Cache Access Path

Spring 2025 ICS Team

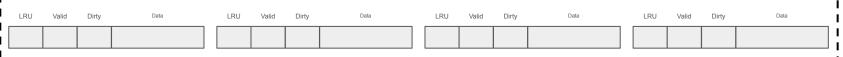
Cache Structure

Cache Line Structure

LRU Valid Dirty Data







L3 (4-way)

b = 20

c = 30

d = 40

e = 50

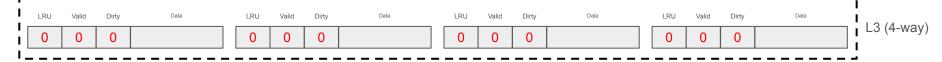
f = 60

Initialize

Tick 0







a = 10

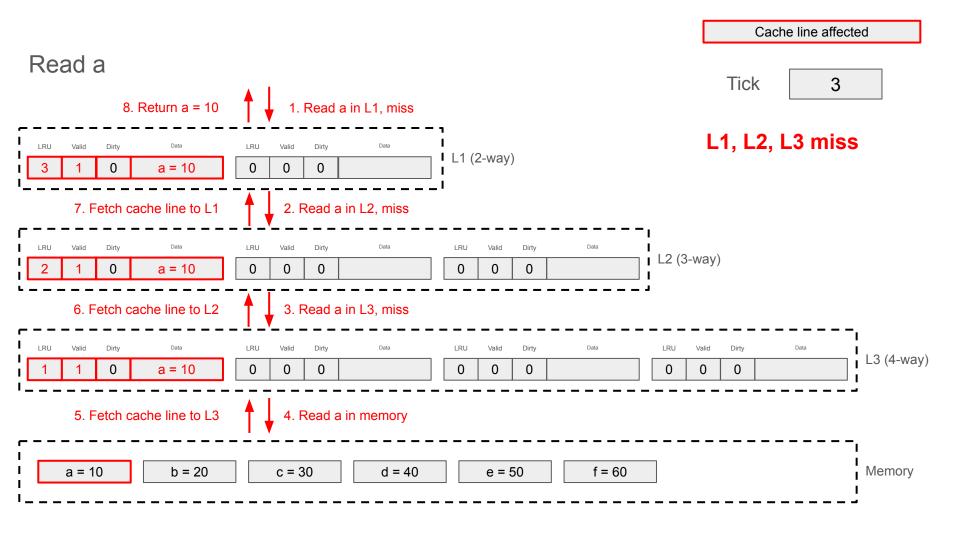
b = 20

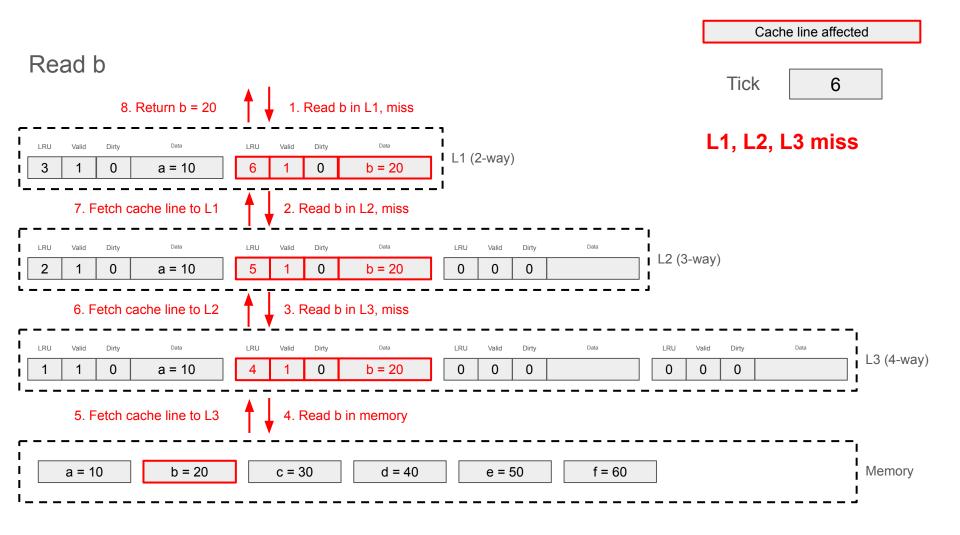
c = 30

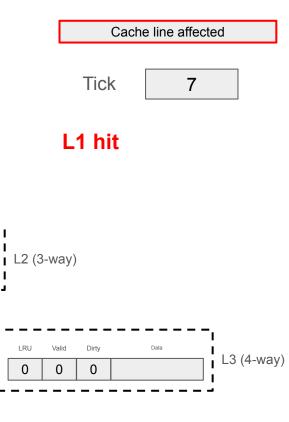
d = 40

e = 50

f = 60







Read a

2. Return a = 10

LRU

Valid

1. Read a in L1, hit

b = 20

LRU Valid Dirty LRU Valid Dirty a = 10 6

I L1 (2-way)

LRU Valid Dirty a = 10

Dirty b = 205

LRU Valid Dirty Data 0 0

Valid Dirty a = 10 LRU Valid Dirty b = 204

LRU Valid Dirty Data 0 0

a = 10

b = 20

c = 30

d = 40

e = 50

f = 60

Write b

2. Write b = 21 and return



1. Write b = 21 in L1, hit

 	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	1 1 4 (2)
i[7	1	0	a = 10	8	1	1	b = 21	L1 (2-way)
l ⁻									1

Tick

8

L1 hit

2	1	0	a = 10	5	1	0	b = 20	0	0	0		L2 (3-wa
LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	i i

vay)

ı	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	ł,
¦[1	1	0	a = 10	4	1	0	b = 20	0	0	0		0	0	0		
L																	

L3 (4-way)

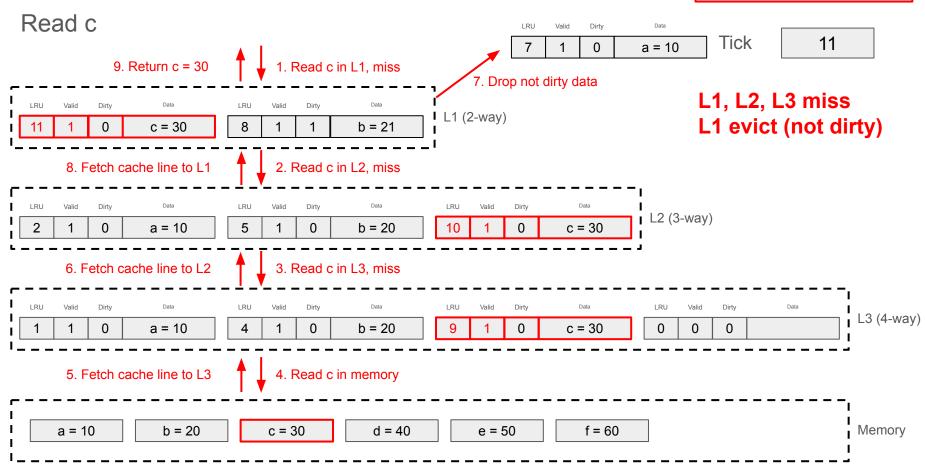
b = 20

c = 30

d = 40

e = 50

f = 60





LRU

Valid

Dirty

5. Write a = 11 and return

1. Write a = 11 in L1, miss

LRU Valid Dirty LRU Valid Dirty a = 11c = 30

LRU

Valid

4. Fetch cache line to L1

a = 10

2. Read a in L2, hit

Dirty

L1 (2-way)

3. Write dirty data back to L2

LRU Valid Dirty

b = 21c = 3010

Tick

b = 21

L2 (3-way)

14

L1 miss, L2 hit L1 evict (dirty) write back to L2

Data

!		Valid		Data	LRU				LRU			Data		Valid	
i	1	1	0	a = 10	4	1	0	b = 20	9	1	0	c = 30	0	0	0

L3 (4-way)

a = 10

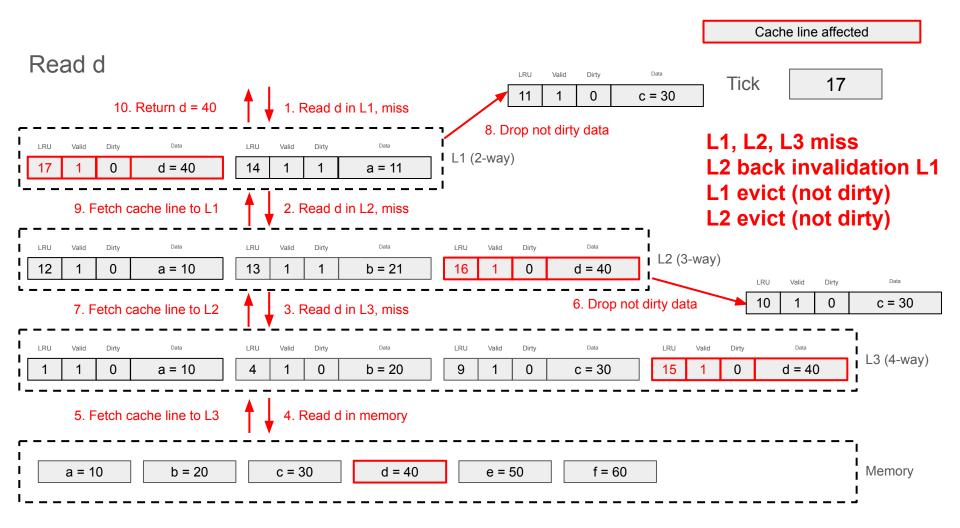
b = 20

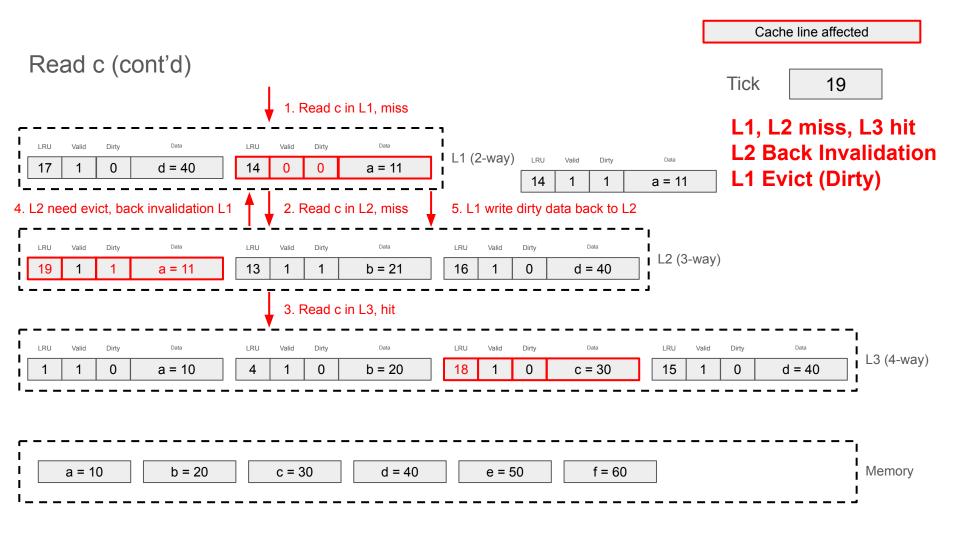
c = 30

d = 40

e = 50

f = 60

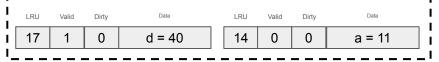




Read c (cont'd)

Tick

20



L1 (2-way)

L1, L2 miss, L3 hit **L2 Back Invalidation** L1 Evict (Dirty) L2 Evict (Dirty)

Data



L2 (3-way)

6. L1	write	dirtv	data	back to	12
O. L.	WITE	unity	autu	Duck to	

Dirty 19 a = 11

			Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	i,
i	20	1	1	a = 11	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40	
L													 				

L3 (4-way)

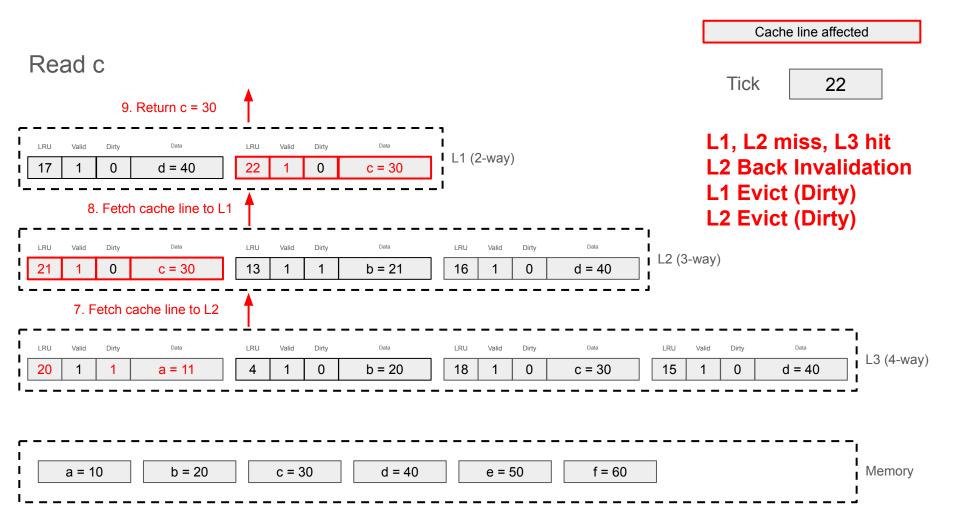
b = 20

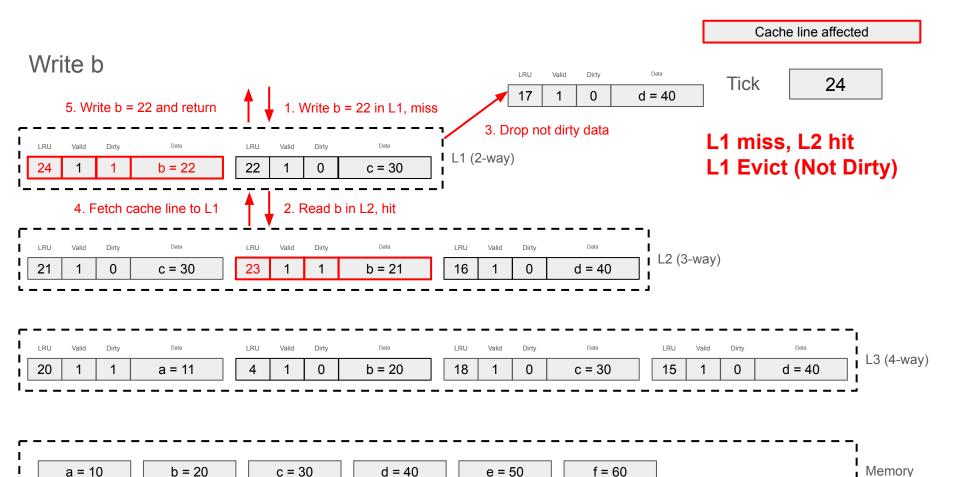
c = 30

d = 40

e = 50

f = 60





Write c

3. Write c = 31 and return



 LRU
 Valid
 Dirty
 Data
 LRU
 Valid
 Dirty
 Data
 I
 L1 (2-way)

 24
 1
 1
 b = 22
 25
 1
 1
 c = 31
 I
 L1 (2-way)

Tick

25

L1 hit

LRU Valid Dirty LRU Valid Dirty LRU Valid Dirty Data L2 (3-way) 23 d = 40c = 30b = 2116

LRU Valid Dirty Data LRU Valid Dirty Data LRU Valid Dirty Data LRU Valid Dirty Data d = 4020 a = 11b = 2018 c = 3015

L3 (4-way)

a = 10

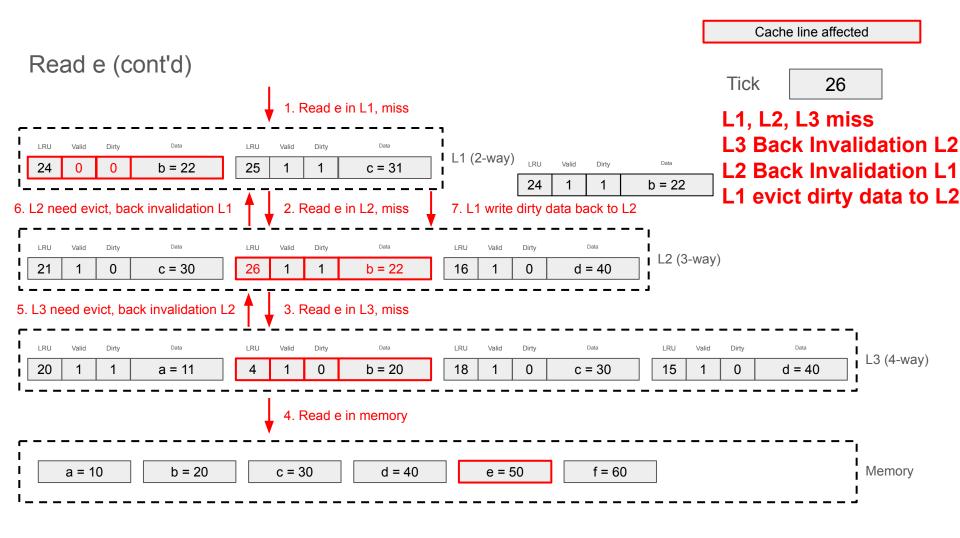
b = 20

c = 30

d = 40

e = 50

f = 60



Read e (cont'd)

Dirtv

b = 22

Valid

24

Tick

27

L1 (2-way)

L1, L2, L3 miss L3 Back Invalidation L2 L2 Back Invalidation L1 L1 evict dirty data to L2 L2 evict dirty data to L3

Data



c = 31

L2 (3-way)

Valid

LRU

Dirty 26 b = 22

	Valid		Data		Valid		Data	LRU		Dirty	Data	LRU		Dirty	Data	i,
20	1	1	a = 11	27	1	1	b = 22	18	1	0	c = 30	15	1	0	d = 40]¦'

L3 (4-way)

a = 10

b = 20

c = 30

LRU

25

Valid

Dirty

d = 40

e = 50

8. L1 write dirty data back to L2

f = 60

27

Read e (cont'd)

 LRU
 Valid
 Dirty
 Data
 LRU
 Valid
 Dirty
 Data

 24
 0
 0
 b = 22
 25
 1
 1
 c = 31

LRU

26

Valid

0

Dirty

L1 (2-way)

Valid

LRU

16

L3 Back Invalidation L2
L2 Back Invalidation L1
L1 evict dirty data to L2
L2 evict dirty data to L3
L3 evict dirty data to Memory
L2 (3-way)

Data

8. L2 write dirty data back to L3

Data

d = 40

Dirty

26 | 1 | 1 | b = 22

Dirty

Valid

Valid

LRU

Tick

L1, L2, L3 miss

LRU Valid Dirty LRU Valid Dirty Data LRU Valid Dirty Data LRU Valid Dirty b = 2220 a = 1127 0 18 c = 3015 d = 40

9. L3 write dirty data back to Memory

27 1 1 b = 22

a = 10

LRU

Valid

Dirty

b = 22

c = 30

c = 30

d = 40

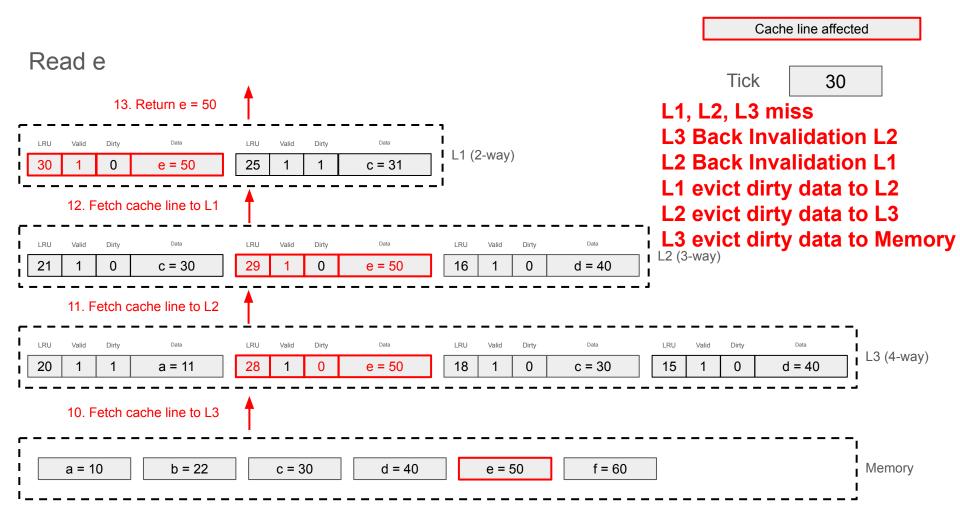
b = 22

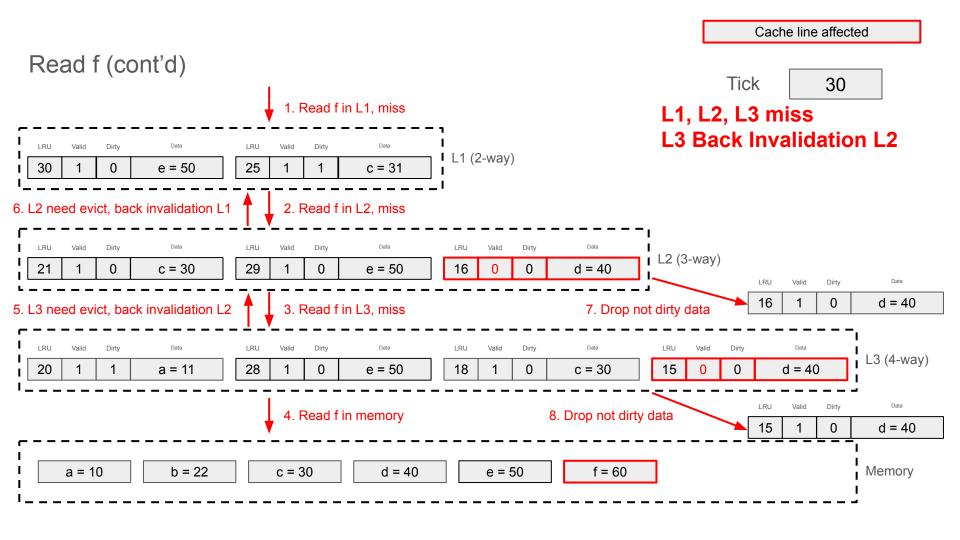
e = 50

f = 60

Memory

L3 (4-wav)







13. Return f = 60

Valid Dirty LRU Valid Dirty e = 50f = 60

L1 (2-way)

12. Fetch cache line to L1

22 4 4 2 - 24	L	Data	DIRTY	valid	LRU	•
33 1 1 C = 31	2	c = 31	1	1	33	

20 1 0 0 = 50	LRU	valid	Dirty	Data
29 1 0 e = 50	29	1	0	e = 50

 LRU	Valid	Dirty	Data
32	1	0	f = 60

L2 (3-way)

a = 11

Dirty

LRU Valid Dirty 28 e = 50 LRU Valid Dirty 18 c = 30

LRU 31 f = 60

a = 10

Valid

LRU

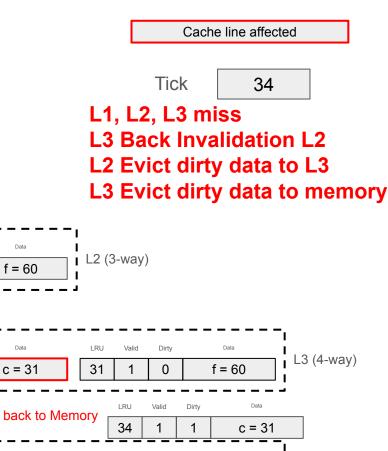
b = 22

c = 30

d = 40

e = 50

f = 60



Read b (cont'd)

Valid Dirtv LRU Valid Dirty 30 e = 5034 f = 60

L1 (2-way)

LRU Valid Dirty LRU Valid Dirty LRU Valid Dirty 29 33 c = 31e = 5032

LRU Valid Dirty LRU Valid Dirty LRU Valid 28 35 a = 11e = 50

8. L3 write dirty data back to Memory

Dirty

a = 10

b = 22

c = 31

d = 40

e = 50

f = 60

