LUBESH KUMAR SHARMA | 22CS30065

B.Tech.(Hons.) in COMPUTER SCIENCE AND ENGINEERING and M.Tech. in COMPUTER SCIENCE AND ENGINEERING

EDUCATION

Year	Degree/Exam	Institute	CGPA/Marks
2027	M.TECH Dual Degree 5Y	IIT Kharagpur	8.84 / 10
2021	CBSE (XII)	Petals International School, Jaipur	95.60%
2019	CBSE (X)	Petals International School, Jaipur	94.00%

COMPETITION/CONFERENCE

Explicit Representations in 4d : A Comparitive analysis with Hexplane | Prof. Debashish Chakravarty **Dec'23 - Feb'24**

- Worked with **6 member** research team to successfully reproduce **CVPR 2023** Paper: **HexPlane:** A Fast Representation for Dynamic Scene
- Conducted in-depth replication of complex **spherical harmonics** experiments, visualized static and dynamic scenes for model insights
- Built highly efficient PyTorch dataloader for large **iPhone dataset**, enhancing overall data throughput and training pipeline robustness
- Integrated temporal loss in training loop, achieving consistent **PSNR of 27** and significantly improving dynamic scene rendering accuracy

WORK EXPERIENCES

Autonomous Ground Vehicle Research Group **Aug'23 - Present**

*Part of the DL and Computer Vision Research Team under **Prof. Debashish Chakravarty**, IIT Kharagpur*

- Worked on autonomous vehicle systems using **F1-TENTH**, learning advanced path-planning algorithms including **Dijkstra** and **RRT**
- Implemented control systems like Automatic Emergency Braking (**AEB**) and **Pure Pursuit** Algorithm in simulation environments
- Developed and tested **RRT planner** within **ROS-based simulators**, ensuring integration with vehicle control and perception modules
- Designed fully functional, dimensioned **robot chassis** in **SolidWorks** with mobility performance validated using **simulation** tools

PROJECTS

Reliable Transport Protocol (KTP) | Course Project | Prof. Abhijnan Chakraborty and Prof. Sandip Chakraborty **Feb'25 - Mar'25**

- Developed a **sequential** transport protocol (KTP) on **UDP** using **C**, implementing a **sliding window** approach with timeouts for delivery
- Built robust concurrent architecture using **Pthreads** and **shared memory** to enable parallel communication between the processes
- Used **mutex locks** and **synchronization** for access to shared structures and prevent race conditions in **multithreaded** environments
- Handled **packet retransmissions**, acknowledgment (**ACK**) messages and adaptive timeouts to ensure reliable delivery across sessions
- Designed shared memory architecture with **garbage collection** to manage socket metadata, ensuring cleanup of abandoned processes

TinyC Compiler | Course Project | Prof. Abhijit Das and Prof. Bivas Mitra **Sep'24 - Oct'24**

- Developed a compiler for a **C subset** (**TinyC**), generating machine-independent **3-address** intermediate code using **Flex** and **Bison**
- Implemented **semantic actions** for expressions, declarations and control flow logic to enable typed translation and code generation
- Designed and managed **symbol tables** and compiler-generated temporaries to ensure precise scoping and **type tracking** across functions
- Constructed a **quad-based** intermediate representation to handle operations including assignments, arithmetic, control and functions
- Integrated **backpatching**, type checking and automatic type conversion to support reliable and efficicent semantic analysis and translation

32-bit RISC Processor Design | Course Project | Prof. Indranil Sengupta and Prof. Sarani Bhattacharya **Oct'24 - Nov'24**

- Designed a 32-bit RISC-like processor in **Verilog, s**ynthesized on **FPGA** using **BRAM** based memory through **Xilinx Vivado & ISE** tools
- Implemented **multiple addressing** modes and instruction types including arithmetic, logic, memory, branch and control operations
- Designed and verified processor components via simulation and **RTL** including hardwired control path and structural **datapath**
- Ran complex programs like division **Booth multiplication** and **insertion sort** on **ISA** and verified correct execution on **FPGA hardware**
- Validated processor functionality on FPGA using **test benches** and demos, covering ISA, instruction formats and control flow accuracy

AWARDS AND ACHIEVEMENTS

- Reached the level **Expert** with maximum rating of **1772** on Codeforces (**Lubesh**) through consistent dedicated practice and contests
- Achieved the competitive **Knight** level on the LeetCode with rating of **1998**, ranking in the top **2.63%** globally (handle –**Lubesh**)
- Earned global rank **361** out of **27,926** in **Educational Codeforces Round 180** (**Div 2**), demonstrating strong problem-solving skills
- Ranked gobally **147th** out of **28,244** participants in the **LeetCode Weekly Contest 455**, showing strong algorithmic proficiency
- Secured impressive All India Rank **6498** in JEE Advanced 2022 among **1.6 lakh** registered candidates, conducted by the **IIT Bombay**
- Achieved commendable All India Rank **9447** in the Joint Entrance Examination (**Main**) 2022 among **10,26,799** appearing candidates
- Secured **department change** to Computer Science and Engineering at IIT Kharagpur among **1900+** peers based on the performance

COURSEWORK INFORMATION

Theory and Laboratory: Programming and Data Structures, Algorithms-I, Software Engineering, Compilers, Switching Circuits and Logic Design, Operating Systems, Computer Networks, Computer Organisation and Architecture, Database Management System, Systems Programming Laboratory
Theory: Algorithms-II, Discrete Structures, Machine Learning, Deep Learning, Formal Language and Automata Theory
Mathematics: Linear Algebra, Probability and Statistics, Advanced Calculus

SKILLS AND EXPERTISE

Languages: C, C++, SQL, Bash, JavaScript, Verilog, MIPS, Assembly, Express.js, ReactJS, Node.js, Gawk, Grep, gdb, Flex, Bison, gprof, Python
Skills: Data Structures, Algorithms, Object-Oriented Design, Systems Programming, Socket Programming
Technologies: ***ML:*** PyTorch, TensorFlow, Keras, Numpy, Matplotlib ***Robotics:*** ROS/ROS2, Docker, Git, Matlab, Solidworks

EXTRA CURRICULAR ACTIVITIES

- Core member of the **Open-Soft backend** team from Nehru Hall of Residence that secured **4th** place in the Inter-Hall **GC - Tech** event
- Successfully completed the **Health &Fitness** training course with **100%** attendance (**98%+** avg.), awarded for dedication and discipline
- Actively participated in **Socult Night** organised by Nehru Hall of Residence, performing in multiple vibrant and diverse cultural segments
- Participated in multiple Intra-Hall General Championship socio-cultural events, showcasing creativity and involvement in hall activities

!Self declared by the student, CDC could not verify the relevant documents