POWER ELECTRONICS (5th semester E&E)

UNIT-I

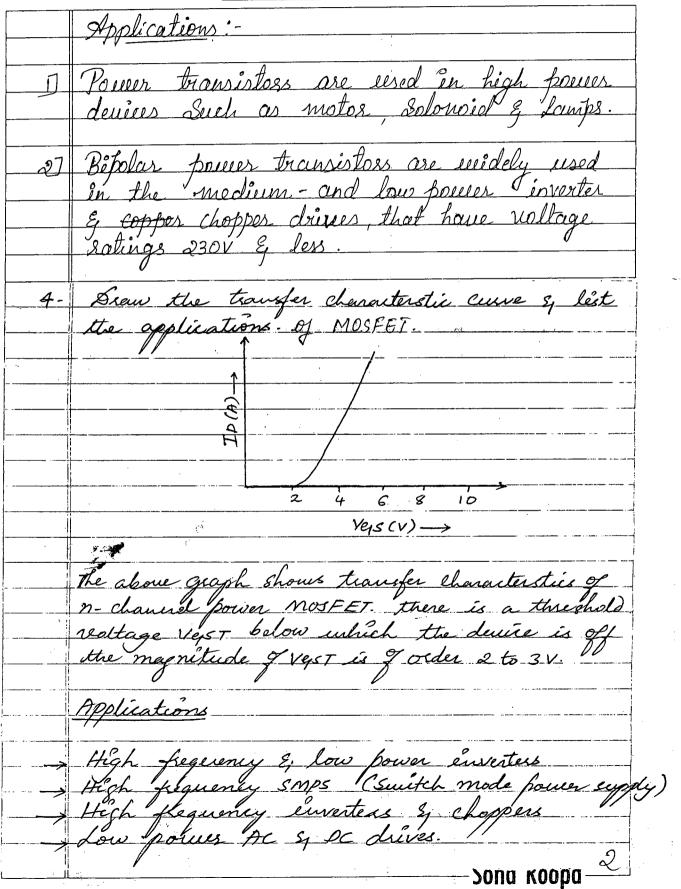
STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

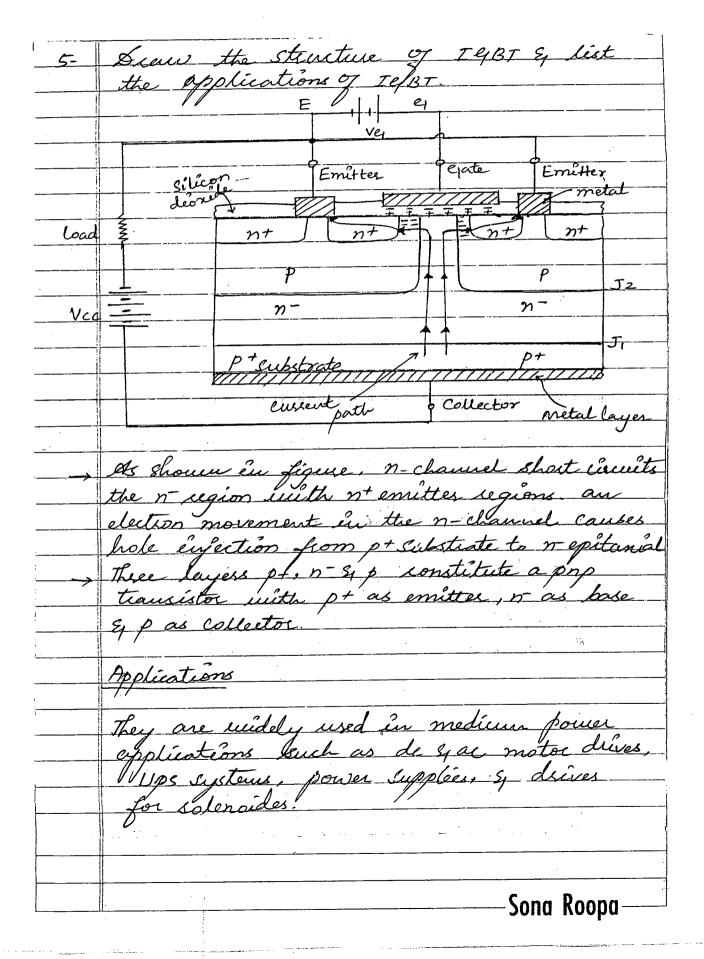
1-	Leaw the layered struck	tue of pouer déode.
	Deaw the layered struck	g Anode (A)
Aus:		
	7	p+ 10 ¹⁹ /cm³
	here are twee regions n+Substrate	n drift region
	n- drift region	1014/cm
3-	pt region	nt substeale 189/cm3
· · · · · !		
\rightarrow	n+ substrate is heavily	cathode(K)
<u> </u>	doped with doping leve	Lg 10/cm Jours
	Called & The acodo	
	is called dift reprior u	ith doping level of 10"4 km
	lightly doped no epitan is called duft region u on junction is formed	by diffusing a
	heavily doped pt region	p+ region forms
. <u></u>	heavely doped pt region ande of the diode.	
	The deliver lovel of pt	0002m in 1019/cm3
	The doping level of P+ region	in in Man.
>	The thickness of nt See	billate is 250 Mm.
->	The thickness of o drift	layer depends upon
	the broakdness rollage of	dode
· · · · · · · · · · · · · · · · · · ·	V V	
<u>2-</u>	Lest types of fourer	diales & thees
i :	applications	
Auc:	There are three types of	pouver déodes
	- esemenal purpose décdes	
	2- Fast seleoury deades_	
· :	3- Schotty diddes	
	•	Song Roong

-Sona Roopa-

	Applications of three types of diodes
	general purpose divode:-
	These dindes, have high severse secovery line
	These diodes, have high severse secovery line of 25 Ms. These are eased in battery charging, cleitric traction, electroplating, enclosing of power Supplies.
	pour Supplies.
	Fast seeouery déodes:
	These diodes have low sovesse seconery line
	These diodes have low sovesse seconery time of 5 Ms. These are used in choppers, communication circuits, switches mode forcer supplies, & induction hoating.
	induction hoating.
	Schotty diodes: -
	The applications of Schotly diode includes high. Juequeency instrumentation & Seul Switching power Supplies.
	presel Supplies.
3.	List types of power bransisters & their applications.
	There are three types of from transmitters:
IJ	Bipolar junction transister (BII).
2]	Bipolar junction transister (BII). Métal oride Semiconductor, field expect transister
	(MOSEET)
-21	Insulated gate bipolar transister (IGBT)
نا,نا	Sona Roopa——

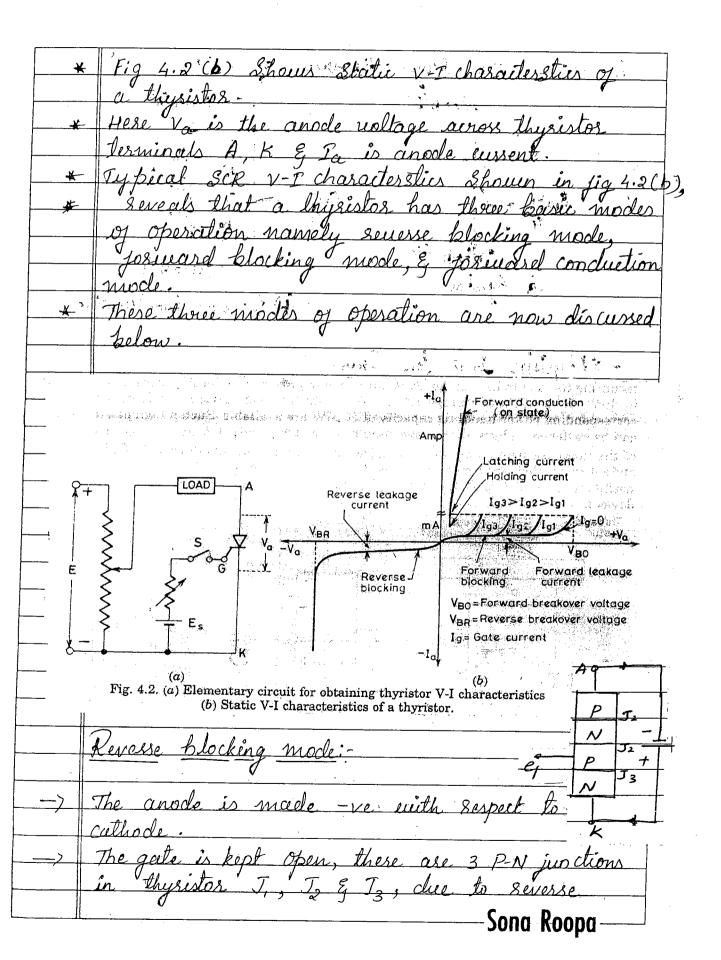
STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	<u></u>





STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

6. Dears the	layer diagram	of GLR.
——·	Anode(A)	Anode (A)
	7	P J
Crate o	Crate o-	N J ₂ P J ₃
(4)	(d)	I N Jos
a Garan	hode (K)	Cathode (K)
G 7 jul	6	Internal Construction
- Thursday &	a four lever three	e junction, P-n-P-n
i hemiconau	tor ownthank ac	vice.
- If has th	ues terninals. Ano	de cathode & Gate.
- 1 is p-	type & n-type Bill here junctions J1	T T
I the tourser	ioil commuted to ou	itel b-region is
called ano	de (A), the termina	cathode and that
commented	o inner b-region	is called the gall (4).
- An SCR.	is so called because	bilicon is used
for its co	notruition and it	En the townered
rectifier C	and very high A	estitance in the
reverse d	very low rest touce and very high r erection) can be	controlled.
	:	
1] Enumente	severse blocking	Foseward blocking
forward	conduction mode.	Foseward blocking
[OR. Statie V-I (USK e SCR.	or charceterstie
CHAVO	SCR:	V
The state of		———Sona Roopa 3



STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

The state of the state of

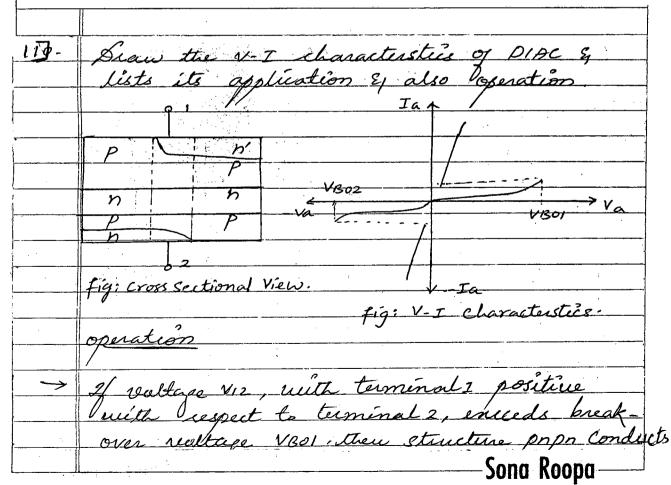
	Sona Roopa- ²
	2
(iv) julieu gate cattrode junition	is emposed + lide +
_ dt	solbik dalle
- Ciji when die encede des	11.°610 -2-0.
- (ii) when gate drive is applied)
- 11) when Wak > 100	,
- there it can go ento for	sand Conduction
uchen the thyrestor is of	orward biasel.
- Forward conduction mode	
_ this current is called form	and leakage current
lusent flows Low ando	to Cattanta
is to be hold by junction	T2 C. 11
_ Ji & T3 are forward brased	y J2 is
J. & T : are forward bease	d the junition
awith supert to cathode	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
ande is made positive	e, P J3 -
forward brased when	
-> The thypistor is said to be	P T, N T, +
Forward blocking mode	A
(Taria) [/a/2] = a/a	A
ealled severse blocking ma	de -
severse leakage current sythic	s male is
catterde to anode. This cure	it is called
severce biase Small current	flows from
Ex junction Iz is forward to	mased. The
	· · · · · · · · · · · · · · · · · · ·
biased junction I, & T3 are also	Reversed biased.

lest its applications Applications are used for low power large used jos high-performance drive Systems, Seich as the field-oriented of Scheme used in Solling mills, sobolics Used for traction peurposes because of their adjestable frequency inverter drives Draw the layered diagram of TRIAC & Application MT2 Main termina (MT1) 'N' (4) a) Symbol terminal(2) N2 b) SCR equivalent. fig: TRIC eymbol considered as on

STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

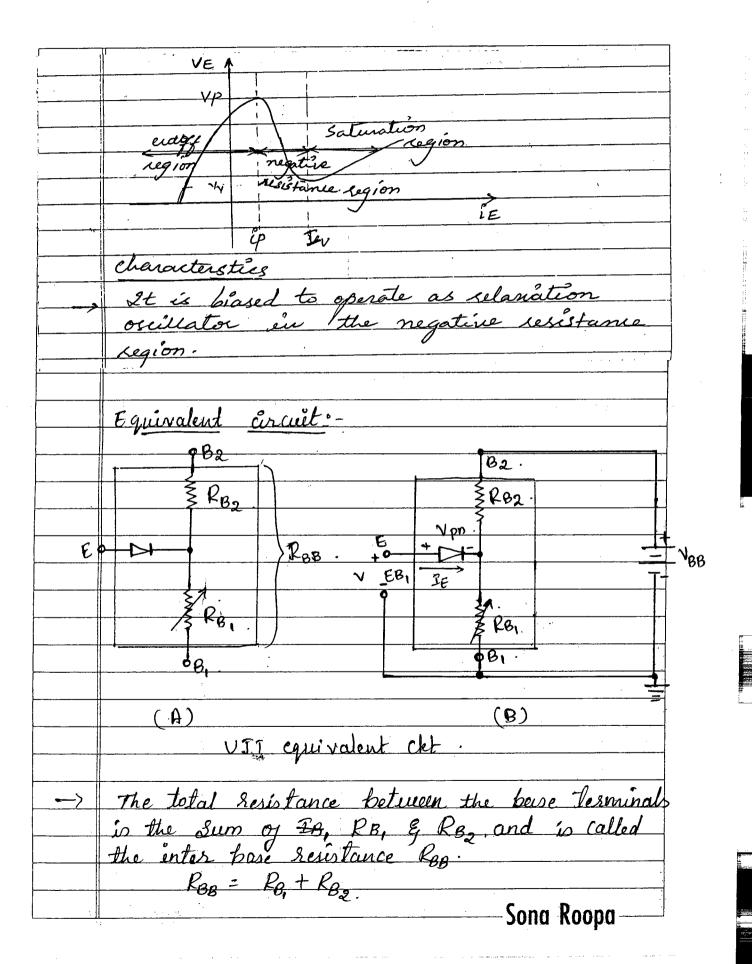
	TRING in the word desired by combining
	1 a stal letter leave the words TRIOGLE
	TRIAC is the word derived by combining the capital letters from the words TRIOCLE
	E AC.
<u> </u>	The Circlet of Symbol & its Charletessias on
	Shown en figure (a) & (b) sespectively.
<i>一</i> >	de the TRIAC can conduct in Both the directions
	The circuit of Symbol & its Charactesstics are Shown in figure (a) & (b) sespectively. As the TRIAC can conduct in both the directions. The Terms anode & cathode are not applicable to
ļ j	1KIHC,
>	The 3-lesminals are usually designed as MT, (main terminal 1), MT2 and the gate by G,
	(main terminal 1), MT2 and the gate by G,
	as in thyristos.
,	
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
	OMT2 $ \begin{cases} MT2 & \text{positive} \\ I_{g2} > I_{g1} > I_{g0} \\ I_{g2} = I_{g1} & I_{g0} = 0 \end{cases} $
	The state of the s
	Vo. √Vo. √VBO2
	Go Va VB02
	→ Ig0 -Ig1 -Ig2
·	MT2 negative
	(a) (b)
<u> </u>	Fig. 4.47. (a) Circuit symbol and (b) static V-I characteristics of a triac.
	1.11. 1.
	Applications:-
	1 1 l l antial links Control
	TRIAC'S are used for heat control, light control
	TRIAC's are used for heat control, light control motor control, & lamp dimmers.
	Sona Roopa <u>5</u>

10-	State	the pr	exerced:	modes	of tun-on of TRIA
Aus:	State the prefessed modes of turn-on of TRIAC operation.				
					Current flow path.
	l I	('	1	l t	
	1	positive	positive	Wegatiu	e Min to Min - (P,-N,-P,-N,)
	111	·	l		$\begin{array}{c c} (P_1 - N_1 - P_2 - N_2) \\ \hline (P_2 - N_1 - P_2 - N_2) \end{array}$
	111	·			
	3	Negative	positive	Negati	(P,-N,-P,-N2)
	4.	Negatine	Negative	positie	
	1)				
	Modes	1940	re ejjícien	t mod	Sona Roopa



STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS.	SUBJECT	
ROLL NO.	DATE	

	If terminal 2 is positive with sespect to theminal 1. & when vs exceeds break-over
	theminal 1. Ex when VI exceeds bleak-over
	realtage VB02, then structure papa' conducte.
	8
	V-I charecteratio
	DIX has symmetrical breakdown character
	sties, its leads are enterchangeable.
	Its tun-on voltage is about 30V.
	when conducting, arts like a low
	resistance with about 3v drop ourossit
	when not conducting, acts like an
	open suitch.
j	<u> </u>
	End: H. UTT construction laword
lac.	Explain the UTT construction, layered diagram & lists its applications.
,	aragram 4 mm
Aus:	B ₂
	
P-	Type 3 RB2 E
i	
	E PBI
-	RBI OBI
	n-type B1
	Au UTT is made up of au n-type Silecon
	base to which p-type limitter is embedded.
-	It has 3-terminals, emitter E, base-one B2,
<u> </u>	Ey base-two B2
	Between B, E, B2, the uniquention behaves
	Ilke an ordinary sesistance.
	RB1 & RB2 are the enternal resistances
	tari da



STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

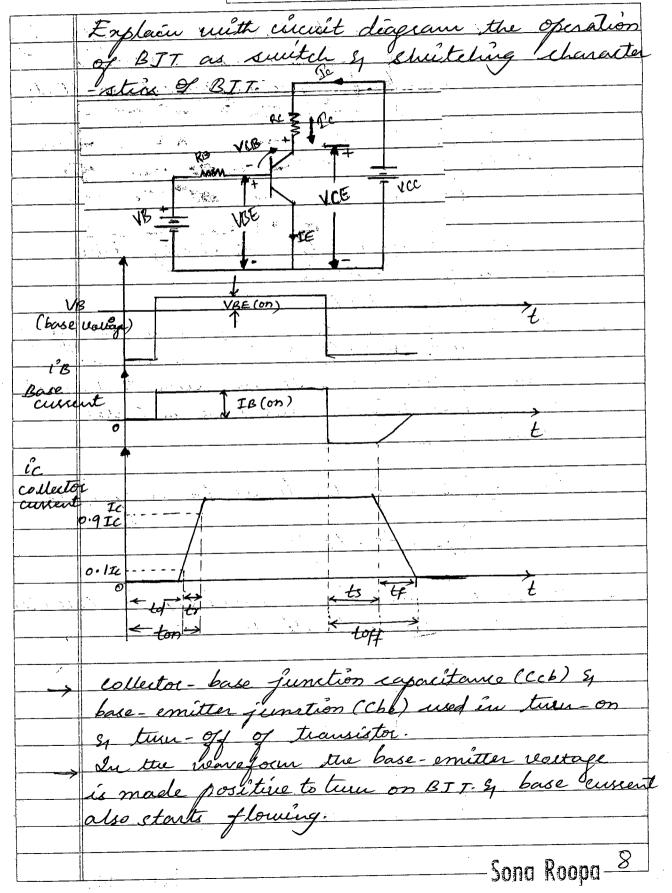
->	The noltage across the resistance RB, can be expressed as
·	expressed as
	$V_{RB} = \frac{R_{BL}}{R_{BB}} \times V_{BB}$
	$\mathcal{R}_{\mathcal{B}\mathcal{B}}$
	Stand off ratio:
<u>ー</u> >	Intrinsic stand of ratio is a UTT characterstic & is designated by n (excel eta)
	& is designated by n (egreek eta)
	$\frac{\eta = R_{B,1}}{R_{BB}}.$
	Rao.
	
	UTT Applications:
	/
	Trigger device for SCR's & TRIAC'S. Non-Sinusodal oscillators.
	Non- Sinusodal oscillators-
*	Sawtooth generators.
#	Phase control.
	Timing Concrits.
7	Tining Cercuits.
·	
<u> </u>	
, s'	
	C D 1
1	Song Roopg

UNDERSTAND. working on the principle of electrons but rested at power level rather the ciqual level. in one form -> Figure Shows the basic Junctioning of power electronic System. -7 The electric energy en one josm is given at

the inpert.

-7 The power electronic System convert the electric
energy into other josm. Sona Roopa

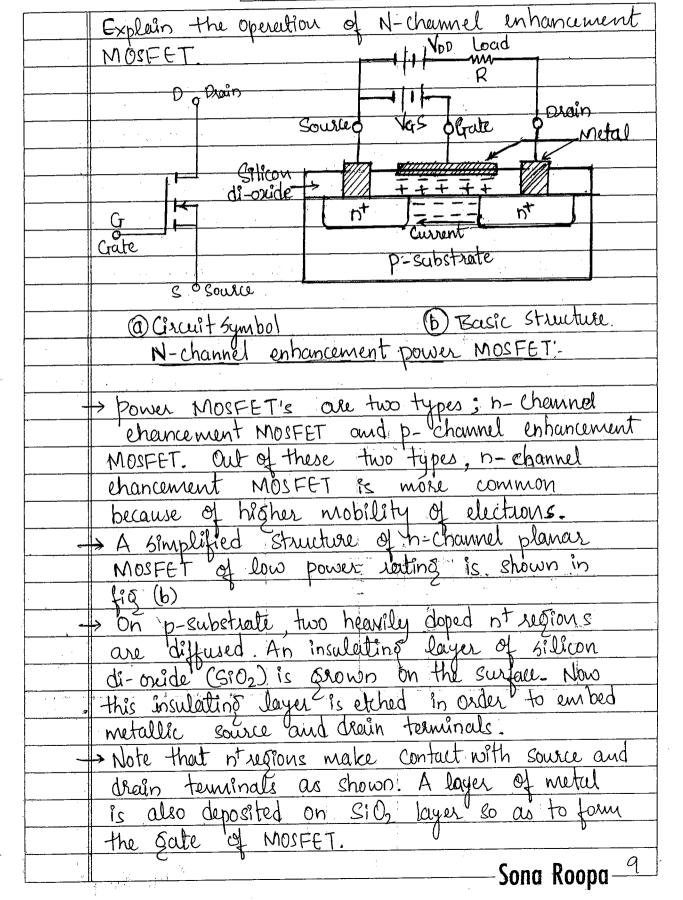
STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

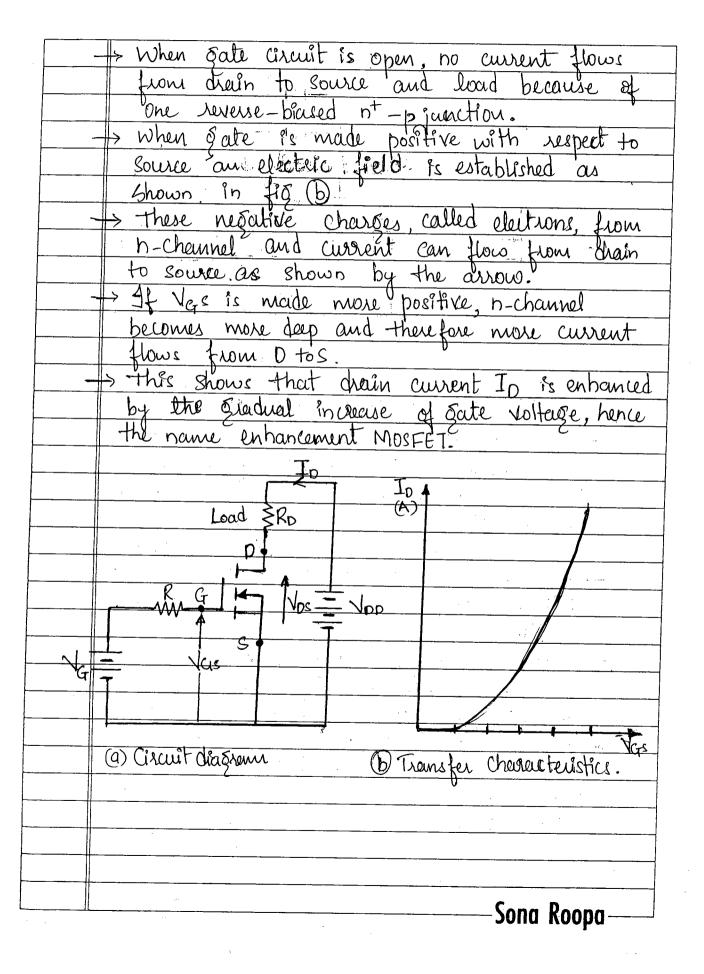


	the collector suscent does not start flowing
	as soon as base deine is applied becouse
	the collector-base function copacitance Starts
	Changing unben base deine is applied.
	delay time (td): time delay engelved when
	base deine is applied.
	base deine is applied.
-	tr (rise time) is time required to raise
	collector current to its steady state.
	turn on time (ton) is
	ton = td +tx
	for turn of the transistor, base resitage
	is made negative & base current is
	also negative, & collector current does not
	Change for time to this time is called
	Stordge time
	•
-	turn of time of the transistor is equal to
	Laco la la
	toff = ts + tf
>	If is the fall time required by the Collector
	current to decay to it 10% value
·	
	Cong Doong
	Sona Roopa

しい アンドラー 一丁芸芸 地元の名 動物機

STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

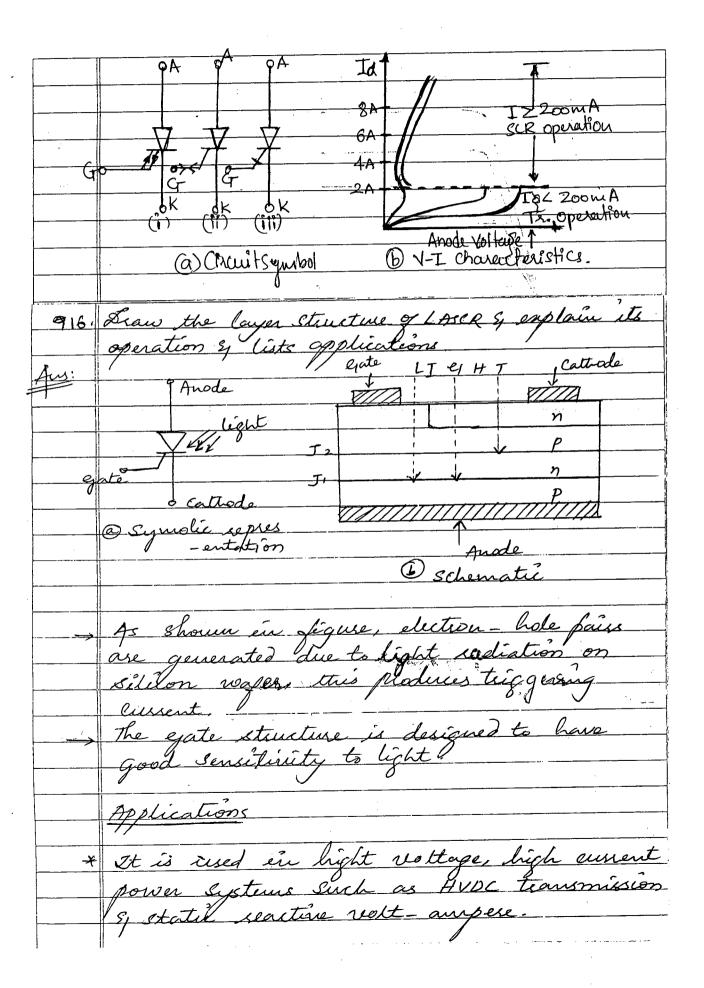




STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO:	DATE	

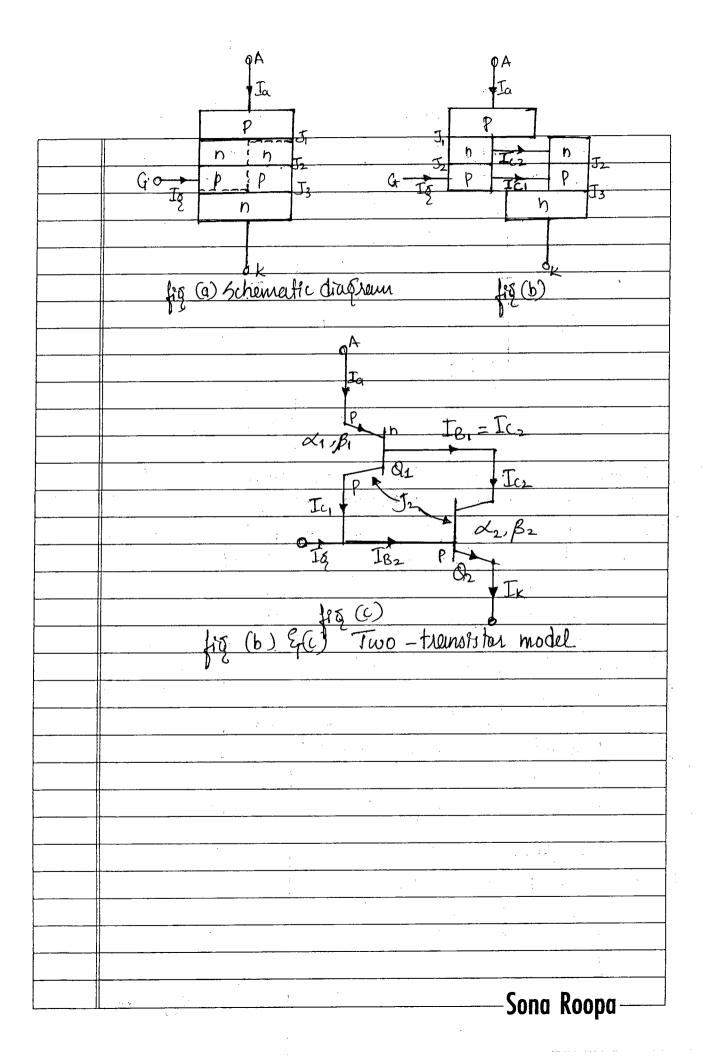
a control of the cont

4
Vast>Vas6>>Vast
Vasc
VG65
S VGS4
VG\$4
√US 2
VG ≤1
Drain Source Voltage Vp; > Vps
© Output characteristics.
C) Output Characteristics.
Explain the principle of operation of GTO.
Costa tura all (GTO) Thrusetne a baba device, com
be turned on like an ordinary thyristor by
be turned on like an ordinary thyristor by a pulse of positive gate current.
Investor and Chopper Circuit a Thylistor Can be
turned Off by forced Communitation. For such applications, a GTO is, however, a more versatile
applications, a GTO is, however, a more versatile
• • • •
-> It can be easily turned off by a hegative
gate pulse of appropriate amplitude.
Fig (a) gives the circuit symbols of a Gio.
device; 1 -> It can be easily turned off by a negative gate pulse of appropriate amplitude. -> Fig @ gives the circuit symbols of a CTO. The Symbols shown in @ (i) and (ii) are self explanatory, gate current can go in for turning on and out for turning off. But the symbol a (iii) tooks easy when circuit Configurations using GTO: are to be drawn.
explanatory, our current can go in for
Has a walson a City tools again without finalit
Contiguations using father are to be drewn.
Confidentions owned die
Sona Roopa
Sona koopa



STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	SUBJECT	
ROLL NO.	DATE	

	Drew the layer diagram of GCR and		
		explain the concept of two transistor analogy.	
		9 Anode (A)	
		P	
		Z C M	
	٧.	Gate o P	
		(G) N	
		Ceithode (K)	
		(a) Symbol Couthode (k)	
3		(b) Internal construction.	
ago.			
3	>	Thysestor is a four layer, three junction, P-n-P-n	
ತ		seluiconductor switching device.	
300	2 -	It has three terminals, anode, cathode & Gate.	
4	3)-	It is p-type & n-type bilicon semiconductor	
/	,	fouring three junctions J. J. J.	
	1)-	The principle of thysistor operation can be explained with the use of the two-teensister model.	
رجي _		with the use of the two-themsister model.	
box)	2)-	Fig (a) shows schematic diagram of a thyristor.	
₽		From this figure, two-transister model is obtained	
		by bisecting the two middle layers, along the	
15th		dotted line, in two seperate halves as shown	
Act 2 shows		in fig(b)	
3	3)-	In figure (b), junctions $J_1 - J_2$ and $J_2 - J_3$ can be considered to constitute prop and upn	
		can be considered to constitute prop and riph	
\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		The Govern to How of the trong to the	
•	9	transistor beperately. The circuit representation of the two-transistor model of a thyristor is shown in fig (c)	
-	-	Moder of a man in Air co	
-			
1		Song Roopa 11	

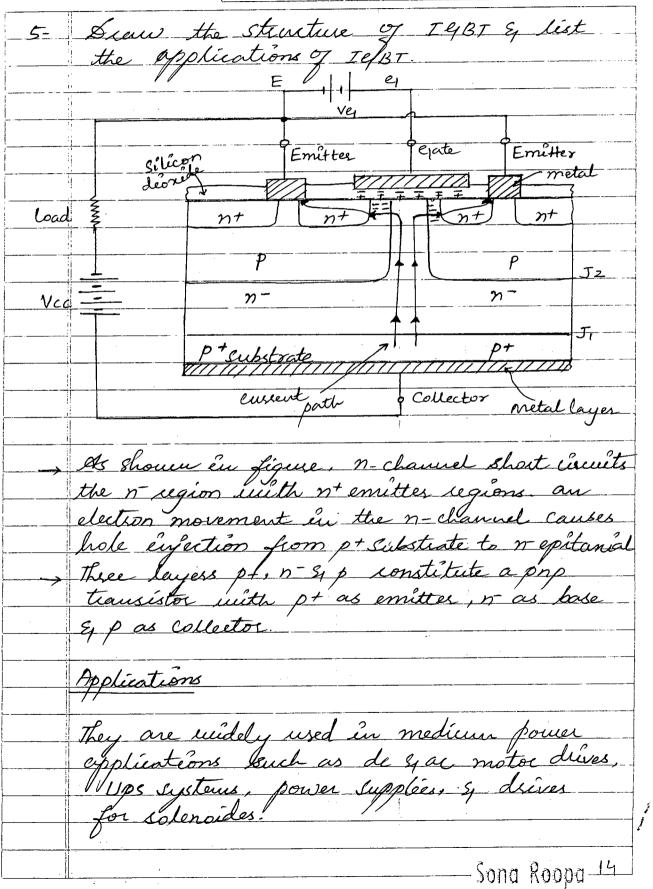


and the second s

The state of the s	
148 Enplain V-I Charactersties of power diade	
* when anode is positive with respect to Cattrode, diode is said to be forward biased.	
Cattrode, diede is wild to le	<u>o_</u>
biased.	
with england ? Source with a in 1	
Zeso value, initially diode custent is zes	22
Lom Vs = 0 to Cut en realte a the	2
from 15=0 to cut en voltage, the forward diale current is very small.	
Beyond cut-en voltage, the diode current	
siles la sidly & 15 9 2 21 +	
siles sapidly & décde is said to condus & cut en realtage is around 0.7 V.	t.
then Catterde is positive with respect to	
angle, the diede is soil of	
biased en this small leakens	se_
biased en This Small leakage sussent flour	<u> </u>
Anode Cottode Anode P D Cottod C	
p n g cattrod	
Vs Vs	
Ø P-n junction & Diode Cymbol.	
IŢ	
1 forward	
realtige drop	
Reverse /	
VRRM & current	
Vs	
Cut-en maltra	
Designed - C. 4V	
breakdown	-
Pain D.	,
- Fig. V-I charactersties : Sona Roopa la	

Sian the V-I characterstice of PIAC & lists its application & also Poperation fig: Cross Sectional View. fig: V-I characterstics. restage VB02, then structure papa' conducts V-I characteratic - on realtage is about onducting, crete like a when not conducting open suitch Sona Roopa —

3 FUDENT'S NAME		FOTAL MACKS OBTAINED
CLA33	SUBJECT	
ROLL NO.	DATE	



	15 10.	Lest the diffe	erence between Mo	ISFET, BJT & IQ	BT
	1	WEL MOSFET		IGBT	
1		recitage - operated		voltage control	
			-tled Levice	deine	
2	- A na	gligible current	It needs an appre	A small cussent	- is
	Cont	tool terminal to	control current for keeping it in one stat	terminal to ma	trol Lintain
	mo	entain en ON-state	Keeping at en ON. Stat	e et en ON-state	2
3-	Its	suitching speed	It's cuitching speed is lower than MOSFE	Its suitching:	speed
4 –	The co	usent sy realtage	ago ectines me his	the current sq	realta
			the current syrealt age ratings are high than most ET	those of mo	FET
5-	ON-Sta	te realtage drop	ON-State realtage	ON-State realta	ige
,	BIT	gher than the	ON-State realtage drop is lower that the MOSFET	- deep is men	Le.
ļ					
					r
}					
-					
\ [-Sona Roopa	

טעטעע אווטכ

SCR Control Circuits

Power Electronics

Methods to Turn-ON SCR

Thyristor can be turned on by following:

i) Forward break over voltage

- ii) $\frac{dv}{dt}$ triggering \smile
- iii) Exceeding internal device temperature
- iv) Focusing light beam on the junction
- v) Gate triggering.

The gate triggering is the most widley used method of turning on the thyristor.

Functions to be Fulfilled by Gate Drive

The gate drive has to satisfy the following requirements:

asmeen.

- i) The maximum gate power should not be exceeded by gate drive, otherwise SCR will be damaged.
- ii) The gate voltage and current should be within the limits specified by gate characteristics for successful turn-on.
- iii) The gate drive should be preferably pulsed. In case of pulsed drive the following relation must be satisfied:
 - (Maximum gate power \times pulse width) \times (Pulse frequency) \leq Allowable average gate power
- iv) The width of the pulse should be sufficient to turn-on the SCR successfully.
- v) The gate drive should be isolated electrically from the SCR. This avoids any damage to the trigger circuit if in case SCR is damaged.
- vi) The gate drive should not exceed permissible negative gate to cathode voltage, otherwise the SCR is damaged.
- vii) The gate drive circuit should not sink current out of the SCR after turn-on.

Pulsed Gate Drive

Instead of applying a continuous (DC) gate drive, the pulsed gate drive is used. The gate voltage and current are applied in the form of high frequency pulses. The frequency of these pulses is upto 10 kHz. Hence the width of the pulse can be upto 100 micro seconds. The pulsed gate drive is applied for following reasons (advantages):

- (i) The SCR has small turn-on time i.e. upto 5 microseconds. Hence a pulse of gate drive is sufficient to turn-on the SCR.
- (ii) Once SCR turns-on, there is no need of gate drive. Hence gate drive in the form of pulses is suitable.

- (iii) The DC gate voltage and current increases losses in the SCR. Pulsed gate drive has reduced losses.
- (iv) The pulsed gate drive can be easily passed through isolation transformers to isolate SCR and trigger circuit.

多数 Gate Turn-On Methods

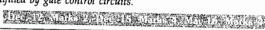
Gate triggering is the most convenient method of triggering the SCR. Various methods are listed below:

- i) R-firing circuit
- ii) RC-half wave firing circuit
- iii) RC-full wave firing circuit iv) UJT triggering circuit

2-3

Review/vallesimis

- 1. State various methods of turn-on of SCR. Methods in the state of th
- 2. List various gate turn-on methods of SCR.
- 3. List the general functions to be fulfilled by gate control circuits.



General Layout Diagram of Firing Circuit

The triggering circuits are called firing circuits. We have already discussed the requirements of gate trigger circuits. The following features or requirements must be fulfilled by the firing circuit in addition to those discussed earlier.

- The firing circuit should produce the triggering pulses for every thyristor at appropriate instants.
- ii) The triggering pulses generated by the control circuit need to be amplified and passed through the isolation circuit. The triggering pulses generated by the control circuit have very small power. Hence their power is increased by pulse amplifier. Fig. 2.2.1 shows the scheme. The firing circuit operates at low voltage levels (5 to 20 volts). And the thyristor operates at high voltage levels (greater than 250 volts). Hence there must be electrical isolation between firing circuit and thyristor. This isolation is provided by the pulse transformer or optocouplers.

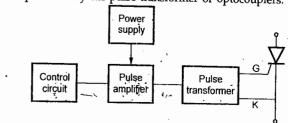


Fig. 2.2.1 Main blocks of firing circuit

I. Draw the general layout diagram firing circuit and explain it.

noiteau© waiva?

'A' and 'B' gate voltage is same. angle of T₁ cannot be delayed beyond 90°. In the above waveforms, observe that at points The anode to cathode voltage and the gate current are in phase. Hence the triggering

5-5

90°. This is because the gate current and anode voltage are in phase. Hence thyristor will turn-on at point 'A' only. Hence maximum triggering angle will be If it is desired to trigger thyristor at point 'B', similar voltage appears at point 'A'.



Explain briefly the simple resistance triggering circuit.

With a neat sketch and waveforms explain working of R-firing circuit.

TATER TO DESCRIPTION OF THE WEST SESSION SECTIONS

AND IN TO 10 DOC 12 12

COMPACT STATE

RC Firing Circuit

maximum firing angle), the following relation holds: thyristor. The triggering angle can be controlled from 0 to 180°. For zero output (i.e. Fig. 2.4.2. The diode D₁ prevents the negative capacitor voltage appearing to gate of the greater than $v_{g\,({
m min})}$. Observe the capacitor voltage and load voltage waveforms in positive half cycle of the supply. The thyristor triggers when capacitor charges to value capacitor then discharges (i.e. charges towards positive) through resistance R during the -1 V_m (i.e. negative peak) of the supply. This is shown in waveforms of Fig. 2.4.2. The capacitor charges through diode D_2 to negative supply voltage. The capacitor charges to Fig. 2.4.1 shows the circuit diagram of RC-firing circuit. In the negative half cycle, the

(I.4.2) ...

 $RC \ge \frac{1.3}{25}$

Fig. 2.4.1 RC half wave firing circuit

the supply, this circuit is also called half wave RC firing circuit. Here f is the supply frequency. Since triggering is controlled only in one half cycle of

A DECEMBER 1 SECTION OF THE SECTION

Anna Garteshiy & Sahahi bi sed

Firing Circuit

supply voltage, then Rmin will be, gate current to its maximum value. If $I_{g\,({\rm max})}$ is maximum gate current and V_m is the peak The resistance R_{min} is used to limit the Fig. 2.3.1 shows the simple K-firing circuit.

shows the waveforms of this circuit.

 $\frac{m^{V}}{(xem)_{8}I} \leq \min_{m} \Re$

Fig. 2.3.1 R-firing circuit

rosq

angle is minimum. The triggering angle increases as value of 'R' is increased. Fig. 2.3.2 variable resistance R is used to trigger the thyristor T_I. When 'R' is zero, the triggering exceed minimum gate voltage $(V_{g\,(min)})$ otherwise thyristor will turn-on directly. Then the resistance. The voltage across R_b should not The resistance R_b is the stabilizing

Fig. 2.3.2 Waveforms of R-firing circuit

TECHNICAL PUBLICATIONS - An up thrust for knowledge

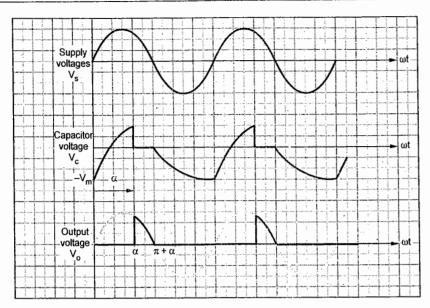


Fig. 2.4.2 Waveforms of half wave RC firing circuit

Review Question

1. Draw RC-firing circuit and explain its operation with waveforms

2-6

May 12 Marks: Dag-16 Marks: Marks Marks Marks 12 Marks Marks Marks C. Marks

Full Wave RC-Firing Circuit

Fig. 2.5.1 shows the full wave RC-firing circuit. The supply to the thyristor is given through the uncontrolled rectifier. Hence both the half cycles are positive half cycles to the thyristor. The capacitor starts charging in every half cycle at the beginning. Whenever the capacitor voltage reaches to the value greater than

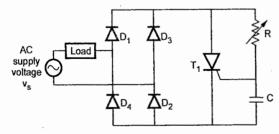


Fig. 2.5.1 Full wave RC firing circuit

 $v_{g(\min)}$, the thyristor turns-on. Fig. 2.5.2 shows the waveforms of this circuit. Once the thyristor turns-on, the capacitor voltage is clamped to zero, till next half cycle. The capacitor again starts charging from zero. The firing angle can be varied from 0 to 180°. The triggering is controlled in both the cycles. The following relation holds for maximum firing angle,

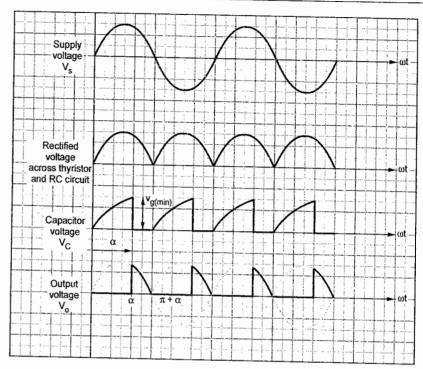


Fig. 2.5.2 Waveforms of full wave RC firing circuit

$$RC \geq \frac{0.157}{2\pi f}$$
 ... (2.5.1)

Here f is the frequency of the supply.

Review Question

1. Explain full wave RC firing circuit with the help of circuit diagrams and waveforms.

Question Bank

Unijunction Transistor (UJT)

Principle of UJT

It has N-type bar. A P-type region is alloyed into one side of this bar. It forms one p-n junction. Hence it is called uni-junction transistor.

- It starts conducting when certain voltage is reached at the emitter. It operates in negative resistance region of the current-voltage characteristics.
- This negative resistance characteristic makes UJT to act an relaxation oscillator.

6~2

- UIT turn-off : When the emitter current is less than valley current (I_V) , the UIT
- turns-off. Thus valley current acts like holding current for the UJT.

263 UJT Relaxation Oscillator

Power Electronics

- UT is off at this time. oscillator. The capacitor 'C' is charged through resistance 'R' from zero voltage. • Fig. 2.6.4 (a) shown the circuit diagram and waveforms of the UIT relaxation
- Hig. 2.6.4 (b). connected to UJT. The voltage across \mathcal{R}_1 is v_0 . The waveforms are shown in discharges through emitter, B_1 and R_1 . Note that R_1 is external resistance When capacitor voltage is equal to V_p, the UTT turns ON. The capacitor

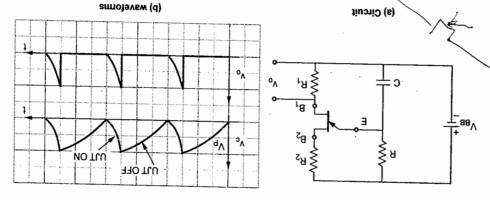


Fig. 2.6.4 UJT relaxation oscillator

capacitor starts charging. Then the cycle repeats. Hence this circuit is called As the capacitor discharges to valley voltage V_v, UIT again turns-OFF and

• The voltage V_p is given as,

 $\Lambda^b = \Lambda^x + \Lambda^D$

(Here $V_x = \eta V_{BB}$) ((d) E.E.S. Giff see See Fig. 2.5.3 (b))

 $a_{\Lambda} + aa_{\Lambda} u =$

TLU 101 erameters for UJT

1. Intrinsic stand-off ratio (ŋ): 0.56 to 0.75 Following are the typical parameters for UIT:

Construction, Working and Characteristics of UJT

8-5

emitter and N-type bar forms a PN junction. • Fig. 2.6.1 shows the construction and equivalent circuit of UJT. Observe that

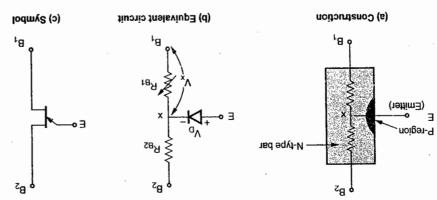


Fig. 2.6.1 Unijunction transistor

• UIT turn-on : When the voltage at since it changes in on and off states of В2 RBZ and RBI. Note that RBI is variable resistance of the bar is represented by • As shown in Fig. 2.6.1 (b), the internal

.2.6.2 .gi^H the bias voltage of UIT as shown in called intrinsic stand-off ratio. VBB is turns on. Here $\eta = 0.63$ typically is point x increases above η V_{BB}, UT

point A and B of the characteristic. Fig. 2.6.3. It is the region between resistance region as shown in further. This forms a negative same time emitter current I_E increases drop. (Refer Fig. 2.6.1) (b)). At the reduces. This causes voltage V_x to number of holes, resistance KBI N-type bar. Because of these large doped emitter are injected in the • When $V_x = \eta V_{BB}$, holes from heavily

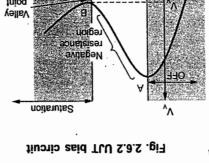


Fig. 2.6.3 UJT characteristics

2. Internal resistance $(R_{B_1}): 4 k\Omega \ to \ 2 \Omega$

3. Valley voltage (V_v) : 2 V

4. Valley current (I_v): 4 mA

Applications

- 1. UJT is used as a trigger device for SCR, GTO and Triac etc.
- 2. It is used as flasher in low power switching circuit.
- 3. Due to negative resistance characteristic it is used as oscillator.

266 Pulse Triggering using UJT

Dec 12-13, 16, May 13-14

The unijunction transistor (UJT) triggering circuit is used in most of the applications. Fig. 2.6.5 shows the circuit diagram of UJT triggering circuit.

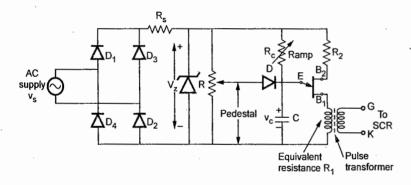


Fig. 2.6.5 UJT triggering circuit

Operation

- The supply voltage is rectified and given to the zener regulator. The voltage of zener diode is V_z. The zener diode clamps the rectified voltage to V_z as shown in the waveforms of Fig. 2.6.6. Hence voltage V_z is applied to the UJT circuit.
- The pedestal control indicates initial voltage level in the capacitor. It can be adjusted through resistance R. The ramp control indicates charging of capacitor from pedestal level. The waveforms of Fig. 2.6.6 shows these levels.
- i) The capacitor charges through resistance R_c . When the capacitor voltage becomes equal to V_p , the peak voltage of the UJT, it turns-on. The capacitor discharges through emitter (E), base (B₁) and primary of pulse transformer. The UJT is turned-on when the capacitor discharges. Since current flows through the primary of pulse transformer, a pulse is generated. This pulse as shown in Fig. 2.6.6 is the gate triggering pulse.

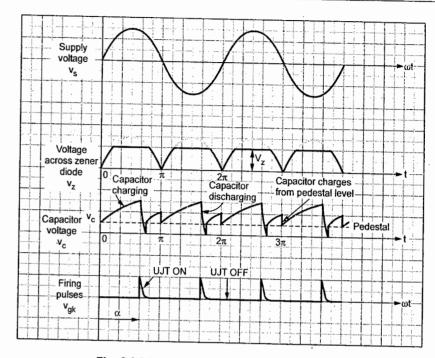


Fig. 2.6.6 Waveforms of UJT triggering circuit

- ii) When the capacitor discharges to a voltage called valley voltage (V_{ν}) , the UJT turns-off and capacitor again starts charging from pedestal level. This mode of working of UJT is called *relaxation oscillator*.
- iii) The delay angle ' α ' is the angle when first triggering pulse is generated in the half cycle. The charging of the capacitor can be varied by resistance R_c . Hence delay angle can also be varied. The UJT trigger circuit has the firing angle range from 0 to 180°.

The zener voltage acts as a supply voltage for UJT relaxation oscillator. This voltage becomes zero at 0, π , 2π , 3π ,etc. The capacitor voltage also becomes zero at these instants. Thus synchronization with zero crossings is achieved. The UJT trigger circuit can be used to trigger SCRs in 1ϕ converters, 1ϕ AC regulators etc.

Mathematical analysis

Power Electronics

The peak voltage at which UJT turns on is given as,

$$V_p = \eta V_{BB} + V_D \qquad \dots (2.6.1)$$

Here V_p is the peak voltage

 V_{BB} is the supply voltage of UJT circuit

(2.6.5) ...

(6.6.5) ...

 $R_2 = \frac{10^4}{10^4}$

Note that, this expression does not require R_{B_1} and R_{B_2} . Normally pulse transformer is connected at the base B_1 of UJT. Pulses are passed through pulse transformer. This provides isolation between SCR circuit and UJT triggering circuit. The resistance of pulse transformer primary can be denoted by R_1 . This resistance controls width of the triggering pulse. From Fig. 2.6.7, this width is given as,

(8.8.5) ...
$$D_I A = {}_{\Delta} r$$
, solug gains gaint definition of the second of the sec

More accurately this pulse width will be,

$$(7.6.2) \dots$$

Here we have considered the interbase resistance R_{B_1} also. It leakage current of UIT is given, then R_1 can be calculated using following equation,

$$(8.8.2) \dots \qquad (_{g_{\overline{B}}} \overline{A} + _{I_{\overline{B}}} \overline{A} + _{I_{\overline{A}}} \overline{A} + _{I_{\overline{A}}} \overline{A} + _{I_{\overline{A}}} \overline{A})_{s_{\overline{B}}} I = _{B_{\overline{B}}} \overline{A}$$

Here I leakage is the leakage current of UJT.

The maximum value of R_c is given as,

$$R_c(\max) = \frac{V_{gg} - V_p}{I_p}$$

and the minimum value of R_{ε} is given as,

$$(01.6.2) \dots \frac{\frac{a^{V} - AgV}{a^{I}}}{a^{I}} = (nim)_{2}A$$

Here V_p is peak voltage

 I_p is peak current

 ${\bf V}_v$ is valley voltage

 \mathbf{I}_v is valley current

Pedestal Circuit with Cosine Modified Ramp

Fig. 2.6.8 shows the pedestal circuit having cosine modified ramp control.

- In the circuit, the zener voltage is given to pedestal control and base of UIT.
- But the charging of capacitor C_1 takes place by rectified voltage.
- ullet The pedestal voltage can be varied by resistance $R_{
 m I}.$
- The charging of capacitor C_1 is cosine modified and its rate can be varied by resistance R_2 .

T[U lo qorb brawrol si $_{\rm G}$ V

n is intrinsic stand-off ratio.

The intrinsic stand-off ratio (n) depends upon the UIT. The period of oscillation of the

UT relaxation oscillator is given as

(2.6.2) ...

SCR Control Circuits

$$T = R_c \subset \ln\left(\frac{1}{1-\eta}\right)$$

Fig. 2.6.7 shows the waveforms of free running UIT relaxation oscillator.

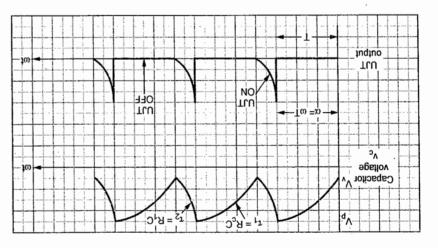


Fig. 2.6.7 Waveforms of free running UJT relaxation oscillator

The capacitor voltage waveform and UIT output are shown in the above figure. From Fig. 2.6.6, it is clear that triggering angle will be,

$$L\omega = 2$$

Hence from equation (2.6.2) we can write,

(E.3.2) ...
$$\left(\frac{1}{n-1}\right)nI\supset_{\mathfrak{I}}\mathcal{H}\ \omega=\omega$$

This equation gives fixing angle of UIT triggering circuit. Here $\omega = 2 \pi J$ and J is the frequency of UIT oscillator. The resistance R_2 should be selected as follows:

$$(4.6.5) \dots \qquad \qquad \boxed{\frac{\left(r_B \lambda + \zeta_B \lambda \right) \nabla O}{r_B V_{BB}} = \varsigma \lambda}$$

Here R_{B_2} and R_{B_1} are interbase resistance of the UIT. R_2 can also be calculated approximately as,

• The firing angle can be controlled by controlling the pedestal voltage.

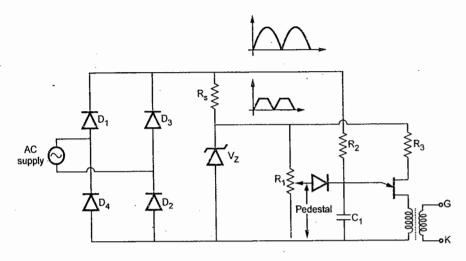


Fig. 2.6.8 Pedestal circuit with cosine modified ramp

Advantages of cosine modified ramp control

- i) The control characteristics is linear.
- ii) Control gain is high.

is 6.2 V. The UIT ratings are:

$$\eta = 0.66$$
, $I_n = 0.5 \ mA$, $I_v = 3 \ mA$,

$$R_{B1} + R_{B2} = 5 k\Omega$$
, leakage current = 3.2 mA

$$V_n = 14 V \text{ and } V_n = 1 V.$$

paramitation

Oscillator frequency is 2 kHz and capacitor C = 0.04 µF. Design the complete circuit.

Solution: From equation (2.6.2),

$$T = R_c C \ln \left(\frac{1}{1-\eta}\right)$$

Here $T = \frac{1}{f} = \frac{1}{2 \times 10^3}$, since f = 2 kHz and putting other values,

$$\frac{1}{2 \times 10^3} = R_c \times 0.04 \times 10^{-6} \ln \left(\frac{1}{1 - 0.66} \right)$$

$$R_c = 11.6 k\Omega$$

The peak voltage is given as,

Power Electronics

$$V_p = \eta V_{BB} + V_D$$

Let $V_D = 0.8$, then putting other values,

$$14 = 0.66 V_{RR} + 0.8$$

$$V_{RR} = 20 \text{ V}$$

The value of R_2 is given by equation (2.6.4) as,

$$R_2 = \frac{0.7 \left(R_{B2} + R_{B1} \right)}{\eta V_{BB}}$$
$$= \frac{0.7 \left(5 \times 10^3 \right)}{0.66 \times 20}$$

$$R_2 = 265 \Omega$$

Value of R_1 can be calculated by equation (2.6.8) as,

$$V_{BB} = I_{leakage} \left(R_1 + R_2 + R_{B1} + R_{B2} \right)$$

$$20 = 3.2 \times 10^{-3} \left(R_1 + 265 + 5000 \right)$$

$$R_1 = 985 \Omega$$

The value of $R_{c \text{ (max)}}$ is given by equation (2.6.9),

$$R_{c \text{ (max)}} = \frac{V_{BB} - V_p}{I_p} = \frac{20 - 14}{0.5 \times 10^{-3}}$$

$$R_{c \text{ (max)}} = 12 \text{ } k\Omega$$

Similarly the value of $R_{c \text{ (min)}}$ is given by equation (2.6.10),

$$R_{c \text{ (min)}} = \frac{V_{BB} - V_{v}}{I_{v}}$$
$$= \frac{20 - 1}{3 \times 10^{-3}}$$

$$R_{c \text{ (min)}} = 6.33 \text{ k}\Omega$$

Fig. 2.6.9 shows the completely designed circuit.

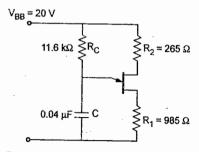


Fig. 2.6.9 UJT triggering circuit of example 2.6.1

Here the pulse width is given, i.e. 50 µs.

Hence, value of R₁ will be,

$$\tau_2 = R_1 C$$
 from equation (2.6.6)

11-2

The width τ_2 = 50 μ sec and C = 1 μ F, hence above equation becomes,

$$20 \times 10^{-6} = R_1 \times 1 \times 10^{-6}$$

$$\Omega_{I} = 50 \Omega$$

Thus we obtained the values of components in UJT triggering circuit as,

$$R_1 = 50 \Omega$$
, $R_2 = 833.33 \Omega$

$$R_c = 10.91 \text{ kg}$$
 C = 1 μ E.

Sounds vest A UJT is connected across a 20 V volts DC supply. The valley and peak point voltages are I V and IS V. The period of UJT relaxation oscillator is 20 ms. Find the value of charging capacitor, if a charging resistor of 100 to is used.

value of charging capacitor, if a charging resistor of 100 kQ is used.

Solution: The given data is,

$$\Lambda \text{ SI} = {}^d \Lambda \qquad \text{ 'I} = {}^a \Lambda$$

$$T = 20 \times 10^{-3}$$

$$\ddot{\mathbf{g}}^{C} = 100 \,\mathrm{K}^{\mathrm{T}}$$

 $V_{BB} = 220 V$

The peak voltage of the UTI is given as,

$$^{Q}\Lambda + ^{gg}\Lambda \mathfrak{u} = {}^{d}\Lambda$$

Let $V_D = 0.8$ and putting values in above equation,

$$12.0 = \eta \approx 8.0 + 0.2 \times \eta = 0.71$$

From equation (2.6.2),
$$T = R_0 \int_0^1 dt dt$$

Putting values in above equation,

$$20 \times 10^{-3} = 10 \times 10^{3} \times C \ln \left(\frac{1}{1 - 0.71}\right)$$

$$C = 0.162 \, \mu F$$

Is suitable that, $V_p = 2V$, $I_p = 10$ mA. The frequency of oscillation is 100 Hz. The triggering $I_p = 10 \text{ µA}$, $V_p = 2V$, $I_p = 10 \text{ mA}$.

pulse width should be 50 µs.

zH 001 = l value frequency = 100 Hz

$$\frac{1}{00I} = \frac{1}{\lambda} = T$$

From equation (2.6.2),

$$\left(\frac{1}{n-1}\right)nI O_3 A = T$$

Putting values in above equation,

$$\left(\frac{1}{6.0 - I}\right) n I O_3 R = \frac{I}{00I}$$

$$R_c C = 0.0109135$$

Let us select C = 1 \mathbf{L}. Then R_c will be,

$$R_c = \frac{0.0109135}{1 \times 10^{-6}}$$

The peak voltage is given as,

$$\Lambda^b = \mu_{\Lambda}^{BB} + \Lambda^D$$

Let $V_D = 0.8$ and putting other values,

$$V 8.2I = 8.0 + 0.0 \times 3.0 = {}_{q}V$$

The minimum value of $R_{\rm c}$ can be calculated from equation (2.6.10) as,

$$R_{c \text{ (min)}} = \frac{V_{BB} - V_p}{I_p} = 1.8 \text{ kg}$$

$$R = \frac{20 - 2}{10 \times 10^{-3}} = 1.8 \text{ kg}$$

Value of R_2 can be calculated from equation (2.6.5) as,

$$\frac{10^4}{88 \text{ Mp}} = \frac{10^4}{833.33}$$

$$\Omega = \frac{10^4}{0.6 \times 20} = \frac{10^4}{0.6 \times 20}$$

Review Questions

1. Explain the UJT pulse triggering circuit with waveforms.

2-18

Dec. 12, 13, May-14, Marks 7, May-13, Marks 3, Dec.-16, Marks 5, Question Bank

2. Explain the construction and operation of UJT.

Question Bank

3. Draw and explain the VI characteristics of UJT.

Question Bank

4. List the applications of UIT.

Question Bank

5. Draw the layer diagram of UIT and explain its operation.

Question Bank

Digital Firing Scheme

May-11, 13, Dec.-12

Fig. 2.7.1 shows the firing scheme that uses digital circuit. Here the AC input supply is given to zero crossing detector (ZCD). At every zero crossing of AC supply voltage, the ZCD circuit produces a pulse. This pulse resets the counter and oscillator. The presettable counter is loaded with a count set by preset input. Then the counter is decremented at every clock input. When the counter is exhausted, it triggers a flip-flop. The flip-flop drives the driver stage. The driver stage amplifies the flip-flop signal and gives it to gate-cathode of SCR.

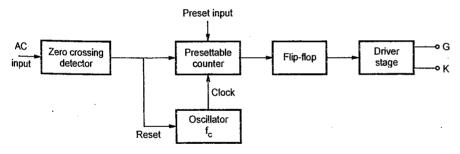


Fig. 2.7.1

The firing delay is set by the preset input. Thus the SCR can be triggered at any delay angle.

Advantages

- 1. The circuit is digital hence no component delays and variations in firing angle.
- 2. Firing angle can be set accurately.

Applications

- 1. Triggering of SCRs in controlled rectifiers.
- 2. Control circuits for AC voltage controllers.

Review Question

1. Explain briefly the block diagram of digital firing circuit used in SCR circuits.

May-11, Dec.-12, Marks 5, May-13; Marks 4, Question Bank, Model Q. P.

28 Commutation of SCRs and its Types

Nov.-11, May-11, 12, 13, 14, 15, 16, Dec.-12, 13, 14, 15, 16

Definition of Commutation

The SCR is used as a switch in many power electronic converters. It is turned on by applying a gate pulse. Once the SCR is latched, the gate has no control over the conduction of the SCR. By removing the gate pulse, SCR cannot be turned-off. An external circuitry is required to turn-off the SCR. Such process of turning-off the SCR is called commutation.

The commutation circuits use LC components. They store energy and it is then used to turn-off the SCR. The commutation can be of two types :

i) Natural commutation and ii) Forced commutation.

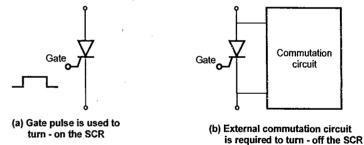


Fig. 2.8.1 Commutation

Conditions for Successful Commutation

Following conditions must be satisfied for successful commutation of SCR.

- i) The anode to cathode current of the SCR must be reduced below holding current value.
- ii) As long as the SCR turns-off, the anode-cathode voltage must be reversed.
- iii) The rate of change of anode-cathode voltage must be less than $\frac{dv}{dt}$ rating of SCR to avoid retriggering.
- iv) Above conditions must be imposed till the SCR regains its forward blocking voltage capability.

Cost of the commutation circuit is significant. Cost of the commutation circuit is nil. ..6 current both. SCR can be turned-off due to voltage and SCR turns-off due to negative supply voltage. .6 _eynenoqmoo commutation. Power loss takes place in commutating No power loss takes place duning 7 controllers etc. Used in choppers, inverters etc. Used in controlled rectifiers, AC voltage 3. Works on DC voltages at the input. Requires AC voltage at the input. .beniupen External commutation components are No external commutation components are ON. Forced commutation Matural commutation .18

12-21

Table 2.8.1 Natural and forced commutation

Self Commutation by Resonating Load (Class A)

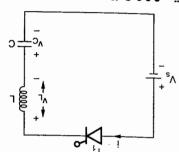


Fig. 2.8.3 Self commutation circuit

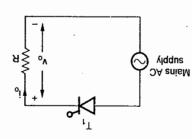
Fig. 2.8.3, the current i(t) is maximum and equal to supply voltage Vs. As shown in charging. At $t = t_1$, the capacitor voltage becomes of the above circuit. The capacitor then starts increases slowly. Fig. 2.8.4 shows the waveforms Because of inductance, the current through T_I The current starts flowing through T₁, L and C. consider that the SCR T_I is triggered at instant t₀. natural characteristics of LC circuit. Let us tor commutation. The SCR is turned-off due to commutation. It uses inductance and capacitance Fig. 2.8.3 shows the circuit diagram of self

conduct. The voltage across the SCR is shown in Fig. 2.8.4. capacitor voltage is greater than V_s . It acts as reverse bias on SCR_1 . Hence it does not becomes zero. Since the current through SCR goes to zero, it turns-off at $t=t_2$. The Since i(t) flows through capacitor, it charges above V_s after t_1 . At $t=t_2$, the current i(t)inductance voltage acts as forward bias for T₁. The current i(t) keeps on decreasing after t₁. $v_{\rm C}(t)=V_{\rm s}.$ But the current i(t) is maintained in the same direction by inductance. The

Impulse Commutation (Class D : Auxiliary Voltage Commutation)

Let the capacitor voltage be $v_{\rm c}\left(t\right)=-V_{\rm s}.$ The SCRs $T_{\rm 2}$ and $T_{\rm 3}$ are off. To initiate turn-off called as auxiliary SCR. Let us assume that SCR T_1 is 'on' and carrying the load current I_0 . current carrying SCR. And T2, T3, C and L are the commutation components. T2 is also Fig. 2.8.5 shows the circuit diagram of impulse commutation. T₁ is the main or load

Matural Commutation (Class F : Line Commutation)



natural commutation to turn-off SCR Fig. 2.8.2 (a) A half wave rectifier uses

flowing. At 'n' the supply voltage is zero. it starts conducting and load current io starts Fig. 2.8.2 (b) Since the SCR is forward biased, half cycle at a. (Refer waveforms of the input. The SCR is triggered in the positive rectifier. The mains AC supply is applied to commutation. It is basically half wave Fig. 2.8.2 shows the circuit using natural Hence it is also called as line commutation. (mains) voltage for turning-off the SCR. any external components. It uses supply The natural commutation does not need

natural commutation takes place without any external components. is then negative. This voltage appears across the SCRs and it does not conduct. Thus Hence current through SCR becomes zero. Therefore the SCR turns-off. The supply voltage

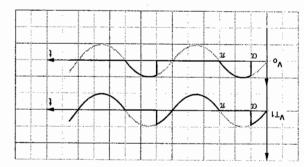


Fig. 2.8.2 (b) Waveforms of natural commutation

Forced Commutation

connected across the SCR. Forced commutation is used when the supply is D.C. A commutation circuit is

holding current and the SCR turns-off. across the SCR due to stored energy. Hence forward current of SCR is dropped below SCR is ON. This energy is used to turn-off the SCR. The LC circuit imposes reverse bias The commutation circuit is normally LC circuit. The LC circuit stores energy when the

Comparison of Natural Commutation and Forced Commutation

Table 2.8.1 shows the comparison between natural and forced commutation techniques.

2 - 23

Power Electronics

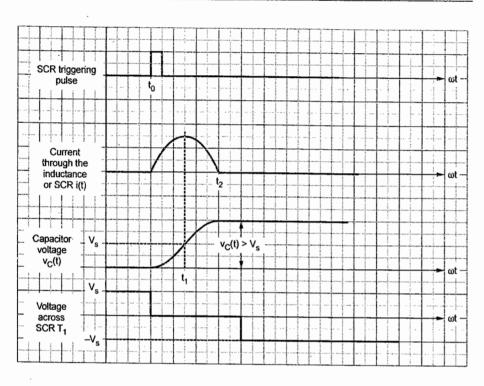


Fig. 2.8.4 Waveforms of self commutation

of T_1 , the auxiliary SCR T_2 is triggered at $t=t_0$ as shown in Fig. 2.8.6. Because of this, the capacitor voltage is imposed as reverse bias on SCR T_1 . Hence T_1 turns-off. The load current I_0 starts flowing through capacitor and SCR T_2 . In Fig. 2.8.6 observe that the capacitor voltage discharges from $-V_s$ towards zero.

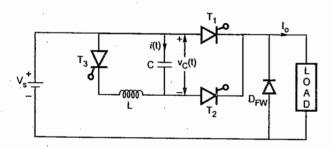


Fig. 2.8.5 Impulse commutation circuit

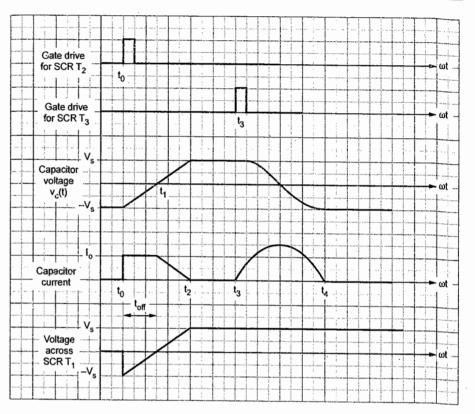


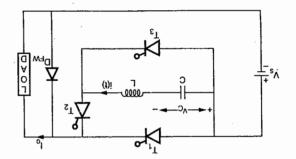
Fig. 2.8.6 Waveforms of impulse commutation circuit

At $t=t_1$ capacitor discharges fully. Thus the reverse bias is maintained across SCR T_1 from t_0 to t_1 . The capacitor then starts charging in positive direction. At $t=t_2$, the capacitor voltage becomes $+V_s$ and its current becomes zero. Hence T_2 also turns-off due to self commutation. The polarity of the capacitor voltage is reversed by triggering T_3 at $t=t_3$. The capacitor discharges through inductance and T_3 . This discharge current (capacitor current) is shown in Fig. 2.8.6. It becomes LC circuit. At $t=t_4$ capacitor voltage becomes $-V_s$ and its current is zero. Hence T_3 turns-off by self-commutation. In this commutation, the SCR T_1 turns off due to negative capacitor voltage. Hence it is also known as voltage commutation. Since auxiliary SCR T_2 and T_3 is used to turn-off main SCR, it is also known as auxiliary voltage commutation. The negative capacitor voltage remains across T_1 from t_0 to t_1 . This period is called circuit turn-off time T_3 . This time must be greater than turn-off time T_3 of the SCR T_1 .

SCR Control Circuits

Commutation) Resonant Pulse Commutation (Class D : Auxiliary Current Table 2.8.2 Self and impulse commutation are required. are required. More number of commutation components Less number of commutation components G Commutation fime depends on load. 7 Commutation time is independent of load. components. components at the time of commutation. Load current flows through commutating Load current flows through commutating 3. main SCR. Additional auxiliary SCR is used to turn-off Only one SCR is used. 7 Commutation takes place due to auxiliary Commutation takes place due to resonating 1 Sr. No. impulse commutation Self commutation Comparison between Self Commutation and Impulse Commutation

the inductance is transferred to capacitor. Hence it overcharges. flow of current, capacitor overcharges to V_C. From t₃ to t₄, the energy (charge) stored in At t_4 , the capacitor current becomes zero and T_2 turns off by self commutation. Because of The available turn-off time is from t_1 to t_2 . In this period the capacitor voltage is negative. current is completely carried by SCR T2 and T1 carries no current. Hence T1 is turned-off. current. This is shown in second equivalent circuit in Fig. 2.8.8. From t₁ to t₃, the load current reaches to I_0 . During period $t_0 - t_1$, the SCRs T_1 and T_2 both carry the load increases from zero as shown in waveforms of Fig. 2.8.8. At $t=t_1$ the capacitor discharge T_1 . The capacitor discharges from – V_C to – V_1 . The capacitor discharge current i(t)SCR T_1 is carrying the load current. At $t = t_0$, SCR T_2 is triggered to initiate the turn-off of to $v_C(t) = -V_C$. This is shown in first (extreme left) equivalent circuit of Fig. 2.8.8. And the auxiliary SCR. It is used to furn-off T_1 . Let us assume that capacitor is charged mutally main SCR carrying load current. T_2 , T_3 , L and C are the commutating components. T_2 is Fig. 2.8.7 shows the circuit diagram of resonant pulse commutation. Here T₁ is the



TECHNICAL PUBLICATIONS - An up thrust for knowledge Fig. 2.8.7 Circuit diagram of resonant pulse commutation

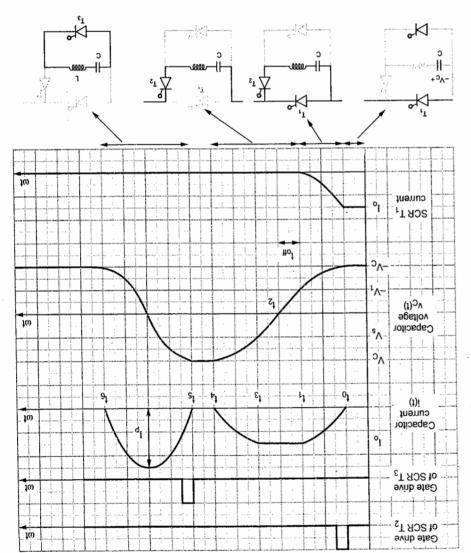


Fig. 2.8.8 Waveforms of resonant pulse commutation

commutation. The circuit turn-off is $t_{\text{off}} = t_1$ to t_2 . Since auxiliary SCR T2 is used to carry the current of T1, it is called as auxiliary current to bypass forward current of T₁. Hence this commutation is called as current commutation. commutation. In this circuit note that the resonant pulse of current (in LC circuit) is used voltage becomes $v_C(t) = -V_C$ and its current falls to zero. T₃ turns-off by self At t₅, SCR T₃ is triggered to reverse the capacitor voltage polarity. The capacitor

2 - 27

Power Electronics

Complementary Commutation (Class C)

Fig. 2.8.9 shows the circuit diagram of complementary commutation. There are two SCRs T_1 and T_2 . These two SCRs are used to transfer the current between two loads R_1 and R_2 . These SCRs turn-off each other. Hence it is called complementary commutation. Let us assume that the capacitor is charged to the voltage $v_C(t) = -V_s$ and SCR T_2 is conducting. The equivalent circuit for this operation is shown in Fig. 2.8.10 (circuit-I). Note that the current through capacitor is zero. SCR T_1 is triggered at $t = t_0$. Hence a negative voltage $-V_s$ is applied across T_1 . The capacitor then discharges from $-V_s$ to zero. A reverse bias due to capacitor voltage is maintained from t_0 to t_1 . This is the circuit turn-off time t_{off} . t_2 turns-off and capacitor charges to t_3 through SCR t_3 . The SCR t_4 also carries load current of t_4 . This is shown by equivalent circuit-III in Fig. 2.8.10. At t_4 , the capacitor charges to t_4 and its current becomes zero (refer circuit-III in Fig. 2.8.10). (See Fig. 2.8.10 on next page)

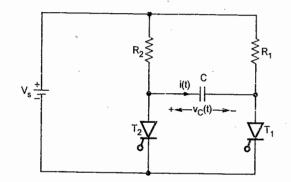


Fig. 2.8.9 Circuit diagram of complementary commutation

SCR T_2 is triggered at t_3 . It applies a reverse voltage of $-V_s$ across SCR T_1 . The capacitor then discharges from V_s to zero and charges towards $-V_s$. Thus the cycle repeats. Here note that the SCRs are switched off due to impulse commutation. Hence this is also called as complementary impulse commutation.

The circuit turn-off time and commutating capacitor are related as follows:

$$t_{off} = 0.693 RC$$
 ... (2.8.1)

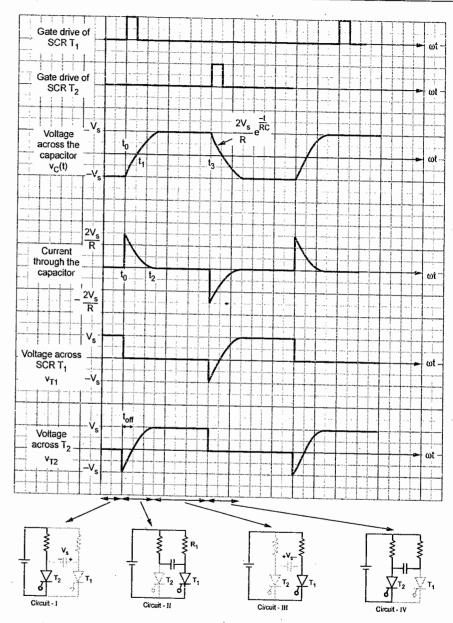


Fig. 2.8.10 Waveforms and operation of complementary commutation

Fig. 2.8.12 shows the circuit diagram of external pulse commutation. Here T_1 is the main SCR carrying load current SCRs T_2 , T_3 and L, C are commutation components. The supply voltage V_3 supplies power to the load. The supply 'V' is the auxiliary supply used to turn-off the SCR. When the SCR T_3 is triggered, the capacitor charges from the auxiliary source. It is LC resonant circuit. A resonant current pulse of peak amplitude $V\sqrt{\frac{C}{L}}$ flows through the LC resonant circuit. A resonant current pulse of peak amplitude $V\sqrt{\frac{C}{L}}$ flows

through the LC circuit. Hence the capacitor charges approximately to voltage 2 V. The SCR T3 turns-off by self commutation. SCR T_2 is turned-on to initiate the commutation of T_1 . The capacitor voltage is v_C (t) = 2 V. This voltage is greater than supply voltage V_s . When T_2 is triggered, a reverse voltage of $(V_s - 2 \text{ V})$ is applied across the SCR T_1 . Hence T_1 turns-off. Here the pulse of current from capacitor is used to bypass the current of T_1 . Hence this is called external pulse commutation.

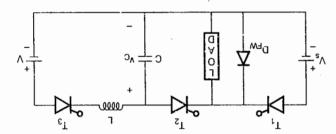
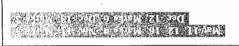


Fig. 2.8.12 External pulse commutation

anoliseuD weiveR



1. List different types of commutation.

2. Define commutation.

Special consoling to the property of the prope

3. Explain natural commutation with neat sketch and waveforms.

TE SHEW TO SEE BY AND A SEE ALL SEE SEE TO BE SEEN SEE AND A SEE AND TO THE TOWN IT SOME

4. Identify the types of commutation.

5. Explain line commutation and forced commutation.

6. Explain load commutation and complementary commutation.

000

Simple 8.3. In Fig. 2.8.11, the source voltage $V_s = 100 \text{ V}$ and the value of capacitor for successful commutation.

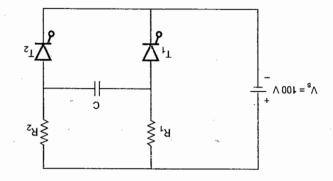


Fig. 2.8.11 Circuit diagram of example 2.8.1

Solution: This is complementary commutation. When T_1 is ON T_2 is OFF and vice versa. The values of R_1 and R_2 will be,

$$K_1 = K_2 = \frac{I_0}{V_S} = \frac{25 \text{ Å}}{100 \text{ V}}$$

$$\Omega = R_1 = R_2 = A$$

For complementary commutation, the available turn-off time is given by equation (2.8.1) as,

If t_q is the turn-off time of the SCRs, then $t_q \le t_{off}$ for successful commutation. Hence above equation can be written as,

$$t_q \le 0.693 \text{ RC}$$
 $t_q \le 0.693 \text{ RC}$

The given data is $t_q=40$ usec and R=4 Ω . Hence above equation becomes,

$$C \ge \frac{40 \times 10^{-6}}{40 \times 10^{-6}}$$

Thus the capacitor must be more than 14.43 µF for successful commutation.

Joseph FEET Sum PENOJES

JOSEPH Zeroze NAME

SUB TOTAL MARKS **CEMIATEO** Explain the types of power / converters sectifies its input 2- DC to AC convertex (Invertex)

Teachar's Elementura

—Sona R**oopa**

STUDENT'S NAME				TOTAL MARKS OBTAINED
CLASS	:	1	RUECT	
ROLL NO.		ī	/ TE	

	Enplain Single quadeant semi converter, tupo quadrant full converter & dual converter.
	typo quadrant full comenter & dual
	converter.
	Single quadrant half wave converter VS 3 & Vo & R
	T, + 10
	VS 3 & V. {R
	_
	to suggest the fee the
	the secondary of the transformer is connected to kesistine load through thyristor or SCR T.
	townells to sensual load studies
	The primary of the transformer is connected to the mains supply. In positive cycle of the Supply, Ti's
	to the mains supply.
-	In positive cycle of the Supply, Ties
	forward biased. This triggered at an
	angle & now Ti conducte & Secondary
!!	
	current & Treattage waveforms are shown in fig.
1:	
	ullent 10 Flouring through 1, becomes
i.	
<u>م</u> - ٠	In negative half cycle of the supply
	Ti is reversed biased & it does not
	conduct-
	Same France
→ · · · · · · · · · · · · · · · · · · ·	reditage is applied to the load, current io starts flowing through the load- current & reditage waveforms are shown in fig. The shape of output current waveform is salue as output reditage waveform. It to supply voltage deops to Zero, hence when io flowing through To becomes zero & it turns of. In negative half cycle of the engply To is seversed biased & it does not

			C.C.	SUBJECT	į	
		, ···	BC.	DATE		
ļ L	the	overage	output 1	eoltage -	3	
!						
		-		A DE LE MANUELLE ALL LE MANUELLE		
		(av) =	Vm (1+ 4	95 X)		j
			2X			
		Tvs.				-
	inpply tage 0 VS					
	mpy.					
real	tage		.:			
	0 73	-K				
	•	L'et,				wt
		1 0 01.7.				
	1-1					
SCR	triggeri nat leg TI	ng				
Sig	nat _				1	
• 0	1411	<		←-T2	ح	wt
		100				
	tout					
7 d	trafe			/		
	tout stage Vo	/				42wt
		~	大	25+2	3 ~	
	; . <u></u>		*			:
	tput.	1				
o ei	Usent		1			<u></u>
	l .		•		Tw.	/ W -
	··· · · · · · · · · · · · · · · · ·	.				
				• •		
	! ~					

		·				:
	•					
				and at		
			No. of 1992 A 1992 A		1 11 11 1 11 11 11 11 11 11 11 11 11 11	
· · · · · · · · · · · · · · · · · · ·			name - Same -			
				[non	Roopa -	
	Teacher's	Carrier Carre		10.10	Nooha	

HARTS NAME

TOTAL MARKS CETAINED

STUDENT'S NAME		TOTAL MARKS DETAINED
CLASS) :3TECJ.	
ROLL NO.	o vra	

	Two quadrant full conve	ter (Lull bridge
		Converter
· ·		
2300, Ac Supplu	T_1 T_3 T_3 T_5 T_6 T_7 T_8	tuo quadroni foreration
//_J	Ty T2 - V	
	It contains four SCR's Ti, I	T2, T3; T4. the
	conduction of all these so	!
	hence this is called ful	Converter.
	du the positive half cy SCRS To Ex T2 are triggered a hence current starts flow load.	de of the supply,
:	SCRS TI E T2 are treggered a	t firing angle &
	here curent starts flow	ing though the
	parafornes are shown in	Legue.
	Londuits.	u, when 11 Ef 12
	Vo = Vs	
	to = vo = vs	
	RR	
:		
		Jane Dagge
	Teacher's Signatura	Sona Roopa

	STUDENT'S NAME			TOTAL MARKS OUTAINED
-	CLASS		SUBJECT	
	ROLL NO.	:	S. TE	

	iagia	<u></u>				üewit	
	is	~~~~	A iT,		+	10	
Vs	+		T_{i}	Di C T	- Vo	L A P	
			B				
A	swit	th 2	(em ne	ted ac	soss E	ductar	re Ej
su	pply	· A fo	etter c	aparito	sis m	sed acros	8 0
ble	reks t Leu ×	te seve suitch	rse fl	ow of	outpu	sed acros e diode t curse	t
and the contract of the contra							
	ouses.	wi is	sune	c on y	0 محمد	(D_0/	tane
he	ne	cuser	t Llou	is the	ough to	te Endu	3019
fu fu	me m tt ses sy	te Supp endi	t flou ely. the chance	is the ende . Stores	referre	e the to ST. te Endue cussent vergy f	com
fr fr sey	me m te ses sy oply.	cunente Supp endir	t flou ely to ctance	es the	ough the starte the e	cussent rergy f	com
fis fis sey	me m to ses sy oply.	cunente Supp endu	t flou	is the	ough the	eussent regy f	com
fis fis sey	me m to ses sy pply.	cunente Supp endu	t flou	is the	ough the	eussent rergy f	com
fis fis sey	me m the ses & pply.	cunente Supp endu	t flou	is the	ough the	eussent vergy f	com
fis fis sey	me m the ses sy pply.	cunente Supp endu	t flou	is the	ough the	eussent vergy f	com
fis fis sey	me m the ses & pply.	cunent ender	t flou	is the	ough the	eussent vergy f	com

: HUDENT'S NAME		OGTA	
1.17. S \$	SUBUECT		
STILL NO.	DATE		
		i	

1,20																		
 wa	7																	
 : :-		ve of th		<u> </u>	1	1	j				T	r			7-1	1-1		
 -		witch i _B			0	δΤ				Τ+δΤ		2	r			ωt .		
 				V _{o(a}											\perp			
 . :					-										4	+		
-		e acros ansistor		e	0 -	δΤ		+-								ωt.		
		VAB	11		1								+			.#		
 I			1	ım	ıx I		1				1				1			
 · i · · ·		ent thro			イン			*									;···	
 -		nductor				δТ									1	ωt		
 · · · · · · · · · · · · · · · · · · ·				V _{o(a}	╮┞╌┞			4			-			+	\dashv	-		
ļ.			1		11													
 	Out	out volta	age .											\dashv		ωt		
 			\pm		1	++											<i>:</i> *	
 j	Out	out curr	rent	I _{o(a}	<u>"</u>							H						
		io	-	-	+	111												
islave	Josus	<u>ک</u>	01		ter)- u	P	d.	رام	bes	 			··		ωt -		
hlave,	Josu	<u> </u>	of	. 0	tep	?-u	P.	d.	of	pes		Touch .			-	- OIL-]		
hlave,	Josus	<u> </u>	of	-	Step	? - u	P	ch	oþ	pes	 	Total Control			-			
Mare	Josus	<u></u>	of		step	? - u	P		oj	pes	2.·.	Total Control of the			-	- OI -]		
Mare	Josu	<u></u>	of	-	Step	? - u	P	ch	oþ	pe	3·.					01		
Mave	Josu	<u></u>	of	. 0	Blep	2 - 11	P	do	oþ	pes	3—.*.				and the state of t			
			-					···										
Mare											-							
			**							· · · · · ·								
			***										-					
					-													
					-					· · · · · · · · · · · · · · · · · · ·			-					
					-					· · · · · · · · · · · · · · · · · · ·			-					

Sona **Roopa**

	STUDENT'S NAME		NARM JATOT OBNIATEC
	CLASS	3 30407	
	ROLL NO.		
Englain V	ST & CST.		
	SI & CSI		
Voltage S	ouce Inverter	<u> </u>	*****
The exput t	the realtage	+ 7.10	eta V
source env	the realtage	Vs T-	eter [][
Dc Voltage	Supply or		
battery, for	or such eur	rentes	
the ampl	itude of loa	d voltage, is	egual
to DC engr	ut realtage.		<i>ν</i>
The curier	itude of loa ut veeltage. t waveform	depends u	pon load
	V		
Cussent S	ourse Inverte	<u>e</u>	
The enput t	the current		
sourie is c	onstant une.	DC	
lurent so	ure.	Ocured Inver	ter []
the Constan	t current	some	
	u be obtain	کھ	
by connect	ions large en	identor en	Sevies
with un	controlled o	s controlled	ectiféer.
	curent is	, ,	// .
cussent:		1	
	2010 1 10 10 10 10 10 10 10 10 10 10 10 1		
			erier von der en rechte der er en
Teacher's Signature		- Song Ro	000

TOTAL MARKS DETAINED

		ALEN'US NAME		TOTAL MARKS OBTAINED
			SUBJECT	
			DATE	
·	Fall - C	L L		
**************************************	Explain Sme	art powe	n modules.	· · · · · · · · · · · · · · · · · · ·
~				
	The power a	eccionic "	convener ma	ry require
	tues, four			
	additional			
	are also regi	wea. za	Color shaw is	seng
	module que	noneus	y denices, o	combined
	module 4	mal 1	devices is in	sed. It is
	called power	maule.	+ · · · + · · · · · · · · · · · · · · ·	°1 11 °
	complete p	rower Co	nverlee is av	aclable en
	single porbe			es the
	fower convert	e very	compact.	
	smart power			
	denices as a			
\rightarrow	Smart powe	n modi	ile Consists	97 D + 1 2
	enterfacing of	poule	dennes unt	h biggering
manager of the state of the sta	& control ci			
- make the	isolation, de	rue cuci	ut, protection) 21
	diagnostic ci			
et to any the effective a source or well to assume a such	Ej pour Su	pply ell	are inclu	ded en
	Smart pour	model	e	
	It also ence	ude EM	c unu co	Moia
	electromagnes	lic Leidi	alion.	
		<u> </u>		
·		. * . <u></u>		
	<u> </u>	Construction and the Construction of the Const		
		and the second s		
	<u> </u>			
			en e	
	;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;			
	Teacher's temphres		Sona	Roopa —

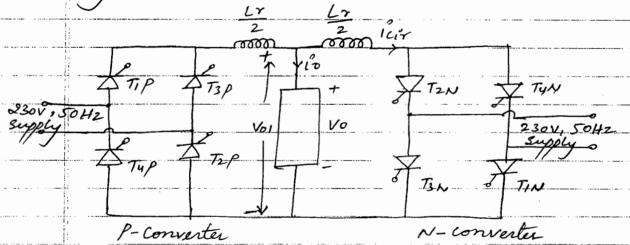
	STUDEN T'S NAME		TOTAL MARKS OBTAINED
	CLASS	SUBJECT	
ľ	ROLL NO.	gara.	

Lich alu tara si dina	dvantages of Gorner
List advantages Es disa electronic converters.	7 7 1
ADVANTAGES	F 0 0L
ij Entremely, compact iii Common heat sink	culut
in Common heat such	& foures dissipation
ing Reduced Cost	
iv) Lasy fault Lindi	ng
iv) Easy fault Lendi	
DISADVANTAGES	
1) Nat repairable	21 - 20/5 + "
ii) Not much suitable pouces applications.	applications.
111) Not much suitable	for very high
pour applications.	
of Dean the circuit of so enplain its operation	top down chopper &
enplain its operation	
is /	نَّ اُنْ
Sw to	1 1+1
SW The	VST BONG diam
	VS Base drive
¥-)	
(a) step down chopper	(b) Step down chopper with transistor as a switch
- The suntch (SW) can	be power transistor
SCR, GTO, DOWN MOSE	ET, IGBT
The Suitch (SW) can SCR, GTO, power MOSF The drop in the Suu & its is neglected.	tch is very small
site is nochested.	
9 22 139	
	- Sonu Roopa
Teacher's Signature	

		DENT'S NAME		TOTAL MARKS DEMIATED
		33	TOSLBUE	
		rica vo.	DATE	
	, , , ,			
	waveforms			
	Base drive of transistor			-(a)-
	1 (on Toff	Γ+δΤ	wt
				(b)
i	Output voltage vo	δΤ		-wt
!	V _S			-(c)
	current			ωt
	Fig. 4.10.2 Wav	eforms of the step-do	own chopper with resistive load	
	Inlaneforms of	Stepdom	n chopper.	
	, · · · · · · · · · · · · · · · · · · ·	J	J J	
		· · · · · · · · · · · · · · · · · · ·		
			,	
1				
				ing to reggy programmed to the contract of the programmer and some states.
<u> </u>		And designation of the second		
	8 4			
	Miles Commission Control of Contr			
				,
	e			
	11.00		Come Da	224
	Teacher's Signatura		Sona R o	UUU

STUDENTS NAME		TOTAL MARKS CETAINED
CLASS	() JECT	
ROLL NO.	1000	

		ROLL.NO.	14.7%	
	Low way	e four the s	load valtage	is Same
		, valtage L		
	the load	is sesentine,	wavefours	of vos
	L'o are Sam	e. The Supp	oly culsent "	is spio
		· Same dire		
->		un off who		
	becomes Z	ero at T. Is	i negative d	half
THE STATE OF THE S	cycle T3	& Ty are to	ggered at T	+x.
	Sual cons	erters		
/	:			· · · · · · · · · · · · · · · · · · ·
	the dual	Converter proo	luces an ou	tput
	vattage the	at combe	positive as	uellas
	negative	Converter product can be		
		1 1		

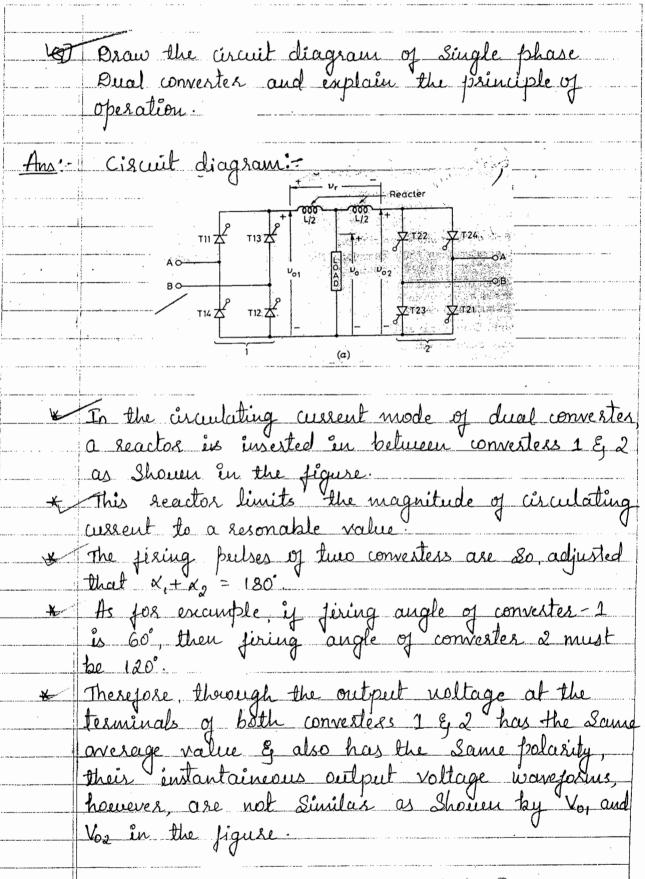


for dual converter the load is normally inductive such as motor the p-converter produces the output recetage which is positive the N-converter produces negative output voltage.

Sana Roopa

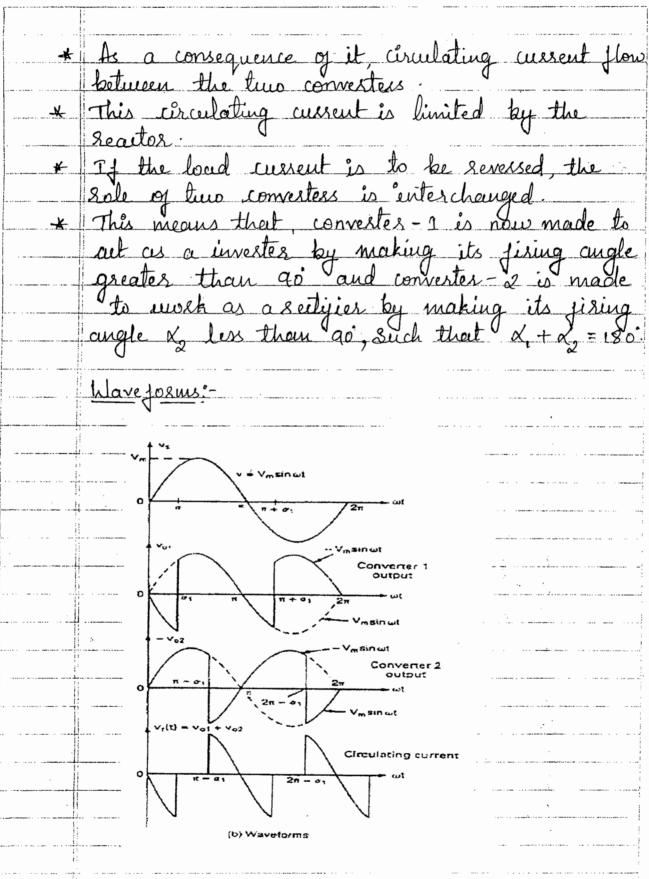
Teacher's Signature

- HOENT'S NAME	TOTAL MARKS OBTAINED	
01. N33	SUBJECT	
	DATE	



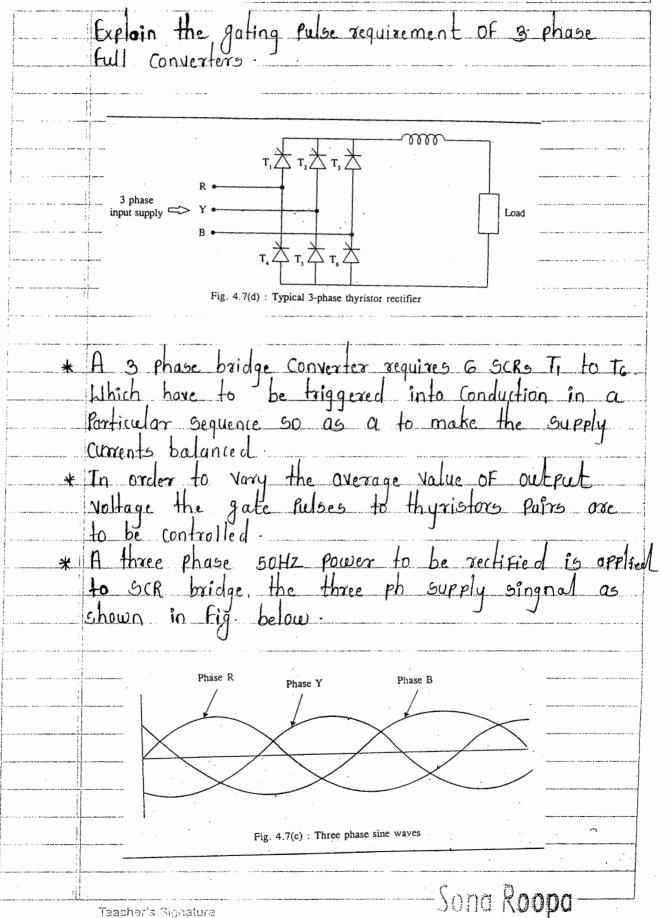
Sona **Roopa**

STUDENT'S NAME		TOTAL MARKS OBTAINED
CLASS	! · · · · · · · · · · · · · · · · · · ·	
ROLL NO.	· · · · · · ·	



Sona Roopa

PIDENT	S NAME			TOTAL MARKS OBTAINED
J 438	Vth sem.	SUBJECT	P. E.	
COLL NO.	-	DATE		



STUDENT'S NAME	·	TOTAL MARKS OBTAINED
CLASS	·EC1	
ROLL NO. LA	E .	

	Waveforms
	Phase R Phase Y Phase B V _{ph} 20 msec T ₁ T ₂ T ₃ T ₄ T ₅ T ₅
.: - '	Fig. 4.7(e): Desired gate pulses
	Teacher's Signature Scient NOODC

FOOSNT'S NAME		TOTAL MARKS OBMIATEO
.: . \33	SUBJECT	
: MO.	DATE	

<u>L</u>	Deau the different chopper configurations
	Deswitte différent chapper configurations (A, B, C, D & E) & enplain them.
	Class A choppes
	T
	The class A chopper operates en the first
	The output ensent sy output
	The output current sy output
	voltage both are positive: vo(ov)
	these realises never go negative
	This type of chapper
	operates as seitiféer Do(av) i
	The energy always flows from source to load. it is also called as
	Louised monitoring motoring.
	forward monitoring motoring.
	Claus a classes.
:	Class B Chopper
	the class of an approximate an
	The class B chopper operates en vo(av) the second quadrant of the Vo-io plane.
i	me secona quadram y me
	Vo-to plane.
	the load voltage is positive & - To (av)
	load current is negative.
	The Load current flows out of the load
	sence the current flows from load to
	the source the energy is transformed
	from load to the source. It is also
	called as serverting operation.
	Y /
i	Song Rappa — M

Taachor's Signature

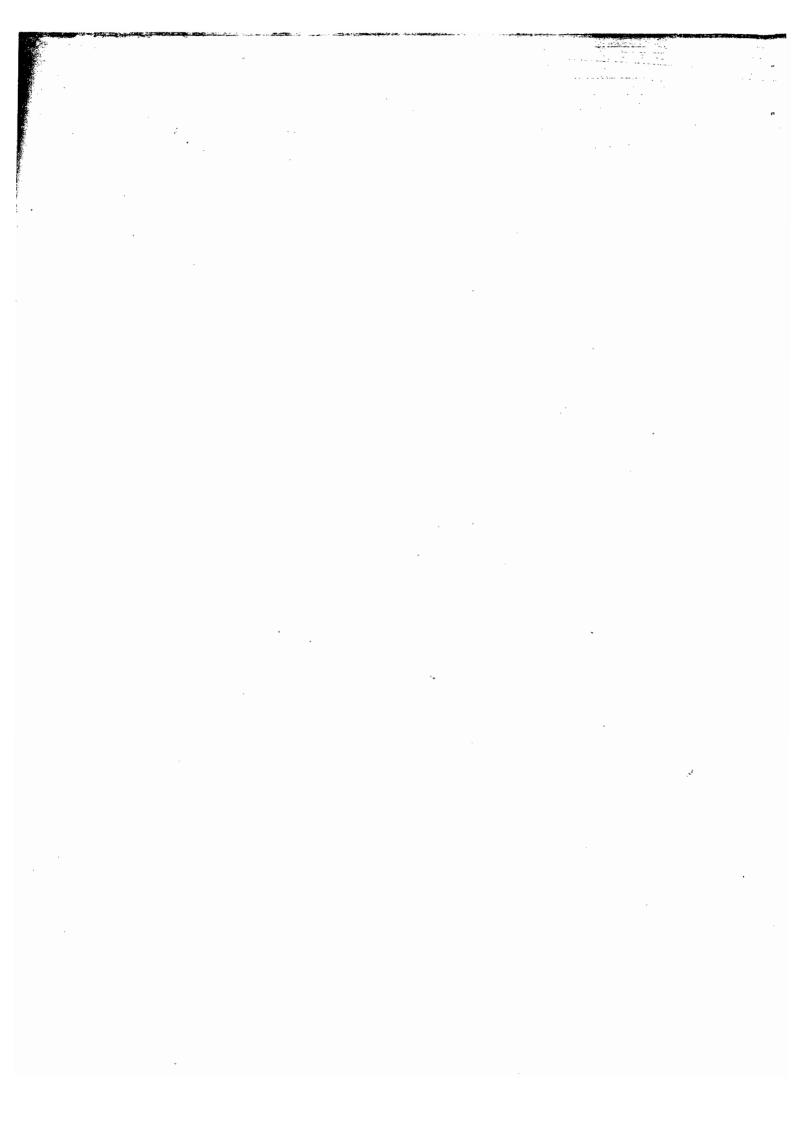
Doug **Koob**a

		CLASS	for JECT	11	
		FOLL NO.	177.76		
	class c ch	opper	A Citata and Allaham Samuel I		9
	The class C	chopper op	erates en	Vo	(av)
	two guad	rants. it.	is		
· ·	Combinato	in of class	9 4 B		
	- Compression			(av)	To lo
	It operate	es as a Lei	tifées as i	uell as	
	éwertes.	in the fir g takes ble forward r	st guadra	ut for	would
	monitorin	g takes ple	nce. Es én	the seco	md
	quadrent	forward 1	egenerative	. breaken	9
	takes place				
				▲ Vo	
	class D chap	oper			Q-I
				Vo (av)	
	cless D Cho	oper also 9	perates en		
	two guad			0	Lo to
	The output			(av)
·-····· · · · · · · · · · · · · · · · ·	positive.	the outpu	t restage	- vo (av)	φ- 1
		ositive or		(-	
	when to	Sy Lo both	are posicio	ue the	
	rectifying) le la l	materia.	re, u	25
	also calle	Notte and	The state of	0	t-3 1
>	when the	toker blace	Hier essel	, 2000ec	Je d
	operation.	ad to Some	2. The 11/4	h and	Cont
	Geom la	is also ca	Hed severs	e leges	Mation
- 175-	1				
				ALL I AMERICAN PROPERTY AND A STATE OF THE S	
	The state of the s				
				n Roopi	4 .
	Teacher's Signature		Mar Maria		_r

STUDENT'S NAME

TOTAL MARKS OBTAINED

	COMPERTS NAME	•	CARAM JATOT
	r - 2.55	SUBJECT	
	in the NC.	DATE .)
·			↑ v₀
class E	chopper-		
<u>i</u>			vo cau)
\rightarrow class E	is a four		
	nt chopper:	-Io(w)	Io (au)
1. /	rates en the		<u> </u>
	uadrants of v	- 20	
	un en fig.		- Volar)
- the o	utput current	Siglottore	¥ V2
bott c	an take posis	time of negat	ine reclina
-> The 1s	+ quadrant	s Jourand n	wiering.
the or	that current	Sy output re	situge
both a	re positive.		
<u>ciscuit</u>	diagrams:		
		A+	
	io	CH1 /	T D2
† L	1 1	V _s	1+ 000 Tio
V _s FD	Vo Load	CH2 / FDZ	T E
0-			
a -st		(a)	
31 Qu	adrant	The Guad	sant
1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -			
Q		+	101
CHI /	2 02	CH1 / 1	DI CHS / J
of the second se	+ LOAD - 5-170	V _s	**************************************
D1, 🛣	, cH2	CH2	02j;¢H4 / _ 本
Sold Bill Bridge	<u> </u>		(a)
	and another control of the control o		and the second s
IInd Quo		IVth Quac	
11- Quo	ioixant ·	IV Quae	saut.
	and a super-		
		— Sona R	ממחמ —
Toacher's Co.	iofore	JUHU N	rooha



UDENT'S NAME	TOTAL MARKS OBTAINED	
DEASS	3UBJECT	
A MALNO.	DATE	

g 里	Ezplain pri	nciple of phase control with waveforms
		load
		· r
		T, 1 +
		io
	Br Blin	V2
	Guphy	1 } k
	.	
	<u> </u>	
Ans-		means to control the postion of the
	Supply vallage	applied across the load
	Explanation	
		mains Ac Supply is applied to the Inpul
	The GCR is to	siggered in the positive half cycle at a.
		is torward biased it starts conducting
	,	ent io Starts flowing. The waveforms of
	LUXXINIS ONO	vallages are shown in fig
	AC Supply	→ WI
	vallag	
	Vs,	
	output	, wi
	vallage	d 7 211-d 316
<u> </u>	10	rollage current
		90es to 2010
	output cussessin.	
		d TI
	cussint	
il		Sona Roopa
	Teacher's Signature	ANIIS WAANA

ETUDENT'S NAME				TOTAL MARKS OBTAINED
CLASS	;	AFCV.		
MOLL NO.	:	75		
·			. !	

Obsesse that the output cussent is basiculty SCR cussent. At 'T' the Supply vallage is zero. Hence cussent through SCR becomes zero. therefore the SCR turns OFF. The Supply vallage is then negative this vallage appears across the SCR and it does not conduct. Hence note that the averge average rms value of output vallage can be controlled by controlling the fraing angle a. It is nothing but controlling the phase of the Supply vallage. Hence it is also called phase control.

Drow the circuit diagram of half bride involves & its operation with wave forms.

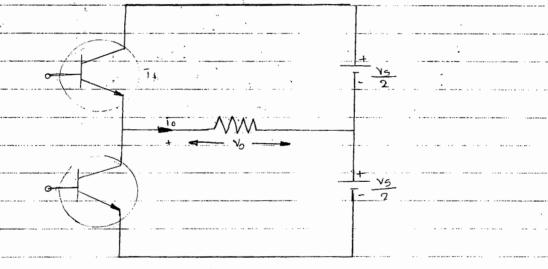


Fig (a)

Ans-> Fig shows the cireuit diagram of Single phase hulf bridge inverter. The two trunsistor T. and T. are used as Switching devices. They can be MOSFET, GTO. SCR IGBT etc., Figoshows & waveforms of the hulf bridge invertex having resistive load Transistor T. conducts from D to T hence the output valtage is positive and it is No In equivalent circuit I in fig observe.

That 2 current flows from paint A to B in the load.

Some Roopa

Teacher's Signature

TOENT'S NAME		SHAAM JATOT OBYRATAO
1 - 1 - 5 C	SUBJECT	
Le la NG.	DATE	

Transistor To worderly from I to I & I; is off.

Equivalent circuit-II in fig (b) Shows the Situation

When To worderly wordent flows from paint B to A in

The load. The output voltage 15 - Vs. this is the negative

half eyele of output. Since the wad is resistive.

output current waveform is same as voltage waveform

also shows the currents through the transistors the output

of this invertex is a square wave since there are two

transistors in the bridge. It is called helf bridge invertex.

Wove towns

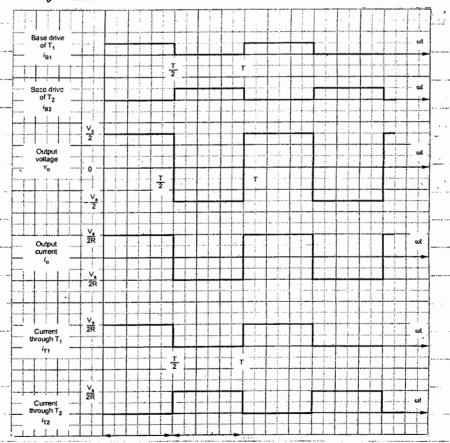


fig (b)

	STUDENT'S NAME TOTAL MARKS DERIGATEC STUDENTS
	CLASS . :JJEG:
	ROLL NO. UTI
(Q)	Draw the circuit diagram of full bride enverter and
3)	its operation with wave forms
	The opening with make forms
	$T_1 \nearrow D_1$ $D_3 \nearrow T_3$
	Vs
	$T_4 abla D_4 \qquad D_2 abla T_2 \qquad D_2 \qquad D_3 \qquad D_4 \qquad D_4 \qquad D_5 \qquad D_6 \qquad D_$
	Fig. 4.19.1 Single phase bridge inverter
	rig. 4.13.1 Single phase bridge inverte:
Ans-	we studied holy bridge inverter earlier, fig shows
	The circuit dragram of full boidge inverter. Observe
	That these are jour transistors and four diades the
	diodes are required for feedback when the load 15
:	inductive.
	When the load is sesistive the diodes does not leasy
:	any current. The transistort, & T, conduct from 0 to I.
	equivalent asseril -I in jig shows the current path when
	T. & T. conduct. the output voltage & cussent are positive.
	Note that the amplitude of wad vallage 15 Vs
	Drive of T ₁ and T ₂
:	i _{B1} , i _{B2} 0 - 1 T T T T T T T T T T T T T T T T T T
	T ₃ and T ₄
	Output
į. į.	Oùtput voltage ————————————————————————————————————
:	
	V _s
	Output R wit
	- R R TT TT TT TT
	T ₁ T ₂ T ₃ T ₄ T ₁ T ₂ T ₃ T ₄ T ₃
	through T ₁ & T ₂ - wt
: 	Current R through T ₃ & T ₄
	173, 174 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

: WENT'S NAME		TOTAL MARKS OBTANED
1. C. 1. S.E.	SUBJECT	
Sydat NO.	DATE	

W-\$5-	Draw the circuit of mid-point of and explain its operation with Circuit diagram	tep-up cyt cycloconverter h Waveforms
	σ τ ₂	
A CONTRACTOR OF THE CONTRACTOR	v _s ≃ V _m sin ωt book Load Load	
	T ₃ p	
	Fig. 4.24.1 Midpoint type cycloconverter	

* klhen the frequency of the output is higher than the frequency of input, then it is called step-up cyclo-converter.

* tig. shows the midpoint type step-up cycloconverter.

* In the positive half cycle, TI conducts From a to tI, hence, output Voltage is positive.

* At tI, TI is forced commutated and TI is triggered. Hence load voltage becames negative as shown in fig.

* Then the at to, TI is forced commutated and TI is turned-on again.

* Therefore output voltage is again positive; At to, TI is turned-on and TI is forced commutated. Hence output vity is negative.

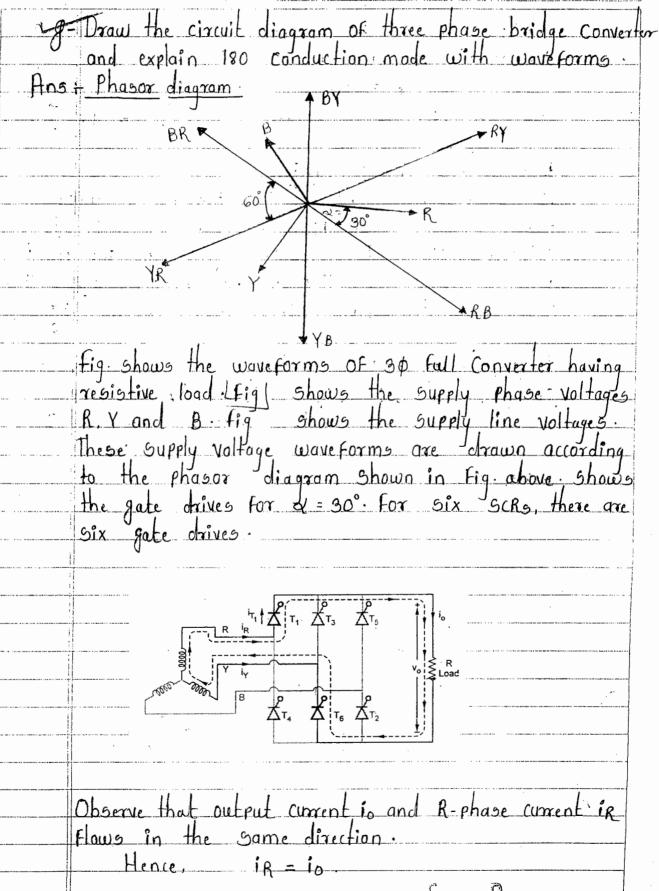
* At IT, To is turned on. Therefore output voltage is positive * At ty, To is forced Commutated and To is triggered. Hence the load voltage is negative.

STUDENT'S NAME		 TOTAL MARKS DEMIATED
CLAS3		
ROLL NO.	1.77	

	PARTIES TO THE PARTIE					
. عاد	This sequence continues. Observe that output voltage blaveform has the Frequency of,					
	in sequence confinues. Observe mai output voituge					
	blaneform has the trequency of,					
	$f_0 = 1$					
	$f_0 = 1$ $t_2 - t_1$					
i						
	This Frequency is higher than supply Frequency.					
· 	Waveforms:					
	Output					
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					
; ;						
	T_1 T_4 T_4 T_4 T_4 T_5 T_2 T_4 T_4 T_4 T_5 T_7 T_8 T_8 T_8 T_8 T_8					
	Fig. 4.24.2 Waveforms of step-up cycloconverter					
	11g. 4.24.2 Waveloinis of Step up dystocentered					
از استنداد است از استنداد است						
	· · · · · · · · · · · · · · · · · · ·					
:						
	The state of the s					
<u> </u>						

-Sun-Roopa-

LINES NAME		EXRAM JATOT OPMATEC
::	SUSUECY	
10.	DATE	



Sona **Roopa**

	STUDERT'S NAME		TOTAL MARKS OBTAINED
-	CLASE	- 514 BCT	
	ROLL NO.	· 1 · 1 E	

Similarly observe that Y-phase current iy and off current is one in opposite directions. Hence,

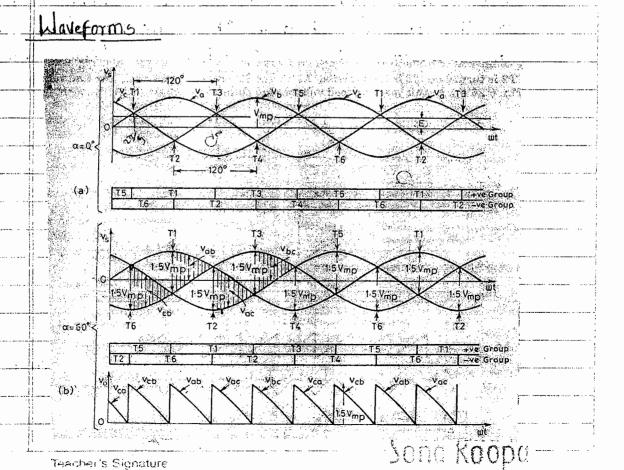
The SCR Pair TG-T1 conduct From [TT + x] to [TT + x]

Line voltage VRY is applied.

During this feriod At [T + x] SCR T2 is triggered.

Here downote that T6 turns-OFF, Since T2 is triggered. Hence Ti-T2 starts Conducting and it is marked as interval-II. In this interval supply line voltage VRB is applied across the load. At [577 + x

To is triggered. Hence II turns-OFF and To-To starts conducting: Therefore line voltage Vyo is applied across the load It is marked as interval-III.



A J	List the differences between VSI and CSI	
Ans:	Voltage Source investers	cussent Sources invester
<u>J</u>	Input is constant voltage Source	J Input is constant cussent Source.
ع	Cussent waveforms depends on load	2) voltage wavejosms depends on load
3)	Free wheeling diodes are required in case of inductive load.	3) Free wheeling diodes are not required.
4]	Large capacitor is connected across DC IIP Side of inverter	4) Large inductor is connected in Series with DC PIP waltage.
5]	Parallel and Series are noltage Source investers	5) Bridge type is current source inverters
6]		6] No sesonent ciscuit is sequired.
QJ	Praw-the circuit diagram of mid-point Step down cycloconverter and explain its operation with waveforms.	
	Teacher : Signatu	Sona Roopa