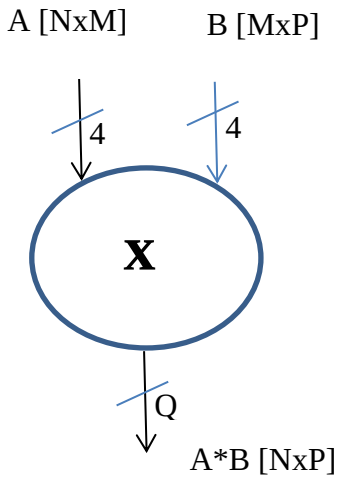
# Matrix Multiplier

Design the VHDL description of a matrix multiplier with the following characteristics:

- input matrices of size (NxM) and (MxP) with elements represented in 2's complement on 4 bits
- Output matrix of size (NxP) with elements represented in 2's complement on Q bits. The value of Q has to be determined in order to avoid any finite arithmetic's error.

For the test-bench simulation, please consider the following values of the parameters: N=2, M=3 and P=4.




**The final report shall include:**

- Brief introduction about state-of-the-art algorithms/architectures to implement matrix multipliers
- Description of the implemented architecture (block diagram, input/outputs, etc.)
- Source VHDL code (with detailed comments)
- Test-plan for matrix multiplier verification
- Testbench implementing all or part of the test-plan
- Synthesis Logic results for the Xilinx FPGA Zync platform: device utilization (slice, LUT, etc.), maximum frequency and relevant critical path. Please justify any synthesis warning messages.
- Conclusion