## Luca Dalmasso

#### COMPUTER ENGINEER · ASIC DESIGN & VERIFICATION

Cork. Ireland

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# **Work Experience**

Apple Munich, Germany

SoC DFT Verification Engineer

August 2024 - Present

- · Verification of the overall SoC DFT infrastructure with focus on controllability and observability of mixed-signal IPs
- Generation of test-patterns for ATE to support silicon bring-up in production phase
- Technical Skills: Design For Testability (DFT), Digital IC Verification, Silicon Bring-up

Qualcomm Cork, Ireland

GPU Design Verification Engineer

February 2023 - June 2024

- Presented verification strategies to validate the latest features in the design
- Collaborated with cross-functional teams located in different geographical locations to get closure of the verification milestones
- · Hands-on experience with verification of complex multi-million gates logic partitioned in multiple power domains
- Technical Skills: SystemVerilog (IEEE 1800), Universal Verification Methodology (UVM), Digital IC Verification, Unified Power Format (UPF)

Sistematica S.p.A Città di Castello (PG), IT

Programmer Analyst April 2020 - July 2020

· Development of Python tool to interface a Raspberry Pi with the ECU of an electric vehicle to monitor and inject traffic in the CAN Network

• Technical Skills: Hardware-in-the-loop (HIL), Testing

I.S.C.S srls Turin. IT

Software Programmer - B.Sc Internship

June 2019 - Sept 2019

• Development of the backend code for an iOS/Android app used for the acquisition and processing of biometric data of medical wearable device

Technical Skills: Software Engineering.

### **Education**

Politecnico di Torino Turin, IT

M.Sc. degree in Computer Engineering

September 2020 - October 2022

- Design of complex digital systems using hardware description languages
- Study of the synthesis and optimisation techniques to improve the product performances
- Analysis of the correctness and reliability of the final product
- Technical Skills: Digital IC Design, Application Specific Integrated Circuits (ASIC), Design For Testability (DFT)

Politecnico di Torino Turin, IT

B.Sc. degree in Computer Engineering

September 2017 - March 2020

- Solid background on maths, physics, computer science & electronics
- In-depth aspects of information processing systems and computer architecture
- Technical Skills: C, Computer Science, Electronics

### **Projects**

#### MC2101: A RISC-V-based Microcontroller for Security Assessment and Training

Politecnico di Torino, IT

M.Sc Thesis - MC2101

2022

- RTL design of the bus infrastructure, memory and peripherals of a RISC-V microcontroller
- Coded the firmware and the test suite to synthesise and validate the design on FPGA

### RTL design & synthesis of a LBIST circuit

Politecnico di Torino, IT

RISC-V Core

RTL design of a LBIST wrapper for testing stuck-at faults of a RISC-V core using Test-per-Scan methodology

#### RTL design & synthesis of a 4-stage pipelined RISC DLX processor

Politecnico di Torino, IT

DLX

2021

• Implemented complex arithmetic blocks from Pentium 4 and UltraSPARC T2 processors, Hazard Detection features and Clock Gating technique

## **Languages**

**English** Professional proficiency **Italian** Native proficiency

AUGUST 30, 2024