# MC2101: A RISC-V-based Microcontroller for Security Assessment and Training

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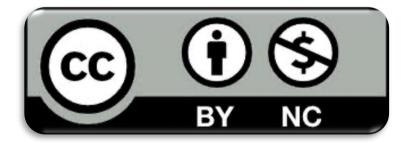
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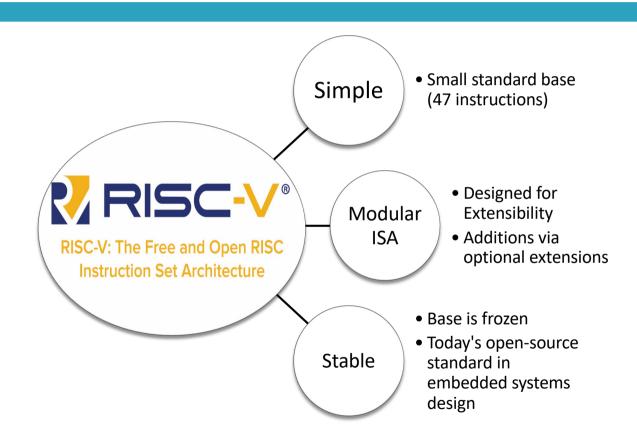
# Outline

- Introduction
- MC2101 Microcontroller
  - Architecture
  - > Peripherals
- Experimental Results
- Conclusions

- Embedded systems are massively used as edge devices in:
  - Safety-critical applications
    - > Cars, Aircrafts, Trains, Medical equipment, ...
  - Business-critical missions
    - Industrial automation, telecommunications, ...
- Key benefits:
  - Real-time reliable
  - Low manufacturing cost
  - Low power consumption
  - Require minimal human intervention on the field

- > Such devices must be secure and reliable
- Problem:
  - Built-in device security is minimal
- Research Solution:
  - Software-based techniques
    - Can be easily tested outside the operating environment with a proper software toolchain
  - Hardware-based solutions
    - Require a CPU architecture description to be physically tested
      - > Most famous architectures are licensed (Intel, ARM) and not accessible to research
      - Production of new silicon (e.g., ASIC) is unaffordable

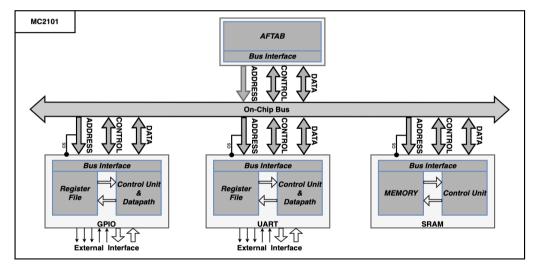
Open-source Open-source design ISA To evaluate • customizable • Simple both HW/SW starting from the **RISC-V ISA** Supported by security core itself popular solutions • Synthesizable on software toolchain, e.g., **FPGA GNU GCC** 



- Purpose of the thesis work: design MC2101, a modular, extensible and synthesizable embedded system to be used as a reliable platform for:
  - Integrate and evaluate security solutions for embedded/IoT domain
  - Run real applications
  - > Teaching microcontrollers architecture
  - Security training activities for students and professionals
    - > E.g., Capture-the-Flag challenges

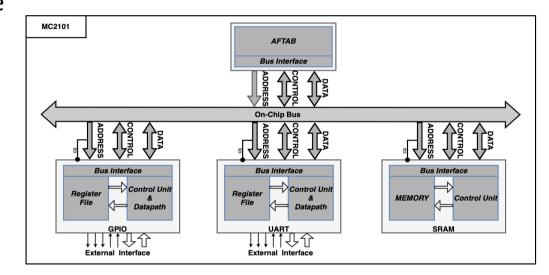
# MC2101 Architecture: overview

- > The microcontroller includes:
  - > A 32-bit RISC-V processor: **AFTAB** 
    - Designed at PoliTO and developed by University of Tehran
    - Sequential core
    - RV32IM Subset RISC-V ISA
      - Integer base + Multiplication and Division Extension
      - Subset of privilege extension for interrupts and exceptions
    - Master of the BUS
    - Access peripherals and RAM in memory mapped mode.



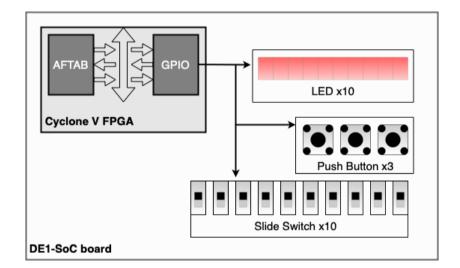
# MC2101 Architecture: overview

- Single BUS interconnecting the processor with memory and peripherals
  - Supports multi-cycle R/W operations
  - Control signals for interrupts
  - Control signals for transfer response
- Minimal set of peripherals designed to provide all necessary I/O functions
  - GPIO, UART



# MC2101 Architecture: GPIO

- General Purpose Input Output (GPIO) peripheral
  - Present in every microcontroller
  - Designed to manage incoming and outcoming digital signals
    - Controlling physical pins
    - Bit-banging operations
- The logic and the software library designed allow to:
  - > configure pins direction
  - read/write pins logic state
  - > enable interrupt on each input pin
  - configure interrupt triggering behavior

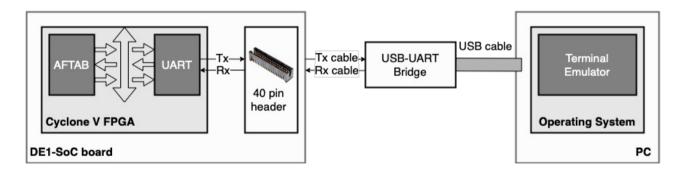


## MC2101 Architecture: UART

- The UART module designed for MC2101 provides a receivertransmitter pair
  - Configurable with different speeds
  - Supporting different data widths
  - Parity codifications
  - > Information status for different error conditions:
    - Overrun Error, Frame Error, Break Interrupt
  - Prioritized interrupts
  - Buffered communications
    - Two dedicated hardware FIFO's

# MC2101 Architecture: UART

- Communication channel between PC and the microcontroller synthesized on FPGA
  - Uart Tx and Rx are bridged to USB
  - > Through a PC terminal, it is possible to send/receive characters
    - > Software libraries integrate *scanf* & *printf* functions

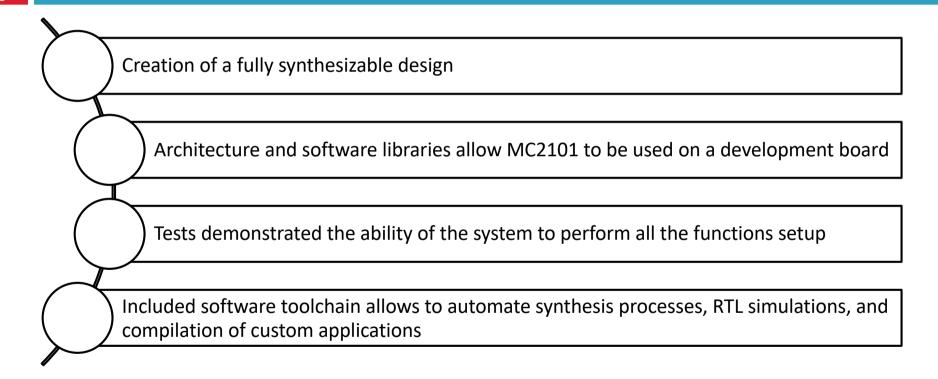


# **Experimental Results**

- Synthesized on Cyclone-V FPGA using Quartus 21.1 software
- Very small percentage of available resources is used
  - Great deal of freedom for future developments

Resource Name	Used Amount	Total Amount	Percentage Used
ALM	2628	32070	8%
FF	3443	64140	5%
PIN	36	457	8%
M10K Memory Bits	131072	4065280	3%
M10K Blocks	16	397	4%

## Conclusions



# Thanks for your attention!

