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Chutung, Hsinchu, Taiwan 310, R.O.C.
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Phison PS3006 Controller

Version 1.2

Contents

Revision History

Revision No	History	Draft Date
0.0	1. Initial issue	Apr.10.2007
1.0	Take out 128 pin package	Oct.11,2007
1.1	1. Page3,Built-in hardware ECC circuit(Reed-Solomon)->(B.C.H.) 2. Page7, FCE7 -> FCE7- Page11, B10 VSSK -> B10 VSS 3. Pin Description add PU/PD field 4. add LQFP-100 Package	Nov.1,2007

1.2	1. Page 44, 45, 46: Add marking information for PS3006 on different package	Nov.14, 2007

A. Features

1. **Support Host Interfaces :**

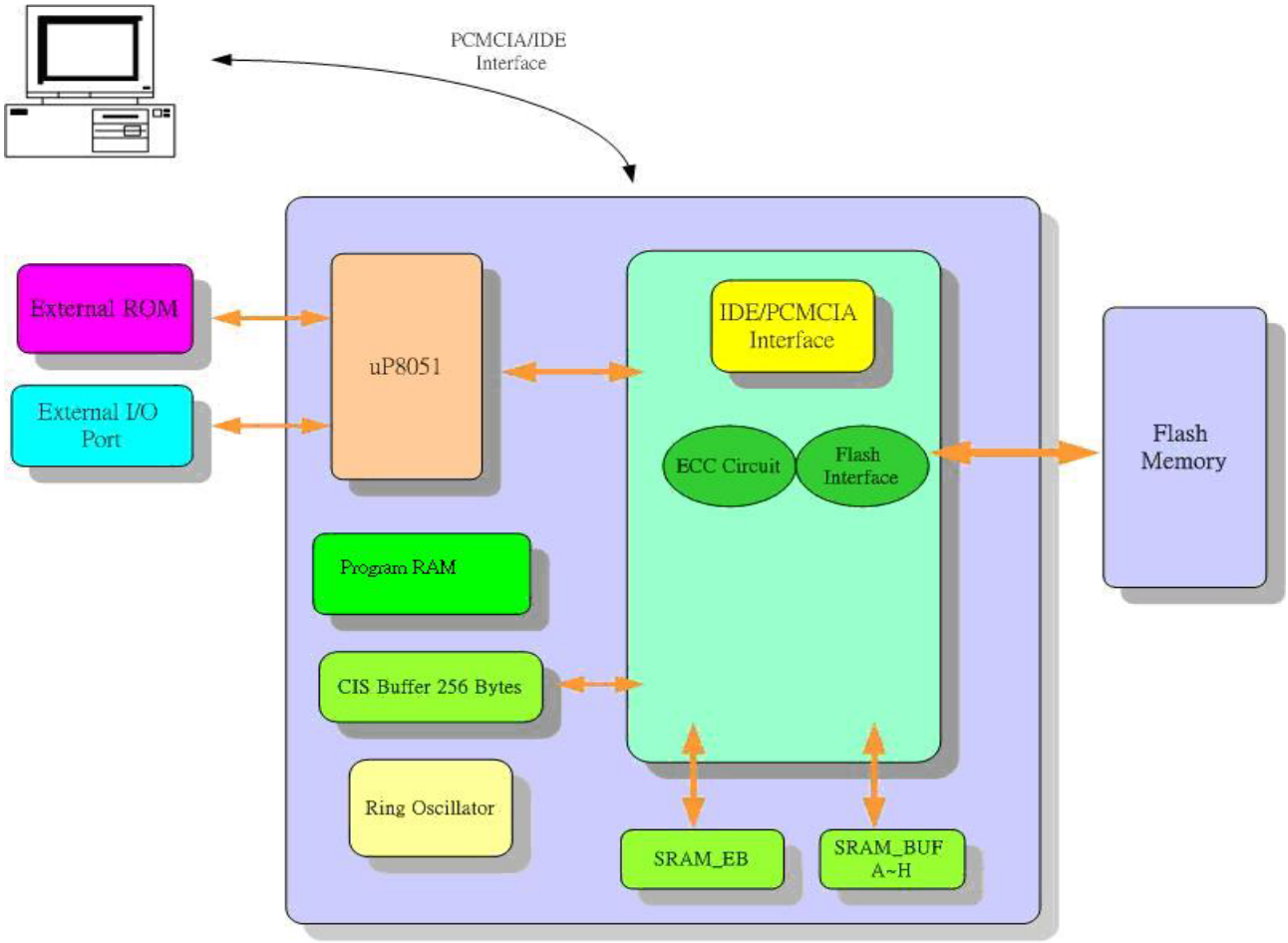
- PCMCIA/IDE Interface (Support to PIO Mode 6 & Multi Word DMA Mode4 & Ultra DMA Mode 6)
  - Fully compatible with CompactFlash Specification Version 3.0
  - Fully compatible with PC Card Standard Release 8.0
  - Fully compatible with the IDE standard interface
  - Host Transfer Rate for PC Card/CompactFlash : 25MB/s (PIO6)
  - Host Transfer Rate for IDE standard interface: 133MB/s (UDMA6)

2. **Build-In NAND Flash Memory Interface(support Individual mode, Dual mode and Quadruple mode)**
   - Build-in hardware ECC circuit (B.C.H.), support max 12 bit ECC.
   - Support SLC(Single level cell) and MLC(Multi level cell) NAND Flash Memory
   - Support 512B per page, 2KB per page, 4KB per page NAND Flash Memory
3. **Build-In 1T RISC uP8051:**
4. **Build-In Oscillator:**
5. **Build-In Low Voltage Detector:**
6. **Build-In Regulator: 3.3V and 1.8V**
7. **100-Pin TQFP/LQFP Package and 85-Ball BGA Package are available.**
8. **Operating Voltage: 2.7~5.5V**
9. **Power Saving implemented**

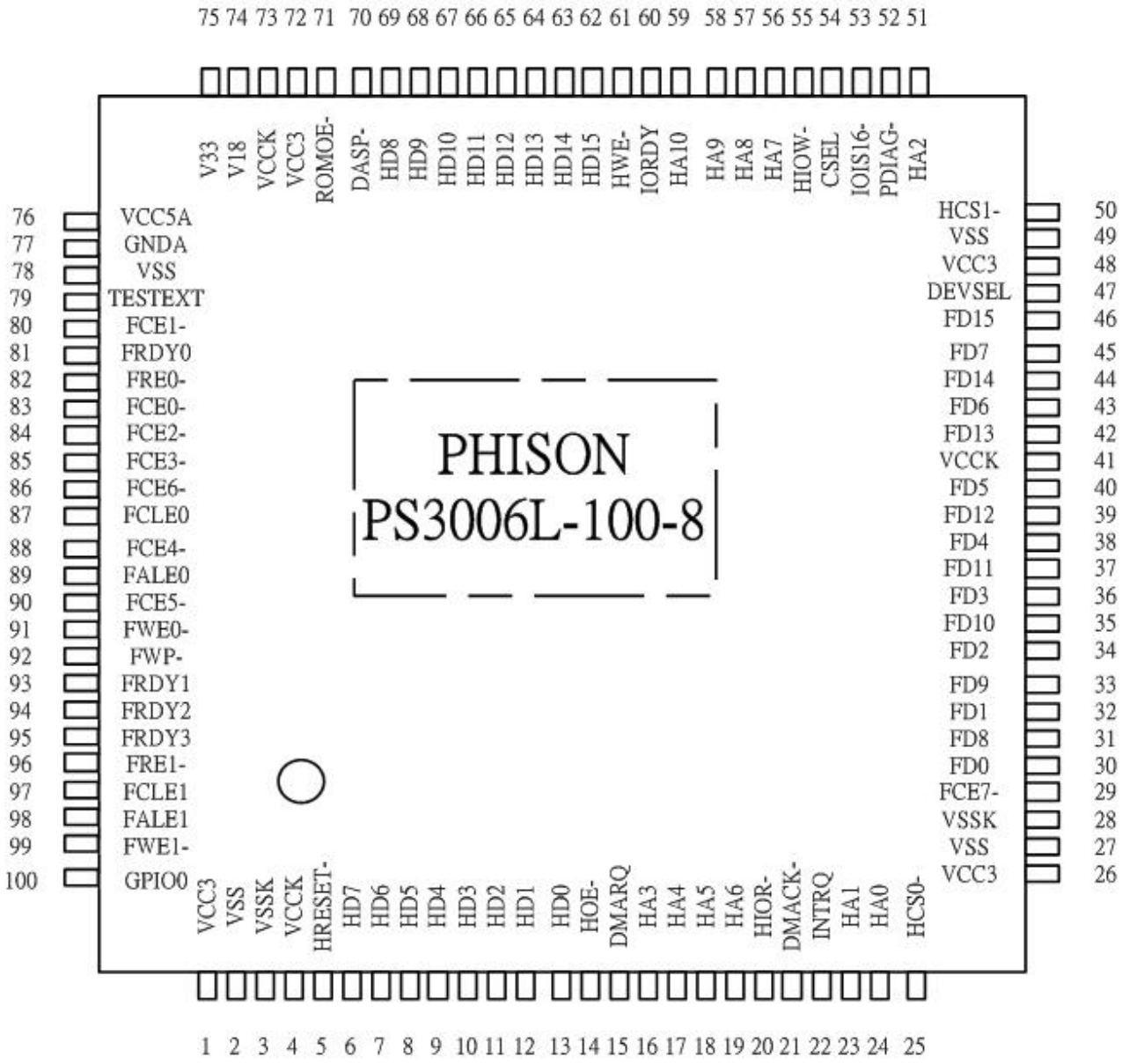
B. General Description

The PHISON PS3006 micro-controller is the best choice for CompactFlash™ card and IDE interface storage devices. It is a powerful chip with excellent performance and low cost. All flash modules, commercial or industrial, designed in with this controller can exclude the mechanical parts which have the full advantage of anti vibration and extremely low power consumption. With built in regulator and oscillator, this reduces cost for external components. With the latest Program RAM and SMART commands integrated into this one chip solution, efforts from R/D to mass production will greatly decrease, at the same time, providing the edge to shortening time to market.

C. Block Diagram

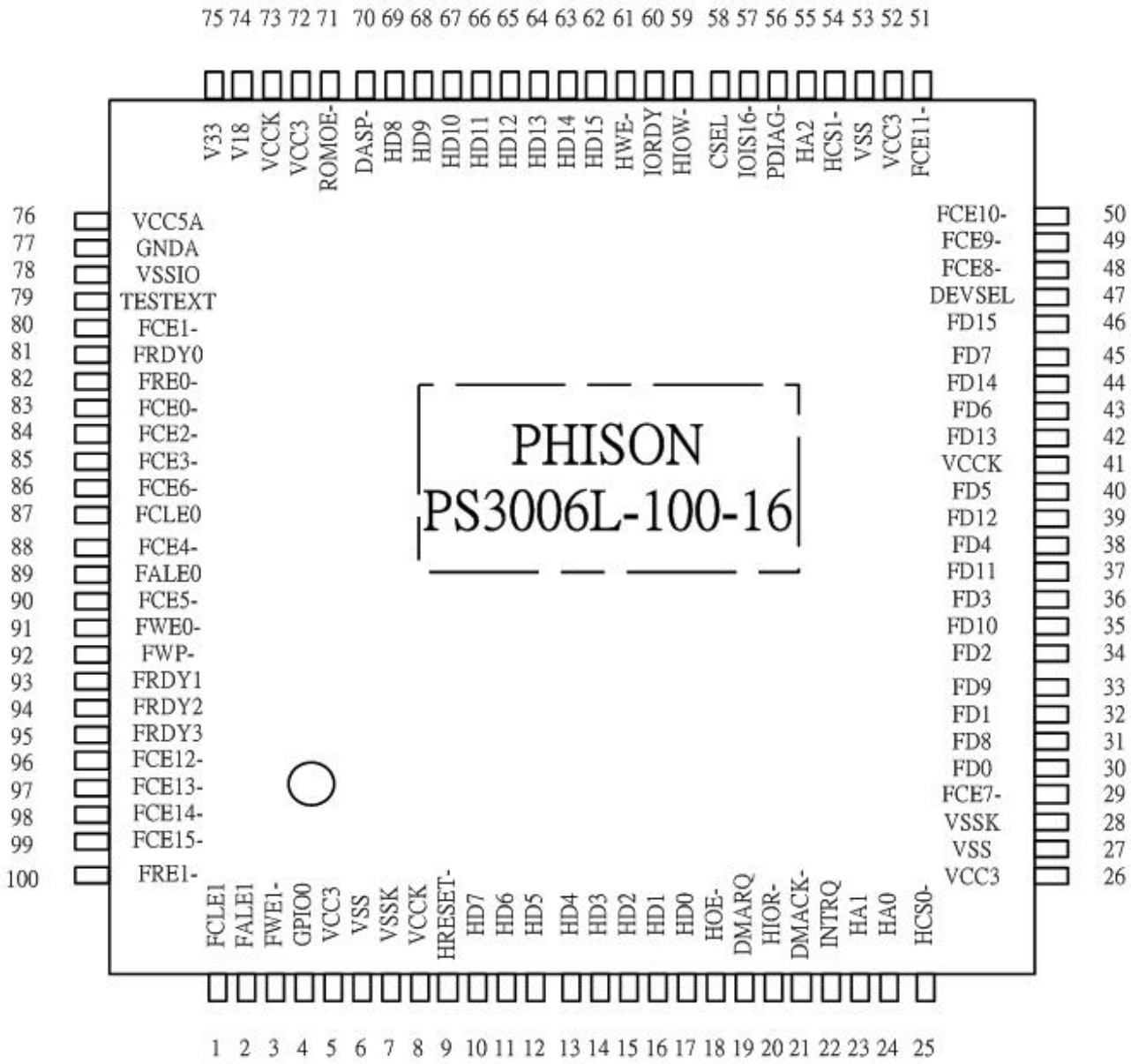

PCMCIA/IDE
Interface
External ROM
External I/O
Port
uP8051
IDE/PCMCIA
Interface
ECC Circuit
Flash
Interface
Flash
Memory
Program RAM
CIS Buffer 256 Bytes
Ring Oscillator
SRAM_EB
SRAM_BUF
A~H

D1. PACKAGE TYPE : TQFP/LQFP100 (8CE)



1	VCC3	26	VCC3	51	HA2	76	VCC5A
2	VSS	27	VSS	52	PDIAG-	77	GNDA
3	VSSK	28	VSSK	53	IOIS16-	78	VSS
4	VCCK	29	FCE7-	54	CSEL	79	TESTEXT
5	HRESET-	30	FD0	55	HIOW-	80	FCE1-
6	HD7	31	FD8	56	HA7	81	FRDY0
7	HD6	32	FD1	57	HA8	82	FRE0-
8	HD5	33	FD9	58	HA9	83	FCE0-
9	HD4	34	FD2	59	HA10	84	FCE2-
10	HD3	35	FD10	60	IORDY	85	FCE3-
11	HD2	36	FD3	61	HWE-	86	FCE6-
12	HD1	37	FD11	62	HD15	87	FCLE0
13	HD0	38	FD4	63	HD14	88	FCE4-
14	HOE-	39	FD12	64	HD13	89	FALE0
15	DMARQ	40	FD5	65	HD12	90	FCE5-
16	HA3	41	VCCK	66	HD11	91	FWE0-
17	HA4	42	FD13	67	HD10	92	FWP-
18	HA5	43	FD6	68	HD9	93	FRDY1
19	HA6	44	FD14	69	HD8	94	FRDY2
20	HIOR-	45	FD7	70	DASP-	95	FRDY3
21	DMACK-	46	FD15	71	ROMOE-	96	FRE1-
22	INTRQ	47	DEVSEL	72	VCC3	97	FCLE1
23	HA1	48	VCC3	73	VCCK	98	FALE1
24	HA0	49	VSS	74	V18	99	FWE1-
25	HCS0-	50	HCS1-	75	V33	100	GPIO0

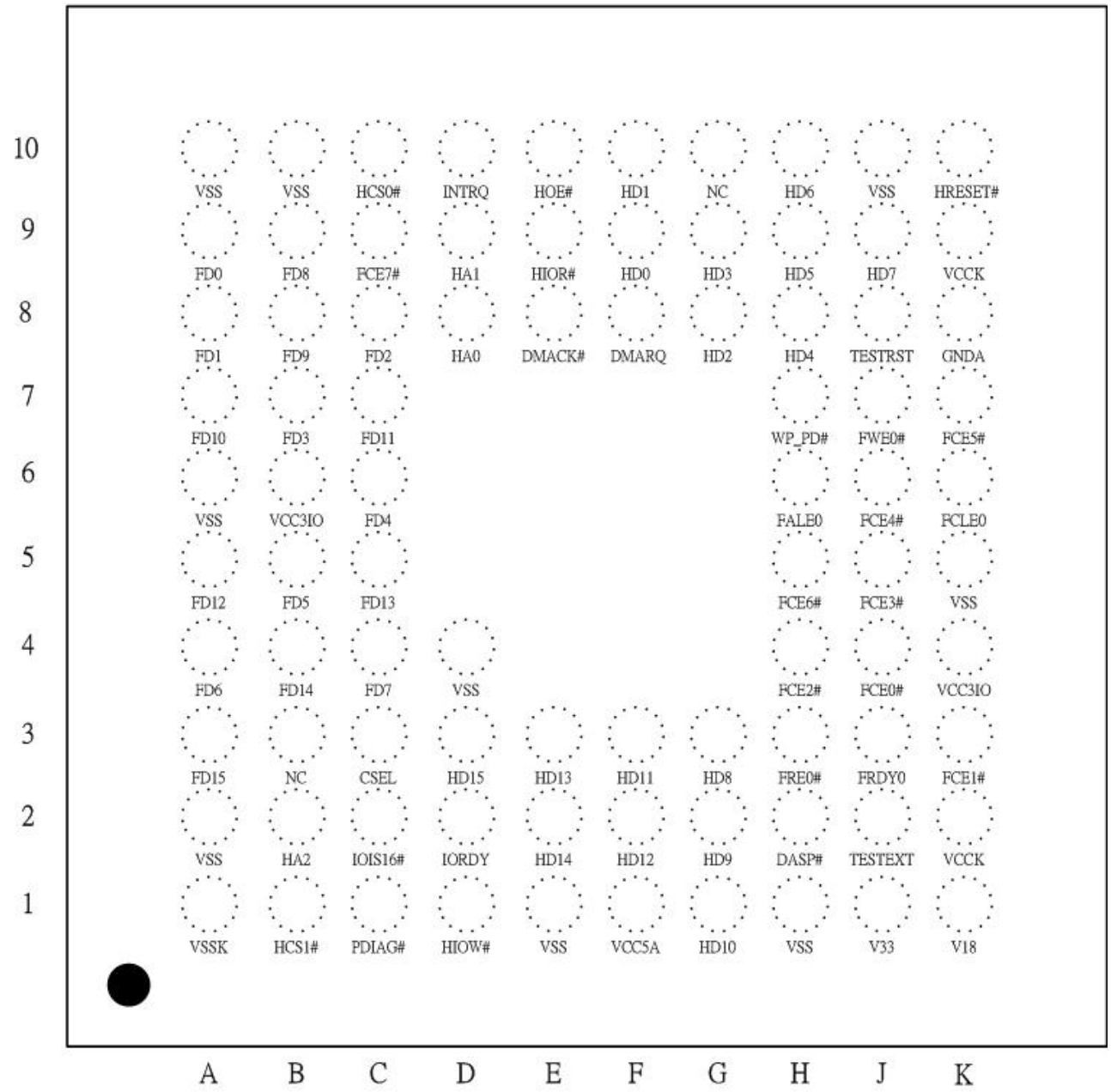
D2. PACKAGE TYPE : TQFP/LQFP100 (16CE)



1	FCLE1	26	VCC3	51	FCE11-	76	VCC5A
2	FALE1	27	VSS	52	VCC3	77	GNDA
3	FWE1-	28	VSSK	53	VSS	78	VSS
4	GPIO0	29	FCE7-	54	HCS1-	79	TESTEXT
5	VCC3	30	FD0	55	HA2	80	FCE1-
6	VSS	31	FD8	56	PDIAG-	81	FRDY0
7	VSSK	32	FD1	57	IOIS16-	82	FRE0-
8	VCCK	33	FD9	58	CSEL	83	FCE0-
9	HRESET-	34	FD2	59	HIOW-	84	FCE2-
10	HD7	35	FD10	60	IORDY	85	FCE3-
11	HD6	36	FD3	61	HWE-	86	FCE6-
12	HD5	37	FD11	62	HD15-	87	FCLE0
13	HD4	38	FD4	63	HD14-	88	FCE4-
14	HD3	39	FD12	64	HD13-	89	FALE0
15	HD2	40	FD5	65	HD12-	90	FCE5-
16	HD1	41	VCCK	66	HD11-	91	FWE0-
17	HD0	42	FD13	67	HD10-	92	FWP-
18	HOE-	43	FD6	68	HD9-	93	FRDY1
19	DMARQ	44	FD14	69	HD8-	94	FRDY2
20	HIOR-	45	FD7	70	DASP-	95	FRDY3
21	DMACK-	46	FD15	71	ROMOE-	96	FCE12-
22	INTRQ	47	DEVSEL	72	VCC3	97	FCE13-
23	HA1	48	FCE8-	73	VCCK	98	FCE14-
24	HA0	49	FCE9-	74	V18	99	FCE15-
25	HCS0-	50	FCE10-	75	V33	100	FRE1-

D3. PACKAGE TYPE : BGA85

TOP VIEW (Balls Face Down)



A1	VSSK	C3	CSEL	F2	HD12	J2	TESTEXT
A2	VSS	C4	FD7	F3	HD11	J3	FRDY0
A3	FD15	C5	FD13	F8	DMARQ	J4	FCE0-
A4	FD6	C6	FD4	F9	HD0	J5	FCE3-
A5	FD12	C7	FD11	F10	HD1	J6	FCE4-
A6	VSS	C8	FD2	G1	HD10	J7	FWE0-
A7	FD10	C9	FCE7-	G2	HD9	J8	TESTRST
A8	FD1	C10	HCS0-	G3	HD8	J9	HD7
A9	FD0	D1	HIOW-	G8	HD2	J10	VSS
A10	VSS	D2	IORDY	G9	HD3	K1	V18
B1	HCS1-	D3	HD15	G10	NC	K2	VCCK
B2	HA2	D4	VSS	H1	VSS	K3	FCE1-
B3	NC	D8	HA0	H2	DASP-	K4	VCC3IO
B4	FD14	D9	HA1	H3	FRE0-	K5	VSS
B5	FD5	D10	INTRQ	H4	FCE2-	K6	FCLE0
B6	VCC3IO	E1	VSS	H5	FCE6-	K7	FCE5-
B7	FD3	E2	HD14	H6	FALE0	K8	GNDA
B8	FD9	E3	HD13	H7	WP_PD-	K9	VCCK
B9	FD8	E8	DMACK-	H8	HD4	K10	HRESET-
B10	VSS	E9	HIOR-	H9	HD5		
C1	PDIAG-	E10	HOE-	H10	HD6		
C2	IOIS16-	F1	VCC5A	J1	V33		

E. Pin Description

Pin Name	Dir.	PU/PD	Description
HA[10:0] (PC Card Memory Mode) HA[10:0] (PC Card I/O Mode) HA[2:0] (True IDE Mode)	I	PD 300K	These address lines along with the DMACK-(REG-) signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, only HA[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
HD[15:0] (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I/O	PD 300K	These lines carry the Data, Commands and Status information between the host and the controller. HD[0] is the LSB of the Even Byte of the Word. HD[8] is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode all Task File operations occur in byte mode on the low order bus HD[0]-HD[7] while all data transfers are 16bit using HD[0]-HD[15].
HCS0-,HCS1- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	These input signals are used to select the card and to indicate to the card whether a byte or a word operation is being performed. HCS1- always accesses the odd byte of the word. HCS0- accesses the even byte or the Odd byte of the word depending on the A0 and HCS1-. This signal is the same as the PC Card Memory Mode signal HCS0- is the address range select for the task file registers while HCS1- is used to select the Alternate Status Register and the Device Control Register. While DMACK- is asserted, HCS0- and HCS1- shall be held negated and the width of the transfers shall be 16 bits.
DMACK- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.
HOE- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.

HWE- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode this input signal is not used and should be connected to VCC by the host.
HIOR- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer. In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
HIOW- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
HRESET- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I	PU 300K	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode this input pin is the active low hardware reset from the host.
DMARQ (PC Card Memory Mode)	O		This signal is not used in this mode.

(PC Card I/O Mode) (True IDE Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by HIOR- and HIOW-. This signal is used in a handshake manner with DMACK-, i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.
HINTRQ (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O		In Memory Mode this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. After the CompactFlash Storage Card has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
IOIS16- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	PU 300K	The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. When the CompactFlash Storage Card is configured for I/O Operation IOIS16- is used for the -I/O Selected is 16 Bit Port function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.
PDIAG- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I/O	PU 300K	This signal is asserted high (BVD1 is not supported). This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. This input/ output is the Pass Diagnostic signal in the Master/ Slave handshake protocol
DASP- (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I/O	PU 300K	This signal is asserted high (BVD2 is not supported). This signal is held negated. This input/ output is the Disk Active/Slave Present signal in the Disk Master/Slave handshake protocol.

CSEL (PC Card Memory Mode)	I	PU 300K	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
(PC Card I/O Mode) (True IDE Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
IORDY (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O		This signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress This signal is the same as the PC Card Memory Mode signal In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. When Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. When Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
FCE-[15:0]	O	PU 75K	Flash Chip Enable, Low active.
FD[15:0]	I/O	PD 75K	Flash Data Bus
FALE[1:0]	O		Flash Address Latch Enable, High active.
FCLE[1:0]	O		Flash Command Latch Enable, High active.
FRE[1:0]	O		Flash Read Control signal, Low active.
FWE[1:0]	O		Flash Write Control signal, Low active.
FWP-	I/O		Flash Write Protect Control signal, Low active.
FRDY0, FRDY1	I	PU 75K	Flash Ready/Busy signal.
Test[2:0]	I/O	PD 75K	Test Mode Signal.
TestExt	I/O		Test Mode Signal.
DEVSel	I		Select flash/MMC interface
GPIO0 GPIO2 GPIO3	I/O	PU 75K	General purpose input/output pins
VCC5A	VCC		5V/3.3V input
V18	VCC		1.8V output
V33	VCC		3.3V output
VCC3	VCC		3.3V in
VCCK	VCC		1.8V in
GND	GND		
GNDA	GND		

*Note :

1. FCE[15:8] and ext ROM Data[7:0] share the same pins

2. All I/O Pin are push pull type.

F. System Power Consumption

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
Iccr	Read current	5V		75		mA
Iccw	Write current	5V		75		mA
Ipd	Power down current	5V				mA
Iccr	Read current	3.3V		55		mA
Iccw	Write current	3.3V		55		mA
Ipd	Power down current	3.3V				mA
Ireg	Regulator leakage current	3.3V				mA

G. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit	Remark
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
3	Ta	Operating Temperature	0	+70	°C	Commercial version
4	Tst	Storage Temperature	0	+85	°C	Commercial version
5	Ta	Operating Temperature	-40	+85	°C	Industry version
6	Tst	Storage Temperature	-40	+100	°C	Industry version

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature	T_a	-40	+25	+125	°C
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

Schmit Trigger Pin:

I = Input O = Output

Pin Name	Pin Number	IOL (mA)	Dir	
HOE-, HWE-, HIOR-, HIOW-	4	12	I	TTL Level Pull-up 300K(SCHMT)
REG-, CE1-, CE2-	3	12	I	TTL Level Pull-up 300K(SCHMT)
HRST	1	12	I	TTL Level(SCHMT)

H. DC Characters

1. DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VCC3I	Power Supply	3.3V I/O	3.0	3.3	3.6	V
VCC3O	Power Supply		3.0	3.3	3.6	V
Temp	Junction Temperature		-40	25	125	°C
Vt-	Schmitt Trigger Negative Going threshold voltage	CMOS		1.1		V
Vt+	Schmitt Trigger Positive Going threshold voltage			1.6		V
Vol	Output Low voltage	|Iol| = 4 ~ 32 mA			0.4	V
Voh	Output High voltage	|Ioh| = 4 ~ 32 mA	2.4			V
Rpu	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

2. DC characteristics of 5V tolerance I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VCC3I	Power Supply	3.3V I/O	3.0	3.3	3.6	V
VCC3O	Power Supply		3.0	3.3	3.6	V
Temp	Junction Temperature		-40	25	125	°C
Vt-	Schmitt Trigger Negative Going threshold voltage	TTL (3.3V)		0.85		V
Vt+	Schmitt Trigger Positive Going threshold voltage			1.25		V
Vt-	Schmitt Trigger Negative Going threshold voltage	TTL (5V)		1.05		V
Vt+	Schmitt Trigger Positive Going threshold voltage			1.75		V
Vol	Output Low voltage	|Iol| = 4 ~ 32 mA			0.4	V
Voh	Output High voltage	|Ioh| = 4 ~ 32 mA	2.4			V
Rpu	Input Pull-Up Resistance	PU=high, PD=low	200	300	450	KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low	200	300	450	KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

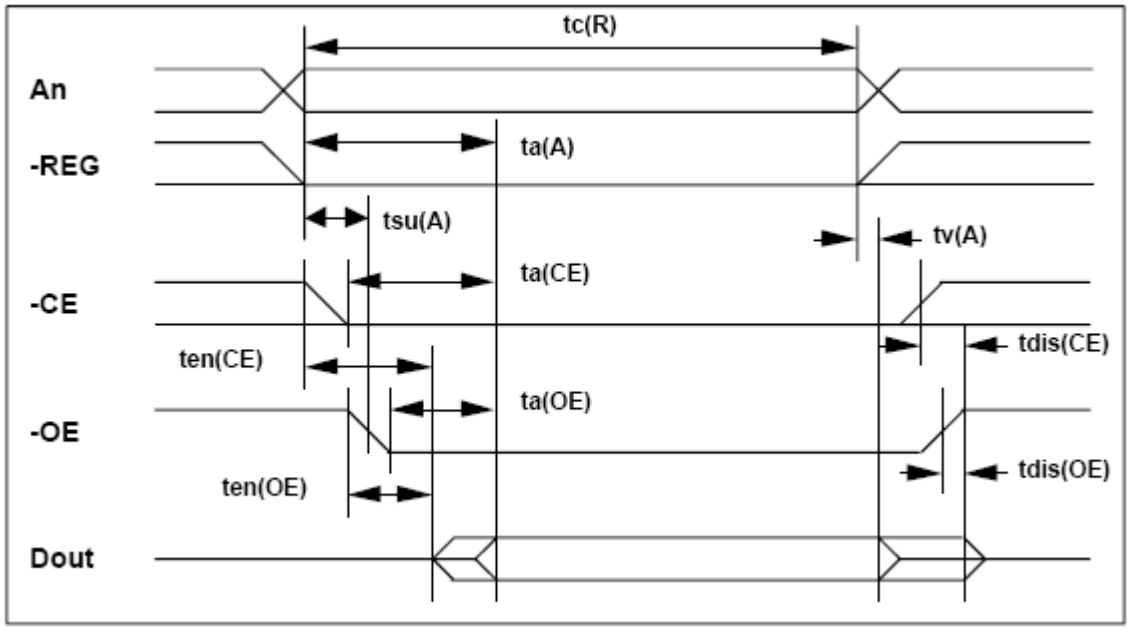
I. AC Characters

I1. PCMCIA Interface

[Attribute Memory Read Timing]

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

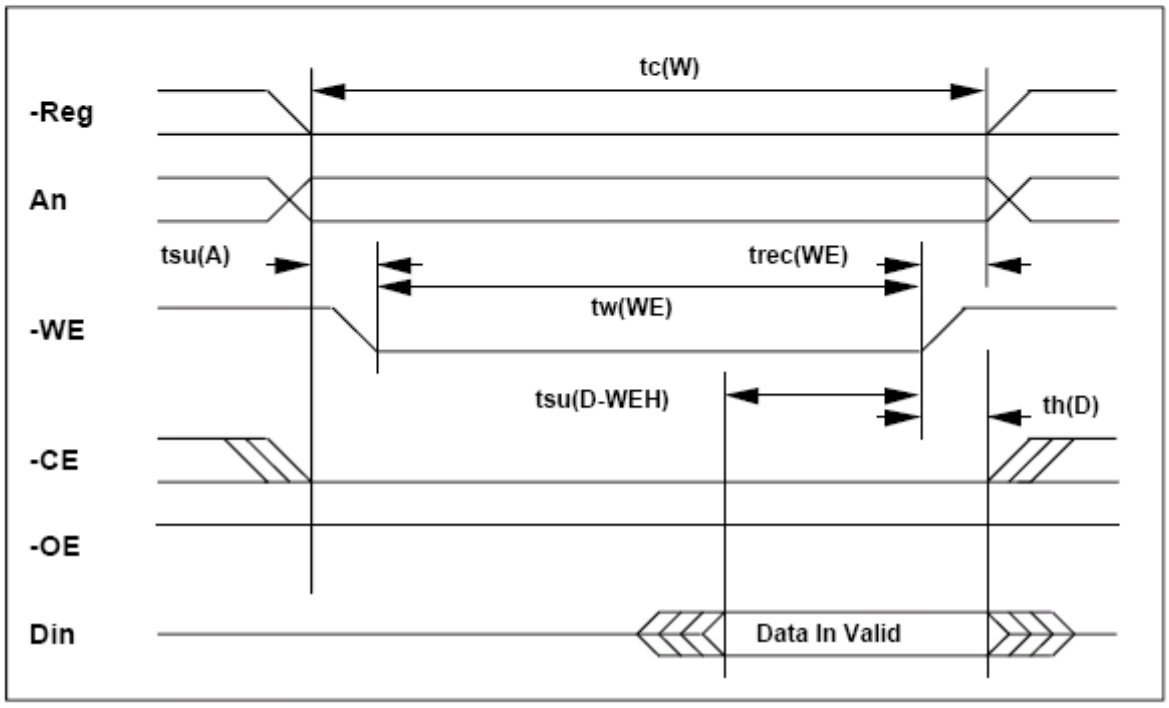
Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.



[Attribute Memory Write Timing]

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min ns	Max ns
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

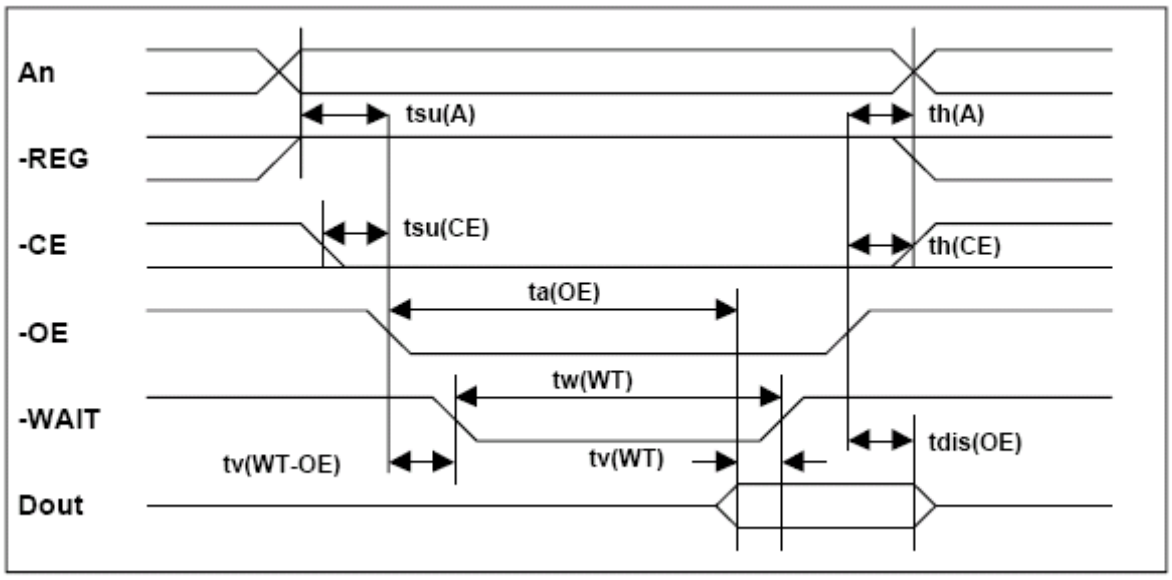
Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.



[Common Memory Read Timing]

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[1]

Notes: 1) –WAIT is not supported in this mode.
2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

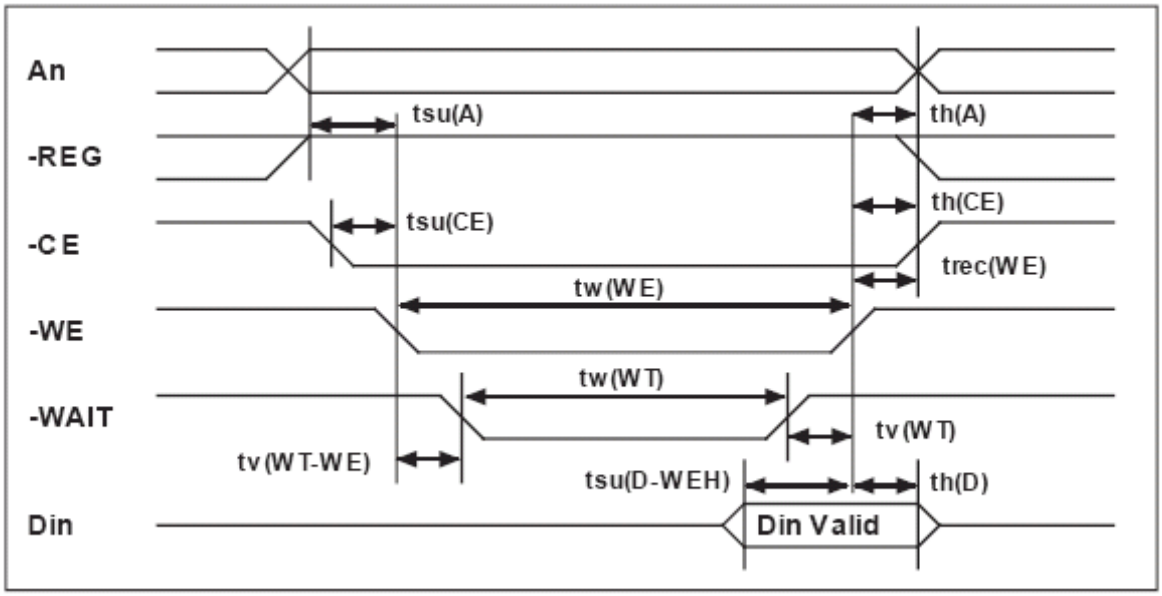


[Common Memory Write Timing]

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[1]

Notes: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.


An
-REG
-CE
-WE
-WAIT
Din
tsu(A)
th(A)
tsu(CE)
th(CE)
trec(WE)
tw(WE)
tw(WT)
tv(WT)
tv(WT-WE)
tsu(D-WEH)
th(D)
Din Valid

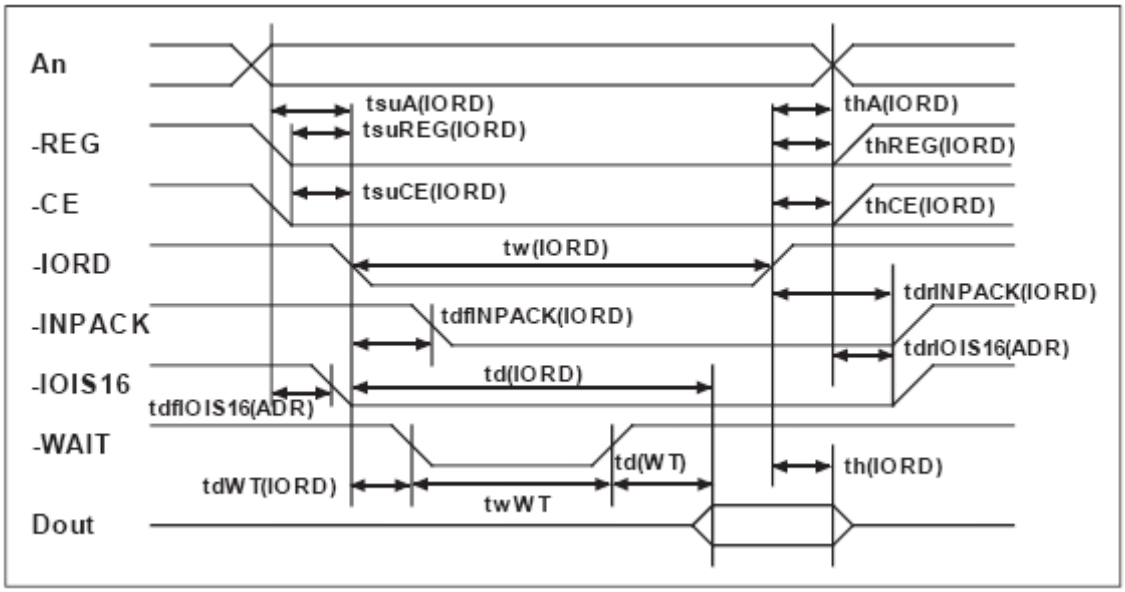
[I/O Read Timing]

Cycle Time Mode:			255 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tIGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tIGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.


An
-REG
-CE
-IORD
-INPACK
-IOIS16
-WAIT
Dout
tsuA(IORD)
tsuREG(IORD)
tsuCE(IORD)
tw(IORD)
tdfINPACK(IORD)
tdfIOIS16(ADR)
td(IORD)
tdWT(IORD)
td(WT)
twWT
thA(IORD)
thREG(IORD)
thCE(IORD)
tdrINPACK(IORD)
tdrIOIS16(ADR)
th(IORD)

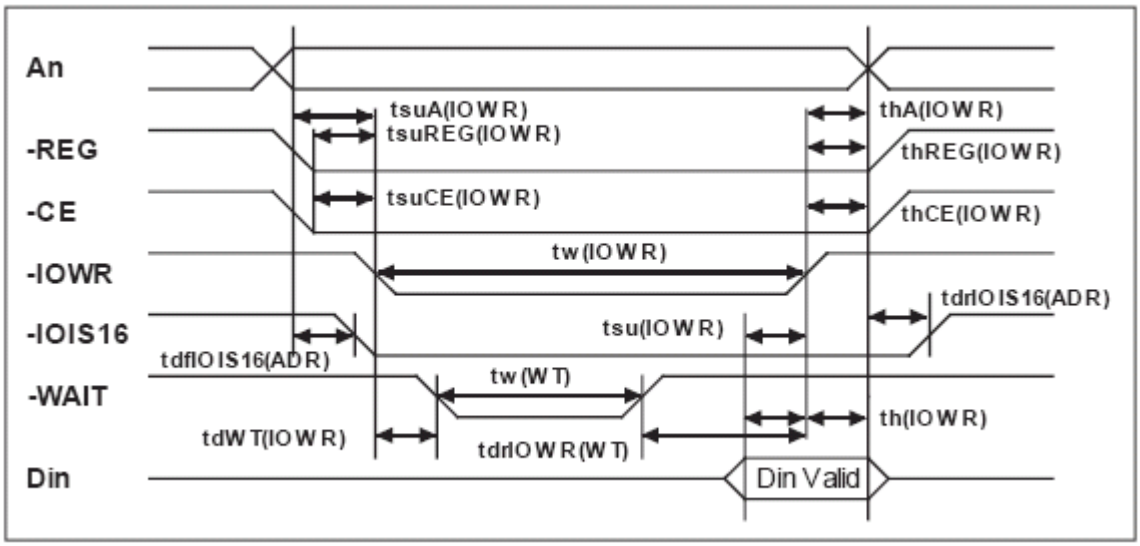
[I/O Write Timing]

Cycle Time Mode:			255 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOWR[3]	tdWT(IOWR)	tIWLWTL		35		35		35		na[2]
IOWR high from Wait high[3]	tdrIOWR (WT)	tWTJIWH	0		0		0		na[2]	
Wait Width Time[3]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.


An
-REG
-CE
-IOWR
-IOIS16
-WAIT
Din
tsuA(IOWR)
tsuREG(IOWR)
tsuCE(IOWR)
tw(IOWR)
tsu(IOWR)
tdfIOIS16(ADR)
tw(WT)
tdWT(IOWR)
tdrIOWR(WT)
thA(IOWR)
thREG(IOWR)
thCE(IOWR)
tdrIOIS16(ADR)
th(IOWR)
Din Valid

I2. IDE Interface Timing

[PIO Mode]

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

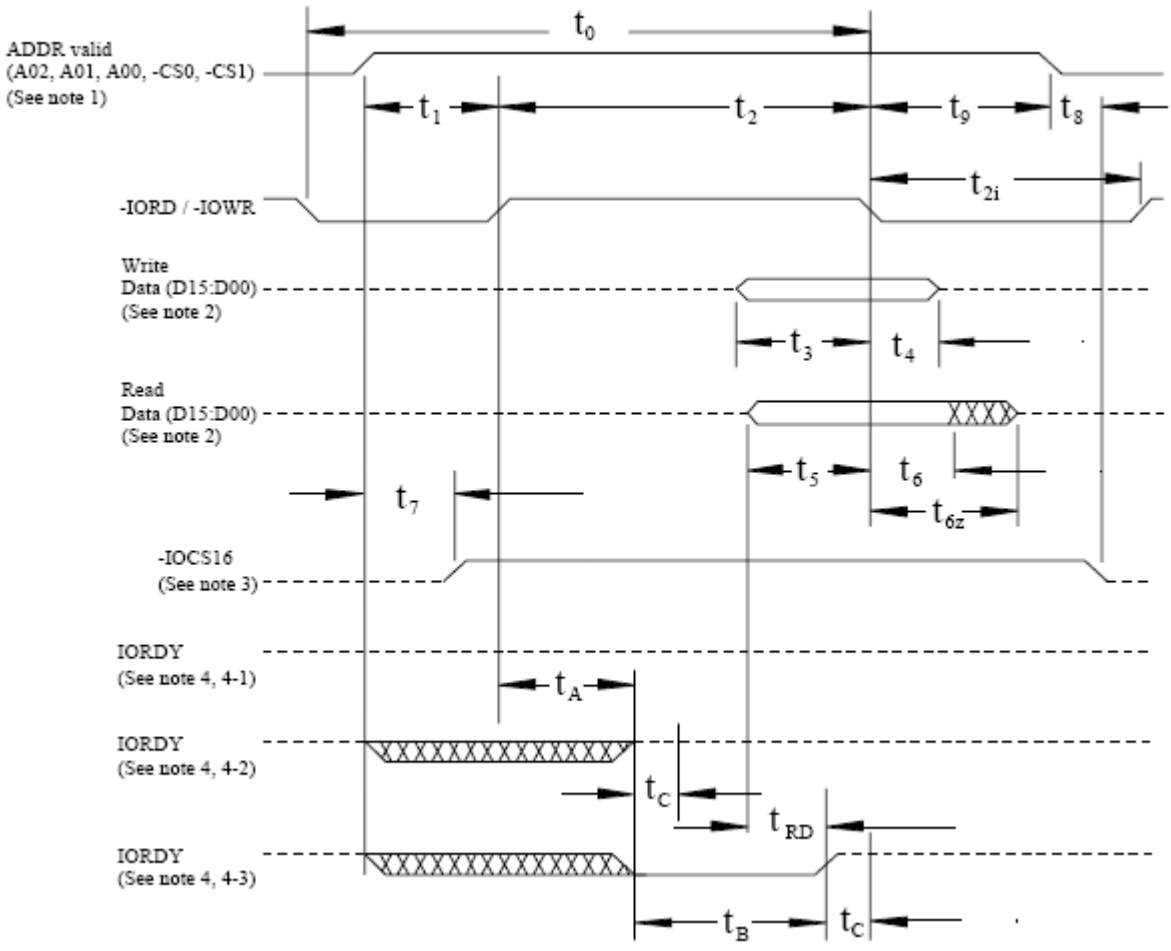
1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.



Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

[Ultra DMA Mode 6]

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)		Mode 6 (in ns)		Measurement location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		Note 3
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	Note 4
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

NOTES –

1 All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2 All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and DMARDY- transitions are measured at the sender connector.

3 The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4 The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5 The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge) (See note 2,5)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid) (See note 2,5)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge) (See note 3)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid) (See note 3)
t_{CS}	CRC word setup time at device (See note 2)
t_{CH}	CRC word hold time device (See note 2)
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK- negation) (See note 3)
t_{CVH}	CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid) (See note 3)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time (See note 1)
t_{MLI}	Interlock time with minimum (See note 1)
t_{UI}	Unlimited interlock time (See note 1)
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY (See note 4)
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

NOTES –

1 The parameters t_{UI}, t_{MLI} (in Figure 74 and Figure 75), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

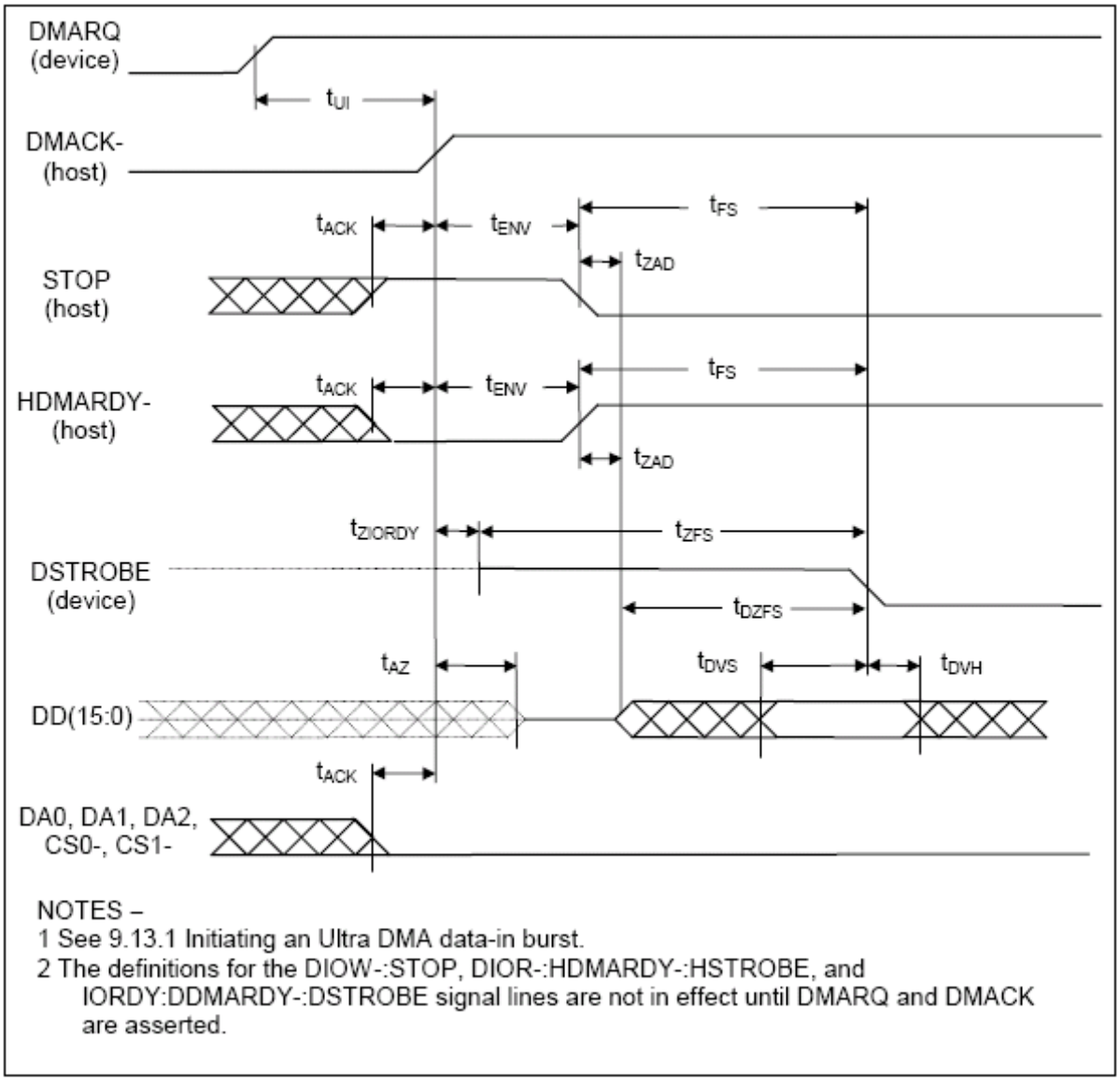
2 80-conductor cabling (See 7.3) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

3 Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4 For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

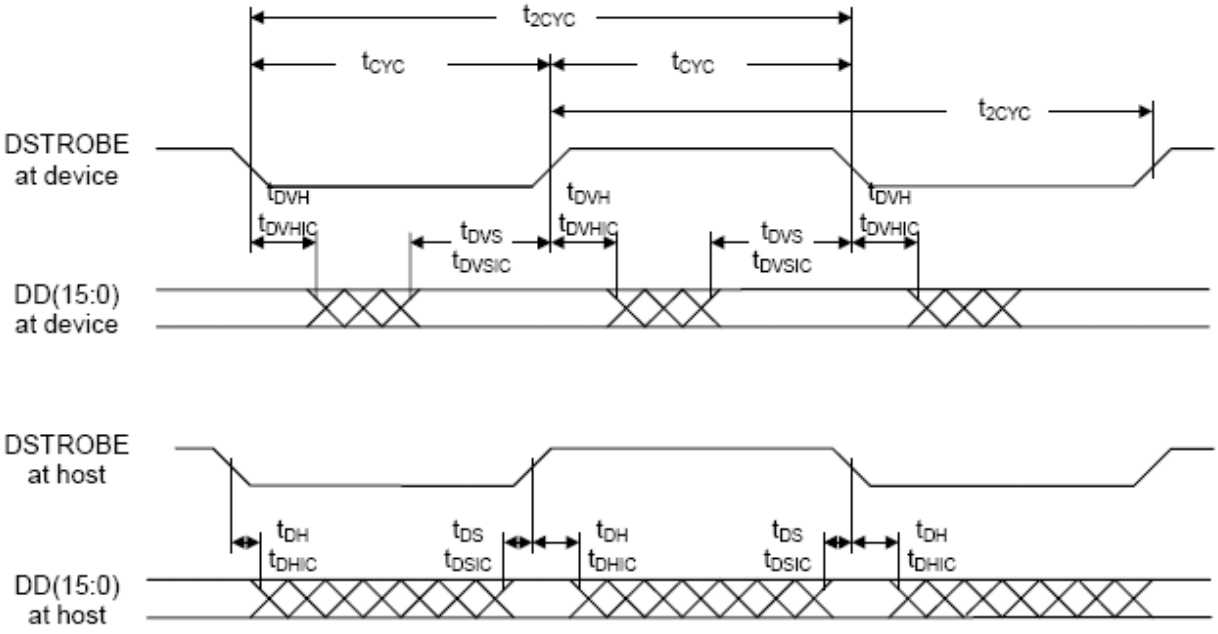
5 The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

[Initial an Ultra DMA Data in Burst]



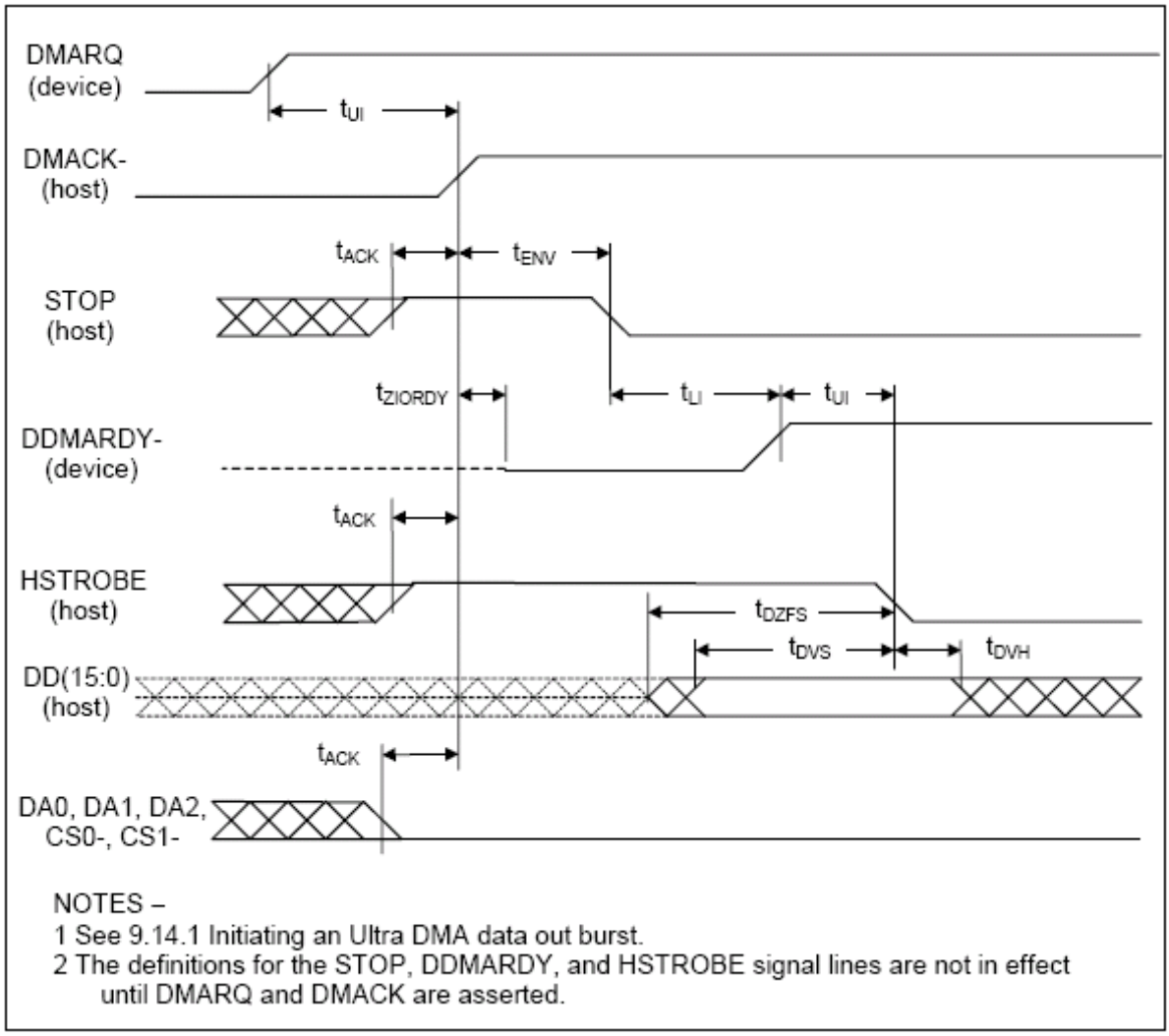
NOTES –
1 See 9.13.1 Initiating an Ultra DMA data-in burst.
2 The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

[Sustained Ultra DMA Data-in Burst]



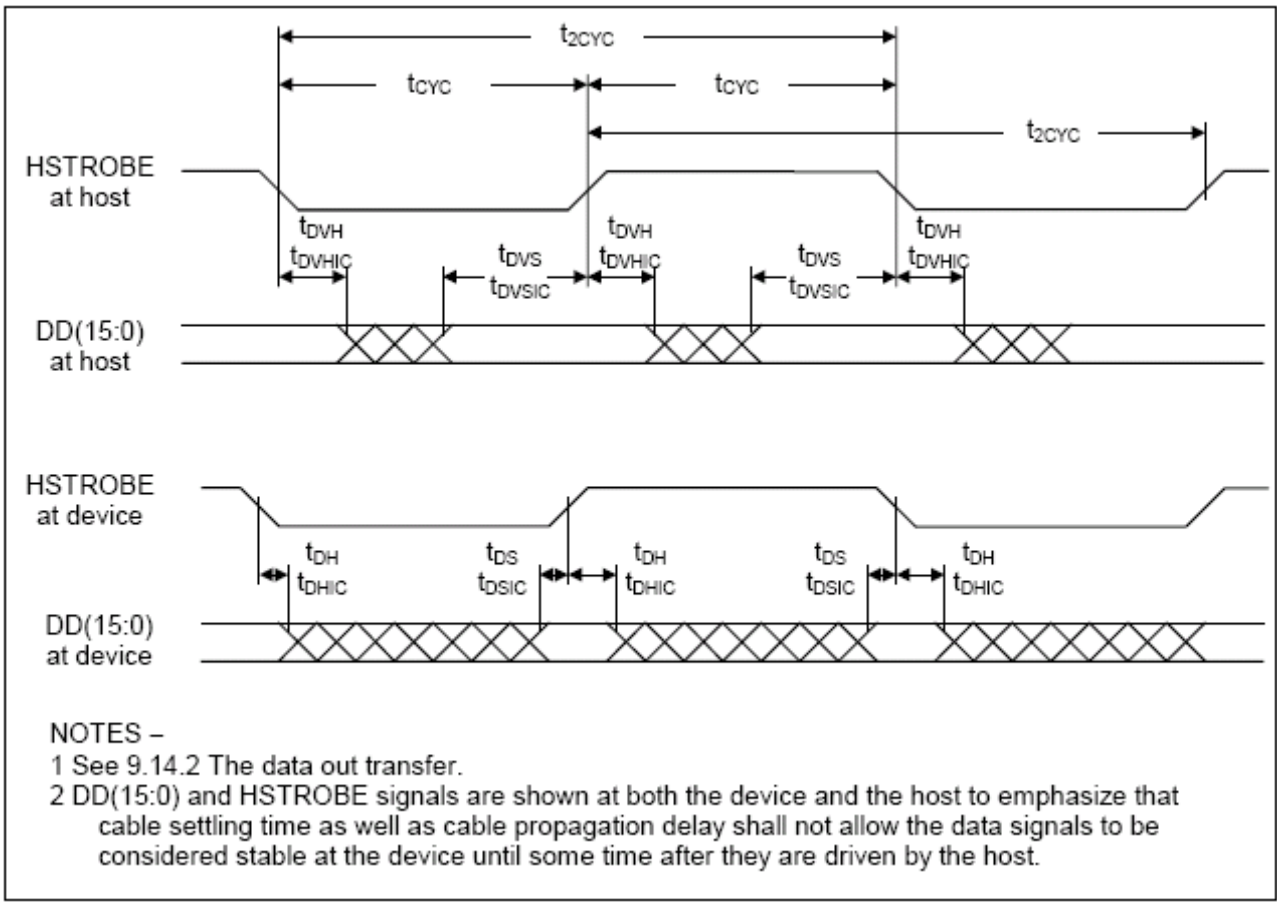
NOTES –
1 See 9.13.2 The data in transfer.
2 DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

[Initialing an Ultra DMA data-out burst]



NOTES –
1 See 9.14.1 Initiating an Ultra DMA data out burst.
2 The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

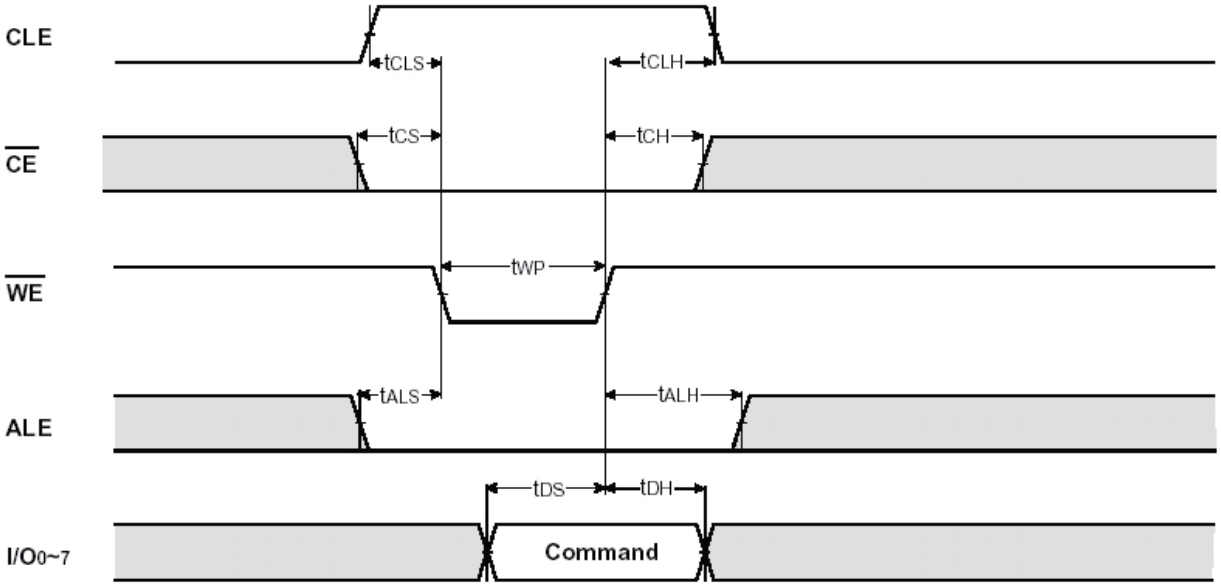
[Sustained Ultra DMA Data-out burst]



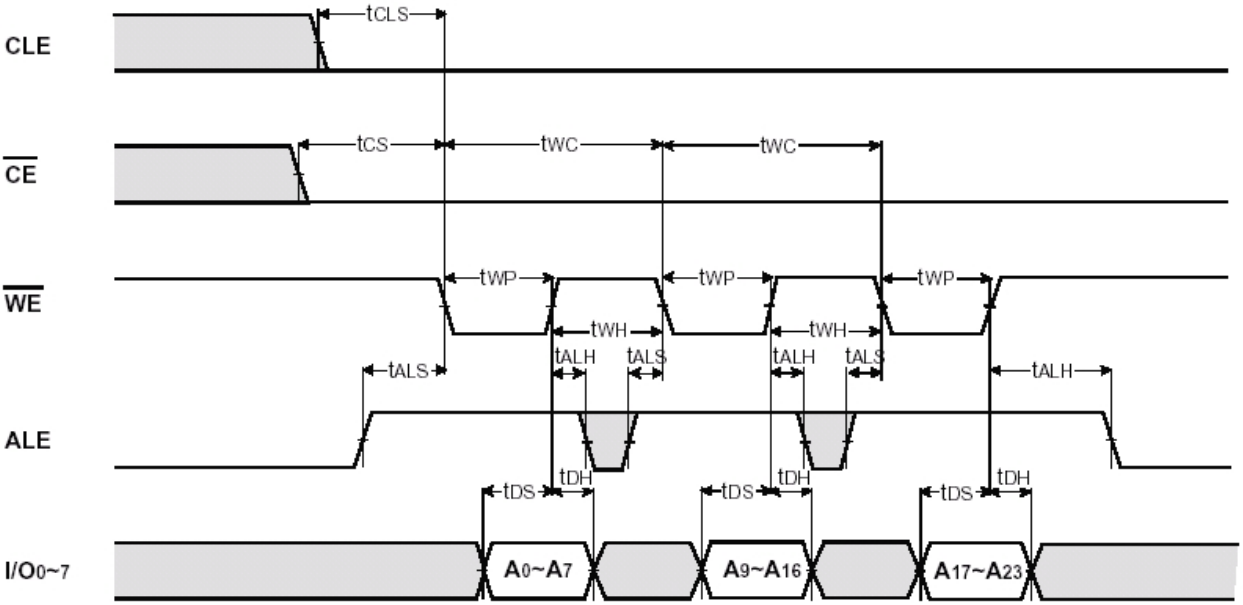
NOTES –
1 See 9.14.2 The data out transfer.
2 DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

I3. Flash Interface Timing

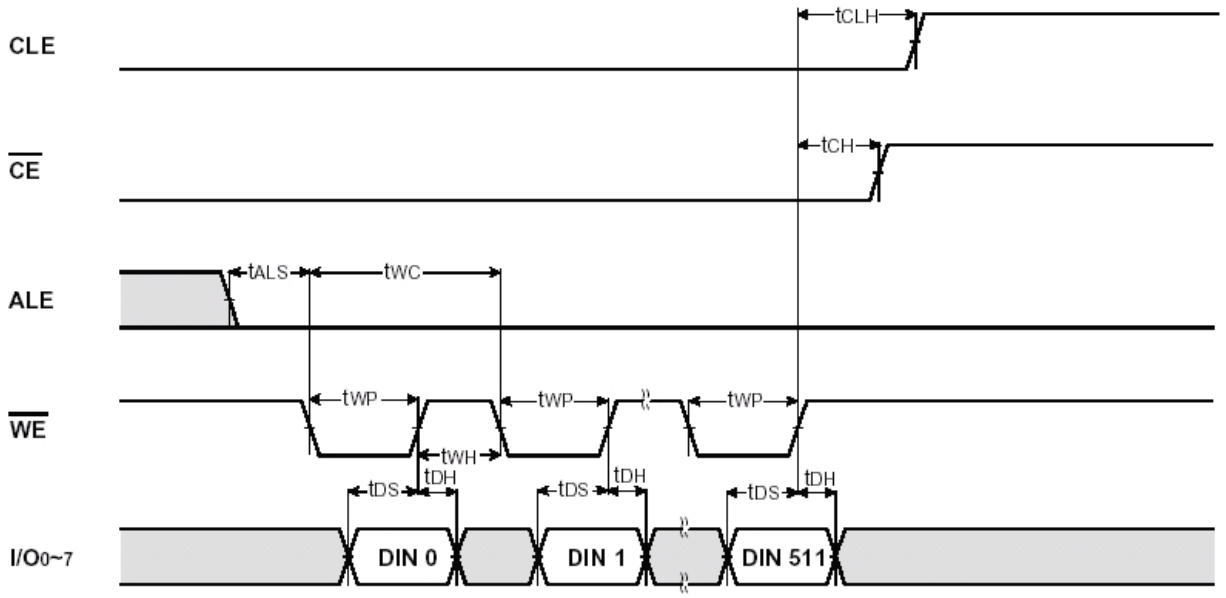
[Command Latch Cycle]



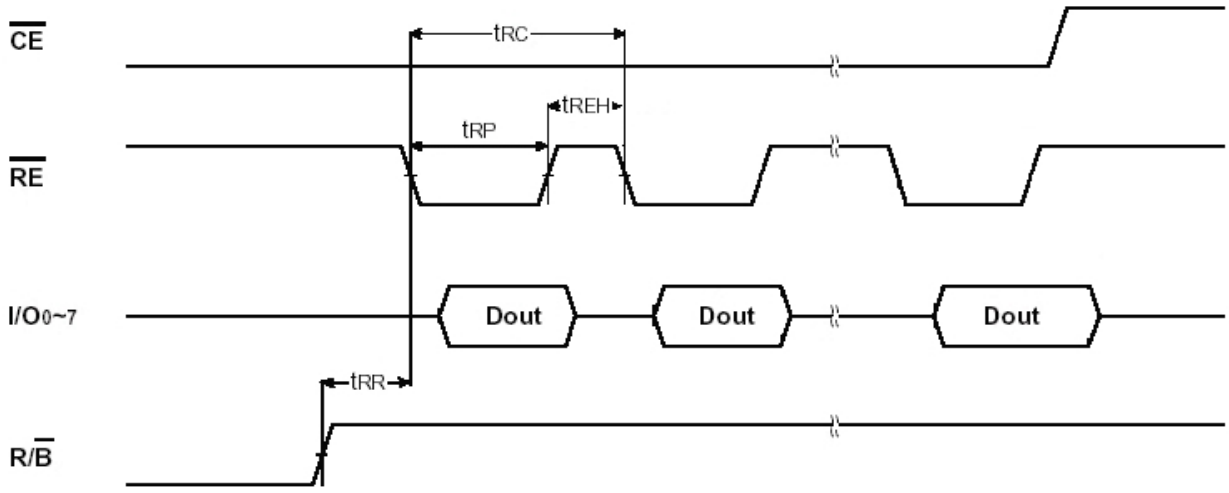
[Address Latch Cycle]



[Input Data Latch Cycle]

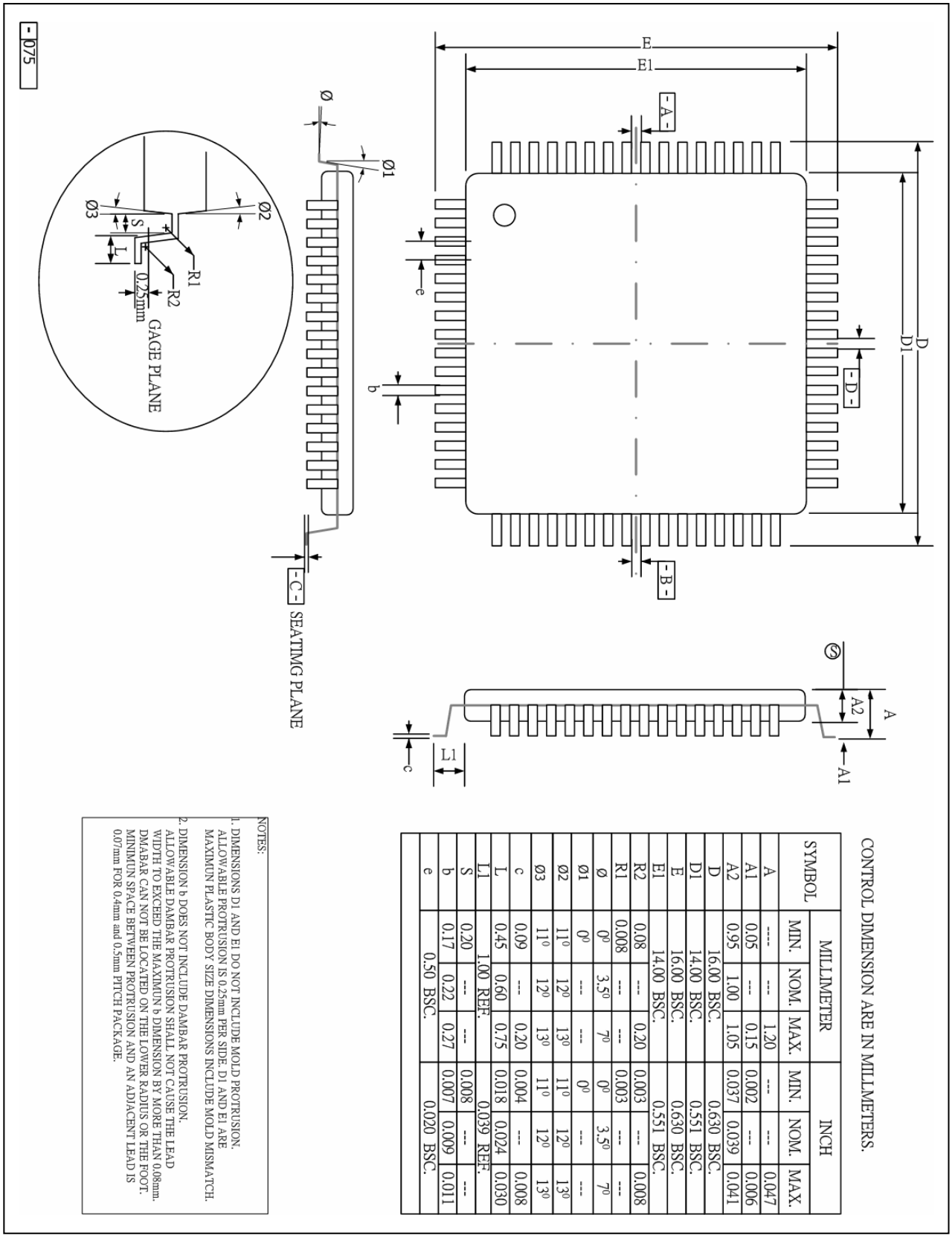


3.4. Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



J.Package

J1. TQFP-100 Package



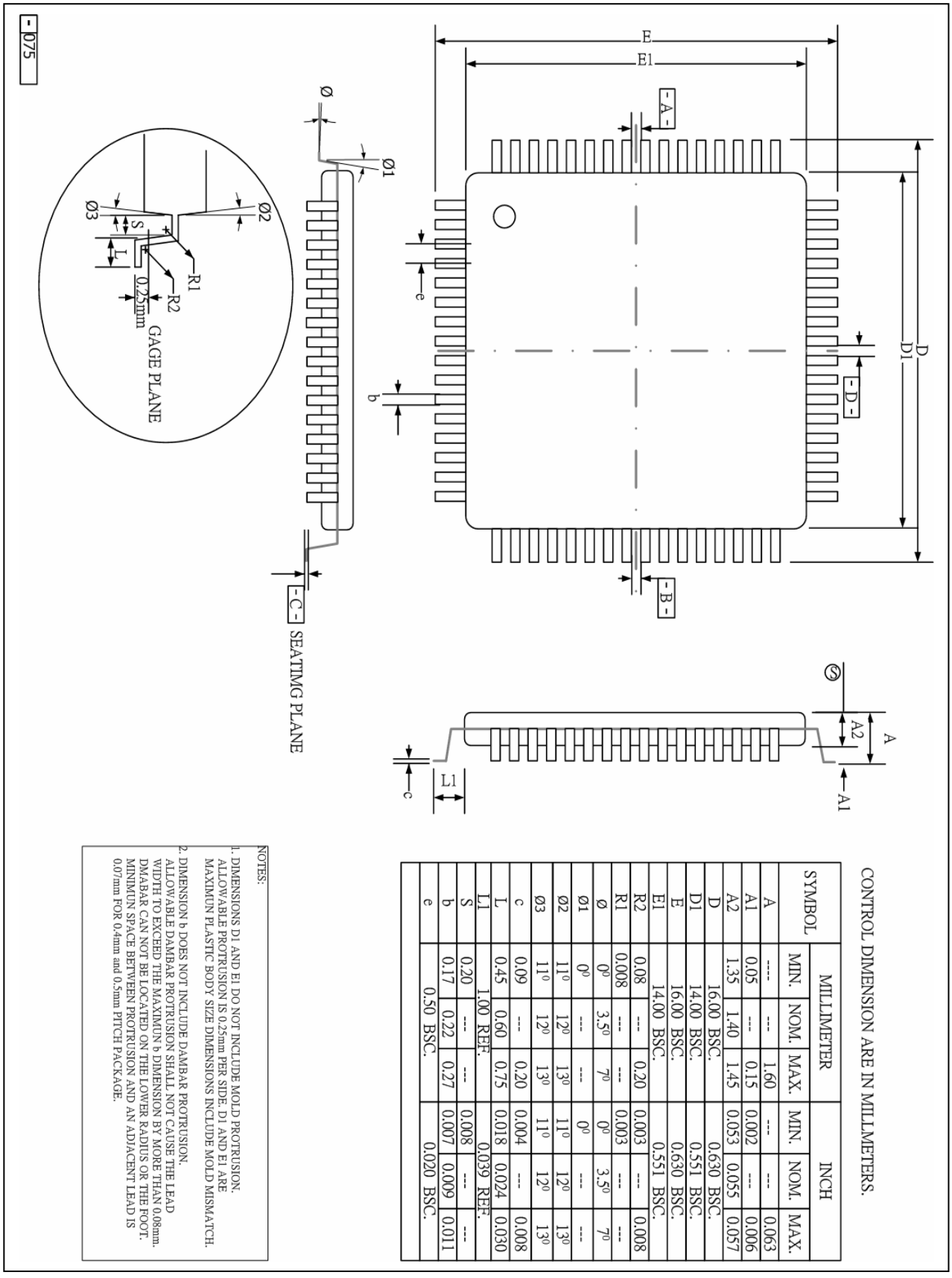
CONTROL DIMENSION ARE IN MILLMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	----	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D		16.00 BSC.			0.630 BSC.	
D1		14.00 BSC.			0.551 BSC.	
E		16.00 BSC.			0.630 BSC.	
E1		14.00 BSC.			0.551 BSC.	
R2	0.08	---	0.20	0.003	---	0.008
R1	0.008	---	---	0.003	---	---
Ø	0^0	3.5^0	7^0	0^0	3.5^0	7^0
Ø1	0^0	---	---	0^0	---	---
Ø2	11^0	12^0	13^0	11^0	12^0	13^0
Ø3	11^0	12^0	13^0	11^0	12^0	13^0
c	0.09	---	0.20	0.004	---	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF.			0.039 REF.	
S	0.20	---	---	0.008	---	---
b	0.17	0.22	0.27	0.007	0.009	0.011
e		0.50 BSC.			0.020 BSC.	

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDE MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMENSION BY MORE THAN 0.08mm. DMABAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUN SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGE.

J2. LQFP-100 Package



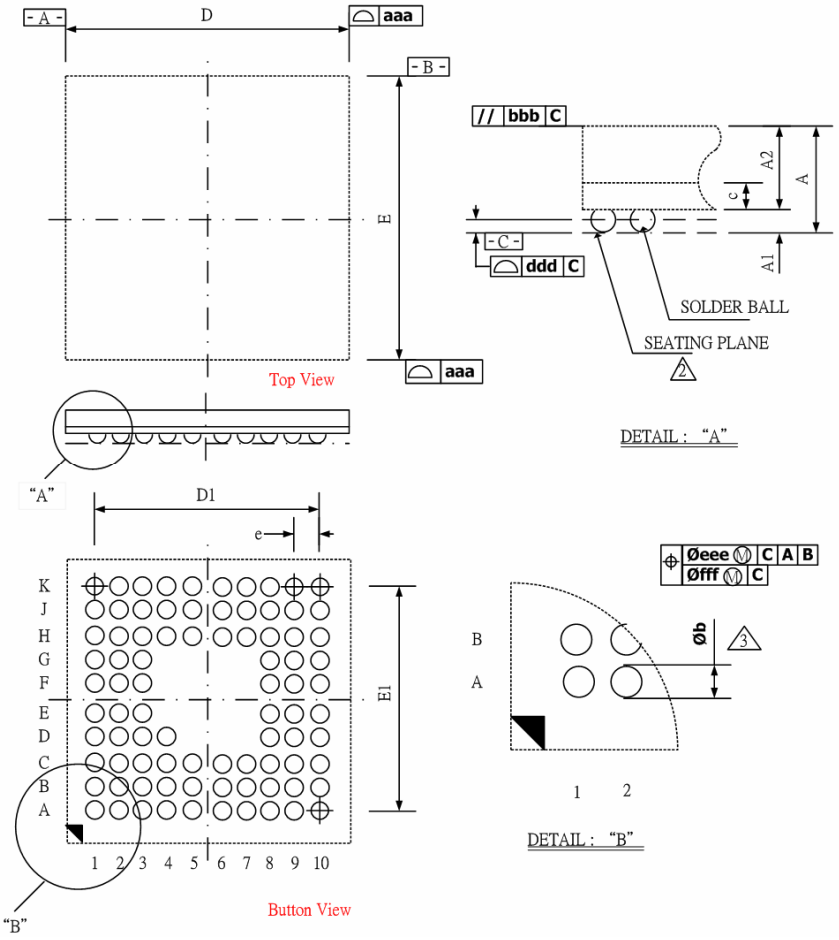
CONTROL DIMENSION ARE IN MILLMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	----	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	---	0.20	0.003	---	0.008
R1	0.008	---	---	0.003	---	---
Ø	0^0	3.5^0	7^0	0^0	3.5^0	7^0
Ø1	0^0	---	---	0^0	---	---
Ø2	11^0	12^0	13^0	11^0	12^0	13^0
Ø3	11^0	12^0	13^0	11^0	12^0	13^0
c	0.09	---	0.20	0.004	---	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
S	0.20	---	---	0.008	---	---
b	0.17	0.22	0.27	0.007	0.009	0.011
e	0.50 BSC.			0.020 BSC.		

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDE MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMENSION BY MORE THAN 0.08mm. DMABAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUN SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGE.

J3. BGA-85 Package



CONTROL DIMENSION ARE IN MILLMETERS.

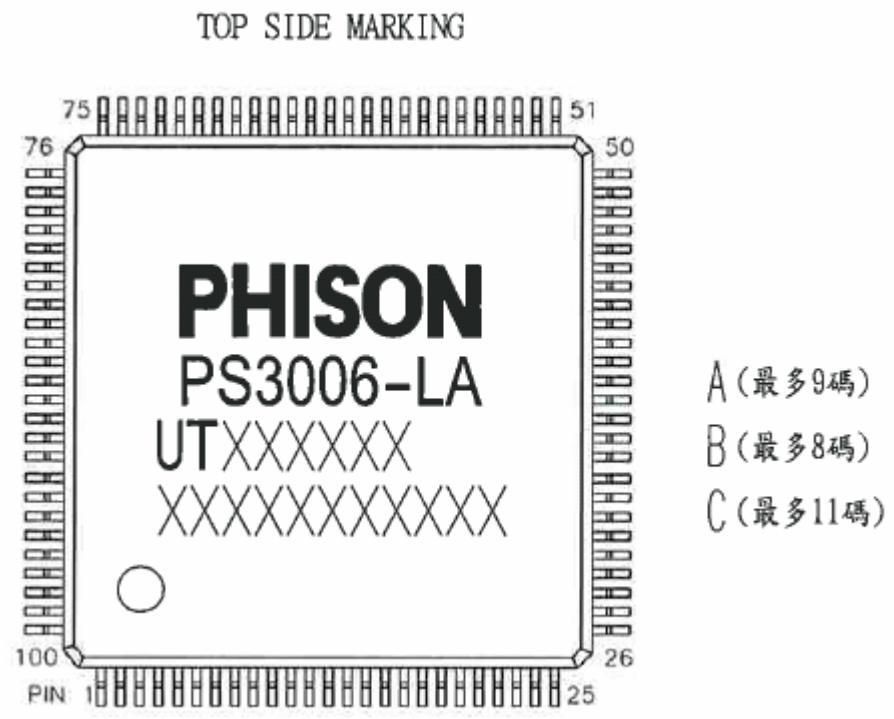
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	----	---	0.8	---	---	0.031
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.436	0.486	0.536	0.017	0.019	0.021
c	0.106	0.136	0.166	0.004	0.005	0.007
D	5.90	6.00	6.10	0.232	0.236	0.240
E	5.90	6.00	6.10	0.232	0.236	0.240
D1	---	4.50	---	---	0.177	---
E1	---	4.50	---	---	0.177	---
b	0.25	0.30	0.35	0.010	0.012	0.014
e	---	0.50	---	---	0.020	---
aaa	0.10			0.004		
bbb	0.10			0.004		
eee	0.15			0.006		
ddd	0.08			0.003		
fff	0.05			0.002		
MD/ME	10/10			10/10		

NOTES:

2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUN SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUN CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDGE MO-225
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS : bbb, ddd

K. PS3006 Marking

K.1 LQFP (Low Voltage Detect at 2.4V)



正　蓋

TOP SIDE MARKING (Laser)

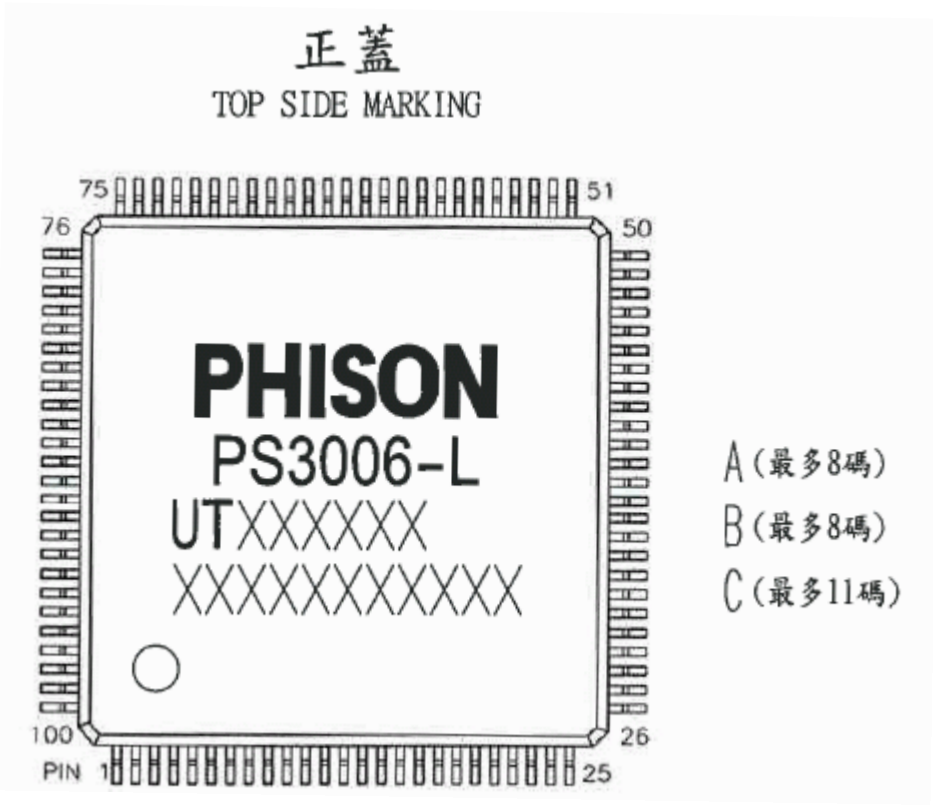
LOGO SIZE	: 8.0 x 1.95 mm
LOGO & LINE A SPACE	: 0.5 mm
LINE A & B & C LETTER HEIGHT	: 1.3 mm
LINE A LETTER WIDTH	: 0.9 mm
LINE B & C LETTER WIDTH	: 0.85 mm
LINE A & B & C SPACE	: 0.4 mm
LINE A & B & C LETTER STYLE	: Arial

LINE A PS3006-LA

LINE B UT□□□□□□ — Version; Date Code: yyww

LINE C □□□□□□□□□□□□ — Lot No.

K.2 LQFP (Low Voltage Detect at 2.8V)



正　蓋

TOP SIDE MARKING (Laser)

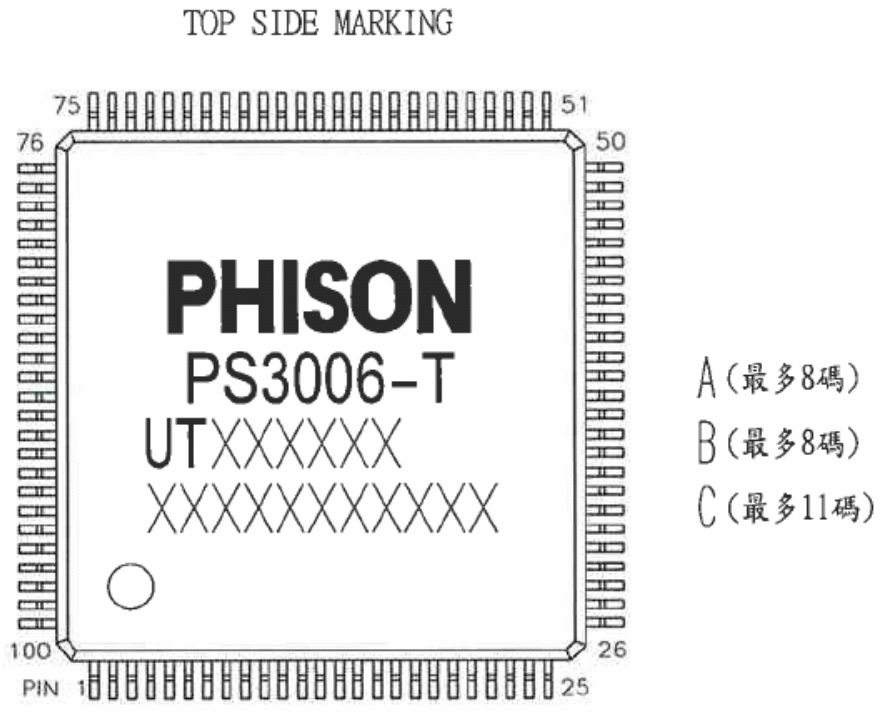
LOGO SIZE	: 8.0 x 1.95 mm
LOGO & LINE A SPACE	: 0.5 mm
LINE A & B & C LETTER HEIGHT	: 1.3 mm
LINE A LETTER WIDTH	: 0.9 mm
LINE B & C LETTER WIDTH	: 0.85 mm
LINE A & B & C SPACE	: 0.4 mm
LINE A & B & C LETTER STYLE	: Arial

LINE A PS3006-LA

LINE B UT□□□□□□ — Version; Date Code: yyww

LINE C □□□□□□□□□□□□ — Lot No.

K.3 TQFP



正　蓋

TOP SIDE MARKING (Laser)

LOGO SIZE	: 8.0 x 1.95 mm
LOGO & LINE A SPACE	: 0.5 mm
LINE A & B & C LETTER HEIGHT	: 1.3 mm
LINE A LETTER WIDTH	: 0.9 mm
LINE B & C LETTER WIDTH	: 0.85 mm
LINE A & B & C SPACE	: 0.4 mm
LINE A & B & C LETTER STYLE	: Arial

LINE A PS3006-LA

LINE B UT□□□□□□

Version

Date Code: yyww

LINE C □□□□□□□□□□□

Lot No.