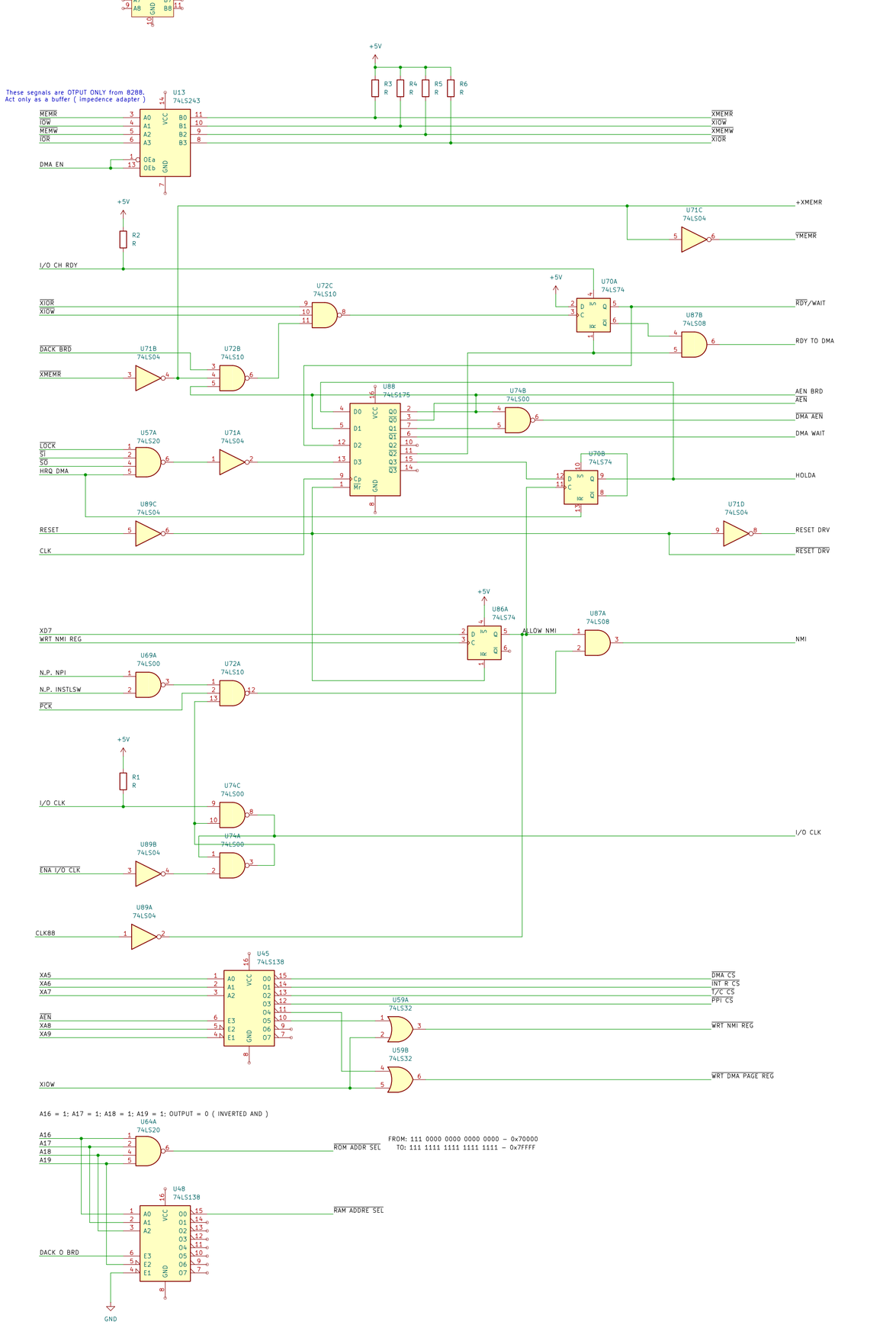
These segnals are OTPUT ONLY from 8288.
Act only as a buffer (impedence adapter)
U13
74LS243
MEMR
IOW
MEMW
IOR
DMA EN
XMEMR
XIOW
XMEMW
XIOR
+5V
R3
R4
R5
R6
R
R2
R1
U71C
74LS04
+XMEMR
YMEMR
I/O CH RDY
U72C
74LS10
U70A
74LS74
RDY/WAIT
U87B
74LS08
RDY TO DMA
DACK BRD
U71B
74LS04
U72B
74LS10
U88
74LS175
U74B
74LS00
AEN BRD
AEN
DMA AEN
DMA WAIT
U57A
74LS20
U71A
74LS04
LOCK
SI
SO
HRQ DMA
U70B
74LS74
HOLDA
U89C
74LS04
U71D
74LS04
RESET
CLK
RESET DRV
U86A
74LS74
U87A
74LS08
ALLOW NMI
NMI
XD7
WRT NMI REG
U69A
74LS00
U72A
74LS10
N.P. NPI
N.P. INSTLSW
PCK
U74C
74LS00
U74A
74LS00
I/O CLK
U89B
74LS04
ENA I/O CLK
U89A
74LS04
CLKBB
U45
74LS138
XA5
XA6
XA7
AEN
XA8
XA9
XIOW
DMA CS
INT R CS
T/C CS
PPI CS
U59A
74LS32
WRT NMI REG
U59B
74LS32
WRT DMA PAGE REG
A16 = 1; A17 = 1; A18 = 1; A19 = 1; OUTPUT = 0 (INVERTED AND)
U64A
74LS20
A16
A17
A18
A19
ROM ADDR SEL
FROM: 111 0000 0000 0000 0000 – 0x70000
TO: 111 1111 1111 1111 1111 – 0x7FFFF
U48
74LS138
RAM ADDRE SEL
DACK 0 BRD
GND
U59C
74LS32
U59D
74LS32
U59E
74LS32
U74D
74LS00
U74E
74LS00
U69B
74LS00
U69C
74LS00
U69D
74LS00
U69E
74LS00
U57B
74LS20
U57C
74LS20
U89E
74LS04
U89F
74LS04
U89D
74LS04
U89G
74LS04
U64B
74LS20
U64C
74LS20
U86B
74LS74
U86C
74LS74
U70C
74LS74
U87C
74LS08
U87D
74LS08
U87E
74LS08
U13
74LS243
U72D
74LS10
U71E
74LS04
U71F
74LS04
U71G
74LS04