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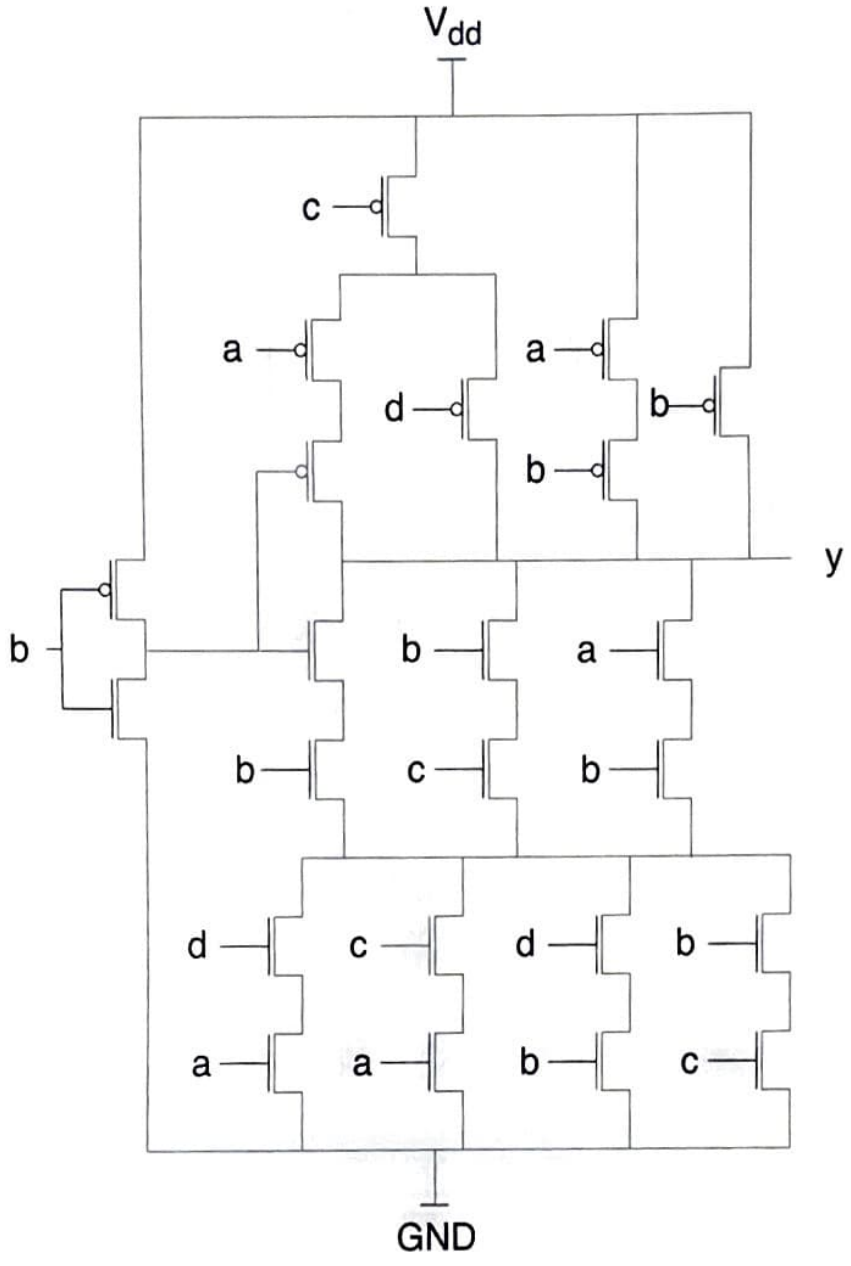
HW 6 **Due: December 3, 2025 at 11:59 PM in Santa Cruz.** Fall 2025

Instructions: Complete the problems below **in your own handwriting.** Box your answers where necessary. The grader will award 1 point for your name and the last four digits of your student ID, and 1 point for neatness.

Problem 1

Consider the CMOS circuit pictured below (6 points):



Fill out the truth table using the CMOS circuit above (4 points):

a	b	c	d	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

The Boolean function implemented by the network is (2 points):

$$f = \overline{abd + bc}$$

$$= (\bar{b} + \bar{c})(\bar{a} + \bar{b} + \bar{d})$$

Problem 2

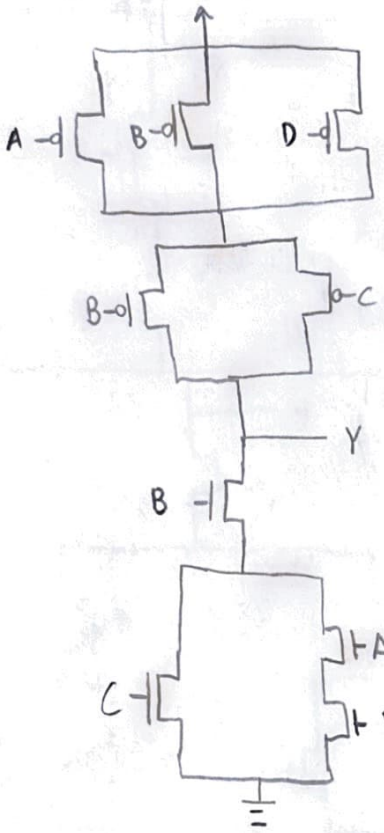
Design a simplified CMOS gate for the Boolean function you derived in Problem 1 (4 points).

pull down => $\overline{bc+abd}$ => $\overline{b(c+ad)}$

$= (\bar{b}+\bar{c})(\bar{a}+\bar{b}+\bar{d})$

PUN = $(\bar{b}+\bar{c})(\bar{a}+\bar{b}+\bar{d})$

NMOS = $b(c+ad)$



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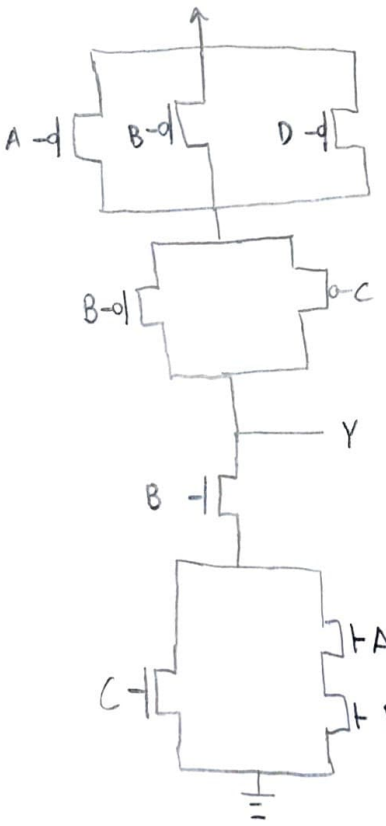

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Problem 3

Design a CMOS gate to implement the function (4 points):

$$f(a,b,c,d,e) = \overline{c} + a\overline{b} + \overline{d}(\overline{a}\,\overline{e} + \overline{b})$$

PDN: $f = 0$

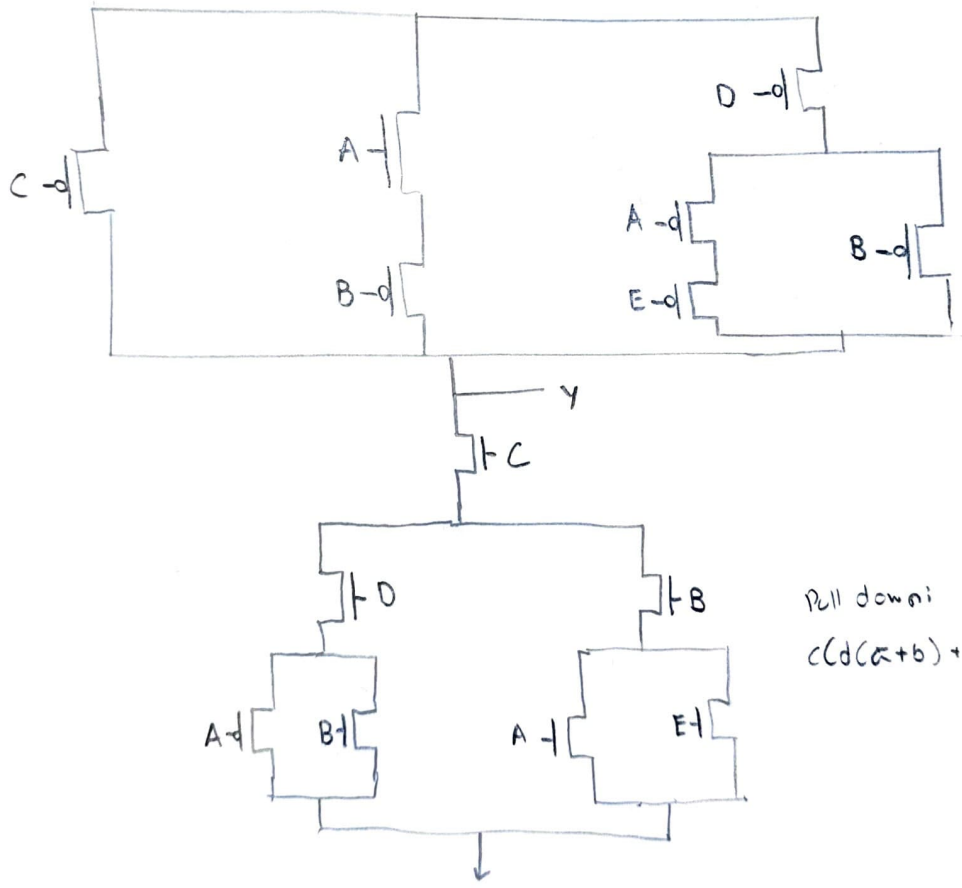
$= c\bar{a}\,\bar{d} + cb\bar{d} + cab + cbe$

$= c(\bar{d}(\bar{a}+b) + b(a+e))$

PUN: $f = 1$

$= \bar{c} + a\bar{b} + \bar{d}(\bar{a}\,\bar{e} + \bar{b})$

Pull up: $\bar{c} + a\bar{b} + \bar{d}(\bar{a}\,\bar{e} + \bar{b})$

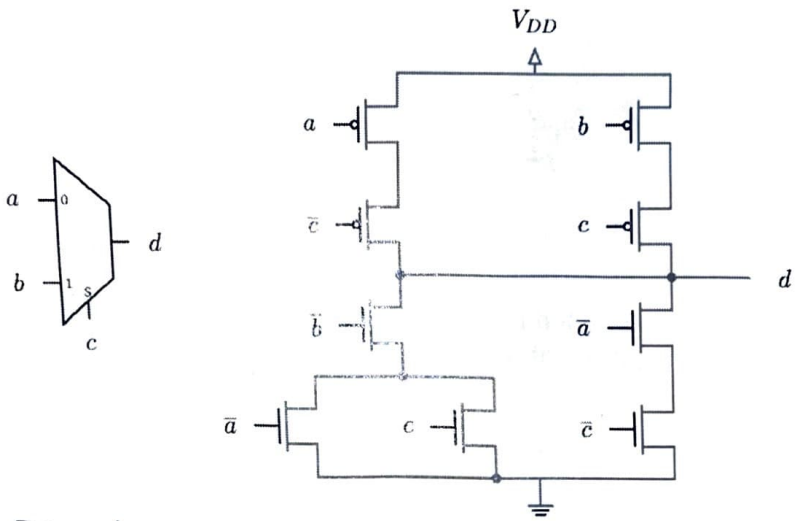


Pull down:

$c(\bar{d}(\bar{a}+b) + b(a+e))$

Problem 4

The CMOS circuit below implements a 2-input multiplexer with the pin connections as shown. Identify the errors in the CMOS circuit (2 points), and draw a valid implementation of a 2-input mux (4 points).



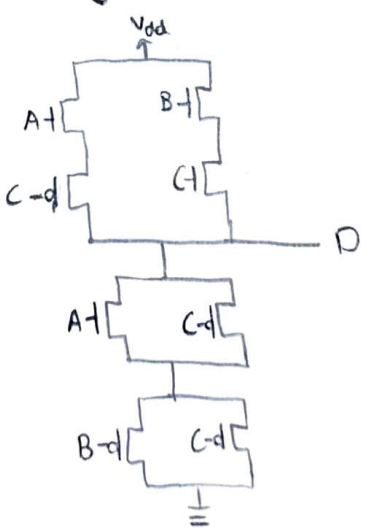
Errors:

Both PUN and PDN can turn on together, meaning not complement and not "opposites"

Branches using wrong sign/polarity

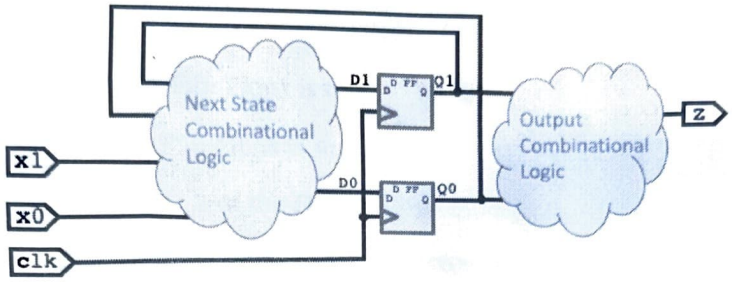
PUN: $(a\bar{c}) + (bc)$

PDN: $(\bar{a} + c)(\bar{b} + \bar{c})$



Problem 5

Below is a sequential circuit consisting of two D Flip-Flops and a combinational logic network which produces the D inputs to the Flip-Flops as well as the output z.



Assume the D Flip-Flops have a setup time of 6ns, a hold time of 4ns and a propagation time (low-to-high and high-to-low) of 2ns. In each of the following give a numeric answer and explain it.

(a) (2 points) If the maximum delay through the combinational logic network between the Flip-Flop outputs and Flip-Flop inputs is 16ns, what is the smallest clock period (time for a clock cycle) for the circuit to function correctly?

$T_{min} = 2+16+6 = 24$ ns

$T_{pmax} = 16$, $T_{c\to q} = 2$, $T_{su} = 6$

(b) (2 points) If the maximum delay of the combinational logic between the two Flip-Flop outputs and z is 10ns, how much time after the clock edge will z be guaranteed to be valid?

a after clock, go to output ebad

$= 2+10 = 12$ ns

(c) (2 points) If the minimum delay of the combination logic network between the Flip-Flop outputs and Flip-Flop outputs is 3ns, would the circuit meet timing (i.e. neither the setup or hold time is violated)? Justify your answer.

Yes, because via hold margin

$T_{min\ from\ c\to q} + T_{min\ earliest} > T_{hold}$

$2+3 > 4 \Rightarrow 5 > 4$ ✓

(d) (2 points) What is the smallest delay possible of the combinational logic network between the Flip-Flop outputs and Flip-Flop inputs that will allow the circuit to function correctly?

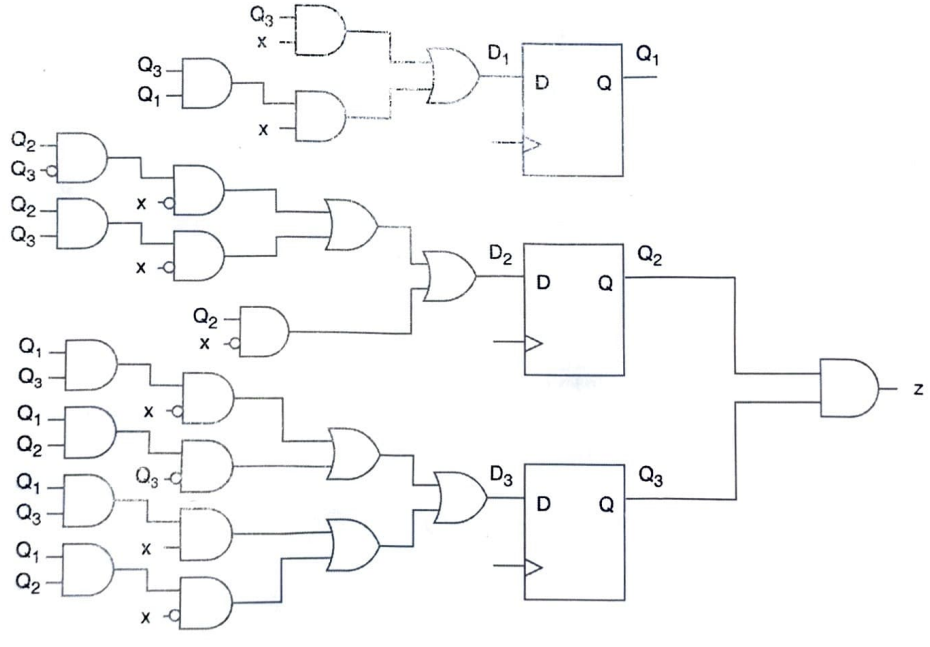
$T_{min\ from\ c\to q} + T_{min\ earliest} > T_{hold}$

$2 + T_{min} > 4 \rightarrow T_{min\ earliest} > 2$ ns

Problem 6

(22 points) Below is an unoptimized circuit that implements a state machine. Your goal is to check if the circuit meets the D Flip-Flop timing constraints specified and increase the maximum frequency of the circuit by optimizing the logic. Assume the following for the questions below:

- The setup time of the D Flip-Flops is 6ns.
- The hold time of the D Flip-Flops is 4ns.
- The propagation time (T_{cq}) of the D Flip-Flops is 2ns.
- AND gates have a delay of 5ns, OR gates have a delay of 3ns, and NOT gates (and bubbles!) have a delay of 2ns.
- Assume all inputs arrive at time = 0.



(a) (4 points) If the clock frequency of the circuit is 50MHz, would the circuit violate setup time? What about hold time? What is the maximum frequency of the initial circuit (in MHz)?

$t_{(total)\,max} = t_{NOT} + t_{OR} + t_{OR} + t_{AND} + t_{AND} = 18\,ns$

~~24~~ 16 $\quad 18 + 6 + 2 \leq 20$?

$26 \not\leq 20$

this violation

$t_{hold} = 4ns$, this would be fine

$f_{max} = \frac{1}{26} \approx 0.03846 \Rightarrow 38.46\ mHz$

(b) (8 points) Optimize the logic using K-maps, and write the logic equations for D_2, D_1, D_0, and z.
K-maps:

Q_1	Q_2	Q_3	x	D_1	D_2	D_3	z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	1	0	0	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	1	0
1	1	0	1	0	0	1	0
1	1	1	0	0	1	1	1
1	1	1	1	1	0	1	1

Logic equations:

See cont. graph paper page

GB cont'd.

D1)

$Q_3 X$ \ $Q_1 Q_2$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

D2)

$Q_3 X$ \ $Q_1 Q_2$	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	0	0
10	0	1	1	0

D3)

$Q_3 X$ \ $Q_1 Q_2$	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	1
10	0	0	1	1

z)

$Q_3 X$ \ $Q_1 Q_2$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	1	0
10	0	1	1	0

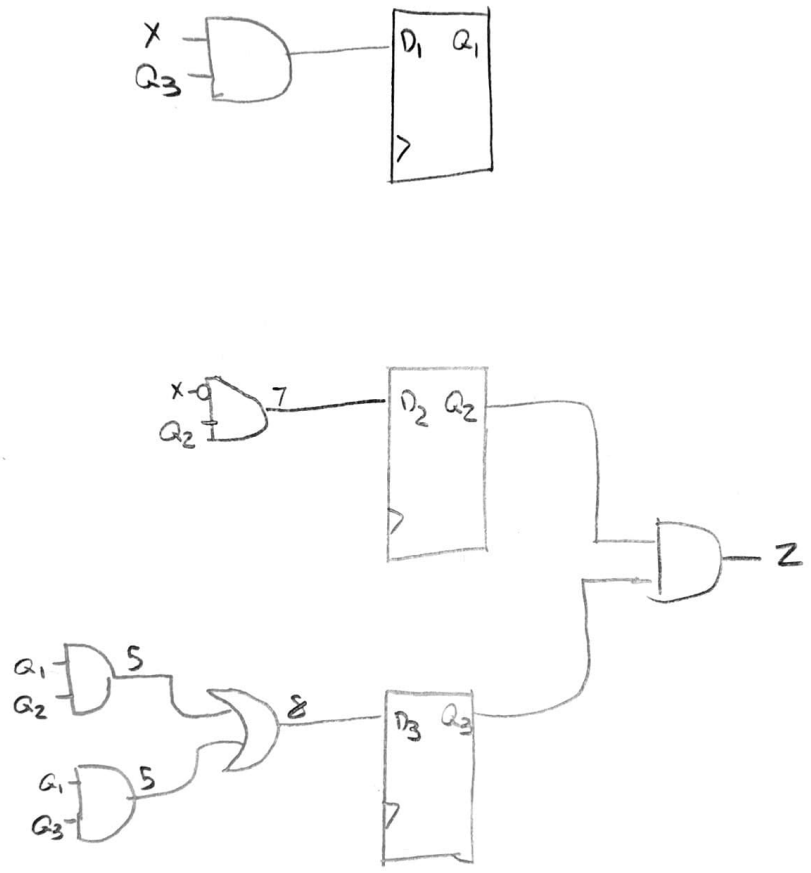
$D_1 = Q_3 X + Q_1 Q_3 X$

$D_2 = Q_2 \bar{Q}_3 \bar{X} + Q_2 Q_3 \bar{X} + Q_2 \bar{X}$

$D_3 = Q_1 Q_3 \bar{X} + Q_1 Q_2 \bar{Q}_3 + Q_1 Q_3 X + Q_1 Q_2 \bar{X}$

$z = Q_2 Q_3$

(c) (6 points) Draw the new optimized circuit (using ONLY 3 flip-flops and 2-input logic gates).



(d) (4 points) If the clock frequency of the circuit is 50MHz, would the circuit violate setup time? What about hold time? What is the maximum frequency of the optimized circuit (in MHz)?

5ns + 3ns = 8 ns ; freq = 50 MHz ; $\frac{1}{50}$ = 20 ns

20 ns ≥ 2 + 8 + 6 ns

20 ns ≥ 16 ns ⟶ $\frac{1}{16}$ => 62.5 MHz

✓ no violation

5 ns + 2 ns ≥ 4 ns

7 ns ≥ 4 ns

✓ no violation