

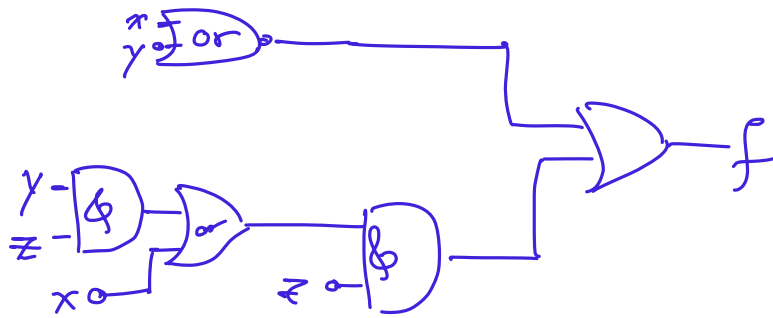
Reading: Sections 2.7-2.10 and 3.1-3.3.

**Instructions:** Complete the problems below in your own handwriting. Box your answers where necessary. The grader will award 1 point for your name and the last four digits of your student ID, and 1 point for neatness.

### Problem 1

For the following equation:  $f(x, y, z) = \overline{(x + \overline{y})} + \overline{z}(yz + \overline{x})$

- (a) (2 points) Draw the network of boolean logic gates that corresponds exactly to the following boolean expression. **Do not simplify the expression!** Make sure that you label all the input and output ports!



- (b) (1 point) Make a truth table for  $f(x, y, z)$ .

			$x$	$y$	$z$	
			0	0	0	1
			0	0	1	0
			0	1	0	1
			0	1	1	1
			1	0	0	0
			1	0	1	0
			1	1	0	0
			1	1	1	0

$$= \overline{(x + \overline{y})} + \overline{z}(yz + \overline{x})$$

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(c) (1 point): Write  $f(x, y, z)$  as the sum of minterms (e.g.  $m_0 + m_1 + \dots$ ).

$$\sum m(m_0 + m_2 + m_3)$$

(d) (1 point): Write  $f(x, y, z)$  in expanded canonical Sum-of-Products form, with all variables in each term (e.g.  $xyz + \bar{x}yz$ ).

$$\begin{array}{ccc} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \end{array} \quad f(x, y, z) = \bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + \bar{x}yz$$

(e) (1 point): Write  $f(x, y, z)$  as the product of maxterms (e.g.  $M_0 \cdot M_1 \cdot \dots$ ).

$$\prod M(M_1 \cdot M_4 \cdot M_5 \cdot M_6 \cdot M_7)$$

(f) (1 point): Write  $f(x, y, z)$  in expanded canonical Product-of-Sums form, with all variables in each term (e.g.  $(x + y + z)(\bar{x} + y + z)$ ).

$$\begin{array}{ccc} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{array} \quad f(x, y, z) = (x + \bar{y} + \bar{z}) \cdot (\bar{x} + \bar{y} + \bar{z}) \cdot (\bar{x} + \bar{y} + z) \cdot (\bar{x} + y + \bar{z}) \cdot (x + y + \bar{z})$$

(g) (2 points): Implement (draw)  $f(x, y, z)$  as a 2-level network of NAND boolean logic gates. You may assume that  $x$ ,  $y$ , and  $z$  are available as inputs to the network.

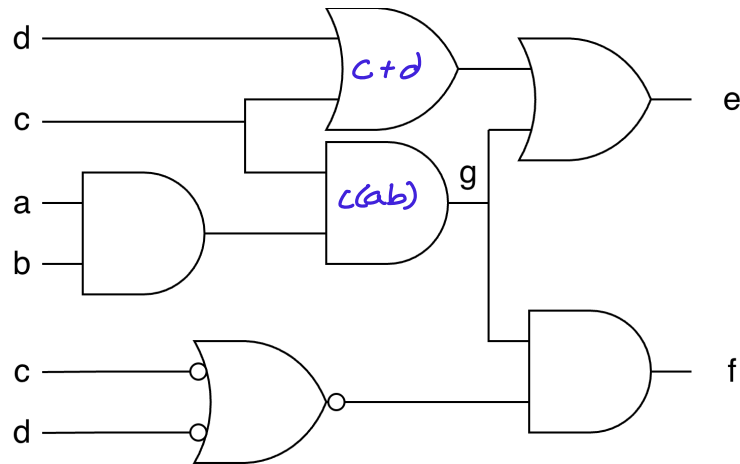
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- (h) (2 points): Implement (draw)  $f(x, y, z)$  as a 2-level network of NOR boolean logic gates. You may assume that  $x, y$ , and  $z$  are available as inputs to the network.

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### Problem 2

For the circuit shown below...



- (a) (1 point): Write the boolean expression for the variable  $g$  in terms of  $a, b, c$ , and  $d$ . (Do not simplify)

$$g(a, b, c, d) = c(ab)$$

- (b) (2 points): Write the boolean expression for the outputs  $e$  and  $f$  in terms of  $a$ ,  $b$ ,  $c$ , and  $d$ . (Do not simplify)

$$e = (c+d) + (c(ab)) \text{ or } (c+d) + g$$

$$f = (\overline{c+d})g \text{ or } (\overline{c+d})(c(ab))$$

- (c) (2 points): If they are not simplified already, simplify the boolean expressions for  $e$  and  $f$  using the laws of boolean algebra to minimize the number of literals in the expression. Show your work!

$$e = (c+d) + c(ab) \quad f = (\overline{c+d})(c(ab))$$

$$e = c + d + cab$$

absorption  $x + xy = x$

$$= c + cab = c$$

$$\text{So } \boxed{c+d} = e$$

$$\overline{c+d}(cab)$$

so

$$cdcab$$

$$c \cdot c = c$$

so

$$f = \underline{abcd}$$

### Problem 3

Suppose  $f(a, b, c) = \underbrace{(a + b + \bar{b} \cdot c)}_F (b + \bar{a} \cdot \bar{c})$ .

(a) (1 point): Make a truth table for  $f(a, b, c)$

$a$	$b$	$c$	$a+b$	$\bar{b}c$	$F+\bar{b}c$	$b+\bar{a}\bar{c}$	$AB$	$\bar{a}\bar{c}+b$
0	0	0	0	0	0	1	0	0
0	0	1	0	1	1	0	0	0
0	1	0	1	0	1	1	0	1
0	1	1	1	0	1	1	0	1
1	0	0	1	0	1	0	0	0
1	0	1	1	1	1	0	0	0
1	1	0	1	0	1	1	1	1
1	1	1	1	0	1	1	1	1

(b) (1 point): Write  $f(a, b, c)$  as the sum of minterms.

$$\sum m(m_2, m_3, m_6, m_7)$$

(c) (1 point): Write  $f(a, b, c)$  in expanded canonical Sum-of-Products form, with all variables in each term.

$$f(a, b, c) = \bar{a}\bar{b}\bar{c} + \bar{a}b\bar{c} + a\bar{b}\bar{c} + abc$$

(d) (1 point): Write  $f(a, b, c)$  as the product of maxterms.

$$\prod M(M_0, M_1, M_4, M_5)$$

(e) (1 point): Write  $f(a, b, c)$  in expanded canonical Product-of-Sums form, with all variables in each term.

$$f(a, b, c) = (\bar{a} + \bar{b} + \bar{c})(\bar{a} + b + c)(a + \bar{b} + \bar{c})(a + b + c)$$

- (f) (2 points): Implement (draw)  $f(a, b, c)$  as a 2-level network of NAND boolean logic gates using the functions you derived above, without simplifying. You may assume that  $a$ ,  $b$ , and  $c$  are available as inputs to the network.

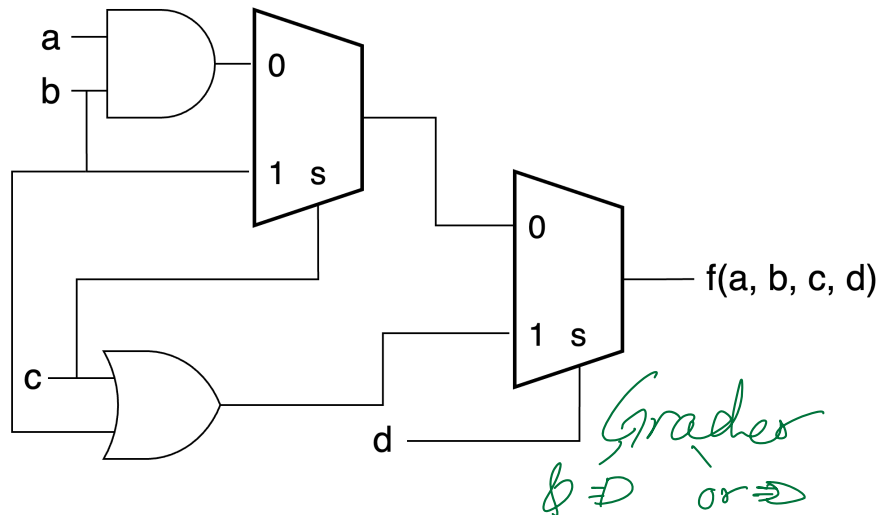
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- (g) (2 points): Implement (draw)  $f(a, b, c)$  as a 2-level network of NOR boolean logic gates using the functions you derived above, without simplifying. You may assume that  $a$ ,  $b$ , and  $c$  are available as inputs to the network.

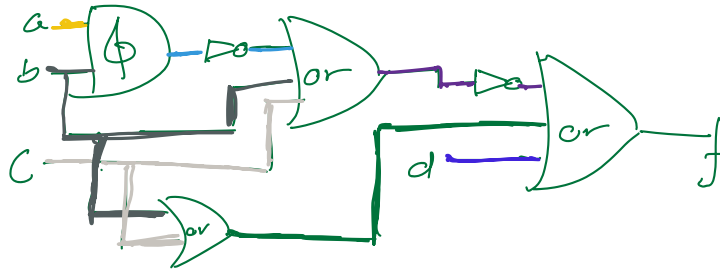
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### Problem 4

For the circuit shown below:



- (a) (4 points) Draw the equivalent boolean network that computes  $f(a, b, c, d)$  using only AND, NAND, OR, NOR and INV boolean gates.



$$\overline{(\overline{a}b + c + b)} + d + (c + b)$$

- (b) (4 points) Write the boolean function that computes  $f(a, b, c, d)$ . **Do not simplify.**

$$f(a, b, c, d) = \overline{(\overline{a}b + c + b)} + d + (c + b)$$

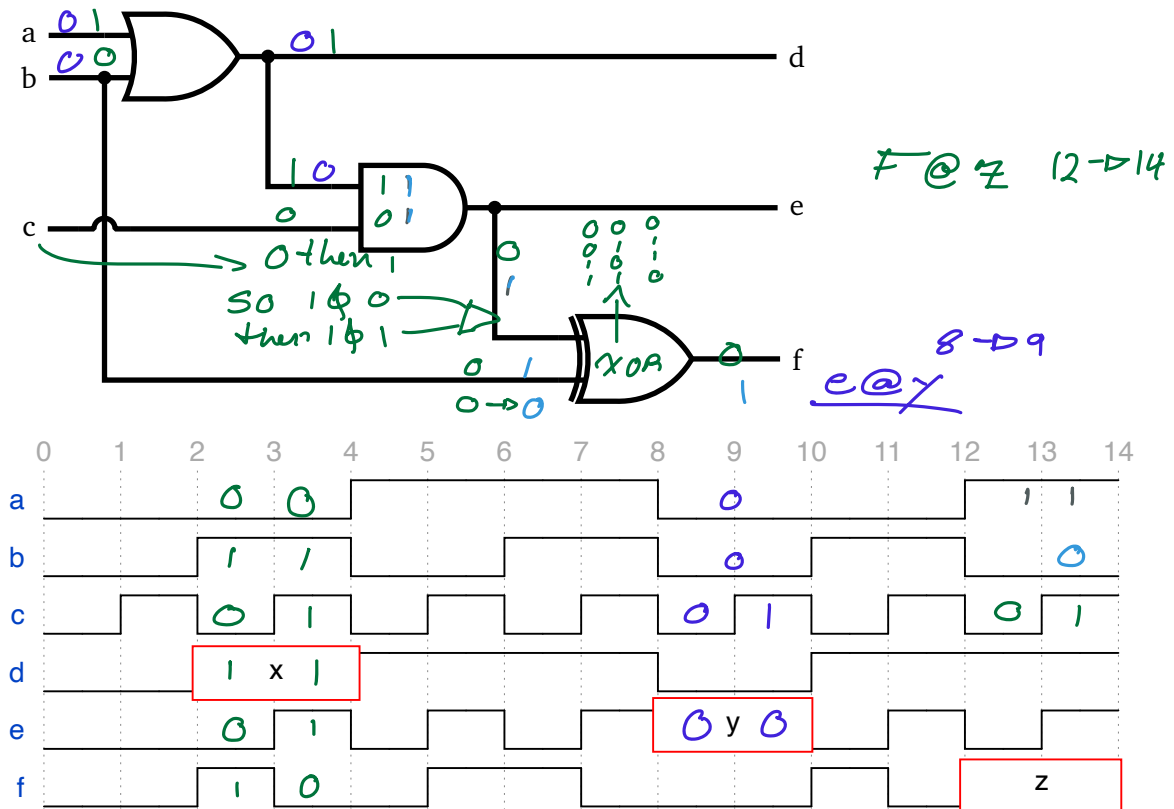
- (c) (4 points) Obtain a *minimal* expression for the function  $f(a, b, c, d)$  using boolean algebraic laws and identities. For full points, show your work by labelling each step with the identity or law that was applied, and ensure your expression has the minimal number of literals possible.

Function	Law/Identity Applied
$\overline{(\overline{a}b + c + b)} + d + (c + b)$ <p><i>for 28er</i></p>	
$\overline{\overline{a}b} \overline{c + b}$	De Morgan's
$a\overline{b} \overline{c + b}$	Involution
$a\overline{c} (b\overline{b}) = 0$	Complementing
$\text{So } 0 + d + c + b$	
$d + c + b$	
$f(a, b, c, d) = b + c + d$	



### Problem 5

The waveform below is incomplete in certain areas. Complete the waveform by indicating which values would be correct given the diagram below. Assume zero gate and wire delay.



(1 point) What is the value of **d** at **x**?

- ☐ 0
- ☒ 1
- ☐ 0 then 1
- ☐ 1 then 0

(1 point) What is the value of **e** at **y**?

- ☒ 0
- ☐ 1
- ☐ 0 then 1
- ☐ 1 then 0

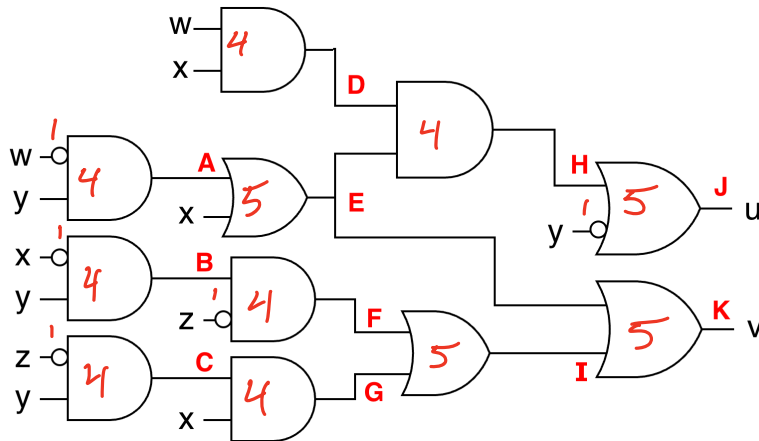
(1 point) What is the value of **f** at **z**?

- ☐ 0
- ☐ 1
- ☒ 0 then 1
- ☐ 1 then 0

# Problem 6

Zero wire delay

Consider the circuit shown below:



Gate Delays	
INV/bubbles	1
NAND	2
NOR	3
AND	4
OR	5

(a) (3 points) What is the function implemented at each of the red-labeled gate outputs?

$$f(A) = \bar{w}y \quad f(B) = \bar{x}y$$

$$f(C) = \bar{z}y \quad f(D) = wx$$

$$f(E) = \bar{w}y + x \quad f(F) = \bar{x}y\bar{z}$$

$$f(G) = \bar{z}yx \quad f(H) = wx(\bar{w}y + x) + \bar{y}$$

$$f(I) = \bar{x}y\bar{z} + xy\bar{z} \quad f(J) = u = (wx(\bar{w}y + x) + \bar{y}) + \bar{y}$$

$$f(K) = v = (\bar{w}y + x) + \bar{x}y\bar{z} + xy\bar{z} \quad E + I$$

(b) (3 points) For each of the labeled gate outputs, determine when the output of that gate will be settled given that the inputs  $w, x, y, z$  are stable at time 0. Gate delays are shown next to the circuit. Assume zero wire delay.

$$d_A = 5 \quad d_B = 5$$

$$d_C = 5 \quad d_D = 4$$

$$d_E = 10 \quad d_F = 9 + 1 = 10$$

$$d_G = 9 \quad d_H = \begin{matrix} D=4 \\ E=10 \end{matrix} H=14$$

$$d_I = \begin{matrix} E=10 \\ F=10 \\ G=9 \end{matrix} 14 \quad d_J = d_u = 19$$

$$d_K = d_v = 19$$

can you have a ckt out of tempo?

- (c) (7 points) Minimize the functions  $u$  and  $v$  by filling out the truth table and using K-maps to find the minimal sum-of-products expressions. Circle all prime implicants in your K-map.

$wx + y$

w	x	y	z	u	v
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

u:

$y \bar{z}$

	00	01	11	10
00	0	0	1	1
01	1	1	1	1
11	1	1	1	1
10	0	0	0	1

v:

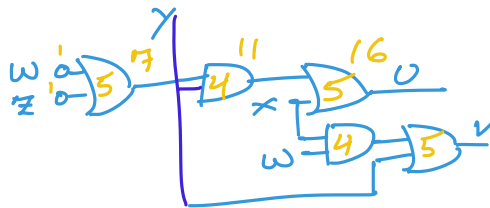
$y \bar{z}$

	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	1	1	1	1
10	1	1	0	0

$u = \underline{u = x + y(\bar{w} + \bar{z})}$

$v = \underline{v = wx + y}$

- (d) (3 points) Given the minimized expressions for  $u$  and  $v$ , implement the optimized circuit using only 2-input logic gates (AND, OR, NAND, NOR, and INV). You may not use 3-input gates or larger.



- (e) (2 points) For your new optimized circuit, determine when the outputs  $u$  and  $v$  will be settled given that the inputs  $w, x, y, z$  are stable at time 0.

$d_u = \underline{16}$

$d_v = \underline{9}$