POWER ELECTRONIC CIRCUITS M

Written report

Three-phase multilevel inverter:

Neutral Point clamped topology (NPC)

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Summary

INTRODUCTION

The devices which can convert electrical energy of DC form into AC form is known as power inverters. A power inverter is a power electronic device or circuit that changes direct current/voltage (DC) into alternating current/voltage (AC). The inverter consists of switching devices, thus the way in which the switching takes place in the inverter gives the required output. They come in all sizes and shapes, from a high-power rating to a very low-power rating, from low power functions like powering a car radio to that of backing up a building in case of power outage. Inverters can come in many different varieties, differing in power, efficiency, price and purpose. Recently, the inverters are also playing important roles in renewable energy applications as they are used to link a photovoltaic or wind system to a power grid. Today inverters use high power switching transistors called IGBT's and/or MOSFETS. The main inverters (Fig.1) seen during the course are summarized below:

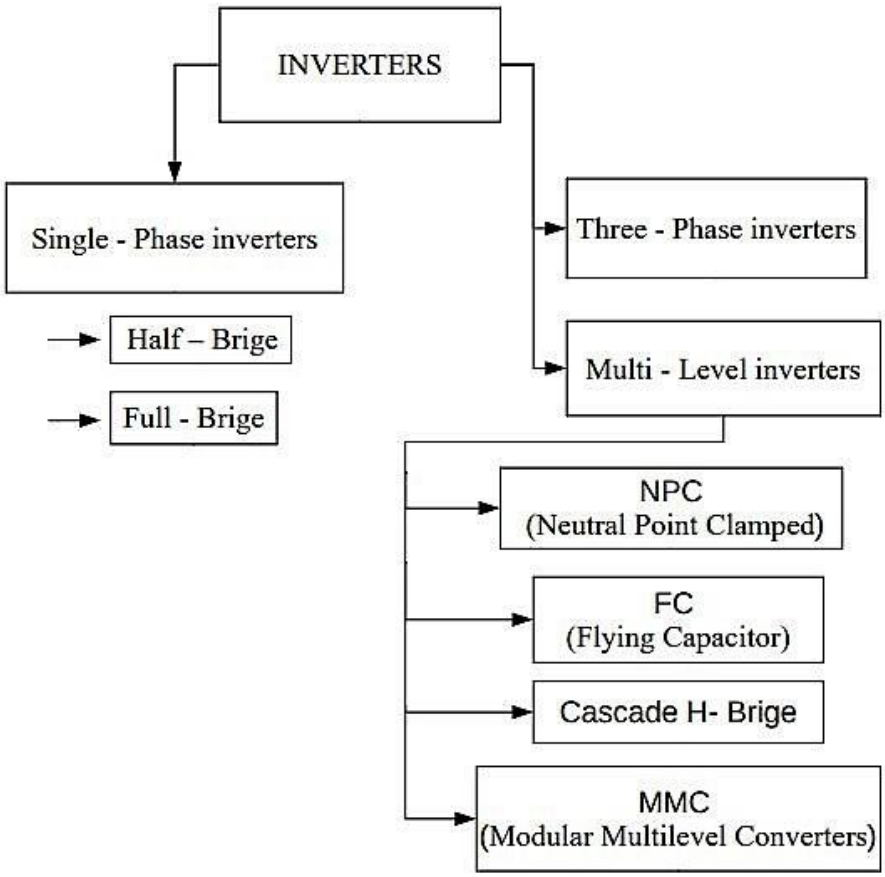


Fig. 1 *Type of inverter.*

In this report we will focus on Multilevel Three-Phase inverter. Multilevel converters present great advantages compared with conventional two-level converters (inverter in which the pole voltages can assume only two values Fig.2). These advantages are fundamentally focused on improvements in the output signal quality and a nominal power increase in the converter.

In the case of high power / high voltage applications the two-level inverters have some limitations to operate at high frequency mainly due to switching losses. The main drawback of the two-level

converter is the high harmonic content of the output voltage, which makes the use of bulky output filter necessary. Moreover, the semiconductor switching devices should be used in such a manner as problematic series / parallel combinations to obtain capability of handling high power. In a high-power conversion processing system, it is nowadays preferred to use the multilevel approach.
The advantages of the multilevel inverter compared to the traditional two-level inverter are:

- They can generate the output voltage with reduced distortion (good power quality).
- dv/dt of the output voltage is lower (reduced stress on the load insulation).
- They have lower voltage stress on switching devices for the same maximum output voltage:

$$\frac{V_{DC}}{n-1}$$

- They generate lower harmonics for the same switching frequency(fig).

A disadvantage of a multilevel inverter is the number of components.

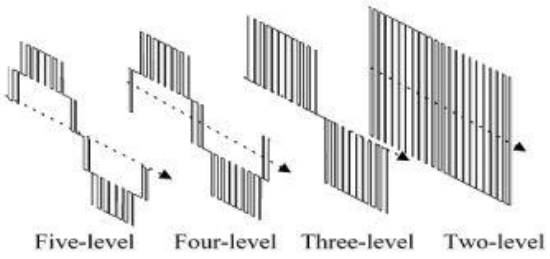


Fig. 2 Number of levels pole voltages.

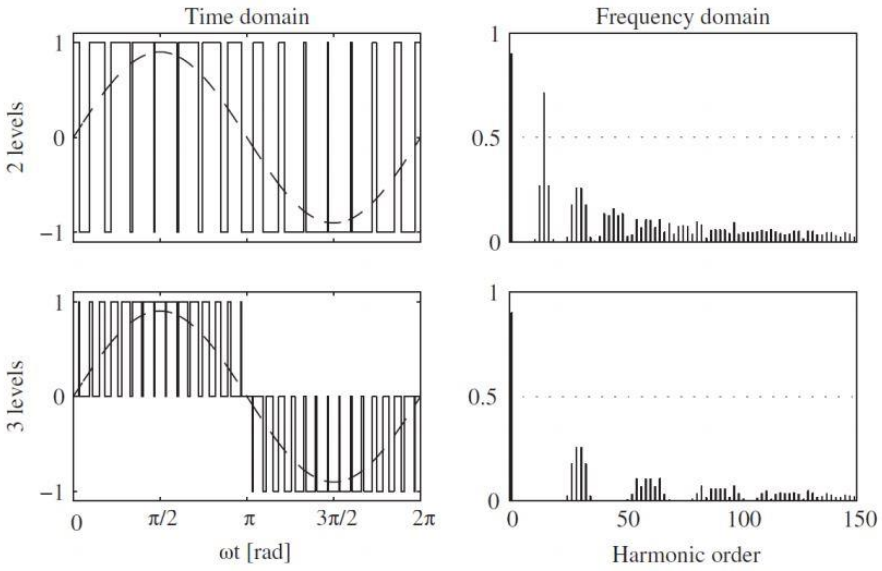


Fig. 3 Harmonic content of the two and three level inverters.

THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER

NPC topology (Fig.4) is obtained by doubling the number of switches in comparison to the two-level inverter and adding the same number of diodes to each additional switch. We usually have DC link, two capacitors in order to get the middle point on the DC side. We have three legs; each leg consists in four switches and two neutral point clamp diodes. The middle point of top two switches is connected to the middle point of the dc link through diode D1 and the middle point of bottom two switches is connected to the middle point of the dc link through diode D2. The middle point of each leg is connected to the load. In this configuration the ground is in the middle point of DC link. The advantages of this configuration are:

- Voltages across the switches are only half of the dc-link voltage.
- The first group of voltage harmonics is centered on twice the switching frequency.

However, practical experience with this topology revealed several technical difficulties that complicate its application for very high-power converter. These are as follows:

- This topology requires clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress.
- For topologies with more than three levels the clamping diodes are subject to increased voltage stress.

The pole voltage is measured between middle point of dc link and the middle point of the leg.

V_{ao}, V_{bo}, V_{co} are the pole voltages.

V_{12}, V_{23}, V_{31} are the line-to-line voltages.

e_1, e_2, e_3 are the phase-voltages.

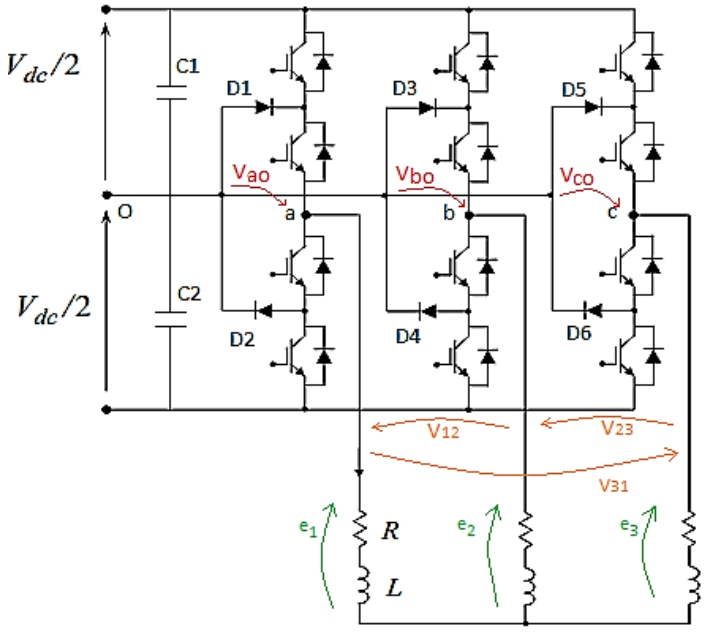


Fig. 4 NPC Three-levels inverter configuration.

Working Principle

Considering only the first leg:

- If the two top switches are turn on, the pole voltages are equal to $\frac{V_{DC}}{2}$. If the current is positive flows through the switches if it is negative flows through the antiparallel diodes (Fig.5).

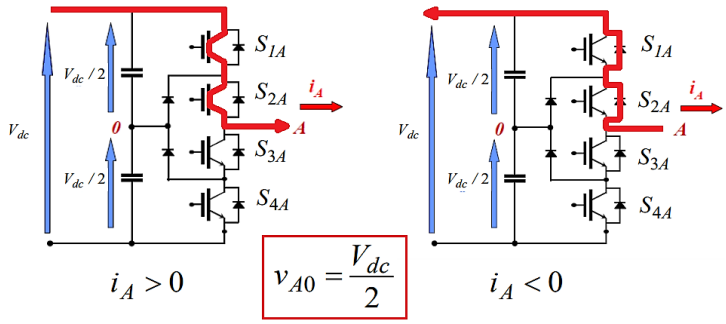


Fig. 5 Two upper switches on.

- If the two middle switches are turn on the pole voltages are equal to 0 (Fig.6).

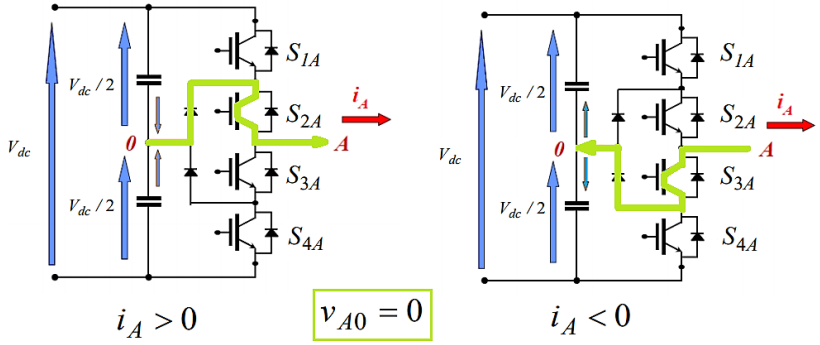


Fig. 6 Two middle switches on.

- If the two bottom switches are turn on (Fig.7) the pole voltages are equal to $-\frac{V_{DC}}{2}$.

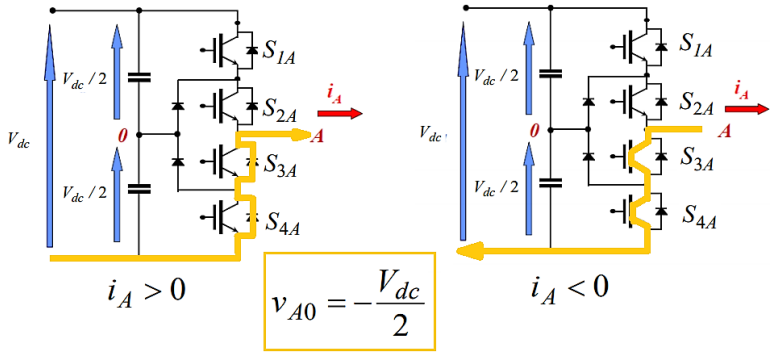


Fig. 7 Two bottom switches on.

We have three possible values for each the pole voltage, for this reason this type of converter is called three level inverters.

IMPLEMENTING CIRCUIT

The LTspice software was used to implement the NPC type three levels inverter. The three-phase case was considered. The circuit is shown in the Fig.8.

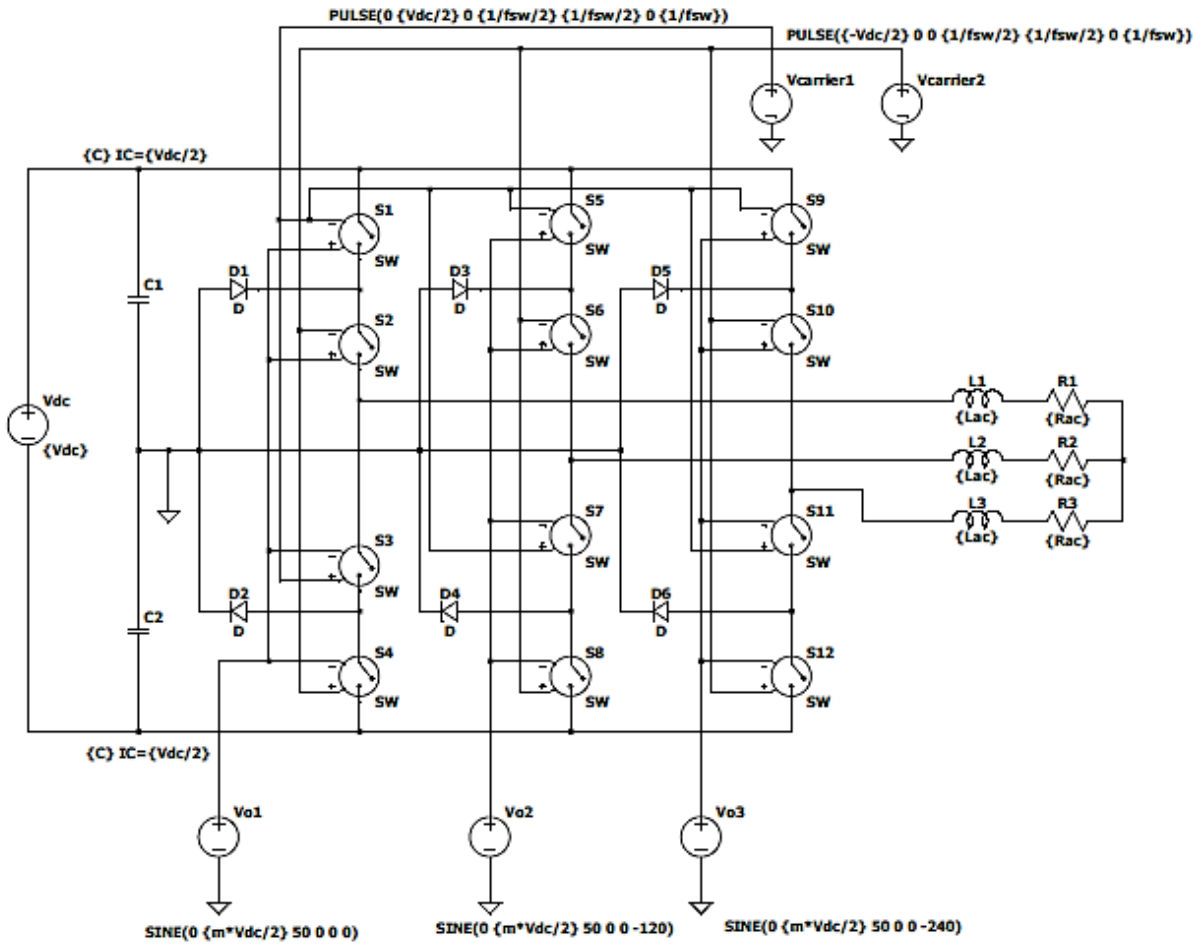


Fig. 8 *Implementing circuit of NPC type three levels.*

In the circuit we have twelve switches, the ideal switches have been chosen. The definition of the static characteristic of these switches was carried out through the "SPISE directive" command (Fig.9), where the following parameters were used $R_{on} = 1m\Omega$, $R_{off} = 1M\Omega$ and $V_t = 0$. ($R_{off} \gg R_{on}$ in order not to have current circulation inside the switches during the off state)

```
.model SW SW(Ron=1m Roff=1Meg Vt=0)
```

Fig. 9 *Static characteristic of the switches.*

We have a DC voltage generator with $V_{dc} = 100$v, six clamped diode and two capacitors. The two capacities have been chosen with the same initial condition equal to $\frac{V_{dc}}{2}$, in such a way as to have at the beginning of the simulation $\frac{V_{dc}}{2}$ on the two capacitors.

The simulation parameters were entered using the "Space analysis" command (Fig.10), in a first analysis the following values were chosen: Stop time = 100ms, Time to start saving data = 0s and Maximum Timestep =1µs. The last parameter is important because it allows to obtain a more accurate result.

.tran 0 100m 0 1u uic

Fig. 10 *Simulation parameters.*

Three voltage sources were used to implement the modulating signals (Fig.11):

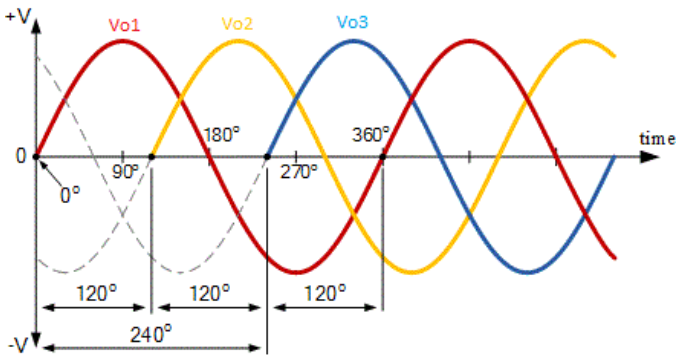


Fig. 11 *Modulating signals.*

The SINE function was used as shown in Fig.12, where m is the amplitude modulation index:

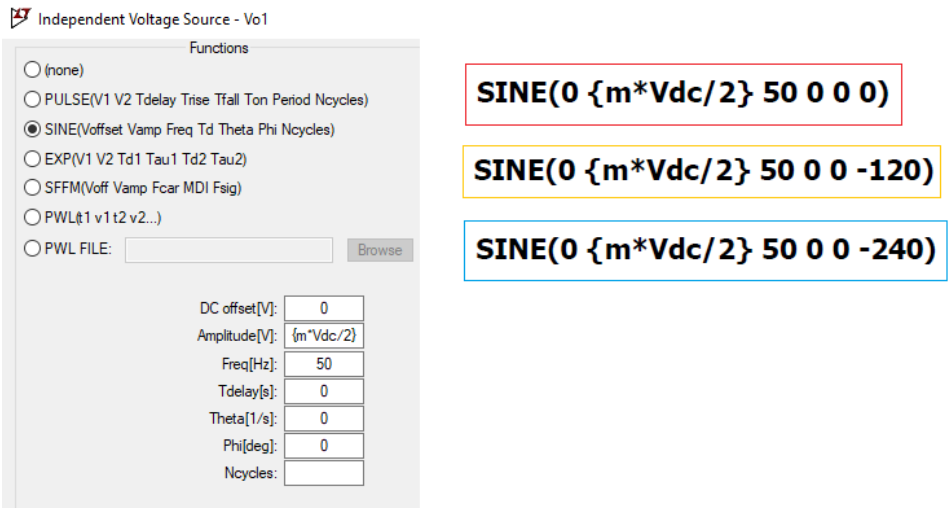


Fig. 12 *Modulating signals implementing circuit.*

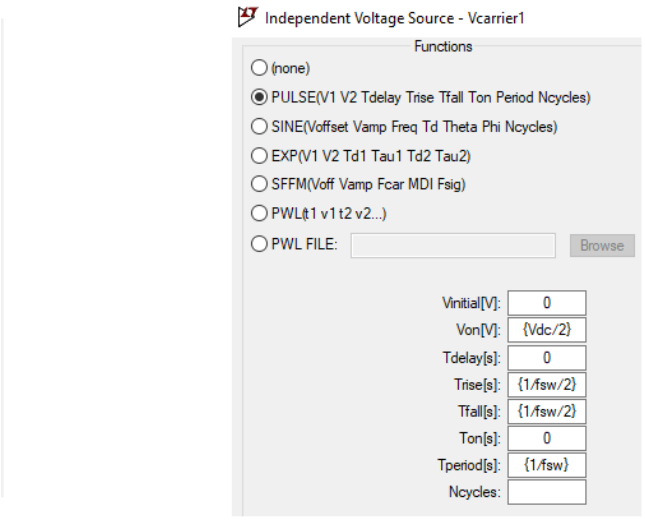
In addition, two other voltage sources were used for the implementation of the carriers: $V_{Carrier1}, V_{Carrier2}$. In this case the PULSE function was used as shown in Fig.13. In both carriers signal the frequency equal to 2kHz ($f_{SW} = 2kH$) was chosen, this means that the period of two carrier is $\frac{1}{2000}$.

$T_{raise} = \frac{1}{2000}/2$ and $T_{fall} = \frac{1}{2000}/2$ were taken to create the triangular waveform.

The two carrier signals only have different levels, there is no phase shift.

$$V_{Carrier1}: 0 \rightarrow \frac{V_{dc}}{2} \; ; \; V_{Carrier2}: -\frac{V_{dc}}{2} \rightarrow 0$$

The signals generated can be seen in Fig.14.



PULSE(0 {Vdc/2} 0 {1/fsw/2} {1/fsw/2} 0 {1/fsw}) First carrier

PULSE({-Vdc/2} 0 0 {1/fsw/2} {1/fsw/2} 0 {1/fsw}) Second carrier

Fig. 13 *How to implement carrier signals.*

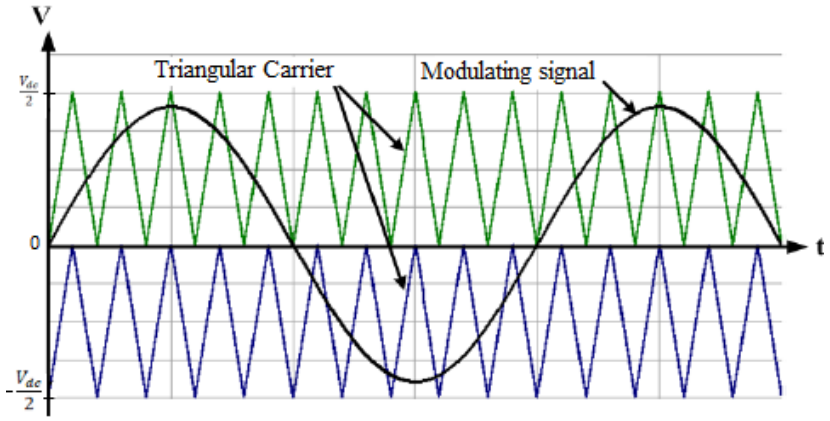


Fig. 14 *Carrier signals and generic modulating signals.*

The different values of the components (Fig.15) of the implementation circuit have been attributed through “SPISE directive” command.

.param Vdc=100, fsw=2k, m=0.95, c=5m, Lac=10mH, Rac=5

Fig. 15 *Definition of system parameters.*

MODULATION TECNIQUE

As seen in the previous paragraph, two carrier signals and a modulating signal were used for each leg. The modulation technique used is based on the use of carriers (CB-PWM, Carrier Based PWM). It is possible to extend the PWM modulation to the multilevel case. This technique involves the adoption of n-1 carriers, where n is the number of levels of the converter. It is based on the concept of intersection of one or more modulating signals with the n-1 carriers.
The interactions between the carriers and the modulators are fundamental to generate the control signals that drive pairs of complementary switches in the inverter.
The reciprocal position of the carriers determines various modulation techniques: PD (Phase Disposition), POD (Phase Opposite Disposition) APOD (Alternative Phase Disposition).
It was decided to use the ***LS-Phase Disposition (PD) modulation*** shown in Fig.16. There are two carrier signals that are shifted in level but in phase among then. For this type of inverter, it is the most used modulation because it produces a lower harmonic distortion of the output voltages. It is a sinusoidal modulation; this means that the maximum value of m is one if m > 1 there is over-modulation.

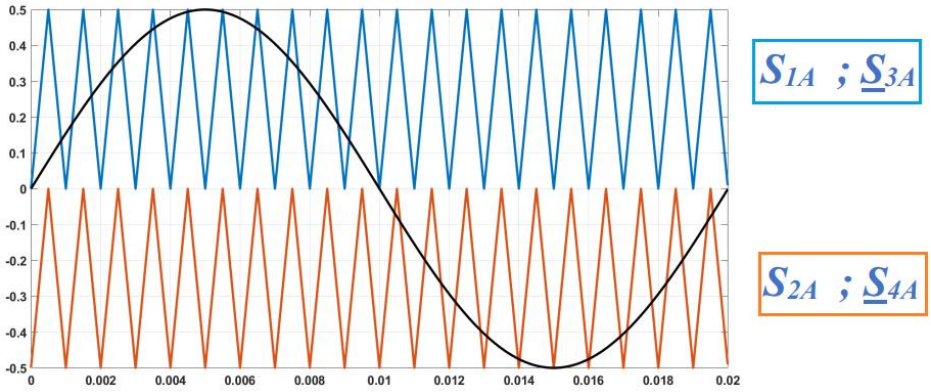


Fig. 16 *LS-Phase Disposition (PD) modulation.*

Considering the first leg, the first carrier drives the switch 1 and switch 3 and second carrier drives switch 2 and switches 4:

- If the modulating signal is greater than the first carrier:

$$S_{1A}\ on \qquad S_{3A}\ off$$

- If the modulating signal is lower than the first carrier:

$$S_{1A}\ off \qquad S_{3A}\ on$$

- If the modulating signal is greater than the first carrier:

$$S_{2A}\ on \qquad S_{4A}\ off$$

- If the modulating signal is lower than the first carrier:

$$S_{2A}\ off \qquad S_{4A}\ on$$

In the first half-cycle, it always occurs: $S_{2A}\ on$ $S_{4A}\ off$

- If the modulating signal is greater than the first carrier: $S_{1A}\ on$ $S_{3A}\ off$ this means that:

$$V_{ao} = \frac{V_{dc}}{2}$$

- If the modulating signal is lower than the first carrier: $S_{1A}\ off$ $S_{3A}\ on$ this means that:

$$V_{ao} = 0$$

In the second half-cycle, it always occurs: $S_{1A}\ off$ $S_{3A}\ on$

- If the modulating signal is greater than the second carrier: $S_{2A}\ on$ $S_{4A}\ off$ this means that:

$$V_{ao} = 0$$

- If the modulating signal is lower than the second carrier: $S_{2A}\ off$ $S_{4A}\ on$ this means that:

$$V_{ao} = -\frac{V_{dc}}{2}$$

Graphically, the result shown in Fig.17.

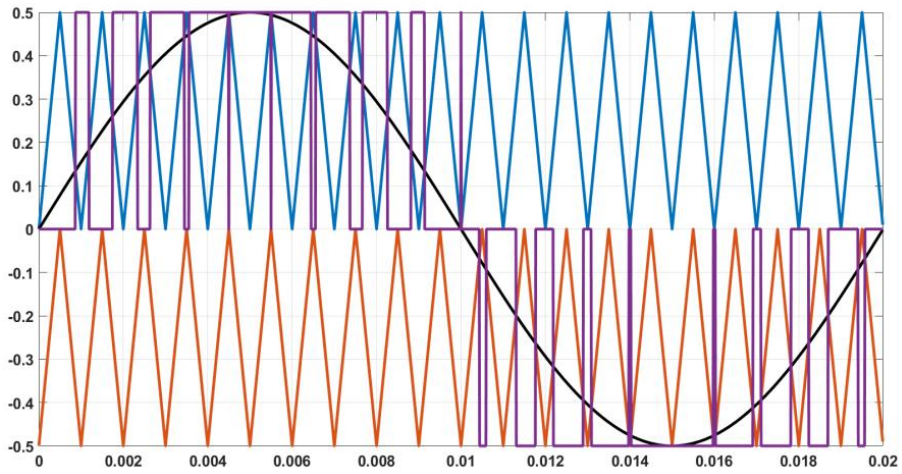


Fig. 17 *Phase Disposition (PD) modulation and* V_{oa}.

SIMULATION

1.Verification of the PD modulation technique

Simulation variables:

V(n001)	First carrier signal $[0,\frac{V_{dc}}{2}]$
V(n002)	Second carrier signal $[-\frac{V_{dc}}{2}, 0]$
V(n006)	First reference signal
V(n004)	Second reference signal
V(n005)	Third reference signal

Choosing **m = 0.95** the waveforms shown in the Fig.18 are obtained. In this situation it is noted that the reference signal does not reach the value $\frac{V_{dc}}{2} = 50v$

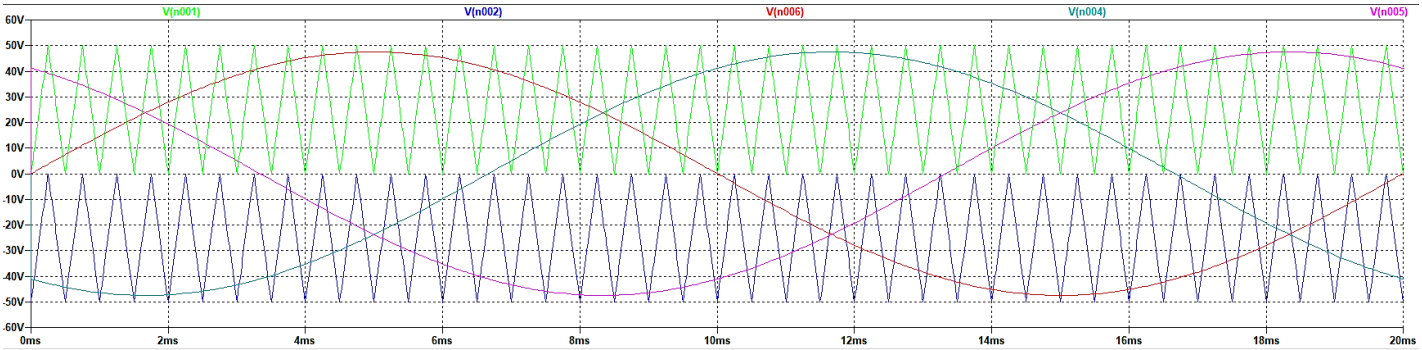


***Fig. 18** PD Modulation technique with **m=0.95**.*

Choosing **m = 1** the waveforms shown in Fig.19 are obtained. The amplitude of the waveforms is equal to the amplitude of the carrier. This is the maximum value of m that can be chosen. With **m>1** there is <u>over modulation.</u> In overmodulation, the amplitude of the waveforms is greater than the amplitude of the carriers (Fig.20).

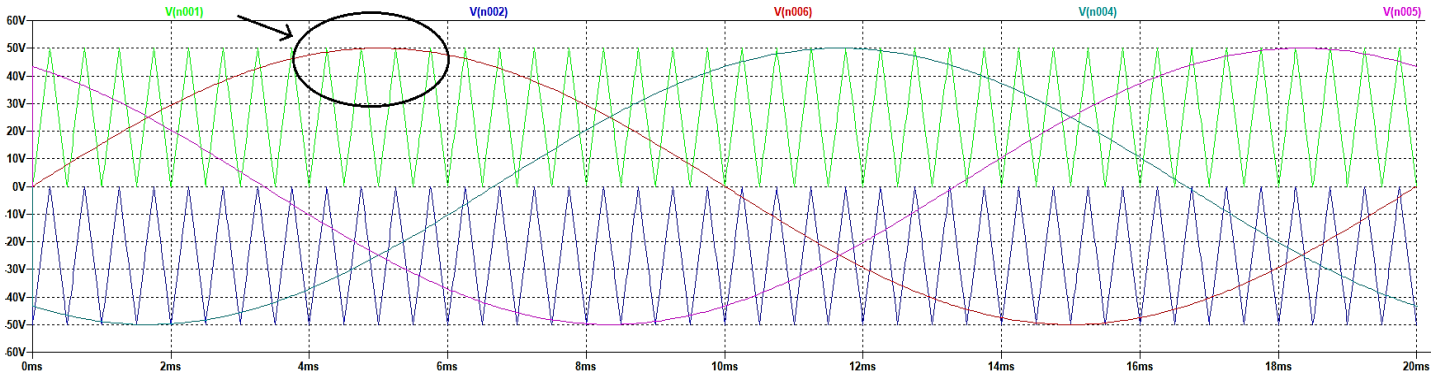


***Fig. 19** PD Modulation technique with **m = 1**.*

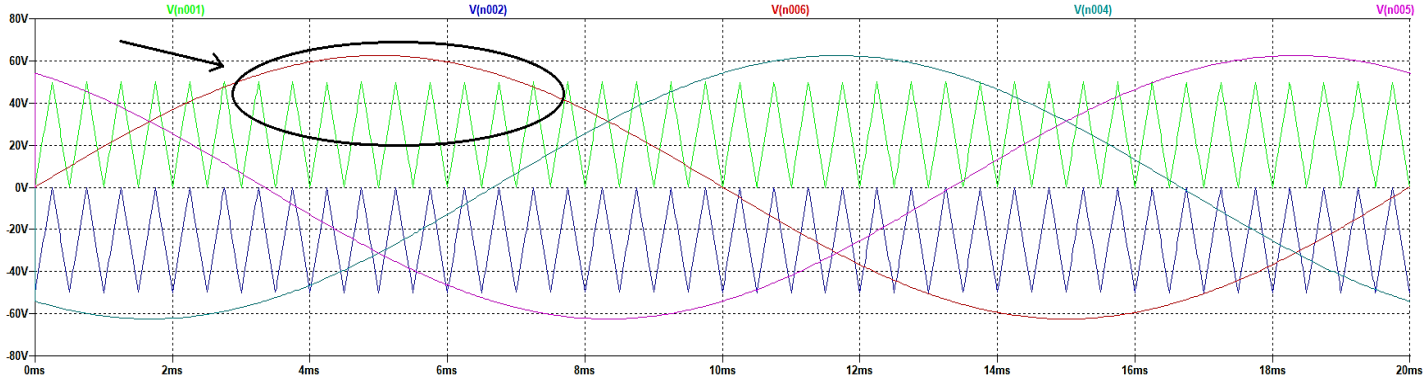


Fig. 20 *PD Modulation technique with* ***m = 1.25****.*

2. Pole voltage, Line-to-line voltage, Phase voltage

- POLE VOLTAGES

As seen above, when working with a three-level inverter, the pole voltages can assume three possible values.

V(n010)	First Pole Voltage (V_{ao})
V(n013)	Second Pole Voltage (V_{bo})
V(n015)	Third Pole Voltage (V_{co})

As shown in the Fig.21, the possible values are: $-\frac{V_{dc}}{2}, 0, \frac{V_{dc}}{2}$ (or -50v,0v,50v)

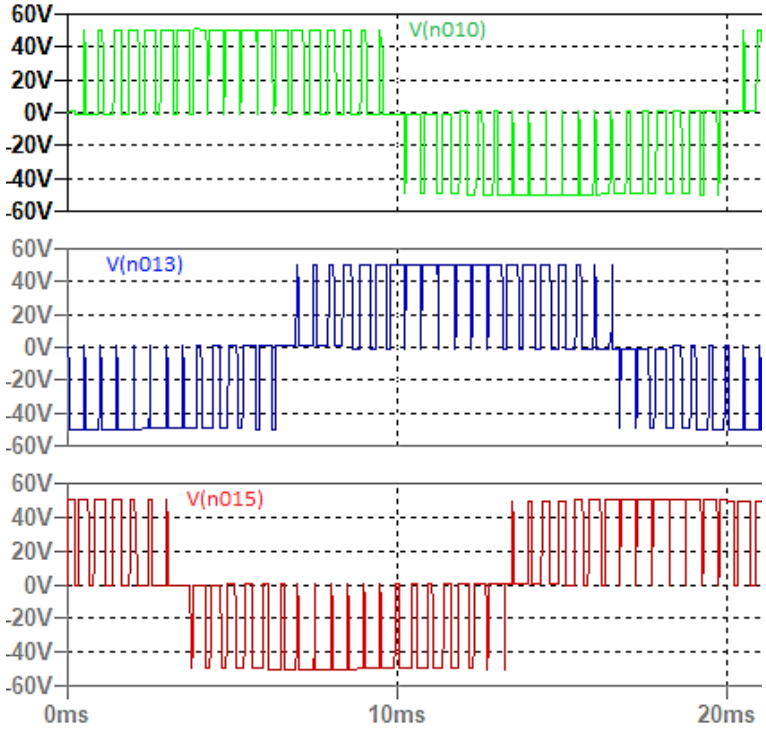


Fig. 21 *Pole voltages three level inverter.*

- LINE-TO-LINE VOLTAGES

The Fig.22 shows the line-to-line voltages. They can be calculated analytically starting from the pole voltages (also through the phase voltage).

$$V_{12} = V_{ao} - V_{bo} \qquad V_{23} = V_{bo} - V_{co} \qquad V_{31} = V_{co} - V_{ao}$$

V(N010, N013)	Line-to-line voltage V_{12}
V(N013, N015)	Line-to-line voltage V_{23}
V(N015, N010)	Line-to-line voltage V_{31}

The line-to-line can assume five possible values: -V_{dc}, $-\frac{V_{dc}}{2}$, 0, $\frac{V_{dc}}{2}$, V_{dc} (or -100, -50, 0, 50, 100)

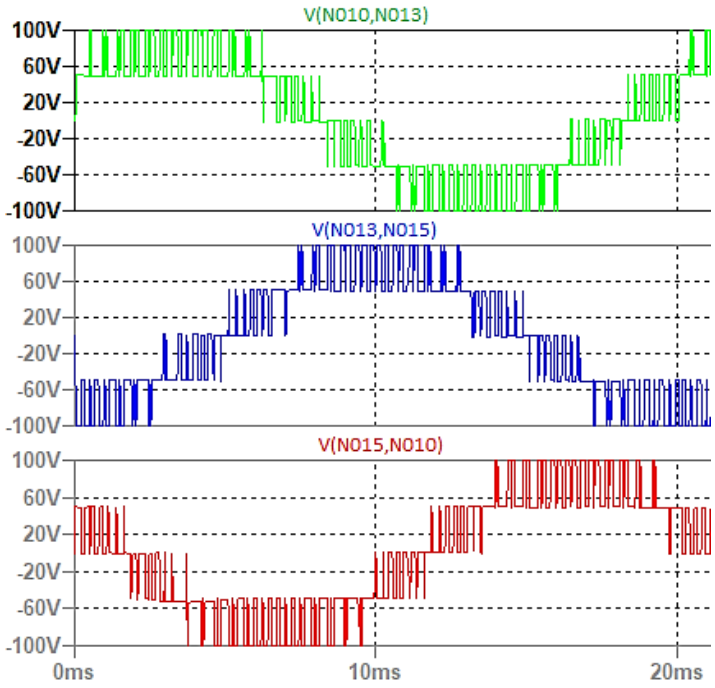


Fig. 22 *Line-to-line three level invert.*

- PHASE VOLTAGE

The Fig.23 shows the phase voltages. They can be calculated analytically starting from the line-to-line voltage.

$$e_1 = \frac{V_{12} - V_{31}}{3}; \quad e_2 = \frac{V_{23} - V_{12}}{3}; \quad e_3 = \frac{V_{31} - V_{23}}{3}$$

V(N010, N012)	Phase Voltage e_1
V(N013, N012)	Phase Voltage e_2
V(N015, N012)	Phase Voltage e_3

The Phase Voltage can assume nine possible values.

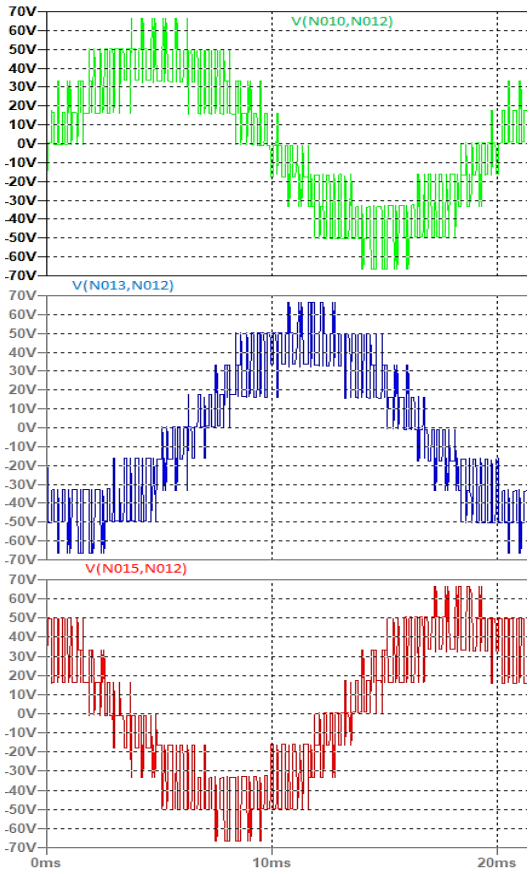


Fig. 23 *Phase voltage three level inverter.*

3. Frequency spectrum and THD

One of the major problems in electric power quality is the harmonic contents. There are several methods of indicating the quantity of harmonic contents. The most widely used measure is the total harmonic distortion (THD). THD allow us to quantify how much the output voltage is distorted. THD represents the harmonic distortion compared to the fundamental component.

- POLE VOLTAGE

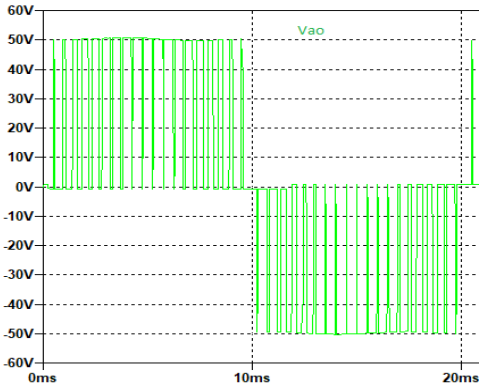


Fig. 24 *Pole Voltage* V_{ao}.

Only the pole voltage V_{ao} has been considered. It is shown in Fig.24. The period of the FFT (Fast Fourier Transform) has been chosen equal to 100ms which is a multiple of the fundamental period equal to 20ms. The frequency spectrum is shown in the Fig.25. The fundamental harmonic is present at 50 Hz the other harmonics are around the multiple of the switching frequency.
There is no DC component, this has been evaluated using the **.four** directive, choosing 50 Hz as the fundamental frequency and 100 as the number of harmonics to be analyzed, the result of which is shown in Fig.26.

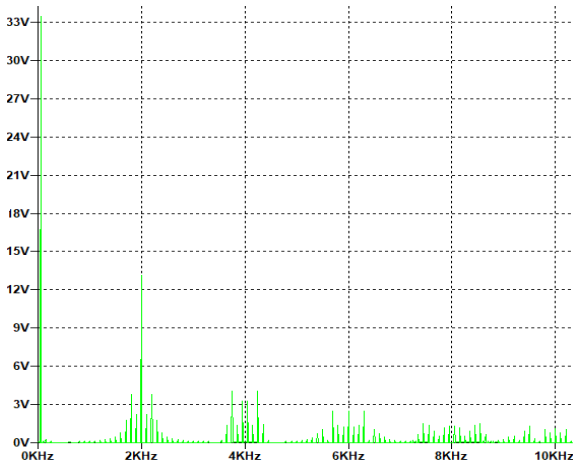


Fig. 25 Frequency spectrum ($f_{sw} = 2kHz$) of the pole voltage V_{ao}.

```
.four 50Hz 100 V(n010)
Fourier components of V(n010)
DC component:0.0556849
Total Harmonic Distortion: 50.199929% (58.740854%)
```

Fig. 26 Directive to find the Fourier transform.

By increasing the switching frequency ($f_{sw} = 5kHz$) the THD of the pole voltage does not change (Fig.27), because its value depends only on m. The harmonics move from low to high frequencies making it easier to build the low pass filter.

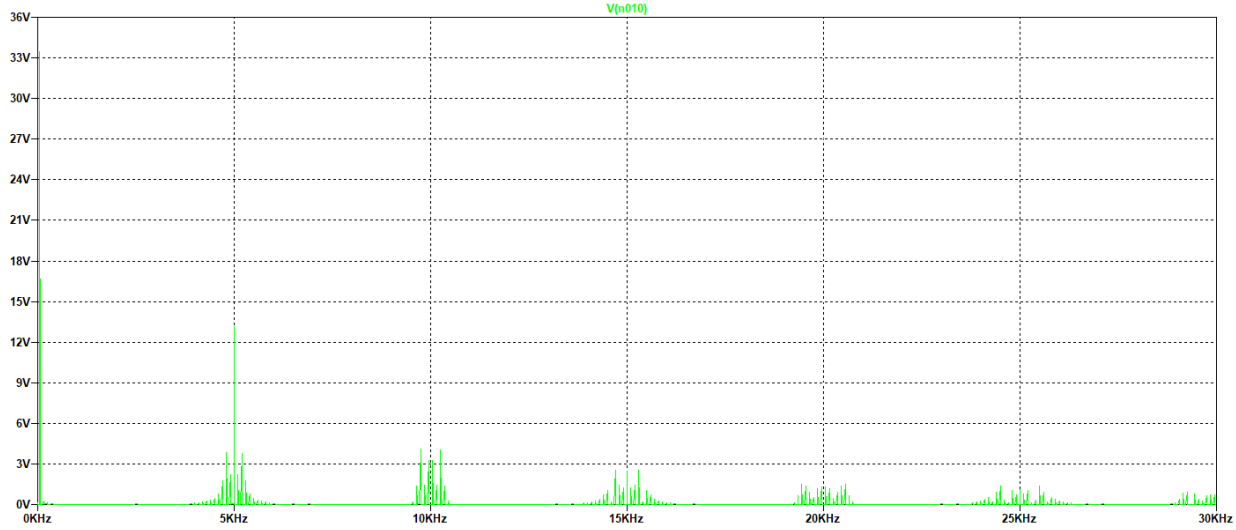


Fig. 27 Frequency spectrum ($f_{sw} = 5kHz$) of the pole voltage V_{ao}.

- PHASE VOLTAGE

Only the phase voltage e_1 has been considered. It is shown in Fig.28. The period of the FFT (Fast Fourier Transform) has been chosen equal to 100ms which is a multiple of the fundamental period equal to 20ms.

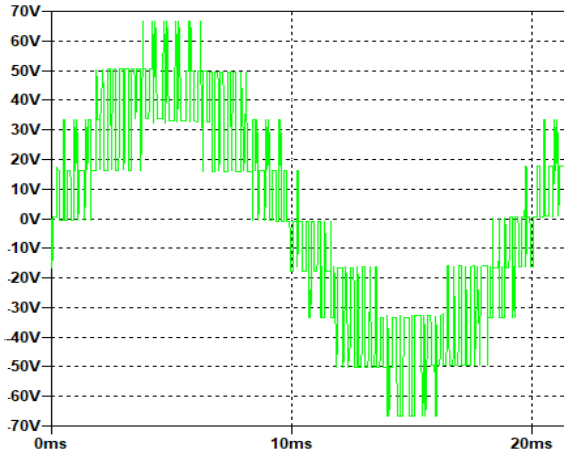


Fig. 28 *Phase voltage e_1.*

The frequency spectrum is shown in the Fig.29. There is <u>no DC component</u>, the fundamental harmonic is present at 50hz, the other harmonics are present around more frequencies of the switching frequency.

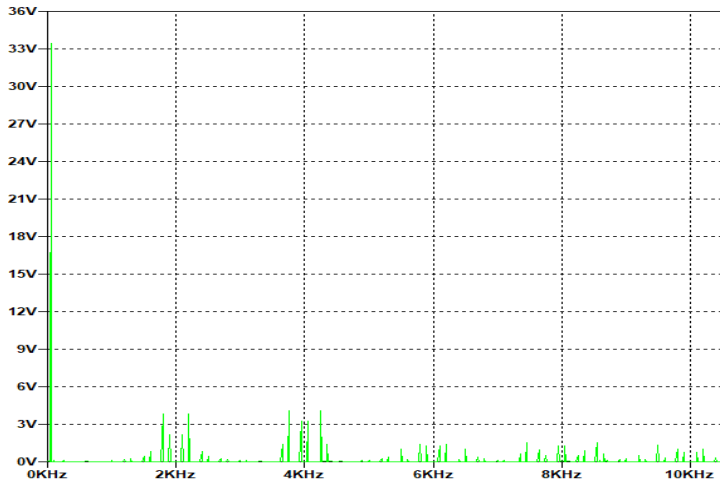


Fig. 29 *Frequency spectrum ($f_{sw} = 2kHz$) of the phase voltage e_1.*

Also, in this case the THD was calculated, in a first analysis it was considered **m = 0.95**, subsequently **m = 1**. The results are shown in Fig30 and Fig.31, respectively.

```
.four 50Hz 100 V(n010,n012)
Fourier components of V(n010,n012)
DC component:-0.0453538
Total Harmonic Distortion: 29.724684% (37.593359%)
```

Fig. 30 *THD phase voltage e_1 with **m = 0.95**.*

```
Fourier components of V(n010,n012)
DC component:-0.0453538
Total Harmonic Distortion: 29.473687% (35.408729%)
```

*Fig. 31 THD phase voltage e_1 with **m = 1**.*

It is noted that increasing the value of m (it must always be m ≤1) the value of the THD decreases. In both cases, a very low THD value is obtained compared to two-level inverters. Increasing the value of the switching frequency the value of THD does not change.

- CURRENT

Only the current that flows through the first phase i_1 has been considered. The course of this current is shown in Fig.32. The quality of the current is much better than the two-level case.

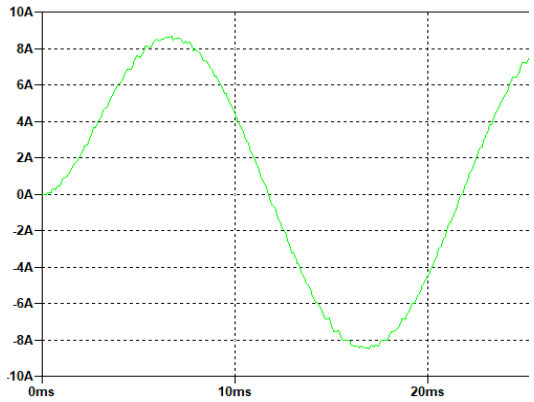


Fig. 32 Phase current one.

The value of the <u>THD of the phase current depends on **m**, f_{sw}, **load** values.</u> The value of THD with m = 0.95, f_{sw} = 2kHz, Load: L=10mH R=5Ω it is shown in Fig.33. The frequency spectrum is shown in the Fig.34. There is <u>no DC component</u>.

```
.four 50Hz 100 I(L1)
Fourier components of I(l1)
DC component:-0.00909696
Total Harmonic Distortion: 1.101436% (1.123304%)
```

Fig. 33 THD Phase current with m = 0.95, fsw = 2kHz, Load: L=10mH R=5Ω.

Changing the values:

m	0.95	1	0.95	0.95	0.95
f_{sw}	2kHz	2kHz	5kHz	2KHz	2KHz
Load	L=10mH R=5Ω	L=10mH R=5Ω	L=10mH R=5Ω	L=50mH R=5Ω	L=10mH R=50Ω
THD	**1.12%**	**1.16%**	**0.48%**	**0.60%**	**5.51%**

It can be seen from the previous table that by increasing the inductance of the load the value of the current THD becomes very small. By increasing the load resistance, the THD increases. The THD also decreases if the switching frequency is increased.

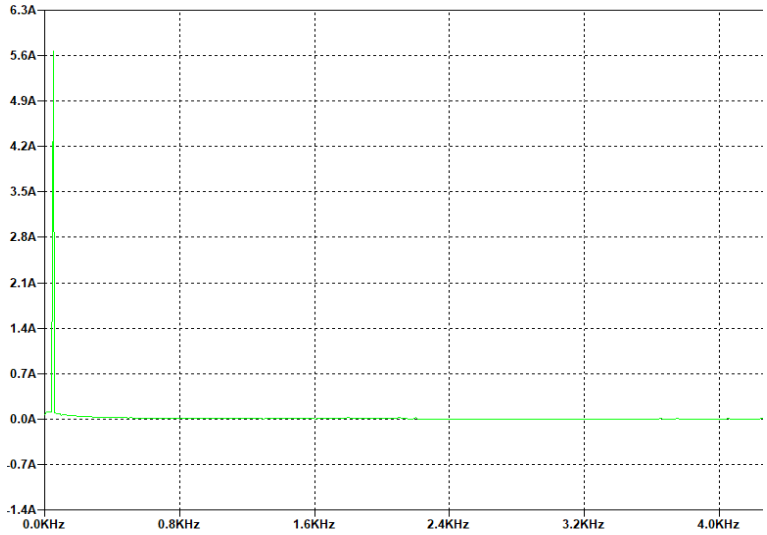


Fig. 34 *Frequency spectrum ($f_{sw} = 2kHz$) of the phase current i_a.*

4. Self-Balancing capacitors

In general, there can be problems when using capacitors. The two capacitors present in the circuit may be unbalanced. As shown in the Fig. 35, the current flows on the capacitors only if the pole voltage (V_{ao}) is zero and corresponds to the load current.

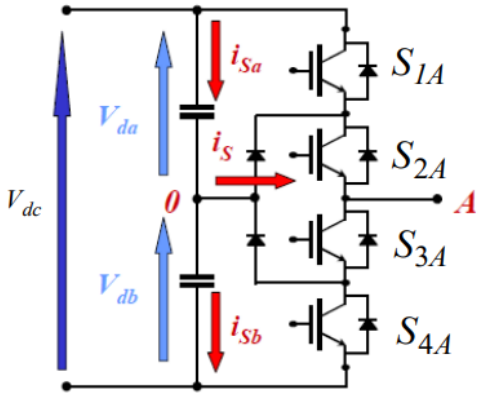


Fig. 35 *Current on the capacitor.*

Decreasing the value of the capacitance of the capacitors (for example C=2mF), the pole voltages have oscillations. These oscillations are shown in the Fig.36. These oscillations are due to the charging and discharging of the two capacitors. Small oscillations can be obtained by increasing the values of the capacitors. By increasing the capacitor values, costs and dimensions increase.
In real applications, the capacitance values are chosen based on the oscillation value that can be accepted.
Fig.37 shows the trends of the voltages on the two capacitors with initial conditions equal to $\frac{V_{dc}}{2}$. The trends show that the two capacitors are perfectly balanced.

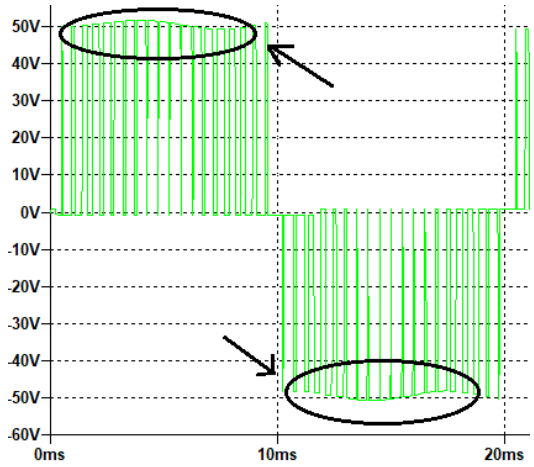


Fig. 37 *Oscillations on pole voltage V_{ao} with C=2mF*

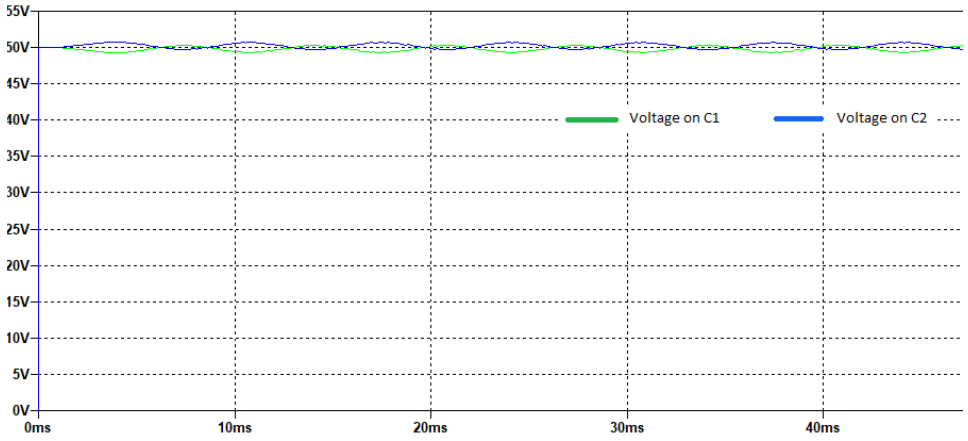


Fig. 36 *Voltage on the two capacitors.*

By changing the initial conditions for example:

$$IC_1 = \{\frac{V_{dc}}{2} + \frac{V_{dc}}{4}\} \quad IC_2 = \{\frac{V_{dc}}{2} - \frac{V_{dc}}{4}\}$$

The trends of Fig. 38 are obtained. The two capacitors voltage start to converge, this means that this inverter is self-balanced. This result was achieved thanks to the type of modulation used.

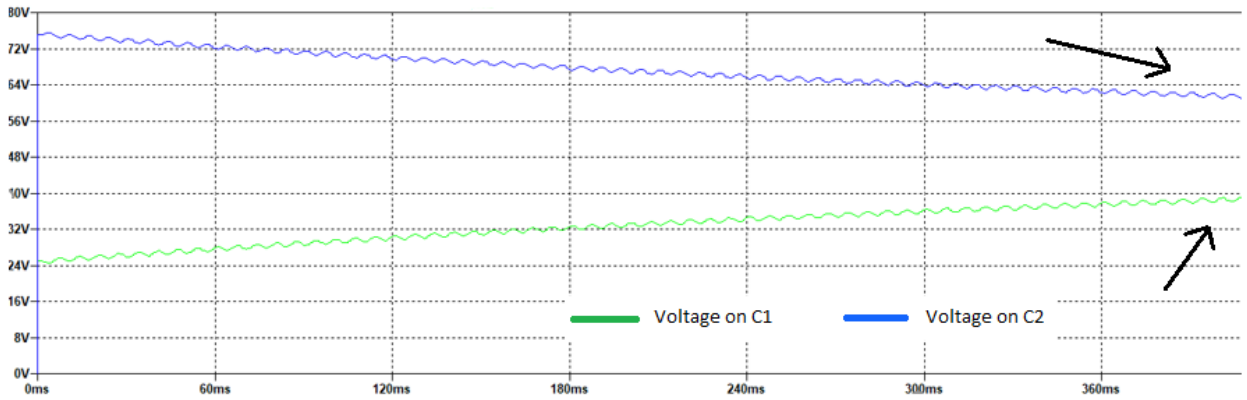


Fig. 38 *Voltage on capacitors with different initial condition.*