KSZ8795CLX

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ8795CLX 10/100Base-T/TX five-port switch, which has four copper ports (Ports 1 to 4) and one uplink port (Port 5). The uplink Port 5 supports GMII/RGMII/MII/RMII™ configurable interface. The checklist items should be followed when using the KSZ8795CLX in a new design. A summary of these items is provided in Section 12.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet Signals"
- Section 5.0, "Clock Circuit"
- Section 6.0, "Configuration for System Application"
- Section 7.0, "Digital Interface"
- Section 8.0, "Management Interface"
- Section 9.0, "Startup"
- Section 10.0, "Configuration Pins (Strapping Options)"
- Section 11.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The KSZ8795CLX implementor should have the following documents on hand:

- *KSZ8795CLX Integrated 5-Port 10/100-Managed Ethernet Switch with Gigabit GMII/RGMII and MII/ RMII Interfaces Data Sheet*
- KSZ8795CLX _DP_V1.1.zip for the KSZ8795CLX Design Package

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

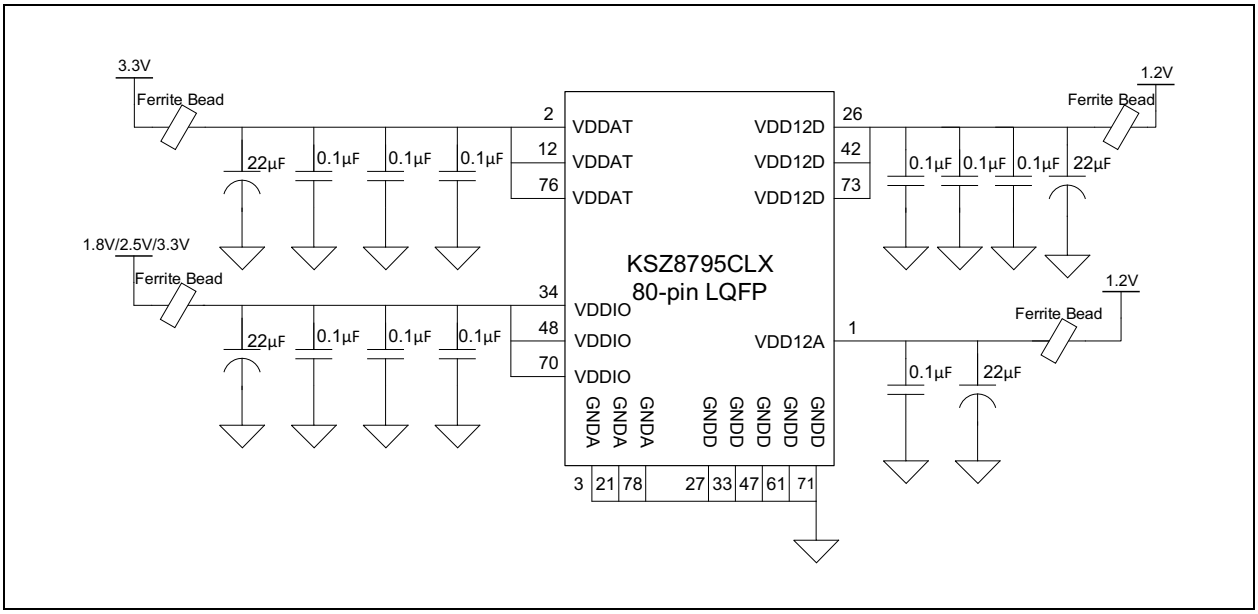
- **GNDD** is the digital ground, while the ground pin **GNDA** is the analog ground. Both **GNDD** and **GNDA** grounds should be connected to the solid contiguous ground plane as a system ground on the board. Separate digital ground and analog ground planes are not recommended.
- If using the magnetics and RJ45 connector, a chassis ground should be used for the line side of the magnetics and the metal case of the RJ45 connector. The system ground and the chassis ground should be tied together by a ferrite bead. The ferrite bead should be placed far away from the Ethernet device for better ESD and EMI.

3.0 POWER

- The analog supply (**VDDAT33**) pins on the KSZ8795CLX are 2, 12, and 76. They require connections to **VDDAT33** (created from +3.3V through a ferrite bead).
- KSZ8795CLX **VDDIO** supports three VDDIO voltages—1.8V, 2.5V, and 3.3V. Pins 34, 48, and 70 (**VDDIO**) should be connected to one of the three VDDIO voltages through a ferrite bead.
- The analog 1.2V core power pin is pin 1, while the digital 1.2V core power pins are pins 26, 42, and 73. Both analog 1.2V and digital 1.2V need a ferrite bead from the 1.2V power rail.
- Be sure to place 4.7 µF to 22 µF bulk capacitors on each side of the ferrite beads. In addition, make sure to use 0.1 µF capacitors to decouple the device for all power pins. The decoupling capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



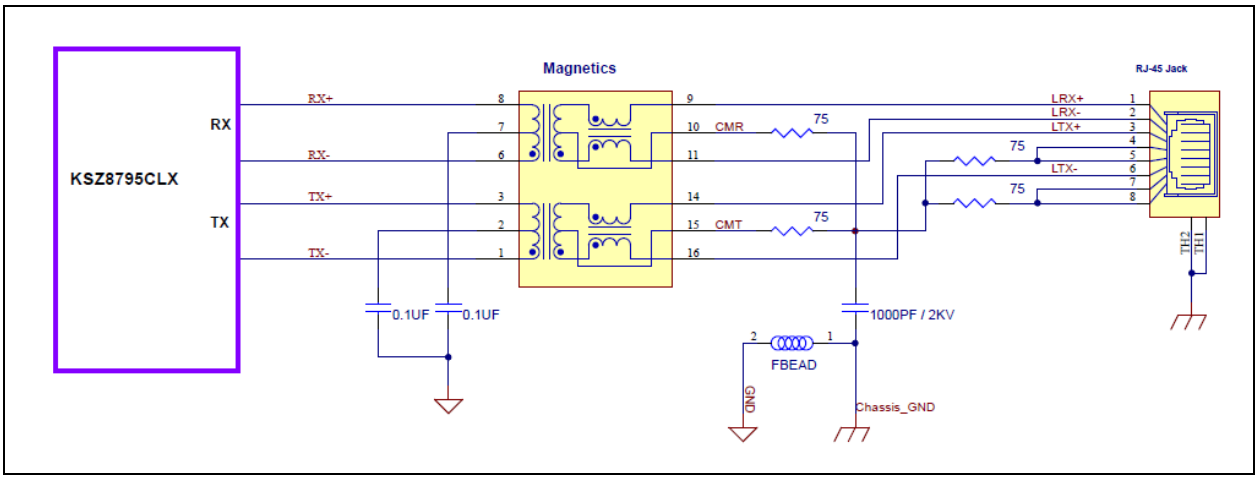
4.0 ETHERNET SIGNALS

The KSZ8795CLX has four integrated PHYs that support 10/100Base-T/TX Ethernet copper ports. These PHYs are fully compliant with the IEEE 802.3u standard.

4.1 KSZ8795CLX Copper Port Connection

- The KSZ8795CLX has four Ethernet copper ports. All ports are voltage drivers with internal DC biasing and on-chip termination, so there are no external termination resistors and DC biasing power on the magnetics. Each port connection between KSZ8795CLX and magnetics is illustrated in Figure 4-1.

FIGURE 4-1: ONE ETHERNET PORT CONNECTION WITH MAGNETICS



- Both center taps, **RX** and **TX**, of the magnetics on the chip side should be separately connected to ground with two capacitors.
- In the Ethernet switch, **RX**+/– differential pair should be connected to RJ45 connector pins 1 and 2 through magnetics.
- In the Ethernet switch, **TX**+/– differential pair should be connected to RJ45 connector pins 3 and 6 through magnetics.
- For unused Ethernet copper port, the user may leave the **RX** pair and the **TX** pair floating, because the KSZ8795-CLX analog ports have internal termination.

4.2 Magnetics Connection at the Chip Side

- The center tap connection on the KSZ8795CLX side for the transmit channel should not be connected to **VDDAT**. The transmit channel center tap of the magnetics should connect to system ground through Common-mode capacitor only. The Common-mode capacitor value can be from 0.1 µF to 10 µF.
- The center tap connection on the KSZ8795CLX side for the receive channel should not be connected to **VDDAT**. The receive channel center tap of the magnetics should connect to system ground through Common-mode capacitor only. The Common-mode capacitor value can be from 0.1 µF to 10 µF.
- When using the KSZ8795CLX switch in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the *Application Note 8.13 Suggested Magnetics* for detailed information on proper magnetics.

4.3 Magnetics Connection at Line Side of the RJ45 Connector

- In the switch design, pin 1 of the RJ45 should connect to **RX**+ of the KSZ8795CLX, while pin 2 of the RJ45 should connect to **RX**– of the device.
- In the switch design, pin 3 of the RJ45 should connect to **TX**+ of the KSZ8795CLX, while pin 6 of the RJ45 should connect to **TX**– of the KSZ8795CLX.
- The center tap connection on the cable side (the RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.

- The center tap connection on the cable side (the RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- RJ45 pins 4 and 5 should be shorted and then terminated with a 75Ω resistor through the 1000 pF to the chassis ground.
- RJ45 pins 7 and 8 should be shorted and then terminated with a 75Ω resistor through the 1000 pF to the chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. The capacitor is shared by both **TX** and **RX** center taps.
- The RJ45 connector shield should be tied directly to the chassis ground.

4.4 Alternative Termination Selection for RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. This can be done in two ways:
  1. Pins 4 and 5 can be connected to two 49.9Ω resistors. The common connection of these resistors should be linked through a third 49.9Ω resistor to the 1000 pF, 2kV capacitor.
  2. For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. An equivalent circuit is created by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2kV capacitor. This can be done in two ways:
  1. Pins 7 and 8 can be connected to two 49.9Ω resistors. The common connection of these resistors should be linked through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  2. For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. An equivalent circuit is created by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both 4 and 5 termination pins as well as pins 7 and 8 termination pins.
- The RJ45 connector shield should be attached directly to the chassis ground.

4.5 Using RJ45 with Integrated LED

- The user can utilize the RJ45 connector with integrated LED components if the product working environment is not very noisy.
- If the designed product works in an electrically noisy external environment, it is not advisable to use RJ45 with integrated LED. This is because the outside interference signal or voltage could be coupled to the LED circuit through the line side of RJ45 due to the LED circuit directly connected to chip and system power or ground. It is better to use independent LED components.
- If the user needs to use the RJ45 with an integrated LED circuit in a noisy environment, consider adding TVS diodes to protect the chip.

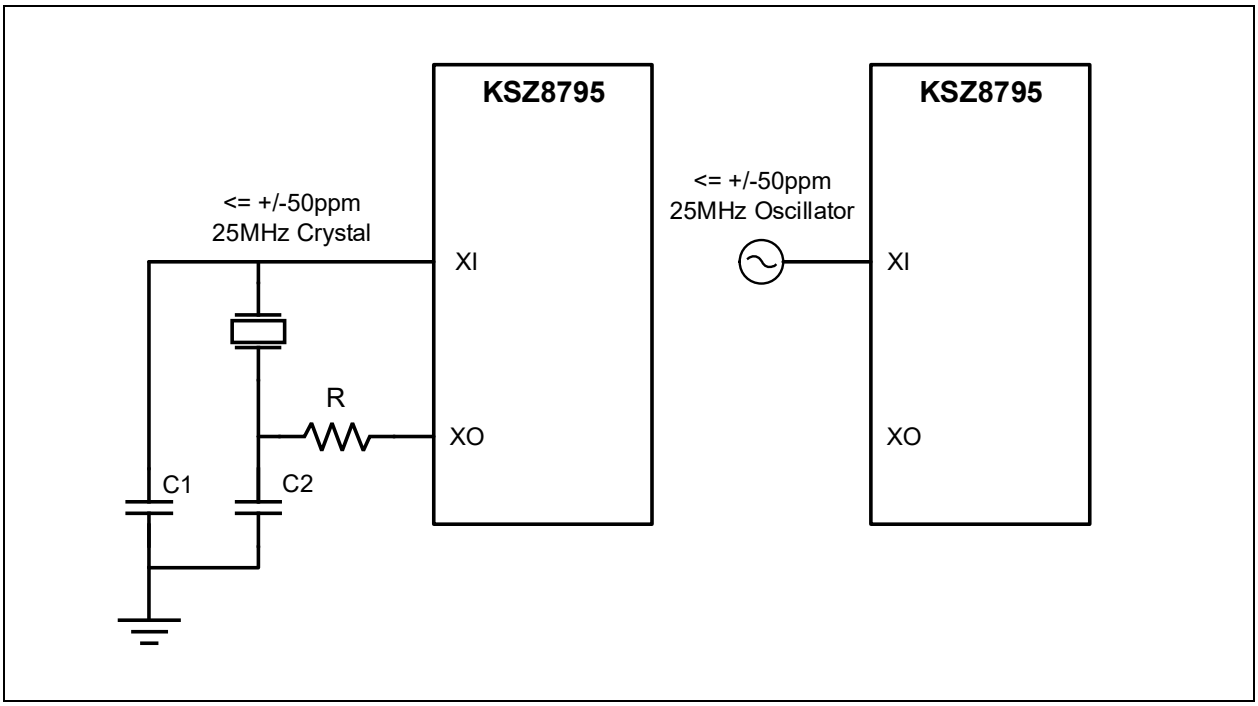
5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections

A 25.000 MHz (±50 ppm) crystal should be used to provide the clock source. For the complete crystal specifications and tolerances, refer to the *KSZ8795CLX Data Sheet*.

- **XI** (pin 79) is the clock circuit input for the KSZ8795CLX device. This pin requires a capacitor to ground directly when a crystal is used. One side of the crystal connects to this pin.
- **XO** (pin 80) is the clock circuit output from the KSZ8795CLX. When a crystal is used, this pin connects to one side of the crystal pin that requires a capacitor to ground. Consider a 0Ω to 470Ω resistor R as an option for better EMI.
- Since every system design is unique, the capacitor values are system dependent, based on the C_L specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.
- Alternately, a 25.000 MHz clock oscillator may be used to provide the clock source for the KSZ8795CLX. When using a single-ended clock source, **XI** (pin 79) connects to a 3.3V tolerant oscillator. **XO** (pin 80) should be left floating as No Connect (NC). See Figure 5-1.
- An external 1 MΩ resistor between **XI** and **XO** pin is unnecessary because the KSZ8795CLX already has this resistor.
- The use of a crystal or oscillator with a minimum drive level of 50 µW (300 µW typical) is recommended. A higher drive level is more preferable.

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS FOR KSZ8795CLX



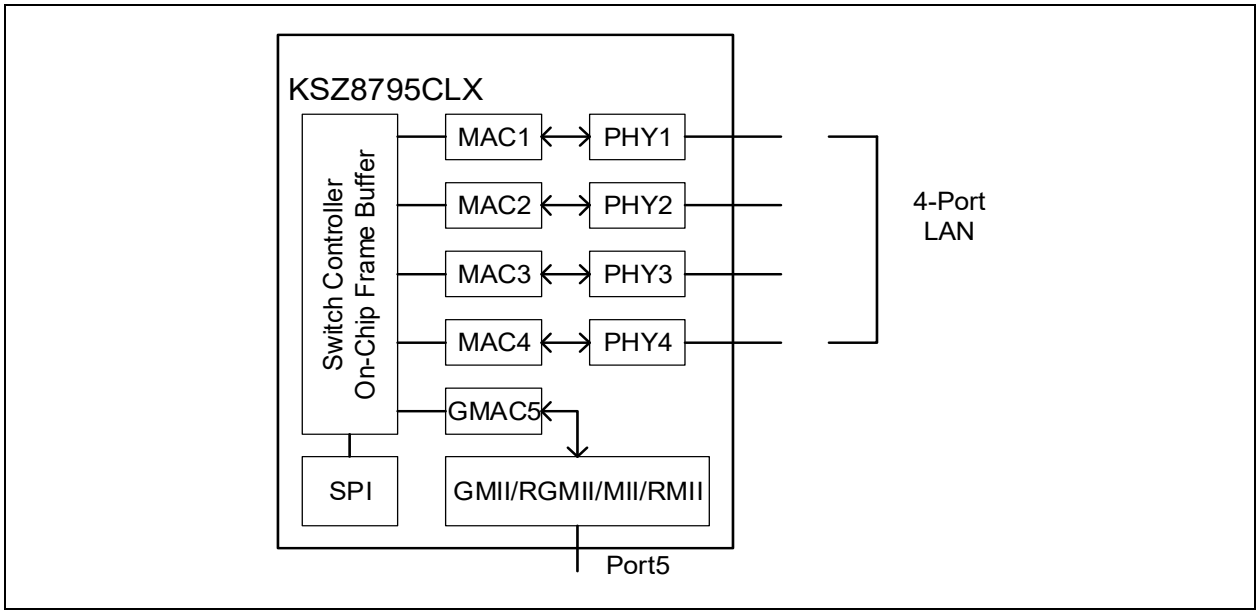
6.0 CONFIGURATION FOR SYSTEM APPLICATION

The KSZ8795CLX applications are in three categories.

6.1 Design for Simple Standalone 4 Port Switch

- In this simple 4-port switch, the unused Port 5 GMAC5 interface should not output any clock signal for better EMI. (See Figure 6-1.)
- Set strap pins LED3[1:0]=01 and LED1_1 with its default state for RMII™ Normal mode (without clockout).

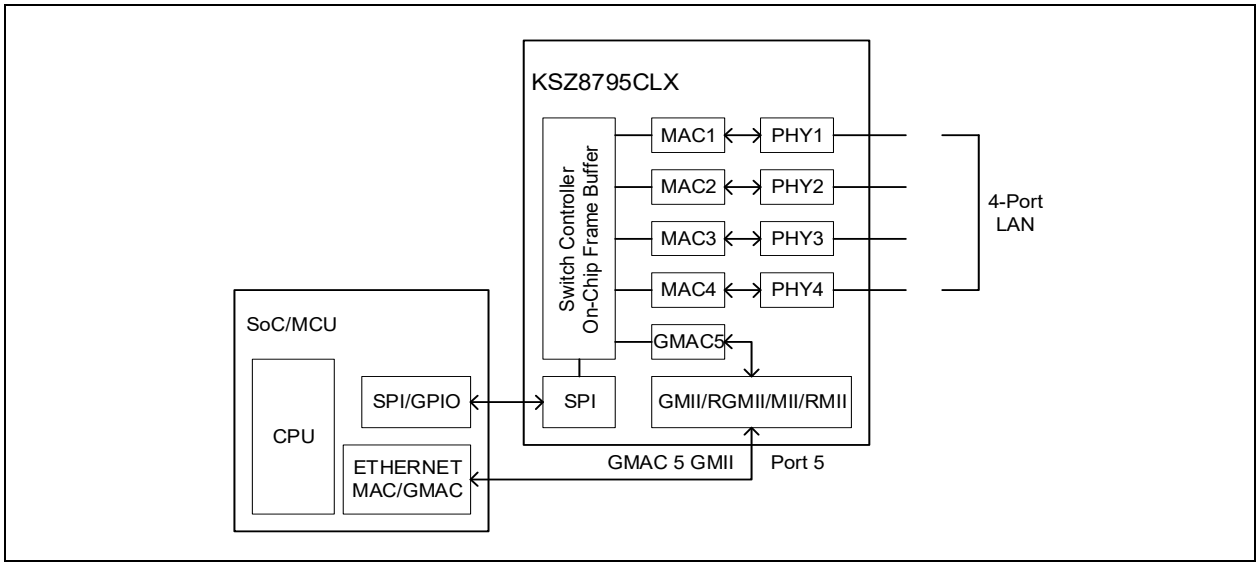
FIGURE 6-1: UNMANAGED STANDALONE SWITCH



6.2 Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 GMII

- Set strap pins LED3[1:0] = 10 for Port 5 GMAC5 to GMII. KSZ8795CLX GMII supports 1000Base-TX mode only.
- Use SPI interface that can access all register for a managed switch. See Figure 6-2.

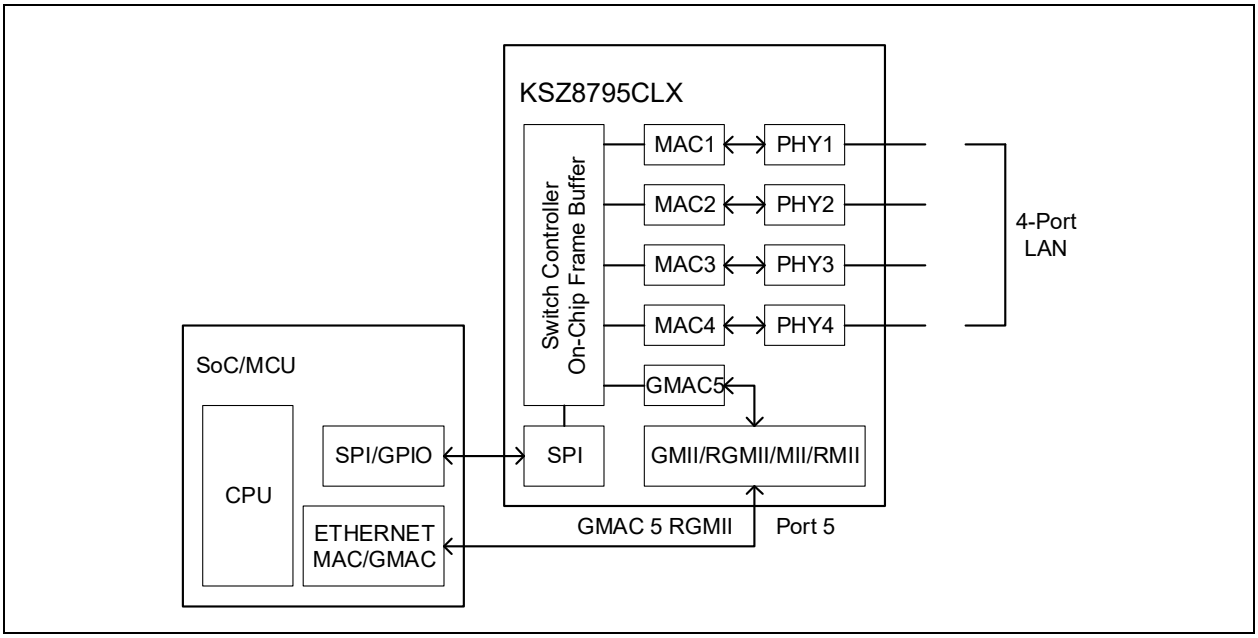
FIGURE 6-2: DIAGRAM EXAMPLE FOR PORT 5 USING GMII INTERFACE



6.3 Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 RGMII

- Set strap pins LED3[1:0] = 11 (default value) for Port 5 GMAC5 to RGMII. KSZ8795CLX RGMII supports 10/100/1000Base-T/TX mode.
- Use SPI interface that can access all register for a managed switch. See Figure 6-3.

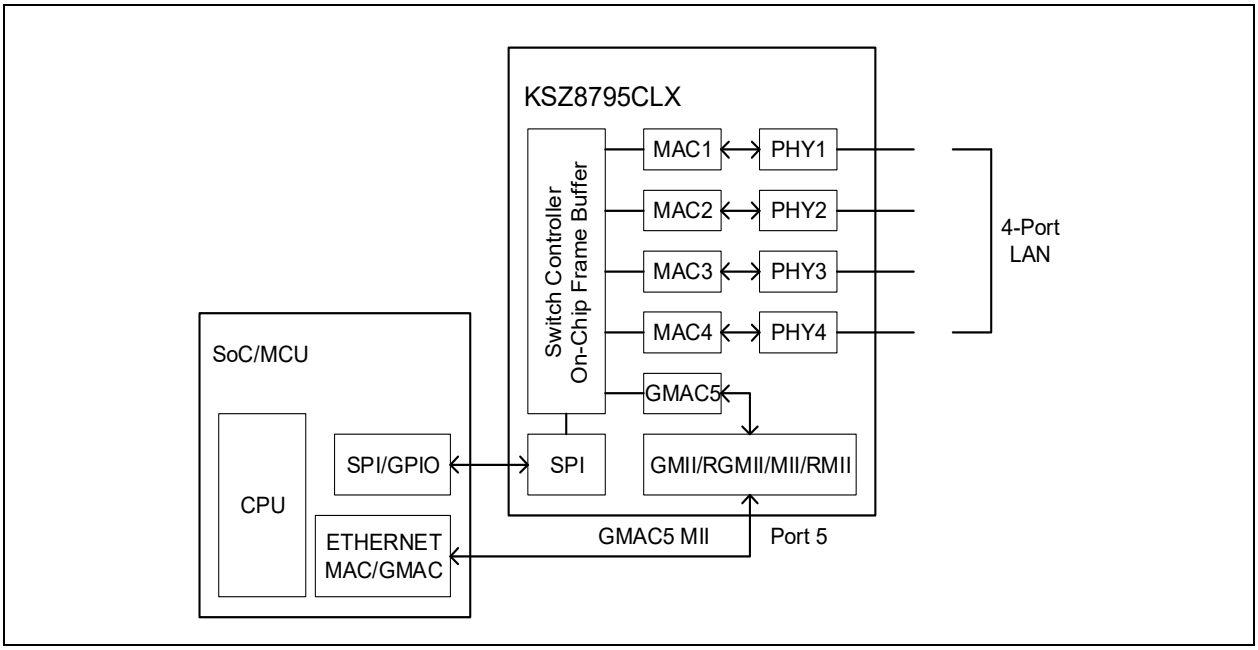
FIGURE 6-3: DIAGRAM EXAMPLE FOR PORT 5 USING RGMII INTERFACE



6.4 Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 MII

- Set strap pins LED3[1:0] = 00 (use two pull-down resistors) for Port 5 GMAC5 to MII. KSZ8795CLX MII supports 10/100Base-T/TX mode.
- Use SPI interface that can access all registers for a managed switch. See Figure 6-4.

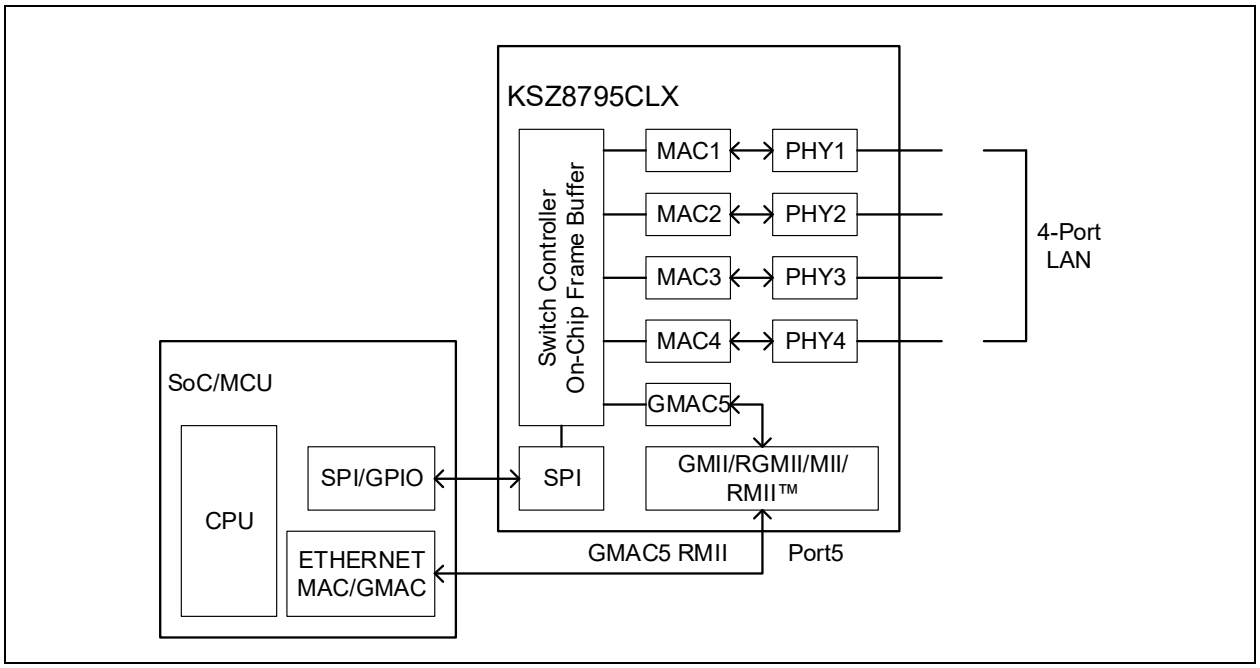
FIGURE 6-4: DIAGRAM EXAMPLE FOR PORT 5 USING MII INTERFACE



6.5 Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 RMII™

- Set strap pins LED3[1:0] = 01 (use one pull-down resistor). LED1_1 can be either pull-up or pull-down for Port 5 GMAC5 to RMII™. KSZ8795CLX RMII supports 10/100Base-T/TX mode.
- Use SPI interface that can access all registers for a managed switch. See Figure 6-5.

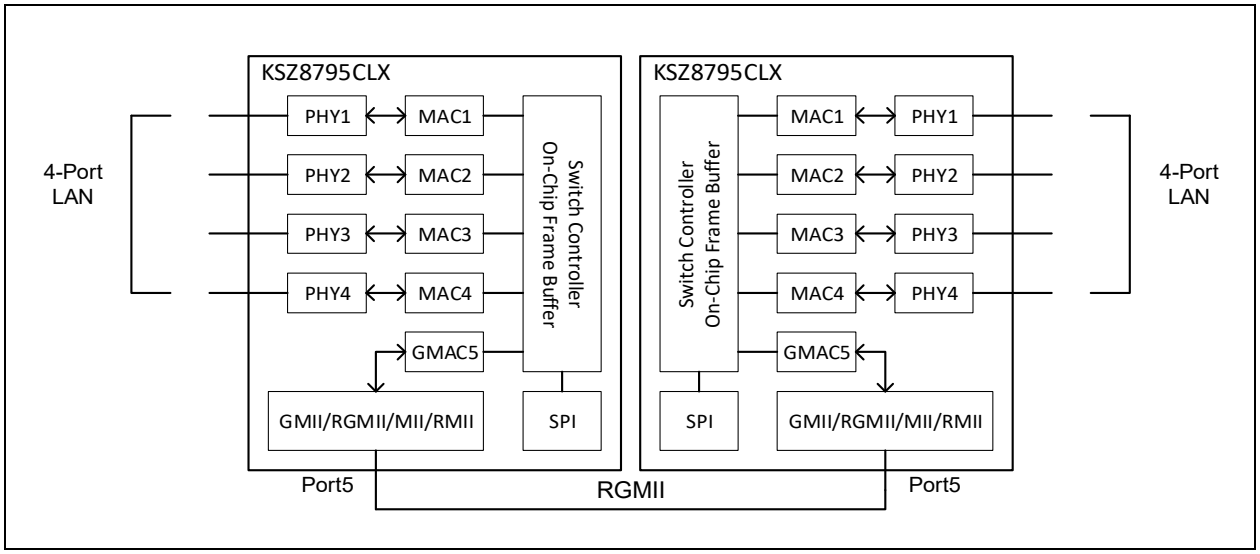
FIGURE 6-5: DIAGRAM EXAMPLE FOR PORT 5 USING RMII™ INTERFACE



6.6 Design for Unmanaged Non-Blocking 8-Port Switch using RGMII Back-to-Back

- No strap-in pins need to be set because Port 5 GMAC5 is RGMII with Gigabit mode by default. See Figure 6-6.

FIGURE 6-6: DIAGRAM EXAMPLE FOR ONE NON-BLOCKING 8-PORT ETHERNET SWITCH



7.0 DIGITAL INTERFACE

7.1 Port 5 GMAC5 SW5-GMII/RGMII/MII/RMII™ Strap Pins for Configuration

- The KSZ8795CLX provides one uplink port, which is Port 5. The uplink Port 5 can be configured to GMII, RGMII, MII, and RMII™ with different modes through the strap pins [24,25], LED3 [1,0], other strap pins, and register. For detailed configurations, refer to Table 7-1.

TABLE 7-1: PORT 5 GMAC5 INTERFACE CONFIGURATIONS

Port 5 GMAC5 Interface Modes	Strap Pin LED3 [1,0] Pull-Up = 1, Pull-Down = 0	Other Related Strap Pins Pull-Up = 1, Pull-Down = 0	Other Related Strap Pins Pull-Up = 1, Pull-Down = 0
MII	00	LED2_1=1 by default, MII MAC mode	LED2_1=0, MII PHY mode
RMII™	01	LED2_1=1 by default, RMII Clock mode (provide 50 MHz)	LED2_1=0, RMII Normal mode (Receive 50 MHz) Device clock source options: 1. LED1_1=1 by default. The switch clock source comes from the local 25 MHz clock. 2. LED1_1=0, the switch clock source comes from the TXC5/ REFCLKI5 external clock.
GMII	10	LED2_1=1 by default, GMII GMAC mode	LED2_1=0, GMII GPHY mode
RGMII	11 (default)	LED1_0=1 by default, RGMII Gbps Speed mode	LED1_0=0 by default, RGMII 10/100 Mbps Speed mode

7.2 Port 5 GMAC5 MII Interface

The KSZ8795CLX provides MAC layer interface for GMAC5. The MII interface contains two distinct groups of signals: one for transmission and one for receiving.

- Refer to Table 7-1 for the detailed configuration of the MAC mode and PHY mode of the Port 5 GMAC5 SW5-MII. The KSZ8795CLX MAC5 MII default is MII MAC mode.
- For major uplink Port 5 GMAC5 MII, set 10 Mbps and 100 Mbps data rates through register 0x06 bit 4. The default speed is 100 Mbps. Set Half-Duplex mode and Full-Duplex mode through register 0x06 bit 6. The default mode is Full-Duplex.
- The other-end MII should have the same speed and Duplex mode settings with KSZ8795CLX Port 5 MII for consistency.
- The KSZ8795CLX Port 5 GMAC5 MII MAC mode and GMAC5 MII PHY mode connections are shown in Figure 7-1 and Figure 7-2.

FIGURE 7-1: CONNECTION BETWEEN KSZ8795CLX PORT 5 GMAC5 MII MAC MODE AND EXTERNAL PHY

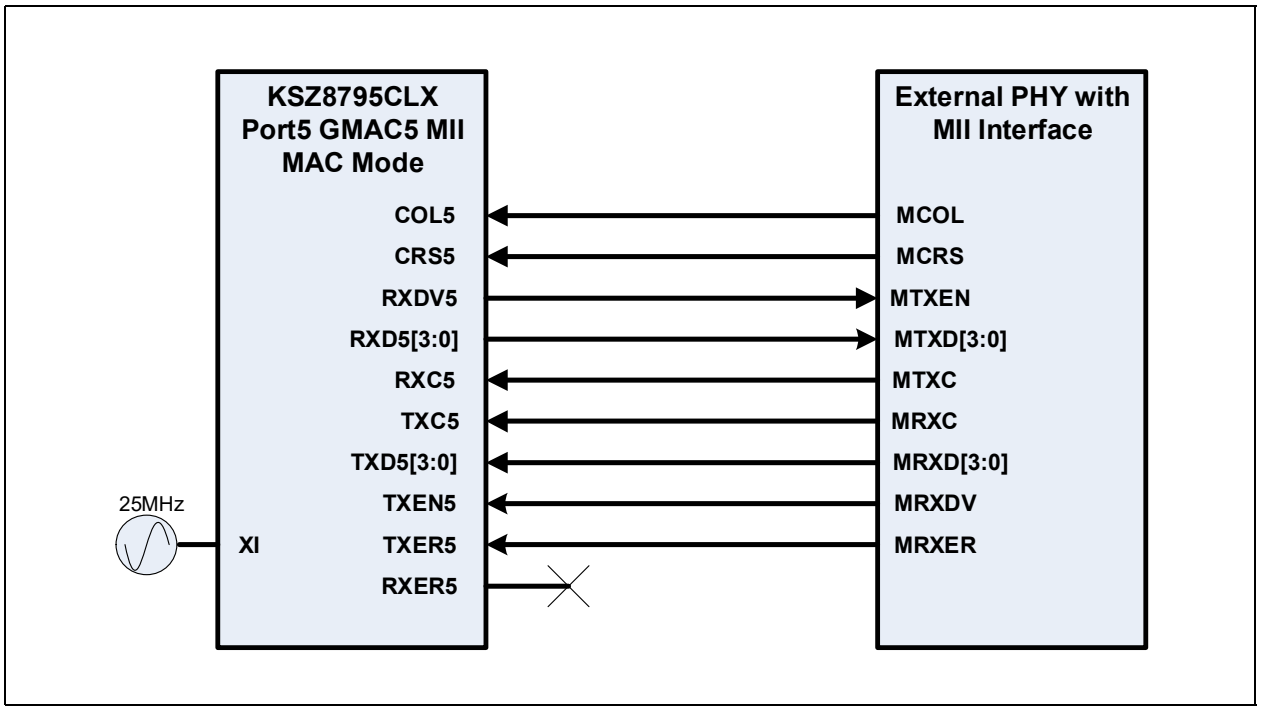
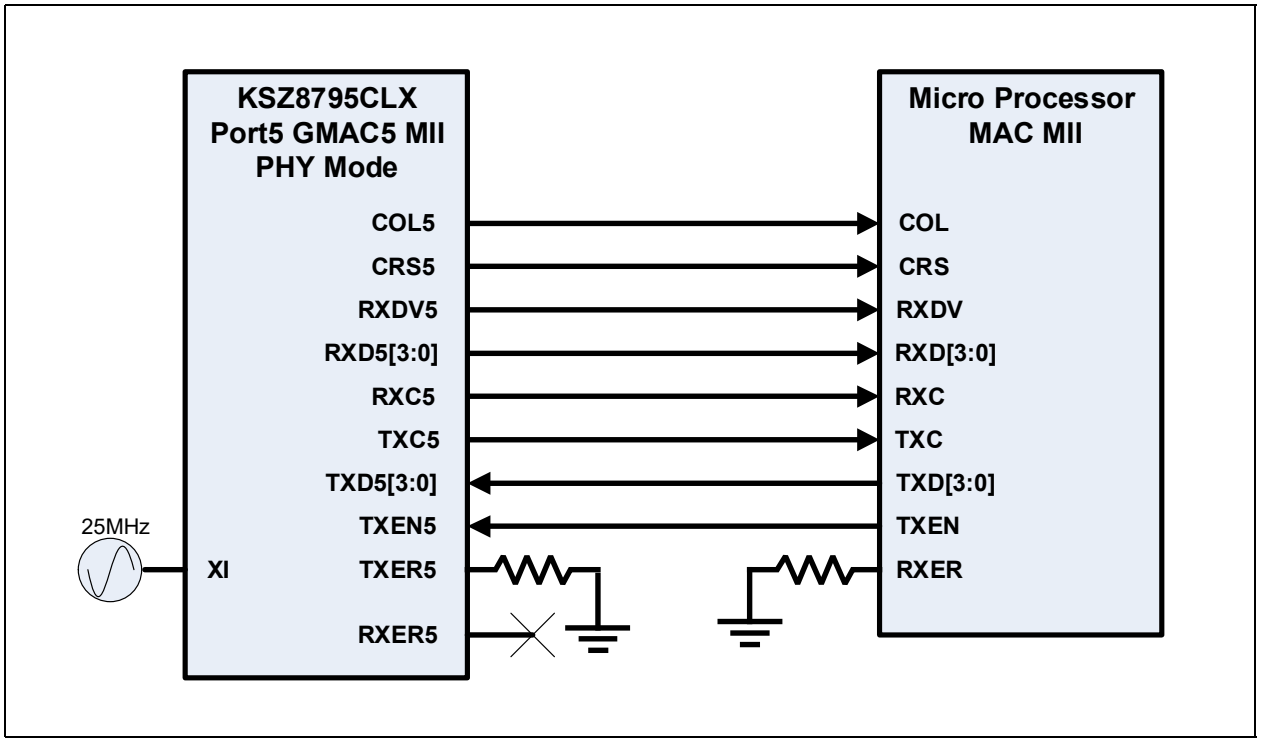


FIGURE 7-2: CONNECTION BETWEEN KSZ8795CLX PORT 5 GMAC5 MII PHY MODE AND MCU



7.3 Port 5 GMAC5 RMII™ Interface

- Table 7-1 shows the detailed configuration of the RMII™ Clock mode and RMII Normal mode of Port 5 GMAC5 SW5-RMII. Based on the diagram, the RMII Clock mode provides a 50 MHz RMII reference clock, while the RMII Normal mode receives a 50 MHz RMII reference clock.
- For major uplink Port 5 GMAC5 RMII, set 10 Mbps and 100 Mbps data rates through register 0x06 bit 4. The default speed is 100 Mbps. Set Half-Duplex mode and Full-Duplex mode through register 0x06 bit 6. The default mode is Full-Duplex. The strap pins [24:25] and LED3 [1:0] should be set to 01.
- SoC MAC RMII should have the same speed and duplex as the RMII interface consistence in the system configuration.
- MAC RMII does not produce any error, so there are minimal error output pins from GMAC5 RMI. The corresponding input pin on the other end can be pulled down by a pull-down resistor.
- The KSZ8795CLX Port 5 GMAC5 RMII Clock mode (output 50 MHz reference clock) and RMII Normal mode (input 50 MHz reference clock) are shown in Figure 7-3 and Figure 7-4, respectively.

7.3.1 PORT 5 GMAC5 RMII™ CLOCK MODE

- The KSZ8795CLX Port 5 GMAC5 can be set to RMII Clock mode by the strap-in pins. See Table 7-1.
- The other side can be an MCU MAC on RMII Normal mode or an external PHY on RMII Normal mode. The connections are illustrated in Figure 7-3 and Figure 7-4, respectively.

FIGURE 7-3: PORT 5 GMAC5 RMII™ CLOCK MODE AND MCU MAC RMII NORMAL MODE

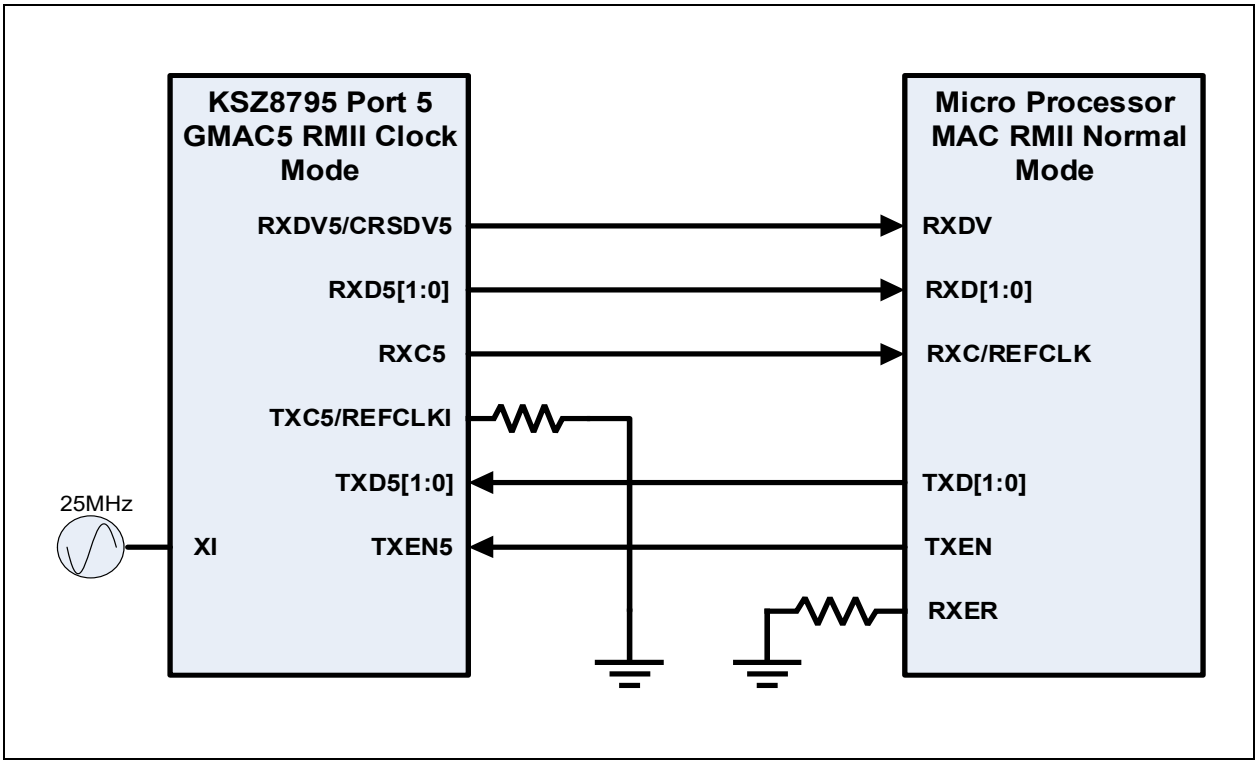
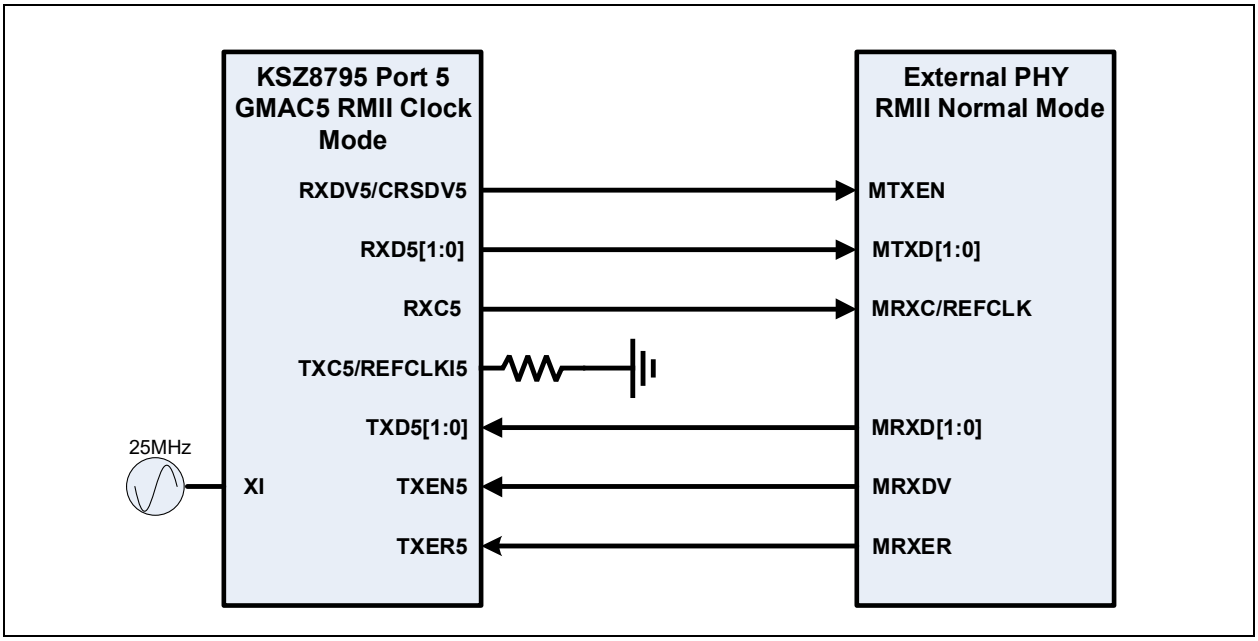


FIGURE 7-4: PORT5 GMAC5 RMII™ CLOCK MODE AND EXTERNAL PHY RMII NORMAL MODE



7.3.2 PORT 5 MAC5 RMII™ NORMAL MODE

- The KSZ8795CLX Port 5 GMAC5 can be set to RMII™ Normal mode by LED2_1 strap pin by a pull-down resistor. In Port 5 GMAC5 RMII Normal mode, the KSZ8795CLX's clock source comes from either 25 MHz crystal/oscillator XI pin (Strap pin LED1_1=1) or TXC5/REFCLKI pin (Strap pin LED1_1=0).
- The other side can be an MCU MAC on RMII Clock mode or an external PHY on RMII Clock mode. The connections are shown in Figure 7-5 and Figure 7-6, respectively.

FIGURE 7-5: CONNECTIONS FOR KSZ8795CLX PORT 5 RMII™ NORMAL MODE AND MCU RMII CLOCK MODE

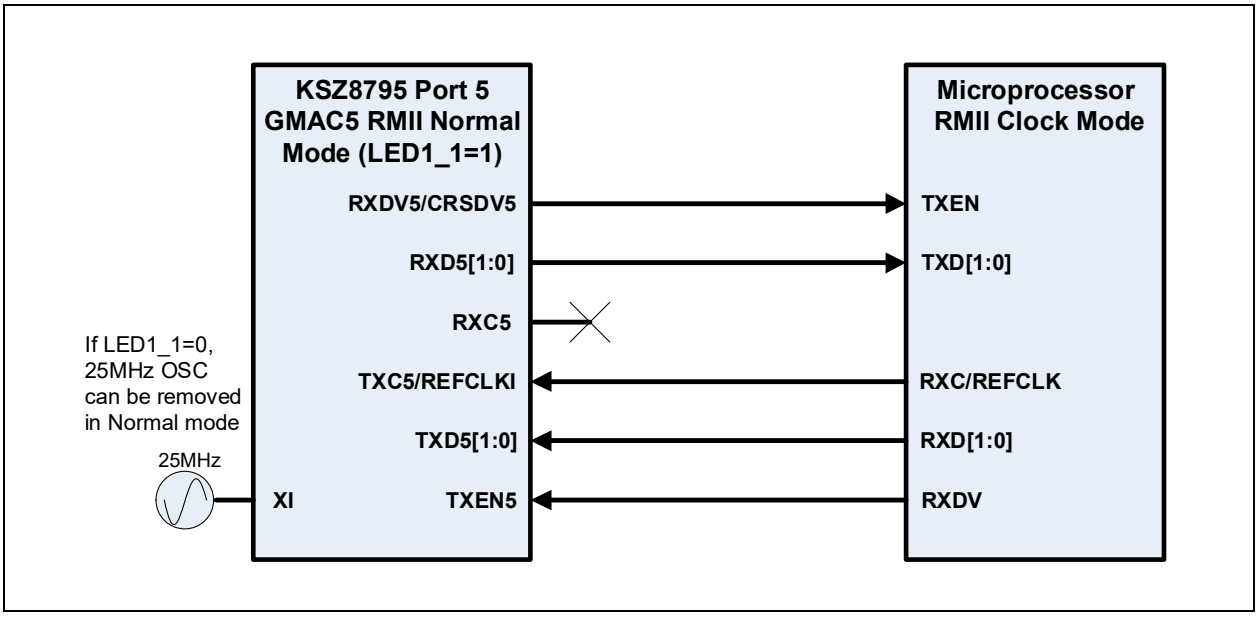
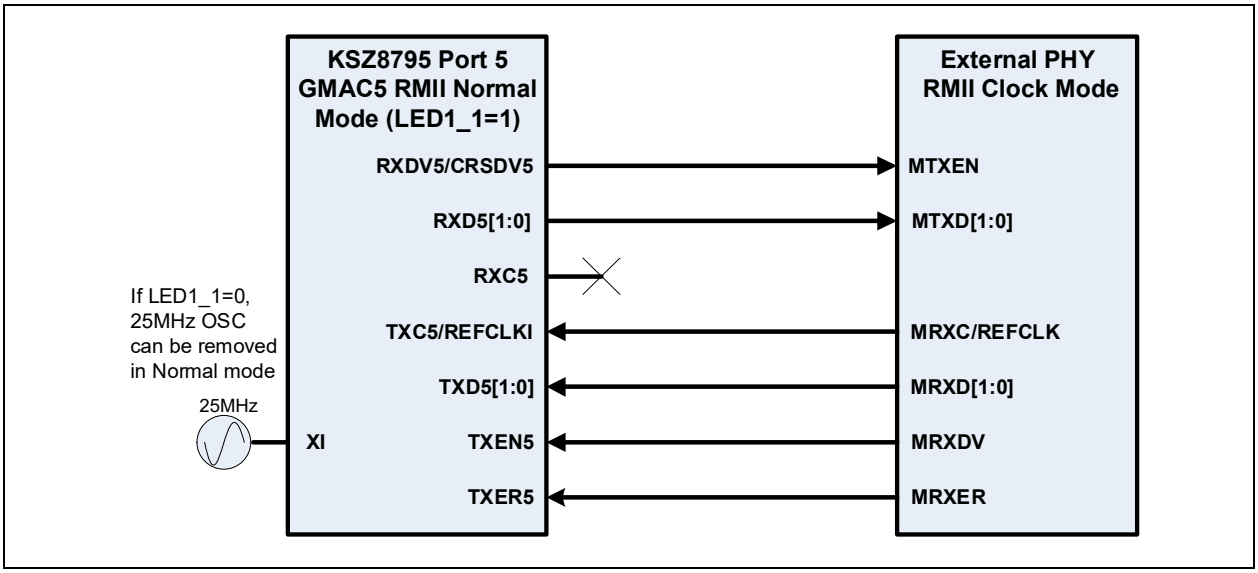


FIGURE 7-6: CONNECTIONS FOR KSZ8795CLX PORT 5 RMII NORMAL MODE AND EXTERNAL PHY RMII™ CLOCK MODE



7.4 Port 5 GMAC5 GMII Interface

- The KSZ8795CLX provides MAC layer interface for GMAC5. The GMII interface contains two distinct groups of signals: one for transmission and one for receiving. The KSZ8795CLX Port 5 GMAC5 GMII GMAC mode and GMAC5 GMII GPHY mode connections are shown in Figure 7-7 and Figure 7-8, respectively.
- Refer to Table 7-1 for the detailed configuration of the GMAC mode and GPHY mode of Port 5 GMAC5 SW5-GMII. The default mode is SW5-MII GMAC.
- KSZ8795CLX GMII supports 1000 Mb/s and Full-Duplex operation only.
- MCU GMAC GMII should have the same speed and duplex as the GMII interface.

FIGURE 7-7: CONNECTIONS BETWEEN KSZ8795CLX PORT 5 GMII GMAC MODE AND EXTERNAL GPHY MODE

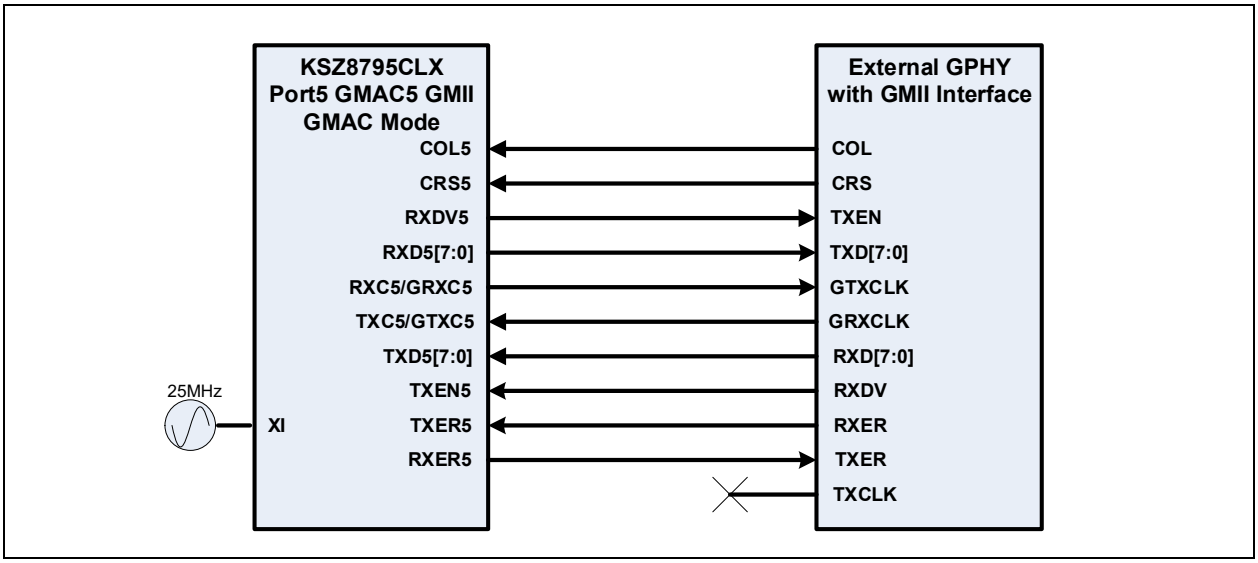
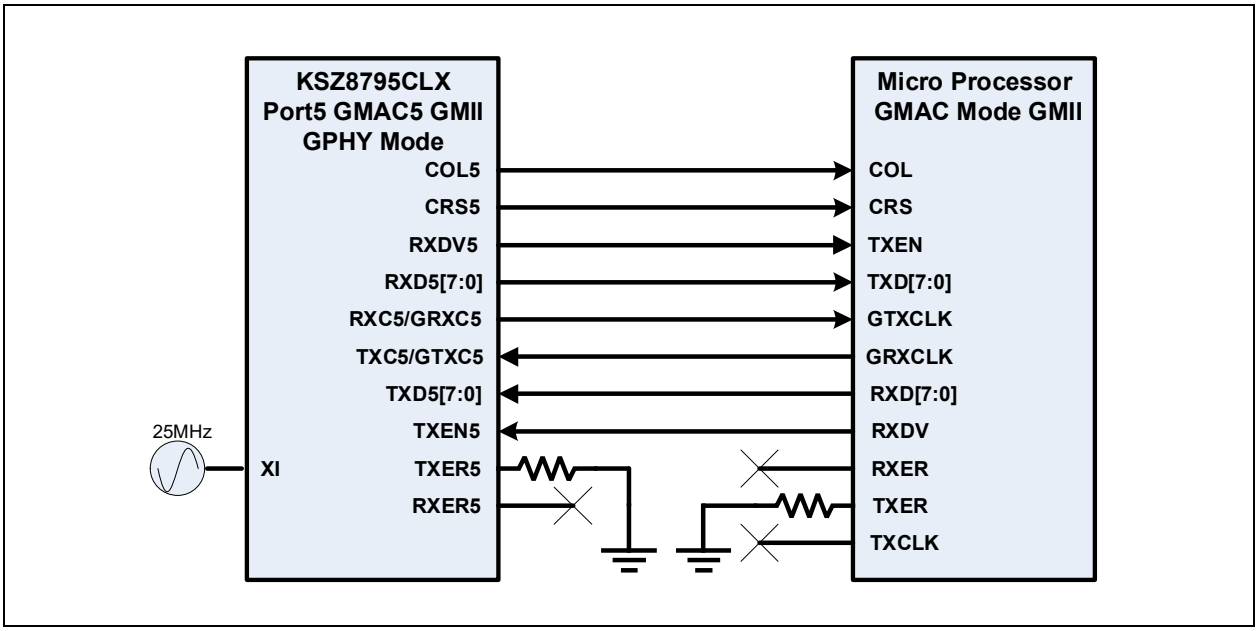


FIGURE 7-8: CONNECTIONS BETWEEN KSZ8795CLX PORT5 GMAC5 GMII GPHY MODE AND MCU GMII

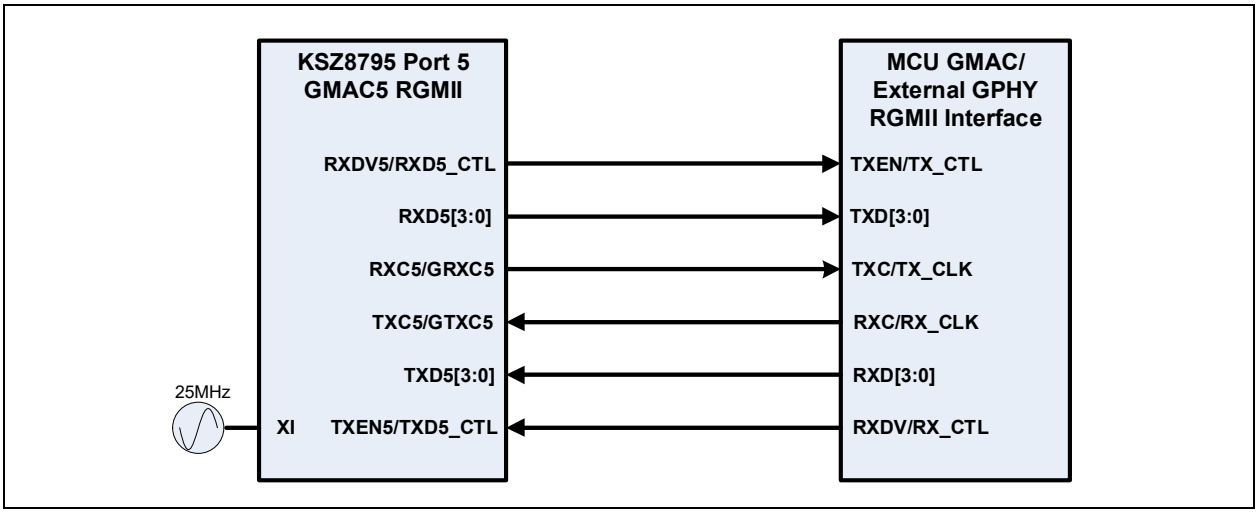


7.5 Port 5 GMAC5 RGMII Interface

The KSZ8795CLX provides GMAC layer RGMII interface for GMAC5. The RGMII interface contains two distinct groups of signals: one for transmission and one for receiving. The KSZ8795CLX Port5 GMAC5 RGMII connections are shown in Figure 7-9.

- Please see the Table 7-1 for the detailed configuration of the Port 5 GMAC5 SW5-RGMII.
- KSZ8795CLX RGMII supports 10/100/1000 Mbps. LED1_0=0 pull-down is 10/100 mode in RGMII, set register 0x06 bit [4] for 10/100 speed, and set bit [6] for Full-Duplex or Half-Duplex mode. LED1_0=1 in default is 1000Mbps mode, and it only supports Full-Duplex in the Gigabit mode.
- MCU GMAC RGMII should have the same speed and duplex as the RGMII interface.

FIGURE 7-9: CONNECTIONS BETWEEN KSZ8795CLX PORT 5 RGMII AND MCU GMAC/GPHY RGMII MODE



7.6 System Consideration for Design with RGMII Interface

- The KSZ8795CLX supports RGMII V2.0 specifications. The RMII interface need to meet Ingress Internal Delay (RGMII-IID) and Egress Internal Delay (RGMII-EID) specifications. In most cases, setting the KSZ8795CLX RGMII ID is required based on other end-RMII-ID to meet the RGMII V2.0 specifications. Note that using the SPI interface is the only way to set RGMII-ID. The KSZ8795 RGMII-ID setting principles are detailed in Table 7-2.
- KSZ8795CLX RGMII register setting is based on other end RGMII clock input/output clock delay and RGMII traces routing with equal length for two distinct groups of signals in PCB layout.

TABLE 7-2: PORT 5 GMAC5 RGMII REGISTER CONFIGURATION

KSZ8795CLX Register 86 Bits [4:3] Configuration	KSZ8795CLX RGMII Clock Input & Output Delay	KSZ8795CLX Register 86 (0x56)	KSZ8795CLX RGMII Clock Delay/ Slew Configuration	Other End RGMII Clock Configuration
Bit [4:3] = 11	Ingress Clock Input	Bit [4] = 1	Delay	No Delay
	Egress Clock Output	Bit [3] = 1	Delay	No Delay
Bit [4:3] = 10	Ingress Clock Input	Bit [4] = 1	Delay	No Delay
	Egress Clock Output	Bit [3] = 0	No Delay	Delay
Bit [4:3] = 01	Ingress Clock Input	Bit [4] = 0 (default)	No Delay	Delay
	Egress Clock Output	Bit [3] = 1 (default)	Delay	No Delay
Bit [4:3] = 00	Ingress Clock Input	Bit [4] = 0	No Delay	Delay

7.7 GMII/RGMII/MII/RMII™ Interface Series Terminations

- Provisions should be made for series resistors for all outputs on the MII/RMII™ interface. Series resistors will enable the designer to closely match the output driver impedance of the KSZ8795CLX and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. The recommended starting point for the value of these series resistors is 22Ω. See Table 7-3.

TABLE 7-3: SERIES TERMINATIONS FOR MII/RMII™ INTERFACE

Signals for Port5 GMAC5 GMII/ RGMII/MII/RMII	Series Resistors at KSZ8795CLX GMII/RGMII/MII/RMII Drive Pins	Series Resistors at the other end GMII/RGMII/MII/RMII Drive Pins
RXD5 [7:0] / RXD5 [3:0] / RXD5 [1:0]	22Ω	—
RXDV5 / CRSDV5/RXD5_CTL	22Ω	—
RXC5/GRXC5	22Ω in GMAC5 MII PHY mode, RMII Clock Mode and GMII/RGMII	22Ω when KSZ8795CLX GMAC5 is set to MII MAC mode.
TXC5/REFCLKI5/GTXC5	22Ω in GMAC5 MII PHY mode	22Ω when KSZ8795CLX GMAC5 is set to MII MAC mode, RMII Normal mode and GMII/RGMII mode.
TXEN/TXD5_CTL	—	22Ω
TXD5 [7:0] / TXD5 [3:0] / TXD5 [1:0]	—	22Ω

Note 1: The series resistors should be placed as close as possible to both KSZ8795CLX RMII drive pins and the other end drive pins in PCB layout.

2: The unused pins of the Port 5 GMAC5 interfaces should be unconnected except unused I/O pin without internal pull-up or pull-down.

8.0 MANAGEMENT INTERFACE

8.1 Configuration for Management Interface Mode

- KSZ8795CLX supports SPI Slave mode and MIIM-MDC/MDIO mode for register access. SPI mode can configure all registers, while MIIM-MDC/MDIO can configure all PHY-related registers.
- For strap pin 66 SPIQ, a pull-down resistor selects the SPI Slave mode for management operation. The recommended pull-down resistor value is 330Ω.
- For strap pin 66 SPIQ, a pull-up resistor selects the MIIM-MDC/MDIO mode for management operation. The recommended pull-up resistor value is 4.7 kΩ.

TABLE 8-1: REGISTER CONFIGURATION INTERFACE MODES

Pin Configuration	Serial Bus Configuration
SPIQ pin 66 pull-down	SPI Slave mode
SPIQ pin 66 pull-up	MIIM-MDC/MDIO mode

- Select one interface mode of SPI or MIIM-MDC/MDIO based on real application in the design.

8.2 Required External Pull-Ups

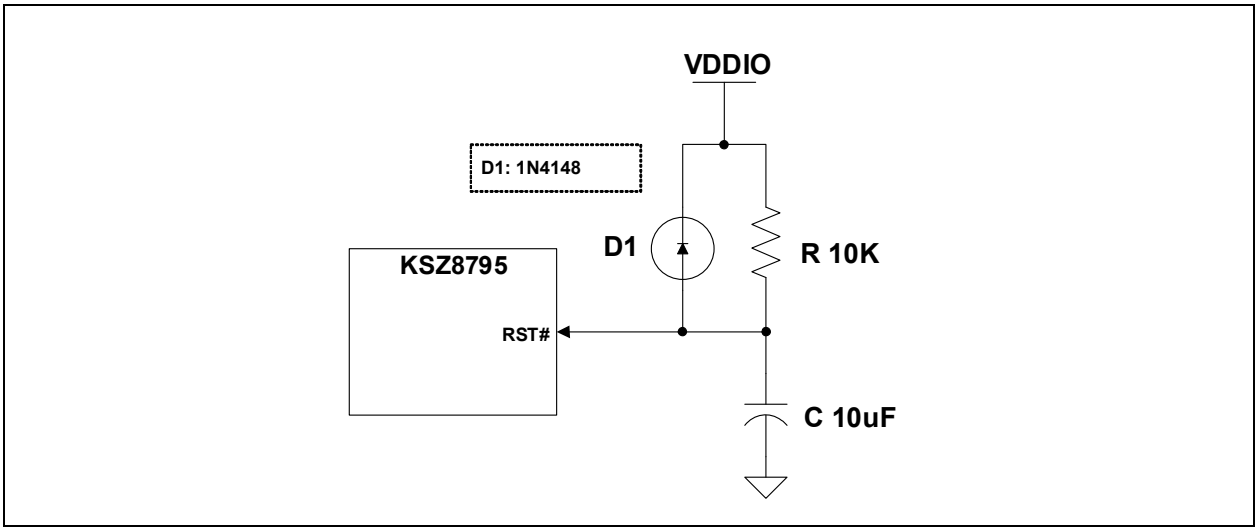
- The **INTR_N** (pin 23) requires a 4.7 kΩ external pull-up resistor because this output is an open-drain type.
- The **SDA_MDIO** (pin 68) requires a 4.7 kΩ external pull-up resistor.

9.0 STARTUP

9.1 Reset Circuit

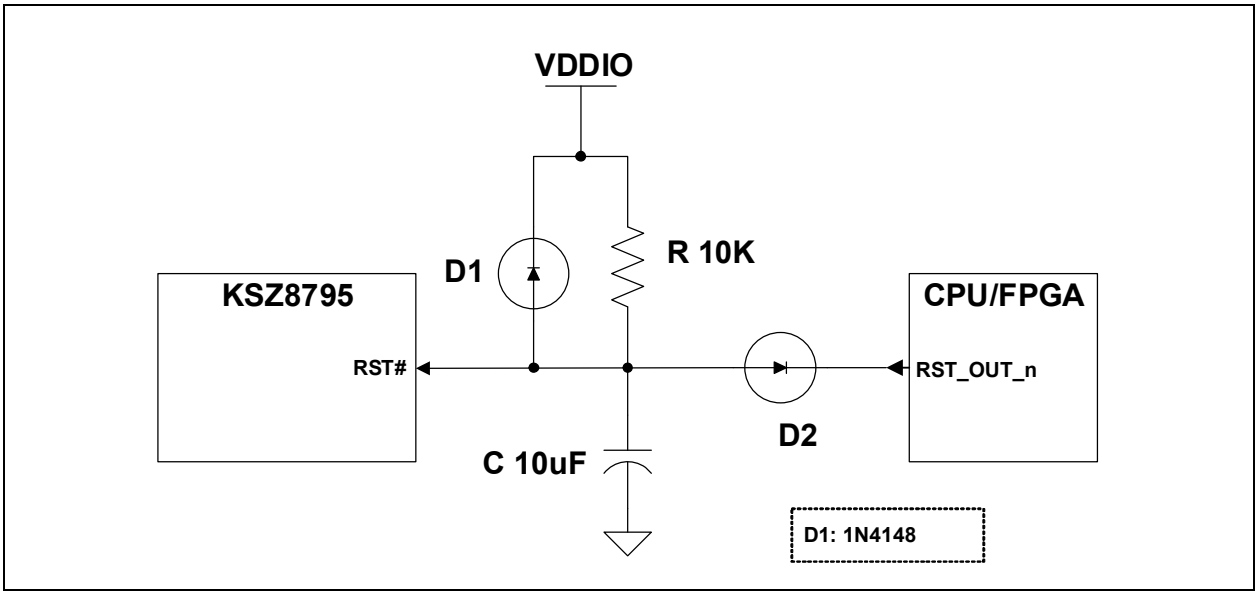
- The RST_N (pin 72) is an active-low RESET input. This signal resets all logic and registers within the KSZ8795-CLX. A hardware Reset (RST_N assertion) is required following power-up. Please refer to the latest copy of the KSZ8795CLX data sheet for reset timing requirements. Figure 9-1 shows a recommended reset circuit for powering up the KSZ8795CLX device when Reset is triggered by the power supply.

FIGURE 9-1: R/C RESET CIRCUIT FOR KSZ8795CLX POWER-UP RESET



- Reset circuit interface with CPU/FPGA RESET output pin shows the recommended Reset circuit for applications where Reset is driven by external CPU or FPGA. The RESET-out pin, RST_OUT_N, from CPU/FPGA provides the warm Reset after a power-up Reset is done. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be connected directly. See Figure 9-1.

FIGURE 9-2: RESET CIRCUIT INTERFACE WITH CPU/FGA RESET OUTPUT



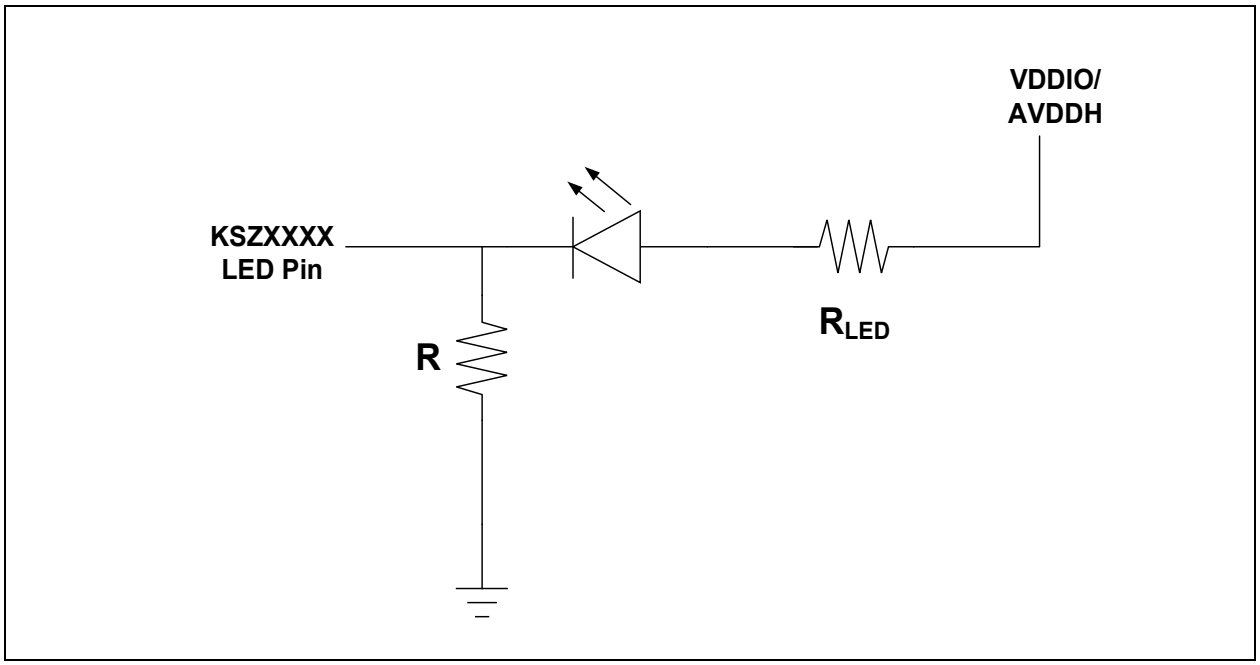
10.0 CONFIGURATION PINS (STRAPPING OPTIONS)

- There are some strap-in pins to help with the KSZ8795CLX configuration after power-up or hardware Reset. The KSZ8795CLX Data Sheet has complete details on the operation of strapping pins. The LED strap pin and other requirements are shown in the succeeding sections.

10.1 LED Pins as Strap-in Pins

- LED pins have internal pull-up resistors in KSZ8795CLX. Generally, LED pin does not typically need an external pull-up resistor for LED pin to be used for the Strap-high. However, LED Strap-low needs an external pull-down resistor R. See LED pin Strap-in circuit in Figure 10-1.

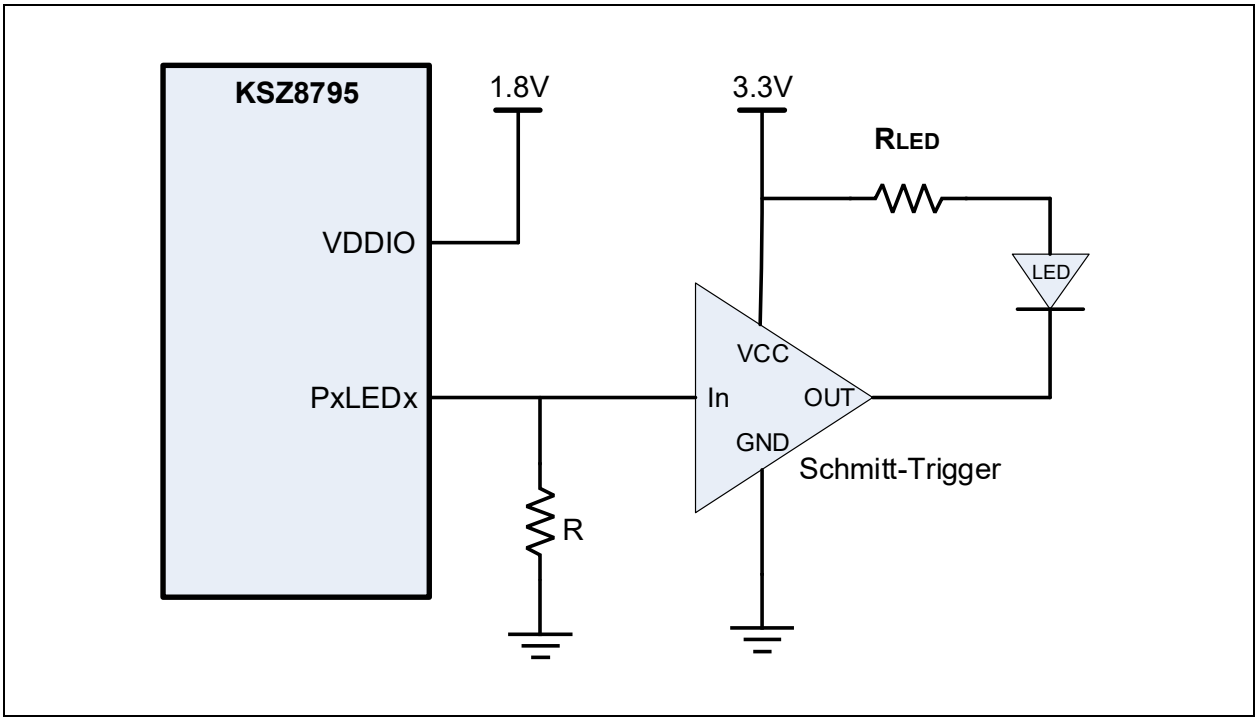
FIGURE 10-1: CONNECTIONS BETWEEN KSZ8795CLX PORT 5 GMII GMAC MODE AND EXTERNAL GPHY MODE



Based on the different VDDIO values in the experiment and testing, use the following recommended pull-down resistor R and the current limit resistor R_{LED} values:

- When using 3.3V VDDIO power, use 1 kΩ current limit resistor R_{LED} and 1 kΩ pull-down resistor R to meet V_{IL} specifications.
- When using 2.5V VDDIO power, use 1 kΩ current limit resistor R_{LED} and 0.75 kΩ pull-down resistor R to meet V_{IL} specifications.
- When using 1.8V VDDIO power, use 1 kΩ current limit resistor R_{LED} and 0.5 kΩ pull-down resistor R to meet V_{IL} specifications.
- The LED luminance with 1.8V VDDIO is preferred to be the same as 3.3V VDDIO, users may refer to the alternative LED circuit in Figure 10-2.

FIGURE 10-2: ALTERNATIVE LED CIRCUIT WITH 1.8V VDDIO



10.2 General Strap-in Pins and Others

- Except LED strap-in pins, the recommended pull-up and pull-down resistors values for strap pins are 4.7 kΩ and 1 kΩ, respectively. Users are highly discouraged from directly executing a pull-up to power and pull-down to ground without pull-up and pull-down resistors.

11.0 MISCELLANEOUS

11.1 ISET Resistor

- The **ISET** pin (pin 77) on the KSZ8795CLX should connect to the system ground through a 12.4 kΩ resistor with a tolerance of 1.0%. This **ISET** pin is used to set up critical bias currents for the embedded 10/100 Ethernet physical devices.

11.2 Other Considerations

- Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor/ferrite bead far away from KSZ8795CLX device in PCB layout placement for better ESD.
- Make sure that enough bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail.

12.0 HARDWARE CHECKLIST SUMMARY

TABLE 12-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.0, "Power"	To meet Figure 3-1 requirements, check all power pins of analog 3.3V **VDDAT** pins, digital **VDDIO** pins, analog 1.2V **VDD12D** pins, and analog 1.2V **VDD12A** pin for the decouple capacitors, bulk capacitors, and ferrite beads.		
Section 4.0, "Ethernet Signals"	Section 4.1, "KSZ8795CLX Copper Port Connection"	Verify if there is no 49.9Ω termination resistors on **TX** and **RX** pairs.		
	Section 4.2, "Magnetics Connection at the Chip Side"	Verify if the center taps of the magnetics on the KSZ8795CLX chip side are NOT connected to the **VDDAT** 3.3V analog power as KSZ8795CLX is an internal biasing device. The center taps of the magnetics on the chip side should also have two 0.1 µF capacitors to ground individually.		
	Section 4.3, "Magnetics Connection at Line Side of the RJ45 Connector"	Verify if the line side of the magnetics has two 75Ω resistors through a 1000 pF, 2 kV capacitor connected to chassis ground that is also linked to the metal case of the RJ45 on the line side.		
	Section 4.4, "Alternative Termination Selection for RJ45 Connector"	If using smith termination for unused pins 4/5 and 7/8 of the RJ45 connector, check if these pins are terminated to chassis ground through a 1000 pF, 2 KV capacitor.		
	Section 4.5, "Using RJ45 with Integrated LED"	Use RJ45 with integrated LED if the product working environment is not very noisy. Otherwise, use an independent LED solution.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections"	Verify the usage of 25 MHz maximum ±50 ppm crystal. The drive level should be about 100 µW or above (preferably higher). If using a 25 MHz oscillator with maximum ±50 ppm, it is better to use a 3.3V power oscillator and 3.3V VDDAT for the oscillator power.		
Section 6.0, "Configuration for System Application"	Section 6.1, "Design for Simple Standalone 4 Port Switch"	Check if the switch Port 5 is set to RMII™ Normal mode with clock source coming from crystal/oscillator.		
	Section 6.2, "Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 GMII"	If uplink Port 5 uses GMII mode, make sure that the configuration strap pins are set correctly.		
	Section 6.3, "Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 RGMII"	If uplink Port 5 uses RGMII mode, make sure that the configuration strap pins are set correctly.		
	Section 6.4, "Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 MII"	If uplink Port 5 uses MII mode, make sure that the configuration strap pins are set correctly.		
	Section 6.5, "Design for Managed 5-Port Switch using Uplink Port 5 GMAC5 RMII™"	If uplink Port 5 uses RMII™ mode, make sure that the configuration strap pins are set correctly.		
	Section 6.6, "Design for Unmanaged Non-Blocking 8-Port Switch using RGMII Back-to-Back"	If using two KSZ8795CLX devices for a non-blocking 8-port 10/100 Ethernet switch, make sure to use the RGMII mode with the correct connections.		

TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Digital Interface"	Section 7.1, "Port 5 GMAC5 SW5-GMII/ RGMII/MII/RMII™ Strap Pins for Configuration"	If using one mode of GMII/RGMII/MII/RMII on Port 5, check or design the configuration correctly based on Table 7-1.		
	Section 7.2, "Port 5 GMAC5 MII Interface"	For Port 5 GMAC5 MII with other end MII connections, make sure that the input and output connections are correct.		
		If connected between KSZ8795CLX GMAC5 MAC mode MII and external PHY MII, check the connections based on Figure 7-1.		
		If connected between KSZ8795CLX GMAC5 PHY mode MII and MCU MAC MII, check the connections based on Figure 7-2.		
	Section 7.3, "Port 5 GMAC5 RMII™ Interface"	Make sure that the RMII mode strap-in configuration is correct based on Table 7-1.		
	Section 7.3.1, "Port 5 GMAC5 RMII™ Clock Mode"	For Port 5 RMII with other end-RMII connections, make sure that the input and output connections are correct.		
		If connected between KSZ8795CLX GMAC5 RMII Clock mode and MCU RMII Normal mode, check the connections based on Figure 7-3.		
		If connected between KSZ8795CLX GMAC5 RMII Clock mode and external PHY RMII Normal mode, check the connections based on Figure 7-4.		
	Section 7.3.2, "Port 5 MAC5 RMII™ Normal Mode"	For Port 5 RMII with other end RMII connections, make sure that the input and output connections are correct.		
		If connected between KSZ8795CLX GMAC5 RMII Normal mode and MCU RMII Clock mode, check the connections based on Figure 7-5.		
		If connected between KSZ8795CLX GMAC5 RMII Normal mode and external PHY RMII Clock mode, check the connections based on Figure 7-6.		
	Section 7.4, "Port 5 GMAC5 GMII Interface"	For Port 5 GMAC5 GMII with other end GMII connection, make sure that the input and output connections are correct.		
		If connected between KSZ8795CLX GMAC5 GMAC mode GMII and external GPHY GMII, check the connections based on Figure 7-7.		
		If connected between KSZ8795CLX GMAC5 GPHY mode GMII and MCU GMAC GMII, check the connections based on Figure 7-8.		
	Section 7.5, "Port 5 GMAC5 RGMII Interface"	For Port 5 GMAC5 RGMII with other end-RGMII connections, make sure that the input and output connections are correct.		
		If connected between KSZ8795CLX GMAC5 RGMII and MCU GMAC RGMII (or external GPHY RGMII), check connections based on Figure 7-9.		
	Section 7.6, "System Consideration for Design with RGMII Interface"	Consider RGMII-ID in RGMII specifications. The SPI access should be design-in if using Port 5 GMAC5 RGMII interface.		
	Section 7.7, "GMII/RGMII/MII/RMII™ Interface Series Terminations"	Check if all drive pins have the series termination resistors for the digital I/O interface.		

TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Management Interface"	Section 8.1, "Configuration for Management Interface Mode"	Always remember that a pull-down resistor is required on the SPIQ pin 66 when using the SPI mode.		
		Always remember that a pull-up resistor is required on the SPIQ pin 66 when using the MDC/MDIO mode.		
	Section 8.2, "Required External Pull-Ups"	Check if there is a pull-up resistor for the data line of the management interface and the interrupt pin if they are used. Use a 4.7 kΩ pull-up resistor.		
Section 9.0, "Startup"	Section 9.1, "Reset Circuit"	Verify if the R/C reset circuit is used for a power-up reset. A 10 kΩ resistor and a 10 µF capacitor are recommended. For the cost-down, the D1 Figure 9-1 and Figure 9-2 can be ignored because the RST_N pin has an internal protection diode. For a warm Reset from CPU/FPGA to KSZ8795CLX, D2 can be removed from Figure 9-2 if the KSZ8795CLX and CPU/FPGA are using the same VDDIO voltage.		
Section 10.0, "Configuration Pins (Strapping Options)"	Section 10.1, "LED Pins as Strap-in Pins"	If using an LED pin to do a strap-in for the different VDDIO design, follow the specified recommended resistor value for the pull-down resistors and the current limit resistor to meet V_{IL} specifications. If the LED strap pin is for pull-up, an external pull-up resistor is unnecessary because KSZ8795CLX LED pins have internal pull-up by default.		
	Section 10.2, "General Strap-in Pins and Others"	It is generally recommended to use 4.7 kΩ pull-up and 1 kΩ pull-down resistors. Avoid pulling up or down to power or ground directly. If not specified, the NC pin should be a no-connect.		
Section 11.0, "Miscellaneous"	Section 11.1, "ISET Resistor"	Check ISET resistor (12.4 kΩ, 1%) without any capacitor in parallel.		
	Section 11.2, "Other Considerations"	Incorporate an SMD footprint (SMD_0805-1210) to connect the chassis ground to the system ground. The SMD footprint should be placed far from the devices in PCB layout.		
		Incorporate sufficient power plane bulk capacitors (4.7 µF to 22 µF) for each power rail.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003579A (08-14-20)	Initial release	

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