AN1903

Configuration Options for USB5734, USB5744, and USB5742

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1.0 INTRODUCTION

The USB5734/USB5744/USB5742 can be configured via:

- SMBus during start-up configuration stage (SOC_CFG)
- SMBus during hub operational stages (during runtime)
- One-Time Programmable (OTP) memory
- A USB interface during hub operational stages (during runtime)
- An external Serial Peripheral Interface (SPI) Flash

SMBus Configuration: The hub may be configured via the SMBus slave interface during the hub's start-up configuration stage (or SOC_CFG). To hold the hub in the SOC_CFG stage, the CONFIG_STRAP pins must be set with the correct configuration mode (CONFIG1 for USB5734/USB5744/USB5742) and the SMBus slave clock and data pins must be sampled as 'high' (10k pull-up resistors to 3.3V recommended) at power-on or when RESET_N is deasserted. Once in the configuration stage, any of the registers may be reconfigured. The hub waits in SOC_CFG indefinitely until it receives the special Attach command.

After the hub has exited the SOC_CFG stage, the configuration registers may still be manipulated via SMBus. This may be useful for enabling an external SOC to control the hub's GPIOs or to check certain hub status registers.

OTP Memory: The hub's registers may be configured via the hub's internal OTP memory. Any register may be given a new default value. The OTP memory is 8 kB, and each bit within the OTP memory may be set once, but never cleared. The OTP commands are loaded sequentially, so it is possible to overwrite a previously programmed register setting by programming that register subsequently with a new value. The OTP memory may be programmed via the USB interface or via SMBus.

USB Interface: All registers are accessible from the USB host using vendor-specific commands issued to the hub's internal Hub Feature Controller (HFC) device.

External SPI Memory Device: If a custom firmware image is being used and executed from an attached SPI memory device, the configuration registers may also be configured within the SPI image. This method mimics the OTP configuration method and is referred to as "pseudo-OTP."

1.1 Sections

Section 2.0, General Information
Section 3.0, Accessing Configuration Registers
Section 4.0, Configuration Registers
Section 5.0, Using GPIOs
Section 6.0, OTP Configuration
Section 7.0, Hub Product IDs
Section 8.0, Physical and Logical Port Mapping

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1.2 References

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *USB5734 Data Sheet*
- *USB5744 Data Sheet*
- *USB5742 Data Sheet*
- *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

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2.0 GENERAL INFORMATION

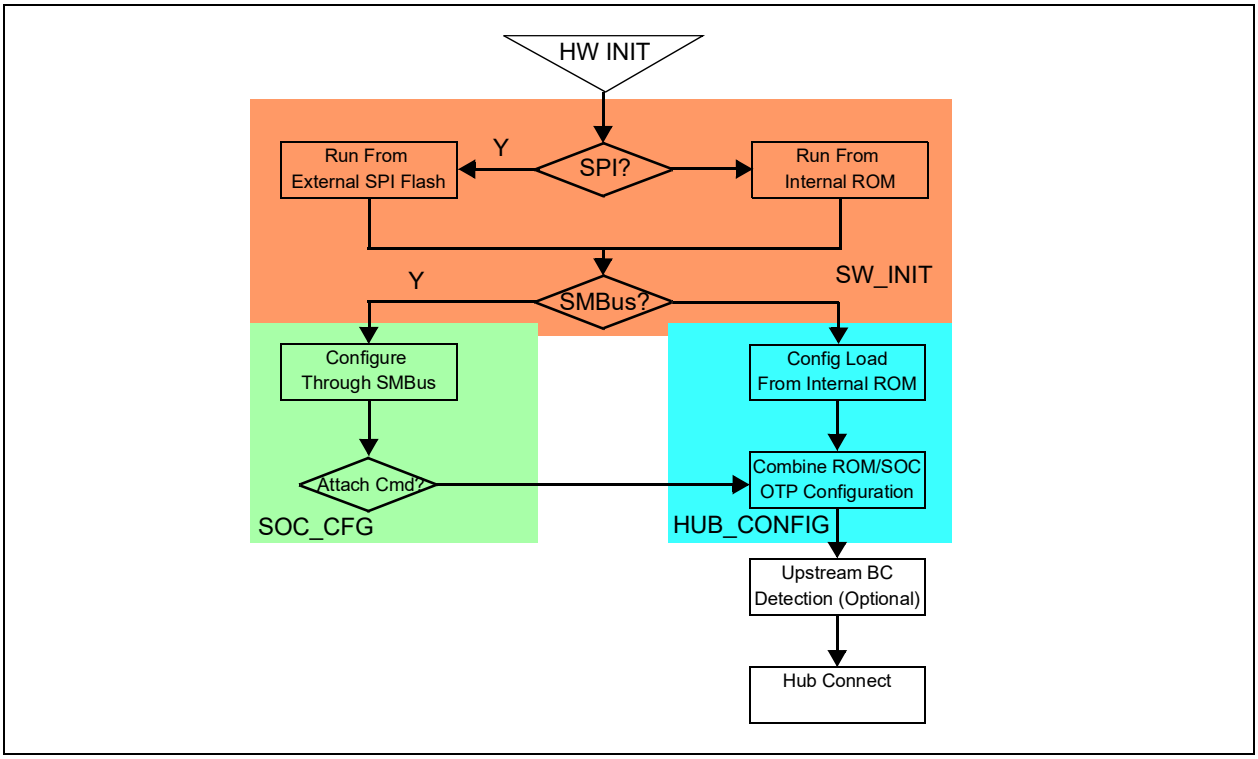
2.1 Hub Configuration Stages

The Controller Hub is configured in three stages:

1. SOC Configuration Stage, which is executed through the SMBus interface
2. Hub Configuration Stage through internal OTP registers
3. Hub Connect Stage

Figure 1 shows how these stages flow:

FIGURE 1: HUB OPERATIONAL MODE FLOWCHART



Note: Because the OTP Configuration registers are loaded after the SOC_CFG stage, it is possible for configuration registers modified in the SOC_CFG stage to be overwritten in the HUB_CONFIG stage.

2.2 SMBus Protocol

The SMBus protocol is a flexible, 2-pin serial protocol used for low-speed communication between integrated circuits. The protocol consists of a SMBCLK pin generated by the SMBus master and a bi-directional SMBDATA pin that can be driven by a master or a slave. In order for the SMbus interface to function, the bus requires a pull-up resistor on both SMBCLK and SMBDATA. The hub configures the pins as Open/Drain buffers where the driver will either tri-state the pin or drive the pin to GND. SOCs operating and 3.3V-2.5V are supported; the input high-level threshold is 1.5V. Refer to the System Management Bus Specification for more details on the timing specifications of the bus.

2.3 SOC Configuration Stage

The SOC Configuration Stage is the first stage of activity on the SMBus interface. In this stage, the SOC may modify any of the configuration settings to customize the hub to specific applications. The SOC may configure the hub as Full-Speed only, or have the hub report a port as non-removable. The SOC can also disable a port entirely to conserve power. During the SOC Configuration Stage, the hub is addressed at 2Dh.

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2.3.1 RUNTIME

The hub can also be configured during runtime after enumeration. During runtime, the hub is also addressed at 2Dh.

2.3.2 SMBUS BLOCK WRITE

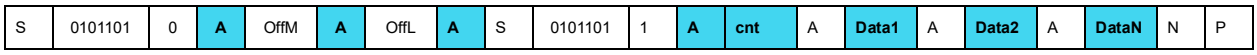
The SMBus block write consists of an Address+Direction(0) byte followed by the 16-bit memory address, split into two bytes. The address is used for special commands as well as a pointer to the hub's internal memory. After the address, the next byte of data is the count of data bytes that will follow, up to 128 bytes in a block. Finally, a write of 00h is used to terminate the write operation followed by the SMBus stop signal.

FIGURE 2: SMBUS BLOCK WRITE

2.3.3 SMBUS BLOCK READ

The SMBus block read consists of an Address+Direction(0) byte with the 16-bit memory address followed by a repeat Start signal and an Address+Direction(1) byte. The hub then starts to output the count (128 bytes) and the contents of the internal registers starting at the 16-bit address specified.

FIGURE 3: SMBUS BLOCK READ



2.3.4 SPECIAL COMMANDS

There are special commands that can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the configuration registers, or reset the device. The commands consist of the 16-bit command, followed by a 00h byte to terminate the command.

TABLE 1: SPECIAL SMBUS COMMANDS

Operation	Opcode	Description
Reboot	9936h	Reset Device
USB Attach	AA55h	Exit Configuration Stage and Begin Enumeration
USB Attach with SMBus	AA56h	Attach with the SMBus still active in Runtime **Note:** If this command is used, the BYPASS_UDC_SUSPEND bit in register 411Dh must be set to ensure that the MCU is always enabled and ready to respond to SMBus runtime commands.
Configuration Register Access Command	9937h	Read and Write Configuration Registers
OTP Write Command	9933h	Write OTP commands to the OTP memory space
OTP Read Command	9934h	Read the contents of the OTP memory space

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3.0 ACCESSING CONFIGURATION REGISTERS

The Configuration Register Access command allows the SMBus master to read or write to the internal registers of the hub. When the Configuration Register Access command is sent, the hub interprets the memory starting at offset 00h as follows:

TABLE 2: MEMORY FORMAT FOR CONFIGURATION REGISTER ACCESS

Ram Address	Description	Notes
0000h	Direction	0 = Register Write, 1 = Register Read
0001h	Configuration Address MSB	Number of bytes to read/write when executing the command
0002h	Configuration Address LSB	The upper byte of the 16-bit configuration register address
0003h	Configuration Address LSB	The lower byte of the 16-bit configuration register address
0004h	Data1	The first byte of data to write to or read from the configuration address
...	...	...
0004h+N	DataN	The Nth byte of data to write to or read from the configuration address N is equal to the data length.

3.1 Configuration Register Write Example

The following example shows how the SMBus messages are formatted to set the Vendor ID (VID) of the hub to a custom value, AA55h.

1. Write data to the memory of the hub.

TABLE 3: EXAMPLE SMBUS WRITE COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	00h	Memory address **00**00h
2	00h	Memory address 00**00**h
3	06h	Number of bytes to write to memory
4	00h	Write configuration register
5	02h	Writing two data bytes
6	30h	VID is in register **30**00h.
7	00h	VID is in register 30**00**h.
8	AAh	LSB of Vendor ID is **AA**55h.
9	55h	MSB of Vendor ID is AA**55**h.

2. Execute the Configuration Register Access command.

TABLE 4: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command completion

3.2 Configuration Register Read Example

The following example shows how to read the Charger Detection register to determine what type of charger the hub has connected to:

1. Write data to the memory of the hub.

TABLE 5: EXAMPLE SMBUS WRITE COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	00h	Memory address **00**00h
2	00h	Memory address 00**00**h
3	04h	Number of bytes to write to memory
4	01h	Read configuration register
5	01h	Reading one data byte
6	30h	BC Detect is in register **30**E2h.
7	E2h	BC Detect is in register 30**E2**h.

2. Execute the Configuration Register Access command.

TABLE 6: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command completion

3. Read back the data starting at memory offset 04h, which is where the Data byte starts.

TABLE 7: EXAMPLE SMBUS READ COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	00h	Memory address **00**04h
2	04h	Memory address 00**04**h
3	5Bh	Address plus read bit
4	80h	Device sends 128 bytes of data.
5	56h	Charging downstream port detect

Note: Although the device can send out 128 bytes of memory data, it is not necessary to read the entire set. The SMBus master can send a stop at any time.

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4.0 CONFIGURATION REGISTERS

Table 8 shows a list of the configuration registers and their addresses. The default column displays the values that will be loaded if the register is not modified during the configuration stage.

Note: Port 3 and 4 related registers and configuration bits are not applicable to the USB5742 (2-port device).

TABLE 8: CONFIGURATION REGISTER MEMORY MAP

Addr	R/W	Name	Function	Modification Stage	Default
0800h	R	DEV_REV	Device Revision Register	Configuration	see reg.
082Fh	R/W	GPIO_1_7_PD	GPIO 1-7 Pull-Down Register (Note 4-1)	Configuration or Runtime	00h
082Eh	R/W	GPIO_8_11_PD	GPIO 8-11 Pull-Down Register (Note 4-1)	Configuration or Runtime	00h
082Dh	R/W	GPIO_16_20_PD	GPIO 17-20 Pull-Down Register (Note 4-1)	Configuration or Runtime	00h
0833h	R/W	GPIO_1_7_DIR	GPIO 1-7 Direction Control Register (Note 4-1)	Configuration or Runtime	00h
0832h	R/W	GPIO_8_11_DIR	GPIO 8-11 Direction Control Register (Note 4-1)	Configuration or Runtime	00h
0831h	R/W	GPIO_16_20_DIR	GPIO 17-20 Direction Control Register (Note 4-1)	Configuration or Runtime	00h
0837h	R/W	GPIO_1_7_OUT	GPIO 1-7 Output Register (Note 4-1)	Configuration or Runtime	00h
0836h	R/W	GPIO_8_11_OUT	GPIO 8-11 Output Register (Note 4-1)	Configuration or Runtime	00h
0835h	R/W	GPIO_16_20_OUT	GPIO 17-20 Output Register (Note 4-1)	Configuration or Runtime	00h
083Bh	R/W	GPIO_1_7_IN	GPIO 1-7 Input Register (Note 4-1)	Configuration or Runtime	00h
083Ah	R/W	GPIO_8_11_IN	GPIO 8-11 Input Register (Note 4-1)	Configuration or Runtime	00h
0839h	R/W	GPIO_16_20_IN	GPIO 17-20 Input Register (Note 4-1)	Configuration or Runtime	00h
083Fh	R/W	GPIO_1_7_PU	GPIO 1-7 Pull-Up Register (Note 4-1)	Configuration or Runtime	00h
083Eh	R/W	GPIO_8_11_PU	GPIO 8-11 Pull-Up Register (Note 4-1)	Configuration or Runtime	00h
083Dh	R/W	GPIO_16_20_PU	GPIO 17-20 Pull-Up Register (Note 4-1)	Configuration or Runtime	00h
0900h	R/W	USB2_OCS_STAT	USB 2.0 OCS Status Register	Runtime	00h
0902h	R/W	USB3_OCS_STAT	USB 3.1 Gen 1 OCS Status Register	Runtime	00h
3000h	R/W	USB2_VIDL	USB 2.0 Hub Vendor ID LSB (Note 4-2)	Configuration	24h
3001h	R/W	USB2_VIDM	USB 2.0 Hub Vendor ID MSB (Note 4-2)	Configuration	04h
3002h	R/W	USB2_PIDL	USB 2.0 Hub Product ID LSB	Configuration	Note 4-3
3003h	R/W	USB2_PIDM	USB 2.0 Hub Product ID MSB	Configuration	27h
3004h	R/W	USB2_DIDL	USB 2.0 Hub Device ID LSB	Configuration	Note 4-4
3005h	R/W	USB2_DIDM	USB 2.0 Hub Device ID MSB	Configuration	Note 4-4
3006h	R/W	CFG1	USB 2.0 Hub Configuration 1	Configuration	9Bh

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TABLE 8: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

Addr	R/W	Name	Function	Modification Stage	Default
3007h	R/W	CFG2	USB 2.0 Hub Configuration 2	Configuration	28h
3008h	R/W	CFG3	USB 2.0 Hub Configuration 3	Configuration	09h
3009h	R/W	USB2_NRD	USB 2.0 Hub Non-Removable Device (Note 4-5)	Configuration	20h
300Ah	R/W	PDS	USB 2.0 Port Disable (Self-Powered)	Configuration	Note 4-6
300Bh	R/W	PDB	USB 2.0 Port Disable (Bus-Powered)	Configuration	Note 4-6
3013h	R/W	MFR_STR_INDEX	USB 2.0 Hub Manufacturer String Index	Configuration	01h
3014h	R/W	PRD_STR_INDEX	USB 2.0 Hub Product String Index	Configuration	02h
3015h	R/W	SER_STR_INDEX	USB 2.0 Hub Serial String Index	Configuration	00h
30FAh	R/W	PRTSP	USB 2.0 DP/DM Port Swap	Configuration	00h
30FBh	R/W	USB2_PRT_EN_12	USB 2.0 Port 1/Port 2 Disable (Note 4-7)	Configuration	21h
30FCh	R/W	USB2_PRT_EN_34	USB 2.0 Port 3/Port 4 Disable (Note 4-7)	Configuration	Note 4-8
30FDh	R/W	USB2_HC_EN	USB 2.0 Hub Controller Disable (Note 4-7)	Configuration	00h
3100h	R	USB2_LINK_STATE1	USB 2.0 Link State Ports 0 ~ 3	Runtime	FCh
3101h	R	USB2_LINK_STATE2	USB 2.0 Link State Port 4	Runtime	0Fh
3104h	R/W	USB2_HUB_CTL	USB 2.0 Hub Control	Configuration	00h
318Eh	R/W	CONNECT_CFG	Connect Configuration Register	Runtime	00h
3840h	R/W	USB3_HUB_CTL	USB 3.1 Gen 1 Hub Control	Runtime	20h
3870h	R/W	LINK_PWR_STATE1	USB 3.1 Gen 1 Link Low Power State 1	Runtime	AAh
3874h	R/W	LINK_PWR_STATE2	USB 3.1 Gen 1 Link Low Power State 2	Runtime	02h
3C00h	R/W	USB3_PRT_CFG_SEL1	USB 3.1 Gen 1 Port 1 Configuration Select (Note 4-7)	Configuration	93h
3C04h	R/W	USB3_PRT_CFG_SEL2	USB 3.1 Gen 1 Port 2 Configuration Select (Note 4-7)	Configuration	83h
3C08h	R/W	USB3_PRT_CFG_SEL3	USB 3.1 Gen 1 Port 3 Configuration Select (Note 4-7)	Configuration	Note 4-9
3C0Ch	R/W	USB3_PRT_CFG_SEL4	USB 3.1 Gen 1 Port 4 Configuration Select (Note 4-7)	Configuration	Note 4-9
3C20h	R/W	OCS_SEL1	Port 1 Overcurrent Sense Source Select	Configuration	01h
3C24h	R/W	OCS_SEL2	Port 2 Overcurrent Sense Source Select	Configuration	01h
3C28h	R/W	OCS_SEL3	Port 3 Overcurrent Sense Source Select	Configuration	01h
3C2Ch	R/W	OCS_SEL4	Port 4 Overcurrent Sense Source Select	Configuration	01h
411Ah	R/W	FLEX_CFG1	FlexConnect Configuration 1	Configuration or Runtime	00h
411Bh	R/W	FLEX_CFG2	FlexConnect Configuration 2	Configuration or Runtime	00h
411Dh	R/W	RUNTIMEFLAGS2	Runtime Flags 2	Configuration	00h
4130h	R/W	OTPFORCEUDCENABLE	Hub Feature Controller Enable	Configuration	00h
413Ch	R/W	BC_CFG_P1	Battery Charging Port 1 Configuration	Configuration	00h
413Dh	R/W	BC_CFG_P2	Battery Charging Port 2 Configuration	Configuration	00h

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TABLE 8: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

Addr	R/W	Name	Function	Modification Stage	Default
413Eh	R/W	BC_CFG_P3	Battery Charging Port 3 Configuration	Configuration	00h
413Fh	R/W	BC_CFG_P4	Battery Charging Port 4 Configuration	Configuration	00h
4140h	R/W	CDCENUMCONTROL	CDC Device Enumeration Control	Configuration	00h
4194h-4214h	R/W	HFC_STRING_CONT	Hub Feature Controller String Container	Configuration	see reg.
426Dh-4272h	R/W	USB2_STR_INDX1_PNTR	USB2 String Index 1 Pointer	Configuration	see reg.
4273h-4278h	R/W	USB2_STR_INDX2_PNTR	USB2 String Index 2 Pointer	Configuration	see reg.
4279h-427Eh	R/W	USB2_STR_INDX3_PNTR	USB2 STRING Index 3 Pointer	Configuration	see reg.
42D0h	R/W	HFC_BCDUSBL	HFC bcdUSB LSB	Configuration	01h
42D1h	R/W	HFC_BCDUSBH	HFC bcdUSB MSB	Configuration	02h
42D6h	R/W	HFC_VIDL	HFC Vendor ID LSD	Configuration	24h
42D7h	R/W	HFC_VIDM	HFC Vendor ID MSB	Configuration	04h
42D8h	R/W	HFC_PIDL	HFC Product ID LSB	Configuration	Note 4-3
42D9h	R/W	HFC_PIDM	HFC Product ID MSB	Configuration	Note 4-3
42DAh	R/W	HFC_DIDL	HFC Device ID LSB	Configuration	see reg.
42DBh	R/W	HFC_DIDM	HFC Device ID MSB	Configuration	see reg.
42DCh	R/W	HFC_MFR_STR_INDEX	HFC Manufacturer String Index	Configuration	02h
42DDh	R/W	HFC_PRD_STR_INDEX	HFC Product String Index	Configuration	03h
42DEh	R/W	HFC_SER_STR_INDEX	HFC Serial String Index	Configuration	00h
4329h-43A6h	R/W	USB2_STRING_CONT	USB2 Hub String Container	Configuration	see reg.
4418h-441Bh	R/W	USB3_STR_INDX1_PNTR	USB2 String Index 1 Pointer	Configuration	see reg.
441Ch-441Fh	R/W	USB3_STR_INDX2_PNTR	USB2 String Index 2 Pointer	Configuration	see reg.
4420h-4423h	R/W	USB3_STR_INDX3_PNTR	USB2 STRING Index 3 Pointer	Configuration	see reg.
4440h	R/W	USB3_BCDUSBL	USB 3.1 Gen 1 Hub bcdUSB LSB	Configuration	02h
4441h	R/W	USB3_BCDUSBM	USB 3.1 Gen 1 Hub bcdUSB MSB	Configuration	03h
4448h	R/W	USB3_VIDL	USB 3.1 Gen 1 Hub Vendor ID LSB (Note 4-2, Note 4-10)	Configuration	24h
4449h	R/W	USB3_VIDM	USB 3.1 Gen 1 Hub Vendor ID MSB (Note 4-2, Note 4-10)	Configuration	04h
444Ah	R/W	USB3_PIDL	USB 3.1 Gen 1 Hub Product ID LSB (Note 4-10)	Configuration	Note 4-3
444Bh	R/W	USB3_PIDM	USB 3.1 Gen 1 Hub Product ID MSB (Note 4-10)	Configuration	57h
444Ch	R/W	USB3_DIDL	USB 3.1 Gen 1 Hub Device ID LSB (Note 4-10)	Configuration	Note 4-4
444Dh	R/W	USB3_DIDM	USB 3.1 Gen 1 Hub Device ID MSB (Note 4-10)	Configuration	Note 4-4
444Eh	R/W	USB3_HUB_MFR_STR_INDEX	USB 3.1 Gen 1 Manufacturer String Index	Configuration	01h

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TABLE 8: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

Addr	R/W	Name	Function	Modification Stage	Default
444Fh	R/W	USB3_HUB_PRD_STR_INDEX	USB 3.1 Gen 1 Product String Index	Configuration	02h
444Gh	R/W	USB3_HUB_SER_STR_INDEX	USB 3.1 Gen 1 Serial String Index	Configuration	00h
44A2h	R/W	USB3_NBR_PRTS	USB 3.1 Gen 1 Number of Ports (Note 4-7, Note 4-10)	Configuration	04h
44A3h	R/W	USB3_COMPOUND	(Note 4-5, Note 4-10)	Configuration	2Ah
44A5h	R/W	UBS3_HUB_PWR2PWR-GOOD	USB3.1 Gen 1 Hub Power to Power Good Descriptor	Configuration	64h
44AAh	R/W	USB3_NRD	USB 3.1 Gen 1 Hub Non Removable Device (Note 4-5, Note 4-10)	Configuration	00h
44ACh -456Eh	R/W	USB3_HUB_STR_CONTAINTER	USB3 Hub String Container	Configuration	see reg.
6086h	R/W	SS_P0_AFE_TEST_IN4	USB3 Port 0 TX Pre-Driver	Configuration	00h
60CAh	R/W	HS_P0_BOOST	USB Port 0 Boost Register	Configuration	00h
60CCh	R/W	HS_P0_VSENSE	USB Port 0 VariSense Register	Configuration	00h
61C0	R	SS_P0_LTSSM_STATE	USB3 Port 0 LTSSM State	Runtime	00h
61D0	R/W	SS_P0_TEST_PIPE_CTL_0	USB3 Port 0 TX_MARGIN	Configuration	00h
6486h	R/W	SS_P1_AFE_TEST_IN4	USB3 Port 1 TX Pre-Driver	Configuration	00h
64CAh	R/W	HS_P1_BOOST	USB Port 1 Boost Register	Configuration	00h
64CCh	R/W	HS_P1_VSENSE	USB Port 1 VariSense Register	Configuration	00h
65C0	R	SS_P1_LTSSM_STATE	USB3 Port 1 LTSSM State	Runtime	00h
65D0	R/W	SS_P1_TEST_PIPE_CTL_0	USB3 Port 1 TX_MARGIN	Configuration	00h
6886h	R/W	SS_P2_AFE_TEST_IN4	USB3 Port 2 TX Pre-Driver	Configuration	00h
68CAh	R/W	HS_P2_BOOST	USB Port 2 Boost Register	Configuration	00h
68CCh	R/W	HS_P2_VSENSE	USB Port 2 VariSense Register	Configuration	00h
69C0	R	SS_P2_LTSSM_STATE	USB3 Port 2 LTSSM State	Runtime	00h
69D0	R/W	SS_P2_TEST_PIPE_CTL_0	USB3 Port 2 TX_MARGIN	Configuration	00h
6C86h	R/W	SS_P3_AFE_TEST_IN4	USB3 Port 3 TX Pre-Driver	Configuration	00h
6CCAh	R/W	HS_P3_BOOST	USB Port 3 Boost Register	Configuration	00h
6CCCh	R/W	HS_P3_VSENSE	USB Port 3 VariSense Register	Configuration	00h
6DC0	R	SS_P3_LTSSM_STATE	USB3 Port 3 LTSSM State	Runtime	00h
7DD0	R/W	SS_P3_TEST_PIPE_CTL_0	USB3 Port 3 TX_MARGIN	Configuration	00h
7086h	R/W	SS_P4_AFE_TEST_IN4	USB3 Port 4 TX Pre-Driver	Configuration	00h
70CAh	R/W	HS_P4_BOOST	USB Port 4 Boost Register	Configuration	00h
70CCh	R/W	HS_P4_VSENSE	USB Port 4 VariSense Register	Configuration	00h
71C0	R	SS_P4_LTSSM_STATE	USB3 Port 4 LTSSM State	Runtime	00h
71D0	R/W	SS_P4_TEST_PIPE_CTL_0	USB3 Port 4 TX_MARGIN	Configuration	00h

Note 4-1 See Section 5.0, "Using GPIOs" for details on how to configure the hub for GPIO control.

Note 4-2 The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.1 Gen 1 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

Note 4-3 Product IDs change according to description in Section 7.0, "Hub Product IDs".

Note 4-4 The default value of this register varies depending on the device firmware and silicon revision.

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Note 4-5 For ports that have both a USB2.0 and USB3.1 Gen 1 component, both the USB2 and USB3.1 hub registers should reflect equivalent Non-Removable settings for that port. Failure to do so may result in compliance testing failures. The Hub Feature Controller port, for example, has only a USB2.0 port component (i.e.: there is no USB3 component to this port), and does not need to adhere to this rule.

Note 4-6 For USB5734 and USB5744, the default value of this register is 00h. For USB5742, the default value of this register is 18h.

Note 4-7 The Port Disable settings must be assigned the same value for both the USB 2.0 Hub and USB 3.1 Gen 1 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

Note 4-8 For USB5734 and USB5744, the default value of this register is 43h. For USB5742, the default value of this register is 00h.

Note 4-9 For USB5734 and USB5744, the default value of this register is 83h. For USB5742, the default value of this register is A4h.

Note 4-10 USB 3.1 Gen 1 registers are not dynamic and can only be configured through OTP or prior to the SMBus Attach.

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4.1 Register Definitions

TABLE 9: DEVICE REVISION REGISTER

DEV_REV (0800h)			Device Revision Register
Bit	**Name**	**R/W**	**Description**
7:0	REV	R	Silicon Revision ID A0h = A0 silicon A1h = A1 silicon B0h = B0 silicon B0h = B1 silicon

TABLE 10: GPIO 1-7 PULL-DOWN REGISTER

GPIO_1_7_PD (082Fh)			GPIO 1-7 Pull-down Register
Bit	**Name**	**R/W**	**Description**
7	GPIO_7_PD	R/W	Set bit to enable GPIO7 Pull-down resistor.
6	GPIO_6_PD	R/W	Set bit to enable GPIO6 Pull-down resistor.
5	GPIO_5_PD	R/W	Set bit to enable GPIO5 Pull-down resistor.
4	GPIO_4_PD	R/W	Set bit to enable GPIO4 Pull-down resistor.
3	GPIO_3_PD	R/W	Set bit to enable GPIO3 Pull-down resistor.
2	GPIO_2_PD	R/W	Set bit to enable GPIO2 Pull-down resistor.
1	GPIO_1_PD	R/W	Set bit to enable GPIO1 Pull-down resistor.
0	Reserved	R	Reserved

TABLE 11: GPIO 8-11 PULL-DOWN REGISTER

GPIO_8_11_PD (082Eh)			GPIO 8-11 Pull-down Register
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	GPIO_11_PD	R/W	Set bit to enable GPIO11 Pull-down resistor.
2	GPIO_10_PD	R/W	Set bit to enable GPIO10 Pull-down resistor.
1	GPIO_9_PD	R/W	Set bit to enable GPIO9 Pull-down resistor.
0	GPIO_8_PD	R/W	Set bit to enable GPIO8 Pull-down resistor.

TABLE 12: GPIO 17-20 PULL-DOWN REGISTER

GPIO_17_20_PD (082Dh)			GPIO 17-20 Pull-down Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_20_PD	R/W	Set bit to enable GPIO20 Pull-down resistor.
3	GPIO_19_PD	R/W	Set bit to enable GPIO19 Pull-down resistor.
2	GPIO_18_PD	R/W	Set bit to enable GPIO18 Pull-down resistor.
1	GPIO_17_PD	R/W	Set bit to enable GPIO17 Pull-down resistor.
0	Reserved	R	Reserved

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TABLE 13: GPIO 1-7 DIRECTION CONTROL REGISTER

GPIO_1_7_DIR (0833h)			GPIO 1-7 Direction Control Register
Bit	**Name**	**R/W**	**Description**
7	GPIO_7_DIR	R/W	Set bit to configure GPIO7 as an output. Clear bit to configure GPIO7 as an input.
6	GPIO_6_DIR	R/W	Set bit to configure GPIO6 as an output. Clear bit to configure GPIO7 as an input.
5	GPIO_5_DIR	R/W	Set bit to configure GPIO5 as an output. Clear bit to configure GPIO7 as an input.
4	GPIO_4_DIR	R/W	Set bit to configure GPIO4 as an output. Clear bit to configure GPIO7 as an input.
3	GPIO_3_DIR	R/W	Set bit to configure GPIO3 as an output. Clear bit to configure GPIO7 as an input.
2	GPIO_2_DIR	R/W	Set bit to configure GPIO2 as an output. Clear bit to configure GPIO7 as an input.
1	GPIO_1_DIR	R/W	Set bit to configure GPIO1 as an output. Clear bit to configure GPIO7 as an input.
0	Reserved	R	Reserved

TABLE 14: GPIO 8-11 DIRECTION CONTROL REGISTER

GPIO_8_11_DIR (0832h)			GPIO 8-11 Direction Control Register
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	GPIO_11_DIR	R/W	Set bit to configure GPIO11 as an output. Clear bit to configure GPIO11 as an input.
2	GPIO_10_DIR	R/W	Set bit to configure GPIO10 as an output. Clear bit to configure GPIO10 as an input.
1	GPIO_9_DIR	R/W	Set bit to configure GPIO9 as an output. Clear bit to configure GPIO9 as an input.
0	GPIO_8_DIR	R/W	Set bit to configure GPIO8 as an output. Clear bit to configure GPIO8 as an input.

TABLE 15: GPIO 17-20 DIRECTION CONTROL REGISTER

GPIO_17_20_DIR (0831h)			GPIO 17-20 Direction Control Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_20_DIR	R/W	Set bit to configure GPIO20 as an output. Clear bit to configure GPIO10 as an input.
3	GPIO_19_DIR	R/W	Set bit to configure GPIO19 as an output. Clear bit to configure GPIO19 as an input.
2	GPIO_18_DIR	R/W	Set bit to configure GPIO18 as an output. Clear bit to configure GPIO18 as an input.
1	GPIO_17_DIR	R/W	Set bit to configure GPIO17 as an output. Clear bit to configure GPIO17 as an input.
0	Reserved	R	Reserved

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TABLE 16: GPIO 1-7 OUTPUT REGISTER

GPIO_1_7_OUT (0837h)			GPIO 1-7 Output Register
Bit	**Name**	**R/W**	**Description**
7	GPIO_7_OUT	R/W	Access to the GPIO7 Output Register
6	GPIO_6_OUT	R/W	Access to the GPIO6 Output Register
5	GPIO_5_OUT	R/W	Access to the GPIO5 Output Register
4	GPIO_4_OUT	R/W	Access to the GPIO4 Output Register
3	GPIO_3_OUT	R/W	Access to the GPIO3 Output Register
2	GPIO_2_OUT	R/W	Access to the GPIO2 Output Register
1	GPIO_1_OUT	R/W	Access to the GPIO1 Output Register
0	Reserved	R	Reserved

TABLE 17: GPIO 8-11 OUTPUT REGISTER

GPIO_8_11_OUT (0836h)			GPIO 8-11 Output Register
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	GPIO_11_OUT	R/W	Access to the GPIO11 Output Register
2	GPIO_10_OUT	R/W	Access to the GPIO10 Output Register
1	GPIO_9_OUT	R/W	Access to the GPIO9 Output Register
0	GPIO_8_OUT	R/W	Access to the GPIO8 Output Register

TABLE 18: GPIO 17-20 OUTPUT REGISTER

GPIO_17_20_OUT (0835h)			GPIO 17-20 Output Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_20_OUT	R/W	Access to the GPIO20 Output Register
3	GPIO_19_OUT	R/W	Access to the GPIO19 Output Register
2	GPIO_18_OUT	R/W	Access to the GPIO18 Output Register
1	GPIO_17_OUT	R/W	Access to the GPIO17 Output Register
0	Reserved	R	Reserved

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TABLE 19: GPIO 1-7 INPUT REGISTER

GPIO_1_7_IN (083Bh)			GPIO 1-7 Input Register
Bit	**Name**	**R/W**	**Description**
7	GPIO_7_IN	R/W	Access to the GPIO7 Input Register
6	GPIO_6_IN	R/W	Access to the GPIO6 Input Register
5	GPIO_5_IN	R/W	Access to the GPIO5 Input Register
4	GPIO_4_IN	R/W	Access to the GPIO4 Input Register
3	GPIO_3_IN	R/W	Access to the GPIO3 Input Register
2	GPIO_2_IN	R/W	Access to the GPIO2 Input Register
1	GPIO_1_IN	R/W	Access to the GPIO1 Input Register
0	Reserved	R	Reserved

TABLE 20: GPIO 8-11 INPUT REGISTER

GPIO_8_11_INP_BUF (083Ah)			GPIO 8-11 Input Register
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	GPIO_11_IN	R/W	Access to the GPIO11 Input Register
2	GPIO_10_IN	R/W	Access to the GPIO10 Input Register
1	GPIO_9_IN	R/W	Access to the GPIO9 Input Register
0	GPIO_8_IN	R/W	Access to the GPIO8 Input Register

TABLE 21: GPIO 17-20 INPUT REGISTER

GPIO_17_20_INP_BUF (0839h)			GPIO 17-20 Input Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_20_IN	R/W	Access to the GPIO20 Input Register
3	GPIO_19_IN	R/W	Access to the GPIO19 Input Register
2	GPIO_18_IN	R/W	Access to the GPIO18 Input Register
1	GPIO_17_IN	R/W	Access to the GPIO17 Input Register
0	Reserved	R	Reserved

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TABLE 22: GPIO 1-7 PULL-UP REGISTER

GPIO_1_7_PU (083Fh)			GPIO 1-7 Pull-up Register
Bit	**Name**	**R/W**	**Description**
7	GPIO_7_PU	R/W	Set bit to enable GPIO7 Pull-up resistor.
6	GPIO_6_PU	R/W	Set bit to enable GPIO6 Pull-up resistor.
5	GPIO_5_PU	R/W	Set bit to enable GPIO5 Pull-up resistor.
4	GPIO_4_PU	R/W	Set bit to enable GPIO4 Pull-up resistor.
3	GPIO_3_PU	R/W	Set bit to enable GPIO3 Pull-up resistor.
2	GPIO_2_PU	R/W	Set bit to enable GPIO2 Pull-up resistor.
1	GPIO_1_PU	R/W	Set bit to enable GPIO1 Pull-up resistor.
0	Reserved	R	Reserved

TABLE 23: GPIO 8-11 PULL-UP REGISTER

GPIO_8_11_PU (083Eh)			GPIO 8-11 Pull-up Register
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	GPIO_11_PU	R/W	Set bit to enable GPIO11 Pull-up resistor.
2	GPIO_10_PU	R/W	Set bit to enable GPIO10 Pull-up resistor.
1	GPIO_9_PU	R/W	Set bit to enable GPIO9 Pull-up resistor.
0	GPIO_8_PU	R/W	Set bit to enable GPIO8 Pull-up resistor.

TABLE 24: GPIO 17-20 PULL-UP REGISTER

GPIO_17_20_PU (083Dh)			GPIO 17-20 Pull-up Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_20_PU	R/W	Set bit to enable GPIO20 Pull-up resistor.
3	GPIO_19_PU	R/W	Set bit to enable GPIO19 Pull-up resistor.
2	GPIO_18_PU	R/W	Set bit to enable GPIO18 Pull-up resistor.
1	GPIO_17_PU	R/W	Set bit to enable GPIO17 Pull-up resistor.
0	Reserved	R	Reserved

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TABLE 25: USB 2.0 OCS STATUS REGISTER

USB2_OCS_STAT (0900h)			USB 2.0 OCS Status Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	USB2_OCS_STAT_P4		Indicates if the USB 2.0 downstream port 4 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
3	USB2_OCS_STAT_P3		Indicates if the USB 2.0 downstream port 3 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
2	USB2_OCS_STAT_P2		Indicates if the USB 2.0 downstream port 2 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
1	USB2_OCS_STAT_P1		Indicates if the USB 2.0 downstream port 1 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
0	Reserved	R	Reserved

TABLE 26: USB 3.1 GEN 1 OCS STATUS REGISTER

USB3_OCS_STAT (0902h)			USB 3.1 Gen 1 OCS Status Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	USB3_OCS_STAT_P4		Indicates if the USB 3.1 Gen 1 downstream port 4 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
3	USB3_OCS_STAT_P3		Indicates if the USB 3.1 Gen 1 downstream port 3 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
2	USB3_OCS_STAT_P2		Indicates if the USB 3.1 Gen 1 downstream port 2 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
1	USB3_OCS_STAT_P1		Indicates if the USB 3.1 Gen 1 downstream port 1 had an OCS event. The bit stays asserted until it is cleared and the OCS event ceases. 0 = No OCS Condition 1 = OCS Condition
0	Reserved	R	Reserved

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TABLE 27: USB 2.0 HUB VENDOR ID LSB

USB2_VIDL (3000h)			USB 2.0 Hub Vendor ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	VID_LSB	R/W	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum). If this register is modified, the contents of the USB 3.1 Gen 1 Hub Vendor ID LSB register must also be identically modified.

TABLE 28: USB 2.0 HUB VENDOR ID MSB

USB2_VIDM (3001h)			USB 2.0 Hub Vendor ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	VID_MSB	R/W	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum). If this register is modified, the contents of the USB 3.1 Gen 1 Hub Vendor ID MSB register must also be identically modified.

TABLE 29: USB 2.0 HUB PRODUCT ID LSB

USB2_PIDL (3002h)			USB 2.0 Hub Product ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	PID_LSB	R/W	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 30: USB 2.0 HUB PRODUCT ID MSB

USB2_PIDM (3003h)			USB 2.0 Hub Product ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	PID_MSB	R/W	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 31: USB 2.0 HUB DEVICE ID LSB

USB2_DIDL (3004h)			USB 2.0 Hub Product ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	DID_LSB	R/W	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

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TABLE 32: USB 2.0 HUB DEVICE ID MSB

USB2_DIDM (3005h)			USB 2.0 Hub Product ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	DID_MSB	R/W	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 33: USB 2.0 HUB CONFIGURATION 1

CFG1 (3006h)			USB 2.0 Hub Configuration 1
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved
6	VSM_DISABLE	R/W	0 = VSM Messaging is supported. 1 = VSM Messaging is disabled. When VSM is disabled, all vendor-specific messaging to the hub end-point will be ignored with no ill effect.
5	HS_DISABLE	R/W	High Speed Disable: Disables the capability to attach as either a High-/Full-Speed device, and forces attachment as Full-Speed only (i.e., no High-Speed support). 0 = High-/Full-Speed. 1 = Full-Speed Only (High-Speed disabled)
4	MTT_ENABLE	R/W	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT). **Note:** The host may force Single-TT mode only. 0 = Single TT for all ports. 1 = One TT per port (multiple TTs supported)
3	Reserved	R	Reserved
2:1	CURRENT_SNS	R/W	Overcurrent Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together) 01 = Individual port-by-port 1x = Overcurrent sensing not supported (must only be used with Bus-Powered configurations!)
0	PORT_PWR	R/W	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching

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TABLE 34: USB 2.0 HUB CONFIGURATION 2

CFG2 (3007h)			USB 2.0 Hub Configuration 2
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Reserved
5:4	OC_TIMER	R/W	Overcurrent Timer delay. This measures the minimum pulse width for which a pulse is considered valid. 00 = 3 Clock samples 01 = 6 Clock samples 10 = 12 Clock samples 11 = 24 Clock samples
3	COMPOUND	R/W	Compound Device: Allows the OEM to indicate that the hub is part of a compound device (see the USB Specification for definition). The applicable ports must also be defined as having a “Non-Removable Device”. **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 = No. 1 = Yes, the hub is part of a compound device. **Note:** If this register is modified, the USB 3.1 Gen 1 Hub equivalent must also be modified in the register.
2:0	Reserved	R	Reserved

TABLE 35: USB 2.0 HUB CONFIGURATION 3

CFG3 (3008h)			USB 2.0 Hub Configuration 3
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	HUB_RESUME_INHIBIT	R/W	When HUB_RESUME_INHIBIT = ‘0’, Normal Resume Behavior per the USB 3.1 Gen 1 Specification. When HUB_RESUME_INHIBIT = ‘1’, Modified Resume Behavior is enabled.
3	PRTMAP_EN	R/W	Port Re-mapping Enable: Selects the method used by the hub to assign port numbers and disable ports. 0 = Standard mode. Strap options or the following registers are used to define which ports are enabled. The ports mapped as Port “n” on the hub are reported as Port “n” to the host. If one of the ports is disabled, the higher numbered ports are remapped in order to report contiguous port numbers to the host. 1 = Port Re-Map mode. This mode enables remapping via the registers defined below.
2	BOS_DISABLE	R/W	0 = BOS Descriptor Enabled. BOS commands processed by hardware. 1 = BOS Descriptor Disabled. BOS commands return STALL response.
1	Reserved	R	Reserved
0	STRING_EN		Enables String Descriptor Support 0 = String Support Disabled 1 = String Support Enabled

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TABLE 36: USB 2.0 HUB NON-REMOVABLE DEVICE

USB2_NRD (3009h)			USB 2.0 Hub Non-Removable Device
Bit	**Name**	**R/W**	**Description**
7:0	NR_DEVICE	R/W	Non-Removable Device: Indicates which ports include non-removable devices: '0' = port is removable, '1' = port is non-removable. Informs the host if one of the active ports has a permanent device that is undetachable from the hub. The ports may also be configured as non-removable using the hardware strapping option described in section 3.4.3 of the *USB57x4 Data Sheet*. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = 1; Physical Port 5 (internal HFC port) is non-removable. Bit 4 = 1; Physical Port 4 is non-removable. Bit 3 = 1; Physical Port 3 is non-removable. Bit 2 = 1; Physical Port 2 is non-removable. Bit 1 = 1; Physical Port 1 is non removable. Bit 0 is Reserved, always = '0' **Note 1:** If this register is modified, the USB 3.1 Gen 1 Hub equivalent should also be modified in the USB 3.1 Gen 1 Hub Non Removable Device register. **2:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 37: USB 2.0 PORT DISABLE (SELF-POWERED)

PDS (300Ah)			USB 2.0 Hub Power Disable (Self-Powered)
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_SP	R/W	Port Disable Self-Powered: Disables one or more ports: '0' = port is available, '1' = port is disabled. During Self-Powered operation, when PRTMAP_EN = 1, this selects the ports that will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, and the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports to ensure proper functioning. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = 1; Physical Port 5 (internal HFC port) is disabled. Bit 4 = 1; Physical Port 4 is disabled. Bit 3 = 1; Physical Port 3 is disabled. Bit 2 = 1; Physical Port 2 is disabled. Bit 1 = 1; Physical Port 1 is disabled. Bit 0 is Reserved, always = '0' **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

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TABLE 38: USB 2.0 PORT DISABLE (BUS-POWERED)

PDB (300Bh)			USB 2.0 Hub Port Disable (Bus-Powered)
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_BP	R/W	Port Disable Bus-Powered: Disables one or more ports: '0' = port is available, '1' = port is disabled. During Bus-Powered operation, when PRTMAP_EN = 1, this selects the ports that will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, and the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports to ensure proper functioning. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = 1; Physical Port 5 (internal HFC port) is disabled. Bit 4 = 1; Physical Port 4 is disabled. Bit 3 = 1; Physical Port 3 is disabled. Bit 2 = 1; Physical Port 2 is disabled. Bit 1 = 1; Physical Port 1 is disabled. Bit 0 is Reserved, always = '0' **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 39: USB 2.0 HUB MANUFACTURER STRING INDEX

MFR_STR_INDEX (3013h)			USB 2.0 Hub Manufacturer String Index Register
Bit	**Name**	**R/W**	**Description**
7:0	MFR_STR_LEN	R/W	Manufacturer String Index. The index number for the manufacturer string.

TABLE 40: USB 2.0 HUB PRODUCT STRING INDEX

PRD_STR_INDEX (3014h)			USB 2.0 Hub Product String Index Register
Bit	**Name**	**R/W**	**Description**
7:0	PRD_STR_LEN	R/W	Product String Index. The index number for the product string.

TABLE 41: USB 2.0 HUB SERIAL STRING INDEX

SER_STR_INDEX (3015h)			USB 2.0 Hub Serial String Index Register
Bit	**Name**	**R/W**	**Description**
7:0	SER_STR_LEN	R/W	Serial String Index. The index number for the serial string.

TABLE 42: USB 2.0 DP/DM PORT SWAP

PRTSP (30FAh)			USB 2.0 DP/DM Port Swap
Bit	**Name**	**R/W**	**Description**
7:0	PRT_SWAP	R/W	Port Swap: Swaps the Upstream and Downstream USB DP and DM pins for ease of board routing to devices and connectors. '0' = USB D+ functionality is associated with the DP pin, and D- functionality is associated with the DM pin. '1' = USB D+ functionality is associated with the DM pin, and D- functionality is associated with the DP pin. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = '1': Physical Port 4 DP/DM is swapped. Bit 3 = '1': Physical Port 3 DP/DM is swapped. Bit 2 = '1': Physical Port 2 DP/DM is swapped. Bit 1 = '1': Physical Port 1 DP/DM is swapped. Bit 0 = '1': Upstream Port DP/DM is swapped. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

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TABLE 43: USB 2.0 PORT 1/PORT 2 DISABLE

USB2_PRT_EN_12 (30FBh)			Port 1/2 Disable
Bit	**Name**	**R/W**	**Description**
7:4	PRT_2_DIS	R/W	0000 - Physical Port 2 is disabled. 0001 - Physical Port 2 is mapped to Logical Port 1. 0010 - Physical Port 2 is mapped to Logical Port 2. 0011 - Physical Port 2 is mapped to Logical Port 3. 0100 - Physical Port 2 is mapped to Logical Port 4. 0101 - Physical Port 2 is mapped to Logical Port 5. 0110 - 1111 Reserved, will default to 0000 value. **Note 1:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports, and the USB 3.1 Gen 1 Equivalent must also be configured in the USB 3.1 Gen 1 Port 2 Configuration Select register. **2:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family. **3:** When disabling USB2 ports through these registers, higher numbered ports should also be remapped such that the port numbering is always contiguous, starting with port number 1 and counting up. As an example, if only Port 1 is disabled, Physical Port 2 must be remapped to Logical Port 1, Physical Port 3 must be remapped to Logical Port 2, and so on.
3:0	PRT_1_DIS	R/W	0000 - Physical Port 1 is disabled. 0001 - Physical Port 1 is mapped to Logical Port 1. 0010 - Physical Port 1 is mapped to Logical Port 2. 0011 - Physical Port 1 is mapped to Logical Port 3. 0100 - Physical Port 1 is mapped to Logical Port 4. 0101 - Physical Port 1 is mapped to Logical Port 5. 0110 - 1111 Reserved, will default to 0000 value. **Note 1:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports, and the USB 3.1 Gen 1 Equivalent must also be configured in the USB 3.1 Gen 1 Port 1 Configuration Select register. **2:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family. **3:** When disabling USB2 ports through these registers, higher numbered ports should also be remapped such that the port numbering is always contiguous, starting with port number 1 and counting up. As an example, if only Port 2 is disabled, Physical Port 3 must be remapped to Logical Port 2, Physical Port 4 must be remapped to Logical Port 3, and so on.

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TABLE 44: USB 2.0 PORT 3/PORT 4 DISABLE

USB2_PRT_EN_34 (30FCh)			Port 3/4 Disable
Bit	**Name**	**R/W**	**Description**
7:4	PRT_4_DIS	R/W	0000 - Physical Port 4 is disabled. 0001 - Physical Port 4 is mapped to Logical Port 1. 0010 - Physical Port 4 is mapped to Logical Port 2. 0011 - Physical Port 4 is mapped to Logical Port 3. 0100 - Physical Port 4 is mapped to Logical Port 4. 0101 - Physical Port 4 is mapped to Logical Port 5. 0110 - 1111 Reserved, will default to 0000 value. **Note 1:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports, and the USB 3.1 Gen 1 Equivalent must also be configured in the USB 3.1 Gen 1 Port 4 Configuration Select register. **2:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family. **3:** When disabling USB2 ports through these registers, higher numbered ports should also be remapped such that the port numbering is always contiguous, starting with port number 1 and counting up. As an example, if only Port 4 is disabled, Physical Port 5 (internal HFC port) must be remapped to Logical Port 4.
3:0	PRT_3_DIS	R/W	0000 - Physical Port 3 is disabled. 0001 - Physical Port 3 is mapped to Logical Port 1. 0010 - Physical Port 3 is mapped to Logical Port 2. 0011 - Physical Port 3 is mapped to Logical Port 3. 0100 - Physical Port 3 is mapped to Logical Port 4. 0101 - Physical Port 3 is mapped to Logical Port 5. 0110 - 1111 Reserved, will default to 0000 value. **Note 1:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports, and the USB 3.1 Gen 1 Equivalent must also be configured in the USB 3.1 Gen 1 Port 3 Configuration Select register. **2:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family. **3:** When disabling USB2 ports through these registers, higher numbered ports should also be remapped such that the port numbering is always contiguous, starting with port number 1 and counting up. As an example, if only Port 3 is disabled, Physical Port 4 must be remapped to Logical Port 3, and Physical Port 5 (internal HFC port) must be remapped to Logical Port 4.

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TABLE 45: USB 2.0 HUB CONTROLLER DISABLE

HC_DIS (30FDh)			Hub Controller Disable
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:0	HC_DIS	R/W	0000 - Physical Port 5 (internal only port) is disabled. 0001 - Physical Port 5 (internal-only port) is mapped to Logical Port 1. 0010 - Physical Port 5 (internal-only port) is mapped to Logical Port 2. 0011 - Physical Port 5 (internal-only port) is mapped to Logical Port 3. 0100 - Physical Port 5 (internal-only port) is mapped to Logical Port 4. 0101 - Physical Port 5 (internal-only port) is mapped to Logical Port 5. 0110 - 1111 Reserved, will default to 0000 value. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 46: USB 2.0 LINK STATE PORTS 0 ~ 3

USB2_LINK_STATE1_3 (3100h)			Port 0-3 USB 2.0 Link States
Bit	**Name**	**R/W**	**Description**
7:6	L_STATE3	R	Indicates the state of downstream Physical Port 3. 00 - L0 Normal Operation 01 - L1 Sleep 10 - L2 Suspend 11 - L3 Off
5:4	L_STATE2	R	Indicates the state of downstream Physical Port 2. 00 - L0 Normal Operation 01 - L1 Sleep 10 - L2 Suspend 11 - L3 Off
3:2	L_STATE1	R	Indicates the state of downstream Physical Port 1. 00 - L0 Normal Operation 01 - L1 Sleep 10 - L2 Suspend 11 - L3 Off
1:0	L_STATE0	R	Indicates the state of upstream Physical Port 0. 00 - L0 Normal Operation 01 - L1 Sleep 10 - L2 Suspend 11 - L3 Off

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 47: USB 2.0 LINK STATE PORT 4

USB2_LINK_STATE2 (3101h)			Port 4 USB 2.0 Link State
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	L_STATE5	R	Indicates the state of the internal only HFC Physical Port 5. 00 - L0 Normal Operation 01 - L1 Sleep 10 - L2 Suspend 11 - L3 Off
1:0	L_STATE4	R	Indicates the state of the downstream Physical Port 4. 00 - L0 Normal Operation 01 - L1 Sleep 10 - L2 Suspend 11 - L3 Off

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 48: USB 2.0 HUB CONTROL

USB2_HUB_CTL (3104h)			USB 2.0 Hub Control
Bit	**Name**	**R/W**	**Description**
7:4	HIRD	R	Host Initiated Resume Duration. This is a direct read of the Host Initiated Resume Duration sent by the USB 2.0 Host. This field indicates the minimum amount of time the host will drive the K-state during a resume. A value 0000b equals 50 us, and each additional increment adds 75 us.
3:2	Reserved	R	Reserved
1	LPM_DISABLE	R/W	Disables Link Power Management.
0	RESET	R/W	Setting this bit will keep the USB 2.0 Hub in reset.

TABLE 49: CONNECT CONFIGURATION REGISTER

CONNECT_CFG (318Eh)			Connect Configuration Register
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	FLEXCONNECT	R/W	FlexConnect Control. When asserted the USB57xx changes its hub connections so that the Swap port (Physical Port 1) changes from its default behavior of a downstream port to an upstream port. The Flex Port (Physical port 0) transitions from an upstream port to a downstream port. ‘0’ - Flex Port = Up (Port 0); Swap Port = Down (Port 1) ‘1’ - Flex Port = Down (Port 1); Swap Port = Up (Port 0)

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TABLE 50: USB 3.1 GEN 1 HUB CONTROL

USB3_HUB_CTL (3840h)			USB3.1 Gen 1 Hub Control
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	GANG_OVER_CURRENT	R/W	0 - Individual Overcurrent 1 - Ganged Overcurrent
3	BUS_POWERED	R/W	0 - Self Powered Hub 1 - Bus Powered Hub
2:0	Reserved	R	Always ‘0’

TABLE 51: USB 3.1 GEN 1 LINK LOW POWER STATE 1

LINK_PWR_STATE1 (3870h)			USB 3.1 Gen 1 Link Low Power State 1
Bit	**Name**	**R/W**	**Description**
7:6	P_STATE3	R	Indicates the state of downstream PHY3 (Physical Port 3). 00 - U0 Normal Operation 01 - U1 Low recovery time latency 10 - U2 Longer recovery time latency 11 - U3 Lowest power state
5:4	P_STATE2	R	Indicates the state of downstream PHY2 (Physical Port 2). 00 - U0 Normal Operation 01 - U1 Low recovery time latency 10 - U2 Longer recovery time latency 11 - U3 Lowest power state
3:2	P_STATE1	R	Indicates the state of downstream PHY1 (Physical Port 1). 00 - U0 Normal Operation 01 - U1 Low recovery time latency 10 - U2 Longer recovery time latency 11 - U3 Lowest power state
1:0	P_STATE0	R	Indicates the state of the upstream PHY (Physical Port 0). 00 - U0 Normal Operation 01 - U1 Low recovery time latency 10 - U2 Longer recovery time latency 11 - U3 Lowest power state

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 52: USB 3.1 GEN 1 LINK LOW POWER STATE 2

LINK_PWR_STATE2 (3874h)			USB 3.1 Gen 1 Link Low Power State 2
Bit	**Name**	**R/W**	**Description**
7:2	Reserved	R	Always '0'
1:0	P_STATE4	R	Indicates the state of downstream PHY4 (Physical Port 4). 00 - U0 Normal Operation 01 - U1 Low recovery time latency 10 - U2 Longer recovery time latency 11 - U3 Lowest power state

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 53: USB 3.1 GEN 1 PORT 1 CONFIGURATION SELECT

USB3_PRT_CFG_SEL1 (3C00h)			Port 1 Configuration Select
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. **Note:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports. The USB 2.0 equivalent must also be configured in the USB 2.0 Port 1/Port 2 Disable register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently-attached device.
3:0	Port Power Select	R/W	This field selects the source for the port power for Physical Port 1. Port power is only set by a USB host via a directed command to the hub. This command is issued independently from both the USB2 and USB3 links to the host. 0000 - Port power is disabled on this port. 0001 - Port power is on if only USB2 port power is on. 0010 - Port power is on if only USB3 port power is on. 0011 - Port power is on if USB2 or USB3 port power is on. 0100 - The pin is a GPIO. All other values are reserved.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

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TABLE 54: USB 3.1 GEN 1 PORT 2 CONFIGURATION SELECT

USB3_PRT_CFG_SEL2 (3C04h)			Port 2 Configuration Select
Bit	**Name**	**R/W**	**Description**
7	Reserved	R/W	Reserved
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. **Note:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports. The USB 2.0 equivalent must also be configured in the USB 2.0 Port 1/Port 2 Disable register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently-attached device.
3:0	Port Power Select	R/W	This field selects the source for the port power for Physical Port 2. Port power is only set by a USB host via a directed command to the hub. This command is issued independently from both the USB2 and USB3 links to the host. 0000 - Port power is disabled on this port. 0001 - Port power is on if only USB2 port power is on. 0010 - Port power is on if only USB3 port power is on. 0011 - Port power is on if USB2 or USB3 port power is on. 0100 - The pin is a GPIO. All other values are reserved.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 55: USB 3.1 GEN 1 PORT 3 CONFIGURATION SELECT

USB3_PRT_CFG_SEL3 (3C08h)			Port 3 Configuration Select
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. **Note:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports. The USB 2.0 equivalent must also be configured in the USB 2.0 Port 3/Port 4 Disable register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently-attached device.
3:0	Port Power Select	R/W	This field selects the source for the port power for Physical Port 3. Port power is only set by a USB host via a directed command to the hub. This command is issued independently from both the USB2 and USB3 links to the host. 0000 - Port power is disabled on this port. 0001 - Port power is on if only USB2 port power is on. 0010 - Port power is on if only USB3 port power is on. 0011 - Port power is on if USB2 or USB3 port power is on. 0100 - The pin is a GPIO. All other values are reserved.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 56: USB 3.1 GEN 1 PORT 4 CONFIGURATION SELECT

USB3_PRT_CFG_SEL4 (3C0Ch)			Port 4 Configuration Select
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. **Note:** If this register is modified, the number of total USB 3.1 Gen 1 ports must be updated in USB 3.1 Gen 1 Number of Ports. The USB 2.0 equivalent must also be configured in the USB 2.0 Port 3/Port 4 Disable register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently-attached device.
3:0	Port Power Select	R/W	This field selects the source for the port power for Physical Port 4. Port power is only set by a USB host via a directed command to the hub. This command is issued independently from both the USB2 and USB3 links to the host. 0000 - Port power is disabled on this port. 0001 - Port power is on if only USB2 port power is on. 0010 - Port power is on if only USB3 port power is on. 0011 - Port power is on if USB2 or USB3 port power is on. 0100 - The pin is a GPIO. All other values are reserved.

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Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 57: PORT 1 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL1 (3C20h)			Port 1 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always '0'
3:0	PRT_SEL	R/W	This selects the source for the port power for Physical Port 1. 0000b - The port is disabled. 0001b - OCS comes from the OCS pin. 0010b - Reserved. 0011b - OCS comes from the GANG_PWR pin. 1111b - Reserved All other values are reserved. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 58: PORT 2 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL2 (3C24h)			Port 2 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always '0'
3:0	PRT_SEL	R/W	This selects the source for the port power for Physical Port 2. 0000b - The port is disabled. 0001b - OCS comes from the OCS pin. 0010b - Reserved 0011b - OCS comes from the GANG_PWR pin. 1111b - Reserved All other values are reserved. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 59: PORT 3 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL3 (3C28h)			Port 3 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for Physical Port 3. 0000b - The port is disabled. 0001b - OCS comes from the OCS pin. 0010b - Reserved 0011b - OCS comes from the GANG_PWR pin. 1111b - Reserved All other values are reserved. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 60: PORT 4 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL4 (3C2Ah)			Port 4 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for Physical Port 4. 0000b - The port is disabled. 0001b - OCS comes from the OCS pin. 0010b - Reserved 0011b - OCS comes from the GANG_PWR pin. 1111b - Reserved All other values are reserved. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

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TABLE 61: FLEXCONNECT CONFIGURATION 1

FLEX_CFG1 (411Ah)			FlexConnect Configuration 1
Bit	**Name**	**R/W**	**Description**
7	CHNG_PIN_FUNCT	R/W	This bit will change the digital pin controls back to the default states. For example, VBUS_DET has the same functionality regardless of the FLEX state.
6	FLEXCONNECT	R/W	The value of FLEXCONNECT after the hub is re-attached.
5	DIS_P5	R/W	Disabled internal Hub Controller on Physical Port 5 after entering the “Flexed” state. If this is disabled, then no commands can be sent to the Hub Controller when in the “Flexed” state.
4	DIS_P4	R/W	Disabled downstream Physical Port 4 after switching directions.
3	DIS_P3	R/W	Disabled downstream Physical Port 3 after switching directions.
2	DIS_P2	R/W	Disabled downstream Physical Port 2 after switching directions.
1	DIS_P1	R/W	Disabled downstream Physical Port 1 after switching directions.
0	Reserved	R	Reserved

TABLE 62: FLEXCONNECT CONFIGURATION 2

FLEX_CFG2 (411Bh)			FlexConnect Configuration 2
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved. This bit must always read ‘1’.
6	DCP_EN	R/W	Enables the universal dedicated charging algorithm to be used on disabled ports. This will cause the hub to enumerate limited ports, but the VBUS and battery charging handshake will still be present on the disabled ports.
3:5	Reserved	R	Reserved
0:2	HD_TIMER	R/W	Host Detect Timeout - The time the hub will wait for a host to enumerate before returning to the default state. 000 = No timeout 001 = 10 ms 010 = 100 ms 011 = 500 ms 100 = 1s 101 = 5s 110 = 10s 111 = 20s

TABLE 63: RUNTIME FLAGS 2

OTPFORCEUDCENABLE (411Dh)			Runtime Flags 2 Register
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	DISABLE_USB3_HUB	R/W	0 - USB3 hub will be enabled by default. 1 - USB3_HUB_ENABLE in USB3_HUB_CTL2 register will not be set and also suspend clock will not be enabled (unless downstream battery charging is enabled).
3	BYPASS_UDC_SUSPEND	R/W	0 - MCU will be suspended if the hub is suspended. This ensures that the lowest possible power is achieved, but many functions (including SMBus register access) will become non-functional. 1 - MCU will not be suspended while USB hub is suspended. This is required if SMBus runtime access is required.
2	OTP_TARGER	R/W	Set Target OTP 0 - Any command targeted to OTP (OTP Read, OTP programming, etc.) is redirected to the pseudo OTP in the SPI flash physical address 0x10000 to 0x11FFF. 1 - Any command targeted to OTP (OTP Read, OTP programming, etc.) is directed to the OTP.
1	CFG_FROM_SPI	R/W	Load Config from SPI 1 - Configuration is loaded from pseudo OTP in SPI. 0 - Configuration will not be loaded from pseudo OTP in SPI.
0	CGF_FROM_OTP	R/W	Load Config from OTP 1 - Firmware will load configuration from OTP. 0 - Configuration will not be loaded from OTP.

TABLE 64: HUB FEATURE CONTROLLER ENABLE

OTPFORCEUDCENABLE (4130h)			Hub Feature Controller Enable Register
Bit	**Name**	**R/W**	**Description**
7:0	OTPFORCEUDCENABLE	R/W	Controls Hub Feature Controller enable. 0000_0000b - Default behavior (enabled) 0000_0001b - Always enable HFC 0000_0010b - Always disable HFC All others are reserved.

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TABLE 65: BATTERY CHARGING PORT 1 CONFIGURATION

BC_CFG_P1 (413Ch)			Battery Charging Port 1 Configuration
Bit	**Name**	**R/W**	**Description**
7:6	DCP_LIM	R/W	Sets the current limit for China/DCP mode when a UCS100x device is connected to the hub. 00b - 500 mA 01b - 1000 mA 10b - 1500 mA 11b - 2000 mA
5	BC12_CDCP	R/W	When set, this enables the BC 1.2 DCP mode. If bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, this enables China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	00 - SE1 mode is disabled. 01 - SE1 1 A mode 10 - SE1 2 A mode 11 - SE1 2.5 A mode
0	BC_EN	R/W	1 - Enables Battery Charging on Physical Port 1 0 - Disables Battery Charging on Physical Port 1

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 66: BATTERY CHARGING PORT 2 CONFIGURATION

BC_CFG_P2 (413Dh)			Battery Charging Port 2 Configuration
Bit	**Name**	**R/W**	**Description**
7:6	DCP_LIM	R/W	Sets the current limit for China/DCP mode when a UCS100x device is connected to the hub. 00b - 500 mA 01b - 1000 mA 10b - 1500 mA 11b - 2000 mA
5	BC12_CDCP	R/W	When set, this enables the BC 1.2 DCP mode. If bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, this enables the China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	00 - SE1 mode is disabled. 01 - SE1 1 A mode 10 - SE1 2 A mode 11 - SE1 2.5 A mode
0	BC_EN	R/W	1 - Enables Battery Charging on Physical Port 2 0 - Disables Battery Charging on Physical Port 2

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

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TABLE 67: BATTERY CHARGING PORT 3 CONFIGURATION

BC_CFG_P3 (413Eh)			Battery Charging Port 3 Configuration
Bit	**Name**	**R/W**	**Description**
7:6	DCP_LIM	R/W	Sets the current limit for China/DCP mode when a UCS100x device is connected to the hub. 00b - 500 mA 01b - 1000 mA 10b - 1500 mA 11b - 2000 mA
5	BC12_CDCP	R/W	When set, this enables the BC 1.2 DCP mode. If bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, this enables the China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	00 - SE1 mode is disabled. 01 - SE1 1 A mode 10 - SE1 2 A mode 11 - SE1 2.5 A mode
0	BC_EN	R/W	1 - Enables Battery Charging on Physical Port 3 0 - Disables Battery Charging on Physical Port 3

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 68: BATTERY CHARGING PORT 4 CONFIGURATION

BC_CFG_P4 (413Fh)			Battery Charging Port 4 Configuration
Bit	**Name**	**R/W**	**Description**
7:6	DCP_LIM	R/W	Sets the current limit for China/DCP mode when a UCS100x device is connected to the hub. 00b - 500 mA 01b - 1000 mA 10b - 1500 mA 11b - 2000 mA
5	BC12_CDCP	R/W	When set, this enables the BC 1.2 DCP mode. If bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, this enables the China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	00 - SE1 mode is disabled. 01 - SE1 1 A mode 10 - SE1 2 A mode 11 - SE1 2.5 A mode
0	BC_EN	R/W	1 - Enables Battery Charging on Physical Port 4 0 - Disables Battery Charging on Physical Port 4

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

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TABLE 69: CDC DEVICE ENUMERATION CONTROL

CDCENUMCONTROL (4140h)			CDC (UART Bridge Device) Enumeration Control Register
Bit	**Name**	**R/W**	**Description**
7:0	CDCMODE	R/W	00h - Default behavior. Enumeration of CDC interface depends on the CFG_STRAP line. When HFC is present, HFC is interface 0, and CDC is interface 1 (control) and 2 (data). If HFC is not present, CDC is enumerated as interface 0 (control) and 1 (data). 01h - Always enable CDC enumeration regardless of CFG_STRAP. When HFC is present, HFC is interface 0, and CDC is interface 1 (control) and 2 (data). If HFC is not present, CDC is enumerated as interface 0 (control) and 1 (data). 02h - Always disable CDC enumeration regardless of CFG_STRAP setting. 03h - Same as 00h, except CDC is enumerated as interface 0 (control) and 1 (data), and HFC enumerates at interface 2 (if HFC is enabled). 04h - Same as 01h, except CDC is enumerated as interface 0 (control) and 1 (data), and HFC enumerates at interface 2 (if HFC is enabled).

TABLE 70: HUB FEATURE CONTROLLER STRING CONTAINER

HFC_STRING_CONT (4198h-4214h)			HFC String Container
Bit	**Name**	**R/W**	**Description**
1024:32	HFC_STRING_CONT	R/W	Container for the HFC string data including Product String, Manufacturer String, and Serial strings. The String for each index has to be formatted as per the USB Specification requirements on string descriptor (using descriptor length, type, and Unicode format). To skip/disable a string descriptor for index i (where i = 1, 2, and 3), set the string descriptor length to 0x01 corresponding to index i. The total combined length for all strings cannot exceed the memory space allotted, which is 128 bytes (including the LANG_ID, which is a fixed length of 4 bytes). The String type for each index assigned in **HFC_MANUFACTURER_INDEX (04DCh)**, **HFC_PRODUCT_INDEX(04DDh)**, and **HFC_SERIAL_INDEX (04DEh)** registers. The formatting for this container is as: • STRING_INDEX_1 (1 byte) • STRING_LEN_1 (1 byte) • STRING_DATA_1 (of length STRING_LEN_1) • STRING_INDEX_2 (1 byte) • STRING_LEN_2 (1 byte) • STRING_DATA_2 (of length STRING_LEN_2) • STRING_INDEX_3 (1 byte) • STRING_LEN_3 (1 byte) • STRING_DATA_3 (of length STRING_LEN_3)
31:16	STRING_DATA_0	R/W	USB-IF Language Identifier Default is English (United States) = 0409h.
15:8	STRING_LEN_0	R/W	Always 04h
7:0	STRING_INDEX_0	R/W	Always 00h

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TABLE 71: USB2 STRING INDEX 1 POINTER

USB2_STR_INDX1_PNTR (426Dh-4272h)			USB2 String Index 1 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
47:40	STR_CONT_OFFSET_L	R/W	Container Offset Pointer LSB Memory pointer to the Unicode data within in the **USB2_STRING_CONT (4325h-43A6h)** memory range for the string assigned as Index 1. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, or **SER_STR_INDEX (3015h)**.
39:32	STR_CONT_OFFSET_M	R/W	Container Offset Pointer MSB Memory pointer to the Unicode data within in the **USB2_STRING_CONT (4325h-43A6h)** memory range for the string assigned as Index 1. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, or **SER_STR_INDEX (3015h)**.
31:24	STRING_LEN	R/W	Total Length of String Unicode Data + 02h
23:15	MANU_STRING_ID	R/W	Always 00h
14:0		R/W	Always 07h
7:0		R/W	Always 01h

TABLE 72: USB2 STRING INDEX 2 POINTER

USB2_STR_INDX2_PNTR (4273h-4278h)			USB2 String Index 2 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
47:40	STR_CONT_OFFSET_L	R/W	Container Offset Pointer LSB Memory pointer to the Unicode data within in the **USB2_STRING_CONT (4325h-43A6h)** memory range for the string assigned as Index 2. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, or **SER_STR_INDEX (3015h)**.
39:32	STR_CONT_OFFSET_M	R/W	Container Offset Pointer MSB Memory pointer to the Unicode data within in the **USB2_STRING_CONT (4325h-43A6h)** memory range for the string assigned as Index 2. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, or **SER_STR_INDEX (3015h)**.
31:24	STRING_LEN	R/W	Total Length of String Unicode Data + 02h
23:15	PROD_STRING_ID	R/W	Always 00h
14:0		R/W	Always 08h
7:0		R/W	Always 01h

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TABLE 73: USB2 STRING INDEX 3 POINTER

USB2_STR_INDX3_PNTR (4279h-427Eh)			USB2 String Index 3 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
47:40	STR_CONT_OFFSET_L	R/W	Container Offset Pointer LSB Memory pointer to the Unicode data within in the **USB2_STRING_CONT (4325h-43A6h)** memory range for the string assigned as Index 3. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, or **SER_STR_INDEX (3015h)**.
39:32	STR_CONT_OFFSET_M	R/W	Container Offset Pointer MSB Memory pointer to the Unicode data within in the **USB2_STRING_CONT (4325h-43A6h)** memory range for the string assigned as Index 3. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, or **SER_STR_INDEX (3015h)**.
31:24	STRING_LEN	R/W	Total Length of String Unicode Data + 02h
23:15	SER_STRING_ID	R/W	Always 00h
14:0		R/W	Always 09h
7:0		R/W	Always 01h

TABLE 74: HFC BCDUSB LSB

HFC_BCDUSB_LSB (42D0h)			HFC BCDUSB LSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_BCDUSB_LSB	R/W	Least Significant Byte of the HFC bcdUSB descriptor Default is 01h.

TABLE 75: HFC BCDUSB MSB

HFC_BCDUSB_MSB (42D1h)			HFC BCDUSB MSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_BCDUSB_MSB	R/W	Most Significant Byte of the HFC bcdUSB descriptor Default is 02h.

TABLE 76: HFC VENDOR ID LSD

HFC_VID_LSB (042D6h)			HFC Vendor ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_VID_LSB	R/W	Least Significant Byte of the HFC Vendor ID descriptor Default is 24h.

TABLE 77: HFC VENDOR ID MSB

HFC_VID_MSB (042D7h)			HFC Vendor ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_VID_MSB	R/W	Most Significant Byte of the HFC Vendor ID descriptor Default is 04h.

TABLE 78: HFC PRODUCT ID LSB

HFC_PID_LSB (42D8h)			HFC Product ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PID_LSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that uniquely identifies this HFC device. The default value depends on the features enabled on the device as shown below: HFC only = 40h HFC only (interface 0), CDC (interfaces 1 and 2) = 4Eh CDC (interfaces 0 and 1), HFC only (interface 2) = 4Fh

TABLE 79: HFC PRODUCT ID MSB

HFC_PID_MSB (42D9h)			HFC Product ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PID_MSB	R/W	Most Significant Byte of the HFC Product ID. This is a 16-bit value that uniquely identifies this HFC device.

TABLE 80: HFC DEVICE ID LSB

HFC_DID_LSB (42DAh)			HFC Device ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_DID_LSB	R/W	Least Significant Byte of the HFC Device ID descriptor Default value varies and depends on the product code.

TABLE 81: HFC DEVICE ID MSB

HFC_DID_MSB (42DBh)			HFC Device ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	HFC_DID_MSB	R/W	Most Significant Byte of the HFC Device ID descriptor Default value varies and depends on the product code.

TABLE 82: HFC MANUFACTURER STRING INDEX

HFC_MFR_STR_INDEX (42DCh)			HFC iManufacturer String Index
Bit	**Name**	**R/W**	**Description**
7:0	HFC_MFR_STR_INDEX	R/W	iManufacturer string index Can be 00- disabled or any free value of 01, 02, or 03.

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TABLE 83: HFC PRODUCT STRING INDEX

HFC_PROD_STR_INDEX (42DDh)			HFC iProduct String Index
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PROD_STR_INDEX	R/W	iProduct string index Can be 00- disabled or any free value of 01, 02, or 03.

TABLE 84: HFC SERIAL STRING INDEX

HFC_SER_STR_INDEX (42DEh)			HFC iSerial String Index
Bit	**Name**	**R/W**	**Description**
7:0	HFC_SER_STR_INDEX	R/W	iSerial string index Can be 00- disabled or any free value of 01, 02, or 03.

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TABLE 85: USB2 HUB STRING CONTAINER

USB2_STRING_CONT (4325h-43A6h)			USB2 Hub String Container
Bit	**Name**	**R/W**	**Description**
1024:32	USB2_STRING_CONT	R/W	Container for the HFC string data including Product String, Manufacturere String, and Serial strings.The maximum combined character count for all 3 strings is 90. The String for each index has to be formatted as per the USB Specification requirements on string descriptor (Unicode format). The Index for each String type is assigned in **MFR_STR_INDEX (3013h)**, **PRD_STR_INDEX (3014h)**, and **SER_STR_INDEX (3015h)** registers. Each index must also be given a pointer to the memory offset within this container in **USB2_STR_INDX1_PNTR (426Dh-4272h)**, **USB2_STR_INDX2_PNTR (4273h-4278h)**, and **USB2_STR_INDX3_PNTR (4279h-427Eh)**. A typical implementation for USB2 string descriptors assigns the manufacturer string as index 1, product string as index 2, and serial string as index 3. Index 0 should not be modified. To skip/disable a string descriptor for index i (where i = 1, 2, & 3), set the string descriptor length to 0x02, but always keep the following 03h byte. The formatting for this container is as: • STRING_LEN_1 (1 byte) - total length of string data + 2 • Always 03h - String Descriptor Type • STRING_DATA_1 (of length STRING_LEN_1 minus 2) • STRING_LEN_1 (1 byte) - total length of string data + 2 • Always 03h - String Descriptor Type • STRING_DATA_1 (of length STRING_LEN_1 minus 2) • STRING_LEN_1 (1 byte) - total length of string data + 2 • Always 03h - String Descriptor Type • STRING_DATA_1 (of length STRING_LEN_1 minus 2) **Note:** An unused string shall have STRING_LEN_x = 02h.
31:16	STRING_DATA_0	R/W	USB-IF Language Identifier. Default is English (United States) = 0409h.
15:8	STRING_LEN_0	R/W	Always 03h - String Descriptor Type
7:0	STRING_LEN_0	R/W	Always 04h

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TABLE 86: USB3 STRING INDEX 2 POINTER

USB3_STR_INDX2_PNTR (4418Dh-441Bh)			USB3 String Index 2 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
31:24	STR_CONT_OFFSET_L	R/W	Container Offset Pointer LSB Memory pointer to the Unicode data within in the **USB3_STRING_CONT (43ACh-43A6h)** memory range for the string assigned as Index 1. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**.
23:15	STR_CONT_OFFSET_M	R/W	Container Offset Pointer MSB Memory pointer to the Unicode data within in the **USB3_STRING_CONT (43ACh-43A6h)** memory range minus **4400h** for the string assigned as Index 1. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**.
14:0	STRING_LEN	R/W	Total length of Unicode string data

TABLE 87: USB3 STRING INDEX 3 POINTER

USB3_STR_INDX3_PNTR (441Ch-441Fh)			USB3 String Index 3 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
31:24	STR_CONT_OFFSET_L	R/W	Container Offset Pointer LSB Memory pointer to the Unicode data within in the **USB3_STRING_CONT (43ACh-43A6h)** memory range for the string assigned as Index 2. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**.

TABLE 87: USB3 STRING INDEX 3 POINTER (CONTINUED)

USB3_STR_INDX3_PNTR (441Ch-441Fh)			USB3 String Index 3 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
23:15	STR_CONT_OFFSET_M	R/W	Container Offset Pointer MSB Memory pointer to the Unicode data within in the **USB3_STRING_CONT (43ACh-43A6h)** memory range for the string assigned as Index 2. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**.
14:0	STRING_LEN	R/W	Total length of Unicode string data

TABLE 88: USB3 STRING INDEX 4 POINTER

USB3_STR_INDX4_PNTR (4420h-4423h)			USB3 String Index 4 Descriptor Pointer
Bit	**Name**	**R/W**	**Description**
31:24	STR_CONT_OFFSET_L	R/W	Container Offset Pointer LSB Memory pointer to the Unicode data within in the **USB3_STRING_CONT (43ACh-43A6h)** memory range for the string assigned as Index 3. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**.
23:15	STR_CONT_OFFSET_M	R/W	Container Offset Pointer MSB Memory pointer to the Unicode data within in the **USB3_STRING_CONT (43ACh-43A6h)** memory range for the string assigned as Index 3. A string may be either a Manufacturer String, a Product String, or a Serial String. This assignment is made in **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**.
14:0	STRING_LEN	R/W	Total length of Unicode string data

TABLE 89: USB 3.1 GEN 1 HUB BCDUSB LSB

USB3_BCDUSB_LSB (4440h)			USB 3.1 Gen 1 Hub BCDUSB LSB
Bit	**Name**	**R/W**	**Description**
7:0	BCDUSB_LSB	R/W	Least Significant Byte of the USB3.1 Gen 1 bcdUSB descriptor Default is 02h.

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TABLE 90: USB 3.1 GEN 1 HUB BCDUSB MSB

USB3_BCDUSB_MSB (4441h)			HFC BCDUSB MSB
Bit	**Name**	**R/W**	**Description**
7:0	BCDUSB_MSB	R/W	Most Significant Byte of the HFC bcdUSB descriptor Default is 03h.

TABLE 91: USB 3.1 GEN 1 HUB VENDOR ID LSB

USB3_VIDL (4448h)			USB 3.1 Gen 1 Hub Vendor ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	VID_LSB	R/W	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Interface Forum). **Note:** If this register is modified, the contents of the GPIO 1-7 Pull-Down Register register must also be identically modified.

TABLE 92: USB 3.1 GEN 1 HUB VENDOR ID MSB

USB3_VIDM (4449h)			USB 3.1 Gen 1 Hub Vendor ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	VID_MSB	R/W	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Interface Forum). **Note:** If this register is modified, the contents of the USB 2.0 Hub Vendor ID MSB register must also be identically modified.

TABLE 93: USB 3.1 GEN 1 HUB PRODUCT ID LSB

USB3_PIDL (444Ah)			USB 3.1 Gen 1 Hub Product ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	PID_LSB	R/W	Least Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 94: USB 3.1 GEN 1 HUB PRODUCT ID MSB

USB3_PIDM (444Bh)			USB 3.1 Gen 1 Hub Product ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	PID_MSB	R/W	Most Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign to uniquely identify this particular product (assigned by OEM).

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TABLE 95: USB 3.1 GEN 1 HUB DEVICE ID LSB

USB3_DIDL (444Ch)			USB 3.1 Gen 1 Hub Product ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	DID_LSB	R/W	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 96: USB 3.1 GEN 1 HUB DEVICE ID MSB

USB3_DIDM (444Dh)			USB 3.1 Gen 1 Hub Product ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	DID_MSB	R/W	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 97: USB 3.1 GEN 1 MANUFACTURER STRING INDEX

USB3_MFR_STR_INDEX (444Eh)			USB3.1 Gen 1 iManufacturer String Index
Bit	**Name**	**R/W**	**Description**
7:0	USB3_MFR_STR_INDEX	R/W	iManufacturer string index Can be 00- disabled or any free value of 02, 03, or 04. Typically, 02 is selected for manufacturer string. Index 01 should not be modified.

TABLE 98: USB 3.1 GEN 1 PRODUCT STRING INDEX

USB3_PROD_STR_INDEX (444Fh)			USB3.1 Gen 1 iProduct String Index
Bit	**Name**	**R/W**	**Description**
7:0	USB3_PROD_STR_INDEX	R/W	iProduct string index Can be 00- disabled or any free value of 02, 03, or 04. Typically, 03 is selected for manufacturer string. Index 01 should not be modified.

TABLE 99: USB 3.1 GEN 1 SERIAL STRING INDEX

USB3_SER_STR_INDEX (4450h)			USB3.1 Gen 1 iSerial String Index
Bit	**Name**	**R/W**	**Description**
7:0	USB3_SER_STR_INDEX	R/W	iSerial string index Can be 00- disabled or any free value of 02, 03, or 04. Typically, 04 is selected for manufacturer string. Index 01 should not be modified.

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TABLE 100: USB3 HUB MAX POWER DESCRIPTOR

USB3_HUB_MAX_POWER OFFSET: 8060h RESET = 01h			USB3 Hub Max Power Descriptor
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_MAX_POWER	R/W	Maximum power consumption of the hub from VBUS when fully operational. 2 mA intervals The default setting for this value is 2 mA (indicating almost no power consumption from VBUS), as most USB3 hub applications are not bus-powered applications.

TABLE 101: USB 3.1 GEN 1 NUMBER OF PORTS

USB3_NBR_PRTS (44A2h)			USB 3.1 Gen 1 Number of Ports
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	Number of Ports	R/W	111 = Reserved 110 = Reserved 101 = Reserved 100 = Four Ports Enabled 011 = Three Ports Enabled 010 = Two Ports Enabled 001 = One Port Enabled 000 = No Ports Enabled **Note:** If this register is modified, the specific USB 3.1 Gen 1 ports must be disabled in USB 3.1 Gen 1 Port 1 Configuration Select, USB 3.1 Gen 1 Port 2 Configuration Select, USB 3.1 Gen 1 Port 3 Configuration Select, and USB 3.1 Gen 1 Port 4 Configuration Select. If this register is modified, the USB 2.0 Hub equivalent must also be modified in the USB 3.1 Gen 1 Port 1 Configuration Select, USB 3.1 Gen 1 Port 2 Configuration Select, USB 3.1 Gen 1 Port 3 Configuration Select, and USB 3.1 Gen 1 Port 4 Configuration Select registers. The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 1/Port 2 Disable and USB 2.0 Port 3/Port 4 Disable registers.

TABLE 102: USB 3.1 GEN 1 HUB COMPOUND DEVICE

USB3_COMPOUND (44A3h)			USB 3.1 Gen 1 Hub Compound Device
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
4:3	OVER_CURRENT_MODE	R/W	00 = Global overcurrent protection. The hub reports overcurrent as a summation of current draw of all ports, without a breakdown of individual port overcurrent status. 01b = Individual port overcurrent protection. The hub reports overcurrent on a per-port basis. Each port has an overcurrent status. 1Xb = No overcurrent protection. This option is allowed only for bus-powered hubs that do not implement overcurrent protection.
2	COMPOUND_DEVICE	R/W	0b = The hub is not part of a compound device. 1b = The hub is part of a compound device. A USB3 device is permanently attached to one or more of the USB3 ports.
1:0	LOGICAL_POWER_MODE	R/W	00 = Ganged power switching. All ports power at once from a single control signal. 01b = Individual port power switching. Each port has an individual power switch with individual control signal. 1Xb = Reserved

TABLE 103: USB3.1 GEN 1 HUB POWER TO POWER GOOD DESCRIPTOR

USB3_HUB_PWR2PWRGOOD (44A5h)			USB3 Hub Power to Power Good Descriptor
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_PWR2PWRGOOD	R/W	Time in 2-ms intervals from the time the power-on sequence begins on a port until power is good on that port. The USB system software uses this value to determine how long to wait before accessing a powered-on port. This value should be set to zero if power-switching is not supported in the system design. **Note:** A ‘zero’ setting should never be used on a design that includes Type-C ports.

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TABLE 104: USB 3.1 GEN 1 HUB NON REMOVABLE DEVICE

USB3_NRD (44AAh)			USB 3.1 Gen 1 Hub Non-Removable Device
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4:1	NR_DEVICE	R/W	Non-Removable Device: Indicates which ports include non-removable devices. '0' = port is removable, '1' = port is non-removable. Informs the host if one of the active ports has a permanent device that is undetachable from the hub. The ports may also be configured as non-removable using the hardware strapping option described in section 3.4.3 of the *USB57x4 Data Sheet*. Bit 4 = 1; LOGICAL Port 4 is non-removable. Bit 3 = 1; LOGICAL Port 3 is non-removable. Bit 2 = 1; LOGICAL Port 2 is non-removable. Bit 1 = 1; LOGICAL Port 1 is non-removable. If this register is modified, the USB 2.0 Hub equivalent must also be modified in the USB 2.0 Hub Non-Removable Device register. **Note:** Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.
0	Reserved	R	Reserved

TABLE 105: USB3 HUB STRING CONTAINER

USB3_STRING_CONT (43ACh-43A6h)			USB3 Hub String Container
Bit	**Name**	**R/W**	**Description**
1024:32	USB2_STRING_CONT	R/W	Container for the HFC string data including Product String, Manufacturer String, and Serial strings. The maximum combined character count for all 3 strings is 90. The String for each index has to be formatted as per the USB Specification requirements on string descriptor (Unicode format). The Index for each String type is assigned in registers **USB3_HUB_MFR_STR_INDEX (444Eh)**, **USB3_HUB_PRD_STR_INDEX (444Fh)**, and **USB3_HUB_SER_STR_INDEX (444Gh)**. Each index must also be given a pointer to the memory offset within this container in **USB3_STR_INDX2_PNTR (4418h-441Bh)**, **USB3_STR_INDX3_PNTR (441Ch-441Fh)**, and **USB3_STR_INDX4_PNTR (4420h-4223h)**. A typical implementation for USB3 string descriptors assigns the manufacturer string as index 2, product string as index 3, and serial string as index 4. Index 0 and 1 should not be modified. To skip/disable a string descriptor for index i (where i = 2, 3, and 4), set the string descriptor length to 0x02, but always keep the following 03h byte. The formatting for this container is as: • STRING_LEN_1 (1 byte) - total length of string data + 2 • Always 03h - String Descriptor Type • STRING_DATA_1 (of length STRING_LEN_1 minus 2) • STRING_LEN_2 (1 byte) - total length of string data + 2 • Always 03h - String Descriptor Type • STRING_DATA_2 (of length STRING_LEN_1 minus 2) • STRING_LEN_3 (1 byte) - total length of string data + 2 • Always 03h - String Descriptor Type • STRING_DATA_3 (of length STRING_LEN_1 minus 2) **Note:** An unused string shall have STRING_LEN_x = 02h.
31:16	STRING_DATA_0	R/W	USB-IF Language Identifier Default is English (United States) = 0409h.
15:8	STRING_LEN_0	R/W	Always 03h - String Descriptor Type
7:0	STRING_LEN_0	R/W	Always 04h’

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TABLE 106: USB3 PORT 0 TX PRE-DRIVER

SS_P0_AFE_TEST_IN4 (6086h)			USB3 PHYSICAL Port 0 TX Pre-Driver
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	PHYSICAL Port 0 Transmitter Pre-Driver current adjust 00: 100 uA (default biasing) 01: 125 uA 10: 87.5 uA 11: 112.5 uA
0	Reserved	R	Reserved. Do not modify.

TABLE 107: USB PORT 0 BOOST REGISTER

HS_P0_BOOST (60CAh)			PHYSICAL USB Port 0 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% **Note:** If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 108: USB PORT 0 VARISENSE REGISTER

HS_P0_VSENSE (60CCh)			PHYSICAL USB Port 0 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625-mV threshold (+8.6%) 10b: 675-mV threshold (+17%) 11b: 700-mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100-mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 109: USB3 PORT 0 LTSSM STATE

SS_P0_LTSSM_STATE (61C0h)			USB3 PHYSICAL Port 0 LTSSM State
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	PHYSICAL Port 0 LTSSM state 0000b - U0 (no sub-states) 0001b - U1 (no sub-states) 0010b - U2 (no sub-states) 0011b - U3 (no sub-states) 0100b - SIS.Disabled (see sub-state below) 0101b - Rx.Detect (see sub-state below) 0110b - SS.Inactive (see sub-state below) 0111b - Polling (see sub-state below) 1000b - Recovery (see sub-state below) 1001b - HotReset (see sub-state below) 1010b - Compliance (no sub-states) 1011b - Loopback (no sub-states)
3	Reserved	R	Always read ‘0’

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TABLE 109: USB3 PORT 0 LTSSM STATE (CONTINUED)

SS_P0_LTSSM_STATE (61C0h)			USB3 PHYSICAL Port 0 LTSSM State
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	PHYSICAL Port 0 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b - SSD.Power3 001b - SSD.Power3A 010b - SSD.Main Rx.Detect sub-states: 000b - Rx.Detect.Init 001b - Rx.Detect.Power2 010b - Rx.Detect.Reset 011b - Rx.Detect.Reset_T 100b - Rx.Detect.Active0 101b - Rx.Detect.Active1 110b - Rx.Detect.Quiet SS.Inactive sub-states: 000b - SS.Inactive.Reset 001b - SS.Inactive.Power2 010b - SS.Inactive.Quite0 011b - SS.Inactive.Quiet1 100b - SS.Inactive.Disconnect.Detect0 100b - SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b - Polling.Reset 001b - Polling.Power0 010b - Polling.LFPS 011b - Polling.RxEQ 100b - Polling.Active 101b - Polling.Configuration 110b - Polling.Idle Recovery sub-states: 000b - Recovery.Reset 001b - Recovery.Power0 010b - Recovery.Active 011b - Recovery.Cofiguration 100b - Recovery.Idle HotReset sub-states: 000b - HotReset.Reset 001b - HotReset.Go 010b - HotReset.Active1 011b - HotReset.Active2 100b - HotReset.Exit

TABLE 110: USB3 PORT 0 TX_MARGIN

SS_P0_TEST_PIPE_CTL_0 (61D0h)			USB3 PHYSICAL Port 0 TX Margin
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always read '0' (do not modify)
6:4	Length	R/W	PHYSICAL Port 0 transmitter biasing and amplitude adjust 000: 0% change (default) 001: +11% 010: +21% 011: +33% 100: -67% 101: -64% 110: -61% 111: -57%
3:0	Reserved	R	Always read '0' (do not modify)

TABLE 111: USB3 PORT 1 TX PRE-DRIVER

SS_P1_AFE_TEST_IN4 (6486h)			USB3 PHYSICAL Port 1 TX Pre-Driver
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	PHYSICAL Port 1 Transmitter Pre-Driver current adjust 00: 100uA (default biasing) 01: 125uA 10: 87.5uA 11: 112.5uA
0	Reserved	R	Reserved. Do not modify.

TABLE 112: USB PORT 1 BOOST REGISTER

HS_P1_BOOST (64CAh)			PHYSICAL USB Port 1 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% **Note:** Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port num-

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ber is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 113: USB PORT 1 VARISENSE REGISTER

HS_P1_VSENSE (64CCh)			PHYSICAL USB Port 1 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625-mV threshold (+8.6%) 10b: 675-mV threshold (+17%) 11b: 700-mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100-mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 114: USB3 PORT 1 LTSSM STATE

SS_P1_LTSSM_STATE (65C0h)			USB3 PHYSICAL Port 1 LTSSM State
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	PHYSICAL Port 1 LTSSM state. 0000b - U0 (no sub-states) 0001b - U1 (no sub-states) 0010b - U2 (no sub-states) 0011b - U3 (no sub-states) 0100b - SIS.Disabled (see sub-state below) 0101b - Rx.Detect (see sub-state below) 0110b - SS.Inactive (see sub-state below) 0111b - Polling (see sub-state below) 1000b - Recovery (see sub-state below) 1001b - HotReset (see sub-state below) 1010b - Compliance (no sub-states) 1011b - Loopback (no sub-states)
3	Reserved	R	Always read ‘0’

TABLE 114: USB3 PORT 1 LTSSM STATE (CONTINUED)

SS_P1_LTSSM_STATE (65C0h)			USB3 PHYSICAL Port 1 LTSSM State
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	PHYSICAL Port 1 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b - SSD.Power3 001b - SSD.Power3A 010b - SSD.Main Rx.Detect sub-states: 000b - Rx.Detect.Init 001b - Rx.Detect.Power2 010b - Rx.Detect.Reset 011b - Rx.Detect.Reset_T 100b - Rx.Detect.Active0 101b - Rx.Detect.Active1 110b - Rx.Detect.Quiet SS.Inactive sub-states: 000b - SS.Inactive.Reset 001b - SS.Inactive.Power2 010b - SS.Inactive.Quite0 011b - SS.Inactive.Quiet1 100b - SS.Inactive.Disconnect.Detect0 100b - SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b - Polling.Reset 001b - Polling.Power0 010b - Polling.LFPS 011b - Polling.RxEQ 100b - Polling.Active 101b - Polling.Configuration 110b - Polling.Idle Recovery sub-states: 000b - Recovery.Reset 001b - Recovery.Power0 010b - Recovery.Active 011b - Recovery.Cofiguration 100b - Recovery.Idle HotReset sub-states: 000b - HotReset.Reset 001b - HotReset.Go 010b - HotReset.Active1 011b - HotReset.Active2 100b - HotReset.Exit

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TABLE 115: USB3 PORT 1 TX_MARGIN

SS_P1_TEST_PIPE_CTL_0 (65D0h)			USB3 PHYSICAL Port 1 TX Margin
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always read '0' (do not modify)
6:4	Length	R/W	PHYSICAL Port 1 transmitter biasing and amplitude adjust 000: 0% change (default) 001: +11% 010: +21% 011: +33% 100: -67% 101: -64% 110: -61% 111: -57%
3:0	Reserved	R	Always read '0' (do not modify)

TABLE 116: USB3 PORT 2 TX PRE-DRIVER

SS_P2_AFE_TEST_IN4 (6886h)			USB3 PHYSICAL Port 2 TX Pre-Driver
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	PHYSICAL Port 2 Transmitter Pre-Driver current adjust 00: 100 uA (default biasing) 01: 125 uA 10: 87.5 uA 11: 112.5 uA
0	Reserved	R	Reserved. Do not modify.

TABLE 117: USB PORT 2 BOOST REGISTER

HS_P2_BOOST (68CAh)			PHYSICAL USB Port 2 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% **Note:** If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 118: USB PORT 2 VARISENSE REGISTER

HS_P2_VSENSE (68CCh)			PHYSICAL USB Port 2 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625-mV threshold (+8.6%) 10b: 675-mV threshold (+17%) 11b: 700-mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100-mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 119: USB3 PORT 2 LTSSM STATE

SS_P2_LTSSM_STATE (69C0h)			USB3 PHYSICAL Port 2 LTSSM State
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	PHYSICAL Port 2 LTSSM state 0000b - U0 (no sub-states) 0001b - U1 (no sub-states) 0010b - U2 (no sub-states) 0011b - U3 (no sub-states) 0100b - SIS.Disabled (see sub-state below) 0101b - Rx.Detect (see sub-state below) 0110b - SS.Inactive (see sub-state below) 0111b - Polling (see sub-state below) 1000b - Recovery (see sub-state below) 1001b - HotReset (see sub-state below) 1010b - Compliance (no sub-states) 1011b - Loopback (no sub-states)
3	Reserved	R	Always read ‘0’

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TABLE 119: USB3 PORT 2 LTSSM STATE (CONTINUED)

SS_P2_LTSSM_STATE (69C0h)			USB3 PHYSICAL Port 2 LTSSM State
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	PHYSICAL Port 2 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b - SSD.Power3 001b - SSD.Power3A 010b - SSD.Main Rx.Detect sub-states: 000b - Rx.Detect.Init 001b - Rx.Detect.Power2 010b - Rx.Detect.Reset 011b - Rx.Detect.Reset_T 100b - Rx.Detect.Active0 101b - Rx.Detect.Active1 110b - Rx.Detect.Quiet SS.Inactive sub-states: 000b - SS.Inactive.Reset 001b - SS.Inactive.Power2 010b - SS.Inactive.Quite0 011b - SS.Inactive.Quiet1 100b - SS.Inactive.Disconnect.Detect0 100b - SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b - Polling.Reset 001b - Polling.Power0 010b - Polling.LFPS 011b - Polling.RxEQ 100b - Polling.Active 101b - Polling.Configuration 110b - Polling.Idle Recovery sub-states: 000b - Recovery.Reset 001b - Recovery.Power0 010b - Recovery.Active 011b - Recovery.Cofiguration 100b - Recovery.Idle HotReset sub-states: 000b - HotReset.Reset 001b - HotReset.Go 010b - HotReset.Active1 011b - HotReset.Active2 100b - HotReset.Exit

TABLE 120: USB3 PORT 2 TX_MARGIN

SS_P2_TEST_PIPE_CTL_0 (69D0h)			USB3 PHYSICAL Port 2 TX Margin
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always read '0' (do not modify)
6:4	Length	R/W	PHYSICAL Port 2 transmitter biasing and amplitude adjust 000: 0% change (default) 001: +11% 010: +21% 011: +33% 100: -67% 101: -64% 110: -61% 111: -57%
3:0	Reserved	R	Always read '0' (do not modify)

TABLE 121: USB3 PORT 3 TX PRE-DRIVER

SS_P3_AFE_TEST_IN4 (6C86h)			USB3 PHYSICAL Port 3 TX Pre-Driver
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	PHYSICAL Port 3 Transmitter Pre-Driver current adjust 00: 100 uA (default biasing) 01: 125 uA 10: 87.5 uA 11: 112.5 uA
0	Reserved	R	Reserved. Do not modify.

TABLE 122: USB PORT 3 BOOST REGISTER

HS_P3_BOOST (6CCAh)			PHYSICAL USB Port 3 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% **Note:** If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port num-

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ber is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 123: USB PORT 3 VARISENSE REGISTER

HS_P3_VSENSE (6CCCh)			PHYSICAL USB Port 3 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625-mV threshold (+8.6%) 10b: 675-mV threshold (+17%) 11b: 700-mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100-mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 124: USB3 PORT 3 LTSSM STATE

SS_P3_LTSSM_STATE (6DC0h)			USB3 PHYSICAL Port 3 LTSSM State
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	PHYSICAL Port 3 LTSSM state. 0000b - U0 (no sub-states) 0001b - U1 (no sub-states) 0010b - U2 (no sub-states) 0011b - U3 (no sub-states) 0100b - SIS.Disabled (see sub-state below) 0101b - Rx.Detect (see sub-state below) 0110b - SS.Inactive (see sub-state below) 0111b - Polling (see sub-state below) 1000b - Recovery (see sub-state below) 1001b - HotReset (see sub-state below) 1010b - Compliance (no sub-states) 1011b - Loopback (no sub-states)
3	Reserved	R	Always read ‘0’

TABLE 124: USB3 PORT 3 LTSSM STATE (CONTINUED)

SS_P3_LTSSM_STATE (6DC0h)			USB3 PHYSICAL Port 3 LTSSM State
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	PHYSICAL Port 3 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b - SSD.Power3 001b - SSD.Power3A 010b - SSD.Main Rx.Detect sub-states: 000b - Rx.Detect.Init 001b - Rx.Detect.Power2 010b - Rx.Detect.Reset 011b - Rx.Detect.Reset_T 100b - Rx.Detect.Active0 101b - Rx.Detect.Active1 110b - Rx.Detect.Quiet SS.Inactive sub-states: 000b - SS.Inactive.Reset 001b - SS.Inactive.Power2 010b - SS.Inactive.Quite0 011b - SS.Inactive.Quiet1 100b - SS.Inactive.Disconnect.Detect0 100b - SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b - Polling.Reset 001b - Polling.Power0 010b - Polling.LFPS 011b - Polling.RxEQ 100b - Polling.Active 101b - Polling.Configuration 110b - Polling.Idle Recovery sub-states: 000b - Recovery.Reset 001b - Recovery.Power0 010b - Recovery.Active 011b - Recovery.Cofiguration 100b - Recovery.Idle HotReset sub-states: 000b - HotReset.Reset 001b - HotReset.Go 010b - HotReset.Active1 011b - HotReset.Active2 100b - HotReset.Exit

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TABLE 125: USB3 PORT 3 TX_MARGIN

SS_P3_TEST_PIPE_CTL_0 (6DD0h)			USB3 PHYSICAL Port 3 TX Margin
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always read '0' (do not modify)
6:4	Length	R/W	PHYSICAL Port 3 transmitter biasing and amplitude adjust 000: 0% change (default) 001: +11% 010: +21% 011: +33% 100: -67% 101: -64% 110: -61% 111: -57%
3:0	Reserved	R	Always read '0' (do not modify)

TABLE 126: USB3 PORT 4 TX PRE-DRIVER

SS_P4_AFE_TEST_IN4 (7086h)			USB3 PHYSICAL Port 4 TX Pre-Driver
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	PHYSICAL Port 4 Transmitter Pre-Driver current adjust 00: 100 uA (default biasing) 01: 125 uA 10: 87.5 uA 11: 112.5 uA
0	Reserved	R	Reserved. Do not modify.

TABLE 127: USB PORT 4 BOOST REGISTER

HS_P4_BOOST (70CAh)			PHYSICAL USB Port 4 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% **Note:** Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port num-

ber is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 128: USB PORT 4 VARISENSE REGISTER

HS_P4_VSENSE (70CCh)			PHYSICAL USB Port 4 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625-mV threshold (+8.6%) 10b: 675-mV threshold (+17%) 11b: 700-mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000: Nominal 100-mV Trip Point 001: Decrease by 12.5 mV 010: Decrease by 25 mV 011: Decrease by 37.5 mV 100: Decrease by 50 mV 101: Decrease by 62.5 mV 110: Increase by 25 mV 111: Increase by 12.5 mV

Note: Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. LOGICAL port numbering is the numbering as communicated to the USB host; it is the end result after any port number remapping or port disabling. PHYSICAL port number is the port number with respect to the physical PHY on the chip; PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. See Section 8.0, Physical and Logical Port Mapping for details on the LOGICAL vs. PHYSICAL mapping for each device in this family.

TABLE 129: USB3 PORT 4 LTSSM STATE

SS_P4_LTSSM_STATE (71C0h)			USB3 PHYSICAL Port 4 LTSSM State
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	PHYSICAL Port 4 LTSSM state. 0000b - U0 (no sub-states) 0001b - U1 (no sub-states) 0010b - U2 (no sub-states) 0011b - U3 (no sub-states) 0100b - SIS.Disabled (see sub-state below) 0101b - Rx.Detect (see sub-state below) 0110b - SS.Inactive (see sub-state below) 0111b - Polling (see sub-state below) 1000b - Recovery (see sub-state below) 1001b - HotReset (see sub-state below) 1010b - Compliance (no sub-states) 1011b - Loopback (no sub-states)
3	Reserved	R	Always read ‘0’

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TABLE 129: USB3 PORT 4 LTSSM STATE (CONTINUED)

SS_P4_LTSSM_STATE (71C0h)			USB3 PHYSICAL Port 4 LTSSM State
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	PHYSICAL Port 4 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b - SSD.Power3 001b - SSD.Power3A 010b - SSD.Main Rx.Detect sub-states: 000b - Rx.Detect.Init 001b - Rx.Detect.Power2 010b - Rx.Detect.Reset 011b - Rx.Detect.Reset_T 100b - Rx.Detect.Active0 101b - Rx.Detect.Active1 110b - Rx.Detect.Quiet SS.Inactive sub-states: 000b - SS.Inactive.Reset 001b - SS.Inactive.Power2 010b - SS.Inactive.Quite0 011b - SS.Inactive.Quiet1 100b - SS.Inactive.Disconnect.Detect0 100b - SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b - Polling.Reset 001b - Polling.Power0 010b - Polling.LFPS 011b - Polling.RxEQ 100b - Polling.Active 101b - Polling.Configuration 110b - Polling.Idle Recovery sub-states: 000b - Recovery.Reset 001b - Recovery.Power0 010b - Recovery.Active 011b - Recovery.Cofiguration 100b - Recovery.Idle HotReset sub-states: 000b - HotReset.Reset 001b - HotReset.Go 010b - HotReset.Active1 011b - HotReset.Active2 100b - HotReset.Exit

TABLE 130: USB3 PORT 4 TX_MARGIN

SS_P4_TEST_PIPE_CTL_0 (71D0h)			USB3 PHYSICAL Port 4 TX Margin
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always read ‘0’ (do not modify)
6:4	Length	R/W	PHYSICAL Port 4 transmitter biasing and amplitude adjust 000: 0% change (default) 001: +11% 010: +21% 011: +33% 100: -67% 101: -64% 110: -61% 111: -57%
3:0	Reserved	R	Always read ‘0’ (do not modify)

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5.0 USING GPIOS

The USB5734 and USB5744 hubs each have GPIOs that can be configured as outputs or inputs. The hub must be configured appropriately before the GPIOs can be used. Table 131 defines all of the available GPIOs and any configuration requirements.

TABLE 131: GPIO CONFIGURATION REQUIREMENTS

GPIO	USB5734 Pin	USB5744 Pin	Configuration Requirements
GPIO1	50	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO2	39	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO3	40	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO4	42	38	Do not attach SPI EEPROM device.
GPIO5	43	39	Do not attach SPI EEPROM device.
GPIO6	46	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO7	45	41	Do not attach SPI EEPROM device.
GPIO8	47	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO9	44	40	Do not attach SPI EEPROM device.
GPIO10	49	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO11	16	—	Use the CFG_STRAP pin to Configure Hub into Configuration 4 - GPIO mode.
GPIO17	38	36	Disable Physical Port 1 (Registers 30FBh, 3C00h, and 44A2h) and Disable OCS1 (Register 3C20h) function in configuration.
GPIO18	37	35	Disable Physical Port 2 (Registers 30FBh, 3C04h, and 44A2h) and Disable OCS2 (Register 3C24h) function in configuration.
GPIO19	36	34	Disable Physical Port 3 (Registers 30FCh, 3C08h, and 44A2h) and Disable OCS3 (Register 3C28h) function in configuration.
GPIO20	34	32	Disable Physical Port 4 (Registers 30FCh, 3C0Ch, and 44A2h) and Disable OCS4 (Register 3C2Ch) function in configuration.

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6.0 OTP CONFIGURATION

The OTP memory can be programmed through the SMBus interface in the SOC_CONFIG stage (during start-up). The OTP memory is configured as a series of commands that manipulate the configuration registers. The USB5734, USB5744, and USB5742 hubs have a total of 8 kB of OTP memory space, and each byte of OTP memory may be written to only once. The OTP memory space can be successively written to (each programming instance appends the new command to the bottom of the OTP memory space) until the space is completely filled.

During the HUB_CONFIG stage, temporary OTP configuration registers are written to. The contents in the OTP configuration registers are then permanently loaded to the OTP memory space after sending a special OTP program command. These registers permanently change the default behavior of the hub during normal operation. These commands are stored into the OTP memory as shown in Figure 4.

Note: The hub OTP memory contains some default configuration data. Different product codes may include different default OTP contents. Your Microchip support representative can provide the default OTP content for specific devices upon request.

6.1 Configuration Commands

TABLE 132: OTP STORAGE COMMANDS

Command	OPCODE	Length	Description
NULL	00h	N/A	No action; advance memory counter by 1 and move to the next instruction.
MODIFY_BYTES	01h-7Fh	OPCODE	Modifies the following bytes starting at the current memory address for length = OPCODE. The previously used SET_MODE command is used for selecting the bit operation. The default MODE is WRITE_BYTES if there is no preceding SET_MODE command.
SET_MEMORY ADDRESS	80h XXh XXh	N/A	Load the MEMORY_ADDRESS register with the two XXh XXh bytes. Example: 80h 30h 00h sets the memory address to 3000h.
SKIP_MEMORY_WRITE	81h-FDh	OPCODE [6:0]	Skip the length number of bytes starting at the location of the MEMORY_ADDRESS register. At the end of the operation, the MEMORY_ADDRESS register is incremented by length = OPCODE[6:0].
SET_MODE_WRITE_BYTE	FEh 00	N/A	If the byte following SET_MODE = 00h, all writes replace the memory value at that location.
SET_MODE_SET_BITS	FEh 01h	N/A	If the byte following SET_MODE = 01h, all writes are OR'ed in. This is a mechanism to set the selected bits in a register without changing the others. Set the bits to be set.
SET_MODE_CLEAR_BITS	FEh 02h	N/A	If the byte following SET_MODE = 02h, all writes are NAND'ed in. This is a mechanism to clear the selected bits in a register without changing the others. Set the bits to be cleared.
STOP	FFh	N/A	After the storage commands are complete, this indicates the termination of the command sequence.

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6.2 Example

If it is desired to have the hub start up in the Flexed state, the user should modify configuration register 411Ah. The command sequence is as follows:

TABLE 133: EXAMPLE OTP CONFIGURATION COMMAND SEQUENCE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	41h	Setting address MSB to 41h (target register **41**1Ah)
3	1Ah	Setting address LSB to 1Ah (target register 41**1A**h)
4	FEh	BIT Command
5	01h	SET_BIT command, only the selected bits will be set.
6	01h	DATA_LENGTH of 1 byte
7	40h	Only set the FLEXCONNECT bit in this register
8	FFh	STOP command

6.3 Writing OTP Data

To program the configuration commands to the OTP memory space (via SMBus commands during the SOC_CFG stage), the following steps must be followed:

4. Write **C1h** to register **0860h** to enable the Hub Feature Controller.

```
5A 00 00 05 00 01 08 60 C1
5A 99 37 00
```

5. Write **01h** to register **0A00h** to resume internal code execution.

```
5A 00 00 05 00 01 0A 00 01
5A 99 37 00
```

6. Write **Config Data Payload** starting at register **8000h**.

```
5A 00 00 DP 00 DL 80 00 d1 d2 d3 ... d(n-2) d(n-1) d(n) FF
5A 99 37 00
```

Where:

DL = Total Data Payload Length (not including terminal FF byte)

DP = Total Data Payload Length + 4

D1-D(n) = Data payload

Note: The maximum data payload of a single SMBus write command is 256 bytes. If the OTP patch is larger than 256 bytes, a second SMBus write command beginning at register **4900h** is required (and to **5000h**, **5100h**, **5200h**, and so on, as needed).

7. Write 04h to register 4800h to instruct the hub to load the new OTP data payload to the next available memory space.

```
5A 00 00 05 00 01 48 00 03
5A 99 37 00
```

8. Write the **Total OTP Patch Length** to register **4803:4h** to instruct the hub to load new OTP data payload to the next available memory space. Note: 4803 is the MSB, 4804 is the LSB.

```
5A 00 00 06 00 02 48 03 TL(msb) TL(lsb)
5A 99 37 00
```

Where:

DL = Total OTP Patch Length

9. Send the OTP Program Command **99 33 00**.

```
5A 99 33 00
```

10. Read register **414Ch** to confirm the OTP programming is successful. If the returned value is 0, then the patch is programmed with no errors.

```
5A 00 00 04 01 01 41 4C
5A 99 37 00
5A 00 00
5B 80 XX
```

Where:

XX = Returned value

6.4 Reading OTP Data

The OTP data can be read to confirm adequate space is available for the desired configuration commands or to verify that a previously programmed OTP patch is correctly written. To read the OTP data, perform the following sequence of commands:

1. Write **C1h** to register **0860h** to enable the Hub Feature Controller.

```
5A 00 00 05 00 01 08 60 C1
5A 99 37 00
```

2. Write **01h** to register **0A00h** to resume internal code execution.

```
5A 00 00 05 00 01 0A 00 01
5A 99 37 00
```

3. Write **07h 00h 00h TL(msb) TL(lsb)** to register **4800h** to configure the length of the OTP data retrieval. The OTP space is 8192 (2000h) bytes.

```
5A 00 00 09 00 05 48 00 07 00 00 TL(msb) TL(lsb)
```

Where:

TL = Total OTP Patch Length

4. Send the OTP Read Command **99 34 00**.

```
5A 99 34 00
```

5. Read register **414Ch** to confirm the OTP programming is successful. If the returned value is 0, then the OTP read is executed correctly.

```
5A 00 00 04 01 01 41 4C
5A 99 37 00
5A 00 04
5B 80 XX
```

Where:

XX = Returned value

6. Read register **8000h** to read back the OTP memory contents.

```
5A 00 00 04 01 80 80 00
5A 99 37 00
5A 00 04
5B 80 d1 d2 d3 ... d(n-2) d(n-1) d(n)
```


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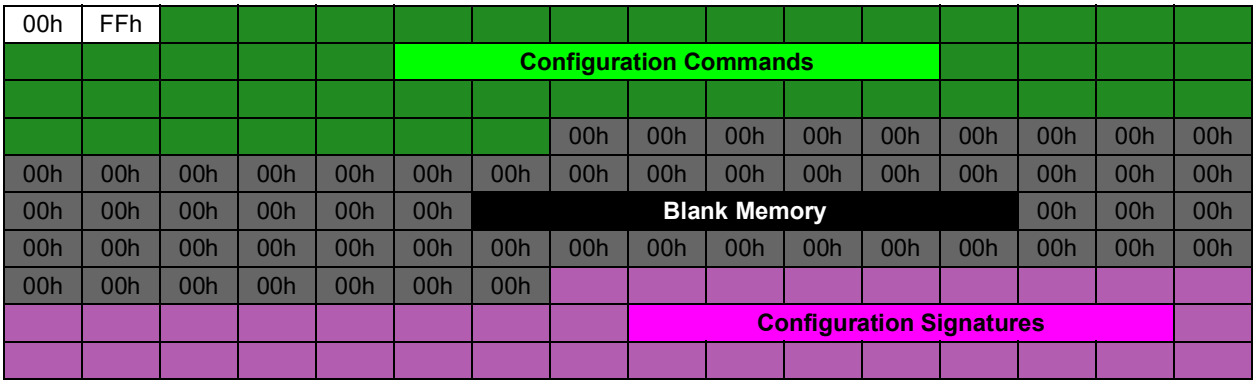
The OTP data is 8192 bytes of data. The contents of the OTP memory space is broken up into three sections: the already programmed Configuration Commands section, the Blank Memory section, and the Command Signature section.

FIGURE 4: OTP MEMORY STRUCTURE



6.4.1 CONFIGURATION COMMAND SECTION

This section grows from the start of the OTP data. These are the commands that are appended every time a Program OTP command is sent through SMBus and can vary in length depending on how many configuration registers have been manipulated.

6.4.2 BLANK MEMORY

This always appears as 00h to show that it has not been written yet.

6.4.3 CONFIGURATION SIGNATURE

The Configuration Signature is automatically generated when the OTP data is programmed. This signature is always 8 bytes per OTP program and is appended to the back of the OTP memory space every time the Program OTP command is sent. This signature contains a checksum to confirm that the configuration command is written correctly, as well as information on the location of the configuration commands within the OTP memory space and their total length.

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7.0 HUB PRODUCT IDS

7.1 Hub Feature Controller (UDC0)

The Hub Feature Controller (UDC0) is either enabled or disabled by default depending on the product code. If enabled, it is reported as a non-removable device.

The Hub Feature Controller exposes different USB interfaces depending on the state of the configuration strap (CONFIG_STRAP pin), enabling the features relevant to the selected PFx pins. Exposing a different PID for different configurations is required so that the correct USB client drivers are loaded.

The base PID is maintained as 0x2740. However, the last nibble is maintained to reflect the enabled features as shown in Table 134, with bit 2 indicating the presence of UART CDC bridge, and bit 3 indicating the presence of Generic USB device (WinUSB on Windows®).

TABLE 134: HUB FUNCTION CONTROLLER (UDC0) PIDS

Generic Device Class (HFC)	CDC (UART)	UDC0 Device Configuration	PID
No	No	No interface present, will not enumerate	NA
No	Yes	CDC Data, CDC Control	274Dh
Yes	No	Generic USB Device (WinUSB on Windows)	2740h
Yes	Yes	Generic USB Device (WinUSB on Windows), CDC Data, CDC Control	274Eh/ 274Fh

7.2 Hub PID Selection

Table 135 shows the USB2 and USB3 hub PIDs by device.

TABLE 135: PID SELECTION OPTIONS

Device	Package	Default USB3 HUB PID	Default USB3 HUB PID
USB5734	QFN64	5734h	2734h
USB5742	QFN56	5742h	2742h
USB5744	QFN56	5744h	2744h

Note: The hub PIDs (both USB2 and USB3) automatically decrease when downstream ports are disabled by port disable strap options. If one port is disabled by default, the PID number decreases by 1. If two ports are disabled by strap, the PID number decreases by 2, and so on. The ports that are disabled by OTP or SMBus do not cause an automatic PID modification.

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8.0 PHYSICAL AND LOGICAL PORT MAPPING

The USB5734/USB5744/USB5742 family of devices is based on a common architecture, but all have different modifications and/or pin bond outs to achieve the various device configurations.

The base chip is composed of a total of four USB3 PHYs and four USB2 PHYs. These PHYs are physically arranged on the chip in a certain way, which is referred to as the PHYSICAL port mapping. By default, the LOGICAL port mapping follows the PHYSICAL port mapping directly.

The actual port numbering may be remapped by default in different ways to meet specific product/design needs. This is referred to as LOGICAL mapping.

The various configuration options available for these devices may at times be relating to PHYSICAL mapping or LOGICAL mapping. Each individual configuration option that has a PHYSICAL or LOGICAL dependency is declared as such within the register description. When modifying the port mapping or disabling ports, care needs to be taken to ensure that the correct settings for all other ports are made with respect to either PHYSICAL or LOGICAL mapping, depending on the setting.

A system design in schematics and layout is generally performed using the pinout from the device data sheet, which is assigned by the default LOGICAL mapping. Hence, it is necessary to cross-reference the PHYSICAL vs. LOGICAL look-up tables when determining the hub configuration.

Note: The MPLAB® Connect tool makes configuration simple; the settings can be selected with respect to the LOGICAL port numbering, and the tool handles the necessary linking to the PHYSICAL port settings.

TABLE 136: USB5734 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER				
		0	1	2	3	4	5	0	1	2	3	4
2	USB2DN_DP1		X						X			
3	USB2DN_DM1		X						X			
4	USB3DN_TXDP1		X						X			
5	USB3DN_TXDM1		X						X			
7	USB3DN_RXDP1		X						X			
8	USB3DN_RXDM1		X						X			
9	USB2DN_DP2			X						X		
10	USB2DN_DM2			X						X		
11	USB3DN_TXDP2			X						X		
12	USB3DN_TXDM2			X						X		
14	USB3DN_RXDP2			X						X		
15	USB3DN_RXDM2			X						X		
19	USB2DN_DP3				X						X	
20	USB2DN_DM3				X						X	
21	USB3DN_TXDP3				X						X	
22	USB3DN_TXDM3				X						X	
24	USB3DN_RXDP3				X						X	
25	USB3DN_RXDM3				X						X	
26	USB2DN_DP4					X						X
27	USB2DN_DM4					X						X
28	USB3DN_TXDP4					X						X
29	USB3DN_TXDM4					X						X
31	USB3DN_RXDP4					X						X
32	USB3DN_RXDM4					X						X
53	USB2UP_DP	X						X				
54	USB2UP_DM	X						X				

TABLE 136: USB5734 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER				
		0	1	2	3	4	5	0	1	2	3	4
55	USB3UP_TXDPA	X						X				
56	USB3UP_TXDMA	X						X				
58	USB3UP_RXDPA	X						X				
59	USB3UP_RXDMA	X						X				

TABLE 137: USB5742 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER				PHYSICAL PORT NUMBER		
		0	1	2	3	0	1	2
1	USB2DN_DP1		X				X	
2	USB2DN_DM1		X				X	
3	USB3DN_TXDP1		X				X	
4	USB3DN_TXDM1		X				X	
6	USB3DN_RXDP1		X				X	
7	USB3DN_RXDM1		X				X	
8	USB2DN_DP2			X				X
9	USB2DN_DM2			X				X
10	USB3DN_TXDP2			X				X
11	USB3DN_TXDM2			X				X
13	USB3DN_RXDP2			X				X
14	USB3DN_RXDM2			X				X
45	USB2UP_DP	X				X		
46	USB2UP_DM	X				X		
47	USB3UP_TXDPA	X				X		
48	USB3UP_TXDMA	X				X		
50	USB3UP_RXDPA	X				X		
51	USB3UP_RXDMA	X				X		

TABLE 138: USB5744 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER				
		0	1	2	3	4	5	0	1	2	3	4
1	USB2DN_DP1		X						X			
2	USB2DN_DM1		X						X			
3	USB3DN_TXDP1		X						X			
4	USB3DN_TXDM1		X						X			
6	USB3DN_RXDP1		X						X			
7	USB3DN_RXDM1		X						X			
8	USB2DN_DP2			X						X		
9	USB2DN_DM2			X						X		
10	USB3DN_TXDP2			X						X		
11	USB3DN_TXDM2			X						X		
13	USB3DN_RXDP2			X						X		
14	USB3DN_RXDM2			X						X		

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TABLE 138: USB5744 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER				
		0	1	2	3	4	5	0	1	2	3	4
17	USB2DN_DP3				X						X	
18	USB2DN_DM3				X						X	
19	USB3DN_TXDP3				X						X	
20	USB3DN_TXDM3				X						X	
22	USB3DN_RXDP3				X						X	
23	USB3DN_RXDM3				X						X	
24	USB2DN_DP4					X						X
25	USB2DN_DM4					X						X
26	USB3DN_TXDP4					X						X
27	USB3DN_TXDM4					X						X
29	USB3DN_RXDP4					X						X
30	USB3DN_RXDM4					X						X
45	USB2UP_DP	X						X				
46	USB2UP_DM	X						X				
47	USB3UP_TXDPA	X						X				
48	USB3UP_TXDMA	X						X				
50	USB3UP_RXDPA	X						X				
51	USB3UP_RXDMA	X						X				

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001903F (07-04-19)	Section 2.0, General Information	Updated this section.
	Table 8	Corrected the value for USB3_NRD to 00h.
	Table 34 and Table 101	Corrected the bit offset typo.
	Section 4.0, Configuration Registers	Added definitions for registers 0800h, 318Eh, 411Dh, 4130h, 4140h-4423h, 4440h-4441h, 444E-444Gh, 44A5h, 44AC-456Eh, and 6086h - 71D0h.
	Section 4.0, Configuration Registers	Updated some register information about port number settings (PHYSICAL or LOGICAL port numbering).
	Section 6.0, OTP Configuration	Added a note about hub OTP's default configuration contents programmed by Microchip at fabrication.
	Section 6.1, Configuration Commands	Updated the section for clarity.
	Section 7.0, Hub Product IDs and Section 8.0, Physical and Logical Port Mapping	Added these sections.
DS00001903E (11-08-16)	Table 65, Table 66, Table 67, Table 68	Updated SE1 mode references.
DS00001903D (06-10-16)	Section 6.3, Writing OTP Data	Updated section to include more detailed procedures on writing OTP data.
	Section 6.4, Reading OTP Data	Updated section to include more detailed procedures on reading OTP data.
DS00001903C (09-24-15)	Section 2.3.1, Runtime	Changed referred I^2C runtime address to 2Dh.
	Table 5, "Example SMBus Write Command"	Fixed errors in the example hex code.
	Table 10 through Table 24	Fixed register address errors.
	Table 24, Table 25, Table 26	Removed "GPIO Input Enable Registers". Registers are not used by hub.
	Table 37, Table 38, Table 50	Added register descriptions.
	All	Added USB5742 to document.
	Table 8, Section 4.1, Register Definitions	Removed Battery Charging register at 30D0h.
	Table 35	Updated bit 3 definition.
	Table 37, Table 38	Updated bit field names.
	Section 5.1.1, SET_ADDRESS Byte (0x80), Section 5.1.2, Address Bytes (MSB, LSB), Section 5.1.3, BIT Command (0xFE), Section 5.1.4, Stop (0xFF)	Updated section titles.
	Section 6.2, Example, Table 133	Corrected register address to 411Ah.
DS00001903B (07-01-15)	All	Updated "USB 3.0" references to "USB 3.1 Gen 1" throughout the document.
DS00001903A (03-24-15)	Initial document release	

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