# USB5734

## Hardware Design Checklist

## 1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB5734. These checklist items should be followed when utilizing the USB5734 in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary," on page 27. Detailed information on these subjects can be found in the corresponding section:



## 2.0 GENERAL CONSIDERATIONS

### 2.1 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

### 2.2 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

### 2.3 USB-IF Compliant USB Connectors

- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

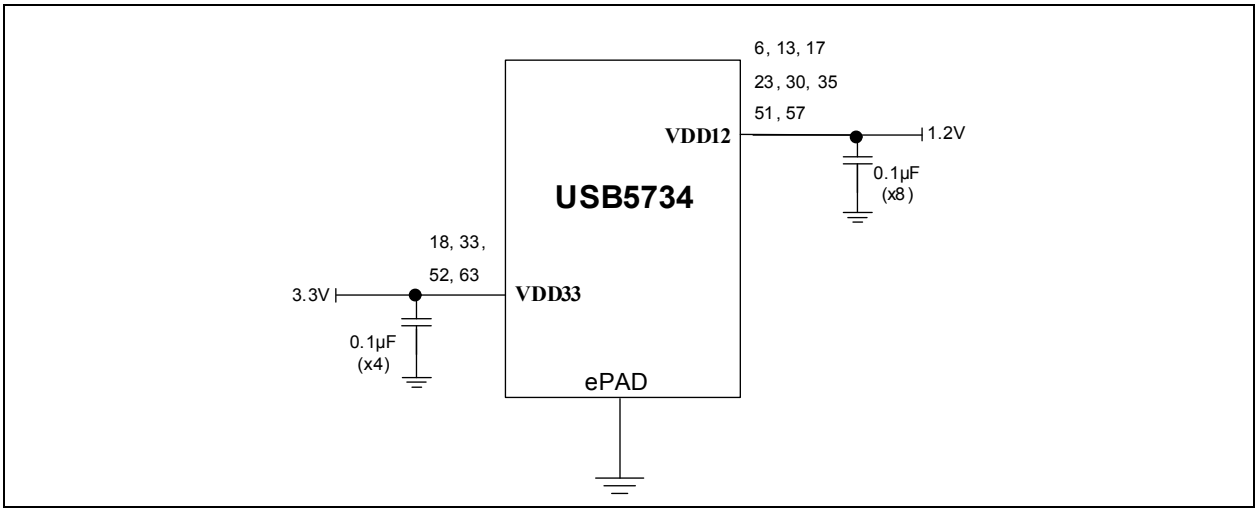
## 3.0 POWER

### 3.1 Power and Bypass Capacitance

- The analog supplies (**VDD33**) are located on pins 18, 33, 52, 63 and require a connection to a regulated 3.3V power plane.
- The **VDD33** pins each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The analog supplies (**VDD12**) are located on pins 6, 13, 17, 23, 30, 35, 51, 57 and require a connection to a regulated 1.2V power plane.
- The **VDD12** pins each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

**FIGURE 3-1: POWER AND GROUND CONNECTIONS**




## 4.0 USB SIGNALS

### 4.1 Upstream Port USB Signals

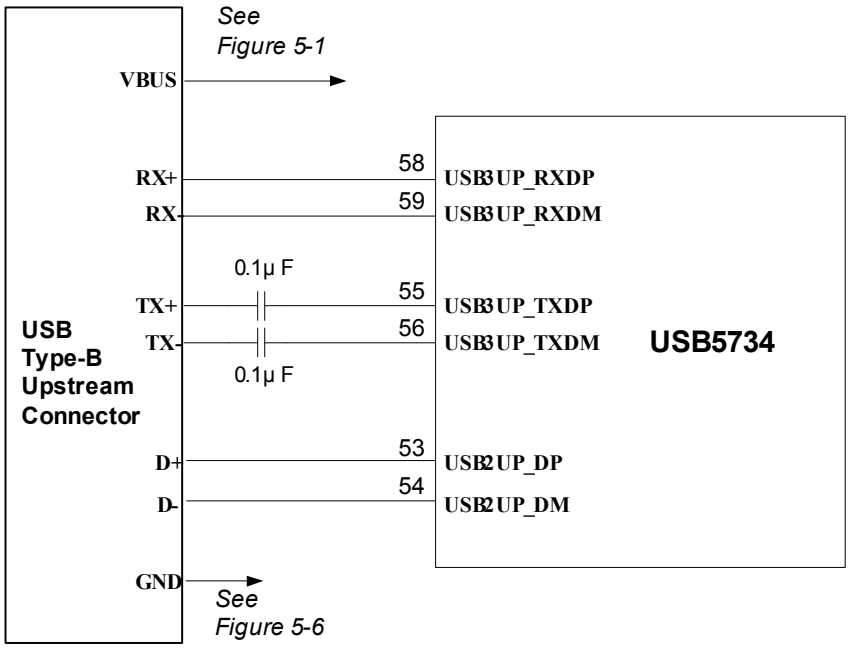
- **USB2UP_DP** (pin 53): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can connect directly to the D+/DP[1] pin of a USB Connector.
- **USB2UP_DM** (pin 54): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internally (no external resistors required).This pin can connect directly to the D–/DM[1] pin of a USB Connector.
- **USB3UP_TXDP** (pin 55): This pin is the positive (+) signal of the upstream USB3.1 'Side A' transmitter (TX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin requires a series 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX–)[2] pin of the USB Connector.
- **USB3UP_TXDM** (pin 56): This pin is the negative (–) signal of the upstream USB3.1 'Side A' transmitter (TX) differential pair. All necessary USB terminations and resistors are included internal the IC. This pin requires a series 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the TX– (or TX+)[2] pin of the USB Connector.
- **USB3UP_RXDP** (pin 58): This pin is the positive (+) signal of the upstream USB3.1 'Side A' receiver (RX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can be connected directly to the RX+ (or RX–)[2] pin of the USB Connector.
- **USB3UP_RXDM** (pin 59): This pin is the negative (–) signal of the upstream USB3.1 'Side A' receiver (RX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can be connected directly to the RX– (or RX+)[2] pin of the USB Connector.

**Note 1:** The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I$^2$C configuration registers.

**2:** A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped.

For the standard Type-B port connection details, refer to Figure 4-1.

**FIGURE 4-1: UPSTREAM PORT TYPE-B USB CONNECTIONS**

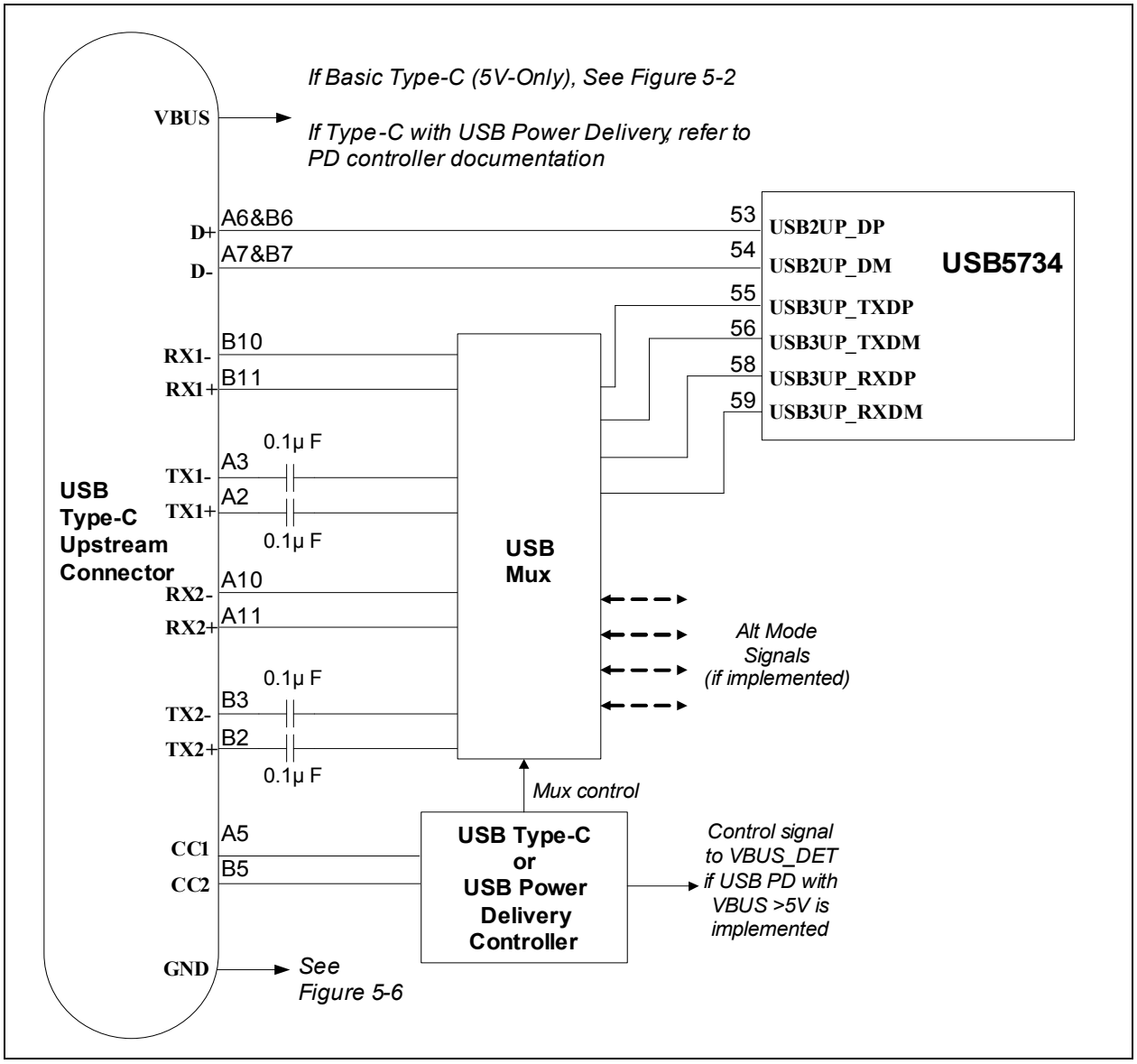



When connecting the upstream port of a USB5734 to a Type-C connector, the following additional components are required:

- A basic Upstream Facing Port (UFP) Type-C Controller or USB Power Delivery Type-C Controller
- A 2:1 Multiplexer (if no Alternate mode support is required) or an Alternate mode-specific cross bar switch (such as a 6:4 mux for DisplayPort Alternate mode support).

For an example on how to connect the upstream port to a Type-C port, refer to Figure 4-2.

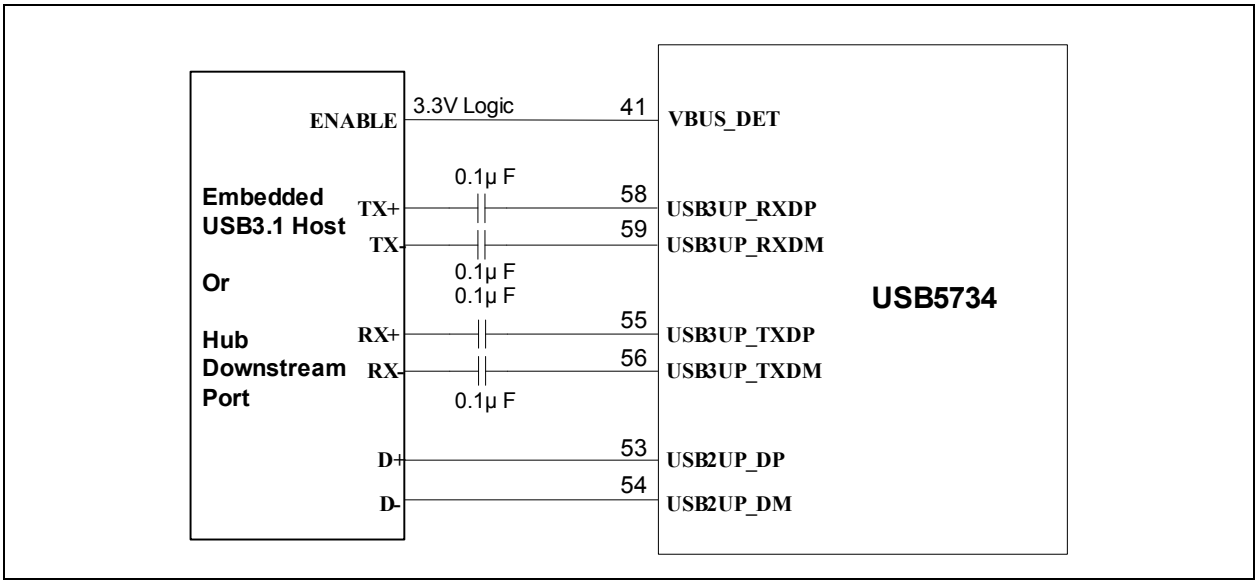
**FIGURE 4-2: UPSTREAM PORT TYPE-C USB CONNECTIONS**




When connecting the upstream port to an embedded USB3.1 host or the downstream port of another embedded USB3.1 hub, ensure that the transmitter pins on the hub are properly connected to the receiver pins of the host, and that the receiver pins on the hub are properly connected to the host transmitter pins. DC blocking decouple capacitors are still required in an embedded connection on both differential pairs.

For an example on how to connect the upstream port to an embedded USB3.1 host, refer to Figure 4-3.

**FIGURE 4-3: UPSTREAM PORT EMBEDDED HOST USB CONNECTIONS**



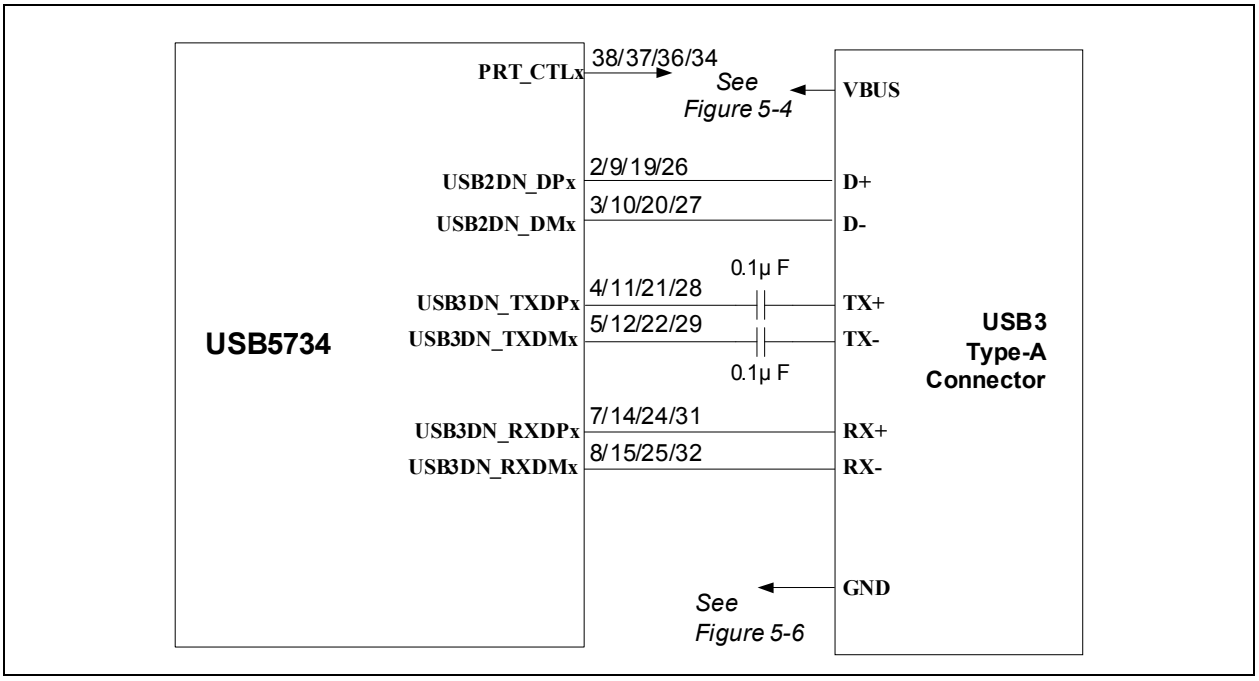

## 4.2 Downstream Port USB Signals

- **USB2DN_DP1/USB2DN_DP2/USB2DN_DP3/USBDN_DP4** (pins 2/9/19/26): This pin is the positive(+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can connect directly to the D+/DP[1] pin of a USB Connector.
- **USB2DN_DM1/USB2DN_DM2/USB2DN_DM3/USB2DN_DM4** (pins 3/10/20/27): This pin is the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can connect directly to the D-/DM[1] pin of a USB Connector.
- **USB3DN_TXDP1/USB3DN_TXDP2/USB3DN_TXDP3/USB3DN_TXDP4** (pins 4/11/21/28): This pin is the positive (+) signal of the downstream port USB3.1 transmitter (TX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin requires a series 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX–)[2] pin of the USB Connector.
- **USB3DN_TXDM1/USB3DN_TXDM2/USB3DN_TXDM3/USB3DN_TXDM4** (pins 5/12/22/29): This pin is the negative (–) signal of the downstream port USB3.1 transmitter (TX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin requires a series 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the TX– (or TX+)[2] pin of the USB Connector.
- **USB3DN_RXDP1/USB3DN_RXDP2/USB3DN_RXDP3/USB3DN_RXDP4** (pins 7/14/24/31): This pin is the positive (+) signal of the downstream port USB3.1 receiver (RX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can be connected directly to the RX+ (or RX–)[2] pin of the USB Connector.
- **USB3DN_RXDM1/USB3DN_RXDM2/USB3DN_RXDM3/USB3DN_RXDM4** (pins 8/15/25/32): This pin is the negative (–) signal of the downstream port USB3.1 receiver (RX) differential pair. All necessary USB terminations and resistors are included internally (no external resistors required). This pin can be connected directly to the RX– (or RX+)[2] pin of the USB Connector.

| | |
|---|---|
| **Note 1:** | The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I$^2$C configuration registers. |
| **2:** | A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped. |

For the standard Type-A port connection details, refer to Figure 4-4.

**FIGURE 4-4: DOWNSTREAM PORT TYPE-A USB CONNECTIONS**

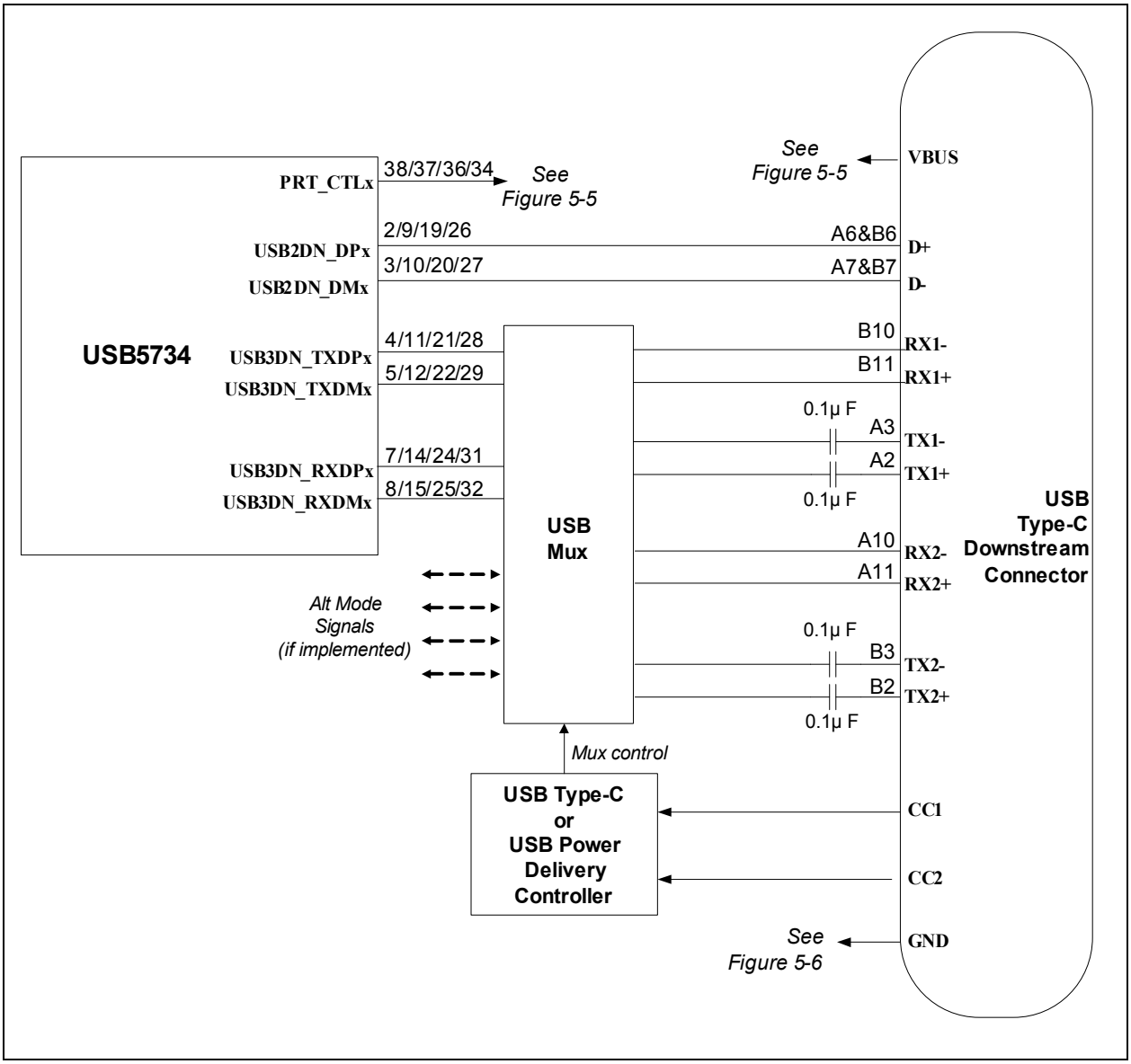



When connecting the upstream port to a legacy Type-C connector, the following additional components are required:

- A Basic Upstream Facing Port (UFP) Type-C Controller or USB Power Delivery Type-C Controller
- A 2:1 Multiplexer (if no Alternate mode support is required) or an Alternate mode specific cross bar switch (such as a 6:4 mux for DisplayPort Alternate mode support)

For an example on how to connect downstream Ports 1 and/or 2 to a legacy Type-B port, refer to Figure 4-5.

**FIGURE 4-5: DOWNSTREAM PORT TYPE-C USB CONNECTIONS**

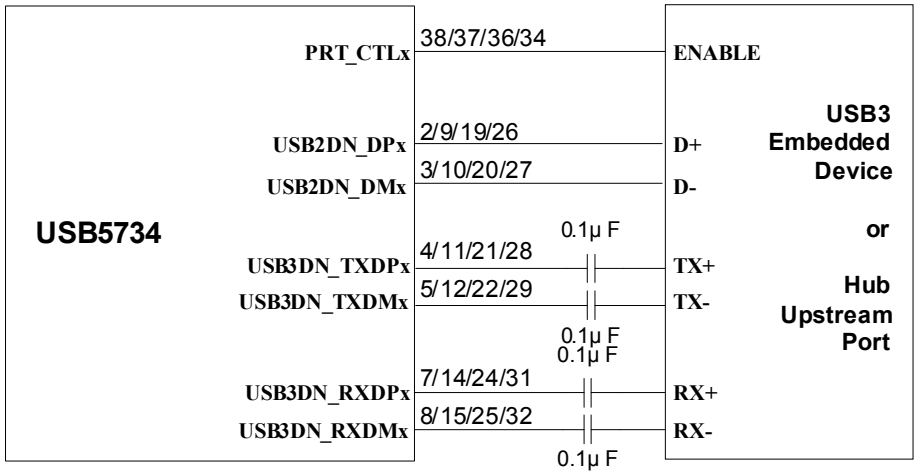



When connecting the downstream port to an embedded USB3.1 device, or the upstream port of another embedded USB3.1 hub, some pin connections change:

- PRT_CTLx should directly control the ‘enable’ of the embedded USB device or hub upstream port. Signal level shifting or inversion may be required, depending on the device.
- USB D+ and USB D– should connect directly to USB D+ and USB D– of the embedded USB device or hub upstream port.
- The downstream port transmitter (TX+/–) pins should connect to the receiver pins of the embedded USB device or hub upstream port. DC blocking 0.1 uF caps must be placed in between the hub downstream and the embedded USB device or hub upstream port. USB3 signals have automatic polarity detection and correction. The polarity of these pins may be swapped to allow for the more straightforward PCB routing.
- The downstream port receiver (RX+/–) pins should connect to the transmitter pins of the embedded USB device or hub upstream port. DC blocking 0.1 uF caps must be placed in between the hub downstream and the embedded USB device or hub upstream port. USB3 signals have automatic polarity detection and correction. The polarity of these pins may be swapped to allow for the more straightforward PCB routing.

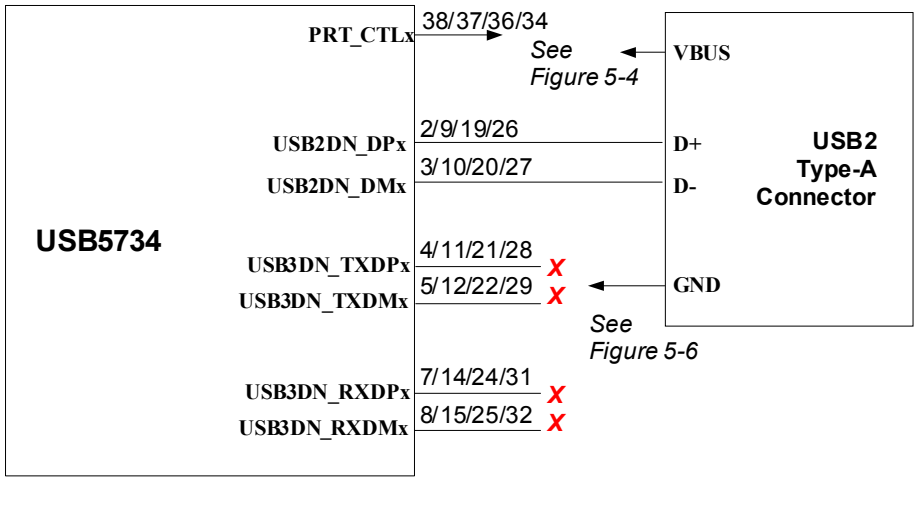
For an example on how to connect downstream Ports 1 and/or 2 to an embedded USB3.1 device or hub upstream port, refer to Figure 4-6.

**FIGURE 4-6: DOWNSTREAM PORT EMBEDDED DEVICE USB CONNECTIONS**




If connecting a downstream port to a USB2.0-only connector, refer to Figure 4-7. Note that in this configuration, the USB3.1 portion of the port should be disabled in the hub configuration to meet USB specification requirements.

**FIGURE 4-7: DOWNSTREAM PORT USB2 ONLY TYPE-A USB CONNECTIONS**




## 4.3 Disabling Downstream Ports

If a downstream port of the USB5734 is unused, it should be disabled. This can be achieved through hub configuration ($I^2C$ or OTP), or through a port disable strap option.

If using the port disable strap option, the USB_DP2 and USB_DM2 signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor. All other signals related to the associated port may be floated.

## 4.4 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These are generally grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system level tests
- Application targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short to battery protection
- Common-mode chokes
  - For EMI reduction

The USB5734 can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have and to select components accordingly and follow the implementation guidelines from the manufacturer of these devices. You may also use the following general guidelines for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB2.0 specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry. In a USB3.1 Gen 1 system ESD protection should add no more than 0.5 pF capacitance to the differential pairs.
- These devices should be placed as close to the USB connector as possible.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

### 4.4.1 ADDITIONAL PROTECTION OPTIONS FOR USB3 PINS

In addition to TVS diodes, some of the following may be implemented:

- Use decoupling capacitors on both the TX and RX differential pairs. Decoupling capacitors on the RX pairs are not required for operation but add some additional ESD immunity at a low cost.
- Use decoupling capacitors with high voltage ratings. 0.1 µF capacitors at 0402 sizes are widely available.
- A very small resistor of 0.3 Ohms to 0.5 Ohms may be placed in series with the decoupling capacitor (placed physically between the TVS diode and the decoupling capacitor) to help steer more of the ESD energy through the TVS diode. A resistor network (2-resistor/4-contact) in 0402 or 0201 size can be placed with very little impact to the differential routing of the signals.

| | |
|---|---|
| **Note:** | Microchip PHYBoost, VariSense, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help overcome marginal failures. It is easier to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests on physical hardware. |

# 5.0 USB CONNECTORS

## 5.1 Upstream Port VBUS and VBUS_DET

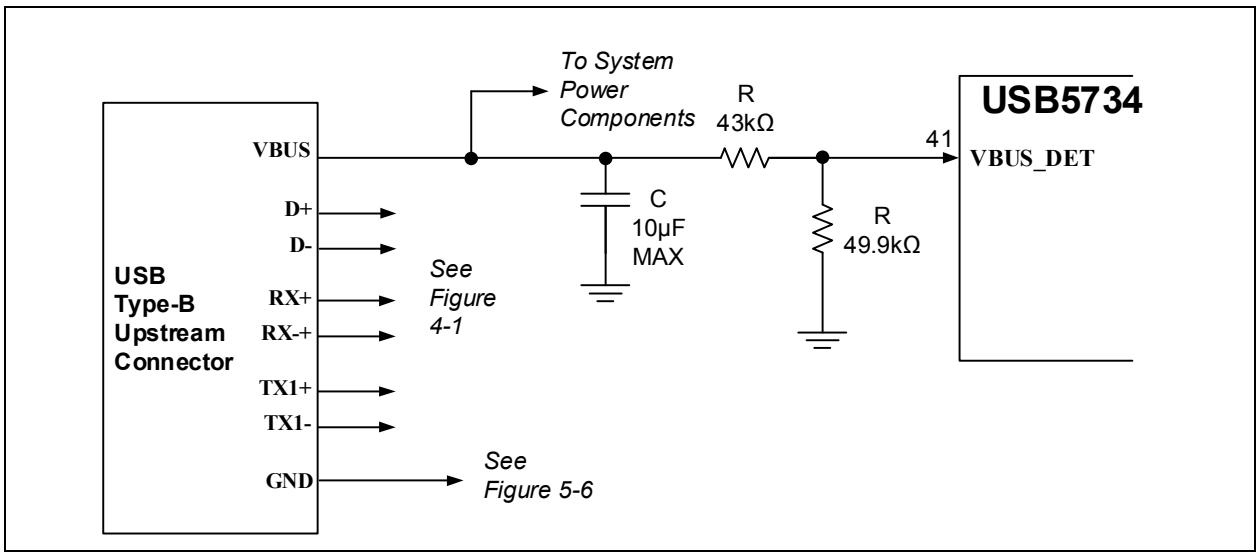
The upstream port VBUS line must have no more than 10 uF of total capacitance connected.

The **VBUS_DET** pin is used by the USB5734 to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft reset and re-connection of the USB5734.

It is permissible to tie **VBUS_DET** directly to 3.3V. However, this is not recommended as the ability to force a reset of the hub from the USB host VBUS control is lost.

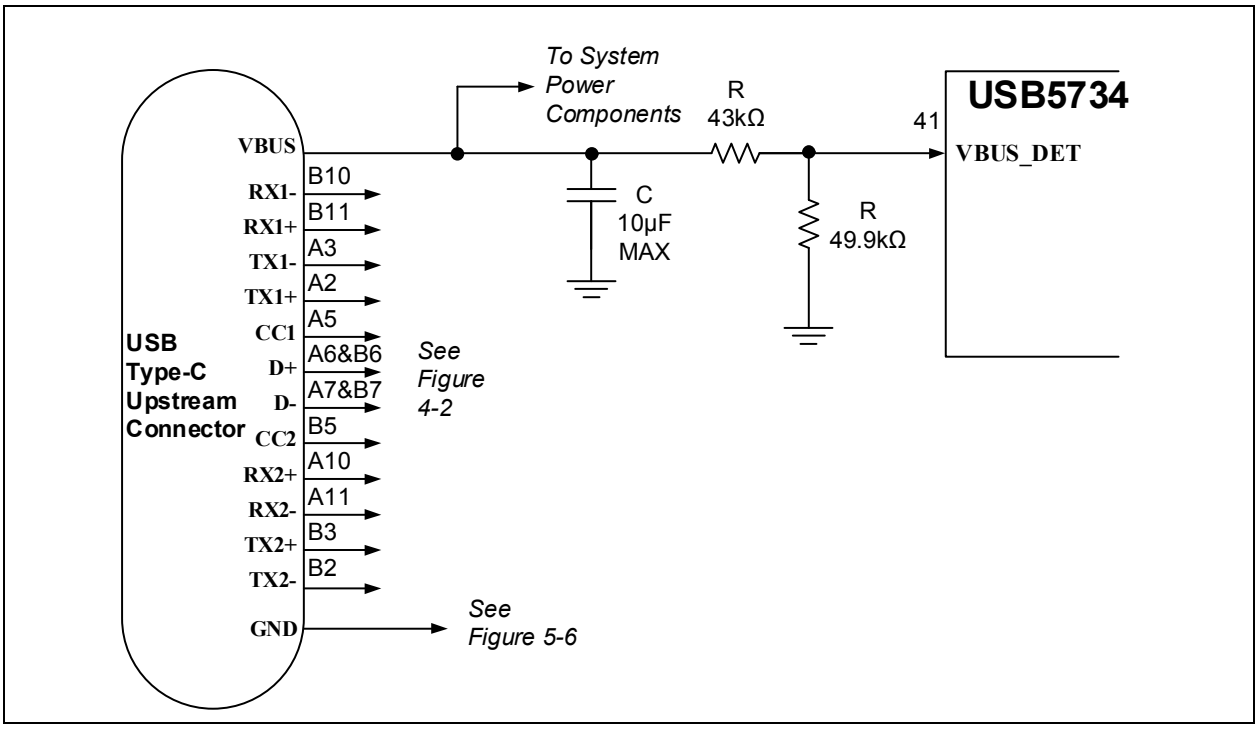
If connecting the upstream port to standard USB Type-B, the recommended implementation is shown in Figure 5-1.

**FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS**



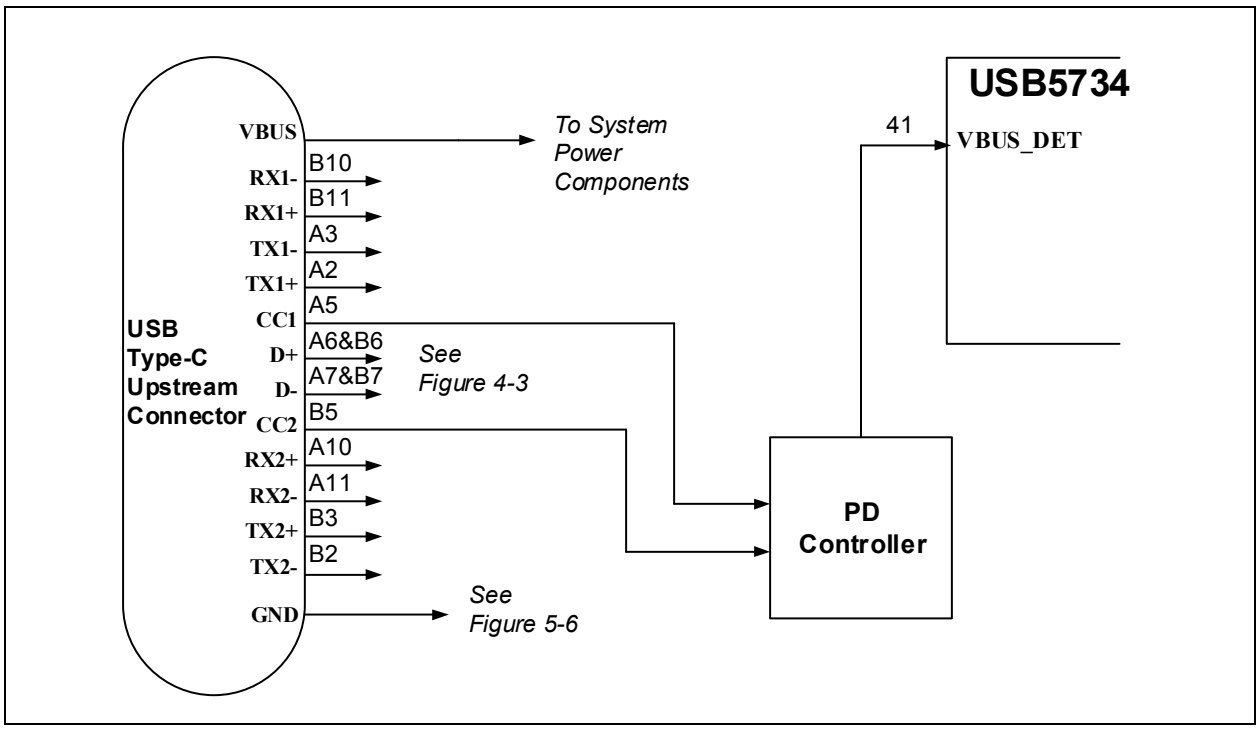
If connecting the upstream port to basic USB Type-C port where VBUS never exceeds 5V, the recommended implementation is shown in Figure 5-2.

**FIGURE 5-2: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS FOR A BASIC TYPE-C PORT**




If connecting the upstream port to USB Type-C with USB Power Delivery support (where VBUS may be elevated above 5V), the recommended implementation is shown in Figure 5-3.

**FIGURE 5-3: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS FOR A FULL FEATURED TYPE-C PORT WITH POWER DELIVERY**




## 5.2 Downstream Port VBUS and PRTCTLx Connections for Standard Type-A Ports

The **PRT_CTLx** pin is a hybrid input/output pin which has the following states:

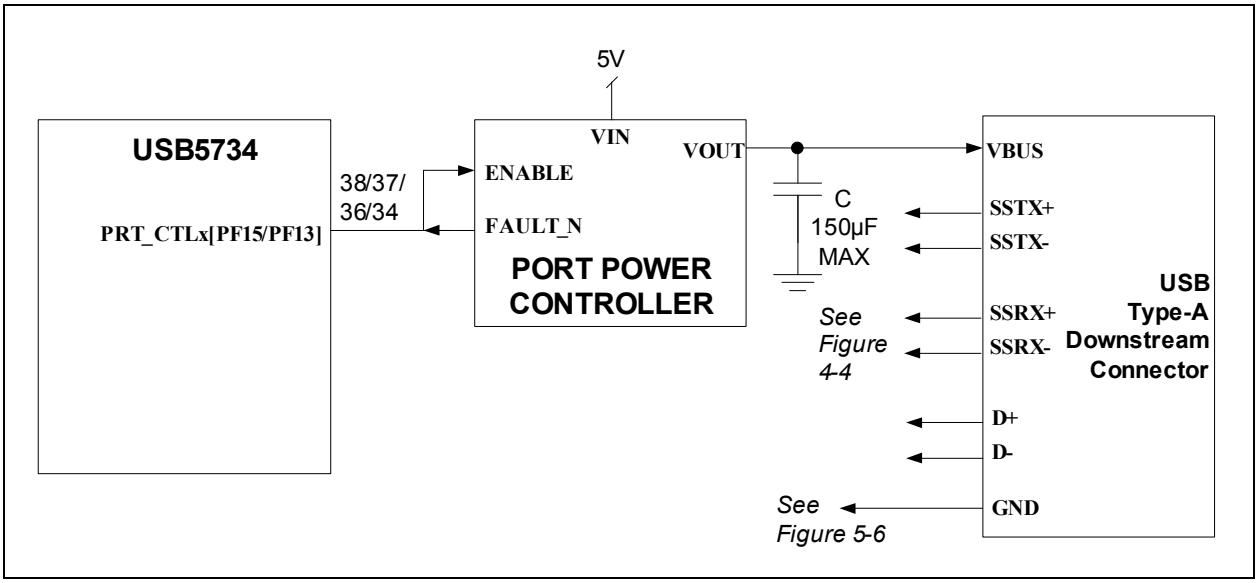
- PORT OFF: **PRT_CTLx** is an output and drives low. The **PRT_CTLx** pin will only transition to the PORT ON state through a specific command from the USB host.
- PORT ON: **PRT_CTLx** is an input with an internal weak pull-up enabled. The input buffer monitors for overcurrent events, which are indicated by the port power controller by pulling the **PRT_CTLx** line low. Once an overcurrent event is detected, the **PRT_CTLx** automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **PRT_CTLx** pin to a port power controller, the signal should be connected to both the enable and the fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

A typical downstream port Type-A implementation is shown in Figure 5-4

**FIGURE 5-4: DOWNSTREAM PORT VBUS AND PRT_CTLX CONNECTIONS**

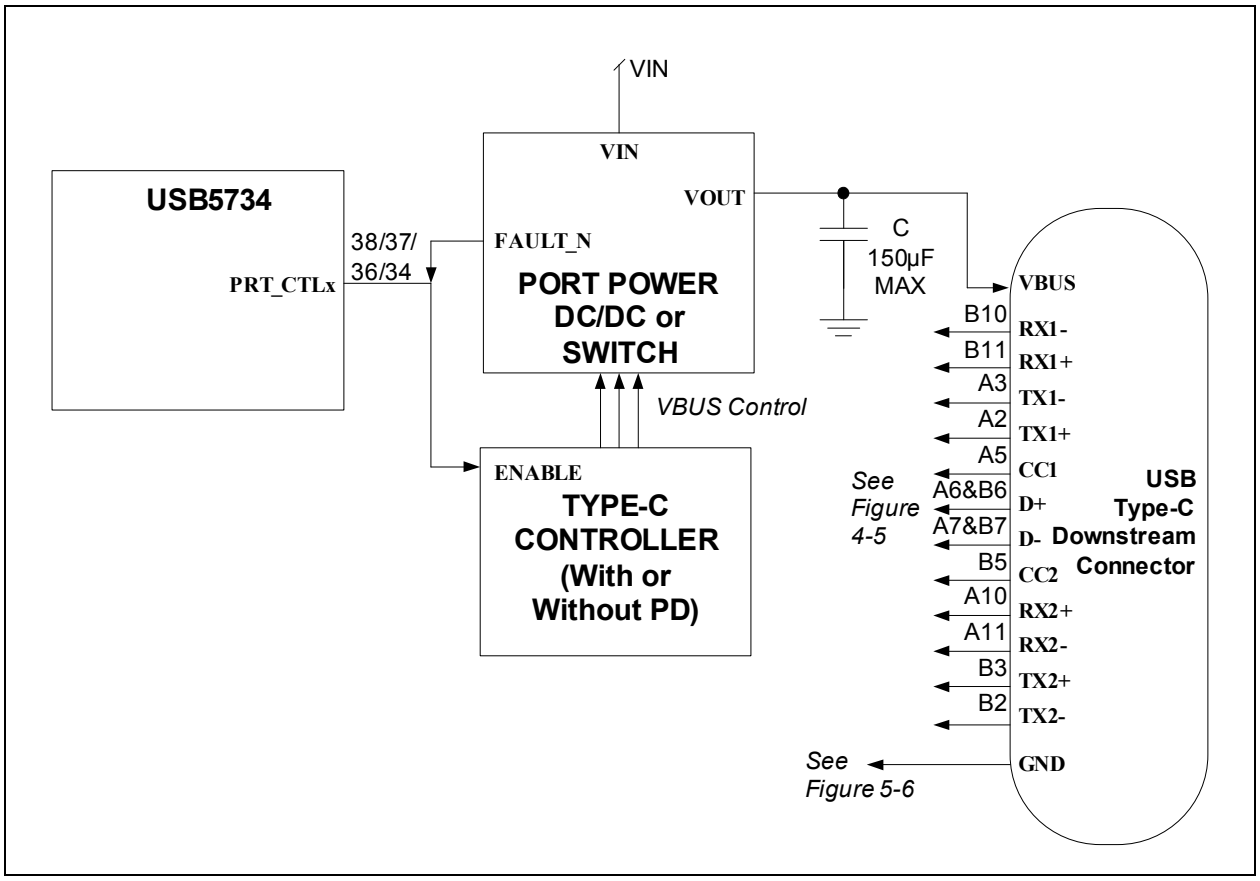



The implementation, as shown in Figure 5-4, assumes that the port power controller has an active-high enable input, and an active-low open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

## 5.3 Downstream Port VBUS and PRTCTLx Connections for Type-C Ports

A typical Type-C implementation is shown in Figure 5-5. Specific details on how to connect the VBUS switch or DC/DC regulator should be obtained from the supplier of the Type-C/Power Delivery controller device.

**FIGURE 5-5: DOWNSTREAM PORT VBUS AND PRT_CTL CONNECTIONS FOR TYPE-C PORT**




The implementation, as shown in Figure 5-5, assumes that the port power controller has an active-high enable input, and an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

## 5.4 GND and EARTH Recommendations

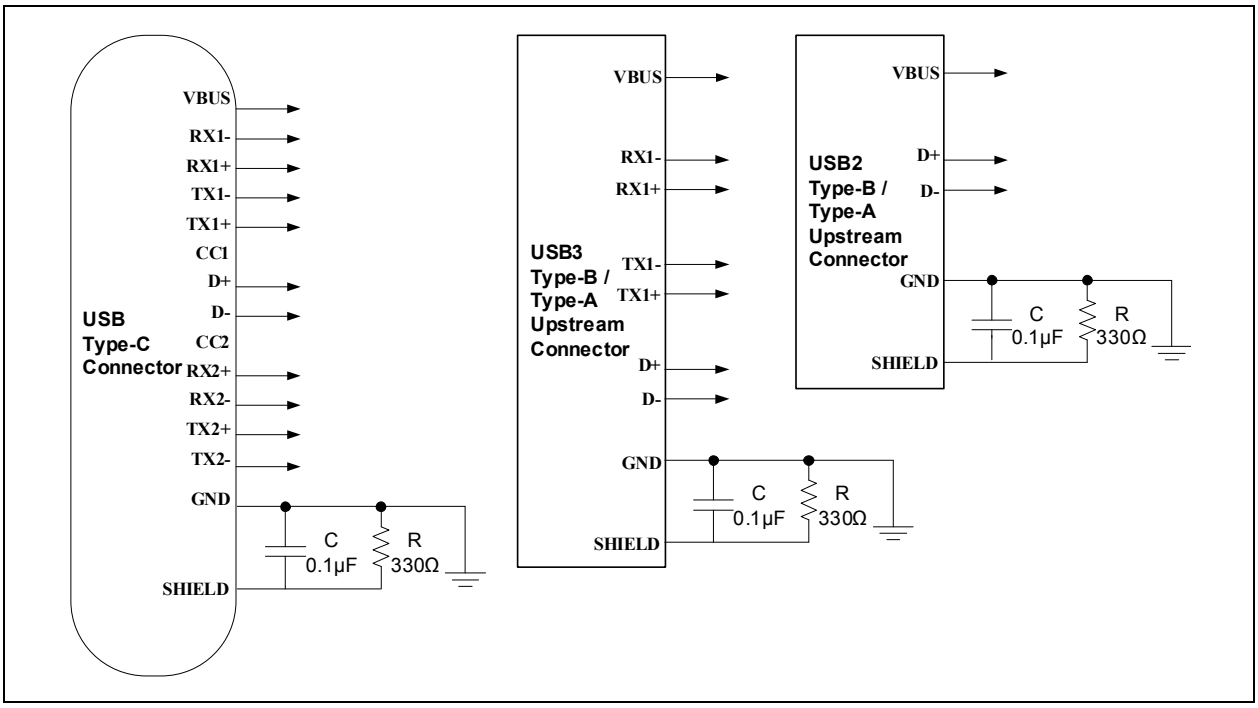
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- [Recommended] To GND through a resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Directly to the GND plane.

The recommended implementation is shown in Figure 5-6.

**FIGURE 5-6: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS**



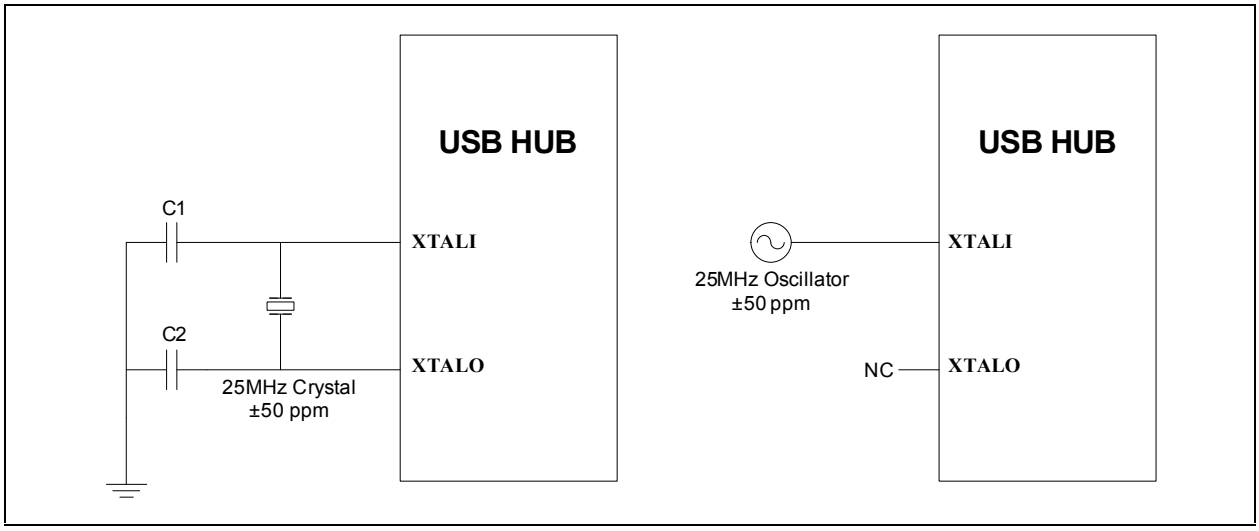
# 6.0 CLOCK CIRCUIT

## 6.1 Crystal or External Clock Connection

A 25.000 MHz (±50 ppm) reference clock is the source for the USB interface and for all other functions of the device (See Figure 6-1.) For exact specifications and tolerances, refer to the latest revision of the USB5734 data sheet.

- **XTALI** (pin 63) is the clock circuit input for the USB5734. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 61) is the clock circuit output for the USB5734. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system dependent, based on the total $C_L$ specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical $C_1$ and $C_2$ capacitor values is:
  - $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$
  - Where: CL is the spec from the crystal datasheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$
  - **Note:** $C_{stray}$ is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1-2 pF range, and then verified by physical experiments in the lab if PCB simulation tools are not available.
- Alternately, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the. When using a single-ended clock source, **XTALO** (pin 37) should be left floating as a No Connect (NC)

**FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS**



# 7.0 POWER AND STARTUP

## 7.1 RBIAS Resistor

The RBIAS pin on the USB5734 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close to the IC pin as possible, and be given a dedicated, low-impedance path to a ground plane.

## 7.2 Board Power Supplies

### 7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the USB5734 data sheet. If a monotonic/fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

### 7.2.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying 500 mA (if BC1.2 is not enabled), 1.5A (if BC1.2 is enabled), or up to 3.0A (if the maximum Type-C current is enabled) to the USB downstream port VBUS without drooping below the minimum voltage permissible in the USB specification.

The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized such that is able to supply the maximum power consumption specifications as displayed in the USB5734 data sheet.

The 1.2V power supply must be able to supply enough power to the USB hub IC. It is recommend that 1.2V power rail be sized such that it is able to supply the maximum power consumption specifications as displayed in the USB5734 data sheet.

## 7.3 Reset Circuit

**RESET_N** (pin XX) is an active-low reset input. This signal resets all logic and registers within the USB5734. A hardware reset (**RESET_N** assertion) is not required following power-up. Please refer to the latest copy of the *USB5734 Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the USB5734 when reset is triggered by the power supply.

**FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY**

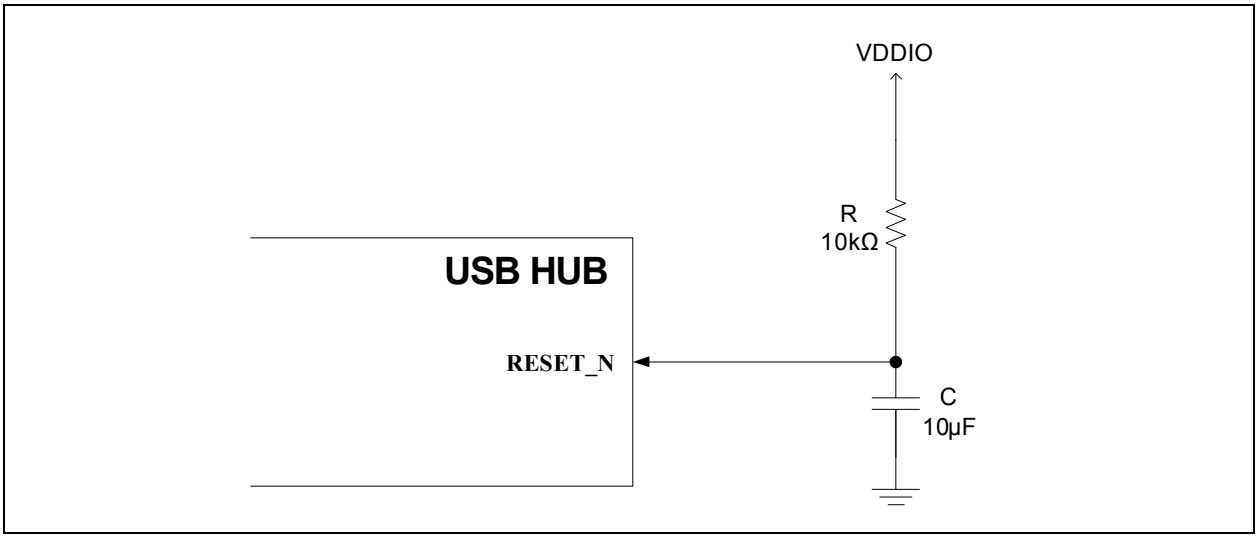
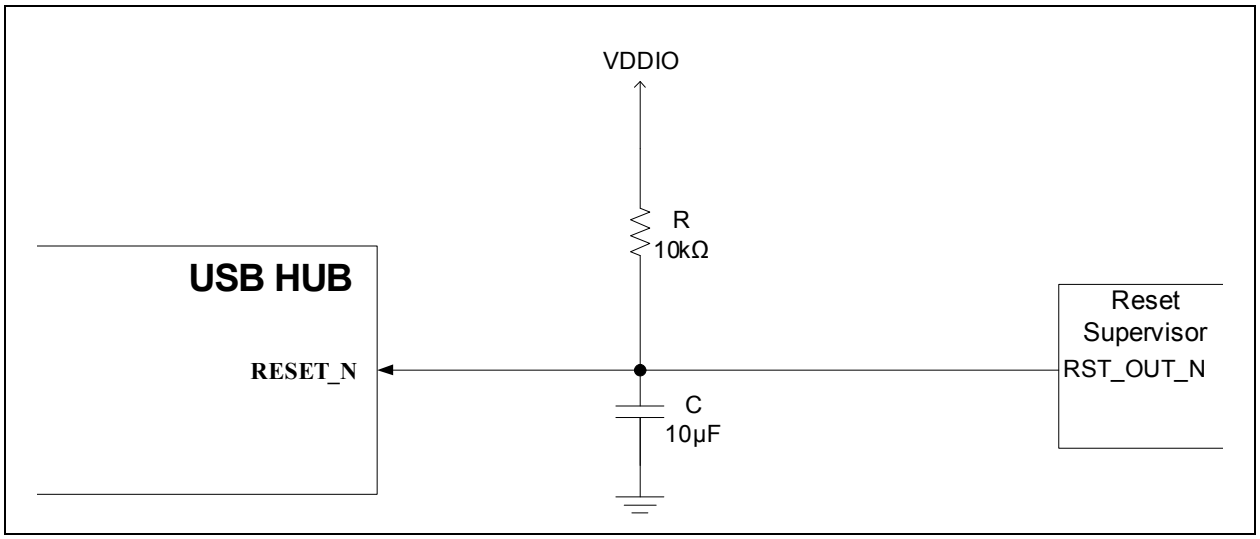


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (RST_OUT_N) from the CPU/MCU provides the warm reset after power-up.

**FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT**



# 8.0 EXTERNAL SPI MEMORY

## 8.1 SPI Operation Summary

By default, the USB5734 executes firmware from an internal read only memory (ROM). The USB5734 supports optional firmware execution from an external SPI Flash device. An SPI Flash is only required if a custom firmware is required for the application.

The SPI interface can operate at 60 MHz or 30 MHz.

The SPI interface can operate in Dual mode or Quad mode.

The firmware image can be executed in one of two ways:

1. **Execute in place:** firmware is continuously executed directly from the SPI Flash, and interface is constantly active.
2. **Execute in internal SRAM:** firmware is loaded into the hub's internal SRAM and executed internally. This may only be supported if the firmware image is smaller than the hub's SRAM size.

| | |
|---|---|
| **Note:** | All firmware images are developed, compiled, tested, and provided by Microchip. The SPI interface speed is an OTP-configurable option, and only speeds which were specifically tested with the firmware image should be selected. The standard speed under which firmware images are developed and tested under is 60 MHz. The execution method is configured with the firmware image itself and cannot be changed via configuration. |

## 8.2 Compatible SPI Flash Devices

Microchip recommend SST brand SPI Flash devices. Microchip has verified compatibility of the following list of SPI Flash devices:

- SST26F016B
- SST26F032B
- SST26VF064B
- SST25VF064C
- SST25VF040C
- SST25VF040B
- SST25VF020B
- SST25VF080B

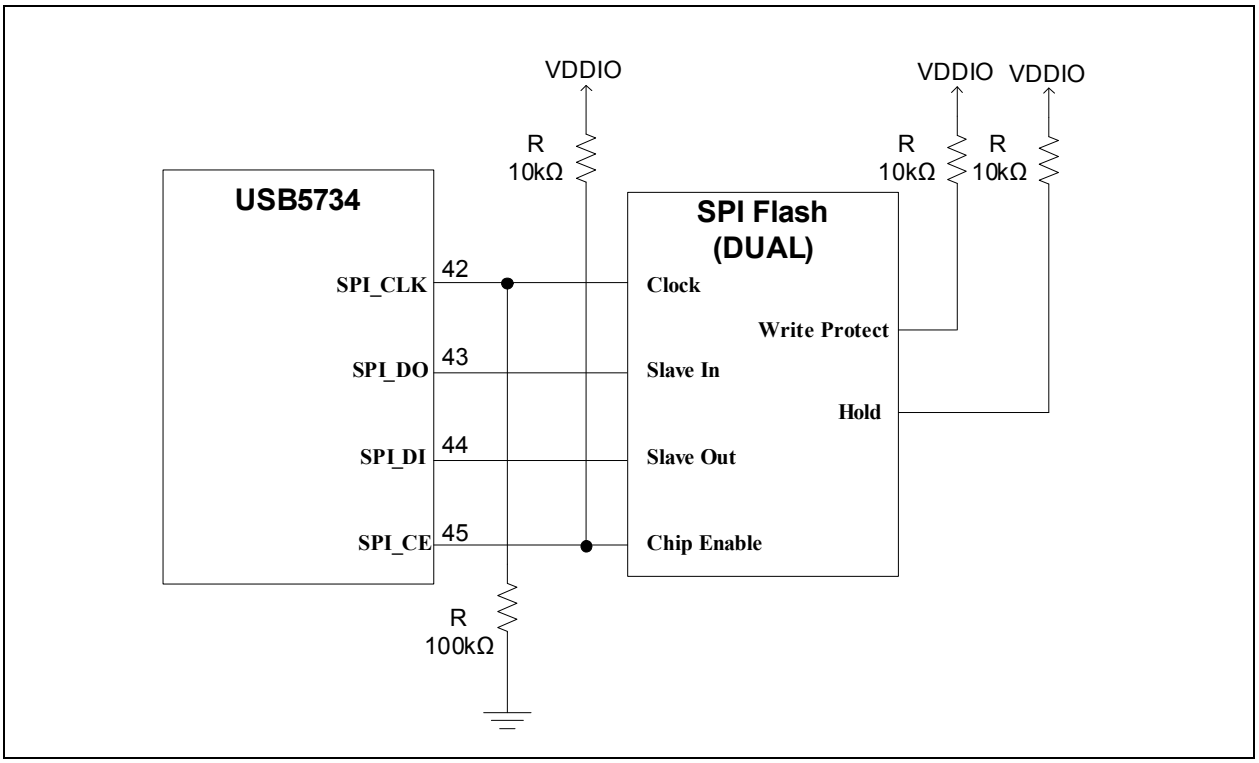
Other SPI Flash devices may be used, provided they meet the following minimum requirements:

- 30 MHz or 60 MHz operation
- Mode 0 or Mode 3
- 256 kB or larger memory
- Utilize same OpCode commands as devices in above list of compatible devices
- Dual mode or Quad mode operation

## 8.3 SPI Connection Diagrams

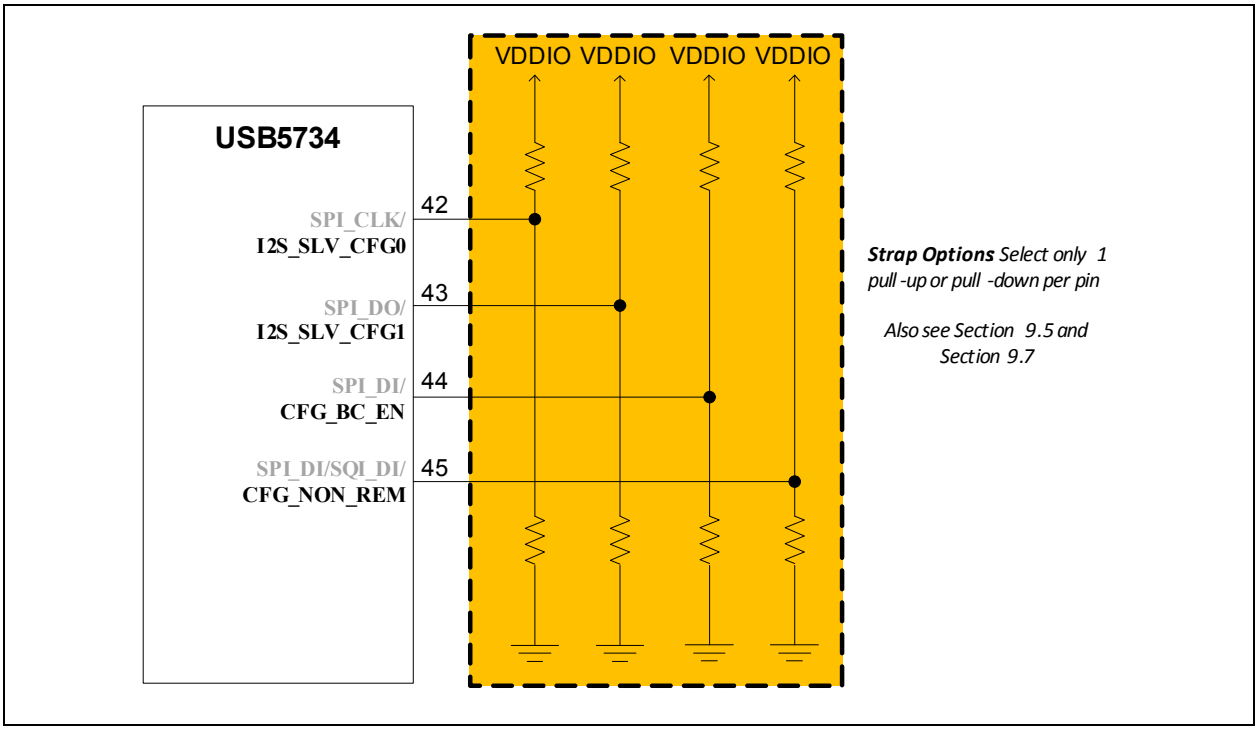
If a Dual SPI Flash device is used, the recommended schematic connections are shown in Figure 8-1.

**FIGURE 8-1: DUAL SPI FLASH CONNECTIONS**



If an SPI Flash device is not used, the recommended schematic connections are shown in Figure 8-2. Some of the SPI pins become configuration straps when an SPI Flash is not connected. A configuration strap option must be selected, and these pins cannot be floated.

**FIGURE 8-2: RECOMMENDED CONNECTIONS IF SPI FLASH IS NOT USED**



# 9.0 MISCELLANEOUS

## 9.1 GPIOs

The 7 Programmable Function pins included in USB5734 may be controlled from the USB host or from an embedded SOC/MCU as GPIOs. These GPIOs are available for use without any additional configuration. By default, all of the GPIOs are configured as inputs. If a default output Power-on state is required, the default pin Output state can be configured in the hub's OTP memory or through the I2C/SMBus slave interface during the configuration stage (SOC_CFG). These pins are described in Table 9-1.

In order to utilize GPIOs, the **CFG_STRAP** pin must be set to the appropriate configuration mode.

**TABLE 9-1: AVAILABLE GPIOS**

| Pin | PF Pin | Name | Configuration Requirements |
|---|---|---|---|
| 50 | PROG_FUNC1 | GPIO1 | Configuration 1 (200 kΩ Pull-down) or Configuration 4 (10 kΩ Pull-up) |
| 39 | PROG_FUNC2 | GPIO2 | Configuration 1 (200 kΩ Pull-down) or Configuration 4 (10 kΩ Pull-up) |
| 40 | PROG_FUNC3 | GPIO3 | Configuration 1 (200 kΩ Pull-down) or Configuration 4 (10k Ω Pull-up) |
| 46 | PROG_FUNC4 | GPIO6 | Configuration 4 (10 kΩ Pull-up) |
| 47 | PROG_FUNC5 | GPIO8 | Configuration 1 (200 kΩ Pull-down) or Configuration 4 (10 kΩ Pull-up) |
| 49 | PROG_FUNC6 | GPIO10 | Configuration 1 (200 kΩ Pull-down) or Configuration 4 (10 kΩ Pull-up) |
| 16 | PROG_FUNC7 | GPIO1 | Configuration 1 (200 kΩ Pull-down) or Configuration 4 (10 kΩ Pull-up) |

Instructions for operating these pins, including register definitions, are described in full in *AN1997 USB-to-GPIO Bridging with Microchip USB3.1 Gen 1 Hubs*.

Ensure that the voltages applied to these pins are within the electrical specifications for the pins, and that any external loading is within the drive strength capabilities as described in the USB5734 data sheet.

## 9.2 I2C/SMBus Connections

There are two I2C/SMBus interfaces available on USB5734. These are described in Table 9-2.

**TABLE 9-2: I2C/SMBUS PINS**

| Pin | Name | Role | Configuration Requirements |
|---|---|---|---|
| 43 | SPI_DO/UART_TX/ GPIO5/ I2C_SLV_CFG1 | I2C Slave or Master Data | I2C Slave mode: Pull-up resistors detected on pins at start-up, and no external SPI FW image is present.<br><br>I2C Master mode: No pull-up resistors detected on pins at start-up, and no external SPI FW image is present. |
| 44 | SPI_CLK/UART_RX/ GPIO4/ I2C_SLV_CFG0 | I2C Slave or Master Clock | I2C Slave mode: Pull-up resistors detected on pins at start-up, and no external SPI FW image is present.<br><br>I2C Master mode: No pull-up resistors detected on pins at start-up, and no external SPI FW image is present. |

### 9.2.1 SLAVE INTERFACE

The USB5734 may be configured by an embedded SOC/MCU during both the start-up and runtime stages. The **CFG_STRAP** pin must set the hub into configuration 1, 2, 3, or 6, and pull-up resistors must be detected on the **SPI_DO/UART_TX/GPIO5/I2C_SLV_CFG1** and **SPI_CLK/UART_RX/GPIO4/I2C_SLV_CFG0** pins by the hub at start-up in order for the I²C/SMBus slave interface to become active. The interface command specification and configuration register set are described in full in *AN1903 Configuration Options for the USB5734, USB5744 and USB5742*.

Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient, depending on the interface speed and total capacitance on I²C tree.

A pull-up voltage of 1.8V to 3.3V is supported.

| | |
|---|---|
| **Note:** | If I²C/SMBus pull-up resistors are detected by the USB5734 at start-up, the hub will wait indefinitely to be configured by the attached I²C/SMBus master. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I²C/SMBus master is fully operational and able to properly configure the hub at start-up. |

### 9.2.2 MASTER INTERFACE

The USB5734 has a I²C/SMBus master interface which can bridge USB commands to I²C/SMBus. Instructions for operating the I²C/SMBus master interface are contained in *AN1998 USB-to-I²C Bridging with Microchip USB 3.1 Gen 1 Hubs*.

In order to enter I²C/SMBus Master mode, the **CFG_STRAP** pin must set the hub into configuration 1, 2, 3, or 6, and pull-up resistors on the **SPI_DO/UART_TX/GPIO5/I2C_SLV_CFG1** and **SPI_CLK/UART_RX/GPIO4/I2C_SLV_CFG0** must not be detected at power-on.

Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient on the **SMDAT** and **SMCLK** pins, depending on the configured interface speed and total capacitance on I²C tree.

A pull-up voltage of 1.8V to 3.3V is supported.

Ensure that all I²C/SMBus slave devices connected to the bus have unique addresses assigned.

Ensure that the USB5734 and all I²C/SMBus slave devices connected to the bus can support the target bus speed.

## 9.3 UART Connections

There is one USB-to-UART interface available on USB5734.

The interface is enabled when Configuration 2 is selected through the **CFG_STRAP** pin. The pins are described in Table 9-3.

These signals may be attached directly to an embedded UART device or connect to an RS232 connector. If routing the UART signals to a RS232 connector, a UART transceiver is recommended.

**TABLE 9-3: UART PINS**

| Pin | PF Pin | Name | Role | Configuration Requirements |
|---|---|---|---|---|
| 43 | n/a/ | SPI_DO/UART_TX/ GPIO5/ I2C_SLV_CFG1 | UART Receiver | Configuration 6 (10Ω Pull-Up) |
| 44 | n/a | SPI_CLK/UART_RX/ GPIO4/ I2C_SLV_CFG0 | UART Transmitter | Configuration 6 (10Ω Pull-Up) |
| 50 | PROG_FUNC1 | UART_nRTSU-ART_RX | Optional UART | Configuration 6 (10Ω Pull-Up) |
| 39 | PROG_FUNC2 | UART_nCTSU-ART_TX | Optional UART | Configuration 6 (10Ω Pull-Up) |
| 40 | PROG_FUNC3 | UART_nDCD | Optional UART | Configuration 6 (10Ω Pull-Up) |
| 49 | PROG_FUNC6 | UART_nDTR | Optional UART | Configuration 6 (10Ω Pull-Up) |
| 16 | PROG_FUNC7 | UART_nDSR | Optional UART | Configuration 6 (10Ω Pull-Up) |

## 9.4 FlexConnect

The FlexConnect feature allows the USB2 and USB3 host role to be re-assigned to any of the downstream ports in the hub. This feature is highly implementation specific and usually has numerous hardware design ramifications. If the Flex-Connect feature is required in any specific application, it is recommended to reach out to a Microchip support representative early on in the design cycle to discuss the options available.

The FlexConnect feature and design guidelines are further explained in *AN1700 – FlexConnect Applications.*

## 9.5 Non-Removable Port Setting

In a typical USB5734 application, downstream Port 1 is routed to a user-accessible USB connector, and hence the downstream port should be configured as a removable port.

The USB5734 has a configuration strap option, **CFG_NON_REM**, which can be used to set the default configuration for Port 1. This is located on pin 45. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI flash device. These are described in Table 9-4.

**TABLE 9-4: CFG_NON_REM**

| Setting | Effect |
|---|---|
| 200 kΩ pull-down to GND | All ports removable<br>(recommended for most USB5734 applications) |
| 200 kΩ pull-up to 3.3V | Port 1 is non-removable. A valid selection only if Port 1 is connected directly to an embedded USB device. |
| 10 kΩ pull-down to GND | Ports 1 and 2 are non-removable. A valid selection only if Ports 1 and 2 are connected directly to embedded USB devices. |
| 10 kΩ pull-up to 3.3V | Ports 1, 2, and 3 are non-removable. A valid selection only if Ports 1, 2 and 3 are connected directly to embedded USB devices. |
| 10Ω pull-down to GND | Ports 1, 2, 3, and 4 are non-removable. A valid selection only if Ports 1, 2, 3, and 4 are connected directly to embedded USB devices. |

The following guidelines can be used to determine which setting to use:

- If the port is routed to a user-accessible USB connector, it is ***removable***.
- If the port is routed to a permanently attached an embedded USB device on the same PCB, or non-user-accessible wiring or cable harness, it is ***non-removable***.

**Note:** The removable/non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host may use to understand if a port is a user-accessible port, or if the device is a permanently attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs which must undergo USB compliance testing and certification must have correct configuration settings.

## 9.6 Self-Powered/Bus-Powered Settings

In a typical USB5734 application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which settings to use:

- If the entire system (hub included) is powered completely from the upstream USB connector's VBUS pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is ***bus-powered***.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is ***self-powered***.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely ***self-powered*** (even if all of the power is derived from the upstream USB connector's VBUS pin).

**Note:** The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device which connects to a self-powered hub that declares it needs more than 100 mA will be prevented from operating by the USB host.

## 9.7 Battery Charging Settings

The USB5734 hub includes built-in Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and vendor-specific (SE1) battery charging support.

The USB5734 has a configuration strap option, **CFG_BC_EN**, which can be used to set the default configuration for Port 1. This is located on pin 44. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI flash device. The configuration strap options are described in Table 9-5.

**TABLE 9-5: CFG_BC_EN**

| Setting | Effect | Additional Notes |
|---|---|---|
| 200k pull-down to GND | Port 1 BC disabled | Battery Charging is not enabled.<br><br>Select this option if configuration will be done in hub OTP, via $I^2C$/SMBus, or by external FW in SPI Flash.<br><br>If SE1 charging is required, this strap option should be selected and SE1 must be enabled in hub OTP, via $I^2C$/SMBus, or by external FW in SPI Flash. |
| 200k pull-up to 3.3V | Port 1 BC enabled | Battery Charging is enabled.<br><br>When no USB host is present (VBUS_DET = 0), downstream Port 1 operates in Dedicated Charging Port mode (DCP mode).<br><br>When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Port 1 operates in Charging Downstream Port mode (CDP mode). |
| 10 kΩ pull-down to GND | Port 1 and 2 BC enabled | Battery Charging is enabled.<br><br>When no USB host is present (VBUS_DET = 0), downstream Ports 1 and 2 operate in Dedicated Charging Port mode (DCP mode).<br><br>When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Ports 1 and 2 operate in Charging Downstream Port mode (CDP mode). |
| 10 kΩ pull-up to 3.3V | Port 1, 2, and 3 BC enabled | Battery Charging is enabled.<br><br>When no USB host is present (VBUS_DET = 0), downstream Ports 1, 2, and 3 operate in Dedicated Charging Port mode (DCP mode).<br><br>When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Ports 1, 2, and 3 operate in Charging Downstream Port mode (CDP mode). |
| 10Ω pull-down to GND | Port 1, 2, 3, and 4 BC enabled | Battery Charging is enabled.<br><br>When no USB host is present (VBUS_DET = 0), downstream Ports 1, 2, 3, and 4 operate in Dedicated Charging Port mode (DCP mode).<br><br>When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Ports 1, 2, 3, and 4 operate in Charging Downstream Port mode (CDP mode). |

**Note:** The vendor-specific SE1 charging mode uses the USB data lines to communicate charging capability. Hence, SE1 can only be active when no USB host is present. Additional vendor-specific charging modes exist for charging at elevated current levels when an active data connection is also present. This is handled by vendor-specific USB protocol between the USB host and the device. The USB5734 supports these vendor-specific protocol exchanges. These vendor-specific command specifications must be obtained from the respective device vendors.

# 10.0 HARDWARE CHECKLIST SUMMARY

## TABLE 10-1: HARDWARE DESIGN CHECKLIST

| Section | Check | Explanation | √ | Notes |
|---|---|---|---|---|
| Section 2.0, "General Considerations" | Section 2.1, "Pin Check" | Verify that the pins match the data sheet. | | |
| | Section 2.2, "Ground" | Verify that the grounds are tied together. | | |
| | Section 2.3, "USB-IF Compliant USB Connectors" | Verify that USB-IF compliant USB connectors with an assigned TID are used in the design (If USB compliance is required for the design.). | | |
| Section 3.0, "Power" | Section 3.1, "Power and Bypass Capacitance" | • Ensure **VDD33** is in the range 3.0V to 3.6V and a 0.1 µF capacitor is on each pin.<br>• Ensure **VDD12** is in the range 1.08V to 1.32V and a 0.1 µF capacitor is on each pin. | | |
| Section 4.0, "USB Signals" | Section 4.1, "Upstream Port USB Signals" | Verify that the USB data pins are correctly routed to the USB connectors. | | |
| | Section 4.2, "Downstream Port USB Signals" | Verify that the USB data pins are correctly routed to the USB connectors. | | |
| | Section 4.3, "Disabling Downstream Ports" | If any of the USB ports are unused, ensure they are properly disabled via pin strap. If pin strapping is not used, other methods may be used such as $I^2C$/SMBus configuration or OTP configuration. | | |
| | Section 4.4, "USB Protection" | Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB2 trace. Protection devices on USB3 traces should not add more than 0.5 pF on each line. | | |
| Section 5.0, "USB Connectors" | Section 5.1, "Upstream Port VBUS and VBUS_DET" | Verify that the Upstream Port VBUS has no more than 10 uF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub. | | |
| | Section 5.2, "Downstream Port VBUS and PRTCTLx Connections for Standard Type-A Ports" | Verify that for any downstream Type-A ports, the **PRT_CTLx** pins are properly connected to both the 'enable' pin of the downstream port power controller and the fault indicator output of the port power controller. | | |
| | Section 5.3, "Downstream Port VBUS and PRTCTLx Connections for Type-C Ports" | Verify that for any downstream Type-C ports, the **PRT_CTLx** pins are properly connected to both the 'enable' pin of the downstream Type-C port controller and the fault indicator output of the port switch or DC/DC regulator. | | |
| | Section 5.4, "GND and EARTH Recommendations" | Verify that the USB connector is properly connected to PCB ground on both the GND pins and the SHIELD pins. | | |
| Section 6.0, "Clock Circuit" | Section 6.1, "Crystal or External Clock Connection" | Confirm the crystal or clock is 25.000 MHz (±50 ppm). | | |

**TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)**

| Section | Check | Explanation | √ | Notes |
|---|---|---|---|---|
| Section 7.0, "Power and Startup" | Section 7.1, "RBIAS Resistor" | Confirm that a 12 kΩ 1% resistor is connected between the **RBIAS** pin and PCB ground. | | |
| | Section 7.2, "Board Power Supplies" | Verify that the board power supplies deliver 3.0V to 3.6V and 1.08V to 1.32V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. | | |
| | Section 7.3, "Reset Circuit" | Ensure that the **RESET_N** signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device. | | |
| Section 8.0, "External SPI Memory" | Section 8.1, "SPI Operation Summary" | Determine if a custom SPI FW image is required, and which mode of operation the selected SPI Flash device must support. | | |
| | Section 8.2, "Compatible SPI Flash Devices" | Ensure the selected SPI Flash device is compatible with the hub. | | |
| | Section 8.3, "SPI Connection Diagrams" | Verify that the SPI Flash is connected according to the diagram in Figure 8-1. Follow Figure 8-2 if no SPI Flash is connected in the design. | | |
| Section 9.0, "Miscellaneous" | Section 9.1, "GPIOs" | Verify that any GPIO pins that will be used as GPIOs within the application are connected properly, and never exceed the voltage maximum/minimum values or overload the current source/sink maximum values as defined by the hub data sheet. | | |
| | Section 9.2, "I2C/SMBus Connections" | If the USB to $I^2C$/SMBus slave interface is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the $I^2C$/SMBus master are correct. | | |
| | Section 9.2, "I2C/SMBus Connections" | If the USB to $I^2C$/SMBus Bridge feature is implemented, ensure that appropriate pull-up resistors are applied within the system only after the hub initialization and that the connections to the $I^2C$/SMBus slave devices are correct. | | |
| | Section 9.3, "UART Connections" | If using the USB-to-UART Bridge feature, ensure that Configuration 3 is selected via the **CFG_STRAP** pin and that the pin connections to the UART device or transceiver are correct. | | |
| | Section 9.4, "FlexConnect" | If using the FlexConnect feature, refer to *AN1700 FlexConnect Applications* and contact Microchip support for design and implementation assistance. | | |
| | Section 9.5, "Non-Removable Port Setting" | Verify that the CFG_NON_REM configuration strap is set per application requirements. | | |
| | Section 9.6, "Self-Powered/Bus-Powered Settings" | Verify the application requirements for Self-Powered or Bus-Powered operation. | | |
| | Section 9.7, "Battery Charging Settings" | Verify that the CFG_BC_EN configuration strap is set per application requirements. | | |

# APPENDIX A: REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision Level & Date | Section/Figure/Entry | Correction |
|---|---|---|
| DS00002968A (03-28-2019) | Initial release | |

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