MNE3002 Lab 3 15/11/2020
Double Dabble Binary-to-BCD Converter Luca Ruggier

Aim: To design a Double Dabble Binary-to-BCD Converter in VHDL, with an 8-bit input, and three 4-bit outputs representing the Hundreds, Tens, and Units.

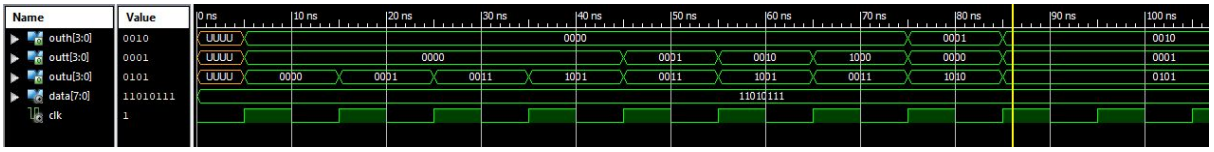
Method: The following three VHD files were created:

(These files have been hosted on Pastebin.com for easier sharing, please right click to open the files in a new tab if viewing this PDF in a browser)

DoubleDabble_tl.vhd
DoubleDabble.vhd
DoubleDabble_tb.vhd

These files include a testbench (DoubleDabble_tb.vhd) which tests the algorithm with a data input of 11010111 (decimal 215)

The VHDL code was simulated, and the following output waveform was captured:



(high res)

From this waveform, it can be seen that the Double Dabble Binary-to-BCD Converter behaves correctly by shifting the outputs, and finally settling on correct outputs of:
Hundreds: 0010 (2)
Tens: 0001 (1)
Units: 0101 (5)