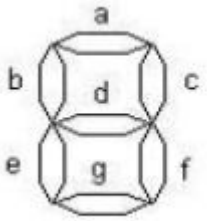
MNE3002 Lab 4 22/11/2020
Hex to SevenSegment & Counter Luca Ruggier

Aim:
To design a hex to seven segment decoder, and a 4 bit counter in VHDL.

Method:
Using the supplied diagram, 7 bit strings (in the form “abcdefg”) were made for each possible character output on the seven segment display. The strings are as follows:

0 : "1110111"	8 : "1111111”
1 : "0010010"	9 : "1111010”
2 : "1011101"	A : "1111110"
3 : "1011011"	B : "1111111"
4 : "0111010"	C : "1100101"
5 : "1101011"	D : "1110111"
6 : "1101111”	E : "1011101"
7 : "1010010"	F : "1110100"



These strings are later used in the VHDL code for the display driver.

The counter was then designed, ensuring all specifications were met. Namely:

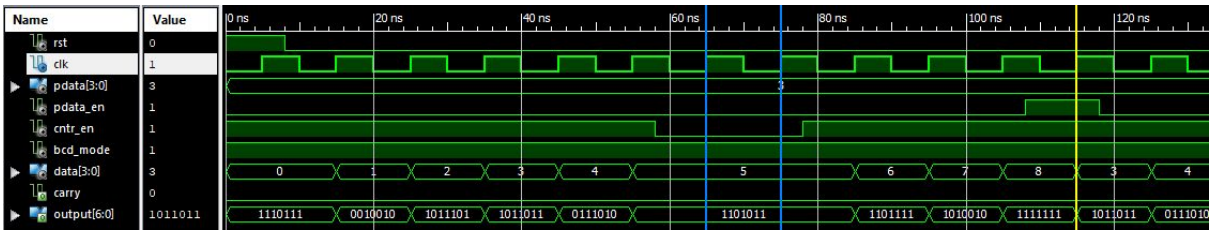
- That it is a 4-bit counter
- That it included an asynchronous reset and carry out
- A pData enable signal, which sets the clock to the value of the pData signal on the next clock cycle
- A BDC_mode signal which defined whether or not the counter counts to 9 or 15
- A counter enable pin that enabled the counter

With the above criteria in mind, and the aforementioned seven segment strings on hand, the VHDL modules for the two components were created. The two components were then described in a top level VHDL module, and a test bench component was created to test all the functionality of the counter, which was connected to the counter in the top level.

The four VHDL files can be seen below:
(These files have been hosted on Pastebin.com for easier sharing, please right click to open the files in a new tab if viewing this PDF in a browser)

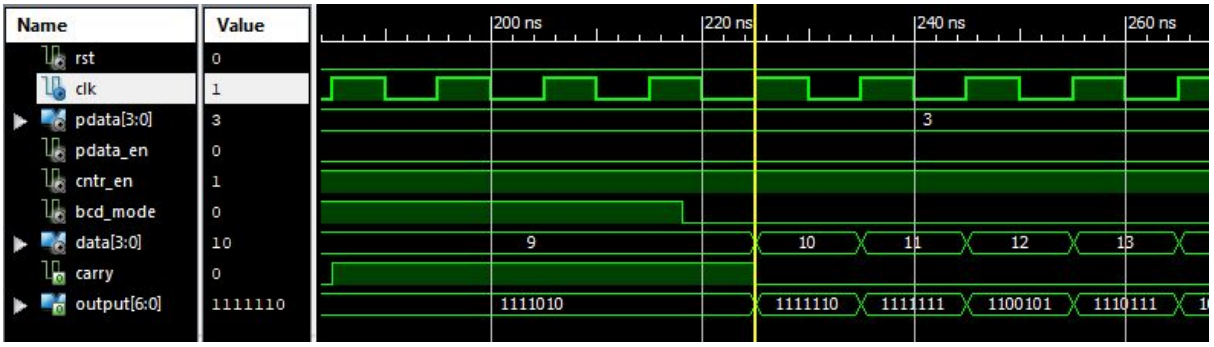
SevenCounter_tl.vhd
Counter.vhd
DisplayDriver.vhd
SevenCounter_tb.vhd

The VHDL project was simulated and the following two screenshots were taken:



(high res)

In this screenshot, it can be seen that while CNTR_en is high, the counter (data) counts with every clock pulse. When CNTR_en is set low, the counter does not count, this can be seen on the two clock pulses marked with the blue lines.
It can also be seen that in this screenshot, when pData_en is set high, that the counter takes the value of pData. This is marked with a yellow line.



(High res)

In this screenshot, it can be seen that initially BCD_mode is set high, declaring that the counter will count to 9. It can also be seen that the counter has stopped at 9, and the carry is high. When BCD_mode is set low, the counter now starts counting again up to 15, this is shown with the yellow line.

In both screenshots, it can be seen that the 7-bit value, “output,” resembles the output from the seven segment display drivers, and follows the value of the counter data.