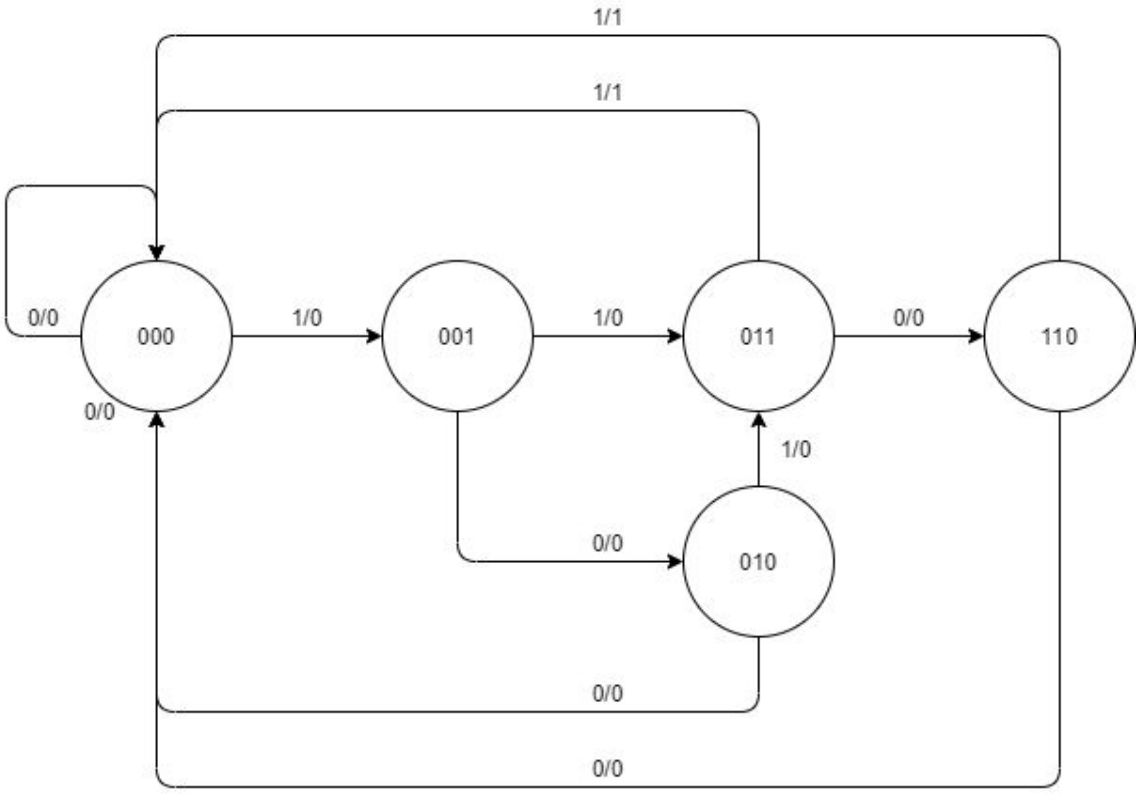
MNE3002 Lab 1 01/11/2020
Finite State Machine - 3 Counter Luca Ruggier

Aim: To design a synchronous finite state machine which detects three near 1's in an input stream, and then outputs a 1. The counter is reset by two consecutive 0's. The finite state machine was then replicated in VHDL code, and simulated with a test bench to verify that the code was correct.

Method: First, the finite state machine was designed using a mealy model and can be seen below.



Then the state machine was implemented in VHDL code. The following 3 files were created:

(These files have been hosted on Pastebin.com for easier sharing, please right click to open the files in a new tab if viewing this PDF in a browser)

Counter3_tl.vhd
Counter3.vhd
Counter3_tb.vhd

Finally, the project was simulated and the following output waveforms were

(full res)

The following can be noted from the waveform:

1. The 3 blue lines indicate a correct count of 1 - 1 - 0 - 1, which then outputs a 1 on the 3rd blue line, as expected.
2. The red lines indicate that the counter counts two 1's but is then reset by the double zero on the second pair of red lines.
3. The 3 yellow lines again show that after the aforementioned reset, the counter functions correctly, counts 1 - 0 - 1 - 1, and output's a 1 on the 3rd yellow line.