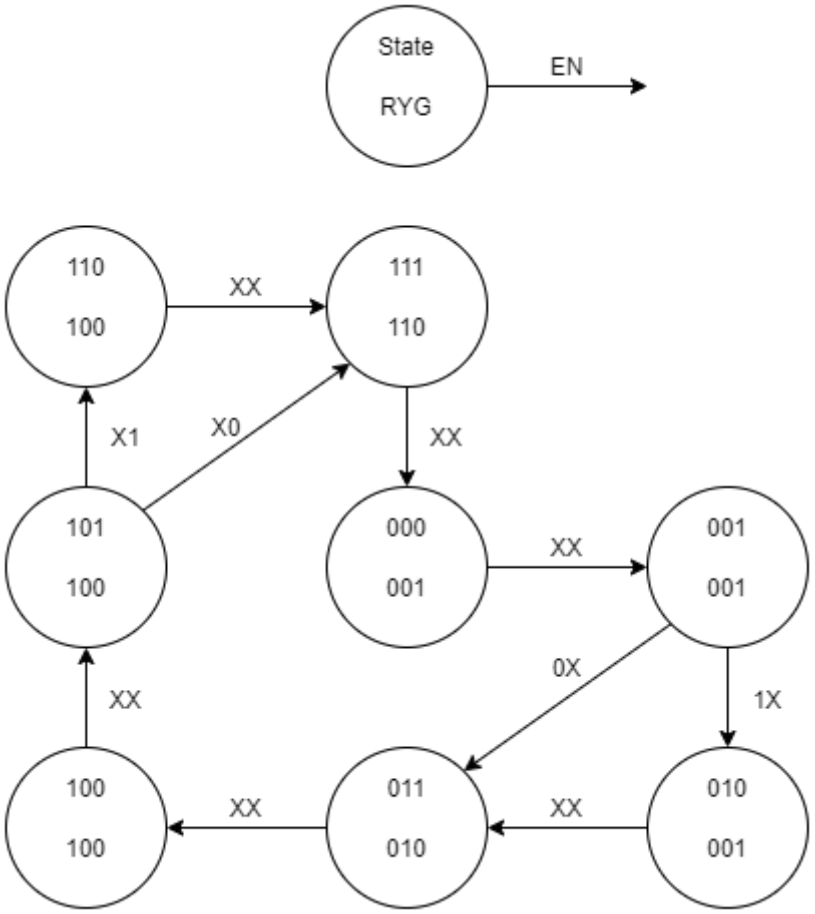
MNE3002 Lab 2 08/11/2020
Finite State Machine - Traffic Light Luca Ruggier

Aim: To design a synchronous finite state machine which controls a traffic light, with two inputs E (for East - West traffic) and N (for North - South traffic), and three outputs, R, Y and G for the colours red, yellow and green.

Method: First, the finite state machine was designed using a moore model and can be seen below. (State 000 is the initial state)

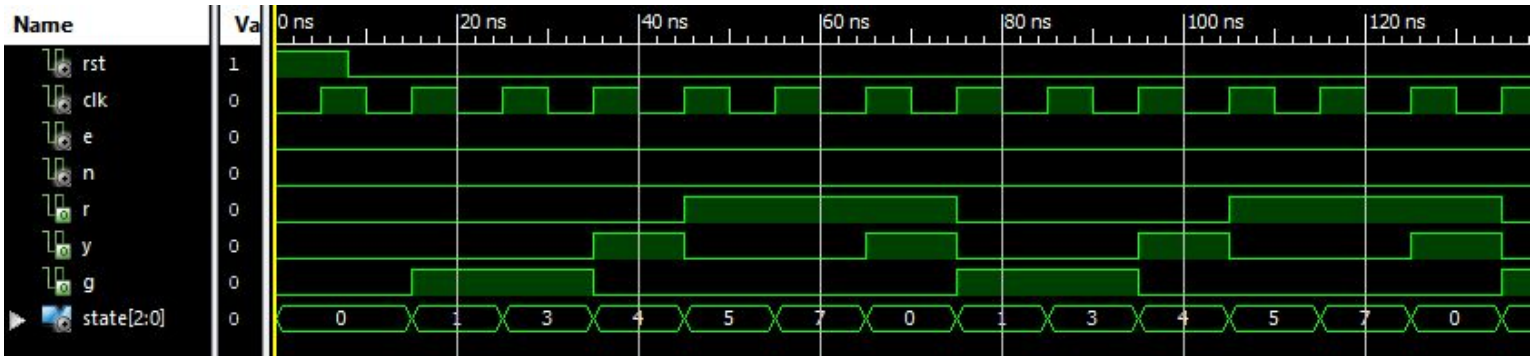


Then the state machine was implemented in VHDL code. The following 2 files were created:

(These files have been hosted on Pastebin.com for easier sharing, please right click to open the files in a new tab if viewing this PDF in a browser)

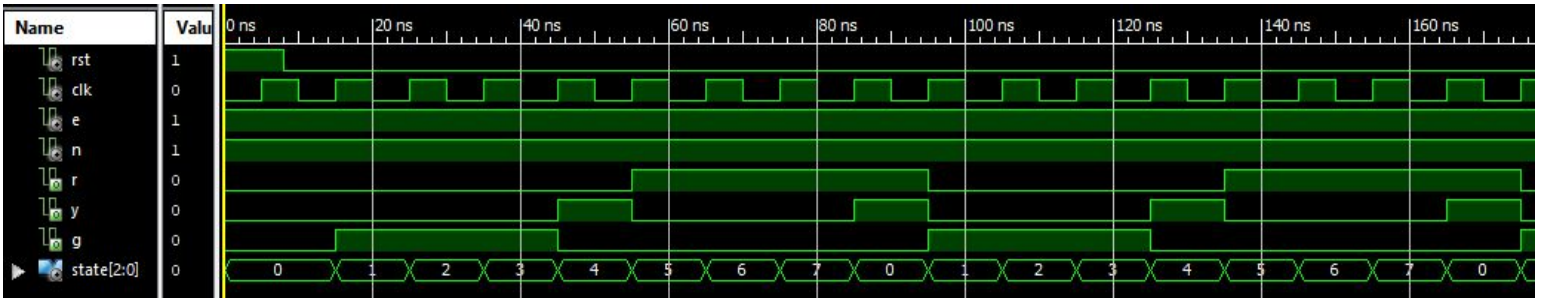
TrafficLight.vhd
TrafficLight_tb.vhd

Finally, the project was simulated and the following output waveforms were captured:



(high res)

In this waveform, E and N are set LOW. This results in states 2 (010) and 6 (110) to be skipped. It can be seen that all other outputs are correct. G is high for two clock cycles, followed by Y high for 1 clock cycle. Then R is high for two clock cycles and finally R and Y are both high for 1 clock cycle before the state machine returns back to the zeroth state.



(high res)

In the second waveform, E and N are now set HIGH. This results in states 2 (010) and 6 (110) to not be skipped. It can be seen that all other outputs remain correct. G is now high for **three** clock cycles, followed by Y high for 1 clock cycle. Then R is now high for **three** clock cycles and finally R and Y are both high for 1 clock cycle before the state machine returns back to the zeroth state once again.