LUCA URBINATI

Electronic Engineer
PhD Fellow

13/02/1995
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Driving licence: B
Italian: native language
English: B2 IELTS 2017

Personal Interests

I am passionate about travel, photography and digital marketing. I love cycling and sailing. I like food, watching dystopian movies, and playing board games.

Education

POLITECNICO DI TORINO
PhD in Hardware Accelerators for Deep Learning • 2020-Now

POLITECNICO DI TORINO
Electronic Engineering: Electronic Systems • 110/110 • 2017-2019

LINKÖPING UNIVERSITET
European Union Programme ERASMUS+ • 2016-2017 (5 months)

UNIVERSITY OF BOLOGNA (CESENA HEADQUARTER)
Electronic Engineering for Energy and Information • 109/110 • 2014-2017

Last update: 10/06/2024

Work Experience

NOW - MAY 2020

PHD STUDENT AT POLITECNICO DI TORINO

- **Digital Hardware Designer of Deep Learning accelerators and precision-scalable multipliers**

Skills: High-Level synthesis (Catapult HLS, C language), Design and simulation of RTL and gate-level digital circuits (VHDL, QuestaSim), Logic synthesis (Design Compiler), Scripting (Python, Bash, TLC), Versioning (GitHub), Linux environment, Time management.

- **End-to-end Machine-Learning projects**

Skills: Data collection, Data pre-processing (Scikit-Learn), Model training (TensorFlow, Keras), Hyper-parameters tuning (Bayesian Optimization), Quantization (QKeras), Pruning, Inference on microcontrollers or FPGAs (TFLite/LiteMicro, Vivado).

- **Author and co-author of 10+ scientific papers**

Skills: Scientific paper writing (LaTex, Draw.io, Gnuplot), Analytical & synthesis skills, Team working.

- **Reviewer of 5+ scientific papers**

Skills: Critical thinking, attention to details, objectivity, communication skills.

- **Presenter at 5+ national/international conferences**

Skills: Slide and poster creation (Power Point, Prezi), Public speaking, Networking.

- **Co-supervisor of 7+ Master's thesis students**

Skills: Linux administration (e.g. accounts, lxc containers) and software installation (e.g. pip, conda), Project management (define students' activities and deadlines).

- **Lab assistant for the Microelectronics Course held by Prof. Casu, for Academic Years 2022/2023, 2021/2022**

Skills: Simulations and layout of simple digital circuits, DRC and LVS (Cadence Virtuoso).

Other Soft Skills

- Autonomy & Team Working
- International Spirit
- Friendly
- Open-minded & Curious
- Problem Solving
- Meticulous
- Continuous Learning
- Public Speaking

Publications

MAR 2024
HIGH-LEVEL DESIGN OF PRECISION-SCALABLE DNN ACCELERATORS BASED ON SUM-TOGETHER MULTIPLIERS
Urbinati L., and Casu M.R., in IEEE Access, vol. 12, pp. 44163–44189, 2024.

MAR 2024
STAR: SUM-TOGETHER/APART RECONFIGURABLE MULTIPLIERS FOR PRECISION-SCALABLE ML WORKLOADS
Manca E., Urbinati L., and Casu M.R., in Proc. of Design, Automation & Test in Europe (DATE) 2024, IEEE, Valencia (Spain).

NOV 2023
ACCELERATING QUANTIZED DNN LAYERS ON RISC-V WITH A STAR MAC UNIT
Manca E., Urbinati L., and Casu M.R., in Proc. of 2023 Annual Meeting of the Italian Electronics Society (SIE), Springer, Noto (Italy).

SEP 2023
ENHANCED MACHINE-LEARNING FLOW FOR MICROWAVE-SENSING SYSTEMS TO DETECT CONTAMINANTS IN FOOD
Štitic B., et al., in Proc. of 2023 Int. Conference on Agrifood Electronics (CAFE), pp. 40–44, IEEE, Turin (Italy).

JUN 2023
DESIGN-SPACE EXPLORATION OF MIXED-PRECISION DNN ACCELERATORS BASED ON SUM-TOGETHER MULTIPLIERS
Urbinati L. and Casu M.R., in Proc. of 2023 PRIME, pp. 377–38, IEEE, Valencia (Spain).

Awards

BEST STUDENT PAPER AWARD AT 2023 CAFE CONFERENCE

As co-author of the work: "Enhanced Machine-Learning Flow for Microwave-Sensing Systems to Detect Contaminants in Food" · Certificate · Sep 2023.

GOLD LEAF AWARD AT 2023 PRIME CONFERENCE

For ranking among the top 10% of the best papers with my work: "Design-Space Exploration of Mixed-precision DNN Accelerators based on Sum-Together Multipliers" · Certificate · Jun 2023.

YOUNG FELLOWS POSTER PRESENTATION AWARD AT 2020 DESIGN AUTOMATION CONFERENCE (DAC).

One of the best 2-minutes elevator pitches, presenting my Master's Thesis work: "Detection of food contaminants with Microwave Sensing and Machine Learning" · Certificate · Jul 2020.

NOV 2022 — **A RECONFIGURABLE DEPTH-WISE CONVOLUTION MODULE FOR HETEROGENEOUSLY QUANTIZED DNNS**

Urbinati L. and Casu M.R., in Proc. of 2022 Int. Symposium on Circuits and Systems (ISCAS), pp. 128-132, IEEE, Austin, (TX, USA).

SEP 2022 — **A RECONFIGURABLE 2D-CONVOLUTION ACCELERATOR FOR DNNS QUANTIZED WITH MIXED-PRECISION**

Urbinati L. and Casu M.R., in Proc. of 2022 ApplePies, pp. 210–215, Springer, Genoa (Italy).

SEP 2022 — **A RECONFIGURABLE MULTIPLIER/DOT-PRODUCT UNIT FOR PRECISION-SCALABLE DEEP LEARNING APPLICATIONS**

Urbinati L. and Casu M.R., in Proc. of 2022 Annual Meeting of the Italian Electronics Society (SIE), Springer, Pizzo (Italy).

JUL 2021 — **MACHINE-LEARNING-BASED MICROWAVE SENSING: A CASE STUDY FOR THE FOOD INDUSTRY**

Ricci M., et al., in Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 11(3), pp. 503–514, IEEE.

OCT 2020 — **A MACHINE-LEARNING BASED MICROWAVE SENSING APPROACH TO FOOD CONTAMINANT DETECTION**

Urbinati L. et al., in Proc. of 2020 Int. Symp. Circuits and Systems (ISCAS), IEEE, Seville (Spain).

OCT 2019 — **FAULT TOLERANT PHOTOVOLTAIC ARRAY: A REPAIR CIRCUIT BASED ON MEMRISTOR SENSING**

Gnoli L., et al., in Proc. of 2019 Int. Symp. Defect and Fault Tolerance in VLSI and Nanotech. Systems (DFT), IEEE, Noordwijk (The Netherlands).

Main University Projects

DEC 2019 — **TRAINING OF MACHINE-LEARNING MODELS AND HARDWARE IMPLEMENTATION ON FPGA (MASTER'S THESIS)**

- Detection of food contaminants in hazelnut-cocoa spread jars using Microwave Sensing and Machine Learning: training Support Vector Machine (SVM) and Multilayer Perceptron (MLP) binary classifiers, generate artificial datasets, hyper-parameter search with grid-search and Bayesian Optimization, hardware accelerator of the best MLP model on FPGA.

Skills: Python, Scikit-Learn, Keras, Jupyter Notebook, conda, Matlab, hls4ml, Vivado HLS).

GEN 2019 - OCT 2017 — **DIGITAL HARDWARE DESIGN (TEAMWORKS)**

- Finite Impulse Response (FIR) filter with unfolding and pipelining
- Modified Booth Encoded Multiplier with compressor.
- MIPS-lite processor with data hazard bypasses (VHDL, QuestaSim).
- Logic circuit based on memristor sensing for fault-tolerant photovoltaic arrays: optimize solar cell connections to boost output power and prevent hot spots (paper).
- Fault Tolerant Photovoltaic Array
- Logic Analyzer with 8 channels, programmable sampling frequency, trigger condition, glitch detector, RS232 interface, tested on Altera DE2.
- Radix-2 "Butterfly" Fast Fourier Transform (FFT) processing element.
- CMOS AND4 X1 standard cell: transistor sizing, schematic, simulation, layout, characterization with parasitics extraction.

Skills: VHDL, QuestaSim, Quartus, Cadence Virtuoso, Teamworking.

OCT 2017 — **PRINTED CIRCUIT BOARD (PCB) DESIGN WITH DISCRETE COMPONENTS (BACHELOR'S THESIS)**

- Interface circuit based on Near-Field Communication (NFC) for low-power sensor nodes: circuit design, research of components on the market, datasheet, breadboard prototyping, PCB design, microcontroller programming.

Skills: LTSpice, KiCad, C language.

JUN 2017 — **FRONT-END DEVELOPMENT**

- Smartphone App called "Rimini Audioguida": play Italian/English audioguides in proximity of the main monuments of Rimini's city center.

Skills: HTML, JavaScript, CSS, Apache Cordova.