



LUCA URBINATI

Electronic Engineer

PhD Fellow

13/02/1995

Rimini, RN, Italy

+39 340 1967521

luca.urbinati.44@gmail.com

linkedin.com/in/luca-urbinati/

Driving licence: B



Italian: native language



English: B2 IELTS 2017

Personal Interests

I am passionate about travel, photography and digital marketing. I love cycling and sailing. I like food, watching dystopian movies, and playing board games.

Education

POLITECNICO DI TORINO

PhD in Hardware Accelerators for Deep Learning • 2020-Now

POLITECNICO DI TORINO

Electronic Engineering: Electronic Systems • 110/110 • 2017-2019

LINKÖPING UNIVERSITET

European Union Programme ERASMUS+ • 2016-2017 (5 months)

UNIVERSITY OF BOLOGNA (CESENA HEADQUARTER)

Electronic Engineering for Energy and Information • 109/110 • 2014-2017

Work experience

NOW

-

MAY

2020

PHD STUDENT AT POLITECNICO DI TORINO

- **Digital Hardware Designer of Deep Learning accelerators and precision-scalable multipliers**

Skills: High-Level synthesis (Catapult HLS, C language), Design and simulation of RTL and gate-level digital circuits (VHDL, QuestaSim), Logic synthesis (Design Compiler), Scripting (Python, Bash, TLC), Versioning (GitHub), Linux environment, Time management.

- **End-to-end Machine-Learning projects**

Skills: Data collection, Data pre-processing (Scikit-Learn), Model training (TensorFlow, Keras), Hyper-parameters tuning (Bayesian Optimization), Quantization (QKeras), Pruning, Inference on microcontrollers or FPGAs (TFLite/LiteMicro, Vivado).

- **Author and co-author of 10+ scientific papers**

Skills: Scientific paper writing (LaTeX, Draw.io, Gnuplot), Analytical & synthesis skills, Team working.

- **Presenter at 5 national/international conferences**

Skills: Slide and poster creation (Power Point, Prezi), Public speaking, Networking.

- **Co-supervisor of 7+ Master's thesis students**

Skills: Linux administration (e.g. accounts, lxc containers) and software installation (e.g. pip, conda), Project management (define students' activities and deadlines).

- **Lab assistant for the Microelectronics Course held by Prof. Casu.**

Skills: Simulations and layout of simple digital circuits, DRC and LVS (Cadence Virtuoso).

Other Soft Skills

- Autonomy & Team Working
- International Spirit
- Friendly
- Open-minded & Curious

- Problem Solving
- Meticulous
- Continuous Learning
- Public Speaking

Main Publications

JUN

2023

DESIGN-SPACE EXPLORATION OF MIXED-PRECISION DNN ACCELERATORS BASED ON SUM-TOGETHER MULTIPLIERS

Urbinati L. and Casu M.R., in Proc. of 2023 International Conference on PhD Research in Microelectronics and Electronics (PRIME), pp. 377–38, IEEE, Valencia (Spain).

NOV

2022

A RECONFIGURABLE DEPTH-WISE CONVOLUTION MODULE FOR HETEROGENEOUSLY QUANTIZED DNNs

Urbinati L. and Casu M.R., in Proc. of 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, (TX, USA).

SEP

2022

A RECONFIGURABLE MULTIPLIER/DOT-PRODUCT UNIT FOR PRECISION-SCALABLE DEEP LEARNING APPLICATIONS

Urbinati L. and Casu M.R., in Proc. of 2022 Annual Meeting of the Italian Electronics Society (SIE), pp. 9–14, Springer, Pizzo (Italy).

JUL

2021

MACHINE-LEARNING-BASED MICROWAVE SENSING: A CASE STUDY FOR THE FOOD INDUSTRY

Ricci M., et al., in IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 11(3), pp. 503–514.

OCT

2020

A MACHINE-LEARNING BASED MICROWAVE SENSING APPROACH TO FOOD CONTAMINANT DETECTION

Urbinati L. et al., in Proc. of 2020 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1–5, Seville (Spain).

Main Courses

PARALLEL AND DISTRIBUTED COMPUTING

25 hours • PhD School of Politecnico di Torino • Prof. Savino • Jul 2021

- Classification of parallel and distributed computers: SIMD (GPUs, Vector processors) and MIMD (Multi-core processors, Clusters).
- Amdahl's law.
- Multithreading, Message passing Interface (MPI), OpenMP.
- Profiler.
- PCI, PCI-Express, Infiniband.

BIG DATA PROCESSING AND PROGRAMMING

20 hours • PhD School of Politecnico di Torino • Prof. Trevisan • Mar 2021

- Introduction to Big data: characteristics, problems, opportunities.
- Hadoop: infrastructure and basic components.
- Apache Spark Architecture.
- Spark RDD programming.
- Spark DataFrame programming.
- Lab on developing applications by means of Spark using Python.

OPERATING SYSTEMS

60 hours • Master's course of Politecnico di Torino • Prof. Rebaudengo • Jun 2019

- Operating system architecture.
- Processes and Threads.
- Process synchronization: mutex, condition variables, semaphores, message passing.

STRUCTURING MACHINE LEARNING PROJECTS

6 hours • DeepLearning.AI on Coursera.org • Instructors: Andrew Ng, Younes Bensouda Mourri, Kian Katanforoosh • Mar 2021 • [Certificate](#).

- How to split data in Train/Dev/Test distributions, and size Dev and Test sets.
- Which evaluation metrics to use
- Error analysis.

LEAN STARTUP E LEAN BUSINESS FOR L'INNOVATION MANAGEMENT

20 hours • PhD School of Politecnico di Torino • Prof. Perboli • Jul 2021.

- Development of business idea: Value Proposition Canvas, Porter's 5 Forces, SWAT Analysis, Business Model Canvas.

Awards

JUN
2023

GOLD LEAF AWARD AT 2023 PRIME CONFERENCE

- For ranking among the top 10% of the best papers with my work entitled "Design-Space Exploration of Mixed-precision DNN Accelerators based on Sum-Together Multipliers". [Certificate](#).

JUL
2020

YOUNG FELLOWS POSTER PRESENTATION AWARD AT 2020 DESIGN AUTOMATION CONFERENCE (DAC).

- For one of the best students' poster presentations as a 2-minutes elevator pitch. I was presenting my Master's Thesis work entitled: "Detection of food contaminants with Microwave Sensing and Machine Learning". [Certificate](#).

Main University Projects

DEC
2019

TRAINING OF MACHINE-LEARNING MODELS AND HARDWARE IMPLEMENTATION ON FPGA ([MASTER'S THESIS](#))

- Detection of food contaminants in hazelnut-cocoa spread jars using Microwave Sensing and Machine Learning: training Support Vector Machine (SVM) and Multilayer Perceptron (MLP) binary classifiers, generate artificial datasets, hyper-parameter search with grid-search and Bayesian Optimization, hardware accelerator of the best MLP model on FPGA.

Skills: Python, Scikit-Learn, Keras, Jupyter Notebook, conda, Matlab, hls4ml, Vivado HLS).

GEN
2019

DIGITAL HARDWARE DESIGN (TEAMWORKS)

- Finite Impulse Response (FIR) filter with unfolding and pipelining
- Modified Booth Encoded Multiplier with compressor.
- MIPS-lite processor with data hazard bypasses (VHDL, QuestaSim).
- Logic circuit based on memristor sensing for fault-tolerant photovoltaic arrays: optimize solar cell connections to boost output power and prevent hot spots ([paper](#)).
- Fault Tolerant Photovoltaic Array
- Logic Analyzer with 8 channels, programmable sampling frequency, trigger condition, glitch detector, RS232 interface, tested on Altera DE2.
- Radix-2 "Butterfly" Fast Fourier Transform (FFT) processing element.
- CMOS AND4 X1 standard cell: transistor sizing, schematic, simulation, layout, characterization with parasitics extraction.

Skills: VHDL, QuestaSim, Quartus, Cadence Virtuoso, Teamworking.

OCT
2017

PRINTED CIRCUIT BOARD (PCB) DESIGN WITH DISCRETE COMPONENTS ([BACHELOR'S THESIS](#))

- Interface circuit based on Near-Field Communication (NFC) for low-power sensor nodes: circuit design, research of components on the market, datasheet, breadboard prototyping, PCB design, microcontroller programming.

Skills: LTSpice, KiCad, C language.

JUN
2017

FRONT-END DEVELOPMENT

- Smartphone App called "[Rimini Audioguida](#)": play Italian/English audioguides in proximity of the main monuments of Rimini's city center.

Skills: HTML, JavaScript, CSS, Apache Cordova.