Abstract

In this project, an optical heart rate sensor was designed and tested to detect heart rates between 40 BPM to 200 BPM using a single 5 V supply while producing a digital output and LED indication for each detected heartbeat. The circuit used an infrared emitter and infrared phototransistor pair to generate a small AC waveform riding on a large DC offset. Following this, a single-supply high-pass filter, 2nd-order multiple-feedback low-pass filter, and an inverting amplifier were used to filter the small AC signal to the specified range while adding gain. Lastly, an LM339 comparator with hysteresis was used to generate a digital pulse output with the filtered signal. The optical sensor produced a DC offset of about 2.662 V with an approximately 40 mV peak-to-peak heartbeat signal. The high pass filter measured a cutoff of 679.5 mHz (40.77 BPM and 1.93% error) with a gain of 26.99 dB (2.78% error from designed value). The low-pass filter measured a cutoff of 3.621 Hz (217.26 BPM and 8.63% error). When cascaded together, the initial filter chain exhibited significant shifts in the cutoff values (a range of 28.5 BPM - 281 BPM), so the circuit was experimentally modified until the overall band pass response matched the target range closely (40.46 BPM - 200.34 BPM). The ADC output successfully produced digital pulses for each heartbeat with a measured peak-to-peak amplitude near 4.48 V (a 10.4% error from 5 V) and a visible LED flashing in sync with the heart rate as measured by a finger on the jugular vein.

Components List:

- Analog Discovery 2 (AD2)
- Breadboard
- IR204 infrared LED
- PT204-6B infrared phototransistor
- LM324N chip
- LM339 chip
- Various resistors and capacitors
- Multiple 10 kΩ potentiometers
- TLHG6400 green LED
- IRFZ44Z NMOS

Introduction

Optical heart rate sensors use photoplethysmography (PPG) to detect the small changes in transmitted light that result from blood flow. Due to the low amplitude and large DC component of the signals produced by phototransistors, the pulsing blood flow frequency

can be difficult to cleanly differentiate from noise and offset. The objective of this project was to design a reliable heart rate sensor capable of detecting a range of 40 BPM to 200 BPM with a digital output of 0 V to 5 V and LED triggering whenever a heartbeat is detected using a single 5 V supply.

This was done by configuring an infrared LED and phototransistor to capture the initial analog heartbeat signal. Following this, a reference voltage (Vref) was created to bias the signal for a single 5 V supply to allow for effective AC coupling and amplification without saturation. Next, the signal was processed through active high and low pass filters to isolate the 40 – 200 BPM band before an inverting amplifier provided extra gain and corrected signal inversion. Lastly, a comparator setup with hysteresis was used to convert the filtered waveform into a digital 0 – 5 V heartbeat signal that triggered an LED indicator for visible confirmation.

Theory

The heart rate sensing circuit can be broken down into three key subsystems: the optical sensor, the active filter cascade, and the analog-to-digital converter (ADC). The following section explains how each subsystem operates and how they work together to produce a digital heartbeat signal.

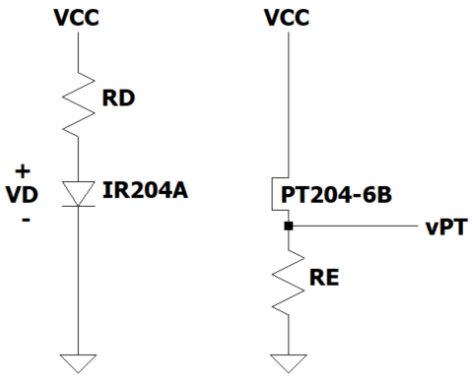

Figure 1: The optical sensor.

The optical sensor (figure 1) is the first stage of the circuit, comprising of an infrared emitter, a phototransistor, and various resistors. The LED emits an infrared light which then passes through a finger before entering a phototransistor. Because blood flow pulses naturally with each heartbeat, more light will be blocked when blood pulses through the fingertip, thus creating a small AC signal through the phototransistor.

The emitter and phototransistor must be designed to operate at the same wavelength and are typically chosen as a pair. The resistors determine the brightness of the emitter and the

DC offset of the heartbeat signal. Using Ohm's law across R_D, the current through the emitter can be written as follows:

$$I_D = \frac{V_{CC} - V_D}{R_D} \quad (Eq. 1)$$

The value for V_D can be found on the emitter's datasheet and it is important to note that the maximum power rating of the resistors is 0.25 Watt. Ohm's law can be used again to determine the DC offset of v_{PT} as follows:

$$v_{PT} = i_{PT} R_E \quad (Eq. 2)$$

Even though i_{PT} is proportional to the light received by the phototransistor, it is not easy to calculate the amount of light that will pass through a finger in practice. As a result, it is better to design R_E experimentally.

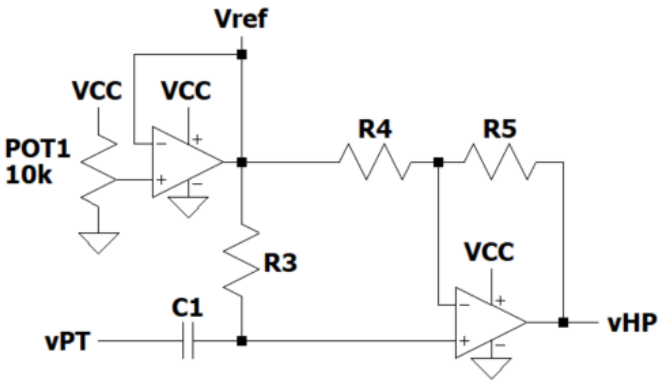

Figure 2: The single-supply high pass filter.

The noninverting high pass filter (figure 2) follows the optical sensor and is the first stage of the filter cascade. It takes the AC signal, removes the DC bias using a capacitor, introduces a reference bias to allow for the op amp to function properly, and then processes the AC signal to only output frequencies above a designed value. The theoretical cutoff frequency, f_C, and gain, k, of the high pass filter can be found by looking at the poles and zeros of the filter's transfer function:

$$H(s) = \frac{s\left(1 + \frac{R_5}{R_4}\right)}{s + \frac{1}{R_3 C_1}} \quad (Eq. 3)$$

$$\omega_0 = \frac{1}{R_3 C_1} = 2\pi f_c \quad (Eq. 4)$$

$$k = 1 + \frac{R_5}{R_4} \quad (Eq. 5)$$

The reference bias, V_{REF}, should be designed so that it sits at the center of the common mode input range of the selected op amps. To make the process of setting V_{REF} easier and more precise, a potentiometer has been selected to be adjusted experimentally.

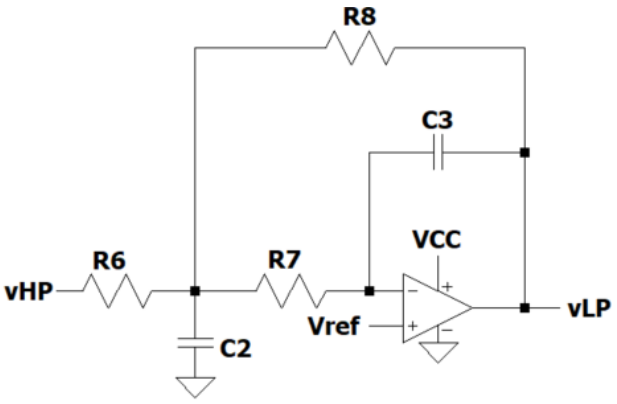

Figure 3: The 2nd-order, multiple feedback, single-supply low-pass filter.

The second stage in the filter cascade is the low-pass filter (figure 3). This filter receives the signal processed by the high pass filter and further removes all the frequencies above a designed threshold, creating a pass band effect. It is important to again introduce V_{REF} to ensure that input signal meets the common mode input range and output voltage swing. The transfer function of the filter can be modeled as follows:

$$H(s) = \frac{\frac{1}{R_7 R_6 C_2 C_3}}{s^2 + s\frac{1}{C_2}\left(\frac{1}{R_8} + \frac{1}{R_7} + \frac{1}{R_6}\right) + \frac{1}{R_8 R_7 C_2 C_3}} = \frac{b_0}{s^2 + a_1 s + a_0}, \omega_0 = a_0^{\frac{1}{2}}, Q = \frac{\omega_0}{a_1} \quad (Eq. 6)$$

Due to the complexity of the system, it is easier to use placeholder values initially and then experimentally test different resistors and capacitors to get as close to the desired cutoff as possible.

While the low-pass filter functions perfectly for its goal of cutting off high frequencies, at small cutoff values it exhibits very small gains. Because it is desired for the filter cascade to have a gain between 100 and 1000 while keeping individual stage gains less than 100, it is necessary to introduce an additional gain stage. Also, the low-pass filter inverts the input signal, to correct for this the additional gain stage should be inverting.

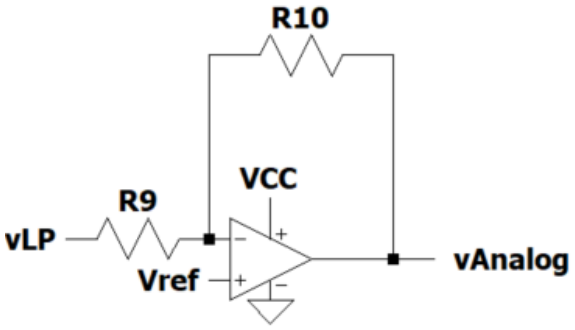

Figure 4: The inverting amplifier.

An inverting amplifier (figure 4) has been selected to represent this gain stage due to its simplicity and capability. The model and gain for the amplifier are as follows:

$$v_{Analog} - V_{REF} = -\frac{R_{10}}{R_9}(v_{LP} - V_{REF}) \qquad (Eq.7)$$

$$k = -\frac{R_{10}}{R_9} \qquad (Eq.8)$$

A major deviation in this design compared to a typical inverting amplifier is the use of V_{REF} instead of a ground through the noninverting input channel. This is necessary to ensure that the input signal rides along the op amps common mode range and keeps the filter working properly.

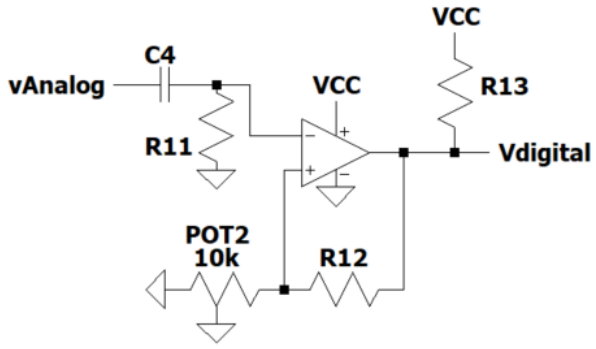

Figure 5: The analog-to-digital converting comparator.

The last subsystem of the heart rate sensor is the ADC and indicator. The ADC uses a comparator to output either 0 V or 5 V when a heartbeat is detected on the analog input signal. Prior to the comparator, a capacitor is used to remove any DC bias in the signal. Then the comparator uses two resistors to determine what amount of hysteresis, v_{hyst}, should be ignored by the comparator. This can be thought of as the remaining noise on the

heartbeat signal and allows the comparator to only trigger when a true heartbeat is detected. This value can be designed using the following equation:

$$v_{hyst} = V_{CC}\frac{R_{12}}{POT_2 + R_{12}} \qquad (Eq. 9)$$

To simplify design, a potentiometer has been used in place of a resistor to act as the effective resistance from the noninverting input channel to ground and allow for better tuning of comparator toggling.

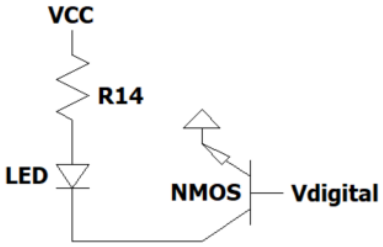

Figure 6: The LED indicator.

The last part of the heart rate sensor is the indicator that triggers when the digital input signal is high. An NMOS takes the digital input initially and becomes an open circuit when the signal is low, allowing no current to flow through the LED. When the signal is high, the NMOS becomes a low resistance path to ground, closing the circuit and allowing current to flow. Any color LED can be selected however the resistor, R_{14} should be chosen to maximize the current, and thus brightness, through the LED. The current through the LED can be approximated as follows (where V_F is the chosen LED's forward voltage):

$$I_{LED} \approx \frac{V_{CC} - V_F}{R_{14}} \qquad (Eq. 10)$$

Design

Using the equations laid out in the previous theory section, the heart rate sensing circuit was designed to meet the project specifications. It should be noted that the low-pass filter and inverting amplifier were designed experimentally.

Results

During experimentation, the high pass and low-pass stages produced accurate cutoff frequencies when tested individually, but the combined band pass cascade exhibited inaccurate cutoffs. In order to correct this, a second circuit was experimentally designed to have a more accurate band pass response, despite the individual filters being inaccurate.

For clarity, the following section will first present the results from the initial design (accurate individual filters) and then present results from the revised design (accurate band pass behavior).

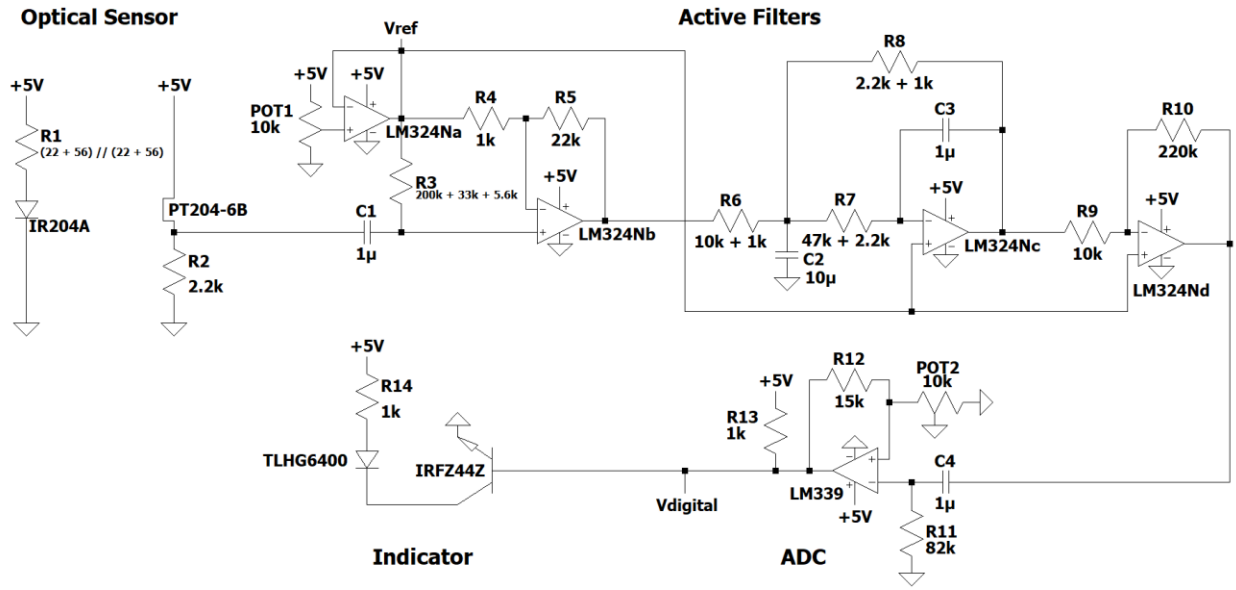

Figure 7: Full circuit schematic (correct individual filters).

After constructing the circuit designed in the previous section (see figure 7), various measurements were taken to assess the overall functionality of the system as well as the accuracy of the individual subsystems.

The optical sensor was designed to produce an AC signal in the range of 10 mVpp to 100 mVpp with a DC offset between 2 V and 4 V when a finger was placed between the infrared emitter and the phototransistor. To confirm this, the oscilloscope tool of the AD2 was used to capture the initial heartbeat waveform (v_{PT} from figure 1).

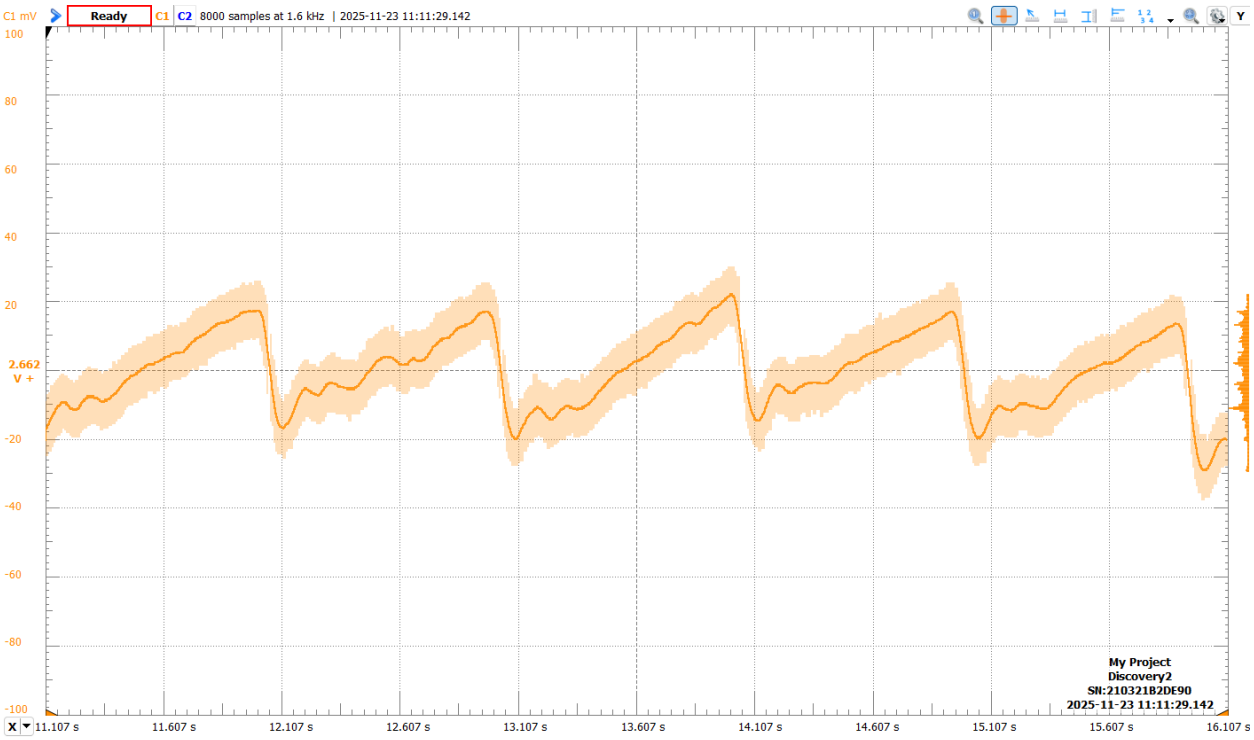

Figure 8: Oscilloscope measurement of the initial heart rate signal.

Looking at figure 8, it can be seen that the produced signal has a DC offset of about 2.662 V and a peak-to-peak voltage of roughly 40 mV. Both of these values fall within their respective valid ranges. It should be noted, however, that there is a small variance in the signal amplitude from period to period as a result of unsteadiness in the finger being tested and the natural instability of the setup. Despite this, the amplitude never drifts outside of the valid range so the optical sensor can safely be considered as fully functional.

The next subsystem tested was the high pass filter. The network tool of the AD2 was used to measure filter's frequency response from 100 mHz to 5 Hz. For reference, the points used as the input and output were v_{PT} and v_{HP} from figure 2 respectively.

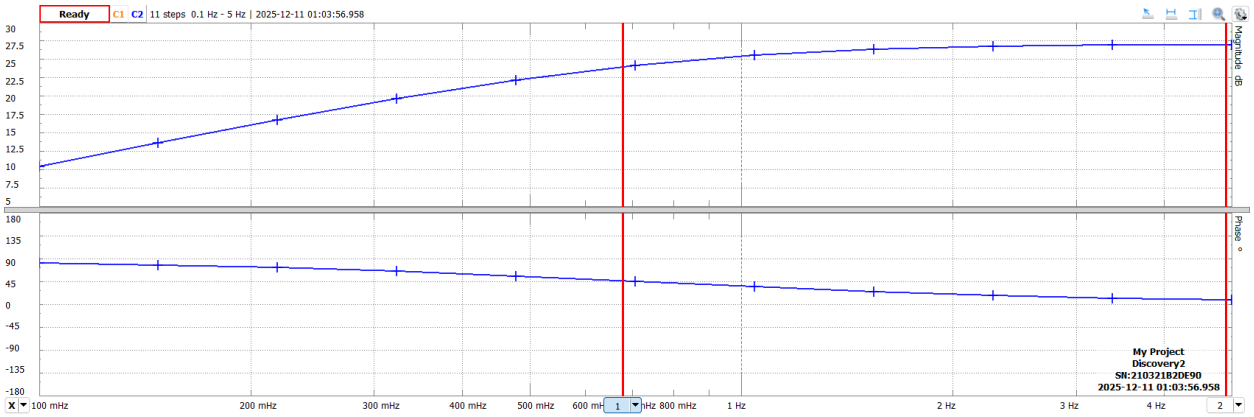

Figure 9: The magnitude and phase frequency responses of the designed high pass filter.

Using the bode plot shown in figure 9, a table was constructed to collect measurements and calculate errors.

Table 1: Results of the high pass filter.

	Measured Value	Converted Value	Desired Value	% Error
f_C	679.5 mHz	40.77 BPM	40 BPM	1.925 %
Gain	26.99 dB	22.36 V/V	23 V/V	2.783 %

Looking at table 1, it can clearly be seen that the filter functions as expected with very small errors for the gain and cutoff frequency.

Following this, the low-pass filter was tested in a similar manner to the high pass filter but from 500 mHz to 20 Hz. For reference, the points used as the input and output of the low pass filter were v_{HP} and v_{LP} from figure 3 respectively.

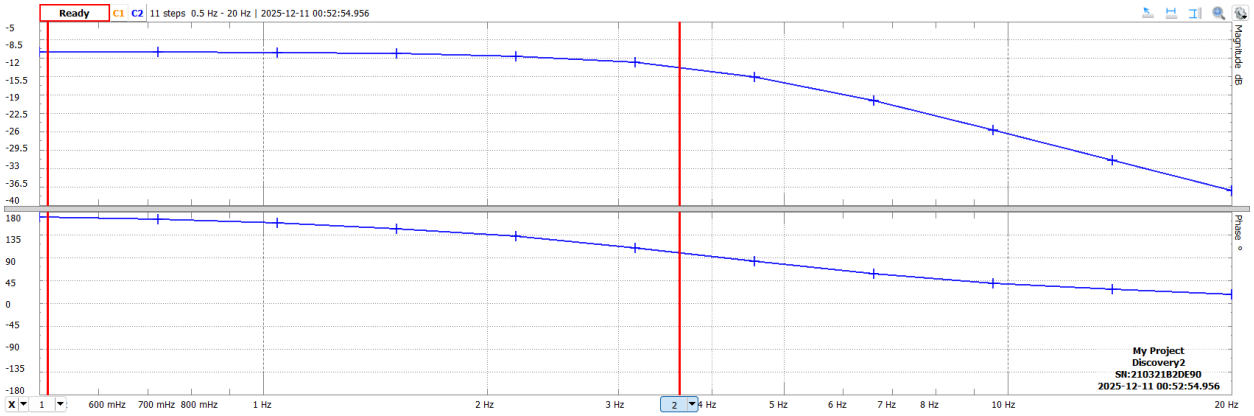

Figure 10: The magnitude and phase frequency responses of the low-pass filter.

Using the bode plot shown in figure 10, a table was constructed to collect measurements and calculate errors.

Table 2: Results of the low-pass filter.

	Measured Value	Converted Value	Desired Value	% Error
f_C	3.621 Hz	217.26 BPM	200 BPM	8.63 %

As shown in table 2, the low pass filter functioned as expected with a small amount of error resulting from the limited resistor and capacitor values in the lab kits. Unlike the high pass filter, there was no specific designed gain, but it was measured at -10.824 dB or 0.29 V/V.

Using this value along with the gain measured for the high pass filter, the resistor values for the inverting amplifier were chosen for the entire gain to be greater than 100 as follows:

$$100 \geq 22.36 \times 0.29 \times k \rightarrow k \geq 15.42$$

For simplicity, 220 kOhm and 10 kOhm resistors were selected, ensuring the gain was greater than 15.42. To further show the full functionality of the entire cascade a frequency response from 200 mHz to 20 Hz of all stages was captured.

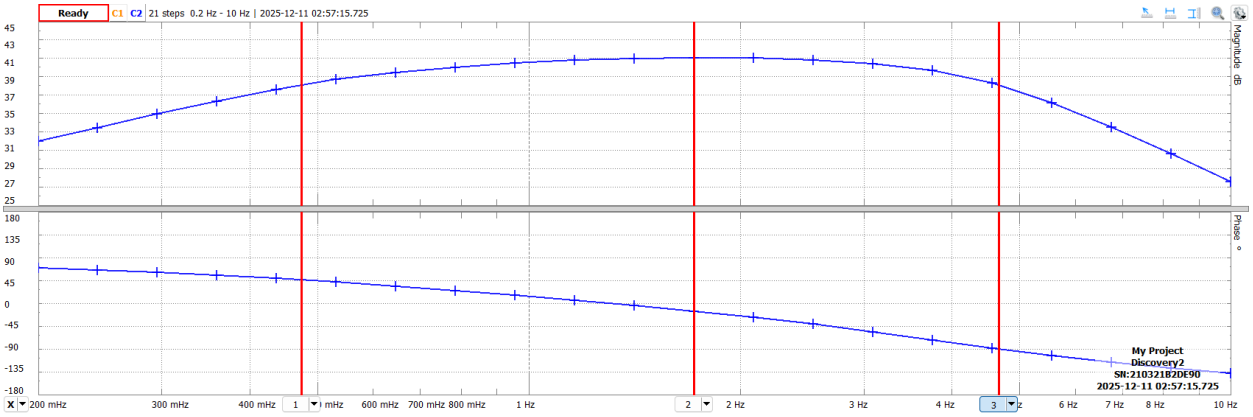

Figure 11: The magnitude and phase plot of entire active filter cascade.

Using data collected from figure 11, a table was constructed to show the cutoff frequencies and total system gain.

Table 3: Results of the entire filter cascade.

	Measured Value	**Converted Value**	**Desired Value**	**% Error**
Low f_C	475 mHz	28.5 BPM	40 BPM	28.75 %
High f_C	4.683 Hz	281 BPM	200 BPM	40.5 %

From table 3, it can be seen that despite the filters working individually, when cascaded together the cutoff frequencies shift dramatically. Despite this, the total gain is measured at over 40 dB (100 V/V) so the gain can be considered still within design specifications.

To continue testing the functionality of the circuit, an oscilloscope measurement of the input and digital output of the ADC was made to assess the conversion from analog to digital and the operating functionality of the circuit.

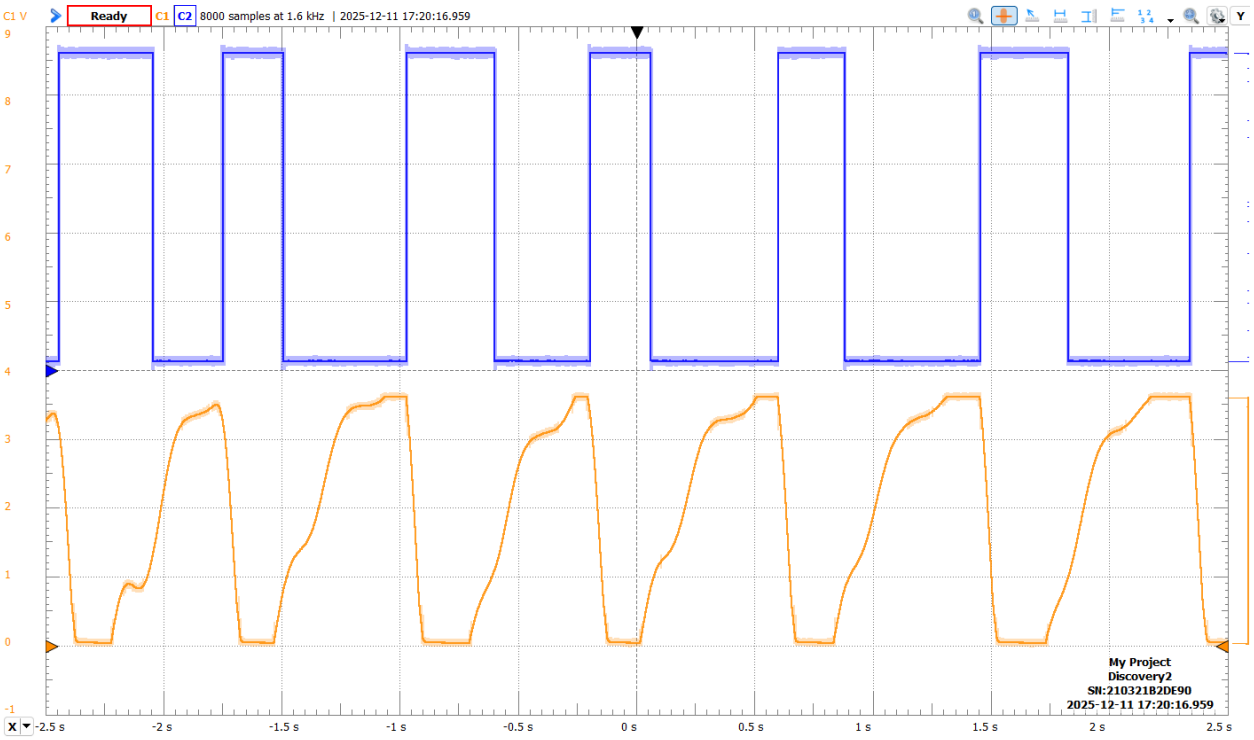

Figure 12: Oscilloscope reading of ADC analog input (orange) and digital output (blue).

From figure 12, it can be seen that the ADC functions as expected when it comes to converting the analog heart rate to a digital pulsing signal. This was further confirmed in lab by the indicator LED flashing in sync with the true heart rate as measured by a finger on the jugular vein. It was measured that the heart rate was 1.25 Hz or 75 BPM, a valid value for a resting human. Additionally, the peak-to-peak amplitude of the output was captured at 4.4804 V (a 10.39 % error from 5 V).

Due to the clear lack of function from the filter cascade operating as a band pass, the circuit was experimentally modified until the band pass response was more accurate.

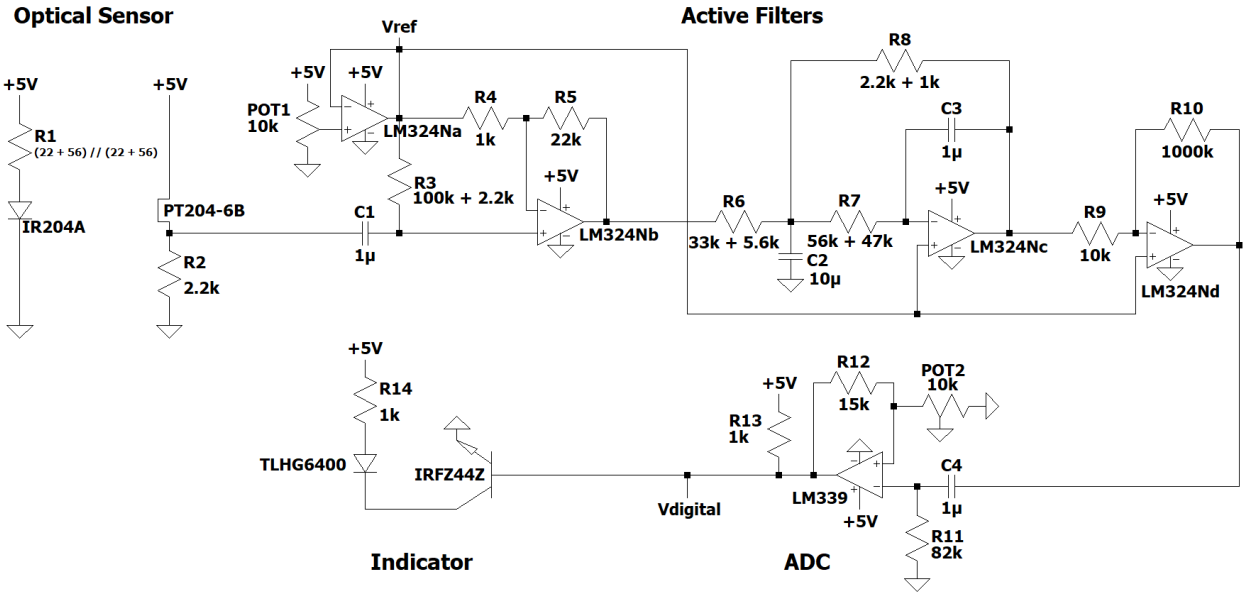

Figure 13: Full circuit schematic (correct band pass behavior).

Using the circuit from figure 13 and the AD2 network tool, the band pass response was recaptured.

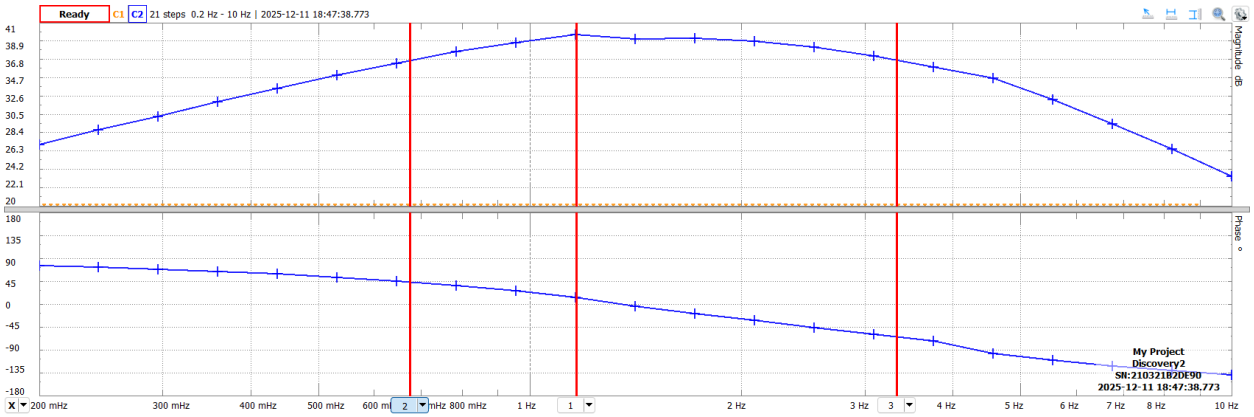

Figure 14: The corrected circuit band pass response.

From figure 14, the cutoff frequency measurements were compiled into a table to show the improvement of the cutoff frequencies.

Table 4: Results of the corrected filter cascade.

	Measured Value	Converted Value	Desired Value	% Error
Low f_C	674.3 mHz	40.46 BPM	40 BPM	1.145 %
High f_C	3.339 Hz	200.34 BPM	200 BPM	0.17 %

As seen in table 4, the corrected circuit was far more accurate in terms of cutoff frequencies. This came at the cost of gain, however, with a peak gain of 39.63 dB (just shy of the necessary 40 dB). Given more time for experimentation, a set of values that achieve all specifications is more than likely.

To further prove the accuracy of this new circuit, the input and output of the ADC was recaptured using the AD2's oscilloscope tool.

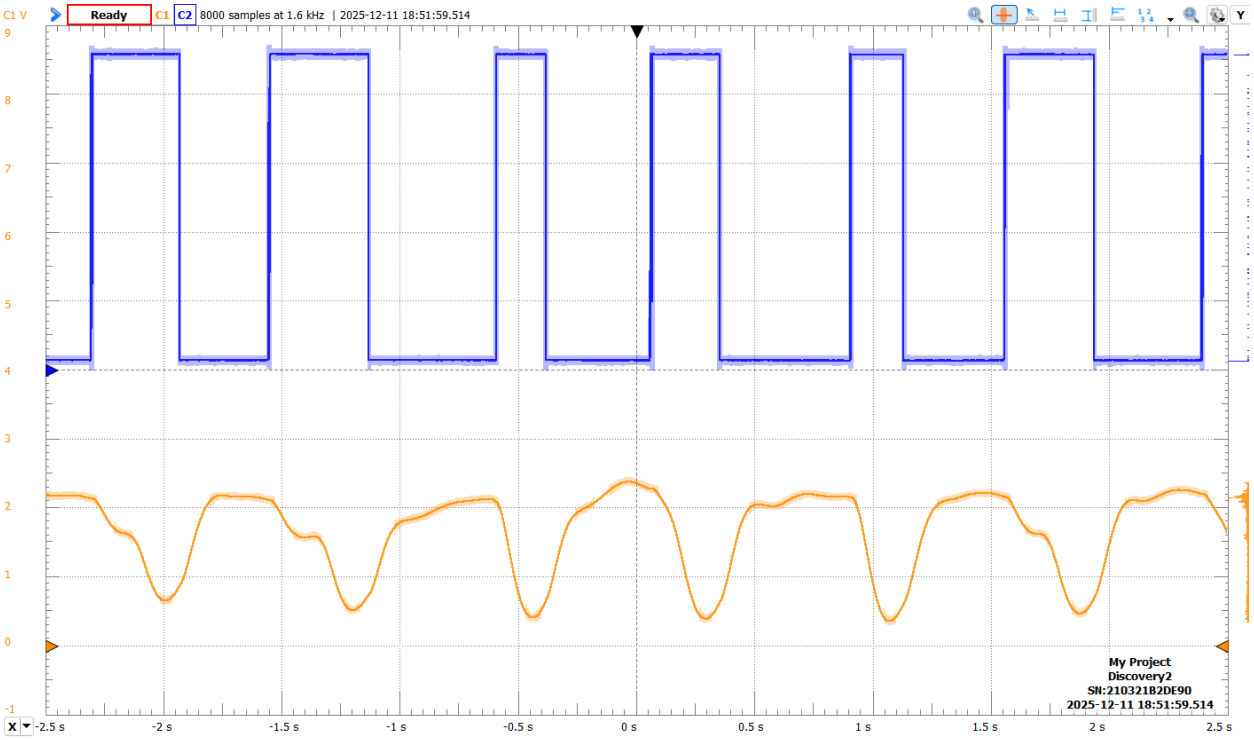

Figure 15: Oscilloscope reading of ADC corrected input (orange) and digital output (blue).

From the oscilloscope reading, it was found that the heart rate was 1.7 Hz or 102 BPM, likely a result of caffeine ingestion while constructing the corrected circuit. Additionally, the peak-to-peak amplitude was measured at 4.447 V (an 11.06% error from 5 V), a value very similar to the previous circuit. From these results it can be determined that at regular human heart rates, the use of the first or second circuit tested has little to no effect on the digital signal output. At the extremes however, the improper cutoff behavior of the first circuit could cause complications in heart rate detection.

Conclusion

Over the course of this project, a single supply optical heart rate sensor was successfully constructed and tested using an optical sensing system, an active filter cascade, and a comparator-based ADC with LED indication. The optical sensor produced a valid heartbeat waveform (2.662 V DC offset and roughly 40 mV peak-to-peak AC ripplet), and the

individual high pass and low-pass filters behaved as expected. The high pass cutoff was measured at 40.77 BPM (1.93% error) and the low-pass cutoff was measured at 217.26 BPM (8.63% error). The ADC subsystem also functioned properly, producing a clear digital pulsing signal and LED flashing in sync with the tested individuals heart rate, with an output peak-to-peak amplitude of about 4.48 V (10.39% error from 5 V).

During testing, it was found that the designed filter cascade when measured as a whole exhibited significant cutoff shifts (28.5 BPM - 281 BPM). This could cause detection issues at more extreme heart rates, so a second circuit was constructed and tested. The second circuit was experimentally designed to achieve a more accurate overall band pass response of 40.46 BPM to 200.34 BPM (1.15% and 0.17% error respectively), although the peak gain was slightly lower at 39.63 dB. The most likely causes of the cutoff shifting and remaining gain error are loading and interaction between filter stages, component tolerances, and nonideal op amp behavior in single-supply operation. Given more time for iteration, selecting more precise RC values and rebalancing gain across stages would likely allow the design to meet both the cutoff and gain specifications.