Listagem e Formato das instruções a serem suportadas pelo Simulador MIPS

:: Instruções do Tipo R

	<u>31</u>	<u> </u>	25	20	15	10	5 0
	R [6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
		Opcode	Source register 1	Source register 2	Destination register	Shift amount	Opcode extension
			register i	register 2	register	amount	extension
add \$1, \$2, \$3			mflo \$1				srl \$1, \$2, 10
. 44 40 40				40.40			44 42 42
sub \$1, \$2, \$3			addu \$1	., \$2, \$3			sra \$1, \$2, 10
slt \$1, \$2, \$3			subu \$1	, \$2, \$3			sllv \$1, \$2, \$3
. , . , .			•	, , , ,			
and \$1, \$2, \$3			mult \$1	, \$2			srlv \$1, \$2, \$3
or \$1, \$2, \$3			multu \$	1 \$2			srav \$1, \$2, \$3
01 71, 72, 73			παιτα γ	Ι, ΨΖ			31av 71, 72, 73
xor \$1, \$2, \$3			div \$1, \$	\$2			jr \$1
4. 40 40			4.	40			
nor \$1, \$2, \$3			divu \$1,	\$2			
mfhi \$1			sll \$1, \$	2. 10			
42			3 Y±, Y	_, _0			

:: Instruções do Tipo I



lui \$1, 100	xori \$1, \$2, 100	bne \$1, \$2, start
addi \$1, \$2, 100	lw \$1, 100(\$2)	addiu \$1, \$2, 100
slti \$1, \$2, 100	sw \$1, 100(\$2)	lb \$1, 100(\$2)
andi \$1, \$2, 100	bltz \$1, start	lbu \$1, 100(\$2)
ori \$1, \$2, 100	beq \$1, \$2, start	sb \$1, 100(\$2)

:: Instruções do Tipo J



j start

jal start

:: Instrução de chamada de sistema (apenas o opcode)

syscall