TEXAS INSTRUMENTS
BQ24091, BQ24092, BQ24093, BQ24095, BQ24090
SLUS968H – JANUARY 2010 – REVISED APRIL 2021

BQ2409x 1-A, Single-Input, Single-Cell Li-Ion and Li-Pol Battery Chargers

1 Features

- Charging
  - 1% charge voltage accuracy
  - 10% charge current accuracy
  - Pin selectable USB 100-mA and 500-mA maximum input current limit
  - Programmable termination and precharge threshold
- Protection
  - 6.6-V overvoltage protection
  - Input voltage dynamic power management
  - 125°C thermal regulation; 150°C thermal shutdown protection
  - OUT short-circuit protection and ISET short detection
  - Operation over JEITA range via battery NTC – ½ fast-charge-current at cold, 4.06 V at hot, BQ092/3
  - Fixed 10-hour safety timer
- System
  - Automatic Termination and Timer Disable Mode (TTDM) for absent battery pack with thermistor
  - Status indication – charging/done
  - Available in a small 10-pin MSOP package

2 Applications

- Smart phones
- PDAs
- MP3 players
- Low-power handheld devices

3 Description

The BQ2409x series of devices are highly integrated Li-ion and Li-Pol linear chargers devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

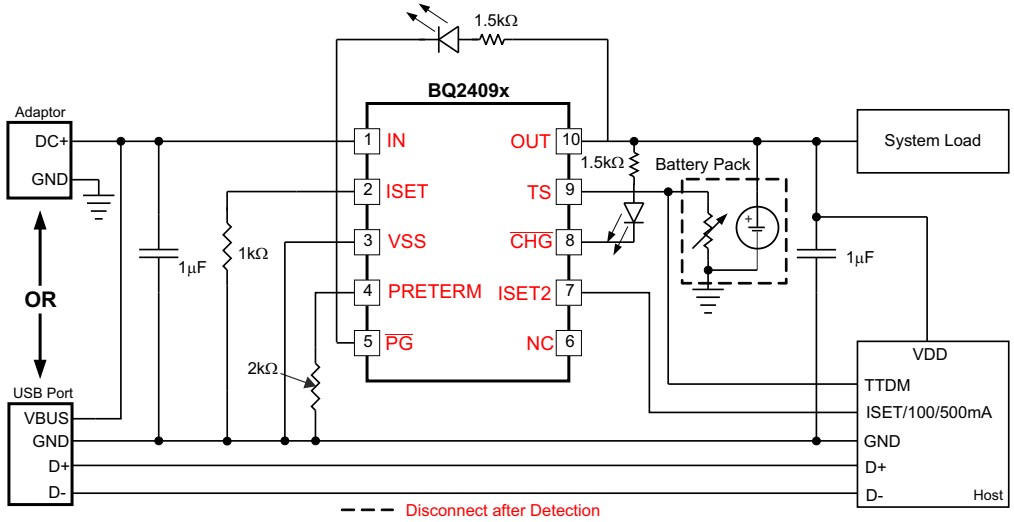
The BQ2409x has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10-hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ2409x	HVSSOP (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

Changes from Revision G (August 2015) to Revision H (April 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the package size From: 5 x 3 mm^2 To 3 x 3 mm^2 in the Section 6 table	5
• Changed $I_{BD-SINK}$ MIN value From: 7 mA to 6 mA in the Electrical Characteristics table	7
• Changed I_{IH} MAX value From: 8 µA to 9.5 µA in the Electrical Characteristics table	7

Changes from Revision F (December 2014) to Revision G (August 2015)	Page
• Changed BQ24095 $V_{O(REG)}$ value From: 4.20 V To: 4.35 V in the Section 6 table	5

Changes from Revision E (September 2013) to Revision F (December 2014)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision D (December 2012) to Revision E (September 2013)	Page
• Deleted the MARKING column from the ORDERING INFORMATION table, and added table note 1	4

Changes from Revision C (May 2012) to Revision D (December 2012)	Page
• Added bq24095 to the ORDERING INFORMATION table	4
• Changed BQ24090/2 to BQ24090/2/5 for TS pin description in Pin Functions table	5
• Changed the K_{ISET} entry in the Electrical Characteristics table	7
• Deleted Line Regulation typical characteristics graph	13
• Changed Current Regulation Overtemperature graph to Load Regulation - BQ24095 graph	13

Changes from Revision B (June 2010) to Revision C (May 2012)	Page
• Changed all instances of Li-ion To: Li-ion and Li-Pol	1

Changes from Revision A (February 2010) to Revision B (June 2010)	Page
• Changed the device number on the front page circuit From: BQ24090 To: BQ2409x	1

- Changed the ORDERING INFORMATION table Marking column From: Product Preview To: bq24092 and bq24093.....4

Changes from Revision * (January 2010) to Revision A (February 2010) **Page**

- Changed $V_{DO(IN-OUT)}$, MAX value From: 500 mV To: 520 mV in the Electrical Characteristics table 7
- Changed $I_{PRE-TERM}$ MAX value From: 79 µA to 81µA in the Electrical Characteristics table..... 7
- Changed $V_{CLAMP(TS)}$ MIN value From: 1900 mV to 1800 mV in the Electrical Characteristics table..... 7

5 Description (continued)

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The pre-charge current and termination current threshold are programmed via an external resistor. The fast charge current value is also programmable via an external resistor.

6 Device Options

PART NUMBER	$V_{O(REG)}$	V_{OVP}	JEITA	TS/CE	PG	PACKAGE
BQ24090	4.20 V	6.6 V	No	10 kΩ NTC	Yes	10 pin 3 x 3 mm^2
BQ24091	4.20 V	6.6 V	No	100 kΩ NTC	Yes	10 pin 3 x 3 mm^2
BQ24092	4.20 V	6.6 V	Yes	10 kΩ NTC	Yes	10 pin 3 x 3 mm^2
BQ24093	4.20 V	6.6 V	Yes	100 kΩ NTC	Yes	10 pin 3 x 3 mm^2
BQ24095	4.35 V	6.6 V	No	10 kΩ NTC	Yes	10 pin 3 x 3 mm^2

7 Pin Configuration and Functions

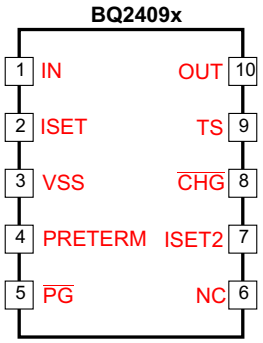


Figure 7-1. DGQ Package 10 Pins Top View

Table 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CHG	8	O	Low (FET on) indicates charging and Open Drain (FET off) indicates no charging or charge complete.
IN	1	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1 µF to 10 µF, connect from IN to V_{SS}.
ISET	2	I	Programs the fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 10.8 kΩ (50 mA) to 540 Ω (1000 mA).
ISET2	7	I	Programming the input/output current limit for the USB or adaptor source: high = 500 mA max, low = ISET, FLOAT = 100 mA max.
NC	6	NA	Do not make a connection to this pin (for internal use) – do not route through this pin.
OUT	10	O	Battery connection. System load may be connected. Average load should not be excessive, allowing battery to charge within the 10 hour safety timer window. Expected range of bypass capacitors 1 µF to 10 µF.
PG	5	O	Low (FET on) indicates the input voltage is above UVLO and the OUT (battery) voltage.
PRE-TERM	4	I	Programs the current termination threshold (5 to 50% of Iout which is set by ISET) and sets the pre-charge current to twice the termination current level. Expected range of programming resistor is 1 kΩ to 10 kΩ (2k: Ipgm/10 for term; Ipgm/5 for precharge).
TS	9	I	Temperature sense pin connected to BQ24090/2/5 -10k at 25°C NTC thermistor and BQ24091/3 -100 k at 25°C NTC thermistor, in the battery pack. Floating TS pin or pulling high puts part in TTDM Charger Mode and disable TS monitoring, timers and termination. Pulling pin low disables the IC. If NTC sensing is not needed, connect this pin to VSS through an external 10-kΩ/100-kΩ resistor. A 250 kΩ from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.
VSS	3	–	Ground terminal
Thermal Pad and Package	—	—	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage(2)	IN (with respect to VSS)	–0.3	12	V
	OUT (with respect to VSS)	–0.3	7	V
	PRE-TERM, ISET, ISET2, TS, $\overline{CHG}$, $\overline{PG}$, ASI, ASO (with respect to VSS)	–0.3	7	V
Input current	IN		1.25	A
Output current (continuous)	OUT		1.25	A
Output sink current	$\overline{CHG}$		15	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions(1)

		MIN	MAX	UNIT
V_{IN}	IN voltage range	3.5	12	V
	IN operating voltage range, Restricted by V_{DPM} and V_{OVP}	4.45	6.45	V
I_{IN}	Input current, IN pin		1.0	A
I_{OUT}	Current, OUT pin		1.0	A
T_J	Junction temperature	0	125	°C
$R_{PRE-TERM}$	Programs precharge and termination current thresholds	1	10	kΩ
R_{ISET}	Fast-charge current programming resistor	0.540	49.9	kΩ
R_{TS}	10-kΩ NTC thermistor range without entering $\overline{BAT\_EN}$ or TTDM	1.66	258	kΩ

(1) Operation with V_{IN} less than 4.5 V or in drop-out may result in reduced performance.

8.4 Thermal Information

THERMAL METRIC(1)		BQ2409x DGQ 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.2	
ψ_{JT}	Junction-to-top characterization parameter	3.5	
ψ_{JB}	Junction-to-board characterization parameter	44.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	19.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Dissipation Ratings(1) (2)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR $T_A > 25°C$
5 x 3 mm MSOP	52°C/W	48°C/W	1.92 W	19.2 mW/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2×3 via matrix

8.6 Electrical Characteristics

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out exit	V_{IN}: 0 V → 4 V update based on sim/char	3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 4 V→0 V, $V_{UVLO\_FALL} = V_{UVLO\_RISE} - V_{HYS-UVLO}$	175	227	280	mV
V_{IN-DT}	Input power good detection threshold is $V_{OUT} + V_{IN-DT}$	(Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$); V_{OUT} = 3.6 V, V_{IN}: 3.5 V → 4 V	30	80	145	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6 V, V_{IN}: 4 V → 3.5 V		31		mV
$t_{DGL(PG\_PWR)}$	Deglitch time on exiting sleep.	Time measured from V_{IN}: 0 V → 5 V 1-µs rise time to $\overline{PG}$ = low, V_{OUT} = 3.6 V		45		µs
$t_{DGL(PG\_NO-PWR)}$	Deglitch time on $V_{HYS-INDT}$ power down. Same as entering sleep.	Time measured from V_{IN}: 5 V → 3.2 V 1-µs fall time to $\overline{PG}$ = OC, V_{OUT} = 3.6 V		29		ms
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V → 7 V	6.5	6.65	6.8	V
$t_{DGL(OVP-SET)}$	Input overvoltage blanking time	V_{IN}: 5 V → 7 V		113		µs

8.6 Electrical Characteristics (continued)

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 7 V → 5 V		95		mV
$t_{DGL(OVP-REC)}$	Deglitch time exiting OVP	Time measured from V_{IN}: 7 V → 5 V 1-µs fall-time to $\overline{PG}$ = LO		30		µs
V_{IN-DPM}	USB/Adaptor low input voltage protection. Restricts Iout at V_{IN-DPM}	Feature active in USB Mode; Limit input source current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 825 Ω	4.34	4.4	4.46	V
		Feature active in Adaptor Mode; Limit input source current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 825 Ω	4.24	4.3	4.36	
$I_{IN-USB-CL}$	USB input I-Limit 100 mA	ISET2 = Float; R_{ISET} = 825 Ω	85	92	100	mA
	USB input I-Limit 500 mA	ISET2 = High; R_{ISET} = 825 Ω	430	462	500	
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest resistor value considered a fault (short). Monitored for Iout>90 mA	Riset: 600 Ω → 250 Ω, I_{OUT} latches off, cycle power to reset.	280		500	Ω
t_{DGL_SHORT}	Deglitch time transition from ISET short to Iout disable	Clear fault by cycling IN or TS/ $\overline{BAT\_EN}$		1		ms
I_{OUT_CL}	Maximum OUT current limit Regulation (Clamp)	V_{IN} = 5 V, V_{OUT} = 3.6 V, V_{ISET2} = Low, R_{ISET}: 600 Ω → 250 Ω, Iout latches off after $t_{DGL-SHORT}$	1.05		1.4	A
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT pin short-circuit detection threshold/ precharge threshold	V_{OUT}: 3 V → 0.5 V, no deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT pin short hysteresis	Recovery ≥ $V_{OUT(SC)}$ + $V_{OUT(SC-HYS)}$; rising, no deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT pin during short-circuit detection		10	15	20	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT pin	V_{IN} = 0 V			1	µA
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 6 V, V_{OUT} > $V_{OUT(REG)}$			6	
$I_{IN(STDBY)}$	Standby current into IN pin	TS = LO, V_{IN} ≤ 6 V			125	µA
I_{CC}	Active supply current, IN pin	TS = open, V_{IN} = 6 V, TTDM – no load on OUT pin, V_{OUT} > $V_{OUT(REG)}$, IC enabled		0.8	1.0	mA
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Battery regulation voltage (BQ24090/1/2/3)	V_{IN} = 5.5 V, I_{OUT} = 25 mA, ($V_{TS-45°C}$≤ V_{TS} ≤ $V_{TS-0°C}$)	4.16	4.2	4.23	V
	Battery regulation voltage (BQ24095)	V_{IN} = 5.5 V, I_{OUT} = 25 mA	4.30	4.35	4.40	
$V_{O\_HT(REG)}$	Battery hot regulation Voltage, BQ24092/3	V_{IN} = 5.5 V, I_{OUT} = 25 mA, $V_{TS-60°C}$≤ V_{TS} ≤ $V_{TS-45°C}$	4.02	4.06	4.1	V
$I_{OUT(RANGE)}$	Programmed Output fast charge current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V, ISET2=Lo, R_{ISET} = 540 to 10.8 kΩ	10		1000	mA
$V_{DO(IN-OUT)}$	Drop-Out, VIN – VOUT	Adjust VIN down until I_{OUT} = 0.5 A, V_{OUT} = 4.15 V, R_{ISET} = 540, ISET2 = Lo (Adaptor Mode); T_J ≤ 100°C		325	520	mV
I_{OUT}	Output fast charge formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V, ISET2 = Lo		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor for BQ24090, 91, 92, 93	R_{ISET} = K_{ISET} /I_{OUT}; 50 < I_{OUT} < 1000 mA	510	540	565	AΩ
		R_{ISET} = K_{ISET} /I_{OUT}; 25 < I_{OUT} < 50 mA	480	527	580	
		R_{ISET} = K_{ISET} /I_{OUT}; 10 < I_{OUT} < 25 mA	350	520	680	
K_{ISET}	Fast charge current factor for BQ24095	R_{ISET} = K_{ISET} /I_{OUT}; 50 < I_{OUT} < 1000 mA	510	560	585	AΩ
		R_{ISET} = K_{ISET} /I_{OUT}; 25 < I_{OUT} < 50 mA	480	557	596	
		R_{ISET} = K_{ISET} /I_{OUT}; 10 < I_{OUT} < 25 mA	350	555	680	
PRECHARGE – SET BY PRETERM PIN						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			70		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
$I_{PRE-TERM}$	Refer to the Termination Section					

8.6 Electrical Characteristics (continued)

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\%I_{PRECHG}$	Pre-charge current, default setting	V_{OUT} < V_{LOWV}; R_{ISET} = 1080 Ω; **$R_{PRE-TERM}$= High Z**	18	20	22	$\%I_{OUT-CC}$
	Pre-charge current formula	$R_{PRE-TERM}$ = $K_{PRE-CHG}$ (Ω/%) × $\%_{PRE-CHG}$ (%)		$R_{PRE-TERM}/K_{PRE-CHG\%}$		
$K_{PRE-CHG}$	% Pre-charge Factor	V_{OUT} < V_{LOWV}, V_{IN} = 5 V, $R_{PRE-TERM}$ = 2 k to 10 kΩ; R_{ISET} = 1080 Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 20 to 100%	90	100	110	Ω/%
		V_{OUT} < V_{LOWV}, V_{IN} = 5 V, $R_{PRE-TERM}$ = 1 k to 2 kΩ; R_{ISET} = 1080 Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10% to 20%	84	100	117	Ω/%
TERMINATION – SET BY PRE-TERM PIN						
$\%_{TERM}$	Termination threshold current, default setting	V_{OUT} > V_{RCH}; R_{ISET} = 1 k; **$R_{PRE-TERM}$ = High Z**	9	10	11	$\%I_{OUT-CC}$
	Termination current threshold Formula	$R_{PRE-TERM}$ = K_{TERM} (Ω/%) × %TERM (%)		$R_{PRE-TERM}/ K_{TERM}$		
K_{TERM}	% Term factor	V_{OUT} > V_{RCH}, V_{IN} = 5 V, $R_{PRE-TERM}$ = 2 k to 10 kΩ; R_{ISET} = 750 Ω K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10 to 50%	182	200	216	Ω/%
		V_{OUT} > V_{RCH}, V_{IN} = 5 V, $R_{PRE-TERM}$ = 1 k to 2 kΩ; R_{ISET} = 750 Ω K_{TERM} × %Iset, where %Iset is 5 to 10%	174	199	224	
$I_{PRE-TERM}$	Current for programming the term. and pre-chg with resistor. $I_{Term-Start}$ is the initial PRE-TERM current.	$R_{PRE-TERM}$ = 2 k, V_{OUT} = 4.15 V	71	75	81	µA
%TERM	Termination current formula			$R_{TERM}/ K_{TERM}\%$		
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms
$I_{Term-Start}$	Elevated PRE-TERM current for, $t_{Term-Start}$, during start of charge to prevent recharge of full battery		80	85	92	µA
$t_{Term-Start}$	Elevated termination threshold initially active for $t_{Term-Start}$			1.25		min
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold – normal temp	V_{IN} = 5V, V_{TS} = 0.5 V, V_{OUT}: 4.25 V → V_{RCH}	$V_{O(REG)}$-0.120	$V_{O(REG)}$-0.095	$V_{O(REG)}$-0.070	V
	Recharge detection threshold – hot temp	V_{IN} = 5 V, V_{TS} = 0.2V, V_{OUT}: 4.15 V → V_{RCH}	$V_{O(REG)}$-0.130	$V_{O(REG)}$-0.105	$V_{O(REG)}$-0.080	V
$t_{DGL1(RCH)}$	Deglitch time, recharge threshold detected	V_{IN} = 5 V, V_{TS} = 0.5 V, V_{OUT}: 4.25 V → 3.5 V in 1µs; $t_{DGL(RCH)}$ is time to ISET ramp		29		ms
$t_{DGL2(RCH)}$	Deglitch time, recharge threshold detected in OUT-Detect Mode	V_{IN} = 5 V, V_{TS} = 0.5V, V_{OUT} = 3.5 V inserted; $t_{DGL(RCH)}$ is time to ISET ramp		3.6		ms
BATTERY DETECT ROUTINE						
V_{REG-BD}	VOUT reduced regulation during battery detect	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	$V_{O(REG)}$-0.450	$V_{O(REG)}$-0.400	$V_{O(REG)}$-350	V
$I_{BD-SINK}$	Sink current during V_{REG-BD}		6		10	mA
$t_{DGL(HI/LOW REG)}$	Regulation time at V_{REG} or V_{REG-BD}			25		ms
V_{BD-HI}	High battery detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	$V_{O(REG)}$ -0.150	$V_{O(REG)}$-0.100	$V_{O(REG)}$-0.050	V
V_{BD-LO}	Low battery detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	V_{REG-BD} +0.50	V_{REG-BD} +0.1	V_{REG-BD} +0.15	V
BATTERY CHARGING TIMERS AND FAULT TIMERS						
t_{PRECHG}	Pre-charge safety timer value	Restarts when entering pre-charge; always enabled when in pre-charge	1700	1940	2250	s
t_{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, TS/ $\overline{BAT\_EN}$ disable, OUT short, exiting LOWV and refresh	34000	38800	45000	s
BATTERY-PACK NTC MONITOR (Note 1); TS pin: 10 k and 100 k NTC						
$I_{NTC-10k}$	NTC bias current, BQ24090/2/5	V_{TS} = 0.3 V	48	50	52	µA
$I_{NTC-100k}$	NTC bias current, BQ24091/3	V_{TS} = 0.3 V	4.8	5.0	5.2	µA

8.6 Electrical Characteristics (continued)

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{NTC-DIS-10k}$	10k NTC bias current when Charging is disabled, BQ24090/2/5	V_{TS} = 0 V	27	30	34	µA
$I_{NTC-DIS-100k}$	100k NTC bias current when Charging is disabled, BQ24091/3	V_{TS} = 0 V	4.4	5.0	5.8	µA
$I_{NTC-FLDBK-10k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM, BQ24090/2/5	V_{TS}: Set to 1.525 V	4	5	6.5	µA
$I_{NTC-FLDBK-100k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM, BQ24091/3	V_{TS}: Set to 1.525 V	1.1	1.5	1.9	µA
$V_{TTDM(TS)}$	Termination and Timer Disable Mode Threshold – enter	V_{TS}: 0.5 V → 1.7 V; timer held in Reset	1550	1600	1650	mV
$V_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7 V → 0.5 V; timer enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS} = Open (float)	1800	1950	2000	mV
$t_{DGL(TTDM)}$	Deglitch exit TTDM between states			57		ms
	Deglitch enter TTDM between states			8		µs
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6 µS) takes place near this spec threshold. V_{TS}: 1.425 V → 1.525 V		1475		mV
C_{TS}	Optional capacitance – ESD			0.22		µF
$V_{TS-0°C}$	Low temperature CHG pending	Low temp charging to pending; V_{TS}: 1.0 V → 1.5 V	1205	1230	1255	mV
$V_{HYS-0°C}$	Hysteresis at 0°C	Charge pending to low temp charging; V_{TS}: 1.5 V → 1 V		86		mV
$V_{TS-10°C}$	Low temperature, half charge, BQ24092/3	Normal charging to low temp charging; V_{TS}: 0.5 V → 1 V	765	790	815	mV
$V_{HYS-10°C}$	Hysteresis at 10°C, BQ24092/3	Low temp charging to normal CHG; V_{TS}: 1.0 V → 0.5 V		35		mV
$V_{TS-45°C}$	High temperature at 4.1V	Normal charging to high temp CHG; V_{TS}: 0.5 V → 0.2 V	263	278	293	mV
$V_{HYS-45°C}$	Hysteresis at 45°C	High temp charging to normal CHG; V_{TS}: 0.2 V → 0.5 V		10.7		mV
$V_{TS-60°C}$	High temperature disable, BQ24092/3	High temp charge to pending; V_{TS}: 0.2 V → 0.1 V	170	178	186	mV
$V_{HYS-60°C}$	Hysteresis at 60°C, BQ24092/3	Charge pending to high temp CHG; V_{TS}: 0.1 V → 0.2 V		11.5		mV
$t_{DGL(TS\_10C)}$	Deglitch for TS thresholds: 10C, BQ24092/3	Normal to cold operation; V_{TS}: 0.6 V → 1 V		50		ms
		Cold to normal operation; V_{TS}: 1 V → 0.6 V		12		
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45/60C.	Battery charging		30		ms
$V_{TS-EN-10k}$	Charge Enable Threshold, (10k NTC)	V_{TS}: 0 V → 0.175 V	80	88	96	mV
$V_{TS-DIS\_HYS-10k}$	HYS below $V_{TS-EN-10k}$ to Disable, (10k NTC)	V_{TS}: 0.125 V → 0 V		12		mV
$V_{TS-EN-100k}$	Charge Enable Threshold, BQ24090/2	V_{TS}: 0 V → 0.175 V	140	150	160	mV
$V_{TS-DIS\_HYS-100k}$	HYS below $V_{TS-EN-100k}$ to Disable, BQ24091/3	V_{TS}: 0.125 V → 0 V		50		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON ISET2						
V_{IL}	Logic LOW input voltage	Sink 8 µA			0.4	V
V_{IH}	Logic HIGH input voltage	Source 8 µA	1.4			V
I_{IL}	Sink current required for LO	V_{ISET2}= 0.4 V	2		9	µA
I_{IH}	Source current required for HI	V_{ISET2}= 1.4 V	1.1		9.5	µA
V_{FLT}	ISET2 Float voltage		575	900	1225	mV

8.6 Electrical Characteristics (continued)

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC LEVELS ON $\overline{CHG}$ AND $\overline{PG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	$V_{\overline{CHG}}$ = 5 V, $V_{\overline{PG}}$ = 5 V			1	µA

8.7 Typical Characteristics

SETUP: BQ2409x typical applications schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise indicated)

8.7.1 Power Up, Power Down, OVP, Disable and Enable Waveforms

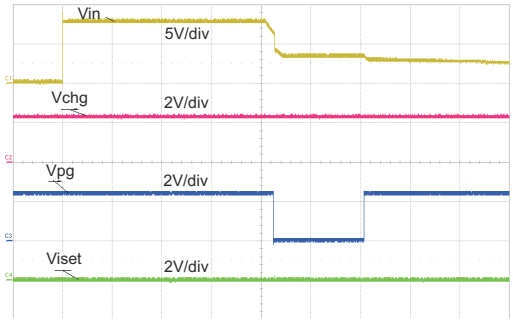


Figure 8-1. OVP 8-V Adaptor - Hot Plug

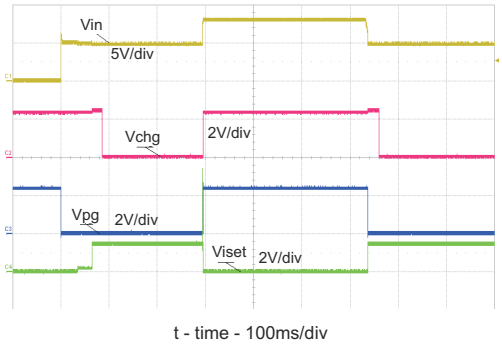
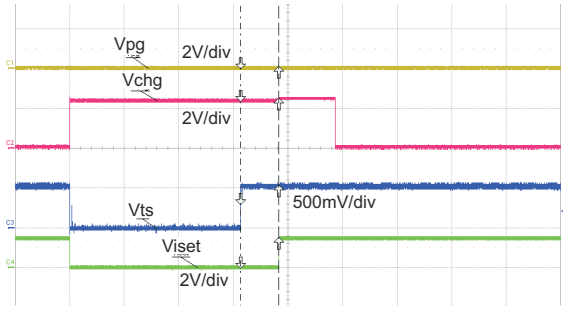


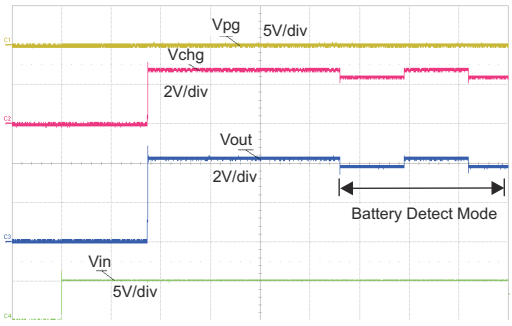
Figure 8-2. OVP from Normal Power-Up Operation – V_{IN} 0 V → 5 V → 6.8 V → 5 V



10-kΩ resistor from TS to GND.

10-kΩ is shorted to disable the IC.

Figure 8-3. TS Enable and Disable



Fixed 10-kΩ resistor, between TS and GND.

Figure 8-4. Hot Plug Source with No Battery – Battery Detection

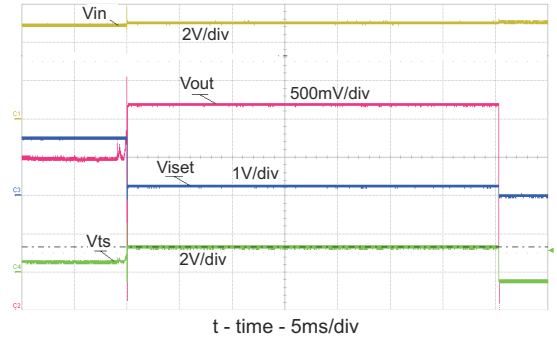


Figure 8-5. Battery Removal – GND Removed 1st, 42-Ω Load

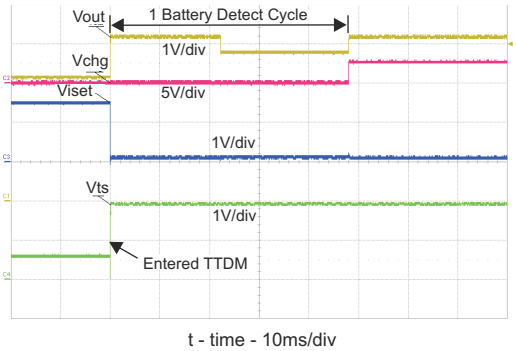
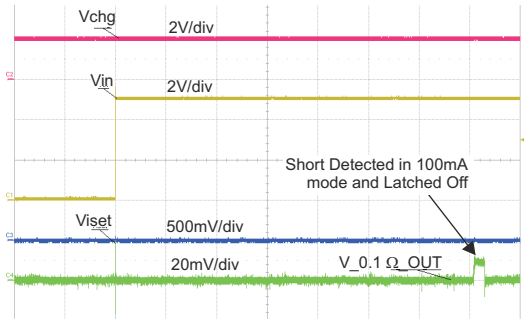


Figure 8-6. Battery Removal with OUT and TS Disconnect 1st, with 100-Ω Load

8.7.2 Protection Circuits Waveforms



CH4: Iout (0.2 A/Div)

Figure 8-7. ISET Shorted Prior to USB Power Up

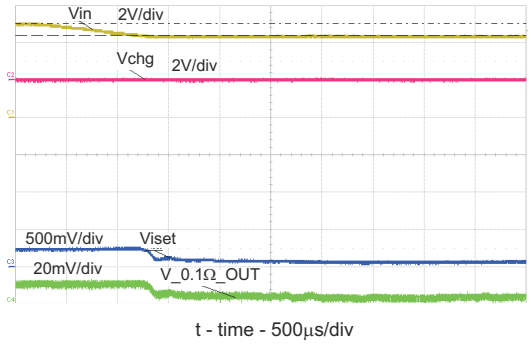
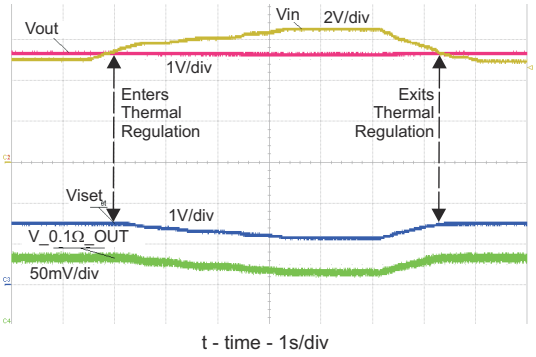
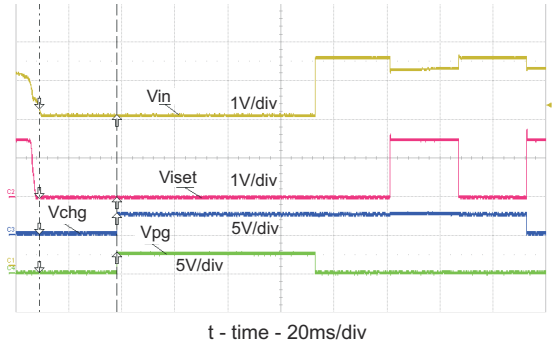


Figure 8-8. DPM – USB Current Limits – Vin Regulated to 4.4 V



The IC temperature rises to 125°C and enters thermal regulation. Charge current is reduced to regulate the IC at 125°C. VIN is reduced, the IC temperature drops, the charge current returns to the programmed value.

Figure 8-9. Thermal Regulation – Vin increases PWR/Iout Reduced



V_{IN} swept from 5 V to 3.9 V to 5 V

V_{BAT} = 4 V

Figure 8-10. Entering and Exiting Sleep Mode

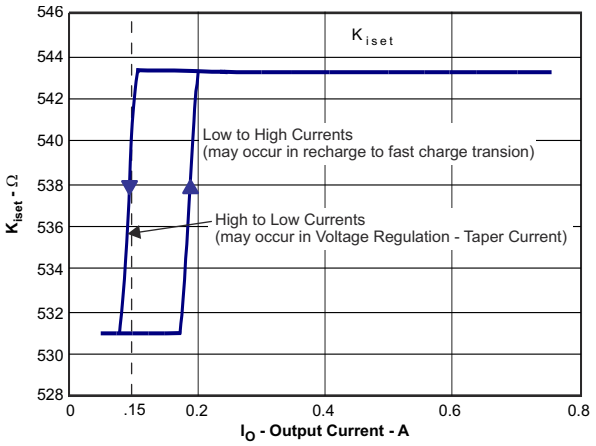


Figure 8-11. K_{ISET} for Low and High Currents

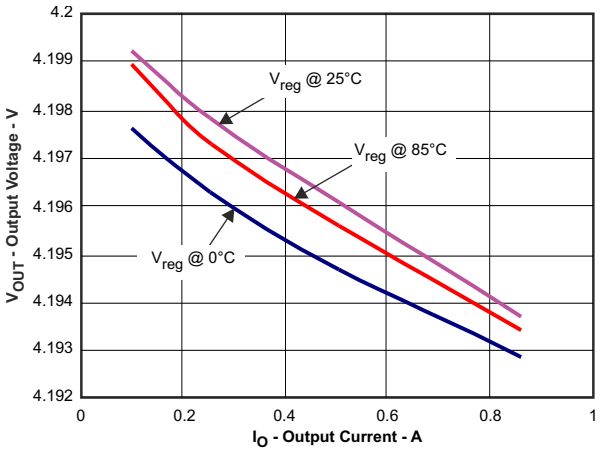


Figure 8-12. Load Regulation Overtemperature

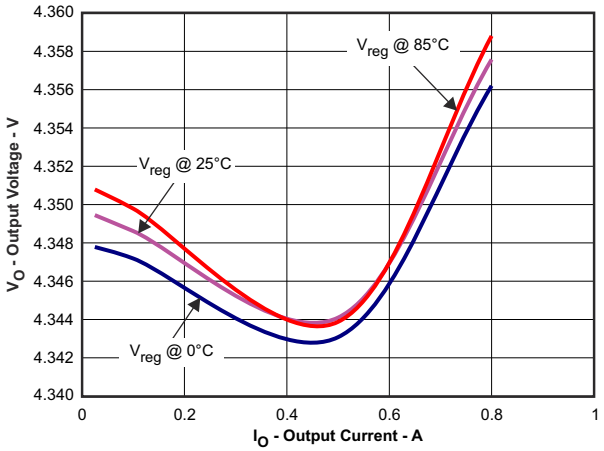


Figure 8-13. Load Regulation – BQ24095

9 Detailed Description

9.1 Overview

The BQ2409x is a highly-integrated family of single cell Li-ion and Li-pol chargers. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: Precharge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current and Precharge/Termination Current. This charger is designed to work with a USB connection or Adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: JEITA temperature standard, overvoltage protection, DPM-IN, safety timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-ion or Li-pol battery pack. Upon application of a 5-V DC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of precharge current can be programmed using the PRE-TERM pin which programs a percent of fast charge current (10 to 100%) as the precharge current. This feature is useful when the system load is connected across the battery *stealing* the battery current. The precharge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. The PRE-TERM pin is a dual function pin which sets the precharge current level and the termination threshold level. The termination "current threshold" is always half of the precharge programmed current level.

Once the battery voltage has charged to the V_{LOWV} threshold, fast charge is initiated and the fast-charge current is applied. The fast-charge constant current is programmed using the ISET pin. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C the IC enters thermal regulation, slows the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. Figure 9-1 shows the charging profile with thermal regulation. Typically under normal operating conditions, the junction temperature of the IC is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination can be disabled if desired. The $\overline{CHG}$ pin is low (LED on) during the first charge cycle only and turns off once the termination threshold is reached, regardless if termination, for charge current, is enabled or disabled.

Further details are mentioned in .Section 9.3.

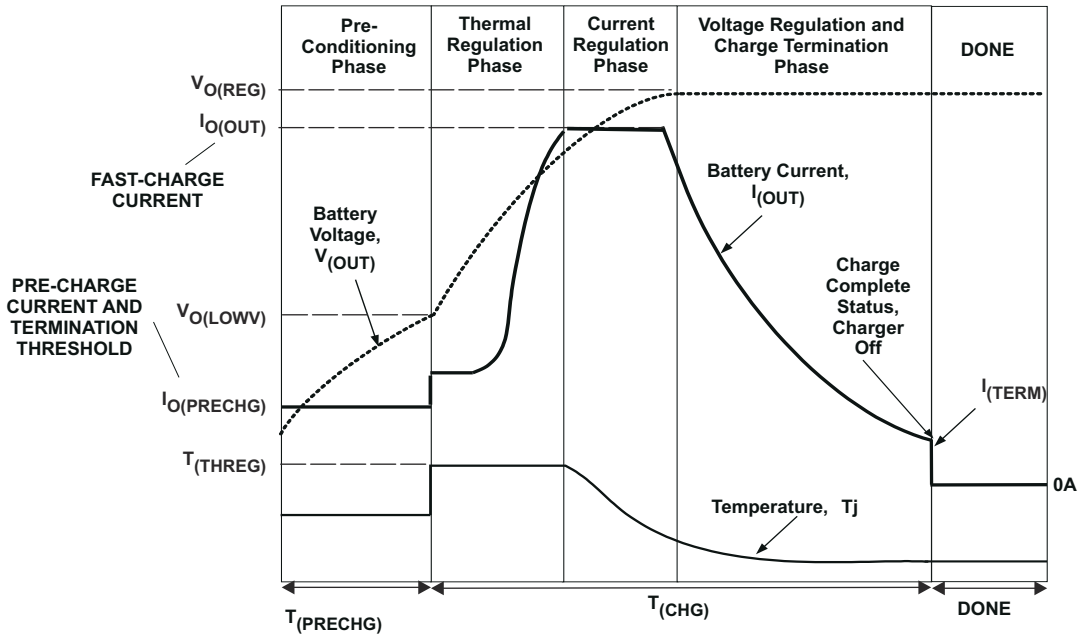
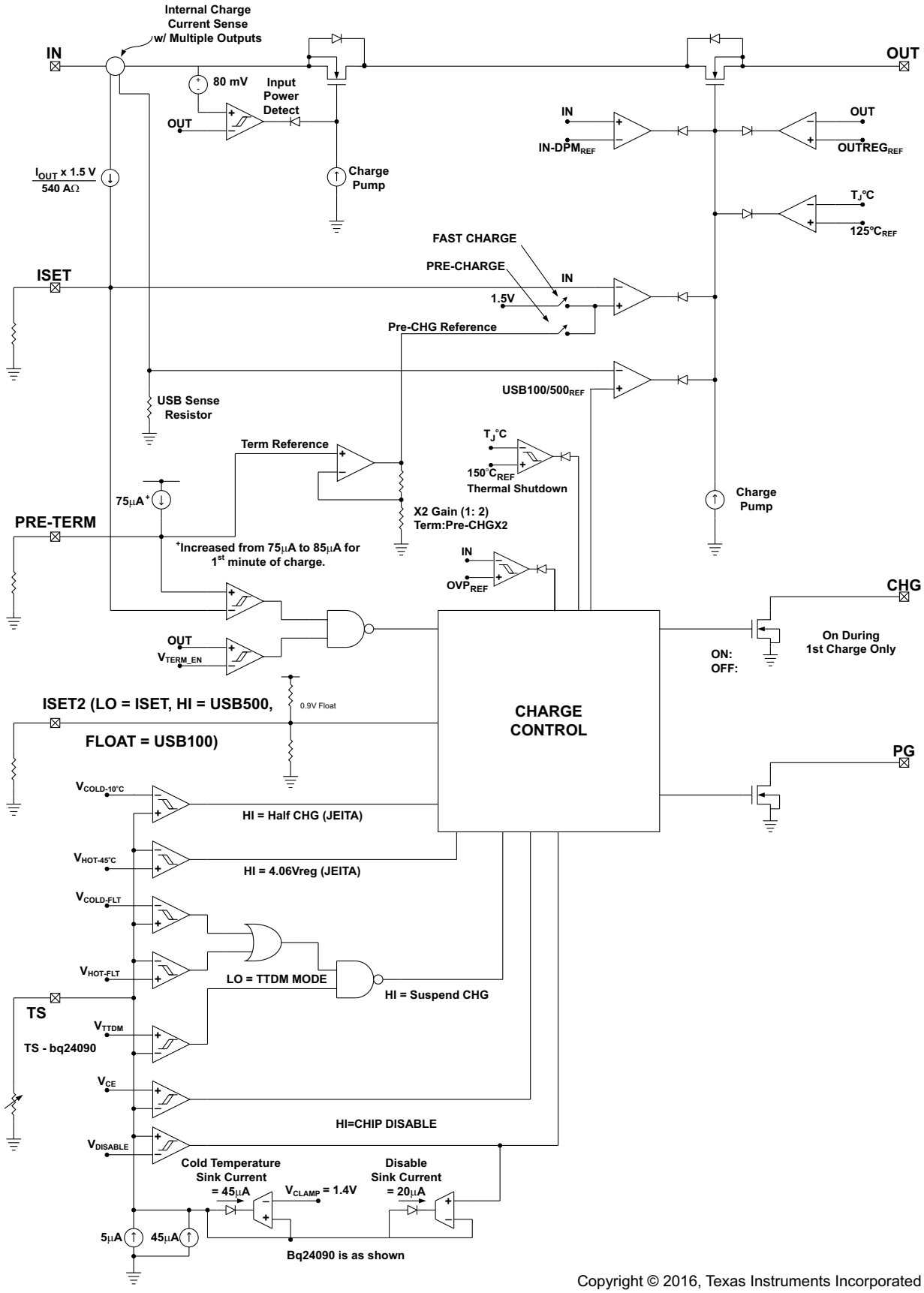


Figure 9-1. Charging Profile with Thermal Regulation

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power Down or Undervoltage Lockout (UVLO)

The BQ2409x family is in power-down mode if the IN pin voltage is less than UVLO. The part is considered *dead* and all the pins are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active Mode depending on the OUT pin (battery) voltage.

9.3.2 UVLO

The BQ2409x family is in power-down mode if the IN pin voltage is less than V_{UVLO}. The part is considered *dead* and all the pins are high impedance.

9.3.3 Power Up

The IC is alive after the IN voltage ramps above UVLO (see Sleep Mode), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100 mA, sets the input current limit threshold base on the ISET2 pin, starts the safety timer, and enables the $\overline{CHG}$ pin. See Figure 9-2.

9.3.4 Sleep Mode

If the IN pin voltage is between than V_{OUT} + V_{DT} and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{PG}$ and $\overline{CHG}$ pins are high impedance. As the input voltage rises and the charger exits Sleep Mode, the $\overline{PG}$ pin goes low, the safety timer continues to count, charge is enabled, and the $\overline{CHG}$ pin returns to its previous state. See Figure 9-3.

9.3.5 New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS pin), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the V_{RCH} threshold. The $\overline{CHG}$ pin is active low only during the first charge cycle, therefore exiting TTDM or a dropping below V_{RCH} will not turn on the $\overline{CHG}$ pin FET, if the $\overline{CHG}$ pin is already high impedance.

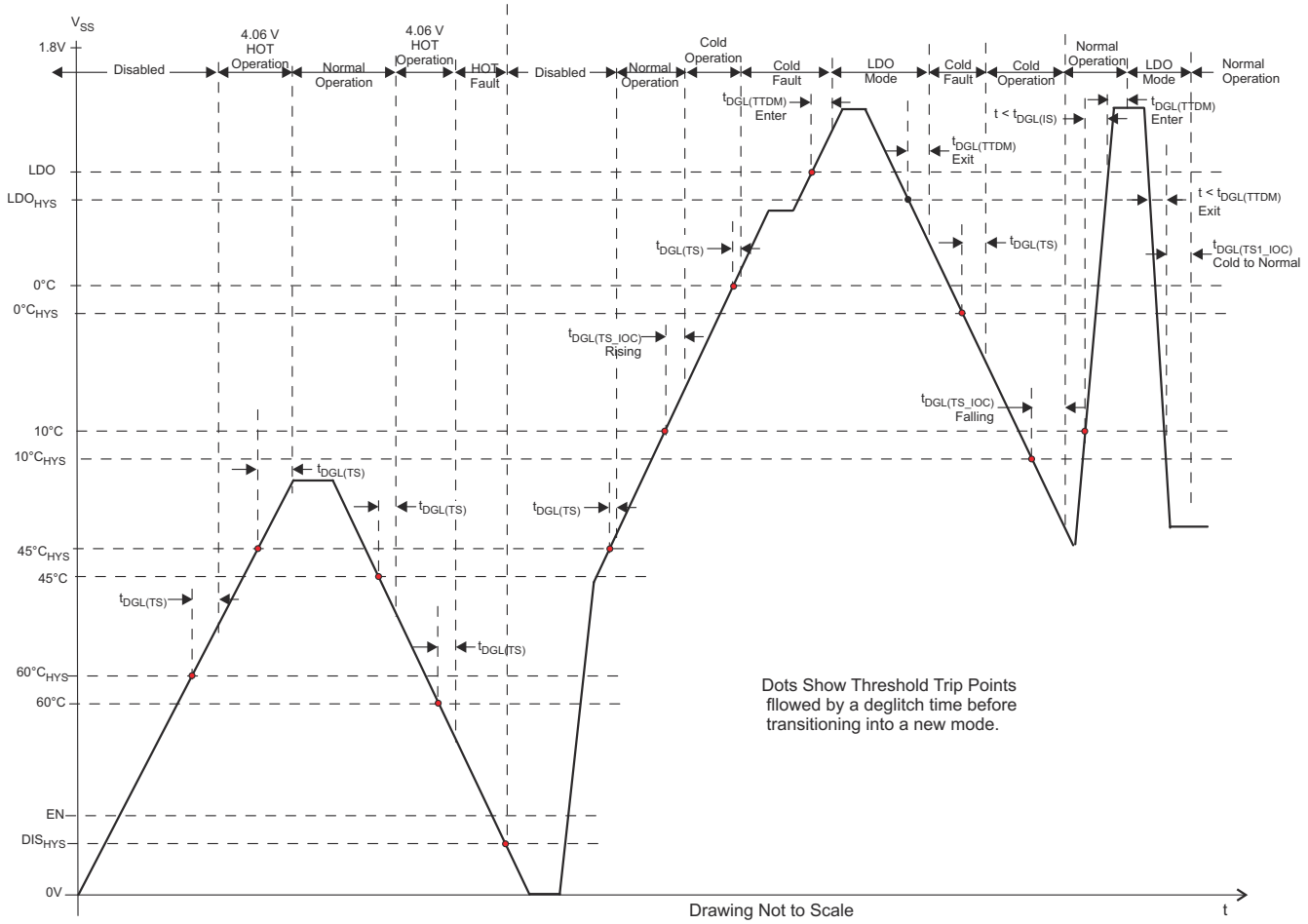


Figure 9-2. TS Battery Temperature Bias Threshold and Deglitch Timers

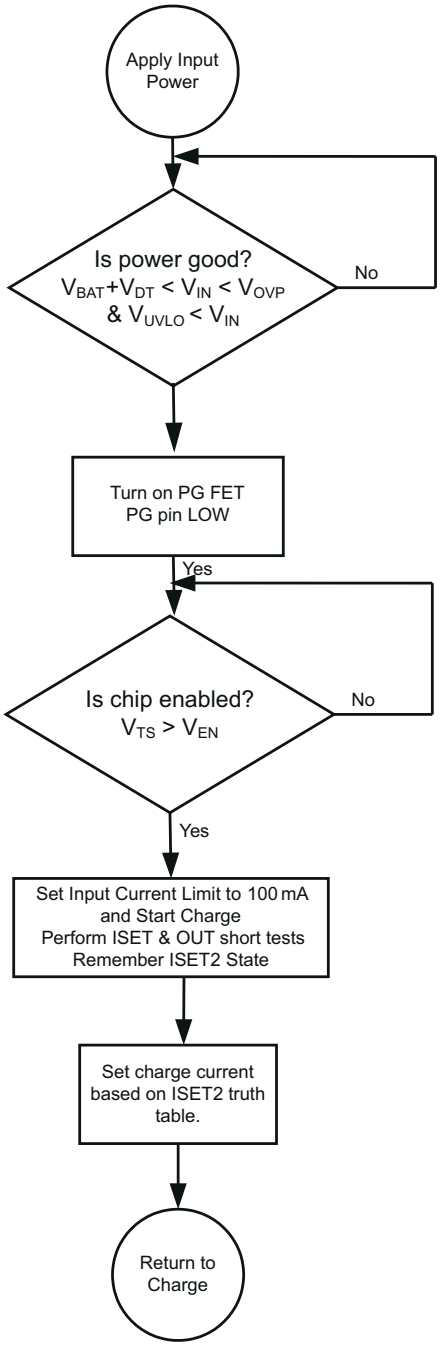


Figure 9-3. BQ2409x Power-Up Flow Diagram

9.3.6 Overvoltage Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ and $\overline{PG}$ pin goes to a high impedance state. Once the overvoltage returns to a normal voltage, the $\overline{PG}$ pin goes low, timer continues, charge continues and the $\overline{CHG}$ pin goes low after a 25ms deglitch. PG pin is optional on some packages.

9.3.7 Power Good Indication ($\overline{PG}$)

After application of a 5-V source, the input voltage rises above the UVLO and sleep thresholds ($V_{IN} > V_{BAT} + V_{DT}$), but is less than OVP ($V_{IN} < V_{OVP}$,), then the PG FET turns on and provides a low impedance path to ground. See Figure 8-1, Figure 8-2, and Figure 8-10.

9.3.8 $\overline{CHG}$ Pin Indication

The charge pin has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor.

The charge pin is high impedance in Sleep Mode and OVP (if $\overline{PG}$ is high impedance) and return to its previous state once the condition is removed.

Cycling input power, pulling the TS pin low and releasing or entering Precharge Mode causes the $\overline{CHG}$ pin to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

9.3.9 $\overline{CHG}$ and $\overline{PG}$ LED Pullup Source

For host monitoring, a pullup resistor is used between the STATUS pin and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the STATUS pin and a power source. If the $\overline{CHG}$ or $\overline{PG}$ source is capable of exceeding 7 V, a 6.2-V Zener diode should be used to clamp the voltage. If the source is the OUT pin, note that as the battery changes voltage, the brightness of the LEDs vary.

Table 9-1. $\overline{CHG}$ Pullup Source

CHARGING STATE	$\overline{CHG}$ FET/LED
1st Charge	ON
Refresh Charge	OFF
OVP	
SLEEP	
TEMP FAULT	ON for 1st Charge

Table 9-2. $\overline{PG}$ LED Pullup Source

V_{IN} POWER-GOOD STATE	$\overline{PG}$ FET/LED
UVLO	OFF
SLEEP Mode	
OVP Mode	
Normal Input (V_{OUT} + V_{DT} < V_{IN} < V_{OUP})	ON
PG is independent of chip disable	

9.3.10 IN-DPM (V_{IN-DPM} or IN–DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the V_{IN-DPM} threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than V_{IN-DPM} to power the out pin. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3 V and 4.4 V respectively. This is an added safety feature that helps protect the source from excessive loads.

9.3.11 OUT

The charger OUT pin provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT pin is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

9.3.12 ISET

An external resistor is used to program the output current (50 to 1000 mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} / I_{OUT}$$

where

- I_{OUT} is the desired fast charge current
- K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Figure 8-11 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15 A.

The ISET resistor is short protected and will detect a resistance lower than ≠340 Ω. The detection requires at least 80 mA of output current. If a *short* is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.1 A and 1.35 A and is independent of the ISET short detection circuitry, as shown in Figure 9-5. Also, see Figure 10-4 and Figure 8-7.

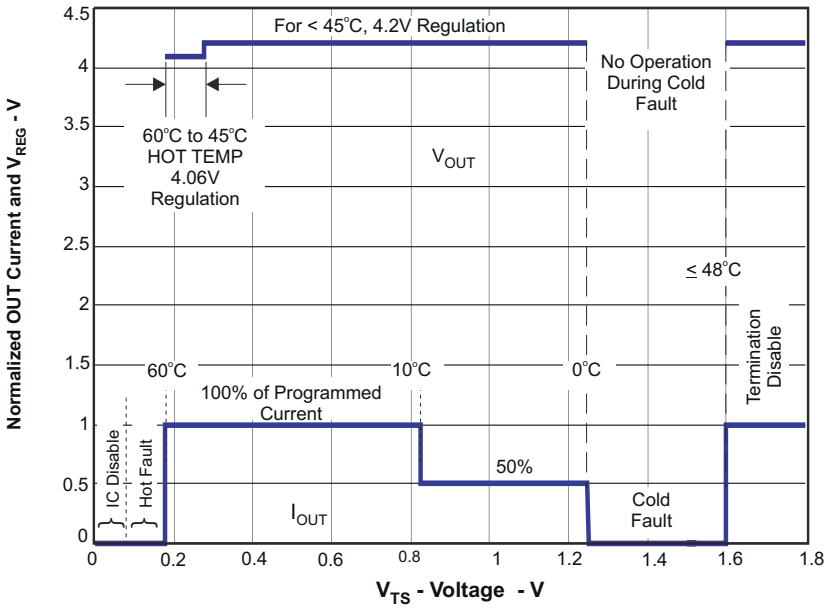


Figure 9-4. Operation Over TS Bias Voltage

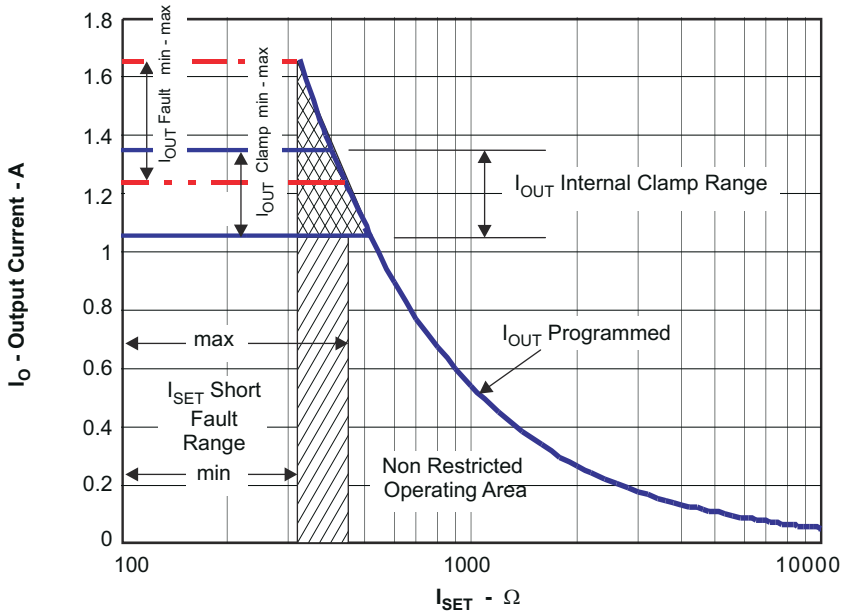


Figure 9-5. Programmed/Clamped Out Current

9.3.13 PRE_TERM – Precharge and Termination Programmable Threshold

PRE_TERM is used to program both the precharge current and the termination current threshold. The precharge current level is a factor of two higher than the termination current level. The termination can be set between 5% and 50% of the programmed output current level set by ISET. If left floating the termination and precharge are set internally at 10 and 20% respectively. The precharge-to-fast-charge, V_{lowv} threshold is set to 2.5 V.

$$R_{PRE\text{-}TERM} = \%Term \times K_{TERM} = \%Pre\text{-}CHG \times K_{PRE\text{-}CHG} \quad (2)$$

where

- %Term is the percent of fast charge current where termination occurs
- %Pre-CHG is the percent of fast charge current that is desired during precharge
- K_{TERM} and $K_{PRE\text{-}CHG}$ are gain factors found in the electrical specifications

9.3.14 ISET2

ISET2 is a 3-state input and programs the input current limit/regulation threshold. A low will program a regulated fast-charge current via the ISET resistor and is the maximum allowed input and output current for any ISET2 setting, Float programs a 100-mA current limit and high programs a 500-mA current limit.

Below are two configurations for driving the 3-state ISET2 pin:

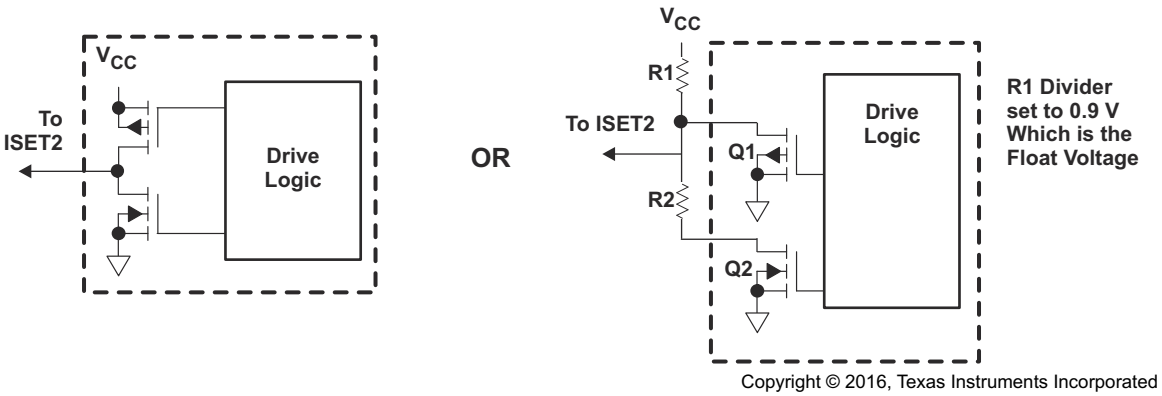


Figure 9-6. Configurations for Driving the 3-State ISET2 Pin

9.3.15 TS

The BQ2409x family contains an NTC monitoring function. The TS function for BQ24090, BQ24091, and BQ24095 follows the classic temperature range and disable charge when the battery temperature is outside of the 0°C and 45°C operating temperature window. The TS function for BQ24092 and BQ24093 is designed to follow the new JEITA temperature standard for Li-ion and Li-pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half, and if between 45°C and 60°C the regulation voltage is reduced to 4.1 V max, see Figure 9-4.

The BQ2409x family has devices to monitor 10-k and 100-k NTC thermistors. The BQ24090/2/5 are designed to work with a 10-k NTC. For these devices, the TS feature is implemented using an internal 50-µA current source to bias the thermistor (designed for use with a 10-k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS pin to V_{SS}. If this feature is not needed, a fixed 10-k can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS pin low to disable charge. The BQ24091/3 are designed to work with a 100-k NTC. For these devices, the TS feature is implemented using an internal 5-µA current source to bias the thermistor (designed for use with a 100-k NTC β = 3370) connected from the TS pin to V_{SS}. If this feature is not needed, a fixed 100-k can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS pin low to disable charge.

The TS pin has two additional features when the TS pin is pulled low or floated/driven high. A low disables charge (similar to a high on the $\overline{\text{BAT\_EN}}$ feature) and a high puts the charger in TTDM.

Above 60°C or below 0°C the charge is disabled. Once the thermistor reaches ≈–10°C the TS current folds back to keep a cold thermistor (between –10°C and –50°C) from placing the IC in the TTDM Mode. If the TS pin is pulled low into Disable Mode, the current is reduced to ≈30 µA, see Figure 9-2. Since the I_{TS} current is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10-k or 100-k (depending on the IC) NTC (at 25°C).

9.4 Device Functional Modes

9.4.1 Termination and Timer Disable Mode (TTDM) - TS Pin High

The battery charger is in TTDM when the TS pin goes high from removing the thermistor (removing battery pack/floating the TS pin) or by pulling the TS pin up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed, then the $\overline{\text{CHG}}$ pin will go to its high impedance state if not already there. If a battery is detected, the $\overline{\text{CHG}}$ pin does not change states until the current tapers to the termination threshold, where the $\overline{\text{CHG}}$ pin goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has precharge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{CHG}$ LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237-k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS pin into TTDM. This creates ≈0.1°C error at hot and a ≈3°C error at cold.

9.4.2 Timers

The precharge timer is set to 30 minutes. The precharge current, can be programmed to offset any system load, making sure that the 30 minutes is adequate.

The fast-charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and the $\overline{CHG}$ pin goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power, or going into and out of TTDM.

9.4.3 Termination

Once the OUT pin goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold, the $\overline{CHG}$ pin goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current terminates. If the battery was removed along with the thermistor, then the TS pin is driven high and the charge enters TTDM. If the battery was removed and the TS pin is held in the active region, then the battery detect routine continues until a battery is inserted.

9.4.4 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT pin at a useable voltage. Whenever the battery is missing the $\overline{CHG}$ pin should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if the battery is missing and not in TTDM. On power up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM or has a TS fault. See Figure 9-7 for the battery detect flow diagram.

9.4.5 Refresh Threshold

After termination, if the OUT pin voltage drops to V_{RCH} (100 mV below regulation) then a new charge is initiated, but the $\overline{CHG}$ pin remains at a high impedance (off).

9.4.6 Starting a Charge on a Full Battery

The termination threshold is raised by ≠14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

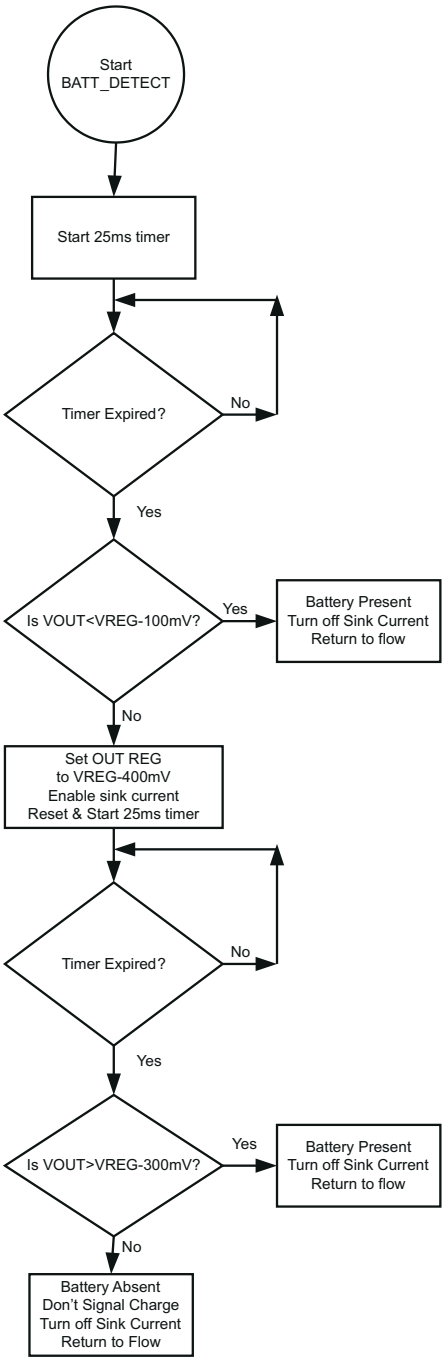


Figure 9-7. Battery Detect Routine

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The BQ2409x series of devices are highly integrated Li-ion and Li-pol linear chargers devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adaptors. These devices have a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

10.2 Typical Application

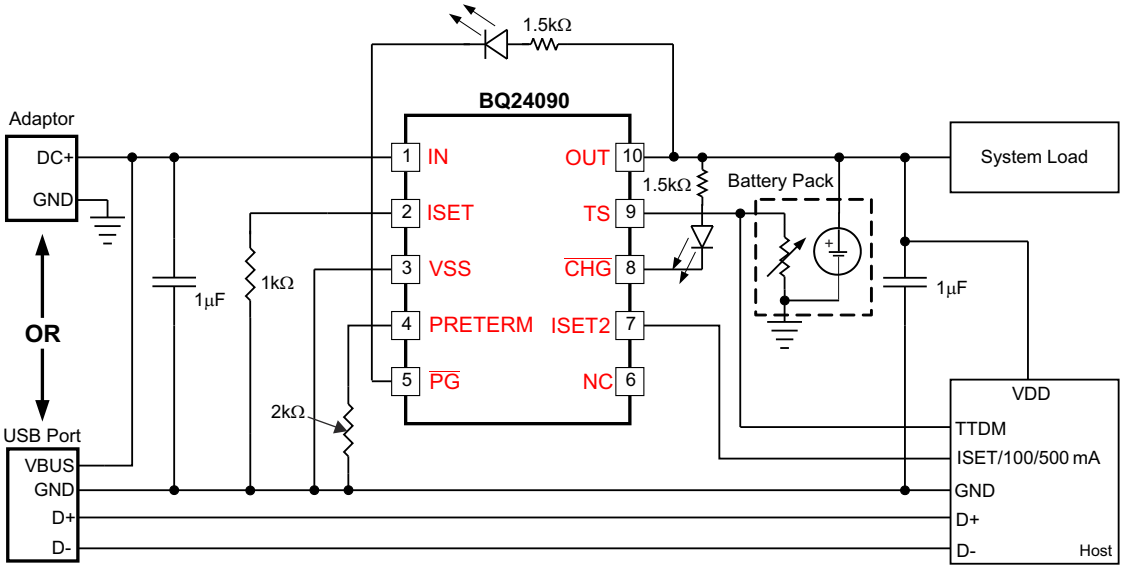


Figure 10-1. Typical Application Schematic

10.2.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: I_{OUT-FC} = 540 mA; ISET - pin 2
- Termination current threshold: $\%_{IOUT-FC}$ = 10% of fast charge or approximately 54 mA
- Pre-charge current by default is twice the termination current or approximately 108 mA
- TS – battery temperature sense = 10k NTC (103AT)

10.2.2 Detailed Design Procedure

10.2.2.1 Calculations

10.2.2.1.1 Program the Fast Charge Current, ISET:

$R_{ISET} = [K_{(ISET)} / I_{(OUT)}]$
from electrical characteristics table. . . $K_{(SET)}$ = 540 AΩ
R_{ISET} = [540AΩ/0.54A] = 1.0 kΩ
Selecting the closest standard value, use a 1-kΩ resistor between ISET (pin 16) and V_{SS}.

10.2.2.1.2 Program the Termination Current Threshold, ITERM:

$R_{PRE\text{-}TERM} = K_{(TERM)} \times \%_{IOUT\text{-}FC}$
$R_{PRE\text{-}TERM} = 200\ \Omega/\% \times 10\% = 2\ k\Omega$
Selecting the closest standard value, use a 2-kΩ resistor between ITERM (pin 15) and Vss.
One can arrive at the same value by using 20% for a pre-charge value (factor of 2 difference).
$R_{PRE\text{-}TERM} = K_{(PRE\text{-}CHG)} \times \%_{IOUT\text{-}FC}$
$R_{PRE\text{-}TERM} = 100\ \Omega/\% \times 20\% = 2\ k\Omega$

10.2.2.1.3 TS Function

Use a 10-kΩ NTC thermistor in the battery pack (103AT).

To disable the temp sense function, use a fixed 10-kΩ resistor between the TS (Pin 1) and Vss.

10.2.2.1.4 $\overline{CHG}$ and PG

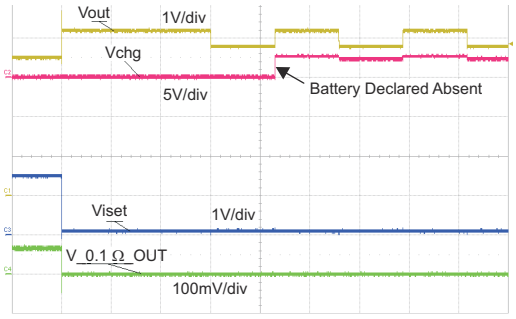
LED Status: connect a 1.5-kΩ resistor in series with a LED between the OUT pin and the $\overline{CHG}$ pin.
Connect a 1.5-kΩ resistor in series with a LED between the OUT pin and the PG pin.

Processor Monitoring: Connect a pull-up resistor between the processor power rail and the $\overline{CHG}$ pin.
Connect a pull-up resistor between the processor power rail and the PG pin.

10.2.2.2 Selecting IN and OUT Pin Capacitors

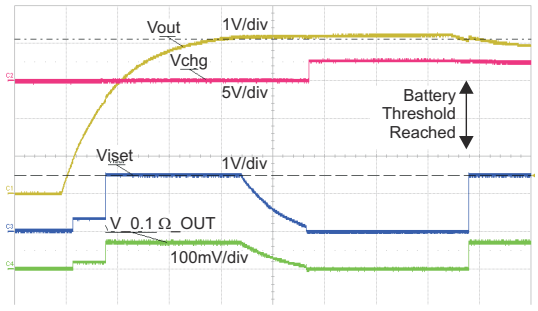
In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input and output pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify tested rating with capacitor manufacturer).

10.2.3 Application Curves



Continuous battery detection when not in TTDM.

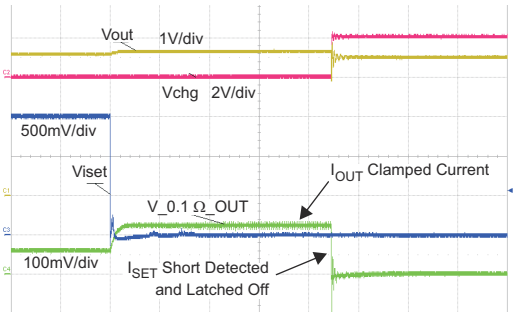
Figure 10-2. Battery Removal with Fixed TS = 0.5 V



CH4: Iout (1 A/Div)

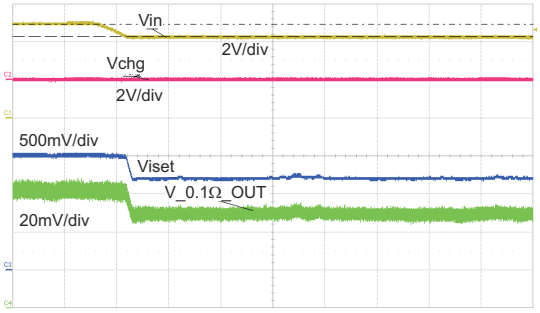
Battery voltage swept from 0 V to 4.25 V to 3.9 V.

Figure 10-3. Battery Charge Profile



CH4: Iout (1 A/Div)

Figure 10-4. ISET Shorted During Normal Operation



CH4: Iout (0.2 A/Div)

Figure 10-5. DPM – Adaptor Current Limits – Vin Regulated

11 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 12 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the BQ2409x IN and GND terminals, a larger capacitor is recommended.

12 Layout

12.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the BQ2409x, with short trace runs to both IN, OUT and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The BQ2409x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10mil vias in the power pad of the IC and in close proximity to conduct the heat to the bottom ground plane. The bottom ground place should avoid traces that “cut off” the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8 mil thick) copper on top and bottom, and is a good example of optimal thermal performance.

12.2 Layout Example

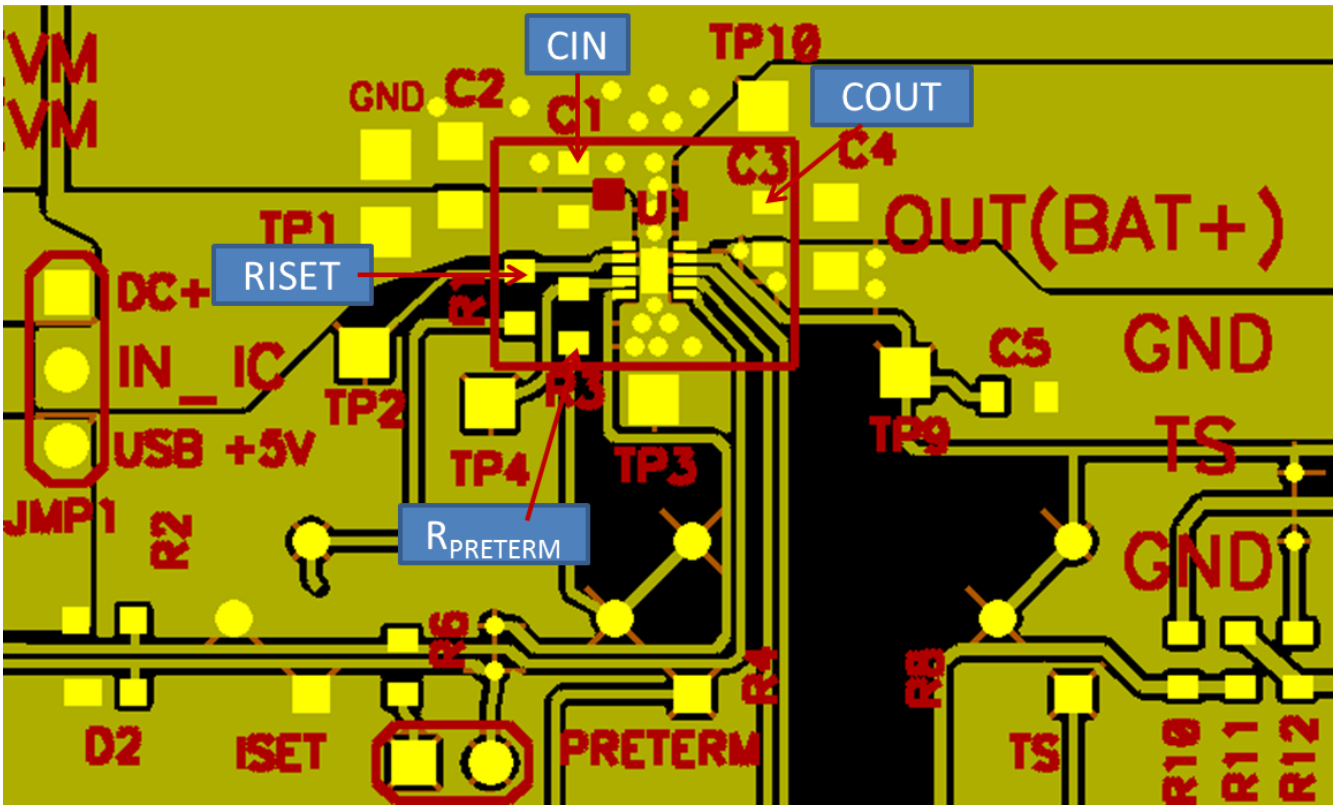


Figure 12-1. PCB Layout Example

12.3 Thermal Considerations

The BQ2409x family is packaged in a thermally enhanced MSOP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS pin. Full PCB design guidelines for this package are provided in the *PowerPAD Thermally Enhanced Package Application Report*. The most common measure of package thermal

performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = (T_J - T) / P \quad (3)$$

where

- T_J = chip junction temperature
- T = ambient temperature
- P = device power dissipation

Factors that can influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-ion and Li-pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(BAT)}] \times I_{(BAT)}$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

12.3.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery will discharge the battery is an easy calculation. The time from full to discharge can be calculated by dividing the amp-hour capacity of the battery by the leakage current. For a 0.75-AHr battery and a 10-µA leakage current (750 mAHr/0.010 mA = 75000 Hours), it would take 75 k hours or 8.8 years to discharge. In reality the self discharge of the cell would be much faster so the 10--µA leakage would be considered negligible.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24090DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 125	24090	Samples
BQ24090DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 125	24090	Samples
BQ24091DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	24091	Samples
BQ24091DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	24091	Samples
BQ24092DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	24092	Samples
BQ24092DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	24092	Samples
BQ24093DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	24093	Samples
BQ24093DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	24093	Samples
BQ24095DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 125	24095	Samples
BQ24095DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 125	24095	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

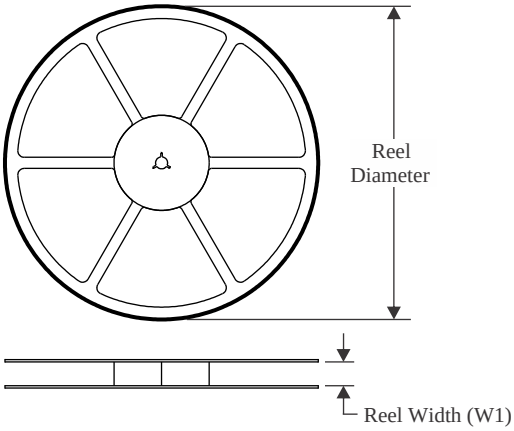
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

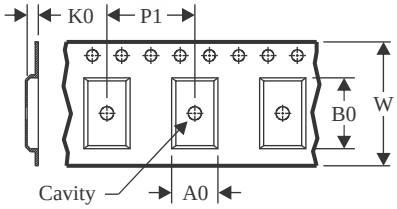
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

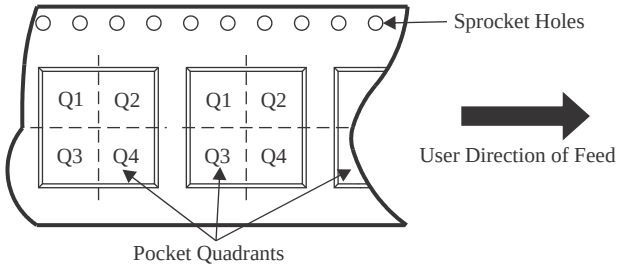


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

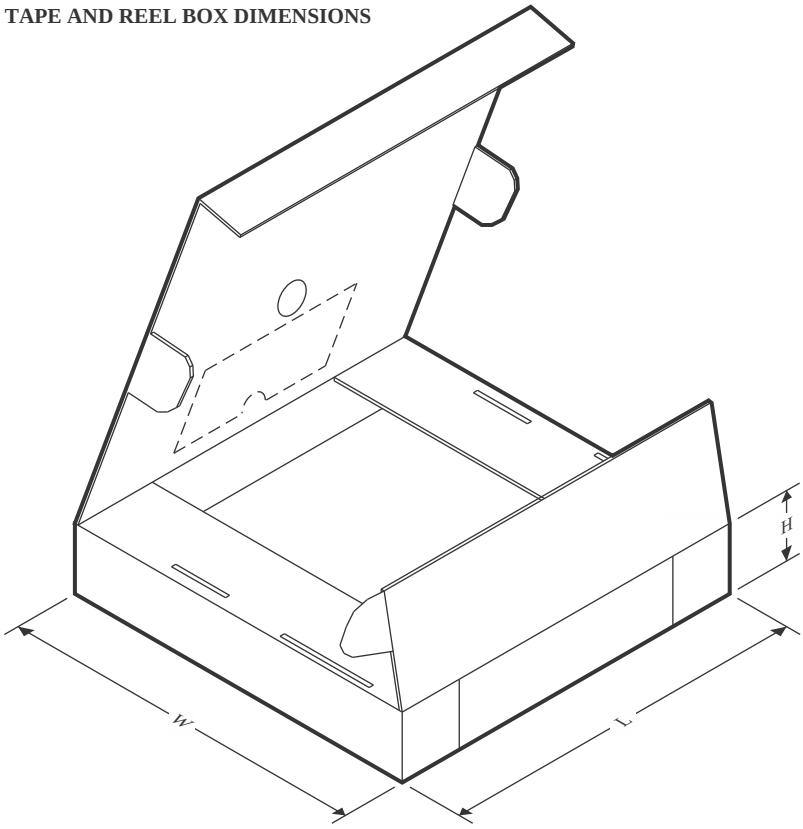
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24090DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
BQ24090DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24090DGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
BQ24090DGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24091DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24091DGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24092DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24092DGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
BQ24092DGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24093DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24093DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
BQ24093DGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24093DGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
BQ24095DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24095DGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
BQ24095DGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24090DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0
BQ24090DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
BQ24090DGQT	HVSSOP	DGQ	10	250	200.0	183.0	25.0
BQ24090DGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0
BQ24091DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
BQ24091DGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0
BQ24092DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
BQ24092DGQT	HVSSOP	DGQ	10	250	200.0	183.0	25.0
BQ24092DGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0
BQ24093DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
BQ24093DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0
BQ24093DGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0
BQ24093DGQT	HVSSOP	DGQ	10	250	200.0	183.0	25.0
BQ24095DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
BQ24095DGQT	HVSSOP	DGQ	10	250	203.0	203.0	35.0
BQ24095DGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0

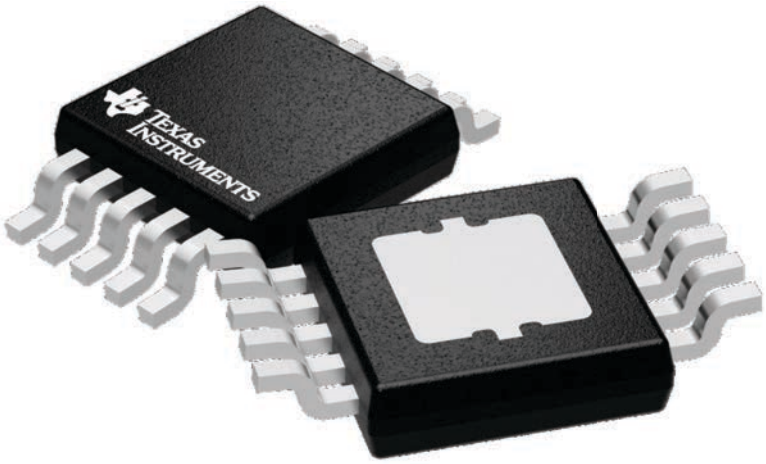
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

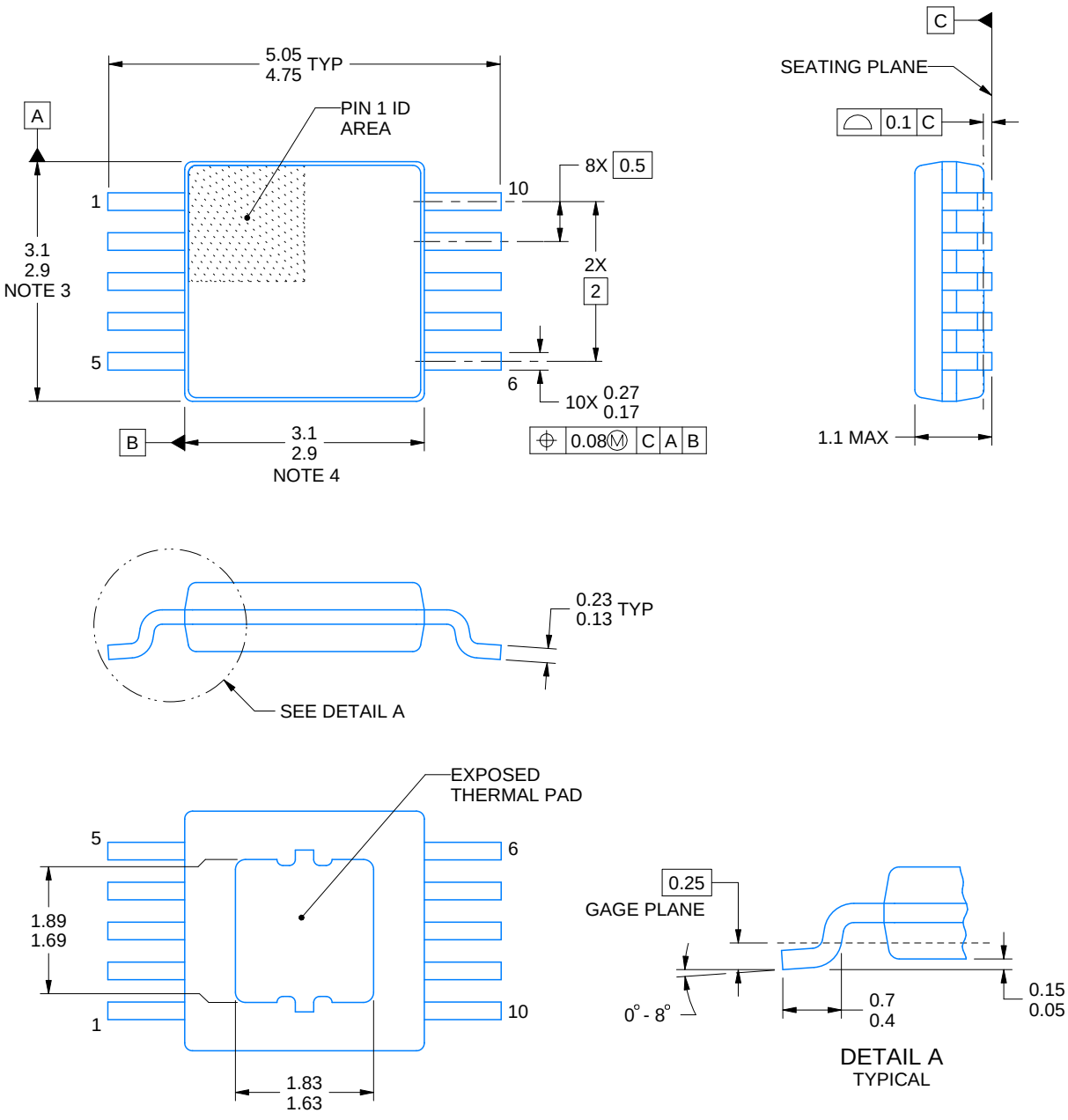
4224775/A

PACKAGE OUTLINE

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



4218842/B 04/2024

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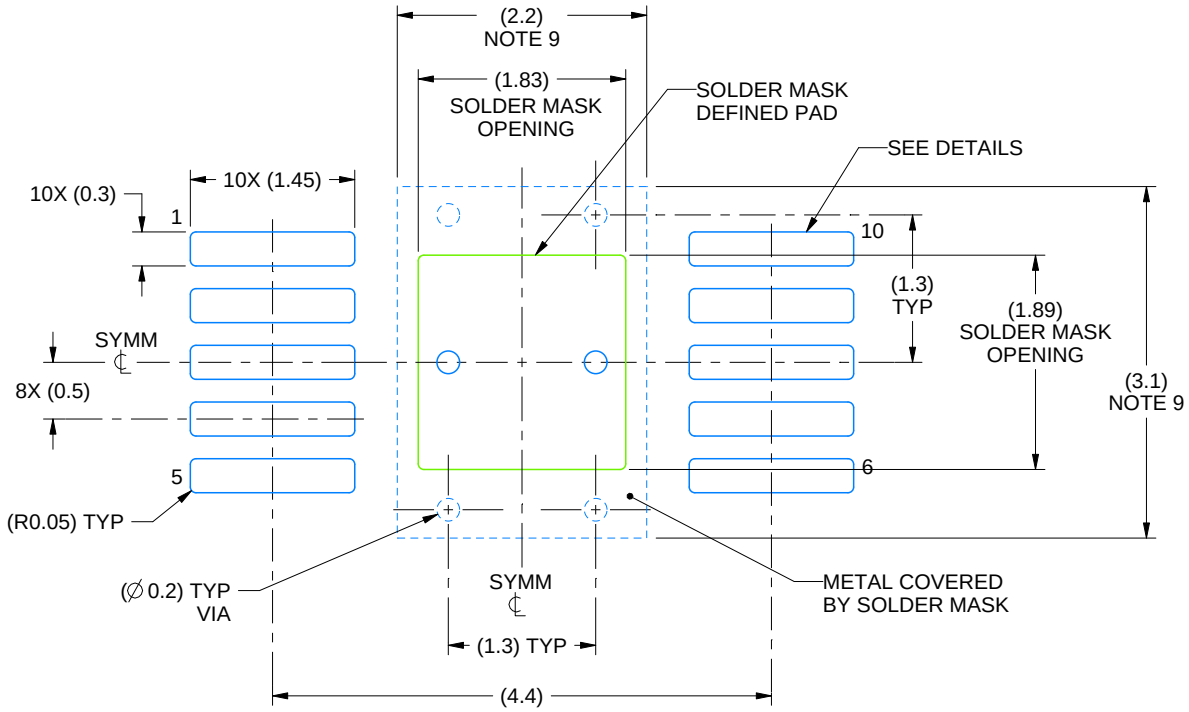
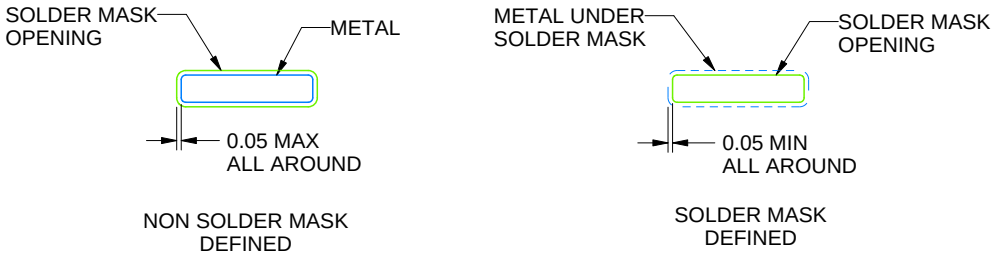
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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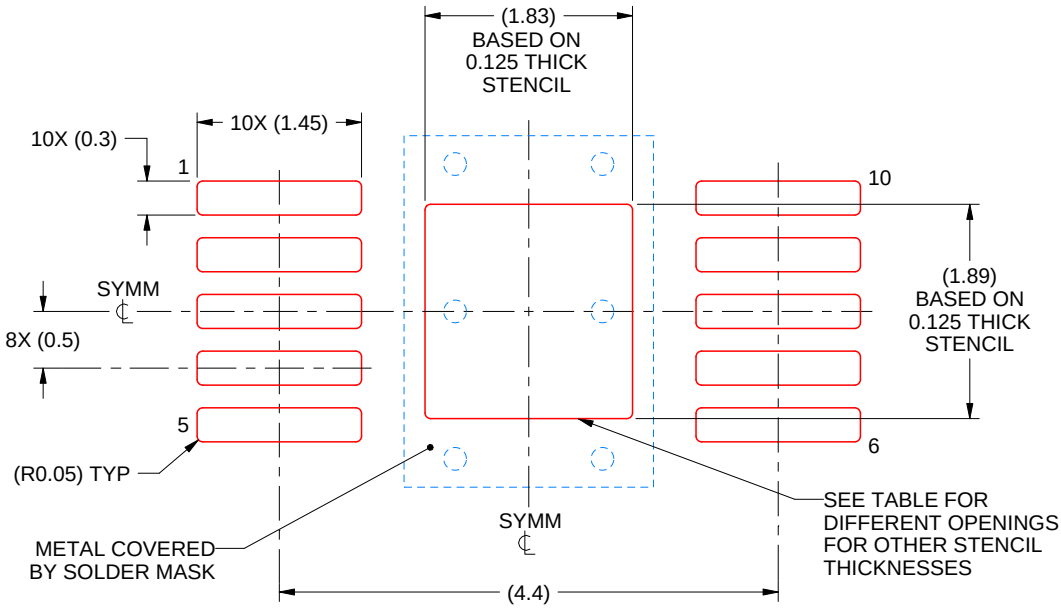
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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