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Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level:

☐ Security 1 - SMIC Confidential ☑ Security 2 - SMIC Restricted ☐ Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T		2002-10-22	Chin Chang Liao	Initiate
0.1T	0.1	2003-06-10	JianHua_Ju	Add Technology Develop Revision:0.1
1.0	1	2004-10-21	Cindy Zhang	Modify ESD rule 2 & 4.
2.0	1	2004-11-18	Cindy Zhang	a) Modify Doc. title. b) Add HV ESD design rule, page 6.
3P	2.0	2005-7-29	Cindy Zhang	1) Separated HV 5V/40V ESD design rule from original document; please refer to document TD-HV18-DR-2007 for HV 5V/40V ESD design rule. 2) Added the descriptions before ESD rule: a) For NMOS ESD protection device, ESD implant is optional. b) The guideline is for I/O 3.3V ESD circuit design without ESD implant. (in page 5) 3) Added design rule 5, 18 &19: DCP, contact number and via number rules. (in page 5 & 6) 4) Modified Fig. 2 with clear gate connection. 5) Modified some literal descriptions in page 13. 6) Updated ESD imp rule 5 from 0.45um to 0.4um. (in page 12).
4P	2.0	2005-10-13	Cindy Zhang	Corrected typing mistake in latch up rule 3 on page 14 (from S2≥30um to S2≤30um).

1. Title:

0.18um Logic 1P6M salicide IO 3.3V ESD and Latch-Up Guideline

2. Purpose:

This guideline is about concepts, issues of practical ESD protection and Latch-Up prevention design and layouts.

3. Scope: All SMIC Fabs.

4. Nomenclature: NA

5. Reference:

1) 0.18um Logic 1P6M Salicide 1.8/3.3V Current Density Design Rules (TD-LO18-DR-2006v0.1T)
2) 0.18μm Generic IO 3.3V ESD Characterization Report (TD-LO18-99-2006)

6. Responsibility: Logic Technology Development Center.

7. Content:

SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION

0. 18um Logic 1P6M Salicide IO 3.3V ESD and Latch-Up Guideline

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I/O 3.3V ESD Design and Layout Guideline:

- **The ESD guideline is to ensure to pass HBM-2KV, and MM-200V spec according to EIA/JEDEC standard and EIA/JESD22 test standard.**
- **The guideline provides layout structure and dimension for N/P MOS ESD protection device design.**
- **Silicide block (SAB) at drain side is essential in ESD design.**
- **For NMOS ESD protection device, ESD implant is optional.**
- **The guideline is for I/O 3.3V ESD circuit design without ESD implant.**
- **For 5V tolerant I/O circuits using stack (cascaded) 3.3V I/O device, ESD implant is required.**

Rule No.	Description	Layout Rule (Unit in um)
1	Finger-type structure with uniform finger width is suggested for N/P MOS ESD protection design	
2	Minimum channel width of NMOS and PMOS for I/O buffer and Vdd to Vss protection.(Channel width=Finger width x Finger No.)	360
3	Gate length for protection circuits: Minimum Lg for 3.3V I/O NMOS Minimum Lg for 3.3V I/O PMOS	 0.35 0.3
4	Unit finger width of NMOS and PMOS for I/O buffer, and Vdd-to-Vss protection.	20≤ F≤ 60 (Fig.1)
5	Minimum spacing of poly edge to CT edge on drain side (DCP) for NMOS and PMOS.	2.22 (Fig.1)
6	Minimum spacing of poly edge to CT edge on source side (SCP) for NMOS and PMOS.	0.75 (Fig.1)
7	SAB should block at least on drain side of NMOS and PMOS (contact region should be kept silicided.)	Fig. 3
8	Minimum width of SAB on drain side (A) and SAB edge to AA edge (B)	B≥A≥2.0 (Fig. 3)
9	For 3.3V I/O, SAB on the drain side of NMOS region needs to overlap the poly gate by	0.06 (Fig. 3)

10	ESD protection devices should be surrounded by pick-up ring with appropriate bias.	(Fig. 1)
11	Gate coupled technique is recommended for better uniformity ESD discharge path of finger-type structure.	Fig. 2
12	The NMOS/PMOS can be added after resistor R as the secondary ESD protection for better ESD immunity if there is no conflict with circuit operation.	Fig. 2
13	Minimum value of I/O resister R as shown in Fig.2	200 Ω
14	The suggested device size for secondary protection are: 3.3V I/O NMOS 3.3V I/O PMOS	 20/0.35 20/0.30
15	For 5V tolerant I/O designed by 3.3V NMOS or PMOS, the spacing between active poly gate and inactive poly gate of stack NMOS should be close.	Fig.4 & Fig.5
16	For 5V tolerant I/O designed by 3.3V NMOS or PMOS, SAB needs to cover all top poly gates and extend to overlap the second poly gate by	0.06 (Fig. 5)
17	For 5V tolerant I/O using stack 3.3V NMOS, ESD implant is required.	
18*	Contacts should be used as many as possible, and at least capable of bearing 100mA DC current, That is, the minimum number of contacts (drawn on rule) should be	189
19*	Vias should be used as many as possible, and at least capable of bearing 100mA DC current, That is, the minimum number of vias (drawn on rule) should be	358
20	Minimum total width of metal lines to connect bonding pad and ESD protecting devices.	W1=20 (Fig. 1)
21	Minimum metal width on drain side of ESD devices.	W2=4.5 (Fig.1)
22	Minimum Vss and Vdd power ring metal width	50
23	Corners of conducting layers in ESD discharge paths	45^{O}
24	All nodes directly connecting to ESD discharge path should follow ESD dimension rules.	

25 AA area of edge side of ESD devices or I/O buffers should be Source or Bulk rather than Drain (Fig. 1), to avoid the unwanted parasitic bipolar effect or abnormal discharge path in ESD zapping.

*** Calculated from contact/via current density rule. (TD-LO18-DR-2006v0.1T)**

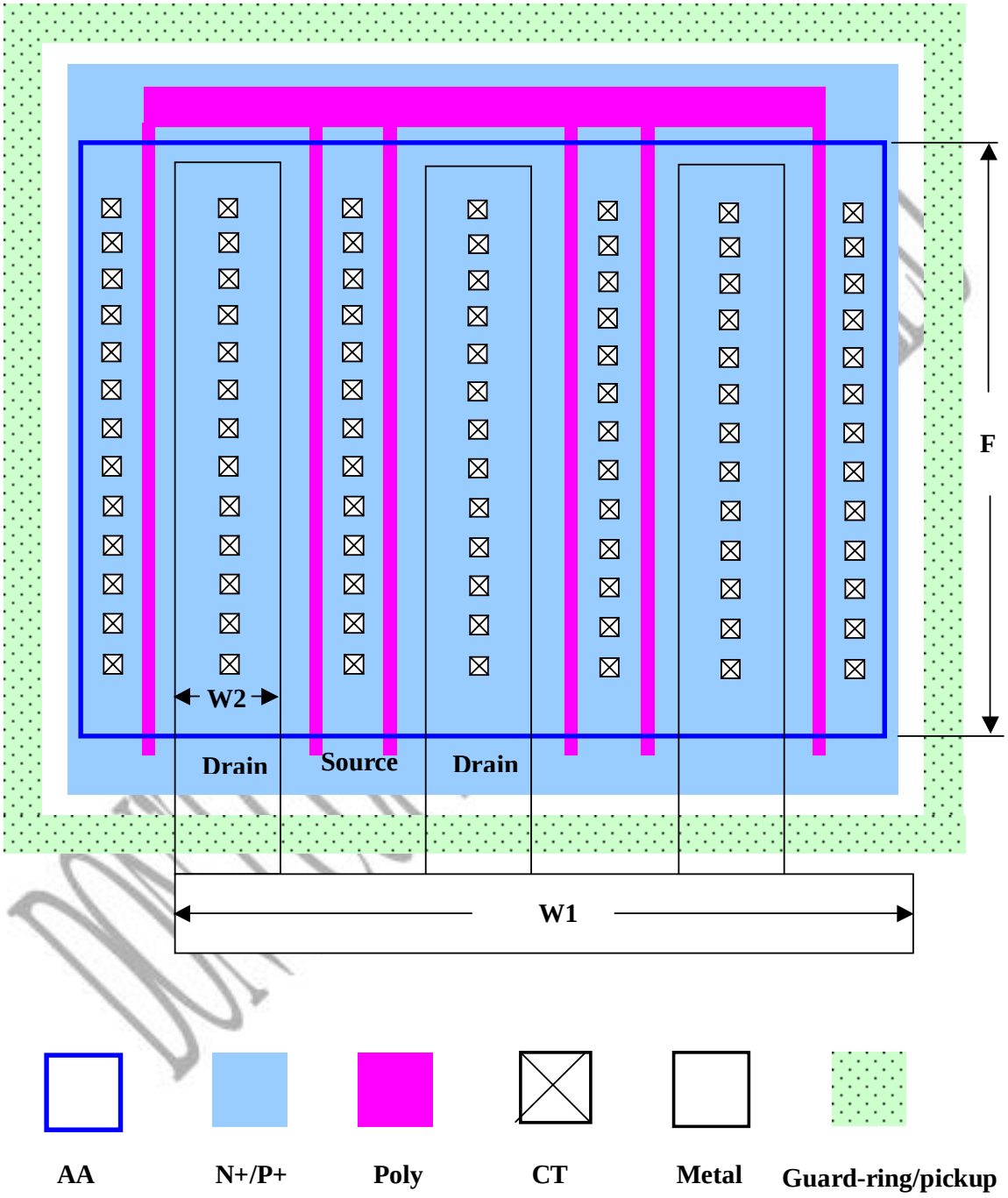

Fig.1 ESD Cell Layout Example

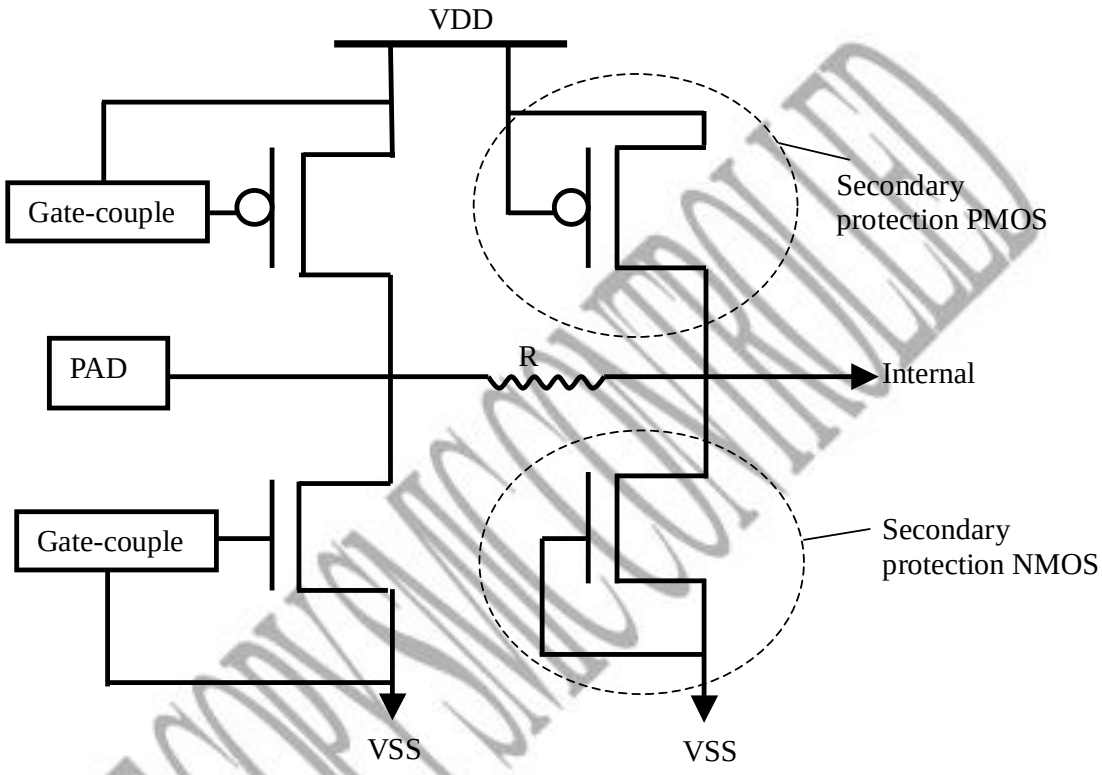

Fig. 2 ESD Protection Scheme

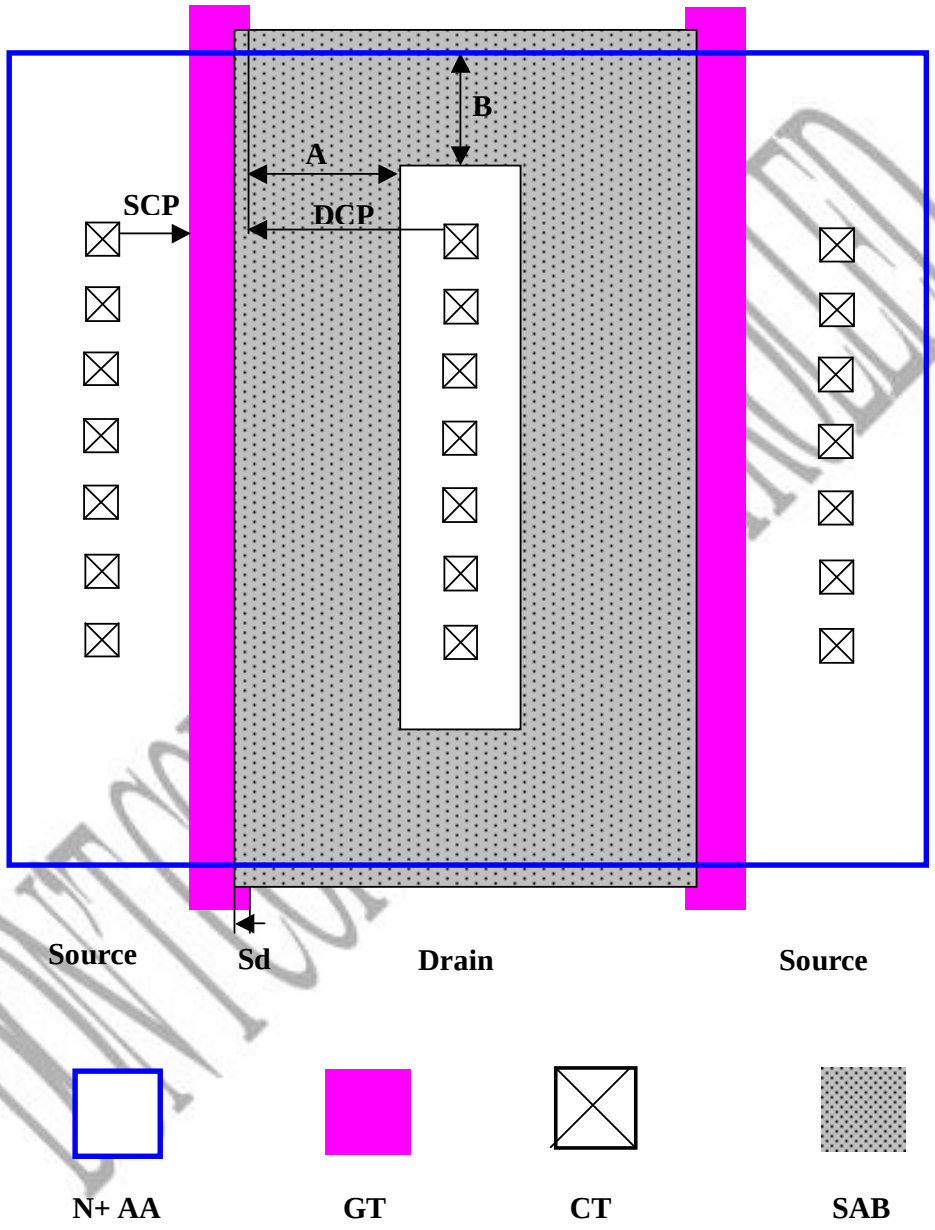

Fig.3 NMOS/PMOS I/O for ESD Protection

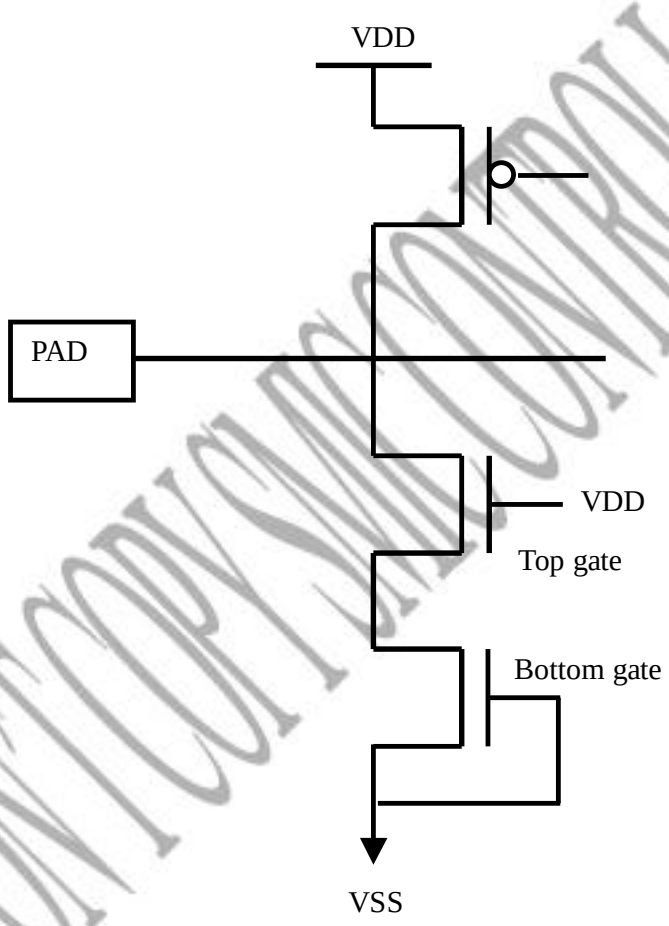

Fig. 4 5V Tolerant 3.3V I/O ESD protection using stacked NMOS

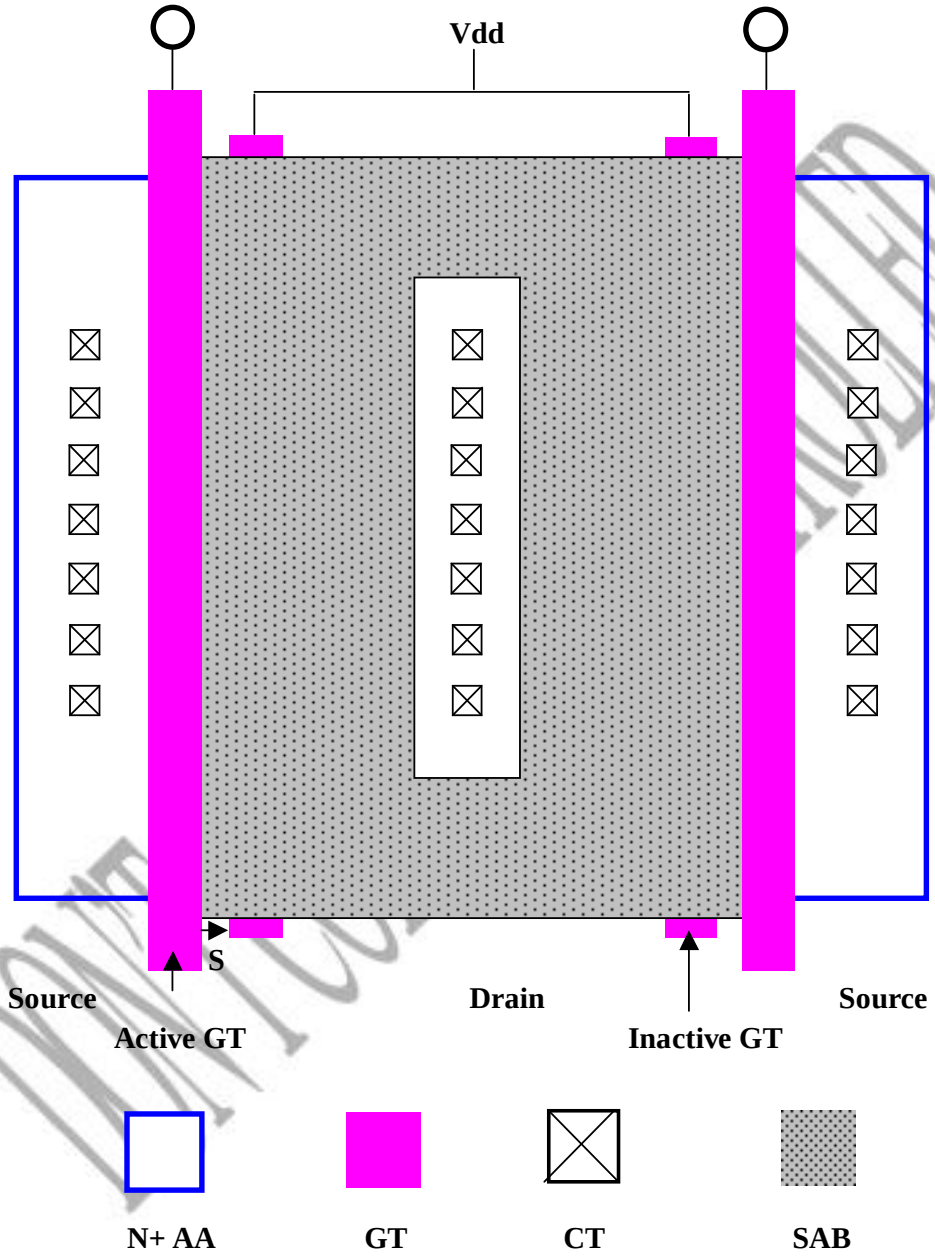

Fig.5– Stack (or Cascaded) NMOS for 5V Tolerant 3.3V I/O

ESD Implantation Guideline

- **ESD implantation layer (P+ type) is for NMOS to further improve ESD performance. It is an optional layer.**
- **This implantation layer can be drawn as a block and generated from logic operation.**

Rule No.	Description	Layout Rule (Unit in um)
ESD.1	Minimum width of an ESD implant region.	0.6
ESD.2	Minimum space between two ESD implant region. Merge if the spec is less than this space	0.6
ESD.3	Minimum space between an ESD implant and SN or SP region in different AA.	0.3
ESD.4	Minimum clearance from an ESD implant region to an SN AA region of different device.	0.6
ESD.5	Minimum clearance from an ESD implant region to a N-channel Poly gate along the direction of poly gate.	0.4
ESD.6	Minimum overlap from an ESD implants edge to an AA region.	0.45
ESD.7	Minimum enclosure of an ESD implant region beyond an ESD implant AA region.	0.25
ESD. 8	ESD implant region is not allowed to overlap with SP.	

ESD Implant

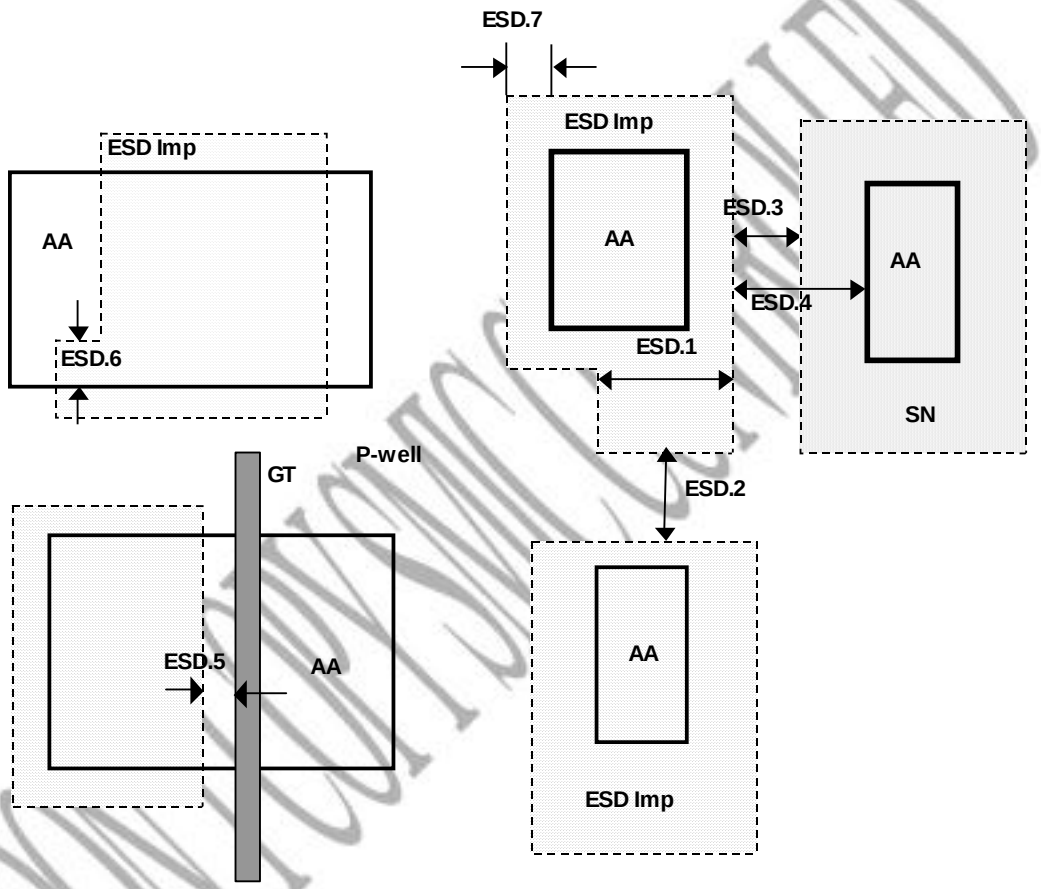

Fig. 6

0.18um IO 3.3V Latch-Up Prevention Layout Guidelines

Rule No.	Description	Layout Rule
1	A double ring structure should be used to surround the NMOS and PMOS for I/O buffers and ESD devices.	Fig. 7
2.	Minimum space between NMOS and PMOS for I/O buffer and ESD devices.	S1≥ 15um
3.	Maximum space from any point within Source/Drain region to the nearest pickup AA region inside the same well for I/O and internal circuits.	S2≤30um
4.	Between I/O buffer and internal circuits, a double ring structure with NW psudo-collector and p+pickup is necessary.	Fig. 8
5.	Minimum space between I/O buffer and internal circuit region.	S3≥ 50um
6.	Hot AA region connecting to I/O pads should be surrounded by a double ring structure	
7.	NW without direct connection to VDD and with hot AA region within it should be enclosed by a double ring structure	
8.	A double ring structure should be inserted surrounding and between the special devices such as bipolar transistor, diode, resistor, or special circuits such as charge pump, power regulator, high noise or high power circuitry.	
9.	All the guard rings and pickups should be connected to VDD/VSS with tiny series resistance. That is, NW should be tied together with N+AA, and AA should be tied together with contacts and metals of VDD/VSS. Contacts and via's should be used as many as possible.	

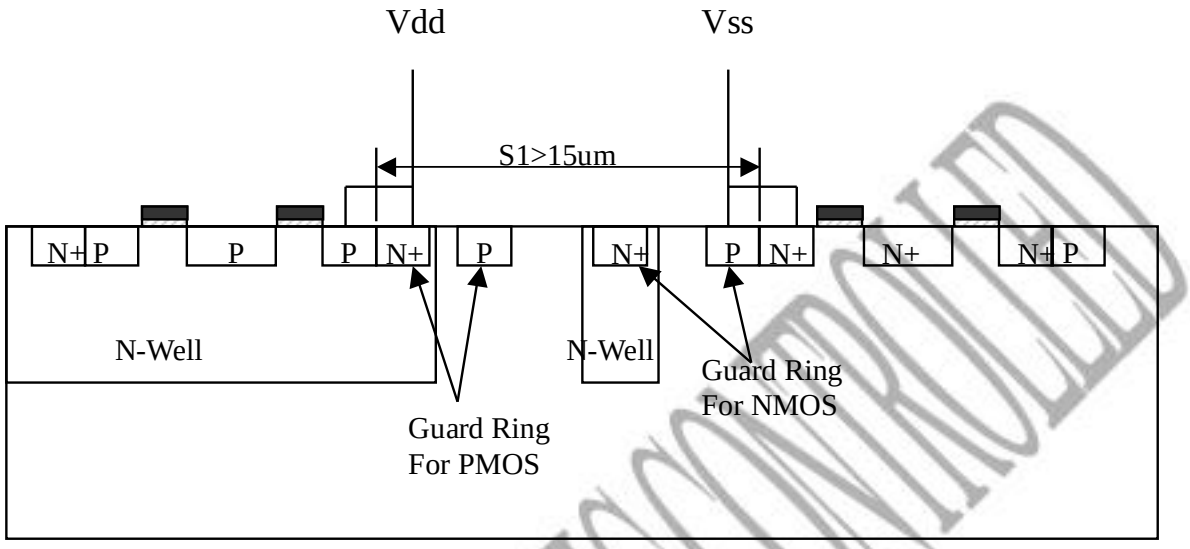

Fig. 7

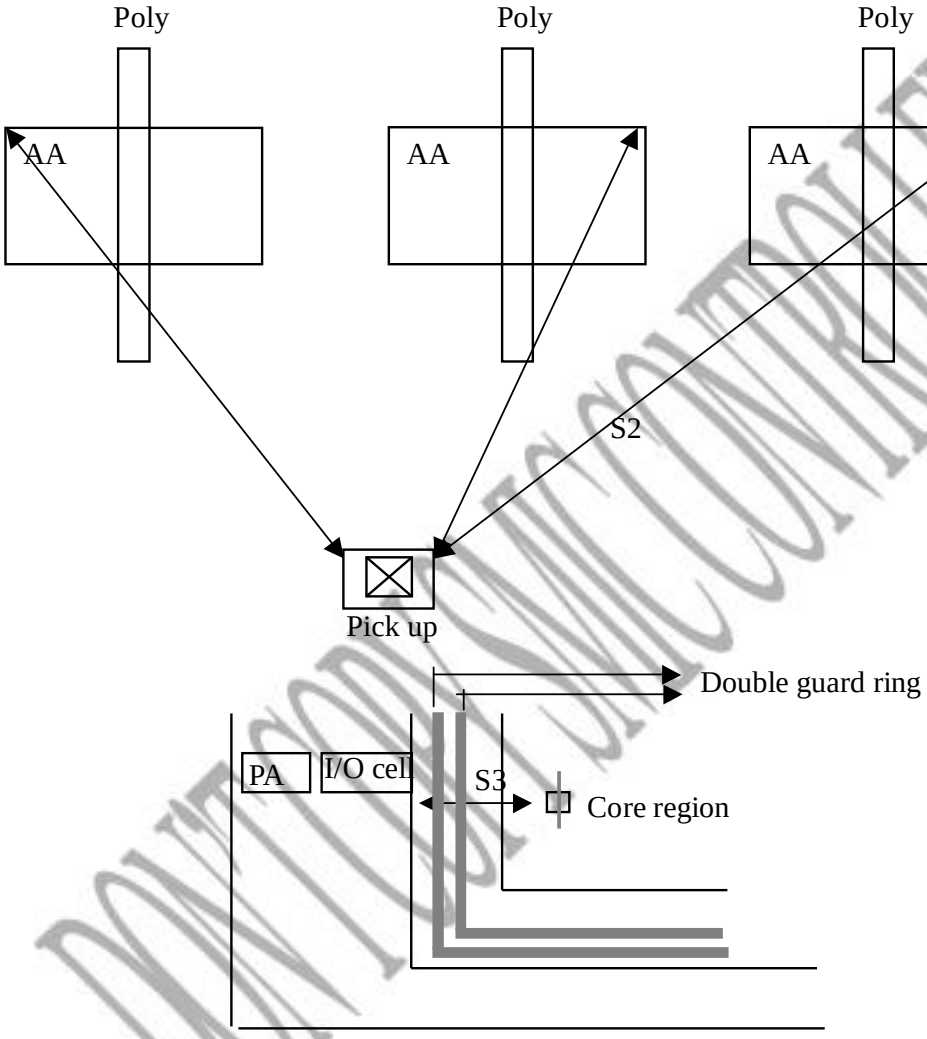

Fig. 8