



**SMIC 0.18µm Logic18 Process
1.8-Volt SAGE-X™
Standard Cell Library
Databook**

March 2003

Release 1.0

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Revision History

This document contains the release history for the SMIC 0.18µm (Logic18) Process SAGE-X™ Standard Cell Library Databook.

| Part Number | Release Number | Date of Release | Updates |
|---------------------|----------------|-----------------|---|
| DB-SX-SMC001-1.0/18 | 1.0 | March 2003 | <ul style="list-style-type: none">Initial release |

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Introduction

Artisan's SAGE-X™ standard cell library builds upon our SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- *Global Parameters* provides an overview of parameters specific to your SAGE-X library.
- *Special Cells* details the types of special cells included in the library.
- *Reading the Standard Cell Datasheet* describes the components of each datasheet.

Datasheets for each cell in this library are provided after the introduction. The datasheets are included in alphabetical order within the following categories:

- Base Cells
- Advanced Arithmetic Cells
- Register File Cells
- Synthesis Optimized Arithmetic Cells

Global Parameters

This section specifies global parameters for the SMIC 0.18µm (Logic18) Process SAGE-X™ Standard Cell Library. It covers physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this library.

Table 1. Physical Specifications

| | |
|--|-----------|
| Drawn Gate Length (μm) | 0.18 |
| Layers of Metal | 4, 5 or 6 |
| Layout Grid (μm) | 0.005 |
| Vertical Pin Grid (μm) | 0.56 |
| Horizontal Pin Grid (μm) | 0.66 |
| Cell Power and Ground Rail Width (μm) | 0.8 |

In this library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The SAGE-X library also supports designs with four, five or six layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "SMIC 0.18 μm LOGIC 1P6M Salicide 1.8v/3.3v process" design rule manual. You must define these rules correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

| Parameter | Minimum | Maximum |
|-------------------------|---------|---------|
| DC Supply Voltage (Vdd) | 1.62V | 1.98V |
| Junction Temperature | 0°C | 125°C |

Table 3 shows the derating factors for this SAGE-X Standard Cell Library.

Table 3. Derating Factors

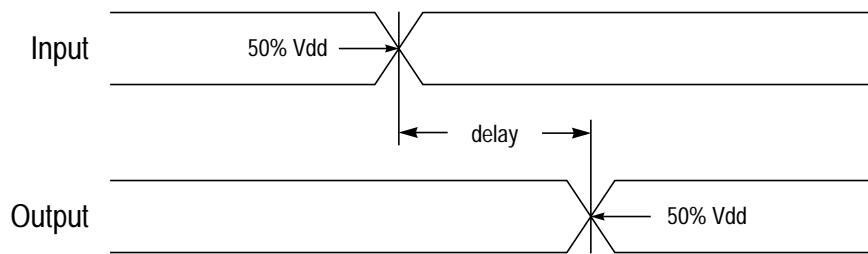
| | |
|--------------------------------|-------|
| K_{Process} (slow) | 1.25 |
| K_{Process} (typical) | 1.0 |
| K_{Process} (fast) | 0.804 |

Table 3. Derating Factors

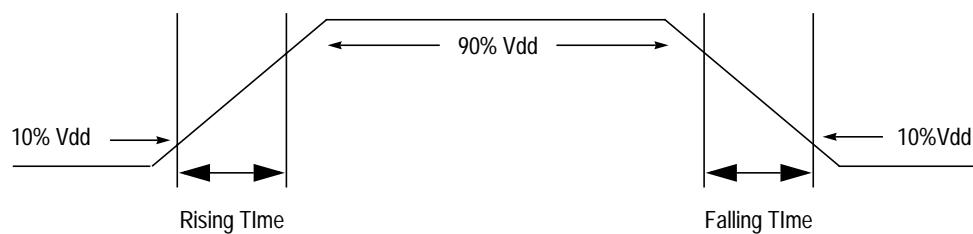
| | |
|----------------------------|-----------|
| K_{Volt} (1.8V to 1.62V) | -0.69/V |
| K_{Volt} (1.8V to 1.98V) | -0.481/V |
| K_{Temp} (25°C to 0°C) | 0.00166°C |
| K_{Temp} (25°C to 125°C) | 0.00157°C |

Propagation Delay and Transition Time

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay.

Figure 1. Propagation Delay

The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 illustrates transition time measurements for rising and falling signals.

Figure 2. Transition Time

Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.03 ns and a linearized load factor, K_{load} , which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.66 μ m horizontal pitch) and metal3 (0.56 μ m vertical pitch) routing grid across the entire cell layout.

The SAGE-X Standard Cell Library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. Table 3 on page 12 provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load} , and C_{load}) and the delay derating factors, the estimated total propagation delay is calculated as such:

$$t_{TPD} = (K_{Process}) \cdot [1 + (K_{Volt} \cdot \Delta V_{dd})] \cdot [1 + (K_{Temp} \cdot \Delta T)] \cdot t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} \cdot C_{load})$$

where:

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner—1.8V, 25°C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;
 K_{Volt} = voltage derating factor (/V);
 ΔV_{dd} = $V_{dd} - 1.8V$;
 K_{Temp} = temperature derating factor (/°C);
 ΔT = junction temperature - 25 °C.

Timing Constraints

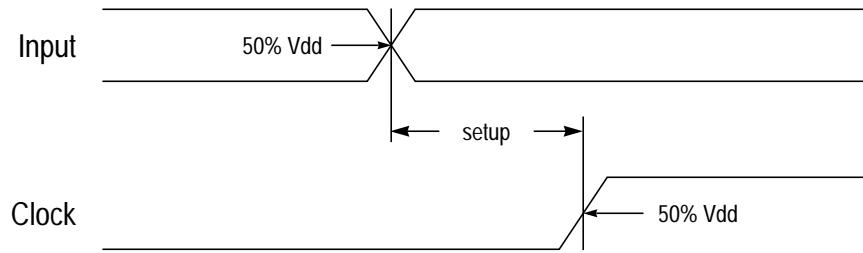
Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.028ns data slew and 0.028ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.66μm horizontal pitch) and metal3 (0.56μm vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

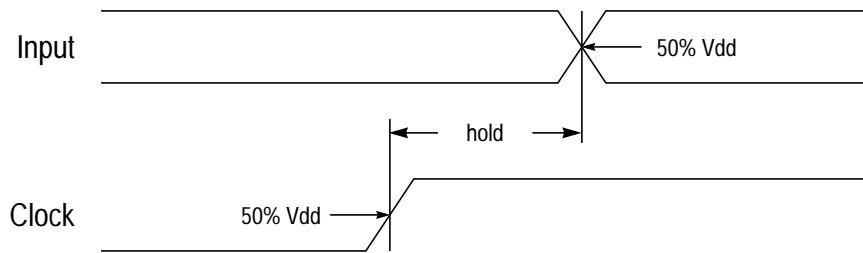
Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup constraint values are measured as the interval between the data signal crossing 50% of V_{dd} and the clock signal crossing 50% of V_{dd} . For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

Figure 3. Setup Time**Hold Time**

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

NOTE: Artisan does not incorporate any hold time margins in the Synopsys, TLF, StarDC, or any other timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

Figure 4. Hold Time

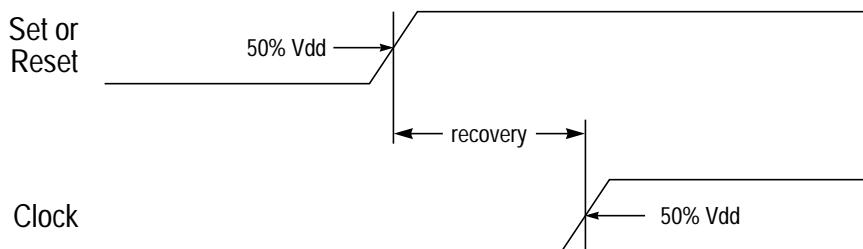
Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%.

Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time.

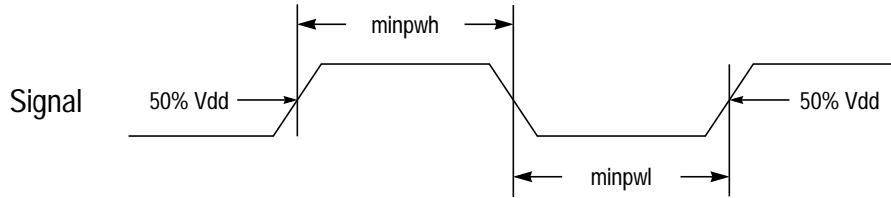
Figure 5 illustrates recovery time.

Figure 5. Recovery Time



Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 6 illustrates minimum pulse width.

Figure 6. Minimum Pulse Width

Minimum pulse width is defined as 0.516ns for all set/reset pins (SN, RN) and 0.35ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Power Dissipation

The SAGE-X Standard Cell Library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The SAGE-X library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell ($\mu\text{W}/\text{MHz}$) when the corresponding pin changes state at 25°C, 1.8V, and typical process. The energy data in the tables were measured for an input slew of 0.03ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^x (E_{in} \bullet f_{in}) + \sum_{n=1}^y \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

where:

- P_{avg} = average power (μW);
- x = number of input pins;
- E_{in} = energy associated with the n th input pin ($\mu\text{W}/\text{MHz}$);
- f_{in} = frequency at which the n th input pin changes state during the normal operation of the design (MHz);
- y = number of output pins;
- C_{on} = external capacitive loading on the n th output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);
- Vdd = operating voltage = 1.8V;
- f_{on} = frequency at which the n th output pin changes state during the normal operation of the design (MHz);
- E_{os} = energy associated with the output pin for sequential cells only ($\mu\text{W}/\text{MHz}$).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFXL Cell

For this exercise, assume that a DFFXL cell has clock switching at 133MHz, input and output pins switching at 20MHz, and an external capacitive loading on the output pin of 0.02pF. Using the AC Power table provided in the sample DFF datasheet on page 27, the power dissipated by the DFFXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^x (E_{in} \bullet f_{in}) + \sum_{n=1}^y \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

Given:

$$x = 2;$$

$$E_{i1} = 0.0056 \mu\text{W}/\text{MHz};$$

$$E_{i2} = 0.0063 \mu\text{W}/\text{MHz};$$

$$f_{i1} = 20 \text{ MHz};$$

$$f_{i2} = 133 \text{ MHz};$$

$$y = 2;$$

$$C_{o1} = 0.02 \text{ pF};$$

$$C_{o2} = 0.02 \text{ pF};$$

$$Vdd = 1.0\text{V};$$

$$f_{o1} = 20 \text{ MHz};$$

$$f_{o2} = 20 \text{ MHz};$$

$$E_{os} = 0.0060 \mu\text{W}/\text{MHz},$$

we have:

$$\begin{aligned} P_{avg} &= \sum_{n=1}^2 (E_{in} \bullet f_{in}) + \sum_{n=1}^2 \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1} \\ P_{avg} &= (E_{i1} \bullet f_{i1}) + (E_{i2} \bullet f_{i2}) \\ &\quad \left(C_{o1} \bullet VDD^2 \bullet \frac{1}{2} f_{o1} \right) + \left(C_{o2} \bullet VDD^2 \bullet \frac{1}{2} f_{o2} \right) \\ &\quad + (E_{os} \bullet f_{o1}) \end{aligned}$$

$$\begin{aligned} P_{\text{avg}} &= (0.0056 \bullet 20) + (0.0063 \bullet 133) \\ &\quad + \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20) \right) + \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20) \right) \\ &\quad + (0.0060 \bullet 20) \\ P_{\text{avg}} &= 1.46 \mu\text{W} \end{aligned}$$

Power-Rail Strapping

You must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

- I_{avg} = total average current for the module, calculated from previous section (mA);
- w_{m1} = VSS/VDD metal1 wire width (μm), see Physical Specifications;
- r = number of rows in module;
- d_{m1} = maximum metal1 current density allowed for the process (mA/ μm);
- d_{m2} = maximum metal2 current density allowed for the process (mA/ μm);
- I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);
- I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);
- w_{m2} = metal2 wire width required for vertical strapping (μm);
- c = minimum number of metal2 straps;

we have:

$$I_{m1} = w_{m1} \bullet r \bullet 2 \bullet d_{m1},$$

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$$I_{\text{strap}} = \frac{(I_{\text{avg}} - I_{m1})}{2},$$

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$$w_{m2} = \frac{I_{\text{strap}}}{d_{m2}},$$

It is recommended that the metal2 wire width, w_{m2} , be divided into c equal portions which are spaced equidistant across the module, where

$$c = \frac{I_{\text{avg}}}{I_{m1}}, \text{ rounded up to the next integer.}$$

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the SAGE-X Standard Cell Library, each cell is designed with a uniform cell height of $5.04\mu\text{m}$ (i.e., 9 tracks tall with $0.56\mu\text{m}$ per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, you may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s).

Table 4 indicates which DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

| Row Separation in Number of Grids | Expected DRC Violations | Action to Correct DRC Violations |
|-----------------------------------|-------------------------|--|
| 0 (Rows Abut) | None | None |
| 1 | NP/PP space < 0.28μm | Draw NWELL layer between rows to merge NWELL regions above and below row separation. |
| 2 | NWELL space < 0.6μm | Draw NWELL layer between rows to merge NWELL regions above and below row separation. |
| 3 | NWELL space < 0.6μm | Draw NWELL layer between rows to merge NWELL regions above and below row separation. |
| 4 | None | None |
| 5 or more | None | None |

Special Cells

This section discusses special cells in the SAGE-X Standard Cell Library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The SMIC antenna effect prevention guideline, "SMIC 0.18μm LOGIC 1P6M Salicide 1.8v/3.3v process," specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

Fill Cells

The library contains several FILL cells: FILL1, FILL2, FILL4, FILL8, FILL16, FILL32, FILL64. The number appended to "FILL" in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

Reading the Standard Cell Datasheet

Please refer to the sample datasheet for DFF on pages 27 and 28 for the arrangement of each of the following datasheet sections.

NOTE: This datasheet contains sample characterization values.

1. Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Functions

The function table gives all possible combinations of input and output signals for the cell. Table 5 defines the symbols used in datasheet function tables.

Table 5. Functions Key

| Symbol | Description |
|--------|------------------------|
| 0 | Logic Low |
| 1 | Logic High |
| ↖ | High to Low Transition |
| ↙ | Low to High Transition |
| x | Don't Care |
| IL | Illegal/Undefined |
| Z | High Impedance |

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (μm) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an “X” followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed ($\mu\text{W}/\text{MHz}$) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C , 1.0V, typical process, input slew of 0.03ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, and input slew of 0.03ns.

10. Timing Constraints

The timing constraints table in the sample DFF datasheet shows the timing conditions (ns) required at 25°C, 1.0V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.028ns data slew and 0.028ns clock slew. Hold constraint values are measured for 0.028ns data slew and 0.028ns clock slew. Minimum pulse width is defined to be 0.516ns for all set/reset pins and 0.35ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

▼ This datasheet contains sample characterization values. ▼

Process Technology:
CustomerName & Code

Cell Description
The DFF cell is a positive-edge-triggered, static D-type flip-flop.

Function

| D | CK | Q[n+1] | QN[n+1] |
|---|----|--------|---------|
| 0 | — | 0 | 1 |
| 1 | — | 1 | 0 |
| x | — | Q[n] | QN[n] |

Logic Symbol

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFXL | 3.69 | 7.36 |
| DFFX1 | 3.69 | 7.36 |
| DFFX2 | 3.69 | 8.74 |
| DFFX4 | 3.69 | 11.50 |

(1)
(4)
(5)

(2)
(3)
(6)
(7)

Functional Schematic

Artisan SAGE-X™ Standard Cell Library Databook

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▼ This datasheet contains sample characterization values. ▼

Process Technology: _____
CustomerName & Code _____

DFF

8 AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0056 | 0.0063 | 0.0081 | 0.0133 |
| CK | 0.0063 | 0.0068 | 0.0087 | 0.0128 |
| Q | 0.0060 | 0.0080 | 0.0124 | 0.0223 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0013 | 0.0013 | 0.0015 | 0.0023 |
| CK | 0.0015 | 0.0019 | 0.0022 | 0.0035 |

9 Delays at 25°C, 1.0V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.1662 | 0.1427 | 0.1287 | 0.1105 | 7.8830 | 4.2853 | 1.9344 | 0.9666 |
| CK → Q↓ | 0.1357 | 0.1098 | 0.0983 | 0.0920 | 4.3787 | 2.4148 | 1.1764 | 0.5884 |
| CK → QN↑ | 0.1828 | 0.1515 | 0.1342 | 0.1292 | 7.8631 | 4.2693 | 1.9226 | 0.9616 |
| CK → QN↓ | 0.2156 | 0.1947 | 0.1789 | 0.1547 | 3.9375 | 2.1923 | 1.1262 | 0.5569 |

10 Timing Constraints at 25°C, 1.0V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0469 | 0.0547 | 0.0391 | 0.0391 |
| | setup↓ → CK | 0.1094 | 0.1250 | 0.1094 | 0.1016 |
| | hold↑ → CK | -0.0312 | -0.0312 | -0.0234 | -0.0234 |
| | hold↓ → CK | -0.0312 | -0.0469 | -0.0312 | -0.0312 |
| CK | minpwh | 0.0933 | 0.0835 | 0.0738 | 0.0641 |
| | minpwl | 0.1418 | 0.1224 | 0.1127 | 0.0835 |

Base Cells

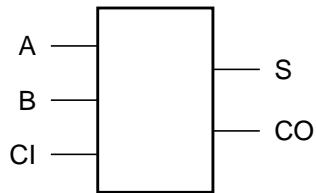
Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



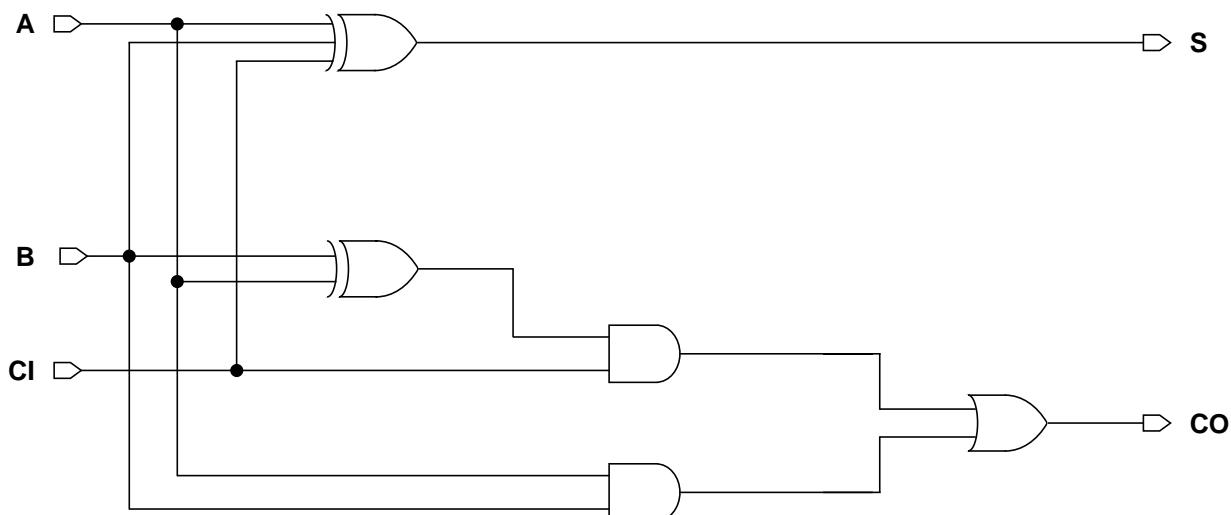
Functions

| CI | A | B | S | CO |
|----|---|---|---|----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| ADDFXL | 5.04 | 13.86 |
| ADDFX1 | 5.04 | 13.86 |
| ADDFX2 | 5.04 | 13.86 |
| ADDFX4 | 5.04 | 15.18 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.1189 | 0.1189 | 0.1441 | 0.2227 |
| B | 0.1542 | 0.1542 | 0.1942 | 0.2717 |
| Cl | 0.0666 | 0.0666 | 0.0949 | 0.1796 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0075 | 0.0075 | 0.0075 | 0.0075 |
| B | 0.0073 | 0.0073 | 0.0073 | 0.0073 |
| Cl | 0.0068 | 0.0068 | 0.0068 | 0.0068 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A → S↑ | 0.2142 | 0.2161 | 0.2363 | 0.2918 | 4.2638 | 4.2205 | 2.1162 | 1.0506 |
| A → S↓ | 0.2678 | 0.2789 | 0.3094 | 0.3748 | 2.9047 | 2.6700 | 1.4019 | 0.7188 |
| B → S↑ | 0.2520 | 0.2541 | 0.2711 | 0.3150 | 4.2730 | 4.2243 | 2.1189 | 1.0531 |
| B → S↓ | 0.3049 | 0.3160 | 0.3466 | 0.4121 | 2.9045 | 2.6700 | 1.4019 | 0.7187 |
| Cl → S↑ | 0.1683 | 0.1702 | 0.1977 | 0.2642 | 4.2671 | 4.2225 | 2.1185 | 1.0530 |
| Cl → S↓ | 0.1438 | 0.1553 | 0.1856 | 0.2503 | 2.9213 | 2.6793 | 1.4132 | 0.7293 |
| A → CO↑ | 0.2563 | 0.2565 | 0.2843 | 0.3473 | 4.2123 | 4.2005 | 2.1059 | 1.0435 |
| A → CO↓ | 0.2486 | 0.2556 | 0.2861 | 0.3435 | 2.7505 | 2.6023 | 1.3707 | 0.7023 |
| B → CO↑ | 0.2929 | 0.2931 | 0.3209 | 0.3836 | 4.2115 | 4.2002 | 2.1057 | 1.0434 |
| B → CO↓ | 0.2750 | 0.2789 | 0.3048 | 0.3535 | 2.6458 | 2.5596 | 1.3405 | 0.6769 |
| Cl → CO↑ | 0.1397 | 0.1409 | 0.1691 | 0.2357 | 4.2466 | 4.2141 | 2.1144 | 1.0493 |
| Cl → CO↓ | 0.1684 | 0.1766 | 0.2081 | 0.2688 | 2.7942 | 2.6197 | 1.3790 | 0.7064 |

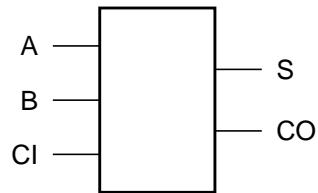
Cell Description

The ADDFH cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



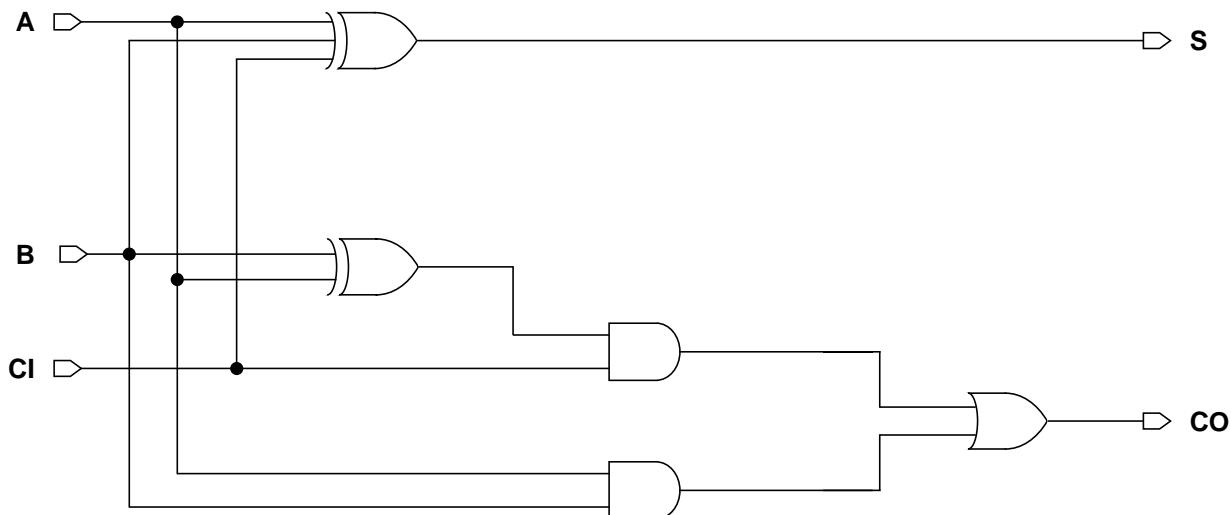
Functions

| CI | A | B | S | CO |
|----|---|---|---|----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| ADDFHXL | 5.04 | 14.52 |
| ADDFHX1 | 5.04 | 15.18 |
| ADDFHX2 | 5.04 | 22.44 |
| ADDFHX4 | 5.04 | 23.10 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.1245 | 0.1452 | 0.2694 | 0.3147 |
| B | 0.1117 | 0.1321 | 0.2360 | 0.2847 |
| Cl | 0.0642 | 0.0730 | 0.1249 | 0.1738 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0047 | 0.0067 | 0.0121 | 0.0121 |
| B | 0.0091 | 0.0147 | 0.0267 | 0.0267 |
| Cl | 0.0025 | 0.0045 | 0.0083 | 0.0084 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A → S↑ | 0.3484 | 0.2327 | 0.2236 | 0.2423 | 5.8999 | 4.2061 | 2.1298 | 1.0423 |
| A → S↓ | 0.3317 | 0.2583 | 0.2437 | 0.2697 | 3.6732 | 2.5770 | 1.3074 | 0.6633 |
| B → S↑ | 0.2512 | 0.1704 | 0.1513 | 0.1745 | 5.9258 | 4.2089 | 2.1310 | 1.0434 |
| B → S↓ | 0.3116 | 0.2026 | 0.1822 | 0.2111 | 3.6607 | 2.5761 | 1.3074 | 0.6633 |
| Cl → S↑ | 0.2993 | 0.1859 | 0.1641 | 0.1913 | 5.9104 | 4.2085 | 2.1307 | 1.0433 |
| Cl → S↓ | 0.2673 | 0.1879 | 0.1628 | 0.1955 | 3.6821 | 2.5817 | 1.3097 | 0.6645 |
| A → CO↑ | 0.3534 | 0.2327 | 0.2229 | 0.2411 | 5.9106 | 4.2050 | 2.1298 | 1.0424 |
| A → CO↓ | 0.3505 | 0.2541 | 0.2408 | 0.2652 | 3.7527 | 2.5715 | 1.3058 | 0.6617 |
| B → CO↑ | 0.2205 | 0.1535 | 0.1404 | 0.1595 | 5.9364 | 4.2063 | 2.1303 | 1.0426 |
| B → CO↓ | 0.3269 | 0.1904 | 0.1724 | 0.1963 | 3.7722 | 2.5548 | 1.3010 | 0.6573 |
| Cl → CO↑ | 0.1405 | 0.1073 | 0.0938 | 0.1087 | 5.9288 | 4.2082 | 2.1308 | 1.0431 |
| Cl → CO↓ | 0.2164 | 0.1457 | 0.1291 | 0.1524 | 3.8555 | 2.5932 | 1.3142 | 0.6653 |

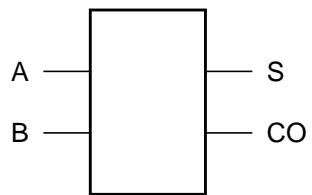
Cell Description

The ADDH cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$$

$$CO = A \bullet B$$

Logic Symbol



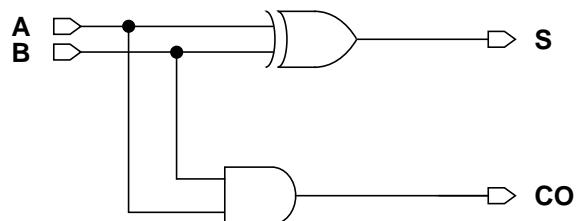
Functions

| A | B | S | CO |
|---|---|---|----|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| ADDHXL | 5.04 | 7.26 |
| ADDHX1 | 5.04 | 7.92 |
| ADDHX2 | 5.04 | 11.88 |
| ADDHX4 | 5.04 | 18.48 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0592 | 0.1082 | 0.1957 | 0.3798 |
| B | 0.0443 | 0.0609 | 0.1067 | 0.1986 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0051 | 0.0113 | 0.0222 | 0.0432 |
| B | 0.0066 | 0.0088 | 0.0131 | 0.0251 |

Delays at 25°C, 1.8V, Typical Process

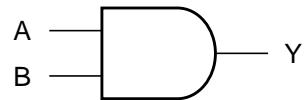
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A → S↑ | 0.1263 | 0.0830 | 0.0740 | 0.0717 | 6.6779 | 2.6588 | 1.2905 | 0.6416 |
| A → S↓ | 0.1348 | 0.0893 | 0.0823 | 0.0788 | 4.1076 | 1.7289 | 0.8455 | 0.4183 |
| B → S↑ | 0.0616 | 0.0545 | 0.0504 | 0.0471 | 6.6079 | 2.6445 | 1.2800 | 0.6358 |
| B → S↓ | 0.0773 | 0.0728 | 0.0670 | 0.0626 | 3.8779 | 1.6477 | 0.8092 | 0.4017 |
| A → CO↑ | 0.0783 | 0.0895 | 0.0808 | 0.0794 | 5.8909 | 4.2073 | 2.0827 | 1.0416 |
| A → CO↓ | 0.0969 | 0.1191 | 0.1058 | 0.1033 | 3.4777 | 2.7061 | 1.2961 | 0.6483 |
| B → CO↑ | 0.0751 | 0.0901 | 0.0773 | 0.0756 | 5.8916 | 4.2075 | 2.0821 | 1.0416 |
| B → CO↓ | 0.0872 | 0.1138 | 0.0974 | 0.0934 | 3.4730 | 2.7029 | 1.2951 | 0.6478 |

Cell Description

The AND2 cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B)$$

Logic Symbol



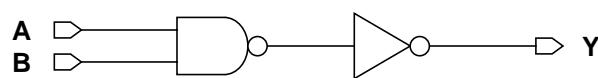
Functions

| A | B | Y |
|---|---|---|
| 0 | x | 0 |
| x | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| AND2XL | 5.04 | 2.64 |
| AND2X1 | 5.04 | 2.64 |
| AND2X2 | 5.04 | 2.64 |
| AND2X4 | 5.04 | 3.30 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0188 | 0.0213 | 0.0327 | 0.0616 |
| B | 0.0214 | 0.0245 | 0.0371 | 0.0737 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0023 | 0.0022 | 0.0035 | 0.0061 |
| B | 0.0024 | 0.0023 | 0.0035 | 0.0066 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0801 | 0.0843 | 0.0750 | 0.0709 |
| A → Y↓ | 0.0908 | 0.1087 | 0.0913 | 0.1006 |
| B → Y↑ | 0.0885 | 0.0930 | 0.0797 | 0.0766 |
| B → Y↓ | 0.1028 | 0.1224 | 0.1027 | 0.1156 |

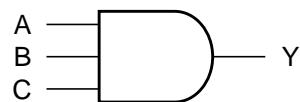
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8983 | 4.2091 | 2.2062 | 1.0356 |
| A → Y↓ | 3.4810 | 2.5429 | 1.2926 | 0.6810 |
| B → Y↑ | 5.8983 | 4.2089 | 2.2061 | 1.0355 |
| B → Y↓ | 3.4874 | 2.5463 | 1.2941 | 0.6819 |

Cell Description

The AND3 cell provides the logical AND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C)$$

Logic Symbol



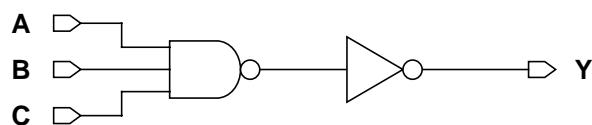
Functions

| A | B | C | Y |
|---|---|---|---|
| 0 | x | x | 0 |
| x | 0 | x | 0 |
| x | x | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| AND3XL | 5.04 | 3.30 |
| AND3X1 | 5.04 | 3.30 |
| AND3X2 | 5.04 | 3.30 |
| AND3X4 | 5.04 | 3.96 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0213 | 0.0237 | 0.0363 | 0.0649 |
| B | 0.0253 | 0.0268 | 0.0425 | 0.0757 |
| C | 0.0284 | 0.0305 | 0.0496 | 0.0844 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0029 | 0.0027 | 0.0038 | 0.0062 |
| B | 0.0028 | 0.0026 | 0.0038 | 0.0063 |
| C | 0.0028 | 0.0026 | 0.0042 | 0.0066 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.1032 | 0.1142 | 0.0924 | 0.0966 |
| A → Y↓ | 0.1115 | 0.1274 | 0.1069 | 0.0965 |
| B → Y↑ | 0.1117 | 0.1229 | 0.1029 | 0.1045 |
| B → Y↓ | 0.1256 | 0.1414 | 0.1204 | 0.1076 |
| C → Y↑ | 0.1164 | 0.1281 | 0.1088 | 0.1096 |
| C → Y↓ | 0.1380 | 0.1542 | 0.1339 | 0.1181 |

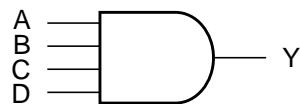
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.9128 | 4.2191 | 2.0870 | 1.0560 |
| A → Y↓ | 3.2660 | 2.7152 | 1.2983 | 0.6380 |
| B → Y↑ | 5.9130 | 4.2192 | 2.0870 | 1.0560 |
| B → Y↓ | 3.2751 | 2.7190 | 1.3000 | 0.6388 |
| C → Y↑ | 5.9130 | 4.2192 | 2.0870 | 1.0560 |
| C → Y↓ | 3.2877 | 2.7243 | 1.3025 | 0.6399 |

Cell Description

The AND4 cell provides the logical AND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C \bullet D)$$

Logic Symbol



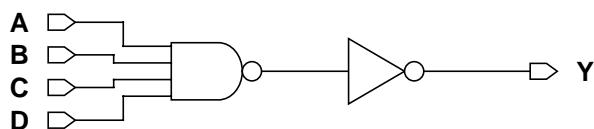
Functions

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | x | x | x | 0 |
| x | 0 | x | x | 0 |
| x | x | 0 | x | 0 |
| x | x | x | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| AND4XL | 5.04 | 3.96 |
| AND4X1 | 5.04 | 3.96 |
| AND4X2 | 5.04 | 3.96 |
| AND4X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0203 | 0.0238 | 0.0394 | 0.0709 |
| B | 0.0238 | 0.0271 | 0.0451 | 0.0838 |
| C | 0.0283 | 0.0302 | 0.0519 | 0.0967 |
| D | 0.0316 | 0.0341 | 0.0581 | 0.1106 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0028 | 0.0026 | 0.0039 | 0.0071 |
| B | 0.0027 | 0.0024 | 0.0038 | 0.0074 |
| C | 0.0029 | 0.0026 | 0.0039 | 0.0081 |
| D | 0.0029 | 0.0027 | 0.0041 | 0.0088 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.1055 | 0.1268 | 0.1107 | 0.1003 |
| A → Y↓ | 0.1072 | 0.1236 | 0.1108 | 0.1113 |
| B → Y↑ | 0.1195 | 0.1411 | 0.1219 | 0.1142 |
| B → Y↓ | 0.1225 | 0.1380 | 0.1251 | 0.1273 |
| C → Y↑ | 0.1295 | 0.1508 | 0.1300 | 0.1228 |
| C → Y↓ | 0.1378 | 0.1523 | 0.1383 | 0.1422 |
| D → Y↑ | 0.1347 | 0.1568 | 0.1354 | 0.1288 |
| D → Y↓ | 0.1499 | 0.1647 | 0.1506 | 0.1564 |

Delays at 25°C, 1.8V, Typical Process

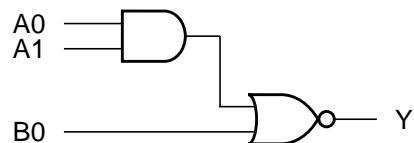
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.9309 | 4.2318 | 2.1652 | 1.0640 |
| A → Y↓ | 3.5089 | 2.5548 | 1.2991 | 0.6506 |
| B → Y↑ | 5.9311 | 4.2318 | 2.1652 | 1.0640 |
| B → Y↓ | 3.5182 | 2.5588 | 1.3011 | 0.6518 |
| C → Y↑ | 5.9311 | 4.2318 | 2.1652 | 1.0640 |
| C → Y↓ | 3.5315 | 2.5645 | 1.3038 | 0.6533 |
| D → Y↑ | 5.9293 | 4.2313 | 2.1652 | 1.0640 |
| D → Y↓ | 3.5475 | 2.5716 | 1.3075 | 0.6554 |

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0}$$

Logic Symbol



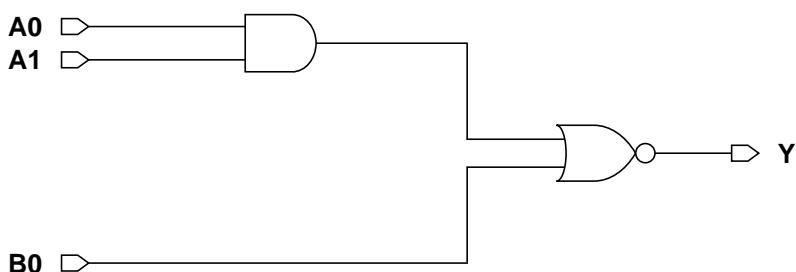
Functions

| A0 | A1 | B0 | Y |
|----|----|----|---|
| 0 | x | 0 | 1 |
| x | 0 | 0 | 1 |
| x | x | 1 | 0 |
| 1 | 1 | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI21XL | 5.04 | 2.64 |
| AOI21X1 | 5.04 | 2.64 |
| AOI21X2 | 5.04 | 4.62 |
| AOI21X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0153 | 0.0221 | 0.0454 | 0.0838 |
| A1 | 0.0192 | 0.0278 | 0.0555 | 0.1049 |
| B0 | 0.0154 | 0.0216 | 0.0426 | 0.0796 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0034 | 0.0050 | 0.0100 | 0.0183 |
| A1 | 0.0034 | 0.0048 | 0.0093 | 0.0183 |
| B0 | 0.0035 | 0.0047 | 0.0086 | 0.0160 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0608 | 0.0572 | 0.0565 | 0.0532 | 8.7152 | 6.0744 | 3.0379 | 1.5644 |
| A0 → Y↓ | 0.0332 | 0.0331 | 0.0325 | 0.0305 | 4.1470 | 2.9440 | 1.4723 | 0.7432 |
| A1 → Y↑ | 0.0749 | 0.0703 | 0.0690 | 0.0670 | 8.7016 | 6.0682 | 3.0343 | 1.5630 |
| A1 → Y↓ | 0.0394 | 0.0386 | 0.0377 | 0.0361 | 4.1487 | 2.9451 | 1.4729 | 0.7435 |
| B0 → Y↑ | 0.0523 | 0.0519 | 0.0491 | 0.0487 | 8.7153 | 6.0744 | 3.0367 | 1.5641 |
| B0 → Y↓ | 0.0213 | 0.0218 | 0.0200 | 0.0190 | 3.4175 | 2.5026 | 1.2795 | 0.6398 |

Cell Description

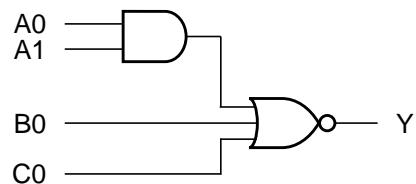
The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1)} + B_0 + C_0$$

Functions

| A0 | A1 | B0 | C0 | Y |
|----|----|----|----|---|
| 0 | x | 0 | 0 | 1 |
| x | 0 | 0 | 0 | 1 |
| x | x | x | 1 | 0 |
| x | x | 1 | x | 0 |
| 1 | 1 | x | x | 0 |

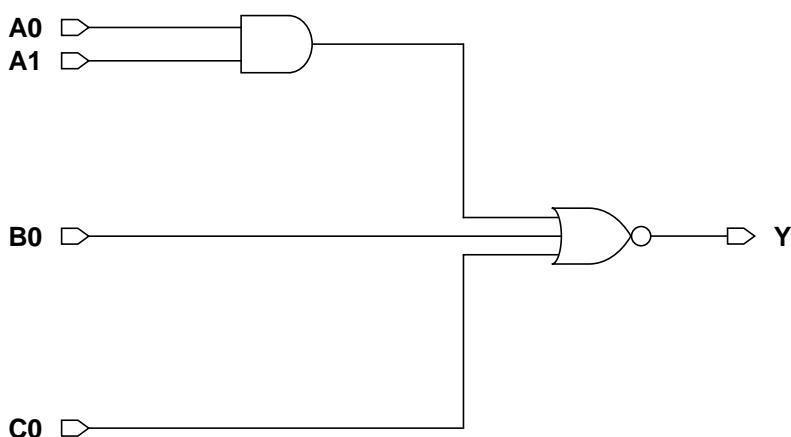
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI211XL | 5.04 | 3.30 |
| AOI211X1 | 5.04 | 3.30 |
| AOI211X2 | 5.04 | 5.94 |
| AOI211X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0230 | 0.0330 | 0.0680 | 0.0862 |
| A1 | 0.0271 | 0.0394 | 0.0785 | 0.0912 |
| B0 | 0.0182 | 0.0258 | 0.0518 | 0.0804 |
| C0 | 0.0219 | 0.0313 | 0.0638 | 0.0868 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0037 | 0.0052 | 0.0105 | 0.0035 |
| A1 | 0.0037 | 0.0051 | 0.0099 | 0.0034 |
| B0 | 0.0038 | 0.0053 | 0.0093 | 0.0037 |
| C0 | 0.0035 | 0.0047 | 0.0098 | 0.0034 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0977 | 0.0966 | 0.0965 | 0.2647 | 11.1188 | 7.6961 | 3.8671 | 1.0402 |
| A0 → Y↓ | 0.0427 | 0.0453 | 0.0449 | 0.1727 | 4.1958 | 2.9703 | 1.4848 | 0.6464 |
| A1 → Y↑ | 0.1156 | 0.1135 | 0.1128 | 0.2850 | 11.1023 | 7.6884 | 3.8630 | 1.0402 |
| A1 → Y↓ | 0.0490 | 0.0512 | 0.0502 | 0.1785 | 4.2000 | 2.9735 | 1.4871 | 0.6464 |
| B0 → Y↑ | 0.0712 | 0.0703 | 0.0673 | 0.2428 | 11.1210 | 7.6967 | 3.8662 | 1.0402 |
| B0 → Y↓ | 0.0249 | 0.0253 | 0.0244 | 0.1427 | 3.4191 | 2.5063 | 1.2796 | 0.6462 |
| C0 → Y↑ | 0.0959 | 0.0947 | 0.0958 | 0.2673 | 11.1080 | 7.6908 | 3.8649 | 1.0402 |
| C0 → Y↓ | 0.0317 | 0.0334 | 0.0342 | 0.1513 | 3.4358 | 2.5113 | 1.2823 | 0.6461 |

Cell Description

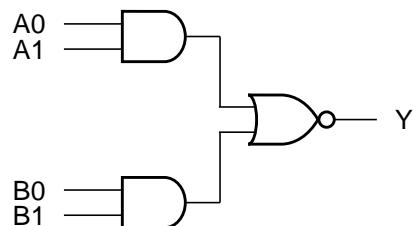
The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Functions

| A0 | A1 | B0 | B1 | Y |
|----|----|----|----|---|
| 0 | x | 0 | x | 1 |
| 0 | x | x | 0 | 1 |
| x | 0 | 0 | x | 1 |
| x | 0 | x | 0 | 1 |
| x | x | 1 | 1 | 0 |
| 1 | 1 | x | x | 0 |

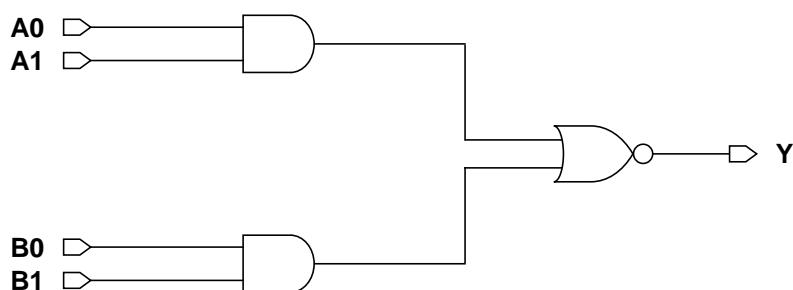
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI22XL | 5.04 | 3.30 |
| AOI22X1 | 5.04 | 3.30 |
| AOI22X2 | 5.04 | 5.94 |
| AOI22X4 | 5.04 | 9.24 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0177 | 0.0242 | 0.0470 | 0.0924 |
| A1 | 0.0217 | 0.0298 | 0.0584 | 0.1148 |
| B0 | 0.0232 | 0.0316 | 0.0621 | 0.1264 |
| B1 | 0.0271 | 0.0374 | 0.0734 | 0.1452 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0037 | 0.0050 | 0.0095 | 0.0185 |
| A1 | 0.0037 | 0.0050 | 0.0102 | 0.0190 |
| B0 | 0.0035 | 0.0047 | 0.0092 | 0.0182 |
| B1 | 0.0034 | 0.0047 | 0.0095 | 0.0183 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0604 | 0.0588 | 0.0584 | 0.0592 | 8.7181 | 6.0757 | 3.0378 | 1.5504 |
| A0 → Y↓ | 0.0280 | 0.0267 | 0.0263 | 0.0259 | 4.1069 | 2.9313 | 1.4656 | 0.7401 |
| A1 → Y↑ | 0.0749 | 0.0728 | 0.0728 | 0.0708 | 8.7091 | 6.0715 | 3.0357 | 1.5097 |
| A1 → Y↓ | 0.0337 | 0.0330 | 0.0328 | 0.0322 | 4.1223 | 2.9361 | 1.4681 | 0.7413 |
| B0 → Y↑ | 0.0939 | 0.0860 | 0.0834 | 0.0819 | 8.7130 | 6.0732 | 3.0366 | 1.5103 |
| B0 → Y↓ | 0.0490 | 0.0464 | 0.0450 | 0.0438 | 4.1416 | 2.9417 | 1.4700 | 0.7431 |
| B1 → Y↑ | 0.1070 | 0.0992 | 0.0968 | 0.0949 | 8.7025 | 6.0685 | 3.0343 | 1.5092 |
| B1 → Y↓ | 0.0545 | 0.0524 | 0.0509 | 0.0505 | 4.1490 | 2.9455 | 1.4720 | 0.7432 |

Cell Description

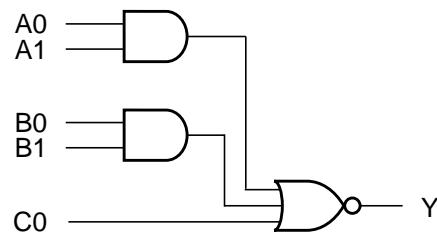
The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1) + (B_0 \bullet B_1) + C_0}$$

Functions

| A0 | A1 | B0 | B1 | C0 | Y |
|----|----|----|----|----|---|
| 0 | x | 0 | x | 0 | 1 |
| 0 | x | x | 0 | 0 | 1 |
| x | 0 | 0 | x | 0 | 1 |
| x | 0 | x | 0 | 0 | 1 |
| x | x | x | x | 1 | 0 |
| x | x | 1 | 1 | x | 0 |
| 1 | 1 | x | x | x | 0 |

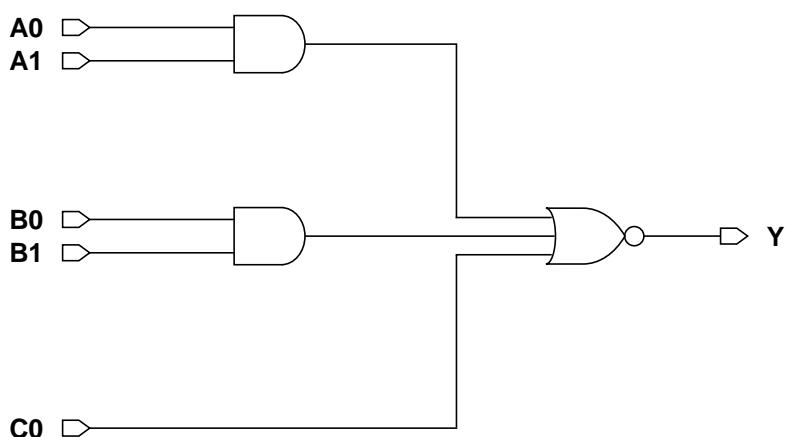
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI221XL | 5.04 | 4.62 |
| AOI221X1 | 5.04 | 4.62 |
| AOI221X2 | 5.04 | 7.92 |
| AOI221X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0246 | 0.0338 | 0.0649 | 0.0835 |
| A1 | 0.0287 | 0.0394 | 0.0765 | 0.0874 |
| B0 | 0.0314 | 0.0435 | 0.0829 | 0.0887 |
| B1 | 0.0353 | 0.0483 | 0.0945 | 0.0930 |
| C0 | 0.0236 | 0.0321 | 0.0619 | 0.0830 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0039 | 0.0053 | 0.0100 | 0.0035 |
| A1 | 0.0039 | 0.0053 | 0.0103 | 0.0034 |
| B0 | 0.0039 | 0.0052 | 0.0100 | 0.0035 |
| B1 | 0.0038 | 0.0050 | 0.0102 | 0.0034 |
| C0 | 0.0037 | 0.0051 | 0.0095 | 0.0036 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.1176 | 0.1102 | 0.1050 | 0.2837 | 10.8961 | 7.7344 | 3.8674 | 1.0766 |
| A0 → Y↓ | 0.0456 | 0.0436 | 0.0411 | 0.1728 | 4.1498 | 2.9451 | 1.4732 | 0.6461 |
| A1 → Y↑ | 0.1353 | 0.1271 | 0.1216 | 0.3031 | 10.8833 | 7.7279 | 3.8639 | 1.0765 |
| A1 → Y↓ | 0.0519 | 0.0496 | 0.0470 | 0.1794 | 4.1576 | 2.9489 | 1.4750 | 0.6461 |
| B0 → Y↑ | 0.1415 | 0.1319 | 0.1271 | 0.3069 | 10.8956 | 7.7339 | 3.8673 | 1.0766 |
| B0 → Y↓ | 0.0537 | 0.0529 | 0.0503 | 0.1858 | 4.2564 | 2.9941 | 1.4983 | 0.6462 |
| B1 → Y↑ | 0.1583 | 0.1482 | 0.1440 | 0.3265 | 10.8814 | 7.7272 | 3.8639 | 1.0766 |
| B1 → Y↓ | 0.0598 | 0.0587 | 0.0565 | 0.1914 | 4.2584 | 2.9960 | 1.4995 | 0.6462 |
| C0 → Y↑ | 0.0842 | 0.0847 | 0.0789 | 0.2559 | 10.8942 | 7.7335 | 3.8668 | 1.0765 |
| C0 → Y↓ | 0.0272 | 0.0266 | 0.0250 | 0.1454 | 3.4277 | 2.5104 | 1.2822 | 0.6458 |

Cell Description

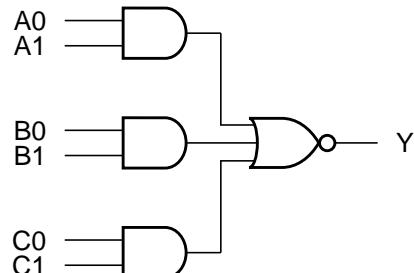
The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1)} + (B_0 \bullet B_1) + (C_0 \bullet C_1)$$

Functions

| A0 | A1 | B0 | B1 | C0 | C1 | Y |
|----|----|----|----|----|----|---|
| 0 | x | 0 | x | 0 | x | 1 |
| 0 | x | 0 | x | x | 0 | 1 |
| 0 | x | x | 0 | 0 | x | 1 |
| 0 | x | x | 0 | x | 0 | 1 |
| x | 0 | 0 | x | 0 | x | 1 |
| x | 0 | 0 | x | x | 0 | 1 |
| x | 0 | x | 0 | 0 | x | 1 |
| x | 0 | x | 0 | x | 0 | 1 |
| x | x | x | x | 1 | 1 | 0 |
| x | x | 1 | 1 | x | x | 0 |
| 1 | 1 | x | x | x | x | 0 |

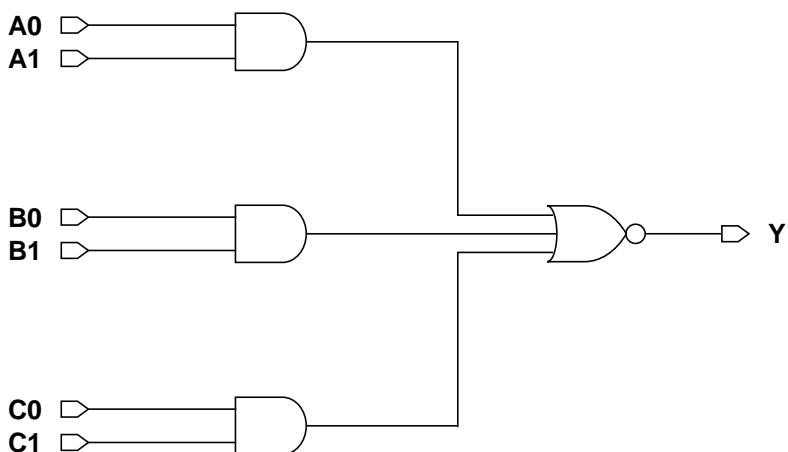
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI222XL | 5.04 | 5.28 |
| AOI222X1 | 5.04 | 5.28 |
| AOI222X2 | 5.04 | 9.24 |
| AOI222X4 | 5.04 | 7.92 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0262 | 0.0353 | 0.0685 | 0.0855 |
| A1 | 0.0303 | 0.0410 | 0.0795 | 0.0909 |
| B0 | 0.0320 | 0.0442 | 0.0853 | 0.0909 |
| B1 | 0.0361 | 0.0497 | 0.0965 | 0.0953 |
| C0 | 0.0382 | 0.0532 | 0.1036 | 0.0970 |
| C1 | 0.0423 | 0.0588 | 0.1164 | 0.1011 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0039 | 0.0054 | 0.0106 | 0.0037 |
| A1 | 0.0040 | 0.0055 | 0.0110 | 0.0038 |
| B0 | 0.0038 | 0.0052 | 0.0100 | 0.0035 |
| B1 | 0.0037 | 0.0051 | 0.0104 | 0.0033 |
| C0 | 0.0037 | 0.0051 | 0.0100 | 0.0034 |
| C1 | 0.0037 | 0.0051 | 0.0102 | 0.0034 |

Delays at 25°C, 1.8V, Typical Process

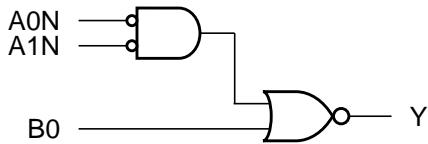
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0971 | 0.0921 | 0.0912 | 0.2582 | 11.3559 | 7.7354 | 3.8680 | 1.0581 |
| A0 → Y↓ | 0.0349 | 0.0338 | 0.0331 | 0.1681 | 4.1237 | 2.9363 | 1.4683 | 0.6464 |
| A1 → Y↑ | 0.1166 | 0.1108 | 0.1085 | 0.2799 | 11.3468 | 7.7310 | 3.8654 | 1.0580 |
| A1 → Y↓ | 0.0417 | 0.0407 | 0.0394 | 0.1733 | 4.1330 | 2.9408 | 1.4706 | 0.6464 |
| B0 → Y↑ | 0.1673 | 0.1509 | 0.1446 | 0.3295 | 11.3524 | 7.7333 | 3.8666 | 1.0581 |
| B0 → Y↓ | 0.0585 | 0.0556 | 0.0541 | 0.1925 | 4.1516 | 2.9471 | 1.4711 | 0.6465 |
| B1 → Y↑ | 0.1857 | 0.1670 | 0.1619 | 0.3488 | 11.3407 | 7.7278 | 3.8641 | 1.0580 |
| B1 → Y↓ | 0.0657 | 0.0622 | 0.0604 | 0.1994 | 4.1525 | 2.9474 | 1.4730 | 0.6465 |
| C0 → Y↑ | 0.1910 | 0.1728 | 0.1673 | 0.3525 | 11.3522 | 7.7335 | 3.8666 | 1.0580 |
| C0 → Y↓ | 0.0738 | 0.0724 | 0.0704 | 0.2072 | 4.2195 | 2.9804 | 1.4898 | 0.6465 |
| C1 → Y↑ | 0.2083 | 0.1897 | 0.1839 | 0.3715 | 11.3398 | 7.7280 | 3.8638 | 1.0580 |
| C1 → Y↓ | 0.0805 | 0.0792 | 0.0773 | 0.2137 | 4.2197 | 2.9805 | 1.4899 | 0.6465 |

Cell Description

The AOI2BB1 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + B0}$$

Logic Symbol



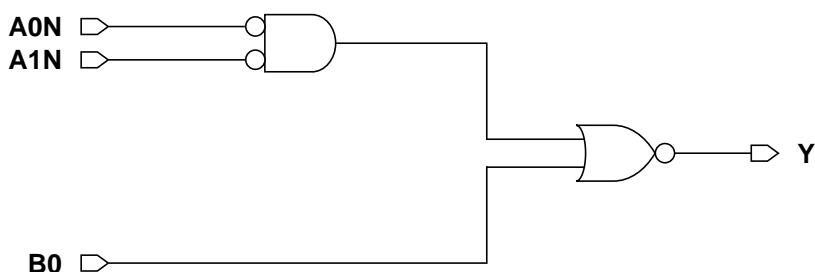
Functions

| A0N | A1N | B0 | Y |
|-----|-----|----|---|
| 1 | x | 0 | 1 |
| x | 1 | 0 | 1 |
| x | x | 1 | 0 |
| 0 | 0 | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI2BB1XL | 5.04 | 3.30 |
| AOI2BB1X1 | 5.04 | 3.30 |
| AOI2BB1X2 | 5.04 | 4.62 |
| AOI2BB1X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0222 | 0.0261 | 0.0420 | 0.0832 |
| A1N | 0.0248 | 0.0283 | 0.0492 | 0.0922 |
| B0 | 0.0144 | 0.0194 | 0.0382 | 0.0724 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0028 | 0.0027 | 0.0045 | 0.0083 |
| A1N | 0.0026 | 0.0027 | 0.0047 | 0.0084 |
| B0 | 0.0034 | 0.0044 | 0.0089 | 0.0162 |

Delays at 25°C, 1.8V, Typical Process

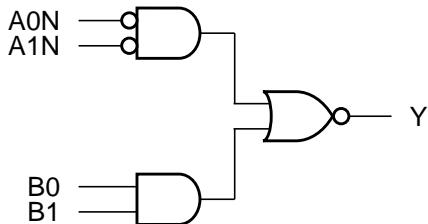
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0N → Y↑ | 0.0813 | 0.0805 | 0.0763 | 0.0749 | 8.7279 | 6.1818 | 3.0377 | 1.5110 |
| A0N → Y↓ | 0.1357 | 0.1527 | 0.1305 | 0.1273 | 3.3175 | 2.6547 | 1.3078 | 0.6532 |
| A1N → Y↑ | 0.0870 | 0.0873 | 0.0821 | 0.0830 | 8.7303 | 6.1830 | 3.0382 | 1.5112 |
| A1N → Y↓ | 0.1466 | 0.1658 | 0.1434 | 0.1391 | 3.3175 | 2.6548 | 1.3078 | 0.6532 |
| B0 → Y↑ | 0.0504 | 0.0473 | 0.0456 | 0.0437 | 8.7061 | 6.1737 | 3.0355 | 1.5094 |
| B0 → Y↓ | 0.0232 | 0.0253 | 0.0246 | 0.0238 | 3.1844 | 2.5905 | 1.2824 | 0.6412 |

Cell Description

The AOI2BB2 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and one AND group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = (\overline{A0N} \bullet \overline{A1N}) + (B0 \bullet B1)$$

Logic Symbol



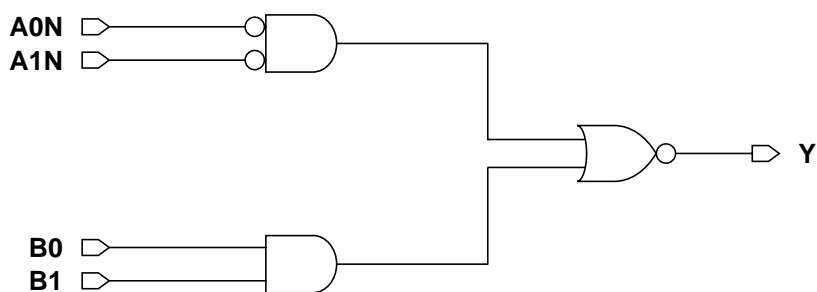
Functions

| A0N | A1N | B0 | B1 | Y |
|-----|-----|----|----|---|
| 1 | x | 0 | x | 1 |
| 1 | x | x | 0 | 1 |
| x | 1 | 0 | x | 1 |
| x | 1 | x | 0 | 1 |
| x | x | 1 | 1 | 0 |
| 0 | 0 | x | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI2BB2XL | 5.04 | 4.62 |
| AOI2BB2X1 | 5.04 | 4.62 |
| AOI2BB2X2 | 5.04 | 5.94 |
| AOI2BB2X4 | 5.04 | 9.90 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0226 | 0.0255 | 0.0421 | 0.0792 |
| A1N | 0.0248 | 0.0275 | 0.0481 | 0.0876 |
| B0 | 0.0166 | 0.0223 | 0.0440 | 0.0869 |
| B1 | 0.0205 | 0.0283 | 0.0562 | 0.1099 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0029 | 0.0027 | 0.0045 | 0.0080 |
| A1N | 0.0025 | 0.0024 | 0.0044 | 0.0085 |
| B0 | 0.0036 | 0.0048 | 0.0098 | 0.0180 |
| B1 | 0.0035 | 0.0048 | 0.0102 | 0.0187 |

Delays at 25°C, 1.8V, Typical Process

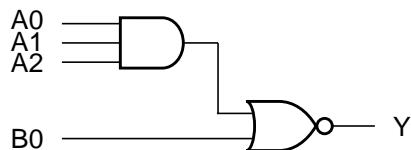
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0N → Y↑ | 0.0762 | 0.0747 | 0.0733 | 0.0717 | 6.5291 | 4.5472 | 2.2728 | 1.1305 |
| A0N → Y↓ | 0.1438 | 0.1511 | 0.1325 | 0.1225 | 3.5682 | 2.5715 | 1.3496 | 0.6516 |
| A1N → Y↑ | 0.0786 | 0.0774 | 0.0812 | 0.0791 | 6.5318 | 4.5486 | 2.2734 | 1.1299 |
| A1N → Y↓ | 0.1524 | 0.1603 | 0.1440 | 0.1350 | 3.5679 | 2.5714 | 1.3496 | 0.6516 |
| B0 → Y↑ | 0.0625 | 0.0589 | 0.0560 | 0.0548 | 8.7168 | 6.0744 | 3.0376 | 1.5106 |
| B0 → Y↓ | 0.0338 | 0.0331 | 0.0314 | 0.0314 | 4.1411 | 2.9446 | 1.4716 | 0.7432 |
| B1 → Y↑ | 0.0761 | 0.0726 | 0.0694 | 0.0683 | 8.7021 | 6.0684 | 3.0344 | 1.5092 |
| B1 → Y↓ | 0.0395 | 0.0392 | 0.0373 | 0.0374 | 4.1419 | 2.9453 | 1.4719 | 0.7435 |

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1 \bullet A_2)} + B_0$$

Logic Symbol



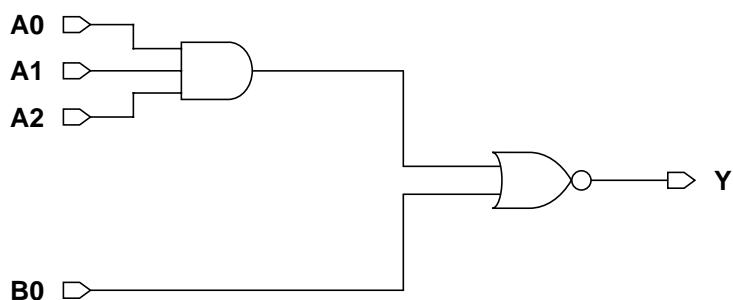
Functions

| A0 | A1 | A2 | B0 | Y |
|----|----|----|----|---|
| 0 | x | x | 0 | 1 |
| x | 0 | x | 0 | 1 |
| x | x | 0 | 0 | 1 |
| x | x | x | 1 | 0 |
| 1 | 1 | 1 | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI31XL | 5.04 | 3.30 |
| AOI31X1 | 5.04 | 3.30 |
| AOI31X2 | 5.04 | 5.94 |
| AOI31X4 | 5.04 | 5.94 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0169 | 0.0229 | 0.0501 | 0.0742 |
| A1 | 0.0219 | 0.0306 | 0.0612 | 0.0794 |
| A2 | 0.0264 | 0.0371 | 0.0761 | 0.0854 |
| B0 | 0.0213 | 0.0298 | 0.0598 | 0.0806 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0038 | 0.0050 | 0.0113 | 0.0036 |
| A1 | 0.0037 | 0.0051 | 0.0105 | 0.0035 |
| A2 | 0.0036 | 0.0049 | 0.0101 | 0.0034 |
| B0 | 0.0035 | 0.0047 | 0.0086 | 0.0035 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0659 | 0.0626 | 0.0657 | 0.2077 | 8.7217 | 6.0773 | 3.0392 | 1.0401 |
| A0 → Y↓ | 0.0389 | 0.0374 | 0.0393 | 0.1721 | 4.7741 | 3.3005 | 1.6516 | 0.6464 |
| A1 → Y↑ | 0.0829 | 0.0802 | 0.0812 | 0.2268 | 8.7076 | 6.0714 | 3.0359 | 1.0402 |
| A1 → Y↓ | 0.0483 | 0.0470 | 0.0472 | 0.1818 | 4.7752 | 3.3029 | 1.6534 | 0.6464 |
| A2 → Y↑ | 0.0974 | 0.0947 | 0.0965 | 0.2439 | 8.7145 | 6.0745 | 3.0376 | 1.0401 |
| A2 → Y↓ | 0.0522 | 0.0510 | 0.0517 | 0.1857 | 4.7748 | 3.3025 | 1.6533 | 0.6464 |
| B0 → Y↑ | 0.0731 | 0.0722 | 0.0695 | 0.2221 | 8.7278 | 6.0806 | 3.0402 | 1.0401 |
| B0 → Y↓ | 0.0215 | 0.0213 | 0.0207 | 0.1434 | 3.4330 | 2.5162 | 1.2846 | 0.6461 |

Cell Description

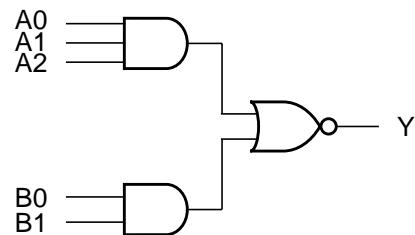
The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1 \bullet A_2) + (B_0 \bullet B_1)}$$

Functions

| A0 | A1 | A2 | B0 | B1 | Y |
|----|----|----|----|----|---|
| 0 | x | x | 0 | x | 1 |
| 0 | x | x | x | 0 | 1 |
| x | 0 | x | 0 | x | 1 |
| x | 0 | x | x | 0 | 1 |
| x | x | 0 | 0 | x | 1 |
| x | x | 0 | x | 0 | 1 |
| x | x | x | 1 | 1 | 0 |
| 1 | 1 | 1 | x | x | 0 |

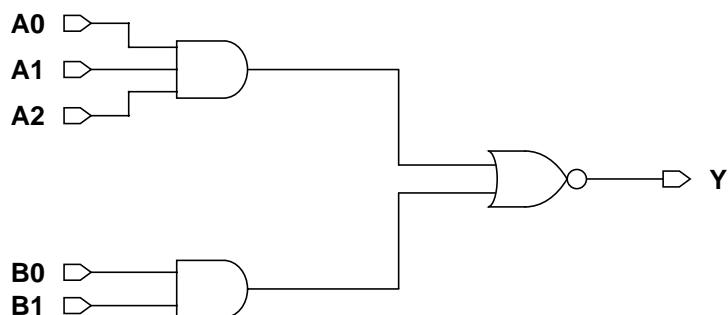
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI32XL | 5.04 | 4.62 |
| AOI32X1 | 5.04 | 4.62 |
| AOI32X2 | 5.04 | 7.26 |
| AOI32X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0249 | 0.0336 | 0.0667 | 0.0805 |
| A1 | 0.0298 | 0.0405 | 0.0804 | 0.0882 |
| A2 | 0.0342 | 0.0469 | 0.0940 | 0.0932 |
| B0 | 0.0237 | 0.0327 | 0.0644 | 0.0834 |
| B1 | 0.0278 | 0.0381 | 0.0753 | 0.0867 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0038 | 0.0051 | 0.0099 | 0.0035 |
| A1 | 0.0038 | 0.0050 | 0.0104 | 0.0035 |
| A2 | 0.0036 | 0.0049 | 0.0107 | 0.0033 |
| B0 | 0.0038 | 0.0049 | 0.0096 | 0.0036 |
| B1 | 0.0039 | 0.0049 | 0.0101 | 0.0036 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0983 | 0.0938 | 0.0918 | 0.2397 | 8.7164 | 6.0755 | 3.0380 | 1.0401 |
| A0 → Y↓ | 0.0557 | 0.0536 | 0.0532 | 0.1896 | 4.7730 | 3.3022 | 1.6492 | 0.6309 |
| A1 → Y↑ | 0.1155 | 0.1108 | 0.1088 | 0.2594 | 8.7065 | 6.0709 | 3.0355 | 1.0401 |
| A1 → Y↓ | 0.0662 | 0.0639 | 0.0626 | 0.2001 | 4.7733 | 3.3024 | 1.6511 | 0.6309 |
| A2 → Y↑ | 0.1301 | 0.1257 | 0.1244 | 0.2762 | 8.7116 | 6.0733 | 3.0368 | 1.0401 |
| A2 → Y↓ | 0.0700 | 0.0680 | 0.0673 | 0.2039 | 4.7732 | 3.3023 | 1.6512 | 0.6309 |
| B0 → Y↑ | 0.0825 | 0.0801 | 0.0787 | 0.2276 | 8.7290 | 6.0810 | 3.0408 | 1.0401 |
| B0 → Y↓ | 0.0290 | 0.0277 | 0.0269 | 0.1626 | 4.1290 | 2.9442 | 1.4721 | 0.6308 |
| B1 → Y↑ | 0.0977 | 0.0941 | 0.0927 | 0.2441 | 8.7198 | 6.0765 | 3.0384 | 1.0401 |
| B1 → Y↓ | 0.0350 | 0.0341 | 0.0333 | 0.1674 | 4.1452 | 2.9488 | 1.4745 | 0.6308 |

Cell Description

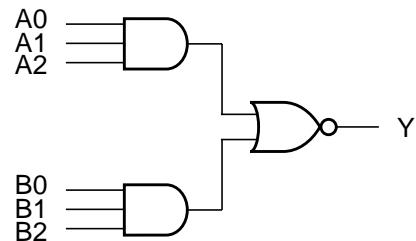
The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 \bullet A_1 \bullet A_2) + (B_0 \bullet B_1 \bullet B_2)}$$

Functions

| A0 | A1 | A2 | B0 | B1 | B2 | Y |
|----|----|----|----|----|----|---|
| 0 | x | x | 0 | x | x | 1 |
| 0 | x | x | x | 0 | x | 1 |
| 0 | x | x | x | x | 0 | 1 |
| x | 0 | x | 0 | x | x | 1 |
| x | 0 | x | x | 0 | x | 1 |
| x | 0 | x | x | x | 0 | 1 |
| x | x | 0 | 0 | x | x | 1 |
| x | x | 0 | x | 0 | x | 1 |
| x | x | x | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | x | x | x | 0 |

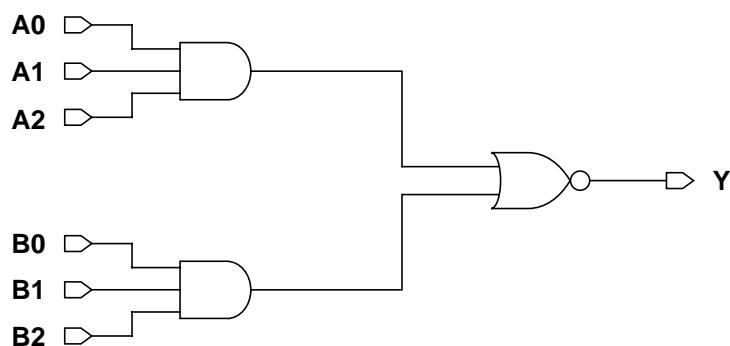
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AOI33XL | 5.04 | 5.28 |
| AOI33X1 | 5.04 | 5.28 |
| AOI33X2 | 5.04 | 8.58 |
| AOI33X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0253 | 0.0359 | 0.0706 | 0.0847 |
| A1 | 0.0299 | 0.0424 | 0.0834 | 0.0897 |
| A2 | 0.0344 | 0.0487 | 0.0968 | 0.0954 |
| B0 | 0.0322 | 0.0459 | 0.0915 | 0.0917 |
| B1 | 0.0370 | 0.0528 | 0.1046 | 0.0966 |
| B2 | 0.0413 | 0.0591 | 0.1183 | 0.1014 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0038 | 0.0052 | 0.0102 | 0.0036 |
| A1 | 0.0038 | 0.0053 | 0.0108 | 0.0036 |
| A2 | 0.0039 | 0.0053 | 0.0116 | 0.0038 |
| B0 | 0.0037 | 0.0051 | 0.0098 | 0.0034 |
| B1 | 0.0037 | 0.0051 | 0.0103 | 0.0035 |
| B2 | 0.0036 | 0.0050 | 0.0109 | 0.0033 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0933 | 0.0924 | 0.0884 | 0.2405 | 8.7277 | 6.0810 | 3.0406 | 1.0402 |
| A0 → Y↓ | 0.0373 | 0.0361 | 0.0348 | 0.1836 | 4.7554 | 3.2992 | 1.6844 | 0.6466 |
| A1 → Y↑ | 0.1108 | 0.1100 | 0.1050 | 0.2600 | 8.7188 | 6.0769 | 3.0383 | 1.0401 |
| A1 → Y↓ | 0.0466 | 0.0461 | 0.0445 | 0.1918 | 4.7705 | 3.3035 | 1.6863 | 0.6466 |
| A2 → Y↑ | 0.1273 | 0.1256 | 0.1227 | 0.2799 | 8.7226 | 6.0784 | 3.0396 | 1.0401 |
| A2 → Y↓ | 0.0514 | 0.0504 | 0.0501 | 0.1974 | 4.7718 | 3.3040 | 1.6868 | 0.6466 |
| B0 → Y↑ | 0.1303 | 0.1298 | 0.1263 | 0.2808 | 8.7244 | 6.0795 | 3.0398 | 1.0401 |
| B0 → Y↓ | 0.0703 | 0.0701 | 0.0696 | 0.2114 | 4.7653 | 3.3000 | 1.6850 | 0.6467 |
| B1 → Y↑ | 0.1477 | 0.1469 | 0.1428 | 0.3003 | 8.7152 | 6.0750 | 3.0376 | 1.0401 |
| B1 → Y↓ | 0.0810 | 0.0805 | 0.0798 | 0.2220 | 4.7654 | 3.3002 | 1.6851 | 0.6468 |
| B2 → Y↑ | 0.1627 | 0.1619 | 0.1589 | 0.3171 | 8.7183 | 6.0766 | 3.0384 | 1.0401 |
| B2 → Y↓ | 0.0848 | 0.0845 | 0.0852 | 0.2257 | 4.7655 | 3.3002 | 1.6851 | 0.6468 |

Cell Description

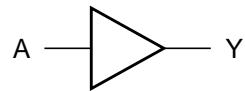
The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| BUFXL | 5.04 | 2.64 |
| BUFX1 | 5.04 | 2.64 |
| BUFX2 | 5.04 | 2.64 |
| BUFX3 | 5.04 | 2.64 |
| BUFX4 | 5.04 | 3.30 |
| BUFX8 | 5.04 | 5.94 |
| BUFX12 | 5.04 | 6.60 |
| BUFX16 | 5.04 | 8.58 |
| BUFX20 | 5.04 | 10.56 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | | | | | | |
|-----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0155 | 0.0181 | 0.0310 | 0.0450 | 0.0585 | 0.1119 | 0.1657 | 0.2252 | 0.2815 |

Pin Capacitance

| Pin | Capacitance (pF) | | | | | | | | |
|-----|------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0026 | 0.0026 | 0.0035 | 0.0048 | 0.0062 | 0.0114 | 0.0168 | 0.0220 | 0.0276 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | | | | | |
|-------------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 0.0543 | 0.0582 | 0.0615 | 0.0606 | 0.0605 | 0.0566 | 0.0567 | 0.0576 | 0.0569 |
| A → Y↓ | 0.0764 | 0.0859 | 0.0851 | 0.0834 | 0.0820 | 0.0778 | 0.0776 | 0.0779 | 0.0772 |

| Description | K_{load} (ns/pF) | | | | | | | | |
|-------------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 5.8769 | 4.1978 | 2.1272 | 1.3834 | 1.0640 | 0.5199 | 0.3466 | 0.2599 | 0.2080 |
| A → Y↓ | 3.4601 | 2.5274 | 1.2908 | 0.8588 | 0.6458 | 0.3227 | 0.2151 | 0.1600 | 0.1290 |

Cell Description

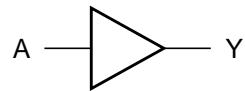
The CLKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| CLKBUFXL | 5.04 | 2.64 |
| CLKBUFX1 | 5.04 | 2.64 |
| CLKBUFX2 | 5.04 | 2.64 |
| CLKBUFX3 | 5.04 | 2.64 |
| CLKBUFX4 | 5.04 | 3.30 |
| CLKBUFX8 | 5.04 | 4.62 |
| CLKBUFX12 | 5.04 | 10.56 |
| CLKBUFX16 | 5.04 | 12.54 |
| CLKBUFX20 | 5.04 | 15.84 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | | | | | | | |
|-----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 | |
| A | 0.0165 | 0.0209 | 0.0260 | 0.0352 | 0.0444 | 0.0862 | 0.2174 | 0.2797 | 0.3457 | |

Pin Capacitance

| Pin | Capacitance (pF) | | | | | | | | | |
|-----|------------------|--------|--------|--------|--------|--------|--------|--------|--------|--|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 | |
| A | 0.0024 | 0.0038 | 0.0033 | 0.0036 | 0.0044 | 0.0081 | 0.0196 | 0.0235 | 0.0324 | |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | | | | | | |
|-------------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|--|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 | |
| A → Y↑ | 0.0520 | 0.0600 | 0.0686 | 0.0808 | 0.0819 | 0.0766 | 0.0762 | 0.0805 | 0.0752 | |
| A → Y↓ | 0.1061 | 0.0608 | 0.0803 | 0.0888 | 0.0872 | 0.0815 | 0.0806 | 0.0850 | 0.0791 | |

| Description | K _{load} (ns/pF) | | | | | | | | | |
|-------------|---------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 | |
| A → Y↑ | 3.7823 | 3.8530 | 2.1274 | 1.4272 | 1.0650 | 0.5203 | 0.2087 | 0.1606 | 0.1304 | |
| A → Y↓ | 4.4301 | 4.3830 | 2.3654 | 1.4566 | 1.1190 | 0.5310 | 0.2150 | 0.1654 | 0.1290 | |

Cell Description

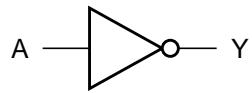
The CLKINV cell provides the logical inversion of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = \bar{A}$$

Functions

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

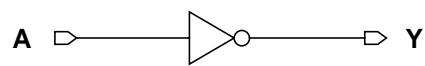
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| CLKINVXL | 5.04 | 1.98 |
| CLKINVX1 | 5.04 | 1.98 |
| CLKINVX2 | 5.04 | 1.98 |
| CLKINVX3 | 5.04 | 1.98 |
| CLKINVX4 | 5.04 | 2.64 |
| CLKINVX8 | 5.04 | 3.96 |
| CLKINVX12 | 5.04 | 12.54 |
| CLKINVX16 | 5.04 | 16.50 |
| CLKINVX20 | 5.04 | 19.14 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | | | | | | |
|-----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0087 | 0.0104 | 0.0177 | 0.0264 | 0.0346 | 0.0712 | 0.2496 | 0.3309 | 0.4136 |

Pin Capacitance

| Pin | Capacitance (pF) | | | | | | | | |
|-----|------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0029 | 0.0034 | 0.0060 | 0.0089 | 0.0115 | 0.0236 | 0.0072 | 0.0090 | 0.0110 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | | | | | |
|-------------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 0.0240 | 0.0223 | 0.0185 | 0.0178 | 0.0177 | 0.0178 | 0.1462 | 0.1486 | 0.1470 |
| A → Y↓ | 0.0201 | 0.0198 | 0.0189 | 0.0171 | 0.0172 | 0.0174 | 0.1480 | 0.1498 | 0.1499 |

| Description | K_{load} (ns/pF) | | | | | | | | |
|-------------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 5.3816 | 4.1927 | 2.0963 | 1.3911 | 1.0559 | 0.5190 | 0.2088 | 0.1566 | 0.1253 |
| A → Y↓ | 4.5606 | 3.8518 | 2.3568 | 1.4485 | 1.1131 | 0.5493 | 0.2222 | 0.1667 | 0.1333 |

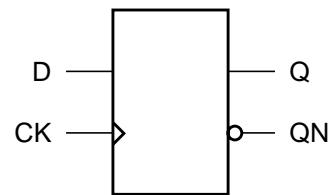
Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

Function Table

| D | CK | Q[n+1] | QN[n+1] |
|---|----|--------|---------|
| 0 | / | 0 | 1 |
| 1 | / | 1 | 0 |
| x | \ | Q[n] | QN[n] |

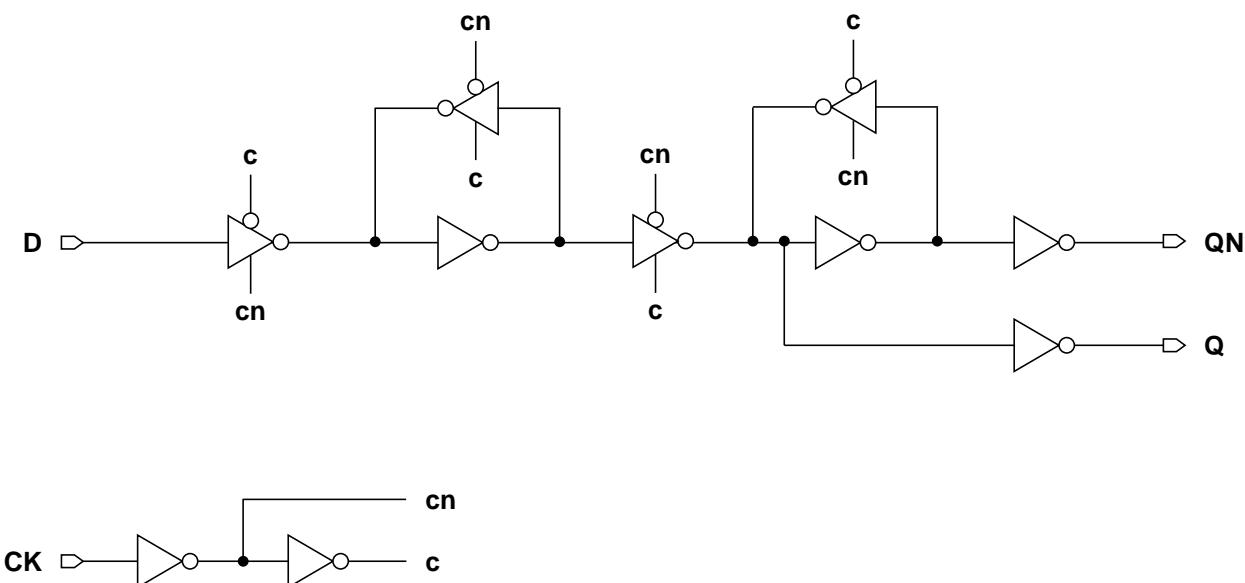
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DFFXL | 5.04 | 11.22 |
| DFFX1 | 5.04 | 11.22 |
| DFFX2 | 5.04 | 13.86 |
| DFFX4 | 5.04 | 16.50 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0345 | 0.0302 | 0.0402 | 0.0641 |
| CK | 0.0364 | 0.0338 | 0.0412 | 0.0678 |
| Q | 0.0395 | 0.0444 | 0.0744 | 0.1212 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0035 | 0.0023 | 0.0026 | 0.0040 |
| CK | 0.0024 | 0.0029 | 0.0040 | 0.0063 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2426 | 0.2133 | 0.1956 | 0.1704 | 5.3145 | 4.0674 | 2.1054 | 1.0781 |
| CK → Q↓ | 0.1939 | 0.1711 | 0.1596 | 0.1418 | 3.5988 | 2.5754 | 1.2868 | 0.6533 |
| CK → QN↑ | 0.2600 | 0.2325 | 0.2115 | 0.1931 | 5.8907 | 4.2042 | 2.1011 | 1.0765 |
| CK → QN↓ | 0.3319 | 0.2982 | 0.2726 | 0.2392 | 3.5137 | 2.5427 | 1.2685 | 0.6464 |

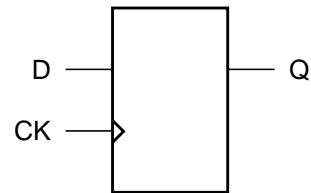
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0430 | 0.0703 | 0.0703 | 0.0625 |
| | setup↓ → CK | 0.0898 | 0.1523 | 0.1484 | 0.1328 |
| | hold↑ → CK | -0.0273 | -0.0430 | -0.0508 | -0.0391 |
| | hold↓ → CK | 0.0156 | -0.0391 | -0.0430 | -0.0312 |
| CK | minpwh | 0.1273 | 0.1176 | 0.1078 | 0.0933 |
| | minpwl | 0.1759 | 0.1613 | 0.1516 | 0.1224 |

Cell Description

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



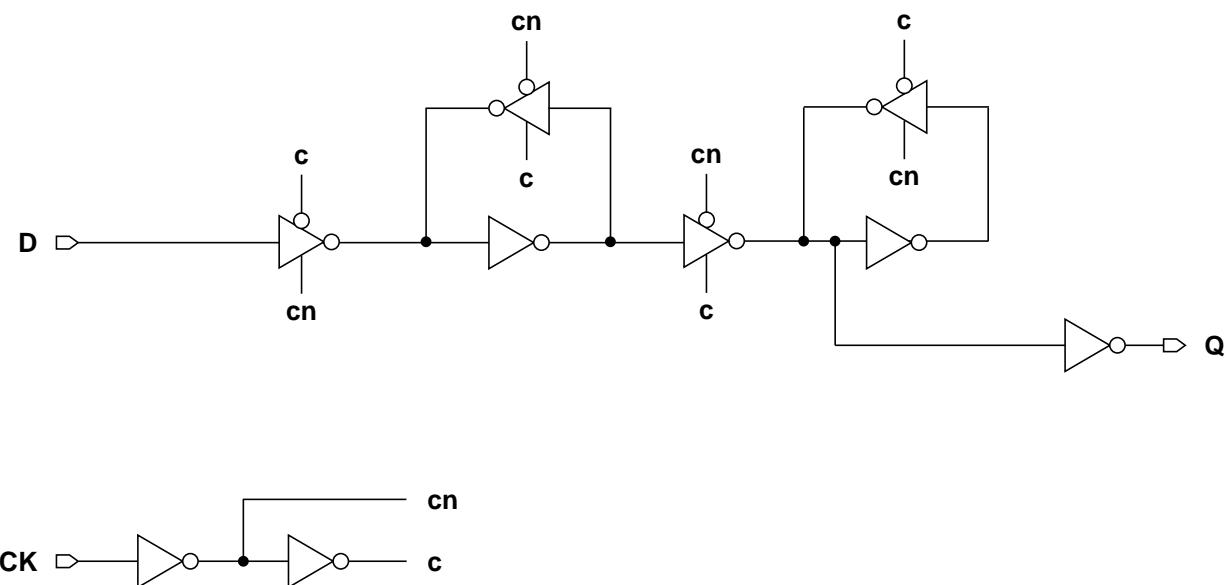
Functions

| D | CK | Q[n+1] |
|---|-----|--------|
| 0 | /\ | 0 |
| 1 | /\ | 1 |
| x | \/\ | Q[n] |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DFFHQXL | 5.04 | 10.56 |
| DFFHQX1 | 5.04 | 10.56 |
| DFFHQX2 | 5.04 | 13.20 |
| DFFHQX4 | 5.04 | 14.52 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0388 | 0.0401 | 0.0540 | 0.0768 |
| CK | 0.0365 | 0.0350 | 0.0416 | 0.0538 |
| Q | 0.0293 | 0.0321 | 0.0469 | 0.0667 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0037 | 0.0024 | 0.0025 | 0.0033 |
| CK | 0.0025 | 0.0032 | 0.0039 | 0.0056 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2191 | 0.1813 | 0.1768 | 0.1562 | 5.9079 | 4.0640 | 2.1036 | 1.0587 |
| CK → Q↓ | 0.2179 | 0.1659 | 0.1601 | 0.1414 | 3.7092 | 2.6900 | 1.3440 | 0.6525 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0508 | 0.0938 | 0.0938 | 0.0859 |
| | setup↓ → CK | 0.1445 | 0.1953 | 0.2031 | 0.1836 |
| | hold↑ → CK | -0.0234 | -0.0469 | -0.0469 | -0.0430 |
| | hold↓ → CK | 0.0117 | -0.0391 | -0.0391 | -0.0391 |
| CK | minpwh | 0.1418 | 0.1078 | 0.1078 | 0.0933 |
| | minpwl | 0.1564 | 0.1564 | 0.1516 | 0.1224 |

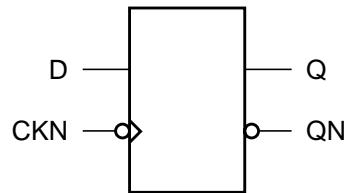
Cell Description

The DFFN cell is a negative-edge triggered, static D-type flip-flop.

Functions

| D | CKN | Q[n+1] | QN[n+1] |
|---|-----|--------|---------|
| 0 | — | 0 | 1 |
| 1 | — | 1 | 0 |
| x | — | Q[n] | QN[n] |

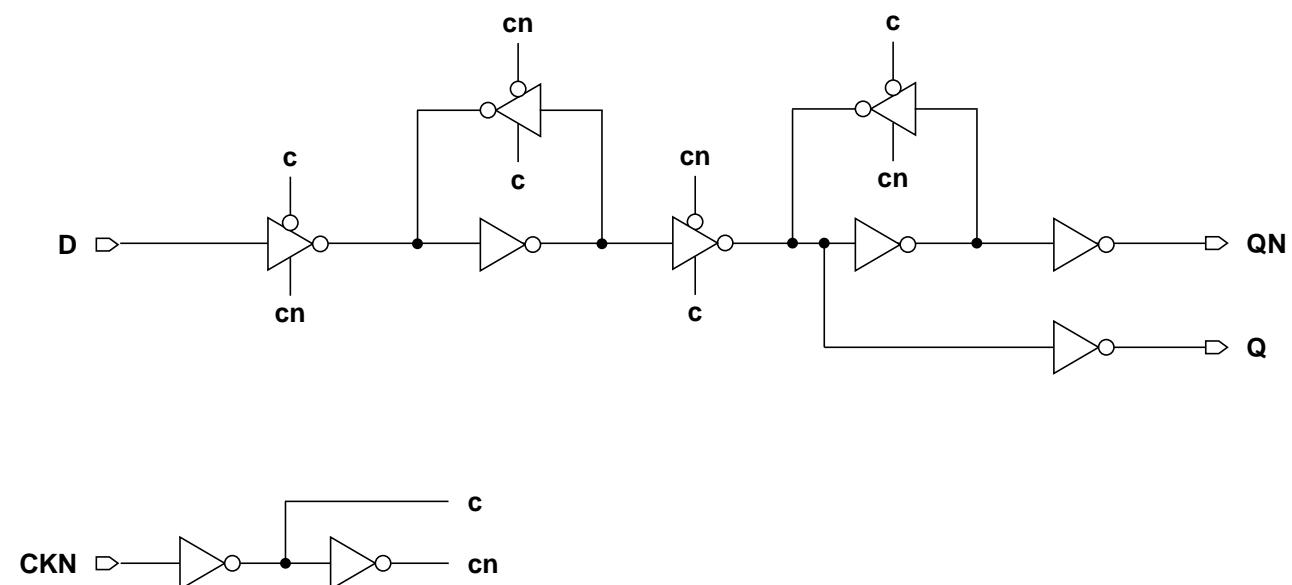
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFNXL | 5.04 | 11.22 |
| DFFNX1 | 5.04 | 11.22 |
| DFFNX2 | 5.04 | 13.86 |
| DFFNX4 | 5.04 | 15.84 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0342 | 0.0304 | 0.0403 | 0.0601 |
| CKN | 0.0369 | 0.0400 | 0.0543 | 0.0849 |
| Q | 0.0388 | 0.0439 | 0.0764 | 0.1283 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0031 | 0.0020 | 0.0024 | 0.0029 |
| CKN | 0.0025 | 0.0031 | 0.0039 | 0.0065 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.1918 | 0.1545 | 0.1402 | 0.1193 | 5.3272 | 4.0701 | 2.1067 | 1.1110 |
| CKN → Q↓ | 0.3245 | 0.2760 | 0.2525 | 0.2134 | 3.6098 | 2.6519 | 1.3251 | 0.6535 |
| CKN → QN↑ | 0.3831 | 0.3365 | 0.3036 | 0.2686 | 5.8930 | 4.2042 | 2.1011 | 1.1091 |
| CKN → QN↓ | 0.2758 | 0.2402 | 0.2175 | 0.1887 | 3.5097 | 2.5432 | 1.2686 | 0.6470 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CKN | 0.0430 | 0.0820 | 0.0859 | 0.0859 |
| | setup↓ → CKN | 0.0625 | 0.1289 | 0.1250 | 0.1211 |
| | hold↑ → CKN | 0.0820 | 0.0391 | 0.0312 | 0.0195 |
| | hold↓ → CKN | -0.0469 | -0.0977 | -0.0938 | -0.0938 |
| CKN | minpwl | 0.2050 | 0.1661 | 0.1516 | 0.1273 |
| | minpwh | 0.1321 | 0.1516 | 0.1418 | 0.1176 |

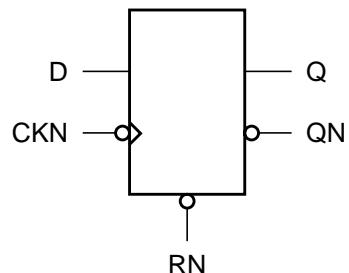
Cell Description

The DFFNR cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Functions

| RN | D | CKN | Q[n+1] | QN[n+1] |
|----|---|-----|--------|---------|
| 0 | x | x | 0 | 1 |
| 1 | 0 | — | 0 | 1 |
| 1 | 1 | — | 1 | 0 |
| 1 | x | — | Q[n] | QN[n] |

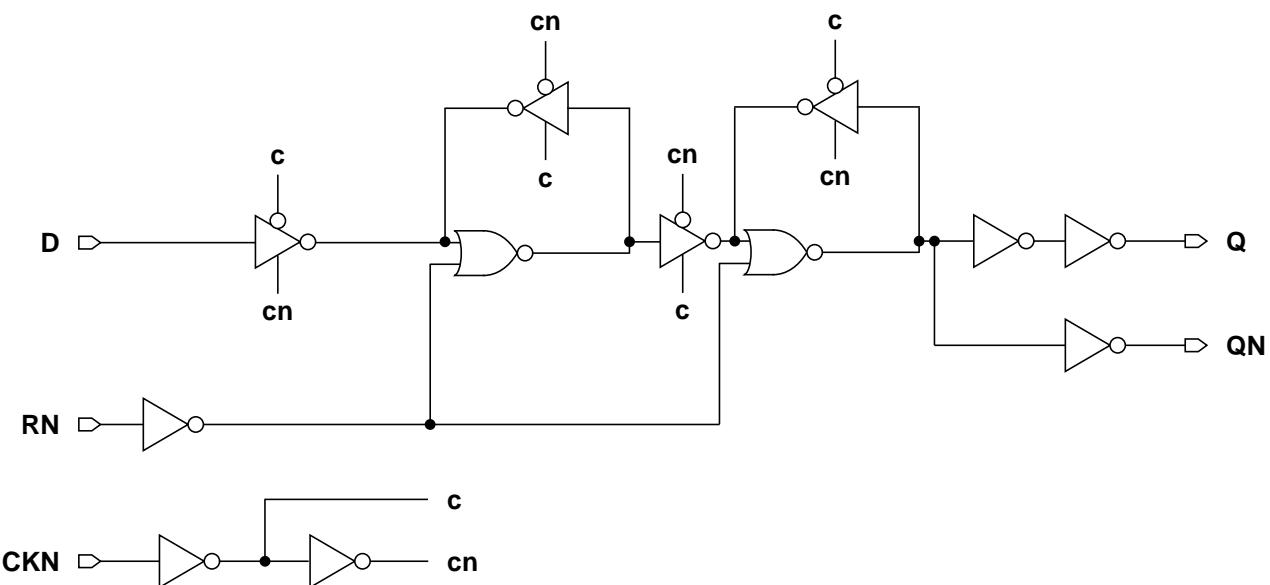
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DFFNRXL | 5.04 | 15.84 |
| DFFNRX1 | 5.04 | 15.18 |
| DFFNRX2 | 5.04 | 17.16 |
| DFFNRX4 | 5.04 | 20.46 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0357 | 0.0286 | 0.0332 | 0.0430 |
| CKN | 0.0379 | 0.0362 | 0.0443 | 0.0563 |
| RN | 0.0167 | 0.0182 | 0.0224 | 0.0344 |
| Q | 0.0478 | 0.0545 | 0.0872 | 0.1510 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0035 | 0.0023 | 0.0023 | 0.0030 |
| CKN | 0.0027 | 0.0030 | 0.0031 | 0.0041 |
| RN | 0.0024 | 0.0027 | 0.0034 | 0.0061 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.3808 | 0.3338 | 0.3251 | 0.2965 | 5.8854 | 4.2015 | 2.0802 | 1.0643 |
| CKN → Q↓ | 0.4442 | 0.4306 | 0.4336 | 0.3825 | 3.4685 | 2.5310 | 1.3364 | 0.6517 |
| RN → Q↓ | 0.2501 | 0.2500 | 0.2405 | 0.2184 | 3.4690 | 2.5312 | 1.3364 | 0.6517 |
| CKN → QN↑ | 0.3920 | 0.3663 | 0.3591 | 0.3148 | 5.8846 | 4.2019 | 2.0815 | 1.0648 |
| CKN → QN↓ | 0.3498 | 0.2963 | 0.2733 | 0.2415 | 3.6990 | 2.5940 | 1.3608 | 0.6627 |
| RN → QN↑ | 0.1983 | 0.1864 | 0.1665 | 0.1512 | 5.8969 | 4.2058 | 2.0836 | 1.0662 |

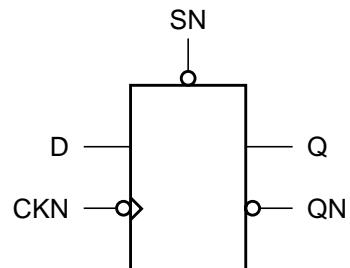
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CKN | 0.0430 | 0.0820 | 0.1133 | 0.0938 |
| | setup↓ → CKN | 0.0664 | 0.1328 | 0.1484 | 0.1211 |
| | hold↑ → CKN | 0.0898 | 0.0352 | 0.0352 | 0.0312 |
| | hold↓ → CKN | -0.0430 | -0.0977 | -0.1016 | -0.0859 |
| CKN | minpwl | 0.2099 | 0.2001 | 0.1904 | 0.1613 |
| | minpwh | 0.1370 | 0.1516 | 0.1759 | 0.1467 |
| RN | minpwl | 0.1856 | 0.1807 | 0.2050 | 0.3022 |
| | recovery | 0.0391 | 0.0703 | 0.0938 | 0.0781 |

Cell Description

The DFFNS cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Logic Symbol



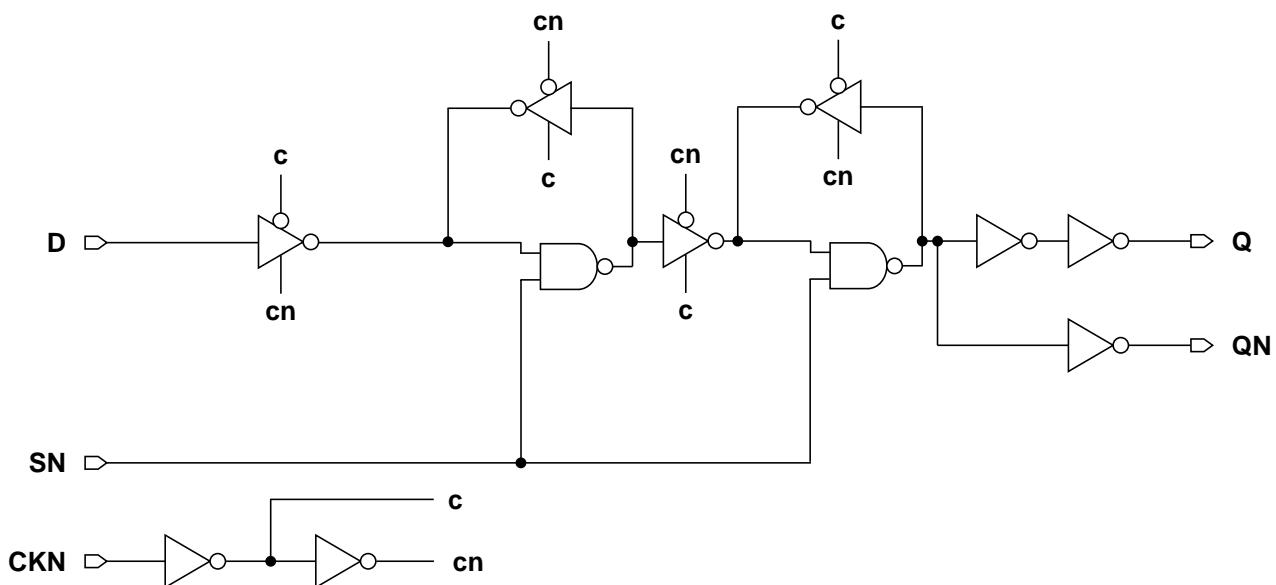
Functions

| SN | D | CKN | Q[n+1] | QN[n+1] |
|----|---|-----|--------|---------|
| 0 | x | x | 1 | 0 |
| 1 | 0 | ¬ | 0 | 1 |
| 1 | 1 | ¬ | 1 | 0 |
| 1 | x | ¬ | Q[n] | QN[n] |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFNSXL | 5.04 | 13.86 |
| DFFNSX1 | 5.04 | 13.86 |
| DFFNSX2 | 5.04 | 13.86 |
| DFFNSX4 | 5.04 | 19.14 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0348 | 0.0274 | 0.0305 | 0.0390 |
| CKN | 0.0361 | 0.0346 | 0.0381 | 0.0502 |
| SN | 0.0068 | 0.0076 | 0.0106 | 0.0177 |
| Q | 0.0435 | 0.0515 | 0.0833 | 0.1477 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0030 | 0.0020 | 0.0020 | 0.0022 |
| CKN | 0.0023 | 0.0028 | 0.0031 | 0.0036 |
| SN | 0.0051 | 0.0056 | 0.0073 | 0.0124 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.3097 | 0.2835 | 0.2802 | 0.2691 | 5.8861 | 4.2009 | 2.1523 | 1.0579 |
| CKN → Q↓ | 0.4274 | 0.4096 | 0.3980 | 0.3833 | 3.4661 | 2.5286 | 1.2919 | 0.6462 |
| SN → Q↑ | 0.1679 | 0.1536 | 0.1579 | 0.1520 | 5.8861 | 4.2010 | 2.1524 | 1.0579 |
| CKN → QN↑ | 0.3809 | 0.3505 | 0.3282 | 0.3158 | 5.9058 | 4.2075 | 2.1571 | 1.0602 |
| CKN → QN↓ | 0.2795 | 0.2461 | 0.2283 | 0.2173 | 3.5423 | 2.5426 | 1.2975 | 0.6486 |
| SN → QN↓ | 0.1378 | 0.1164 | 0.1062 | 0.1005 | 3.5300 | 2.5427 | 1.3000 | 0.6509 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CKN | 0.0234 | 0.0664 | 0.0703 | 0.0703 |
| | setup↓ → CKN | 0.0664 | 0.1328 | 0.1406 | 0.1289 |
| | hold↑ → CKN | 0.0859 | 0.0352 | 0.0352 | 0.0352 |
| | hold↓ → CKN | -0.0547 | -0.1055 | -0.1133 | -0.1016 |
| CKN | minpwl | 0.1953 | 0.1856 | 0.1661 | 0.1613 |
| | minpwh | 0.1273 | 0.1418 | 0.1467 | 0.1418 |
| SN | minpwl | 0.1321 | 0.1176 | 0.1224 | 0.1516 |
| | recovery | -0.0859 | -0.0430 | -0.0430 | -0.0391 |

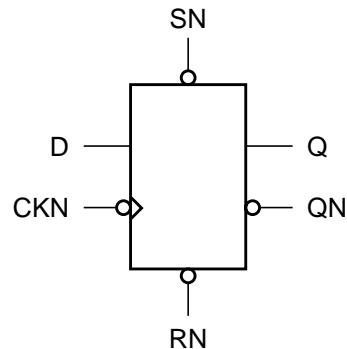
Cell Description

The DFFNSR cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Functions

| RN | SN | D | CKN | Q[n+1] | QN[n+1] |
|----|----|---|-----|--------|---------|
| 0 | 1 | x | x | 0 | 1 |
| 1 | 0 | x | x | 1 | 0 |
| 0 | 0 | x | x | 1 | 0 |
| 1 | 1 | 0 | — | 0 | 1 |
| 1 | 1 | 1 | — | 1 | 0 |
| 1 | 1 | x | — | Q[n] | QN[n] |

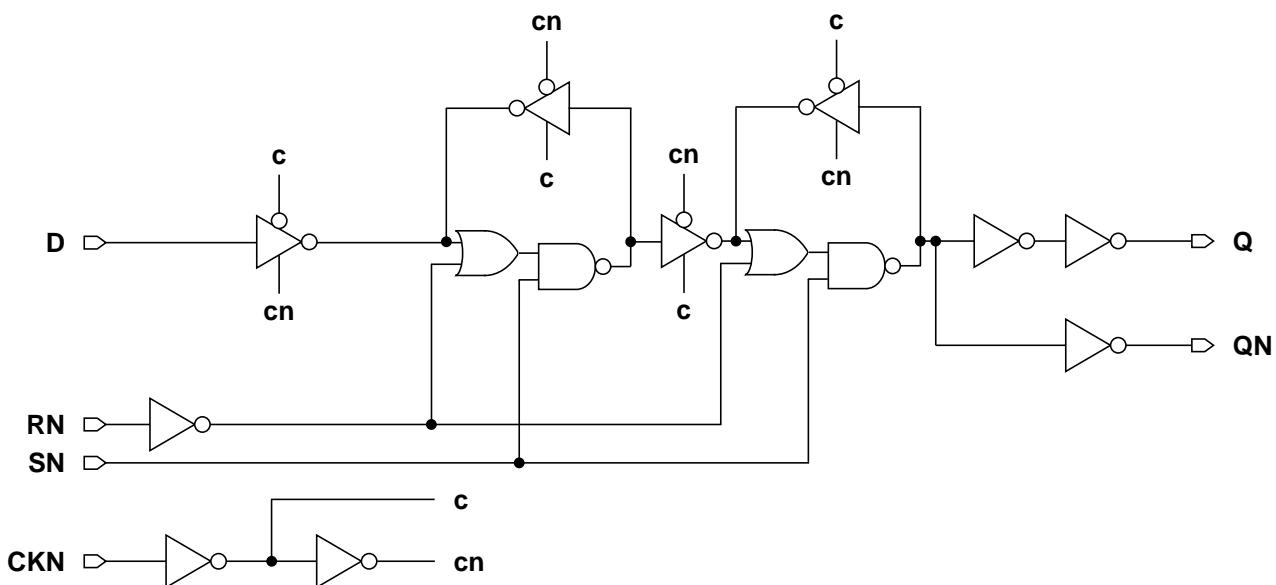
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFNSRXL | 5.04 | 17.16 |
| DFFNSRX1 | 5.04 | 16.50 |
| DFFNSRX2 | 5.04 | 17.16 |
| DFFNSRX4 | 5.04 | 23.10 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0400 | 0.0320 | 0.0359 | 0.0519 |
| CKN | 0.0386 | 0.0378 | 0.0424 | 0.0602 |
| SN | 0.0086 | 0.0090 | 0.0121 | 0.0187 |
| RN | 0.0185 | 0.0201 | 0.0252 | 0.0421 |
| Q | 0.0515 | 0.0569 | 0.0901 | 0.1629 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0035 | 0.0024 | 0.0023 | 0.0034 |
| CKN | 0.0025 | 0.0028 | 0.0030 | 0.0042 |
| SN | 0.0067 | 0.0070 | 0.0092 | 0.0156 |
| RN | 0.0027 | 0.0029 | 0.0039 | 0.0061 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.3873 | 0.3400 | 0.3249 | 0.3055 | 5.8845 | 4.2004 | 2.1526 | 1.0641 |
| CKN → Q↓ | 0.4639 | 0.4436 | 0.4152 | 0.3876 | 3.2338 | 2.5336 | 1.2926 | 0.6463 |
| SN → Q↑ | 0.1944 | 0.1795 | 0.1751 | 0.1660 | 5.8833 | 4.2000 | 2.1525 | 1.0641 |
| SN → Q↓ | 0.2043 | 0.1899 | 0.1785 | 0.1700 | 3.2350 | 2.5339 | 1.2927 | 0.6463 |
| RN → Q↓ | 0.2901 | 0.2736 | 0.2482 | 0.2364 | 3.2349 | 2.5339 | 1.2927 | 0.6463 |
| CKN → QN↑ | 0.4030 | 0.3710 | 0.3445 | 0.3203 | 5.9226 | 4.2121 | 2.1575 | 1.0671 |
| CKN → QN↓ | 0.3479 | 0.2964 | 0.2691 | 0.2544 | 3.7716 | 2.6061 | 1.3201 | 0.6612 |
| SN → QN↑ | 0.1440 | 0.1182 | 0.1085 | 0.1028 | 5.9517 | 4.2249 | 2.1641 | 1.0713 |
| SN → QN↓ | 0.1527 | 0.1332 | 0.1193 | 0.1151 | 3.5750 | 2.5608 | 1.3050 | 0.6560 |
| RN → QN↑ | 0.2296 | 0.2017 | 0.1780 | 0.1691 | 5.9499 | 4.2244 | 2.1638 | 1.0711 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CKN | 0.0703 | 0.1406 | 0.1250 | 0.1094 |
| | setup↓ → CKN | 0.0938 | 0.1562 | 0.1719 | 0.1328 |
| | hold↑ → CKN | 0.0703 | 0.0156 | 0.0195 | 0.0273 |
| | hold↓ → CKN | -0.0664 | -0.1055 | -0.1250 | -0.0938 |
| CKN | minpwl | 0.2001 | 0.1953 | 0.1710 | 0.1564 |
| | minpwh | 0.1370 | 0.1661 | 0.1661 | 0.1370 |
| SN | minpwl | 0.1516 | 0.1370 | 0.1370 | 0.1759 |
| | recovery | -0.0742 | -0.0352 | -0.0352 | -0.0352 |
| | removal | 0.0820 | 0.0430 | 0.0430 | 0.0469 |
| RN | minpwl | 0.2050 | 0.1904 | 0.2050 | 0.3167 |
| | recovery | 0.0625 | 0.1211 | 0.0977 | 0.0977 |
| | removal | 0.0859 | 0.0234 | 0.0469 | 0.0469 |

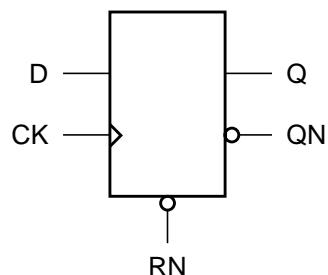
Cell Description

The DFFR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Functions

| RN | D | CK | Q[n+1] | QN[n+1] |
|----|---|----|--------|---------|
| 0 | x | x | 0 | 1 |
| 1 | 0 | — | 0 | 1 |
| 1 | 1 | — | 1 | 0 |
| 1 | x | — | Q[n] | QN[n] |

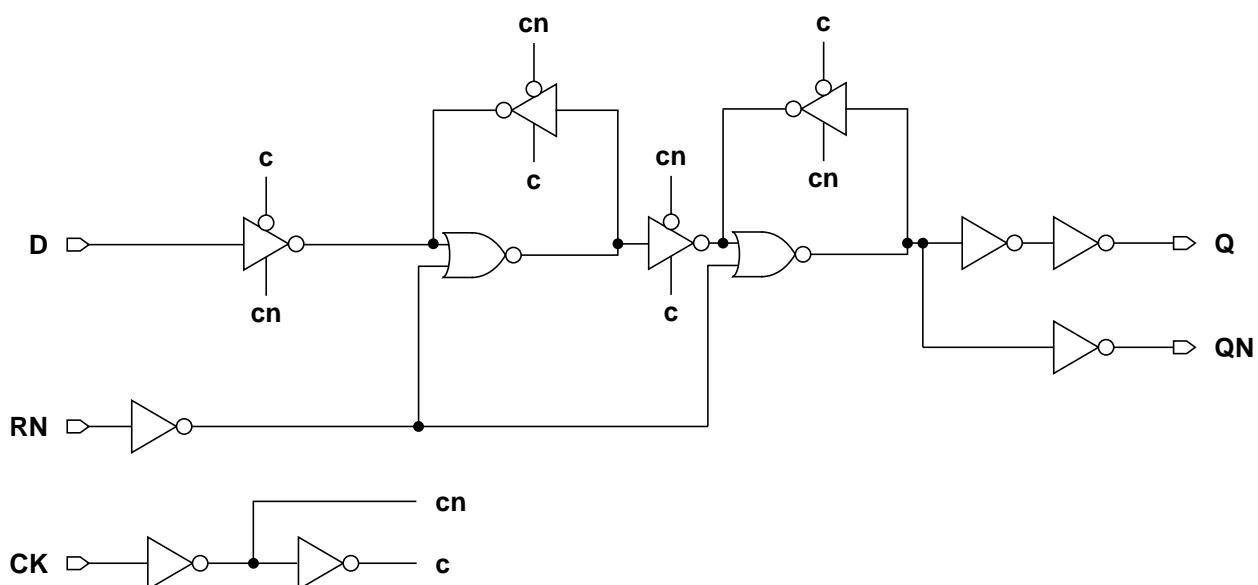
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFRLXL | 5.04 | 15.18 |
| DFFRX1 | 5.04 | 15.18 |
| DFFRX2 | 5.04 | 17.16 |
| DFFRX4 | 5.04 | 19.80 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0356 | 0.0286 | 0.0326 | 0.0428 |
| CK | 0.0370 | 0.0351 | 0.0387 | 0.0452 |
| RN | 0.0160 | 0.0180 | 0.0221 | 0.0341 |
| Q | 0.0500 | 0.0563 | 0.0897 | 0.1548 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0035 | 0.0024 | 0.0022 | 0.0031 |
| CK | 0.0025 | 0.0030 | 0.0031 | 0.0042 |
| RN | 0.0023 | 0.0027 | 0.0034 | 0.0061 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.4355 | 0.3976 | 0.3961 | 0.3536 | 5.8906 | 4.2015 | 2.0803 | 1.0643 |
| CK → Q↓ | 0.3013 | 0.3186 | 0.3046 | 0.2774 | 3.4685 | 2.5313 | 1.2943 | 0.6517 |
| RN → Q↓ | 0.2477 | 0.2497 | 0.2405 | 0.2183 | 3.4691 | 2.5314 | 1.2943 | 0.6517 |
| CK → QN↑ | 0.2514 | 0.2543 | 0.2307 | 0.2098 | 5.8878 | 4.2019 | 2.0814 | 1.0649 |
| CK → QN↓ | 0.4065 | 0.3601 | 0.3431 | 0.2986 | 3.7020 | 2.5945 | 1.3188 | 0.6627 |
| RN → QN↑ | 0.1980 | 0.1862 | 0.1671 | 0.1511 | 5.8994 | 4.2059 | 2.0835 | 1.0662 |

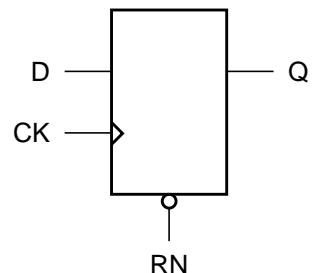
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0547 | 0.0781 | 0.0977 | 0.0781 |
| | setup↓ → CK | 0.0859 | 0.1406 | 0.1680 | 0.1406 |
| | hold↑ → CK | -0.0391 | -0.0586 | -0.0664 | -0.0547 |
| | hold↓ → CK | 0.0273 | -0.0391 | -0.0352 | -0.0312 |
| CK | minpwh | 0.1321 | 0.1418 | 0.1321 | 0.1127 |
| | minpwl | 0.1953 | 0.1759 | 0.2001 | 0.1564 |
| RN | minpwl | 0.1807 | 0.1807 | 0.2050 | 0.2973 |
| | recovery | 0.0430 | 0.0508 | 0.0703 | 0.0547 |
| | removal | -0.0234 | -0.0352 | -0.0430 | -0.0195 |

Cell Description

The DFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



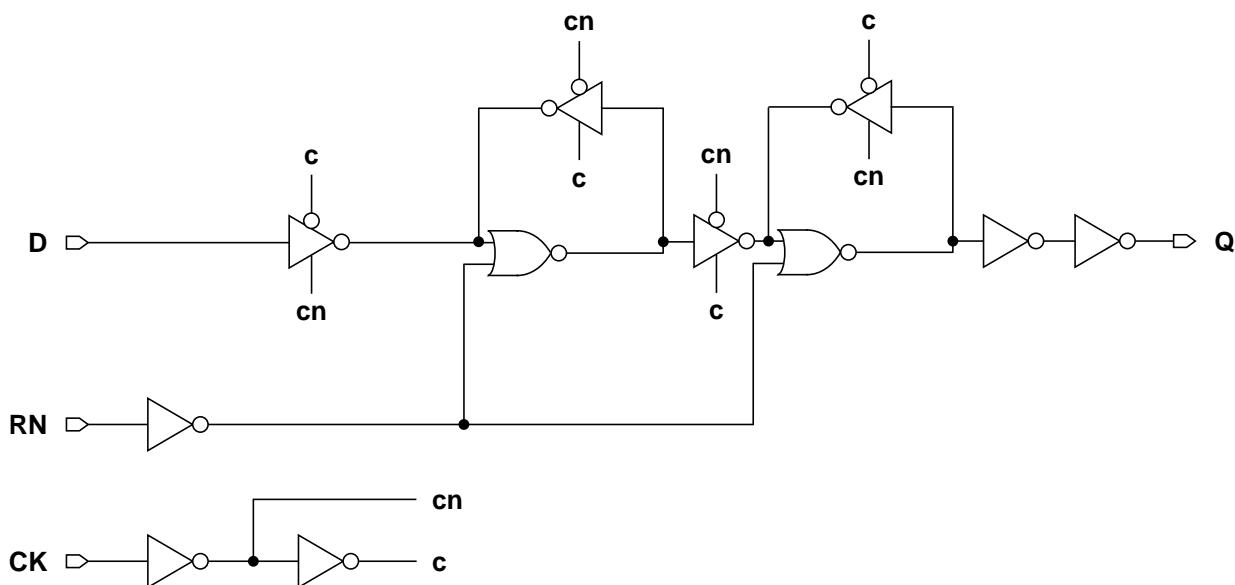
Functions

| RN | D | CK | $Q[n+1]$ |
|----|---|----|----------|
| 0 | x | x | 0 |
| 1 | 0 | — | 0 |
| 1 | 1 | — | 1 |
| 1 | x | — | $Q[n]$ |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DFFRHQXL | 5.04 | 13.86 |
| DFFRHQX1 | 5.04 | 13.86 |
| DFFRHQX2 | 5.04 | 17.16 |
| DFFRHQX4 | 5.04 | 21.12 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0366 | 0.0430 | 0.0646 | 0.1006 |
| CK | 0.0378 | 0.0382 | 0.0483 | 0.0666 |
| RN | 0.0211 | 0.0261 | 0.0354 | 0.0570 |
| Q | 0.0357 | 0.0396 | 0.0506 | 0.0819 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0034 | 0.0022 | 0.0028 | 0.0046 |
| CK | 0.0024 | 0.0033 | 0.0044 | 0.0065 |
| RN | 0.0028 | 0.0043 | 0.0058 | 0.0098 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2450 | 0.1986 | 0.1784 | 0.1616 | 8.7423 | 6.0781 | 3.0379 | 1.6812 |
| CK → Q↓ | 0.2556 | 0.1755 | 0.1557 | 0.1424 | 3.8011 | 2.5696 | 1.3048 | 0.7203 |
| RN → Q↓ | 0.1829 | 0.1414 | 0.1238 | 0.1070 | 3.0099 | 2.0112 | 1.1284 | 0.6780 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0781 | 0.1250 | 0.1250 | 0.1211 |
| | setup↓ → CK | 0.1484 | 0.2109 | 0.2031 | 0.1797 |
| | hold↑ → CK | -0.0234 | -0.0547 | -0.0508 | -0.0430 |
| | hold↓ → CK | 0.0195 | -0.0352 | -0.0234 | -0.0195 |
| CK | minpwh | 0.1661 | 0.1176 | 0.1030 | 0.0933 |
| | minpwl | 0.1710 | 0.1661 | 0.1467 | 0.1224 |
| RN | minpwl | 0.2536 | 0.2536 | 0.3362 | 0.5159 |
| | recovery | 0.1016 | 0.1133 | 0.1172 | 0.1133 |
| | removal | -0.0312 | -0.0430 | -0.0352 | -0.0195 |

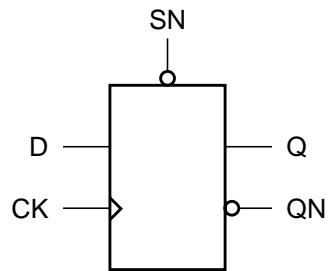
Cell Description

The DFFS cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Functions

| SN | D | CK | Q[n+1] | QN[n+1] |
|----|---|----|--------|---------|
| 0 | x | x | 1 | 0 |
| 1 | 0 | ✓ | 0 | 1 |
| 1 | 1 | ✓ | 1 | 0 |
| 1 | x | ✗ | Q[n] | QN[n] |

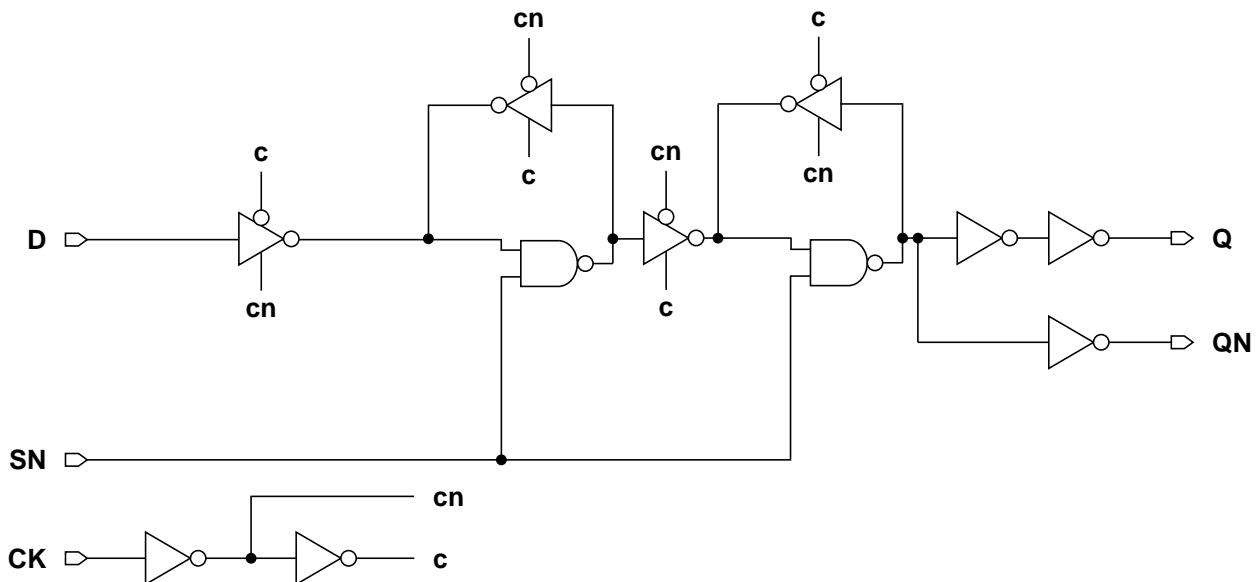
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFSXL | 5.04 | 12.54 |
| DFFSX1 | 5.04 | 12.54 |
| DFFSX2 | 5.04 | 13.86 |
| DFFSX4 | 5.04 | 18.48 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0336 | 0.0259 | 0.0299 | 0.0373 |
| CK | 0.0346 | 0.0314 | 0.0346 | 0.0418 |
| SN | 0.0070 | 0.0077 | 0.0118 | 0.0182 |
| Q | 0.0445 | 0.0489 | 0.0840 | 0.1453 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0035 | 0.0022 | 0.0022 | 0.0025 |
| CK | 0.0025 | 0.0031 | 0.0032 | 0.0037 |
| SN | 0.0055 | 0.0059 | 0.0079 | 0.0130 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.3594 | 0.3309 | 0.3449 | 0.3265 | 5.8865 | 4.2010 | 2.0795 | 1.0639 |
| CK → Q↓ | 0.2909 | 0.2931 | 0.2996 | 0.2779 | 3.4690 | 2.5300 | 1.2922 | 0.6460 |
| SN → Q↑ | 0.1689 | 0.1507 | 0.1597 | 0.1520 | 5.8866 | 4.2011 | 2.0796 | 1.0639 |
| CK → QN↑ | 0.2434 | 0.2353 | 0.2284 | 0.2117 | 5.9044 | 4.4004 | 2.0846 | 1.0422 |
| CK → QN↓ | 0.3284 | 0.2950 | 0.2933 | 0.2758 | 3.5432 | 2.7022 | 1.2981 | 0.6485 |
| SN → QN↓ | 0.1381 | 0.1149 | 0.1084 | 0.1017 | 3.5336 | 2.7023 | 1.3007 | 0.6509 |

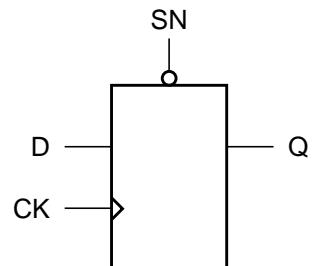
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0391 | 0.0625 | 0.0625 | 0.0664 |
| | setup↓ → CK | 0.0898 | 0.1484 | 0.1484 | 0.1484 |
| | hold↑ → CK | -0.0312 | -0.0469 | -0.0508 | -0.0430 |
| | hold↓ → CK | 0.0039 | -0.0547 | -0.0508 | -0.0430 |
| CK | minpwh | 0.1176 | 0.1273 | 0.1224 | 0.1127 |
| | minpw1 | 0.1613 | 0.1516 | 0.1564 | 0.1516 |
| SN | minpw1 | 0.1321 | 0.1127 | 0.1273 | 0.1516 |
| | recovery | -0.0117 | -0.0039 | 0.0000 | 0.0078 |
| | removal | 0.1367 | 0.0977 | 0.1055 | 0.0977 |

Cell Description

The DFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



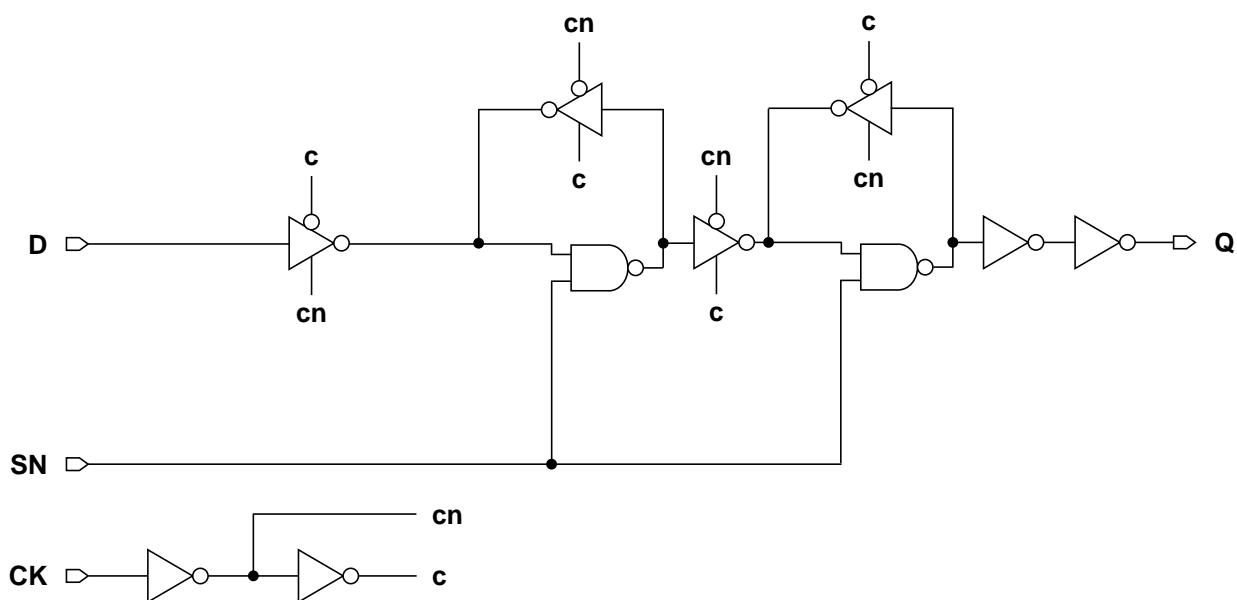
Functions

| SN | D | CK | Q[n+1] |
|----|---|----|--------|
| 0 | x | x | 1 |
| 1 | 0 | — | 0 |
| 1 | 1 | — | 1 |
| 1 | x | — | Q[n] |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFSHQXL | 5.04 | 13.20 |
| DFFSHQX1 | 5.04 | 13.20 |
| DFFSHQX2 | 5.04 | 15.84 |
| DFFSHQX4 | 5.04 | 18.48 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0377 | 0.0415 | 0.0596 | 0.0921 |
| CK | 0.0367 | 0.0375 | 0.0443 | 0.0621 |
| SN | 0.0107 | 0.0117 | 0.0198 | 0.0318 |
| Q | 0.0340 | 0.0365 | 0.0521 | 0.0845 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0036 | 0.0021 | 0.0028 | 0.0040 |
| CK | 0.0026 | 0.0031 | 0.0040 | 0.0060 |
| SN | 0.0088 | 0.0095 | 0.0147 | 0.0228 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2417 | 0.2035 | 0.1834 | 0.1652 | 5.9321 | 4.2091 | 2.1306 | 1.0651 |
| CK → Q↓ | 0.2432 | 0.1745 | 0.1530 | 0.1442 | 4.4174 | 2.9838 | 1.4863 | 0.7488 |
| SN → Q↑ | 0.0739 | 0.0841 | 0.0870 | 0.0902 | 3.3614 | 2.3065 | 1.2157 | 0.6577 |

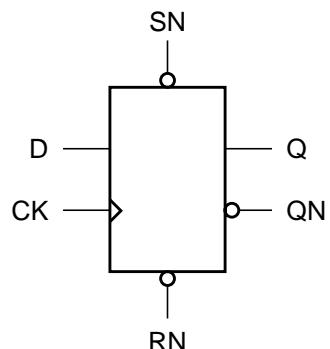
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0547 | 0.0938 | 0.0898 | 0.0859 |
| | setup↓ → CK | 0.1719 | 0.2305 | 0.2148 | 0.1914 |
| | hold↑ → CK | -0.0234 | -0.0469 | -0.0430 | -0.0391 |
| | hold↓ → CK | 0.0078 | -0.0586 | -0.0391 | -0.0312 |
| CK | minpwh | 0.1613 | 0.1176 | 0.1078 | 0.0933 |
| | minpwl | 0.1661 | 0.1613 | 0.1418 | 0.1224 |
| SN | minpwl | 0.1176 | 0.1321 | 0.1613 | 0.2390 |
| | recovery | 0.0508 | 0.0664 | 0.0664 | 0.0664 |
| | removal | 0.1445 | 0.1016 | 0.1055 | 0.1094 |

Cell Description

The DFFSR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Logic Symbol



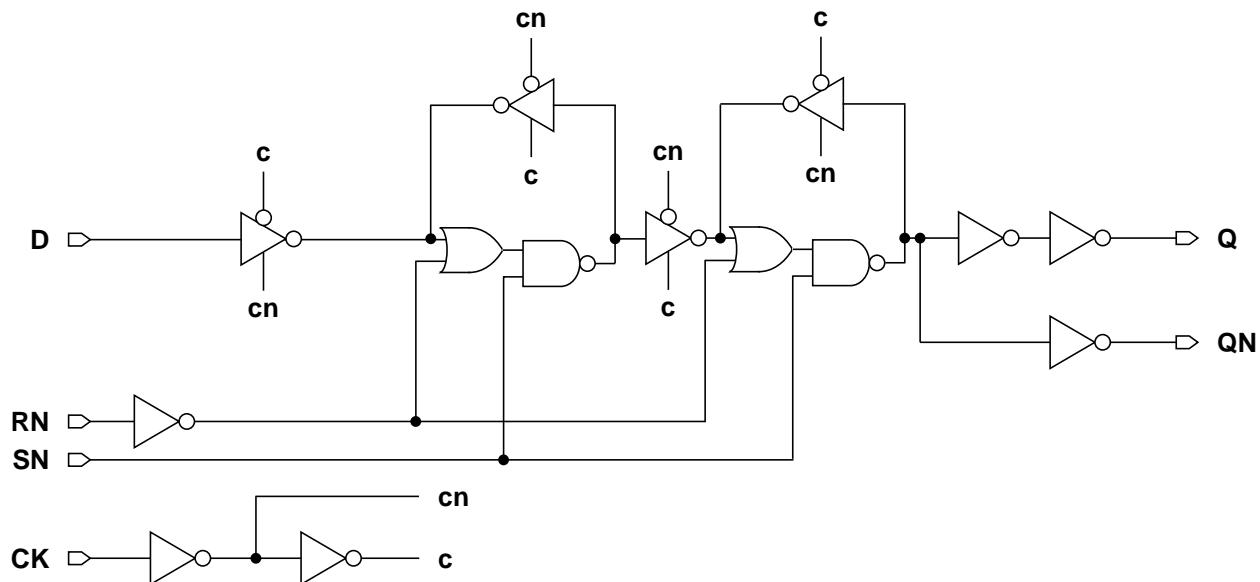
Functions

| RN | SN | D | CK | $Q[n+1]$ | $QN[n+1]$ |
|----|----|---|----|----------|-----------|
| 0 | 1 | x | x | 0 | 1 |
| 1 | 0 | x | x | 1 | 0 |
| 0 | 0 | x | x | 1 | 0 |
| 1 | 1 | 0 | ✓ | 0 | 1 |
| 1 | 1 | 1 | ✓ | 1 | 0 |
| 1 | 1 | x | ✗ | $Q[n]$ | $QN[n]$ |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DFFSRXL | 5.04 | 17.16 |
| DFFSRX1 | 5.04 | 17.16 |
| DFFSRX2 | 5.04 | 17.16 |
| DFFSRX4 | 5.04 | 23.76 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0391 | 0.0318 | 0.0364 | 0.0508 |
| CK | 0.0387 | 0.0361 | 0.0372 | 0.0496 |
| SN | 0.0095 | 0.0099 | 0.0132 | 0.0199 |
| RN | 0.0178 | 0.0193 | 0.0244 | 0.0421 |
| Q | 0.0529 | 0.0602 | 0.0923 | 0.1652 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0033 | 0.0022 | 0.0022 | 0.0033 |
| CK | 0.0026 | 0.0030 | 0.0033 | 0.0043 |
| SN | 0.0067 | 0.0071 | 0.0093 | 0.0157 |
| RN | 0.0026 | 0.0029 | 0.0039 | 0.0062 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|----------------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q \uparrow | 0.4326 | 0.3921 | 0.3763 | 0.3601 | 5.8855 | 4.2008 | 2.1526 | 1.0642 |
| CK → Q \downarrow | 0.3329 | 0.3349 | 0.3038 | 0.2922 | 3.4818 | 2.5354 | 1.2926 | 0.6464 |
| SN → Q \uparrow | 0.1949 | 0.1819 | 0.1746 | 0.1673 | 5.8840 | 4.2004 | 2.1525 | 1.0642 |
| SN → Q \downarrow | 0.2061 | 0.1933 | 0.1778 | 0.1714 | 3.4828 | 2.5357 | 1.2927 | 0.6464 |
| RN → Q \downarrow | 0.2982 | 0.2779 | 0.2475 | 0.2383 | 3.4830 | 2.5357 | 1.2927 | 0.6464 |
| CK → QN \uparrow | 0.2701 | 0.2605 | 0.2332 | 0.2238 | 5.9240 | 4.2125 | 2.1574 | 1.0672 |
| CK → QN \downarrow | 0.3928 | 0.3477 | 0.3206 | 0.3081 | 3.7796 | 2.6098 | 1.3199 | 0.6612 |
| SN → QN \uparrow | 0.1439 | 0.1199 | 0.1079 | 0.1032 | 5.9536 | 4.2250 | 2.1640 | 1.0713 |
| SN → QN \downarrow | 0.1527 | 0.1349 | 0.1188 | 0.1156 | 3.5793 | 2.5617 | 1.3050 | 0.6560 |
| RN → QN \uparrow | 0.2358 | 0.2042 | 0.1774 | 0.1700 | 5.9518 | 4.2244 | 2.1637 | 1.0712 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0820 | 0.1367 | 0.1211 | 0.0859 |
| | setup↓ → CK | 0.1133 | 0.1758 | 0.1836 | 0.1523 |
| | hold↑ → CK | -0.0586 | -0.0898 | -0.0820 | -0.0586 |
| | hold↓ → CK | 0.0078 | -0.0312 | -0.0469 | -0.0273 |
| CK | minpwh | 0.1273 | 0.1418 | 0.1176 | 0.1127 |
| | minpwl | 0.1904 | 0.2050 | 0.1953 | 0.1564 |
| SN | minpwl | 0.1516 | 0.1370 | 0.1370 | 0.1759 |
| | recovery | -0.0039 | 0.0117 | 0.0156 | 0.0156 |
| | removal | 0.1289 | 0.0977 | 0.0977 | 0.1016 |
| RN | minpwl | 0.2147 | 0.1904 | 0.2050 | 0.3216 |
| | recovery | 0.0625 | 0.1172 | 0.0859 | 0.0703 |
| | removal | -0.0430 | -0.0820 | -0.0586 | -0.0352 |

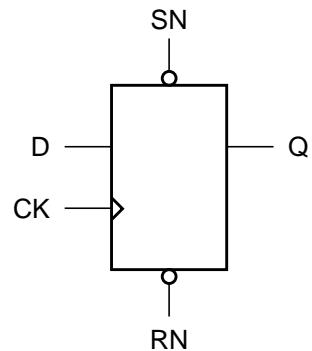
Cell Description

The DFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Functions

| RN | SN | D | CK | Q[n+1] |
|----|----|---|----|--------|
| 0 | 1 | x | x | 0 |
| 1 | 0 | x | x | 1 |
| 0 | 0 | x | x | 1 |
| 1 | 1 | 0 | / | 0 |
| 1 | 1 | 1 | / | 1 |
| 1 | 1 | x | / | Q[n] |

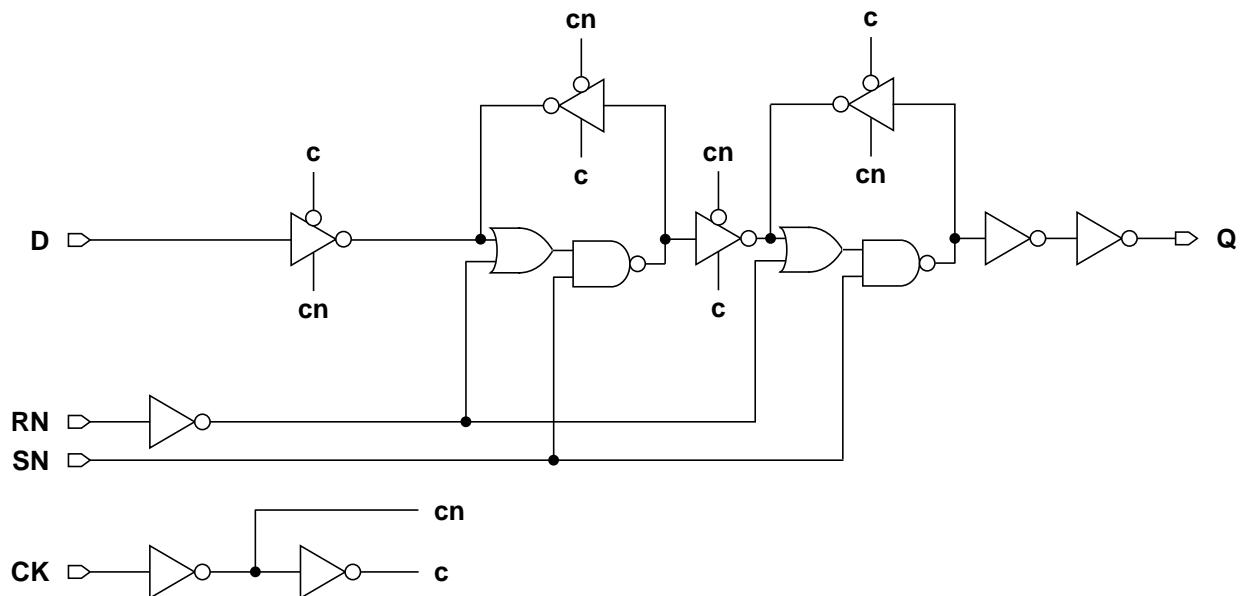
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFSRHQXL | 5.04 | 15.84 |
| DFFSRHQX1 | 5.04 | 15.84 |
| DFFSRHQX2 | 5.04 | 22.44 |
| DFFSRHQX4 | 5.04 | 30.36 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0392 | 0.0448 | 0.0678 | 0.1160 |
| CK | 0.0382 | 0.0382 | 0.0495 | 0.0733 |
| SN | 0.0133 | 0.0147 | 0.0204 | 0.0342 |
| RN | 0.0249 | 0.0300 | 0.0448 | 0.0726 |
| Q | 0.0366 | 0.0399 | 0.0592 | 0.1010 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0036 | 0.0025 | 0.0034 | 0.0052 |
| CK | 0.0025 | 0.0034 | 0.0047 | 0.0070 |
| SN | 0.0115 | 0.0125 | 0.0179 | 0.0294 |
| RN | 0.0029 | 0.0042 | 0.0062 | 0.0107 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2554 | 0.2066 | 0.1953 | 0.1820 | 8.7386 | 6.0794 | 3.0395 | 1.5196 |
| CK → Q↓ | 0.2477 | 0.1689 | 0.1618 | 0.1496 | 4.3773 | 2.9711 | 1.5009 | 0.7522 |
| SN → Q↑ | 0.0792 | 0.0863 | 0.0913 | 0.0915 | 3.8072 | 2.6433 | 1.3665 | 0.7330 |
| SN → Q↓ | 0.0558 | 0.0598 | 0.0551 | 0.0453 | 3.8928 | 2.6462 | 1.4219 | 0.7491 |
| RN → Q↓ | 0.1874 | 0.1398 | 0.1224 | 0.1070 | 3.9171 | 2.6425 | 1.4196 | 0.7481 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0977 | 0.1367 | 0.1328 | 0.1250 |
| | setup↓ → CK | 0.1602 | 0.2109 | 0.2031 | 0.1953 |
| | hold↑ → CK | -0.0273 | -0.0547 | -0.0469 | -0.0391 |
| | hold↓ → CK | 0.0195 | -0.0195 | -0.0156 | -0.0117 |
| CK | minpwh | 0.1613 | 0.1176 | 0.1078 | 0.0933 |
| | minpw1 | 0.1807 | 0.1710 | 0.1467 | 0.1321 |
| SN | minpw1 | 0.1273 | 0.1467 | 0.1856 | 0.2730 |
| | recovery | 0.0586 | 0.0742 | 0.0781 | 0.0820 |
| | removal | 0.1367 | 0.0938 | 0.1016 | 0.1055 |
| RN | minpw1 | 0.2633 | 0.2001 | 0.2924 | 0.4916 |
| | recovery | 0.1016 | 0.1328 | 0.1289 | 0.1211 |
| | removal | -0.0312 | -0.0586 | -0.0391 | -0.0195 |

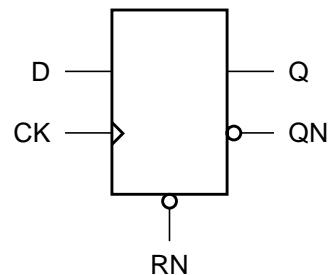
Cell Description

The DFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-low reset (RN).

Functions

| RN | D | CK | Q[n+1] | QN[n+1] |
|----|---|----|--------|---------|
| 0 | x | — | 0 | 1 |
| x | x | — | Q[n] | QN[n] |
| 1 | 0 | — | 0 | 1 |
| 1 | 1 | — | 1 | 0 |

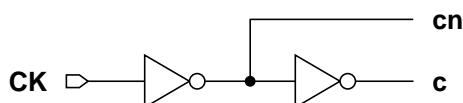
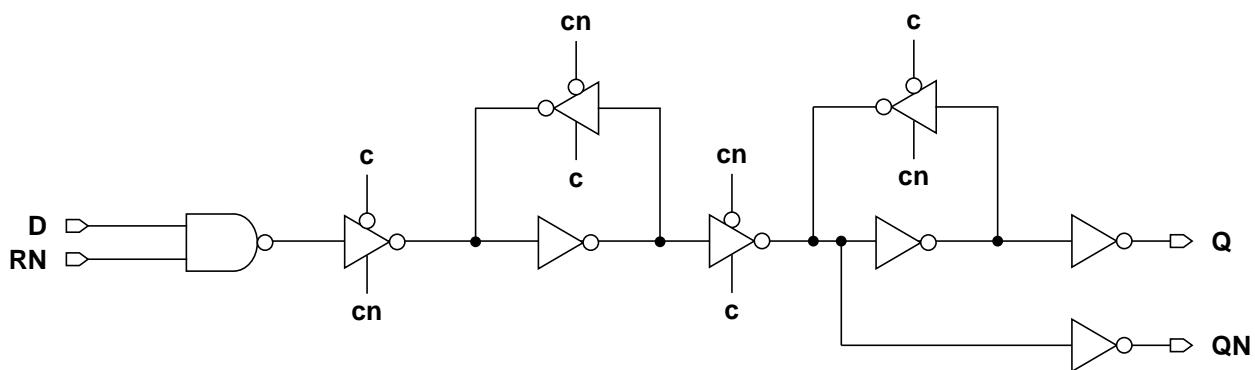
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| DFFTRXL | 5.04 | 11.22 |
| DFFTRX1 | 5.04 | 11.22 |
| DFFTRX2 | 5.04 | 13.86 |
| DFFTRX4 | 5.04 | 16.50 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0318 | 0.0307 | 0.0383 | 0.0607 |
| CK | 0.0366 | 0.0366 | 0.0440 | 0.0635 |
| RN | 0.0342 | 0.0328 | 0.0404 | 0.0636 |
| Q | 0.0346 | 0.0426 | 0.0715 | 0.1187 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0031 | 0.0025 | 0.0025 | 0.0034 |
| CK | 0.0026 | 0.0033 | 0.0043 | 0.0067 |
| RN | 0.0027 | 0.0021 | 0.0022 | 0.0030 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2338 | 0.2166 | 0.2096 | 0.1736 | 5.8937 | 4.2048 | 2.1313 | 1.0658 |
| CK → Q↓ | 0.1798 | 0.1634 | 0.1532 | 0.1415 | 3.5794 | 2.5646 | 1.3102 | 0.6533 |
| CK → QN↑ | 0.2310 | 0.2171 | 0.2130 | 0.1943 | 5.8945 | 4.2048 | 2.1284 | 1.0641 |
| CK → QN↓ | 0.3063 | 0.2925 | 0.2886 | 0.2415 | 3.5027 | 2.5411 | 1.2951 | 0.6464 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.0742 | 0.1016 | 0.1094 | 0.0977 |
| | setup↓ → CK | 0.1445 | 0.2109 | 0.2148 | 0.1836 |
| | hold↑ → CK | -0.0625 | -0.0781 | -0.0820 | -0.0703 |
| | hold↓ → CK | -0.0352 | -0.1055 | -0.1016 | -0.0859 |
| CK | minpwh | 0.1176 | 0.1176 | 0.1176 | 0.0933 |
| | minpwl | 0.2050 | 0.1856 | 0.1856 | 0.1564 |
| RN | setup↑ → CK | 0.0820 | 0.1055 | 0.1133 | 0.1016 |
| | setup↓ → CK | 0.1523 | 0.2305 | 0.2305 | 0.1992 |
| | hold↑ → CK | -0.0625 | -0.0820 | -0.0898 | -0.0742 |
| | hold↓ → CK | -0.0391 | -0.1172 | -0.1133 | -0.0938 |

Cell Description

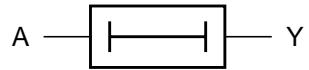
The DLY1 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

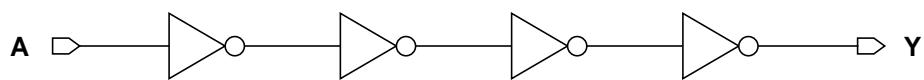
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DLY1X1 | 5.04 | 3.96 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) |
|-----|----------------------|
| | X1 |
| A | 0.0333 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|------------------|
| | X1 |
| A | 0.0022 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|--------------------|
| | X1 | X1 |
| A → Y↑ | 0.1449 | 4.2002 |
| A → Y↓ | 0.1701 | 2.5318 |

Cell Description

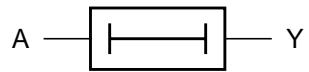
The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DLY2X1 | 5.04 | 3.96 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) |
|-----|----------------------|
| | X1 |
| A | 0.0400 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|------------------|
| | X1 |
| A | 0.0022 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|--------------------|
| | X1 | X1 |
| A → Y↑ | 0.2777 | 4.2123 |
| A → Y↓ | 0.3049 | 2.5993 |

Cell Description

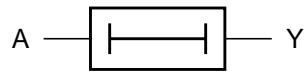
The DLY3 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DLY3X1 | 5.04 | 4.62 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) |
|-----|----------------------|
| | X1 |
| A | 0.0468 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|------------------|
| | X1 |
| A | 0.0022 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|--------------------|
| | X1 | X1 |
| A → Y↑ | 0.4397 | 4.2282 |
| A → Y↓ | 0.4444 | 2.6934 |

Cell Description

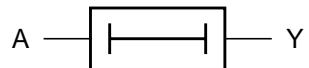
The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| DLY4X1 | 5.04 | 4.62 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) |
|-----|----------------------|
| | X1 |
| A | 0.0543 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|------------------|
| | X1 |
| A | 0.0022 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|--------------------|
| | X1 | X1 |
| A → Y↑ | 0.6375 | 4.2545 |
| A → Y↓ | 0.6026 | 2.8116 |

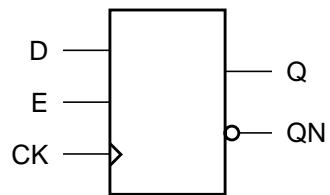
Cell Description

The EDFF cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E).

Functions

| E | D | CK | Q[n+1] | QN[n+1] |
|---|---|----|--------|---------|
| 0 | x | x | Q[n] | QN[n] |
| 1 | 0 | — | 0 | 1 |
| 1 | 1 | — | 1 | 0 |
| 1 | x | — | Q[n] | QN[n] |

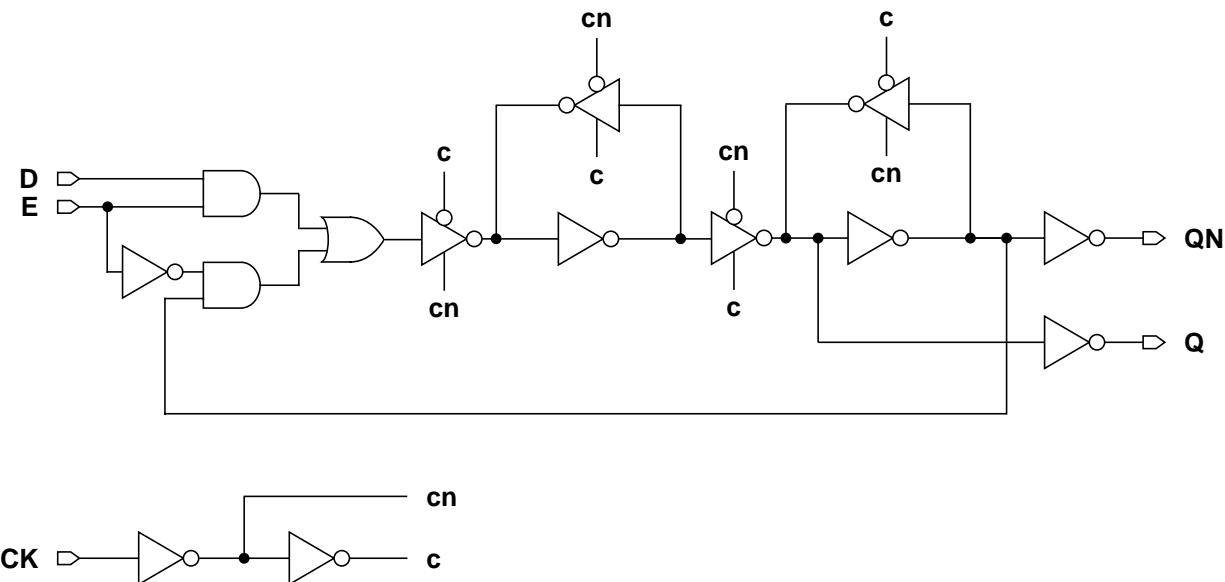
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| EDFFXL | 5.04 | 15.18 |
| EDFFX1 | 5.04 | 15.18 |
| EDFFX2 | 5.04 | 17.82 |
| EDFFX4 | 5.04 | 20.46 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0364 | 0.0355 | 0.0473 | 0.0735 |
| CK | 0.0433 | 0.0411 | 0.0483 | 0.0701 |
| E | 0.0531 | 0.0497 | 0.0619 | 0.0915 |
| Q | 0.0439 | 0.0505 | 0.0800 | 0.1384 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0031 | 0.0022 | 0.0026 | 0.0038 |
| CK | 0.0025 | 0.0032 | 0.0044 | 0.0071 |
| E | 0.0058 | 0.0050 | 0.0053 | 0.0064 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2479 | 0.2207 | 0.1943 | 0.1757 | 5.8884 | 4.7244 | 2.0954 | 1.0661 |
| CK → Q↓ | 0.1903 | 0.1628 | 0.1505 | 0.1431 | 3.5789 | 2.8119 | 1.3406 | 0.6544 |
| CK → QN↑ | 0.2727 | 0.2303 | 0.2156 | 0.2016 | 5.9027 | 4.2067 | 2.0932 | 1.0648 |
| CK → QN↓ | 0.3624 | 0.3125 | 0.2816 | 0.2525 | 3.5963 | 2.5563 | 1.3317 | 0.6481 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.1016 | 0.1172 | 0.1406 | 0.1289 |
| | setup↓ → CK | 0.2227 | 0.3867 | 0.3438 | 0.2891 |
| | hold↑ → CK | -0.0820 | -0.0938 | -0.1055 | -0.0938 |
| | hold↓ → CK | -0.1094 | -0.2500 | -0.2109 | -0.1758 |
| CK | minpwh | 0.1370 | 0.1224 | 0.1078 | 0.0933 |
| | minpwl | 0.2196 | 0.1953 | 0.1953 | 0.1759 |
| E | setup↑ → CK | 0.2617 | 0.4180 | 0.3789 | 0.3359 |
| | setup↓ → CK | 0.1602 | 0.2969 | 0.2578 | 0.2070 |
| | hold↑ → CK | -0.0977 | -0.1094 | -0.1250 | -0.1094 |
| | hold↓ → CK | -0.0977 | -0.1484 | -0.1641 | -0.1641 |

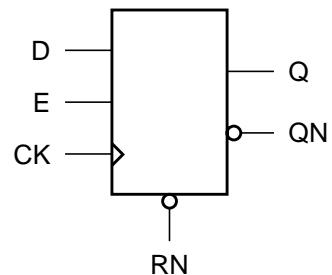
Cell Description

The EDFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E) and synchronous active-low reset (RN).

Functions

| RN | E | D | CK | Q[n+1] | QN[n+1] |
|----|---|---|-----|--------|---------|
| 0 | x | x | /\ | 0 | 1 |
| x | x | x | \/\ | Q[n] | QN[n] |
| 1 | 0 | x | /\ | Q[n] | QN[n] |
| 1 | 1 | 0 | /\ | 0 | 1 |
| 1 | 1 | 1 | /\ | 1 | 0 |

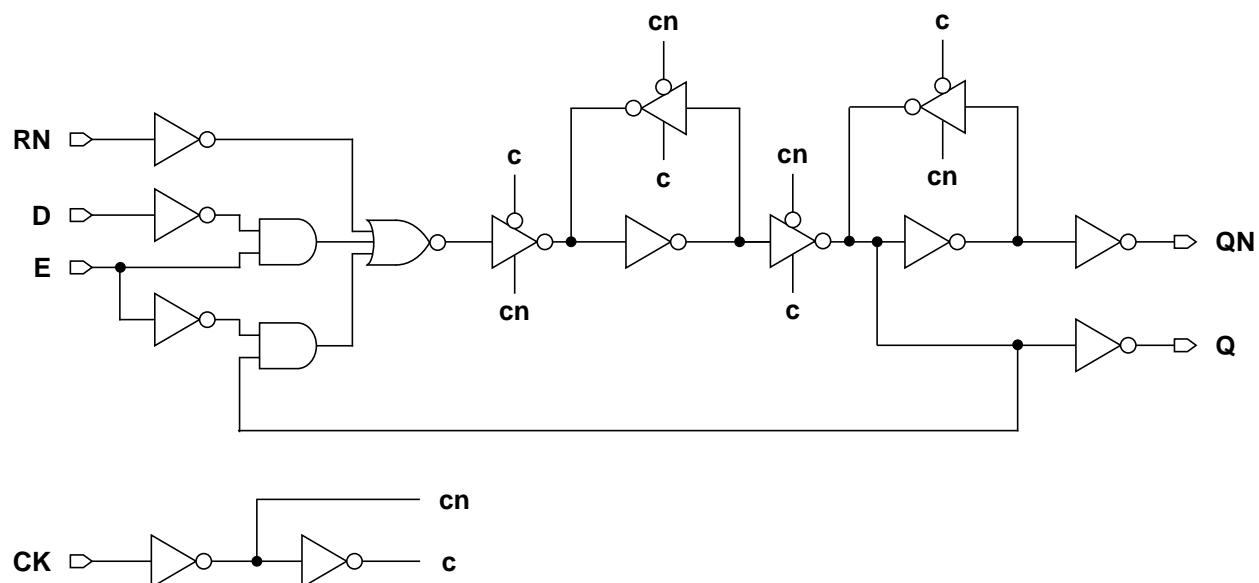
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| EDFFTRXL | 5.04 | 16.50 |
| EDFFTRX1 | 5.04 | 16.50 |
| EDFFTRX2 | 5.04 | 17.82 |
| EDFFTRX4 | 5.04 | 21.12 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0395 | 0.0375 | 0.0501 | 0.0801 |
| CK | 0.0476 | 0.0460 | 0.0544 | 0.0764 |
| E | 0.0577 | 0.0520 | 0.0657 | 0.0990 |
| RN | 0.0456 | 0.0421 | 0.0547 | 0.0866 |
| Q | 0.0455 | 0.0511 | 0.0795 | 0.1367 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0031 | 0.0022 | 0.0025 | 0.0039 |
| CK | 0.0027 | 0.0034 | 0.0046 | 0.0068 |
| E | 0.0064 | 0.0053 | 0.0058 | 0.0069 |
| RN | 0.0029 | 0.0022 | 0.0025 | 0.0038 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2585 | 0.2291 | 0.2062 | 0.1797 | 5.9060 | 4.2080 | 2.2485 | 1.0660 |
| CK → Q↓ | 0.2016 | 0.1736 | 0.1514 | 0.1398 | 3.3764 | 2.5748 | 1.3090 | 0.6543 |
| CK → QN↑ | 0.2978 | 0.2495 | 0.2160 | 0.1984 | 5.9083 | 4.2082 | 2.2467 | 1.0647 |
| CK → QN↓ | 0.3749 | 0.3287 | 0.2875 | 0.2572 | 3.5932 | 2.5592 | 1.2987 | 0.6484 |

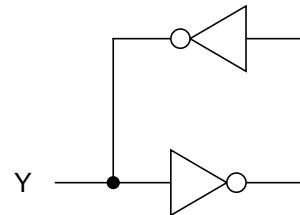
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → CK | 0.1367 | 0.1602 | 0.1758 | 0.1562 |
| | setup↓ → CK | 0.2461 | 0.4180 | 0.3672 | 0.3086 |
| | hold↑ → CK | -0.1055 | -0.1250 | -0.1406 | -0.1250 |
| | hold↓ → CK | -0.1211 | -0.2773 | -0.2383 | -0.1914 |
| CK | minpwh | 0.1418 | 0.1224 | 0.1127 | 0.0981 |
| | minpw1 | 0.2633 | 0.2439 | 0.2342 | 0.2001 |
| E | setup↑ → CK | 0.2852 | 0.4414 | 0.3945 | 0.3438 |
| | setup↓ → CK | 0.1992 | 0.3438 | 0.2930 | 0.2305 |
| | hold↑ → CK | -0.1328 | -0.1523 | -0.1641 | -0.1406 |
| | hold↓ → CK | -0.1211 | -0.1914 | -0.2109 | -0.1992 |
| RN | setup↑ → CK | 0.1523 | 0.1836 | 0.1914 | 0.1719 |
| | setup↓ → CK | 0.2148 | 0.3320 | 0.3047 | 0.2617 |
| | hold↑ → CK | -0.1250 | -0.1523 | -0.1562 | -0.1367 |
| | hold↓ → CK | -0.0664 | -0.1836 | -0.1680 | -0.1367 |

Cell Description

The HOLD cell holds data at a known value. This cell is often used for holding data on a tri-state bus.

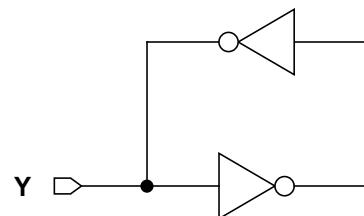
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| HOLDX1 | 5.04 | 2.64 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) |
|-----|-------------------------|
| | X1 |
| Y | 0.0293 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|---------------------|
| | X1 |
| Y | 0.0587 |

Cell Description

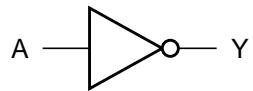
The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$$Y = \bar{A}$$

Functions

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

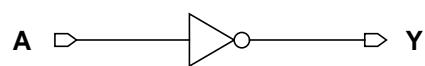
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| INVXL | 5.04 | 1.32 |
| INVX1 | 5.04 | 1.32 |
| INVX2 | 5.04 | 1.98 |
| INVX3 | 5.04 | 2.64 |
| INVX4 | 5.04 | 2.64 |
| INVX8 | 5.04 | 3.96 |
| INVX12 | 5.04 | 8.58 |
| INVX16 | 5.04 | 11.22 |
| INVX20 | 5.04 | 12.54 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | | | | | | |
|-----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0083 | 0.0112 | 0.0219 | 0.0323 | 0.0399 | 0.0797 | 0.1751 | 0.2408 | 0.3015 |

Pin Capacitance

| Pin | Capacitance (pF) | | | | | | | | |
|-----|------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0029 | 0.0037 | 0.0072 | 0.0106 | 0.0139 | 0.0278 | 0.0070 | 0.0094 | 0.0113 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | | | | | |
|-------------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 0.0239 | 0.0231 | 0.0216 | 0.0222 | 0.0202 | 0.0196 | 0.1285 | 0.1259 | 0.1255 |
| A → Y↓ | 0.0148 | 0.0145 | 0.0137 | 0.0143 | 0.0126 | 0.0128 | 0.1230 | 0.1212 | 0.1190 |

| Description | K_{load} (ns/pF) | | | | | | | | |
|-------------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 5.8735 | 4.1949 | 2.0974 | 1.3919 | 1.0750 | 0.5193 | 0.3467 | 0.2600 | 0.2081 |
| A → Y↓ | 3.4127 | 2.5003 | 1.2768 | 0.8485 | 0.6385 | 0.3247 | 0.2224 | 0.1669 | 0.1334 |

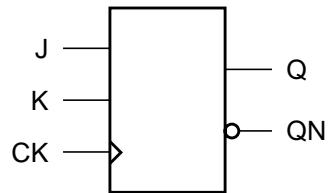
Cell Description

The JKFF cell is a positive-edge triggered JK-type flip-flop.

Functions

| J | K | CK | Q[n+1] | QN[n+1] |
|---|---|----|--------|---------|
| x | x | ✓ | Q[n] | QN[n] |
| 0 | 0 | ✓ | Q[n] | QN[n] |
| 0 | 1 | ✓ | 0 | 1 |
| 1 | 0 | ✓ | 1 | 0 |
| 1 | 1 | ✓ | QN[n] | Q[n] |

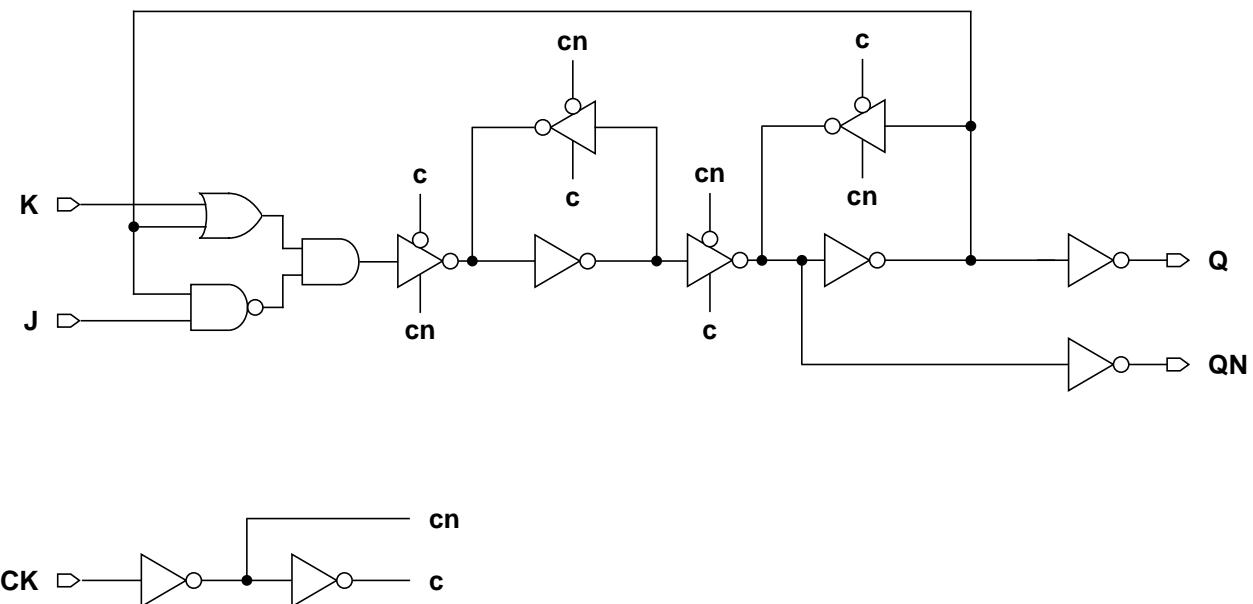
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| JKFFXL | 5.04 | 13.86 |
| JKFFX1 | 5.04 | 13.86 |
| JKFFX2 | 5.04 | 16.50 |
| JKFFX4 | 5.04 | 19.80 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0318 | 0.0308 | 0.0413 | 0.0669 |
| K | 0.0291 | 0.0275 | 0.0385 | 0.0593 |
| CK | 0.0390 | 0.0384 | 0.0477 | 0.0686 |
| Q | 0.0530 | 0.0551 | 0.0929 | 0.1484 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0017 | 0.0015 | 0.0016 | 0.0018 |
| K | 0.0031 | 0.0022 | 0.0025 | 0.0037 |
| CK | 0.0023 | 0.0031 | 0.0040 | 0.0072 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2809 | 0.2332 | 0.2263 | 0.1966 | 5.9135 | 4.2093 | 2.0816 | 1.0407 |
| CK → Q↓ | 0.3709 | 0.3191 | 0.2960 | 0.2546 | 3.6356 | 2.5656 | 1.2978 | 0.6483 |
| CK → QN↑ | 0.2384 | 0.2147 | 0.2121 | 0.1770 | 5.8949 | 4.6112 | 2.0835 | 1.0420 |
| CK → QN↓ | 0.1793 | 0.1573 | 0.1602 | 0.1384 | 3.5829 | 3.0033 | 1.3105 | 0.6540 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| J | setup↑ → CK | 0.1562 | 0.2344 | 0.2227 | 0.2227 |
| | setup↓ → CK | 0.1328 | 0.1484 | 0.1641 | 0.1758 |
| | hold↑ → CK | -0.0898 | -0.1758 | -0.1562 | -0.1484 |
| | hold↓ → CK | -0.1211 | -0.1367 | -0.1523 | -0.1641 |
| K | setup↑ → CK | 0.0938 | 0.1094 | 0.1211 | 0.1172 |
| | setup↓ → CK | 0.1289 | 0.3008 | 0.2383 | 0.1914 |
| | hold↑ → CK | -0.0898 | -0.0977 | -0.1172 | -0.1055 |
| | hold↓ → CK | -0.1094 | -0.2656 | -0.2070 | -0.1602 |
| CK | minpwh | 0.1370 | 0.1176 | 0.1224 | 0.0981 |
| | minpwl | 0.2001 | 0.2390 | 0.2196 | 0.1759 |

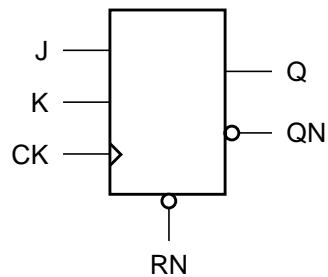
Cell Description

The JKFFR cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low reset (RN).

Functions

| RN | J | K | CK | Q[n+1] | QN[n+1] |
|----|---|---|----|--------|---------|
| 1 | x | x | ↖ | Q[n] | QN[n] |
| 0 | x | x | x | 0 | 1 |
| 1 | 0 | 0 | ↙ | Q[n] | QN[n] |
| 1 | 0 | 1 | ↙ | 0 | 1 |
| 1 | 1 | 0 | ↙ | 1 | 0 |
| 1 | 1 | 1 | ↙ | QN[n] | Q[n] |

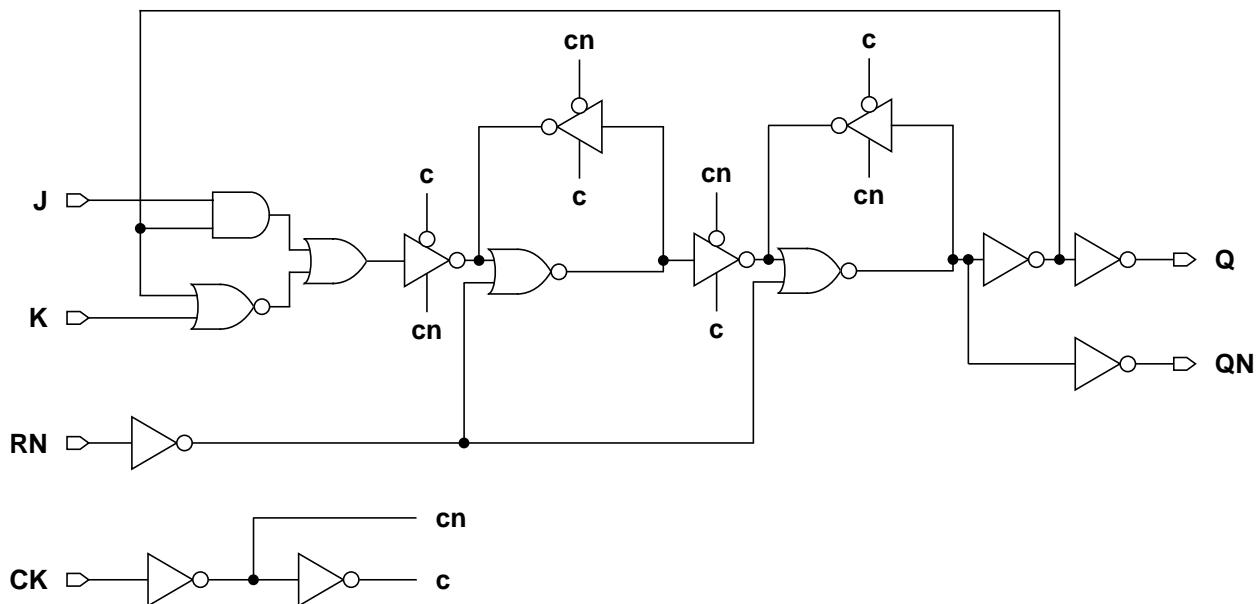
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| JKFFRXL | 5.04 | 17.16 |
| JKFFRX1 | 5.04 | 18.48 |
| JKFFRX2 | 5.04 | 18.48 |
| JKFFRX4 | 5.04 | 23.10 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0309 | 0.0271 | 0.0290 | 0.0416 |
| K | 0.0363 | 0.0320 | 0.0348 | 0.0474 |
| CK | 0.0405 | 0.0390 | 0.0409 | 0.0478 |
| RN | 0.0178 | 0.0199 | 0.0235 | 0.0378 |
| Q | 0.0780 | 0.0829 | 0.1213 | 0.1876 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0030 | 0.0022 | 0.0021 | 0.0025 |
| K | 0.0028 | 0.0027 | 0.0027 | 0.0028 |
| CK | 0.0024 | 0.0029 | 0.0032 | 0.0043 |
| RN | 0.0026 | 0.0029 | 0.0036 | 0.0062 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.5029 | 0.4525 | 0.4240 | 0.3671 | 5.9093 | 4.2114 | 2.0832 | 1.0412 |
| CK → Q↓ | 0.3800 | 0.3793 | 0.3372 | 0.2937 | 3.6284 | 2.5841 | 1.3041 | 0.6387 |
| RN → Q↓ | 0.3418 | 0.3171 | 0.2762 | 0.2489 | 3.6227 | 2.5808 | 1.3027 | 0.6380 |
| CK → QN↑ | 0.2403 | 0.2472 | 0.2335 | 0.2095 | 5.8852 | 4.2022 | 2.0822 | 1.0412 |
| CK → QN↓ | 0.3887 | 0.3522 | 0.3420 | 0.2979 | 3.7015 | 2.7056 | 1.3206 | 0.6473 |
| RN → QN↑ | 0.1980 | 0.1819 | 0.1708 | 0.1635 | 5.8915 | 4.2050 | 2.0849 | 1.0425 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| J | setup↑ → CK | 0.1211 | 0.1289 | 0.1445 | 0.1523 |
| | setup↓ → CK | 0.1133 | 0.2539 | 0.2617 | 0.2109 |
| | hold↑ → CK | -0.1133 | -0.1211 | -0.1328 | -0.1367 |
| | hold↓ → CK | -0.0781 | -0.2031 | -0.2031 | -0.1602 |
| K | setup↑ → CK | 0.1523 | 0.2383 | 0.2578 | 0.2383 |
| | setup↓ → CK | 0.1641 | 0.1562 | 0.1680 | 0.1836 |
| | hold↑ → CK | -0.0820 | -0.1875 | -0.1953 | -0.1641 |
| | hold↓ → CK | -0.1562 | -0.1445 | -0.1523 | -0.1719 |
| CK | minpwh | 0.1273 | 0.1370 | 0.1273 | 0.1127 |
| | minpwl | 0.2390 | 0.2196 | 0.2244 | 0.2099 |
| RN | minpwl | 0.1904 | 0.1807 | 0.2196 | 0.2973 |
| | recovery | 0.0508 | 0.0625 | 0.0781 | 0.0703 |

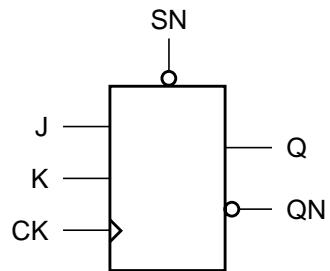
Cell Description

The JKFFS cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low set (SN).

Functions

| SN | J | K | CK | Q[n+1] | QN[n+1] |
|----|---|---|----|--------|---------|
| 1 | x | x | ↖ | Q[n] | QN[n] |
| 0 | x | x | x | 1 | 0 |
| 1 | 0 | 0 | ↙ | Q[n] | QN[n] |
| 1 | 0 | 1 | ↙ | 0 | 1 |
| 1 | 1 | 0 | ↙ | 1 | 0 |
| 1 | 1 | 1 | ↙ | QN[n] | Q[n] |

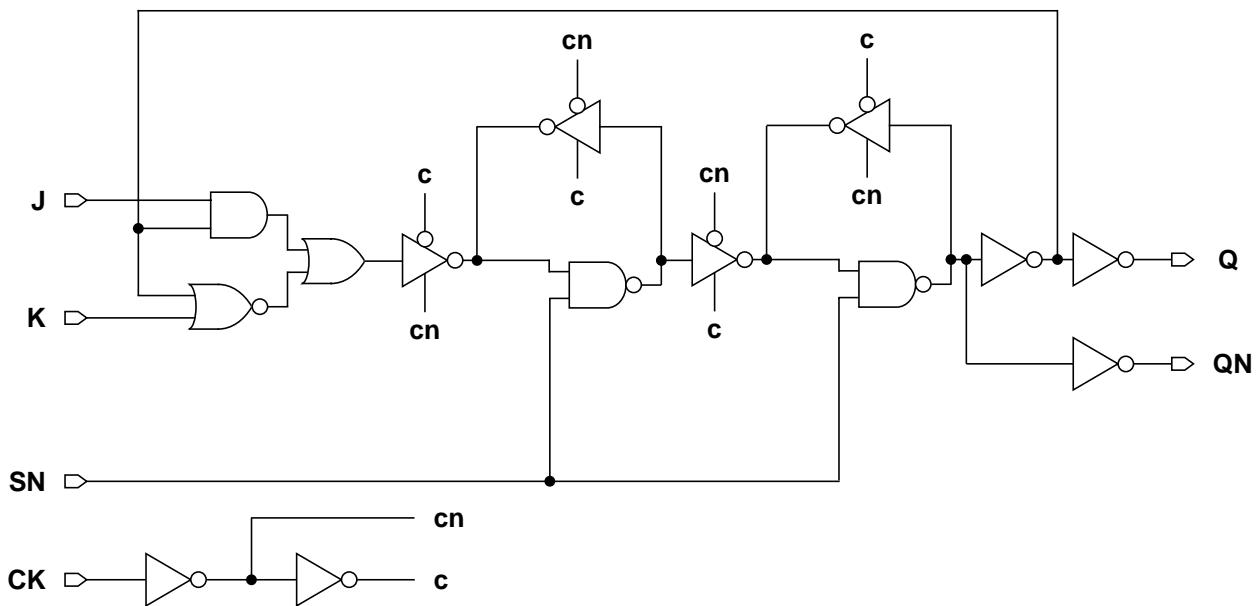
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| JKFFSXL | 5.04 | 16.50 |
| JKFFSX1 | 5.04 | 17.16 |
| JKFFSX2 | 5.04 | 17.82 |
| JKFFSX4 | 5.04 | 20.46 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0297 | 0.0247 | 0.0269 | 0.0316 |
| K | 0.0393 | 0.0331 | 0.0364 | 0.0432 |
| CK | 0.0402 | 0.0374 | 0.0390 | 0.0434 |
| SN | 0.0055 | 0.0068 | 0.0093 | 0.0162 |
| Q | 0.0748 | 0.0838 | 0.1093 | 0.1768 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0029 | 0.0020 | 0.0020 | 0.0022 |
| K | 0.0027 | 0.0027 | 0.0027 | 0.0027 |
| CK | 0.0025 | 0.0028 | 0.0031 | 0.0038 |
| SN | 0.0056 | 0.0066 | 0.0084 | 0.0130 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.4536 | 0.4018 | 0.3821 | 0.3520 | 5.9102 | 4.2078 | 2.1688 | 1.0407 |
| CK → Q↓ | 0.4093 | 0.3637 | 0.3305 | 0.2953 | 3.6328 | 2.5605 | 1.3045 | 0.6484 |
| SN → Q↑ | 0.2446 | 0.1960 | 0.1859 | 0.1622 | 5.9057 | 4.2069 | 2.1684 | 1.0406 |
| CK → QN↑ | 0.2611 | 0.2550 | 0.2259 | 0.2151 | 5.9244 | 4.4085 | 2.1710 | 1.0428 |
| CK → QN↓ | 0.3456 | 0.3195 | 0.3008 | 0.2901 | 3.5745 | 2.6315 | 1.2994 | 0.6493 |
| SN → QN↓ | 0.1405 | 0.1156 | 0.1063 | 0.1013 | 3.5573 | 2.6313 | 1.3017 | 0.6517 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| J | setup↑ → CK | 0.1094 | 0.1250 | 0.1289 | 0.1406 |
| | setup↓ → CK | 0.1289 | 0.2891 | 0.3047 | 0.2266 |
| | hold↑ → CK | -0.1055 | -0.1172 | -0.1211 | -0.1289 |
| | hold↓ → CK | -0.1094 | -0.2578 | -0.2695 | -0.1992 |
| K | setup↑ → CK | 0.1797 | 0.2852 | 0.3008 | 0.2500 |
| | setup↓ → CK | 0.1562 | 0.1523 | 0.1523 | 0.1641 |
| | hold↑ → CK | -0.0938 | -0.2188 | -0.2305 | -0.1758 |
| | hold↓ → CK | -0.1484 | -0.1406 | -0.1445 | -0.1562 |
| CK | minpwh | 0.1321 | 0.1370 | 0.1273 | 0.1224 |
| | minpwl | 0.2147 | 0.2099 | 0.2050 | 0.2001 |
| SN | minpwl | 0.1564 | 0.1321 | 0.1321 | 0.1516 |
| | recovery | -0.0312 | -0.0117 | -0.0039 | -0.0039 |

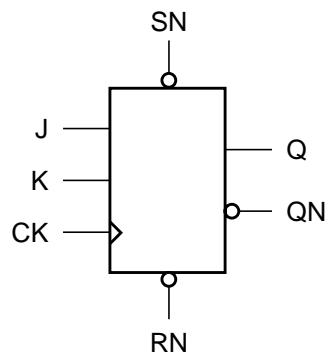
Cell Description

The JKFFSR cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Functions

| RN | SN | J | K | CK | Q[n+1] | QN[n+1] |
|----|----|---|---|----|--------|---------|
| 1 | 1 | x | x | — | Q[n] | QN[n] |
| 1 | 0 | x | x | x | 1 | 0 |
| 0 | 1 | x | x | x | 0 | 1 |
| 0 | 0 | x | x | x | 1 | 0 |
| 1 | 1 | 0 | 0 | — | Q[n] | QN[n] |
| 1 | 1 | 0 | 1 | — | 0 | 1 |
| 1 | 1 | 1 | 0 | — | 1 | 0 |
| 1 | 1 | 1 | 1 | — | QN[n] | Q[n] |

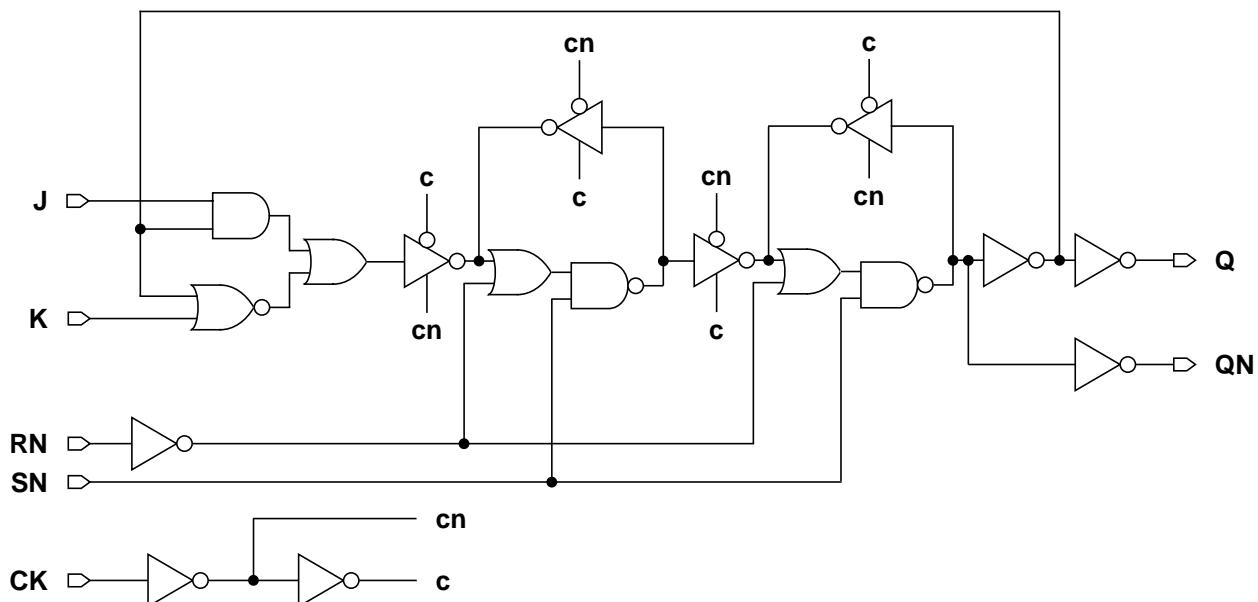
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| JKFFSRXL | 5.04 | 19.80 |
| JKFFSRX1 | 5.04 | 19.80 |
| JKFFSRX2 | 5.04 | 20.46 |
| JKFFSRX4 | 5.04 | 21.78 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0346 | 0.0295 | 0.0327 | 0.0327 |
| K | 0.0392 | 0.0337 | 0.0391 | 0.0390 |
| CK | 0.0410 | 0.0392 | 0.0410 | 0.0414 |
| SN | 0.0053 | 0.0061 | 0.0096 | 0.0096 |
| RN | 0.0160 | 0.0178 | 0.0231 | 0.0231 |
| Q | 0.0824 | 0.0874 | 0.1234 | 0.1820 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| J | 0.0029 | 0.0020 | 0.0022 | 0.0022 |
| K | 0.0029 | 0.0029 | 0.0029 | 0.0029 |
| CK | 0.0023 | 0.0027 | 0.0031 | 0.0031 |
| SN | 0.0048 | 0.0054 | 0.0074 | 0.0074 |
| RN | 0.0028 | 0.0031 | 0.0042 | 0.0042 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.5586 | 0.4692 | 0.4512 | 0.4983 | 5.9170 | 4.2091 | 2.1302 | 1.0471 |
| CK → Q↓ | 0.4421 | 0.3806 | 0.3587 | 0.3965 | 3.6513 | 2.5614 | 1.3004 | 0.6316 |
| SN → Q↑ | 0.2527 | 0.2111 | 0.1880 | 0.2198 | 5.9125 | 4.2076 | 2.1295 | 1.0469 |
| SN → Q↓ | 0.2954 | 0.2276 | 0.2200 | 0.2562 | 3.6363 | 2.5550 | 1.2982 | 0.6309 |
| RN → Q↓ | 0.3747 | 0.3013 | 0.2848 | 0.3211 | 3.6367 | 2.5550 | 1.2982 | 0.6309 |
| CK → QN↑ | 0.2964 | 0.2785 | 0.2655 | 0.2928 | 5.9228 | 4.7328 | 2.1355 | 1.0527 |
| CK → QN↓ | 0.4438 | 0.3911 | 0.3776 | 0.4179 | 3.7744 | 2.8948 | 1.3256 | 0.6549 |
| SN → QN↑ | 0.1482 | 0.1246 | 0.1260 | 0.1519 | 5.9503 | 4.7446 | 2.1413 | 1.0552 |
| SN → QN↓ | 0.1543 | 0.1375 | 0.1184 | 0.1448 | 3.5725 | 2.8555 | 1.3059 | 0.6379 |
| RN → QN↑ | 0.2274 | 0.1982 | 0.1907 | 0.2167 | 5.9494 | 4.7443 | 2.1412 | 1.0551 |

Timing Constraints at 25°C, 1.8V, Typical Process

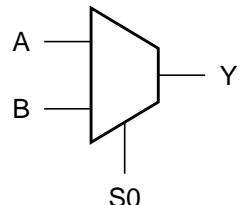
| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| J | setup↑ → CK | 0.1328 | 0.1758 | 0.1602 | 0.1602 |
| | setup↓ → CK | 0.1094 | 0.2617 | 0.2266 | 0.2188 |
| | hold↑ → CK | -0.1250 | -0.1562 | -0.1445 | -0.1445 |
| | hold↓ → CK | -0.0625 | -0.1914 | -0.1719 | -0.1719 |
| K | setup↑ → CK | 0.1680 | 0.2773 | 0.2539 | 0.2500 |
| | setup↓ → CK | 0.1797 | 0.1953 | 0.1836 | 0.1836 |
| | hold↑ → CK | -0.0820 | -0.1914 | -0.1719 | -0.1680 |
| | hold↓ → CK | -0.1680 | -0.1719 | -0.1680 | -0.1680 |
| CK | minpwh | 0.1467 | 0.1467 | 0.1467 | 0.1516 |
| | minpwl | 0.2584 | 0.2633 | 0.2342 | 0.2342 |
| SN | minpwl | 0.1661 | 0.1467 | 0.1370 | 0.1613 |
| | recovery | -0.0234 | 0.0000 | 0.0000 | -0.0039 |
| | removal | 0.1445 | 0.1094 | 0.1133 | 0.1133 |
| RN | minpwl | 0.2147 | 0.1904 | 0.2147 | 0.2342 |

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

Logic Symbol



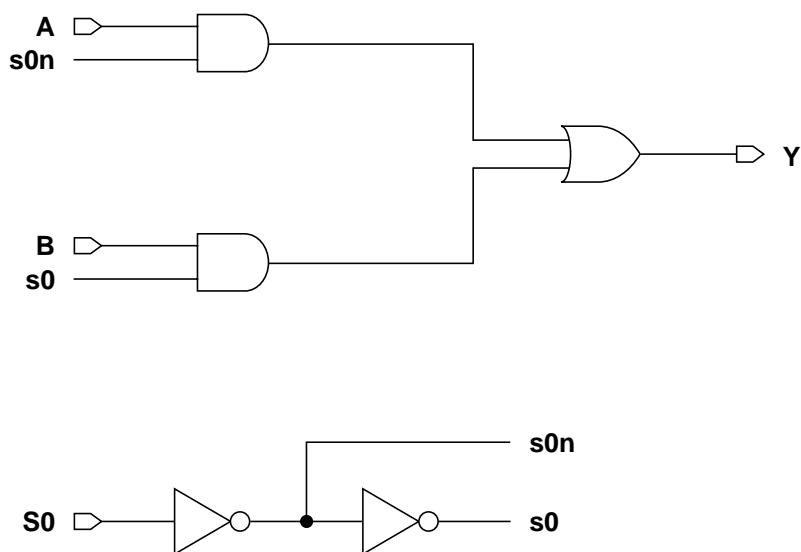
Functions

| S0 | A | B | Y |
|----|---|---|---|
| 0 | 0 | x | 0 |
| 0 | 1 | x | 1 |
| 1 | x | 0 | 0 |
| 1 | x | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| MX2XL | 5.04 | 5.28 |
| MX2X1 | 5.04 | 5.28 |
| MX2X2 | 5.04 | 5.94 |
| MX2X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0370 | 0.0374 | 0.0637 | 0.0931 |
| A | 0.0270 | 0.0311 | 0.0565 | 0.0876 |
| B | 0.0312 | 0.0349 | 0.0634 | 0.0971 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0067 | 0.0063 | 0.0092 | 0.0106 |
| A | 0.0026 | 0.0036 | 0.0060 | 0.0074 |
| B | 0.0026 | 0.0035 | 0.0055 | 0.0063 |

Delay Tables at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 → Y↑ | 0.1318 | 0.1258 | 0.1278 | 0.1375 |
| S0 → Y↓ | 0.1359 | 0.1190 | 0.1181 | 0.1400 |
| A → Y↑ | 0.1082 | 0.0949 | 0.0889 | 0.1028 |
| A → Y↓ | 0.1583 | 0.1258 | 0.1185 | 0.1333 |
| B → Y↑ | 0.1069 | 0.0922 | 0.0898 | 0.0992 |
| B → Y↓ | 0.1613 | 0.1291 | 0.1226 | 0.1463 |

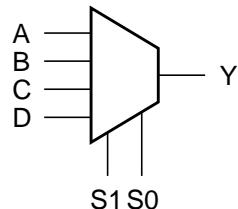
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 → Y↑ | 5.9002 | 4.2054 | 2.1179 | 1.0664 |
| S0 → Y↓ | 3.6682 | 2.5724 | 1.3118 | 0.6858 |
| A → Y↑ | 5.9004 | 4.2052 | 2.1180 | 1.0667 |
| A → Y↓ | 3.6630 | 2.5751 | 1.3120 | 0.6825 |
| B → Y↑ | 5.9012 | 4.2055 | 2.1185 | 1.0667 |
| B → Y↓ | 3.6691 | 2.5761 | 1.3119 | 0.6859 |

Cell Description

The MX4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \cdot \overline{S1} \cdot A) + (S0 \cdot \overline{S1} \cdot B) + (\overline{S0} \cdot S1 \cdot C) + (S0 \cdot S1 \cdot D)$$

Logic Symbol



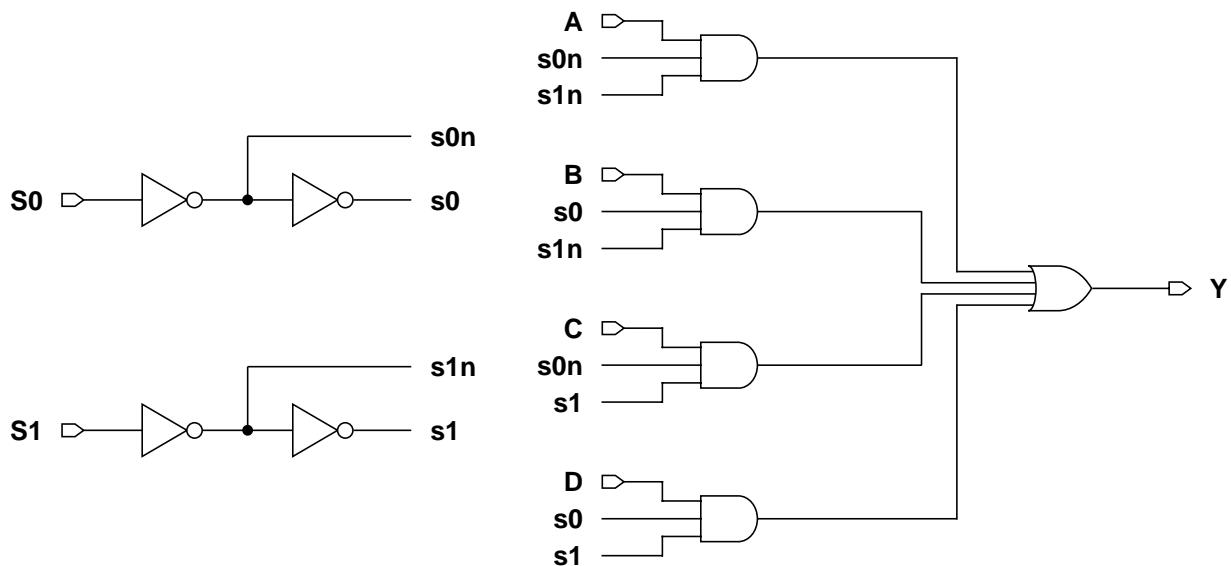
Functions

| S1 | S0 | A | B | C | D | Y |
|----|----|---|---|---|---|---|
| 0 | 0 | 0 | x | x | x | 0 |
| 0 | 0 | 1 | x | x | x | 1 |
| 0 | 1 | x | 0 | x | x | 0 |
| 0 | 1 | x | 1 | x | x | 1 |
| 1 | 0 | x | x | 0 | x | 0 |
| 1 | 0 | x | x | 1 | x | 1 |
| 1 | 1 | x | x | x | 0 | 0 |
| 1 | 1 | x | x | x | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| MX4XL | 5.04 | 13.20 |
| MX4X1 | 5.04 | 13.20 |
| MX4X2 | 5.04 | 15.18 |
| MX4X4 | 5.04 | 15.84 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0642 | 0.0788 | 0.1304 | 0.1662 |
| S1 | 0.0361 | 0.0441 | 0.0701 | 0.0925 |
| A | 0.0405 | 0.0531 | 0.0891 | 0.1222 |
| B | 0.0448 | 0.0583 | 0.0994 | 0.1346 |
| C | 0.0469 | 0.0598 | 0.1027 | 0.1391 |
| D | 0.0523 | 0.0661 | 0.1119 | 0.1479 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0113 | 0.0144 | 0.0233 | 0.0233 |
| S1 | 0.0066 | 0.0074 | 0.0113 | 0.0113 |
| A | 0.0024 | 0.0046 | 0.0070 | 0.0070 |
| B | 0.0023 | 0.0044 | 0.0068 | 0.0068 |
| C | 0.0023 | 0.0045 | 0.0071 | 0.0071 |
| D | 0.0024 | 0.0045 | 0.0069 | 0.0069 |

Delays at 25°C, 1.8V, Typical Process

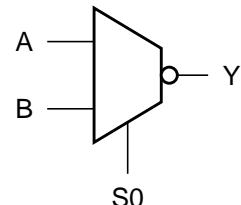
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| S0 → Y↑ | 0.2365 | 0.1784 | 0.1675 | 0.1846 | 5.9527 | 4.2176 | 2.1240 | 1.0467 |
| S0 → Y↓ | 0.2562 | 0.1932 | 0.1938 | 0.2242 | 4.0677 | 2.6700 | 1.3604 | 0.7149 |
| S1 → Y↑ | 0.1435 | 0.1390 | 0.1290 | 0.1451 | 5.9485 | 4.2159 | 2.1229 | 1.0465 |
| S1 → Y↓ | 0.1349 | 0.1313 | 0.1293 | 0.1584 | 4.0045 | 2.6587 | 1.3545 | 0.7128 |
| A → Y↑ | 0.1806 | 0.1408 | 0.1349 | 0.1537 | 5.9510 | 4.2172 | 2.1231 | 1.0463 |
| A → Y↓ | 0.2560 | 0.1821 | 0.1778 | 0.2076 | 4.0451 | 2.6667 | 1.3559 | 0.7127 |
| B → Y↑ | 0.1795 | 0.1393 | 0.1354 | 0.1545 | 5.9505 | 4.2170 | 2.1234 | 1.0467 |
| B → Y↓ | 0.2597 | 0.1856 | 0.1823 | 0.2123 | 4.0505 | 2.6679 | 1.3555 | 0.7123 |
| C → Y↑ | 0.1862 | 0.1427 | 0.1389 | 0.1567 | 5.9566 | 4.2182 | 2.1242 | 1.0468 |
| C → Y↓ | 0.2667 | 0.1901 | 0.1891 | 0.2189 | 4.0794 | 2.6724 | 1.3612 | 0.7151 |
| D → Y↑ | 0.1850 | 0.1405 | 0.1377 | 0.1556 | 5.9552 | 4.2178 | 2.1244 | 1.0469 |
| D → Y↓ | 0.2714 | 0.1935 | 0.1919 | 0.2217 | 4.0831 | 2.6730 | 1.3606 | 0.7147 |

Cell Description

The MXI2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

Logic Symbol



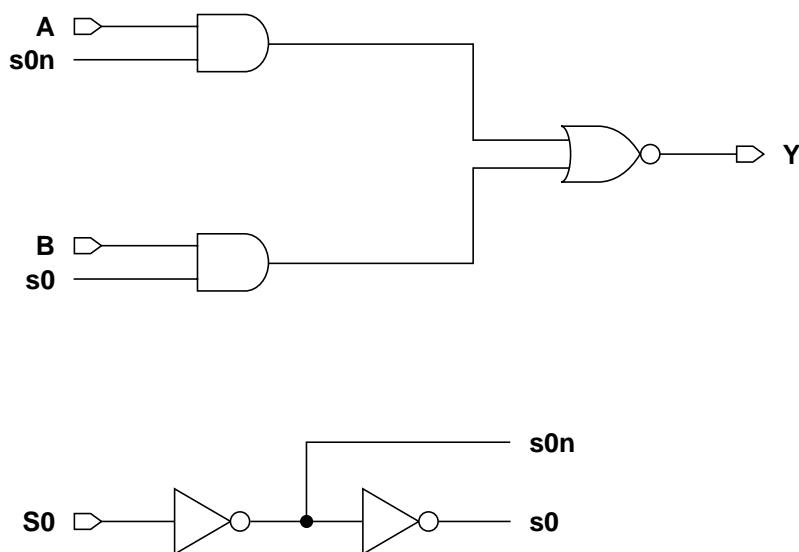
Functions

| S0 | A | B | Y |
|----|---|---|---|
| 0 | 0 | x | 1 |
| 0 | 1 | x | 0 |
| 1 | x | 0 | 1 |
| 1 | x | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| MXI2XL | 5.04 | 4.62 |
| MXI2X1 | 5.04 | 4.62 |
| MXI2X2 | 5.04 | 5.28 |
| MXI2X4 | 5.04 | 9.24 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0273 | 0.0322 | 0.0554 | 0.1012 |
| A | 0.0170 | 0.0221 | 0.0376 | 0.0798 |
| B | 0.0189 | 0.0266 | 0.0444 | 0.0971 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0067 | 0.0074 | 0.0103 | 0.0215 |
| A | 0.0029 | 0.0041 | 0.0071 | 0.0140 |
| B | 0.0023 | 0.0042 | 0.0065 | 0.0141 |

Delay Tables at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 → Y↑ | 0.0551 | 0.0551 | 0.0569 | 0.0527 |
| S0 → Y↓ | 0.0572 | 0.0695 | 0.0599 | 0.0638 |
| A → Y↑ | 0.0629 | 0.0518 | 0.0518 | 0.0506 |
| A → Y↓ | 0.0464 | 0.0418 | 0.0441 | 0.0434 |
| B → Y↑ | 0.0839 | 0.0551 | 0.0541 | 0.0558 |
| B → Y↓ | 0.0500 | 0.0385 | 0.0442 | 0.0397 |

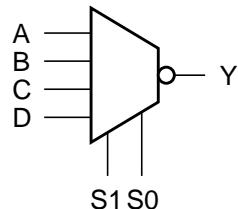
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 → Y↑ | 9.0115 | 4.5821 | 2.6375 | 1.2829 |
| S0 → Y↓ | 4.6442 | 2.9093 | 1.9240 | 0.8438 |
| A → Y↑ | 6.6632 | 4.6085 | 2.6472 | 1.2893 |
| A → Y↓ | 4.0824 | 2.9797 | 1.7527 | 0.8601 |
| B → Y↑ | 9.1888 | 4.6088 | 2.6881 | 1.2871 |
| B → Y↓ | 4.9305 | 2.9784 | 1.9952 | 0.8578 |

Cell Description

The MXI4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S_1 , S_0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S_0} \cdot \overline{S_1} \cdot A)} + (S_0 \cdot \overline{S_1} \cdot B) + (\overline{S_0} \cdot S_1 \cdot C) + (S_0 \cdot S_1 \cdot D)$$

Logic Symbol



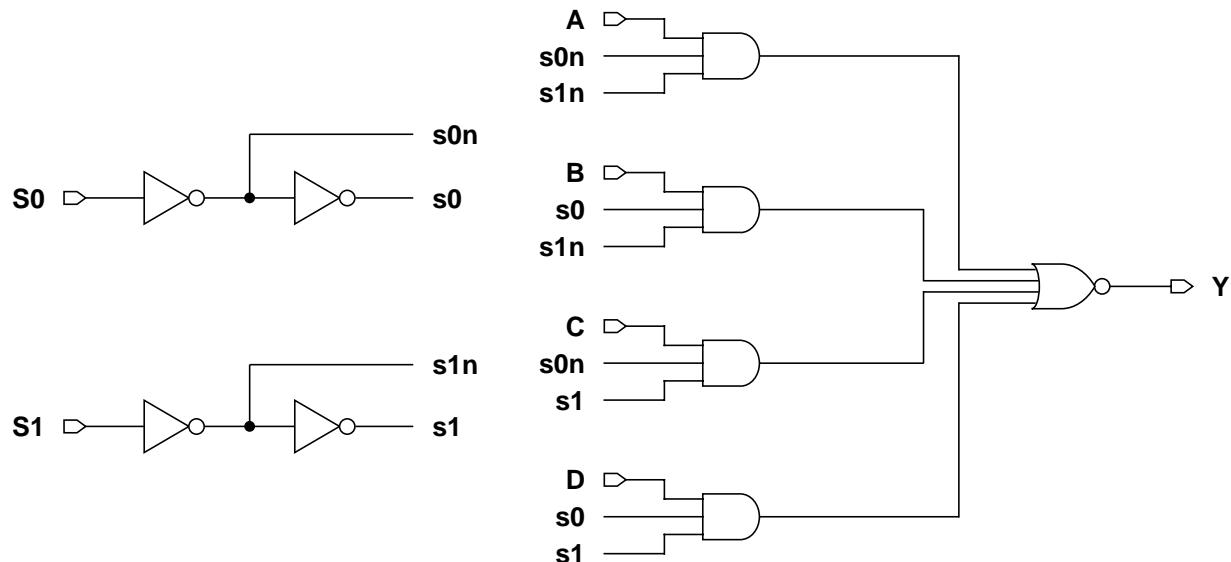
Functions

| S1 | S0 | A | B | C | D | Y |
|----|----|---|---|---|---|---|
| 0 | 0 | 0 | x | x | x | 1 |
| 0 | 0 | 1 | x | x | x | 0 |
| 0 | 1 | x | 0 | x | x | 1 |
| 0 | 1 | x | 1 | x | x | 0 |
| 1 | 0 | x | x | 0 | x | 1 |
| 1 | 0 | x | x | 1 | x | 0 |
| 1 | 1 | x | x | x | 0 | 1 |
| 1 | 1 | x | x | x | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| MXI4XL | 5.04 | 15.18 |
| MXI4X1 | 5.04 | 15.18 |
| MXI4X2 | 5.04 | 15.84 |
| MXI4X4 | 5.04 | 16.50 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0743 | 0.0700 | 0.1182 | 0.1610 |
| S1 | 0.0381 | 0.0387 | 0.0625 | 0.0868 |
| A | 0.0458 | 0.0482 | 0.0873 | 0.1218 |
| B | 0.0503 | 0.0516 | 0.0947 | 0.1296 |
| C | 0.0458 | 0.0463 | 0.0807 | 0.1156 |
| D | 0.0427 | 0.0445 | 0.0799 | 0.1107 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S0 | 0.0111 | 0.0095 | 0.0148 | 0.0176 |
| S1 | 0.0047 | 0.0046 | 0.0055 | 0.0064 |
| A | 0.0024 | 0.0028 | 0.0047 | 0.0058 |
| B | 0.0024 | 0.0028 | 0.0047 | 0.0059 |
| C | 0.0026 | 0.0030 | 0.0050 | 0.0060 |
| D | 0.0023 | 0.0027 | 0.0047 | 0.0057 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| S0 → Y↑ | 0.2701 | 0.2326 | 0.2119 | 0.2199 | 5.9099 | 4.2092 | 2.1813 | 1.0607 |
| S0 → Y↓ | 0.3161 | 0.2678 | 0.2384 | 0.2491 | 3.6976 | 2.5861 | 1.3136 | 0.6620 |
| S1 → Y↑ | 0.1426 | 0.1350 | 0.1297 | 0.1342 | 5.9056 | 4.2073 | 2.1806 | 1.0603 |
| S1 → Y↓ | 0.1487 | 0.1262 | 0.1167 | 0.1278 | 3.6913 | 2.5842 | 1.3102 | 0.6611 |
| A → Y↑ | 0.2791 | 0.2331 | 0.2117 | 0.2203 | 5.9100 | 4.2092 | 2.1814 | 1.0607 |
| A → Y↓ | 0.2628 | 0.2185 | 0.2006 | 0.2167 | 3.6973 | 2.5859 | 1.3135 | 0.6621 |
| B → Y↑ | 0.2812 | 0.2352 | 0.2159 | 0.2242 | 5.9100 | 4.2093 | 2.1813 | 1.0607 |
| B → Y↓ | 0.2610 | 0.2156 | 0.1994 | 0.2137 | 3.6970 | 2.5860 | 1.3135 | 0.6620 |
| C → Y↑ | 0.2613 | 0.2175 | 0.1931 | 0.1947 | 5.9073 | 4.2084 | 2.1809 | 1.0602 |
| C → Y↓ | 0.2529 | 0.2109 | 0.1897 | 0.2047 | 3.6927 | 2.5850 | 1.3106 | 0.6618 |
| D → Y↑ | 0.2625 | 0.2191 | 0.1942 | 0.1988 | 5.9073 | 4.2084 | 2.1809 | 1.0602 |
| D → Y↓ | 0.2508 | 0.2082 | 0.1907 | 0.2022 | 3.6924 | 2.5849 | 1.3106 | 0.6618 |

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B)}$$

Logic Symbol



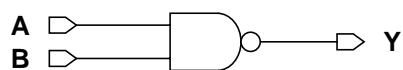
Functions

| A | B | Y |
|---|---|---|
| 0 | x | 1 |
| x | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| NAND2XL | 5.04 | 1.98 |
| NAND2X1 | 5.04 | 1.98 |
| NAND2X2 | 5.04 | 3.30 |
| NAND2X4 | 5.04 | 4.62 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0102 | 0.0137 | 0.0264 | 0.0515 |
| B | 0.0137 | 0.0187 | 0.0372 | 0.0723 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0034 | 0.0043 | 0.0084 | 0.0166 |
| B | 0.0031 | 0.0040 | 0.0088 | 0.0162 |

Delay at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0305 | 0.0292 | 0.0273 | 0.0279 |
| A → Y↓ | 0.0203 | 0.0198 | 0.0186 | 0.0183 |
| B → Y↑ | 0.0382 | 0.0369 | 0.0366 | 0.0366 |
| B → Y↓ | 0.0250 | 0.0247 | 0.0248 | 0.0239 |

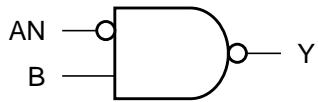
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8798 | 4.1977 | 2.0308 | 1.0645 |
| A → Y↓ | 4.0994 | 2.9980 | 1.4622 | 0.7370 |
| B → Y↑ | 5.8706 | 4.1941 | 2.0297 | 1.0638 |
| B → Y↓ | 4.1075 | 3.0021 | 1.4646 | 0.7381 |

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B)}$$

Logic Symbol



Functions

| AN | B | Y |
|----|---|---|
| 1 | x | 1 |
| x | 0 | 1 |
| 0 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| NAND2BXL | 5.04 | 2.64 |
| NAND2BX1 | 5.04 | 2.64 |
| NAND2BX2 | 5.04 | 3.96 |
| NAND2BX4 | 5.04 | 5.28 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0178 | 0.0212 | 0.0389 | 0.0747 |
| B | 0.0112 | 0.0145 | 0.0285 | 0.0551 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0024 | 0.0024 | 0.0037 | 0.0066 |
| B | 0.0032 | 0.0042 | 0.0089 | 0.0164 |

Delays at 25°C, 1.8V, Typical Process

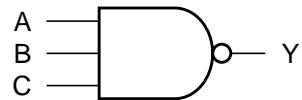
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0643 | 0.0675 | 0.0706 | 0.0704 | 5.8846 | 4.2013 | 2.0544 | 1.0657 |
| AN → Y↓ | 0.0844 | 0.0926 | 0.0910 | 0.0860 | 4.1388 | 2.9478 | 1.4740 | 0.7426 |
| B → Y↑ | 0.0382 | 0.0364 | 0.0360 | 0.0357 | 5.8768 | 4.1977 | 2.0873 | 1.0648 |
| B → Y↓ | 0.0276 | 0.0274 | 0.0277 | 0.0274 | 4.1186 | 2.9364 | 1.4685 | 0.7402 |

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C)}$$

Logic Symbol



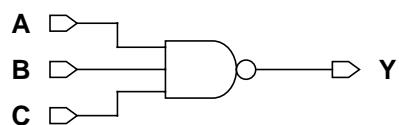
Functions

| A | B | C | Y |
|---|---|---|---|
| 0 | x | x | 1 |
| x | 0 | x | 1 |
| x | x | 0 | 1 |
| 1 | 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| NAND3XL | 5.04 | 2.64 |
| NAND3X1 | 5.04 | 2.64 |
| NAND3X2 | 5.04 | 4.62 |
| NAND3X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0118 | 0.0177 | 0.0313 | 0.0531 |
| B | 0.0160 | 0.0241 | 0.0449 | 0.0731 |
| C | 0.0209 | 0.0293 | 0.0564 | 0.0905 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0037 | 0.0051 | 0.0089 | 0.0154 |
| B | 0.0034 | 0.0049 | 0.0094 | 0.0147 |
| C | 0.0034 | 0.0047 | 0.0101 | 0.0151 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0407 | 0.0350 | 0.0339 | 0.0359 |
| A → Y↓ | 0.0295 | 0.0266 | 0.0234 | 0.0248 |
| B → Y↑ | 0.0508 | 0.0447 | 0.0457 | 0.0464 |
| B → Y↓ | 0.0379 | 0.0354 | 0.0332 | 0.0335 |
| C → Y↑ | 0.0601 | 0.0530 | 0.0561 | 0.0566 |
| C → Y↓ | 0.0419 | 0.0393 | 0.0380 | 0.0381 |

| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8808 | 3.7394 | 2.0556 | 1.3133 |
| A → Y↓ | 4.7212 | 3.2788 | 1.6391 | 1.0495 |
| B → Y↑ | 5.8729 | 3.7366 | 2.0544 | 1.3125 |
| B → Y↓ | 4.7284 | 3.2827 | 1.6413 | 1.0505 |
| C → Y↑ | 5.8806 | 3.7406 | 2.0567 | 1.3136 |
| C → Y↓ | 4.7283 | 3.2827 | 1.6416 | 1.0506 |

Cell Description

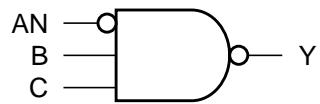
The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C)}$$

Functions

| AN | B | C | Y |
|----|---|---|---|
| 1 | x | x | 1 |
| x | 0 | x | 1 |
| x | x | 0 | 1 |
| 0 | 1 | 1 | 0 |

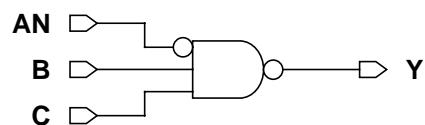
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| NAND3BXL | 5.04 | 3.30 |
| NAND3BX1 | 5.04 | 3.30 |
| NAND3BX2 | 5.04 | 5.28 |
| NAND3BX4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0236 | 0.0290 | 0.0448 | 0.0765 |
| B | 0.0136 | 0.0187 | 0.0350 | 0.0549 |
| C | 0.0175 | 0.0248 | 0.0481 | 0.0754 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0026 | 0.0027 | 0.0041 | 0.0068 |
| B | 0.0035 | 0.0048 | 0.0094 | 0.0146 |
| C | 0.0034 | 0.0048 | 0.0103 | 0.0153 |

Delays at 25°C, 1.8V, Typical Process

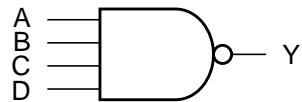
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0802 | 0.0834 | 0.0769 | 0.0742 | 5.8866 | 3.7809 | 2.0571 | 1.2821 |
| AN → Y↓ | 0.1028 | 0.1114 | 0.0921 | 0.0869 | 4.7519 | 3.2956 | 1.6464 | 1.0598 |
| B → Y↑ | 0.0499 | 0.0454 | 0.0447 | 0.0442 | 5.8800 | 3.7780 | 2.0565 | 1.2815 |
| B → Y↓ | 0.0395 | 0.0399 | 0.0363 | 0.0365 | 4.7376 | 3.2885 | 1.6439 | 1.0586 |
| C → Y↑ | 0.0599 | 0.0548 | 0.0556 | 0.0545 | 5.8844 | 3.7803 | 2.0576 | 1.2866 |
| C → Y↓ | 0.0445 | 0.0450 | 0.0417 | 0.0413 | 4.7384 | 3.2889 | 1.6441 | 1.0586 |

Cell Description

The NAND4 cell provides a logical NAND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C \bullet D)}$$

Logic Symbol



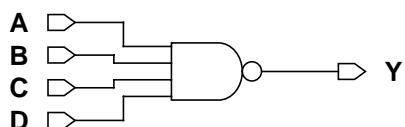
Functions

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | x | x | x | 1 |
| x | 0 | x | x | 1 |
| x | x | 0 | x | 1 |
| x | x | x | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NAND4XL | 5.04 | 3.30 |
| NAND4X1 | 5.04 | 3.30 |
| NAND4X2 | 5.04 | 5.94 |
| NAND4X4 | 5.04 | 11.22 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0135 | 0.0186 | 0.0351 | 0.0716 |
| B | 0.0184 | 0.0253 | 0.0490 | 0.0988 |
| C | 0.0237 | 0.0330 | 0.0646 | 0.1302 |
| D | 0.0282 | 0.0397 | 0.0789 | 0.1597 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0035 | 0.0051 | 0.0095 | 0.0199 |
| B | 0.0038 | 0.0050 | 0.0097 | 0.0201 |
| C | 0.0037 | 0.0050 | 0.0100 | 0.0205 |
| D | 0.0034 | 0.0048 | 0.0106 | 0.0220 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0419 | 0.0396 | 0.0402 | 0.0406 |
| A → Y↓ | 0.0306 | 0.0298 | 0.0293 | 0.0297 |
| B → Y↑ | 0.0564 | 0.0516 | 0.0527 | 0.0527 |
| B → Y↓ | 0.0454 | 0.0426 | 0.0421 | 0.0421 |
| C → Y↑ | 0.0670 | 0.0621 | 0.0640 | 0.0641 |
| C → Y↓ | 0.0527 | 0.0500 | 0.0498 | 0.0498 |
| D → Y↑ | 0.0747 | 0.0707 | 0.0749 | 0.0757 |
| D → Y↓ | 0.0554 | 0.0540 | 0.0554 | 0.0562 |

Delays at 25°C, 1.8V, Typical Process

| Description | K_{load} (ns/pF) | | | |
|--------------------|---------------------------------|-----------|-----------|-----------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8789 | 3.9354 | 2.0555 | 1.0278 |
| A → Y↓ | 5.4421 | 3.7914 | 1.8955 | 0.9478 |
| B → Y↑ | 5.8762 | 3.9330 | 2.0543 | 1.0271 |
| B → Y↓ | 5.4530 | 3.7956 | 1.8976 | 0.9488 |
| C → Y↑ | 5.8837 | 3.9371 | 2.0564 | 1.0282 |
| C → Y↓ | 5.4524 | 3.7956 | 1.8977 | 0.9488 |
| D → Y↑ | 5.9021 | 3.9466 | 2.0615 | 1.0308 |
| D → Y↓ | 5.4507 | 3.7955 | 1.8980 | 0.9491 |

Cell Description

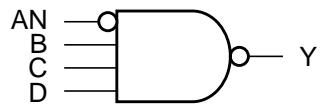
The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C \bullet D)}$$

Functions

| AN | B | C | D | Y |
|----|---|---|---|---|
| 1 | x | x | x | 1 |
| x | 0 | x | x | 1 |
| x | x | 0 | x | 1 |
| x | x | x | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |

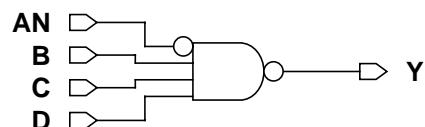
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NAND4BXL | 5.04 | 3.96 |
| NAND4BX1 | 5.04 | 4.62 |
| NAND4BX2 | 5.04 | 6.60 |
| NAND4BX4 | 5.04 | 11.88 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0227 | 0.0282 | 0.0507 | 0.1012 |
| B | 0.0144 | 0.0218 | 0.0395 | 0.0797 |
| C | 0.0188 | 0.0281 | 0.0530 | 0.1056 |
| D | 0.0235 | 0.0348 | 0.0678 | 0.1354 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0027 | 0.0025 | 0.0041 | 0.0073 |
| B | 0.0037 | 0.0050 | 0.0097 | 0.0201 |
| C | 0.0036 | 0.0049 | 0.0101 | 0.0205 |
| D | 0.0034 | 0.0047 | 0.0108 | 0.0222 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0825 | 0.0867 | 0.0839 | 0.0848 | 5.8883 | 3.9379 | 2.0570 | 1.0286 |
| AN → Y↓ | 0.1035 | 0.1108 | 0.0987 | 0.0980 | 5.4657 | 3.8016 | 1.9005 | 0.9503 |
| B → Y↑ | 0.0548 | 0.0525 | 0.0515 | 0.0513 | 5.8839 | 3.9376 | 2.0565 | 1.0283 |
| B → Y↓ | 0.0476 | 0.0480 | 0.0450 | 0.0447 | 5.4593 | 3.7998 | 1.8994 | 0.9498 |
| C → Y↑ | 0.0659 | 0.0636 | 0.0634 | 0.0631 | 5.8873 | 3.9393 | 2.0574 | 1.0288 |
| C → Y↓ | 0.0552 | 0.0562 | 0.0533 | 0.0533 | 5.4589 | 3.7999 | 1.8994 | 0.9498 |
| D → Y↑ | 0.0751 | 0.0727 | 0.0747 | 0.0752 | 5.9036 | 3.9470 | 2.0618 | 1.0310 |
| D → Y↓ | 0.0590 | 0.0603 | 0.0589 | 0.0597 | 5.4583 | 3.7996 | 1.8997 | 0.9499 |

Cell Description

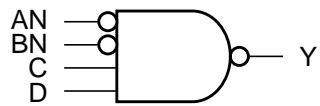
The NAND4BB cell provides a logical NAND of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet \overline{BN} \bullet C \bullet D)}$$

Functions

| AN | BN | C | D | Y |
|----|----|---|---|---|
| 1 | x | x | x | 1 |
| x | 1 | x | x | 1 |
| x | x | 0 | x | 1 |
| x | x | x | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |

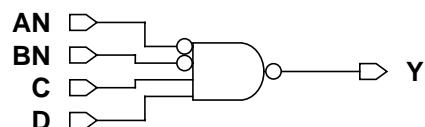
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NAND4BBXL | 5.04 | 5.28 |
| NAND4BBX1 | 5.04 | 5.28 |
| NAND4BBX2 | 5.04 | 7.26 |
| NAND4BBX4 | 5.04 | 12.54 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0233 | 0.0282 | 0.0529 | 0.1030 |
| BN | 0.0267 | 0.0335 | 0.0640 | 0.1243 |
| C | 0.0171 | 0.0232 | 0.0444 | 0.0890 |
| D | 0.0217 | 0.0297 | 0.0576 | 0.1153 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0025 | 0.0025 | 0.0041 | 0.0073 |
| BN | 0.0025 | 0.0026 | 0.0040 | 0.0075 |
| C | 0.0036 | 0.0050 | 0.0101 | 0.0205 |
| D | 0.0035 | 0.0049 | 0.0108 | 0.0219 |

Delays at 25°C, 1.8V, Typical Process

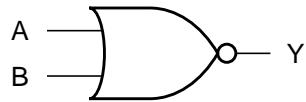
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0837 | 0.0868 | 0.0849 | 0.0856 | 5.8830 | 3.9383 | 2.0571 | 1.0287 |
| AN → Y↓ | 0.1035 | 0.1105 | 0.0993 | 0.0981 | 5.4594 | 3.8015 | 1.9004 | 0.9502 |
| BN → Y↑ | 0.0954 | 0.0990 | 0.0982 | 0.0966 | 5.8844 | 3.9392 | 2.0541 | 1.0278 |
| BN → Y↓ | 0.1146 | 0.1231 | 0.1133 | 0.1108 | 5.4736 | 3.8104 | 1.9040 | 0.9519 |
| C → Y↑ | 0.0678 | 0.0626 | 0.0631 | 0.0627 | 5.8917 | 3.9430 | 2.0594 | 1.0297 |
| C → Y↓ | 0.0585 | 0.0577 | 0.0557 | 0.0555 | 5.4617 | 3.8030 | 1.9010 | 0.9505 |
| D → Y↑ | 0.0775 | 0.0720 | 0.0747 | 0.0748 | 5.9062 | 3.9497 | 2.0631 | 1.0316 |
| D → Y↓ | 0.0629 | 0.0622 | 0.0619 | 0.0622 | 5.4614 | 3.8030 | 1.9013 | 0.9507 |

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B)}$$

Logic Symbol



Functions

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| x | 1 | 0 |
| 1 | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| NOR2XL | 5.04 | 1.98 |
| NOR2X1 | 5.04 | 1.98 |
| NOR2X2 | 5.04 | 3.30 |
| NOR2X4 | 5.04 | 4.62 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0108 | 0.0147 | 0.0283 | 0.0562 |
| B | 0.0140 | 0.0190 | 0.0368 | 0.0742 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0035 | 0.0046 | 0.0084 | 0.0172 |
| B | 0.0031 | 0.0042 | 0.0086 | 0.0163 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0383 | 0.0359 | 0.0321 | 0.0328 |
| A → Y↓ | 0.0209 | 0.0200 | 0.0184 | 0.0188 |
| B → Y↑ | 0.0476 | 0.0458 | 0.0440 | 0.0436 |
| B → Y↓ | 0.0251 | 0.0249 | 0.0245 | 0.0243 |

| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 8.7141 | 6.0734 | 3.0360 | 1.5231 |
| A → Y↓ | 3.5488 | 2.5000 | 1.2766 | 0.6383 |
| B → Y↑ | 8.7025 | 6.0688 | 3.0351 | 1.5222 |
| B → Y↓ | 3.5691 | 2.5104 | 1.2820 | 0.6410 |

Cell Description

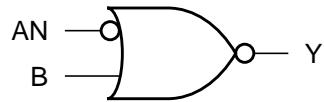
The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A}N + B)}$$

Functions

| AN | B | Y |
|----|---|---|
| 1 | 0 | 1 |
| x | 1 | 0 |
| 0 | x | 0 |

Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NOR2BXL | 5.04 | 2.64 |
| NOR2BX1 | 5.04 | 2.64 |
| NOR2BX2 | 5.04 | 3.96 |
| NOR2BX4 | 5.04 | 5.28 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0182 | 0.0224 | 0.0359 | 0.0724 |
| B | 0.0142 | 0.0194 | 0.0366 | 0.0748 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0025 | 0.0025 | 0.0040 | 0.0068 |
| B | 0.0033 | 0.0044 | 0.0088 | 0.0165 |

Delays at 25°C, 1.8V, Typical Process

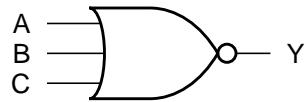
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0712 | 0.0742 | 0.0699 | 0.0711 | 8.7172 | 6.0754 | 3.0372 | 1.5174 |
| AN → Y↓ | 0.0899 | 0.1023 | 0.0894 | 0.0909 | 3.4685 | 2.5321 | 1.2906 | 0.6456 |
| B → Y↑ | 0.0492 | 0.0480 | 0.0457 | 0.0459 | 8.7065 | 6.0704 | 3.0358 | 1.5162 |
| B → Y↓ | 0.0241 | 0.0247 | 0.0240 | 0.0240 | 3.4346 | 2.5118 | 1.2827 | 0.6414 |

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C)}$$

Logic Symbol



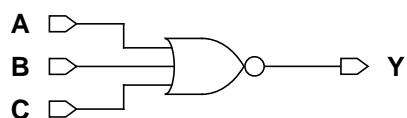
Functions

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| x | x | 1 | 0 |
| x | 1 | x | 0 |
| 1 | x | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| NOR3XL | 5.04 | 2.64 |
| NOR3X1 | 5.04 | 2.64 |
| NOR3X2 | 5.04 | 4.62 |
| NOR3X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0140 | 0.0188 | 0.0368 | 0.0589 |
| B | 0.0174 | 0.0238 | 0.0474 | 0.0754 |
| C | 0.0212 | 0.0296 | 0.0584 | 0.0931 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0038 | 0.0050 | 0.0094 | 0.0166 |
| B | 0.0036 | 0.0047 | 0.0098 | 0.0157 |
| C | 0.0034 | 0.0046 | 0.0099 | 0.0156 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0509 | 0.0474 | 0.0436 | 0.0443 |
| A → Y↓ | 0.0236 | 0.0226 | 0.0216 | 0.0213 |
| B → Y↑ | 0.0767 | 0.0731 | 0.0704 | 0.0695 |
| B → Y↓ | 0.0305 | 0.0311 | 0.0306 | 0.0293 |
| C → Y↑ | 0.0864 | 0.0830 | 0.0822 | 0.0807 |
| C → Y↓ | 0.0337 | 0.0350 | 0.0362 | 0.0346 |

| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 11.1208 | 7.7335 | 3.8660 | 2.3698 |
| A → Y↓ | 3.4079 | 2.5012 | 1.2770 | 0.7506 |
| B → Y↑ | 11.1087 | 7.7285 | 3.8643 | 2.3685 |
| B → Y↓ | 3.4281 | 2.5080 | 1.2804 | 0.7523 |
| C → Y↑ | 11.1064 | 7.7280 | 3.8649 | 2.3686 |
| C → Y↓ | 3.4731 | 2.5312 | 1.2906 | 0.7572 |

Cell Description

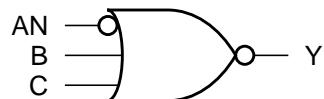
The NOR3B cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C)}$$

Functions

| AN | B | C | Y |
|----|---|---|---|
| 1 | 0 | 0 | 1 |
| x | x | 1 | 0 |
| x | 1 | x | 0 |
| 0 | x | x | 0 |

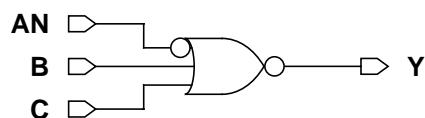
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NOR3BXL | 5.04 | 3.96 |
| NOR3BX1 | 5.04 | 3.96 |
| NOR3BX2 | 5.04 | 5.28 |
| NOR3BX4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0193 | 0.0236 | 0.0403 | 0.0738 |
| B | 0.0183 | 0.0243 | 0.0467 | 0.0788 |
| C | 0.0219 | 0.0298 | 0.0580 | 0.0980 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0023 | 0.0025 | 0.0041 | 0.0066 |
| B | 0.0035 | 0.0047 | 0.0093 | 0.0162 |
| C | 0.0035 | 0.0047 | 0.0101 | 0.0166 |

Delays at 25°C, 1.8V, Typical Process

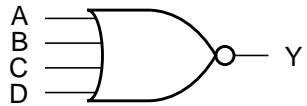
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0869 | 0.0865 | 0.0802 | 0.0825 | 11.1242 | 7.7349 | 3.8664 | 2.2494 |
| AN → Y↓ | 0.0985 | 0.1039 | 0.0947 | 0.0994 | 3.4666 | 2.5281 | 1.2894 | 0.7573 |
| B → Y↑ | 0.0799 | 0.0762 | 0.0715 | 0.0710 | 11.1103 | 7.7293 | 3.8644 | 2.2478 |
| B → Y↓ | 0.0308 | 0.0311 | 0.0300 | 0.0302 | 3.4303 | 2.5094 | 1.2813 | 0.7528 |
| C → Y↑ | 0.0889 | 0.0855 | 0.0838 | 0.0826 | 11.1072 | 7.7284 | 3.8653 | 2.2481 |
| C → Y↓ | 0.0341 | 0.0353 | 0.0361 | 0.0365 | 3.4719 | 2.5306 | 1.2906 | 0.7573 |

Cell Description

The NOR4 cell provides a logical NOR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C + D)}$$

Logic Symbol



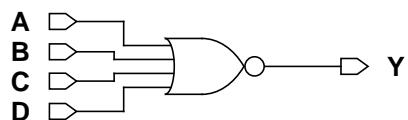
Functions

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| x | x | x | 1 | 0 |
| x | x | 1 | x | 0 |
| x | 1 | x | x | 0 |
| 1 | x | x | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NOR4XL | 5.04 | 3.96 |
| NOR4X1 | 5.04 | 3.96 |
| NOR4X2 | 5.04 | 5.94 |
| NOR4X4 | 5.04 | 11.22 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0168 | 0.0223 | 0.0425 | 0.0780 |
| B | 0.0211 | 0.0286 | 0.0555 | 0.1011 |
| C | 0.0260 | 0.0356 | 0.0698 | 0.1250 |
| D | 0.0304 | 0.0419 | 0.0834 | 0.1490 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0043 | 0.0056 | 0.0103 | 0.0194 |
| B | 0.0041 | 0.0054 | 0.0105 | 0.0203 |
| C | 0.0040 | 0.0053 | 0.0110 | 0.0200 |
| D | 0.0038 | 0.0051 | 0.0115 | 0.0203 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0554 | 0.0496 | 0.0441 | 0.0477 |
| A → Y↓ | 0.0265 | 0.0258 | 0.0243 | 0.0248 |
| B → Y↑ | 0.0965 | 0.0920 | 0.0876 | 0.0924 |
| B → Y↓ | 0.0361 | 0.0370 | 0.0363 | 0.0377 |
| C → Y↑ | 0.1220 | 0.1174 | 0.1129 | 0.1154 |
| C → Y↓ | 0.0422 | 0.0436 | 0.0430 | 0.0428 |
| D → Y↑ | 0.1311 | 0.1269 | 0.1256 | 0.1283 |
| D → Y↓ | 0.0422 | 0.0447 | 0.0452 | 0.0452 |

Delays at 25°C, 1.8V, Typical Process

| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 12.4775 | 8.7586 | 4.3778 | 2.4989 |
| A → Y↓ | 3.4158 | 2.5019 | 1.2773 | 0.7094 |
| B → Y↑ | 12.4674 | 8.7560 | 4.3782 | 2.4993 |
| B → Y↓ | 3.4297 | 2.5089 | 1.2810 | 0.7100 |
| C → Y↑ | 12.4681 | 8.7565 | 4.3781 | 2.4987 |
| C → Y↓ | 3.4743 | 2.5305 | 1.2920 | 0.7164 |
| D → Y↑ | 12.4654 | 8.7556 | 4.3794 | 2.4993 |
| D → Y↓ | 3.5423 | 2.5660 | 1.3107 | 0.7255 |

Cell Description

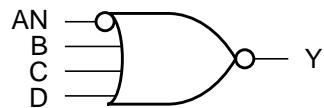
The NOR4B cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C + D)}$$

Functions

| AN | B | C | D | Y |
|----|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 |
| x | x | x | 1 | 0 |
| x | x | 1 | x | 0 |
| x | 1 | x | x | 0 |
| 0 | x | x | x | 0 |

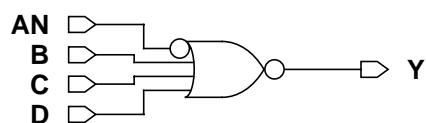
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NOR4BXL | 5.04 | 3.96 |
| NOR4BX1 | 5.04 | 3.96 |
| NOR4BX2 | 5.04 | 6.60 |
| NOR4BX4 | 5.04 | 11.88 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0223 | 0.0272 | 0.0459 | 0.0839 |
| B | 0.0205 | 0.0269 | 0.0560 | 0.1008 |
| C | 0.0251 | 0.0334 | 0.0705 | 0.1249 |
| D | 0.0298 | 0.0394 | 0.0836 | 0.1485 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0026 | 0.0029 | 0.0047 | 0.0073 |
| B | 0.0041 | 0.0052 | 0.0104 | 0.0200 |
| C | 0.0040 | 0.0051 | 0.0111 | 0.0201 |
| D | 0.0040 | 0.0051 | 0.0111 | 0.0206 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0909 | 0.0908 | 0.0826 | 0.0863 | 12.4768 | 9.3391 | 4.3779 | 2.4991 |
| AN → Y↓ | 0.1114 | 0.1078 | 0.1011 | 0.1052 | 3.4743 | 2.5275 | 1.3109 | 0.7157 |
| B → Y↑ | 0.0956 | 0.0942 | 0.0876 | 0.0932 | 12.4710 | 9.3369 | 4.3778 | 2.4992 |
| B → Y↓ | 0.0353 | 0.0342 | 0.0355 | 0.0357 | 3.4322 | 2.5097 | 1.3034 | 0.7116 |
| C → Y↑ | 0.1200 | 0.1188 | 0.1152 | 0.1170 | 12.4674 | 9.3356 | 4.3787 | 2.4987 |
| C → Y↓ | 0.0412 | 0.0410 | 0.0441 | 0.0428 | 3.4763 | 2.5288 | 1.3137 | 0.7163 |
| D → Y↑ | 0.1295 | 0.1285 | 0.1260 | 0.1299 | 12.4664 | 9.3352 | 4.3789 | 2.4993 |
| D → Y↓ | 0.0417 | 0.0420 | 0.0458 | 0.0458 | 3.5388 | 2.5617 | 1.3324 | 0.7248 |

Cell Description

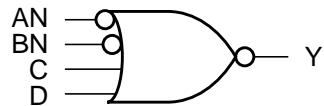
The NOR4BB cell provides a logical NOR of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + \overline{BN}) + C + D}$$

Functions

| AN | BN | C | D | Y |
|----|----|---|---|---|
| 1 | 1 | 0 | 0 | 1 |
| x | x | x | 1 | 0 |
| x | x | 1 | x | 0 |
| x | 0 | x | x | 0 |
| 0 | x | x | x | 0 |

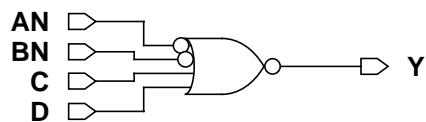
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| NOR4BBXL | 5.04 | 5.28 |
| NOR4BBX1 | 5.04 | 5.28 |
| NOR4BBX2 | 5.04 | 7.26 |
| NOR4BBX4 | 5.04 | 13.20 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0212 | 0.0267 | 0.0472 | 0.0836 |
| BN | 0.0256 | 0.0316 | 0.0583 | 0.1035 |
| C | 0.0279 | 0.0372 | 0.0727 | 0.1268 |
| D | 0.0323 | 0.0439 | 0.0862 | 0.1505 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| AN | 0.0025 | 0.0029 | 0.0048 | 0.0073 |
| BN | 0.0027 | 0.0030 | 0.0049 | 0.0072 |
| C | 0.0040 | 0.0054 | 0.0109 | 0.0201 |
| D | 0.0040 | 0.0053 | 0.0115 | 0.0204 |

Delays at 25°C, 1.8V, Typical Process

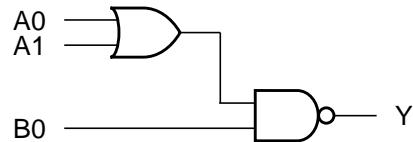
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| AN → Y↑ | 0.0966 | 0.0928 | 0.0865 | 0.0873 | 12.4742 | 8.7580 | 4.3790 | 2.4994 |
| AN → Y↓ | 0.1113 | 0.1105 | 0.1017 | 0.1058 | 3.4648 | 2.5252 | 1.2889 | 0.7156 |
| BN → Y↑ | 0.1458 | 0.1404 | 0.1310 | 0.1360 | 12.4673 | 8.7561 | 4.3782 | 2.5004 |
| BN → Y↓ | 0.1248 | 0.1241 | 0.1153 | 0.1229 | 3.4669 | 2.5266 | 1.2892 | 0.7162 |
| C → Y↑ | 0.1317 | 0.1254 | 0.1195 | 0.1198 | 12.4681 | 8.7564 | 4.3781 | 2.4990 |
| C → Y↓ | 0.0440 | 0.0447 | 0.0437 | 0.0428 | 3.4766 | 2.5317 | 1.2925 | 0.7168 |
| D → Y↑ | 0.1412 | 0.1354 | 0.1315 | 0.1321 | 12.4660 | 8.7559 | 4.3788 | 2.4993 |
| D → Y↓ | 0.0447 | 0.0465 | 0.0462 | 0.0455 | 3.5381 | 2.5648 | 1.3098 | 0.7252 |

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0}$$

Logic Symbol



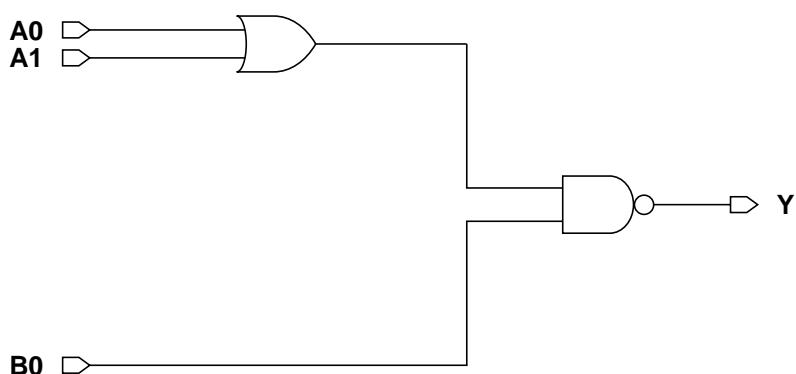
Functions

| A0 | A1 | B0 | Y |
|----|----|----|---|
| 0 | 0 | x | 1 |
| x | x | 0 | 1 |
| x | 1 | 1 | 0 |
| 1 | x | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI21XL | 5.04 | 2.64 |
| OAI21X1 | 5.04 | 3.30 |
| OAI21X2 | 5.04 | 5.28 |
| OAI21X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0182 | 0.0242 | 0.0473 | 0.0863 |
| A1 | 0.0208 | 0.0282 | 0.0549 | 0.1073 |
| B0 | 0.0144 | 0.0191 | 0.0363 | 0.0705 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0037 | 0.0048 | 0.0100 | 0.0191 |
| A1 | 0.0035 | 0.0046 | 0.0091 | 0.0183 |
| B0 | 0.0033 | 0.0043 | 0.0082 | 0.0159 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0657 | 0.0617 | 0.0628 | 0.0571 | 8.7109 | 6.0727 | 3.0367 | 1.5102 |
| A0 → Y↓ | 0.0340 | 0.0313 | 0.0325 | 0.0295 | 4.3971 | 2.9308 | 1.4834 | 0.7349 |
| A1 → Y↑ | 0.0768 | 0.0735 | 0.0735 | 0.0681 | 8.7060 | 6.0704 | 3.0355 | 1.5096 |
| A1 → Y↓ | 0.0423 | 0.0397 | 0.0405 | 0.0377 | 4.4087 | 2.9368 | 1.4862 | 0.7363 |
| B0 → Y↑ | 0.0343 | 0.0316 | 0.0312 | 0.0294 | 5.8978 | 4.2120 | 2.1056 | 1.0498 |
| B0 → Y↓ | 0.0334 | 0.0298 | 0.0298 | 0.0282 | 4.4037 | 2.9335 | 1.4845 | 0.7354 |

Cell Description

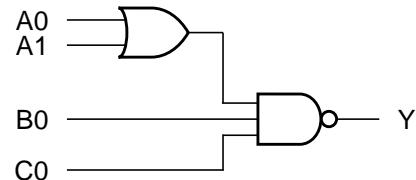
The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1)} \bullet B_0 \bullet C_0$$

Functions

| A0 | A1 | B0 | C0 | Y |
|----|----|----|----|---|
| 0 | 0 | x | x | 1 |
| x | x | 0 | x | 1 |
| x | x | x | 0 | 1 |
| x | 1 | 1 | 1 | 0 |
| 1 | x | 1 | 1 | 0 |

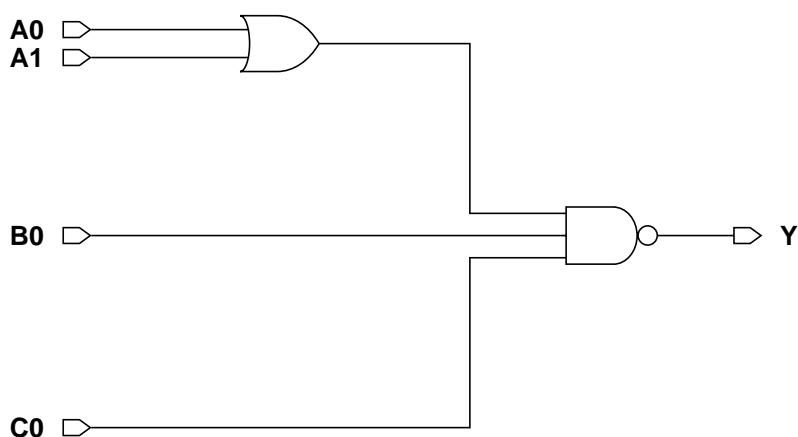
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI211XL | 5.04 | 3.96 |
| OAI211X1 | 5.04 | 3.96 |
| OAI211X2 | 5.04 | 6.60 |
| OAI211X4 | 5.04 | 5.94 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0252 | 0.0346 | 0.0679 | 0.0857 |
| A1 | 0.0282 | 0.0388 | 0.0757 | 0.0918 |
| B0 | 0.0153 | 0.0208 | 0.0397 | 0.0715 |
| C0 | 0.0204 | 0.0281 | 0.0540 | 0.0782 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0037 | 0.0051 | 0.0106 | 0.0035 |
| A1 | 0.0036 | 0.0049 | 0.0097 | 0.0035 |
| B0 | 0.0035 | 0.0046 | 0.0087 | 0.0036 |
| C0 | 0.0034 | 0.0045 | 0.0091 | 0.0030 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0956 | 0.0929 | 0.0919 | 0.2483 | 8.7269 | 6.0801 | 3.0405 | 1.0401 |
| A0 → Y↓ | 0.0472 | 0.0460 | 0.0452 | 0.1820 | 4.7317 | 3.3092 | 1.6472 | 0.6464 |
| A1 → Y↑ | 0.1074 | 0.1045 | 0.1023 | 0.2595 | 8.7234 | 6.0784 | 3.0396 | 1.0401 |
| A1 → Y↓ | 0.0568 | 0.0557 | 0.0547 | 0.1935 | 4.7430 | 3.3145 | 1.6552 | 0.6464 |
| B0 → Y↑ | 0.0401 | 0.0395 | 0.0392 | 0.1667 | 5.9006 | 4.2124 | 2.2107 | 1.0401 |
| B0 → Y↓ | 0.0385 | 0.0379 | 0.0361 | 0.1786 | 4.7377 | 3.3117 | 1.6536 | 0.6465 |
| C0 → Y↑ | 0.0516 | 0.0511 | 0.0518 | 0.1781 | 5.8941 | 4.2097 | 2.2093 | 1.0401 |
| C0 → Y↓ | 0.0482 | 0.0475 | 0.0462 | 0.1848 | 4.7451 | 3.3154 | 1.6556 | 0.6464 |

Cell Description

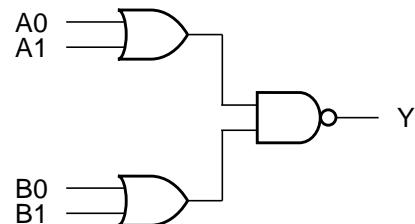
The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet (B_0 + B_1)}$$

Functions

| A0 | A1 | B0 | B1 | Y |
|----|----|----|----|---|
| 0 | 0 | x | x | 1 |
| x | x | 0 | 0 | 1 |
| x | 1 | x | 1 | 0 |
| x | 1 | 1 | x | 0 |
| 1 | x | x | 1 | 0 |
| 1 | x | 1 | x | 0 |

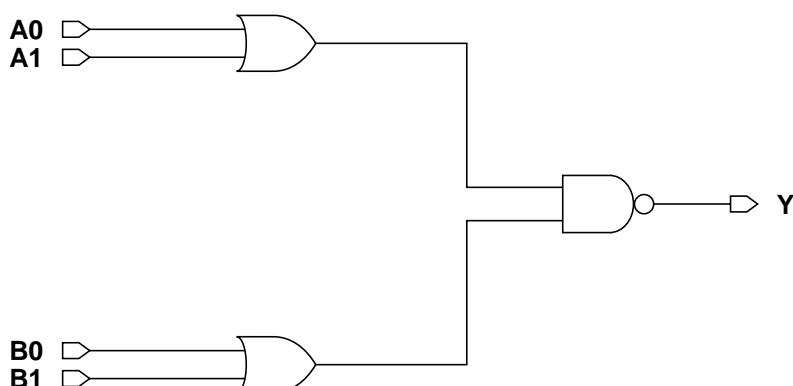
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI22XL | 5.04 | 3.96 |
| OAI22X1 | 5.04 | 3.96 |
| OAI22X2 | 5.04 | 5.94 |
| OAI22X4 | 5.04 | 9.24 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0167 | 0.0227 | 0.0451 | 0.0905 |
| A1 | 0.0200 | 0.0275 | 0.0539 | 0.1091 |
| B0 | 0.0254 | 0.0341 | 0.0681 | 0.1300 |
| B1 | 0.0280 | 0.0378 | 0.0757 | 0.1458 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0036 | 0.0049 | 0.0101 | 0.0191 |
| A1 | 0.0038 | 0.0049 | 0.0091 | 0.0184 |
| B0 | 0.0037 | 0.0049 | 0.0101 | 0.0192 |
| B1 | 0.0034 | 0.0045 | 0.0091 | 0.0184 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0506 | 0.0484 | 0.0508 | 0.0493 | 8.7579 | 6.0981 | 3.0494 | 1.5165 |
| A0 → Y↓ | 0.0343 | 0.0344 | 0.0368 | 0.0365 | 4.1199 | 2.9344 | 1.5038 | 0.7539 |
| A1 → Y↑ | 0.0637 | 0.0605 | 0.0608 | 0.0599 | 8.7565 | 6.0969 | 3.0477 | 1.5157 |
| A1 → Y↓ | 0.0434 | 0.0432 | 0.0447 | 0.0448 | 4.1302 | 2.9399 | 1.5063 | 0.7553 |
| B0 → Y↑ | 0.0887 | 0.0829 | 0.0851 | 0.0792 | 8.7124 | 6.0734 | 3.0367 | 1.5103 |
| B0 → Y↓ | 0.0478 | 0.0466 | 0.0490 | 0.0471 | 4.1244 | 2.9377 | 1.5053 | 0.7548 |
| B1 → Y↑ | 0.0988 | 0.0933 | 0.0952 | 0.0899 | 8.7068 | 6.0709 | 3.0355 | 1.5097 |
| B1 → Y↓ | 0.0556 | 0.0549 | 0.0575 | 0.0560 | 4.1319 | 2.9413 | 1.5071 | 0.7556 |

Cell Description

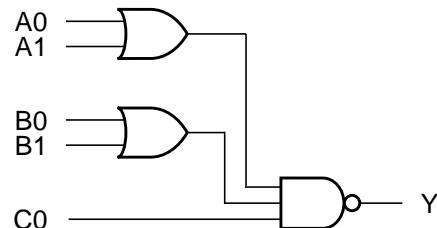
The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet (B_0 + B_1) \bullet C_0}$$

Functions

| A0 | A1 | B0 | B1 | C0 | Y |
|----|----|----|----|----|---|
| 0 | 0 | x | x | x | 1 |
| x | x | 0 | 0 | x | 1 |
| x | x | x | x | 0 | 1 |
| x | 1 | x | 1 | 1 | 0 |
| x | 1 | 1 | x | 1 | 0 |
| 1 | x | x | 1 | 1 | 0 |
| 1 | x | 1 | x | 1 | 0 |

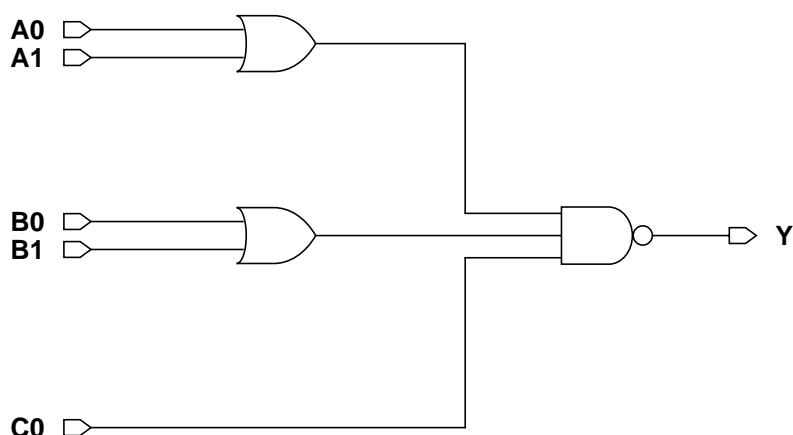
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI221XL | 5.04 | 4.62 |
| OAI221X1 | 5.04 | 5.28 |
| OAI221X2 | 5.04 | 8.58 |
| OAI221X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0250 | 0.0337 | 0.0654 | 0.0831 |
| A1 | 0.0276 | 0.0376 | 0.0732 | 0.0883 |
| B0 | 0.0334 | 0.0450 | 0.0873 | 0.0931 |
| B1 | 0.0361 | 0.0489 | 0.0952 | 0.0977 |
| C0 | 0.0193 | 0.0266 | 0.0498 | 0.0746 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0039 | 0.0053 | 0.0102 | 0.0036 |
| A1 | 0.0038 | 0.0051 | 0.0102 | 0.0035 |
| B0 | 0.0038 | 0.0052 | 0.0102 | 0.0036 |
| B1 | 0.0036 | 0.0049 | 0.0101 | 0.0033 |
| C0 | 0.0036 | 0.0046 | 0.0091 | 0.0035 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0874 | 0.0824 | 0.0794 | 0.2401 | 8.7529 | 6.0960 | 3.0483 | 1.1022 |
| A0 → Y↓ | 0.0566 | 0.0541 | 0.0525 | 0.1859 | 4.7465 | 3.2908 | 1.6476 | 0.6459 |
| A1 → Y↑ | 0.0983 | 0.0935 | 0.0900 | 0.2508 | 8.7493 | 6.0941 | 3.0472 | 1.1021 |
| A1 → Y↓ | 0.0662 | 0.0640 | 0.0620 | 0.1968 | 4.7532 | 3.2939 | 1.6491 | 0.6459 |
| B0 → Y↑ | 0.1212 | 0.1150 | 0.1108 | 0.2729 | 8.7473 | 6.0888 | 3.0448 | 1.1021 |
| B0 → Y↓ | 0.0662 | 0.0632 | 0.0611 | 0.1955 | 4.7459 | 3.2905 | 1.6475 | 0.6459 |
| B1 → Y↑ | 0.1316 | 0.1255 | 0.1215 | 0.2827 | 8.7436 | 6.0870 | 3.0439 | 1.1021 |
| B1 → Y↓ | 0.0757 | 0.0727 | 0.0706 | 0.2063 | 4.7522 | 3.2939 | 1.6491 | 0.6459 |
| C0 → Y↑ | 0.0425 | 0.0418 | 0.0389 | 0.1691 | 5.9220 | 4.2269 | 2.1136 | 1.1021 |
| C0 → Y↓ | 0.0487 | 0.0480 | 0.0455 | 0.1804 | 4.7542 | 3.2945 | 1.6495 | 0.6459 |

Cell Description

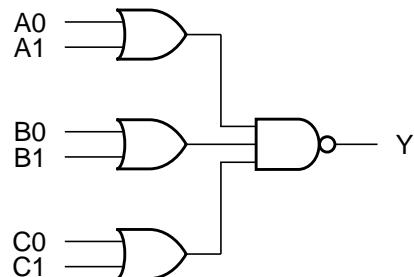
The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1) \bullet (B_0 + B_1) \bullet (C_0 + C_1)}$$

Functions

| A0 | A1 | B0 | B1 | C0 | C1 | Y |
|----|----|----|----|----|----|---|
| 0 | 0 | x | x | x | x | 1 |
| x | x | 0 | 0 | x | x | 1 |
| x | x | x | x | 0 | 0 | 1 |
| x | 1 | x | 1 | 1 | x | 0 |
| x | 1 | x | 1 | x | 1 | 0 |
| x | 1 | 1 | x | 1 | x | 0 |
| x | 1 | 1 | x | x | 1 | 0 |
| 1 | x | x | 1 | 1 | x | 0 |
| 1 | x | x | 1 | x | 1 | 0 |
| 1 | x | 1 | x | x | 1 | 0 |

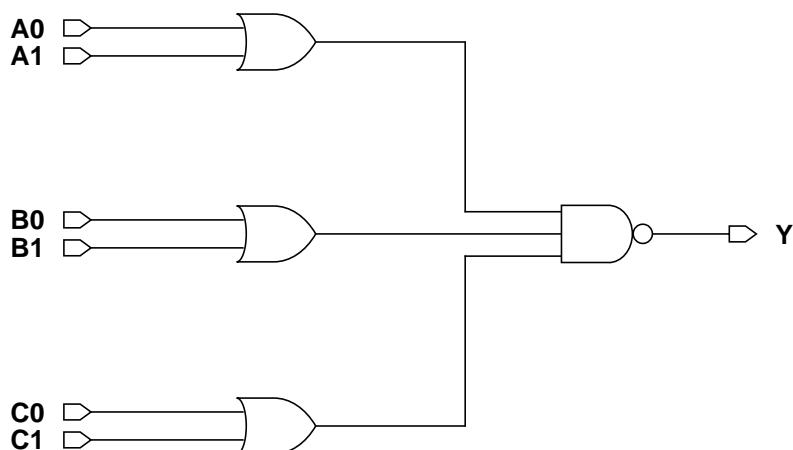
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI222XL | 5.04 | 5.28 |
| OAI222X1 | 5.04 | 5.94 |
| OAI222X2 | 5.04 | 9.90 |
| OAI222X4 | 5.04 | 7.92 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0336 | 0.0444 | 0.0877 | 0.0943 |
| A1 | 0.0363 | 0.0484 | 0.0954 | 0.0999 |
| B0 | 0.0418 | 0.0556 | 0.1098 | 0.1036 |
| B1 | 0.0444 | 0.0595 | 0.1177 | 0.1088 |
| C0 | 0.0230 | 0.0315 | 0.0612 | 0.0816 |
| C1 | 0.0253 | 0.0352 | 0.0692 | 0.0852 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0039 | 0.0051 | 0.0103 | 0.0035 |
| A1 | 0.0038 | 0.0051 | 0.0103 | 0.0035 |
| B0 | 0.0038 | 0.0052 | 0.0102 | 0.0035 |
| B1 | 0.0036 | 0.0049 | 0.0101 | 0.0033 |
| C0 | 0.0042 | 0.0054 | 0.0103 | 0.0038 |
| C1 | 0.0037 | 0.0051 | 0.0107 | 0.0034 |

Delays at 25°C, 1.8V, Typical Process

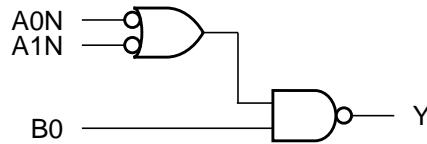
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.1124 | 0.1031 | 0.1007 | 0.2667 | 8.7625 | 6.1036 | 3.0517 | 1.1021 |
| A0 → Y↓ | 0.0774 | 0.0734 | 0.0708 | 0.2126 | 4.7549 | 3.2949 | 1.6336 | 0.6460 |
| A1 → Y↑ | 0.1233 | 0.1148 | 0.1114 | 0.2783 | 8.7581 | 6.1019 | 3.0506 | 1.1021 |
| A1 → Y↓ | 0.0873 | 0.0837 | 0.0805 | 0.2246 | 4.7593 | 3.2972 | 1.6346 | 0.6460 |
| B0 → Y↑ | 0.1511 | 0.1410 | 0.1383 | 0.3016 | 8.7316 | 6.0813 | 3.0408 | 1.1021 |
| B0 → Y↓ | 0.0867 | 0.0823 | 0.0797 | 0.2220 | 4.7543 | 3.2948 | 1.6335 | 0.6460 |
| B1 → Y↑ | 0.1614 | 0.1514 | 0.1489 | 0.3122 | 8.7282 | 6.0796 | 3.0399 | 1.1021 |
| B1 → Y↓ | 0.0963 | 0.0921 | 0.0894 | 0.2335 | 4.7589 | 3.2971 | 1.6347 | 0.6461 |
| C0 → Y↑ | 0.0692 | 0.0663 | 0.0620 | 0.2231 | 8.8048 | 6.1232 | 3.0612 | 1.1022 |
| C0 → Y↓ | 0.0557 | 0.0550 | 0.0519 | 0.1929 | 4.7508 | 3.2919 | 1.6320 | 0.6460 |
| C1 → Y↑ | 0.0779 | 0.0762 | 0.0740 | 0.2316 | 8.7954 | 6.1194 | 3.0603 | 1.1022 |
| C1 → Y↓ | 0.0632 | 0.0631 | 0.0622 | 0.2003 | 4.7643 | 3.2999 | 1.6340 | 0.6461 |

Cell Description

The OAI2BB1 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N})} \bullet B0$$

Logic Symbol



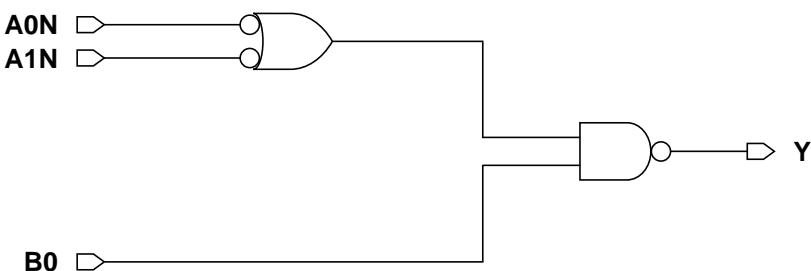
Functions

| A0N | A1N | B0 | Y |
|-----|-----|----|---|
| 1 | 1 | x | 1 |
| x | x | 0 | 1 |
| x | 0 | 1 | 0 |
| 0 | x | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI2BB1XL | 5.04 | 3.30 |
| OAI2BB1X1 | 5.04 | 3.30 |
| OAI2BB1X2 | 5.04 | 4.62 |
| OAI2BB1X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0231 | 0.0265 | 0.0461 | 0.0870 |
| A1N | 0.0198 | 0.0236 | 0.0413 | 0.0784 |
| B0 | 0.0110 | 0.0145 | 0.0271 | 0.0561 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0022 | 0.0021 | 0.0035 | 0.0059 |
| A1N | 0.0018 | 0.0017 | 0.0027 | 0.0045 |
| B0 | 0.0028 | 0.0037 | 0.0072 | 0.0132 |

Delays at 25°C, 1.8V, Typical Process

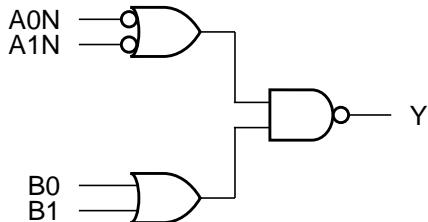
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0N → Y↑ | 0.0896 | 0.0954 | 0.0884 | 0.0937 | 5.8995 | 4.2094 | 2.0833 | 1.0418 |
| A0N → Y↓ | 0.1060 | 0.1181 | 0.1070 | 0.1014 | 4.1554 | 2.9562 | 1.4767 | 0.7443 |
| A1N → Y↑ | 0.0844 | 0.0884 | 0.0842 | 0.0896 | 5.8873 | 4.2096 | 2.0833 | 1.0419 |
| A1N → Y↓ | 0.0949 | 0.1066 | 0.0966 | 0.0926 | 4.1506 | 2.9541 | 1.4757 | 0.7438 |
| B0 → Y↑ | 0.0382 | 0.0373 | 0.0345 | 0.0357 | 5.8748 | 4.1967 | 2.0780 | 1.0390 |
| B0 → Y↓ | 0.0271 | 0.0280 | 0.0267 | 0.0282 | 4.1201 | 2.9382 | 1.4690 | 0.7411 |

Cell Description

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and one OR group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(A0N + A1N)} \bullet (B0 + B1)$$

Logic Symbol



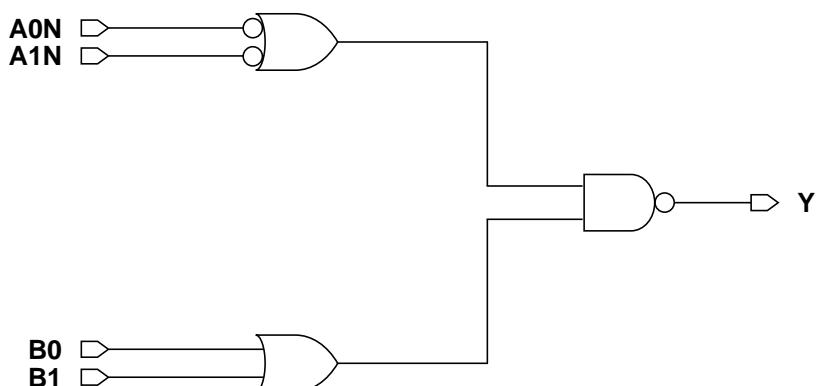
Functions

| A0N | A1N | B0 | B1 | Y |
|-----|-----|----|----|---|
| 1 | 1 | x | x | 1 |
| x | x | 0 | 0 | 1 |
| x | 0 | x | 1 | 0 |
| x | 0 | 1 | x | 0 |
| 0 | x | x | 1 | 0 |
| 0 | x | 1 | x | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI2BB2XL | 5.04 | 4.62 |
| OAI2BB2X1 | 5.04 | 4.62 |
| OAI2BB2X2 | 5.04 | 6.60 |
| OAI2BB2X4 | 5.04 | 9.90 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0260 | 0.0306 | 0.0565 | 0.1101 |
| A1N | 0.0207 | 0.0242 | 0.0447 | 0.0852 |
| B0 | 0.0150 | 0.0196 | 0.0381 | 0.0724 |
| B1 | 0.0177 | 0.0235 | 0.0470 | 0.0879 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0N | 0.0022 | 0.0022 | 0.0038 | 0.0083 |
| A1N | 0.0026 | 0.0025 | 0.0041 | 0.0078 |
| B0 | 0.0038 | 0.0050 | 0.0102 | 0.0199 |
| B1 | 0.0036 | 0.0048 | 0.0105 | 0.0186 |

Delays at 25°C, 1.8V, Typical Process

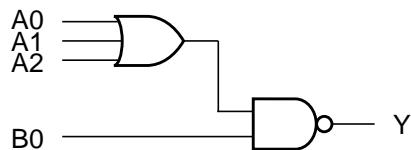
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0N → Y↑ | 0.0922 | 0.0977 | 0.0962 | 0.0933 | 5.9187 | 4.2222 | 2.1090 | 1.0455 |
| A0N → Y↓ | 0.1181 | 0.1305 | 0.1244 | 0.1217 | 4.1520 | 2.9536 | 1.4928 | 0.7478 |
| A1N → Y↑ | 0.0881 | 0.0934 | 0.0917 | 0.0877 | 5.8980 | 4.2084 | 2.1022 | 1.0421 |
| A1N → Y↓ | 0.0976 | 0.1090 | 0.1033 | 0.0990 | 4.1473 | 2.9524 | 1.4913 | 0.7474 |
| B0 → Y↑ | 0.0674 | 0.0620 | 0.0605 | 0.0585 | 8.7165 | 6.0750 | 3.0375 | 1.5107 |
| B0 → Y↓ | 0.0357 | 0.0354 | 0.0355 | 0.0351 | 4.1236 | 2.9394 | 1.4859 | 0.7450 |
| B1 → Y↑ | 0.0785 | 0.0731 | 0.0725 | 0.0692 | 8.7113 | 6.0724 | 3.0366 | 1.5100 |
| B1 → Y↓ | 0.0440 | 0.0441 | 0.0442 | 0.0439 | 4.1330 | 2.9436 | 1.4885 | 0.7460 |

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1 + A_2) \bullet B_0}$$

Logic Symbol



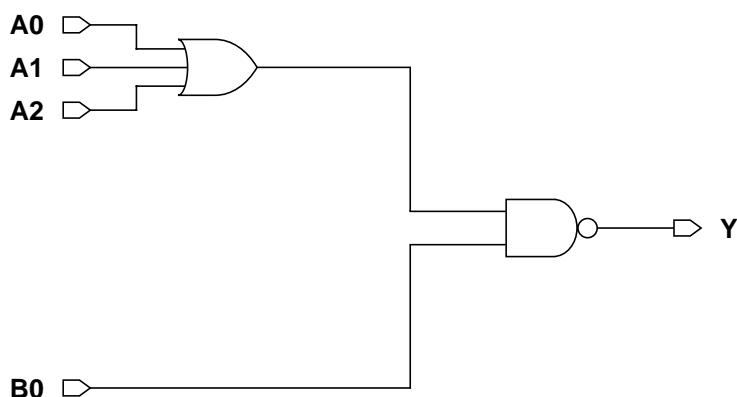
Functions

| A0 | A1 | A2 | B0 | Y |
|----|----|----|----|---|
| 0 | 0 | 0 | x | 1 |
| x | x | x | 0 | 1 |
| x | x | 1 | 1 | 0 |
| x | 1 | x | 1 | 0 |
| 1 | x | x | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI31XL | 5.04 | 3.96 |
| OAI31X1 | 5.04 | 3.96 |
| OAI31X2 | 5.04 | 5.94 |
| OAI31X4 | 5.04 | 5.94 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0195 | 0.0265 | 0.0550 | 0.0819 |
| A1 | 0.0237 | 0.0326 | 0.0675 | 0.0875 |
| A2 | 0.0273 | 0.0379 | 0.0787 | 0.0912 |
| B0 | 0.0186 | 0.0258 | 0.0493 | 0.0754 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0040 | 0.0052 | 0.0103 | 0.0038 |
| A1 | 0.0038 | 0.0050 | 0.0106 | 0.0036 |
| A2 | 0.0036 | 0.0049 | 0.0108 | 0.0035 |
| B0 | 0.0033 | 0.0043 | 0.0083 | 0.0032 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0815 | 0.0766 | 0.0804 | 0.2617 | 11.1182 | 7.7331 | 3.8675 | 1.0401 |
| A0 → Y↓ | 0.0350 | 0.0342 | 0.0353 | 0.1629 | 4.1127 | 2.9318 | 1.4759 | 0.6464 |
| A1 → Y↑ | 0.1083 | 0.1038 | 0.1078 | 0.2869 | 11.1107 | 7.7297 | 3.8659 | 1.0401 |
| A1 → Y↓ | 0.0451 | 0.0450 | 0.0462 | 0.1745 | 4.1251 | 2.9380 | 1.4789 | 0.6464 |
| A2 → Y↑ | 0.1174 | 0.1135 | 0.1191 | 0.2972 | 11.1096 | 7.7293 | 3.8663 | 1.0401 |
| A2 → Y↓ | 0.0498 | 0.0504 | 0.0526 | 0.1827 | 4.1698 | 2.9604 | 1.4903 | 0.6465 |
| B0 → Y↑ | 0.0336 | 0.0328 | 0.0315 | 0.1632 | 5.9028 | 4.2146 | 2.1074 | 1.0400 |
| B0 → Y↓ | 0.0384 | 0.0392 | 0.0384 | 0.1701 | 4.1635 | 2.9572 | 1.4887 | 0.6465 |

Cell Description

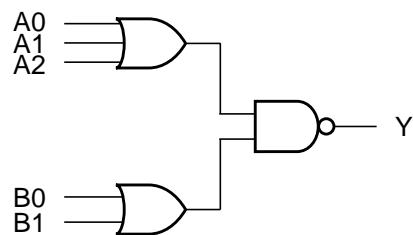
The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1 + A_2) \bullet (B_0 + B_1)}$$

Functions

| A0 | A1 | A2 | B0 | B1 | Y |
|----|----|----|----|----|---|
| 0 | 0 | 0 | x | x | 1 |
| x | x | x | 0 | 0 | 1 |
| x | x | 1 | x | 1 | 0 |
| x | x | 1 | 1 | x | 0 |
| x | 1 | x | 1 | x | 0 |
| x | 1 | x | x | 1 | 0 |
| 1 | x | x | 1 | x | 0 |
| 1 | x | x | x | 1 | 0 |

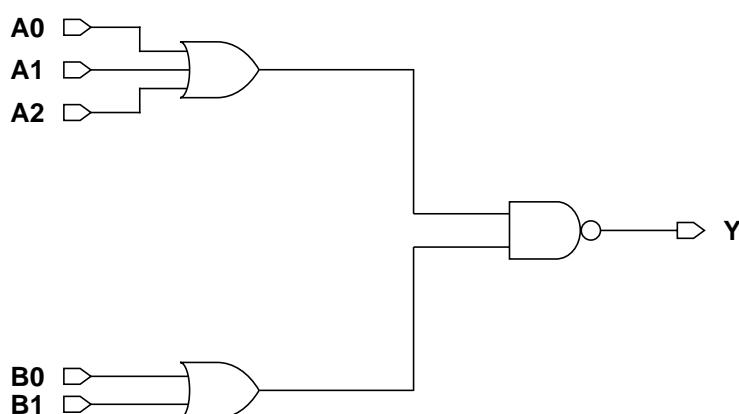
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI32XL | 5.04 | 4.62 |
| OAI32X1 | 5.04 | 4.62 |
| OAI32X2 | 5.04 | 7.26 |
| OAI32X4 | 5.04 | 6.60 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0280 | 0.0371 | 0.0714 | 0.0935 |
| A1 | 0.0323 | 0.0433 | 0.0843 | 0.0965 |
| A2 | 0.0361 | 0.0486 | 0.0953 | 0.0997 |
| B0 | 0.0217 | 0.0300 | 0.0598 | 0.0817 |
| B1 | 0.0251 | 0.0346 | 0.0694 | 0.0864 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0040 | 0.0054 | 0.0099 | 0.0037 |
| A1 | 0.0039 | 0.0053 | 0.0101 | 0.0037 |
| A2 | 0.0038 | 0.0050 | 0.0102 | 0.0033 |
| B0 | 0.0037 | 0.0051 | 0.0091 | 0.0036 |
| B1 | 0.0038 | 0.0049 | 0.0095 | 0.0034 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.1153 | 0.1059 | 0.1020 | 0.2931 | 11.1180 | 7.7342 | 3.8672 | 1.0400 |
| A0 → Y↓ | 0.0518 | 0.0501 | 0.0566 | 0.1795 | 4.1256 | 2.9382 | 1.7084 | 0.6464 |
| A1 → Y↑ | 0.1423 | 0.1328 | 0.1297 | 0.3196 | 11.1109 | 7.7307 | 3.8656 | 1.0400 |
| A1 → Y↓ | 0.0626 | 0.0614 | 0.0703 | 0.1921 | 4.1332 | 2.9420 | 1.7102 | 0.6464 |
| A2 → Y↑ | 0.1514 | 0.1423 | 0.1395 | 0.3282 | 11.1104 | 7.7306 | 3.8657 | 1.0400 |
| A2 → Y↓ | 0.0682 | 0.0677 | 0.0786 | 0.1999 | 4.1701 | 2.9606 | 1.7199 | 0.6465 |
| B0 → Y↑ | 0.0527 | 0.0505 | 0.0512 | 0.2098 | 8.7663 | 6.1064 | 3.0522 | 1.0402 |
| B0 → Y↓ | 0.0435 | 0.0443 | 0.0524 | 0.1752 | 4.1636 | 2.9573 | 1.7186 | 0.6465 |
| B1 → Y↑ | 0.0657 | 0.0622 | 0.0635 | 0.2214 | 8.7647 | 6.1046 | 3.0513 | 1.0402 |
| B1 → Y↓ | 0.0532 | 0.0537 | 0.0631 | 0.1834 | 4.1690 | 2.9594 | 1.7212 | 0.6465 |

Cell Description

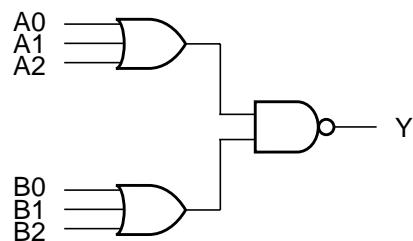
The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A_0 + A_1 + A_2) \bullet (B_0 + B_1 + B_2)}$$

Functions

| A0 | A1 | A2 | B0 | B1 | B2 | Y |
|----|----|----|----|----|----|---|
| 0 | 0 | 0 | x | x | x | 1 |
| x | x | x | 0 | 0 | 0 | 1 |
| x | x | 1 | x | x | 1 | 0 |
| x | x | 1 | x | 1 | x | 0 |
| x | x | 1 | 1 | x | x | 0 |
| x | 1 | x | x | x | 1 | 0 |
| x | 1 | x | x | 1 | x | 0 |
| 1 | x | x | x | x | 1 | 0 |
| 1 | x | x | x | 1 | x | 0 |
| 1 | x | x | 1 | x | x | 0 |

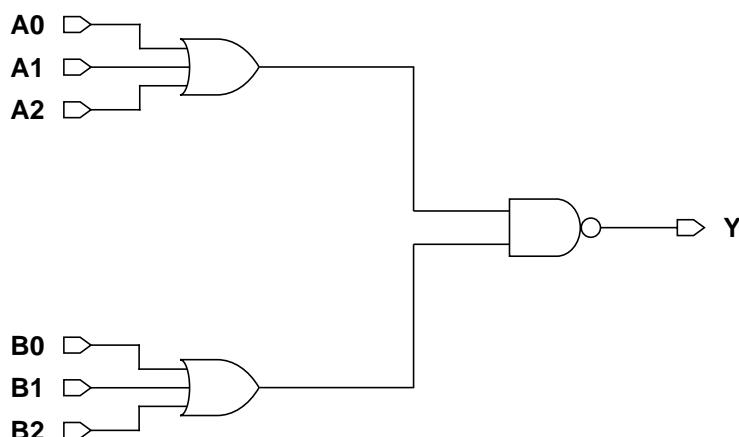
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| OAI33XL | 5.04 | 5.28 |
| OAI33X1 | 5.04 | 5.28 |
| OAI33X2 | 5.04 | 8.58 |
| OAI33X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0254 | 0.0350 | 0.0678 | 0.0908 |
| A1 | 0.0294 | 0.0404 | 0.0798 | 0.0942 |
| A2 | 0.0332 | 0.0465 | 0.0909 | 0.0973 |
| B0 | 0.0359 | 0.0490 | 0.0950 | 0.1040 |
| B1 | 0.0403 | 0.0553 | 0.1081 | 0.1076 |
| B2 | 0.0440 | 0.0607 | 0.1191 | 0.1113 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A0 | 0.0041 | 0.0054 | 0.0100 | 0.0039 |
| A1 | 0.0039 | 0.0052 | 0.0102 | 0.0036 |
| A2 | 0.0040 | 0.0053 | 0.0110 | 0.0035 |
| B0 | 0.0040 | 0.0054 | 0.0098 | 0.0038 |
| B1 | 0.0039 | 0.0052 | 0.0103 | 0.0035 |
| B2 | 0.0037 | 0.0051 | 0.0102 | 0.0035 |

Delays at 25°C, 1.8V, Typical Process

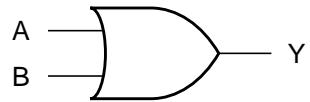
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A0 → Y↑ | 0.0731 | 0.0685 | 0.0659 | 0.2553 | 11.1977 | 7.7800 | 3.8890 | 1.0404 |
| A0 → Y↓ | 0.0487 | 0.0492 | 0.0562 | 0.1829 | 4.1585 | 2.9547 | 1.7175 | 0.6466 |
| A1 → Y↑ | 0.0995 | 0.0966 | 0.0932 | 0.2821 | 11.1892 | 7.7770 | 3.8877 | 1.0404 |
| A1 → Y↓ | 0.0601 | 0.0610 | 0.0708 | 0.1936 | 4.1604 | 2.9594 | 1.7173 | 0.6467 |
| A2 → Y↑ | 0.1106 | 0.1090 | 0.1051 | 0.2912 | 11.1907 | 7.7778 | 3.8883 | 1.0404 |
| A2 → Y↓ | 0.0677 | 0.0702 | 0.0811 | 0.2033 | 4.1896 | 2.9728 | 1.7258 | 0.6468 |
| B0 → Y↑ | 0.1399 | 0.1319 | 0.1268 | 0.3227 | 11.1138 | 7.7317 | 3.8655 | 1.0401 |
| B0 → Y↓ | 0.0650 | 0.0656 | 0.0739 | 0.1994 | 4.1668 | 2.9613 | 1.7197 | 0.6467 |
| B1 → Y↑ | 0.1669 | 0.1585 | 0.1548 | 0.3484 | 11.1084 | 7.7286 | 3.8645 | 1.0401 |
| B1 → Y↓ | 0.0767 | 0.0776 | 0.0885 | 0.2120 | 4.1679 | 2.9615 | 1.7197 | 0.6467 |
| B2 → Y↑ | 0.1762 | 0.1679 | 0.1645 | 0.3584 | 11.1071 | 7.7282 | 3.8644 | 1.0401 |
| B2 → Y↓ | 0.0834 | 0.0850 | 0.0979 | 0.2214 | 4.1961 | 2.9756 | 1.7272 | 0.6468 |

Cell Description

The OR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A + B)$$

Logic Symbol



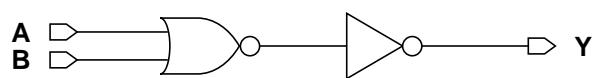
Functions

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| x | 1 | 1 |
| 1 | x | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| OR2XL | 5.04 | 2.64 |
| OR2X1 | 5.04 | 2.64 |
| OR2X2 | 5.04 | 2.64 |
| OR2X4 | 5.04 | 3.96 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0191 | 0.0227 | 0.0362 | 0.0687 |
| B | 0.0222 | 0.0259 | 0.0418 | 0.0783 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0027 | 0.0027 | 0.0037 | 0.0065 |
| B | 0.0029 | 0.0029 | 0.0040 | 0.0064 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0617 | 0.0652 | 0.0667 | 0.0640 |
| A → Y↓ | 0.1180 | 0.1329 | 0.1220 | 0.1274 |
| B → Y↑ | 0.0697 | 0.0726 | 0.0735 | 0.0717 |
| B → Y↓ | 0.1334 | 0.1483 | 0.1365 | 0.1396 |

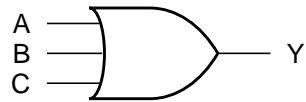
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8828 | 4.2003 | 2.2041 | 1.0401 |
| A → Y↓ | 3.5463 | 2.5701 | 1.3085 | 0.6562 |
| B → Y↑ | 5.8857 | 4.2052 | 2.2049 | 1.0404 |
| B → Y↓ | 3.5462 | 2.5701 | 1.3084 | 0.6561 |

Cell Description

The OR3 cell provides the logical OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (A + B + C)$$

Logic Symbol



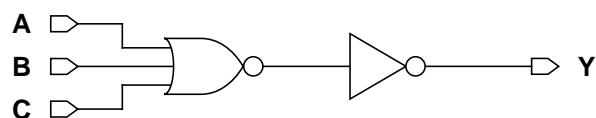
Functions

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| x | x | 1 | 1 |
| x | 1 | x | 1 |
| 1 | x | x | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| OR3XL | 5.04 | 3.30 |
| OR3X1 | 5.04 | 3.96 |
| OR3X2 | 5.04 | 3.96 |
| OR3X4 | 5.04 | 5.94 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0234 | 0.0265 | 0.0427 | 0.0818 |
| B | 0.0259 | 0.0291 | 0.0475 | 0.0923 |
| C | 0.0285 | 0.0317 | 0.0519 | 0.1014 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0032 | 0.0029 | 0.0041 | 0.0077 |
| B | 0.0029 | 0.0027 | 0.0039 | 0.0080 |
| C | 0.0028 | 0.0027 | 0.0039 | 0.0082 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0674 | 0.0696 | 0.0724 | 0.0701 |
| A → Y↓ | 0.1577 | 0.1712 | 0.1602 | 0.1528 |
| B → Y↑ | 0.0752 | 0.0773 | 0.0822 | 0.0808 |
| B → Y↓ | 0.1836 | 0.1976 | 0.1871 | 0.1806 |
| C → Y↑ | 0.0790 | 0.0815 | 0.0867 | 0.0859 |
| C → Y↓ | 0.1948 | 0.2083 | 0.1977 | 0.1919 |

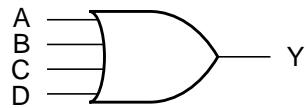
| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8824 | 4.1999 | 2.1528 | 1.0934 |
| A → Y↓ | 3.6813 | 2.6291 | 1.3365 | 0.6678 |
| B → Y↑ | 5.8865 | 4.2018 | 2.1540 | 1.0939 |
| B → Y↓ | 3.6812 | 2.6291 | 1.3365 | 0.6678 |
| C → Y↑ | 5.8967 | 4.2062 | 2.1563 | 1.0952 |
| C → Y↓ | 3.6813 | 2.6290 | 1.3365 | 0.6678 |

Cell Description

The OR4 cell provides the logical OR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A + B + C + D)$$

Logic Symbol



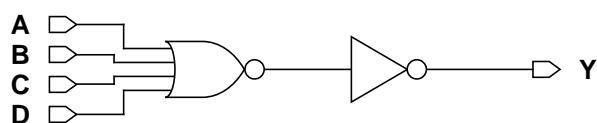
Functions

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| x | x | x | 1 | 1 |
| x | x | 1 | x | 1 |
| x | 1 | x | x | 1 |
| 1 | x | x | x | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| OR4XL | 5.04 | 3.96 |
| OR4X1 | 5.04 | 3.96 |
| OR4X2 | 5.04 | 3.96 |
| OR4X4 | 5.04 | 7.26 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0261 | 0.0307 | 0.0479 | 0.0950 |
| B | 0.0291 | 0.0337 | 0.0534 | 0.1052 |
| C | 0.0322 | 0.0370 | 0.0589 | 0.1176 |
| D | 0.0357 | 0.0404 | 0.0642 | 0.1294 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0031 | 0.0031 | 0.0046 | 0.0086 |
| B | 0.0028 | 0.0028 | 0.0045 | 0.0088 |
| C | 0.0032 | 0.0032 | 0.0043 | 0.0090 |
| D | 0.0034 | 0.0034 | 0.0044 | 0.0098 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | |
|-------------|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 0.0725 | 0.0762 | 0.0762 | 0.0767 |
| A → Y↓ | 0.1812 | 0.2061 | 0.1775 | 0.1747 |
| B → Y↑ | 0.0816 | 0.0838 | 0.0885 | 0.0904 |
| B → Y↓ | 0.2233 | 0.2482 | 0.2201 | 0.2194 |
| C → Y↑ | 0.0886 | 0.0924 | 0.0957 | 0.0964 |
| C → Y↓ | 0.2522 | 0.2772 | 0.2451 | 0.2438 |
| D → Y↑ | 0.0927 | 0.0974 | 0.0992 | 0.1025 |
| D → Y↓ | 0.2659 | 0.2912 | 0.2566 | 0.2570 |

Delay Table at 25°C, 1.8V, Typical Process

| Description | K _{load} (ns/pF) | | | |
|-------------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A → Y↑ | 5.8836 | 4.2012 | 2.1531 | 1.1130 |
| A → Y↓ | 3.8425 | 2.7169 | 1.3679 | 0.6718 |
| B → Y↑ | 5.8875 | 4.2000 | 2.1541 | 1.1135 |
| B → Y↓ | 3.8430 | 2.7168 | 1.3679 | 0.6718 |
| C → Y↑ | 5.8954 | 4.2081 | 2.1570 | 1.1149 |
| C → Y↓ | 3.8430 | 2.7168 | 1.3679 | 0.6718 |
| D → Y↑ | 5.9152 | 4.2159 | 2.1616 | 1.1173 |
| D → Y↓ | 3.8420 | 2.7166 | 1.3678 | 0.6718 |

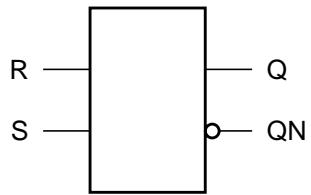
Cell Description

The RSLAT cell is an RS-type latch with active-high set (S) and reset (R).

Functions

| R | S | Q[n+1] | QN[n+1] |
|---|---|--------|---------|
| 0 | 0 | Q[n] | QN[n] |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | IL | IL |

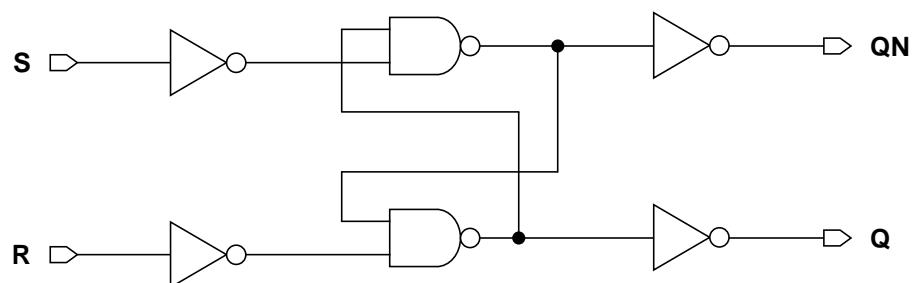
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| RSLATXL | 5.04 | 6.60 |
| RSLATX1 | 5.04 | 6.60 |
| RSLATX2 | 5.04 | 7.92 |
| RSLATX4 | 5.04 | 11.88 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S | 0.0095 | 0.0101 | 0.0134 | 0.0253 |
| R | 0.0096 | 0.0108 | 0.0151 | 0.0253 |
| Q | 0.0429 | 0.0545 | 0.0930 | 0.1717 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| S | 0.0024 | 0.0025 | 0.0028 | 0.0047 |
| R | 0.0025 | 0.0026 | 0.0028 | 0.0047 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| S → Q↑ | 0.2402 | 0.2201 | 0.2056 | 0.1930 | 5.9094 | 4.2104 | 2.1310 | 1.0418 |
| R → Q↑ | 0.1668 | 0.1595 | 0.1543 | 0.1404 | 5.9088 | 4.2103 | 2.1312 | 1.0418 |
| R → Q↓ | 0.1601 | 0.1482 | 0.1388 | 0.1320 | 3.5372 | 2.5444 | 1.2943 | 0.6474 |
| S → QN↑ | 0.1538 | 0.1501 | 0.1540 | 0.1373 | 5.9082 | 4.2088 | 2.1313 | 1.0417 |
| S → QN↓ | 0.1488 | 0.1405 | 0.1397 | 0.1292 | 3.5328 | 2.5439 | 1.2947 | 0.6473 |
| R → QN↑ | 0.2489 | 0.2232 | 0.2072 | 0.1946 | 5.9094 | 4.2093 | 2.1314 | 1.0417 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|--------|--------|--------|
| | | XL | X1 | X2 | X4 |
| S | minpwh | 0.1273 | 0.1078 | 0.1030 | 0.0981 |
| R | minpwh | 0.1224 | 0.1078 | 0.1030 | 0.0981 |

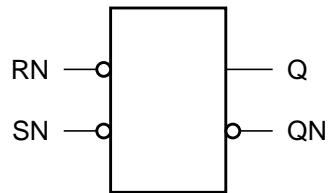
Cell Description

The RSLATN cell is an RS-type latch with active-low set (SN) and reset (RN).

Function

| RN | SN | Q[n+1] | QN[n+1] |
|----|----|--------|---------|
| 0 | 0 | IL | IL |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Q[n] | QN[n] |

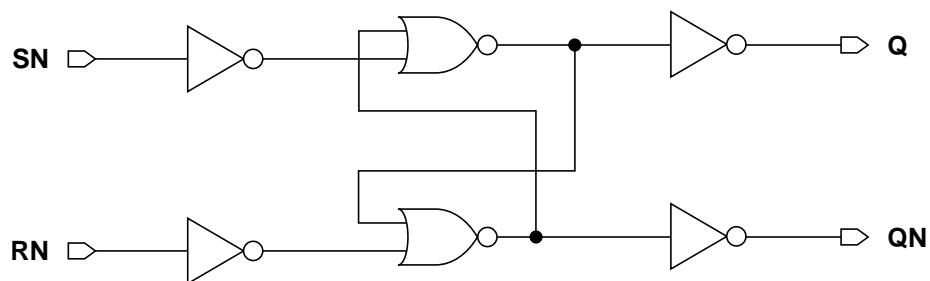
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| RSLATNXL | 5.04 | 6.60 |
| RSLATNX1 | 5.04 | 7.26 |
| RSLATNX2 | 5.04 | 7.26 |
| RSLATNX4 | 5.04 | 11.88 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SN | 0.0116 | 0.0126 | 0.0170 | 0.0334 |
| RN | 0.0116 | 0.0119 | 0.0181 | 0.0332 |
| Q | 0.0448 | 0.0558 | 0.0978 | 0.1780 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SN | 0.0024 | 0.0024 | 0.0030 | 0.0051 |
| RN | 0.0025 | 0.0025 | 0.0032 | 0.0052 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| SN → Q↑ | 0.1481 | 0.1535 | 0.1446 | 0.1368 | 5.9002 | 4.2063 | 2.1303 | 1.0652 |
| SN → Q↓ | 0.1996 | 0.1777 | 0.1647 | 0.1567 | 3.4164 | 2.5818 | 1.3114 | 0.6550 |
| RN → Q↓ | 0.2988 | 0.2845 | 0.2674 | 0.2480 | 3.4167 | 2.5818 | 1.3115 | 0.6550 |
| SN → QN↓ | 0.3010 | 0.2831 | 0.2615 | 0.2477 | 3.4200 | 2.5829 | 1.3109 | 0.6549 |
| RN → QN↑ | 0.1492 | 0.1553 | 0.1477 | 0.1380 | 5.9000 | 4.2060 | 2.1301 | 1.0651 |
| RN → QN↓ | 0.2006 | 0.1795 | 0.1660 | 0.1575 | 3.4200 | 2.5829 | 1.3109 | 0.6549 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|--------|--------|--------|
| | | XL | X1 | X2 | X4 |
| SN | minpwl | 0.1321 | 0.1370 | 0.1273 | 0.1224 |
| RN | minpwl | 0.1418 | 0.1467 | 0.1321 | 0.1273 |

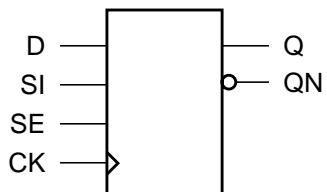
Cell Description

The SDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Functions

| D | SI | SE | CK | Q[n+1] | QN[n+1] |
|---|----|----|----|--------|---------|
| 1 | x | 0 | / | 1 | 0 |
| 0 | x | 0 | / | 0 | 1 |
| x | x | x | \ | Q[n] | QN[n] |
| x | 1 | 1 | / | 1 | 0 |
| x | 0 | 1 | / | 0 | 1 |

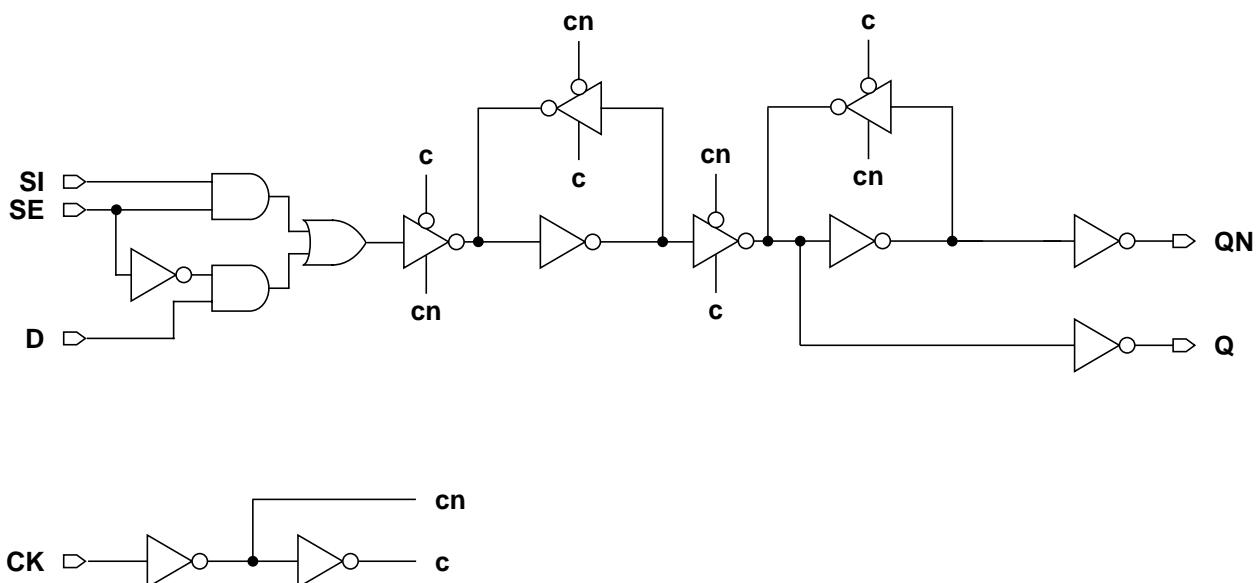
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFXL | 5.04 | 13.20 |
| SDFFX1 | 5.04 | 13.86 |
| SDFFX2 | 5.04 | 16.50 |
| SDFFX4 | 5.04 | 19.14 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0430 | 0.0404 | 0.0505 | 0.0785 |
| SE | 0.0496 | 0.0461 | 0.0559 | 0.0815 |
| D | 0.0365 | 0.0346 | 0.0442 | 0.0675 |
| CK | 0.0414 | 0.0399 | 0.0462 | 0.0700 |
| Q | 0.0396 | 0.0434 | 0.0736 | 0.1192 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0026 | 0.0024 | 0.0025 | 0.0024 |
| SE | 0.0054 | 0.0046 | 0.0048 | 0.0055 |
| D | 0.0031 | 0.0021 | 0.0024 | 0.0034 |
| CK | 0.0024 | 0.0030 | 0.0040 | 0.0064 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2542 | 0.2183 | 0.2015 | 0.1691 | 5.3213 | 4.0666 | 2.1053 | 1.0782 |
| CK → Q↓ | 0.2081 | 0.1759 | 0.1616 | 0.1412 | 3.6149 | 2.6525 | 1.3253 | 0.6534 |
| CK → QN↑ | 0.2726 | 0.2369 | 0.2125 | 0.1924 | 5.8908 | 4.2043 | 2.1011 | 1.0765 |
| CK → QN↓ | 0.3444 | 0.3035 | 0.2783 | 0.2378 | 3.7944 | 2.5431 | 1.2685 | 0.6463 |

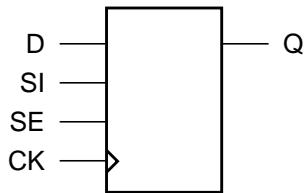
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1367 | 0.1367 | 0.1602 | 0.1875 |
| | setup↓ → CK | 0.3047 | 0.3477 | 0.3633 | 0.4336 |
| | hold↑ → CK | -0.1094 | -0.1016 | -0.1211 | -0.1445 |
| | hold↓ → CK | -0.1875 | -0.2383 | -0.2383 | -0.3086 |
| SE | setup↑ → CK | 0.3320 | 0.3711 | 0.3828 | 0.4688 |
| | setup↓ → CK | 0.1875 | 0.3398 | 0.3047 | 0.2617 |
| | hold↑ → CK | -0.1016 | -0.0859 | -0.1055 | -0.1289 |
| | hold↓ → CK | -0.0703 | -0.1406 | -0.1602 | -0.1406 |
| D | setup↑ → CK | 0.0898 | 0.1133 | 0.1367 | 0.1172 |
| | setup↓ → CK | 0.1875 | 0.3516 | 0.3125 | 0.2617 |
| | hold↑ → CK | -0.0703 | -0.0859 | -0.0977 | -0.0859 |
| | hold↓ → CK | -0.0742 | -0.2422 | -0.1914 | -0.1523 |
| CK | minpwh | 0.1418 | 0.1224 | 0.1078 | 0.0981 |
| | minpwl | 0.2099 | 0.2001 | 0.2001 | 0.1661 |

Cell Description

The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



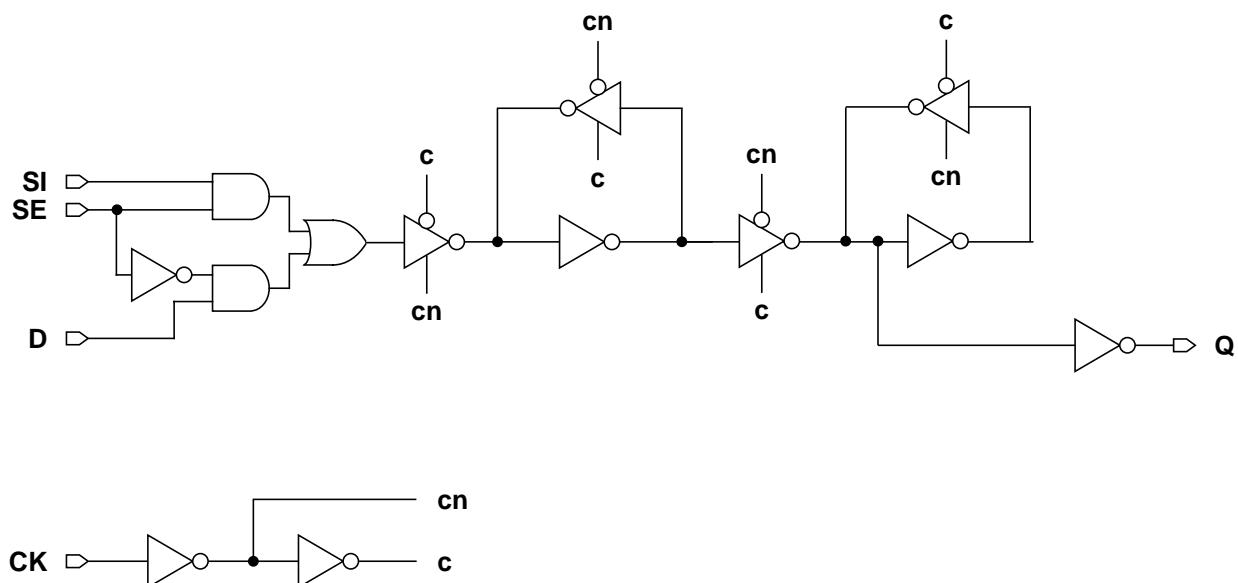
Functions

| D | SI | SE | CK | Q[n+1] |
|---|----|----|----|--------|
| 1 | x | 0 | / | 1 |
| 0 | x | 0 | / | 0 |
| x | x | x | \ | Q[n] |
| x | 1 | 1 | / | 1 |
| x | 0 | 1 | / | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| SDFFHQXL | 5.04 | 13.20 |
| SDFFHQX1 | 5.04 | 13.20 |
| SDFFHQX2 | 5.04 | 15.84 |
| SDFFHQX4 | 5.04 | 17.16 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0472 | 0.0507 | 0.0674 | 0.0940 |
| SE | 0.0526 | 0.0565 | 0.0734 | 0.0963 |
| D | 0.0409 | 0.0458 | 0.0615 | 0.0823 |
| CK | 0.0425 | 0.0420 | 0.0471 | 0.0604 |
| Q | 0.0280 | 0.0305 | 0.0473 | 0.0707 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0025 | 0.0025 | 0.0025 | 0.0024 |
| SE | 0.0051 | 0.0047 | 0.0047 | 0.0052 |
| D | 0.0028 | 0.0021 | 0.0023 | 0.0029 |
| CK | 0.0024 | 0.0031 | 0.0037 | 0.0053 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2260 | 0.1895 | 0.1871 | 0.1596 | 5.9104 | 4.0636 | 2.1035 | 1.0408 |
| CK → Q↓ | 0.2235 | 0.1725 | 0.1687 | 0.1436 | 3.7100 | 2.6899 | 1.3442 | 0.6530 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1484 | 0.1523 | 0.1602 | 0.1914 |
| | setup↓ → CK | 0.3750 | 0.4062 | 0.4258 | 0.4609 |
| | hold↑ → CK | -0.1094 | -0.1094 | -0.1133 | -0.1289 |
| | hold↓ → CK | -0.1875 | -0.2461 | -0.2383 | -0.2852 |
| SE | setup↑ → CK | 0.4023 | 0.4375 | 0.4414 | 0.4766 |
| | setup↓ → CK | 0.2734 | 0.3945 | 0.3906 | 0.3320 |
| | hold↑ → CK | -0.0898 | -0.0859 | -0.0938 | -0.1211 |
| | hold↓ → CK | -0.1016 | -0.1523 | -0.1523 | -0.1484 |
| D | setup↑ → CK | 0.1016 | 0.1328 | 0.1445 | 0.1445 |
| | setup↓ → CK | 0.2734 | 0.4062 | 0.3906 | 0.3320 |
| | hold↑ → CK | -0.0664 | -0.0859 | -0.0938 | -0.0938 |
| | hold↓ → CK | -0.1055 | -0.2461 | -0.2148 | -0.1680 |
| CK | minpwh | 0.1418 | 0.1176 | 0.1176 | 0.0981 |
| | minpw1 | 0.2099 | 0.2001 | 0.1904 | 0.1710 |

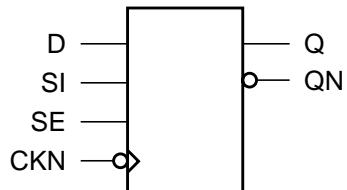
Cell Description

The SDFFN cell is a negative-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Functions

| D | SI | SE | CKN | Q[n+1] | QN[n+1] |
|---|----|----|-----|--------|---------|
| 1 | x | 0 | — | 1 | 0 |
| 0 | x | 0 | — | 0 | 1 |
| x | x | x | — | Q[n] | QN[n] |
| x | 1 | 1 | — | 1 | 0 |
| x | 0 | 1 | — | 0 | 1 |

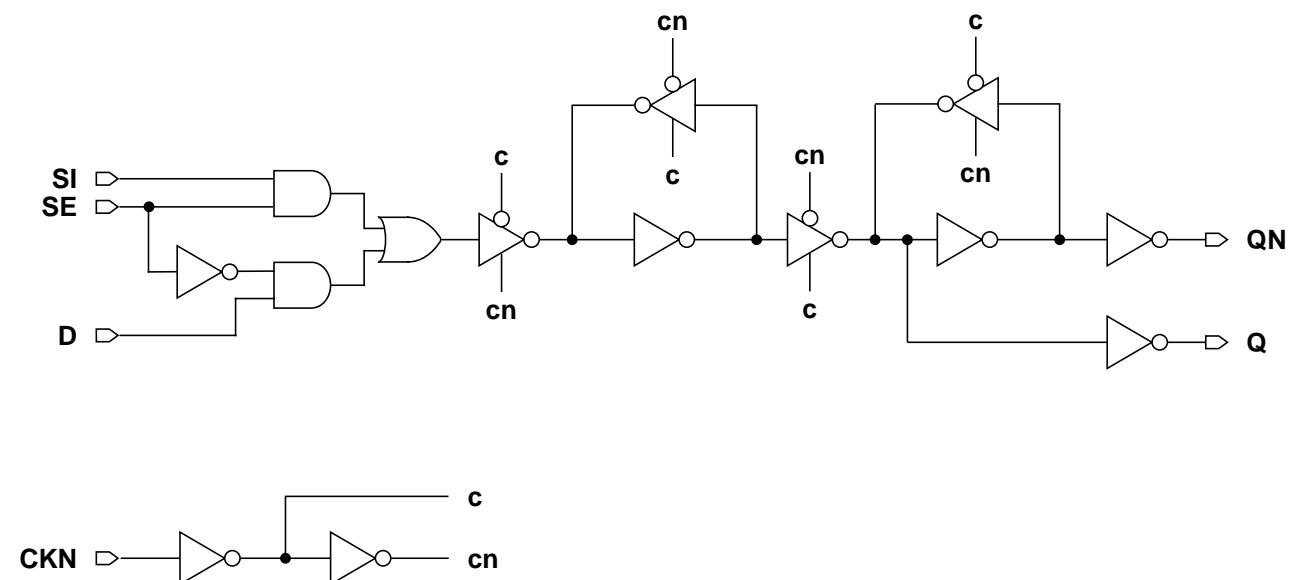
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFNXL | 5.04 | 13.86 |
| SDFFNX1 | 5.04 | 13.86 |
| SDFFNX2 | 5.04 | 16.50 |
| SDFFNX4 | 5.04 | 18.48 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0437 | 0.0417 | 0.0516 | 0.0782 |
| SE | 0.0507 | 0.0475 | 0.0570 | 0.0815 |
| D | 0.0371 | 0.0361 | 0.0453 | 0.0677 |
| CKN | 0.0376 | 0.0405 | 0.0550 | 0.0844 |
| Q | 0.0378 | 0.0437 | 0.0779 | 0.1283 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0024 | 0.0022 | 0.0023 | 0.0022 |
| SE | 0.0050 | 0.0045 | 0.0046 | 0.0051 |
| D | 0.0027 | 0.0019 | 0.0022 | 0.0030 |
| CKN | 0.0023 | 0.0030 | 0.0040 | 0.0064 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.1945 | 0.1566 | 0.1427 | 0.1202 | 5.3253 | 4.0698 | 2.1067 | 1.0601 |
| CKN → Q↓ | 0.3234 | 0.2783 | 0.2535 | 0.2185 | 3.5961 | 2.6523 | 1.3251 | 0.6750 |
| CKN → QN↑ | 0.3867 | 0.3390 | 0.3054 | 0.2709 | 5.8914 | 4.2043 | 2.1012 | 1.0581 |
| CKN → QN↓ | 0.2833 | 0.2425 | 0.2208 | 0.1895 | 3.5169 | 2.5432 | 1.2689 | 0.6686 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CKN | 0.1289 | 0.1406 | 0.1758 | 0.1992 |
| | setup↓ → CKN | 0.3086 | 0.3438 | 0.3555 | 0.4219 |
| | hold↑ → CKN | 0.0273 | 0.0039 | -0.0195 | -0.0508 |
| | hold↓ → CKN | -0.2695 | -0.2930 | -0.2969 | -0.3516 |
| SE | setup↑ → CKN | 0.3281 | 0.3672 | 0.3750 | 0.4453 |
| | setup↓ → CKN | 0.1797 | 0.3320 | 0.2930 | 0.2383 |
| | hold↑ → CKN | 0.0352 | 0.0156 | -0.0078 | -0.0430 |
| | hold↓ → CKN | -0.0117 | -0.0508 | -0.0742 | -0.0664 |
| D | setup↑ → CKN | 0.0859 | 0.1250 | 0.1562 | 0.1328 |
| | setup↓ → CKN | 0.1797 | 0.3398 | 0.3008 | 0.2383 |
| | hold↑ → CKN | 0.0430 | 0.0078 | -0.0156 | -0.0078 |
| | hold↓ → CKN | -0.1523 | -0.2852 | -0.2461 | -0.1953 |
| CKN | minpwl | 0.2050 | 0.1661 | 0.1516 | 0.1273 |
| | minpwh | 0.1516 | 0.1759 | 0.1807 | 0.1418 |

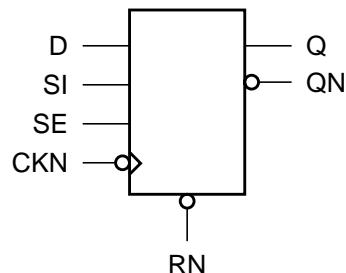
Cell Description

The SDFFNR cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Functions

| RN | D | SI | SE | CKN | Q[n+1] | QN[n+1] |
|----|---|----|----|-----|--------|---------|
| 1 | 1 | x | 0 | — | 1 | 0 |
| 1 | 0 | x | 0 | — | 0 | 1 |
| 1 | x | x | x | — | Q[n] | QN[n] |
| 1 | x | 1 | 1 | — | 1 | 0 |
| 1 | x | 0 | 1 | — | 0 | 1 |
| 0 | x | x | x | x | 0 | 1 |

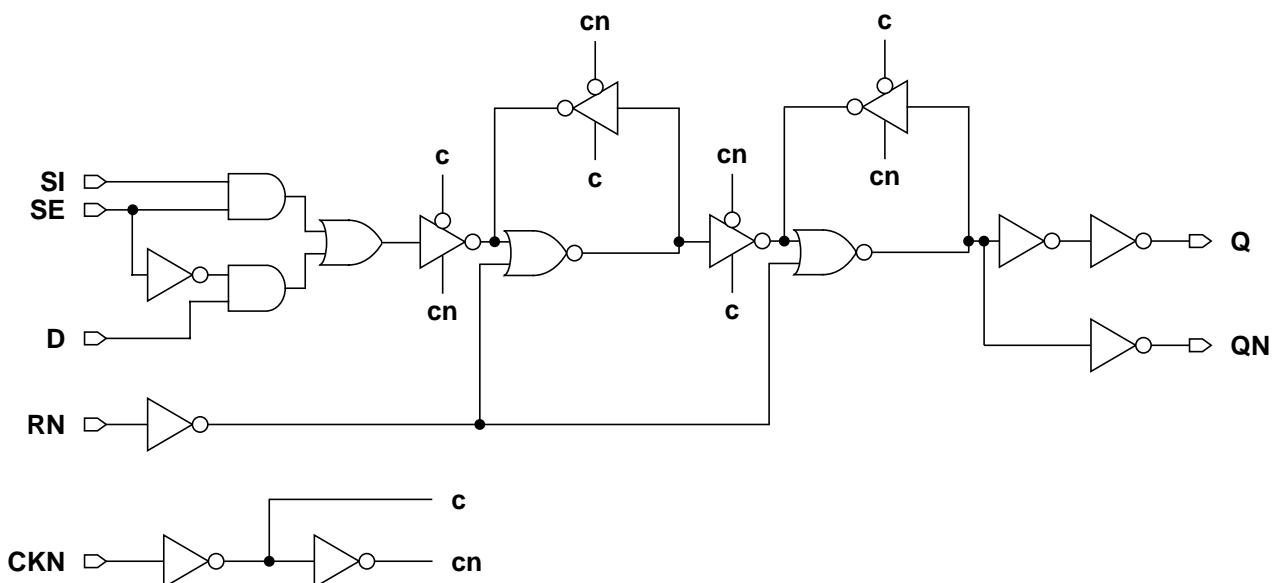
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFNRXL | 5.04 | 18.48 |
| SDFFNRX1 | 5.04 | 17.82 |
| SDFFNRX2 | 5.04 | 19.80 |
| SDFFNRX4 | 5.04 | 23.10 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0448 | 0.0405 | 0.0445 | 0.0549 |
| SE | 0.0518 | 0.0460 | 0.0516 | 0.0613 |
| D | 0.0384 | 0.0347 | 0.0389 | 0.0481 |
| CKN | 0.0385 | 0.0369 | 0.0460 | 0.0568 |
| RN | 0.0167 | 0.0184 | 0.0224 | 0.0340 |
| Q | 0.0479 | 0.0556 | 0.0860 | 0.1525 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0022 | 0.0022 | 0.0023 | 0.0022 |
| SE | 0.0050 | 0.0044 | 0.0047 | 0.0051 |
| D | 0.0027 | 0.0020 | 0.0020 | 0.0025 |
| CKN | 0.0026 | 0.0030 | 0.0033 | 0.0040 |
| RN | 0.0025 | 0.0029 | 0.0035 | 0.0060 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.3894 | 0.3403 | 0.3271 | 0.2991 | 5.8853 | 4.2032 | 2.0799 | 1.0642 |
| CKN → Q↓ | 0.4515 | 0.4386 | 0.4379 | 0.3900 | 3.4685 | 2.5308 | 1.4337 | 0.6516 |
| RN → Q↓ | 0.2501 | 0.2541 | 0.2392 | 0.2215 | 3.4690 | 2.5309 | 1.4337 | 0.6517 |
| CKN → QN↑ | 0.3994 | 0.3738 | 0.3632 | 0.3224 | 5.8845 | 4.2050 | 2.0812 | 1.0648 |
| CKN → QN↓ | 0.3584 | 0.3026 | 0.2774 | 0.2470 | 3.6990 | 2.5958 | 1.4564 | 0.6628 |
| RN → QN↑ | 0.1983 | 0.1899 | 0.1651 | 0.1543 | 5.8969 | 4.2089 | 2.0832 | 1.0662 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CKN | 0.1289 | 0.1445 | 0.1797 | 0.1797 |
| | setup↓ → CKN | 0.3164 | 0.3516 | 0.3789 | 0.3750 |
| | hold↑ → CKN | 0.0312 | -0.0039 | -0.0078 | -0.0273 |
| | hold↓ → CKN | -0.2734 | -0.3008 | -0.3281 | -0.3203 |
| SE | setup↑ → CKN | 0.3359 | 0.3750 | 0.3984 | 0.3906 |
| | setup↓ → CKN | 0.1836 | 0.3320 | 0.3672 | 0.2773 |
| | hold↑ → CKN | 0.0430 | 0.0078 | 0.0078 | -0.0117 |
| | hold↓ → CKN | 0.0000 | -0.0625 | -0.0625 | -0.0742 |
| D | setup↑ → CKN | 0.0859 | 0.1289 | 0.1602 | 0.1523 |
| | setup↓ → CKN | 0.1836 | 0.3398 | 0.3711 | 0.2812 |
| | hold↑ → CKN | 0.0547 | 0.0000 | -0.0039 | -0.0156 |
| | hold↓ → CKN | -0.1484 | -0.2852 | -0.3125 | -0.2305 |
| CKN | minpwl | 0.2196 | 0.2001 | 0.1953 | 0.1661 |
| | minpwh | 0.1613 | 0.1807 | 0.2050 | 0.1807 |
| RN | minpwl | 0.1856 | 0.1856 | 0.2050 | 0.3022 |
| | recovery | 0.0352 | 0.0703 | 0.0898 | 0.0742 |

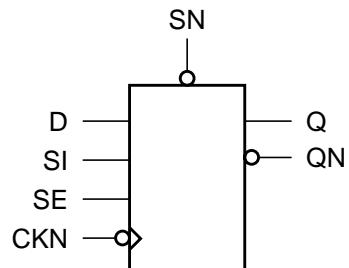
Cell Description

The SDFFNS cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Functions

| SN | D | SI | SE | CKN | Q[n+1] | QN[n+1] |
|----|---|----|----|-----|--------|---------|
| 1 | 1 | x | 0 | — | 1 | 0 |
| 1 | 0 | x | 0 | — | 0 | 1 |
| 1 | x | x | x | — | Q[n] | QN[n] |
| 1 | x | 1 | 1 | — | 1 | 0 |
| 1 | x | 0 | 1 | — | 0 | 1 |
| 0 | x | x | x | x | 1 | 0 |

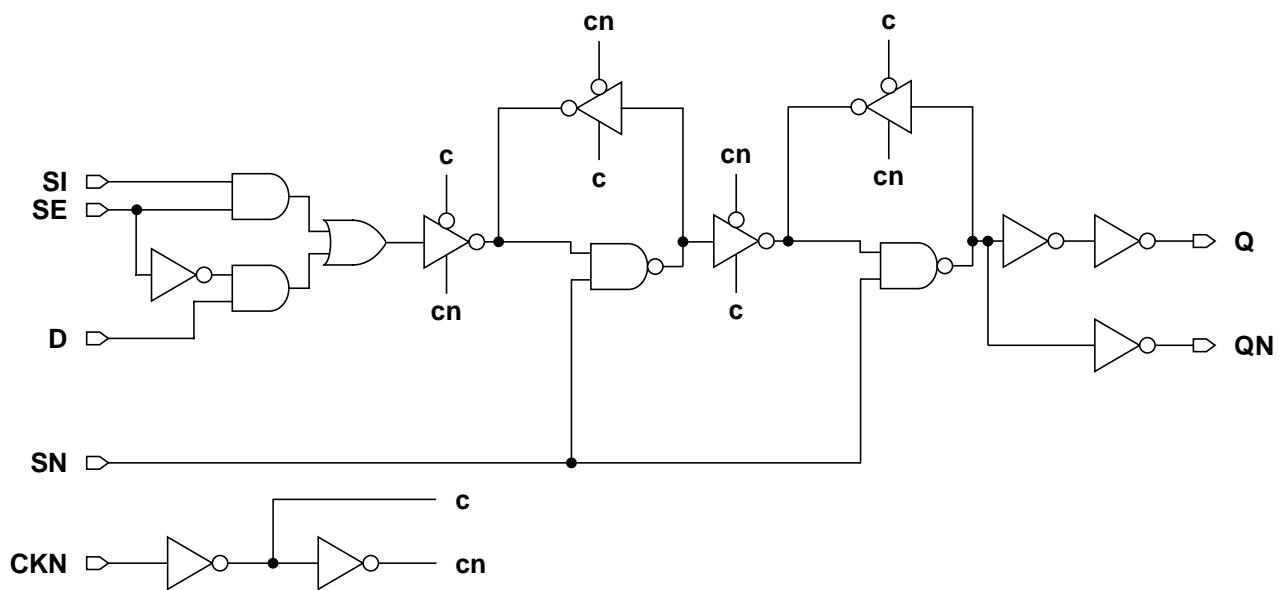
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFNSXL | 5.04 | 15.84 |
| SDFFNSX1 | 5.04 | 15.84 |
| SDFFNSX2 | 5.04 | 16.50 |
| SDFFNSX4 | 5.04 | 21.78 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0440 | 0.0381 | 0.0415 | 0.0504 |
| SE | 0.0510 | 0.0441 | 0.0476 | 0.0562 |
| D | 0.0376 | 0.0323 | 0.0357 | 0.0440 |
| CKN | 0.0368 | 0.0358 | 0.0388 | 0.0510 |
| SN | 0.0066 | 0.0074 | 0.0104 | 0.0177 |
| Q | 0.0427 | 0.0516 | 0.0829 | 0.1481 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0021 | 0.0021 | 0.0021 | 0.0021 |
| SE | 0.0051 | 0.0046 | 0.0046 | 0.0048 |
| D | 0.0027 | 0.0019 | 0.0019 | 0.0020 |
| CKN | 0.0024 | 0.0029 | 0.0029 | 0.0036 |
| SN | 0.0050 | 0.0055 | 0.0073 | 0.0124 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.3121 | 0.2844 | 0.2876 | 0.2716 | 5.8865 | 4.2019 | 2.0797 | 1.0579 |
| CKN → Q↓ | 0.4278 | 0.4130 | 0.4072 | 0.3829 | 3.4685 | 2.5299 | 1.2926 | 0.6462 |
| SN → Q↑ | 0.1677 | 0.1529 | 0.1574 | 0.1521 | 5.8865 | 4.2020 | 2.0797 | 1.0579 |
| CKN → QN↑ | 0.3810 | 0.3546 | 0.3362 | 0.3154 | 5.9029 | 4.2070 | 2.0843 | 1.0602 |
| CKN → QN↓ | 0.2816 | 0.2474 | 0.2365 | 0.2198 | 3.5404 | 2.5418 | 1.2975 | 0.6486 |
| SN → QN↓ | 0.1374 | 0.1161 | 0.1065 | 0.1006 | 3.5302 | 2.5423 | 1.3000 | 0.6509 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CKN | 0.1094 | 0.1211 | 0.1250 | 0.1445 |
| | setup↓ → CKN | 0.3164 | 0.3438 | 0.3516 | 0.3594 |
| | hold↑ → CKN | 0.0273 | 0.0000 | 0.0039 | -0.0156 |
| | hold↓ → CKN | -0.2852 | -0.3047 | -0.3086 | -0.3164 |
| SE | setup↑ → CKN | 0.3359 | 0.3672 | 0.3750 | 0.3789 |
| | setup↓ → CKN | 0.1836 | 0.3281 | 0.3359 | 0.2969 |
| | hold↑ → CKN | 0.0352 | 0.0117 | 0.0156 | 0.0000 |
| | hold↓ → CKN | -0.0078 | -0.0547 | -0.0547 | -0.0703 |
| D | setup↑ → CKN | 0.0664 | 0.1094 | 0.1094 | 0.1289 |
| | setup↓ → CKN | 0.1836 | 0.3398 | 0.3477 | 0.3047 |
| | hold↑ → CKN | 0.0469 | 0.0039 | 0.0078 | -0.0078 |
| | hold↓ → CKN | -0.1641 | -0.2969 | -0.3008 | -0.2617 |
| CKN | minpwl | 0.1953 | 0.1904 | 0.1710 | 0.1564 |
| | minpwh | 0.1467 | 0.1564 | 0.1710 | 0.1710 |
| SN | minpwl | 0.1321 | 0.1176 | 0.1224 | 0.1516 |
| | recovery | -0.0859 | -0.0469 | -0.0469 | -0.0391 |

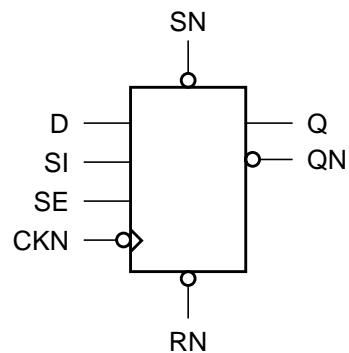
Cell Description

The SDFFNSR cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Functions

| RN | SN | D | SI | SE | CKN | Q[n+1] | QN[n+1] |
|----|----|---|----|----|-----|--------|---------|
| 1 | 1 | 1 | x | 0 | — | 1 | 0 |
| 1 | 1 | 0 | x | 0 | — | 0 | 1 |
| 1 | 1 | x | x | x | — | Q[n] | QN[n] |
| 1 | 1 | x | 1 | 1 | — | 1 | 0 |
| 1 | 1 | x | 0 | 1 | — | 0 | 1 |
| 0 | 1 | x | x | x | x | 0 | 1 |
| 1 | 0 | x | x | x | x | 1 | 0 |
| 0 | 0 | x | x | x | x | 1 | 0 |

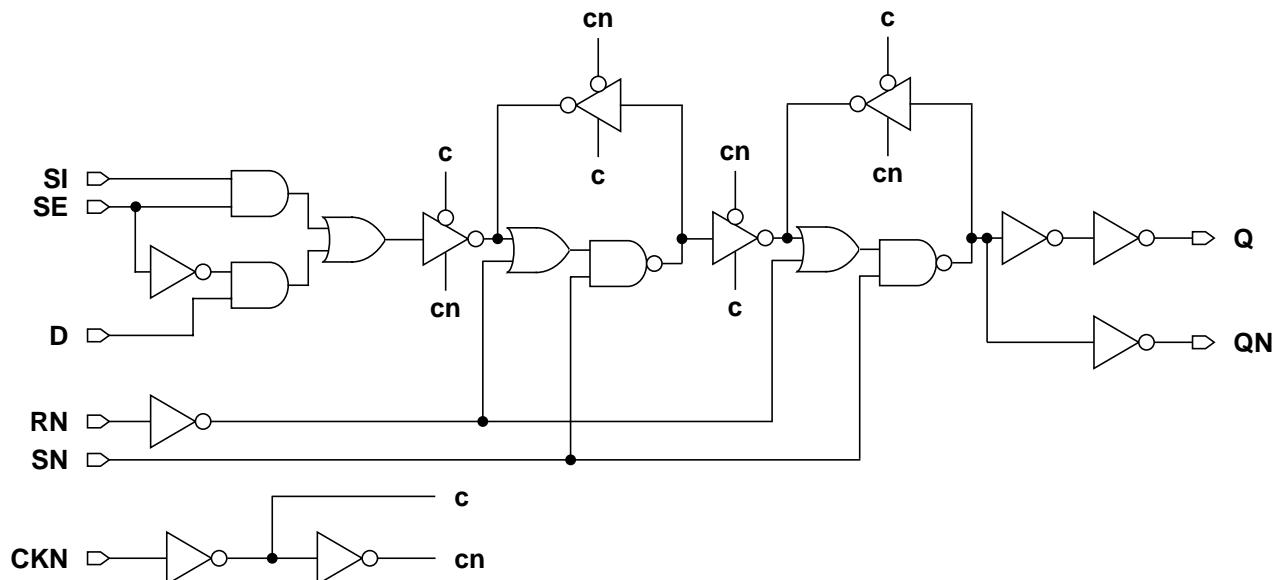
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFNSRXL | 5.04 | 19.14 |
| SDFFNSRX1 | 5.04 | 19.14 |
| SDFFNSRX2 | 5.04 | 19.14 |
| SDFFNSRX4 | 5.04 | 25.08 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0451 | 0.0399 | 0.0448 | 0.0595 |
| SE | 0.0519 | 0.0459 | 0.0511 | 0.0662 |
| D | 0.0390 | 0.0342 | 0.0390 | 0.0522 |
| CKN | 0.0390 | 0.0382 | 0.0424 | 0.0596 |
| SN | 0.0087 | 0.0090 | 0.0123 | 0.0186 |
| RN | 0.0184 | 0.0203 | 0.0249 | 0.0423 |
| Q | 0.0510 | 0.0584 | 0.0896 | 0.1637 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0021 | 0.0020 | 0.0020 | 0.0021 |
| SE | 0.0048 | 0.0045 | 0.0047 | 0.0051 |
| D | 0.0023 | 0.0018 | 0.0019 | 0.0025 |
| CKN | 0.0025 | 0.0030 | 0.0030 | 0.0042 |
| SN | 0.0067 | 0.0071 | 0.0093 | 0.0155 |
| RN | 0.0027 | 0.0030 | 0.0040 | 0.0063 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CKN → Q↑ | 0.3875 | 0.3448 | 0.3351 | 0.3071 | 5.8858 | 4.2012 | 2.0801 | 1.0641 |
| CKN → Q↓ | 0.4638 | 0.4487 | 0.4162 | 0.3887 | 3.4810 | 2.5352 | 1.2932 | 0.6464 |
| SN → Q↑ | 0.1958 | 0.1822 | 0.1738 | 0.1668 | 5.8843 | 4.2008 | 2.0801 | 1.0641 |
| SN → Q↓ | 0.2076 | 0.1934 | 0.1770 | 0.1707 | 3.4822 | 2.5355 | 1.2933 | 0.6464 |
| RN → Q↓ | 0.3001 | 0.2784 | 0.2449 | 0.2379 | 3.4824 | 2.5355 | 1.2933 | 0.6464 |
| CKN → QN↑ | 0.4002 | 0.3747 | 0.3439 | 0.3210 | 5.9261 | 4.2118 | 2.0850 | 1.0672 |
| CKN → QN↓ | 0.3471 | 0.3006 | 0.2791 | 0.2558 | 3.7786 | 2.6079 | 1.3256 | 0.6613 |
| SN → QN↑ | 0.1445 | 0.1205 | 0.1053 | 0.1033 | 5.9556 | 4.2245 | 2.0913 | 1.0713 |
| SN → QN↓ | 0.1530 | 0.1353 | 0.1182 | 0.1158 | 3.5791 | 2.5605 | 1.3050 | 0.6561 |
| RN → QN↑ | 0.2369 | 0.2052 | 0.1730 | 0.1703 | 5.9538 | 4.2239 | 2.0912 | 1.0712 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|--------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CKN | 0.1562 | 0.1914 | 0.1836 | 0.1953 |
| | setup↓ → CKN | 0.3164 | 0.3672 | 0.3711 | 0.3750 |
| | hold↑ → CKN | 0.0078 | -0.0273 | -0.0195 | -0.0352 |
| | hold↓ → CKN | -0.2734 | -0.3086 | -0.3164 | -0.3125 |
| SE | setup↑ → CKN | 0.3398 | 0.3906 | 0.3906 | 0.3984 |
| | setup↓ → CKN | 0.2422 | 0.3594 | 0.3398 | 0.2617 |
| | hold↑ → CKN | 0.0195 | -0.0117 | -0.0039 | -0.0234 |
| | hold↓ → CKN | -0.0312 | -0.0781 | -0.0742 | -0.0625 |
| D | setup↑ → CKN | 0.1133 | 0.1758 | 0.1641 | 0.1523 |
| | setup↓ → CKN | 0.2422 | 0.3633 | 0.3398 | 0.2617 |
| | hold↑ → CKN | 0.0312 | -0.0156 | -0.0117 | -0.0039 |
| | hold↓ → CKN | -0.2031 | -0.3008 | -0.2812 | -0.2109 |
| CKN | minpwl | 0.2001 | 0.1953 | 0.1710 | 0.1564 |
| | minpwh | 0.1613 | 0.1904 | 0.1953 | 0.1661 |
| SN | minpwl | 0.1516 | 0.1370 | 0.1370 | 0.1759 |
| | recovery | -0.0664 | -0.0352 | -0.0312 | -0.0312 |
| | removal | 0.0742 | 0.0391 | 0.0391 | 0.0391 |
| RN | minpwl | 0.2147 | 0.1904 | 0.1953 | 0.3216 |
| | recovery | 0.0625 | 0.1211 | 0.0977 | 0.0898 |
| | removal | 0.0742 | 0.0195 | 0.0430 | 0.0508 |

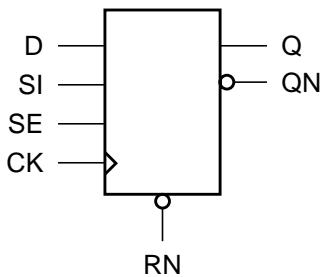
Cell Description

The SDFFR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Functions

| RN | D | SI | SE | CK | Q[n+1] | QN[n+1] |
|----|---|----|----|----|--------|---------|
| 1 | 1 | x | 0 | / | 1 | 0 |
| 1 | 0 | x | 0 | / | 0 | 1 |
| 1 | x | x | x | / | Q[n] | QN[n] |
| 1 | x | 1 | 1 | / | 1 | 0 |
| 1 | x | 0 | 1 | / | 0 | 1 |
| 0 | x | x | x | x | 0 | 1 |

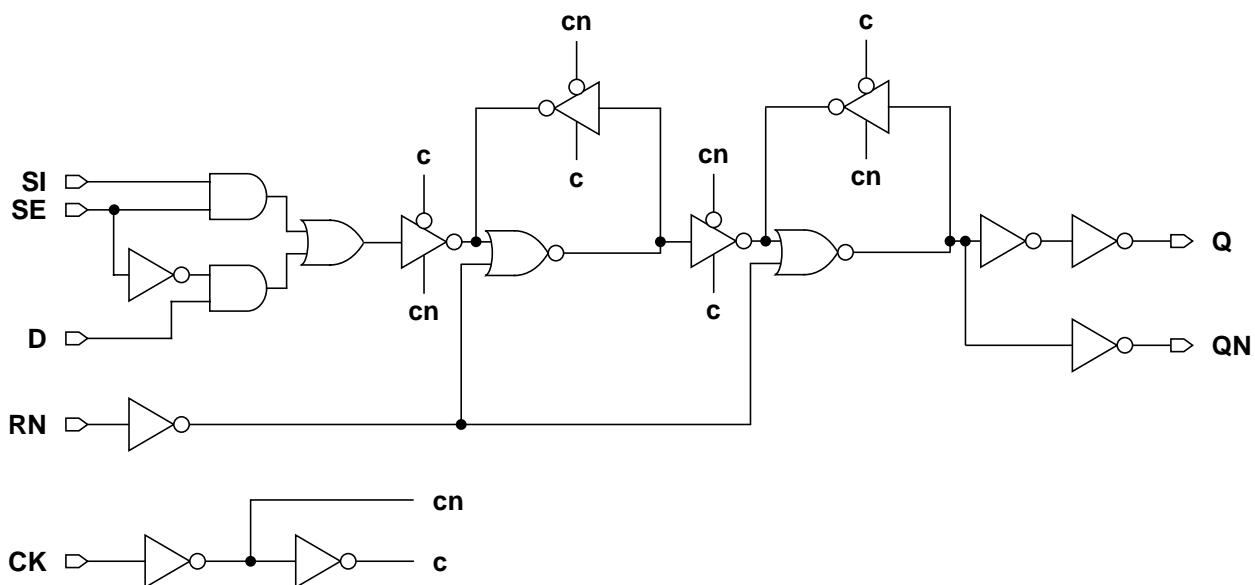
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFRXL | 5.04 | 18.48 |
| SDFFRX1 | 5.04 | 18.48 |
| SDFFRX2 | 5.04 | 19.80 |
| SDFFRX4 | 5.04 | 23.10 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0441 | 0.0402 | 0.0431 | 0.0542 |
| SE | 0.0513 | 0.0456 | 0.0502 | 0.0606 |
| D | 0.0378 | 0.0343 | 0.0375 | 0.0475 |
| CK | 0.0431 | 0.0407 | 0.0458 | 0.0499 |
| RN | 0.0163 | 0.0182 | 0.0221 | 0.0335 |
| Q | 0.0496 | 0.0570 | 0.0875 | 0.1548 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0024 | 0.0025 | 0.0025 | 0.0025 |
| SE | 0.0053 | 0.0047 | 0.0050 | 0.0053 |
| D | 0.0031 | 0.0024 | 0.0022 | 0.0029 |
| CK | 0.0026 | 0.0030 | 0.0033 | 0.0039 |
| RN | 0.0024 | 0.0029 | 0.0034 | 0.0059 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.4391 | 0.4007 | 0.3941 | 0.3541 | 5.8853 | 4.2019 | 2.0799 | 1.0643 |
| CK → Q↓ | 0.3084 | 0.3236 | 0.3064 | 0.2796 | 3.4683 | 2.5312 | 1.4336 | 0.6517 |
| RN → Q↓ | 0.2497 | 0.2507 | 0.2388 | 0.2210 | 3.4687 | 2.5314 | 1.4337 | 0.6517 |
| CK → QN↑ | 0.2563 | 0.2589 | 0.2313 | 0.2120 | 5.8848 | 4.2024 | 2.0810 | 1.0649 |
| CK → QN↓ | 0.4081 | 0.3627 | 0.3459 | 0.2991 | 3.6988 | 2.5946 | 1.5669 | 0.6627 |
| RN → QN↑ | 0.1979 | 0.1867 | 0.1641 | 0.1538 | 5.8970 | 4.2065 | 2.0832 | 1.0662 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1602 | 0.1484 | 0.1758 | 0.1719 |
| | setup↓ → CK | 0.3242 | 0.3516 | 0.3867 | 0.3867 |
| | hold↑ → CK | -0.1289 | -0.1250 | -0.1367 | -0.1367 |
| | hold↓ → CK | -0.1992 | -0.2383 | -0.2578 | -0.2695 |
| SE | setup↑ → CK | 0.3438 | 0.3750 | 0.4023 | 0.4062 |
| | setup↓ → CK | 0.1992 | 0.3359 | 0.3750 | 0.2930 |
| | hold↑ → CK | -0.1211 | -0.1016 | -0.1172 | -0.1211 |
| | hold↓ → CK | -0.0781 | -0.1680 | -0.1797 | -0.1719 |
| D | setup↑ → CK | 0.1016 | 0.1289 | 0.1484 | 0.1445 |
| | setup↓ → CK | 0.1992 | 0.3477 | 0.3789 | 0.3008 |
| | hold↑ → CK | -0.0859 | -0.1055 | -0.1172 | -0.1133 |
| | hold↓ → CK | -0.0781 | -0.2383 | -0.2500 | -0.1836 |
| CK | minpwh | 0.1370 | 0.1467 | 0.1321 | 0.1127 |
| | minpwl | 0.2487 | 0.2196 | 0.2439 | 0.2099 |
| RN | minpwl | 0.1856 | 0.1856 | 0.2050 | 0.3022 |
| | recovery | 0.0352 | 0.0508 | 0.0703 | 0.0547 |
| | removal | -0.0156 | -0.0312 | -0.0391 | -0.0195 |

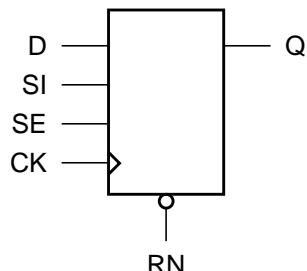
Cell Description

The SDFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Functions

| RN | D | SI | SE | CK | Q[n+1] |
|----|---|----|----|----|--------|
| 1 | 1 | x | 0 | / | 1 |
| 1 | 0 | x | 0 | / | 0 |
| 1 | x | x | x | \ | Q[n] |
| 1 | x | 1 | 1 | / | 1 |
| 1 | x | 0 | 1 | / | 0 |
| 0 | x | x | x | x | 0 |

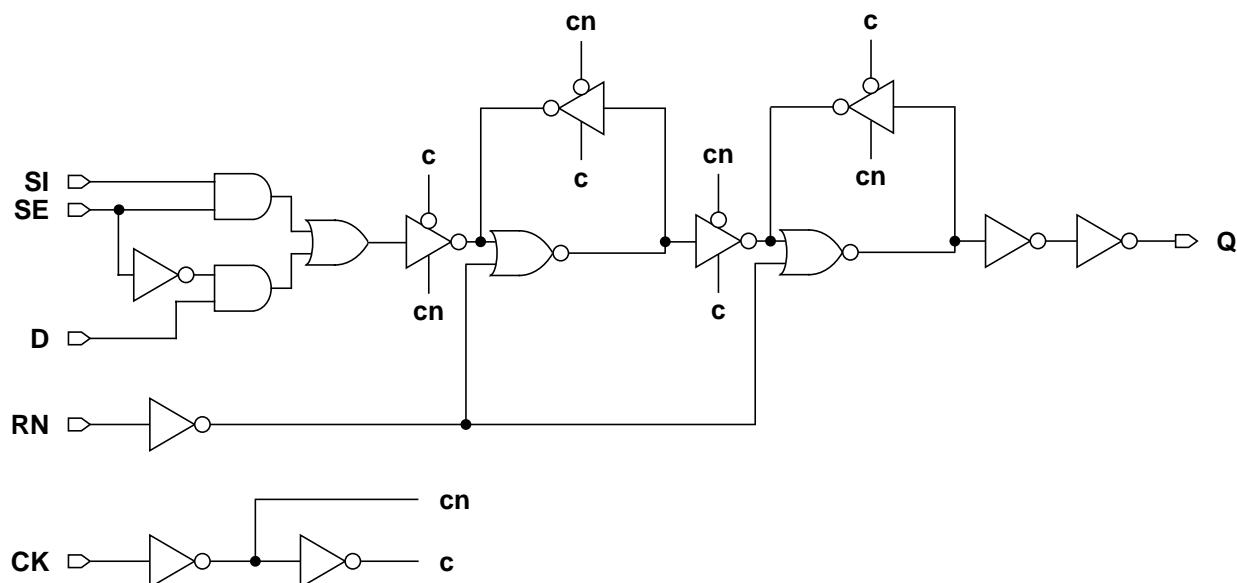
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFRHQXL | 5.04 | 16.50 |
| SDFFRHQX1 | 5.04 | 16.50 |
| SDFFRHQX2 | 5.04 | 19.80 |
| SDFFRHQX4 | 5.04 | 24.42 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0455 | 0.0549 | 0.0777 | 0.1199 |
| SE | 0.0542 | 0.0636 | 0.0854 | 0.1259 |
| D | 0.0384 | 0.0479 | 0.0706 | 0.1052 |
| CK | 0.0451 | 0.0452 | 0.0544 | 0.0731 |
| RN | 0.0210 | 0.0260 | 0.0354 | 0.0564 |
| Q | 0.0356 | 0.0387 | 0.0526 | 0.0807 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0024 | 0.0024 | 0.0024 | 0.0024 |
| SE | 0.0054 | 0.0049 | 0.0051 | 0.0059 |
| D | 0.0029 | 0.0021 | 0.0025 | 0.0038 |
| CK | 0.0024 | 0.0031 | 0.0042 | 0.0065 |
| RN | 0.0027 | 0.0042 | 0.0057 | 0.0100 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2487 | 0.2044 | 0.1806 | 0.1674 | 8.7407 | 6.0770 | 3.0376 | 1.6812 |
| CK → Q↓ | 0.2608 | 0.1788 | 0.1553 | 0.1445 | 3.7971 | 2.5683 | 1.3047 | 0.7203 |
| RN → Q↓ | 0.1833 | 0.1414 | 0.1238 | 0.1067 | 3.0071 | 2.0056 | 1.1292 | 0.6783 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1719 | 0.1914 | 0.2227 | 0.2461 |
| | setup↓ → CK | 0.3906 | 0.4336 | 0.4727 | 0.5234 |
| | hold↑ → CK | -0.1172 | -0.1211 | -0.1445 | -0.1680 |
| | hold↓ → CK | -0.1875 | -0.2422 | -0.2695 | -0.3203 |
| SE | setup↑ → CK | 0.4102 | 0.4492 | 0.4805 | 0.5547 |
| | setup↓ → CK | 0.2617 | 0.4062 | 0.3750 | 0.3125 |
| | hold↑ → CK | -0.1094 | -0.1055 | -0.1328 | -0.1562 |
| | hold↓ → CK | -0.0742 | -0.1602 | -0.1758 | -0.1328 |
| D | setup↑ → CK | 0.1250 | 0.1719 | 0.1875 | 0.1641 |
| | setup↓ → CK | 0.2539 | 0.4062 | 0.3711 | 0.3125 |
| | hold↑ → CK | -0.0742 | -0.1055 | -0.1172 | -0.0859 |
| | hold↓ → CK | -0.0742 | -0.2188 | -0.1797 | -0.1367 |
| CK | minpwh | 0.1661 | 0.1176 | 0.1030 | 0.0933 |
| | minpwl | 0.2196 | 0.2099 | 0.2001 | 0.1661 |
| RN | minpwl | 0.2536 | 0.2487 | 0.3362 | 0.5159 |
| | recovery | 0.1016 | 0.1094 | 0.1133 | 0.1094 |
| | removal | -0.0312 | -0.0391 | -0.0352 | -0.0195 |

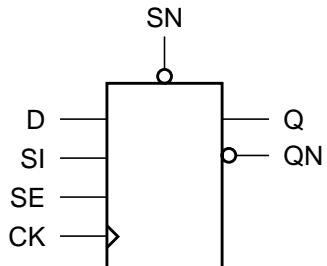
Cell Description

The SDFFS cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Functions

| SN | D | SI | SE | CK | Q[n+1] | QN[n+1] |
|-----------|----------|-----------|-----------|-----------|---------------|----------------|
| 1 | 1 | x | 0 | —/— | 1 | 0 |
| 1 | 0 | x | 0 | —/— | 0 | 1 |
| 1 | x | x | x | —\— | Q[n] | QN[n] |
| 1 | x | 1 | 1 | —/— | 1 | 0 |
| 1 | x | 0 | 1 | —/— | 0 | 1 |
| 0 | x | x | x | x | 1 | 0 |

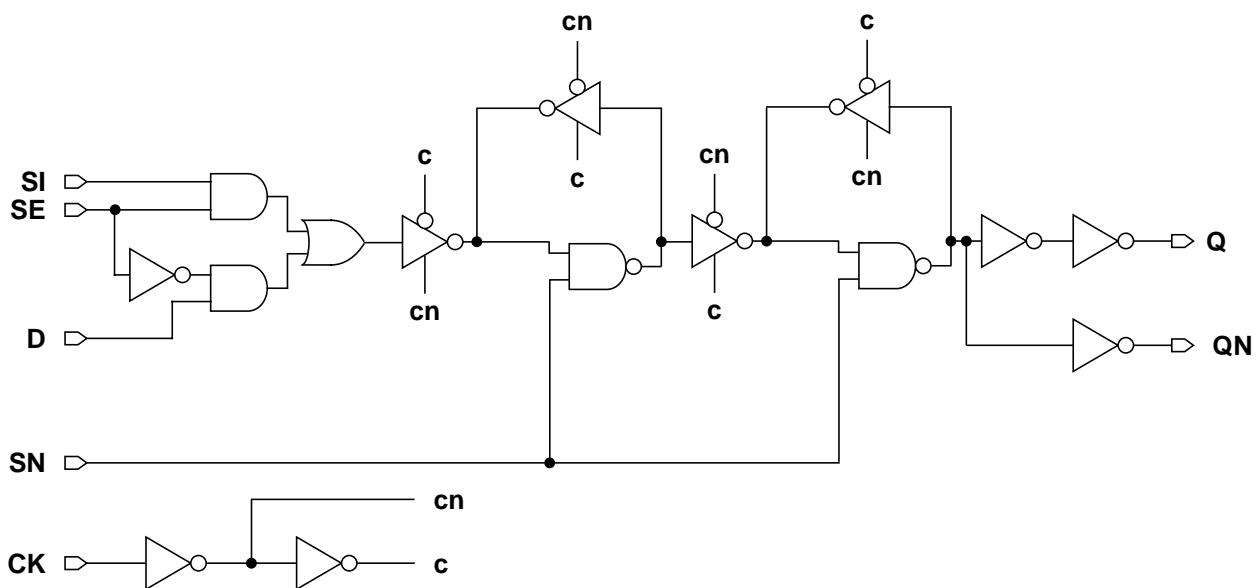
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFSXL | 5.04 | 15.84 |
| SDFFSX1 | 5.04 | 15.84 |
| SDFFSX2 | 5.04 | 16.50 |
| SDFFSX4 | 5.04 | 21.12 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0422 | 0.0361 | 0.0399 | 0.0473 |
| SE | 0.0488 | 0.0418 | 0.0456 | 0.0529 |
| D | 0.0355 | 0.0301 | 0.0341 | 0.0408 |
| CK | 0.0422 | 0.0395 | 0.0443 | 0.0486 |
| SN | 0.0070 | 0.0078 | 0.0119 | 0.0183 |
| Q | 0.0432 | 0.0499 | 0.0812 | 0.1437 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0023 | 0.0023 | 0.0023 | 0.0024 |
| SE | 0.0056 | 0.0049 | 0.0049 | 0.0050 |
| D | 0.0029 | 0.0020 | 0.0021 | 0.0022 |
| CK | 0.0026 | 0.0032 | 0.0032 | 0.0038 |
| SN | 0.0055 | 0.0059 | 0.0080 | 0.0130 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.3620 | 0.3390 | 0.3538 | 0.3275 | 5.8882 | 4.2020 | 2.1276 | 1.0399 |
| CK → Q↓ | 0.2983 | 0.3048 | 0.3072 | 0.2790 | 3.4693 | 2.5309 | 1.2925 | 0.6460 |
| SN → Q↑ | 0.1686 | 0.1536 | 0.1602 | 0.1509 | 5.8881 | 4.2020 | 2.1276 | 1.0399 |
| CK → QN↑ | 0.2512 | 0.2441 | 0.2358 | 0.2123 | 5.9043 | 4.4013 | 2.1324 | 1.0424 |
| CK → QN↓ | 0.3313 | 0.3015 | 0.3013 | 0.2771 | 3.5413 | 2.7910 | 1.2982 | 0.6486 |
| SN → QN↓ | 0.1378 | 0.1161 | 0.1079 | 0.1007 | 3.5267 | 2.7913 | 1.3006 | 0.6510 |

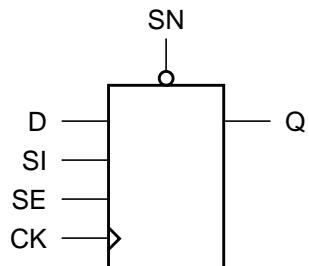
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1406 | 0.1289 | 0.1289 | 0.1445 |
| | setup↓ → CK | 0.3242 | 0.3477 | 0.3594 | 0.3672 |
| | hold↑ → CK | -0.1172 | -0.1094 | -0.1016 | -0.1172 |
| | hold↓ → CK | -0.2266 | -0.2578 | -0.2578 | -0.2656 |
| SE | setup↑ → CK | 0.3516 | 0.3750 | 0.3867 | 0.3867 |
| | setup↓ → CK | 0.1992 | 0.3398 | 0.3516 | 0.3125 |
| | hold↑ → CK | -0.1016 | -0.0859 | -0.0859 | -0.0977 |
| | hold↓ → CK | -0.0977 | -0.1484 | -0.1484 | -0.1562 |
| D | setup↑ → CK | 0.0898 | 0.1094 | 0.1094 | 0.1211 |
| | setup↓ → CK | 0.2031 | 0.3477 | 0.3633 | 0.3164 |
| | hold↑ → CK | -0.0742 | -0.0859 | -0.0859 | -0.0977 |
| | hold↓ → CK | -0.1016 | -0.2617 | -0.2656 | -0.2188 |
| CK | minpwh | 0.1224 | 0.1321 | 0.1224 | 0.1127 |
| | minpwl | 0.2196 | 0.2001 | 0.2147 | 0.2001 |
| SN | minpwl | 0.1321 | 0.1176 | 0.1273 | 0.1467 |
| | recovery | -0.0234 | -0.0039 | -0.0078 | 0.0078 |
| | removal | 0.1328 | 0.0938 | 0.1016 | 0.0859 |

Cell Description

The SDFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



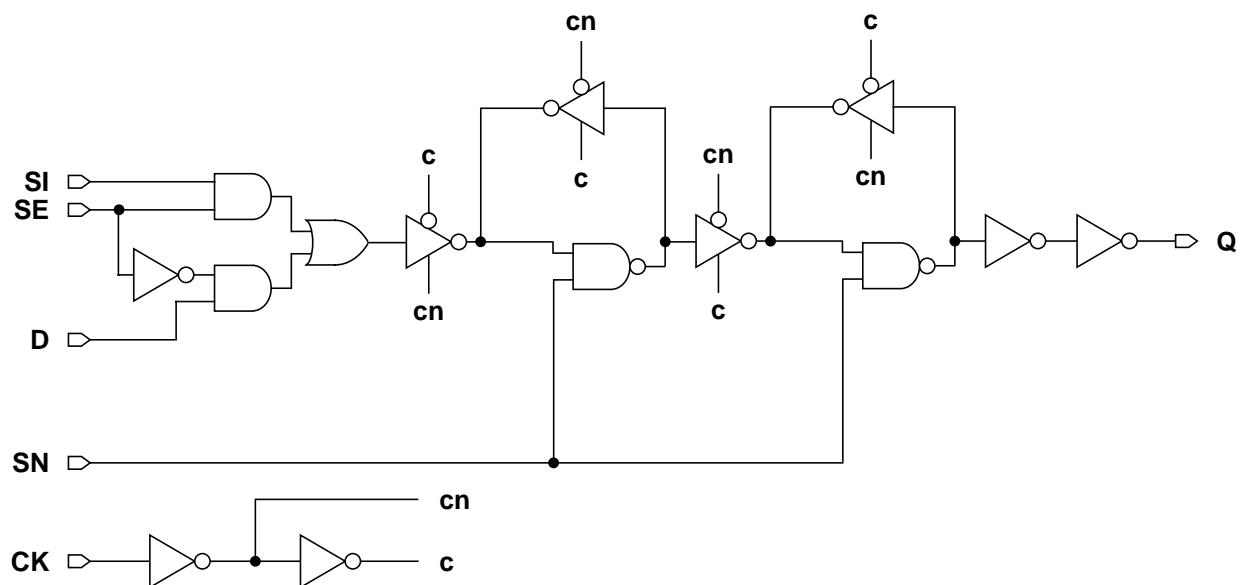
Functions

| SN | D | SI | SE | CK | Q[n+1] |
|----|---|----|----|----|--------|
| 1 | 1 | x | 0 | /\ | 1 |
| 1 | 0 | x | 0 | /\ | 0 |
| 1 | x | x | x | _ | Q[n] |
| 1 | x | 1 | 1 | /\ | 1 |
| 1 | x | 0 | 1 | /\ | 0 |
| 0 | x | x | x | x | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFSHQXL | 5.04 | 15.84 |
| SDFFSHQX1 | 5.04 | 15.84 |
| SDFFSHQX2 | 5.04 | 18.48 |
| SDFFSHQX4 | 5.04 | 21.12 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0467 | 0.0536 | 0.0723 | 0.1115 |
| SE | 0.0546 | 0.0600 | 0.0780 | 0.1143 |
| D | 0.0403 | 0.0471 | 0.0636 | 0.0973 |
| CK | 0.0436 | 0.0438 | 0.0512 | 0.0701 |
| SN | 0.0107 | 0.0117 | 0.0198 | 0.0319 |
| Q | 0.0350 | 0.0346 | 0.0537 | 0.0876 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0024 | 0.0026 | 0.0024 | 0.0025 |
| SE | 0.0055 | 0.0050 | 0.0051 | 0.0056 |
| D | 0.0030 | 0.0021 | 0.0023 | 0.0033 |
| CK | 0.0024 | 0.0031 | 0.0039 | 0.0059 |
| SN | 0.0088 | 0.0095 | 0.0147 | 0.0228 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2507 | 0.2056 | 0.1859 | 0.1653 | 5.9319 | 4.2091 | 2.1307 | 1.0651 |
| CK → Q↓ | 0.2801 | 0.1774 | 0.1561 | 0.1430 | 4.4912 | 2.9832 | 1.4865 | 0.7488 |
| SN → Q↑ | 0.0738 | 0.0840 | 0.0870 | 0.0902 | 3.3415 | 2.3042 | 1.2161 | 0.6579 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1562 | 0.1641 | 0.1836 | 0.2188 |
| | setup↓ → CK | 0.3555 | 0.4531 | 0.4648 | 0.5156 |
| | hold↑ → CK | -0.1172 | -0.1133 | -0.1289 | -0.1484 |
| | hold↓ → CK | -0.2227 | -0.2656 | -0.2734 | -0.3242 |
| SE | setup↑ → CK | 0.3711 | 0.4648 | 0.4727 | 0.5273 |
| | setup↓ → CK | 0.2266 | 0.4531 | 0.3867 | 0.3398 |
| | hold↑ → CK | -0.1094 | -0.0977 | -0.1094 | -0.1406 |
| | hold↓ → CK | -0.0977 | -0.1523 | -0.1602 | -0.1484 |
| D | setup↑ → CK | 0.1055 | 0.1445 | 0.1602 | 0.1484 |
| | setup↓ → CK | 0.2188 | 0.4570 | 0.3906 | 0.3359 |
| | hold↑ → CK | -0.0781 | -0.0938 | -0.1016 | -0.0859 |
| | hold↓ → CK | -0.1016 | -0.2734 | -0.2070 | -0.1641 |
| CK | minpwh | 0.1904 | 0.1176 | 0.1078 | 0.0933 |
| | minpwl | 0.2099 | 0.2001 | 0.1953 | 0.1710 |
| SN | minpwl | 0.1127 | 0.1273 | 0.1613 | 0.2390 |
| | recovery | -0.0039 | 0.0625 | 0.0664 | 0.0664 |
| | removal | 0.1328 | 0.0938 | 0.0977 | 0.0977 |

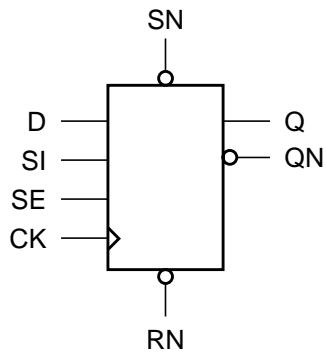
Cell Description

The SDFFSR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Functions

| RN | SN | D | SI | SE | CK | Q[n+1] | QN[n+1] |
|----|----|---|----|----|----|--------|---------|
| 1 | 1 | 1 | x | 0 | /\ | 1 | 0 |
| 1 | 1 | 0 | x | 0 | /\ | 0 | 1 |
| 1 | 1 | x | x | x | _ | Q[n] | QN[n] |
| 1 | 1 | x | 1 | 1 | /\ | 1 | 0 |
| 1 | 1 | x | 0 | 1 | /\ | 0 | 1 |
| 0 | 1 | x | x | x | x | 0 | 1 |
| 1 | 0 | x | x | x | x | 1 | 0 |
| 0 | 0 | x | x | x | x | 1 | 0 |

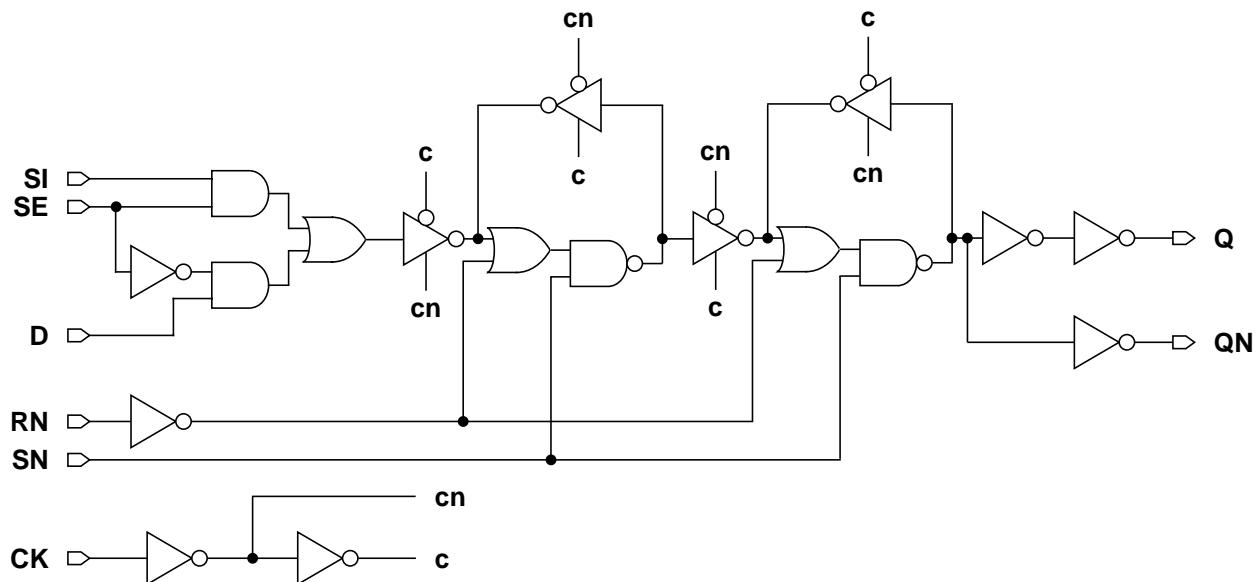
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| SDFFSRXL | 5.04 | 19.14 |
| SDFFSRX1 | 5.04 | 19.80 |
| SDFFSRX2 | 5.04 | 19.14 |
| SDFFSRX4 | 5.04 | 25.74 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0449 | 0.0391 | 0.0444 | 0.0588 |
| SE | 0.0521 | 0.0450 | 0.0503 | 0.0654 |
| D | 0.0384 | 0.0332 | 0.0383 | 0.0516 |
| CK | 0.0413 | 0.0394 | 0.0401 | 0.0515 |
| SN | 0.0094 | 0.0098 | 0.0131 | 0.0198 |
| RN | 0.0178 | 0.0191 | 0.0242 | 0.0421 |
| Q | 0.0515 | 0.0591 | 0.0905 | 0.1654 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0023 | 0.0022 | 0.0022 | 0.0023 |
| SE | 0.0051 | 0.0048 | 0.0049 | 0.0053 |
| D | 0.0026 | 0.0020 | 0.0021 | 0.0028 |
| CK | 0.0027 | 0.0032 | 0.0032 | 0.0042 |
| SN | 0.0067 | 0.0071 | 0.0093 | 0.0157 |
| RN | 0.0026 | 0.0029 | 0.0039 | 0.0063 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.4330 | 0.3946 | 0.3911 | 0.3625 | 5.8845 | 4.2004 | 2.1531 | 1.0641 |
| CK → Q↓ | 0.3335 | 0.3385 | 0.3045 | 0.2906 | 3.4811 | 2.5344 | 1.3259 | 0.6464 |
| SN → Q↑ | 0.1944 | 0.1819 | 0.1755 | 0.1668 | 5.8831 | 4.1999 | 2.1530 | 1.0641 |
| SN → Q↓ | 0.2062 | 0.1930 | 0.1786 | 0.1709 | 3.4822 | 2.5347 | 1.3259 | 0.6464 |
| RN → Q↓ | 0.2985 | 0.2765 | 0.2457 | 0.2380 | 3.4824 | 2.5349 | 1.3260 | 0.6464 |
| CK → QN↑ | 0.2701 | 0.2656 | 0.2313 | 0.2225 | 5.9250 | 4.2114 | 2.1582 | 1.0672 |
| CK → QN↓ | 0.3928 | 0.3514 | 0.3342 | 0.3108 | 3.7759 | 2.6076 | 1.3587 | 0.6613 |
| SN → QN↑ | 0.1433 | 0.1211 | 0.1060 | 0.1031 | 5.9544 | 4.2239 | 2.1646 | 1.0714 |
| SN → QN↓ | 0.1519 | 0.1359 | 0.1188 | 0.1154 | 3.5785 | 2.5600 | 1.3381 | 0.6561 |
| RN → QN↑ | 0.2354 | 0.2044 | 0.1730 | 0.1700 | 5.9526 | 4.2234 | 2.1644 | 1.0712 |

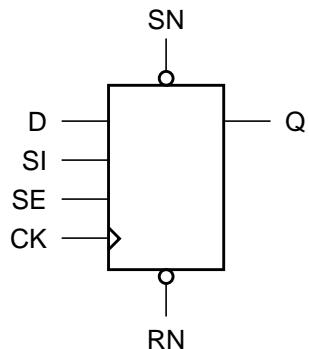
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1719 | 0.1914 | 0.1797 | 0.1875 |
| | setup↓ → CK | 0.3242 | 0.3633 | 0.3750 | 0.3828 |
| | hold↑ → CK | -0.1406 | -0.1406 | -0.1406 | -0.1484 |
| | hold↓ → CK | -0.1953 | -0.2305 | -0.2344 | -0.2539 |
| SE | setup↑ → CK | 0.3516 | 0.3828 | 0.3906 | 0.4062 |
| | setup↓ → CK | 0.2539 | 0.3555 | 0.3438 | 0.2812 |
| | hold↑ → CK | -0.1211 | -0.1211 | -0.1172 | -0.1328 |
| | hold↓ → CK | -0.1250 | -0.1875 | -0.1836 | -0.1484 |
| D | setup↑ → CK | 0.1211 | 0.1680 | 0.1562 | 0.1367 |
| | setup↓ → CK | 0.2617 | 0.3594 | 0.3477 | 0.2812 |
| | hold↑ → CK | -0.0938 | -0.1250 | -0.1172 | -0.0977 |
| | hold↓ → CK | -0.1289 | -0.2266 | -0.2070 | -0.1523 |
| CK | minpwh | 0.1224 | 0.1418 | 0.1176 | 0.1127 |
| | minpwl | 0.2147 | 0.2293 | 0.2244 | 0.1904 |
| SN | minpwl | 0.1516 | 0.1370 | 0.1370 | 0.1759 |
| | recovery | -0.0039 | 0.0078 | 0.0156 | 0.0156 |
| | removal | 0.1250 | 0.0898 | 0.0938 | 0.0938 |
| RN | minpwl | 0.2147 | 0.1904 | 0.1953 | 0.3216 |
| | recovery | 0.0625 | 0.1094 | 0.0820 | 0.0703 |
| | removal | -0.0391 | -0.0781 | -0.0547 | -0.0352 |

Cell Description

The SDFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



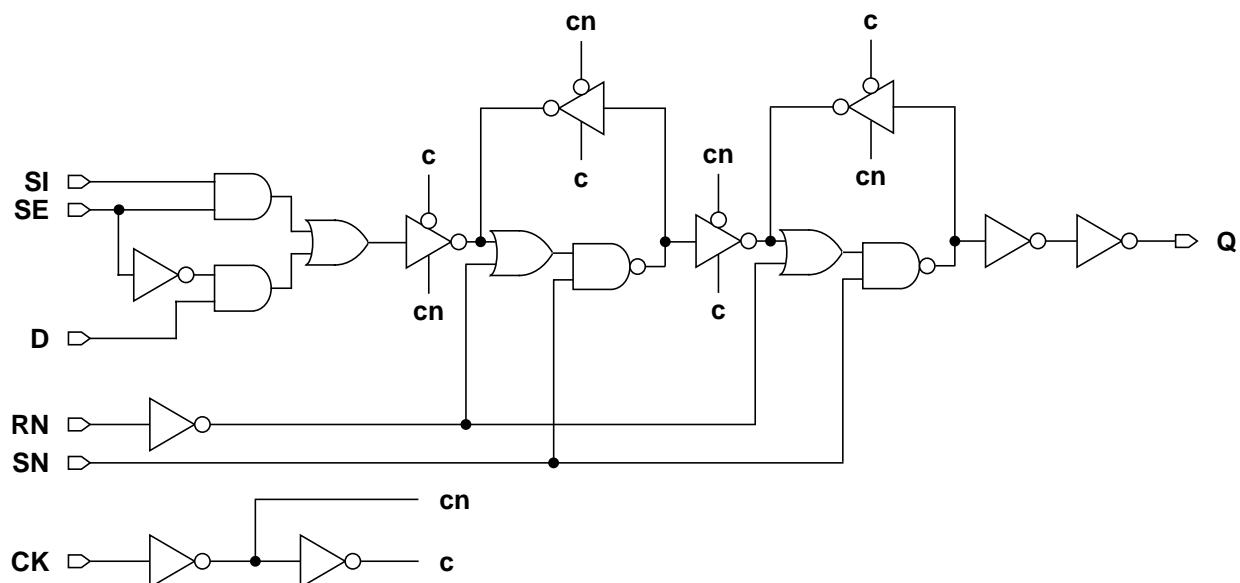
Functions

| RN | SN | D | SI | SE | CK | Q[n+1] |
|----|----|---|----|----|----|--------|
| 1 | 1 | 1 | x | 0 | / | 1 |
| 1 | 1 | 0 | x | 0 | / | 0 |
| 1 | 1 | x | x | x | / | Q[n] |
| 1 | 1 | x | 1 | 1 | / | 1 |
| 1 | 1 | x | 0 | 1 | / | 0 |
| 0 | 1 | x | x | x | x | 0 |
| 1 | 0 | x | x | x | x | 1 |
| 0 | 0 | x | x | x | x | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFSRHQXL | 5.04 | 19.80 |
| SDFFSRHQX1 | 5.04 | 19.80 |
| SDFFSRHQX2 | 5.04 | 25.08 |
| SDFFSRHQX4 | 5.04 | 33.66 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0499 | 0.0573 | 0.0804 | 0.1278 |
| SE | 0.0576 | 0.0650 | 0.0921 | 0.1369 |
| D | 0.0431 | 0.0509 | 0.0723 | 0.1129 |
| CK | 0.0444 | 0.0439 | 0.0558 | 0.0799 |
| SN | 0.0132 | 0.0143 | 0.0203 | 0.0338 |
| RN | 0.0249 | 0.0293 | 0.0446 | 0.0726 |
| Q | 0.0370 | 0.0399 | 0.0609 | 0.0954 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0023 | 0.0023 | 0.0024 | 0.0024 |
| SE | 0.0062 | 0.0056 | 0.0059 | 0.0065 |
| D | 0.0030 | 0.0021 | 0.0028 | 0.0045 |
| CK | 0.0026 | 0.0031 | 0.0047 | 0.0068 |
| SN | 0.0116 | 0.0124 | 0.0177 | 0.0291 |
| RN | 0.0027 | 0.0040 | 0.0062 | 0.0107 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2640 | 0.2147 | 0.1994 | 0.1828 | 8.7395 | 6.0795 | 3.0393 | 1.5196 |
| CK → Q↓ | 0.2543 | 0.1749 | 0.1660 | 0.1515 | 4.3811 | 2.9712 | 1.5381 | 0.7760 |
| SN → Q↑ | 0.0789 | 0.0868 | 0.0906 | 0.0910 | 3.8145 | 2.6487 | 1.3673 | 0.7297 |
| SN → Q↓ | 0.0544 | 0.0597 | 0.0563 | 0.0466 | 3.8966 | 2.6498 | 1.4521 | 0.7702 |
| RN → Q↓ | 0.1874 | 0.1386 | 0.1236 | 0.1080 | 3.9224 | 2.6457 | 1.4498 | 0.7685 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1953 | 0.2070 | 0.2305 | 0.2891 |
| | setup↓ → CK | 0.4219 | 0.4375 | 0.4766 | 0.5781 |
| | hold↑ → CK | -0.1289 | -0.1328 | -0.1484 | -0.1875 |
| | hold↓ → CK | -0.2070 | -0.2461 | -0.2773 | -0.3750 |
| SE | setup↑ → CK | 0.4492 | 0.4648 | 0.5000 | 0.6133 |
| | setup↓ → CK | 0.2930 | 0.3867 | 0.3477 | 0.3125 |
| | hold↑ → CK | -0.1133 | -0.1133 | -0.1328 | -0.1719 |
| | hold↓ → CK | -0.0781 | -0.1758 | -0.1562 | -0.1328 |
| D | setup↑ → CK | 0.1445 | 0.1836 | 0.1875 | 0.1758 |
| | setup↓ → CK | 0.2930 | 0.3984 | 0.3516 | 0.3164 |
| | hold↑ → CK | -0.0781 | -0.1094 | -0.1094 | -0.0898 |
| | hold↓ → CK | -0.0820 | -0.2031 | -0.1562 | -0.1367 |
| CK | minpwh | 0.1613 | 0.1224 | 0.1078 | 0.0981 |
| | minpwl | 0.2293 | 0.2196 | 0.2001 | 0.1710 |
| SN | minpwl | 0.1273 | 0.1516 | 0.1856 | 0.2682 |
| | recovery | 0.0508 | 0.0664 | 0.0703 | 0.0742 |
| | removal | 0.1328 | 0.0938 | 0.0977 | 0.0977 |
| RN | minpwl | 0.2536 | 0.2001 | 0.2924 | 0.4771 |
| | recovery | 0.1172 | 0.1289 | 0.1250 | 0.1211 |
| | removal | -0.0352 | -0.0508 | -0.0352 | -0.0117 |

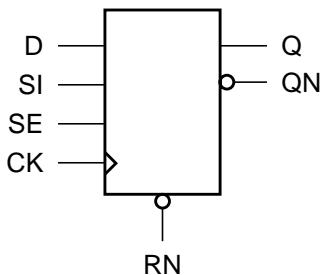
Cell Description

The SDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-low reset (RN). Scan enable (SE) dominates reset (RN).

Functions

| RN | D | SI | SE | CK | Q[n+1] | QN[n+1] |
|----|---|----|----|----|--------|---------|
| x | x | 0 | 1 | / | 0 | 1 |
| x | x | 1 | 1 | / | 1 | 0 |
| 0 | x | x | 0 | / | 0 | 1 |
| 1 | 0 | x | 0 | / | 0 | 1 |
| 1 | 1 | x | 0 | / | 1 | 0 |
| x | x | x | x | \ | Q[n] | QN[n] |

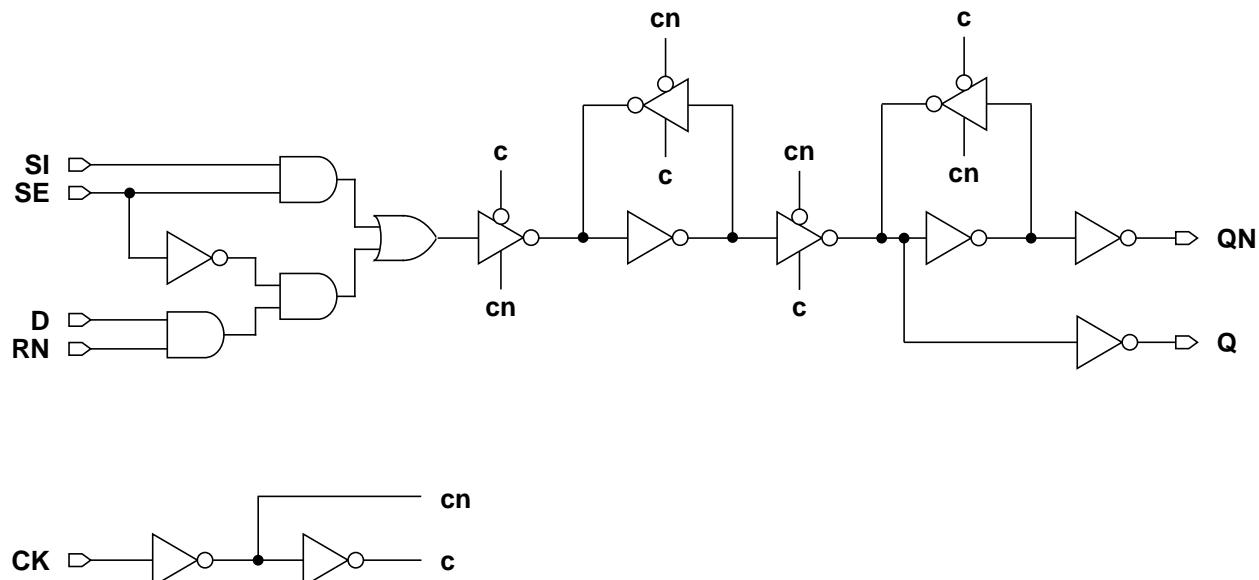
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SDFFTRXL | 5.04 | 14.52 |
| SDFFTRX1 | 5.04 | 14.52 |
| SDFFTRX2 | 5.04 | 17.16 |
| SDFFTRX4 | 5.04 | 19.80 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0429 | 0.0405 | 0.0512 | 0.0777 |
| SE | 0.0507 | 0.0474 | 0.0572 | 0.0810 |
| D | 0.0361 | 0.0350 | 0.0446 | 0.0651 |
| CK | 0.0435 | 0.0415 | 0.0513 | 0.0715 |
| RN | 0.0408 | 0.0386 | 0.0481 | 0.0722 |
| Q | 0.0339 | 0.0391 | 0.0739 | 0.1230 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0025 | 0.0025 | 0.0024 | 0.0026 |
| SE | 0.0056 | 0.0050 | 0.0050 | 0.0060 |
| D | 0.0025 | 0.0019 | 0.0021 | 0.0026 |
| CK | 0.0024 | 0.0031 | 0.0042 | 0.0068 |
| RN | 0.0029 | 0.0021 | 0.0023 | 0.0041 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2355 | 0.2069 | 0.2088 | 0.1748 | 5.8932 | 4.2042 | 2.1314 | 1.0420 |
| CK → Q↓ | 0.1856 | 0.1621 | 0.1537 | 0.1449 | 3.3437 | 2.7256 | 1.3097 | 0.6542 |
| CK → QN↑ | 0.2379 | 0.2141 | 0.2121 | 0.1980 | 5.8911 | 4.2032 | 2.1282 | 1.0402 |
| CK → QN↓ | 0.3072 | 0.2828 | 0.2861 | 0.2442 | 3.4999 | 2.5398 | 1.2944 | 0.6466 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1484 | 0.1406 | 0.1641 | 0.1914 |
| | setup↓ → CK | 0.3633 | 0.3867 | 0.3828 | 0.4727 |
| | hold↑ → CK | -0.1211 | -0.1094 | -0.1289 | -0.1523 |
| | hold↓ → CK | -0.2539 | -0.2734 | -0.2578 | -0.3555 |
| SE | setup↑ → CK | 0.3867 | 0.4062 | 0.3984 | 0.4766 |
| | setup↓ → CK | 0.2383 | 0.3867 | 0.3359 | 0.2773 |
| | hold↑ → CK | -0.1094 | -0.0938 | -0.1094 | -0.1445 |
| | hold↓ → CK | -0.1289 | -0.1875 | -0.2031 | -0.1680 |
| D | setup↑ → CK | 0.1172 | 0.1523 | 0.1758 | 0.1367 |
| | setup↓ → CK | 0.2383 | 0.3867 | 0.3359 | 0.2656 |
| | hold↑ → CK | -0.0977 | -0.1211 | -0.1406 | -0.1055 |
| | hold↓ → CK | -0.1211 | -0.2734 | -0.2109 | -0.1641 |
| CK | minpwh | 0.1224 | 0.1127 | 0.1176 | 0.0981 |
| | minpwl | 0.2293 | 0.2196 | 0.2293 | 0.1759 |
| RN | setup↑ → CK | 0.1250 | 0.1641 | 0.1875 | 0.1484 |
| | setup↓ → CK | 0.2773 | 0.4453 | 0.3750 | 0.3086 |
| | hold↑ → CK | -0.1094 | -0.1289 | -0.1484 | -0.1172 |
| | hold↓ → CK | -0.1484 | -0.3164 | -0.2383 | -0.1914 |

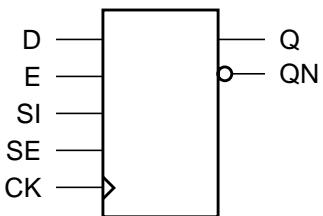
Cell Description

The SEDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E).

Functions

| D | E | SI | SE | CK | Q[n+1] | QN[n+1] |
|---|---|----|----|----|--------|---------|
| x | x | 1 | 1 | / | 1 | 0 |
| x | x | 0 | 1 | / | 0 | 1 |
| x | 0 | x | 0 | / | Q[n] | QN[n] |
| 0 | 1 | x | 0 | / | 0 | 1 |
| 1 | 1 | x | 0 | / | 1 | 0 |
| x | x | x | x | \ | Q[n] | QN[n] |

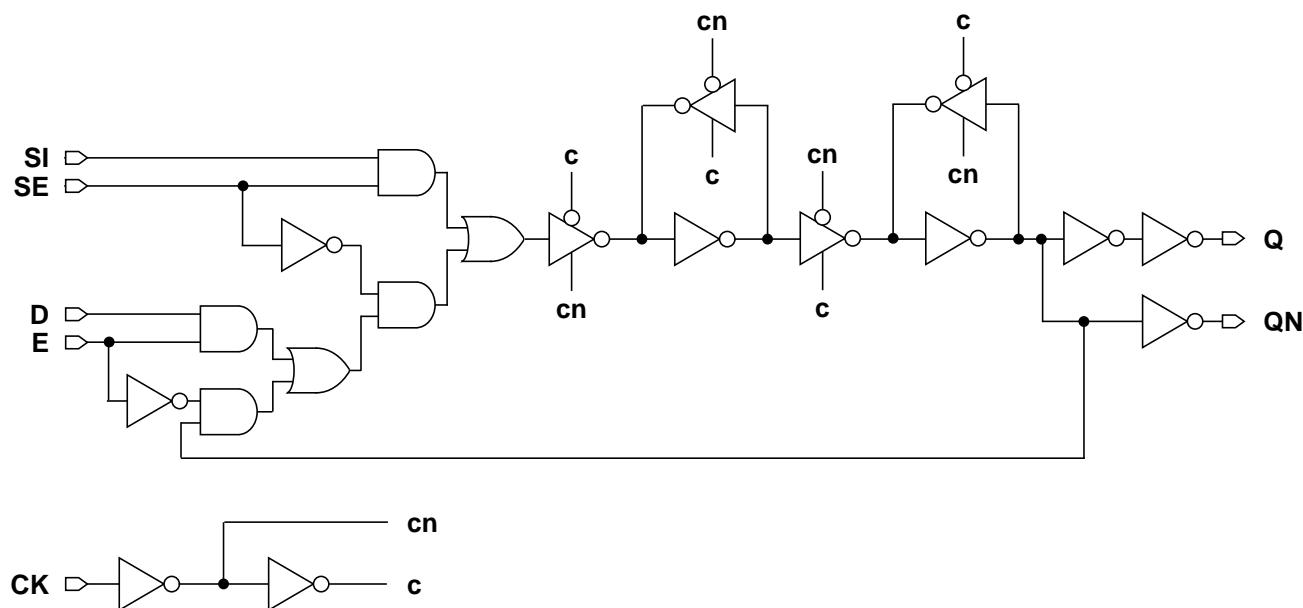
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| SEDFFXL | 5.04 | 17.82 |
| SEDFFX1 | 5.04 | 17.82 |
| SEDFFX2 | 5.04 | 19.80 |
| SEDFFX4 | 5.04 | 23.10 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0463 | 0.0478 | 0.0622 | 0.0920 |
| SE | 0.0547 | 0.0573 | 0.0711 | 0.1012 |
| D | 0.0382 | 0.0414 | 0.0536 | 0.0787 |
| CK | 0.0662 | 0.0721 | 0.0903 | 0.1300 |
| E | 0.0561 | 0.0580 | 0.0713 | 0.0991 |
| Q | 0.0425 | 0.0492 | 0.0782 | 0.1397 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0023 | 0.0021 | 0.0024 | 0.0035 |
| SE | 0.0045 | 0.0044 | 0.0049 | 0.0057 |
| D | 0.0022 | 0.0020 | 0.0024 | 0.0034 |
| CK | 0.0023 | 0.0031 | 0.0042 | 0.0071 |
| E | 0.0054 | 0.0052 | 0.0055 | 0.0064 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2433 | 0.2200 | 0.1893 | 0.1723 | 5.8900 | 4.6116 | 2.1311 | 1.0424 |
| CK → Q↓ | 0.1913 | 0.1623 | 0.1473 | 0.1407 | 3.5973 | 2.7299 | 1.3410 | 0.6346 |
| CK → QN↑ | 0.2757 | 0.2311 | 0.2117 | 0.2033 | 5.8988 | 4.2050 | 2.1293 | 1.0409 |
| CK → QN↓ | 0.3552 | 0.3130 | 0.2743 | 0.2513 | 3.5842 | 2.5553 | 1.3308 | 0.6281 |

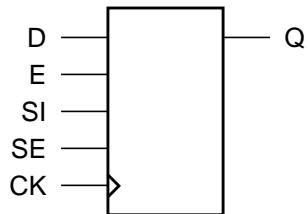
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.1758 | 0.1641 | 0.1914 | 0.1719 |
| | setup↓ → CK | 0.4258 | 0.5742 | 0.4766 | 0.3984 |
| | hold↑ → CK | -0.1523 | -0.1445 | -0.1562 | -0.1367 |
| | hold↓ → CK | -0.2773 | -0.3984 | -0.3281 | -0.2656 |
| SE | setup↑ → CK | 0.4414 | 0.5938 | 0.4961 | 0.4180 |
| | setup↓ → CK | 0.4648 | 0.6016 | 0.5000 | 0.4336 |
| | hold↑ → CK | -0.1289 | -0.1172 | -0.1289 | -0.1172 |
| | hold↓ → CK | -0.2344 | -0.2266 | -0.2383 | -0.2266 |
| D | setup↑ → CK | 0.1797 | 0.1797 | 0.1992 | 0.1758 |
| | setup↓ → CK | 0.4258 | 0.5625 | 0.4688 | 0.4023 |
| | hold↑ → CK | -0.1523 | -0.1445 | -0.1523 | -0.1328 |
| | hold↓ → CK | -0.2930 | -0.4141 | -0.3281 | -0.2773 |
| CK | minpwh | 0.1370 | 0.1224 | 0.1078 | 0.0933 |
| | minpwl | 0.2730 | 0.2293 | 0.2293 | 0.1953 |
| E | setup↑ → CK | 0.4648 | 0.6016 | 0.5117 | 0.4492 |
| | setup↓ → CK | 0.3633 | 0.5000 | 0.3945 | 0.3242 |
| | hold↑ → CK | -0.1680 | -0.1562 | -0.1680 | -0.1484 |
| | hold↓ → CK | -0.2266 | -0.2148 | -0.2305 | -0.2188 |

Cell Description

The SEDFFHQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q) and fast clock-to-output path.

Logic Symbol



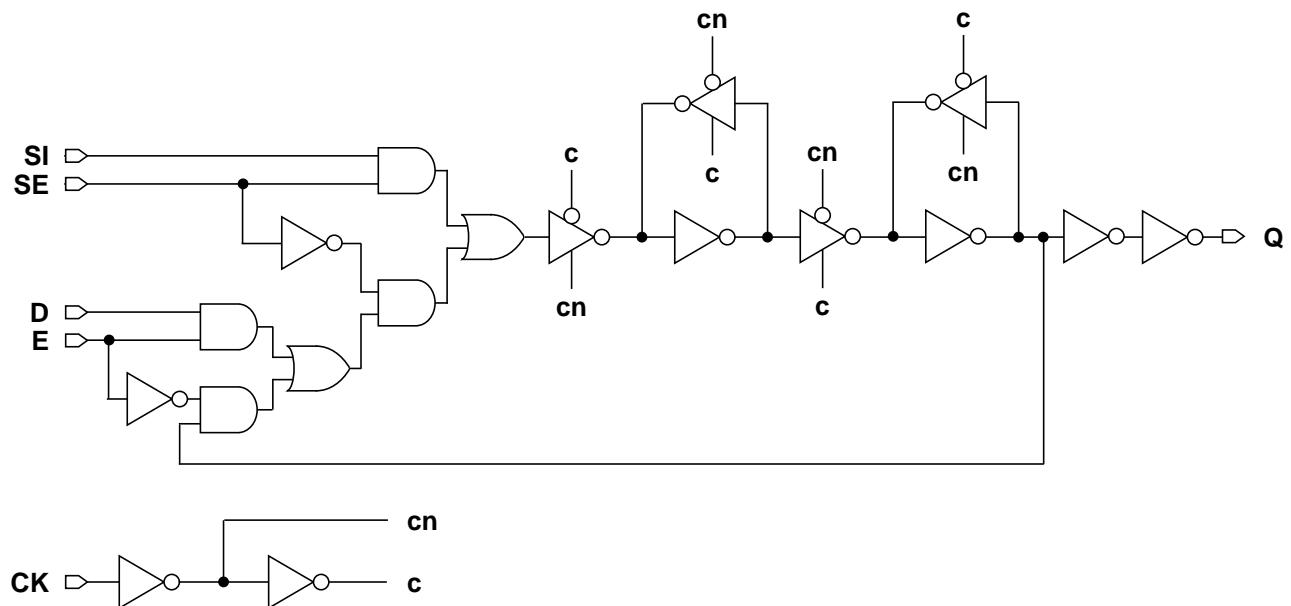
Functions

| D | E | SI | SE | CK | Q[n+1] |
|---|---|----|----|-----|--------|
| x | x | 1 | 1 | /\ | 1 |
| x | x | 0 | 1 | /\ | 0 |
| x | 0 | x | 0 | /\ | Q[n] |
| 0 | 1 | x | 0 | /\ | 0 |
| 1 | 1 | x | 0 | /\ | 1 |
| x | x | x | x | \/\ | Q[n] |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| SEDFFHQXL | 5.04 | 20.46 |
| SEDFFHQX1 | 5.04 | 20.46 |
| SEDFFHQX2 | 5.04 | 22.44 |
| SEDFFHQX4 | 5.04 | 25.08 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0532 | 0.0651 | 0.0855 | 0.1249 |
| SE | 0.0741 | 0.0842 | 0.1054 | 0.1458 |
| D | 0.0707 | 0.0821 | 0.1034 | 0.1442 |
| CK | 0.0621 | 0.0814 | 0.1099 | 0.1596 |
| E | 0.0927 | 0.0991 | 0.1185 | 0.1565 |
| Q | 0.0350 | 0.0454 | 0.0622 | 0.0913 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0024 | 0.0024 | 0.0024 | 0.0024 |
| SE | 0.0024 | 0.0024 | 0.0024 | 0.0024 |
| D | 0.0030 | 0.0032 | 0.0032 | 0.0032 |
| CK | 0.0024 | 0.0037 | 0.0048 | 0.0068 |
| E | 0.0024 | 0.0025 | 0.0025 | 0.0025 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q↑ | 0.2764 | 0.1790 | 0.1720 | 0.1510 | 5.8980 | 4.2002 | 2.0801 | 1.0400 |
| CK → Q↓ | 0.3251 | 0.2203 | 0.2107 | 0.1935 | 3.6063 | 2.5306 | 1.2916 | 0.6461 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.2227 | 0.2422 | 0.2695 | 0.3086 |
| | setup↓ → CK | 0.1953 | 0.2188 | 0.2227 | 0.2461 |
| | hold↑ → CK | -0.0938 | -0.1211 | -0.1406 | -0.1836 |
| | hold↓ → CK | -0.1758 | -0.1875 | -0.1953 | -0.2109 |
| SE | setup↑ → CK | 0.2891 | 0.3125 | 0.3398 | 0.3789 |
| | setup↓ → CK | 0.3008 | 0.3086 | 0.3281 | 0.3711 |
| | hold↑ → CK | -0.1602 | -0.1953 | -0.2148 | -0.2422 |
| | hold↓ → CK | -0.1523 | -0.1719 | -0.1953 | -0.2383 |
| D | setup↑ → CK | 0.3086 | 0.2930 | 0.3203 | 0.3594 |
| | setup↓ → CK | 0.3047 | 0.2656 | 0.2734 | 0.2969 |
| | hold↑ → CK | -0.1680 | -0.1719 | -0.1914 | -0.2383 |
| | hold↓ → CK | -0.2852 | -0.2305 | -0.2422 | -0.2617 |
| CK | minpwh | 0.1370 | 0.0933 | 0.0884 | 0.0787 |
| | minpwl | 0.1953 | 0.1856 | 0.1904 | 0.2196 |
| E | setup↑ → CK | 0.3672 | 0.3711 | 0.3945 | 0.4336 |
| | setup↓ → CK | 0.3320 | 0.2891 | 0.2930 | 0.3047 |
| | hold↑ → CK | -0.2422 | -0.2539 | -0.2734 | -0.3047 |
| | hold↓ → CK | -0.1172 | -0.1406 | -0.1914 | -0.2852 |

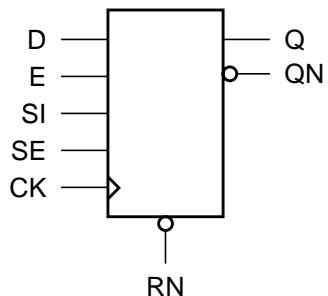
Cell Description

The SEDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), synchronous active-high enable (E) and synchronous active low reset (RN). Scan enable (SE) dominates reset (RN) and enable (E).

Functions

| RN | D | E | SI | SE | CK | Q[n+1] | QN[n+1] |
|----|---|---|----|----|----|--------|---------|
| x | x | x | 0 | 1 | / | 0 | 1 |
| x | x | x | 1 | 1 | / | 1 | 0 |
| 1 | x | 0 | x | 0 | / | Q[n] | QN[n] |
| 0 | x | x | x | 0 | / | 0 | 1 |
| 1 | 1 | 1 | x | 0 | / | 1 | 0 |
| 1 | 0 | 1 | x | 0 | / | 0 | 1 |
| x | x | x | x | x | / | Q[n] | QN[n] |

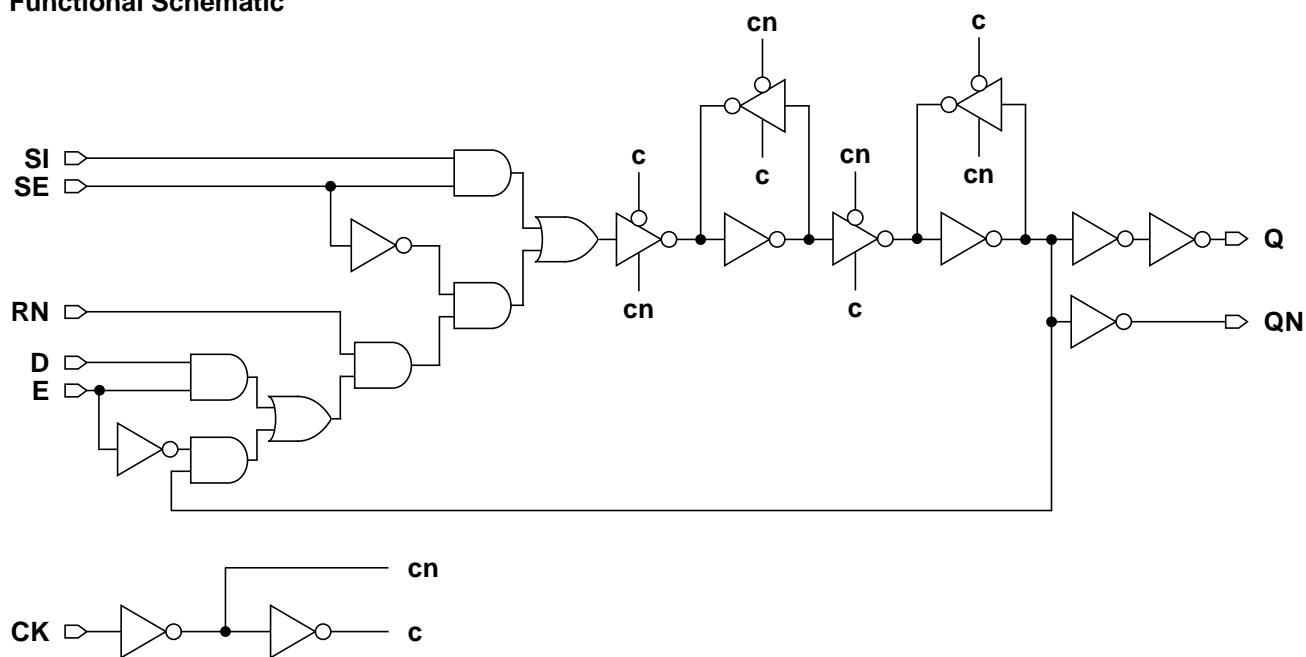
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| SEDFFFTRXL | 5.04 | 25.08 |
| SEDFFFTRX1 | 5.04 | 25.74 |
| SEDFFFTRX2 | 5.04 | 26.40 |
| SEDFFFTRX4 | 5.04 | 27.72 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0565 | 0.0724 | 0.0724 | 0.0723 |
| SE | 0.0820 | 0.0978 | 0.0978 | 0.0961 |
| D | 0.0721 | 0.0932 | 0.0932 | 0.0928 |
| CK | 0.0645 | 0.0901 | 0.0914 | 0.0912 |
| E | 0.0926 | 0.1148 | 0.1144 | 0.1136 |
| RN | 0.0513 | 0.0707 | 0.0707 | 0.0705 |
| Q | 0.0461 | 0.0621 | 0.0890 | 0.1514 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| SI | 0.0025 | 0.0025 | 0.0025 | 0.0025 |
| SE | 0.0046 | 0.0046 | 0.0046 | 0.0046 |
| D | 0.0023 | 0.0032 | 0.0032 | 0.0032 |
| CK | 0.0023 | 0.0039 | 0.0038 | 0.0039 |
| E | 0.0025 | 0.0025 | 0.0025 | 0.0025 |
| RN | 0.0030 | 0.0030 | 0.0030 | 0.0030 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|----------------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| CK → Q \uparrow | 0.3316 | 0.2032 | 0.2236 | 0.2682 | 5.9026 | 4.2016 | 2.1285 | 1.0405 |
| CK → Q \downarrow | 0.3571 | 0.2317 | 0.2426 | 0.2652 | 3.6258 | 2.5319 | 1.3364 | 0.6413 |
| CK → QN \uparrow | 0.2164 | 0.1674 | 0.1766 | 0.1974 | 5.9191 | 4.2055 | 2.1330 | 1.0453 |
| CK → QN \downarrow | 0.2253 | 0.1534 | 0.1750 | 0.2187 | 3.7821 | 2.5696 | 1.3660 | 0.6699 |

Timing Constraints at 25°C, 1.8V, Typical Process

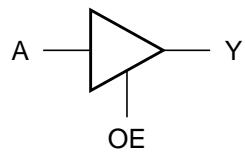
| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| SI | setup↑ → CK | 0.2734 | 0.3242 | 0.3203 | 0.2930 |
| | setup↓ → CK | 0.2188 | 0.2422 | 0.2422 | 0.2422 |
| | hold↑ → CK | -0.1367 | -0.1836 | -0.1836 | -0.1797 |
| | hold↓ → CK | -0.1992 | -0.2070 | -0.2070 | -0.2070 |
| SE | setup↑ → CK | 0.3359 | 0.3945 | 0.3867 | 0.3633 |
| | setup↓ → CK | 0.3594 | 0.3828 | 0.3789 | 0.3477 |
| | hold↑ → CK | -0.2031 | -0.2461 | -0.2461 | -0.2461 |
| | hold↓ → CK | -0.1758 | -0.2383 | -0.2383 | -0.2344 |
| D | setup↑ → CK | 0.3555 | 0.3594 | 0.3516 | 0.3203 |
| | setup↓ → CK | 0.3164 | 0.2812 | 0.2812 | 0.2812 |
| | hold↑ → CK | -0.2070 | -0.2148 | -0.2188 | -0.2109 |
| | hold↓ → CK | -0.2969 | -0.2461 | -0.2422 | -0.2461 |
| CK | minpwh | 0.1807 | 0.1030 | 0.1224 | 0.1613 |
| | minpwl | 0.2244 | 0.2196 | 0.2244 | 0.2244 |
| E | setup↑ → CK | 0.4219 | 0.4297 | 0.4336 | 0.3945 |
| | setup↓ → CK | 0.3438 | 0.3242 | 0.3125 | 0.3047 |
| | hold↑ → CK | -0.2969 | -0.2969 | -0.2969 | -0.2969 |
| | hold↓ → CK | -0.1094 | -0.1289 | -0.1602 | -0.2422 |
| RN | setup↑ → CK | 0.2578 | 0.2930 | 0.2930 | 0.2656 |
| | setup↓ → CK | 0.2031 | 0.2344 | 0.2344 | 0.2344 |
| | hold↑ → CK | -0.1172 | -0.1562 | -0.1523 | -0.1484 |
| | hold↓ → CK | -0.1875 | -0.1992 | -0.1992 | -0.1992 |

Cell Description

The TBUF cell provides the logical buffer of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



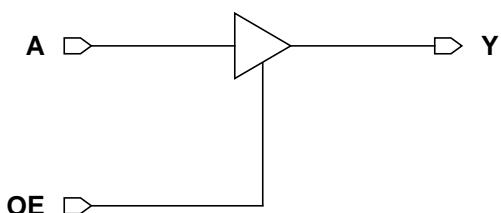
Functions

| OE | A | Y |
|----|---|---|
| 0 | x | Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TBUFXL | 5.04 | 4.62 |
| TBUFX1 | 5.04 | 4.62 |
| TBUFX2 | 5.04 | 4.62 |
| TBUFX3 | 5.04 | 5.28 |
| TBUFX4 | 5.04 | 5.94 |
| TBUFX8 | 5.04 | 7.92 |
| TBUFX12 | 5.04 | 9.90 |
| TBUFX16 | 5.04 | 11.22 |
| TBUFX20 | 5.04 | 15.18 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | | | | | | |
|-----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0266 | 0.0303 | 0.0403 | 0.0527 | 0.0680 | 0.1242 | 0.1777 | 0.2323 | 0.2909 |
| OE | 0.0200 | 0.0226 | 0.0307 | 0.0386 | 0.0510 | 0.0911 | 0.1374 | 0.1745 | 0.2243 |

Pin Capacitance

| Pin | Capacitance (pF) | | | | | | | | |
|-----|------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0026 | 0.0026 | 0.0035 | 0.0047 | 0.0061 | 0.0125 | 0.0176 | 0.0212 | 0.0277 |
| OE | 0.0047 | 0.0049 | 0.0049 | 0.0049 | 0.0053 | 0.0073 | 0.0104 | 0.0131 | 0.0161 |
| Y | 0.0018 | 0.0023 | 0.0041 | 0.0047 | 0.0063 | 0.0123 | 0.0181 | 0.0238 | 0.0302 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | | | | | |
|-------------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 0.0988 | 0.1061 | 0.1093 | 0.1075 | 0.1036 | 0.0984 | 0.0904 | 0.0920 | 0.0909 |
| A → Y↓ | 0.1533 | 0.1628 | 0.1468 | 0.1384 | 0.1348 | 0.1255 | 0.1222 | 0.1250 | 0.1222 |
| OE → Y↑ | 0.0635 | 0.0687 | 0.0790 | 0.0836 | 0.0805 | 0.0790 | 0.0753 | 0.0747 | 0.0748 |
| OE → Y↓ | 0.1149 | 0.1172 | 0.1128 | 0.1089 | 0.1100 | 0.1069 | 0.1064 | 0.1048 | 0.1049 |

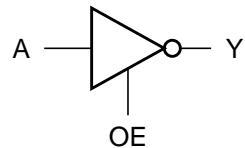
| Description | K_{load} (ns/pF) | | | | | | | | |
|-------------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 5.8989 | 4.2124 | 2.2112 | 1.4106 | 1.0805 | 0.5400 | 0.3477 | 0.2608 | 0.2146 |
| A → Y↓ | 4.5682 | 2.6166 | 1.3511 | 0.8499 | 0.6640 | 0.3494 | 0.2387 | 0.1794 | 0.1386 |
| OE → Y↑ | 5.8913 | 4.2081 | 2.2100 | 1.4100 | 1.0801 | 0.5399 | 0.3476 | 0.2607 | 0.2146 |
| OE → Y↓ | 4.5626 | 2.6105 | 1.3471 | 0.8473 | 0.6624 | 0.3488 | 0.2384 | 0.1791 | 0.1383 |

Cell Description

The TBUFI cell provides the logical inversion of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$$Y = \bar{A}$$

Logic Symbol



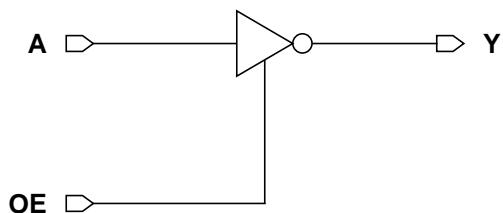
Functions

| OE | A | Y |
|----|---|---|
| 0 | x | Z |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| TBUFIXL | 5.04 | 2.64 |
| TBUFIX1 | 5.04 | 2.64 |
| TBUFIX2 | 5.04 | 3.96 |
| TBUFIX3 | 5.04 | 6.60 |
| TBUFIX4 | 5.04 | 6.60 |
| TBUFIX8 | 5.04 | 8.58 |
| TBUFIX12 | 5.04 | 11.22 |
| TBUFIX16 | 5.04 | 12.54 |
| TBUFIX20 | 5.04 | 16.50 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | | | | | | |
|-----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0246 | 0.0244 | 0.0461 | 0.0542 | 0.0667 | 0.1240 | 0.1843 | 0.2386 | 0.2978 |
| OE | 0.0152 | 0.0151 | 0.0263 | 0.0402 | 0.0490 | 0.0918 | 0.1409 | 0.1832 | 0.2279 |

Pin Capacitance

| Pin | Capacitance (pF) | | | | | | | | |
|-----|------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A | 0.0048 | 0.0048 | 0.0096 | 0.0025 | 0.0029 | 0.0051 | 0.0070 | 0.0091 | 0.0112 |
| OE | 0.0033 | 0.0033 | 0.0045 | 0.0049 | 0.0052 | 0.0074 | 0.0104 | 0.0129 | 0.0161 |
| Y | 0.0030 | 0.0030 | 0.0045 | 0.0048 | 0.0058 | 0.0120 | 0.0184 | 0.0246 | 0.0306 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | | | | | |
|-------------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 0.0628 | 0.0626 | 0.0591 | 0.1881 | 0.1785 | 0.1645 | 0.1610 | 0.1563 | 0.1570 |
| A → Y↓ | 0.0325 | 0.0335 | 0.0309 | 0.1829 | 0.1717 | 0.1655 | 0.1647 | 0.1643 | 0.1613 |
| OE → Y↑ | 0.0627 | 0.0631 | 0.0655 | 0.0850 | 0.0842 | 0.0777 | 0.0767 | 0.0760 | 0.0761 |
| OE → Y↓ | 0.0211 | 0.0219 | 0.0192 | 0.1117 | 0.1075 | 0.1082 | 0.1074 | 0.1064 | 0.1051 |

| Description | K_{load} (ns/pF) | | | | | | | | |
|-------------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | XL | X1 | X2 | X3 | X4 | X8 | X12 | X16 | X20 |
| A → Y↑ | 6.0770 | 6.0686 | 3.0348 | 1.3911 | 1.1010 | 0.5599 | 0.3481 | 0.2610 | 0.2148 |
| A → Y↓ | 2.8809 | 2.9379 | 1.4695 | 0.8522 | 0.6691 | 0.3158 | 0.2259 | 0.1685 | 0.1300 |
| OE → Y↑ | 6.0916 | 6.0747 | 3.0383 | 1.3895 | 1.0999 | 0.5594 | 0.3477 | 0.2608 | 0.2147 |
| OE → Y↓ | 2.8836 | 2.9394 | 1.4706 | 0.8492 | 0.6673 | 0.3150 | 0.2255 | 0.1681 | 0.1298 |

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 1$$

Logic Symbol



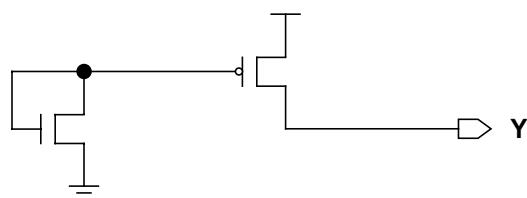
Function

| |
|---|
| Y |
| 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TIEHI | 5.04 | 1.32 |

Functional Schematic

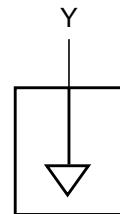


Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 0$$

Logic Symbol



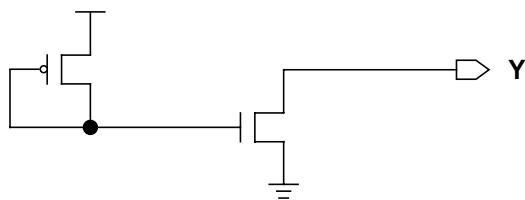
Function

| |
|---|
| Y |
| 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TIELO | 5.04 | 1.32 |

Functional Schematic



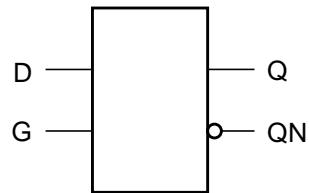
Cell Description

The TLAT cell is an active-high D-type transparent latch. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

| G | D | Q[n+1] | QN[n+1] |
|---|---|--------|---------|
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 0 | x | Q[n] | QN[n] |

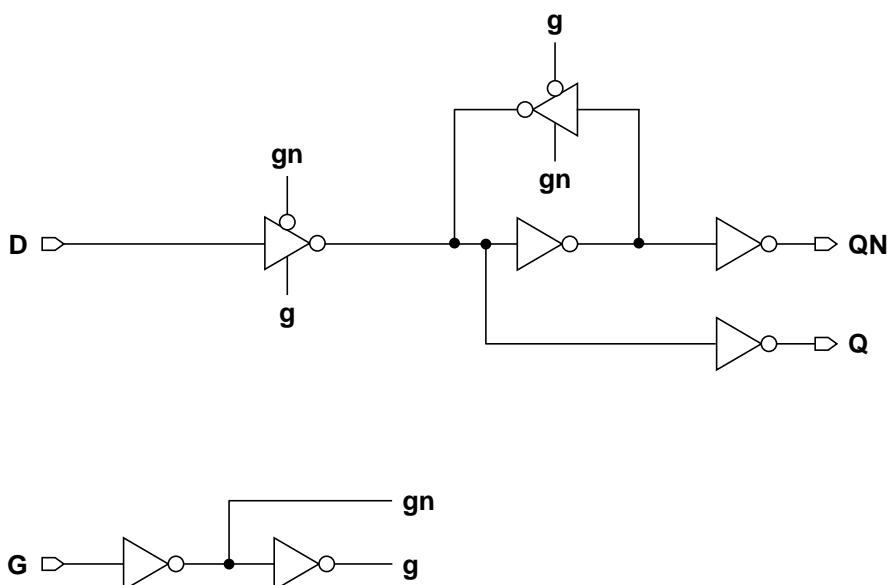
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| TLATXL | 5.04 | 7.26 |
| TLATX1 | 5.04 | 7.26 |
| TLATX2 | 5.04 | 7.92 |
| TLATX4 | 5.04 | 11.22 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0049 | 0.0060 | 0.0097 | 0.0213 |
| G | 0.0226 | 0.0242 | 0.0290 | 0.0477 |
| Q | 0.0374 | 0.0436 | 0.0683 | 0.1187 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0035 | 0.0042 | 0.0063 | 0.0144 |
| G | 0.0023 | 0.0028 | 0.0029 | 0.0047 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.0967 | 0.0942 | 0.0902 | 0.0814 | 5.8967 | 4.2068 | 2.1568 | 1.0783 |
| D → Q↓ | 0.1516 | 0.1505 | 0.1428 | 0.1295 | 3.5853 | 2.5733 | 1.3129 | 0.6542 |
| G → Q↑ | 0.1964 | 0.1856 | 0.1942 | 0.1676 | 5.8957 | 4.2065 | 2.1566 | 1.0783 |
| G → Q↓ | 0.1649 | 0.1601 | 0.1587 | 0.1450 | 3.5816 | 2.5719 | 1.3125 | 0.6539 |
| D → QN↑ | 0.2050 | 0.2090 | 0.2151 | 0.2028 | 5.8942 | 4.2045 | 2.1539 | 1.0773 |
| D → QN↓ | 0.1723 | 0.1761 | 0.1855 | 0.1725 | 3.5079 | 2.5434 | 1.3005 | 0.6502 |
| G → QN↑ | 0.2190 | 0.2193 | 0.2315 | 0.2185 | 5.8946 | 4.2047 | 2.1539 | 1.0773 |
| G → QN↓ | 0.2731 | 0.2685 | 0.2903 | 0.2592 | 3.5081 | 2.5434 | 1.3005 | 0.6502 |

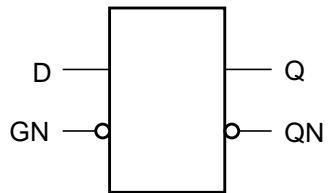
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → G | -0.0156 | -0.0039 | -0.0195 | -0.0195 |
| | setup↓ → G | 0.0898 | 0.0977 | 0.0859 | 0.0781 |
| | hold↑ → G | 0.0273 | 0.0195 | 0.0312 | 0.0312 |
| | hold↓ → G | -0.0859 | -0.0938 | -0.0820 | -0.0703 |
| G | minpwh | 0.1127 | 0.1127 | 0.1127 | 0.0981 |

Cell Description

The TLATN cell is an active-low D-type transparent latch. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



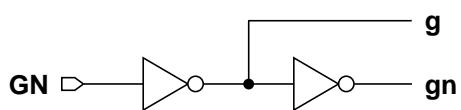
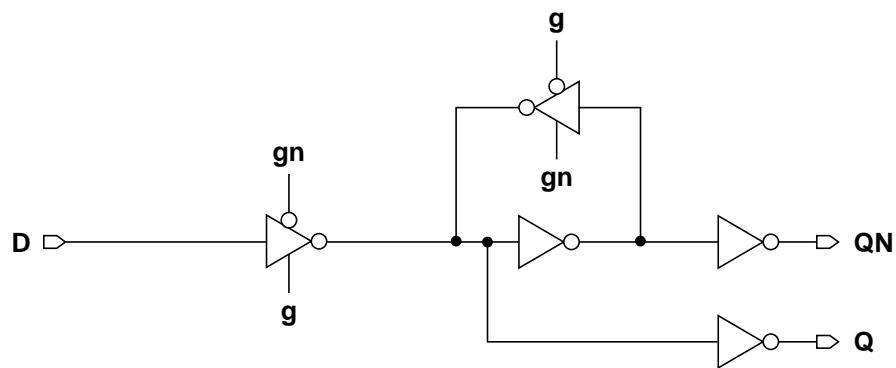
Functions

| GN | D | Q[n+1] | QN[n+1] |
|----|---|--------|---------|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | x | Q[n] | QN[n] |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TLATNXL | 5.04 | 7.26 |
| TLATNX1 | 5.04 | 7.26 |
| TLATNX2 | 5.04 | 7.92 |
| TLATNX4 | 5.04 | 11.22 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0051 | 0.0062 | 0.0095 | 0.0210 |
| GN | 0.0254 | 0.0286 | 0.0359 | 0.0632 |
| Q | 0.0372 | 0.0443 | 0.0735 | 0.1246 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0036 | 0.0042 | 0.0065 | 0.0144 |
| GN | 0.0023 | 0.0028 | 0.0029 | 0.0047 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.0959 | 0.0914 | 0.0890 | 0.0794 | 5.8974 | 4.2061 | 2.1323 | 1.0783 |
| D → Q↓ | 0.1511 | 0.1481 | 0.1450 | 0.1308 | 3.5832 | 2.5711 | 1.3139 | 0.6543 |
| GN → Q↑ | 0.1659 | 0.1436 | 0.1466 | 0.1224 | 5.9010 | 4.2078 | 2.1333 | 1.0788 |
| GN → Q↓ | 0.2511 | 0.2347 | 0.2390 | 0.2175 | 3.5824 | 2.5709 | 1.3137 | 0.6542 |
| D → QN↑ | 0.2043 | 0.2071 | 0.2191 | 0.2044 | 5.8940 | 4.2041 | 2.1292 | 1.0773 |
| D → QN↓ | 0.1713 | 0.1741 | 0.1870 | 0.1708 | 3.5069 | 2.5438 | 1.3009 | 0.6502 |
| GN → QN↑ | 0.3048 | 0.2942 | 0.3133 | 0.2912 | 5.8944 | 4.2041 | 2.1293 | 1.0773 |
| GN → QN↓ | 0.2428 | 0.2279 | 0.2464 | 0.2148 | 3.5074 | 2.5439 | 1.3009 | 0.6502 |

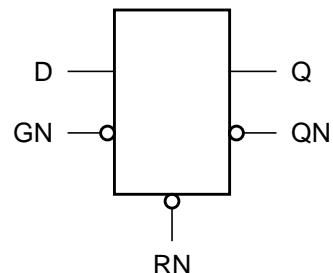
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → GN | 0.0586 | 0.0625 | 0.0586 | 0.0547 |
| | setup↓ → GN | 0.0547 | 0.0625 | 0.0469 | 0.0352 |
| | hold↑ → GN | -0.0508 | -0.0508 | -0.0508 | -0.0430 |
| | hold↓ → GN | -0.0430 | -0.0430 | -0.0312 | -0.0234 |
| GN | minpw1 | 0.1613 | 0.1516 | 0.1467 | 0.1273 |

Cell Description

The TLATNR cell is an active-low D-type transparent latch with asynchronous active-low reset (RN). When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



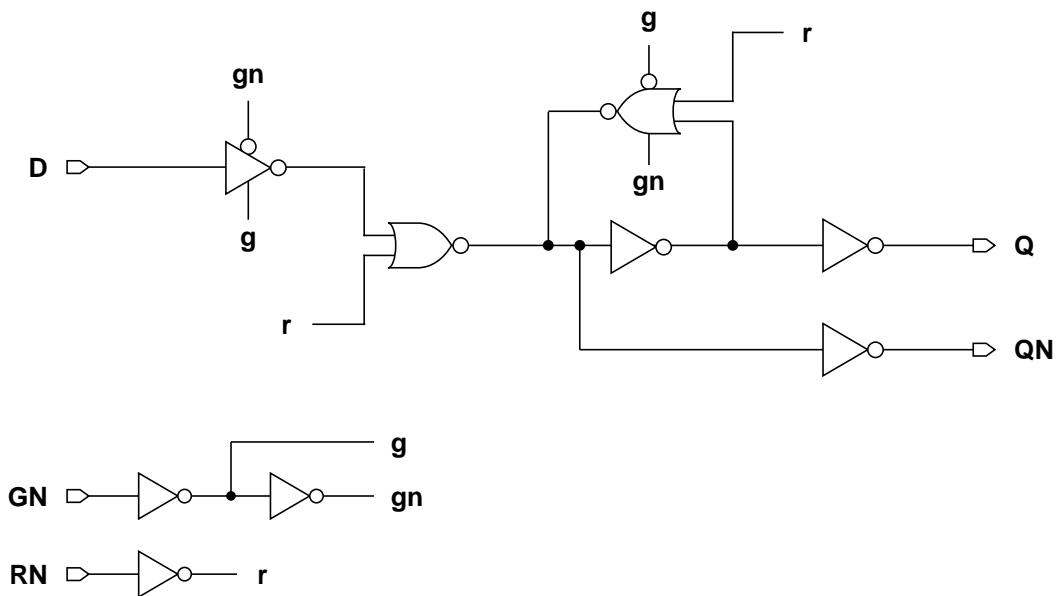
Functions

| RN | GN | D | Q[n+1] | QN[n+1] |
|----|----|---|--------|---------|
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | x | Q[n] | QN[n] |
| 0 | x | x | 0 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TLATNRXL | 5.04 | 8.58 |
| TLATNRX1 | 5.04 | 8.58 |
| TLATNRX2 | 5.04 | 9.24 |
| TLATNRX4 | 5.04 | 11.88 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0037 | 0.0044 | 0.0073 | 0.0144 |
| GN | 0.0276 | 0.0295 | 0.0396 | 0.0628 |
| RN | 0.0046 | 0.0046 | 0.0057 | 0.0074 |
| Q | 0.0411 | 0.0491 | 0.0793 | 0.1386 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0028 | 0.0033 | 0.0055 | 0.0105 |
| GN | 0.0023 | 0.0023 | 0.0026 | 0.0039 |
| RN | 0.0043 | 0.0045 | 0.0056 | 0.0075 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1431 | 0.1358 | 0.1231 | 0.1183 | 5.9359 | 4.2216 | 2.1388 | 1.0457 |
| D → Q↓ | 0.2218 | 0.2167 | 0.1959 | 0.1826 | 3.7329 | 2.6284 | 1.3320 | 0.6635 |
| GN → Q↑ | 0.2138 | 0.2081 | 0.1840 | 0.1677 | 5.9359 | 4.2218 | 2.1392 | 1.0463 |
| GN → Q↓ | 0.3249 | 0.3224 | 0.2945 | 0.2798 | 3.7319 | 2.6281 | 1.3317 | 0.6634 |
| RN → Q↑ | 0.1402 | 0.1317 | 0.1158 | 0.1096 | 5.9358 | 4.2215 | 2.1387 | 1.0458 |
| RN → Q↓ | 0.1477 | 0.1683 | 0.2492 | 0.4030 | 3.6131 | 2.6156 | 1.3932 | 0.7611 |
| D → QN↑ | 0.2812 | 0.2794 | 0.2709 | 0.2592 | 5.8959 | 4.2059 | 2.1291 | 1.0409 |
| D → QN↓ | 0.2267 | 0.2247 | 0.2231 | 0.2174 | 3.5230 | 2.5503 | 1.3014 | 0.6510 |
| GN → QN↑ | 0.3853 | 0.3860 | 0.3701 | 0.3566 | 5.8960 | 4.2061 | 2.1292 | 1.0409 |
| GN → QN↓ | 0.2991 | 0.2984 | 0.2853 | 0.2679 | 3.5253 | 2.5513 | 1.3017 | 0.6511 |
| RN → QN↑ | 0.2080 | 0.2303 | 0.3280 | 0.4992 | 5.8941 | 4.2058 | 2.1291 | 1.0407 |
| RN → QN↓ | 0.2244 | 0.2210 | 0.2162 | 0.2089 | 3.5238 | 2.5506 | 1.3015 | 0.6510 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → GN | 0.1055 | 0.1016 | 0.0859 | 0.0820 |
| | setup↓ → GN | 0.1289 | 0.1211 | 0.0898 | 0.0664 |
| | hold↑ → GN | -0.0977 | -0.0898 | -0.0781 | -0.0742 |
| | hold↓ → GN | -0.1133 | -0.1055 | -0.0742 | -0.0586 |
| GN | minpwl | 0.2390 | 0.2293 | 0.1953 | 0.1710 |
| RN | minpwl | 0.1467 | 0.1613 | 0.2244 | 0.3362 |
| | recovery | 0.1055 | 0.0938 | 0.0781 | 0.0703 |

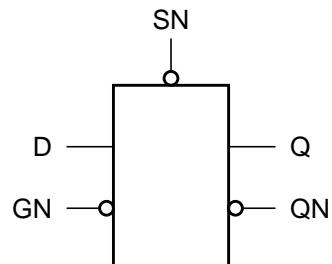
Cell Description

The TLATNS cell is an active-low D-type transparent latch with asynchronous active-low set (SN). When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Functions

| SN | GN | D | Q[n+1] | QN[n+1] |
|----|----|---|--------|---------|
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | x | Q[n] | QN[n] |
| 0 | x | x | 1 | 0 |

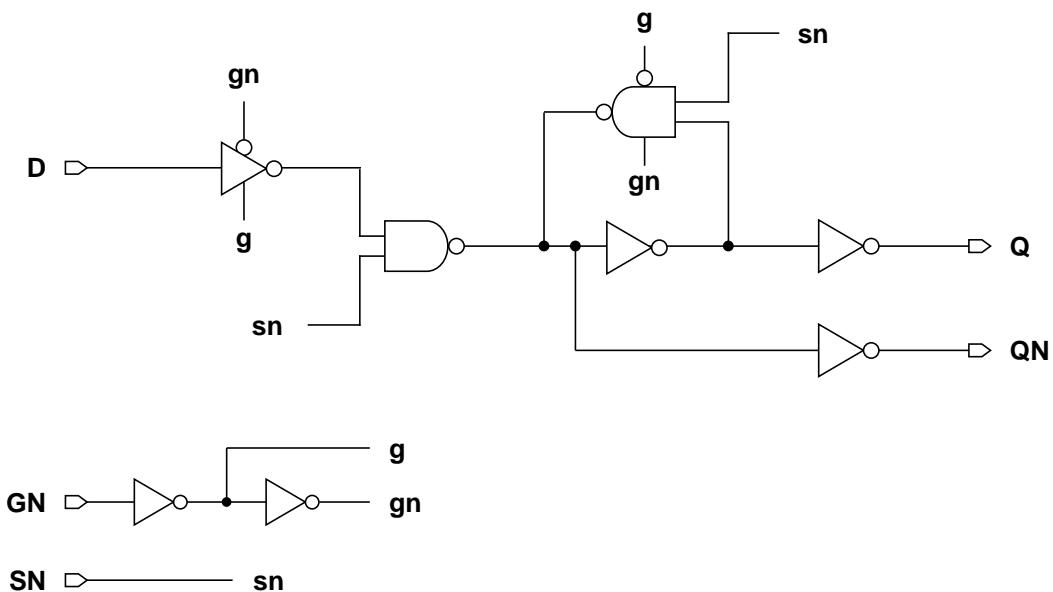
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| TLATNSXL | 5.04 | 10.56 |
| TLATNSX1 | 5.04 | 10.56 |
| TLATNSX2 | 5.04 | 11.22 |
| TLATNSX4 | 5.04 | 13.86 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0040 | 0.0048 | 0.0077 | 0.0141 |
| GN | 0.0268 | 0.0297 | 0.0355 | 0.0526 |
| SN | 0.0149 | 0.0152 | 0.0161 | 0.0226 |
| Q | 0.0545 | 0.0607 | 0.0918 | 0.1483 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0029 | 0.0033 | 0.0052 | 0.0096 |
| GN | 0.0024 | 0.0029 | 0.0030 | 0.0042 |
| SN | 0.0022 | 0.0022 | 0.0027 | 0.0039 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1489 | 0.1374 | 0.1220 | 0.1178 | 5.9405 | 4.2248 | 2.1376 | 1.0457 |
| D → Q↓ | 0.2927 | 0.2829 | 0.2567 | 0.2388 | 3.7706 | 2.8052 | 1.3717 | 0.6814 |
| GN → Q↑ | 0.2286 | 0.1946 | 0.1799 | 0.1627 | 5.9394 | 4.2258 | 2.1398 | 1.0469 |
| GN → Q↓ | 0.3832 | 0.3580 | 0.3377 | 0.3024 | 3.7701 | 2.8053 | 1.3717 | 0.6815 |
| SN → Q↑ | 0.2015 | 0.2150 | 0.2498 | 0.3402 | 5.8986 | 4.2116 | 2.1403 | 1.0552 |
| SN → Q↓ | 0.3274 | 0.3174 | 0.2840 | 0.2627 | 3.7706 | 2.8054 | 1.3717 | 0.6815 |
| D → QN↑ | 0.3742 | 0.3558 | 0.3361 | 0.3174 | 5.8926 | 4.2056 | 2.1299 | 1.0410 |
| D → QN↓ | 0.2480 | 0.2491 | 0.2288 | 0.2164 | 3.2944 | 2.5608 | 1.3045 | 0.6509 |
| GN → QN↑ | 0.4662 | 0.4322 | 0.4179 | 0.3817 | 5.8933 | 4.2059 | 2.1301 | 1.0410 |
| GN → QN↓ | 0.3295 | 0.3083 | 0.2890 | 0.2632 | 3.2947 | 2.5609 | 1.3045 | 0.6510 |
| SN → QN↑ | 0.4094 | 0.3907 | 0.3636 | 0.3416 | 5.8930 | 4.2058 | 2.1300 | 1.0410 |
| SN → QN↓ | 0.2995 | 0.3254 | 0.3609 | 0.4503 | 3.2890 | 2.5597 | 1.3048 | 0.6520 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → GN | 0.1250 | 0.1172 | 0.0938 | 0.0898 |
| | setup↓ → GN | 0.2109 | 0.1875 | 0.1484 | 0.1289 |
| | hold↑ → GN | -0.1172 | -0.1133 | -0.0898 | -0.0820 |
| | hold↓ → GN | -0.1641 | -0.1445 | -0.1172 | -0.1094 |
| GN | minpwl | 0.3070 | 0.2682 | 0.2342 | 0.2001 |
| SN | minpwl | 0.1710 | 0.1807 | 0.1953 | 0.2439 |
| | recovery | 0.2383 | 0.2148 | 0.1719 | 0.1523 |

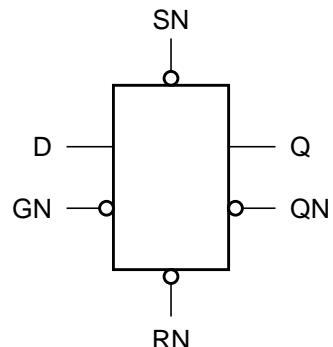
Cell Description

The TLATNSR cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Functions

| RN | SN | GN | D | Q[n+1] | QN[n+1] |
|----|----|----|---|--------|---------|
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | x | Q[n] | QN[n] |
| 0 | 1 | x | x | 0 | 1 |
| 1 | 0 | x | x | 1 | 0 |
| 0 | 0 | x | x | 1 | 0 |

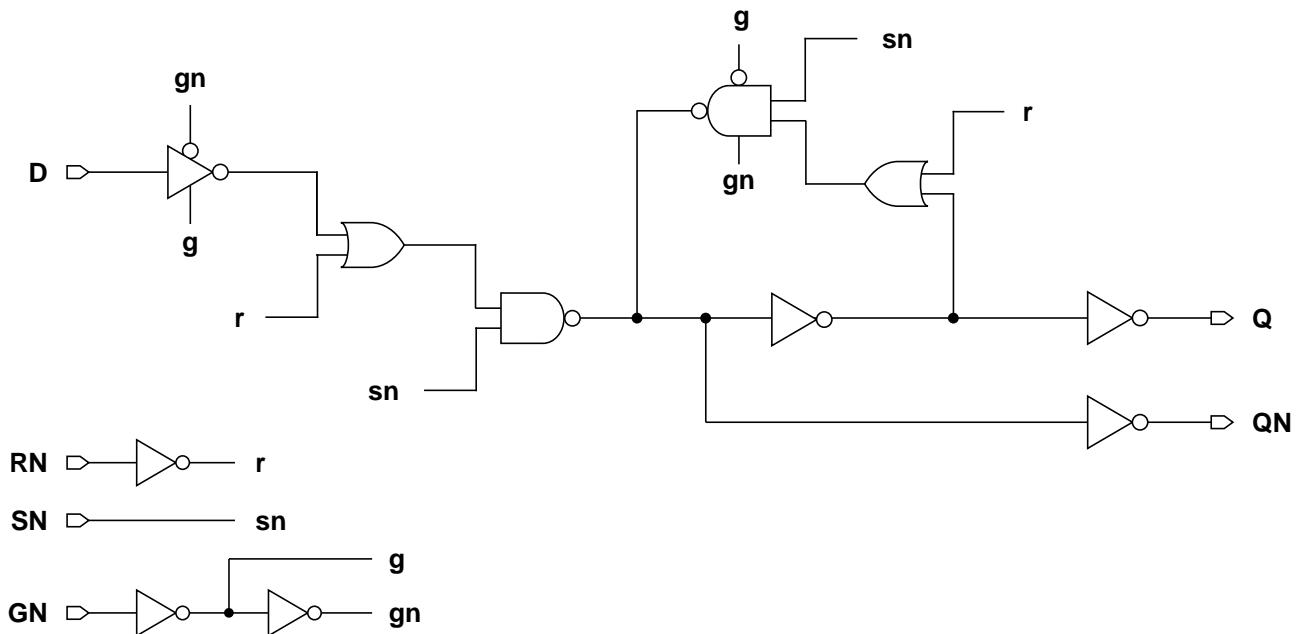
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| TLATNSRXL | 5.04 | 11.22 |
| TLATNSRX1 | 5.04 | 11.22 |
| TLATNSRX2 | 5.04 | 11.88 |
| TLATNSRX4 | 5.04 | 16.50 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0037 | 0.0045 | 0.0077 | 0.0157 |
| GN | 0.0282 | 0.0309 | 0.0393 | 0.0688 |
| SN | 0.0164 | 0.0184 | 0.0248 | 0.0448 |
| RN | 0.0051 | 0.0057 | 0.0094 | 0.0178 |
| Q | 0.0601 | 0.0688 | 0.1081 | 0.1886 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0030 | 0.0035 | 0.0054 | 0.0115 |
| GN | 0.0023 | 0.0029 | 0.0031 | 0.0044 |
| SN | 0.0023 | 0.0028 | 0.0041 | 0.0070 |
| RN | 0.0043 | 0.0047 | 0.0065 | 0.0116 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1944 | 0.1805 | 0.1801 | 0.1664 | 5.9895 | 4.2433 | 2.1482 | 1.0497 |
| D → Q↓ | 0.3412 | 0.3326 | 0.3072 | 0.2879 | 4.2006 | 2.8990 | 1.4225 | 0.7053 |
| GN → Q↑ | 0.2654 | 0.2259 | 0.2259 | 0.2022 | 5.9881 | 4.2431 | 2.1482 | 1.0499 |
| GN → Q↓ | 0.4199 | 0.3933 | 0.3746 | 0.3530 | 4.2024 | 2.8990 | 1.4225 | 0.7054 |
| SN → Q↑ | 0.2325 | 0.2158 | 0.1882 | 0.1857 | 5.9208 | 4.2195 | 2.1360 | 1.0445 |
| SN → Q↓ | 0.3728 | 0.3580 | 0.3238 | 0.3071 | 4.1835 | 2.8914 | 1.4185 | 0.7033 |
| RN → Q↑ | 0.1891 | 0.1752 | 0.1750 | 0.1617 | 5.9895 | 4.2433 | 2.1482 | 1.0497 |
| RN → Q↓ | 0.2524 | 0.2436 | 0.2177 | 0.2009 | 4.0890 | 2.8672 | 1.4045 | 0.6983 |
| D → QN↑ | 0.4237 | 0.4092 | 0.3884 | 0.3675 | 5.8952 | 4.2063 | 2.1298 | 1.0410 |
| D → QN↓ | 0.2999 | 0.2978 | 0.2882 | 0.2675 | 3.5443 | 2.5634 | 1.3036 | 0.6513 |
| GN → QN↑ | 0.5040 | 0.4715 | 0.4569 | 0.4332 | 5.8957 | 4.2066 | 2.1299 | 1.0410 |
| GN → QN↓ | 0.3724 | 0.3449 | 0.3352 | 0.3042 | 3.5466 | 2.5643 | 1.3040 | 0.6514 |
| SN → QN↑ | 0.4551 | 0.4346 | 0.4045 | 0.3859 | 5.8960 | 4.2067 | 2.1300 | 1.0410 |
| SN → QN↓ | 0.3366 | 0.3307 | 0.2936 | 0.2848 | 3.5356 | 2.5610 | 1.3027 | 0.6509 |
| RN → QN↑ | 0.3330 | 0.3167 | 0.2939 | 0.2747 | 5.8924 | 4.2071 | 2.1303 | 1.0412 |
| RN → QN↓ | 0.2952 | 0.2932 | 0.2835 | 0.2629 | 3.5453 | 2.5638 | 1.3038 | 0.6513 |

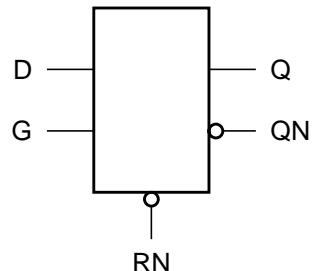
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → GN | 0.1680 | 0.1602 | 0.1484 | 0.1328 |
| | setup↓ → GN | 0.2656 | 0.2461 | 0.2070 | 0.1719 |
| | hold↑ → GN | -0.1562 | -0.1484 | -0.1406 | -0.1250 |
| | hold↓ → GN | -0.2148 | -0.1992 | -0.1719 | -0.1484 |
| GN | minpwl | 0.3507 | 0.3119 | 0.2779 | 0.2439 |
| SN | minpwl | 0.2001 | 0.1807 | 0.1516 | 0.1418 |
| | recovery | 0.2852 | 0.2617 | 0.2148 | 0.1836 |
| | removal | -0.2891 | -0.2656 | -0.2148 | -0.1836 |
| RN | minpwl | 0.2487 | 0.2244 | 0.1856 | 0.1516 |
| | recovery | 0.1602 | 0.1523 | 0.1445 | 0.1289 |
| | removal | -0.1602 | -0.1523 | -0.1406 | -0.1250 |

Cell Description

The TLATR cell is an active-high D-type transparent latch with asynchronous active-low reset (RN). When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



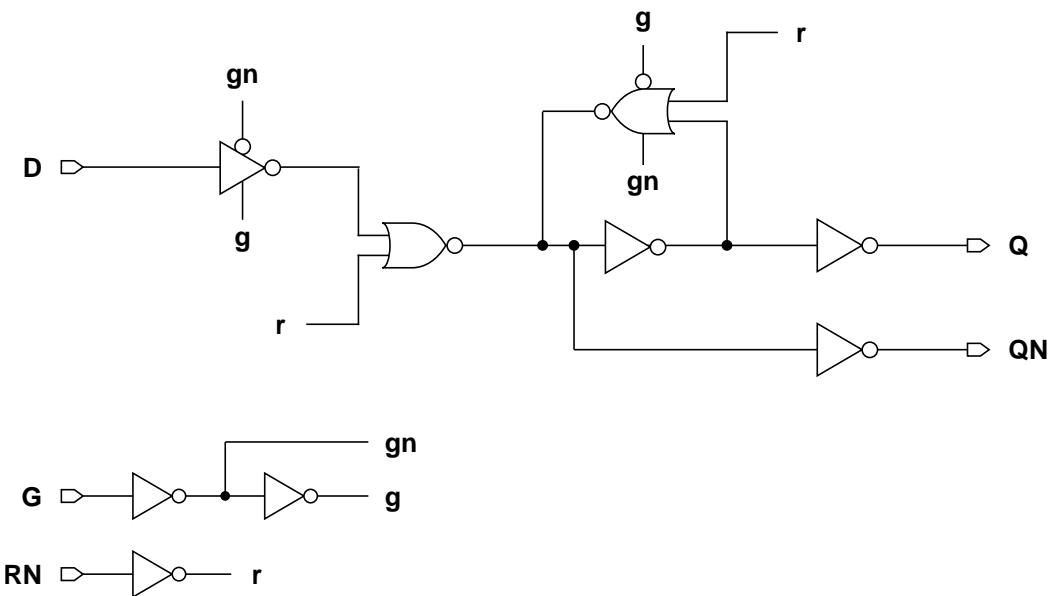
Functions

| RN | G | D | Q[n+1] | QN[n+1] |
|----|---|---|--------|---------|
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | x | Q[n] | QN[n] |
| 0 | x | x | 0 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TLATRXL | 5.04 | 8.58 |
| TLATRX1 | 5.04 | 8.58 |
| TLATRX2 | 5.04 | 9.24 |
| TLATRX4 | 5.04 | 11.88 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0034 | 0.0041 | 0.0072 | 0.0145 |
| G | 0.0275 | 0.0280 | 0.0320 | 0.0557 |
| RN | 0.0046 | 0.0046 | 0.0058 | 0.0075 |
| Q | 0.0384 | 0.0457 | 0.0768 | 0.1342 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0028 | 0.0033 | 0.0054 | 0.0105 |
| G | 0.0023 | 0.0024 | 0.0027 | 0.0041 |
| RN | 0.0043 | 0.0044 | 0.0055 | 0.0076 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1460 | 0.1371 | 0.1242 | 0.1205 | 5.9359 | 4.2223 | 2.1389 | 1.0458 |
| D → Q↓ | 0.2245 | 0.2175 | 0.1960 | 0.1820 | 3.7389 | 2.6307 | 1.3324 | 0.6636 |
| G → Q↑ | 0.2490 | 0.2369 | 0.2318 | 0.2317 | 5.9345 | 4.2218 | 2.1386 | 1.0457 |
| G → Q↓ | 0.2287 | 0.2224 | 0.2079 | 0.1913 | 3.7368 | 2.6299 | 1.3326 | 0.6647 |
| RN → Q↑ | 0.1425 | 0.1320 | 0.1170 | 0.1116 | 5.9357 | 4.2222 | 2.1388 | 1.0458 |
| RN → Q↓ | 0.1494 | 0.1678 | 0.2500 | 0.4035 | 3.6134 | 2.6177 | 1.3940 | 0.7615 |
| D → QN↑ | 0.2832 | 0.2805 | 0.2719 | 0.2587 | 5.8950 | 4.2059 | 2.1292 | 1.0409 |
| D → QN↓ | 0.2292 | 0.2264 | 0.2250 | 0.2196 | 3.5243 | 2.5502 | 1.3015 | 0.6510 |
| G → QN↑ | 0.2890 | 0.2870 | 0.2850 | 0.2696 | 5.8952 | 4.2060 | 2.1292 | 1.0409 |
| G → QN↓ | 0.3336 | 0.3275 | 0.3336 | 0.3317 | 3.5266 | 2.5512 | 1.3020 | 0.6511 |
| RN → QN↑ | 0.2090 | 0.2302 | 0.3298 | 0.4998 | 5.8930 | 4.2058 | 2.1291 | 1.0407 |
| RN → QN↓ | 0.2262 | 0.2218 | 0.2182 | 0.2110 | 3.5252 | 2.5507 | 1.3017 | 0.6510 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → G | 0.0352 | 0.0312 | 0.0039 | 0.0000 |
| | setup↓ → G | 0.1719 | 0.1680 | 0.1445 | 0.1289 |
| | hold↑ → G | -0.0117 | -0.0039 | 0.0117 | 0.0156 |
| | hold↓ → G | -0.1680 | -0.1602 | -0.1367 | -0.1250 |
| G | minpwh | 0.1807 | 0.1759 | 0.1613 | 0.1467 |
| RN | minpwl | 0.1467 | 0.1613 | 0.2244 | 0.3362 |
| | recovery | 0.0273 | 0.0156 | -0.0078 | -0.0156 |

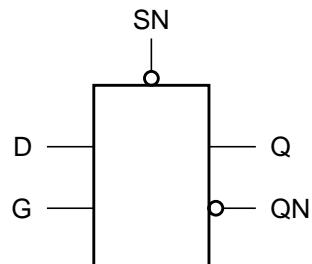
Cell Description

The TLATS cell is an active-high D-type transparent latch with asynchronous active-low set (SN). When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

| SN | G | D | Q[n+1] | QN[n+1] |
|----|---|---|--------|---------|
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | x | Q[n] | QN[n] |
| 0 | x | x | 1 | 0 |

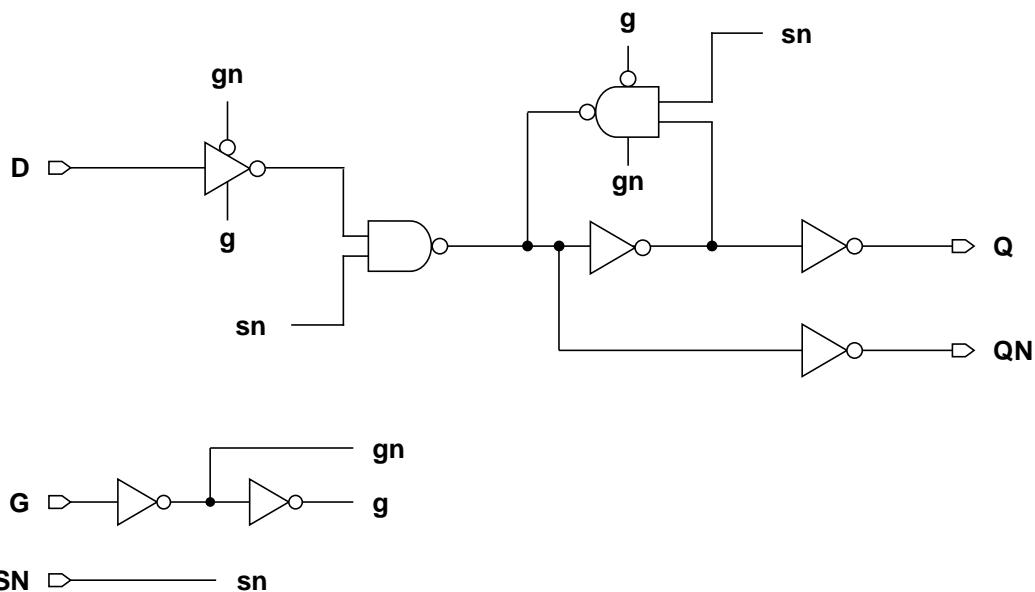
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TLATSLX | 5.04 | 10.56 |
| TLATSX1 | 5.04 | 10.56 |
| TLATSX2 | 5.04 | 11.22 |
| TLATSX4 | 5.04 | 13.86 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0040 | 0.0048 | 0.0078 | 0.0141 |
| G | 0.0293 | 0.0299 | 0.0325 | 0.0418 |
| SN | 0.0149 | 0.0151 | 0.0160 | 0.0225 |
| Q | 0.0474 | 0.0536 | 0.0847 | 0.1395 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0029 | 0.0033 | 0.0053 | 0.0096 |
| G | 0.0024 | 0.0029 | 0.0030 | 0.0042 |
| SN | 0.0022 | 0.0022 | 0.0027 | 0.0039 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1494 | 0.1385 | 0.1241 | 0.1196 | 5.9421 | 4.2258 | 2.1377 | 1.0458 |
| D → Q↓ | 0.2910 | 0.2818 | 0.2557 | 0.2371 | 3.7658 | 2.8835 | 1.3704 | 0.6813 |
| G → Q↑ | 0.2633 | 0.2506 | 0.2363 | 0.2185 | 5.9405 | 4.2251 | 2.1373 | 1.0455 |
| G → Q↓ | 0.2640 | 0.2514 | 0.2382 | 0.2212 | 3.7643 | 2.8829 | 1.3696 | 0.6810 |
| SN → Q↑ | 0.2014 | 0.2133 | 0.2488 | 0.3397 | 5.8988 | 4.2125 | 2.1403 | 1.0553 |
| SN → Q↓ | 0.3259 | 0.3157 | 0.2820 | 0.2614 | 3.7658 | 2.8837 | 1.3704 | 0.6813 |
| D → QN↑ | 0.3731 | 0.3536 | 0.3334 | 0.3160 | 5.8929 | 4.2056 | 2.1298 | 1.0410 |
| D → QN↓ | 0.2493 | 0.2508 | 0.2291 | 0.2184 | 3.2948 | 2.5607 | 1.3039 | 0.6510 |
| G → QN↑ | 0.3475 | 0.3247 | 0.3167 | 0.3004 | 5.8938 | 4.2060 | 2.1300 | 1.0410 |
| G → QN↓ | 0.3645 | 0.3643 | 0.3423 | 0.3179 | 3.2949 | 2.5606 | 1.3039 | 0.6510 |
| SN → QN↑ | 0.4084 | 0.3879 | 0.3600 | 0.3405 | 5.8933 | 4.2058 | 2.1298 | 1.0410 |
| SN → QN↓ | 0.3003 | 0.3244 | 0.3580 | 0.4500 | 3.2891 | 2.5595 | 1.3042 | 0.6521 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → G | 0.0195 | 0.0312 | -0.0078 | -0.0039 |
| | setup↓ → G | 0.2383 | 0.2266 | 0.1914 | 0.1719 |
| | hold↑ → G | -0.0078 | -0.0195 | 0.0156 | 0.0156 |
| | hold↓ → G | -0.2266 | -0.2148 | -0.1797 | -0.1641 |
| G | minpwh | 0.2196 | 0.2050 | 0.1807 | 0.1661 |
| SN | minpwl | 0.1710 | 0.1759 | 0.1953 | 0.2439 |
| | recovery | 0.2734 | 0.2578 | 0.2148 | 0.1992 |

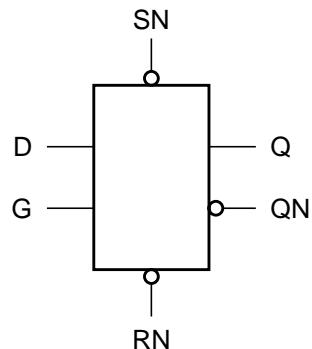
Cell Description

The TLATSR cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and reset(RN), and set dominating reset. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

| RN | SN | G | D | Q[n+1] | QN[n+1] |
|----|----|---|---|--------|---------|
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | x | Q[n] | QN[n] |
| 0 | 1 | x | x | 0 | 1 |
| 1 | 0 | x | x | 1 | 0 |
| 0 | 0 | x | x | 1 | 0 |

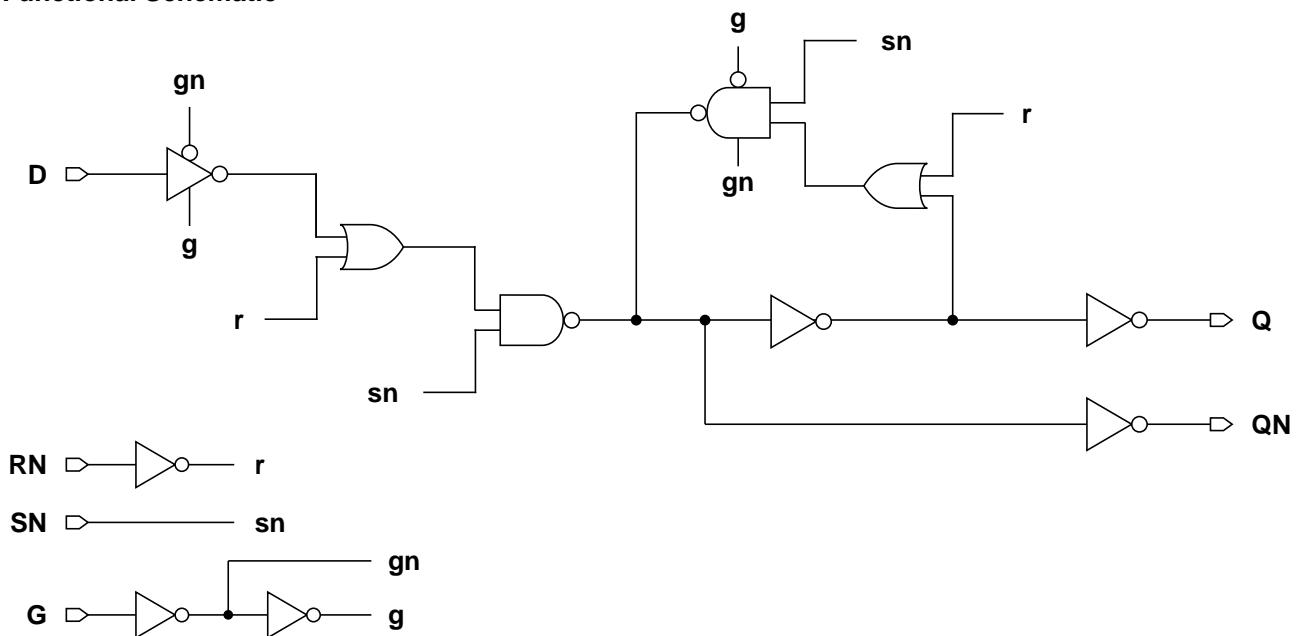
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| TLATSRXL | 5.04 | 11.22 |
| TLATSRX1 | 5.04 | 11.22 |
| TLATSRX2 | 5.04 | 11.88 |
| TLATSRX4 | 5.04 | 16.50 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0037 | 0.0045 | 0.0076 | 0.0157 |
| G | 0.0306 | 0.0312 | 0.0337 | 0.0577 |
| SN | 0.0165 | 0.0185 | 0.0249 | 0.0451 |
| RN | 0.0048 | 0.0056 | 0.0093 | 0.0178 |
| Q | 0.0571 | 0.0657 | 0.1031 | 0.1795 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0030 | 0.0035 | 0.0054 | 0.0115 |
| G | 0.0023 | 0.0028 | 0.0031 | 0.0044 |
| SN | 0.0023 | 0.0028 | 0.0041 | 0.0071 |
| RN | 0.0042 | 0.0047 | 0.0065 | 0.0116 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1948 | 0.1830 | 0.1810 | 0.1678 | 5.9895 | 4.2442 | 2.1483 | 1.0498 |
| D → Q↓ | 0.3429 | 0.3357 | 0.3069 | 0.2865 | 4.2046 | 2.9041 | 1.4225 | 0.7052 |
| G → Q↑ | 0.2950 | 0.2763 | 0.2760 | 0.2539 | 5.9881 | 4.2437 | 2.1480 | 1.0496 |
| G → Q↓ | 0.3393 | 0.3241 | 0.2942 | 0.2695 | 4.2070 | 2.9046 | 1.4225 | 0.7052 |
| SN → Q↑ | 0.2330 | 0.2169 | 0.1883 | 0.1836 | 5.9209 | 4.2203 | 2.1362 | 1.0447 |
| SN → Q↓ | 0.3744 | 0.3609 | 0.3237 | 0.3053 | 4.1875 | 2.8965 | 1.4184 | 0.7031 |
| RN → Q↑ | 0.1893 | 0.1775 | 0.1757 | 0.1630 | 5.9896 | 4.2443 | 2.1483 | 1.0498 |
| RN → Q↓ | 0.2533 | 0.2460 | 0.2177 | 0.2007 | 4.0930 | 2.8713 | 1.4044 | 0.6981 |
| D → QN↑ | 0.4251 | 0.4119 | 0.3882 | 0.3662 | 5.8950 | 4.2063 | 2.1298 | 1.0409 |
| D → QN↓ | 0.3001 | 0.3003 | 0.2892 | 0.2689 | 3.5440 | 2.5637 | 1.3036 | 0.6513 |
| G → QN↑ | 0.4234 | 0.4022 | 0.3768 | 0.3498 | 5.8957 | 4.2067 | 2.1299 | 1.0410 |
| G → QN↓ | 0.4018 | 0.3951 | 0.3853 | 0.3556 | 3.5464 | 2.5647 | 1.3039 | 0.6514 |
| SN → QN↑ | 0.4565 | 0.4371 | 0.4045 | 0.3843 | 5.8959 | 4.2068 | 2.1300 | 1.0410 |
| SN → QN↓ | 0.3367 | 0.3317 | 0.2938 | 0.2827 | 3.5353 | 2.5613 | 1.3026 | 0.6509 |
| RN → QN↑ | 0.3337 | 0.3187 | 0.2941 | 0.2747 | 5.8922 | 4.2071 | 2.1303 | 1.0412 |
| RN → QN↓ | 0.2951 | 0.2954 | 0.2843 | 0.2643 | 3.5451 | 2.5641 | 1.3037 | 0.6514 |

Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → G | 0.0820 | 0.0938 | 0.0625 | 0.0430 |
| | setup↓ → G | 0.2812 | 0.2734 | 0.2422 | 0.2188 |
| | hold↑ → G | -0.0508 | -0.0625 | -0.0391 | -0.0234 |
| | hold↓ → G | -0.2695 | -0.2617 | -0.2305 | -0.2070 |
| G | minpwh | 0.2827 | 0.2682 | 0.2390 | 0.2099 |
| SN | minpwl | 0.2001 | 0.1807 | 0.1516 | 0.1370 |
| | recovery | 0.3086 | 0.2969 | 0.2578 | 0.2383 |
| | removal | -0.3086 | -0.2969 | -0.2539 | -0.2344 |
| RN | minpwl | 0.2536 | 0.2293 | 0.1856 | 0.1516 |
| | recovery | 0.0703 | 0.0781 | 0.0508 | 0.0273 |
| | removal | -0.0703 | -0.0781 | -0.0469 | -0.0273 |

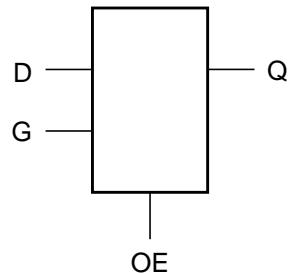
Cell Description

The TTLAT cell is an active-high D-type transparent latch with active-high output enable (OE). When the enable (G) is high and the output enable (OE) is high, data is transferred to the output (Q).

Functions

| OE | G | D | Q[n+1] |
|----|---|---|--------|
| 0 | x | x | Z |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 0 | x | Q[n] |

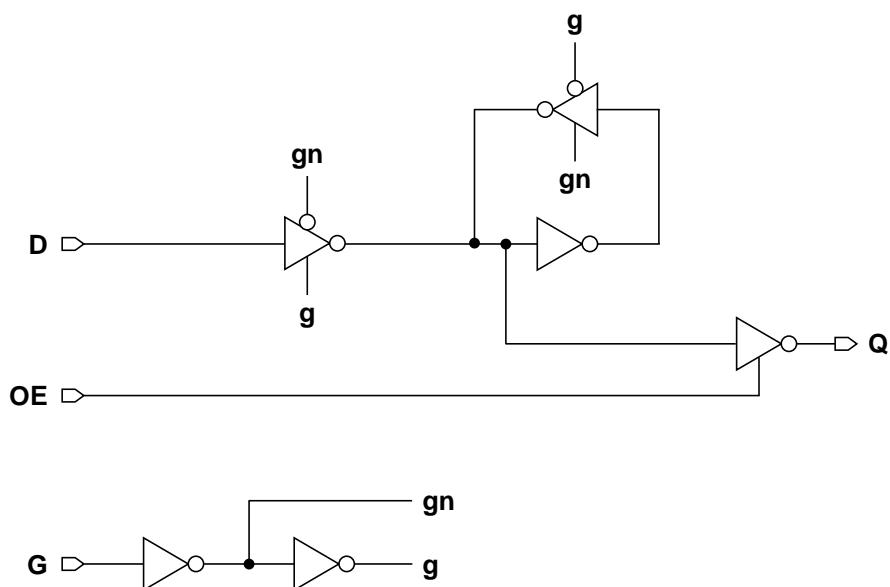
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| TTLATXL | 5.04 | 8.58 |
| TTLATX1 | 5.04 | 8.58 |
| TTLATX2 | 5.04 | 12.54 |
| TTLATX4 | 5.04 | 15.18 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | | | |
|-----|----------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0050 | 0.0095 | 0.0177 | 0.0177 |
| G | 0.0256 | 0.0271 | 0.0420 | 0.0561 |
| OE | 0.0374 | 0.0663 | 0.1206 | 0.1926 |
| Q | 0.0359 | 0.0620 | 0.1111 | 0.1783 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| D | 0.0036 | 0.0063 | 0.0118 | 0.0119 |
| G | 0.0024 | 0.0029 | 0.0043 | 0.0071 |
| OE | 0.0031 | 0.0037 | 0.0061 | 0.0105 |
| Q | 0.0018 | 0.0043 | 0.0061 | 0.0112 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|--------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| D → Q↑ | 0.1281 | 0.1156 | 0.1163 | 0.1286 | 8.0453 | 2.5723 | 1.3426 | 0.6920 |
| D → Q↓ | 0.1817 | 0.1587 | 0.1545 | 0.1874 | 5.4007 | 1.7311 | 0.8584 | 0.4807 |
| G → Q↑ | 0.2285 | 0.2139 | 0.2130 | 0.1951 | 8.0510 | 2.5730 | 1.3431 | 0.6923 |
| G → Q↓ | 0.2002 | 0.1738 | 0.1684 | 0.1949 | 5.3956 | 1.7299 | 0.8578 | 0.4805 |
| OE → Q↑ | 0.0294 | 0.0255 | 0.0203 | 0.0252 | 7.9506 | 2.5217 | 1.3188 | 0.6809 |
| OE → Q↓ | 0.0170 | 0.0169 | 0.0138 | 0.0164 | 5.3027 | 1.6870 | 0.8374 | 0.4665 |

Timing Constraints at 25°C, 1.8V, Typical Process

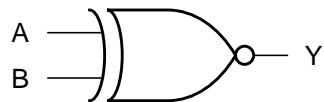
| Pin | Requirement | Interval (ns) | | | |
|-----|-------------|---------------|---------|---------|---------|
| | | XL | X1 | X2 | X4 |
| D | setup↑ → G | -0.0156 | -0.0195 | -0.0234 | 0.0117 |
| | setup↓ → G | 0.1055 | 0.0859 | 0.0820 | 0.1211 |
| | hold↑ → G | 0.0312 | 0.0312 | 0.0352 | 0.0000 |
| | hold↓ → G | -0.0859 | -0.0703 | -0.0664 | -0.1016 |
| G | minpwh | 0.1321 | 0.1078 | 0.1030 | 0.1321 |

Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B) + (\bar{A} \bullet \bar{B})$$

Logic Symbol



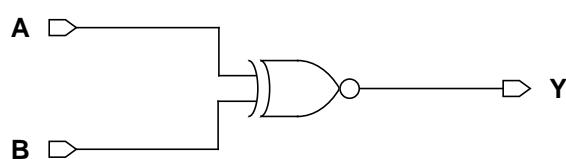
Functions

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| XNOR2XL | 5.04 | 5.28 |
| XNOR2X1 | 5.04 | 5.28 |
| XNOR2X2 | 5.04 | 7.26 |
| XNOR2X4 | 5.04 | 11.22 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0383 | 0.0404 | 0.0704 | 0.1270 |
| B | 0.0429 | 0.0568 | 0.1096 | 0.2096 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0065 | 0.0062 | 0.0094 | 0.0162 |
| B | 0.0023 | 0.0068 | 0.0147 | 0.0277 |

Delays at 25°C, 1.8V, Typical Process

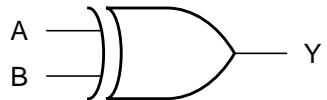
| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A → Y↑ | 0.1382 | 0.1328 | 0.1394 | 0.1238 | 5.9034 | 4.2063 | 2.1299 | 1.1309 |
| A → Y↓ | 0.1320 | 0.1151 | 0.1070 | 0.1043 | 3.6872 | 2.5676 | 1.3048 | 0.6073 |
| B → Y↑ | 0.1968 | 0.1317 | 0.1197 | 0.1197 | 5.9064 | 4.2066 | 2.1301 | 1.1310 |
| B → Y↓ | 0.2062 | 0.1470 | 0.1358 | 0.1319 | 3.6638 | 2.5745 | 1.3101 | 0.6096 |

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet \bar{B}) + (\bar{A} \bullet B)$$

Logic Symbol



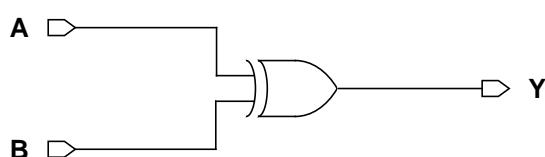
Functions

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| XOR2XL | 5.04 | 5.28 |
| XOR2X1 | 5.04 | 5.28 |
| XOR2X2 | 5.04 | 6.60 |
| XOR2X4 | 5.04 | 11.22 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | | |
|-----|------------------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0372 | 0.0375 | 0.0650 | 0.1155 |
| B | 0.0401 | 0.0537 | 0.1033 | 0.2012 |

Pin Capacitance

| Pin | Capacitance (pF) | | | |
|-----|------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 |
| A | 0.0066 | 0.0061 | 0.0093 | 0.0171 |
| B | 0.0024 | 0.0067 | 0.0147 | 0.0278 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | | K_{load} (ns/pF) | | | |
|-------------|----------------------|--------|--------|--------|---------------------------|--------|--------|--------|
| | XL | X1 | X2 | X4 | XL | X1 | X2 | X4 |
| A → Y↑ | 0.1373 | 0.1221 | 0.1283 | 0.1096 | 5.9050 | 4.2016 | 2.1279 | 1.1296 |
| A → Y↓ | 0.1337 | 0.1206 | 0.1227 | 0.1131 | 3.4020 | 2.5741 | 1.3095 | 0.6087 |
| B → Y↑ | 0.1901 | 0.1290 | 0.1187 | 0.1140 | 5.9029 | 4.2058 | 2.1302 | 1.1306 |
| B → Y↓ | 0.1973 | 0.1475 | 0.1385 | 0.1337 | 3.4025 | 2.5743 | 1.3094 | 0.6087 |

Synthesis Optimized Arithmetic Cells

Cell Description

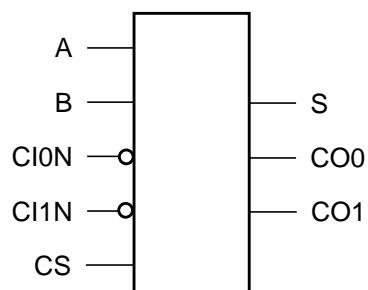
The AFCSHCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carry-outs (CO0, CO1) of the operands (A, B) with active-low carry-ins (CI0N, CI1N). The three outputs (S, CO0, CO1) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus \overline{CI1N}) + \overline{CS} \bullet (A \oplus B \oplus \overline{CI0N})$$

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol



Cell Size

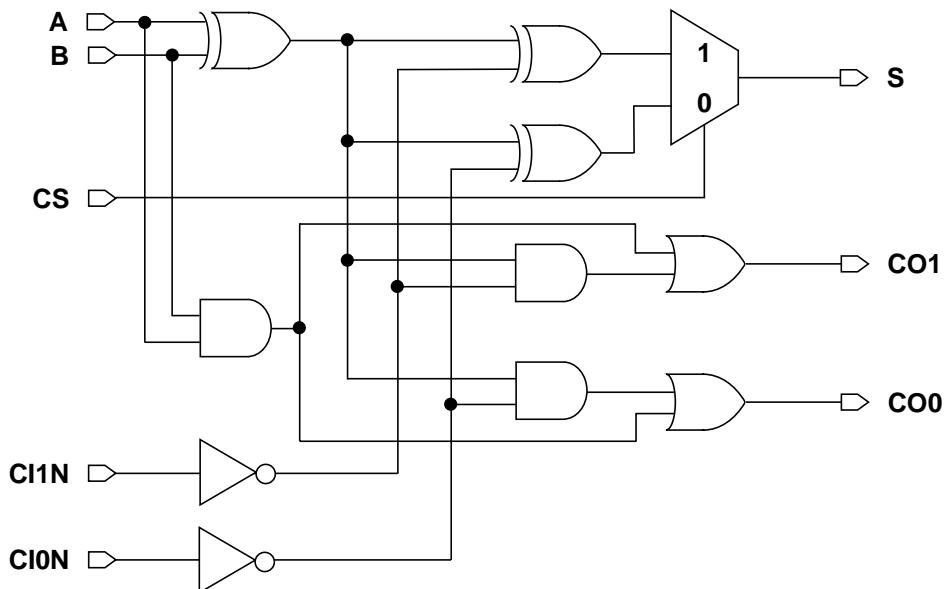
| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AFCSHCINX2 | 5.04 | 33.00 |
| AFCSHCINX4 | 5.04 | 38.28 |

Functions

| A | B | CI0N | CI1N | CS | S | CO0 | CO1 |
|---|---|------|------|----|---|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| A | B | CI0N | CI1N | CS | S | CO0 | CO1 |
|---|---|------|------|----|---|-----|-----|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|------|------------------------------------|--------|
| | X2 | X4 |
| CS | 0.0685 | 0.0687 |
| A | 0.3539 | 0.3938 |
| B | 0.3203 | 0.3608 |
| CI0N | 0.1392 | 0.1723 |
| CI1N | 0.1410 | 0.1736 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|------|------------------|--------|
| | X2 | X4 |
| CS | 0.0058 | 0.0058 |
| A | 0.0078 | 0.0078 |
| B | 0.0174 | 0.0174 |
| CI0N | 0.0091 | 0.0151 |
| CI1N | 0.0089 | 0.0149 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|--------------------|-----------------------------|-----------|---------------------------------|-----------|
| | X2 | X4 | X2 | X4 |
| CS → S↑ | 0.1406 | 0.1415 | 2.1308 | 2.1261 |
| CS → S↓ | 0.1247 | 0.1278 | 1.3120 | 1.2915 |
| A → S↑ | 0.4345 | 0.4633 | 2.1317 | 2.1265 |
| A → S↓ | 0.4054 | 0.4282 | 1.3143 | 1.2922 |
| B → S↑ | 0.3574 | 0.3815 | 2.1317 | 2.1265 |
| B → S↓ | 0.3458 | 0.3740 | 1.3146 | 1.2926 |
| CI0N → S↑ | 0.2705 | 0.2770 | 2.1317 | 2.1265 |
| CI0N → S↓ | 0.2856 | 0.2913 | 1.3147 | 1.2924 |
| CI1N → S↑ | 0.2435 | 0.2405 | 2.1310 | 2.1261 |
| CI1N → S↓ | 0.2697 | 0.2657 | 1.3123 | 1.2916 |
| A → CO0↑ | 0.2131 | 0.2444 | 2.8845 | 2.8349 |
| A → CO0↓ | 0.2518 | 0.3036 | 1.6691 | 1.6396 |
| B → CO0↑ | 0.1673 | 0.1967 | 2.8137 | 2.8278 |
| B → CO0↓ | 0.1901 | 0.2324 | 1.6469 | 1.6320 |
| CI0N → CO0↑ | 0.0791 | 0.0619 | 2.9110 | 1.4595 |
| CI0N → CO0↓ | 0.0478 | 0.0399 | 1.6131 | 0.8162 |
| A → CO1↑ | 0.2073 | 0.2531 | 2.7984 | 2.5740 |
| A → CO1↓ | 0.2674 | 0.3162 | 1.6892 | 1.6642 |
| B → CO1↑ | 0.1426 | 0.1850 | 2.8156 | 2.5632 |
| B → CO1↓ | 0.1892 | 0.2358 | 1.6773 | 1.6564 |
| CI1N → CO1↑ | 0.0748 | 0.0586 | 2.8556 | 1.4253 |
| CI1N → CO1↓ | 0.0473 | 0.0392 | 1.6344 | 0.8165 |

Cell Description

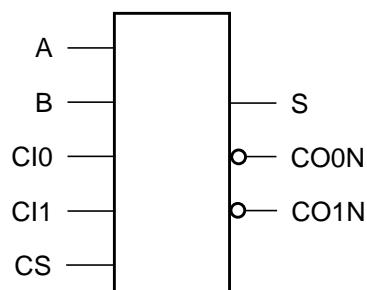
The AFCSHCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carry-outs (CO0N, CO1N) of two operands (A, B) with carry-ins (CI0, CI1). The three outputs (S, CO0N, CO1N) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus CI1) + \overline{CS} \bullet (A \oplus B \oplus CI0)$$

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol



Cell Size

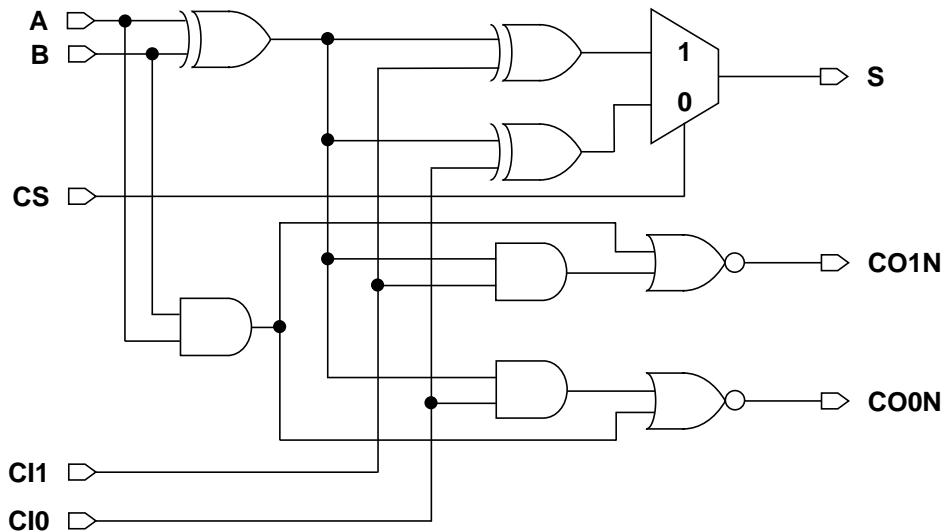
| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AFCSHCONX2 | 5.04 | 33.66 |
| AFCSHCONX4 | 5.04 | 38.94 |

Functions

| A | B | CI0 | CI1 | CS | S | CO0N | CO1N |
|---|---|-----|-----|----|---|------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

| A | B | CI0 | CI1 | CS | S | CO0N | CO1N |
|---|---|-----|-----|----|---|------|------|
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| CS | 0.0686 | 0.0687 |
| A | 0.3628 | 0.4025 |
| B | 0.3398 | 0.3850 |
| CI0 | 0.1629 | 0.2125 |
| CI1 | 0.1391 | 0.1854 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| CS | 0.0095 | 0.0095 |
| A | 0.0139 | 0.0139 |
| B | 0.0160 | 0.0160 |
| CI0 | 0.0132 | 0.0259 |
| CI1 | 0.0128 | 0.0258 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|--------------------|-----------------------------|-----------|---------------------------------|-----------|
| | X2 | X4 | X2 | X4 |
| CS → S↑ | 0.1412 | 0.1418 | 2.1309 | 2.1263 |
| CS → S↓ | 0.1244 | 0.1276 | 1.3116 | 1.2915 |
| A → S↑ | 0.4663 | 0.5110 | 2.1318 | 2.1266 |
| A → S↓ | 0.4167 | 0.4525 | 1.3138 | 1.2928 |
| B → S↑ | 0.4168 | 0.4590 | 2.1318 | 2.1266 |
| B → S↓ | 0.3854 | 0.4098 | 1.3138 | 1.2923 |
| Cl0 → S↑ | 0.2674 | 0.2611 | 2.1318 | 2.1266 |
| Cl0 → S↓ | 0.2659 | 0.2546 | 1.3139 | 1.2925 |
| Cl1 → S↑ | 0.2256 | 0.2163 | 2.1310 | 2.1261 |
| Cl1 → S↓ | 0.2358 | 0.2248 | 1.3118 | 1.2916 |
| A → CO0N↑ | 0.2669 | 0.3146 | 2.5067 | 2.5263 |
| A → CO0N↓ | 0.2599 | 0.3176 | 1.7007 | 1.6675 |
| B → CO0N↑ | 0.2258 | 0.2825 | 2.7634 | 2.5251 |
| B → CO0N↓ | 0.2111 | 0.2625 | 1.6918 | 1.6668 |
| Cl0 → CO0N↑ | 0.0678 | 0.0575 | 2.8374 | 1.5092 |
| Cl0 → CO0N↓ | 0.0492 | 0.0398 | 1.7834 | 0.9112 |
| A → CO1N↑ | 0.2736 | 0.3219 | 2.7970 | 2.8653 |
| A → CO1N↓ | 0.2574 | 0.3194 | 1.6887 | 1.6783 |
| B → CO1N↑ | 0.2424 | 0.2900 | 2.7975 | 2.8652 |
| B → CO1N↓ | 0.2050 | 0.2649 | 1.6889 | 1.6780 |
| Cl1 → CO1N↑ | 0.0634 | 0.0530 | 2.8301 | 1.4397 |
| Cl1 → CO1N↓ | 0.0464 | 0.0361 | 1.7845 | 0.8293 |

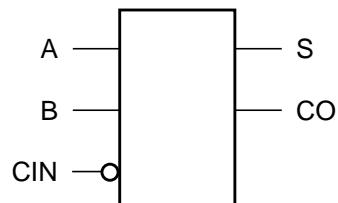
Cell Description

The AFHCIN cell is a full adder that provides the arithmetic sum (S) and carry-out (CO) of two operands (A, B) with active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus \overline{CIN}$$

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol



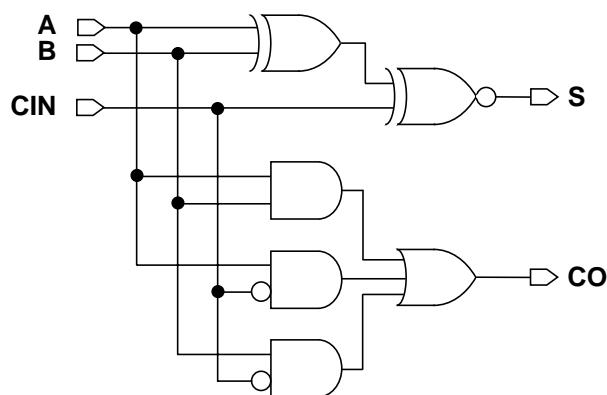
Functions

| A | B | CIN | S | CO |
|---|---|-----|---|----|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AFHCINX2 | 5.04 | 16.50 |
| AFHCINX4 | 5.04 | 18.48 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| A | 0.1816 | 0.2034 |
| B | 0.1894 | 0.2090 |
| CIN | 0.1275 | 0.1789 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| A | 0.0073 | 0.0073 |
| B | 0.0179 | 0.0158 |
| CIN | 0.0138 | 0.0271 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|-------------|----------------------|--------|---------------------------|--------|
| | X2 | X4 | X2 | X4 |
| A → S↑ | 0.2341 | 0.2497 | 2.6485 | 2.1260 |
| A → S↓ | 0.2759 | 0.2974 | 1.4240 | 1.2909 |
| B → S↑ | 0.2057 | 0.2212 | 2.6493 | 2.1264 |
| B → S↓ | 0.2069 | 0.2258 | 1.4230 | 1.2904 |
| CIN → S↑ | 0.1361 | 0.1217 | 2.6483 | 2.1258 |
| CIN → S↓ | 0.1465 | 0.1463 | 1.4276 | 1.2921 |
| A → CO↑ | 0.1649 | 0.1894 | 2.8493 | 2.8413 |
| A → CO↓ | 0.2012 | 0.2342 | 1.9066 | 1.8841 |
| B → CO↑ | 0.1249 | 0.1455 | 2.8315 | 2.8329 |
| B → CO↓ | 0.1674 | 0.1969 | 1.8878 | 1.8765 |
| CIN → CO↑ | 0.0483 | 0.0424 | 2.5961 | 1.3035 |
| CIN → CO↓ | 0.0413 | 0.0399 | 1.6620 | 0.8364 |

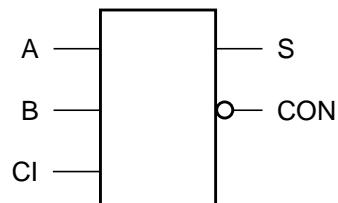
Cell Description

The AFHCON cell is a full adder that provides the arithmetic sum (S) and active-low carry-out (CON) of two operands (A, B) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus B \oplus CI$$

$$CON = \overline{(A \bullet B)} + (A \bullet CI) + (B \bullet CI)$$

Logic Symbol



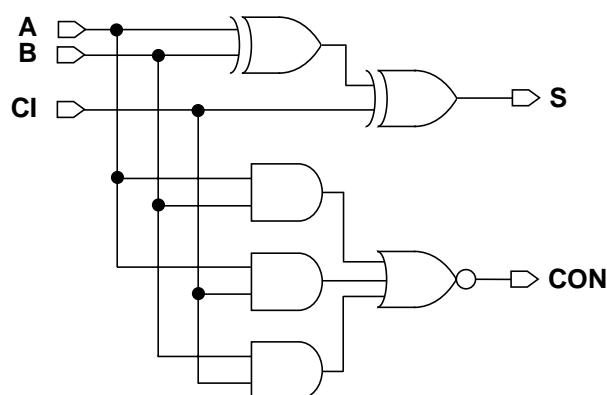
Functions

| A | B | CI | S | CON |
|---|---|----|---|-----|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AFHCONX2 | 5.04 | 15.84 |
| AFHCONX4 | 5.04 | 17.16 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| A | 0.1810 | 0.2047 |
| B | 0.1730 | 0.1938 |
| Cl | 0.1187 | 0.1737 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| A | 0.0073 | 0.0073 |
| B | 0.0218 | 0.0228 |
| Cl | 0.0138 | 0.0276 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|-------------|----------------------|--------|---------------------------|--------|
| | X2 | X4 | X2 | X4 |
| A → S↑ | 0.2257 | 0.2411 | 2.6477 | 2.6443 |
| A → S↓ | 0.2606 | 0.2755 | 1.6508 | 1.6398 |
| B → S↑ | 0.1591 | 0.1663 | 2.6477 | 2.6433 |
| B → S↓ | 0.1805 | 0.1979 | 1.6516 | 1.6396 |
| Cl → S↑ | 0.1302 | 0.1202 | 2.6462 | 2.6440 |
| Cl → S↓ | 0.1417 | 0.1475 | 1.6525 | 1.6401 |
| A → CON↑ | 0.2107 | 0.2334 | 2.9289 | 2.8118 |
| A → CON↓ | 0.1748 | 0.2046 | 1.9523 | 1.8658 |
| B → CON↑ | 0.1386 | 0.1590 | 2.9657 | 2.8305 |
| B → CON↓ | 0.1115 | 0.1377 | 1.9687 | 1.8759 |
| Cl → CON↑ | 0.0590 | 0.0480 | 2.5910 | 1.2757 |
| Cl → CON↓ | 0.0428 | 0.0379 | 1.6580 | 0.8302 |

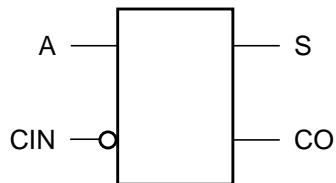
Cell Description

The AHHCIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus \overline{CIN}$$

$$CO = A \bullet \overline{CIN}$$

Logic Symbol



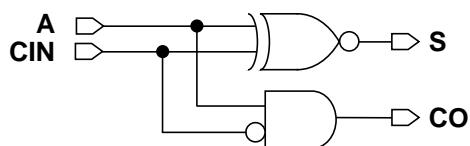
Functions

| A | CIN | S | CO |
|---|-----|---|----|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AHHCINX2 | 5.04 | 7.92 |
| AHHCINX4 | 5.04 | 9.24 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| A | 0.0908 | 0.1102 |
| CIN | 0.0778 | 0.1046 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| A | 0.0084 | 0.0105 |
| CIN | 0.0160 | 0.0215 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|-------------|----------------------|--------|---------------------------|--------|
| | X2 | X4 | X2 | X4 |
| A → S↑ | 0.0876 | 0.0862 | 3.0572 | 3.0633 |
| A → S↓ | 0.0926 | 0.0848 | 1.9076 | 1.9461 |
| CIN → S↑ | 0.0516 | 0.0512 | 3.0577 | 3.0627 |
| CIN → S↓ | 0.0669 | 0.0636 | 1.9362 | 1.9562 |
| A → CO↑ | 0.0766 | 0.0730 | 4.5292 | 2.2646 |
| A → CO↓ | 0.0958 | 0.0897 | 1.7120 | 0.8556 |
| CIN → CO↑ | 0.0493 | 0.0480 | 4.5268 | 2.2637 |
| CIN → CO↓ | 0.0249 | 0.0242 | 1.7033 | 0.8518 |

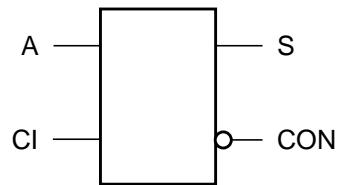
Cell Description

The AHHCON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus CI$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol



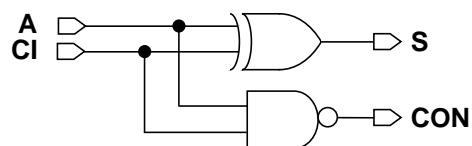
Functions

| A | CI | S | CON |
|---|----|---|-----|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| AHHCONX2 | 5.04 | 7.26 |
| AHHCONX4 | 5.04 | 8.58 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| A | 0.0965 | 0.1238 |
| Cl | 0.0605 | 0.0772 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| A | 0.0123 | 0.0187 |
| Cl | 0.0174 | 0.0235 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|-------------|----------------------|--------|--------------------|--------|
| | X2 | X4 | X2 | X4 |
| A → S↑ | 0.0936 | 0.0943 | 3.0715 | 3.0693 |
| A → S↓ | 0.1035 | 0.1035 | 1.9773 | 1.9744 |
| Cl → S↑ | 0.0540 | 0.0527 | 3.0582 | 3.0636 |
| Cl → S↓ | 0.0661 | 0.0620 | 1.9339 | 1.9557 |
| A → CON↑ | 0.0356 | 0.0362 | 2.7612 | 1.3809 |
| A → CON↓ | 0.0262 | 0.0249 | 2.1774 | 1.0051 |
| Cl → CON↑ | 0.0289 | 0.0278 | 2.7628 | 1.3815 |
| Cl → CON↓ | 0.0230 | 0.0208 | 2.1776 | 1.0049 |

Cell Description

The booth encoder block, BENC, cell performs a 2-bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (M0, M1, M2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction. The outputs (S, A, X2) are represented by the logic equations:

$$S = \overline{M2} \bullet (M1 + M0)$$

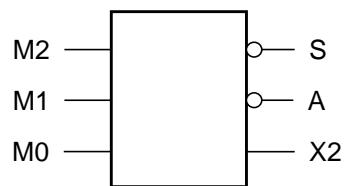
$$A = M2 \bullet (\overline{M1} + \overline{M0})$$

$$X2 = M1 \oplus M0$$

Functions

| M2 | M1 | M0 | X2 | A | S |
|----|----|----|----|---|---|
| 0 | 0 | 0 | x | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | x | 1 | 1 |

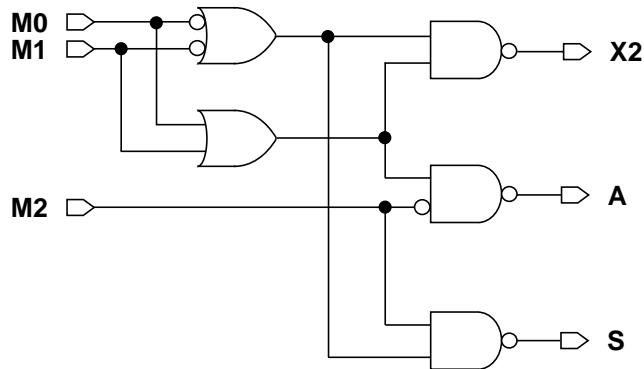
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| BENCX1 | 5.04 | 20.46 |
| BENCX2 | 5.04 | 27.06 |
| BENCX4 | 5.04 | 40.26 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | |
|-----|------------------------------------|--------|--------|
| | X1 | X2 | X4 |
| M2 | 0.0817 | 0.1469 | 0.2740 |
| M1 | 0.1680 | 0.2934 | 0.5995 |
| M0 | 0.1852 | 0.3146 | 0.6277 |

Pin Capacitance

| Pin | Capacitance (pF) | | |
|-----|------------------|--------|--------|
| | X1 | X2 | X4 |
| M2 | 0.0078 | 0.0099 | 0.0157 |
| M1 | 0.0107 | 0.0176 | 0.0310 |
| M0 | 0.0095 | 0.0158 | 0.0248 |

Delays at 25°C, 1.8V, Typical Process

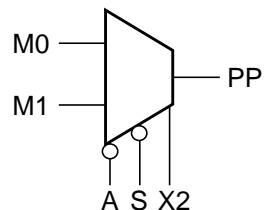
| Description | Intrinsic Delay (ns) | | | K_{load} (ns/pF) | | |
|--------------------|-----------------------------|-----------|-----------|---------------------------------|-----------|-----------|
| | X1 | X2 | X4 | X1 | X2 | X4 |
| M2 → A↑ | 0.2158 | 0.2216 | 0.2125 | 1.0515 | 0.5342 | 0.2644 |
| M2 → A↓ | 0.1961 | 0.2081 | 0.2155 | 0.6941 | 0.3457 | 0.1717 |
| M1 → A↑ | 0.2334 | 0.2160 | 0.1956 | 1.0512 | 0.5340 | 0.2643 |
| M1 → A↓ | 0.1735 | 0.1708 | 0.1858 | 0.6950 | 0.3462 | 0.1719 |
| M0 → A↑ | 0.2259 | 0.2060 | 0.1839 | 1.0511 | 0.5339 | 0.2643 |
| M0 → A↓ | 0.1660 | 0.1611 | 0.1712 | 0.6948 | 0.3460 | 0.1719 |
| M2 → S↑ | 0.1676 | 0.1697 | 0.1629 | 1.1124 | 0.5339 | 0.2628 |
| M2 → S↓ | 0.1336 | 0.1267 | 0.1368 | 0.6906 | 0.3445 | 0.1640 |
| M1 → S↑ | 0.2935 | 0.2639 | 0.2437 | 1.1120 | 0.5337 | 0.2627 |
| M1 → S↓ | 0.2874 | 0.2588 | 0.2732 | 0.6919 | 0.3448 | 0.1642 |
| M0 → S↑ | 0.2663 | 0.2329 | 0.2262 | 1.1119 | 0.5337 | 0.2626 |
| M0 → S↓ | 0.2297 | 0.2278 | 0.2302 | 0.6913 | 0.3447 | 0.1641 |
| M1 → X2↑ | 0.2087 | 0.1796 | 0.1873 | 1.0509 | 0.5250 | 0.2407 |
| M1 → X2↓ | 0.2455 | 0.2187 | 0.2107 | 0.7479 | 0.4841 | 0.1832 |
| M0 → X2↑ | 0.2496 | 0.2116 | 0.2224 | 1.0508 | 0.5244 | 0.2407 |
| M0 → X2↓ | 0.2535 | 0.2494 | 0.2487 | 0.7479 | 0.4841 | 0.1833 |

Cell Description

The BMX cell performs the shifting and 2's complement inversion of the multiplicand bits (M1, M0) based on the recode control signals (X2, A, S) from the booth encoder block cell. The partial product output (PP) is represented by the logic equation:

$$PP = X2 \bullet ((M0 \bullet \bar{A}) + (\bar{M0} \bullet \bar{S})) + \bar{X2} \bullet ((M1 \bullet \bar{A}) + (\bar{M1} \bullet \bar{S}))$$

Logic Symbol



Functions¹

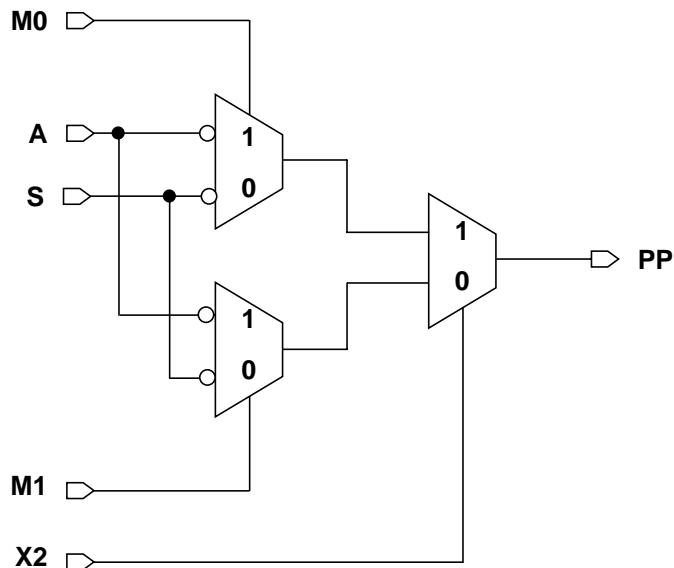
| X2 | A | S | M0 | M1 | PP |
|----|---|---|----|----|----|
| 0 | 0 | 0 | x | x | x |
| 0 | 0 | 1 | x | 0 | 0 |
| 0 | 0 | 1 | x | 1 | 1 |
| 0 | 1 | 0 | x | 0 | 1 |
| 0 | 1 | 0 | x | 1 | 0 |
| 0 | 1 | 1 | x | x | 0 |
| 1 | 0 | 0 | x | x | x |
| 1 | 0 | 1 | 0 | x | 0 |
| 1 | 0 | 1 | 1 | x | 1 |
| 1 | 1 | 0 | 0 | x | 1 |
| 1 | 1 | 0 | 1 | x | 0 |
| 1 | 1 | 1 | x | x | 0 |

¹ Shaded areas represent illegal conditions.

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| BMXX1 | 5.04 | 12.54 |

Functional Schematic



AC Power

| Pin | Power (μ W/ |
|-----|------------------|
| | X1 |
| X2 | 0.0390 |
| M0 | 0.0616 |
| A | 0.0600 |
| S | 0.0769 |
| M1 | 0.0519 |

Pin Capacitance

| Pin | Capacitanc |
|-----|------------|
| | X1 |
| X2 | 0.0036 |
| M0 | 0.0060 |
| A | 0.0047 |
| S | 0.0046 |
| M1 | 0.0056 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K _{load} (ns/pF) |
|-------------|----------------------|---------------------------|
| | X1 | X1 |
| X2 → PP↑ | 0.1357 | 4.2028 |
| X2 → PP↓ | 0.1243 | 2.5798 |
| M0 → PP↑ | 0.1938 | 4.2065 |
| M0 → PP↓ | 0.2353 | 2.5825 |
| A → PP↑ | 0.2101 | 4.2065 |
| A → PP↓ | 0.2081 | 2.5820 |
| S → PP↑ | 0.2283 | 4.2071 |
| S → PP↓ | 0.2236 | 2.5826 |
| M1 → PP↑ | 0.1812 | 4.2067 |
| M1 → PP↓ | 0.2166 | 2.5782 |

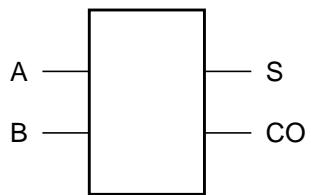
Cell Description

The CMPR22 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$$

$$CO = A \bullet B$$

Logic Symbol



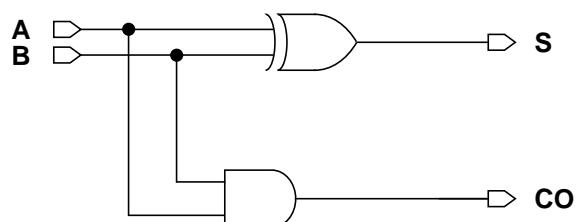
Functions

| A | B | S | CO |
|---|---|---|----|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| CMPR22X1 | 5.04 | 7.92 |

Functional Schematic



AC Power

| Pin | Power (μ W) |
|-----|------------------|
| | X1 |
| A | 0.1085 |
| B | 0.0611 |

Pin Capacitance

| Pin | Capacitance |
|-----|-------------|
| | X1 |
| A | 0.0113 |
| B | 0.0089 |

Delays (25°C, 1.8V, Typical Process)

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|--------------------|
| | X1 | X1 |
| A → S↑ | 0.0830 | 2.6588 |
| A → S↓ | 0.0893 | 1.7289 |
| B → S↑ | 0.0545 | 2.6445 |
| B → S↓ | 0.0728 | 1.6477 |
| A → CO↑ | 0.0877 | 4.2068 |
| A → CO↓ | 0.1171 | 2.7049 |
| B → CO↑ | 0.0880 | 4.2070 |
| B → CO↓ | 0.1113 | 2.7017 |

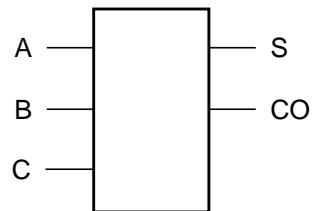
Cell Description

The CMPR32 cell takes in 3 bits of the partial product (A, B, C) and compresses them into 2-bits of partial product (S, CO). The two outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus C$$

$$CO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

Logic Symbol



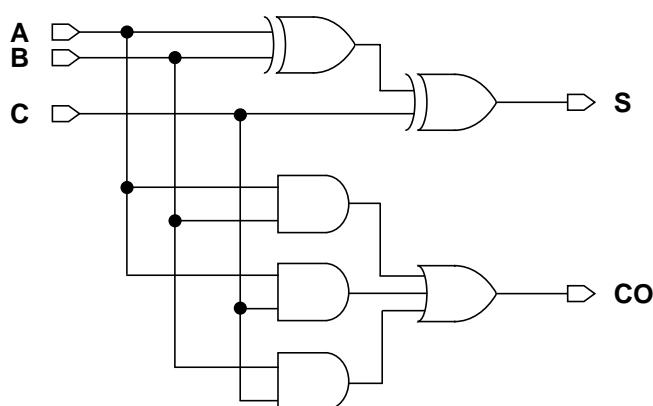
Functions

| A | B | C | S | CO |
|---|---|---|---|----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| CMPR32X1 | 5.04 | 13.86 |

Functional Schematic



AC Power

| Pin | Power |
|-----|--------|
| | X1 |
| A | 0.1189 |
| B | 0.1542 |
| C | 0.0666 |

Pin Capacitance

| Pin | Capacit |
|-----|---------|
| | X1 |
| A | 0.0075 |
| B | 0.0073 |
| C | 0.0068 |

Delays at 25°C, 1.8V, Typical Process

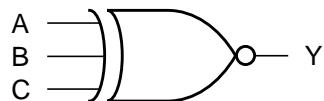
| Description | Intrinsic Delay (ns) | K _{load} (ns/ pF) |
|-------------|----------------------|-------------------------------|
| | X1 | X1 |
| A → S↑ | 0.2161 | 4.2205 |
| A → S↓ | 0.2789 | 2.6700 |
| B → S↑ | 0.2541 | 4.2243 |
| B → S↓ | 0.3160 | 2.6700 |
| C → S↑ | 0.1702 | 4.2225 |
| C → S↓ | 0.1553 | 2.6793 |
| A → CO↑ | 0.2565 | 4.2005 |
| A → CO↓ | 0.2555 | 2.6023 |
| B → CO↑ | 0.2931 | 4.2002 |
| B → CO↓ | 0.2788 | 2.5596 |
| C → CO↑ | 0.1408 | 4.2141 |
| C → CO↓ | 0.1766 | 2.6197 |

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE NOR of three inputs (A, B, C). The output (Y) is represented by the following equation:

$$Y = \overline{A \oplus B \oplus C}$$

Logic Symbol



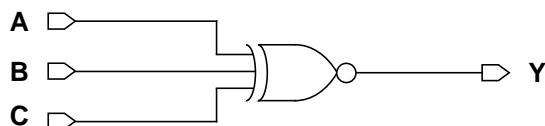
Functions

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| XNOR3X2 | 5.04 | 11.88 |
| XNOR3X4 | 5.04 | 19.80 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| A | 0.1575 | 0.2965 |
| B | 0.1349 | 0.2537 |
| C | 0.0621 | 0.1169 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| A | 0.0071 | 0.0141 |
| B | 0.0154 | 0.0291 |
| C | 0.0053 | 0.0094 |

Delays at 25°C, 1.8V, Typical Process

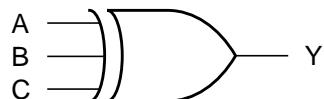
| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|-------------|----------------------|--------|---------------------------|--------|
| | X2 | X4 | X2 | X4 |
| A → Y↑ | 0.2591 | 0.2473 | 2.0909 | 1.0455 |
| A → Y↓ | 0.2851 | 0.2677 | 1.3761 | 0.6851 |
| B → Y↑ | 0.1715 | 0.1627 | 2.0907 | 1.0454 |
| B → Y↓ | 0.2024 | 0.1932 | 1.3699 | 0.6839 |
| C → Y↑ | 0.1418 | 0.1339 | 2.0897 | 1.0450 |
| C → Y↓ | 0.1429 | 0.1401 | 1.3689 | 0.6824 |

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A, B, C). The output (Y) is represented by the following equation:

$$Y = A \oplus B \oplus C$$

Logic Symbol



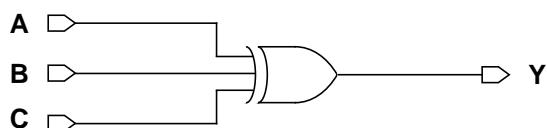
Functions

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| XOR3X2 | 5.04 | 11.88 |
| XOR3X4 | 5.04 | 19.80 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | |
|-----|------------------------------------|--------|
| | X2 | X4 |
| A | 0.1570 | 0.3027 |
| B | 0.1391 | 0.2638 |
| C | 0.0620 | 0.1172 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X2 | X4 |
| A | 0.0071 | 0.0141 |
| B | 0.0154 | 0.0292 |
| C | 0.0090 | 0.0168 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|-------------|----------------------|--------|---------------------------|--------|
| | X2 | X4 | X2 | X4 |
| A → Y↑ | 0.2599 | 0.2476 | 2.0913 | 1.0456 |
| A → Y↓ | 0.2824 | 0.2644 | 1.3775 | 0.6856 |
| B → Y↑ | 0.1701 | 0.1611 | 2.0907 | 1.0454 |
| B → Y↓ | 0.2044 | 0.1961 | 1.3693 | 0.6835 |
| C → Y↑ | 0.1414 | 0.1340 | 2.0903 | 1.0451 |
| C → Y↓ | 0.1442 | 0.1400 | 1.3655 | 0.6819 |

Advanced Arithmetic Cells

Cell Description

The CMPR42 cell takes in 4 bits of the partial product (A, B, C, D) and compresses them into 2-bits of partial product (S, CO). The cell requires an intermediate carry-in input (ICI) from the n-1 compressor and an intermediate carry-out output (CO) to the n+1 compressor. The CMPR42 cell also contains an internal sum IS. The internal sum IS, carry-in output (ICO), and the two outputs (S, CO) are represented by the logic equations:

$$IS = A \oplus B \oplus C$$

$$ICO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

$$S = IS \oplus D \oplus ICI$$

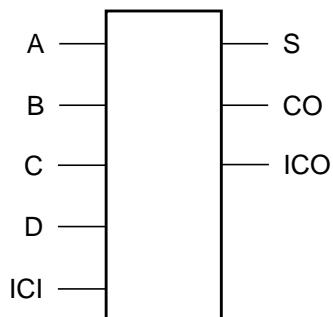
$$CO = (IS \bullet D) + (IS \bullet ICI) + (D \bullet ICI)$$

Functions

| A | B | C | IS | ICO |
|---|---|---|----|-----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

| IS | D | ICI | S | CO |
|----|---|-----|---|----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

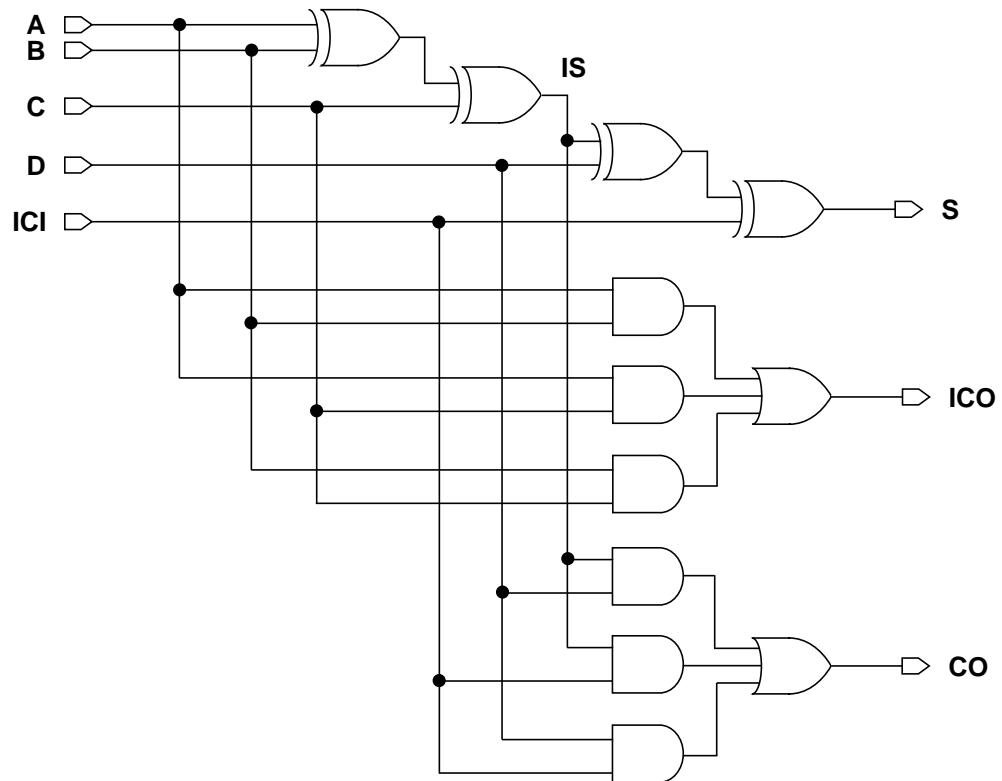
Logic Symbol



Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|-------------|------------|
| CMPR42X1 | 5.04 | 22.44 |
| CMPR42X2 | 5.04 | 26.40 |

Functional Schematic



AC Power

| Pin | Power (μ W/MHz) | |
|-----|----------------------|--------|
| | X1 | X2 |
| A | 0.1712 | 0.3082 |
| B | 0.1644 | 0.2918 |
| C | 0.1572 | 0.2786 |
| D | 0.1340 | 0.2426 |
| ICI | 0.0661 | 0.1184 |

Pin Capacitance

| Pin | Capacitance (pF) | |
|-----|------------------|--------|
| | X1 | X2 |
| A | 0.0090 | 0.0165 |
| B | 0.0092 | 0.0166 |
| C | 0.0081 | 0.0133 |
| D | 0.0048 | 0.0097 |
| ICI | 0.0030 | 0.0062 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | K_{load} (ns/pF) | |
|--------------------|-----------------------------|-----------|---------------------------------|-----------|
| | X1 | X2 | X1 | X2 |
| A → S↑ | 0.5029 | 0.5069 | 4.2187 | 2.1219 |
| A → S↓ | 0.5950 | 0.6009 | 2.5814 | 1.3752 |
| B → S↑ | 0.4570 | 0.4234 | 4.2140 | 2.1219 |
| B → S↓ | 0.5277 | 0.5176 | 2.5812 | 1.3752 |
| C → S↑ | 0.4095 | 0.3835 | 4.2141 | 2.1217 |
| C → S↓ | 0.4886 | 0.4798 | 2.5814 | 1.3752 |
| D → S↑ | 0.4222 | 0.3324 | 4.2140 | 2.1179 |
| D → S↓ | 0.4403 | 0.3974 | 2.5806 | 1.3751 |
| ICI → S↑ | 0.2359 | 0.1828 | 4.2163 | 2.1199 |
| ICI → S↓ | 0.2488 | 0.1990 | 2.5833 | 1.3758 |
| A → ICO↑ | 0.1235 | 0.0930 | 4.2173 | 2.1207 |
| A → ICO↓ | 0.1787 | 0.1527 | 2.5842 | 1.3095 |
| B → ICO↑ | 0.1223 | 0.0948 | 4.2177 | 2.1209 |
| B → ICO↓ | 0.1704 | 0.1475 | 2.5844 | 1.3097 |
| C → ICO↑ | 0.1075 | 0.0840 | 4.2135 | 2.1192 |
| C → ICO↓ | 0.1499 | 0.1314 | 2.5960 | 1.3142 |
| A → CO↑ | 0.4885 | 0.4910 | 4.2200 | 2.1197 |
| A → CO↓ | 0.5637 | 0.5732 | 2.5943 | 1.3092 |
| B → CO↑ | 0.4506 | 0.4281 | 4.2112 | 2.1196 |
| B → CO↓ | 0.4965 | 0.5103 | 2.5943 | 1.3092 |
| C → CO↑ | 0.4007 | 0.3747 | 4.2199 | 2.1196 |
| C → CO↓ | 0.4353 | 0.4152 | 2.5946 | 1.3092 |
| D → CO↑ | 0.3743 | 0.3087 | 4.2125 | 2.1176 |
| D → CO↓ | 0.3804 | 0.3049 | 2.5945 | 1.3034 |
| ICI → CO↑ | 0.1462 | 0.1017 | 4.2216 | 2.1201 |
| ICI → CO↓ | 0.1812 | 0.1484 | 2.6280 | 1.3221 |

Register File Cells

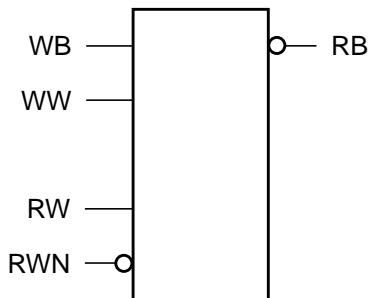
Cell Description

The RF1R1W register file cell is an active-high D-type transparent latch with an active-high tri-state output. The output (RB) is inverted.

Functions for Write Operations

| WW | WB | q[n+1] |
|----|----|--------|
| 0 | 0 | 0 |
| 0 | 1 | q[n] |
| 0 | 0 | q[n] |
| 0 | 1 | q[n] |
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 1 | 0 | q[n] |
| 1 | 1 | 1 |

Logic Symbol



Cell Size

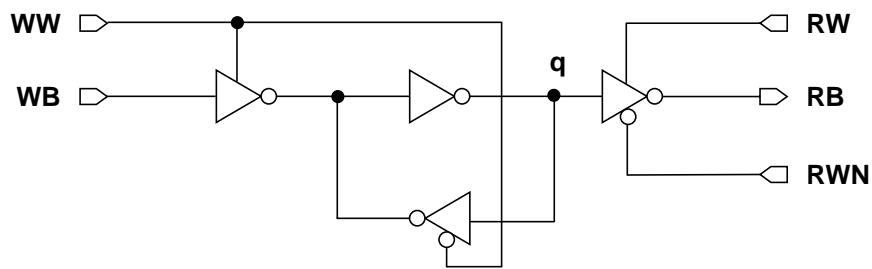
| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| RF1R1WX2 | 5.04 | 6.60 |

Functions for Read Operations¹

| RW | RWN | q | RB |
|----|-----|---|------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | Hi-Z |
| 0 | 1 | 0 | Hi-Z |
| 0 | 1 | 1 | Hi-Z |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | Hi-Z |
| 1 | 1 | 1 | 0 |

¹ Shaded areas represent operations that are legal only during RW/RWN transitions.

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) |
|-----|------------------------------------|
| | X2 |
| WW | 0.0345 |
| WB | 0.0368 |
| RW | 0.0059 |
| RB | 0.0248 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|------------------|
| | X2 |
| WW | 0.0057 |
| WB | 0.0025 |
| RW | 0.0032 |
| RWN | 0.0018 |
| RB | 0.0082 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|---------------------------|
| | X2 | X2 |
| WW → RB↑ | 0.2757 | 4.0862 |
| WW → RB↓ | 0.1731 | 1.9683 |
| WB → RB↑ | 0.2559 | 4.0862 |
| WB → RB↓ | 0.1889 | 1.9683 |
| RW → RB↑ | 0.0278 | 4.0824 |
| RW → RB↓ | 0.0132 | 1.9622 |

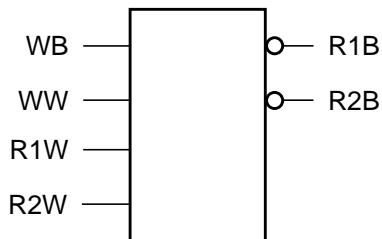
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) |
|-----|-------------|---------------|
| | | X2 |
| WW | minpwh | 0.1613 |
| WB | setup↑ → WW | 0.1055 |
| | setup↓ → WW | 0.1406 |
| | hold↑ → WW | -0.0938 |
| | hold↓ → WW | -0.1328 |

Cell Description

The RF2R1W register file cell is an active-high D-type transparent latch with two independently controlled, active-high tri-state outputs. The cell has two read ports and one write port. The outputs (R1B, R2B) are inverted.

Logic Symbol



Functions for Write Operations

| WW | WB | $q[n+1]$ |
|----|----|----------|
| 0 | 0 | $q[n]$ |
| 0 | 1 | $q[n]$ |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

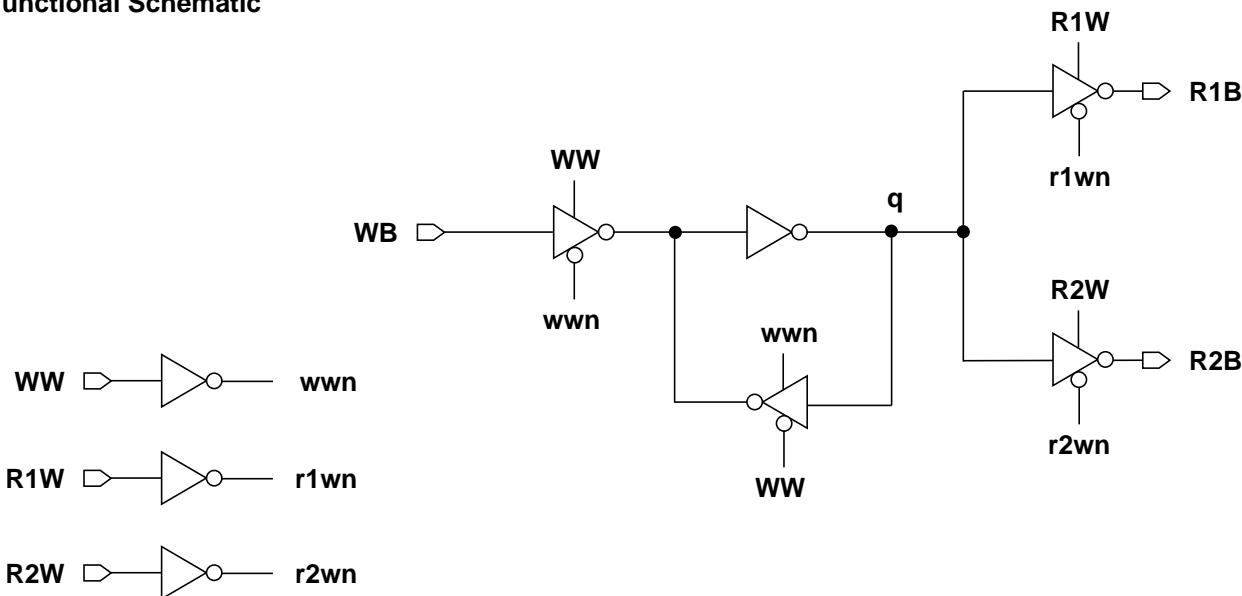
Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|----------------|--------------------------|-------------------------|
| RF2R1WX2 | 5.04 | 10.56 |

Functions for Read Operations

| R1W/ R2W | q | R1B/ R2B |
|----------|---|----------|
| 0 | 0 | Hi-Z |
| 0 | 1 | Hi-Z |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) |
|-----|------------------------------------|
| | X2 |
| WB | 0.0515 |
| WW | 0.0140 |
| R1W | 0.0120 |
| R2W | 0.0119 |
| R1B | 0.0990 |

Pin Capacitance

| Pin | Capacitance (pF) |
|-----|------------------|
| | X2 |
| WB | 0.0026 |
| WW | 0.0047 |
| R1W | 0.0037 |
| R2W | 0.0049 |
| R1B | 0.0043 |
| R2B | 0.0042 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | K_{load} (ns/pF) |
|-------------|----------------------|---------------------------|
| | X2 | X2 |
| WB → R1B↑ | 0.2957 | 4.0875 |
| WB → R1B↓ | 0.2243 | 1.9738 |
| WW → R1B↑ | 0.3121 | 4.0875 |
| WW → R1B↓ | 0.2091 | 1.9738 |
| R1W → R1B↑ | 0.0642 | 4.0811 |
| R1W → R1B↓ | 0.0153 | 1.9616 |
| WB → R2B↑ | 0.2953 | 4.0876 |
| WB → R2B↓ | 0.2241 | 1.9738 |
| WW → R2B↑ | 0.3116 | 4.0876 |
| WW → R2B↓ | 0.2088 | 1.9739 |
| R2W → R2B↑ | 0.0636 | 4.0812 |
| R2W → R2B↓ | 0.0152 | 1.9615 |

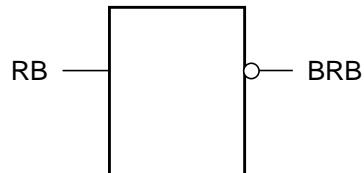
Timing Constraints at 25°C, 1.8V, Typical Process

| Pin | Requirement | Interval (ns) |
|-----|-------------|---------------|
| | | X2 |
| WB | setup↑ → WW | 0.1250 |
| | setup↓ → WW | 0.1641 |
| | hold↑ → WW | -0.1055 |
| | hold↓ → WW | -0.1406 |
| WW | minpwh | 0.1807 |

Cell Description

The RFRD output buffer has a “keeper” function that holds the input and output ports at the present level when the input (RB) is in a state of high-impedance.

Logic Symbol



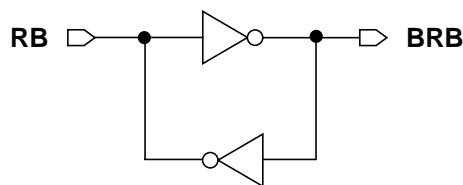
Functions

| RB | BRB |
|-----------|------------|
| 0 | 1 |
| 1 | 0 |
| Hi-Z | Keep |

Cell Size

| Drive Strength | Height (μm) | Width (μm) |
|-----------------------|--|---|
| RFRDX1 | 5.04 | 3.30 |
| RFRDX2 | 5.04 | 3.30 |
| RFRDX4 | 5.04 | 3.96 |

Functional Schematic



AC Power

| Pin | Power ($\mu\text{W}/\text{MHz}$) | | |
|-----|------------------------------------|--------|--------|
| | X1 | X2 | X4 |
| RB | 0.0311 | 0.0387 | 0.0559 |

Pin Capacitance

| Pin | Capacitance (pF) | | |
|-----|------------------|--------|--------|
| | X1 | X2 | X4 |
| RB | 0.0443 | 0.0477 | 0.0563 |

Delays at 25°C, 1.8V, Typical Process

| Description | Intrinsic Delay (ns) | | | K_{load} (ns/pF) | | |
|-------------|----------------------|--------|--------|--------------------|--------|--------|
| | X1 | X2 | X4 | X1 | X2 | X4 |
| RB → BRB↑ | 0.0493 | 0.0337 | 0.0258 | 4.1998 | 2.1138 | 1.0567 |
| RB → BRB↓ | 0.0315 | 0.0219 | 0.0167 | 2.5016 | 1.2769 | 0.6384 |