Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level:

☐ Security 1 - SMIC Confidential ☑ Security 2 - SMIC Restricted ☐ Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T		2002-11-14	JianHua Ju	Initiate
0.1T	0.1	2003-06-10	JianHua Ju	Add Technology Develop Revision:0.1
1T	0.2	2003-11-20	Stella_Huang	1) Update the description of ANT.GT1,ANT.GT3 &ANT.GT6 Rule ; 2) Add poly ,M1-M5 & M6 thickness size for the definition of CT,Via1-Via5 antenna ratio.
2T	0.3	2004-02-25	Shirly_Ye	Add several bond pad options
3T	0.4	2004-05-19	Brian_Zhang	Added comments on the reasons for via and via array shapes should be used in bond pad. Add comments in the PA.1 item.

1. Title: 0.18 µm LOGIC 1.8/3.3V Antenna Ratio / Scribe Line and Guard Ring Guideline / Bond Pad Opening Design Guide Rule

2. Purpose: This Design Guideline is additional rule for 0.18um Logic design rule

3. Scope: All SMIC Fabs

4. Nomenclature: NA

5. Reference: NA

6. Responsibility: LOGIC Technology Development and Manufacture Center

7. Subject Content:

SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION

0.18 µm LOGIC 1.8/3.3V Antenna Ratio / Scribe Line and Guard Ring Guideline / Bond Pad Opening Design Guide Rule (recommendation)

01-Jan-2004

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Table of Contents

1. Antenna Ratio Rules

Antenna ratio rules are intended to reduce gate oxide damage during high density plasma processing in chip fabrication.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**ANT – Antenna Ratio Rules for GT, M1 to M6**	
ANT.GT1	Maximum ratio of poly perimeter area on field to the related poly gate area	200
ANT.GT2	When a protection diode is not used, the maximum ratio of single-layer metal perimeter area to the related poly gate area (for M1 to M5)	400
ANT.GT3	The maximum ratio of metal perimeter area (single-layer) to the active poly gate area can be calculated by the following equation, if a protection diode with area larger than 0.203 um^2 is used. Ratio = diode area * 400 + 2200 for M1, 2, 3, 4, and 5 single layer. Ratio = diode area * 8000 + 30000 for M6 single layer.	
ANT.GT4	Maximum drawn ratio of CT area to the related poly gate area	10
ANT.GT5	When the protection diode is not used, the maximum single layer drawn ratio of Via area to the active GT area connected directly to it	20
ANT.GT6	The maximum drawn ratio of the via area to the active Poly gate area can be calculated by the following equation, if a protection diode with area larger than 0.203 um^2 is used. Ratio = diode area * 83.33 + 75 for single layer	

The definition of poly, M1-M6 antenna ratio for each layer is

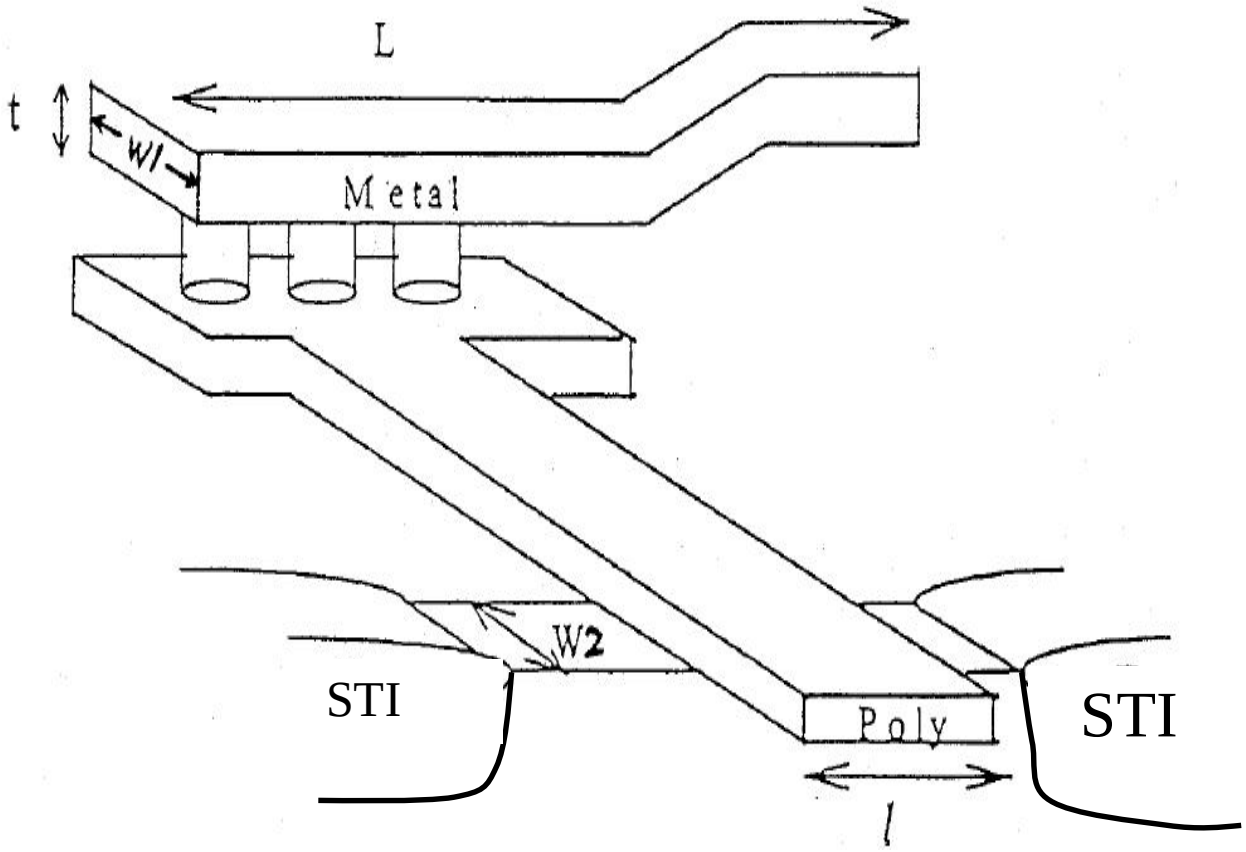
Ratio= 2[(L+W)x t]/ W2 x l

L : floating metal length connected to gate
W1 : floating metal width connected to gate
t : metal thickness
W2 : connected transistor channel width
l : connected transistor channel length

The definition of CT,Via1-Via5 antenna ratio is

Ratio={total CT (Via) area }/W2 x l

The poly thickness is 2000A
The M1-M5 thickness is 5300A.
The M6 thickness is 9900A.



2. BOND PAD OPENING RULES

Bond pad opening mask defines the window where the bond wires connect the circuit to the lead frame. The pitch and size should be increased whenever possible in order to facilitate bonding and wafer sorting. However, assembly house may impose additional constraints according to their wafer sort and assembly capabilities. It is designers' responsibility to take these additional constraints into consideration during layout. There is no universal rule for bond pad pattern designs. In this section, we provide several pattern examples for pad layout. You can select the one(s) which fits your need most.

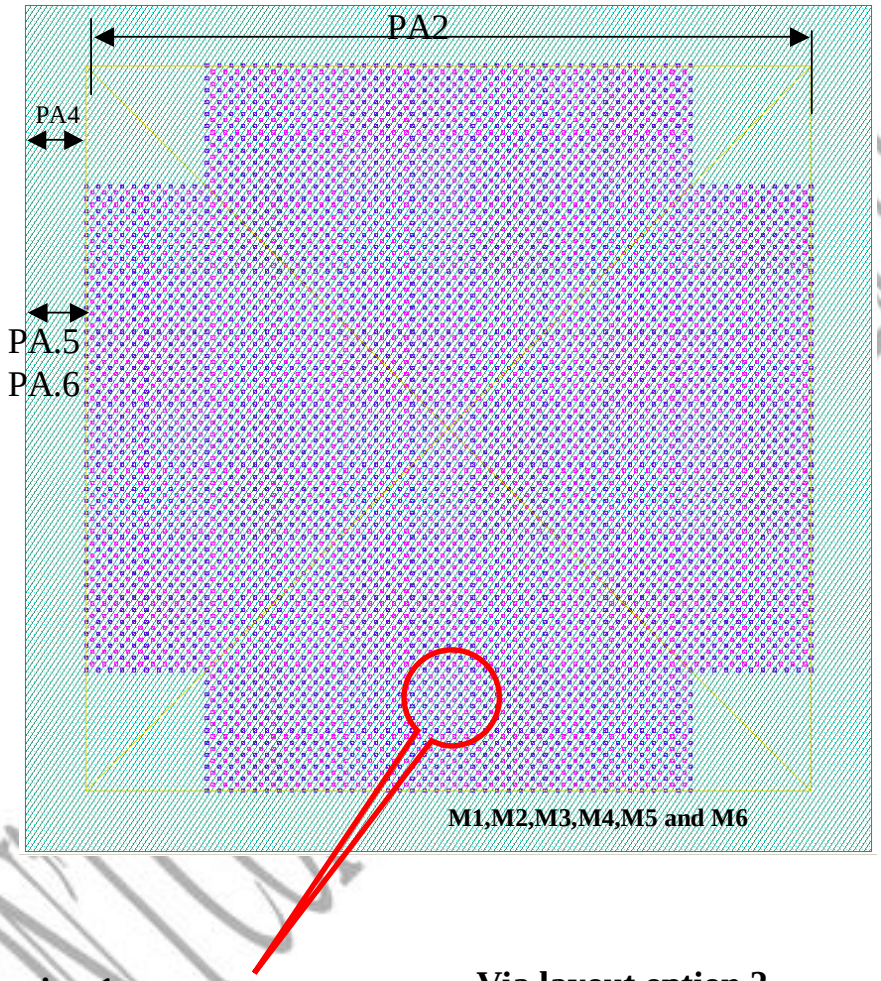
RULE NO.	DESCRIPTION	LAYOUT GUIDELINE
Layer	**PA – Passivation Area**	
PA.1	The bond pad structure must be M6/Via5/M5/Via4/M4/Via3/M3/Via2/M2/Via1/M1. You can choose any bond pad pattern options list in the next few pages. Notice that vias of any two adjacent via layers should not be stacked up directly. The via array is arranged in a shape to reduce mechanical stress in the bond pad.	
PA.2	Minimum dimension of a bond pad window	86.0
PA.3	Minimum space between two bond pad windows	15.0
PA.4	Minimum and maximum extension of Metal n (n=1-6) over a bond pad	5.0
PA.5	Minimum extension of Metal n (n=1-6) over the nearest Via n (n=1-5) {vias on the four corner of diamond}	3.0
PA.6	Maximum extension of Metal n (n=1-6) over the nearest Via n (n=1-5) {vias on the four corner of diamond}	6.0
PA.7	Minimum and maximum width of Via n (n=1, 5) in a bond pad	0.36
PA.8	Minimum space between two Via n (n=1, 5) in a bond pad	0.68
PA.9	Minimum space between Via n and Via (n+1)	0.2
PA.10	Minimum ratio of total exposed Via n area to bond pad window	5%

* Add 8 dummy bond pads at 4 corners of the die to form the double bond pads for wire sweep protection during mold encapsulation of packaging.

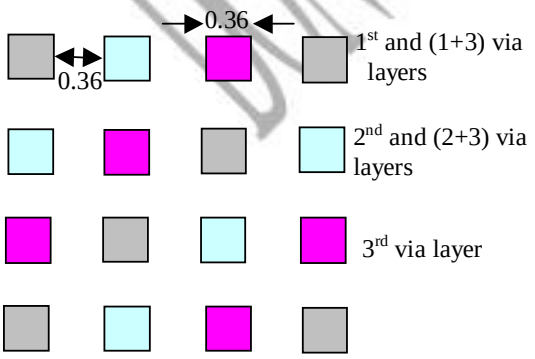
* If there is space > 150um x 150um left in the corner of the die after the 8 dummy pads are added, please add more dummy pads in the corner to keep the pad free area in the corner less than 150 um x150 um. The pad structure must be M6/M5/M4/M3/M2/M1.

* For 1P5M process, please skip metal5 and via4 layers.
* For 1P4M process, please skip metal5, metal4, via4 and via3 layers.
* For 1P3M process, please skip metal5, metal4, metal3, via4, via3 and via2 layers.
* For 1P2M process, please skip metal5, metal4, metal3, metal2, via4, via3 and via2, via1 layers.

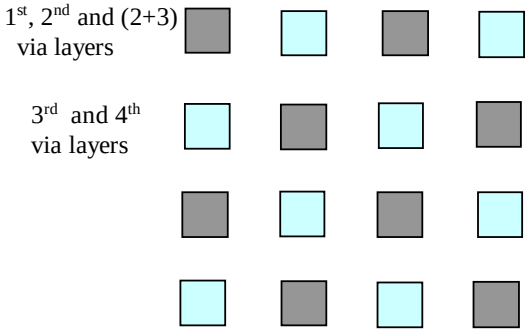
PASSIVATION PATTERN –Option 1



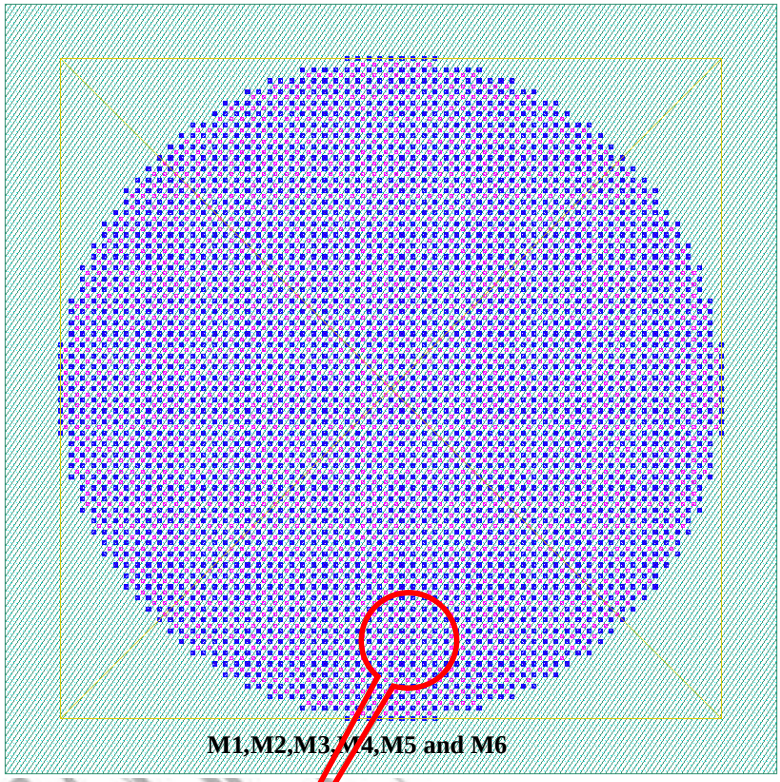
Via layout option 1



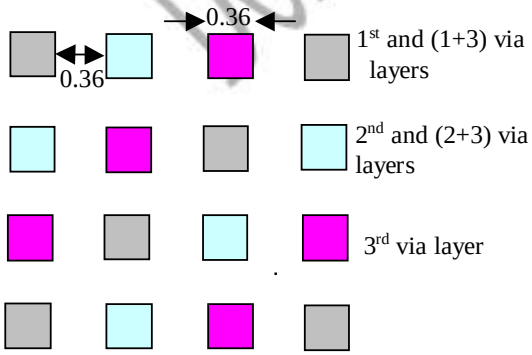
Via layout option 2



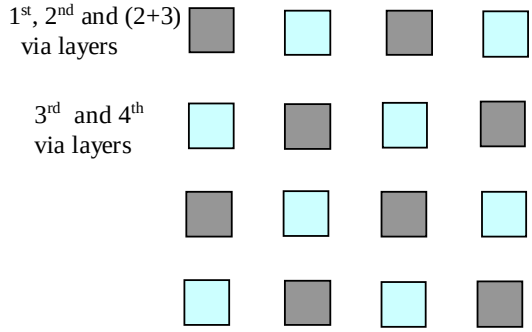
PASSIVATION PATTERN –Option 2



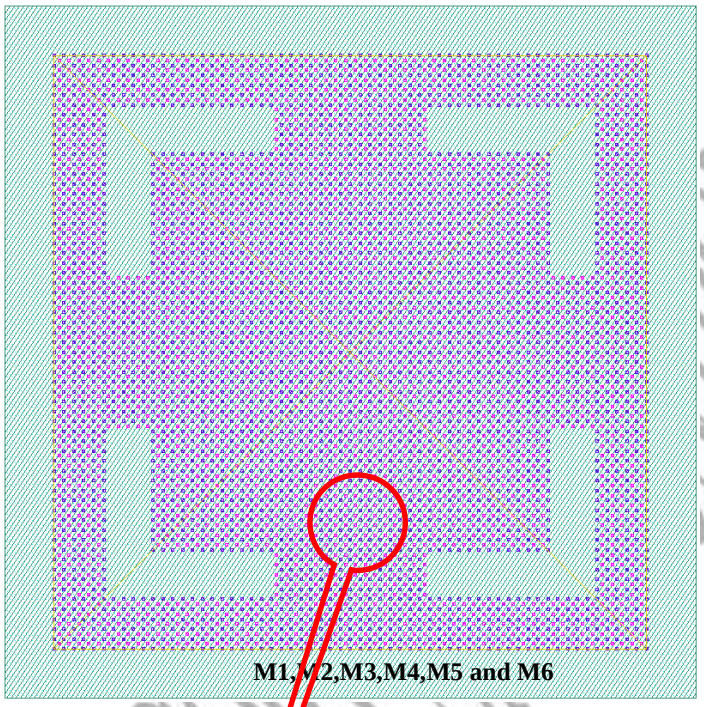
Via layout option 1



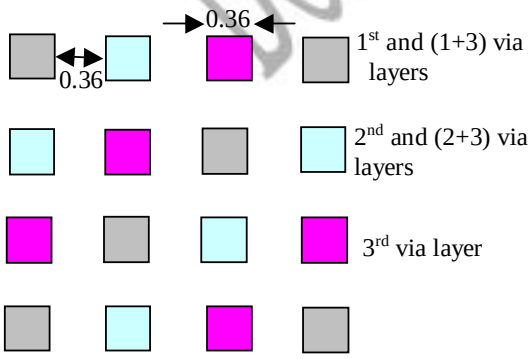
Via layout option 2



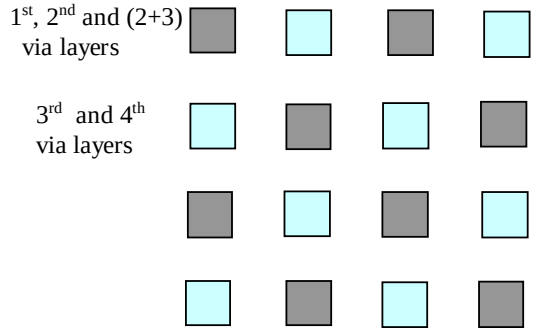
PASSIVATION PATTERN –Option 3



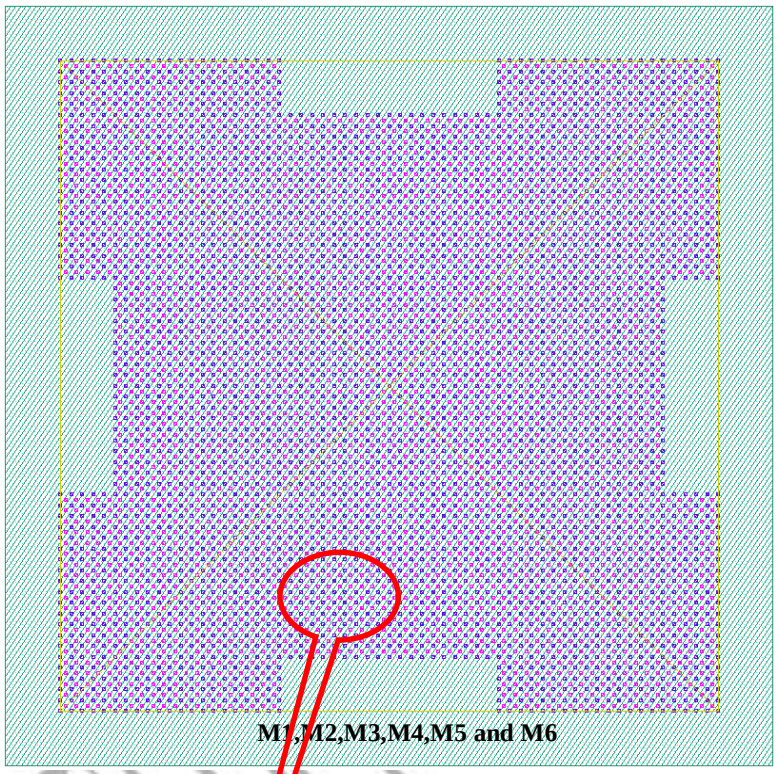
Via layout option 1



Via layout option 2

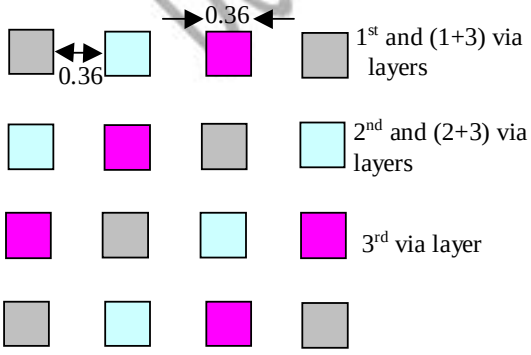


PASSIVATION PATTERN–Option 4

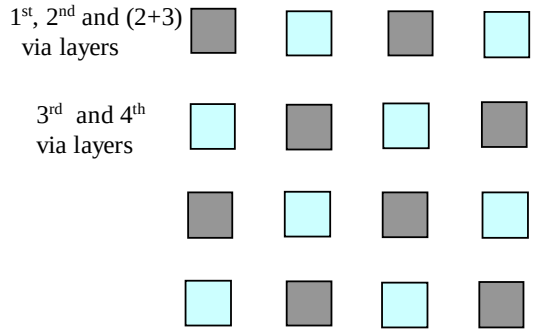


M1,M2,M3,M4,M5 and M6

Via layout option 1



Via layout option 2



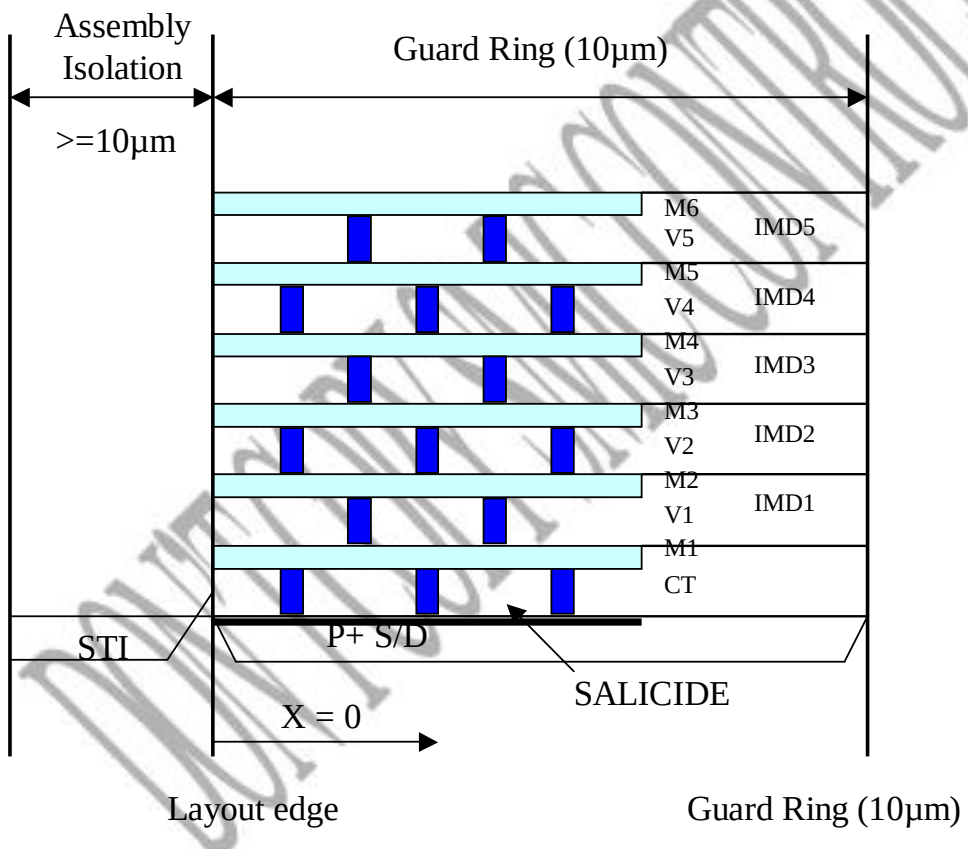
3. Scribe Line and Guard Ring Guideline

A. Use of the scribe line guard ring to protect test pattern is recommended

A continuous scribble line guard ring is required on all sides of a chip, which is intended for dicing and packaging. SMIC recommends that test pattern should have scribe line guard ring. The dimensions stated in this section are minimum

*B. Typical structure of scribe line guard ring

The typical structure of scribe line guard ring for 1P6M process is as follows:



* For 1P5M process, please skip metal5 and via4 layers.
* For 1P4M process, please skip metal5, metal4, via4 and via3 layers.
* For 1P3M process, please skip metal5, metal4, metal3, via4, via3 and via2 layers.
* For 1P2M process, please skip metal5, metal4, metal3, metal2, via4, via3 and via2 , via1 layers.

*C. Detailed dimension for scribe line guard ring layout

For detailed dimension of scribe line guard ring layout, please refer to the following table, where X0 means starting X-coordinate and X1 means ending X-coordinate.

Layers inside Ring	X0	X1	Size (µm)
AA	0.2	9.8	9.6
CT	1.32	1.54	0.22
CT	3.08	3.30	0.22
CT	4.84	5.06	0.22
M1	0.00	6.00	6.00
V1	2.07	2.33	0.26
V1	3.86	4.12	0.26
M2	0.00	6.00	6.00
V2	1.28	1.54	0.26
V2	3.07	3.33	0.26
V2	4.86	5.12	0.26
M3	0.00	6.00	6.00
V3	2.07	2.33	0.26
V3	3.86	4.12	0.26
M4	0.00	6.00	6.00
V4	1.28	1.54	0.26
V4	3.07	3.33	0.26
V4	4.86	5.12	0.26
M5	0.00	6.00	6.00
VT	2.07	2.43	0.36
VT	3.86	4.22	0.36
MT	0.00	6.00	6.00

8. Attachment: NA