Paper Title

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I. DSP Part

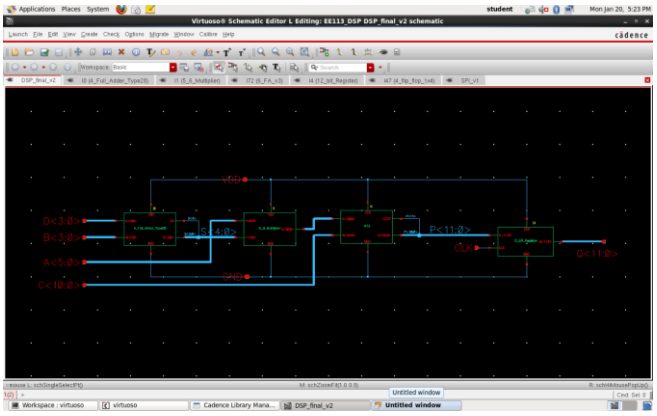
In our DSP module, the cornerstone of its computational prowess lies in the meticulously designed arithmetic units, where simplicity meets ingenuity. At its heart, we utilized a one-bit Full Adder structure, masterfully crafted using a Static CMOS Mirror Adder configuration. This architecture, requiring only 24 transistors, achieves an impressive balance between efficiency, area optimization, and reliability. The choice of this specific design was driven by its capacity to minimize propagation delays while maintaining robust signal integrity—qualities that are paramount in high-performance digital systems.

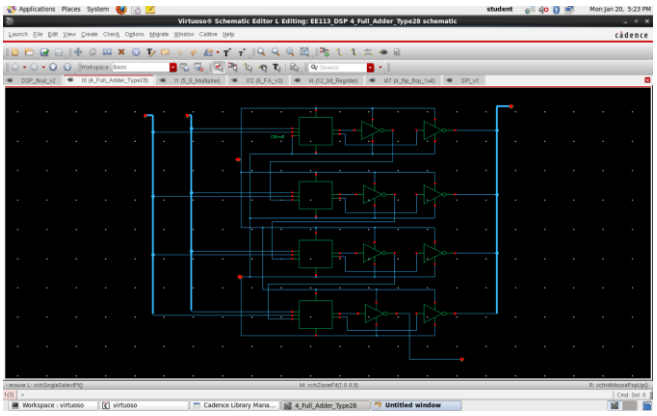
The CMOS Mirror Adder, with its elegant logic for carry generation and propagation, operates as a seamless amalgamation of speed and power efficiency. The carry generation logic ensures swift computation, while the kill logic averts unnecessary propagation, reducing delay (t_carry) in multi-bit cascaded adders. Simultaneously, the sum delay (t_sum) is minimized, ensuring the module meets stringent timing requirements. This level of synchronization becomes even more critical in our application, where arithmetic precision fuels subsequent modules.

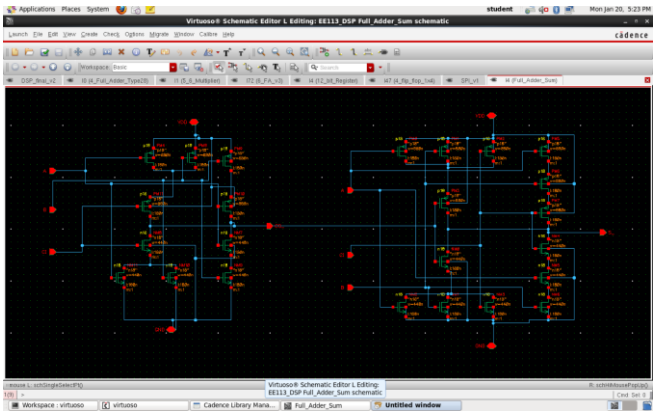
To complement this, the multiplier leverages AND gates to construct its core logic, enabling efficient bit-wise multiplication. This simple yet effective strategy allowed us to seamlessly integrate a 6-bit multiplier, adhering to the overall operation $P = (B + D) \times A + C$, where every component synergizes to uphold the computational integrity.

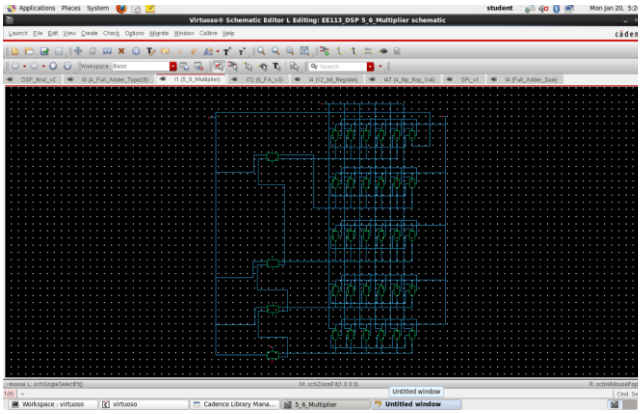
Finally, for output storage, we incorporated a robust 16-bit parallel D Flip-Flop register. This module functions as the ultimate arbiter, ensuring precise data retention and synchronization at the clock's rising edge. Its parallel architecture adeptly captures and stores the DSP's 16-bit output, aligning with system-wide timing constraints. The use of D Flip-Flops eliminates glitches, securing a clean output even in scenarios with rapid state transitions.

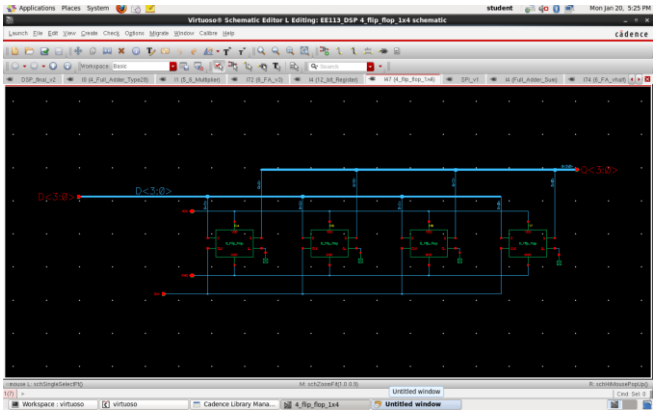
Through exhaustive simulations, the DSP design has demonstrated impeccable performance. Every stage, from arithmetic logic to the final register, has validated its functionality under varying input conditions. The layout optimization further ensures that the design meets area constraints without compromising on speed, achieving an ideal harmony of power, performance, and area (PPA). The integration of these meticulously engineered components highlights a design philosophy that marries simplicity with precision, paving the way for scalable and adaptable digital solutions.

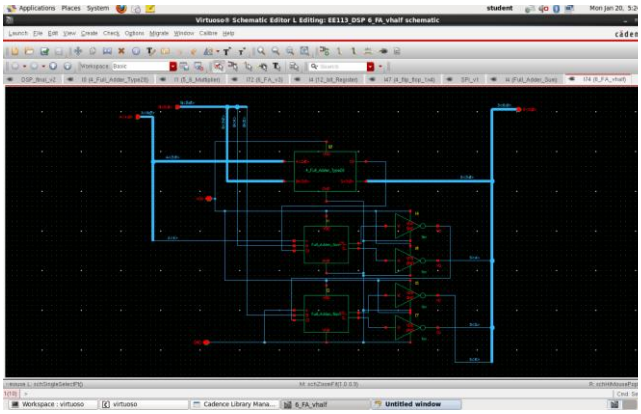


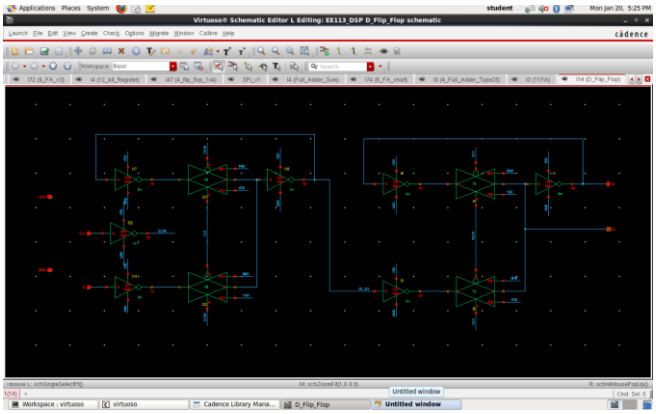


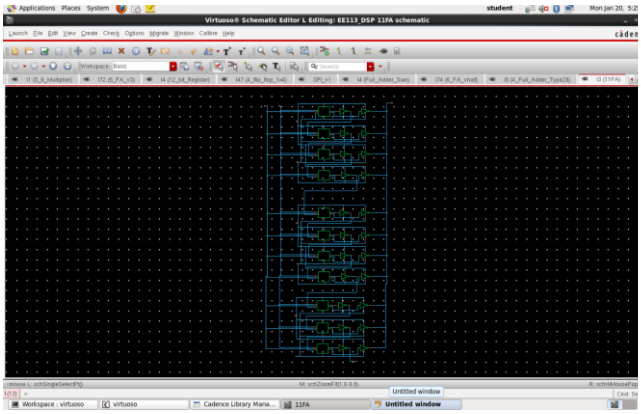


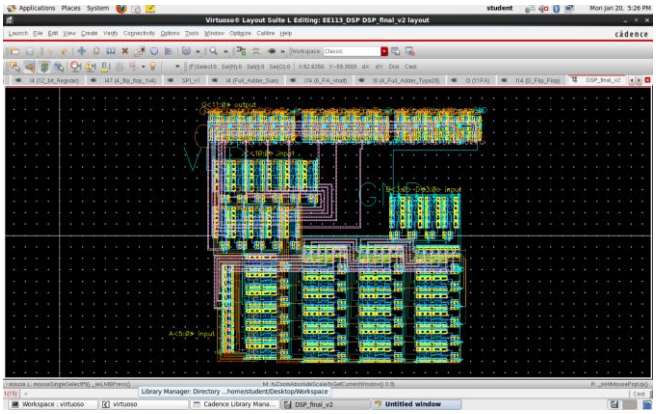


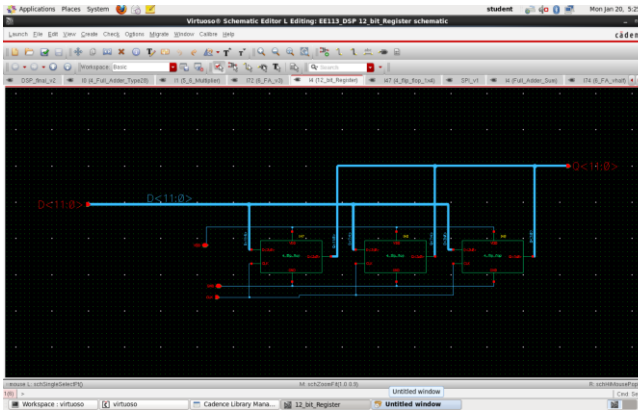












II. SPI Part

In the SPI module, the input data is received in a serial format, which necessitated the design of a 16-bit shift register to convert the serial data into a parallel output. This shift register is constructed using D Flip-Flops, ensuring precise data latching at each clock cycle. To prevent erroneous data transmission during the process, we implemented a 4-bit counter to count 16 clock cycles, generating a "DONE" signal upon completion. This signal serves as the control trigger for subsequent operations, ensuring synchronization across the system.

The 16-bit shift register is thoughtfully structured. The first bit indicates whether the operation is a write operation. The second, third, and fourth bits determine the target RAM address for the operation. To store the data efficiently, we utilized SRAM as the fundamental building block for the RAM. Each RAM block consists of 12 bits grouped together under the same control signal. The write operation to a specific

RAM location is enabled only when the following conditions are simultaneously satisfied:

The first bit indicates a write operation.

The second, third, and fourth bits collectively match the target address.

The "DONE" signal is high, signaling the end of the serial-to-parallel conversion process.

When these conditions are all met, the corresponding RAM location accepts the data and stores it correctly. This design ensures the integrity and precision of data transmission, successfully completing the SPI operation. By combining the shift register, counter, and SRAM logic, our SPI module achieves efficient and reliable serial-to-parallel data conversion and storage, seamlessly integrating with the overall system.