Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level:

☐ Security 1 - SMIC Confidential ☑ Security 2 - SMIC Restricted ☐ Security 3 - SMIC Internal

Document Change History

| Doc. Rev. | Tech Dev. Rev. | Effective Date | Author | Change Description |
|---|---|---|---|---|
| 0T | | 2001-12-24 | Allen Fan 范忠黎 | Initiate |
| 1T | | 2002-3-7 | Feng Guang Tao | In this new version 1T, the terminology is uniformed. And a number of verbal description errors and figure errors in previous version are also corrected. |
| 1.1T | 1.0 | 2003-06-10 | JianHua_Ju | Add Technology Develop Revision:1.0 |
| 2T | 2.0 | 2003-12-09 | Stella_Huang | 1) Delete ESD2 layer<br>2) Add mask layer digitized area description<br>3) Add nwell resistor rule description<br>4) Add native device rule<br>5) Modify GT.10, GT.11, GT.12<br>6) Add GT.14 rule<br>7) Add GT density recommendation.<br>8) Add poly resistor rule recommendation 1.8g<br>9) Add NLL.14, PLL.14, NLH.14, PLH.14 rule<br>10) Modify metal dummy rule description M1.8, Mn.8, MT.7 |
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1.Title: 0.18µm LOGIC 1P6M Salicide 1.8V/3.3V Design Rules.

2.Purpose: To provide SMIC 0.18µm layout design rules for the customers use.

3.Scope: All SMIC Fabs.

4.Nomenclature: N/A

5.Reference: N/A

6.Responsibility:

TD is responsible for this design rule maintenance before the technology is transferred to FAB;

Fab/E1 is responsible for this design rule maintenance after the technology is transferred to FAB.

7.Subject Content:

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# 0 USER GUIDE

## Part I Description of SMIC Mask Layer
## Part II Suggestions for the Optimization of Circuit Design

## Part I

**SMIC Key Process Sequence and Layer Digitized Area**

| No | Layer Name | Pattern Description | Digitized Area (Dark/Clear) |
|---|---|---|---|
| 1 | AA | Active Area | D |
| 2 | AR | Reverse Active Area | C |
| 3 | KV | Alignment mark clear-out | C |
| 4 | NW | N-Well | C |
| 5 | PW | N-Well | D |
| 6 | DG | Dual Gate (thick oxide) | D |
| 7 | GT | Poly gate | D |
| 8 | PLH | PMOS LDD implant for 3.3V | C |
| 9 | NLH | NMOS LDD implant for 3.3V | C |
| 10 | PLL | PMOS LDD implant for 1.8V | C |
| 11 | NLL | NMOS LDD implant for 1.8V | C |
| 12 | SP | P+ implant | C |
| 13 | SN | N+ implant | C |
| 14 | ESD1 | ESD implant for Boron (B) | C |
| 15 | SAB | Salicide block area | D |
| 16 | CT | Contact | C |
| 17 | M1 | Metal-1 | D |
| 18 | V1 | VIA-1 | C |
| 19 | M2 | Metal-2 | D |
| 20 | V2 | VIA-2 | C |
| 21 | M3 | Metal-3 | D |
| 22 | V3 | VIA-3 | C |
| 23 | M4 | Metal-4 | D |
| 24 | V4 | VIA-4 | C |
| 25 | M5 | Metal-5 | D |
| 26 | V5 | VIA-5 | C |
| 27 | M6 | Metal-6 | D |
| 28 | PA | Passivation/Pad | C |
| 29 | PI | Polyimide | D |

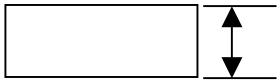
## Part II Suggestion for the optimization of circuit design

1. Front-end concerns
   A. AA: add dummy patterns for isolated small structures or open areas around AA.
   B. Poly: add dummy poly patterns at the edge of isolated structures especially when the pattern density is less than 14%.
   C. Follow the antenna rules to ensure gate oxide reliability.
   D. For the leakage concern, avoid 90 degree bent poly designs, which should be replaced by 45 degree bent poly on AA with shortest length.
   E. Avoid island pattern designs for implantation layers.
2. Back-end concerns
   A. Add dog-bone or wider line end designs for metal lines.
   B. Use redundant contacts or Via's if possible.
   C. Avoid small island structures for metal.

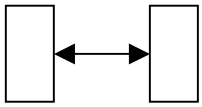
# 1.0 LAYOUT RULE DESCRIPTION

## 1.1 Definition of the Layout Layers

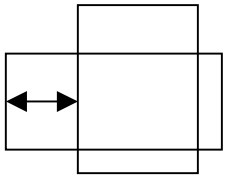
**Width**



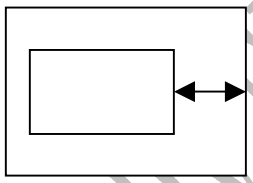
**Space /separation**



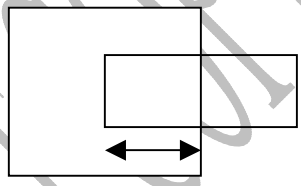
**Extension**



**Enclosure**

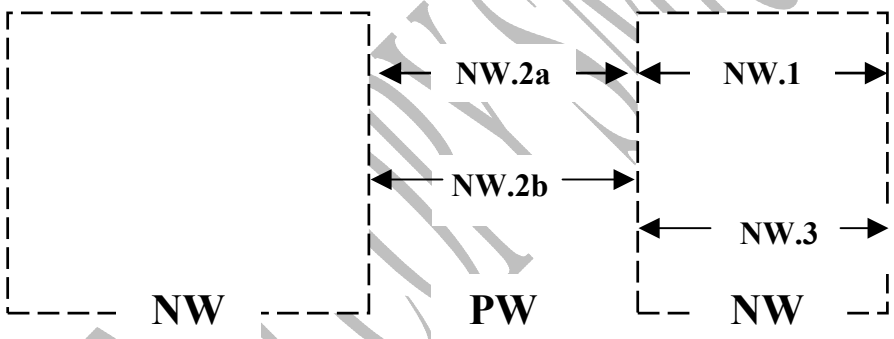


**Overlap**



### 1.2 N-Well

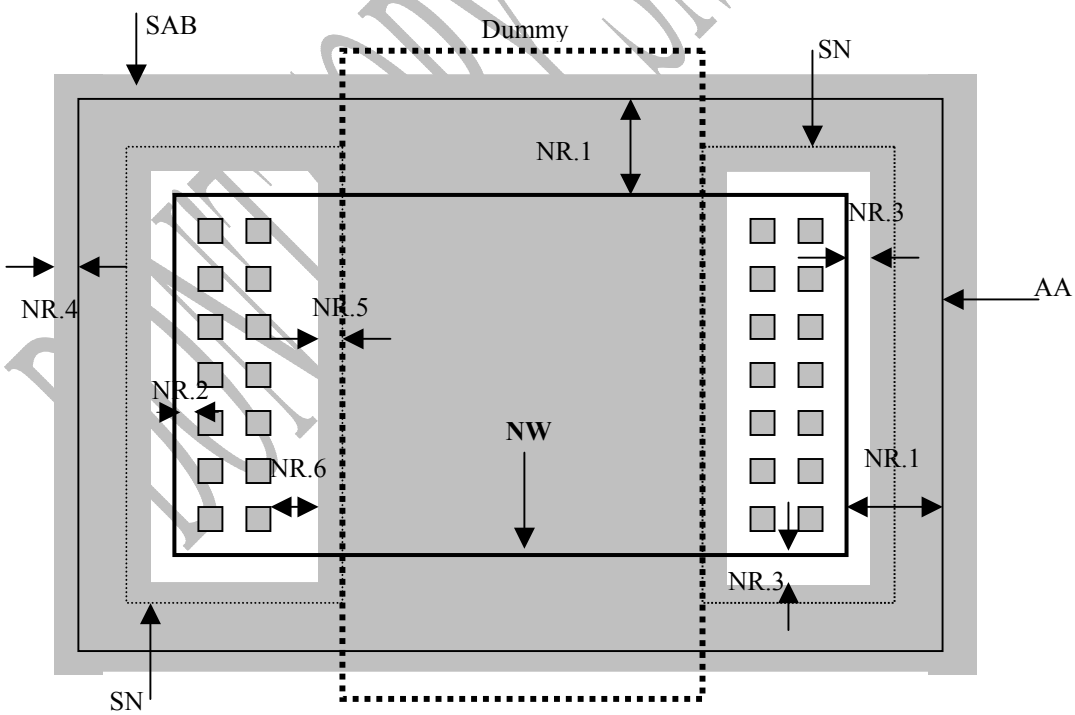
| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| NW.1 | Minimum width of an NW region | 0.86 |
| NW.2a | Minimum space between two NW regions with the same potential<br><br>Merge if space is less than 0.6µm | 0.60 |
| NW.2b | Minimum space between two NW with different potential | 1.40 |
| NW.3 | Minimum dimension of an NW region not connected to the most positive power supply<br><br>Put an NW resistor in the AA region to minimize the influence of process variation on NW resistance | 2.10 |



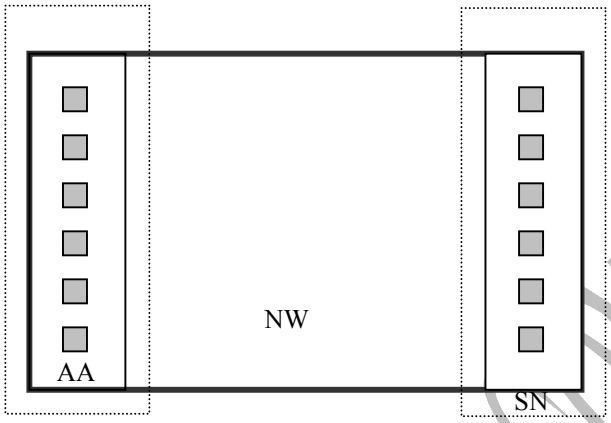
### 1.3 N-Well Resistor

a. NW resistor within AA
* Use SAB to prevent the NW resistance region from forming salicide
* Use a dummy layer to prevent LDD and SN/SP from penetrating into the NW resistance region

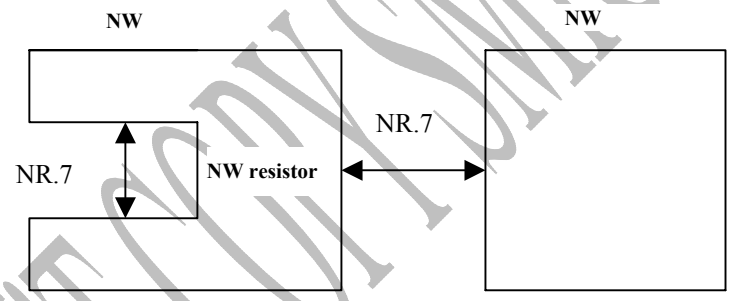
| RULE NO | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| NR.1 | Minimum enclosure of an AA beyond a NW | 1.00 |
| NR.2 | Minimum enclosure of a salicide NW beyond a CT | 0.30 |
| NR.3 | Minimum space between SAB to related NW | 0.30 |
| NR.4 | Minimum enclosure of a SAB beyond a related AA | 0.22 |
| NR.5 | Minimum overlap of a SN to SAB inside NW | 0.40 |
| NR.6 | Minimum space between SAB to related CT in SAB hole | 0.30 |
| NR.7 | Minimum NW space 1.4um | 1.40 |
| NR.8 | LDD, SN or SP is not allowed in the NW resistance area. | |



b. NW resistor under STI



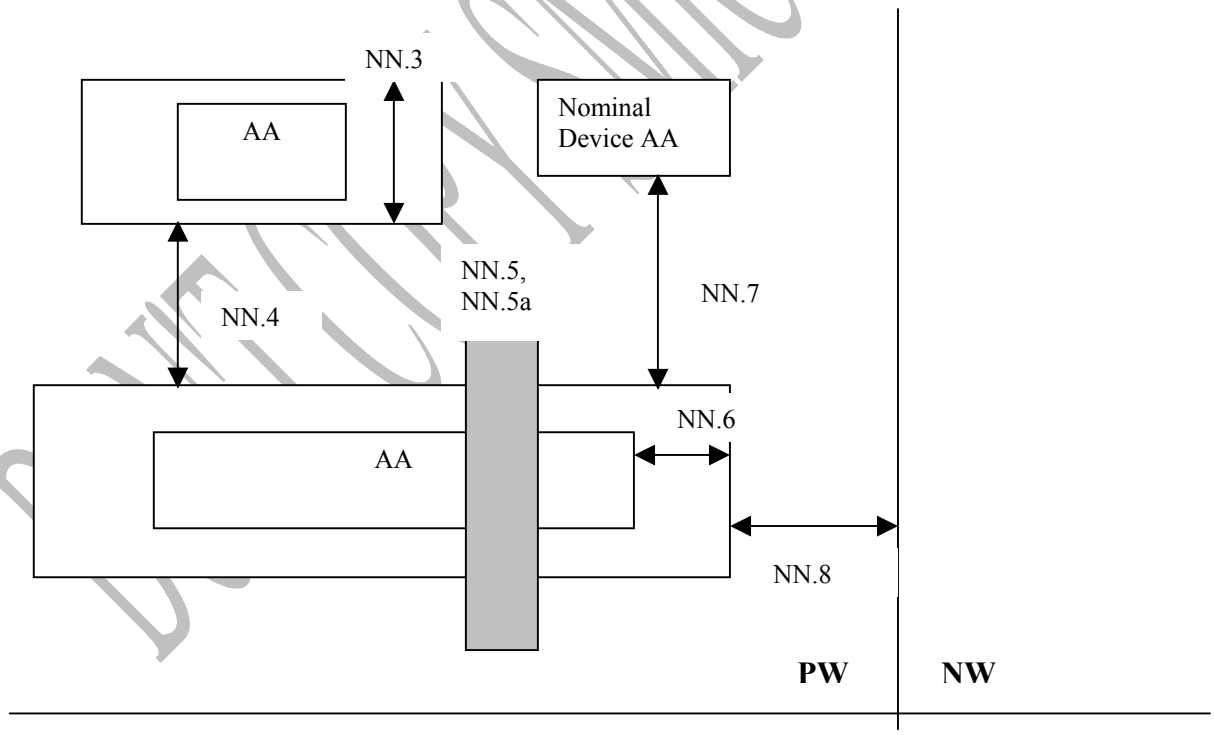

c. Minimum NW resistor space is 1.4um (NR.7), otherwise the space less than 1.4um will cause resistance decrease of NW resistor due to mergence of different regions.



### 1.4 NN(Native Device) rule

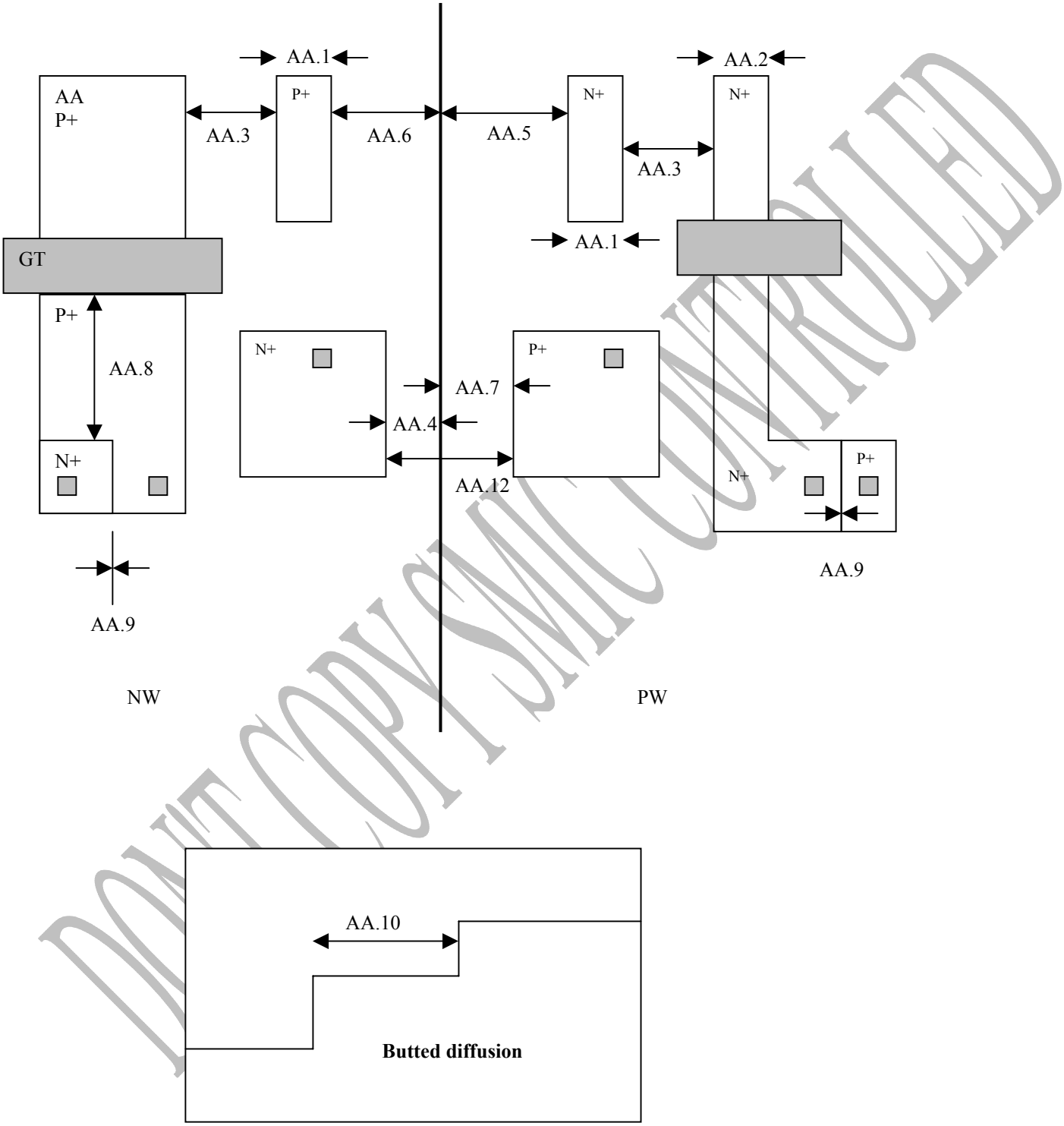
This dummy layer is used for mask making. If using native NMOS in circuit, P-Well is generated by reverse tone of (N-Well + Native dummy layer)

| RULE NO. | DESCRIPTION | LAYOUT GUIDELINE (Unit in μm) |
|---|---|---|
| NN.1 | NN inside or cross over a N-Well is not allowed | |
| NN.2 | NN inside or cross over a Deep N-Well is not allowed | |
| NN.3 | Minimum dimension of NN region | 0.84 |
| NN.4 | Minimum space between 2 NN region in same potential | 0.84 |
| NN.5 | Minimum Gate dimension of 1.8V native device | 0.50 |
| NN.5a | Minimum Gate dimension of 3.3V native device | 1.20 |
| NN.6 | Minimum and Maximum NN enclosure beyond SN(N+) AA region | 0.26 |
| NN.7 | Minimum space from NN region to a nominal AA region | 0.52 |
| NN.8 | Minimum space from NN region to N-Well edge | 1.62 |
| NN.9 | Bent Gate Poly is not allowed to put in NN region | |
| NN.10 | P+ region is not allowed to put in NN region | |
| NN.11 | Only one AA region is allowed to put in NN region | |



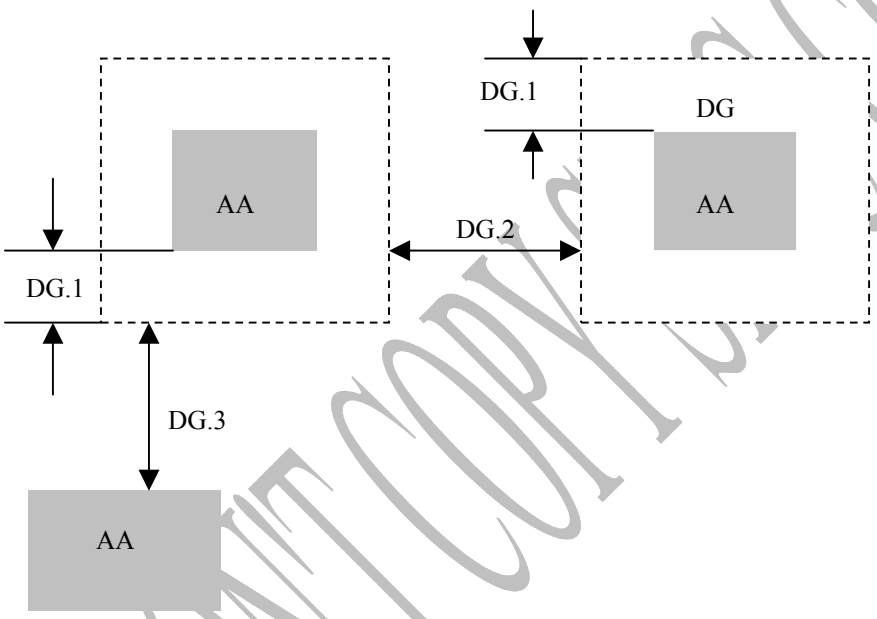
## 1.5 AA – Active area

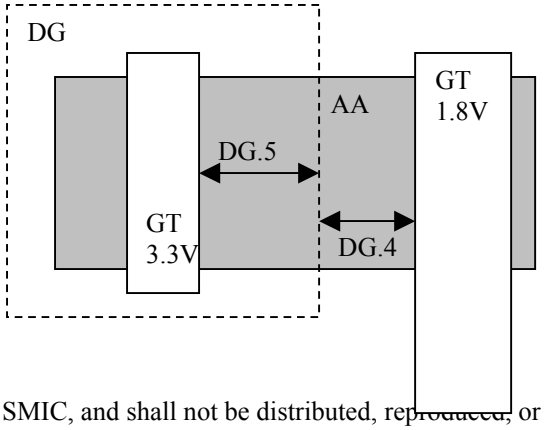
| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| AA.1 | Minimum width of an active region for interconnect (N+/P+) | 0.22 |
| AA.2 | Minimum width of an active region to define the width of NMOS/PMOS | 0.22 |
| AA.3 | Minimum space between N+ AA and N+ AA or P+ AA and P+ AA (both regions are either inside or outside NW) | 0.28 |
| AA.4 | Minimum enclosure from NW edge to an N-well pick-up | 0.12 |
| AA.5 | Minimum space between N-Well edge and an N+AA region which is outside an NW | 0.43 |
| AA.6 | Minimum space between N-Well edge and a P+AA region which is inside an NW | 0.43 |
| AA.7 | Minimum space between N-Well edge and a P+AA region (for PW pick-up) outside an NW | 0.12 |
| AA.8 | Minimum space between poly edge and edge of a butted diffusion AA region | 0.32 |
| AA.9 | Minimum space between N+AA and P+ AA for butted diffusion | 0.00 |
| AA.10 | Minimum area of a butted diffusion AA is 0.176µm$^2$. At least one segment (AA.10) of the consecutive SN/SP edge of butted diffusion AA should be longer than 0.42µm. | 0.42 |
| AA.11 | Minimum area of a stand-along AA region | 0.20µm$^2$ |
| AA.12 | For the situation where N-well and P-well pick-ups are put head-to-head across the well boundary, the space between N-pick-up and P-pick-up should be 0.36µm in order to meet the implant layout rules. | |



### 1.6 DG – Dual Gate

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| DG.1 | Minimum enclosure of DG beyond the active AA region | 0.32 |
| DG.2 | Minimum DG space between two DG regions, merge if the space is less than 0.45um | 0.45 |
| DG.3 | Minimum space between DG edge and AA region | 0.32 |
| DG.4 | Minimum space between DG region and 1.8V transistor gate | 0.40 |
| DG.5 | Minimum enclosure of DG region beyond 3.3V transistor gate | 0.40 |

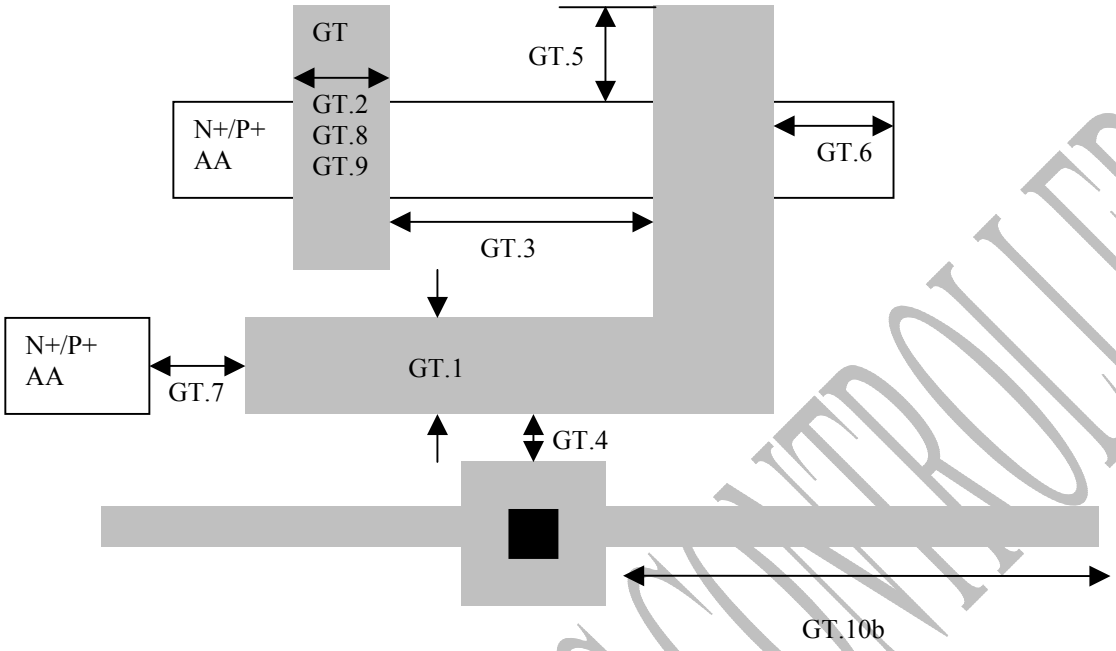


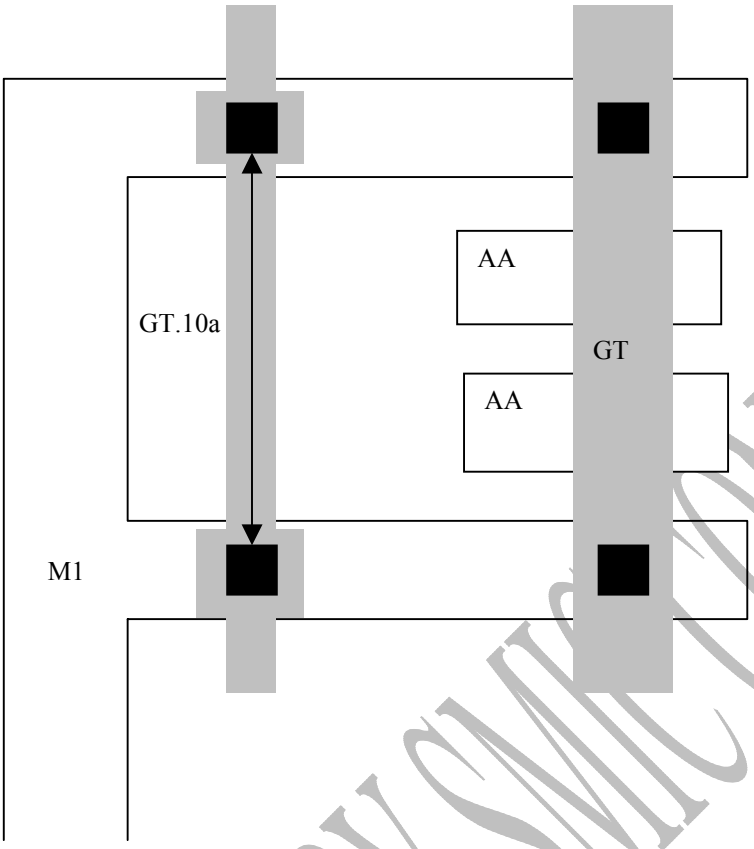



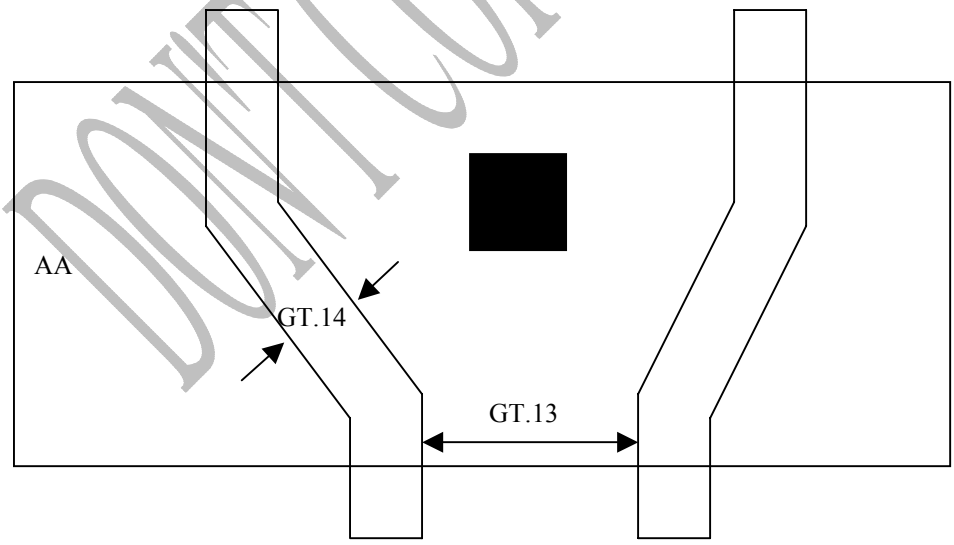
## 1.7 Poly

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in μm) |
|---|---|---|
| GT.1 | Minimum width of a GT region for interconnects. | 0.18 |
| GT.2 | Minimum width of a GT region for channel length of 1.8V PMOS/NMOS. | 0.18 |
| GT.3 | Minimum space between two GT regions on AA with no contact. | 0.25 |
| GT.4 | Minimum space between two GT regions on field oxide area. | 0.25 |
| GT.5 | Extension beyond diffusion to form poly end cap | 0.22 |
| GT.6 | Minimum extension from AA region to GT | 0.32 |
| GT.7 | Minimum space between field interconnect poly and AA | 0.10 |
| GT.8 | Minimum width of a GT region for 3.3V PMOS | 0.30 |
| GT.9 | Minimum width of a GT region for 3.3V NMOS | 0.35 |
| GT.10a | Maximum length of salicide poly on STI between two contacts when poly width ≤ 0.24um | 50 |
| GT.10b | Maximum length of salicide poly on STI between one contact and poly line end when poly width ≤ 0.24um | 50 |
| GT.11a | 90° bends on active area are not allowed. | |
| GT.11b | GT must enter AA region perpendicularly | |
| GT.12 | Minimum GT density must be greater than or equal to 14%. | |
| GT.13 | Minimum space between two GT's with CT on active area. | 0.375 |
| GT.14 | Minimum channel length of 1.8V device poly gate on AA with 45° bent. | 0.21 |

**Recommendation:**
**If GT density is less than 14%, please add GT dummy on STI. The dummy pattern generation can refer to SMIC dummy rule.**

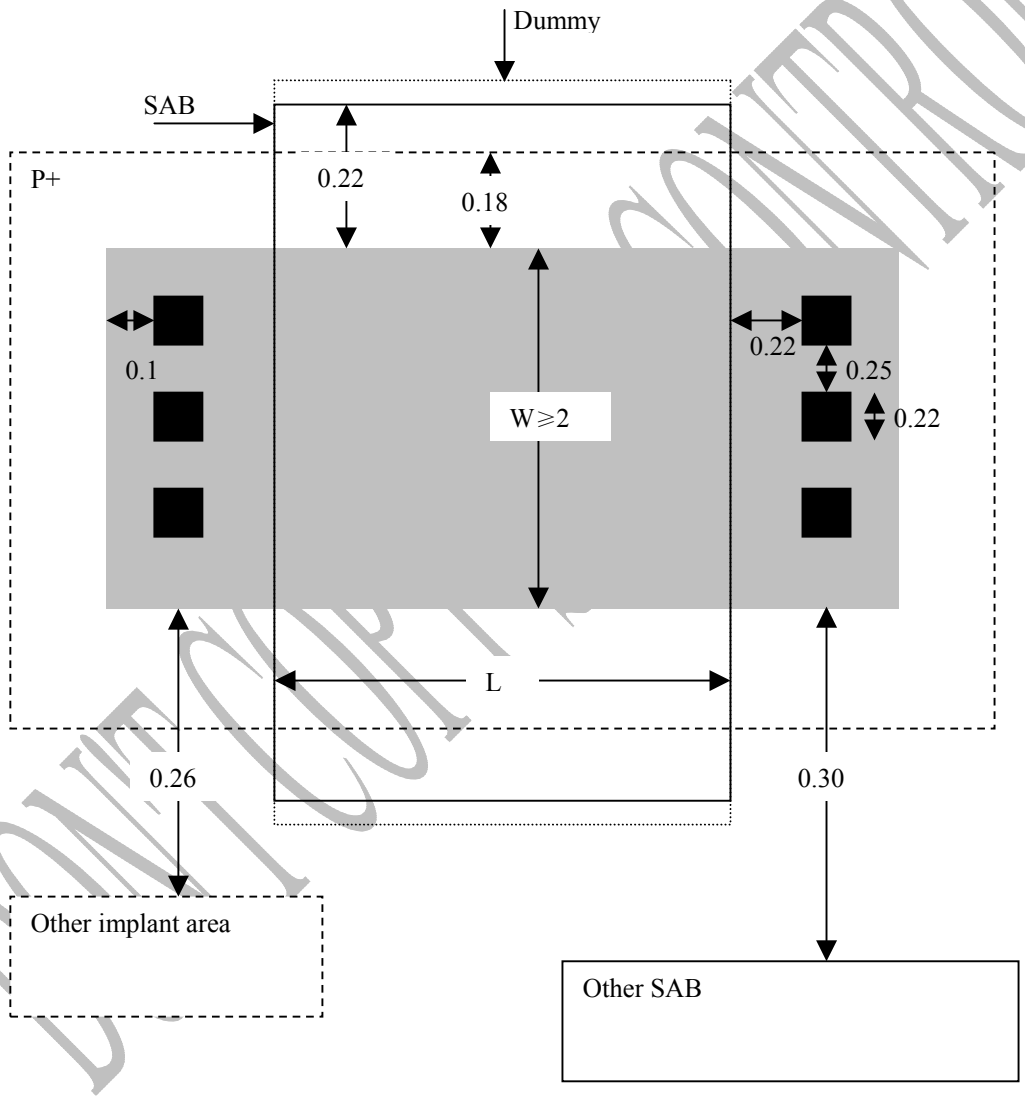




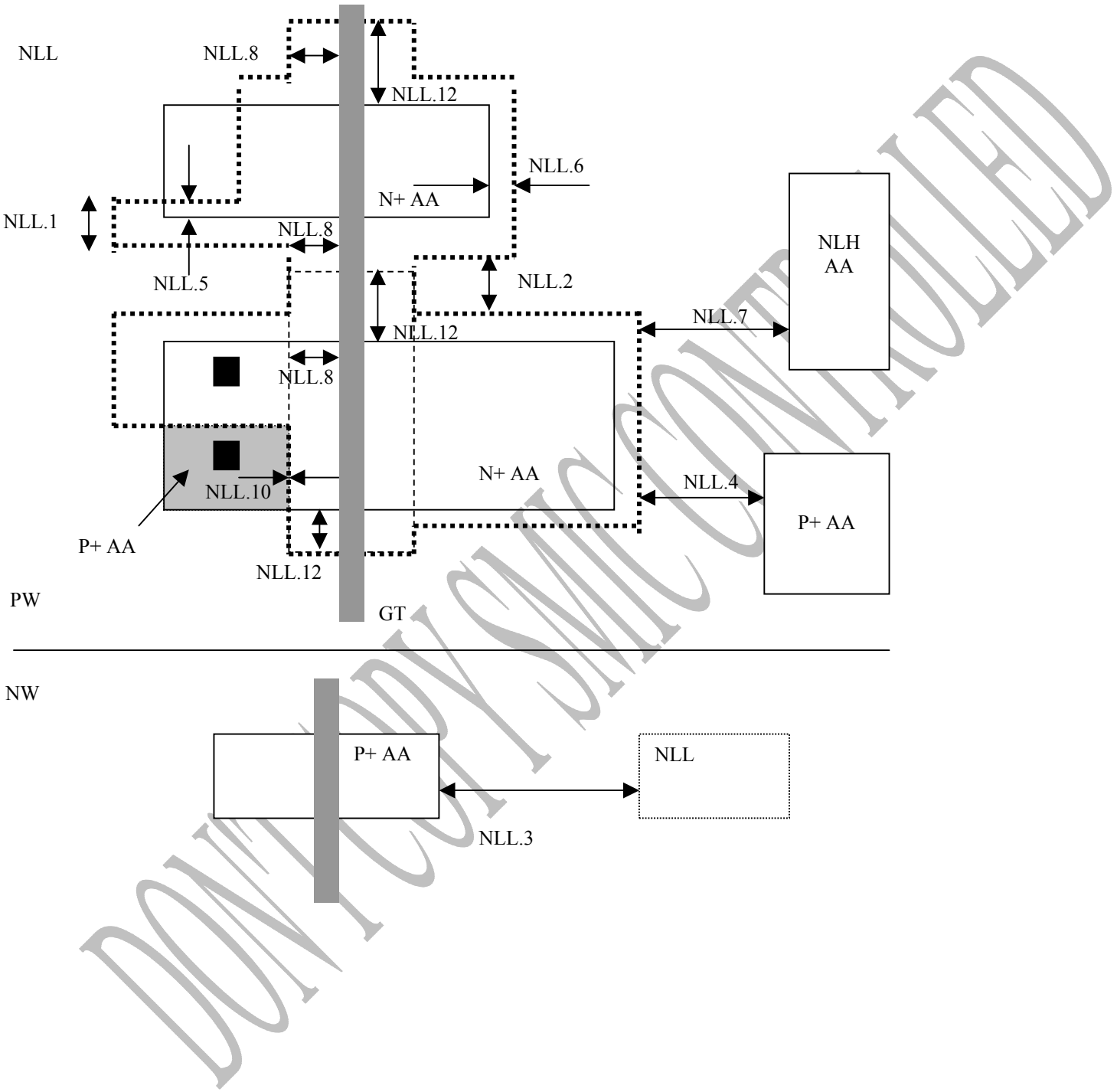
### 1.8 Poly resistor design rule recommendation

a. The resistor width is larger than 2.0µm and Nsq>=5
b. The separation from SAB to contact on poly must be equal to 0.22µm
c. The space from an un-related SAB to a resistor poly must be larger than or equal to 0.3µm
d. The minimum separation between resistors and un-related implant region is 0.26µm
e. The contact to pick-up poly resistor should be a single column
f. Can not use dog-bone at the end of poly resistor for contact pick-up
g. PLL, NLL, PLH and NLH implant are not allowed in N+ and P+ poly resistor



### 1.9 NLL — 1.8V NLDD implantation

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| NLL.1 | Minimum width of an NLL region | 0.44 |
| NLL.2 | Minimum space between two NLL regions. Merge if the space is less than 0.44µm | 0.44 |
| NLL.3 | Minimum space between an NLL region and a P+ AA region | 0.26 |
| NLL.4 | Minimum space between an NLL region and a P+ pick-up AA region | 0.10 |
| NLL.5 | Minimum overlap from an NLL edge to an AA | 0.23 |
| NLL.6 | Minimum enclosure of an NLL region over SN active region | 0.18 |
| NLL.7 | Minimum space between an NLL region and an NLH AA region | 0.21 |
| NLL.8 | Minimum enclosure of an NLL region to an N-channel poly gate | 0.32 |
| NLL.9 | Minimum area of an NLL region | 0.40 |
| NLL.10 | Separation from an NLL to a butted edge of a butted diffusion P+ AA (inside P-Well) | 0.00 |
| NLL.11 | Minimum space between NLL and NLH if two AAs are overlapped | 0.00 |
| NLL.12 | Minimum enclosure of an NLL region over N-channel along the direction of poly gate | 0.35 |
| NLL.13 | Minimum NLL area for a N-channel poly gate must follow NLL.8 and NLL.12 | |
| NLL.14 | NLL implant is not allowed in non-salicide AA/Poly resistor region. | |



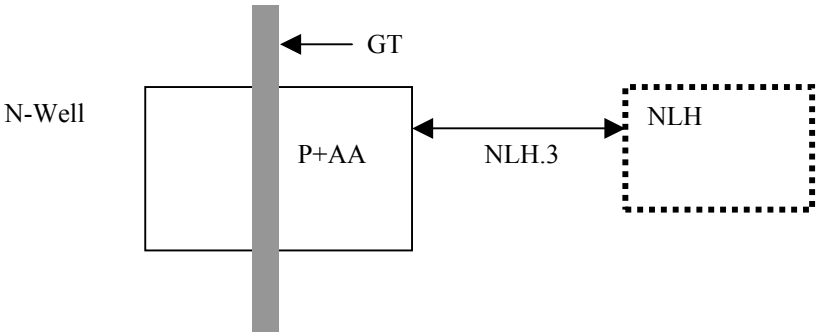
### 1.10 PLL — 1.8V PLDD Implantation

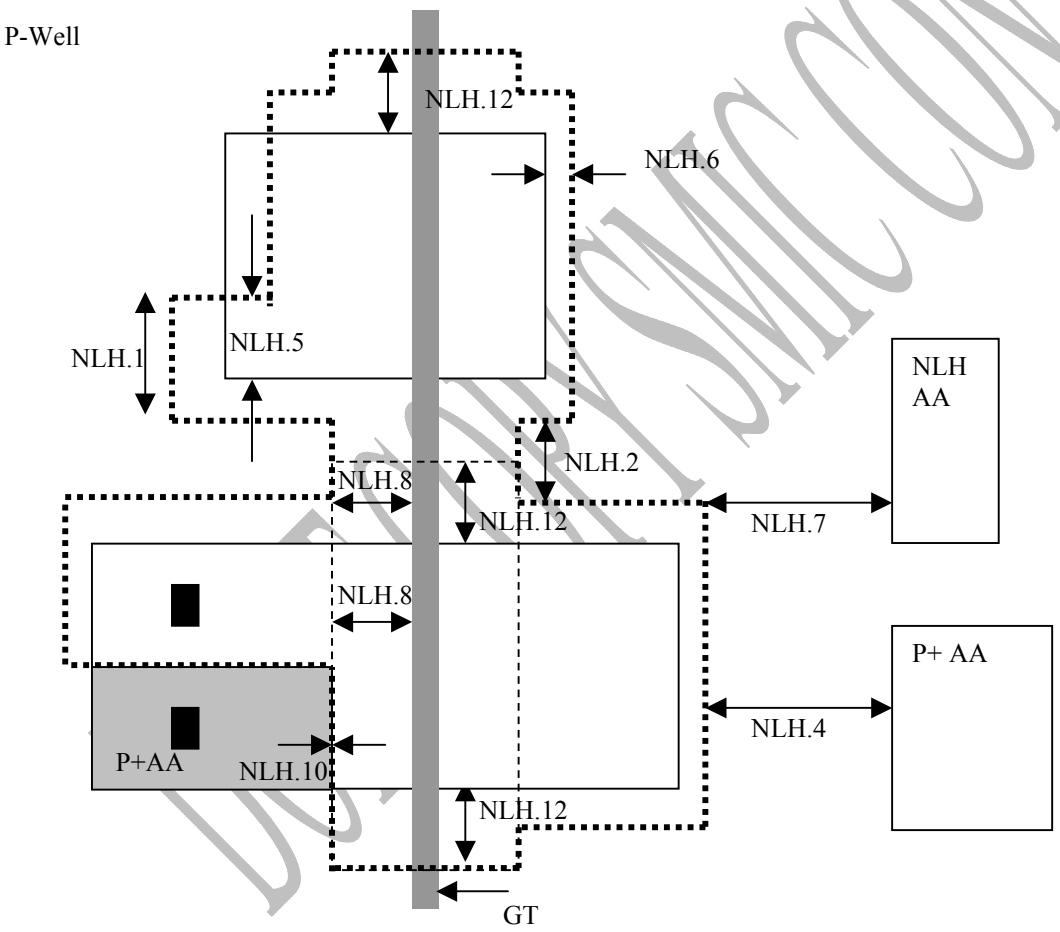
| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| PLL.1 | Minimum width of a PLL region | 0.44 |
| PLL.2 | Minimum space between two PLL regions. Merge if the space is less than 0.44µm | 0.44 |
| PLL.3 | Minimum space from a PLL region to an N+ AA region. (inside Pwell) | 0.26 |
| PLL.4 | Minimum space from a PLL region to an N+ pick-up AA region. | 0.10 |
| PLL.5 | Minimum overlap from a PLL edge to an AA | 0.23 |
| PLL.6 | Minimum enclosure of a PLL region beyond a SP active region | 0.18 |
| PLL.7 | Minimum space of a PLL region to a PLH AA region | 0.21 |
| PLL.8 | Minimum enclosure of a PLL region to a P-channel poly gate | 0.32 |
| PLL.9 | Minimum area of a PLL region | 0.40 |
| PLL.10 | Separation from a PLL to a butted edge of a butted diffusion N+ AA (inside N-Well) | 0.00 |
| PLL.11 | Minimum space between PLL and PLH if two AAs are overlapped | 0.00 |
| PLL.12 | Minimum enclosure of a PLL region of P-channel along the direction of poly gate | 0.35 |
| PLL.13 | Minimum PLL area for a P-channel poly gate must follow PLL.8 and PLL.12 | |
| PLL.14 | PLL implant is not allowed in non-salicide AA/Poly resistor region | |

Diagram refers to section 1.9 and change N+ AA to P+AA, P+AA to N+AA, PW to NW and NW to PW, NLL to PLL and NLH to PLH

### 1.11 NLH — 3.3V NLDD Implantation

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| NLH.1 | Minimum width of an NLH region | 0.44 |
| NLH.2 | Minimum space between two NLH regions. Merge if the space is less than 0.44µm | 0.44 |
| NLH.3 | Minimum space between an NLH region and a P+ AA region (inside N-well). | 0.26 |
| NLH.4 | Minimum space between an NLH region and a Pwell pick-up P+ AA region. | 0.10 |
| NLH.5 | Minimum overlap from an NLH edge to an AA | 0.23 |
| NLH.6 | Minimum enclosure of an NLH region beyond an NP active region | 0.18 |
| NLH.7 | Minimum space between an NLH region and an NLL AA region | 0.21 |
| NLH.8 | Minimum enclosure of an NLH region to an N-channel | 0.32 |
| NLH.9 | Minimum area of an NLH region | 0.40 |
| NLH.10 | Separation from an NLH to a butted edge of a butted diffusion P+ AA (inside P-Well) | 0.00 |
| NLH.11 | Minimum space between NLL and NLH if two AAs are overlapped | 0.00 |
| NLH.12 | Minimum enclosure of an NLL region to N-channel along the direction of poly gate | 0.35 |
| NLH.13 | Minimum NLH area for a N-channel poly gate must follow NLH.8 and NLH.12 | |
| NLH.14 | NLH implant is not allowed in non-salicide AA/Poly resistor region | |



### 1.12 PLH — 3.3V PLDD implantation

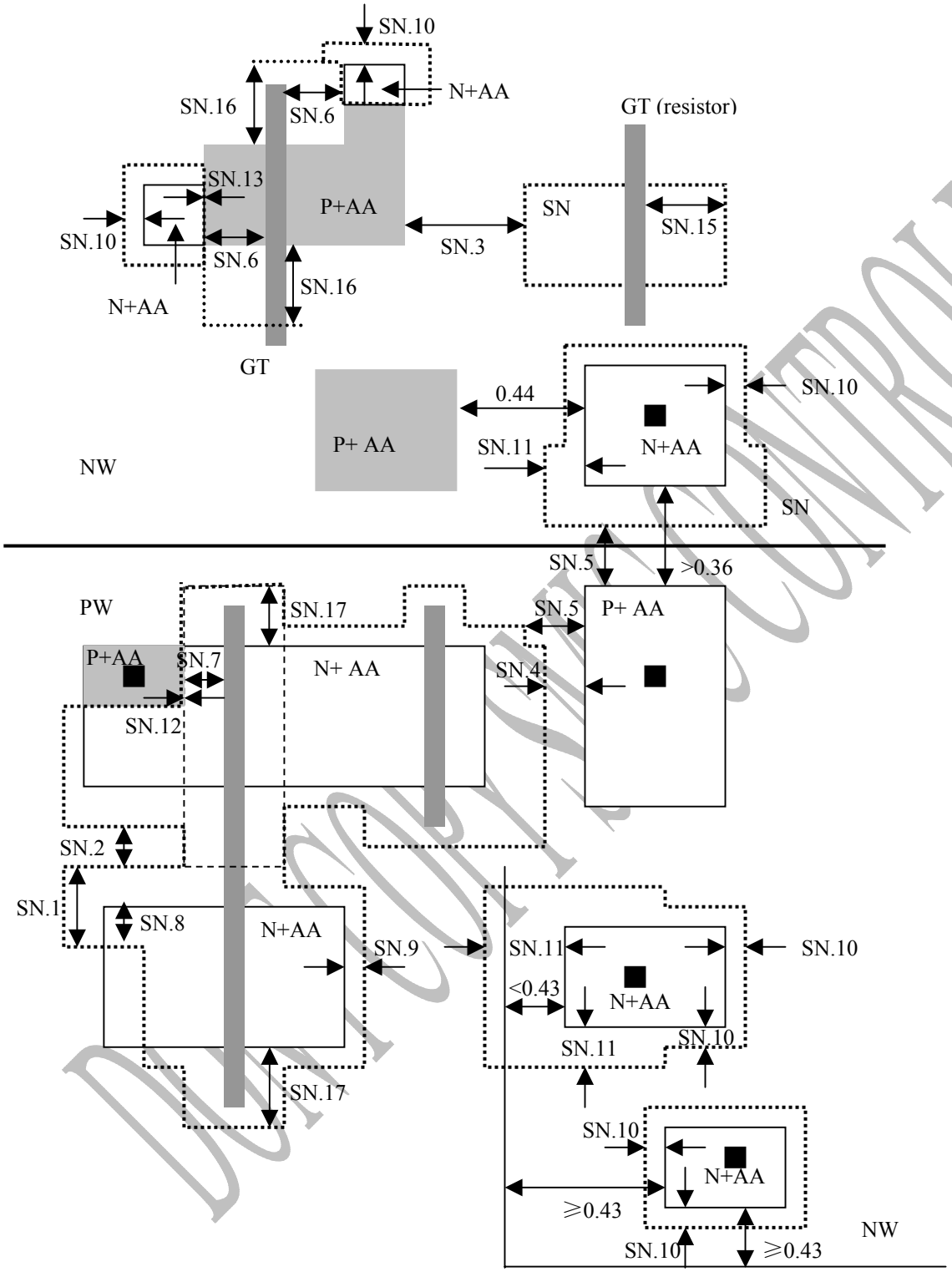
| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| PLH.1 | Minimum width of a PLH region | 0.44 |
| PLH.2 | Minimum space between two PLH regions. Merge if the space is less than 0.44µm | 0.44 |
| PLH.3 | Minimum space between a PLH region and an N+ AA region. (inside Pwell) | 0.26 |
| PLH.4 | Minimum space between a PLH region and an N+ pick-up AA region. | 0.10 |
| PLH.5 | Minimum overlap from a PLH edge to an AA | 0.23 |
| PLH.6 | Minimum enclosure of a PLH region beyond a SP active region | 0.18 |
| PLH.7 | Minimum space between a PLH region and a PLL AA region | 0.21 |
| PLH.8 | Minimum enclosure of a PLH region to a P-channel poly gate | 0.32 |
| PLH.9 | Minimum area of a PLH region | 0.40 |
| PLH.10 | Separation from a PLH to butted edge of a butted N+ AA (inside N-Well) | 0.00 |
| PLH.11 | Minimum space between PLL and PLH if two AAs are overlapped | 0.00 |
| PLH.12 | Minimum enclosure of an PLL region to P-channel along the direction of poly gate | 0.35 |
| PLH.13 | Minimum PLH area for a P-channel poly gate must follow PLH.8 and PLH.12 | |
| PLH.14 | PLH implant is not allowed in non-salicide AA/Poly resistor region | |

Diagram refers to section 1.11 and replaces N+ as P+, P+ as N+ and NLH as PLH, P-well as N-well, N-well as P-well.

### 1.13 SN — S/D Implantation

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| SN.1 | Minimum width of an SN region | 0.44 |
| SN.2 | Minimum space between two SN regions. Merge if space is less than 0.44µm | 0.44 |
| SN.3 | Minimum space between a SN region and a P+ AA region. (inside N-well) | 0.26 |
| SN.4 | Minimum space between a SN region and a non-butted edge of P+ pick-up AA region if the distance between P+AA and N-well >=0.43µm. | 0.10 |
| SN.5 | Minimum space between a SN region and a non-butted edge of P-well pick-up P+AA region if the distance between P+AA and N-well <0.43µm | 0.18 |
| SN.6 | Minimum space from a SN edge to a P-channel Poly gate. | 0.32 |
| SN.7 | Minimum enclosure of a SN edge to an N-channel Poly gate. | 0.32 |
| SN.8 | Minimum overlap from a SN edge to an AA | 0.23 |
| SN.9 | Minimum enclosure of a SN region beyond a SN active region | 0.18 |
| SN.10 | Minimum enclosure of a SN region beyond an N+ pick-up AA region if the distance between N+AA and P-Well >=0.43µm | 0.02 |
| SN.11 | Minimum enclosure of a SN region beyond an N+ pick-up AA region if the distance between N+AA and P-Well < 0.43µm<br>a. To obey this rule and SN.3 simultaneously, the minimum space between N+ pick-up AA and SP active AA should be increased to 0.44µm<br>b. To obey this rule and SN.5 simultaneously, the minimum space between N+ pick-up AA and SP active AA should be increased to 0.36µm | 0.18 |
| SN.12 | Separation from a SN region to butted edge of a butted diffusion SP AA (inside P-well) | 0.00 |
| SN.13 | Minimum extension of a SN region along the edge of a butted diffusion N+AA/P+AA | 0.00 |

| | | |
|---|---|---|
| SN.14 | Minimum area of a SN region | 0.40um$^2$ |
| SN.15 | Minimum extension of a SN region beyond a poly as a resistor. SAB poly without SN or SP implant is not allowed. | 0.18 |
| SN.16 | Minimum space from a SN edge to a P-channel Poly gate along the direction of poly gate. | 0.35 |
| SN.17 | Minimum enclosure of a SN edge to a N-channel Poly gate along the direction of poly gate. | 0.35 |
| SN.18 | SN is not allowed to overlap with SP | |
| SN.19 | It is prohibited that SN being generated by the reverse tone of SP, since this operation might violate SN.3 and SN.4 | |
| SN.20 | Minimum SN area for a N-channel poly gate must follow SN.7 and SN.17 | |



### 1.14 SP — S/D Implantation

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| SP.1 | Minimum width of a SP region | 0.44 |
| SP.2 | Minimum space between two SP regions. Merge if the space is less than 0.44µm | 0.44 |
| SP.3 | Minimum space between a SP region and a N+ AA region (inside P-well) | 0.26 |
| SP.4 | Minimum space between a SP region and a non-butted edge of N+ pick-up AA region if the distance between N+AA and P-well >=0.43µm. | 0.10 |
| SP.5 | Minimum space between a SP region and a non-butted edge of N-well pick-up N+AA region if the distance between N+AA and P-well <0.43µm | 0.18 |
| SP.6 | Minimum space from a SP edge to N-channel Poly gate. | 0.32 |
| SP.7 | Minimum enclosure of a SP edge to P-channel Poly gate. | 0.32 |
| SP.8 | Minimum overlap from a SP edge to an AA | 0.23 |
| SP.9 | Minimum enclosure of a SP region beyond a SP active region | 0.18 |
| SP.10 | Minimum enclosure of a SP region beyond a P-Well pick-up P+AA region if the distance between P+AA and N-Well >=0.43µm | 0.02 |
| SP.11 | Minimum enclosure of a SP region beyond a P-Well pick-up P+AA region if the distance between P+AA and N-Well < 0.43µm<br>c. To obey this rule and SP.3 simultaneously, P+ pick-up AA to SN active AA minimum spacing must be increased to 0.44µm<br>d. To obey this rule and SP.5 simultaneously, P+ pick-up AA to SN pick-up AA minimum spacing must be increased to 0.36µm | 0.18 |
| SP.12 | Separation from a SP region to butted edge of a butted diffusion SN AA (inside N-well) | 0.00 |
| SP.13 | Minimum extension of a SP region along the edge of a butted diffusion P+AA/N+AA | 0.00 |
| SP.14 | Minimum area of a SP region | 0.40um$^2$ |

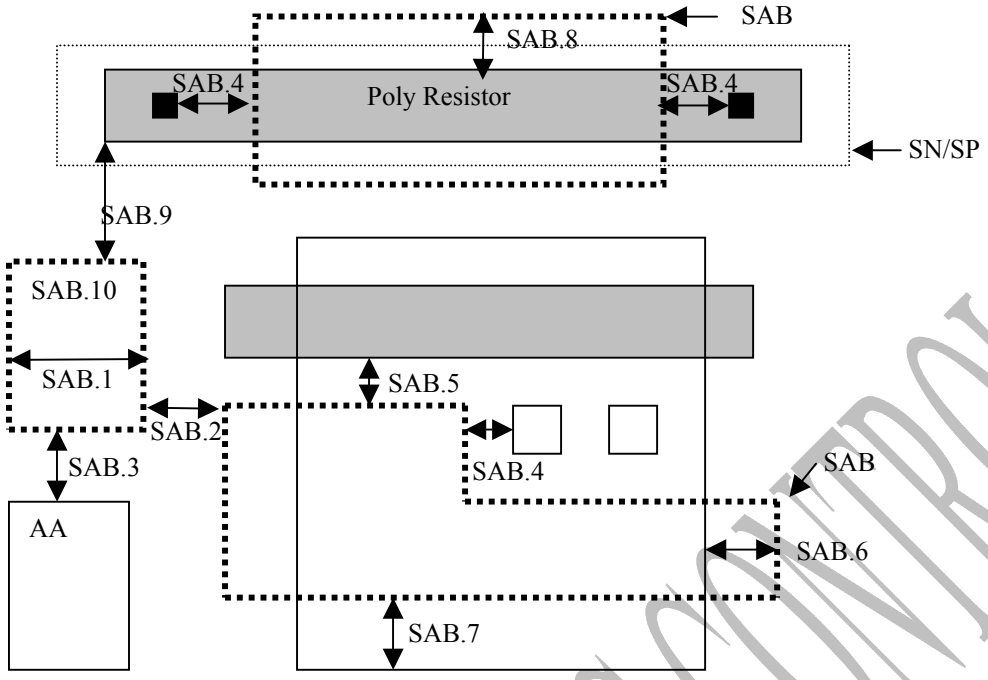
| | | |
|---|---|---|
| SP.15 | Minimum extension of a SP region beyond a poly as a resistor. SAB poly without SN or SP implant is not allowed. | 0.18 |
| SP.16 | Minimum space from a SP edge to N-channel Poly gate along the direction of poly gate | 0.35 |
| SP.17 | Minimum enclosure of a SP edge to P-channel Poly gate along the direction of poly gate | 0.35 |
| SP.18 | SP is not allowed to overlap with SN | |
| SP.19 | It is prohibited that SP is generated by the reverse tone of SN, since this operation might violated SP.3 and SP.4 | |
| SP.20 | Minimum SP area for a P-channel poly gate must follow SP.7 and SP.17 | |

Diagram refers to section 1.13 and replaces SP as SN, P+AA as N+AA, N-Well as P-Well.

### 1.15 SAB — Salicide Block

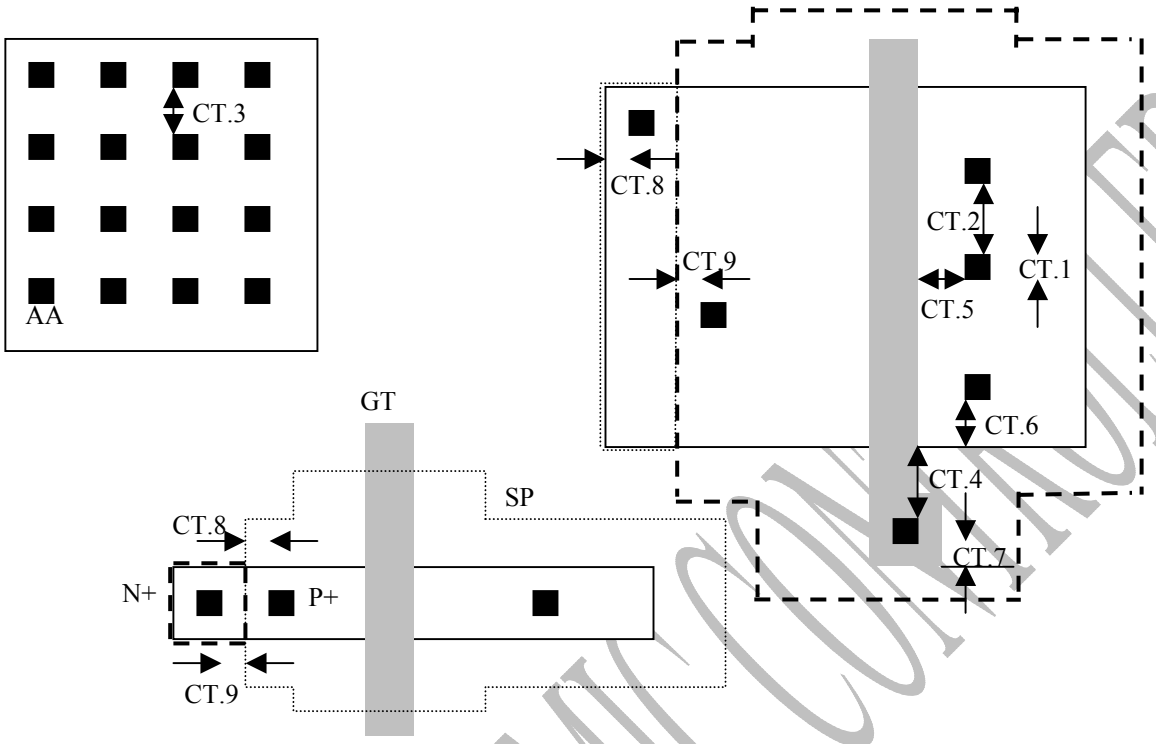
| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| SAB.1 | Minimum width | 0.43 |
| SAB.2 | Minimum space | 0.43 |
| SAB.3 | Minimum space to unrelated diffusion | 0.22 |
| SAB.4 | Minimum space to contact | 0.22 |
| SAB.5 | Minimum space to poly on diffusion | 0.45 |
| SAB.6 | Minimum extension over related diffusion | 0.22 |
| SAB.7 | Minimum extension of diffusion over related SAB | 0.22 |
| SAB.8 | Minimum extension of SAB over related poly on field oxide | 0.22 |
| SAB.9 | Minimum space of SAB to unrelated poly on field oxide | 0.30 |
| SAB.10 | Minimum area of SAB | 2.00um$^2$ |

Note:
1 Follow poly resistor guideline, if poly resistor is used.
2 Follow ESD guideline, if SAB is used in ESD.



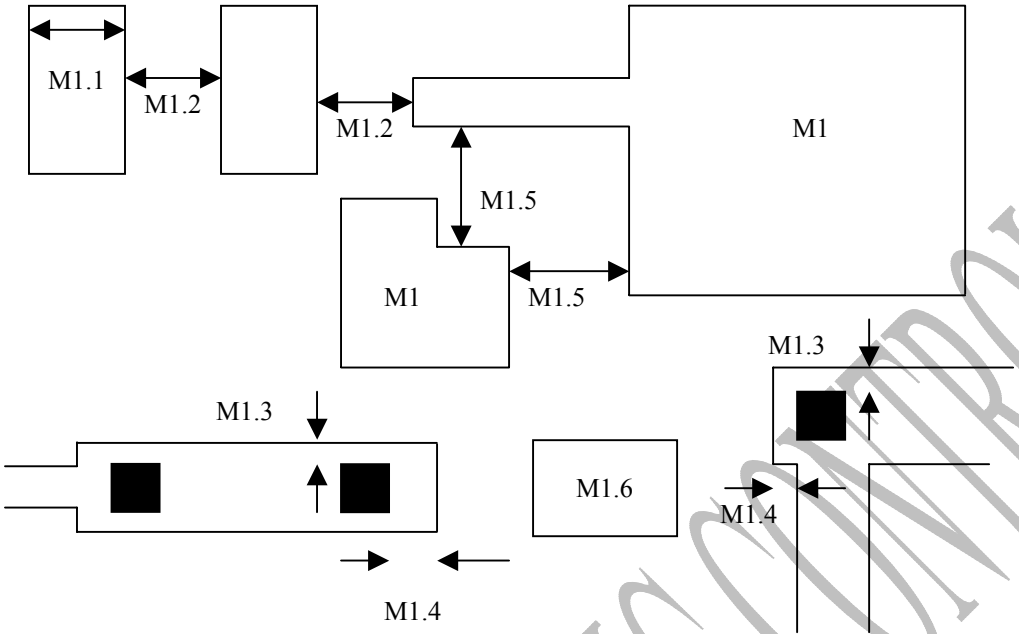
### 1.16 CT — Contact

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| CT.1 | Minimum/maximum contact size | 0.22 |
| CT.2 | Minimum space between two contacts | 0.25 |
| CT.3 | Minimum space between two contacts in a contact array with row and column numbers are both greater than 3 | 0.28 |
| CT.4 | Minimum space between poly contact to AA | 0.20 |
| CT.5 | Minimum space between poly gate to diffusion contact | 0.16 |
| CT.6 | Minimum enclosure of an AA region beyond an AA CT region | 0.10 |
| CT.7 | Minimum enclosure of a poly region beyond a poly CT region | 0.10 |
| CT.8 | Minimum enclosure of a SP region beyond an AA CT region | 0.12 |
| CT.9 | Minimum enclosure of an SN region beyond an AA CT region | 0.12 |
| CT.10 | CT on gate region is forbidden | |
| CT.11 | AA contact located on SN/SP boundary is not allowed | |
| CT.12 | Non-salicided contacts are not allowed | |

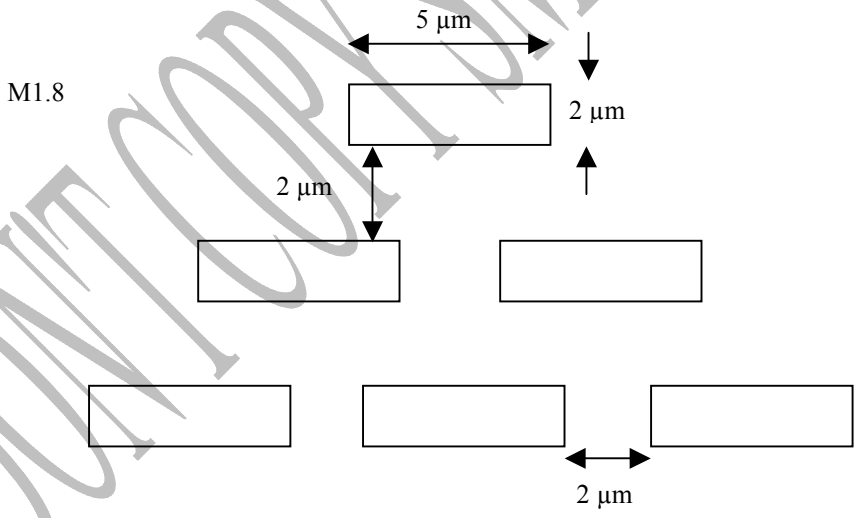


### 1.17 Metal 1

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| M1.1 | Minimum width of M1 region | 0.23 |
| M1.2 | Minimum space between two M1 regions | 0.23 |
| M1.3 | Minimum enclosure of M1 region over CT region | 0.005 |
| M1.4 | Minimum enclosure of M1 line end region beyond CT region<br>For CT at 90 degrees corner, one side of metal enclosure must be considered as line end region. | 0.06 |
| M1.5 | Minimum space between Ml lines with one or both metal line width and length are greater than 10µm; the minimum space must be maintained between a metal line and a small piece of metal (<10µm) that is connected to the wide metal within 1.0µm range from the wide metal | 0.60 |
| M1.6 | Minimum area of M1 region | 0.20um$^2$ |
| M1.7 | Minimum density of M1 area<br>Density is calculated as [total metal layout area]/[chip area]<br>Dummy pattern is required for those with M1 density less than 30%. | 30% |
| M1.8 | For dummy metal pattern, please check SMIC dummy rule. | |

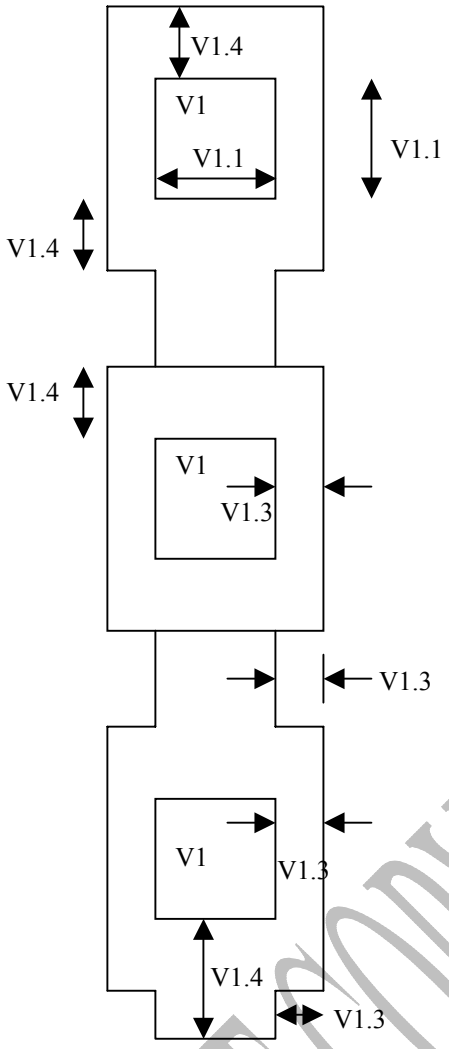


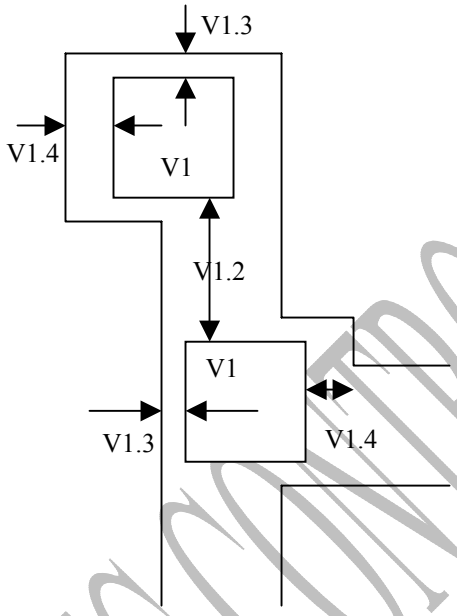

Example of dummy Pattern



### 1.18 Via1

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| V1.1 | Minimum/maximum size of a V1 | 0.26 |
| V1.2 | Minimum space between two V1 | 0.26 |
| V1.3 | Minimum metal 1 enclosure for a V1 | 0.01 |
| V1.4 | If Metal 1 line end beyond V1<br>For V1 located at the 90 degree corner, one side of metal extension must be treated as end-of-line and the other side follows V1.3 | 0.06 |
| V1.5 | Stacked Via's and contacts are allowed | |



### 1.19 Metal n (n=2,3,4,5)

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| Mn.1 | Minimum width of an Mn region | 0.28 |
| Mn.2 | Minimum space between two Mn regions | 0.28 |
| Mn.3 | Minimum extension of Mn region beyond Vn-1 region | 0.01 |
| Mn.4 | Minimum extension of Mn line end region beyond Vn-1 region<br>For Vn-1 located at 90 degree corner, one side of metal extension must be treated as end-of-line, the other side follow Mn.3. | 0.06 |
| Mn.5 | Minimum space between metal lines with one or both metal line width and length are greater than 10µm; the minimum space must be maintained between a metal line and a small piece of metal (<10µm) that is connected to the wide metal within 1.0µm range from the wide metal | 0.60 |
| Mn.6 | Minimum area of a Mn region | 0.20um$^2$ |
| Mn.7 | Minimum density of Mn area<br>Density is calculated as [total metal layout area]/[chip area]<br>Dummy pattern is required for those with Mn density less than 30%. | 30% |
| Mn.8 | As to metal dummy pattern, please check SMIC Dummy rule. | |

### 1.20 Via n (n=2,3,4)

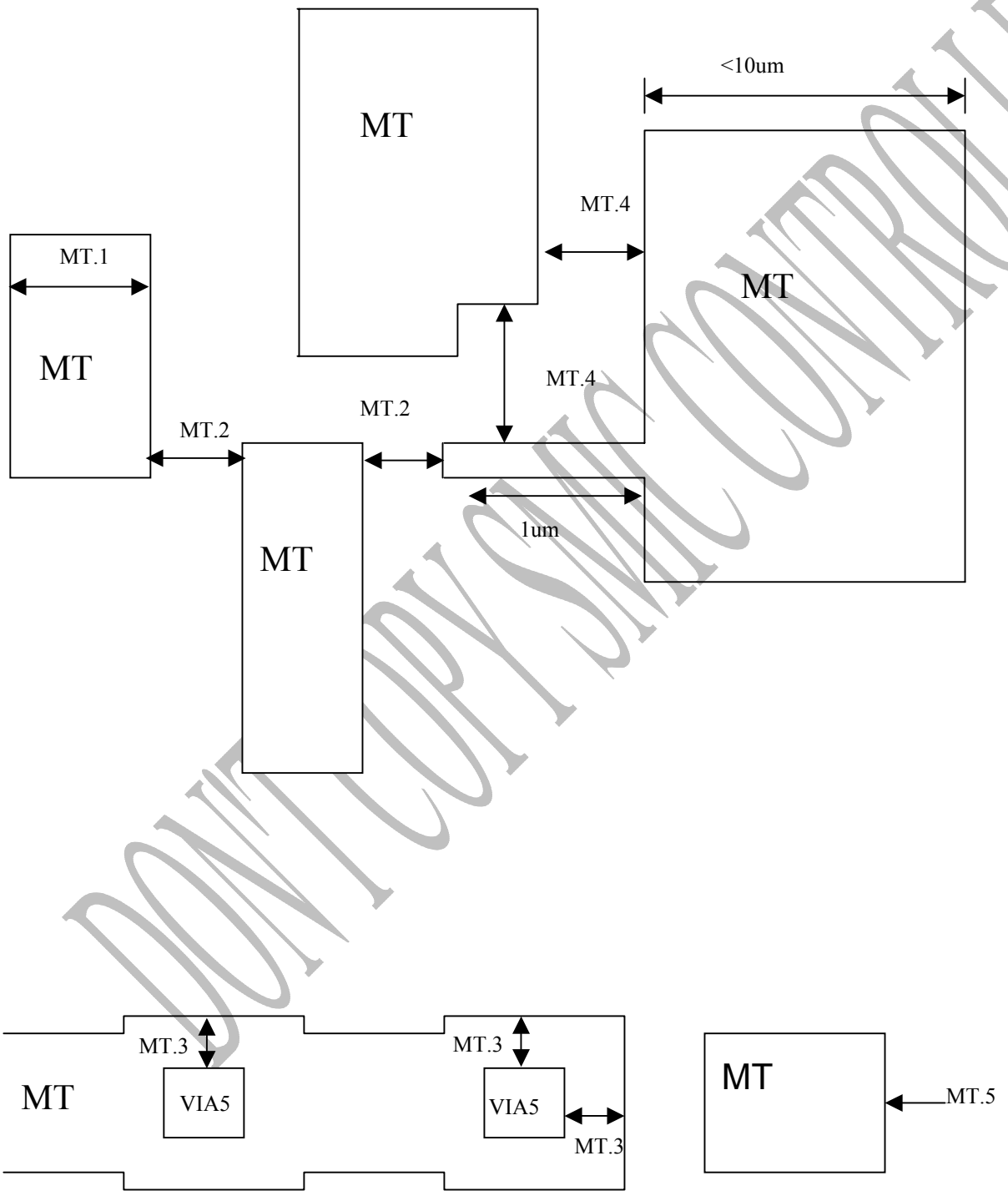
| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in μm) |
|---|---|---|
| **Layer** | **Vn --- Via n n=2,3,4** | |
| | Vn can be located at any region | |
| Vn.1 | Minimum/maximum size of a Vn | 0.26 |
| Vn.2 | Minimum space between two Vn | 0.26 |
| Vn.3 | Minimum Mn enclosure for a Vn | 0.01 |
| Vn.4 | Minimum enclosure of Mn over Vn along metal line direction | 0.06 |
| | For Vn located at the 90 degree corner, one side of metal extension must be treated as end-of-line and the other side follows Vn.3 | |
| Vn.5 | Vn can be fully or partially stacked on Vn-1, any stacked structure such as stacked Vn/Vn-1/…/CT | |

### 1.21 Via 5

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| V5.1 | Minimum/maximum size of a V5 | 0.36 |
| V5.2 | Minimum space between two V5 | 0.35 |
| V5.3 | Minimum M5 enclosure for a V5 | 0.01 |
| V5.4 | Minimum enclosure of M5 over V5 along metal line direction<br>For V5 located at the 90 degree corner, one side of metal extension must be treated as end-of-line and the other side follows V5.3 | 0.06 |
| V5.5 | V5 can be fully or partially stacked on V4, V3, V2, V1, any stacked structure such as stacked V5/V4/V3/V2/V1/CT | |

### 1.22 Top Metal—Metal 6

| RULE NO. | DESCRIPTION | LAYOUT RULE (Unit in µm) |
|---|---|---|
| **Layer** | **MT -- Top Metal** | |
| MT.1 | Minimum width of a top metal region | 0.44 |
| MT.2 | Minimum space between two top metal regions | 0.46 |
| MT.3 | Minimum extension of M6 region over V5 | 0.09 |
| MT.4 | Minimum space between top metal lines with one or both metal line width and length are greater than 10µm; this also includes all metals attached to these areas or extending out for a distance of 1.0µm or less | 0.60 |
| MT.5 | Minimum area of an M6 region | 0.56um$^2$ |
| MT.6 | Minimum density of metal n area<br>Density is calculated as [total metal layout area]/[chip area]<br>Dummy pattern is required for those with MT density less than 30%. | 30% |
| MT.7 | As to MT dummy pattern, please check SMIC Dummy rule. | |



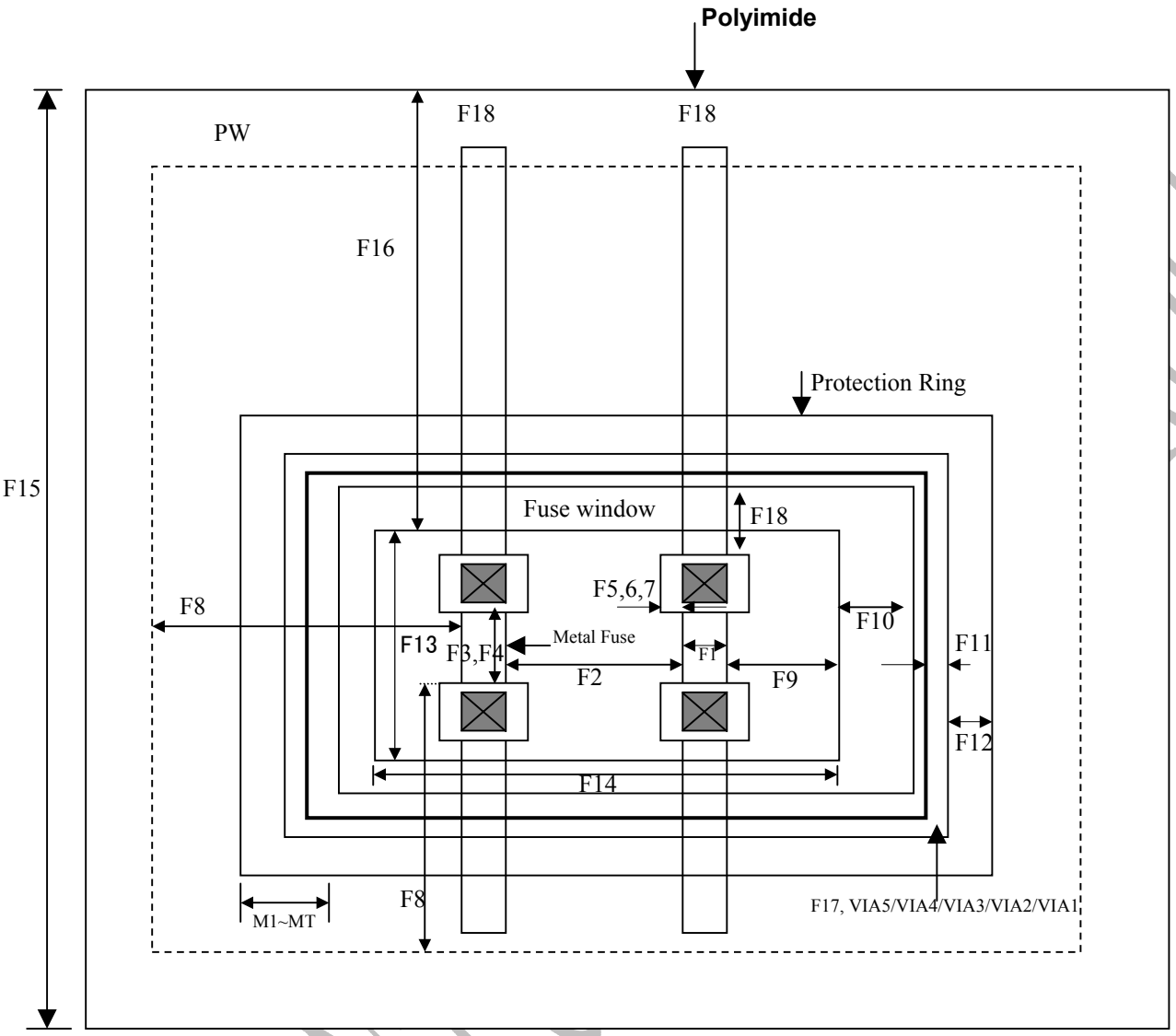
## 2.0 Metal Fuse, Alignment Mark for Laser Repairing and Stress Relief

### 2.1 Metal Fuse Rules

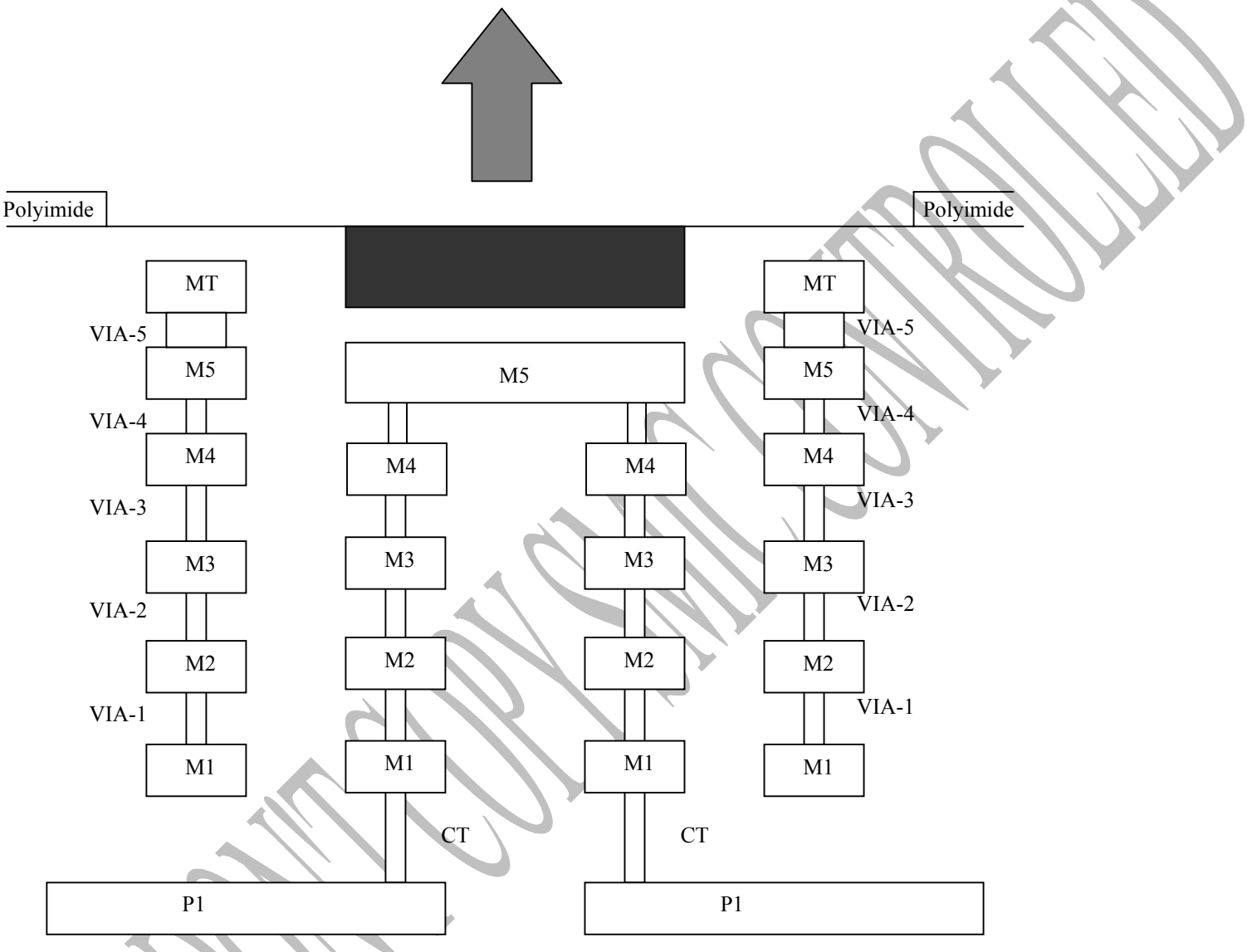
| RULE NO. | DESCRIPTION | LAYOUT GUIDELINE (Unit in μm) |
|---|---|---|
| Fuse.1 | Width of metal fuse | 0.80 |
| Fuse.2 | Minimum space of metal fuse | 4.00 |
| Fuse.3 | Minimum length of metal fuse | 4.00 |
| Fuse.4 | Maximum length of metal fuse | 10 |
| Fuse.5 | Minimum extension from GT to CT | 0.30 |
| Fuse.6 | Minimum extension from M1 to CT | 0.30 |
| Fuse.7 | Minimum extension from M1 to MT-1 to CT/V1~V3 (stacked via) | 0.30 |
| Fuse.8 | Min. separation from fuse edge to p-well edge (p-type substrate are used) | 8.00 |
| Fuse.9 | Min. separation from fuse to fuse window | 3.50 |
| Fuse.10 | Min. separation from fuse window to protection ring | 1.50 |
| Fuse.11 | Width of V1~Vx-1 in protection ring | 0.26 |
| | Width of Vx-1 in protection ring | 0.36 |
| Fuse.12 | Minimum extension from M1~Mx to V1~Vx-1 in protection ring | 0.40 |
| Fuse.13 | Minimum width of fuse window | 5.00 |
| Fuse.14 | Minimum length of fuse window | 20 |
| Fuse.15 | Minimum width of polyimide opening | 30 |
| Fuse.16 | Min. extension from polyimide window to passivation window | 12 |
| Fuse.17 | Min. separation between Via's inside protection ring | 0.00 |
| Fuse.18 | Min. separation from metal island to protection ring | 1.00 |

Metal Fuse Rule

- **In 1PxM process, MT-1 is required to be used as fuse.**
  **For Example:**
  **In 1P5M process, M4 is required to be used as fuse.**
  **In 1P4M process, M3 is required to be used as fuse.**
  **In 1P3M process, M2 is required to be used as fuse.**
  **In 1P2M process, M1 is required to be used as fuse.**
- **Metal fuse has to be connected to P1 through stacked Via/contact.**
- **Alignment Mark should be located at each corner of the chip.**
- **Alignment Mark should follow the Alignment Mark Rule for laser repairing.**



## Fuse (Metal) Window Cross Section




***1.1.1 Field***

**P-WELL**

**2.2 Alignment Mark for Laser Repairing**

L mark should be on each corner of a chip
L mark should be the top metal layer and with passivation open above the target
L mark should be surrounded by protection ring
L mark and its protection ring can replace corner dummy pads to serve as stress-relieve structure, i.e. alignment marks do not occupy extra die area.

| RULE NO. | DESCRIPTION | LAYOUT GUIDELINE (Unit in µm) |
|---|---|---|
| Mark.1 | Minimum width of mark | 10 |
| Mark.2 | Minimum length of mark | 40 |
| Mark.3 | Min. separation from a mark to the protection opening | 30 |
| Mark.4 | Min. separation from passivation opening to protection ring | 1.50 |
| Mark.5 | Min. and max. width of V1/V2/V3/V4 in protection ring | 0.36 |
| Mark.6 | Min. extension from M1/M2/M3/M4/M5 to V1/V2/V3/V4 | 0.40 |

8.Attachment: N/A