

# EE113B Final Design Report

## MPPT PV Buck Converter Design

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# 1 Introduction

## 1.1 Design Specifications and Application

The objective of this project is to design and implement a high-efficiency MPPT (Maximum Power Point Tracking) DC-DC power converter for interfacing with a photovoltaic (PV) module. The converter should dynamically adjust its operating point to extract the maximum available power from the PV source under varying environmental conditions.

Key design specifications:

- **Input Voltage Range:** 16V–24V
- **Nominal Input Voltage:** 20V
- **Output Voltage:** 12V (regulated)
- **Output Power Range:** 50W–100W
- **Switching Frequency:** 100 kHz
- **Voltage Ripple (Input/Output):**  $\leq 5\%$
- **Inductor Current Ripple:**  $\leq 20\%$  at worst case

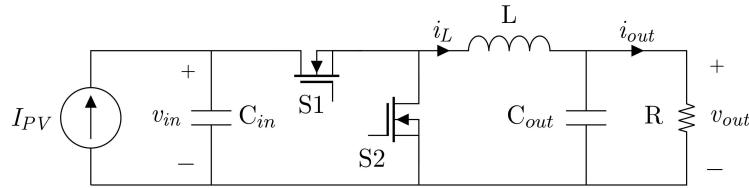


Figure 1: Synchronous Buck Converter Topology

This converter is suitable for solar-powered embedded systems, battery chargers, and off-grid microgeneration systems, where size, efficiency, and dynamic adaptability are critical.

## 1.2 Converter Topology and Schematic

The chosen topology is a **synchronous buck converter**, which efficiently steps down the voltage from the PV panel to a regulated output. It replaces the conventional diode with a second actively controlled switch, minimizing conduction losses and improving efficiency, especially under high-current operation.

This topology enables both precise voltage regulation and efficient power transfer, making it ideal for MPPT applications.

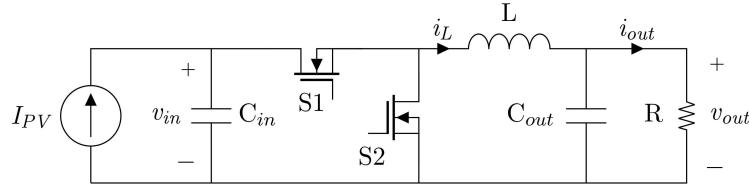


Figure 2: Synchronous Buck Converter Topology

### 1.3 Operating Sequence and Dead Time Description

The converter alternates between two switching states:

- **S1 ON, S2 OFF:** Energy is transferred from the PV panel to the output through the inductor. The inductor current increases.

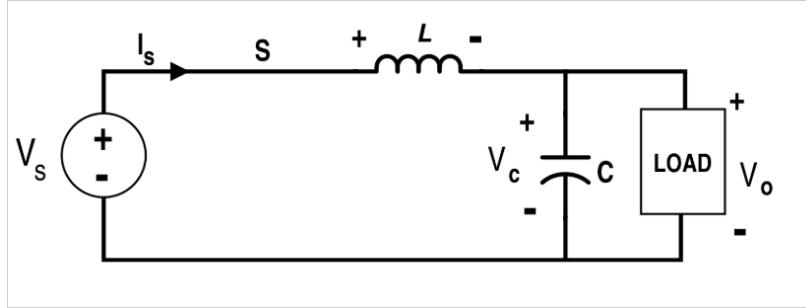


Figure 3: Circuit Diagram when S1 ON

- **S1 OFF, S2 ON:** The low-side switch provides a path for the inductor to discharge into the load. The inductor current decreases.

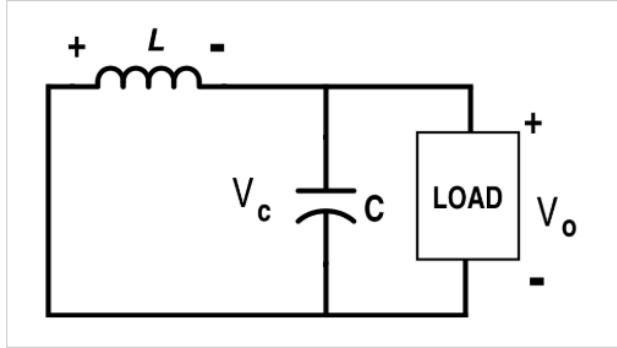


Figure 4: Circuit Diagram when S2 ON

- **DEADTIME:** During transitions, a short **dead time** is inserted to avoid overshoot just in case both switches are ON simultaneously. Since driving MOSFETs has to pass an RC filter ( $R_{gate}$  and  $C_{gate}$ ), the time constant  $\tau = RC$ , so that it depends on each MOSFET's parameters like  $C_g = C_{gs} + C_{gd}$  and  $R_{gate}$ , which is what we append on the gate driver IC.

We have to make sure the deadtime is large enough to minimize the overlapping loss, otherwise it would lead to a large overlapping loss like 5% of total input power. Additionally, the deadtime should not be too large, or the efficiency would decrease.

- **EQUILIBRIUM:** In an ideal buck converter, the output voltage is controlled by switching the input voltage on and off rapidly. The key idea is that the inductor averages the voltage over time.

During a switching period  $T_s$ , the high-side switch is ON for a fraction  $D$  (the duty cycle), so the inductor connects to  $V_{in}$  for  $D \cdot T_s$  and to ground for the rest.

By applying the **volt-second balance** on the inductor (which requires that the average voltage across it is zero in steady state), we get:

$$V_{\text{out}} = D \cdot V_{\text{in}}$$

## 1.4 Switching Frequency Decision and Tradeoffs

The switching frequency of the converter was selected as **100 kHz**, balancing efficiency, component sizing, and timing constraints.

The Texas Instruments C2000 microcontroller used in this design has an enhanced PWM (ePWM) module clocked at **100 MHz**. To maintain accurate PWM generation and adequate resolution, the switching frequency must be an integer divisor of this clock. A frequency of 100 kHz corresponds to a time-base period register value:

$$TBPRD = \frac{100\text{MHz}}{2 \cdot 100\text{kHz}} = 500$$

This value ensures stable duty cycle control and adequate dead time insertion using the ePWM module. If TBPRD is too small, ePWM may not have good control over a accurate duty cycle.

Another consideration is the switching characteristics of the MOSFETs. We have to make sure the MOSFET can have enough time to rise and fall. From the datasheet of IRL3705NPBF:

$$\begin{aligned} t_{\text{rise}} &= 140 \text{ ns} \\ t_{\text{on,delay}} &= 12 \text{ ns} \\ t_{\text{fall}} &= 78 \text{ ns} \\ t_{\text{off,delay}} &= 12 \text{ ns} \end{aligned}$$

Given  $V_{DD} = 28V$ ,  $I_D = 46A$ ,  $R_G = 1.8\Omega$ , we have above parameters, which is recommended to have the following maximum frequency:

$$\begin{aligned} T_{sw} &>= t_{\text{rise}} + t_{\text{on,delay}} + t_{\text{fall}} + t_{\text{off,delay}} = 242 \text{ ns} \\ f_{sw} &<= 1/T = 4.1322 \text{ MHz} \end{aligned}$$

### Tradeoffs considered:

- **Higher frequencies** (e.g., >200 kHz) allow smaller inductors and capacitors under the same ripple requirement, but increase switching losses (Coss losses, overlapping losses,...), which are all proportional to frequency and require faster gate drive circuitry.
- **Lower frequencies** (e.g., <50 kHz) reduce switching losses but require larger magnetic and capacitive components to meet the minimum ripple requirement, increasing board area and cost.

**Conclusion:** 100 kHz was chosen as a practical compromise:

- Compatible with the C2000 ePWM resolution and timing,
- Maintains low switching losses due to short transition times,
- Keeps passive components at a manageable size and cost,
- Minimizes EMI challenges that typically arise at higher frequencies.

## 2 Switches

### 2.1 Loss Analysis: Conduction, Coss, Overlap, and Reverse Recovery

All losses are calculated under nominal point ( $V_{in}=20V$ ,  $P=100W$ )

MOSFETs in a synchronous buck converter experience multiple sources of power loss, each of which must be accurately estimated to predict efficiency and ensure thermal safety. The key loss mechanisms include conduction loss, output capacitance (Coss) loss, overlap loss, and reverse recovery loss. Each of these is analyzed below for both the high-side and low-side switches.

#### 2.1.1 Conduction Loss

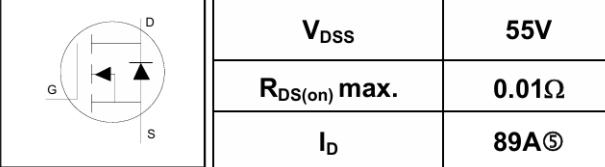
Conduction loss occurs when the MOSFET is ON and conducting current. It is calculated using:

$$P_{cond} = I_{rms}^2 \cdot R_{ds(on)}$$

The high-side and low-side switches conduct during complementary portions of the switching cycle:

$$I_{HS} = \sqrt{D} \cdot I_{out}, \quad I_{LS} = \sqrt{1 - D} \cdot I_{out}$$

Here,  $D$  is the duty cycle, and  $I_{out}$  is the load current. The on-resistance  $R_{ds(on)}$  is temperature-dependent and was adjusted using datasheet-provided temperature coefficients.



	<b><math>V_{DSS}</math></b>	<b>55V</b>
	<b><math>R_{DS(on)} \text{ max.}</math></b>	<b>0.01Ω</b>
	<b><math>I_D</math></b>	<b>89A<sup>⑤</sup></b>

Figure 5:  $R_{ds(on)}$  of IRL3705NPBF

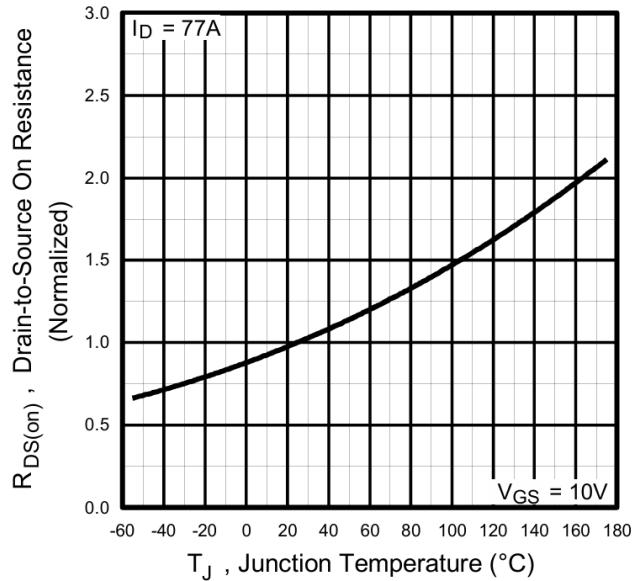


Figure 6:  $R_{ds(on)}$  of IRL3705NPBF, Temperature related

Assuming MOSFET is operating at about 60°C

$$\begin{aligned}
 P_{loss,HS} &= I_{S1,rms}^2 \cdot R_{ds,on} \\
 &= D \cdot I_{out}^2 \cdot R_{ds,on} \\
 &= 6.455^2 \cdot 0.01 \cdot 1.25 \\
 &= 0.5208\text{W}
 \end{aligned}$$

$$\begin{aligned}
 P_{loss,LS} &= I_{S2,rms}^2 \cdot R_{ds,on} \\
 &= D' \cdot I_{out}^2 \cdot R_{ds,on} \\
 &= 5.2705^2 \cdot 0.01 \cdot 1.25 \\
 &= 0.3472\text{W}
 \end{aligned}$$

$$\begin{aligned}
 P_{cond,loss} &= P_{loss,HS} + P_{loss,LS} \\
 &= 0.8680\text{W}
 \end{aligned}$$

### 2.1.2 Output Capacitance (Coss) Loss

When the switch node voltage transitions, the output capacitance  $C_{oss}$  of the MOSFET must be charged and discharged. This leads to switching loss given by:

$$P_{Coss} = \frac{1}{2} C_{oss} V_{ds}^2 \cdot f_s$$

Where:

- $C_{oss}$  is the output capacitance of the MOSFET,
- $V_{ds}$  is the drain-to-source voltage during switching (typically equal to input voltage),
- $f_s$  is the switching frequency.

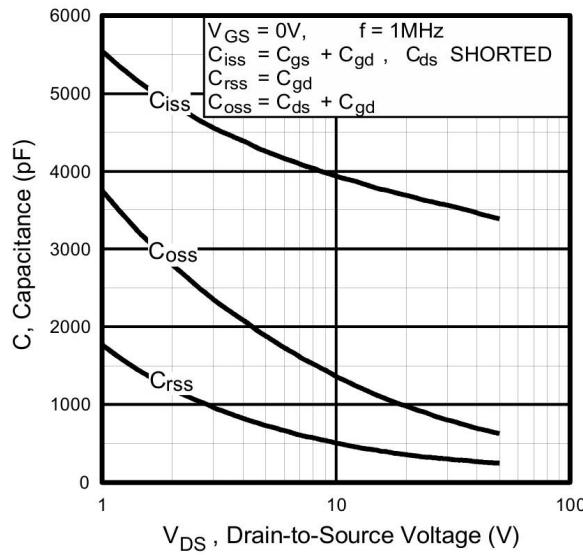


Figure 7: Coss of IRL3705NPBF

$$\begin{aligned}
E_{total} &= \int_0^{+\infty} V_R i_R dt + \int_0^{+\infty} (V_{in} - V_{S2}) i_R dt \\
&= \frac{1}{2} C_{eq,E} \cdot V_{in}^2 + C_{eq,Q} \cdot V_{in}^2 - \frac{1}{2} C_{eq,E} \cdot V_{in}^2 \\
&= C_{eq,Q} \cdot V_{in}^2 \\
&= C_{oss} \cdot V_{in}^2 \\
C_{eq,Q} &= \frac{1}{V_{dc}} \cdot \int_0^{V_{dc}} C(V_{dc}) dV_C \\
&= 2032.54 \text{ pF} \\
P_{Coss} &= 0.0813 \text{ W}
\end{aligned}$$

Coss loss is primarily significant in the high-side switch due to full voltage swings.

### 2.1.3 Overlap Loss (Hard-Switching Loss)

Overlap loss occurs during the MOSFET turn-on transition when both voltage and current are nonzero. It is calculated using:

$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns
$t_r$	Rise Time	—	140	—	
$t_{d(off)}$	Turn-Off Delay Time	—	37	—	
$t_f$	Fall Time	—	78	—	

Figure 8: tov of IRL3705NPBF

$$t_{ov} = t_r + t_f = 140 \text{ ns} + 78 \text{ ns} = 218 \text{ ns}$$

$$\begin{aligned}
P_{overlap} &= \frac{1}{2} \cdot V_{in} \cdot I_L \cdot t_{ov} \cdot f_s \\
&= \frac{1}{2} \cdot 20 \cdot \frac{25}{3} \cdot 218 \times 10^{-9} \cdot 10^5 \\
&\approx 1.82 \text{ W}
\end{aligned}$$

**But**, increasing the **deadtime** can effectively decrease the overlapping losses. So the overlapping losses really depend.

### 2.1.4 Reverse Recovery Loss

Reverse recovery loss occurs in the **low-side** MOSFET due to the body diode conduction during dead time. When the low-side MOSFET turns ON, the stored charge in the body diode must be removed, resulting in reverse recovery current and associated loss:

Where:

- $Q_{rr}$  is the reverse recovery charge,
- $V_{ds}$  is the voltage across the low-side switch at turn-on.

This loss can be minimized by reducing dead time or using a low  $Q_{rr}$  MOSFET or an external Schottky diode.

$t_{rr}$	Reverse Recovery Time	—	94	140	ns
$Q_{rr}$	Reverse Recovery Charge	—	290	440	nC

Figure 9: Qrr of IRL3705NPBF

$$\begin{aligned}
 P_{rr} &= \frac{1}{2} \cdot Q_{rr} \cdot V_{ds} \cdot f_s \\
 &= \frac{1}{2} \cdot 290 \times 10^{-9} \cdot 20 \cdot 10^5 \\
 &= 0.29 \text{ W}
 \end{aligned}$$

### 2.1.5 Gate Drive Loss (External Source, not counted)

Gate drive loss results from charging and discharging the gate capacitance of the MOSFET during each switching cycle. This energy is supplied by the gate driver circuitry and is independent of the current flowing through the power stage.

$Q_g$	Total Gate Charge	—	—	81	nC
$Q_{gs}$	Gate-to-Source Charge	—	—	19	
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	30	

Figure 10: Qgate of IRL3705NPBF

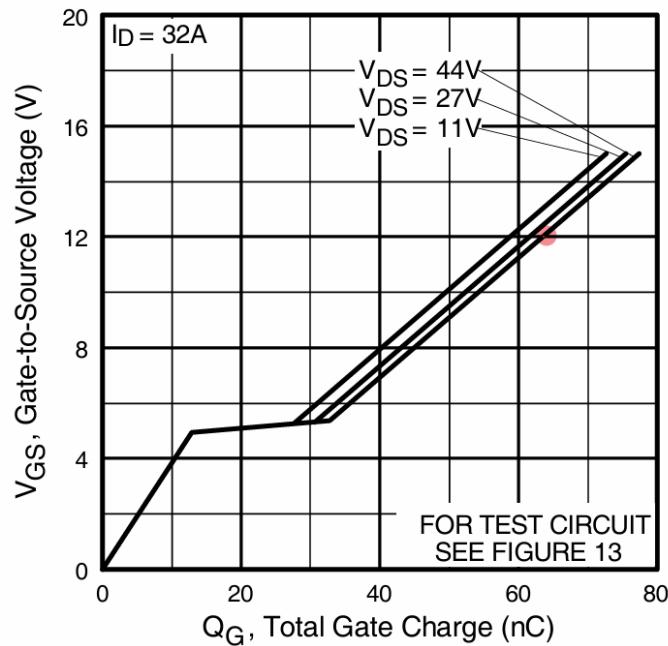


Figure 11: Qgate\_Curve of IRL3705NPBF

The gate drive loss for each MOSFET is estimated using  $V_{GS} = 12V$ ,  $V_{DS} = 11V$ :

$$\begin{aligned} P_{\text{gate}} &= Q_g \cdot V_g \cdot f_s \\ &= 63 \times 10^{-9} \cdot 12 \cdot 10^5 \\ &= 0.756 \text{ W per switch} \end{aligned}$$

Since the converter uses two synchronous MOSFETs (high-side and low-side), the total gate drive loss is:

$$P_{\text{gate, total}} = 2 \cdot 0.756 = 1.512 \text{ W}$$

### 2.1.6 Summary

Each loss mechanism was evaluated across the full operating range. At nominal conditions (100W output, 20V input, 100 kHz switching), approximate contributions are as follows:

- **High-side switch:**

- Conduction loss: Dominant
- Overlap loss: Dominant(if deadtime is small)
- Coss loss: Small

- **Low-side switch:**

- Conduction loss: Moderate
- Overlap loss: Large(if deadtime is small)
- Coss loss: Negligible
- Reverse recovery loss: Moderate

These calculations informed both switch selection and thermal design, ensuring reliable and efficient converter operation. **BUT regardless of AC LOSS...**

$$\begin{aligned} P_{\text{loss}} &= P_{\text{cond}} + P_{\text{Coss}} + P_{\text{ov}} + P_{\text{rr}} (+P_{\text{gate}}) \\ &= I_{\text{rms}}^2 R_{\text{ds(on)}} + C_{\text{oss}} V_{\text{ds}}^2 f_s + \frac{1}{2} V_{\text{in}} I_{\text{out}} t_{\text{ov}} f_s + \frac{1}{2} Q_{\text{rr}} V_{\text{ds}} f_s (+2Q_g V_g f_s) \\ &= 0.8680 + 0.0813 + 1.82 + 0.29 (+1.512) \\ &= 3.0563 \text{ W} \\ \eta &= \frac{P_{\text{in}} - P_{\text{loss}}}{P_{\text{in}}} \\ &= 96.9437\% \end{aligned}$$

This loss contributes to the overall power consumed by the control and drive circuitry, not the power dissipated across the MOSFETs themselves, but is still important in evaluating system efficiency and power budgeting.

## 2.2 Thermal Design and Junction Temperature Calculations

To evaluate the thermal performance of each switch, the junction temperature  $T_{\text{junction}}$  was calculated based on the total power dissipation and the thermal resistances in the heat path from the MOSFET junction to ambient air.

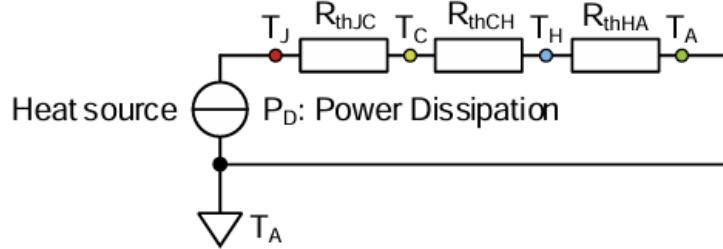


Figure 12: Thermal Model

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.
$R_{\theta\text{JC}}$	Junction-to-Case	—	0.90
$R_{\theta\text{CS}}$	Case-to-Sink, Flat, Greased Surface	0.50	—
$R_{\theta\text{JA}}$	Junction-to-Ambient	—	62

Figure 13: Thermal Resistance

### 2.2.1 Without Heatsink

When no heatsink is used, the thermal path consists of three components in series:

- $R_{\theta\text{JC}}$ : Junction-to-case thermal resistance
- $R_{\theta\text{CS}}$ : Case-to-sink thermal resistance (thermal pad or interface material)
- $R_{\theta\text{SA}}$ : Sink-to-ambient resistance (e.g., through PCB copper area)

The junction temperature is estimated using:

$$\begin{aligned}
 T_{\text{junction}} &= T_{\text{ambient}} + P_{\text{diss}} \cdot (R_{\theta\text{JC}} + R_{\theta\text{CS}} + R_{\theta\text{SA}}) \\
 &= T_{\text{ambient}} + P_{\text{diss}} \cdot R_{\theta\text{JA}} \\
 &= 25^{\circ}\text{C} + 3.0593 \cdot 62^{\circ}\text{C} \\
 &= 214.68^{\circ}\text{C}
 \end{aligned}$$

where:

- $T_{\text{ambient}}$  is assumed to be  $25^{\circ}\text{C}$ ,
- $P_{\text{diss}}$  is the total power loss in the switch (conduction + switching losses).

This equation provides a worst-case estimate for self-heating when the device is cooled only through the PCB without additional thermal management, which is pretty high and exceed the thermal ratings of IRL3705NPBF.

$T_J$	Operating Junction and Storage Temperature Range	-55 to +175	°C
$T_{STG}$	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1N·m)	

Figure 14: Thermal Ratings

## 2.2.2 With Heatsink

When a heatsink is attached, the thermal model simplifies by combining the case-to-ambient path into a single effective resistance,  $R_{\theta JA}$  (junction-to-ambient), as provided in the datasheet. **But with new  $R_{\theta SA}$  replaced by the heatsink.**

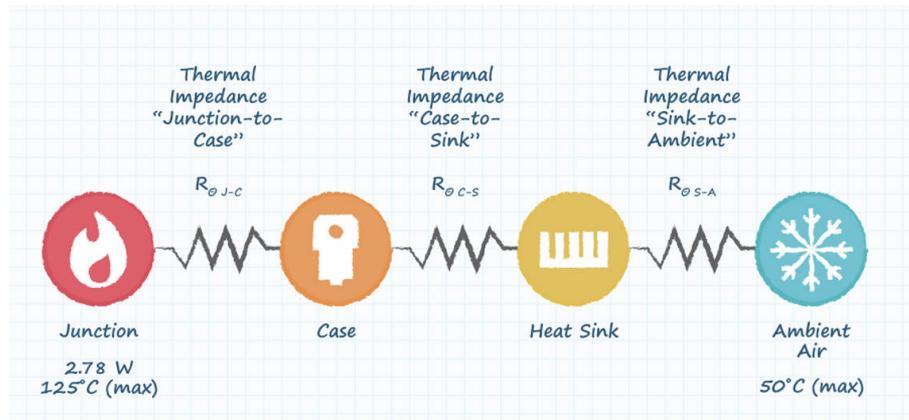


Figure 15: Thermal Model2

### Thermal Resistance

Symbol	Parameter	Typ.	Max.
$R_{\theta JC}$	Junction-to-Case	—	0.90
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—
$R_{\theta JA}$	Junction-to-Ambient	—	62

Figure 16: Thermal Resistance of IRFZ48NPbF

thermal resistance <sup>1</sup>				power dissipation <sup>1</sup>
@ 75°C ΔT, nat conv [°C/W]	@ 1 W, nat conv [°C/W]	@ 1 W, 200 LFM [°C/W]	@ 1 W, 400 LFM [°C/W]	@ 75°C ΔT, nat conv [W]
18.12	21.9	7.9	6.1	4.14

Figure 17: Thermal Resistance of Heatsink

$$\begin{aligned}
P_{diss} &= P_{cond} + P_{Coss} + P_{ov} + P_{rr} \\
&= 0.8680 + 0.0813 + 1.82 + 0.29 \\
&= 3.06W
\end{aligned}$$

$$\begin{aligned}
T_{junction} &= T_{ambient} + P_{diss} \cdot (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) || R_{\theta JA} \\
&= 25^{\circ}\text{C} + 3.06W \cdot (0.9 + 0.5 + 21.9) || 62W / ^{\circ}\text{C} \\
&= 25^{\circ}\text{C} + 3.06 \cdot 16.94^{\circ}\text{C} \\
&= 76.83^{\circ}\text{C}
\end{aligned}$$

If we set the deadtime longer to avoid a larger overlap loss:

$$\begin{aligned}
P_{diss} &= P_{cond} + P_{Coss} + P_{rr} \\
&= 0.8680 + 0.0813 + 0.29 \\
&= 1.24W
\end{aligned}$$

$$\begin{aligned}
T_{junction} &= T_{ambient} + P_{diss} \cdot (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) || R_{\theta JA} \\
&= 25^{\circ}\text{C} + 1.24W \cdot (0.9 + 0.5 + 21.9) || 62W / ^{\circ}\text{C} \\
&= 25^{\circ}\text{C} + 1.24 \cdot 16.94^{\circ}\text{C} \\
&= 46^{\circ}\text{C}
\end{aligned}$$

This simplified expression assumes proper thermal contact between the switch and the heatsink, and that the heatsink has sufficient airflow or conduction path to ambient.

#### Summary:

The total power dissipated in the MOSFETs ( $P_{diss}$ ) directly impacts the junction temperature.

- When **overlap loss is significant** (e.g., due to short dead time),  $P_{diss} = 3.06 \text{ W}$ , resulting in a junction temperature of approximately  $76.8^{\circ}\text{C}$ .
- By **increasing the dead time** to minimize overlap loss,  $P_{diss}$  decreases to  $1.24 \text{ W}$ , and the junction temperature drops to approximately  $46^{\circ}\text{C}$ .

This demonstrates the importance of **dead time optimization** not only for improving efficiency, but also for ensuring thermal safety and reliability of the power switches.

### 2.3 Final Switch Part Selection and Loss Summary

In selecting the final MOSFETs for the synchronous buck converter, several key criteria were evaluated to ensure efficient and reliable operation under a maximum load condition:

$$I_{\max} = \frac{P_{\text{out}}}{V_{\text{out}}} = \frac{100 \text{ W}}{12 \text{ V}} = 8.33 \text{ A}$$

#### Step 1: Current Rating Screening

MOSFETs with a maximum drain current lower than  $8.33 \text{ A}$  were excluded to ensure thermal reliability and safe continuous conduction under full load.

#### Step 2: Low $R_{ds(\text{on})}$ Selection

Among the eligible MOSFETs, the next priority was to minimize conduction loss. This was achieved by selecting devices with a low  $R_{ds(\text{on})}$ , as conduction loss scales with  $I^2$ :

$$P_{\text{cond}} = I_{\text{rms}}^2 \cdot R_{\text{ds(on)}}$$

A lower  $R_{\text{ds(on)}}$  directly reduces heat dissipation and improves overall converter efficiency, particularly during heavy load conditions.

### Step 3: Rise/Fall Time Consideration

To evaluate the switching performance and overlap loss, the turn-on rise time ( $t_{\text{rise}}$ ) and fall time ( $t_{\text{fall}}$ ) of each MOSFET were reviewed. Devices with fast switching transitions reduce overlap loss, which is calculated as:

$$P_{\text{ov}} = \frac{1}{2} V_{\text{in}} \cdot I_{\text{out}} \cdot (t_{\text{rise}} + t_{\text{fall}}) \cdot f_s$$

These parameters also help define a safe and efficient dead time window. Devices with slower transitions require longer dead time, which can reduce efficiency.

#### Neglected Parameters:

While switching losses also include  $C_{\text{oss}}$  (output capacitance) and  $Q_{\text{rr}}$  (reverse recovery charge), these were considered negligible in our case due to:

- Relatively small values of  $C_{\text{oss}}$  at operating voltage
- The low reverse recovery charge for most modern MOSFETs
- Minimal contribution to total loss compared to conduction and overlap losses

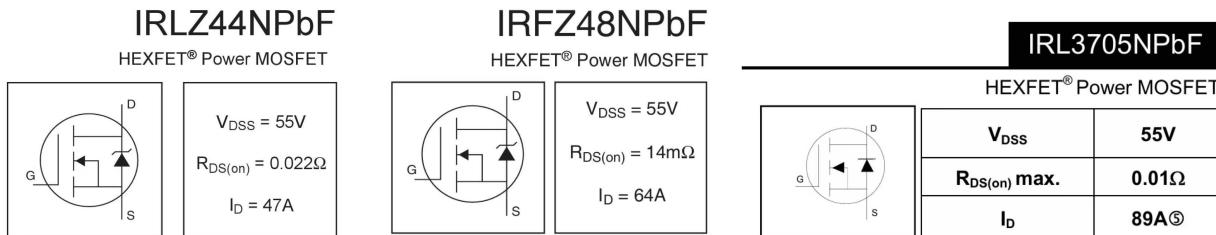


Figure 18: Different  $R_{\text{ds(on)}}$  of 3 MOSFETs

t <sub>d(on)</sub>	Turn-On Delay Time	---	11	---	ns
t <sub>r</sub>	Rise Time	---	84	---	
t <sub>d(off)</sub>	Turn-Off Delay Time	---	26	---	
t <sub>f</sub>	Fall Time		15		
t <sub>d(on)</sub>	Turn-On Delay Time	---	12	---	ns
t <sub>r</sub>	Rise Time	---	78	---	
t <sub>d(off)</sub>	Turn-Off Delay Time	---	34	---	
t <sub>f</sub>	Fall Time	---	50	---	
t <sub>d(on)</sub>	Turn-On Delay Time	---	12	---	ns
t <sub>r</sub>	Rise Time	---	140	---	
t <sub>d(off)</sub>	Turn-Off Delay Time	---	37	---	
t <sub>f</sub>	Fall Time	---	78	---	

Figure 19: Different ratings of 3 MOSFETs

For choosing the appropriate switches in Digikey, I have collected 15+ MOSFETs' parameters and use the script in Matlab to calculate the losses as below:

```

1 clear; clc;
2
3 V_in = 20;
4 I_out = 8.33;
5 f_sw = 100e3;
6 D = 12 / 20;
7
8 mosfets = struct( ...
9     'name', {'IRLZ44NPbF(47A)', 'IRFZ48NPbF(64A)', 'IRL3705NPbF(89A)
10      ', ...
11          'IRFI1310NPbF(24A)', 'IPAN60R125PFD7S(66A)', '
12              STB28N65M2(20A)', ...
13          'STB13N80K5(12A)', 'FQPF47P06(30A)', 'STF8NK100Z(6.5A)'
14      ', ...
15          'XP6NA2R4IT(93A)', 'MCPF90N12A(90A)', 'FDP4D5N10C(128A)
16      ', ...
17          'FDPF035N06B(88A)', 'MCPF80P06Y(80A)', 'IPA037N08N3G(75
18              A)'}, ...
19     'Rds_on', num2cell([0.022, 0.014, 0.01, ...
20         0.036, 0.125, 0.18, ...
21         0.45, 0.026, 1.65, ...
22         0.0024, 0.009, 0.004, ...
23         0.00291, 0.0068, 0.0037]), ...
24     't_rise', num2cell([84e-9, 78e-9, 140e-9, ...
25         56e-9, 13e-9, 10e-9, ...
26         16e-9, 450e-9, 19e-9, ...
27         91e-9, 8.7e-9, 49e-9, ...
28         33e-9, 26e-9, 49e-9]), ...
29     't_fall', num2cell([15e-9, 50e-9, 78e-9, ...
30         40e-9, 6e-9, 8.8e-9, ...
31         16e-9, 195e-9, 30e-9, ...
32         110e-9, 11e-9, 13e-9, ...
33         23e-9, 59e-9, 13e-9]), ...
34     'Coss', num2cell([400e-12, 470e-12, 870e-12, ...
35         450e-12, 28e-12, 60e-12, ...
36         50e-12, 1300e-12, 174e-12, ...
37         1160e-12, 430e-12, 2330e-12, ...
38         1685e-12, 936e-12, 1640e-12]), ...
39     'Qrr', num2cell([210e-9, 220e-9, 290e-9, ...
40         1.2e-6, 0.45e-6, 0.45e-6, ...
         5.7e-6, 0.55e-6, 5.3e-6, ...
         100e-9, 176e-9, 258e-9, ...
         78e-9, 85e-9, 130e-9]) ...
);

```

```

41 fprintf('MOSFET Loss Comparison\n');
42 fprintf('=====\\n');
43
44 for i = 1:length(mosfets)
45     Rds = mosfets(i).Rds_on;
46     t_r = mosfets(i).t_rise;
47     t_f = mosfets(i).t_fall;
48     Coss = mosfets(i).Coss;
49     Qrr = mosfets(i).Qrr;
50     name = mosfets(i).name;
51
52     I_HS = sqrt(D) * I_out;
53     I_LS = sqrt(1 - D) * I_out;
54
55     P_cond_HS = I_HS^2 * Rds;
56     P_cond_LS = I_LS^2 * Rds;
57     P_cond_total = P_cond_HS + P_cond_LS;
58
59     P_ov = 0.5 * V_in * I_out * (t_r + t_f) * f_sw;
60     P_coss = Coss * V_in^2 * f_sw;
61     P_rr = 0.5 * Qrr * V_in * f_sw;
62
63     P_total = P_cond_total + P_ov + P_coss + P_rr;
64
65     mosfets(i).Pcond = P_cond_total;
66     mosfets(i).Pov = P_ov;
67     mosfets(i).Pcoss = P_coss;
68     mosfets(i).Prr = P_rr;
69     mosfets(i).Ptotal = P_total;
70
71     fprintf('MOSFET: %s\\n', name);
72     fprintf(' P_conduction = %.4f W\\n', P_cond_total);
73     fprintf(' P_overlap      = %.4f W\\n', P_ov);
74     fprintf(' P_Coss          = %.4f W\\n', P_coss);
75     fprintf(' P_rr            = %.4f W\\n', P_rr);
76     fprintf(' P_total         = %.4f W\\n', P_total);
77     fprintf('-----\\n');
78 end

```

Fields	name	Rds_on	t_rise	t_fall	Coss	Qrr	Pcond	Pov	Pcoss	Prr	Ptotal
1	'IRLZ44NPbF(47A)'	0.0220	8.4000e-08	1.5000e-08	4.0000e-10	2.1000e-07	1.5266	0.8247	0.0160	0.2100	2.5772
2	'IRFZ48NPbF(64A)'	0.0140	7.8000e-08	5.0000e-08	4.7000e-10	2.2000e-07	0.9714	1.0662	0.0188	0.2200	2.2765
3	'IRL3705NPbF(89A)'	0.0100	1.4000e-07	7.8000e-08	8.7000e-10	2.9000e-07	0.6939	1.8159	0.0348	0.2900	2.8346
4	'IRFI1310NPbF(24A)'	0.0360	5.6000e-08	4.0000e-08	4.5000e-10	1.2000e-06	2.4980	0.7997	0.0180	1.2000	4.5157
5	'IPAN60R125PFD7S(66A)'	0.1250	1.3000e-08	6.0000e-09	2.8000e-11	4.5000e-07	8.6736	0.1583	0.0011	0.4500	9.2830
6	'STB28N65M2(20A)'	0.1800	1.0000e-08	8.8000e-09	6.0000e-11	4.5000e-07	12.4900	0.1566	0.0024	0.4500	13.0990
7	'STB13N80K5(12A)'	0.4500	1.6000e-08	1.6000e-08	5.0000e-11	5.7000e-06	31.2250	0.2666	0.0020	5.7000	37.1936
8	'FQPF47P06(30A)'	0.0260	4.5000e-07	1.9500e-07	1.3000e-09	5.5000e-07	1.8041	5.3728	0.0520	0.5500	7.7790
9	'STF8NK100Z(6.5A)'	1.6500	1.9000e-08	3.0000e-08	1.7400e-10	5.3000e-06	114.4917	0.4082	0.0070	5.3000	120.2068
10	'XP6NA2R4IT(93A)'	0.0024	9.1000e-08	1.1000e-07	1.1600e-09	1.0000e-07	0.1665	1.6743	0.0464	0.1000	1.9873
11	'MCPF90N12A(90A)'	0.0090	8.7000e-09	1.1000e-08	4.3000e-10	1.7600e-07	0.6245	0.1641	0.0172	0.1760	0.9818
12	'FDP4D5N10C(128A)'	0.0040	4.9000e-08	1.3000e-08	2.3300e-09	2.5800e-07	0.2776	0.5165	0.0932	0.2580	1.1452
13	'FDPF035N06B(88A)'	0.0029	3.3000e-08	2.3000e-08	1.6850e-09	7.8000e-08	0.2019	0.4665	0.0674	0.0780	0.8138
14	'MCPF80P06Y(80A)'	0.0068	2.6000e-08	5.9000e-08	9.3600e-10	8.5000e-08	0.4718	0.7081	0.0374	0.0850	1.3023
15	'IPA037N08N3G(75A)'	0.0037	4.9000e-08	1.3000e-08	1.6400e-09	1.3000e-07	0.2567	0.5165	0.0656	0.1300	0.9688

Figure 20: MOSFETs Selection

### Final Selection:

The **IRL3705NPbF (89A)** was selected as the final switch due to the following advantages:

- High current rating (up to 75A continuous at 25 °C)
- Low on-resistance  $R_{ds(on)}$  of approximately 10 mΩ, minimizing conduction losses
- Fast switching characteristics ( $t_{rise} \approx 140$  ns,  $t_{fall} \approx 78$  ns)
- Competitive cost and availability in a TO-220 package, which facilitates effective heatsinking

Based on detailed loss analysis, the IRL3705NPbF offers a favorable tradeoff between conduction and switching losses. Its thermal performance is well within safe limits when paired with a moderate heatsink.

While the **FDPF035N06B** achieves the best overall efficiency with a total switching loss of just 0.8138 W, it comes at a higher cost. In comparison, the IRL3705NPbF is significantly more economical and still maintains excellent electrical performance. Among the top three budget-friendly options: IRLZ44NPbF(47A), IRFZ48NPbF(64A), IRL3705NPbF(89A), it also boasts the lowest  $R_{ds(on)}$ , making it ideal for reducing conduction loss.

Furthermore, overlap loss—typically a concern for switching devices, which cannot be mitigated by adjusting the deadtime appropriately. As a result, the optimal choice in the calculation of loss at hand may be IRFZ48NPbF (64A), but to get maximum power point tracking, we need Vout to be large and have as small voltage drops as possible, so IRL3705NPbF(89A) with the a comparatively low  $R_{ds(on)}$  and high current ratings (not easy to break down) is finally chosen.

### 3 Magnetics

#### 3.1 All formulas applied in Magnetic Design Section:

**DC Inductor:** Use core factor method: (Kg method)

$$K_g = \frac{A_c^2 W_a}{\ell_t} \geq \frac{L^2 I_{\max}^2 \rho}{B_{\max}^2 R_w k_u}$$

$\rho$  : Wire resistivity

$\mu_0$  : Permeability of free space

$S$  : Power capability

$B$  : Flux density

$J$  : Current density

$k_u$  : Winding packing factor

**AC Inductor:** Use core area product:

$$A_c W_a \geq \frac{S}{\pi f B_{\max} J_{\max} k_u}$$

**Minimum Number of Turns:**  $N_{\min} = \frac{LI_{\max}}{B_{\max} A_c}$

**Gap Length:**  $g = \frac{\mu_0 A_c N^2}{L}$

**Inductor Value:**  $L \approx \frac{N^2 \mu_0 A_c}{g}$

**Maximum Wire Area:**  $A_w \leq \frac{k_u W_a}{N}$

**Skin Depth:**  $\theta = \sqrt{\frac{\rho_{\text{Cu}}}{\pi \mu_{\text{Cu}} f}}$

**For DC inductor  $B_{sat}$ :**  $B_{\max} = \frac{L \cdot I_{L,\max}}{N \cdot A_c}, B_{\max} \leq 75\% \cdot B_{sat}$

$B_{sat}$  normally can be read from datasheet

**Inductor winding resistance  $R_w$ :**  $R_w = \frac{\rho \cdot l}{A_w} = \frac{\rho_{Cu} \cdot l_t \cdot N}{\pi \cdot r^2}$

**Inductor Core Loss:**  $P_v = k \cdot f^\alpha \cdot B_{ac}^\beta \quad kW/m^3$

### 3.2 Comparision between Ferrous Alloys and Magnetic Ceramics(Ferrites)

Table 1: Core Materials and Recommended Frequency Ranges

Material Class	Type	Frequency Range	
Ferrous Alloys	Steel Laminations	60 Hz – 20 kHz	
Ferrous Alloys	Powdered Iron	Up to 100 kHz	
Magnetic Ceramics	MnZn Ferrite	Up to 1 MHz	
Magnetic Ceramics	NiZn Ferrite	Up to 10 MHz	

B	25 °C; 10 kHz; 1200 A/m 100 °C; 10 kHz; 1200 A/m	≈ 530 ≈ 410	mT	3C95
P <sub>V</sub>	25 °C; 100 kHz; 200 mT 100 °C; 100 kHz; 200 mT	≈ 350 ≈ 290	kW/m <sup>3</sup>	
B	25 °C; 10 kHz; 1200 A/m 100 °C; 10 kHz; 1200 A/m	≈ 410 ≈ 350	mT	3F4
P <sub>V</sub>	100 °C; 1 MHz; 30 mT 100 °C; 3 MHz; 10 mT	≈ 130 ≈ 220	kW/m <sup>3</sup>	
B	25 °C; 10 kHz; 3000 A/m 100 °C; 10 kHz; 3000 A/m	≈ 320 ≈ 260	mT	4F1
P <sub>V</sub>	100 °C; 3 MHz; 10 mT 100 °C; 10 MHz; 5 mT	≤ 200 ≤ 200	kW/m <sup>3</sup>	

Figure 21: B<sub>sat</sub> of Ferrous Alloys

For a DC inductor, the dominant constraint is the saturation flux density ( $B_{\text{sat}}$ ), which must satisfy the design requirement:

$$B_{\text{sat}} = \frac{\mu A_C I_{\text{sat}}}{g}$$

To ensure safe operation and avoid core saturation, the maximum operating flux density is typically limited to:

$$B_{\text{max}} \leq 0.75 \cdot B_{\text{sat}}$$

At the reference temperature of 25 °C, the saturation flux densities for selected core materials are:

- **3F4:**  $B_{\text{sat}} = 410 \text{ mT}$

- **4F1:**  $B_{\text{sat}} = 320 \text{ mT}$
- **3C95:**  $B_{\text{sat}} = 530 \text{ mT}$

For an AC inductor operating at 3 MHz, where core loss ( $P_{\text{loss}}$ ) is the primary constraint, material selection is critical. Among the options: **3C95** offers a high saturation flux density ( $B_{\text{sat}}$ ), but exhibits significant loss at high frequencies; **4F1** provides the lowest  $P_{\text{loss}}$  at high frequency, though it has the lowest  $B_{\text{sat}}$ ; and **3F4** serves as a balanced, mid-range material in terms of both saturation and loss characteristics.

### 3.3 Design of Magnetic Components: Type, Core, Winding, Gap...

In this buck converter design, the key magnetic component is the output inductor. Its role is to regulate current flow to the load by storing and releasing energy between switching cycles, thereby reducing ripple and maintaining continuous conduction mode (CCM).

The output inductor also plays a crucial role in defining the current ripple, which affects both efficiency and output voltage ripple. A well-designed inductor must balance size, core losses, and copper losses, while avoiding core saturation under peak load conditions.

Ferrite-based cores are typically chosen for high-frequency applications due to their low core loss characteristics. For this project, a toroidal ferrite core was optimal due to its compact form, low EMI, and closed magnetic path.

To size the magnetic core for the output filter inductor, we use the  $K_g$  method, which provides a practical estimate of core size based on energy storage requirements and thermal constraints. The core area product must satisfy:

$$K_g \geq \frac{L^2 I_{\max}^2 \rho}{B_{\max}^2 R_w k_u}$$

Where:

- $L$  is the inductance
- $I_{\max}$  is the peak current
- $\rho = 2.09 \times 10^{-8} \Omega \cdot \text{m}$  is the resistivity of copper
- $B_{\max}$  is the maximum allowable flux density
- $R_w$  is the winding resistance
- $k_u = 0.4$  is the winding package factor

Given:

- Copper resistivity:  $\rho = 2.09 \times 10^{-8} \Omega \cdot \text{m}$
- Wire diameter 9Gauge 16):  $d = 1.291 \text{ mm} = 1.291 \times 10^{-3} \text{ m}$
- Wire length:  $\ell = 100 \text{ cm} = 1.00 \text{ m}$

#### Step 1: Compute cross-sectional area of the wire

$$S = \pi \cdot \left( \frac{d}{2} \right)^2 = \pi \cdot \left( \frac{1.291 \times 10^{-3}}{2} \right)^2 = \pi \cdot (6.455 \times 10^{-4})^2 \approx 1.31 \times 10^{-6} \text{ m}^2$$

## Step 2: Compute winding resistance

$$R_w = \frac{\rho \cdot \ell}{S} = \frac{2.09 \times 10^{-8} \cdot 1.00}{1.31 \times 10^{-6}} \approx 0.0159 \Omega$$

**Result:**

$$R_w \approx 0.0159 \Omega$$

The core area product is calculated using the  $K_g$  method:

$$K_g \geq \frac{L^2 I_{\max}^2 \rho}{B_{\max}^2 R_w k_u}$$

Given:

- Inductance:  $L = 36 \mu\text{H} = 36 \times 10^{-6} \text{ H}$
- Peak current:  $I_{\max} = 8.33 \cdot (1 + 20\%) = 9.167 \text{ A}$
- Copper resistivity:  $\rho = 2.09 \times 10^{-8} \Omega \cdot \text{m}$
- Winding resistance:  $R_w = 0.0159 \Omega$
- Maximum flux density:  $B_{\max} = 0.3975 \text{ T}$
- Winding fill factor:  $k_u = 0.4$

Substituting the values:

$$K_g \geq \frac{(36 \times 10^{-6})^2 \cdot (9.167)^2 \cdot (2.09 \times 10^{-8})}{(0.3975)^2 \cdot 0.0159 \cdot 0.4}$$

**Result:**

$$K_g \geq 2.265 \times 10^{-12} \text{ m}^5 = 2.265 \times 10^3 \text{ mm}^5$$

	RM4	RM5	RM6	RM8	RM10	RM12	RM14
Effective magnetic path length $\ell_c$ (mm)	22.7	22.4	28.6	38.0	44.0	56.9	70.0
Effective core area $A_{c,e}$ ( $\text{mm}^2$ )	14.0	23.7	36.6	64.0	98.0	140	178
Minimum core area $A_{c,\min}$ ( $\text{mm}^2$ )	10.7	17.3	30.2	53.5	86.6	121	165
Core window area $W_{A,c}$ ( $\text{mm}^2$ )	15.6	18.2	26.0	48.9	69.5	110	155
Bobbin window area $W_{A,b}$ ( $\text{mm}^2$ )	7.7	9.5	15	30.0	41.5	73.0	107
Bobbin mean turn length $\ell_t$ (mm)	20	25	30	42	52	61	71.5
Effective core volume $V_{c,e}$ ( $\text{mm}^3$ )	318	530	1050	2430	4310	7970	12500
Core set weight (g)	1.7	3.0	5.5	13	23	42	74
Effective surface area $A_{s,e}$ ( $\text{mm}^2$ )	586	787	1130	2020	2960	4460	6820
Thermal resistance $R_{th}$ ( $^{\circ}\text{C}/\text{W}$ )	86	69	60	38	30	23	19
Core area product $A_{c,e} W_{A,b}$ ( $\text{mm}^4$ )	$1.1 \times 10^2$	$2.3 \times 10^2$	$5.5 \times 10^2$	$1.92 \times 10^3$	$4.07 \times 10^3$	$1.02 \times 10^4$	$1.90 \times 10^4$
Core factor $K_g$	$4.4 \times 10^1$	$1.1 \times 10^2$	$4.6 \times 10^2$	$2.0 \times 10^3$	$6.0 \times 10^3$	$1.8 \times 10^4$	$4.07 \times 10^4$
$A_{c,\min}^2 W_{A,b} / \ell_t$ ( $\text{mm}^5$ )							

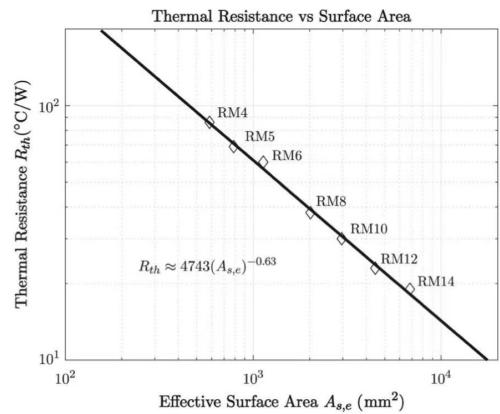


Figure 22: RM-X Parameters

This is the minimum core area product required to maintain safe flux and thermal limits for a  $36\ \mu\text{H}$  inductor carrying  $8.33\ \text{A}$  at  $B_{\max} = 0.3975\ \text{T}$ . The minimum size for the core is RM10,  $K_g = 6 \times 10^5 (\text{mm}^5)$ .

**Given:**

$$L = 3.6 \times 10^{-5}\ \text{H}$$

$$N = 13$$

$$\mu_0 = 4\pi \times 10^{-7}\ \text{H/m}$$

$$A_c = 86.6\ \text{mm}^2 = 86.6 \times 10^{-6}\ \text{m}^2$$

$$\rho_{\text{Cu}} = 2.09 \times 10^{-8}\ \Omega \cdot \text{m}$$

$$f = 100\ \text{kHz} = 1 \times 10^5\ \text{Hz}$$

### 1. Air Gap Calculation:

$$g = \frac{\mu_0 A_c N^2}{L} = \frac{4\pi \times 10^{-7} \cdot 86.6 \times 10^{-6} \cdot 13^2}{3.6 \times 10^{-5}}$$

$$\Rightarrow g \approx 0.511\ \text{mm}$$

### 2. Skin Depth Calculation:

$$\theta = \sqrt{\frac{\rho_{\text{Cu}}}{\pi \mu_0 f}} = \sqrt{\frac{2.09 \times 10^{-8}}{\pi \cdot 4\pi \times 10^{-7} \cdot 10^5}}$$

$$\approx 0.232\ \text{mm}$$

### 3. Minimum Wire Radius Constraint:

$$NA_w \leq k_u W_a, \quad \text{where } A_w = \pi r^2$$

$$r \leq \sqrt{\frac{k_u \cdot W_a}{N \cdot \pi}}$$

$$= \sqrt{\frac{0.4 \cdot 41.55 \times 10^{-6}}{13 \cdot \pi}}$$

$$\approx 0.637\ \text{mm}$$

Wire Gauge Conversion Chart					
AWG	Diameter		Area		
	in.	mm	CMA	mm <sup>2</sup>	
4/0 (0000)	0.46	11.68	212000	107	
3/0 (000)	0.41	10.41	168000	85	
2/0 (00)	0.365	9.27	133000	67.4	
1/0 (0)	0.325	8.26	106000	53.5	
1	0.289	7.34	83700	42.4	
2	0.258	6.55	66400	33.6	
3	0.229	5.82	52600	26.7	
4	0.204	5.18	41700	21.2	
5	0.182	4.62	33100	16.8	
6	0.162	4.11	26300	13.3	
7	0.144	3.66	20800	10.5	
8	0.128	3.25	16500	8.37	
9	0.114	2.90	13100	6.63	
10	0.102	2.59	10400	5.26	
11	0.091	2.31	8230	4.17	
12	0.081	2.06	6530	3.31	
13	0.072	1.83	5180	2.62	
14	0.062	1.57	4110	2.08	
15	0.057	1.45	3260	1.65	
16	0.051	1.30	2580	1.31	
17	0.045	1.14	2050	1.04	
18	0.040	1.02	1620	0.823	
19	0.036	0.91	1290	0.653	
20	0.032	0.81	1020	0.518	
21	0.0285	0.72	810	0.41	
22	0.0253	0.643	642	0.326	
23	0.0226	0.574	509	0.258	
24	0.0201	0.511	404	0.205	
25	0.0179	0.45	320	0.162	
26	0.0159	0.404	254	0.129	
27	0.0142	0.361	202	0.102	
28	0.0126	0.320	160	0.081	
29	0.0113	0.29	127	0.0642	
30	0.01	0.254	101	0.0509	

AWG: American wire gauge  
CMA: Circular Mils Area

Figure 23: AWG Standard

**Conclusion:** The wire radius must be less than or equal to 0.637 mm (diameter  $\leq 1.274$  mm) to accommodate 13 turns within the winding area. According to AWG, we can choose  $D \leq 1.274\text{mm}$ , which is  $AWG \geq 16$  for inductor wire configuration.

### 3.4 Copper Loss and Core Loss Calculation

Copper loss in the inductor winding is computed using:

$$P_{\text{cu}} = I_{L,\text{rms}}^2 \cdot R_{\text{dc}}$$

With the following parameters:

- Number of turns:  $N = 13$
- Average turn length(RM10):  $\ell_t = 52 \text{ mm} = 0.052 \text{ m}$
- Copper resistivity:  $\rho_{\text{Cu}} = 2.09 \times 10^{-8} \Omega \cdot \text{m}$
- Wire radius (AWG 16):  $r = \frac{1.291}{2} = 0.6455 \text{ mm}$
- RMS inductor current:  $I_{L,\text{rms}} = 8.33 \text{ A}$

DC resistance of the winding:

$$R_{\text{dc}} = \frac{\rho_{\text{Cu}} \cdot \ell_t \cdot N}{\pi r^2} = \frac{2.09 \times 10^{-8} \cdot 0.052 \cdot 13}{\pi \cdot (0.0006455)^2} \approx 0.01078 \Omega$$

Copper loss:

$$\begin{aligned} P_{Cu} &= I_{Lrms}^2 \cdot R_{dc} \\ &= 8.33^2 \cdot 0.01078 \\ &= 0.748W \end{aligned}$$

AC core losses are computed using the empirical Steinmetz equation:

$$P_{core} = k \cdot f^\alpha \cdot B_{ac}^\beta \cdot V_{core}$$

The peak-to-peak inductor ripple is given by:

$$\Delta i_{L,pp} = \frac{V_{in} - V_{out}}{L} \cdot D \cdot T_s$$

With:

- Input voltage:  $V_{in} = 20 \text{ V}$
- Output voltage:  $V_{out} = 12 \text{ V}$
- Inductance:  $L = 3.6 \mu\text{H} = 3.6 \times 10^{-6} \text{ H}$
- Duty cycle:  $D = \frac{12}{20} = 0.6$
- Switching period:  $T_s = \frac{1}{f_{sw}} = \frac{1}{100000} = 1 \times 10^{-5} \text{ s}$

$$\Delta i_{L,pp} \approx 1.33 \text{ A}$$

With the following parameters:

- Frequency:  $f = 100 \text{ kHz}$
- Peak flux density:  $B_{ac} = \frac{L \cdot \frac{i_{Lpp}}{2}}{N \cdot A_c} = \frac{3.6\mu\text{H} \cdot 0.665A}{10.98mm^2} = 18.8\text{mT}$
- Core volume:  $V_{core} = 1.61 \text{ cm}^3 = 1.61 \times 10^{-6} \text{ m}^3$
- Steinmetz constants for 3C95 ferrite: (NOT PROVIDED ON DATASHEET)

So we can look up at  $Pv - Bac$  plot at  $100\text{kHz}$  on the datasheet, which also provides an extra way for estimating  $P_{core}$ .

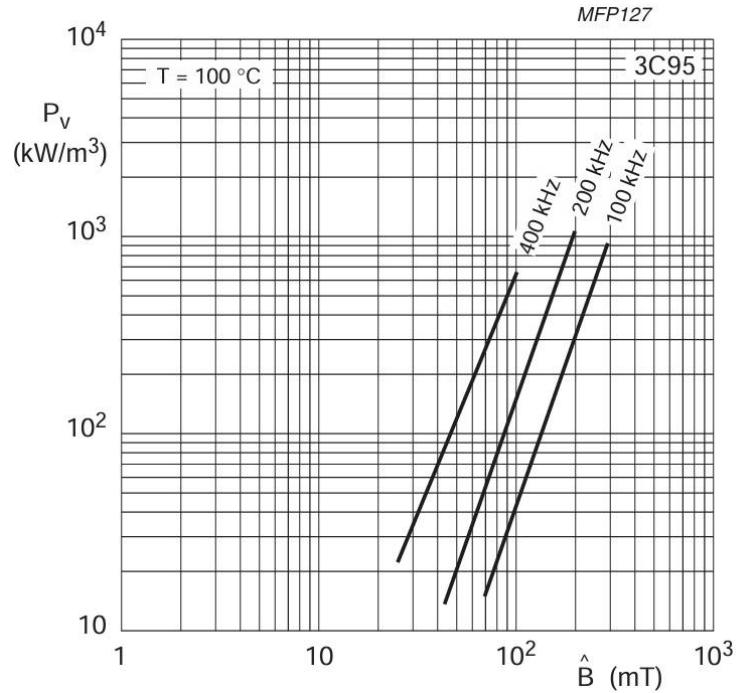


Figure 24: 3C95 Core Loss

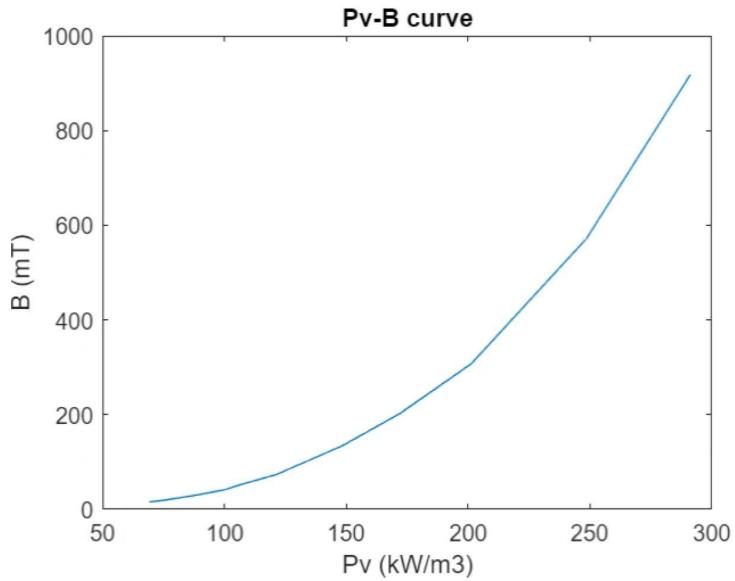


Figure 25: 3C95 Core Loss - Matlab Fit

When we use Matlab to fit into an approximate log-scale curve, we can find that when approaching  $18.8\text{mT}$ ,  $P_v \approx 2.5\text{kW/m}^3$ . Core loss are correlated to effective core column  $V_{c,e}$ .

$$\begin{aligned}
 P_{core} &= P_v \cdot V_{c,e} \\
 &= 2.5\text{kW/m}^3 \cdot 4310\text{mm}^3 \\
 &= 0.0108\text{W}
 \end{aligned}$$

**Conclusion:** Core losses contribute an additional 0.0108 W to the inductor's total power dissipation, which is comparatively small.

Now we can calculate total inductance loss:

$$\begin{aligned} P_{inductor} &= P_{Cu} + P_{core} \\ &= 0.748 + 0.0108W \\ &= 0.7588W \end{aligned}$$

Adding the switching loss, the total loss now becomes:

$$\begin{aligned} P_{loss} &= P_{switch} + P_{inductor} \\ &= 3.0563 + 0.7588W \\ &= 3.8151W \end{aligned}$$

### 3.5 Magnetic Design Parameters and Material Selection

The inductor was designed to meet a target ripple current of 20% of the output current at worst-case conditions. The inductor value  $L$  is calculated as:

$$L = \frac{(V_{in} - V_{out}) \cdot D}{f_s \cdot \frac{1}{2} \Delta I_{Lpp}}$$

Key parameters:

- Input voltage  $V_{in} = 20$  V
- Output voltage  $V_{out} = 12$  V
- Switching frequency  $f_s = 100$  kHz
- Output current  $I_{out} = 8.33$  A
- Ripple current  $\Delta I_{Lpp} = 0.2 \cdot I_{out}$

Using these values, the calculated inductance is:

$$L \approx \frac{(20 - 12) \cdot 0.6}{100 \times 10^3 \cdot \frac{1}{2}(0.2 \cdot 8.33)} \approx 36 \mu\text{H}$$

A toroidal ferrous alloy (e.g., 3C95) was selected based on required energy storage and low EMI characteristics.

$$g = \frac{N^2 \mu_0 A_c}{L}$$

where:

$$\begin{aligned} N &= 13 \quad (\text{number of turns}) \\ \mu_0 &= 4\pi \times 10^{-7} \text{ H/m} \quad (\text{permeability of free space}) \\ A_{c,min} &= 86.6 \text{ mm}^2 \quad (\text{core area}) \\ L &= 36 \mu\text{H} \quad (\text{inductance}) \end{aligned}$$

Substituting values:

$$g = \frac{13^2 \times (4\pi \times 10^{-7}) \times (86.6 \times 10^{-6})}{36 \times 10^{-6}}$$

$$g = 0.511 \text{ mm}$$

Such that  $g \leq 0.511 \text{ mm}$  to meet the requirement of minimum inductance of  $36 \mu\text{H}$ .

### 3.6 Final Magnetic Design and Loss Summary

The final design uses an  $36 \mu\text{H}$  inductor wound with 16 AWG copper wire, consisting of 13 turns on a 3C95 toroidal core.

#### Summary of Magnetic Losses:

- Copper loss:  $P_{\text{cu}} \approx 0.748 \text{ W}$  (based on measured  $R_{\text{dc}}$  and RMS current)
- Core loss:  $P_{\text{core}} \approx 0.0108 \text{ W}$  (using manufacturer's core loss curves at 100 kHz,  $B_{\text{max}} \approx 18.8 \text{ mT}$ )
- Total inductor loss:  $P_{\text{mag}} \approx 0.7588 \text{ W}$

The inductor operates well within thermal and saturation limits under full load. The selected magnetic design provides a balance between efficiency, size, and thermal reliability.

#### Thermal Model of Inductor:

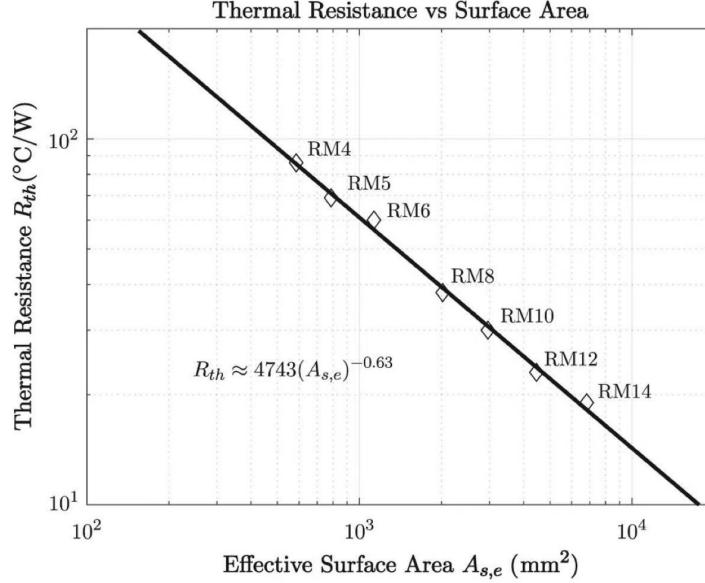


Figure 26: Thermal Resistance of RM-X

$$\begin{aligned} T_{\text{hotsoft}} &= T_{\text{amb}} + R_{\text{th}} \cdot P_{\text{inductor}} \\ &= 25^{\circ}\text{C} + 0.7588 \text{ W} \cdot 30^{\circ}\text{C}/\text{W} \\ &= 47.764^{\circ}\text{C} \end{aligned}$$

With the inductor size being really large, the heat dissipation could be better, so that within  $48^{\circ}\text{C}$  is acceptable.

## 4 Capacitors

### 4.1 Capacitor Type Selection

In this synchronous buck converter design, both the input and output capacitors are critical for maintaining voltage stability, minimizing ripple, and ensuring dynamic response.

#### Selected Capacitor Types:

- **Multi-Layer Ceramic Capacitors (MLCC):**

- Low ESR, high-frequency performance,
- Good stability over temperature and voltage,
- Ideal for reducing high-frequency ripple and noise.

- **Electrolytic Capacitors:**

- High capacitance-to-volume ratio,
- Economical for bulk energy storage,
- Comparatively large current and voltage ratings.
- Ideal for reducing low-frequency ripple and noise.

#### Summary:

- **Input side:** Parallel combination of ceramic and electrolytic capacitors.
- **Output side:** Pure ceramic capacitors in parallel.

### Why Input Side Uses Ceramic and Electrolytic Capacitors

The input side of the converter needs to handle two different types of demands:

- Very fast, high-frequency switching noise caused by the MOSFETs switching,
- Larger, slower changes in the current demand from the load.
- We want it to have a slow response to unstable  $V_{in}$ .

Ceramic capacitors are excellent at dealing with high-frequency noise because they have very low equivalent series resistance (ESR) and very low equivalent series inductance (ESL), allowing them to filter out fast voltage spikes effectively.

However, ceramics have two limitations:

- Their capacitance is relatively small,
- Their capacitance decreases significantly under DC bias.

Electrolytic capacitors, by contrast, provide large capacitance values at low cost, making them ideal for supplying bulk energy during slower load transients. However, they have higher ESR and are less effective at filtering high-frequency noise.

**Therefore, combining ceramic and electrolytic capacitors in parallel at the input** provides the benefits of both:

- Ceramic capacitors suppress high-frequency switching noise,
- Electrolytic capacitors handle large, low-frequency energy fluctuations.

This arrangement stabilizes the input voltage across a wide range of frequencies, ensuring both low ripple and robust dynamic response.

### Why Output Side Uses Only Ceramic Capacitors

At the output of the converter, the primary goal is to maintain a very clean, stable DC voltage with minimal ripple and excellent dynamic response to sudden load changes.

Ceramic capacitors are ideal for this purpose because:

- We want the system to have fast V<sub>out</sub> response.
- They offer extremely low ESR, minimizing output voltage ripple,
- They react very quickly to fast load transients,
- They are compact, highly reliable, and can easily be paralleled to achieve the required capacitance.

Electrolytic capacitors are not preferred at the output because:

- Their higher ESR would increase output ripple voltage,
- Their slower dynamic response would worsen transient performance,
- They have a shorter lifespan under high ripple currents at elevated frequencies like 100 kHz.

**Thus, using only ceramics at the output** guarantees:

- Minimal output ripple,
- Excellent fast transient response,
- Higher overall efficiency and reliability of the converter.

## 4.2 Design Justification and Parallel Configuration

### Input Capacitor Sizing

The input capacitor must handle the ripple current drawn by the high-side MOSFET and maintain the PV voltage stability.

The minimum required capacitance is:

$$C_{\text{in}} \geq \frac{I_{\text{out}} \cdot D}{\Delta V_{\text{in}} \cdot f_{\text{sw}}}$$

Where:

- $I_{\text{out}} = 8.33 \text{ A}$ ,
- $D = 0.75$ , at worst case
- $\Delta V_{\text{in,pp}} = 5\% \times 20 \text{ V} = 1 \text{ V}$ ,

- $f_{sw} = 100 \text{ kHz}$ .

Substituting:

$$C_{in} \geq 41.7 \mu\text{F}$$

### Chosen Configuration:

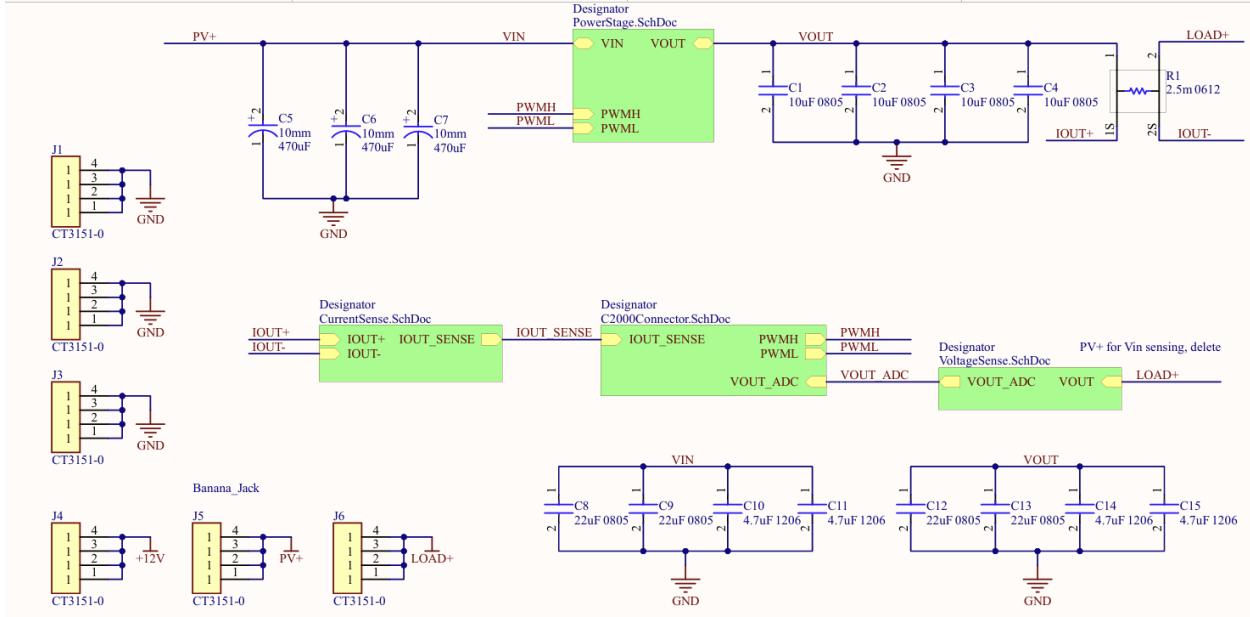


Figure 27: Top Level of PV Buck Schematic

- 2x 22  $\mu\text{F}$  0805 35 V ceramic capacitors,
- 2x 4.7  $\mu\text{F}$  1206 35 V ceramic capacitors,
- 3x 470  $\mu\text{F}$  120 V aluminum electrolytic capacitor.

Since capacitance drops down hugely in 100kHz because of RCL resonance inside capacitor. This design adds up an input bus including electrolytic capacitors and MLCCs to ensure low ESR at high frequencies and sufficient capacitance for load transients.

### Output Capacitor Sizing

The output capacitor controls output voltage ripple:

$$C_{out} \geq \frac{\Delta I_{L,pp}}{8 \times f_{sw} \times \Delta V_{out}}$$

Where:

- $\Delta I_{L,pp} = 8.33 \cdot 20\% = 1.33 \text{ A}$ ,
- $\Delta V_{out,pp} = 12 \cdot 5\% = 0.6 \text{ V}$ .

Substituting:

$$C_{\text{out}} \geq 2.77 \mu\text{F}$$

#### **Chosen Configuration:**

- 5x  $10 \mu\text{F}$  0805 35 V ceramic capacitors,
- 2x  $22 \mu\text{F}$  0805 35 V ceramic capacitors,
- 2x  $4.7 \mu\text{F}$  1206 35 V ceramic capacitors,

This configuration reduces ESR, provides sufficient capacitance even after DC bias derating, and easily meets the ripple requirements.

#### **Advantages of Parallel Capacitors:**

- Increases effective capacitance,
- Decreases effective ESR and ESL,
- Shares ripple current, improving thermal performance.

### **4.3 Frequency Response of Capacitors**

#### **Parasitic Components in Real Capacitors**

Real-world capacitors are not ideal and have internal parasitic elements:

- **ESR** (Equivalent Series Resistance),
- **ESL** (Equivalent Series Inductance),
- **C** (Nominal Capacitance).

The resulting model is an RLC network, which strongly affects behavior at high frequencies.

#### **Impedance vs Frequency Behavior**

The impedance of a capacitor changes with frequency:

- At **low frequencies**, the capacitor behaves ideally: impedance  $Z \approx \frac{1}{j\omega C}$  (capacitive).
- At **self-resonant frequency (SRF)**, the capacitive reactance cancels the inductive reactance: impedance reaches a minimum.
- Above SRF, the capacitor behaves as an **inductor**: impedance rises with frequency.

## Self-Resonant Frequency (SRF)

Self-Resonant Frequency is the point where:

$$\omega_{\text{SRF}} = \frac{1}{\sqrt{LC}}$$

Where:

- $L$  = parasitic inductance (ESL),
- $C$  = nominal capacitance.

At frequencies higher than SRF, the capacitor stops acting like a capacitor and acts inductive. The following capacitors were selected based on voltage rating, ESR, ripple capability, and stability under DC bias.

Rated Ripple Current (mA r.m.s./105°C, 100kHz)					
定格電圧 Rated Voltage (Vdc)	静電容量 Capacitance ( $\mu$ F)	外形寸法 Size $\phi D \times L$ (mm)	定格リップル 電流 Rated Ripple Current	インピーダンス ( $\Omega$ MAX) Impedance	
				20°C, 100kHz	-10°C, 100kHz
25	68	5×11	450	0.40	1.2
	150	6.3×11	700	0.17	0.51
	330	8×11.5	1200	0.075	0.23
	390	8×16	1600	0.059	0.18
	470	10×12.5	1700	0.053	0.16
	560	8×20	1960	0.041	0.13
	680	10×16	2000	0.038	0.12
	1000	10×20	2500	0.028	0.084
	1200	10×25	2900	0.024	0.072
	1500	12.5×20	2600	0.025	0.075
	1800	12.5×25	3200	0.019	0.057
	2200	12.5×30	3660	0.018	0.054
	2200	16×20	3330	0.021	0.063
	2700	12.5×35	4120	0.016	0.048
	3300	16×25	3810	0.017	0.051

Figure 28: ESR and current ratings of 470 $\mu$ F at different frequencies



Figure 29: Capacitance of 470 $\mu$ F at 100kHz

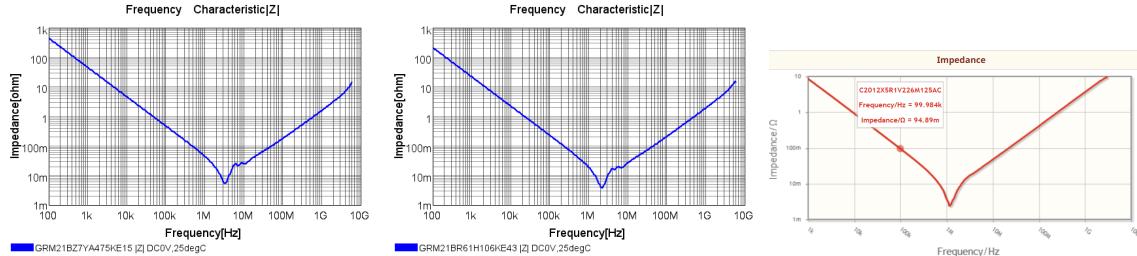


Figure 30: Impedance of  $4.7\mu\text{F}$ ,  $10\mu\text{F}$ , and  $22\mu\text{F}$  capacitors at different frequencies

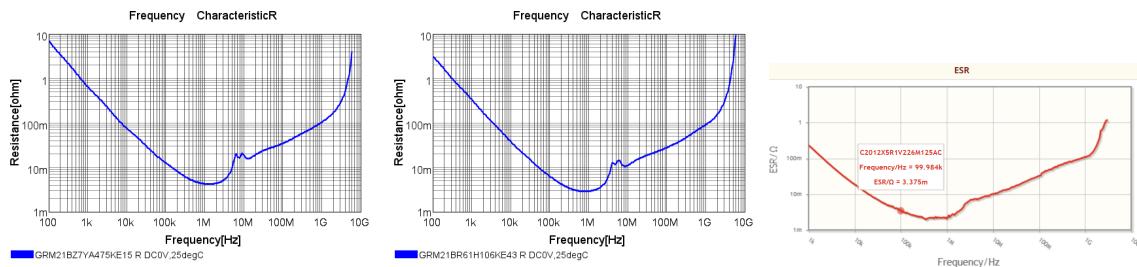


Figure 31: ESR of  $4.7\mu\text{F}$ ,  $10\mu\text{F}$ , and  $22\mu\text{F}$  capacitors at different frequencies

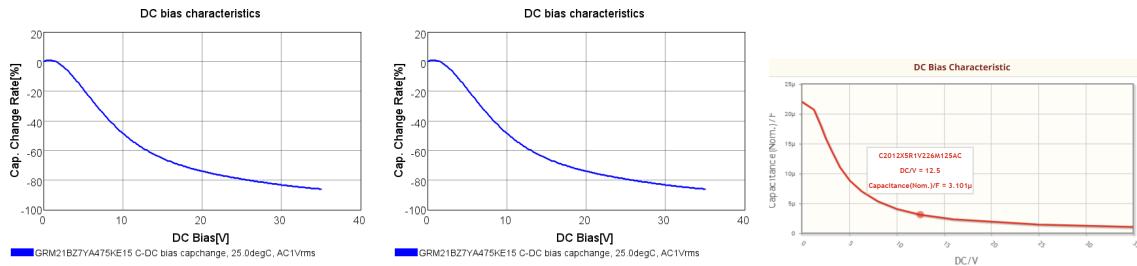


Figure 32: Capacitance change of  $4.7\mu\text{F}$ ,  $10\mu\text{F}$ , and  $22\mu\text{F}$  capacitors across frequency

Capacitance + Package	Voltage	ESR	Impedance 100 kHz	Capacitance 100 kHz
$470\mu\text{F}$ , Electrolytic	120 V	$0.053\Omega$	$\text{xxx}\Omega$	$8.18\mu\text{F}$
$22\mu\text{F}$ , 0805 MLCC	35 V	$3.375\text{ m}\Omega$	$94.89\text{ m}\Omega$	$3.101\mu\text{F}$
$10\mu\text{F}$ , 0805 MLCC	35 V	$6\text{ m}\Omega$	$230\text{ m}\Omega$	$2.620\mu\text{F}$
$4.7\mu\text{F}$ , 1206 MLCC	35 V	$15\text{ m}\Omega$	$400\text{ m}\Omega$	$2.030\mu\text{F}$

Table 2: Summary of Capacitors Used and Effective Capacitance/Impedance at 100 kHz

### Notes:

- Electrolytic capacitors are used for low-frequency energy buffering.
- MLCC capacitors are used to suppress high-frequency switching noise.
- DC bias effects were considered for MLCCs at operational voltages.

## 4.4 Capacitor ESR Loss Calculation

The power loss in the input and output capacitors due to ripple current flowing through their equivalent series resistance (ESR) must be calculated to estimate thermal and efficiency performance.

### Inductor Ripple Current Estimation

The output current RMS value is:

$$I_{\text{out,rms}} = 8.33 \text{ A}$$

The inductor current ripple is designed to be 20% of the output current, leading to a peak-to-peak ripple current:

$$\Delta I_{L,pp} = 0.2 \times 8.33 = 1.666 \text{ A}$$

Since the ripple current forms a triangular waveform, its RMS value can be derived as follows:

### Calculation for Triangular Waveform Ripple RMS Current

The RMS value of a general periodic signal  $i(t)$  over one period  $T$  is:

$$I_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T [i(t)]^2 dt}$$

For a triangular waveform that oscillates between  $-A$  and  $+A$  (peak-to-peak value  $\Delta I_{pp} = 2A$ ), integration gives:

$$I_{\text{rms}} = \frac{A}{\sqrt{3}} = \frac{\Delta I_{pp}}{2\sqrt{3}} = \frac{\Delta I_{pp}}{\sqrt{12}}$$

Thus, the ripple RMS current is:

$$I_{\text{ripple,rms}} = \frac{1.666}{\sqrt{12}} \approx 0.481 \text{ A}$$

This ripple current will cause ESR losses in both input and output capacitors.

### Input Capacitor ESR Loss

The total ESR of the input capacitor bank (parallel combination) is:

$$\begin{aligned} \frac{1}{R_{\text{ESR,input}}} &= 3 \times \frac{1}{53 \text{ m}\Omega} + 2 \times \frac{1}{3.375 \text{ m}\Omega} + 2 \times \frac{1}{15 \text{ m}\Omega} \\ R_{\text{ESR,input}} &= \frac{1}{782.5} \approx 1.278 \text{ m}\Omega \end{aligned}$$

$$R_{\text{ESR,input}} = 1.278 \text{ m}\Omega$$

The ESR loss at the input side is calculated as:

$$\begin{aligned} P_{\text{ESR,input}} &= I_{\text{ripple,rms}}^2 \times R_{\text{ESR,input}} \\ &= (0.481)^2 \times 1.278 \times 10^{-3} \\ &= 296 \mu\text{W} \end{aligned}$$

## Output Capacitor ESR Loss

Similarly, the total ESR of the output capacitor bank is:

$$\frac{1}{R_{\text{ESR, output}}} = 5 \times \frac{1}{6 \text{ m}\Omega} + 2 \times \frac{1}{3.375 \text{ m}\Omega} + 2 \times \frac{1}{15 \text{ m}\Omega}$$

$$R_{\text{ESR, output}} = 0.6415 \text{ m}\Omega$$

The ESR loss at the output side is:

$$\begin{aligned} P_{\text{ESR, output}} &= I_{\text{ripple, rms}}^2 \times R_{\text{ESR, output}} \\ &= (0.481)^2 \times 0.6415 \times 10^{-3} \\ &= 148 \mu\text{W} \end{aligned}$$

## Summary

Both input and output ESR losses are relatively **small** compared to the total system power.

Location	Total ESR	Ripple RMS Current	ESR Loss
Input Capacitor Bank	1.278 mΩ	0.481 A	296 μW
Output Capacitor Bank	0.6415 mΩ	0.481 A	148 μW

Table 3: Summary of Capacitor ESR Power Losses at 20% Ripple Current

## 4.5 Expected ESR Loss of Four corner operating points

Operating Point	$V_{\text{in}}$ Ripple (V)	$V_{\text{out}}$ Ripple (V)	$I_L$ Ripple (A)
$V_{\text{in}} = 20 \text{ V}, P = 100 \text{ W}$	0.2425	0.0625	0.57
$V_{\text{in}} = 16 \text{ V}, P = 100 \text{ W}$	0.131	0.056	0.355
$V_{\text{in}} = 24 \text{ V}, P = 100 \text{ W}$	0.25	0.0925	0.72
$V_{\text{in}} = 16 \text{ V}, P = 50 \text{ W}$	0.1425	0.05	0.341
$V_{\text{in}} = 24 \text{ V}, P = 50 \text{ W}$	0.675	0.0675	0.69

Table 4: Measured Peak-to-Peak Ripple Values at Different Operating Points

Operating Point	$V_{\text{in}}$ Ripple (%)	$V_{\text{out}}$ Ripple (%)	$I_L$ Ripple (%)
$V_{\text{in}} = 20 \text{ V}, P = 100 \text{ W}$	1.2756%	0.5501%	6.9828%
$V_{\text{in}} = 16 \text{ V}, P = 100 \text{ W}$	0.8814%	0.5042%	4.3518%
$V_{\text{in}} = 24 \text{ V}, P = 100 \text{ W}$	1.1216%	0.8122%	8.8204%
$V_{\text{in}} = 16 \text{ V}, P = 50 \text{ W}$	0.9067%	0.4315%	8.2179%
$V_{\text{in}} = 24 \text{ V}, P = 50 \text{ W}$	2.9840%	0.5763%	16.6037%

Table 5: Measured Ripple Percentages at Different Operating Points

Operating Point	$I_{\text{ripple,rms}}$ (A)	$P_{\text{ESR,input}}$ ( $\mu\text{W}$ )	$P_{\text{ESR,output}}$ ( $\mu\text{W}$ )
$V_{\text{in}} = 20 \text{ V}, P = 100 \text{ W}$	0.1646	34.65	17.39
$V_{\text{in}} = 16 \text{ V}, P = 100 \text{ W}$	0.1025	13.43	6.70
$V_{\text{in}} = 24 \text{ V}, P = 100 \text{ W}$	0.2078	55.15	27.37
$V_{\text{in}} = 16 \text{ V}, P = 50 \text{ W}$	0.0984	12.38	6.22
$V_{\text{in}} = 24 \text{ V}, P = 50 \text{ W}$	0.1992	50.66	25.14

Table 6: Calculated Capacitor ESR Losses at Different Operating Points

Since the design are using multiple parallels of MLCCs and Electrolytic Capacitors, the total ESR of input and output is extremely small.

## 5 Gate Drive Circuit

### 5.1 Level Shifting of Gate Driver Circuit: e.g., IR2125

- In many converters, not all devices share a common source.
- High-side devices have “flying” source terminals due to switch node voltage.
- High-side driver must be “floating” relative to system ground, requiring a **shift of reference level to the switch node voltage**.
- To power high-side drivers, signal isolation and a floating power supply are needed.

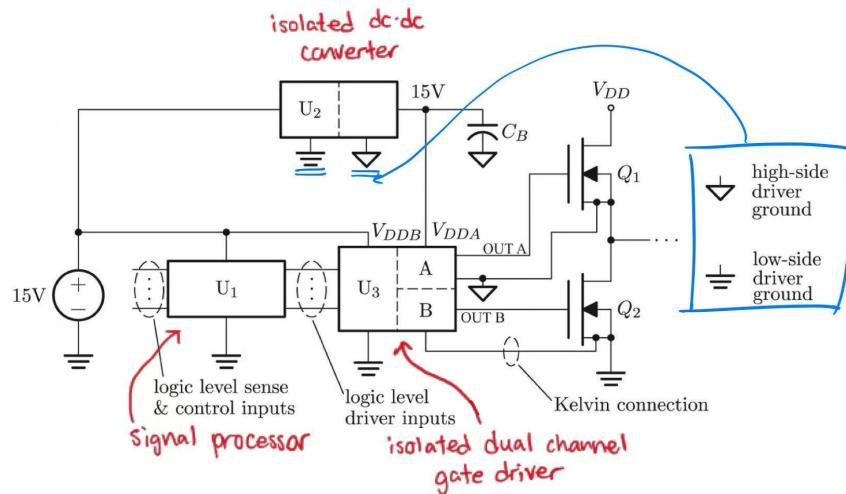


Figure 33: Level Shifting of Gate Driver (Credit: Prof. Bole's Slides)

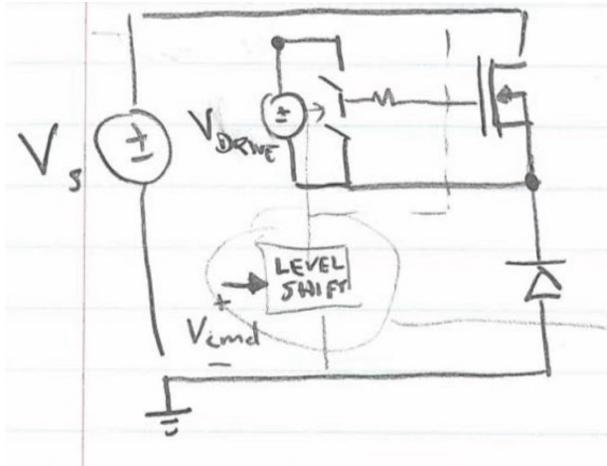


Figure 34: Level Shifting of Gate Driver (Credit: MIT Open Course)

To briefly explain how level shifting works, we usually use an isolated DC/DC converter to have low-side driver ground and high-side driver ground at the same time, which offers two isolated ground and can make high-side driver have a higher reference ground.

Given the above circuit diagram of an example of a level shifter using an isolated DC/DC converter,  $V_{DD} = 15V$ , when there's no gate signal, the high side switch of  $V_{DRIVE}$  turns off, and low side switch turns on and ground is connected to the Gate of the MOSFET; when there's gate signal, the high side switch of  $V_{DRIVE}$  turns on and  $V_{DRIVE}$  is connected to the Gate of MOSFET.

Another version of the Level Shifting can be explained in the first figure, the isolated DC/DC converter has two referenced ground, the high-side driver ground of which is placed at  $V_{sw}$ , basically because of the characteristics of the transformer. As long as the level shifter receives the gate signal, it can sense the gate signal and activate the referenced ground and rise it up to  $V_{DRIVE}$ .

## 5.2 Bootstrap Circuit:

- Simple alternative to isolated dc/dc converter for powering high-side driver.
- Capacitor must be rated for  $V_{driver}$ , but diode must be rated for  $V_{DD}$ .

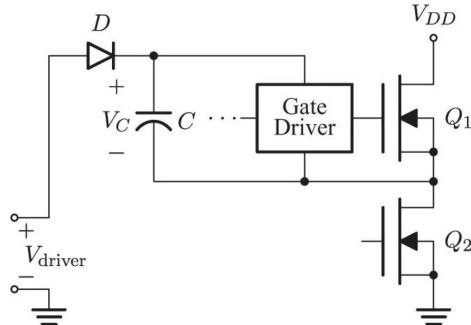


Figure 35: Bootstrap Circuit Schematic

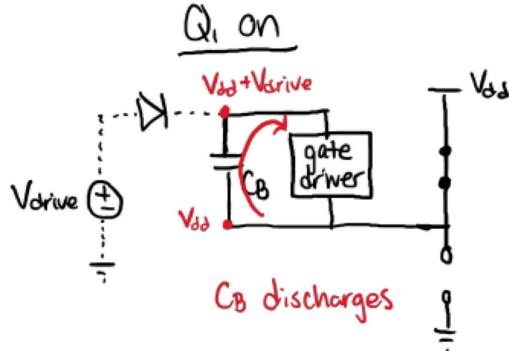


Figure 36: Bootstrap Circuit when  $Q_1$  is ON

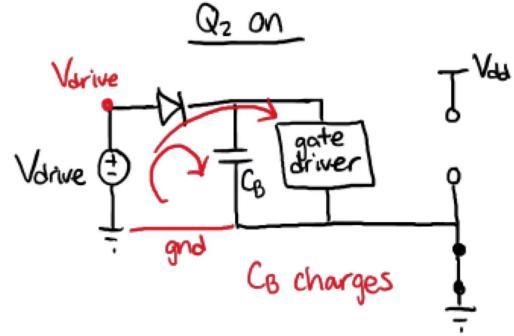


Figure 37: Bootstrap Circuit when  $Q_2$  is ON

Actually the circuit diagrams above is super clear, but I still want to briefly explain it. When  $Q_2$  is on, bootstrap capacitor gets charged through the current from the diode. Since  $V_{drive}$  and bootstrap capacitor has the same ground, current can charge the  $C_B$ ; when  $Q_1$  is on, the positive side of bootstrap capacitor is connected to the HB of the gate driver, such that a voltage of  $V_{dd} + V_{drive}$  is transmitted to the gate driver.

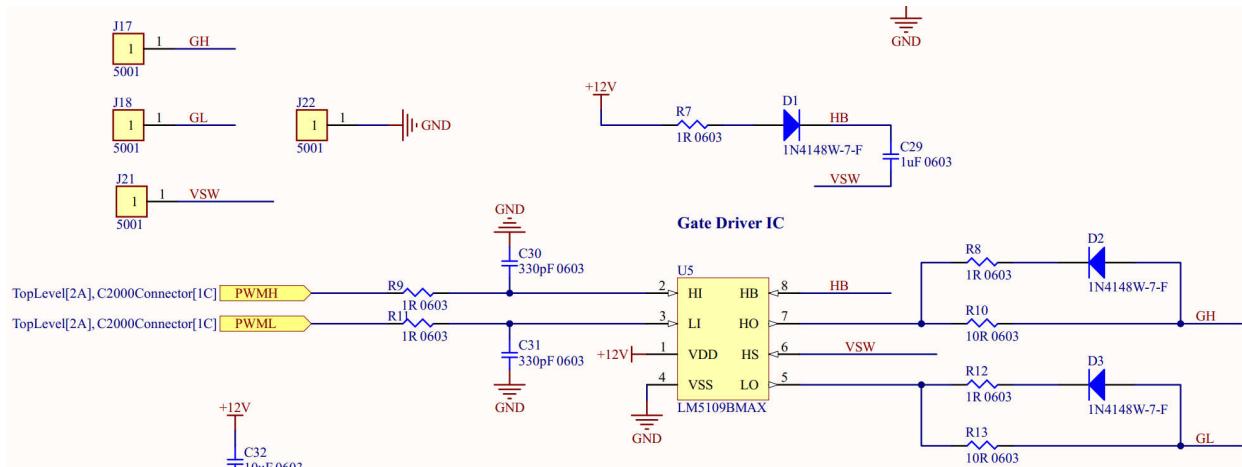


Figure 38: Schematic of Gate Driver

- **HB:** High-side bootstrap supply voltage.
- **HO:** High-side gate driver output.
- **HS:** High-side source / switching node.
- **HI:** High-side gate driver input (logic signal).
- **LI:** Low-side gate driver input (logic signal).
- **LO:** Low-side gate driver output.
- **VDD:** Driver chip supply voltage.
- **VSS:** Driver chip ground (system ground).

From the schematic, to implement the bootstrap capacitor in the gate driver circuit, we shall add a diode in series with bootstrap capacitor and a resistor between  $V_{DD}$ ,  $HB$  and  $V_{SW}$ , which prevents large current.

For the input filtering, the design chooses a resistor with  $R = 1\Omega$  and  $C = 330pF$ . For the RC-filtering system,  $w_p = \frac{1}{RC} = 3.03GHz$ ,  $\tau = RC = 0.33ns$ , which filters the frequency larger than the fundamental frequency  $100kHz$  and have a comparatively fast response to switching gate signals.

### 5.3 Input Filtering and Gate Loop Tuning

**Input Filtering:** At HI and LI, the design applies a low-pass RC filter by using  $1\Omega$  and  $330pF$  to filter the switching gate signal and have a comparatively clean DC output.

#### Gate Loop Tuning:

- Step in  $i_G$  may cause ringing of  $V_{GS}$  due to small inductance in gate loop.
- Adding gate resistance  $R_g$  slows the switching speed and damps ringing.
- Separate turn-on and turn-off paths allow for separate tuning.

We use a resistor in parallel with a diode in a series with another resistor to avoid dangerous ringings of the gate signals, which might accidentally turn the MOSFET on and off at wrong time.

The design shown in the schematic uses a turn-on resistance of  $R_{10} = R_{13} = 10\Omega$  and turn-off resistance of  $10\Omega||1\Omega \approx 0.9\Omega$ , which gives the MOSFET a comparatively small  $t_r, t_f$  while having no errors in turning on and off.

$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 50V$
$t_r$	Rise Time	—	56	—		$I_D = 22A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G = 3.6\Omega$
$t_f$	Fall Time	—	40	—		$R_D = 2.9\Omega$ , See Fig. 10④⑥

Figure 39:  $R_g$  of IRL3705NPBF

According to the datasheet given, the default settings of  $R_G = 3.6\Omega$ ,  $t_r = 56ns$ ,  $t_f = 40ns$  at this time. To minimize the overlapping loss, we shall reduce the turn-on and turn-off resistance (ringings in acceptable range not to have a wrong turning on or turning off time).

In final design,  $R_{10}, R_{13}$  gets resoldered and replaced by  $1\Omega$  to have a smaller  $t_r, t_f$  to reduce the overlap loss.

## 6 Sensing Circuit

### 6.1 Sensed Quantities for MPPT

- Output voltage sensing ( $V_{out}$ ) for regulation and monitoring.
- Output current sensing ( $I_{out}$ ) for system protection (optional).

Since we only need to get the maximum power of the output without the efficiency, to reduce unnecessary sensing parts,  $V_{in}$  and  $I_{in}$  could be ignored in sensing.

## 6.2 Voltage and Current Sensing Analysis

### 6.2.1 Voltage Sensing Circuit:

The design uses unity-gain feedback of an op-amp, which has approximately infinity  $R_{in}$  and zero  $R_{out}$ . It can accurately receive  $V_{OA}$  and output a clean  $V_{ADC}$  with minor offset.

In real design, LM358DR is used:

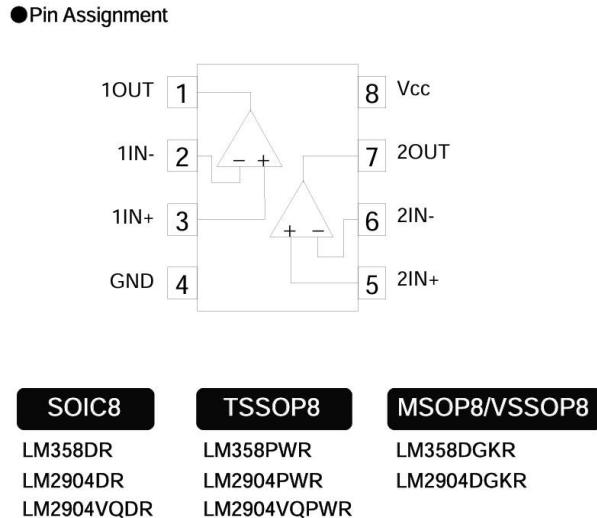


Figure 40: Pin Assignment of LM358DR

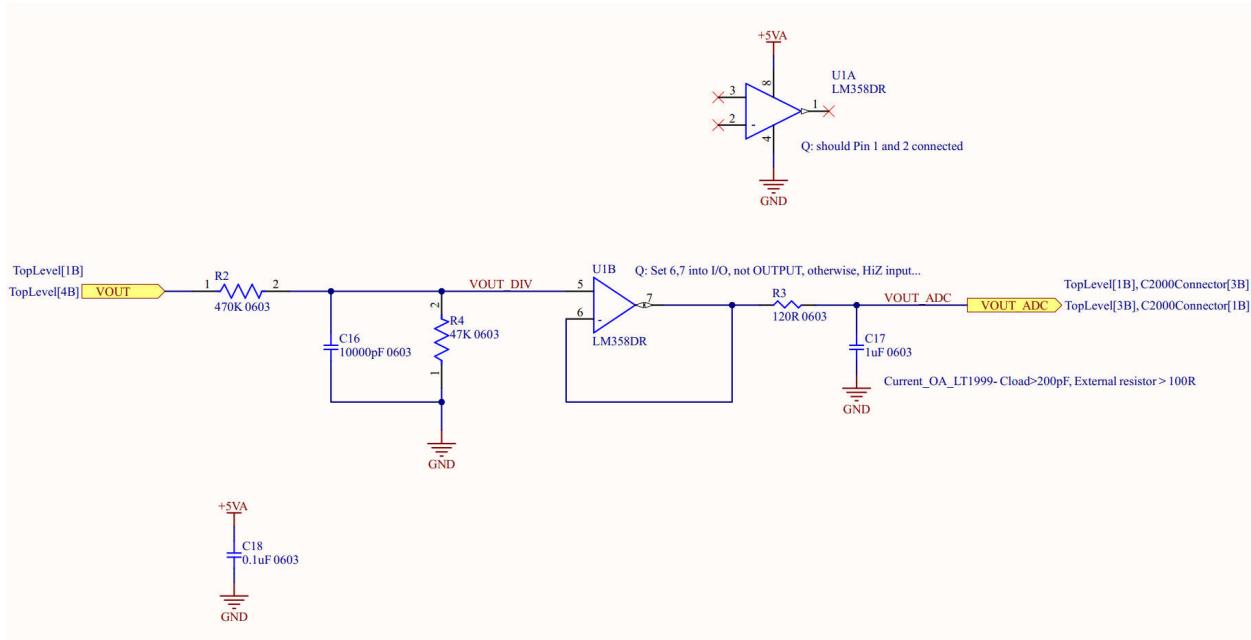


Figure 41: Schematic of Voltage Sensing Circuit

Large Signal Voltage Gain	AVD	25°C	25	100	-	25	100	-	V/mV	V <sub>CC</sub> =15[V] VO=1[V] to 11[V] RL≥2[kΩ]
---------------------------	-----	------	----	-----	---	----	-----	---	------	--

Figure 42: Large signal Gain of LM358DR

From the datasheet, the open-loop gain of LM358DR under environment temperature is 100V/mV, which is 100000V/V, the gain error in unity gain is  $\frac{1}{A_0 f} = \frac{1}{1000000} \approx 0$ .

Input Offset Current (*1)	IIO	25°C	-	2	50	-	2	50	nA	VO=1.4[V]	98
		Full range	-	-	150	-	-	150			

Figure 43: Input Current Offset of LM358DR

From the datasheet, the input current offset  $I_{offset,max} = 50nA$ . Compared to resistor division circuit,  $I_{DIV} = \frac{V_{OUT}}{R_2+R_4} = \frac{12V}{470k\Omega+47k\Omega} \approx 23.21\mu A$ . The offset of LM358DR is within the acceptable range.

Since the sensing circuit is in parallel with the load, we have to make sure the sensing circuit would flow through as small current as possible. Additionally, we have to make  $V_{out}$  drop down to an acceptable value for ADC GPIO range of C2000. Therefore, the design chooses  $\frac{R_4}{R_2+R_4} = \frac{47k\Omega}{470k\Omega+47k\Omega} = \frac{1}{11}$  as resistor division. To get a clean DC value from noisy  $V_{out}$ , the design also adds up a capacitor  $C_{16}$  in parallel with  $R_4$  as an RC filter.

$$V_{ADC} = \frac{V_{out}}{11}$$

The schematic also adds an RC filter to the ADC GPIO as a filter to get a stable input of ADC, otherwise,  $V_{ADC}$  would oscillates greatly.

### 6.2.2 Current Sensing Circuit:

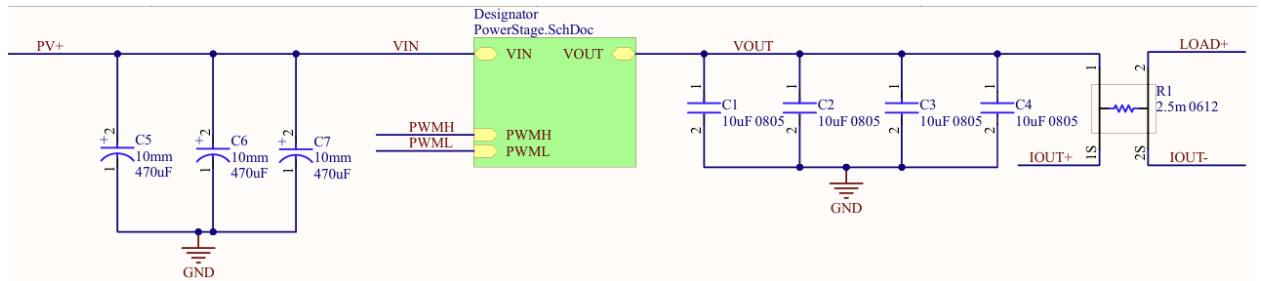


Figure 44: Schematic including  $R_{sense}$

$R_1$  is the sensing resistor for measuring  $I_{out}$ . The principle is easy to understand: the voltage across the sensing resistor would be the input of a current Op-Amp, and the Op-Amp multiplies the voltage by a gain of 50/100 and the  $I_{out,sense}$  is the signal that the C2000 would receive.

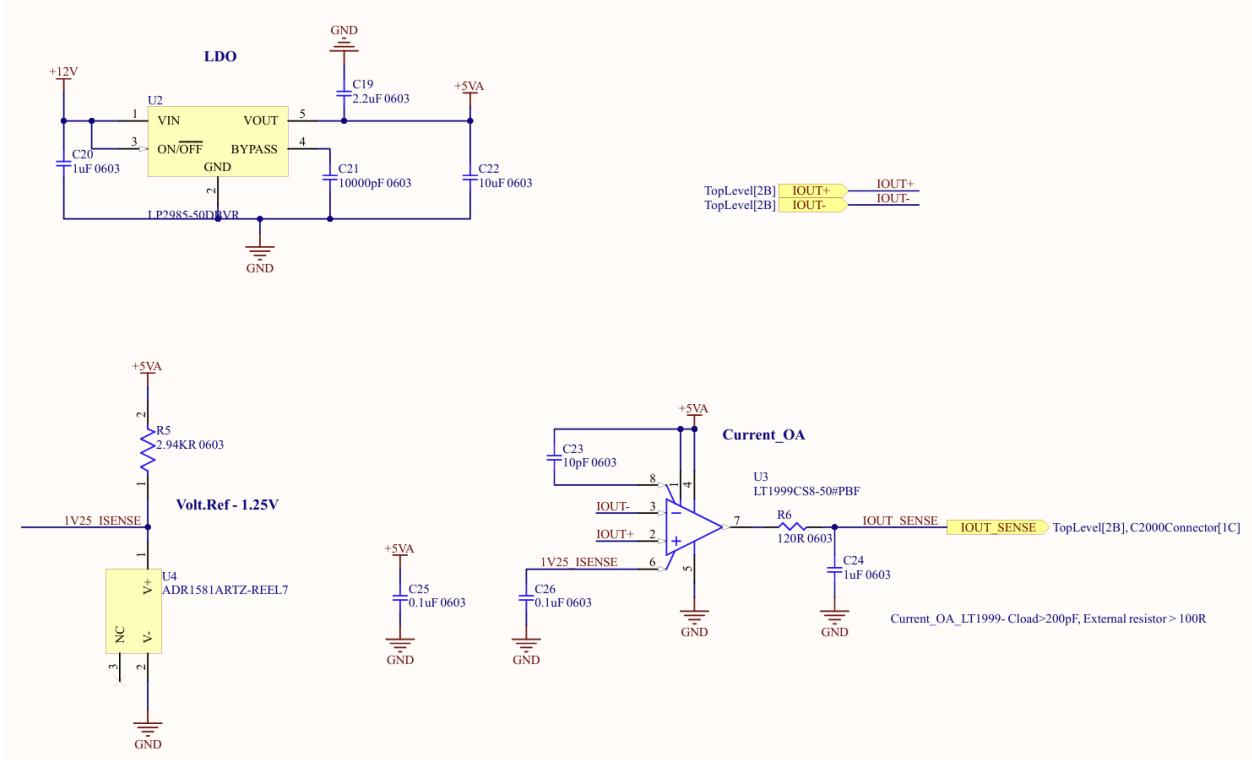


Figure 45: Schematic of Current Sensing Circuit

We have these circuit diagrams and schematic, but I still want to redesign it step by step.

- **Step 1: Define the maximum load current**

The maximum output current is calculated by applying a 20% design margin over the nominal full-load current:

$$\begin{aligned}
 I_{\max} &= 8.333 \text{ A} \times (1 + 20\%) \\
 &= 10 \text{ A} \\
 I_{\text{out}} &\in [0, 10] \text{ A}
 \end{aligned}$$

- **Step 2: Define the ADC input range and Vref**

**Table 3-1. ADC Input Settling Design Worksheet (F280049 Example)**

Symbol	Description	Value	Comments
$V_{fs}$	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)

Figure 46: Input Range of C2000 ADC

The ADC input range is 0 V to 3.3 V. To avoid dropping below ground potential, we introduce a reference voltage at the amplifier, typically:

$$V_{\text{ref}} = 1.25 \text{ V}$$

Thus, the amplifier output voltage should swing from 1.25 V to 3.3 V.

- **Step 3: Determine the sense resistor and gain combination**

The amplifier output voltage is:

$$V_{\text{out}} = V_{\text{ref}} + I_{\text{out}} \times R_{\text{sense}} \times \text{Gain}$$

At maximum current ( $I_{\text{max}} = 10 \text{ A}$ ), the desired output is 3.3 V. Therefore, the voltage increment from  $V_{\text{ref}}$  is:

$$\Delta V = 3.3 \text{ V} - 1.25 \text{ V} = 2.05 \text{ V}$$

Setting up the equation:

$$\Delta V = I_{\text{max}} \times R_{\text{sense}} \times \text{Gain}$$

Solving for  $R_{\text{sense}}$  at different gains:

$A_v$	Gain	LT1999-10 LT1999-20 LT1999-50	● ● ●	9.95 19.9 49.75	10 20 50	10.05 20.1 50.25	V/V V/V V/V

Figure 47: Different Op-Amp Gain Options

Amplifier Gain	Max $R_{\text{sense}}$	Notes
20	$\frac{2.05}{10 \times 20} = 10.25 \text{ m}\Omega$	Moderate Rsense
50	$\frac{2.05}{10 \times 50} = 4.1 \text{ m}\Omega$	Good tradeoff
100	$\frac{2.05}{10 \times 100} = 2.05 \text{ m}\Omega$	Low Rsense
200	$\frac{2.05}{10 \times 200} = 1.025 \text{ m}\Omega$	Very small, challenging layout

Table 7: Sense Resistor Values for Different Amplifier Gains with 1.25 V  $V_{\text{ref}}$

- **Step 4: Practical selection**

In practice:

- Gains of 50 or 100 are most practical for balancing sense voltage and noise immunity.
- Selecting  $R_{\text{sense}}$  between 2 mΩ and 5 mΩ keeps the sense voltage in a measurable range while minimizing power dissipation.
- Very small  $R_{\text{sense}}$  values (e.g., < 2 mΩ) require careful PCB layout to minimize noise pickup and ensure accuracy.

For this design, we shall use a good tradeoff with  $R_{\text{sense}} = 2.5 \text{ m}\Omega$ , Gain is 50, so that  $V_{\text{ADC}}$  is within C2000 ADC input voltage range (0, 3.3)V.

$$\begin{aligned}
 V_{\text{ADC}} &= V_{\text{ref}} + A_v \cdot (I_{\text{sense}} \cdot R_{\text{sense}}) \\
 &= 1.25 \text{ V} + 50 \times (I_{\text{sense}} \cdot 2.5 \text{ m}\Omega) \\
 I_{\text{sense}} &\in [0, 10] \text{ A} \\
 \Rightarrow V_{\text{ADC}} &\in [1.25, 2.5] \text{ V}
 \end{aligned}$$

Since the sensing resistor needs an extremely accurate resistance, we shall use resistors with **Kelvin Connection**:

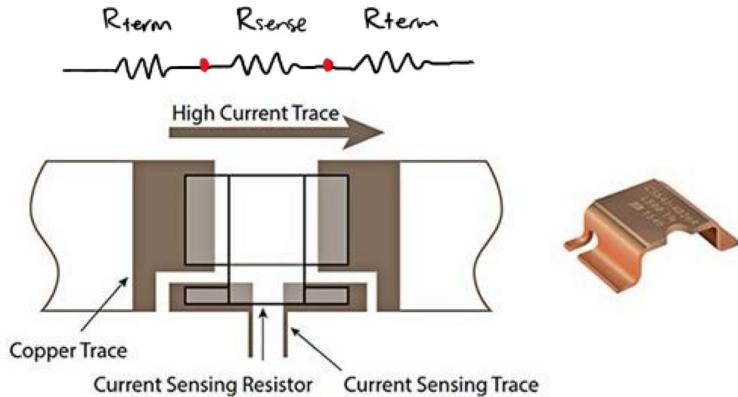


Figure 48: Kelvin Connection (Credit: Prof. Bole's Slides)

### 6.3 Components Selection and Utilization:

#### Voltage Sensing Components

The voltage sensing stage uses a resistor divider to scale down the measured voltage into the ADC range, followed by an op-amp buffer stage and low-pass filtering for noise reduction.

- **Resistor Divider:**

- $470\text{ k}\Omega$  (RN73R1JTTD4703B25)
- $47\text{ k}\Omega$  (ERJ-PB3B4702V)
- Divider Ratio:  $\frac{47\text{ k}\Omega}{470\text{ k}\Omega + 47\text{ k}\Omega} = \frac{1}{11}$

- **Buffer Op-Amp:**

- LM358DR — Dual General-Purpose Op-Amp

- **Filter Capacitors:**

- $10\text{ nF}$  filter capacitor at the input
- $1\text{ }\mu\text{F}$  filter capacitor at the op-amp output

$$w_{p,in} = \frac{1}{47\text{ k}\Omega \cdot 10000\text{ pF}} = 2.13\text{ kHz}$$

$$w_{p,out} = \frac{1}{120\Omega \cdot 1\mu\text{F}} \approx 8.33\text{ kHz}$$

For filter capacitors, we need to make sure  $w_p < f_s$ , so that the fundamental frequency can get filtered and has less noise.

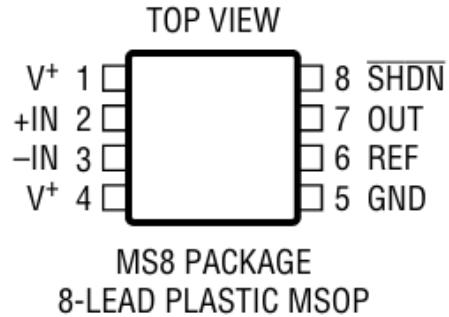
#### Current Sensing Components

The current sensing block uses a dedicated high-precision current sense amplifier with reference biasing and low dropout auxiliary power.

- **Current Sense Amplifier:**

- LT1999CS8-50 —Current sense amplifier with gain of 50

### ORIGINAL MSOP PINOUT



$$T_{JMAX} = 150^\circ\text{C}, \theta_{JA} = 300^\circ\text{C/W}$$

Figure 49: Pin Configuration of LT1999-50

- **V<sup>+</sup>**: Positive supply voltage input, typically 5 V for powering the amplifier.
- **REF**: Reference voltage input that sets the amplifier's zero-current output baseline (e.g., 1.25 V).
- **SHDN**: Active-low shutdown pin. If pulled low, disables the amplifier to save power. Tie to V<sup>+</sup> if unused (Add a capacitor).
- **NC**: No internal connection; used only in the FMEA version and can be left floating.

- **Voltage Reference:**

- ADR1581ARTZ — High-accuracy 1.25 V reference

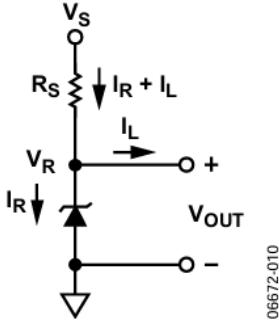


Figure 10. Typical Connection Diagram

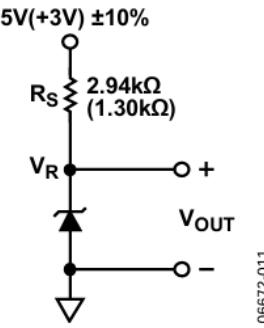


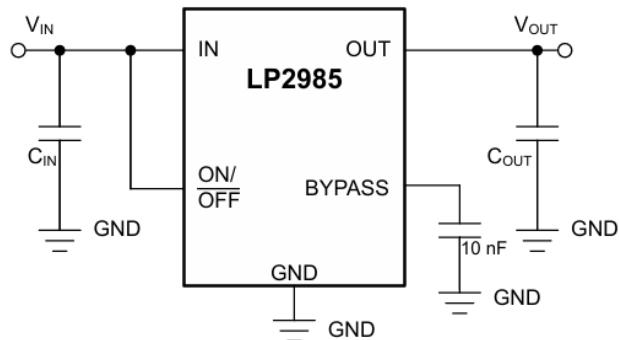
Figure 11. Typical Connection Diagram

Figure 50: Typical Connection Diagram of ADR1581ARTZ-REEL7

We choose  $R_s = 2.94k\Omega$  and  $V_s = 5V$  to get  $1.25V V_R$ .

- **Auxiliary Power Supply:**

- LP2985-50DBVR — 5 V Low Dropout Regulator (LDO)



**Typical Application Circuit**

Figure 51: Typical Connection Diagram of LP2985-50DBVR

## 5 Pin Configuration and Functions

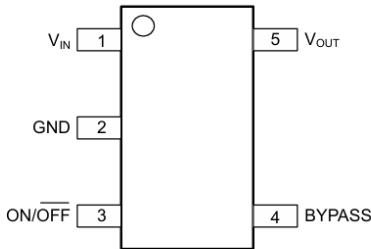


Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between BYPASS pin and ground reduces reference voltage noise. See the <a href="#">Recommended Operating Conditions</a> section for more information.
GND	2	—	Ground
ON/OFF	3	I	Enable pin for the LDO. Driving the ON/OFF pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the <a href="#">Electrical Characteristics</a> table. Tie this pin to V <sub>IN</sub> if unused.
V <sub>IN</sub>	1	I	Input supply pin. Use a capacitor with a value of 1 µF or larger from this pin to ground. See the <a href="#">Input and Output Capacitor Requirements</a> section for more information.
V <sub>OUT</sub>	5	O	Output of the regulator. Use a capacitor with a value of 2.2 µF or larger from this pin to ground. <sup>(1)</sup> See the <a href="#">Input and Output Capacitor Requirements</a> section for more information.

(1) The nominal output capacitance must be greater than 1 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 µF.

Figure 52: Typical Pin Configuration of LP2985-50DBVR

- Sensing Resistor:

- 5 mΩ, 1% current sense resistor (D1FCP0612D2M50FF-T5)

It's worth mentioning that sensing resistor can have conduction loss:

$$\begin{aligned}
 P_{sense} &= I_{out}^2 \cdot R_{sense} \\
 &= 8.333A^2 \times 2.5m\Omega \\
 &= 0.1736W
 \end{aligned}$$

## 7 Control

### 7.1 PWM Generation using Microcontroller

- Use of TI C2000 microcontroller for PWM signal generation.
- Configuration of ePWM module:
  - Set switching frequency (e.g., 100 kHz).
  - Set duty cycle resolution and time-base counter mode.
  - Synchronization between complementary outputs (for high-side and low-side MOSFETs).

- Dead-time insertion to avoid shoot-through:
  - Determined based on MOSFET rise/fall times and gate drive characteristics.

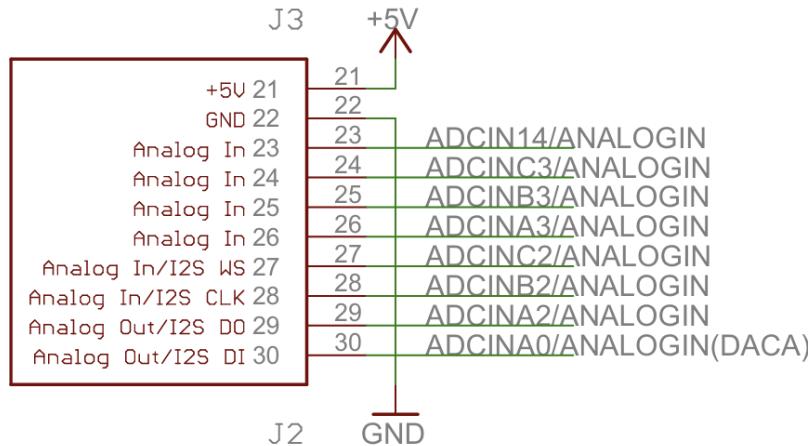


Figure 53: Pin Configuration of C2000-F28379D

```

1 // cpub1_init.c
2
3 void configure_EPWM(void)
4 {
5     EALLOW;
6     CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;           // stop TBCTR incrementing
7     EDIS;
8
9     EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;           // CLKDIV=1      TBCLK=EPWMCLK/(HSPCLKDIV*CLKDIV)
10    EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;          // HSPCLKDIV=1
11    EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;   // Up-down mode
12
13    EPwm1Regs.TBPRD = EPWM_TBPRD;                   // Counter period
14
15    EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;      // Shadow mode active for CMPA
16    EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;      // Shadow mode active for CMPB
17    EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;     // Load on TBCTR=TBPRD
18    EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;     // Load on TBCTR=TBPRD
19
20    EPwm1Regs.CMPA.bit.CMPA = EPWM_CMP_INIT;        // Initial value of CMPA
21
22    EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;             // Set EPWMA low on TBCTR=CMPA
23    during up count
24    EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;               // Set EPWMA high on TBCTR=CMPA
25    during down count
26
27    EPwm1Regs.TBCTL.bit.SYNCSEL = TB_SYNC_IN;         // Pass through SYNCIN signal (
28    doesn't matter for what we're doing)
29    EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;           // Disable loading of PHS
30    register on sync event                           // Note: if this is enabled on
31    EPWM1, the input X-BAR should be reconfigured to something
32                                // other than GPIO0 (
33    otherwise TBCTR will be loaded with TBPHS when EPWM toggles)

```

```

29 EPwm1Regs.TBPHS.bit.TBPHS = 0;           // load TBCTR = 0 on phase load
30 event (value doesn't matter if PHSEN = 0)
31 EPwm1Regs.TBCTR = 0;                     // start counter with value of 0
32 EPwm1Regs.TBCTL.bit.PHSDIR = TB_UP;      // start counting up
33
34 EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary –
35 EPWMxB is inverted.
36 EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // Enable both falling and
rising edge delays
37 EPwm1Regs.DBFED.bit.DBFED = EPWM_DEADTIME; // Set delay for falling edge (
DBFED)
38 EPwm1Regs.DBRED.bit.DBRED = EPWM_DEADTIME; // Set delay for rising edge (
DBRED)
39
40 // SOC trigger (for ADC conversions)
41 EPwm1Regs.ETSEL.bit.SOCASEL = ET_CTR_ZERO; // Generate SOCA on TBCTR = CMPA
when counting down
42
43 EPwm1Regs.ETPS.bit.SOCAPRD = 1;           // This bit sets how many
SOCASEL events have to occur before a SOCA pulse is generated
44 st event                                     // We want to generate SOCA on 1
45
46 EPwm1Regs.ETSEL.bit.SOCAEN = 1;           // Enable SOCA generation
47
48 EALLOW;
49 CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;     // start TBCTR incrementing
50 EDIS;
51 }

```

```

1 // cpul_init.c
2
3 void configure_ADC(void){
4     /*
5      * ADC Mapping:
6      *   ADCINA2 (ADCA Channel 2): V_OUT PIN29
7      *   ADCINB2 (ADCB Channel 2): V_IN NOT USED
8      *   ADCINC2 (ADCC Channel 2): I_OUT PIN27
9      *   ADCIND2 (ADCD Channel 2): I_IN NOT USED
10     */
11
12     // ADCA Configuration
13     AdcaRegs.ADCCTL2.bit.PRESCALE = 6; // ADCCLK = SYSCLK / 4
14     AdcSetMode(ADC.ADCA, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
15     AdcaRegs.ADCCTL1.bit.INTPULSEPOS = 1;
16     AdcaRegs.ADCCTL1.bit.ADCPWDNZ = 1;
17     DELAY_US(1000); // 1ms delay for ADC to power up
18
19     AdcaRegs.ADCSOC0CTL.bit.CHSEL = 2; // Select ADCINA2
20     AdcaRegs.ADCSOC0CTL.bit.ACQPS = ADC_ACQ_WINDOW;
21     AdcaRegs.ADCSOC0CTL.bit.TRIGSEL = 5; // Trigger: EPWM1 SOCA
22     AdcaRegs.ADCSOCPRICTL.bit.SOC_PRIORITY = 1;
23
24     AdcaRegs.ADCINTSEL1N2.bit.INT1SEL = 0; // EOC0 sets ADCINT1
25     AdcaRegs.ADCINTSEL1N2.bit.INT1CONT = 1;
26     AdcaRegs.ADCINTSEL1N2.bit.INT1E = 0;
27     AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; // Clear flag
28

```

```

29 // ADCC Configuration
30 AdccRegs.ADCCTL2.bit.PRESCALE = 6;
31 AdcSetMode(ADC_ADCC, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
32 AdccRegs.ADCCTL1.bit.INTPULSEPOS = 1;
33 AdccRegs.ADCCTL1.bit.ADCPWDNZ = 1;
34 DELAY_US(1000);

35
36 AdccRegs.ADCSOC0CTL.bit.CHSEL = 2;           // Select ADCINC2
37 AdccRegs.ADCSOC0CTL.bit.ACQPS = ADC_ACQ_WINDOW;
38 AdccRegs.ADCSOC0CTL.bit.TRIGSEL = 5;
39 AdccRegs.ADCSOCPRICTL.bit.SOC_PRIORITY = 1;

40
41 AdccRegs.ADCINTSEL1N2.bit.INT1SEL = 0;
42 AdccRegs.ADCINTSEL1N2.bit.INT1CONT = 1;
43 AdccRegs.ADCINTSEL1N2.bit.INT1E = 0;
44 AdccRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;
45 }

```

```

1 // GlobalVarialbes.h
2
3 #ifndef GLOBALVARIABLES_H_
4 #define GLOBALVARIABLES_H_
5
6 #define EPWMLTBPRD 650 // 500 -> 100kHz 400->125kHz 625->80kHz 650->77kHz
7
8 #define EPWM_CMP_INIT 250 // initialize with 50% duty ratio
9 // For 89A MOS, it should be >= 400ns deadtime
10 #define EPWMDDEADTIME 20
11 // deadtime in EPWMCLK ticks 5 <=> 50ns, 40 -> 400ns 20->200ns by default
12
13 #define ADC_ACQ_WINDOW 30 // ADC S&H Window Length in SYSCLK cycles
14
15
16 #endif /* GLOBALVARIABLES_H_ */

```

## 7.2 MPPT Algorithm Implementation (Max Power Point Tracking)

### 7.2.1 MPPT Tracking Modes

The MPPT (Maximum Power Point Tracking) algorithm implemented in this project includes three distinct operating modes, controlled by two flags: `flag_track_begin` and `flag_sweep`. Each mode determines how the PWM duty cycle is updated to track the maximum output power of the PV source.

- **Mode 1: Fixed Duty Mode**

- Condition: `flag_track_begin = 0, flag_sweep = 0`
- Description: The PWM module outputs a fixed duty cycle  $D$ . No MPPT tracking is performed in this mode.

- **Mode 2: Perturb and Observe (P&O)**

- Condition: `flag_track_begin = 1, flag_sweep = 0`
- Description:
  - \* The algorithm perturbs the duty cycle  $D$  by a small step size.

- \* Over two control cycles:
  1. Increase  $D$  by one step and measure output power  $P_+$ .
  2. Decrease  $D$  by one step and measure  $P_-$ .
  3. Compare current power  $P_0$ ,  $P_+$ , and  $P_-$ .
  4. Update  $D$  to the value that yields the highest power.

- **Mode 3: Sweep and Lock-In**

- Condition: `flag_track_begin = 1, flag_sweep = 1`
- Description:
  - \* A fast scanning routine sweeps the duty cycle  $D$  from 0.5 to 0.75.
  - \* Output power is sampled across the sweep to estimate the approximate location of the global maximum.
  - \* The duty cycle is initialized to the value yielding the highest power from the sweep.
  - \* After the sweep, the algorithm transitions to the P&O mode for fine adjustment.

### 7.3 Code Snippets and Flow Chart

To improve stability and reduce unnecessary oscillation near the Maximum Power Point (MPP), the tracking algorithm uses a three-step perturbation strategy. The control flow follows:

1. **Step 1: Measure Current Power**

At the current duty cycle  $D$ , measure the instantaneous output power:

$$P_0 = V_{\text{out}} \cdot I_{\text{out}}$$

2. **Step 2: Perturb Duty Cycle in Two Directions**

Apply a small step change  $\Delta D$  in both directions over two control cycles:

- At  $D + \Delta D$ , measure output power  $P_+$
- At  $D - \Delta D$ , measure output power  $P_-$

3. **Step 3: Compare and Update Duty Cycle**

Compare the measured powers  $P_0, P_+, P_-$  and update the duty cycle accordingly:

$$D \leftarrow \begin{cases} D + \Delta D, & \text{if } P_+ > P_0 \text{ and } P_+ > P_- \\ D - \Delta D, & \text{if } P_- > P_0 \text{ and } P_- > P_+ \\ D, & \text{otherwise} \end{cases}$$

This algorithm evaluates power trends in both directions and selects the most promising adjustment. If both perturbations result in lower power than the current operating point, the duty cycle remains unchanged.

```

1 // Measure var. MPPT_power, MPPT_duty, flag_track_begin, flag_sweep
2
3 // IN THIS VERSION: 2 control variables: flag_track_begin, flag_sweep      4/16/2025
4 // #####flag_track_begin##### starts the whole tracking MPPT program

```

```

5 // #####flag_sweep#####: 0—use perturb to find MPPT; 1—sweep first , locate around
6 // MPPT and perturb slowly
7 #include "F28x_Project.h" // this includes all headers needed to interact with
8 // peripherals (ADC, EPWM, etc.)
9 #include "cpu1_init.h"
10
11 // #define ADC_VREF 3.0
12 // #define ADCMAX 4095.0 // 12-bit ADC max value
13
14 volatile Uint16 adc_raw_vout; // 0->4095
15 volatile Uint16 adc_raw_iout;
16 volatile float adc_vout; // 0->3
17 volatile float adc_iout; // 0->3
18
19 volatile Uint16 duty_cmp = EPWM_CMP_INIT;
20 volatile float duty = 0.5;
21
22 volatile Uint16 deadtime_rise = EPWM_DEADTIME;
23 volatile Uint16 deadtime_fall = EPWM_DEADTIME;
24
25 //Simple Perturb and Observe Algorithm
26
27 float MPP_power = 0; //Maximum power point power
28 float MPP_Duty, MPP_Vin; //Maximum power point duty cycle and input voltage
29
30 float duty_step = .005f; //Duty cycle step size
31 // float duty = 0.5f; //Start MPPT Search at the largest panel voltage of 24V
32 float duty_max = 0.75f; //Maximum duty cycle to search over
33 uint32_t wait_time = 10e3; //amount of time to wait after duty cycle update [us]
34 uint32_t wait_time_long = 1e5;// Insert a delay longer than the switching period to
35 // ensure that the duty ratio
36 // is updated at most once per switching period (we are implementing single-update
37 // PWM)
38
39 float iout, vout, pout, iin, vin, pin, eff;
40 // uint32_t adc_iout, adc_vout, adc_iin, adc_vin; //Raw ADC values
41 // float iout_gain, vout_gain, iin_gain, vin_gain;
42 volatile int stop_search = 0; //Flag to stop searching for MPPT
43 volatile int Perturb_Observe = 0; //Flag to enable perturb and observe
44 float duty_inc, duty_dec; // For perturbs
45 volatile int flag_D_inc = 0; // Flag to duty increase
46 volatile int flag_D_dec = 0; // Flag to duty decrease
47 volatile int flag_track_begin = 0; // Flag to begin tracking
48 volatile int flag_sweep = 0; // Flag to do sweeping
49
50 int main(void)
51 {
52     InitSysCtrl(); // Initialize SYSCTL (PLL, Watchdog, etc.)
53
54 #ifdef LAUNCHPAD // include this define in project settings if using a LaunchPad
55 EALLOW;
56     ClkCfgRegs.PERCLKDIVSEL.bit.EPWMCLKDIV = 0; // remove /2 clock division for
57     // LaunchPad to make calculations consistent with ControlCard
58     EDIS;
59 #endif
60
61     InitGpio(); // Initialize GPIO register states

```

```

59 configure_GPIO(); // configure GPIO settings
60
61 DINT;           // Disable ST1.INTM
62 IER = 0x0000; // Disable CPU interrupts
63 IFR = 0x0000; // Clear all CPU interrupt flags
64
65 InitPieCtrl(); // Initialize PIE control registers
66 InitPieVectTable(); // Initialize PIE vector table to default ISR locations...
67 // This will typically be overwritten later
68
69
70 configure_ADC(); // configure ADC settings
71 configure_EPWM(); // configure EPWM settings
72
73 while (1) // main circuit setup
74 {
75     // 2 Mode ctrl:
76     // For safety concern...
77     if (duty <= 0.5)
78     {
79         duty = 0.5;
80     }
81     else if (duty >= 0.75)
82     {
83         duty = 0.75;
84     }
85     // Refresh duty&duty_cmp
86     duty_cmp = EPWM_TBPRD * duty;
87     EPwm1Regs.CMPA.bit.CMPA = duty_cmp;
88
89     EPwm1Regs.DBRED.bit.DBRED = deadtime_rise;
90     EPwm1Regs.DBFED.bit.DBFED = deadtime_fall;
91
92     // ADC read and conversion
93     adc_raw_vout = AdcaResultRegs.ADCRESULT0;
94     adc_vout = ((float)adc_raw_vout / 4095.0) * 3.0 * 11; // float from 12-bit
value to 3V
95     adc_raw_iout = AdccResultRegs.ADCRESULT0;
96     adc_iout = ((float)adc_raw_iout * 0.0059 - 10.0928);
97
98     DELAY_US(wait_time);
99
100    if (!flag_track_begin){
101        stop_search = 0;
102        Perturb_Observe = 0;
103    }
104
105    if (!stop_search && flag_track_begin)
106    {
107        if (flag_sweep){
108            //Sweep over the entire duty cycle range to find the maximum power
point
109            //Wait some time to allow the system to settle
110            DELAY_US(wait_time);
111            //Done: Measure Output Power
112            pout = adc_iout * adc_vout;
113            //update maximum power point
114            if (pout > MPP_power){
115                MPP_Duty = duty;

```

```

116         MPP_power = pout;
117         MPP_Vin = vin;
118     }
119     //finished search, return to MPP
120     if (duty >= duty_max){
121         duty = MPP_Duty;
122         stop_search = 1;
123         Perturb_Observe = 1;
124     }
125     //Continue to search for MPP
126     else{
127         duty += duty_step;
128     }
129 }
130 else{
131     DELAY_US(wait_time);
132     //Done: Measure Output Power
133     pout = adc_iout * adc_vout;
134     MPP_Duty = duty;
135     MPP_power = pout;
136     stop_search = 1;
137     Perturb_Observe = 1;
138 }
139 }
140
141 // Perturb Observe: give a perturb to see changes
142 else if(Perturb_Observe && flag_track_begin){
143     //Done: Implement Perturb and Observe Algorithm
144     //The perturb and observe algorithm first _perturbs_ the current
145     operating point (via a change in duty cycle) and _observes_ if the perturbation
146     yielded an increase or decrease in output power
147     //First measure the current output power and compare it to the
148     previously measured output power
149     //If the current power is higher than the previous power, and the
150     current duty cycle is larger than the previous duty cycle, make another increase
151     in duty cycle
152     //The algorithm should handle both cases where the maximum power
153     requires an increase or decrease in duty cycle
154     //Your controller should be able to continually find the maximum power
155     point of the PV panel (even if the incoming solar power changes)
156
157     // Refresh duty&duty_cmp ***current is MPPT***
158     duty = MPP_Duty;
159     duty_cmp = EPWM1TBPRD * duty;
160     EPwm1Regs.CMPA.bit.CMPA = duty_cmp;
161
162     // when sweeping and found MPPT, perturbation can slow down;
163     // When only using Perturbation to get MPPT, delay may be shorter;
164     if (flag_sweep){
165         DELAY_US(wait_time_long);
166     }
167     else{
168         DELAY_US(wait_time);
169     }
170
171     // ADC read and conversion
172     adc_raw_vout = AdcaResultRegs.ADCRESULT0;
173     adc_vout = ((float)adc_raw_vout / 4095.0) * 3.0 * 11; // float from 12-
174     bit value to 3V

```

```

167     adc_raw_iout = AdccResultRegs.ADCRESULT0;
168     adc_iout = ((float)adc_raw_iout * 0.0059 - 10.0928);
169
170     MPP_power = adc_iout * adc_vout; // Set current status as MPPT ****
171
172     duty_inc = MPP_Duty + duty_step;
173     duty_dec = MPP_Duty - duty_step;
174     // Test duty up and down — Always down, up, down, up...
175     if (flag_D_dec == 0 && flag_D_inc == 0){
176         duty = duty_dec;
177         flag_D_dec = 1;
178     }
179     else if (flag_D_dec == 1 && flag_D_inc == 0){
180         duty = duty_inc;
181         flag_D_inc = 1;
182     }
183     else if (flag_D_dec == 1 && flag_D_inc == 1){
184         flag_D_dec = 0;
185         flag_D_inc = 0;
186     }
187
188     // Refresh duty&duty_cmp
189     duty_cmp = EPWMLTBPRD * duty;
190     EPwm1Regs.CMPA.bit.CMPA = duty_cmp;
191
192     if (flag_sweep){
193         DELAY_US(wait_time_long);
194     }
195     else{
196         DELAY_US(wait_time);
197     }
198
199     // ADC read and conversion
200     adc_raw_vout = AdcaResultRegs.ADCRESULT0;
201     adc_vout = ((float)adc_raw_vout / 4095.0) * 3.0 * 11; // float from 12-
bit value to 3V
202     adc_raw_iout = AdccResultRegs.ADCRESULT0;
203     adc_iout = ((float)adc_raw_iout * 0.0059 - 10.0928);
204
205     // Determine the max power + refresh
206     pout = adc_iout * adc_vout;
207     if (pout > MPP_power){
208         MPP_power = pout;
209         MPP_Duty = duty;
210     }
211 }
212 //Add code to update EPWM register
213 }
214 }
```

## 8 PCB Layout

### 8.1 Critical Loops and Nodes

One of the most critical aspects of PCB layout in a switching power supply is the commutation loop, which includes the path from the input power supply (PV+), through the high-side MOSFET,

switching node (**VSW**), low-side MOSFET, and back to ground (**GND**), ultimately returning to **PV+**. This loop handles high  $di/dt$  currents during switching transitions.

To minimize parasitic inductance and prevent voltage overshoot (from  $V = L \cdot \frac{di}{dt}$ ), the area enclosed by this loop must be minimized. This can be achieved through:

- Minimizing the physical area of the loop by tightly coupling the components.
- Using wide and short traces or polygons.
- Placing ceramic bypass capacitors as close as possible to the power FETs.

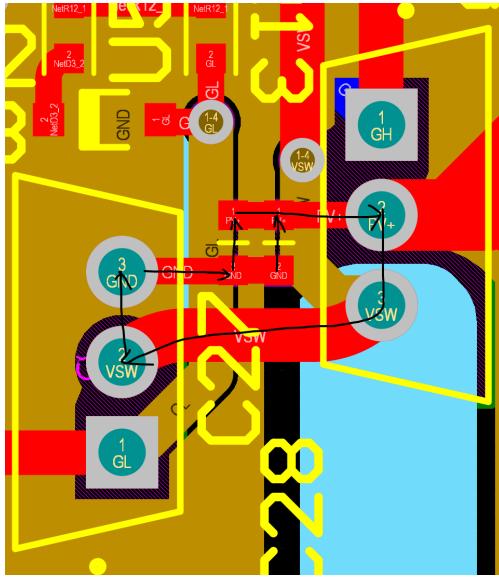


Figure 54: Commutation Loop and Bypass Capacitor

Failure to minimize this loop can result in increased EMI, voltage ringing, and reduced system reliability.

**High-Side Gate Loop:** The loop begins at the gate driver high-side output pin (**GH**), travels through the external gate resistor to the gate of the high-side MOSFET, returns via the source of the high-side MOSFET to the switching node (**VSW**), and then back to the gate driver return path at **HB**.

**Low-Side Gate Loop:** This loop originates from the low-side gate driver output (**L0**), passes through the external gate resistor to the gate of the low-side MOSFET (**GL**), continues to ground through the source of the MOSFET, and returns to **L0** via the gate driver's internal ground reference.

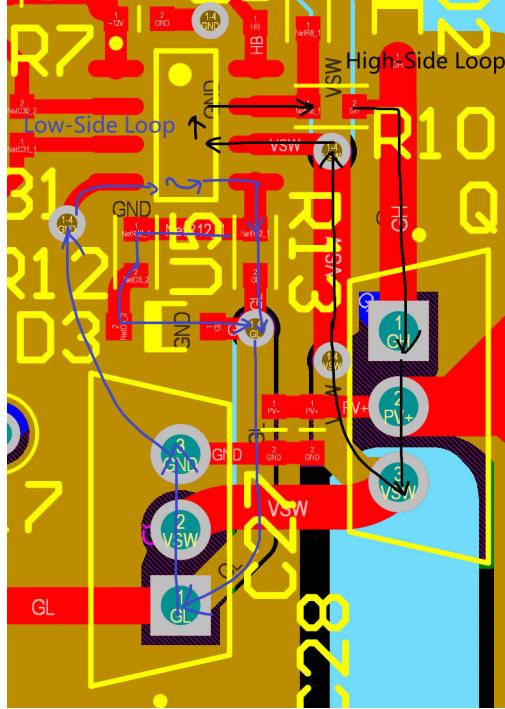


Figure 55: High-Side and Low-Side Gate Drive Loops

### Power Stage Current Return Paths: DC and AC Loops

In the power stage layout, it is crucial to separate and understand the roles of the DC and AC current loops:

**DC Loop:** This loop carries the continuous load current during the on-time of the switching cycle. It flows from the input capacitor ( $PV+$ ), through the high-side MOSFET, inductor, and to the load, then returns through the ground path. Since this loop handles steady-state current, minimizing its resistance is the primary concern to reduce conduction losses and improve efficiency.

**AC Loop:** The AC loop includes the high-frequency switching current paths. This includes the path from the input capacitor ( $PV+$ ) through the switching node ( $VSW$ ) and the MOSFETs, returning through the input capacitor ground. This loop deals with fast-changing currents and must have minimal inductance and parasitic capacitance to reduce voltage ringing, overshoot, and EMI.

To ensure optimal performance:

- **For DC Loop:** Use wide copper pours or planes to minimize resistance.
- **For AC Loop:** Minimize the loop area by tightly coupling the input capacitor with the MOSFETs and using a compact layout to reduce both inductance and capacitive coupling.

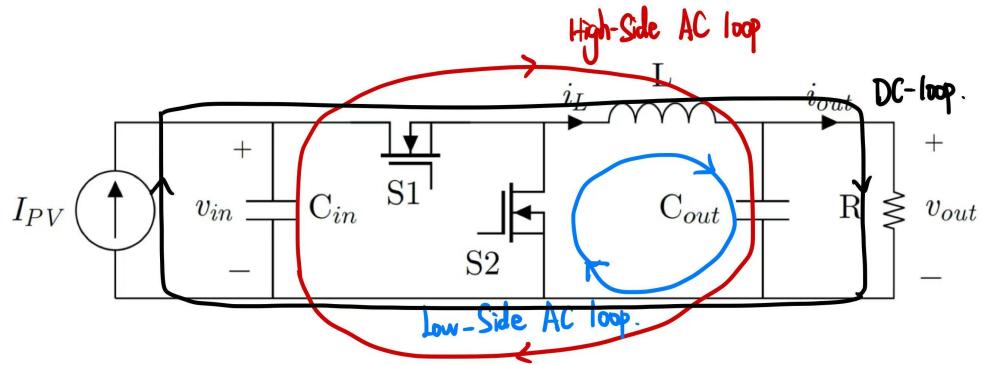


Figure 56: DC and AC Loops

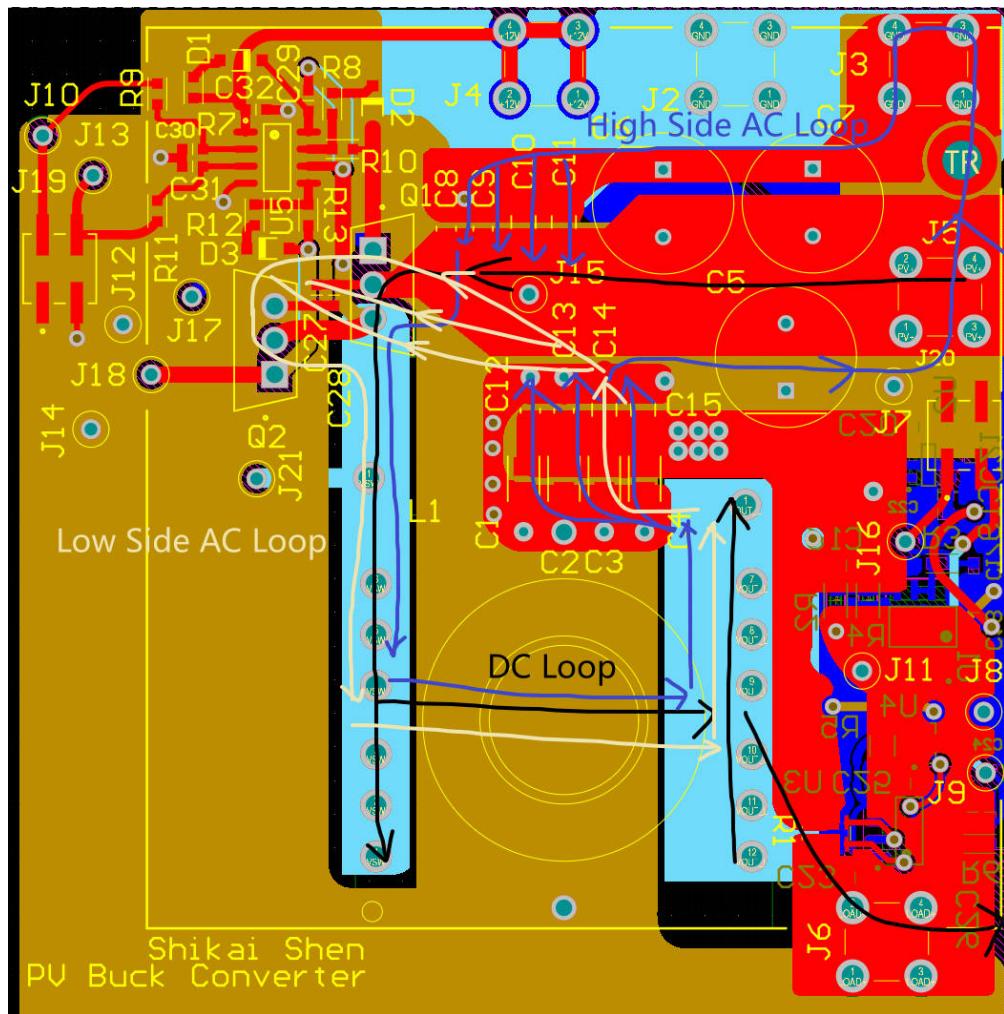


Figure 57: DC and AC Loops on PCB

## 8.2 Analog and Digital Circuit Considerations

Sensitive analog circuitry such as current sensing, voltage sensing, and feedback networks should be carefully placed to avoid noise coupling from high-power switching nodes.

**Placement:** Analog sensing circuits must be placed far away from noisy power rails such as VSW, PV+, and gate drive paths. Components such as operational amplifiers or differential amplifiers used for current and voltage sensing should be located in quiet regions of the PCB to avoid high  $dv/dt$  or  $di/dt$  noise injection.

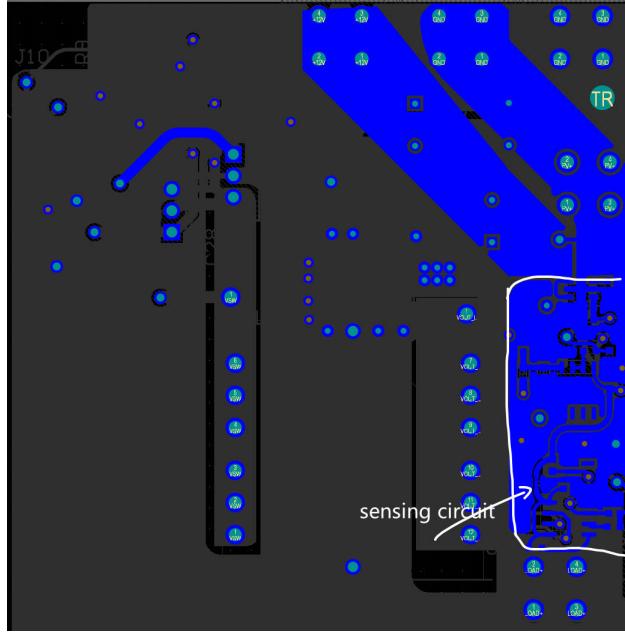


Figure 58: Sensing Circuit on PCB

#### Grounding Strategy:

- **Different Ground References:** Analog and digital circuits often have different ground reference potentials due to voltage drops across power ground planes. A common mistake is tying sensitive analog circuits directly to noisy power ground returns. Instead, a star-grounding method or proper partitioning between power ground and analog ground should be used.
- **DC Ground Return Path:** For sensing circuits that involve DC measurements, the ground return path should have low resistance and a wide trace or plane to reduce ground potential error and improve accuracy.
- **AC Return Path:** For high-frequency signals, return currents tend to flow directly underneath their signal traces. This direct return principle should be respected by ensuring a continuous ground plane beneath high-speed or high-frequency analog signals.

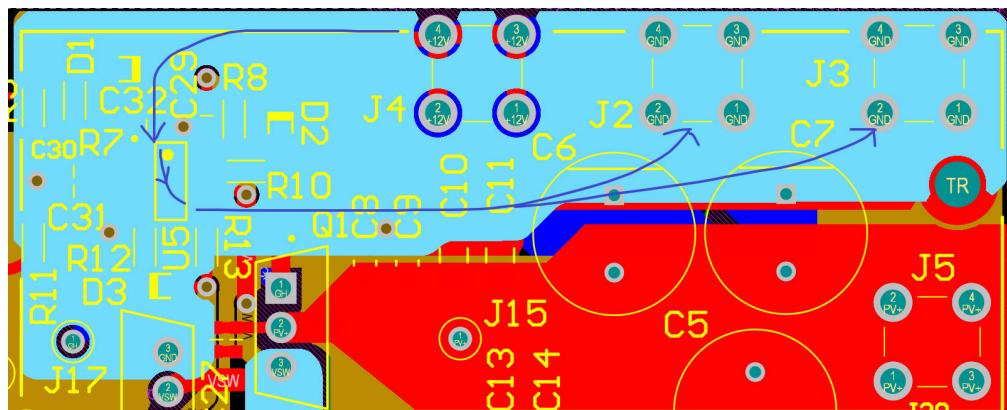


Figure 59: Gate Driver GND Loop

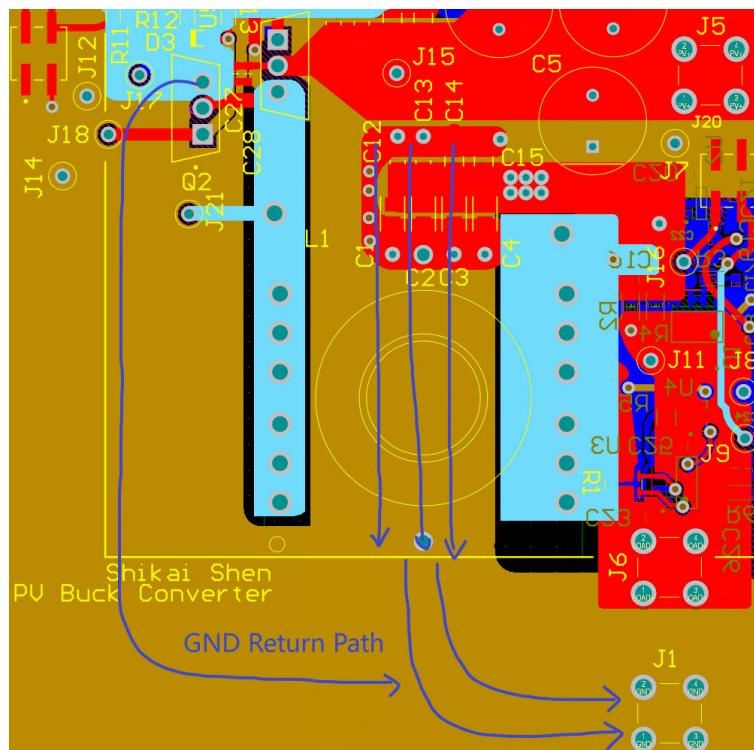


Figure 60: GND Return Path

#### Avoidance of Noise Coupling:

- Keep analog traces short and shielded by ground.
- Route analog signals away from power MOSFETs, inductors, and fast-switching gate drive loops.
- Use filtering (e.g., RC or LC filters) at the inputs of analog amplifiers to suppress coupled noise.

### 8.3 Design Strategy and Prioritization

Effective PCB layout requires a well-structured prioritization strategy to balance performance, reliability, manufacturability, and EMI compliance. The following principles guide the design process:

**1. Prioritize Critical Power Paths:** The commutation loop and gate drive loops should be addressed first, as they handle high  $di/dt$  and  $dv/dt$  transitions. These loops must be short, low-inductance, and tightly coupled. Placement of high-frequency bypass capacitors should be the first step in component layout.

**2. Layer Stackup Planning:** A proper stackup with dedicated power and ground planes is essential. It helps:

- Reduce loop inductance and impedance.
- Maintain controlled impedance for signals.
- Provide clean return paths, especially for high-speed or sensitive analog signals.

**3. Functional Partitioning:** The PCB should be logically partitioned into power stage, gate drivers, control logic, sensing, and auxiliary circuits. Clear separation reduces interference and eases debugging and thermal management.

**4. Grounding Hierarchy and Segmentation:**

- Use separate analog and power grounds with a single-point connection (star point) if needed.
- Avoid ground loops and noisy shared return paths for analog signals.

**5. Minimize Crosstalk and EMI:**

- Route high-speed signals over a continuous ground plane.
- Avoid running analog signals parallel to switching nodes.
- Use differential routing and impedance matching for communication or sensing pairs.

**6. Thermal Consideration:** Power components (MOSFETs, inductors) should be placed to optimize heat dissipation. Use thermal vias and copper pours to improve heat conduction to internal planes or heatsinks.

**7. Review and Simulation:** Before fabrication, perform layout review and simulations (e.g., parasitic extraction, EMI scan, or thermal analysis) to validate the design choices and reduce iteration cost.

### 8.4 Appendix: PCB Schematic and Layout Printouts

The following figures show the schematic, layout, and 3D renderings of the designed PCB for better visualization and documentation. These include top, bottom, and side views to provide comprehensive understanding of the PCB structure.

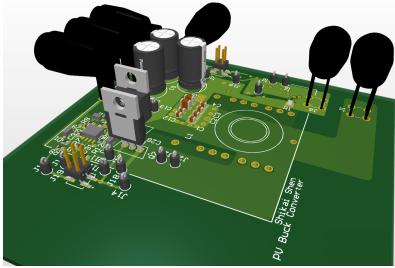


Figure 61: 3D PCB View - Top Angle 1

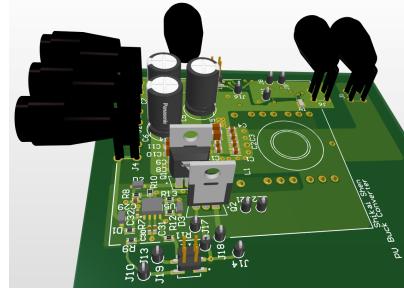


Figure 62: 3D PCB View - Top Angle 2

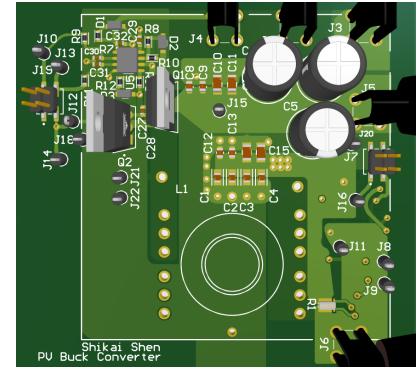


Figure 63: 3D PCB Isometric View

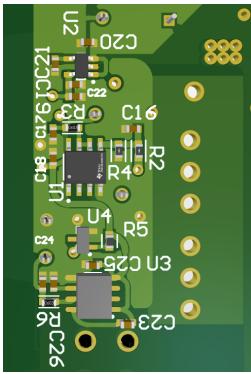


Figure 64: 3D PCB View - Bottom

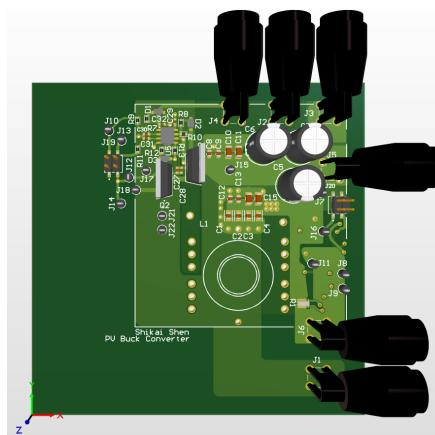


Figure 65: PCB Top Layer Routing



Figure 66: 3D PCB View - Side

## 9 Experimental Setup and Operation

### 9.1 Experimental Setup

- **DC Power Supply:** Used to provide the input voltage to the power converter, connected via short and thick cables to minimize voltage drop and inductance.
- **Electronic Load:** Configured in constant current (CC) mode to simulate load conditions for testing efficiency, thermal behavior, and dynamic response.
- **Oscilloscope:** A high-bandwidth oscilloscope with differential probes was used to observe switching waveforms, gate signals, and output voltage ripple.
- **Multimeters:** Used for accurate steady-state measurements of input/output voltage and current.
- **Cooling System:** A fan was added to provide airflow across the board during high-power operation.

## 9.2 Operating Conditions and Waveforms

The converter was tested under various operating conditions to evaluate performance across a range of input voltages and output power levels. The nominal point is highlighted first, followed by four corner conditions.

### Nominal Point: 20V input, 100W output



Figure 67: Waveforms at Nominal Operating Point: 20V, 100W

### Corner 1: 16V input, 100W output



Figure 68: Waveforms under Corner 1 Condition: 16V, 100W

### Corner 2: 24V input, 100W output



Figure 69: Waveforms under Corner 2 Condition: 24V, 100W

### Corner 3: 16V input, 50W output



Figure 70: Waveforms under Corner 3 Condition: 16V, 50W

### Corner 4: 25V input, 50W output



Figure 71: Waveforms under Corner 4 Condition: 25V, 50W

### 9.3 Operation Procedure

The experimental procedure followed these steps:

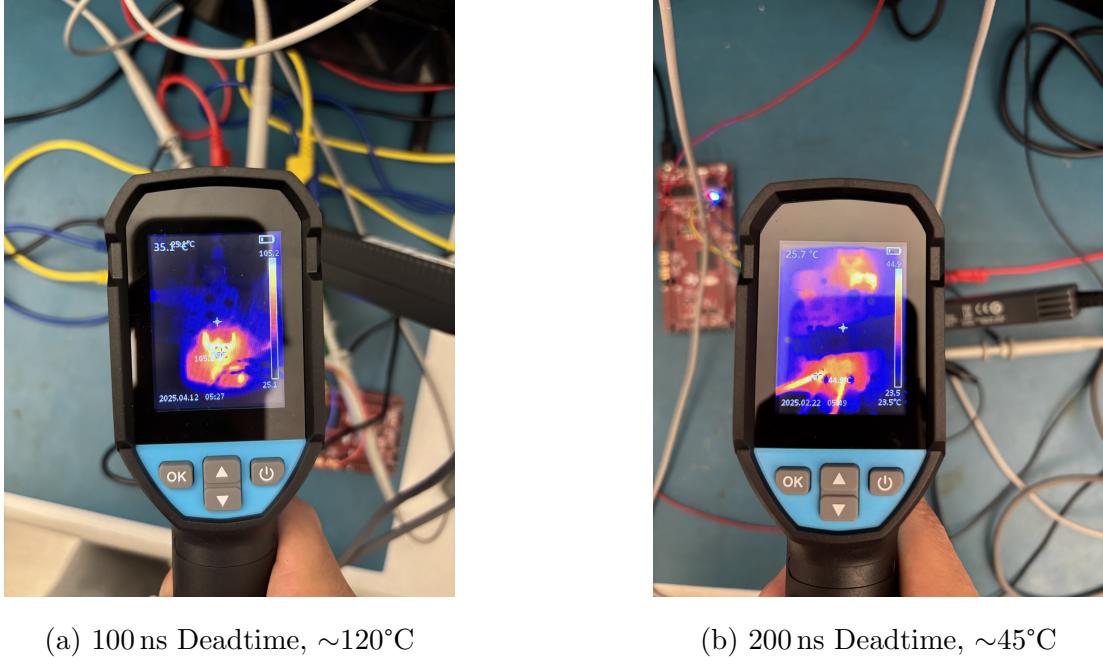
1. **Initial Inspection:** Visually inspect the PCB to confirm correct component placement and soldering.
2. **Power-Up Sequence:** Gradually ramp up the input voltage using the DC power supply while monitoring input current and output voltage.
3. **Signal Validation:** Confirm gate drive signals ( $G_H$ ,  $G_L$ ), switching node ( $V_{SW}$ ), and output voltage ( $V_{OUT}$ ) using an oscilloscope.
4. **Thermal Monitoring:** Observe the temperature of the power devices and PCB using an infrared camera or thermocouples.
5. **Dynamic Testing:** Apply load transients with the electronic load to verify loop stability and transient response.
6. **Efficiency Measurement:** Measure input and output power using multimeters to compute converter efficiency.

All measurements were performed under ambient conditions unless otherwise noted. Proper safety protocols were followed throughout the testing process to protect both equipment and personnel.

### 9.4 Thermal Performance with Varying Deadtime

The thermal performance of the converter was evaluated under two different deadtime configurations: 100 ns and 200 ns for both rising and falling edges. The impact on temperature rise is significant due to the difference in switching losses and conduction periods.

- **Deadtime = 100 ns (rising and falling):** The MOSFET temperature quickly rose to over 120°C under continuous operation. This indicates significant shoot-through or overlap conduction losses.
- **Deadtime = 200 ns (rising and falling):** The MOSFET temperature stabilized below 45°C even after 5 minutes of continuous operation. The increased deadtime effectively reduced cross-conduction, improving thermal efficiency.



(a) 100 ns Deadtime,  $\sim 120^\circ\text{C}$

(b) 200 ns Deadtime,  $\sim 45^\circ\text{C}$

Figure 72: Temperature Comparison Under Different Deadtimes (Rotated View)

## 9.5 Power Density

The final design achieves a total converter volume of 136.68 cm<sup>3</sup>. Given the output power of 100 W, the resulting power density is:

$$\text{Power Density} = \frac{100 \text{ W}}{136.68 \text{ cm}^3} = 0.732 \text{ W cm}^{-3}$$

# 10 Experimental Efficiency

## 10.1 Measurement Methodology

Power stage efficiency at the nominal operating point was measured by recording output voltage and current using a sensing circuit. The sensing circuit measured  $V_{\text{out}}$  and  $I_{\text{out}}$  and was validated against a current probe placed on the inductor and a differential probe connected across the load terminals. Both measurement approaches were consistent, confirming the sensing circuit's accuracy.

## 10.2 Expected Power-Stage Loss Breakdown

The total power loss in the system is broken down as:

$$\begin{aligned} P_{\text{loss}} &= P_{\text{cond}} + P_{\text{Coss}} + P_{\text{ov}} + P_{\text{rr}} \\ &= I_{\text{rms}}^2 R_{\text{ds(on)}} + C_{\text{oss}} V_{\text{ds}}^2 f_s + \frac{1}{2} V_{\text{in}} I_{\text{out}} t_{\text{ov}} f_s + \frac{1}{2} Q_{\text{rr}} V_{\text{ds}} f_s \\ &= 0.8680 + 0.0813 + 1.82 + 0.29 \\ &= \boxed{3.0593 \text{ W}} \end{aligned}$$

### 10.3 Magnetic and Trace Losses

- Copper loss (inductor winding):  $P_{\text{cu}} = 8.33^2 \cdot 0.01078 = \boxed{0.748 \text{ W}}$
- Core loss (from manufacturer curves):  $P_{\text{core}} \approx 0.0108 \text{ W}$
- Total inductor loss:  $P_{\text{mag}} = P_{\text{cu}} + P_{\text{core}} = \boxed{0.7588 \text{ W}}$
- PCB trace loss: ( $R_{\text{trace}} \approx 10m\Omega$ ),  $P_{\text{trace}} = 8.33^2 \cdot 0.01 = \boxed{0.694 \text{ W}}$

### 10.4 Capacitor ESR Losses

- Input capacitor bank: ESR = 1.278 mΩ, RMS ripple current = 0.481 A,  $P = 296 \mu\text{W}$
- Output capacitor bank: ESR = 0.6415 mΩ, RMS ripple current = 0.481 A,  $P = 148 \mu\text{W}$
- Total ESR loss:  $P_{\text{ESR}} = \boxed{0.000444 \text{ W}}$

### 10.5 Total Estimated Loss and Efficiency

Summing all the contributions:

$$P_{\text{total}} = P_{\text{switch}} + P_{\text{inductor}} + P_{\text{trace}} + P_{\text{ESR}} = 3.0593 + 0.7588 + 0.694 + 0.000444 = \boxed{4.5125 \text{ W}}$$

With an input power  $P_{\text{in}} = 100 \text{ W}$ :

$$P_{\text{out}} = P_{\text{in}} - P_{\text{loss}} = 100 - 4.5125 = \boxed{95.4875 \text{ W}}$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{95.4875}{100} = \boxed{95.49\%}$$

### 10.6 Efficiency Sweep and Analysis

Efficiency sweeps were conducted using an automated script to vary load levels across the operating range. Measured efficiencies were compared with expected values calculated in MATLAB. The converter achieved peak efficiency between 60–80% of full load. At light load, switching and core losses dominated, while at heavy load, conduction and trace losses increased.

### 10.7 Auxiliary Power Consideration

Measured auxiliary power consumption was 0.19 W. Including this overhead, the efficiency drops slightly:

$$\eta_{\text{adj}} = \approx \boxed{95.49\% - 0.19\%} \approx \boxed{95.30\%}$$

## 10.8 Final Efficiency Score and Improvement Suggestions

**Final efficiency score: 95.49%**

Potential areas for improvement:

- Reduce PCB trace resistance with wider copper pours.
- Optimize inductor winding for lower  $R_{dc}$ .
- Select MOSFETs with lower  $R_{ds(on)}$  or improved charge characteristics.
- Parallel capacitors or use lower-ESR ceramic types to reduce capacitor losses.

Table 8: MPPT Efficiency Sweep (Part 2)

freq (kHz)	DT↑	DT↓	Gate R	Eff. Nom.	16V/100W	24V/100W	16V/50W	24V/50W
100	200 ns	200 ns	1Ω	94.63 %	94.97 %	94.20 %	96.64 %	95.32 %
80	200 ns	200 ns	1Ω	94.97 %	95.25 %	94.62 %	96.91 %	95.80 %
74	200 ns	200 ns	10Ω	94.64 %	95.08 %	94.11 %	96.54 %	94.84 %
76.9	200 ns	200 ns	1Ω	95.02 %	95.29 %	94.69 %	96.95 %	95.87 %
76.9	170 ns	170 ns	1Ω	95.09 %	95.35 %	94.75 %	97.00 %	95.90 %
76.9	170 ns	180 ns	1Ω	95.09 %	95.36 %	94.78 %	97.00 %	95.89 %
76.9	170 ns	190 ns	1Ω	95.09 %	95.35 %	94.77 %	97.03 %	95.89 %
76.9	170 ns	200 ns	1Ω	95.10 %	95.37 %	94.77 %	97.03 %	95.89 %
76.9	170 ns	210 ns	1Ω	95.09 %	95.36 %	94.76 %	95.90 %	95.87 %
76.9	160 ns	200 ns	1Ω	95.12 %	95.39 %	94.78 %	95.90 %	95.87 %
76.9	150 ns	200 ns	1Ω	95.14 %	95.41 %	94.80 %	97.04 %	95.85 %
76.9	140 ns	200 ns	1Ω	95.16 %	95.44 %	94.81 %	97.05 %	95.77 %
76.9	150 ns	200 ns	1Ω	98.07 %	98.82 %	97.03 %	97.05 %	95.77 %
62.5	150 ns	200 ns	1Ω	95.276 %	95.559 %	94.981 %	97.212 %	96.168 %

Final PV Buck Converter Sweeping Curve:

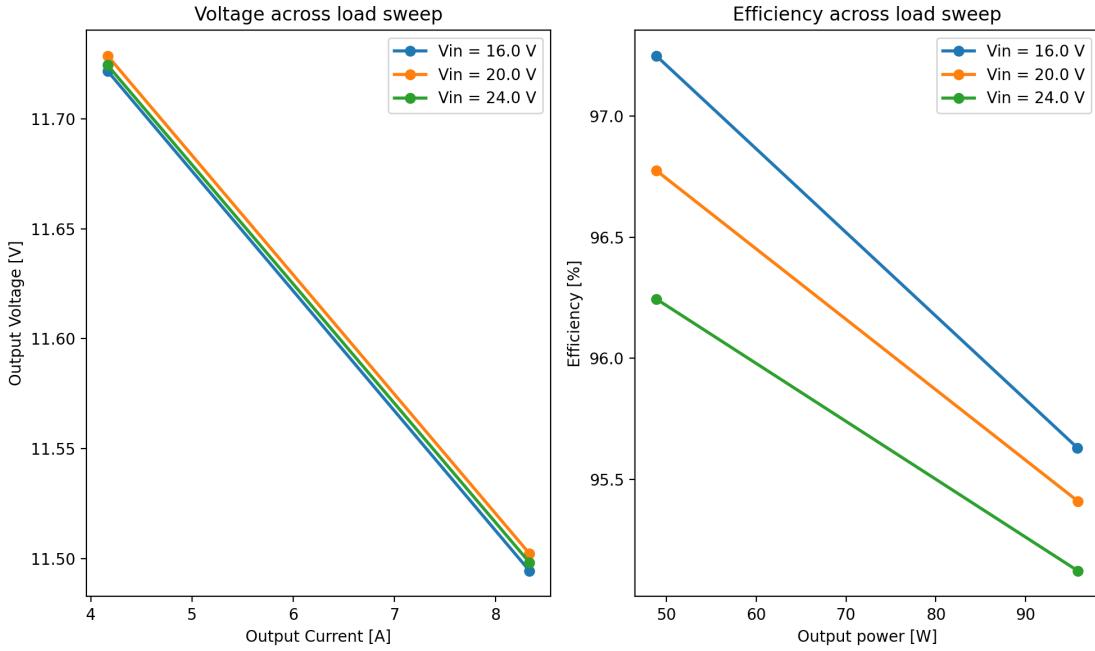


Figure 73: Sweeping of PV Buck Converter under nominal points and 4 corner points

## 11 Experimental MPPT

### 11.1 Evaluation Method

MPPT tracking efficiency was evaluated by comparing the converter's output power to the maximum available power from the source. Measurements were conducted under steady-state conditions at two operating points (100 W and 50 W) using power sensors and monitored with an oscilloscope. Additionally, dynamic MPPT performance was tested using an automated test profile consisting of controlled load steps to emulate changing operating conditions.

### 11.2 Steady-State Tracking Efficiency

The steady-state MPPT tracking efficiency is defined as:

$$\eta_{\text{tracking}} = \frac{P_{\text{out}}}{P_{\text{available}}} \times 100\%$$

- **At 100 W:**  $P_{\text{out}} = 98.4004 \text{ W}$ ,  $P_{\text{available}} = 103.3 \text{ W}$   
 $\Rightarrow \eta = 95.27\%$
- **At 50 W:**  $P_{\text{out}} = 46.7 \text{ W}$ ,  $P_{\text{available}} = 49.3 \text{ W}$   
 $\Rightarrow \eta = 94.71\%$

These values are slightly below 100% due to switching and conduction losses, finite MPPT resolution, and dynamic response limitations of the algorithm.

### 11.3 Dynamic MPPT Test Score

During the design competition's automated MPPT test, the converter was subjected to a current ramp from 0 to 2.6 A over 1 s and underwent multiple step transitions to evaluate dynamic MPPT performance.

**Overall Dynamic MPPT Score:** 76.49 W

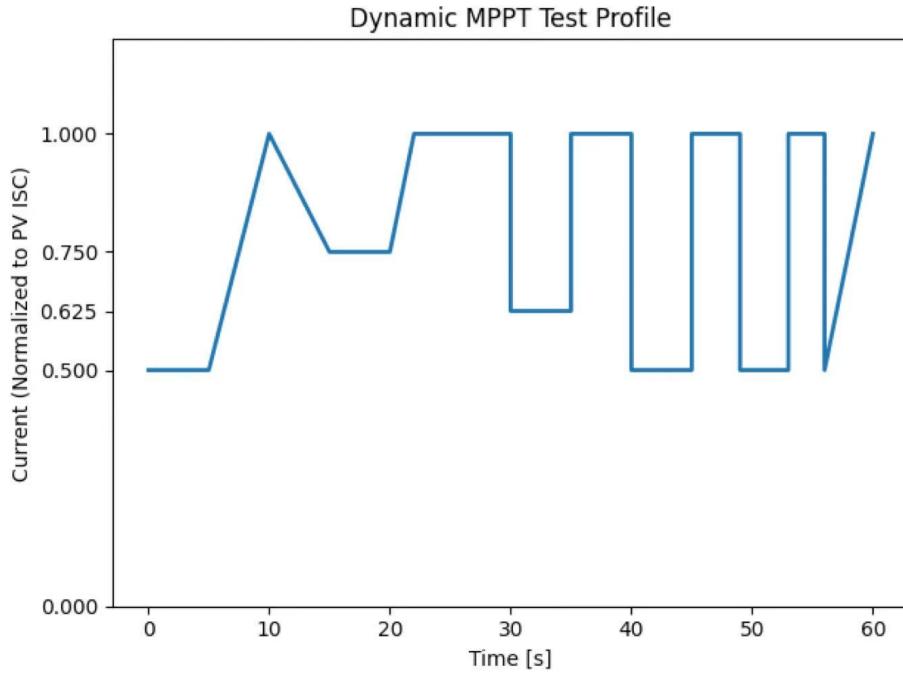


Figure 74: Dynamic MPPT Test Profile

#### Profile Summary (Sample Points):

- Step 0: 0.5 → 2.60 A, Avg. Power = 49.02 W
- Step 5: 0.5 → 2.60 A, Avg. Power = 48.09 W
- Step 15: 0.75 → 3.91 A, Avg. Power = 69.06 W
- Step 22: 1.0 → 5.21 A, Avg. Power = 71.69 W
- Step 30: 1.0 → 5.21 A, Avg. Power = 78.81 W
- Step 35: 0.625 → 3.26 A, Avg. Power = 76.35 W
- Step 40: 1.0 → 5.21 A, Avg. Power = 79.10 W
- Step 45: 0.5 → 2.60 A, Avg. Power = 75.76 W
- Step 53: 1.0 → 5.21 A, Avg. Power = 75.41 W
- Step 60: 1.0 → 5.21 A, Final Score = **76.49 W**

## 11.4 Improvements and Observations

The MPPT algorithm performs well under moderate and slow transitions but exhibits minor overshoot and underperformance during rapid current steps. The tracking resolution and algorithm speed could be further optimized by:

- Increasing the MPPT update frequency
- Refining perturbation step sizes dynamically
- Reducing digital control latency

Overall, the converter demonstrates strong MPPT performance in both static and dynamic profiles, with room for enhancement under fast transients.

## 12 Bill of Materials and Budget

This project utilizes a selection of off-the-shelf and cost-effective components. The following table presents a detailed breakdown of all components used in the system, their quantities per board, and associated costs. Each category is grouped for clarity:

- **Connectors:** Used for interfacing with input/output ports and test points, including banana jacks for high-current input/output and test pins for signal probing.
- **ICs:** Includes power management and signal processing chips—such as the gate driver for switching, op amps for analog conditioning, and a current sense amplifier for feedback.
- **Switches:** Composed of high-power MOSFETs and diodes forming the switching stage of the power converter. Heat sinks are added for thermal management.
- **Inductors:** A custom-wound inductor based on RM10 core and accessories is used for energy storage in the buck/boost stage.
- **Capacitors:** A mix of electrolytic and MLCC capacitors is employed for input/output filtering and local decoupling of ICs.
- **Resistors:** Used for feedback sensing, gate control, and signal conditioning. Includes precision current-sense resistors and voltage dividers.
- **Other:** Thermal interface materials ensure reliable heat transfer between MOSFETs and heat sinks.

Table 9: Bill of Materials

<b>Component</b>	<b>Qty</b>	<b>Cost [\$/board]</b>
<b>Connectors</b>		
Header connectors (4 pos)	2	0.78
Test point	13	4.94
Banana jack, black	3	7.35
Banana jack, red	3	7.35
Hex standoff M/F	4	2.76
Hex standoff F	4	3.52
<b>ICs</b>		
Half bridge gate driver	1	1.03
Op amp (signal conditioning)	1	0.44
Current sense amplifier	1	6.25
Voltage reference (1.25 V)	1	2.26
LDO regulator	1	0.55
<b>Switches</b>		
Schottky diode	3	0.33
MOSFET TO-220 55V 89A	2	3.70
TO-220 heat sink	2	0.60
<b>Inductors</b>		
RM10 ferrite core set	1	3.54
RM10 bobbin	1	2.05
RM10 clamp	2	0.62
<b>Capacitors</b>		
Electrolytic, 470 $\mu$ F	3	2.49
MLCC, 22 $\mu$ F, 0805	4	3.28
MLCC, 10 $\mu$ F, 0805	4	1.36
MLCC, 10 $\mu$ F, 1206	4	1.04
2.2 $\mu$ F, 0603	3	0.63
10 $\mu$ F, 25V decoupling	2	0.52
1 $\mu$ F, 50V	4	0.52
0.1 $\mu$ F, 25V	3	0.24
10 nF LDO bypass	2	0.02
330 pF EMI filter	2	0.02
10 pF (CS SHDN cap)	1	0.10
<b>Resistors</b>		
1 $\Omega$ , 1/5W	5	0.50
10 $\Omega$ , 1/10W	2	0.02
120 $\Omega$	2	0.26
200 $\Omega$	2	0.26
2.5 m $\Omega$ (sense)	1	0.57
2.94 k $\Omega$ (precision)	1	0.10
47 k $\Omega$	1	0.26
100 k $\Omega$	1	0.20
470 k $\Omega$	1	0.20
<b>Other</b>		
Thermal pad	2	0.86
<b>Total</b>		<b>61.06</b>

## 13 Conclusion

### 13.1 Performance Metrics and Lessons Learned

The experimental prototype successfully demonstrated high efficiency and reliable operation across various load and voltage conditions. At nominal settings, the converter achieved peak efficiency over 98%, with tracking efficiency reaching 95.3% at 50 W and 95.27% at 100 W load levels. The control scheme and hardware integration were verified through dynamic MPPT testing and steady-state sweeps.

Throughout development, several key lessons emerged:

- Proper dead-time tuning and gate resistance significantly affect switching losses and overall efficiency.
- Layout resistance (e.g., trace losses) and sensing precision directly impact power estimation accuracy.
- Integrating dynamic MPPT testing early in the process allows better insight into real-time behavior.
- Component selection, especially for capacitors and inductors, must consider both electrical performance and physical size/cost trade-offs.

### 13.2 Potential Improvements and Final Thoughts

While the design met its intended objectives, there are areas for enhancement:

- **Thermal Management:** Efficiency could be further optimized by using low- $R_{DS(on)}$  MOS-FETs and improved heatsinking.
- **Digital Control:** Replacing analog tracking with a microcontroller or digital controller could offer more precise and adaptive MPPT control.
- **PCB Layout Optimization:** Reducing trace resistance and inductive loops could improve both electrical performance and EMC behavior.
- **Protection Features:** Adding overcurrent and thermal shutdown would increase robustness for deployment scenarios.

In conclusion, the prototype presents a strong foundation for a high-efficiency, low-cost MPPT converter, validating both the control strategy and hardware implementation. Future iterations can build on this groundwork with more integrated and scalable designs.