

EE 113B/213B: Power Electronics Design
Module 3: Passive Components

Objectives

By the end of this module, you should be able to...

- Select a magnetic material
- Design and construct a power inductor
- Compare and select filter capacitors
- Calculate expected losses for power passives
- Characterize power passives
- Simulate power passive nonidealities

Recommended reading: KPVS Sections 15.2, 15.4, 15.5, 18.1-18.3, 18.5, 20.1, 20.2, 20.6

Pre-lab Assignment

Last week's module focused on switch selection, so this week's module will focus on passive components. In this module, we will design and prototype inductor L of Fig. 1 and select capacitors C_{in} and C_{out} .

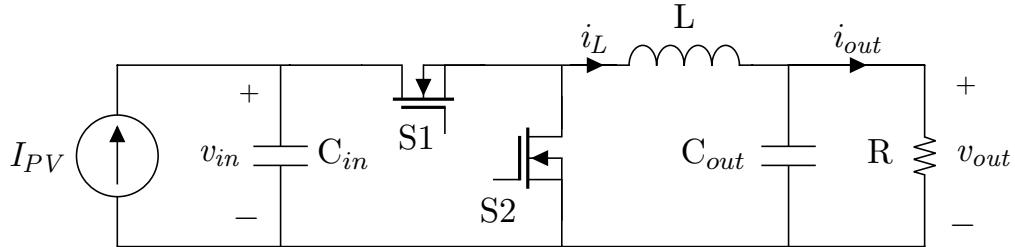


Figure 1: Synchronous buck converter.

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power Range	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq 5\%$
Output Voltage Ripple	$\leq 5\%$
Inductor Current Ripple (at 100W)	$\leq 20\%$

Magnetic Material Selection

Magnetic components serve a variety of different purposes in power electronics. One common example of these is the “filter inductor”, characterized by the ac component (i.e., ripple) of the current traveling through the inductor being small compared to its dc component (i.e., average value). In the buck converter of Fig. 1, L can be considered a filter inductor if i_L has small ripple. Design of filter inductors is often constrained by core saturation.

In Module 0, you sized L according to a maximum ripple allowance of 20% at full power, which meets the small ripple criterium for assuming L is a filter inductor. Now, you will design L beginning with its magnetic material. For this section, consider the iron powder and ferrite core material datasheets provided on bCourses.

1. Out of the available magnetic materials, select the best material for designing a filter inductor operating at 100 kHz and explain your reasoning.
2. Out of the available magnetic materials, select the best material for an ac transformer operating at 3 MHz and explain your reasoning.
3. Now, assume you must constrain your design to ferrite materials due to manufacturing limitations. Out of the available ferrite materials, select the best material for your design and explain your reasoning.
4. Provide the maximum allowable flux density B_{max} of your inductor, assuming you will design B_{max} to be 75% the material’s saturation flux density B_{sat} (to leave some margin).

Filter Inductor Design

Filter inductors are commonly designed using the K_g method, and ac magnetics are more effectively designed using the core area product (see KPVS Chapter 20 for more info). In the following steps, you will design your filter inductor L using the K_g method, assuming an RM core shape and the material you selected. You may assume the same converter specifications as the previous module, shown in Table 1. You may further assume a wire resistivity of $\rho = 2.09 \times 10^{-8} \Omega\text{-m}$ and a winding packing factor of $k_u = 0.4$. For selecting a wire size, you will need to refer to an American Wire Gauge (AWG) chart like [this one](#).

1. Calculate the peak inductor current $I_{L,max}$ for this design.
2. Assuming a maximum inductor power loss of 1 W, calculate the maximum dc winding resistance R .
3. Calculate the minimum core factor K_g for this filter inductor assuming the material you selected.
4. Select the smallest RM-type core that satisfies this K_g requirement.
5. Calculate the minimum number of turns required to avoid saturating this core. Note: this should be an integer.
6. Calculate the gap length necessary to provide inductance L that you sized in last week's module.
7. Determine whether or not Litz wire is necessary in your inductor design, or whether single-strand magnet wire would suffice. Since Litz wire has higher cost, you should only utilize it if you expect high-frequency losses to be significant in your design. If you determine that single-strand magnet wire would suffice, select a wire size (i.e., wire gauge) that will minimize conduction loss. If you determine that Litz wire is needed, select a Litz wire configuration (i.e., AWG of each strand and number of strands in parallel) that will minimize both conduction losses and high-frequency losses. Common practice for this is to choose a wire strand size (i.e., wire gauge for the Litz strands) with radius approximately equal or less than the skin depth, and then to parallelize as many of these strands as possible to minimize dc resistance.
8. Show that whatever wire configuration you choose will fit within the bobbin's window area, considering the assumed packing factor and number of turns.

Filter Inductor Losses

Now that you have designed your filter inductor, let's take a second look at its expected loss. The K_g method used to design this inductor assumed (a) a maximum copper loss allowance according to thermal constraints, and (b) that core loss could be ignored since the ac component of i_L is small compared to its dc component. You will verify both of these assumptions in this section.

1. Calculate the actual dc resistance of your filter inductor's winding. How does it compare to the intended value you used to design the inductor?
2. Using the actual dc resistance, calculate your filter inductor's expected copper loss at the nominal operating point and all four corner operating points. You are encouraged to augment your design script for this.
3. Calculate your filter inductor's expected core loss at the nominal operating point. Comment on whether or not this is negligible compared to the copper loss, and whether or not the K_g method was an appropriate design strategy. If core loss is not negligible, also calculate it for all four corner operating points. If core loss is negligible, you may ignore it in subsequent calculations.
4. Calculate the maximum temperature rise for your filter inductor design, considering its maximum-loss operating point. Comment on whether or not this is acceptable according to material temperature limits.

Filter Capacitor Selection and Loss

There are several types of capacitors utilized in power circuits. In Module 0, you sized C_{in} and C_{out} according to a ripple specification. Such large dc filter capacitances are commonly realized with electrolytic capacitors, which offer very high capacitance per unit volume compared to other types. However, electrolytic capacitors tend to have higher series resistance and therefore low current ratings. Multilayer ceramic capacitors (MLCCs) offer low series resistance and inductance, which is particularly useful for high-frequency filtering (i.e., decoupling capacitors). Thus, use of electrolytic capacitors in parallel with ceramic capacitors often provides a fruitful combination of high density and low impedance.

In this section, you will evaluate electrolytic capacitors and MLCCs for realizing C_{in} and C_{out} . Note: Not all capacitor manufacturers provide plots for voltage dependence, temperature dependence, etc. For evaluating MLCCs without such plots in their datasheets, search for similar parts on TDK's or Murata's website (same voltage rating, capacitance, size, and temperature code). You may assume the provided plots for comparable parts are representative of your part. See an example TDK MLCC part [here](#).

1. Out of the electrolytic capacitors provided in our part library, select a capacitor and the number of them needed in parallel for realizing C_{in} . You should consider not only the voltage ratings of candidate parts but also their rms current ratings and ESR at the relevant frequency. On your board, there is space for up to three electrolytic capacitors for realizing C_{in} , though you should only use the number of spaces you actually need.
2. For realizing C_{in} , select a potential alternative capacitor arrangement based on Class II ceramic parts in the provided parts library. In addition to voltage ratings and frequency-dependent ESR of candidate parts, you should also consider how their capacitances derate with bias voltage. On your board, there is space for up to four Class II ceramic capacitors of package size 1206 or 0805 for realizing C_{in} , though you should only use the number of capacitors in parallel that you actually need. Comment on the size and efficiency tradeoffs between the electrolytic and ceramic configurations.
3. For realizing C_{in} , choose either the electrolytic capacitors, the ceramic capacitors, or a parallel configuration of both that provides a good combination of high density and low ESR. Provide part numbers for each, and how many of each are needed. Show that the resulting ripple is acceptable and that rms currents of all electrolytic capacitors are within their limits according to the datasheets. If you have multiple types of capacitors in parallel, you should either use impedance division to determine the rms current through each or assume all of the current goes through each type (as a very conservative estimate).
4. Similarly design a ceramic capacitor configuration for realizing C_{out} from the parts provided in our library. On your board, there is space for up to eight Class II ceramic capacitors of package size 1206 or 0805 for realizing C_{out} , though you should only use the number of capacitors in parallel that you actually need.
5. Calculate the expected conduction loss each for C_{in} and C_{out} . You should consider the rms current through each capacitance and the capacitance's total ESR at the relevant frequency. If you have multiple types of capacitors in parallel, you should use impedance division to determine the rms current through each.
6. Determine whether or not your expected capacitor losses are significant compared to your total expected converter losses. If so, consider adding additional capacitors in parallel to reduce ESR, but only as many as you actually need to reduce your capacitor losses to the point of being negligible compared to your whole converter's loss. If not, consider reducing the number of capacitors in parallel in order to reduce the necessary size and cost, ensuring your designs still meet ripple and rms current requirements. The decision of how many capacitors to use in parallel often involves this tradeoff.

Assignment Feedback (Required)

How much dedicated time did you spend on this pre-lab?

Lab Assignment

3C95

Pre-Lab Check-off: Before you begin the lab assignment, confirm with the instructor that your inductor design is appropriate for your converter design. Provide the core size, number of turns, wire size, and gap length.

Build Your Inductor

RM10,12,... N \geq 10 Gauge 26 0.4049 mm. g \leq 0.3023 mm.

Now that you have designed your inductor, it's time to build it! Obtain the core size you selected for your inductor, its corresponding bobbin, and a strand of the wire size you selected. The inductor cores are fragile, so use care when handling. Then, assemble the inductor in the following steps:

1. Wrap the magnet wire around the bobbin up to the number of turns you selected for your inductor.
2. Select a shim stock thickness to serve as a spacer for your inductor's designed air gap. You should anticipate half of this air gap being in the center post and half being on the outer posts, so that the pieces of ferrite are equally spaced from each other in all three places. **Be sure to convert this thickness to mils to match the units of the shim stock in our parts library.** Cut pieces of shim stock for each of the three spacing locations, with each piece being about the size of the cross-sectional core.
3. Insert the two ferrite core pieces into the bobbin. Where the core pieces meet, insert the appropriate piece of shim stock, creating your designed air gap.
4. With the shim stock in place, clamp the two ferrite pieces together to hold them in place.
5. Cut the magnet wire sticking out of the inductor to a length that is appropriate for how the inductor will be mounted on your board (not too short!). Then, with a soldering iron, burn the insulation off of the magnet wire ends.

I_L, $\frac{d}{2} \rightarrow$ small nipple. neglect

For capacitor, $\int i(t)dt = 0$.  ripples \downarrow AC

LCR Meter

For the inductor, I_L is DC value \rightarrow only consider dc L value

Now that you have built your inductor, characterize it using an LCR meter as follows:

36uF real

1. Measure your inductor's inductance at low frequency, and compare it to your design value. If your inductance measurement is significantly off, double check your inductance calculation and your shim stock thickness. The acceptable range for your characterized inductance is 100-110% the minimum value needed to meet the ripple specifications.
2. Measure your inductor's equivalent series resistance (ESR), and compare it to your design value.
3. Measure your inductor's inductance and ESR at 100 kHz, and compare these values to your low-frequency measurements.

Obtain one electrolytic capacitor part you selected, and characterize it using an LCR meter as follows:

1. Measure the capacitor's capacitance at low frequency, and compare it to its datasheet value.
2. Measure the capacitor's ESR at low frequency, and compare it to its datasheet value.
3. Measure the capacitor's capacitance and ESR at 100 kHz, and compare these values to the low-frequency measurements.

Check-off: (a) For your inductor, show that your low-frequency inductance and ESR measurements are close to their designed values. Discuss any variation between these low-frequency measurements and your measurements at 100 kHz, and discuss which measurement is more appropriate for modeling your inductor. (b) For your capacitor selections, show that your capacitance and ESR measurements are close to their anticipated values. Discuss any variation between these low-frequency measurements and your measurements at 100 kHz, and discuss which measurement is more appropriate for modeling your input and output capacitors.

Expected Loss

Now that you have characterized your passive components, calculate their expected losses for the nominal operating point and each corner operating point. For your inductor and electrolytic capacitor, you should use ESR measurements at an appropriate frequency for each. For MLCC capacitors, you should determine the appropriate ESR using manufacturer-provided plots. Re-calculate the expected converter efficiencies for each of these operating points, considering loss in both the switches and the passive components.

Simulation Considering Passive Component Loss

During Module 1, you simulated your buck converter considering only switch parasitics. Now, update the inductance and capacitances to their characterized values (i.e., your characterized inductance and capacitance for the inductor and the electrolytic capacitor, respectively, and the manufacturer-provided capacitance of any MLCCs considering derating). Then, add parasitics (i.e., ESR) to each component as characterized at the appropriate frequency. Note: If you use several identical capacitors in parallel, you may combine their impedances in parallel (considering each to be an R-C branch) to form a single R-C branch.

Simulate your converter with both switch and passive component nonidealities, and determine the following for the nominal operating point and each corner operating point:

1. The efficiency of your power converter. Compare this to the efficiency you measured in Module 1 considering only switch parasitics.
2. The power loss incurred by each of the passives, estimated via simulation. Compare this to the expected loss you calculated in the previous section.
3. The maximum ripples on i_L , v_{in} , and v_{out} .
4. The rms current through any electrolytic capacitors.

Check-off: Confirm correct (a) component models, and which frequency's measurements to use for model parameters, (b) simulated efficiency, (c) expected loss and simulated loss for each component, (d) that the actual components satisfy ripple requirements, and (e) that all electrolytic capacitors adhere to rms current requirements. Tell us (f) how much dedicated time you spent on this lab, and (g) if any other student(s) in the lab helped you, and who.

Post-lab Assignment

Lab Results

1. Provide your characterized inductance and ESR values for your inductor at each test frequency.
2. Provide your characterized capacitance and ESR values for your electrolytic capacitor at each test frequency.
3. Provide your simulation-based loss estimates for your passive components, and discuss how they compare with your calculations. Discuss any discrepancies.

Lab Takeaways

1. In your own words, describe how to choose a magnetic material.
2. In your own words, describe the design process for a filter inductor (given a magnetic material).
3. In your own words, describe how to select electrolytic capacitors.
4. In your own words, describe how to select multilayer ceramic capacitors.
5. In your own words, describe why frequency matters when characterizing a passive component, and how a designer should choose which frequency to use.

Build Intuition

1. Describe how to determine whether or not core loss may be considered negligible when designing a magnetic component. If your inductor had been sized such that your buck converter operated in DCM, would the expected core loss be greater or less than the value you calculated in the pre-lab? If you were designing an ac transformer (i.e., a transformer intended to handle primarily ac waveform content), could you have neglected core loss?
2. The K_g method, while very useful, has its limitations. Describe at least one aspect of magnetics design that the K_g method neglects, and how you should design magnetic components if that aspect is relevant to your design.
3. Describe when electrolytic capacitors are more useful than multilayer ceramic capacitors, and the same vice versa. When should a designer choose one over the other?
4. Assuming a capacitor also has ESR and ESL (equivalent series inductance), which characteristic between its capacitance, inductance, and resistance do you expect to be dominant at extremely high frequencies? Why?

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Design the magnetic component(s) and select the capacitor(s) for your chosen converter topology. Provide justification for whether or not core loss should be considered when designing your magnetic components. For filter inductors, you may use the procedure outlined in the pre-lab (i.e., the K_g method). For transformers and ac inductors, you should use the procedure outlined in Section 20.6 of KPVS and justify your assumptions.

If you would like to propose an additional part for our library, please follow the procedure outlined at the end of Module 2.

Assignment Feedback (Required)

How much dedicated time did you spend on this post-lab?

Last week's module focused on switch selection, so this week's module will focus on passive components. In this module, we will design and prototype inductor L of Fig. 1 and select capacitors C_{in} and C_{out} .

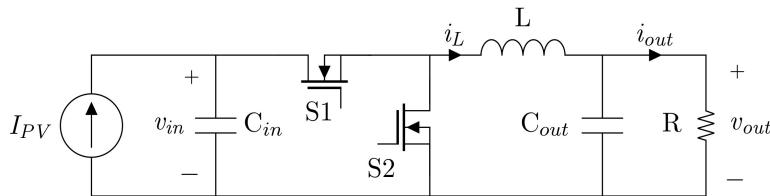


Figure 1: Synchronous buck converter.

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power Range	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq 5\%$
Output Voltage Ripple	$\leq 5\%$
Inductor Current Ripple (at 100W)	$\leq 20\%$

In Module 0, you sized L according to a maximum ripple allowance of 20% at full power, which meets the small ripple criterium for assuming L is a filter inductor. Now, you will design L beginning with its magnetic material. For this section, consider the iron powder and ferrite core material datasheets provided on bCourses.

- Out of the available magnetic materials, select the best material for designing a filter inductor operating at 100 kHz and explain your reasoning.
- Out of the available magnetic materials, select the best material for an ac transformer operating at 3 MHz and explain your reasoning.
- Now, assume you must constrain your design to ferrite materials due to manufacturing limitations. Out of the available ferrite materials, select the best material for your design and explain your reasoning.
- Provide the maximum allowable flux density B_{max} of your inductor, assuming you will design B_{max} to be 75% the material's saturation flux density B_{sat} (to leave some margin).

- Ferrous Alloys:
- Steel (laminated alloys): 60 Hz, up to 20 kHz
 - Powdered Iron (toroid): up to 100 kHz

From lecture, we've learned that. For Ferrous Alloys [Fe]
high saturation flux density, $B_{sat} \uparrow$
but $P_{loss} \uparrow$

Magnetic Ceramics (ferrites):

- MnZn: up to 1 MHz
 - NiZn: up to 10 MHz
- + higher efficiency @ high frequency
- brittle
- lower saturation flux density

For Magnetic Ceramics, Ferrites, $P_{loss} \downarrow$ at high frequency
but lower $B_{sat} \downarrow$

(1). In 100kHz, quite low-frequency and within $\leq 100\text{kHz}$.
choose powdered iron. \rightarrow TBC next page

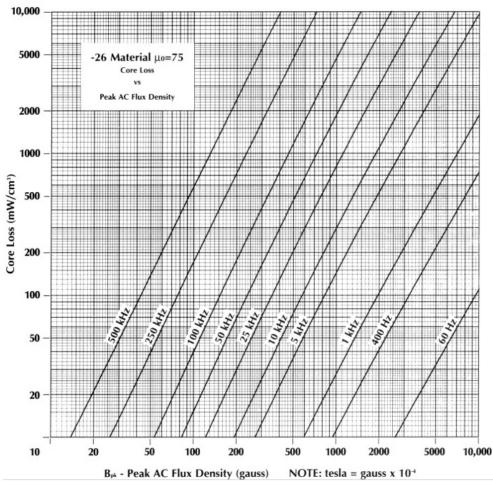
(2). In 3MHz, quite a high frequency, $\geq 1\text{MHz}$.
choose ferrite. \rightarrow TBC

(1) For DC-inductor, it's only constrained by B_{sat} to meet the requirement of $B_{sat} = \frac{M_i \cdot I_{sat}}{g}$.

$\Rightarrow B_{max} \leq 75\% B_{sat}$

Ferrous Alloys.

since I've been given only one material. I would choose -26 Material.



GENERAL MATERIAL PROPERTIES

Material Mix No.	Reference Permeability (μ_r)	Material Density (g/cm^3)	Relative Cost	Color Code
-2	10	5.0	2.7	Red/Clear
-8	35	6.5	5.0	Yellow/Red
-14	14	5.2	3.6	Black/Red
-26	75	6.6	3.4	Green/Red
-30	55	7.0	1.0	Yellow/White
-34*	22	6.0	1.4	Green/Gray
-35*	33	6.2	1.5	Gray/Blue
-38	85	6.3	1.4	Yellow/Gray
-40	60	7.1	1.1	Gray/Black
-45	100	6.9	1.0	Green/Yellow
-52	75	7.2	2.6	Black/Black
		7.0	1.2	Green/Blue

* The -30 Material was developed as a lower cost, lower loss alternate to the -26 Material. Similarly, the -34 & -35 Materials were developed to replace the -33 Material. The -28 & -33 Materials are not listed in this catalog but are still available.

(2) so to be specific, it's a AC-inductor and operates at 3MHz. **Ferrites**

DC magnetic design is only constrained by Ploss

\Rightarrow check Ploss of the magnetic material

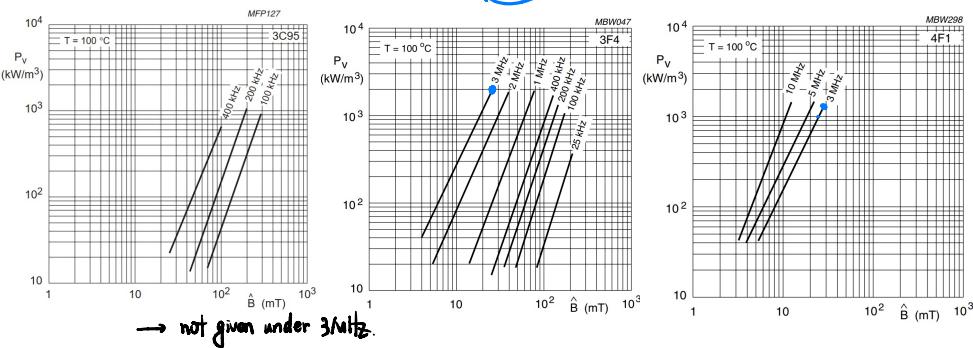


Fig.4 Specific power loss as a function of peak flux density with frequency as a parameter.

Given $P_V = k \cdot f^\alpha \cdot B_{AC}^\alpha$, $B_{AC} = \frac{1.5 \cdot I_{PP}}{N \cdot A_C}$. so we choose $P_V \min$ when $I \leq I_{sat}$.

\Rightarrow when $f = 3\text{MHz}$, 3F4 gets minimum I_{sat} and gets $P_V \min$

$I \leq I_{sat}$ satisfy

3. Now, assume you must constrain your design to ferrite materials due to manufacturing limitations. Out of the available ferrite materials, select the best material for your design and explain your reasoning.

4. Provide the maximum allowable flux density B_{max} of your inductor, assuming you will design B_{max} to be 75% the material's saturation flux density B_{sat} (to leave some margin).

Fe Alloy: $B_{sat} \uparrow$ $P_{loss} \uparrow$ at $f \uparrow$

Ferrite: $B_{sat} \downarrow$, $P_{loss} \downarrow$ at $f \uparrow$

(3) Ferrite materials: low-saturation, but low-loss
 $B_{sat} \downarrow$, $P_{loss} \downarrow$

For Ferrite materials in dc-inductor, we need to consider B_{sat} ← which is the constraint.

we should find $B_{sat max}$

$$\left. \begin{array}{l} 3T4: B_{sat} = 410 mT \\ 4F1: B_{sat} = 320 mT \\ 3C95: B_{sat} = 530 mT. \end{array} \right\} \quad \begin{array}{l} 3C95 \text{ should be better, with higher } B_{sat}. \\ I \text{ choose } 25^\circ C \text{ for default.} \end{array}$$

(4) $B_{max} = B_{sat} \times 75\% = 530 \times 75\% = 397.5 \text{ mT.}$

Lab 10: Inductor ESR↑, Winding↑

Filter Inductor Design

Filter inductors are commonly designed using the K_g method, and ac magnetics are more effectively designed using the core area product (see KPVS Chapter 20 for more info). In the following steps, you will design your filter inductor L using the K_g method, assuming an RM core shape and the material you selected. You may assume the same converter specifications as the previous module, shown in Table 1. You may further assume a wire resistivity of $\rho = 2.09 \times 10^{-8} \Omega \cdot \text{m}$ and a winding packing factor of $k_u = 0.4$. For selecting a wire size, you will need to refer to an American Wire Gauge (AWG) chart like this one.

1. Calculate the peak inductor current $I_{L,max}$ for this design.

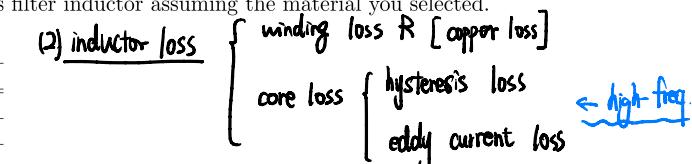
2. Assuming a maximum inductor power loss of 1 W, calculate the maximum dc winding resistance R .

3. Calculate the minimum core factor K_g for this filter inductor assuming the material you selected.

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power Range	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq 5\%$
Output Voltage Ripple	$\leq 5\%$
Inductor Current Ripple (at 100W)	$\leq 20\%$

(2) inductor loss



In low-freq., assume $P_{loss} \gg P_W$

$$I_{W,loss} \approx I_{RMS}^2 \cdot R_{ESR}$$

$$R_{ESR} \leq \frac{1}{9.67^2} \approx 0.012 \Omega$$

$$R_{winding, max} = 0.012 \Omega$$

$$(1) I_{L,max} = \frac{P_{max}}{V_{out}} = \frac{100W}{12V} = \frac{25}{3} A. \quad \left. \begin{array}{l} I_{L,max} = \frac{25}{3} \times (1+10\%) \\ = 9.167 A \end{array} \right\}$$

$$\Delta I_L = 20\% I_L$$

Here is the entire AWG chart in table format:

Gauge No. Diameter (Inches) Diameter (Millimeters)

7/0 0.651300 16.54

6/0 0.580049 14.73

5/0 0.516549 13.12

4/0 0.460000 11.68

3/0 0.409642 10.40

2/0 0.364797 9.266

1/0 0.324861 8.251

1 0.289297 7.348

2 0.257626 6.544

3 0.229423 5.827

4 0.204307 5.189

5 0.181941 4.621

6 0.162023 4.115

7 0.144285 3.665

8 0.128490 3.264

9 0.114424 2.906

10 0.101897 2.588

11 0.090742 2.305

12 0.080808 2.053

13 0.071962 1.828

14 0.064084 1.628

15 0.057068 1.450

16 0.050821 1.291

17 0.045257 1.150

18 0.040303 1.024

19 0.035891 0.9116

20 0.031961 0.8118

21 0.028462 0.7229

22 0.025347 0.6438

23 0.022572 0.5733

24 0.020101 0.5106

25 0.017900 0.4547

26 0.015941 0.4049

27 0.014196 0.3606

28 0.012641 0.3211

29 0.011258 0.2860

30 0.010025 0.2546

31 0.008928 0.2268

32 0.007950 0.2019

33 0.007080 0.1798

34 0.006305 0.1601

35 0.005615 0.1426

36 0.005000 0.1270

37 0.004453 0.1131

38 0.003965 0.1007

39 0.003531 0.08969

40 0.003145 0.07988

41 0.002800 0.07112

42 0.002494 0.06335

43 0.002221 0.05641

44 0.001978 0.05024

45 0.001761 0.04473

46 0.001568 0.03983

47 0.001397 0.03548

48 0.001244 0.03160

49 0.001108 0.02814

50 0.000986 0.02504

51 0.000878 0.02230

52 0.000782 0.01986

53 0.000697 0.01770

54 0.000620 0.01575

55 0.000552 0.01402

56 0.000492 0.01250

57 0.000438 0.01113

58 0.000390 0.00991

59 0.000347 0.00881

60 0.000309 0.00785

3. Calculate the minimum core factor K_g for this filter inductor assuming the material you selected.
4. Select the smallest RM-type core that satisfies this K_g requirement.
5. Calculate the minimum number of turns required to avoid saturating this core. Note: this should be an integer.

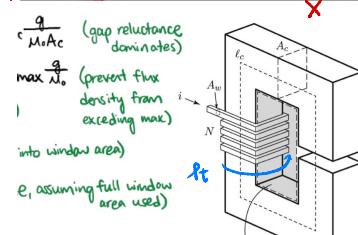
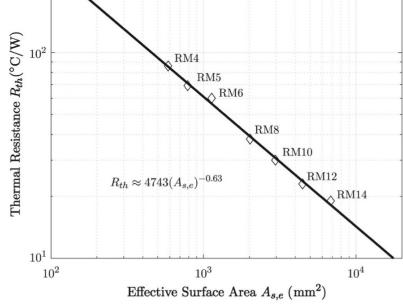
$$(3) \quad K_g = \frac{I^2 J_{max} \cdot P}{B_{max}^2 \cdot R_w \cdot k_u} \quad \leftarrow R_w = \frac{P}{S} . \quad \text{we know } P = 2.9 \times 10^{-8} \Omega \cdot \text{m}, \quad I_{max} = 9.67 \text{ A}.$$

$$B_{max} = 397.5 \text{ mT}, \quad R_w \text{ max} = 0.012 \Omega, \quad k_u = 0.4.$$

$$\Rightarrow \text{when } D = 0.5, \quad L \geq \frac{5(24-12) \times 0.5 \times 10^{-5} \times 12}{50} = 3.6 \times 10^{-5} \text{ H.}$$

(4) From reference book, $K_g = \frac{A_c^2 W_A}{l_t}$ such that RM10, 12, 14 ✓ \Rightarrow RM10

	RM4	RM5	RM6	RM8	RM10	RM12	RM14
Effective magnetic path length l_e (mm)	22.7	22.4	28.6	38.0	44.0	56.9	70.0
Effective core area $A_{c,e}$ (mm^2)	14.0	23.7	36.6	64.0	98.0	140	178
Minimum core area $A_{c,min}$ (mm^2)	10.7	17.3	30.2	53.5	86.6	121	165
Core window area W_A (mm^2)	15.6	18.2	26.0	48.9	69.5	110	155
Bobbin window area $W_{A,b}$ (mm^2)	7.7	9.5	15	30.0	41.5	73.0	107
Bobbin mean turn length l_t (mm)	20	25	30	42	52	61	71.5
Effective core volume $V_{c,e}$ (mm^3)	318	530	1050	2430	4310	7970	12500
Core set weight (g)	1.7	3.0	5.5	13	23	42	74
Effective surface area $A_{s,e}$ (mm^2)	586	787	1130	2020	2960	4460	6820
Thermal resistance R_{th} ($^\circ\text{C}/\text{W}$)	86	69	60	38	30	23	19
Core area product $A_{c,e} W_{A,b}$ (mm^4)	1.1×10^2	2.3×10^2	5.5×10^2	1.92×10^3	4.07×10^3	1.02×10^4	1.90×10^4
Core factor K_g	4.4×10^1	1.1×10^2	4.6×10^2	2.0×10^3	6.0×10^3	1.8×10^4	4.07×10^4



ρ : wire resistivity
 μ_0 : permeability of free space
 S : power capability
 B : flux density
 J : current density
 k_u : packing factor

$$\frac{I^2 J_{max} \cdot P}{B_{max}^2 \cdot R_w \cdot k_u} \leq \frac{A_c^2 W_A}{l_t} = K_g \quad (\text{m}^5)$$

design requirements
geometrical property of core

$$(5). \quad B_{max} = 397.5 \text{ mT}$$

$$B_{max} = \frac{1 \cdot I_{max}}{N \cdot A_c} \leq 397.5 \text{ mT}$$

$$N \geq \frac{1 \cdot I_{max}}{B_{max} \cdot A_c} = 9.5868$$

$$\Rightarrow N = 10$$

$A_c, min = 86.6$ mm²

Here is the entire AWG chart in table format:

Gauge No. Diameter (Inches) Diameter (Millimeters)

7/0 0.651300 16.54

6/0 0.580049 14.73

5/0 0.516549 13.12

4/0 0.460000 11.68

3/0 0.409642 10.40

2/0 0.364797 9.266

1/0 0.324861 8.251

1 0.289297 7.348

2 0.257626 6.544

3 0.229423 5.827

4 0.204307 5.189

5 0.181941 4.621

6 0.162023 4.115

7 0.144285 3.665

8 0.128490 3.264

9 0.114424 2.906

10 0.101897 2.588

11 0.090742 2.305

12 0.080808 2.053

13 0.071962 1.828

14 0.064084 1.628

15 0.057068 1.450

16 0.050821 1.291

17 0.045257 1.150

18 0.040303 1.024

19 0.035891 0.9116

20 0.031961 0.8118

21 0.028462 0.7229

22 0.025347 0.6438

23 0.022572 0.5733

24 0.020101 0.5106

25 0.017900 0.4547

26 0.015941 0.4049

27 0.014196 0.3606

28 0.012641 0.3211

29 0.011258 0.2860

30 0.010025 0.2546

31 0.008928 0.2268

32 0.007950 0.2019

33 0.007080 0.1798

34 0.006305 0.1601

35 0.005615 0.1426

36 0.005000 0.1270

37 0.004453 0.1131

38 0.003965 0.1007

39 0.003531 0.08969

40 0.003145 0.07988

41 0.002800 0.07112

42 0.002494 0.06335

43 0.002221 0.05641

44 0.001978 0.05024

45 0.001761 0.04473

46 0.001568 0.03983

47 0.001397 0.03548

48 0.001244 0.03160

49 0.001108 0.02814

50 0.000986 0.02504

51 0.000878 0.02230

52 0.000782 0.01986

53 0.000697 0.01770

54 0.000620 0.01575

55 0.000552 0.01402

56 0.000492 0.01250

57 0.000438 0.01113

58 0.000390 0.00991

59 0.000347 0.00881

60 0.000309 0.00785

6. Calculate the gap length necessary to provide inductance L that you sized in last week's module.
7. Determine whether or not Litz wire is necessary in your inductor design, or whether single-strand magnet wire would suffice. Since Litz wire has higher cost, you should only utilize it if you expect high-frequency losses to be significant in your design. If you determine that single-strand magnet wire would suffice, select a wire size (i.e., wire gauge) that will minimize conduction loss. If you determine that Litz wire is needed, select a Litz wire configuration (i.e., AWG of each strand and number of strands in parallel) that will minimize both conduction losses and high-frequency losses. Common practice for this is to choose a wire strand size (i.e., wire gauge for the Litz strands) with radius approximately equal or less than the skin depth, and then to parallelize as many of these strands as possible to minimize dc resistance.
8. Show that whatever wire configuration you choose will fit within the bobbin's window area, considering the assumed packing factor and number of turns.

6. L is mainly decided by g .

$$\Rightarrow L \approx \frac{N^2 \mu_0 A_c}{g} \Rightarrow g \approx \frac{N^2 \mu_0 A_c}{L}$$

suppose $L = 3.6 \times 10^{-5} H$

$N = 10$

$\mu_0 = 4\pi \times 10^{-7}$

$A_c = 86.6 mm^2$

$L \geq 3.6 \times 10^{-5} H$

$$\Rightarrow g \leq 3.023 \times 10^{-4} m = 0.3023 mm.$$

high-freq. loss

7. check for need for $\delta \leftarrow$ skin depth

$$f = \sqrt{\frac{\rho_{ac}}{\mu_0 f \cdot \mu_{air}}} \quad \text{copper is non-magnetic, } \mu_{air} = 4\pi \times 10^{-7} H/m$$
$$\rho_{ac} = 2.09 \times 10^{-8} \Omega \cdot m. \quad \Rightarrow \delta \approx 0.23 mm.$$
$$f = 100 kHz$$

* If single-strand wire have a large core loss

↓
Use Litz wire

For conduction loss = 1W, core loss: $P_v = k f^\alpha B_{ac}^\beta$ $P_{vmax} = k f^\alpha \cdot B_{max}^\beta$

For 3C95: $\alpha_f = 1.5 \pm 2 \times 10^{-6}$, $k, \beta \text{ const}$ $\Rightarrow P_v \text{ given,} = 350 kW/m^3$

$A_{ce} = 98 mm^2, l_c = 44 mm$

$$\Rightarrow P_{v, \text{given}} = 350 \times 10^3 \times (98 \times 44 \times 10^{-9}) = 1.5 W$$

compared to 1.67 W conduction loss, 1 W ESR of L . loss.

1.5 W is very large even under 100 kHz, account for 40% of total loss.

choose $r \ll \delta$

Use Gauge 25, $r = 0.2025 mm$, $\delta = 0.23 mm$.

600

8. *constraints: $N \cdot A_w \leq k_u \cdot W_A$

winding area window area bobbin window area $\leftarrow \frac{1}{12}$ wind up x

$$\Rightarrow N = 10, A_w = \pi r^2, k_u = 0.4, W_A = 41.55 \text{ mm}^2$$

$$N \cdot A_w = 1.288 \quad k_u \cdot W_A = 16.62$$

I can wind up at most 12 strands of Litz wire. using Gauge 26.

Filter Inductor Losses

Now that you have designed your filter inductor, let's take a second look at its expected loss. The K_g method used to design this inductor assumed (a) a maximum copper loss allowance according to thermal constraints, and (b) that core loss could be ignored since the ac component of i_L is small compared to its dc component. You will verify both of these assumptions in this section.

1. Calculate the actual dc resistance of your filter inductor's winding. How does it compare to the intended value you used to design the inductor?
2. Using the actual dc resistance, calculate your filter inductor's expected copper loss at the nominal operating point and all four corner operating points. You are encouraged to augment your design script for this.

Table 1: Buck Converter Design Specifications

(1). $R_{\text{W max}} = 0.012 \Omega$. From problem 2.

$$\text{Actual: } R_{\text{dc}} = \frac{P_L}{A_w} = \frac{P_{\text{dc}} \cdot N}{\pi r^2}$$

$$= \frac{209 \times 10^{-8} \times 52 \times 10^{-3} \times 10}{\pi \times (0.2025 \times 10^{-3})^2}$$

$$= 0.0844 \Omega$$

with 12 Litz winding:

$$\Rightarrow R_{\text{dc}} = \frac{0.0844}{12} = 0.007 \Omega \leq 0.012 \text{ max requirement}$$

(2). Inductor copper loss

$$P_{\text{Cu}} = I_L^2 R_{\text{dc}} \cdot R$$

① Nominal point:

$$I_L = \frac{100 \text{ W}}{20 \text{ V}} = 5 \text{ A}, P_{\text{Cu}} = 5^2 \times 0.007 = 0.175 \text{ W}$$

② Point = 100W ($V_{\text{in}} = 16, 24 \text{ V}$)

$$I_L = \frac{100}{12} = \frac{25}{3} \text{ A}, P_{\text{Cu}} = \left(\frac{25}{3}\right)^2 \times 0.007 = 0.4861 \text{ W}$$

③ Point = 50W ($V_{\text{in}} = 16, 24 \text{ V}$)

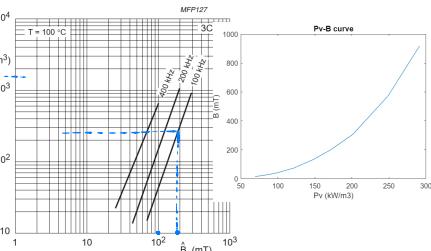
$$I_L = \frac{25}{6} \text{ A}, P_{\text{Cu}} = 0.1215 \text{ W}$$

3. Calculate your filter inductor's expected core loss at the nominal operating point. Comment on whether or not this is negligible compared to the copper loss, and whether or not the K_g method was an appropriate design strategy. If core loss is not negligible, also calculate it for all four corner operating points. If core loss is negligible, you may ignore it in subsequent calculations.

$$P_V = k_f^{\text{tot}} B_{\text{ac}}, B_{\text{ac}} = \frac{1}{N} \frac{2 \pi f_{\text{pp}}}{L} = \frac{1}{L} \cdot D \cdot T_s = \frac{1}{L} \cdot D \cdot 10^{-3}$$

$$B_{\text{ac}} = \frac{3.6 \times 10^{-5} \times \frac{1}{2} \times 133}{10 \times 98 \times 10^{-6}} = \frac{20 - 12}{36 \times 10^{-5}} \times 0.6 \times 10^{-5} = 133 \text{ A}$$

$$= 0.024 \text{ T} = 24 \text{ mT}$$



From MATLAB curve fitting:

\Rightarrow when $B=24\text{mT}$, $P_{v \rightarrow 0} < 10\text{kW/m}^3$, which is very small, so can be negligible.

Since it's negligible, I just calculate the worst case, when $(V_o - V_i)_{\max} \rightarrow \Delta i_{LPP \max}$

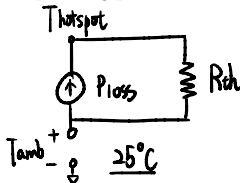
when $V_o = 12\text{V}$, $V_{in} = 24\text{V}$, $\Delta i_{LPP} = \left| \frac{V_o - V_i}{L} \cdot \Delta T_s \right| = 1.67\text{A}$

$\Rightarrow B_{ac} = 0.0306\text{T} = 30.6\text{mT}$.

\downarrow From MATLAB.
It's very small, $< 10\text{kW/m}^3$.
so negligible.

$\Rightarrow P_{v \max} \leq 10\text{kW/m}^3 \times V_{CE}$
 $\leq 10 \times 10^3 \times 4310 \times 10^{-9}$ compared to copper loss,
 $P_{v \max} \leq 0.043\text{W}$ It's not negligible.

4. Calculate the maximum temperature rise for your filter inductor design, considering its maximum-loss operating point. Comment on whether or not this is acceptable according to material temperature limits.



$P_{loss \ max} = 0.043\text{W}$

Table 25.1

Thermal Resistivities of Materials Used in Electronic Equipment

MATERIAL THERMAL RESISTIVITY ($^\circ\text{C}\cdot\text{m/W}$)

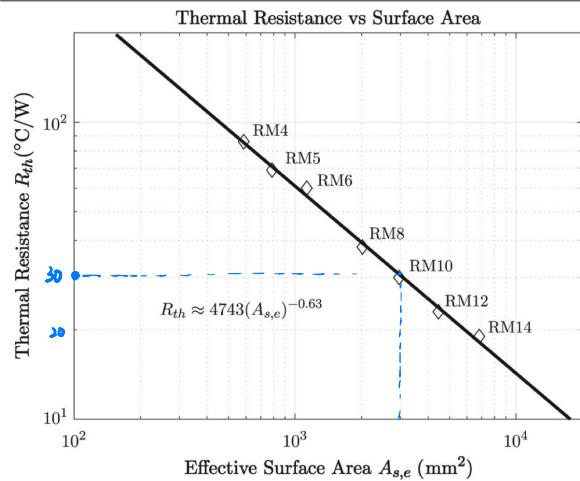
Still air	30.50
Mylar	6.35
Silicone grease	5.20
Mica	1.50
Filled silicone grease	1.30
Filled silicone rubber	1.0
Alumina (Al_2O_3)	0.06
Silicon	0.012
Beryllia (BeO)	0.01
Aluminum Nitride (AlN)	0.0064
Aluminum	0.0042
Copper	0.0025

For Inductor core loss, which we use RM10. $R_{th} = 30^\circ\text{C/W}$

$\Rightarrow T_{hotspot} = T_{amb} + 0.043 \times 30$

$= 25 + 1.293$

$= 26.93^\circ\text{C}$, ✓ ΔT very small



Filter Capacitor Selection and Loss

There are several types of capacitors utilized in power circuits. In Module 0, you sized C_{in} and C_{out} according to a ripple specification. Such large dc filter capacitances are commonly realized with electrolytic capacitors, which offer very high capacitance per unit volume compared to other types. However, electrolytic capacitors tend to have higher series resistance and therefore low current ratings. Multilayer ceramic capacitors (MLCCs) offer low series resistance and inductance, which is particularly useful for high-frequency filtering (i.e., decoupling capacitors). Thus, use of electrolytic capacitors in parallel with ceramic capacitors often provides a fruitful combination of high density and low impedance.

In this section, you will evaluate electrolytic capacitors and MLCCs for realizing C_{in} and C_{out} . Note: Not all capacitor manufacturers provide plots for voltage dependence, temperature dependence, etc. For evaluating MLCCs without such plots in their datasheets, search for similar parts on TDK's or Murata's website (same voltage rating, capacitance, size, and temperature code). You may assume the provided plots for comparable parts are representative of your part. See an example TDK MLCC part [here](#).

- Out of the electrolytic capacitors provided in our part library, select a capacitor and the number of them needed in parallel for realizing C_{in} . You should consider not only the voltage ratings of candidate parts but also their rms current ratings and ESR at the relevant frequency. On your board, there is space for up to three electrolytic capacitors for realizing C_{in} , though you should only use the number of spaces you actually need.
- For realizing C_{in} , select a potential alternative capacitor arrangement based on Class II ceramic parts in the provided parts library. In addition to voltage ratings and frequency-dependent ESR of candidate parts, you should also consider how their capacitances derate with bias voltage. On your board, there is space for up to four Class II ceramic capacitors of package size 1206 or 0805 for realizing C_{in} , though you should only use the number of capacitors in parallel that you actually need. Comment on the size and efficiency tradeoffs between the electrolytic and ceramic configurations.

From Module 0

$$C_{out} \geq 3.47 \mu F, C_{in} \geq 4.17 \times 10^{-5} F = 41.7 \mu F$$

Last week's module focused on switch selection, so this week's module will focus on passive components. In this module, we will design and prototype inductor L of Fig. 1 and select capacitors C_{in} and C_{out} .

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power Range	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq 5\%$
Output Voltage Ripple	$\leq 5\%$
Inductor Current Ripple (at 100W)	$\leq 20\%$

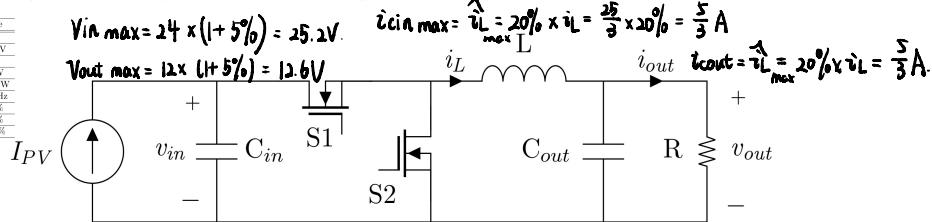


Figure 1: Synchronous buck converter.

So the requirement:

$$C_{in} \geq 41.7 \mu F, \text{ voltage rating} \geq 25.2V, \text{ current rating} \geq 1.67A$$

$$C_{out} \geq 3.47 \mu F, \text{ voltage rating} \geq 12.6V, \text{ current rating} \geq 1.67A$$

\times ESR ↓ at 100kHz.

PARTS: CAPACITOR LIBRARY

Electrolytic, 330 μ F	EL1V331MP51016U
Electrolytic, 470 μ F	502LJ470M10X20
MLCC, 22 μ F, 35V, X5R, 0805	C2012X5R1V226M125A
MLCC, 4.7 μ F, 35V, X7R, 0805	GRM21BZ7Y4A75KE15K
MLCC, 22uF, 35V, X5R, 1206	C3216X5R1V226M160AC
MLCC, 10uF, 35V, X7R, 1206	C1208Y106K035T
MLCC, 10uF, 50V, X5R, 0805	GRM21BR61H106KE43K
MLCC, 10uF, 50 V, X7R, 1206	C1208Y7R500-106KNE-CT
2.2 μ F, Commutation loop decoupling, 0803, 50V	GRM188R61H225KE11J
10 uF, 25 V Decoupling for gate drive, LDO, lbg reg, current sense	GRM188R61E06KAT73J
1 μ F, 50V	0603X105K500T
.1 μ F, 25V Current sense, op amp, regulator input decoupling	C0603Z25U250-104MNPF-CT
LDO bypass, 10nF, 0603, 3 V	C0603XTR250-103MNPF-CT
Filter cap, 330 pF, 50V, NPO, 0603	C0603CUG250-331KNE-CT
Current sense SHDN cap, 10 pF, 5V max, 0603	C0603C100J3HAC7867

PARTS: CAPACITOR LIBRARY

Electrolytic, 330 μ F	EL1V331MP51016U
Electrolytic, 470 μ F	50ZLJ470M10X20
MLCC, 22 μ F, 35V, X5R, 0805	C2012X5R1V22M0125A
MLCC, 4.7uF, 35V, X7R, 0805	GRM21BZ7Y4475KE15K
MLCC, 10uF, 35V, X7R, 1206	C3216X5R1V22M160AC
MLCC, 10uF, 50V, X5R, 0805	C1206X106K035T
MLCC, 10uF, 50 V, X7R, 1206	GRM21BR61H106KE43K
2.2 μ F, Commutation loop decoupling, 0603, 50V	C1206X7R500-106KNE-CT
10 μ F, 25 V Decoupling for gate drive, LDO, lg reg, current sense	GRM18BR61H225KE11J
.1 μ F, 50V	0603X105K500CT
.1 μ F, 25V Current sense, op amp, regulator input decoupling	C0603Z5U250-104MNP-CT
LDO bypass, 10nF, 0603, 3 V	C0603X7R250-103MNP-CT
Filter cap, 330 pF, 50V, NPO, 0603	C0603CG250-331KNE-CT
Current sense SHDN cap, 10 pF, 5V max, 0603	C0603C100J3HAC786T

So the requirement:

$C_{in} \geq 47 \mu F$, voltage rating $\geq 25.2V$, current rating $\geq 1.67A$

$C_{out} \geq 347 \mu F$ voltage rating $\geq 12.6V$ current rating $\geq 1.67A$

& ESR ✓ at 100 kHz

ii) If we use Electrolytic capacitor:

cheap

EL1V331...

TYPE	DESCRIPTION
Category	Capacitors Aluminum Electrolytic Capacitors
Mfr	Chisan (Elite)
Series	EL
Packaging	Cut Tape (CT) ② Tape & Box (TB) ②
Part Status	Active
Capacitance	<u>330 μF</u> ✓
Tolerance	±20%
Voltage - Rated	<u>35 V</u> ✓
ESR (Equivalent Series Resistance)	-
Lifetime @ Temp.	2000 Hrs @ 105°C
Operating Temperature	-40°C ~ 105°C
Polarization	Polar
Ratings	-
Applications	General Purpose
Ripple Current @ Low Frequency	886.6 mA @ 120 Hz
Ripple Current @ High Frequency	* <u>1.43 A @ 100 kHz</u> $\leq 1.67A$ (must parallel to tolerate current ripples)
Impedance	<u>38 mOhms</u>
Lead Spacing	0.197" (5.00mm)
Size / Dimension	0.394" Dia (10.00mm)
Height - Seated (Max)	0.689" (17.50mm)
Surface Mount Land Size	-
Mounting Type	Through Hole

TYPE	DESCRIPTION
Category	Capacitors Aluminum Electrolytic Capacitors
Mfr	Rubycon
Series	ZLJ
Packaging	Bulk ②
Part Status	Active
Capacitance	<u>470 μF</u> ✓
Tolerance	±20%
Voltage - Rated	<u>50 V</u> ✓
ESR (Equivalent Series Resistance)	-
Lifetime @ Temp.	10000 Hrs @ 105°C
Operating Temperature	-40°C ~ 105°C
Polarization	Polar
Ratings	-
Applications	General Purpose
Ripple Current @ Low Frequency	1.375 A @ 120 Hz
Ripple Current @ High Frequency	<u>2.5 A @ 100 kHz</u> ✓ no need to parallel.
Impedance	<u>37 mOhms</u>
Lead Spacing	0.197" (5.00mm)
Size / Dimension	0.394" Dia (10.00mm)
Height - Seated (Max)	0.866" (22.00mm)
Surface Mount Land Size	-
Mounting Type	Through Hole

choose 50 ZLJ4---- (Ideally no parallel is ok) ✓ → For both C_{in} and C_{out}
but in case, parallel 2 Capacitors.

(2). If we use MLCC,

For C_{in} , we must parallel 3~4 MLCCs. ← same type, only different package { 0805
1206 }

For C_{out} , it's pretty loose terms.

So we choose to parallel 2~3 $47 \mu F$ GRM21B... ✓

3. For realizing C_{in} , choose either the electrolytic capacitors, the ceramic capacitors, or a parallel configuration of both that provides a good combination of high density and low ESR. Provide part numbers for each, and how many of each are needed. Show that the resulting ripple is acceptable and that rms currents of all electrolytic capacitors are within their limits according to the datasheets. If you have multiple types of capacitors in parallel, you should either use impedance division to determine the rms current through each or assume all of the current goes through each type (as a very conservative estimate).

4. Similarly design a ceramic capacitor configuration for realizing C_{out} from the parts provided in our library. On your board, there is space for up to eight Class II ceramic capacitors of package size 1206 or 0805 for realizing C_{out} , though you should only use the number of capacitors in parallel that you actually need.

(3) For power supplies (bulk energy storage) C_{in}

* use electrolytic capacitor (to be the best, just choose the same paralleled capacitor for balancing current and division of heat and loss)

$$\text{so we choose to parallel 3 } C_{in} = 4.7\mu F, \underline{C_{total} = 14.1\mu F}, \underline{I_{ripples} = \frac{B \cdot 0.1}{8C}}, \underline{i_{rms} = \frac{1}{3} \times \frac{5}{3} = \frac{5}{9} \leq 2.5A \text{ (datasheet)}}.$$

$$\underline{\geq 41.7\mu F}$$

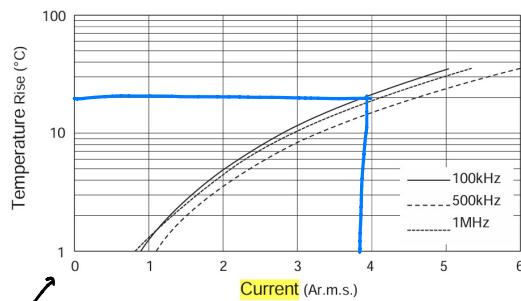
For C_{out} , we can use ceramic capacitor for its not so strict requirement

\Rightarrow parallel 3~4 $10\mu F$ capacitors, and $C = 30\mu F > 3.47\mu F$, inoted meets requirement.

[Example of Temperature Rise (Heat Generation) in Chip Monolithic Ceramic Capacitors in Contrast to Ripple Current]

Sample: R(R1) characteristics $10\mu F$, Rated voltage: DC10V

Ripple Current



$$\text{inoted ripple} = \frac{1}{3} \times \frac{5}{3} = \frac{5}{9} \leq 4A \text{ (datasheet).}$$

(4). From (3). C_{out} , we choose 3 paralleled $10\mu F$ capacitors. packaged 1206 (0805 ok also)

5. Calculate the expected conduction loss each for C_{in} and C_{out} . You should consider the rms current through each capacitance and the capacitance's total ESR at the relevant frequency. If you have multiple types of capacitors in parallel, you should use impedance division to determine the rms current through each.
6. Determine whether or not your expected capacitor losses are significant compared to your total expected converter losses. If so, consider adding additional capacitors in parallel to reduce ESR, but only as many as you actually need to reduce your capacitor losses to the point of being negligible compared to your whole converter's loss. If not, consider reducing the number of capacitors in parallel in order to reduce the necessary size and cost, ensuring your designs still meet ripple and rms current requirements. The decision of how many capacitors to use in parallel often involves this tradeoff.

$$\frac{12V}{20V}$$

(5). conduction loss, basically because of ESR

For C_{in} : 470μF, $ESR = 37m\Omega$ at 100kHz, parallel 3 of them.

$$\Rightarrow i_{C1\text{rms}} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{C1(t)}^2 dt} \\ = \sqrt{3.33^2 \times 0.6 + 5^2 \times 0.4} \\ = 4.089A$$

$$P_{loss} = 3 \times \left(\frac{4.089}{3}\right)^2 \times 37 \times 10^{-3} = 0.2053W$$

Multilayer Ceramic Chip Capacitors

Product Top Page | Part No. List | Search by Part No. | Search by Characteristics | Cross Reference | Catalog | Te

C2012X5R1E106K125AB

TDK item description	C2012X5R1E106K125AB
Applications	Commercial Grade
Feature	General (General Up to 75V)
Series	C2012 (EIA 0805)
Status	Production
Brand	TDK

C_{in} .

↓ 470μF, but expensive ↓



At nominal point

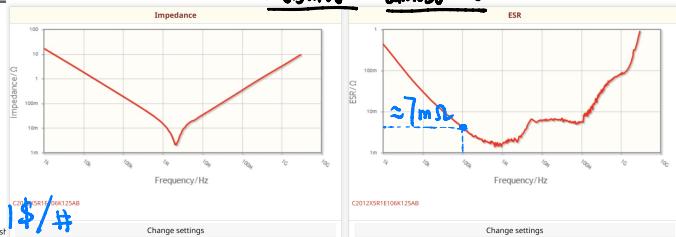
$$i_C = |I_{PV} - I_L| = \left| \frac{100W}{20V} - \frac{100W}{12V} \right| \\ = 3.33A \quad DTS \quad D=0.6$$

$$i_Q = |I_{PV}| = 5A. \quad DTS. \quad D=0.4$$

For C_{out} . Since for MLFF, I have to find a capacitor not from the list, all of MLFF in the lists do not provide ESR.

$$i_{C2} = \Delta i_L = 1.67A. \quad s.t. \parallel 3 \text{ cap.}$$

$$\rightarrow P = 3 \times \left(\frac{1.67}{3}\right)^2 \times 7m\Omega \\ = 6.5mW \quad \underline{\text{almost } \rightarrow 0}$$



- (b) In my design, electrolytic capacitor # can be reduced to 1 or 2, but will lead to some comparatively large ripples and large losses, but not so much. [which also meets requirement]

→ Also to avoid ESR losses

C_{out} : ceramic capacitor, # → may not be reduced so much, can even be parallel more, for C_{out} requirement ↓ and P_{loss} is small. So we don't need to reduce #.

Feedback: pre-lab 18 hours. (quite large workload).

Lab:

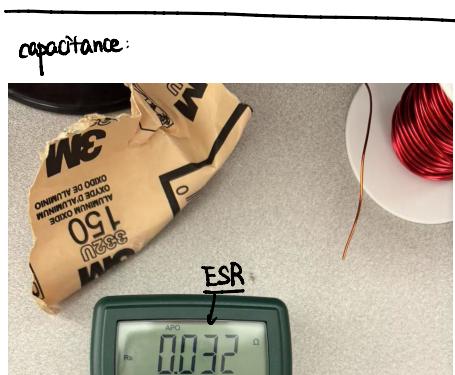
LCR Meter

Now that you have built your inductor, characterize it using an LCR meter as follows:

39.1 uH read

36uF

1. Measure your inductor's inductance at low frequency, and compare it to your design value. If your inductance measurement is significantly off, double check your inductance calculation and your shim stock thickness. The acceptable range for your characterized inductance is 100-110% the minimum value needed to meet the ripple specifications.
2. Measure your inductor's equivalent series resistance (ESR), and compare it to your design value.
3. Measure your inductor's inductance and ESR at 100 kHz, and compare these values to your low-frequency measurements.



During Module 1, you simulated your buck converter considering only switch parasitics. Now, update the inductance and capacitances to their characterized values (i.e., your characterized inductance and capacitance for the inductor and the electrolytic capacitor, respectively, and the manufacturer-provided capacitance of any MLCCs considering derating). Then, add parasitics (i.e., ESR) to each component as characterized at the appropriate frequency. Note: If you use several identical capacitors in parallel, you may combine their impedances in parallel (considering each to be an R-C branch) to form a single R-C branch.

Simulate your converter with both switch and passive component nonidealities, and determine the following for the nominal operating point and each corner operating point:

③ C_{in} not enough. ② datasheet.

1. The efficiency of your power converter. Compare this to the efficiency you measured in Module 1 considering only switch parasitics.
2. The power loss incurred by each of the passives, estimated via simulation. Compare this to the expected loss you calculated in the previous section.
3. The maximum ripples on i_L , v_{in} , and v_{out} .
4. The rms current through any electrolytic capacitors.

characterized values: $C: 100\text{Hz} = 0.032\Omega \text{ ESR}$
 $422.3\mu\text{F}$

$100\text{kHz} = 8.18\mu\text{F}$
 0.036Ω

$L: 100\text{Hz} = 38\mu\text{H}$
 $0.01\Omega \text{ ESR}$ ✓

$100\text{kHz} = 3846\text{H}$
 0.385Ω

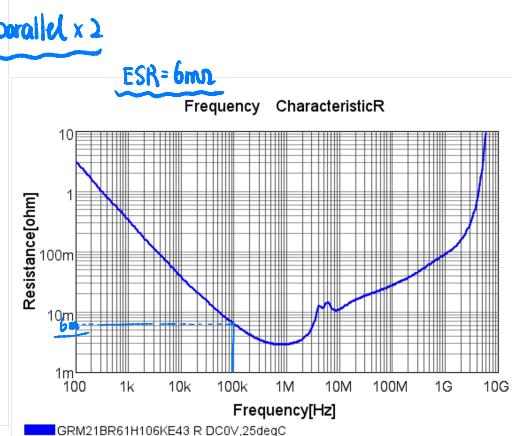
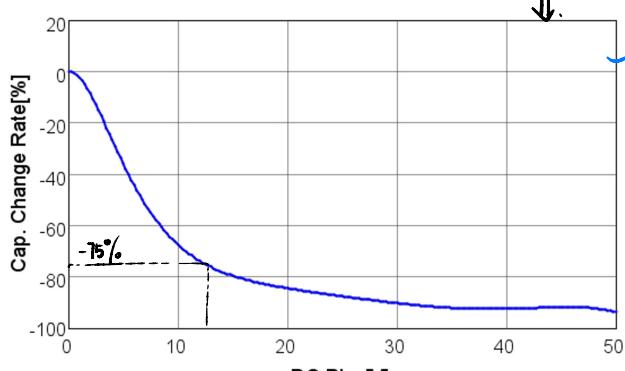
We know that $\Delta i_L = 20\% i_L$ at nominal point.

$$\Delta i_L = 20\% \times \frac{100}{12} = \frac{20}{12} = \frac{5}{3} \text{ A} \quad I_L = \frac{100}{12} = \frac{25}{3} \text{ A}$$

$$\Delta i_C \approx \Delta i_L = \frac{5}{3} \text{ A} \text{ (peak-to-peak)}.$$

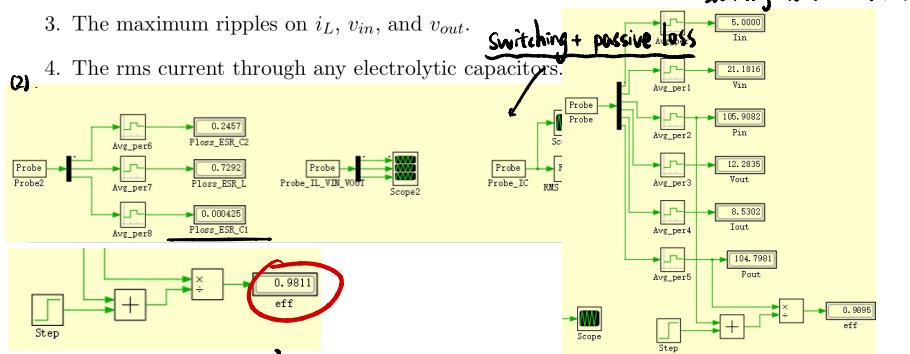
$$\Delta i_C \text{ RMS} = \frac{5}{6} \cdot \frac{1}{\sqrt{2}} = \frac{5}{6\sqrt{2}} \text{ (A)}$$

GRM21BR61 = $C \approx (1-75\%) \times 10\mu\text{F} = 2.5\mu\text{F}$
 DC bias characteristics



- The efficiency of your power converter. Compare this to the efficiency you measured in Module 1 considering only switch parasitics.
- The power loss incurred by each of the passives, estimated via simulation. Compare this to the expected loss you calculated in the previous section.
- The maximum ripples on i_L , v_{in} , and v_{out} .
- The rms current through any electrolytic capacitors.

(2)



$$P_L = I_{rms}^2 \cdot ESR_L$$

$$= \left(\frac{100}{12}\right)^2 \times 0.01$$

$$\approx 0.6944 \quad \text{by hand}$$

$$= 0.7292 \quad \text{by simulation}$$

$$P_{cout} = \Delta V_L \cdot \frac{1}{\sqrt{2}} \times ESR_{cout}$$

$$= \frac{5}{3} \times \frac{1}{\sqrt{2}} \times 0.006$$

$$= 0.0071$$

$$P_{cout-2} = 2P_{cout} = 0.0142$$

Higher because ignore C ripples.

0.004 simulation.

Efficiency: $P = 100W$ $V_{in} = 16V$ 98.14%

$P = 100W$ $V_{in} = 24V$ 98.10%

$P = 50W$ $V_{in} = 16V$ 98.87%

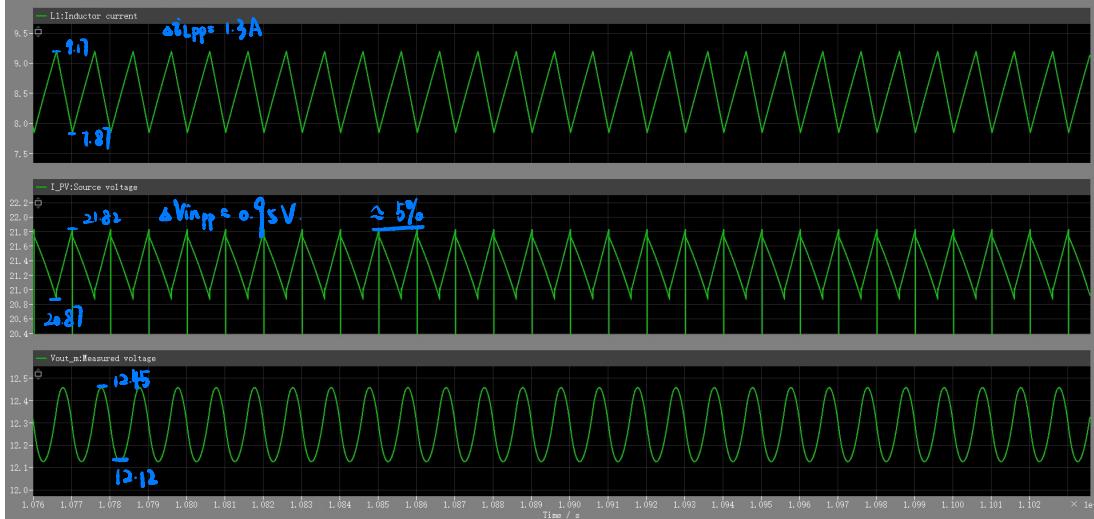
$P = 50W$ $V_{in} = 24V$ 98.82%

(3)

why strikes?

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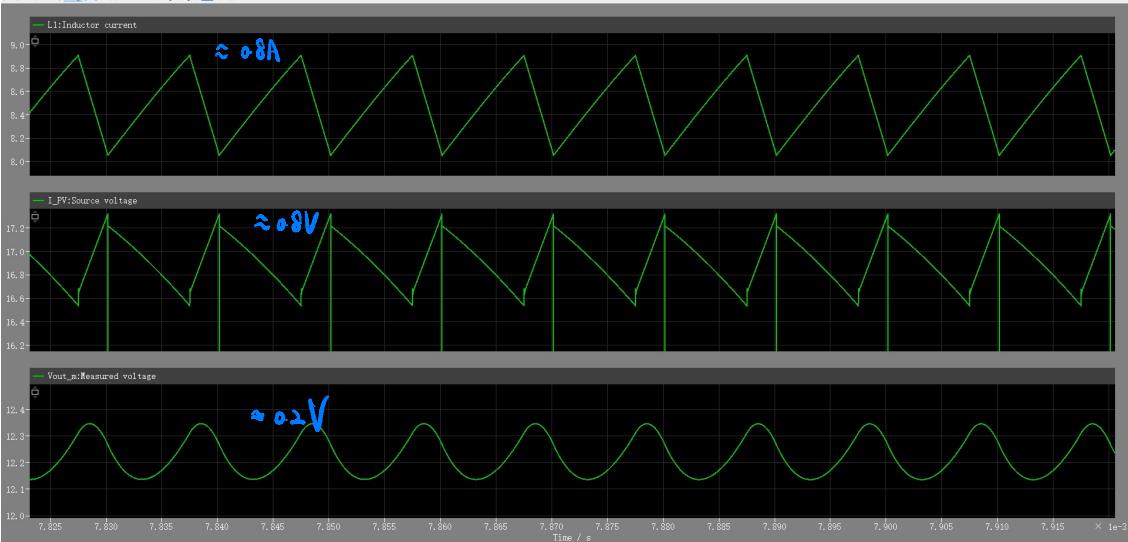
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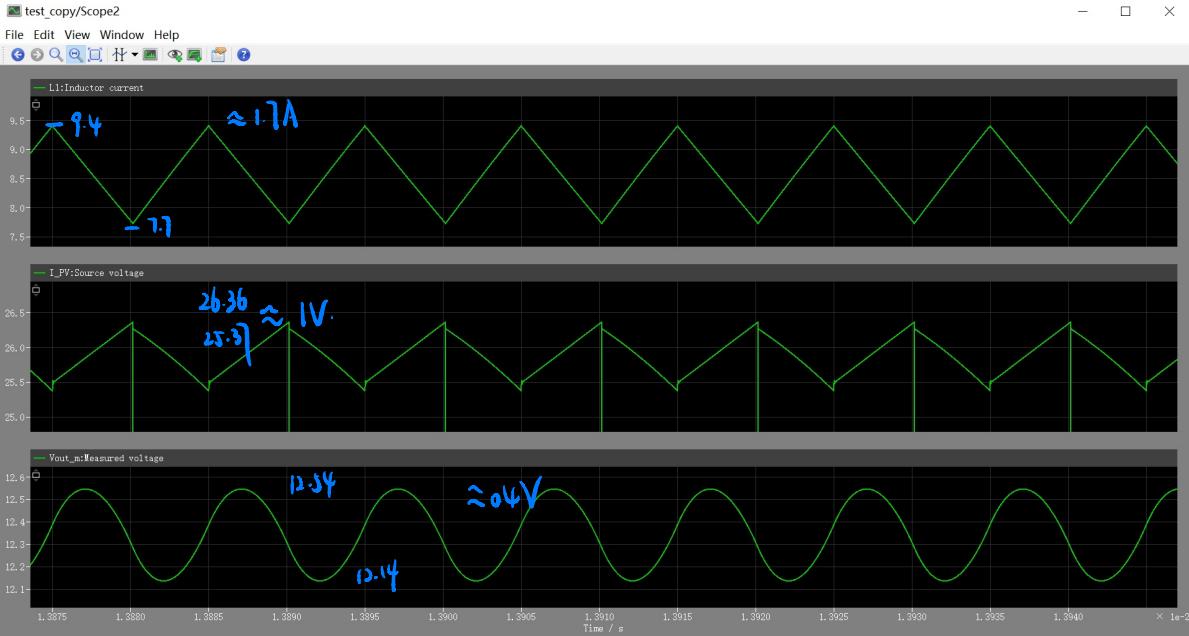
$$P = 100W, V_{in} = 16V$$

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$$P=100W, V_{in}=24V \cdot (\text{worst-case})$$



4).

