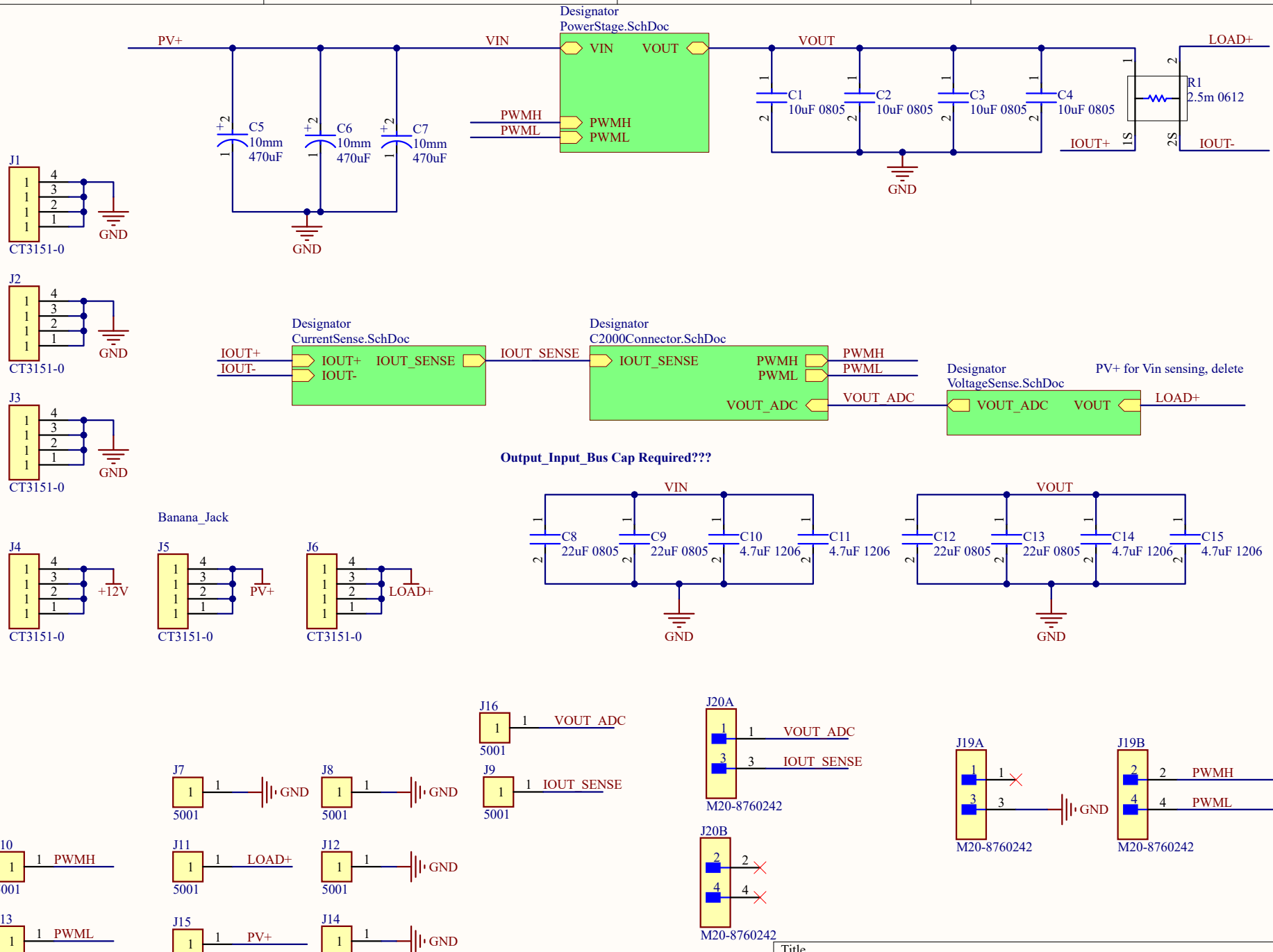
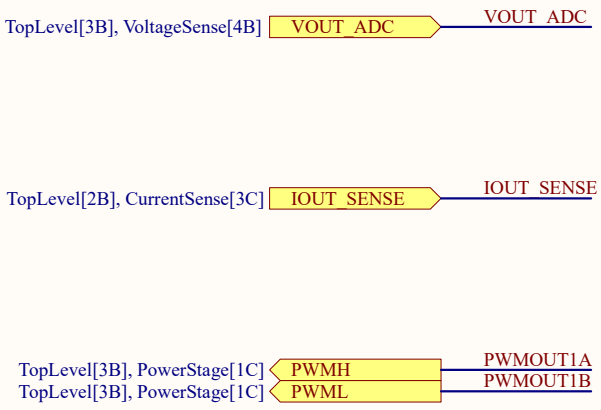


Title	**EE113B PV Buck Converter**	
Size: A	Number: **TopLevel.SchDoc**	Revision:
Date: 3/18/2025		Sheet 1 of 5
File: D:\Altium_learn\..\TopLevel.SchDoc		Drawn By: *Shikai Shen*



Title	**EE113B PV Buck Converter**	
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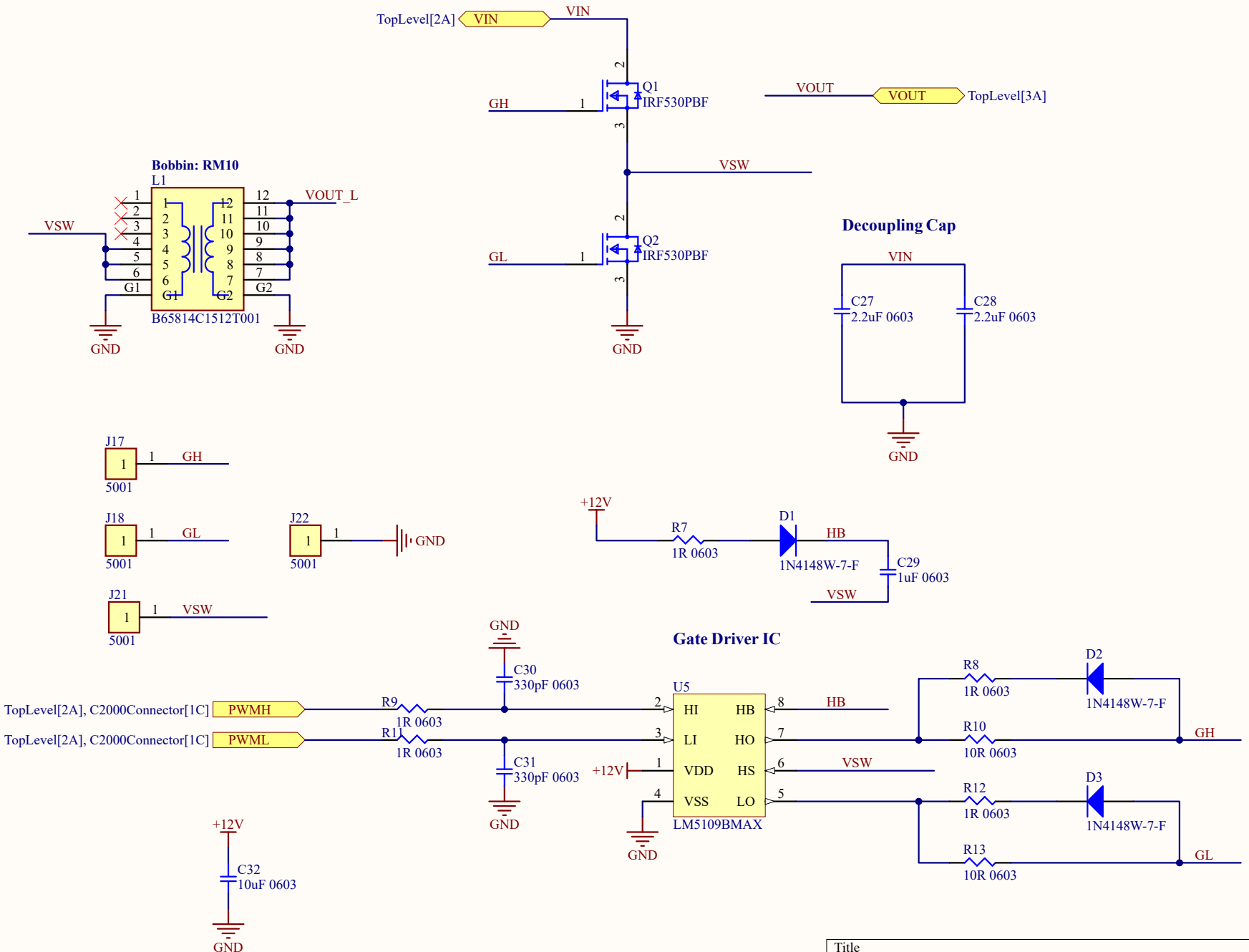
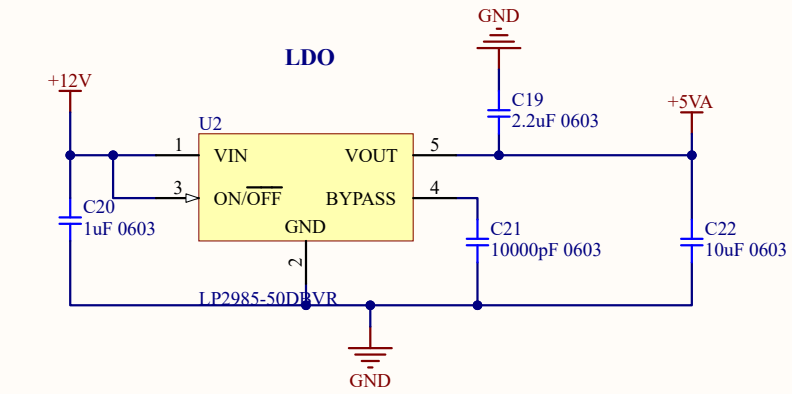
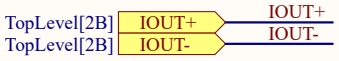
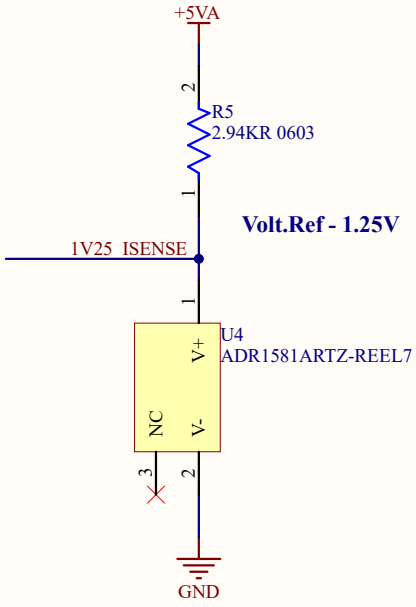
Date: 3/18/2025		Sheet 5 of 5
File: D:\Altium_learn\..\C2000Connector.SchDoc		Drawn By: *Shikai Shen*

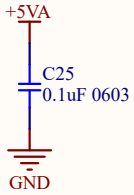


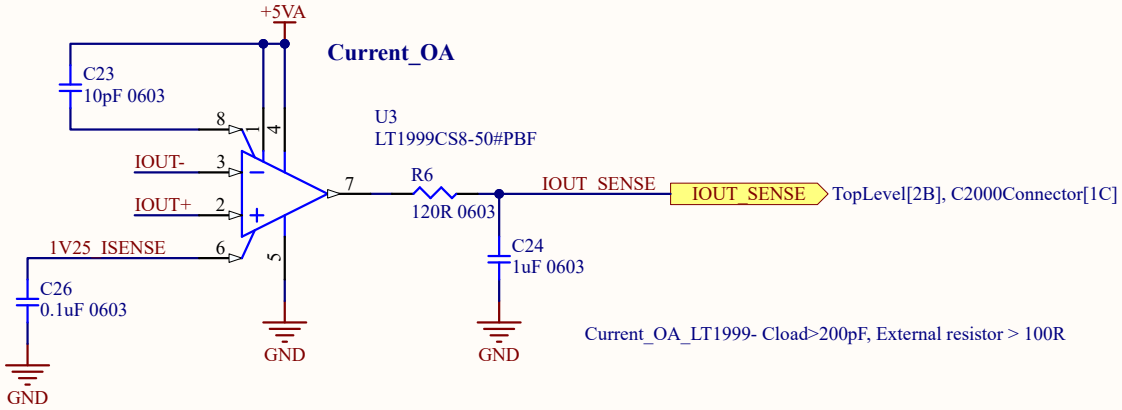
Title	**EE113B PV Buck Converter**	
Size: A	Number: **PowerStage.SchDoc**	Revision:
Date: 3/18/2025		Sheet4 of 5
File: D:\Altium_learn\..\PowerStage.SchDoc		Drawn By: *Shikai Shen*



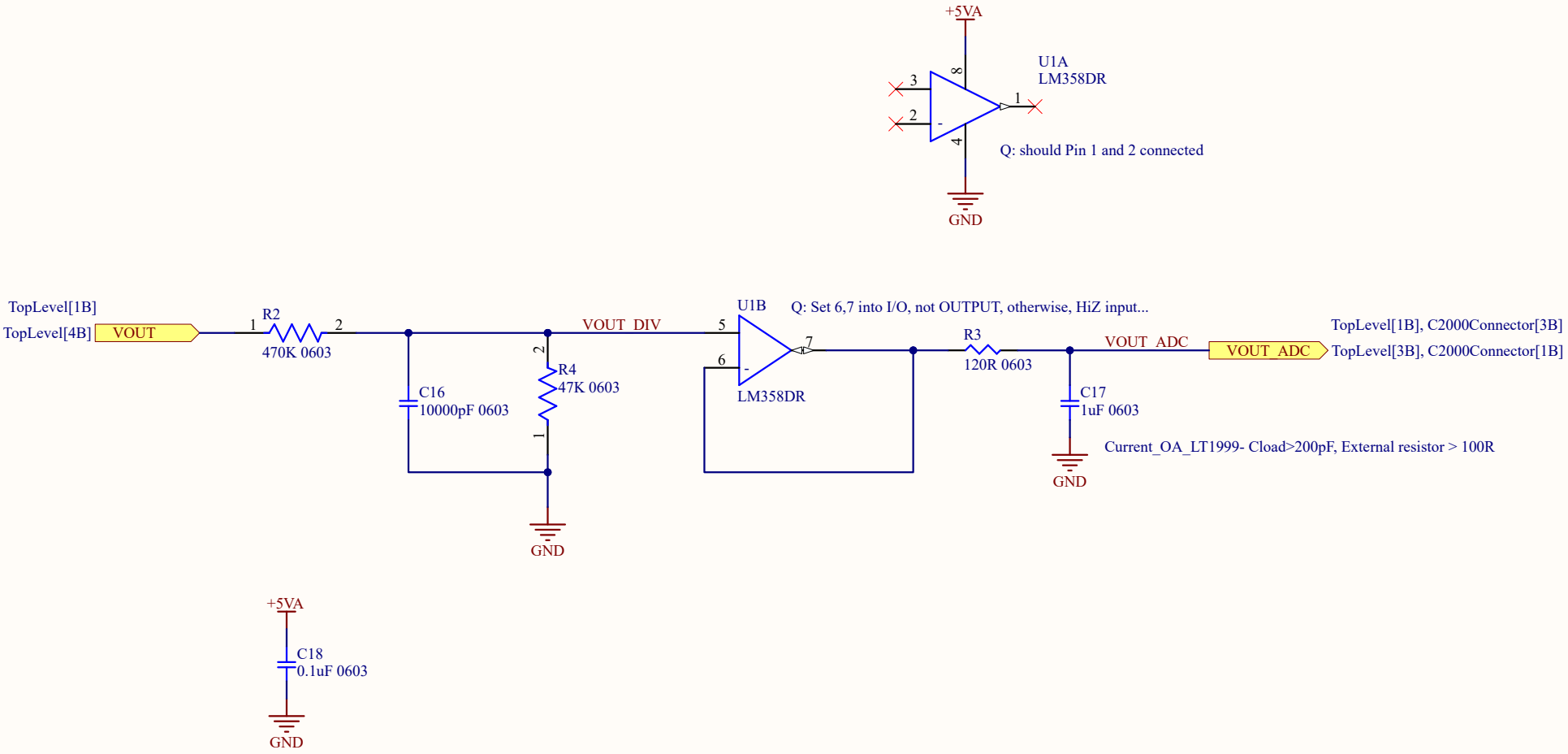




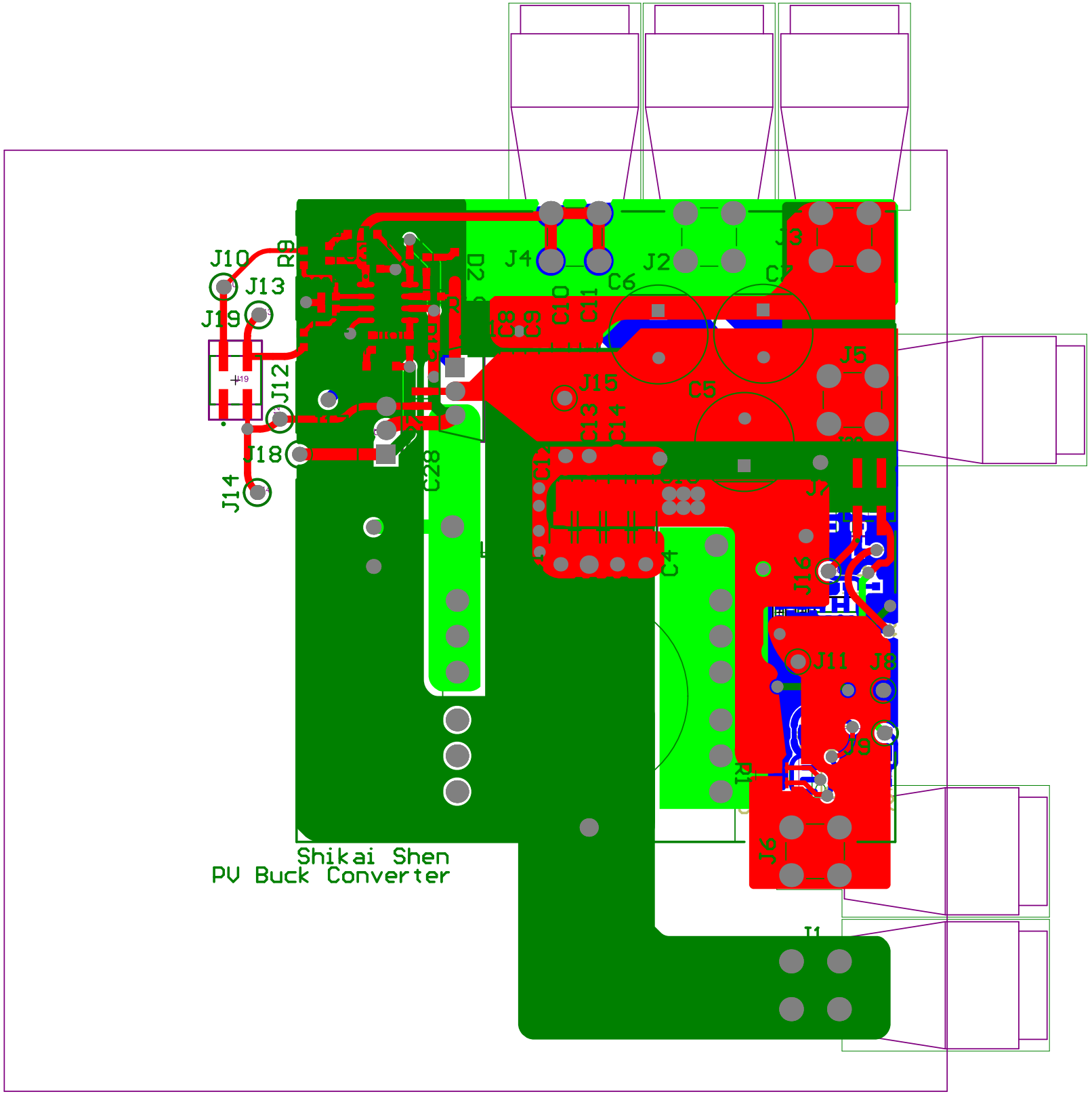




Title	**EE113B PV Buck Converter**	
Size: A	Number: **CurrentSense.SchDoc**	Revision:
Date: 3/18/2025		Sheet3 of 5
File: D:\Altium_learn\..\CurrentSense.SchDoc		Drawn By: *Shikai Shen*



Title	**EE113B PV Buck Converter**	
Size: A	Number: **VoltageSense.SchDoc**	Revision:
Date: 3/18/2025		Sheet2 of 5
File: D:\Altium_learn\..\VoltageSense.SchDoc		Drawn By: *Shikai Shen*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C28
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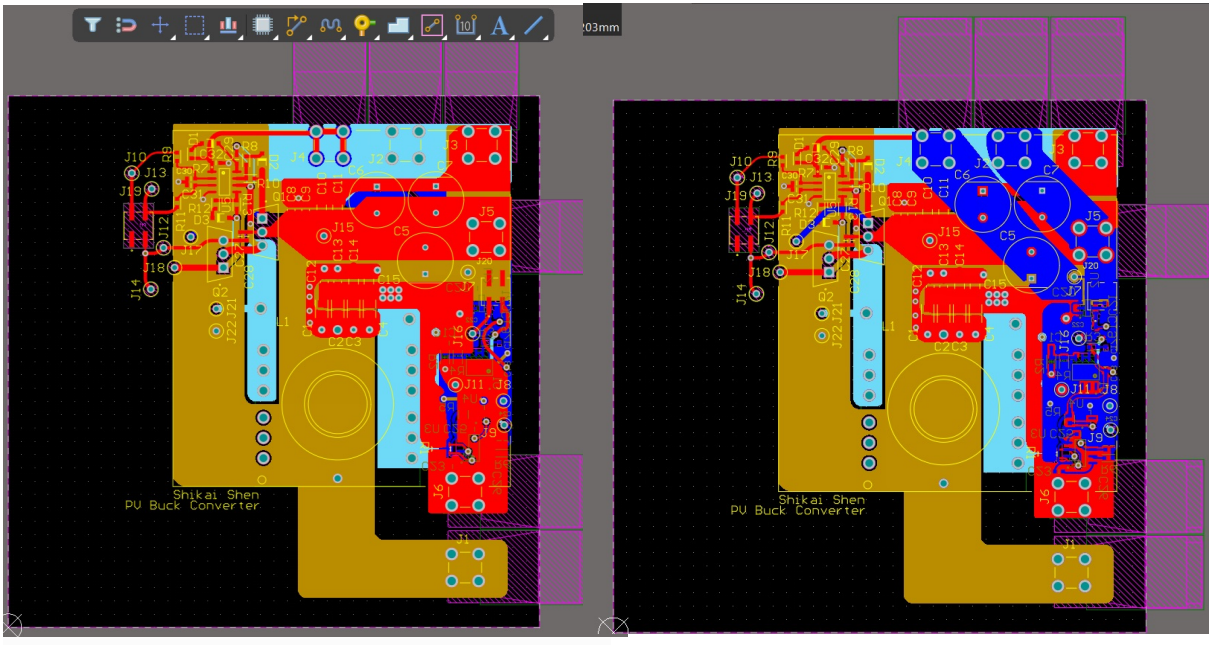
PV Buck Converter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PV Buck Converter
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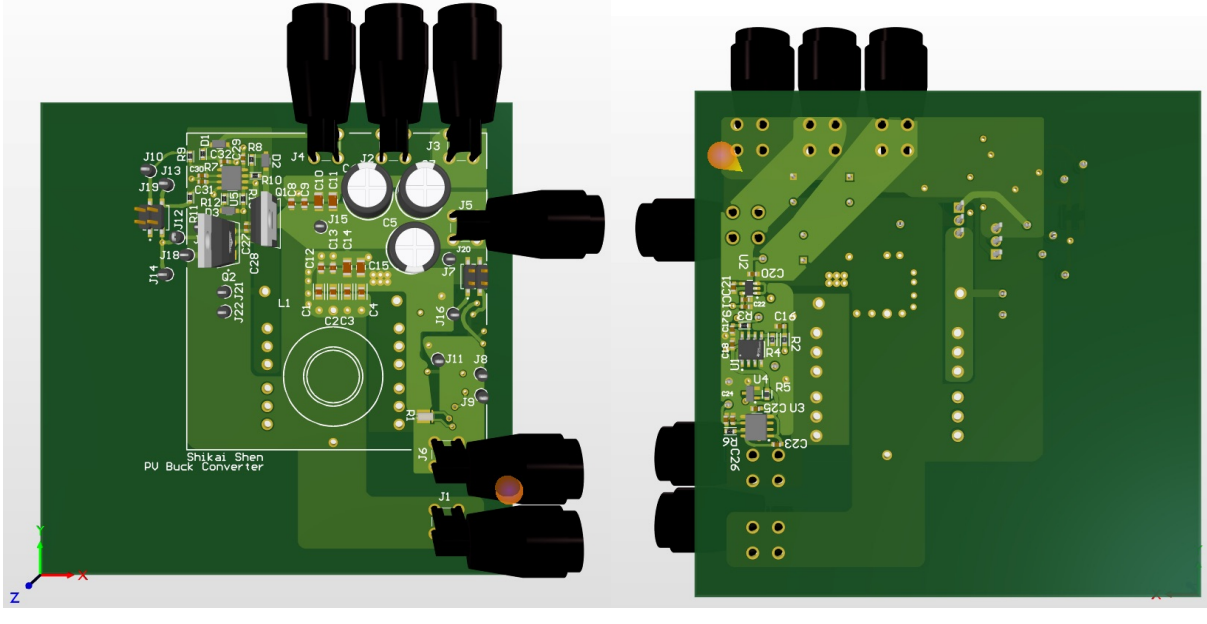
PV Buck Converter


Shikai Shen
PV Buck Converter

Lab Takeaway

1. In your own words, describe what parasitic inductance is, what types of loops are most sensitive to it, how parasitic inductance in these loops affects power converter operation, and how parasitic inductance can be minimized.

Parasitic inductance is the unintended inductance carried out by the circuits in twining shape like wires or some loops. High di/dt loops are very sensitive to it, which might be gate loops (GL and GH) and commutation loops (mostly flowing through capacitors and switches). To minimize the unintended parasitic inductance, we shall apply basically small loops, ground planes, wide traces.

2. In your own words, describe what parasitic capacitance is, what types of nodes are most sensitive to it, how parasitic capacitance in these loops affects power converter operation, and how parasitic capacitance can be minimized. Describe one strategy for protecting critical aspects of a power converter design from parasitic capacitance.

Parasitic capacitance is the unintended capacitance that forms between conductive elements due to their proximity in a circuit, such as between PCB traces, component leads, or different layers of a PCB. It has significant impact on circuits, especially in high-voltage, high frequency and high dv/dt nodes, which leads to large current spikes, increasing the loss and damaging the components.

1st strategy is by using shield to avoid the impact of parasitic capacitance, which can be seen as an isolation. 2nd strategy is to leave enough space between high dv/dt nodes.

3. In your own words, describe important considerations for placing and routing power stage current paths.

As for the AC traces, we should minimize the parasitic inductance and capacitance by having as small area as possible; For DC traces, we should minimize the ESR by having large and short traces. Also identify the high-frequency loops and high-current loops to try to reduce the parasitic parameters.

4. In your own words, describe important considerations for placing and routing analog circuits.

First, we shall place the sensing circuit away from the high dv/dt and di/dt nodes, otherwise the spikes on these nodes may directly go to the sensing circuits and have inconsistent voltage references. Second, the circuits should be placed away from the return loops from Vout to Vin since the ground between these two nodes have comparatively large inductance and resistance.

5. Describe the benefits of using a ground plane, and considerations to be made when designing one.

Using a ground plane in a PCB design provides several key benefits, particularly in power electronics and high-frequency circuits. One of the primary advantages is that it offers a low-impedance return path for current, which helps to minimize voltage fluctuations and ensure stable circuit operation

Build Intuition

1. Describe a systematic strategy for power converter PCB layout. Which aspects would you prioritize, and in what order?

1st, Identify the high dv/dt nodes and high di/dt nodes.

2nd, Find the high dv/dt loops and using commutation loops, gate loops and decoupling capacitors to minimize the area of these loops.

3rd, Place the sensing circuits far away from these nodes and try to find the power stage current returns and sensing circuits should also be far away from them.

4th, Place the ground or Vin polygons, to minimize the resistance of DC or inductance, capacitance of AC.

5th, Place the test points.

2. How would this PCB layout strategy change for a converter operating at a higher switching frequency

For a higher switching frequency converter, the PCB layout strategy must further minimize high-current loop areas, use shorter and wider traces, enhance grounding and return paths, select low-parasitic components, improve shielding and noise isolation, consider low-loss PCB materials, optimize thermal management, and implement EMI mitigation techniques to maintain efficiency and reliability.

3. Describe the role that component packages (i.e., package size, package shape, length of leads, etc.) play in the critical aspects of PCB layout. Are there certain aspects of your PCB layout that could have been improved with different component packages? If so, which components?

Component packages impact PCB layout by affecting parasitic inductance, resistance, thermal performance, and space efficiency, where smaller SMD packages reduce parasitics and improve high-frequency performance, while larger packages handle higher power but may increase trace lengths and inductance. PCB layout could be improved by using low-inductance MOSFET packages (e.g., PQFN instead of TO-220) to reduce switching losses and low-profile ceramic capacitors to minimize ESR and inductance, leading to better efficiency and thermal management.

4. Describe how PCB layout affects the efficiency of your power converter.

PCB layout directly impacts the efficiency of a power converter by influencing resistive losses, switching losses, EMI, and thermal performance. Poor layout choices, such as narrow traces or long current paths, increase resistance and voltage drops, leading to power dissipation and reduced efficiency. Excessive parasitic inductance in high-speed switching loops can cause voltage spikes, ringing, and increased switching losses, lowering overall performance. Similarly, parasitic capacitance between traces and layers can lead to unintended coupling and increased EMI, requiring additional filtering that can further impact efficiency. Inefficient thermal management due to poor component placement or inadequate copper pours results in higher operating temperatures, increasing conduction losses in semiconductors. A well-optimized PCB layout with short, wide traces, minimal parasitics, proper grounding, and efficient heat dissipation ensures reduced power losses, stable operation, and higher overall efficiency in a power converter.

Post-Lab hour: 1hour