

**EE 113B/213B: Power Electronics Design**  
**Module 2: Gate Drive Circuit**

## Objectives

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By the end of this module, you should be able to...

- Determine the gate drive needs of a MOSFET
- Evaluate the features of a gate driver IC
- Calculate expected gate drive and overlap loss
- Design a bootstrap circuit
- Place and size decoupling capacitors
- Systematically assemble and test a gate drive circuit
- Tune gate loop resistance and dead time

Recommended reading: KPVS Chapters 22.1, 23.1

# Pre-lab Assignment

Now that you have selected your switches, it's time to design the gate drive circuits for S1 and S2. Gate drive circuits commonly employ integrated circuits (ICs), and a plethora of possibilities exists for both the features of these ICs and the circuit architectures enabled by them. This module will focus on how we *utilize* ICs in gate drive circuits; we will leave the details of how these ICs operate to an analog integrated circuit design class.

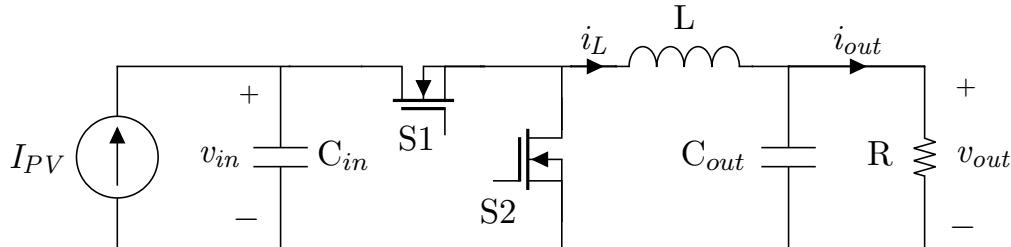


Figure 1: Synchronous buck converter.

## Gate Drive Needs and IC Characteristics

For your gate drive circuit you may assume you will use the half-bridge gate driver IC provided in the parts library. This IC has inputs and outputs for driving both the high side and low side devices of a half bridge. In this section you will learn more about the features of this gate driver.

1. Based on information provided in the datasheet for your selected switch, choose an appropriate gate-source drive voltage.
2. For the specified gate driver, what is the gate drive supply range? Comment on whether or not this is suitable for your intended drive voltage.
3. Unlike low side gate drivers, a half-bridge gate driver must be capable of withstanding the *difference* between the supply voltages for the high side and low side switches. While the low side supply voltage is fixed and referenced to ground, the high side supply voltage is floating and referenced to the switch node. For the specified gate driver, what is the maximum high side supply voltage relative to ground? Comment on whether or not this is suitable for the expected range of your converter's switch node voltage plus your drive voltage.
4. An important feature of any gate driver is how much current it can source and sink. What are the current source and sink capabilities of the specified gate driver?

## Overlap Loss

To calculate overlap loss in Module 1, you approximated the rise and fall times for the switch's drain-source voltage, and you assumed overlap loss was only present during hard turn-on transitions. These approximations may or may not reflect your actual design. Given the current source and sink capabilities of your half-bridge gate driver IC,

1. Determine which switch transitions have non-negligible overlap loss, and justify your claim. You should consider both turn-on and turn-off transitions.
2. For switch transitions with non-negligible overlap loss, calculate the overlap time based on the  $V_{gs}$  vs.  $Q_g$  plot for your switch.
3. Recalculate the expected overlap loss for the nominal operating point and the four corner operating points.

- Provide a final breakdown of all losses in your switches at the nominal operating point and the four corner operating points. These calculations should reflect how the change in overlap loss affects the junction temperature, and how a change in junction temperature affects conduction loss.

Note: We didn't require this in Module 1, but a realistic switch selection process must consider these actual rise and fall times (based on the  $V_{gs}$  vs.  $Q_g$  plot) when calculating and comparing overlap loss. Thus, switches are often selected in conjunction with an appropriately sized gate drive IC.

## Gate Drive Loss

While gate drive loss is dissipated outside of the switch itself, it can be a significant portion of the converter's overall loss. Thus, gate drive loss can also be an important consideration during the switch selection process.

- Assume you have chosen a gate drive voltage of 10 V. Based on the  $V_{gs}$  vs.  $Q_g$  plot provided in your switch's datasheet, estimate the effective gate capacitance for your selected drive voltage. You may approximate the  $V_{gs}$  vs.  $Q_g$  relationship to be linear, based on the actual value of  $Q_g$  at the drive voltage.
- Based on the  $V_{gs}$  vs.  $Q_g$  plot provided in your switch's datasheet, estimate the energy that must be delivered to the gate (i.e., stored in the gate capacitance) to bring the gate-source voltage up to the drive voltage. You may calculate this directly from the  $V_{gs}$  vs.  $Q_g$  or using the effective gate capacitance calculated in the previous question.
- Calculate the total gate drive loss (i.e., the total power loss associated with driving your switches) assuming a drive voltage of 10 V.

## Bootstrap Circuit Design

Because the gate driver's low side supply voltage is referenced to ground, it can be easily generated from a fixed external supply. By contrast, the high side supply voltage is referenced to the switch node, which changes in voltage throughout the switching cycle. To drive the high side switch, the designer must generate a floating supply referenced to the switch node. This is commonly (and cost-effectively) done using a bootstrap circuit, shown in Fig. 2.

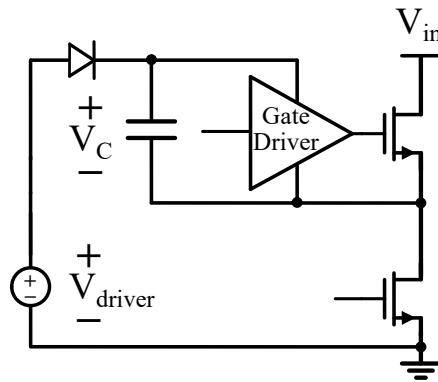


Figure 2: A bootstrap circuit to create a high side supply voltage.

- Calculate the necessary voltage ratings for a bootstrap capacitor and diode in your design.
- While the low side switch is on and the switch node is connected to the ground node, the bootstrap diode allows the high side floating supply to charge from the fixed external supply. Accordingly, it is important to select a bootstrap diode that has a low forward voltage drop (so the floating supply can charge as close as possible to the fixed supply voltage) and minimal reverse recovery (so the diode turning off doesn't discharge the floating supply). According to these criteria, select a bootstrap diode from the components provided in the parts library.

3. Calculate the effective drive voltage for the high side switch (i.e., what the gate driver actually sees as its supply voltage) considering the bootstrap diode's forward voltage drop.
4. To ensure that driving the gate of the high side switch does not deplete the floating high side supply by more than 10%, bootstrap capacitors are commonly sized to have at least 10x more capacitance than the switch's gate. Calculate the minimum bootstrap capacitor size accordingly, and select an appropriate value based on standard capacitor sizes.
5. Considering the charge delivered to drive the switch each cycle, show that your selected capacitance value will prevent the floating high side supply voltage from discharging by more than 10%.
6. A bootstrap resistor is often added in series with the diode to limit its peak current. Size this bootstrap resistor such that the bootstrap diode current is limited to an allowable value based on the diode's maximum ratings. Show that the resulting time constant between the bootstrap capacitor and this resistor is small compared to the switching cycle; otherwise, the presence of this resistor may prevent the bootstrap capacitor from fully charging.

## Decoupling Capacitors

Decoupling capacitors are important for isolating circuit components and ICs from high-frequency noise generated by other components on the same bus.

1. Based on the specified gate driver's datasheet, describe where decoupling capacitor(s) are needed. Draw a circuit diagram of how you plan to connect these decoupling capacitor(s) to the gate driver IC pins.
2. Size your decoupling capacitor assuming an 0603 MLCC package. It is generally advisable to size decoupling capacitors to have as large capacitance as possible to provide a low-impedance path for high-frequency noise. Show that the decoupling capacitor that will charge the bootstrap capacitor will not discharge by more than 10% when this occurs.

## Assignment Feedback (Required)

How much dedicated time did you spend on this pre-lab?

# Lab Assignment

When building circuit prototypes, it is best practice to systematically assemble and test small portions of the circuit at a time to verify correct operation before continuing. This helps reduce troubleshooting time later by isolating the scope of potential problems if the circuit doesn't operate correctly upon first assembly. In this lab, you will systematically assemble and test your gate drive circuit.

## Connect the Microcontroller

To systematically assemble and test your gate drive circuit, you will need a PWM signal. Thus, now is a good time to connect your microcontroller to the PCB.

1. Solder the C2000 connector to your PCB. Additionally, solder the test points for PWMH, PWML and GND for easier probing.
2. Connect the C2000 connector pins for PWM signals to the corresponding pins on the C2000 using jumper cables.
3. With the microcontroller producing a PWM signal, use an oscilloscope to probe another pad on the PCB that should be receiving the PWM signal or probe the corresponding test point. If the appropriate PWM signal appears, your connections are correct. If the appropriate PWM signal does not appear, identify the error in your connections and repeat.

Note: You should not move on until you confirm your PWM inputs are receiving the correct signals.

input ✓

## Assemble the Gate Circuit

Once your PCB is receiving PWM signals, systematically assemble your gate circuit as follows, **detaching the microcontroller from your PCB anytime you need to solder:**

1. When the PWM signal travels a long distance on the PCB, it is advisable to include an RC filter near the gate driver input to attenuate any noise that may have coupled to the signal. Using the buck converter schematic on bCourses, identify which resistors and capacitors on the PCB correspond to this filter for the high side PWM signal and the low side PWM signal respectively. For each RC filter, solder a  $10\ \Omega$  resistor and a  $330\text{ pF}$  capacitor. ✓ R7 R8 C1 C20 C25, C26 C48~51 C40~C47 C27~C29, C31
2. Solder the gate drive IC, decoupling capacitors, bootstrap circuit, and the 12V and GND banana jack connectors to the PCB. It will also be useful to solder the "GATE HIGH" and "GATE LOW" test points. Once again, refer to the buck converter schematic to confirm the identity of the footprints on the PCB. Be sure to follow the inspection recommendations from Module 0, and use a multimeter to check for short circuits between gate driver pins. It may be useful to solder all the GND banana jack connectors, so you can use them when probing.
3. Connect your DC power supply to the banana jack connectors labeled 12V and GND. Configure your DC power supply to an output voltage of 10 V. Set the current limit to a reasonable value. Do not turn on the supply yet.
4. Reattach the microcontroller and configure it to produce a PWM output. Turn the DC power supply on. Probe the gate driver's low side signal output (pin "LO") to confirm it is producing an appropriate PWM signal; this signal will drive the low side switch's gate. If it does not produce an appropriate PWM signal, troubleshoot the gate drive IC's solder connections.
5. Probe the gate driver's high side signal output (pin "HO"). You will notice that there is no PWM signal. To troubleshoot this, probe the switch node (pin "VS") and then the high side power rail (pin "VB"). *Be sure to inspect these signals with two different probes referenced to ground; measuring the voltage from pin "HO" to pin "VB" with a single ended probe may damage the oscilloscope.* You will notice that there is no

voltage difference between the two signals. This means your bootstrap capacitor, which must charge to power the high side signal output, is not charging. However, since you have not yet installed the switches, this makes sense; the bootstrap capacitor is charged during the part of the cycle when the low side switch is on, shorting the switch node to ground.

6. To test the high side signal output before installing the switches, solder a temporary short circuit between the switch node and ground using a jumper wire. This will allow your bootstrap capacitor to charge and power the high side gate signal.
7. Probe the gate driver's high side signal output to confirm it is producing an appropriate PWM signal. If it does not produce an appropriate PWM signal, troubleshoot the gate drive IC's solder connections.

Check-off: Confirm gate driver is producing appropriate PWM signals. 

After completing this check-off, remove the short circuit you added between the switch node and ground.

## Add Switches, Heat Sinks, and Gate Loop Resistors

Now that you have systematically assembled and verified correct operation of your gate circuit, it's time to add the switches.

1. Before soldering on the switches, add heat sinks to one or both of your switches as designed. First, cut the thermal pad down to an appropriate size for your switch. Then, add the heat sink, and secure it into place with a bolt and nut. The fins of the heatsink should face away from the switch.
2. Solder the switches in place, and use a multimeter to check for short circuits between pins.
3. To test the gate signals, solder a temporary short circuit across the gate resistors (i.e., resistor pads between the gate drive PWM output and switch gates).
4. Reattach the microcontroller and configure it to produce a PWM output. Probe the gate-source of each switch to confirm it is receiving an appropriate PWM signal.

Once you have added switches, it is important to tune the rising and falling edges of the gate signal to find a good compromise between (a) damping problematic ringing caused by parasitics, and (b) ensuring turn on and turn off occur as quickly as possible.

1. Still with shorted gate resistors, probe the gate-source signal and measure the ringing frequency for both the rising and falling edges (assuming the response is underdamped). If there is no ringing (i.e., the response is overdamped), there will be no frequency to measure and there is no need to add additional resistance (as this would further damp the signal).
2. If there is ringing, remove the short and add a gate resistor. Re-probe the gate-source of each switch to view the newly-tuned rising and falling edges of each PWM signal. Repeat this process until the rising and falling responses are close to critically damped. To achieve this, you may have to independently tune the rising and falling edges using separate turn-on and turn-off gate loop paths. Do not overdamp the responses with too much gate resistance.
3. Probe the gate-source signals of both switches, and measure the deadtime. Ensure one switch is fully off before the other switch begins to turn on, with substantial buffer in between.

Check-off: Confirm switches are appropriately installed and gate signals are appropriately tuned. Tell us (a) how much dedicated time you spent on this lab, and (b) if any other student(s) in the lab helped you, and who.

# Post-lab Assignment

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## Lab Results

1. List the gate resistance values you added to each gate loop, if any.
2. Provide screenshots of your appropriately tuned gate signals and dead time.

## Lab Takeaways

1. Describe the most important features you would consider when selecting a gate drive IC and why they matter to your converter design.
2. In your own words, describe how a bootstrap circuit works to power a high side switch.
3. In your own words, describe the role of decoupling capacitors in circuits.
4. In your own words, describe the importance of tuning a gate loop.

## Build Intuition

1. Describe the relationship between the capabilities of a gate driver and switching losses. If a gate driver is capable of sourcing and sinking greater levels of current, what effect (if any) does this have on gate loss, overlap loss, and  $C_{oss}$  loss?
2. Explain the necessity of dead time in gate drive circuits. If a gate driver is capable of sourcing and sinking greater levels of current, what effect does this have on the minimum dead time?
3. Describe the origin of gate drive loss (i.e., why it exists), and the degree to which it should be considered in your converter design. Should it be considered when evaluating switch temperature rise? Should it be considered when evaluating overall converter efficiency? Explain.

## EE 213B

From our provided part library, select switches and heat sinks (if needed) for your converter design. When choosing parts, you are constrained by a cost limit of \$60 for the total board, and there will be opportunity for you to change your part selections later if you find you may exceed \$60. Justify your selections, and provide a loss breakdown for the nominal operating point and all corner operating points considering realistic junction temperatures. Provide the worst-case junction temperature for your switches. You are required to use at least two active switches.

Provide a breakdown of your simulated switch losses, and compare them to your calculated values.

If you would like to propose an additional part for our library, please select the part from an online marketplace (Digikey, Mouser, Amazon, etc.) and a backup part from our library, and include both in your post-lab writeup. Then, write a proposal of approximately 1 page explaining the following:

1. The least-expensive online marketplace to purchase this part, out of major marketplaces (e.g., Digikey, Mouser, Amazon, etc.).
2. The advantage of this part over our current parts and why this advantage justifies its cost.
3. Calculations to back up your arguments.
4. How you've budgeted this part into the total cost of your board so that it doesn't exceed the maximum cost.
5. How this part may be broadly useful to other designs/topologies meeting the same specifications.

Proposals will be reviewed within one week of submission. Students may collaborate on a single proposal for the same part.

### **Assignment Feedback (Required)**

How much dedicated time did you spend on this post-lab?

Now that you have selected your switches, it's time to design the gate drive circuits for S1 and S2. Gate drive circuits commonly employ integrated circuits (ICs), and a plethora of possibilities exists for both the features of these ICs and the circuit architectures enabled by them. This module will focus on how we utilize ICs in gate drive circuits; we will leave the details of how these ICs operate to an analog integrated circuit design class.

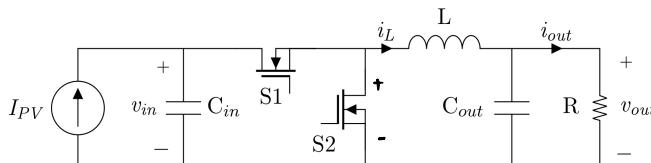


Figure 1: Synchronous buck converter.

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq 5\%$
Output Voltage Ripple	$\leq 5\%$
Inductor Current Ripple	$\leq 20\%$

## Gate Drive Needs and IC Characteristics

For your gate drive circuit you may assume you will use the half-bridge gate driver IC provided in the parts library. This IC has inputs and outputs for driving both the high side and low side devices of a half bridge. In this section you will learn more about the features of this gate driver.

$V_{GS}$

- Based on information provided in the datasheet for your selected switch, choose an appropriate gate-source drive voltage.
- For the specified gate driver, what is the gate drive supply range? Comment on whether or not this is suitable for your intended drive voltage.
- Unlike low side gate drivers, a half-bridge gate driver must be capable of withstanding the *difference* between the supply voltages for the high side and low side switches. While the low side supply voltage is fixed and referenced to ground, the high side supply voltage is floating and referenced to the switch node. For the specified gate driver, what is the maximum high side supply voltage relative to ground? Comment on whether or not this is suitable for the expected range of your converter's switch node voltage plus your drive voltage.
- An important feature of any gate driver is how much current it can source and sink. What are the current source and sink capabilities of the specified gate driver?

### 1. Use IRL3705N-55V-89A.

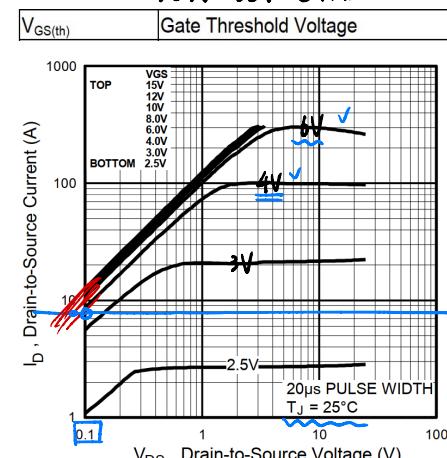


Fig. 1 Typical Output Characteristics

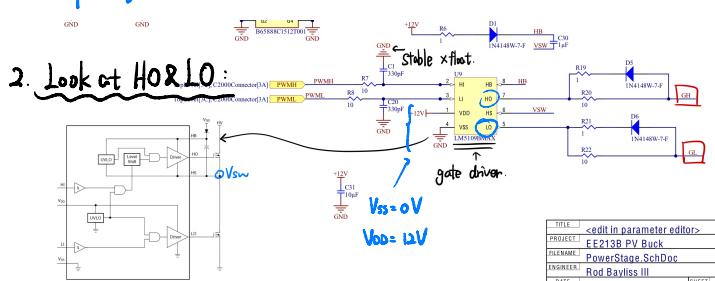
$S_1 \text{ off } S_2 \text{ on: } (V_{DS_1} = V_{in} = 20V)$ ,  $I_{DS_2} = <i_L> = I_{out} = \frac{-P_{out}}{V_{out}} = \frac{-100W}{12V} = \frac{25}{3} A$

$S_2 \text{ off } S_1 \text{ on: } (V_{DS_2} = V_{in} = 20V)$ ,  $I_{DS_1} = <i_L> = \frac{25}{3} A \approx 8.3A$ .

$\Rightarrow$  when  $I_{DS} = 8.3A$ , I need  $V_{GS}$  to be small enough not to affect output

$\Rightarrow$  choose  $V_{GS} = 4V$ . (or  $\geq 6V$ ).

### 2. Look at H<sub>O</sub> & L<sub>O</sub>:



## 6 Specifications

normally,  $V_{SS} \leftrightarrow \text{gnd}$

In startboard,  $V_{SS} = 0V$ ,  $V_{DD} = 12V$ .

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
$V_{DD}$ to $V_{SS}$	-0.3	18	V
HB to HS	-0.3	18	V
LI or HI to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
LO to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
HO to $V_{SS}$	$V_{HS} - 0.3$	$V_{HB} + 0.3$	V
HS to $V_{SS}$ <sup>(2)</sup>	-5	90	V
HB to $V_{SS}$		108	V
Junction temperature	-40	150	°C
Storage temperature, $T_{stg}$	-55	150	°C

$$10 - V_{SS} = 10 \in [-0.3, V_{DD} + 0.3] = [-0.3, 12.3] \text{ V} \leftarrow \text{LO} \quad \left. \right\} 10 \leq V \checkmark$$

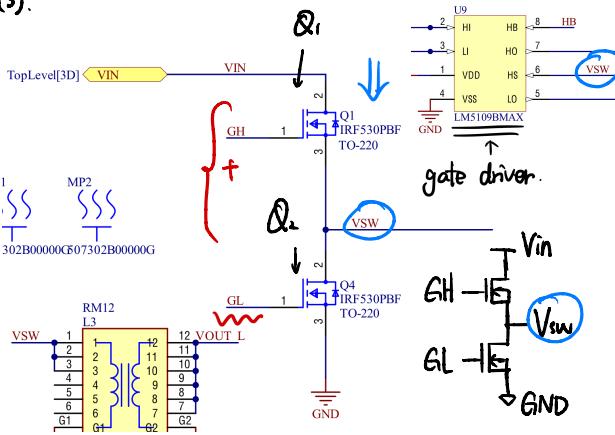
$$HO - V_{SS} = V_{O} \in [V_{HS} - 0.3, V_{HB} + 0.3] = [-5.3 \text{ V}, 108.3 \text{ V}] \leftarrow \text{HO.} \quad \left. \right\} HO \geq 6V \checkmark$$

It's suitable.

3. Unlike low side gate drivers, a half-bridge gate driver must be capable of withstanding the *difference* between the supply voltages for the high side and low side switches. While the low side supply voltage is fixed and referenced to ground, the high side supply voltage is floating and referenced to the switch node. For the specified gate driver, what is the maximum high side supply voltage relative to ground? Comment on whether or not this is suitable for the expected range of your converter's switch node voltage plus your drive voltage.

4. An important feature of any gate driver is how much current it can source and sink. What are the current source and sink capabilities of the specified gate driver?

(3).

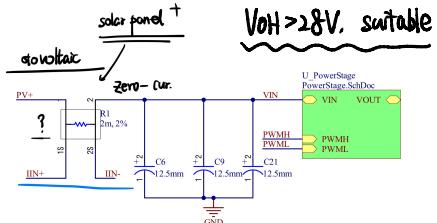


$V_{SW}$  to  $V_{drive}$  range:

suppose:  $Q_1$  - high side,  $Q_2$  - low side

$$\text{For } GH: V_{GH} = V_S + V_{AS} = V_{SW} + V_{AS} = V_{SW} + V_{drive}$$

$$V_{GH \text{ max}} \geq V_{int} + V_{drive} = 20 + 8 = 28 \text{ V.}$$



- (4). source  $\leftrightarrow$  I current into gate  
sink  $\leftrightarrow$  I current out of gate. both are 1.

- 1-A Peak Output Current (1.0-A Sink and 1.0-A Source)

## Overlap Loss

To calculate overlap loss in Module 1, you approximated the rise and fall times for the switch's drain-source voltage, and you assumed overlap loss was only present during hard turn-on transitions. These approximations may or may not reflect your actual design. Given the current source and sink capabilities of your half-bridge gate driver IC,

both 1A.

- Determine which switch transitions have non-negligible overlap loss, and justify your claim. You should consider both turn-on and turn-off transitions.
- For switch transitions with non-negligible overlap loss, calculate the overlap time based on the  $V_{gs}$  vs.  $Q_g$  plot for your switch.
- Recalculate the expected overlap loss for the nominal operating point and the four corner operating points.
- Provide a final breakdown of all losses in your switches at the nominal operating point and the four corner operating points. These calculations should reflect how the change in overlap loss affects the junction temperature, and how a change in junction temperature affects conduction loss.

Note: We didn't require this in Module 1, but a realistic switch selection process must consider these actual rise and fall times (based on the  $V_{gs}$  vs.  $Q_g$  plot) when calculating and comparing overlap loss. Thus, switches are often selected in conjunction with an appropriately sized gate drive IC.

(1). From the conclusion on class,

$$I_g = 1A \quad I_d = <\bar{V}_L> \text{ in buck}$$

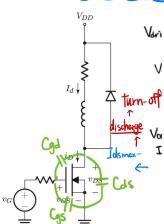
$$= \frac{25}{3} A$$

$$C_{iss} = C_{gst} + C_{gd}$$

$$C_{oss} = C_{gd} + C_{ds}$$

Slowest voltage rise dominates.

$$\Rightarrow \text{Want } \frac{I_g}{C_{gd}} \gg \frac{I_d}{C_{oss}} \text{ for negligible overlap @ turnoff}$$



$V_{DD}$	$V_{in}$	$C_{iss}$	Input Capacitance	—	3600	—	$V_{GS} = 0V$
		$C_{oss}$	Output Capacitance	—	870	—	$V_{DS} = 25V$
		$C_{rss}$	Reverse Transfer Capacitance	—	320	—	$f = 1.0MHz$ , See Fig. 5

$$\Rightarrow \frac{I_g}{C_{gd}} \text{ vs. } \frac{I_d}{C_{oss}} \Leftrightarrow \frac{1A}{320pF} \text{ vs. } \frac{\frac{25}{3}A}{870pF}$$

$$3.125 \times 10^9 \text{ vs. } 9.5785 \times 10^9$$

$\Rightarrow$  s.t. cannot neglect turn-off loss For  $S_1, S_2$ , applying Z305.

Questions.

$V_{GS(m)}$	Gate Threshold Voltage	1.0	2.0	$V$	$V_{DS} = V_{GS}, I_D = 250\mu A$
					Suppose $V_{th} = 1.5V, V_{GS} = 20V$

$\Delta Q_{ov} \approx 40.5 - 35nC$ , suppose rising & falling time are similar

$$t_{ov(\text{con})} = \frac{\Delta Q_{ov}}{I_{source}} = \frac{35nC}{1A} = 3.5 \times 10^{-8}s$$

$$t_{ov(\text{off})} = 3.5 \times 10^{-8}s$$

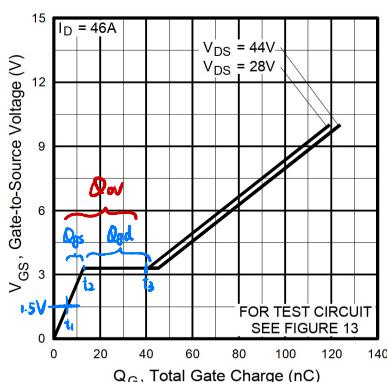


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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Input Voltage Ripple	≤ 5%
Output Voltage Ripple	≤ 5%
Inductor Current Ripple	≤ 20%

$$(3) \quad P_{ov} = P_{ov, on} + P_{ov, off} \approx \frac{1}{2} V_{ds, id} \cdot (t_{ov, on} + t_{ov, off}) \cdot f_{sw}$$

$$= \frac{1}{2} \times 20 \times \frac{25}{3} \times (3.5 \times 2 \times 10^{-8}) \times 10^5$$

① nominal:

$$P_{ov} = \frac{1}{2} \times 20 \times \frac{25}{3} \times (3.5 \times 2 \times 10^{-8}) \times 10^5 \\ = 0.5833 W$$

$$1.1. \quad V_{in, max} = 24V, \quad P_{max} = 100W$$

$$P_{ov} = \frac{1}{2} \times 24 \times \frac{25}{3} \times 7 \times 10^{-8} \times 10^5 \\ = 0.7W$$

$$1.2. \quad V_{in, min} = 16V, \quad P_{max} = 100W$$

$$P_{ov} = \frac{1}{2} \times 16 \times \frac{25}{3} \times 7 \times 10^{-8} \times 10^5 \\ = 0.4667W$$

$$1.3. \quad V_{in, max} = 24V, \quad P_{min} = 50W$$

$$P_{ov} = \frac{1}{2} \times 24 \times \frac{25}{6} \times 7 \times 10^{-8} \times 10^5 \\ = 0.35W$$

$$1.4. \quad V_{in, min} = 16V, \quad P_{min} = 50W$$

$$P_{ov} = \frac{1}{2} \times 16 \times \frac{25}{6} \times 7 \times 10^{-8} \times 10^5 \\ = 0.2333W.$$

4. Provide a final breakdown of all losses in your switches at the nominal operating point and the four corner operating points. These calculations should reflect how the change in overlap loss affects the junction temperature, and how a change in junction temperature affects conduction loss.

Note: We didn't require this in Module 1, but a realistic switch selection process must consider these actual rise and fall times (based on the  $V_{gs}$  vs.  $Q_g$  plot) when calculating and comparing overlap loss. Thus, switches are often selected in conjunction with an appropriately sized gate drive IC.

```
% Circuit parameters % Rds_Iteration_1st
Vin = 20;
Vm_min = 16;
Vm_max = 24;
I_L_max = 12;
P_min = 50;
P_max = 100;
P = P_max;
IL_max = P_max/Vout;
Vm_min = P_min/Vout;
Vm_max = R_th*Vm/Vout;
P_loss_cond1_heatsink = DIL*2*Rds1_noisink;
P_loss_cond2_heatsink = Dbar*IL*2*Rds2_noisink;
Tamb = 25;
Tj1_noisink = Tamb + (P_loss_cond1_noisink * P_loses_coss) * R_th_JA;
Tj2_noisink = Tamb + P_loss_cond2_noisink * R_th_JA;

% Thermal Model: ***
Tj1_heatsink = Tamb + (P_loss_cond1_heatsink + P_loss_ov + P_loss_coss) * R_parallel;
Tj2_heatsink = Tamb + P_loss_cond2_heatsink * R_parallel;
R_parallel = 0.05;
R_th_CS = 0.5;
R_th_SA = 0.22;
R_parallel = R_th_JA * R_th_JC * R_th_CS * R_th_SA;

% Switches parameters -- For IRFZ34Npbf
% Rds_Iteration_1st
Rds1_noisink = Rds * T(Tj1_noisink);
Rds2_noisink = Rds * T(Tj2_noisink);

% Parameters_appendix
Qgd = 14*1e-9;
tov = Qgd/d;
eta_vd = 1;
eta_vd2 = 1;
Ceq_Q = Coss_Q * 1e-12; % from matlab script demo
Rds = 0.94;

% Losses
P_loss_ov = 0.5 * Vin*IL + tov*fsw;
P_loses_coss = Ceq_Q * Vin^2 * fsw;

% nominal condition: Vin Vout P
D = Vout/Vin;
Dbar = 1-D;
P_loss_cond1 = DIL*2*Rds;
P_loss_cond2 = Dbar*IL*2*Rds;

P_loss1 = P_loss_cond1 + P_loss_ov + P_loses_coss;
P_loss2 = P_loss_cond2 + P_loses_coss;

% Junction Temperature
Tj1_noisink = Tamb + P_loses1*R_parallel;
Tj2_noisink = Tamb + P_loses2*R_parallel;
```

```
% Coss_Vs_Vds = @(t) F(t); % Create function based on int
figure
plot(x, Coss_Vs_Vds()); % Plot function to make sure it
title("Coss-Vds curve")
xlabel("VDS (V)")
ylabel("C (PF)")
CossQ = integral(Coss_V, 0, Vdd)/Vdd; % Calculate
vx = .01:.01:Vdd;
Cx = 10.^1*interp1(x,log10(y),vx,"linear","extrap");
E = cumtrapz(vx,Cx.^"vx");
CeqEcum = CeqEcum(2000); % Calculate energy-equivalent
% parameters_appendix: ***
% Qgd = 49*1e-9;
% tov = Qgd/d;
];
x = Data(:,1);
y = Data(:,2));
plot(x,y.^"x);
p = griddedInterpolant(x,y); % Interpolate data points
```

normal:  $P_{loss} = 1.35W$

$V_{in, max}$ , $I_{max}$	$V_{in, min}$ , $P_{min}$
$P_{loss} = 1.46W$	$P_{loss} = 0.95W$

$V_{in, min}$ , $P_{max}$	$V_{in, max}$ , $P_{min}$
$P_{loss} = 1.23W$	$P_{loss} = 0.48W$

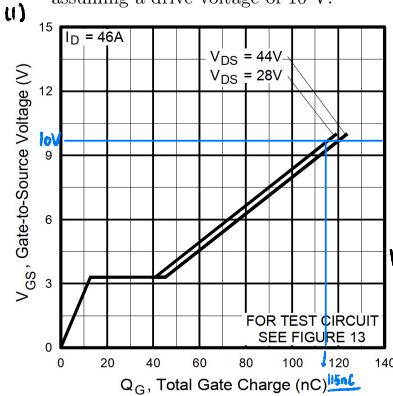
final score:  $e_{ta\_score} = 0.9874$

## Gate Drive Loss

While gate drive loss is dissipated outside of the switch itself, it can be a significant portion of the converter's overall loss. Thus, gate drive loss can also be an important consideration during the switch selection process.

- Assume you have chosen a gate drive voltage of 10 V. Based on the  $V_{gs}$  vs.  $Q_g$  plot provided in your switch's datasheet, estimate the effective gate capacitance for your selected drive voltage. You may approximate the  $V_{gs}$  vs.  $Q_g$  relationship to be linear, based on the actual value of  $Q_g$  at the drive voltage.
- Based on the  $V_{gs}$  vs.  $Q_g$  plot provided in your switch's datasheet, estimate the energy that must be delivered to the gate (i.e., stored in the gate capacitance) to bring the gate-source voltage up to the drive voltage. You may calculate this directly from the  $V_{gs}$  vs.  $Q_g$  or using the effective gate capacitance calculated in the previous question.
- Calculate the total gate drive loss (i.e., the total power loss associated with driving your switches) assuming a drive voltage of 10 V.

what is ② ??



$$Q_G \approx 115 \text{nC} \quad C_G = \frac{Q_G}{V_{GS}} = \frac{115 \text{nC}}{10 \text{V}} = 1.15 \times 10^{-8} \text{F} \approx 115 \text{fF}$$

(2)

$$\begin{aligned} E_{R,loss} &= \int_0^{\infty} V_R i_R dt = \int_0^{\infty} (V_{drive} - V_C) \cdot C \cdot \frac{dV_C}{dt} dt \\ &= \int_0^{V_{drive}} (V_{drive} - V_C) \cdot C \cdot dV_C \quad \underbrace{E_{C,store} = \frac{1}{2} \cdot C \cdot V_{drive}^2}_{\downarrow} \\ C_G &= C \cdot V_{drive} - \frac{1}{2} C \cdot V_{drive}^2 \\ &= \frac{1}{2} C \cdot V_{drive}^2 \end{aligned} \Rightarrow E_{all} = C \cdot V_{drive}^2$$

$$\Rightarrow E_{all} = 115 \text{nC} \times (20)^2 = 4.6 \times 10^{-5} \text{J}$$

(3) - gate drive loss

$\Leftrightarrow$  gate loss + overlap loss +  $C_{oss}$  loss.

$$= E_{all} \cdot f_s + P_{ov} + P_{oss}$$

$$= 4.6 \times 10^{-5} \times 10^5 + 0.5833 + 0.067$$

$$\underline{\underline{= 5.25 \text{W}}}$$

## Bootstrap Circuit Design

Because the gate driver's low side supply voltage is referenced to ground, it can be easily generated from a fixed external supply. By contrast, the high side supply voltage is referenced to the switch node, which changes in voltage throughout the switching cycle. To drive the high side switch, the designer must generate a floating supply referenced to the switch node. This is commonly (and cost-effectively) done using a bootstrap circuit, shown in Fig. 2.

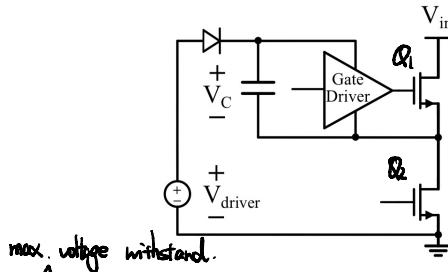
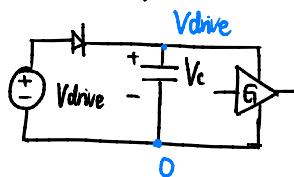


Figure 2: A bootstrap circuit to create a high side supply voltage.

1. Calculate the necessary voltage ratings for a bootstrap capacitor and diode in your design.
2. While the low side switch is on and the switch node is connected to the ground node, the bootstrap diode allows the high side floating supply to charge from the fixed external supply. Accordingly, it is important to select a bootstrap diode that has a low forward voltage drop (so the floating supply can charge as close as possible to the fixed supply voltage) and minimal reverse recovery (so the diode turning off doesn't discharge the floating supply). According to these criteria, select a bootstrap diode from the components provided in the parts library.

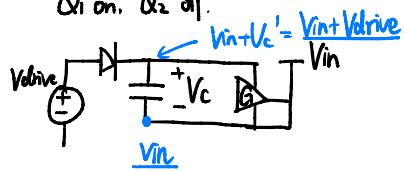
(1)  
Q2 on, Q1 off



$$\text{For C: } V_{c\max} = V_{\text{drive}}$$

$$\text{For diode: } V_d = 0$$

Q1 on, Q2 off.



$$\text{For C: } V_{c\max} = V_{\text{drive}}$$

$$\text{For diode: } V_d = V_{\text{in}}$$

capacitor:  $V_{\text{drive}}$ .

diode:  $V_{\text{in}}$

Select BAV16W/1N4148W

(2).

### Electrical Characteristics (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Max	Unit	Test Condition
Reverse Breakdown Voltage (Note 6)	$V_{(\text{BR})R}$	100	—	V	$I_R = 1.0\mu\text{A}$
Forward Voltage	$V_{FM}$	—	0.715 0.855 1.0 1.25	V	$I_F = 1.0\text{mA}$ $I_F = 10\text{mA}$ $I_F = 50\text{mA}$ $I_F = 150\text{mA}$
Peak Reverse Current (Note 6)	$I_{RM}$	—	1.0 50 30 25	μA μA μA nA	$V_R = 75\text{V}$ $V_R = 75\text{V}, T_J = +150^\circ\text{C}$ $V_R = 25\text{V}, T_J = +150^\circ\text{C}$ $V_R = 20\text{V}$
Total Capacitance	$C_T$	—	2.0	pF	$V_R = 0, f = 1.0\text{MHz}$
Reverse Recovery Time	$t_{RR}$	—	4.0	ns	$I_F = I_R = 10\text{mA}$ , $I_{RR} = 0.1 \times I_R, R_L = 100\Omega$

I only find 1 diode in the library, with  $V_{FM\max} = 1.25\text{V}$

$$t_{reverse} = t_{RR} = 4\text{ns}$$

3. Calculate the effective drive voltage for the high side switch (i.e., what the gate driver actually sees as its supply voltage) considering the bootstrap diode's forward voltage drop. As problem before, choose  $V_{drive} = 10V$
4. To ensure that driving the gate of the high side switch does not deplete the floating high side supply by more than 10%, bootstrap capacitors are commonly sized to have at least 10x more capacitance than the switch's gate. Calculate the minimum bootstrap capacitor size accordingly, and select an appropriate value based on standard capacitor sizes.
5. Considering the charge delivered to drive the switch each cycle, show that your selected capacitance value will prevent the floating high side supply voltage from discharging by more than 10%.
6. A bootstrap resistor is often added in series with the diode to limit its peak current. Size this bootstrap resistor such that the bootstrap diode current is limited to an allowable value based on the diode's maximum ratings. Show that the resulting time constant between the bootstrap capacitor and this resistor is small compared to the switching cycle; otherwise, the presence of this resistor may prevent the bootstrap capacitor from fully charging.  $RC \gg \tau$ ?

(3) No matter Q<sub>1</sub> on or off,

$V_{gate\_driver} = V_{drive}$ , when low-side on,  $V_{eff} = V_{drive} - V_{fD} = 10 - 1.25 = 8.75V$

when high-side on,  $V_{eff} \leq V_{drive}$  due to discharging

$\Rightarrow V_{eff} = 8.75V$ .

(4)

$\frac{V_{m} + V_{drive}}{2} \rightarrow \text{MOS gate.}$

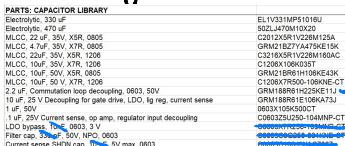
$\Rightarrow \text{make sure } V_{drive} \rightarrow \text{drop } 10\%$

$\Rightarrow C_{boot} \geq 10 C_g = 10 (C_{gdt} + C_{gs})$

$\downarrow$

$C_{boot} \geq 3.6 \times 10^{-8} = 3.6 \text{nF}$

(5) As long as  $C \geq 3.6 \text{nF}$ , it's OK to choose.



$I_{shoot} \leq 1A \Leftrightarrow \frac{V_{drive} - 0}{R_{boot}} \leq 1A \Leftrightarrow R_{boot} \geq 10\Omega$  (to prevent current shooting).  $= 10\mu\text{s}$

$\Leftrightarrow R_{boot} \geq 10\Omega$  (to prevent current shooting).  $= 10\mu\text{s}$

$\frac{1}{RC} \downarrow$

$\text{In RC circuit}$

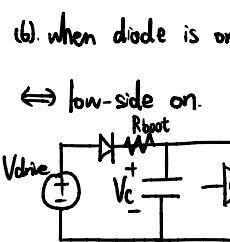
$V_c = V_{dd} + (V_0 - V_{dd}) \cdot e^{-\frac{t}{RC}}$

$= V_{drive} - V_{drive} \cdot e^{-\frac{t}{RC}}$

$= V_{drive} (1 - e^{-\frac{t}{RC}})$

$f = 100\text{Hz}, T_s = 10^{-5}$

$\frac{T_s}{I_s} = 3.6\%$



Maximum Ratings (@ TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Peak Repetitive Reverse Voltage	V <sub>RRM</sub>	100	V
Working Peak Reverse Voltage	V <sub>WRM</sub>		
DC Blocking Voltage	V <sub>R</sub>		
RMS Reverse Voltage	V <sub>r(RMS)</sub>	71	V
Forward Continuous Current	I <sub>FM</sub>	300	mA
Non-Repetitive Peak Forward Surge Current	I <sub>FSM</sub>	2.0 1.0	A
		choose min	

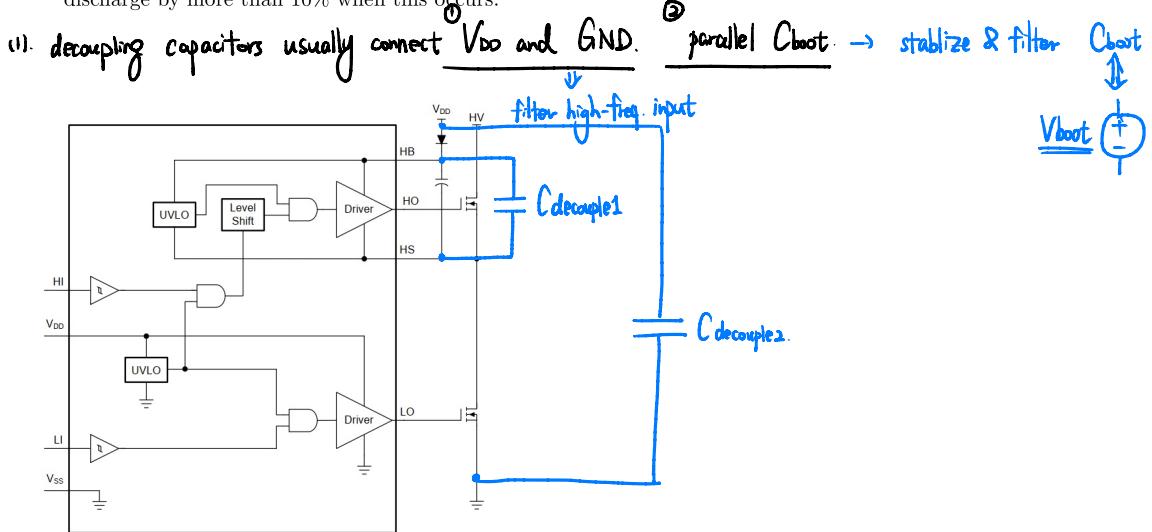
OK!

## Decoupling Capacitors

Decoupling capacitors are important for isolating circuit components and ICs from high-frequency noise generated by other components on the same bus.

1. Based on the specified gate driver's datasheet, describe where decoupling capacitor(s) are needed. Draw a circuit diagram of how you plan to connect these decoupling capacitor(s) to the gate driver IC pins.

2. Size your decoupling capacitor assuming an 0603 MLCC package. It is generally advisable to size decoupling capacitors to have as large capacitance as possible to provide a low-impedance path for high-frequency noise. Show that the decoupling capacitor that will charge the bootstrap capacitor will not discharge by more than 10% when this occurs.



(2) size 0603 MLCC since  $\times$  discharge by 10%.

$$\frac{Q_{out}}{Q_{all}} = \frac{C_{boot}}{C_{decouple}} \leq 10\%$$

$$\Rightarrow C_{decouple} = 10 \cdot C_{boot} = 36 \mu F$$

2.2 uF, Commutation loop decoupling, 0603, 50V

GRM188R61H225KE11J <https://www.digikey.com/en/products/detail/murata-electronics/GRM188R61H225KE11J/4905364>

### 4. Rated value

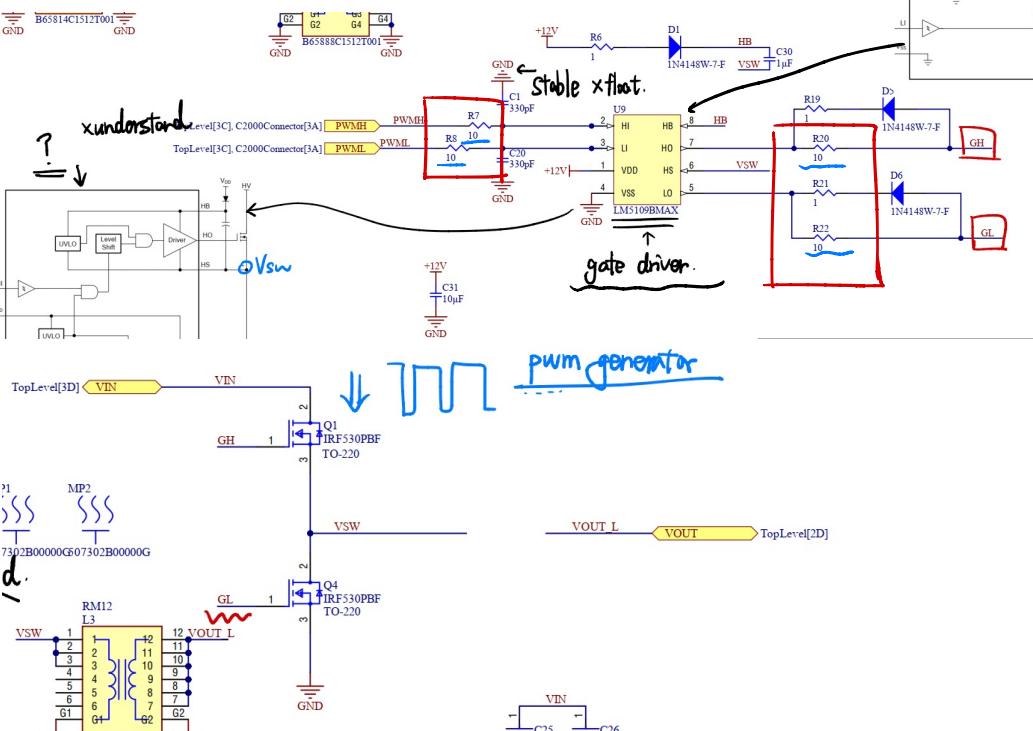
(3) Temperature Characteristics (Public STD Code) XSR(EIA)		(4) Rated Voltage	(5) Nominal Capacitance	(6) Capacitance Tolerance	Specifications and Test Methods (Operating Temp. Range)
Temp. coeff or Cap. Change -15 to 15 %	Temp. Range -55 to 85 °C (25 °C)	DC 50 V	<u>2.2 uF</u>	±10 %	-55 to 85 °C

Feedback: Pre-lab time: ~9h30min

# post-Lab :

## Lab Results

1. List the gate resistance values you added to each gate loop, if any.
2. Provide screenshots of your appropriately tuned gate signals and dead time.



1. For the gate resistor. From C2000 to gate driver. choose Rgate = 10Ω

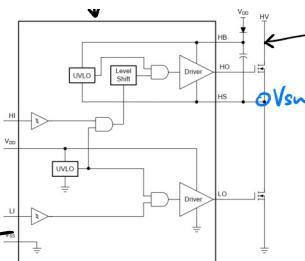
From gate driver to Gth or GL, Rgs, Rg2 = 10Ω, parallel with a reverse diode

2. Screenshots of tuned gate signals and dead time:



← Gate High

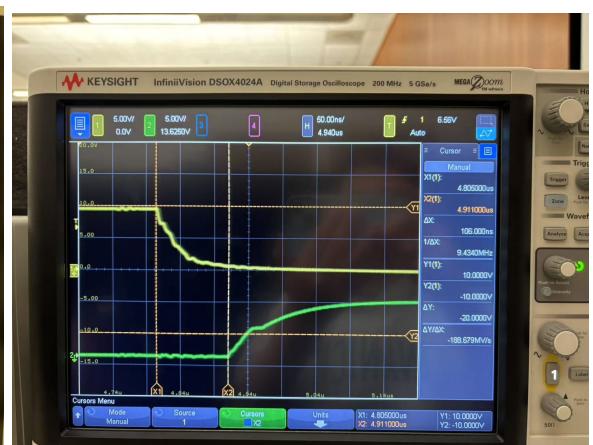
← Gate Low





set rising deadtime  $\approx$  50ns

In C2000, you can set rising and falling time respectively.



falling deadtime  $\approx$  100ns.