Pre-lab Assignment Shikai Shen.

Welcome to EE 113B/213B! Throughout the semester, we will design, prototype, and validate a maximum power point tracking (MPPT) converter for a PV module. To get started, let's assume we plan to use a synchronous buck topology, shown in Fig. 1. Notice the PV module is modeled as a current source. In this first pre-lab, we will size the converter's components. We will also download and install the Code Composer Studio (CCS) integrated development environment (IDE) as well as the C2000Ware software development kit (SDK).

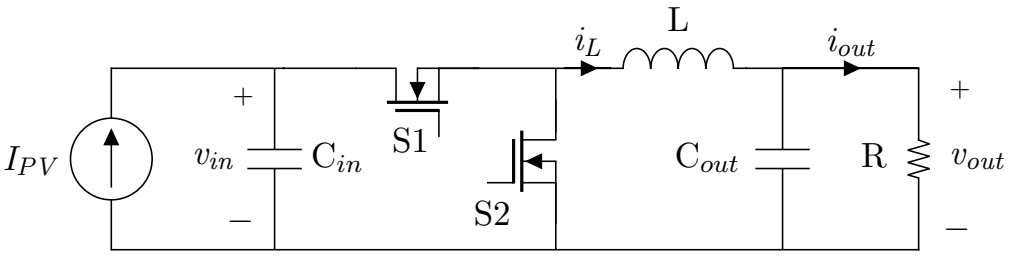

Figure 1: Synchronous buck converter.

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq$ 5 %
Output Voltage Ripple	$\leq$ 5 %
Inductor Current Ripple	$\leq$ 20 %

Size Components

Assume your buck converter has the specifications shown in Table 1. For all of the following calculations, you may assume deadtime is negligible. Hint: You are encouraged to write a script for these sizing calculations in case you change your design later.

1. Calculate the duty cycles required for the nominal operating point and all four corner operating points (i.e., all four combinations of highest load, lowest load, highest input voltage, and lowest input voltage).
2. Assuming a peak-to-peak inductor current ripple of no more than 20% at full power, calculate the minimum inductance required for L.
3. Assuming a peak-to-peak output voltage ripple of no more than 5% for any operating point, calculate the minimum capacitance required for C_{out}.
4. Assuming a peak-to-peak input voltage ripple of no more than 5% for any operating point, calculate the minimum capacitance required for C_{in}.
5. Calculate the maximum voltage and current stress for each switch (i.e., each power transistor).
6. How would choosing a higher switching frequency affect your answers for questions 1-5? Explain.

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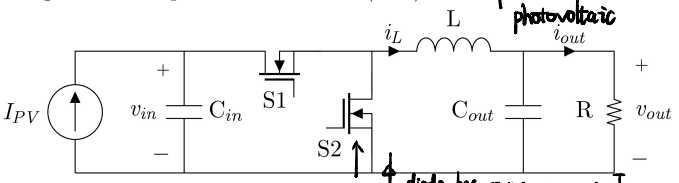

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Specification	Value
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Output Voltage	12 V
Nominal Output Power	100 W
Output Power	50-100 W load
Switching Frequency	100 kHz
Input Voltage Ripple	≤ 5 %
Output Voltage Ripple	≤ 5 %
Inductor Current Ripple	≤ 20 %

① ⇐⇒

Size Components

$T_s = \frac{1}{f_s} = 10^{-5}\,s$

Assume your buck converter has the specifications shown in Table 1. For all of the following calculations, you may assume deadtime is negligible. Hint: You are encouraged to write a script for these sizing calculations in case you change your design later.

1. Calculate the duty cycles required for the nominal operating point (24V) and all four corner operating points (16V) (i.e., all four combinations of highest load, lowest load, highest input voltage, and lowest input voltage).
2. Assuming a peak-to-peak inductor current ripple of no more than 20% at full power, calculate the minimum inductance required for L.

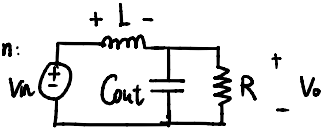
For Buck Converter, $V_{out} = D \cdot V_{in}$.

1. Nominal operating point:

$V_{in} = 20V$, $P_{out} = 100W$, $V_{out} = 12V$, $D = 0.6$

2. $\frac{di_L}{dt} = \frac{V_L}{L}$

S_1 on:

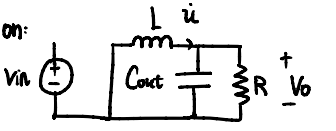


1.2 highest V_{in}, highest load ⇐⇒ P_{max}

⇒ $V_{in} = 24V$, $P_{max} = 100W$, $V_{out} = 12V$.

⇒ $D = 0.5$

S_2 on:



$\langle v_L \rangle = D \cdot (V_{in} - V_o) + D' \cdot (-V_o) = 0$

$\langle i_L \rangle = \cdots = 0$

⇒ $\langle i_L \rangle = I_L = \frac{V_o}{R}$.

1.3 highest V_{in}, lowest load ⇐⇒ P_{min}

⇒ $V_{in} = 24V$, $P_{min} = 50W$, $V_{out} = 12V$.

⇒ $D = 0.5$

$2\Delta i_L = \Delta i_{L,pp} = \left| \frac{V_L}{L} \cdot DT_s \right| = \left| \frac{V_o - V_{in}}{L} \cdot DT_s \right|$

$\Delta i_{L,pp} \le i_L \cdot 20\%$, $\Rightarrow \left| \frac{V_o - V_{in}}{L} \cdot DT_s \right| \le \frac{V_o}{R} \cdot 20\%$

$\Rightarrow L \ge \frac{5(V_{in} - V_o) \cdot DT_s}{V_o} \cdot R$, $R = \frac{V_o^2}{P}$

$\Rightarrow L \ge \frac{5(V_{in} - V_o) \cdot DT_s \cdot V_o}{P}$

1.4 lowest V_{in}, highest load ⇐⇒ P_{max}

⇒ $V_{in} = 16V$, $P_{max} = 100W$, $V_{out} = 12V$

⇒ $D = 0.75$

max

when $D = 0.5$, $L \ge \frac{5(24-12) \times 0.5 \times 10^{-5} \times 12}{50} = 3.6 \times 10^{-5}\,H$

1.5 lowest V_{in}, lowest load ⇐⇒ P_{min}

⇒ $V_{in} = 16V$, $P_{min} = 50W$, $V_{out} = 12V$, $D = 0.75$

3. Assuming a peak-to-peak output voltage ripple of no more than 5% for any operating point, calculate the minimum capacitance required for C_{out}. $2\Delta V_c \le 5\%$

4. Assuming a peak-to-peak input voltage ripple of no more than 5% for any operating point, calculate the minimum capacitance required for C_{in}.

5. Calculate the maximum voltage and current stress for each switch (i.e., each power transistor).

6. How would choosing a higher switching frequency affect your answers for questions 1-5? Explain.

3. $\frac{dV_c}{dt} = \frac{i_c}{C}$, $I_c = I_L - \frac{V_o}{R}$, $\Rightarrow \Delta i_c = \Delta i_L$ (neglect V_c).

$q = C \cdot 2\Delta V_c = \frac{1}{2} \cdot \frac{1}{2} T_s \cdot \Delta i_L$

$\Rightarrow \Delta V_c = \frac{T_s \cdot \Delta i_L}{8C}$, $\left(\Delta i_L = \left|\frac{V_o - V_{in}}{2L} \cdot D T_s\right|\right)$, $2\Delta i_L = 20\% I_L \Rightarrow 2\Delta i_L = 20\% \times \frac{100}{12}$ or $20\% \times \frac{50}{12}$

$= \frac{5}{3}$ or $\frac{5}{6}$

$\Rightarrow 2\Delta V_c \le V_c \cdot 5\% = V_o \cdot 5\% = 12 \times 5\% = 0.6V$

$\Rightarrow \frac{T_s \cdot \Delta i_L}{8C} \le 0.3V$

$\Rightarrow C \ge \frac{10^{-5} \times \frac{5}{6}}{8 \times 0.3} = 3.47 \mu F$

4. $\frac{dV_c}{dt} = \frac{i_c}{C}$, from KCL for small ripples: * $\Delta i_c = D \cdot \Delta i_L$ (on-state)

$\Rightarrow \Delta V_c = \frac{I_c}{C} \cdot T_s$, $\Delta V_c \le \frac{5\%}{2} \times V_c = 0.3V$

$\Rightarrow$ To simplify calculation

$\frac{I_c}{C} \cdot T_s \le 0.3$

$\Rightarrow C \ge \frac{D \cdot \Delta i_L \cdot T_s}{0.3} = \frac{0.75 \times \frac{5}{3} \times 10^{-5}}{0.3} \approx 4.17 \times 10^{-5} F.$

5. Q1: $V_{stress, Q_1} = V_{in} + \Delta V_{in} = (1+2.5\%) \times V_{in} = 24.6V$

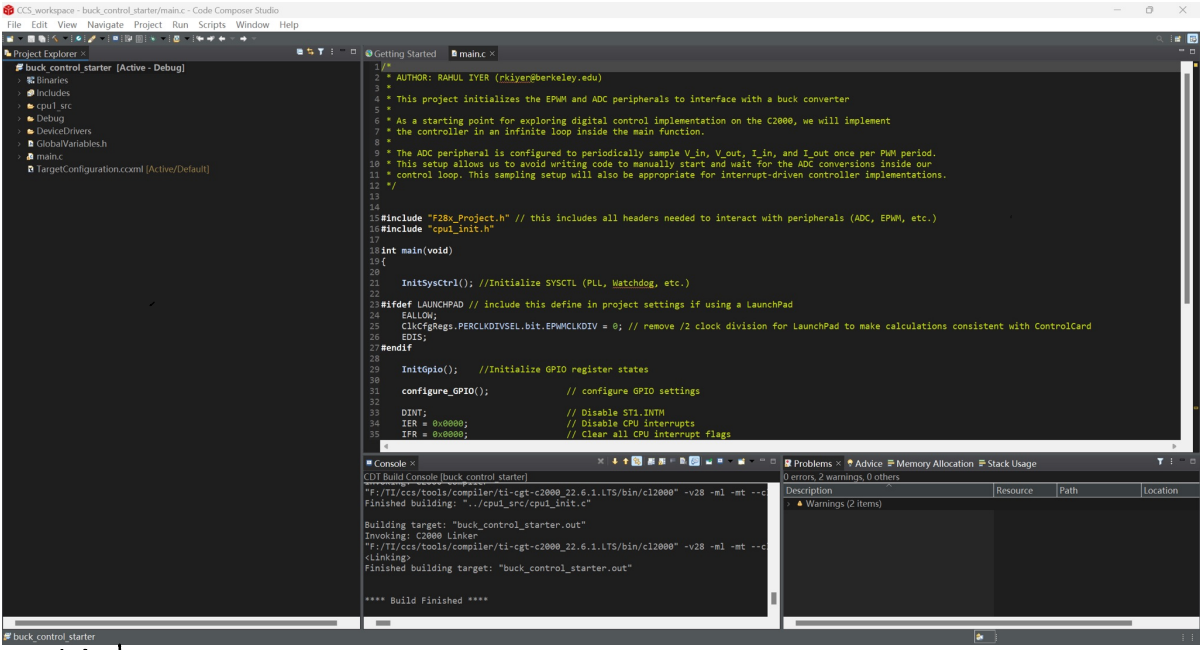
$I_{stress, Q_1} = i_L + \Delta i_L = (1+10\%) \times I_L = 9.17A$

Q2: $V_{stress, Q_2} = 24.6V$

$I_{stress, Q_2} = 9.17A$

6. when $f \uparrow$, $T_s \downarrow$, $\Rightarrow$ current/voltage ripples $\downarrow$,

To maintain the same ripples, smaller L, C are better choices.



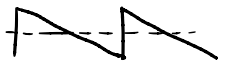
build finish.

Digital PWM Calculations

Now calculate the following, referencing the EPWM section of the technical reference manual as needed. You may assume $f_{\text{EPWMCLK}} = 100\,\text{MHz}$ and $f_{\text{sw}} = 100\,\text{kHz}$.

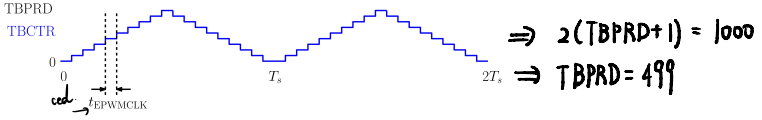
1. Number of EPWMCLK counts per switching period
2. For a leading-edge carrier, calculate the value of TBPRD. Explain your reasoning.
3. For a trailing-edge carrier, calculate the value of TBPRD.
4. For a triangular carrier, calculate the value of TBPRD. Explain your reasoning. (**Hint: the calculation for a triangular carrier is different from that for a sawtooth carrier**).

1. counts per switching period = $\frac{f_{\text{EPWMCLK}}}{f_{\text{sw}}} = \frac{100\text{MHz}}{100\text{kHz}} = 1000$

2. leading-edge: 
counts = 1000 = TBPRD+1
$\Rightarrow$ TBPRD = 999

3. trailing edge: 
$\Rightarrow$ TBPRD = 999

4. triangular edge 
TBPRD is actually achieved by counter and register,
st. 0 → TBPRD → TBPRD → 0
$\Rightarrow$ 2(TBPRD+1) = 1000
$\Rightarrow$ TBPRD = 499



5. In **GlobalVariables.h** update the value of the preprocessor definition `#define EPWM_TBPRD` with the value you calculated in step 4 (we are using a triangular carrier)

6. We want to initialize our code to start PWMs with 50% duty ratio. Update the value of `#define EPWM_CMP_INIT` accordingly (We are using a triangular carrier).

7. Draw the carrier, modulating waveform, and resulting duty switching signal corresponding to our initial duty ratio.

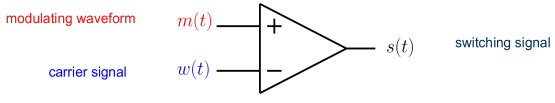
8. Assume we want 50 nanoseconds of deadtime. Calculate the number of EPWMCLK ticks that elapse in 50 nanoseconds. Update the value of `#define EPWM_DEADTIME` with the value you calculated.

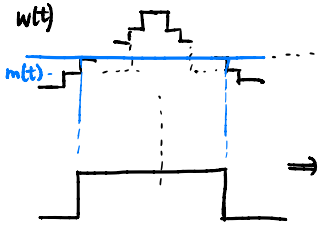
5. ✓

6. TBPRD.
0 ---- we need $\frac{TBPRD+1}{2}$ counts.

$\Rightarrow$ CMP = $\frac{TBPRD-1}{2} = \frac{498}{2} = 249$.

7.





CMP ~ TBPRD.

$\Rightarrow D = \frac{2(TBPRD-CMP+1)}{2(TBPRD+1)} = \frac{TBPRD-CMP+1}{TBPRD+1}$

8. 50ns deadtime.

$EPWM\_DEADTIME = \frac{50ns}{t_{EPWMCLK}} = \frac{50ns}{\frac{1}{100MHz}} = 5$

Getting Started | main.c | GlobalVariables.h ×

```
1 #ifndef GLOBALVARIABLES_H_
2 #define GLOBALVARIABLES_H_
3
4 #define EPWM_TBPRD 499
5
6 #define EPWM_CMP_INIT 249       // initialize with 50% duty ratio
7 #define EPWM_DEADTIME 5                   // deadtime in EPWMCLK ticks
8
9 #define ADC_ACQ_WINDOW 30                 // ADC S&H Window Length in SYSCLK cycles
10
11
12 #endif /* GLOBALVARIABLES_H_ */
13
```

9. Maybe ≈ 3.5 hours - 4 hours (include some review of EE113).