Lab Results:

2. Provide your simulation-based loss estimates for your switches, including a breakdown of loss types, and discuss how they compare with your calculations from the pre-lab. Discuss any discrepancies, any neglected losses, and whether or not neglecting these losses is valid.

Breakdown of loss types:
Conduction loss + switching losses (overlap and output capacitance losses) + body diode losses + reverse recovery losses…

Conduction loss is very close to hand calculations in pre-lab, since P = I^2R.
Switching loss differs from hand calculation because of some parasitics that are not taken into account. (including overlapping losses, body diode, reverse recovery, ESR…)

Lab Takeaways:

1. In your own words, describe how to choose power FETs for a converter design.

First, the voltage and current ratings. They are the maximum voltage and current that the switch can stand. To be mentioned, you have to choose at what frequency the circuit operates.
Then, some parasitic parameters like Rds_on, which determines the conduction loss; Q_gd, determining the overlapping time and the overlapping loss; Coss(Cds+Cgd), determining the Coss loss. These parameters determine the power losses.
Also, the thermal modeling parameters of the switches, you have to estimate the power losses and thermal models of the switches to determine whether it operates correctly.
Finally, use simulation to verify what you have just designed.

2. In your own words, describe how to analyze and manage the heat transfer of power devices

When analyzing and managing heat transfer for power devices, start by estimating the total power losses—both conduction and switching—that the device will experience under normal and worst-case operating conditions. Represent the device and its environment using a thermal equivalent circuit, where each element (the chip, package, heat sink, and PCB) has a thermal resistance and capacity. From there, calculate the expected junction temperature based on power dissipation and thermal resistances in the heat path. If the resulting temperature exceeds safe limits, adjust your design by lowering power losses (using devices with lower on-resistance or optimizing switching) or improving heat dissipation (adding larger heat sinks, thermal pads, or forced-air cooling). Continuous monitoring and refinement—such as evaluating airflow, ambient temperature variations, and contact resistance—help ensure your power device operates reliably within its thermal limits.

3. In your own words, describe how to model switch parastics in PLECS, and the degree to which this model reflects the true behavior of a power FET. Describe any limitations to the model.

In PLECS, you typically model the parasitic effects of a power FET by adding or adjusting parameters in the built-in switch component or by creating a more detailed equivalent circuit. For instance, you might specify an on-state resistance RDS(on) to capture conduction losses, along with junction capacitances (e.g. Cgs, Cgd, Cds) to represent switching behavior. If the switch component has a built-in body diode, you can also include its forward voltage drop and reverse recovery characteristics. In more advanced setups, you can insert small inductances in series with the drain, source, or gate to emulate lead or PCB trace inductances, and sometimes even link the device's thermal profile to account for temperature-dependent losses. Limitations: thermal model may not be accurate(I haven't used thermal resistivity in PLECS).

4. In your own words, describe how to measure switch losses (due to conduction and switching) in PLECS.

Switching loss cannot be directly shown in PLECS, you have to calculate P_sw by P_total – P_cond, and P_cond can be calculated and simulated by I_rms of the switches.

5. Describe your strategy for conducting an optimal part search on Digikey, and at least one pitfall to watch out for.

I have not done marketing in Lab1 quite much, but the strategy depends on your need. For low-frequency circuit, Rds_on is the crucial factor on the loss; for high-frequency circuit, switching loss including Q_gd, Coss are leading factor on the loss. Pitfall: ~.

Build Intuition:

1. Tradeoffs of Selecting a Switching Frequency

Choosing a switching frequency involves balancing component size against switching losses. A higher frequency allows you to shrink the inductor and capacitors (because energy is transferred more often, so less energy storage per cycle is needed). However, each switching event incurs a loss, and switching more frequently increases total switching losses. Conversely, a lower frequency reduces switching losses but requires larger, heavier, and often more expensive inductors and capacitors to maintain the same ripple. If you were to double the switching frequency in your design (while keeping the same current and voltage ripple targets), your passive components could become roughly half as large (in terms of inductance and capacitance needed), but your switches would experience more frequent transitions, generally resulting in higher switching losses.

2. Tradeoffs of Choosing a Maximum Inductor Current Ripple

Allowing a larger inductor current ripple means you can use a smaller inductance value for the

same switching frequency. A smaller inductor is cheaper, lighter, and often has lower series resistance, but the higher current ripple increases the RMS current through the switches, raising conduction losses. If you want to keep the same output voltage ripple (i.e., the same ripple on the capacitor), a larger current ripple usually demands a larger output capacitor to smooth out that higher ripple current. In short, more current ripple ⇒ smaller inductor ⇒ potential for higher conduction losses ⇒ and possibly larger output capacitor (to maintain the same voltage ripple specification).

3. Describe the general relationship between a power FET's die size (i.e., area) and its Rds,on and Coss, assuming the same voltage rating. Generally speaking, how would the Rds,on and Coss of a smaller transistor compare to those of a larger one? How would the distribution of switch losses compare?

For a given voltage rating, a larger FET die area typically yields a lower RDS(on) (reducing conduction losses) but a higher parasitic output capacitance Coss. In contrast, a smaller die has higher on-resistance (increasing conduction losses) but lower Coss (potentially lowering switching losses). As a result, bigger devices are often chosen when conduction losses dominate (e.g., low-voltage, high-current applications), while smaller devices might be preferred if switching losses are the primary concern (e.g., high-frequency operation or lower current). The distribution of losses tilts more toward conduction losses for larger transistors and more toward switching losses for smaller ones.

4. Relationship Between a Power FET's Voltage Rating and RDS(on) (Same Die Size)

Higher-voltage MOSFETs require a thicker, more robust structure to withstand larger voltages, which generally increases their on-resistance for a given die area. In other words, if you keep the same die size but increase the voltage rating, the device's RDS(on) will typically rise, leading to higher conduction losses under the same current conditions. This is why it's common to see specialized low-voltage MOSFET families with extremely low on-resistance, while higher-voltage devices of the same physical size inherently have higher RDS(on) .