

Lab:

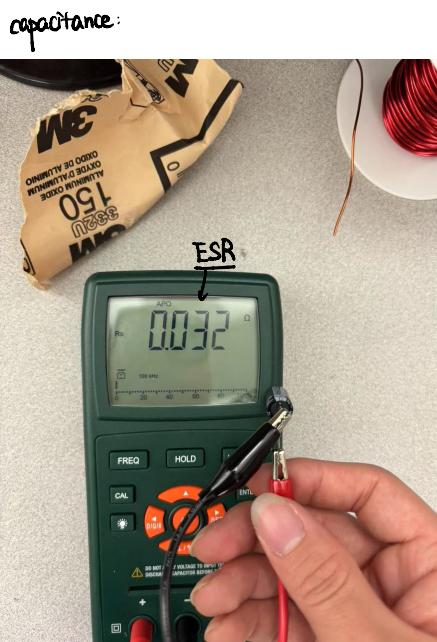
LCR Meter

Now that you have built your inductor, characterize it using an LCR meter as follows:

39.1 uH read

36uF

1. Measure your inductor's inductance at low frequency, and compare it to your design value. If your inductance measurement is significantly off, double check your inductance calculation and your shim stock thickness. The acceptable range for your characterized inductance is 100-110% the minimum value needed to meet the ripple specifications.
2. Measure your inductor's equivalent series resistance (ESR), and compare it to your design value.
3. Measure your inductor's inductance and ESR at 100 kHz, and compare these values to your low-frequency measurements.



During Module 1, you simulated your buck converter considering only switch parasitics. Now, update the inductance and capacitances to their characterized values (i.e., your characterized inductance and capacitance for the inductor and the electrolytic capacitor, respectively, and the manufacturer-provided capacitance of any MLCCs considering derating). Then, add parasitics (i.e., ESR) to each component as characterized at the appropriate frequency. Note: If you use several identical capacitors in parallel, you may combine their impedances in parallel (considering each to be an R-C branch) to form a single R-C branch.

Simulate your converter with both switch and passive component nonidealities, and determine the following for the nominal operating point and each corner operating point:

③ C_{in} not enough. ② datasheet.

1. The efficiency of your power converter. Compare this to the efficiency you measured in Module 1 considering only switch parasitics.
2. The power loss incurred by each of the passives, estimated via simulation. Compare this to the expected loss you calculated in the previous section.
3. The maximum ripples on i_L , v_{in} , and v_{out} .
4. The rms current through any electrolytic capacitors.

characterized values: $C: 100\text{Hz} = 0.032\Omega \text{ ESR}$
 $422.3\mu\text{F}$

$100\text{kHz} = 8.18\mu\text{F}$
 0.036Ω

$L: 100\text{Hz} = 38\mu\text{H}$
 $0.01\Omega \text{ ESR}$ ✓

$100\text{kHz} = 3846\text{H}$
 0.385Ω

We know that $\Delta i_L = 20\% i_L$ at nominal point.

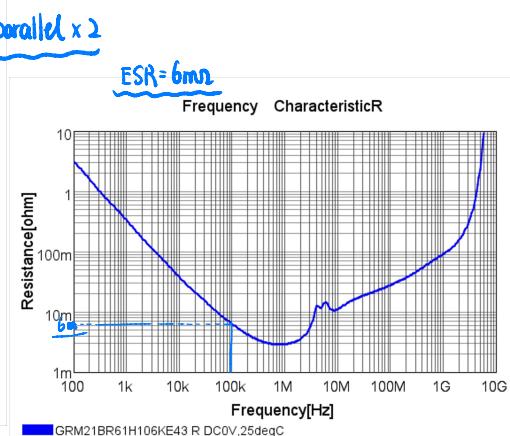
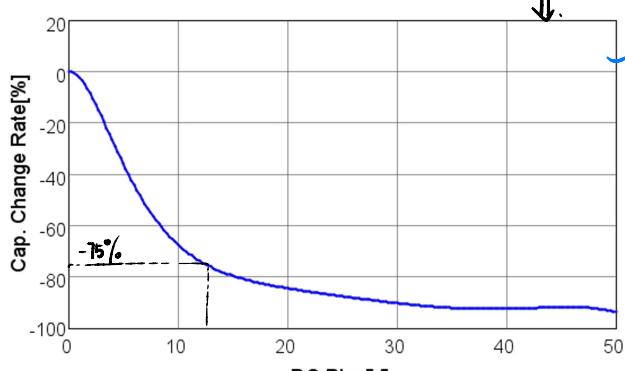
$$\Delta i_L = 20\% \times \frac{100}{12} = \frac{20}{12} = \frac{5}{3} \text{ A} \quad \underline{\underline{I_L = \frac{100}{12} = \frac{25}{3} \text{ A}}}$$

$$\underline{\Delta i_C \approx \Delta i_L = \frac{5}{3} \text{ A (peak-to-peak)}}.$$

$$\Delta i_C \text{ RMS} = \frac{5}{6} \cdot \frac{1}{\sqrt{2}} = \frac{5}{6\sqrt{2}} \text{ (A)}$$

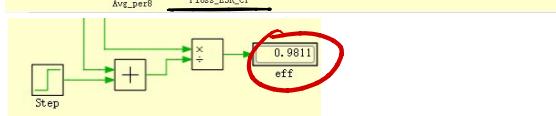
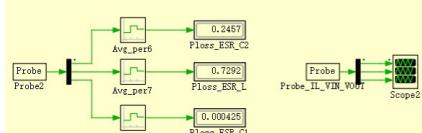
GRM21BR6 - DC bias characteristics

$$C \approx (1-75\%) \times 10\mu\text{F} = 2.5\mu\text{F}$$



- The efficiency of your power converter. Compare this to the efficiency you measured in Module 1 considering only switch parasitics.
- The power loss incurred by each of the passives, estimated via simulation. Compare this to the expected loss you calculated in the previous section.
- The maximum ripples on i_L , v_{in} , and v_{out} .
- The rms current through any electrolytic capacitors.

(2)



switching loss in Module 1

$$\text{For the loss: } P_{cin} = I_{rms}^2 \cdot ESR_{cin}$$

$$= \Delta U \cdot \frac{1}{\sqrt{2}} \cdot \frac{1}{D} \cdot ESR_{cin}$$

$$= \frac{5}{3} \times \frac{1}{\sqrt{2}} \times \frac{1}{0.6} \times 0.036$$

$$\xrightarrow{\text{parallelled} \times 3} \approx 0.0707$$

$$\underline{P_{cin-3} = 3 \cdot P_{cin} = 0.2121.} \quad \xrightarrow{\text{by hand}} \underline{0.2457} \quad \xrightarrow{\text{by simulation}}$$

higher because of ripples.

$$P_{cout} = \Delta U \cdot \frac{1}{\sqrt{2}} \times ESR_{cout}$$

$$= \frac{5}{3} \times \frac{1}{\sqrt{2}} \times 0.006$$

$$= 0.0071$$

$$P_{cout-2} = 2P_{cout} = 0.0142. \quad \underline{0.004} \quad \text{simulation.}$$

higher because ignore C ripples.

$$P_L = I_{rms}^2 \cdot ESR_L$$

$$= (\frac{100}{12})^2 \times 0.01$$

$$\approx 0.6944 \quad \xleftarrow{\text{by hand}}$$

$$= \underline{0.7292} \quad \xleftarrow{\text{by simulation}}$$

Efficiency: $P = 100W \quad V_{in} = 16V \quad 98.14\%$

$P = 100W \quad V_{in} = 24V \quad 98.10\%$

$P = 50W \quad V_{in} = 16V \quad 98.87\%$

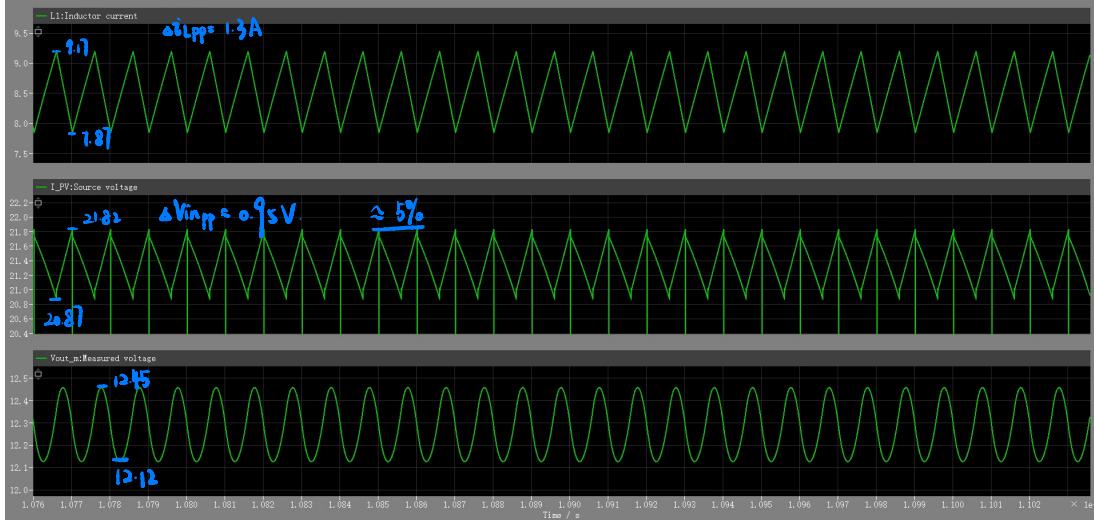
$P = 50W \quad V_{in} = 24V \quad 98.82\%$

(3)

why strikes?

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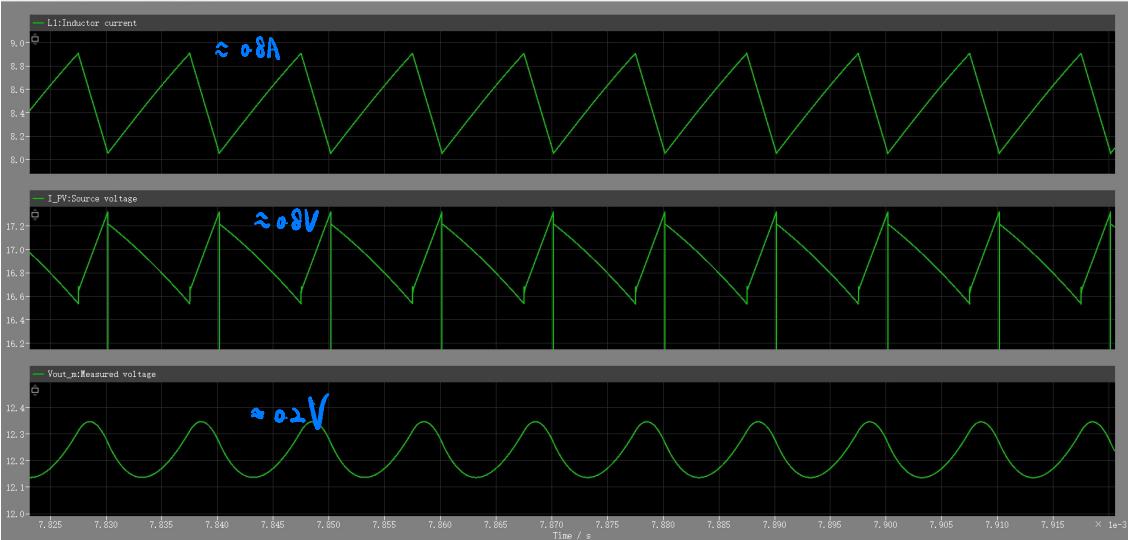
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$$P = 100W, V_{in} = 16V$$

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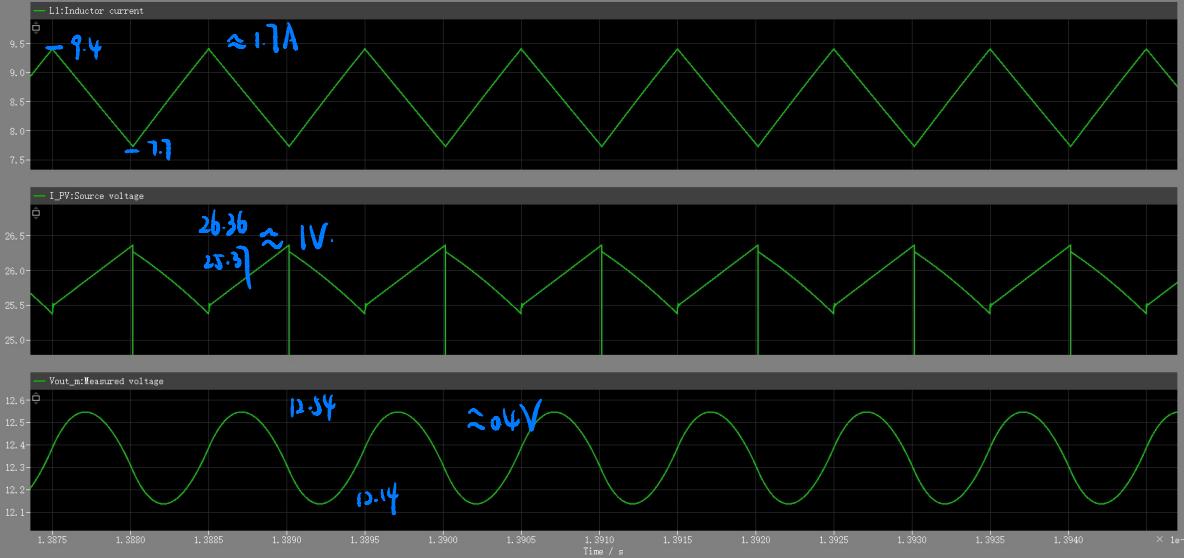
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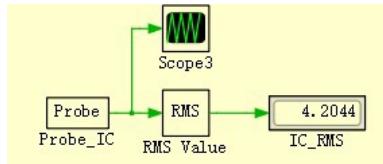
$$P=100W, V_{in}=24V \cdot (\text{worst-case})$$

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4).



Lab3

Lab Results:

Simulation-based loss and hand-calculated loss analysis:

I have put my hand-calculation of my calculation in the PDF before. For the power loss of by simulation (passive components):

C_{in} , by simulation: 0.2457W; by hand: 0.2121. Hand calculation is larger than simulation, which is probably because we neglect ripples when calculating by hand, only DC-bias is calculated.

L : by simulation: 0.7292W; by hand: 0.6944. The same reason as C_{in} , hand calculation ignores ripples, such that the loss by hand calculation is smaller.

C_{out} , by simulation: 0.00425W, which is very small; by hand: 0.0142. Probably because the ripples is much smaller than what we have estimated because the paralleled ceramic capacitors have static capacitance in high-frequency, which leads to smaller ripples and less loss.

Lab Takeaways:

1. In your own words, describe how to choose a magnetic material.

When choosing material, we should first classify the circuit we are building. If low-frequency, we should choose ferrous alloys with high saturation flux density but lossy in high-frequency. If high-frequency, we should choose ferrites with higher efficiency in high frequency but low saturation flux density. In low-frequency, we should consider B_{sat} as the constraint; in high-frequency, we should consider P_v as the constraint.

2. In your own words, describe the design process for a filter inductor (given a magnetic material)

Inductor losses include winding loss (copper loss) and core loss (hysteresis loss and eddy current loss). For low frequency, we use Kg method to choose core type and core size; for high-frequency, we use “AcWa” method to choose.

3. In your own words, describe how to select electrolytic capacitors.

At the source side, we should normally choose electrolytic capacitor for its high-capacitance value. At load side, we should normally choose ceramic capacitor for its stable capacitance at high frequency.

4. In your own words, describe how to select multilayer ceramic capacitors.

To select a multilayer ceramic capacitor (MLCC), first determine the required capacitance value and tolerance based on your circuit's needs. Ensure the voltage rating is at least 1.5x the operating voltage and choose a dielectric type (e.g., C0G/NP0 for stability, X7R for general use, or Y5V for high capacitance but lower stability) suitable for your temperature range. Select the appropriate physical size (e.g., 0402, 0603) to fit space constraints, and consider ESR/ESL for high-frequency applications. Check for quality factors like high Q or low dissipation for efficiency, account for aging effects in Class II/III dielectrics, and ensure the part meets reliability standards for your application. Finally, balance cost, availability, and manufacturer specifications to finalize your choice.

5. In your own words, describe why frequency matters when characterizing a passive component, and how a designer should choose which frequency to use.

Frequency matters when characterizing a passive component because its behavior changes with frequency due to parasitic effects, reactance, and resonance. Components like capacitors and inductors exhibit frequency-dependent impedance, while real-world parasitics (e.g., capacitance in inductors or inductance in capacitors) can dominate performance at high frequencies. Designers choose characterization frequencies based on the operating frequency of the circuit, critical performance points like resonance, and industry standards. This ensures the component performs predictably in the intended application and accounts for real-world factors like energy losses (e.g., ESR) or deviations from ideal behavior, ensuring reliable and efficient circuit design.

Build Intuition:

1. Describe how to determine whether or not core loss may be considered negligible when designing a magnetic component. If your inductor had been sized such that your buck converter operated in DCM, would the expected core loss be greater or less than the value you calculated in the pre-lab? If you were designing an ac transformer (i.e., a transformer intended to handle primarily ac waveform content), could you have neglected core loss?

Core loss in a magnetic component can be considered negligible if the operating frequency and flux density are low, as core loss increases with both factors. To determine this, compare the estimated core loss (using the Steinmetz equation or datasheet data) to other losses like copper loss; if core loss is significantly smaller, it can be ignored. For a buck converter

operating in discontinuous conduction mode (DCM), the core loss would typically be less than in continuous conduction mode (CCM), as the inductor experiences smaller flux density variations and spends less time at high flux levels. However, for an AC transformer designed to handle primarily AC waveform content, core loss cannot be neglected, as the alternating magnetic field induces substantial hysteresis and eddy current losses that are critical to the design and efficiency of the transformer.

2. The Kg method, while very useful, has its limitations. Describe at least one aspect of magnetics design that the Kg method neglects, and how you should design magnetic components if that aspect is relevant to your design.

The **Kg method** simplifies magnetic design by focusing on optimizing the core geometry for minimizing copper and core losses, but it neglects other critical factors such as **core saturation, thermal problems and nonlinear effects of the magnetic material**. Core saturation occurs when the magnetic flux density exceeds the material's saturation point, leading to a rapid loss of inductance and potential circuit failure. If core saturation is a concern, the design must ensure that the peak flux density remains below the core material's saturation limit, even under worst-case operating conditions. Additionally, the Kg method doesn't account for high-frequency effects like eddy current losses in the windings or skin and proximity effects, which become significant in high-frequency designs. To address these, you should carefully select core materials with high-frequency performance and use techniques like litz wire for windings or design with distributed air gaps to mitigate losses and prevent saturation.

3. Describe when electrolytic capacitors are more useful than multilayer ceramic capacitors, and the same vice versa. When should a designer choose one over the other?

Electrolytic capacitors are more useful than multilayer ceramic capacitors (MLCCs) when high capacitance values are required, especially in bulk energy storage or filtering applications in low-frequency circuits, such as power supplies. They are cost-effective for large capacitance and can handle higher ripple currents, but their drawbacks include lower lifespan, larger physical size, and limited high-frequency performance. On the other hand, MLCCs are ideal for high-frequency applications, such as decoupling or noise suppression, due to their low equivalent series resistance (ESR) and inductance, compact size, and reliability. However, MLCCs are limited in capacitance range and may exhibit capacitance loss with applied DC voltage (DC bias effect). Designers should choose electrolytic capacitors for bulk capacitance in power management and MLCCs for high-frequency performance, low losses, and space-constrained applications.

4. Assuming a capacitor also has ESR and ESL (equivalent series inductance), which characteristic between its capacitance, inductance, and resistance do you expect to be

dominant at extremely high frequencies? Why?

At extremely high frequencies, the **equivalent series inductance (ESL)** of a capacitor becomes the dominant characteristic. This is because the impedance of an inductive element increases with frequency, while the impedance of the capacitor decreases as frequency rises. At high enough frequencies, the inductive behavior from the ESL will overshadow the capacitive behavior, causing the capacitor to behave more like an inductor. Additionally, the resistance (ESR) generally remains constant or increases slightly with frequency, but it is typically much smaller than the inductive impedance at high frequencies. As a result, ESL dominates and dictates the capacitor's high-frequency performance.

Feedback: post-lab, about 1.5 hours.