

EE 113B/213B: Power Electronics Design
Module 4: Open Loop Operation

Objectives

By the end of this module, you should be able to...

- Systematically assemble, test, and ramp up a converter's power stage
- Emulate source behavior using a dc power supply
- Emulate load behavior using an electronic load
- Obtain voltage and current waveforms using an oscilloscope
- Approximate converter efficiency
- Measure temperature rise using a thermal camera

Pre-lab Assignment

Safety Training

Log in to the UC Learning Center [here](#) and complete the EHS 804 Electrical Safety Awareness Training (referred to as Electrical Safety 2.0 in the course itself). This should take approximately 30 minutes. Once completed, take a screenshot of your Completion Status Report that includes your name, the course title, and completion status, and upload this as screenshot as part of your post-lab. You may NOT begin this lab until you complete this safety training.

Lab Safety

By beginning this module, you agree to the following important safety rules in the lab:

1. Always wear safety glasses when you, or any of your neighbors, have your main power supply on (i.e., the power supply acting as your converter's voltage/current source). Power converter failures often involve small projectiles that can cause serious damage to your eyes.
2. Do not wear metal jewelry on your hands or wrists, including watches, while testing your power converter.
3. Do not increase any power supply voltage above 30 V for any reason. To ensure a power supply does not surpass this limit when operating in constant-current mode, ensure its internal voltage limit is set to 30 V (or lower, to prevent your converter from failing).
4. Do not touch your converter configuration, even with probes, when your main power supply is on. Get in the habit of arranging your probes how you would like them before turning on the main power supply. "Live probing" is reserved for TAs only.
5. Make sure all wires and loose pieces are far from your converter, and that the converter itself and all connected cables are far from your body, before you turn on the main power supply. Position your converter in a location where you will not have to reach directly over it to adjust equipment.
6. Adopt a "risk minimization" mindset when configuring your test setup and test procedure. For example, make sure no wires are hanging off the bench in a way that you could bump them. If you are concerned about bumping certain cables, tape them down.
7. If at any point your converter begins to malfunction, turn off the main power supply if it is safe to do so. This should be your first reaction to stop testing.
8. If at any point you must work with an energized circuit (e.g., the gate circuit), use only one hand and make sure the rest of your body isn't touching any conductive surfaces.
9. Keep your converter on the rubber heat mat at all times while soldering and testing.
10. Keep your workbench is clean and free of other objects as possible. Use the lab computer instead of your own if you need to free up space.
11. Never touch the heated surface of a soldering iron or hot air gun.
12. Always use the solder fan when soldering to protect yourself from fumes.
13. Be sure to appropriately shield heat-sensitive components (e.g., plastic components, ICs, and electrolytic capacitors) with foil when using the hot air gun for soldering. Some components (e.g., electrolytic capacitors) may explode if exposed to heat.
14. Some types of solder contain Lead. Always wash your hands after soldering, especially before eating or drinking, and beware of contaminating personal property.

If you have any questions, please reach out to course staff before proceeding.

Lab Assignment

Note: You may not begin this lab until you have completed the mandatory safety training.

Adopting the strategy of systematic assembly and testing is similarly wise when building up power converters. In this lab, you will finish populating your power stage and get it working (i.e., converting power) first at a very low voltage and power level. Then, you will slowly ramp up its operation to the nominal operating point, and characterize its performance.

Akin to systematic assembly is systematic circuit debugging. If at any point you encounter abnormal operating behavior in your power converter, you should first document what the behavior is, what the behavior should be, and under what operating conditions the abnormality occurs. Then, you should systematically test other operating conditions, as well as the behaviors of surrounding components, to try to isolate the scope of the issue. Then, you should use the information you have to logically reason about what could be causing the abnormal behavior. You may request the help of course staff to help you troubleshoot issues, but it is important to follow these steps first to characterize the problem (rather than just telling course staff something doesn't work).

power supply

Switch Testing with Bus Voltage

Before assembling the entire power stage, it is good practice to verify correct operation of the switches as follows:

between 2 transistors

777

Input → GND.

PV+

- 25.26
1. Solder all remaining power stage components between the source and the inductor (i.e., the commutation loop decoupling capacitor, the input bus capacitors, and the input power source connectors) onto the PCB. Remember to shield plastic connectors and electrolytic capacitors from the hot air, and/or add the electrolytic capacitors last. DO NOT use hot air to solder the commutation loop decoupling capacitors; use the soldering iron to avoid damaging the switches with hot air. Electrolytic capacitors cannot withstand reverse voltage, so MAKE SURE you position your electrolytic capacitors in the correct orientation. Additionally, solder a short for R1. Later we will replace this short with a sense resistor for control purposes.
 2. Attach the microcontroller and configure it to produce a PWM output for a medium duty cycle (around 0.5). Turn on the auxiliary dc power supply for the gate drive circuit and set the output voltage to 10 V.
 3. Create a ground spring for an oscilloscope probe using a strand of wire, as shown in Fig. 1. Remove the witch hat from the probe, and attach the ground spring. The ground spring creates a lower inductance path for the measurement, which is important for observing voltages with high frequency content.
 4. Attach the voltage probe to the switch node and configure the oscilloscope to trigger between 0 and 10 V.
 5. Connect the dc supply WITH CORRECT POLARITY, and slowly ramp it up in constant voltage mode to about 10 V. Attaching your dc supply in the reverse direction will expose your electrolytic capacitor(s) to negative voltage and may cause them to explode.
 6. Based on the switch node's waveforms, verify that both switches are appropriately turning on and off. The switch node should look somewhat like a square wave between ground and 10 V.

Check-off: Confirm switches are functioning properly with bus voltage.

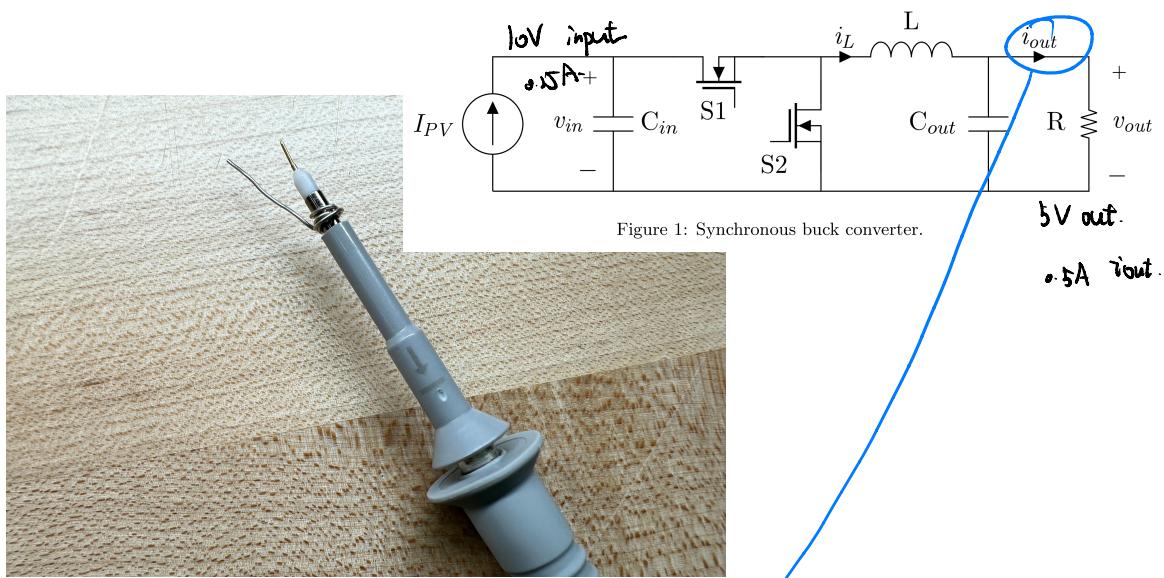


Figure 1: Oscilloscope probe configured with a ground spring.

Initial Power Stage Testing

R₁ ~~0.5~~

Now that you have verified your switches are functioning properly, you are ready to test the whole power stage!

1. Solder the remaining power stage components (inductor, output bus capacitors, output load connectors) to the PCB. Remember to shield plastic connectors and electrolytic capacitors from the hot air. Solder shorts for R₂ and R₃. These shorts will be replaced with sense resistors later.
2. Create a wire loop to connect the inductor to the output. This loop should be large enough to fit a current probe. Solder this wire to the PCB. ??
3. Reattach the microcontroller and configure it to produce a PWM output for the duty cycle corresponding to your nominal operating point. Turn on the auxiliary dc power supply for the gate drive circuit and set the output voltage to 10 V.
4. Attach probes for measuring the switch node voltage and inductor current.
5. Connect the electronic load, and configure it to operate like a constant-current 0.5 A load. Turn the electronic load on.
6. Turn on the dc supply, and slowly ramp it up to about 10 V still in constant voltage mode. If at any point you need to abruptly stop converter testing, your reaction should be to turn off this dc supply first.
7. Based on the voltage and current waveforms, verify that the converter is operating correctly at low voltage and low power.
8. Once you have finished, turn off the converter by first turning off the dc supply. Then proceed to turn off other equipment.

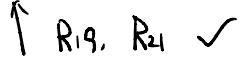
$$\text{current ripple: } \Delta I_{pp} = \frac{|V_o - V_{in}|}{L} \cdot DT_s = \frac{(10-5)V}{36\mu H} \times 0.5 \times 10^{-5} \approx 694.44 \text{ mA}$$

Check-off: Check waveforms and confirm appropriate converter behavior for low voltage, low power. ✓

Ramping up to Nominal Operation

Now that your converter is functioning properly, you are ready to ramp it up to nominal operation!

1. With the same dc supply and electronic load settings as the previous section, slowly increase the load (i.e., increase load current to increase power) until you reach the nominal output current. As you increase load, monitor the waveforms on the oscilloscope for appropriate converter behavior, and stop to troubleshoot any issues you encounter before proceeding.

- $\Delta V_{\text{OVP}} = \left(\frac{V_{\text{in}} - V_{\text{o}}}{L} \right) \cdot D T_s = \frac{36 \mu\text{H}}{R_{22}, R_{20} ? \checkmark}$
- Measure the voltage overshoot on the switch node with an input voltage of 10 V and a load corresponding to the maximum output current. Solder a 10Ω turn-on resistor for both switches. Compare the new voltage overshoot on the switch node to the previous case. Why does changing the gate resistance affect the voltage overshoot seen at the switch node? 
 - Oftentimes a turn-off gate resistance different than the turn-on gate resistance is used to achieve a higher efficiency. The turn-off gate resistance can be realized with a resistor in parallel with the turn-on resistor. Solder a 1Ω turn-off resistor on the PCB, and add a diode in series with the turn-off resistor that will allow the turn-off resistor to carry current only during turn-off. 
 - Once you have reached the full current load at low voltage begin slowly ramping up the voltage in small increments until you reach nominal. As you increase voltage, monitor the waveforms on the oscilloscope for appropriate converter behavior, and stop to troubleshoot any issues you encounter before proceeding.

$$V_{\text{in}} = 16 \sim 24 \text{V}$$

$$V_{\text{out}} = 12 \text{V} \quad P = 100 \text{W} \Rightarrow I = 8.33 \text{A}$$

Documenting Power Converter Performance

Now that you have a fully operational power stage, you should document its operation and evaluate its performance. For the nominal operating point and each of the four corner operating points, conduct the following:

- Before you begin operating the converter, attach probes to the input voltage, output voltage, switch node, and inductor current. Once the converter is operating at the desired voltages and power level, configure the oscilloscope to show 2-3 complete periods and ensure all waveforms are visible and appropriately zoomed to show the true ripple (even if high-frequency “spikes” extend off the screen). Take a screenshot of the waveforms. Use the oscilloscope’s cursors to measure the input voltage, output voltage, and inductor current ripples and average values, and compare these with your expected values. Ripple measurements should consider only true ripple and not high-frequency spikes (if present).
- Save the oscilloscope screenshot and export it as a file to include in your post-lab. You should repeat this for each operating point, perhaps in conjunction with the next steps.
- Approximate the efficiency of the converter by measuring the input and output voltages and currents. For current measurements, you may directly record the current levels shown on the dc supply and electronic load at your operating point of interest. For voltage measurements, you should measure the averages of your input voltage and output voltage waveforms using the oscilloscope. You will find that these voltage measurements are different from the values on the dc supply and electronic load due to resistance (and therefore loss) in the power cables. $V_{\text{in}} =$
- For only the nominal operating point and the highest-loss corner operating point, use the thermal camera to examine the temperature rise in different parts of your power converter while it operates at full load. Note which of your components have the greatest temperature rise. Compare the temperature rise of your inductor and your switches to their expected values. Note: Since temperature rise is not uniform throughout a component, you should focus on the highest “hotspot” temperature you observe for each component.

Note: For critical efficiency measurements, we would realistically use a power analyzer that simultaneously measures both currents and voltages and calculates efficiency in real time.

Check-off: (a) Confirm waveforms and efficiencies for nominal operating point and four corner operating points.
 (b) Indicate which converter components have appreciable temperature rise at the nominal and corner point tested, and how this temperature rise compares with your calculated value.

Set Up PV Module Emulation

A PV module is commonly modeled by the equivalent circuit shown in Fig. 2. The short-circuit current I_{SC} is generated by solar irradiance, so to test a PV module indoors, we must emulate I_{SC} using a current source

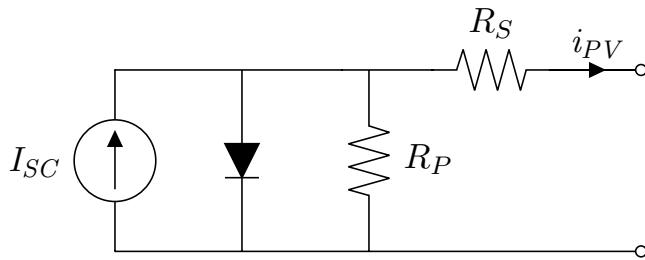


Figure 2: PV module circuit model.

I_{sc}

(implemented with a dc supply in constant current mode). In this class, you may assume the PV module is ideal (i.e., R_S and R_P are zero).

24.3

5.21A

- Configure the dc supply to operate in constant current mode, with a current limit equal to I_{SC} for the PV module and a voltage limit higher than the PV module's open-circuit voltage V_{OC} . Refer to the PV module's datasheet to find these values. Connect the dc supply in parallel with the PV module's output leads, and connect both to the input of your power converter.
- Configure the electronic load to operate in constant voltage mode at 12 V, with a current limit higher than the expected maximum output current. Connect the electronic load to the output of your power converter.
- Connect the microcontroller and begin switching with a duty cycle corresponding to low V_{in} .
- To begin operation, first turn on the electronic load and then turn on the constant current source. Confirm that the resulting input voltage is close to its expected value considering the duty cycle and 12 V output voltage.
75% → 50%
- Slightly change the duty cycle, and observe the changes in input voltage and current. Confirm these changes are in the expected directions for each.
0.025 2.5%
- Once you have confirmed correct behavior, identify the emulated PV panel's maximum power point. Start with a duty cycle that corresponds to one of the converter's input voltage boundaries, and sweep the duty cycle in small increments (e.g., .025) until you find a duty cycle that corresponds to maximum output power according to the electronic load. Record this maximum power point's duty cycle, input voltage, and output power.

Check-off: Confirm (a) the PV module emulator is functioning appropriately, and (b) the observed maximum power point duty cycle, input voltage, and output power. Tell us (c) how much dedicated time you spent on this lab, and (d) if any other student(s) in the lab helped you, and who.

RNG-100D-SS

100W Monocrystalline Solar Panel

Electrical Data

Maximum Power at STC*	100 W
Optimum Operating Voltage (V_{mp})	20.4 V
Optimum Operating Current (I_{mp})	4.91 A
Open Circuit Voltage (V_{oc})	24.3 V
Short Circuit Voltage (I_{sc})	5.21 A
Module Efficiency	17.8 %
Maximum System Voltage	600 VDC UL
Maximum Series Fuse Rating	15 A

Mechanical Data

Solar Cell Type	Monocrystalline (6.5 x 3.3 in)
Number of Cells	36 (3 x 12)
Dimensions	1062 x 530 x 35 mm(41.8x20.9x1.4in)
Weight	6.4 kg(14.1lbs)
Front Glass	Tempered Glass 0.13 in (3.2 mm)
Frame	Anodized Aluminium Alloy
Connectors	Solar Connectors
Fire Performance	Type 1

Thermal Characteristics

Operating Temp. Range	-40°C - 85°C(-40°F - 185°F)
Nominal Operating Cell Temperature (NOCT)	47±2°C
Temperature Coefficient of Pmax	-0.37%/°C
Temperature Coefficient of Voc	-0.28%/°C
Temperature Coefficient of Isc	0.05%/°C

MC4 Connectors

Rated Current	30A
Maximum Voltage	1000V DC
Maximum AWG Size Range	10 AWG
Temperature Range	-40°C - 90°C(-40°F - 194°F)
IP Rating	IP 67

Post-lab Assignment

Lab Results

1. Provide a screenshot of your UC Learning Center dashboard that shows you have completed the EHS 804 Electrical Safety Awareness training.
2. For the nominal operating point and all four corner operating points, provide waveform screenshots showing the switch node voltage, the input/output voltage, and the inductor current. Ensure ripple waveforms are zoomed in enough vertically to show the ripple, even if high-frequency spikes extend off the screen.
3. For the nominal operating point and all four corner operating points, provide the input/output voltage ripple and inductor current ripple measurements. These ripple measurements should consider only true ripple and not high-frequency spikes (if present).
4. For the nominal operating point and all four corner operating points, provide efficiency measurements. From these efficiency values, calculate the total power loss for each operating point.
5. For the nominal operating point and all four corner operating points, compare the measured power loss to the expected power loss based on your calculations.
6. Provide the duty cycle, input voltage, and output power corresponding to the maximum power point you observed for the emulated PV panel.

Lab Takeaways

1. Describe the merits of systematic assembling and testing. What is the potential downside of adding all components at once and then powering up the converter in one step?
2. Describe your sequence of setting up and powering on equipment (high-power dc supply, auxiliary dc supply, electronic load, microcontroller, oscilloscope probes, etc.) for testing your power converter.
3. When a certain part of your converter doesn't immediately operate correctly, describe your systematic approach for troubleshooting the issue. You may use an issue you encountered during this lab or a previous lab as an example.

Build Intuition

1. Describe how a thermal camera could be helpful for troubleshooting issues while ramping up your power converter.
2. Describe at least one limitation of the efficiency estimation procedure utilized in this module.
3. Are there other potential sources of loss in your converter power stage beyond what was considered in your loss calculations, and if so, what are they?
4. Describe how your efficiency measurements would change if your gate drive circuit was being powered by your converter's input voltage (stepped down to an appropriate level) rather than an auxiliary dc supply.

EE 213B

Make any final changes to your power stage design (e.g., component sizes, parts selected, etc.), with the understanding that your dual design goals are high efficiency and high power density within the cost budget detailed below. A question you should repeatedly ask is “If I add thing x to reduce loss, is the gain in whole-converter efficiency actually worth the extra size/weight/cost?” This applies to choosing fancier switches, adding heat sinks, choosing larger inductors, choosing to parallel several capacitors, etc. If the reduction in loss is negligible compared to other losses in your power converter, perhaps the extra size/weight/cost isn’t worth it after all.

In terms of budget, you are constrained to a cost limit of \$50 for the total board, not including the PCB itself. This also does not include standoffs, heat sink screws, magnet wire, shim stock, banana jacks, connectors, and test points, but it includes everything else you would be getting from our parts library (or special ordered). You must meet this budget constraint to be eligible for the efficiency, power density, and MPPT competitions. If you are over-budget, you are encouraged to consider the following to reduce your cost: (1) Reduce magnetics / capacitor sizes by increasing your switching frequency or allowing more ripple (though the input/output voltage ripple specifications are firm); (2) Only implement the minimum sensing needed for MPPT: output voltage and current.

Prepare PowerPoint slides for a power stage design review meeting with Prof. Boles. The purpose of these slides is to convey the necessary information about your design in a clear, concise way; the slides themselves need not be fancy, and you are welcome to digitally draw topologies, waveforms, etc. as long as the end result is clear. You should organize your slides as follows:

Topology and Operation:

1. Schematic of converter topology.
2. Converter operating sequence. Show each consecutive switch state, ignoring dead times for now.
3. Switching frequency, and how you selected it. Note: We are looking for technical justification here, including how this decision affects the size and loss of your converter.
4. The maximum voltage observed at any node in your topology.

Passive Sizing:

1. Minimum input and output capacitor/filter sizes needed to meet the ripple specifications.
2. How you sized all other passive components. Note: We are looking for technical justification here, including how this decision affects the part you are sizing but also other parts of your converter. What size and efficiency tradeoffs are there? What tradeoffs are associated with larger and smaller ripple?

Switches:

1. Voltage stresses and rms currents for each switch.
2. Whether or not C_{oss} and overlap losses are present in each switch. Show each switch transition of your switching cycle considering deadtime, and why C_{oss} loss and/or overlap loss do or do not occur during each one. Note: for each ideal switch state transition (i.e., not considering dead time), there are at least two actual switch state transitions that occur: at least one switch going from on to off (followed by deadtime), and then at least one switch going from off to on (followed by the new switch state).
3. Parts you selected for each switch. Provide each part's voltage rating, temperature-adjusted $R_{ds,on}$, and relevant equivalent C_{oss} .
4. Loss breakdown for each switch, including conduction loss, C_{oss} loss, and overlap loss, at the nominal and worst-case operating points. Note: Overlap loss should be calculate using actual rise and fall times with your selected gate driver.
5. Thermal design for each switch (i.e., whether or not you will be heat sinking each switch), and what junction temperature you expect for each switch with this design.

Magnetics:

1. Whether your magnetics are dc, ac, or both.

2. The method you used to design your magnetics, and what assumptions were made. For example, if using the K_g method to design an inductor, provide the inductance needed, your budgeted power loss, your assumed packing factor, your assumed maximum flux density, and whether or not Litz wire is needed.
3. Your final magnetics design(s). Include the material, core size, number of turns, wire size, and gap length.
4. Show that your final design meets the necessary constraints (inductance value, power loss / winding resistance, maximum flux density, etc.).
5. Expected loss for each magnetic component, including winding and core losses (if applicable), at the nominal and worst-case operating points.
6. Expected temperature rise for each magnetic component. In absence of thermal information for a given core, you should use the estimation method provided in KPVS.

Capacitors:

1. Whether you will implement each capacitor with electrolytic capacitor(s), multilayer ceramic capacitor(s), or both.
2. Your final design for implementing each capacitor (i.e., which parts, and how many in parallel). You should provide technical justification for the number of parts you choose to use in parallel. If reducing loss is the reason, you should justify whether the whole-converter efficiency improvement is worth the added volume/weight/cost.
3. For each electrolytic part you will be using, provide the voltage rating, capacitance, ESR, and current rating from the datasheet. Provide the expected rms current in your design, and show that it is below the safe limit.
4. For each MLCC, provide the voltage rating, derated capacitance value at the intended voltage, and ESR value at the frequency of use.
5. Expected loss for each capacitor (input, output, etc) at the nominal and worst-case operating points.

Efficiency:

1. Full power-stage loss breakdown for the nominal operating point and each corner operating point. For components with multiple loss types (e.g., switches), you should explicitly show each type. Note: Gate drive loss is not considered a power-stage loss.
2. Final expected power-stage efficiency for the nominal operating point and each corner operating point.

Budget:

1. A list of all parts, quantities, and prices for your power-stage parts.
2. The total cost of your power-stage parts. This does not include the gate drive or sensing circuits, so you should still leave significant room in your budget.

To submit your slides, email them as a PDF to course staff.

Assignment Feedback (Required)

How much dedicated time did you spend on this post-lab?

Nominal operating points: $\Delta V_{pp} = 1.44 \text{ A}$

$V_{in} = 20V$, $I_{out} = 8.33A$. $V_{out} = \underline{20 \times 0.6} \approx 12V$. $\underline{\text{Set}}$

REDO: use EBPRD = 480 $\Rightarrow f = 104.167 \text{ kHz}$

$$\text{Ideal } \Delta V_{pp} = \frac{|V_{in} - V_o|}{L} \cdot D \cdot I_s$$

$$= \frac{20-12}{36 \mu\text{H}} \times 0.6 \times 10^{-5}$$

Actually: $\overline{V_{out}} = 11.520V$. $I_{out} = 8.3365A$

$$\Delta V_{pp} = 1.41 \text{ A} \rightarrow 16.91\%$$

$$\overline{V_{in}} = 20.187V \quad \overline{I_{in}} = 4.99A$$

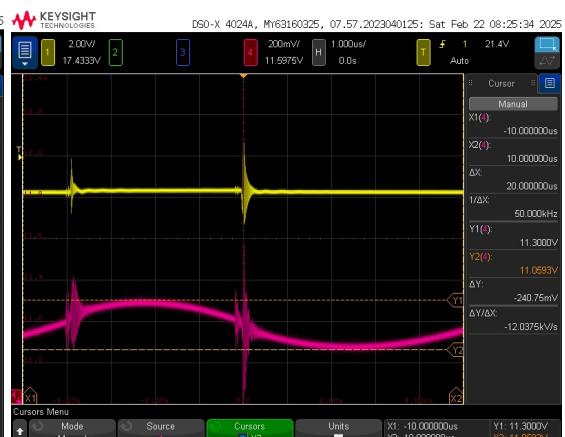
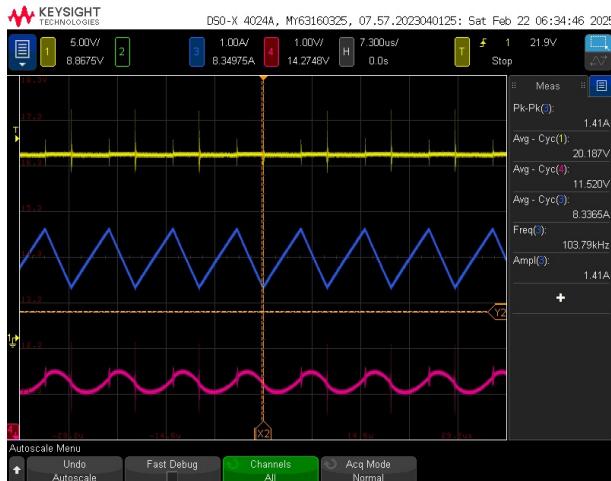
$$\Delta I_{in} = 105 \text{ mA} \rightarrow 2.10\%$$

$$\eta = \frac{V_{out} \cdot I_{out}}{P} = \frac{11.52 \times 8.3365}{20.187 \times 4.99} = 95.34\%$$

$$\Delta V_{out} = 240.75 \text{ mV} \rightarrow 2.09\%$$

$$\approx \underline{1.33A}$$

Loss = 4.70W



Operating point #1. $\underline{12V}$ $D = 0.75$

$$V_{in} = 16V \quad P = 100W \quad I_{o} \approx 8.33A$$

Measurement: $\overline{V_{out}} = 11.337V$. $\overline{I_{out}} = 8.323A$ $\Delta V_{pp} = 0.81A$

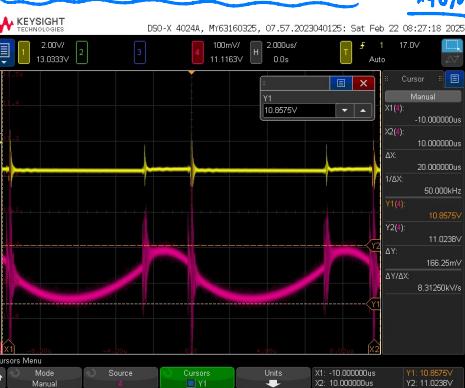
$$\% = 10.54\%$$

$$\overline{V_{in}} = 15.846V \quad \overline{I_{in}} = 6.24A \quad \Delta I_{in} = 88.75mA$$

$$\downarrow 14.42\%$$

$$\eta = \frac{11.337 \times 8.323}{15.846 \times 6.24} \approx 95.43\% \quad \text{Loss} = 15.12W$$

$$\downarrow 14.46\%$$



$$V_{in} = 24V, P = 100W, I_o \approx 8.33A, D = 0.5$$

$$\text{Measurement: } V_{in} = 23.725V, V_{out} = 11.243V, I_o = 8.3284A$$

$$\Delta I_{app} = 1.64A$$

$$I_{in} = 4.16A$$

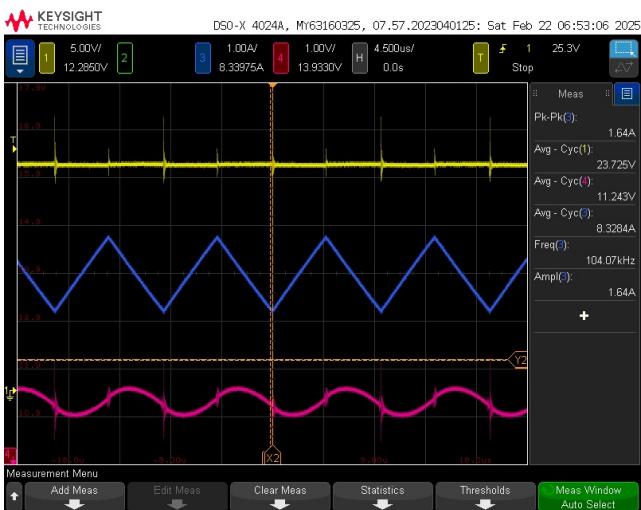
$$j = \frac{11.243 \times 8.3284}{23.725 \times 4.16} \approx 94.87\%$$

$$\Delta I_{in} = 105.0mA$$

$$\Delta I_{out} = 24.5\%$$

$$\Delta V_{out} = 273.75mV$$

$$\text{loss} = 5.0598W$$



$$V_{in} = 16V, P = 50W, I_o \approx 4.17A, D = 0.75$$

$$\text{Measurement: } V_{in} = 16.184V, V_{out} = 11.753V$$

$$\Delta I_{app} = 0.85A$$

$$I_{in} = 4.179V$$

$$j = \frac{11.753 \times 4.17}{16.184 \times 3.13} \approx 96.96\%$$

$$I_{in} = 3.13W$$

$$\text{loss} = 1.5401W$$

$$V_{in} = 50mA \rightarrow 16\%$$

$$V_{out} = 159.375mA \rightarrow 136\%$$



$$V_{in} = 24V, P = 50W, I \approx 4.7A, V_0 = 12V, D = 0.5$$



$$\text{Measurement: } V_{out} = 11.564V \quad I_0 = 4.1793A$$

$$V_{in} = 23.969V \quad \Delta i_{app} = 1.61A$$

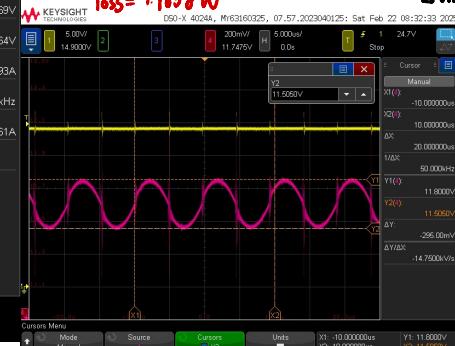
$$y = \frac{11.564 \times 4.1793}{23.969 \times 2.09} \approx 96.48\% \quad I_m = 2.09A$$

$$\text{loss} = 1.7658W$$

$$\Delta i_{in} = 48.70mA$$

$$\% = 233\%$$

$$\Delta V_{out} = 29mV \downarrow \\ 2.55\%$$



ripples maximum: At $V_{in}=24V, P=100W$

$$\frac{\Delta i_{app}}{I_0} = \frac{1.64A}{8.3284A} \approx 19.69\% < 20\%.$$

$$\frac{\Delta V_{out}}{V_{out} \text{ max}} = \frac{273.75mV}{11.243} = 2.43\%$$

(5).

compared to expected losses:

From the MATLAB code before,
we know that

```
P_loss_cond1_nosink = 2.9193
P_loss_cond2_nosink = 1.5866
P_loss_cond1_heatsink = 1.7253
P_loss_cond2_heatsink = 1.1386
```

Tj1_nosink = 214.3021

Tj2_nosink = 123.3710

Tj1_heatsink = 30.1848

Tj2_heatsink = 28.1752

P_loss1 = 1.8592

P_loss2 = 1.1386

eta_nominal = 0.9700

Lab:
95.34%

eta_v1 = 0.9698 94.87%

eta_v2 = 0.9842 96.48%

eta_v3 = 0.9701 95.43%

eta_v4 = 0.9846 96.96%

eta_score = 0.9743

From calculation with thermal model

loss - calculation	loss - lab
3W	4.70W
3.02W	5.0598W
1.58W	1.7658W
2.99W	4.5212W
1.54W	1.5401W

Lab efficiency and losses nominal point

$V_{in}=24V, P=100W$

$V_{in}=24V, P=50W$

$V_{in}=16V, P=100W$

$V_{in}=16V, P=50W$

because we neglect spikes, parasitic capacitance, loop commutations
diode reverse recovery

(b)

Isc = 5.21A Vout = 12V

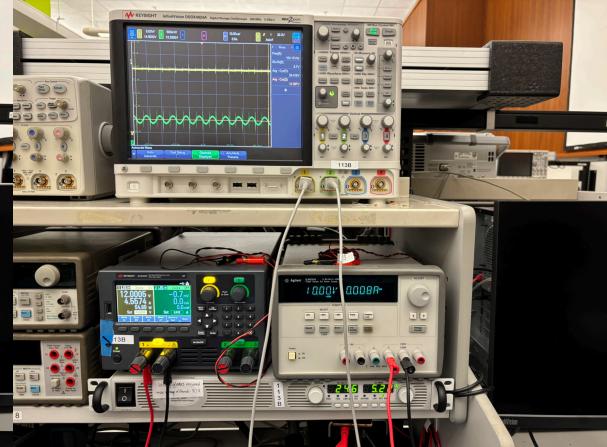
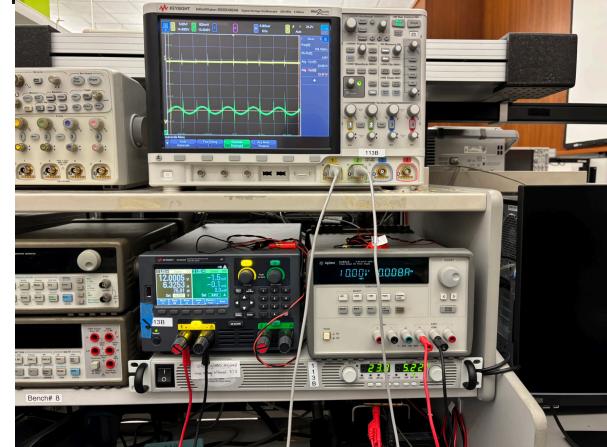
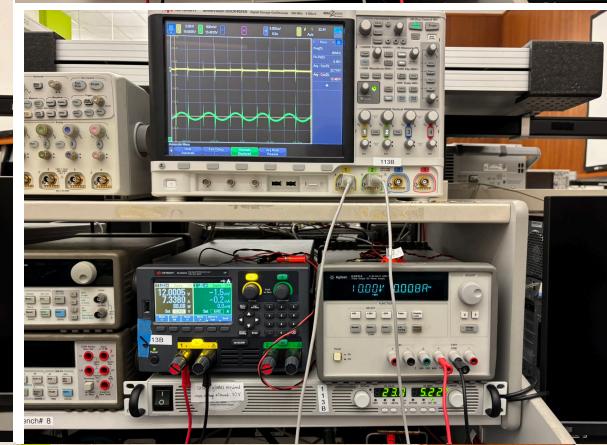
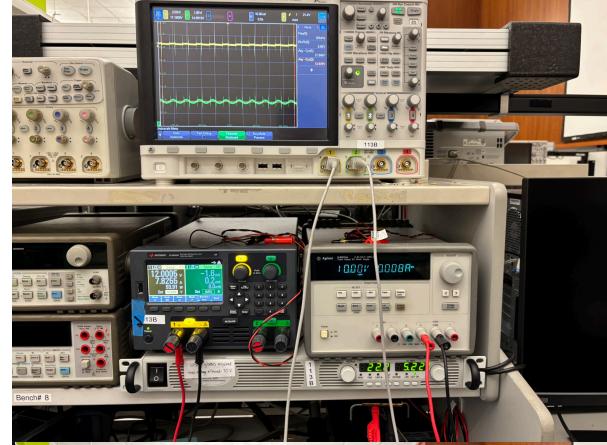
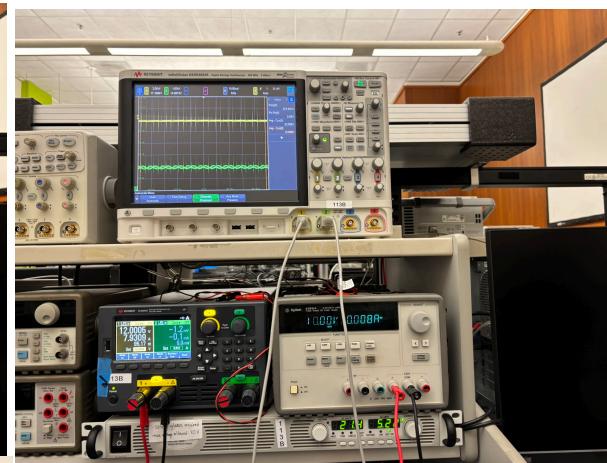
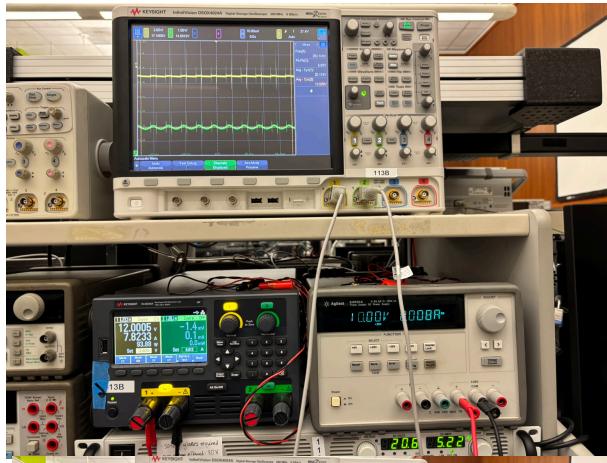
load

source		load		Duty %	Power_OUT (W)
Vin (V)	Iin (A)	Vout (V)	Iout (A)		
17.8	5.22	12.0005	6.9373	75	83.25
18.4	5.22	12.0005	7.1648	72.5	85.98
19	5.22	12.0005	7.3969	70	88.77
19.8	5.22	12.0005	7.6255	67.5	91.51
20.6	5.22	12.0005	7.8233	65	93.88
21.4	5.22	12.0005	7.9309	62.5	95.17
22.2	5.22	12.0005	7.8255	60	93.91
23	5.22	12.0005	7.338	57.5	88.06
23.8	5.22	12.0005	6.3253	55	75.91
24.6	5.22	12.0005	4.5574	52.5	54.69

maximum power point at

$D = 62.5\%$. $P_{out \max} = 95.17 \text{ W}$
 $V_m = 21.4 \text{ V}$.





Nominal operating points: $\Delta V_{pp} = 1.44 \text{ A}$

$$V_{in} = 20 \text{ V}, I_{out} = 8.33 \text{ A}, V_{out} = \underline{20 \times 0.6} \approx 12 \text{ V.} \quad \text{Set} \quad \% = 16.58\% \quad \text{Ideal } \Delta V_{pp} = \frac{|V_{in}-V_{o}|}{L} \cdot D \cdot I_s \\ = \frac{20-12}{36 \mu \text{H}} \times 0.6 \times 10^{-5}$$

Actually: $\overline{V_{out}} = 11.061 \text{ V}, I_{out} = 8.322 \text{ A.} \quad \Delta V_{pp} = 1.38 \text{ A.}$

$$\overline{V_{in}} = 19.27 \text{ V.} \quad \overline{I_{in}} = 4.99 \text{ A.} \quad \Delta V_{in} = 101.25 \text{ mA}$$

$$\% = 2.03\%$$

$$\approx 1.33 \text{ A}$$

$$\eta = \frac{V_{out} \cdot I_{out}}{P} = \frac{11.061 \times 8.322}{19.27 \times 4.99} \approx 95.73\%$$

MOS: 44.2°C . LOAD PVT: 45°C .

IMG

scope0

1 - nipple.

12

MOS Q1: 56.4°C

12V D=0.75

MOS: 47°C . LOAD PVT: 53.4°C

$\% = 10.54\%$

$V_{in} = 16 \text{ V}$. P = 100 \text{ W}. $I_o \approx 8.33 \text{ A}$

Measurement: $\overline{V_{out}} = 11.269 \text{ V.} \quad \overline{I_{out}} = 8.342 \text{ A.} \quad \Delta V_{pp} = 0.88 \text{ A}$

$\overline{V_{in}} = 15.65 \text{ V} \quad \overline{I_{in}} = 6.24 \text{ A.} \quad \Delta V_{in} = 88.75 \text{ mA}$

$$\eta = \frac{11.269 \times 8.342}{15.65 \times 6.24} \approx 96.26\%$$

IMG - scope2.

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$$V_{in} = 24V \quad P = 100W, \quad I_o \approx 8.33A \quad D = 0.5$$

-1.66A ripple - scope 7 + scope 19

Measurement: $\overline{V_{in}} = 23.612V$, $\overline{V_{out}} = 11.283V$, $\overline{I_o} = 8.34A$

at load $\% = 20.62\%$

$\Delta \dot{I}_{app} = 1.69A$, $\overline{I_{in}} = 4.16A$

$\eta = \frac{11.283 \times 8.34}{23.612 \times 4.16} = 95.80\%$, $\Delta V_{in} = 92.50mA$

IMG: scope 3

60.1°C MOS



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500 → 100 kHz

scope 19: $E_B P_{RD} = 400 \Rightarrow 125kHz$
 $\Rightarrow \text{ripple} = 1.34A$.

At 200kHz, $\dot{I}_o = 84mA$
scope 20 $\% = \dots 10\%$

$$\frac{0.6}{11.48} > 20\%$$

$$V_{in} = 16V, \quad P = 50W, \quad I_o \approx 4.17A \quad D = 0.75$$

Measurement: $\overline{V_{in}} = 15.412V$, $\overline{V_{out}} = 11.308V$

% = 19.85%
 $\Delta \dot{I}_{app} = 0.83A$, $\overline{I_o} = 4.1865A$

$\eta = \frac{11.308 \times 4.1865}{15.412 \times 3.13} = 98.1\%$, $\overline{I_{in}} = 3.13W$

IMG: scope 4

$\Delta V_{in} = 50mA$
 $\% = 1.59\%$

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 =

$$V_{in} = 24V, P = 50W, I \approx 4.17A, V_0 = 12V, D = 0.5$$

Measurement: $\overline{V_{out}} = 11.662V, \overline{I_o} = 4.168A$
 $\overline{V_{in}} = 23.908V, \Delta I_{app} = 1.72A$

$$\eta = \frac{11.662 \times 4.168}{23.908 \times 2.09} = 97.27\%$$

$$\overline{I_m} = 2.09A, \Delta I_{in} = 48.7mA$$

\downarrow
 $\% = 20.37\%$

IMG - Scope 5

- 11.

↓ slope 20, 200kHz, $\Delta I_o = 830mA$, $I_L = 4.185A$.

$$\Rightarrow \underline{\underline{\% = 19.83\%}}$$

$$\overline{V_{in}} = 23.662V, \overline{I_{in}} = 2.07A, \overline{V_0} = 11.47V, \overline{I_o} = 4.18A$$

$$\Rightarrow \eta = \frac{11.47 \times 4.18}{23.662 \times 2.07} = 97.43\%$$