

EE 113B/213B: Power Electronics Design
Module 1: Switches and Simulation

Objectives

By the end of this module, you should be able to...

- Extract performance-relevant information from power FET datasheets
- Calculate expected losses for power FETs
- Compare and select power FETs from a marketplace
- Size power FET heatsinks
- Simulate power FET parasitics
- Estimate losses using simulation

Recommended reading: KPVS Sections 15.1, 15.3.2 (MOSFET section), 16.4, 16.5, 17.5, 17.10, 22.4, 25.1, 25.2
Additional background on semiconductor physics: 16.1

Pre-lab Assignment

Now that you have sized the components for your buck converter, you are ready to begin selecting and designing these components. In this pre-lab, we will select switches S1 and S2 as shown in Fig. 1 and download PLECS for use in the lab.

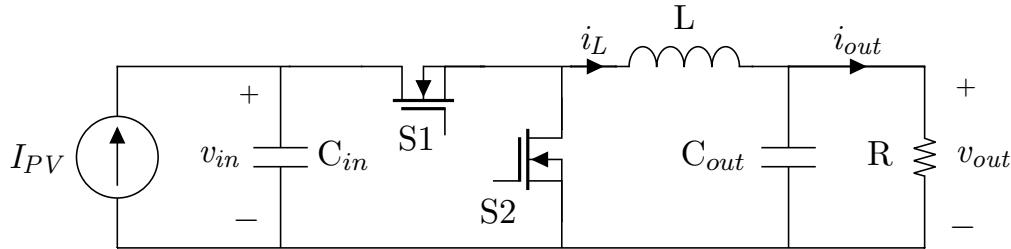


Figure 1: Synchronous buck converter.

Table 1: Buck Converter Design Specifications

Specification	Value
Nominal Input Voltage	20 V
Input Voltage Range	16-24 V
Output Voltage	12 V
Nominal Output Power	100 W
Output Power Range	50-100 W
Switching Frequency	100 kHz
Input Voltage Ripple	$\leq 5\%$
Output Voltage Ripple	$\leq 5\%$
Inductor Current Ripple (at 100W)	$\leq 20\%$

Switch Loss

The power loss incurred by each of a converter's components directly affects its overall efficiency, which is an important metric for evaluating power converter performance. Thus, component selection is often closely intertwined with loss estimation.

For the following calculations, assume the 55 V International Rectifier IRFZ34NpbF power MOSFET for both buck converter switches, and the nominal voltage, maximum power operating point in Table 1. You may find this part's datasheet in a [zip file uploaded to bCourses](#), and you may assume both switches operate with a junction temperature of 25 °C (for now). Hint: You may want to write a [script](#) to calculate these losses based on a set of switch parameters.

1. Calculate the conduction loss for each switch. To do this, you should first calculate the rms current through the switch (ignoring deadtime) and note its $R_{ds,on}$ reported in the datasheet.
2. Specify which switching transitions (high-side turn on, high-side turn off, low-side turn on, and low-side turn off) are hard transitions.
3. Calculate the overlap loss expected for each switch. For this module only, you may approximate the overlap time as being $t_{ov} \approx \frac{Q_{gd}}{I_g}$, where Q_{gd} is reported in the switch's datasheet and the gate drive current I_g is 1 A. For this module only, you may assume only hard turn-on transitions have overlap loss.

4. Calculate the C_{oss} loss expected for each switch. To do this, you should use the appropriate charge- or energy-equivalent capacitance as a linearization of C_{oss} with respect to drain-source voltage. We have uploaded a Matlab script to bCourses that computes these equivalent capacitances based on data points extracted from the C_{oss} plot in a switch's datasheet. If you have trouble running this script, try updating Matlab to the latest version.
5. What is the total expected power loss for each switch?

Thermal Management

An often overlooked step in choosing components for a power converter is thermal management. In many cases, the power loss of a component results in an unacceptable temperature rise, requiring heat sinking for safe operation and/or loss reduction. Conduct the following for the part and operating point assumed in the previous section:

1. Based on the expected power loss, calculate each switch's expected junction temperature assuming an ambient temperature of 25 °C. Comment on whether or not this is within each switch's acceptable operating temperature range.
2. With this junction temperature, determine each switch's actual $R_{ds,on}$. Calculate each switch's actual conduction loss with these $R_{ds,on}$ for the same operating point, and compare it to the conduction loss you calculated assuming a junction temperature of 25 °C.
3. One common strategy for cooling TO-220 switches involves mounting the device onto a heatsink with an insulating thermal pad in between. The thermal resistance of the insulating pad may be represented by $R_{\theta CS}$, and the thermal resistance between the sink and ambient is $R_{\theta SA}$. Sketch a thermal circuit model of this structure, including $R_{\theta JC}$, $R_{\theta CS}$, and $R_{\theta SA}$.
4. Consider the TO-220 heat sink and the thermal pad provided in the parts library, and their respective thermal resistances assuming natural convection. Using your thermal circuit model, calculate what each switch's expected junction temperature would be with this heat sink configuration assuming an ambient temperature of 25 °C.
5. At this junction temperature, determine each switch's $R_{ds,on}$ and calculate its conduction loss for the same operating point. Compare its loss to the configuration without a heat sink.
6. Choose whether or not a converter design using this power transistor should use these heat sinks. You may consider using heat sinks on one, both, or neither switch.
7. With this heat sink configuration, calculate the total conduction loss for the nominal operating point and all four corner operating points assuming the switches' actual operating junction temperatures.

Switch Selection

Consider the selection of other power transistors in the parts library on bCourses (datasheets are provided in a .zip folder under this module). Select (a) the most appropriate power transistor parts for your buck converter design based on power loss, voltage rating, etc., and (b) whether or not each switch will have a heat sink. You may choose to implement your switches with the same part or different parts, each with or without a heatsink. To help you make this selection, you should calculate expected loss at the nominal operating point and at all four corner operating points, considering each switch's actual $R_{ds,on}$ with or without the heatsink. If you choose to use two different power transistor parts, you must consider how this affects the C_{oss} loss calculation (i.e., use of both charge- and energy-equivalent capacitance). Based on total loss, you should ensure that the junction temperature of each switch is within its acceptable operating temperature range for all five relevant operating points. If helpful, you may assume your converter's final efficiency score will be evaluated as follows:

$$\eta_{score} = 0.4(\eta_{nominal}) + 0.15(\eta_{corner,1}) + 0.15(\eta_{corner,2}) + 0.15(\eta_{corner,3}) + 0.15(\eta_{corner,4}) \quad (1)$$

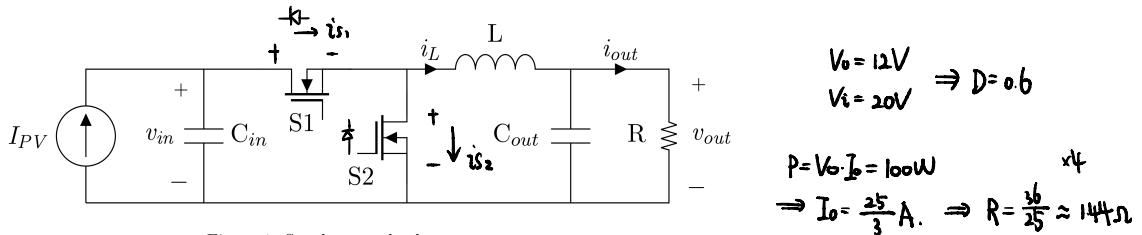


Figure 1: Synchronous buck converter.

$$V_0 = 12V \\ V_i = 20V \Rightarrow D = 0.6$$

$$P = V_0 \cdot I_0 = 100W \\ \Rightarrow I_0 = \frac{25}{3} A. \Rightarrow R = \frac{36}{25} \approx 14\Omega$$

assume the 55 V International Rectifier IRFZ34NpbF power MOSFET

- Calculate the conduction loss for each switch. To do this, you should first calculate the rms current through the switch (ignoring deadtime) and note its $R_{ds, on}$ reported in the datasheet.
- Specify which switching transitions (high-side turn on, high-side turn off, low-side turn on, and low-side turn off) are hard transitions. *For the overlap, the total charge needed to complete = Q_{gd} .*
- Calculate the overlap loss ~~expected for each switch~~. For this module only, you may approximate the overlap time as being $t_{ov} \approx \frac{Q_{gd}}{I_g}$, where Q_{gd} is reported in the switch's datasheet and the gate drive current I_g is 1 A. For this module only, you may assume only hard turn-on transitions have overlap loss. ?

$$1. P_{loss, cond1} = i_{sw, rms}^2 \cdot R_{ds, on}$$

$$i_{sw, rms} = \sqrt{\frac{1}{T_s} \int_{t_0}^{T_s} i_{sw}^2 dt}$$

$$i_{sw, rms} = \sqrt{D} \cdot i_{S1} = \sqrt{D} \cdot I_L = 6.455A$$

$$i_{sw, rms} = \sqrt{D} \cdot i_{S2} = \sqrt{D} \cdot (-I_L) \approx -5.2705A$$

① S_1 on S_2 off

$$i_{S1} = i_L = \frac{V_0}{R} = \frac{12V}{14\Omega}$$

$$i_{S2} = 0$$

② S_1 off S_2 on

$$i_{S2} = -i_L = -\frac{DV_{in}}{R}$$

$$i_{S1} = 0$$

max condition.

$$\text{let } R_{ds, on} = 0.04\Omega$$

$$P_{loss, cond1} = 6.455^2 \times 0.04 = 1.67W$$

$$P_{loss, cond2} = 5.2705^2 \times 0.04 = 1.11W$$

	$\frac{V_{S1}}{0}$	$\frac{V_{S2}}{Vin}$	high-side turn on:	$V_{S1}: Vin \rightarrow 0$	$i_{S1} \leftarrow i_L$	X	hard transitions
deadtime	Vin	0	high-side turn off	$V_{S1}: 0 \rightarrow Vin$	$i_{S1} \rightarrow i_L$	X	soft transitions
(body diode)			low-side turn on	$V_{S2}: Vin \rightarrow 0$	$i_{S2} \uparrow i_L$	✓	soft transitions
S_2 on	Vin	0	low-side turn off	$V_{S2}: 0 \rightarrow Vin$	$i_{S2} \downarrow i_L$	X	hard transitions

\Rightarrow high-side on, low-side off are hard transitions.

3. Q_{gd} represents the charge accumulated between G, S.

Only considering hard-turn-on transitions, $V_{S1}: Vin \rightarrow 0$ $i_{S1}: 0 \rightarrow i_L$

Always increase first, then decline

maybe the & to completely on.

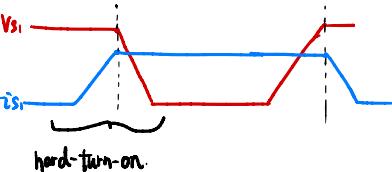
$$t_{ov} \approx \frac{Q_{gd}}{I_g} = \frac{14nC}{1A} = 1.4 \times 10^{-8}s$$

$$f_{sw} = 100kHz = 10^5 Hz$$

$$P_{loss, ov} = \left(\frac{1}{2} V_{in} \cdot I_L \right) \cdot t_{ov} \cdot f_{sw}$$

$$= \frac{1}{2} \times 20 \times \frac{25}{3} \times 1.4 \times 10^{-8} \times 10^5$$

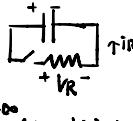
$$= 0.1167W$$



4. Calculate the C_{oss} loss expected for each switch. To do this, you should use the appropriate charge- or energy-equivalent capacitance as a linearization of C_{oss} with respect to drain-source voltage. We have uploaded a Matlab script to bCourses that computes these equivalent capacitances based on data points extracted from the C_{oss} plot in a switch's datasheet. If you have trouble running this script, try updating Matlab to the latest version.

5. What is the total expected power loss for each switch?

(4) For the output capacitance loss,



$$E_{total} = E_{S1} + E_{S2} = \underbrace{\int_0^{+∞} V_R i_R dt}_{\text{Energy}} + \underbrace{\int_0^{+∞} (V_{in} - V_{S2}) i_R dt}_{\text{charge-energy}}$$

$$= \frac{1}{2} C_{eq,E} \cdot V_{in}^2 + C_{eq,Q} \cdot V_{in}^2 - \frac{1}{2} C_{eq,E} \cdot V_{in}^2$$

$$= C_{eq,Q} \cdot V_{in}^2$$

$$\Delta Q = \int_0^{+∞} i_C dt$$

$$= \int_0^{+∞} C \frac{dV_C}{dt} dt$$

$$= \int_0^{V_{dc}} C \cdot dV_C = C_{eq,Q} \cdot V_{dc}$$

$$\Rightarrow C_{eq,Q} = \frac{1}{V_{dc}} \int_0^{V_{dc}} C(V_C) \cdot dV_C \quad \begin{matrix} V_C \text{ in MOSFET} \\ \Leftrightarrow V_C = V_{os} \end{matrix}$$

\Leftrightarrow average value of C

$$\Rightarrow C_{eq,E} = \frac{2}{V_{dc}^2} \int_0^{V_{dc}} C(V_C) \cdot V_C dV_C$$

↑ For Review

↓ For Problem (4).

We should choose $C_{eq,Q}$ as linearization of C_{oss}

$$\Rightarrow C_{oss} = C_{eq,Q} = 432.54 \text{ pF} \quad . \quad C_{eq,E} \approx 337.94 \text{ pF}$$

From MATLAB.

$$(5) \text{ For } S_1: E_{total1} = \int_0^{+∞} V_R i_R dt = \frac{1}{2} C_{eq,E} \cdot V_{in}^2$$

$$= \frac{1}{2} \times 337.94 \times 20^2 \times 10^{-12}$$

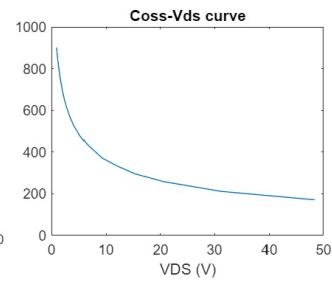
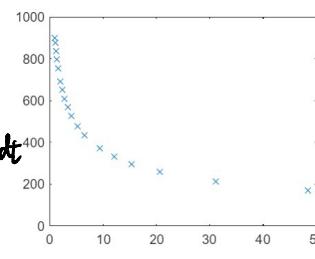
$$= 6.76 \times 10^{-8} \text{ J (in one cycle)}$$

$$\text{For } S_2: E_{total2} = \int_0^{+∞} V_R i_R dt = \int_0^{+∞} (V_{in} - V_{S2}) C \frac{dV_C}{dt} dt$$

$$= C_{eq,Q} \cdot V_{in}^2 - \frac{1}{2} C_{eq,E} \cdot V_{in}^2$$

$$= 432.54 \times 10^{-12} \times 20^2 - \frac{1}{2} \times 337.94 \times 10^{-12} \times 20^2$$

$$= 1.05 \times 10^{-7} \text{ J (in one cycle)}$$



$$P_{total1} = 1.67W + 0.116W + 0.0173W$$

$$= 1.7954W \approx 1.8W$$

$$P_{total2} = 1.11W + 0.116W$$

$$= 1.2335W \approx 1.2W$$

Some of the mistake here, C_{oss} loss only goes

$$P_{loss1} = E_{total1} \times f \approx 1.05 \times 10^{-7} W \quad \left. \begin{array}{l} \text{Coss loss} \\ \text{(output capacitance loss)} \end{array} \right\}$$

$$P_{loss2} = E_{total2} \times f \approx 6.76 \times 10^{-8} W \quad \left. \begin{array}{l} \text{Coss loss} \\ \text{(output capacitance loss)} \end{array} \right\}$$

$$\Rightarrow 1.73 \times 10^{-8} W \text{ all}$$

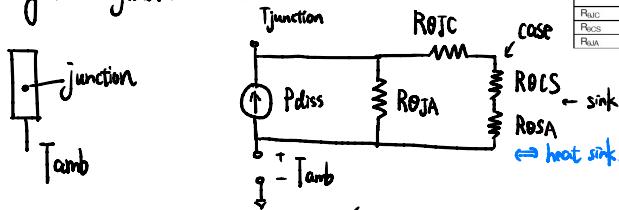
to hard turn-on transitions, but P_{oss} is small, we can neglect.

Thermal Management

An often overlooked step in choosing components for a power converter is thermal management. In many cases, the power loss of a component results in an unacceptable temperature rise, requiring heat sinking for safe operation and/or loss reduction. Conduct the following for the part and operating point assumed in the previous section:

- Based on the expected power loss, calculate each switch's expected junction temperature assuming an ambient temperature of 25 °C. Comment on whether or not this is within each switch's acceptable operating temperature range.
- With this junction temperature, determine each switch's actual $R_{ds,on}$. Calculate each switch's actual conduction loss with these $R_{ds,on}$ for the same operating point, and compare it to the conduction loss you calculated assuming a junction temperature of 25 °C.
- One common strategy for cooling TO-220 switches involves mounting the device onto a heatsink with an insulating thermal pad in between. The thermal resistance of the insulating pad may be represented by $R_{\theta CS}$, and the thermal resistance between the sink and ambient is $R_{\theta SA}$. Sketch a thermal circuit model of this structure, including $R_{\theta JC}$, $R_{\theta CS}$, and $R_{\theta SA}$.

1. normally for a junction-device



Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
P _{JKC}	Junction-to-Case	—	—	—	°C/W
P _{PCS}	Case-to-Sink, Flat, Greased Surface	—	0.50	—	—
P _{PA}	Junction-to-Ambient	—	—	62	—

From datasheet

① without heat sink, ROSA 200

$$\Rightarrow T_{\text{junction}} = T_{\text{amb}} + P_{\text{diss}} \cdot R_{\theta JA}$$

$$= 25^{\circ}\text{C} + P_{\text{diss}} \cdot b_2$$

$$\Rightarrow T_{\text{junction1}} = 25 + 1.8 \times b_2 \approx 136.6^{\circ}\text{C}$$

$$T_{\text{junction2}} = 25 + 1.2 \times b_2 \approx 99.4^{\circ}\text{C}.$$

T_j Operating Junction and Storage Temperature Range -55 to +175 °C

I know it's very high, but seemingly $T_{\text{junction1,2}}$ are within operating temperature.

(under $V_{DS} = 10V$).

(2). From the datasheet, 25°C, $R_{DS} = 0.04\Omega$ \Rightarrow

$$\begin{cases} 99.4^{\circ}\text{C} \approx 1.45 \times 0.04 = 0.058\Omega & 2 \\ 136.6^{\circ}\text{C} \approx 1.72 \times 0.04 = 0.069\Omega & 1 \end{cases}$$

T_{junction} : vs. 25°C

1.67W

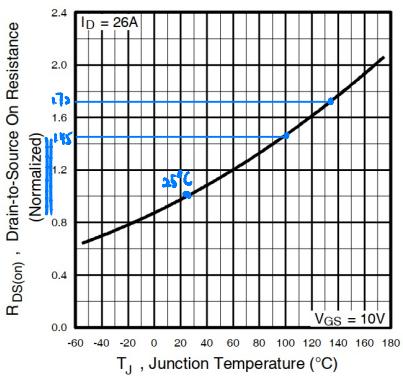
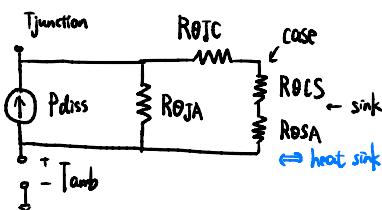
$$\Rightarrow P_{\text{loss, cond1}} = 6.45^2 \times 0.058 = 2.875\text{W}$$

$$P_{\text{loss, cond2}} = 5.27^2 \times 0.069 = 1.611\text{W}$$

1.11W

same as (1).

(3).

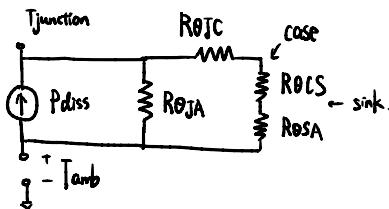


4. Consider the TO-220 heat sink and the thermal pad provided in the parts library, and their respective thermal resistances assuming natural convection. Using your thermal circuit model, calculate what each switch's expected junction temperature would be with this heat sink configuration assuming an ambient temperature of 25°C .
5. At this junction temperature, determine each switch's $R_{ds,on}$ and calculate its conduction loss for the same operating point. Compare its loss to the configuration without a heat sink.
6. Choose whether or not a converter design using this power transistor should use these heat sinks. You may consider using heat sinks on one, both, or neither switch.
7. With this heat sink configuration, calculate the total conduction loss for the nominal operating point and all four corner operating points assuming the switches' actual operating junction temperatures.

(4). FEATURES AND BENEFITS

• Thermal impedance: $0.22^{\circ}\text{C-in}^2/\text{W}$ @ 50 psi

normally we choose $R_{QJA} = 0.22^{\circ}\text{C/W}$ @ 50 psi (pounds per square inch).



$$R_{QJA} = 62, R_{QJC} = 2.2, R_{QCS} = 0.5, R_{QSA} = 0.22$$

$$\Rightarrow R_{\text{total}} = 62 \parallel (2.2 + 0.5 + 0.22) \\ \approx 2.79^{\circ}\text{C/W}$$

22.4

22.9

$$R_{\text{total}} = 62 \parallel (2.2 + 0.5 + 0.22) \\ = 17.87^{\circ}\text{C/W}$$

$$\Rightarrow T_{\text{junction}} = T_{\text{amb}} + P_{\text{diss}} \cdot R_{\text{total}}$$

$$\Rightarrow T_{\text{junction1}} = 25 + 1.8 \times 2.79 \approx 30.02^{\circ}\text{C} \quad [25 + 1.8 \times 17.87 = 57.166^{\circ}\text{C}]$$

$$T_{\text{junction2}} = 25 + 1.2 \times 2.79 \approx 28.35^{\circ}\text{C}. \quad [25 + 1.2 \times 17.87 = 46.444^{\circ}\text{C}]$$

(5). $R_{ds,\text{on}}$, they are approximately same, assume increase 3% - 5%.

25°C

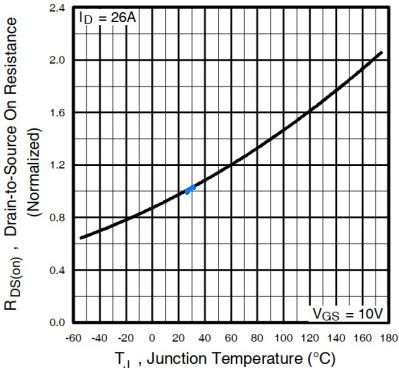
T_j

$$\Rightarrow R_{ds1} = 0.04 \times (1+5\%) \approx 0.042 \Omega \Rightarrow P_{\text{loss, cond1}} = 1.67 \times (1+5\%) = 1.75 \text{ W} \\ R_{ds2} = 0.04 \times (1+3\%) \approx 0.0412 \Omega. \quad P_{\text{loss, cond2}} = 1.11 \times (1+3\%) = 1.14 \text{ W}.$$

on both SW

(6). Yes, I shall choose to use heat sink, although 130°C & 100°C are within operating Temperature range, $R_{ds,\text{on}}$ largely increases. P_{loss} increases about 50% and 75%.

with heat sink applied, only 3% and 5% losses are increased.



(7). For nominal operating points, with heat sink applied, only $P_{\text{cond,loss}}$ affected.

$$\Rightarrow P_{\text{total1}} = 0.08 \text{ W} \Rightarrow P_{\text{total1}} = 1.88 \text{ W}$$

$$P_{\text{total2}} = 0.03 \text{ W} \Rightarrow P_{\text{total2}} = 1.23 \text{ W}$$

Four operating points.

1. Nominal operating point:

$$V_{in} = 20V, P_{out} = 100W, V_{out} = 12V, D = 0.6$$

$$\text{I: } P_{loss, \text{cond1}} = (\overline{fD} \cdot I_L)^2 \cdot R_{ds1} \quad T_1 \approx 30^\circ C, R_{ds1} \approx 0.042 \Omega$$
$$P_{loss, \text{cond2}} = (\overline{fD} \cdot I_L)^2 \cdot R_{ds2} \quad T_2 \approx 28^\circ C, R_{ds2} = 0.041 \Omega$$
$$\text{II: } P_{loss, \text{ov}} = \left(\frac{1}{2} V_{in} \cdot I_L\right) \cdot \text{tov} \cdot f_{sw}$$

1.2 highest V_{in} , highest load $\Leftrightarrow P_{max}$

$$\Rightarrow V_{in} = 24V, P_{max} = 100W, V_{out} = 12V$$

$$\Rightarrow D = 0.5 \quad I_L = \frac{25}{3}A$$

$$= \frac{1}{2} \times 24 \times \frac{25}{3} \times 1.4 \times 10^{-8} \times 10^5$$
$$= 0.0058 \cdot V_{in}$$

III: $P_{loss} \approx$ remains the same.

$$P_{loss, \text{loss}} = 0.0173W$$

1.3 highest V_{in} , lowest load $\Leftrightarrow P_{min}$

$$\Rightarrow V_{in} = 24V, P_{min} = 50W, V_{out} = 12V$$

$$\Rightarrow D = 0.5 \quad I_L = \frac{25}{6}A$$

\Rightarrow 4 corner operating points

① $V_{in \text{ max}}, Z_{load \text{ max}}$:

$$P_{loss1} = 0.5 \times \left(\frac{25}{3}\right)^2 \times 0.042 + 0.0058 \times 24 + 0.0173W$$
$$= 1.61W$$

$$P_{loss2} = 0.5 \times \left(\frac{25}{3}\right)^2 \times 0.041$$
$$= 1.47W$$

1.4 lowest V_{in} , highest load $\Leftrightarrow P_{max}$

$$\Rightarrow V_{in} = 16V, P_{max} = 100W, V_{out} = 12V$$

$$\Rightarrow D = 0.75 \quad I_L = \frac{25}{3}A$$

1.5 lowest V_{in} , lowest load $\Leftrightarrow P_{min}$

$$\Rightarrow V_{in} = 16V, P_{min} = 50W, V_{out} = 12V, D = 0.75$$

$$I_L = \frac{25}{6}A$$

② $V_{in \text{ max}}, Z_{load \text{ min}}$

$$P_{loss1} = 0.5 \times \left(\frac{25}{6}\right)^2 \times 0.042 + 0.0058 \times 24 + 0.0173W$$
$$= 0.51W$$

$$P_{loss2} = 0.5 \times \left(\frac{25}{6}\right)^2 \times 0.041$$
$$= 0.41W$$

③ $V_{in \text{ min}}, Z_{load \text{ max}}$

$$P_{loss1} = 0.75 \times \left(\frac{25}{3}\right)^2 \times 0.042 + 0.0058 \times 16 + 0.0173W$$
$$= 2.29W$$

$$P_{loss2} = 0.25 \times \left(\frac{25}{3}\right)^2 \times 0.041$$
$$= 0.71W$$

④ $V_{in \text{ min}}, Z_{load \text{ min}}$

$$P_{loss1} = 0.75 \times \left(\frac{25}{6}\right)^2 \times 0.042 + 0.0058 \times 16 + 0.0173W$$
$$= 0.65W$$

$$P_{loss2} = 0.25 \times \left(\frac{25}{6}\right)^2 \times 0.041$$
$$= 0.18W$$

Switch Selection

Consider the selection of other power transistors in the parts library on bCourses (datasheets are provided in a .zip folder under this module). Select (a) the most appropriate power transistor parts for your buck converter design based on power loss, voltage rating, etc., and (b) whether or not each switch will have a heatsink. You may choose to implement your switches with the same part or different parts, each with or without a heatsink. To help you make this selection, you should calculate expected loss at the nominal operating point and at all four corner operating points, considering each switch's actual $R_{ds,on}$ with or without the heatsink. (If you choose to use two different power transistor parts, you must consider how this affects the C_{oss} loss calculation) (i.e., use of both charge- and energy-equivalent capacitance). Based on total loss, you should ensure that the junction temperature of each switch is within its acceptable operating temperature range for all five relevant operating points. If helpful, you may assume your converter's final efficiency score will be evaluated as follows:

$$\eta_{score} = 0.4(\eta_{nominal}) + 0.15(\eta_{corner,1}) + 0.15(\eta_{corner,2}) + 0.15(\eta_{corner,3}) + 0.15(\eta_{corner,4}) \quad (1)$$

For the parts and heatsink configurations you choose, provide junction temperatures and a final loss breakdown at the nominal operating point and all four corner operating points. These will be the parts you use to build your converter in subsequent modules.

I will show the MATLAB Code and some of the results like P_{loss} $\left\{ \begin{array}{l} \text{conduction} \\ \text{overlap} \\ C_{oss} \end{array} \right\}$ and Temperature [before and after iteration]

General Coding from the default:

```
% Rds_iteration 1st
Rds1_nosink = Rds * Rds_T(Tj1_nosink);
Rds2_nosink = Rds * Rds_T(Tj2_nosink);

% Circuit parameters
Vin = 20;
Vin_min = 16;
Vin_max = 24;
Vout = 12;
P_min = 50;
P_max = 100;
P = P_max;
IL_max = P_max/Vout;
IL_min = P_min/Vout;
IL = IL_max;
Tamb = 25;

Rds1_heatsink = Rds * Rds_T(Tj1_heatsink);
Rds2_heatsink = Rds * Rds_T(Tj2_heatsink);

% Iteration 1st for Ploss calculation
P_loss_cond1_nosink = D*IL^2*Rds1_nosink
P_loss_cond2_nosink = Dbar*IL^2*Rds2_nosink

P_loss_cond1_heatsink = *IL^2*Rds1_heatsink
P_loss_cond2_heatsink = Dbar*IL^2*Rds2_heatsink

Tj1_nosink = Tamb + (P_loss_cond1_nosink + P_loss_ov + P_loss_coss)*R_th_JA
Tj2_nosink = Tamb + P_loss_cond2_nosink*R_th_JA

Tj1_heatsink = Tamb + (P_loss_cond1_heatsink + + P_loss_ov + P_loss_coss)*R_parallel
Tj2_heatsink = Tamb + P_loss_cond2_heatsink*R_parallel

% Thermal Model: ***
R_th_JA = 62;
R_th_JC = 0.9;
R_th_CS = 0.5;
R_th_SA = 0.22;
R_parallel = R_th_JA*(R_th_JC+R_th_CS+R_th_SA)/(R_th_JA+R_th_JC+R_th_CS+R_th_SA);

% Switches parameters -- For IRFZ34NpbF
% Coss vs Vds
Vdd = 20; % Voltage at which we want to linearize capacita
```

```
Data=[ 0.9628266749651312, 900.4843218110868
1.046917707721207, 876.605872479035
1.1969488136800037, 838.0372512661556
1.3781324308852323, 797.630974455484
1.620525962009465, 753.583816774714
2.0302258354118387, 692.967611324829
2.403876686337815, 650.6296183544127
2.846114353271883, 610.1799806924419
3.4172843882170858, 567.8797774887223
4.102817733669937, 527.4070794011014
5.28389378305395, 475.86416848863917
6.15545913210241, 433.49846400797054
9.267642072885504, 370.86319984501694
12.09753680812563, 332.08424431959713
15.35669801488527, 295.17615476157533
20.61252173849381, 258.1795035009545
31.1616747178382, 211.8617330418178
48.433885360498955, 170.97943707967738
];
x = Data(:,1);
y = Data(:,2);
plot(x,y,'x');
F = griddedInterpolant(x,y); % Interpolate data points
```

```
Coss_V = @(t) F(t); % Create function based on int
figure
plot(x, Coss_V(x)); % Plot function to make sure it
title("Coss-Vds curve")
xlabel("VDS (V)")
ylabel("C (pF)")

CossQ = integral(Coss_V, 0, Vdd); % Calculate c
vx = .01:01:Vdd;
Cx = 10.^interp1(x,log10(y),vx,"linear","extrap");
E = cumtrapz(vx,Cx.*vx);
CeqEcum = 2^(E)./vx.^2;
CeqE = CeqEcum(2000); % Calculate energy-equivalent
```

Sorry, but I've written 300~400 lines, which cannot be shown on this page and the next page

```
% Rds_iteration 1st
Rds1_nosink = Rds * Rds_T(Tj1_nosink);
Rds2_nosink = Rds * Rds_T(Tj2_nosink);

Rds1_heatsink = Rds * Rds_T(Tj1_heatsink);
Rds2_heatsink = Rds * Rds_T(Tj2_heatsink);

% Iteration 1st for Ploss calculation
P_loss_cond1_nosink = D*IL^2*Rds1_nosink
P_loss_cond2_nosink = Dbar*IL^2*Rds2_nosink

P_loss_cond1_heatsink = *IL^2*Rds1_heatsink
P_loss_cond2_heatsink = Dbar*IL^2*Rds2_heatsink

Tj1_nosink = Tamb + (P_loss_cond1_nosink + P_loss_ov + P_loss_coss)*R_th_JA
Tj2_nosink = Tamb + P_loss_cond2_nosink*R_th_JA

Tj1_heatsink = Tamb + (P_loss_cond1_heatsink + + P_loss_ov + P_loss_coss)*R_parallel
Tj2_heatsink = Tamb + P_loss_cond2_heatsink*R_parallel

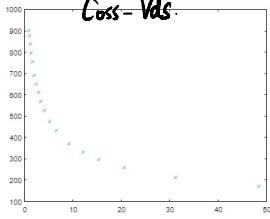
% I choose to use heatsink
P_loss1 = P_loss_cond1_heatsink+ P_loss_ov + P_loss_coss
P_loss2 = P_loss_cond2_heatsink

% nominal condition: Vin Vout P
D = Vout/Vin;
Dbar = 1-D;
P_loss_cond1 = D*IL^2*Rds;
P_loss_cond2 = Dbar*IL^2*Rds;

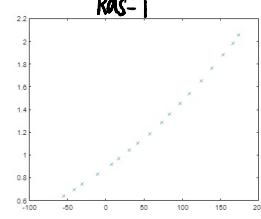
P_loss1 = P_loss_cond1 + P_loss_ov + P_loss_coss;
P_loss2 = P_loss_cond2;

% junction Temperature
Tj1_nosink = Tamb + P_loss1*R_parallel;
Tj2_nosink = Tamb + P_loss2*R_parallel;
```

Coss-Vds



Rds-T



① IRFZ34NPBF

P_loss_cond1_nosink = 2.9193
P_loss_cond2_nosink = 1.5866
P_loss_cond1_heatsink = 1.7253
P_loss_cond2_heatsink = 1.1386
Tj1_nosink = 214.3021
Tj2_nosink = 123.3710
Tj1_heatsink = 30.1848
Tj2_heatsink = 28.1752
P_loss1 = 1.8592
P_loss2 = 1.1386
eta_norminal = 0.9700
eta_v1 = 0.9698
eta_v2 = 0.9842
eta_v3 = 0.9701
eta_v4 = 0.9846
eta_score = 0.9743

② IRL3705NPBF

P_loss_cond1_nosink = 0.5494
P_loss_cond2_nosink = 0.3022
P_loss_cond1_heatsink = 0.4174
P_loss_cond2_heatsink = 0.2768
Tj1_nosink = 88.5339
Tj2_nosink = 43.7346
Tj1_heatsink = 26.4095
Tj2_heatsink = 25.4370
P_loss1 = 0.8928
P_loss2 = 0.2768
eta_norminal = 0.9883
eta_v1 = 0.9875
eta_v2 = 0.9903
eta_v3 = 0.9891
eta_v4 = 0.9919
eta_score = 0.9891

③ IRFZ48NPBF

P_loss_cond1_nosink = 0.8164
P_loss_cond2_nosink = 0.4522
P_loss_cond1_heatsink = 0.5920
P_loss_cond2_heatsink = 0.3925
Tj1_nosink = 93.6055
Tj2_nosink = 53.0333
Tj1_heatsink = 26.6014
Tj2_heatsink = 25.7125
P_loss1 = 0.8822
P_loss2 = 0.3925
eta_norminal = 0.9873
eta_v1 = 0.9868
eta_v2 = 0.9913
eta_v3 = 0.9877
eta_v4 = 0.9923
eta_score = 0.9886

④ IRLZ44NPBF

P_loss_cond1_nosink = 1.3765
P_loss_cond2_nosink = 0.7588
P_loss_cond1_heatsink = 0.9247
P_loss_cond2_heatsink = 0.6122
Tj1_nosink = 126.6619
Tj2_nosink = 72.0456
Tj1_heatsink = 27.4351
Tj2_heatsink = 26.2549
P_loss1 = 1.1879
P_loss2 = 0.6122
eta_norminal = 0.9820
eta_v1 = 0.9816
eta_v2 = 0.9888
eta_v3 = 0.9824
eta_v4 = 0.9896
eta_score = 0.9842

10:00 - 12:30 4h 6:30 + 8~9h

3705 = 98.91% ✓

Z48N = 98.86%

Z44N = 98.42% ✓

Z34N = 97.43%

* η -efficiency represents the total loss

Marketplace Switch and Heat Sink Selection

A realistic component selection process involves searching existing marketplaces for an “optimal” component based on loss, size, cost, and/or a number of other factors. One such marketplace is DigiKey, which sells a variety of electronics parts and test equipment. On DigiKey, conduct a search for an “optimal” power FET and heat sink pair for your buck converter design. You may assume you are interested in an n-channel FET in a TO-220 package, and filter your searches accordingly.

Note: Optimal component selection can take a very long time. You may limit each search to 30 minutes, assuming you are using a script to quickly calculate loss.

1. The most efficient power FET in a TO-220 family package for your high-side switch.
2. The smallest (by box volume) heat sink that will keep this FET’s on-state resistance within 20% of its value at 25 °C.

(1) From above, they are all TO-220 packages

(2) maybe 7 inch³ $\xleftarrow{\text{0.22 W-m}^{-2}/\text{C}}$

IRL3705NPBF is the best

And the lab is only 2 days after the lecture, it's really tight.

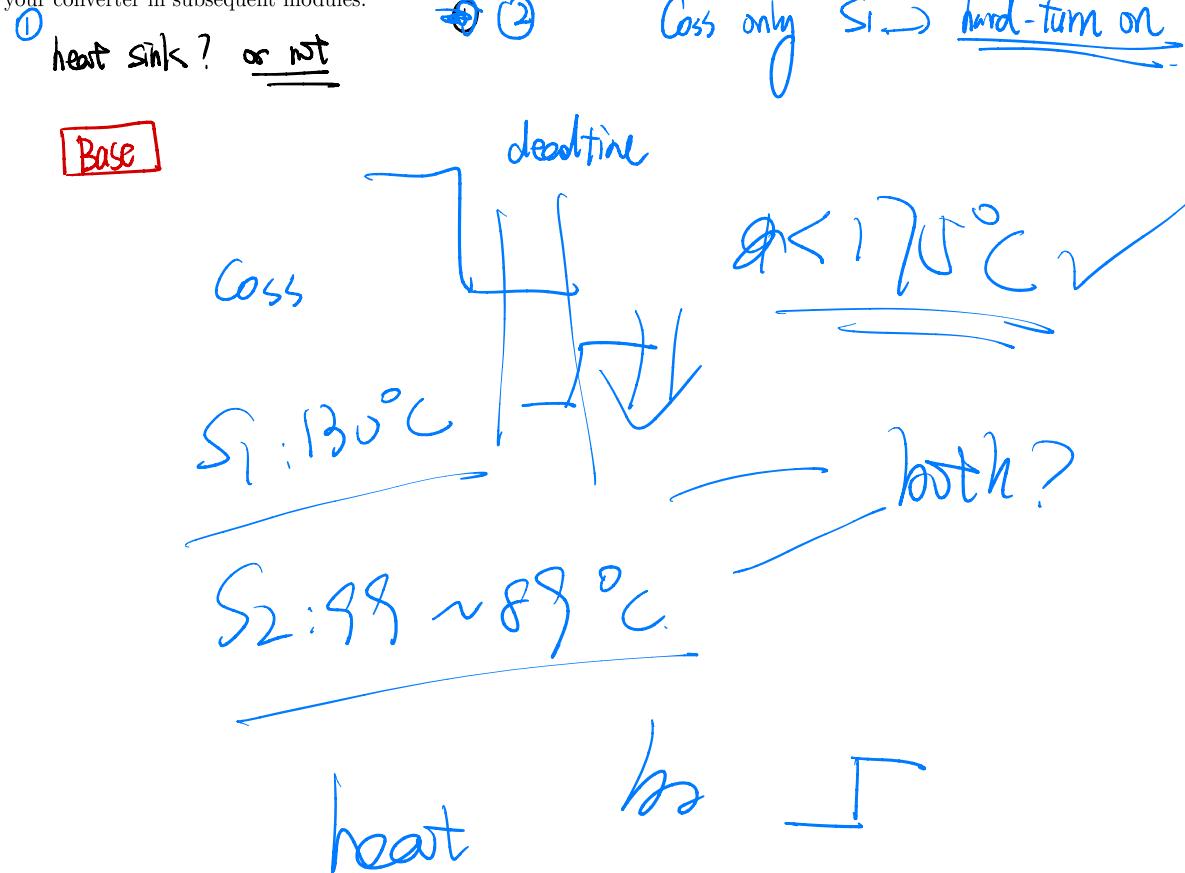
Next time maybe divide into 2 lab-times.]

Switch Selection

Consider the selection of other power transistors in the parts library on bCourses (datasheets are provided in a .zip folder under this module). Select (a) the most appropriate power transistor parts for your buck converter design based on power loss, voltage rating, etc., and (b) whether or not each switch will have a heat sink. You may choose to implement your switches with the same part or different parts, each with or without a heatsink. To help you make this selection, you should calculate expected loss at the nominal operating point and at all four corner operating points, considering each switch's actual $R_{ds,on}$ with or without the heatsink. (If you choose to use two different power transistor parts, you must consider how this affects the C_{oss} loss calculation) (i.e., use of both charge- and energy-equivalent capacitance). Based on total loss, you should ensure that the junction temperature of each switch is within its acceptable operating temperature range for all five relevant operating points. If helpful, you may assume your converter's final efficiency score will be evaluated as follows:

$$\eta_{score} = 0.4(\eta_{nominal}) + 0.15(\eta_{corner,1}) + 0.15(\eta_{corner,2}) + 0.15(\eta_{corner,3}) + 0.15(\eta_{corner,4}) \quad (1)$$

For the parts and heatsink configurations you choose, provide junction temperatures and a final loss breakdown at the nominal operating point and all four corner operating points. These will be the parts you use to build your converter in subsequent modules.



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Marketplace Switch and Heat Sink Selection

A realistic component selection process involves searching existing marketplaces for an “optimal” component based on loss, size, cost, and/or a number of other factors. One such marketplace is DigiKey, which sells a variety of electronics parts and test equipment. On DigiKey, conduct a search for an “optimal” power FET and heat sink pair for your buck converter design. You may assume you are interested in an n-channel FET in a TO-220 package, and filter your searches accordingly.

Note: Optimal component selection can take a very long time. You may limit each search to 30 minutes, assuming you are using a script to quickly calculate loss.

1. The most efficient power FET in a TO-220 family package for your high-side switch.
2. The smallest (by box volume) heat sink that will keep this FET’s on-state resistance within 20% of its value at 25 °C.

Download PLECS

PLECS is a widely used time-domain power circuit simulation tool. Instructions for downloading PLECS and obtaining a license are as follows:

1. Download ‘PLECS Standalone’ from <https://plexim.com/download/standalone>
2. Start PLECS without a license file. In the dialog box that appears click ‘Open license manager’ then ‘Request license.’ Select ‘Student license,’ enter the student license code **7Nf-CnvtPfqh**. Select ‘PLECS Combo’ as the ‘Base Product’ and ‘PLECS Coder’ as an ‘Add-on Product.’ Click ‘Open web form.’
3. A webpage will open with your hostID already populated. Fill out the personal contact information using your *berkeley.edu* email address. Submit the form and check your email for the license file.
4. Once you receive the license file, save the file anywhere on your machine.
5. Re-open PLECS. In the dialog box that appears click ‘Manage license files’ and then click ‘Install.’ Navigate to the license file you just downloaded and select it. Then click ‘Save.’ You should now be ready to use PLECS.

Additional resources can be found at <https://plexim.com/support/tutorials>.

NOTE: Your PLECS Student License is only valid for one machine per student and you cannot use PLECS through a remote desktop connection, so choose a machine you will have access to throughout the semester.

Assignment Feedback (Required)

How much dedicated time did you spend on this pre-lab?

Lab Assignment

Once you have sized (and perhaps selected) components for a power converter design, it is good practice to simulate its operation and compare the behavior to your calculations. In the next several sections, we will first simulate our designs with ideal circuit components and then incorporate non-idealities for realistic operation.

Switch Block for Simulation

In PLECS, modeling of power FETs and other subsystems can be streamlined using ‘Custom Subsystems’, which allow the designer to create reusable components that can be associated with multiple schematics or configurations. Such subsystems are particularly useful for creating ‘switch blocks’, which can consist of just an ideal switch (Fig. 2) or may be modified to include parasitics (Fig. 3).

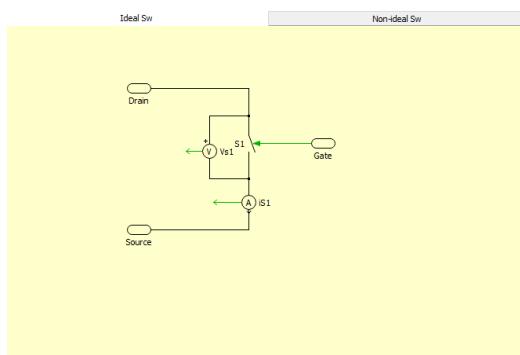


Figure 2: Sub-circuit for an ideal switch.

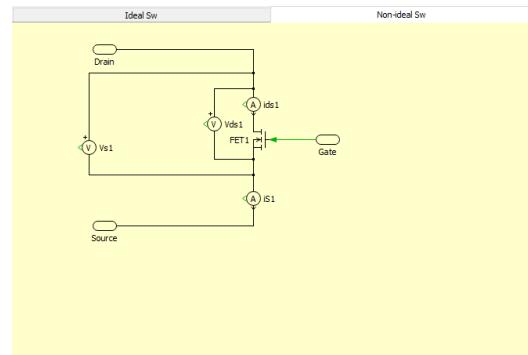


Figure 3: An **INCOMPLETE** sub-circuit for a non-ideal switch.

Custom Subsystems: For information about creating subsystems, refer to the *Subsystems* Section beginning on page 63 of <https://www.plexim.com/sites/default/files/plecsmanual.pdf> and the video tutorial series <https://www.plexim.com/support/videos/custom-component-part-1>

1. Download the ‘SwitchBlock.plecs’ file from bCourses and add to a file directory of your choice.
2. Add the ‘SwitchBlock.plecs’ file as a library file in PLECS.
 - (a) Navigate to *File/PLECS Preferences/Libraries*.
 - (b) Add (click + symbol) the file directory where you saved the ‘SwitchBlock.plecs’ file to the ‘Search path’.
 - (c) Add (click + symbol) the file ‘SwitchBlock.plecs’ file to the ‘User libraries’.
 - (d) This block can now be added to your canvas from the library under ‘User libraries’
3. Construct a model (Fig. 4) for a synchronous buck converter in PLECS.

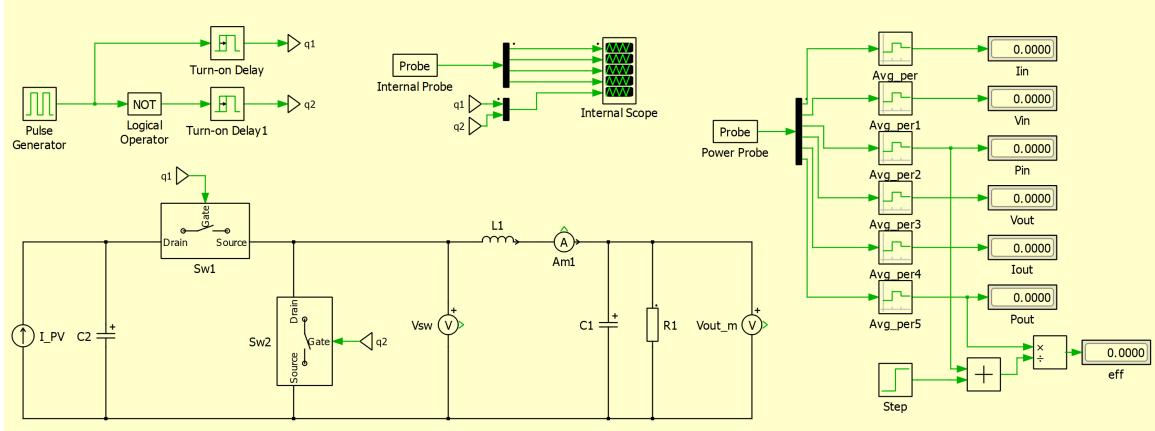


Figure 4: Buck Converter PLECS schematic.

Note: The measurements/displays aren't required, but are useful for evaluating circuit operation. You can drag the custom switch blocks to the probe to access the various probes that are within the block. When using a 'Periodic Average' block, what averaging time makes sense to use?

Ideal Simulation

Now, simulate your ideal synchronous buck converter using the component sizes you selected in Module 0. For the configurable switch blocks, double-click each block and select *Configuration/Ideal Sw*. You can ignore the 'Parameters' for now. **Make sure to define the deadtime ('Turn-on Delay' block) as 0 [s].** Based on your converter simulation, determine the following:

1. The efficiency of your power converter at the nominal operating point and at each corner operating point.
2. The maximum peak-to-peak ripple (as a percentage) on v_{out} , considering the entire operating range.
3. The maximum peak-to-peak ripple (as a percentage) on i_L , considering the entire voltage range at full power.
4. The maximum voltage stress on each of your switches, considering the entire operating range.
5. The maximum current stress on each of your switches, considering the entire operating range.

PLECS Tip: If waveforms look jagged instead of smooth, try increasing the refine factor. A higher refine factor improves the rendering of an output from the scope without increasing simulation time. The refine factor can be set in the Solver pane of the Simulation Parameter window. A refine factor less than 10 is recommended.

Check-off: Confirm (a) that chosen components satisfy ripple requirements and can tolerate maximum stress, and (b) that your switch selections are appropriate for your design.

Simulation with Switch Parasitics

Now, let's add switch parasitics to your simulation for the final parts you selected from our library in the pre-lab of this module. To do this, modify the 'Custom Subsystem' switch blocks according to the instructions detailed below. Add circuit components for modeling switch $R_{ds,on}$, C_{oss} , and the switch's body diode.

1. Open the 'SwitchBlock.plecs' file.
2. Right-click the block and navigate to *Subsystem/Unprotect*. Click 'Unprotect' to make the module editable.
3. Right-click the block and navigate to *Subsystem/Edit Mask*. On the 'Dialog' tab, make note of the variables and their names. You will need to assign these variables as parameters for the parasitic component you add.

Ideal Simulation

Now, simulate your ideal synchronous buck converter using the component sizes you selected in Module 0. For the configurable switch blocks, double-click each block and select *Configuration/Ideal Sw*. You can ignore the ‘Parameters’ for now. **Make sure to define the deadtime (‘Turn-on Delay’ block) as 0 [s].** Based on your converter simulation, determine the following:

1. The efficiency of your power converter at the nominal operating point and at each corner operating point.
2. The maximum peak-to-peak ripple (as a percentage) on v_{out} , considering the entire operating range.
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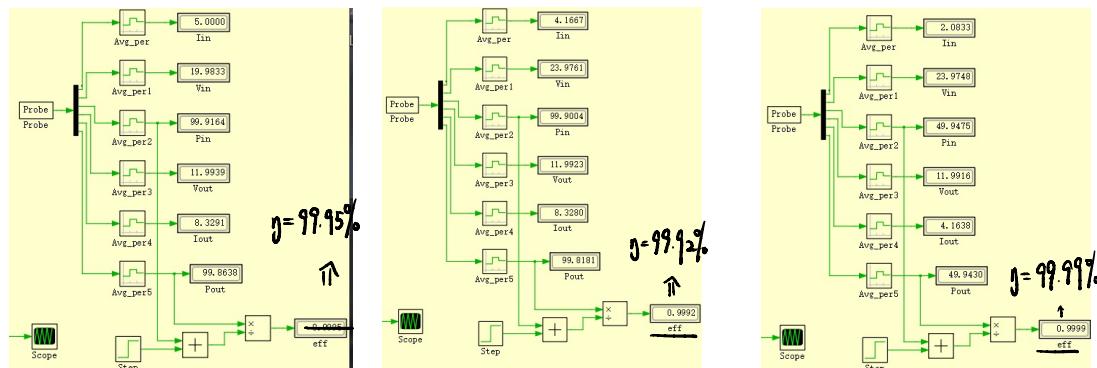
Check-off: Confirm (a) that chosen components satisfy ripple requirements and can tolerate maximum stress, and (b) that your switch selections are appropriate for your design.

4)

1. nominal operating points

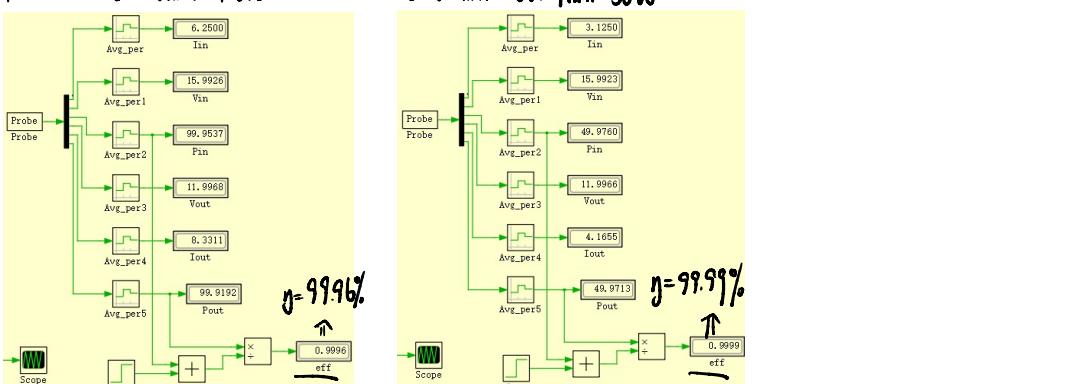
2. $V_{in \ max}, P_{max}$
 $= 24V = 100W$

3. $V_{in \ max} = 24V, P_{min} = 50W$

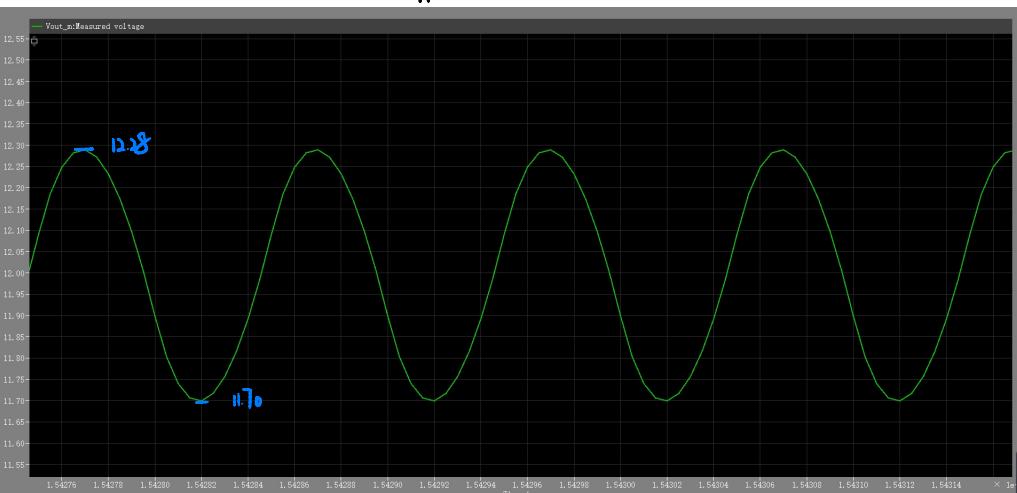


4. $V_{in \ min} = 16V, P_{max} = 100W$

5. $V_{in \ min} = 16V, P_{min} = 50W$

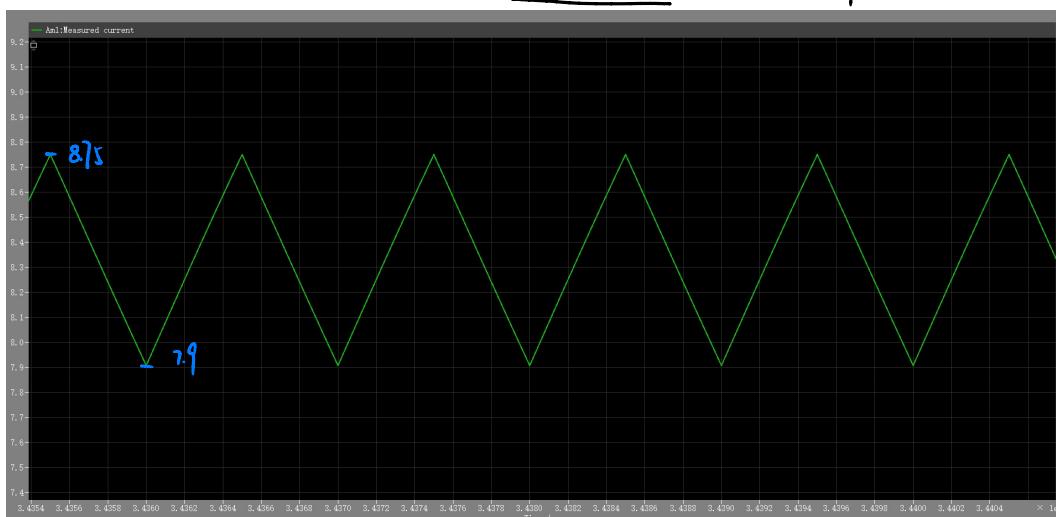


(2). V_{out} ripple: (worst-case) — $V_{in\ max} = 24V$. \downarrow $P_{min} = 50W \Rightarrow I_L\ min.$ $\text{ripple \% } = \frac{12.28 - 11.70}{12} = 0.58A \approx 4.83\%$
ripple max. $\approx 5\% \text{ ideally}$



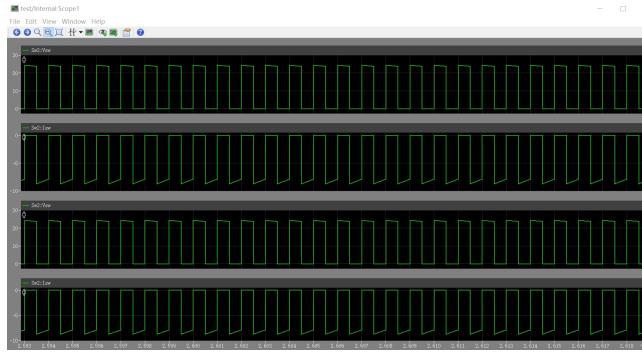
pp max

3. i_L ripple $\langle i_L \rangle = \frac{P_{out}}{V_{out}} = \frac{100}{12} \approx 8.34$ ideal & real: $\langle i_L \rangle = 8.3219$ $\text{ripple} = \frac{8.75 - 7.9}{8.3219} = 0.85A \approx 10.21\%$.

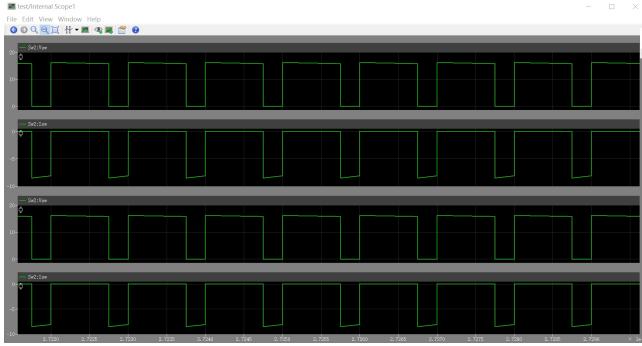


All of the ripples on switches:

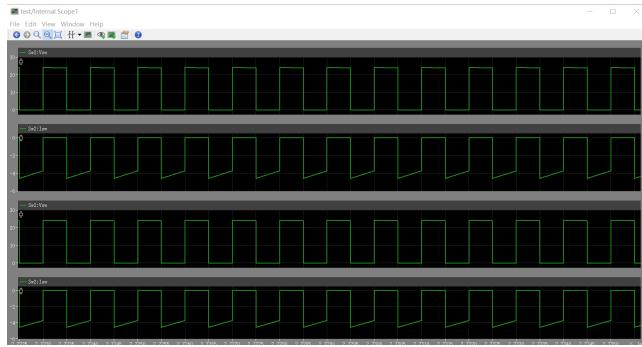
$$P=100\text{W}, V_{in}=24\text{V}$$



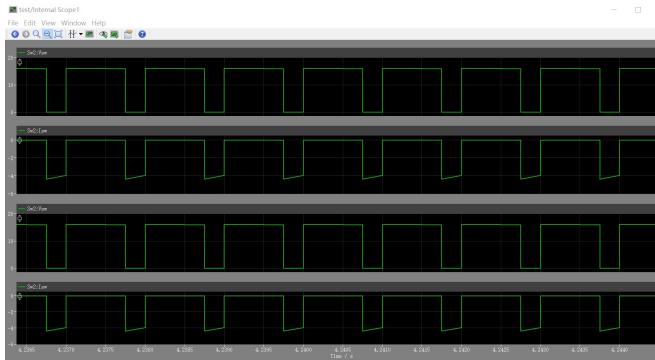
$$V_{in}=16\text{V}, P=100\text{W}$$



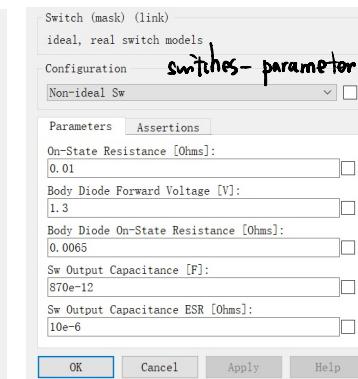
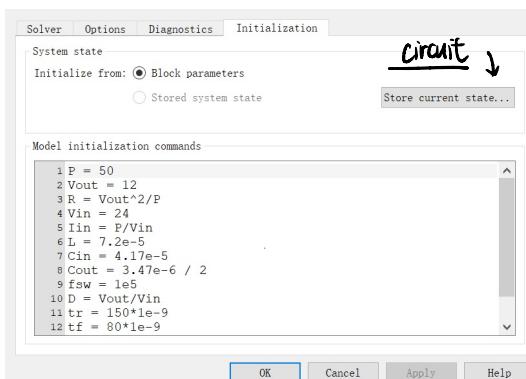
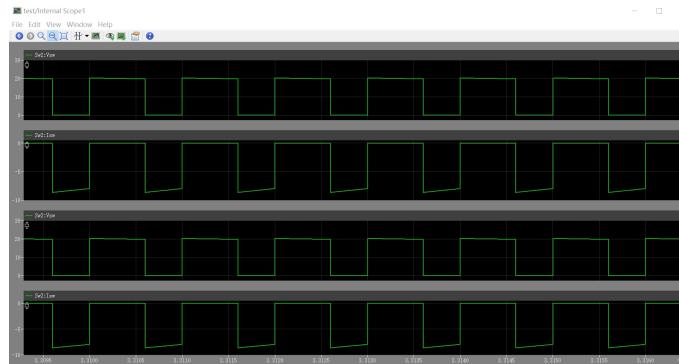
$$V_{in}=24\text{V}, P=50\text{W}$$



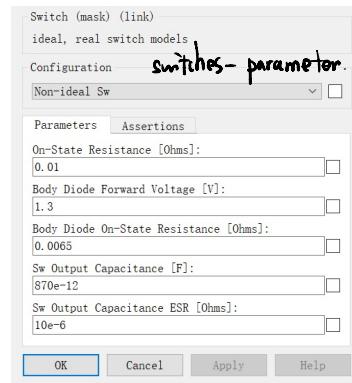
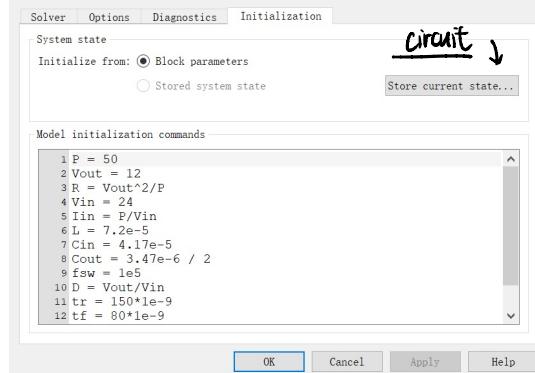
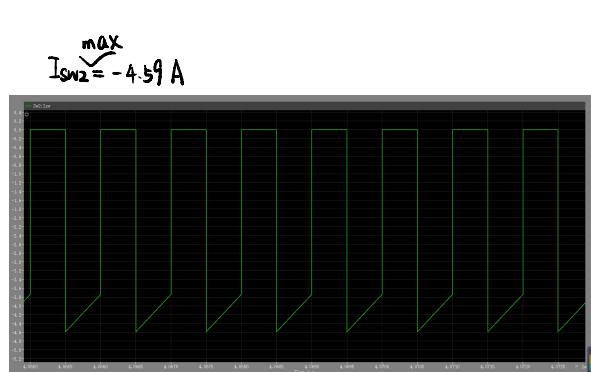
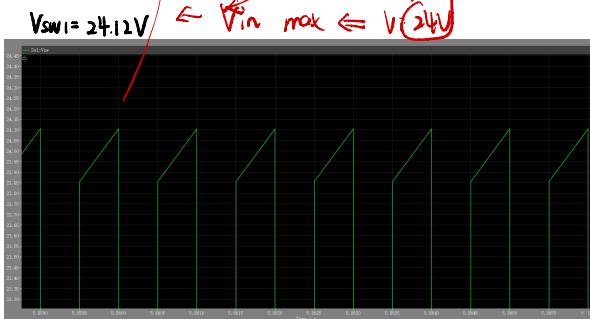
$V_{in}=16V$, $P=50W$



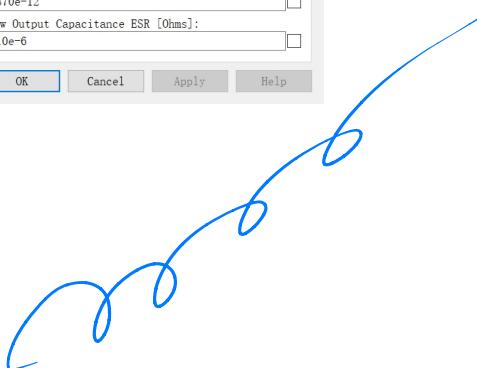
$V_{in}=20V$, $P=100W$ norminal situation



= parameters given



= parameters given

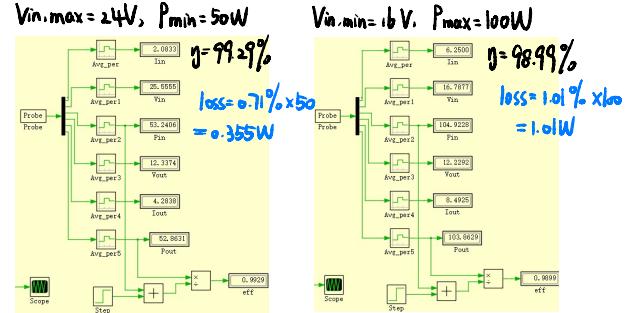
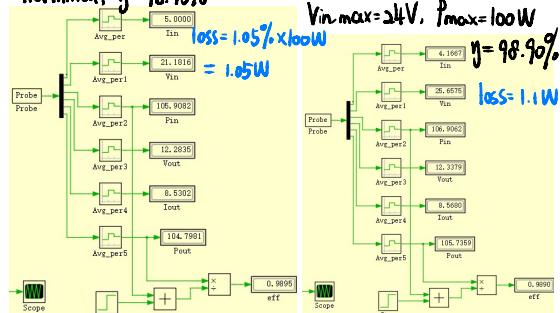


↓ All switch nippes 截圖

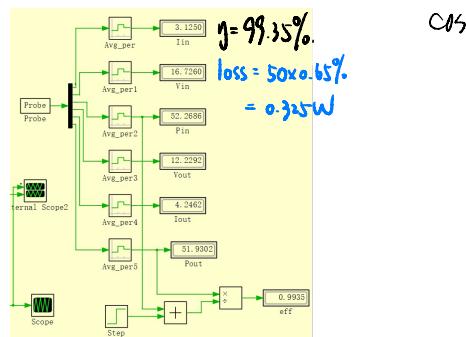
Simulation with parasitics:

- The efficiency of your power converter.
- The maximum voltage and current stresses on each of your switches, considering the entire operating range.

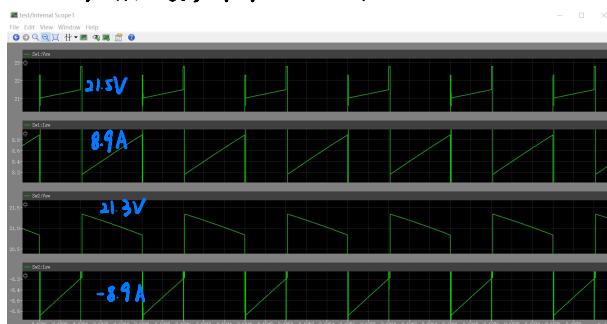
nominal, $\eta = 98.95\%$



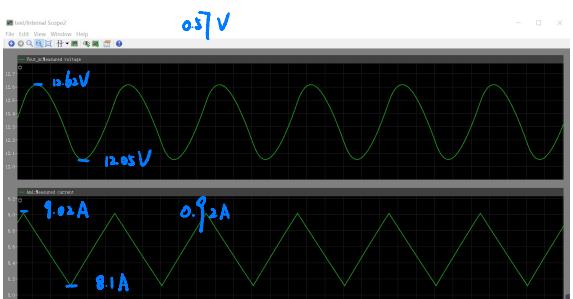
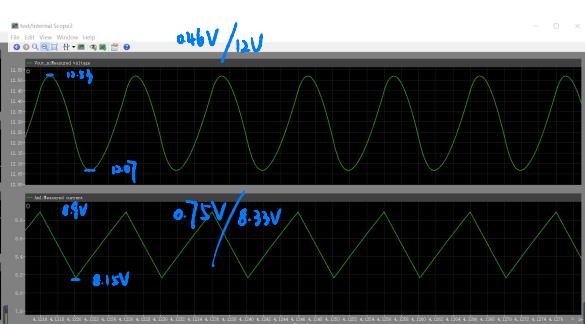
$V_{in,min} = 16V, P_{min} = 50W$



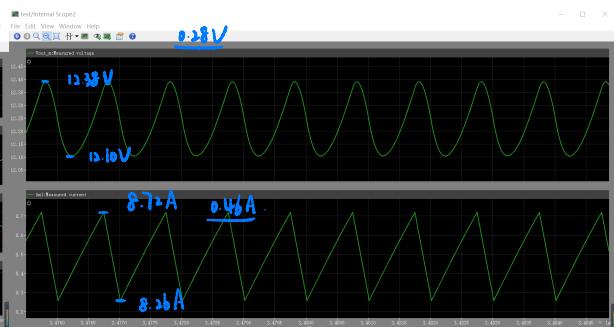
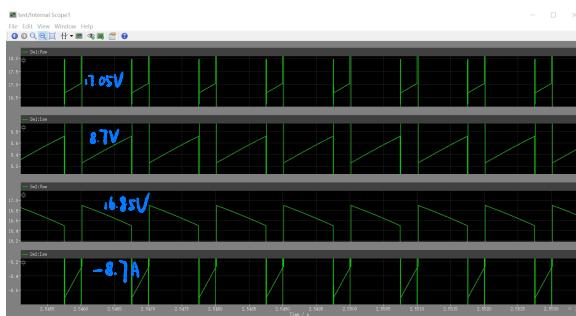
nominal: $V_{in} = 20V, P = 100W$. Stresses.



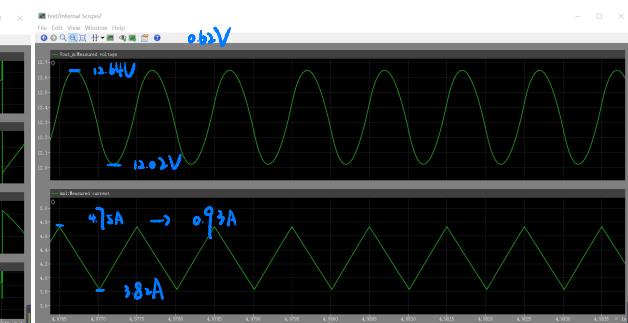
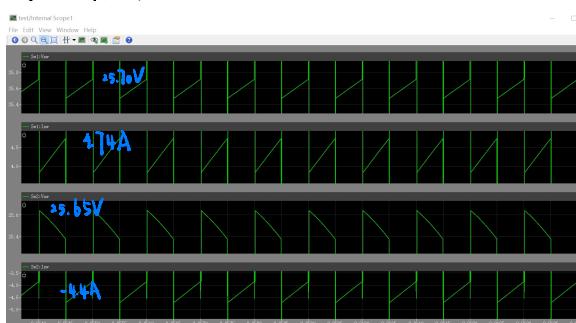
$V_{in} = 24V, P = 100W$



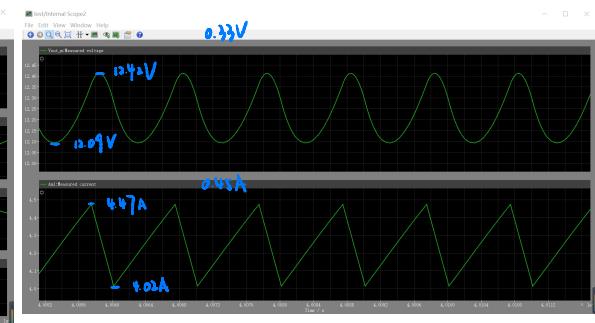
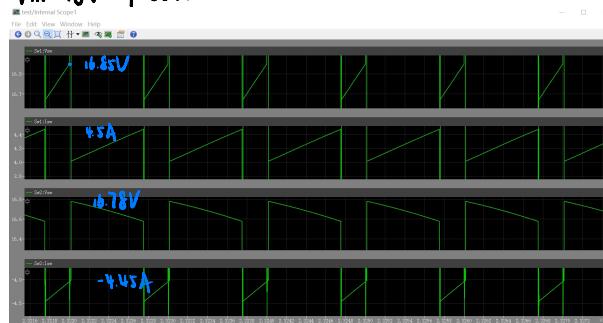
$V_{in}=16V$, $P=100W$



$V_{in}=24V$, $P=50W$.



$V_{in}=16V$, $P=50W$



1. Total converter losses, based on measured efficiency. \rightarrow seen before.

2. RMS current for each switch.

PLECS Tip: Use probe and RMS blocks. What sampling time makes sense to get a good rms estimate? Because we are not modeling all circuit parasitics, there will be very large voltage/current spikes on the switches. For the conduction loss estimate, you can ignore the large spikes in switch current, so try different sampling times until you get a 'reasonable' rms measurement.

3. Conduction losses for each switch.

4. Switching losses (as the remaining losses). $V_{out} = 12V$

$$(2) I_{rms,1} = \sqrt{D} \cdot I_L$$

$$I_{rms,2} = \sqrt{D} \cdot I_L$$

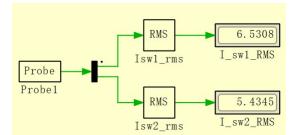
$$\text{nominal}$$

$$\textcircled{1} V_{in}=20V, P=100W$$

$$D=0.6$$

$$I_{rms,1} = \sqrt{0.6} \times \frac{100}{12} = 6.46 \text{ Arms}$$

$$I_{rms,2} = \sqrt{0.4} \times \frac{100}{12} = 5.27 \text{ Arms}$$

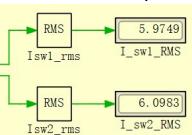


$$\textcircled{2} V_{in}=24V, P=100W$$

$$D=0.5$$

$$I_{rms,1} = \sqrt{0.5} \times \frac{100}{12} = 5.89 \text{ Arms}$$

$$I_{rms,2} = \sqrt{0.5} \times \frac{100}{12} = 5.89 \text{ Arms}$$

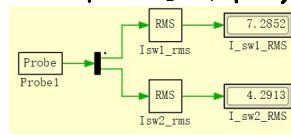


$$\textcircled{3} V_{in}=16V, P=100W$$

$$D=0.75$$

$$I_{rms,1} = \sqrt{0.75} \times \frac{100}{12} = 7.22 \text{ Arms}$$

$$I_{rms,2} = \sqrt{0.25} \times \frac{100}{12} = 4.17 \text{ Arms}$$

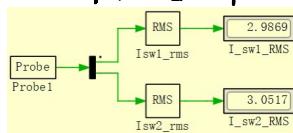


$$\textcircled{4} V_{in}=24V, P=50W$$

$$D=0.5$$

$$I_{rms,1} = \sqrt{0.5} \times \frac{50}{12} = 2.95 \text{ Arms}$$

$$I_{rms,2} = \sqrt{0.5} \times \frac{50}{12} = 2.95 \text{ Arms}$$

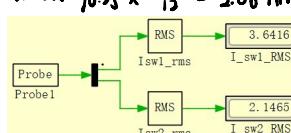


$$\textcircled{5} V_{in}=16V, P=50W$$

$$D=0.75$$

$$I_{rms,1} = \sqrt{0.75} \times \frac{50}{12} = 3.61 \text{ Arms}$$

$$I_{rms,2} = \sqrt{0.25} \times \frac{50}{12} = 2.08 \text{ Arms}$$



$$(3) P_{cond,loss} = I_{rms}^2 \cdot Rds.on$$

$$P_{sw,loss} = (P_{ov} + P_{oss})$$

$$= P_{total} - P_{cond,loss}$$

```
% nominal Vin=20V P=100W [real situation]
P_loss_total = 1.05*1e-2 * 100
I_rms_1 = 6.5308;
I_rms_2 = 5.4345;
Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on
P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1
P_sw_2 = P_loss_total - P_cond_2

% Vin=24V P=100W [real situation]
P_loss_total = 1.1
I_rms_1 = 5.9749;
I_rms_2 = 6.0983;
Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on
P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1
P_sw_2 = P_loss_total - P_cond_2

% Vin=24V P=50W [real situation]
P_loss_total = 0.355
I_rms_1 = 2.9869;
I_rms_2 = 3.0517;
Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on
P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1
P_sw_2 = P_loss_total - P_cond_2
```

Real Situation:

<pre>% Vin=16V P=100W [real situation] P_loss_total = 1.0500 I_rms_1 = 7.2852; I_rms_2 = 4.2913; Rds_on = 0.01; P_cond_1 = I_rms_1^2 * Rds_on P_cond_2 = I_rms_2^2 * Rds_on P_sw_1 = P_loss_total - P_cond_1 P_sw_2 = P_loss_total - P_cond_2</pre>	<pre>% Vin=16V P=50W [real situation] P_loss_total = 0.325 I_rms_1 = 3.6416; I_rms_2 = 2.1465; Rds_on = 0.01; P_cond_1 = I_rms_1^2 * Rds_on P_cond_2 = I_rms_2^2 * Rds_on P_sw_1 = P_loss_total - P_cond_1 P_sw_2 = P_loss_total - P_cond_2</pre>	<pre>P_loss_total = 0.3250 P_cond_1 = 0.1336 P_cond_2 = 0.0461 P_sw_1 = 0.1924 P_sw_2 = 0.2278</pre>
<pre>P_loss_total = 0.3550 P_cond_1 = 0.0892 P_cond_2 = 0.0931 P_sw_1 = 0.2658 P_sw_2 = 0.2619</pre>		

% nominal Vin=20V P=100W [real situation]

P_loss_total = 1.05*1e-2 * 100

I_rms_1 = 6.5308;

I_rms_2 = 5.4345;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on

P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1

P_sw_2 = P_loss_total - P_cond_2

% Vin=24V P=100W [real situation]

P_loss_total = 1.1

I_rms_1 = 5.9749;

I_rms_2 = 6.0983;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on

P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1

P_sw_2 = P_loss_total - P_cond_2

% Vin=24V P=80W [real situation]

P_loss_total = 0.355

I_rms_1 = 2.9869;

I_rms_2 = 3.0517;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on

P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1

P_sw_2 = P_loss_total - P_cond_2

% Vin=16V P=100W [real situation]

P_loss_total = 1.01

I_rms_1 = 7.2852;

I_rms_2 = 4.2913;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on

P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1

P_sw_2 = P_loss_total - P_cond_2

% Vin=16V P=80W [real situation]

P_loss_total = 0.325

I_rms_1 = 3.6416;

I_rms_2 = 2.1465;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on

P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1

P_sw_2 = P_loss_total - P_cond_2

conduction and switching loss

P_loss_total = 1.0500

P_loss_cond1 = D*IL^2*Rds

P_loss_cond2 = Dbar*IL^2*Rds

P_sw_1 = P_loss_cond1 + P_loss_ov + P_loss_coss

P_sw2 = P_loss2 - P_loss_cond2

P_loss_total = 1.1000

P_loss_cond1 = D*IL^2*Rds

P_loss_cond2 = Dbar*IL^2*Rds

P_loss1 = P_loss_cond1 + P_loss_ov + P_loss_coss

P_loss2 = P_loss_cond2

P_sw1 = P_loss1 - P_loss_cond1

P_sw2 = P_loss2 - P_loss_cond2

P_loss_total = 0.3550

P_loss_cond2 = Dbar*IL^2*Rds

P_loss_cond1 = P_loss_cond1 + P_loss_ov + P_loss_coss

P_loss2 = P_loss_cond2

P_sw1 = P_loss1 - P_loss_cond1

P_sw2 = P_loss2 - P_loss_cond2

P_loss_total = 1.0100

P_loss_cond1 = D*IL^2*Rds

P_loss_cond2 = Dbar*IL^2*Rds

P_loss1 = P_loss_cond1 + P_loss_ov + P_loss_coss

P_loss2 = P_loss_cond2

P_sw1 = P_loss1 - P_loss_cond1

P_sw2 = P_loss2 - P_loss_cond2

P_loss_total = 0.3250

P_loss_cond1 = 0.1326

P_loss_cond2 = 0.0461

P_sw1 = P_loss1 - P_loss_cond1

P_sw2 = P_loss2 - P_loss_cond2

% junction Temperature

Tj1_nosink = Tamb + P.loss1*R_th_JA;

Tj2_nosink = Tamb + P.loss2*R_th_JA;

P_loss_cond1 = 0.4187

P_loss_cond2 = 0.2778

P_sw1 = 0.8920

P_sw2 = 0.2778

P_sw1 = 0.4754

P_sw2 = 0

P_loss_cond1 = 0.3472

P_loss_cond2 = 0.3472

P_sw1 = 0.9338

P_sw2 = 0.3472

P_sw1 = 0.5865

P_sw2 = 0

P_loss_cond1 = 0.0868

P_loss_cond2 = 0.0868

P_sw1 = 0.4203

P_sw2 = 0.0868

P_sw1 = 0.3415

P_sw2 = 0

P_loss_cond1 = 0.5208

P_loss_cond2 = 0.1736

P_sw1 = 0.8904

P_sw2 = 0.1736

P_sw1 = 0.3696

P_sw2 = 0

P_loss_cond1 = 0.1302

P_loss_cond2 = 0.0434

P_sw1 = 0.3364

P_sw2 = 0.0434

P_sw1 = 0.2062

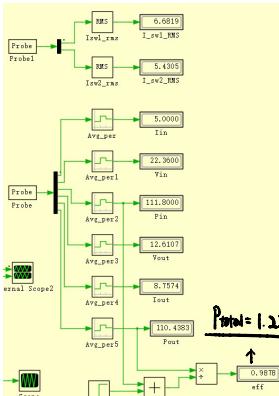
P_sw2 = 0

converter design tradeoff

- Simulate your converter for the same operating point as above but with twice the switching frequency. In PLECS, estimate your conduction losses and switching losses, and compare these to the losses of the previous section. Estimate the ripple on the inductor current, and compare this to the previous ripple. Are these differences predictable using calculations?

f_s : 100kHz \rightarrow 200kHz

Nominal Situation: Vin=20V, Pout=100W



% Vin=20V P=100W [real situation]

P_loss_total = 1.22

I_rms_1 = 6.6819;

I_rms_2 = 5.4305;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on
P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1 - P_cond_2
P_sw_2 = 0 % It's negelected

% Vin=20V P=100W [real situation]

P_loss_total = 1.05

I_rms_1 = 6.5308;

I_rms_2 = 5.4345;

Rds_on = 0.01;

P_cond_1 = I_rms_1^2 * Rds_on
P_cond_2 = I_rms_2^2 * Rds_on

P_sw_1 = P_loss_total - P_cond_1 - P_cond_2
P_sw_2 = 0 % It's negelected

2fs

P_loss_total = 1.2200

P_cond_1 = 0.4465

P_cond_2 = 0.2949

P_sw1 = 0.4786

P_sw2 = 0

P_loss_total = 1.0500

P_cond_1 = 0.4265

P_cond_2 = 0.2953

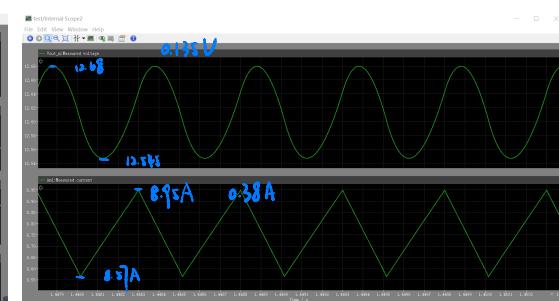
P_sw1 = 0.3281

P_sw2 = 0

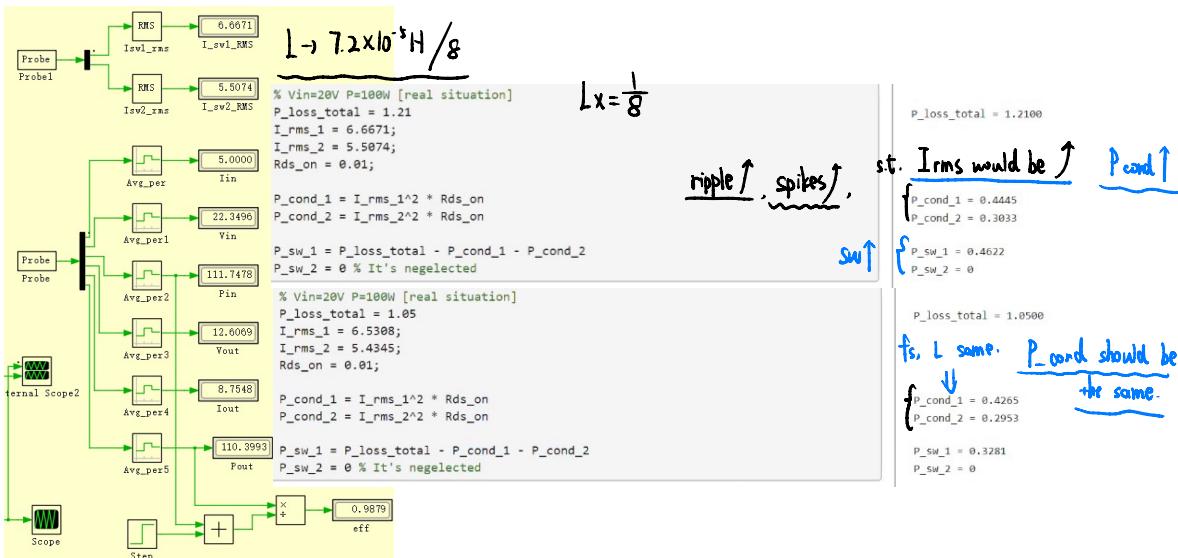
Smaller ripples



normal: $V_{in} = 20V, P = 100W$. STRESSES.



2. Simulate your converter for the same operating point as above but with 1/8 the inductor size. In PLECS, estimate your conduction losses and switching losses, and compare these to the losses of the previous section. Are these differences predictable using calculations?



3. The $R_{ds,on}$ and C_{oss} of a switch are closely related to its die size. Select a different switch with the same voltage rating but a significantly larger die size (i.e., higher current rating), and use it to simulate your converter. In PLECS, estimate your conduction losses and switching losses, and compare these to the losses of the previous section. How does the switch's $R_{ds,on}$ and C_{oss} compare to the switch you chose?

Use IRZ34NPBF, but smaller die size [29A]

$$R_{ds} = 0.04 \Omega, C_{oss,E} = 4.3254 \times 10^{-10} F \text{ (From MATLAB)}$$

$$C_{oss} = 240 pF$$

% Vin=38V Ps100W [real situation]

$$P_{loss_total} = 1.05$$

$$I_{rms_1} = 6.5308;$$

$$I_{rms_2} = 5.4345;$$

$$R_{ds_on} = 0.01;$$

$$P_{cond_1} = I_{rms_1}^2 * R_{ds_on}$$

$$P_{cond_2} = I_{rms_2}^2 * R_{ds_on}$$

$$P_{sw_1} = P_{loss_total} - P_{cond_1} - P_{cond_2}$$

$$P_{sw_2} = 0 \text{ % It's neglected}$$

% Vin=38V Ps100W [real situation]

$$P_{loss_total} = 3.2$$

$$I_{rms_1} = 6.6745;$$

$$I_{rms_2} = 5.5118;$$

$$R_{ds_on} = 0.04;$$

$$P_{cond_1} = I_{rms_1}^2 * R_{ds_on}$$

$$P_{cond_2} = I_{rms_2}^2 * R_{ds_on}$$

$$P_{sw_1} = P_{loss_total} - P_{cond_1} - P_{cond_2}$$

$$P_{sw_2} = 0 \text{ % It's neglected}$$

original

$$P_{loss_total} = 1.0500$$

$$\{ P_{cond_1} = 0.4265 \\ P_{cond_2} = 0.2953 \}$$

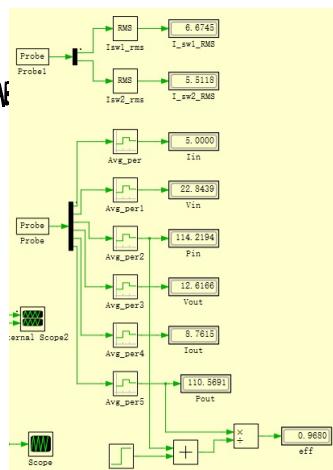
$$\{ P_{sw_1} = 0.3281 \\ P_{sw_2} = 0 \}$$

smaller die size.

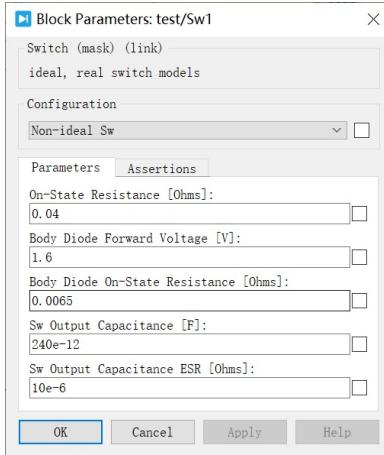
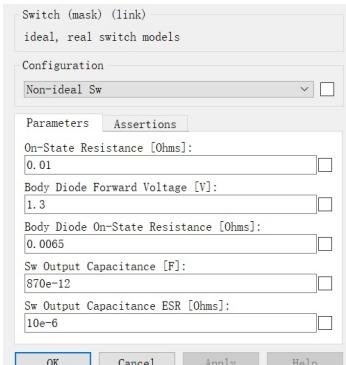
$$P_{loss_total} = 3.2000$$

$$\{ P_{cond_1} = 1.7820 \\ P_{cond_2} = 1.2152 \}$$

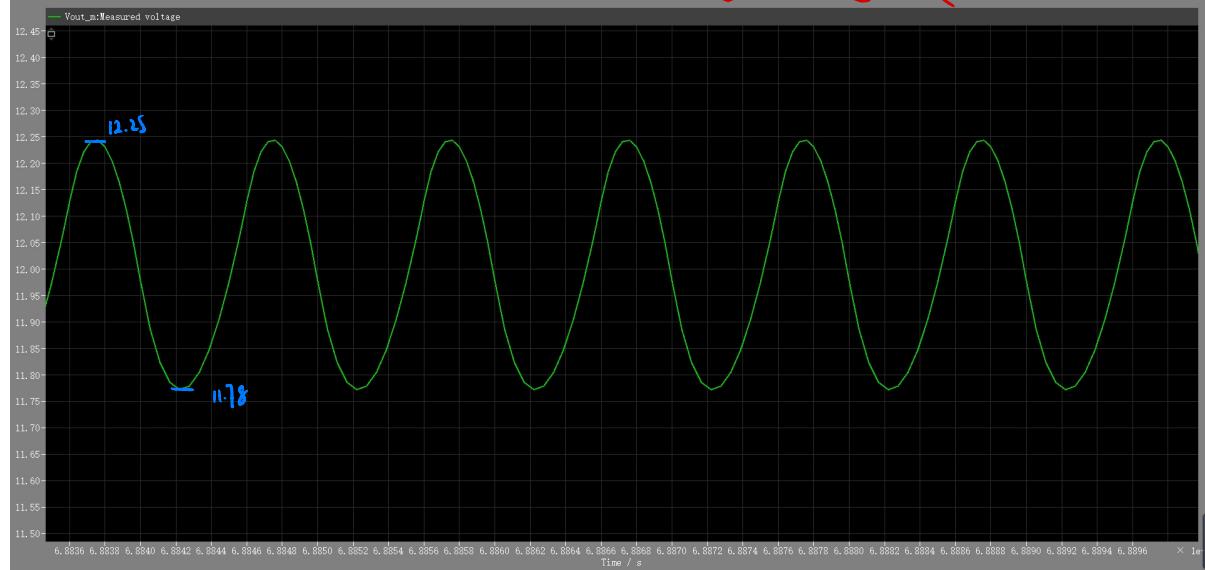
$$\{ P_{sw_1} = 0.2028 \\ P_{sw_2} = 0 \}$$



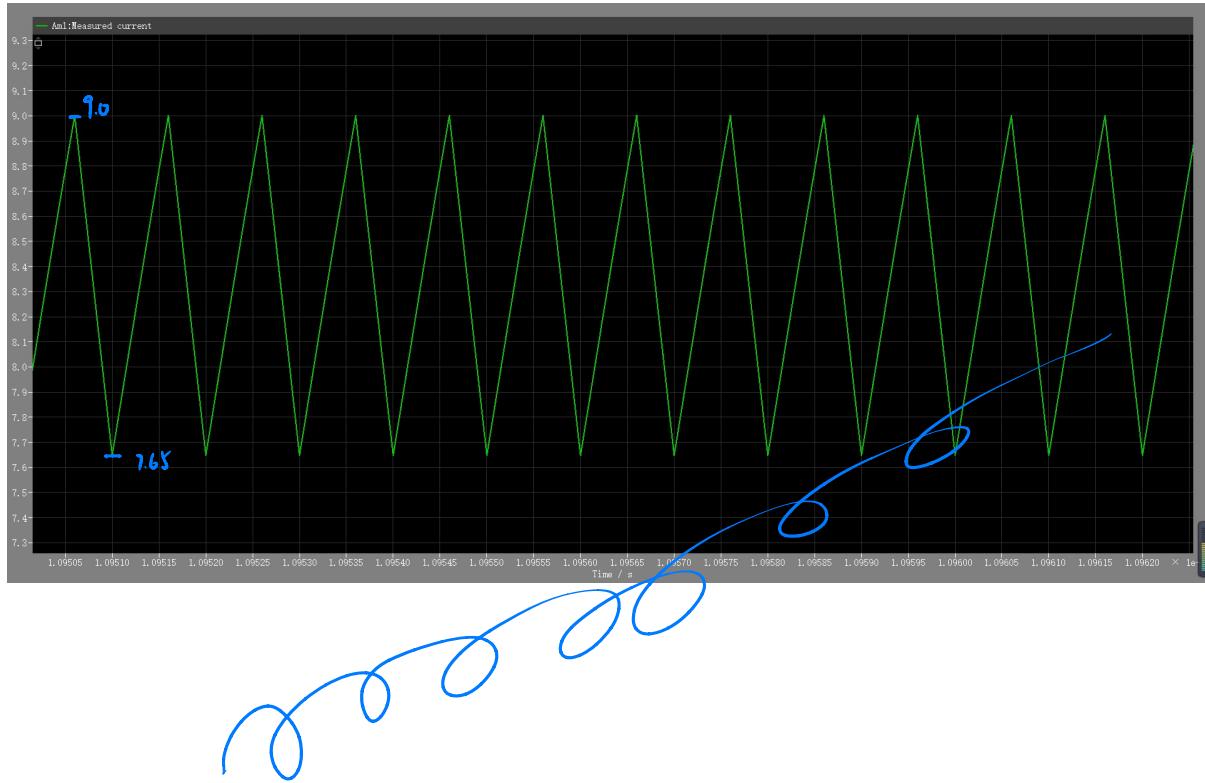
comparison on C_{oss} and $R_{ds, on}$.



2. Vout ripple - $\frac{12.25 - 11.78}{12} = \frac{0.47}{12} \approx 3.92\%$ worst-case X



3. iL ripple $\langle i_{L} \rangle = \frac{P_{out}}{V_{out}} = \frac{100}{12} \approx 8.33 \text{ A}$ & real: $\langle i_L \rangle = 8.3291$. Ripple: $\frac{9.0 - 7.65}{8.3291} = \frac{1.35}{8.3291} \approx 16.21\%$

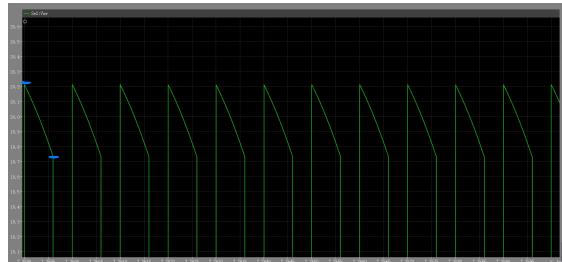
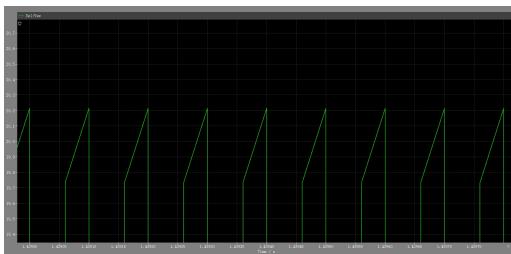


(4). Volt. stresses of S_1, S_2

Stress: 20.23V

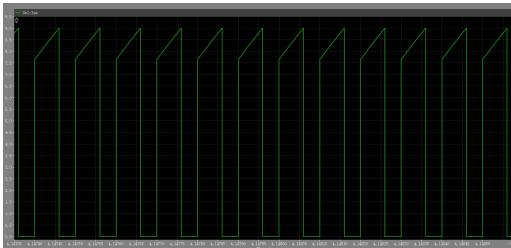
$$V_{S2} = 20.23 \text{ V}$$

X



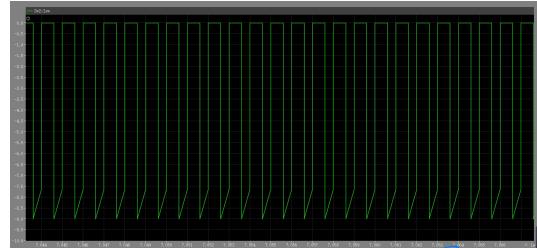
(5). Cur. stresses of S_1, S_2

$S_1: 9.0 \text{ A}$ $\langle I_1 \rangle \approx 833 \text{ A}$



$S_2: -9 \text{ A}$, $\langle I_{S2} \rangle = -833 \text{ A}$

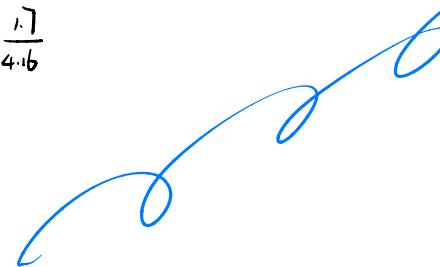
X



4.1638

3.0 - 3.3

$\frac{1.7}{4.6}$



- Right-click the block and navigate to *Subsystem/Look Under Mask*. Select the ‘Non-ideal Sw’ tab and add library components as usual. Assign variable names as parameters for the parasitic component you add.
- Save the SwitchBlock files.

PLECS Tip: You may notice that there is an additional variable defined in the Switch Block subsystem: ‘Sw Output Capacitance ESR’. Try simulating your converter without adding a series resistor in line with the switch output capacitance. What is the error?

Now add the ESR and re-run your simulation setting the ESR to $10\mu\Omega$.

Set the switch parameters by double-clicking each switch block and entering the appropriate information for your switch based on its datasheet. **Make sure to define the deadtime (‘Turn-on Delay’ block) as > 0 [s].** Find an appropriate deadtime to prevent the switches from conducting current at the same time. Simulate your circuit, and determine the following:

- The efficiency of your power converter.
- The maximum voltage and current stresses on each of your switches, considering the entire operating range.

Simulation-Based Loss Estimation

Based on your simulation, determine the following:

- Total converter losses, based on measured efficiency.
- RMS current for each switch.

PLECS Tip: Use probe and RMS blocks. What sampling time makes sense to get a good rms estimate? Because we are not modeling all circuit parasitics, there will be very large voltage/current spikes on the switches. For the conduction loss estimate, you can ignore the large spikes in switch current, so try different sampling times until you get a ‘reasonable’ rms measurement.

- Conduction losses for each switch.
- Switching losses (as the remaining losses).

Compare your total simulated loss to the total loss you calculated in the pre-lab. Determine which losses (if any) have been neglected in your simulation, and whether or not it is a valid assumption to neglect them.

Check-off: Confirm correct (a) switch model and model parameters, (b) simulated efficiency, (c) simulated voltage and current stresses, (d) simulated RMS current, and (e) simulated breakdown of losses. Discuss (f) how closely your simulated loss aligns with your calculated loss in the pre-lab, (g) if any losses are neglected in your simulation, and (h) whether or not neglecting such loss is appropriate for your design.

Converter Design Tradeoffs

Power electronics design must often balance a variety of tradeoffs between efficiency, size, cost, transient response, reliability, etc. All of these metrics matter to some degree, but which matter more than others? And how much more do they matter than others? The answer depends on the power converter’s intended application. Now, let’s explore some common design tradeoffs using PLECS simulations with switch parasitics.

- Simulate your converter for the same operating point as above but with twice the switching frequency. In PLECS, estimate your conduction losses and switching losses, and compare these to the losses of the previous section. Estimate the ripple on the inductor current, and compare this to the previous ripple. Are these differences predictable using calculations?

2. Simulate your converter for the same operating point as above but with 1/8 the inductor size. In PLECS, estimate your conduction losses and switching losses, and compare these to the losses of the previous section. Are these differences predictable using calculations?
3. The $R_{ds,on}$ and C_{oss} of a switch are closely related to its die size. Select a different switch with the same voltage rating but a significantly larger die size (i.e., higher current rating), and use it to simulate your converter. In PLECS, estimate your conduction losses and switching losses, and compare these to the losses of the previous section. How does the switch's $R_{ds,on}$ and C_{oss} compare to the switch you chose?

Check-off: Discuss the design tradeoffs associated with (a) frequency, (b) ripple allowance, and (c) switch size. Tell us (d) how much dedicated time you spent on this lab, and (e) if any other student(s) in the lab helped you, and who.

Post-lab Assignment

Lab Results

- From your ideal PLECS simulation, provide screenshots of your simulated i_L ripple, v_{out} ripple, and switch stress for each corner operating point.
- Provide your simulation-based loss estimates for your switches, including a breakdown of loss types, and discuss how they compare with your calculations from the pre-lab. Discuss any discrepancies, any neglected losses, and whether or not neglecting these losses is valid.
$$\underbrace{P_{cond,loss} + P_{sw,loss}} \Leftrightarrow P_{total}$$

Lab Takeaways

- In your own words, describe how to choose power FETs for a converter design.
- In your own words, describe how to analyze and manage the heat transfer of power devices.
- In your own words, describe how to model switch parasitics in PLECS, and the degree to which this model reflects the true behavior of a power FET. Describe any limitations to the model.
- In your own words, describe how to measure switch losses (due to conduction and switching) in PLECS.
- Describe your strategy for conducting an optimal part search on Digikey, and at least one pitfall to watch out for.

Build Intuition

- Describe the tradeoffs associated with selecting a switching frequency. Are there particular size, loss, or other consequences for selecting a very high or very low frequency? If you had designed your converter to operate at twice the switching frequency, how would this affect your passive component sizes (assuming the same ripple) and switch losses?
- Describe the tradeoffs associated with choosing a maximum inductor current ripple. How does this selection affect your inductor size (for the same frequency), output capacitor size (for the same v_{out} ripple) and the loss of your switches?
- Describe the general relationship between a power FET's die size (i.e., area) and its $R_{ds,on}$ and C_{oss} , assuming the same voltage rating. Generally speaking, how would the $R_{ds,on}$ and C_{oss} of a smaller transistor compare to those of a larger one? How would the distribution of switch losses compare?
- Describe the general relationship between a power FET's voltage rating and its $R_{ds,on}$, assuming the same die size.

EE 213B

Choose a switching frequency for your design, and size the components for your chosen converter topology. This should include switch current and voltage stresses, along with inductance and capacitance values corresponding to your chosen requirements (e.g., ripple specifications). Your converter design must adhere to the input and output voltage ripples specified in Table 1.

Simulate your power converter in PLECS using ideal switches. Demonstrate with screenshots of your waveforms that the passive components are sized appropriately, that you meet the input and output voltage ripple requirements, and that your switch stress calculations are valid.

Assignment Feedback (Required)

How much dedicated time did you spend on this post-lab?