

Diseño Digital Avanzado

Unidad 1 - Herramientas

Dr. Ariel L. Pola

apola@fundacionfulgor.org.ar

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Proyecto Leds

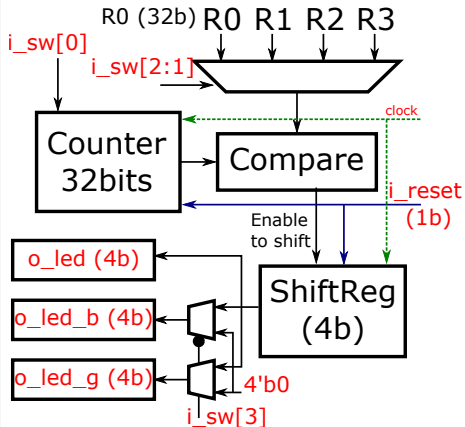


Proyecto LEDS

Implementación en FPGA - Leds

Descripción

- Los nombres en **ROJO** son puertos.
- *ck_rst* es el reset del sistema, el cual pone a cero el contador e inicializa el shiftregister (SR).
- *i_sw[0]* controla el enable (1) del contador. En estado (0) todo se detiene sin alterar el estado actual del contador y del SR.
- El SR se desplaza únicamente cuando el contador llegó a algún límite R0-R3.
- La elección del límite se puede realizar en cualquier momento del funcionamiento.
- *i_sw[3]* elije el color de los leds RGB.



Descripción

- El test bench (banco de pruebas) es un módulo que no tiene puertos declarados.
- Genera los estímulos de reloj y señales de control para modelar un escenario de prueba.
- Las variables utilizadas para estimular los puertos de entrada son declaradas como tipo **reg**.
- Las variables utilizadas para conectar los puertos de salida son declaradas como tipo **wire**.
- Lectura y cambio de estado de variables internas a los módulos
 - Definiendo las instancias se puede leer las variables internas
Ejemplo, assign `tb_count = tb_shiftleds.u_shiftleds.counter;`
 - Utilizando **force** se cambia el valor de una variable en una instancia. Se debe definir dentro de un bloque de procesamiento **initial**.
Ejemplo, force `tb_shiftleds.u_shiftleds.o_led = 4'b0001;`

Proyecto LEDS

Test Bench

Ejemplo - Generando Estímulos

```
1 'define N_LEDS 4
2 'define NB_SW 4
3
4 'timescale 1ns/100ps
5
6 module tb_shiftleds();
7
8     parameter N_LEDS = 'N_LEDS ;
9
10    wire [N_LEDS - 1 : 0] o_led ;
11    reg [NB_SW - 1 : 0] i_sw ;
12    reg ck_rst ;
13    reg CLK100MHZ;
14
15    initial begin
16        i_sw = 4'b0000 ;
17        CLK100MHZ = 1'b0 ;
18        ck_rst = 1'b0 ;
19        #100 ck_rst = 1'b1 ;
20        #100 i_sw = 4'b0001 ;
21        #1000000 i_sw = 4'b0011 ;
22        #1000000 i_sw = 4'b1011 ;
23        #1000000 $finish;
24    end
```

```
1
2 always #5 CLK100MHZ = ~CLK100MHZ;
3
4 shiftleds
5     #(N_LEDS (N_LEDS) ,
6       .NB_SW (NB_SW)
7     )
8 u_shiftleds
9     (.o_led (o_led) ,
10      .i_sw (i_sw) ,
11      .ck_rst (ck_rst) ,
12      .CLK100MHZ (CLK100MHZ)
13     );
14
15 endmodule // tb_shiftleds
```

Proyecto LEDS

Test Bench

Ejemplo - Estímulos desde Archivos

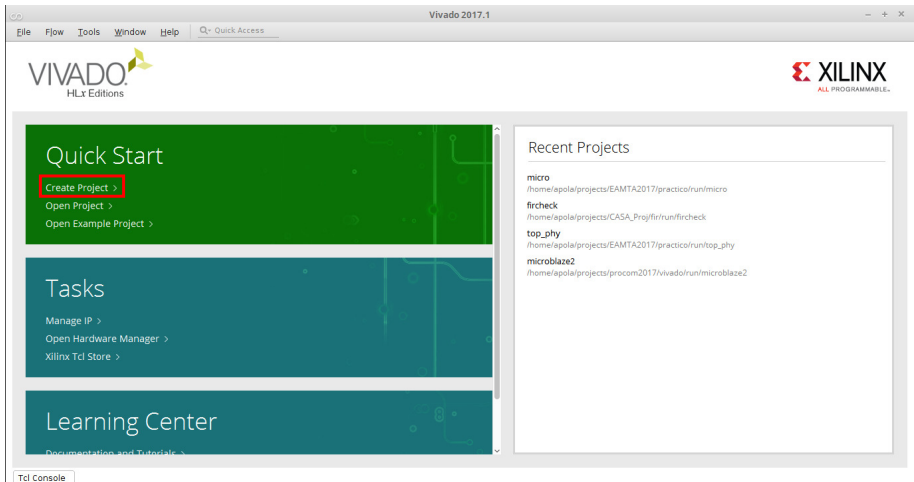
```
1 'define N_LEDS 4
2 'define NB_SW 4
3
4 'timescale 1ns/100ps
5
6 module tb_shiftleds_file();
7
8     parameter N_LEDS = 'N_LEDS ;
9     parameter NB_SW   = 'NB_SW   ;
10
11     wire [N_LEDS - 1 : 0] o_led ;
12     reg [NB_SW - 1 : 0] i_sw ;
13     reg [NB_SW - 1 : 0] sw_tmp ;
14     reg ck_rst, CLK100MHZ, reset_tmp;
15
16     integer fid_reset, fid_sw;
17     integer code_error, code_error1;
18     integer ptr_sw;
19
20     initial begin
21         fid_reset = $fopen("./vectors/reset.out"
22             , "r");
23         fid_sw = $fopen("./vectors/switch.out", "r"
24             );
25         if (fid_sw==0) $stop;
26         if (fid_reset==0) $stop;
27         CLK100MHZ = 1'b0 ;
28     end
29
30     always #5 CLK100MHZ = ~CLK100MHZ;
31
32     always@(posedge CLK100MHZ) begin
33         code_error <=
34             $fscanf(fid_reset, "%d", reset_tmp);
35         if (code_error!=1) $stop;
36
37         for (ptr_sw=0; ptr_sw<NB_SW;
38             ptr_sw = ptr_sw+1) begin
39             code_error1 <=
40                 $fscanf(fid_sw, "%d", sw_tmp[(ptr_sw+1)
41                     -1 -: 1]);
42             if (code_error1!=1) $stop;
43         end
44
45         ck_rst <= reset_tmp;
46         i_sw <= sw_tmp;
47         $display("%d", ck_rst);
48     end
49
50     shiftleds
51     u_shiftleds
52     (.o_led (o_led) ,
53     .i_sw (i_sw) ,
54     .ck_rst (ck_rst) ,
55     .CLK100MHZ (CLK100MHZ));
56
57 endmodule // tb_shiftleds
```

Herramienta Vivado



Herramienta Vivado

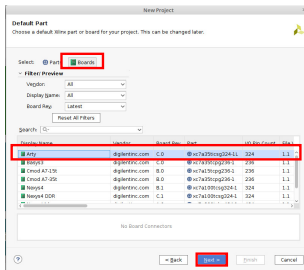
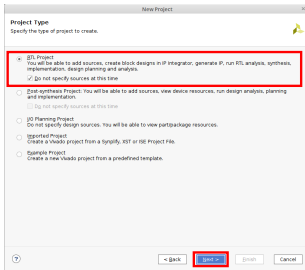
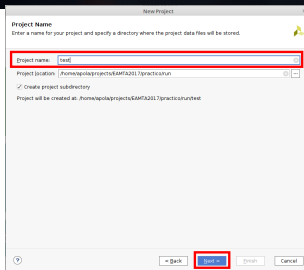
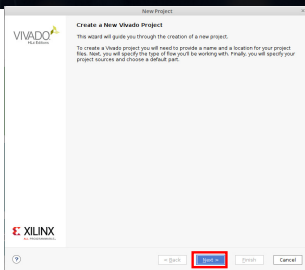
Vivado



Crea un nuevo proyecto

Herramienta Vivado

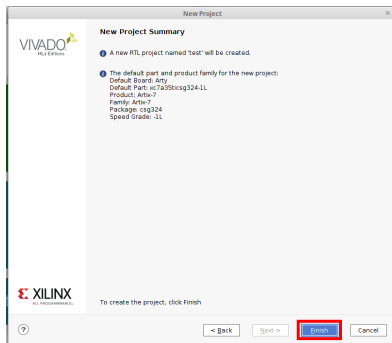
Vivado



Configura el kit de trabajo

Herramienta Vivado

Vivado



Configura el kit de trabajo

Herramienta Vivado

Vivado

test - [/home/apola/projects/EAMTA2017/practico/run/test/test.xpr] - Vivado 2017.1

File Edit Flow Tools Window Layout View Help Quick Access

Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources**
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design

PROJECT MANAGER - test

Sources

- Design Sources
 - Constraints
 - Simulation Sources
 - sim_1
- Hierarchy
- Libraries
- Compile Order

Properties

Select an object to see properties

Project Summary

Settings Edit

Project name: test

Project location: /home/apola/projects/EAMTA2017/practico/run/test

Product family: Artix-7

Project part: Arty (xc7a35t1csg324-1L)

Top module name: Not defined

Target language: Verilog

Simulator language: Mixed

Board Part

Tcl Console Messages Log Reports Design Runs

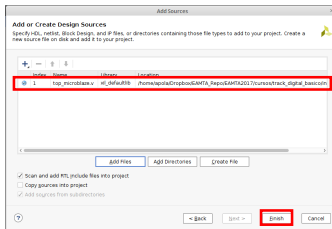
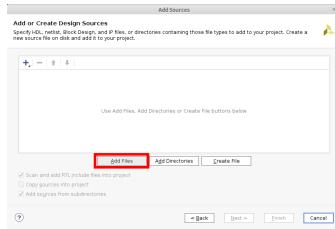
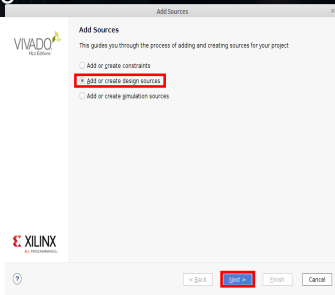
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Specify and/or create source files to add to the project

Agrega nuevas fuentes a *Design Sources*

Herramienta Vivado

Vivado



Seleccionar todos los archivos verilog relacionados al diseño

Herramienta Vivado

Vivado

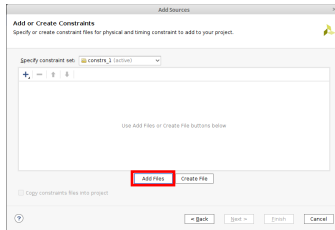
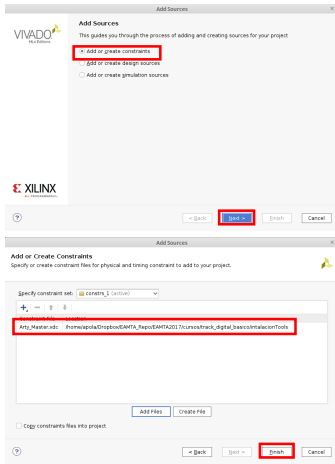
The screenshot displays the Vivado IDE interface for a project named 'test'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The 'Flow Navigator' on the left lists project stages: PROJECT MANAGER (with 'Add Sources' highlighted), IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, and IMPLEMENTATION. The 'PROJECT MANAGER - test' panel shows a tree view of 'Sources' with 'Design Sources', 'Constraints', and 'Simulation Sources'. The 'Properties' panel below it is empty, prompting the user to 'Select an object to see properties'. The 'Project Summary' panel on the right provides details about the project, including the name 'test', location, product family 'Artix-7', and target language 'Verilog'. The 'Design Runs' panel at the bottom shows a table of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Agrega nuevas fuentes a *Constraints*

Herramienta Vivado

Vivado



Selecciona el archivo xdc

Herramienta Vivado

Vivado

The screenshot displays the Vivado IDE interface for a project named 'test'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The 'Flow Navigator' on the left shows the project hierarchy, with 'Add Sources' highlighted under 'PROJECT MANAGER'. The 'PROJECT MANAGER - test' window is open, showing the 'Sources' tab with 'Design Sources', 'Constraints', and 'Simulation Sources'. The 'Simulation Sources' section is expanded, showing 'sim_1'. The 'Properties' tab is also visible, displaying 'Select an object to see properties'. The 'Project Summary' window on the right shows the project details, including the project name 'test', location, product family 'Artix-7', project part 'Arty (xc7a35tcsig324-1L)', top module name 'Not defined', target language 'Verilog', and simulator language 'Mixed'. The 'Board Part' section is also visible. The 'Tcl Console' and 'Messages' tabs are active, showing the 'Design Runs' table.

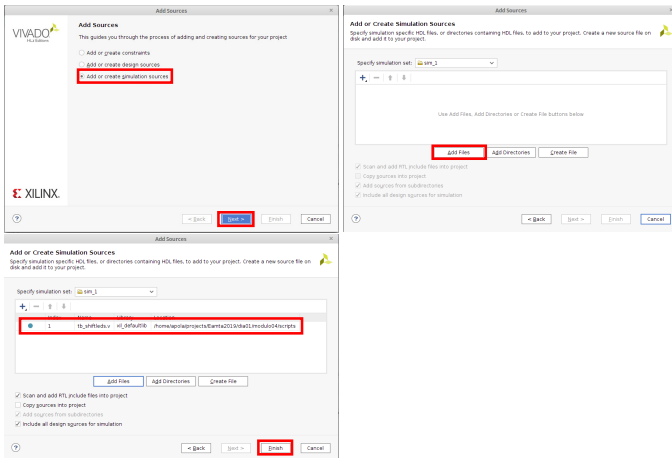
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Specify and/or create source files to add to the project

Agrega nuevas fuentes a *Simulation Sources*

Herramienta Vivado

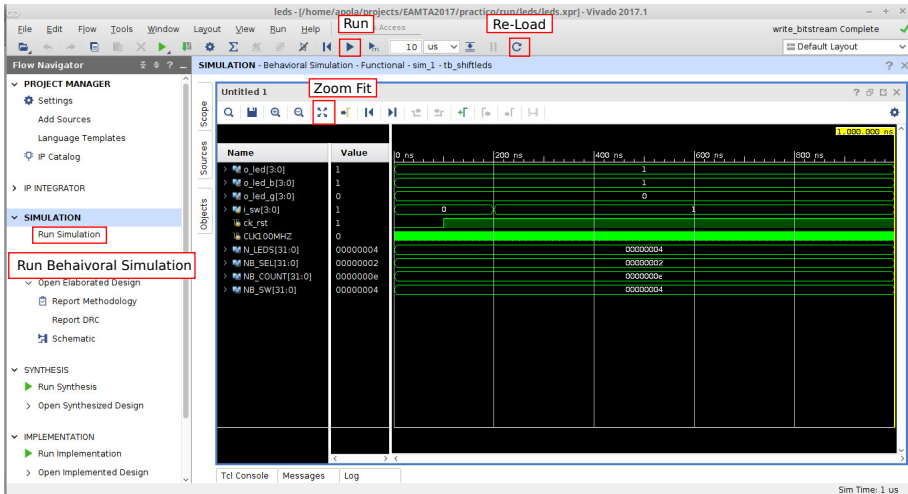
Vivado



Selecciona el archivo verilog para simulación

Herramienta Vivado

Run Simulation - Run Behavioral Simulation



Simulando el comportamiento del diseño

Herramienta Vivado

Vivado

The screenshot shows the Vivado IDE interface for a project named 'test'. The title bar indicates the file path: 'test - [/home/apola/projects/EAMTA2017/practico/run/test/test.xpr] - Vivado 2017.1'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The 'Flow Navigator' on the left lists various project steps: IP Catalog, IP INTEGRATOR (Create, Open, Generate Block Design), SIMULATION (Run Simulation), RTL ANALYSIS (Open Elaborated Design), SYNTHESIS (Run Synthesis, Open Synthesized Design), IMPLEMENTATION (Run Implementation, Open Implemented Design), and PROGRAM AND DEBUG (Generate Bitstream, Open Hardware Manager). The 'Generate Bitstream' option is highlighted with a red box. The 'PROJECT MANAGER' pane shows the 'Sources' tab with a hierarchy of 'constrs_1 (1)' containing 'Arty_Master.xdc' and 'Simulation Sources (1)' containing 'sim_1 (1)'. The 'Properties' tab is empty, prompting to 'Select an object to see properties'. The 'Project Summary' pane on the right displays project details: Project name: test, Project location: /home/apola/projects/EAMTA2017/practico/run/test, Product family: Artix-7, Project part: Arty (xc7a35ticsg324-1L), Top module name: top_microblaze, Target language: Verilog, and Simulator language: Mixed. The 'Board Part' section is also visible. At the bottom, the 'Design Runs' table shows the status of synthesis and implementation runs.

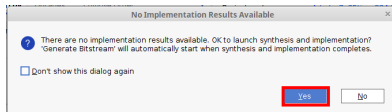
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Generate a programming file after implementation

Generar el *bitstream*

Herramienta Vivado

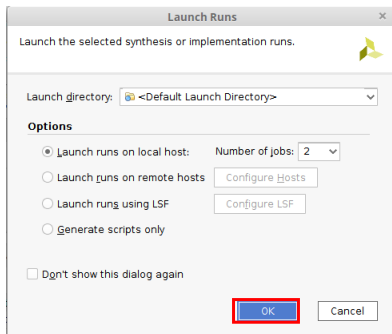
Vivado



Generar el *bitstream*

Herramienta Vivado

Vivado



Generar el *bitstream*

Herramienta Vivado

Vivado

The screenshot displays the Vivado IDE interface for a project named 'test'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A red box highlights the 'Running synth_design' button in the top right corner, which is accompanied by a green checkmark icon.

The left sidebar shows the 'Flow Navigator' with the following sections:

- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis**
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

The main workspace is divided into several panels:

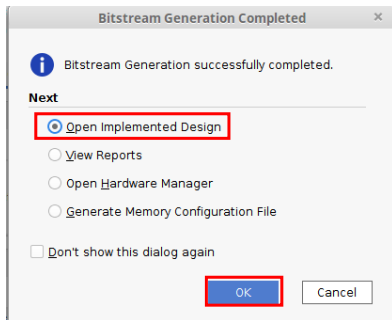
- Sources:** Shows a hierarchy of files including 'constrs_1 (1)', 'Arty_Master.xdc', 'Simulation Sources (1)', and 'sim_1 (1)'. The 'Hierarchy' tab is selected.
- Properties:** A panel for viewing properties of selected objects, currently showing 'Select an object to see properties'.
- Project Summary:** Displays project details:
 - Settings: Edit
 - Project name: test
 - Project location: /home/apola/projects/EAMTA2017/practico/run/test/test.xpr
 - Product family: Artix-7
 - Project part: Arty (xc7a35ticsg324-1L)
 - Top module name: top_microblaze
 - Target language: Verilog
 - Simulator language: Mixed
 - Board Part: (empty)
- Design Runs:** A table showing the progress of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start
synth_1	constrs_1	Running synth_design...													7/1...
impl_1	constrs_1	Queued...													

Ejecutando tareas de implementación

Herramienta Vivado

Vivado



Abriendo el modelo implementado

Herramienta Vivado

Vivado

test - [/home/apola/projects/EAMTA2017/practico/run/test/test.xpr] - Vivado 2017.1

write_bitstream Complete

Default Layout

IMPLEMENTED DESIGN - xc7a35ticsg324-1L (active)

Sources Netlist x

- top_microblaze
 - Nets (21)
 - Leaf Cells (19)

Properties

Select an object to see properties

Project Summary x Device x

Timing x

Design Timing Summary

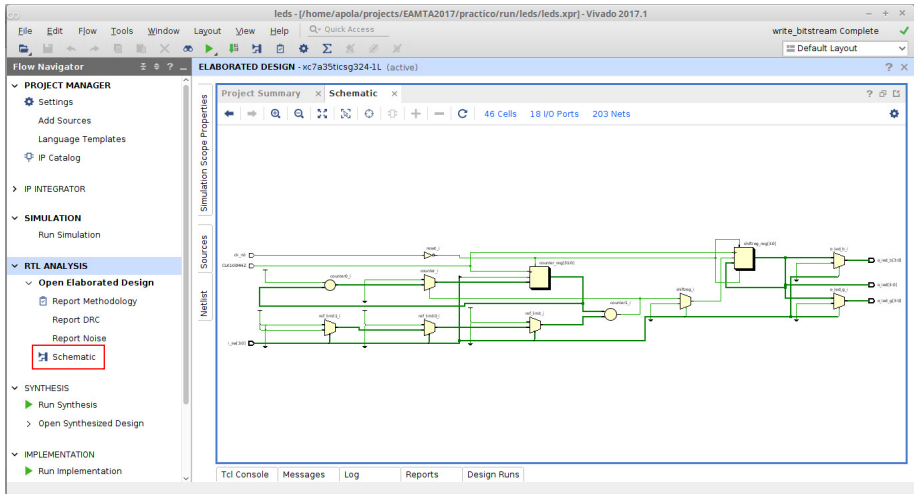
General Information	Setup	Hold	Pulse Width
Timer Settings			
Design Timing Summary			
Clock Summary (1)			
Check Timing (5)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
All user specified timing constraints are met.			
Timing Summary - impl_1 (saved)			

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 7.592 ns	Worst Hold Slack (WHS): 0.130 ns	Worst Pulse Width Slack (WPWS):
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:
Total Number of Endpoints: 6	Total Number of Endpoints: 6	Total Number of Endpoints:

Diseño implementado

Herramienta Vivado

RTL Schematic



Esquemático RTL

Herramienta Vivado

Synthesis - Schematic

leds - [/home/apola/projects/EAMTA2017/practico/run/leds/leds.xpr] - Vivado 2017.1

File Edit Flow Tools Window Layout View Help Q- Quick Access write_bitstream Complete ✓ Default Layout

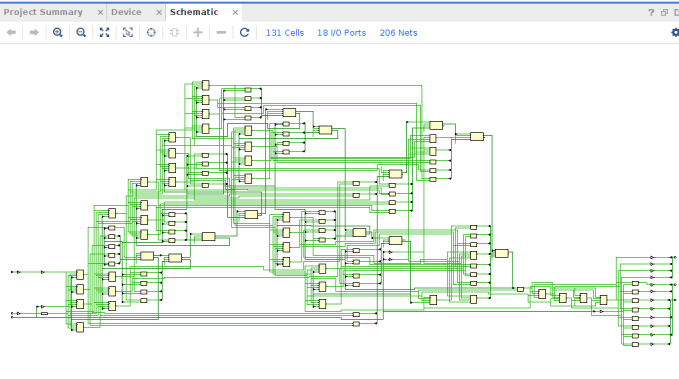
Flow Navigator

- SIMULATION
- RTL ANALYSIS
- SYNTHESIS**
 - Run Synthesis
 - Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic**
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design

SYNTHESIZED DESIGN - xc7a35ticsg324-1L (active)

Project Summary x Device x **Schematic** x ? ? ?

131 Cells 18 I/O Ports 206 Nets



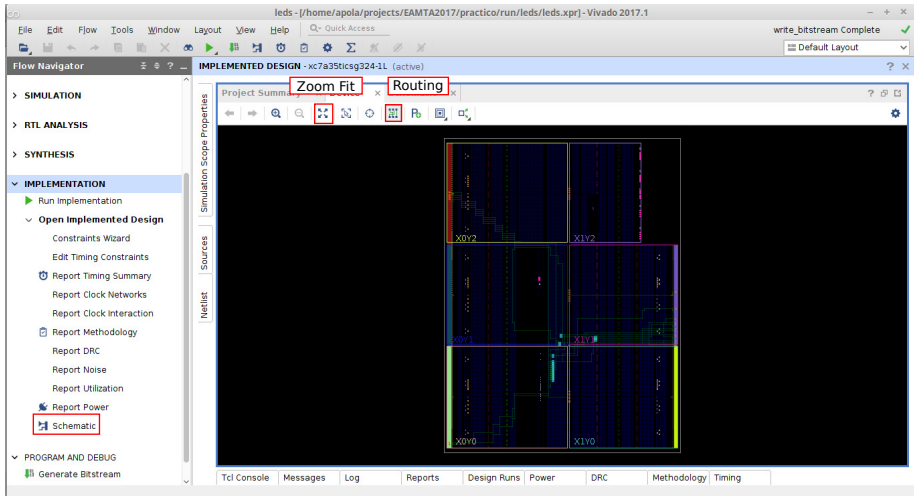
Simulation Scope Properties Sources Netlist

Tcl Console Messages Log Reports Design Runs

Esquemático Implementación

Herramienta Vivado

Implementation - Schematic



Implementation