ESE 118 Lab 1 Report

Andy Dong and Lucas Rhode
ESE 118.05

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1 Task 1: Creating a Logic Schematic

For this task, we created a new project file in OrCAD and implemented the logic expression:

$$Z = AB' + C'D$$

To do this, we needed to add the 74HC library (and later the SOURCESIM library for the logic analyzer). After adding it, we placed the necessary AND, OR, and NOT gates.

Since each chip contains four individual gates, we learned that a fifth gate requires a different chip and is labeled accordingly. To construct the expression, we placed an inverter for the B and C inputs, then ANDed them with A and D, respectively. We then used an OR gate to combine the outputs of these AND gates. Finally, we connected all components with appropriate wiring.

After completing the schematic, we added logic probes and labeled the intermediate signals E, F, and Z to prepare for the logic simulation in the next task.

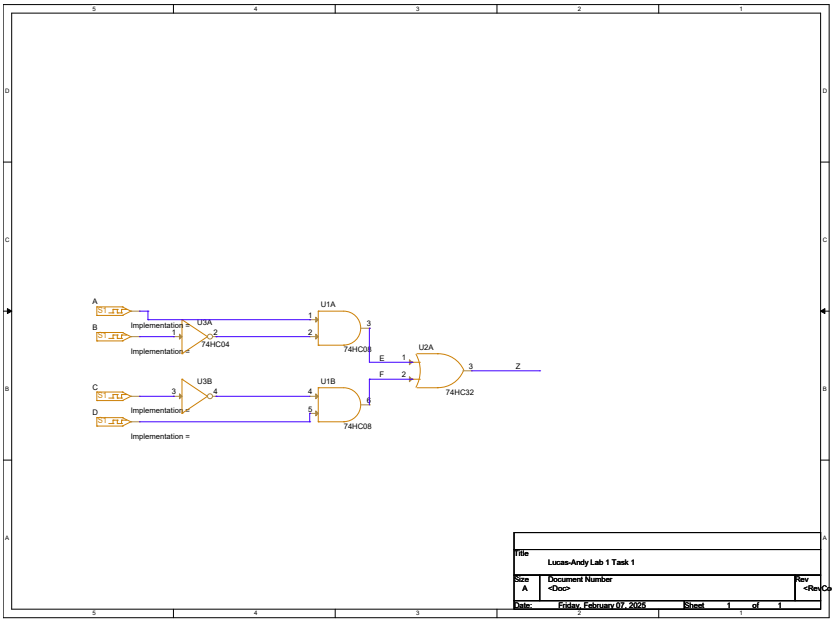

Figure 1: Task 1: Logic schematic for $Z = AB' + C'D$.

2 Task 2: Simulating the Circuit Using PSpice

In this task, we used PSpice to simulate the circuit's functionality. We set up 16 possible input combinations in the DigStim1 components to observe the system's function for every possible input.

The simulation waveforms below illustrate every input possibility and the corresponding outputs. For example:

- Initially, all inputs (A, B, C, and D) were set to 0, resulting in E, F, and Z also being 0.
- In the next scenario, inputs A, B, and C remained 0 while D was 1. This resulted in F being 1 since C' becomes 1 and is ANDed with D. Since Z is obtained via OR operation on E and F, and E remains 0, Z takes the value of F (which is 1).

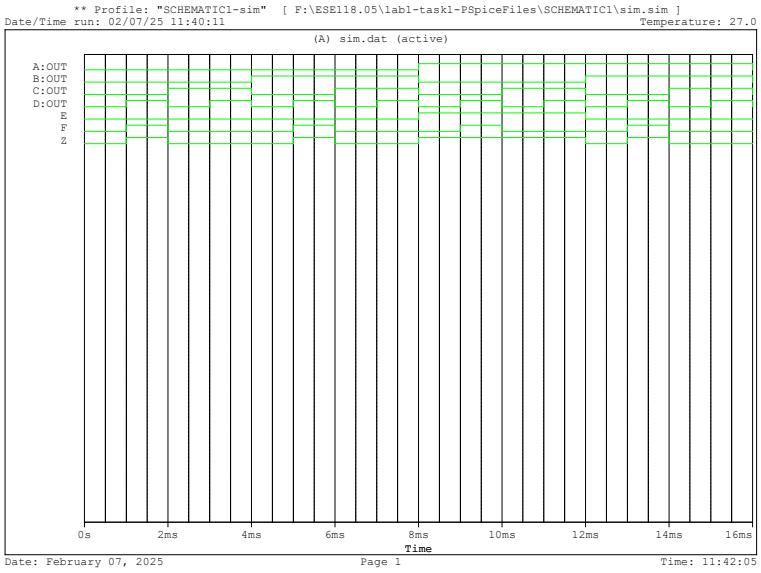

Figure 2: Task 2: Simulation waveforms displaying circuit behavior.

3 Task 3: Designing a New Circuit

Using the knowledge gained from Tasks 1 and 2, we constructed a new circuit with a different Boolean function and performed logic analysis. The approach followed was similar to the previous tasks but applied to a different expression.

One challenge we encountered was forgetting to create a new simulation profile, which initially prevented PSpice from running. However, after identifying the issue, we quickly resolved it. By completing this task, we solidified our understanding of the steps involved in circuit design and PSpice simulations.

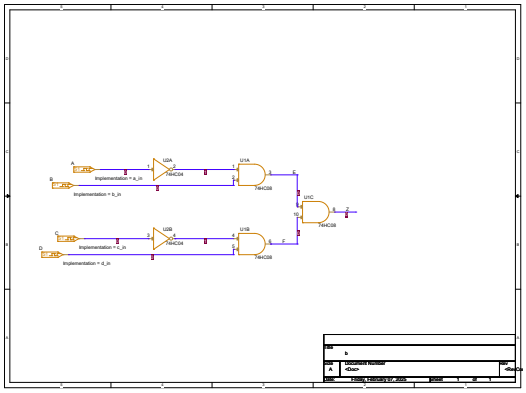

Figure 3: Task 3: Schematic for new Boolean function implementation.

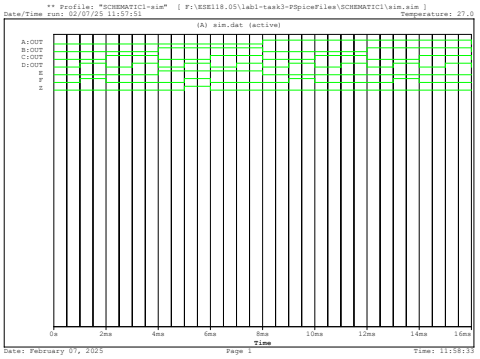

Figure 4: Task 3: Simulation waveforms for the new circuit.

4 Conclusion

In this lab, we learned how to:

- Use OrCAD Capture CIS to design digital circuits.
- Implement Boolean logic expressions using AND, OR, and NOT gates.
- Perform logic simulations in PSpice to verify circuit behavior.
- Troubleshoot common errors such as incorrect library setup and missing simulation profiles.