Program 1

Assembly

```
Line 1 # Lucas Hasting
Line 2 addi $t0, $zero, 5000
Line 3 addi $t1, $zero, 973
Line 4 addi $t2, $zero, 246
Line 5 add $t1, $t1, $t2
Line 6 sw $t1, 0($t0)
```

Registers

$zero	0
$t0	5000
$t1	1219
$t2	246
$t3	0
$t4	0
$t5	0
$t6	0
$sp	0
$ra	0

Data memory

5000	1219
5004	0
5008	0
8180	0
8184	0
8188	0

Program 2

Assembly

```
Line 1 # Lucas Hasting
Line 2 addi $t0, $zero, 5000
Line 3 addi $t1, $zero, 5004
Line 4 addi $t2, $zero, 5008
Line 5 lw $t3, 0($t1)
Line 6 lw $t4, 0($t2)
Line 7 mul $t3, $t3, $t4
Line 8 sw $t3, 0($t0)
```

Registers

$zero	0
$t0	5000
$t1	5004
$t2	5008
$t3	258741
$t4	777
$t5	0
$t6	0
$sp	0
$ra	0

Data memory

5000	258741
5004	333
5008	777
8180	0
8184	0
8188	0

Program 3

Assembly

```
 Line 1 # Lucas Hasting
 Line 2 addi $t0, $zero, 5000
 Line 3 addi $t1, $zero, 5004
 Line 4 lw $t2, 0($t1)
 Line 5 addi $t3, $zero, 13
 Line 6 addi $t4, $zero, 27
 Line 7 addi $t5, $zero, 49
 Line 8 beq $t2, $t3, condition
 Line 9 sw $t5, 0($t0)
Line 10 j end
Line 11 condition: sw $t4, 0($t0)
Line 12 end:
```

Registers

$zero	0
$t0	5000
$t1	5004
$t2	13
$t3	13
$t4	27
$t5	49
$t6	0
$sp	0
$ra	0

Data memory

5000	27
5004	13
5008	0
8180	0
8184	0
8188	0

Assembly

```
 Line 1 # Lucas Hasting
 Line 2 addi $t0, $zero, 5000
 Line 3 addi $t1, $zero, 5004
 Line 4 lw $t2, 0($t1)
 Line 5 addi $t3, $zero, 13
 Line 6 addi $t4, $zero, 27
 Line 7 addi $t5, $zero, 49
 Line 8 beq $t2, $t3, condition
 Line 9 sw $t5, 0($t0)
Line 10 j end
Line 11 condition: sw $t4, 0($t0)
Line 12 end:
```

Registers

$zero	0
$t0	5000
$t1	5004
$t2	31
$t3	13
$t4	27
$t5	49
$t6	0
$sp	0
$ra	0

Data memory

5000	49
5004	31
5008	0
8180	0
8184	0
8188	0

Problem 4

Assembly

```
 Line 1 # Lucas Hasting
 Line 2 addi $t0, $zero, 5008
 Line 3 addi $t1, $zero, 5004
 Line 4 addi $t2, $zero, 5000
 Line 5 lw $t3, 0($t0)
 Line 6 lw $t4, 0($t1)
 Line 7 beq $t4, $zero, end
 Line 8 condition: addi $t3, $t3, 397
 Line 9 sw $t3, 0($t0)
Line 10 addi $t4, $t4, -1
Line 11 sw $t4, 0($t1)
Line 12 bne $t4, $zero, condition
Line 13 end: sw $t3, 0($t2)
```

Registers

$zero	0
$t0	5008
$t1	5004
$t2	5000
$t3	3779
$t4	0
$t5	0
$t6	0
$sp	0
$ra	0

Data memory

5000	3779
5004	0
5008	3779
8180	0
8184	0
8188	0