Chip 2/ Project 2

Goal: M2I w/ 25 GHz FSR of ~ 1310 nm

same as chip I, except:

- · device is air cladded
- · different fub, so different palk
- · using on-chip luser

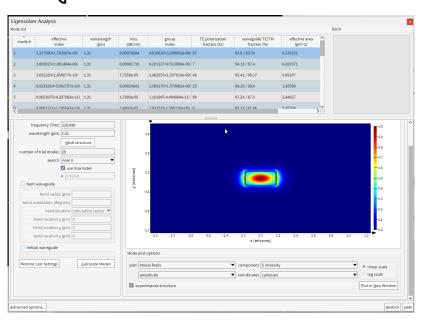
Process:

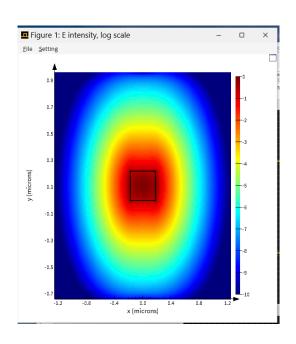
- 1) Simulate wave guide w/ air cladding in Lumerical MODE
 - · were guide itself still siliun, 350m x 220m using same 360m width
 - · air chaddiny disable 5102 daddiny

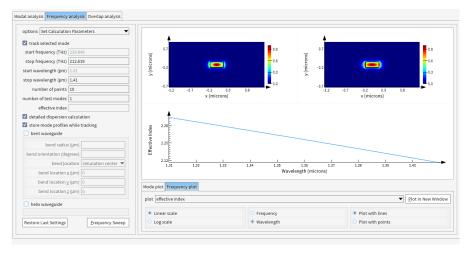
Nair = N vercum = 1.0

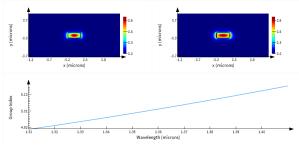
· eigensolver analysis yields

 $n_g = 4.910620$









② Calculate required ΔL $\Delta L = \frac{C}{47 n_g} = 2.442 mm$

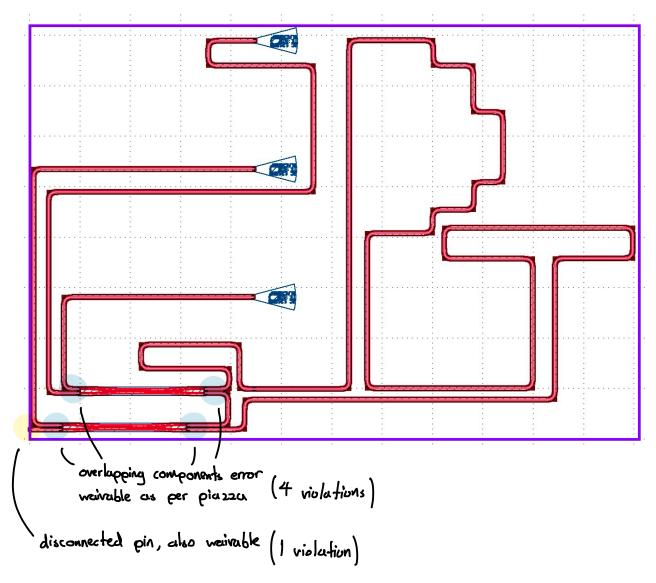
3) Physical design in klayout

• using EBeam_ZEP PDK library
ebeam_GC_Air_TEB10_BB

350nm × D20nm @ 1310nm wave guide
EBeam_directional_coupler_surgassist_te 1310

· Floorplan: 605 mm x 410 mm

· input wave guide at (0,10), un



S violations, but are all waivable

4 Lumerical INTERCONNECT simulation

to be completed...