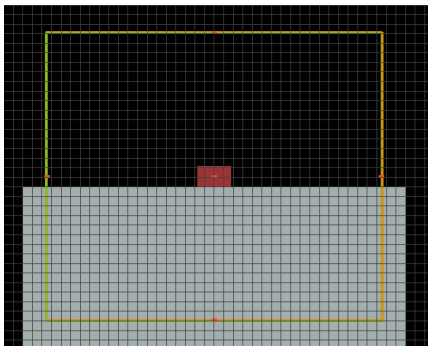
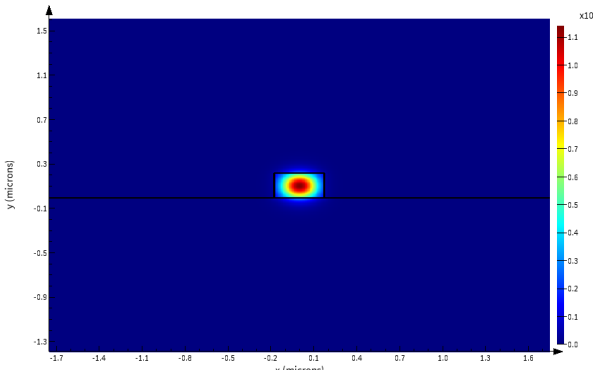
Project 2 (chip #2)

- Fabricated at UBC with the ZEP Process
- Main difference from Chip 1: Air Cladding and new input from on-chip laser

Design Process

- Start by understanding waveguide properties
    - Waveguide with 350 nm width is used so that compatibility is maintained with the components in the provided PDK.
    - Waveguide has dimensions 350x220 nm, has air cladding and sits on an SiO2 layer
        - This should be fairly accurate since there is no significant process bias on this platform
    - Simulated in MODE with the following parameters:
        - 3.5x3.0 um simulation area
        - 400x400 mesh cells
        - 
        - Simulated Group Index: 4.724525
        - Energy density distribution:
        - 
- Interferometer
    - Lock in L1, L2, delta L for good interferometer function
        - Formula from simulated group index gives delta L = 2699 um
    - Beck-of-the-chocolate-wrapper estimate: $\Delta L = \frac{c}{\Delta\nu \cdot n_g}$ gives path length difference of 2.538181 mm
    - Have not simulated in INTERCONNECT since there is some concern about the accuracy of the waveguide models, see Piazza

Floorplan

    - 605*410 um
    - Two devices:
        - Main interferometer uses calculated path length difference and sends output to first and third grating couplers
            - Input can come from either on-chip laser or second grating coupler, routed into the two inputs of the first directional coupler
        - Second device is just a pair of grating couplers to allow calibrating insertion loss when using the external laser
    - Several verification errors: overlapping DevRec regions near the directional couplers, and a disconnected pin where the waveguide enters the cell. Seems normal.
- Testability
    - Grating couplers and spacing
        - 127 um grating coupler spacing is required
    - Input on fibre 2
    - Named fibre 2 like opt_in_TE_1310_device_RonNelson_comment