Lab 1: Introduction to Verilog Simulation and Synthesis

Demo Due: Demo to TA by the end of your lab session during the week of Sep 4-8, 2023.

Code submission: Submit the following files by 11.59 PM on Friday September 8, 2023.

1) Verilog (.v) file – using *Procedural assignment statement* of the lab1 circuit
2) Verilog (.v) file for Testbench.
3) .xdc file

To find .v files, assuming that your Vivado project is called lab1,
the .v file for the circuit is located in lab1/lab1**.srcs**/**sources_1**/new
the .v file for the testbench is located in lab1/lab1**.srcs**/**sim_1**/new

Resources:

- On D2L, under Content -> Vivado_DownLoad_Tutorial_Resources,
  Xilinx Vivado **Simulation Tutorial** and
  Xilinx Vivado **Synthesis Tutorial**, Nexys 4DDR
- On D2L, under Content -> Lecture Notes -> Unit: Verilog, ***Verilog_Basic.pptx***
- In zyBooks, section 7.1 – 7.4

Pre-Lab Assignment (15 pts) - individual work: Write the truth table and logic equations of the digital circuit given in the **Problem Statement** below. Show the TA your work during the first hour of your lab session.

Problem Statement: Design a digital circuit that has

- Four 1-bit inputs (A, B, C, D) representing votes from 4 judges, and
- Three 1-bit outputs (I2, I1, I0) where the 3-bit output shows number of judges ***voting with 1***.

For example,
if A = 0, B = 0, C = 0, D = 0, then
I2 = 0, I1 = 0, I0 = 0 since all 4 judges vote 0. I2I1I0 = 000 is a binary for a decimal 0.
If A = 0, B = 1, C = 1, D = 0, then
I2 = 0, I1 = 1, I0 = 0 since 2 judges vote with 1. I2I1I0 = 010 is a binary for a decimal 2.
If A = 1, B = 1, C = 0, D = 1, then
I2 = 0, I1 = 1, I0 = 1 since 3 judge votes with 1. Observe that I2I1I0 = 011, a binary for 3.

Lab Procedure and Demo:

A) **(15 pts)** **Pre-lab assignment** – see the details above.

B) Verilog: code and testbench for simulation
B1. Verilog file for the designed circuit and Testbench for Simulation
Refer to SimulationTutorial.pdf (on D2L) on how to do this part

- **(25 pts)** Write the Verilog code using procedural assignment statement for the designed circuit. See chapter 7 of Zybook or Verilog_lecture1.pdf under Content -> Lecture Notes -> Unit: Verilog on D2L for more details.

- **(20 pts)** Create and use a Testbench to perform a Behavioral/Functional simulation of your designed circuit. The waveforms for the output signals should match with the outputs of your truth table. If matched or correct, show this waveform to your TA/ULA.

B2 **(10 pts)** Synthesize your design and Run Post-Synthesis Functional Simulation. The output waveform should be the same as the one generated in the Behavioral Simulation. Show this waveform to your TA/ULA.

C) (30 pts) Demo on the board
Refer to SynthesisTutorial.pdf (on D2L) on how to do this part
C1 Create .xdc file to assign pin numbers to the inputs and outputs of the circuit.
C2 Generate Bitstream and Download your circuit design to the Nexys4 Artix-7 FPGA board. Test your design exhaustively trying all possible input combinations. When working on the board, demo this part to TA