A compact and low loss Y-junction for submicron silicon waveguide

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Abstract: We designed a compact, low-loss and wavelength insensitive Y-junction for submicron silicon waveguide using finite difference time-domain (FDTD) simulation and particle swarm optimization (PSO), and fabricated the device in a 248 nm complementary metal-oxide-semiconductor (CMOS) compatible process. Measured average insertion loss is 0.28 ± 0.02 dB, uniform across an 8-inch wafer. The device footprint is less than 1.2 μm x 2 μm, an order of magnitude smaller than typical multimode interferometers (MMIs) and directional couplers.

OCIS codes: (130.3120) Integrated optics devices; (230.7370) Waveguides; (230.1360) Beam splitters.

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1. Introduction

The last decade has witnessed a series of breakthroughs in silicon photonics. Key components such as an electrically pumped laser [1], high-speed modulators [2] and photodetectors [3] have been successfully demonstrated. Foundry services are also becoming available to the community, making it easier to explore system-level functionalities [4,5]. The intrinsic advantage of silicon as a photonic material system is its high refractive index contrast with silicon dioxide, allowing submicron waveguides and tight bends. Moreover, state-of-the-art CMOS fabrication infrastructure developed by the electronics industry can be leveraged [6]. However, these two advantages do not always go in parallel. For example, a Y-junction is theoretically lossless, while this is generally not the case due to finite resolution of micro fabrication. Sharp corners favored by photonics designs usually violate the minimum feature size rule of a CMOS process, which can be easily detected by design rule checking (DRC) routines. The possible detrimental effects of this violation in fabrication includes peeling off of photoresists, shallower etch in the narrow gap, and voids in subsequent oxide cladding deposition. All of the above degrade device performance and lower the yield.

A Y-junction formed by circular bends with a butt waveguide in between to avoid the sharp corners is observed to have over 1 dB insertion loss in our experiment. Mach-Zehnder modulators consisting two such Y-branches readily have more than 2 dB insertion loss in the budget [7], regardless of other losses from free carrier absorption and on-and-off chip light coupling, making them less competitive than state of the art III-V electro-optic modulators, which usually have around 5 dB fiber to fiber insertion loss. Obviously, complex and large scale integrated optical circuits cannot be built on such lossy components. Moreover, the abrupt waveguide discontinuity causes light scattering and back-reflection. Implicit resonant cavities formed by these scattering sites degrade the system spectral response.

As one the most basic building blocks, a low loss and compact Y-junction is critical to silicon photonic circuits. Recently a number of authors have demonstrated attractive device performance for Y-junctions [8], MMI couplers [9], cascaded splitters [10,11], photonic crystal 3 dB couplers [12] and directional couplers [13]. However, a Y-junction with low excess loss, low wavelength sensitivity, small footprint, and dimensions clearly within the typical design rules of a modern CMOS photonics process has remained elusive.

In this paper, we report the design and fabrication of a Y-junction for submicron silicon waveguides with a taper size less than 1.2 μm x 2 μm, and cross-wafer average insertion loss of 0.28 ± 0.02 dB, comparable to or better than the results demonstrated by electron beam lithography (EBL) and for MMIs with much larger footprint. Coupling ratio is wavelength insensitive over 80 nm bandwidth from 1500 nm to 1580 nm. The device has a minimum feature size of 200 nm, and was successfully fabricated using 248 nm lithography.

2. Design and fabrication

2.1 Design and optimization

Our goal was to design a compact, low loss and wavelength insensitive Y-junction for submicron silicon waveguide, compatible with typical CMOS photonic processes, where 193

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nm or 248 nm steppers are commonly used. A minimum feature size of 200 nm was assumed during the design, which would not break the designs rules, thus ensuring optimal yield. Silicon waveguide geometry is 500 nm wide x 220 nm high and the taper width is 0.5 µm at the input and 1.2 µm at the output, as shown in Fig. 1(a). The length of the taper connecting input and output waveguides was set to 2 µm to keep the device compact. The size of Ge-on-Si photodetectors and absorption modulators are usually on the order of 10 µm, and p-n junction modulator with phase shifter length of 50 µm has been demonstrated [14]. A simple passive component like a Y-junction should be compact enough to be part of a more complicated active device or an integrated optical circuit. The Y-junction is symmetric in the propagation direction to ensure balanced output at the two branches.

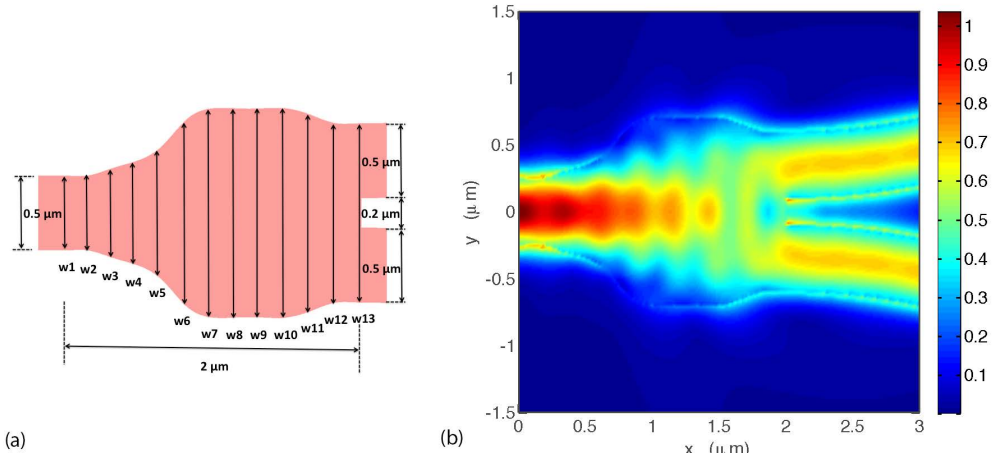

Fig. 1. (a) Schematic of device layout. The taper geometry is defined by spline interpolation of w1 to w13. (b) Contour plot of simulated E-field distribution at 1550 nm wavelength.

The electromagnetic response of dielectric structures of size on the order of the wavelength of interest can be simulated by Finite Difference Time Domain (FDTD) method. FDTD can be coupled with optimization algorithms for design optimization. Sanchis *et al.* demonstrated a waveguide crossing with 0.2 dB insertion loss and –40 dB cross-talk designed by FDTD and Genetic Algorithm (GA) [15]. We utilized a different optimization algorithm, Particle Swarm Optimization (PSO), in this design. PSO was originally inspired by the social behavior of flocks of birds or schools of fishes [16], and has been successfully applied to electromagnetic optimization problems [17]. In PSO, the potential solutions, called particles or agents, are initialized at random positions with random velocities in the parameter space. A figure of merit function is defined to evaluate the particle position according to the optimization goal. The best position for each individual particle is recorded, as well as a global best position ever achieved by any particle in the swarm. The position of a particle is updated by the following equation,

$$x_n = x_n + \Delta t * v_n \tag{1}$$

$$v_n = \omega * v_n + c_1 * rand() * (p_{best,n} - x_n) + c_2 * rand() * (g_{best,n} - x_n) \tag{2}$$

where v_n and x_n are particle's velocity and position in the nth dimension of the parameter space, and $p_{best,n}$ and $g_{best,n}$ are individual and global best positions, respectively. Apparent from Eq. (2), the new velocity is the old velocity scaled by ω and increased in the direction of $p_{best,n}$ and $g_{best,n}$. ω, known as the inertial weight, is a measurement of how much a particle would like to stay at the old velocity. c_1 determines how much a particle is influenced

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by the memory of its best position, thus sometimes called cognitive rate. And c_2 is a factor demining how much the particle is affected by the global best position of the whole swarm, hence called social rate. The two random numbers *rand*(), uniformly distributed between 0 and 1, are used to simulate the unpredictable behavior of natural swarm. It can be seen that the particle velocity is large when it is far from $p_{best,n}$ and $g_{best,n}$, becomes smaller as it is closer to the best position and gets pulled back after flying over. The optimization is stopped when the figure of merit is good enough or a large number of iterations is reached.

In this design, the taper was first digitalized into 13 segments of equal length. The width of each segment, labeled as w1 to w13 in Fig. 1(a), was optimized to achieve low loss coupling. Taper geometry is defined by spline interpolation of these 13 points. The optimization figure of merit (FOM) was the power in the TE_0 mode at either branch. It was calculated by the overlap integral of the TE_0 mode of a 500 nm x 220 nm waveguide with the detected field at the output branch at wavelength 1550 nm. Note that it is not proper to set the total detected power to be FOM, since higher order modes will leak out of the waveguide along the way. Maximizing the power effectively reduces the scattering and back-reflection. The swarm population was set to 30. 2D FDTD was used as an approximation of 3D FDTD for computing efficiency during optimization. A commercially available code wad used [18]. Within 50 iterations, one solution with sub-0.2 dB insertion loss emerged, as shown in Table 1. Then 3D FDTD was run on this solution to double check the result with a mesh equal to 1/34 of the free space wavelength. The insertion loss was determined to be 0.13 dB. Scattering is negligible, as shown in the contour plot of electric field in Fig. 1(b). There is an interference pattern at the input end, indicating existence of very weak back-reflection. The normalized transmission and reflection power as a function of wavelength is plotted in Fig. 2. It can be seen that both the transmission and reflection are virtually wavelength insensitive, with variation below 1% and 0.5% over the wavelength range from 1500 nm to 1580 nm.

Table 1. Taper width in μm

w1	w2	w3	w4	w5	w6	w7	w8	w9	w10	w11	w12	w13
0.5	0.5	0.6	0.7	0.9	1.26	1.4	1.4	1.4	1.4	1.31	1.2	1.2

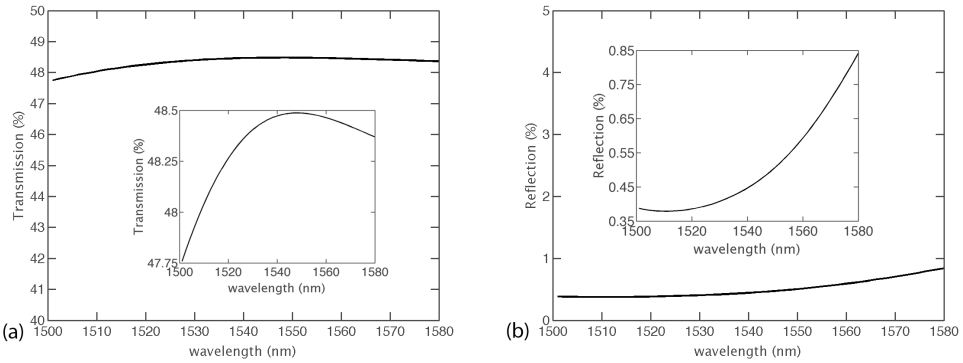

Fig. 2. Simulated (a) power transmission and (b) reflection as a function of wavelength, with zoomed-in view in the insets.

2.2 Device fabrication

Starting substrate was an 8-inch SOI wafer, with 220 nm, 10 ohm-cm p-type top silicon film, 2 μm buried oxide on top of a silicon handle. Photo mask was fabricated in a commercial mask shop with grid resolution much finer than the device minimum feature size. Waveguides were patterned using 248 nm UV lithography followed by dry etching. Then 2.3 μm of oxide was deposited as top cladding. Light coupling on and off the chip was achieved by grating couplers (GC). Two kinds of characterization structures were laid out, as shown in Fig. 3. A

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cascade of Mach-Zehnder structures formed by butt coupled Y-junctions were used to measure the insertion loss, similar to those used in [19]. The other structure has the three terminals of the Y-junction connected to three grating couplers to measure the two outputs directly. In both cases, the bend radius of the connecting waveguides is 5 μm, large enough to introduce negligible bending loss. The grating coupler pitch is 127 μm, determined by the pitch of our fiber array. Simple GC loops, i.e. two GCs connected by a U-turn waveguide, were used as a reference structure. Tiles used around the devices to achieve a certain filling ratio are not shown.

3. Results and discussion

3.1 Testing configuration

Devices were measured on a wafer scale setup that can map the wafer coordinate to the stage coordinate, so that any device can be easily probed after initial alignment. Light from a tunable laser was coupled into the device under test (DUT) via a polarization maintaining (PM) fiber and grating coupler, then to a photodetector through another grating coupler and PM fiber. Chuck temperature was set to 35 °C, slightly higher than room temperature, where it is most stable. The device performance reported in this paper is not expected to vary strongly as a function of temperature. Reticle size on the wafer is 2.5 cm x 3.2 cm. Excluding incomplete dies on the edge, Y-junctions in 26 dies were tested to characterize the cross-wafer performance.

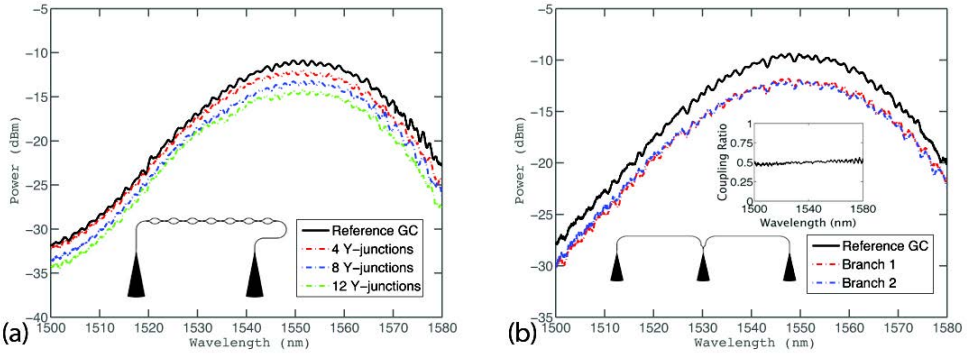

Fig. 3. Typical measured spectra and corresponding test structure. The inset in (b) gives coupling ratio as a function of wavelength. Parabolic line shape and ripples are determined by grating coupler spectral response and imperfect linear polarization, respectively, as discussed in the main text. Offset in y-axis is from Y-junction insertion loss.

Typical measured spectra and corresponding test structure are shown in Fig. 3. The parabolic-like shape is determined by the grating coupler spectral response. The grating coupler design used here works for TE mode only, which has over 20 dB selectivity over TM mode at the fiber array angle we used for testing. If non-perfectly linear polarization light is fed into the grating coupler from a fiber, both *s* and *p* polarization, which are not in phase, partially overlap with the TE mode of grating coupler and couple into the waveguide. They interfere and create ripples on the spectrum. The ripple magnitude scales with the amount of fiber polarization mixture. With a simple fiber birefringence based polarization controller, we typically manage to control the fringes within 0.5 dB peak to peak. It is possible to reduce the fringe even further with more dedicated polarization adjustment.

3.2 Device performance

It is difficult to measure sub-0.5 dB insertion loss from a single device. Therefore, test structures with different numbers of Y-junctions in the loop were used to extract the insertion loss. For each transmission spectrum, a 30 nm wavelength span near the peak was fitted by a

#179570 - $15.00 USD Received 8 Nov 2012; revised 28 Dec 2012; accepted 30 Dec 2012; published 11 Jan 2013

parabolic curve, and the maximum of the parabolic fit was used as the peak power in insertion loss calculation to minimize the effect of ripples. The measured peak power as a function of number of Y-junctions is plotted in Fig. 4(a). Blue dots are test data, and red line is a linear fit. The slope of the line gives the insertion loss in dB per Y-junction, 0.27 ± 0.01 dB in the case of the DUT. Loop baseline losses – about 11 dB, mainly due to grating coupler insertion loss – are the same for all structures, thus won't affect the slope of the fitting line.

Photonic devices performances are sensitive to geometry variations, which can be from either the SOI wafer itself, exhibiting typically ± 20 nm thickness variation for an 8 inch SOI wafer with 220 nm top silicon, or the fabrication process flow. Resonant wavelengths variation on the order of 10 nm is observed in devices fabricated by CMOS high-volume tools [20–22]. As a basic building block, high cross-wafer uniformity is as important as other metrics such as compact footprint and low insertion loss. For this Y-junction design, a major contribution to performance non-uniformity is the silicon film thickness variation. Our 3D-FDTD simulation indicates excess loss is 0.2 dB at thickness of 200 nm and increases to 0.3 dB at 240 nm. A contour plot of insertion loss is shown in Fig. 4(b). From the histogram in Fig. 4(c), we can see that the insertion loss is bounded between 0.23 and 0.32 dB, with a cross-wafer average of 0.28 dB and a standard deviation of 0.02 dB. Low cross-wafer variation confirms that our device is not fabrication sensitive, and fully addresses the DRC violation issue of conventional Y-junctions. Thus it can be a reliable component of an integrated photonic system.

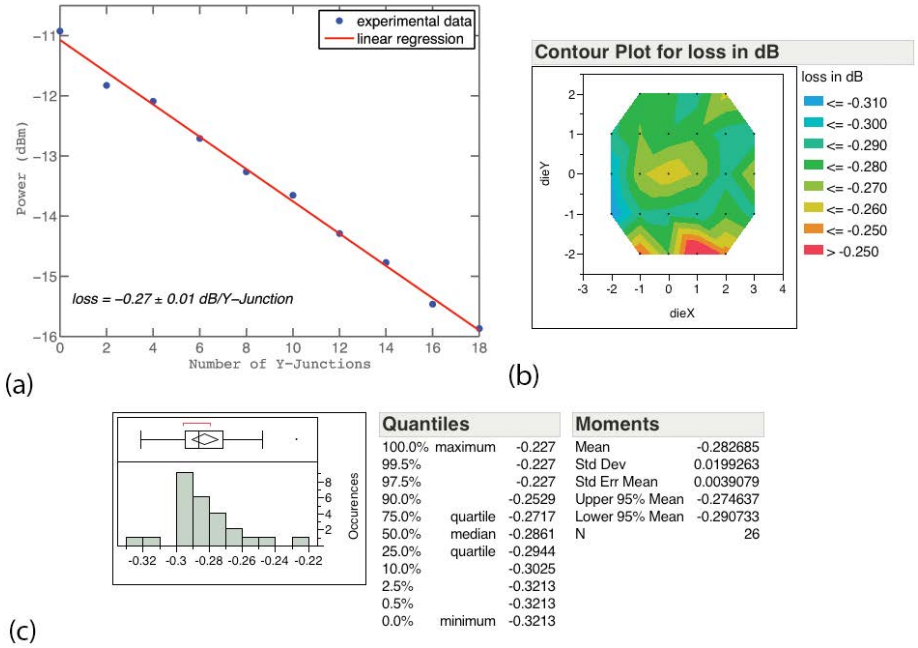

Fig. 4. (a) Blue dots are measured peak optical power. Red line is linear fit; (b) Contour plot of measured Y-junction insertion loss across the wafer; and (c) Histogram of 26-reticle test data of measured insertion loss, showing mean value of 0.28 dB and standard deviation of 0.02 dB.

It is shown in [11] that etch residues or air voids in the gap defined by sharp corners in the layout will lead to non-uniform output at two branches of the Y-junction. In Fig. 3(b), the spectra of two branches overlap over the whole testing wavelength range, indicating balanced output power and wavelength insensitive coupling ratio. From the simulation, we note that the coupling efficiency does roll off at shorter wavelength, as the mode confinement gets tighter. For example, calculated excess loss is about 0.6 dB at wavelength 1310 nm. So for data

#179570 - $15.00 USD Received 8 Nov 2012; revised 28 Dec 2012; accepted 30 Dec 2012; published 11 Jan 2013

communication wavelength of 1310 nm, the Y-junction geometry has to be redesigned or scaled properly.

3.3 Design methodology

Our result also confirms PSO as an efficient optimization algorithm for silicon photonic device design and optimization. We utilized moderate swarm population and iteration cycle. The taper length could also be included in the optimization parameter space, instead of the constant length of 2 μm used in our design. It is possible that even better device geometry will emerge with more dedicated optimization. This design method can be readily used to address other challenges such as non-uniform grating couplers and distributed brag gratings (DBRs).

4. Conclusion

We designed a low loss and compact Y-junction for submicron silicon waveguides. The device is successfully fabricated by 248 nm CMOS. The device footprint is less than 1.2 μm x 2 μm, an order of magnitude smaller than MMIs and directional couplers. Measured insertion loss is 0.28 ± 0.02 dB, uniform across an 8-inch wafer. Output power and splitting ratio are uniform and wavelength insensitive.

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