INDIVIDUAL COMPONENT

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ANALOGUE ELECTRONICS

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Table of Contents

List of Tables

List of Figures

Introduction

This objective of this assignment is to design and create a multi-stage bipolar junction transistor amplifier that that can meet the following requirement under the following conditions.

1. Supply voltage to the amplifier circuit: 12V
2. Input peak to peak signal voltage: 10mV
3. Gain of the amplifier circuit: 38dB to 40dB
4. Lower cut-off frequency: 0 to 300Hz
5. Upper cut-off frequency: 1MHz to 10MHz
6. Amplifier circuit load resistance: 32Ω
7. Total power consumption of the amplifier circuit: less than 1W

This report records the amplifier circuit design that is created to fulfill all the requirements above. The analysis and calculations are also recorded in this report clearly. The simulation of the circuit designed is done using ltspice. While other apps such as multisim live is also used to verify some of the calculations.

Circuit Design

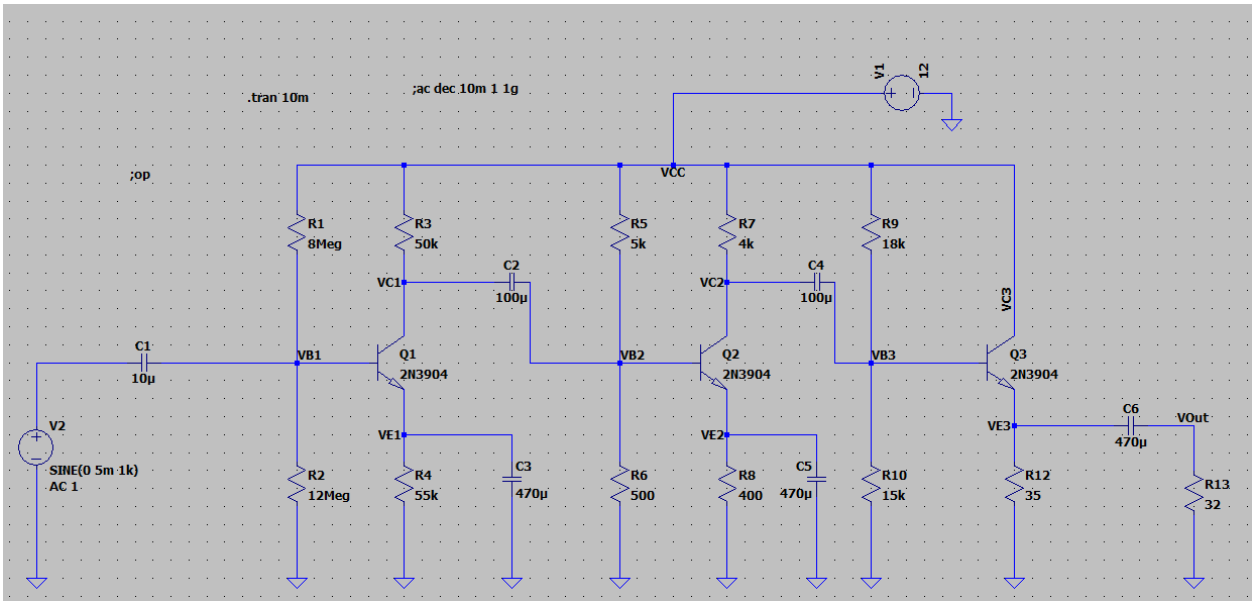

Figure 1: Amplifier Circuit Design

Resistor Name	Resistance (Ω)
R1	8×10^6
R2	12×10^6
R3	50×10^3
R4	55×10^3
R5	5×10^3
R6	500
R7	4×10^3
R8	400
R9	18×10^3
R10	15×10^3
R12	35
R13 (Rout)	32

Table 1: Resistor Resistance Table

Capacitor Name	Capacitance (F)
C1	10×10^{-6}
C2	100×10^{-6}
C3	470×10^{-6}
C4	100×10^{-6}
C5	470×10^{-6}
C6	470×10^{-6}

Table 2: Capacitor Capacitance Table

The circuit designed is a 3-stage cascaded amplifier circuit with 2 common emitter amplifier and 1 common collector amplifier. The 2 common emitter amplifiers are the voltage amplifier of the circuit to amplify the input signal. While the common collector amplifier is the buffer circuit of the, in other words it means that it amplifies the current of the input. Without buffer circuit or the common collector amplifier, the signal cannot be amplified properly because the load resistance is only 32Ω. Hence the output load impedance is very small. The output of common emitter is only suitable for high output impedance load. Thus, to use 32Ω as a load resistance, common collector amplifier must be used to connect a high impedance input source to a low impedance output load.

Cascaded amplifier circuit basically means that the output of one amplifier stage is connected to the input of the next amplifier stage (Cadence, n.d.). All the transistors are connected in series. The reason of choosing this arrangement of amplifier is because the calculation on cascaded amplifiers is easier to understand and to be done. While the other type of arrangement is called as cascode amplifier circuit. In cascode amplifier circuit, the transistors are connected in parallel with each other which results in different characteristics and properties between cascade and cascode.

All the transistor that is used in the design is npn transistor and is 2N3904 type, the rb in this type of transistor is 20Ω. The reason of having 2 common emitter stages in the circuit design is to convert the signal back to in phase. One common emitter stage will cause the signal to be 180 degrees out of phase. Hence by having 2 of it, the signal will return to back in phase. While having 1 common collector stage is to increase the current gain of the signal. Common collector amplifier has a voltage gain of close to 0 which means that it has very minimal effect on the voltage amplitude of the signal. However, current gain is very important because all the

transistors are current operated device (electronicsnotes, n.d.). Hence it is very significant to have ample of current gain to let the whole circuit to function correctly.

Besides that, the resistance of R1 and R2 is also very high. This is because by having high resistance at R1 and R2, the input impedance will be high. This will maximize the voltage transfer from the input to the output which will cause the whole amplifier circuit to get more voltage input and will also results in good amplification of the input signal.

Moreover, in the design there are also 6 capacitors that is used. They act as different roles in the circuit which can be divided into coupling capacitors and bypass capacitors. Capacitor C1, C2, C4 and C6 are coupling capacitors. They play a vital role in the amplifier circuit. They are used while transferring the input AC signal from one stage to another. By having coupling capacitors, only the input AC signal will be transferred while the DC component from the supply will be blocked totally (Ndiritu, 2022). This helps in maintaining all the values of current, voltage and resistance while transferred through stages and the signal transferred will have 0 DC offset. As an example, the existence of C6 will block the DC component and there will be no current flowing through the R13 which is the load resistor when there is no signal input into the amplifier circuit. With no current flowing, the amplifier circuit will not consume power when there is no signal being input into the circuit. This is good as it will save power when the amplifier circuit is not used.

While capacitor C3 and C5 acts as the bypass capacitor. The main function of bypass capacitor is to provide a much lower impedance path for AC signals to pass through and also at the same time blocking DC. In this case the C3 and C5 is conducting the AC away from R4 and R8 to the ground and leaving only DC passing through them. The reason of blocking any AC going through R4 and R8 is because they are known as the emitter resistor. If there is any AC passing through the emitter resistor, the whole amplifier circuit will turn into a negative feedback circuit which will affect the again of the amplifier circuit. In this case C3 and C5 must have larger value of capacitance to ensure that no AC will flow into the emitter resistor.

Analytical Calculations

DC Analysis

The whole amplifier circuit is divided into 3 stages to be calculated and analyzed one by one.

Stage 1

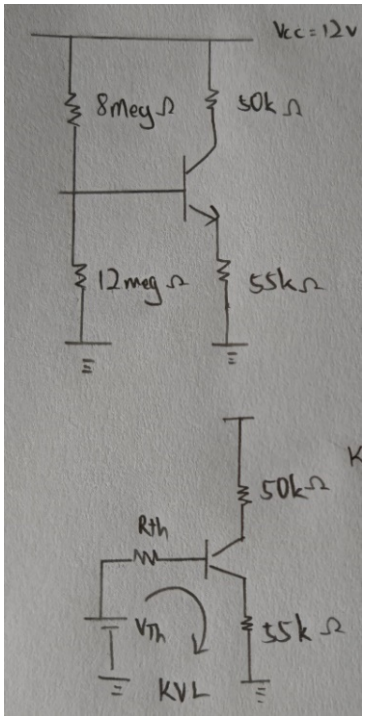

Figure 2: DC Analysis Stage 1

Figure 2 shows the way of simplifying the while circuit using the Thevenin theorem to simplify the circuit to be calculated. The V_{CC} indicates the DC supply to the amplifier circuit which is 12V. The V_{BE} and β values are assumed as what is shown below. They are obtained from the simulation.

$$V_{BE} = 0.593V, \beta = 305, V_{CC} = 12V$$

Below are the steps of converting the resistors of 8 Mega Ω and 12 Mega Ω into one Rth and also the voltage source into Vth. The way of calculating the voltage that is supplied into the base of the transistor which is Vth is calculated using voltage divider rule. The circuit is designed to supply sufficient voltage into the base to let $V_{BE} = 0.593V$ which prevents the transistors to be in cut-off region.

The following part is calculating the current through the stage 1 circuit which includes I_B, I_C and I_E.

$$R_{th} = R1//R2$$
$$= 8 \times 10^6 // 12 \times 10^6$$
$$= 4.8 \times 10^6 \Omega$$

$$V_{th} = \frac{R2}{R1 + R2} \times V_{CC}$$
$$= \frac{12 \times 10^6}{8 \times 10^6 + 12 \times 10^6} \times 12$$
$$= 7.2V$$

Kirchhoff Voltage law, nodal analysis is applied in the circuit to form the equation below.

$$-V_{th} + I_B R_{th} + V_{BE} + 55 \times 10^3 (I_E) = 0$$

To calculate I_B, the I_E is substituted according to the relation $I_E = [\beta + 1]I_B$ so that I_B existed in the equation.

$$-V_{th} + I_B R_{th} + V_{BE} + (55 \times 10^3) \times ([\beta + 1]I_B) = 0$$

Then the equation is arranged, all the values are substituted and calculated.

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (55 \times 10^3) \times ([\beta + 1]I_B)}$$
$$= 3.05 \times 10^{-7} A$$

Then I_C is also calculated using the relation $I_C = \beta I_B$.

$$I_C = \beta I_B$$
$$= 305 \times 3.05 \times 10^{-7}$$
$$= 9.302 \times 10^{-5} A$$

Then I_E is also calculated using the relation $I_E = [\beta + 1]I_B$.

$$I_E = (\beta + 1)I_B$$
$$= (305 + 1) \times 3.05 \times 10^{-7}$$
$$= 9.333 \times 10^{-5} A$$

The following part is calculating the voltage drop across every part of the stage 1 circuit.

$I_C R_C$ is the voltage drop across the resistor 50k**Ω** hence, to calculate the voltage at the collector V_C is to minus the voltage drop from the voltage supply V_{Cc}

$$V_C = V_{CC} - I_C R_C$$
$$= 12 - (9.302 \times 10^{-5})(50 \times 10^3)$$

$$= 7.349V$$

For emitter voltage, V_E because it is also the voltage across the 55kΩ resistor hence it is calculated using the $V = I * R$ formula since that I_E is already known.

$$V_E = I_E R_E$$
$$= (9.333 \times 10^{-5})(55 \times 10^3)$$
$$= 5.133V$$

Then by using the equation $V_{BE} = V_B - V_E$, which means that the voltage drops across V_B and V_E is V_{BE}. V_B is calculated by rearranging the equation to make V_B as the subject.

$$V_B = V_{BE} + V_E$$
$$= 0.593 + 5.133$$
$$= 5.706V$$

Then the same voltage drop concept is also applied to calculate for V_{BC} which is the voltage drop across V_B and V_C.

$$V_{BC} = V_B - V_C$$
$$= 5.706 - 7.349$$
$$= -1.643V$$

Lastly the V_{CE} is also the voltage drop across V_C and V_E.

$$V_{CE} = V_C - V_E$$
$$= 7.349 - 5.133$$
$$= 2.216V$$

Component	Calculation Value
I_B	$3.05 \times 10^{-7} A$
I_E	$9.333 \times 10^{-5} A$
I_C	$9.302 \times 10^{-5} A$
V_B	$5.706V$
V_E	$5.133V$
V_C	$7.349V$
V_{BC}	$-1.643V$
V_{CE}	$2.216V$
V_{BE}	$0.593V$

Table 3: DC Analysis Stage 1

All the DC Analysis calculated values in stage 1 are recorded in table 3. By referring to the values it is obvious that the transistor is not in neither cutoff region nor saturation region.

The cutoff region is where the transistor is not activated where the emitter-base junction in the transistor is not forward biased. In this condition there will be no base current and collector current where I_B and I_C is equal to 0. The transistor will behave like an open circuit when it is in the cutoff region because there will be no current flow from the collector to the emitter.

While for saturation region is where the base current is too high beyond what is needed to make the emitter-base junction forward biased. In this condition the increase in the base current will make minimal to no increase to the collector current. In this case the transistor will act like a short circuit where the current from collector will directly flow to the emitter. To be in the saturation mode the V_{CE} must be smaller than 0.2V which indicates that there are little to no potential difference between the collector and the emitter. At the same time I_B and I_C also must larger than 0.

Hence this stage 1 amplifier circuit is at the forward active region where the conditions are V_{CE} is larger than 0.2V but smaller than V_{CC}, the voltage source. I_B and I_C also must be larger than 0. Lastly the V_{BE} also must be close to 0.7V which is the voltage required to overcome the emitter-base junction and make it forward biased. In stage 1,

$$V_{CE} = 2.216V, V_{BE} = 0.593V, I_B = 3.05 \times 10^{-7} A, I_C = 9.302 \times 10^{-5} A$$

All the values calculated fulfills the condition of forward active region. The reason of the value V_{BC} is negative is because the current is flowing from the collector to the base. Hence, the voltage is higher at the collector which results in a negative value.

Stage 2

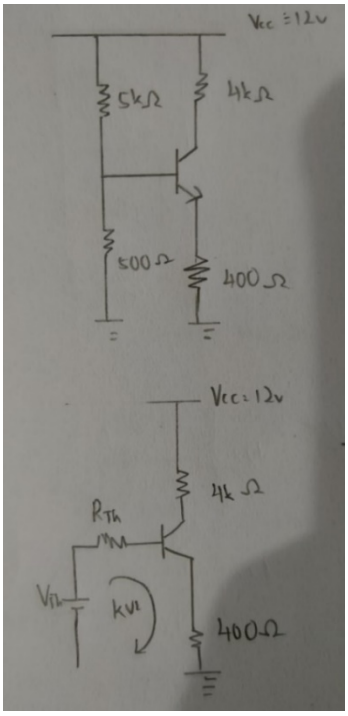

Figure 3: DC Analysis Stage 2

Figure 3 shows the stage 2 of the whole amplifier circuit. The reason of being able to separate them into stages is that there are capacitors between each of them which is the coupling capacitors. The function of coupling capacitors is explained in detail in the circuit design section. The V_{BE} and β values are assumed as what is shown below.

$$V_{BE} = 0.656V, \beta = 319, V_{CC} = 12V$$

The calculations that are done below is similar to what is done in stage 1 where the resistors and the supply are simplified using Thevenin theorem into Rth and Vth. Voltage divider rule is also applied in the calculation and the design to ensure that $V_{BE} = 0.656V$ to prevent the transistor be in the cutoff region.

Below are the calculations of the current that is flowing in stage 2 which are I_B, I_E and I_C

$$R_{th} = R5//R6$$
$$= 5 \times 10^3//500$$
$$= 454.55\Omega$$

$$V_{th} = \frac{R6}{R5 + R6} \times V_{CC}$$
$$= \frac{500}{5 \times 10^3 + 500} \times 12$$
$$= 1.09V$$

Kirchhoff voltage law, nodal analysis is applied to form the equation below.

$$-V_{th} + I_B R_{th} + V_{BE} + 400(I_E) = 0$$

To calculate I_B, the I_E is substituted according to the relation $I_E = [\beta + 1]I_B$ so that I_B existed in the equation.

$$-V_{th} + I_B R_{th} + V_{BE} + (400) \times ([\beta + 1]I_B) = 0$$

Then the equation is arranged, all the values are substituted and I_B is calculated.

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (400) \times ([\beta + 1]I_B)}$$

$$= 3.386 \times 10^{-6} A$$

Then I_C is also calculated using the relation $I_C = \beta I_B$.

$$I_C = \beta I_B$$

$$= 319 \times 3.386 \times 10^{-6}$$

$$= 1.08 \times 10^{-3} A$$

Then I_E is also calculated using the relation $I_E = [\beta + 1]I_B$.

$$I_E = (\beta + 1)I_B$$

$$= (319 + 1) \times 3.386 \times 10^{-6}$$

$$= 1.084 \times 10^{-3} A$$

The following part is calculating the voltage drop across every part of the stage 2 circuit.

$I_C R_C$ is the voltage drop across the resistor 4kΩ hence, to calculate the voltage at the collector V_C is to minus the voltage drop from the voltage supply V_{Cc}.

$$V_C = V_{CC} - I_C R_C$$

$$= 12 - (1.08 \times 10^{-3})(4 \times 10^{3})$$

$$= 7.68V$$

For emitter voltage, V_E because it is also the voltage across the 400Ω resistor hence it is calculated using the $V = I \times R$ formula since that I_E is already known.

$$V_E = I_E R_E$$
$$= (1.084 \times 10^{-3})(400)$$
$$= 0.434V$$

Then by using the equation $V_{BE} = V_B - V_E$, which means that the voltage drops across V_B and V_E is V_{BE}. V_B is calculated by rearranging the equation to make V_B as the subject.

$$V_B = V_{BE} + V_E$$
$$= 0.656 + 0.434$$
$$= 1.09V$$

Then the same voltage drop concept is also applied to calculate for V_{BC} which is the voltage drop across V_B and V_C.

$$V_{BC} = V_B - V_C$$
$$= 1.06 - 7.68$$
$$= -6.59V$$

Lastly the V_{CE} is also the voltage drop across V_C and V_E.

$$V_{CE} = V_C - V_E$$
$$= 7.68 - 0.434$$
$$= 7.246V$$

Component	Calculation Value
I_B	$3.386 \times 10^{-6} A$
I_E	$1.084 \times 10^{-3} A$
I_C	$1.08 \times 10^{-3} A$
V_B	$1.09V$
V_E	$0.434V$
V_C	$7.68V$
V_{BC}	$-6.59V$
V_{CE}	$7.246V$
V_{BE}	$0.656V$

Table 4: DC Analysis Stage 2

All the DC analysis calculated values in stage 2 are recorded in table 4. In stage 2 it is also the same case where the transistor is not in cutoff nor saturation region. In stage 2,

$$V_{CE} = 7.246, V_{BE} = 0.656V, I_B = 3.386 \times 10^{-6} A, I_C = 1.08 \times 10^{-3} A$$

V_{CE} is larger than 0.2V and smaller than V_{CC}. I_B and I_C is larger than 0. V_{BE} is also close to 0.7V. The value of V_{BC} is also negative because the current is flowing from the collector to the emitter.

Stage 3

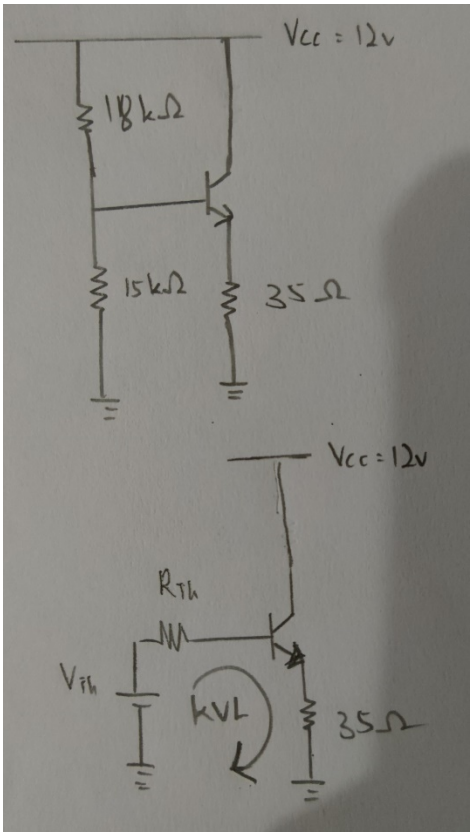

Figure 4: DC Analysis Stage 3

Figure 4 shows the way of simplifying the stage 3 part of the whole amplifier circuit using Thevenin theorem. The V_{BE} and β values are assumed as what is shown below.

$$V_{BE} = 0.78V, \beta = 319, V_{CC} = 12V$$

The calculations done below is also similar to what is done in stage 1 and 2. where the resistors and the supply are simplified using Thevenin theorem into Rth and Vth. Voltage divider rule is also applied in the calculation and the design to ensure that $V_{BE} = 0.78V$ to prevent the transistor be in the cutoff region

Below are the calculations of the current that is flowing in stage 3 which are I_B, I_E and I_C

$$R_{th} = R9//R10$$
$$= 18 \times 10^3 // 15 \times 10^3$$
$$= 8181.82\Omega$$

$$V_{th} = \frac{R10}{R9 + R10} \times V_{CC}$$
$$= \frac{15 \times 10^3}{18 \times 10^3 + 15 \times 10^3} \times 12$$
$$= 5.45V$$

Kirchhoff voltage law, nodal analysis is applied to form the equation below.

$$-V_{th} + I_B R_{th} + V_{BE} + 35(I_E) = 0$$

To calculate I_B, the I_E is substituted according to the relation $I_E = [\beta + 1]I_B$ so that I_B existed in the equation.

$$-V_{th} + I_B R_{th} + V_{BE} + (35) \times ([\beta + 1]I_B) = 0$$

Then the equation is arranged, all the values are substituted and I_B is calculated.

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (35) \times ([\beta + 1]I_B)}$$

$$= 2.6 \times 10^{-4} A$$

Then I_C is also calculated using the relation $I_C = \beta I_B$.

$$I_C = \beta I_B$$

$$= 279 \times 2.6 \times 10^{-4}$$

$$= 7.25 \times 10^{-2} A$$

Then I_E is also calculated using the relation $I_E = [\beta + 1]I_B$.

$$I_E = (\beta + 1)I_B$$

$$= (279 + 1) \times 2.6 \times 10^{-4}$$

$$= 7.28 \times 10^{-2} A$$

The following part is calculating the voltage drop across every part of the stage 2 circuit.

$I_C R_C$ is the voltage drop across the resistor 4kΩ hence, to calculate the voltage at the collector V_C is to minus the voltage drop from the voltage supply V_{Cc}.

$$V_C = V_{CC} - I_C R_C$$

$$= 12 - (7.25 \times 10^{-2})(0)$$

$$= 12V$$

For emitter voltage, V_E because it is also the voltage across the 400Ω resistor hence it is calculated using the $V = I \times R$ formula since that I_E is already known.

$$V_E = I_E R_E$$

$$= (7.28 \times 10^{-2})(35)$$

$$= 2.55V$$

Then by using the equation $V_{BE} = V_B - V_E$, which means that the voltage drops across V_B and V_E is V_{BE}. V_B is calculated by rearranging the equation to make V_B as the subject.

$$V_B = V_{BE} + V_E$$

$$= 0.78 + 2.55$$

$$= 3.33$$

Then the same voltage drop concept is also applied to calculate for V_{BC} which is the voltage drop across V_B and V_C.

$$V_{BC} = V_B - V_C$$

$$= 3.33 - 12$$

$$= -8.67V$$

Lastly the V_{CE} is also the voltage drop across V_C and V_E.

$$V_{CE} = V_C - V_E$$

$$= 12 - 2.55$$

$$= 9.45V$$

Component	Calculation Value
I_B	$2.6 \times 10^{-4} A$
I_E	$7.28 \times 10^{-2} A$
I_C	$7.25 \times 10^{-2} A$
V_B	$3.33V$
V_E	$2.55V$
V_C	$12V$
V_{BC}	$-8.67V$
V_{CE}	$9.45V$
V_{BE}	$0.78V$

Table 5: DC Analysis Stage 3

All the DC analysis calculated values in stage 3 are recorded in table 5. In stage 3 it is also the same case where the transistor is not in cutoff nor saturation region. In stage 3,

$$V_{CE} = 9.45, V_{BE} = 0.78V, I_B = 2.6 \times 10^{-4} A, I_C = 7.25 \times 10^{-2} A$$

V_{CE} is larger than 0.2V and smaller than V_{CC}. I_B and I_C is larger than 0. V_{BE} is also close to 0.7V. The value of V_{BC} is also negative because the current is flowing from the collector to the emitter.

AC Analysis: Gain

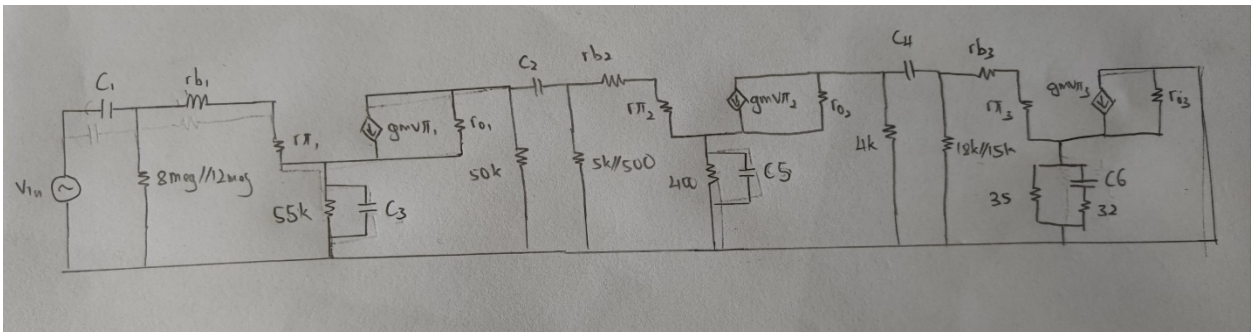

Figure 5: AC Analysis Gain Small Signal Model

Figure 5 shows the whole amplifier circuit that is converted into small signal model to be analyzed and do the calculation.

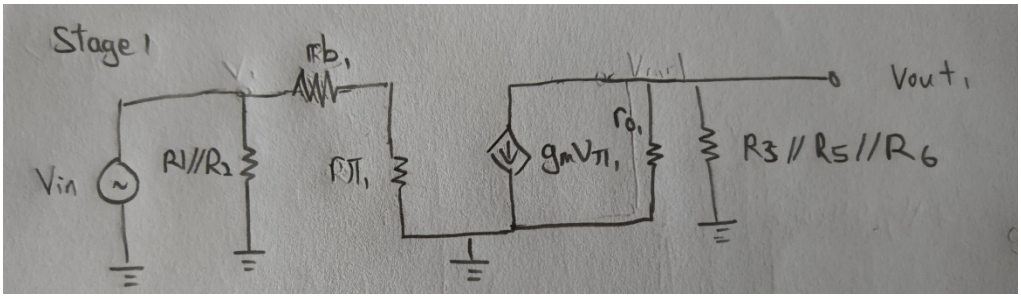

Figure 6: Gain Stage 1 Small Signal Model

Then the whole small signal model is also separated into 3 stages to calculate their gain 1 by one. Figure 6 shows the small signal model of stage 1 amplifier.

Since the transistor model that is used in the whole amplifier circuit is 2N3904. Hence the rb for all the transistors will be 20Ω. While the values of ro, $r\pi$, and gm is all assumed as the values below. All the values are obtained from the simulation.

$$[rb_1 = 20\Omega], [ro_1 = 1.09 \times 10^6\Omega], [r\pi_1 = 8.46 \times 10^4\Omega], [gm_1 = 3.6 \times 10^{-3}s]$$

In order to reduce the complexity of the calculations, all the resistors that are in parallel are combined and calculated.

$$(R1//R2) = (8 \times 10^{-6}//12 \times 10^{-6})$$

$$= 4.8 \times 10^{-6}\Omega$$

$$(R3//R5//R6) = (50 \times 10^3//5 \times 10^3//500)$$

$$= 450.45\Omega$$

Then the output voltage equation is created using the formula $V = I \times R$ where the $gmV\pi$ acts like a dependent source which depends on the voltage across $r\pi$. And also the reason of $gmV\pi$ is negative is because the flow of the current in the circuit is against the current of $gmV\pi$.

$$V_{out1} = -gmV\pi_1(ro_1//R3//R5//R6)$$

Then the voltage across $r\pi$ is calculated using voltage divider rule to get $V\pi$.

$$V\pi_1 = V_{in} \times \frac{r\pi_1}{r\pi_1 + rb_1}$$

$$V\pi_1 = V_{in} \times \frac{8.46 \times 10^4}{8.46 \times 10^4 + 20}$$

$$= \frac{4230}{4231} \cdot V_{in}$$

Then the $V\pi$ is substituted into the output voltage equation to calculate the gain.

$$V_{out1} = -(3.6 \times 10^{-3})(\frac{4230}{4231} \cdot V_{in})(450.26)$$

$$= -1.62V_{in}$$

$$Gain_{Stage\ 1} = \frac{V_{out1}}{V_{in1}}$$

$$Gain_{Stage\ 3} = -1.62$$

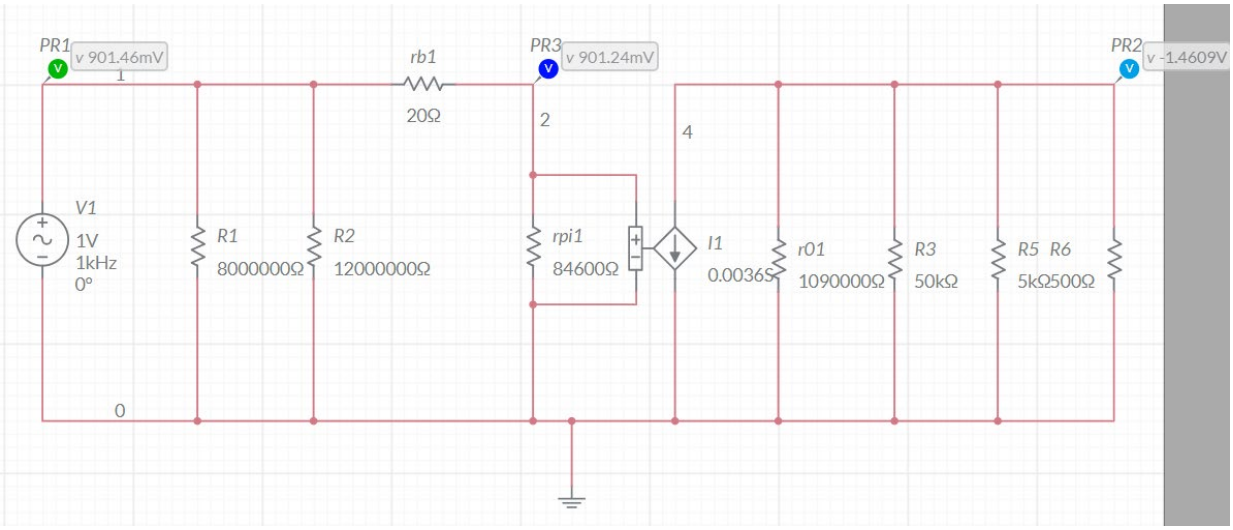

Figure 7: Gain Stage 1 Multisim Verification

In order to verify the gain that is calculated, Multisim is used to simulate the small signal model and the gain of the stage 1 circuit is calculated using the output divide by input.

$$Gain_{Stage\ 1}(Multisim) = \frac{V_{out}}{V_{in}}$$

$$= \frac{-1.46}{0.9}$$

$$= -1.62$$

The gain that is obtained through calculation and simulation is the same which indicates that the calculation done is correct.

The reason of getting a negative gain is because stage 1 is a common emitter configuration of amplifier. In this case the output signal is 180 degrees out of phase compared to the input signal, which is one of the characteristics of common emitter amplifiers.

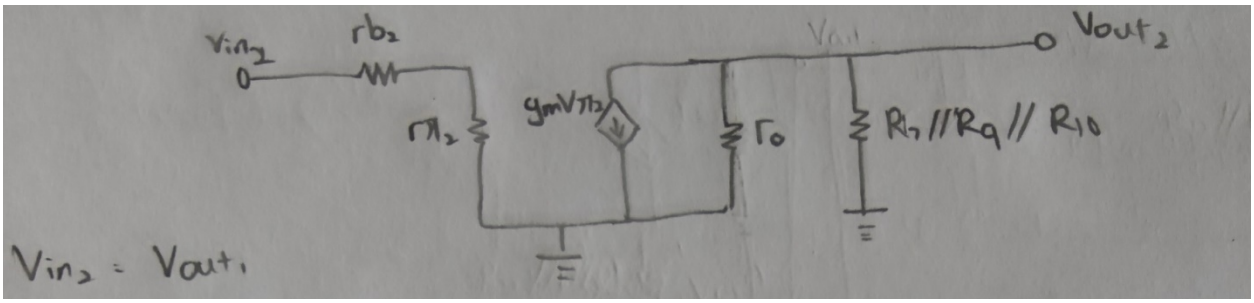

Figure 8: Gain Stage 2 Small Signal Model

Figure 8 shows the small signal model of stage 2. The input of stage 2 is equal to the output of stage 1.

The calculation that will be done in stage 2 is similar to what is done in stage 1 since that they have the same configuration of common emitter. The only difference is that the some of the resistor values are different which also includes the ro, $r\pi$ and also the gm value. The values of ro, $r\pi$ and gm are obtained from the simulation. rb is also 20Ω because the transistor model is also 2N3094.

$$[rb_2 = 20\Omega], [ro_2 = 9.86 \times 10^4\Omega], [r\pi_2 = 7.63 \times 10^3\Omega], [gm_2 = 4.17 \times 10^{-2}s]$$

All the resistor values that are in parallel are also simplified.

$$(R7//R9//R10) = (4 \times 10^3//18 \times 10^3//15 \times 10^3)$$
$$= 2686.57\Omega$$
$$V_{in2} = V_{out1}$$

Firstly, the equation to find the output of stage 1 is also created using voltage divider rule.

$$V_{out2} = -gmV\pi_2(ro_2//R7//R9//R10)$$

Then the voltage across $r\pi$ is calculated using voltage divider rule to get $V\pi$.

$$V\pi_2 = V_{in2} \times \frac{r\pi_2}{r\pi_2 + rb_2}$$
$$V\pi_2 = V_{in2} \times \frac{7.63 \times 10^3}{7.63 \times 10^3 + 20}$$
$$= \frac{763}{765} \cdot V_{in2}$$

Then the $V\pi$ is substituted into the output voltage equation to calculate the gain.

$$V_{out2} = -(4.17 \times 10^{-2})(\frac{763}{765} \cdot V_{in2})(2615.31)$$

$$= -108.77V_{in2}$$

$$Gain_{Stage\ 2} = \frac{V_{out2}}{V_{in2}}$$

$$Gain_{Stage\ 2} = -108.77$$

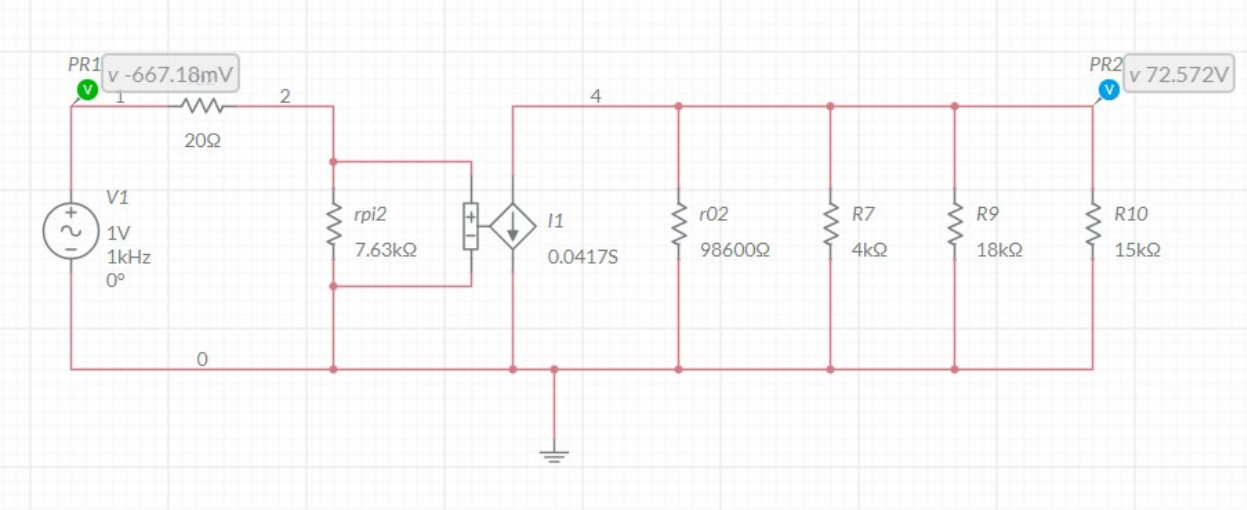

Figure 9: Gain Stage 2 Multisim Verification

Multisim is also used to verify the calculation done and the gain is calculated using output divided by input.

$$Gain_{Stage\ 2}(Multisim) = \frac{V_{out}}{V_{in}}$$

$$= \frac{72.57}{-0.67}$$

$$= -108.31$$

The gain that is obtained through calculations and the simulation are close to each other and can be assumed as the same. The reason of having slightly different gain is because during the calculations many values had been rounded off which results in the slightly inaccurate in the results.

The gain in stage 2 is also negative because it is also a common emitter configuration.

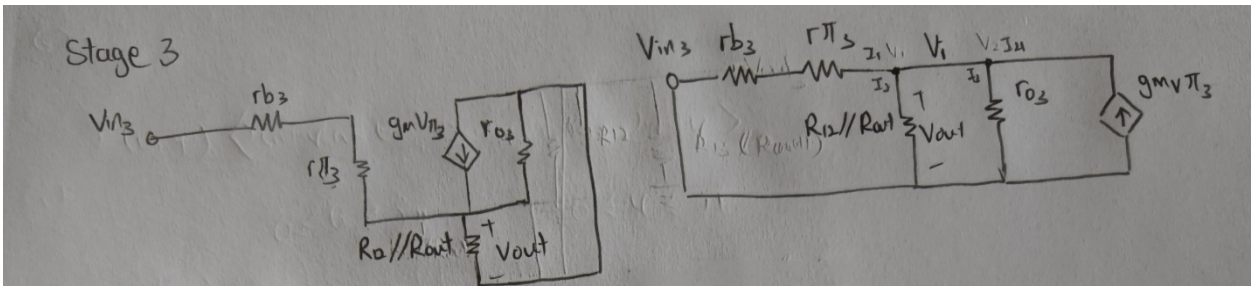

Figure 10: Gain Stage 3 Small Signal Model

Figure 10 shows the small signal model of the stage 3. The input of stage 3 is also the output of stage 2. The calculations that are done in stage 3 to calculate the gain is different with what is done in stage 1 and 2. This is because the configuration of stage 3 is common collector where the output is located at the emitter of the transistor. Hence after converting stage 3 into small signal model, the model is further simplified into a circuit that is easier to apply nodal analysis.

The values of ro, $r\pi$ and gm are obtained from the simulation. rb is also 20Ω because the transistor model is also 2N3094.

$$[rb_3 = 20\Omega], [ro_3 = 1.5 \times 10^3\Omega], [r\pi_3 = 99.6\Omega], [gm_3 = 2.45s]$$

All the resistor values that are in parallel are also simplified.

$$(R12//R_{out}) = (35//32)$$

$$= 16.72\Omega$$

$$V_{in3} = V_{out2}$$

Nodal analysis is applied to the stage 3 circuit to create the equation below.

$$I_1 + I_2 + I_3 + I_4 = 0$$

Then the variables and values are all substituted into the equations.

$$\frac{V_1 - V_{in3}}{rb_3 + r\pi_3} + \frac{V_1}{R12//R_{out}//ro_3} - gmV\pi_3 = 0$$

$$\frac{V_1 - V_{in3}}{119.6} + \frac{V_1}{16.53} - 2.45V\pi_3 = 0$$

Then the equation for $V\pi_3$ is also created using voltage divider rule.

$$V\pi_3 = \frac{r\pi_3}{rb_3 + r\pi_3} \times (V_{in3} - V_1)$$

$$= \frac{249}{299} \times (V_{in3} - V_1)$$

Then $V\pi_3$ is substituted back to the nodal analysis equation and the node V_1 is calculated.

$$\frac{V_1 - V_{in3}}{119.6} + \frac{V_1}{16.53} - 2.45(\frac{249}{299} \times (V_{in3} - V_1)) = 0$$

$$\frac{V_1}{119.6} - \frac{V_{in3}}{119.6} + \frac{V_1}{16.45} - 2.04V_{in3} + 2.04V_1 = 0$$

$$2.11V_1 = 2.04V_{in3}$$

$$V_1 = 0.97V_{in3}$$

Then by looking at figure 10 it is obvious that the V_1 is also the V_{out3}. Hence,

$$V_1 = V_{out3}$$

$$V_{out3} = 0.97V_{in3}$$

$$Gain_{Stage\ 3} = \frac{V_{out3}}{V_{in3}}$$

$$Gain_{Stage\ 3} = 0.97$$

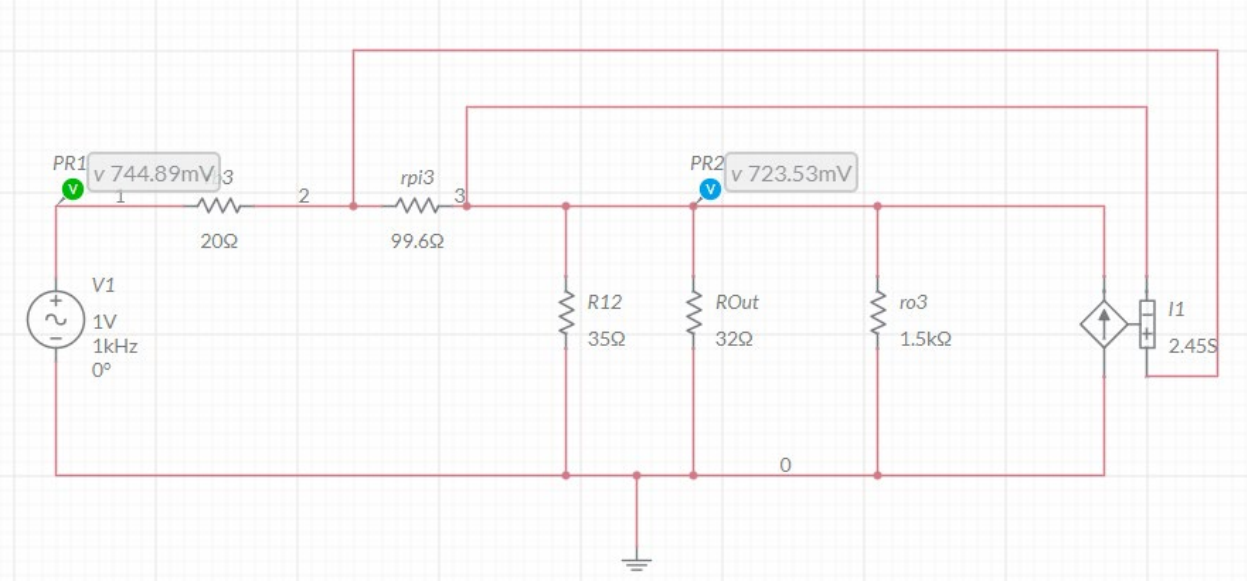

Figure 11: Gain Stage 3 Multisim Verification

Lastly, Multisim is also used to verify the calculations and the gain is calculated by dividing output with input.

$$Gain_{Stage\ 3}(Multisim) = \frac{V_{out}}{V_{in}}$$

$$= \frac{0.724}{0.745}$$

$$= 0.97$$

The gain that is obtained through calculation is similar to what is obtained in the simulation. This verifies that the calculations are correct.

In stage 3 the gain is not negative because the output signal is in phase with the input signal. Besides that, the gain is also close to 1 for common collector. This is because the common emitter configuration is a buffer circuit and it is designed to have current gain instead of voltage gain.

Finally, the whole circuit gain is calculated by multiplying all the gain from each stage which is represented as the equation below.

$$Overall\ Circuit\ Gain = Gain_{Stage\ 1} \times Gain_{Stage\ 2} \times Gain_{Stage\ 3}$$
$$= (-1.62) \times (-108.77) \times (0.97)$$
$$= 170.92$$

Then to convert the gain into log scale, the calculations are done as below.

$$Overall\ Circuit\ Gain\ in\ dB = 20\log(Overall\ Circuit\ Gain)$$
$$= 20\log(170.92)$$
$$= 44.66dB$$

While from the simulation the gain is 39.87dB and the error is also calculated.

$$From\ Simulation\ Gain = 39.87dB$$
$$Error = \frac{Small\ Signal\ Model\ Calculated\ Gain - Simulation\ Gain}{Simulation\ Gain} \times 100\%$$
$$= 12.04\%$$

Besides of using the small signal model to calculate the gain of the common emitter stages of the designed amplifier circuit, there is an easier way to calculate the overall gain of the circuit which is using the following formula (Electronic Tutorials, n.d.).

$$Gain = \frac{R_{Load}}{R_{Emitter}}$$

R_{Load} is the resistance on the collector circuit of the common emitter stages while $R_{Emitter}$ is the resistance on the emitter circuit.

$$Gain_{Stage\ 1} = -\frac{R_{Load}}{R_{Emitter}}$$

$$= -\frac{R3}{R4}$$

$$= -\frac{50 \times 10^3}{55 \times 10^3}$$

$$= -0.91$$

$$Gain_{Stage\ 2} = -\frac{R_{Load}}{R_{Emitter}}$$

$$= -\frac{R7}{R8}$$

$$= -\frac{4 \times 10^3}{400}$$

$$= -10$$

While for gain stage 3 is assumed as 1 because it is a common collector configuration where it only amplifies the current.

$$Gain_{Stage\ 3} = 1$$

Then the overall gain is calculated using the formula below.

$$Overall\ Gain = Gain_{Stage\ 1} \times Gain_{Stage\ 2} \times Gain_{Stage\ 3}$$

$$= -0.91 \times (-100) \times 1$$

$$= 91$$

Then to convert the gain into log scale, the calculations are done as below.

$$Overall\ Gain\ in\ dB = 20\log(Overall\ Gain)$$

$$= 20\log(91)$$

$$= 39.18dB$$

While from the simulation the gain is 39.87dB and the error is also calculated.

$$From\ Simulation\ Gain = 39.87dB$$

$$Error = \left|\frac{Overall\ Gain - Simulation\ Gain}{Simulation\ Gain}\right| \times 100\%$$

$$= 1.73\%$$

AC Analysis: Lower Cutoff Frequency

The steps of finding the lower cutoff frequency of the whole amplifier circuit are to find the resistance for all the capacitors in the whole amplifier circuit using short circuit time constant method.

RC1

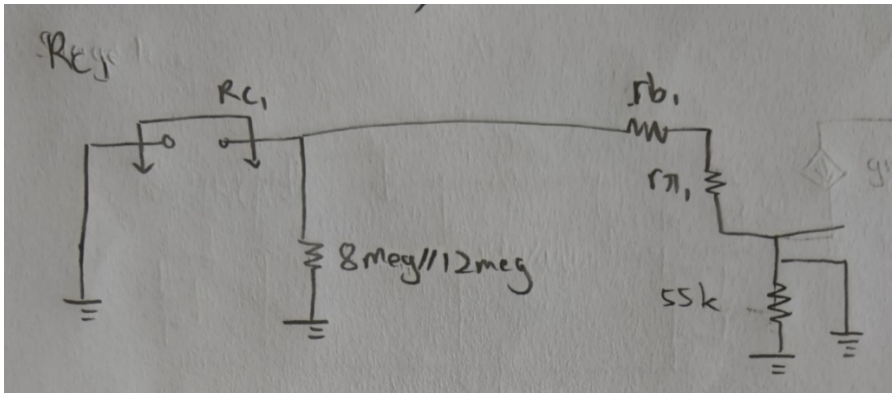

Figure 12: RC1 Small Signal Model

The C1 value and the assumptions on $r\pi_1$ and β_1 are as below. The assumptions are made based on the simulation.

$$[C_1 = 10 \times 10^{-6} F], [rb_1 = 20\Omega], [r\pi_1 = 8.46 \times 10^4 \Omega], [\beta_1 = 305]$$

$$RC1 = (R1)//(R2)//(rb_1 + r\pi_1)$$
$$= (8 \times 10^6)//(12 \times 10^6)//(rb_1 + r\pi_1)$$
$$= 83154.06\Omega$$

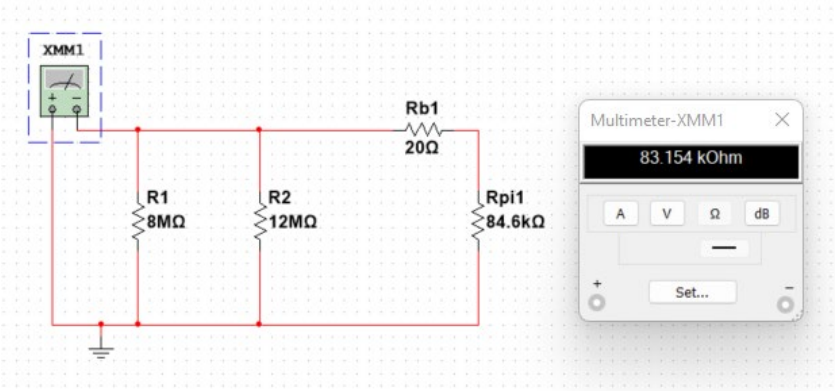

Figure 13: RC1 Multisim Verification

RC2

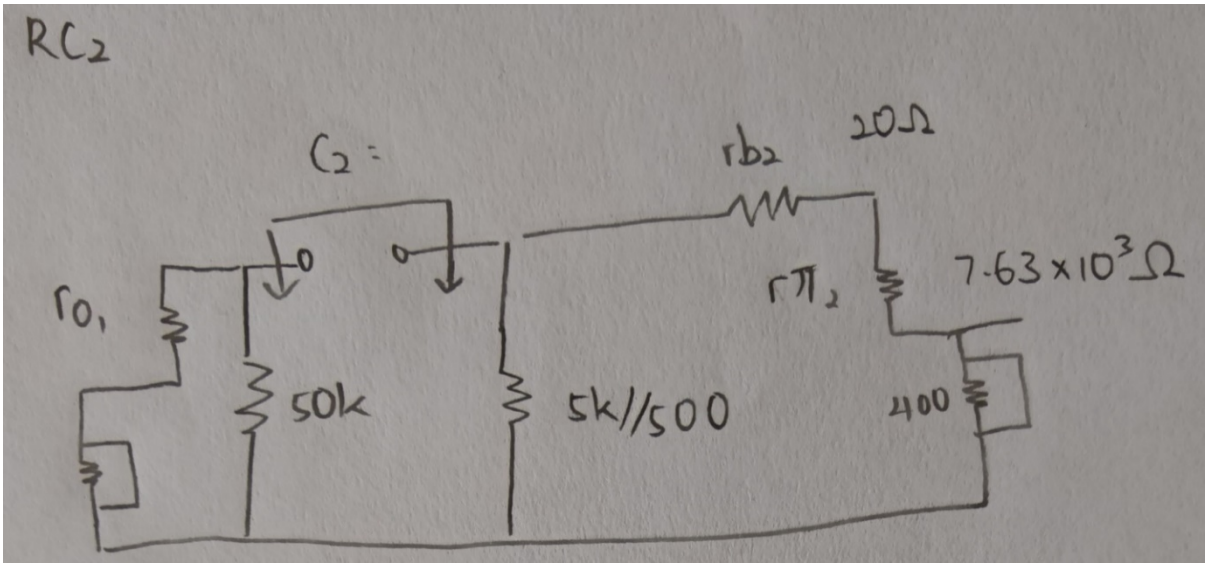

Figure 14: RC2 Small Signal Model

The C2 value and the assumptions on ro_1 and rb_2 are as below. The assumptions are made based on the simulation.

$$[C_2 = 100 \times 10^{-6}F]\,,[ro_1 = 1.09 \times 10^6\Omega]\,,[rb_2 = 20\Omega]\,,[r\pi_2 = 7.63 \times 10^3\Omega]$$

$$RC2 = [ro_1//R3] + [(R5)//(R6)//(rb_2 + r\pi_1)]$$
$$= [ro_1//(50 \times 10^3)] + [(5 \times 10^3)//(500)//(rb_2 + r\pi_1)]$$
$$= 48236.07\Omega$$

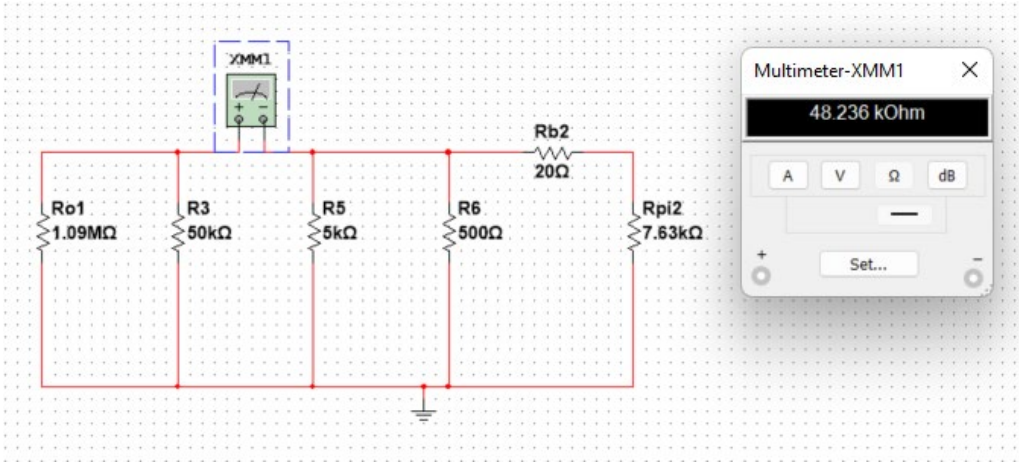

Figure 15: RC2 Multisim Verification

RC3

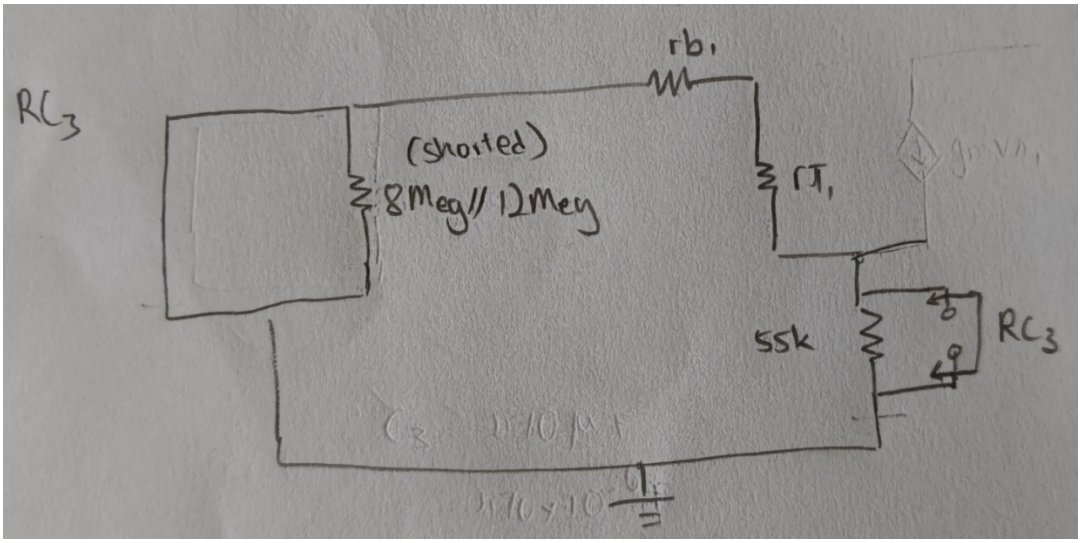

Figure 16: RC3 Small Signal Model

The C3 value and the assumptions on $r\pi_1$ and β_1 are as below. The assumptions are made based on the simulation.

$$[C_3 = 470 \times 10^{-6} F], [rb_1 = 20\Omega], [r\pi_1 = 8.46 \times 10^4 \Omega], [\beta_1 = 305]$$

$$RC3 = (R4)//\frac{rb_1 + r\pi_1}{\beta_1 + 1}$$

$$= (55 \times 10^3)//\frac{rb_1 + r\pi_1}{\beta_1 + 1}$$

$$= 275.16\Omega$$

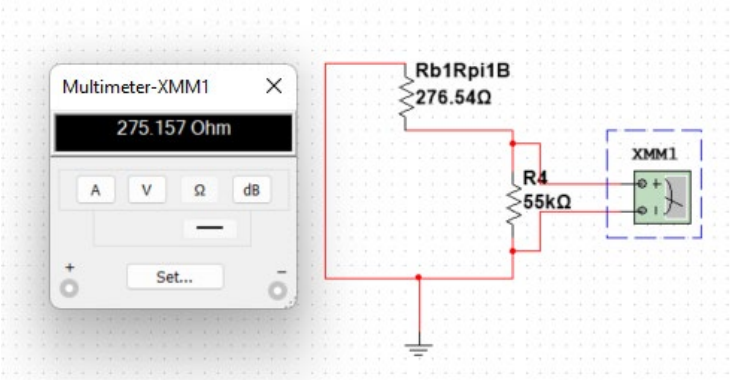

Figure 17: RC3 Multisim Verification

RC4

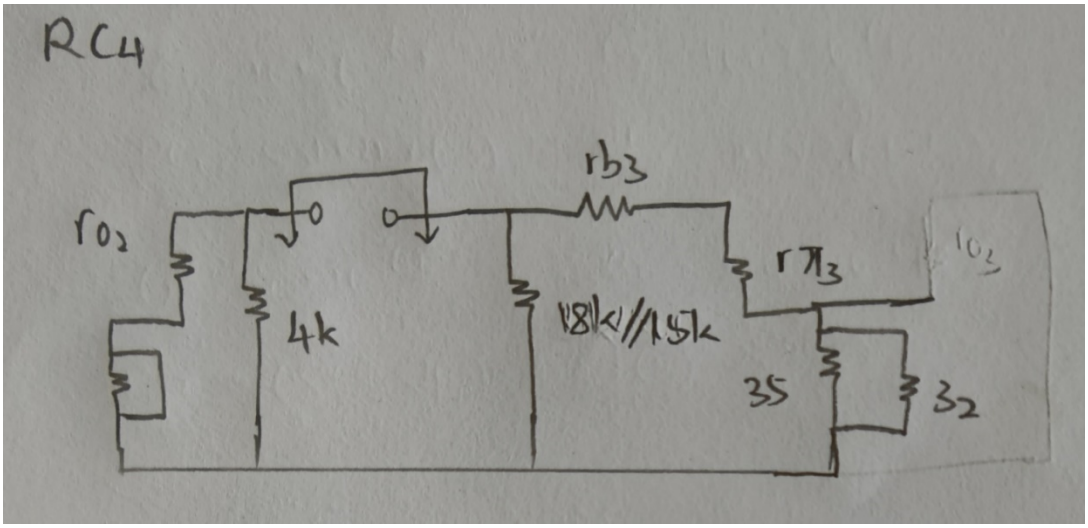

Figure 18: RC4 Small Signal Model

The C4 value and the assumptions on ro_2, $r\pi_3$ and β_3 are as below. The assumptions are made based on the simulation.

$$[C_4 = 100 \times 10^{-6} F], [rb_3 = 20\Omega], [ro_2 = 9.86 \times 10^4 \Omega], [r\pi_3 = 99.6\Omega], [\beta_3 = 279]$$

$$RC4 = [ro_2 // R7] + [(R9) // (R10) // [(R11 // R12)(\beta_3 + 1) + rb_3 + r\pi_3]]$$

$$RC4 = [ro_2 // (4 \times 10^3)] + [(18 \times 10^3) // (15 \times 10^3) // [(35 // 32)(\beta_3 + 1) + rb_3 + r\pi_3]]$$

$$= 6869.34\Omega$$

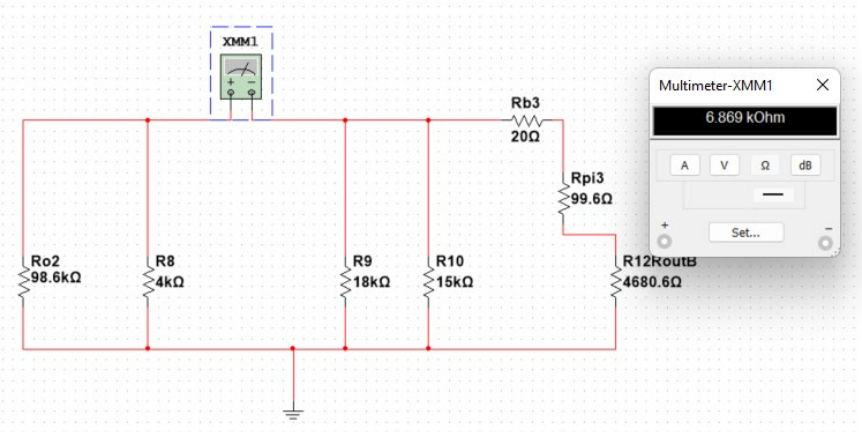

Figure 19: RC4 Multisim Verification

RC5

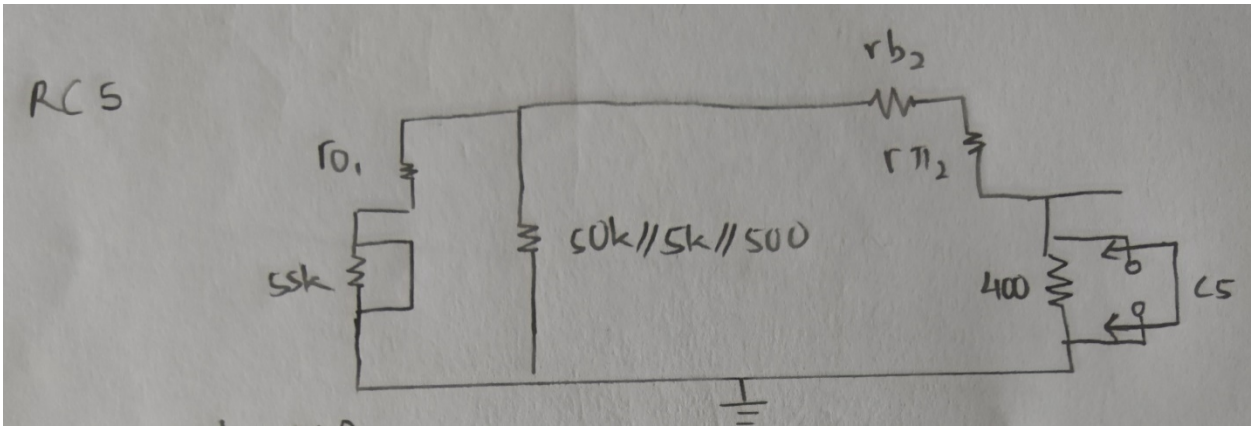

Figure 20: RC5 Small Signal Model

The C5 value and the assumptions on $r\pi_2$, ro_1 and β_2 are as below. The assumptions are made based on the simulation.

$$[C_5 = 470 \times 10^{-6} F], [ro_1 = 1.09 \times 10^6 \Omega], [rb_2 = 20\Omega], [r\pi_2 = 7.63 \times 10^3 \Omega], [\beta_2 = 319]$$

$$RC5 = R8 // \frac{[ro_1 // R3 // R5 // R6] + rb_2 + r\pi_2}{\beta_2 + 1}$$

$$RC5 = 400 // \frac{[ro_1 // 50 \times 10^3 // 5 \times 10^3 // 500] + rb_2 + r\pi_2}{\beta_2 + 1}$$

$$= 23.8\Omega$$

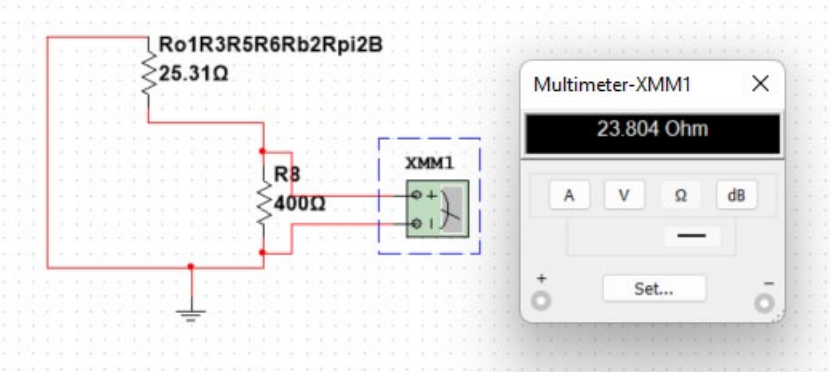

Figure 21: RC5 Multisim Verification

RC6

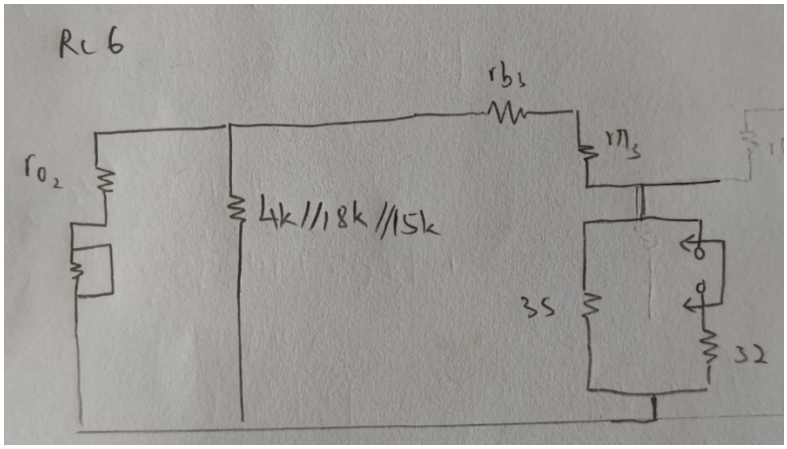

Figure 22: RC6 Small Signal Model

The C5 value and the assumptions on $r\pi_3$, ro_2 and β_3 are as below. The assumptions are made based on the simulation.

$$[C_6 = 470 \times 10^{-6} F], [ro_2 = 9.86 \times 10^4 \Omega], [rb_3 = 20\Omega], [r\pi_3 = 99.6\Omega], [\beta_3 = 279]$$

$$RC6 = R11 + //[R12 // \frac{[ro_2 // R7 // R9 // R10] + rb_3 + r\pi_3}{\beta_3 + 1}]$$

$$RC6 = 32 + //[35 // \frac{[ro_2 // 4 \times 10^3 // 18 \times 10^3 // 15 \times 10^3] + rb_3 + r\pi_3}{\beta_3 + 1}]$$

$$= 39.64\Omega$$

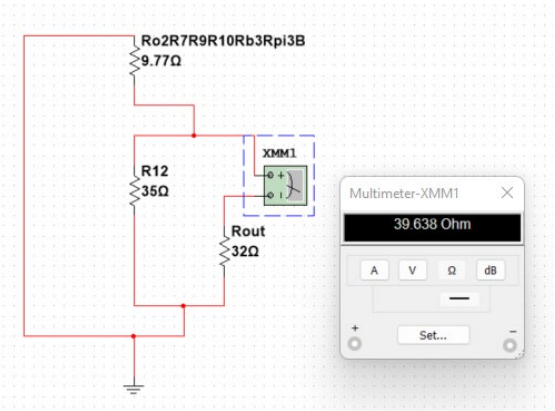

Figure 23: RC6 Multisim Verification

	Capacitance, C, (F)	Resistance, Rc, (Ω)	$\frac{1}{Rc \times C}$
C_1 (Stage 1)	100×10^{-6}	83154.06	1.2
C_2 (Stage 1)	100×10^{-6}	48236.07	0.21
C_3 (Stage 1)	470×10^{-6}	275.16	7.73
C_4 (Stage 2)	100×10^{-6}	6869.34	1.46
C_5 (Stage 2)	470×10^{-6}	23.8	89.4
C_6 (Stage 3)	470×10^{-6}	39.64	53.67

Table 6: Capacitor Resistance Value

Table 6 record all the capacitance of the capacitor and their corresponding resistance.$\frac{1}{Rc \times C}$ is also recorded in the table to make the calculation easier.

The lower cutoff frequency of the amplifier circuit is calculated using the formula below. They are not divided into stages.

$$F_{lower} = \frac{1}{2\pi}\left[\frac{1}{Rc_1 \times C_1} + \frac{1}{Rc_2 \times C_2} + \frac{1}{Rc_3 \times C_3} + \frac{1}{Rc_4 \times C_4} + \frac{1}{Rc_5 \times C_5} + \frac{1}{Rc_6 \times C_6}\right]$$

$$= 24.46Hz$$

The error is calculated.

$$From\ Simulation\ F_{lower} = 17.71Hz$$

$$Error = \frac{Calculated\ Lower\ Cutoff\ Freq - Simulation\ Lower\ Cutoff\ Freq}{Simulation\ Lower\ Cutoff\ Freq} \times 100\%$$

$$= 38.11\%$$

The lower cutoff frequency of the amplifier circuit is also calculated using a different method which is the transfer function method. By using this method, all the capacitors are divided into stages which is shown in table 6. Then all the lower cutoff frequency of each stage is calculated separately.

This is transfer function of cascaded amplifier formula to combine the lower cutoff frequency according to stages,

$$F_{lower} = 1.1 \times \sqrt{{F_{lower1}}^2 + {F_{lower2}}^2 + {F_{lower3}}^2}$$

The lower cutoff frequency of each stage is calculated.

$$F_{lower1} = \frac{1}{2\pi}[1.2 + 0.21 + 7.73]$$

$$= 1.45Hz$$

$$F_{lower2} = \frac{1}{2\pi}[1.46 + 89.4]$$

$$= 14.46Hz$$

$$F_{lower3} = \frac{1}{2\pi}[53.67]$$

$$= 8.54Hz$$

Then the formula is applied to calculate the overall lower cutoff frequency.

$$F_{lower} = 1.1 \times \sqrt{1.45^2 + 14.46^2 + 8.54^2}$$

$$= 18.54Hz$$

The error is calculated.

$$From\ Simulation\ F_{lower} = 17.71Hz$$

$$Error = \frac{Transfer\ Function\ Lower\ Cutoff\ Freq - Simulation\ Lower\ Cutoff\ Freq}{Simulation\ Lower\ Cutoff\ Freq} \times 100\%$$

$$= 4.69\%$$

Simulation Results

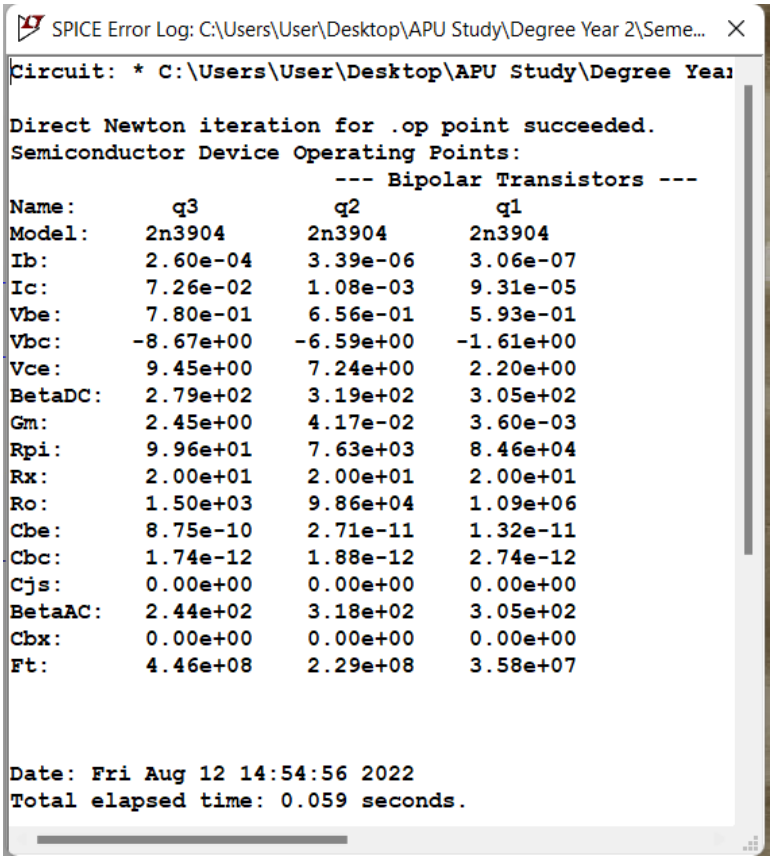

Figure 24: Spice Error Log Result

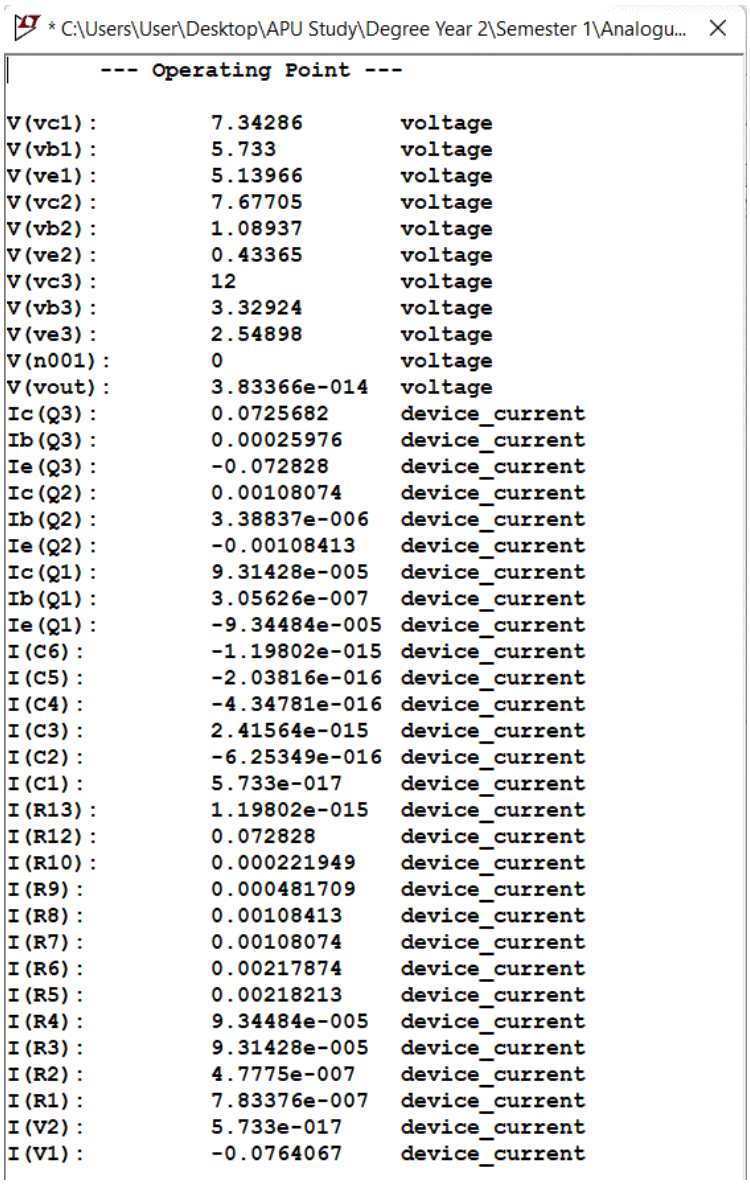

Figure 25: Operating Point Result

Figure 24 and 25 shows the spice error log and the operating point result of the simulation of the circuit design. Many assumption values that are used during calculations are obtained from here such as V_{BE} and β while calculating the DC analysis and also ro, $r\pi$ and gm while calculating the AC analysis gain.

Component	Simulation Value
I_B	$3.06 \times 10^{-7} A$
I_E	$9.345 \times 10^{-5} A$
I_C	$9.31 \times 10^{-5} A$
V_B	$5.733V$
V_E	$5.139V$
V_C	$7.342V$
V_{BC}	$-1.61V$
V_{CE}	$2.2V$
V_{BE}	$0.593V$

Table 7: Stage 1 Simulation Value

Component	Simulation Value
I_B	$3.39 \times 10^{-6} A$
I_E	$1.084 \times 10^{-3} A$
I_C	$1.08 \times 10^{-3} A$
V_B	$1.09V$
V_E	$0.434V$
V_C	$7.68V$
V_{BC}	$-6.59V$
V_{CE}	$7.24V$
V_{BE}	$0.656V$

Table 8: Stage 2 Simulation Value

Component	Simulation Value
I_B	$2.6 \times 10^{-4} A$
I_E	$7.28 \times 10^{-2} A$
I_C	$7.26 \times 10^{-2} A$
V_B	$3.33V$
V_E	$2.55V$
V_C	$12V$
V_{BC}	$-8.67V$
V_{CE}	$9.45V$
V_{BE}	$0.78V$

Table 9: Stage 3 Simulation Value

Table 7, 8 and 9 records the important components from the spice error log and the operating point result to be analyzed. Referring all the values obtained from figure 24, it is known that all the transistors in the amplifier circuit are operating in the forward active region. This is because all the V_{BE} of the transistors are all close to 0.7V, I_B and I_C are not equals to 0 and V_{CE} is also more than 0.2V. The operating region that is observed in the simulation is also verified by the calculations.

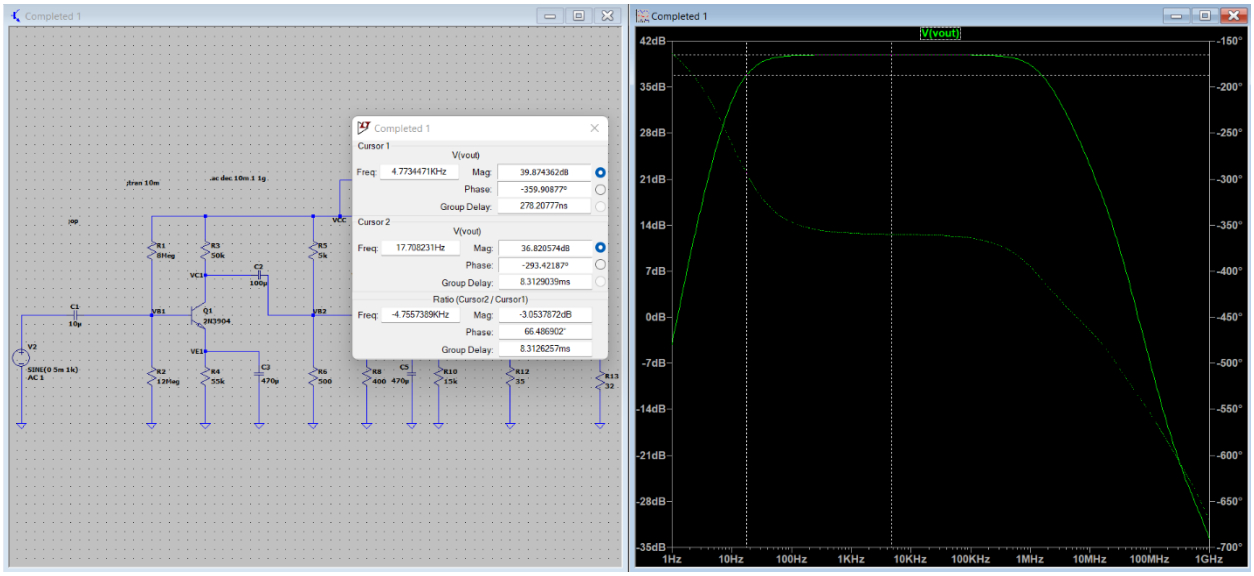

Figure 26: Lower Cutoff Frequency Result

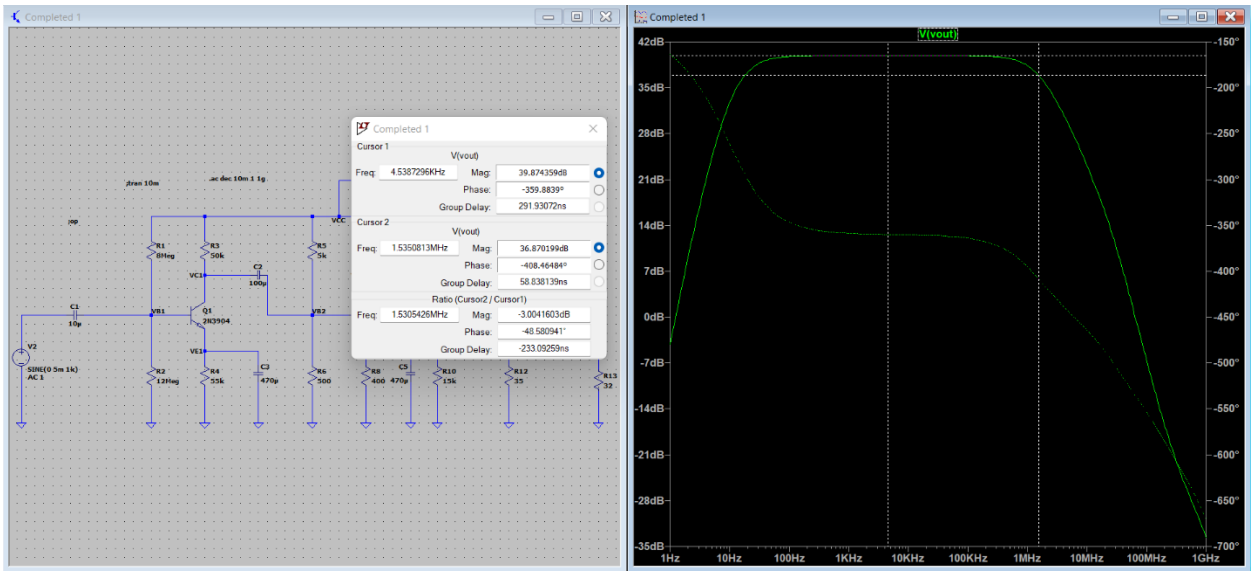

Figure 27: Upper Cutoff Frequency Result

Figure 26 and 27 shows the maximum gain of the whole amplifier circuit which is 39.87dB which meets the requirement of between 38 and 40dB. Besides that, figure 26 also shows the lower cutoff frequency of the amplifier circuit, which is the lower frequency 3dB lesser than the maximum gain. The lower cutoff frequency of the amplifier circuit is 17.71Hz which also fulfill the requirement of between 0 to 300Hz. While the higher cutoff frequency is 1.54MHz which also fulfill the requirement of between 1MHz to 10MHz. Therefore, the bandwidth of the amplifier circuit is 1.54MHz

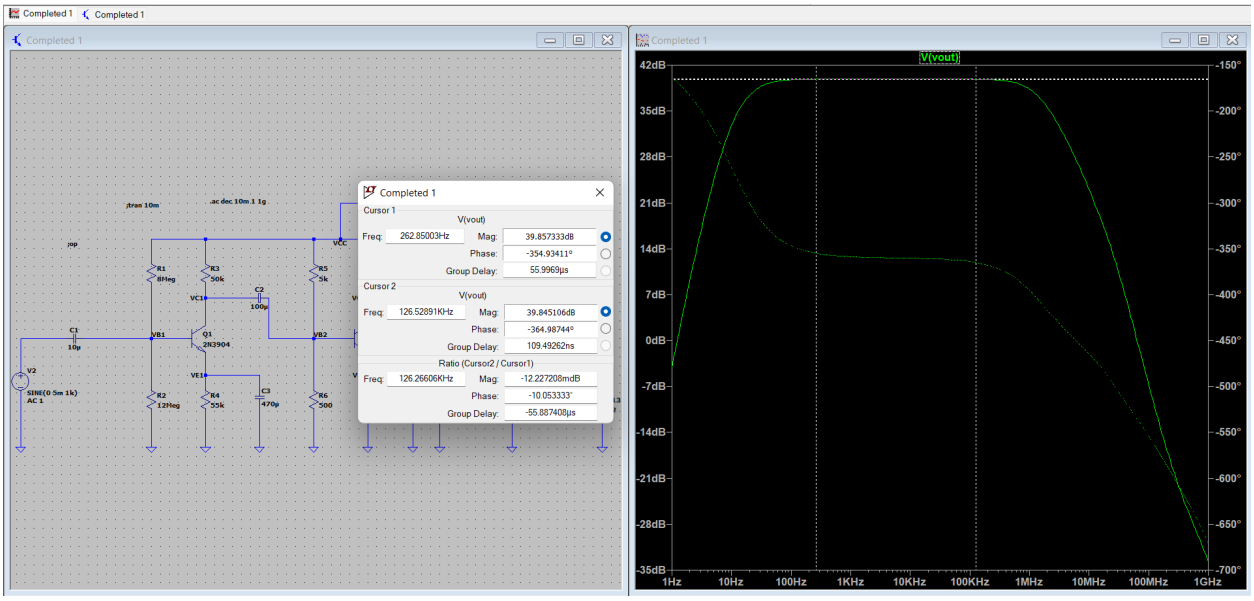

Figure 28: Max Gain Range

Figure 28 shows the rough range of frequency where the gain is at maximum. The range of maximum gain is from 262.85Hz to 126.53kHz.

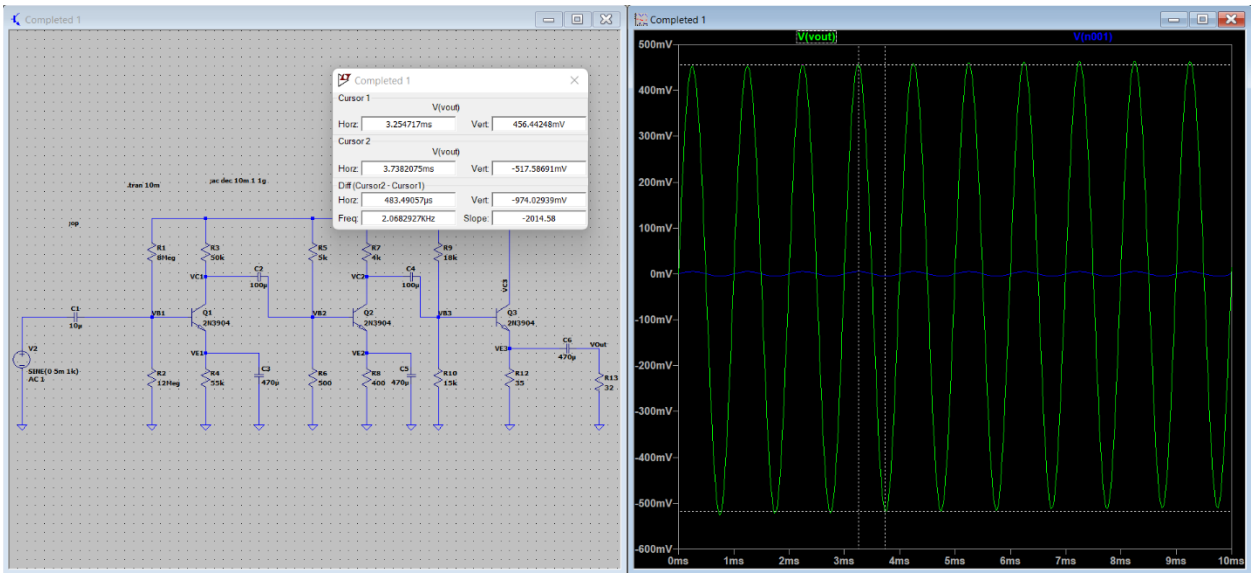

Figure 29: Input AC Signal and Output AC Signal

Figure 29 shows the transient process of the input signal and the output signal of the amplifier circuit. The input signal is a perfect sin wave while the output is also a perfect sin wave that have no cutoff or clipping at any of the lower or upper peak. The amplifier circuit have the capability to fully recover the input signal and no distortion happened. This is very good for the

amplifier is because the input signal can be perfectly amplified by the amplifier signal without any changes.

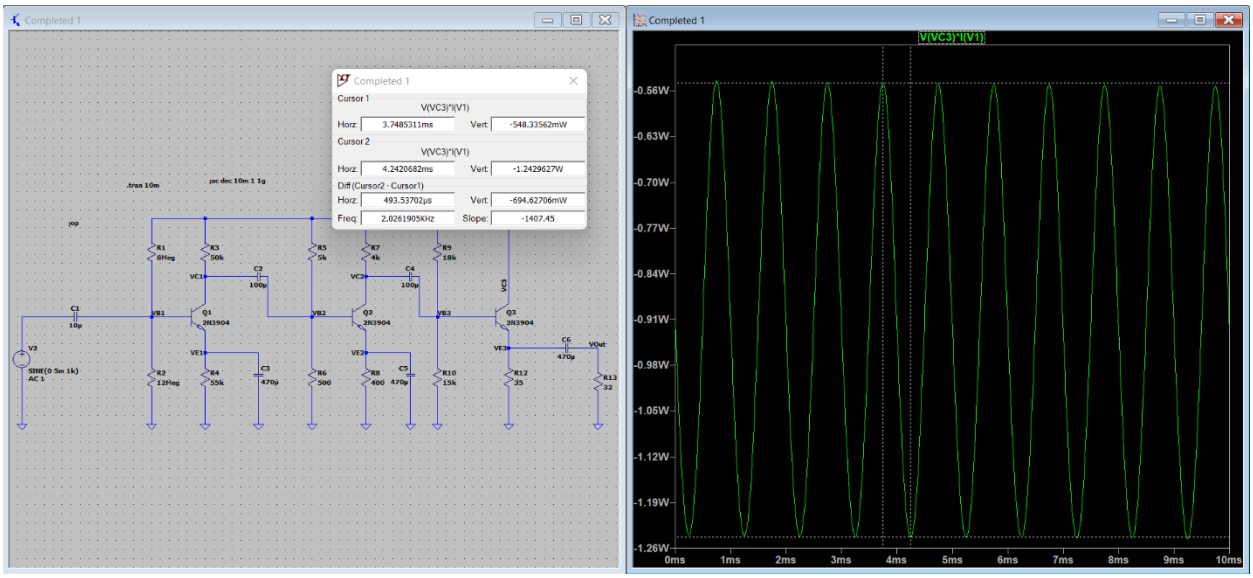

Figure 30: Power Consumption

Figure 30 shows the power consumption of the amplifier circuit. To calculate the average power consumption the formula,

$$\frac{Power_{Higher\ \ Peak} + Power_{Lower\ Peak}}{2}$$

$$Power\ Consumption = \frac{-0.548 - 1.243}{2}$$

$$= 0.896W$$

According to the calculations done above the power consumption is also lower than 1W which also meets the requirement of power consumption of lower than 1W.

Discussion

Component	Calculation Value	Simulation Value	Error Percentage, $\lvert\frac{Simulation-Calculation}{Simulation}\rvert \times 100\%$
I_B	$3.05 \times 10^{-7}A$	$3.06 \times 10^{-7}A$	0.33%
I_E	$9.333 \times 10^{-5}A$	$9.345 \times 10^{-5}A$	0.13%
I_C	$9.302 \times 10^{-5}A$	$9.31 \times 10^{-5}A$	0.09%
V_B	$5.706V$	$5.733V$	0.47%
V_E	$5.133V$	$5.139V$	0.12%
V_C	$7.349V$	$7.342V$	0.01%
V_{BC}	$-1.643V$	$-1.61V$	2.05%
V_{CE}	$2.216V$	$2.2V$	0.73%
V_{BE}	$0.593V$	$0.593V$	0%

Table 10: DC Analysis Stage 1 Error

Component	Calculation Value	Simulation Value	Error Percentage, $\lvert\frac{Simulation-Calculation}{Simulation}\rvert \times 100\%$
I_B	$3.386 \times 10^{-6}A$	$3.39 \times 10^{-6}A$	0.12%
I_E	$1.084 \times 10^{-3}A$	$1.084 \times 10^{-3}A$	0%
I_C	$1.08 \times 10^{-3}A$	$1.08 \times 10^{-3}A$	0%
V_B	$1.09V$	$1.09V$	0%
V_E	$0.434V$	$0.434V$	0%
V_C	$7.68V$	$7.68V$	0%
V_{BC}	$-6.59V$	$-6.59V$	0%
V_{CE}	$7.246V$	$7.24V$	0.08%
V_{BE}	$0.656V$	$0.656V$	0%

Table 11: DC Analysis Stage 2 Error

Component	Calculation Value	Simulation Value	Error Percentage, $\lvert\frac{Simulation-Calculation}{Simulation}\rvert \times 100\%$
I_B	$2.6 \times 10^{-4}A$	$2.6 \times 10^{-4}A$	0%
I_E	$7.28 \times 10^{-2}A$	$7.28 \times 10^{-2}A$	0
I_C	$7.25 \times 10^{-2}A$	$7.26 \times 10^{-2}A$	0.14%
V_B	$3.33V$	$3.33V$	0%
V_E	$2.55V$	$2.55V$	0%
V_C	$12V$	$12V$	0%
V_{BC}	$-8.67V$	$-8.67V$	0%
V_{CE}	$9.45V$	$9.45V$	0%
V_{BE}	$0.78V$	$0.78V$	0%

Table 12: DC Analysis Stage 3 Error

Table 10, 11 and 12 shows the comparison of the results obtained from calculation and from simulation regarding the DC analysis of the designed amplifier circuit. The error between the calculations and the simulation are very minimal and could be assumed as no error. The slightly different occurred is because during manual calculations, many of the values were rounded off which cause some small difference between them. All the results in DC analysis were analyzed in the calculation and analysis section and all the transistors in every stage were not in the saturation nor cutoff region. They are in the forward active region where changes in the base current of the transistor can control the collector current. In this case the input signal can be fully restored with no distortion at the peak. As according to figure 29, the output signal is unclipped and perfectly amplified from the input signal.

To achieve this result, sufficient voltage has to be supplied to the base of the transistors. To ensure that the voltage is sufficient, R1, R2, R5, R6 R9 and R10 is used to control the voltage supplied into the base of the transistors using voltage divider rule. Typically, to ensure that the voltage is sufficient, the resistance of the resistor that is at the lower side must not be too low or else it will take too less of the voltage from the voltage supply which causes the voltage into the base to be too low that will lead to too low base emitter voltage and the transistor will not be turned on which is also known as the cutoff region. Besides the resistors mentioned above, the emitter

resistor which are R4, R8 and R12 also plays a role in manipulating the base emitter voltage. The resistance of the emitter resistor cannot be too high. If the emitter resistance is increased, it would cause the base current and the base emitter voltage to be too small which leads to the transistor not be able to be turned on and will stay in cutoff region. However, the base current also should not be too high or else it will destroy the transistor in real life. Hence it is all about the sweet spot for every value of the resistors to design a good amplifier circuit. This is because the emitter resistance also plays a role in controlling the AC signal gain of the circuit. Too low of the emitter resistance will cause increase in gain of the amplifier circuit. This will be further discussed in the following paragraph.

Calculation Method	Stage 1 Gain	Stage 2 Gain	Stage 3 Gain	Overall Gain (dB)
Small Signal Model	-1.62	-108.77	0.97	44.66
$Gain = \frac{R_{Load}}{R_{Emitter}}$	-0.91	-100	1 (Assumption)	39.81

Table 13: AC Analysis Gain by Stages

Calculation Method	Overall Amplifier Circuit Gain (dB)	Overall Amplifier Circuit Simulation Gain (dB)	Error, $\lvert\frac{Simulation-Calculation}{Simulation}\rvert \times 100\%$
Small Signal Model	44.66	39.87	12.01%
$Gain = \frac{R_{Load}}{R_{Emitter}}$	39.18	39.87	1.73%

Table 14: AC Analysis Overall Gain Error

Table 13 recorded all the voltage gain by each stages calculated using 2 different method and the overall voltage gain obtained using each method. By using the $Gain = \frac{R_{Load}}{R_{Emitter}}$ method, the gain in stage 3 is assumed as 1 because stage 3 is the common collector circuit where the gain voltage gain is always close to 1 because the main purpose of common collector circuit is for current gain. The formula $Gain = \frac{R_{Load}}{R_{Emitter}}$ is only applicable on common emitter circuit and also when the transistor is at forward active region.

For the AC analysis gain of the designed amplifier circuit, the main resistors that are controlling the gain of the circuit are R3, R4, R7 and R8. The concept of how it affects the gain is also similar to voltage divider rule. While doing the analysis on the AC gain, the DC component in the circuit is ignored. R3 and R5 is the collector resistor of stage 1 and stage 2 while R4 and R6 is the emitter resistor of stage 1 and stage 2. According to the formula $Gain = \frac{R_{Load}}{R_{Emitter}}$, decrease in the emitter resistance will increase the voltage gain of the particular stage and also the overall gain of the whole amplifier circuit. This comes in conflict with the condition in DC analysis where the emitter resistance shouldn't be too high as it will cause the base emitter voltage to be too small and leads to cutoff region. Hence an equilibrium has to be found to ensure that the resistance of

the emitter resistor is at optimal value where it can provide sufficient emitter base current and give desired gain. While increase in the collector resistance also known as the load resistance in common emitter circuit, will also increase the voltage gain of the stage and also for the whole gain of the circuit.

From the small signal model calculation point of view, the reason that there is a larger error compared to the simulation gain value is that there is an assumption that is made while using the small signal model method to calculate which is all capacitors are shorted. As example in stage 1, the calculation for the gain in stage 1 using small signal method includes R5 and R6 but it ignores R4. Because in small signal model all the capacitors will be shorted and shorting C3 also shorts R4. Hence from the small signal model point of view, changes in R4 should not make any changes on the gain of the amplifier circuit. However, this is not the case for this amplifier circuit design. This is because all the transistors in the design is in the forward active region. Hence R4 which is the emitter resistor will affect the base current, while if the transistor is in the forward active region, change in base current will also causes changes in the collector current. In this case, using small signal model calculation with the assumption of shorting all the capacitor may not be the best way to analyze and calculate the circuit because the R4 is shorted. The formula $Gain = \frac{R_{Load}}{R_{Emitter}}$ is a better way to calculate the gain of the common emitter amplifier circuit when it is in the forward active region because no assumptions.is made. This is the reason why the result of small signal model method has a slightly larger error. This is also the same case for stage 2. The emitter resistance R8 will also affect the base current, collector current and the voltage gain.

By having all the transistors in the forward active region and the input signal to the amplifier circuit is small enough, the output signal will be the undistorted version of the input signal which is achieved by this amplifier circuit design. In order to manipulate the gain of the whole amplifier circuit the resistance value of R3, R4, R7 and R8 can be changed. R3 and R7 is the collector resistor of stage 1 and stage 2, the resistor value is also known as the load resistance. On the other hand, R4 and R8 is the emitter resistors. To increase the gain of the amplifier circuit, resistance of R4 and R8 can be reduced and resistance of R3 and R7 can be increased. Contrastingly to reduce the gain R4 and R8 can be increased while R3 and R7 can be decreased.

Calculation Method	Formula	Lower Cutoff Frequency (Hz)	Simulation Lower Cutoff Frequency (Hz)	Error, $\lvert\frac{Simulation-Calculation}{Simulation}\rvert \times 100\%$
Normal Method	$F = \frac{1}{2\pi}[\frac{1}{Rc_1 \times C_1} + \frac{1}{Rc_2 \times C_2} \dots]$	24.46	17.71	38.11%
Transfer Function	$F = 1.1 \times \sqrt{F_1{}^2 + F_2{}^2 + F_3{}^2}$	18.54	17.71	4.69%
Highest Lower Cutoff Frequency	Max (F_{lower1}, F_{lower2}, F_{lower3})	14.46	17.71	18.35%

Table 15: Lower Cutoff Frequency Error

Table 15 records the results of calculating lower cutoff frequency using different methods. While doing research on the calculation on multistage cutoff frequency, there is also a way to make assumption on the lower cutoff frequency where only the highest lower cutoff frequency among the stages is assumed as the overall lower cutoff frequency of the while amplifier circuit. However, the reason of using the transfer function method has a lesser error is because the simulation is done using ltspice and ltspice also uses transfer function to run the simulation.

$$Lower\ Cutoff\ Frequency = \frac{1}{2\pi}[\frac{1}{Rc \times C}]$$

According to the formula above, it is obvious that the resistance to the capacitor and the capacitance is the major parameter that is affecting the lower cutoff frequency. Hence, to manipulate the lower cutoff frequency the values of the resistors and the capacitor has to be manipulated. However, it is not too realistic to manipulate the value of the resistors if the only thing that is wanted to change is the lower cutoff frequency. This is because by changing the value of the resistors, the gain of the amplifier circuit will also be affected. Thus, the best way to

manipulate the lower cutoff frequency is to change the capacitor value. Referring to the equation above, to increase the lower cutoff frequency, the capacitance has to be decreased and vice versa for decreasing the lower cutoff frequency. The capacitors that have the major effect on the overall lower cutoff frequency of the whole amplifier circuit are C5 and C6. This is because referring to 6 they have the highest $\frac{1}{Rc \times C}$ values because the resistance to C5 and C6 is 2 of the lowest in the whole circuit.

$$Upper\ Cutoff\ Frequency = \frac{1}{2\pi}[\frac{1}{Rc_{in} \times C_{in} + Rc_{out} \times C_{out}}]$$

The equation above is the formula for upper cutoff frequency. By looking at the formula it is obvious that to Rc_{in}, Rc_{out}, C_{in} and C_{out} is the major parameters that manipulates the upper cutoff frequency. Unfortunately, unlike what is going on in the lower cutoff frequency where we can only manipulate the capacitor value to change the lower cutoff frequency. This is not the case in upper cutoff frequency, because the capacitance component in the calculations of upper cutoff frequency only includes the inner capacitor which is the capacitor inside the transistor. While calculating for lower cutoff frequency, we open circuit all the internal capacitor and only consider external capacitor.

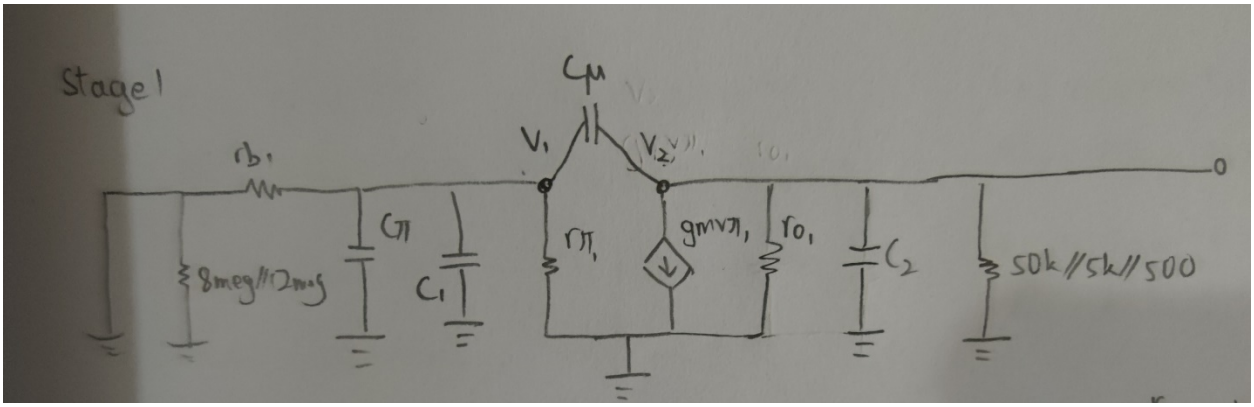

Figure 31: Upper Cutoff Frequency Calculation Example

Figure 31 shows an example AC equivalent circuit for calculations of upper cutoff frequency after applying miller's theorem. C_μ and C_π is the internal capacitance of the transistor. According to miller's theorem,

$$C_1 = C_\mu(1 - K), C_2 = C_\mu(1 - K^{-1}), K = \frac{V_1}{V_2},$$

Where V_1 is the voltage across the internal resistance, r_π and V_2 is the voltage across the internal dependent current source, $gmV\pi$. Then,

$$C_{in} = C_\pi + C_1 \text{ and } C_{out} = C_2$$

Thus, to manipulate the upper cutoff frequency, the thing that has to be manipulated is the resistance to the input capacitor and the output capacitor. For stage 1 they are R1 and R2 for input capacitor resistance and R3, R5 and R6 for output capacitor resistance. The capacitor resistance has to be reduced in order to increase the upper cutoff frequency and increased to reduce the upper cutoff frequency. However, by changing the resistance of the resistor in the circuit, it will change the characteristics of the whole circuit such as changing the operation region of the transistor and the gain will also be affected.

Lastly the power consumption of the whole amplifier circuit is 0.896W which is quite high and very close to the requirements of below 1 watt. The reason of having such high-power consumption is because the whole amplifier circuit consists of 3 stages and there are coupling capacitors between each of them. This causes that every stage draws new power from the voltage source V_{CC} which causes the overall power consumption to be high. To overcome this problem, the base voltage V_B has to be decreased to as low as possible which it doesn't causes distortion or clipping on the signal. This means that resistors R1, R2, R5, R6 R9 and R10 has to be adjusted to reduce the V_B, base voltage of each stage by applying voltage divider rule.

Conclusion

In a nutshell, the circuit designed in this assignment fulfill all the requirements. The lower cutoff frequency and higher cutoff frequency of the circuit designed are 17.71Hz and 1.54MHz. The overall gain of the circuit is 38.87dB and the power consumption is 0.896W. One of the main limitations while doing calculation on the circuit designed is that all the transistors are all in forward active region. Hence using small signal model with the assumption of shorting all the capacitors which leads to shorting the emitter resistor will not get the accurate gain of the designed amplifier circuit. This is because change in the emitter resistance will make change to the base current and when the transistor is in forward active region, change in base current will also affect the collector current which also affects the gain. To overcome this problem, the circuit can be designed to be in saturation region. On the other hand, some of the transistor in the circuit has the base emitter voltage that were higher than 0.7V. This is bad because in real life, a base emitter voltage that is higher than 0.7V will destroy the transistor. Hence it is important to design a circuit that has a base current that is optimal to turn on the transistor and not damage the transistor. In addition, the upper cutoff frequency of the designed circuit is also relatively low which causes the bandwidth is also small. To overcome this problem, a new circuit has to be designed because to manipulate the upper cutoff frequency, the resistor values have to be changed which will affect the operating region of the transistor and the gain. Last but not least, the main limitations of the amplifier circuit are there are a total of 3 stages which causes the power consumption to be high. The gain of this amplifier circuit provide can also be achieved using a 2 stage CE, CC amplifier. In this case, the overall power consumption will be decreased.

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