ASIA PACIFIC UNIVERSITY OF TECHNOLOGY & INNOVATION

ANALOG INTEGRATED CIRCUITS AND SYSTEMS

INDIVIDUAL ASSIGNMENT

NAME	Su Xin Hong
STUDENT ID	TP061159
INTAKE	APD4F2408CE
LECTURER	Assoc. Prof. Dr. Lai Nai Shyan
HAND OUT DATE	16th October 2024
HAND IN DATE	1st December 2024

Table of Contents

List of Figures

List of Tables

Introduction

The design of high-performance analog circuits, particularly operational amplifiers (op-amps) remain critical in the evolution of integrated circuits (ICs) as demands for compactness, efficiency and precision increase. In this assignment, a multi-stage operational amplifier is designed in open-loop configuration using the TSMC 0.18μm CMOS process to achieve specific electrical and performance criteria. The primary object objective is to develop a multi-stage CMOS amplifier capable of driving a 3pF capacitor and 30Ω resistor load in parallel, maintaining operational integrity within the constraints of a 1.8V supply voltage and a maximum DC power consumption of 8mW. Below is the list of requirements to be met for the operational amplifier design.

1. Operational amplifier circuit supply voltage : $V_{DD} = 1.8V$
2. Input signal peak voltage : $5mV$
3. Open Loop Gain : $36dB \leq A_v \leq 40dB$
4. Open Loop Bandwidth : $f_{3dB} \geq 300kHz$
5. Total DC power consumption : $P_{DC} \leq 8mW$
6. Current mirror as biasing circuit

This report records the design and analysis of the operational amplifier circuit which fulfills the requirements above. Simulation is done using LTSpice and the results are also analyzed and discussed in detail in this report. Besides, an enhancement of the circuit is provided in this report.

Topology Identification

Dual-Supply Configuration

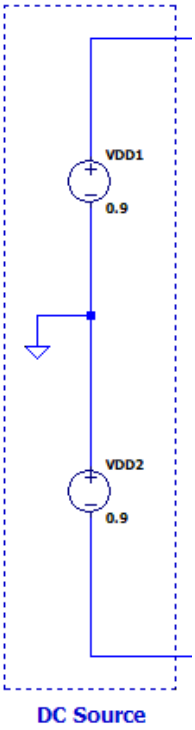

Figure 1: Dual Source Configuration Implementation

A dual-supply configuration is utilized in the multi-stage operational amplifier design as shown in Figure 1 where the V_{DD} is separated into half which are $+0.9V$ (V_{DD1}) and $-0.9V$ (V_{DD2}). A dual-supply configuration is advantageous as it enables symmetrical handling of both positive and negative signal swing around 0V ground reference. With dual sources, the differential amplifier can directly process an AC input signal by referencing the other input to ground which is the $-0.9V$, without needing additional DC offset.

Current Mirror Circuit

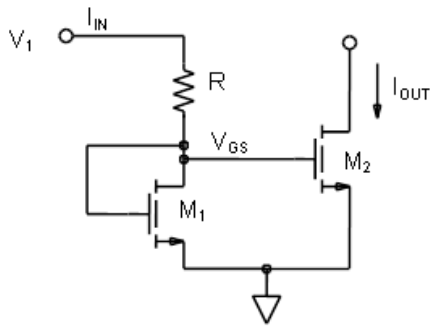

Figure 2: Basic Current Mirror Circuit (Analog Devices, 2018)

The current mirror serves as the foundational component in the multi-stage operational amplifier which provides stable and predictable current source for the differential amplifier stage and stabilizes the amplifier's operating point. This biasing mechanism utilizes matched MOS transistors to replicate a reference current, which can be precisely controlled by adjusting both a reference resistor and the width-to-length ratio, W/L of the MOS transistors involved.

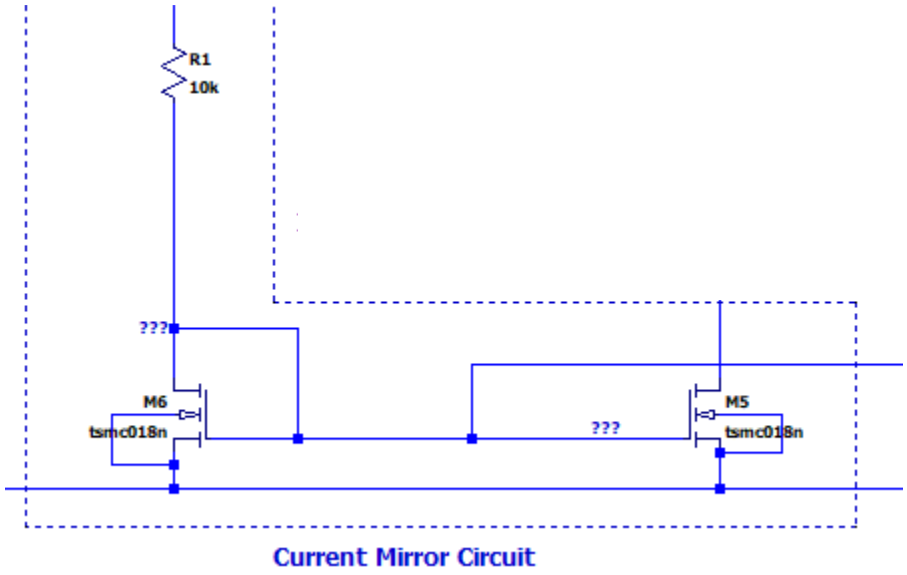

Figure 3: Current Mirror Circuit Implementation

Figure 2 shows the implementation of current mirror in the multi-stage operational amplifier design. By tuning the reference resistor, the initial current flowing through the reference branch can be modified, which in turn sets the bias current replicated in the mirror's

output branches. Adjusting widths allows for scaled current outputs where the current ratio is roughly given by the formula $I_{out} = \frac{W_{out}}{W_{ref}} \times I_{ref}$ under the assumption of the impedance seen by both the reference and output side is equal.

However, this is hard to maintain as the load at the output side will contain multiple stages where the impedance is hard to be calculated and replicated at the reference side. This mismatch leads to a deviation in the mirrored current from the intended ratio. When the resistances seen by the reference and output sides in a current mirror are different, it creates a mismatch in the drain-source voltage V_{DS} of the two transistors, causing them to operate at different region.

Differential Amplifier

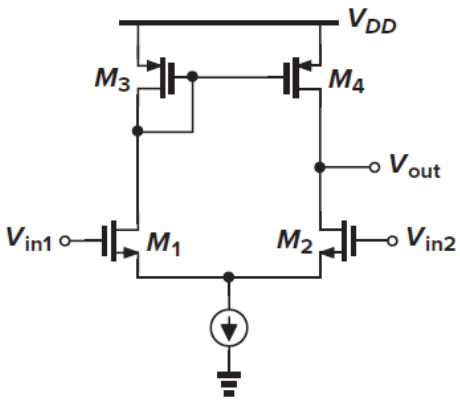

Figure 4: Differential Pair with Active Current Mirror (Razavi, 2017)

A differential amplifier is a circuit that amplifies the difference between 2 input signals while rejecting signal that is common to both inputs which is also known as common-mode signals. Differential amplifier is more superior than single ended amplifier is that differential amplifier is more immune to natural noise (Razavi, 2017). The two input into differential amplifier is one the original signal while the other is the inverted version of the first input signal. When a noisy supply voltage is provided, the noise will both occur in the inputs and will be filtered out as common-mode signal leaving only the desired signal to be amplified.

Figure 4 shows a differential amplifier with active current mirror which is also known as differential amplifier with current mirror load. M1 and M2 form the differential input pair while

M3 and M4 form a current mirror which act as high impedance load for the differential pair. The current source at the source of M1 and M2, I_{bias} is representing the bias current supplied from the current mirror circuit explained in the previous section.

When a differential voltage which is the difference between V_{in1} and V_{in2} is applied, M1 and M2 will steer more current to one side depending on the relative difference in their gate voltages. If $V_{in1} > V_{in2}$ then M1 will conduct more current than M2 which pulls more current through M3. Conversely, if $V_{in2} > V_{in1}$ then M2 will conduct more current than M1 which pulls more current through M4 while total current flowing through M1 and M2 remains constant which is set by the tail current source I_{bias}. The difference in current will create voltage differences at the drain of M1 and M2 which are the output nodes.

M3 and M4 form a current mirror with serves as the load for the differential pair. They are designed to mirror the current from one branch to the other similar to the previous current mirror circuit. The gate and drain of M3 are connected which sets the gate-source voltage of M3 such that it draws a specific current. When both M1 and M2 have the same V_{in1} and V_{in2} applied, both M1 and M2 will conduct the same current, the current mirror balances two branches in M3 and M4 meaning that the current the current through M4 will be nearly equal to the current through M3 and no differential output voltage is produced. The current mirror provides high impedance at the output nodes which results in a high voltage gain $V_{out} = I_D \cdot R_{out}$. Since R_{out} is the high resistance of the current source load, when there is a voltage difference which only cause small current differences will lead to significant voltage differences, resulting in high gain.

When V_{in1} is much more negative than V_{in2}, M1 is off, thus no current pass through, M3 and M4 are also off as there is no current from M1. All current from M5 flows through M2 but since M2 has low V_{DS}, it is in deep triode region and cannot conduct any significant current. As a result, the circuit carries 0 current and V_{out} is 0. When V_{in1} approaches V_{in2}, M1 begins to turn on and current flows through both M1 and M2. Thus, M1 and M2 are in saturation where they operate as effective current source. The current from M1 flows through M3 and is mirrored to M4. Similarly, the current through M2 determines I_{D2}. The output voltage depends on the current difference between I_{D2} and I_{D4}. Since M2 and M4 are in saturation, the circuit exhibits high gain in this region. As V_{in} becomes much more positive than V_{in2}, M1 draws a large current from M5. M1 is fully on and I_{D1} increases. M2 will receive little to no current and eventually turns off. Most of the current form M5 flows through M1 and M3 which is mirrored to M4. If I_{D4} becomes

large enough. M4 is forced into the triode region where it behaves like a resistor. As V_{in} continues to increase, M4 operates in deep triode region carrying nearly zero current and cause V_{out} approaches V_{DD}.

The differential pair with active current mirror only operates linearly only for small differential inputs. For large differential inputs, the amplifier moves out of its linear region, causing transistors to enter triodes or turn off. This limits the output swing and the overall dynamic range of the differential amplifier.

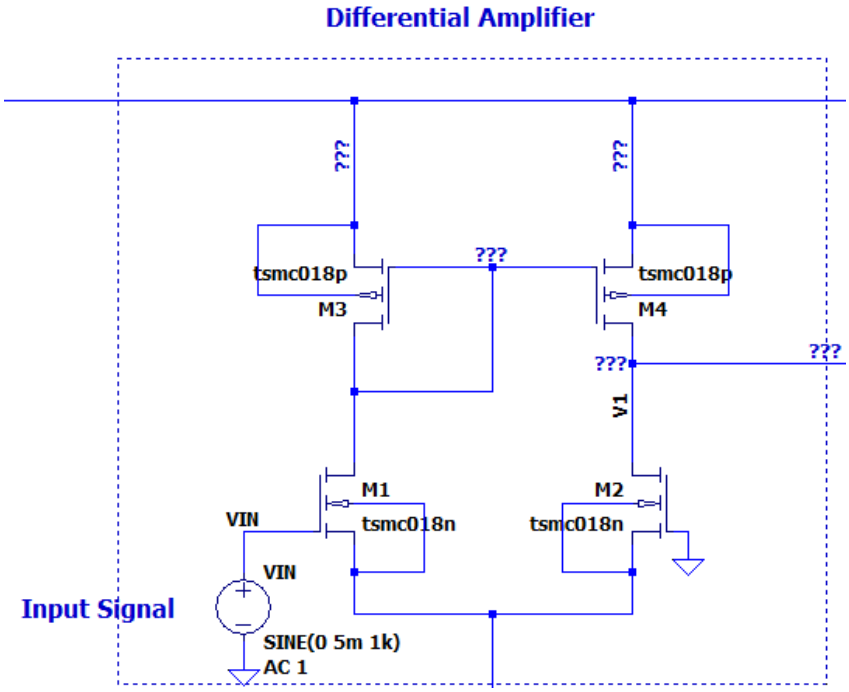

Figure 5: Differential Amplifier Implementation

Figure 5 shows the implementation of the differential amplifier with current mirror load in the design of multi-stage operational amplifier. As shown in Figure 1, the dual-supply configuration where V_{DD1} is positive $0.9V$ and V_{DD2} is negative $0.9V$ result in a virtual ground, $0V$ in the middle. In this case the ground acts as the common-mode input level for the differential amplifier. This simplifies the input design as there is no need for a separate DC offset to bring the input signal into the active range of the amplifier. In this circuit, the input signal is centered around $0V$ which naturally falls within the common-mode range of the differential amplifier. The output will be the amplified version of the input AC signal.

Common-Source Stage

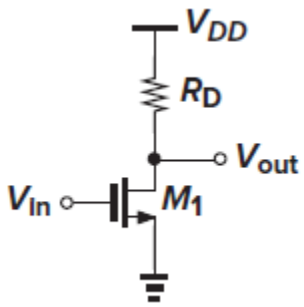

Figure 6: NMOS Common-Source Configuration (Razavi, 2017)

Figure 6 shows an example of common-source stage using NMOS to amplify input signal. Common-source stage is one of the fundamental amplifier configurations used in MOSFET. The input voltage V_{in} is applied to the gate of the NMOS which changes the gate-source voltage V_{GS} of the MOSFET. As V_{GS} changes, it controls the drain current I_D according to the MOSFET characteristics where if V_{GS} increase, I_D increases and vice versa. The current I_D flows through R_D which creates a voltage drop $V_{out} = V_{DD} - I_D R_D$. This results in an inverted output voltage. The voltage gain of a common-source amplifier is given by $A = -g_m \cdot R_D$ where g_m is the transconductance and R_D is the effective load resistance seen at the drain of the MOSFET.

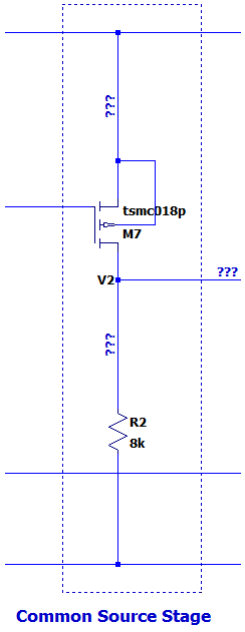

Figure 7: PMOS Common-Source Stage Implementation

Figure 7 shows the implementation of common-source stage using PMOS in the operational amplifier circuit design. In a PMOS transistor, current flows from the source to the drain which is opposite to NMOS. When a negative gate-source voltage V_{SG} where the gate is lower than the source is applied, the PMOS transistor will turn on and conduct current. The reason of choosing PMOS to create the common-source stage is to make the output swing closer to V_{DD} to allow for more headroom to the downside in the next stage as common-drain stage tends to downshift the whole signal swing at a lower voltage.

Common-Drain Stage

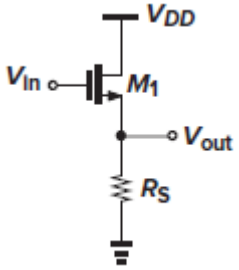

Figure 8: NMOS Common-Drain Configuration (Razavi, 2017)

Figure 8 shows a common-drain configuration using NMOS. Common-drain stage is also known as a source follower. In a common-drain configuration, the drain is connected to a fixed voltage (V_{DD} for NMOS, ground for PMOS), the input signal is applied to the gate and the output is taken from the source. The input voltage V_{in} applied to the gate modulates the gate-source voltage V_{GS} which control the current flowing through the transistor. For the NMOS to turn on, V_{GS} must be greater than the threshold voltage V_{th}. This means that the transistor must satisfy $V_{GS} = V_{in} - V_{out} \geq V_{th}$. Initially when V_{in} is applied, V_{out} is low, thus V_{GS} is large. Large V_{GS} allows current to flow through the transistor which pulls the source voltage V_{out} up. As V_{out} rises, V_{GS} reduces according to the formula $V_{GS} - V_{in} - V_{out}$. The source voltage V_{out} will keep rising until $V_{GS} \approx V_{th}$ which barely meets the threshold condition to turn on. At this point, the output will be $V_{out} \approx V_{in} - V_{th}$. Hence, V_{out} is taken form the source which follows the input voltage with a small offset which is the V_{th} of the transistor and with unity gain. This behavior of common-drain configuration is the main reason why PMOS was chosen in the previous common-source stage to prevent cutoff.

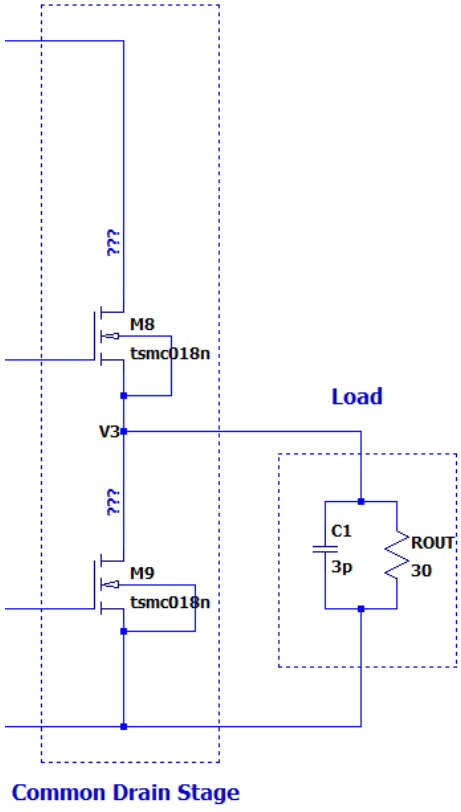

Figure 9: NMOS Common-Drain Stage Implementation

Figure 9 shows the implementation of NMOS common-drain configuration as a buffer circuit in the operational amplifier circuit to drive the load of $3pF$ capacitor parallel with 30Ω resistor. Common-drain configuration is commonly used as buffer circuit due to its unique characteristics of high input impedance, low output impedance and unity gain. High input impedance and lower output impedance are essential characteristics in an operational amplifier. High input impedance ensures that the amplifier draws very little current from the signal source which preserves the strength of the input signal and prevents signal loss. Low output impedance allows the amplifier to deliver maximum voltage to the load which is more vital when driving low load to prevent low output voltage. In Figure 9, NMOS transistor M9 is used as load instead of a resistor. M9 is biased with a fixed voltage to control the amount of current that M9 conducts. Unlike a resistor, the MOSFET can provide a high load impedance while occupying less chip area, which is beneficial in integrated circuit (IC) design.

Final Complete Circuit Design

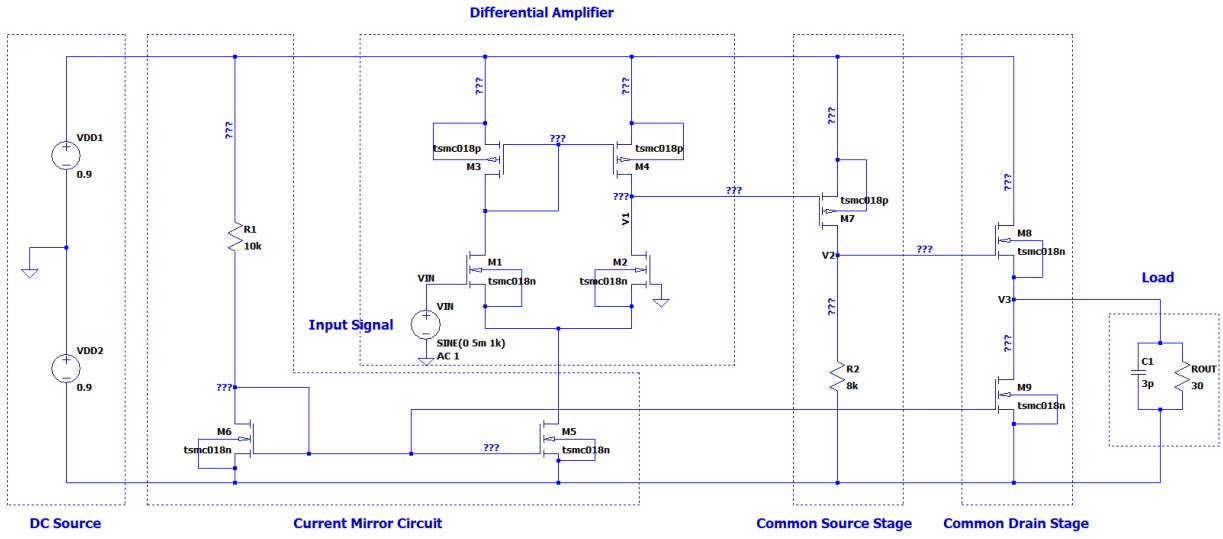

Figure 10: Final Operational Amplifier Circuit Design

Figure 10 shows the complete circuit of the operational amplifier design where it consists of a total of 3 stages which include the differential amplifier stage, common-source stage and the common-drain stage. The differential amplifier is biased with a current mirror circuit. The whole circuit is powered with the dual-supply configuration.

Table 1: Final Operational Amplifier Circuit Design Transistor List

Transistor	Function	Length	Width
M1	Differential Amplifier (Differential Pair)	0.18μ	3μ
M2	Differential Amplifier (Differential Pair)	0.18μ	3μ
M3	Differential Amplifier (Current Mirror Load)	0.18μ	50μ
M4	Differential Amplifier (Current Mirror Load)	0.18μ	50μ
M5	Current Mirror (Biasing)	0.18μ	1800μ
M6	Current Mirror (Reference)	0.18μ	18μ
M7	Common-Source Amplifier Stage	0.18μ	18μ
M8	Common-Drain Buffer Circuit (Active Transistor)	0.18μ	1800μ
M9	Common-Drain Buffer Circuit (MOS Load)	0.18μ	18μ

Table 1 shows the list of transistors and their corresponding function, width and length in the operation al amplifier circuit design.

Analytic Calculations

Power Consumption

As according to the power consumption requirement of the operational amplifier where the total power consumption of the circuit without load must be lower than $8mV$.

$$P = V \times I$$
$$8mA = 1.8V \times I$$
$$I = 4.44mA$$

According to the calculations above, the maximum current without load must not exceed $4.44mA$ to fulfil the power requirement.

Gain

According to the requirement, the gain of the operational amplifier circuit should be within 36 to $40dB$.

Minimum:

$$20\log A = 36dB$$
$$A = 63.09$$

$$V_{out} = V_{in} \times A$$
$$= 5mV \times 63.09$$
$$= 0.315V$$

Maximum:

$$20\log A = 40dB$$
$$A = 100$$

$$V_{out} = V_{in} \times A$$
$$= 5mV \times 100$$
$$= 0.5V$$

According to the calculations above, the output voltage peak should be from $0.315V$ to $0.5V$.

DC Analysis

Current Mirror Circuit

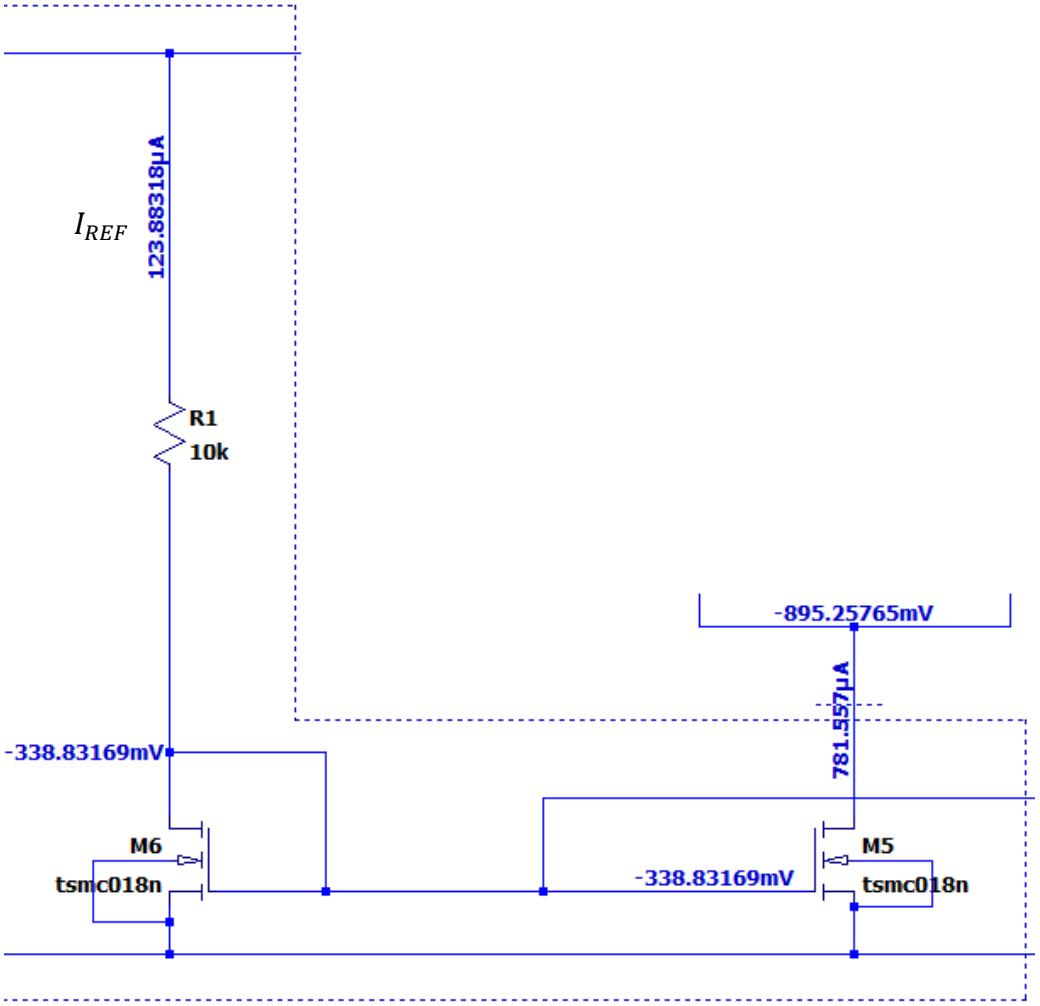

Figure 11: Current Mirror Circuit Analytic Calculation DC Analysis

$$V_{GS} \geq V_{th}$$

$$V_{DS} \geq V_{GS} - V_{th}$$

Figure 11 shows the DC analysis of the current mirror circuit and equations above shows the condition of a MOSFET transistor to be in saturation region. For a 180nm process the threshold voltage of an NMOS would be the range of $0.3 - 0.5V$. The current through $R1$ is set by the voltage difference between V_{DD1} and the voltage at the gate M6 is $-338.8mV$ according to the simulation. Where the reference current I_{REF} can be calculated using the formula below.

$$I_{REF} = \frac{V_{R1}}{R_1}$$
$$= \frac{0.9V - (-338{,}8mV)}{10k\Omega}$$
$$= 123.88\mu A$$

The I_{REF} calculation matched with the simulated result. While the gate-source voltage of M6 can also be calculated using the formula below.

$$V_{GS_{M6}} = V_{G_{M6}} - V_{S_{M6}}$$
$$= -338.8mV - (-0.9V)$$
$$= 561.2mV$$

The V_{GS} of $561.2mV$ is sufficient to keep M6 in saturation. In an identical current mirror, the output current and the reference current should be the same. However, in this design, the output current is much higher at $781.6mA$. This is due to the different width-to-length ratio W/L where both of them have the same length of 0.18μ but $W_{M6} = 0.18\mu$ while $W_{M5} = 1800\mu$. The current of a MOSFET is proportional to its W/L ratio which can be represented using the equation below.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2$$

μ_n is the electron mobility in the channel which represents how easily electrons can move through the semiconductor field when an electric field is applied. C_{ox} is the oxide capacitance per unit area of the MOSFET gate. The combination of $\mu_n C_{ox}$ can also be represented by k', it is a key parameter that determines how effective the gate voltage can control the current flowing through the channel which is a process-dependent constant. In an ideal case with different MOS length, the input output of a current mirror can be calculated using their width length.

$$I_{M5} = I_{M6} \times \frac{W_{M5}}{W_{M6}}$$
$$= 123.83\mu \times \frac{1800}{18}$$
$$= 12383\mu A$$

Ideally, the current at M5 should be $1238300\mu A$ according to the calculation above, however this is not the case shown in Figure 11 which is only $781.56\mu A$. This is due to the operating region of M5 which is in triode region, which is cause by low drain-source voltage of M5 $V_{DS_{M5}}$.

$$V_{DS_{M5}} = V_{D_{M5}} - V_{S_{M5}}$$
$$= -895.26mV - (-900mV)$$
$$= 4.74mV$$

This cause M5 to not be able to achieve $V_{DS} \geq V_{GS} - V_{th}$ which cause it to stay at triode region.

$$V_{GS_{M5}} = V_{G_{M5}} - V_{S_{M5}}$$
$$= -338.83mV - (-900mV)$$
$$= 561.17mV$$

Assuming $V_{th_{M5}} = 500mV$

$$V_{DS_{M5}} \geq V_{GS_{M5}} - V_{th_{M5}}$$
$$4.74mV < 561.17mV - 500mV$$

This make M5 behave more like a resistor and the current through it becomes dependent on $V_{DS_{M5}}$. This is not an ideal design for a current mirror, but it can effectively reduce the power consumption of the circuit by limiting the current. Besides, it also increases the allowable output voltage swing at the differential amplifier that it drives as the output operating point can be lowered by only requiring low V_{DS}.

Differential Amplifier Circuit

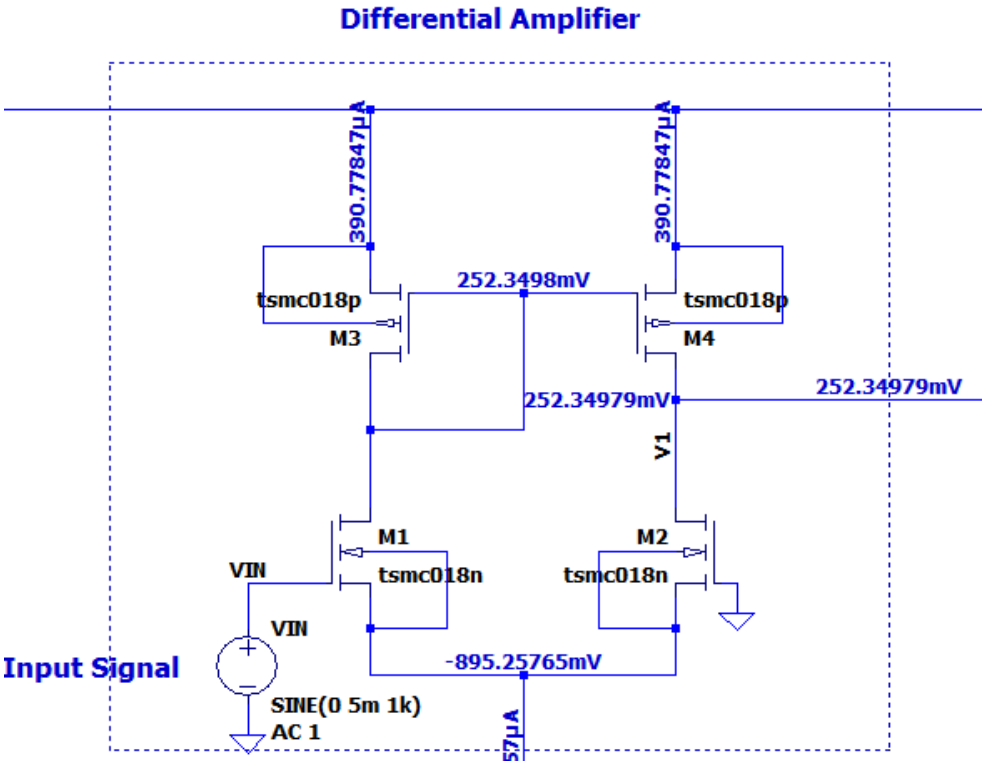

Figure 12: Differential Amplifier Analytic Calculation DC Analysis

Figure 12 shows the differential amplifier stage in the operational amplifier circuit design. The current being pulled in the circuit is controlled by the current mirror explained in the previous section which is $781.56\mu A$. The current is equally divided into 2 and is pulled into each side of the differential amplifier.

$$I_{S_{M3}} = I_{S_{M4}} = \frac{I_{D_{M5}}}{2}$$
$$= \frac{781.56\mu A}{2}$$
$$= 390.75\mu A$$

This proves the transistors in the differential amplifier are identical on both sides. M1 and M2 are the differential pair of the differential amplifier. M3 is a diode-connected load where its gate and drain are connected together, it is used to generate bias voltage for the gate of M4. M4 is an active PMOS load operating in the saturation region and acting as a current source with high

output impedance. Together M3 and M4 form a current mirror which is the current mirror load in the differential amplifier.

To perform DC analysis, the input V_{in} is assumed to be 0 as it only contains the AC input signal to be amplified. While V_{th} is assumed to be $500mV$ in NMOS and $-500mV$ in PMOS.

M1:

Gate-source voltage:

$$\begin{aligned} V_{GS_{M1}} &= V_{G_{M1}} - V_{S_{M1}} \\ &= V_{in} - (-895.26mV) \\ &= 895.26mV \end{aligned}$$

Drain-source voltage:

$$\begin{aligned} V_{DS_{M1}} &= V_{D_{M1}} - V_{S_{M1}} \\ &= 252.35mV - (-895.26mV) \\ &= 1147.61mV \end{aligned}$$

Saturation condition:

$$V_{DS_{M1}} \geq V_{GS_{M1}} - V_{th}$$
$$1147.61mV \geq 895.26mV - 500mV$$
$$1147.61mV \geq 395.26mV$$

M2:

Gate-source voltage:

$$\begin{aligned} V_{GS_{M2}} &= V_{G_{M2}} - V_{S_{M2}} \\ &= 0 - (-895.26mV) \\ &= 895.26mV \end{aligned}$$

Drain-source voltage:

$$\begin{aligned} V_{DS_{M2}} &= V_{D_{M2}} - V_{S_{M2}} \\ &= 252.35mV - (-895.26mV) \\ &= 1147.61mV \end{aligned}$$

Saturation condition:

$$V_{DS_{M2}} \geq V_{GS_{M2}} - V_{th}$$
$$1147.61mV \geq 895.26mV - 500mV$$
$$1147.61mV \geq 395.26mV$$

M3:

Source-gate voltage:

$$\begin{aligned} V_{SG_{M3}} &= V_{S_{M3}} - V_{G_{M3}} \\ &= 0.9V - 252.35mV \\ &= 647.65mV \end{aligned}$$

Source-drain voltage:

$$\begin{aligned} V_{SD_{M3}} &= V_{S_{M3}} - V_{D_{M3}} \\ &= 0.9V - 252.35mV \\ &= 647.65mV \end{aligned}$$

Saturation condition:

$$V_{SD_{M3}} \geq V_{SG_{M3}} - |V_{th}|$$
$$647.65mV \geq 647.65mV - 500mV$$
$$647.65mV \geq 147.65mV$$

M4:

Source-gate voltage:

$$\begin{aligned} V_{SG_{M4}} &= V_{S_{M4}} - V_{G_{M4}} \\ &= 0.9V - 252.35mV \\ &= 647.65mV \end{aligned}$$

Source-drain voltage:

$$\begin{aligned} V_{SD_{M4}} &= V_{S_{M4}} - V_{D_{M4}} \\ &= 0.9V - 252.35mV \\ &= 647.65mV \end{aligned}$$

Saturation condition:

$$V_{SD_{M4}} \geq V_{SG_{M4}} - |V_{th}|$$
$$647.65mV \geq 647.65mV - 500mV$$
$$647.65mV \geq 147.65mV$$

According to the calculations above transistors M1, M2, M3 and M4 are all in saturation region. For the differential pair M1 and M2 it is vital to be in saturation region to ensure linear amplification by making I_D dependent of V_{DS}. While saturation region in M3 and M4 provides high output impedance for high gain and enables proper current mirroring.

Common-Source Stage

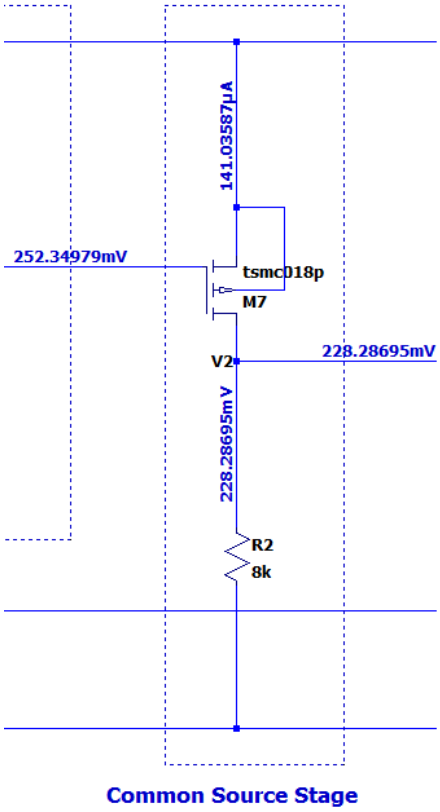

Figure 13: Common-Source Stage Analytic Calculation DC Analysis

Figure 13 shows the common-source stage of the operational amplifier circuit used to further amplify the output from the differential amplifier. To perform DC analysis, the V_{th} of M7 is assumed to be $500mV$.

Source-gate voltage:

$$V_{SG_{M7}} = V_{S_{M7}} - V_{G_{M7}}$$
$$= 0.9v - 252.35mV$$
$$= 647.65mV$$

Source-drain voltage:

$$V_{SD_{M7}} = V_{S_{M7}} - V_{D_{M7}}$$
$$= 0.9v - 228.29mV$$
$$= 671.71mV$$

Saturation condition:

$$V_{SD_{M7}} \geq V_{SG_{M7}} - |V_{th}|$$
$$671.71mV \geq 647.65mV - 500mV$$
$$671.71mV \geq 147.65mV$$

According to the calculations above, M7 is also operating in a saturation region. This is vital to ensure the common-source stage provides a linear amplification of the input signal.

Common-Drain Stage

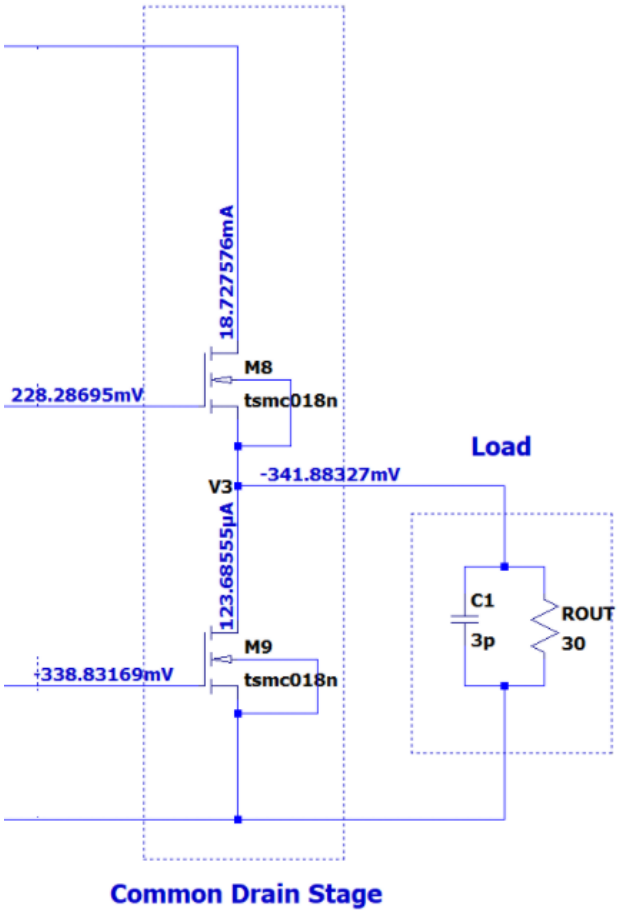

Figure 14: Common-Drain Stage Analytic Calculation DC Analysis

Figure 14 shows the common-drain stage of the operational amplifier circuit using an NMOS transistor where M8 is the active transistor and M9 is the MOS load. It is used to drive the load of $30pF$ and 30Ω. To perform DC analysis, the V_{th} of M8 and M9 is assumed to be $500mV$

M8:

Gate-source voltage:

$$V_{GS_{M8}} = V_{G_{M8}} - V_{S_{M8}}$$
$$= 228.29mv - (-341.88mV)$$
$$= 570.17mV$$

Drain-source voltage:

$$V_{DS_{M8}} = V_{D_{M8}} - V_{S_{M8}}$$
$$= 900mV - (-341.88mV)$$
$$= 1241.88mV$$

Saturation condition:

$$V_{DS_{M7}} \geq V_{GS_{M7}} - V_{th}$$
$$1241.88mV \geq 570.17mV - 500mV$$
$$1241.88mV \geq 70.17mV$$

M9:

Gate-source voltage:

$$V_{GS_{M9}} = V_{G_{M9}} - V_{S_{M9}}$$
$$= -338.83mV - (-900mV)$$
$$= 651.17mV$$

Drain-source voltage:

$$V_{DS_{M9}} = V_{D_{M9}} - V_{S_{M9}}$$
$$= -341.88mV - (-900mV)$$
$$= 558.12mV$$

Saturation condition:

$$V_{DS_{M7}} \geq V_{GS_{M7}} - V_{th}$$
$$558.12mV \geq 651.17mV - 500mV$$
$$558.12mV \geq 151.17mV$$

According to the calculations above, M8 and M9 are operating in saturation region. M8 operates as the active source follower, buffering the input signal and providing low input impedance to drive the load, operating in saturation ensures linear voltage transfer. While M9 is a passive MOS load which operates in saturation to provide high resistance.

DC Analysis Summary

Table 2: DC Analysis Transistor Summary Table

Transistor	Function	Length	Width	Operating Region
M1	Differential Amplifier (Differential Pair)	0.18μ	3μ	Saturation
M2	Differential Amplifier (Differential Pair)	0.18μ	3μ	Saturation
M3	Differential Amplifier (Current Mirror Load)	0.18μ	50μ	Saturation
M4	Differential Amplifier (Current Mirror Load)	0.18μ	50μ	Saturation
M5	Current Mirror	0.18μ	1800μ	Triode

	(Biasing)			
M6	Current Mirror (Reference)	0.18μ	18μ	Saturation
M7	Common-Source Amplifier Stage	0.18μ	18μ	Saturation
M8	Common-Drain Buffer Circuit (Active Transistor)	0.18μ	1800μ	Saturation
M9	Common-Drain Buffer Circuit (MOS Load)	0.18μ	18μ	Saturation

Final Circuit Power Consumption Without Load

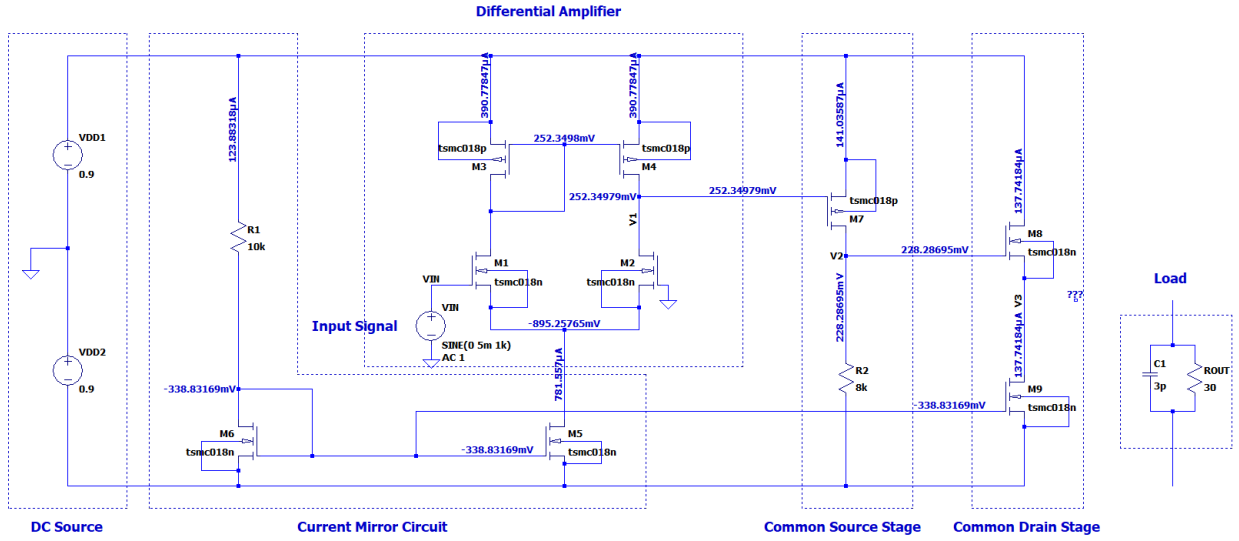

Figure 15: Operational Amplifier Circuit Design Without Load

Figure 15 shows the operational amplifier circuit without load. The total current drawn can be calculated using the formula below.

$$I_{total} = I_{R1} + I_{D_{M3}} + I_{D_{M4}} + I_{S_{M7}} + I_{D_{M8}}$$
$$= 123.88\mu A + 390.78\mu A + 390.78\mu A + 141.04\mu A + 137.74\mu A$$
$$= 1.18422mA$$

The total current drawn from the source is only $1.18422mA$ without load which is lower than the maximum current calculated in the previous section, $4.44mA$.

$$P = VI$$
$$= 1.8V \times 1.18422mA$$
$$= 2.1316mW$$

The power consumption is only $2.1316mW$ which is lower than the requirement of $8mW$.

AC Analysis

Differential Amplifier Circuit

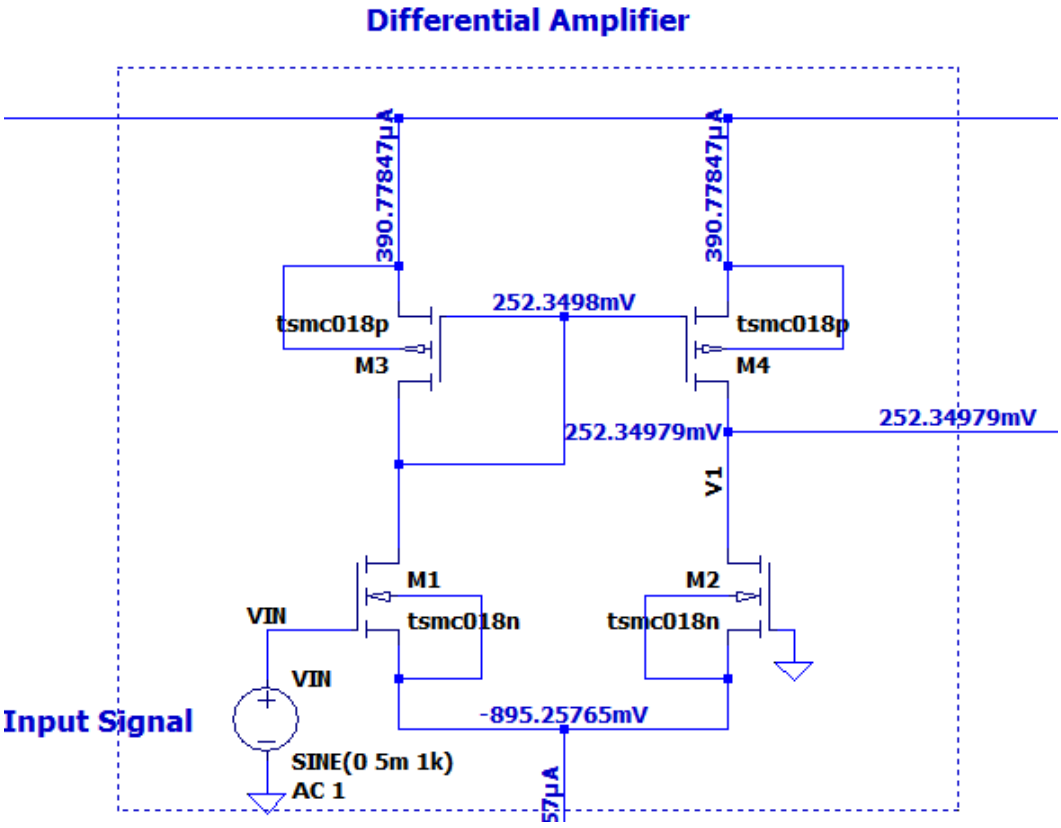

Figure 16: Differential Amplifier Analytic Calculation AC Analysis

The gain of a differential amplifier is given by the equation below.

$$A = g_{m1,2} \cdot R_{out}$$

g_m is the transconductance of the NMOS differential pair M1 and M2 while R_{out} is the effective resistance at output node which is determined by the PMOS M3 and M4. From the equation above it is evident that a gain of a differential amplifier is highly dependent on both g_m and

R_{out}. While g_m is directly proportional to the width-to-length ratio of the transistor $\left(\frac{W}{L}\right)$ which can be given by the formula below.

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

According to the simulation, g_m of M1, M2, M3 and M4 are given as below.

$$g_{m1} = g_{m2} = 1.31mS$$

$$g_{m3} = g_{m4} = 4.27mS$$

The output resistance of the differential circuit can be estimated by the formula below provided transistors are identical at both sides (Razavi, 2017).

$$R_{out} = r_{o1,2} || r_{o3,4}$$

While r_o can be calculated using the formula below.

$$r_o = \frac{1}{\lambda \cdot I_D}$$

Where λ is the channel-length modulation parameter. It is a measure of how the effective length of the MOSFET's channel changes with variations in the drain-source voltage which can be calculated assuming $\lambda_{typical} = 0.02V^{-1}$ for $L = 1\mu m$. For $L = 0.18\mu m$, λ can be calculated using the formula below.

$$\lambda = \frac{1}{L} \cdot \lambda_{typical}$$
$$= \frac{0.02}{0.18}$$
$$= 0.111V^{-1}$$

Thus, λ is assumed to be $0.111V^{-1}$

$$r_{o2} = \frac{1}{\lambda \cdot I_{D2}}$$
$$= \frac{1}{0.111V^{-1} \cdot 390.78\mu A}$$
$$= 23.05k\Omega$$

$$r_{o4} = \frac{1}{\lambda \cdot I_{D4}}$$
$$= \frac{1}{0.111V^{-1} \cdot 390.78\mu A}$$
$$= 23.05k\Omega$$

$$R_{out} = \frac{r_{o2} \cdot r_{o4}}{r_{o2} + r_{o4}}$$
$$= \frac{23.05 \cdot 23.05}{23.05 + 23.05} k\Omega$$
$$= 11.53k\Omega$$

$$A = 1.31mS \cdot 11.53k\Omega$$
$$= 15.11$$
$$= 23.59dB$$

According to the estimation calculations above, the gain of the differential amplifier should be approximate $23.59dB$.

Common-Source Stage

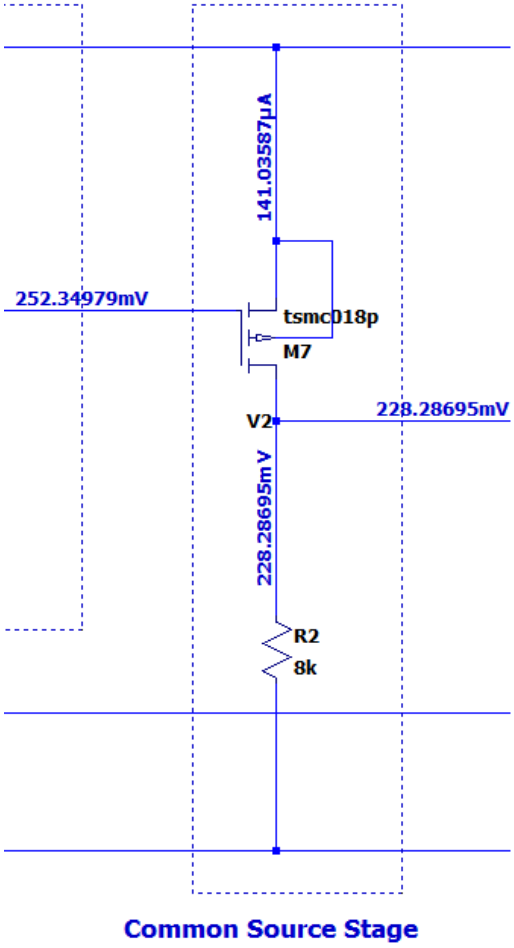

Figure 17: Common-Source Stage Analytic Calculation AC Analysis

Figure 17 shows the common-source stage and the gain of common-source stage is given by the formula below.

$$A = -g_m \cdot R_{out}$$

According to the simulation, $g_{m7} = 1.54mS$.

$$A = -1.54mS \cdot 8k\Omega$$
$$= -12.32$$
$$= 21.81dB$$

The gain of the common-source stage is approximately $21.81dB$ and the negative sign indicate that the output is 180° out of phase.

Common Drain Stage

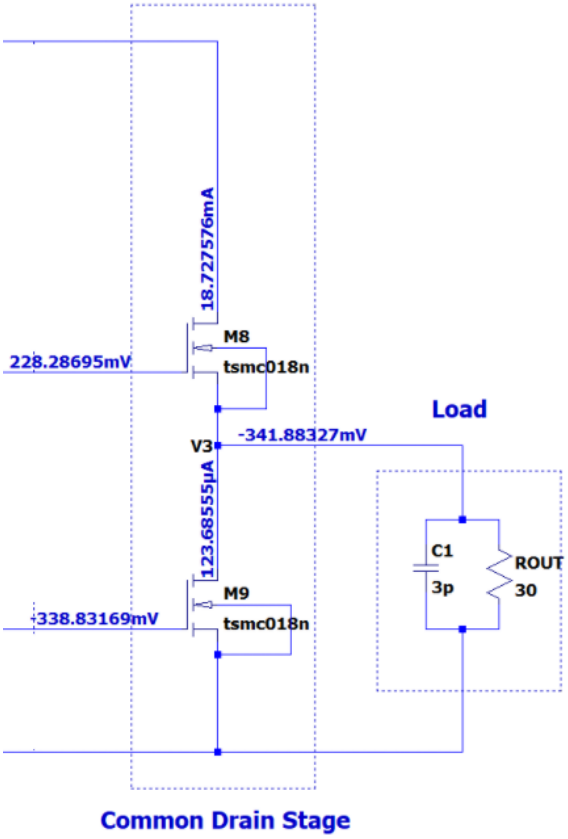

Figure 18: Common-Drain Stage Analytic Calculation AC Analysis

Figure 18 shows the common-drain stage and the voltage gain is given by the formula below.

$$A = \frac{R_L}{R_L + \frac{1}{g_m}}$$

Since that, the load resistor is very low which is 30Ω and is with parallel with the M9 MOS load which is a very high impedance. R_L can be assumed to be 30Ω. According to the simulation $g_{m8} = 0.296S$.

$$A = \frac{30\Omega}{30\Omega + \frac{1}{0.296S}}$$
$$= 0.899$$

The gain is close to 1, which is as intended where the main purpose of a common-drain stage is only to provide low output impedance, not high gain.

Operational Amplifier Circuit Total Gain

$$A_{final} = A_{stage1} \times A_{stage2} \times A_{stage3}$$
$$= 15.11 \times -12.32 - 0.899$$
$$= 167.35$$
$$= 44.47dB$$

The total gain of the operational amplifier is estimated to be $44.47dB$ through approximation calculations, which is close to the requirement of $40dB$.

SPICE Simulation Results

DC Analysis

Operating Point

Name:	m1	m2	m5	m6	m8	m9	m3	m4	m7
Model:	tsmc018n	tsmc018n	tsmc018n	tsmc018n	tsmc018n	tsmc018n	tsmc018p	tsmc018p	tsmc018p
Id:	3.91e-04	3.91e-04	7.82e-04	1.24e-04	1.87e-02	1.24e-04	-3.91e-04	-3.91e-04	-1.41e-04
Vgs:	8.95e-01	8.95e-01	5.61e-01	5.61e-01	5.70e-01	5.61e-01	-6.48e-01	-6.48e-01	-6.48e-01
Vds:	1.15e+00	1.15e+00	4.74e-03	5.61e-01	1.24e+00	5.58e-01	-6.48e-01	-6.48e-01	-6.72e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	4.85e-01	4.85e-01	5.05e-01	4.99e-01	4.97e-01	4.99e-01	-4.85e-01	-4.85e-01	-4.84e-01
Vdsat:	1.87e-01	1.87e-01	6.88e-02	7.10e-02	7.56e-02	7.10e-02	-1.48e-01	-1.48e-01	-1.48e-01
Gm:	1.31e-03	1.31e-03	1.07e-02	2.17e-03	2.96e-01	2.17e-03	4.27e-03	4.27e-03	1.54e-03
Gds:	5.21e-05	5.21e-05	1.59e-01	6.47e-05	7.01e-03	6.48e-05	6.54e-05	6.54e-05	2.29e-05
Gmb	3.11e-04	3.11e-04	2.66e-03	5.24e-04	7.06e-02	5.24e-04	1.27e-03	1.27e-03	4.59e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	2.57e-15	2.57e-15	1.54e-12	1.54e-14	1.54e-12	1.54e-14	3.91e-14	3.91e-14	1.41e-14
Cgdov:	2.57e-15	2.57e-15	1.54e-12	1.54e-14	1.54e-12	1.54e-14	3.91e-14	3.91e-14	1.41e-14
Cgbov:	1.46e-19	1.46e-19	1.46e-19	1.46e-19	1.46e-19	1.46e-19	1.21e-19	1.21e-19	1.21e-19
dQgdVgb:	8.30e-15	8.30e-15	5.00e-12	4.78e-14	4.83e-12	4.78e-14	1.22e-13	1.22e-13	4.38e-14
dQgdVdb:	-2.55e-15	-2.55e-15	-2.10e-12	-1.54e-14	-1.54e-12	-1.54e-14	-3.91e-14	-3.91e-14	-1.41e-14
dQgdVsb:	-5.51e-15	-5.51e-15	-2.73e-12	-3.02e-14	-3.08e-12	-3.02e-14	-8.03e-14	-8.03e-14	-2.89e-14
dQddVgb:	-3.79e-15	-3.79e-15	-2.43e-12	-2.17e-14	-2.19e-12	-2.17e-14	-5.59e-14	-5.59e-14	-2.01e-14
dQddVdb:	2.56e-15	2.56e-15	2.19e-12	1.54e-14	1.54e-12	1.54e-14	3.91e-14	3.91e-14	1.41e-14
dQddVsb:	1.56e-15	1.56e-15	4.78e-13	7.93e-15	8.27e-13	7.93e-15	2.20e-14	2.20e-14	7.91e-15
dQbdVgb:	-7.15e-16	-7.15e-16	-1.30e-13	-4.49e-15	-4.45e-13	-4.49e-15	-9.93e-15	-9.93e-15	-3.59e-15
dQbdVdb:	8.11e-19	8.11e-19	-7.41e-13	3.52e-18	5.99e-16	3.47e-18	-8.72e-18	-8.72e-18	-2.66e-18
dQbdVsb:	-1.82e-16	-1.82e-16	2.25e-13	-1.11e-15	-1.15e-13	-1.11e-15	-2.70e-15	-2.70e-15	-9.59e-16

Figure 19: SPICE Simulation Result – DC Operating Point

Figure 19 shows the output of SPICE simulation of DC operating point. The main purpose of this simulation is to observe the operating region of the transistors. To validate if a transistor is turned on, V_{GS} must be larger than V_{th}. All the transistors fulfill the requirement and are turned on. While if the transistor is turned on but $V_{DS} < V_{DSat}$, the transistor is in triode region which is the condition of M5. While if $V_{DS} \geq V_{DSat}$, the transistor is in saturation region which is the condition of the rest of the transistors. This result is same to what is calculated in the analytic calculation section summarized in Table 2.

```
I(Vdd1):        -0.00118422     device_current
I(Vdd2):        -0.00118422     device_current
I(Vin):         0               device_current
```

Figure 20: SPICE Simulation Result – Current Drawn Without Load

Figure 20 shows the current drawn from V_{DD1} and V_{DD2} without load are $1.18mA$. The power consumption can be computed by multiplying it with the total DC source with total

supply voltage $1.8V$, which comes to $2.124mW$. This is similar to the result calculated in DC analysis and also proves that the operational amplifier circuit is within the requirement of $8mW$.

DC Sweep

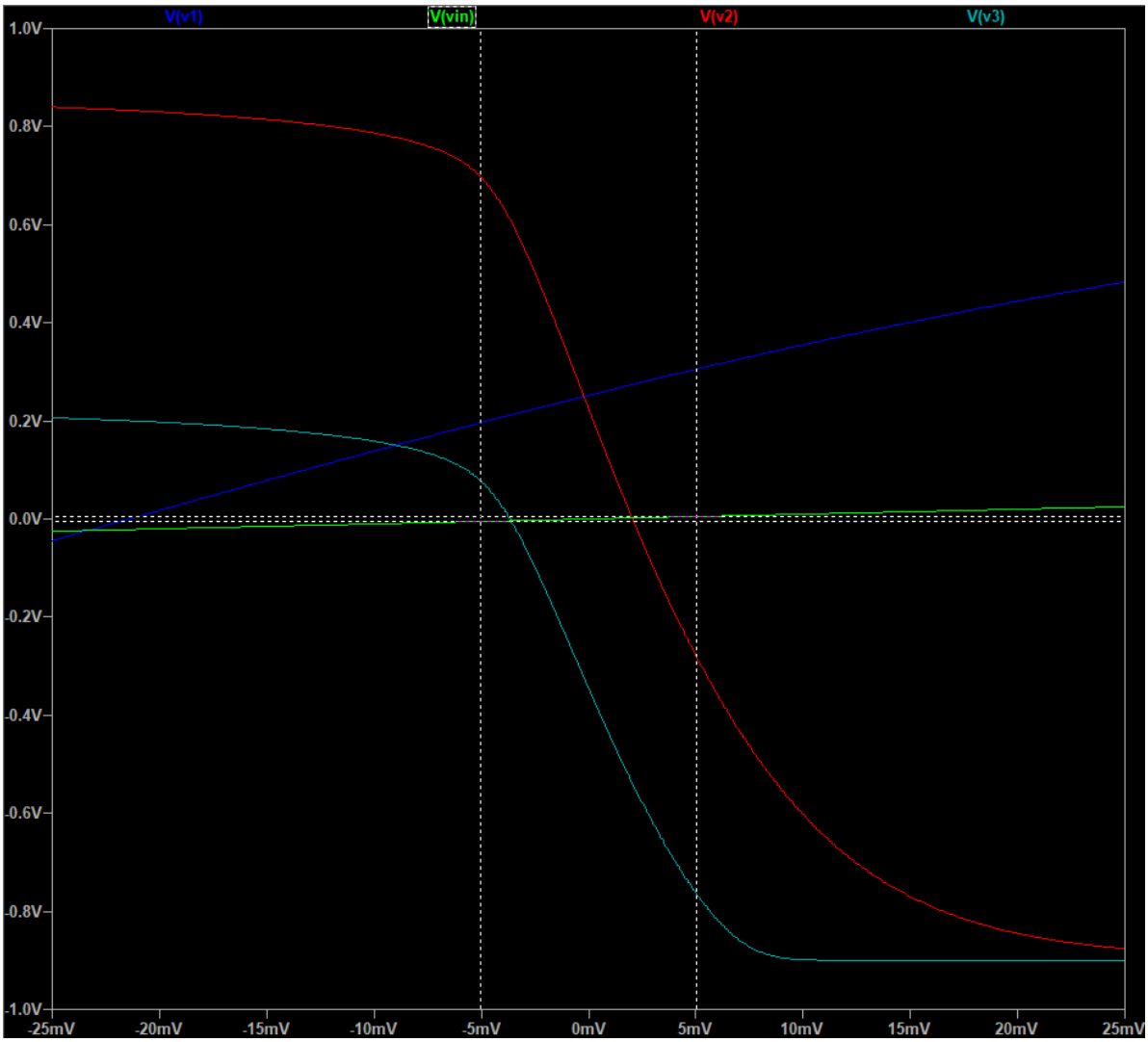

Figure 21: SPICE Simulation Result – DC Sweep

Figure 21 shows the SPICE simulation output of DC sweep where V_{in} is swept from $-0.1V$ to $0.1V$ and zoomed to $\pm 25mV$. The reason of doing it is because the DC input had been separated into $-0.9V$ to $+0.9V$ while the input AC signal has the amplitude of $5mV$ which means that the AC will swing from $-0.005V$ to $+0.005V$. Thus, $\pm\ 0.1V$ is enough to see what is going on in the output. In Figure 21. There are 2 cursors being placed at $-5mV$ and $+5mV$ which is the area where the input signal will swing. The region between these 2 cursors indicates

the outputs of each stage when the AC input is applied and swinging. The green line is the swept input, V_{in}. The dark blue line , V_1 is the output of the differential amplifier. The red line, V_2 is the output of the common-source stage. The light blue line, V_3 is the output of the common-drain stage which is also the final output of the operational amplifier circuit.

As shown in the result, in the range of $\pm 5mV$ input, the corresponding output of each stage are linear which means that, the gain is quite uniform in that area. This means that in the particular input range, all the transistors are operating in saturation region which provides linearity. When the input of $\pm 5mV$ is provided, the whole signal can be amplified equally with almost the same gain at every point of the signal without going into triode or cutoff region. This ensures no distortion or clipping in the output signal which will be reflected in the transient response. This proves that this operational amplifier circuit design can handle AC signal input of $5mV$ amplitude as per requirement.

Transient Response

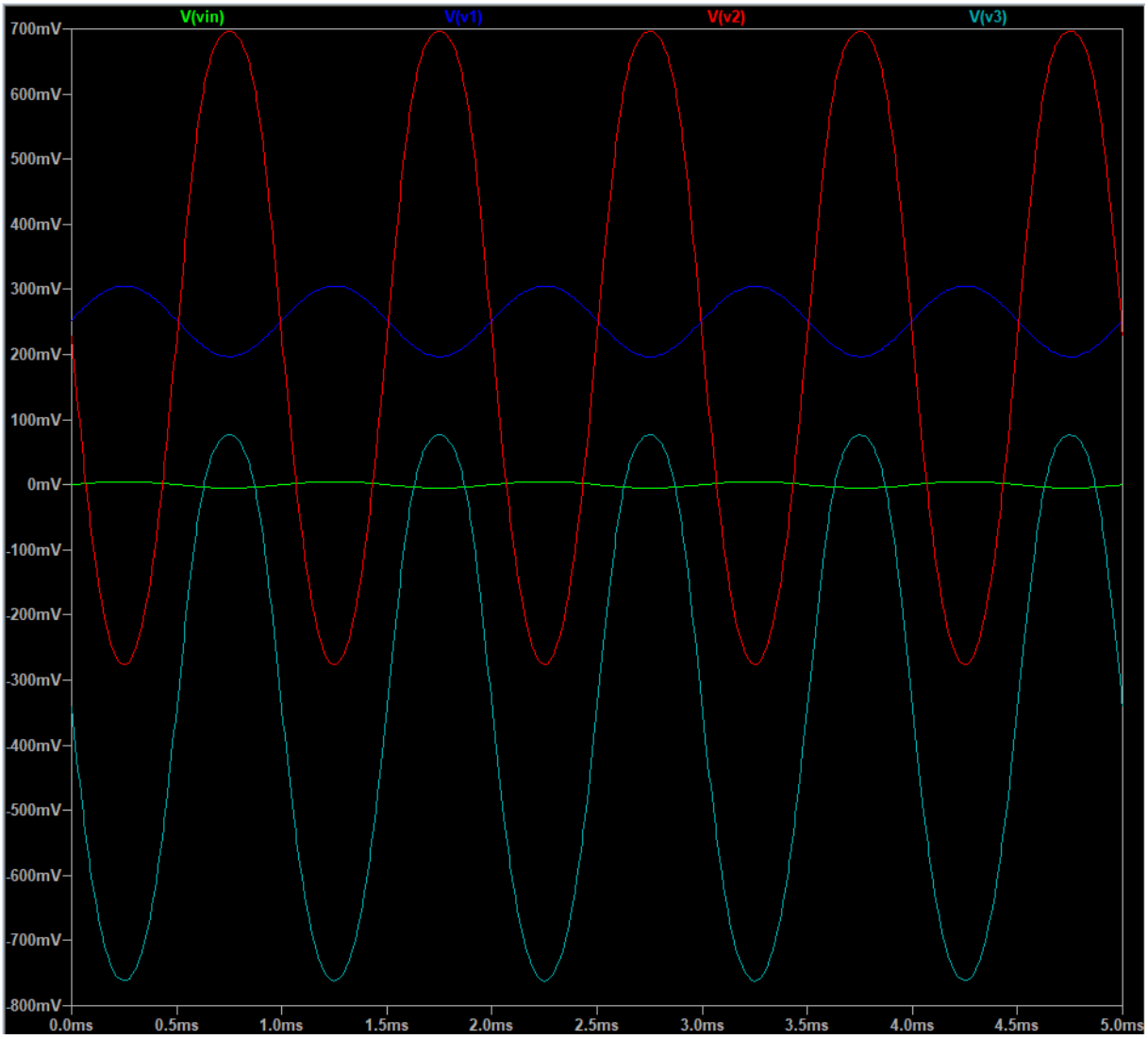

Figure 22: SPICE Simulation Result – Transient Response (All)

Figure 22 shows the transient response of each stage. As mentioned in the DC sweep simulation result, the operational amplifier circuit can handle $5mV$ amplitude AC input where the whole signal can be amplified equally. As shown in the transient response, all the signals are passed down stage by stage nicely without significant or visible clipping and cutoff.

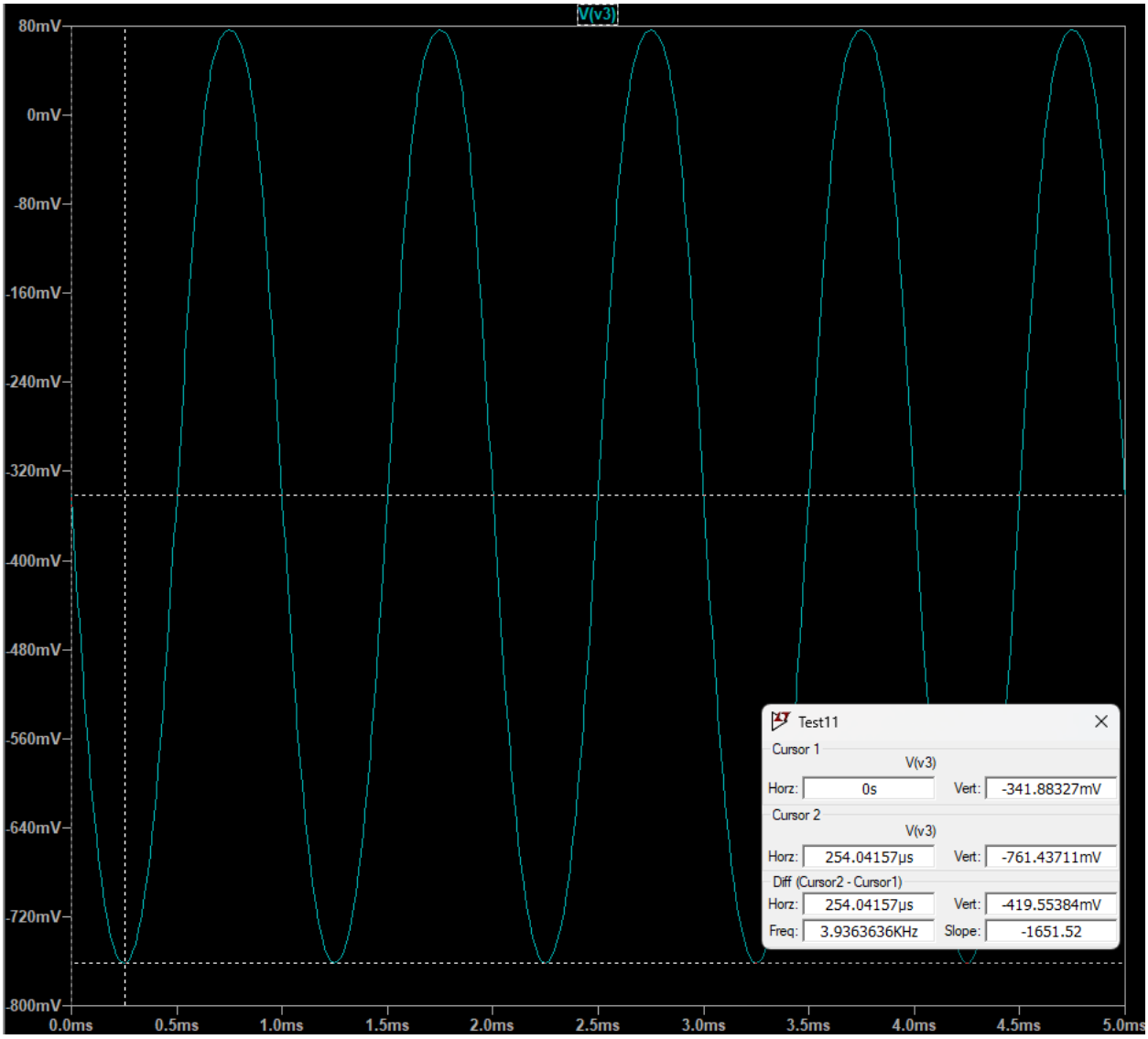

Figure 23: SPICE Simulation Result – Transient Response (V3 Lower Difference)

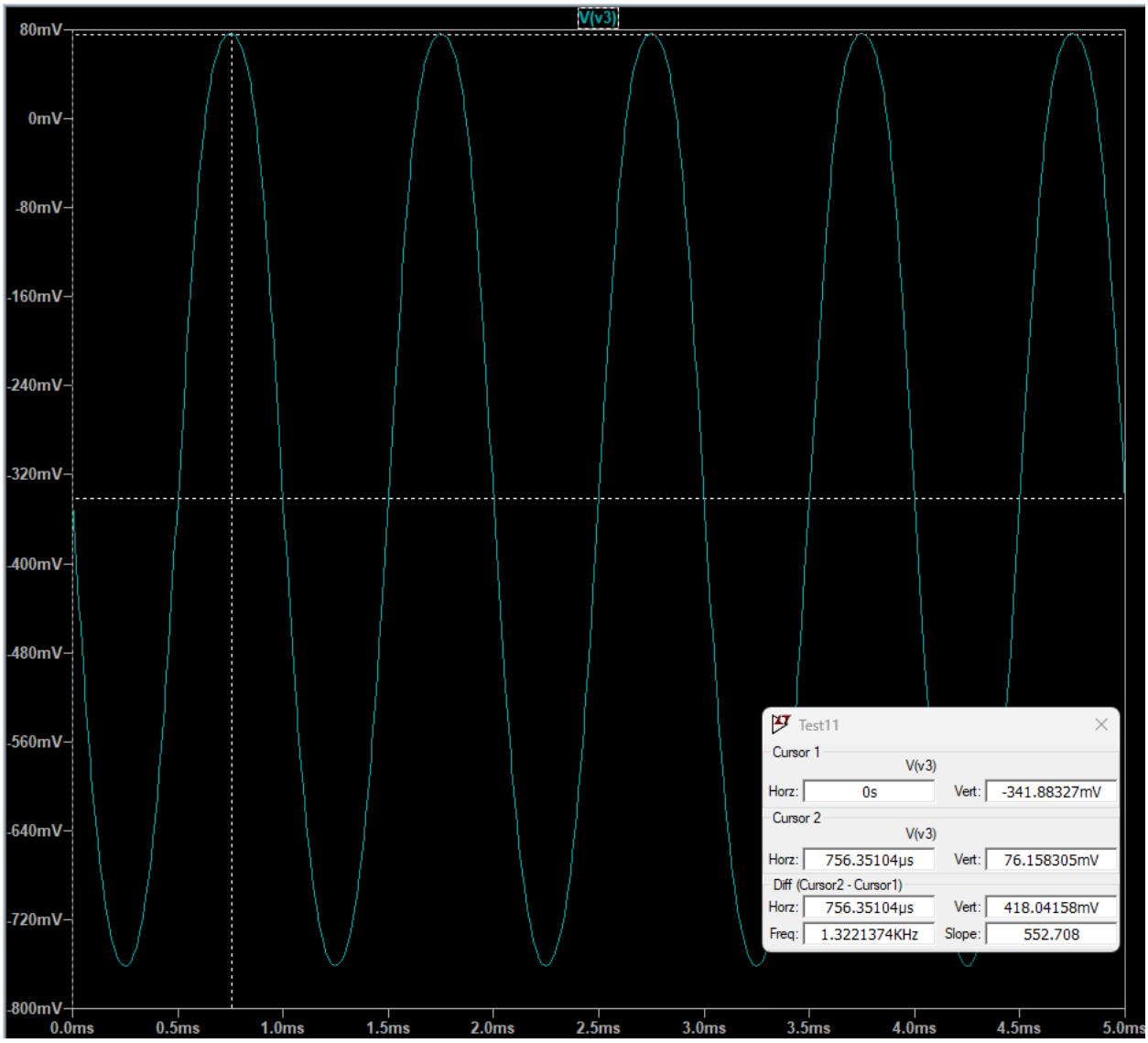

Figure 24: SPICE Simulation Result – Transient Response (V3 Upper Difference)

Figure 23 and Figure 24 shows a more detailed transient response output of the operational amplifier circuit V_3. The output signal is operating at $-341.88mV$ and the lowest point is at $-761.44mV$ while the highest point is at $76.16mV$. This brings the signal to a peak-to-peak of $837.6mV$. The lower cycle peak is $-341.88mV - (-761.44mV) = 419.56mV$. The upper cycle peak is $76.16mV - (-341.88mV) = 418.04mV$. This shows the upper and lower cycle are almost identical where they only have the difference of $1.52mV$. This proves that the whole signal is amplified almost equally at every point.

AC Analysis

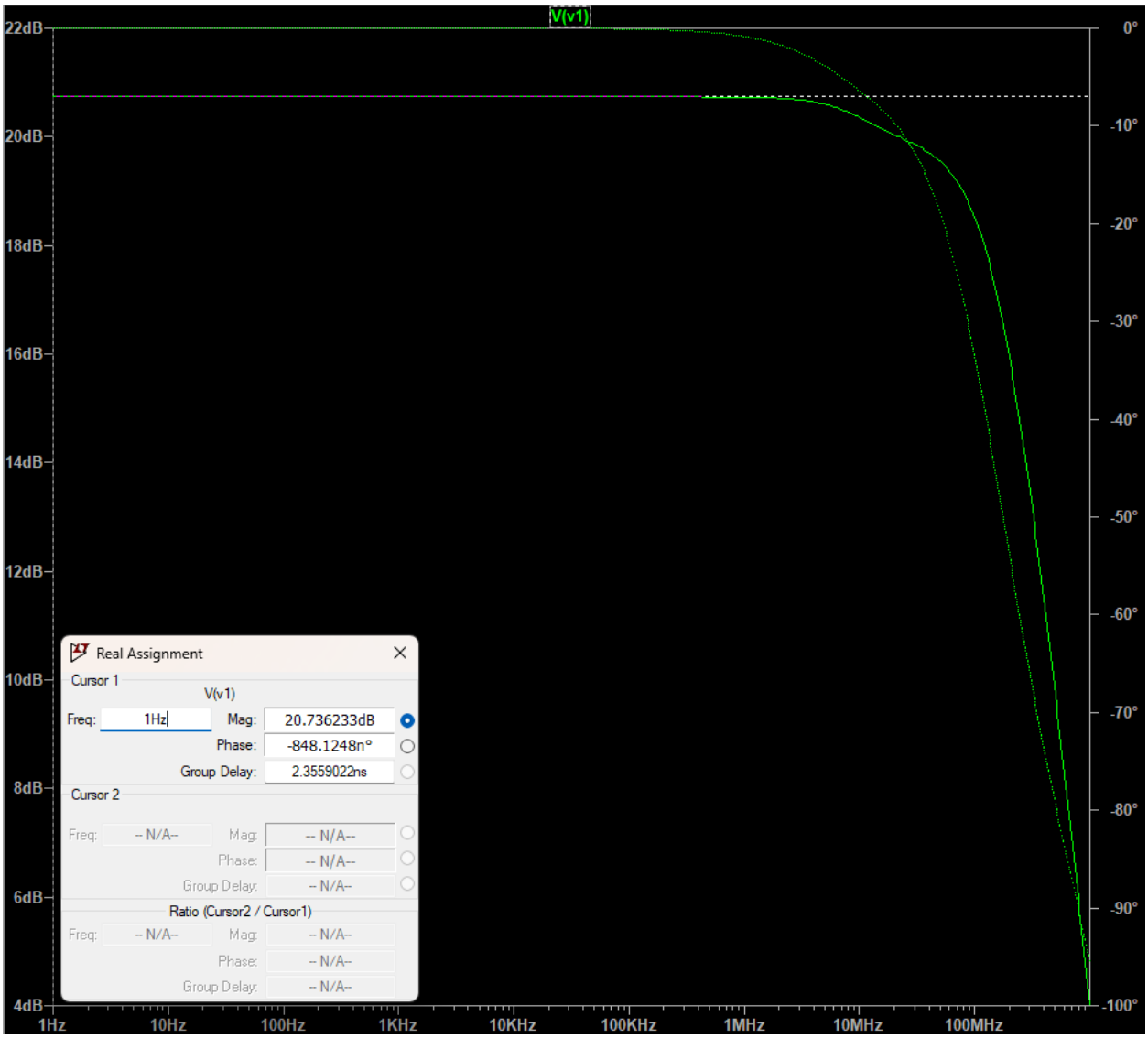

Figure 25: SPICE Simulation Result – AC Analysis (Differential Amplifier Output)

Figure 25 shows the AC analysis of the differential amplifier circuit. The gain of the differential amplifier circuit is $20.74dB$, which is close to the calculation at analytic calculation section of $23.59dB$.

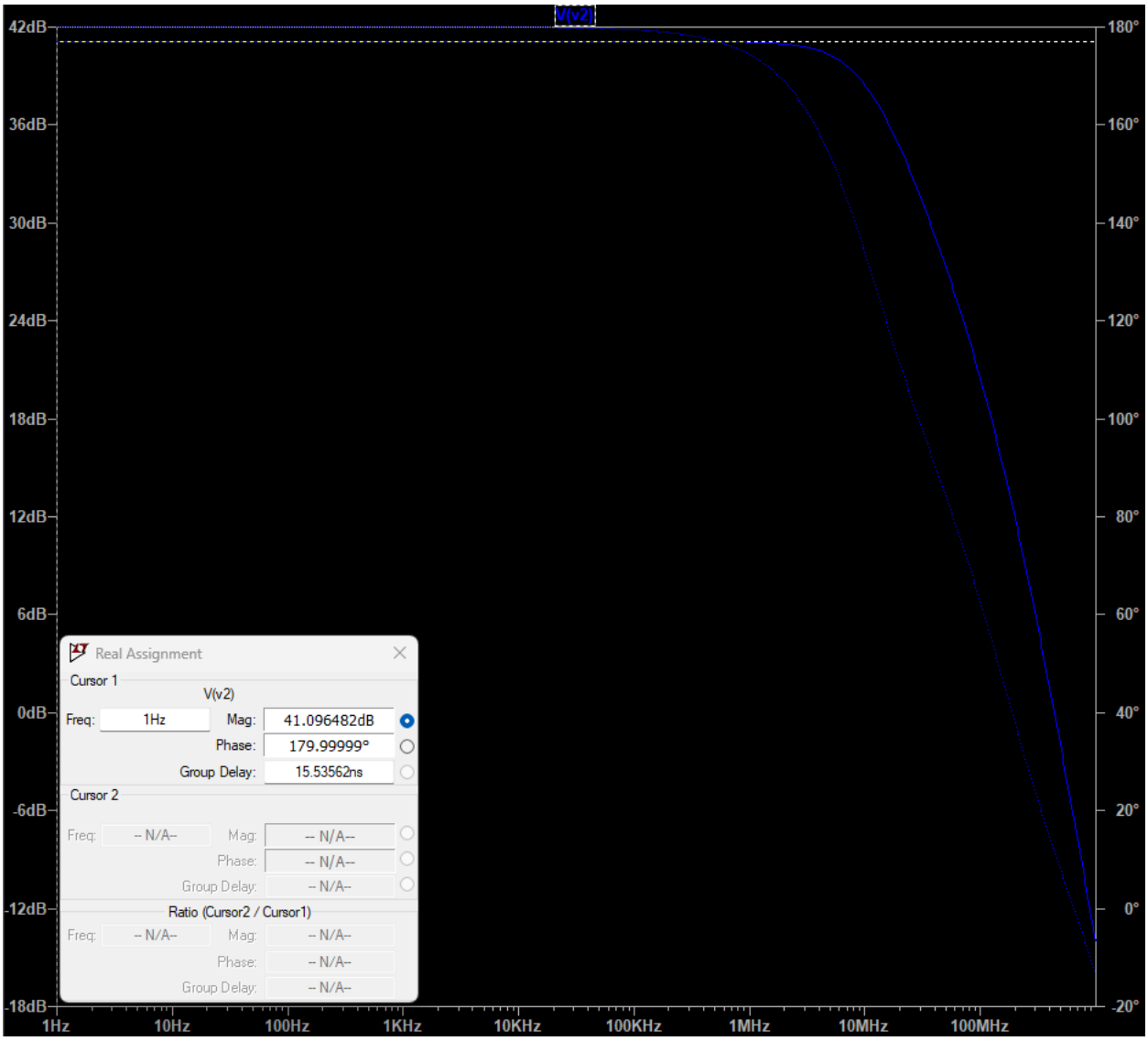

Figure 26: SPICE Simulation Result – AC Analysis (Common-Source Stage Output)

Figure 26 shows the AC analysis of the common-source stage. The gain of the signal after going through the common-source stage is $41.1dB$ which is slightly higher than the requirement, it is intended because the common-drain stage will slightly reduce the signal.

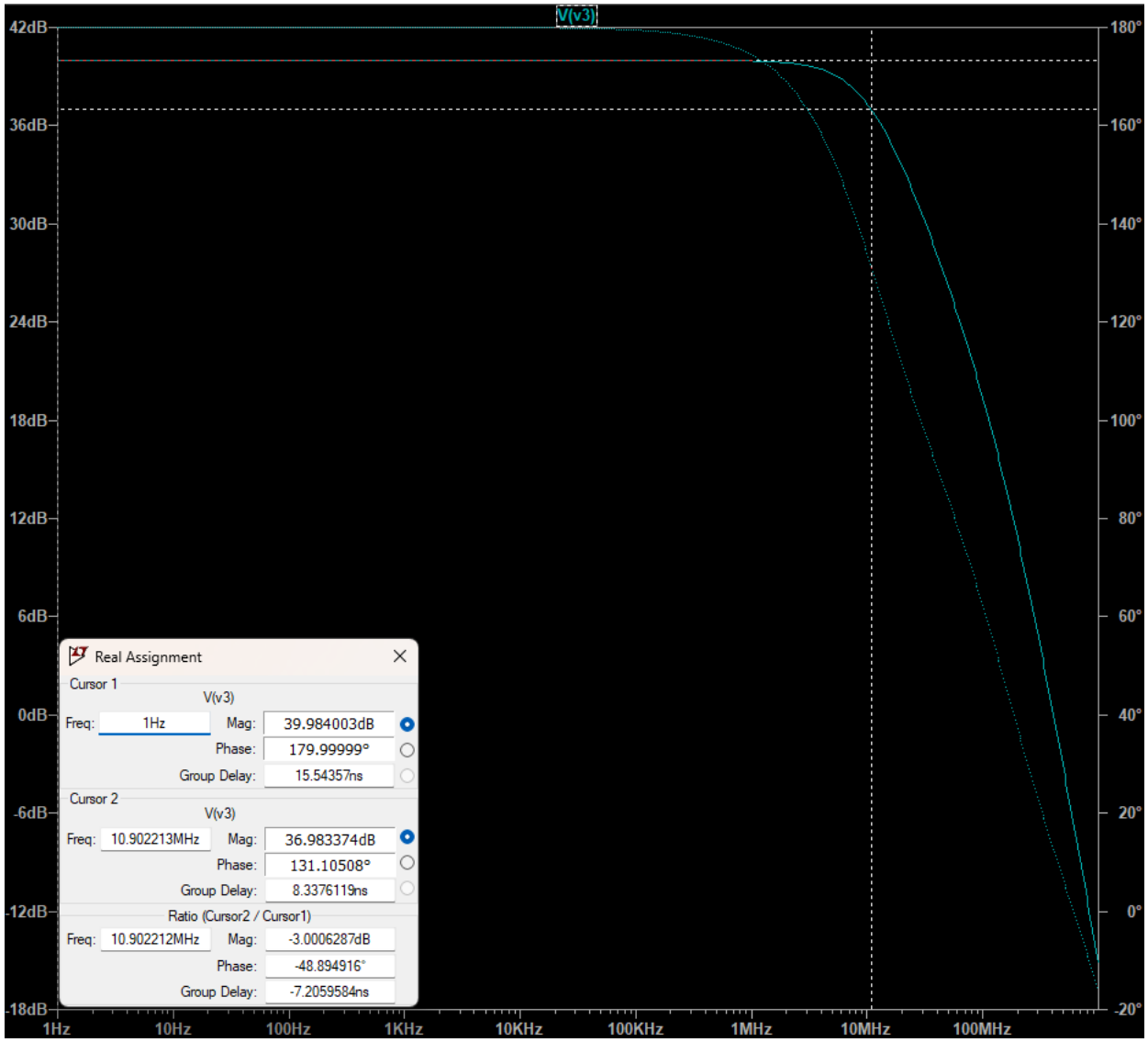

Figure 27: SPICE Simulation Result – AC Analysis (Final Output)

Figure 27 shows the AC analysis of the operational amplifier circuit which is also the output of the common-drain stage. The final gain is $39.98dB$ which fulfills the requirement. Besides the bandwidth of the circuit is also $10.9MHz$ which easily fulfills the requirement of $300kHz$.

Enhancement of Circuit Performance

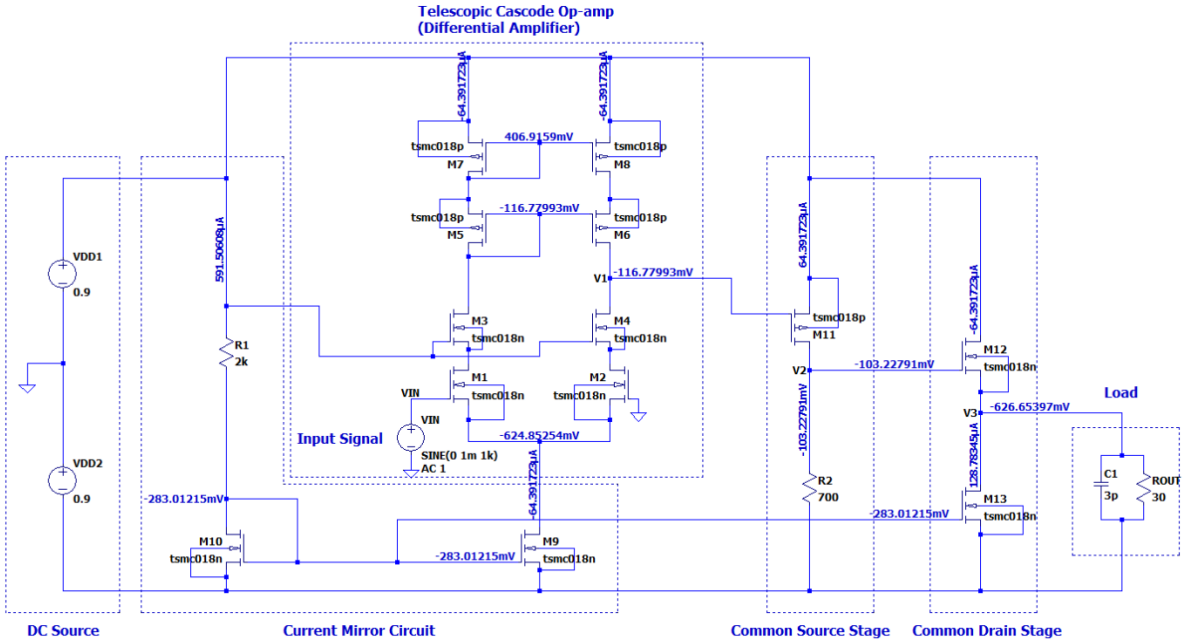

Figure 28: Circuit Enhancement – Telescopic Cascode Operational Amplifier

Figure 28 shows the enhancement implied to the operational amplifier circuit which is the application of differential cascode topology in the differential amplifier circuit which is also called as telescopic cascode operational amplifier.

A telescopic cascode op-amp uses multiple transistors arranged in a cascode configuration as shown in Figure 28. M1 and M2 are the differential input pair. M3 and M4 are the input cascode transistors to increase output resistance and increase gain. M5 and M6 are the current mirror which ensure equal current in both sides and convert the current difference into a voltage signal at the output. M7 and M8 are the output cascode transistors to further increase output resistance and enhance gain.

The cascode structure increases the output resistance significantly which contributes to higher gain. Additionally, the telescopic structure's compact design and lower power consumption compared to alternative configurations, like the folded cascode, make it a preferred choice in IC implementations (Gulati & Lee, 1998). The cascode transistors stacked on top of the input stage also isolate the input and output stages to mitigate the Miller effect. This design improves the bandwidth, allowing the amplifier to handle high-frequency signals effectively as compared to other cascode amplifier topologies.

However, there are several drawbacks such as limited output swing. The vertical stacking of transistors requires a significant portion of the supply voltage for biasing, leaving limited headroom for the output voltage swing (Gulati & Lee, 1998). Furthermore, the input common-mode range is also reduced because the tail current source and stacked transistors consume a portion of the supply voltage, restricting the range of allowable input signals. The amplitude of the input signal that the amplifier can accept to ensure uniform amplification is also limited. Thus, in this circuit the input signal is only $1mV$.

Name:	m1	m2	m9	m10	m12
Model:	tsmc018n	tsmc018n	tsmc018n	tsmc018n	tsmc018n
Id:	6.44e-05	6.44e-05	1.29e-04	5.92e-04	9.36e-03
Vgs:	6.25e-01	6.25e-01	6.17e-01	6.17e-01	5.23e-01
Vds:	5.00e-01	5.00e-01	2.75e-01	6.17e-01	1.53e+00
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	4.54e-01	4.54e-01	4.99e-01	5.00e-01	4.95e-01
Vdsat:	1.33e-01	1.33e-01	9.43e-02	9.40e-02	5.92e-02
Gm:	7.16e-04	7.16e-04	1.74e-03	7.84e-03	1.74e-01
Gds:	8.46e-06	8.46e-06	9.90e-05	2.39e-04	3.88e-03
Gmb	1.95e-04	1.95e-04	4.17e-04	1.87e-03	4.21e-02
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	7.72e-15	7.72e-15	7.72e-15	3.09e-14	1.54e-12
Cgdov:	7.72e-15	7.72e-15	7.72e-15	3.09e-14	1.54e-12
Cgbov:	5.06e-19	5.06e-19	1.46e-19	1.46e-19	1.46e-19
dQgdVgb:	4.75e-14	4.75e-14	2.47e-14	9.88e-14	4.57e-12
dQgdVdb:	-7.64e-15	-7.64e-15	-7.69e-15	-3.07e-14	-1.54e-12
dQgdVsb:	-3.77e-14	-3.77e-14	-1.61e-14	-6.44e-14	-2.74e-12
dQddVgb:	-2.04e-14	-2.04e-14	-1.13e-14	-4.50e-14	-2.05e-12
dQddVdb:	7.68e-15	7.68e-15	7.71e-15	3.08e-14	1.54e-12
dQddVsb:	1.66e-14	1.66e-14	4.52e-15	1.80e-14	6.45e-13
dQbdVgb:	-6.69e-15	-6.69e-15	-2.15e-15	-8.70e-15	-4.67e-13
dQbdVdb:	-8.18e-18	-8.18e-18	-1.94e-17	6.22e-18	4.88e-16
dQbdVsb:	-3.17e-15	-3.17e-15	-6.21e-16	-2.45e-15	-9.27e-14

Figure 29: Circuit Enhancement – DC Operating Point 1

Name:	m13	m3	m4	m7	m8	m11	m5	m6
Model:	tsmc018n	tsmc018n	tsmc018n	tsmc018p	tsmc018p	tsmc018p	tsmc018p	tsmc018p
Id:	2.51e-04	6.44e-05	6.44e-05	-6.44e-05	-6.44e-05	-1.14e-03	-6.44e-05	-6.44e-05
Vgs:	6.17e-01	1.03e+00	1.03e+00	-4.93e-01	-4.93e-01	-1.02e+00	-5.24e-01	-5.24e-01
Vds:	2.73e-01	8.41e-03	8.41e-03	-4.93e-01	-4.93e-01	-1.00e+00	-5.24e-01	-5.24e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	5.01e-01	5.01e-01	5.01e-01	-4.85e-01	-4.85e-01	-4.84e-01	-4.85e-01	-4.85e-01
Vdsat:	9.34e-02	2.10e-01	2.10e-01	-6.25e-02	-6.25e-02	-3.88e-01	-7.43e-02	-7.43e-02
Gm:	3.41e-03	1.02e-04	1.02e-04	1.33e-03	1.33e-03	3.41e-03	1.23e-03	1.23e-03
Gds:	1.94e-04	7.56e-03	7.56e-03	1.69e-05	1.69e-05	1.21e-04	1.53e-05	1.53e-05
Gmb	8.17e-04	2.82e-05	2.82e-05	3.99e-04	3.99e-04	1.08e-03	3.67e-04	3.67e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.54e-14	7.72e-15	7.72e-15	7.82e-14	7.82e-14	1.41e-14	4.22e-14	4.22e-14
Cgdov:	1.54e-14	7.72e-15	7.72e-15	7.82e-14	7.82e-14	1.41e-14	4.22e-14	4.22e-14
Cgbov:	1.46e-19	1.46e-19	1.46e-19	1.21e-19	1.21e-19	1.21e-19	1.21e-19	1.21e-19
dQgdVgb:	4.94e-14	2.65e-14	2.65e-14	2.16e-13	2.16e-13	4.40e-14	1.23e-13	1.23e-13
dQgdVdb:	-1.54e-14	-1.26e-14	-1.26e-14	-7.82e-14	-7.82e-14	-1.41e-14	-4.22e-14	-4.22e-14
dQgdVsb:	-3.22e-14	-1.34e-14	-1.34e-14	-1.25e-13	-1.25e-13	-2.93e-14	-7.53e-14	-7.53e-14
dQddVgb:	-2.26e-14	-1.32e-14	-1.32e-14	-9.71e-14	-9.71e-14	-2.02e-14	-5.57e-14	-5.57e-14
dQddVdb:	1.54e-14	1.35e-14	1.35e-14	7.82e-14	7.82e-14	1.41e-14	4.22e-14	4.22e-14
dQddVsb:	9.02e-15	1.20e-15	1.20e-15	2.48e-14	2.48e-14	8.01e-15	1.77e-14	1.77e-14
dQbdVgb:	-4.30e-15	-4.95e-17	-4.95e-17	-2.20e-14	-2.20e-14	-3.54e-15	-1.14e-14	-1.14e-14
dQbdVdb:	-3.86e-17	-6.60e-15	-6.60e-15	-4.49e-18	-4.49e-18	-4.62e-18	-3.66e-18	-3.66e-18
dQbdVsb:	-1.25e-15	3.32e-15	3.32e-15	-3.32e-15	-3.32e-15	-8.45e-16	-2.30e-15	-2.30e-15

Figure 30: Circuit Enhancement – DC Operating Point 2

Figure 29 and Figure 30 shows the DC operating points of the transistors. All the transistors are operating in saturation region except M3 and M4 which are in triode region.

I(Vdd1):	-0.00213391	device_current
I(Vdd2):	-0.00213391	device_current
I(Vin):	0	device_current

Figure 31: Circuit Enhancement – Off Load Current

Figure 31 shows the current drawn from the source when load is removed which is $2.13mA$. Hence the power consumption is only $2.13mA \times 1.8V = 3.834mW$ which is also within the requirement.

Table 3: Circuit Enhancement Transistor Summary Table

Transistor	Function	Length	Width	Operating Region
M1	Differential Amplifier (Differential Pair)	0.54μ	9μ	Saturation
M2	Differential Amplifier (Differential Pair)	0.54μ	9μ	Saturation
M3	Differential Amplifier (Cascode Transistor)	0.18μ	9μ	Triode
M4	Differential Amplifier	0.18μ	9μ	Triode

	(Cascode Transistor)			
M5	Differential Amplifier (Current Mirror Load)	0.18μ	54μ	Saturation
M6	Differential Amplifier (Current Mirror Load)	0.18μ	54μ	Saturation
M7	Differential Amplifier (Cascode Transistor)	0.18μ	100μ	Saturation
M8	Differential Amplifier (Cascode Transistor)	0.18μ	100μ	Saturation
M9	Current Mirror (Biasing)	0.18μ	9μ	Saturation
M10	Current Mirror (Reference)	0.18μ	36μ	Saturation
M11	Common-Source Amplifier Stage	0.18μ	18μ	Saturation
M12	Common-Drain Buffer Circuit (Active Transistor)	0.18μ	1800μ	Saturation
M13	Common-Drain Buffer Circuit (MOS Load)	0.18μ	18μ	Saturation

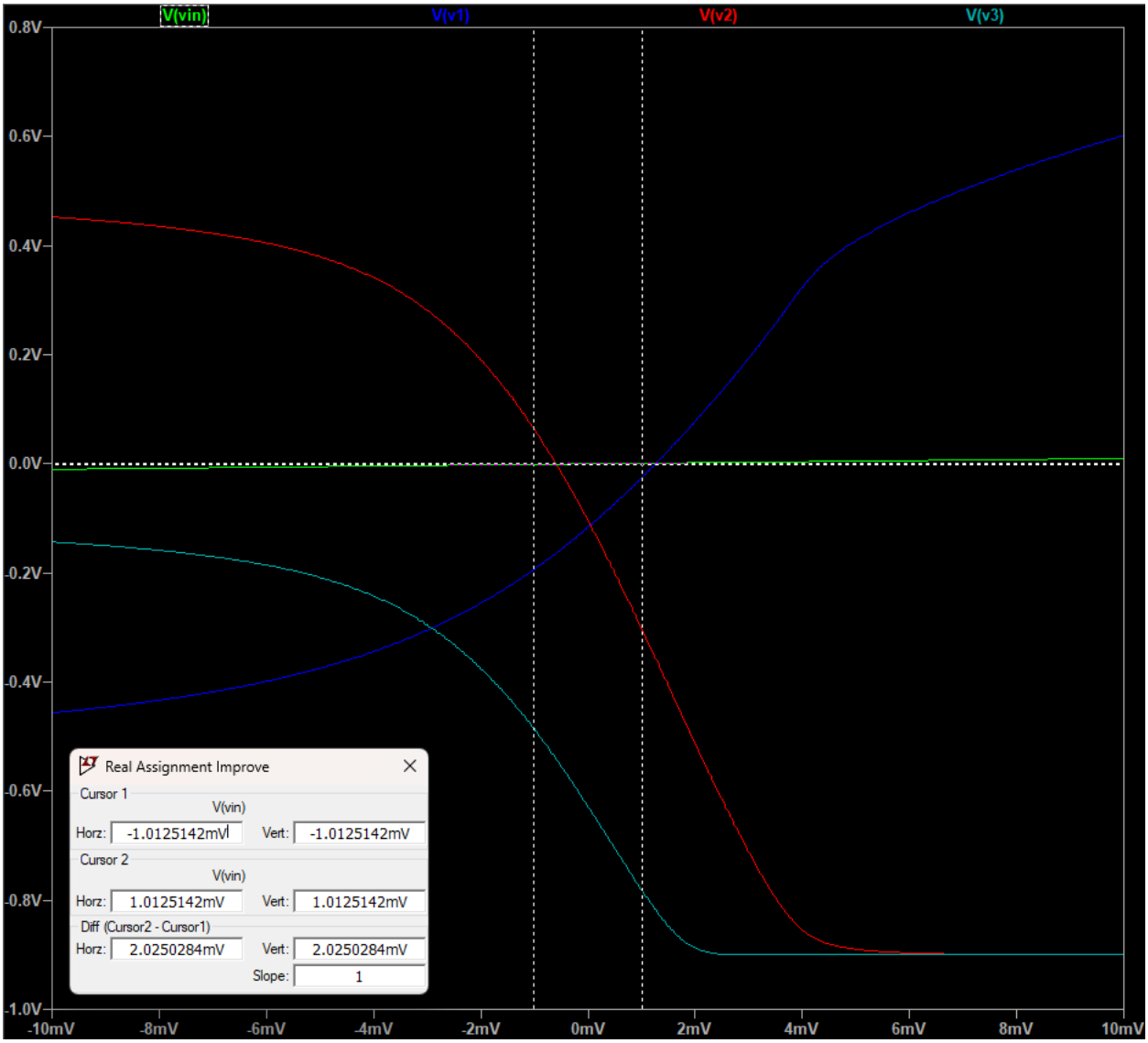

Figure 32: Circuit Enhancement – DC Sweep

Figure 32 shows the DC sweep simulation output where there are 2 cursors placed at around $\pm 1mV$ which is the area where the input signal will swing. The dark blue line V_1 is the output of the telescopic cascode op-amp, which is quite linear, so does the output of the other stages common-source stage (V_2) and common-drain stage (V_3). This means that the circuit can amplify input signal of $1mV$ AC uniformly at every point without going into triode or cutoff region and produce output without significant clipping, cutoff or distortion.

The reason it only allows smaller AC input is because the linear region becomes smaller and smaller as gain increases. As compared to the DC sweep of differential amplifier output in

Figure 21, it is much steeper which means that the gain is higher, at the same linear region had been reduced. In Figure 21 almost the whole range between $\pm 25mV$ is linear.

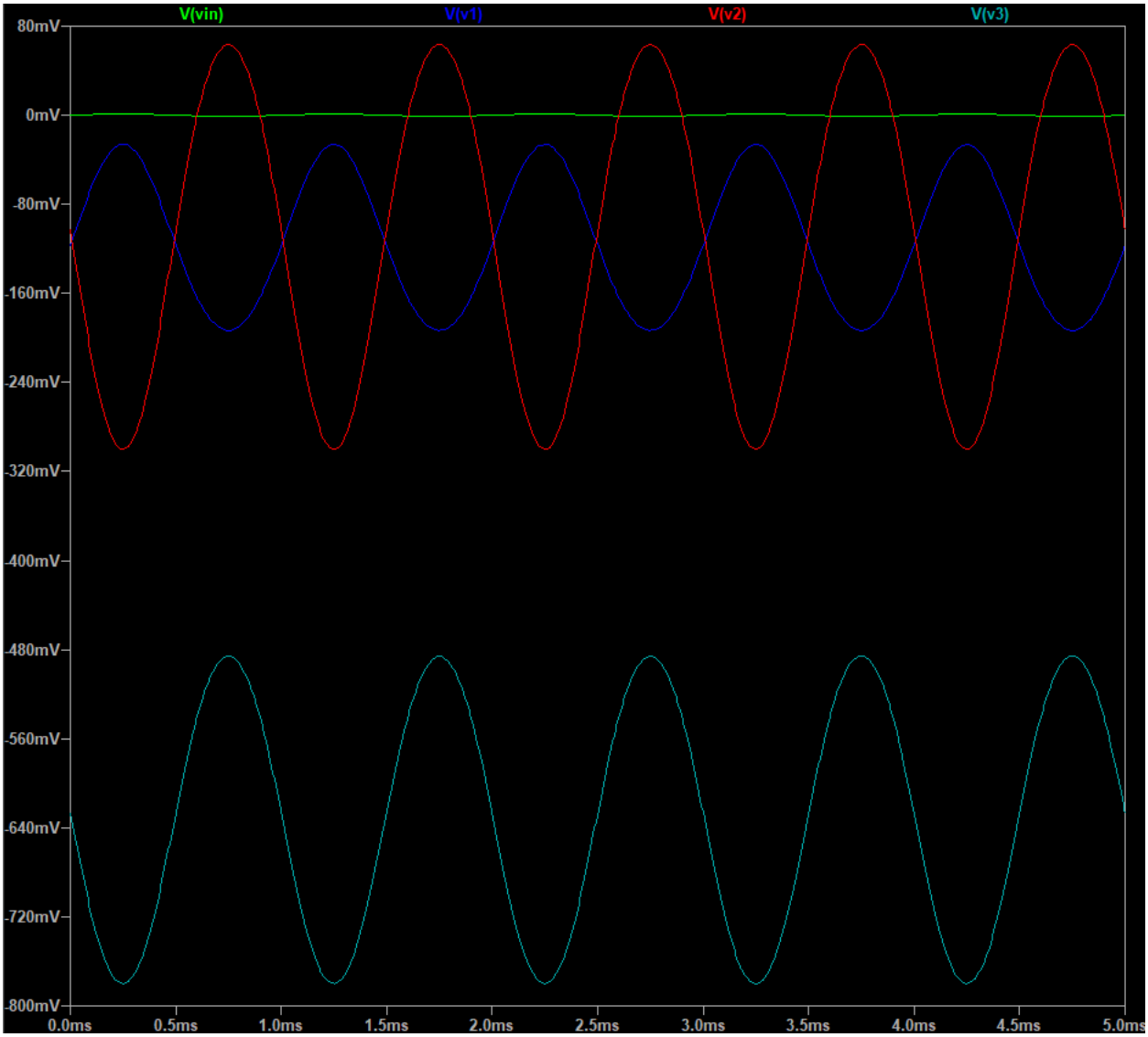

Figure 33: Circuit Enhancement – Transient Response

Figure 33 shows the transient response of each stage where all of the signals had no visible clipping or cutoff which is as expected depending on the output of DC sweep.

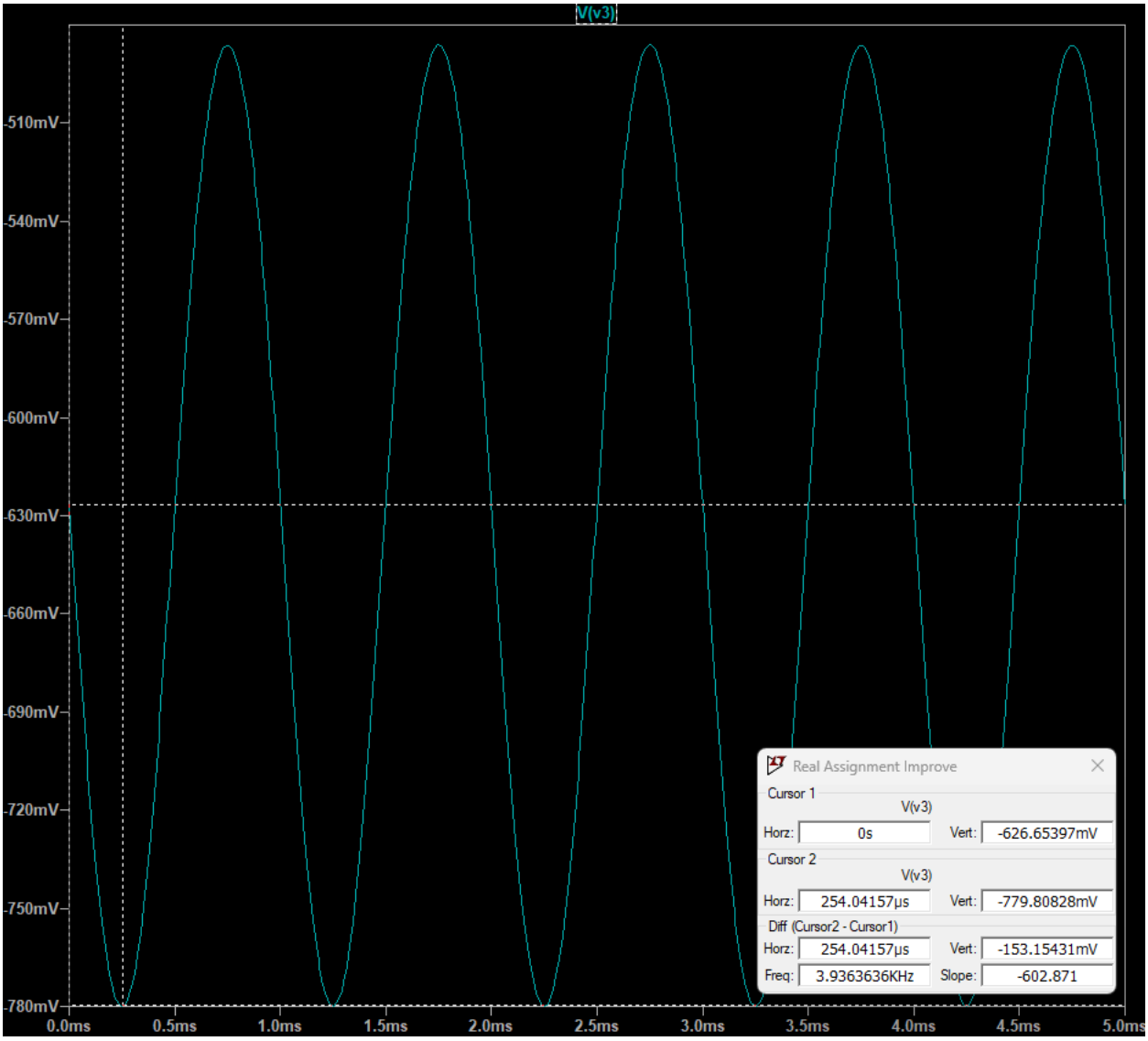

Figure 34: Circuit Enhancement – Final Output Transient Response 1

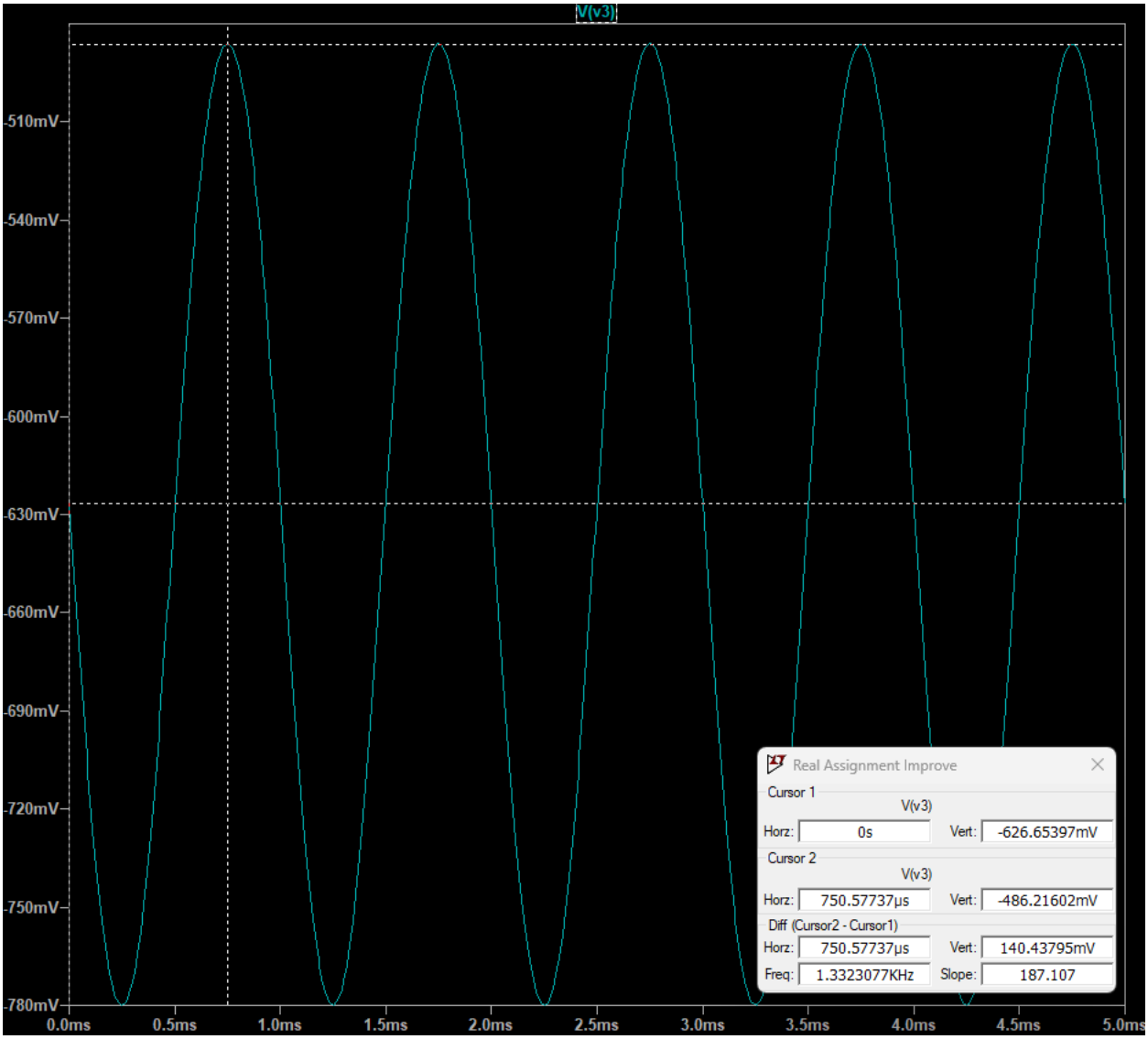

Figure 35: Circuit Enhancement – Final Output Transient Response 2

Figure 34 and Figure 35 shows a more detailed output of the enhanced op-amp which is also the output of the common-drain stage. The output signal is operating at $-656.65mV$, the highest point is $-486.21mV$ and the lowest point is $-779.81mV$. The upper half cycle has the amplitude of $140.44mV$, while the lower half has amplitude of $153.15mV$ which only have a difference of $153.15mV - 140.44mV = 12.71mV$. This proves that the signal is amplified almost equally at every point.

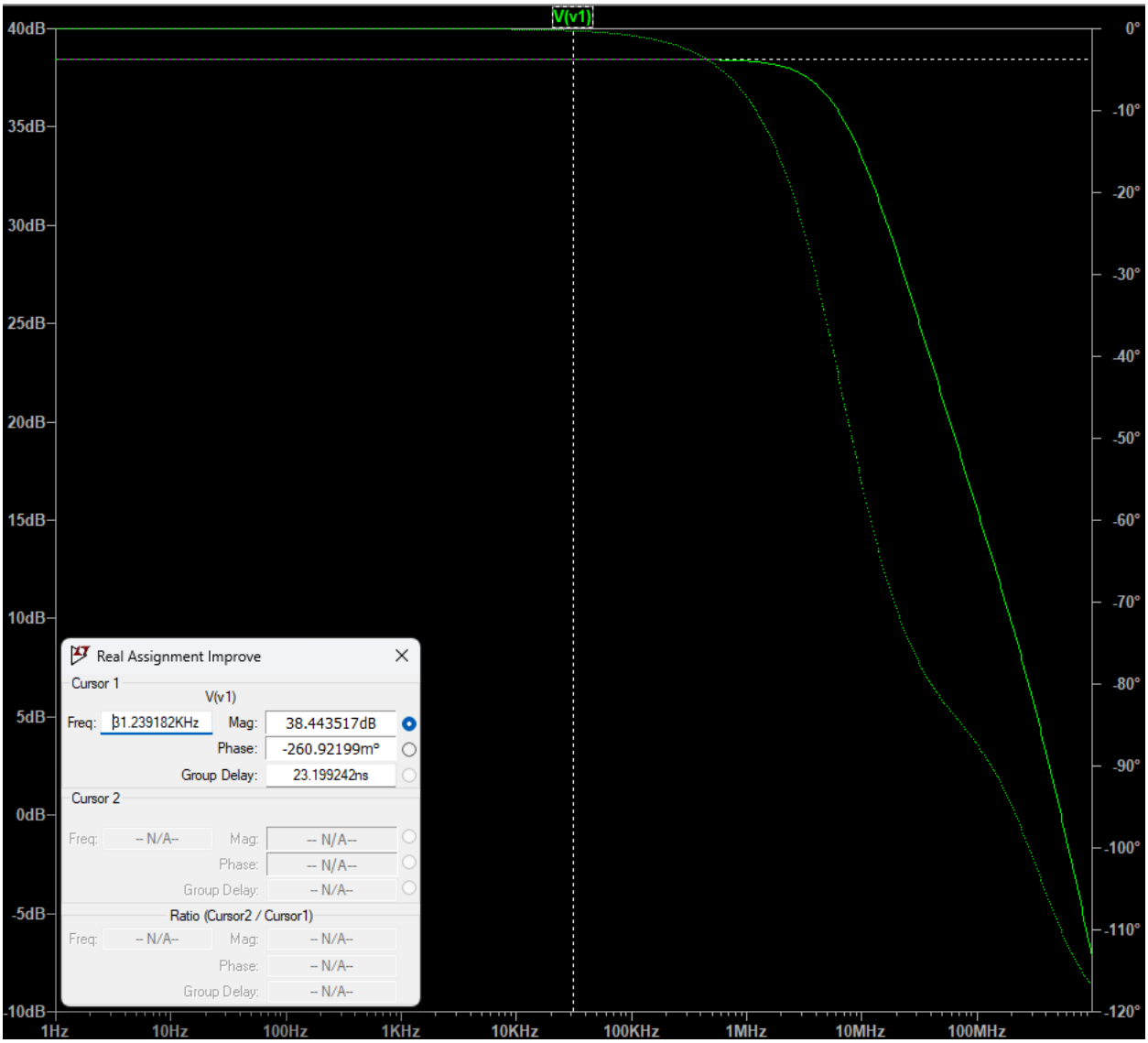

Figure 36: Circuit Enhancement – Cascode Differential Amplifier Output Gain

Figure 36 shows the output gain of the telescopic cascode op-amp which is $38.44dB$ and is already achieving the requirement without the need of extra common-source stage. As compared to a normal differential amplifier, as shown in Figure 25 the gain is only $20.73dB$. Telescopic cascode op-amp can easily provide high gain but at the cost of reduced output voltage swing.

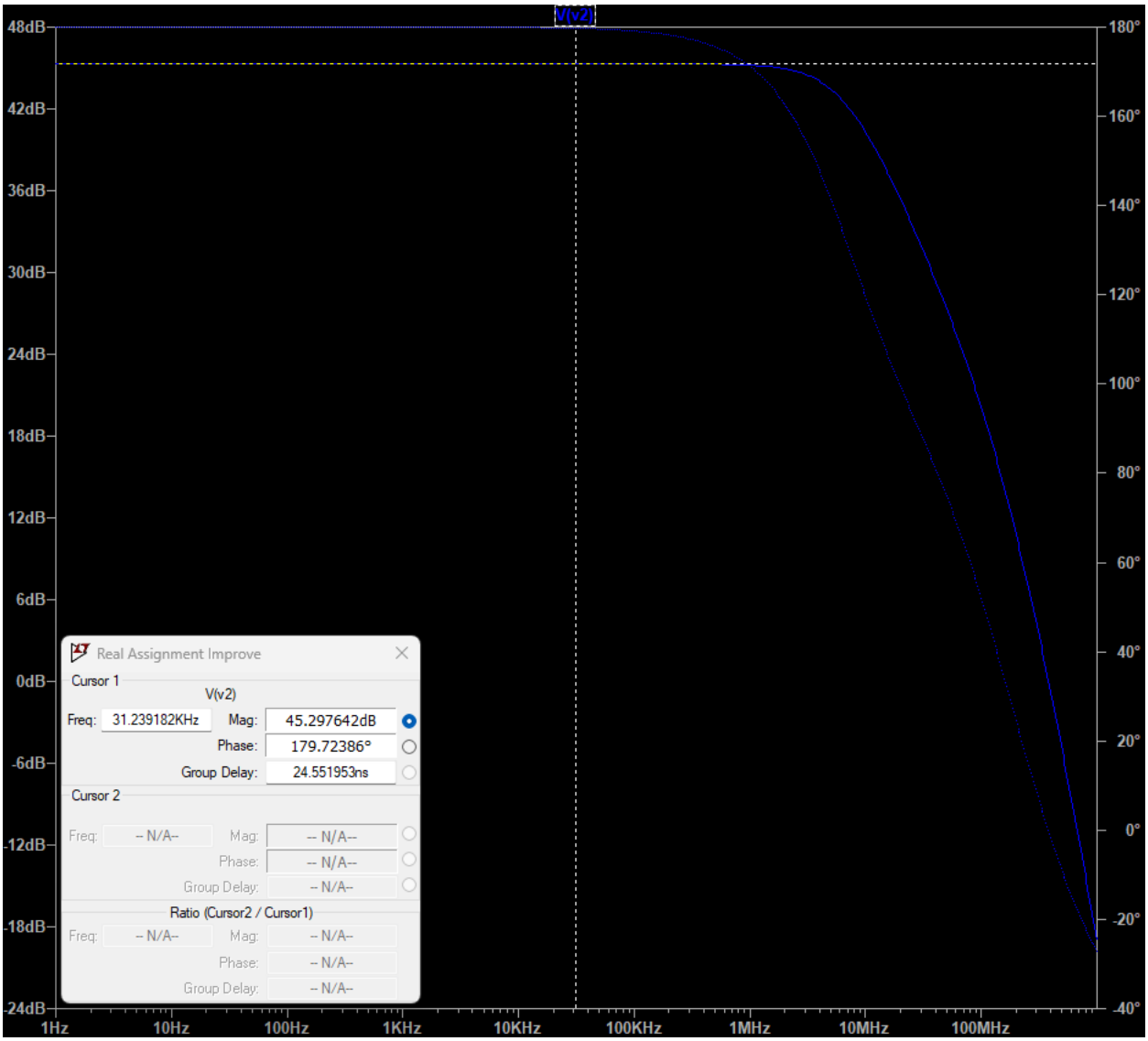

Figure 37: Circuit Enhancement – Common-Source Stage Output Gain

Figure 37 shows the gain of the signal after common-source stage which is $45.3dB$.

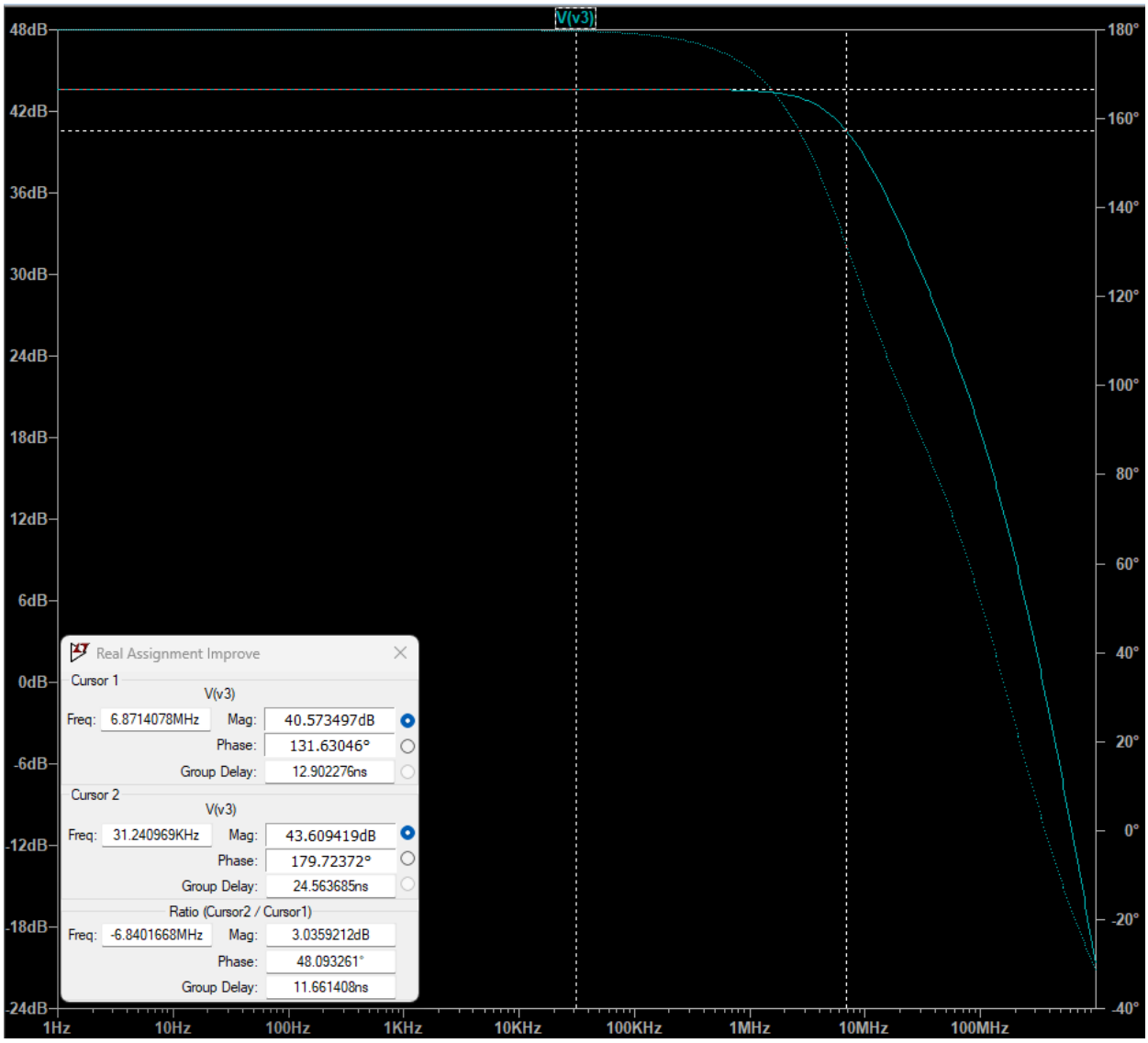

Figure 38: Circuit Enhancement - Final Output Gain

Figure 38 shows the final output gain which is $43.61dB$ and the cutoff frequency at roughly $6.84MHz$.

Discussion

The output of the multi-stage operational amplifier design shows strong alignment with the initial design requirements and specifications. Through extensive simulation and analysis, key parameters such as gain, bandwidth, voltage swing, power consumption and stability were verified, demonstrating the effectiveness of the implemented design.

The total gain achieved in the operational amplifier is $39.98dB$ which is close to the upper limit of the requirement $40dB$. The bandwidth is $10.9MHz$ which also achieved the requirement of minimum 300kHz. The power consumption is only $2.124mW$ which is only close to a quarter of the requirement $8mW$. The operational amplifier design can also amplify input of $5mV$ amplitude AC signal nicely without any distortion, clipping or cutoff and ensuring linearity and high fidelity as shown in Figure 23 and Figure 24.

The analytic calculations on DC analysis are mostly accurate. The analysis on the operating region of the transistors is all accurate where only M5 is in triode region. Besides, the calculated power consumption $2.124mW$ is also same with the simulation result. While for AC analysis, the calculated gain of the circuit $44.47dB$ is slightly off with the simulation result $39.98dB$ due to the assumptions made during the calculation. This is because there are too many parameters to be considered and is very hard to obtain the accurate gain of an amplifier circuit without the help of simulation tools like LTSpice.

The differential amplifier is controlled by the tail current source, which sets the bias current for differential pair M1 and M2. Proper W/L sizing of M1, M2, M3 and M4 ensures adequate gain and linearity. Additionally, the high impedance provided by the current mirror load is critical for achieving the desired output characteristics. Ideally, the voltage gain of a differential amplifier is given by $A = g_m \cdot R_{out}$ where g_m is the transconductance and R_{out} is the output resistance. To increase gain, increasing the width of M1 and M2 will increase their g_m which leads to the increase in the gain of the amplifier. However, the length used in the design for M1 and M2 is only $3\mu m$, this is because of the behavior of MOSFET in differential amplifier under specific conditions. Reducing the width of M1 and M2 will reduce the current passing through M1, M2, M3 and M4. While the effective resistance of M3 and M4 is denoted by $r_o = \frac{1}{\lambda \cdot I_D}$. Hence, when the current decrease, the effective resistance of M3 and M4 increases which cause the overall R_{out} increases then leads to the overall increase in the gain. The rate of gain

decreases due to the reduction of g_m is much slower than the rate of R_{out} increasing. Thus, it is more ideal to reduce the width of M1 and M2 to increase gain. This is why in the design, M1 and M2 width is only $3\mu m$. While having slightly high width of 50μ for M3 and M4 is to increase the gate voltage input into the gate of the PMOS, M7 to reduce its $|V_{SG}|$ slightly such that it can fall into saturation region easier according to the equation $|V_{SD}| \geq |V_{SG}| - |V_{th}|$ while still bring turned on.

Moving on to the common-source stage, PMOS is chosen to shift up the operating point of the output signal such that the common-drain stage will shift down the operating point of the signal by V_{th}. While $8k\Omega$ is chosen as load to give sufficient gain as calculated in the analytic calculation section and shown in AC analysis simulation result.

Lastly, for the common-drain stage, an NMOS is used and a NMOS load is used as the source load. This is to replace the resistor with a transistor because a transistor consumes smaller area on an IC which is more favorable. On top of that, the resistance at the source of common-drain NMOS is not very significant as it is connected in parallel with the load of 30Ω and $30pF$ which is relatively small.

Figure 21 shows the SPICE simulation output of a DC sweep. It is used to understand the behavior of the operational amplifier circuit when a range of input is given. It is also used to identify the operating range of the circuit where uniform gain exists. The green line represents V_{in} swept from $-25mV$ to $+25mV$. While the dark blue V_1, red V_2 and light blue V_3 lines represent the outputs of the differential amplifier, common-source stage and common-drain stage respectively. The range of interest for the AC input signal swing is $\pm 5mV$, as indicated by the two cursors. This range is critical for observing the linear behavior of the circuit, ensuring that all stages operate correctly without distortion. A steeper slope indicates a higher gain. This is because the slope of the graph $\left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)$ indicates how sensitive the output is to changes in the input. The first stage V_1 has the smallest slope, corresponding to a lower gain, as it primarily provides initial differential signal amplification. The second stage V_2 as a much steeper slope, indicating higher gain due to the common-source configuration. The third stage V_3 common-drain stage, has a similar slope to V_2, resulting in almost unity gain. Its primary role is to buffer the signal while preserving its amplitude and phase, rather than providing further amplification.

Within the $\pm 5mV$ input range, the outputs of all stages exhibit linear behavior, indicating uniform gain throughout this region. This linearity suggests that all transistors operate in the saturation region within this range, ensuring consistent signal amplification. When the input signal swings between $\pm 5mV$, the circuit amplifies the signal evenly without any transistors entering the triode or cutoff regions, preventing distortion or clipping. This behavior ensures that the transient response remains clean as shown in Figure 22, Figure 23 and Figure 24, with no signal degradation. These results confirm that the operational amplifier design is capable of handling an AC input signal with a 5mV amplitude as required. Figure 25, Figure 26 and Figure 27 shows the gain of each stage where the final output gain is $39.98dB$ with bandwidth of $10.9MHz$ which fulfilled the requirements perfectly.

Nevertheless, there are spaces for improvement on the circuit. One of the main flaws in the circuit is the high width of M5 $(1800\mu m)$ which is the transistor that is biasing the differential amplifier. It can be further tuned to reduce its width to reduce chip area. Besides, MOS load can also be used to replace the $8k\Omega$ resistor in the common-source stage to further reduce chip area. On top of that, it is also more ideal to design the circuit such that all transistors are in saturation region.

Furthermore, for circuit enhancement, a telescopic cascode differential operational amplifier is implemented to replace the normal current mirror load differential amplifier to provide higher gain. This is because according to the gain formula of a normal differential amplifier which is approximately the equation below referring to Figure 16.

$$A = g_m R_{out}$$

$$R_{out} = r_{o1,2} || r_{o3,4}$$

In a telescopic cascode design, the output resistance is increased due to the cascode configuration, which stacks additional transistors where the gain is approximately the equation below referring to Figure 28 (All About Electronics, 2021).

$$A \approx g_{m1,2}(R_{cascode\ amplifier} || R_{cascode\ current\ source})$$

$$R_{cascode\ amplifier} = g_{m3,4} \cdot r_{o3,4} \cdot r_{o1,2}$$

$$R_{cascode\ current\ source} = g_{m5,6} \cdot r_{o5,6} \cdot r_{o7,8}$$

The cascode transistor effectively increases the output resistance. After implementing the telescopic cascode differential operational amplifier, the gain of the differential amplifier stage had reached a whopping of $38.44dB$ which easily achieved the requirement without the need of

a common-source stage. As comparing the DC sweep in Figure 21 and Figure 32, the slope of differential amplifier output V_1 in Figure 32 is much steeper which indicates higher gain. At the same time, within the range of input into the enhanced circuit $\pm 1mV$, all stages also exhibit linear behavior which indicates uniform gain. The enhanced circuit had a final output gain of $43.61dB$. The power consumption of the enhanced circuit $3.834mW$ is also relatively low which is not even half of the requirement. Besides, it can be further reduced if the common-source stage is removed as it already provides sufficient gain.

However, the enhancement circuit comes with a drawback which is reduced input signal amplitude range and reduced output swing. The stacking of transistors in a telescopic cascode reduces the available headroom for output voltage swing due to the increased voltage drops across the transistors. To ensure equal amplification and prevent cutoff, the circuit can only accept input AC signal of $1mV$ amplitude. According to DC sweep, this drawback comes with high gain where the linear gain region had been decreased. The bandwidth of the enhanced circuit is also reduced which is due to the increased transistors which leads to higher parasitic capacitance as compared to the normal design. On top of that, there is a flaw in the enhanced circuit where M3 and M4 are in triode region which reduces the output resistance of the differential amplifier and reduces the gain. A higher gain can be achieved if M3 and M4 are designed to be in saturation region.

Conclusion

The multi-stage operational amplifier design presented in this report successfully meets the specified performance criteria, showcasing a careful balance of gain, bandwidth, power consumption, and stability. The final design achieves an open loop gain of $39.98dB$, which closely aligns with the required range and a bandwidth of $10.9MHz$, exceeding the minimum specification of $300kHz$. Additionally, the power consumption of $2.124mW$ is significantly below the $8mW$ threshold, demonstrating the efficiency of the circuit.

Key design elements, such as the current mirror load differential amplifier stage, the PMOS common-source stage, and the NMOS common-drain stage, have been analyzed and optimized for their respective roles. The differential amplifier, controlled through its tail current source and load transistors, provides the necessary high gain and linearity. The common-source stage further amplifies the signal, while the common-drain stage serves as an effective buffer to drive the load.

Areas for improvement were identified, including optimizing the width of certain transistors to reduce chip area and exploring alternatives like MOS loads to replace resistors for further area reduction. The implementation of a telescopic cascode differential amplifier in the enhanced design demonstrated the potential for even higher gain of $38.44dB$ in the telescopic cascode operational amplifier alone and with $43.61dB$ final gain, But it introduced trade-offs such as reduced output swing, input range and bandwidth. The implementation of telescopic cascode differential amplifier is also simulated and analyzed in detail to highlight the benefits and drawbacks that it provides.

This assignment underscores the importance of analytical calculations and simulations in achieving a balanced trade-off between gain, bandwidth, power consumption and stability.

References

Analog Devices. (2018). *Chapter 11: The Current Mirror.* https://wiki.analog.com/university/courses/electronics/text/chapter-11

Razavi, B. (2017). *Design of Analog CMOS Integrated Circuits.* Mc Graw Hill Education.

Keim, R. (2016) *The MOSFET Differential Pair with Active Load.* https://www.allaboutcircuits.com/technical-articles/the-mosfet-differential-pair-with-active-load/

Gulati, K., & Lee, H., S. (1998). A High-Swing CMOS Telescopic Operational Amplifier. *IEEE Journal of Solid-State Circuits, 33*(12), 2010–2019

All About Electronics. (2021). *Cascode Amplifier using MOSFET Explained.* https://www.allaboutelectronics.org/cascode-amplifier-using-mosfet-explained/