GROUP ASSIGNMENT

TECHNOLOGY PARK MALAYSIA

EE008-3-2-DE

DIGITAL ELECTRONICS

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Introduction

The purpose of the group assignment is to investigate several digital timer circuits which includes a 15 hours clock with varying minutes and seconds, a 10 hours clock with varying minutes and seconds, and a 7 hours clock with varying minutes and seconds. After investigating and designing the designated clock specification we will design a digital clock that can display the three different digital timer circuits and switch between them. We combine the best features from each of our group members into a single digital clock circuit as it would have the best of both worlds. The combined features of the digital clock work extremely well together and makes the clock more realistic. We will justify the reason to choose the best feature from each of our individual clock designs and combine it into a single clock design.

The result of combining the best features from all of our individual circuits has made a masterpiece of a clock as it has a myriad of features that go well with each other. For example, the combined digital clock's minute and second can be changed according to the user's preference. There is a reset feature that allows the user to reset their clock back to 0. There is a pause feature that allows the user to pause the clock. There is a feature where the user can edit their clock's hours, minutes and seconds to fit the exact time that the users want and there's also a feature where the user can alter the alarm of the clock where the clock will buzz after a given interval.

The group report is crucial because it teaches the user on how a clock works by breaking down the clock's logic so that it's easier to understand. At the end of the day, the clock's design is purely made from various IC's which in and of itself are constructed by logic gates. Hence, this huge project with several extraordinary features can be simplified to logic gates. We however, prefer to use IC instead of logic gates because it is more cost effective and more aesthetically pleasing.

Objective

The objective of this group assignment is to study a clock circuit that displays time in three distinct formats. The digital timer will show time in hours, minutes, and seconds, with three different time ranges which includes 15 hours, 10 hours, and 7 hours. The display mode can be selected by adjusting the input values to the control unit which is the 4 to 1 mux where there will be 4 inputs into the mux and only 1 output will be selected as display. The mux is controlled by the user to choose their desired output. There will be only one mode of operation active at any given time in the clock design.

Besides that, there are also different designs of clock circuits for the minutes and seconds section. Hence, the objective of the group assignment is also to choose the best or integrate the clock circuits design of all the members to come up with the most marvelous design clock that is going to be done as the prototype.

In addition, the objective of the group assignment is also combining all the extra features that are designed by each group member so that the integrated design and the prototype will contain many different features that will make the clock circuit design more user friendly and have more functionalities.

Components Required

Components list of the circuit design plays a very important role in understanding the design and its complexity. It serves as a guide for future modification or enhancements to the design. Table below contains the list of components we have used in our circuit design. It is important to note that the simulation tool we used, Logisim, focuses solely on the logical aspect and operates with the bare minimum of components. Therefore, the list in table below excludes components such as power supply and resistors that would typically be required for a real-world implementation.

#	**Component Name**	**Component Qty**
1	JK Flip-Flop	29
2	D Flip-Flop	16
3	AND Gate	24
4	OR Gate	12
5	X-NOR Gate	16
6	4 to 7 Decoder	6
7	Seven Segment Display	6
8	Slide Switch	20
9	Push Button	4
10	4 to 1 Multiplexer	6
1	Buzzer	1

Table 1: Component Table

Proposed Design

15 Hours Clock (Su Xin Hong TP061159)

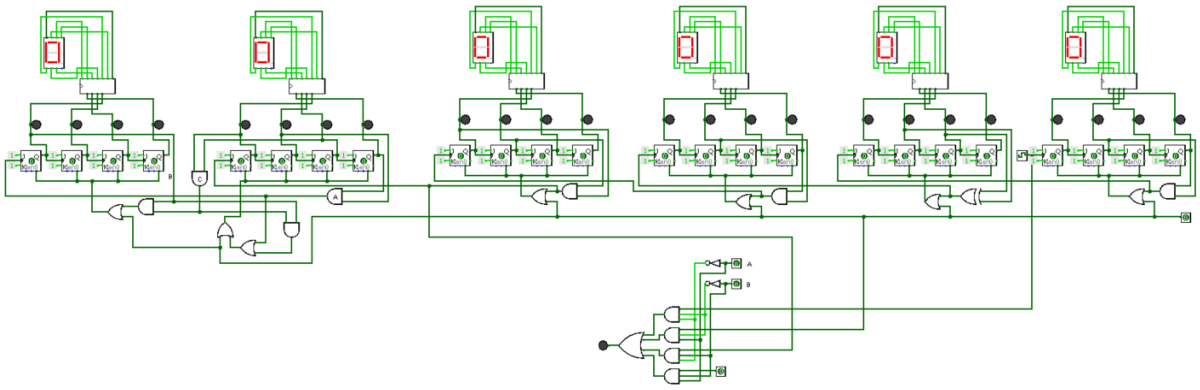


Figure 1: 15 Hours Clock Design

The figure above is the 15 hours clock design with 20 seconds per minute and 30 minutes per hour. On top of that, there are also 2 additional extra features which are the reset button and the sound notification system.

The feature of the reset button is to reset all the JK flip flops in the whole clock circuit. This is done by integrating the signal that is used to reset the JK flip flops when they hit the threshold or limit, with a button. Two of the signals are combined with an OR gate so that all the JK flip flop will be reset when the button is pressed.

While for the sound notification system. There is a LED used to represent the buzzer because there is no buzzer component in Logisim. The circuit design of 4 AND gates and 1 OR gates with 4 inputs is the MUX component where it will accept 4 inputs and choose 1 from it as the output. The output of the MUX is controlled using the switch A and B. The first input into the MUX is the clock signal where it will light up the LED whenever each second passes. While the second input is the signal that is used to increment the minutes section. Hence the LED will light up whenever there is an increment in the minutes section to indicate 1 minute had passed. This is also the same for the third input where the input is the signal to increment the hours section. The last input will be left empty to give the choice to the user to turn off the sound notification system.

10 Hours Clock (Mohammad Fawzan Alim TP064501)

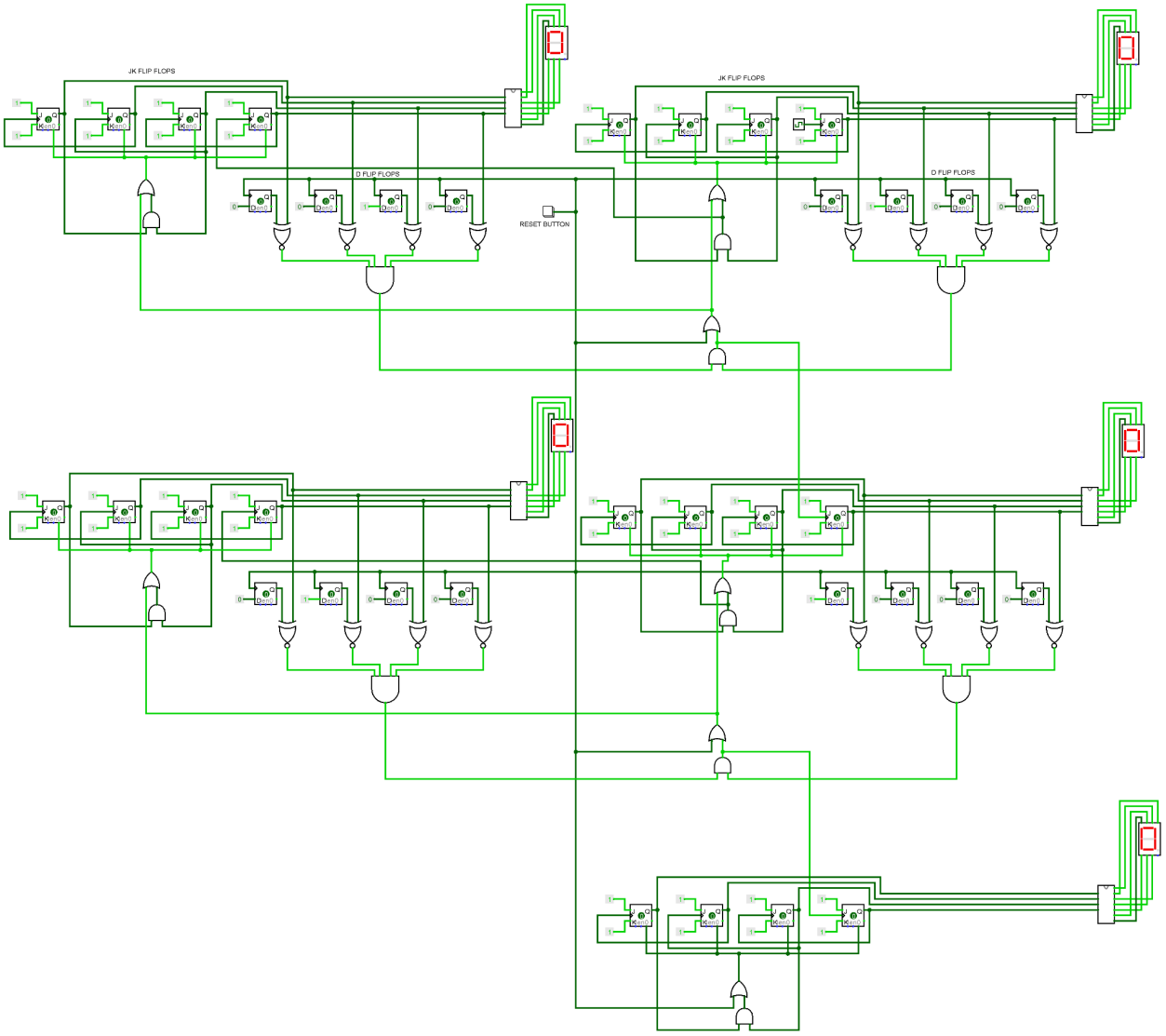


Figure 2: 10 Hours Clock Design

The figure above is the design for the 10 hours clock. Top two displays are for seconds, the middle ones are for minutes and the bottom most display is for hours. As for minutes and seconds, I have decided not to go with any fixed numbers. That means the user can configure the clock based on their need to any number of minutes per hour and any number of seconds per minute. They will achieve that using the switch for every bit. Each digit of the minutes and seconds can go up to 9. 9 in binary is 1001, which is four bits. Therefore, we will need four switches per display. That means, four displays for minutes and seconds will have 16 buttons in total.

A new problem arises with the integration of configurable switches. If they alter the values of the switches while the clock is in operation, it will read the new values and will have a very high chance of malfunctioning. Even if it does not malfunction, it will give us wrong information. To avoid that, I have used a D flip-flop along with every switch. The D flip-flops read the switches as the input and hold on to the value while the clock is in operation. Because of this, even if the user alters the switches, the clock functions according to the old value without the risk of malfunctioning as it works based on the value it gets from D flip-flops instead of switches. The only way to reset the number of minutes per hour and number of seconds per minute is to press the reset button and start from scratch. The reset button is connected to the clock (CLK) pin of the D flip-flops. So, when the button is pressed, the D flip-flops reset and read the new values from the switches.

To check if the current minutes and seconds of the clock are matching with the value from the configurable switches, I have used X-NOR gates. X-NOR gate gives us high output when the inputs are the same. This way, we can detect when the values coming from the clock and values coming from the switches are matching. Then I have checked if all four bits are matching at once using an AND gate. If both digits of seconds are matching, that means we have reached the limit. Once that happens, I have reset both digits of seconds by resetting the JK flip-flops. At the same time, I have sent a signal to the minutes section. The Minutes section works identically to the second's section.

This is a brief explanation of my 10 hours clock functionality. The detailed report and design process can be found in my individual report.

7 Hours Clock (Nicholas Tan Peng Gen TP061291)

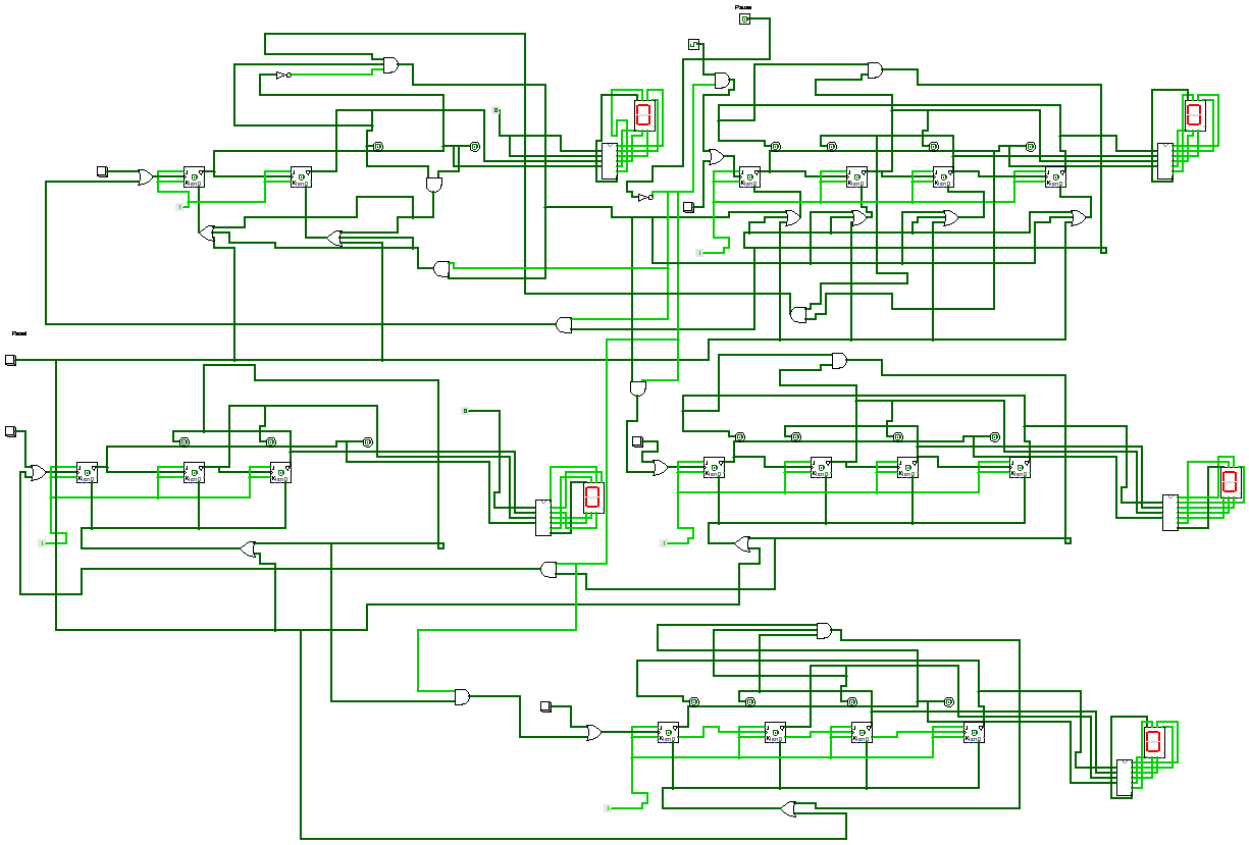


Figure 3: 7 Hours Clock Design

The figure above is the 7 hours clock design with 40 minutes per hour and 25 seconds per minute. There are 3 additional features that were incorporated in this design which are the reset button, the pause feature and the ability to set the time to whatever time the user wants.

The features of the reset button allow the user to reset all the J-K flip flops to 0 in the whole circuit. There are several ways that this is accomplished. The first way is when the counter hits a specific limit. For example, if the counter reaches 10, it resets to 0. The next way to reset the counter is by pressing a button which will directly feed a signal to the clear pin of the J-K flip flop.

The next feature is the pause feature. The pause button is a switch that can be turned ON or OFF. When the pause button is switched ON, it prevents the clock signal from the clock signal generator from entering the first J-K flip flop's clock pin. This would prevent the clock from continuously counting upwards and let the clock's time remain the same until the pause button was

pressed. For example, if the clock's time is 5 hours 24 minutes and 19 seconds and the pause button was switched on, the time would remain at 5 hours 24 minutes and 19 seconds until the pause button is switched off.

The last feature is the ability for the user to set the clock's time. There are buttons for each digit of the clock. The user can press the button to increase the number value of that particular digit by 1. For example, if the user wants to increase the hour from 2 hours to 5 hours, the user will need to press the hour digit button 3 times. The digit will reset to 0 if the button is pressed until the digit exceeds the limit of the clock. The best way to use this feature is to use it along with the pause feature. If the user edits the digit while pausing the clock, when the digit resets because it reaches the limit, the reset wouldn't affect the other digits. Therefore, it is a more efficient way of editing the clock's time.

Initial Integrated Circuit Design

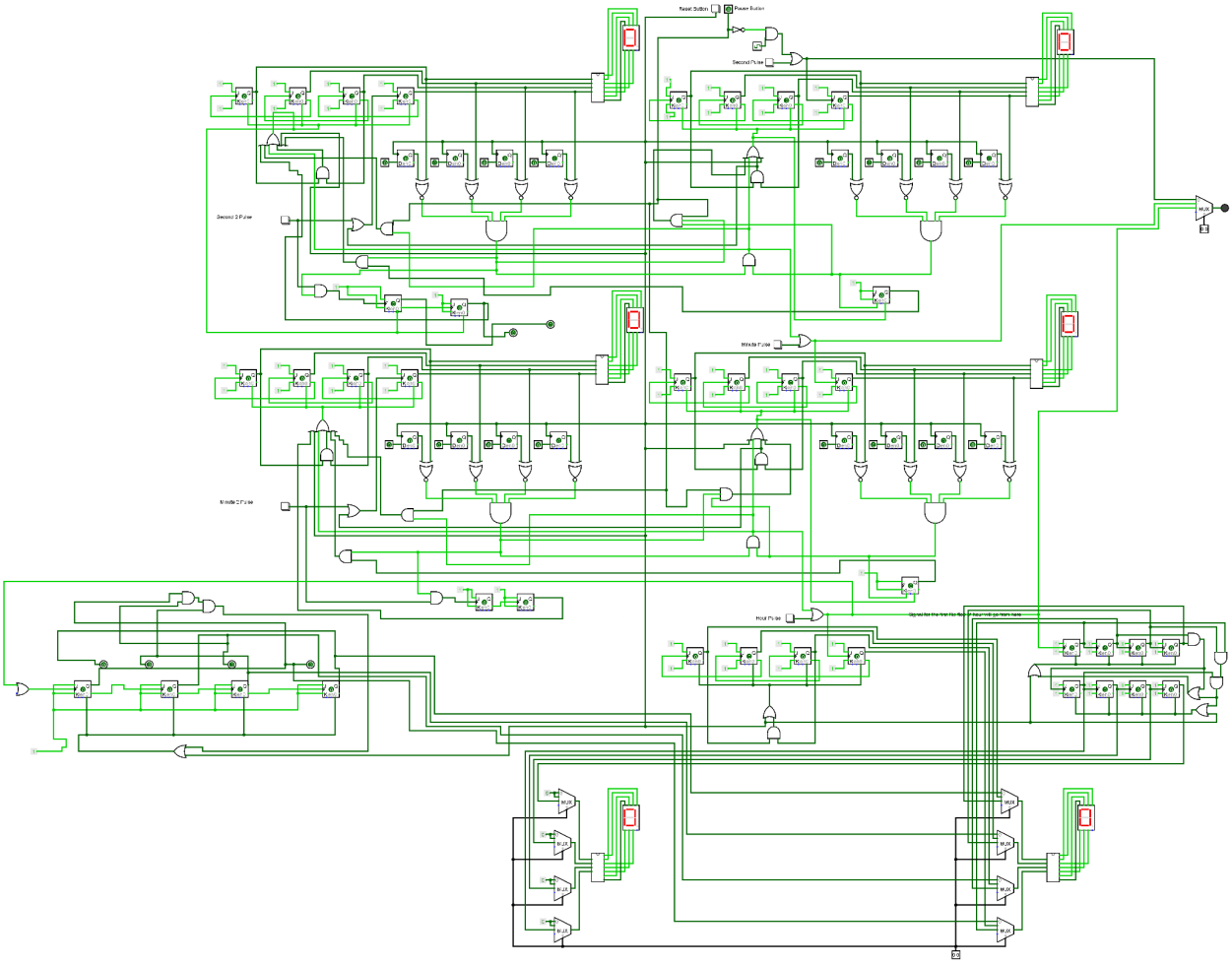


Figure 4: Initial Integrated Circuit Design

The figure above shows the initial integrated design that we came up with. This design has all the features from the various design clocks. At first glance the integrated design looks extremely daunting as it is complex. The initial integrated design uses a lot of J-K flip flops to incorporate the time setting feature.

The difference between the initial integrated design and the final integrated design is that the initial integrated design can fully set the time of the clock with a lot of validations. In the image above there are several buttons that are located near the display. The button is an ON/ OFF button which when pressed, releases a pulse which triggers the negative edge J-K flip flop. This increases the counter of the J-K flip flop by 1. Since there are two buttons for the minutes and the seconds, each of the buttons serve different purposes. The first button is responsible for increasing the value

of the “ones” while the second button is responsible for increasing the value of the “tens”. By pressing the “ones” button that controls the second, the “ones” in the second will increase by 1. For example, if the user presses the “ones” button that controls the second two times when the second initially displays 20, the new second will be 22. Similarly, by pressing the “tens” button that controls the second, the “tens” in the second will increase by 1. For example, if the user presses the “tens” button that controls the second two times when the second is initially 20, the new second will be 40.

Having the “tens” button for the hour and minute helps improve the quality of life for the user as they do not have to press the button twenty times to increase the “tens” digit by 2. Instead, they would only need to press the “tens” button twice. The “tens” button also lets the user revert back the time as the digit would reset to 0 if they reached their specific limit. For example, if the user sets the limit of the second to 45, and the current second is 22, if the user presses the “tens” button three times, the new second display will be 05. This is because the value 2 will increase to 3, then to 4, the next increment will make the value larger than 45, hence, the “tens” will reset to 0. 05 seconds is less than 45 seconds. Hence, it can be seen that the “tens” button helps the user set the time to a previous time in a much more efficient manner.

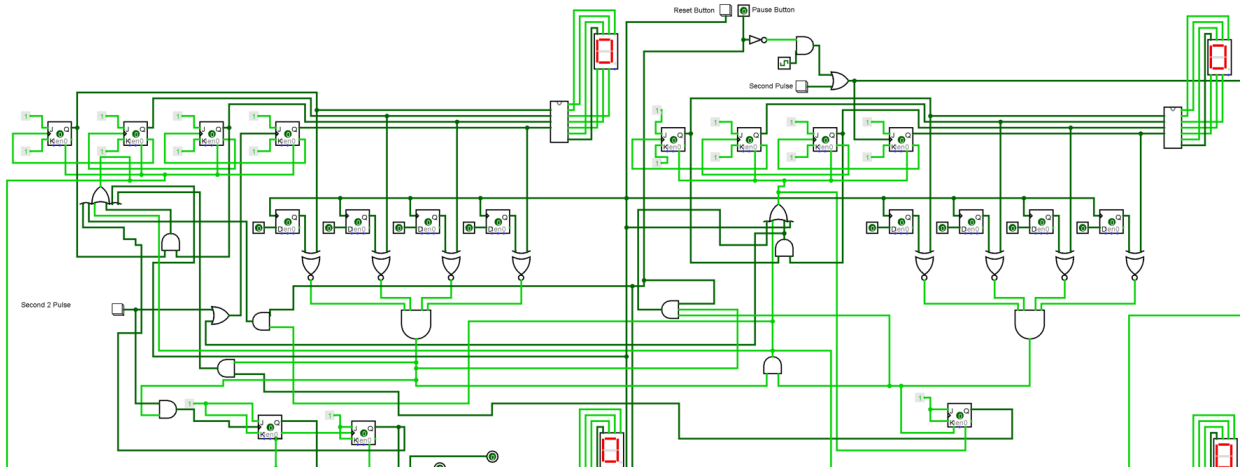


Figure 5: Initial Integrated Circuit Design (Seconds Section)

In the figure above, there are several additional J-K flip flops that were used to ensure that the clock runs smoothly. There is a single J-K flip flop on the “ones” digit that is used like a flag, where it has an on and off state. This is to prevent a bug where if the user sets the second to 28 on a 44 second limit clock and presses the “tens” button twice. This would result in the second

becoming 48 which is over the limit of 44. Therefore, the limit of the 2nd digit of the second will be used as a benchmark, when the counter of the "ones" digit in the second exceeds that benchmark, the state of the J-K flip flop is set to 1 and it can only be cleared if the counter is reset to 0. The state of the J-K flip flop, which is 1 with some logic gates, prevents the second digit from hitting their digit's limit, which in the previous case, it is 4. Therefore, the "tens" digit will increase to 3 then reset if the user increases it further. This prevents the clock from going over the limit that it was set to.

The reason why there are two J-K flip flops on the "tens" digit is because if the logic was to reset the seconds at 45 seconds, when the "tens" digit hits 4, the AND gate will be true and the counter will be reset. Therefore, the clock would look something like this if the "tens" were to be incremented from 22. 22 seconds would become 32 seconds, and then it would reset to 02 because of the initial AND gate becoming true. The J-K flip flops serve as an additional counter that holds on to the value so that the user can increase it to 40 instead of resetting it when the "tens" reaches 4.

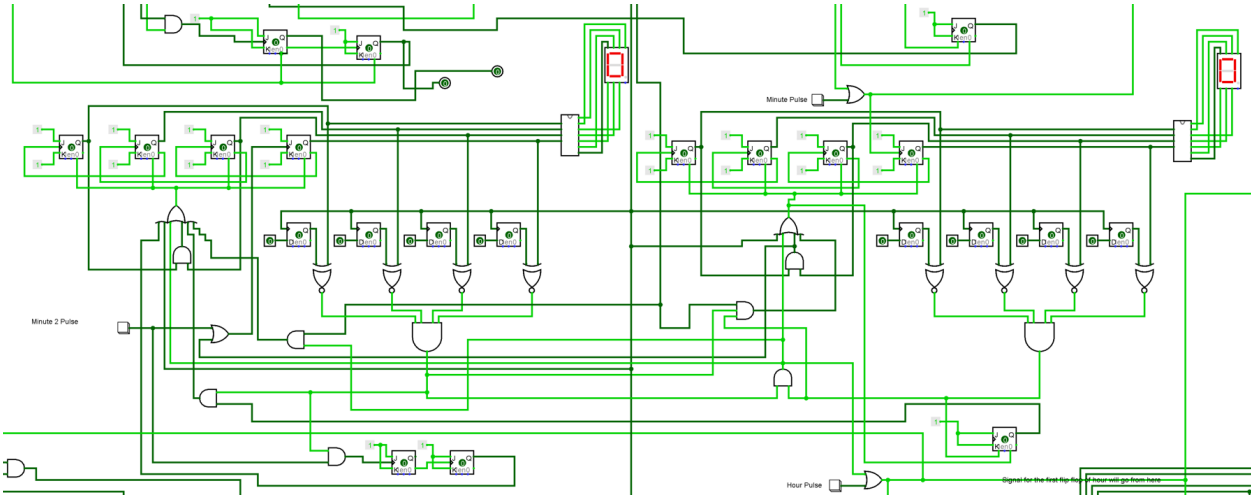


Figure 6: Initial Integrated Circuit Design (Minutes Section)

The minute segment has the same J-K flip flop configuration with the seconds and the functionality is similar to the seconds segment.

In addition to that, there are several ways for the user to reset the clock. One way is for the digit to reach the limit set by the user. Another way that the clock can be reset is by pressing the reset button located on the center top of the whole image.

Another additional feature that is incorporated is the pause feature. Where a user can stop the counter of the clock which freezes the clock's display when the user turns on the switch. This is because the turning on of the switch disconnects the J-K flip flop with the clock signal generator. The pulse from the clock signal generator can't feed the pulse signal to the J-K flip flop clock pin.

In addition to that, another additional feature is the ability of the clock to set the limit for the second and minutes. The user can manually configure their desired limits for the seconds and minutes. This gives the user control over the clock. For example, the user can set the limit for the seconds of the clock to be 30 and seconds won't go past 30 seconds.

Finally, another additional feature that is added is an alarm, the user can manually change whether the user wants the alarm to buzz every second, minute or hour. There is no buzzer in Logisim therefore, it is represented with an LED in the image of the initial integrated circuit.

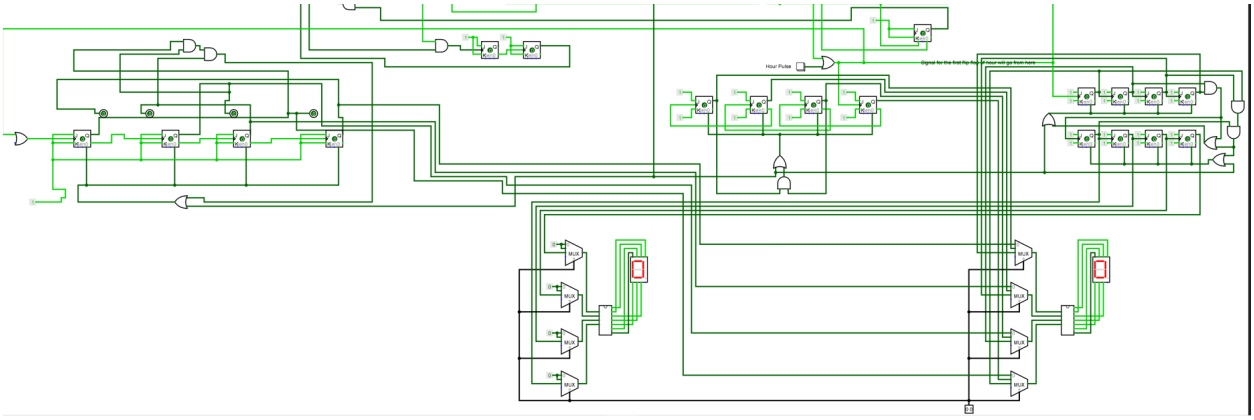


Figure 7: Initial Integrated Circuit Design (Hours Section)

There are three different hours that the user can choose from which is 7 hours, 10 hours or 15 hours. The user can select different hours by toggling the switch to select their preferred hours. The output from the switch goes into a 4 to 1 mux which then chooses the appropriate hours for the user.

Initial Simulation Result

Minutes and Seconds Section

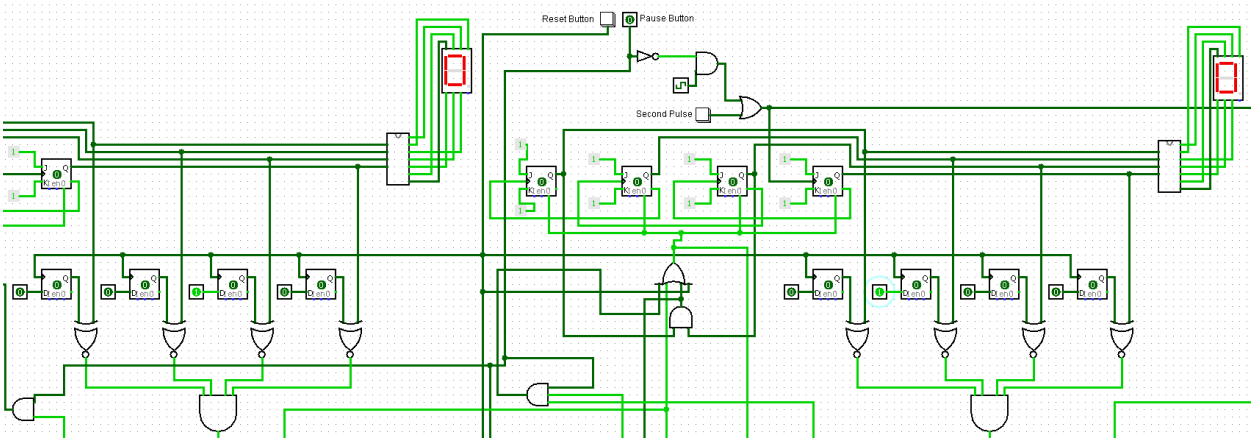


Figure 8: Initial Design Minutes and Seconds Section Simulation 1

Diagram above is showing the switch that is used to control the limit of seconds is set to 0100 in the first digit and also 0010 in the second digit. Hence this means that there will be 24 seconds in a minute and the seconds section will reset once it hits 24 seconds and add 1 into the minutes section.

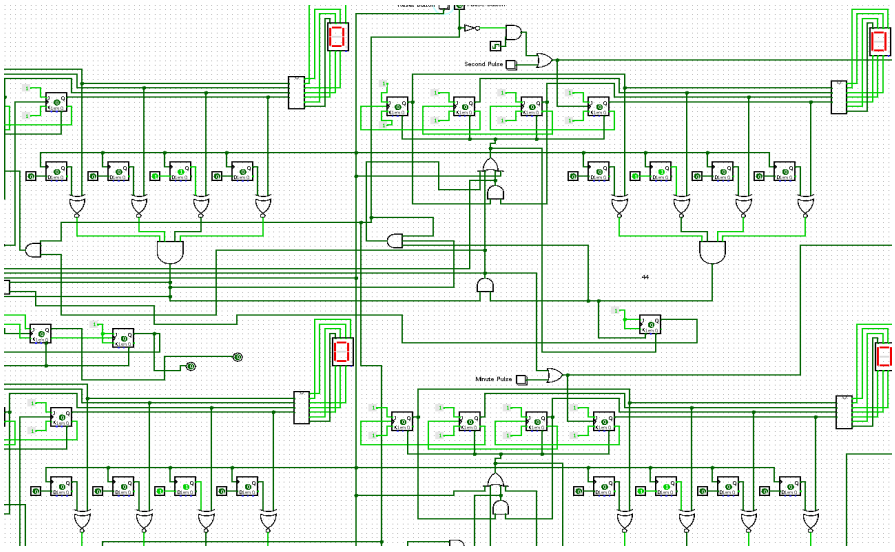
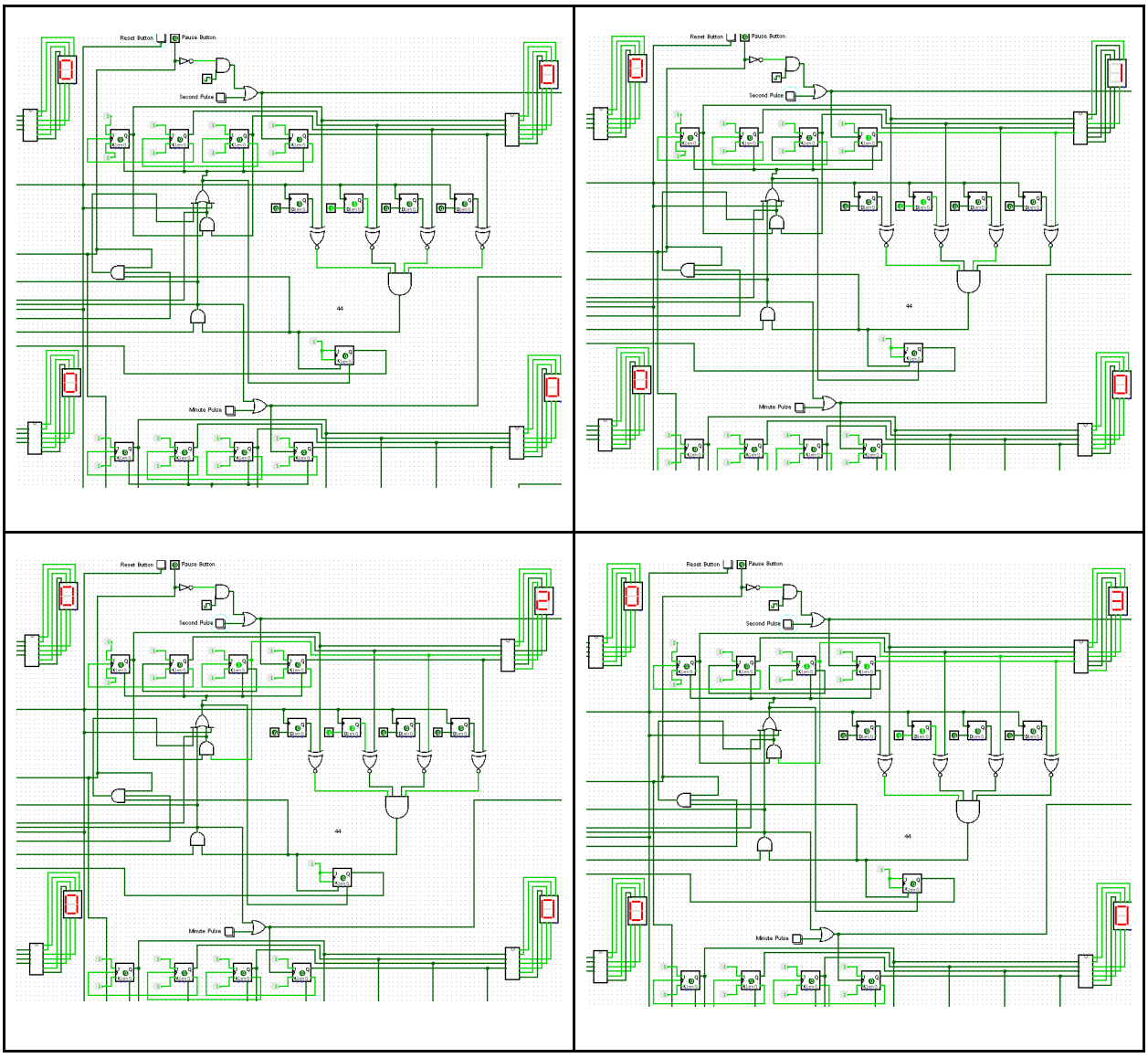
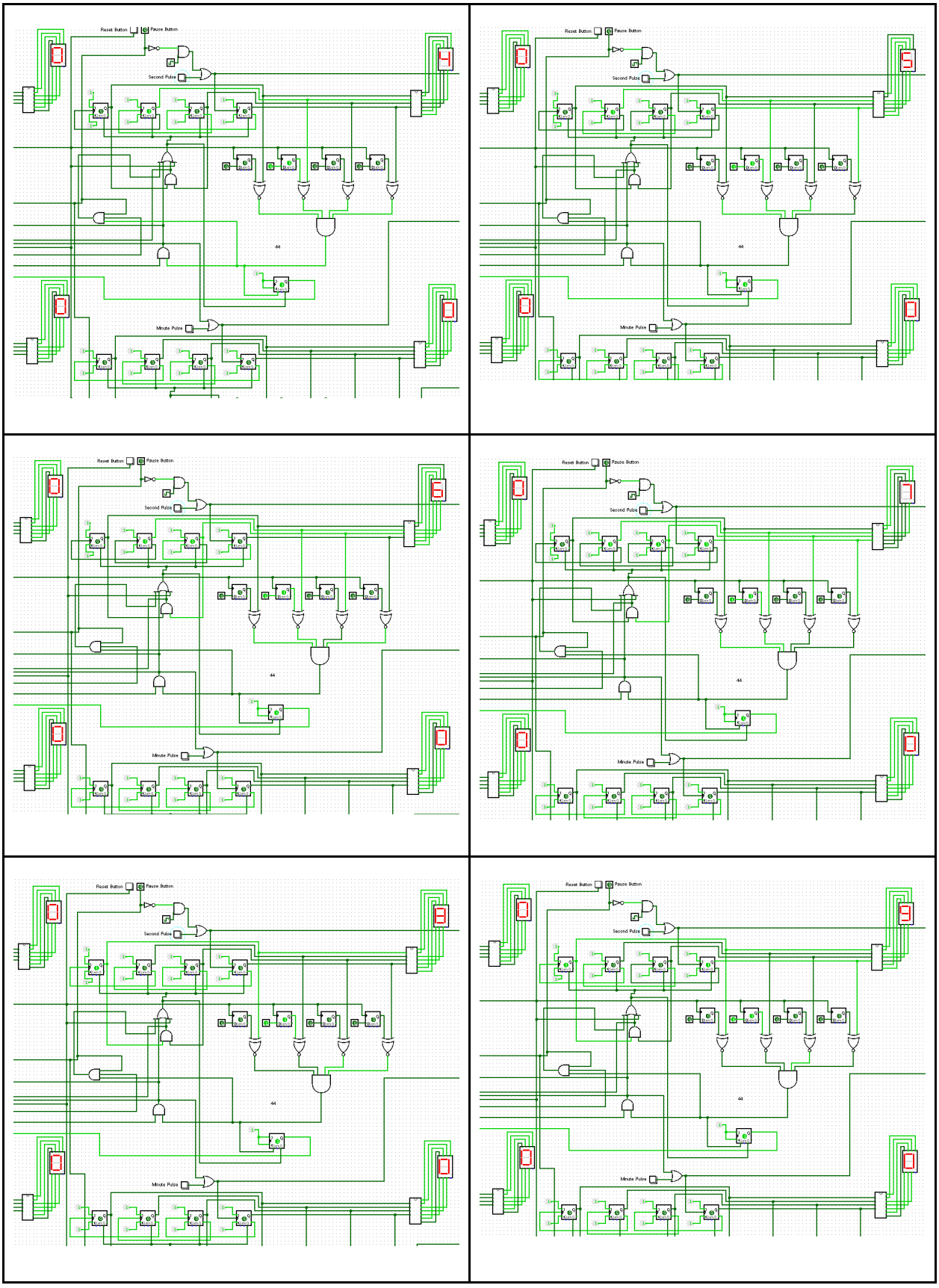
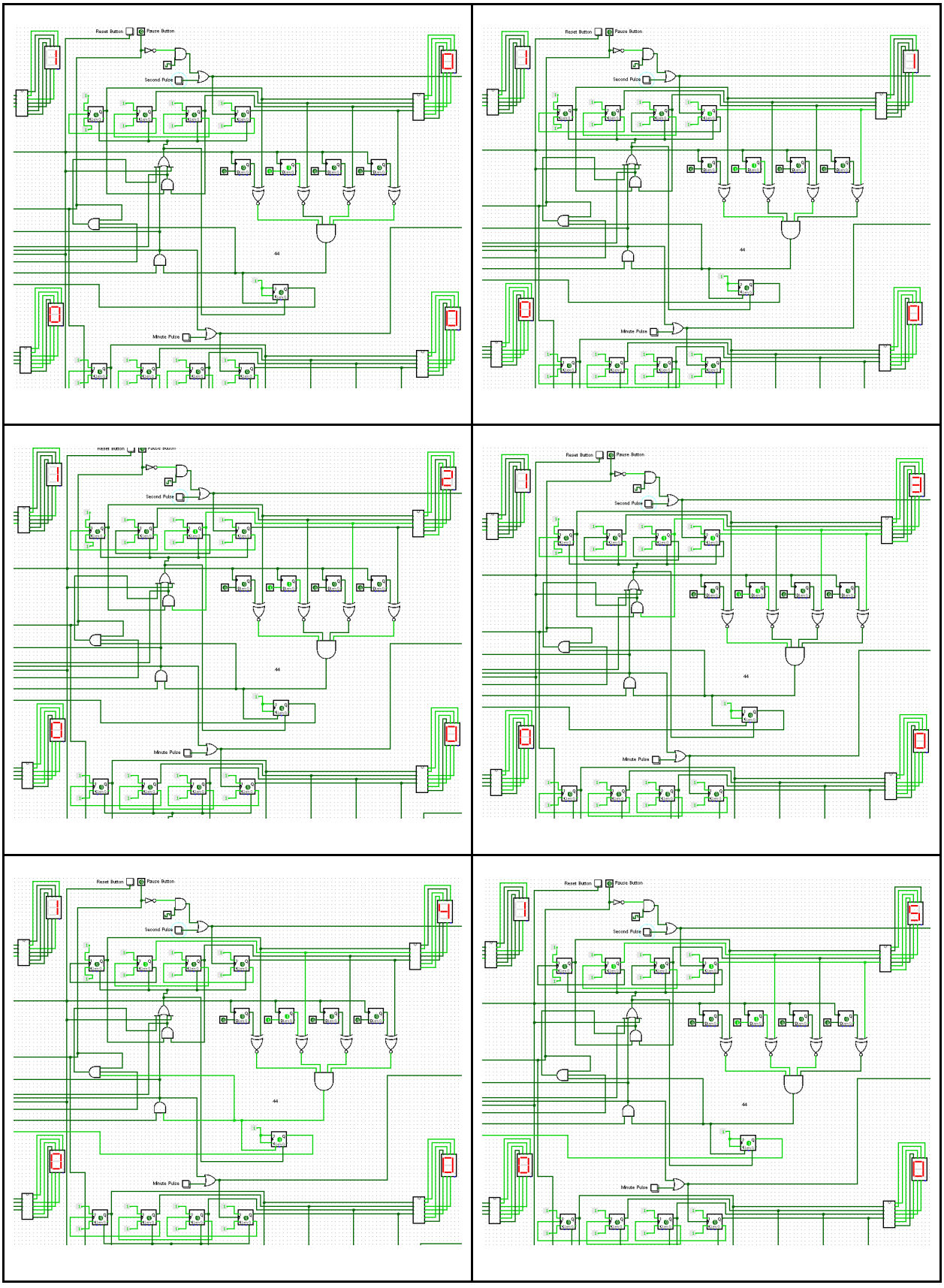


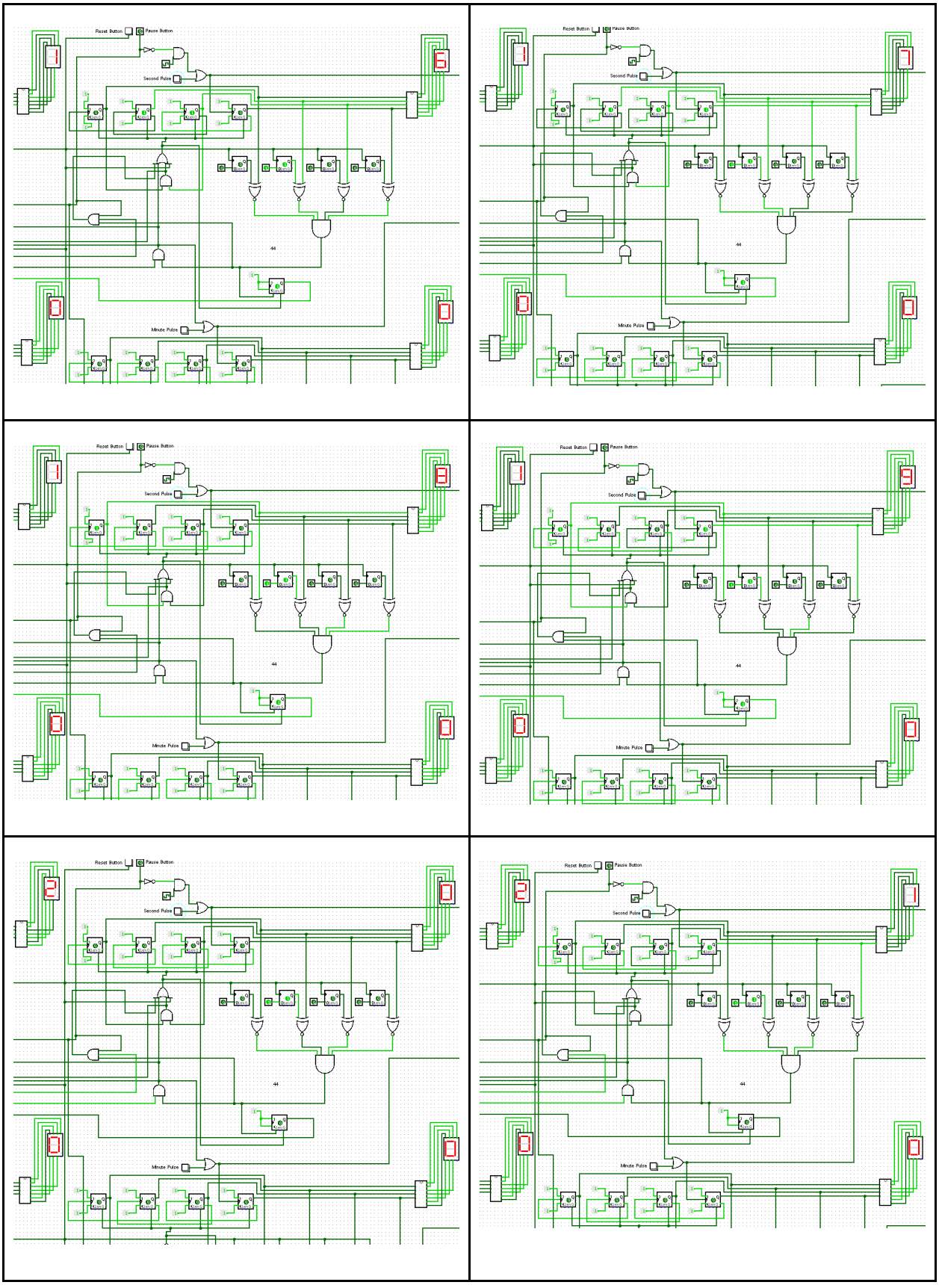
Figure 9: Initial Design Minutes and Seconds Section Simulation 2

Diagram above shows the initial condition of the seconds and minutes section before running the simulation.


Reset Button
Pause Button
Second Pulse
Minute Pulse
44


Reset Button
Pause Button
Second Pulse
Minute Pulse


Reset Button
Pause Button
Second Pulse
Minute Pulse
44


Reset Button
Pause Button
Second Pulse
Minute Pulse

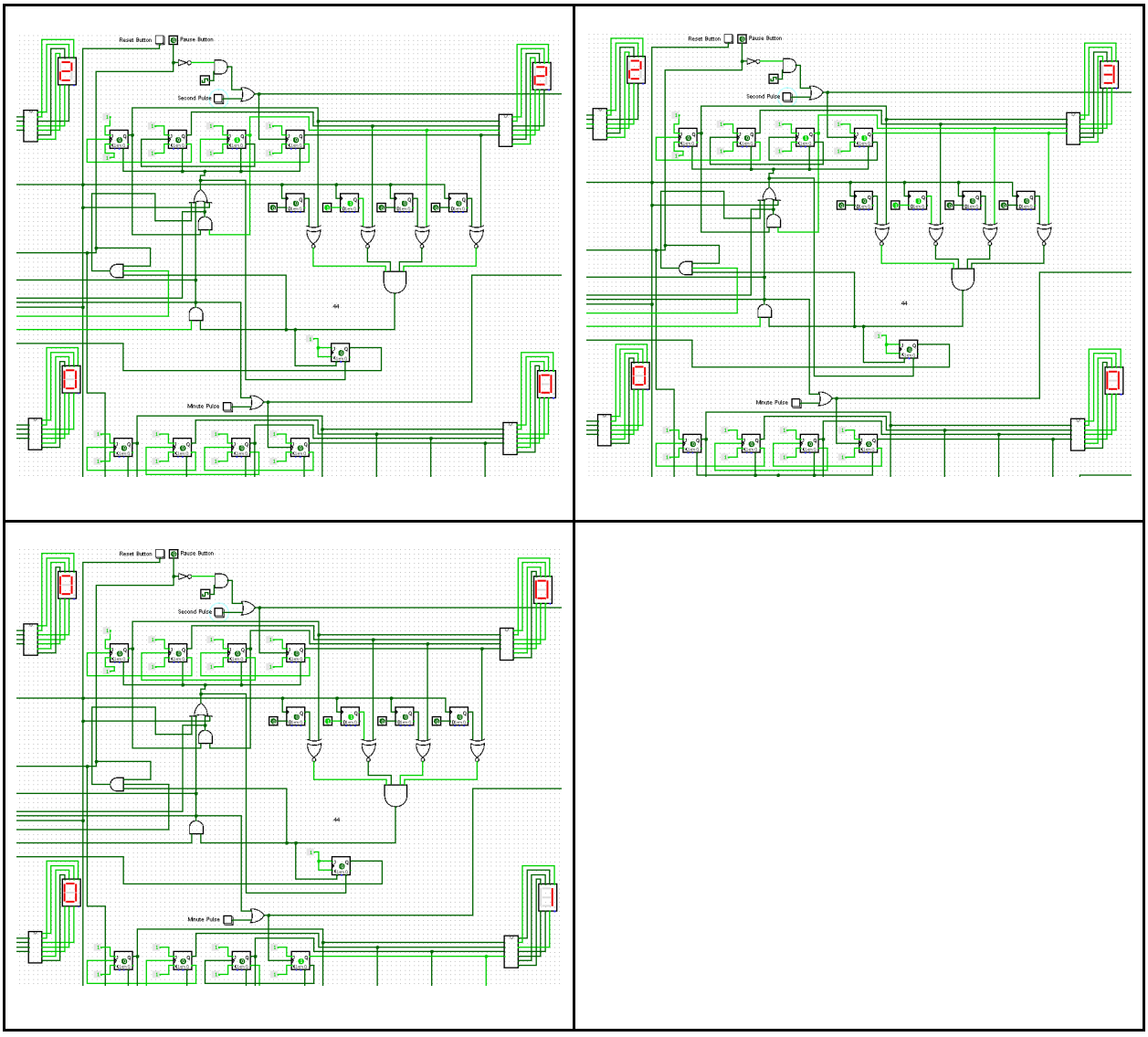


Table 2: Initial Design Minutes and Seconds Section Simulation Result

Table above shows the simulation result of the final design where it resets when the seconds section hits 24 and also results in an increment in the minutes section. The result is as desired and the clock design is working perfectly. While for the minutes section it's the same with the seconds section where the user can also set the limit themselves by using the switches.

Hours Section

7 Hour Clock

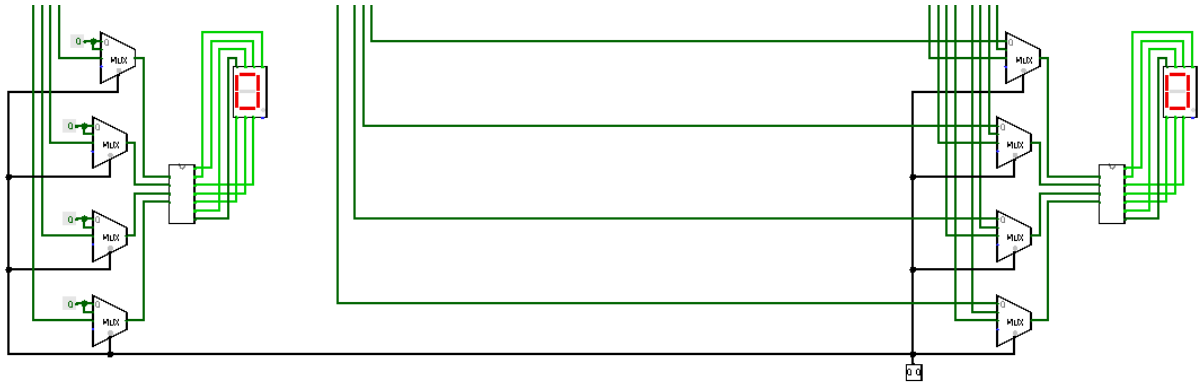
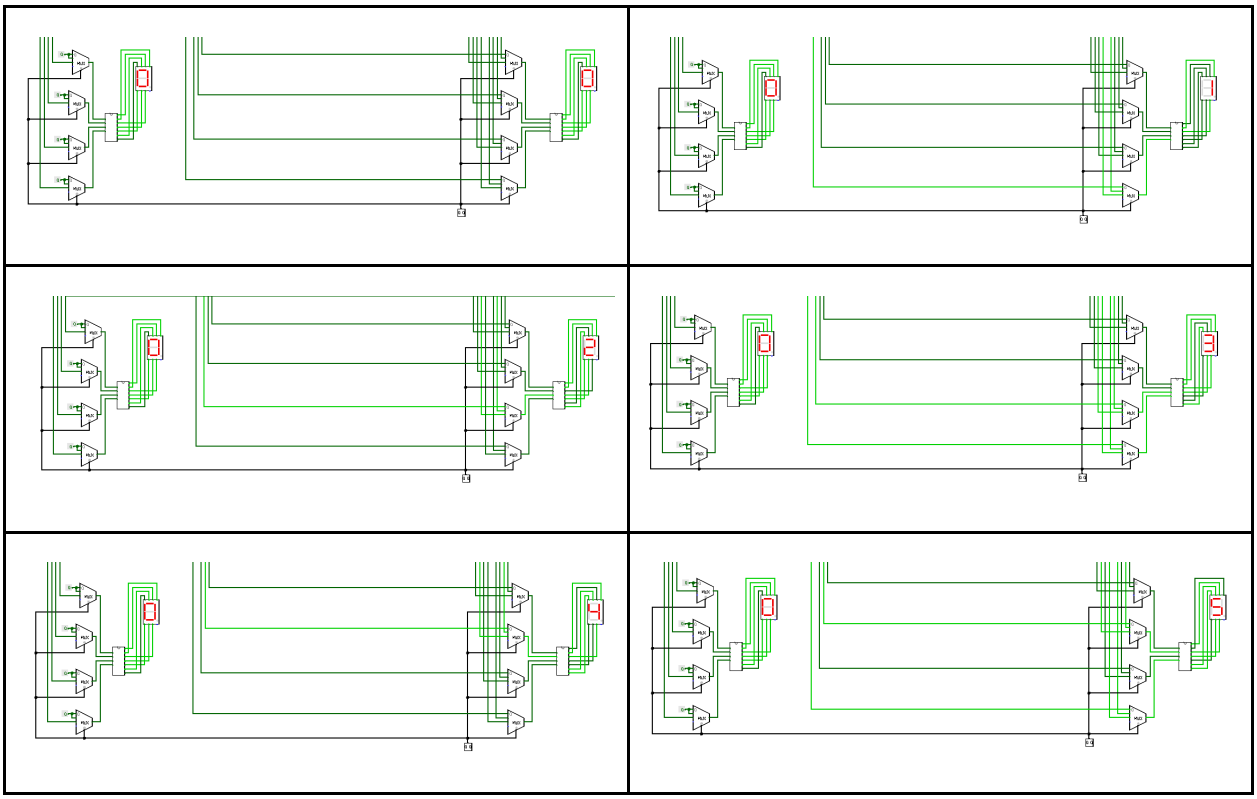


Figure 10: Initial Design 7 Hour Clock Simulation

Diagram above is the clock design of the hour section where the input into the MUX is 00. The input is located at the bottom right corner. When the input is 00 the output will be the first input which is the 7 hour clock.



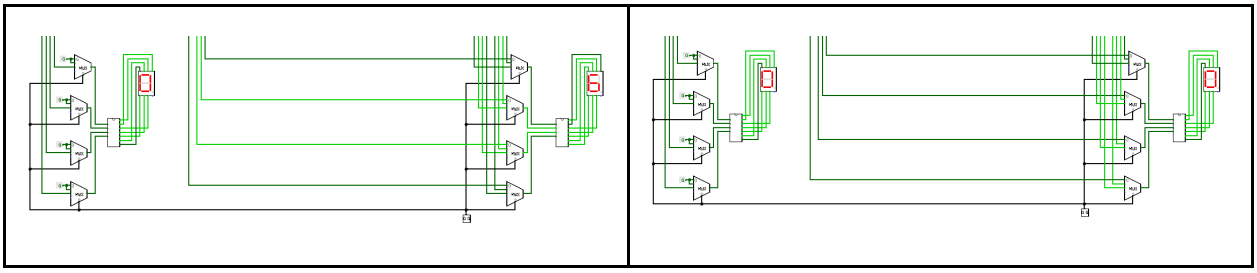


Table 3: Initial Design 7 Hour Clock Simulation Result

The table above shows the simulation of the 7 hour clock. The clock is reset to 0 once it hits 7. The result of the simulation is as desired.

10 Hour Clock

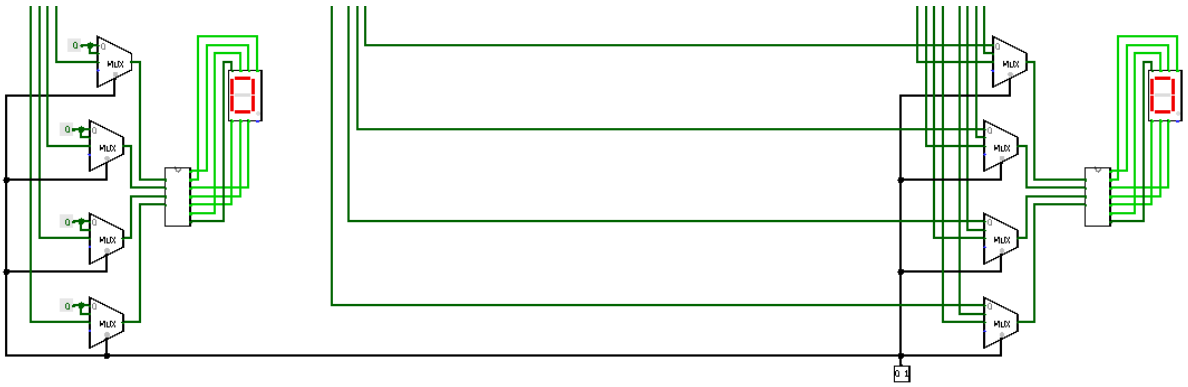
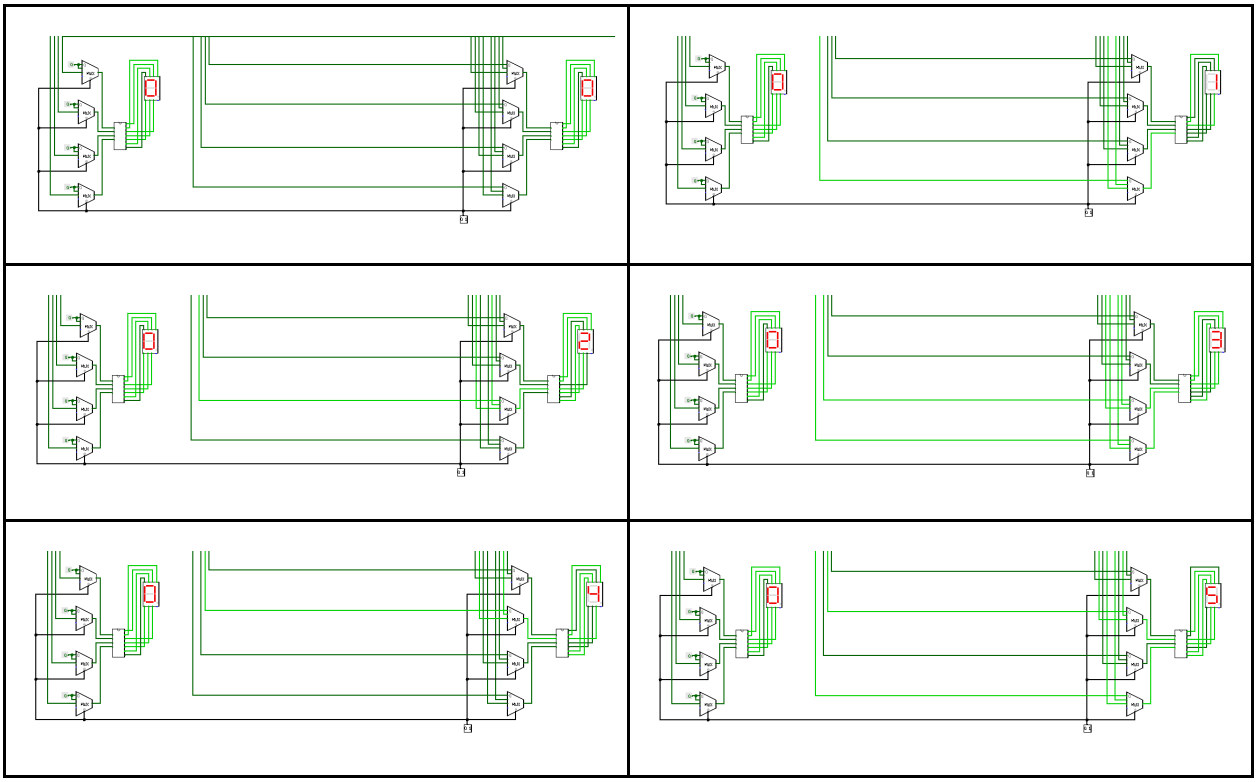


Figure 11: Initial Design 10 Hour Clock Simulation

Diagram above is the clock design of the hour section where the input into the MUX is 01. The input is located at the bottom right corner. When the input is 01 the output will be the second input which is the 10 hour clock.



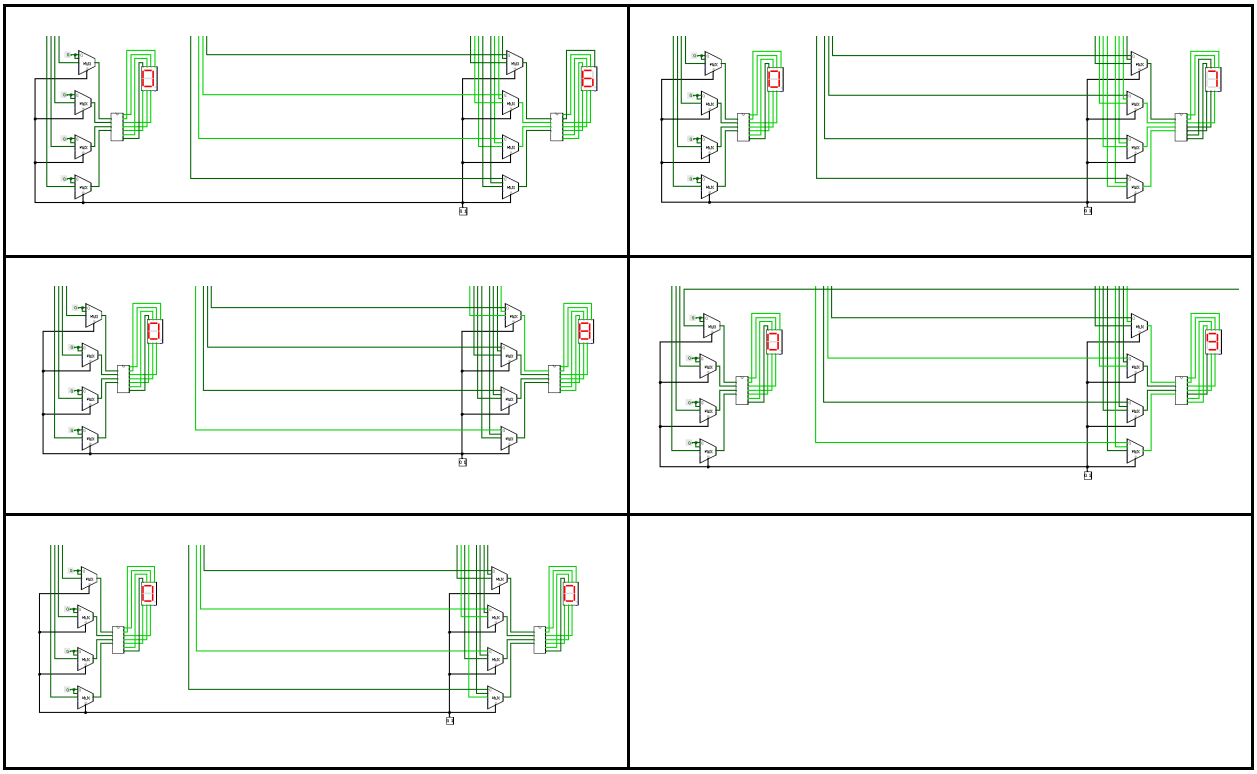


Table 4: Initial Design 10 Hour Clock Simulation Result

The table above shows the simulation of the 10 hour clock. The clock is reset to 0 once it hits 10. The result of the simulation is as desired.

15 Hour Clock

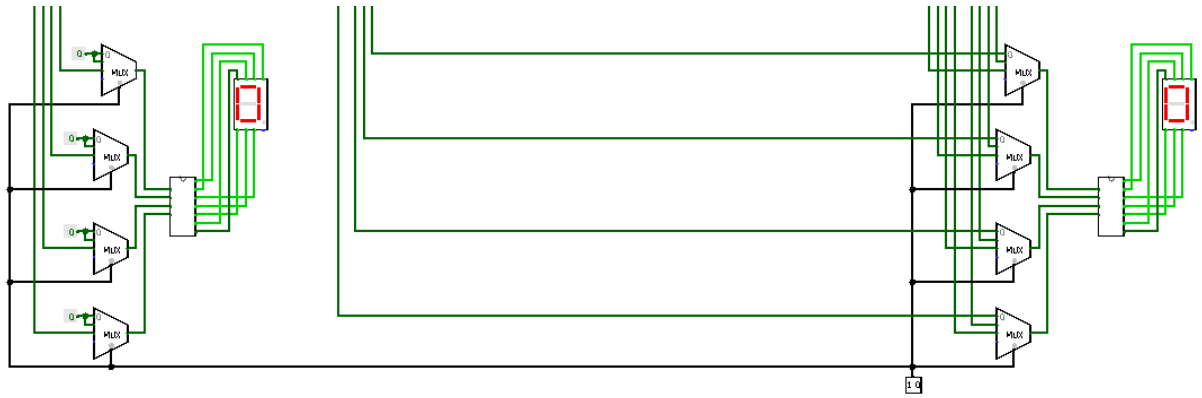
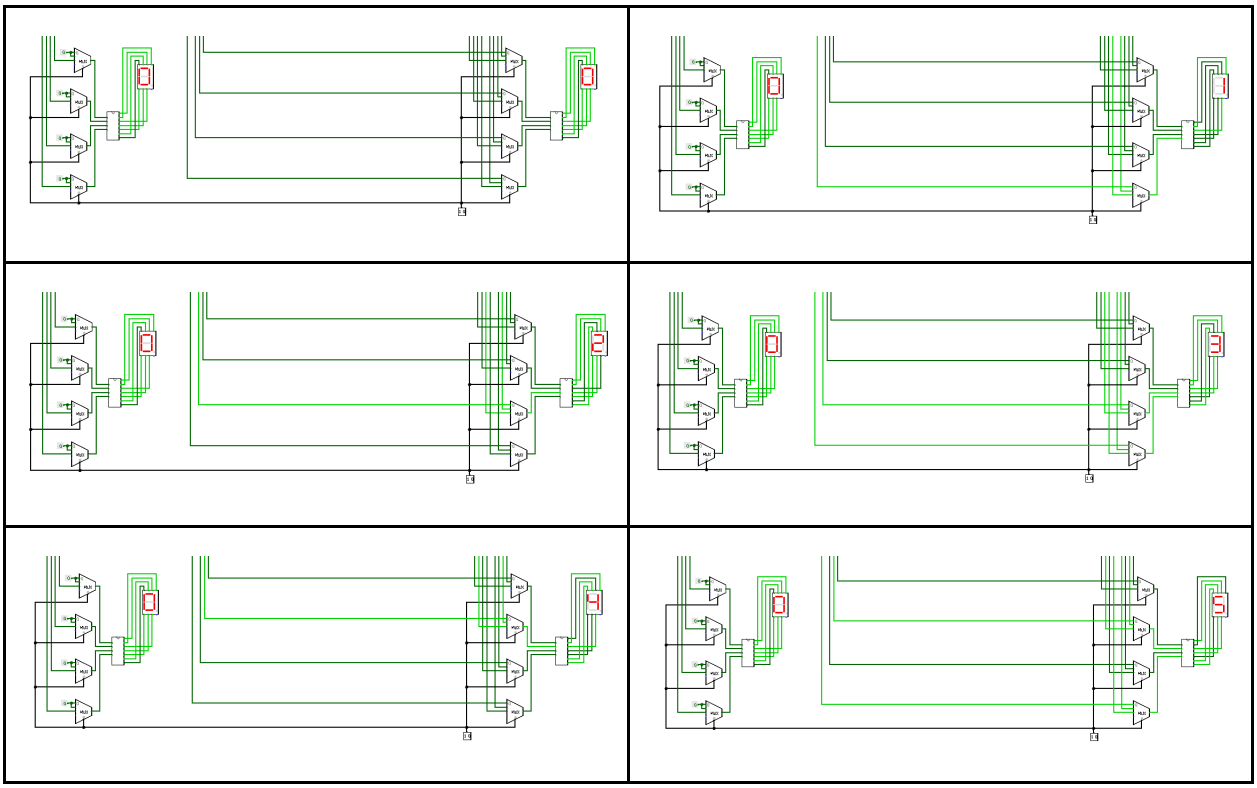


Figure 12: Initial Design 15 Hour Clock Simulation

Diagram above is the clock design of the hour section where the input into the MUX is 10. The input is located at the bottom right corner. When the input is 10 the output will be the second input which is the 15 hour clock.



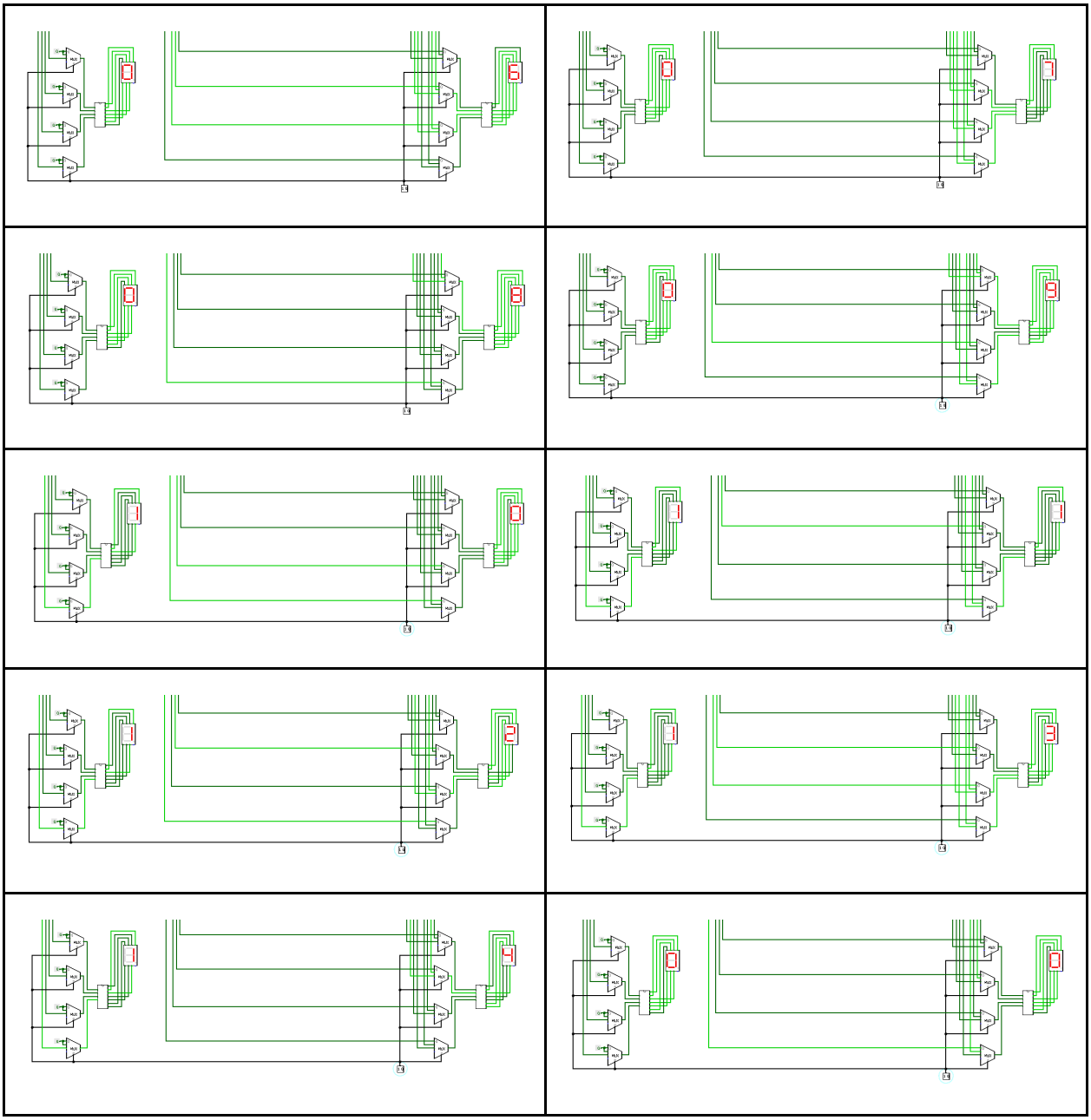


Table 5: Initial Design 15 Hour Clock Simulation Result

The table above shows the simulation of the 15 hour clock. The clock is reset to 0 once it hits 15. The result of the simulation is as desired.

Final Integrated Circuit Design

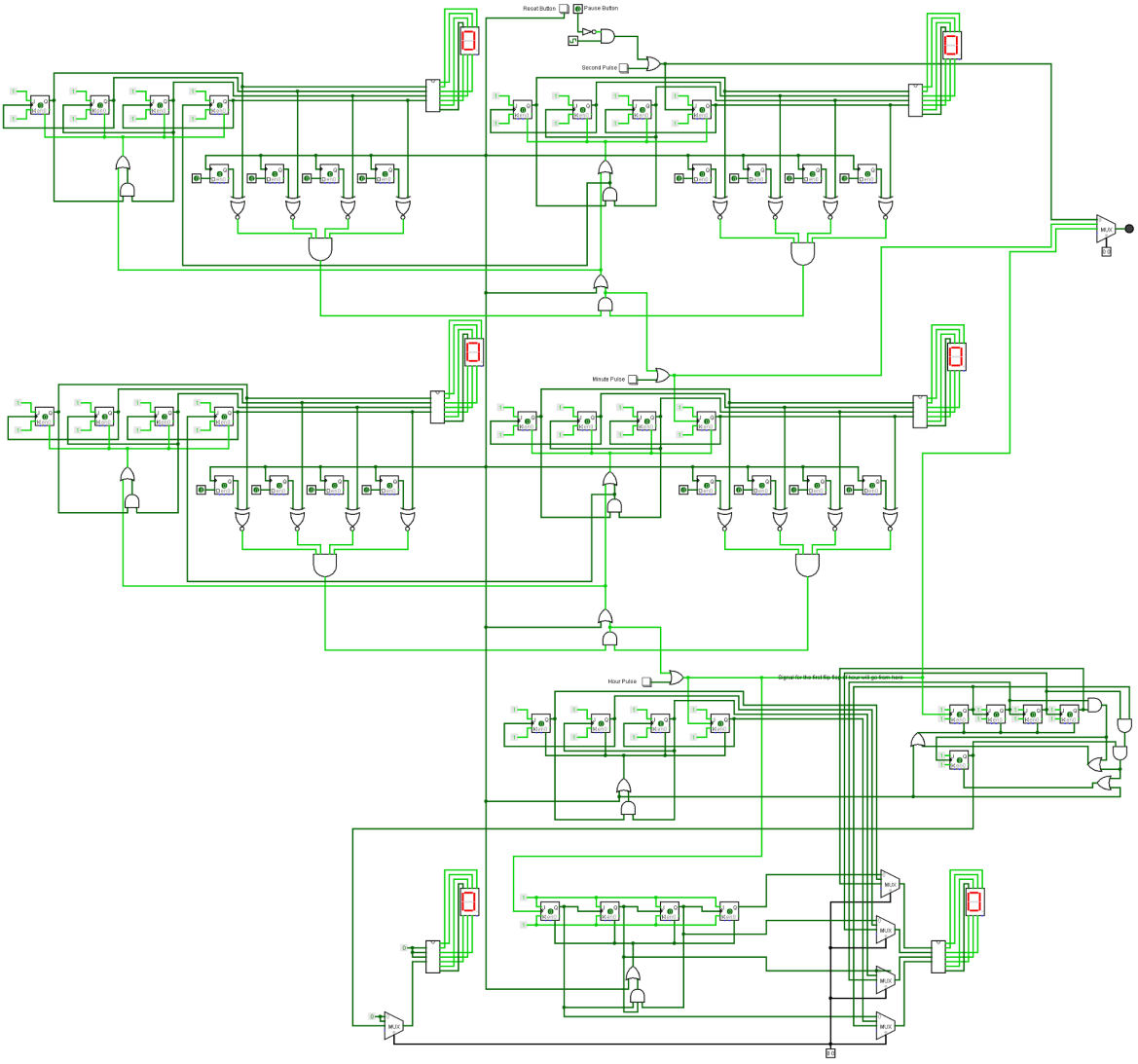


Figure 13: Final Integrated Circuit Design

Figure above is the final integrated design that we decided to work our prototype with. The difference between the final and the first integrated design is that the final design has no time editing feature. The reason for removing the feature is because the whole circuit will be too hard to build in real life. Hence, the final design will only have 1 button for each of the sections which are the hours, minutes and seconds. Which is made up of 3 buttons to edit the time instead of 6. The logic is much less complex compared with the first integrated design. Besides that there is also some reduction of JK flip flops and mux in the design which further reduces the complexity but the logic still stays the same.

Other than that, other features still stay the same where it can let the user decide on their own how many seconds in a minute, how many minutes in an hour and can switch freely between 15, 9 and 7 hours clock. The sound notification system is also the same.

Final Simulation Result

Minutes and Seconds Section

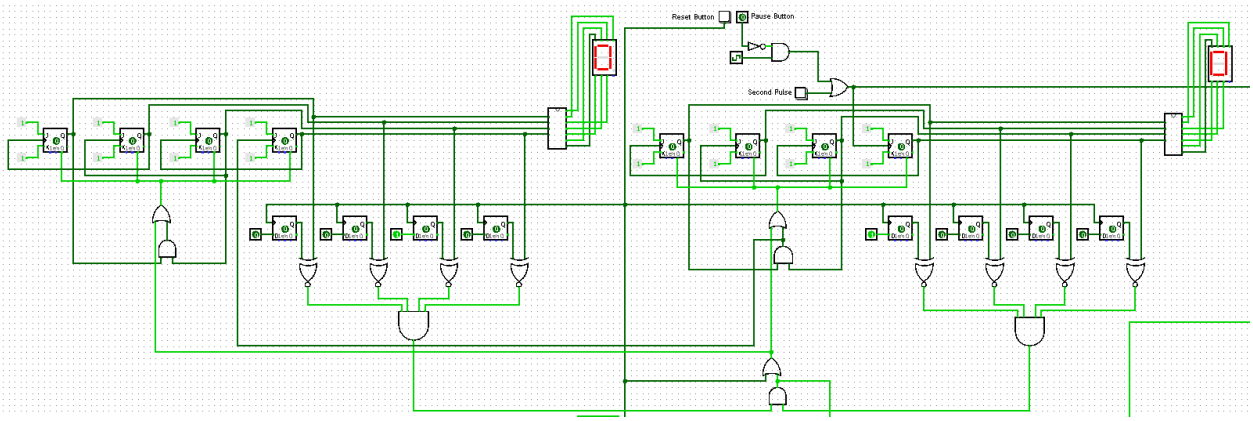


Figure 14: Final Design Minutes and Seconds Section Simulation 1

Diagram above is showing the switch that is used to control the limit of seconds is set to 1000 in the first digit and also 0010 in the second digit. Hence this means that there will be 28 seconds in a minute and the seconds section will reset once it hits 28 seconds and add 1 into the minutes section.

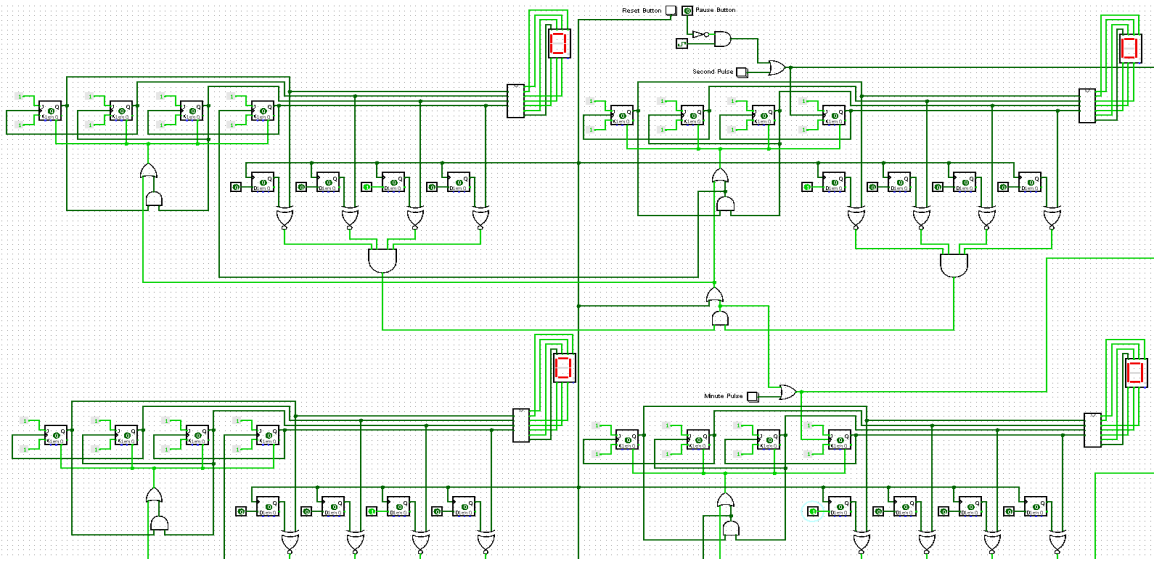
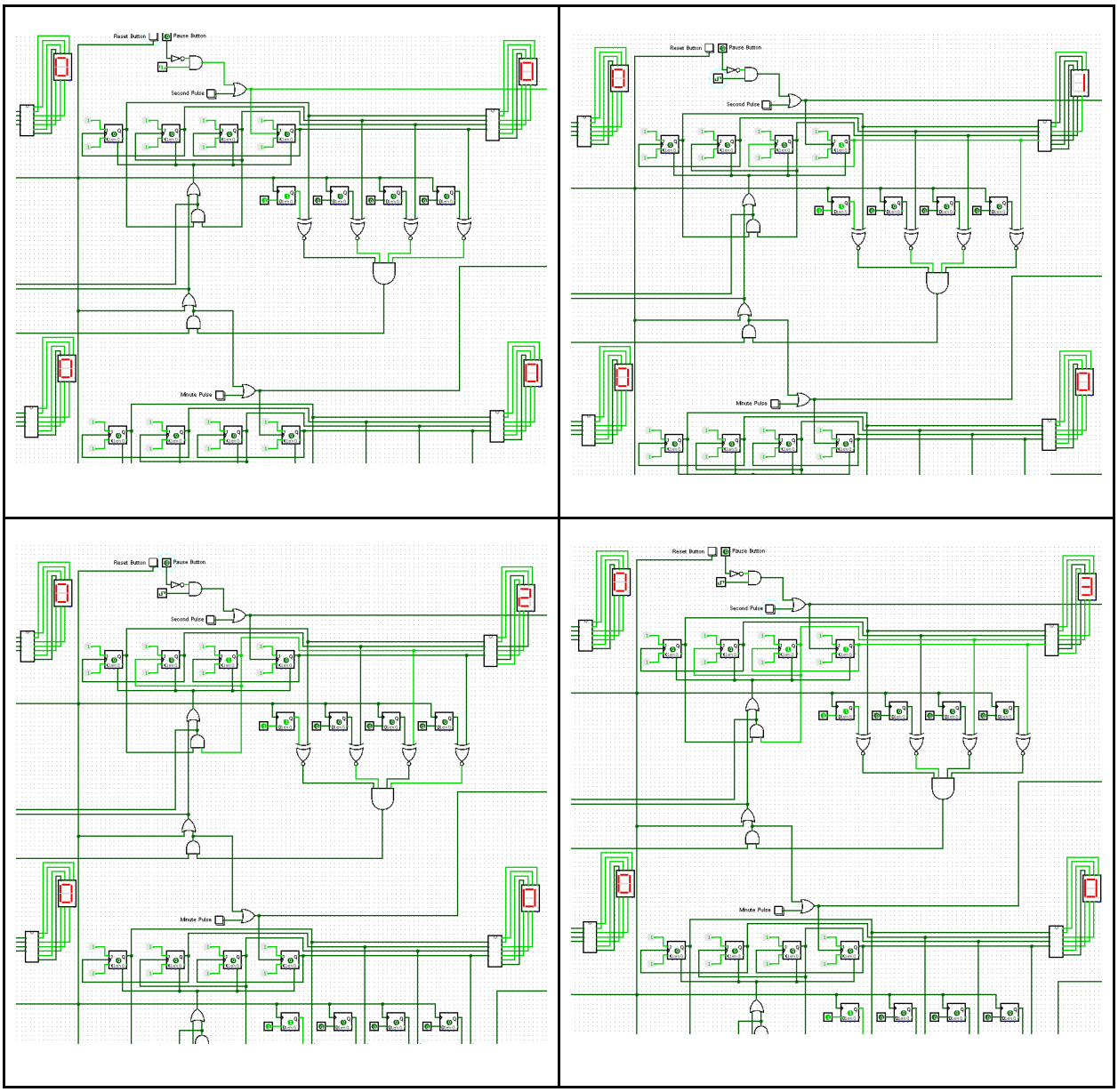
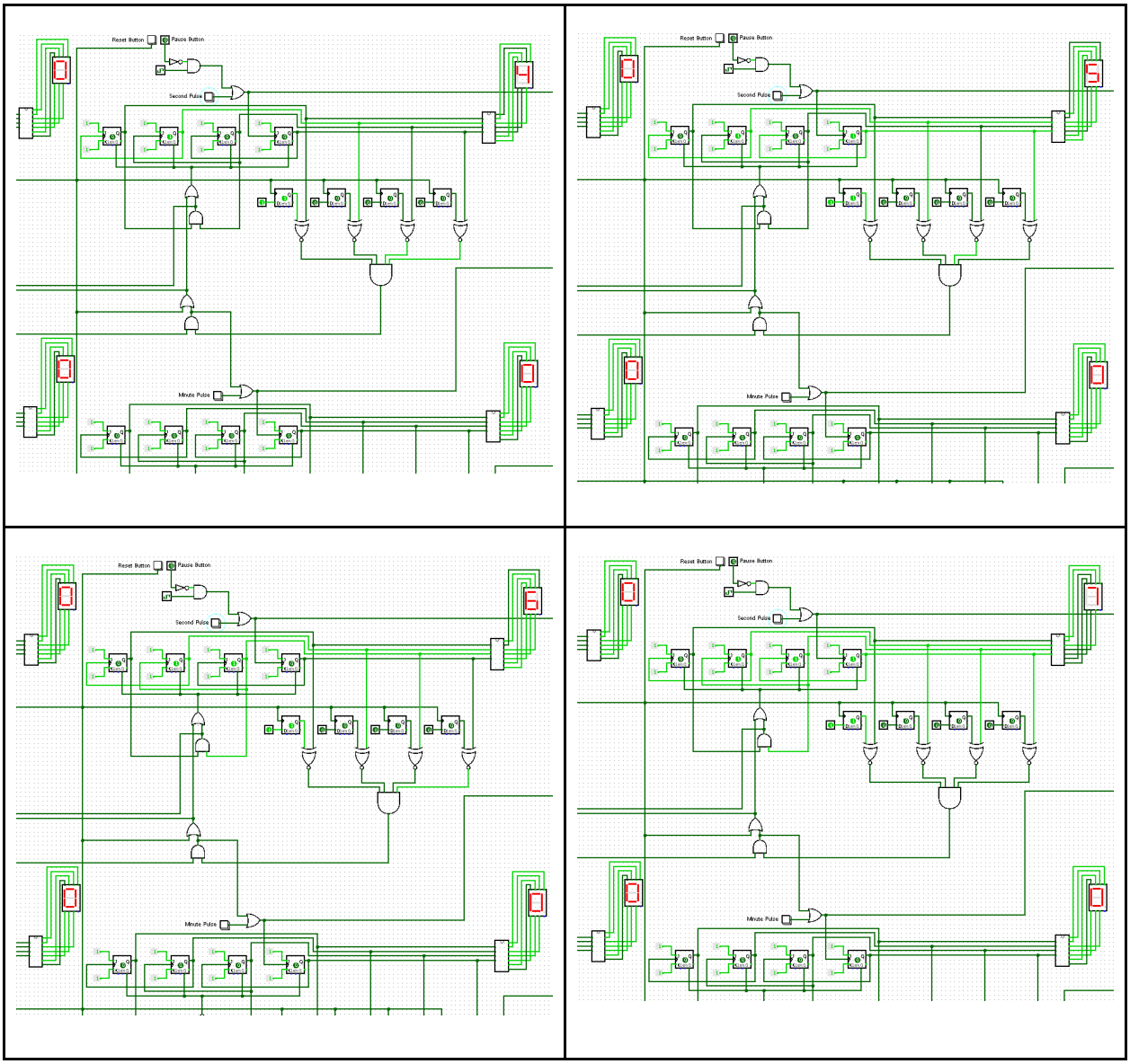
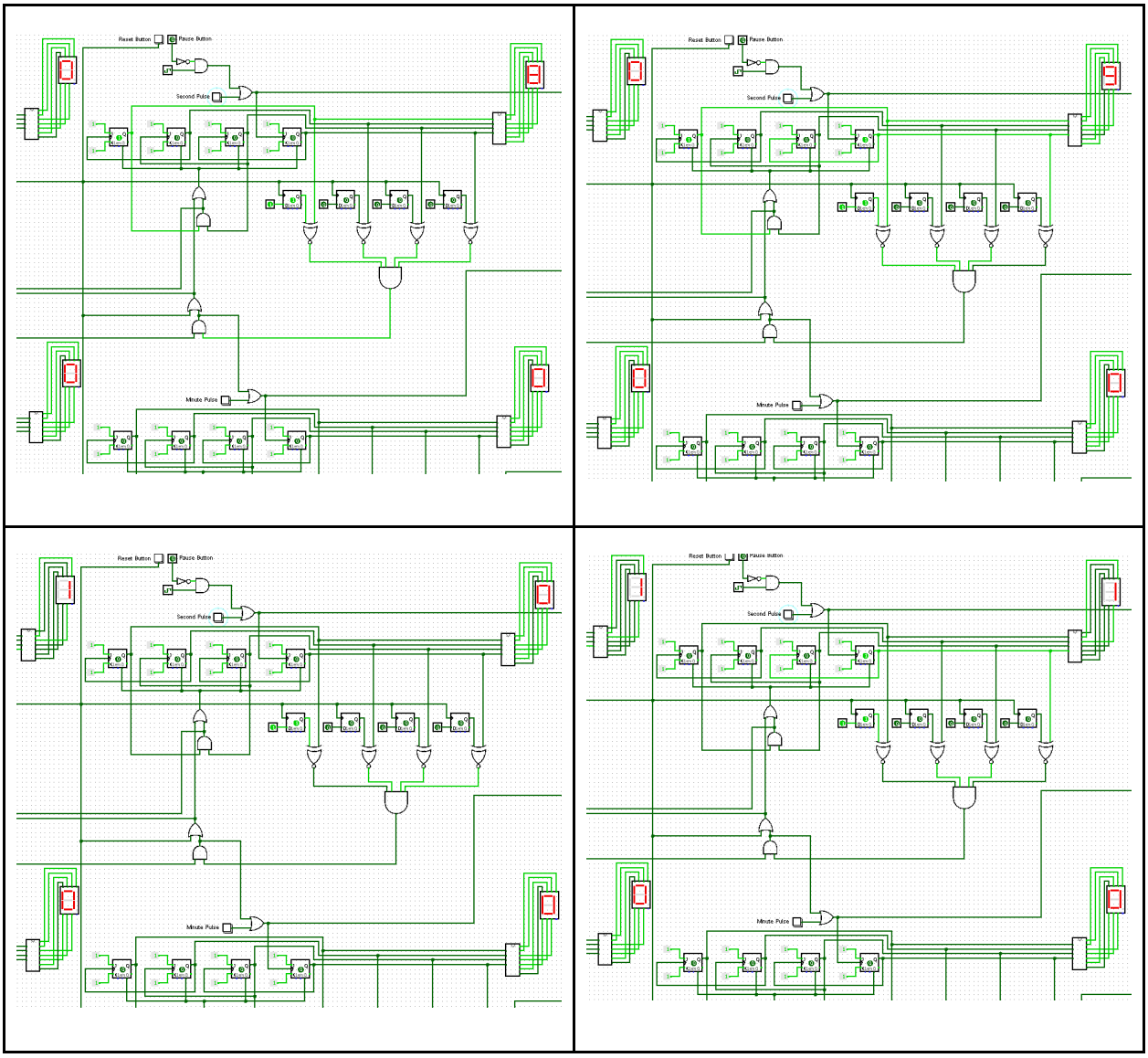


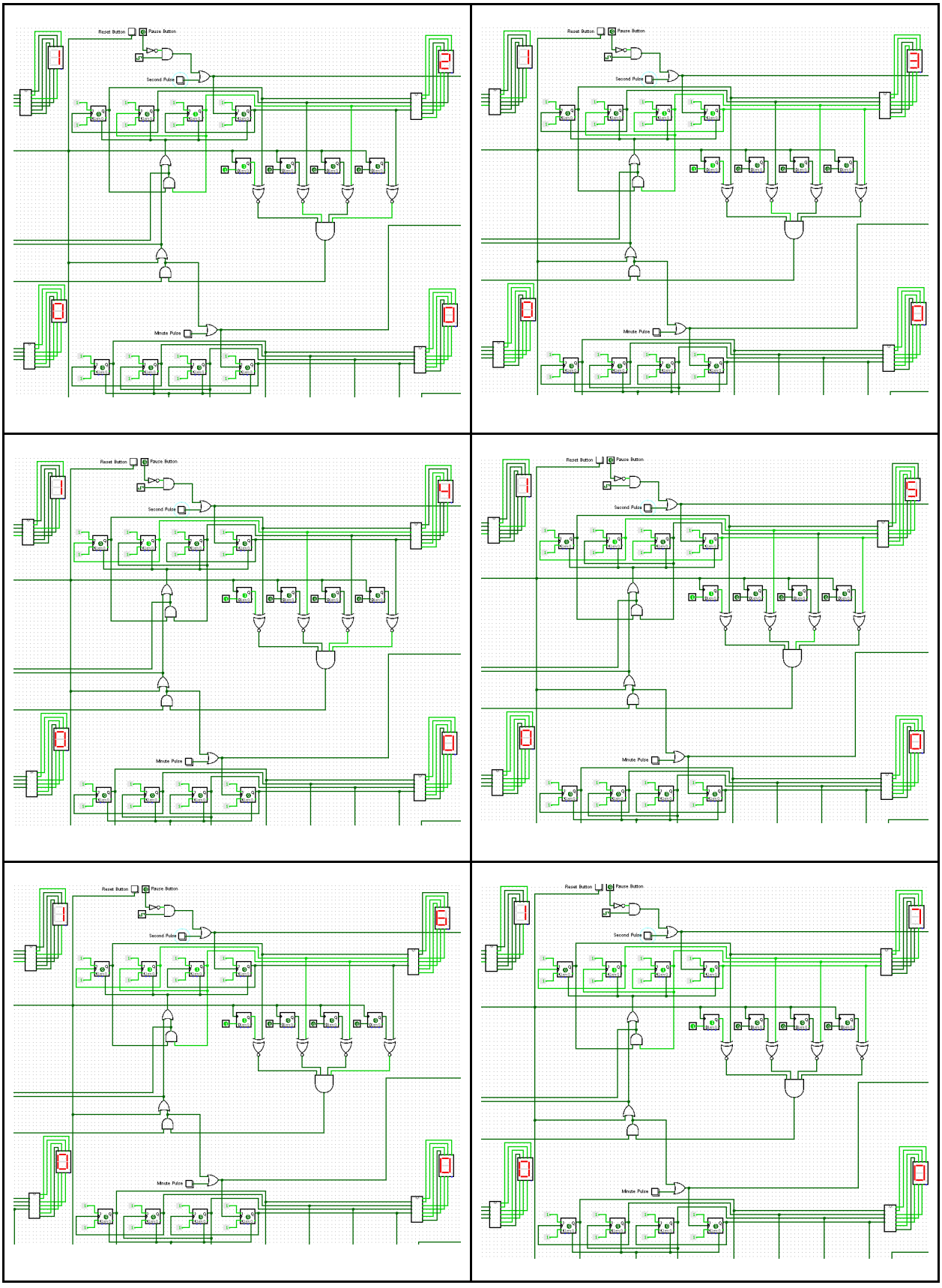
Figure 15: Final Design Minutes and Seconds Section Simulation 2

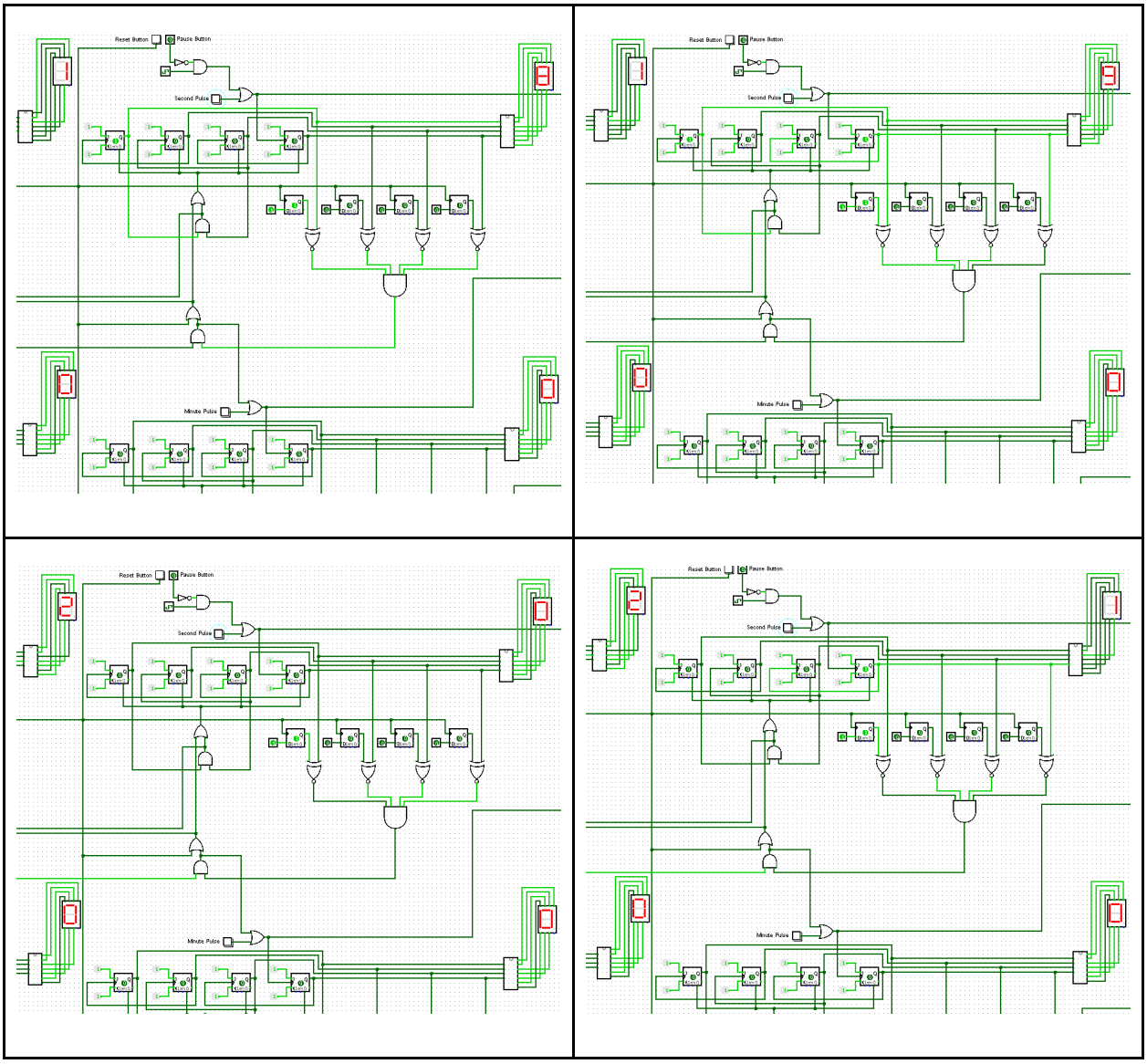
Diagram above shows the initial condition of the seconds and minutes section before running the simulation.

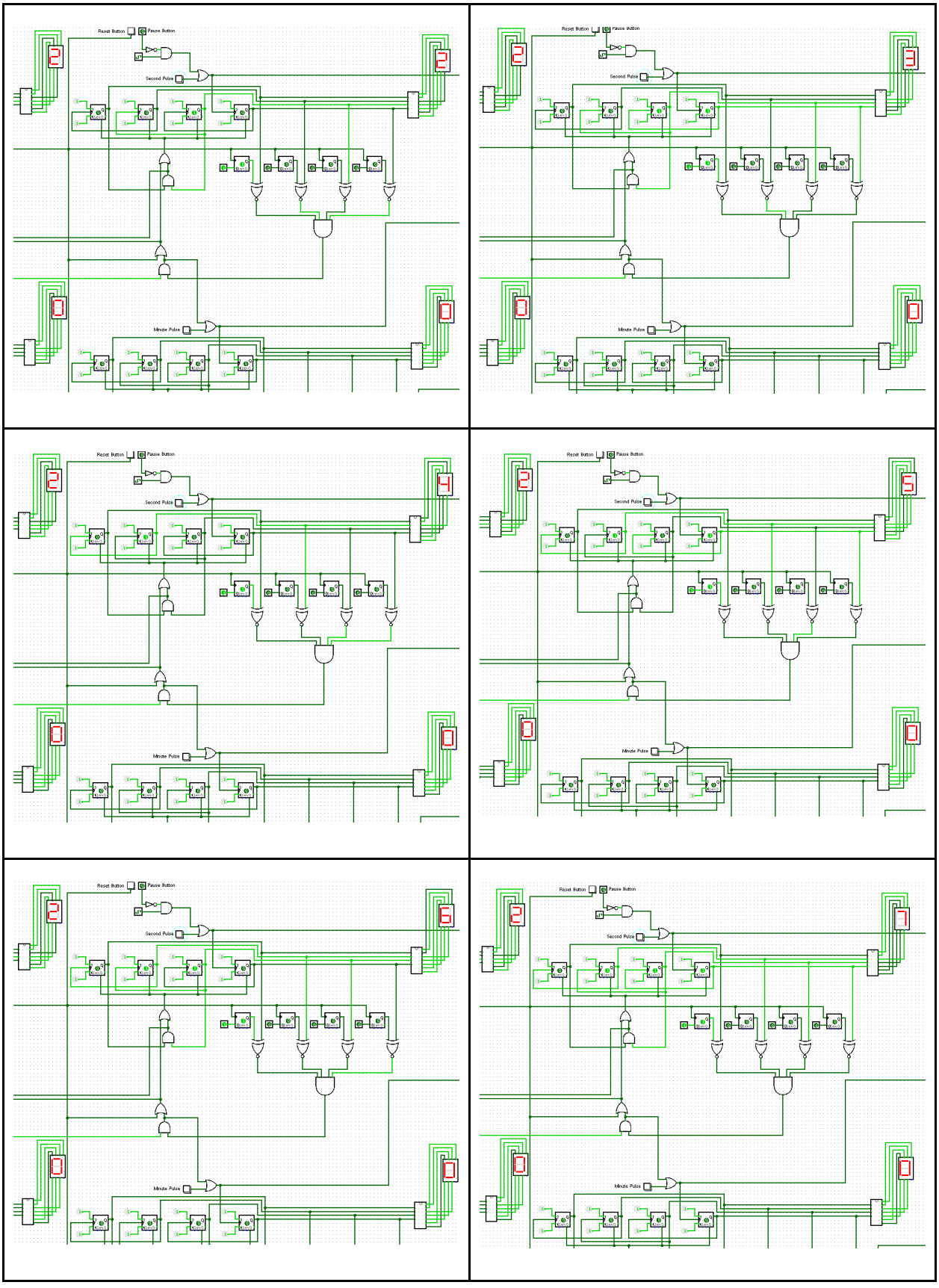

Reset Button
Pause Button
Second Pulse
Minute Pulse


Reset Button
Pause Button
Second Pulse
Minute Pulse


Reset Button
Pause Button
Second Pulse
Minute Pulse


Reset Button
Pause Button
Second Pulse
Minute Pulse


Reset Button
Pause Button
Second Pulse
Minute Pulse


Reset Button
Pause Button
Second Pulse
Minute Pulse

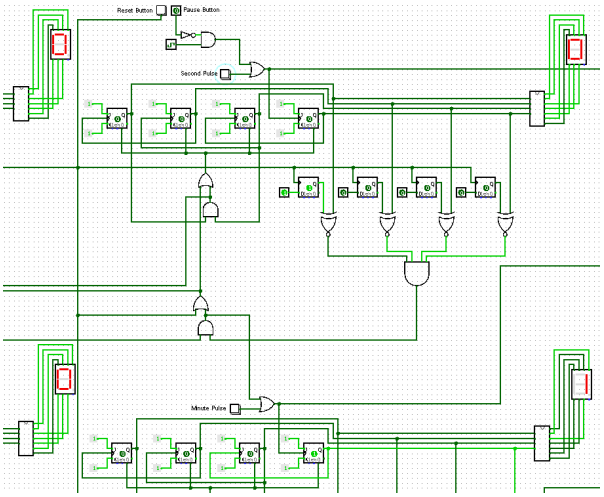


Table 6: Final Design Minutes and Seconds Section Simulation Result

Table above shows the simulation result of the final design where it resets when the seconds section hits 28 and also results in an increment in the minutes section. The result is as desired and the clock design is working perfectly. While for the minutes section it's the same with the seconds section where the user can also set the limit themselves by using the switches.

Hours Section

7 Hour Clock

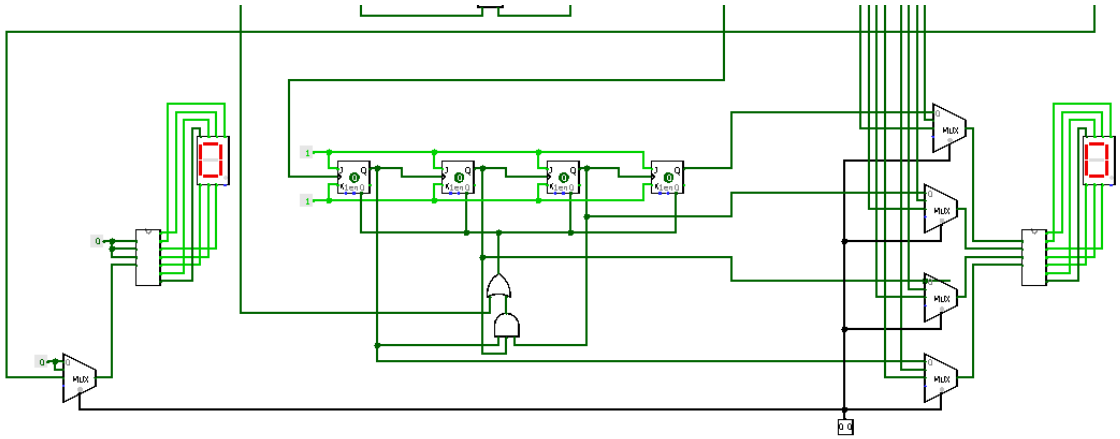
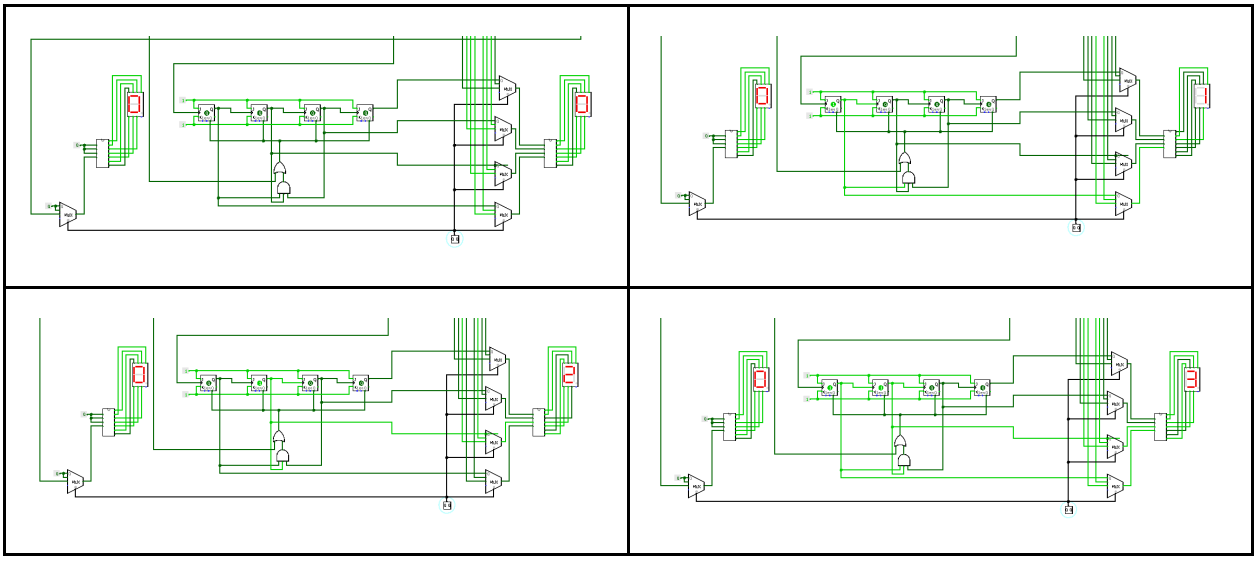


Figure 16: Final Design 7 Hour Clock Simulation

Diagram above is the clock design of the hour section where the input into the MUX is 00. The input is located at the bottom right corner. When the input is 00 the output will be the first input which is the 7 hour clock.



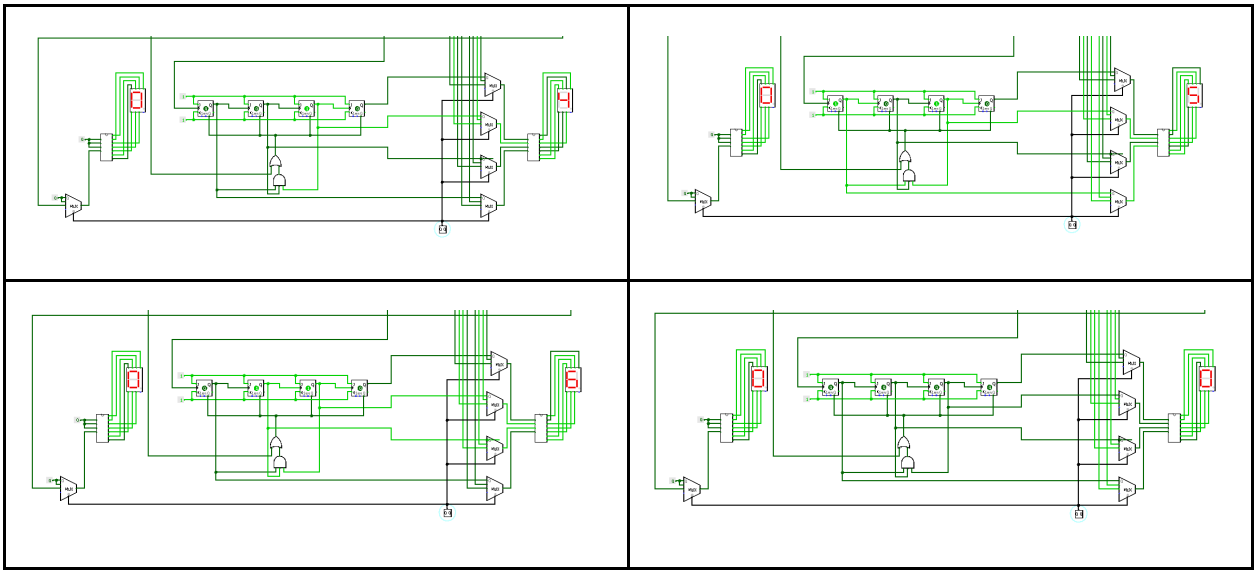


Table 7: Final Design 7 Hour Clock Simulation Result

The table above shows the simulation of the 7 hour clock. The clock is reset to 0 once it hits 7. The result of the simulation is as desired.

10 Hour Clock

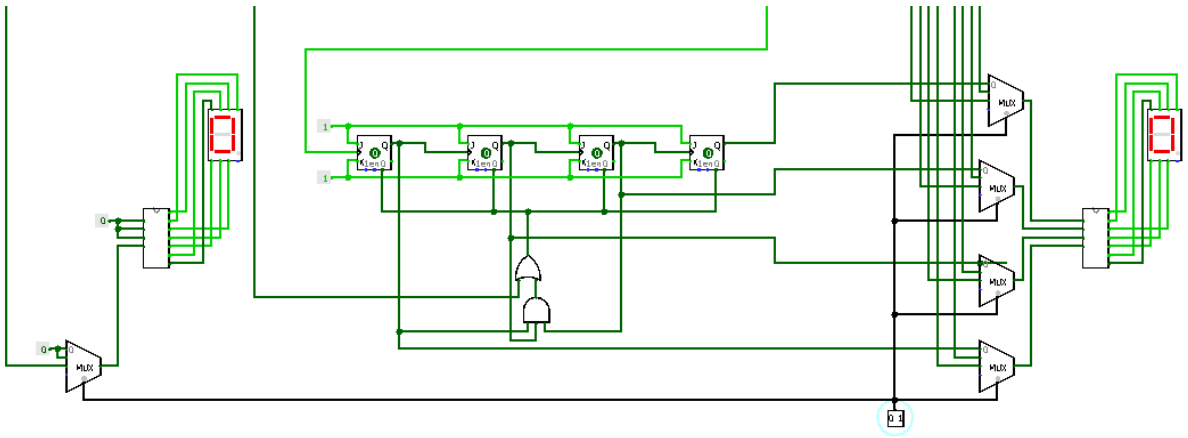
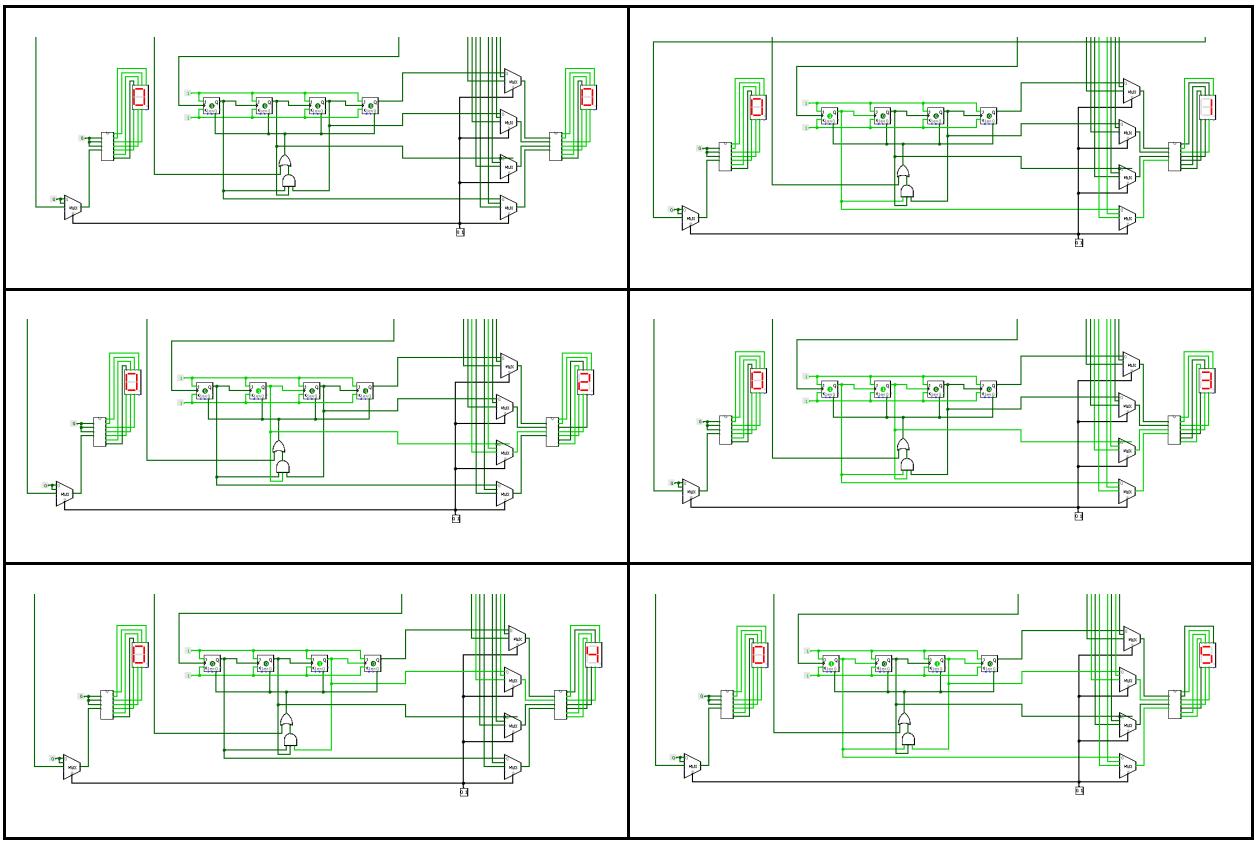


Figure 17: Final Design 10 Hour Clock Simulation

Diagram above is the clock design of the hour section where the input into the MUX is 01. The input is located at the bottom right corner. When the input is 01 the output will be the second input which is the 10 hour clock.



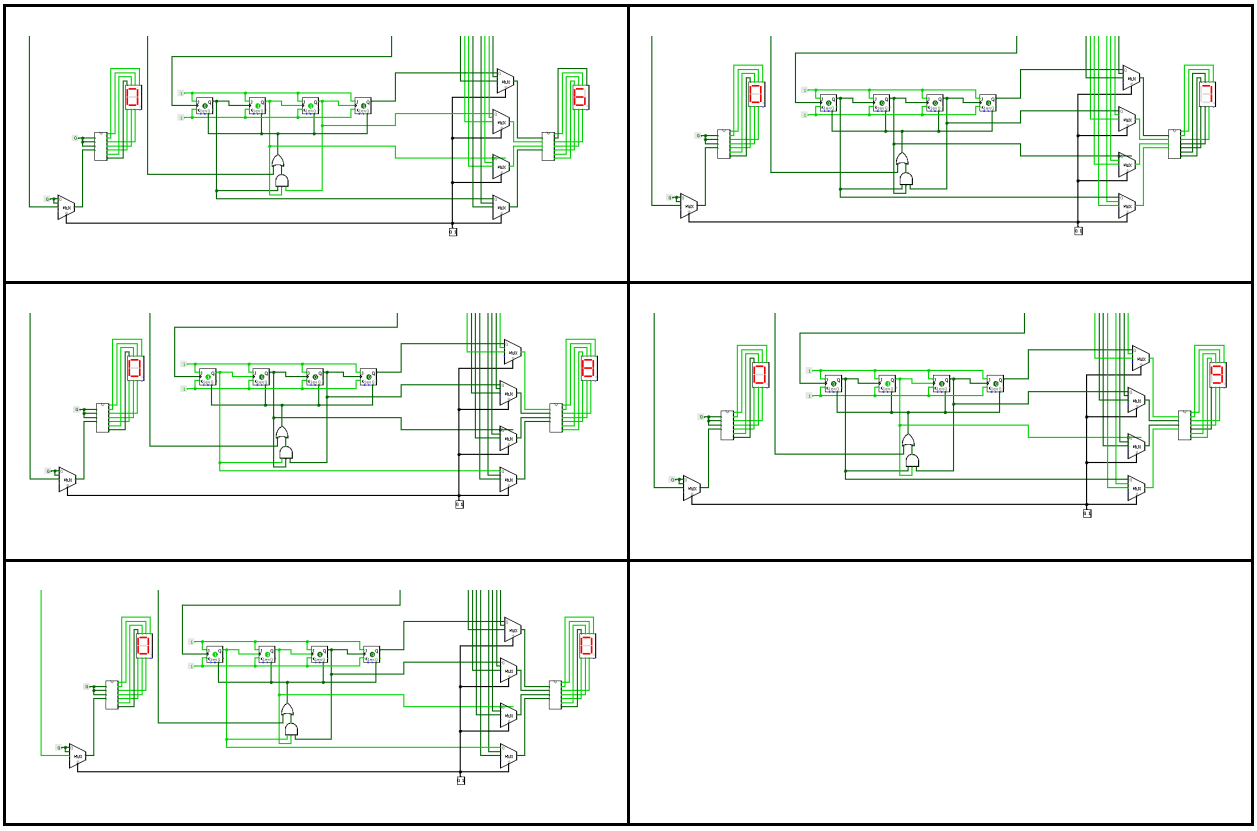


Table 8: Final Design 10 Hour Clock Simulation Result

The table above shows the simulation of the 10 hour clock. The clock is reset to 0 once it hits 10. The result of the simulation is as desired.

15 Hour Clock

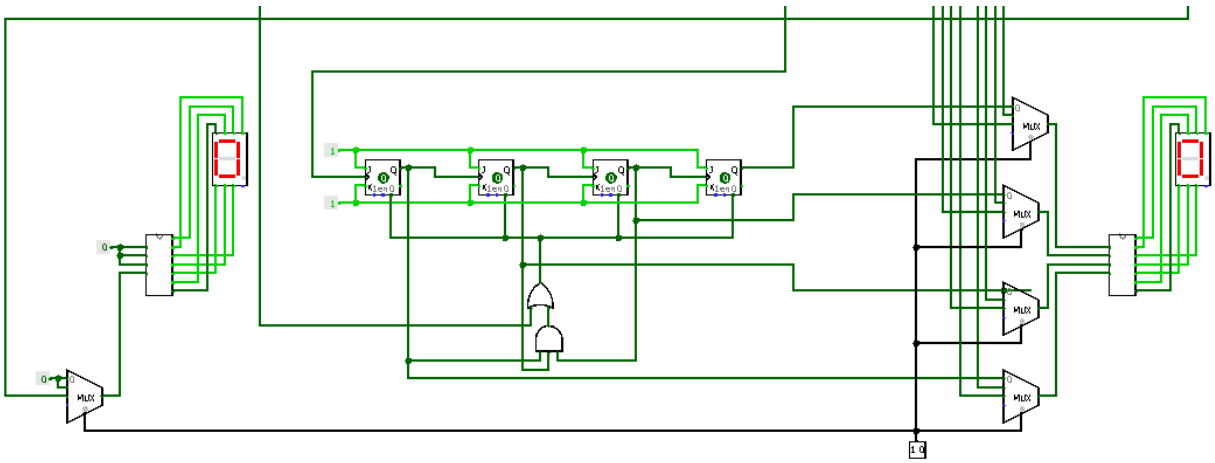
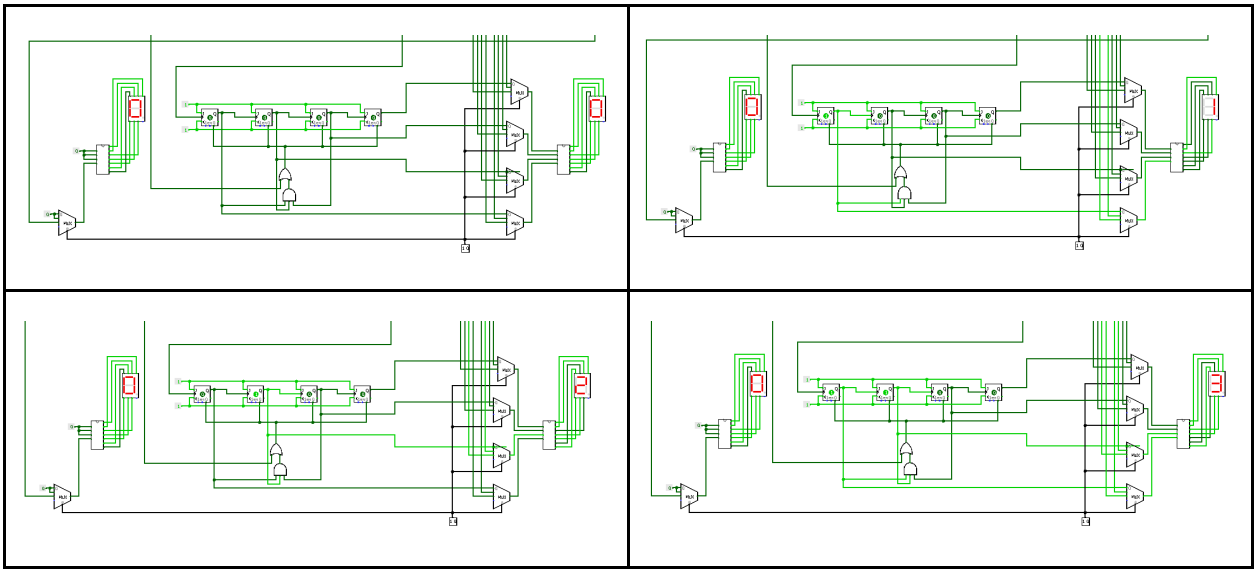


Figure 18: Final Design 15 Hour Clock Simulation

Diagram above is the clock design of the hour section where the input into the MUX is 10. The input is located at the bottom right corner. When the input is 10 the output will be the third input which is the 15 hour clock.



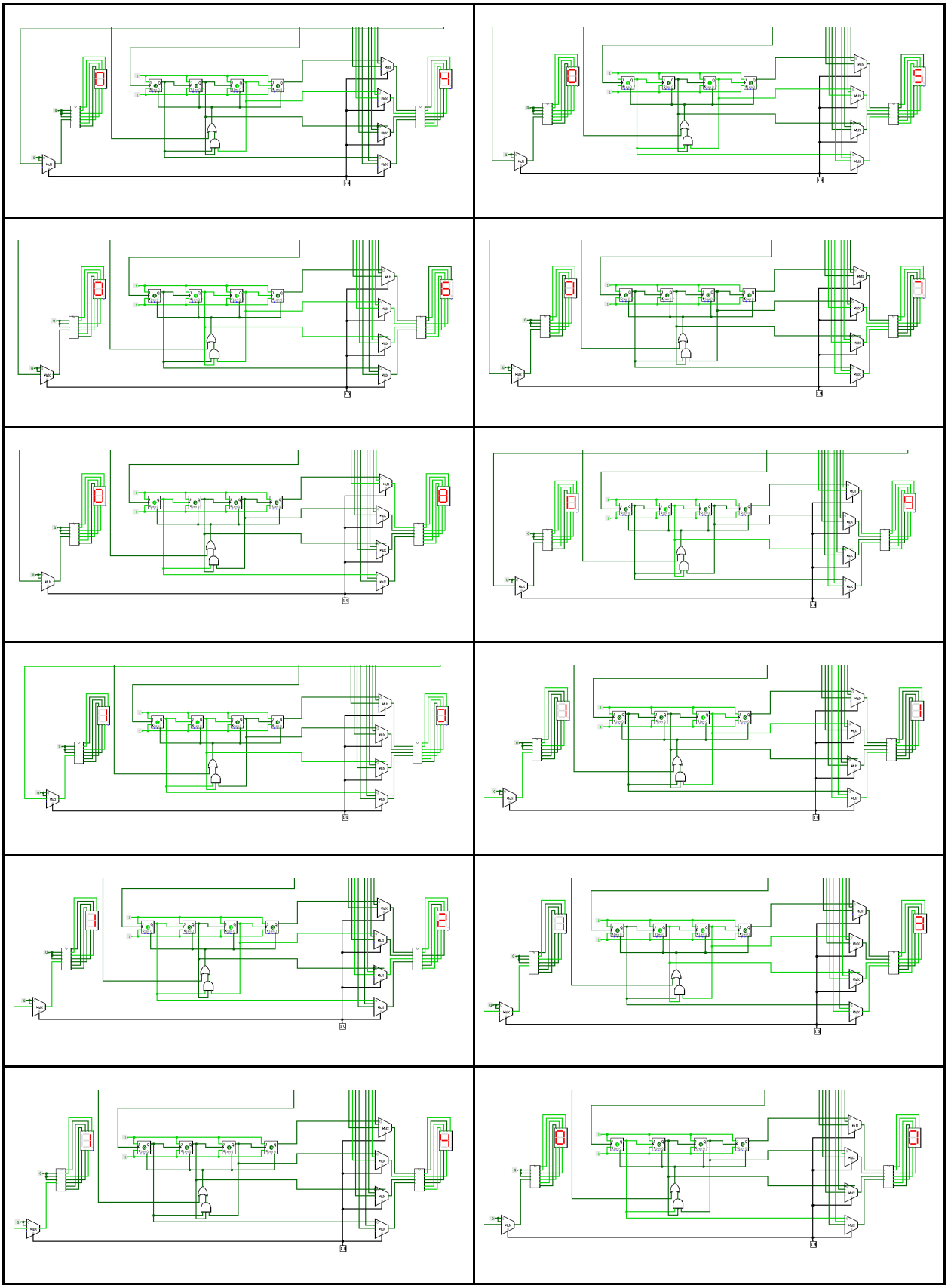


Table 9: Final Design 10 Hour Clock Simulation Result

The table above shows the simulation of the 15 hour clock. The clock is reset to 0 once it hits 15. The result of the simulation is as desired.

Discussion

Some of the features that were implemented were only partially implemented. For example, the setting the time feature is only partially implemented in final integrated circuit design. There were initial designs that included the full implementation of the editing time feature for the clock with the clock, however, the complexity of the circuit grew exponentially with the addition of editing feature mainly due to the fact that the minutes and seconds were not fixed and can be changed by the user. Due to the rise in complexity, the number of components that we had to use to build the prototype skyrocketed. Due to our limited resources, complexity of the design, the expensive cost of integrated circuits, logic gates, wires, breadboards and even buttons, we decided to not proceed with the initial design. However, since the features in the initial integrated clock design works flawlessly, we decided to keep it so we can further improve the clock prototype by implementing the entire feature instead of partially implementing it.

Although our integrated clock design works exceptionally well, there are still some limitations to our design. One of the limitations of our design is that the user can set the individual limit of each digit of the clock to be higher than 9. The way the user sets the limit for the clock is by toggling some switches, so the combined 4 binary bits of the switches translate to a decimal value that the user wants. For example, if the user wants the limit of the seconds of the clock to be 99, both digits limit needs to be set to 9, therefore, the binary version of the value 9 would be 1001. This would be fruitful as the clock will function perfectly. However, since there's 4 switches, the user can input up to 4 bits, which means the user can input up to 15. Therefore, instead of entering 1001, the user can enter 1111, which is greater than 9, and can't be properly decoded by the binary to decimal decoder and hence, the display of the clock would show values that we do not expect.

Conclusion

In conclusion, the objectives of the group assignment have been met as we've successfully studied three distinct clock designs which display time in different formats. The different format includes the clock with 15 hours, 10 hours and 7 hours. The user can select between the different display modes by adjusting the input values. The input values will be fed to a control unit which is the 4 to 1 mux where there would be 4 inputs into the mux and 1 output will be selected to be displayed to the user. Therefore, the user can choose to view between three different outputs.

Another objective that was met is the combination of the extra features that were designed by each group member so that the clock design will be the best design that we can come up with. We've worked as a team to design the best clock there is by merging different features from each group member so that the final outcome of the clock's design is completely unique and has many additional features that would impact real world usage. This subsequently made the design of our integrated circuit extremely user friendly and appealing.

The findings of the assignment are that our integrated circuit works as intended, all the additional features work well with one another. The results observed from the circuit matches with the results that we expect the integrated circuit to output. For example, the reset feature works when the reset button is pressed, which sets the values of all the counters back to 0. The pause feature also works as intended as when the switch button is turned on, the digits on the clock remain frozen. The clocks' minute and second can also be altered to any value from 0 to 99 which works as intended. The clock can be set to any time according to the user if they pressed the appropriate button. The user can also set the interval in which the clock will buzz, which acts as an alarm. These features are common in modern digital clocks and by implementing it into our integrated circuit, we think that it makes it closer to reality and more of a pleasure to use.

The assignment has led us to think critically and out of the box to create additional features. The implication of the assignment is that it is possible to add any features to any circuit design with the right understanding of how different components work as even the most complex features can be broken down into a simple truth table which can then be converted into a logic expression with the help of a Karnaugh map.

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