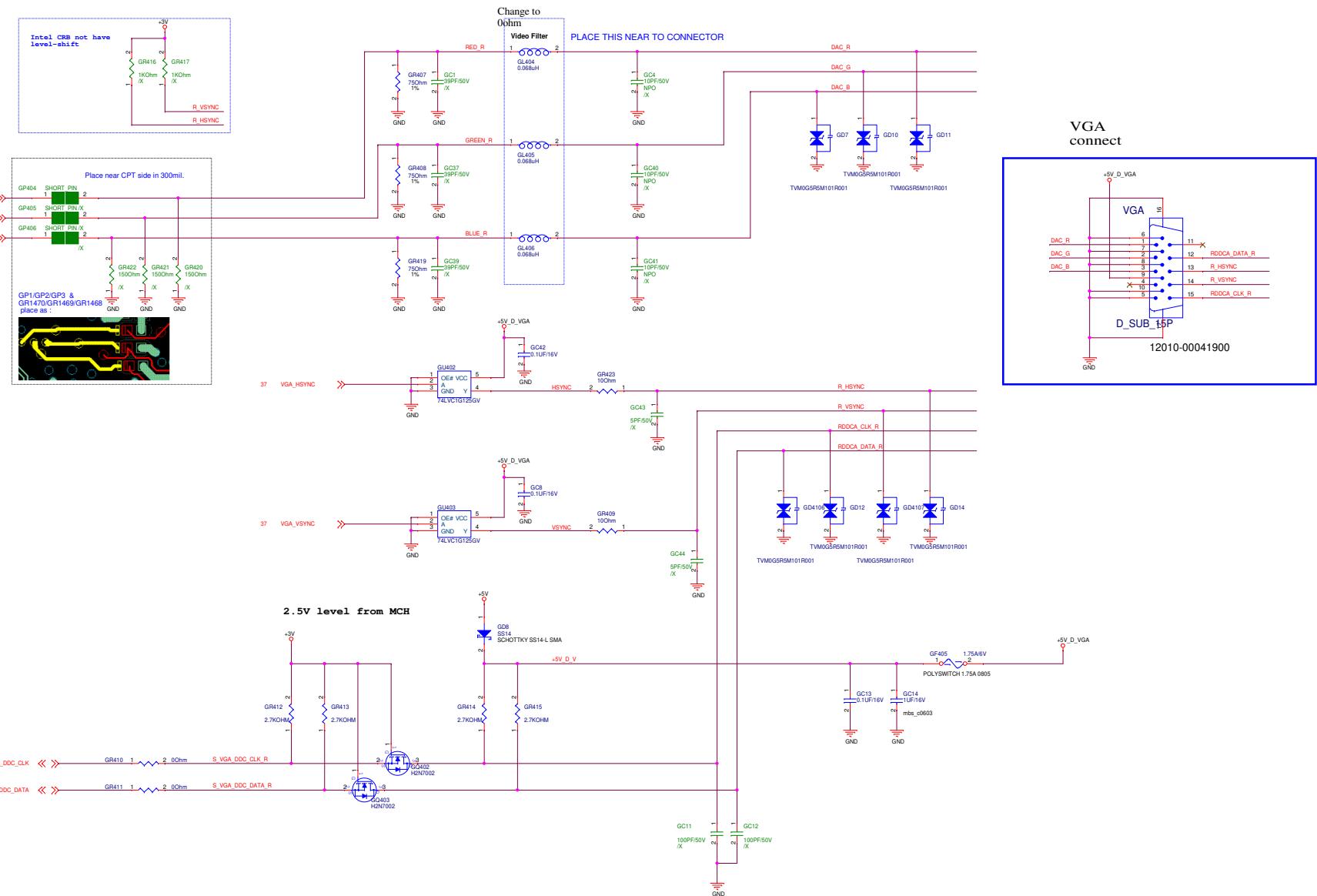
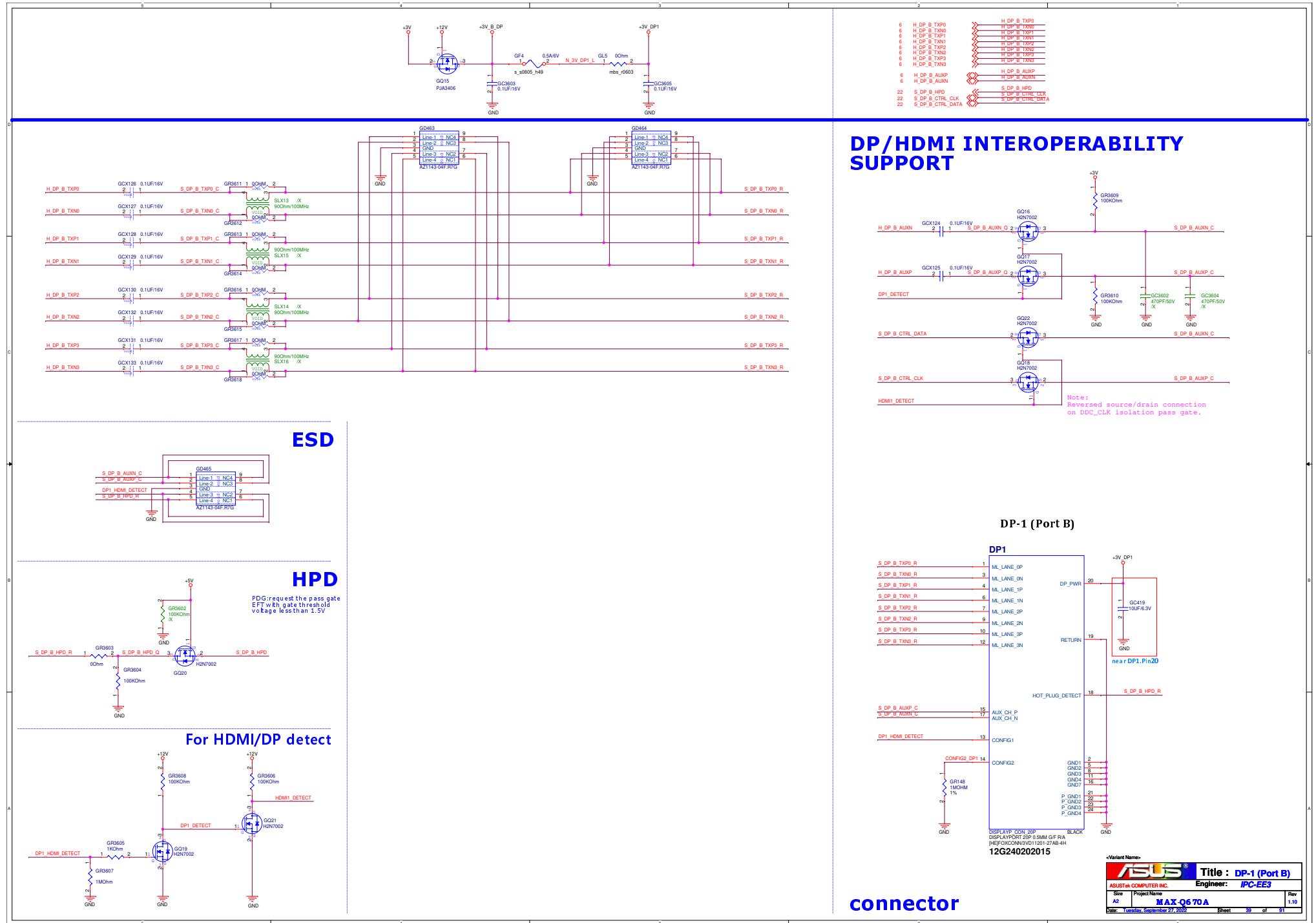
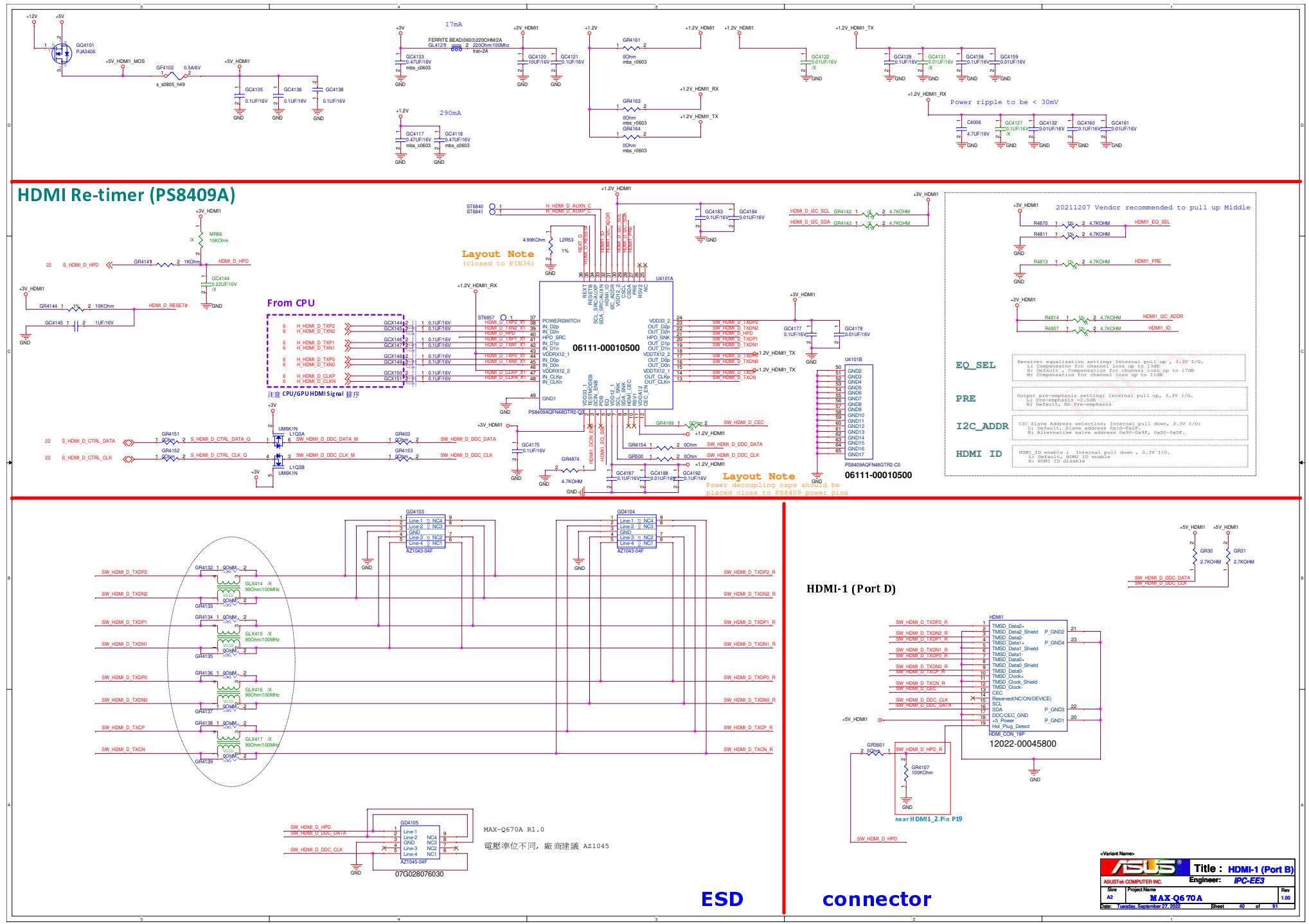


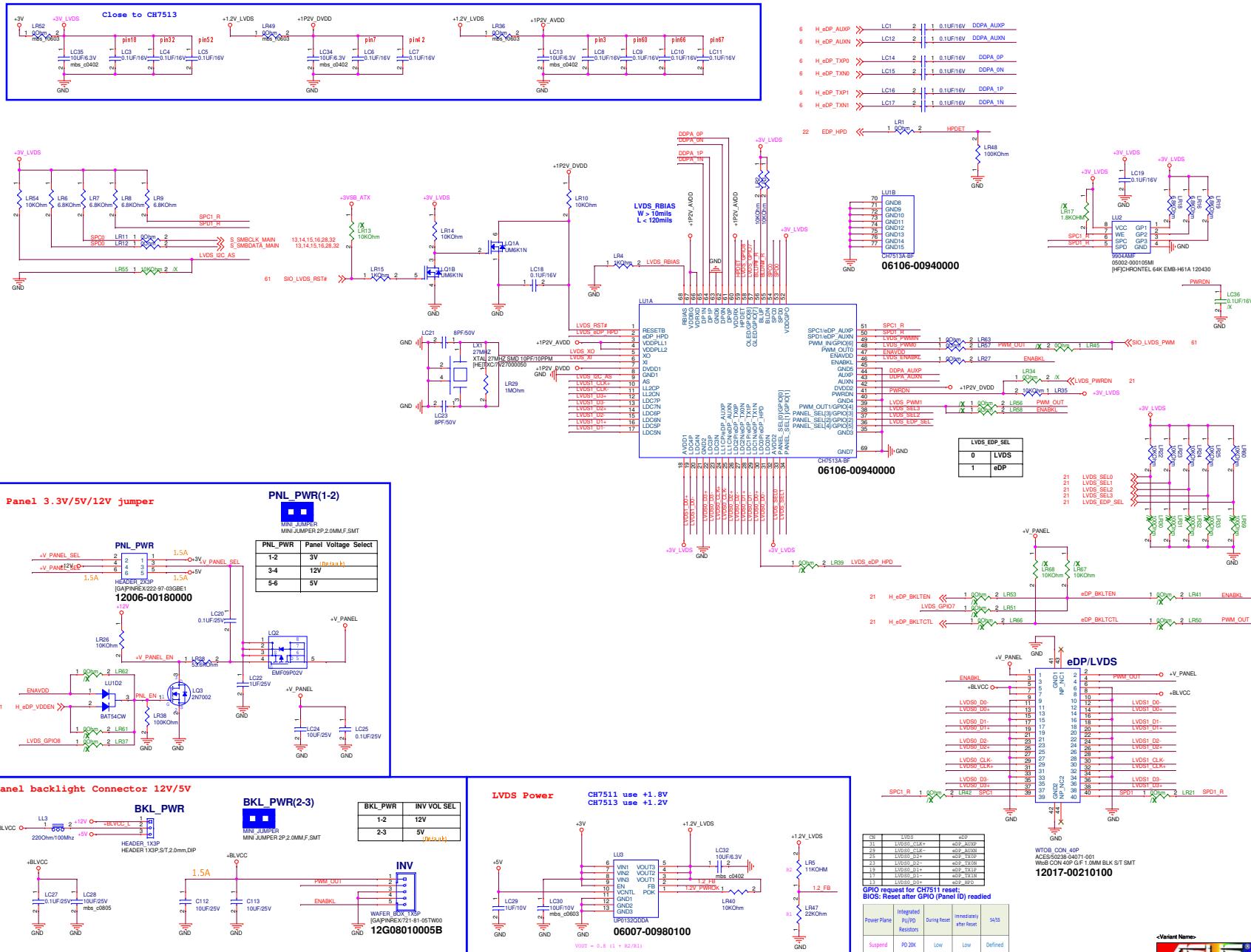
20220802 VGA (DDIC port)



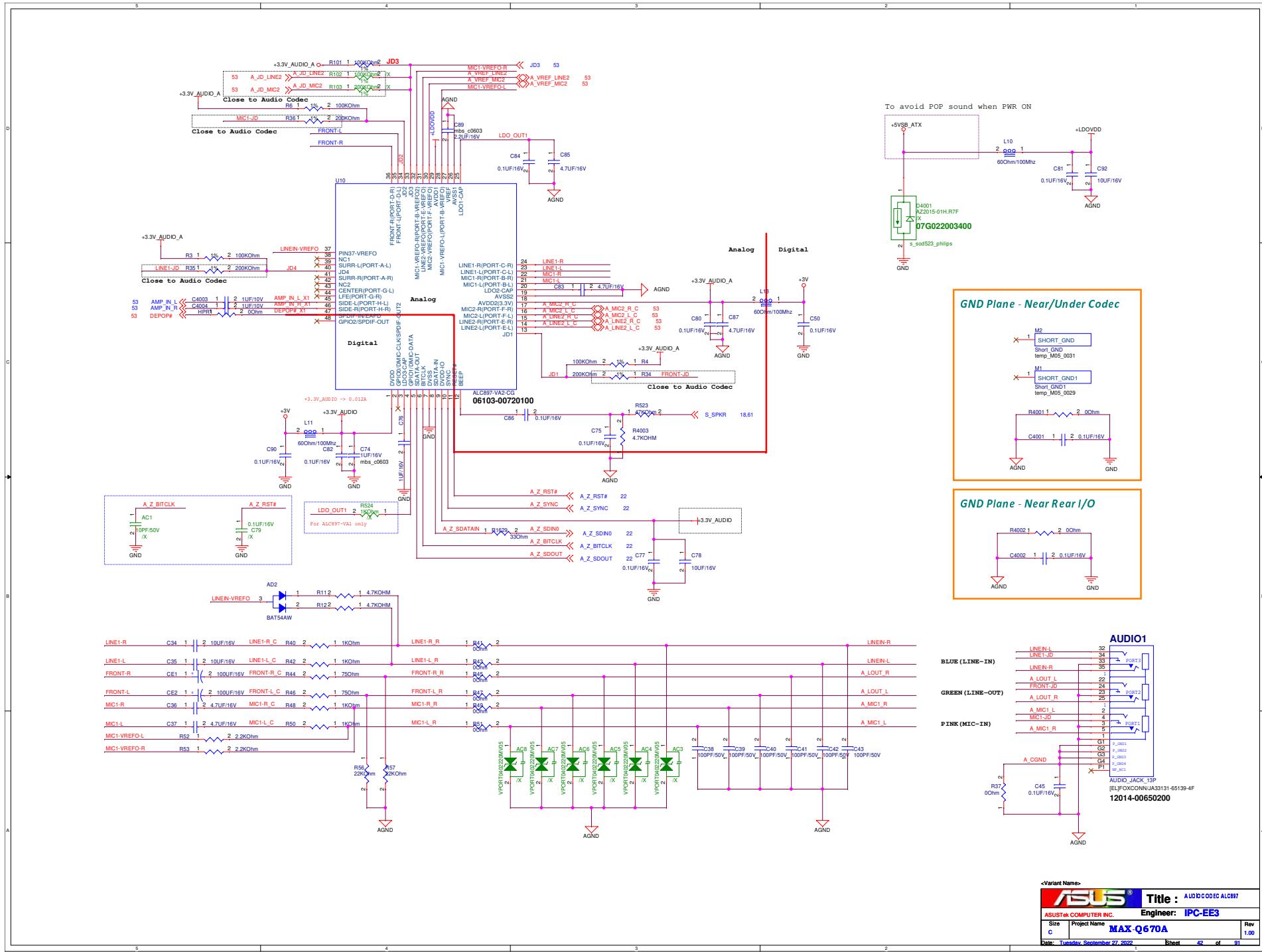
<Variant Name>		Title : VGA_header	
ASUSTek COMPUTER INC.		Engineer: IPC-EE3	
Size	Project Name	MAX-Q670A	Rev
A2			1.00
Date: Tuesday, September 07, 2022	Sheet	38	of 91



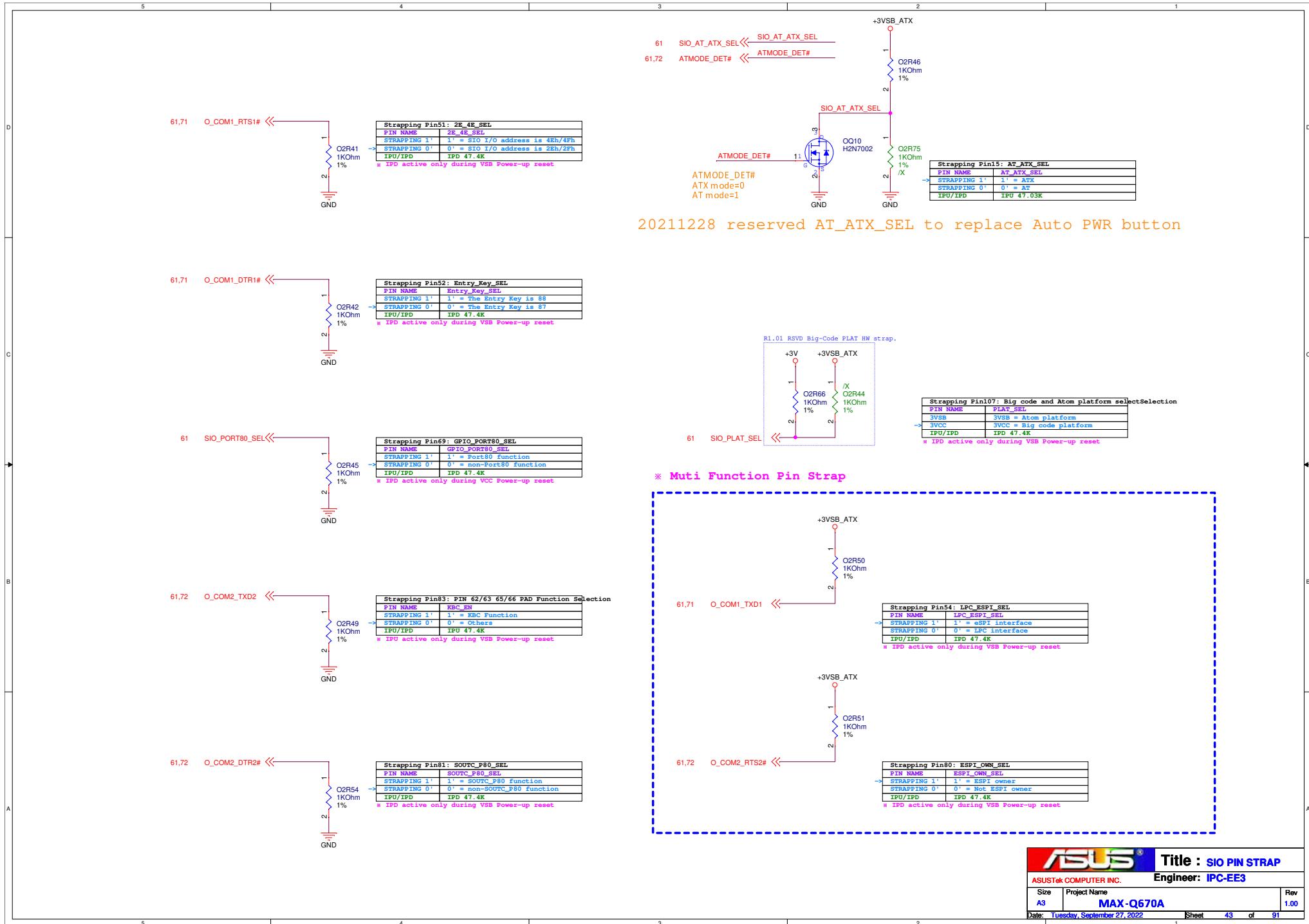


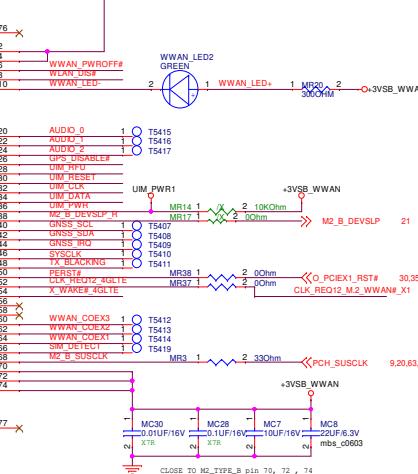
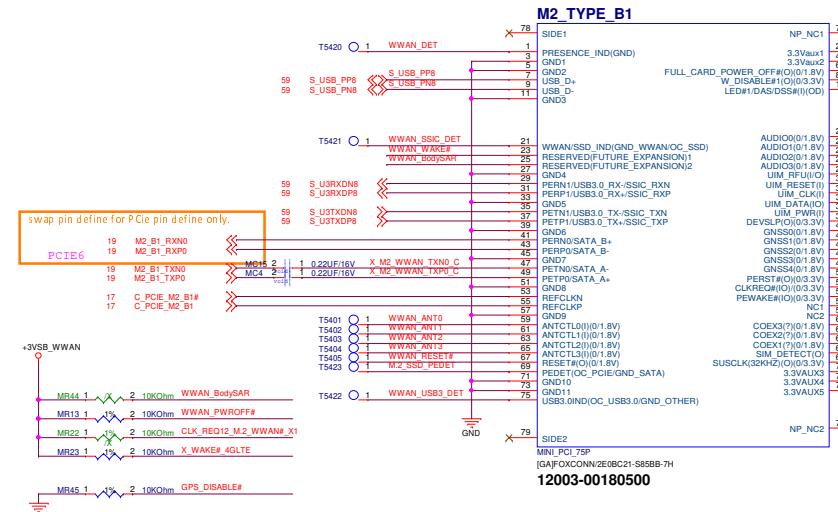
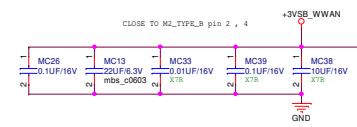
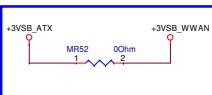


Variant Name: **ASUS MAX Q 670 A** Title: **eDP/LVDS (CH7513)**
 Engineer: **IPC-EE3**
 Rev 1.00
 Page 41 of 61
 Date: Tuesday, September 27, 2022



<Variant Name>
ASUS® Title : **AUDIO CODEC ALC887**
 ASUSTek COMPUTER INC. Engineer: **IPC-EE3**
 Size | Project Name **MAX-Q670A** Rev
 c Date: Tuesday, September 27, 2022 Sheet 42 of 91

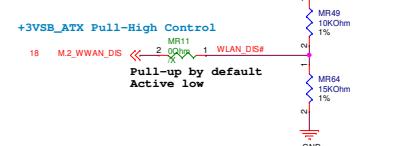
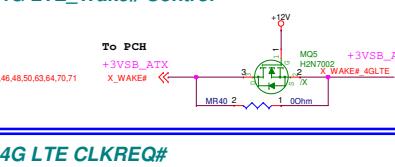
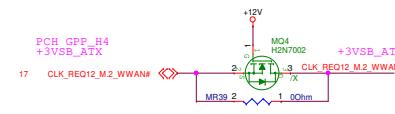
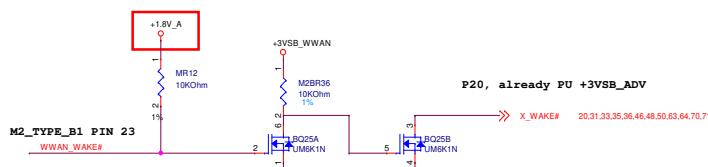




12003-00180500

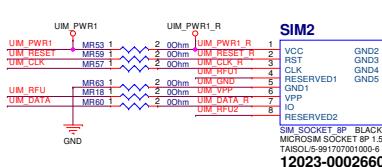
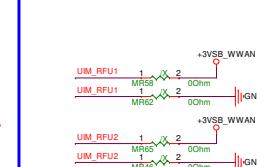
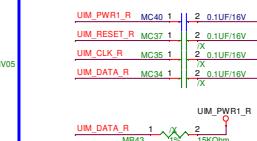
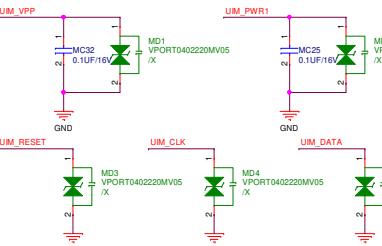
WWAN Disable

Disable wireless communications

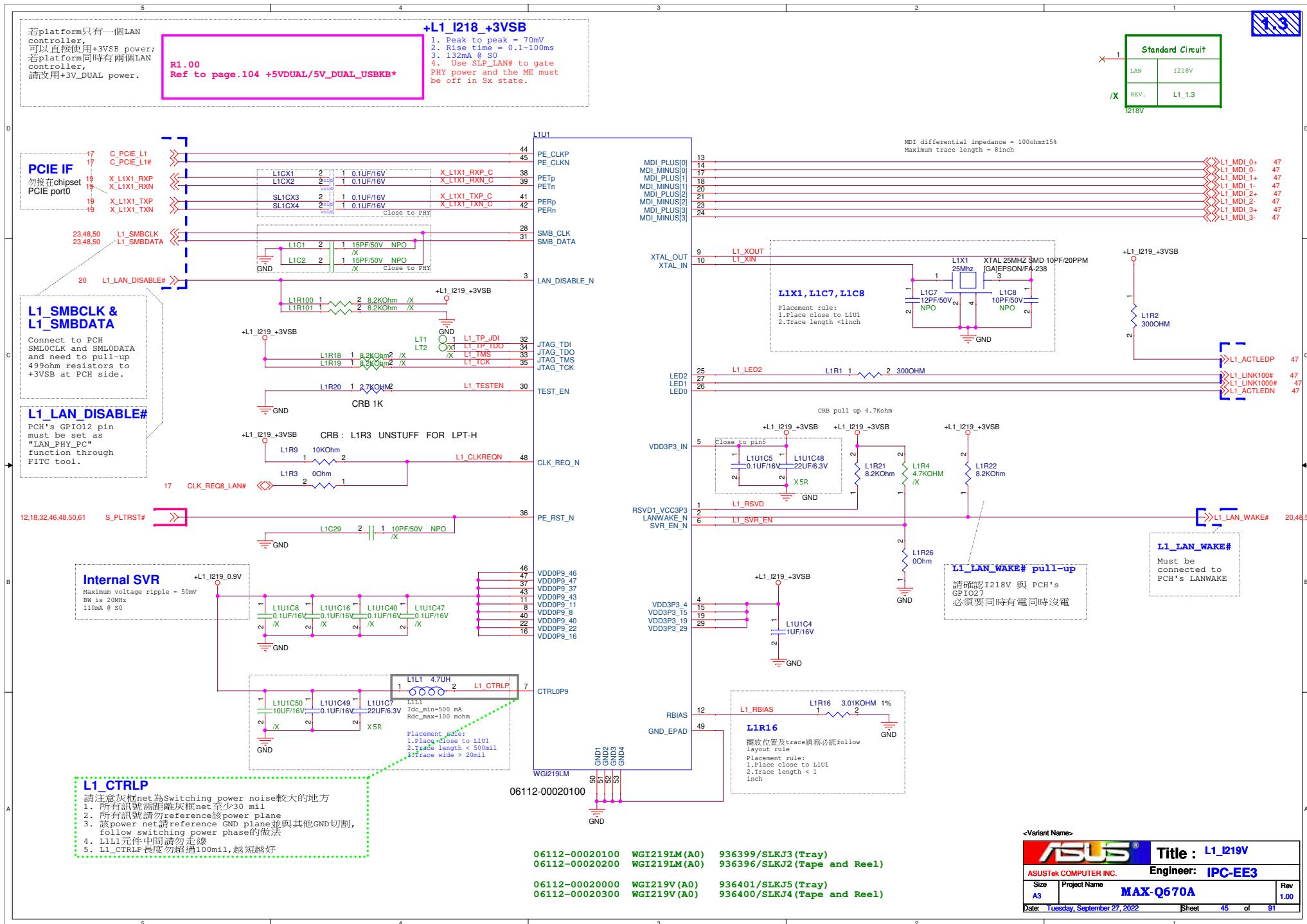
**4G LTE_Wake# Control****4G LTE CLKREQ#****WWAN_WAKE# (SPEC voltage 1.8V)**

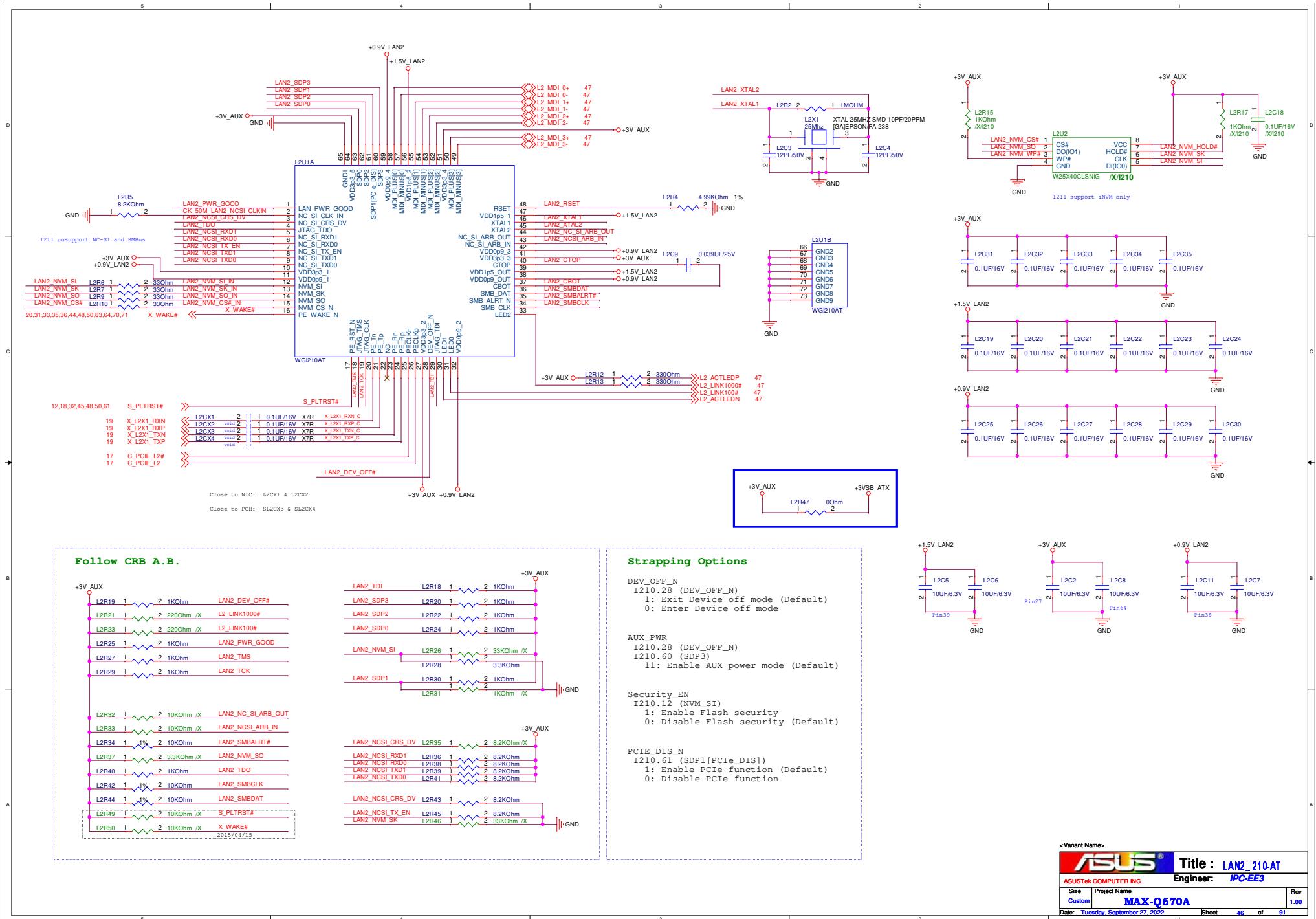
20220118 remove the SATA/PCIe DET circuits

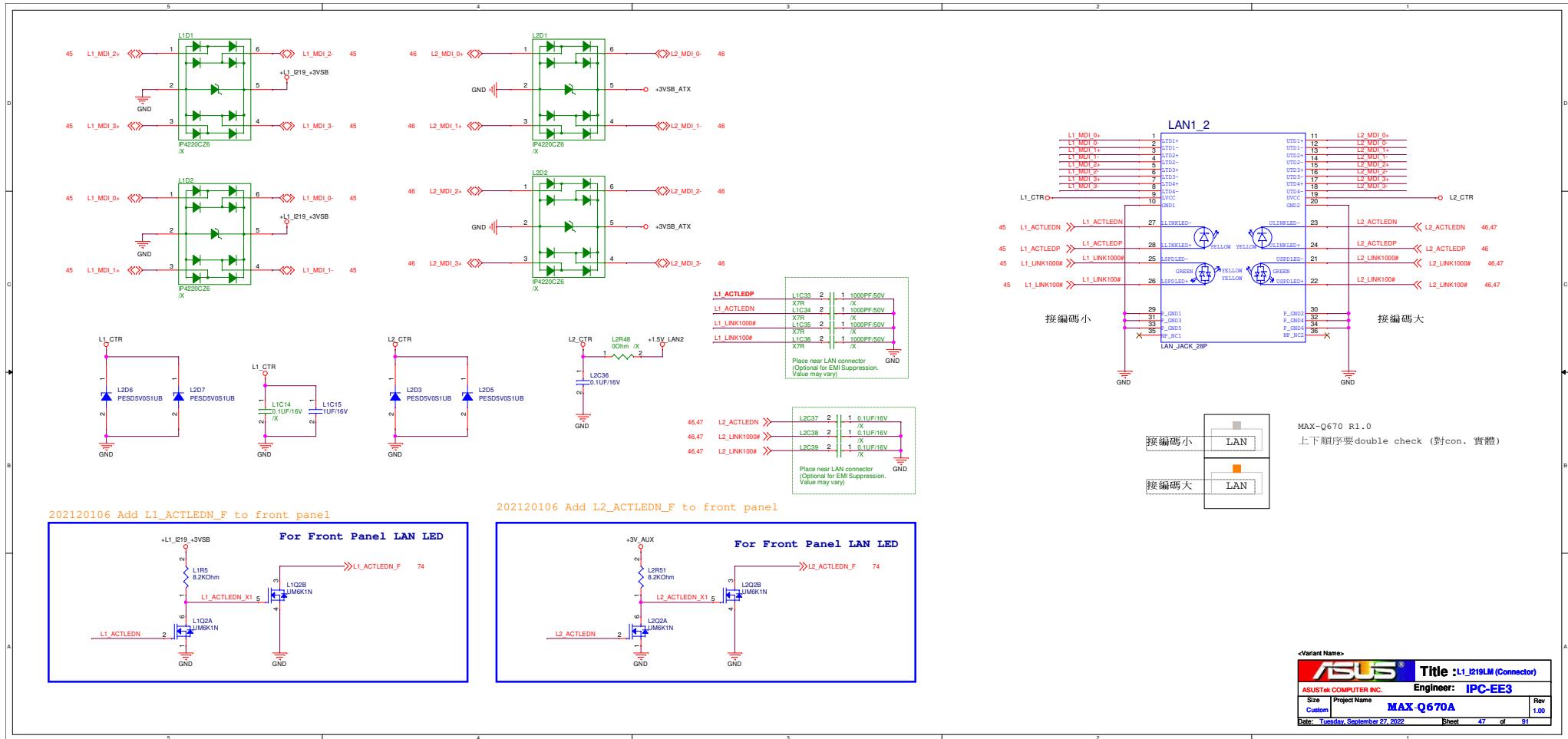
MAX Q670 8 個SATA port MKT SPEC 已規劃使用,故不support SATA

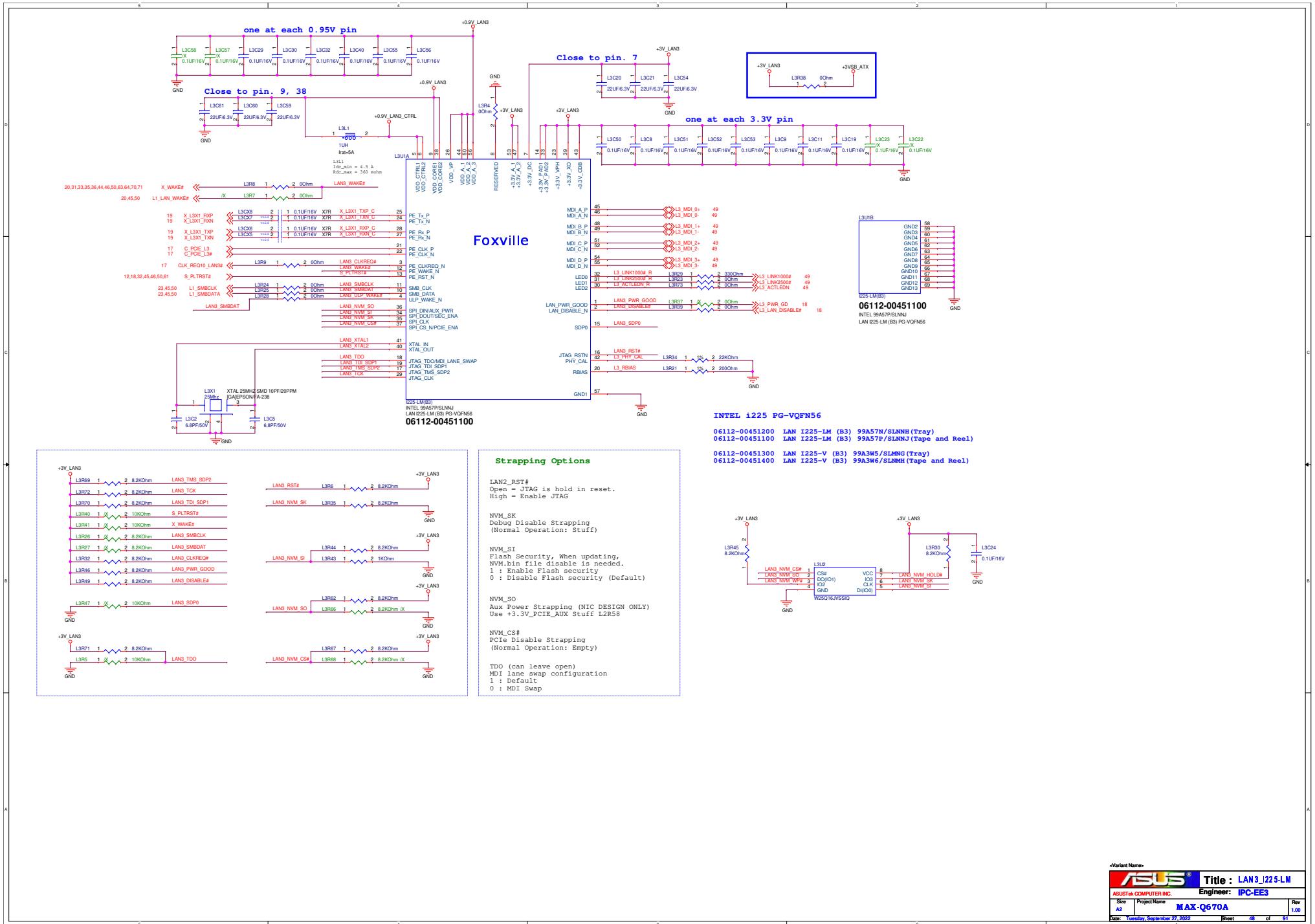
Micro-SIM Card**Reserved Pin for Signal Quality****Micro-SIM Card - ESD Protection**

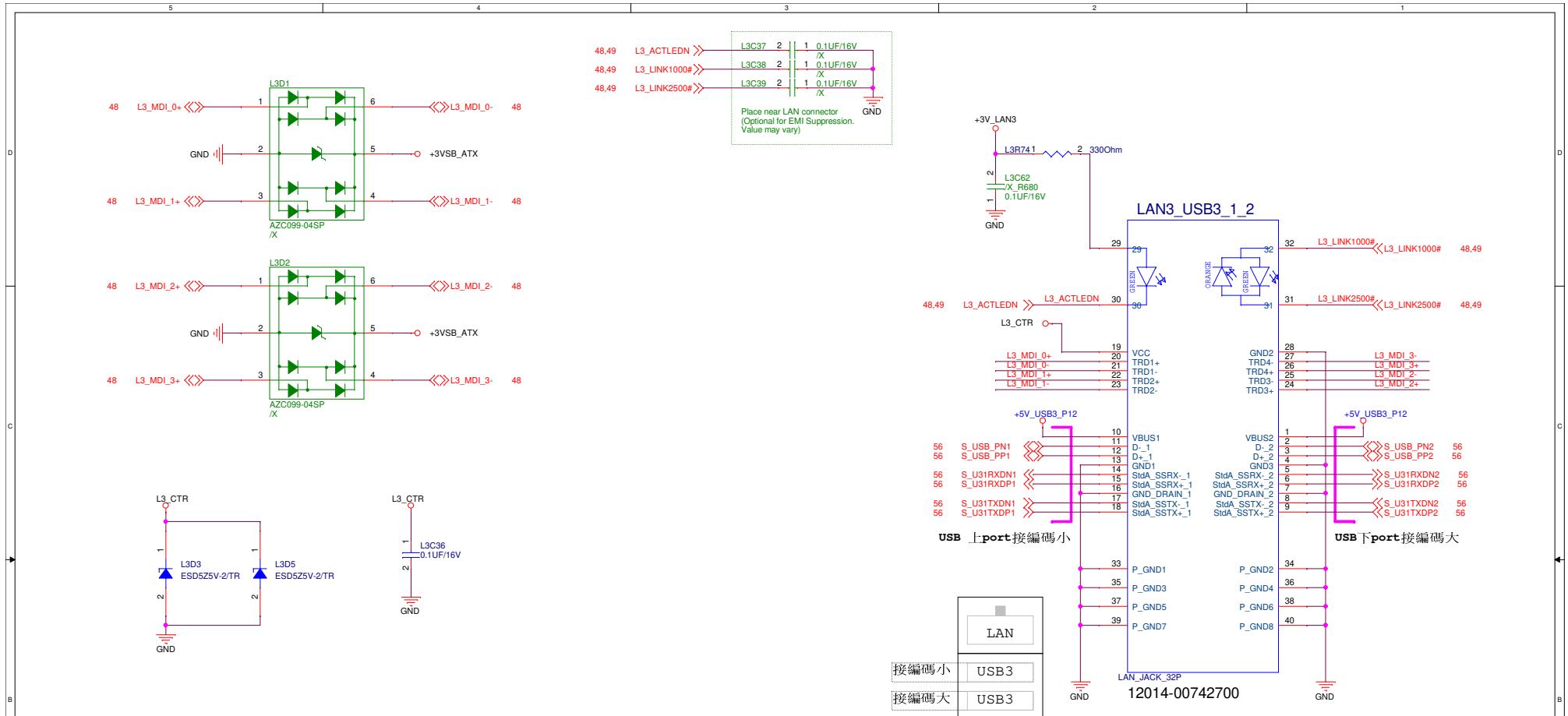
Variant Name:		Title : M.2_Key-B_LTE	
ASUS COMPUTER INC.		Engineer: IPC-EE3	
Size	Project Name	MAX-Q670A	Rev
C			1.00
Date: Tuesday, September 27, 2022	Sheet	44	of 91



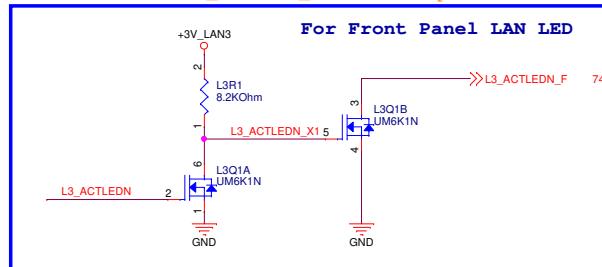








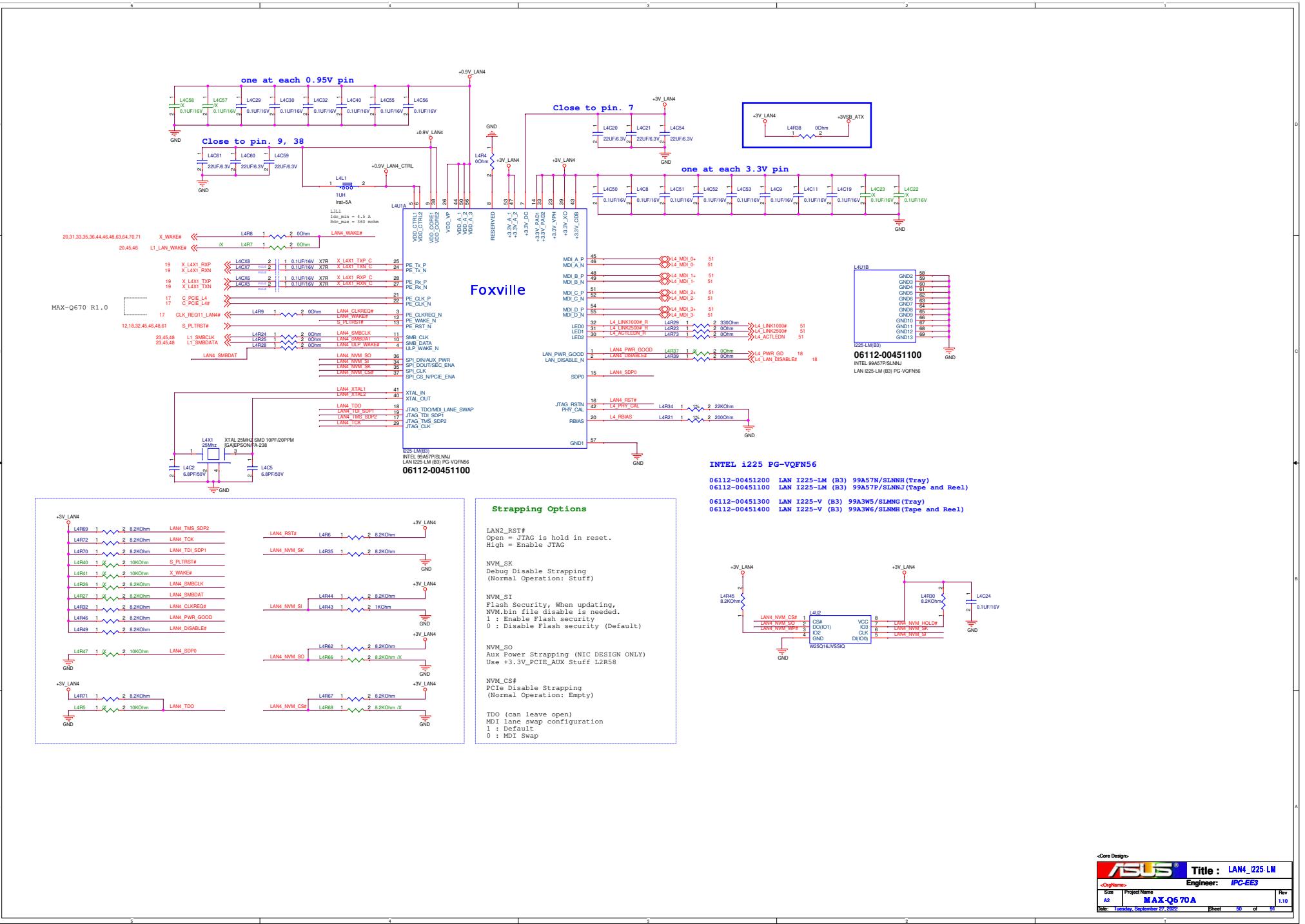
202120106 Add L3_ACTLEDN_F to front panel

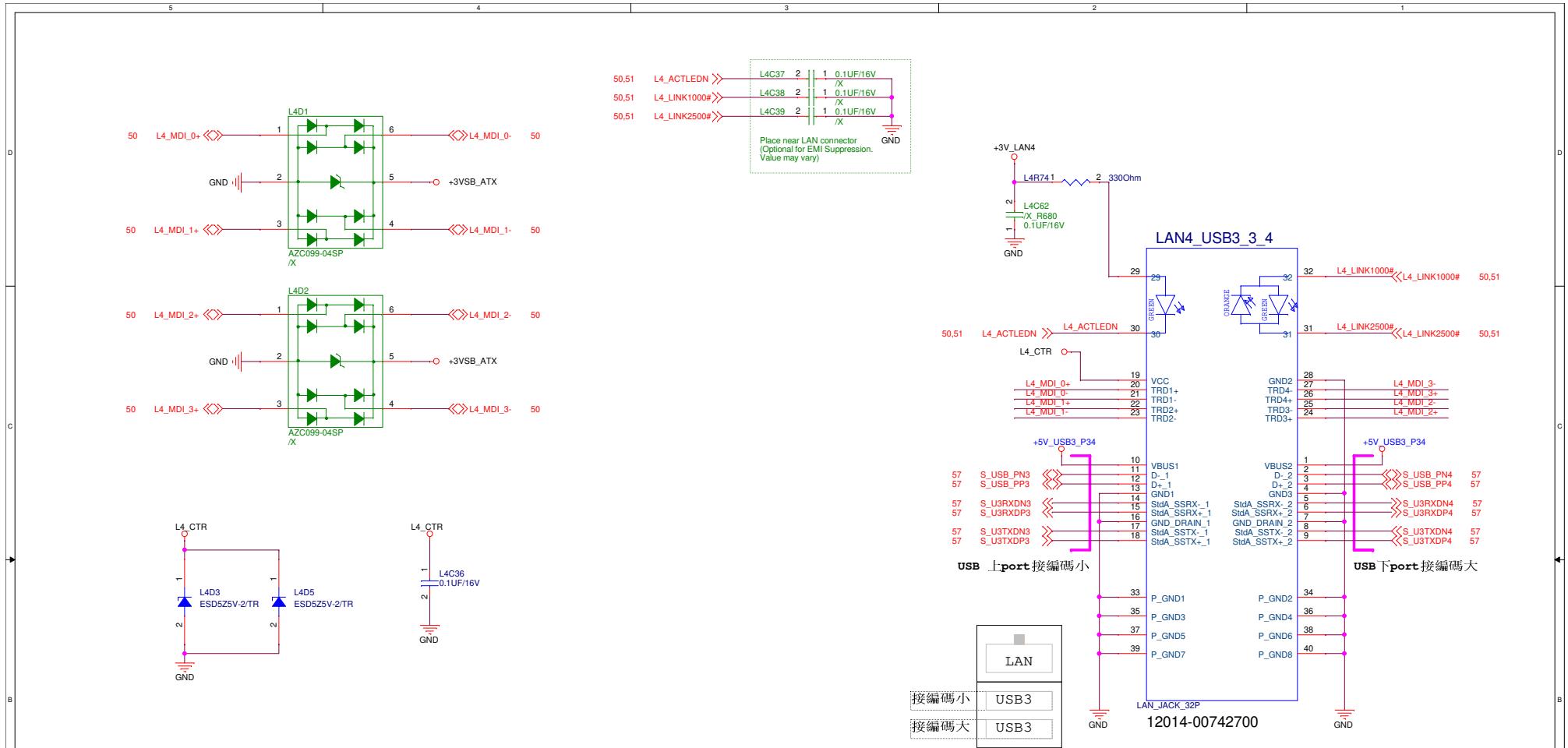


LED Configuration #1 Expected Behavior

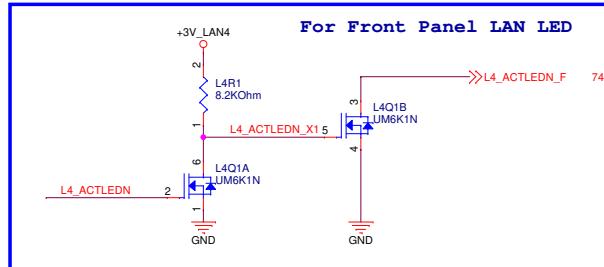
Speed LED	
10 Mbps	OFF
100 Mbps	OFF
1000 Mbps	Yellow
2500 Mbps	Green
Link-Activity LED	
Link-up	Green
Tx/Rx Activity	Blinking Green

← 2nd Highest Speed
← Highest Speed



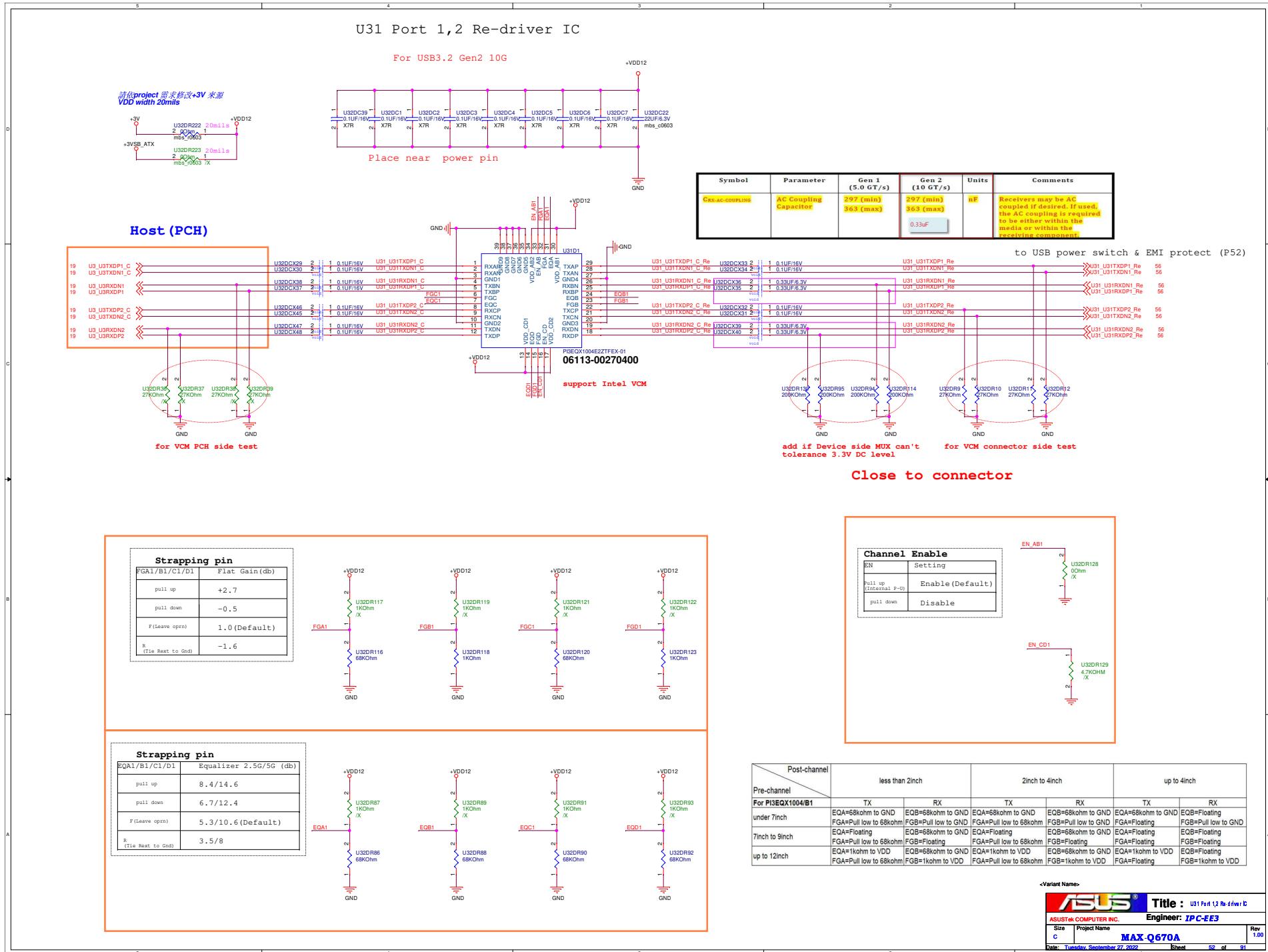


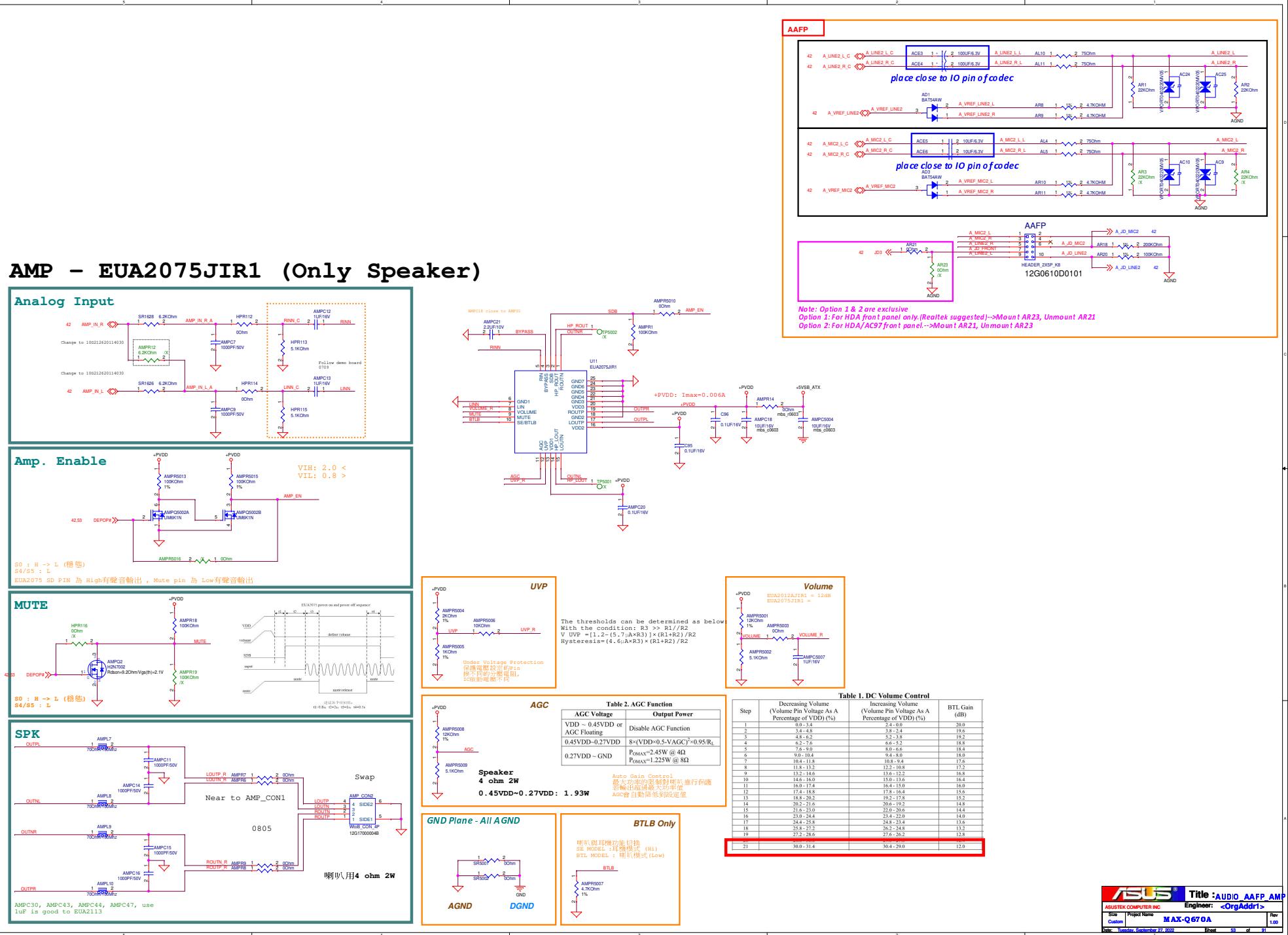
202120106 Add L3_ACTLEDN_F to front panel

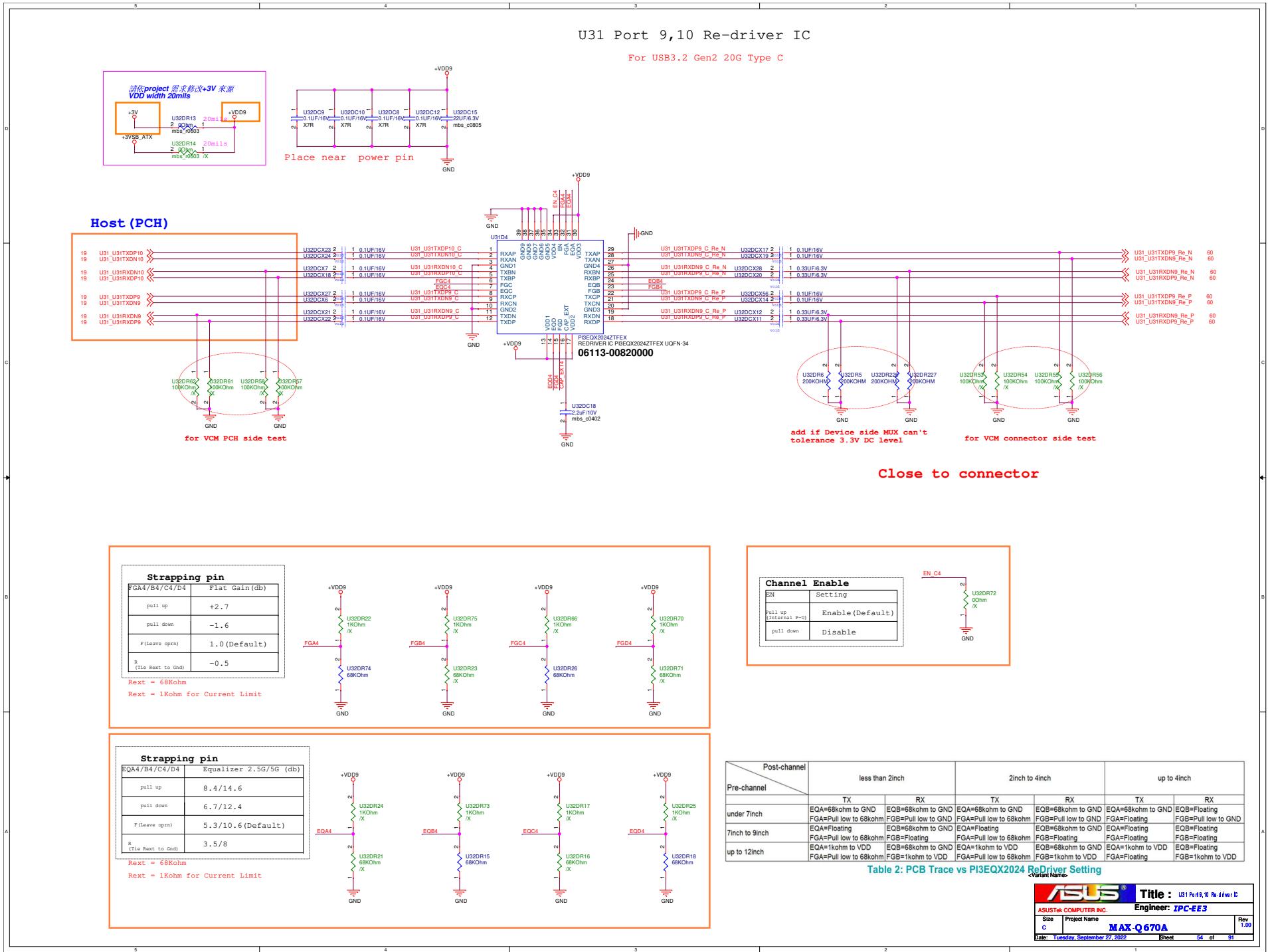


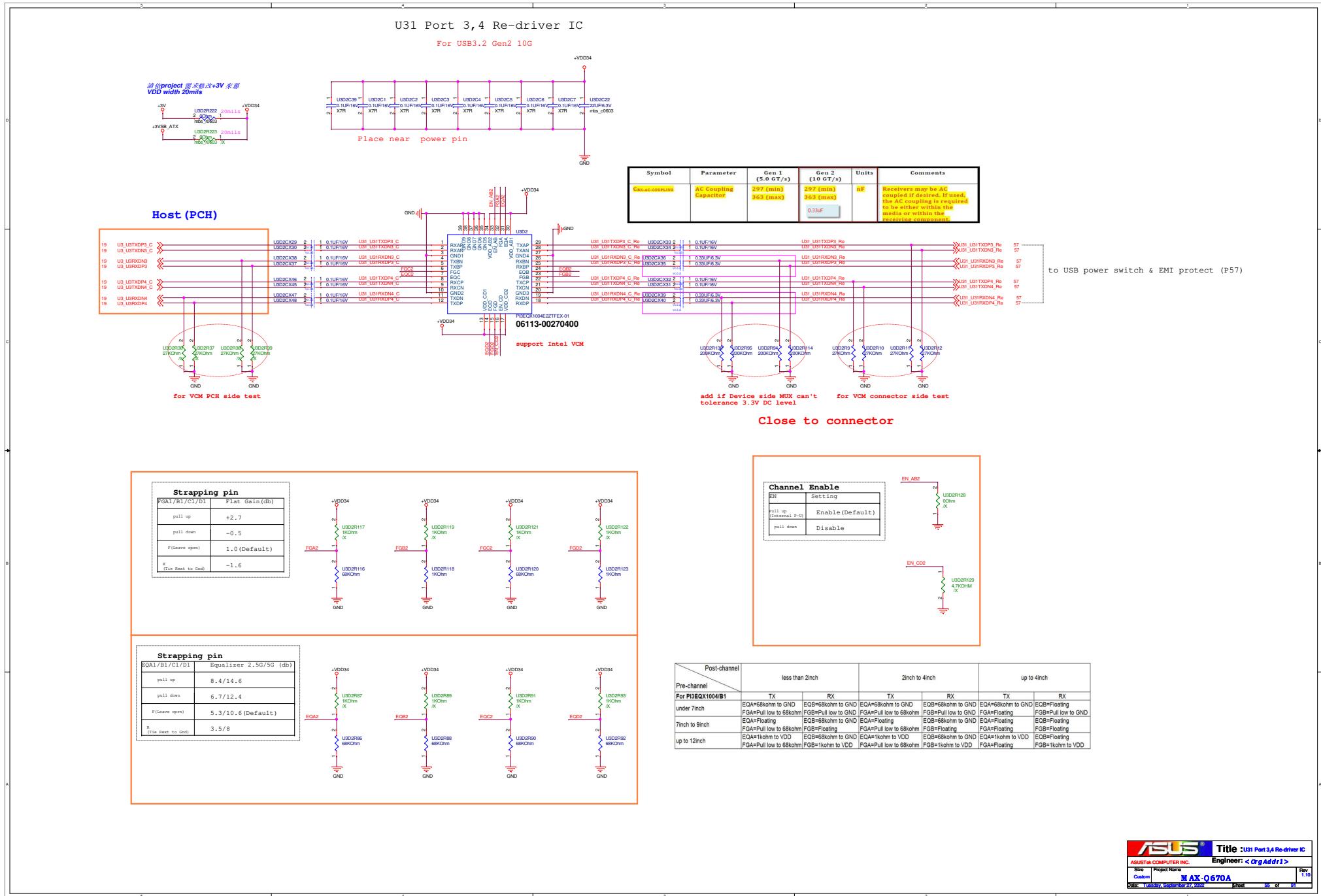
LED Configuration #1 Expected Behavior

Speed LED	
10 Mbps	OFF
100 Mbps	OFF
1000 Mbps	Yellow
2500 Mbps	Green
Link-Activity LED	
Link-up	Green
Tx/Rx Activity	Blinking Green









USB power switch & EMI protect (1, 2)

Related :

052.U31 Port 1,2 Re-driver IC
056.USB31 Port 1,2
USB power switch & EMI protect
047.LAN1_RJ45_USB31 Port 1,2

IN/Output signal List :

USB3

from re-driver

U31_U31RXDN1_Re
U31_U31RXDP1_Re
U31_U31TXDN1_Re
U31_U31TXDP1_Re

U31_U31RXDN2_Re
U31_U31RXDP2_Re
U31_U31TXDN2_Re
U31_U31TXDP2_Re

to LAN/USB3 connector

S_U3RXDN1
S_U3RXDP1
S_U3TXDN1
S_U3TXDP1

S_U3RXDN2
S_U3RXDP2
S_U3TXDN2
S_U3TXDP2

USB3 OC :

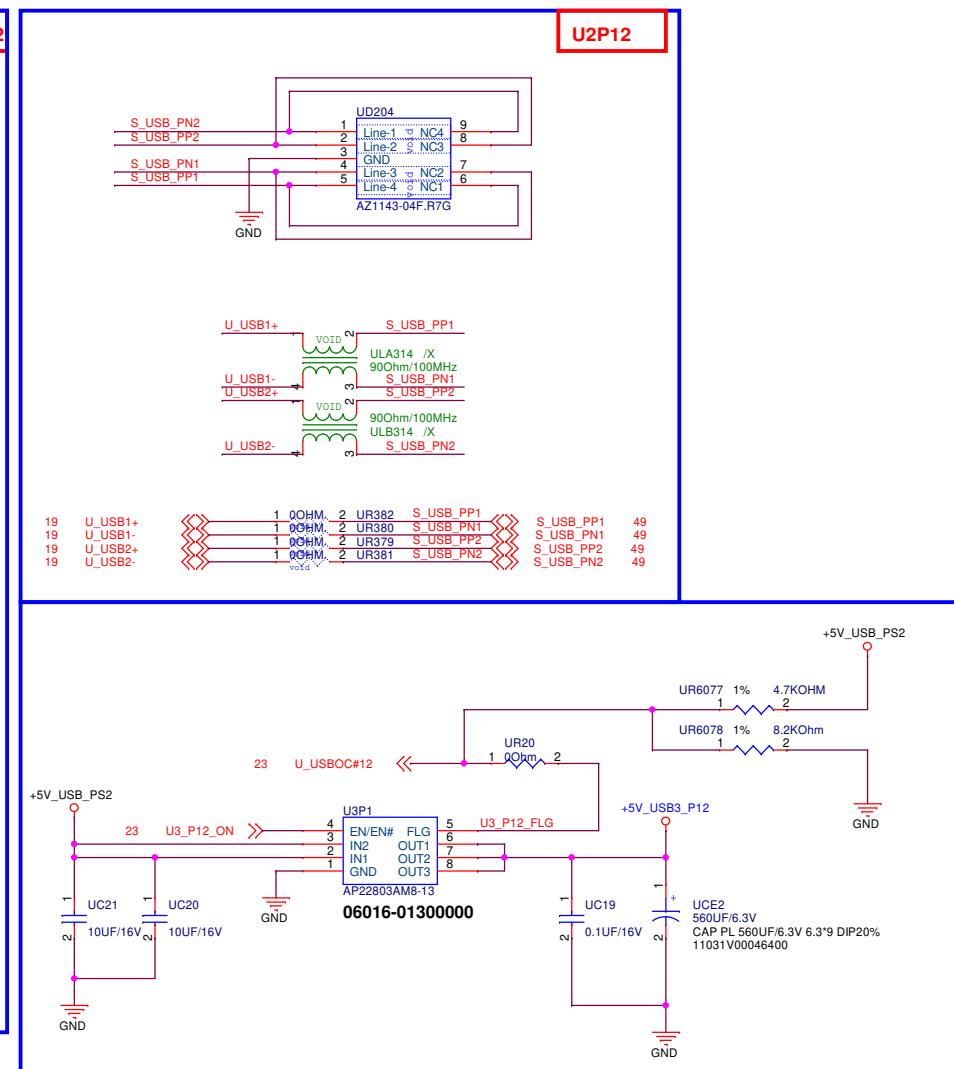
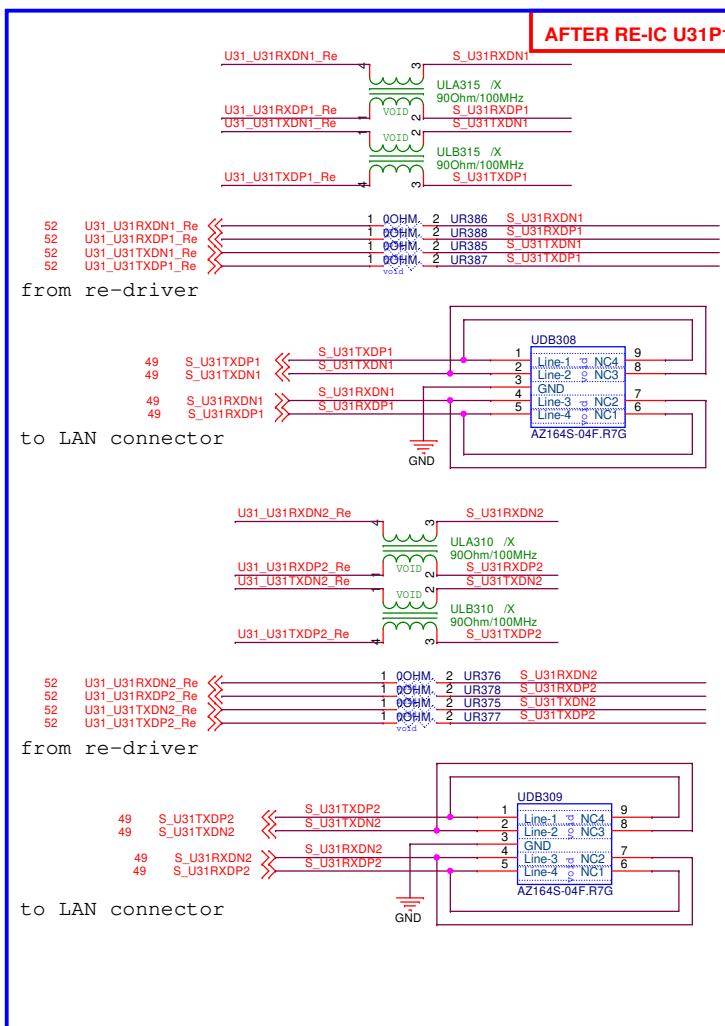
U_USBOC#12

USB2

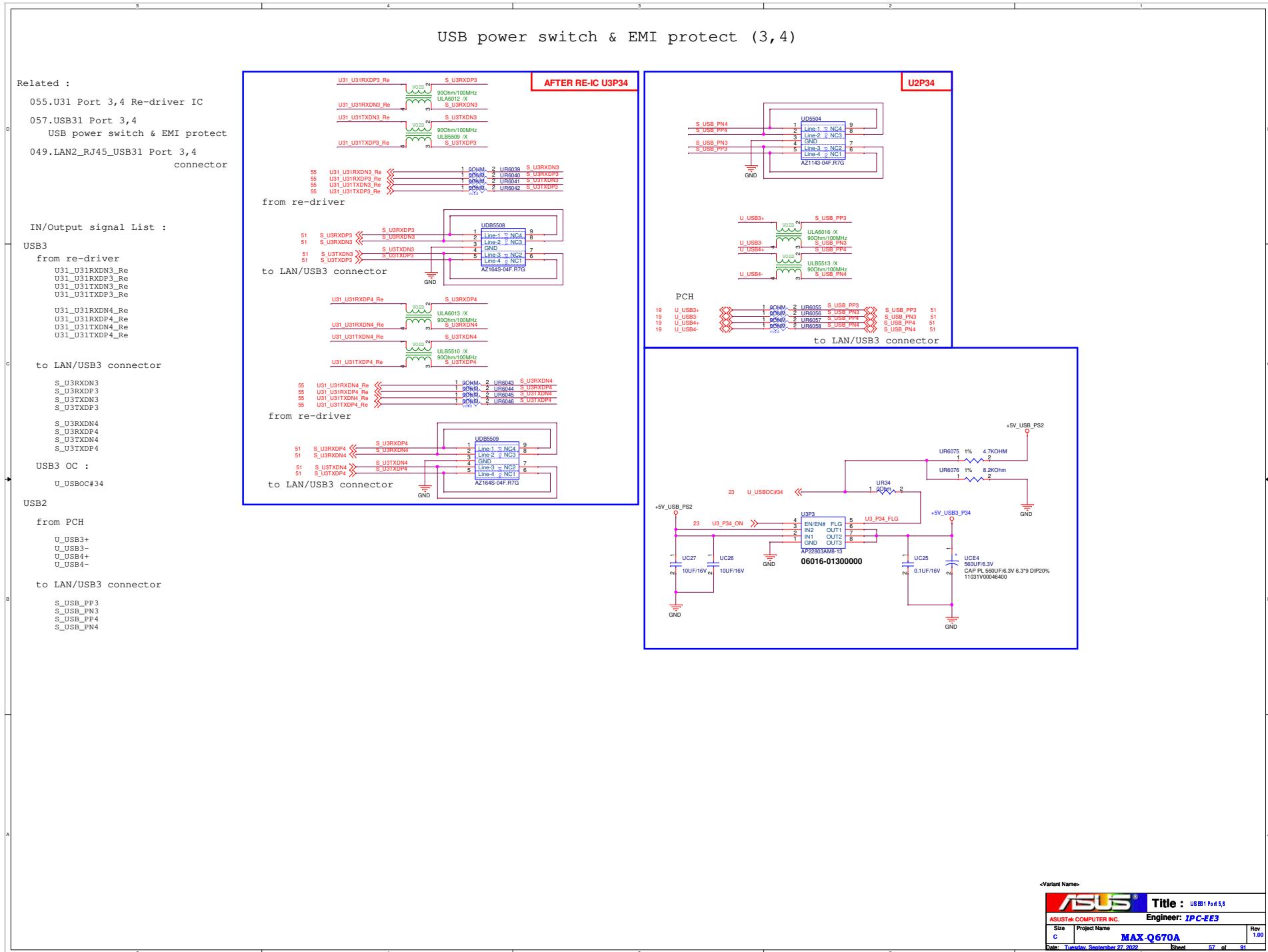
from PCH
U_USB1+
U_USB1-
U_USB2+
U_USB2-

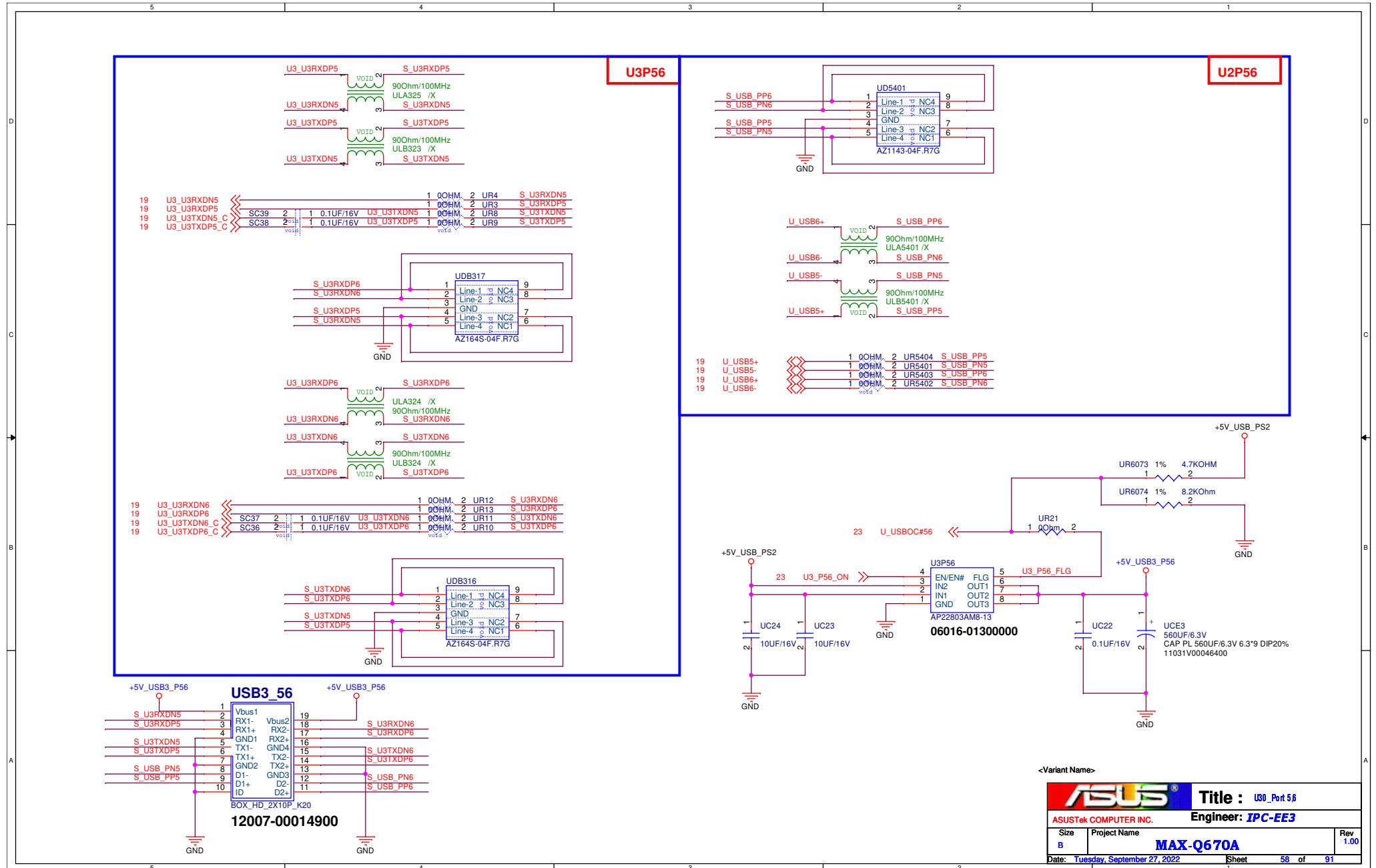
to LAN/USB3 connector

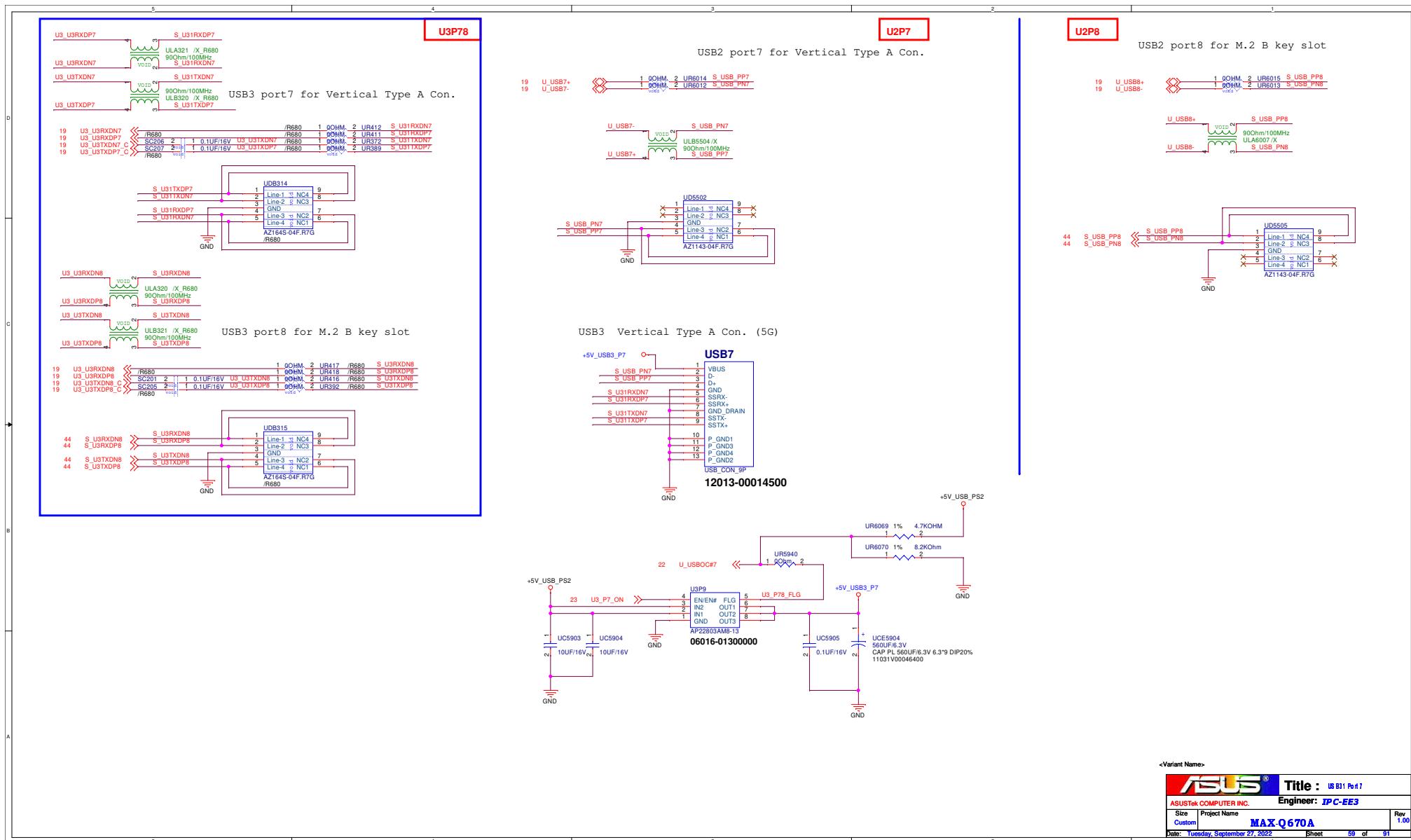
S_USB_PP1
S_USB_PN1
S_USB_PP2
S_USB_PN2

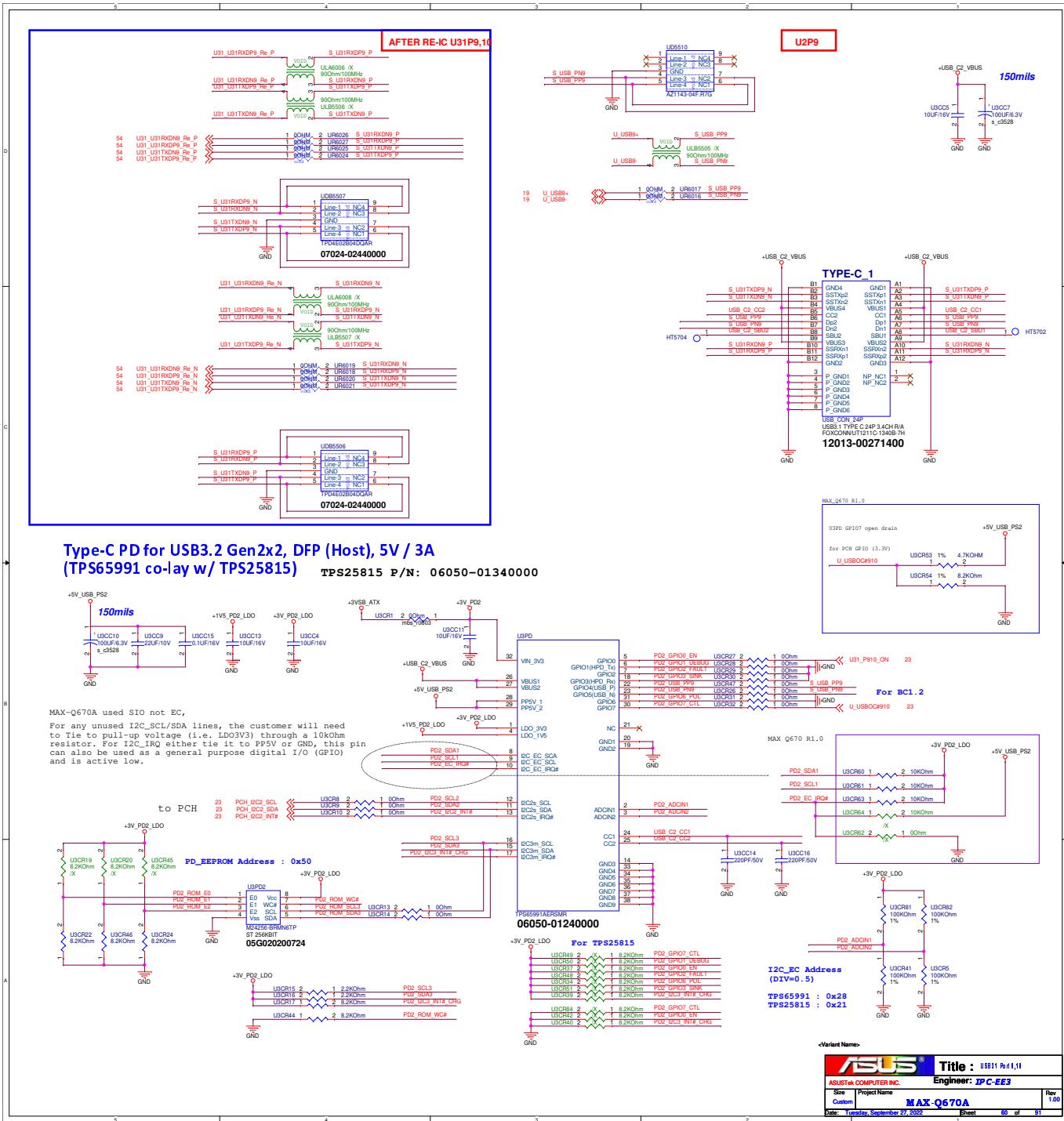


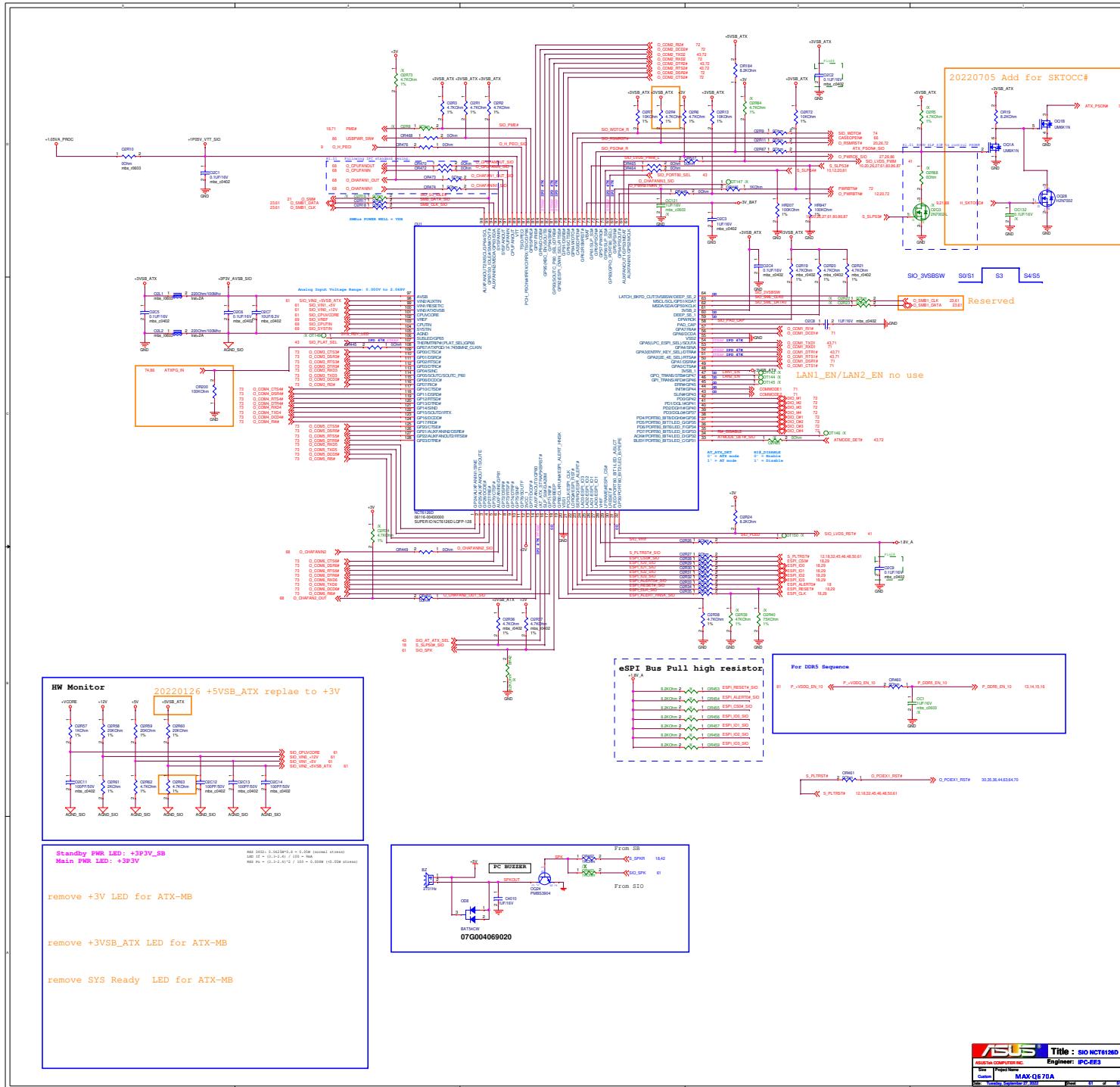
Variant Name:	
ASUS	Title : U31_Port,2
ASUSTek COMPUTER INC.	Engineer: IPC-EE3
Size B	Project Name MAX-Q670A
Date: Tuesday, September 27, 2022	Sheet 1 of 91
	Rev 1.00

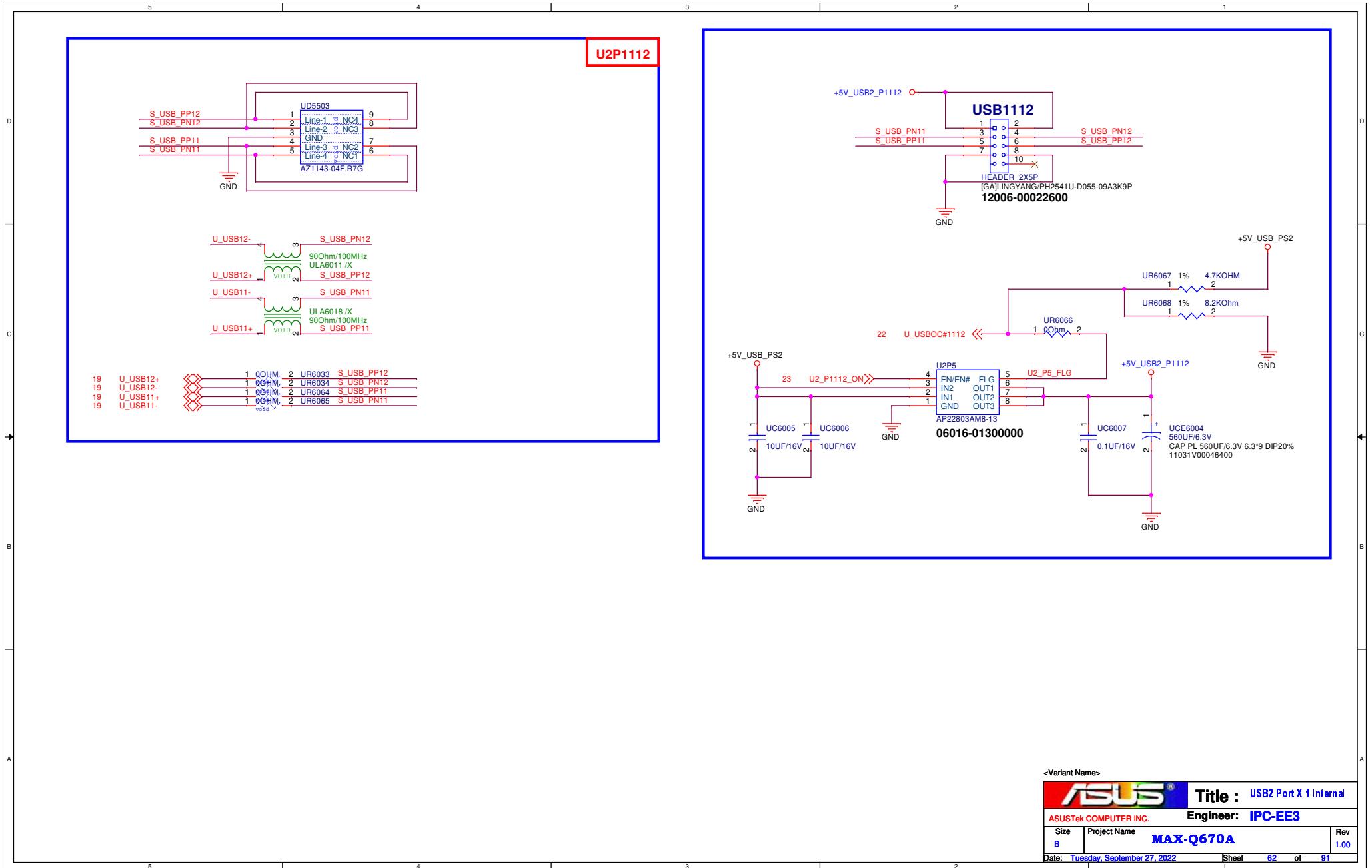




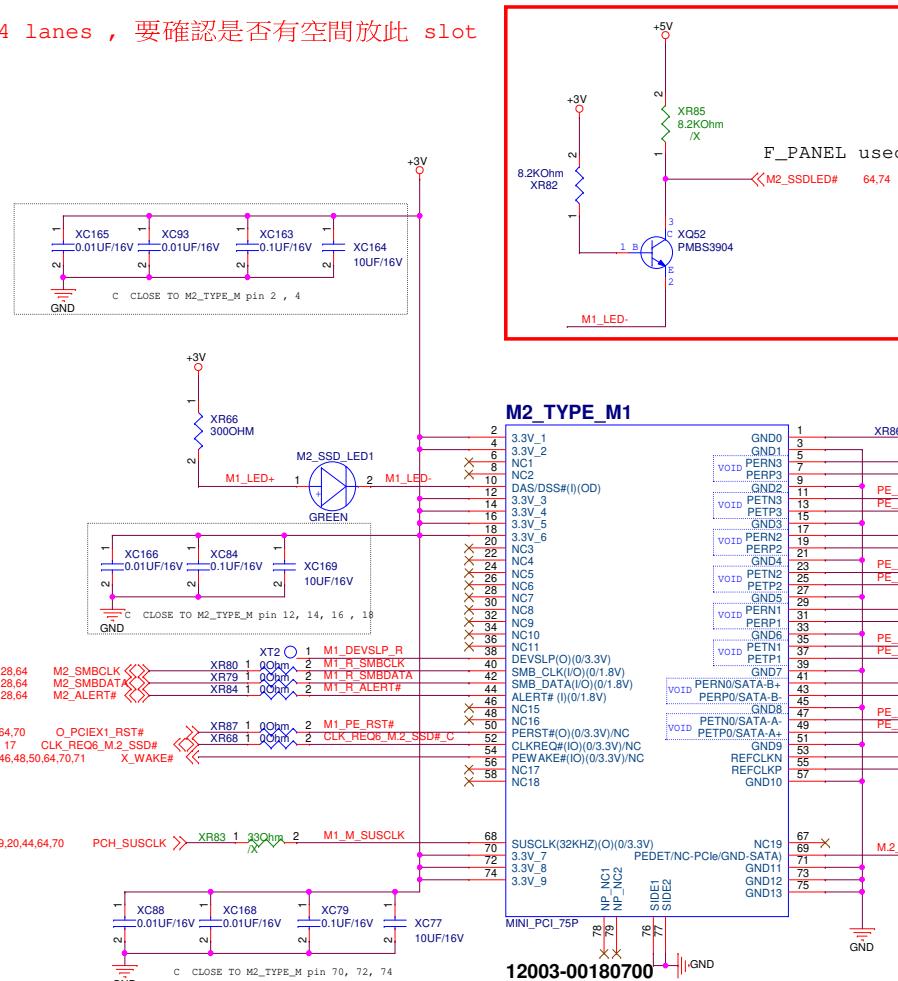




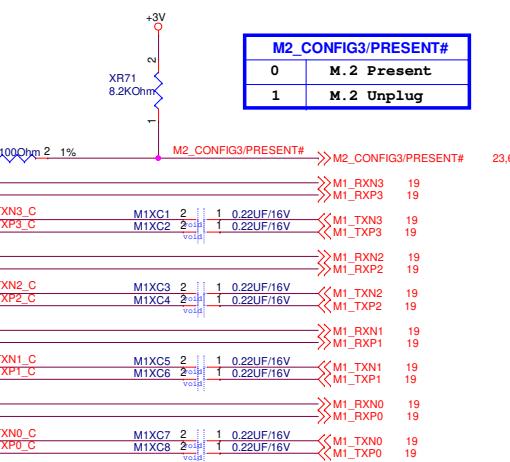
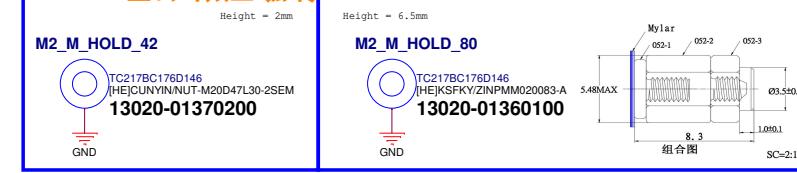


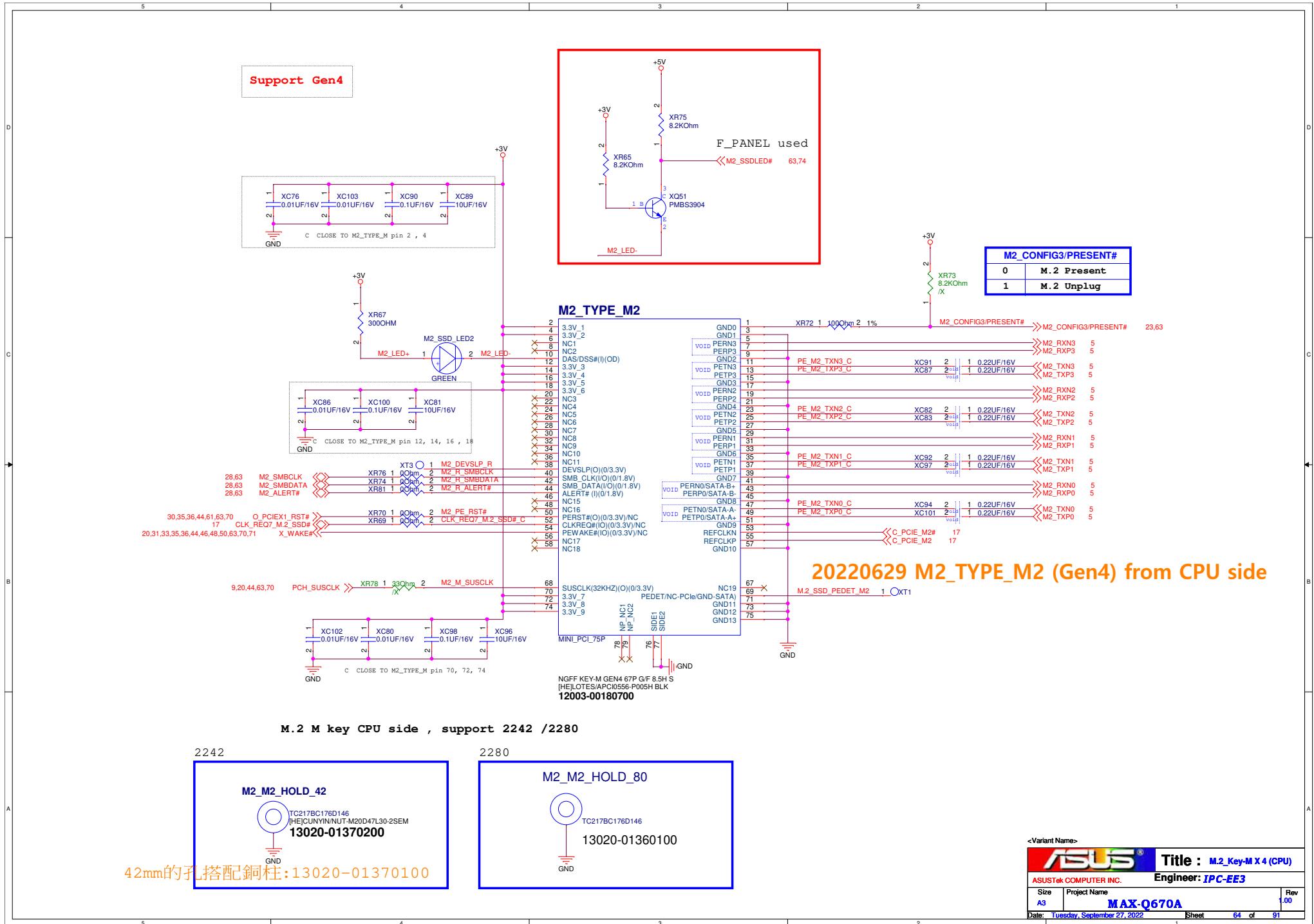


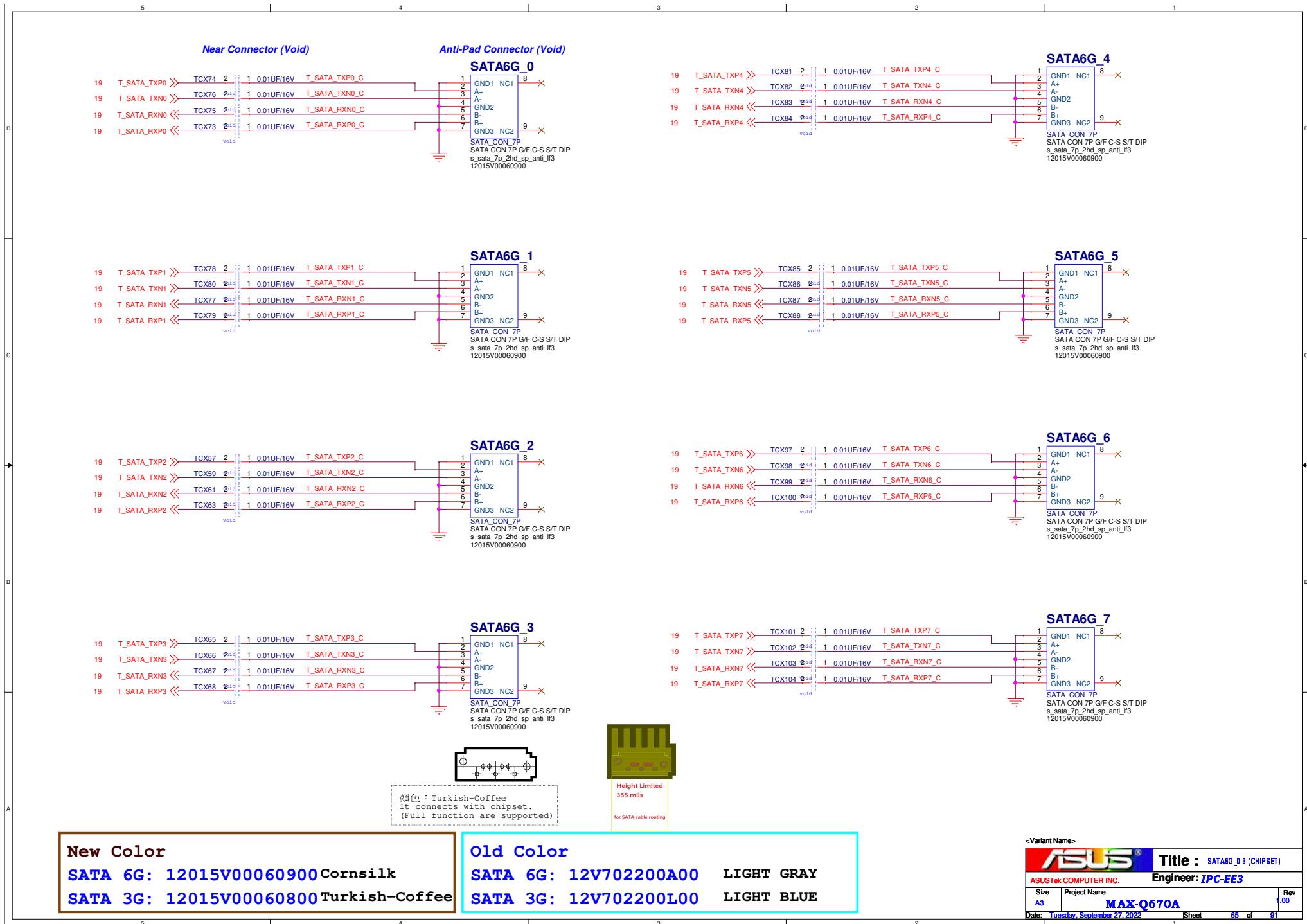
要改 4 lanes , 要確認是否有空間放此 slot

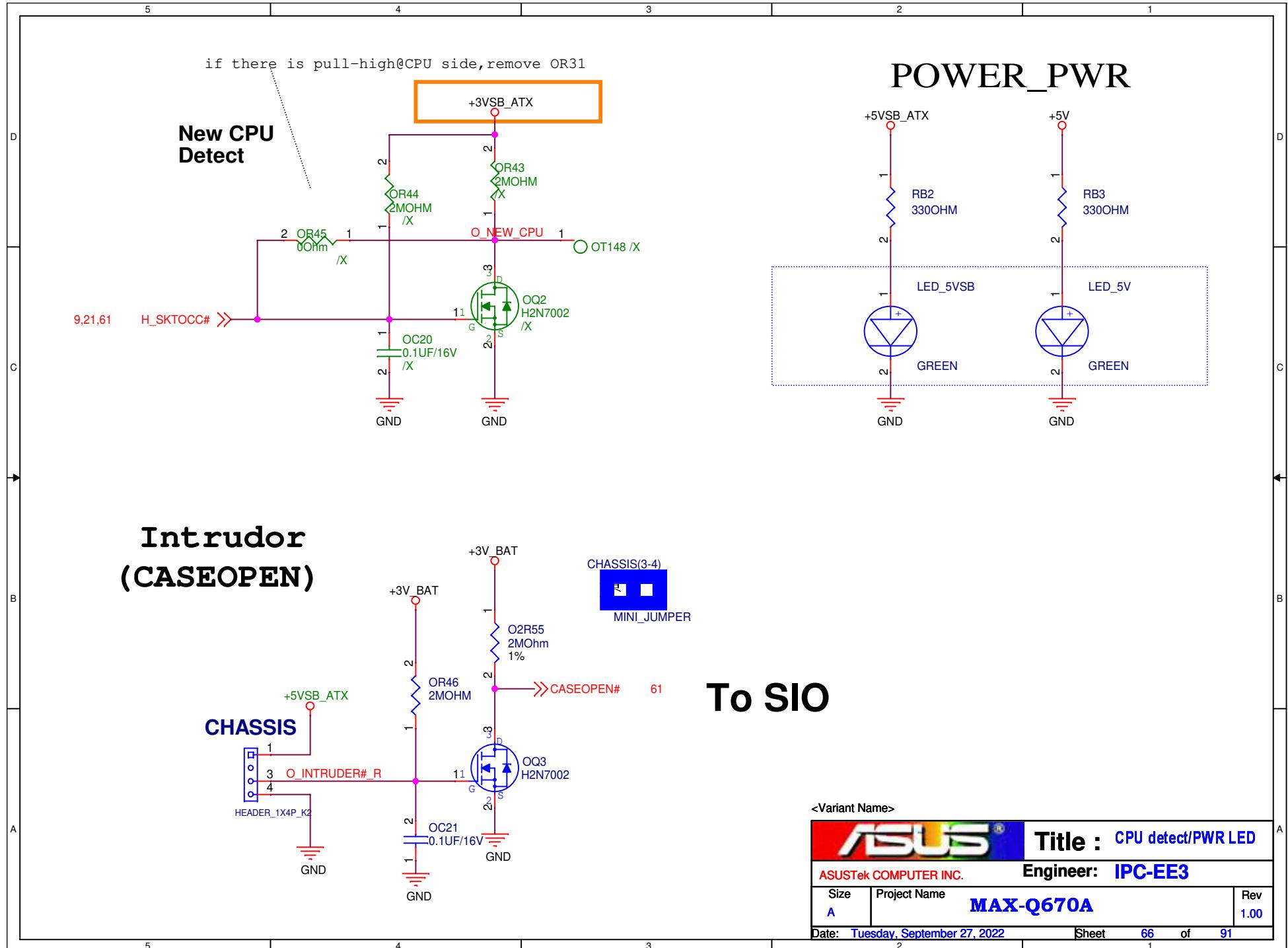


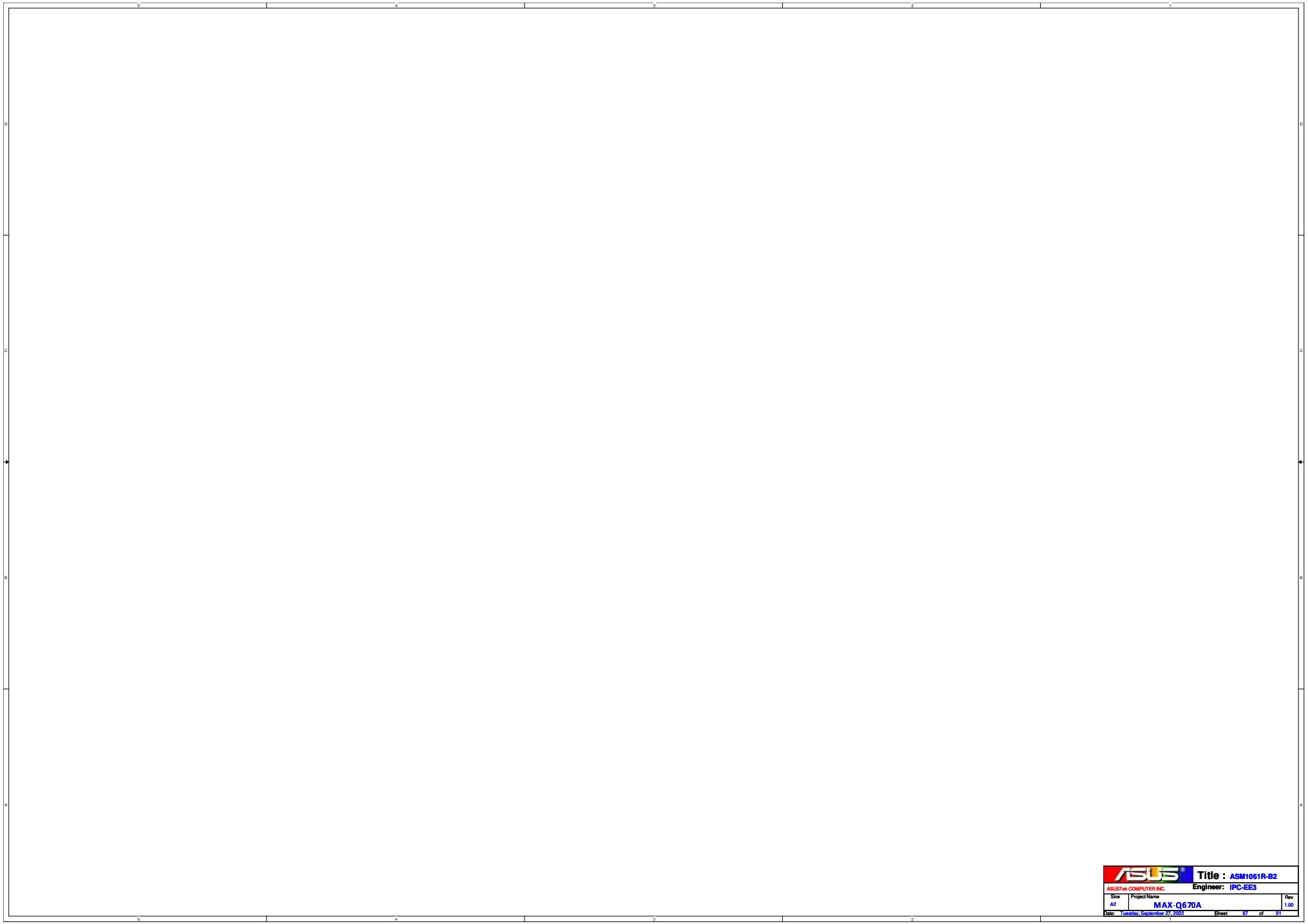
42mm安裝規範編號:13020-01370100

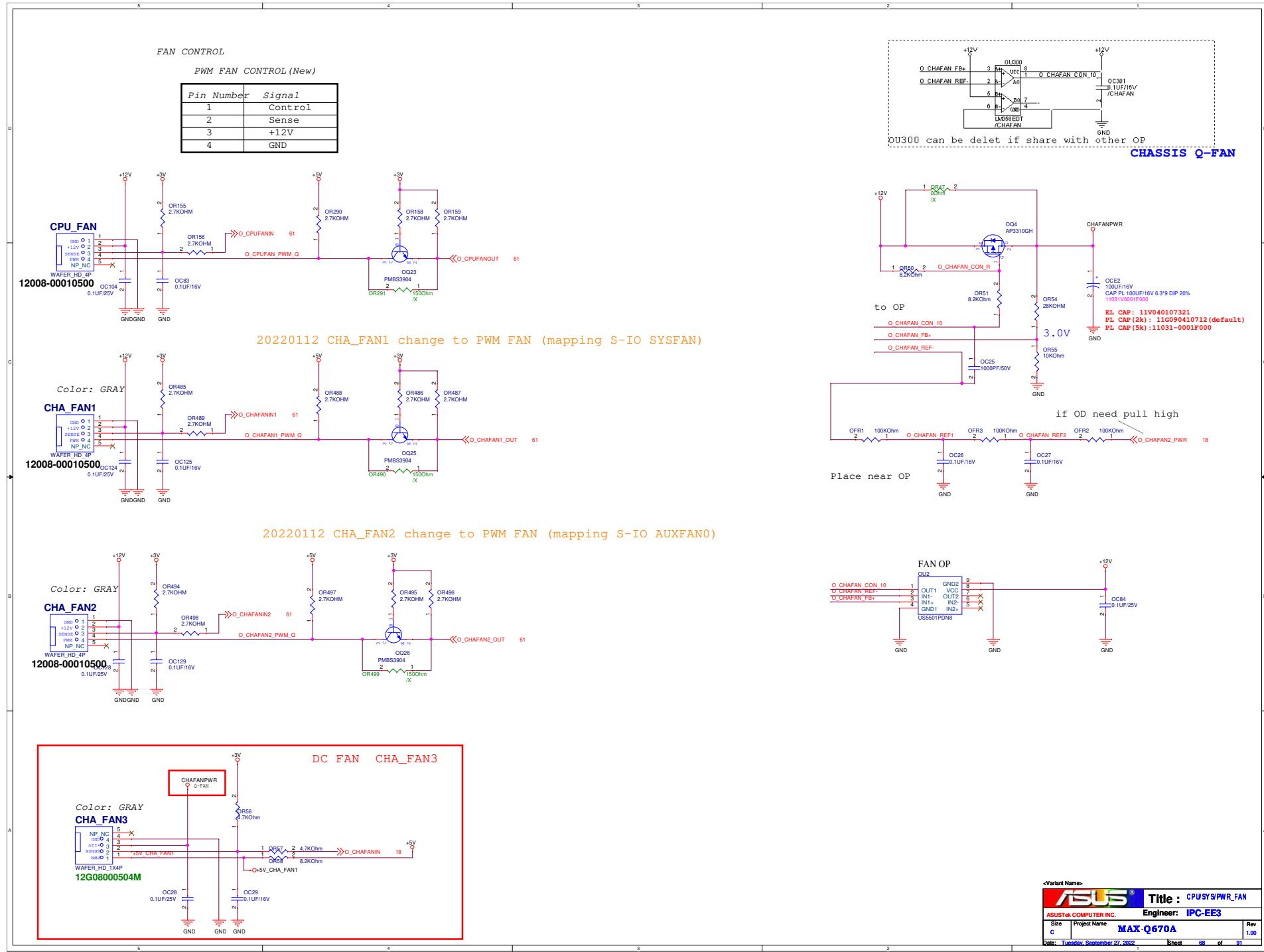


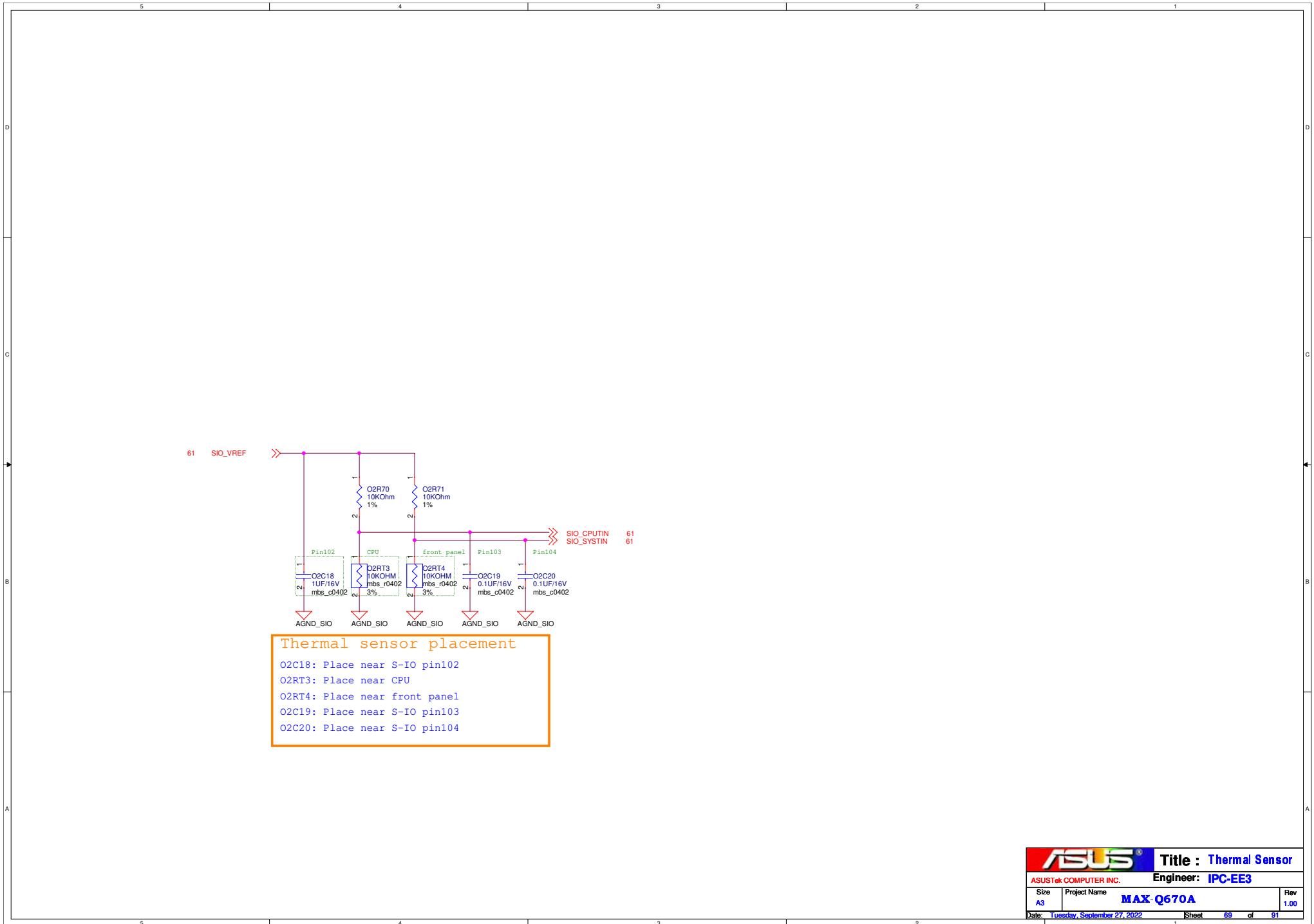


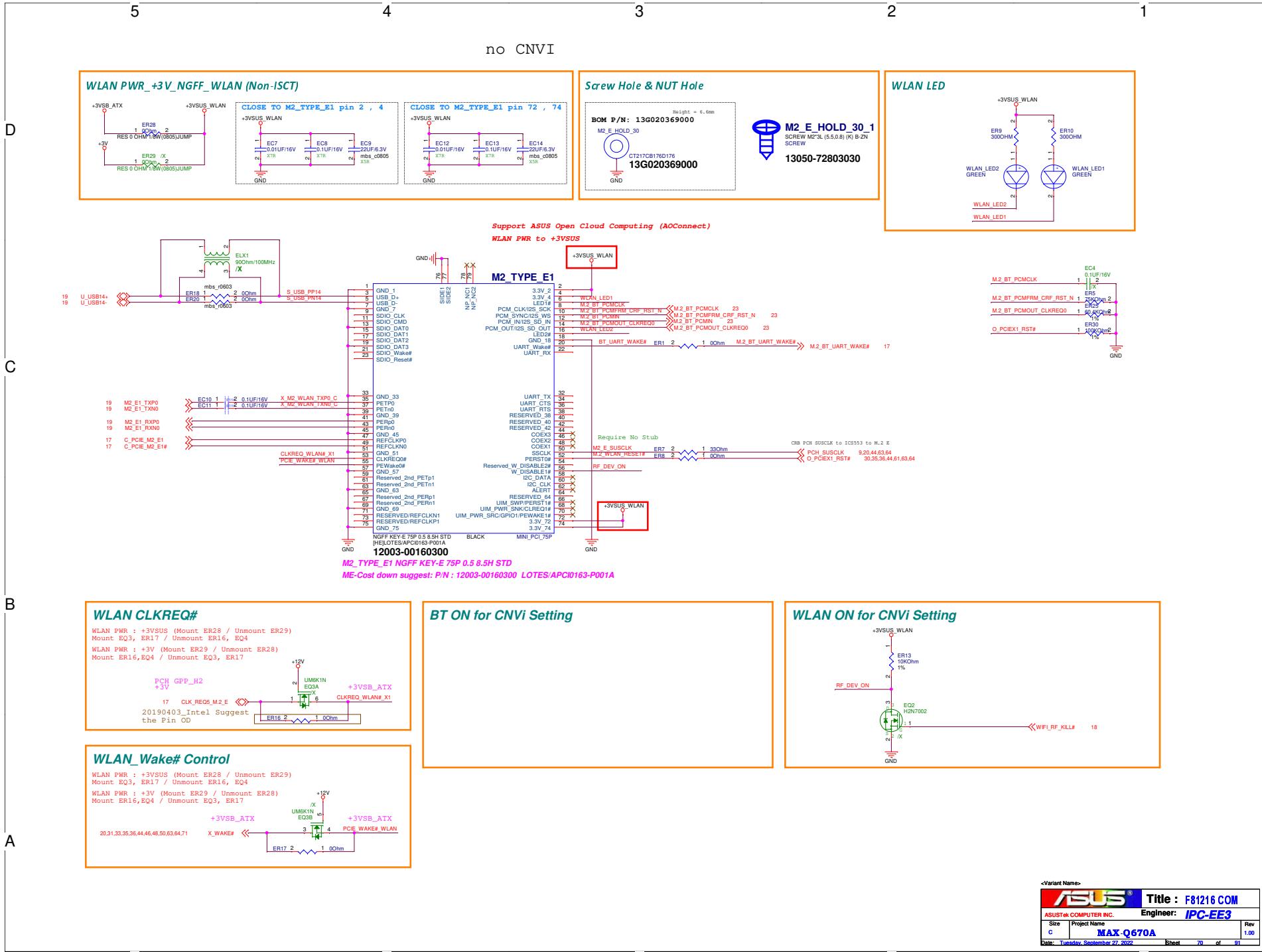


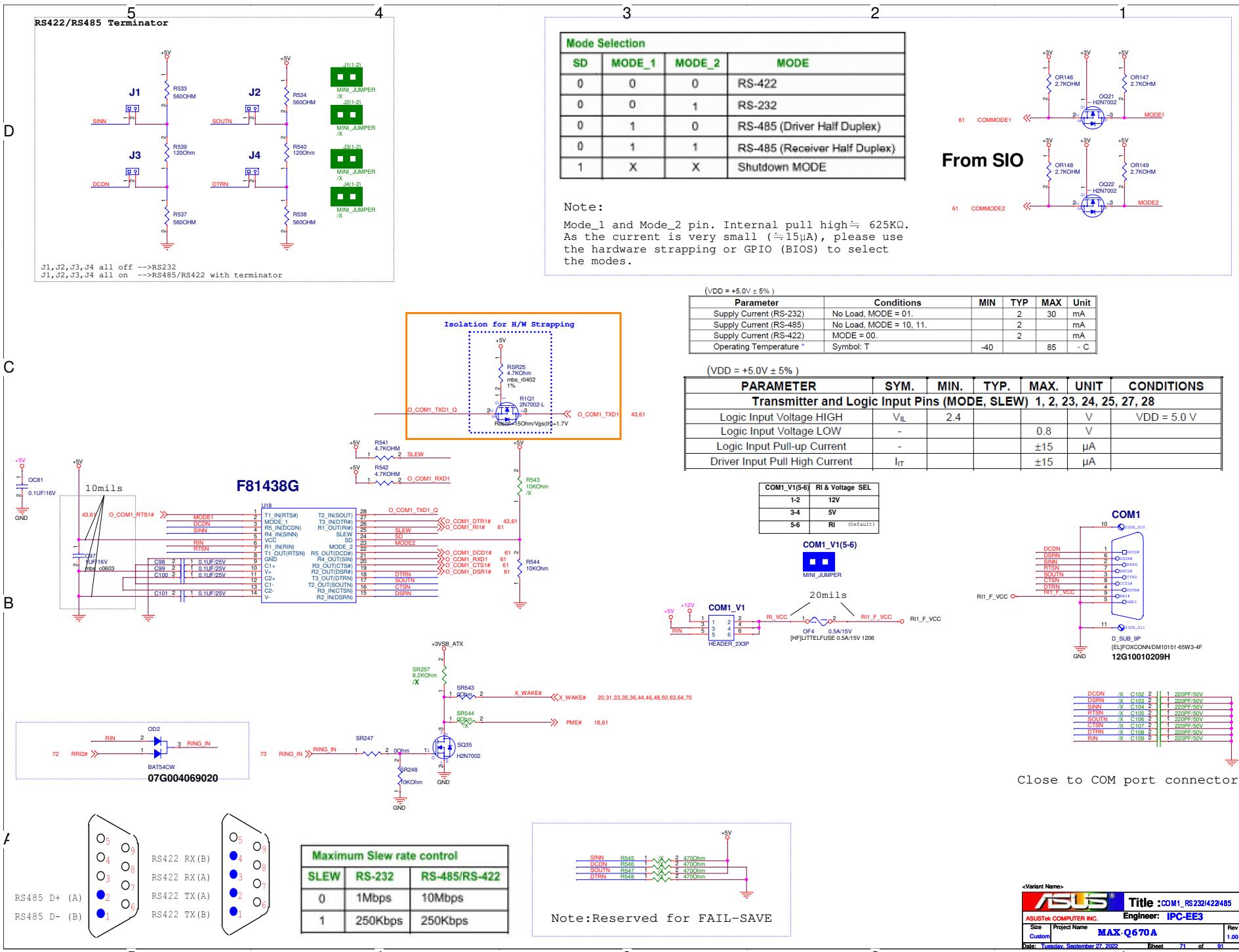


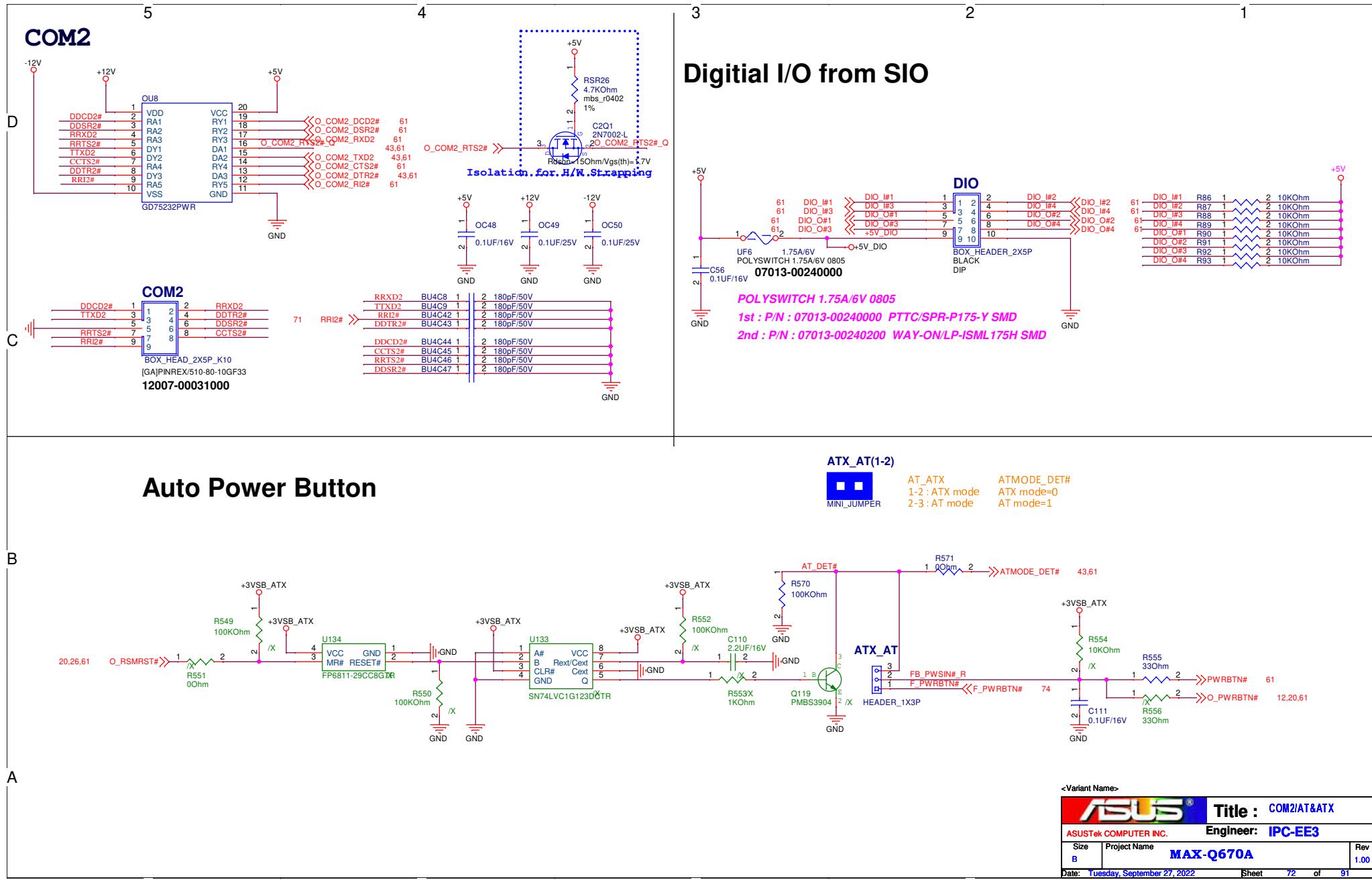


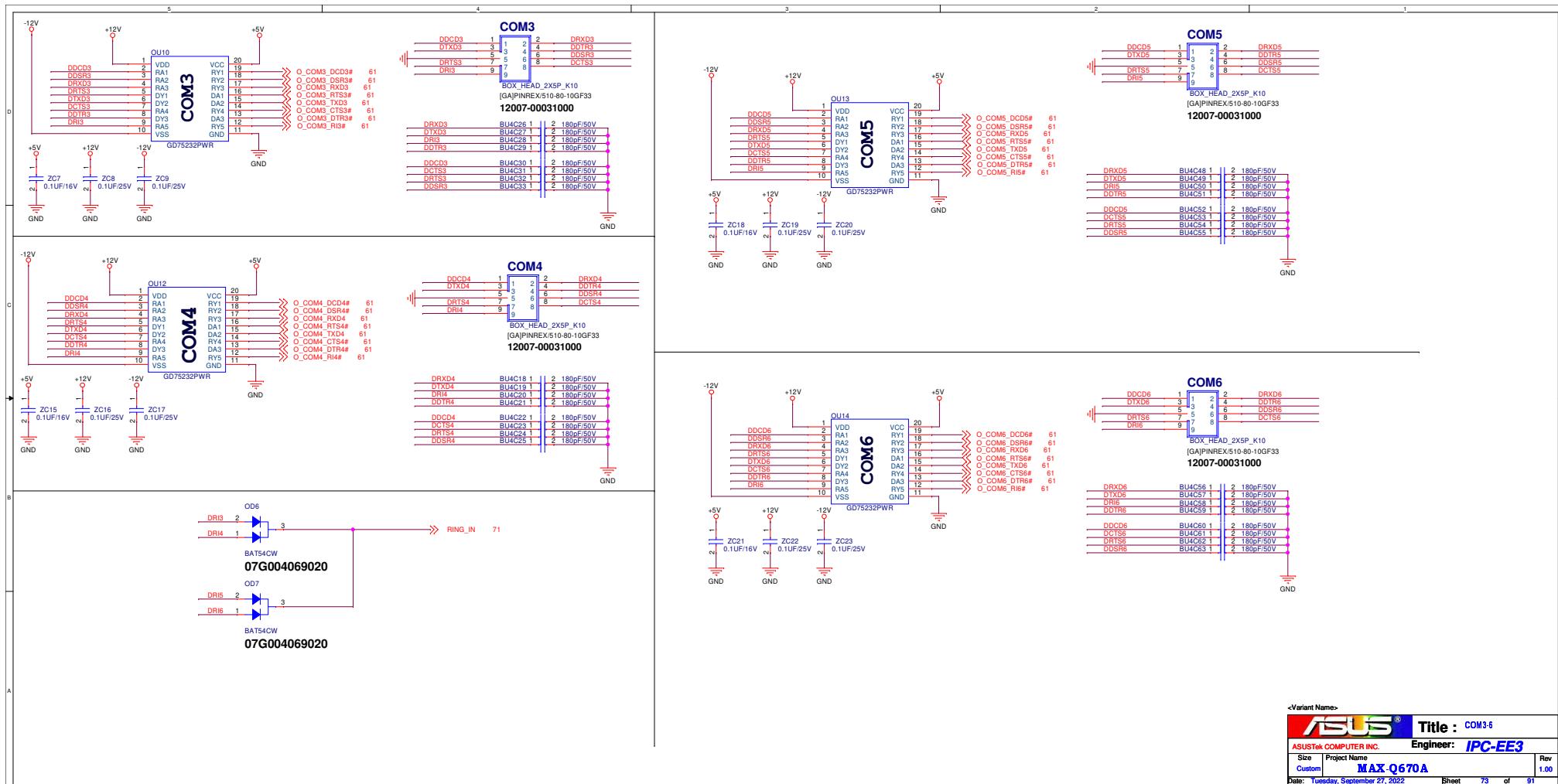


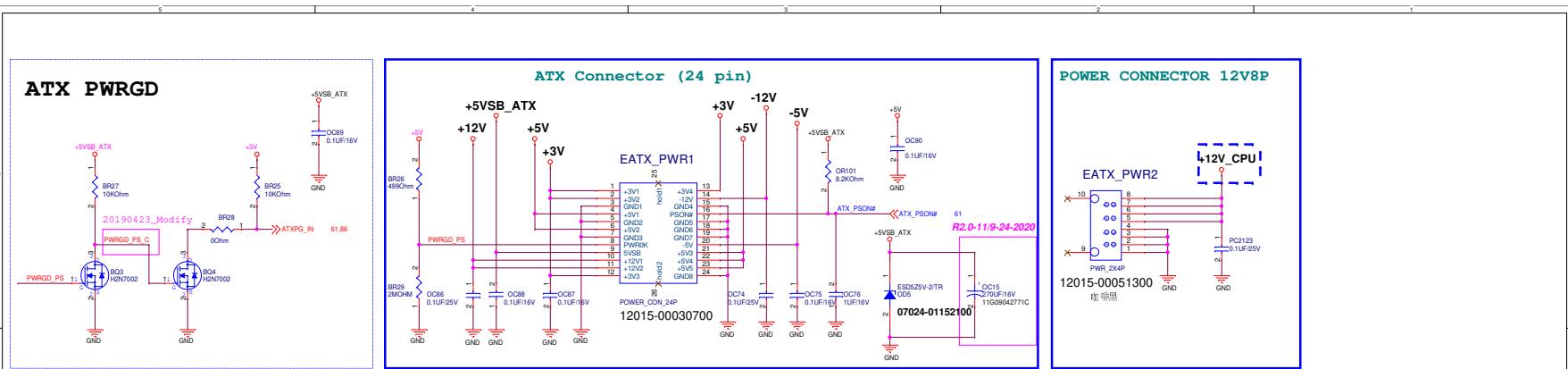




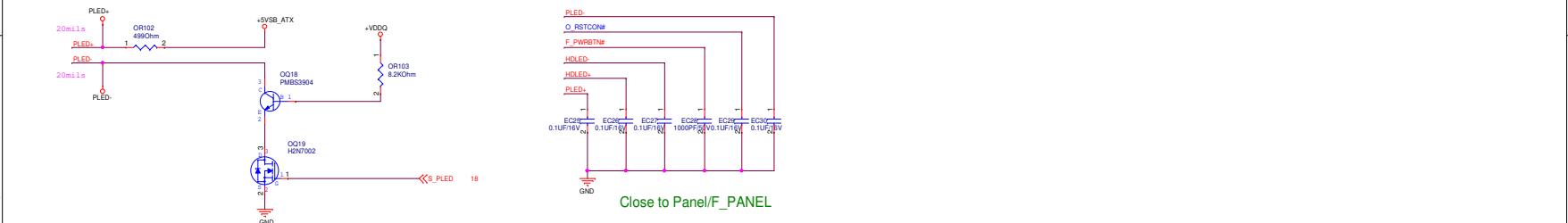
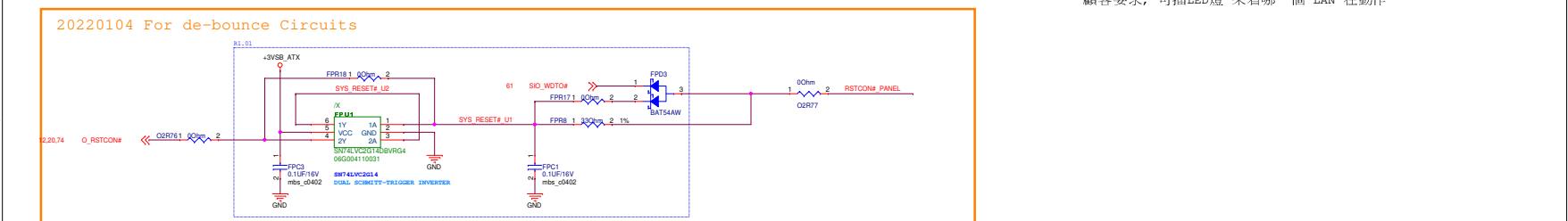
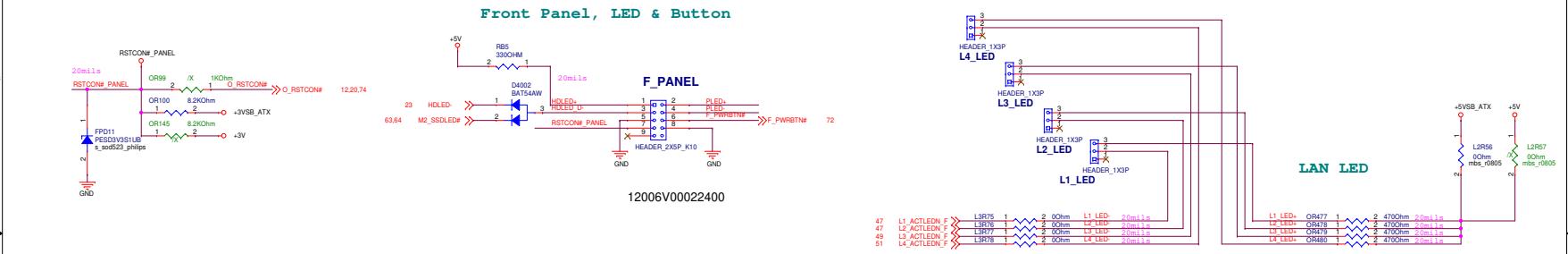


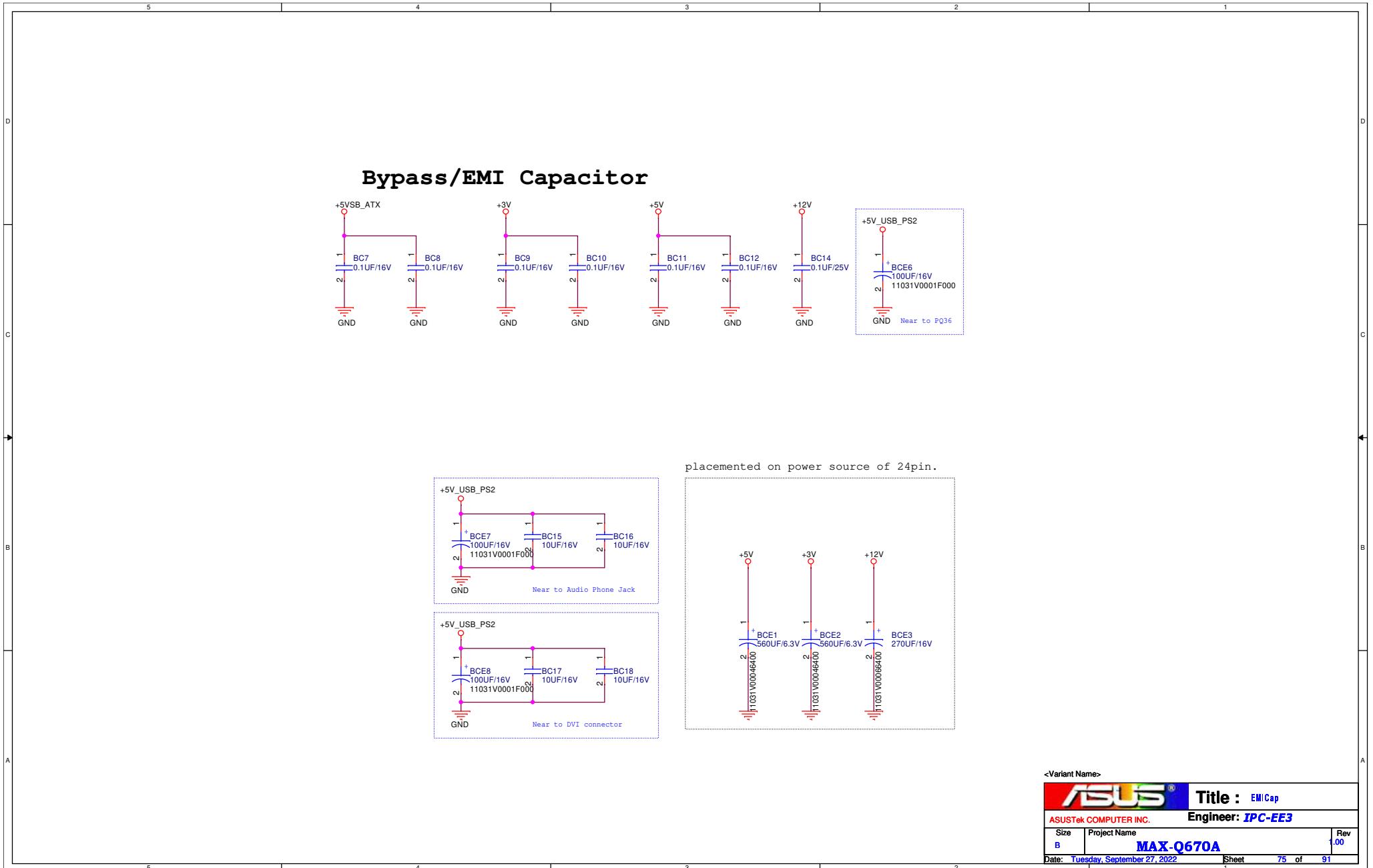


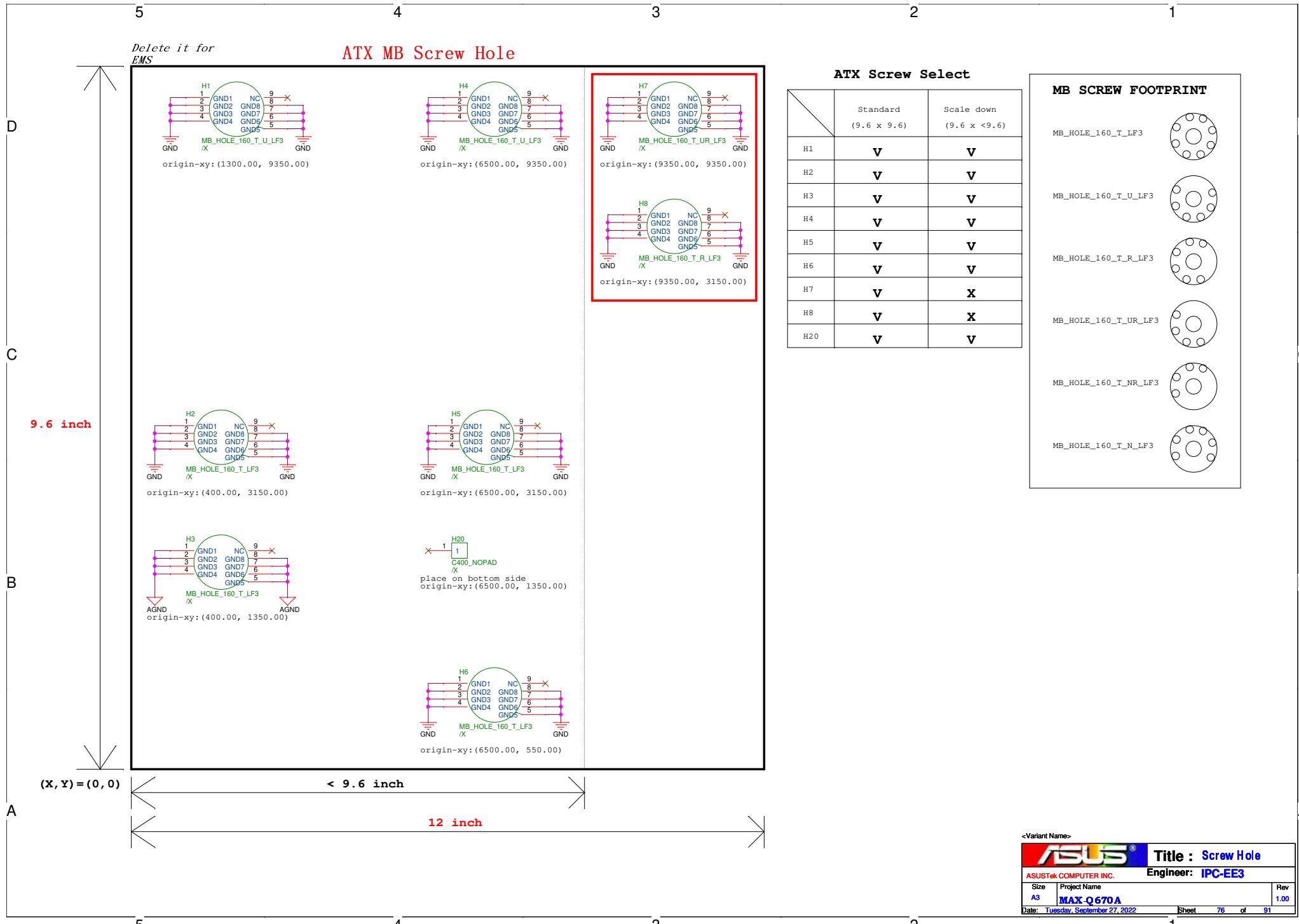




Change the F_PANEL CONN. to add the LAN LED control signals

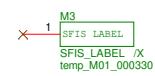




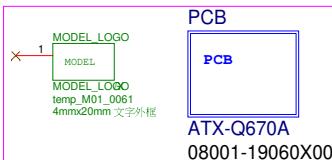


Selling Point

20220104 add no pad_TP for layout request



The U-DIMM Order of Insertion



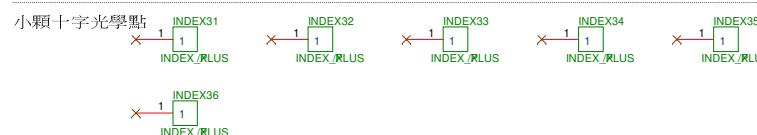
ATX-Q670A R1.00 PCB-08 :

08001-19060100 ATX-Q670A R1.00//GECS 12*9.6,6L(1).1.6,1080
08001-19060200 ATX-Q670A R1.00//TRUSTECH 12*9.6,6L(1).1.6,1080
08001-19060000 ATX-Q670A R1.00//DF 12*9.6,6L(1).1.6,1080

Fiducial Mask (光學點)

大顆十字光學點

光學點需要 6 ~ 10 頭,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除。



2012/09/11

MAX-Q670A : 板外的INDEX40 , INDEX39 , INDEX38 , INDEX37 是多餘的 , remove

Logo

common Logo for all projects



LOGO2
FCC
FCC /X
temp_M01_000348

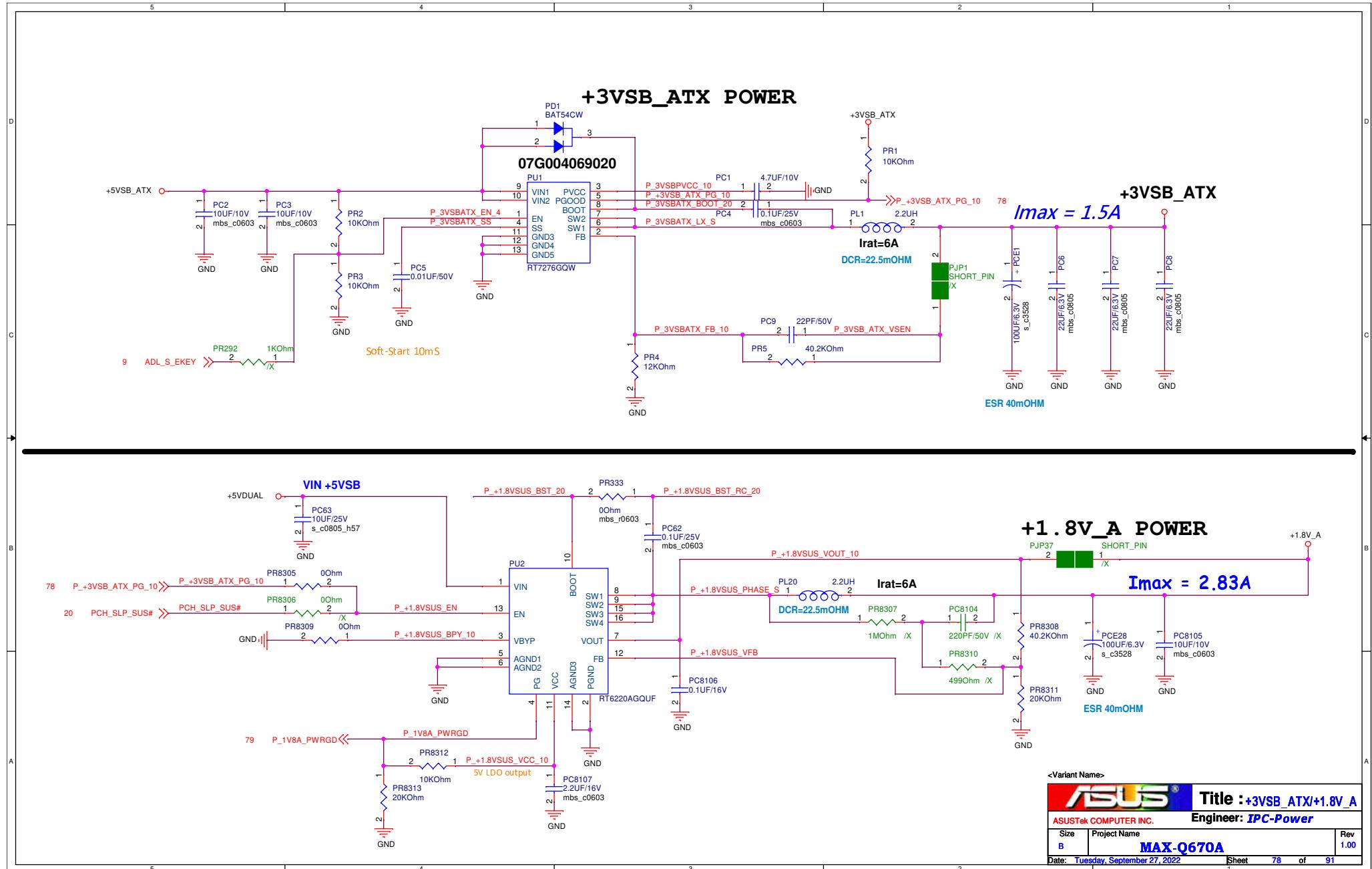


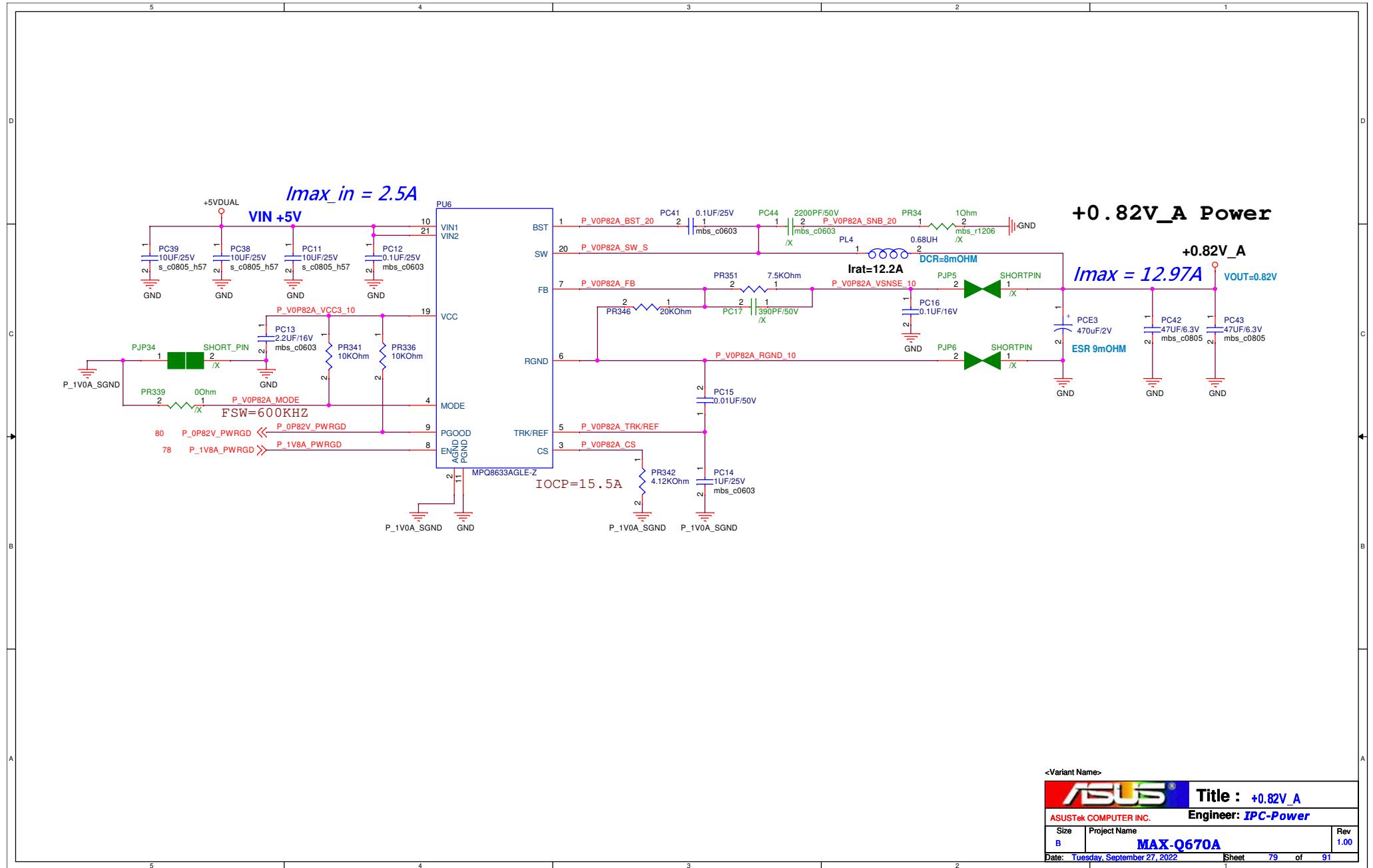
LOGO5
WEEE_LOGO
WEEE_LOGO /X

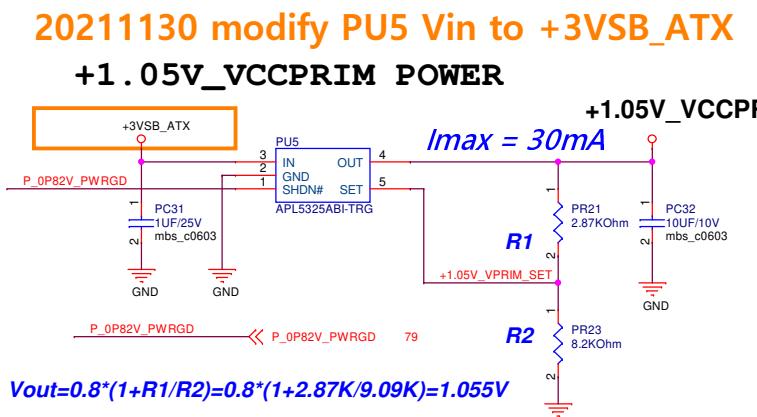
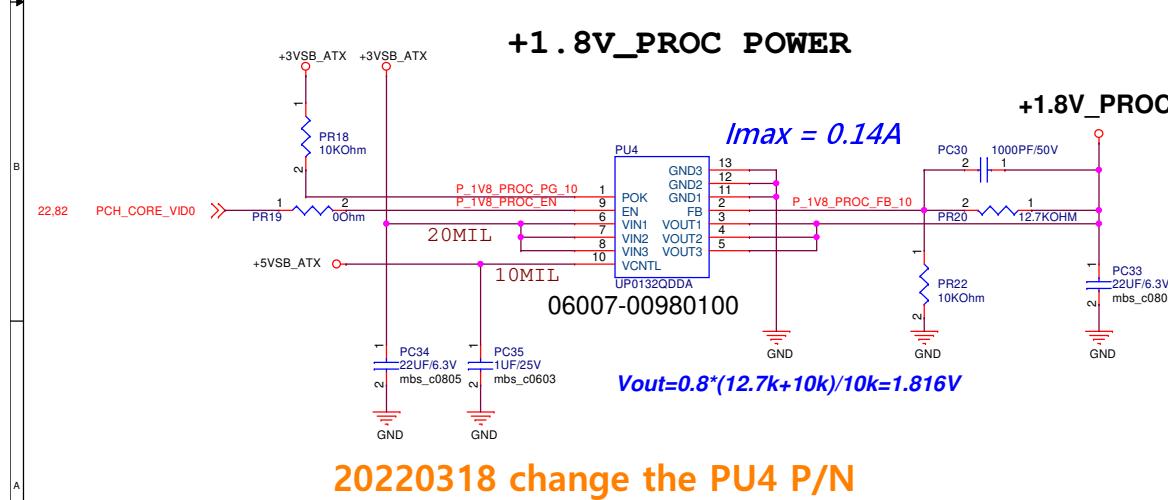
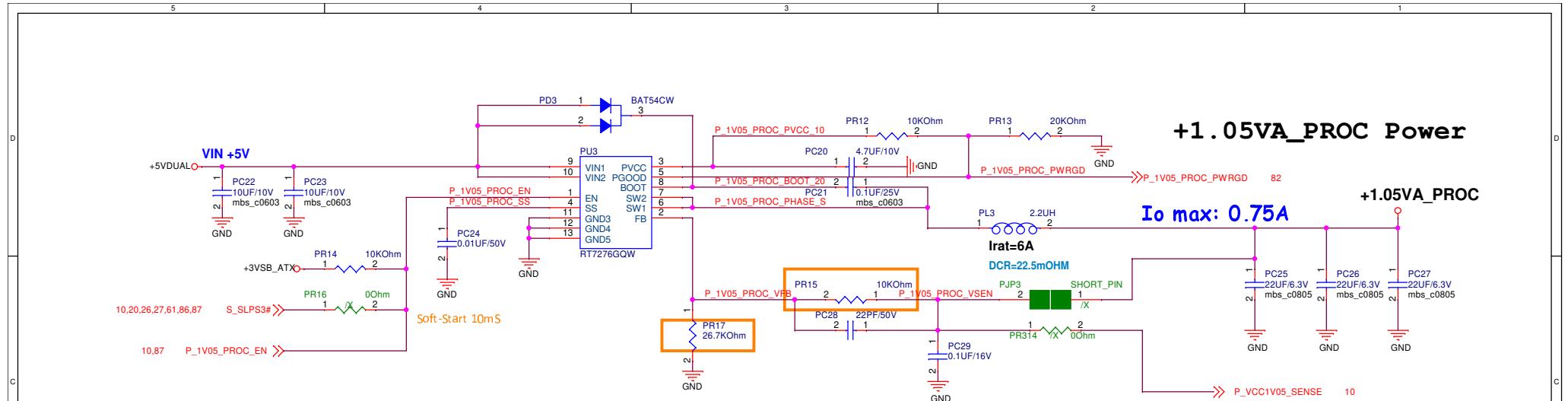
LOGO6
CE
CE /X

LOGO7
PCB MADE IN CHINA
PCB_MADE_IN_CHINA /X

<Variant Name>		
	Title : Selling Point_Logo	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MAX-Q670A	Rev 1.00
Date: Tuesday, September 27, 2022	Sheet 77	of 91



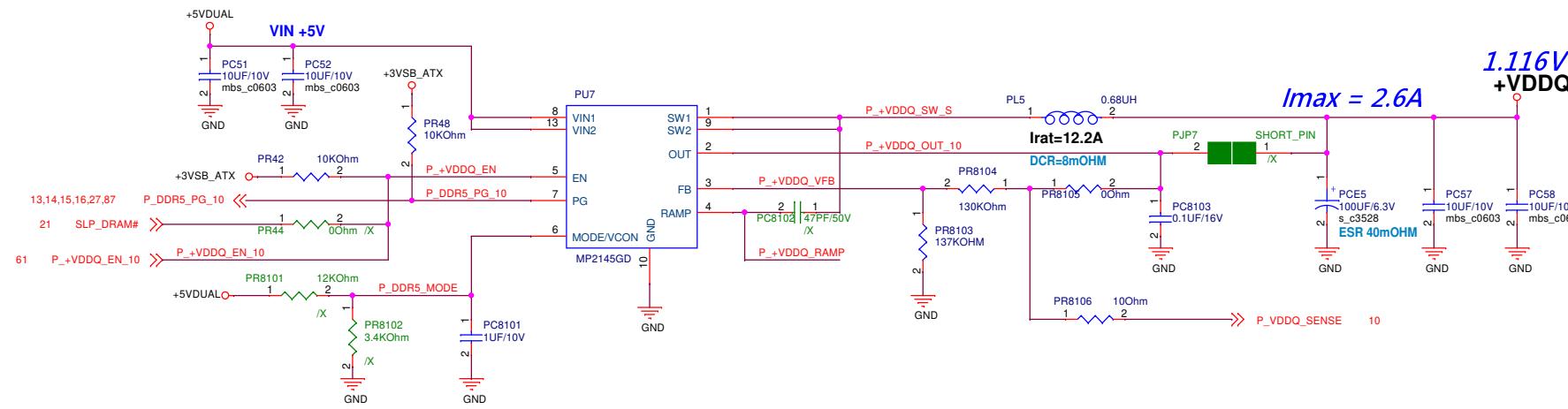
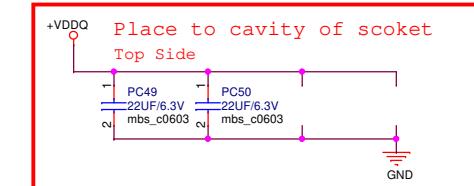
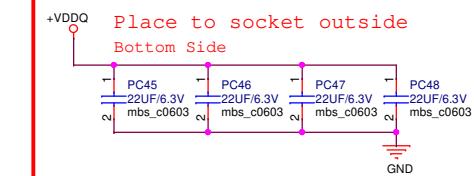




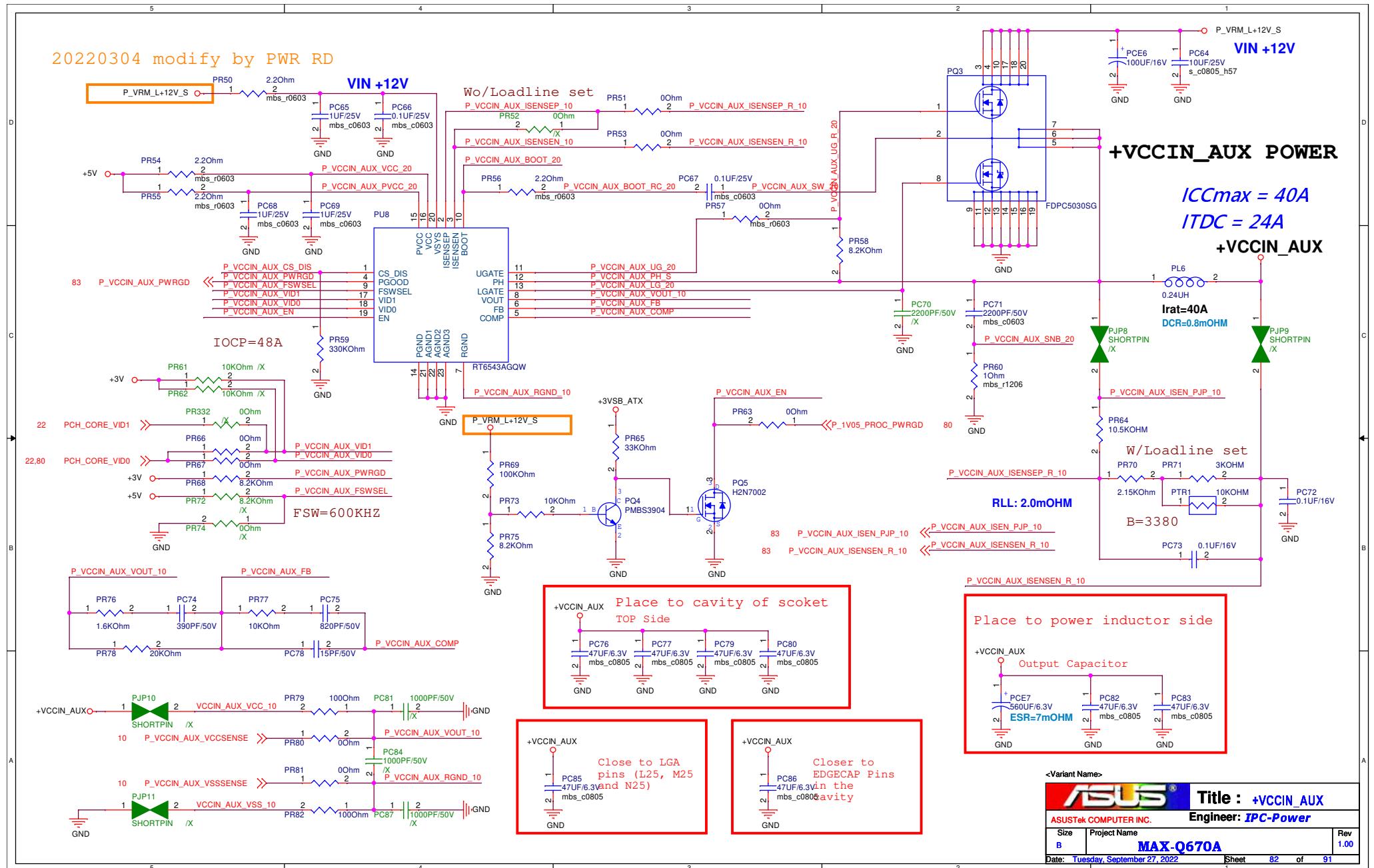
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		ASUSTek COMPUTER INC.	
Size	Project Name	Engineer: IPC-Power	
B	MAX-Q670A		Rev 1.00
Date: Tuesday, September 27, 2022		Sheet 80	of 91

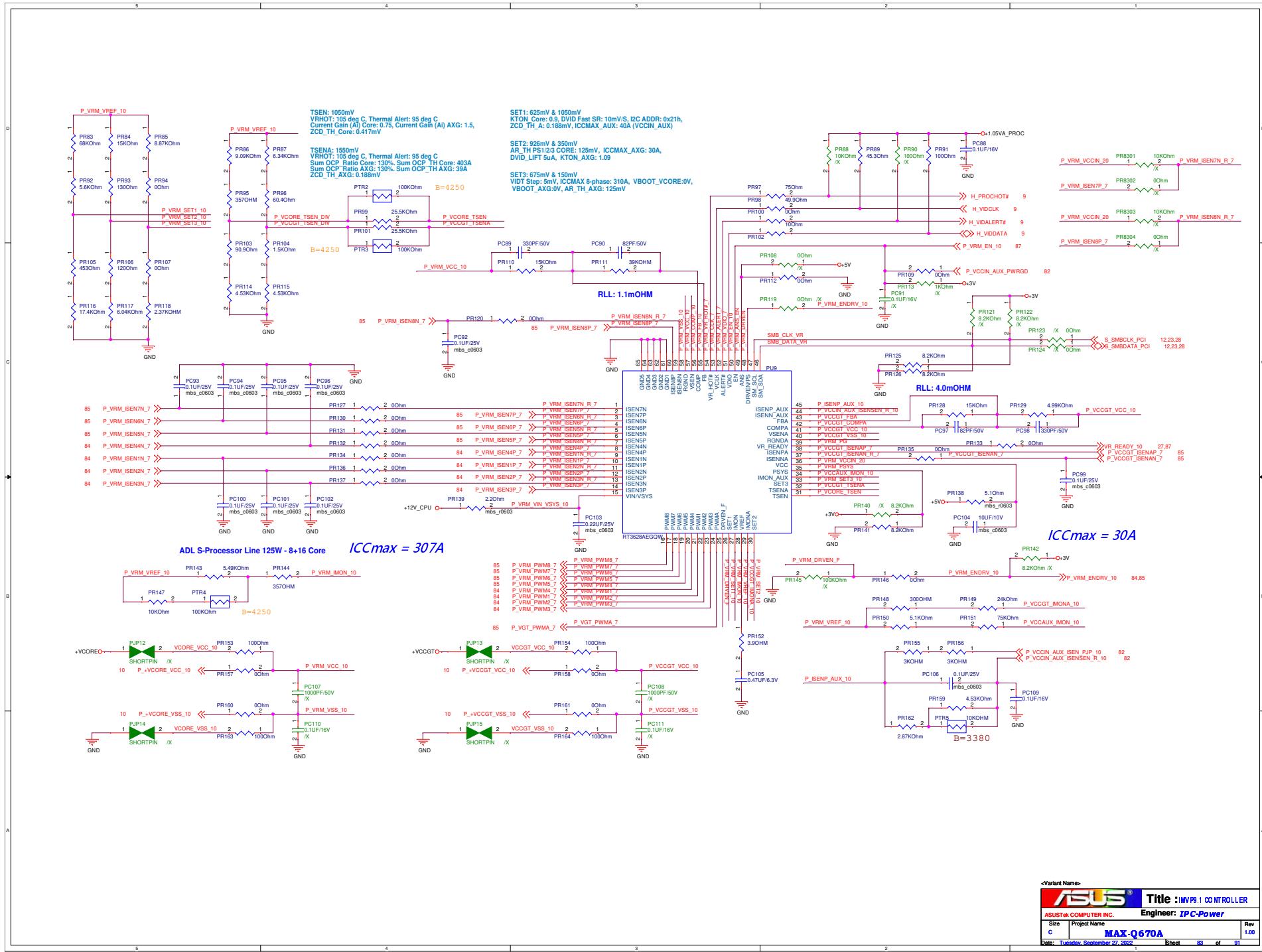
+VPPDDR POWER

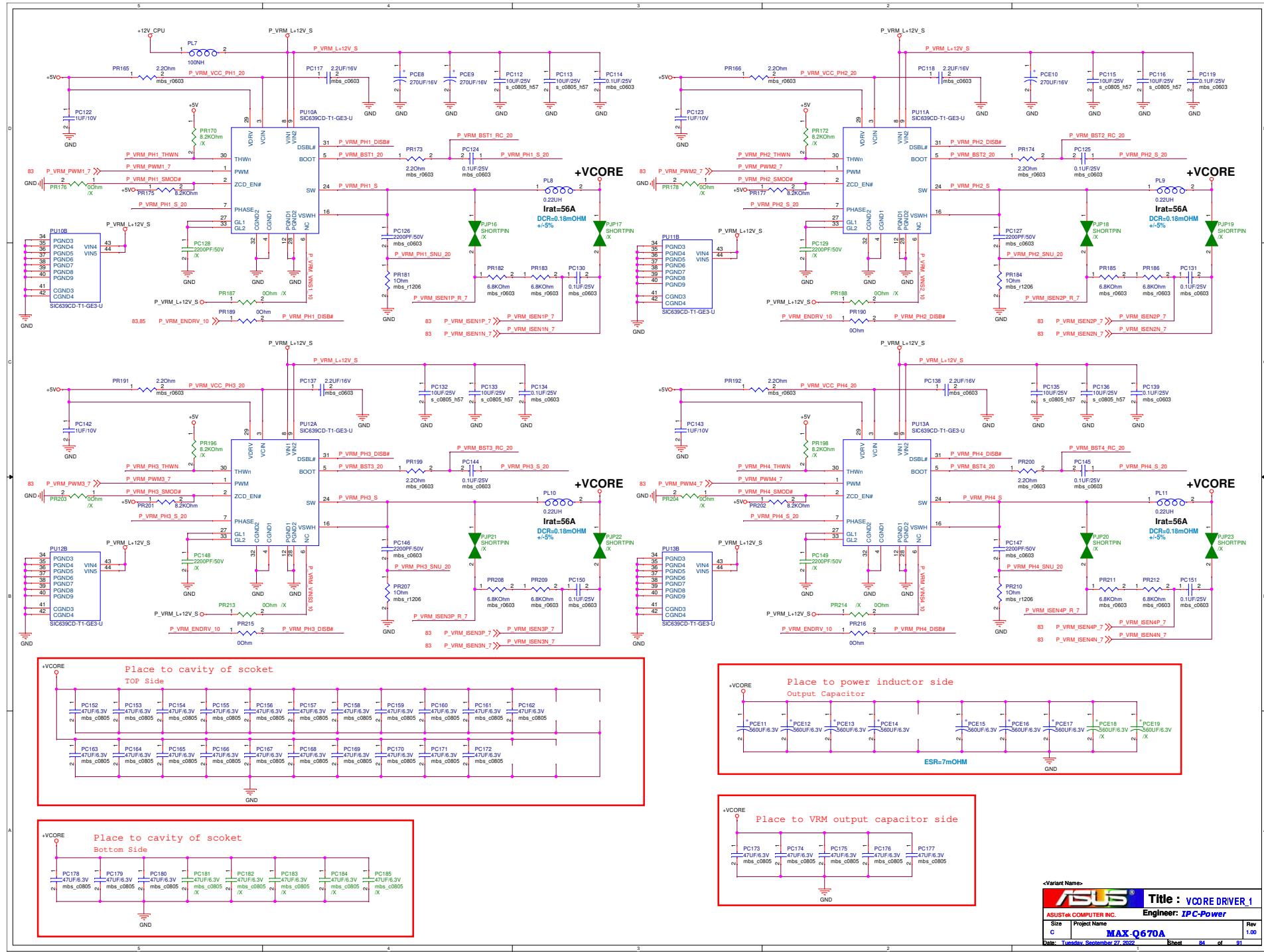
Delete +VPPDDR Power, It is directly powered by DDR5 DIMM.

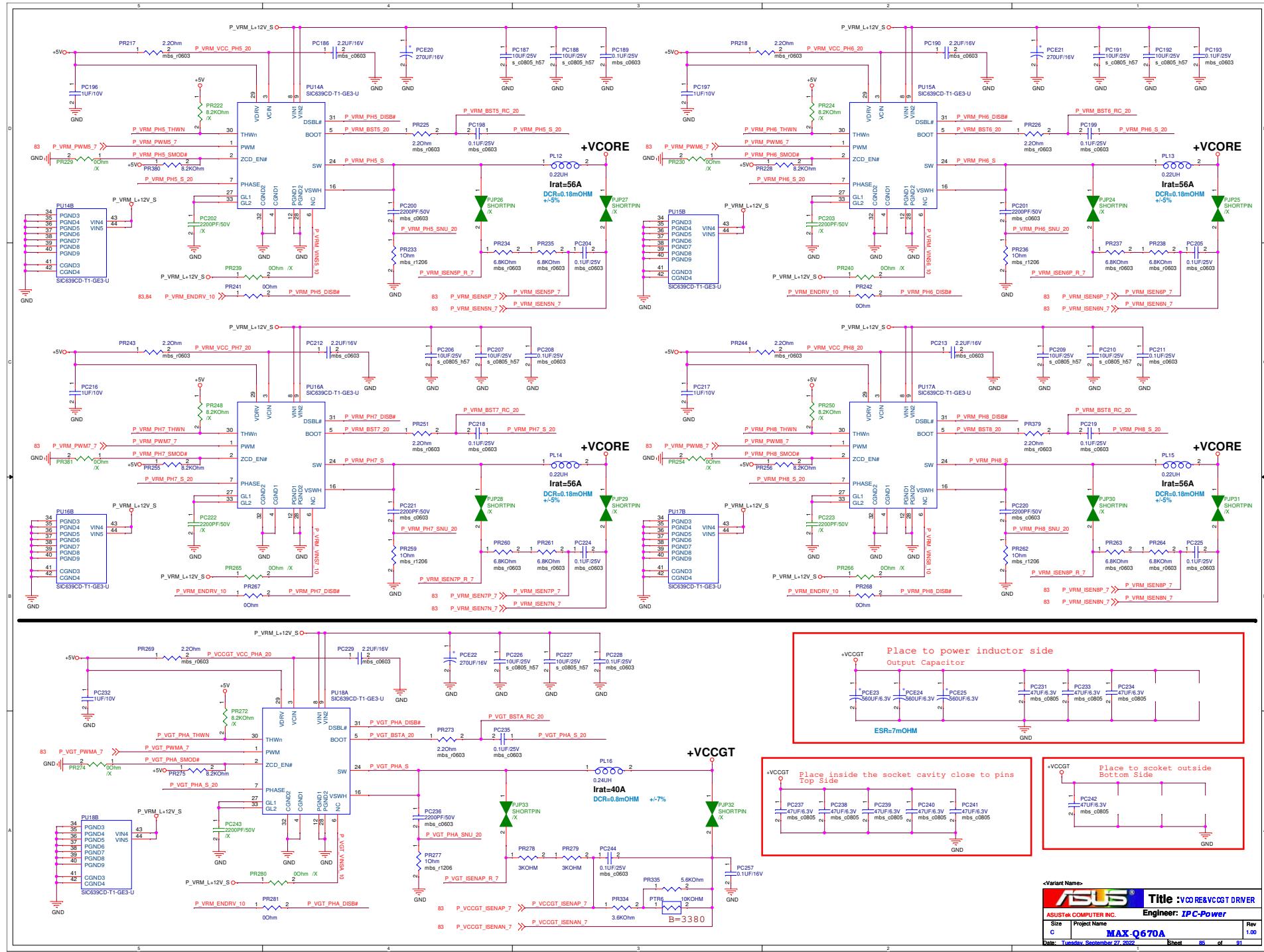


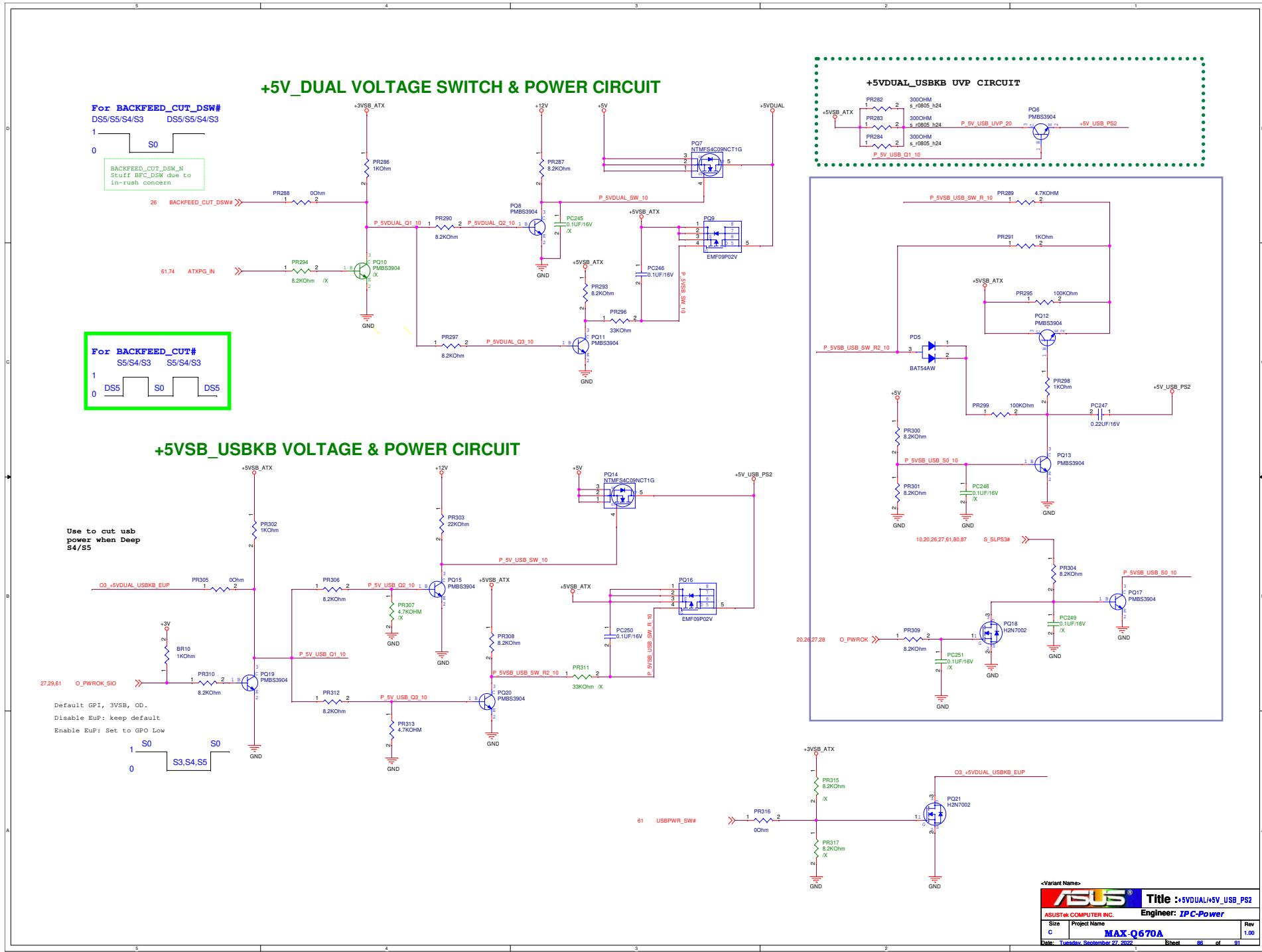
<Variant Name>		Title : +VDDQ	
ASUSTek COMPUTER INC.		Engineer: IPC-Power	
Size	Project Name	Rev 1.00	
B	MAX-Q670A	Date: Tuesday, September 27, 2022	Sheet 81 of 91

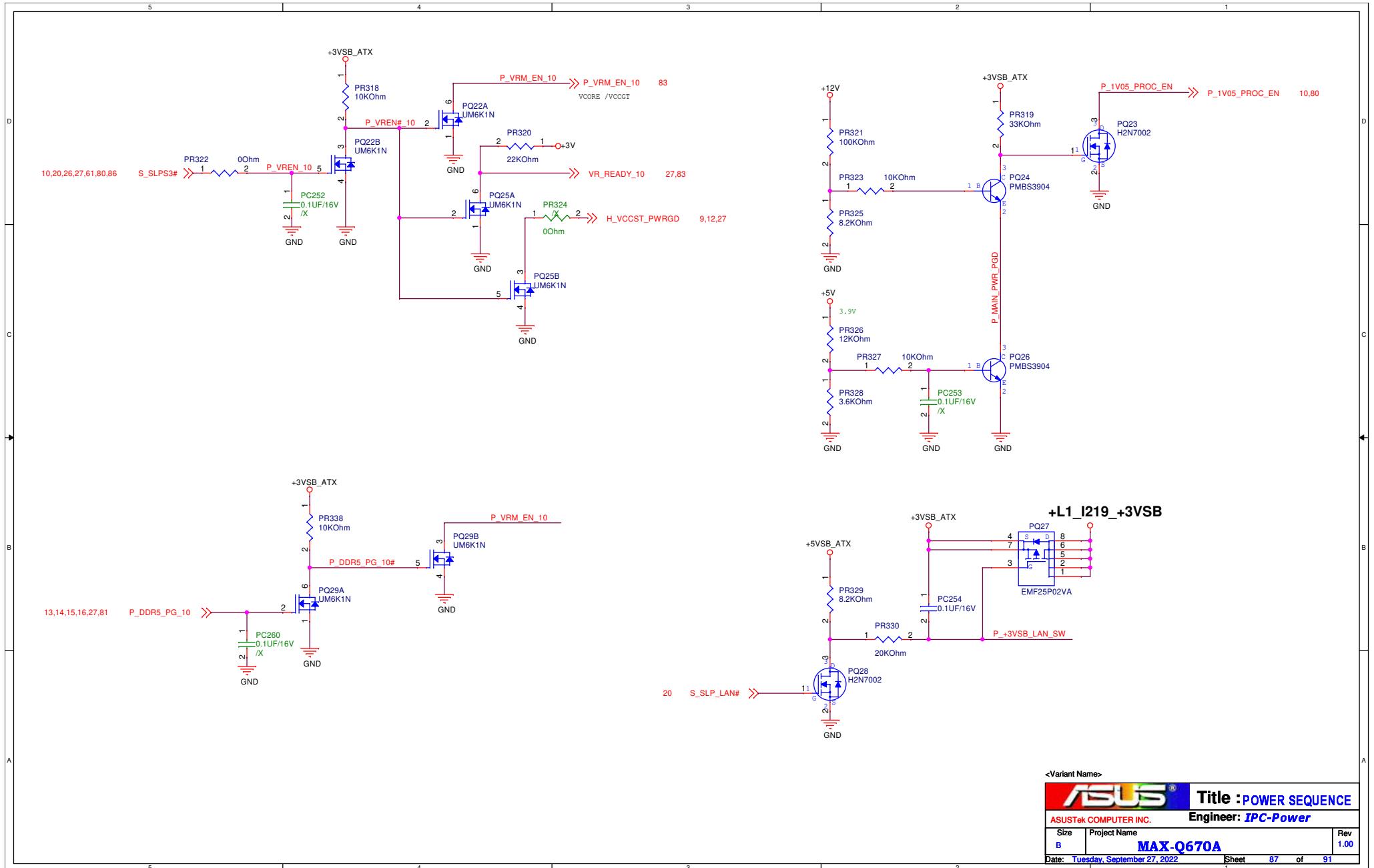












<Variant Name>



Title : POWER SEQUENCE

Engineer: IPC-Power

ASUSTek COMPUTER INC.

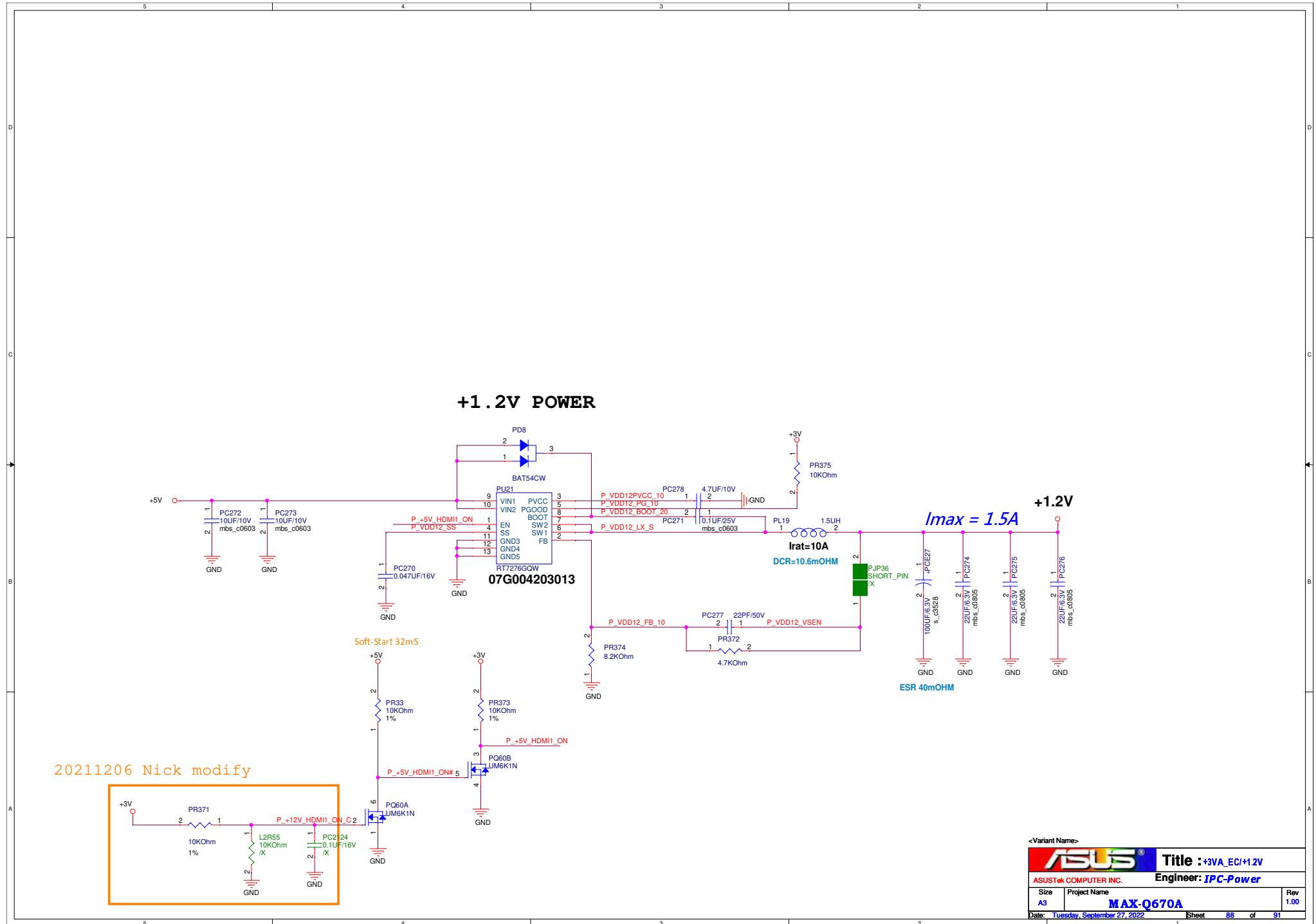
Size Project Name

B MAX-Q670A

Rev 1.00

Date: Tuesday, September 27, 2022

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History 2022/8/8	R1.0
<ul style="list-style-type: none"> * MAX-Q670A V1 release 	
History 2022/8/9	
<ul style="list-style-type: none"> * P17 , add Link CLK_REQ_PCIE16_2_SL4# * P32, modify PCIe Gen3 SW schematic about address pin 	
History 2022/8/14	
<ul style="list-style-type: none"> * P17 , add Link CLK_REQ_PCIE16_2_SL4# * P17 ,CLK REQ_PCIE16_2_SL1# :CLK REQ_PCIE16_2_SL4# , OR409 OR410 損留不工作 * P17 , modify net name CLK_REQ5.M.2_R --> CLK_REQ5.M.2_E 	
History 2022/8/15	
<ul style="list-style-type: none"> * P19 , modify USB3 net name (统一規則命名) * P32 , PCIe Slot RXE=15 add cap. * P61 , FAN5 FANOUT 損留 LVDS PWM 使用 -->net: SIO_LVDS_PWM 	
History 2022/8/18	
<ul style="list-style-type: none"> * P32 , modify QN03 , JY53_PRNT_A -->JY53_PRNT_B & JY53_PRNT_B -->JY53_PRNT_B 	
History 2022/8/19	
<ul style="list-style-type: none"> * P59 ULS320 修正地線位置 * P59 add UD5503 for layout placement needed * 修正 M.2 硬孔元件 M.2 2242/2280 SSD (M-key) CPU side M.2 2242/2280 SSD (M-key) PCH side M.2 2230 (B-key) M.2 3042/3052 /2242 SSD (B-key) * 修正 SATA Connector * 修正 RTC battery +RTC Connector (修改為直立式 Battery 之 connector) * P60 , U3CR6,U3CR7,U3CR2 沒不工作 (板測健 	
History 2022/8/22	
<ul style="list-style-type: none"> * P32 , Gen 5 SW 使用 AI 料件, 不需多加 smttrig 觸發路徑 * P32 , 加入mode/address setting 說明解說 * P40 , QD4105 插件 --> 0TQD2807630 ; 電瓶座位不回, 露底建議 A21045 * P60 , P12_CEC 相關, remove 系本接腳, 電瓶座建議 FU: Add U3TR61,U3TR61,U3CR2 * P65 , Remove SATA ESD 隔離接建議 * P18,P66 , Remove DC_FAM 保固 4 周的建議 	
History 2022/8/23	
<ul style="list-style-type: none"> * P60 , P10_LC_LN04 因 LKX PU 3V , 損留 PU 5V & PD * P32 , S8605 損留 MOS LVDS 面板已有 PU 3V , MOS 共用 S01 , 故不再做跳接 	
History 2022/8/29	
<ul style="list-style-type: none"> * P76, remove H5, H21,H22 (多出不需要) 	
History 2022/8/30	
<ul style="list-style-type: none"> * Layout 亂 HSMAP : 1. UD5503.1 reassigned from S_USB_PP12 to S_USB_PN12 2. UD5503.2 reassigned from S_USB_PP12 to S_USB_PN12 3. UD5503.4 reassigned from S_USB_PP11 to S_USB_PN11 4. UD5503.5 reassigned from S_USB_PP11 to S_USB_PN11 5. UD5503.6 reassigned from S_USB_PP11 to S_USB_PN11 6. UD5503.7 reassigned from S_USB_PP11 to S_USB_PN11 7. UD5503.8 reassigned from S_USB_PP11 to S_USB_PN11 8. UD5503.9 reassigned from S_USB_PP12 to S_USB_PN12 9. UD5505.1 reassigned from S_USB_PP9 to S_USB_PN9 10. UD5505.2 reassigned from S_USB_PP9 to S_USB_PN9 11. UD5505.6 reassigned from S_USB_PP9 to S_USB_PN8 12. UD5505.7 reassigned from S_USB_PP9 to S_USB_PN8 13. UD8314.4 reassigned from S_U3RXNDP7 to S_U3RXNDP7 14. UD8314.5 reassigned from S_U3RXNDP7 to S_U3RXNDP7 15. UD8314.6 reassigned from S_U3RXNDP7 to S_U3RXNDP7 16. UD8314.7 reassigned from S_U3RXNDP7 to S_U3RXNDP7 17. UD85508.1 reassigned from S_U3RXNDP7 to S_U3RXNDP7 18. UD85508.2 reassigned from S_U3RXNDP7 to S_U3RXNDP7 19. UD85508.3 reassigned from S_U3RXNDP7 to S_U3RXNDP7 20. UD85508.9 reassigned from S_U3RXNDP7 to S_U3RXNDP7 21. UD85509.1 reassigned from S_U3RXNDP7 to S_U3RXNDP7 22. UD85509.2 reassigned from S_U3RXNDP7 to S_U3RXNDP7 23. UD85509.8 reassigned from S_U3RXNDP7 to S_U3RXNDP7 24. UD85509.9 reassigned from S_U3RXNDP7 to S_U3RXNDP7 25. UL46011.1 reassigned from U3_0J1XKNDP7_JUE_KR4 to U3_0J1XKNDP7_JUE_KR4 26. UL46011.2 reassigned from U3_0J1XKNDP7_JUE_KR4 to U3_0J1XKNDP7_JUE_KR4 27. UL46011.3 reassigned from S_U3RXNDP7 to S_U3RXNDP7 28. UL46011.4 reassigned from S_U3RXNDP7 to S_U3RXNDP7 29. UD320.1 reassigned from U3_U3TXNDP7 to U3_U3TXNDP7 30. UD320.2 reassigned from U3_U3TXNDP7 to U3_U3TXNDP7 31. UD320.3 reassigned from U3_U3TXNDP7 to U3_U3TXNDP7 32. UD320.4 reassigned from U3_U3TXNDP7 to U3_U3TXNDP7 33. UD85509.1 reassigned from S_U3TXNDP3 to S_U3TXND3_RB 34. UD85509.2 reassigned from S_U3TXNDP3 to S_U3TXND3 35. UD85509.3 reassigned from S_U3TXNDP3 to S_U3TXND3 36. UD85509.4 reassigned from U3_U3TXNDP3_RB to U3_U3TXNDP3_RB 	
<ul style="list-style-type: none"> * P8211 插改為下伸 (follow spec. Power VCORE 相應) * P314P33 , remove Slot RX AC cap . intel spec 176nF - 265nF including tolerance * P17,OR409,OR410 改為上伸 	
History 2022/9/2	
<ul style="list-style-type: none"> * P23 , 損留 S8260 , 預防漏電 	
History 2022/9/4	
<ul style="list-style-type: none"> * P65 , SATA Connector 改回 佈 V M, follow MB rule * P57 未改 for layout 1. UD5505.1 reassigned from S_U3RXND3 to S_U3RXND3 2. UD85508.2 reassigned from S_U3RXNDP3 to S_U3RXND3 3. UD85509.1 reassigned from S_U3RXNDP7 to S_U3RXND3 4. UD85509.9 reassigned from S_U3RXND3 to S_U3RXND3 	
History 2022/9/5	
<ul style="list-style-type: none"> * P90 , update power net for check 	
<div style="border: 1px solid black; padding: 5px; text-align: center;">  Title : History_01 ASUSTEK COMPUTER INC. Engineer: IPC-E83 Date: 2022-08-24 10:21:35 Page: 100 / 100 </div>	

