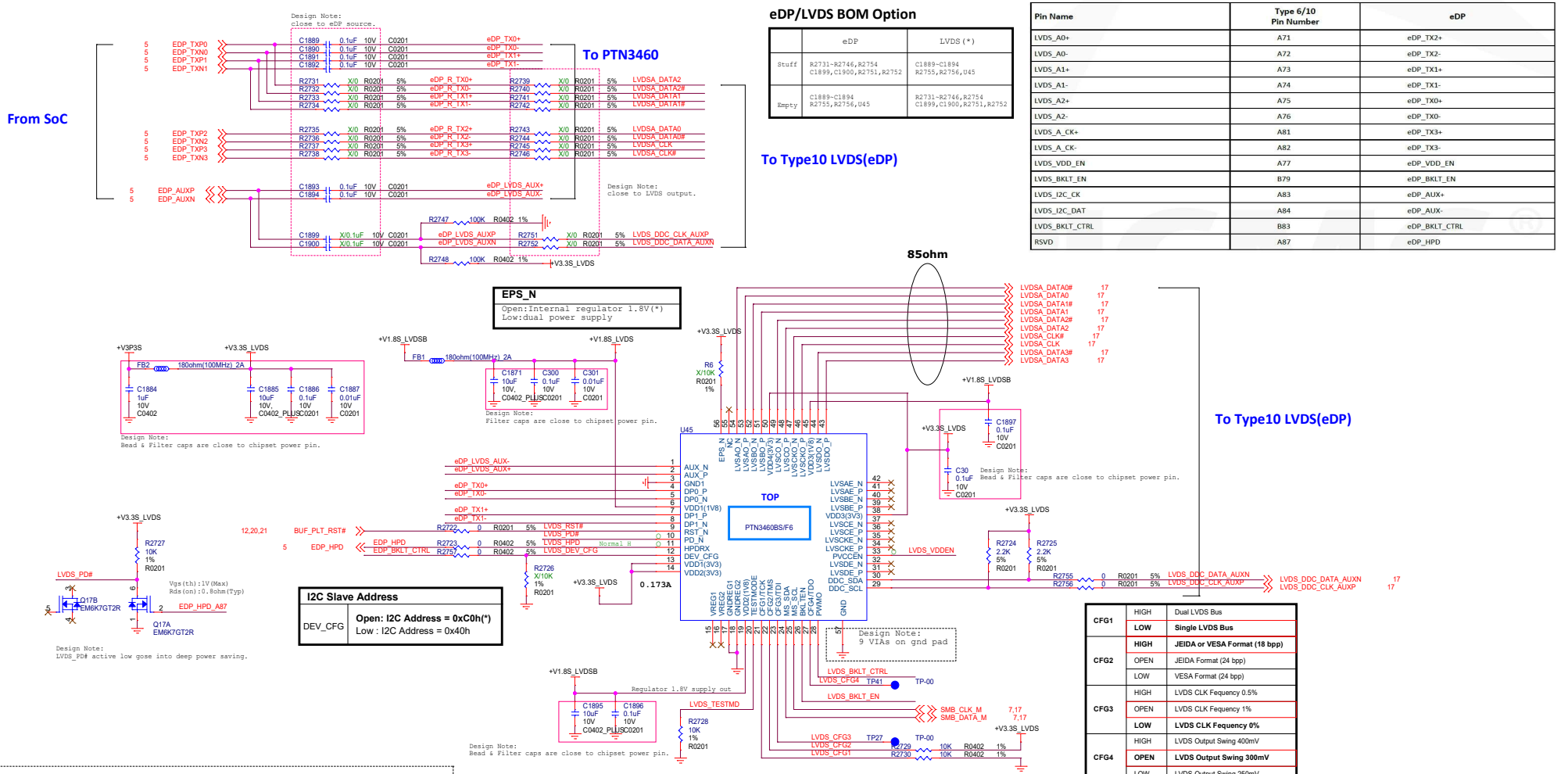
eDP to LVDS_PTN3460



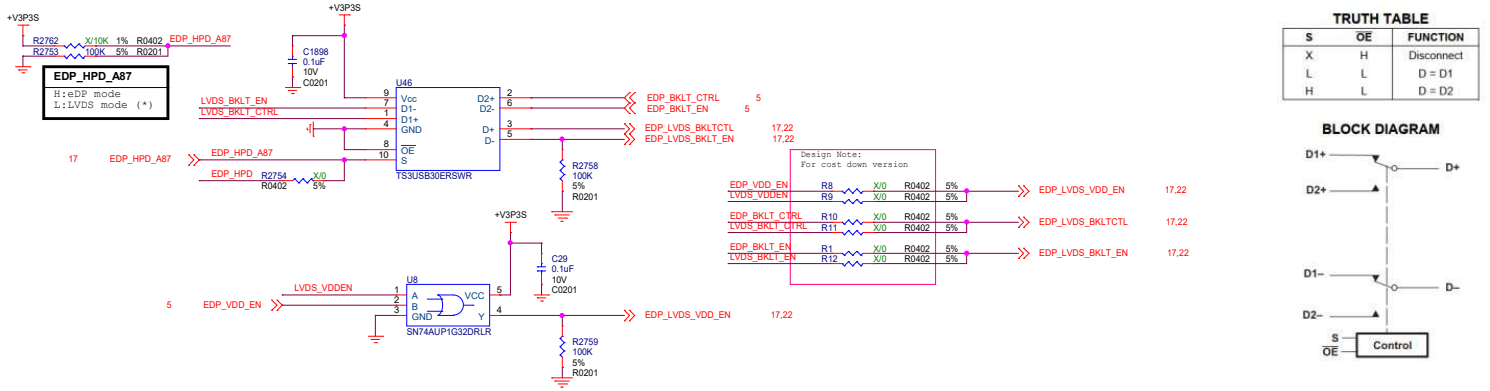
eDP/LVDS BOM Option

	eDP	LVDS(*)
Stuff	R2731-R2746,R2754 C1899,C1900,R2751,R2752	C1889-C1894 R2755,R2756,U45
Empty	C1889-C1894 R2755,R2756,U45	R2731-R2746,R2754 C1899,C1900,R2751,R2752

Pin Name	Type 6/10 Pin Number	eDP
LVDS_A0+	A71	eDP_TX2+
LVDS_A0-	A72	eDP_TX2-
LVDS_A1+	A73	eDP_TX1+
LVDS_A1-	A74	eDP_TX1-
LVDS_A2+	A75	eDP_TX0+
LVDS_A2-	A76	eDP_TX0-
LVDS_A_CK+	A81	eDP_TX3+
LVDS_A_CK-	A82	eDP_TX3-
LVDS_VDD_EN	A77	eDP_VDD_EN
LVDS_BKLT_EN	B79	eDP_BKLT_EN
LVDS_I2C_CK	A83	eDP_AUX+
LVDS_I2C_DAT	A84	eDP_AUX-
LVDS_BKLT_CTRL	B83	eDP_BKLT_CTRL
RSVD	A87	eDP_HPD

CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

eDP/LVDS Backlight Switch



TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM

<Core Design>

AAEON Technology INC.

Title: eDP to LVDS

Size: C | Document Number: NANOCOM-WHU | Rev: B0.1_0_0

Date: Thursday, October 29, 2020 | Sheet 22 of 35