NCT6791D

Nuvoton LPC I/O

(For ASUS Only)

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1. GENERAL DESCRIPTION

The NCT6791D is a member of Nuvoton's Super I/O product line. The NCT6791D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6791D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6791D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6791D provides two high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6791D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6791D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6791D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6791D supports the Intel® PECI (Platform Environment Control Interface) and AMD® SB-TSI interface. The NCT6791D supports AMD® CPU power on sequence, and it also supports Intel® Deep Sleep Well glue logic to help customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6791D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. It also supports two-color LED control to indicate system power states. The NCT6791D supports Consumer IR function for remote control purpose. It also supports Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6791D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Specification 1.1
Support AMD power on sequence
Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Single 24-MHz or 48-MHz clock input
Support selective pins of 5 V tolerance

UART

Two high-speed, 16550-compatible UART with 16-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

Compatible with IBM® parallel port
Support PS/2-compatible bi-directional parallel port
Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
Enhanced printer port back-drive current protection

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset
12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system

Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode

Support Current Mode (dual current source) temperature sensing method

Fourteen voltage inputs (CPUVCORE, VCOREREFIN, VIN0~7, 3VCC, AVCC, 3VSB and VBAT)

Five fan-speed monitoring inputs

Five fan-speed controls

Dual mode for fan control (PWM and DC) for SYSFANOUT

Built-in case-open and CPU socket occupied detection circuit

Programmable hysteresis and setting points for all monitored items

Issue SMI#, OVT# (Over-temperature) to activate system protection

Nuvoton Health Manager support

Provide I^2C master / slave interface to read / write registers

CIR and IR (Infrared)

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR, including CIRTX, CIRRX, CIRRXWB

General Purpose I/O Ports

GPIO0 ~ GPIO8 programmable general purpose I/O ports

Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions

Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys

Mouse Wake-Up by programmable buttons

OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification

Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement
Fading LED driver control for power status and diagnostic indications

Intel Deep Sleep Well (DSW) Glue Logic

Support Deep Sleep Well (DSW) Glue Logic

AMD® CPU Power on Sequence

Support AMD® CPU power on sequence

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

- 3.3 voltage

Package

128-pin LQFP
Green

3. BLOCK DIAGRAM

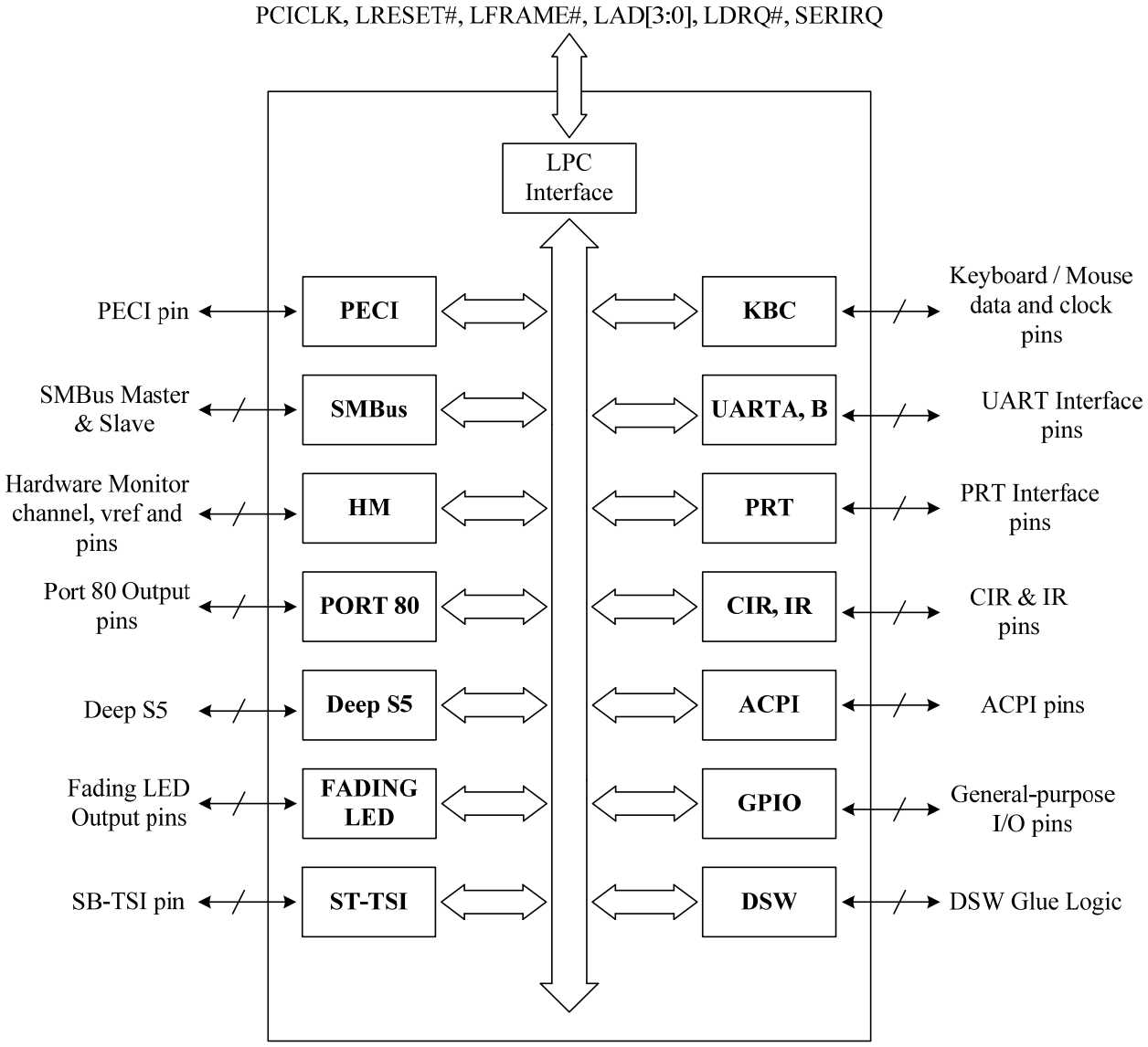

Figure 3-1 NCT6791D Block Diagram

4. PIN LAYOUT

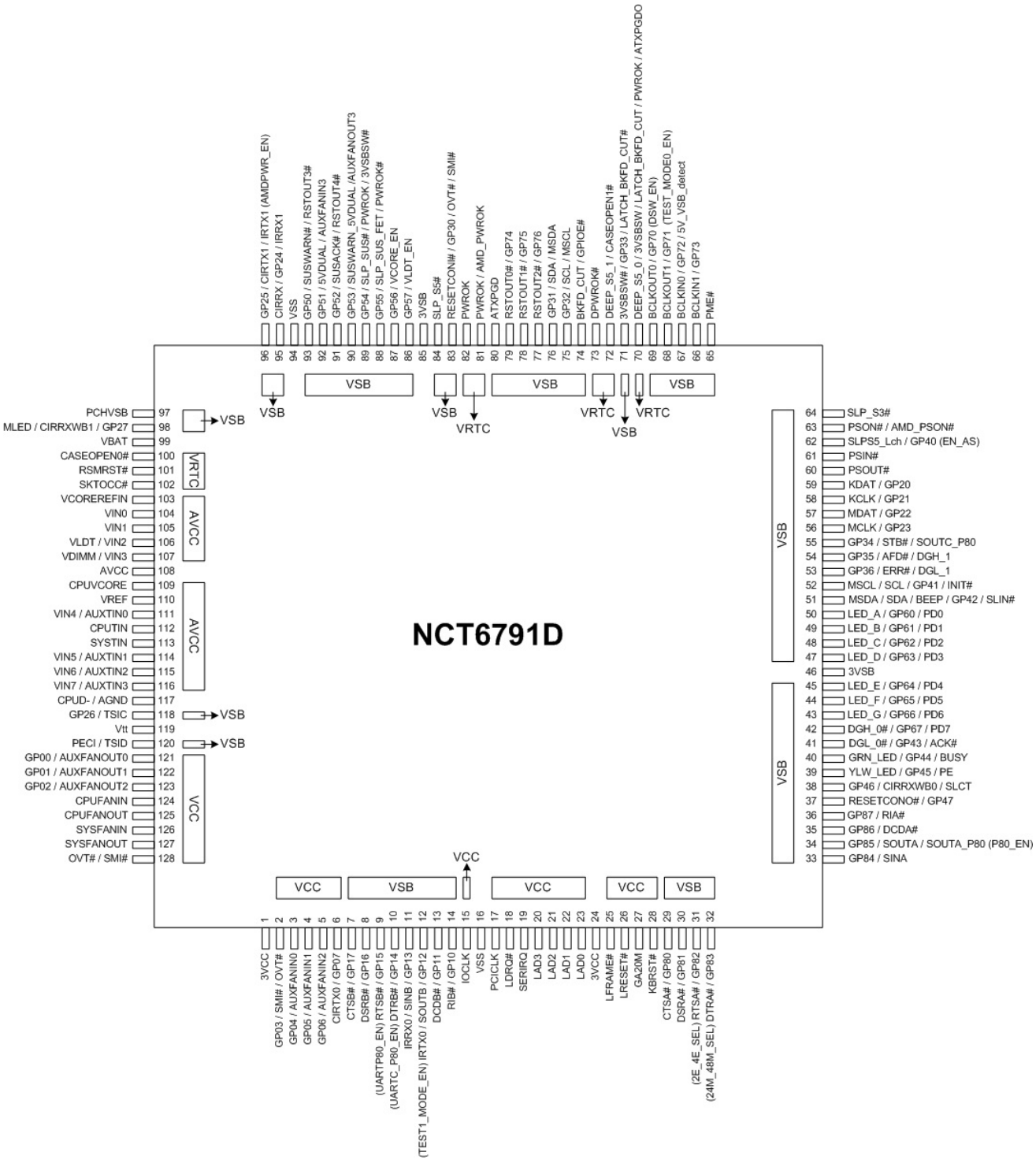

Figure 4-1 NCT6791D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to **Error! Reference source not found. Error! Reference source not found.** for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{tsp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5} - 5V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tcup5} - 5V TTL-level, input buffer with controllable pull-up
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
15	IOCLK	I	IN_{tp5}	VCC	System clock input, either 24MHz or 48MHz. The actual frequency must be specified by 24M_48M_SEL strapping.
65	PME#	O	OD_{12}	VSB	Generated PME event.
17	PCICLK	I	IN_{tp5}	VCC	PCI-clock 33-MHz input.
18	LDRQ#	O	O_{12}	VCC	Encoded DMA Request signal.
19	SERIRQ	I/O	IN_{tp3} O_{12} OD_{12}	VCC	Serialized IRQ input / output.
20-23	LAD[3:0]	I/O	IN_{tp3} OD_{12}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
25	LFRAME#	I	IN_{tp3}	VCC	Indicates the start of a new cycle or the termination of a broken cycle.
26	LRESET#	I	IN_{tsp3}	VCC	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 Multi-Mode Parallel Port

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
38	SLCT	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
39	PE	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
40	BUSY	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
41	ACK#	I	IN_{tsp5}	VSB	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
53	ERR#	I	IN_{tsp5}	VSB	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
51	SLIN#	O	O_{12}	VSB	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
52	INIT#	O	O_{12}	VSB	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
54	AFD#	O	O_{12}	VSB	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
55	STB#	O	O_{12}	VSB	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
50	PD0	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
49	PD1	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
48	PD2	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
47	PD3	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
45	PD4	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
44	PD5	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
43	PD6	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
42	PD7	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.3 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
35	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
34	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
33	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
32	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
31	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
30	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
29	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
14	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
13	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
12	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
11	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
10	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
9	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
8	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

5.4 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
27	GA20M	O	O_{12} OD_{12}	VCC	Gate A20 output. This pin is high after system reset. (KBC P21)
28	KBRST#	O	O_{12} OD_{12}	VCC	Keyboard reset. This pin is high after system reset. (KBC P20)
58	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock. Pull up is recommended if useless.
59	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data. Pull up is recommended if useless.
56	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock. Pull up is recommended if useless.
57	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data. Pull up is recommended if useless.

5.5 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
95	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length
6	CIRTX0	O	O_{12}	VCC	CIR transmission output
96	CIRTX1	O	O_{12}	VSB	CIR transmission output
38	CIRRXWB0	I	IN_{tsp5}	VSB	CIR input for wide band.
98	CIRRXWB1	I	IN_{tsp5}	VSB	CIR input for wide band.

5.6 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
102	SKTOCC#	I	IN_{tsp5}	VRTC	CPU socket occupied detection
100	CASEOPEN0#	I	IN_{tsp5}	VRTC	CASE OPEN 0 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
72	CASEOPEN1#	I	IN_{tsp5}	VRTC	CASE OPEN 1 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
103	VCOREREFIN	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
116	VIN7	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
115	VIN6	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
114	VIN5	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
111	VIN4	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
107	VIN3	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
106	VIN2	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
105	VIN1	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
104	VIN0	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
109	CPUVCORE	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
110	VREF	O	AOUT	AVCC	Reference Voltage (around 2.048 V).
116	AUXTIN3	I	AIN	AVCC	The input of temperature sensor 6.
115	AUXTIN2	I	AIN	AVCC	The input of temperature sensor 5. It is used for AUX2 temperature sensing.
114	AUXTIN1	I	AIN	AVCC	The input of temperature sensor 4. It is used for AUX1 temperature sensing.
111	AUXTIN0	I	AIN	AVCC	The input of temperature sensor 3. It is used for AUX0 temperature sensing.
112	CPUTIN	I	AIN	AVCC	The input of temperature sensor 2. It is used for CPU temperature sensing.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
113	SYSTIN	I	AIN	AVCC	The input of temperature sensor 1. It is used for system temperature sensing.
128	OVT#	O	OD_{12}	VCC	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#	O	OD_{12}	VCC	System Management Interrupt channel output.
83	OVT#	O	OD_{12}	VCC	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#	O	OD_{12}	VCC	System Management Interrupt channel output.
3	AUXFANIN0	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
4	AUXFANIN1	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
5	AUXFANIN2	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
5	AUXFANIN3	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
121	AUXFANOUT0	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
122	AUXFANOUT1	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
123	AUXFANOUT2	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
90	AUXFANOUT3	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
124	CPUFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
125	CPUFANOUT	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
126	SYSFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
127	SYSFANOUT	O	O_{12} OD_{12} AOUT	VCC	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.
51	BEEP	O	OD_{12}	VSB	Beep function for hardware monitor.

5.7 Intel® PECI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
120	PECI	I/O	I/O_{V3}	Vtt	INTEL® CPU PECI interface. Connect to CPU.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
119	Vtt	I	Power	Vtt	INTEL® CPU Vtt Power.

5.8 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
61	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
60	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
101	RSMRST#	O	OD_{8}	VRTC	Resume reset signal output.
73	DPWROK#	O	OD_{8}	VRTC	V3A signal output
64	SLP_S3#	I	IN_{tp5}	VSB	SLP_S3# input.
84	SLP_S5#	I	IN_{tp5}	VSB	SLP_S5# input.
80	ATXPGD	I	IN_{tcup5}	VSB	ATX power good signal.
63	PSON#	O	OD_{12}	VSB	Power supply on-off output.
82	PWROK	O	O_{8} OD_{8}	VRTC	3VCC PWROK signal.
81	PWROK	O	O_{8} OD_{8}	VRTC	3VCC PWROK signal.
70	PWROK	O	OD_{8}	VRTC	3VCC PWROK signal.
89	PWROK	O	OD_{12}	VSB	3VCC PWROK signal.
88	PWROK#	O	OD_{12}	VSB	3VCC PWROK# signal.
81	AMD_PWROK	O	OD_{8}	VRTC	3VCC AMD PWROK signal.
83	RESETCONI#	I	IN_{tp5}	VSB	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
37	RESETCONO#	O	OD_{12}	VSB	RESETCONO# output.
70	3VSBSW	O	OD_{12}	VRTC	Switch 3VSB power to memory when in S3 state.
71	3VSBSW#	O	OD_{24}	VSB	Switch 3VSB power to memory when in S3 state.
89	3VSBSW#	O	OD_{12}	VSB	Switch 3VSB power to memory when in S3 state.
79	RSTOUT0#	O	OD_{24}	VSB	PCI Reset Buffer 0. (from pin26)
78	RSTOUT1#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 1. (from pin26) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit6.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
77	RSTOUT2#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 2. (from pin26) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit7.
91	RSTOUT4#	O	O_{12}	VSB	PCI Reset Buffer 4. (from pin26) This pin is push-pull output.
93	RSTOUT3#	O	O_{12}	VSB	PCI Reset Buffer 3. (from pin26) This pin is push-pull output.

5.9 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	SLPS5_Lch	O	O_{12}	VSB	This pin has the same signal output as SLP_S5#, but keeps the output signal high while in deep S3.
70	DEEP_S5_0	O	OD_{12}	VRTC	This pin is to control system power for entering “more power saving mode”.
72	DEEP_S5_1	O	OD_{8}	VRTC	This pin is to control system power for entering “more power saving mode”.

5.10 Port 80 Message Display & LED Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
42	DGH_0#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
41	DGL_0#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
54	DGH_1#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
53	DGL_1#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
50 49 48 47 45 44 43	LED_A LED_B LED_C LED_D LED_E LED_F LED_G	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
39	YLW_LED	O	OD_{12}	VSB	Yellow LED output control. This pin could indicate the power status.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
40	GRN_LED	O	OD_{12}	VSB	Green LED output control. This pin could indicate the power status.

5.11 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
75	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
76	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
52	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
51	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
75	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
76	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
52	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
51	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.

5.12 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46, 85	3VSB	I			+3.3 V stand-by power supply for the digital circuits.
99	VBAT	I			+3 V on-board battery for the digital circuits.
1,24	VCC	I			+3.3 V power supply for driving 3 V on host interface.
108	AVCC	I			Analog +3.3 V power input. Internally supply power to all analog circuits.
117	CPUD- / AGND	I			Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
16, 94	VSS	I			Ground.
119	VTT	I			INTEL® CPU Vtt power.

5.13 AMD Power-On Sequence

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
109	CPUVCORE	I	AIN	AVCC	Power sequence group B signal
106	VLDT	I	AIN	AVCC	Power sequence group C signal
107	VDIMM	I	AIN	AVCC	Memory power enable
87	VCORE_EN	O	OD_{12}	VSB	CPU Vcore power enable
86	VLDT_EN	O	OD_{12}	VSB	Hyper transport I/O power enable
81	AMD_PWROK	O	OD_{12}	VSB	AMD power on sequence ok signal
63	AMD_PSON#	O	OD_{12}	VSB	Power supply on/off output to enable ATX

5.14 AMD SB-TSI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
118	TSIC	O	OD_{12}	VCC	AMD SB-TSI clock output.
120	TSID	I/O	IN_{tsp3} OD_{12}	VCC	AMD SB-TSI data input / output.

5.15 Dual Voltage Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
74	BKFD_CUT	O	OD_{12}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S3 sleep state.
71	LATCH_BKFD_CUT#	O	O_{24}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.
70	LATCH_BKFD_CUT	O	O_{12}	VRTC	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

5.16 DSW

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
89	SLP_SUS#	I	IN_{tp5}	VSB	This pin connects to SLP_SUS# in CPT PCH
90	SUS_WARN_5VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits
91	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
92	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
93	SUSWARN#	I	IN_{tp5}	VSB	This pin connects to SUSWARN# in CPT PCH

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
88	SLP_SUS_FET	O	OD_{12}	VSB	This pin connects to VSB power switch
97	PCHVSB	I	AIN	VSB	PCHVSB function

5.17 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
11	IRRX0	I	IN_{tp5}	VSB	IR Receiver input.
12	IRTX0	O	O_{12}	VSB	IR Transmitter output.
95	IRRX1	I	IN_{tsp5}	VSB	IR Receiver input.
96	IRTX1	O	O_{12}	VSB	IR Transmitter output.

5.18 General Purpose I/O Port

5.18.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
121	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 0.
122	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 1.
123	GP02	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 2.
2	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 3.
3	GP04	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 4.
4	GP05	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 5.
5	GP06	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 6.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
6	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 7.

5.18.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
13	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
12	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.
11	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
10	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
9	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.
8	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
7	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.18.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
59	GP20	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 0.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
58	GP21	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 1.
57	GP22	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 2.
56	GP23	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 3.
95	GP24	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 4.
96	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 5.
118	GP26	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 6.
98	GP27	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 7.

5.18.4 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
83	GP30	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 0.
76	GP31	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 1.
75	GP32	I/O	IN_{tsp5} O_{12} OD_{12}	VRTC	General-purpose I/O port 3 bit 2.
71	GP33	I/O	IN_{tp5} O_{24} OD_{24}	VRTC	General-purpose I/O port 3 bit 3.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
55	GP34	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 4.
54	GP35	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 5.
53	GP36	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 6.

5.18.5 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	GP40	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 0.
52	GP41	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 1.
51	GP42	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 2.
41	GP43	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 4 bit 3.
40	GP44	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 4.
39	GP45	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 5.
38	GP46	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 6.
37	GP47	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 7.

5.18.6 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
93	GP50	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 0.
92	GP51	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 1.
91	GP52	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 2.
90	GP53	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 3.
89	GP54	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 4.
88	GP55	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 5.
87	GP56	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 6.
86	GP57	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 7.

5.18.7 GPIO-6 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
50	GP60	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 0.
49	GP61	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 1.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
48	GP62	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 2.
47	GP63	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 3.
45	GP64	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 4.
44	GP65	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 5.
43	GP66	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 6.
42	GP67	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 6 bit 7.

5.18.8 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
69	GP70	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 0.
68	GP71	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 1.
67	GP72	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 2.
66	GP73	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 3.
79	GP74	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 7 bit 4.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
78	GP75	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 7 bit 5.
77	GP76	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 7 bit 6.

5.18.9 GPIO-8 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
29	GP80	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 0.
30	GP81	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 1.
31	GP82	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 2.
32	GP83	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 3.
33	GP84	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 4.
34	GP85	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 5.
35	GP86	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 6.
36	GP87	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 7.

5.19 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	2E_4E_SEL	I	IN_{tdp5}	VSB	SIO I/O address selection. (Strapped by LRESET#) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
32	24M_48M_SEL	I	IN_{tdp5}	VSB	Input clock rate selection (Strapped by **VCC**: internal Power OK signal without any delay.) Strapped to high: The clock input on pin 15 is 48MHz. Strapped to low: The clock input on pin 15 is 24MHz.
34	PO80_EN	I	IN_{tdp5}	VSB	Port80 / GPIO function selection. (Strapped by LRESET#) Strapped to high: Port80 function. Strapped to low: non-PRT function
9	UARTP80_EN	I	IN_{tdp5}	VSB	Pin34 function selection. (Strapped by LRESET#) See configuration register
10	UARTCP80_EN	I	IN_{tdp5}	VSB	Pin55 function selection. (Strapped by LRESET#) See configuration register
62	EN_AS	I	IN_{tdp5}	VSB	Enable ASUS specific function. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high: Enable ASUS function Strapped to low: Disable ASUS function
68	TEST_MODE0_EN	I	IN_{tp5}	VSB	PSIN# function selection. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high:LNV PSIN# function Strapped to low: Normal PSIN# function
69	DSW_EN	I	IN_{tp5}	VSB	DSW position selection. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high: DSW function Strapped to low: GPIO function

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
96	AMDPWR_EN	I	IN_{tdp5}	VSB	Enable AMD power sequence function. (Strapped by **VSB** power: internal RSMRST# signal.) Strapped to high: Enable AMD power sequence Strapped to low: Disable AMD power sequence

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.20 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	31	3VSB	Pull-down	47.4K	1
24M_48M_SEL	32	3VSB	Pull-down	47.4K	1
PO80_EN	34	3VSB	Pull-down	47.4K	1
UARTP80_EN	9	3VSB	Pull-down	47.4K	1
UARTCP80_EN	10	3VSB	Pull-down	47.4K	1
TEST1_MODE_EN	12	3VSB	Pull-down	47.4K	1
TEST_MODE0_EN	68	3VSB	Pull-down	47.4K	1
EN_AS	62	3VSB	Pull-down	47.4K	2
AMDPWR_EN	96	3VSB	Pull-down	47.4K	2
Advanced Configuration & Power Interface					
PSIN#	61	3VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

5.21 Strapping multi function pin control

PO80_EN	**Pin38** function selection (See CR27) **Pin39 ~ 40** function selection (See CR1B) **Pin41 ~ 50** function selection (See CR27)

<table>
<tr><td></td><td>
Pin51 function selection (See CR1B)
Pin52 function selection (See CR1A)
Pin53 function selection
<table>
<tr><td>PO80_EN</td><td>Pin53</td></tr>
<tr><td>0</td><td>GP36</td></tr>
<tr><td>1</td><td>DGL_1#</td></tr>
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Pin54 function selection
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<tr><td>PO80_EN</td><td>Pin54</td></tr>
<tr><td>0</td><td>GP35</td></tr>
<tr><td>1</td><td>DGH_1#</td></tr>
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</td></tr>
<tr><td>UARTP80_EN</td><td>Pin34 function selection (See CR2A)</td></tr>
<tr><td>UARTCP80_EN</td><td>
Pin55 function selection
<table>
<tr><td>UARTCP80_EN</td><td>Pin55</td></tr>
<tr><td>0</td><td>GP34</td></tr>
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<tr><td>EN_AS</td><td>
Pin66 function selection
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<tr><td>EN_AS</td><td>Pin66</td></tr>
<tr><td>0</td><td>GP73</td></tr>
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Pin67 function selection
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Pin68 function selection
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Pin69 function selection
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<tr><td>DSW_EN</td><td>
Pin90 function selection
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Pin92 function selection
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<table>
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<td>AMDPWR_EN</td>
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Pin63 function Selection
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<tr><td>AMDPWR_EN</td><td>Pin63</td></tr>
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<tr><td>1</td><td>AMD_PSON#</td></tr>
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Pin81 function Selection
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<tr><td>0</td><td>PWROK</td></tr>
<tr><td>1</td><td>AMD_PWROK</td></tr>
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Pin86 function Selection
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<tr><td>AMDPWR_EN</td><td>Pin86</td></tr>
<tr><td>0</td><td>GP57</td></tr>
<tr><td>1</td><td>VLDT_EN</td></tr>
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Pin87 function Selection
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<tr><td>AMDPWR_EN</td><td>Pin87</td></tr>
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<tr><td>1</td><td>VCORE_EN</td></tr>
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6. TOP MARKING SPECIFICATIONS

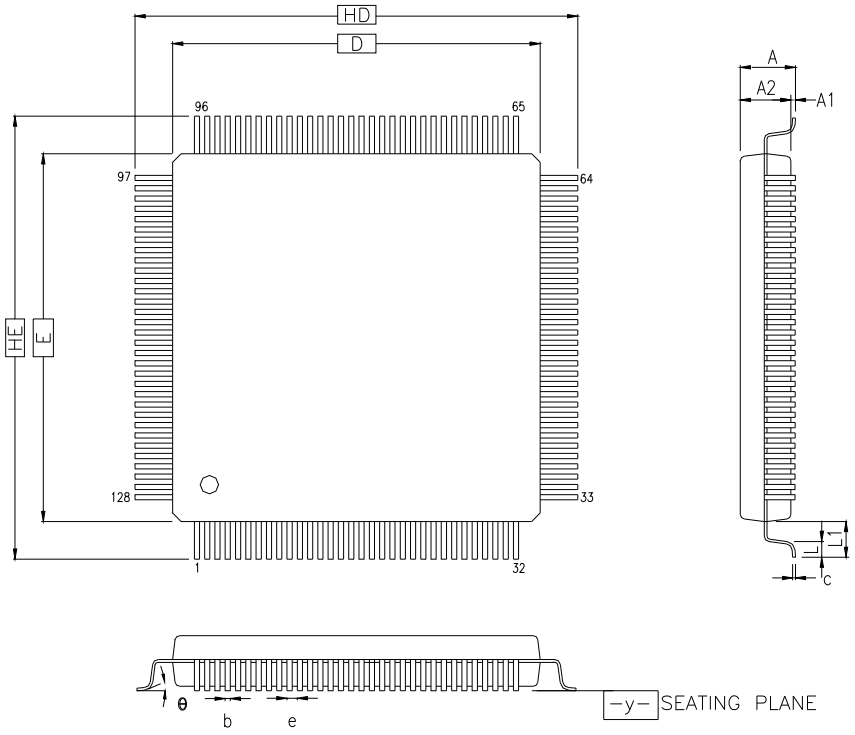
1st line: Nuvoton logo
2nd line: part number NCT6791D
3rd line: wafer production series lot number 28201234
4th line: tracking code 123G9AFA

123: packages made in 2011, week 23
G: assembly house ID; G means GR, A means ASE, etc.
9: code version; 9 means code 009
A: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use.

7. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6791D	128Pin LQFP (Green package)	Commercial, 0°C to +70°C

8. PACKAGE SPECIFICATION



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-pin LQFP (14mm x 14mm x 1.4mm)

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	06/05/2012	N.A.	Draft datasheet

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

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