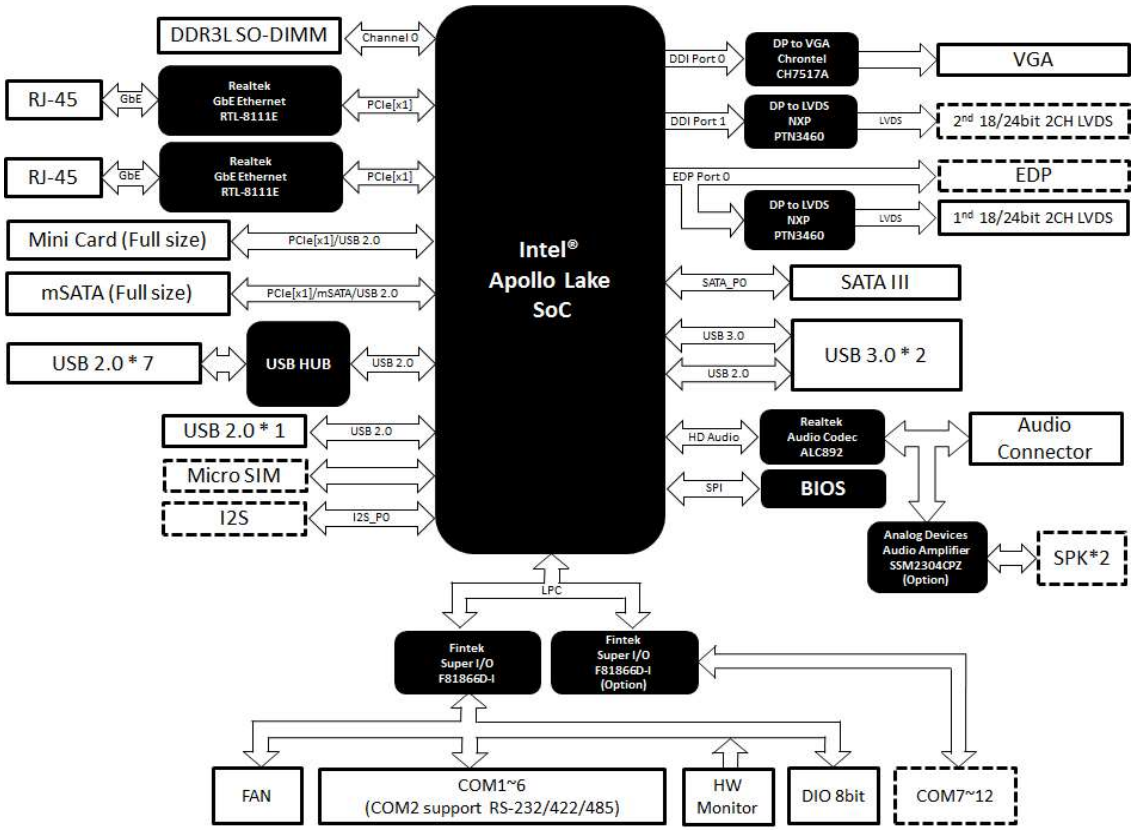
GENE-APL7 A1.0_0_2

Sub Compact Board



Project Number :
Production Line : Sub.ESB.AASM

<Core Design>

Title: Cover Sheet
Size: Custom | Document Number: GENE-APL7 | Rev: A1.0_0_2
Date: Friday, December 08, 2017 | Sheet: 1 of 40

SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	BOARDID_BIT0
GPIO_1	1.8V	20K PD/I	BOARDID_BIT1
GPIO_2	1.8V	20K PD/I	BOARDID_BIT2
GPIO_3	1.8V	20K PD/I	BOARDID_BIT3
GPIO_4	1.8V	20K PD/I	LVDS_RBIT0
GPIO_5	1.8V	20K PD/I	LVDS_RBIT1
GPIO_6	1.8V	20K PD/I	LVDS_RBIT2
GPIO_7	1.8V	20K PD/I	LVDS_RBIT3
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	WAKE_RI#
GPIO_15	1.8V	20K PD/I	
GPIO_16	1.8V	20K PD/I	
GPIO_17	1.8V	20K PD/I	
GPIO_18	1.8V	20K PD/I	
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GPI[0]
GPIO_23	1.8V	20K PD/I	SATA_GPI[1]
GPIO_24	1.8V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	1.8V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/I/O	
GPIO_217	1.8V	20K PD/I/O	
GPIO_218	1.8V	20K PD/I/O	
GPIO_219	1.8V	20K PD/I/O/OP	

SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
LCD Backlight Contoller	2Eh
CMOS Backup EEPROM	AEh
GPIO IC	6Eh
PTN3460 Slave	C0h
PTN3460 Slave	40h

PCB Footprints

PCB STACK :

Impedence 55ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : Signal
- Layer 5 : POWER
- Layer 6 : Signal
- Layer 7 : GND
- Layer 8 : Solder

F81866D GPIO Pins :

Name	Tolerance	Power Well	Default	Function	
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#	
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#	
GPIO02	5V	I_VSB3V	Native	PM_SUS_WARN#	
GPIO03	5V	I_VSB3V	Native	PM_SUS_ACK#	
GPIO04	5V	I_VSB3V	Native	PM_SLP_SUS#	
GPIO05	5V	I_VSB3V	Native	LAN1_DISABLE#	
GPIO06	5V	I_VSB3V	Native	LAN2_DISABLE#	
GPIO07	5V	I_VSB3V	Native	W_DISABLE0#	
GPIO10	5V	I_VSB3V	Native	W_DISABLE1#	
GPIO11	5V	I_VSB3V	Native	EN_USB	
GPIO12	5V	I_VSB3V	Native	8WIRE_EN#	
GPIO13	5V	I_VSB3V	Native		-
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP	
GPIO15	5V	I_VSB3V	Native	WDT_RST#	
GPIO16	5V	I_VSB3V	Native		-
GPIO17	5V	I_VSB3V	Native	SIO_PECI	
GPIO20	5V	I_VSB3V	Native	mSATA_PCIE_SEL	
GPIO21	5V	I_VSB3V	Native	ATX_PG	
GPIO22	5V	I_VSB3V	Native	EXT_PWRBTN#	
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#	
GPIO24	5V	I_VSB3V	Native	PM_SLP_S3#	
GPIO25	5V	I_VSB3V	Native	PSON#	
GPIO26	5V	VBAT	Native	PWOK	
GPIO27	5V	VBAT	Native	SIO_RSMRST#	
GPIO30	5V	3VCC	Native	DCD3#	
GPIO31	5V	3VCC	Native	RI3#	
GPIO32	5V	3VCC	Native	CTS3#	
GPIO33	5V	3VCC	Native	DTR3#	
GPIO34	5V	3VCC	Native	RTS3#	
GPIO35	5V	3VCC	Native	DSR3#	
GPIO36	5V	3VCC	Native	TX3#	
GPIO37	5V	3VCC	Native	RX3#	
GPIO40	5V	3VCC	Native	DCD4#	
GPIO41	5V	3VCC	Native	RI4#	
GPIO42	5V	3VCC	Native	CTS4#	
GPIO43	5V	3VCC	Native	DTR4#	
GPIO44	5V	3VCC	Native	RTS4#	
GPIO45	5V	3VCC	Native	DSR4#	
GPIO46	5V	3VCC	Native	TX4#	
GPIO47	5V	3VCC	Native	RX4#	
GPIO50	5V	3VCC	Native	ADM213_EN	1, diver mode 0
GPIO51	5V	3VCC	Native	81438_SD	
GPIO52	5V	3VCC	Native	SEL_COM2_MD0	
GPIO53	5V	3VCC	Native	SEL_COM2_MD1	
GPIO54	5V	3VCC	Native	COM2_SLEW	
GPIO55	5V	3VCC	Native	SEL_COM3_MD0	
GPIO56	5V	3VCC	Native	SEL_COM3_MD1	
GPIO57	5V	3VCC	Native	COM3_SLEW	
GPIO60	5V	3VCC	Native	LVDS1_EN	
GPIO61	5V	3VCC	Native	LVDS1_PD#	
GPIO62	5V	3VCC	Native	LVDS2_EN	
GPIO63	5V	3VCC	Native	LVDS2_PD#	
GPIO64	5V	3VCC	Native	CH7517_RST#	
GPIO65	5V	I_VSB3V	Native	LPC_PME#	
GPIO66	5V	VBAT	Native	DPWROK	
GPIO67	5V	I_VSB3V	Native	PM_SLP_S5#	
GPIO70	5V	3VCC	Native	PE	
GPIO71	5V	3VCC	Native	BUSY	
GPIO72	5V	3VCC	Native	ACK#	
GPIO73	5V	3VCC	Native	SLIN#	
GPIO74	5V	3VCC	Native	PINIT#	
GPIO75	5V	3VCC	Native	ERR#	
GPIO76	5V	3VCC	Native	AFD#	
GPIO77	5V	3VCC	Native	STB#	
GPIO80	5V	3VCC	Native	PD0	DIO_0
GPIO81	5V	3VCC	Native	PD1	DIO_1
GPIO82	5V	3VCC	Native	PD2	DIO_2
GPIO83	5V	3VCC	Native	PD3	DIO_3
GPIO84	5V	3VCC	Native	PD4	DIO_4
GPIO85	5V	3VCC	Native	PD5	DIO_5
GPIO86	5V	3VCC	Native	PD6	DIO_6
GPIO87	5V	3VCC	Native	PD7	DIO_7

F81866D GPIO Pins :

Name	Tolerance	Power Well	Default	Function	
GPIO01	5V	I_VSB3V	Native	ERP_CTRL0#	
GPIO02	5V	I_VSB3V	Native	ERP_CTRL1#	
GPIO03	5V	I_VSB3V	Native	PM_SUS_WARN#	
GPIO04	5V	I_VSB3V	Native	PM_SUS_ACK#	
GPIO05	5V	I_VSB3V	Native	PM_SLP_SUS#	
GPIO06	5V	I_VSB3V	Native	LAN1_DISABLE#	
GPIO07	5V	I_VSB3V	Native	LAN2_DISABLE#	
GPIO08	5V	I_VSB3V	Native	W_DISABLE0#	
GPIO11	5V	I_VSB3V	Native	W_DISABLE1#	
GPIO12	5V	I_VSB3V	Native	EN_USB	
GPIO13	5V	I_VSB3V	Native	8WIRE_EN#	
GPIO14	5V	I_VSB3V	Native		-
GPIO15	5V	I_VSB3V	Native	ATX_AT_TRAP	
GPIO16	5V	I_VSB3V	Native	WDT_RST#	
GPIO17	5V	I_VSB3V	Native		-
GPIO18	5V	I_VSB3V	Native	SIO_PECI	
GPIO21	5V	I_VSB3V	Native	mSATA_PCIE_SEL	
GPIO22	5V	I_VSB3V	Native	ATX_PG	
GPIO23	5V	I_VSB3V	Native	EXT_PWRBTN#	
GPIO24	5V	I_VSB3V	Native	PM_PWRBTN#	
GPIO25	5V	I_VSB3V	Native	PM_SLP_S3#	
GPIO26	5V	I_VSB3V	Native	PSON#	
GPIO27	5V	VBAT	Native	PWOK	
GPIO28	5V	VBAT	Native	SIO_RSMRST#	
GPIO31	5V	3VCC	Native	DCD3#	
GPIO32	5V	3VCC	Native	RI3#	
GPIO33	5V	3VCC	Native	CTS3#	
GPIO34	5V	3VCC	Native	DTR3#	
GPIO35	5V	3VCC	Native	RTS3#	
GPIO36	5V	3VCC	Native	DSR3#	
GPIO37	5V	3VCC	Native	TX3#	
GPIO38	5V	3VCC	Native	RX3#	
GPIO41	5V	3VCC	Native	DCD4#	
GPIO42	5V	3VCC	Native	RI4#	
GPIO43	5V	3VCC	Native	CTS4#	
GPIO44	5V	3VCC	Native	DTR4#	
GPIO45	5V	3VCC	Native	RTS4#	
GPIO46	5V	3VCC	Native	DSR4#	
GPIO47	5V	3VCC	Native	TX4#	
GPIO48	5V	3VCC	Native	RX4#	
GPIO51	5V	3VCC	Native	ADM213_EN	1, diver mode 0
GPIO52	5V	3VCC	Native	81438_SD	
GPIO53	5V	3VCC	Native	SEL_COM2_MD1	
GPIO54	5V	3VCC	Native	SEL_COM2_MD2	
GPIO55	5V	3VCC	Native	COM2_SLEW	
GPIO56	5V	3VCC	Native	SEL_COM3_MD1	
GPIO57	5V	3VCC	Native	SEL_COM3_MD2	
GPIO58	5V	3VCC	Native	COM3_SLEW	
GPIO61	5V	3VCC	Native	LVDS1_EN	
GPIO62	5V	3VCC	Native	LVDS1_PD#	
GPIO63	5V	3VCC	Native	LVDS2_EN	
GPIO64	5V	3VCC	Native	LVDS2_PD#	
GPIO65	5V	3VCC	Native	CH7517_RST#	
GPIO66	5V	I_VSB3V	Native	LPC_PME#	
GPIO67	5V	VBAT	Native	DPWROK	
GPIO68	5V	I_VSB3V	Native	PM_SLP_S5#	
GPIO71	5V	3VCC	Native	PE	
GPIO72	5V	3VCC	Native	BUSY	
GPIO73	5V	3VCC	Native	ACK#	
GPIO74	5V	3VCC	Native	SLIN#	
GPIO75	5V	3VCC	Native	PINIT#	
GPIO76	5V	3VCC	Native	ERR#	
GPIO77	5V	3VCC	Native	AFD#	
GPIO78	5V	3VCC	Native	STB#	
GPIO81	5V	3VCC	Native	PD1	DIO_1
GPIO82	5V	3VCC	Native	PD2	DIO_2
GPIO83	5V	3VCC	Native	PD3	DIO_3
GPIO84	5V	3VCC	Native	PD4	DIO_4
GPIO85	5V	3VCC	Native	PD5	DIO_5
GPIO86	5V	3VCC	Native	PD6	DIO_6
GPIO87	5V	3VCC	Native	PD7	DIO_7
GPIO88	5V	3VCC	Native	PD8	DIO_8

<Core Design>

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Title: **System Settings**

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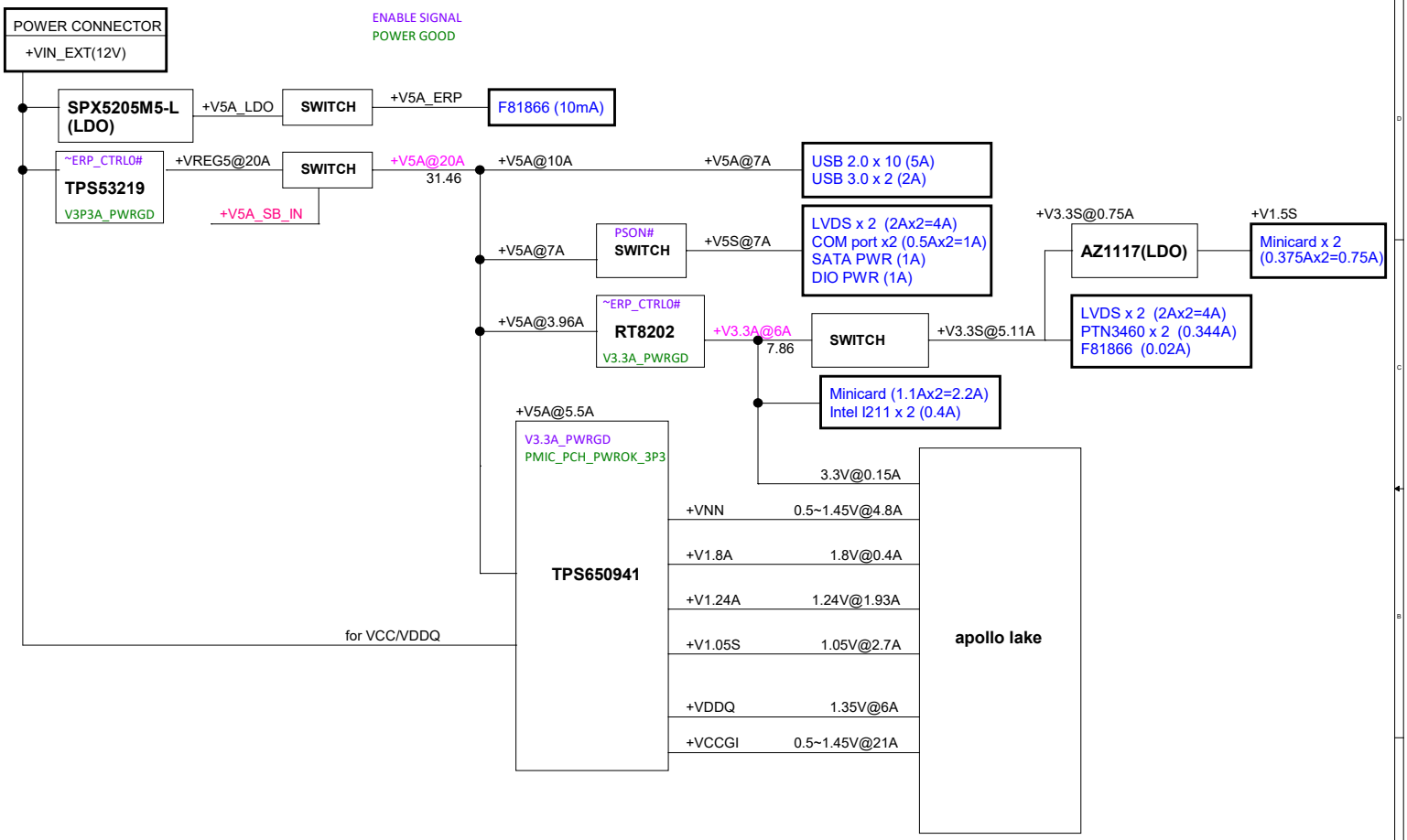

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AAEON an ASUS assoc. co.

Title: Power Delivery

Size	Document Number	Rev:
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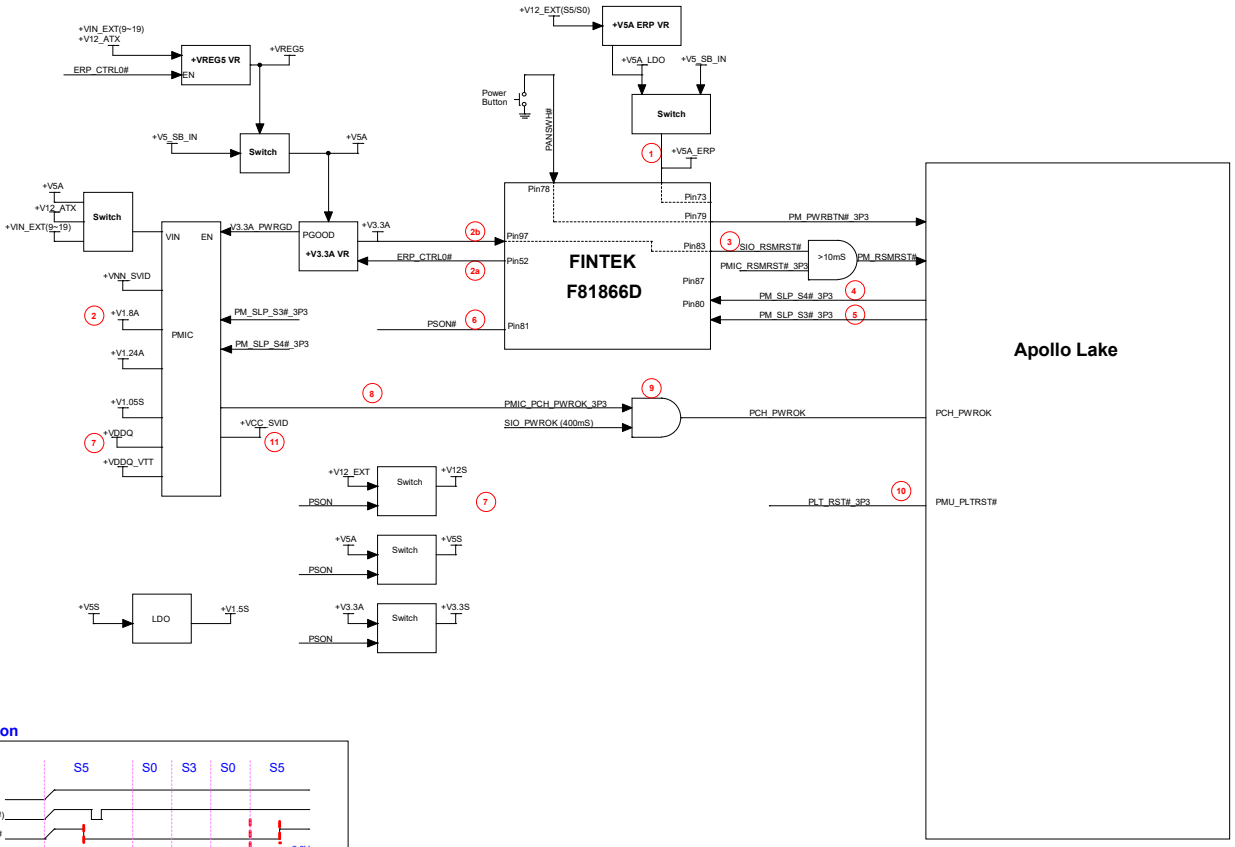
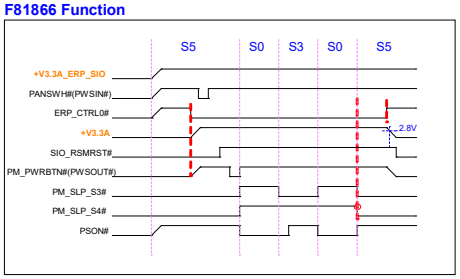
ERP Mode



F81866 Function



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AAEON an ASUS assoc. co.	Title: Power Sequence	
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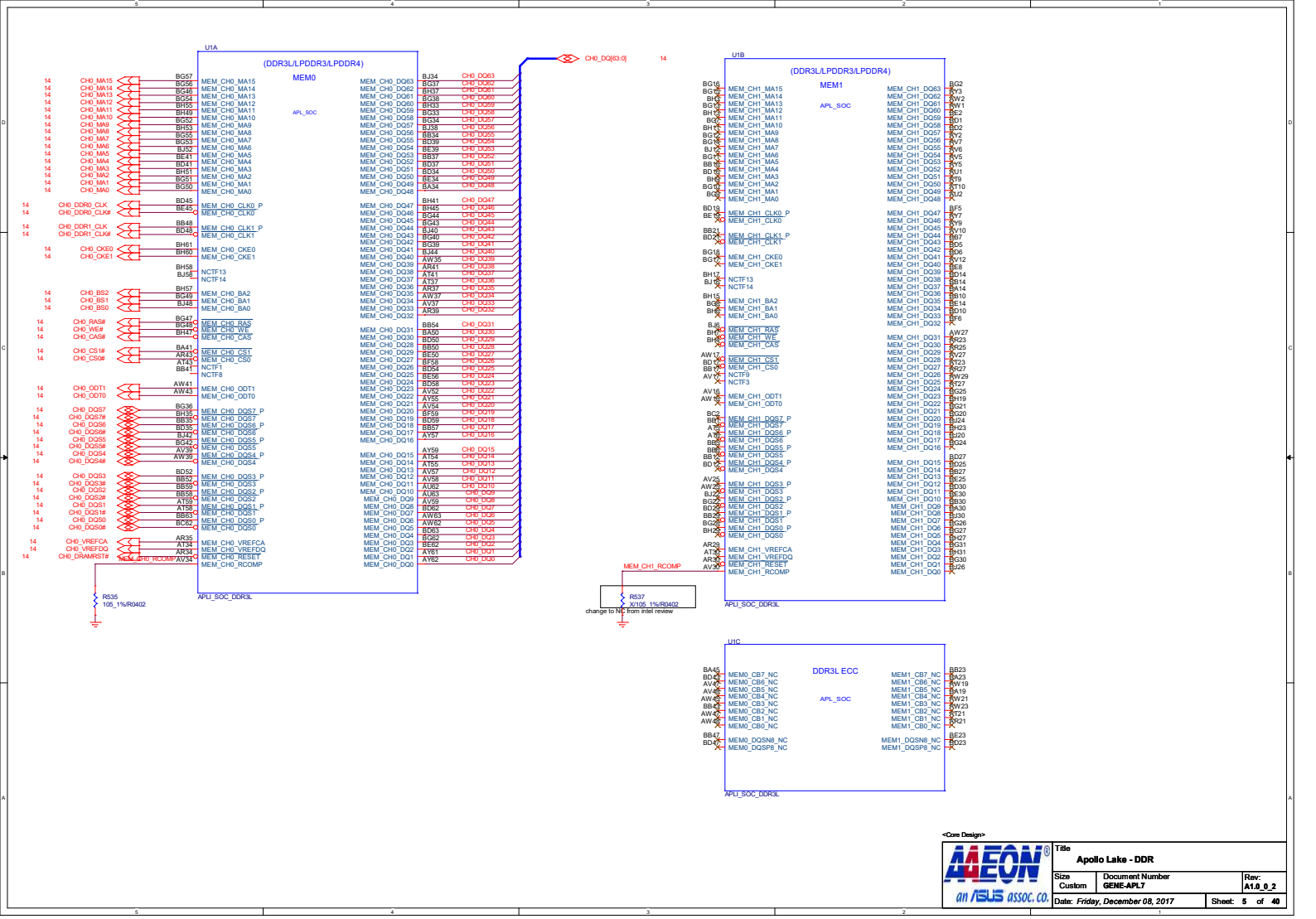

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Title: Apollo Lake - DDR		
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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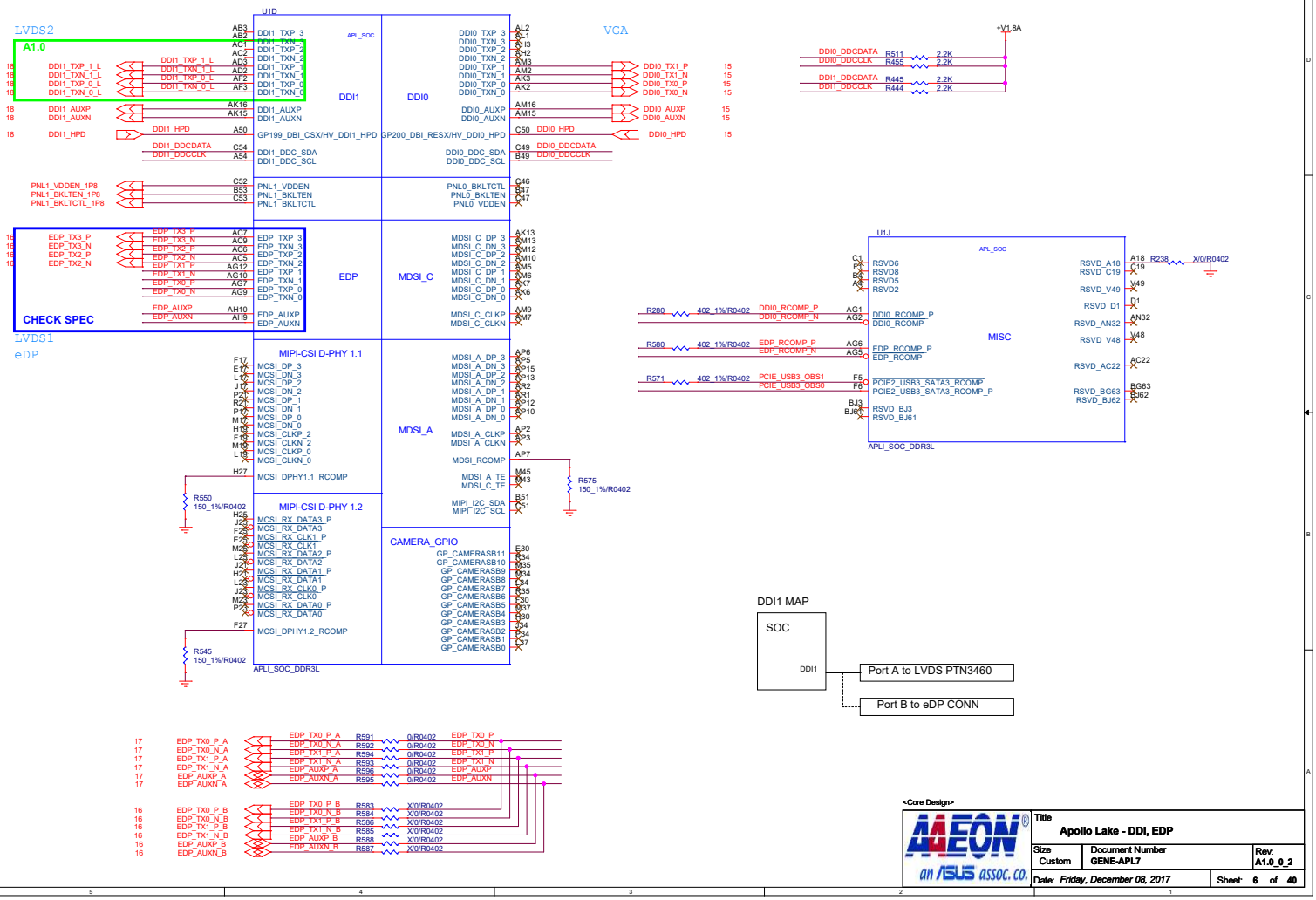

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Title	Apollo Lake - DDI, EDP
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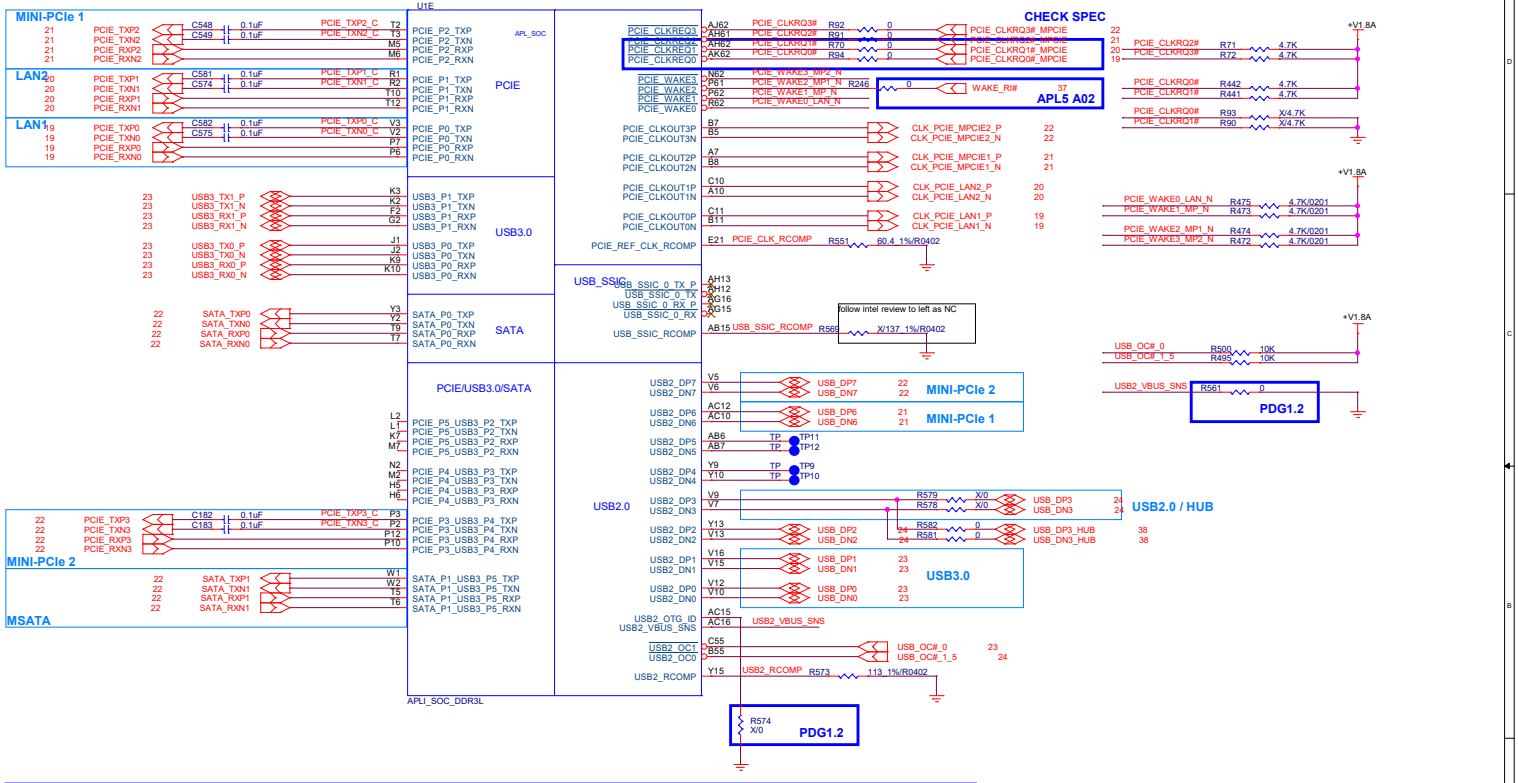

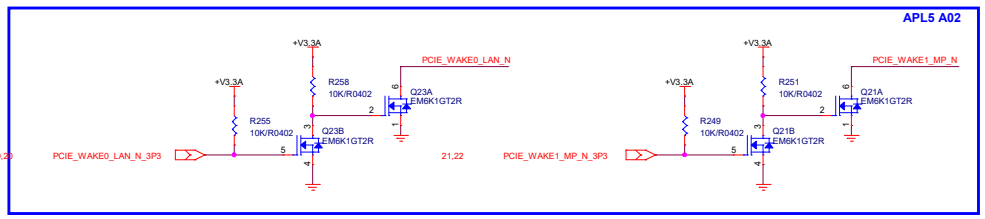

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AAEON an ASUS assoc. co.	Title: Apollo Lake - SATA_PCIE_USB	
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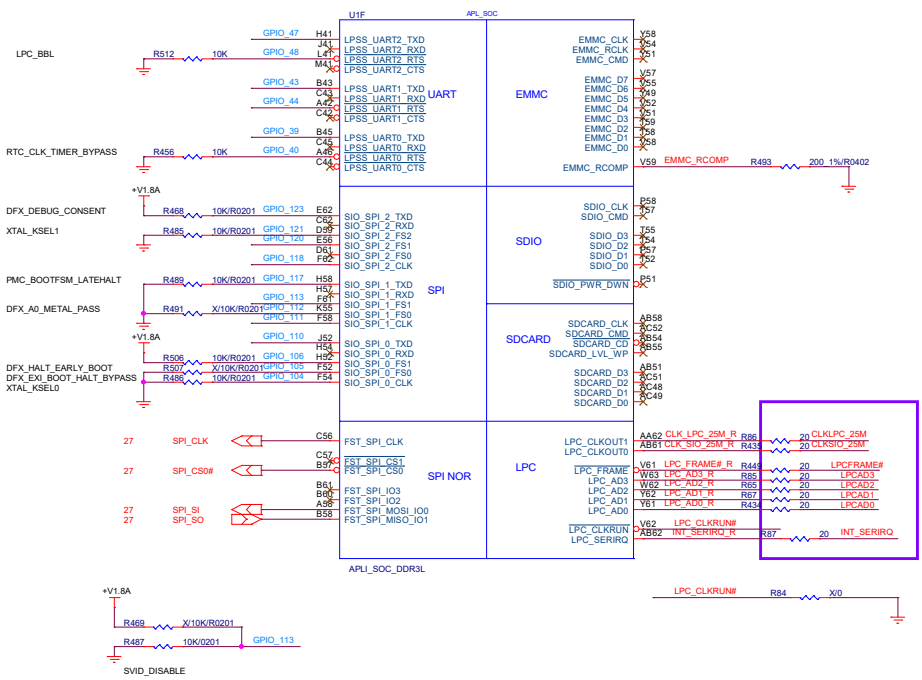
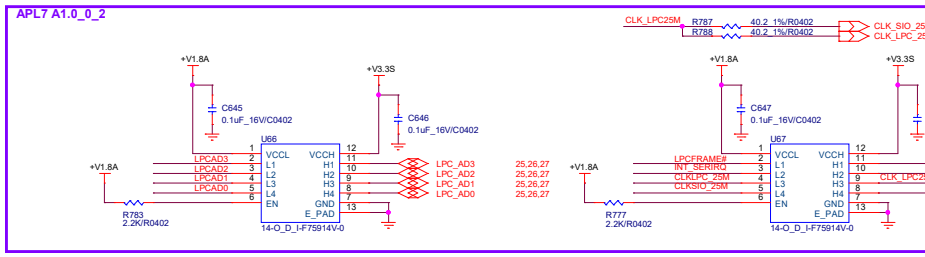
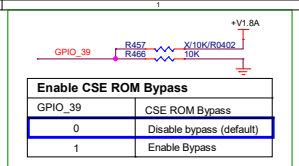
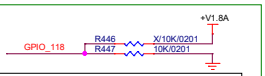


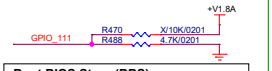




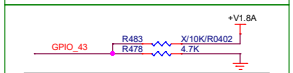
Enable CSE ROM Bypass	
GPIO_39	CSE ROM Bypass
0	Disable bypass (default)
1	Enable Bypass



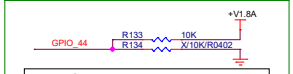
Flash Descriptor Override	
GPIO_118	
0	No Override (Normal Operation)
1	Override



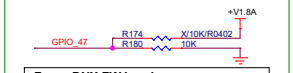
Boot BIOS Strap (BBS)	
GPIO_111	
0	Boot from SPI
1	Do not boot from SPI (default)



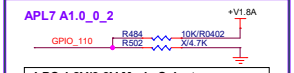
Allow eMMC as a boot source	
GPIO_43	eMMC as a boot
0	Disable
1	Enable (default)



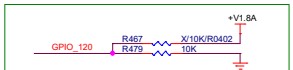
Allow SPI as a boot source	
GPIO_44	SPI as a boot
0	Disable
1	Enable (default)



Force DNX FW Load	
GPIO_47	DNX FW Load
0	Do not force (default)
1	Enable



LPC 1.8V/3.3V Mode Select	
GPIO_110	LPC Voltage
0	3.3V mode
1	1.8V mode (default)



Top swap override	
GPIO_120	
0	Disable (default)
1	Override

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Title		
Apollo Lake - LPC,SPI,EMMC,SD,UART		
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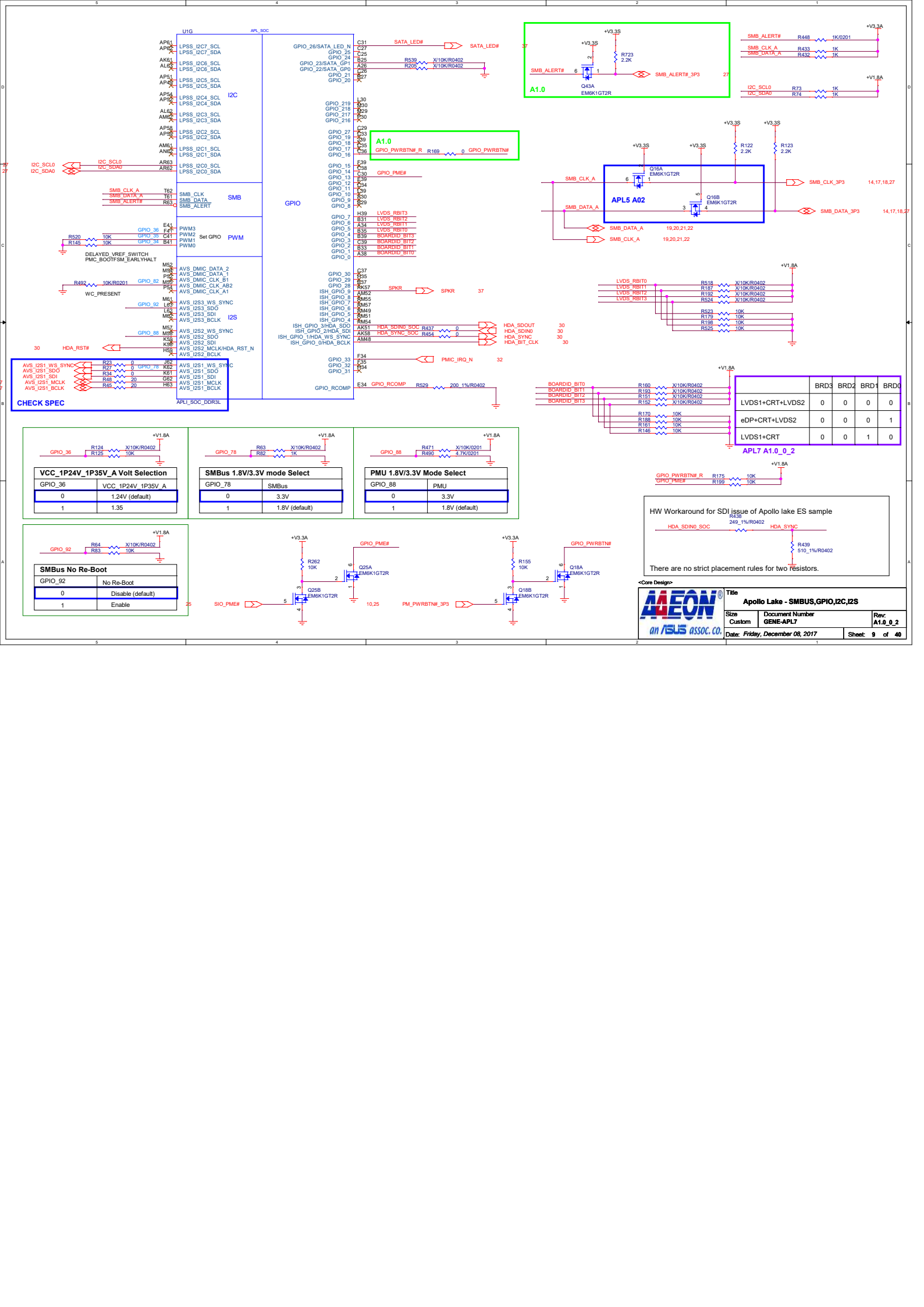


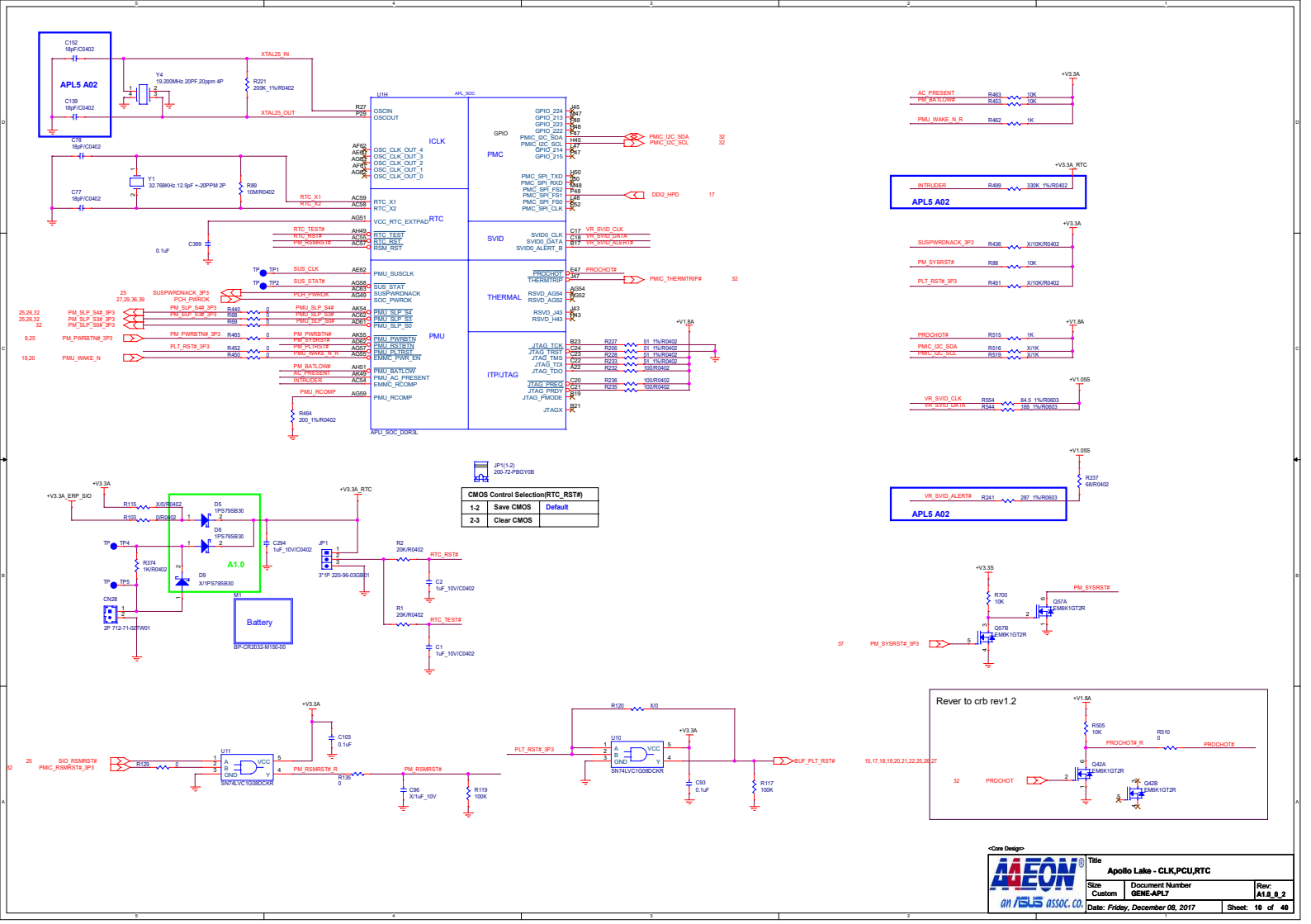
	BRD3	BRD2	BRD1	BRD0
LVDS1+CRT+LVDS2	0	0	0	0
eDP+CRT+LVDS2	0	0	0	1
LVDS1+CRT	0	0	1	0

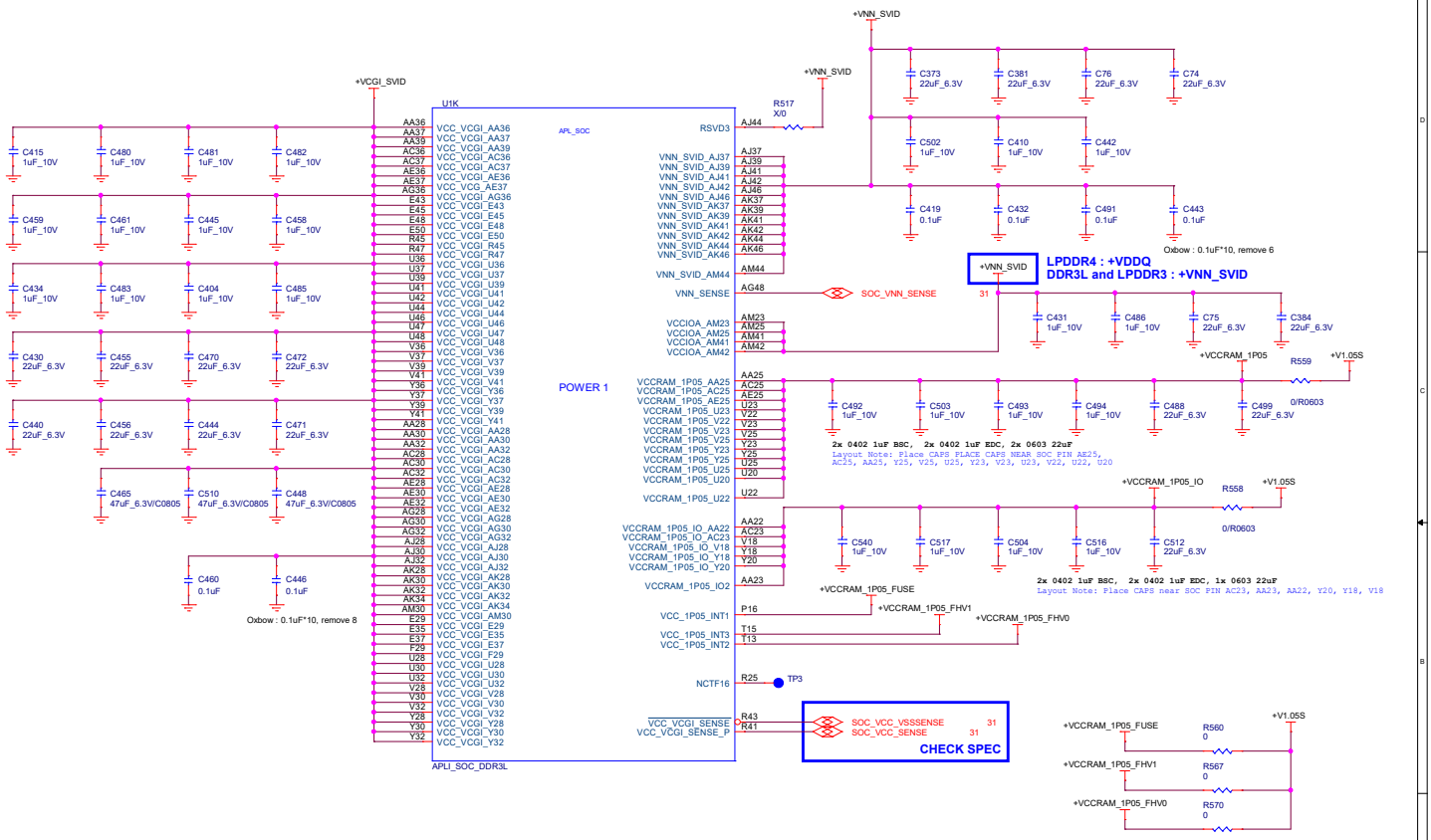
VCC_1P24V_1P35V_A Volt Selection	
GPIO_36	VCC_1P24V_1P35V_A
0	1.24V (default)
1	1.35

SMBus 1.8V/3.3V mode Select	
GPIO_78	SMBus
0	3.3V
1	1.8V (default)

PMU 1.8V/3.3V Mode Select	
GPIO_88	PMU
0	3.3V
1	1.8V (default)

SMBus No Re-Boot	
GPIO_92	No Re-Boot
0	Disable (default)
1	Enable





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Title: Apollo Lake - Power I		
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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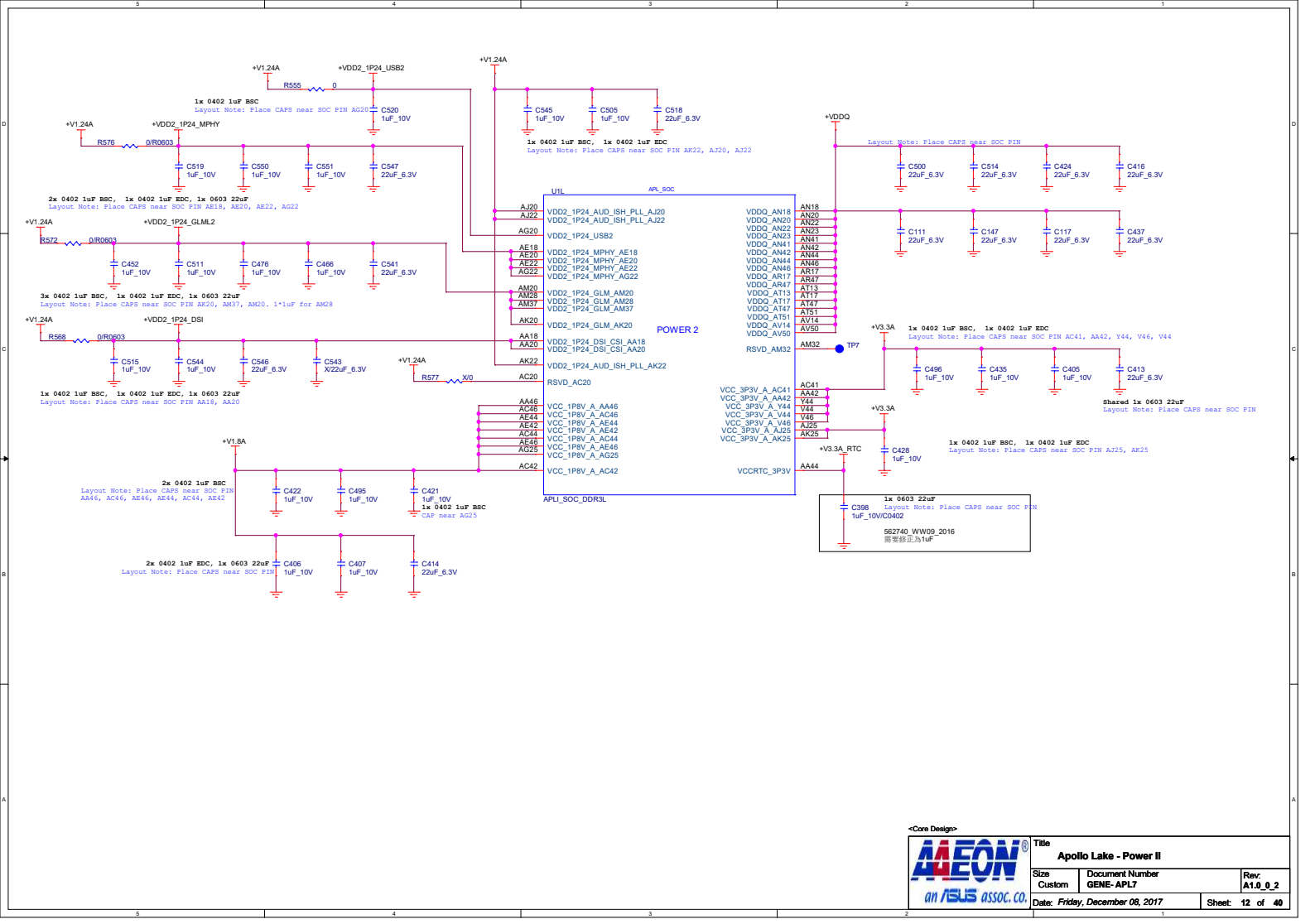

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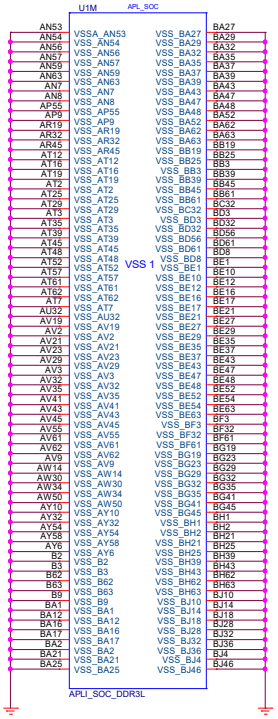
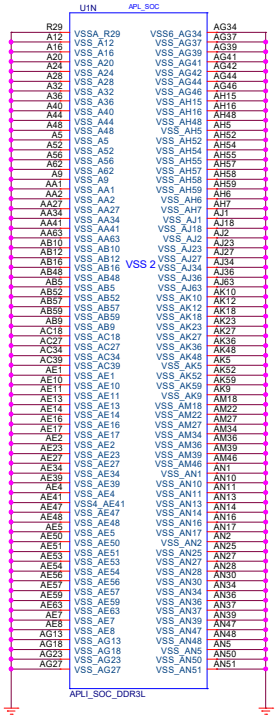
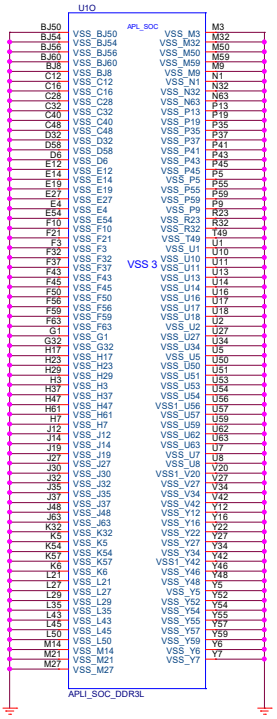
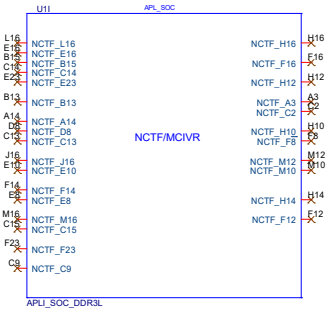
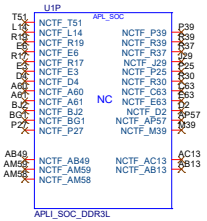
AAEON an ASUS assoc. co.	Title: Apollo Lake - Power II	
Size: Custom	Document Number: GENE- APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 12 of 40











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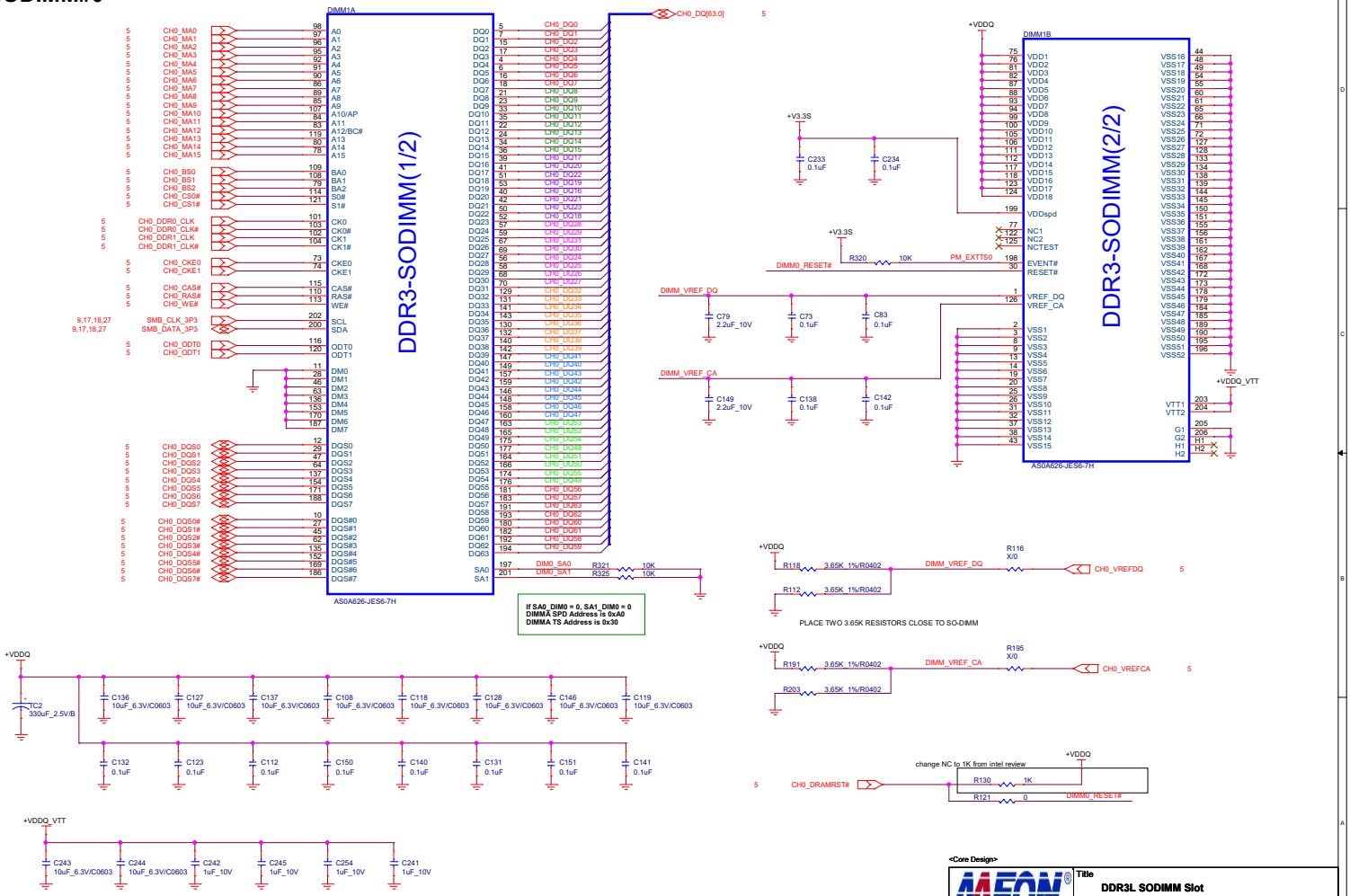
AAEON an ASUS assoc. co.	Title: Apollo Lake - GND, NC	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 13 of 40

SODIMM#0



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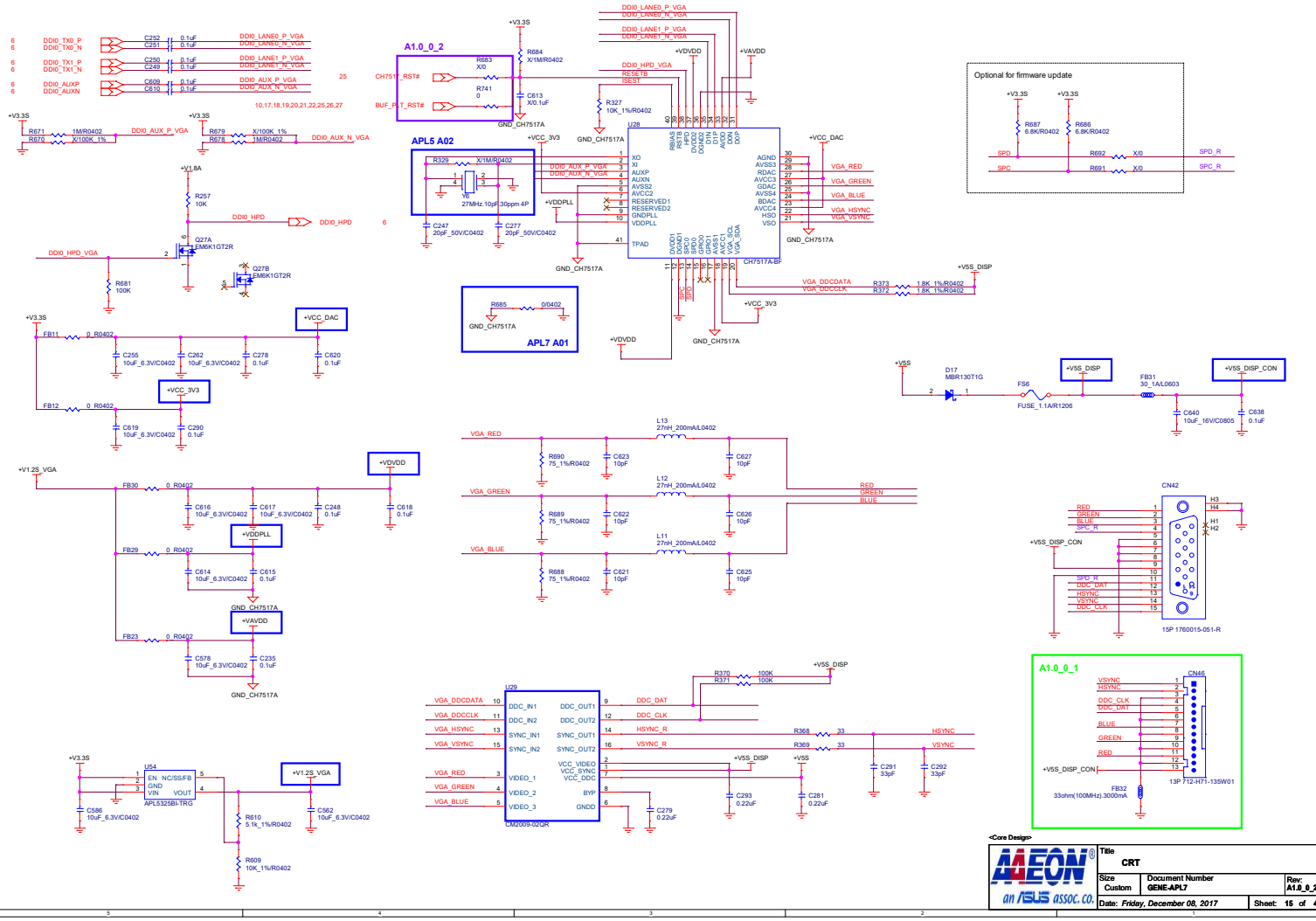
AAEON an ASUS ASSOC. CO.	Title: DDR3L SODIMM Slot	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 14 of 40

CRT

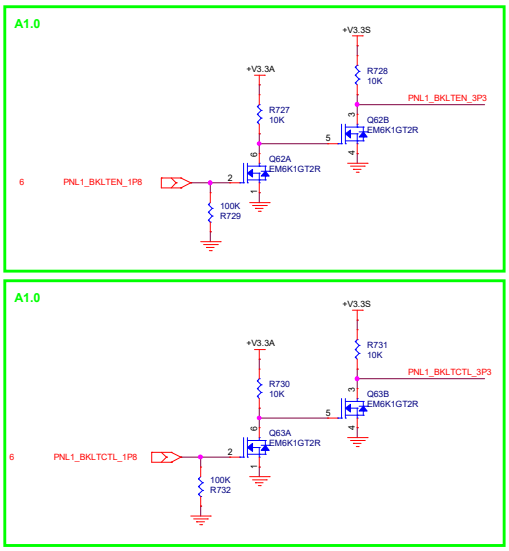


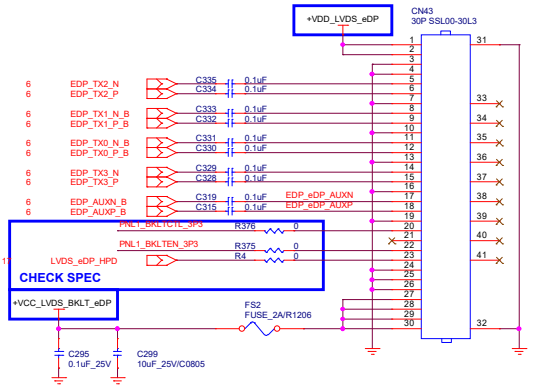
<Core Design>

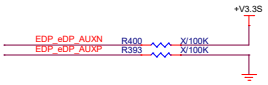
an ASUS assoc. co.

Title: CRT		
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 15 of 40

eDP







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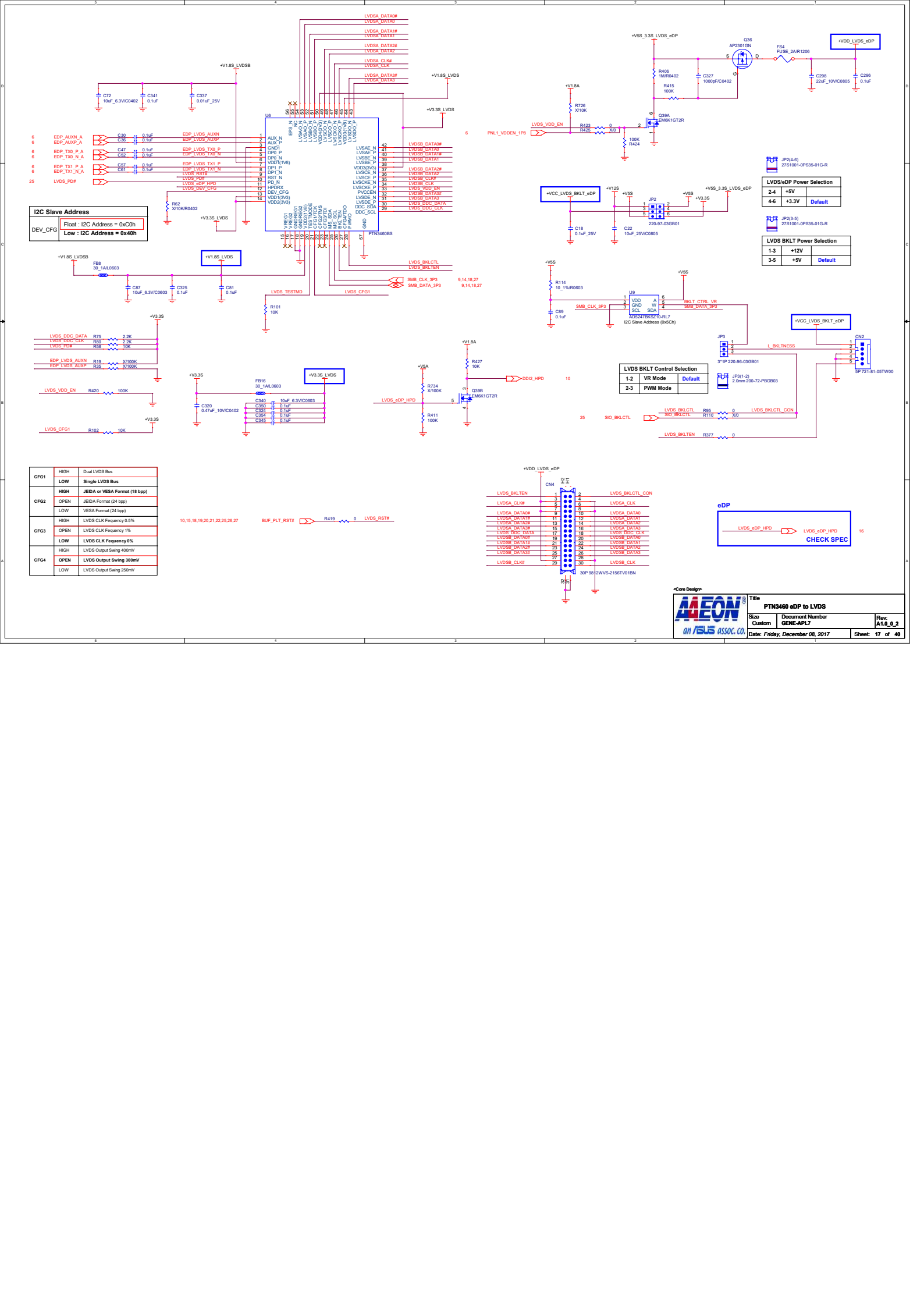
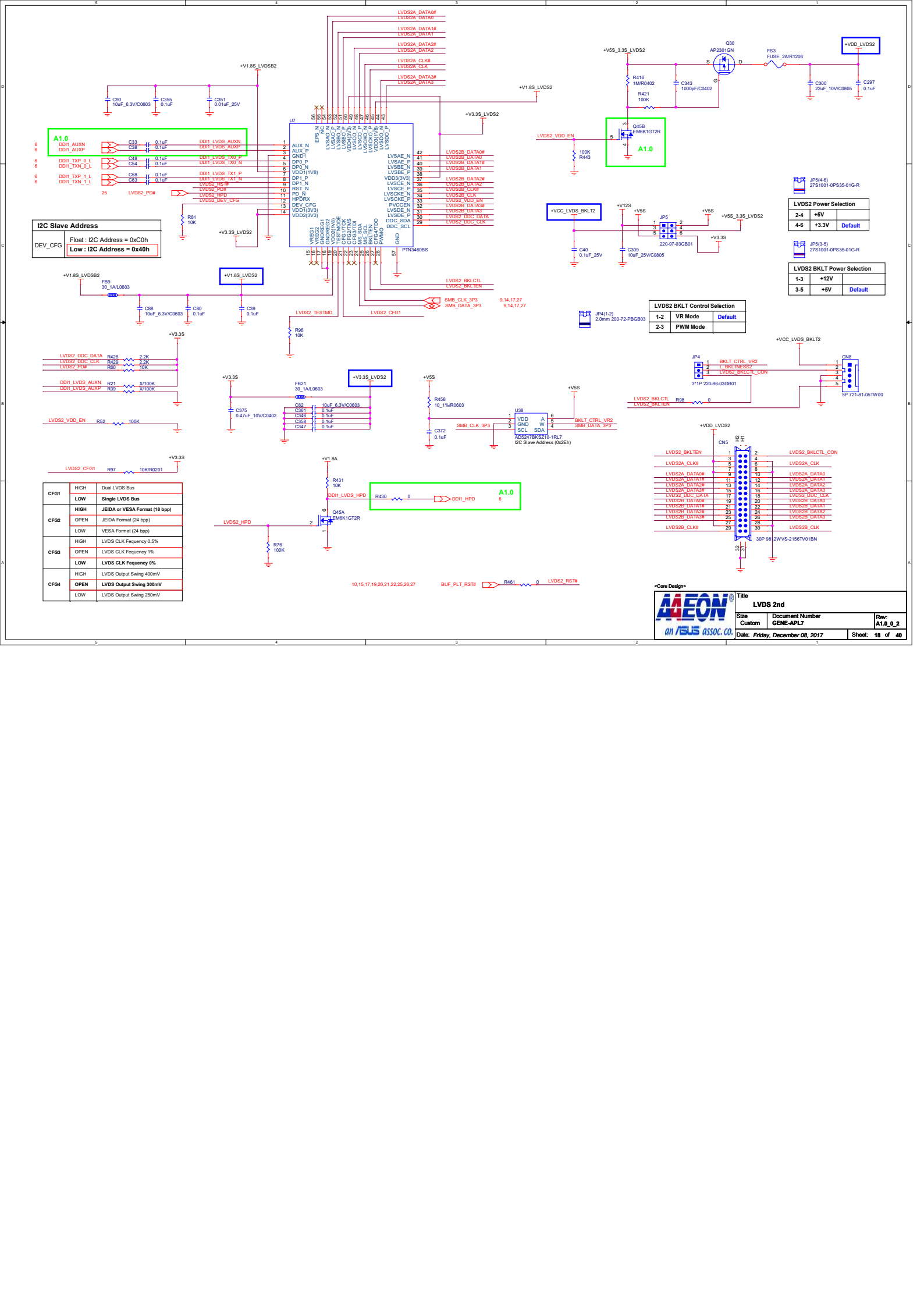
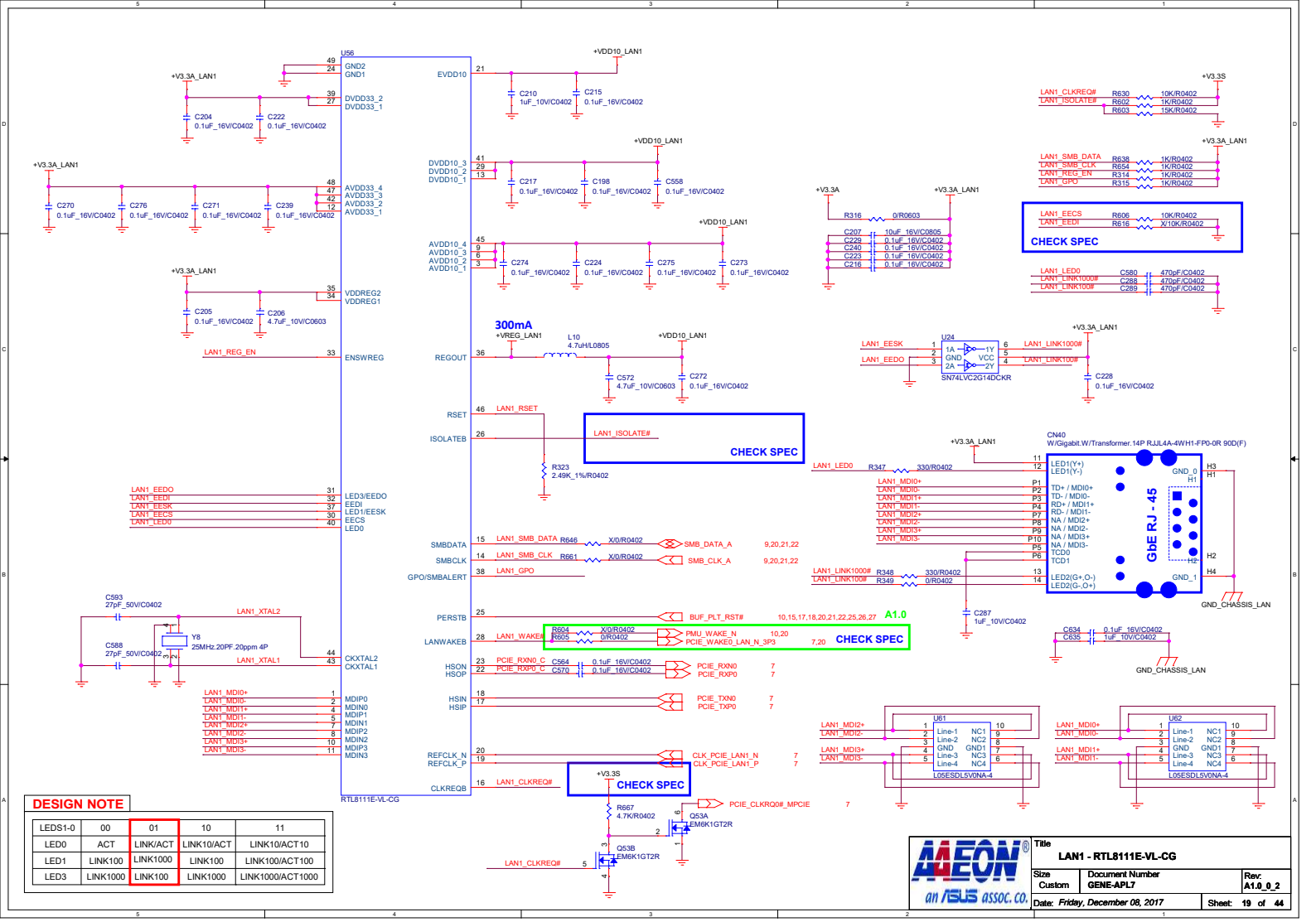
AAEON an ASUS assoc. co.	Title: eDP	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017	Sheet: 16 of 40	


I2C Slave Address
DEV_CFG
Float : I2C Address = 0xC0h
Low : I2C Address = 0x40h
LVDS/eDP Power Selection
2-4 +5V
4-6 +3.3V Default
LVDS BKLT Power Selection
1-3 +12V
3-5 +5V Default
LVDS BKLT Control Selection
1-2 VR Mode Default
2-3 PWM Mode
CFG1 HIGH Dual LVDS Bus
LOW Single LVDS Bus
CFG2 HIGH JEIDA or VESA Format (18 bpp)
OPEN JEIDA Format (24 bpp)
LOW VESA Format (24 bpp)
CFG3 HIGH LVDS CLK Fequency 0.5%
OPEN LVDS CLK Fequency 1%
LOW LVDS CLK Fequency 0%
CFG4 HIGH LVDS Output Swing 400mV
OPEN LVDS Output Swing 300mV
LOW LVDS Output Swing 250mV
eDP
CHECK SPEC
PTN3460BS
AD5247BKSZ10-RL7
I2C Slave Address (0x5Ch)
Title
PTN3460 eDP to LVDS
Size Custom
Document Number GENE-APL7
Rev. A1.0_0_2
Date: Friday, December 08, 2017
Sheet 17 of 40


I2C Slave Address
DEV_CFG
Float : I2C Address = 0xC0h
Low : I2C Address = 0x40h
LVDS2 Power Selection
2-4 +5V
4-6 +3.3V Default
LVDS2 BKLT Power Selection
1-3 +12V
3-5 +5V Default
LVDS2 BKLT Control Selection
1-2 VR Mode Default
2-3 PWM Mode
CFG1 HIGH Dual LVDS Bus
LOW Single LVDS Bus
CFG2 HIGH JEIDA or VESA Format (18 bpp)
OPEN JEIDA Format (24 bpp)
LOW VESA Format (24 bpp)
CFG3 HIGH LVDS CLK Fequency 0.5%
OPEN LVDS CLK Fequency 1%
LOW LVDS CLK Fequency 0%
CFG4 HIGH LVDS Output Swing 400mV
OPEN LVDS Output Swing 300mV
LOW LVDS Output Swing 250mV
<Core Design>
Title
LVDS 2nd
Size Custom
Document Number GENE-APL7
Rev: A1.0_0_2
Date: Friday, December 08, 2017
Sheet: 18 of 40



DESIGN NOTE

LEDS1-0	00	01	10	11
LED0	ACT	LINK/ACT	LINK10/ACT	LINK10/ACT10
LED1	LINK100	LINK1000	LINK100	LINK100/ACT100
LED3	LINK1000	LINK100	LINK1000	LINK1000/ACT1000

Title	LAN1 - RTL8111E-VL-CG		
Size: Custom	Document Number: GENE-APL7		Rev: A1.0_0_2
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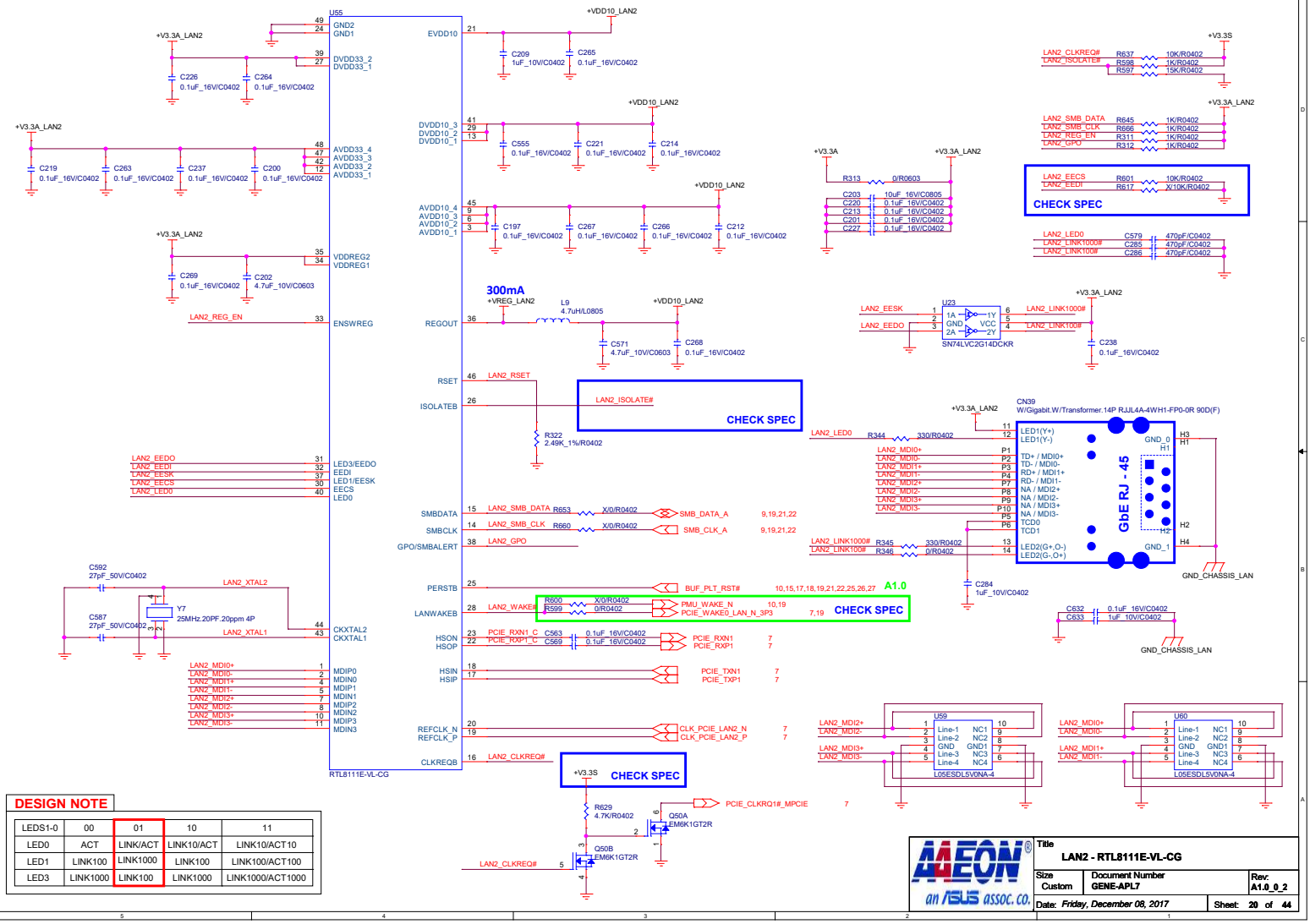
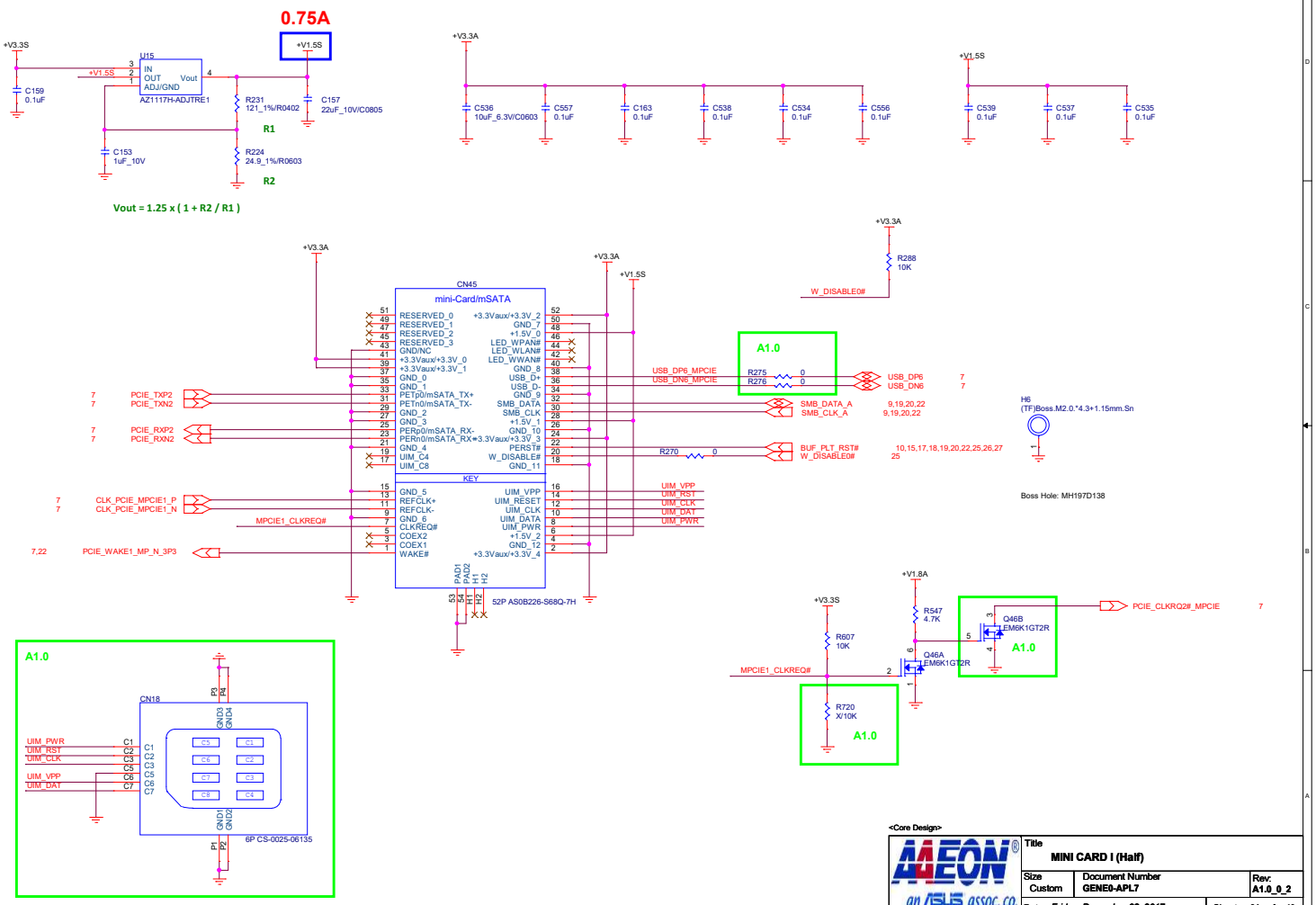


DESIGN NOTE

LEDS1-0	00	01	10	11
LED0	ACT	LINK/ACT	LINK10/ACT	LINK10/ACT10
LED1	LINK100	LINK1000	LINK100	LINK100/ACT100
LED3	LINK1000	LINK100	LINK1000	LINK1000/ACT1000

Title	LAN2 - RTL8111E-VL-CG		
Size: Custom	Document Number: GENE-APL7		Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 20 of 44	

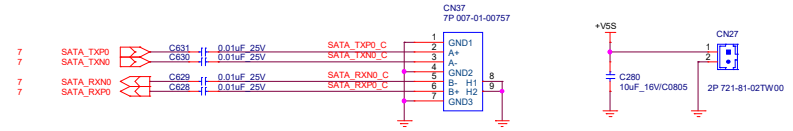


<Core Design>

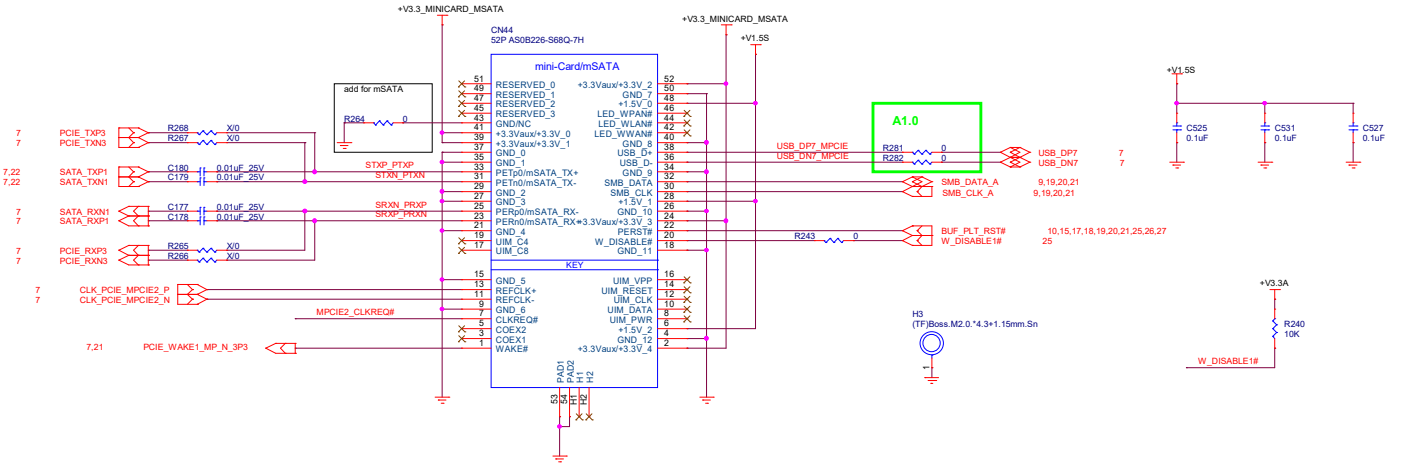
AEON an ASUS assoc. co.	Title: MINI CARD I (Half)	
	Size: Custom	Document Number: GENE0-APL7
	Date: Friday, December 08, 2017	Sheet: 21 of 40

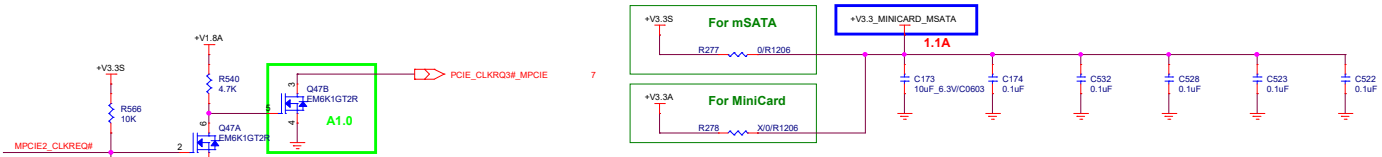
Rev: A1.0_0_2

SATA 3.0



mSATA or Mini-Card





<Core Design>
AAEON an ASUS assoc. co.

Title		
SATA, mSATA/MINI CARD		
Size: Custom	Document Number: GENE0-APL7	Rev: A1.0_0_2
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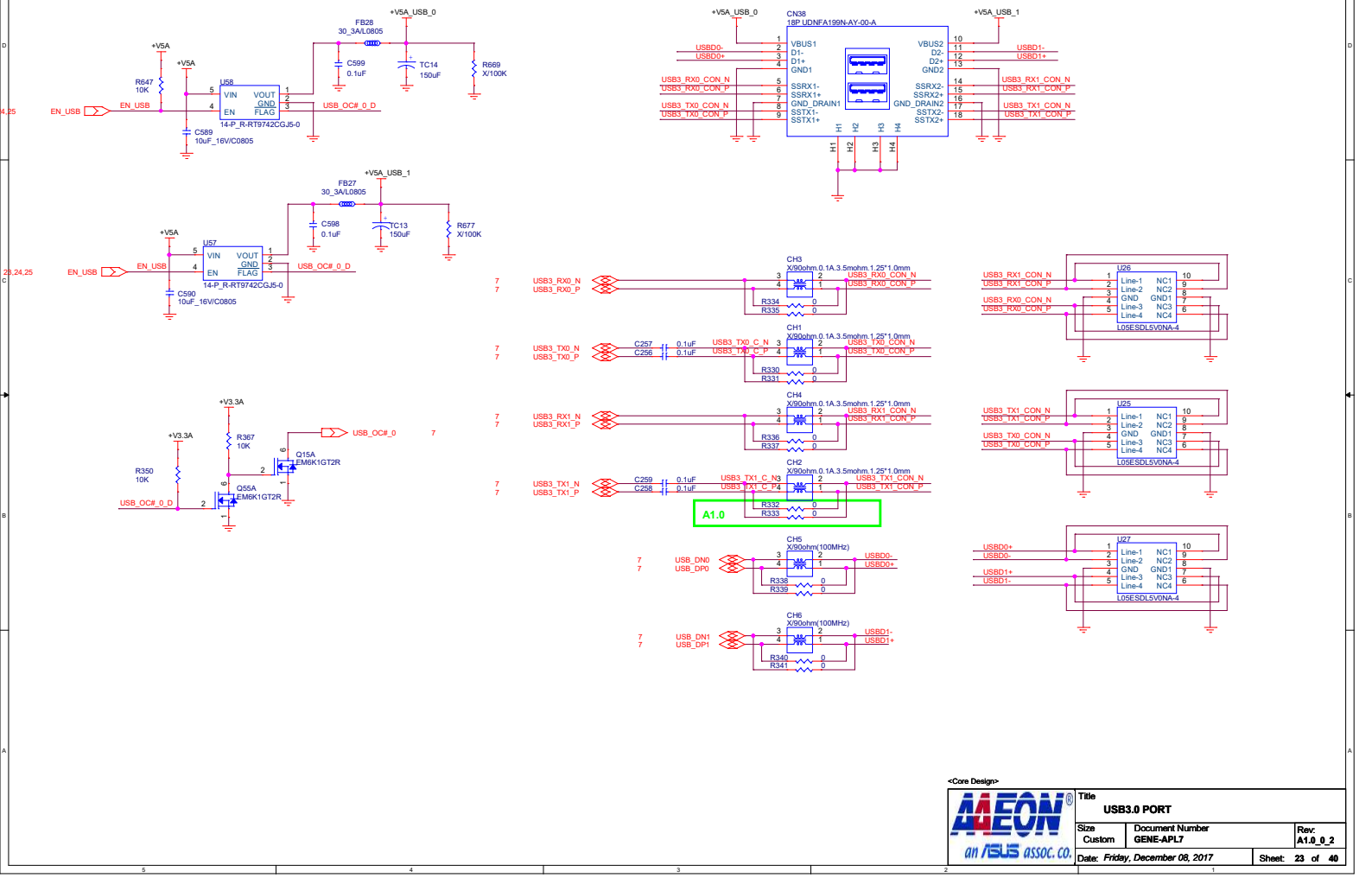
7,22 SATA_TXN1
7,22 SATA_TXP1

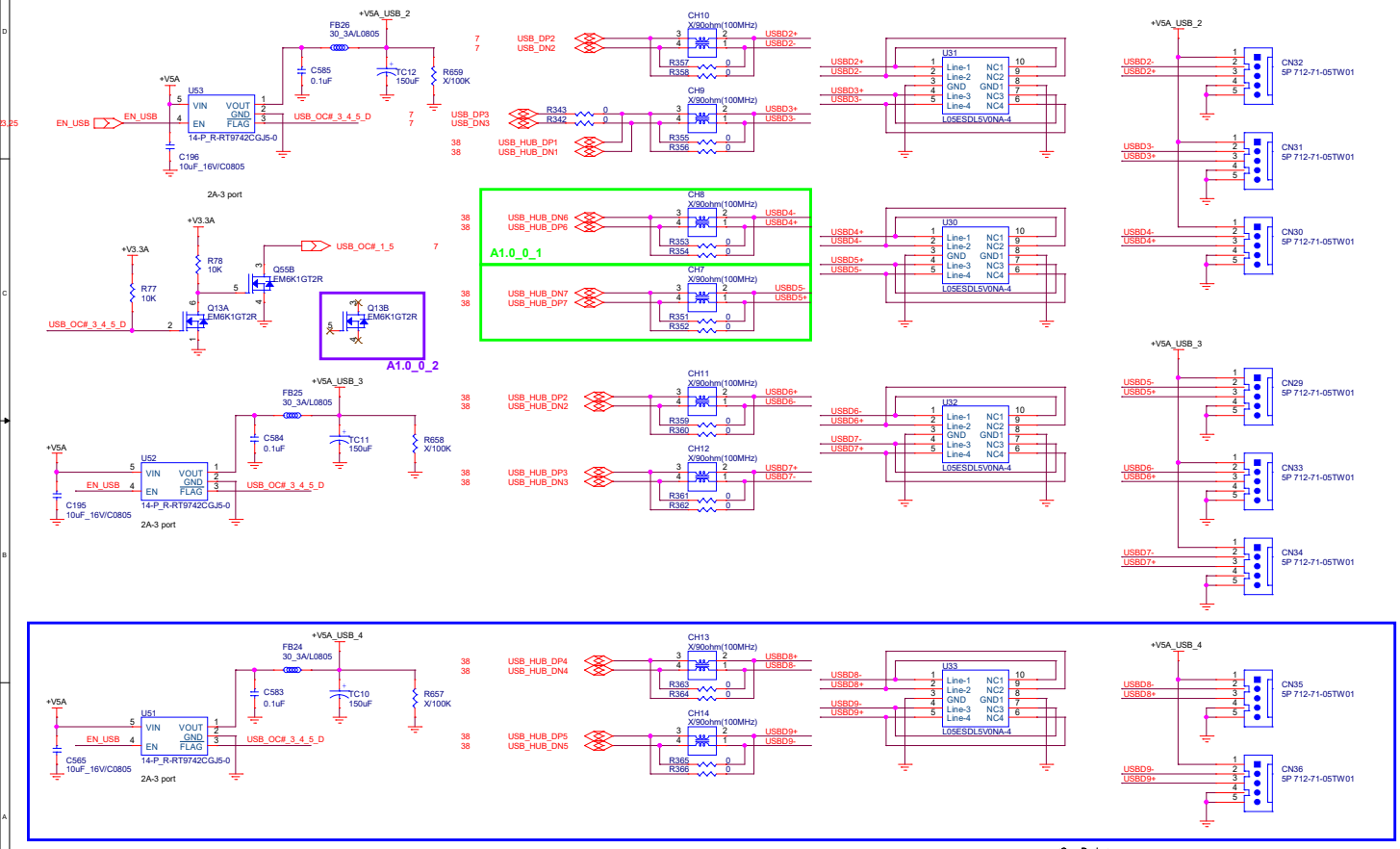
USB3.0 x 2 + USB2.0 x 2



<Core Design>

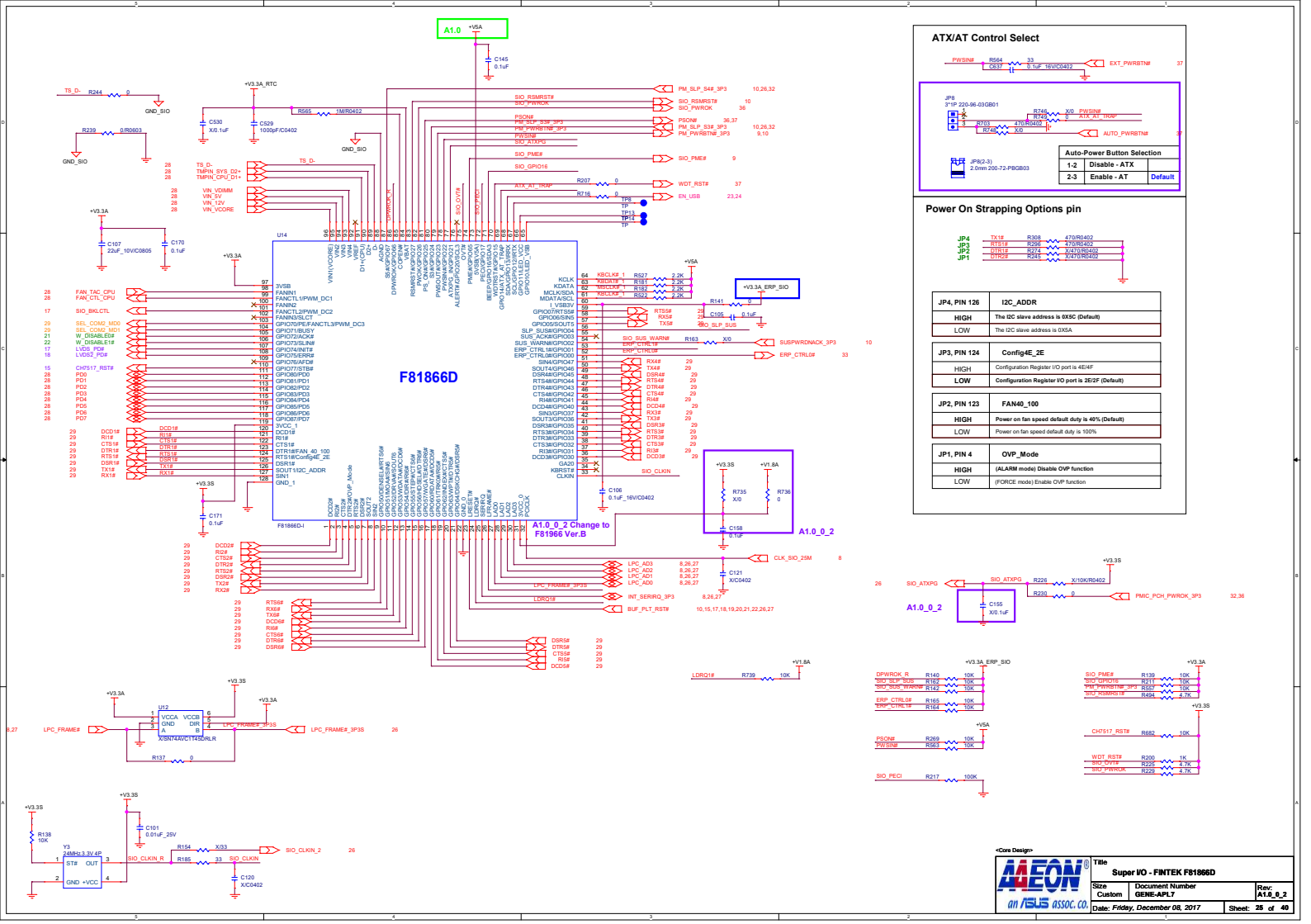
AAEON an ASUS assoc. co.	Title: USB3.0 PORT	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 23 of 40

USB2.0 x 6



<Core Design>

AAEON an /SUS assoc. co.	Title: USB2.0 PORT	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
Date: Friday, December 08, 2017		Sheet: 24 of 40


A1.0
F81866D
A1.0_0_2 Change to F81966 Ver.B
A1.0_0_2
ATX/AT Control Select
Auto-Power Button Selection
1-2 Disable - ATX
2-3 Enable - AT Default
Power On Strapping Options pin
JP4 JP3 JP2 JP1
JP4, PIN 126 I2C_ADDR
HIGH The I2C slave address is 0X5C (Default)
LOW The I2C slave address is 0X5A
JP3, PIN 124 Config4E_2E
HIGH Configuration Register I/O port is 4E/4F
LOW Configuration Register I/O port is 2E/2F (Default)
JP2, PIN 123 FAN40_100
HIGH Power on fan speed default duty is 40% (Default)
LOW Power on fan speed default duty is 100%
JP1, PIN 4 OVP_Mode
HIGH (ALARM mode) Disable OVP function
LOW (FORCE mode) Enable OVP function
<Core Design>
Title
Super I/O - FINTEK F81866D
Size Custom
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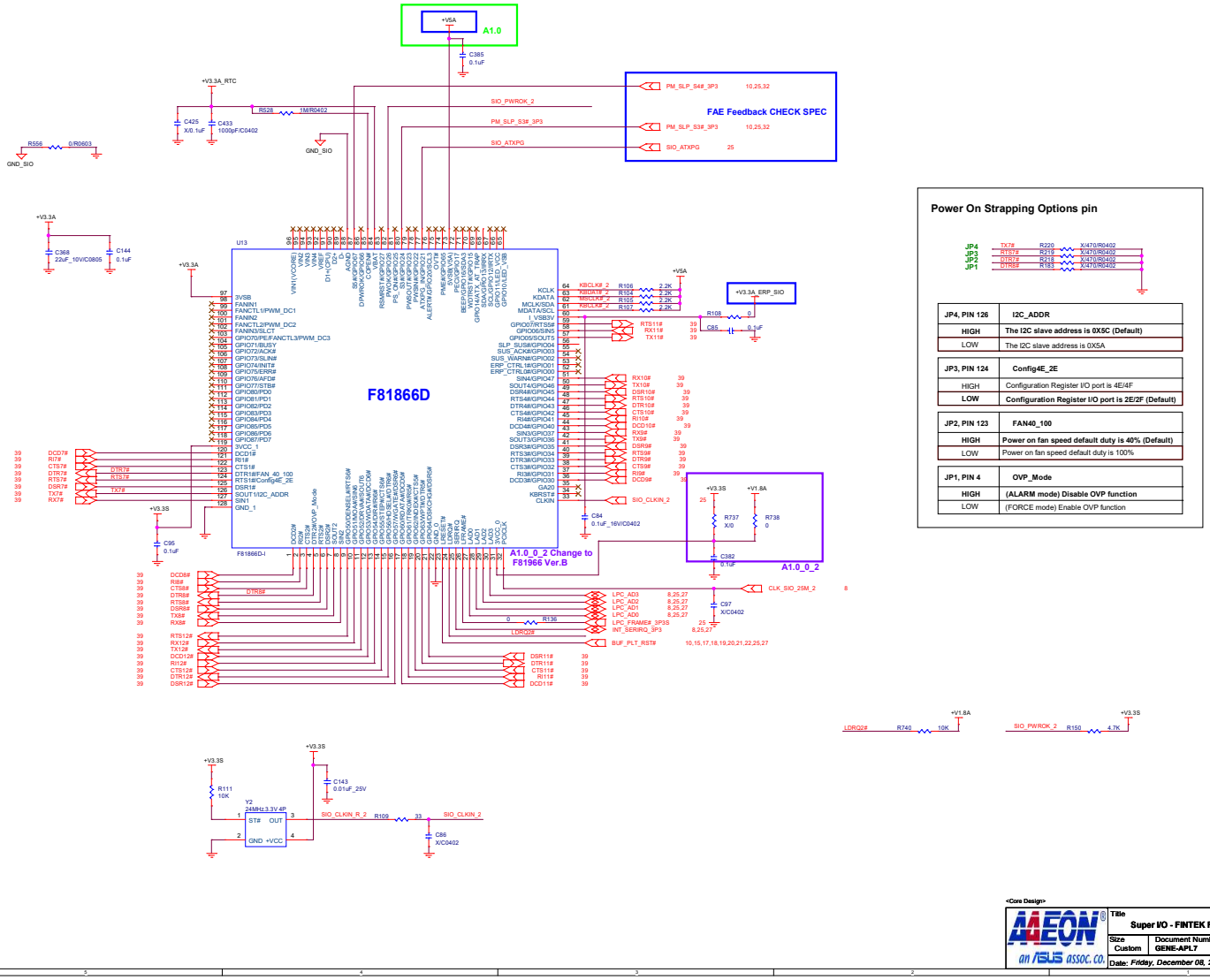

Power On Strapping Options pin

JP4	TX7#	R220	X/470/R0402
JP3	RTS7#	R219	X/470/R0402
JP2	DTR7#	R218	X/470/R0402
JP1	DTR8#	R183	X/470/R0402

JP4, PIN 126	I2C_ADDR
HIGH	The I2C slave address is 0X5C (Default)
LOW	The I2C slave address is 0X5A

JP3, PIN 124	Config4E_2E
HIGH	Configuration Register I/O port is 4E/4F
LOW	Configuration Register I/O port is 2E/2F (Default)

JP2, PIN 123	FAN40_100
HIGH	Power on fan speed default duty is 40% (Default)
LOW	Power on fan speed default duty is 100%

JP1, PIN 4	OVP_Mode
HIGH	(ALARM mode) Disable OVP function
LOW	(FORCE mode) Enable OVP function

<Core Design>

Title	Super I/O - FINTEK F81866D	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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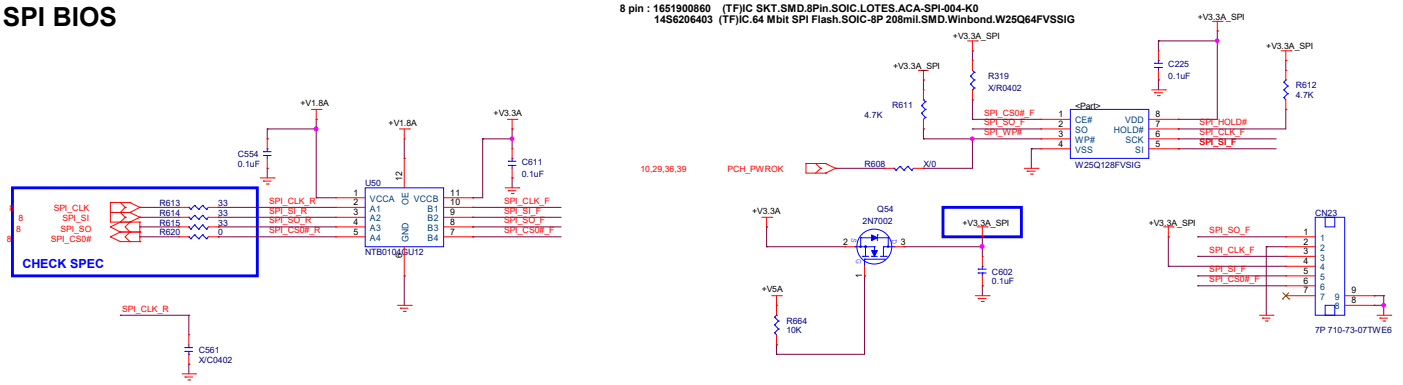
an ASUS assoc. co.

SPI BIOS

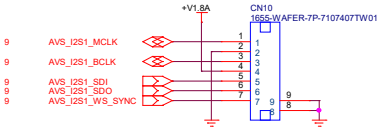
8 pin : 1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0
14S6206403 (TF)IC.64 Mbit SPI Flash.SOIC-8P 208mil.SMD.Winbond.W25Q64FVSSIG



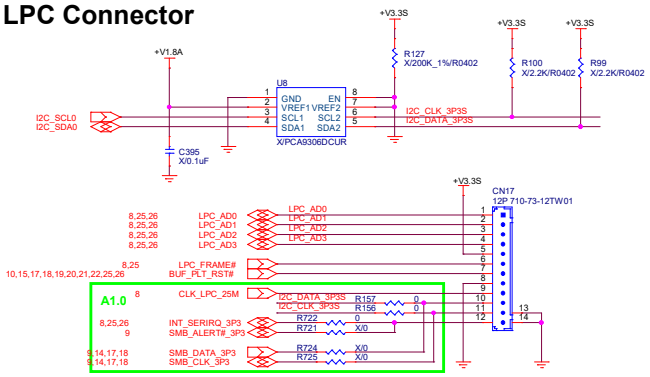
CMOS Backup

N/A

I2S Connector



LPC Connector



<Core Design>

Title: SPI BIOS,CMOS BACKUP,I2S		
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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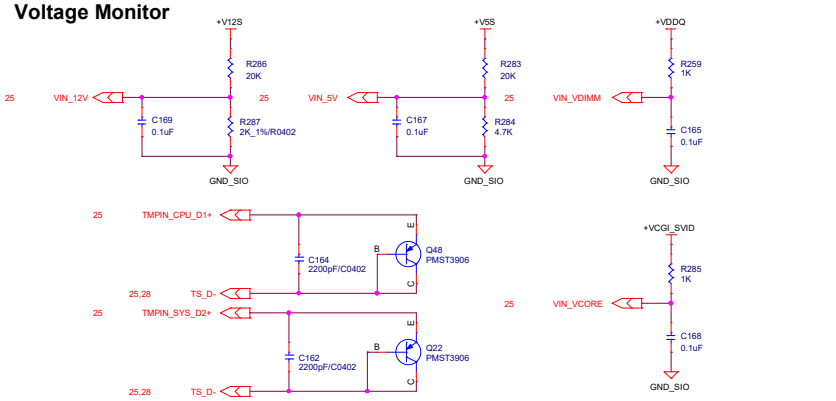
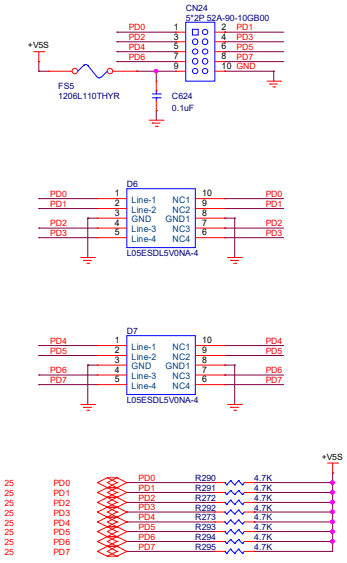
PS/2 Keyboard/Mouse

N/A

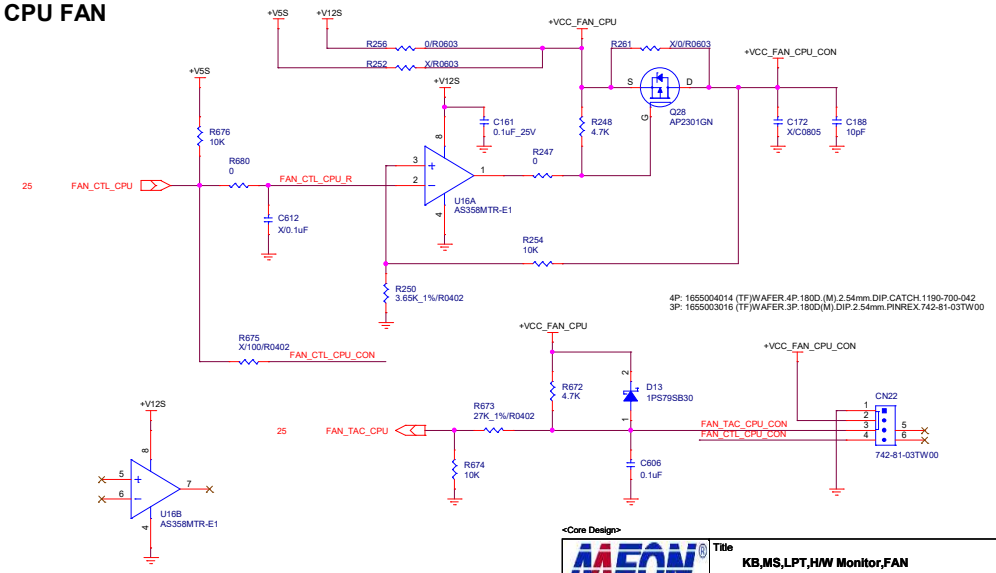
Voltage Monitor



DIO



CPU FAN



<Core Design>

AAEON an ASUS assoc. co.	Title: KB,MS,LPT,H/W Monitor,FAN	
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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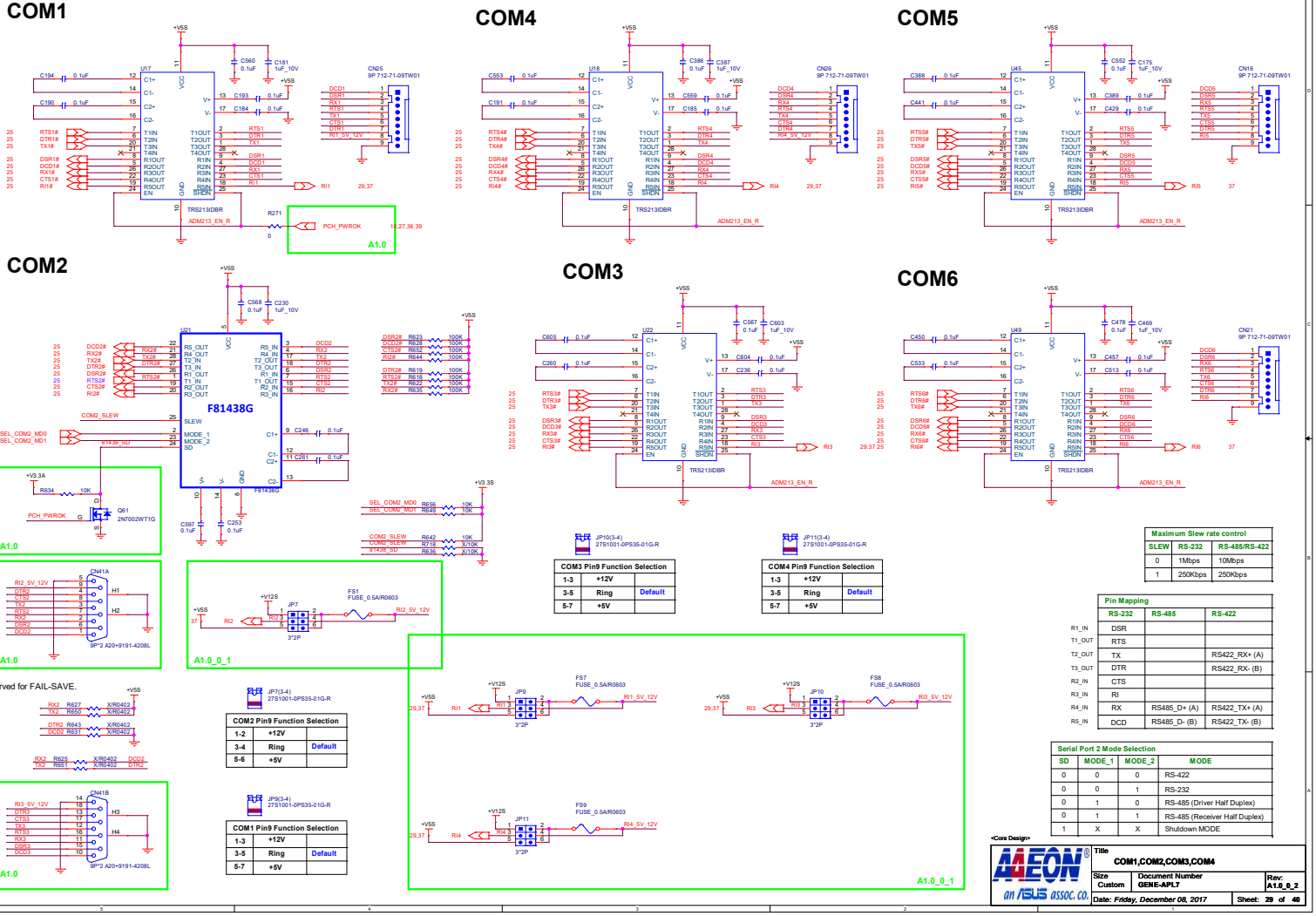
COM1
COM4
COM5
COM2
COM3
COM6
F81438G
TRS213IDBR
ADM213_EN_R
A1.0
A1.0_0_1
Reserved for FAIL-SAVE.
COM2_SLEW
PCH_PWROK
JP10(3-4) 27S1001-0PS35-01G-R
JP11(3-4) 27S1001-0PS35-01G-R
JP7(3-4) 27S1001-0PS35-01G-R
JP9(3-4) 27S1001-0PS35-01G-R
COM3 Pin9 Function Selection
COM4 Pin9 Function Selection
COM2 Pin9 Function Selection
COM1 Pin9 Function Selection
1-3 +12V
3-5 Ring Default
5-7 +5V
Maximum Slew rate control
SLEW RS-232 RS-485/RS-422
0 1Mbps 10Mbps
1 250Kbps 250Kbps
Pin Mapping
RS-232 RS-485 RS-422
R1_IN DSR
T1_OUT RTS
T2_OUT TX RS422_RX+ (A)
T3_OUT DTR RS422_RX- (B)
R2_IN CTS
R3_IN RI
R4_IN RX RS485_D+ (A) RS422_TX+ (A)
R5_IN DCD RS485_D- (B) RS422_TX- (B)
Serial Port 2 Mode Selection
SD MODE_1 MODE_2 MODE
0 0 0 RS-422
0 0 1 RS-232
0 1 0 RS-485 (Driver Half Duplex)
0 1 1 RS-485 (Receiver Half Duplex)
1 X X Shutdown MODE
<Core Design>
AAEON an ASUS assoc. co.
Title COM1,COM2,COM3,COM4
Size Custom
Document Number GENE-APL7
Rev: A1.0_0_2
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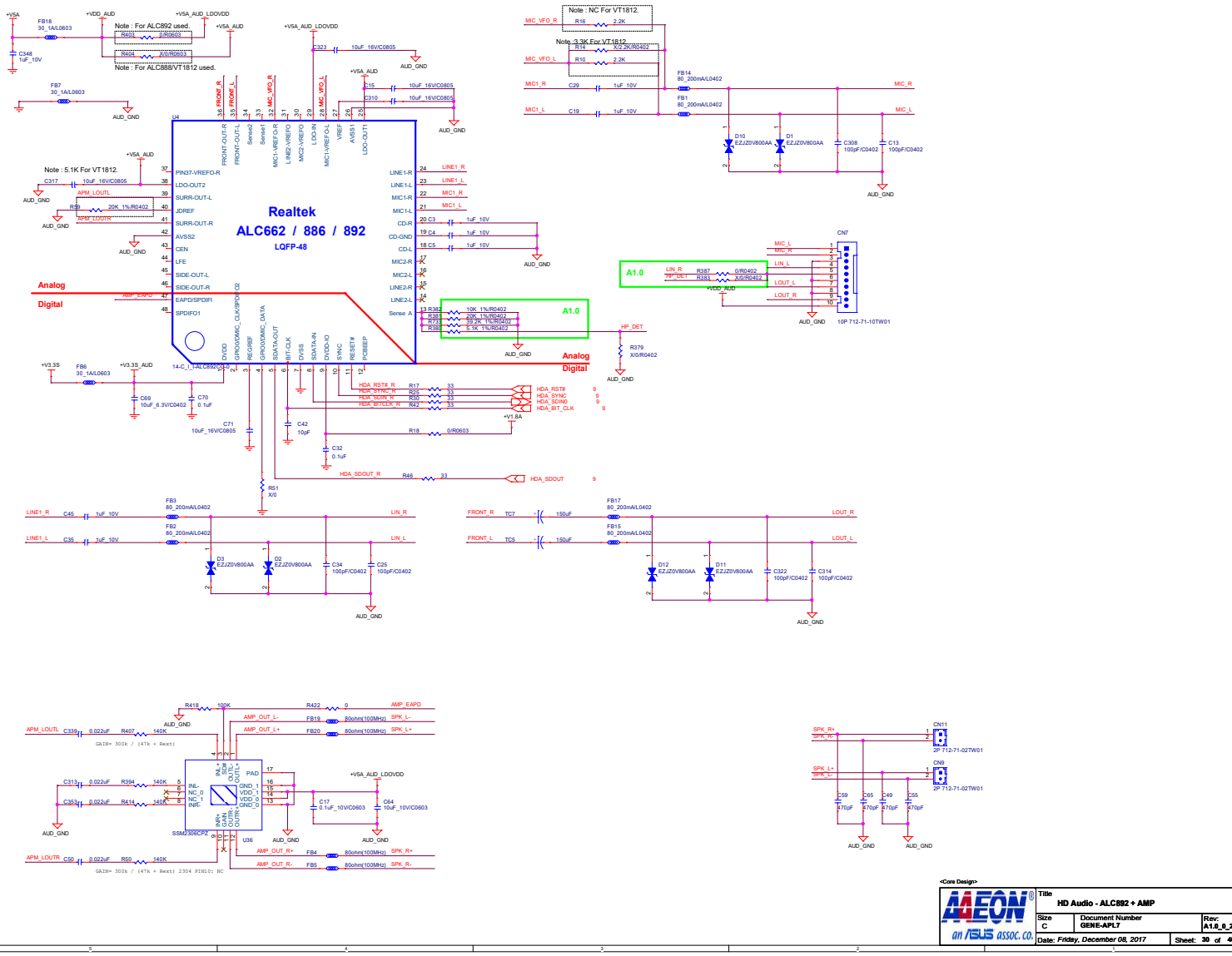

<Core Design>

Title: HD Audio - ALC892 + AMP		
Size: C	Document Number: GENE-APL7	Rev: A1.0_0_2
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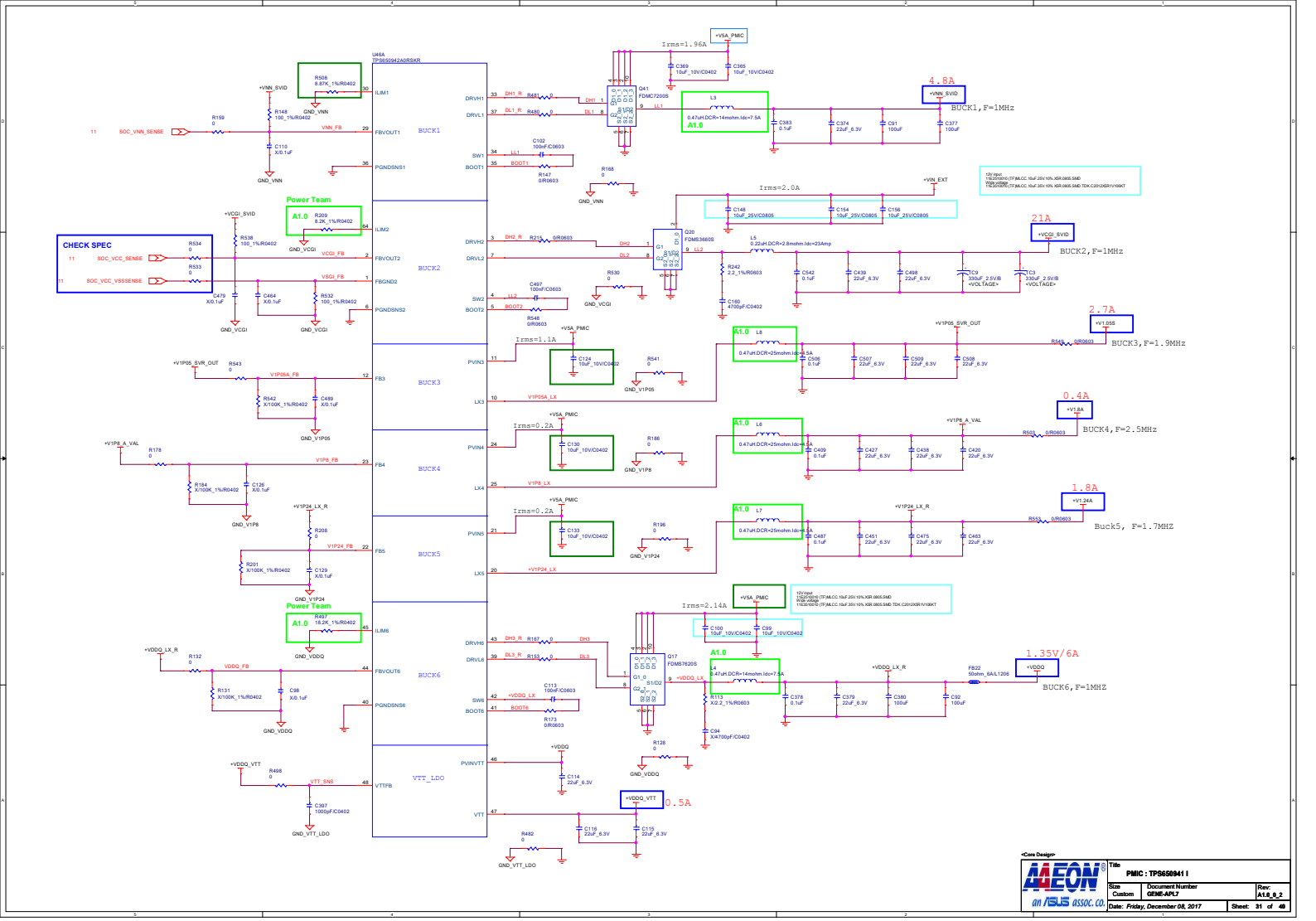
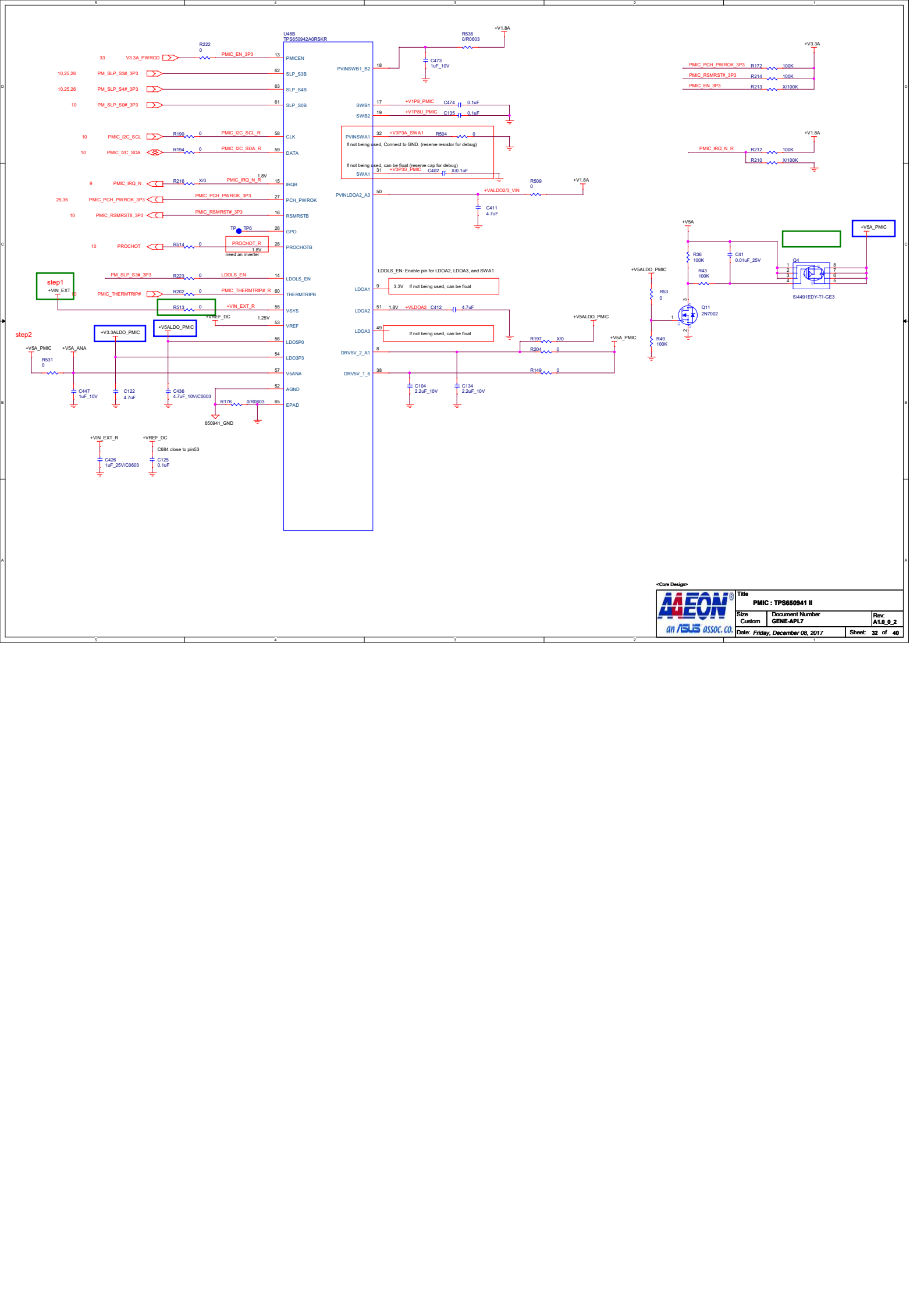

U46A
TPS650942A0RSKR
BUCK1
BUCK2
BUCK3
BUCK4
BUCK5
BUCK6
VTT_LDO
ILIM1
FBVOUT1
PGNDSNS1
ILIM2
FBVOUT2
FBGND2
PGNDSNS2
FB3
FB4
FB5
ILIM6
FBVOUT6
PGNDSNS6
VTTFB
DRVH1
DRVL1
SW1
BOOT1
DRVH2
DRVL2
SW2
BOOT2
PVIN3
LX3
PVIN4
LX4
PVIN5
LX5
DRVH6
DRVL6
SW6
BOOT6
PVINVTT
VTT
+VSA_PMIC
Irms=1.96A
4.8A
+VNN_SVID
BUCK1,F=1MHz
Irms=2.0A
+VIN_EXT
21A
+VCGI_SVID
BUCK2,F=1MHz
Irms=1.1A
2.7A
+V1.05S
BUCK3,F=1.9MHz
Irms=0.2A
0.4A
+V1.8A
BUCK4,F=2.5MHz
Irms=0.2A
1.8A
+V1.24A
Buck5, F=1.7MHZ
Irms=2.14A
1.35V/6A
+VDDQ
BUCK6,F=1MHZ
0.5A
+VDDQ_VTT
CHECK SPEC
SOC_VCC_SENSE
SOC_VCC_VSSSENSE
SOC_VNN_SENSE
Power Team
A1.0
GND_VNN
GND_VCGI
GND_V1P05
GND_V1P8
GND_V1P24
GND_VDDQ
GND_VTT_LDO
Q41
FDMC7200S
Q30
FDMB3660S
Q17
FDMS7620S
L3
0.47uH.DCR=14mohm.Idc=7.5A
L5
0.22uH.DCR=2.8mohm.Idc=23Amp
L8
0.47uH.DCR=25mohm.Idc=9.5A
L6
0.47uH.DCR=25mohm.Idc=9.5A
L7
0.47uH.DCR=25mohm.Idc=9.5A
L4
0.47uH.DCR=14mohm.Idc=7.5A


U46B
TPS650942A0RSKR
PMICEN
SLP_S3B
SLP_S4B
SLP_S0B
CLK
DATA
IRQB
PCH_PWROK
RSMRSTB
GPO
PROCHOTB
LDOLS_EN
THERMTRIPB
VSYS
VREF
LDO5P0
LDO3P3
V5ANA
AGND
EPAD
PVINSWB1_B2
SWB1
SWB2
PVINSWA1
SWA1
PVINLDOA2_A3
LDOA1
LDOA2
LDOA3
DRV5V_2_A1
DRV5V_1_6
LDOLS_EN: Enable pin for LDOA2, LDOA3, and SWA1.
If not being used, Connect to GND. (reserve resistor for debug)
If not being used, can be float (reserve cap for debug)
If not being used, can be float
If not being used, can be float
need an inverter
step1
step2
650941_GND
C684 close to pin53
Si4491EDY-T1-GE3
Q11
2N7002
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Title
PMIC : TPS650941 II
Size
Custom
Document Number
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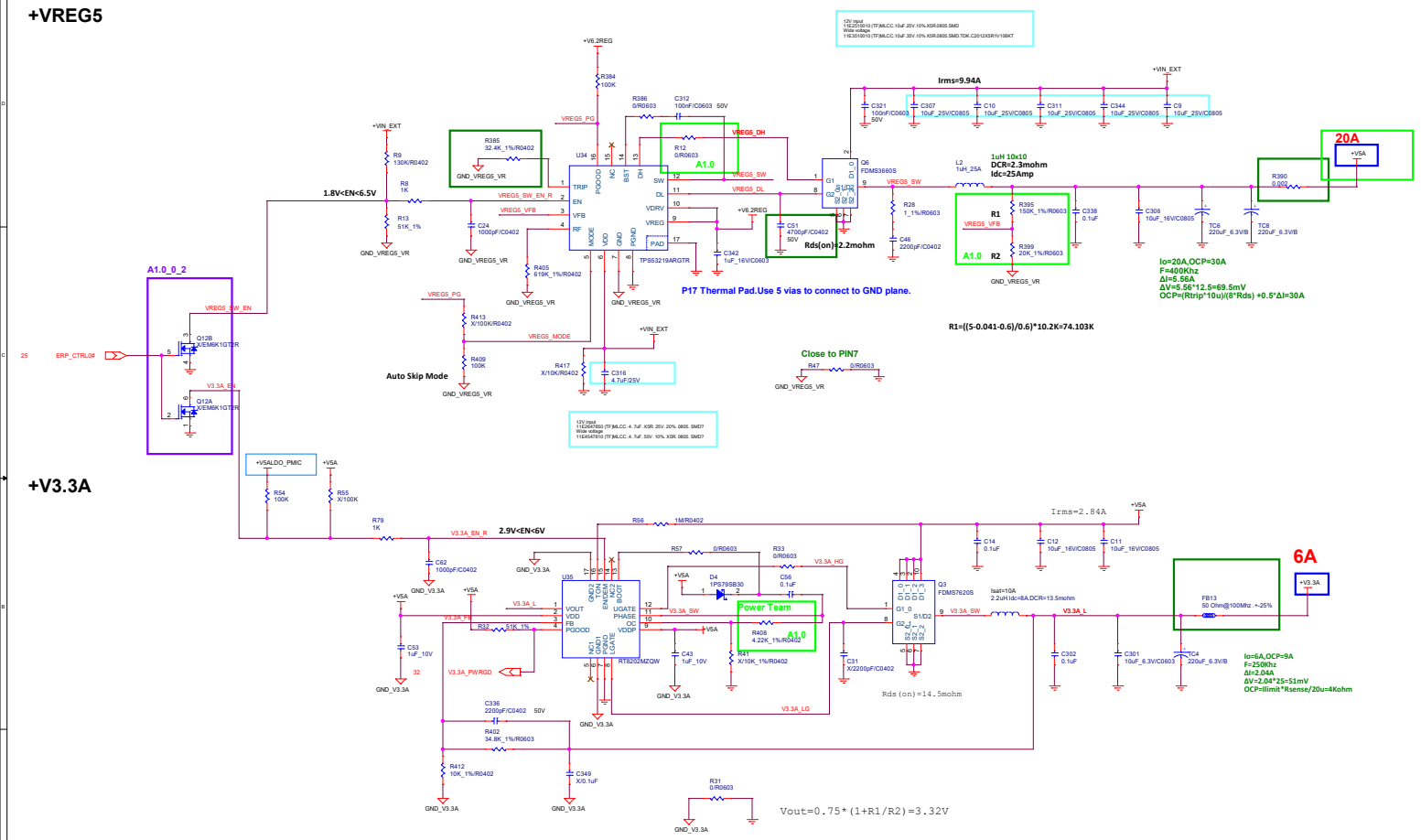
+VREG5



+V3.3A

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ASUSTeK COMPUTER INC.	Title: POWER VR: +VREG5, +V3.3A	
	Size: Custom	Document Number: GENE-APL7 Rev: A1.0_0_2
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A1.0 Remove

<Core Design>

Title: POWER +V12A		
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5VDAUL Switch Circuit

A1.0 Remove

Powering ERP well of SIO

A1.0 Remove

<Core Design>

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Title: Standby Power		
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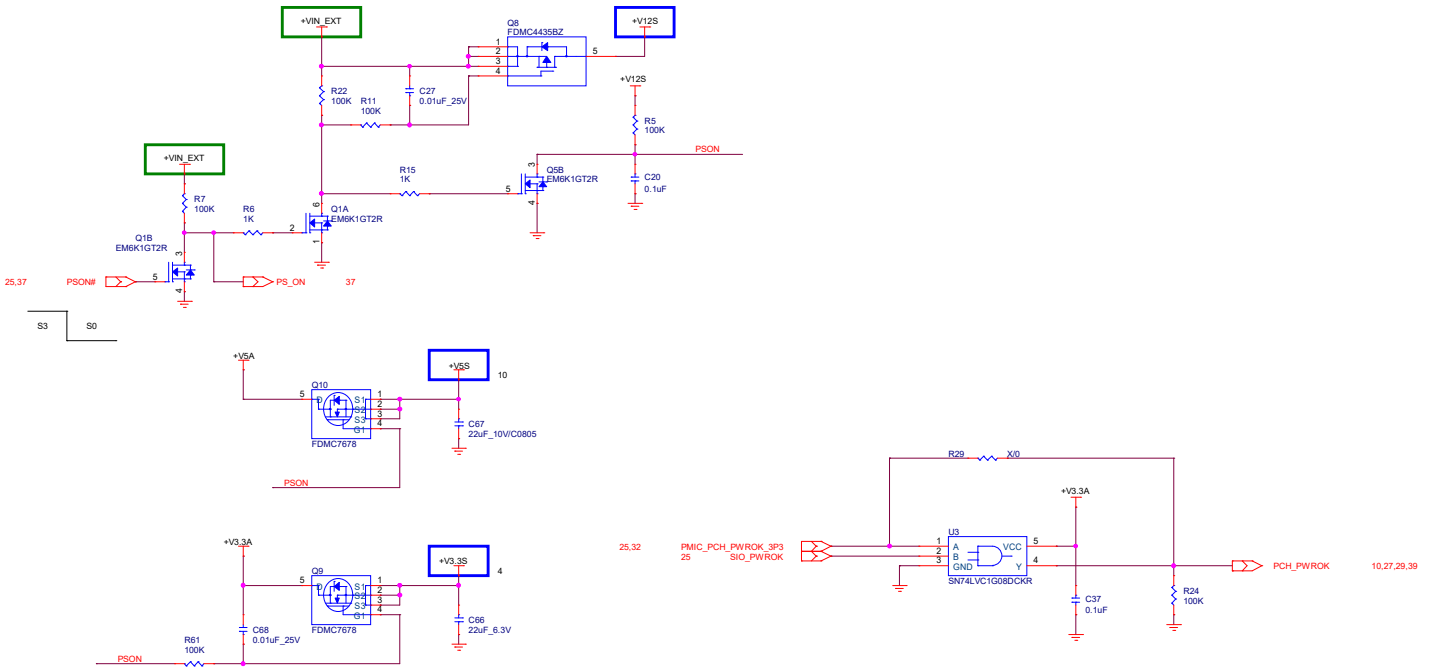

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Title: System Power		
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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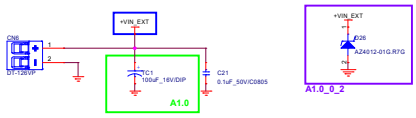
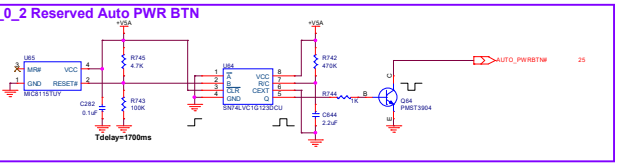
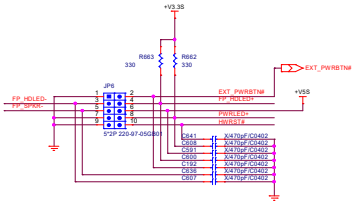
Power Input



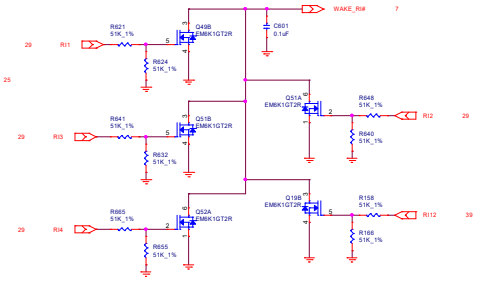
A1.0_0_2 Reserved Auto PWR BTN



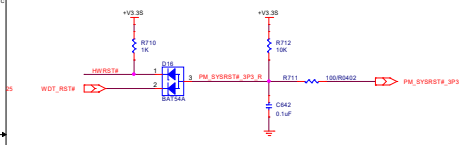
Front Panel



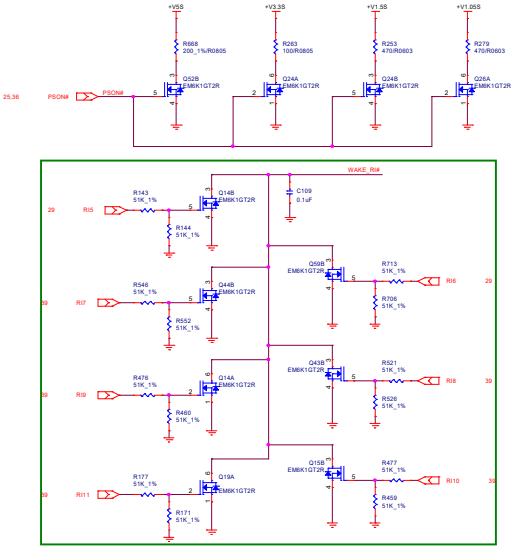
Wake On Modem



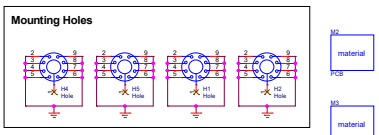
Reset Circuit



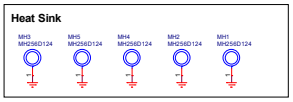
Discharge Circuit



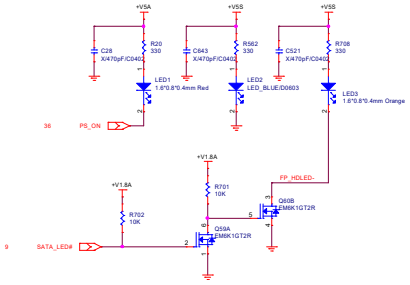
Mounting Holes



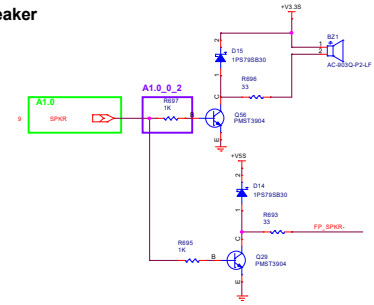
Heat Sink



LED



Speaker



Title: Power Input,Misc		
Size: Custom	Document Number: GENE-APL7	Rev: A1.0_0_2
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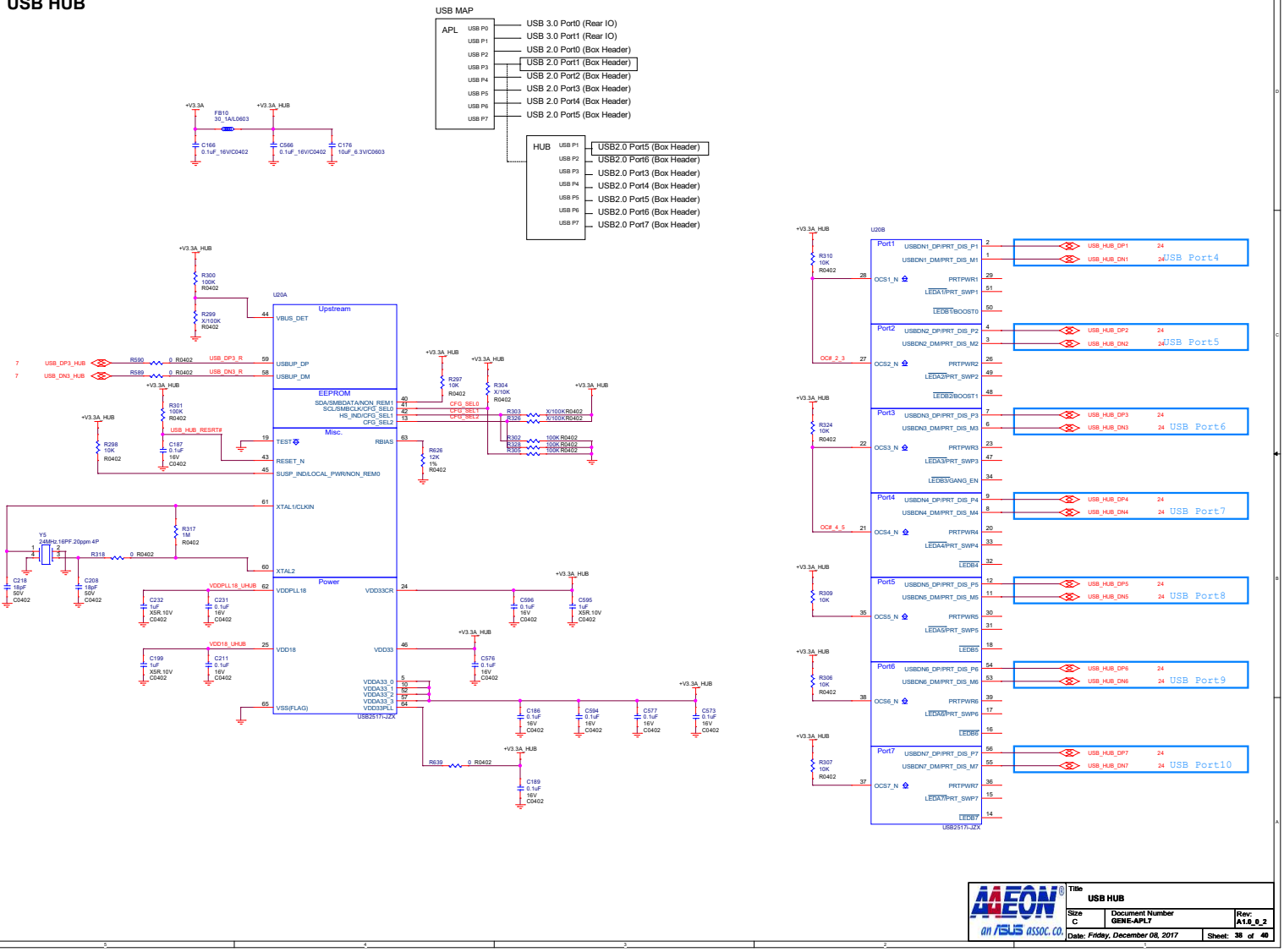
USB HUB



Title: USB HUB			
Size: C	Document Number: GENE-APL7		Rev: A1.8_0_2
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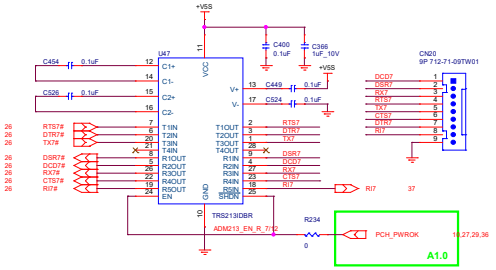
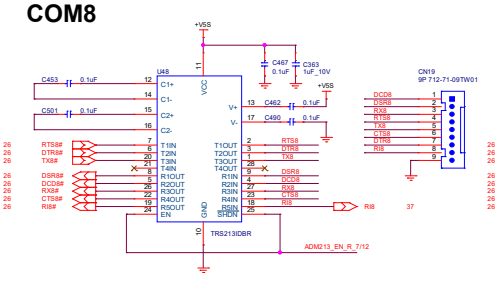
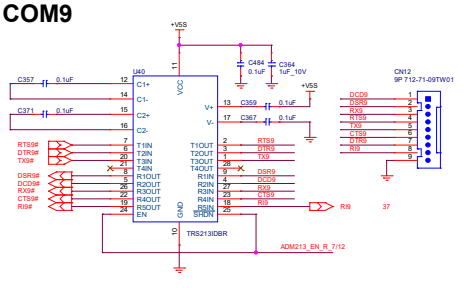
COM7



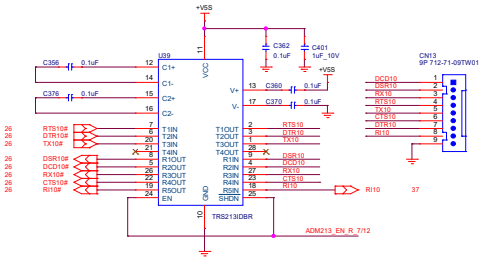
COM8



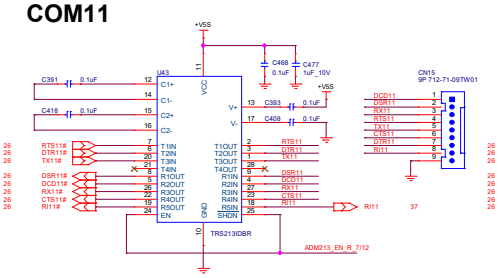
COM9



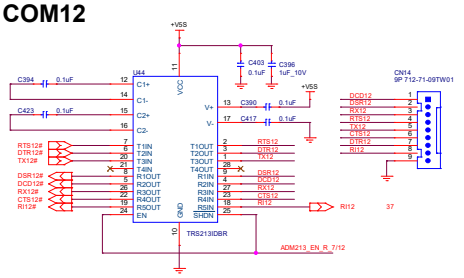
COM10



COM11



COM12



<Core Design>

AAEON an ASUS assoc. co.	Title: COM7,COM8,COM9,COM10,COM11,COM12	
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HISTORY

Item	Date	Revision	Page	Modification List	Reason
1	2016/09/12	A0.1		First Release	Release and follow GENE-APL5 A0.2 modify lists.
1	2016/12/13	A1.0	06	DDI1_TXP_1_L, DDI1_TXN_1_L, DDI1_TXP_0_L, DDI1_TXN_0_L DSN modifications	R&D Internal modifications
			09	GPIO_PWRBTN# DSN modifications	R&D Internal modifications (APL team suggest)
			09	Add Q43A, R723 for SMB_ALERT#_3P3	R&D Internal modifications (ECD expert suggest)
			10	D5, D8, D9 change the part number to 1301793040	R&D Internal modifications
			16	eDP PNL1_BKLTEN_3P3, PNL1_BKLTCTL_3P3 level shifter Q62, Q63	R&D Internal modifications
			18	C33, C38 for DDI1_AUXN and DDI1_AUXP	R&D Internal modifications
			18	R430 for DDI1_HPD	R&D Internal modifications
			21	Add CN18 for uSIM	R&D Internal modifications
			21	Add R720 for PCIE_CLKRQ2#_MPCIE	R&D Internal modifications
			22	Add R719 for PCIE_CLKRQ3#_MPCIE	R&D Internal modifications
			25	U14 PIN 5VSB modifications to +V5A	R&D Internal modifications
			26	U13 PIN 5VSB modifications to +V5A	R&D Internal modifications
			27	CN17 add SMB_ALERT#_3P3, SMB_DATA_3P3, SMB_CLK_3P3	R&D Internal modifications
			29	CN41 modifications to pin define	R&D Internal modifications
			29	Add Q61 for 81438_SD pin	R&D Internal modifications
			29	R271 modifications to PCH_PWROK	R&D Internal modifications
			30	Add R733 and LIN_R	R&D Internal modifications
			31	Change R209 from 5.6K to 8.2Kohm(1050508224) for OCP adjust.	Power Team
			31	Change R497 from 10.2K to 18.2Kohm(105A518223) for OCP adjust.	Power Team
			31	L6, L7, L8 change to 121110477B	R&D Internal modifications(Cost)
			31	L4, change to 121110477A	R&D Internal modifications(Cost)
			32	R12 change to 0ohm(105A700004) for Dead time adjust.	Power Team
			33	R395, R399 change to 150K and 20K for Vout adjust.	Power Team
			37	TC1 chanhe to 1181610196	R&D Internal modifications
			39	R234 change to netname to PCH_PWROK	R&D Internal modifications
	2017/11/29	A1.0_0_2	15	CH7517 RST# change to PLT_RST#	
			08	LPC change to 1.8V(R502 unstuff, R484 stuff)	
			25,26	LPC change to 1.8V(R735,R737 unstuff, R736,R738 stuff)	
			25	Fix AC Power Loss (remove C155)	
			25,26	Change F81966(1440819661) to new version	
			33	Remove Q12 (no ERP function)	
			37	Add D26 for ESD protection	

<Core Design>

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Title: Revision History

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