



PIN	Name	0	1	Power	Description
31	2E_4E_SEL	2E	4E	vcc	I/O Configuration Address
32	24_48_SEL	24M clock source	48M clock source	vcc	Clock Source Selection
34	LPT_EN	Disable LPT	Enable LPT	vcc	LPT OR OTHERS
62	ASUS_EN	Disable ASUS ASIC	Enable ASUS ASIC	VSB	ASUS GLUE LOGIC
69	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	VSB	DSW OR SVID FUNCTION
71	ANTISURGE_EN	DISABLE ANTISURGE FUNCTION	ENABLE ANTISURGE FUNCTION	VSB	ANTISURGE FUNCTION
96	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	VSB	AMD SEQ OR PVID FUNCTION

ASSET COMPUTE NC Engineer: COrgAddr1>
Size Provide Nate SP-1060 Rev Nt. 61 April 10 April 10

if there is pull-high@CPU side, remove OR31 **New CPU Detect** +3V\_BAT OR60 2MOHM −>>O\_INTRUDER# 48 OR59 MOHM OR477 1MOhm RB1 330Ohm →>>O\_NEW\_CPU 48 WAFER\_HD\_1X2P Chasis OC58 H2N7002 /X 9,21 H\_SKTOCC# >> OC20 0.1UF/16V N/X 0.1UF/16V GREEN GND GND GND ĘND. GND ->> 33M\_CLK1\_C ->> 33M\_CLK2\_C ->> 33M\_CLK3\_C DC\_OUT1 WC40 WC41 WC42 WC43 SPF/50V SPF/50V SPF/50V SPF/50V WC44 5PF/50V POWER\_CON\_6P GND

WR40

WC45 \_\_22UF/6.3V

WU2 REF CLK2 CLK1 GND

21 CK\_24M\_PCH >>-

CLKOUT CLK4 VDD CLK3

ICS9112AM\_16LFT

## **POWER LED**









