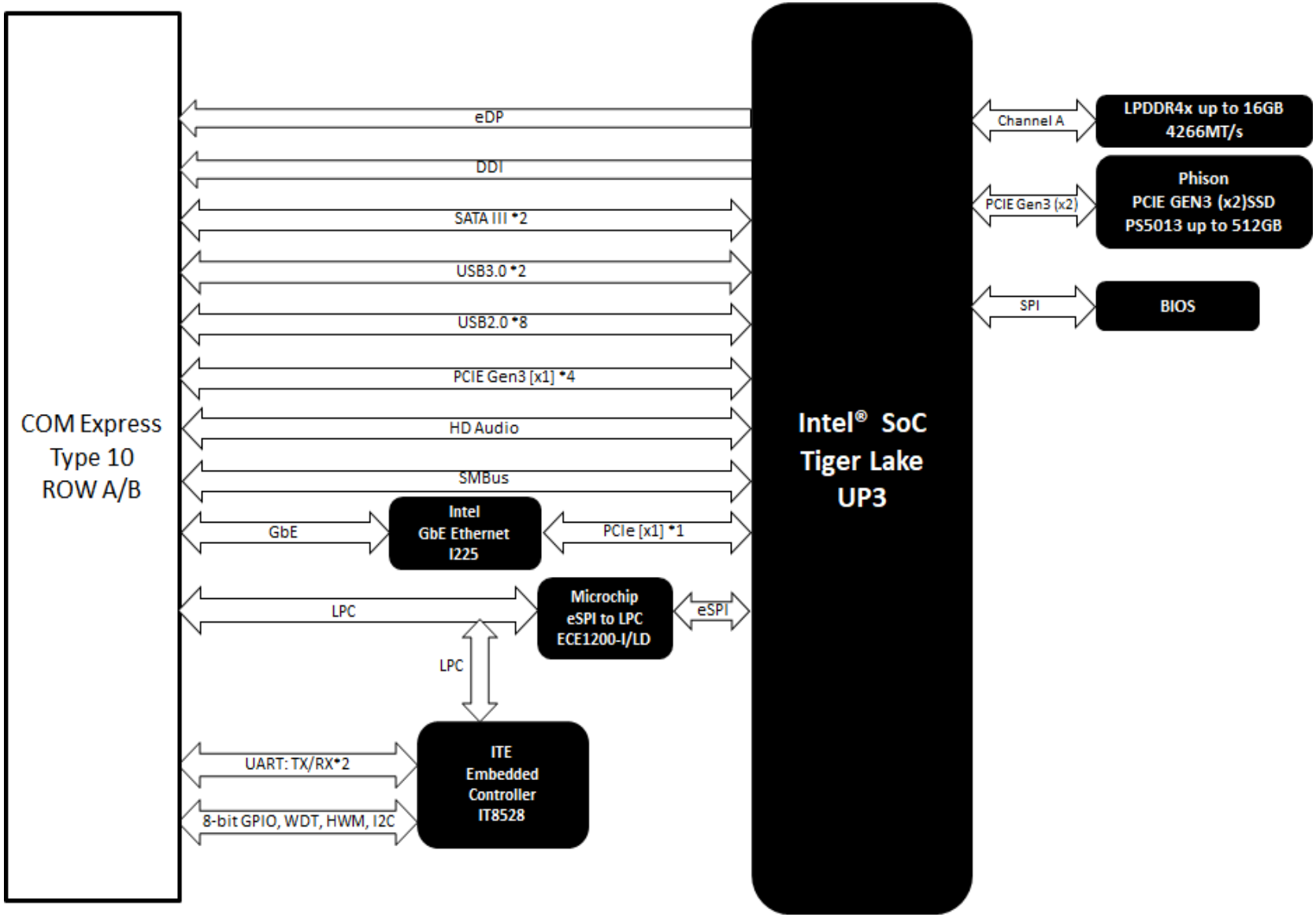
Project Name: NANOCOM-TGU
Project Number:E210103
Version: A0.2_0_0



A0.2

AAEON Technology INC.

Title: Cover Sheet

Size | Document Number: NANOCOM-TGU | Rev: A0.2_0_0

Date: Thursday, April 15, 2021 | Sheet 1 of 34

***Nanocom-TGU A01 don't support C10 Deep Sleep mode**

SMBus/I2C Addresses :

Device	address
I219	0XC8
PTN3460BSIFHI	0C4h

PCB Footprints

MOSFET BJT

Board ID

ID0	ID1	Description
0	0	Total 16GB support 4266 MPN:Micron MT53E2G32D4DT-046 WT:A
0	1	Total 8GB support 3733 MPN:Micron MT53D1024M32D4DT-053 WT:D
1	0	N/A
1	1	N/A

PCB STACK :

Board: FR4
Impedence: 40ohm, 50ohm, 75ohm, 80ohm, 85ohm, 100ohm +/-10%
Thickness: 2.0mm +-10%

- Layer 1 : Component (Top)
- Layer 2 : GND (GND1)
- Layer 3 : Signal (IN1)
- Layer 4 : GND (GND2)
- Layer 5 : Signal (IN2)
- Layer 6 : GND (GND3)
- Layer 7 : Signal (IN3)
- Layer 8 : POWER (VCC)
- Layer 9 : POWER (VCC)
- Layer 10 : Signal (IN4)
- Layer 11 : GND (GND4)
- Layer 12 : Signal (IN5)
- Layer 13 : GND (GND5)
- Layer 14 : Signal (IN6)
- Layer 15 : GND (GND6)
- Layer 16 : Solder (Bottom)

SOC GPIO table　　*實際以線路圖為主

Name	Power Rail	Default	GPIO Function	Location
GPP_E14/DDSP_HPDA/DISP_MISCA	+V3P3S	PD	EDP_HPD	DR5
GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD	Refer to intel setting		DDI1_CTRL_CLK	DU8
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD			DDI1_CTRL_DATA	DV8
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD	+V3P3A	PU	HW strap TBT LSX #1 PINS VCCIO CONFIGURATION	DD6
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK	+V3P3A	PU	HW strap TBT LSX #2 PINS VCCIO CONFIGURATION	DM23
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI	+V3P3A	PU	HW strap TBT LSX #3 PINS VCCIO CONFIGURATION	DN21
GPP_A19/DDSP_HPD1/DISP_MIS	+V3P3S	PD	DDI1_HPD	DF45
GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	+V3P3A	PU	USB2_OC1#	DH52
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK	+V3P3A	PU	USB2_OC2#	DK45
GPP_E8/SATA_LED#	+V3P3S	PD	SATALED#	DV11
GPP_E6/THC0_SPI1_RST#	+V3P3A	PU	HW STRAP JTAG ODT Disable	DT8
GPP_C0/SMBCLK	+V3P3A	PU	SMB_CLK	DK21
GPP_C1/SMBDATA	+V3P3A	PU	SMB_DATA	DM19
GPP_C2/SMBALERT#	+V3P3A	PU	SMBALERT#	DN19
GPP_C3/SML0CLK	+V3P3A	PU	LAN_SM_CLK	DK19
GPP_C4/SML0DATA	+V3P3A	PU	LAN_SM_DATA	DM17
GPP_C5/SML0ALERT#	+V3P3A	PU	SML0ALERT#	DN17
GPP_C6/SML1CLK	+V3P3A	PU	EC_SMCLK0	DK17
GPP_C7/SML1DATA	+V3P3A	PU	EC_SMDAT0	DJ17
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#	+V3P3A	PU	SML1ALERT#	CY50
GPP_E7/CPU_GP1	+V3P3A	PU	SMI#	DF8
GPP_E3/CPU_GP0	+V3P3A	PU	SCI#	DU5
GPP_B18/GSPI0_MOSI	CPU internal	PD	HW strap No Reboot	DA51
GPP_C14/UART1_RTS#/ISH_UART1_RTS#	+V3P3A	PU	TPM_PIRQ# (From TPM interrupt)	DU19
GPP_D16/ISH_UART0_CTS# DV25	without external resister	PD	CPU_SSD_PWREN (Reserved for eanbling PCIe SSD)	DV25
GPP_T3	+V3P3A	PD	BOARD_ID0	DN33
GPP_T2	+V3P3A	PD	BOARD_ID1	DT35
GPP_U5	+V3P3A	PD	BOARD_ID2	DG17
GPP_E9/USB_OC0#	+V3P3A	PU	USB2_OC0#	DD8
GPP_A16/USB_OC3#/I2S4_SFRM	+V3P3A	PU	USB2_OC3#	DJ45
GPP_D5/SRCCLKREQ0#	+V3P3S	PD	PCIE_CLKREQ#0	DW30
GPP_D8/SRCCLKREQ3#	+V3P3S	PD	PCIE_CLKREQ#3	DT24
GPP_H10/SRCCLKREQ4#	+V3P3S	PD	PCIE_CLKREQ#4	DG25
GPD8/SUSCLK	Refer to intel setting		SUSCLK	DW41
GPP_F2/CNV_RGI_DT/UART0_TXD	+V3P3A	PU	HW strap M.2 CNVi Mode Select	DG13
GPP_F0/CNV_BRI_DT/UART0_RTS#	CPU internal	PD	HW strap XTAL SEL1	DF17
GPP_H3/SX_EXIT_HOLDOFF#	+V3P3A	PU	SX_EXIT_HOLDOFF#	DG31
GPD2/LAN_WAKE#	+V3P3A	PU	LAN_WAKE#	DM41
GPD11/LANPHYPC/DSWLDO_MON	+V3P3A	PU	PM_LAN1PHY_ENABLE	DT41
CFG_14	VCCIO_OUT	PU	HW strap PEG* Static x4 Lane Numbering Reversal	V17
CFG_4	VCCIO_OUT	PD	HW strap eDP Presence	E6
CFG_7	CPU internal	PU	HW strap PEG Training	H7

EC Table For Nanocom-TGU A02

GPIO Group	IT8528 (LPC)	ECD's Definition	Platform Type 10 (IT8528)	Note
N/A	WRST#	WRST#	WRST#	
LPC				
GPM0	LAD0	LPC	LAD0	
GPM1	LAD1	LPC	LAD1	
GPM2	LAD2	LPC	LAD2	
GPM3	LAD3	LPC	LAD3	
GPM4	LPCCLK	LPC	LPCCLK	
GPM5	LFRAME#	LPC	LFRAME#	
GPM6	SERIRQ	LPC	SERIRQ	
N/A	FSCK	EC FW SPI	EC FW SPI	
N/A	FSCE#	EC FW SPI	EC FW SPI	
N/A	FMOSI	EC FW SPI	EC FW SPI	
N/A	FMISO	EC FW SPI	EC FW SPI	
GPH0	CLKRUN#/IDO	LPC		LPC用不到，但未來eSPI會用到 >> EVB_RESET ??
GPD2	LPCRST#	LPC	LPCRST#	
Debug use				
GPJ6	CK32K_X1	TP debug message.	COM留option clock 空間以避免產品將SMBus 20K公接至	
GPJ7	CK32KE_X2	TP debug message.		
Power Sequence Management				
N/A	KSI0	I_B4_RSMRST		If no uses, it needs an external PU to +VSALW_EC
N/A	KSI1	I_RSMRST	I_RSMRST	If it is no use in your project which must be pulled up.
N/A	KSI2	I_SLP_S5	I_SLP_S5	Suggestion
N/A	KSI3	I_SLP_S4	I_SLP_S4	Must
N/A	KSI4	I_SPI_S3	I_SPI_S3	Must
N/A	KSI5	I_PWRGD_CB	I_PWRGD_CB	If it is no use in your project which must be pulled up.
N/A	KSI6	I_ASYS_PWRGD	I_ASYS_PWRGD	
N/A	KSI7	I_Auto_PWRBTN	I_Auto_PWRBTN	
GPE4	PWRSW	I_PowerBTN	I_PowerBTN	
GPJ1	HDIO3	O_ERP_ON#	O_ERP_ON#	當作3.3VA_EN用 It should be pulled by EC internally.
GPB2	CTX0	O_B4_RSMRST		
GPB7	RING#/CK32KOUT/LPCRST#	O_RSMRST	O_RSMRST	It should be pulled by EC internally.
N/A	KSO12	O_SLP_S3	O_SLP_S3	
N/A	KSO13	O_SLP_S4	O_SLP_S4	
N/A	KSO14	O_SLP_S5	O_SLP_S5	
N/A	KSO15	O_SYS_PWROK	O_SYS_PWROK	
GPE6	LPCPD#	O_PWR_BTN#	O_PWR_BTN#	
GPE7	L80LLAT	O_PS_ON#	O_PS_ON#	由EC控制，做一個12V PMOS當開關注意電流大小
GPB5	GA20	O_WDT	O_SYSRST#	
GPB6	KBRST#	O_WDT#	O_WDT#	COMe必須做反向
Embedded Controller Interface				
GPD3	ECSCI#	SCI	SCI#	SCI
GPD4	ECSMI#	SMI	SMI#	SMI
I2C , SMBUS functions				
GPB3	SMCLK0	I2C Slave	SMCLK0	
GPB4	SMDAT0	I2C Slave	SMDAT0	
GPC1	SMCLK1	I2C Master	I2C_CLK	
GPC2	SMDAT1	I2C Master	I2C_DAT	
GPC7	PWUREQ#	SMCLK2		
GPF7	SMDAT2	SMDAT2		
DIO funciton				
GPE0	L80HLAT	DIO 0	GPI 0	
GPE1	EGAD	DIO 1	GPI 1	
GPE2	EGCS#	DIO 2	GPI 2	
GPE3	EGCLK	DIO 3	GPI 3	
GPH3	HSCE#/ID3	DIO 4	GPO 0	
GPH4	HSCK/ID4	DIO 5	GPO 1	
GPH5	HMISO/ID5	DIO 6	GPO 2	
GPH6	HMOSI/ID6	DIO 7	GPO 3	
GPH7		GPIO		

EC Table For Nanocom-TGU A02

GPIO Group	IT8528 (LPC)	ECD's Definition	Platform Type 10 (IT8528)	Note
SMART FAN Function				
GPA0	PWM0	FAN1 PWM	FAN1 PWM	
GPA1	PWM1	FAN2 PWM		
GPA2	PWM2	FAN3 PWM		
GPD6	TACH0A	FAN_TACH 1	FAN_TACH 1	
GPD7	TACH1A	FAN_TACH 2		
GPJ0	HDIO2/TACH2	FAN_TACH 3		
COM#1 function				
GPB0	SIN0/RXD	UART1 - 4 wire	SRXD1	這八隻腳可以組成1x RS-232
GPB1	SOUT0/TXD	UART1 - 4 wire	STXD1	
GPD5	GINT/CTS0#	UART1 - 4 wire		
GPF3	PS2DAT1/RTS0#	UART1 - 4 wire		
GPF2	PS2CLK1/DTR0#	UART1 - Full / GPIO		
GPG6	FDIO3/DSR0#	UART1 - Full / GPIO		HW Strap
GPJ4	DAC4/DCD0#	UART1 - Full / GPIO		
GPJ5	DAC5/RIG0#	UART1 - Full / GPIO		
COM#2 function				
GPH1	SIN1/CRX1/ID1	UART2 - 2 wire	SRXD2	此組預留給SBC或有需求的模組
GPH2	SOUT1/CTX1/ID2	UART2 - 2 wire	STXD2	
GPJ7	ADC7/CTS1#	ADC GFX		Conflict wit ADC
GPG1	SBUSY/FDIO2/DTR1#/ID7			
GPA7	PWM7/RIG1#	UART2 - Full / GPIO		
GPE5	RTS1#	UART2 - Full / GPIO		
GPJ5	ADC5/DCD1#	ADC		Conflict wit ADC
GPJ6	ADC6/DSR1#	ADC		Conflict wit ADC
Second SPI function				
GPA6	PWM6/SSCK	SSPI		For SPI Devices
GPC3	KSO16/SMOSI	SSPI		
GPC5	KSO17/SMISO	SSPI		
GPG0	SSCE1	HW Strap / SSPI		
GPG2	SSCE0#	HW Strap SPI		
Hardware Monitor				
GPF6	SMCLK2/PECI	PECI	PECI	
GPI0	ADC0	T1 Tolerant 3V	T1	
GPI1	ADC1	T2 Tolerant 3V	T2	
GPI2	ADC2	T3 Tolerant 3V		
GPI3	ADC3	ADC 5V	ADC 5V	
GPI4	ADC4	ADC 12V	ADC 12V	
GPI5	ADC5/DCD1#	ADC MEM ?		
GPI6	ADC6/DSR1#	ADC CPU ?	ADC MEM	Follow COM-TGUC6; Otherwise, it should connect to pin F10.
GPI7	ADC7/CTS1#	ADC GFX ?		
Wake function				
GPD0	RI1#	WAKE1#	WAKE1#	
GPD1	RI2#	WAKE2#		
IR RX function				
GPC0	CRX0	OEM IRX		
PWM Controller				
GPA4	PWM4	PWM1		
GPA5	PWM5	PWM2		
Backlight brightness controller function				
GPA3	PWM3	Brightness		For LVDS only
N/A	KSO10	I_BLK_EN		eDP or LVDS
N/A	KSO11	O_BLK_EN		eDP or LVDS
Timer Interrupt fucntion				
GPC4	TMRI0	TMRI0		
GPC6	TMRI1	TMRI1		
DAC Controller				
GPJ2	DAC2/TACH0B	Revserved		
GPJ3	DAC3/TACH1B	Revserved		
Flexible GPIO				
GPF0	PS2CLK0	CEC		
GPF1	PS2DAT0	Revserved		
GPF4	PS2CLK2	BIOS_SEL0#(GPO)	BIOS_SEL0#(GPO)	BIOS_SEL0#: 選擇 BIOS boot from Module or C/B
GPF5	PS2DAT2	BIOS_SEL1#(GPO)	BIOS_SEL1#(GPO)	BIOS_SEL1#: 選擇 LPC or eSPI interface operation
N/A	KSO0	Revserved		
N/A	KSO1	SLEEP#	SLEEP#	
N/A	KSO2	LID#	LID#	
N/A	KSO3	BIOS_DIS1#(GPI)	BIOS_DIS1#(GPI)	Follow COM-TGUC6; Otherwise, it should connect to pin K8.
N/A	KSO4	BIOS_DIS0#(GPI)	BIOS_DIS0#(GPI)	Follow COM-TGUC6; Otherwise, it should connect to pin M9.
N/A	KSO5	eSPI_EN#(GPI)	eSPI_EN#(GPI)	
N/A	KSO6	BRD_ID1(GPI)	BOARD_ID1	
N/A	KSO7	BRD_ID2(GPI)	BOARD_ID2	
N/A	KSO8	I_BATLOW#	I_BATLOW#	
N/A	KSO9	O_BATLOW#	O_BATLOW#	The EC will bypass this signal if there are no special requirements.

A0.2

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AAEON Technology INC.

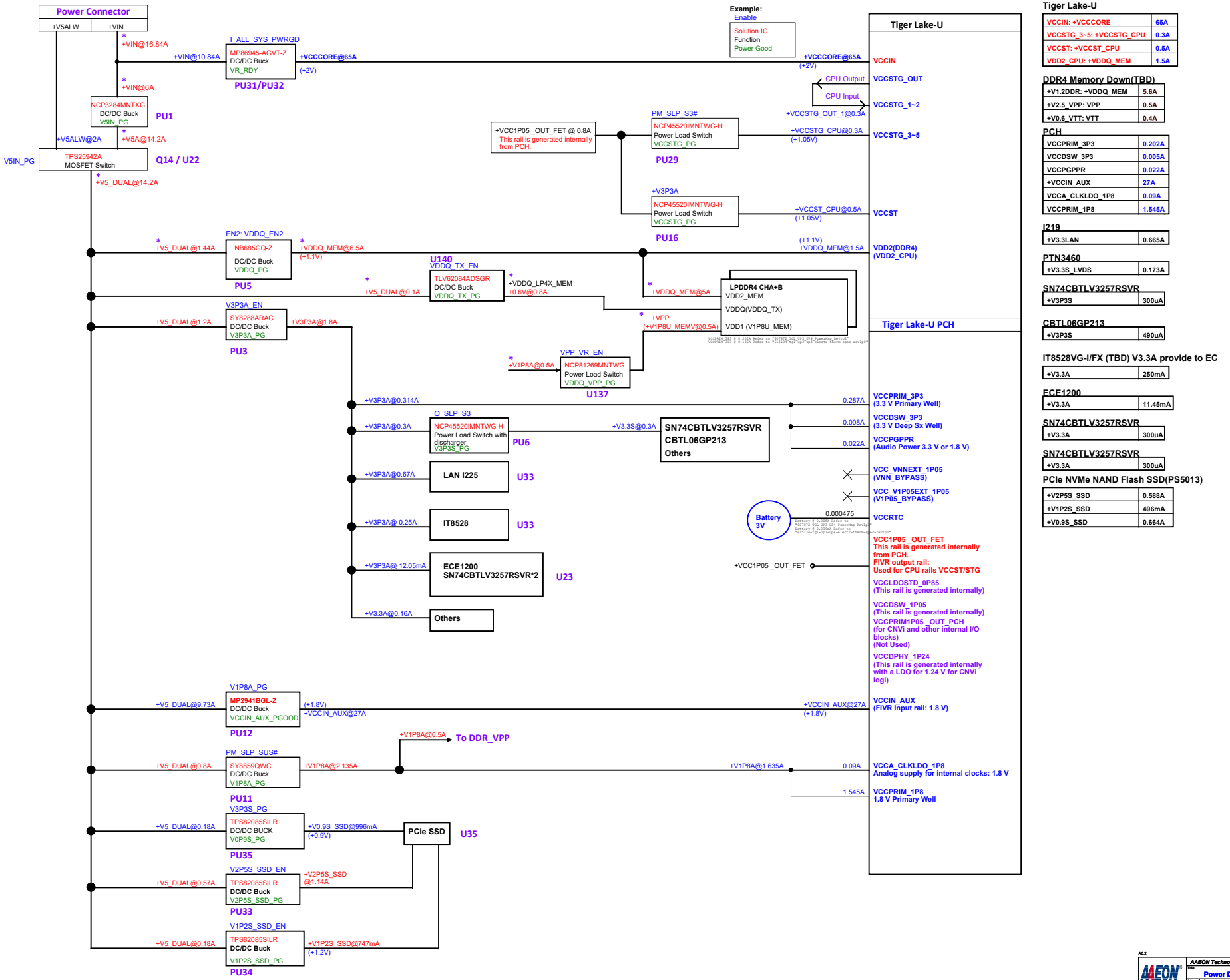
Title: System Setting

Size: Document Number: NANOCOM-TGU　Rev: A0.2_0_0

Date: Wednesday, April 21, 2021　Sheet 2 of 34

*Dinken suggested that the eff. is equal to 1 to calculate each source current of buck.

Power Delivery



Tiger Lake-U

VCCIN: +VCCCORE	65A
VCCSTG_3~5: +VCCSTG_CPU	0.3A
VCCST: +VCCST_CPU	0.5A
VDD2_CPU: +VDDQ_MEM	1.5A

DDR4 Memory Down(TBD)

+V1.2DDR: +VDDQ_MEM	5.6A
+V2.5_VPP: VPP	0.5A
+V0.6_VTT: VTT	0.4A

PCH

VCCPRIM_3P3	0.202A
VCCDSW_3P3	0.005A
VCCPGPPR	0.022A
+VCCIN_AUX	27A
VCCA_CLKLDO_1P8	0.09A
VCCPRIM_1P8	1.545A

I219

+V3.3LAN	0.665A

PTN3460

+V3.3S_LVDS	0.173A

SN74CBTLV3257RSVR

+V3P3S	300uA

CBTL06GP213

+V3P3S	490uA

IT8528VG-I/FX (TBD) V3.3A provide to EC

+V3.3A	250mA

ECE1200

+V3.3A	11.45mA

SN74CBTLV3257RSVR

+V3.3A	300uA

SN74CBTLV3257RSVR

+V3.3A	300uA

PCIe NVMe NAND Flash SSD(PS5013)

+V2P5S_SSD	0.588A
+V1P2S_SSD	496mA
+V0.9S_SSD	0.664A

A0.2

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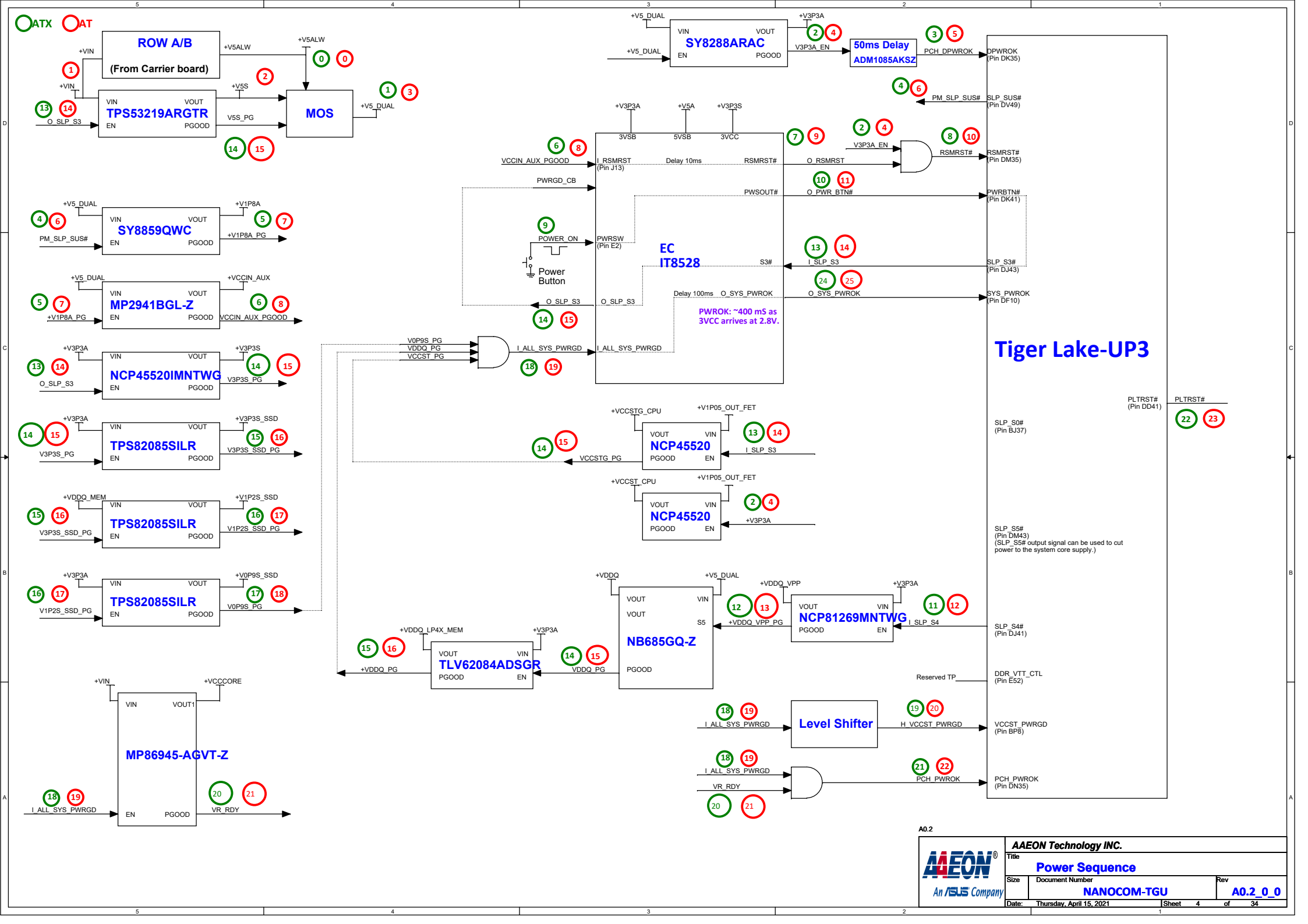
Title: Power Delivery

Size | Document Number: NANOCOM-TGU | Rev: A0.2_0_0

Date: Thursday, April 15, 2021 | Sheet 3 of 34



A0.2

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Title	Power Sequence	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 15, 2021	Sheet 4 of 34	

GPP_D10	TBT LSX #2 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

The internal pull-down 20k is disabled after RSMRST# de-asserts.

+V3P3A — R2 R0402 4.7K 1% — GPP_D10

20200724 Remove reserved Pull low

0 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V
1 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 3.3V

GPP_D12	TBT LSX #3 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

The internal pull-down 20k is disabled after RSMRST# de-asserts.

+V3P3A — R10 R0402 4.7K 1% — GPP_D12

20200724 Remove reserved Pull low

0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 3.3

TBT_LSX0_RXD	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R16 R0402 4.7K 1% — DDI1_CTRL_DATA

20200724 Remove reserved Pull low

+V3P3S — R19 R0402 2.2K 1% — DDI1_CTRL_CLK
R20 R0402 Do Not Stuff 1% — DDI1_CTRL_DATA

TBT_LSX1_RXD	TBT LSX #1 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

This strap has a 20 kohm ± 30% internal pull-down

+V3P3A — R23 R0402 4.7K 1% — GPP_E21

20200724 Remove reserved Pull low

Table 41. TCP Port Signal Mapping For DisplayPort*

Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3
Note: Apply to TCP ports only.		

CPU1A — 1 OF 21

eDP1

(17) EDP_LANE3_DP — AC2 DDIA_TXP_3
(17) EDP_LANE3_DN — AC1 DDIA_TXN_3
(17) EDP_LANE2_DP — AD2 DDIA_TXP_2
(17) EDP_LANE2_DN — AD1 DDIA_TXN_2
(17) EDP_LANE1_DP — AF1 DDIA_TXP_1
(17) EDP_LANE1_DN — AF2 DDIA_TXN_1
(17) EDP_LANE0_DP — AG2 DDIA_TXP_0
(17) EDP_LANE0_DN — AG1 DDIA_TXN_0
(17) EDP_AUXP — AJ2 DDIA_AUX_P
(17) EDP_AUXN — AJ1 DDIA_AUX_N
DN4 GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD — Undriven PD 15-40 kOhm
DT6 GPP_E23/DDPA_CTRLDATA
(17) EDP_HPD — EDP_HPD — DR5 GPP_E14/DDSP_HPDA/DISP_MISCA — Undriven
R7 100K 5% R0201

DDIB_TXP_3 T12
DDIB_TXN_3 T11
DDIB_TXP_2 Y1
DDIB_TXN_2 Y2
DDIB_TXP_1 P2
DDIB_TXN_1 P1
DDIB_TXP_0 V1
DDIB_TXN_0 V2
DDIB_AUX_P AB3
DDIB_AUX_N AB2
DM28 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN — Undriven PD 15-40 kOhm
DK27 GPP_H17/DDPB_CTRLDATA
DDIB_HPD — DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD — Undriven
R13 100K 5% R0201
TP71 TP20 — EDP2_BKLT_EN — DG47 GPP_A21/DDPC_CTRLCLK/I2S5_TXD — Driven Low PD 20 kOhm
TP72 TP20 — EDP2_BKLT_CTRL — DJ47 GPP_A22/DDPC_CTRLDATA/I2S5_RXD
DDI1
DDI1_CTRL_CLK — DU8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD — Undriven PD 20 kOhm
DDI1_CTRL_DATA — DV8 GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD
GPP_E21 — DF6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD — Undriven PD 20 kOhm
DD6 GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD
GPP_D10 — DN23 GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0# — Undriven PD 20 kOhm
DM25 GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK
GPP_D12 — DN27 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO — PD 20 kOhm PD 20 kOhm
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI
A02, 20210312 Saving PCB space Remove TP1 (DK23).
TP73 TP20 — EDP2_PWR_EN — DF43 GPP_A17/DISP_MISCC/I2S4_TXD — Driven Low PD 20 kOhm
DDI1_HPD — DF45 GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK — PD 20 kOhm
GPP_A20 — DF47 GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM — PD 20 kOhm
(17) USB2_OC1# — DH52 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1 — PD 20 kOhm
(17) USB2_OC2# — DK45 GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK — PD 20 kOhm

eDP1
(17) EDP_VDD_EN — DM8 EDP_VDDEN — Driven Low
(17) EDP_BKLT_EN — DN8 EDP_BKLTEN — Driven Low
(17) EDP_BKLT_CTRL — DG10 EDP_BKLTCTL — Driven Low
DESIGN NOTE: VDDEN 100K PD PER PDG BKLTEN 100K PD PER PDG
R8538 100K 5% R0201
R8539 100K 5% R0201

<TOLERANCE>

CB_DDI1

TCP0_TXRX_P1 AY2 — DDI1_LANE3_DP (17)
TCP0_TXRX_N1 AY1 — DDI1_LANE3_DN (17)
TCP0_TXRX_P0 BB1 — DDI1_LANE1_DP (17)
TCP0_TXRX_N0 BB2 — DDI1_LANE1_DN (17)
TCP0_TX_P1 AM5 — DDI1_LANE2_DP (17)
TCP0_TX_N1 AM7 — DDI1_LANE2_DN (17)
TCP0_TX_P0 AT7 — DDI1_LANE0_DP (17)
TCP0_TX_N0 AT5 — DDI1_LANE0_DN (17)
TCP0_AUX_P AP7 — DDI1_AUX_C_DP
TCP0_AUX_N AP5 — DDI1_AUX_C_DN
TCP0_AUX

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5
TCP1_AUX

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE1
TCP2_TXRX_N0 BE2
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7
TCP2_AUX

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7
TCP3_AUX

TC_RCOMP_P AN2 — TCRCOMP_DP — R15 150 1% R0402 — TCRCOMP_DN
TC_RCOMP_N AN1
TC_RCOMP
DSI_DE_TE_2 M8 — TP2 TP20
DDI_RCOMP AB1 — EDP_RCOMP
DISP_UTILS/DSI_DE_TE_1 CE4 — DSI_DE_TE_1 — TP3 TP20 — R18 150 1% R0402

DDI1 / AUX Switch

+V3P3S — C1 0.1uF 6.3V C0201 — DDI1_DDC_AUX_SEL
U1 ,C2 ,C3 close to CN RAW AB CON
DDI1_AUX_C_DP — C2 C0201 0.1uF 6.3V — DDI1_AUX_DP_C
DDI1_DDC_AUX_SEL
DDI1_AUX_C_DN — C3 C0201 0.1uF 6.3V — DDI1_AUX_DN_C
DDI1_AUX_DN
U1 14-T_C_L-74CBTLV3125BQ-0
DDI1_DDC_SEL
DDI1_CTRL_DATA
DDI1_AUX_DN
DDI1_DDC_SEL
DDI1_CTRL_CLK
(17) DDI1_AUX_DP — DDI1_AUX_DP — R6 100K 1% R0402
DDI1_DDC_AUX_SEL:
H: DDC (HDMI/DVI)
L: AUX (DP/eDP)

+V3P3S — R1 100K 1% R0402 — DDI1_AUX_DN (17)

(17) DDI1_DDC_AUX_SEL — DDI1_DDC_AUX_SEL
+V3P3S — R8 10K 1% R0201 — DDI1_DDC_SEL
R9 Do Not Stuff 1% R0201
Q1A EM6K7GT2R
R12 1M 5% R0201

+V3P3S — R14 100K 5% R0201 — CB_DDI1_HPD (17)
DDI1_HPD — Q1B EM6K7GT2R

Disable DDI2/3/4
GPP_A20 — R2900 100K 5% R0201

5.3.5 Digital Display Interface Termination Guidelines
Disabling and Termination Guidelines — From 607872_TGL_UP3_UP4_PHDoc_Rev1p2
Table 53. Disabling and Termination Guidelines

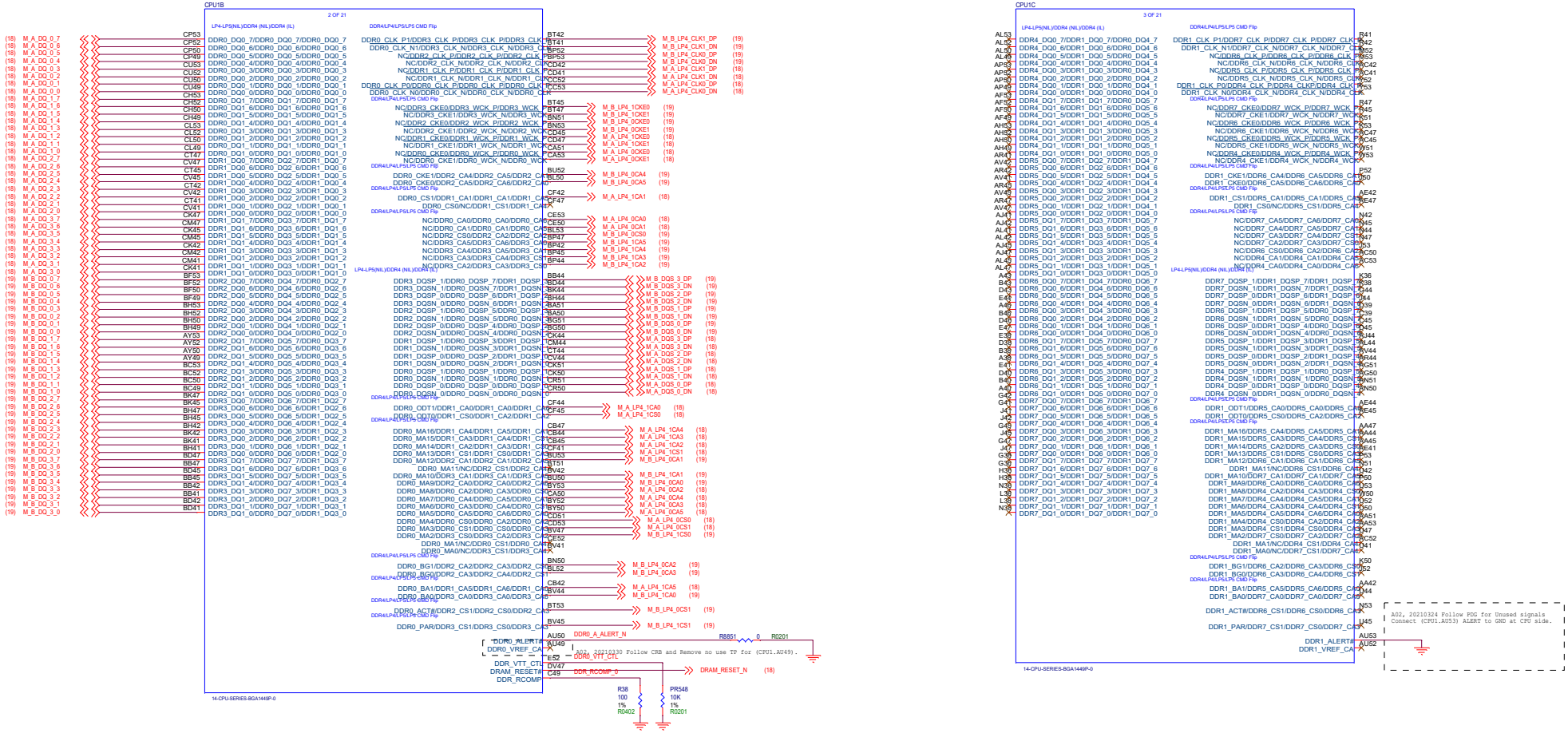
Pin name	Recommendation
DDIx_TXN/P[3:0]	No connect
DDIx_AUXN/P	No connect
DDIx_HPD	Pull down to ground via 100k Ω resistor
DDIA_RCOMP	Pull Down to VSS via 150 Ohm resistor.
DISP_UTIL	No connect

Add OC1#/OC2# cuz DDI3/4 no used
USB2_OC1# — R126 10K 1% R0201 — +V3P3A
USB2_OC2# — R28 10K 1% R0201 — +V3P3A

A0.2

AAEON Technology INC.
Title: SoC DDI
Size: — Document Number: NANOCOM-TGU — Rev: A0.2_0_0
Date: Thursday, April 22, 2021 — Sheet 5 of 34

SoC LPDDR4x x32



A0.2

AAEON Technology INC.		
Title: SoC LPDDR4x		
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 15, 2021	Sheet 6 of 34	

SPI0_MOSI	Reserved
	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on- board device driving it to opposite direction during strap sampling.

External pull-up is required. Recommend 4.7 kohm pull up

+V3P3A — R45 R0402 4.7K 1% — SPI0_PCH_SI

SPI0_IO2	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+V3P3A — R57 R0201 100K 5% — SPI0_PCH_WP#

External pull-up is required.

SPI0_IO3	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+V3P3A — R66 R0402 100K 1% — SPI0_PCH_HOLD#

External pull-up is required.

GPP_E6	JTAG ODT Disable
0	JTAG ODT is disabled
1 *	JTAG ODT is enabled

This strap does not have an internal pull-up or pull-down.
External pull-up is recommended

+V3P3A — R72 R0402 100K 1% — GPP_E6

CRB (Q)
609003_TGL_UP3_DDR4_SODIMM
_RVP_SCH_REV1P0
PU 100K ohm to V1.8A

20200724 Remove reserved +V1P8A Pull High & low

DBG_PMODE	Reserved
	This strap should sample high. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-up.

R82 R0402 Do Not Stuff 1% DBG_PMODE — May change 0201

GPP_H0	BFX STRAP 1- BIT 2

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R91 R0402 Do Not Stuff 1% GPP_H0 — Remove Reserve PD

GPP_H1	BFX STRAP 2- BIT 3

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R96 R0402 Do Not Stuff 1% GPP_H1 — Remove Reserve PD

GPP_H2	BFX STRAP 3- BIT 4

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R103 R0402 Do Not Stuff 1% GPP_H2 — Remove Reserve PD

PCH

SPI0_PCH_CLK — R2917 R0402 62 5% — SPI0_CLK
SPI0_PCH_SI — R8507 R0402 62 5% — SPI0_SI
SPI0_PCH_SO — R8508 R0402 62 5% — SPI0_SO
SPI0_PCH_CS0# — R8509 R0402 0 5% — SPI0_CS0#

SPI Level shifter

A02, 20210226
Due to SW EE unable supporting sharing SPI Flash design,
modify that EC and BIOS connect their own SPI Flash.
Remove R2921and R8499-R8501.
Change R2917, R8507, R8508, R8536,R8537 from 0 to 62 ohm ±5% based on
607872_TGL_UP3_PDG_Rev2p2.

SoC SPI/LPC/SMBus

SPI0_PCH_CLK — R43 100K 5% R0201

(21) SPI0_DQ3_HOLD# — R8536 62 — R0402 62 5%
(21) SPI0_DQ2_WP# — R8537 62 — R0402 62 5%

SPI0_PCH_HOLD#
SPI0_PCH_WP#
SPI0_PCH_SO
SPI0_PCH_SI
SPI0_PCH_CS0#

A02, 20210226 Due to adding intel I225
Remove TPM ciruit for PM requirement (Add I225).
Remove SPI0_TPM_CS2# (DF39).

+V3P3S — R59 R0201 10K 1% — SATALED# — (17) SATALED#

GPP_E6

A02, 20210312 Saving PCB space
Remove TP4 (DK13).

CPU1E — 5 OF 21

DJ37	SPI0_CLK	PD 20K ohm	
DG35	SPI0_IO3	PD 20K ohm	
DJ39	SPI0_IO2	PD 20K ohm	
DJ35	SPI0_MISO	PD 20K ohm	
DF35	SPI0_MOSI		
DG37	SPI0_CS1#	PD 20K ohm	
DF39	SPI0_CS2#		
DJ5	GPP_E11/THC0_SPI1_CLK	Undriven	
DN5	GPP_E2/THC0_SPI1_IO3	I/O	
DM7	GPP_E1/THC0_SPI1_IO2	I/O	
DK6	GPP_E12/THC0_SPI1_IO1	I/O	
DK3	GPP_E13/THC0_SPI1_IO0	Undriven	
DK1	GPP_E10/THC0_SPI1_CS#	Undriven	
DM3	GPP_E8/SATA_LED#	Undriven	
DM1	GPP_E17/THC0_SPI1_INT#	Undriven	
DT8	GPP_E6/THC0_SPI1_RST#	Undriven	
DN15			
DK13	GPP_F11/THC1_SPI2_CLK	Undriven	
DM13	GPP_F15/GSXSRESET#/THC1_SPI2_IO3		
DN13	GPP_F14/GSXDIN/THC1_SPI2_IO2		
DJ13	GPP_F13/GSXSLOAD/THC1_SPI2_IO1		
DK15	GPP_F12/GSXDOUT/THC1_SPI2_IO0	Undriven	
DN19	GPP_F16/GSXCLK/THC1_SPI2_CS#	Undriven	
DV13	GPP_F18/THC1_SPI2_INT#	Undriven	
	GPP_F17/THC1_SPI2_RST#		
DH3		PU 31.25/PD 100 ohm	
DH5	CL_CLK	PU 31.25/PD 100 ohm	
DH2	CL_DATA	Drive High/Low	
	CL_RST#		

14-CPU-SERIES-BGA1449P-0

Note: SUSPWRDNACK is not available as hard signals when eSPI, SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered

Carrier board

GPP_C0/SMBCLK — DK21 SMB_CLK
GPP_C1/SMBDATA — DM19 SMB_DATA
GPP_C2/SMBALERT# — DN19 SMBALERT# — SMBALERT# (17)

I225

GPP_C3/SML0CLK — DK19 LAN_SM_CLK — LAN_SM_CLK (23)
GPP_C4/SML0DATA — DM17 LAN_SM_DATA — LAN_SM_DATA (23)
GPP_C5/SML0ALERT# — DN17 SML0ALERT#

EC

GPP_C6/SML1CLK — DJ17 EC_SMCLK0 — EC_SMCLK0 (20)
GPP_C7/SML1DATA — CY50 SML1ALERT# — EC_SMDAT0 (20)
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# — DK17 EC_SMCLK0

GPP_A5/ESPI_CLK — DN53 ESPI_CLK — R60 49.9 1% R0402 — BDG_ESPI_CLK (25)
GPP_A3/ESPI_IO3/SUSACK# — DJ53 ESPI_IO_3 — R61 15 5% R0402 — BDG_ESPI_IO_3 (25)
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK — DH50 ESPI_IO_2 — R62 15 5% R0402 — BDG_ESPI_IO_2 (25)
GPP_A1/ESPI_IO1 — DF50 ESPI_IO_1 — R63 15 5% R0402 — BDG_ESPI_IO_1 (25)
GPP_A0/ESPI_IO0 — DF52 ESPI_IO_0 — R64 15 5% R0402 — BDG_ESPI_IO_0 (25)
GPP_A4/ESPI_CS# — DL52 ESPI_CS# — R65 0 5% R0402 — BDG_ESPI_CS# (25)
GPP_A6/ESPI_RESET# — DL50 ESPI_RESET# — R67 Do Not Stuff 1% R0402 — CRB 609003_TGL_UP3_DDR4 SODIMM_RVP_SCH_REV1P0 75K unmount
R70 0 5% R0402 May change 0201 — BDG_ESPI_RST# — BDG_ESPI_RST# (25)
R71 75K 1% R0402

XDP

(20) PECI_EC — R73 43 5% R0402 — PECI_EC

+V1P05_VCCSTG_LGC — R78 1K 1% R0402

(29) H_PROCHOT# — R79 499 1% R0402 — H_PROCHOT#

+VCCST_CPU — R521 1K 1% R0402

+VCCST_CPU — R80 1K 1% R0402

H_THRMTRIP_# — R81 60.4 1% R0402 — THRMTRIP#
R83 49.9 1% R0402
R85 49.9 1% R0402

CPU1U — 21 OF 21

	CATERR#	M7	
	PECI	BK9	
	PROCHOT#	E2	
	THRMTRIP#	M5	
CT39	PROC_POPIRCOMP		
CB9	PCH_OPIRCOMP		
CW12	TP_1		
CM28	TP_2		
DF4	DBG_PMODE		
DB42	GPP_B4/CPU_GP3		
DB41	GPP_B3/CPU_GP2		
DP8	GPP_E7/CPU_GP1		
DU5	GPP_E3/CPU_GP0		
DF31	EAR_N/EAR_N_TEST_NCTF		
DV32	GPP_H2		
DW32	GPP_H1		
	GPP_H0		
DJ27	GPP_H19/TIME_SYNC0		

(20) SMI# — SMI#
(20) SCI# — SCI#

TP65 TP20 — CPU_KBRST# — DJ27

K4	XDP_CPU_JTAG_TRST#		
B9	XDP_CPU_JTAG_TMS		
D12	XDP_CPU_JTAG_TDO		
A12	XDP_CPU_JTAG_TDI		
B6	XDP_CPU_JTAG_TCLK		
PROC_TCK			
D8	XDP_CPU_JTAG_TCLK		
A9	XDP_CPU_JTAG_TMS		
E12	XDP_CPU_JTAG_TDO		
B12	XDP_CPU_JTAG_TDI		
A7	XDP_CPU_JTAG_TCLK		
H4	XDP_CPU_JTAG_TRST#		
C11	PREQ#	TP20	TP35
D11	PRDY#	TP20	TP36
G1	CPU_EAR		
DT15	GPP_F7	TP20	TP37
DR15	GPP_F9		
DT14	GPP_F10	TP20	TP39

CPU JTAG

PCH JTAG

TP20 TP38 — May Remove TP38

This strap is used in conjunction with Boot Strap 0,1,2,3, (on GPP_C5, GPP_H0, GPP_H1, GPP_H2 respectively).

4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled
0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.

SMBALERT#	TLS confidentiality
0	Disable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 *	Enable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to pupport IntelR AMT with TLS

* Default, Internal Pull-Down 20K

+V3P3A — SMBALERT# R48 R0402 4.7K 1% — May change 0201

GPP_C5/ SML0ALERT#	This is bit 0 (LSB) of a total of 4-bit boot strap configuration encodings
0 *	
1	

* Default, Internal Pull-Down 20K

+V3P3A — SML0ALERT# R58 R0402 150K 1%

GPP_F7	Reserved
	This strap should sample LOW. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

GPP_F10	Reserved
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — GPP_F10 R8520 R0201 Do Not Stuff 5% — Remove Reserve PD

CPU_EAR	Stall CPU reset sequence until de-asserted:
1 *	(Default) Normal Operation; No stall.
0	Stall

+VCCSTG_CPU — CPU_EAR R84 R0201 1K 5%

Refer to PDG REV. 1.2
Remove PD reserve 1k ohm

XDP PU/PD

+V1P05_VCCSTG_LGC

Refer to PDG Rev1.2 & CRB Rev1.0
Change PU R from 100 to 51 ohm.

XDP_CPU_JTAG_TDO — R88 51 5% R0201
XDP_CPU_JTAG_TDI — R89 Do Not Stuff 5% R0201
XDP_CPU_JTAG_TMS — TP34 TP20 — Refer Intel COMe board connect to pin H4 with TP.
XDP_CPU_JTAG_TCLK — R93 51 5% R0201 — Note: PLACE BES CLOSE TO CPU
XDP_CPU_JTAG_TRST# — TP33 TP20 — Refer Intel COMe board connect to pin H4 with TP.
XDP_PCH_JTAG_TCLK — R95 Do Not Stuff 5% R0201

SML1ALERT#	CPUNSSC CLOCK FREQ
0 *	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

* Default, Internal Pull-Down 20k
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

SML1ALERT# — R102 R0402 150K 1% — +V3P3A

20200921
Remove BDG_ESPI_ALT_3P3#
level-shifter due to following CRB
design

SMB level-shift

A02, 20210413 Jeff D. suggestion for SMBus Drving issue
Remove Q5 and change R105 & R108 to 0ohm (0201) for SMB_DATA/SMB_CLK.

SMB_DATA — R105 R0201 0 5% — To COMe connector — SMB_DATA_S (17)

SMB_CLK — R108 R0201 0 5% — To COMe connector — SMB_CLK_S (17)

THRMTRIP# level-shift

+VCCST_CPU — PC541 0.1uF 6.3V C0201
+V3P3A — R98 10K 1% R0201

H_THRMTRIP_# — PU28 — NC A GND VCC Y — SN74AUP1G07DRLR SOT-553.5P.SMD
PCH_THRMTRIP# — PCH_THRMTRIP# (17)

A0.2

AAEON Technology INC.
An ASUS Company

Title	SoC SPI/LPC/SMBus	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 7 of 34	

SoC HDA/Board ID

A02, 20210406
Due to detecting ME version problem and CPU1.DT37 internal low level problem.
Change R115 from pull high 1k ohm to pull down 1k ohm.

Undriven

HDA_SDO	Flash Descriptor Security Override
0 *	Disabled (Default)
1	Enable (Disable ME)(debug ONLY)

* Default, Internal Pull-Down 20K

R115 1K HDA_SDO_R
R0201 5%

SPKR	Top Swap Override
0 *	Disabled
1	Enable

* Default, Internal Pull-Down 20K

+V3P3A
Refer to CRB
TGL_UP3_DDR4_SODIMM_RVP_SCH_REV1P0
Change PU from mounting 150K to X/4.7K.
R117 Do Not Stuff SPKR
R0201 5%

GSPI1_MOSI	No Reboot
0 *	Disable No Reboot mode
1	Enable No Reboot mode(ITP/XDP)

* Default, Internal Pull-Down 20K
SAMPLING- PCH_PWROK

+V3P3A
R118 Do Not Stuff GSPI0_MOSI
R0201 5%

Design Note:ALL GPP_R ARE ON
VCCPGPPR POWER WELL = V3P3A
Note: All HDA R placement close to SOC

CPU1G
7 OF 21

(17) HDA_BCLK — R111 33R0201 HDA_BCLK_R — DR38 GPP_R0/HDA_BCLK/I2S0_SCLK
(17) HDA_SYNC — R112 33R0201 HDA_SYNC_R — DU37 GPP_R1/HDA_SYNC/I2S0_SFRM
(17) HDA_SDO — R109 33R0201 HDA_SDO_R — DT37 GPP_R2/HDA_SDO/I2S0_TXD
(17) HDA_SDI0 — DV37 GPP_R3/HDA_SDI0/I2S0_RXD
(17) HDA_RST# — R113 33R0201 HDA_RST#_R — DV41 GPP_R4/HDA_RST#
DL53 GPP_A7/I2S2_SCLK/DMIC_CLK_A0
DG51 GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
DG50 GPP_A10/I2S2_RXD/DMIC_DATA1
DL49 GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
DL52 GPP_A11/PMC_I2C_SDA/I2S3_SCLK
DH49 GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
R116 200 SNDW_RCOMP — DF33 SNDW_RCOMP
1% R0201
Change size to 0201

Driven Low / PD 20K ohm / PD 20K/5K ohm / PD 5K ohm

DW15 GPP_F8/I2S_MCLK2_INOUT / GPP_D19/I2S_MCLK1
DG41 GPP_A23/I2S1_SCLK
DT38 GPP_R7/I2S1_SFRM
DV38 GPP_R6/I2S1_TXD
DW38 GPP_R5/HDA_SDI1/I2S1_RXD
DN31 GPP_S6/SNDW3_CLK/DMIC_CLK_A0
DM31 GPP_S7/SNDW3_DATA/DMIC_DATA0
DK33 GPP_S4/SNDW2_CLK/DMIC_CLK_A1
DK31 GPP_S5/SNDW2_DATA/DMIC_DATA1
DW35 GPP_S2/SNDW1_CLK/DMIC_CLK_B0
DV35 GPP_S3/SNDW1_DATA/DMIC_CLK_B1
DT32 GPP_S0/SNDW0_CLK
DR35 GPP_S1/SNDW0_DATA

14-CPU-SERIES-BGA1449P-0

CPU1F
6 OF 21

GSPI0_MOSI — DC53 GPP_B16/GSPI0_CLK
DA51 GPP_B18/GSPI0_MOSI
DC49 GPP_B17/GSPI0_MISO
(17) SPKR — SPKR — DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
DC52 GPP_B15/GSPI0_CS0#
CY49 GPP_B20/GSPI1_CLK
CY53 GPP_B22/GSPI1_MOSI
CY52 GPP_B21/GSPI1_MISO
DA50 GPP_B19/GSPI1_CS0#

TP67 TP20 — UART0_TXD — DV21 GPP_C9/UART0_TXD
TP68 TP20 — UART0_RXD — DT21 GPP_C8/UART0_RXD
DR21 GPP_C11/UART0_CTS#
DW21 GPP_C10/UART0_RTS#

A02, 20210226 Due to adding intel I225
Remove TPM ciruit for PM requirement (Add I225).
Remove TPM_PIRQ# (DU19).

DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD
DT19 GPP_C12/UART1_RXD/ISH_UART1_RXD
DR19 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#

TP69 TP20 — UART2_TXD — DJ21 GPP_C21/UART2_TXD
TP70 TP20 — UART2_RXD — DG23 GPP_C20/UART2_RXD
DJ19 GPP_C23/UART2_CTS#
DF21 GPP_C22/UART2_RTS#

DV18 GPP_C17/I2C0_SCL
DW18 GPP_C16/I2C0_SDA
DJ23 GPP_C19/I2C1_SCL
DT18 GPP_C18/I2C1_SDA
DJ29 GPP_H5/I2C2_SCL
DJ31 GPP_H4/I2C2_SDA

Refer to Nancom WHU/KBU
Remove CPU I2C3, I2C from EC
TP40 TP20 — I2C3_SCL — DF29 GPP_H7/I2C3_SCL
TP41 TP20 — I2C3_SDA — DG29 GPP_H6/I2C3_SDA

DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

Undriven / PD 20K ohm

DR27 GPP_D14/ISH_UART0_TXD
DW27 GPP_D13/ISH_UART0_RXD
DV25 GPP_D16/ISH_UART0_CTS#
DT25 GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
A02, 20210303
Remove reserved CPU_SSD_PWREN (DV25).

DB45 GPP_B6/ISH_I2C0_SCL
DB44 GPP_B5/ISH_I2C0_SDA
CY39 GPP_B8/ISH_I2C1_SCL
DB47 GPP_B7/ISH_I2C1_SDA
DD47 GPP_B10/I2C5_SCL/ISH_I2C2_SCL
DD44 GPP_B9/I2C5_SDA/ISH_I2C2_SDA

I/O: DJ8 GPP_E16/ISH_GP7; DR7 GPP_E15/ISH_GP6; DR24 GPP_D18/ISH_GP5; DU25 GPP_D17/ISH_GP4; DV31 GPP_D3/ISH_GP3/BK3/SBK3; DU31 GPP_D2/ISH_GP2/BK2/SBK2; DT27 GPP_D1/ISH_GP1/BK1/SBK1; DV27 GPP_D0/ISH_GP0/BK0/SBK0

DR51 GPP_RCOMP
Note: Close to CPU
Change size from 0402 to 0201
GPPC_RCOMP R123 200
1% R0201

DN33 GPP_T3 — BOARD_ID0
DT35 GPP_T2 — BOARD_ID1
DG17 GPP_U5 — BOARD_ID2
DG19 GPP_U4
Remove Board ID3 for saving space.

Check Board ID pin use and amounts.

BOARD ID

BOARD_ID0: +V3P3A — R418 Do Not Stuff (R0402 1%) — R419 20K (R0402 1%)
BOARD_ID1: +V3P3A — R420 Do Not Stuff (R0402 1%) — R421 20K (R0402 1%)
BOARD_ID2: +V3P3A — R8518 Do Not Stuff (R0402 1%) — R8519 20K (R0402 1%)
20200730 change to 0402 size

BOARD ID[1:0]:
000 MEM support total 16GB
001 MEM support total 8GB.

A0.2

AAEON Technology INC.

Title		
SoC HDA/I2C		
Size	Document Number	Rev
	NANOCOM-TGU	A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 8 of 34	

SoC PCIe/SATA/USB

SATA

LAN_GbE

PCIe x4

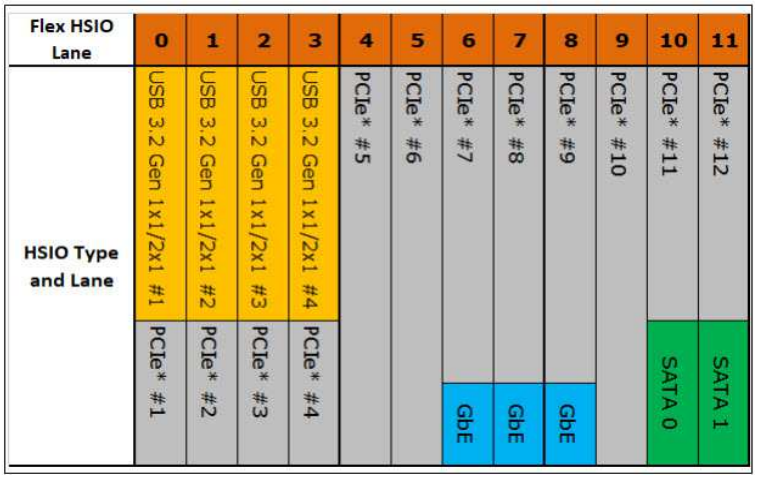
USB 3.2

USB2.0

PCIe SSD

A02, 20210303, Change C11/C12 placement for I225.
*Design Note:
The AC coupling capacitors should be placed within 1 inch of the transmit or receiver side.

20201007 PM Requirement
Remove PCH PCIe x2. Change to CPU PCIe x2.



PCI Express* Support

The TGL UP4/UP3 processor PCI Express* interface is a 4-lane (x4) port. The interconnect between the TGL UP4/UP3 processor and NVMe* storage provided through the M.2 connector. In addition, it will support graphics PCIe Gen4 devices too.

The TGL UP4/UP3/H processor supports the configurations shown in the following table:

PCI Express* 4 -lane Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
1x4	x4	1	0	1	2	3
1x4 **Reversed**	x4	0	3	2	1	0

Note: PCIe* Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable

A0.2

AAEON Technology INC.

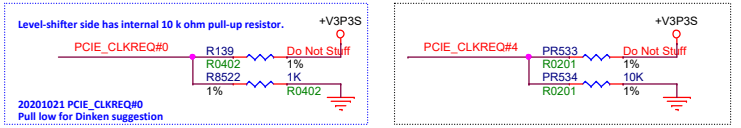
Title	SoC PCIe/SATA/USB	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 9 of 34	

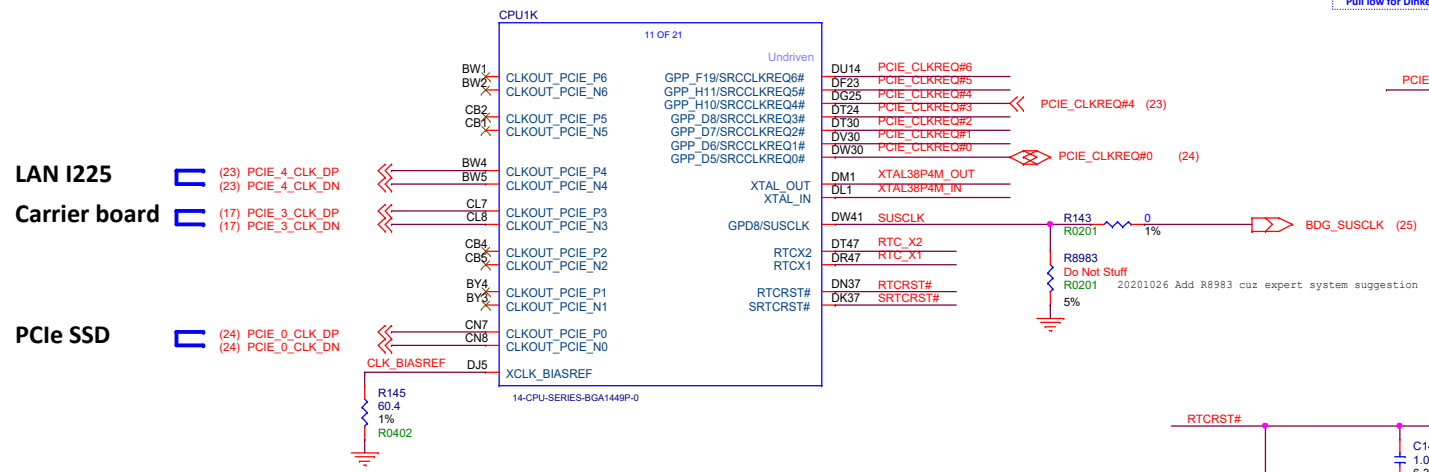
SoC PCIE_CLK/ RTC/ XTAL

A02, 20210312 Saving PCB space
Change PR533/PR534 from 1050510024 to 105B501039 (0201).

Level-shifter side has internal 10 k ohm pull-up resistor.

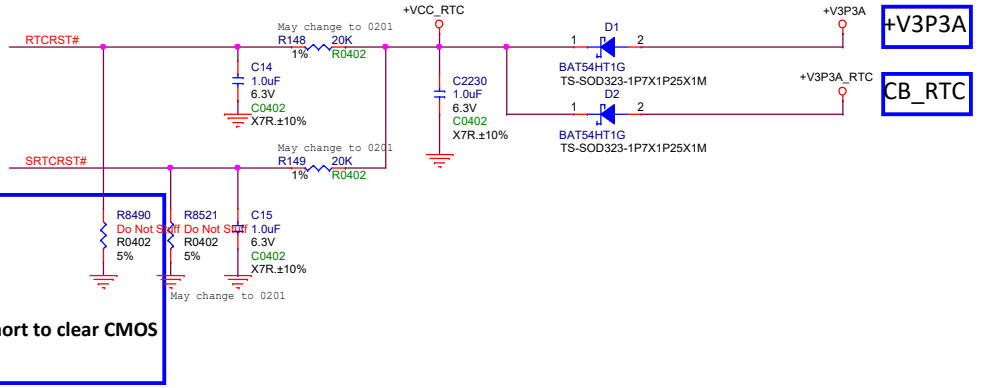
20201021 PCIE_CLKREQ#0
Pull low for Dinken suggestion





+VCC_RTC

SOC_RTC



+V3P3A

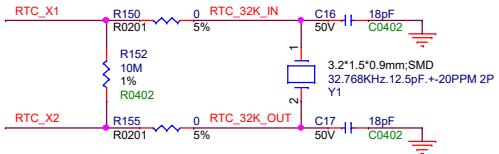
CB_RTC

RTC_RESET

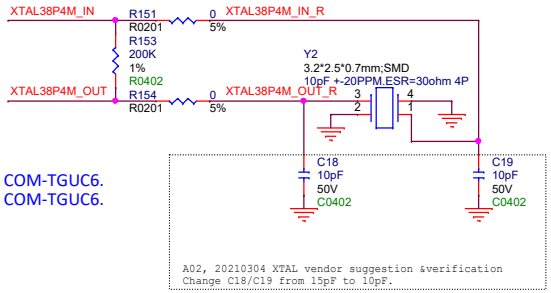
Status of CLR_CMOS at G3/S5/S0		
CLR_CMOS	RTCRST#	SRTCRST
HIGH (SW"SHORT")	RESET	RESET
LOW (SW"OPEN")	Normal Operation	Normal Operation

CLKOUT_PCIE_P /N [6:4, 2:1] = Support up to PCIe Gen3
CLKOUT_PCIE_P /N [3, 0] = Support up to PCIe Gen4

XTAL 32.768KHz



XTAL 38.4MHz



20201021 Change P/N of Y1 from 1231327631 to 1231327632 following COM-TGUC6.
20201021 Change P/N of Y2 from 1231038450 to 1231038451 following COM-TGUC6.

A02, 20210304 XTAL vendor suggestion &verification
Change C18/C19 from 15pF to 10pF.

A0.2

AAEON Technology INC.

Title		
SoC PCIE_CLK/ RTC		
Size: A3	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 10 of 34	

SoC CNVi

GPP_F0	XTAL SEL1
0 *	38.4/19.2MHZ (DEFAULT)
1	24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

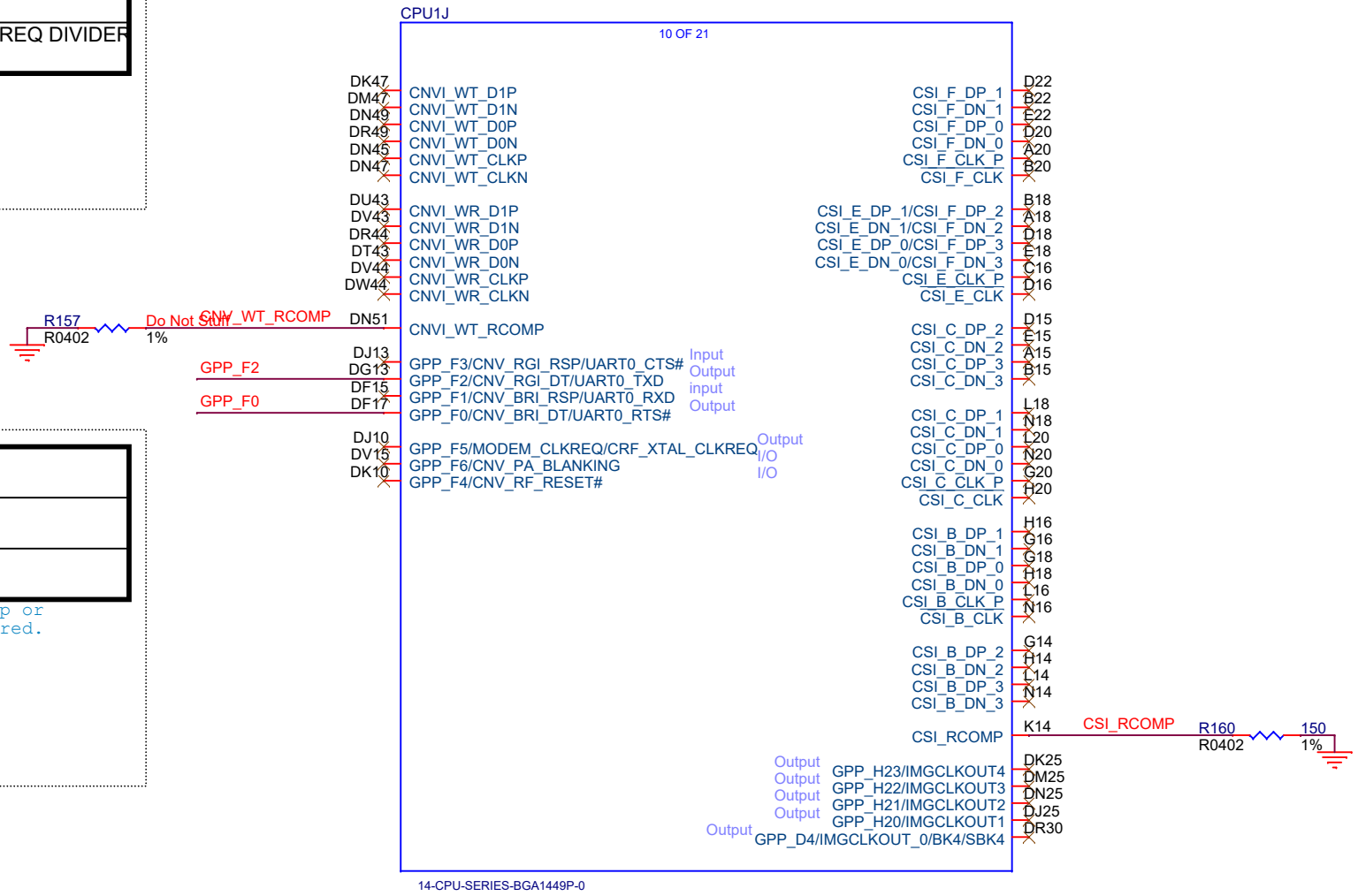
* Default, Internal Pull-Down 20k
24 MHz crystal is not supported

Remove reserve PU R, change to Test Point.
TP44 GPP_F0
TP20

GPP_F2	M.2 CNVi Mode Select
0	Integrated CNVi enabled.
1 *	Integrated CNVi disabled.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.

+V3P3A
May change 0201
R158 4.7K GPP_F2
R0402 1%
Remove reserve PD R



A0.2

AAEON An ASUS Company

AAEON Technology INC.

Title: SoC CNVi

Size	Document Number	Rev
	NANOCOM-TGU	A0.2_0_0

Date: Thursday, April 15, 2021 Sheet 11 of 34

SoC System

GPD7	Reserved
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A

20200724 Change to 0201

R167 0201 Do Not Stuff 5% GPD_7

Remove reserve PD R

SPIVCCIOSEL	STRAP FOR SPI 1.8V/3.3V SELECTION
0 *	3.3 V
1	1.8 V

An external resistor is required.

Remove reserve PU R

R176 0402 4.7K 1% SPIVCCIOSEL

May change to 0201

+VCC_RTC

R179 0402 1M 1% SM_INTRUDER#

PDG: DSW_PWROK and RSMRST# are always separate power good signals

R184 0201 1M 5% PCH_DPWROK

C20 C0201 Do Not Stuff 10V

+V3P3S

R185 0201 Do Not Stuff 5% O_SYS_PWROK

R8510 0201 Do Not Stuff 5%

Refer to 607872_TGL_UP3_UP4_Sch_Chk_Rev1p5 Reserved PD100K ohm

A02 20210317 Based on PDG suggestion Mount R2911.

R2911 0201 100K 5% I_SLP_S5

R544 0201 100K 5% I_SLP_S4

R545 0201 100K 5% I_SLP_S3

R8527 0201 100K 5% SLP_A#

R8528 0201 100K 5% SLP_WLAN#

R8529 0201 100K 5% PM_SLP_SUS#

R8530 0201 100K 5% SLP_LAN#

R8531 0201 100K 5% CPU_C10_GATE#

+V3P3A

A02, 20210303 follow PDG suggestion Modify SLP_S0# from pull down to pull high.

R186 0201 100K 5% SLP_S0#

Nanocom-TGU don't support C10 Deep Sleep mode.

CPU1L

12 OF 21

(31) PM_SLP_SUS# — PM_SLP_SUS# DV49

(20) I_SLP_S5 — R171 0 5% R0201 — SLP_S5# DM43

(20,28) I_SLP_S4 — R173 0 5% R0201 — SLP_S4# DJ41

(20,31,32) I_SLP_S3 — R174 0 5% R0201 — SLP_S3# DJ43

May remove TP8

May remove TP9

SLP_A# DR41

SLP_WLAN# DT44

A02, 20210303 Remove reserved EC PM_SLP_S0#(N12) & R177.

SLP_S0# DD42

SLP_LAN# DN39

(22,25) RSMRST# — RSMRST# DM35

PCH_SYSRST# DD10

R178 0201 Do Not Stuff 1%

PLTRST# DD41

(22) PCH_DPWROK — PCH_DPWROK R180 0402 0 5% — DSW_PWROK DK35

(20) O_SYS_PWROK — O_SYS_PWROK DF10

(25,32) PCH_PWROK — PCH_PWROK DN35

SM_INTRUDER# DM37

SPIVCCIOSEL DT49

SLP_SUS#

GPD10/SLP_S5#

GPD5/SLP_S4#

GPD4/SLP_S3#

GPD6/SLP_A#

GPD9/SPL_WLAN#

GPP_B12/SLP_S0#

SLP_LAN#

RSMRST#

SYS_RESET#

GPP_B13/PLTRST#

DSW_PWROK

SYS_PWROK

PCH_PWROK

INTRUDER#

SPIVCCIOSEL

Undriven

Undriven

Undriven

PROCPWRGD

GPD3/PWRBTN#

GPD0/BATLOW#

GPD1/ACPRESENT

GPP_B11/PMCALERT#

GPP_H18/CPU_C10_GATE#

GPP_H3/SX_EXIT_HOLDOFF#

WAKE#

GPD2/LAN_WAKE#

GPD11/LANPHYPC/DSWLDO_MON

GPD7

VCCSTPWRGOOD_TCSS

VCCST_PWRGD

VCCST_OVERRIDE

GPP_F20/EXT_PWR_GATE#

GPP_F21/EXT_PWR_GATE2#

BM9 CPUPWRGD

DK41 PWRBTN# — TP20 — R170 0 5% R0201 — O_PWR_BTN# (20)

DN41 O_BATLOW_R# — TP7 — R175 0 5% R0201 — O_BATLOW# (20)

DK43 AC_PRESENT

CW40 PMCALERT#

DN27 CPU_C10_GATE#

DG31 SX_EXIT_HOLDOFF#

DK39 — PCIE_WAKE# (17,23)

DM41 — LAN_WAKE# (23)

DT41

DN43 GPD_7

A02, 20210303 PM Spec change to I225, Remove PM_LAN1PHY_ENABLE (DT41) cuz this give to I219 use.

CE5 VCCSTPWRGOOD

BP8 VCCST_PWRGOOD — R182 0402 60.4 1% — H_VCCST_PWRGD (32)

BP9 VCCST_OVERRIDE

DR12 EXT_PWR_GATE#

DW12 EXT_PWR_GATE2#

14-CPU-SERIES-BGA1449P-0

+V3P3A

PCIE_WAKE# R161 0201 10K 1%

LAN_WAKE# R162 0201 10K 1%

O_BATLOW_R# R163 0402 8.2K

AC_PRESENT R164 0201 10K 1%

PWRBTN# R165 0402 8.2K 1%

EXT_PWR_GATE# R166 0201 100K 5%

EXT_PWR_GATE2# R168 0201 100K 5%

PMCALERT# R522 0201 10K 1%

SX_EXIT_HOLDOFF# R523 0201 10K 1%

CRB TGL_UP3_DDR4_SODIMM_RVP_SCH_REV1P0 Mount 10k ohm

CRB TGL_UP3_DDR4_SODIMM_RVP_SCH_REV1P0 PU 100k ohm

CRB TGL_UP3_DDR4_SODIMM_RVP_SCH_REV1P0 PU 100k ohm

Change to 0201

VCCSTPWRGOOD

VCCST_OVERRIDE

R181 0201 0 5%

A02, 20210303 Remove R183 and move PR160 to CPU side.

PR160 100K 5% R0201

Carry Board

*DESIGN NOTE: VCCST_PWRGD = 1: INDICATED VCCST (FIVR_1.05V) AND VDDQ RAIL ARE WITHIN VOLTAGE TOLERANCE SPEC

20200724 Change from 14S5A00821 to 145901G081 for saving PCB space.

+V3P3A

C2234 0.1uF 6.3V C0201

PLTRST#

U5

SN74AUP1G08DRLR

TS-SOT553_5-1P7X1P3X0P6M

R8534 100K 5% R0201

R8533 100K 5% R0201

R625 0 5% R0201

BUF_CB_RST# (17)

BUF_PLT_RST# (20,23,24,25)

eSPI to LPC
eDP to LVDS
LAN
EC
SSD

SYSRST#

+V3P3A

R192 10K 1% R0201

PCH_SYSRST#

D4 40V 1PS79SB30 TS-SOD523 — O_SYSRST# — O_SYSRST# (20)

D5 40V 1PS79SB30 TS-SOD523 — CARRY_SYSRST# — CARRY_SYSRST# (17)

A0.2

AAEON Technology INC.

Title: SoC System

Size: A3 | Document Number: NANOCOM-TGU | Rev: A0.2_0_0

Date: Thursday, April 22, 2021 | Sheet 12 of 34

SoC Strap

CFG14	PEG* Static x4 Lane Numbering Reversal
0	Lane numbers reversed
1 *	Normal operation

The CFG signals have a default value of '1'

+VCCIO_OUT

R193 R0201 10K 1% CFG14

R194 R0201 Do Not Stuff 5%

Change size to 0201

+VCCIO_OUT

R197 R0201 1K 5% CFG1

R195 R0201 1K 5% CFG2

R198 R0201 1K 5% CFG3

R199 R0201 1K 5% CFG9

R200 R0201 1K 5% CFG10

R201 R0201 1K 5% CFG11

CFG4	eDP Presence
0 *	ENABLE
1	DISABLE

The CFG signals have a default value of '1'

+VCCIO_OUT

R207 R0201 Do Not Stuff 1% CFG4

R209 R0201 1K 5%

CFG7	PEG Training
0	PEG Wait for BIOS for training
* 1	PEG Train immediately following RESET# de assertion

The CFG signals have a default value of '1'

+VCCIO_OUT

R211 R0201 Do Not Stuff 1% CFG7

R212 R0201 Do Not Stuff 5%

CPU1T

20 OF 21

20200730 Remove reserved TP

CFG14 → T15 CFG_15, V17 CFG_14, U15 CFG_13, K11 CFG_12, CFG11 → K12 CFG_11, CFG10 → K9 CFG_10, CFG9 → T17 CFG_9, K7 CFG_8, CFG7 → H7 CFG_7, K8 CFG_6, H9 CFG_5, CFG4 → E6 CFG_4, CFG3 → H5 CFG_3, CFG2 → E9 CFG_2, CFG1 → D9 CFG_1, E7 CFG_0

R202 R0402 49.9 1% CFG_RCOMP → B5 CFG_RCOMP

20200730 follow Intel COMe CRB Remove TP for pin U17/H11 → U17 CFG_17, H11 CFG_16

A02, 20210408 Saving PCB space
Remove all BPM nets and R203 (CPU1.Y3) & R204 (CPU1.M4) & R205 (CPU1.AB4) & R206 (CPU1.Y2) .

Y1 BPM#_3, M4 BPM#_2, AB4 BPM#_1, Y2 BPM#_0

DESIGN NOTE: FOR DEBUG PURPOSE ONLY

A3 RSVD_6, B3 RSVD_7

R208 R0402 2.2K 1% TCP0_MBIAS_RCOMP → AR2 TCP0_MBIAS_RCOMP

AL10 RSVD_TP_2, AM12 RSVD_TP_3, AH12 RSVD_TP_4, AJ10 RSVD_TP_5, AR1 RSVD_TP_6

BN10 RSVD_8, BM12 RSVD_9, DD13 RSVD_10, DF13 RSVD_11

RSVD_TP_7 A51, RSVD_TP_8 B51, RSVD_TP_9 C1, RSVD_TP_10 D2, RSVD_TP_11 CP39, RSVD_TP_12 CU40, RSVD_12 AK9, RSVD_13 AH9, RSVD_14 DW6, RSVD_15 DV6, RSVD_TP_13 DV4, RSVD_TP_14 DW3, RSVD_TP_15 DU1, RSVD_TP_16 DT2, RSVD_TP_17 DW2, RSVD_TP_18 DV2, RSVD_TP_19 E1, RSVD_TP_20 F1, RSVD_16 AB2, RSVD_TP_21 DR1, RSVD_TP_22 DR2, RSVD_TP_23 DR53, RSVD_TP_24 DW5

VSS_1 DV51, TP_3 DW52, TP_4 DV53, RSVD_17 W34, RSVD_18 V35, SKTOCC# D52

VSS_1 → TP20 TP20

+V3P3A

SKTOCC# → R210 R0201 Do Not Stuff 5% Change size to 0201

14-CPU-SERIES-BGA1449P-0

A0.2

AAEON® An ASUS Company

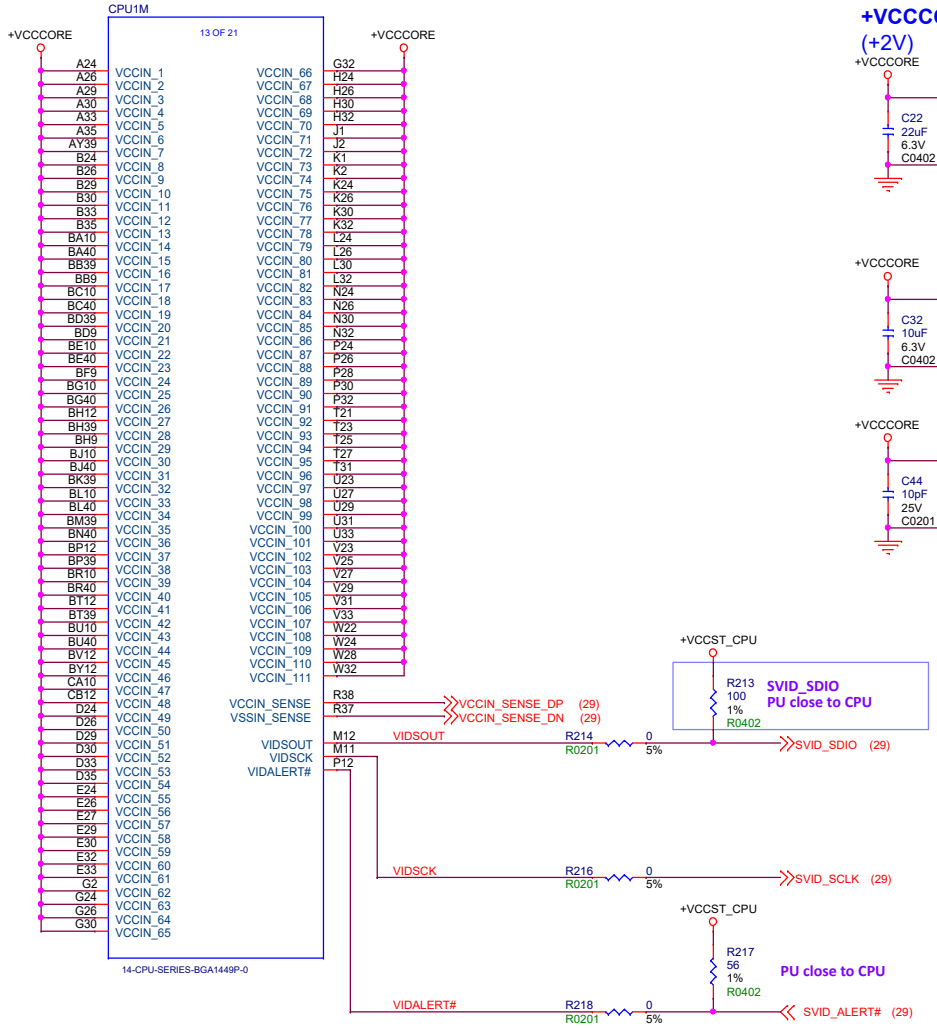
AAEON Technology INC.

Title: SoC Strap

Size	Document Number	Rev
A4	NANOCOM-TGU	A0.2_0_0

Date: Thursday, April 22, 2021 Sheet 13 of 34

SoC Power



Note: Intel COMe CRB Place 1uF x 24 for +VCCCORE

+VCCCORE@65A

(+2V)

+VCCCORE

22uF x 8~10 for UP3

C22 22uF 6.3V C0402
C23 22uF 6.3V C0402
C24 22uF 6.3V C0402
C25 22uF 6.3V C0402
C26 22uF 6.3V C0402
C27 22uF 6.3V C0402
C28 22uF 6.3V C0402
C29 22uF 6.3V C0402
C30 22uF 6.3V C0402
C31 22uF 6.3V C0402

+VCCCORE

10uF x 6~12 for UP3

C32 10uF 6.3V C0402
C33 10uF 6.3V C0402
C34 10uF 6.3V C0402
C35 10uF 6.3V C0402
C36 10uF 6.3V C0402
C37 10uF 6.3V C0402
C38 10uF 6.3V C0402
C39 10uF 6.3V C0402
C40 10uF 6.3V C0402
C41 10uF 6.3V C0402
C42 10uF 6.3V C0402
C43 10uF 6.3V C0402

+VCCCORE

10pF x 6 for EMC

C44 10pF 25V C0201
C45 10pF 25V C0201
C46 10pF 25V C0201
C47 10pF 25V C0201
C48 10pF 25V C0201
C49 10pF 25V C0201

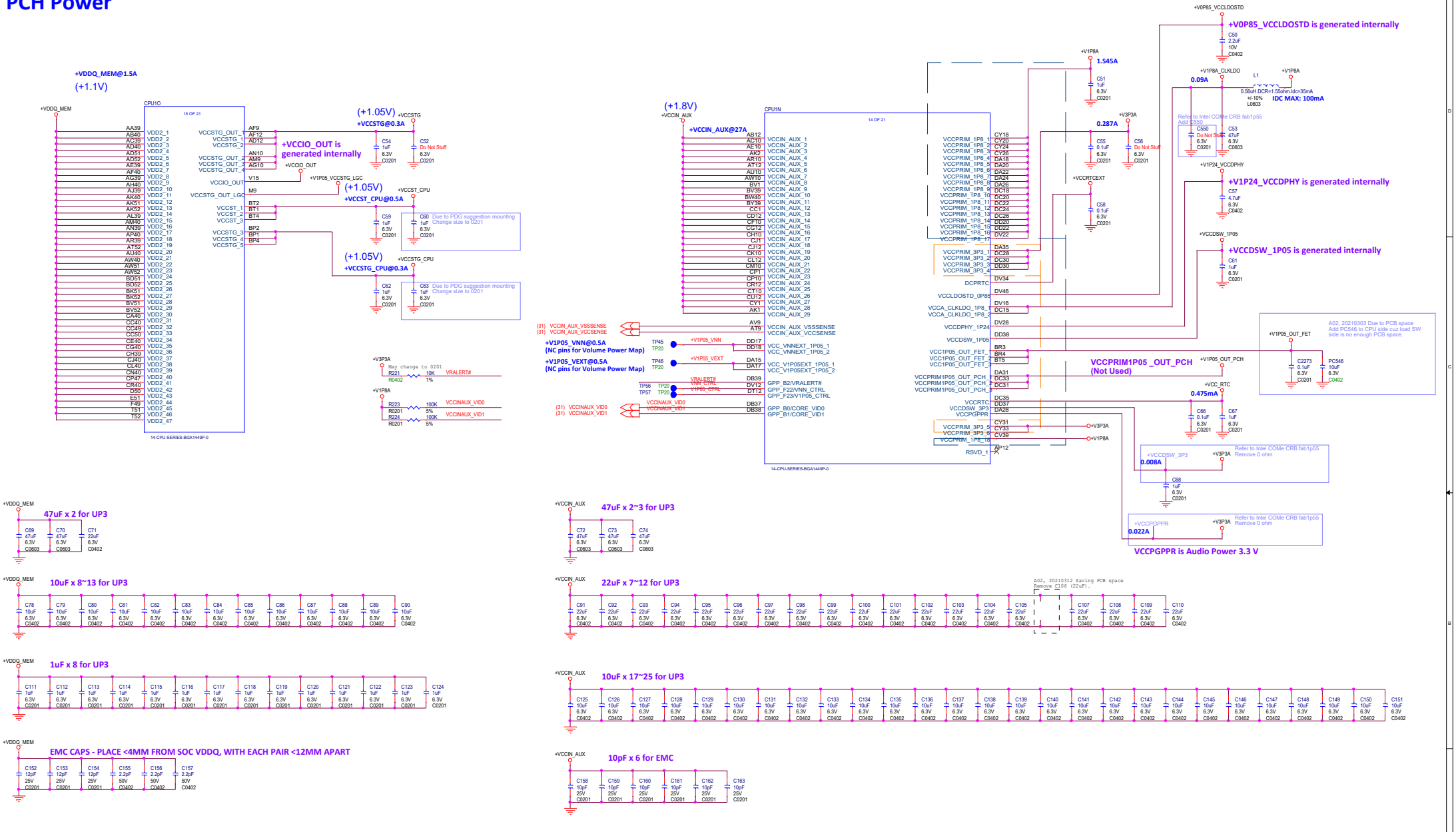
Place the PU resistors close to CPU

A0.2

AAEON Technology INC.

Title	SoC Power1	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 14 of 34	

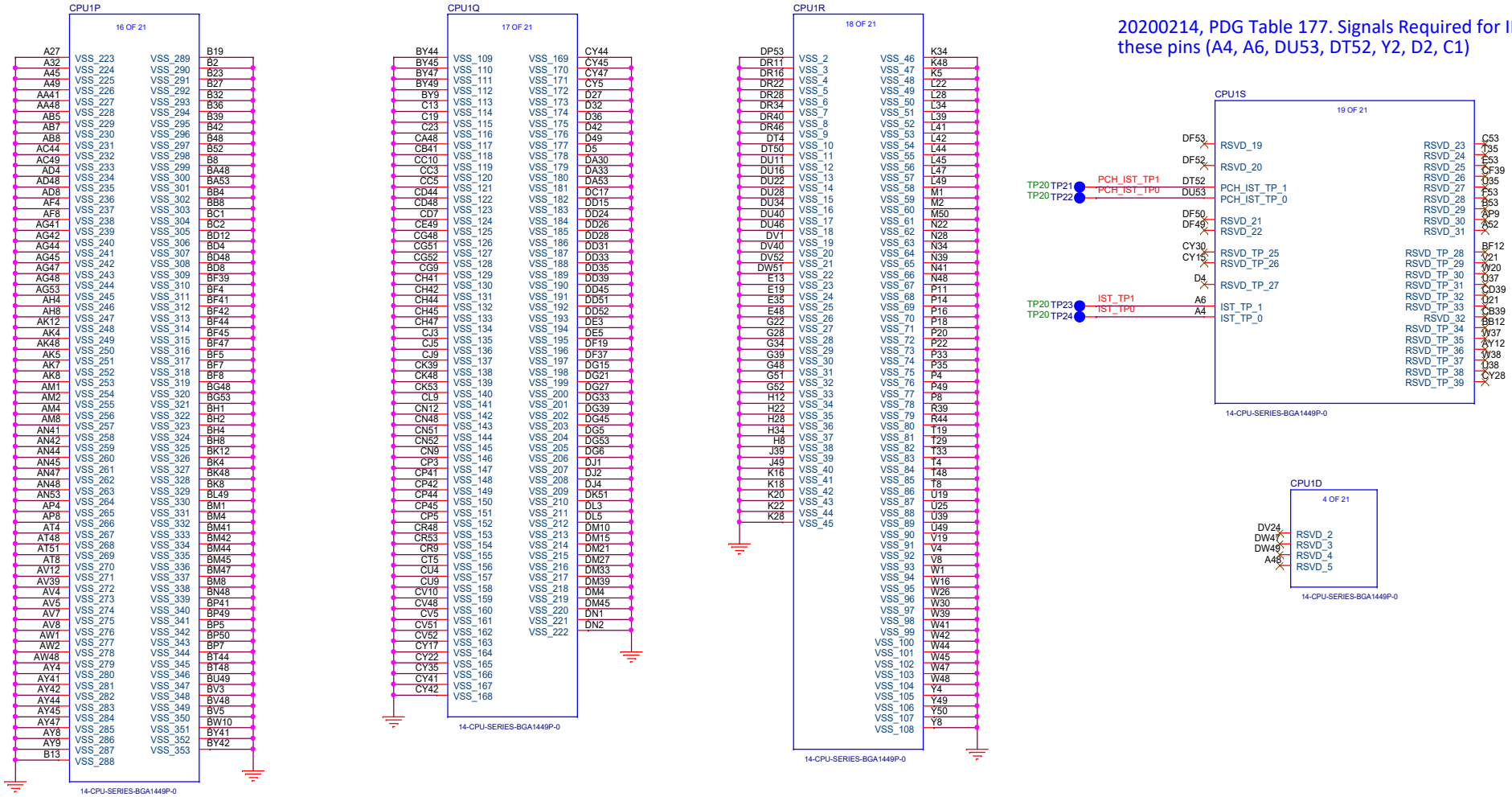
PCH Power



A0.2

AAEON Technology INC.	
Title	PCH Power
Size	A2
Document Number	NANOCOM-TGU
Rev	A0.2_0_0
Date:	Thursday, April 22, 2021
Sheet	15 of 34

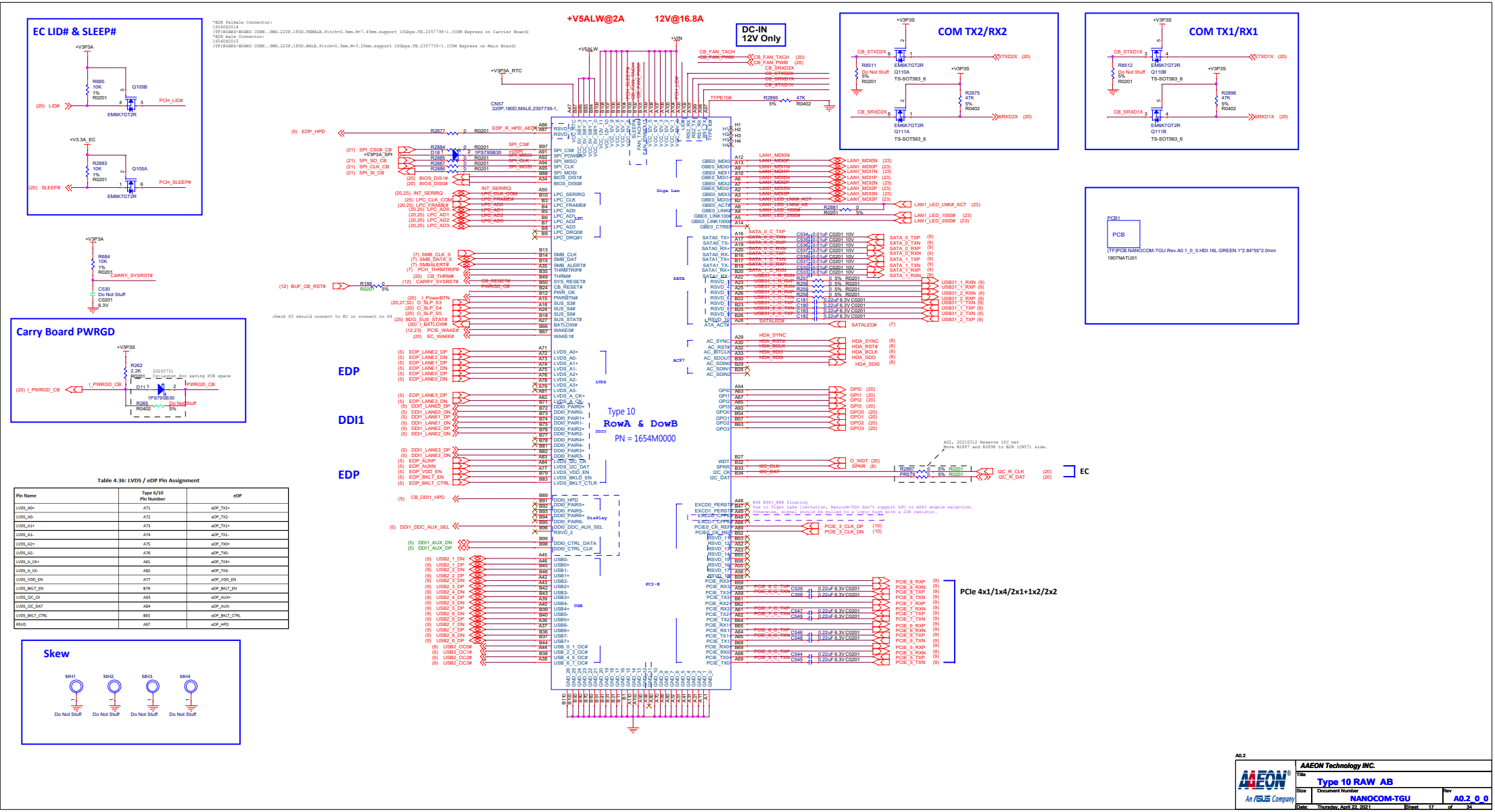
SoC GND



20200214, PDG Table 177. Signals Required for IFDIM at these pins (A4, A6, DU53, DT52, Y2, D2, C1)

A0.2

AAEON An ASUS Company	AAEON Technology INC.	
	Title: SoC GND	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 16 of 34	



A0.2

AAEON Technology INC.

Title: Type 10 RAW AB

Size | Document Number: NANOCOM-TGU | Rev: A0.2_0_0

Date: Thursday, April 22, 2021 | Sheet 17 of 34

LPDDR4x CHA

*LPDDR4x type:
1. 8GB per SDRAM supoort 4266
PN:1468X00013
(TF)SDRAM.SMD.64(2Gig x 32)Gb.8GB.2133MHz.1.1V.FBGA.200P.X8.LPDDR4/4x.4266(Mb/s/pin).Micron.MT53E2G32D4DT-046 WT:A
2.4GB per SDRAM supoort 3733
PN:1468X00012
(TF)SDRAM.SMD.32(1024Mx32)Gb.4GB.1866MHz.1.1V.FBGA.200P.X8.LPDDR4/4x.Micron.MT53D1024M32D4DT-053 WT:D

U28
200P,MT53E2G32D4DT-046 WT:A,

*Layout note:
Ecah 8 bits
swap by routing

A02, 20210325 SWAP DQ cause re-routing DDR net.

(6) M_A_DQ_0_4
(6) M_A_DQ_0_6
(6) M_A_DQ_0_3
(6) M_A_DQ_0_2
(6) M_A_DQ_0_0
(6) M_A_DQ_0_1
(6) M_A_DQ_0_7
(6) M_A_DQ_0_5
(6) M_A_DQ_1_5
(6) M_A_DQ_1_6
(6) M_A_DQ_1_1
(6) M_A_DQ_1_0
(6) M_A_DQ_1_2
(6) M_A_DQ_1_3
(6) M_A_DQ_1_7
(6) M_A_DQ_1_4
(6) M_A_DQ_2_4
(6) M_A_DQ_2_6
(6) M_A_DQ_2_7
(6) M_A_DQ_2_5
(6) M_A_DQ_2_3
(6) M_A_DQ_2_1
(6) M_A_DQ_2_0
(6) M_A_DQ_2_2
(6) M_A_DQ_3_1
(6) M_A_DQ_3_2
(6) M_A_DQ_3_3
(6) M_A_DQ_3_0
(6) M_A_DQ_3_5
(6) M_A_DQ_3_7
(6) M_A_DQ_3_6
(6) M_A_DQ_3_4

B2 C2 E2 F2 F4 E4 C4 B4 B11 C11 E11 F11 F9 E9 C9 B9 AA2 Y2 V2 U2 U4 V4 Y4 AA4 AA11 Y11 V11 U11 U9 V9 Y9 AA9
DQ0_A DQ1_A DQ2_A DQ3_A DQ4_A DQ5_A DQ6_A DQ7_A DQ8_A DQ9_A DQ10_A DQ11_A DQ12_A DQ13_A DQ14_A DQ15_A
DQ0_B DQ1_B DQ2_B DQ3_B DQ4_B DQ5_B DQ6_B DQ7_B DQ8_B DQ9_B DQ10_B DQ11_B DQ12_B DQ13_B DQ14_B DQ15_B

(6) M_A_DQS_0_DP
(6) M_A_DQS_0_DN
(6) M_A_DQS_1_DP
(6) M_A_DQS_1_DN
(6) M_A_DQS_2_DP
(6) M_A_DQS_2_DN
(6) M_A_DQS_3_DP
(6) M_A_DQS_3_DN

D3 E3 D10 E10 W3 V3 W10 V10
DQS0_t_A DQS0_c_A DQS1_t_A DQS1_c_A DQS0_t_B DQS0_c_B DQS1_t_B DQS1_c_B

(19) DDR4_DRAMRST_R_N — T11 RESET_n

C454 Do Not Stuff 6.3V C0201

CA0_A CA1_A CA2_A CA3_A CA4_A CA5_A CA0_B CA1_B CA2_B CA3_B CA4_B CA5_B
H2 J2 H9 H10 H11 J11 R2 P2 R9 R10 R11 P11
M_A_LP4_0CA0 (6) M_A_LP4_0CA1 (6) M_A_LP4_0CA2 (6) M_A_LP4_0CA3 (6) M_A_LP4_0CA4 (6) M_A_LP4_0CA5 (6) M_A_LP4_1CA0 (6) M_A_LP4_1CA1 (6) M_A_LP4_1CA2 (6) M_A_LP4_1CA3 (6) M_A_LP4_1CA4 (6) M_A_LP4_1CA5 (6)

CK_t_A CK_c_A CK_t_B CK_c_B
J8 J9 P8 P9
M_A_LP4_CLK0_DP (6) M_A_LP4_CLK0_DN (6) M_A_LP4_CLK1_DP (6) M_A_LP4_CLK1_DN (6)

DMI0_A DMI1_A DMI0_B DMI1_B
C3 C10 Y3 Y10

CS0_A CS1_A CS2_A CS0_B CS1_B CS2_B
H4 H3 K5 R4 R3 N5
M_A_LP4_0CS0 (6) M_A_LP4_0CS1 (6) M_A_LP4_1CS0 (6) M_A_LP4_1CS1 (6)

CKE0_A CKE1_A CKE2_A CKE0_B CKE1_B CKE2_B
J4 J5 K8 P4 P5 N8
M_A_LP4_0CKE0 (6) M_A_LP4_0CKE1 (6) M_A_LP4_1CKE0 (6) M_A_LP4_1CKE1 (6)

ZQ0 A5 — ZQ0_CHA_0 — R588 240 1% R0201 — +VDDQ_LP4X_MEM
ZQ1 A8 — ZQ1_CHA_0 — R584 240 1% R0201 — +VDDQ_MEM
ZQ2 G11

ODT_CA_A G2 — ODT_A_CHA_0 — R601 0 R0201
ODT_CA_B T2 — ODT_B_CHA_0 — R602 0 R0201

DNU1 A1
DNU2 A2
DNU3 A11
DNU4 A12
DNU5 B1
DNU6 B12
DNU7 AA1
DNU8 AA12
DNU9 AB1
DNU10 AB2
DNU11 AB11
DNU12 AB12

VDD2_1 VDD2_2 VDD2_3 VDD2_4 VDD2_5 VDD2_6 VDD2_7 VDD2_8 VDD2_9 VDD2_10 VDD2_11 VDD2_12 VDD2_13 VDD2_14 VDD2_15 VDD2_16 VDD2_17 VDD2_18 VDD2_19 VDD2_20 VDD2_21 VDD2_22 VDD2_23 VDD2_24
A4 A9 F5 F8 H1 H5 H8 H12 K1 K3 K10 K12 N1 N3 N10 N12 R1 R5 R8 R12 U5 U8 AB4 AB9

VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12 VDDQ_13 VDDQ_14 VDDQ_15 VDDQ_16 VDDQ_17 VDDQ_18 VDDQ_19 VDDQ_20
B3 B5 B8 B10 D1 D5 D8 D12 F3 F10 U3 U10 W1 W5 W8 W12 AA3 AA5 AA8 AA10

VDD1_1 VDD1_2 VDD1_3 VDD1_4 VDD1_5 VDD1_6 VDD1_7 VDD1_8
F1 F12 G4 G9 T4 T9 U1 U12

+VDDQ_MEM
C2306 1uF 6.3V C0201
C2307 1uF 6.3V C0201
C2308 1uF 6.3V C0201
C2309 1uF 6.3V C0201
C2310 1uF 6.3V C0201
1uF x 6 for UP3
10uF x 2 for UP3

+VDDQ_LP4X_MEM
C2315 1uF 6.3V C0201
C2311 1uF 6.3V C0201
C2312 1uF 6.3V C0201
C2313 1uF 6.3V C0201
C2314 1uF 6.3V C0201
1uF x 6 for UP3
10uF x 2 for UP3

+V1.8U_MEM
C2318 1uF 6.3V C0201
C2316 1uF 6.3V C0201
C2317 1uF 6.3V C0201
1uF x 4 for UP3
10uF x 2 for UP3

+VDDQ_MEM 1.1V
C2291 10uF 6.3V C0402
C2297 10uF 6.3V C0402
C2299 1uF 6.3V C0201

+VDDQ_LP4X_MEM 0.6V
C2292 10uF 6.3V C0402
C2296 10uF 6.3V C0402
C2303 1uF 6.3V C0201

+V1.8U_MEM
C2294 10uF 6.3V C0402
C2305 10uF 6.3V C0402
C2298 1uF 6.3V C0201

20210324 Saving PCB space for DDR routing & follow PDG about the caps amount
Remove C2302/C2293 for +VDDQ_MEM.
Remove C2304/C2295 for +VDDQ_LP4X_MEM.
Remove C2301/C2300 for +V1.8U_MEM.

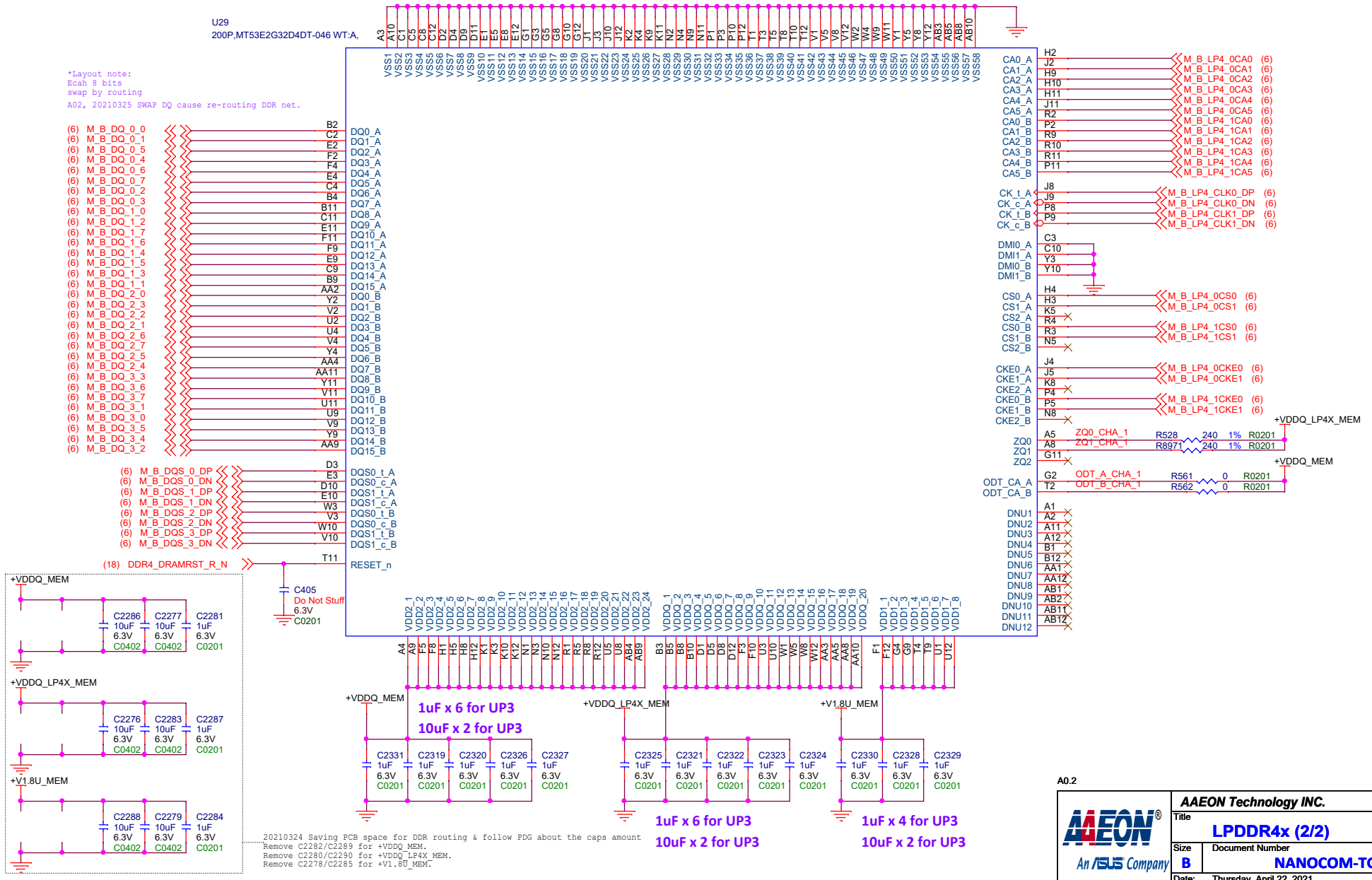
+VDDQ_MEM
*Layout note: CPU->CA_VREF Circuit-->DRAM0-->DRAM1-->DRAM2-->DRAM3
R2855 470 1% R0402
(6) DRAM_RESET_N — R2933 0 5% R0402 — DDR4_DRAMRST_R_N

A0.2

AAEON Technology INC.
An ASUS Company

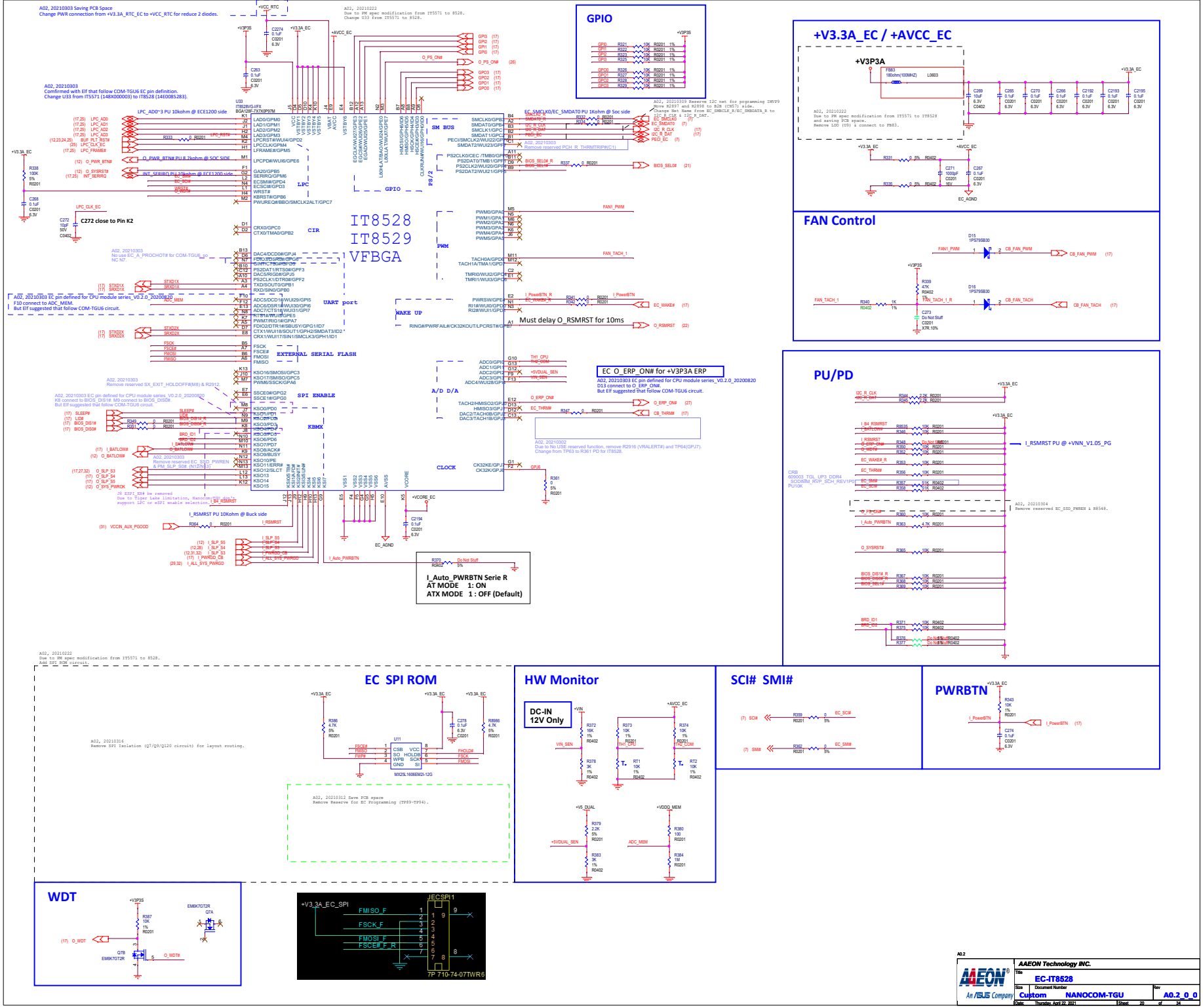
Title: LPDDR4x (1/2)		
Size: B	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 18 of 34	

LPDDR4x CHB

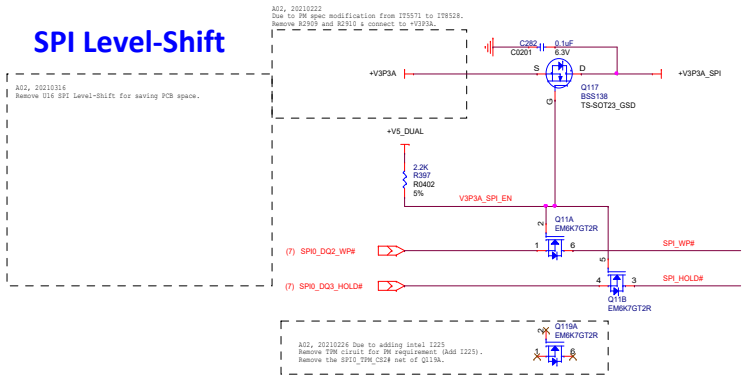


A0.2

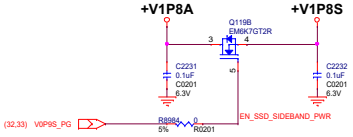
AAEON Technology INC.		
Title: LPDDR4x (2/2)		
Size: B	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 19 of 34	


GPIO
+V3.3A_EC / +AVCC_EC
+V3P3A
FAN Control
PU/PD
IT8528
IT8529
VFBGA
EC_O_ERP_ON# for +V3P3A ERP
I_RSMRST PU @ +VNN_V1.05_PG
Must delay O_RSMRST for 10ms
EC SPI ROM
HW Monitor
DC-IN
12V Only
SCI# SMI#
PWRBTN
WDT
I_Auto_PWRBTN Serie R
AT MODE 1: ON
ATX MODE 1 : OFF (Default)
C272 close to Pin K2
EC_AGND
AAEON Technology INC.
EC-IT8528
NANOCOM-TGU
A0.2_0_0

SPI Level-Shift



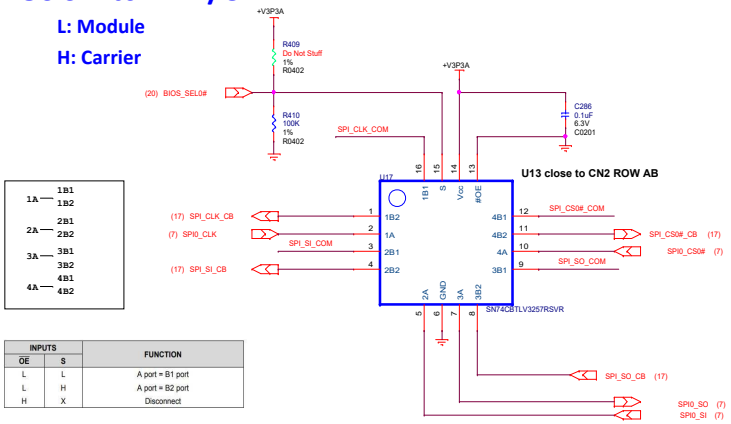
For PCIe SSD 1 Pull high and One Level-shifter use



BIOS Switch MB/CB

L: Module

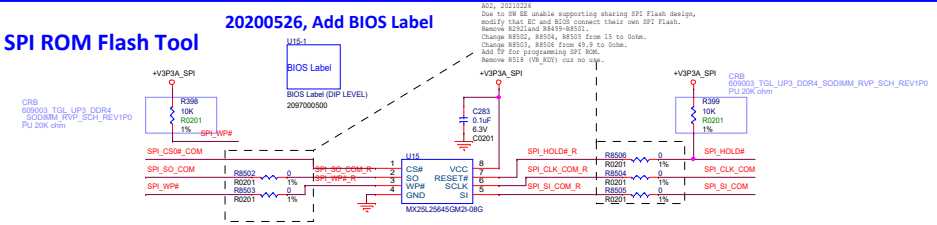
H: Carrier



INPUTS		FUNCTION
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

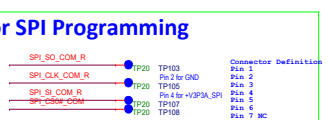
SPI ROM Flash Tool

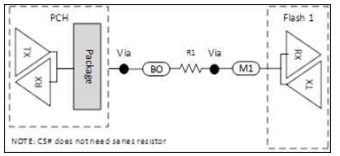
20200526, Add BIOS Label



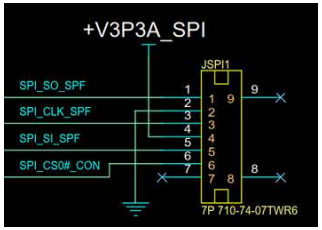
1462002564 / (TF)IC.Flash Memory.256M Bit serial.SOP-8(209mil).w/ Dual & Quad SPI.SMD.MACRONIX.MX25L25645GM2I-08G

Reserve for SPI Programming





*Jumper wire reference for Debug use:



IO\LSIO\Interfaces\SPI0 Flash\1-Load Topology (Device Down) MAF\Notes

Notes	Details
Number of vias allowed	7
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	75Ω±5% for 1.8V, 62Ω±5% for 3.3V To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3

TPM

A02, 20210226 Due to adding intel I225
Remove TPM circuit for PM requirement (Add I225).
Remove TPM IC (U151).

A0.2

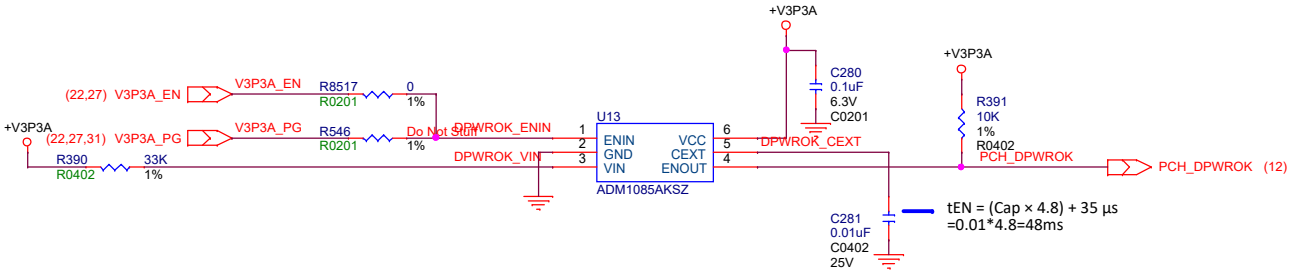
AAEON Technology INC.

Title: SPI ROM / SW

Size: Custom | Document Number: NANOCOM-TGU | Rev: A0.2_0_0

Date: Thursday, April 22, 2021 | Sheet 21 of 34

DSW_PWROK Control



3.3V x 10 / (10+33) = 0.767

ENIN VIH = 0.3*VCC+0.2 =1.19V

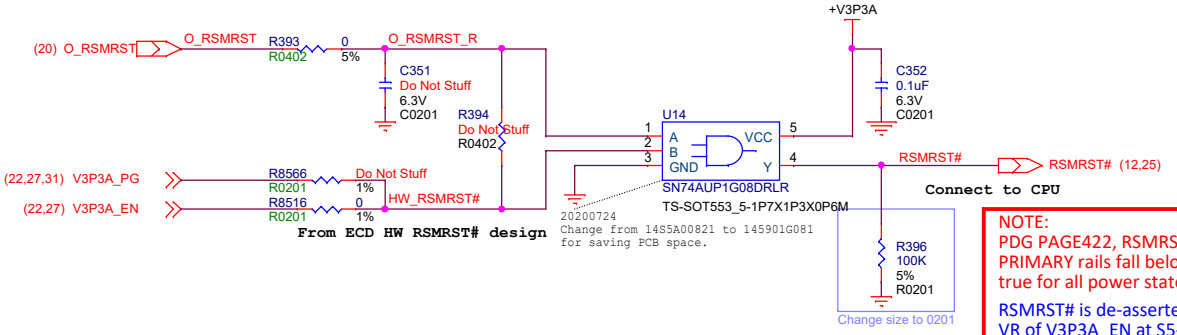
ENIN VIL = 0.3*VCC- 0.2 = 0.79V

ENOUT/ENOUT# Voltage Low (MAX =0.4V),When Vin < Vth_falling (ENOUT) / Vin > Vth_rising (ENOUT#)

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	2.25		3.6	V	
V_{IN} Operating Voltage Range	0		22	V	
Supply Current		10	15	µA	
V_{IN} Rising Threshold, V_{TH_RISING}	0.56	0.6	0.64	V	V_{CC} = 3.3 V
V_{IN} Falling Threshold, $V_{TH\_FALLING}$	0.545	0.585	0.625	V	V_{CC} = 3.3 V
V_{IN} Hysteresis		15		mV	

RSMRST# Control



NOTE:
PDG PAGE422, RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band. This is true for all power states transitions including emergency power loss.

RSMRST# is de-asserted by EC of O_RSMRSTon G3->S5, Asserted by VR of V3P3A_EN at S5->G3 before VccPRIM dropping.

A0.2

AAEON Technology INC.

Title: RSMEST# Control

Size	Document Number	Rev
B	NANOCOM-TGU	A0.2_0_0

Date: Thursday, April 22, 2021 Sheet 22 of 34

LAN I225

20210303, A02, Change ethernet controller from I219 (1440219LM0) to I225(144X000026)(U8).

Foxville
I225

56P,I225-LM SLNNH(version.B3),
TA=0 to 70 °C
QFN56G-7X7-1
(TF)IC.Ethernet.SMD.PCI-E 2.5G GigaBit Ethernet Chipset.VQFN.56P.Intel.I225-LM SLNNH(version.B3)

*SMBUS DESIGN NOTE:
I225 Default SMBUS Address is 0x49.

*SMBUS DESIGN NOTE:
1. I225 SMBUS speed default is 1MHz so the pull-ups should be 499ohm.
2.When adding VoltageShifter/Buffer/Repeater on the SMBUS, the pull-up value might change to 1Kohm.
3.Change the pull-ups to 2.2Kohm when runs @400KHz or 10Kohm when runs @100KHz.

*PCIe DESIGN NOTE:
PCIe must be configured as a standard PCIe port. Do Not configure to the Gbe port (like I219).

A02, 20210319 TGU only support I219 LAN WAKE from EDS
Connect R9012 to PCIe WAKE & Reserve R8990 for LAN WAKE.

*Nomal opeartion: unmount R52
At low, the JTAG is in the reset state and the multiplexed pins JTAG/SDPs act as SDPs. This pin has an internal weak pull-down that holds the JTAG controller in its reset state if the pin is left open.
*Enable Test Reset. Mount R52.
*If need PCB space, could remove R52 and add Test point.

A02, 20210416
Change XTAL(Y4) back to 12310025A5 cuz 12310025AF doesn't suggest by purchaser and lead time 1 year/no stock in Aeeon.

*Crystal
Trace Length: The crystal trace lengths should be less than 1 inch.

A02, 20210312 Save PCB space
Remove Reserve for EC Programming (TP97~TP102).
SPI Isolation

A02, 20210312 Save PCB space
Remove Reserve for EC Programming (TP97~TP102).

*If PCB space isn't enough, change U141 from 1469000007 to 1463X00007.
Add MOS and TP for code programming.

*LED DESIGN NOTE:
There is no specific industrial standard for Ethernet LEDs.
This schematic just shows the most common SPEED LED configuration:
Highest Speed = Green
2nd Highest Speed = Yellow
All other lower Speeds = OFF
No Cable/Link = OFF
All LED pins are set active low. See Datasheet for additional info.

ADD THE CIRCUIT FOR LAN LED LEAKAGE ISSUE

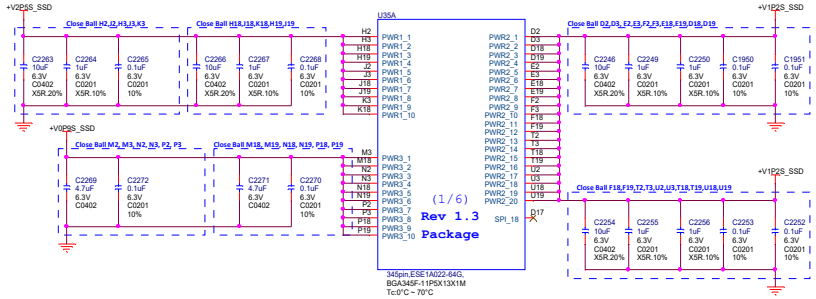
A0.2

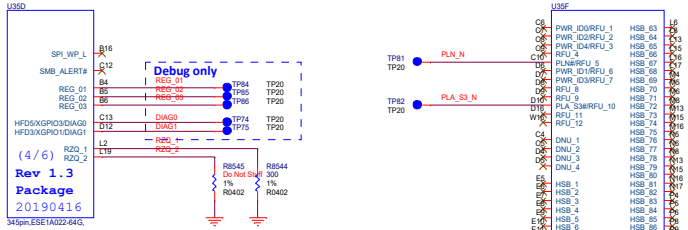
AAEON Technology INC.

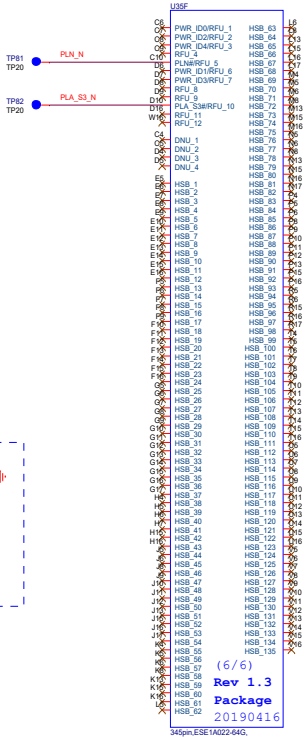
Title: LAN I225		
Size: Custom	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 23 of 34	

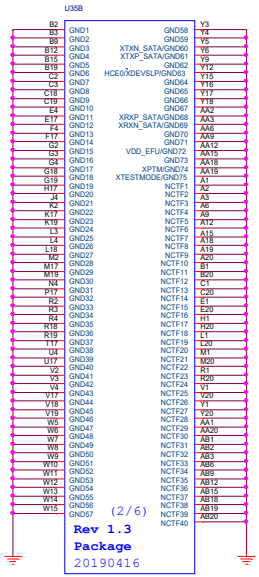
PCIe SSD

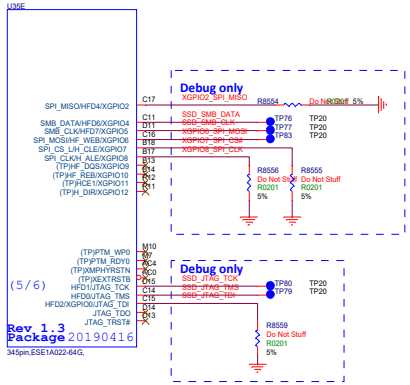
DNU: Do not use. Manufacturing purpose only
RFU: Reserved for future use

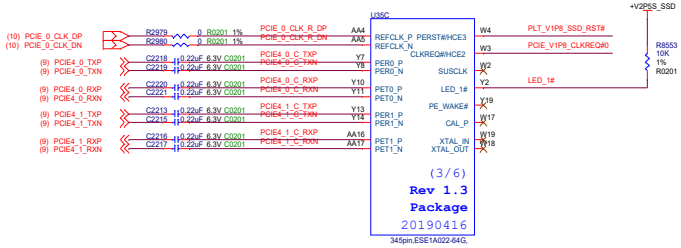


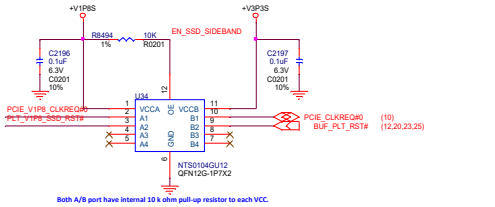








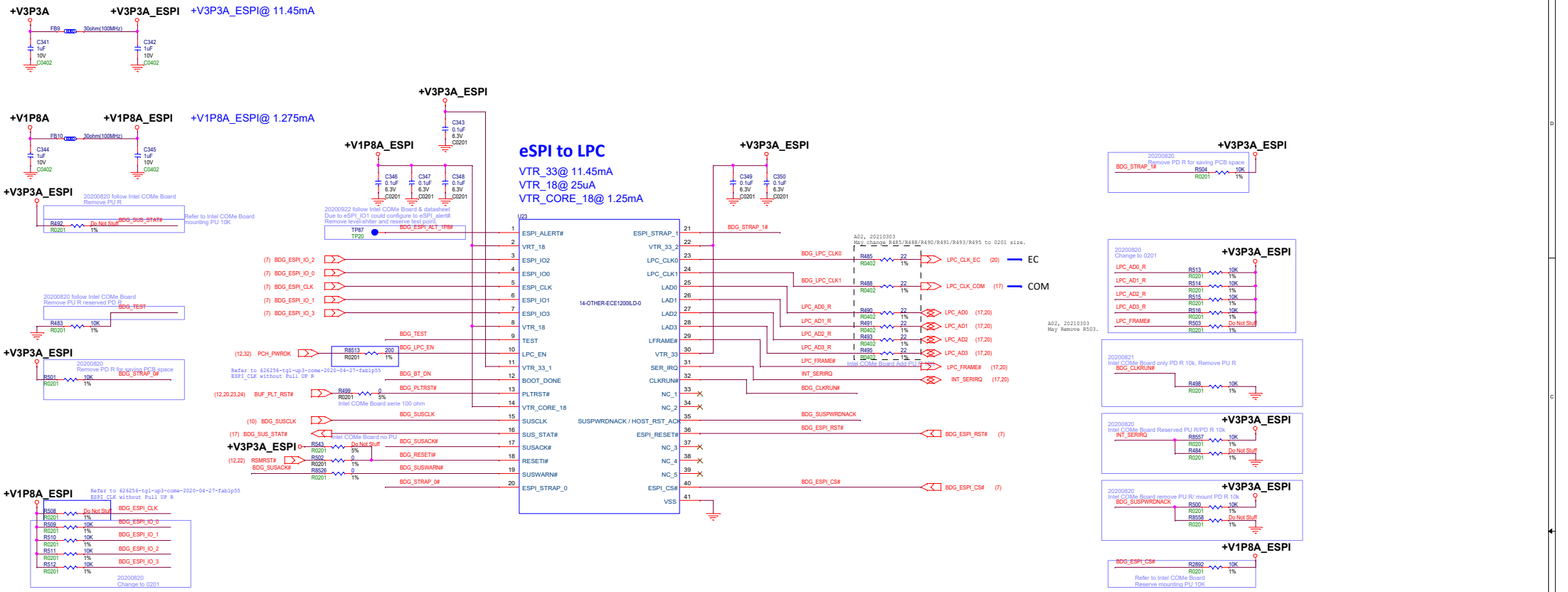




A0.2

AAEON Technology INC.

Title	PCIe SSD	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 24 of 34	



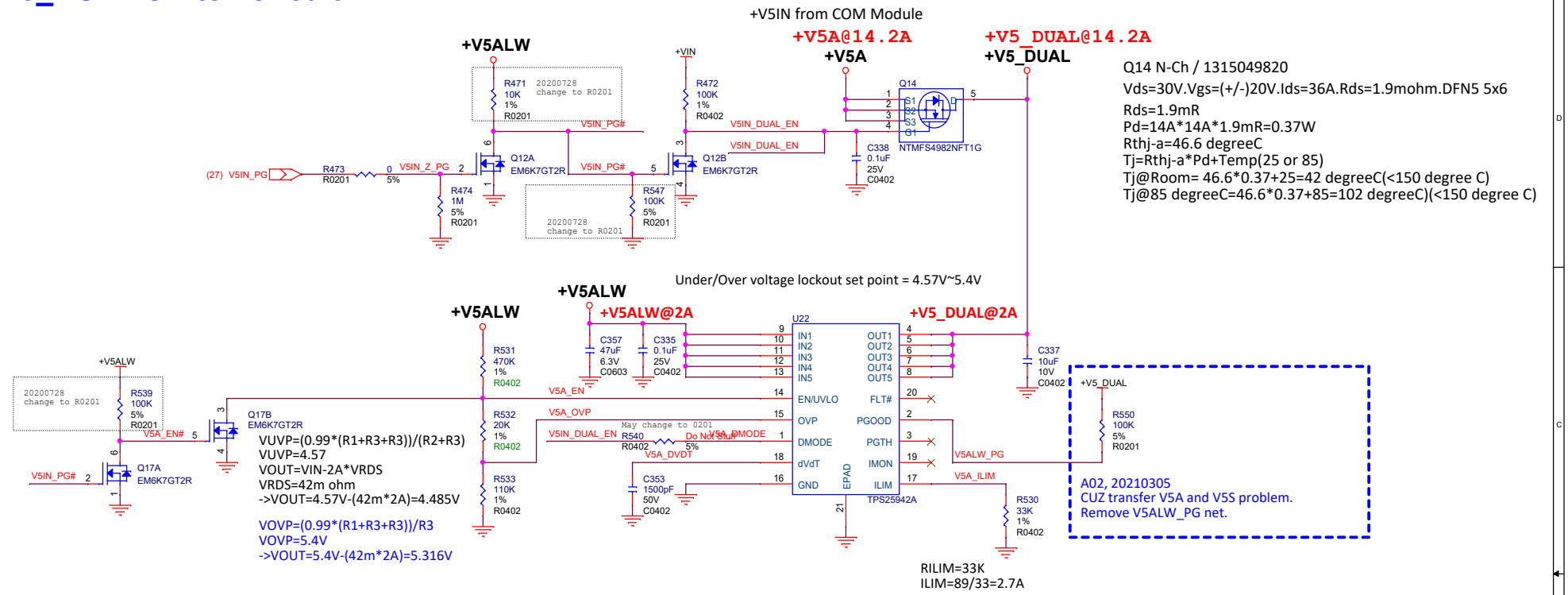
BOOT_DONE	
0	ECE1200 assumes the Secondary eSPI Slave role. Certain Virtual Wire interactions will not occur, deferring to another Primary device for this traffic. SUSPWRDNACK/HOST_RST_ACK pin = HOST_RST_ACK
1 *	ECE1200 assumes the Primary eSPI Slave role. At the first oppor-tunity, it will transmit VWires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS as '1' to the Chipset. SUSPWRDNACK/HOST_RST_ACK pin = SUSPWRDNACK

A0.2

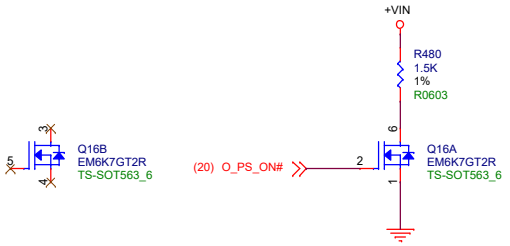
AAEON Technology INC.

Title	eSPI to LPC	
Size	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 25 of 34	

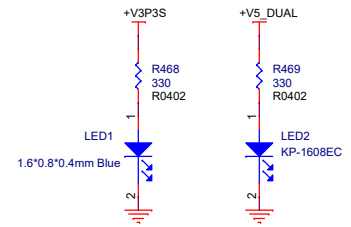
+V5_DUAL switch circuit



Discharge Circuit



LED



A0.2

AAEON An ASUS Company

Title: +V5_Dual/ Discharge/ LED		
Size: A3	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet: 26 of 34	

+V5A

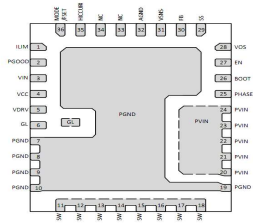
$$I_{LMT} = I_{LMT\_Valley} + \frac{V_o \times (V_{IN} - V_o)}{2 \times V_{in} \times L \times F_{SW}}$$

$$= 1.5412 \times R_{Ilim} + \frac{V_o \times (V_{IN} - V_o)}{2 \times V_{IN} \times L \times F_{SW}}$$

Table 1. MODE AND SWITCHING FREQUENCY CONFIGURATION

Resistance @ MODE/FSET Pin (Ω, ±1%)	Frequency (kHz)	Operation Mode
0	600	FCCM
2.49k	1000	FCCM
4.99k	500	Auto CCM/DCM
7.5k	500	FCCM
10.5k	600	Auto CCM/DCM
12.1k	800	Auto CCM/DCM
14.0k	1000	Auto CCM/DCM
Float	800	FCCM

PINOUT



A02, 20210226
CUZ the voltage divider is wrong for +V5A EN, FAE suggest the correct value.
Change PR524 from 26.1kohm to 120kohm and change PR525 from 10kohm to 22kohm.

A02, 20210226 FAE suggestion
CUZ the PG of +V5A discharge slowly, cause MOS of +V5 DUAL switching mismatch.
Change the PG of PWR from +V5A to V5IN_VCC (internal LDO PWR).

+VIN
V5IN_VCC
PR524 120K 1% R0402
PR525 22K 1% R0402
C2167 16V 0.001uF C0402
PR527 5.11K 1% R0402
PR528 Do Not Stuff R0402
(26,27) V5IN_PG
R8471 1 R0603
C2169 25V 1uF C0402
C2170 16V 4.7uF C0603
C2179 25V 1uF C0402
R8472 1 R0402
R8474 100 C0402
R8475 0 C0402
C2181 50V 10pF C0402
R8476 0 C0402
R8477 63.4K R0402
R8478 12K R0402
C2182 100pF 50V C0402
R8480 100 C0402
R8481 0 C0402
R8482 0 C0402
R8483 6.04K R0402
R8484 Do Not Stuff C0402
R8479 1 R0805
C2189 50V 1000pF C0402
R8485 1K R0402

PU1
EN
PGood
VIN
VDRV
VCC
FB
Vsns-
GL1
GL2
SS
MODE/FSET
Ilim
HICCUP#
AGND
36P,NCP3284MNTXG,
QFN37F-5X6X0P75M

VSIN_EN
VSIN_VIN
VSIN_VDRV
VSIN_VCC
VSIN_R_FB
VSIN_FB
VSIN_VSNS-
VSIN_SS
VSIN_MODE
VSIN_ILIM
VSIN_HICCUP#
VSIN_BOOT
VSIN_PHASE
VSIN_SW
VSIN_VOS

20201005 R8478 for 2*LPDDR4x
Randy modification

VFB : 800mV

SS~1mS 600kHZ OCP~20.7A
FCCM
20201005 OCP
Randy modification

Floating : latch-off OVP/OCP/UVP
Tie to GND : Hiccup OVP/OCP/UVP

Different than Jake's schematic
CUZ current different

Vin = 12 V
Vout = 5 V
Iout = 14.2A
Fsw = 600 Khz

+V12 @ 6A
+VIN
Irms=7.05A

PVIN1
BOOT
PHASE
SW1
PGND1
VOS
C2171 1000pF C0402 50V
C2172 1000pF C0402 50V
C2173 10uF C0603 25V
C2174 10uF C0603 25V
C2175 10uF C0603 25V
C2176 10uF C0603 25V
C2177 10uF C0603 25V
C2178 10uF C0603 25V
R8473 1 R0603
C2180 25V 0.1uF C0603
L26 DCR=0.9mohm,ZPWM-6040BB-R22M,
SCOILA-7P4X6P7X4M
C2183 22uF 10V C0805
C2184 22uF 10V C0805
C2185 22uF 10V C0805
C2186 22uF 10V C0805
C2187 22uF 10V C0805
C2188 22uF 10V C0805
C2190 330uF 6.3V 20% B2(3.5*2.8*1.9);45mohm.SMD
C2233 330uF 6.3V 20% B2(3.5*2.8*1.9);45mohm.SMD

A02, 20210310 Due to height limitation for PM requirment.
Change L26 from 1211102276 to 1211X00044.

+V5A@14.2A
+V5A

A02, 20210310 Due to PM requirment for I225 and PCIe SSD support 512GB,
change +V5A (PU1) from 13.82A to 14.294A and +V3P3A (PU3) from 2.45A to 2.9A.

+V3P3A

+V5_DUAL / 1.62A-->1.914A
+V5_DUAL

Reserved for Efficiency
Irms=1.16A

PC501 22uF 10V C0603
PC502 Do Not Stuff 10V C0603
PC503 0.1uF 16V C0402

+V3P3A
PR501 10K 1% R0402
(22,31) V3P3A_PG
Ven > 1.1V
V3P3A_R_EN
(20) O_ERP_ON#
(22) V3P3A_EN
PR502 5% Do Not Stuff R0402
PR503 5% 0 R0402
PC504 Do Not Stuff 50V C0402

PU3
SY8859QWC QFN7M-1P5X1P5
IN
PG
EN
MODE
LX
FB
GND
V3P3A_LX
V3P3A_FB

PL25
1uH,DCR=24mohm,Idc=4.5Amp
SCOILA-45X41

R1
R2
PR504 47.5K 1% R0402
PR505 10.5K 1% R0402
PR506 5% 0 R0402
PC505 47pF 50V C0402
V3P3A_FB_CR_COMP
PC506 22uF 10V C0603
PC507 22uF 10V C0603
PC508 0.1uF 16V C0402
PC574 22uF 10V C0603

Vout= 0.6 x (1 + R1 / R2)

A02, 20210330 Randy modify
Add PC574 (22uF) for +V3P3A.

+V3P3A
Vout = 3.3 V
Iout = 1.8A
Fsw = 1 Mhz

+V3P3A / 1.8A
+V3P3A

+V5_DUAL
+V5_DUAL
+V5_DUAL

PR507 100K 1% R0402
PR508 100K 5% R0402
V3P3A_MODE

CCM mode=Pull high
PFM Mode=Pull low

20200924 Due to the push-pull output of U2
Remove R8571 & R8570 for 3.3V voltage divider.

(26,27) V5IN_PG
V5ALW_RESET#
U2
A
B
GND
VCC
Y
SN74LVC1G32DCK
C7 0.1uF 16V C0402

20200924 Fix PWR Down Sequence fail
(R8MB3T#/DSWPWROK/SLP_S0I#)
Remove R8569 & R8568 for saving PCB space.
Add U142 (TLV809EA46DPWR) and C2350 for monitor
S5B and sending reset# to fix pwr down issue.

U142
RESET#
MR#
PGND
VCC
GND
5,TLV809EA46DPWR,
+V5ALW
C2350 0.1uF 16V C0402

U142料料號申請中141X000011

+V3P3S

+V3P3A/ 0.5A
+V3P3A
PC26 10uF 6.3V C0402
PC27 0.1uF 6.3V C0201
PU4
VIN_1
VIN_9
VCC
EN
PG
BLEED
VOUT_7
VOUT_8
GND
NCP45520IMNTWG-H
DFN8F-2X2-1
(17,20,32) O_SLP_S3
PR25 R0201 0 5%
V3P3_EN
V3P3_DISCHARGE
PR26 5% 470 R0402
PR27 10K 1% R0201
V3P3S_PG
(33) V3P3S_PG
+V3P3S/ 0.5A
+V3P3S
PC28 10uF 6.3V C0402

A0.2

AAEON An ASUS Company

Title: POWER_+V5S_+V3P3A		
Size: A2	Document Number	Rev: A0.2_0_0
Date: Thursday, April 22, 2021		Sheet: 27 of 34

+VDDQ

+V5_DUAL/ 1.44A

+V5_DUAL

20200929 Run out of PCB space for DDR4 Memory down
Change design from DDR4 to LPDDR4x
Modify +VDDQ/+VDDQ_VPP/+VDDQ_TX for PU5/U137/U140

Irms=2.69A

C425 22uF 10V C0603
C431 22uF 10V C0603
C415 22uF 10V C0603
C434 0.1uF 25V C0402

PU5
NB685GQ-Z
QFN16F-3X3-5

VIN, OTW, BST, SW, EN1, EN2, PG, 3V3, FB, VDDQ, VTTS, VTT, AGND, PGND, MODE, VTTREF

PR28 0 5% R0603
PC29 0.22uF 50V C0603
+VDDQ_BST
+VDDQ_SW

20201005 L27 for 2*LPDDR4x
Randy modification
L27
0.68uH,DCR=11mohm,Idc=8.5A
SCOILA-4P85X4P7X2P8M

20200930 PR31
Randy modification

PR30 1M 1% R0402
PC34 220pF 50V C0402
PR31 16.9K 1% R0402 Rup
PR35 20K 1% R0402 Rdown
PR34 499 1% R0402
+VDDQ_FB

Vo=0.6*(1+Rup/Rdown)=1.1V

PC35 22uF 6.3V C0603
PC36 22uF 6.3V C0603
PC37 22uF 6.3V C0603
PC38 22uF 6.3V C0603
PC155 Do Not Stuff 6.3V C0603
PC156 22uF 6.3V C0603

Different than Jake's schematic
NL 22uF

+VDDQ_MEM
Vout = 1.1 V
Iout = 6.5 A
Fsw = 700 Khz

1.1V/ 6.5A
+VDDQ_MEM

GND_+VDDQ

+V3P3A

PR33 0 5% R0402 +VTT_EN1
VDDQ_EN2
VDDQ_PG
PR36 100K 5% R0402
PR37 5.1 1% R0402
VDDQ_3V3
PC39 1uF 16V C0402

GND_+VDDQ

VDD2 ENABLE SIGNAL GENERATION

VDDQ_VPP_PG
PR38 10K 1% R0402
VDDQ_EN2
PC42 4700pF 10% X7R C0402
(12,20,28) I_SLP_S4
PR41 100 1% R0402
VDDQ_DIS
PD1 40V 1PS79SB30 TS-SOD523

PR39 0 5% R0402
PC41 0.22uF 10V C0402
VDDQ_MODE
VDDQ_VTTREF

PR40 0 5% R0603

GND_+VDDQ

+VDDQ_VPP

For tPLT16 sequence
May change to 0201

PD2 40V 1PS79SB30 TS-SOD523
PM_SLP_S4#_D
PR44 100 1% R0402
(12,20,28) I_SLP_S4
PR45 330K 1% R0402
VPP_VR_EN
PC47 0.1uF 16V C0402

+V1P8A @ 0.5A

+V1P8A

+V3P3A

R648 10K 1% R0201
VDDQ_VPP_PG
C2243 10uF 6.3V C0402

U137
VIN_1, VIN_9, VCC, EN, PG, BLEED, GND, VOUT_7, VOUT_8
NCP45520IMNTWG-H
DFN8F-2X2-1

VPP_VR_EN
DIS_+V1.8U_MEM
R8961 470 5% R0402
C2275 10uF 6.3V C0402

PC520 0.1uF 6.3V C0201

+V1.8U_MEM @ 0.5A

+V1.8U_MEM

+VDDQ_TX

+V5_DUAL / 0.1A

+V5_DUAL

Irms=0.32A

C13 10uF 10V C0402
C2152 10uF 10V C0402

U140
VIN, EN, GND_0, GND_1, PAD, PG, SW, VOS, FB
TLV62084ADSGR

R650 10K 1% R0201
VDDQ_TX_PG (32)
VDDQ_TX_EN
SW_VDDQ_TX
L11 1uH,DCR=73mohm,Irms=1.8Amp SCOILA-2P1X2P6X1P2M
+VDDQ_LP4X_MEM
FB_VDDQ_TX

R8973 13K R0402 R1
R8970 39.2K R0402 R2

C2153 22uF 10V C0603
C400 22uF 10V C0603

+VDDQ_LP4X_MEM
Vout = 0.6 V
Iout = 0.8 A
Fsw = 2M hz

0.6V/0.8A

+VDDQ_LP4X_MEM

FSW=2MHz
Vout=VFB(0.45) X (1+R1/R2)

VDDQ_PG
R385 10K R0402
VDDQ_TX_EN
(12,20,28) I_SLP_S4
R8969 100 R0402
DIS_VDDQ_TX
D9 1PS79SB30 TS-SOD523
PC521 Do Not Stuff 16V C0402

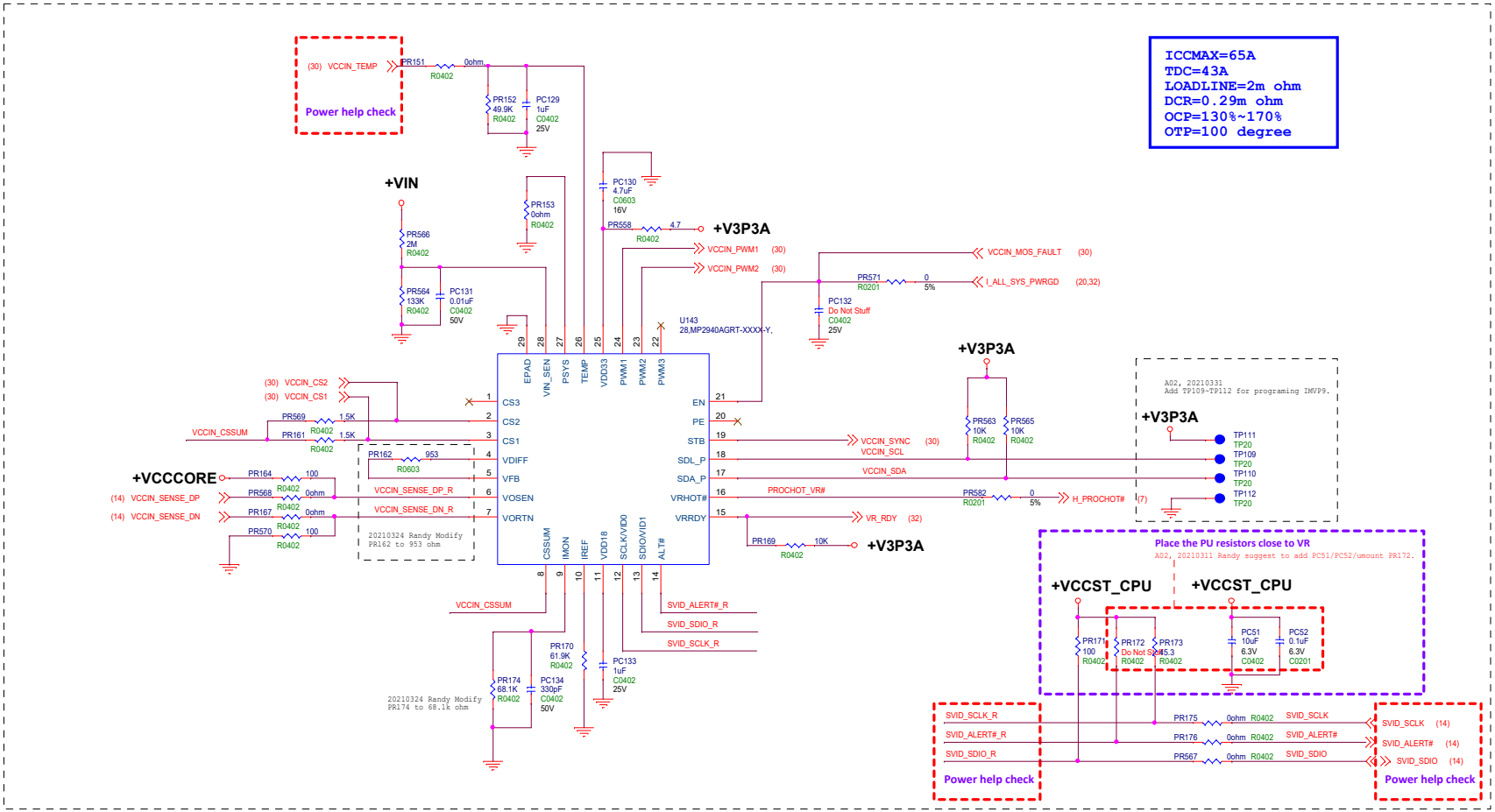
A0.2

AAEON Technology INC.

Title	PWR_+VDDQ/ +VDDQ_VPP/+VDDQ_TX	
Size: Custom	Document Number: NANOCOM-TGU	Rev: A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 28 of 34	

Tiger Lake IMVP9

A02, 20210310 Saving PCB space
CUZ PM adding more spec modification, must narrow IMVP9 circuit (+VCCCORE) to saving more PCB space.
Remove whole IMVP9 circuit to add whole New IMVP9 ciruit (PU30).



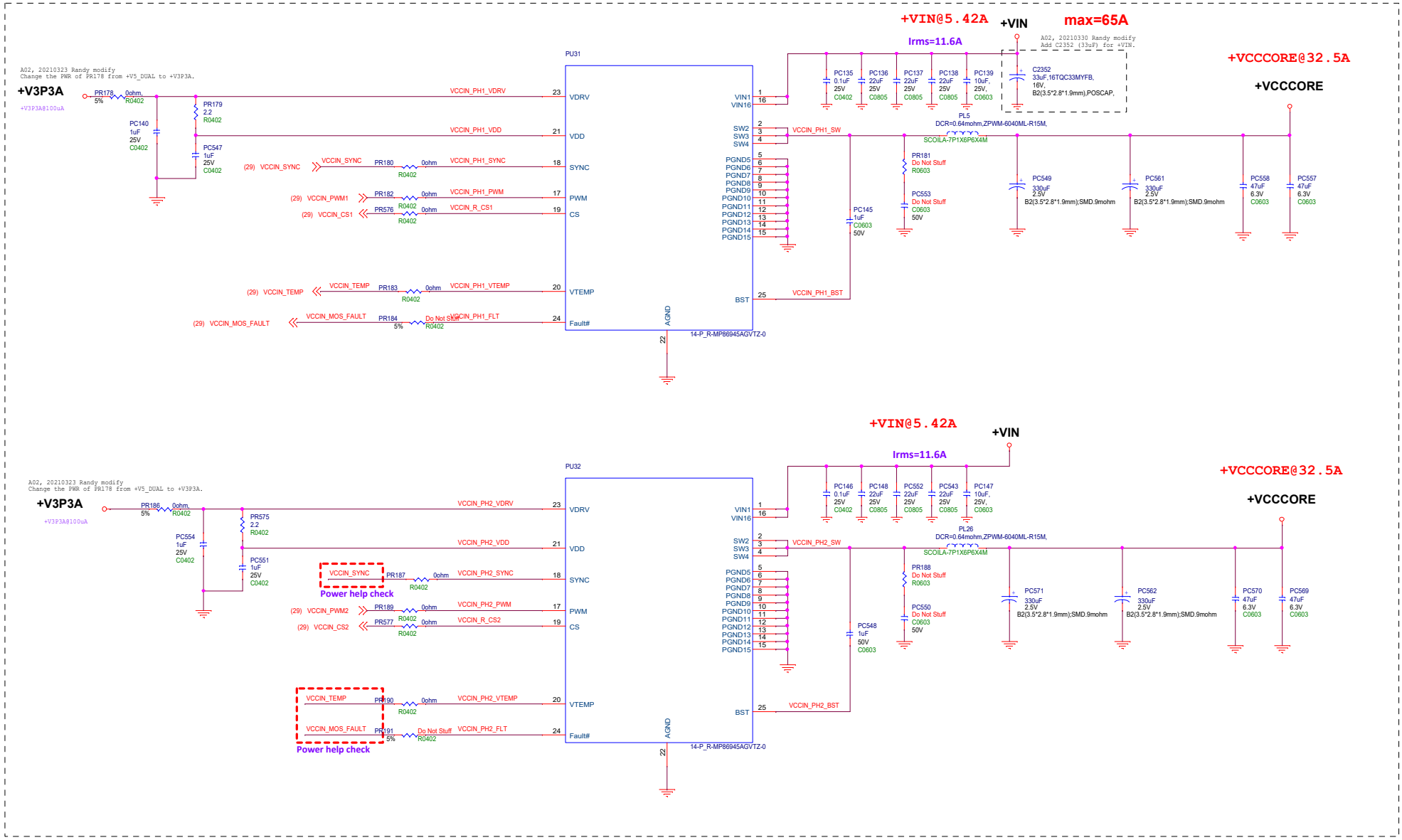
A0.2

AAEON Technology INC.

Title	PWR_IMVP9 Controller	
Size	Document Number	Rev
	Custom NANOCOM-TGU	A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 29 of 34	

+VCCCORE

A02, 20210310 Saving PCB space
CU2 PM adding more spec modification, must narrow IMVP9 circuit (+VCCCORE) to saving more PCB space.
Remove whole IMVP9 circuit to add whole New IMVP9 ciruit (PU31/PU32).



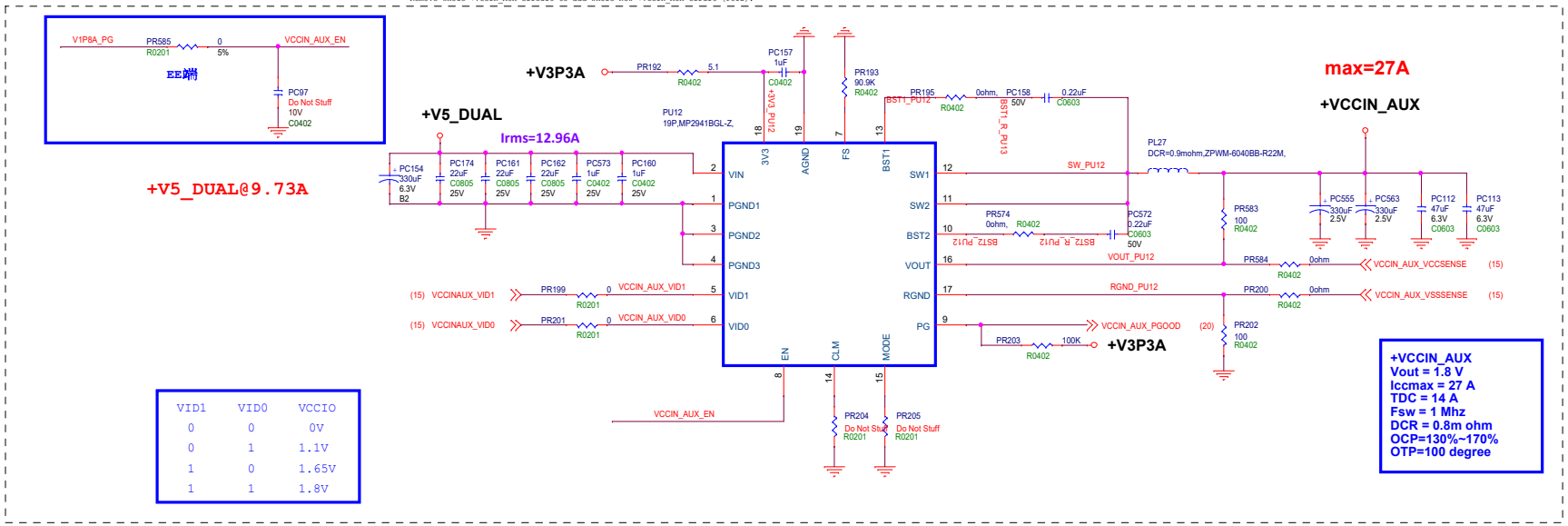
A0.2

AAEON Technology INC.

Title	PWR_+VCCCORE	
Size	Document Number	Rev
	Custom NANOCOM-TGU	A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 30 of 34	

+VCCIN_AUX

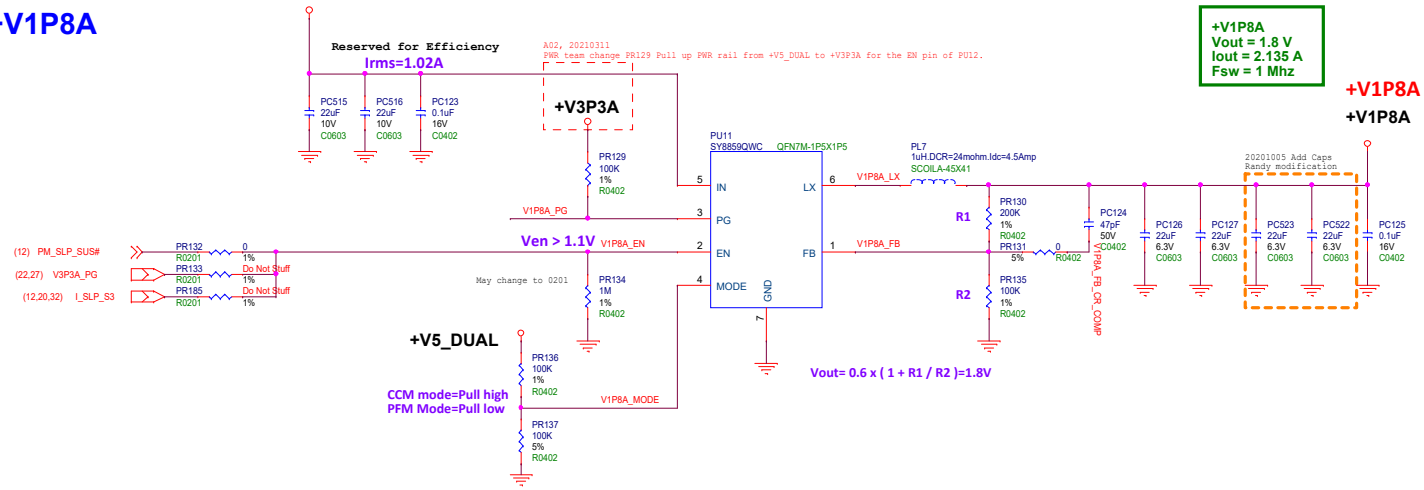
A02, 20210310 Saving PCB space
CUZ PM adding more spec modification, must narrow IMVP9 circuit (+VCCIN_AUX) to saving more PCB space.
Remove whole +VCCIN_AUX circuit to add whole New +VCCIN_AUX ciruit (PU12).



VID1	VID0	VCCIO
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

+V1P8A

+V5_DUAL / 0.8A
+V5_DUAL



A0.2

AAEON Technology INC.

Title: PWR_+VCCIN_AUX/+V1P8A

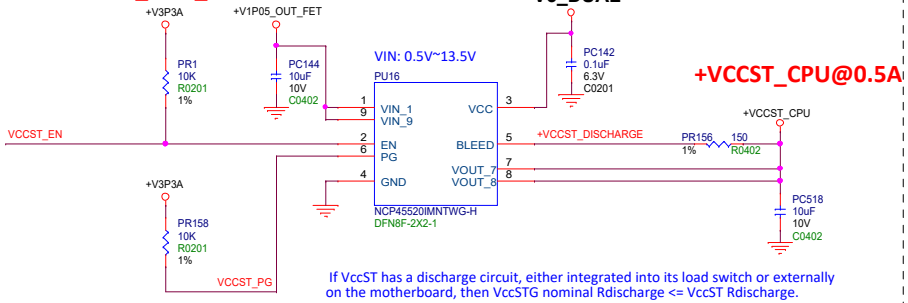
Size	Document Number	Rev
Custom	NANOCOM-TGU	A0.2_0_0

Date: Thursday, April 22, 2021 | Sheet 31 of 34

+VCCST_CPU

A02, 20210303
Change PC144 from 10uF to 0.1uF for saving PCB sapce.
Based on Sighting #632245, change EN of PU16 to Pull high PR1 to +V3P3A.
Change PC144 & PC518 from 0.1uF to 10uF.

+V1P05_OUT_FET@ 0.5A

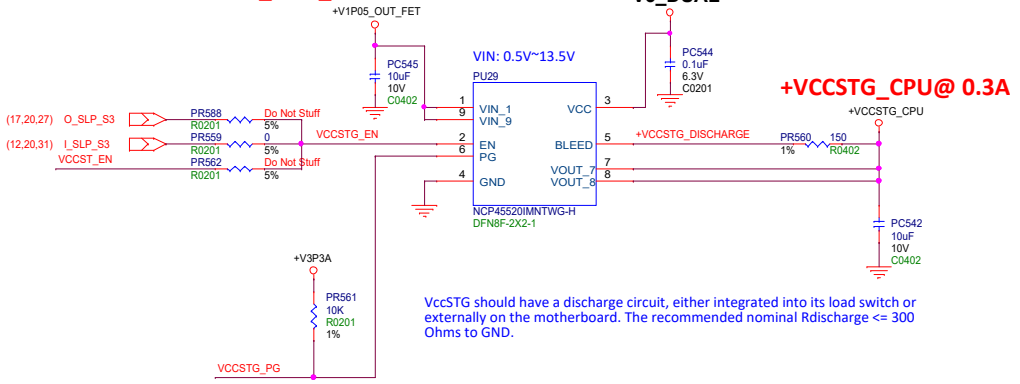


If VccST has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal Rdischarge <= VccST Rdischarge.

+VCCSTG_CPU

A02, 20210303 Split VCCSTG due to Sighting #632245
Add PU29 circuit. Enable connect to SLP_S3# based on IPS 00557861 replied.
Change PC545 & PC542 from 0.1uF to 10uF.

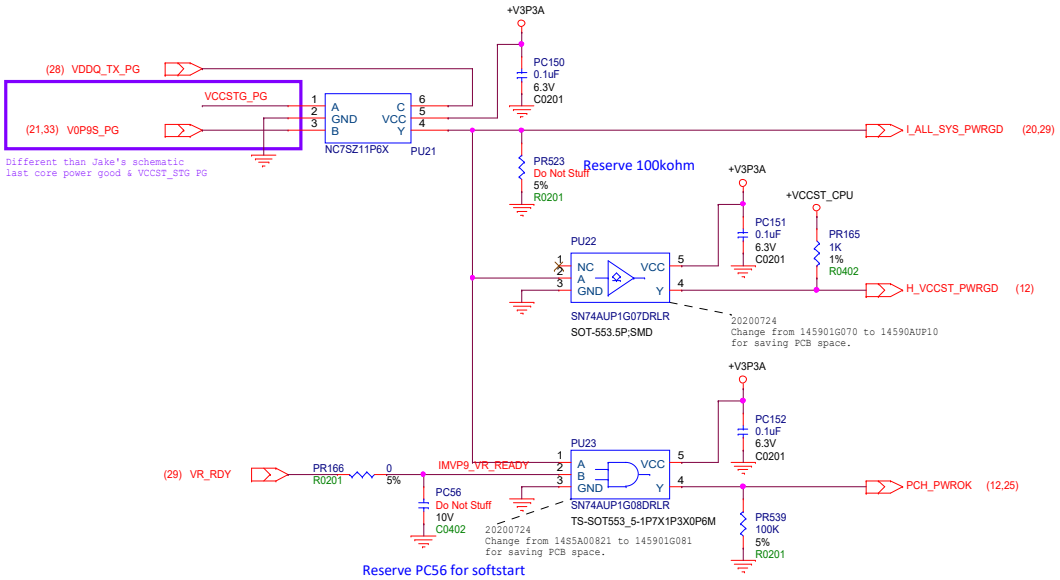
+V1P05_OUT_FET@ 0.3A



VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal Rdischarge <= 300 Ohms to GND.

Nanocom-TGU don't support C10 Deep Sleep mode.

A02, 20210303 Split VCCSTG due to Sighting #632245
and based on IPS 00557861 replied.
Remove PU14/PU15/PQ3/PU20/PU24 circuit for saving PCB space.



Reserve PC56 for softstart

A0.2

AAEON Technology INC.

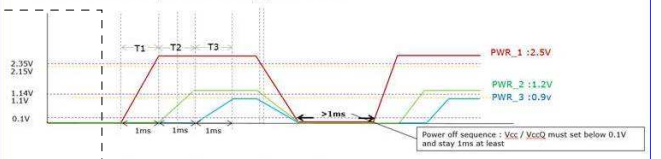
Title	PWR_+VCCST_CPU/+VCCSTG_CPU	
Size	Document Number	Rev
	NANOCOM-TGU	A0.2_0_0
Date: Thursday, April 22, 2021	Sheet 32 of 34	

PCIe SSD 3* PWR supply

A02, 20210310 Saving PCB space
CUI PM adding more spec modification, must narrow 3 PCIe SSD PWR (2.5V/1.2V/0.9V) to saving more PCB space.
Remove whole PCIe SSD PWR circuit to add whole New 3 * Buck ciruits (PU33/PU34/PU35).

1. Power domain:

1.4 Power on sequence timing parameter



Parameter	Min	Nom	Max	Unit
PWR_1 Ready(T1)	0.8	1	1.2	mS
PWR_2 Ready (T2)	0.8	1	1.2	mS
PWR_3 Ready(T3)	0.8	1	1.2	mS
PWR_2 to PWR_3	0.9	1	1.1	mS
PWR_1 to PWR_2	0.9	1	1.1	mS

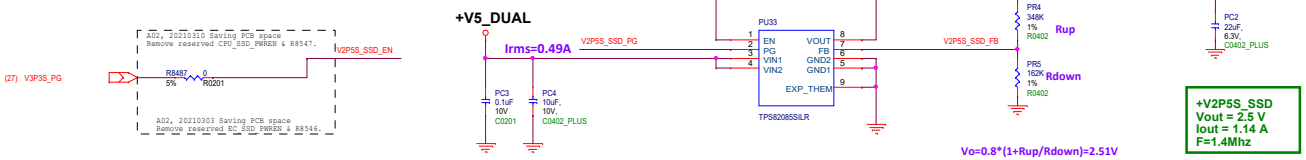
+V2P5S_SSD

20201029 A02 Vendor update PWR consumption spec
20210303 A02 Support 512GB for PM spec update
Change Max. current from 0.588 to 1.14A.

A02, 20210312 Change PWR source from +V3P3A to +V5_DUALfor layout routing.

+V5_DUAL@0.57A

+V2P5S_SSD@1.14A



Vendor update PWR consumption spec
Support 512GB for PM spec update
+V2P5S_SSD change Max. current from 0.588 to 0.747A.
+V1P2S_SSD change Max. current from 0.588 to 1.14A.
+V0P9S_SSD change Max. current from 0.664 to 0.996A

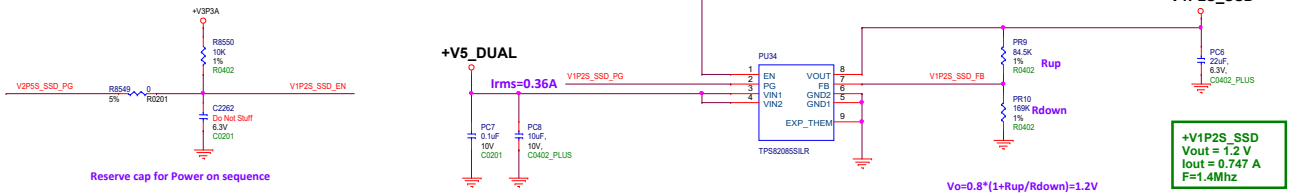
+V1P2S_SSD

20201029 A02 Vendor update PWR consumption spec
20210303 A02 Support 512GB for PM spec update
Change Max. current from 0.588 to 0.747A.

A02, 20210312 Change PWR source from +V3P3A to +V5_DUALfor layout routing.

+V5_DUAL@0.18A

+V1P2S_SSD@0.747A

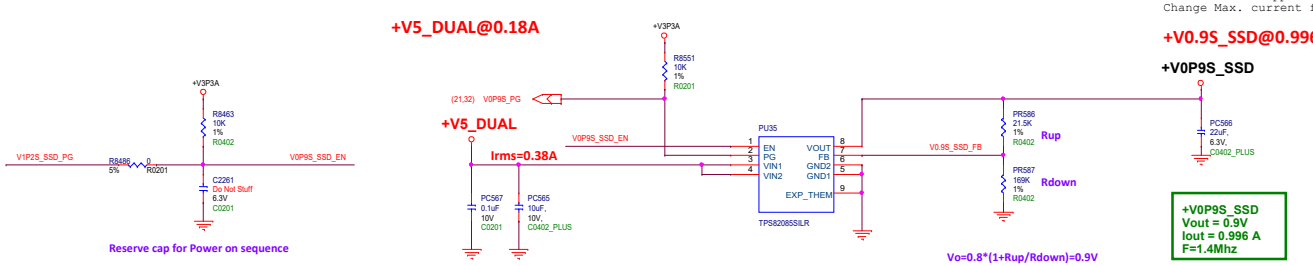


+V0P9S_SSD

20201029 A02 Vendor update PWR consumption spec
20210303 A02 Support 512GB for PM spec update
Change Max. current from 0.664 to 0.996A

+V5_DUAL@0.18A

+V0.9S_SSD@0.996A



A0.2

AAEON An ASUS Company

Title: PWR_+V2P5S/+V1P2S/+V0P9S_SSD		
Size: A2	Document Number	Rev: A0.2_0_0
Date: Thursday, April 22, 2021		Sheet: 33 of 34

NANOCOM-TGU Revision History

NANOCOM-TGU A0.2_0_0 PCB: 1907NATU01 Date: 2021/03/10

01. Project code: E210103
02. Model name: NANOCOM-TGU
03. Model revision: A0.2_0_0
04. 96-Level: 9697NATU-
05. PCB 料號: 1907NATU01
06. PCB 厚度: 2.0 mm
07. PCB 層數: 16 Layer
08. 連板數量: 2 pcs
09. 2階HDI

分BOM
1. 9697NATU01-D, (TF)ASS'Y.NANOCOM-TGU.Rev.A0.1_0_0.Intel Tiger Lake UP3 i3-1115G4E.LPDDR4x 16GB.PCIe SSD 64GB
2. 9697NATU02-D, (TF)ASS'Y.NANOCOM-TGU.Rev.A0.1_0_0.Intel Tiger Lake UP3 i3-1115GRE.LPDDR4x 16GB.PCIe SSD 64GB
3. 9697NATU03-D, (TF)ASS'Y.NANOCOM-TGU.Rev.A0.1_0_0.Intel Tiger Lake UP3 i5-1145GRE.LPDDR4x 16GB.PCIe SSD 64GB
4. 9697NATU04-D, (TF)ASS'Y.NANOCOM-TGU.Rev.A0.1_0_0.Intel Tiger Lake UP3 I7-1185G7E.LPDDR4x 16GB_PCIe SSD 64GB
5. 9697NATU05-D, (TF)ASS'Y.NANOCOM-TGU.Rev.A0.1_0_0.Intel Tiger Lake UP3 I7-1185GRE.LPDDR4x 16GB_PCIe SSD 64GB

Revision History Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.	Bug ID
1	10	38.4MHz	03/10	HW	XTAL vendor suggestion and verification.	Change C18/C19 from 15pF to 10pF.	A02	
2	12	SLP_S0#	03/03	HW	PDG require pull-up resistor on SLP_S0# if a device is monitoring SLP_S0# before RSMRST# de-assertion	Modify R186 from pull down to pull high for SLP_S0# .	A02	
3	32, 12	Split VCCST and VCCSTG PWR	03/03	HW	Due to Intel Sighting Report #632245, the System May Fail to Exit S3. Enable VCCST with +V3P3A pull high and VCCSTG with SLP_S3#.	Remove PU14/PU15/PQ3/PU20/PU24 circuit for saving PCB space and based on IPS 00557861 replied.. Remove R183 and directly short net. Move PR160 to CPU side. Add PC546 to CPU side cuz load SW side is no enough PCB space. Add PU29 circuit. VCCSTG EN pin connect to SLP_S3# based on IPS 00557861 replied. Based on Sighting #632245, change EN of PU16 to Pull high PR1 to +V3P3A. Change PC144 from 10uF to 0.1uF.	A02	
4	20	EC PWR	02/22	HW	Due to PM spec modification from IT5571 to IT8528.	Remove LDO (U9) & connect to FB83.	A02	
5	21	EC PWR	02/22	HW	Due to PM spec modification from IT5571 to IT8528.	Remove R2909 and R2910 & connect to +V3P3A.	A02	
6	27	Switch 5VSB & 5Vcore for +V5_DUAL	02/26	HW	CUZ the PG of +V5A discharge slowly, casue MOS switch mismatch and let +V5_DUAL turn off, then turn on.	Change the PG of PWR from +V5A to V5IN_VCC (internal LDO PWR).	A02	
7	27	Fix +V5A enable & Choke modification	02/26	HW	CUZ the voltage divider is wrong for +V5A EN, FAE suggest the correct value. Due to the height of choke for PM reqirment.	Change PR524 from 26.1kohm to 120kohm and change PR525 from 10kohm to 22kohm. Change L26 from 1211102276 to 1211X00044.	A02	
8	21, 07, 08	Remove TPM	02/26	HW	Remove TPM ciruit for PM requirement (Add intel I225).	Remove SPI0_TPM_CS2# (DF39), the TPM net of Q119, R8977, R8978, R8974, R8976, R8979~R8982, R8975, C2332~C2335, U151 and TPM_PIRQ# (DU19).	A02	
9	21, 07	Remove Sharing Flash	02/26	HW	Due to SW EE unable supporting sharing SPI Flash design, remove EC and BIOS sharing SPI Flash design. And EC and BIOS connect their own SPI Flash.	Remove R2921and R8499~R8501. Change R2917, R8507, R8508, R8536,R8537 from 0 to 62 ohm ±5% based on 607872_TGL_UP3_PDG_Rev2p2. Change R8502, R8504, R8505 from 15 to 0ohm. Change R8503, R8506 from 49.9 to 0ohm. Add R8985 for Jumper wire. Remove R518 (VR_RDY) cuz no use.	A02	
10	20	Add SPI ROM	03/02	HW	Due to PM spec modification from IT5571 to IT8528.	Add SPI ROM circuit Q7A/Q9/Q120/U11. Add TP89~TP91 for progamming code.	A02	
11	20, 33, 12	Change EC	03/02	HW	Due to PM spec modification from IT5571 to IT8528.	Remove reserved EC_SSD_PWREN & R8546/R8548. Remove reserved SX_EXIT_HOLDOFF#(M8) & R2912. Remove reserved EC PM_SLP_S0#(N12) & R177. Change PWR connection from +V3.3A_RTC_EC to +VCC_RTC for reduce 2 diodes. Comfirmed with Elf that follow COM-TGU6 pin definition. No use EC_A_PROCHOT# for COM-TGU6, so NC N7. Remove reserved PCH_R_THRMTRIP#(C1). Due to No USE reserved function, remove R2916 (VRALERT#) and TP64(GPJ7). Change from TP63 to R361 PD for IT8528. Change U33 from IT5571 (146X000003) to IT8528 (14E0085283). For details, please refer to page 20 for modification.	A02	
12	23, 9, 7	Change to I225	03/02 ~>4/16	HW	Due to PM spec modification from I219 to I225.	Change U8 from 1440219LM0 (I219) to 144X00002e (I225) including whole related circuit. Change R46/R47 from 1k(0201) to 499ohm (0402) for I225. Change C2346 & C2347 from 10pF to 20pF based on Intel CRB. LAN_DISABLE#_R remove PD 10kohm for saving PCB space. LAN_SDP0 reserve TP96 & Remove reserved PU 10k & PD 10k for saving PCB space. Remove PM_LAN1PHY_ENABLE (DT41) cuz this give to I219 use. Add C2351 for U8 pin decoupling. Change XTAL(Y4) back to 12310025A5 cuz 12310025AF doesn't suggest by purchaser and lead time 1 year/no stock in Aaeon.	A02	
13	27	Fix PWR Down Sequecne fail	03/05	HW	Due to RSMRST# / DSW_PWROK / SLP_SUS# PWR Down Sequence fail, RSMRST# & DSW_PWROK must fall faster than +V3P3A and SLP_SUS# must fall faster than +V1P8A.	Remove R8569 & R8568 for saving PCB space.Add U142 (TLV809EA46DPWR) and C2350 for monitor SSB and sending reset# to fix pwr down issue. 20200924 Due to the push-pull output of U2 Remove R8571 & R8570 for 3.3V voltage divider.	A02	
14	17, 20, 29, 30	PM update spec	03/10	PM	CUZ PM spec modification add I225 and IT8528, must narrow IMVP9 circuit (+VCCCORE / +VCCIN_AUX) to saving more PCB space.	Remove whole IMVP9 circuit to add whole New IMVP9 ciruit (PU30/PU31/ PU32). Remove whole +VCCIN_AUX circuit to add whole New +VCCIN_AUX ciruit (PU12). Move R2897 and R2898 to B2B (CN57) side. Change Net Name from EC_SMBCLK_R/EC_SMBDATA_R to I2C_R_CLK & I2C_R_DAT. Add TP109~TP112 for programing IMVP9.	A02	
15	33, 8	PM update spec	03/10	PM	CUZ PM spec modification add I225 and IT8528, must narrow 3 PCIe SSD PWR (2.5V/1.2V/0.9V) to saving more PCB space. Support 512GB for PM spec update & vendor update PWR consumption spec to design PWR.	Remove whole 3 * PCIe SSD PWR circuits to add whole New 3 * Buck ciruits (PU33/PU34/PU35). Remove reserved CPU_SSD_PWREN (DV25) & R8547. Due to spec support 512GB, +V2P5S_SSD change Max. current from 0.588 to 0.747A. +V1P2S_SSD change Max. current from 0.588 to 1.14A. +V0P9S_SSD change Max. current from 0.664 to 0.996A.	A02	
16	27	PM update spec	03/02	HW	Due to PM requirment for I225 and PCIe SSD support 512GB.	Change +V5A (PU1) from 13.82A to 14.294A and +V3P3A (PU3) from 2.45A to 2.9A.	A02	
17	31	PWR PG Modify	03/11	HW	PWR team change Pull up PWR rail from +V5_DUAL to +V3P3A for the EN pin of PU12.	Change PR129 Pull up PWR rail from +V5_DUAL to +V3P3A.	A02	
18	7, 5, 10	Saving PCB space	03/16	HW	Due to PCB limitation, remove reserved parts. And change parts size.	Remove TP4 (DK13) / TP1 (DK23)/C106/U16. Change PR533/PR534 from 1050510024 to 105B501039 (0201). Remove U16 SPI Level-Shift for saving PCB space.	A02	
19	20	Routing	03/16	HW	Due to PCB space limitation, remove SPI Isolation circuit.	Remove SPI Isolation (Q7/Q9/Q120 circuit) for layout routing.	A02	
20	12	SLP_S5#	03/17	HW	Based on PDG suggestion	Mount R2911.	A02	
21	23	LAN WAKE	03/19	HW	TGU only support I219 LAN WAKE from 576591-tgl-lp-pch-eds-vol1-rev2p1.	Connect R9012 to PCIe WAKE & Reserve R8990 for LAN WAKE.	A02	
22	30, 27	PWR modify	3/23	HW	Randy Modify	Change the PWR of PR178 & PR186 from +V5_DUAL to +V3P3A. Add PC574 (22uF) for +V3P3A. Add C2352 (33uF) for +VIN. Change PR162 to (105A595303) 953 ohm & change PR174 to (1050568124) 68.1K ohm for IMVP9.	A02	
23	06	Unuse DDR	3/24	HW	Follow PDG & CRB for Unused DDR signals	Connect CPU1.AU53 (ALERT) to GND at CPU side. Follow CRB and Remove no use TP for (CPU1.AU49).	A02	
24	18, 19, 13	Saving PCB space	4/8	HW	Saving PCB space for DDR routing & follow PDG about the caps amount.	Remove C2302/C2293/C2282/C2289 for +VDDQ_MEM. Remove C2304/C2295/C2280/C2290 for +VDDQ_LP4X_MEM. Remove C2301/C2300/C2278/C2285 for +V1.8U_MEM. Remove all BPM nets and R203 (CPU1.Y3) & R204 (CPU1.M4) & R205 (CPU1.AB4) & R206 (CPU1.Y2) .	A02	
25	08	ME	4/6	HW	Due to detecting ME version problem and CPU1.DT37 internal low level problem.	Change R115 from pull high 1k ohm to pull down 1k ohm.	A02	
26	07	SMBUS	4/6	HW	Jeff D. suggestion for SMbus Drving issue	Remove Q5 and change R105 & R108 to 0ohm (0201) for SMB_DATA/SMB_CLK.	A02	

A0.2

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Date: Friday, April 16, 2021 | Sheet 34 of 34