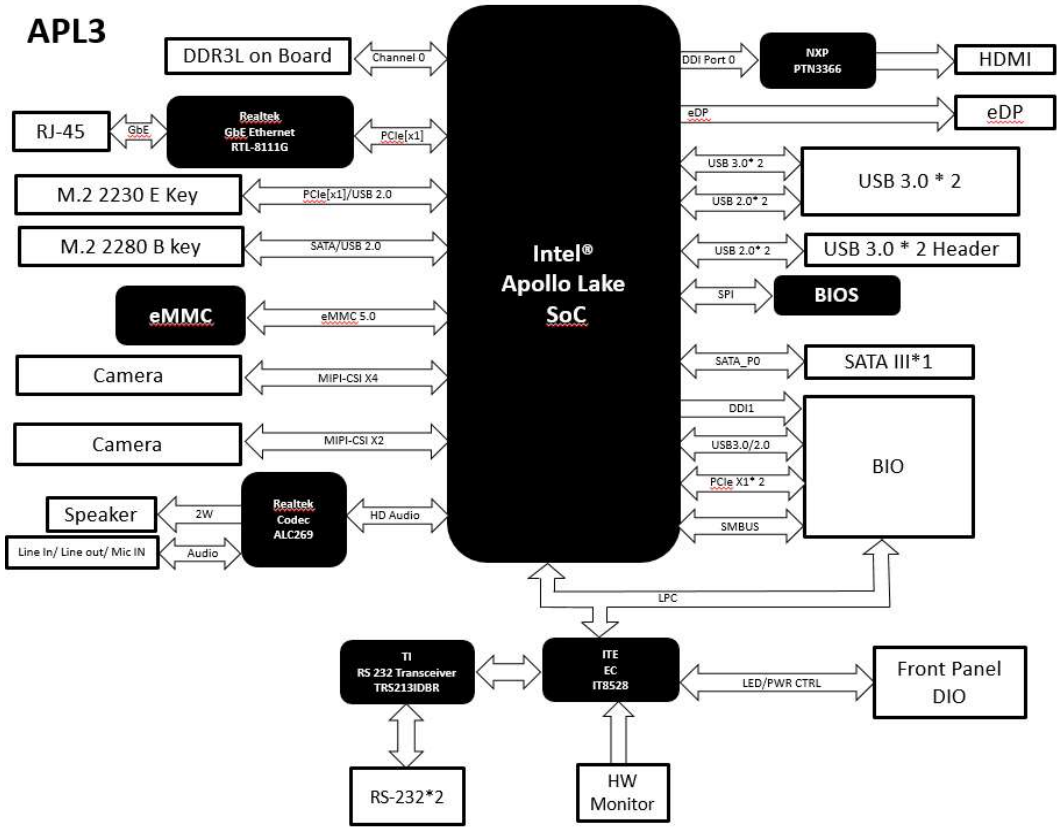
PICO-APL3 Rev.A1.0_0_0

Apollo Lake SoC Platform Cross Compatibility



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Project Number : E16XXXX

Production Line : Sub.EPI.AA2M

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SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	
GPIO_1	1.8V	20K PD/I	
GPIO_2	1.8V	20K PD/I	
GPIO_3	1.8V	20K PD/I	
GPIO_4	1.8V	20K PD/I	
GPIO_5	1.8V	20K PD/I	
GPIO_6	1.8V	20K PD/I	
GPIO_7	1.8V	20K PD/I	
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	
GPIO_15	1.8V	20K PD/I	
GPIO_16	1.8V	20K PD/I	GPIO_BTN#
GPIO_17	1.8V	20K PD/I	
GPIO_18	1.8V	20K PD/I	
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GPI[0]
GPIO_23	1.8V	20K PD/I	
GPIO_24	1.8V	20K PD/I	
GPIO_25	1.8V	20K PD/I	
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/IO	
GPIO_217	1.8V	20K PD/IO	
GPIO_218	1.8V	20K PD/IO	
GPIO_219	1.8V	20K PD/IO/OP	EMMC0_RST_N

PCB STACK :

Impedence 50ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : GND
- Layer 5 : Signal
- Layer 6 : VCC
- Layer 7 : Signal
- Layer 4 : Signal
- Layer 9 : GND
- Layer 10 : Solder

The Mapping Table For Super E/C IT8528 GPIOs :

Name	PIN No.	5VT	Type	Description & setting	Name	PIN No.	5VT	Type	Description & setting
GPIO[A0]	M5				GPIO[F0]	A11			GPI0
GPIO[A1]	N5				GPIO[F1]	B11			GPI1
GPIO[A2]	M6				GPIO[F2]	A10			DTRA#
GPIO[A3]	N6			FAN_PWM1	GPIO[F3]	B10			RTSA#
GPIO[A4]	K6			BRD_ID0	GPIO[F4]	D9			
GPIO[A5]	J6			BRD_ID1	GPIO[F5]	B9			EC_MUTE#
GPIO[A6]	M7			BRD_ID2	GPIO[F6]	B1			SMB_CLK_BIO
GPIO[A7]	K7			RTSB#	GPIO[F7]	C1			SMB_DAT_BIO
GPIO[B0]	A4			RXA#	GPIO[G0]	E6			
GPIO[B1]	A3			TXA#	GPIO[G1]	A5			DTRB#
GPIO[B2]	D2				GPIO[G2]	E7			
GPIO[B3]	B4			SMB_CLK_A	GPIO[G6]	D6			DSRA#
GPIO[B4]	A2			SMB_DATA_A	GPIO[H0]	D8			EC_RSMRST#(Reseved)
GPIO[B5]	F1			PMIC_ON	GPIO[H1]	E8			RXB#
GPIO[B6]	H4			WDT_RST#	GPIO[H2]	D7			TXB#
GPIO[B7]	A1			SYS_RESET#	GPIO[H3]	A9			PCH_PWROK(Reseved)
GPIO[C0]	D1				GPIO[H4]	B8			BIO-GPIO-R(Reserved)
GPIO[C1]	B3				GPIO[H5]	A8			
GPIO[C2]	B2				GPIO[H6]	B7			
GPIO[C3]	K13				GPIO[I0]	G10			TH1_CPU
GPIO[C4]	C2			EC_WAKE0#	GPIO[I1]	G13			TH2_SYS
GPIO[C5]	J10				GPIO[I2]	G12			VCORE_SEN
GPIO[C6]	E1			LAN1_EN	GPIO[I3]	F9			V5ALW_SEN
GPIO[C7]	M2			PM_PWRBTN#_3P3	GPIO[I4]	F13			VDDR3L_SEN
GPIO[D0]	N1			PM_SLP_S3#_3P3	GPIO[I5]	F10			DCDB#
GPIO[D1]	N3			M_SLP_S4#_3P3	GPIO[I6]	F12			DSRB#
GPIO[D2]	M4			LPC_RST#	GPIO[I7]	E13			CTSB#
GPIO[D3]	N4			EC_SCI#	GPIO[J0]	E12			
GPIO[D4]	L2			EC_SMI#	GPIO[J1]	D13			ATX_DIPSW
GPIO[D5]	N7			CTSA#	GPIO[J2]	D12			
GPIO[D6]	M11			FAN_TACH1	GPIO[J3]	C13			ADM213_EN
GPIO[D7]	M12				GPIO[J4]	B13			DCDA#
GPIO[E0]	N2			GPO0	GPIO[J5]	B13			RIA#
GPIO[E1]	A13			GPO1	GPIO[J6]	F2			
GPIO[E2]	A12			W_DISABLE2#	GPIO[J7]	G1			
GPIO[E3]	B12			W_DISABLE1#					
GPIO[E4]	E2			EXT_PWRBTN#					
GPIO[E5]	N8			RTSB#					
GPIO[E6]	M1			EN_USB					
GPIO[E7]	M3			PS_ON#					

GA20/ECSCI/ECSMI/KBRST# pay attention for leak current DO NOT place any pull up resistor on G0,G2,G6 (Reserved for Hardware strap
(2) Open-drain output pin should be pulled.
(1) Each input pin should be driven or pulled.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float
the GPIO input.

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Title: System Settings

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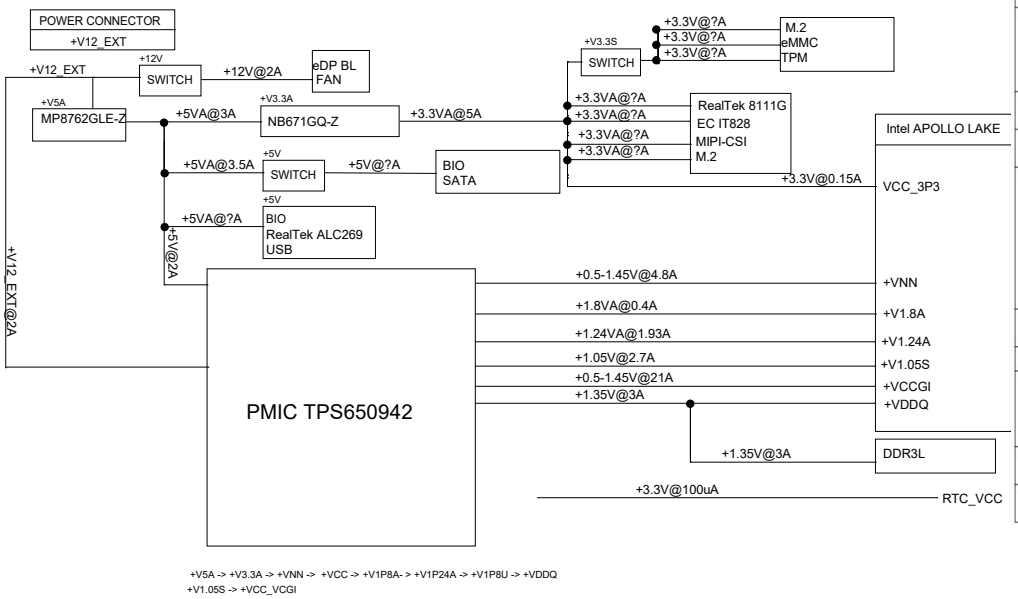

+V5A -> +V3.3A -> +VNN -> +VCC -> +V1P8A- > +V1P24A -> +V1P8U -> +VDDQ
+V1.05S -> +VCC_VCGI

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Iccmax (A)
VCC_VCGI	0.45~1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	21
VNN	0.45~1.3	+/-50mV	4.8
VCC_V1P05	1.05	+/-5%	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	1.3
VCC_V1P24_A	1.24	+/-5%	TBD
VCC_V1P8V_A	1.8	+/-5%	0.4
VDDQ	1.35	+/-5%	2.8 (excluding DRAM)
	1.24	+/-5%	
VCC_3P3V_A	3.3	+/-5%	0.15
VCC_RTC_3P3V	2~3.47	N/A	TBD

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Title: Power Tree

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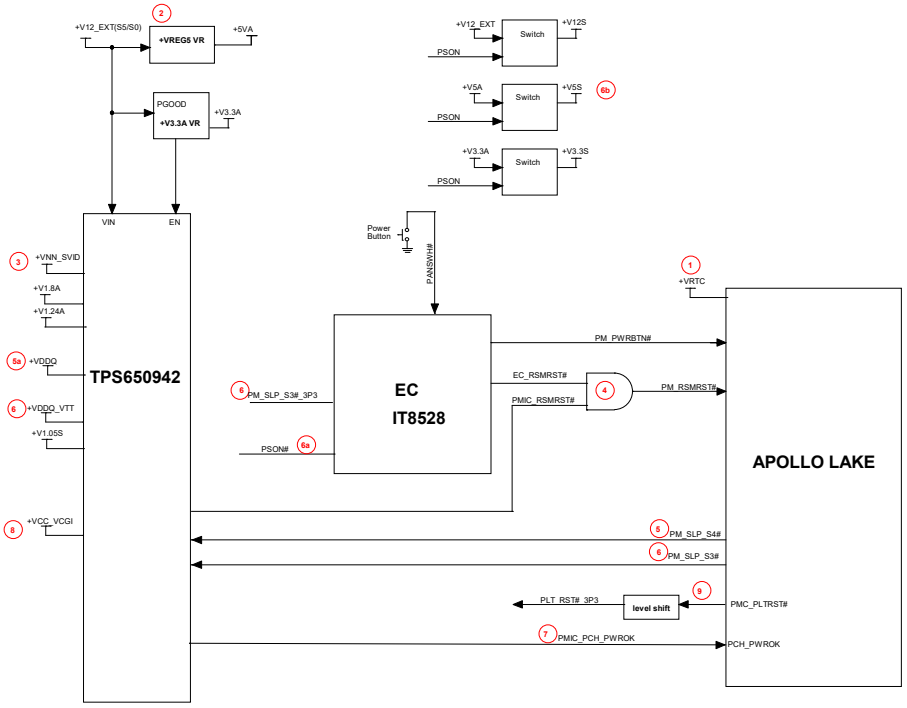
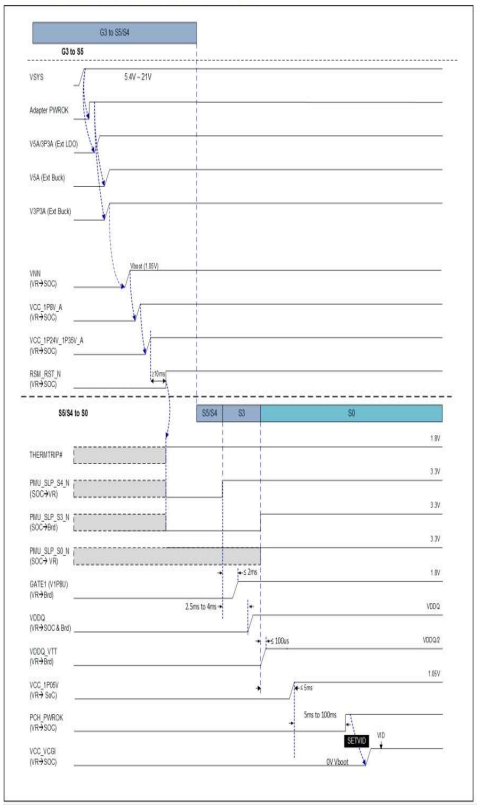


Power-Up Sequencing (G3 to S0)—Adapter



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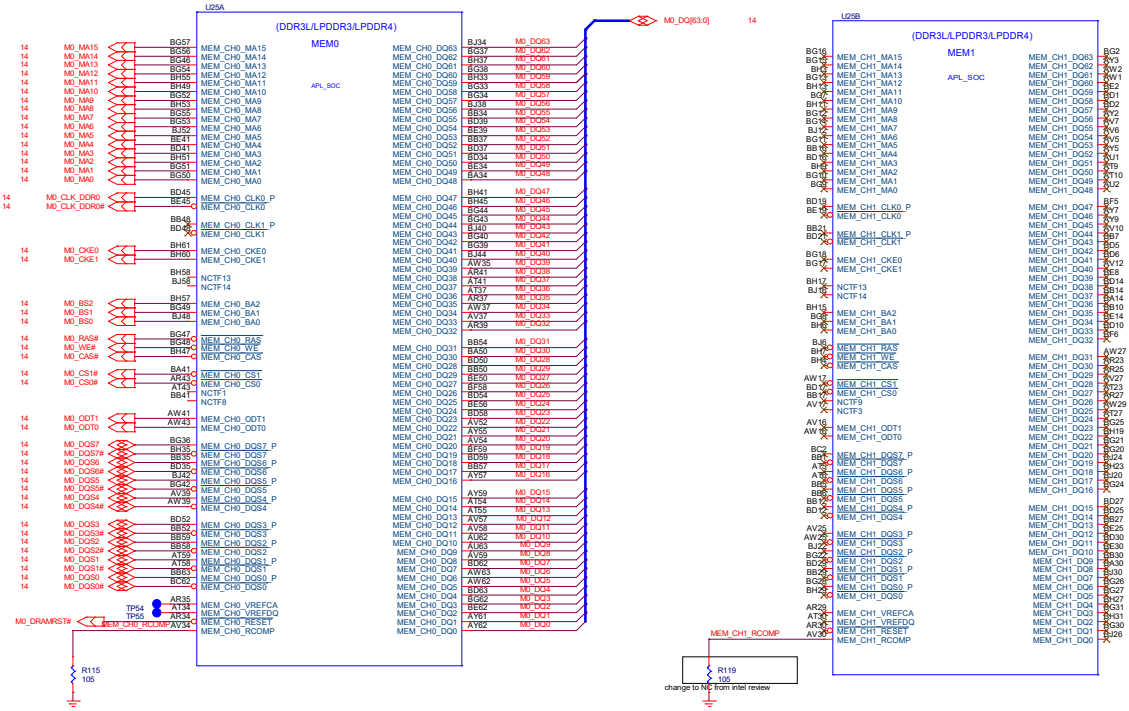

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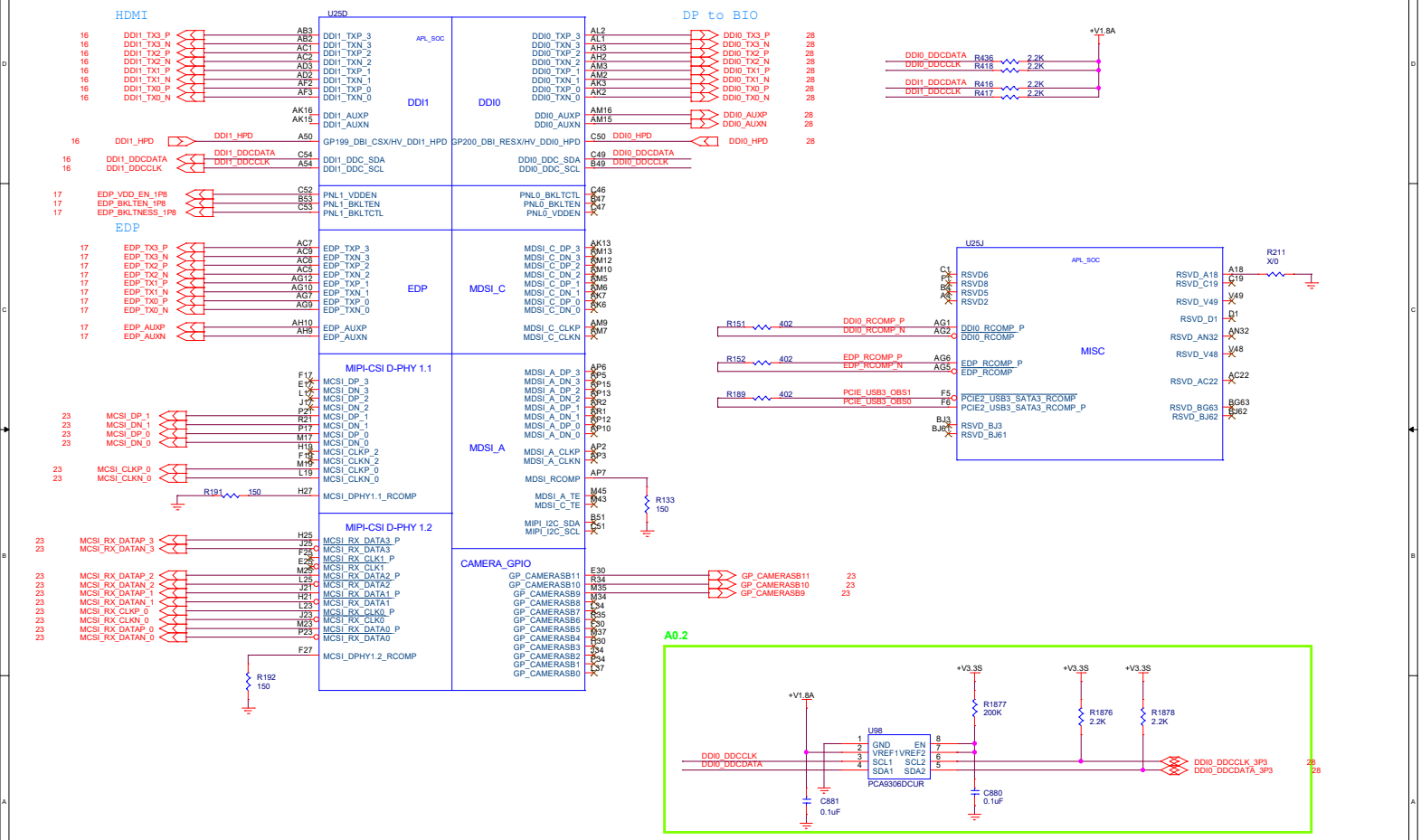

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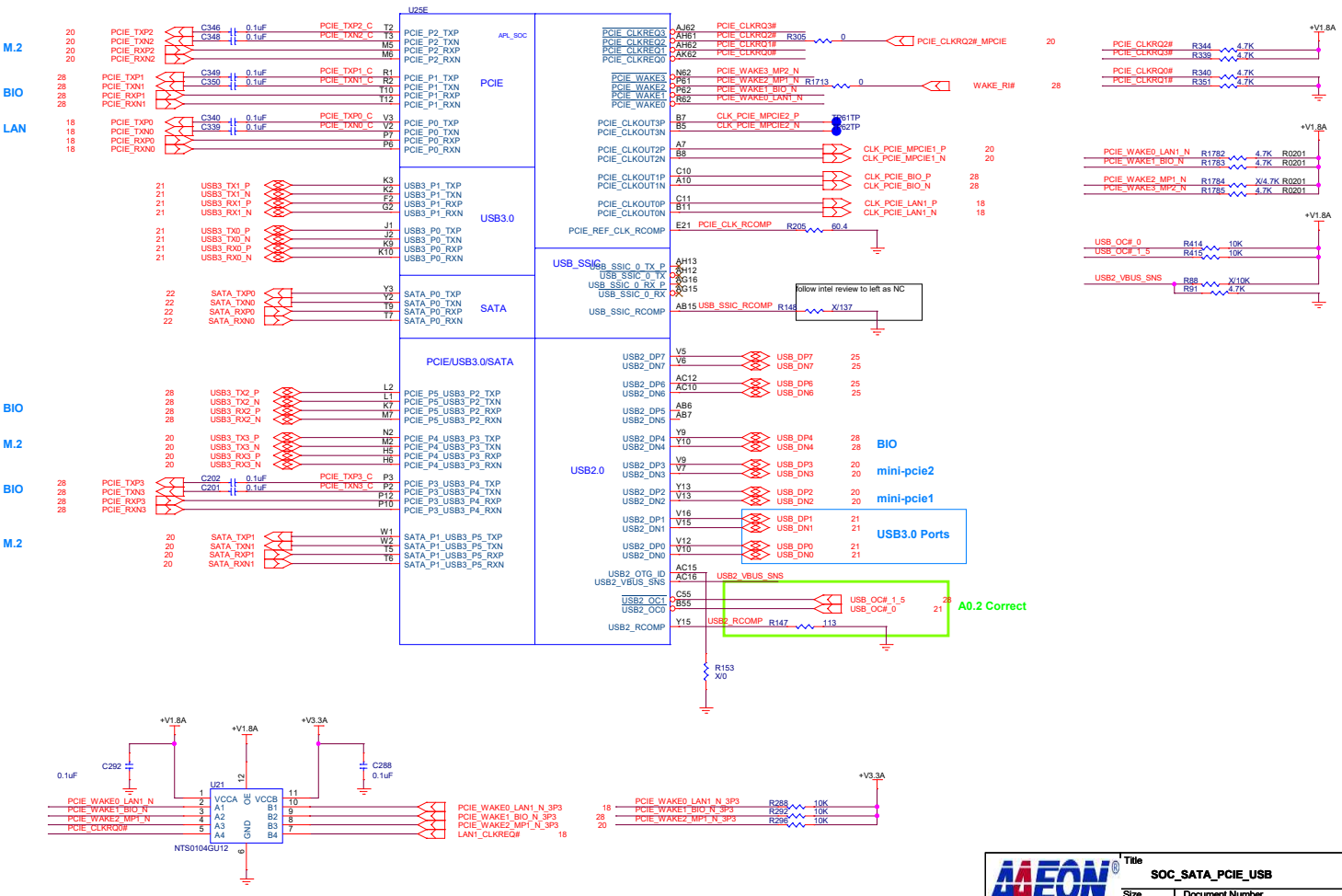

Title: SOC_SATA_PCIE_USB			
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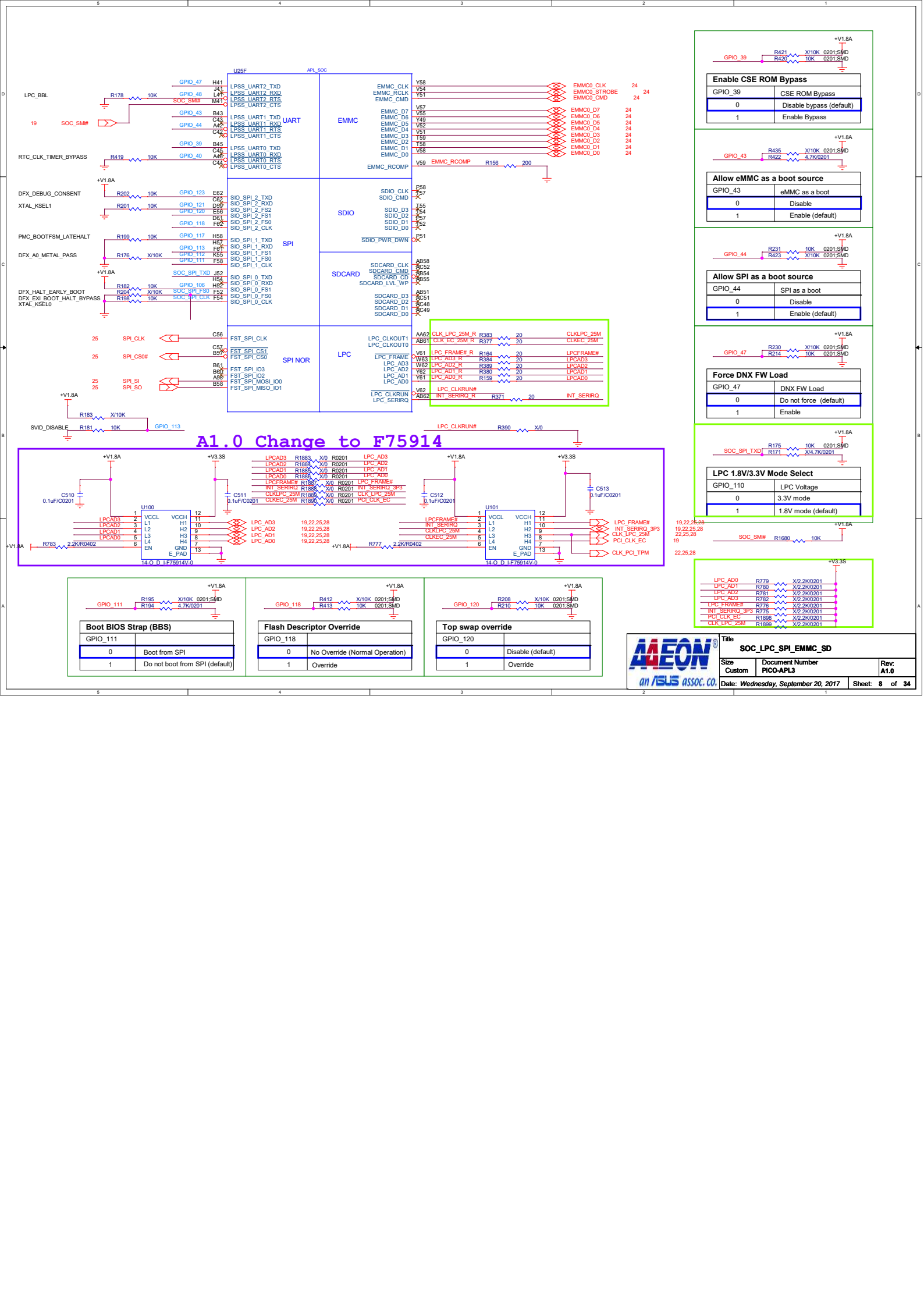
U25F
APL_SOC
UART
EMMC
SPI
SDIO
SDCARD
SPI NOR
LPC
LPC_BBL
RTC_CLK_TIMER_BYPASS
DFX_DEBUG_CONSENT
XTAL_KSEL1
PMC_BOOTFSM_LATEHALT
DFX_A0_METAL_PASS
DFX_HALT_EARLY_BOOT
DFX_EXI_BOOT_HALT_BYPASS
XTAL_KSEL0
SVID_DISABLE
A1.0 Change to F75914
U100
U101
14-O_D_I-F75914V-0
Enable CSE ROM Bypass
GPIO_39 | CSE ROM Bypass
0 | Disable bypass (default)
1 | Enable Bypass
Allow eMMC as a boot source
GPIO_43 | eMMC as a boot
0 | Disable
1 | Enable (default)
Allow SPI as a boot source
GPIO_44 | SPI as a boot
0 | Disable
1 | Enable (default)
Force DNX FW Load
GPIO_47 | DNX FW Load
0 | Do not force (default)
1 | Enable
LPC 1.8V/3.3V Mode Select
GPIO_110 | LPC Voltage
0 | 3.3V mode
1 | 1.8V mode (default)
Boot BIOS Strap (BBS)
GPIO_111
0 | Boot from SPI
1 | Do not boot from SPI (default)
Flash Descriptor Override
GPIO_118
0 | No Override (Normal Operation)
1 | Override
Top swap override
GPIO_120
0 | Disable (default)
1 | Override
Title
SOC_LPC_SPI_EMMC_SD
Size
Custom
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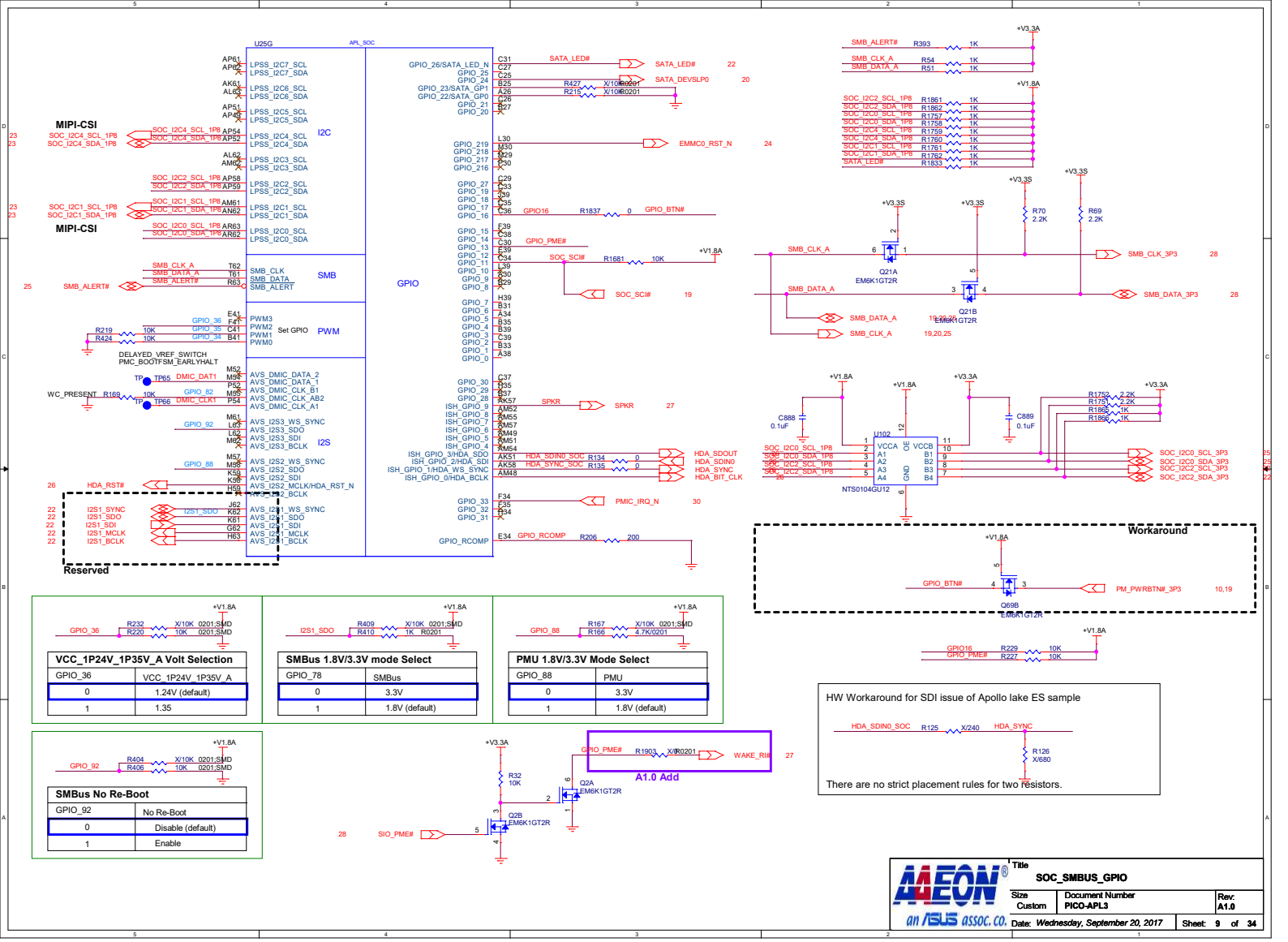

VCC_1P24V_1P35V_A Volt Selection

GPIO_36	VCC_1P24V_1P35V_A
0	1.24V (default)
1	1.35

SMBus 1.8V/3.3V mode Select

GPIO_78	SMBus
0	3.3V
1	1.8V (default)

PMU 1.8V/3.3V Mode Select

GPIO_88	PMU
0	3.3V
1	1.8V (default)

SMBus No Re-Boot

GPIO_92	No Re-Boot
0	Disable (default)
1	Enable

Title	SOC_SMBUS_GPIO
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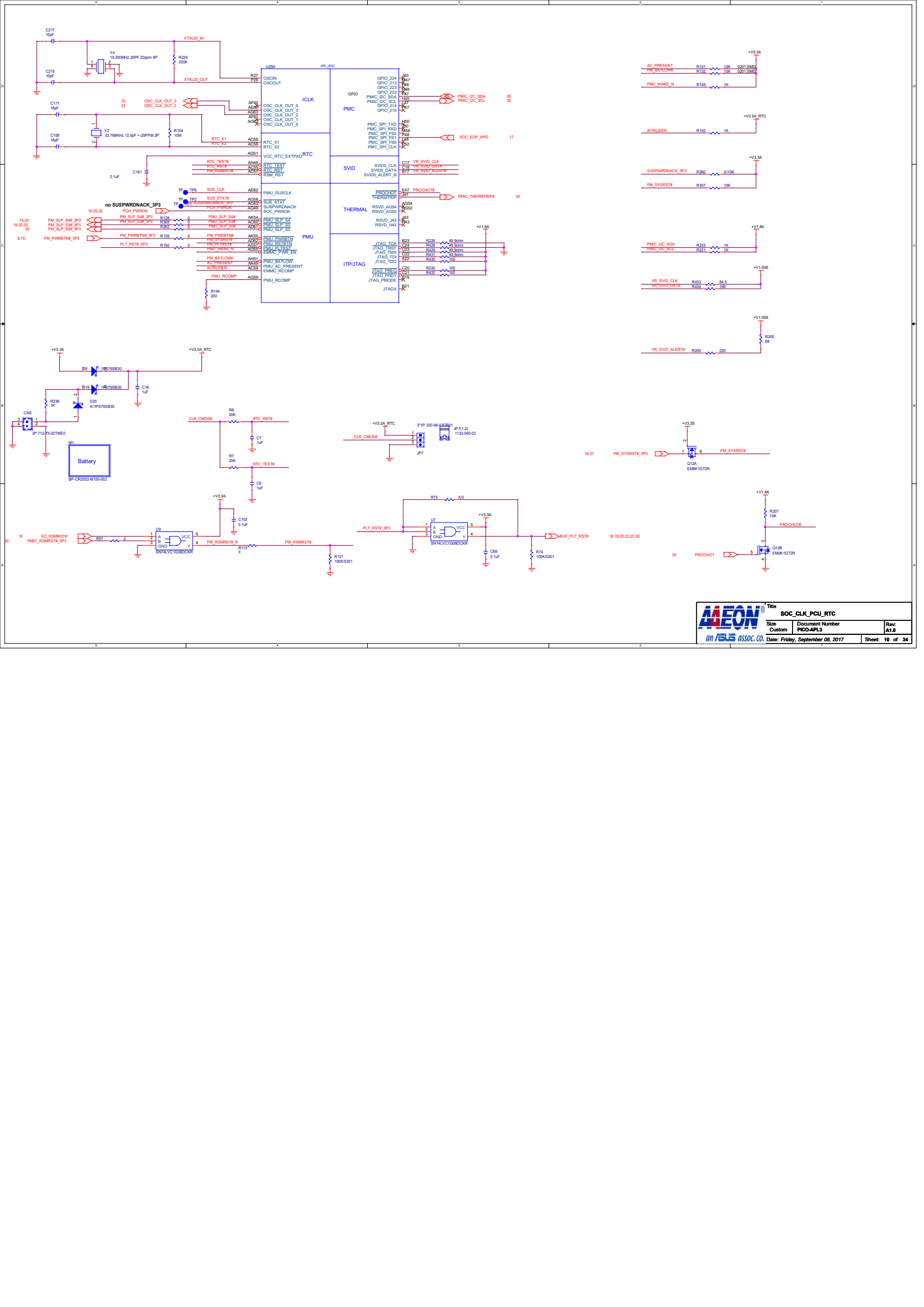

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Size: Custom	Document Number: PICO-APL3	Rev: A1.0	
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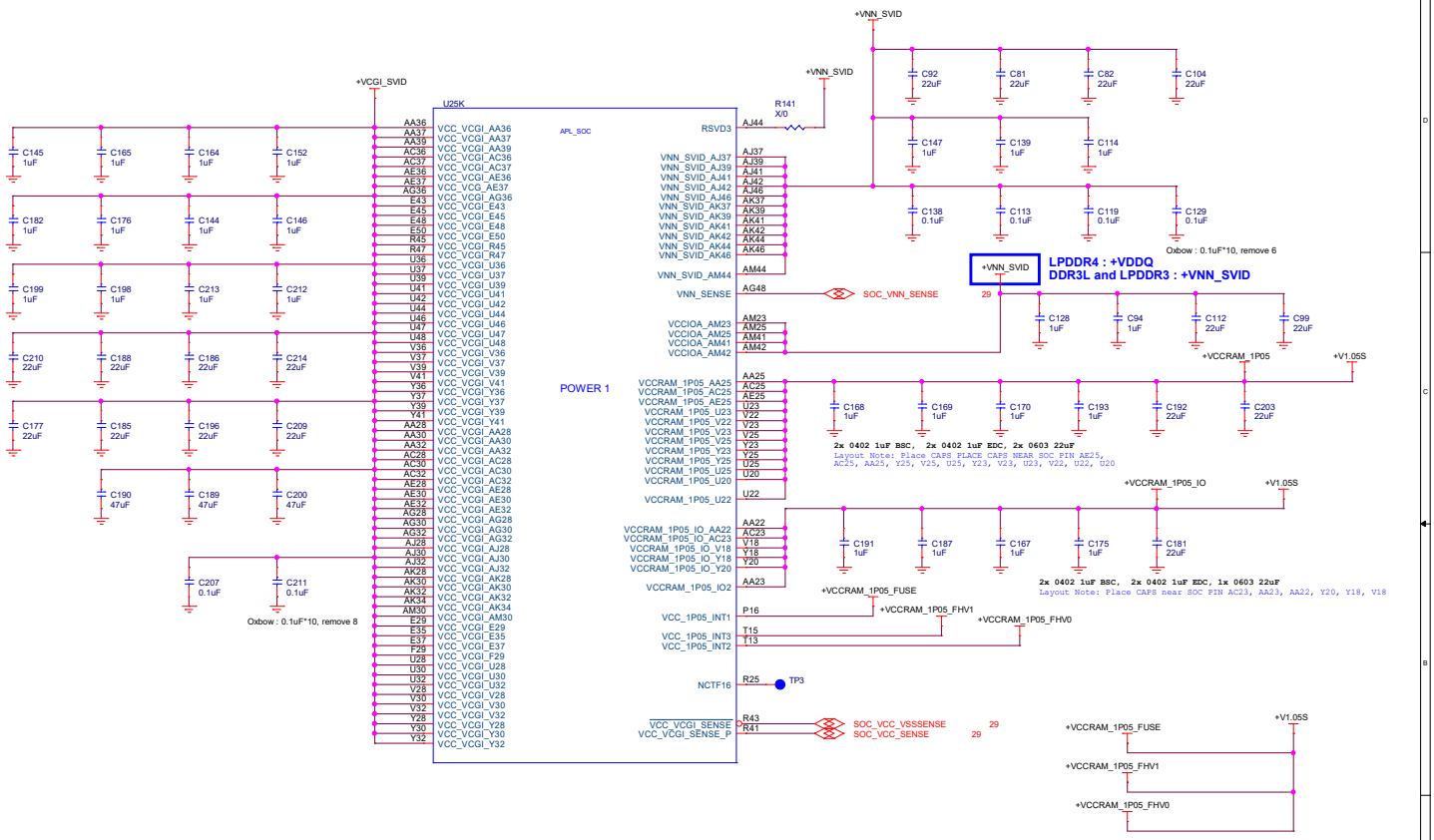

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Size	Custom
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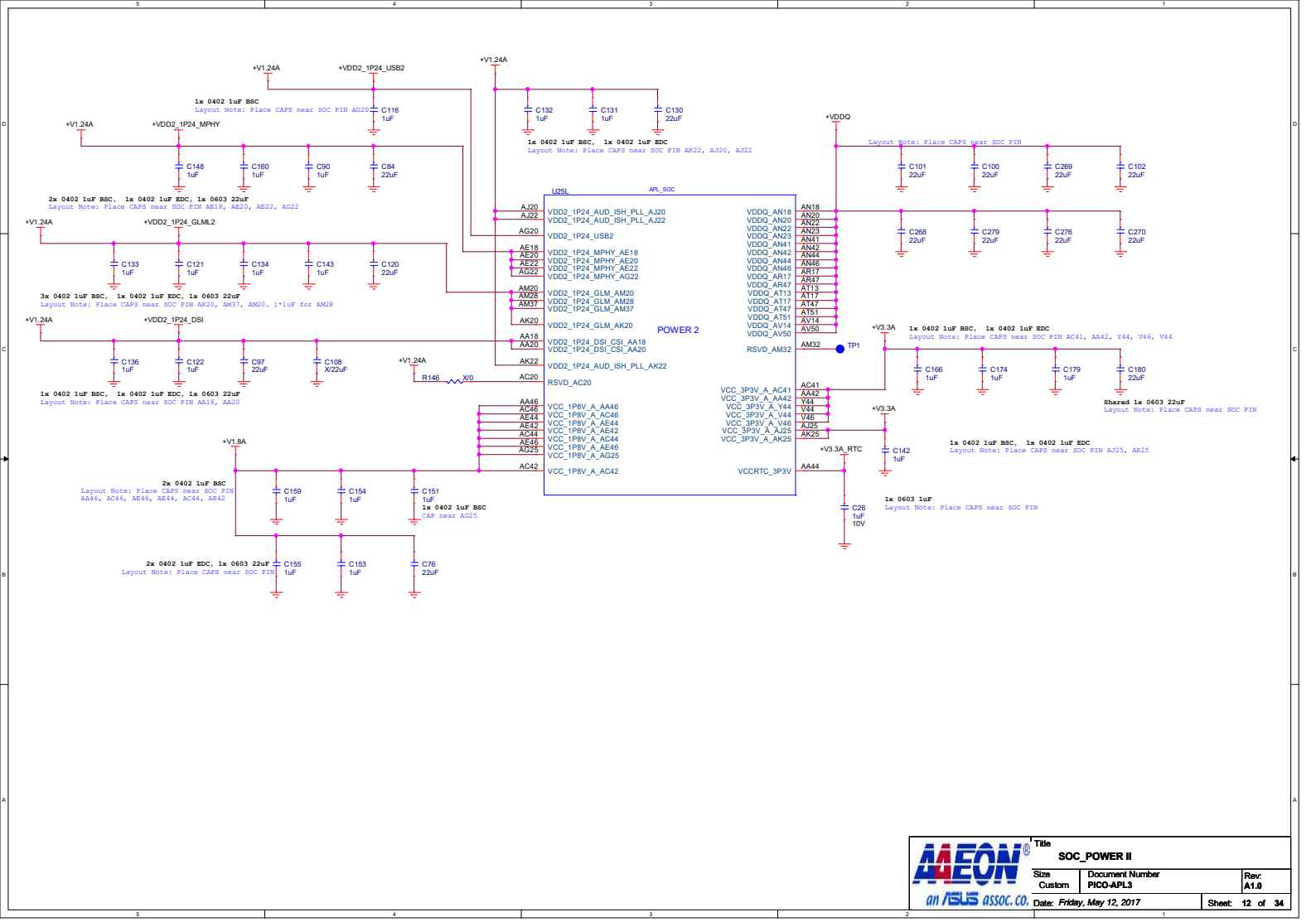

Title	SOC_POWER II	
Size: Custom	Document Number: PICO-APL3	Rev: A1.0
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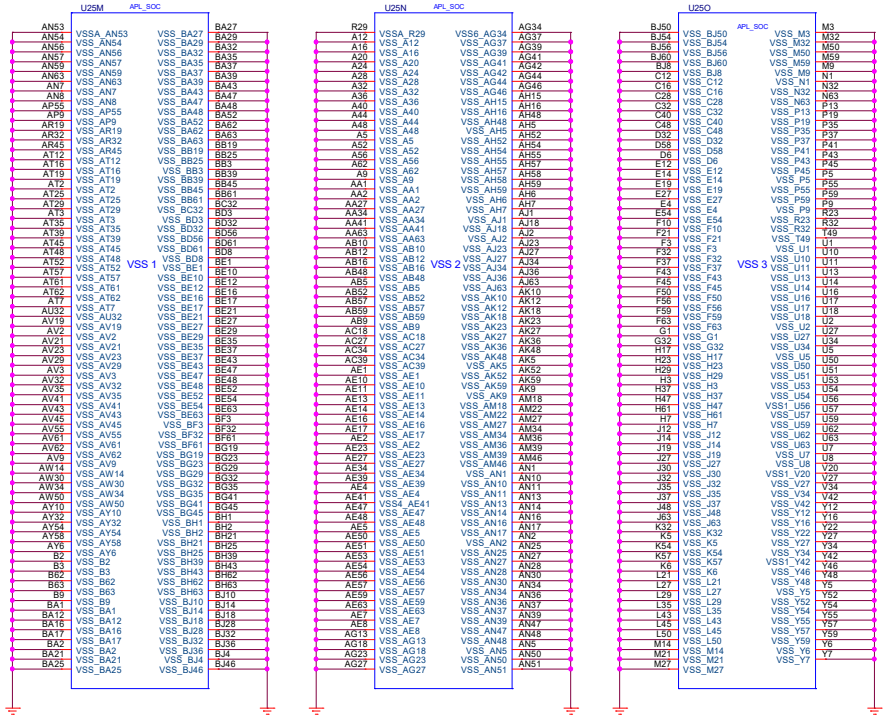

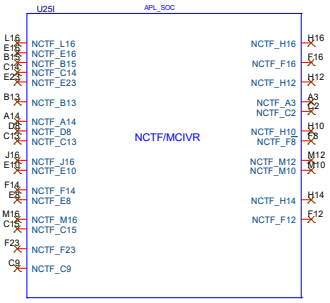

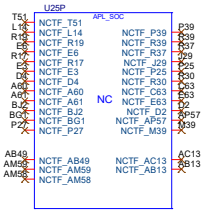

AAEON an ASUS assoc. co.	Title: SOC_GND		
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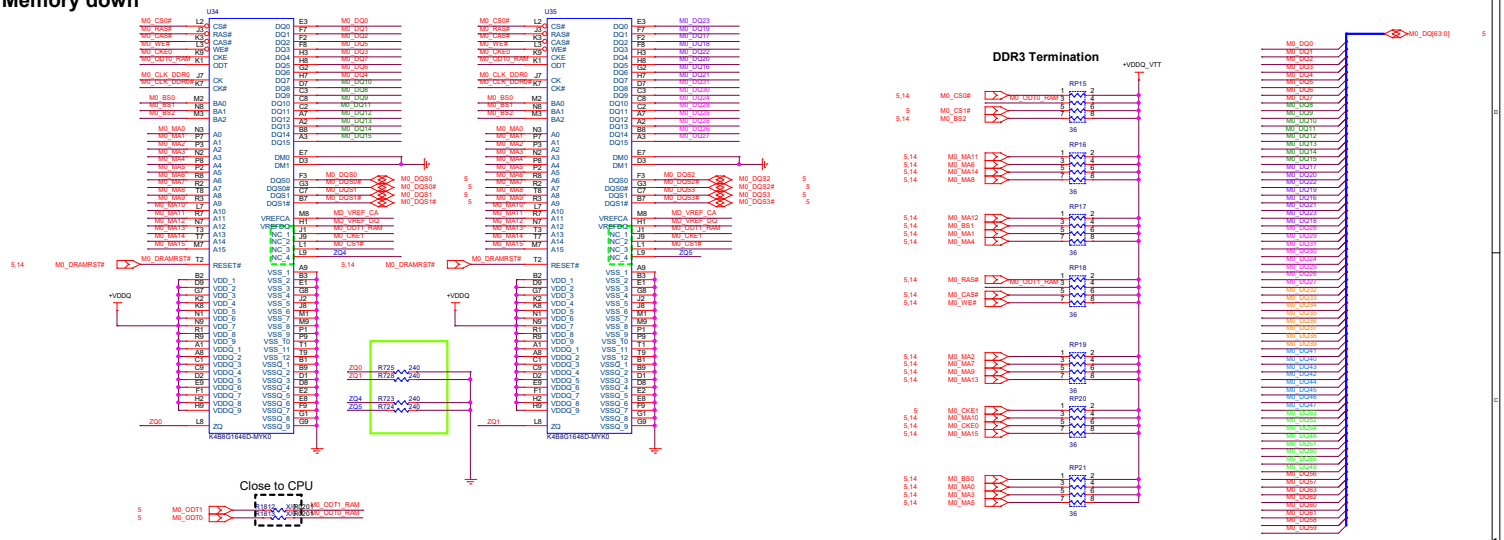
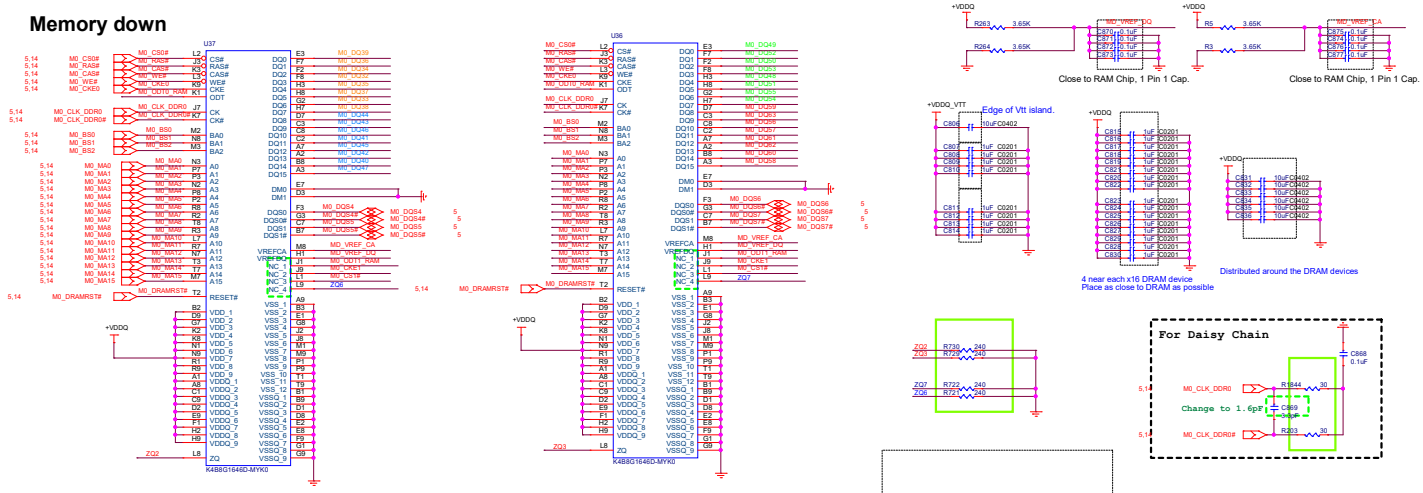
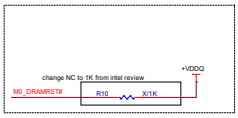
Memory down



Memory down





ASUS	Title: DDR3L X16		
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AAEON an ASUS assoc. co.	Title: Level Shift		
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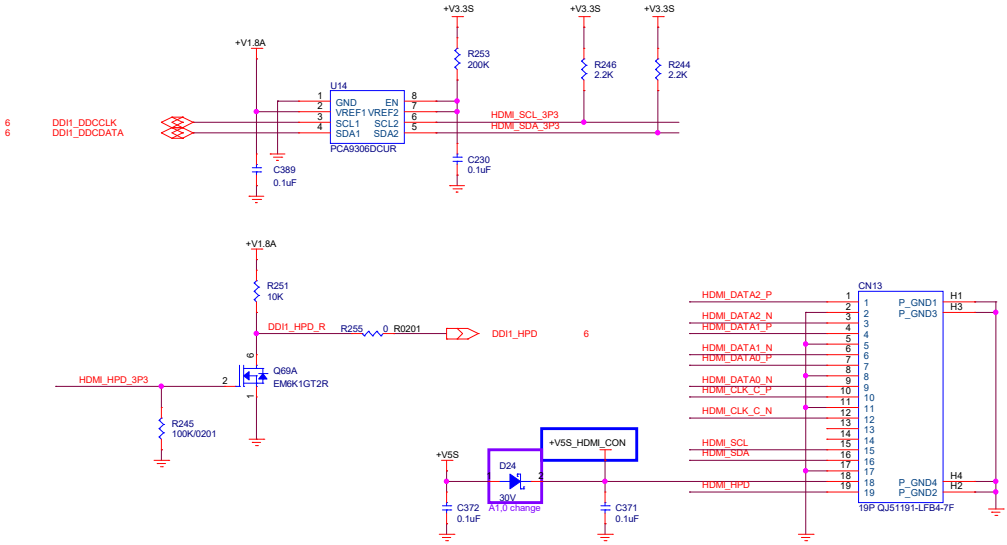
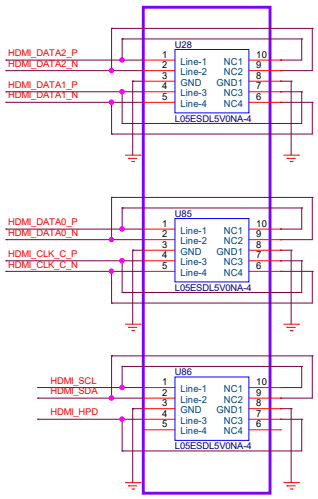
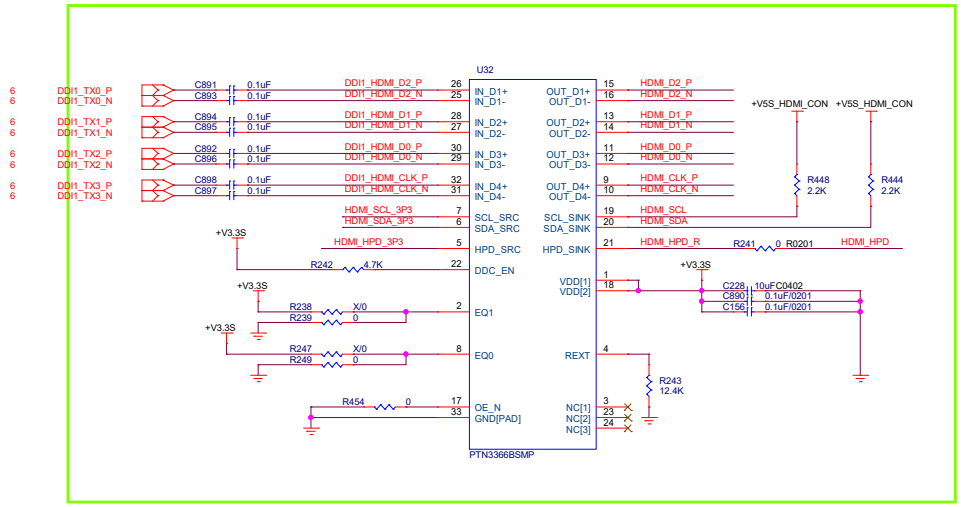
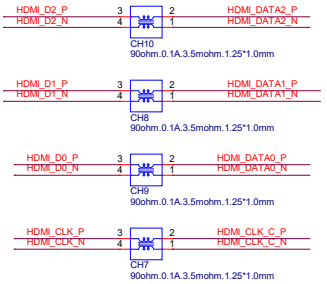
HDMI









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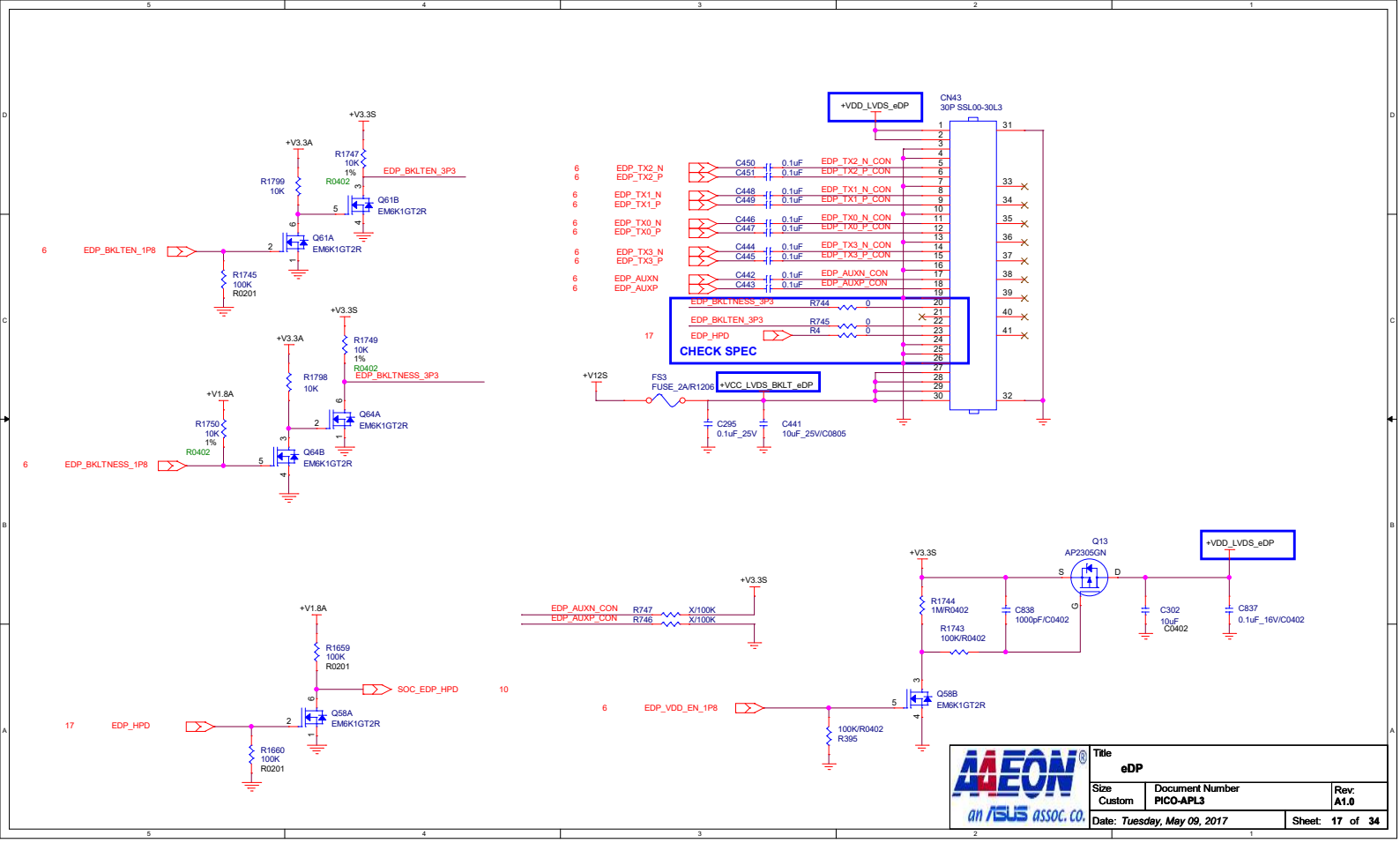

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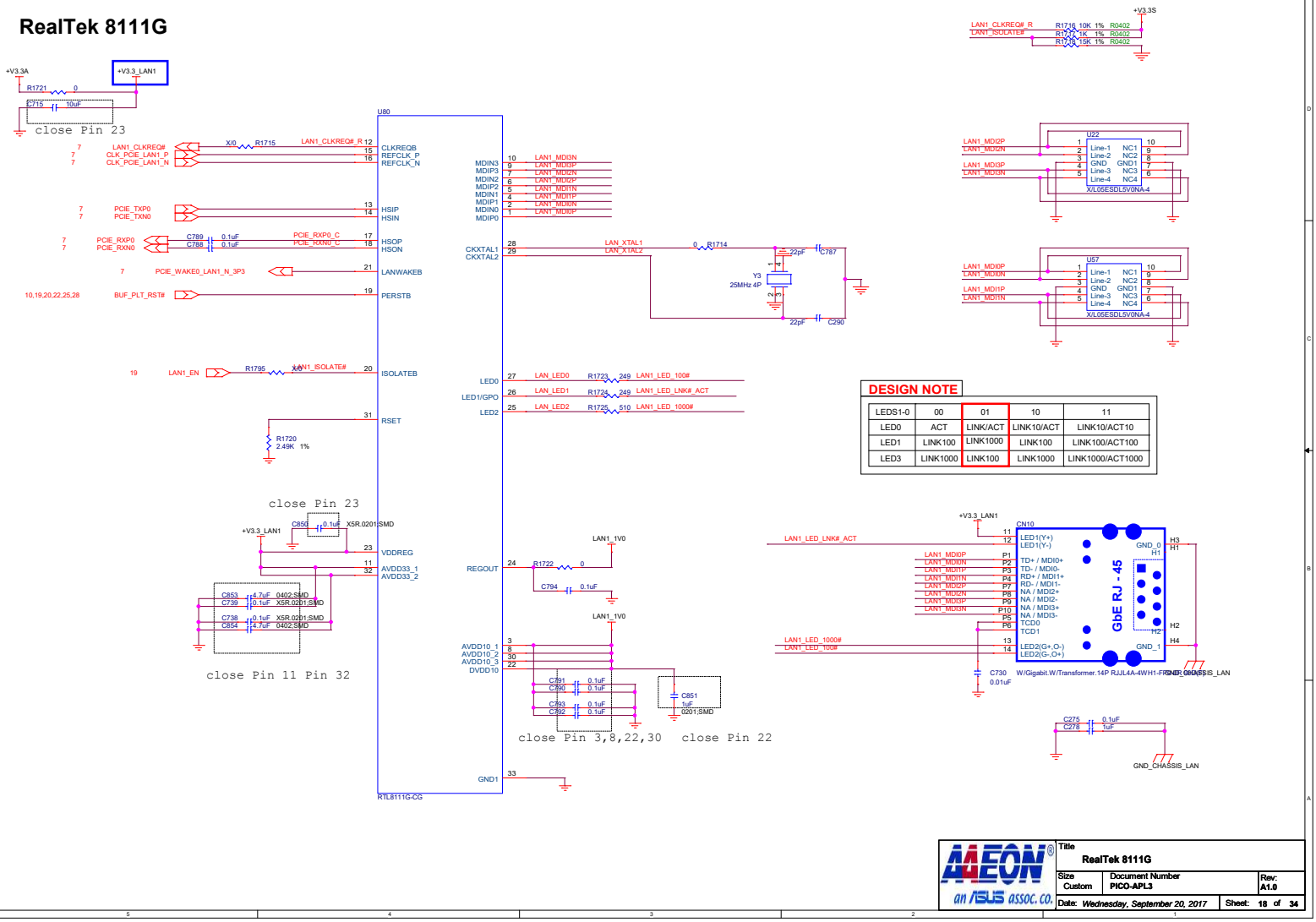
RealTek 8111G



AAEON an ASUS ASSOC. CO.	Title: RealTek 8111G		
	Size: Custom	Document Number: PICO-APL3	Rev: A1.0
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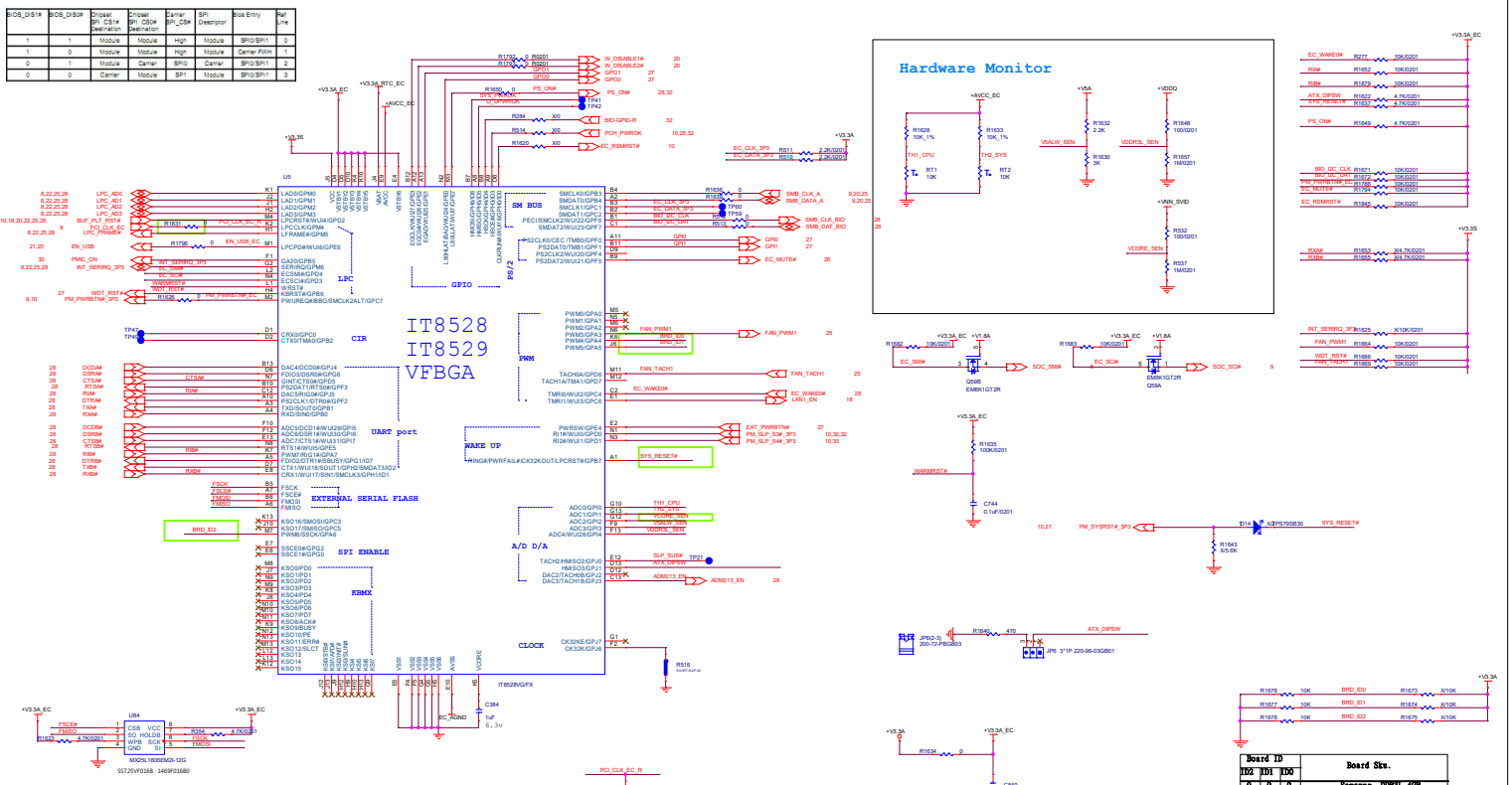
BIOS_DIS1#	BIOS_DIS0#	Chipset SPI_CS1# Destination	Chipset SPI_CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier R/W	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI	Module	SPI0/SPI1	3



GA20/ECSCI/ECSMI/KBRST# pay attention for leak current

(1) Each input pin should be driven or pulled.

(2) Open-drain output pin should be pulled.

DO NOT place any pull up resistor on G0,G2,G6 (Reserved for Hardware strapping)

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Board ID			
ID2	ID1	ID0	Board Stu.
0	0	0	Samsung DDR3L 4GB
0	0	1	Samsung DDR3L 2GB

Note: Place all capacitors close to IT8518.

Title	EC IT8528		
Size: Custom	Document Number: PICO-APL3		Rev: A1.0
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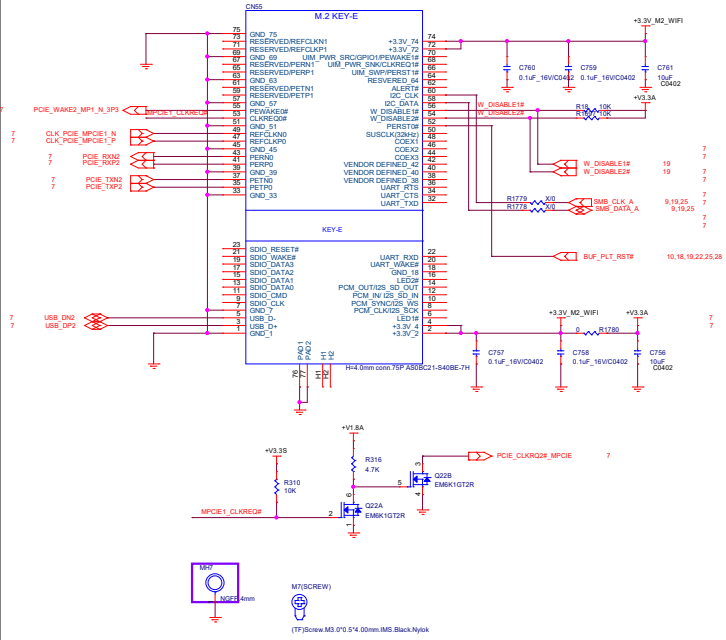
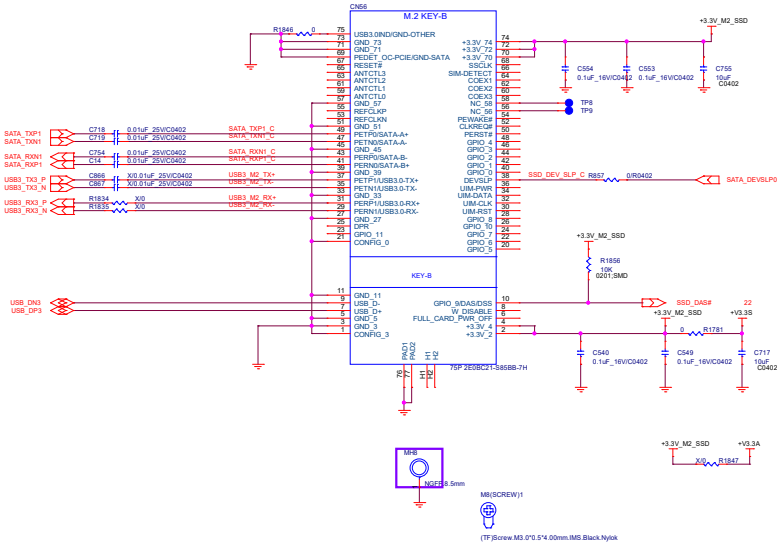
M.2 Key E

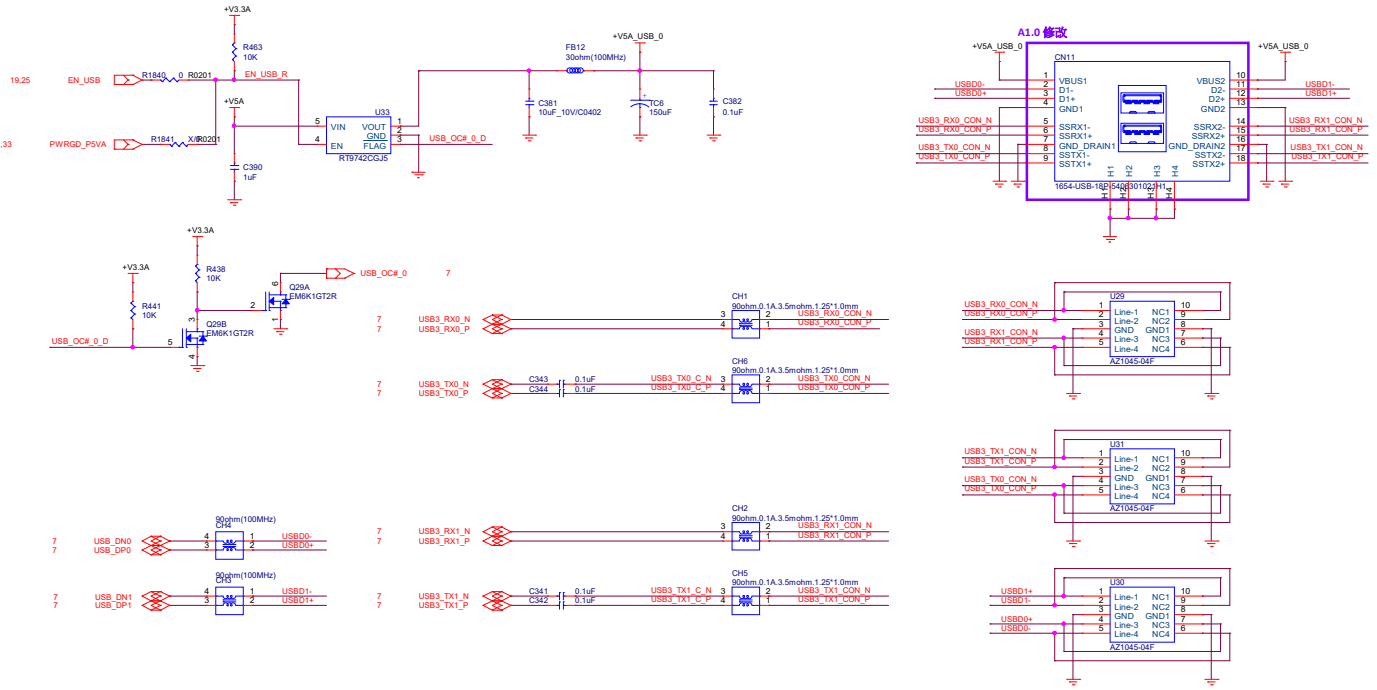


M.2 Key B

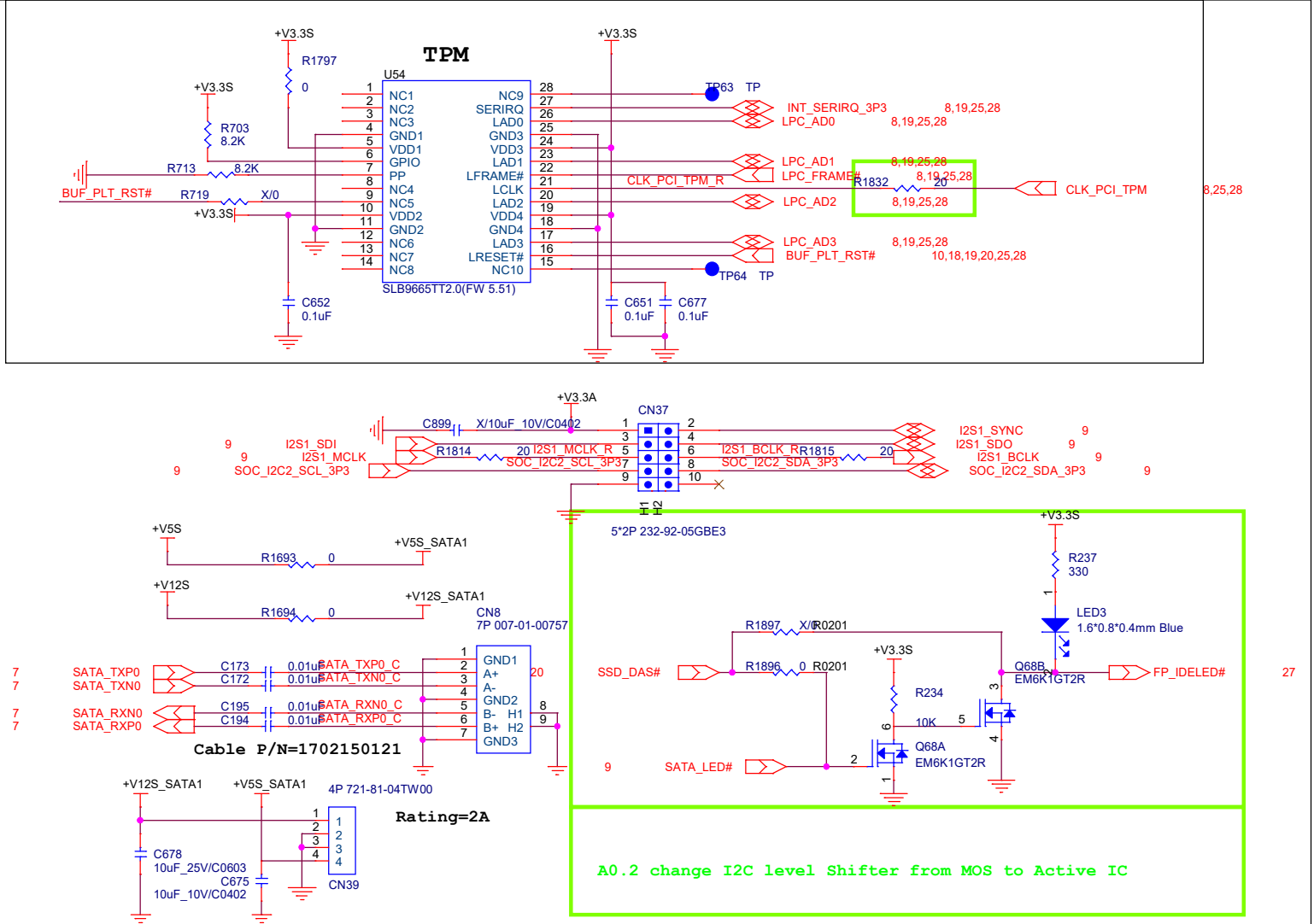


AAEON an ASUS assoc. co.	Title: M.2 *2		
	Size: Custom	Document Number: PICO-APL3	Rev: A1.0
	Date: Wednesday, September 20, 2017	Sheet: 28 of 34	

USB3.0 x 2

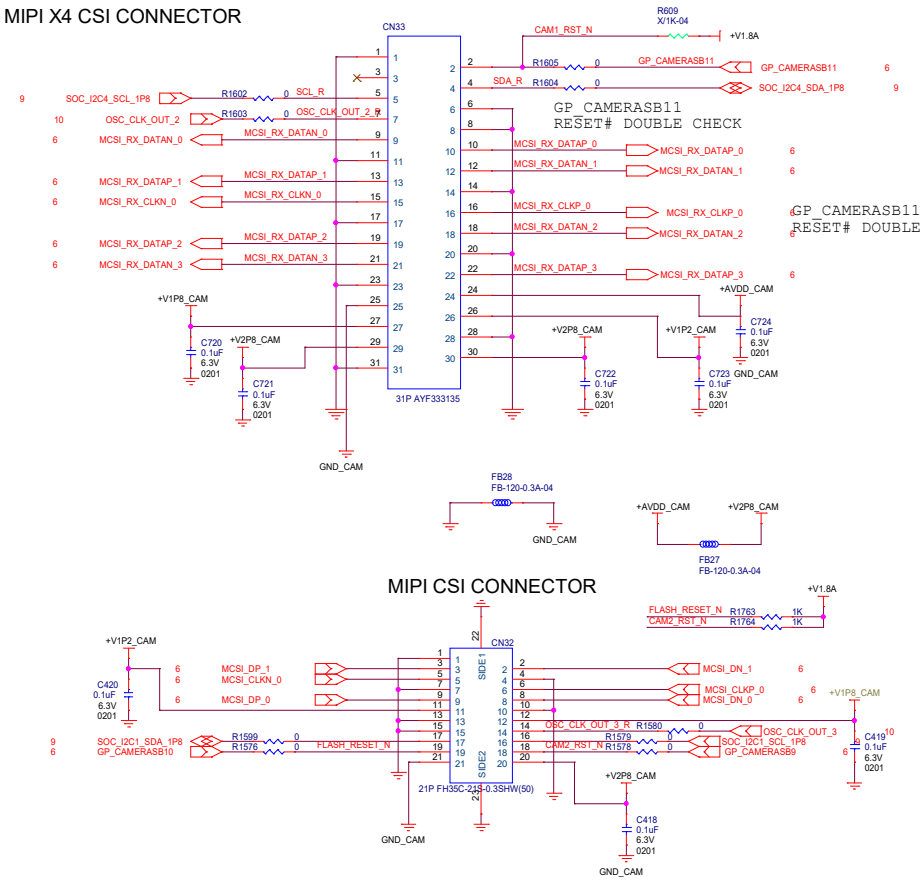


AAEON an ASUS assoc. co.	Title: USB 3.0/2.0 PORT		
	Size: Custom	Document Number: PICO-APL3	Rev: A1.0
	Date: Friday, September 01, 2017		Sheet: 21 of 34



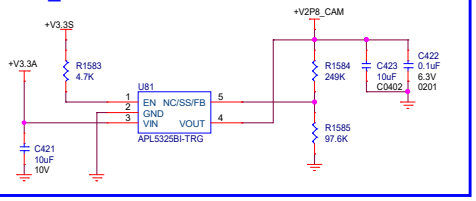
Title: TPM & SATA & MISC		
Size: Custom	Document Number: PICO-APL3	Rev: A1.0
Date: Wednesday, September 20, 2017	Sheet: 22 of 34	

MIPI X4 CSI CONNECTOR

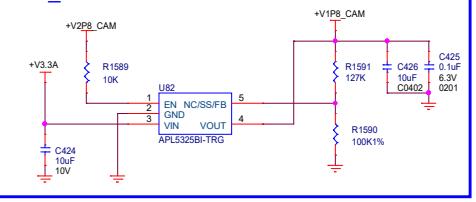


MIPI CSI CONNECTOR

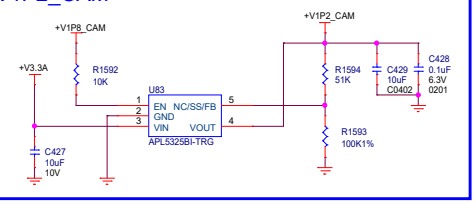
+V2P8_CAM



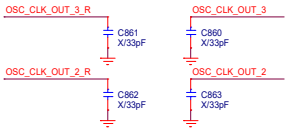
+V1P8_CAM



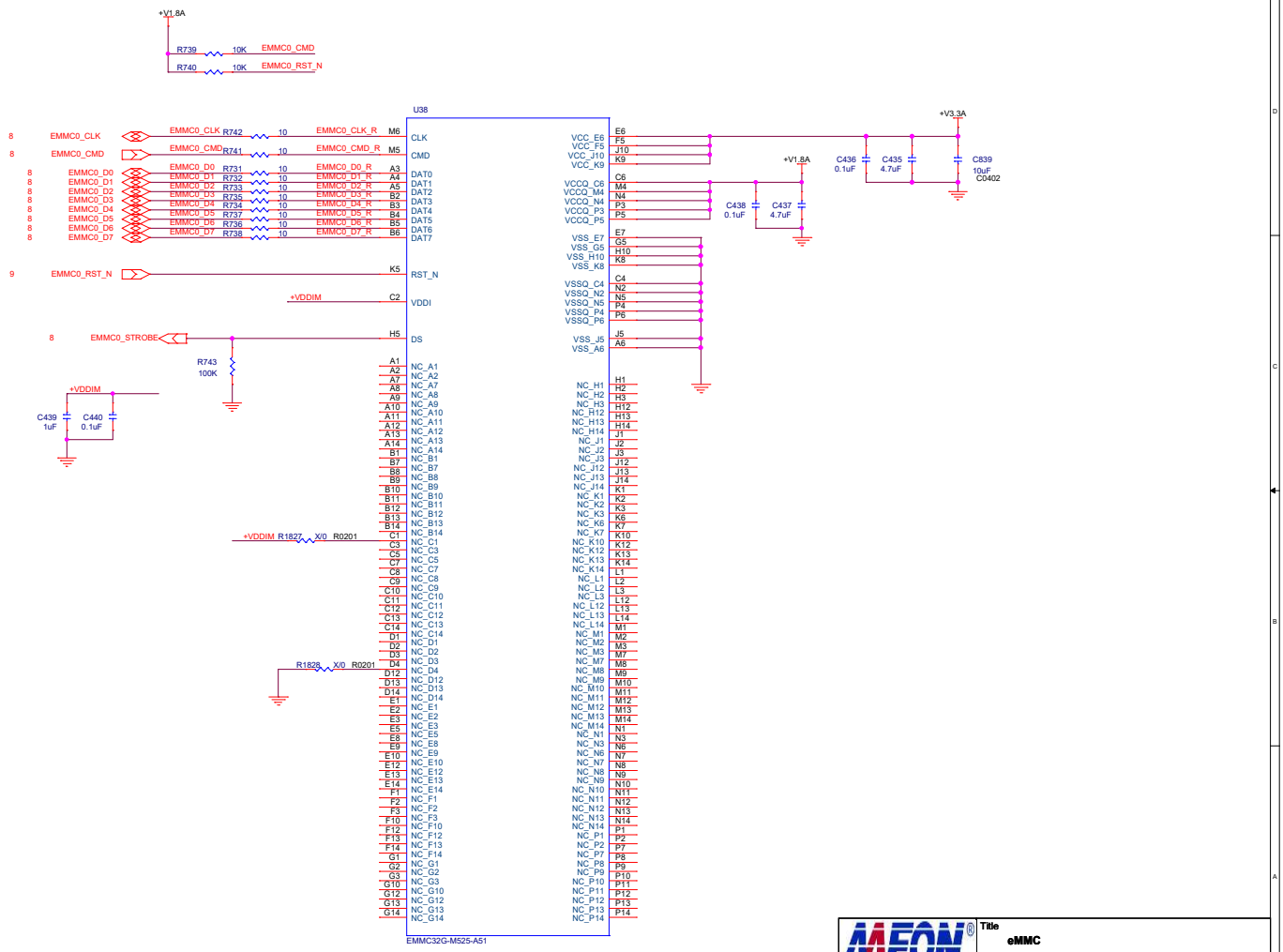
+V1P2_CAM



Reserved for OSC Clock Filter (Close to Connector)



AAEON an ASUS assoc. co.	Title: MIPI-CSI	
Size: Custom	Document Number: PICO-APL3	Rev: A1.0
Date: Tuesday, May 09, 2017		Sheet: 23 of 32



Title: eMMC		
Size: Custom	Document Number: PICO-APL3	Rev: A1.0
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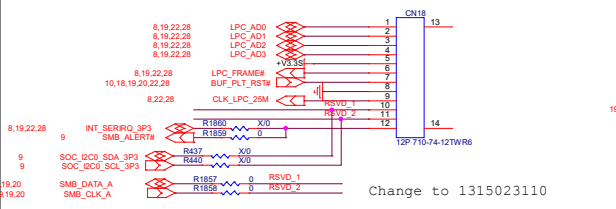
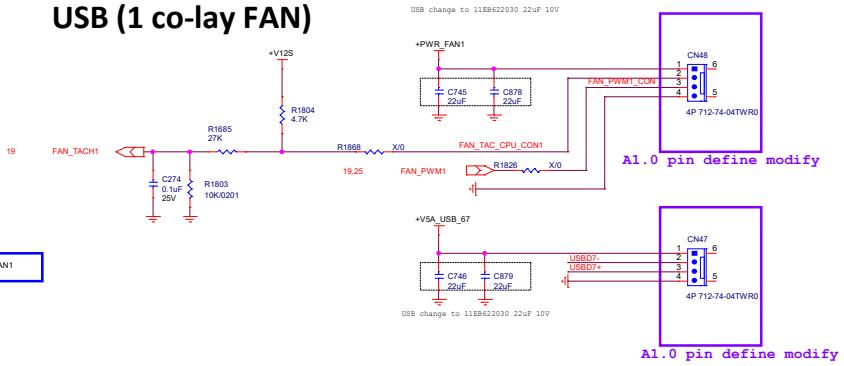
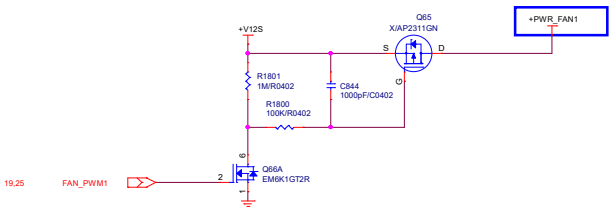
LPC Debug Connector

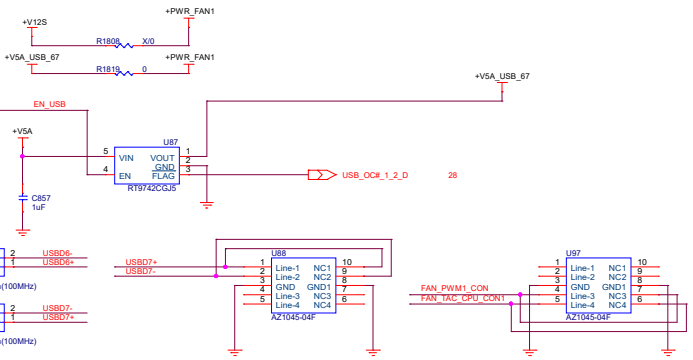


Change to 1315023110

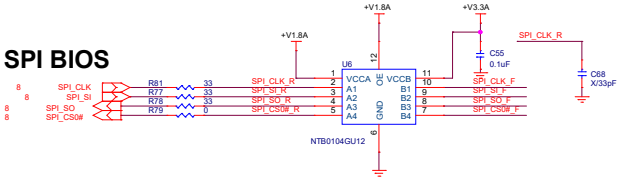
USB (1 co-lay FAN)

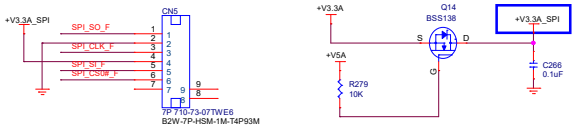


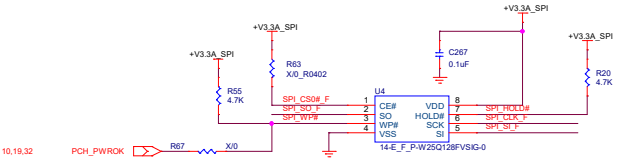




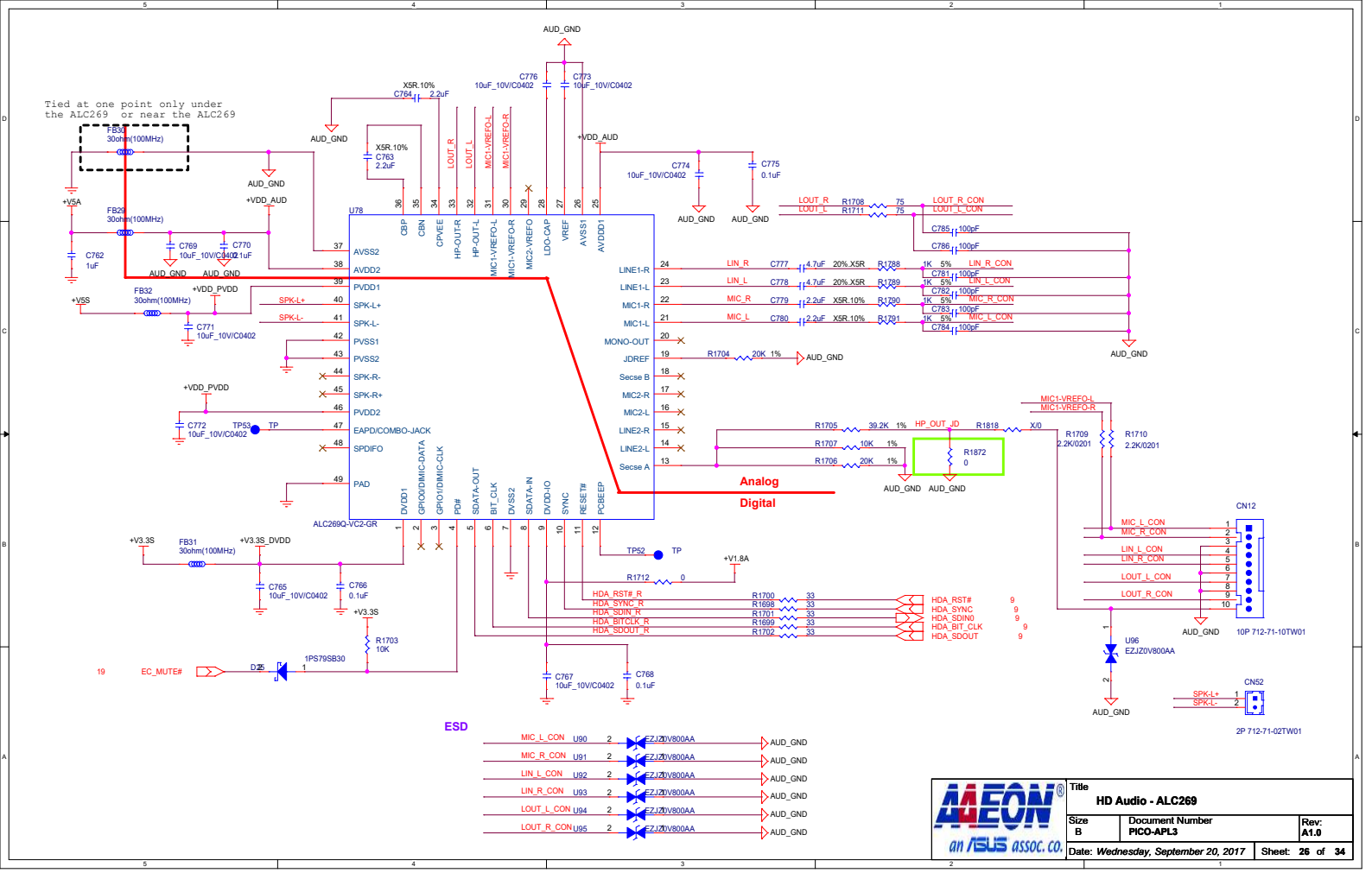
SPI BIOS







AAEON an ASUS assoc. co.	Title: FAN/ Debug		
	Size: Custom	Document Number: PICO-APL3	Rev: A1.0
	Date: Wednesday, September 20, 2017	Sheet: 25 of 34	


Tied at one point only under
the ALC269 or near the ALC269
ALC269Q-VC2-GR
Analog
Digital
ESD
Title
HD Audio - ALC269
Size
B
Document Number
PICO-APL3
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A1.0
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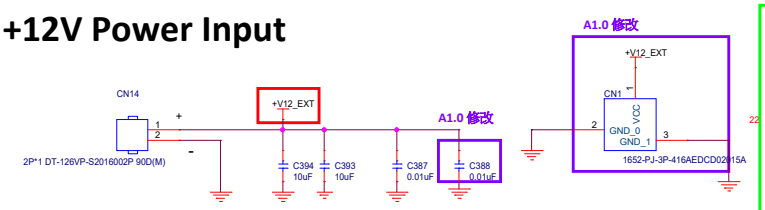
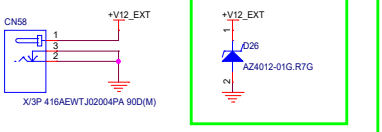
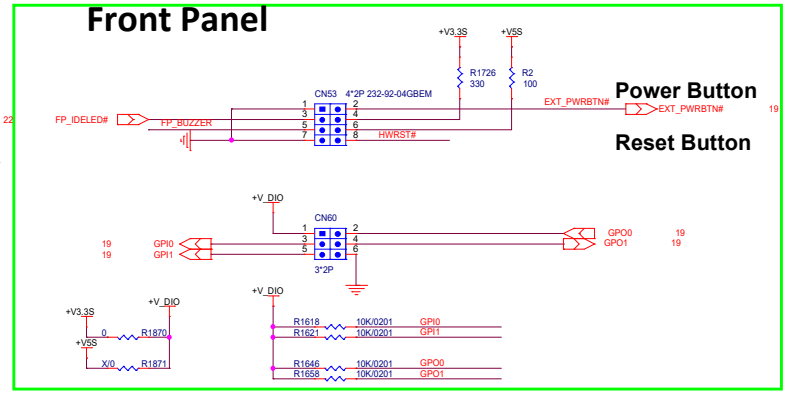
+12V Power Input



Auto Power Button

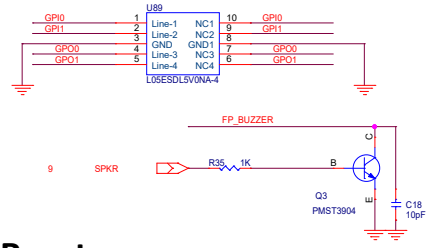


Front Panel

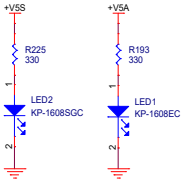


CMOS Control Selection(RTC_RST#)		
No Stuff	Save CMOS	Default
3-4	Clear CMOS	

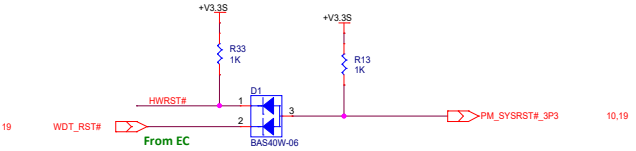
Auto power button		
No Stuff	ATX	Default
1-2	AT	



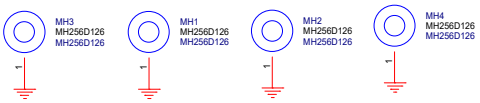
Power LED



System Reset



Mounting Holes / Non-PTH



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Title: Front Panel/Power in

Size	Document Number	Rev:
B	PICO-APL3	A1.0

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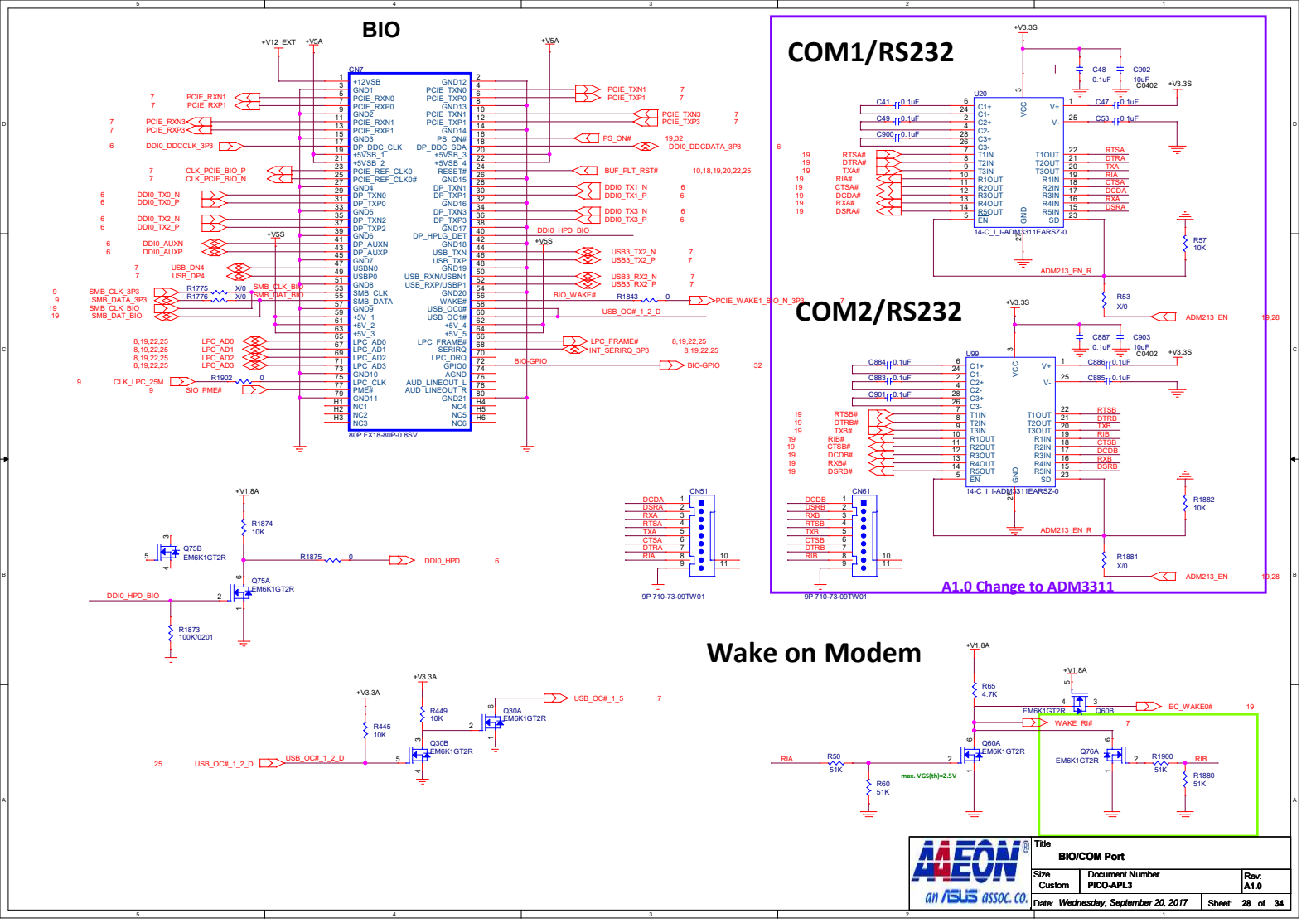

Title	BIO/COM Port		
Size	Document Number		Rev:
Custom	PICO-APL3		A1.0
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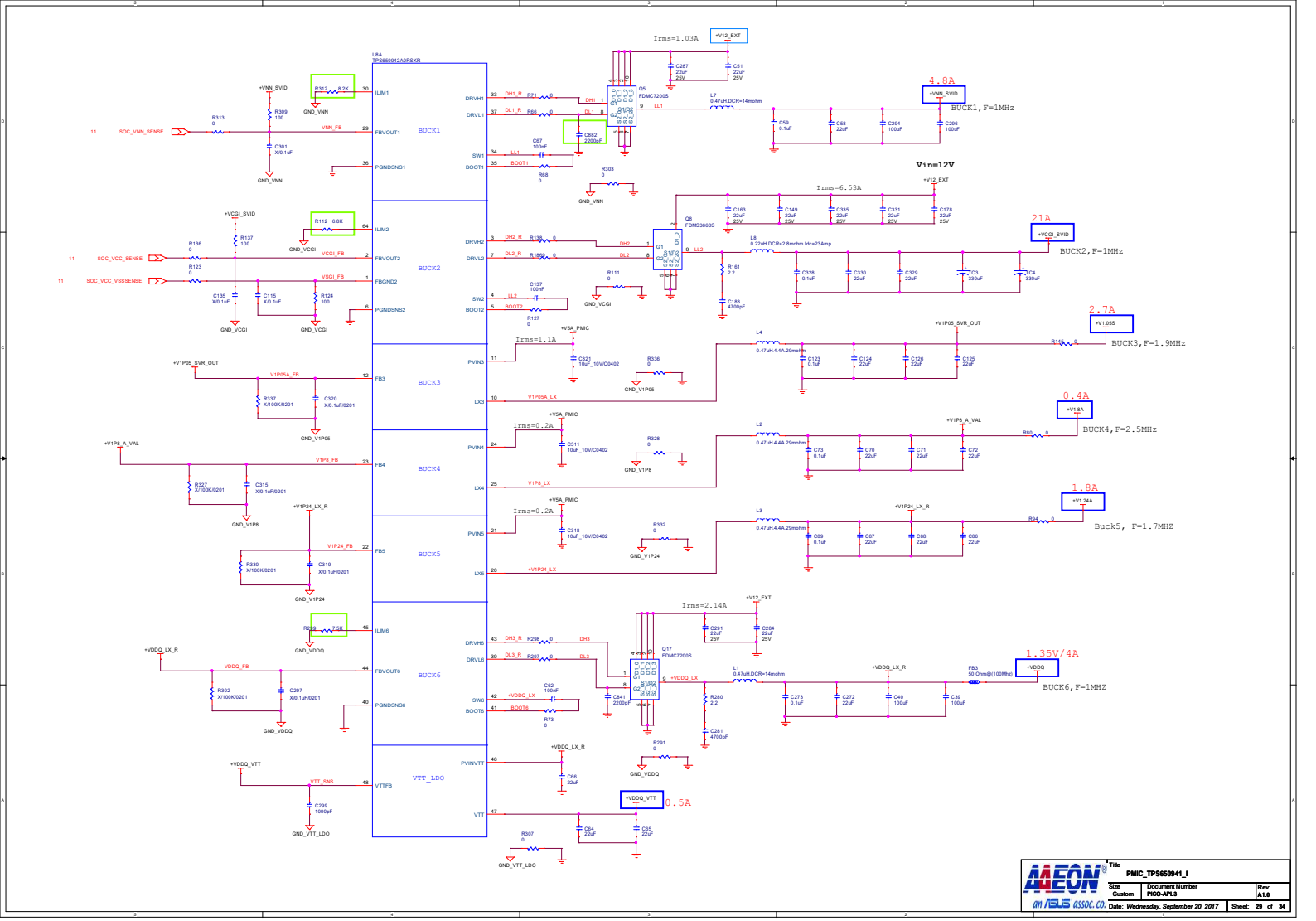
U8A
TPS650942A0RSKR
BUCK1
BUCK2
BUCK3
BUCK4
BUCK5
BUCK6
VTT_LDO
ILIM1
FBVOUT1
PGNDSNS1
ILIM2
FBVOUT2
FBGND2
PGNDSNS2
FB3
FB4
FB5
ILIM6
FBVOUT6
PGNDSNS6
VTTFB
DRVH1
DRVL1
SW1
BOOT1
DRVH2
DRVL2
SW2
BOOT2
PVIN3
LX3
PVIN4
LX4
PVIN5
LX5
DRVH6
DRVL6
SW6
BOOT6
PVINVTT
VTT
+V12_EXT
Irms=1.03A
4.8A
+VNN_SVID
BUCK1,F=1MHz
Vin=12V
Irms=6.53A
21A
+VCGI_SVID
BUCK2,F=1MHz
2.7A
+V1.05S
BUCK3,F=1.9MHz
Irms=1.1A
+V1P05_SVR_OUT
0.4A
+V1.8A
BUCK4,F=2.5MHz
Irms=0.2A
+V1P8_A_VAL
1.8A
+V1.24A
Buck5, F=1.7MHZ
Irms=0.2A
+V1P24_LX_R
Irms=2.14A
1.35V/4A
+VDDQ
BUCK6,F=1MHZ
+VDDQ_LX_R
+VDDQ_VTT
0.5A
SOC_VNN_SENSE
SOC_VCC_SENSE
SOC_VCC_VSSSENSE
VNN_FB
VCGI_FB
VSGI_FB
V1P05A_FB
V1P8_FB
V1P24_FB
VDDQ_FB
VTT_SNS
+V5A_PMIC
+V1P8
+V1P24
+VDDQ
GND_VNN
GND_VCGI
GND_V1P05
GND_V1P8
GND_V1P24
GND_VDDQ
GND_VTT_LDO
Q5
FDMC7200S
Q8
FDMS3660S
Q17
FDMC7200S
L7
0.47uH,DCR=14mohm
L8
0.22uH,DCR=2.8mohm,Idc=23Amp
L4
0.47uH,4.4A,29mohm
L2
0.47uH,4.4A,29mohm
L3
0.47uH,4.4A,29mohm
L1
0.47uH,DCR=14mohm
FB3
50 Ohm@100Mhz
Title
PMIC_TPS650941_I
Size
Custom
Document Number
PICO-APL3
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A1.6
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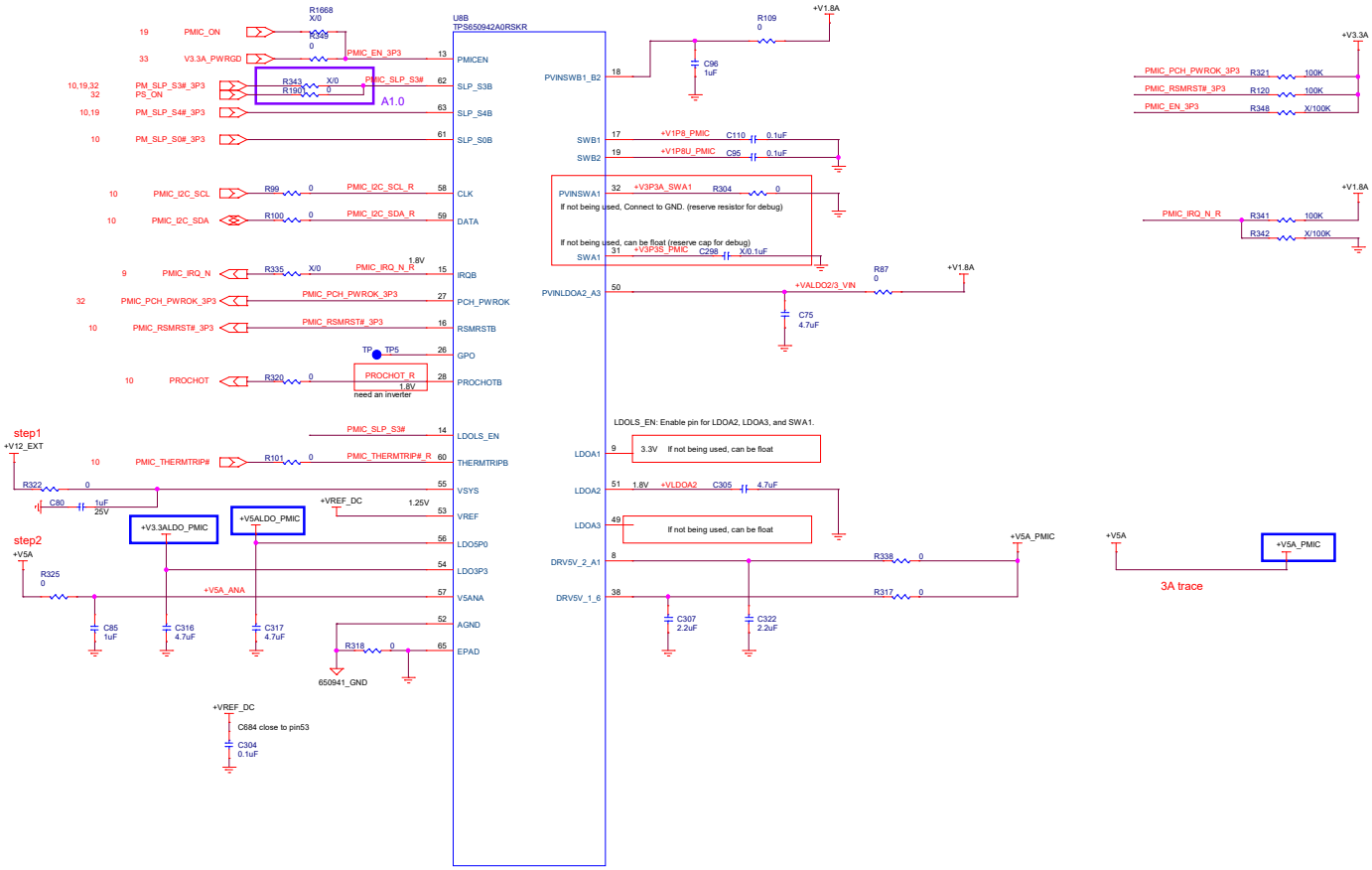

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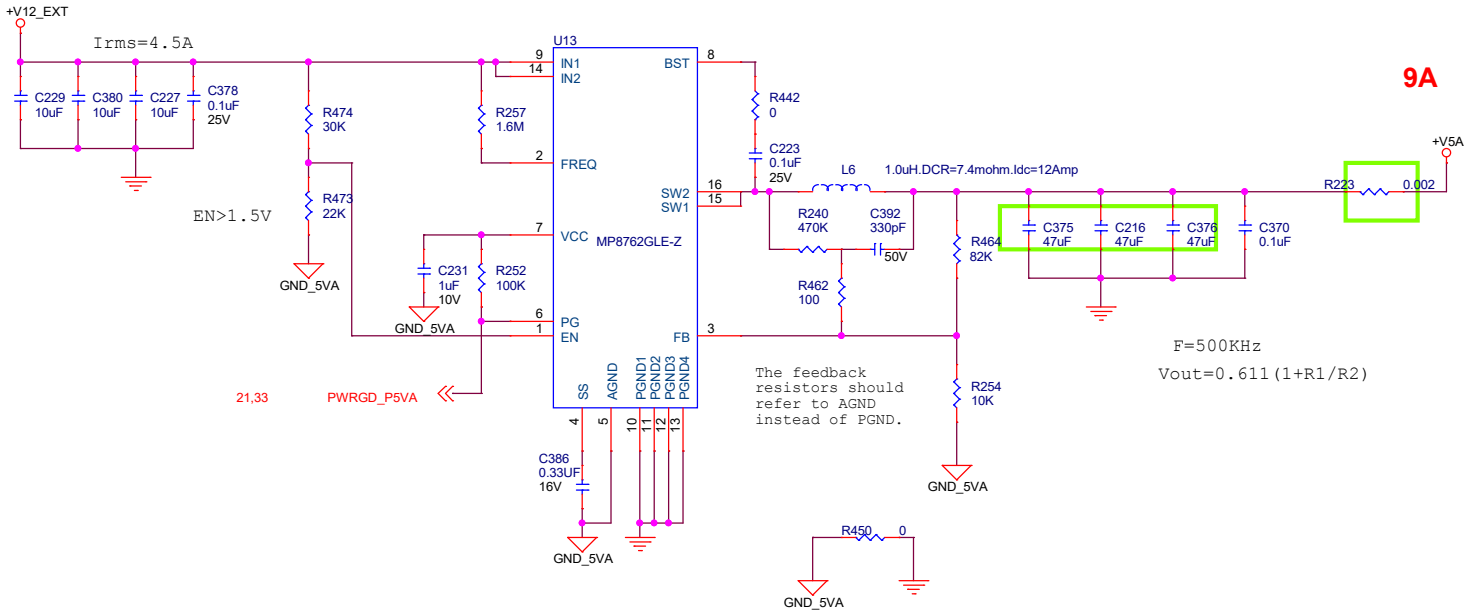
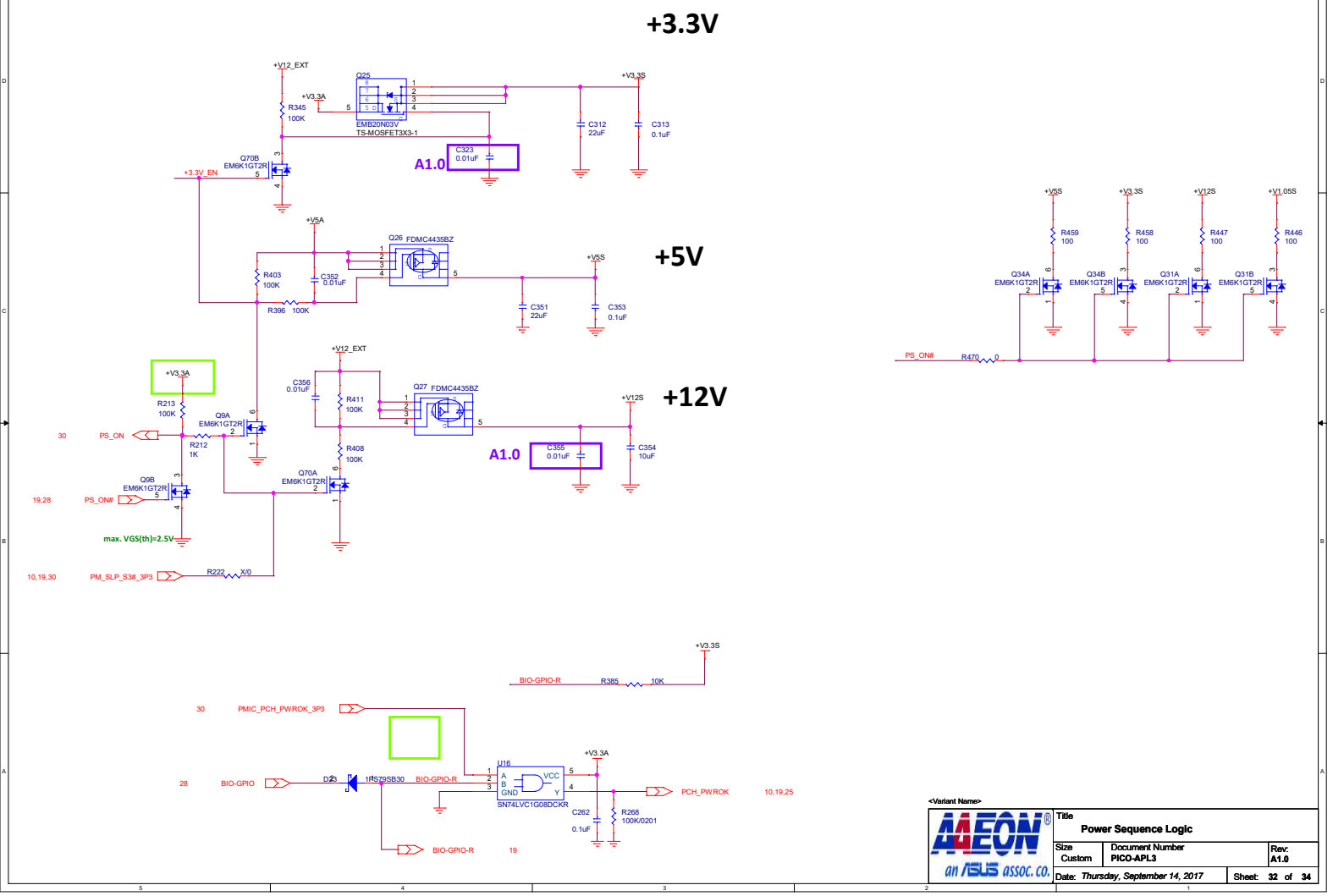
Size: Custom	Document Number: PICO-APL3		Rev: A1.0
Date: Wednesday, September 20, 2017		Sheet: 30 of 34	



Title: **Power VR : +V5A**		
Size: Custom	Document Number: **PICO-APL3**	Rev: **A1.0**
Date: *Tuesday, May 09, 2017*	Sheet: **31** of **34**	

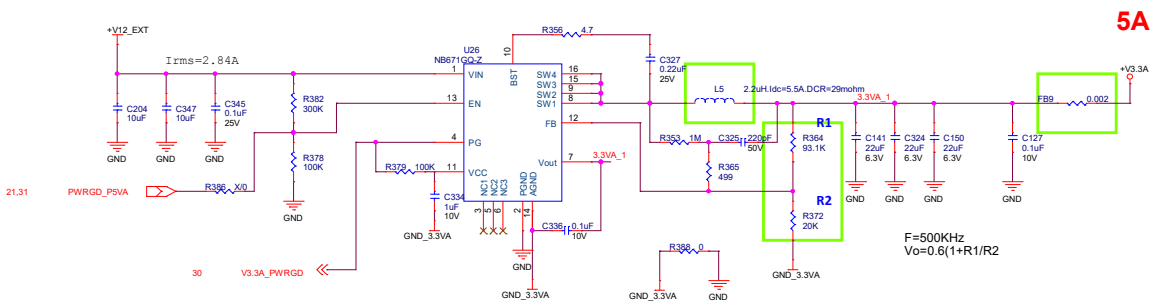


<Variant Name>

AAEON an ASUS assoc. co.

Title: Power Sequence Logic		
Size: Custom	Document Number: PICO-APL3	Rev: A1.0
Date: Thursday, September 14, 2017		Sheet: 32 of 34

1.35V<EN<12V
EN voltage should be lower than 12V



Title: Power VR : +V3.3A.+V1.5S		
Size: Custom	Document Number: PICO-APL3	Rev: A1.0
Date: Wednesday, September 20, 2017		Sheet: 33 of 34

HISTORY

Item	Date	Revision	Page	Modification List	Reason	Approve By
1	2016/12/20	A0.1	1-34	First Release.		
2	2017/05/08	A0.2	2	PICO-APL3 System Setting	Correct the GPIO Table	
		A0.2	3	PICO-APL3 Power Sequence	Correct the Power Sequence Diagram	
		A0.2	7	Add U98	DDC level shifter change	
		A0.2	8	Add U100 U101	Add LPC Level Shifter	
		A0.2	8	Del R171, Add R175	LPC level change to 1.8V	
		A0.2	9	GPIO_BTN# move to GPIO16	GPIO_BTN# move to GPIO16	
		A0.2	14	R725,R723,R724,R728,R730,R729,R722,R721 R1844 R203	Correct footprint	
		A0.2	16	Add U32	Add HDMI Active Level Shifter	
		A0.2	19	Add Second COM port	Add Second COM port	
		A0.2	25	Del Q67 R1809 R1820 R1823 R1824	Del second FAN	
		A0.2	27	Add CN60	Devide A0.1 Front Panel Header into 2 headers (CN53 CN60)and 2 Jumpers (JP6 JP7)	
		A0.2	28	Add U99 CN61	Add Second COM port	
		A0.2	20	CN11 Change to 1654801832	CN11 Change to 1654801832	
		A0.2	30	PS_ON connect to PMIC pin 62	Reserved PS_ON to PMIC for 4 sec. force shutdown	
		A0.2	27	CN53 CN54 chang to CN53, CN60, JP7, JP6	CN53 CN54 change Pin Define	
		A0.2	27	USB_OC0#, USB_OC1# Swap	Correct USB_OC# order	
		A1.0	16	D24 change	using big current diode	
		A1.0	27	U20 U99 change to ADM3311	EC UART using 3.3V level	
		A1.0	9	SIO_PME# reserved to WAKE_RI#	Reserved	
		A1.0	25	CN47 CN48 USB (pin header) change pin definition	for AAEON COMMON USB 4 pin header definition	
		A1.0	21	CN11 USB 3.0 Dual Port change to 1654801833		

AAEON an ASUS assoc. co.

Title: Revision History

Size	Document Number	Rev:
C	PICO-APL3	A1.0

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