

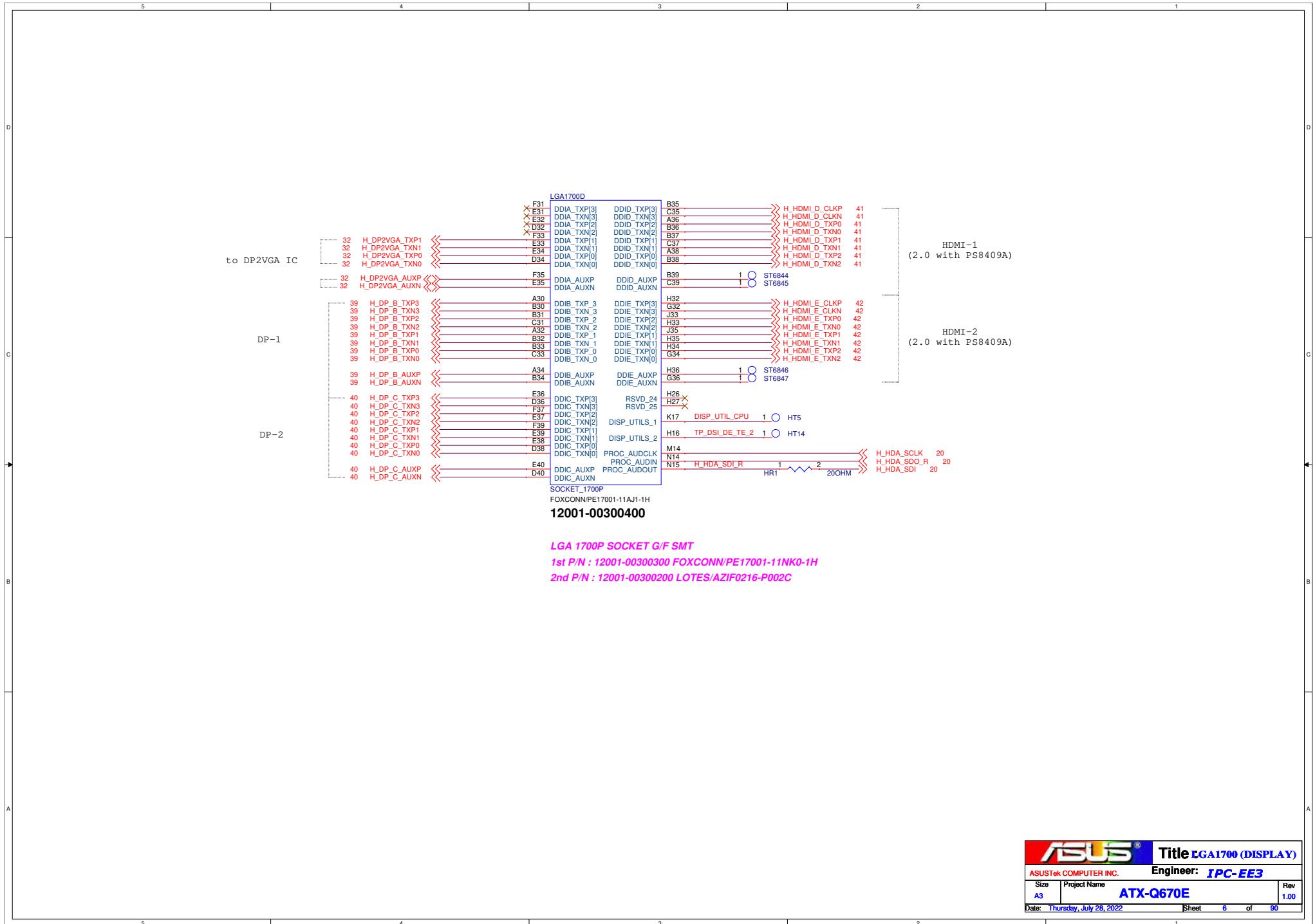
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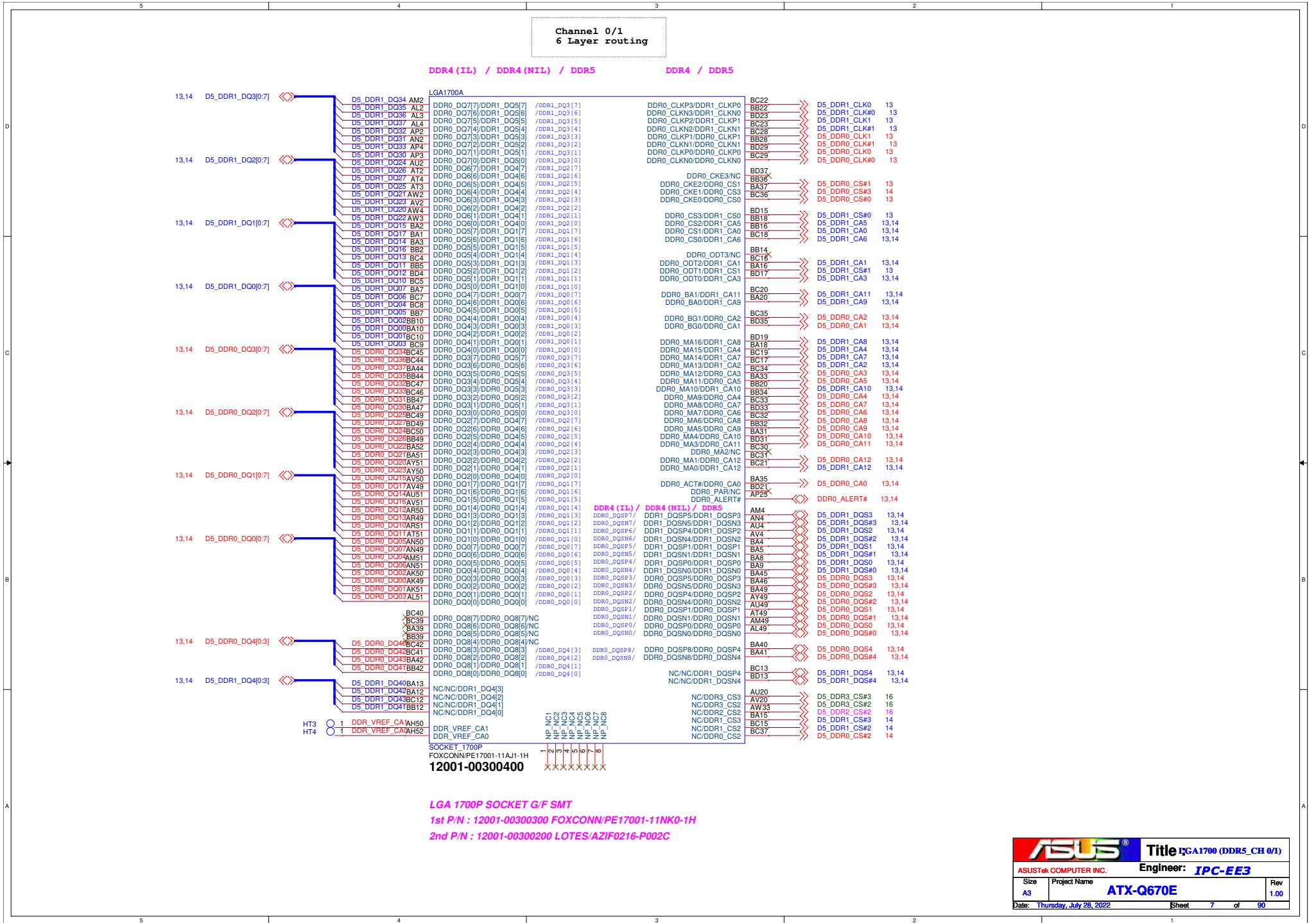
LGA 1700P SOCKET G/F SMT

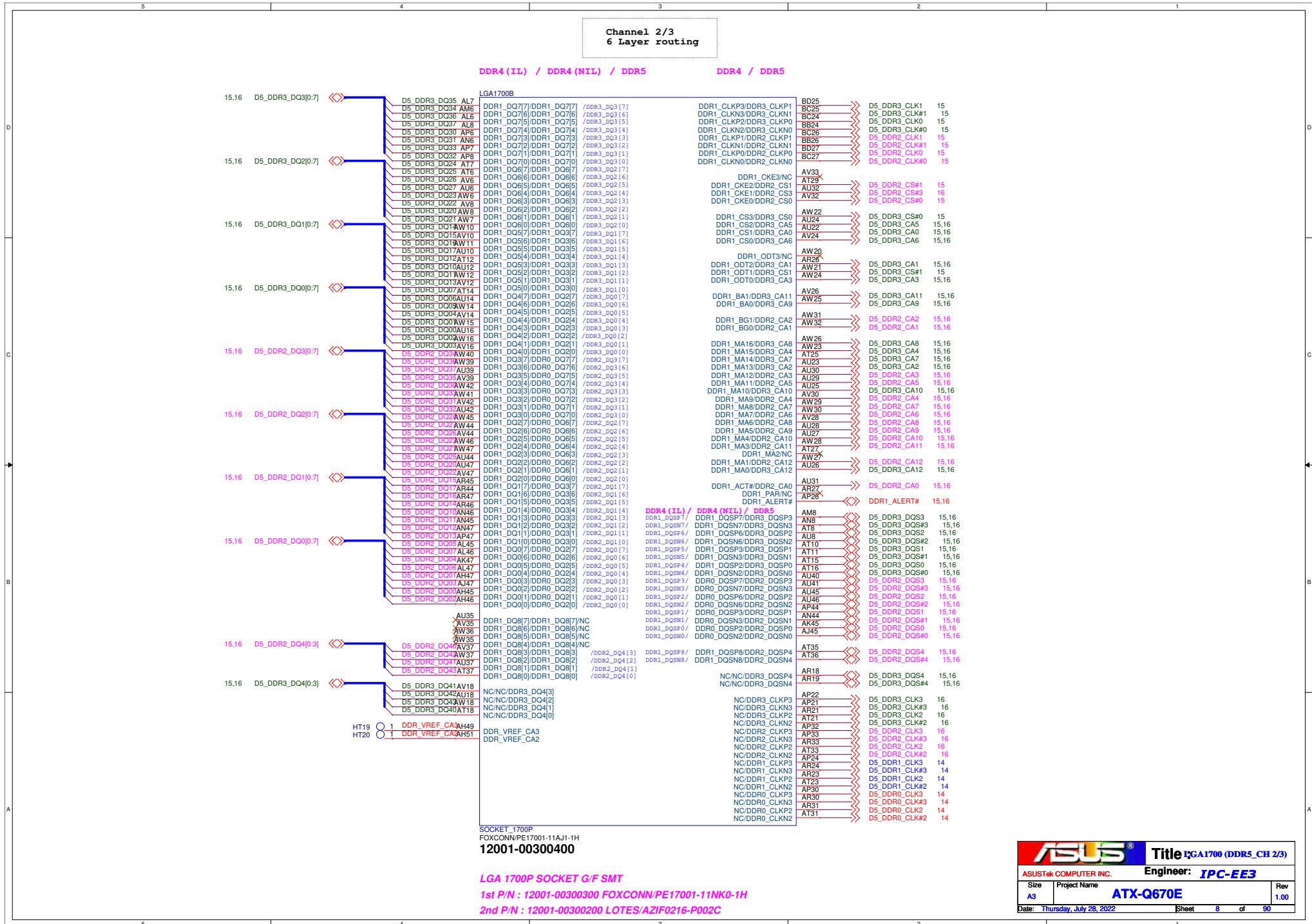
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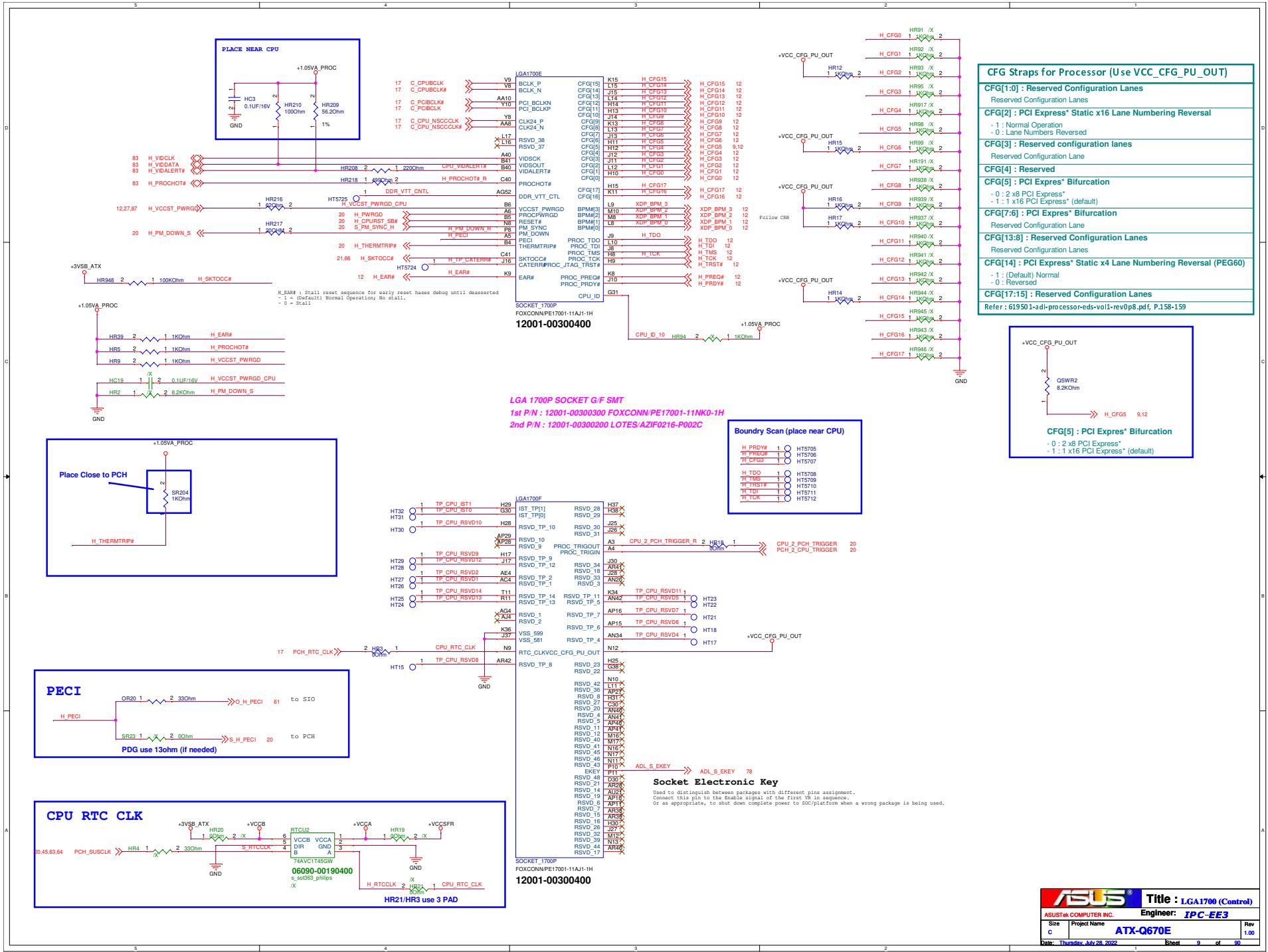
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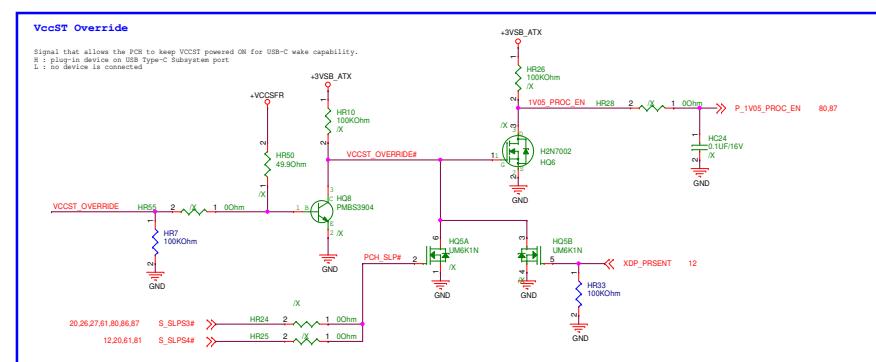
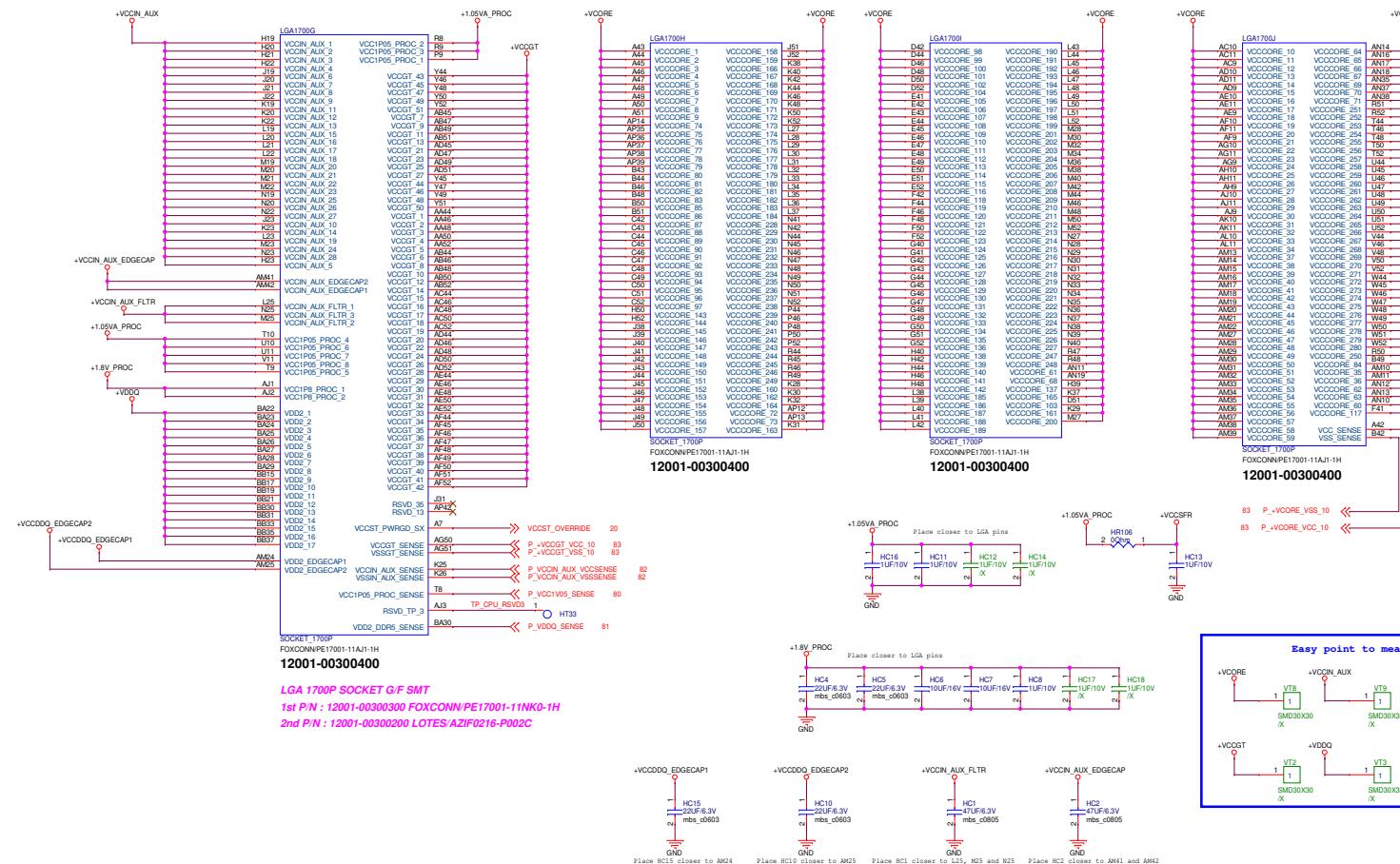


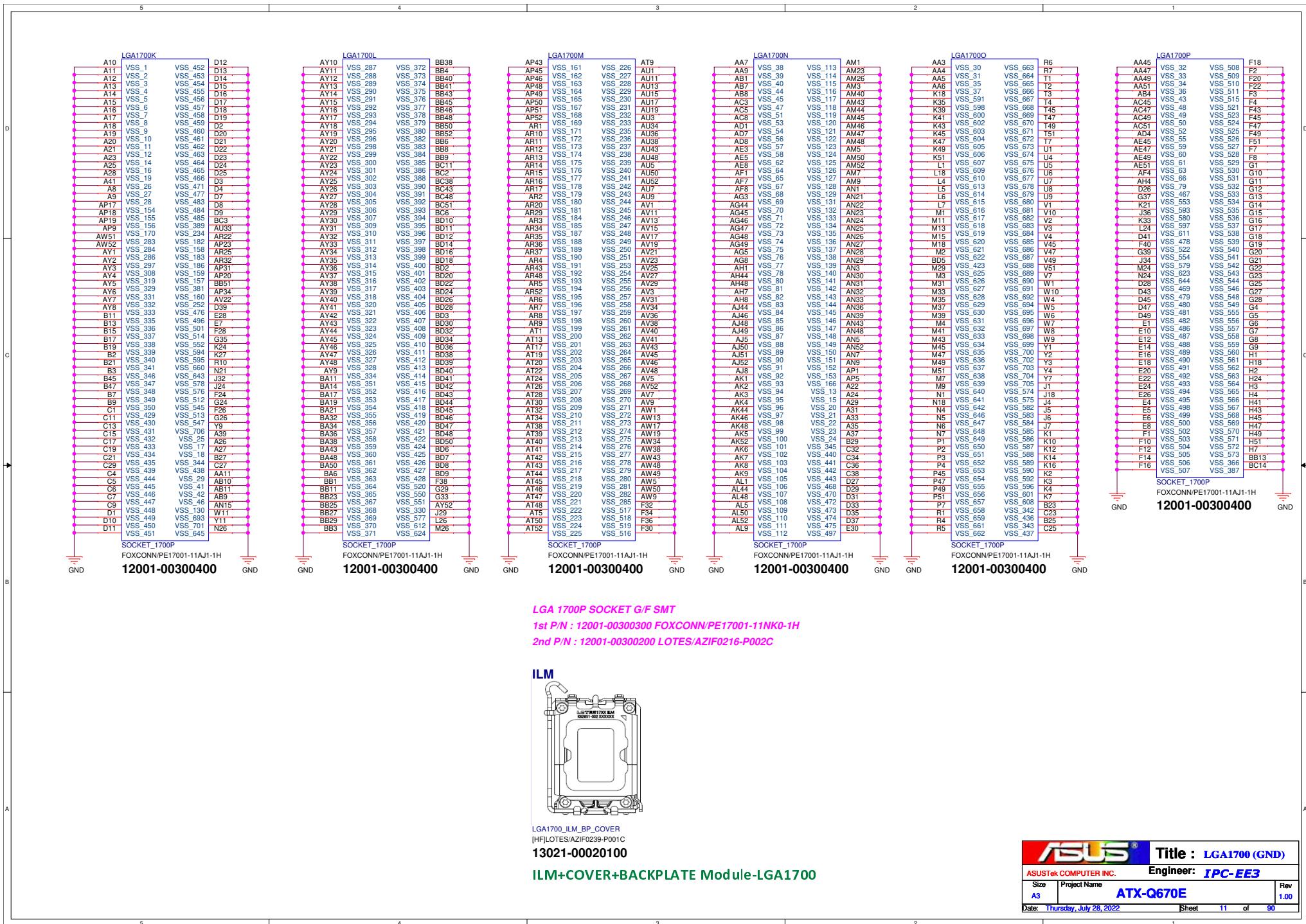


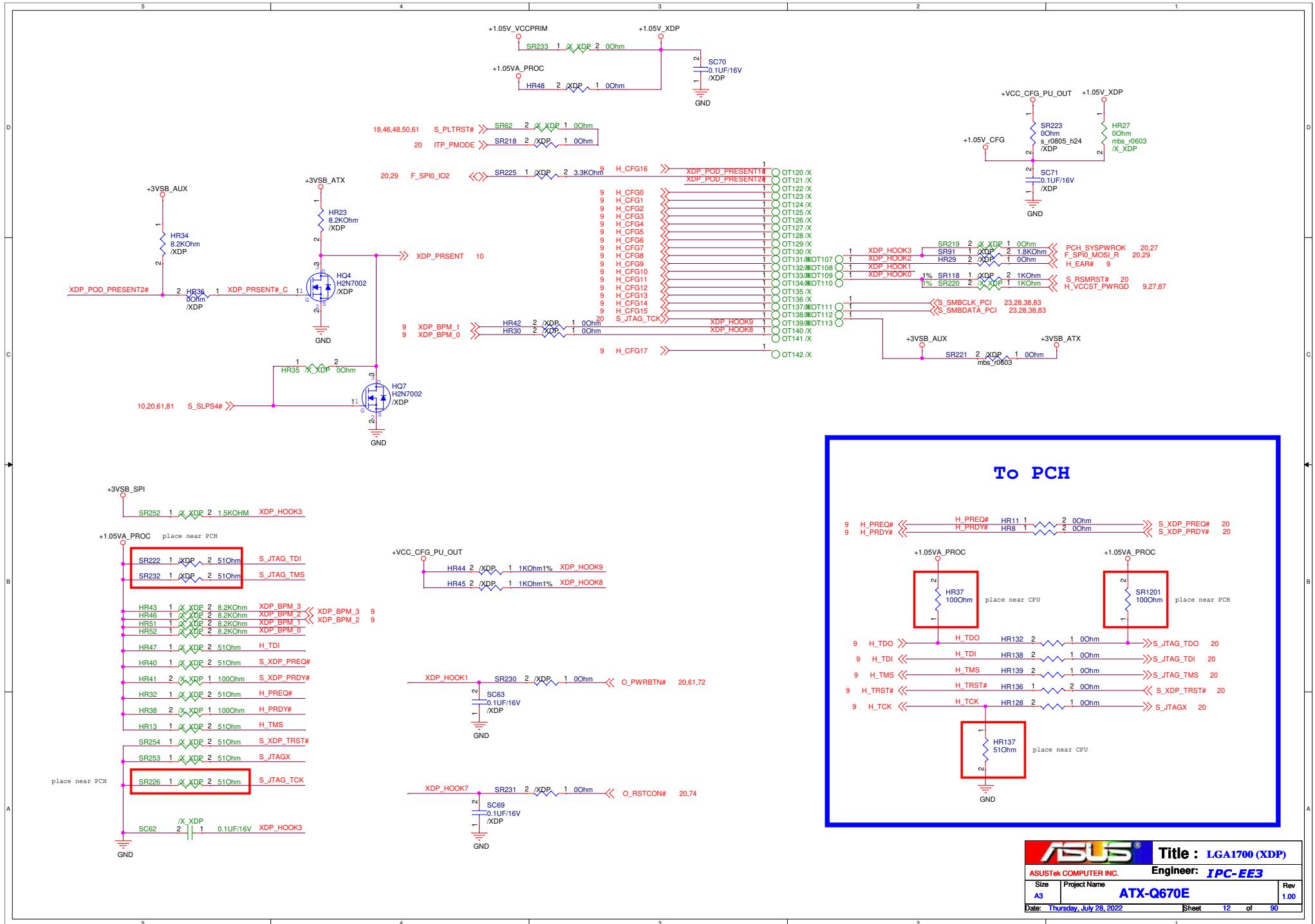


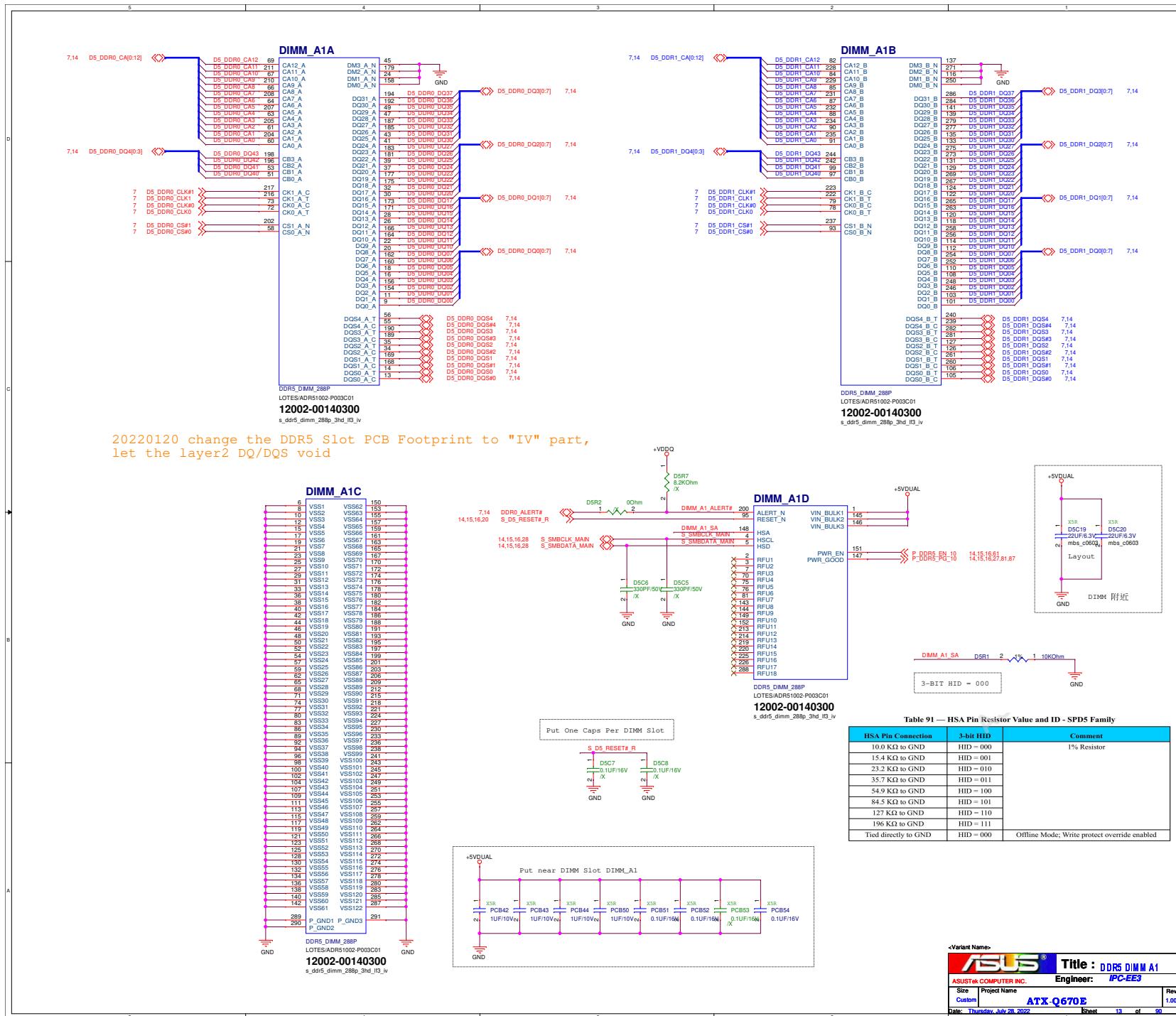


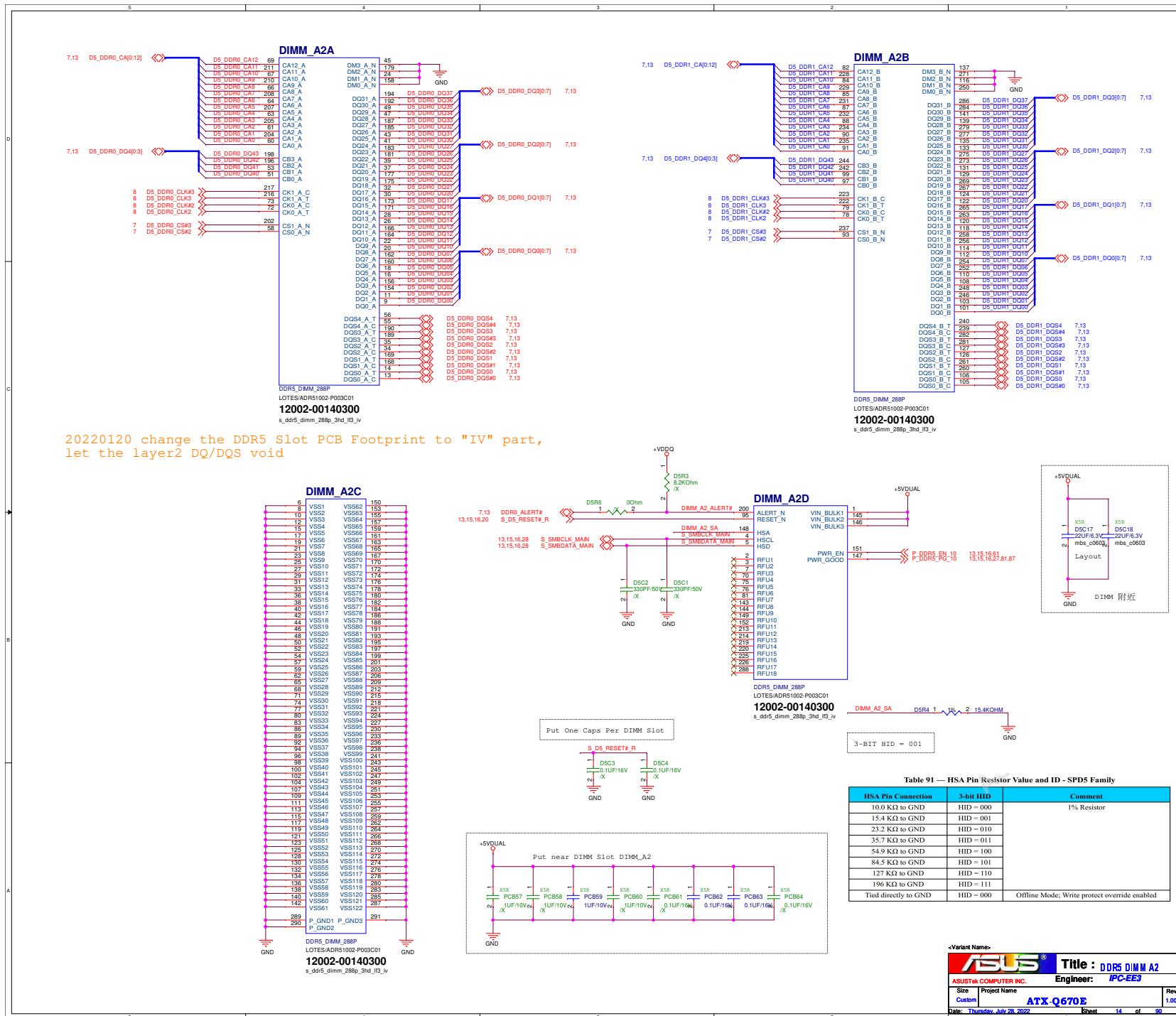


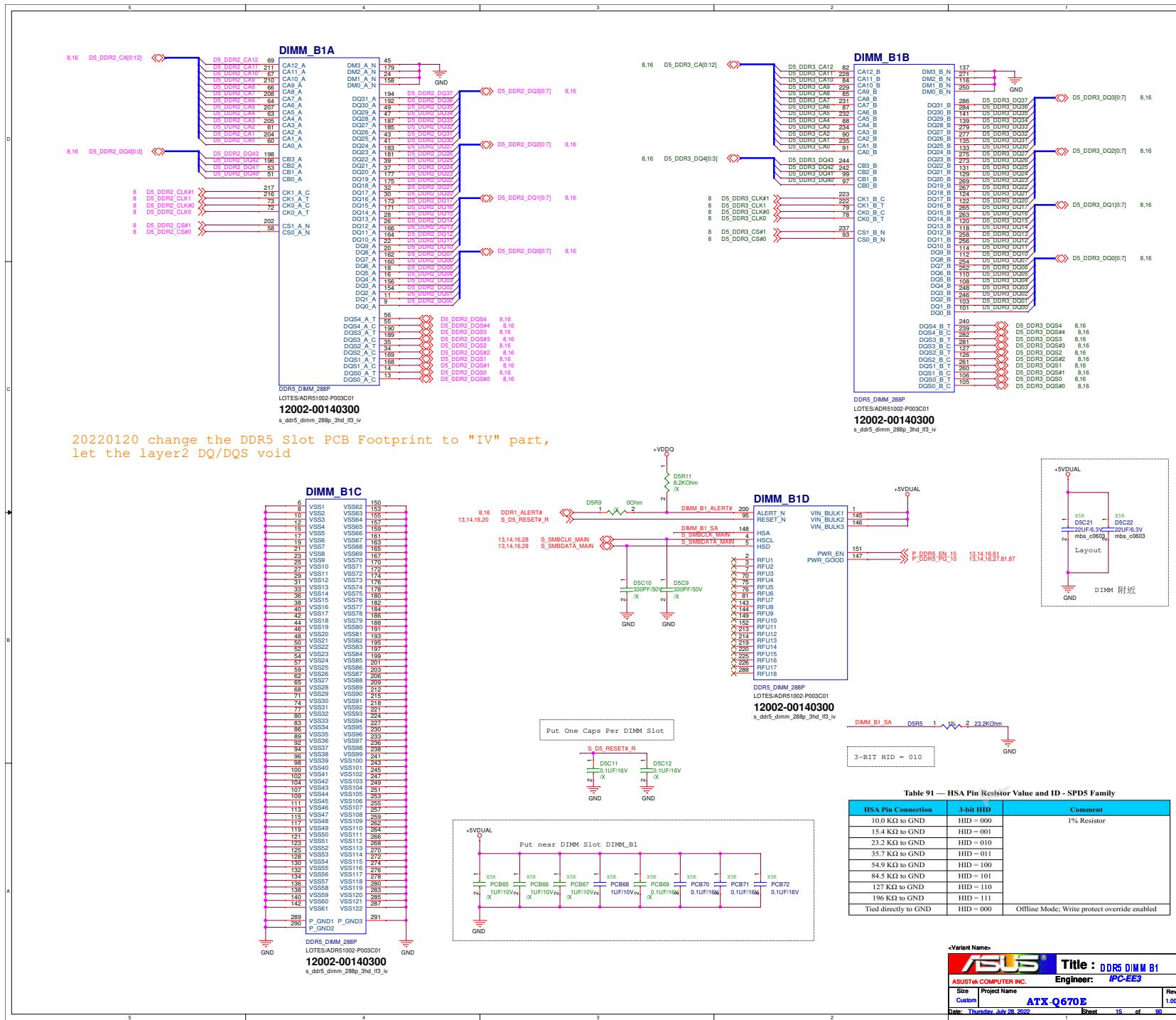


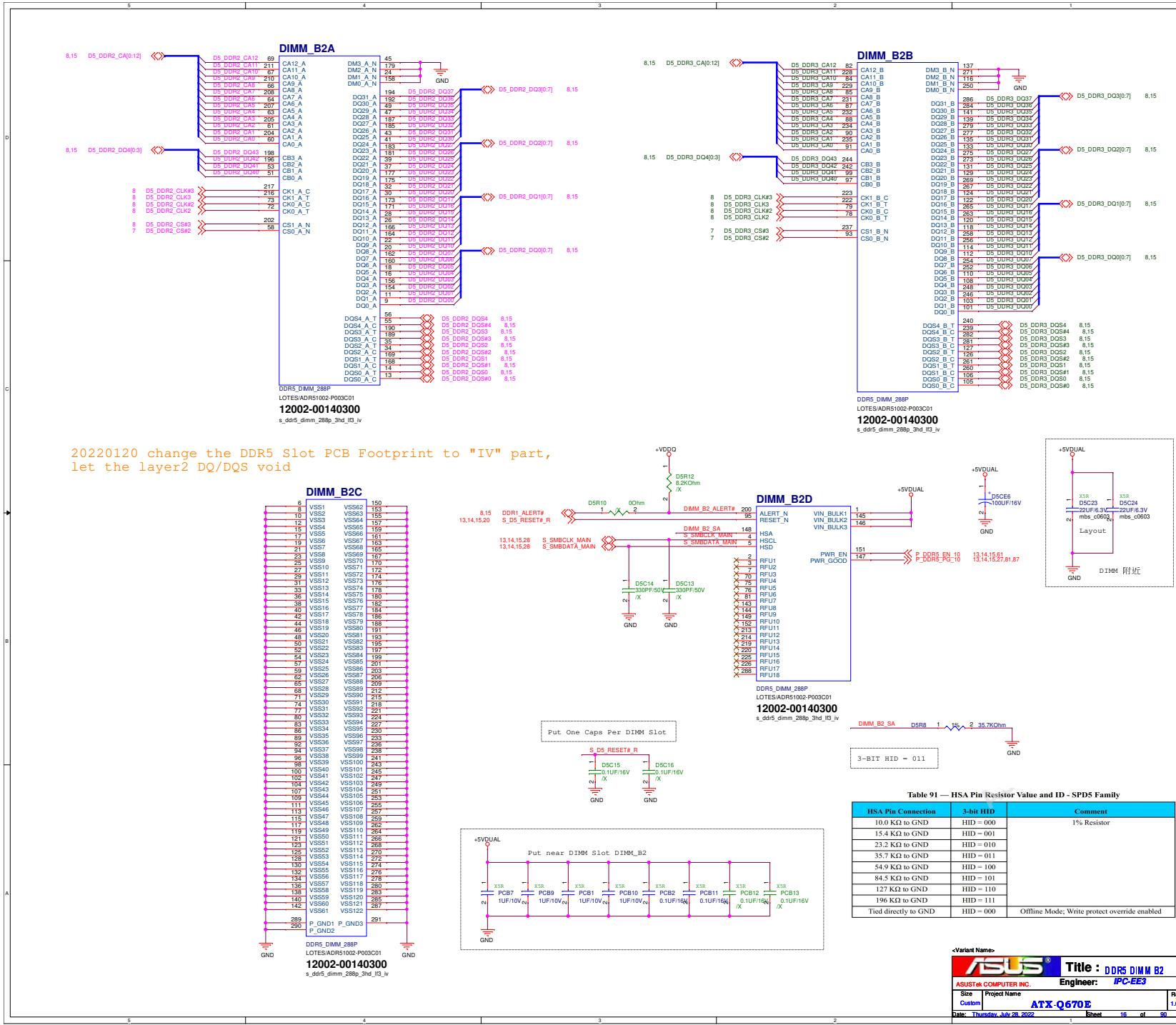


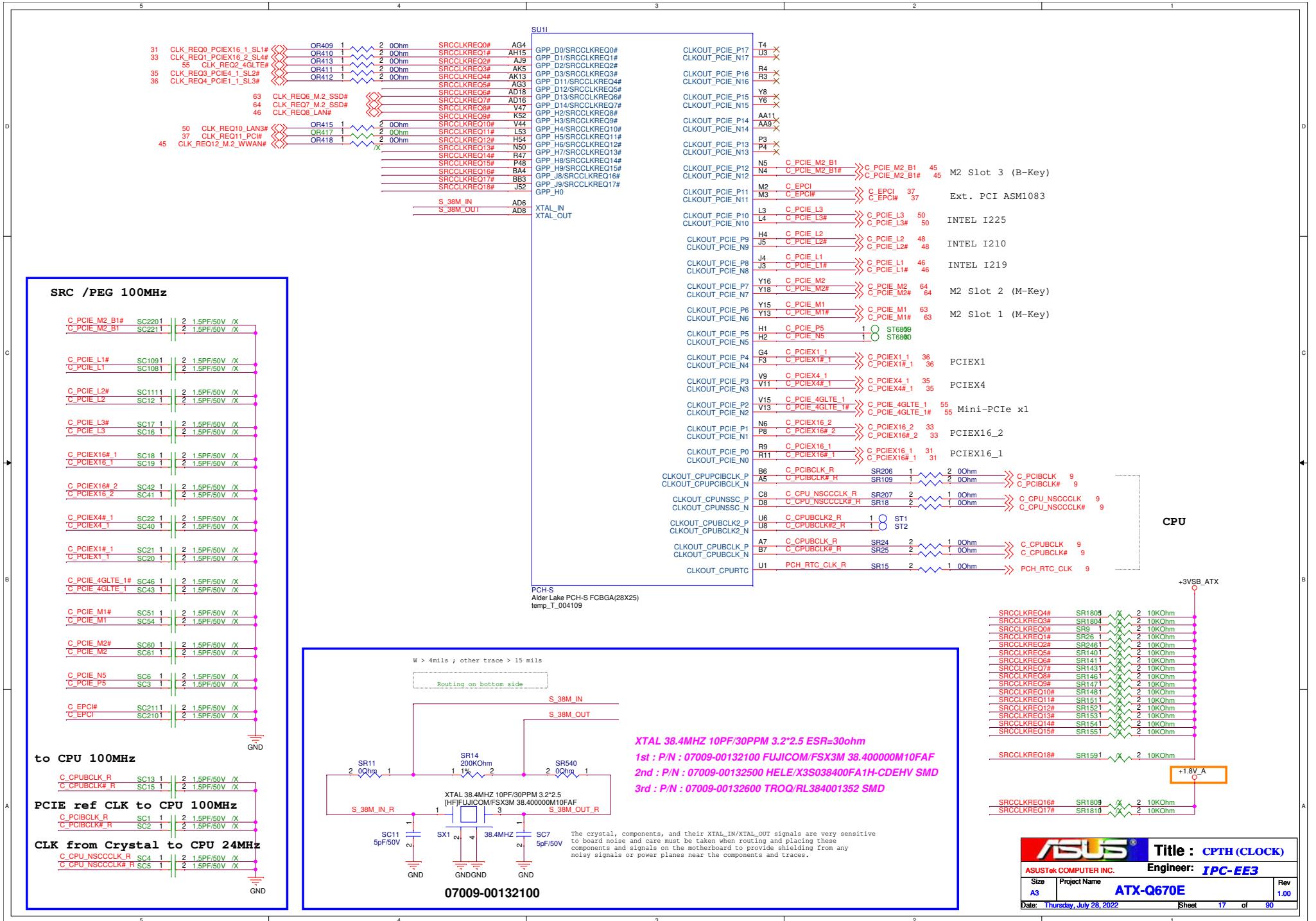


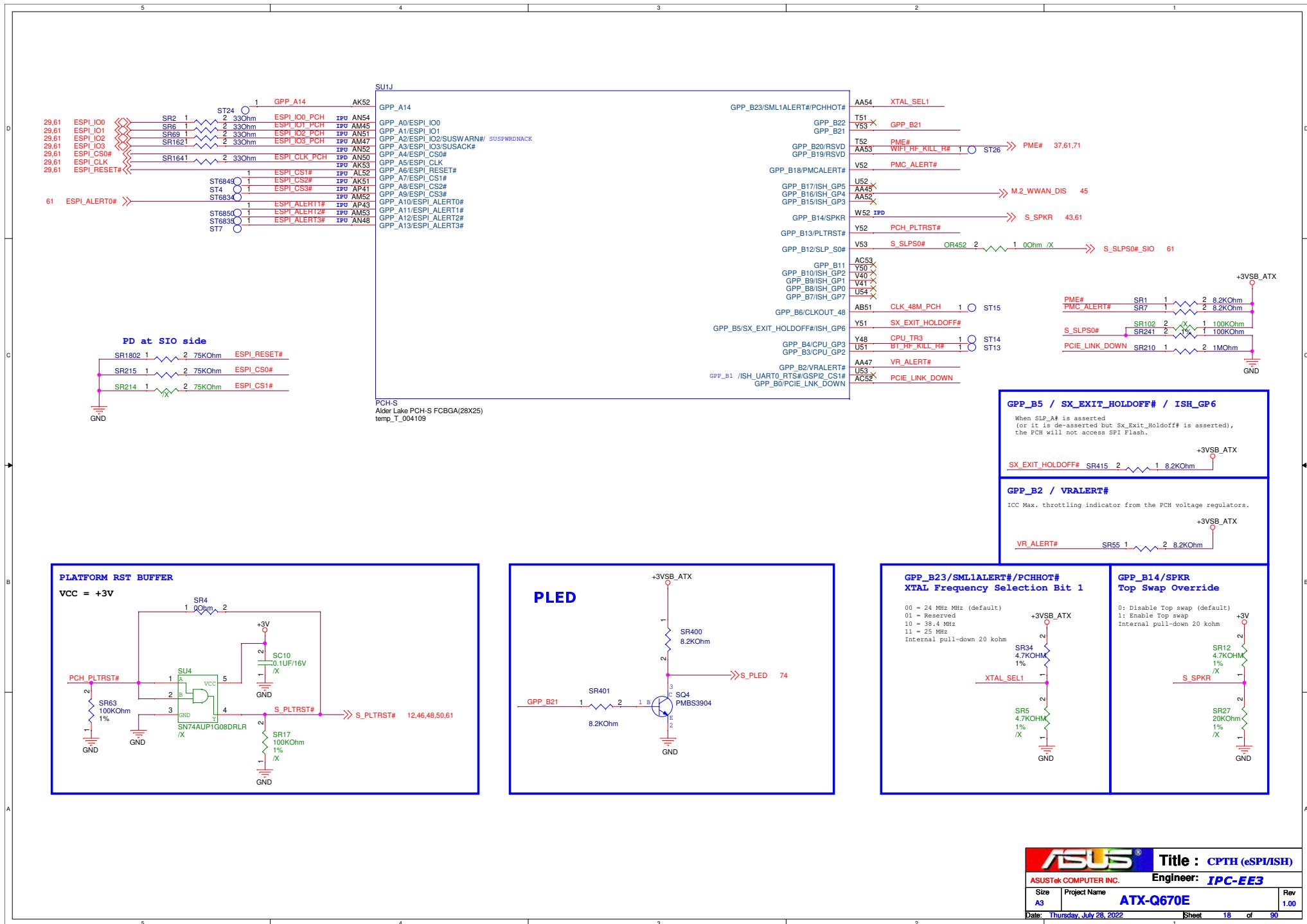


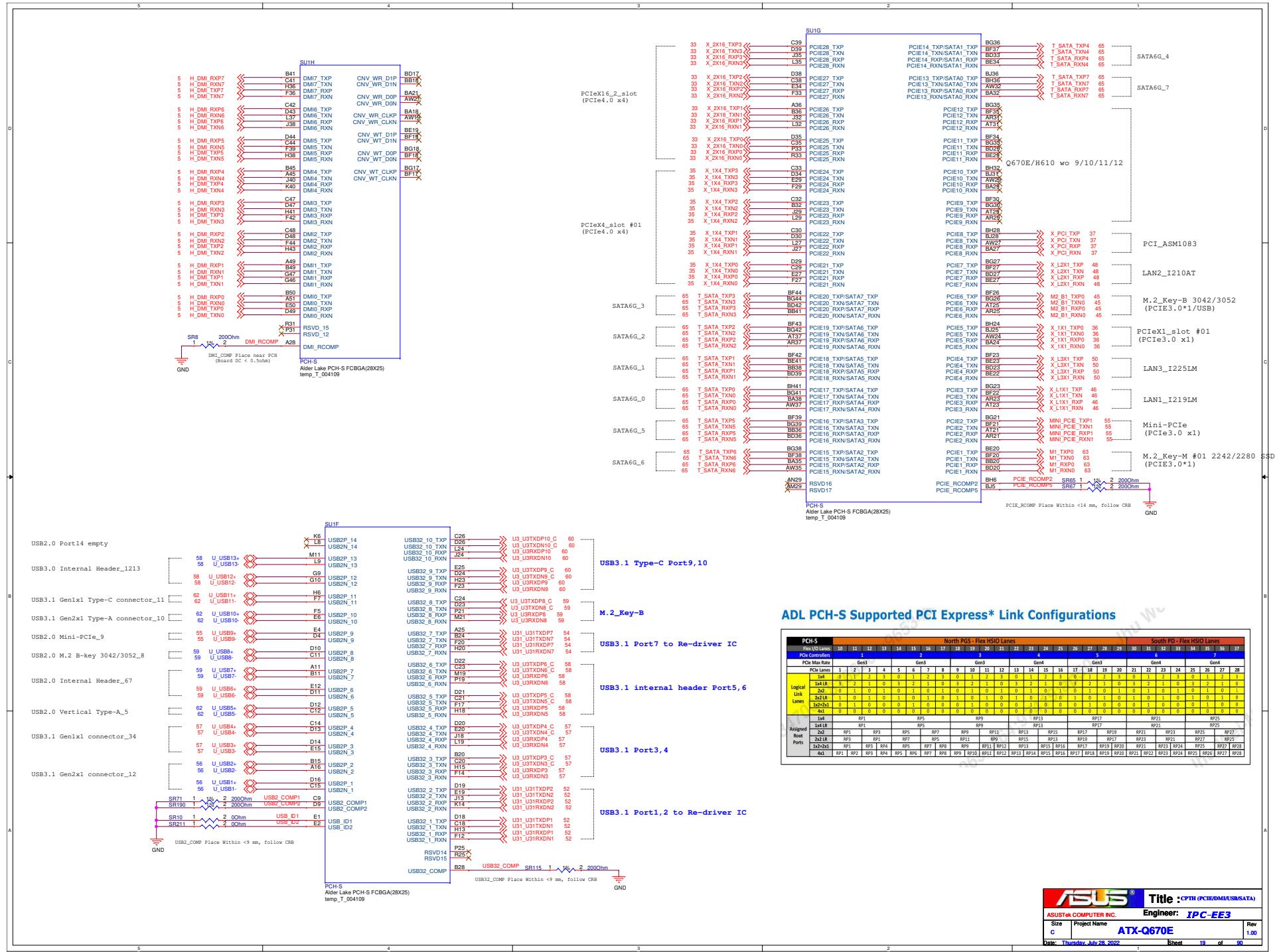


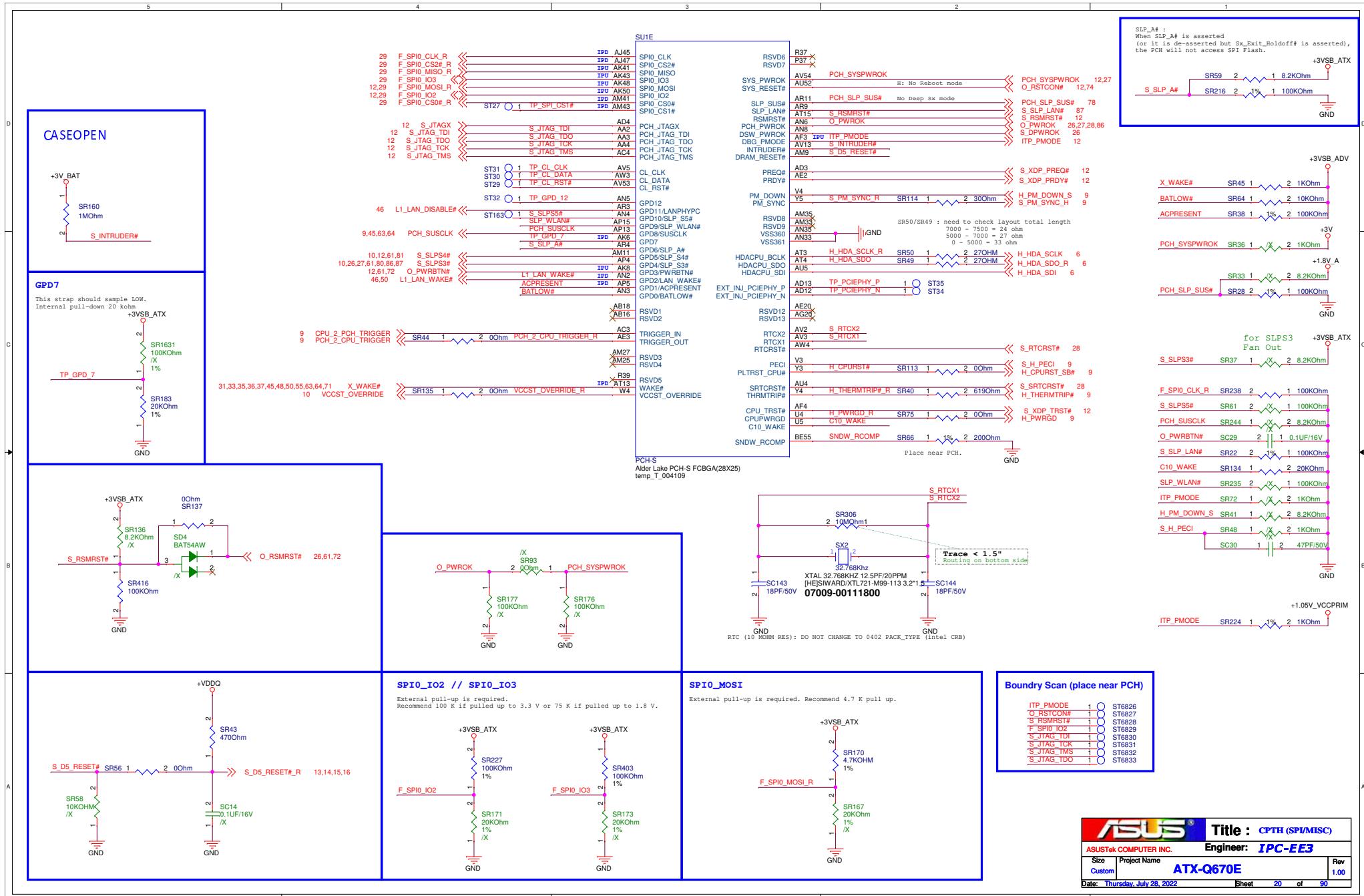


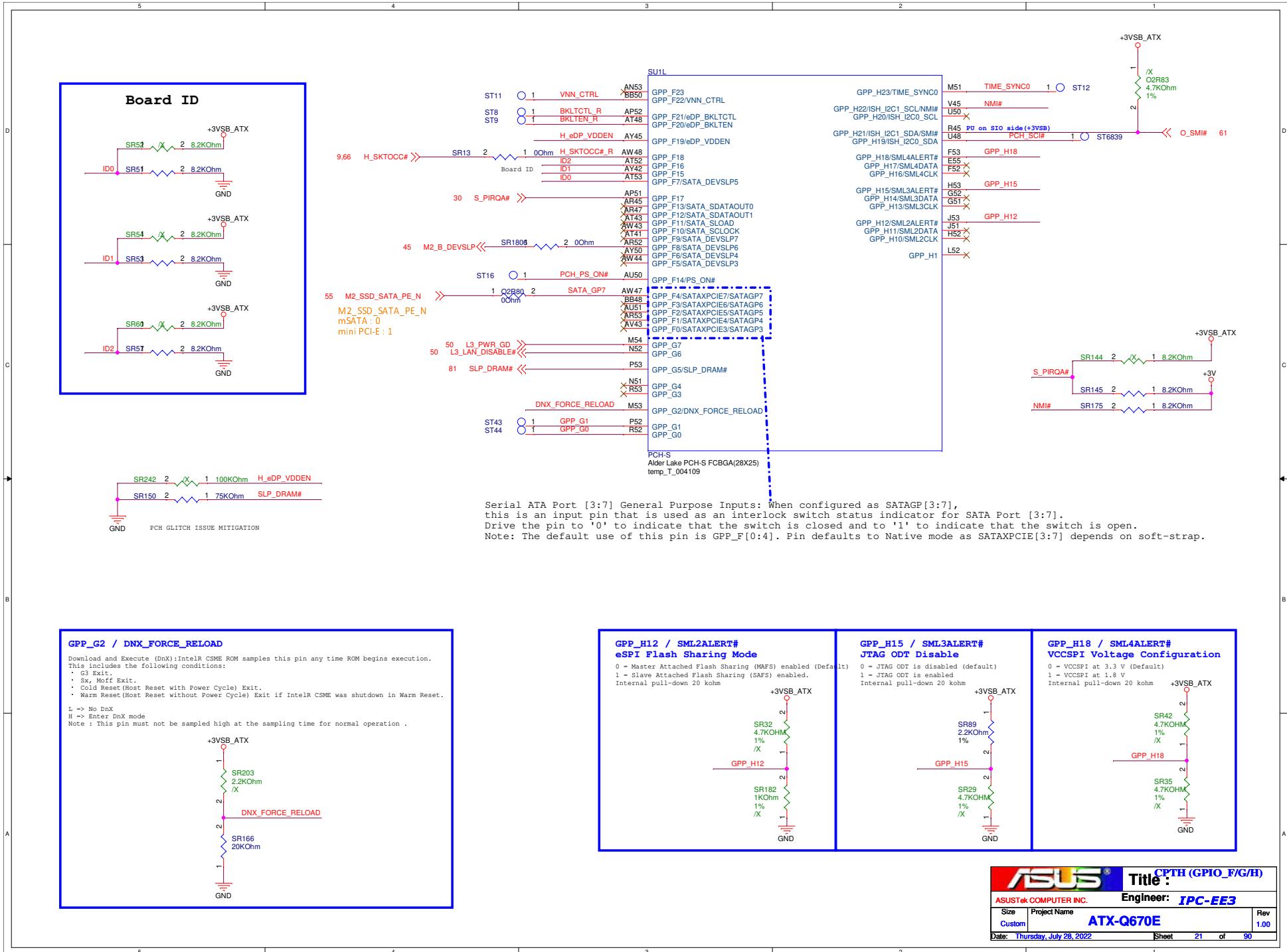


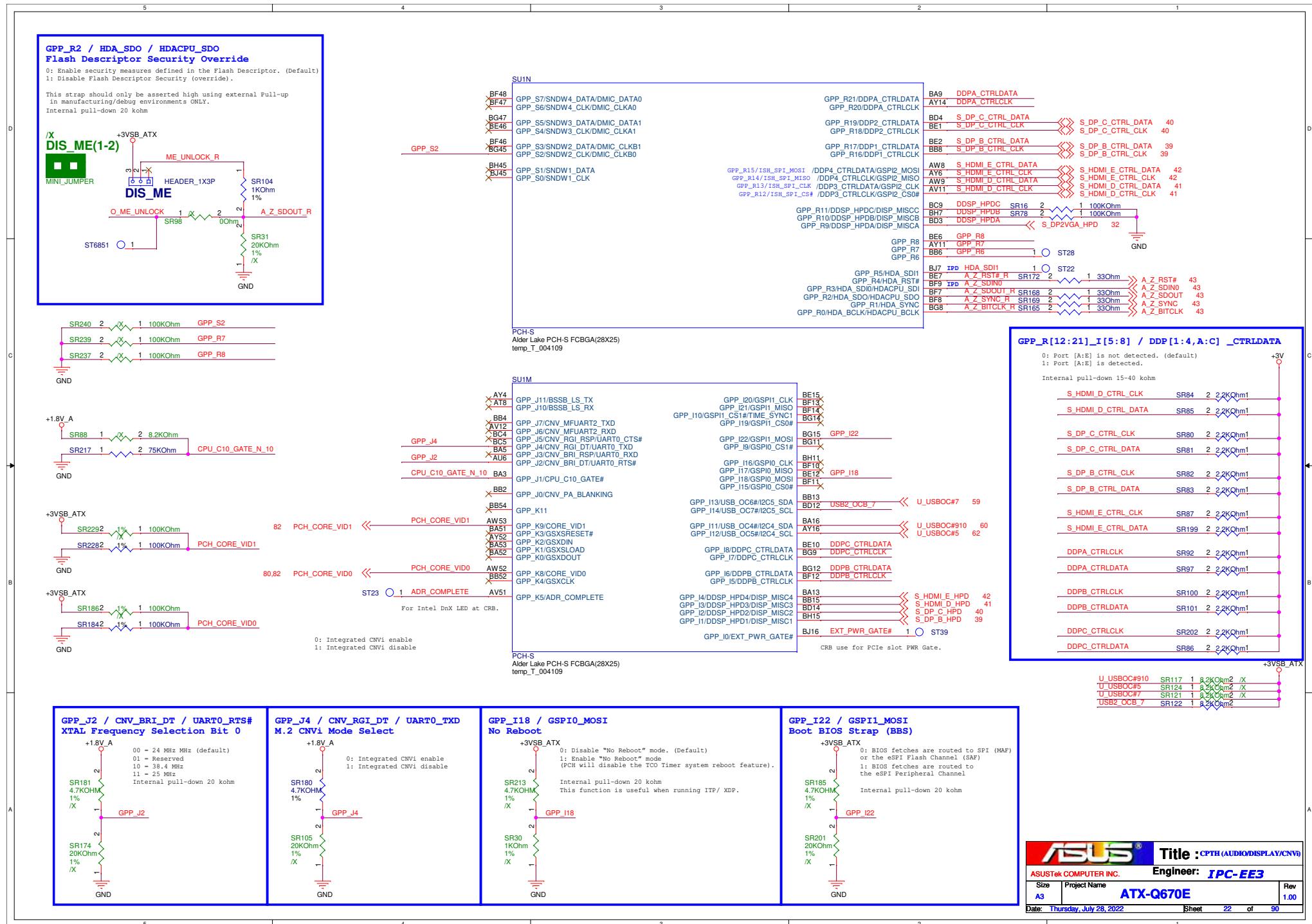


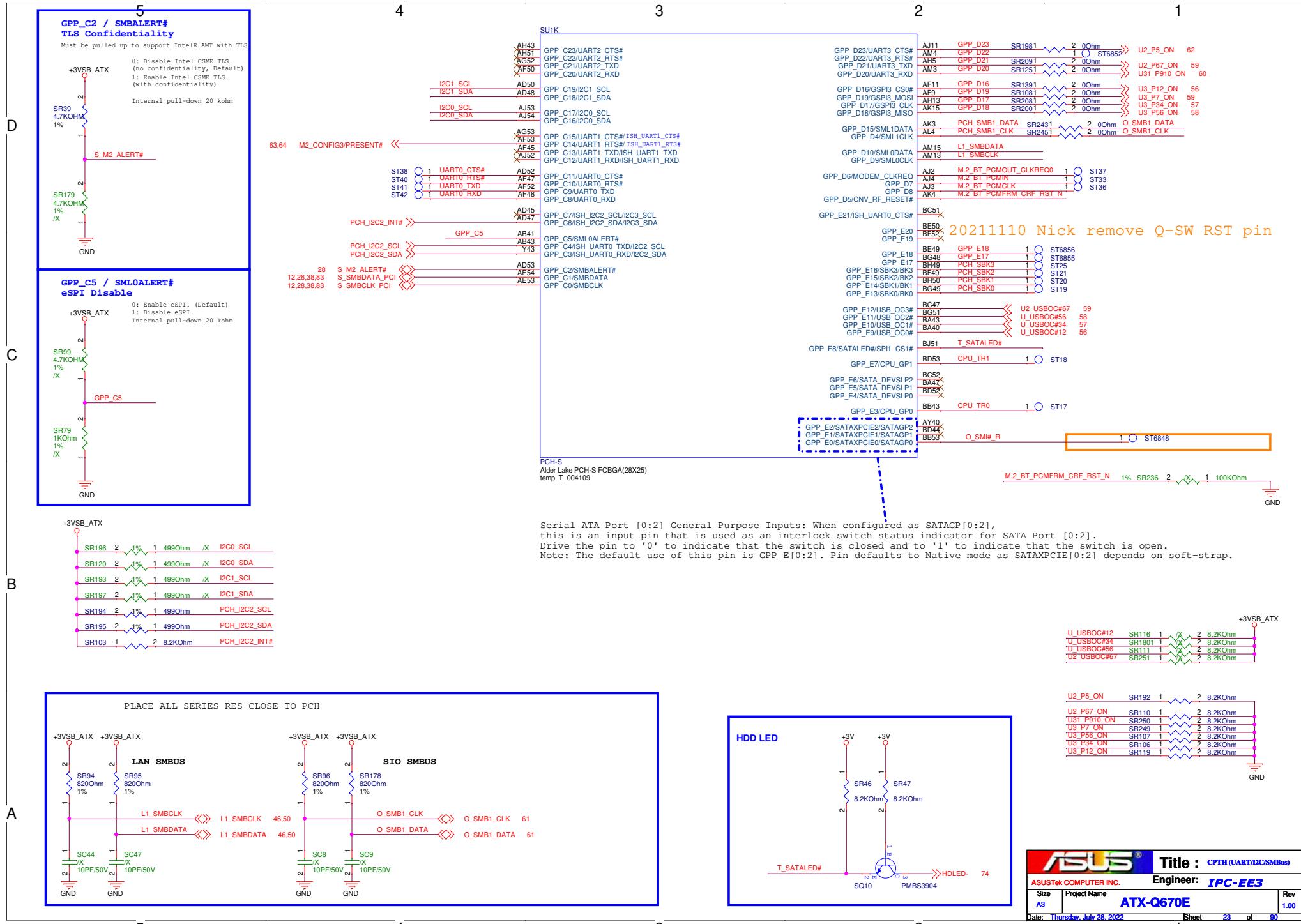


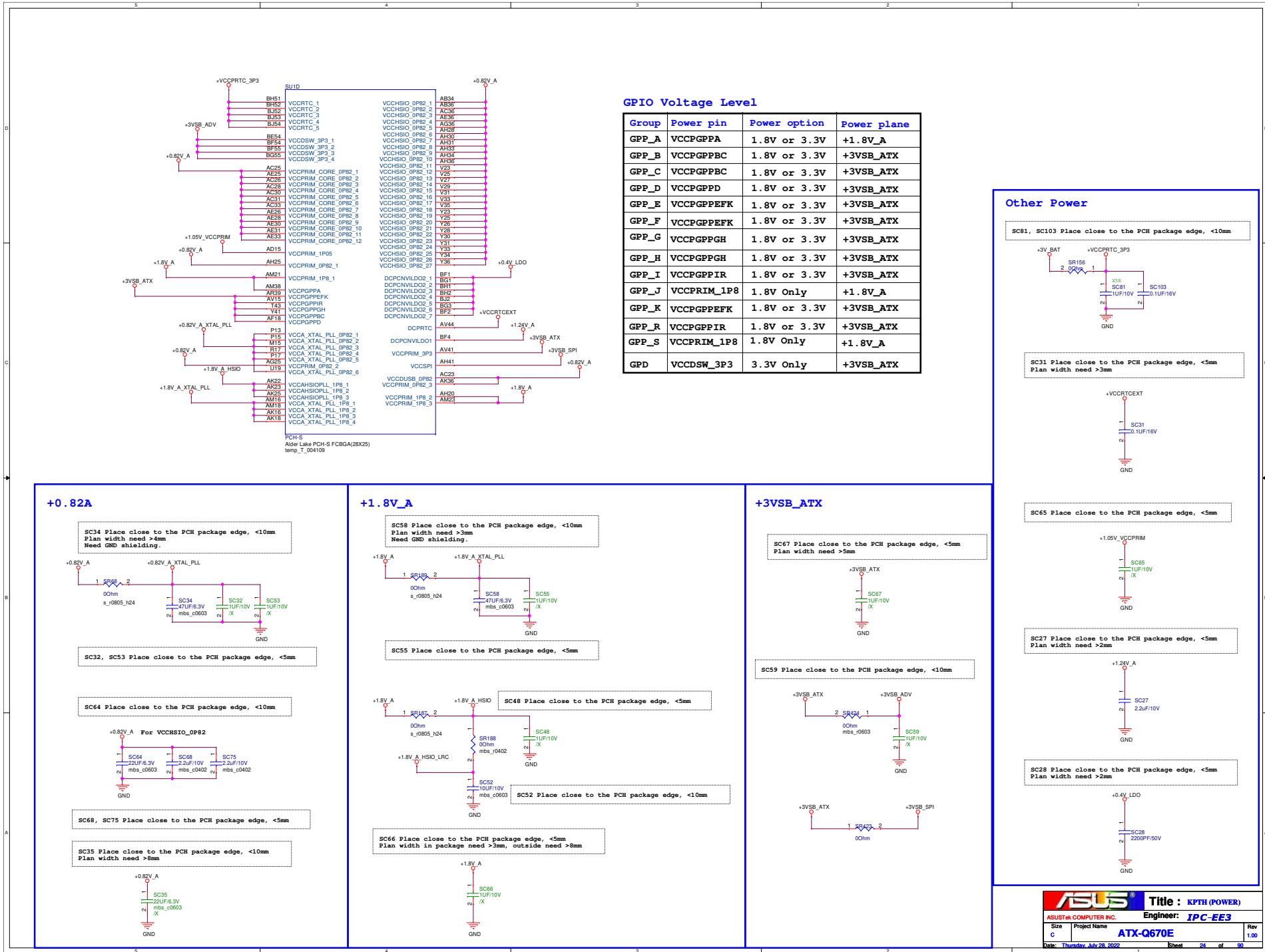


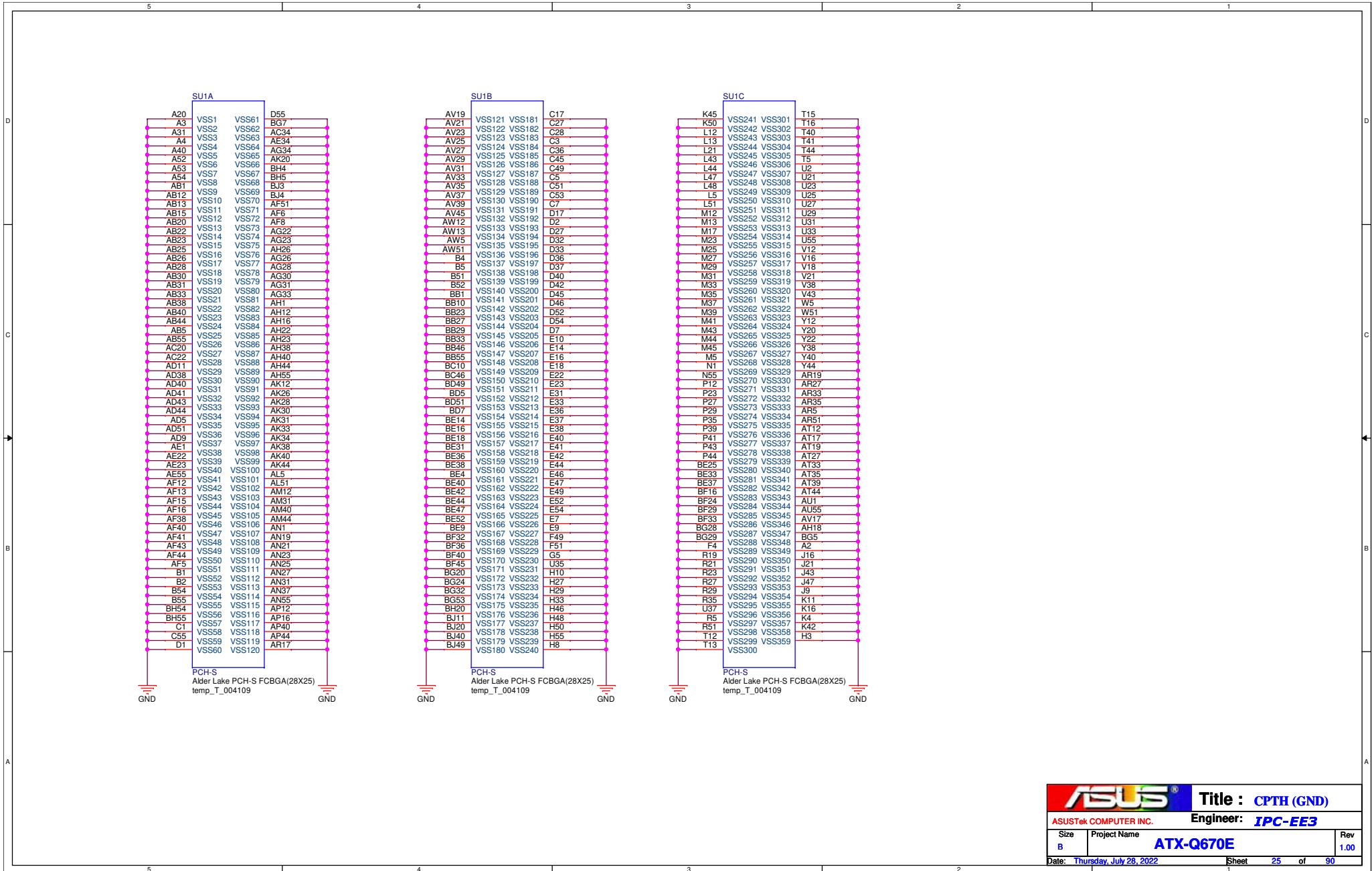


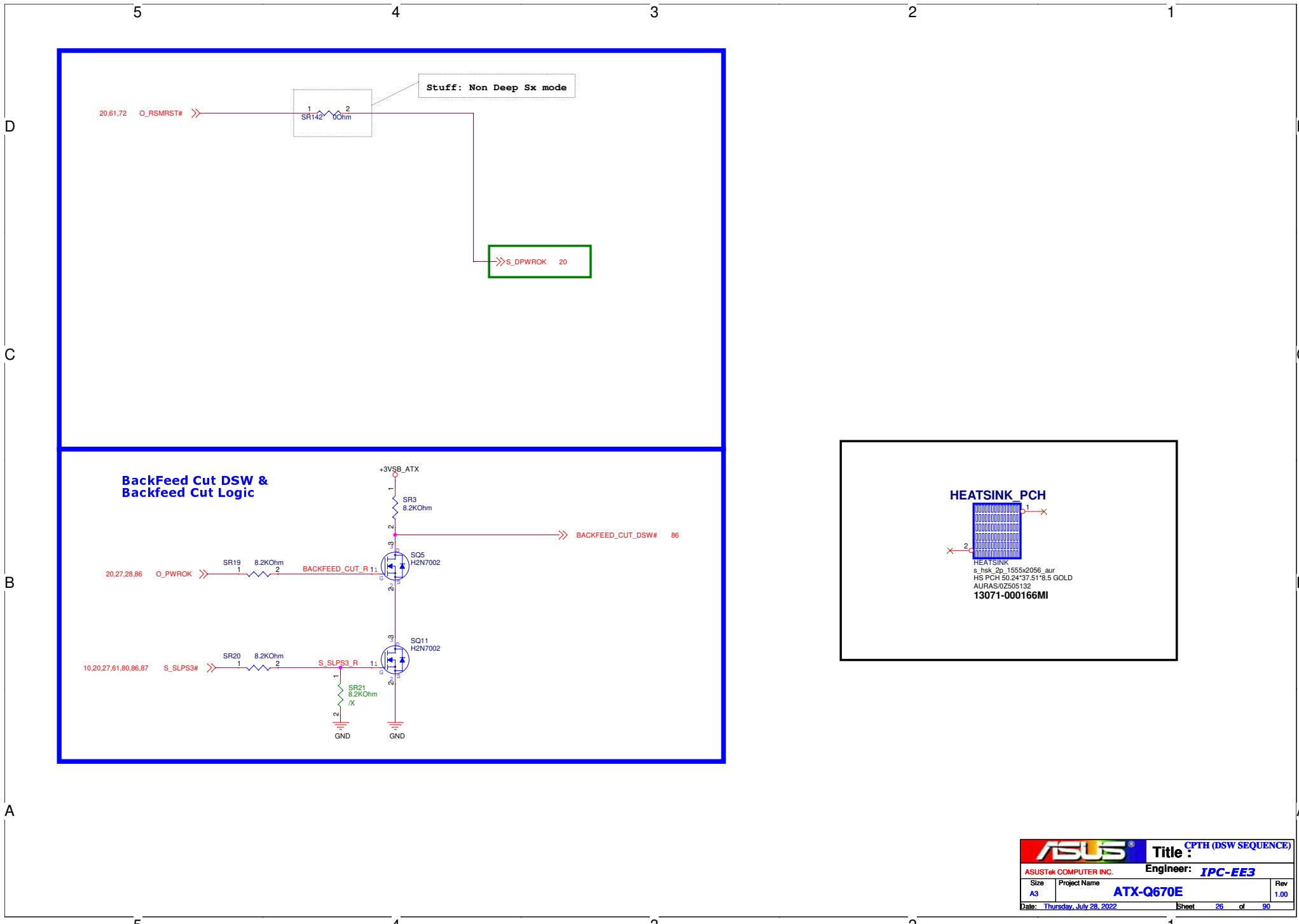


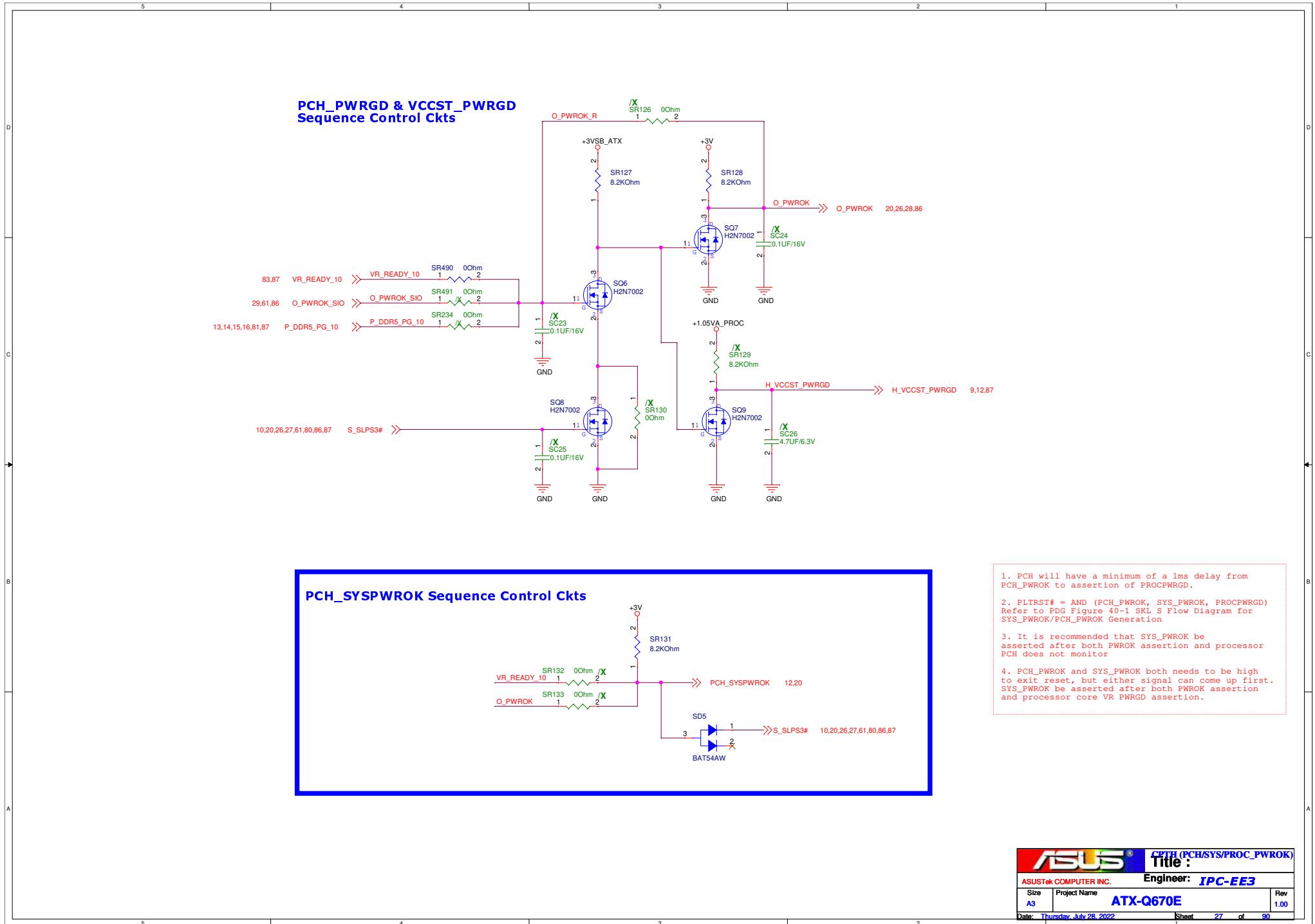


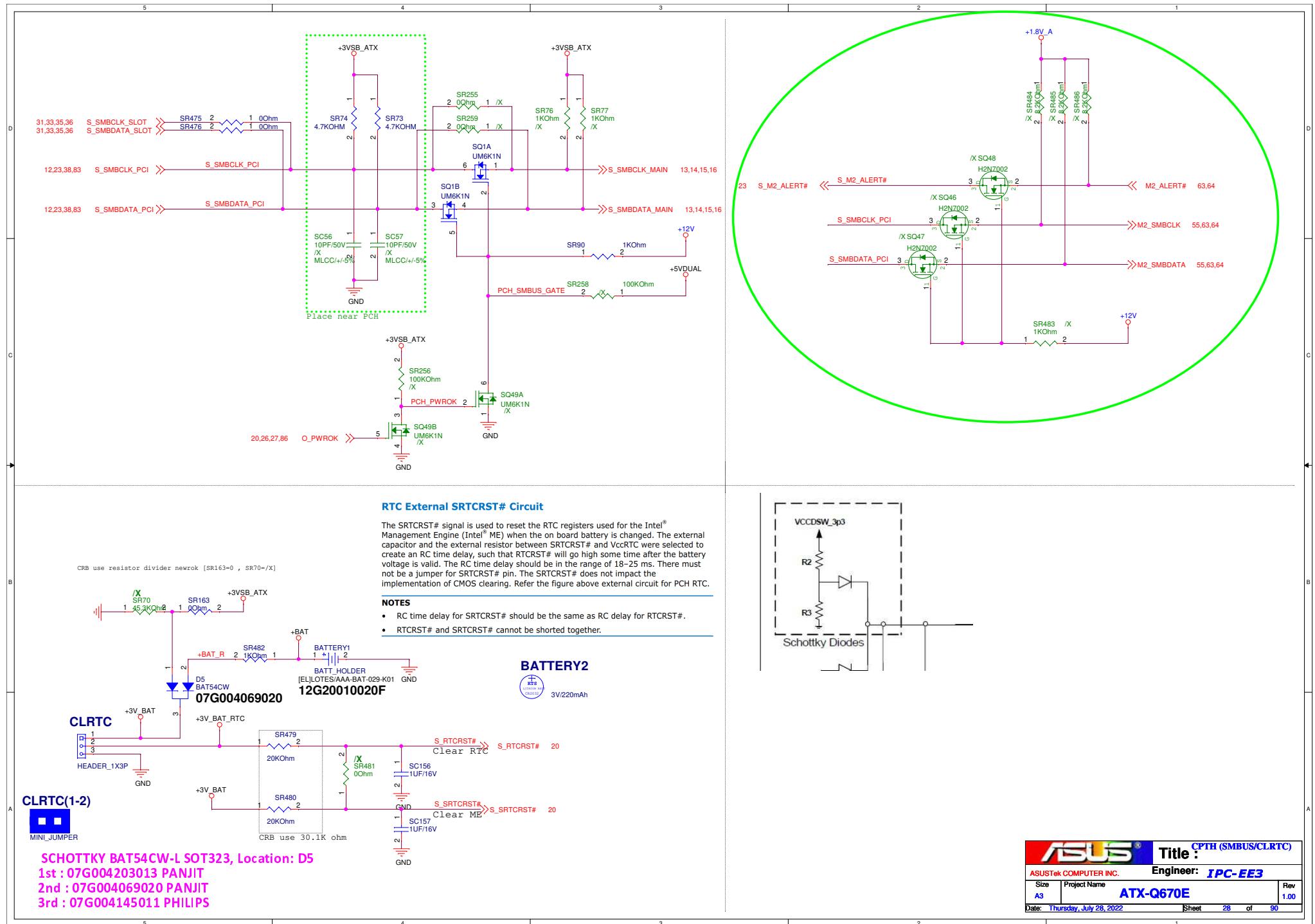


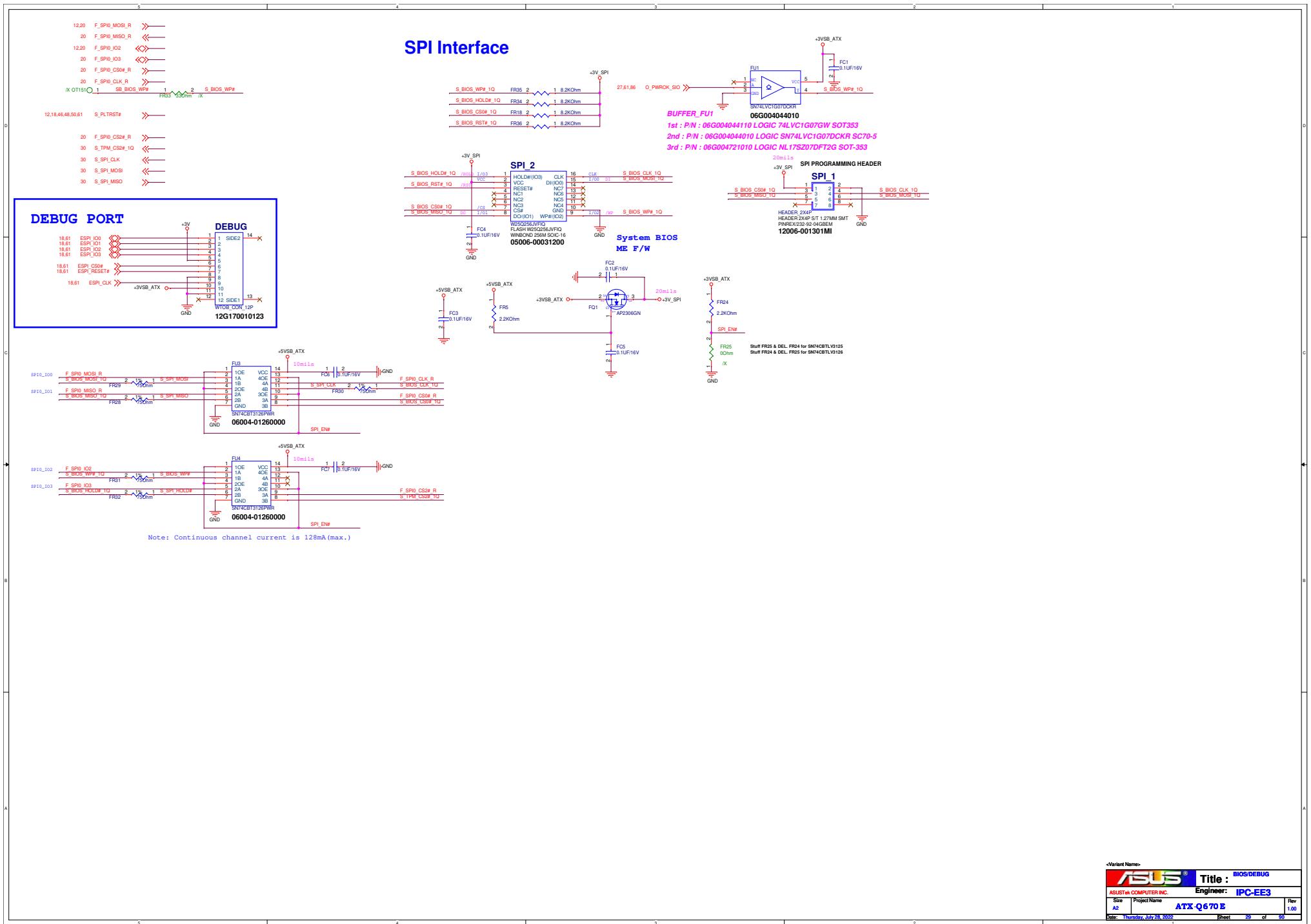


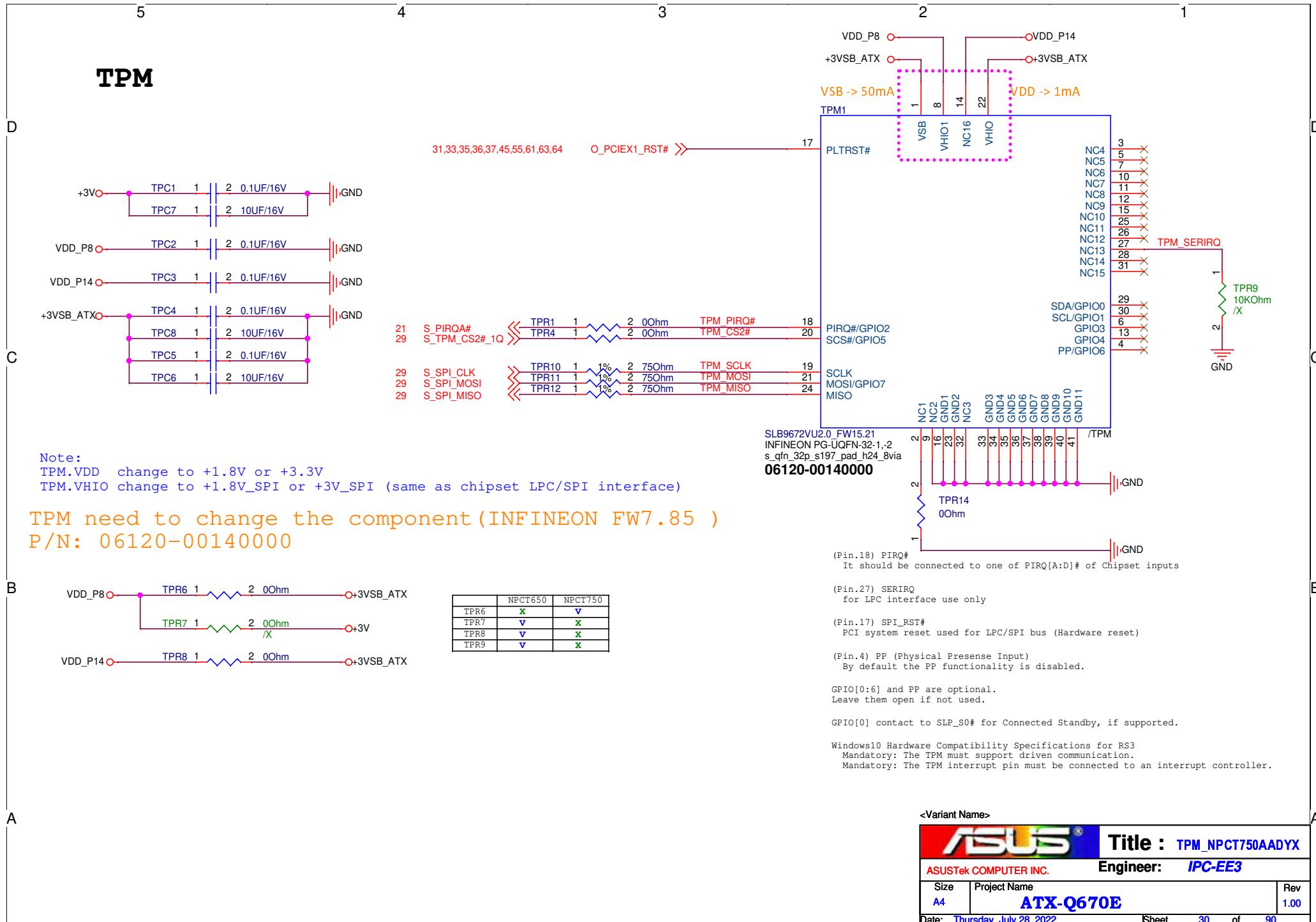






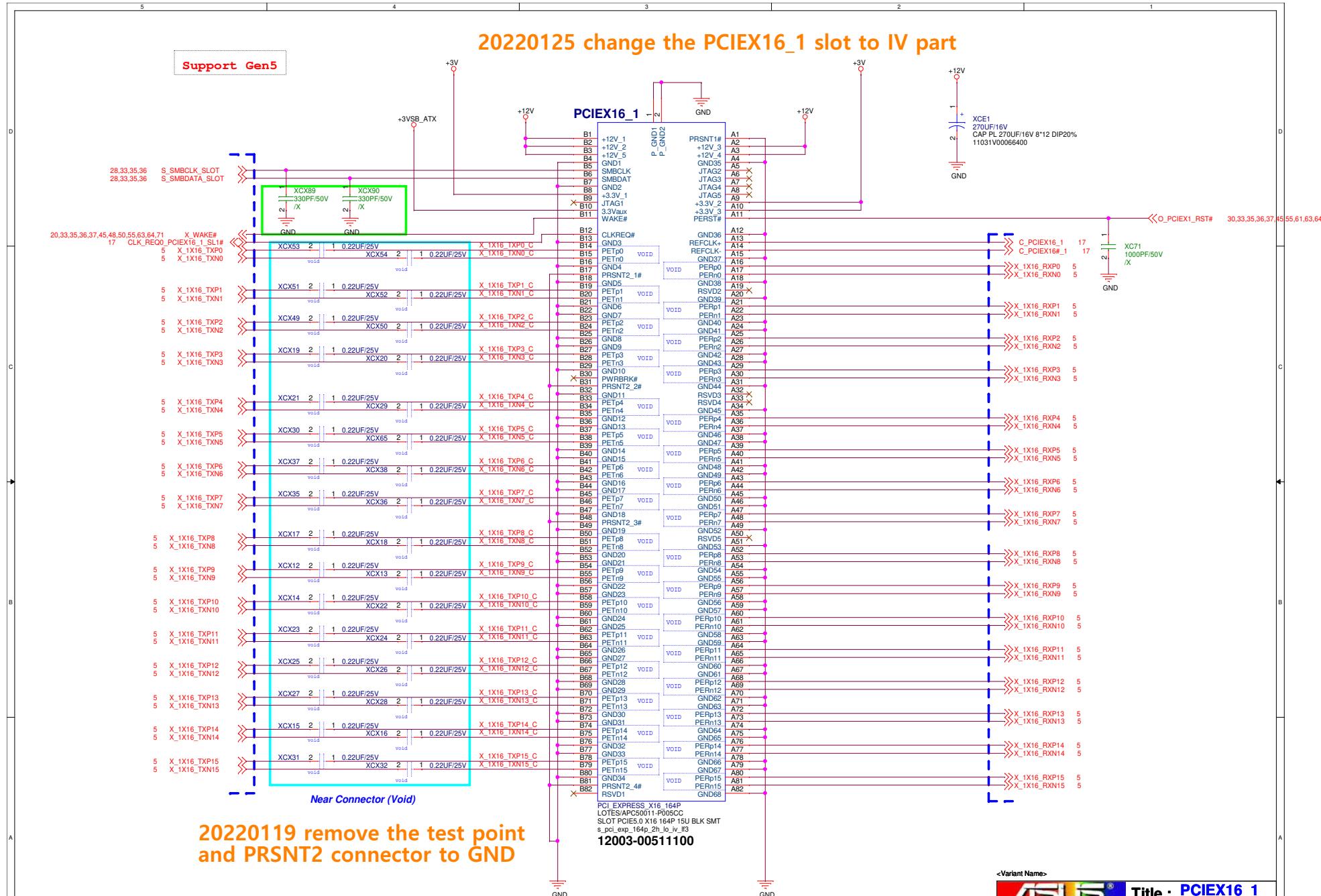






20220125 change the PCIEX16_1 slot to IV part

Support Gen5



20220119 remove the test point and PRSNT2 connector to GND

s_pci_exp_164p_2h_lo_iv_if3
12003-00511100

Variant Name



Title : PCIEX16_1

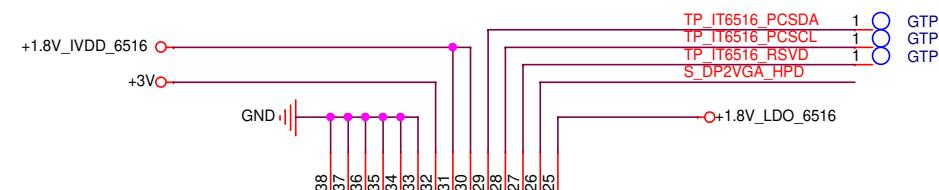
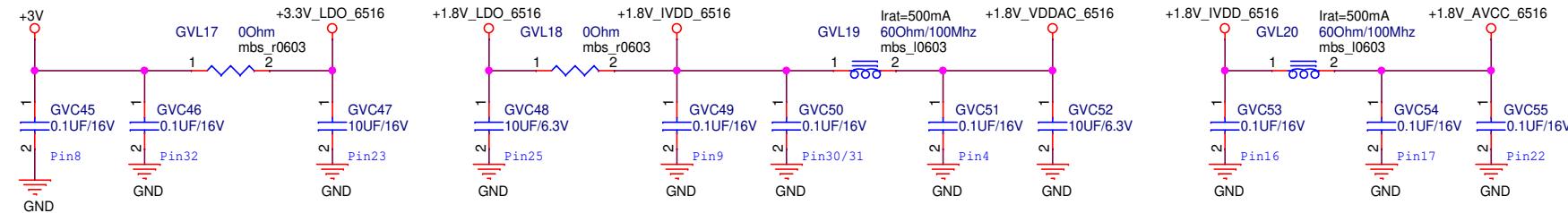
Page 1

ASUSTek COMPUTER INC. Engineer: IPC-EE3

| | | |
|--------|------------------|------|
| Size | Project Name | Re |
| Custom | ATX-Q670E | 1.00 |

Date: Thursday, July 28, 2022 Sheet 31 of 90

IT6516B Power Caps and Beads



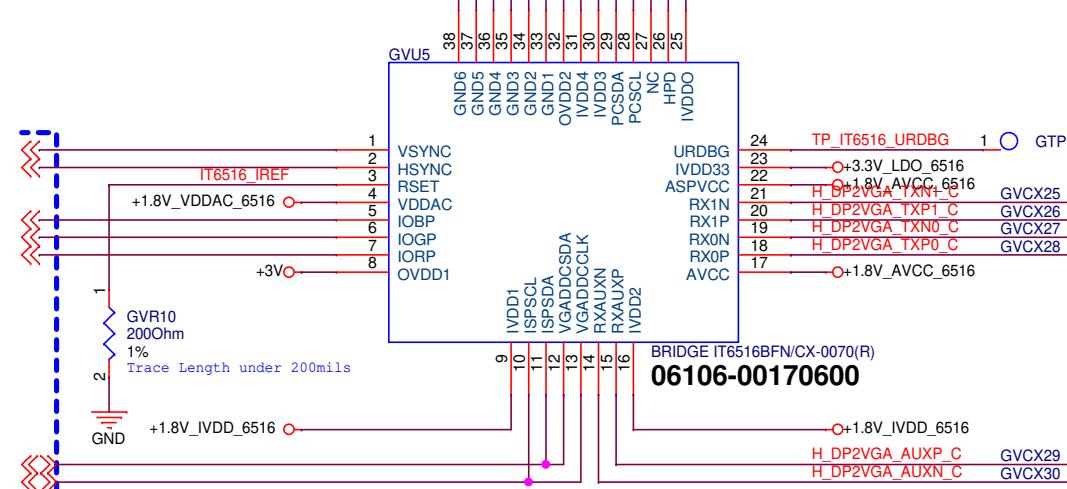
Voltage Level +3.3V

Circuit diagram for S_DP2VGA_HPD:

- The pin is connected to a blue resistor labeled "GVR9 100KOhm".
- The other end of the resistor is connected to GND.
- The pin is also connected to a red wire labeled "S_DP2VGA_HPD" which extends to the right.

```
34     VGA_VSYNC  
34     VGA_HSYNC  
  
34     VGA_BLUE  
34     VGA_GREEN  
34     VGA_RED
```

34 VGA_DDC_DATA
34 VGA_DDC_CLK



BRIDGE IT6516BFN/CX-0070(06106-00170600)

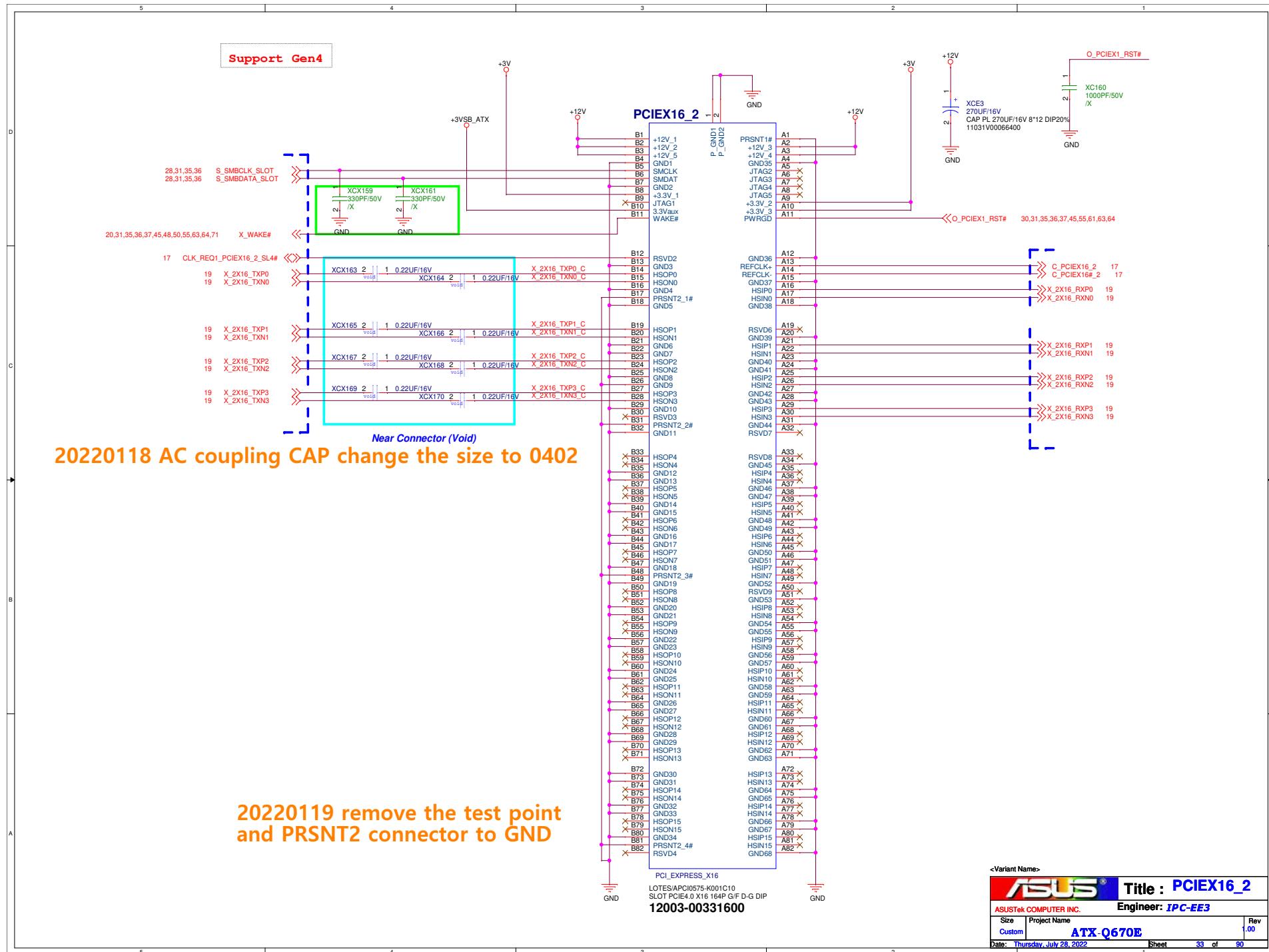
<Variant Name>



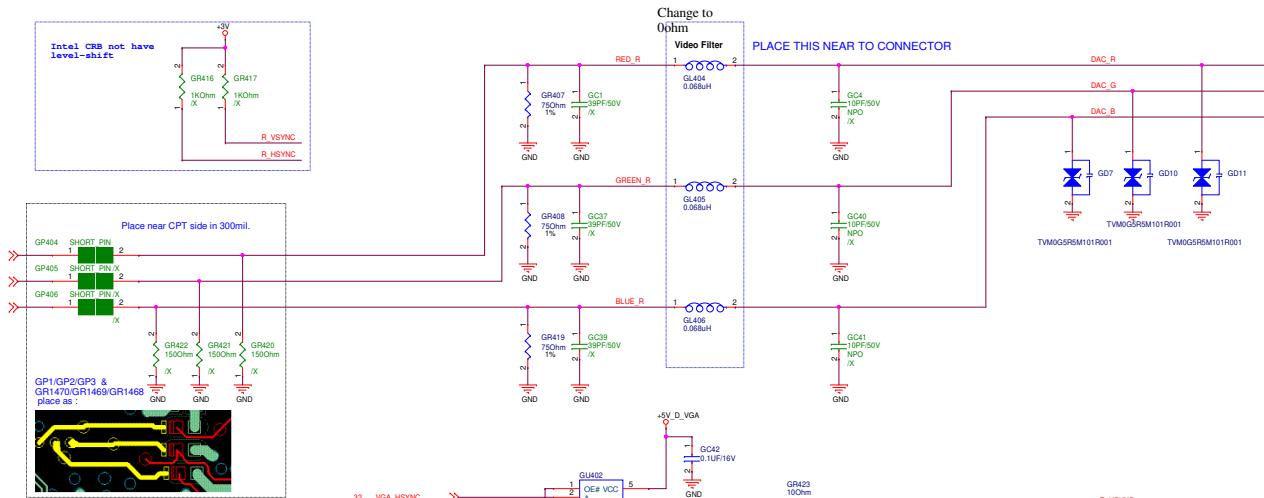
Title :VGA IT6516B (Port A)

—
Engineer: IPC-EE3

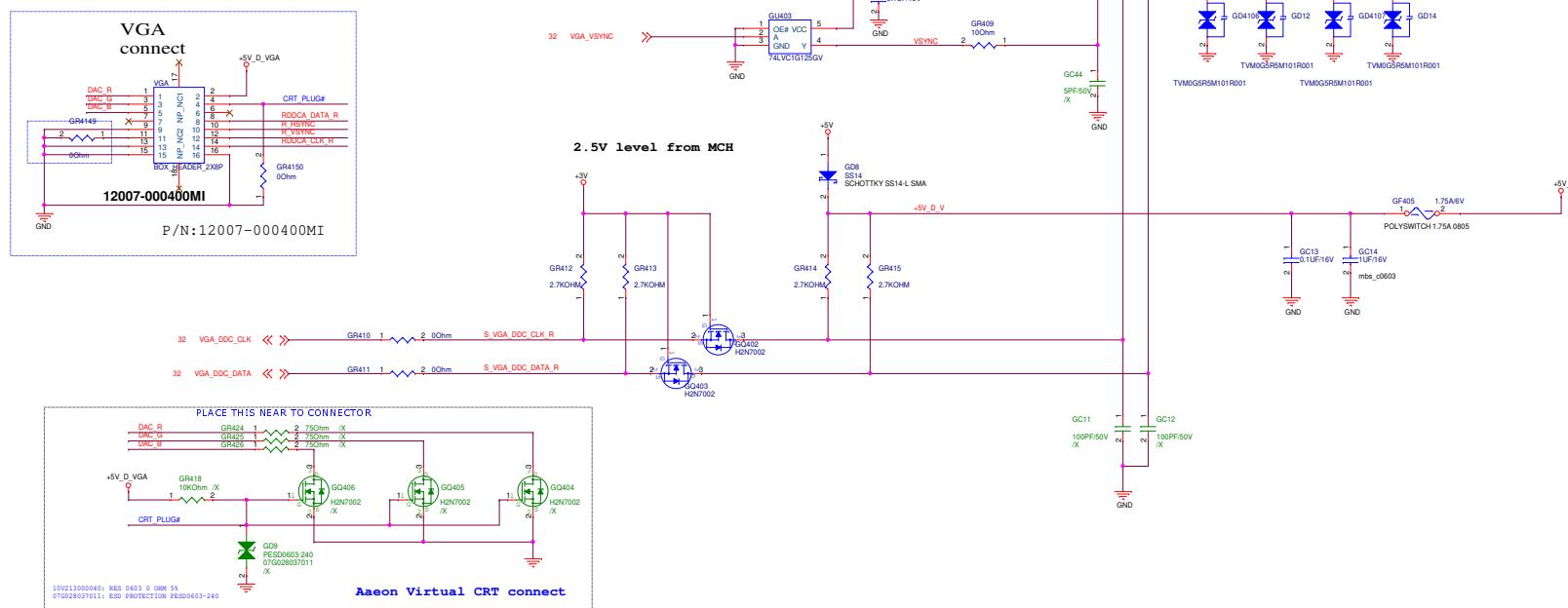
| | | |
|-------------------------------|----------------------------------|-------------|
| ASUSTOR COMPUTER INC. | Engineering | PCB |
| Size A4 | Project Name ATX-Q670E | Rev 1.00 |
| Date: Thursday, July 28, 2022 | Sheet 32 | of 86 |

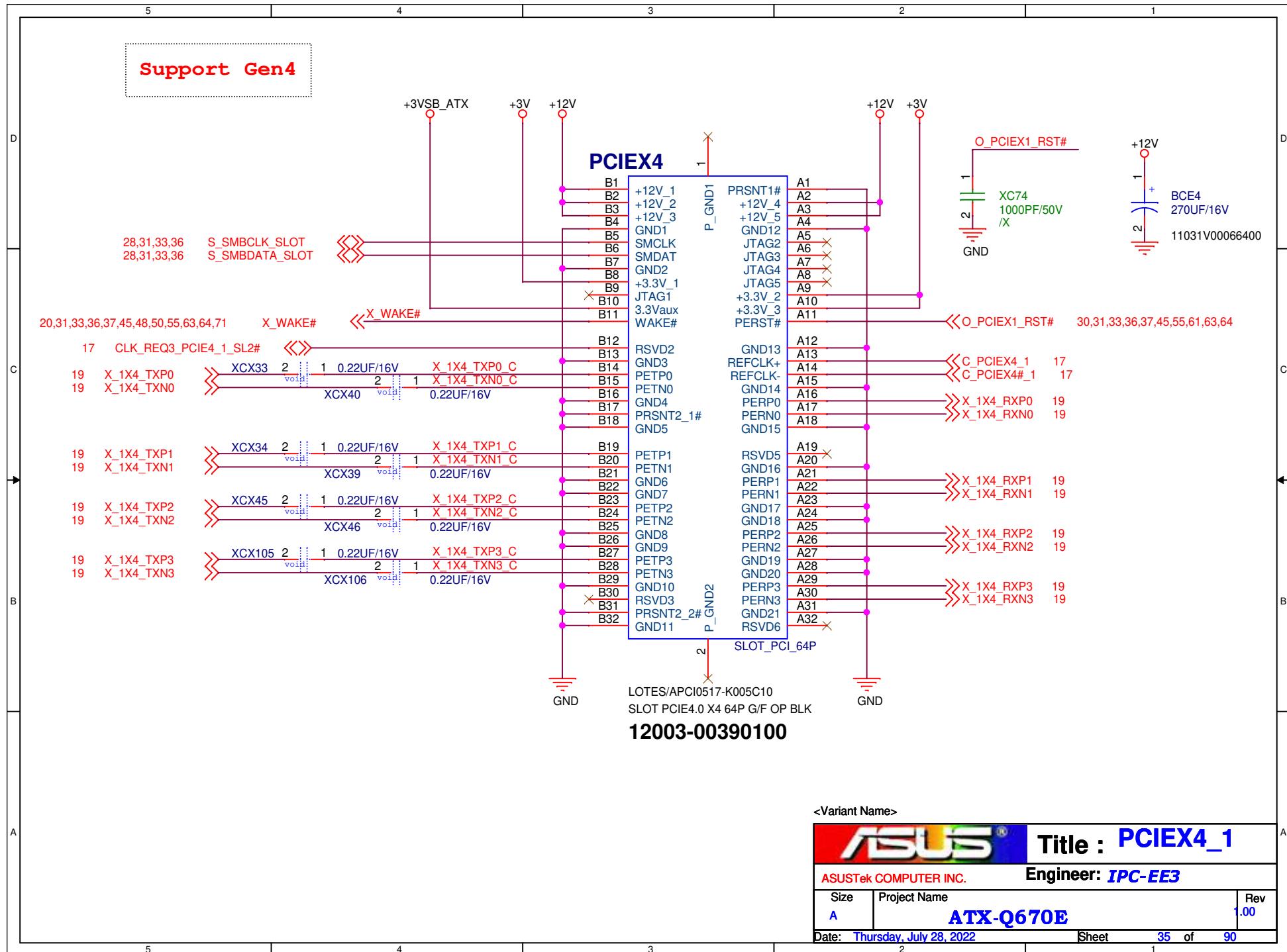


20211118 VGA (DDIA port), reference MAX-Q470A

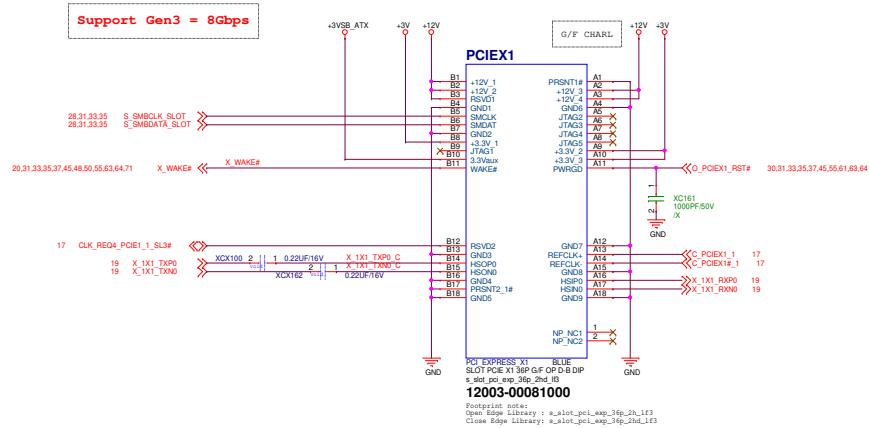


20211118 VGA header (DDIA port),
reference IMBA-Q87A



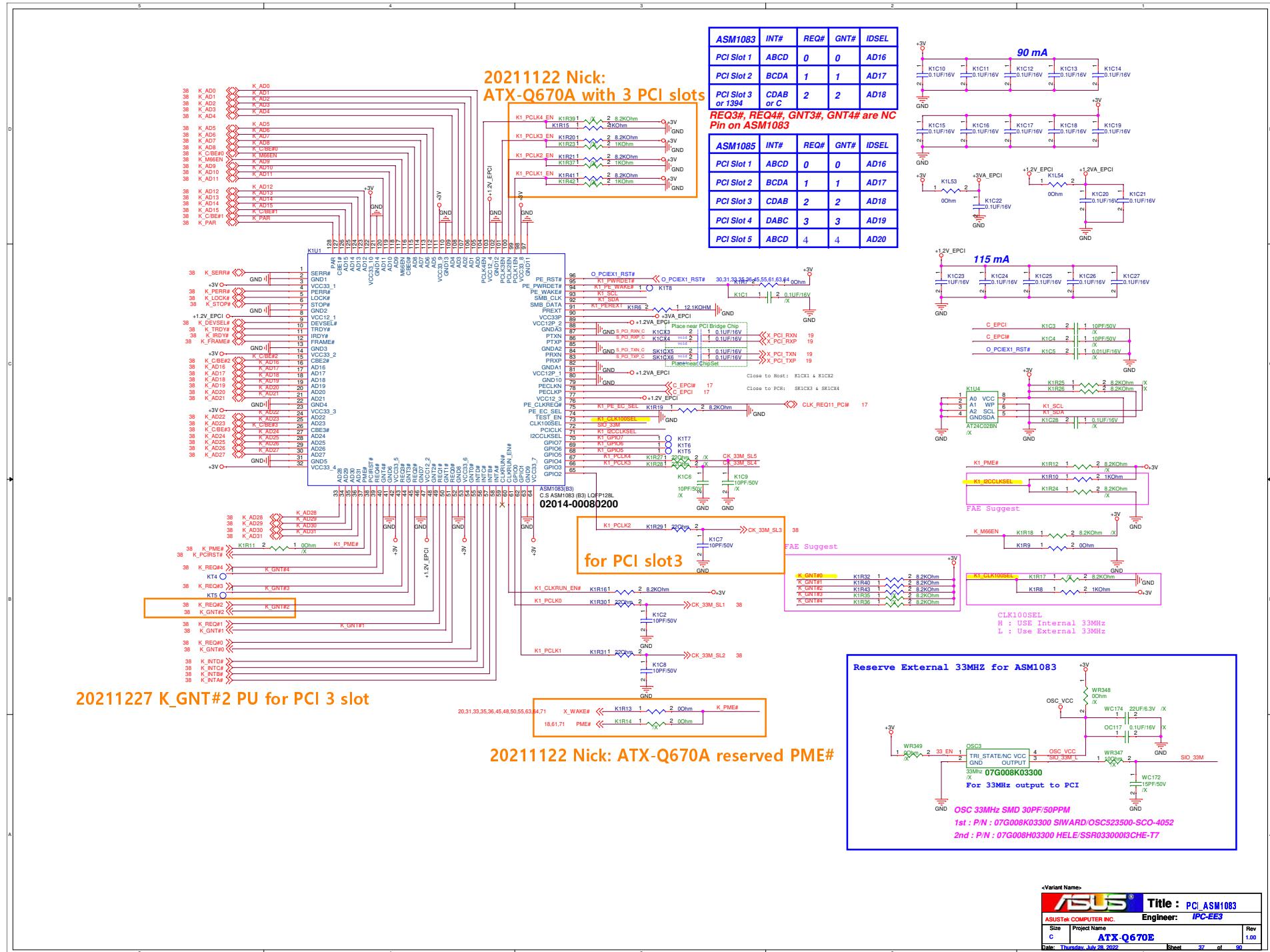


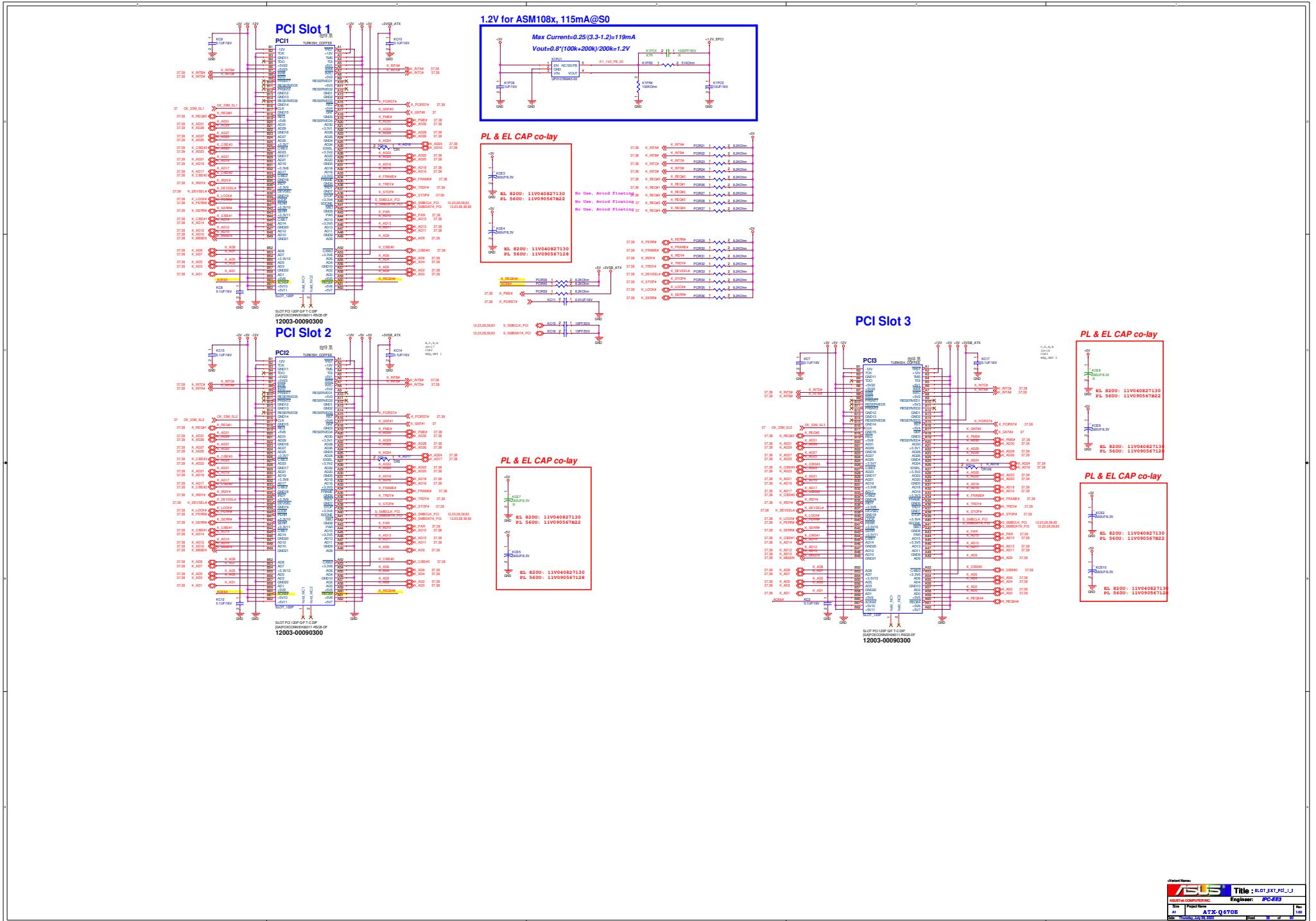
20211110 Nick modify, reference ATX-C246A, PCIEx1_1

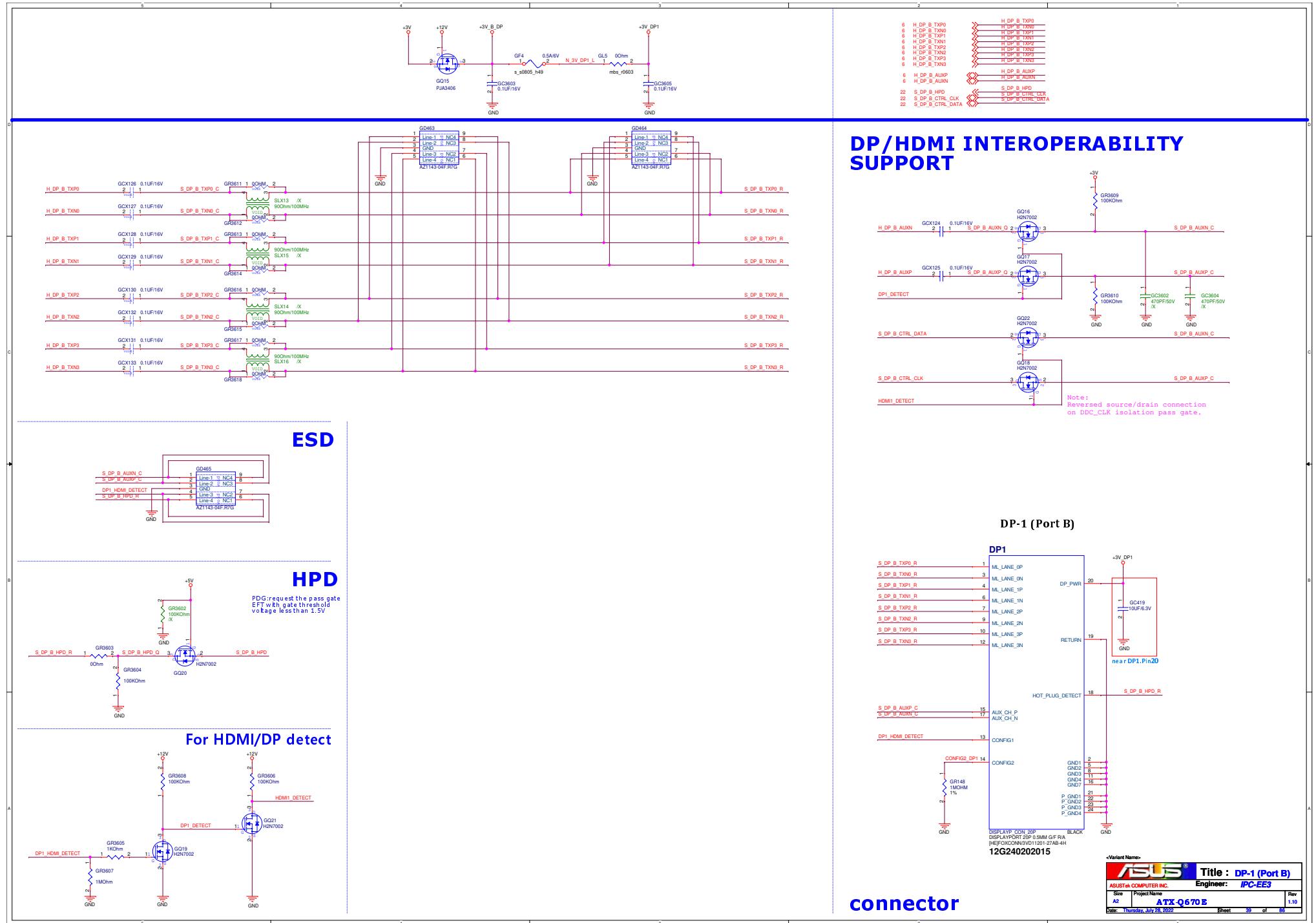


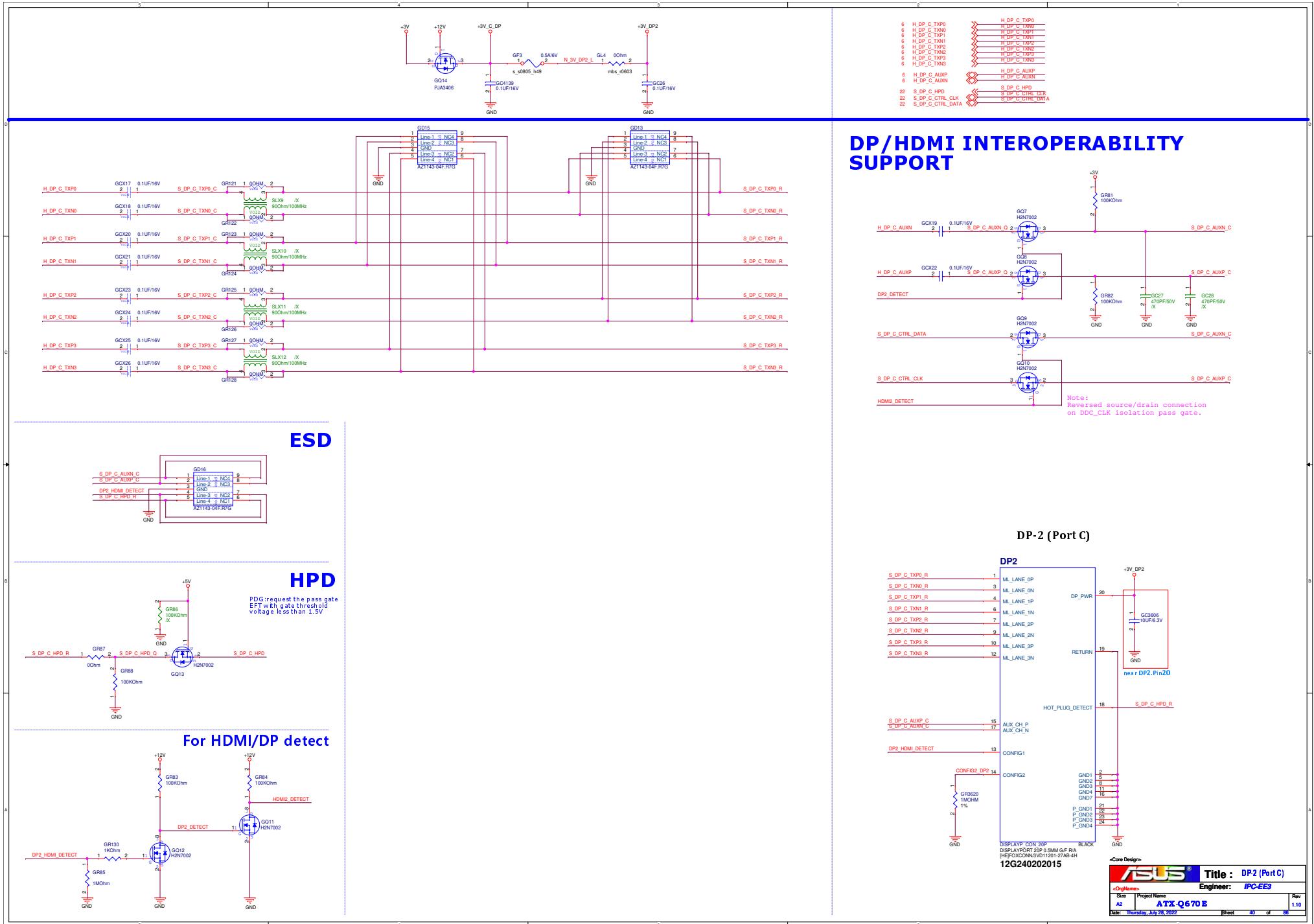
20211227 remove PCIEx1_2

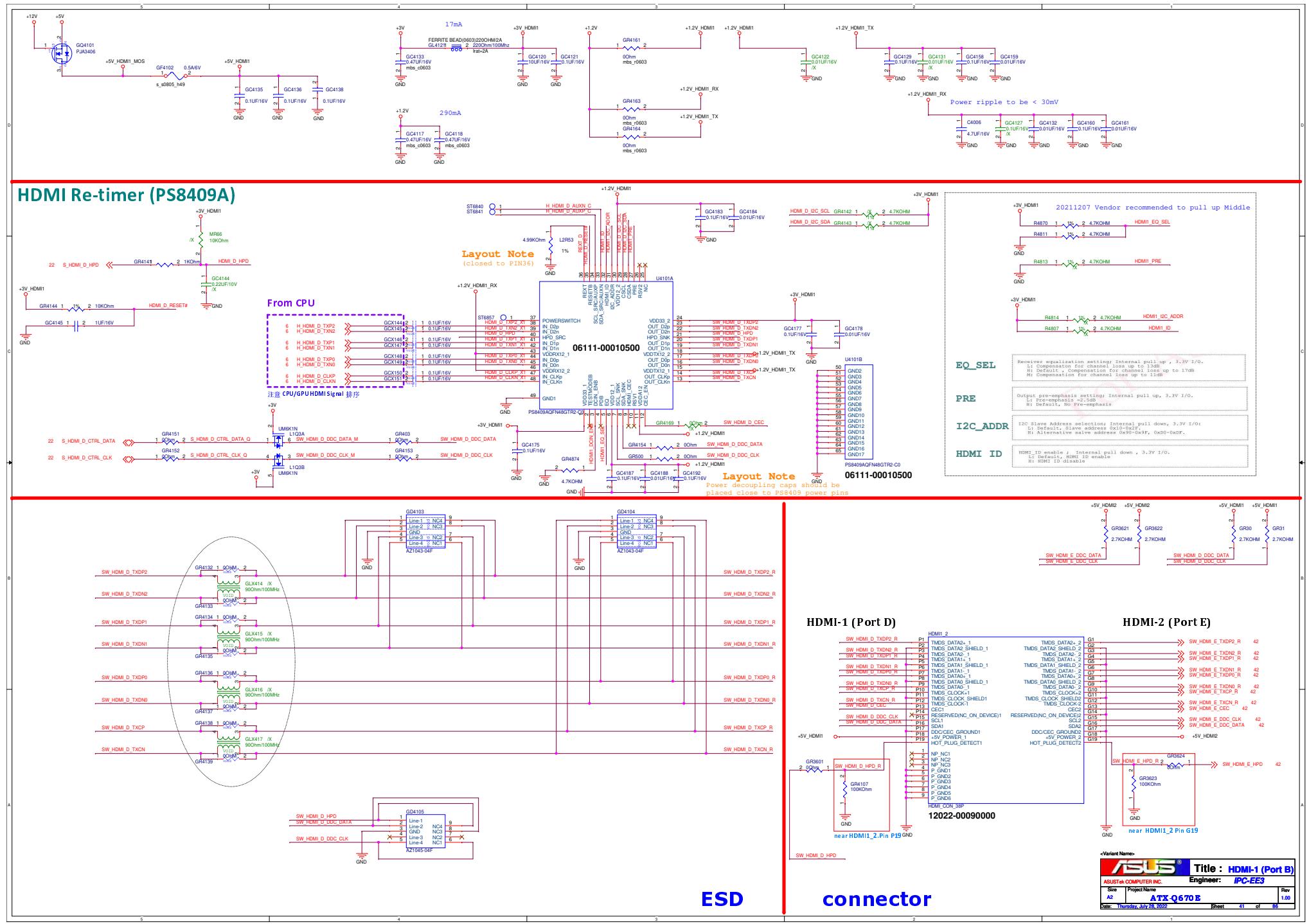
Support Gen3 = 8Gbps

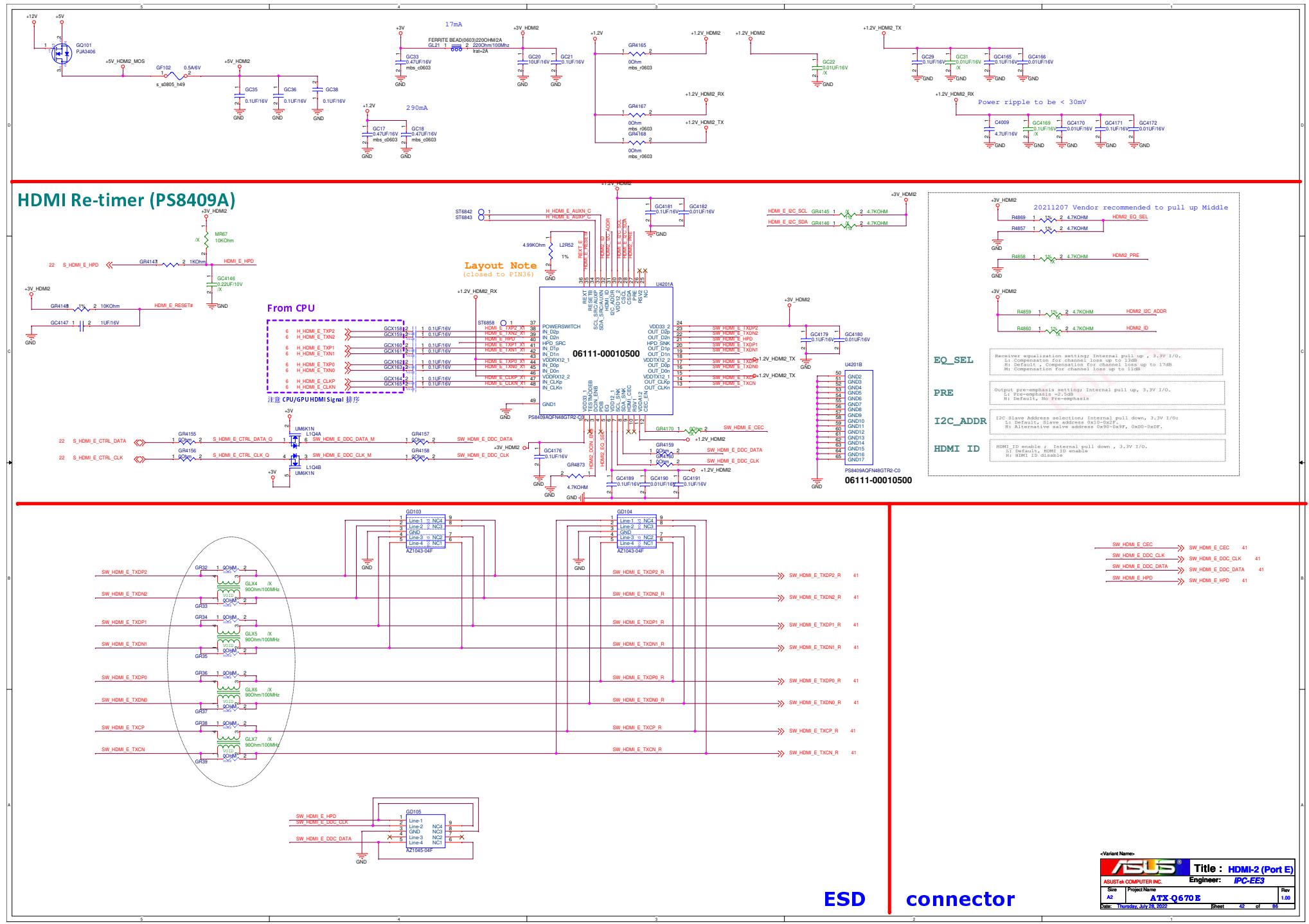


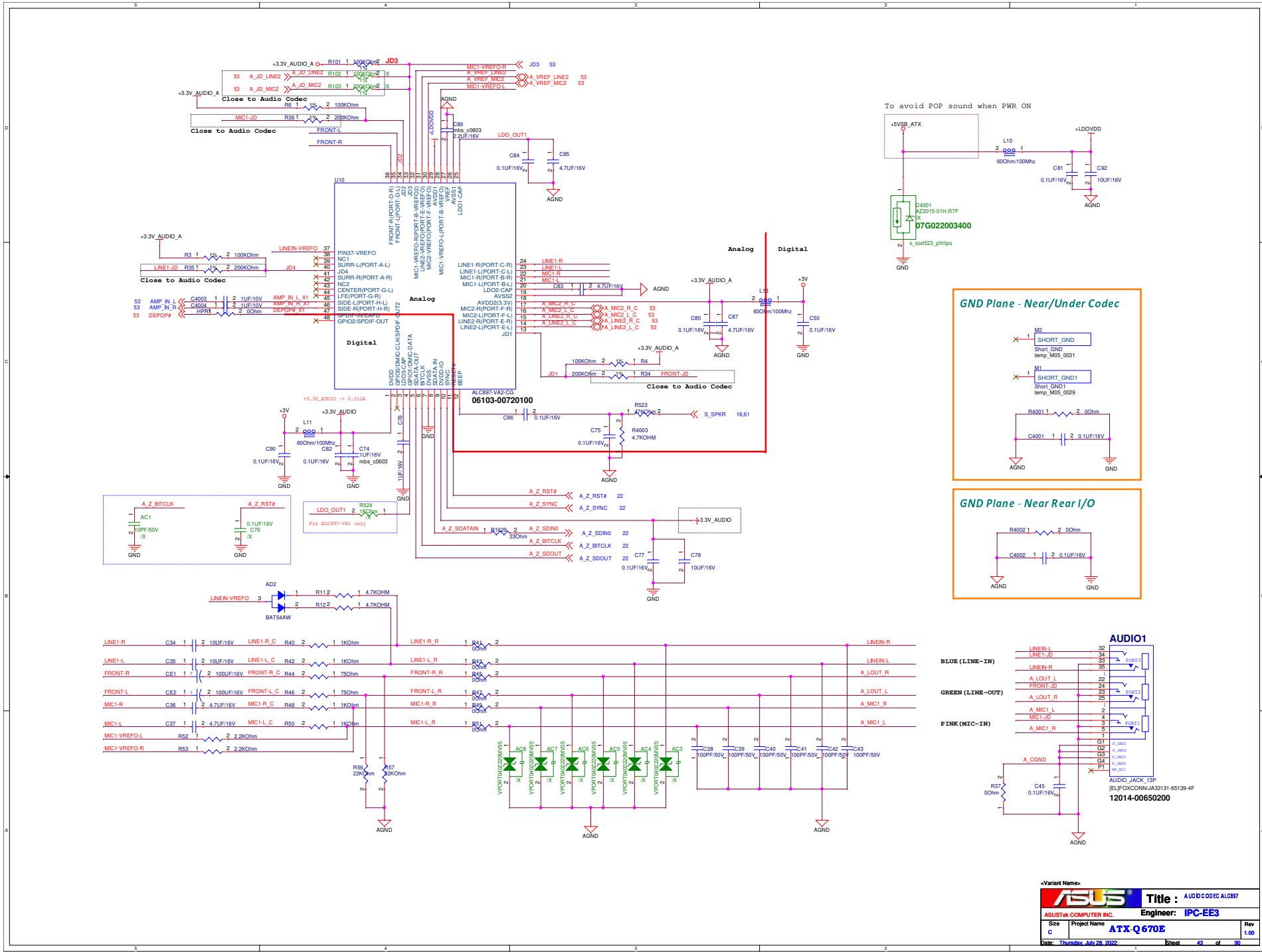


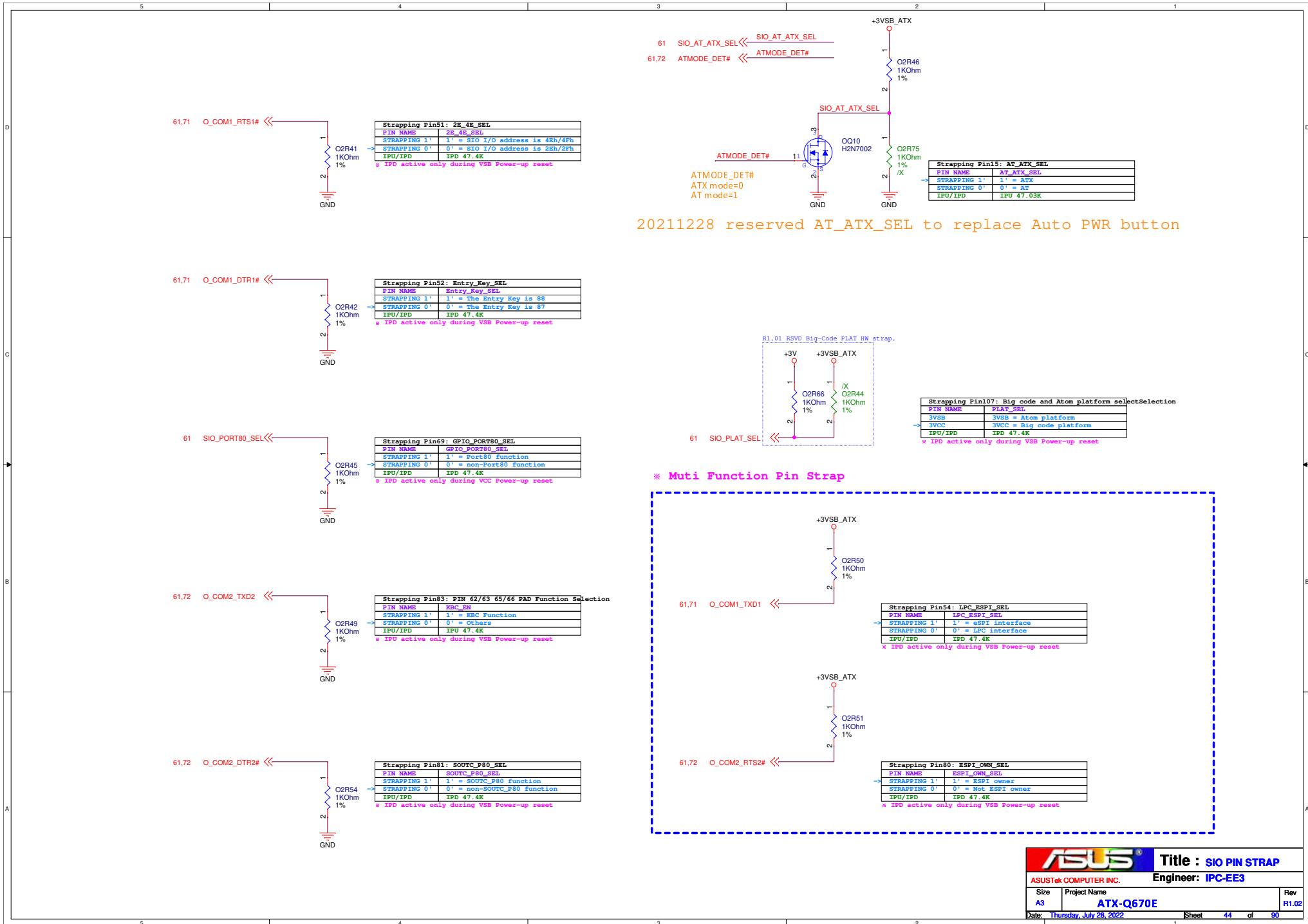








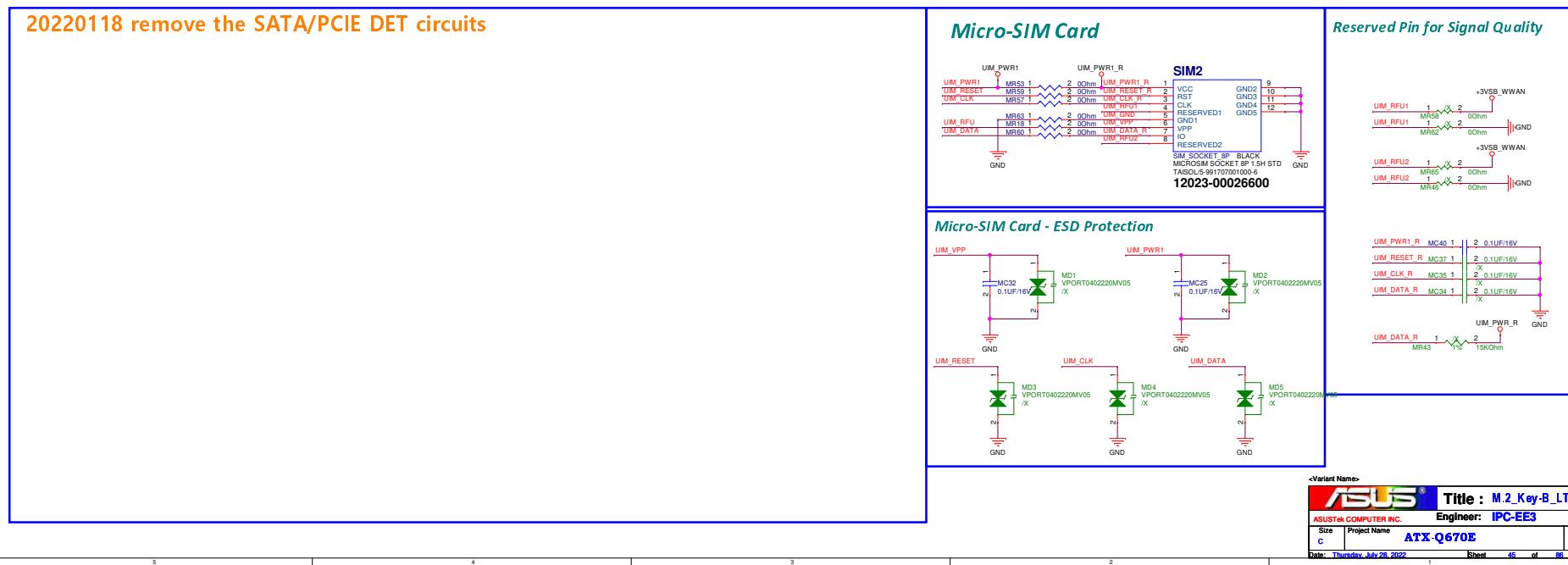
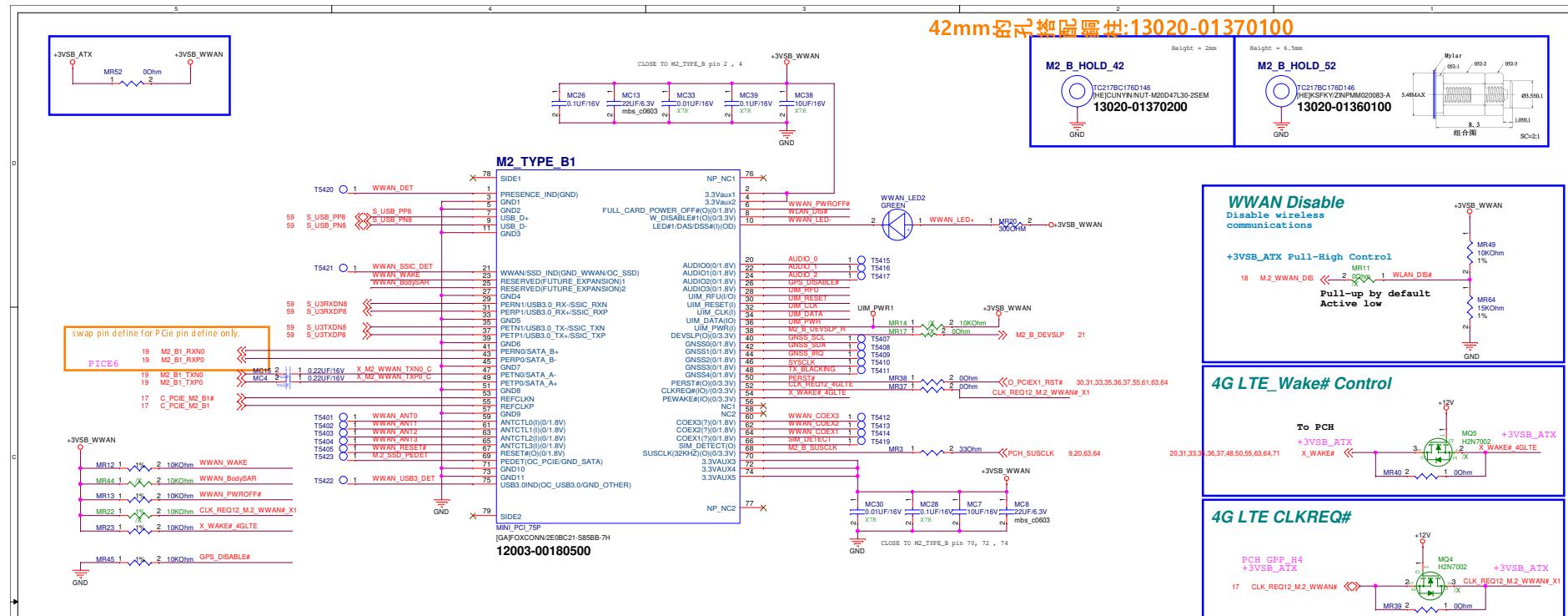


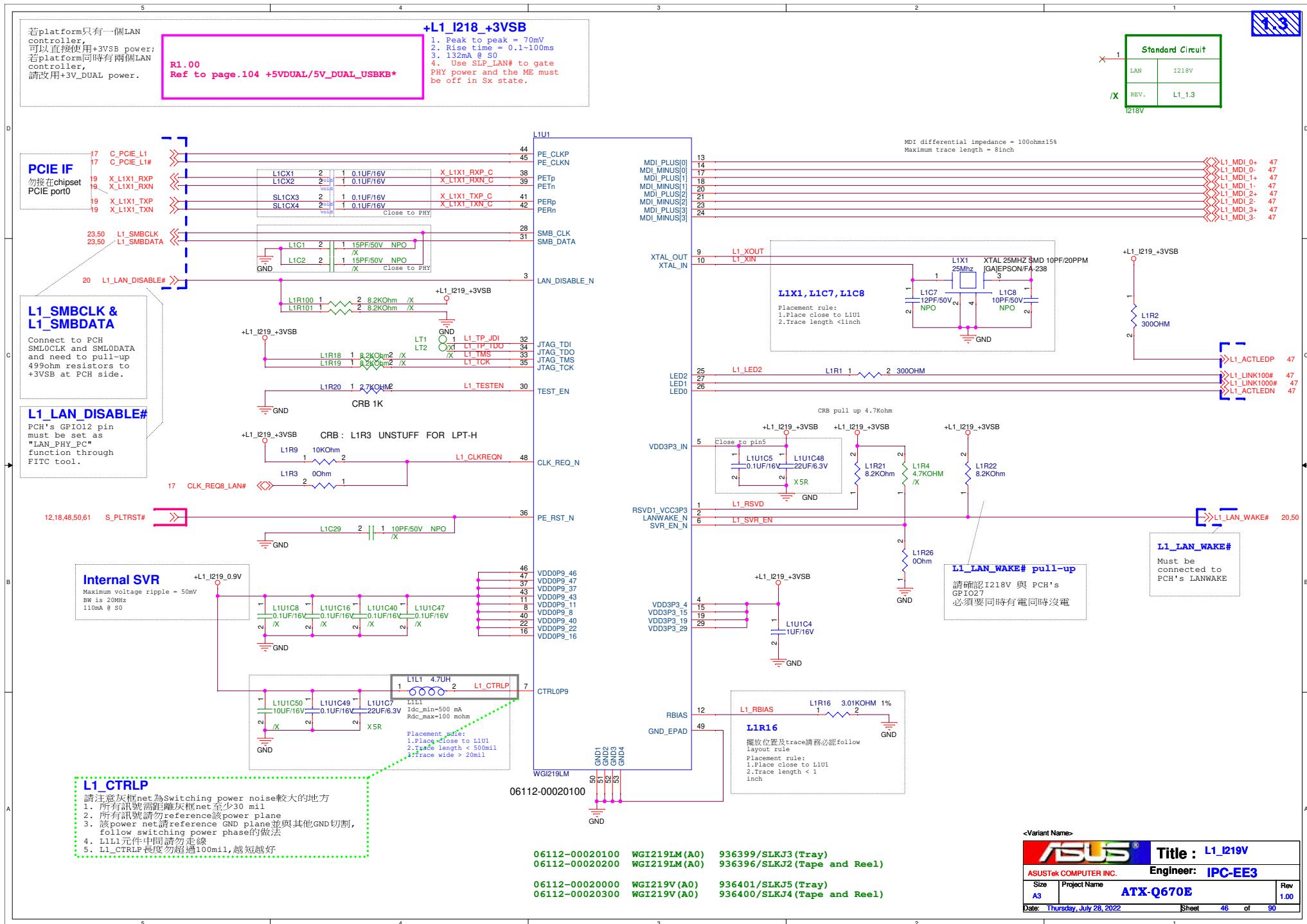


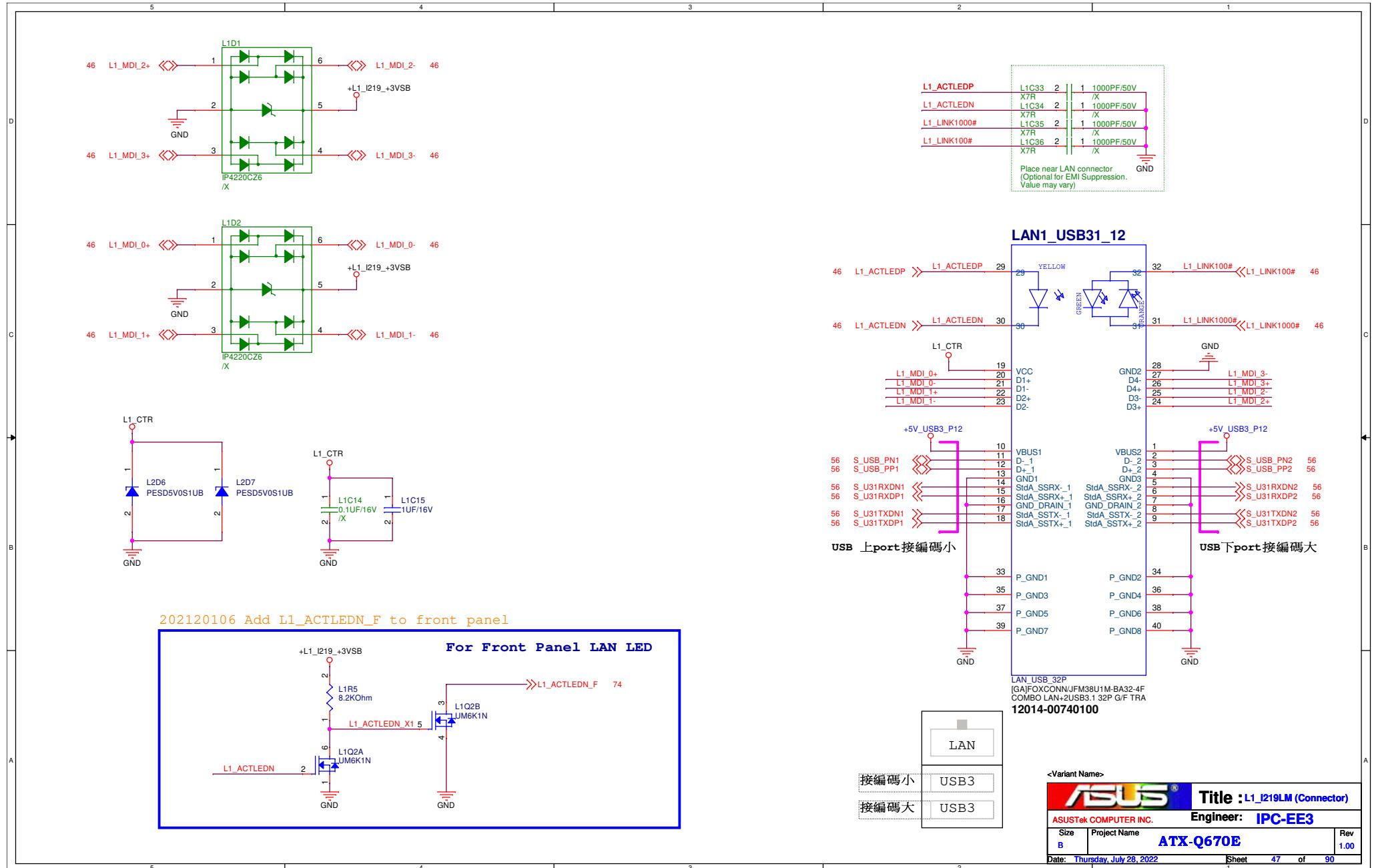
Title : SIO PIN STRAP

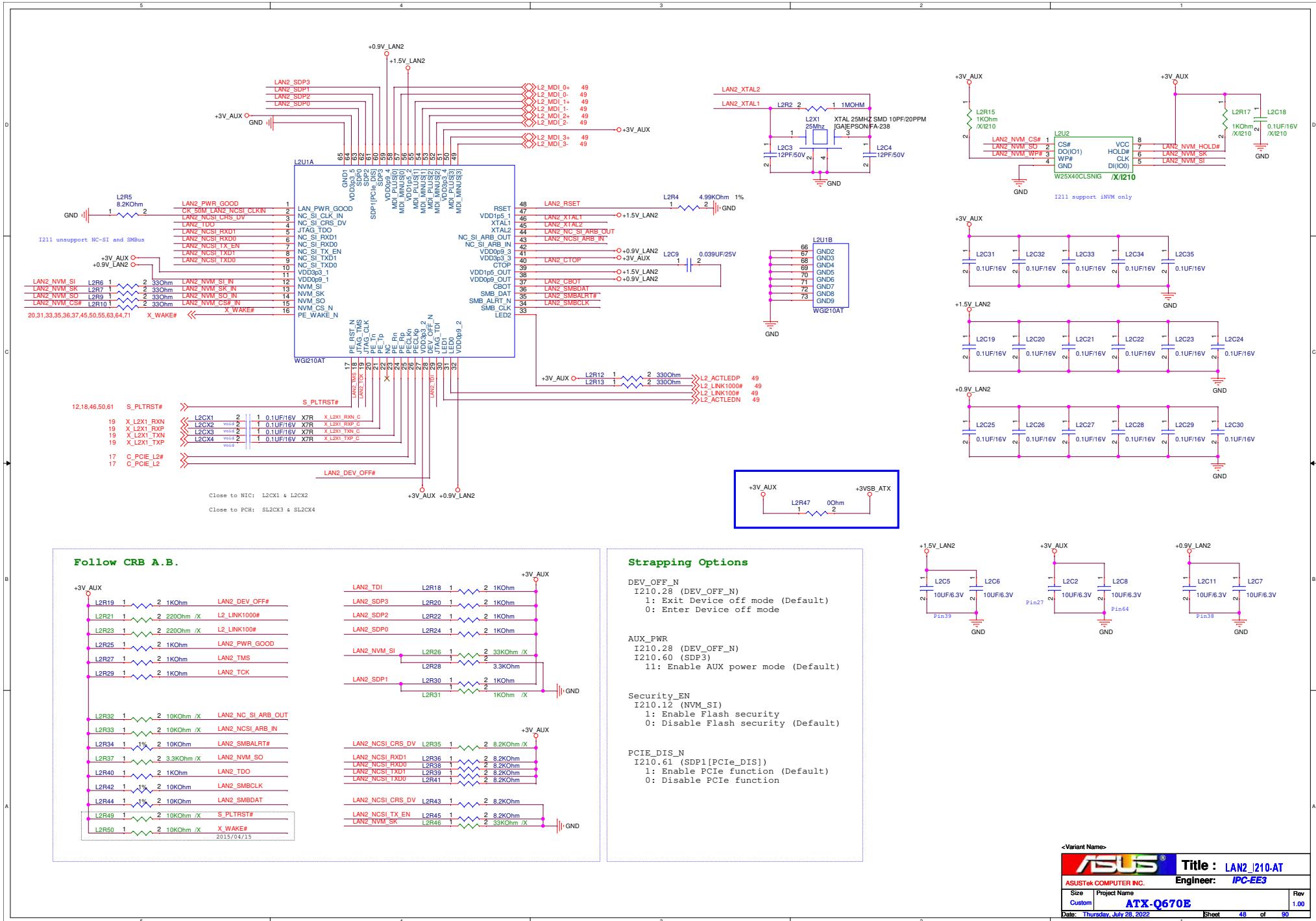
Engineer: IPC-EE3

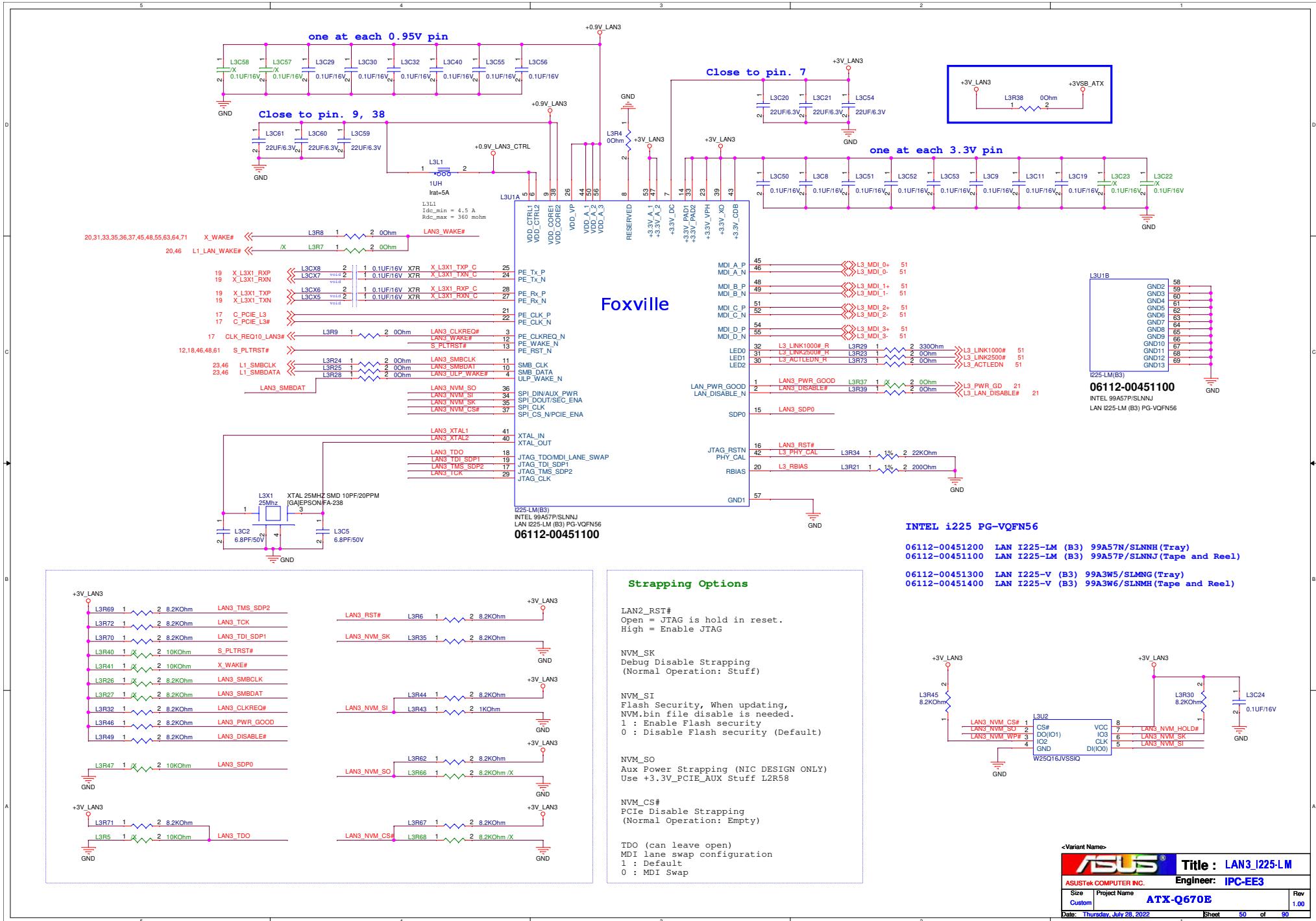
| Size | Project Name | Rev |
|-------------------------------|----------------|-------|
| A3 | ATX-Q670E | R1.02 |
| Date: Thursday, July 28, 2022 | Sheet 44 of 90 | 1 |

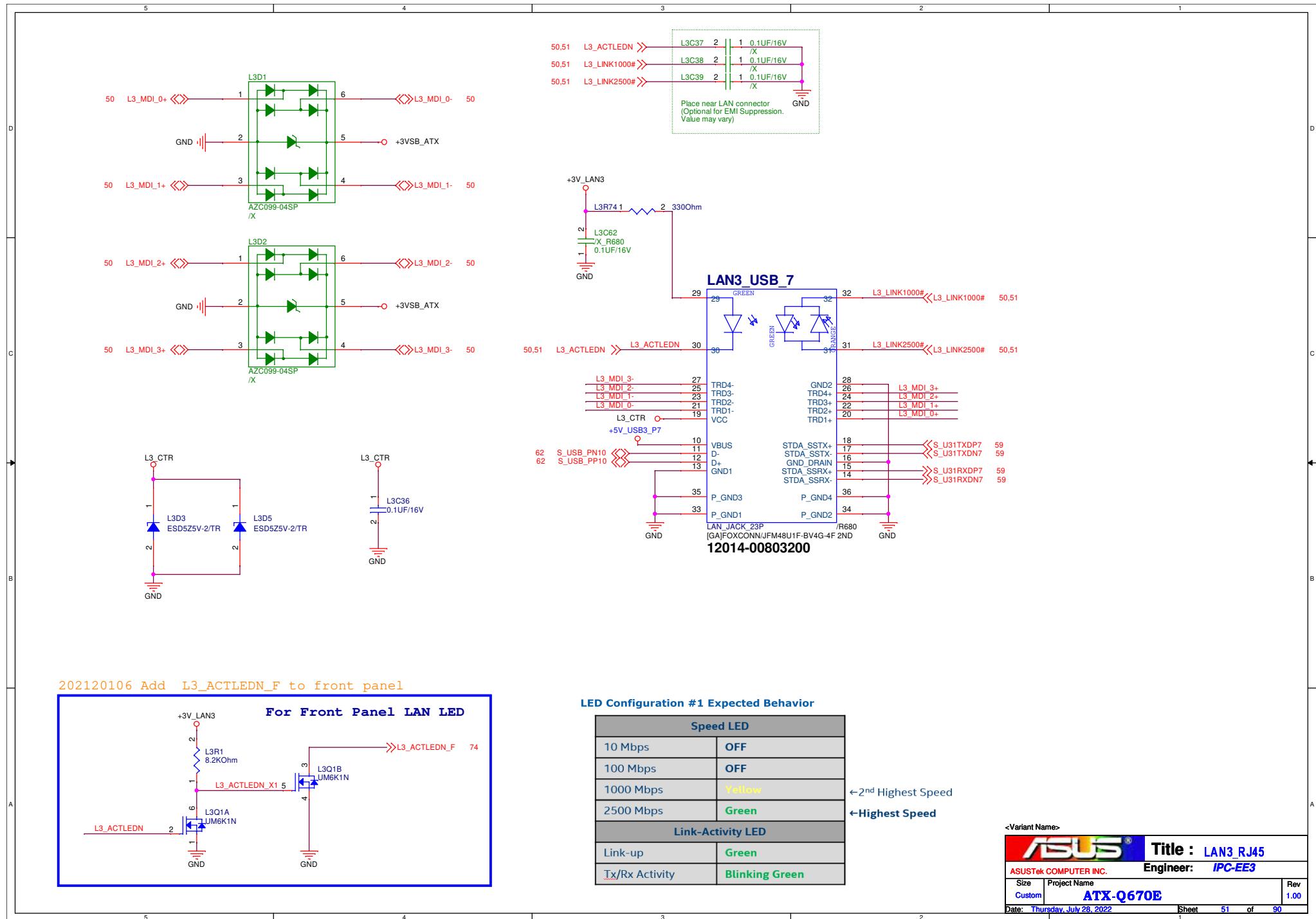


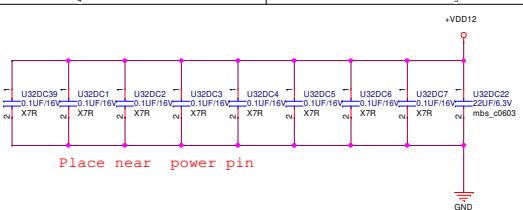






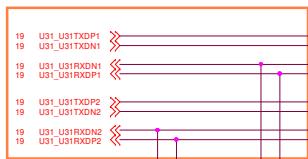




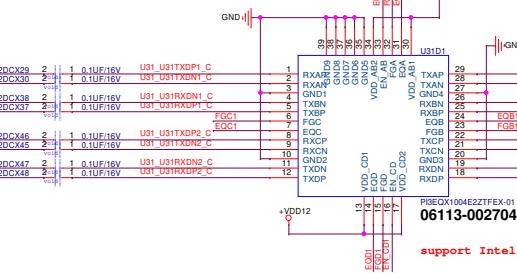


| Symbol | Parameter | Gen 1 (5.0 GT/s) | Gen 2 (10 GT/s) | Units | Comments |
|-----------------|-----------------------|------------------------|--------------------------------------|-------|---|
| Cxx ac-coupling | AC Coupling Capacitor | 297 (min) 363 (max) | 297 (min) 363 (max) 0.33uF | nF | Receivers may be AC coupled if desired. If used, the AC coupling is required to be either within the media or within the receiving component. |

Host (PCH)



for VCM PCH side test



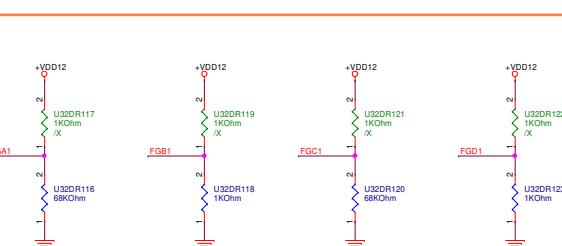
06113-002704

support Intel

add if Device side MUX can't
tolerance 3.3V DC level

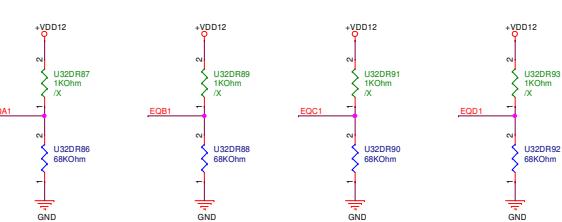
Close to connector

| <u>Strapping pin</u> | |
|------------------------|----------------|
| FGA1/B1/C1/D1 | Flat Gain (db) |
| pull up | +2.7 |
| pull down | -0.5 |
| F(Leave open) | 1.0 (Default) |
| R (Tie Rest to Gnd) | -1.6 |

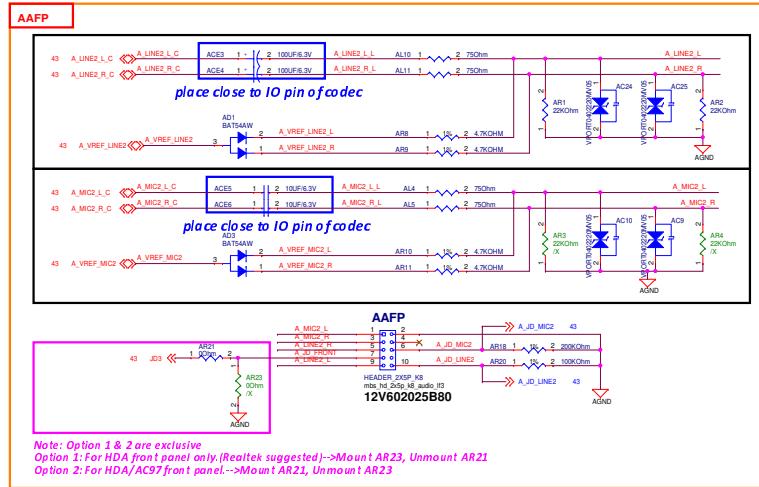
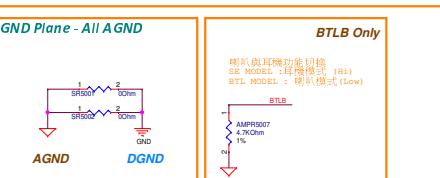
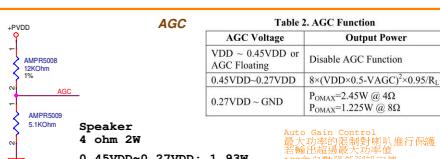
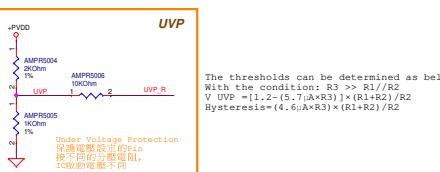
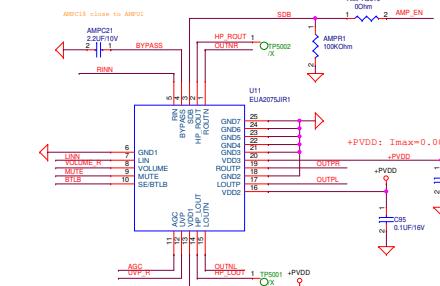
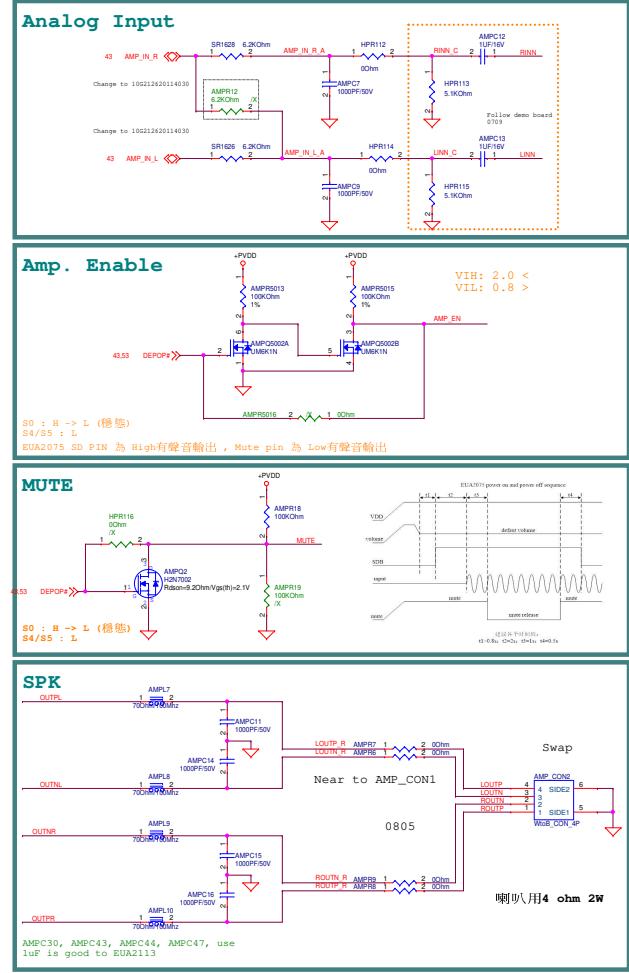


| Channel Enable | |
|---------------------------|------------------|
| EN | Setting |
| Pull up (Internal P-U) | Enable (Default) |
| pull down | Disable |

| Strapping pin | |
|------------------------|------------------------|
| EQA1/B1/C1/D1 | Equalizer 2.5G/5G (db) |
| pull up | 8.4/14.6 |
| pull down | 6.7/12.4 |
| F (Leave open) | 5.3/10.6 (Default) |
| R (Tie Rext to Gnd) | 3.5/8 |

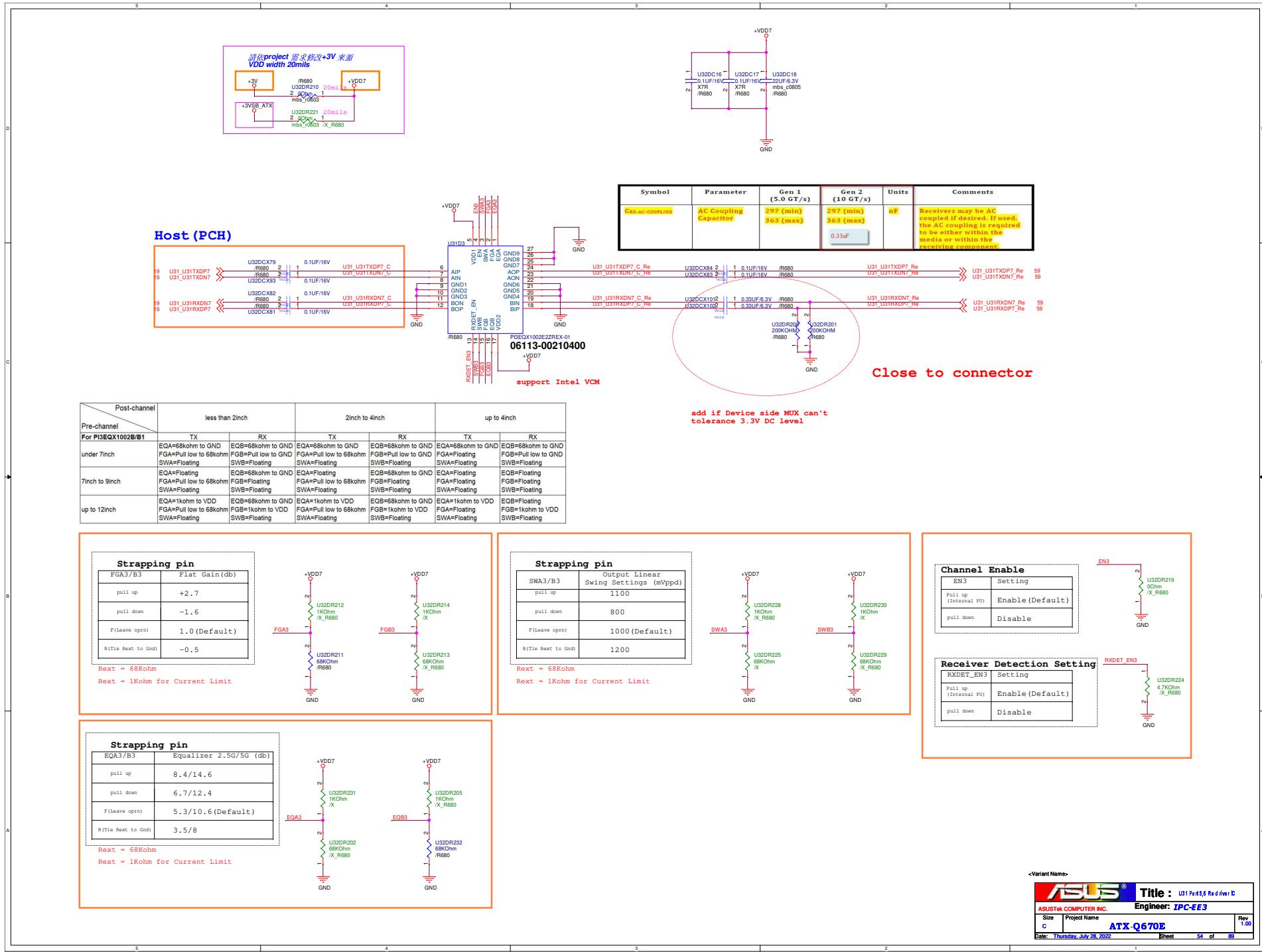


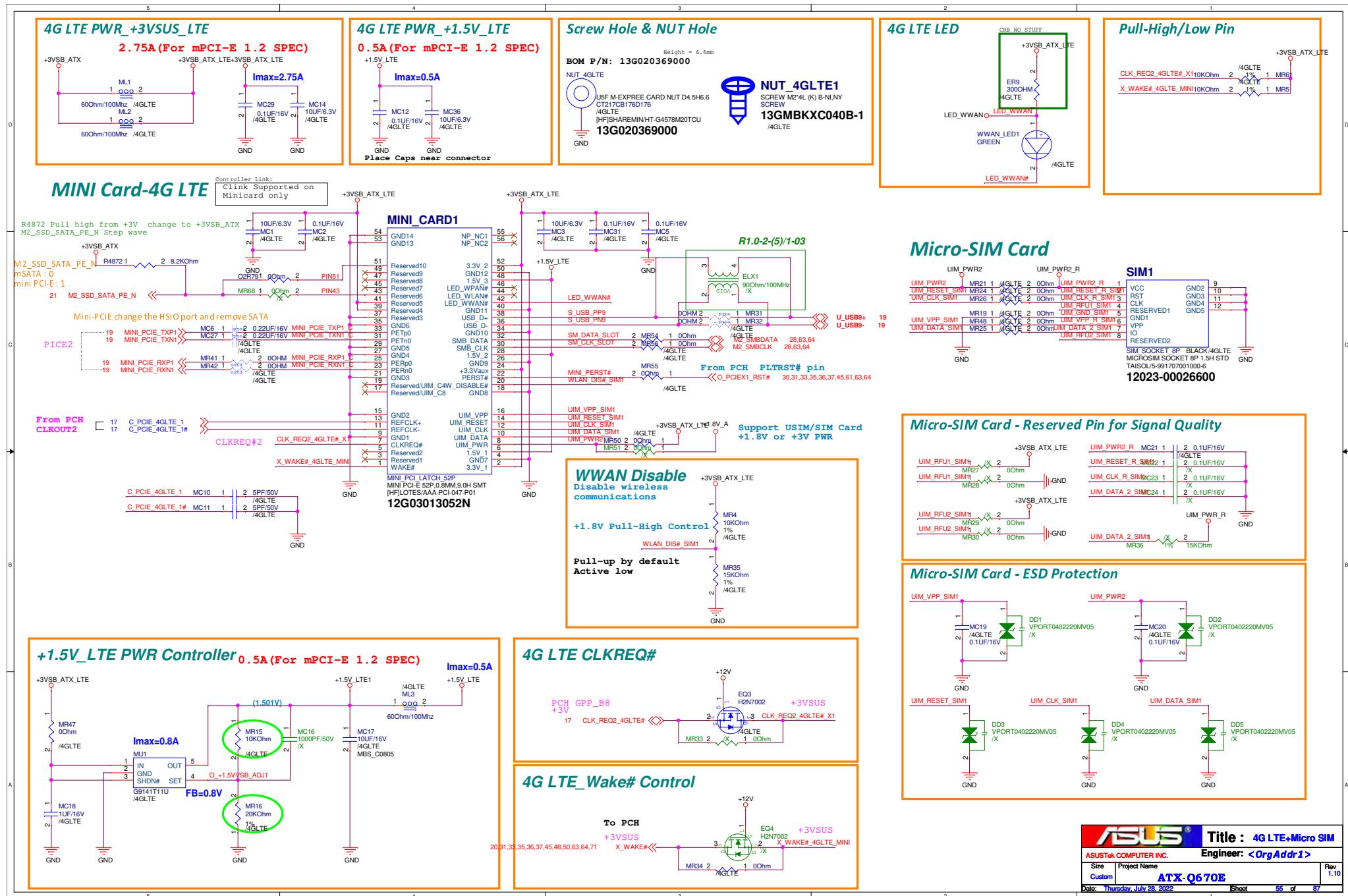
AMP - EUA2075JIR1 (Only Speaker)

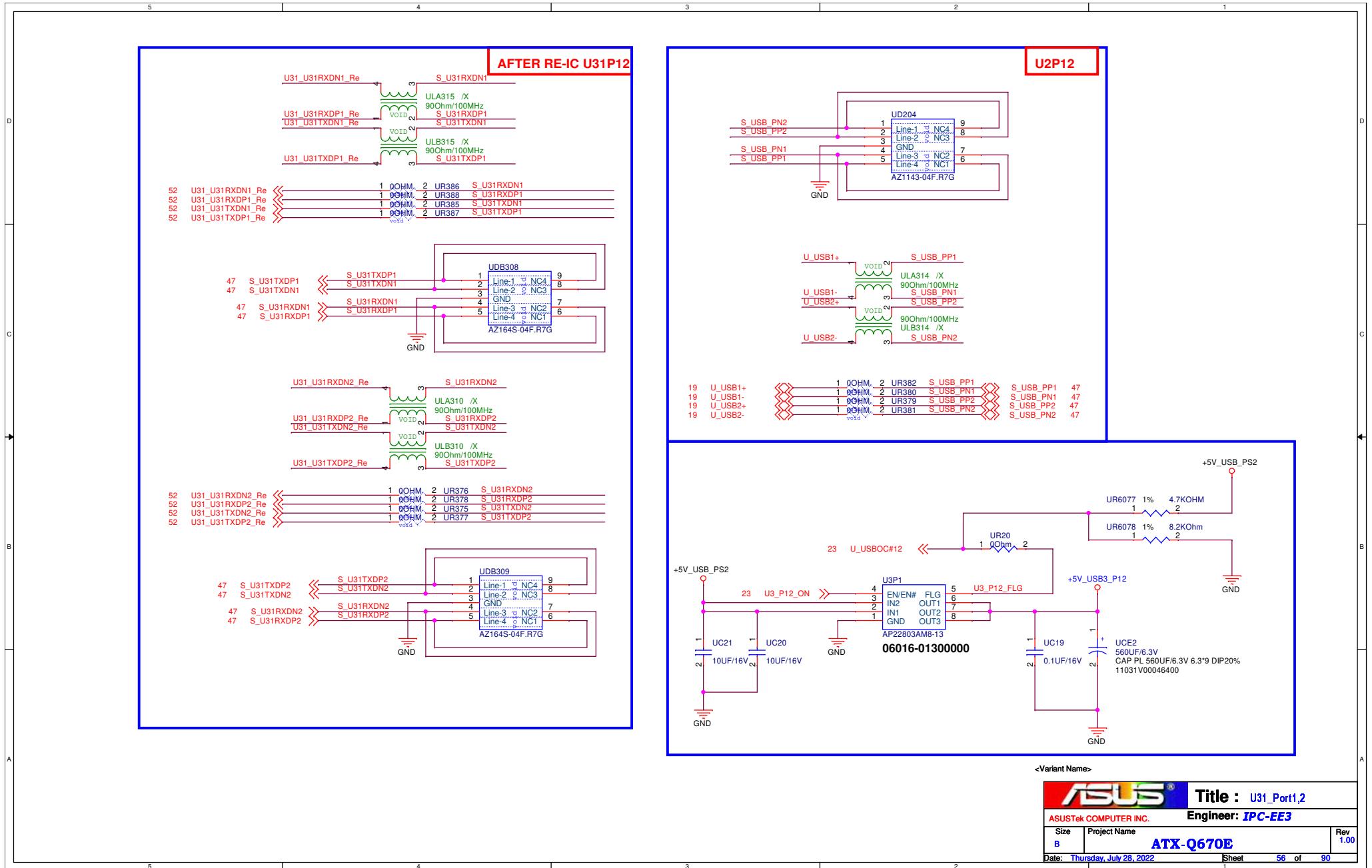


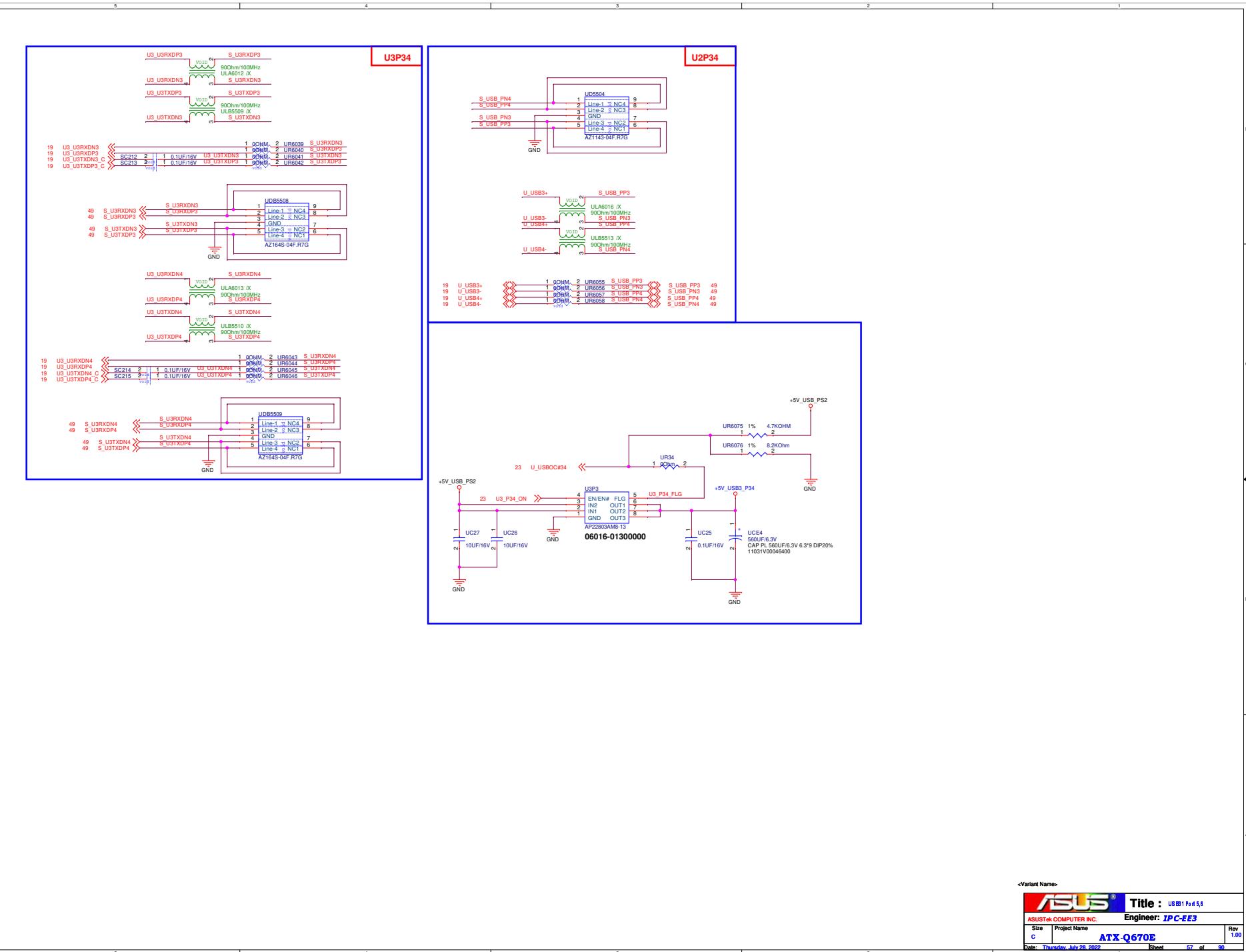
Note: Option 1 & 2 are exclusive
Option 1: For HDA front panel only.(Realtek suggested)-->Mount AR23, Unmount AR21
Option 2: For HDA/AC97 front panel.-->Mount AR21, Unmount AR23

| Table 1. DC Volume Control | | | |
|----------------------------|---|---|------------------|
| Step | Decreasing Volume (Volume Pin Voltage As A Percentage of 3.3VDC (%)) | Increasing Volume (Volume Pin Voltage As A Percentage of 3.3VDC (%)) | BTU Gain (dB) |
| 1 | 3.4 - 3.0 | 3.4 - 3.0 | 70.0 |
| 2 | 3.4 - 3.8 | 3.8 - 2.4 | 19.6 |
| 3 | 4.8 - 6.2 | 5.2 - 3.8 | 19.2 |
| 4 | 5.2 - 7.2 | 6.5 - 5.5 | 18.8 |
| 5 | 7.6 - 9.0 | 8.0 - 6.6 | 18.4 |
| 6 | 9.0 - 10.4 | 9.4 - 8.0 | 18.0 |
| 7 | 11.4 - 12.8 | 10.8 - 9.4 | 17.6 |
| 8 | 11.8 - 13.2 | 12.2 - 10.8 | 17.2 |
| 9 | 13.2 - 14.6 | 13.6 - 12.2 | 16.8 |
| 10 | 14.6 - 16.0 | 15.0 - 13.6 | 16.4 |
| 11 | 16.0 - 17.4 | 16.4 - 15.0 | 16.0 |
| 12 | 17.4 - 18.8 | 17.8 - 16.4 | 15.6 |
| 13 | 18.8 - 20.2 | 19.2 - 17.8 | 15.2 |
| 14 | 20.2 - 21.6 | 20.6 - 19.2 | 14.8 |
| 15 | 21.6 - 23.0 | 22.0 - 20.6 | 14.4 |
| 16 | 23.0 - 24.4 | 23.4 - 20.0 | 14.0 |
| 17 | 24.4 - 25.8 | 24.8 - 23.4 | 13.6 |
| 18 | 25.8 - 27.2 | 26.2 - 24.8 | 13.2 |
| 19 | 27.2 - 28.6 | 27.6 - 26.2 | 12.8 |
| 20 | 28.6 - 30.0 | 29.0 - 27.6 | 12.4 |
| 21 | 30.0 - 31.4 | 30.4 - 29.0 | 12.0 |



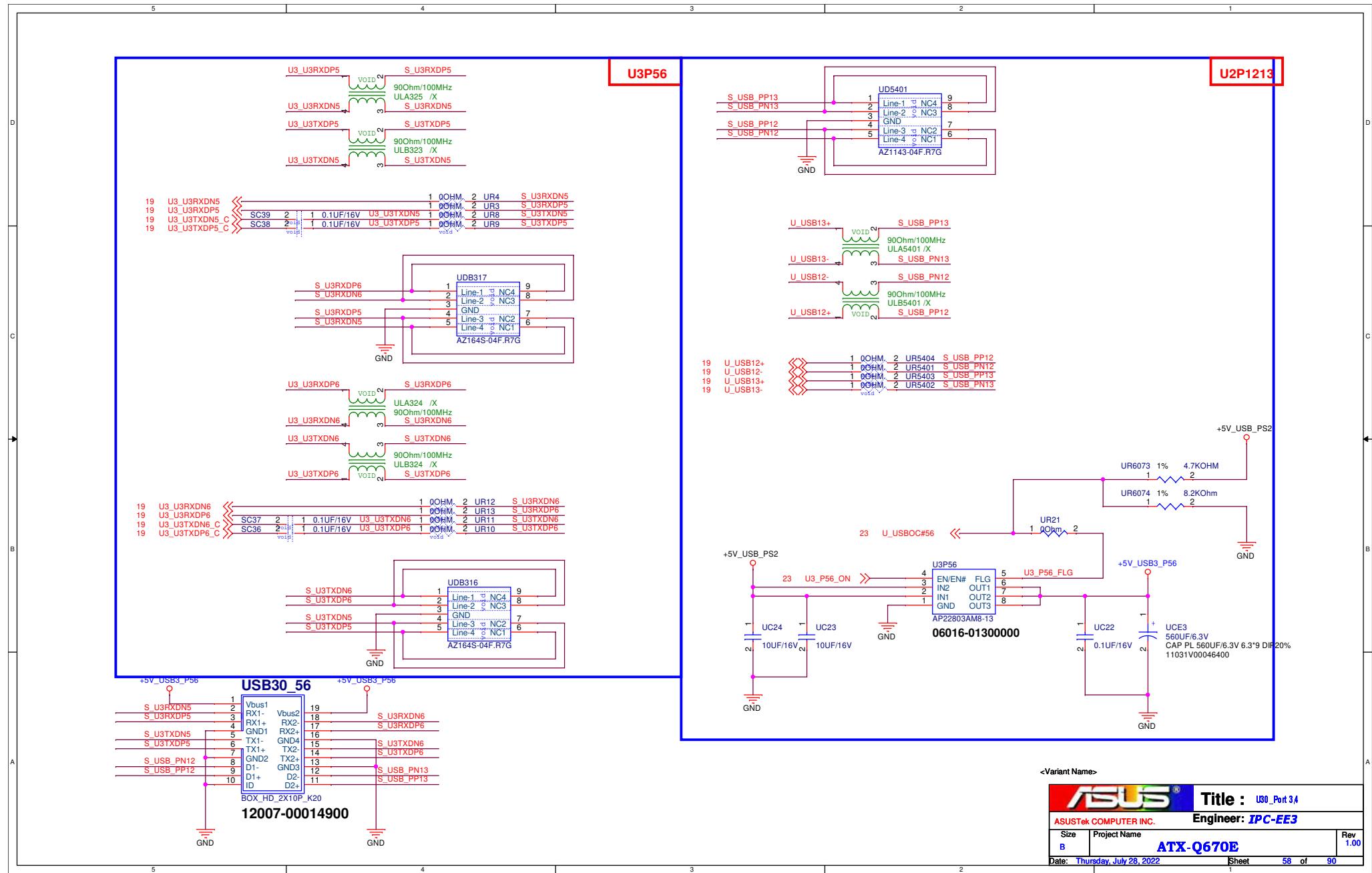


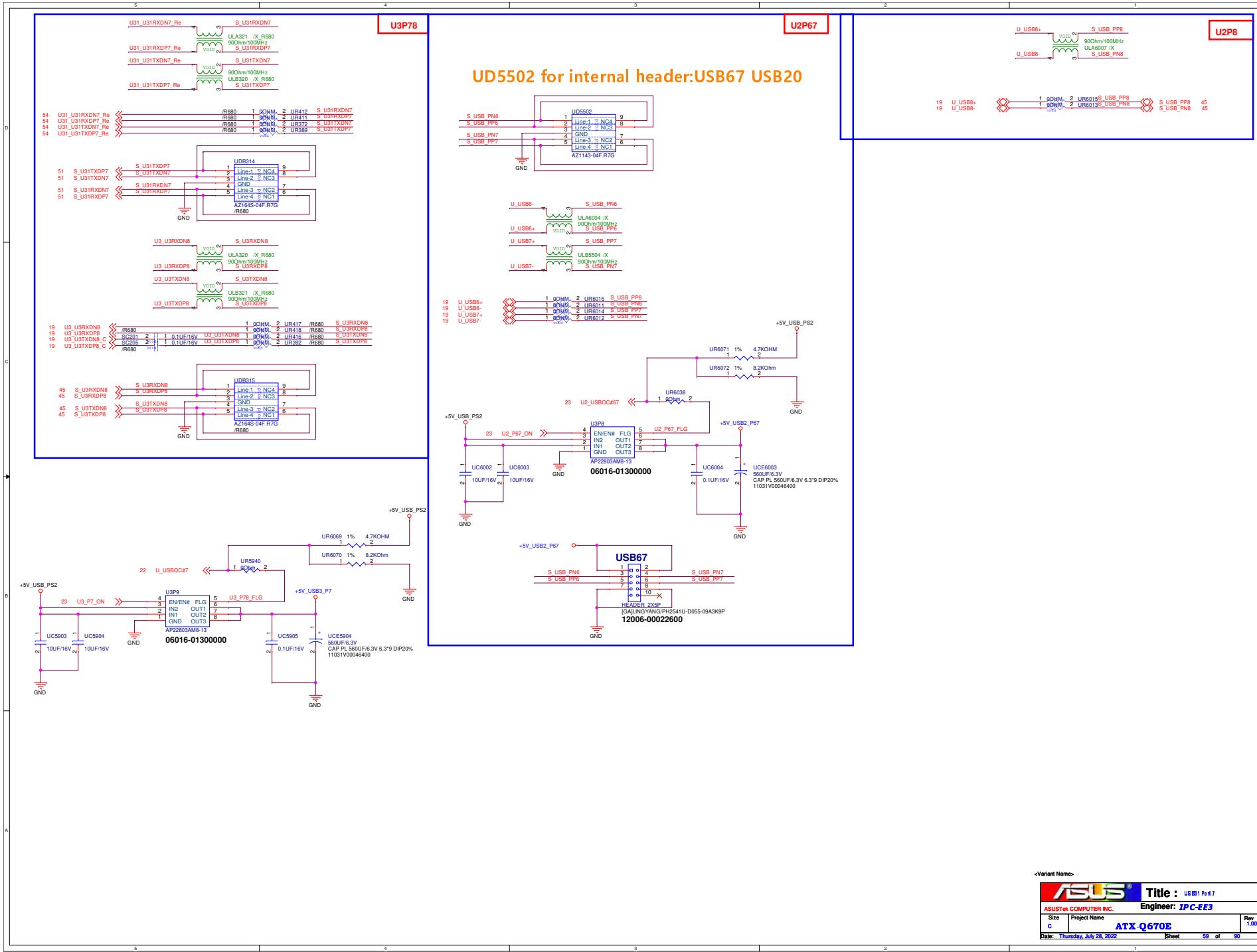


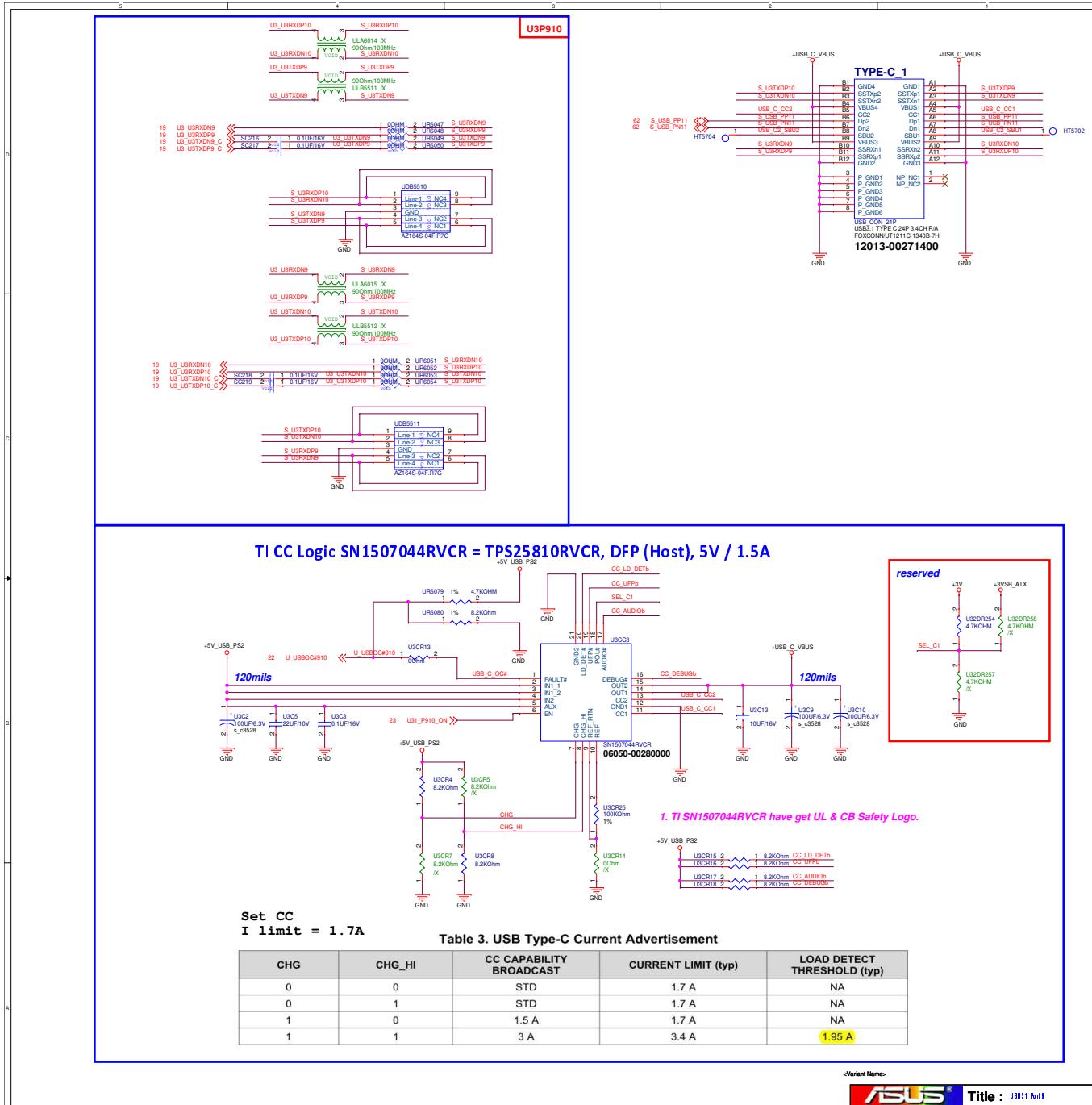


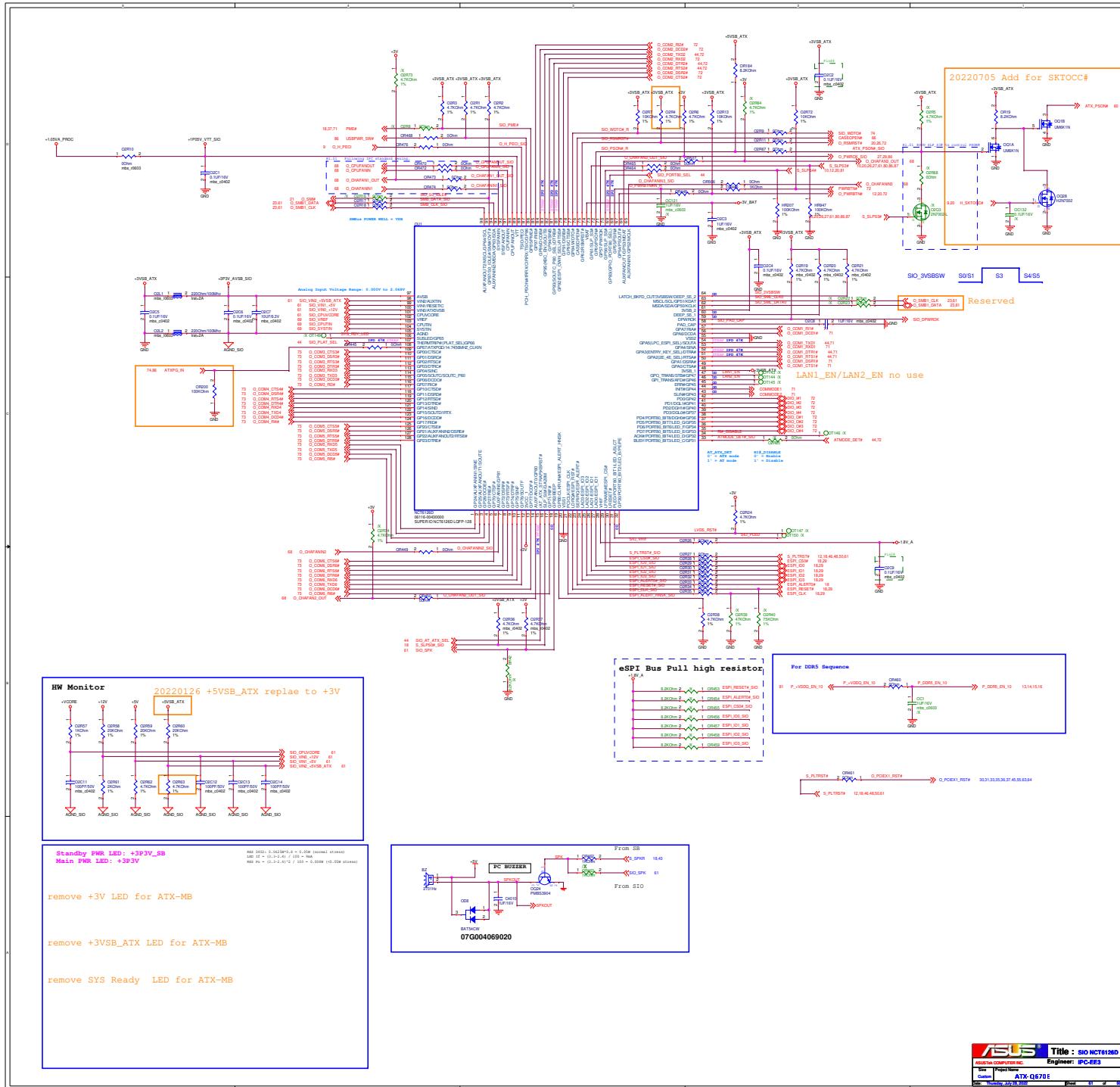
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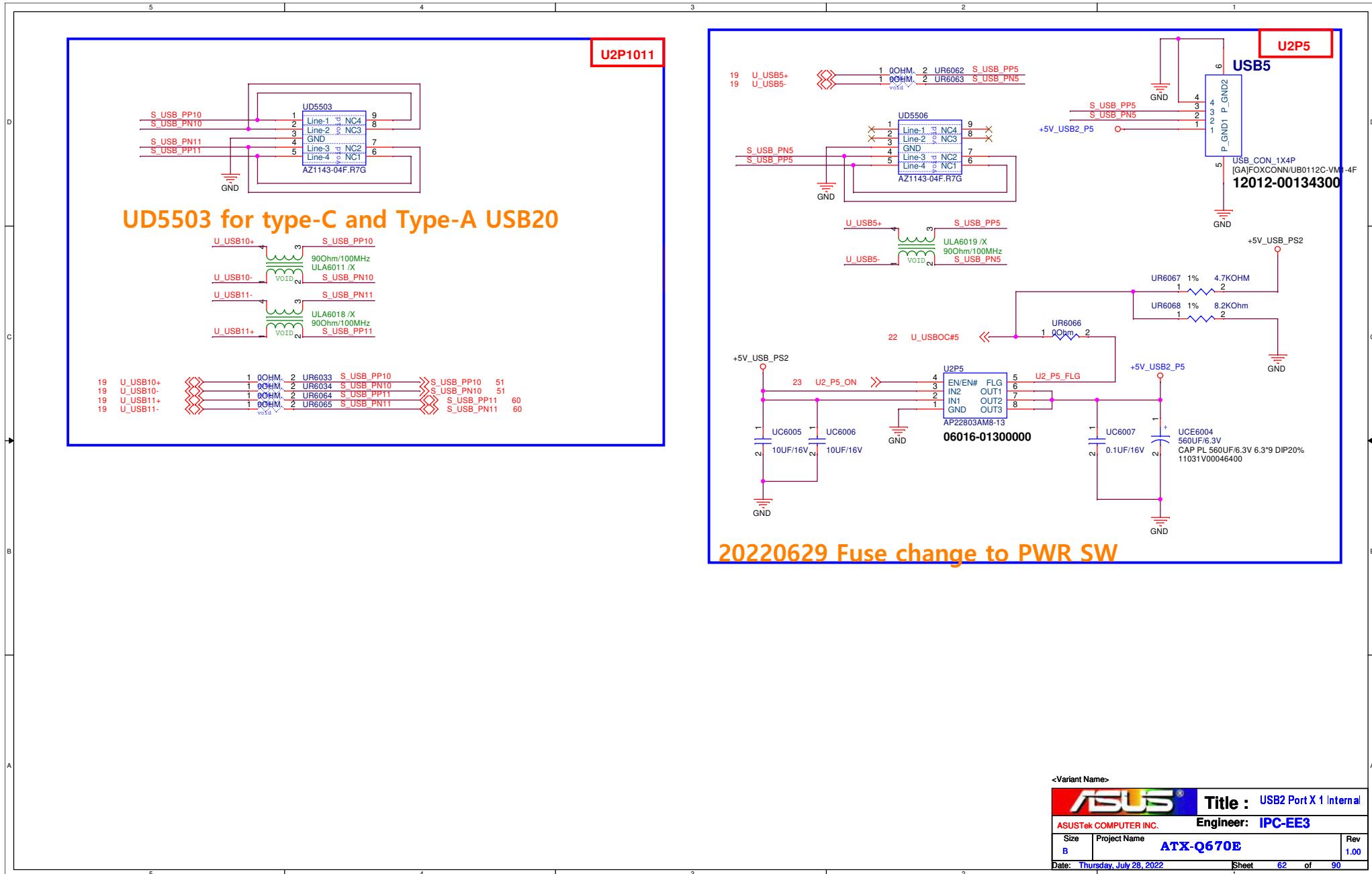
| | |
|-------------------------------|------------------------------|
| ASUS® | Title : USB1 Part 5.0 |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 |
| Size C | Project Name ATX-Q670E |
| Date: Thursday, July 21, 2022 | Sheet 57 of 90 Rev 1.00 |

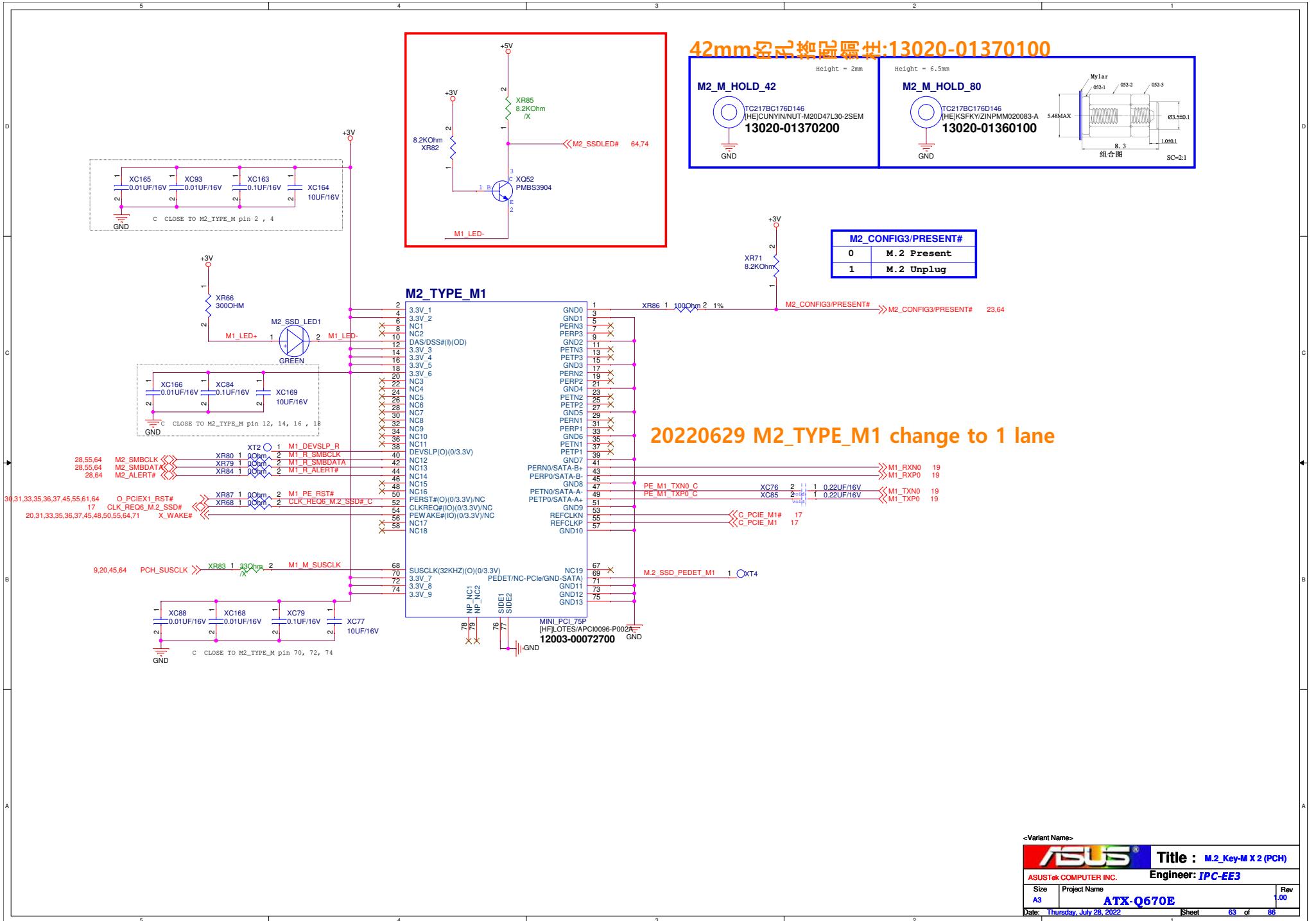


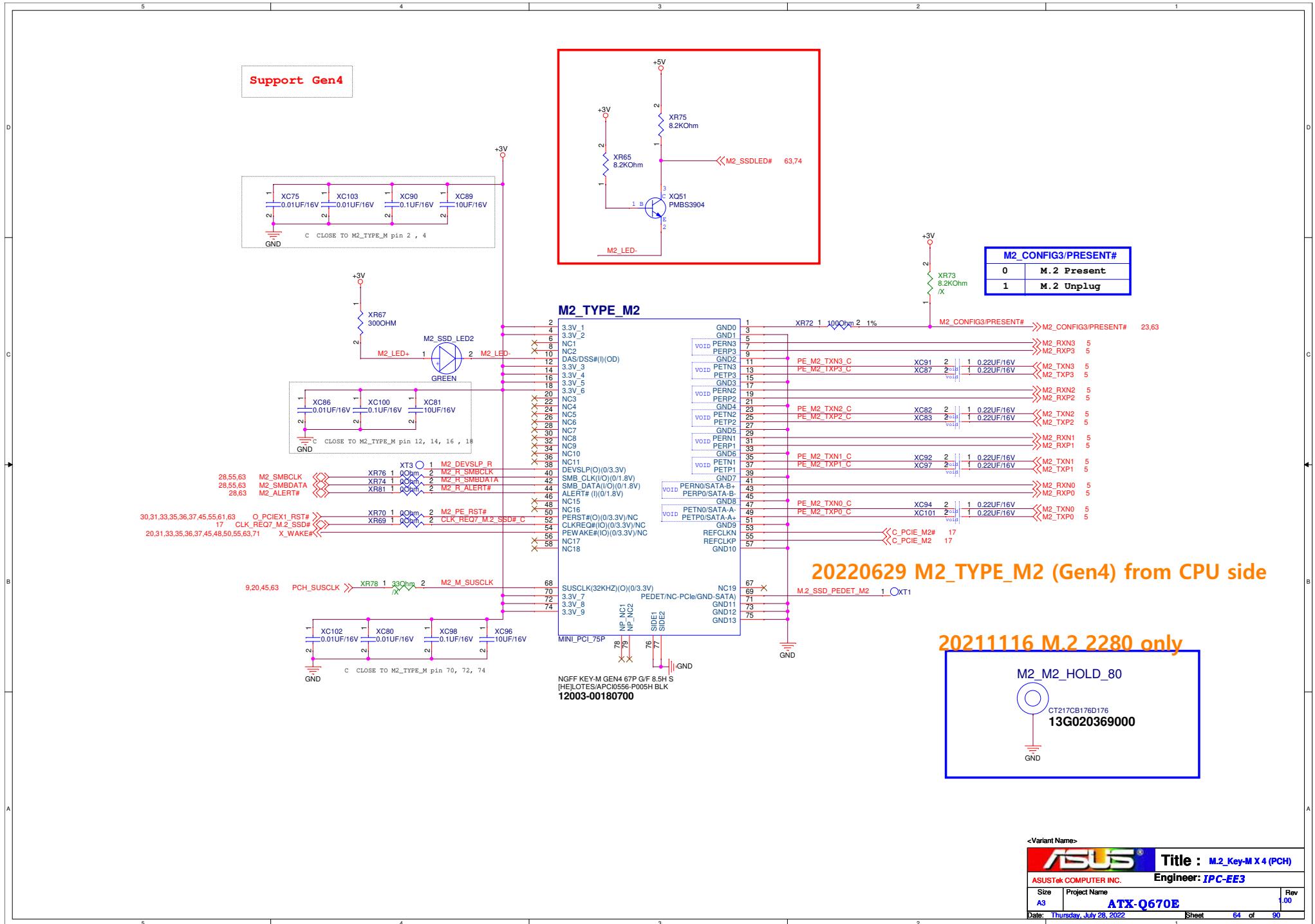


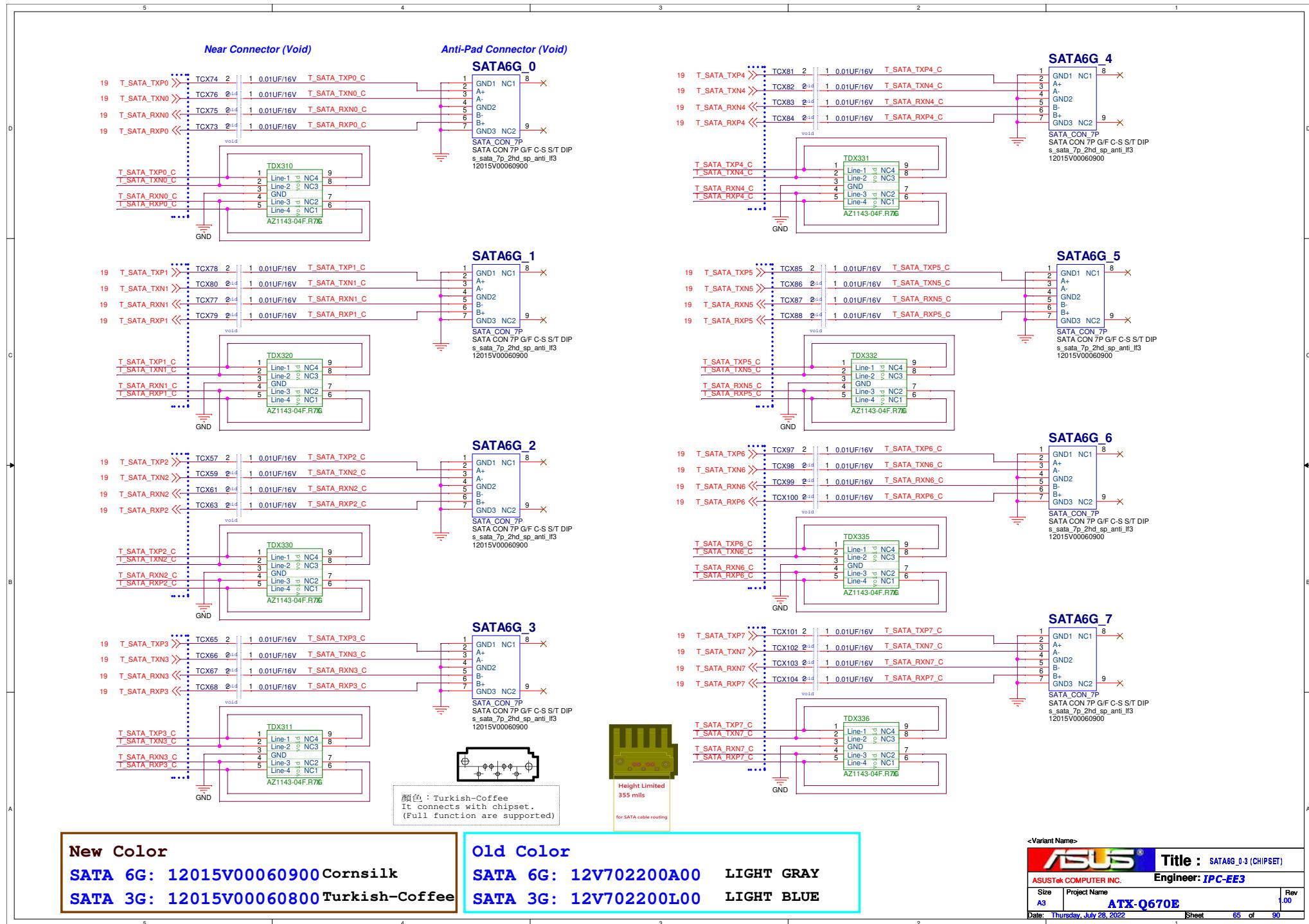


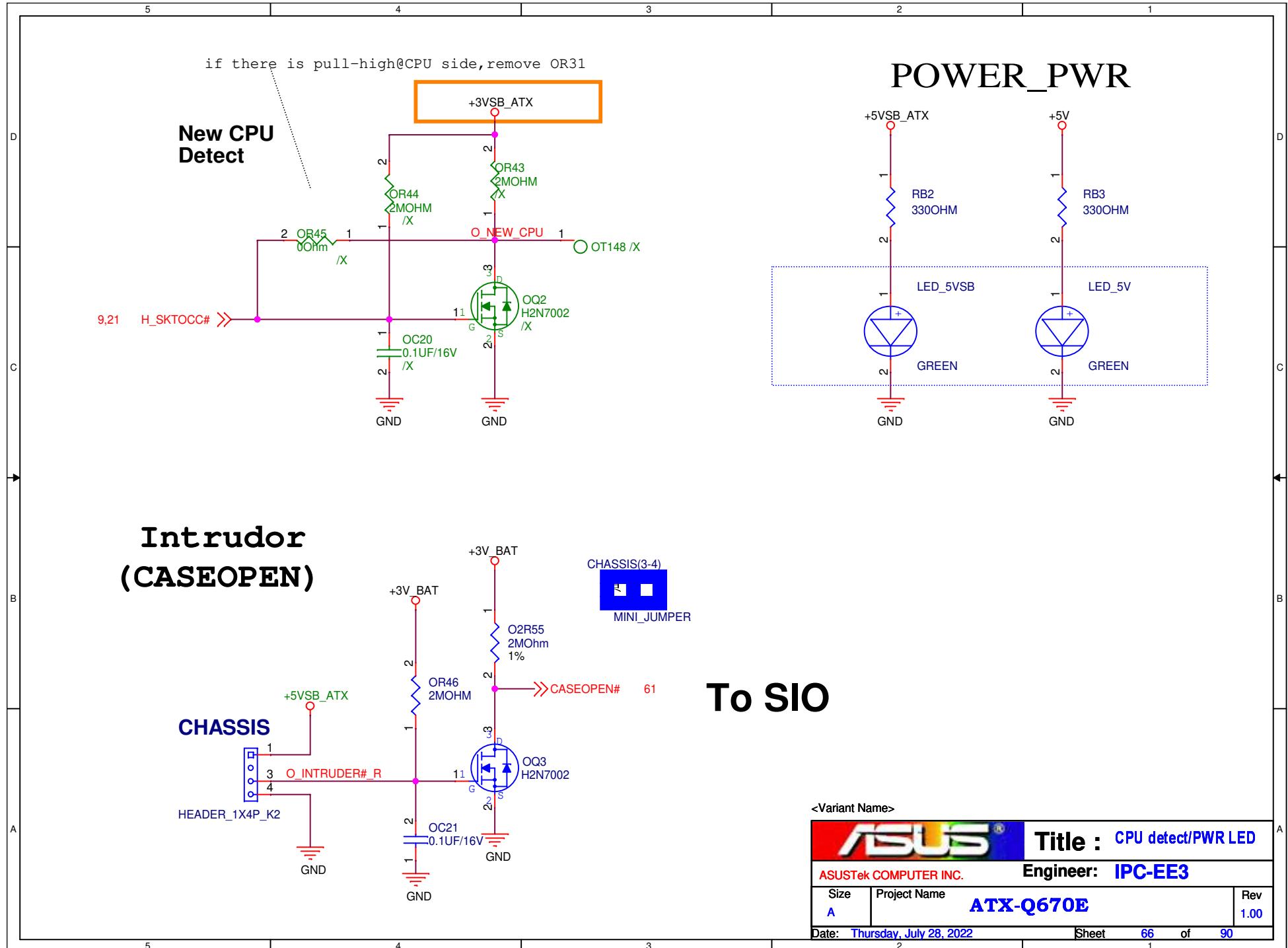


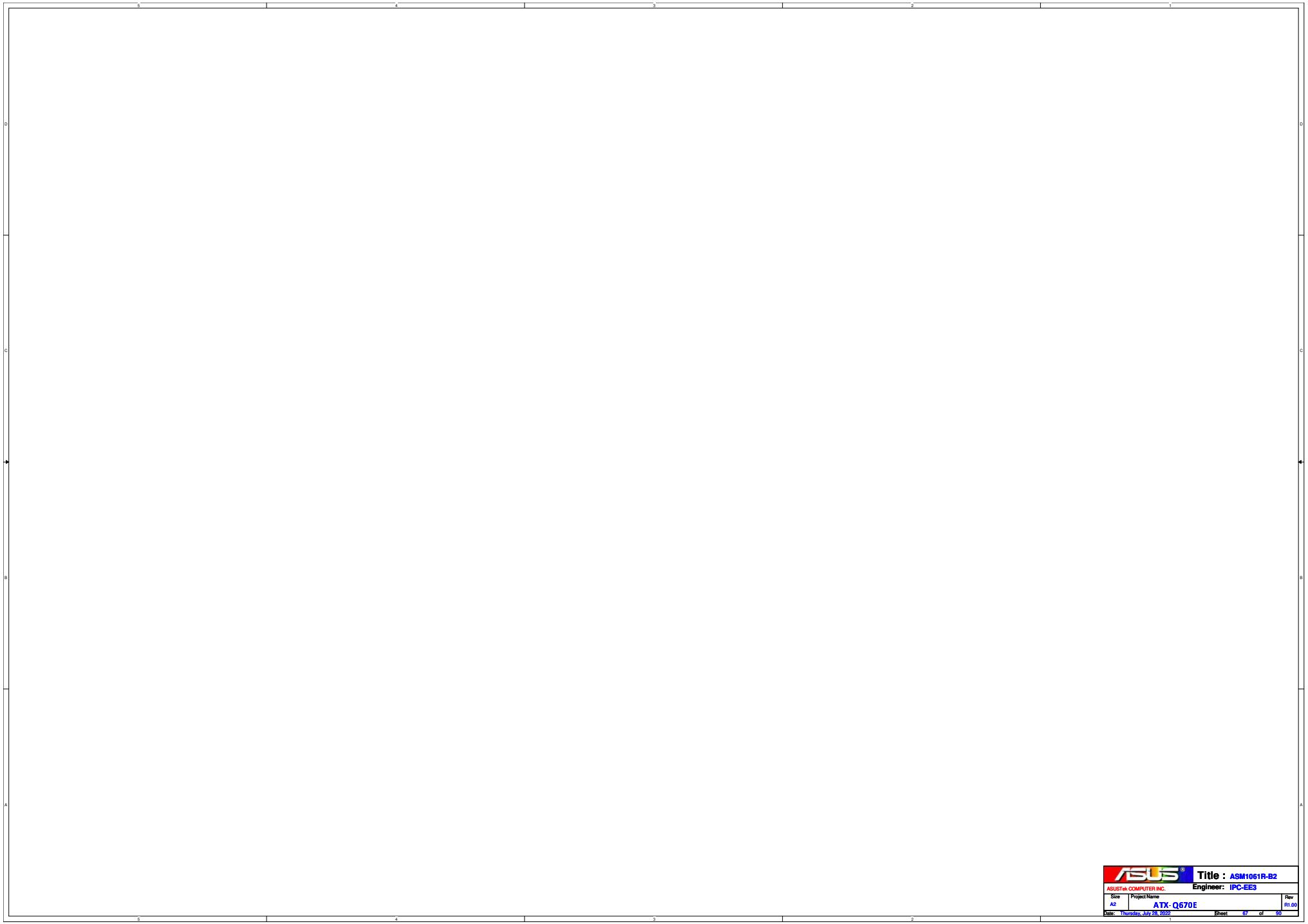


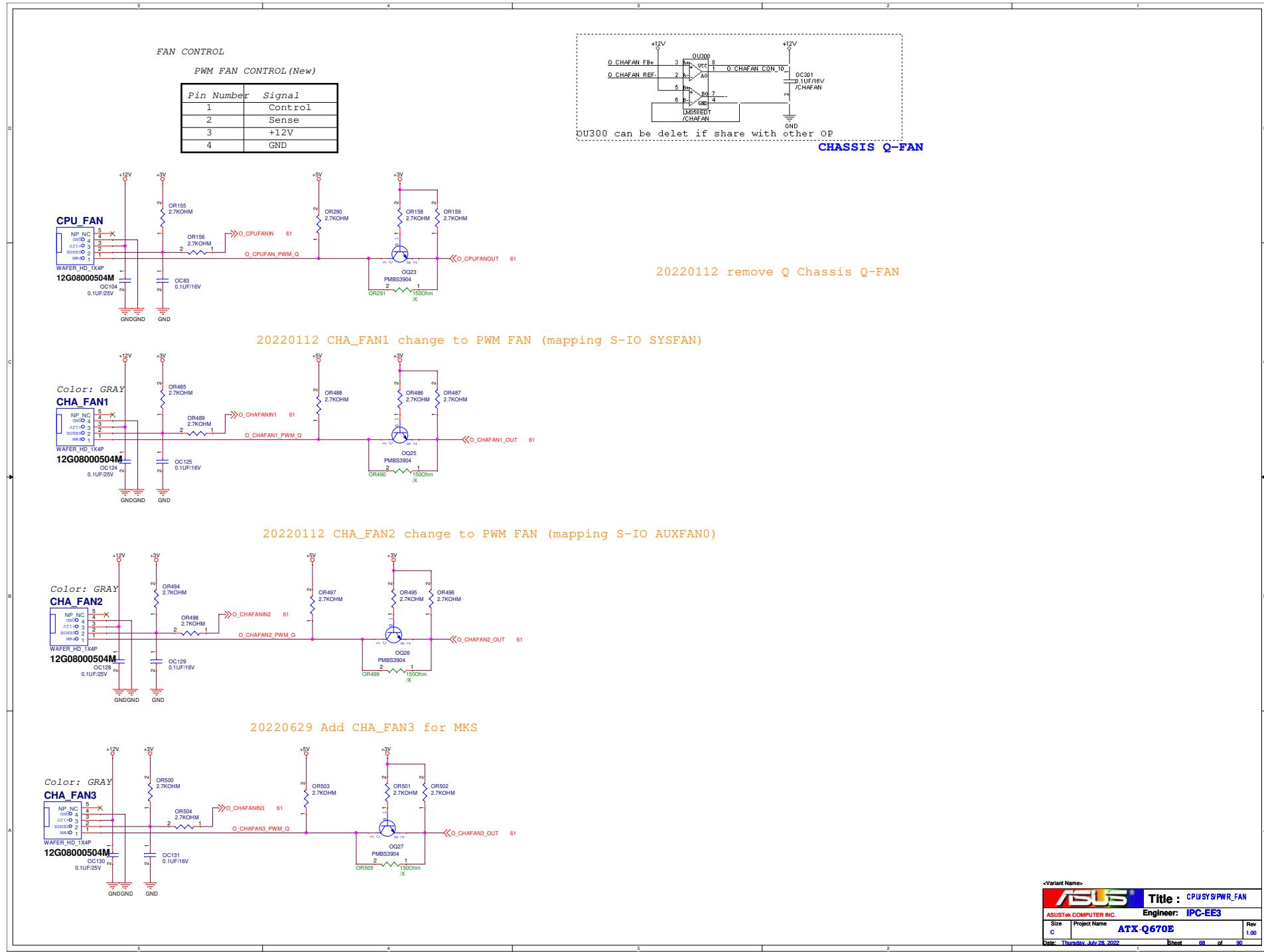


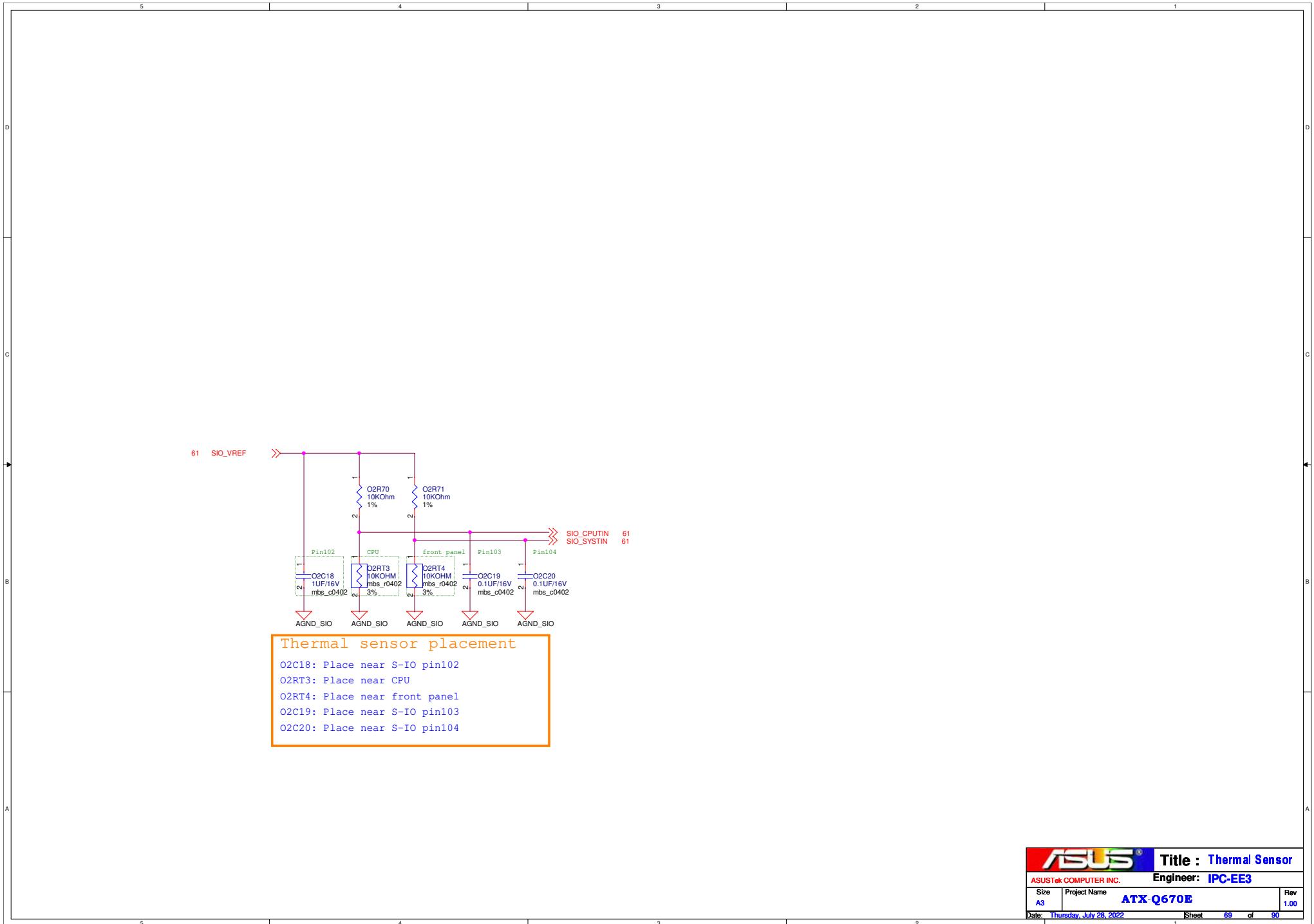


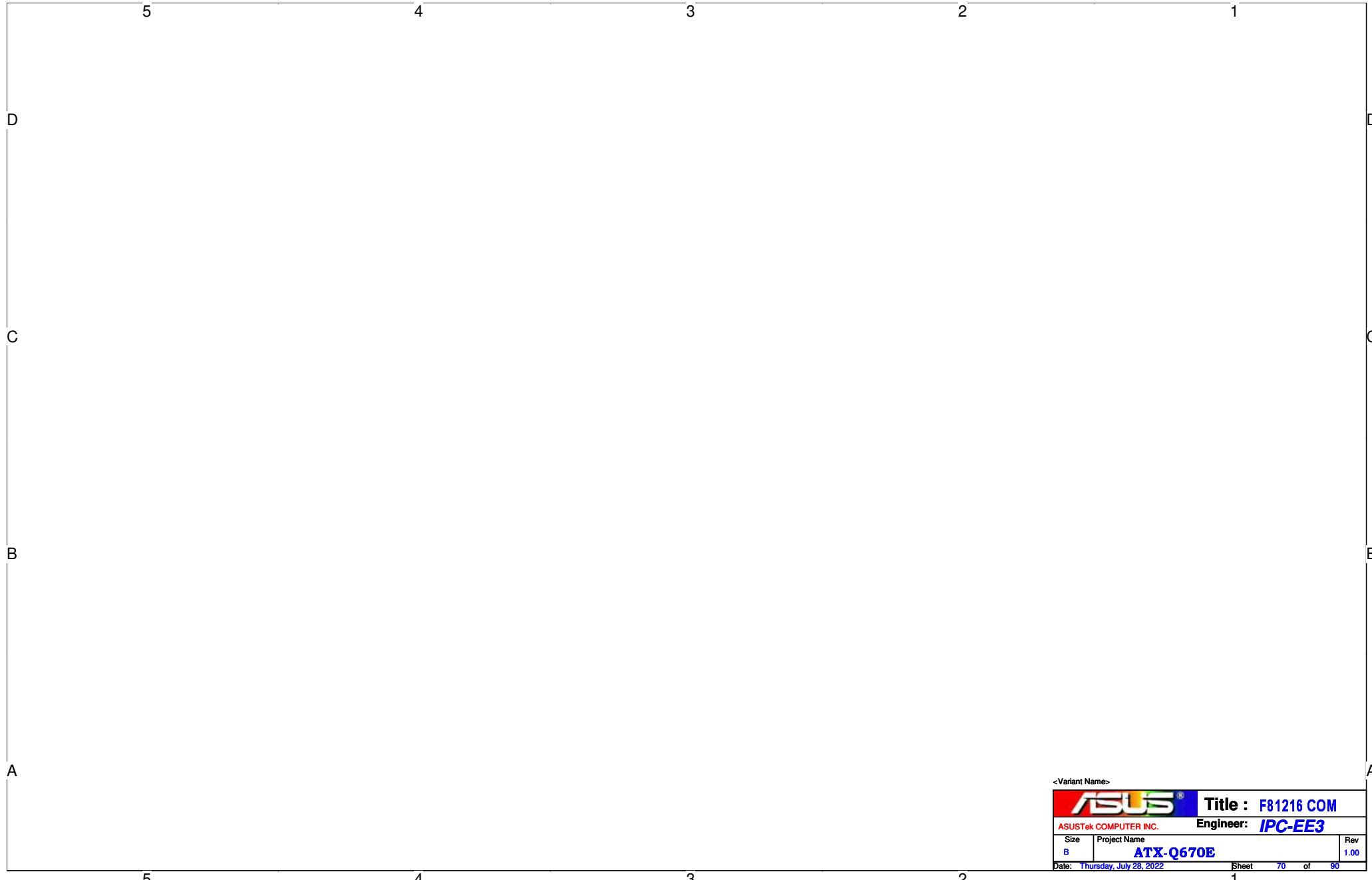




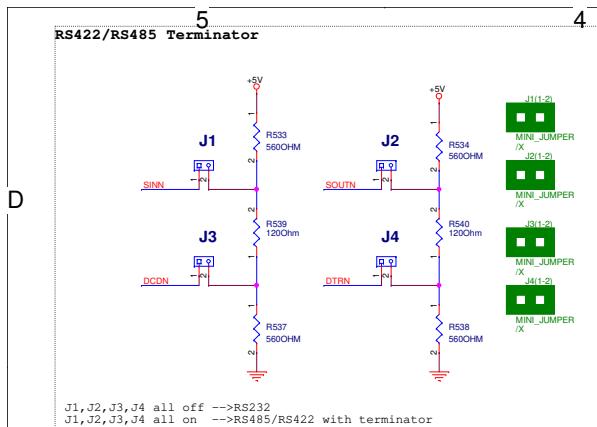








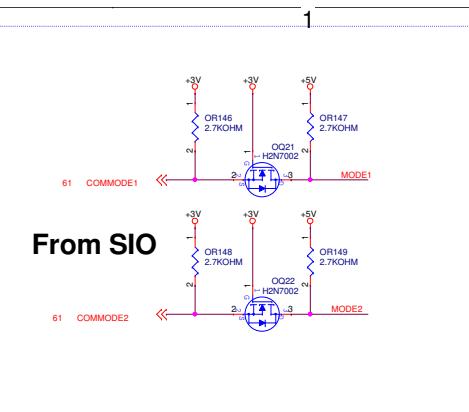
<Variant Name>
 Title : F81216 COM
ASUSTek COMPUTER INC. Engineer: IPC-EE3
Size B Project Name ATX-Q670E Rev 1.00
Date: Thursday, July 28, 2022 Sheet 70 of 90



| Mode Selection | | | |
|----------------|--------|--------|-------------------------------|
| SD | MODE_1 | MODE_2 | MODE |
| 0 | 0 | 0 | RS-422 |
| 0 | 0 | 1 | RS-232 |
| 0 | 1 | 0 | RS-485 (Driver Half Duplex) |
| 0 | 1 | 1 | RS-485 (Receiver Half Duplex) |
| 1 | X | X | Shutdown MODE |

Note:

Mode_1 and Mode_2 pin. Internal pull high = 625KΩ. As the current is very small ($\approx 15\mu A$), please use the hardware strapping or GPIO (BIOS) to select the modes.

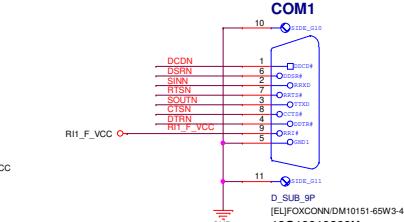


| (VDD = +5.0V ± 5%) | | | | | |
|-------------------------|-------------------------|-----|-----|-----|------|
| Parameter | Conditions | MIN | TYP | MAX | Unit |
| Supply Current (RS-232) | No Load, MODE = 01, | 2 | 30 | mA | |
| Supply Current (RS-485) | No Load, MODE = 10, 11. | 2 | | mA | |
| Supply Current (RS-422) | MODE = 00. | 2 | | mA | |
| Operating Temperature * | Symbol: T | -40 | 85 | ° C | |

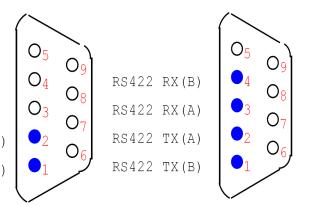
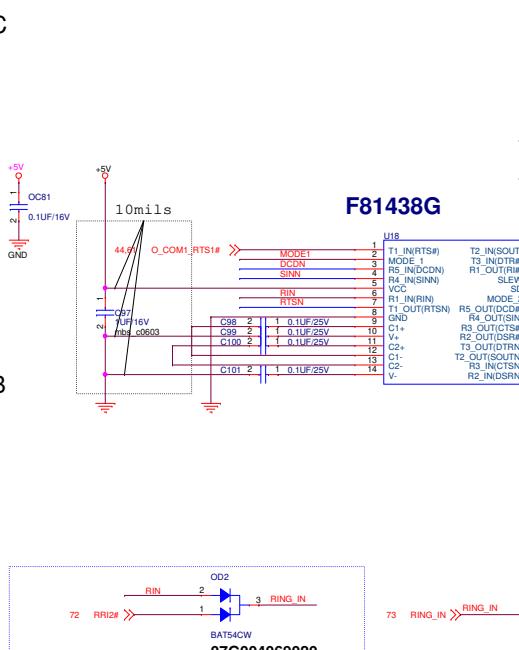
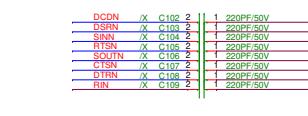
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|-----------------|------|------|------|------|-------------|
| Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28 | | | | | | |
| Logic Input Voltage HIGH | V _{IL} | 2.4 | | | V | VDD = 5.0 V |
| Logic Input Voltage LOW | - | - | - | 0.8 | V | |
| Logic Input Pull-up Current | - | - | - | ±15 | µA | |
| Driver Input Pull High Current | I _{IT} | - | - | ±15 | µA | |

| COM1_V1(5-6) RI & Voltage SEL |
|-------------------------------|
| 1-2 12V |
| 3-4 5V |
| 5-6 RI (Default) |

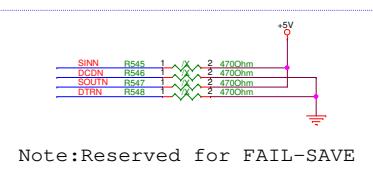
COM1_V1(5-6)

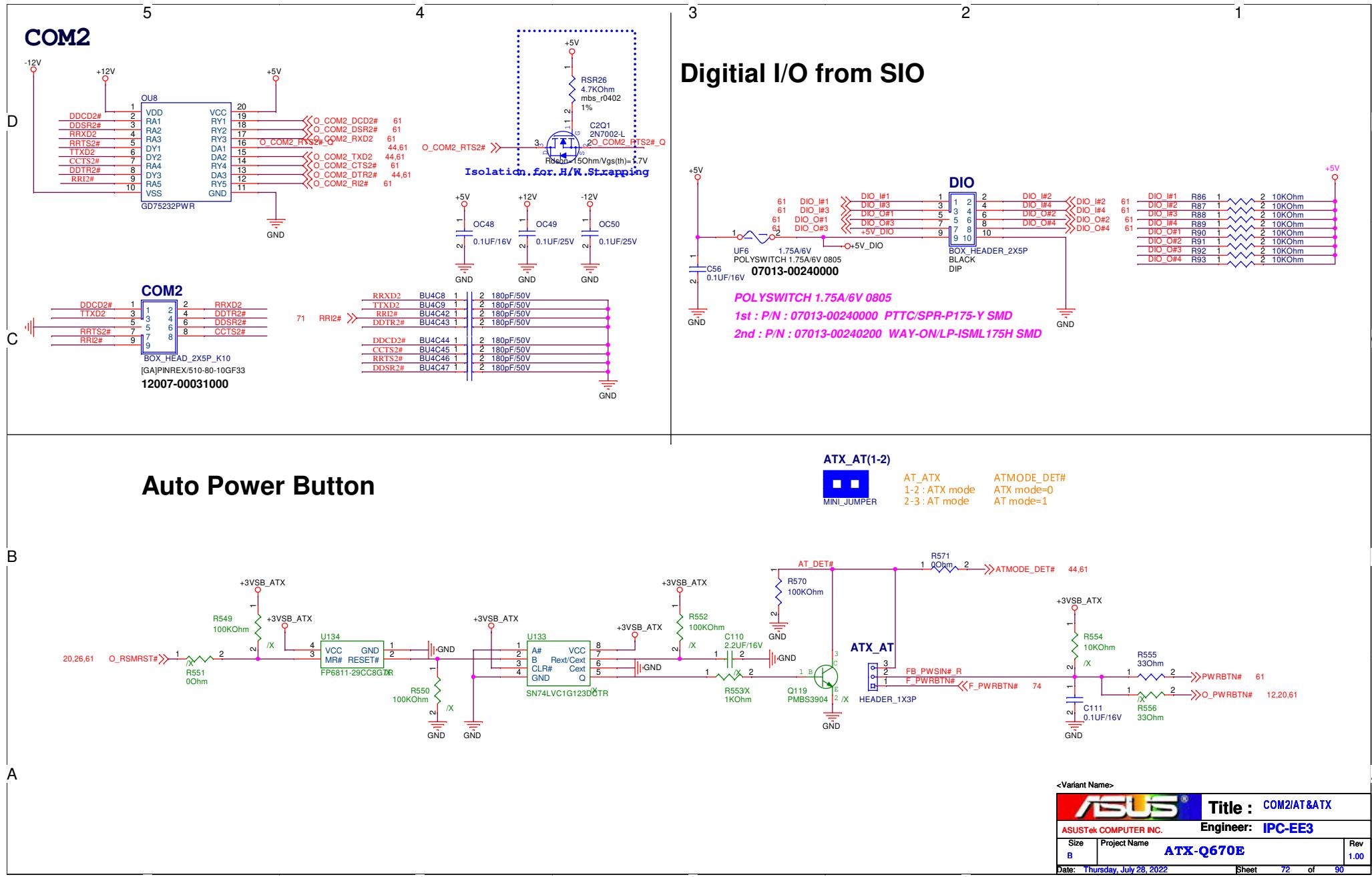


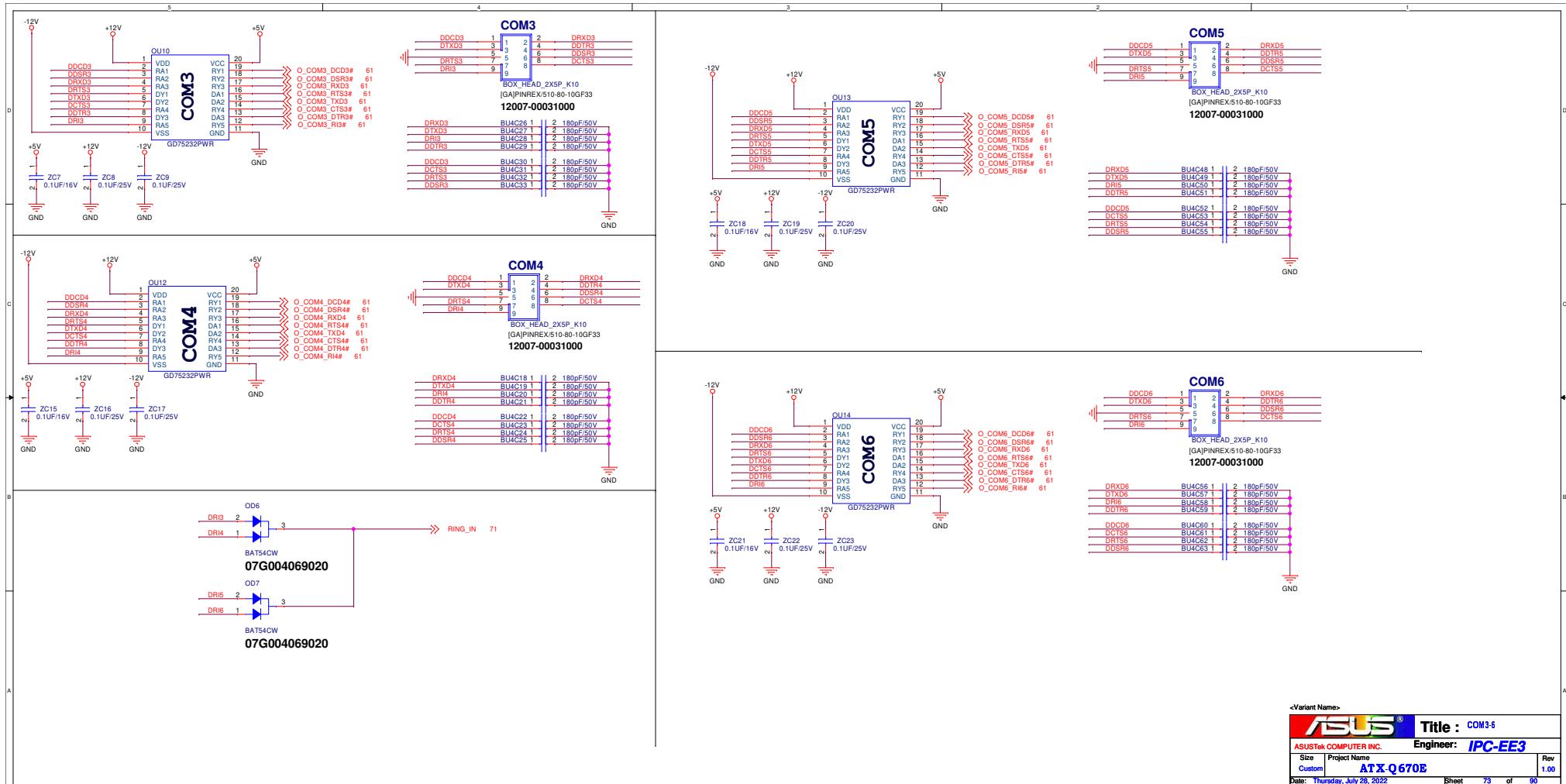
Close to COM port connector

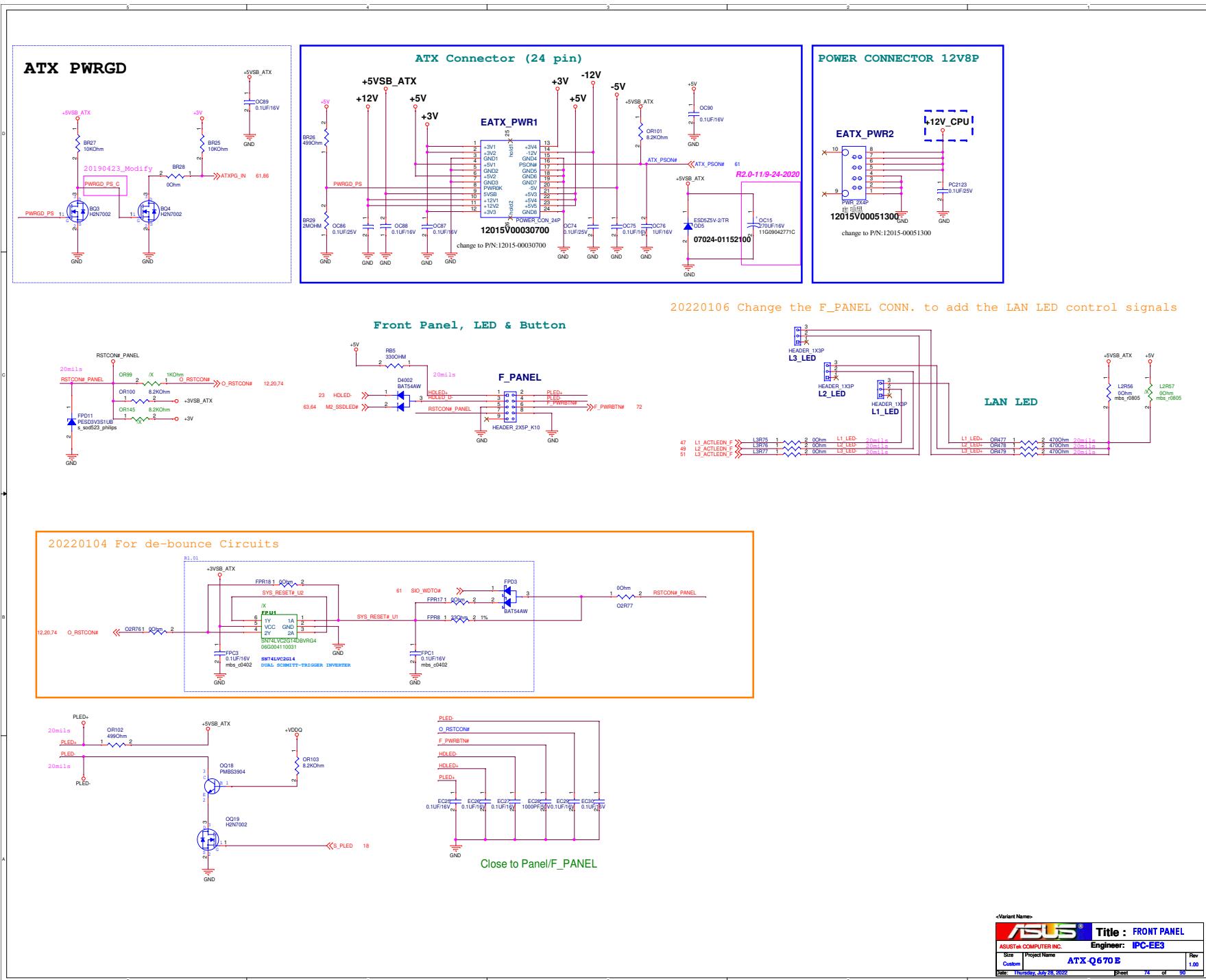


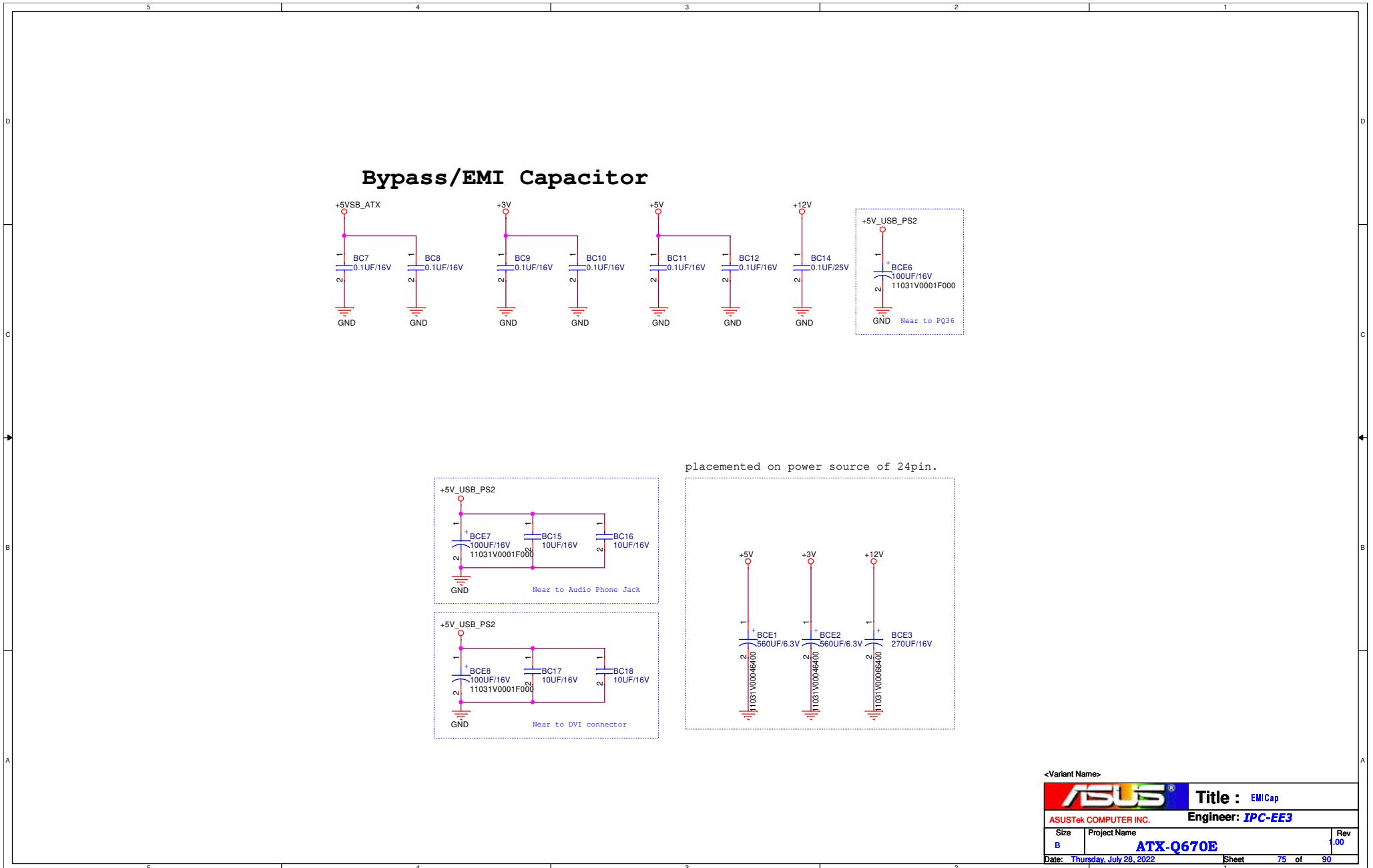
| Maximum Slew rate control | | |
|---------------------------|---------|---------------|
| SLEW | RS-232 | RS-485/RS-422 |
| 0 | 1Mbps | 10Mbps |
| 1 | 250Kbps | 250Kbps |

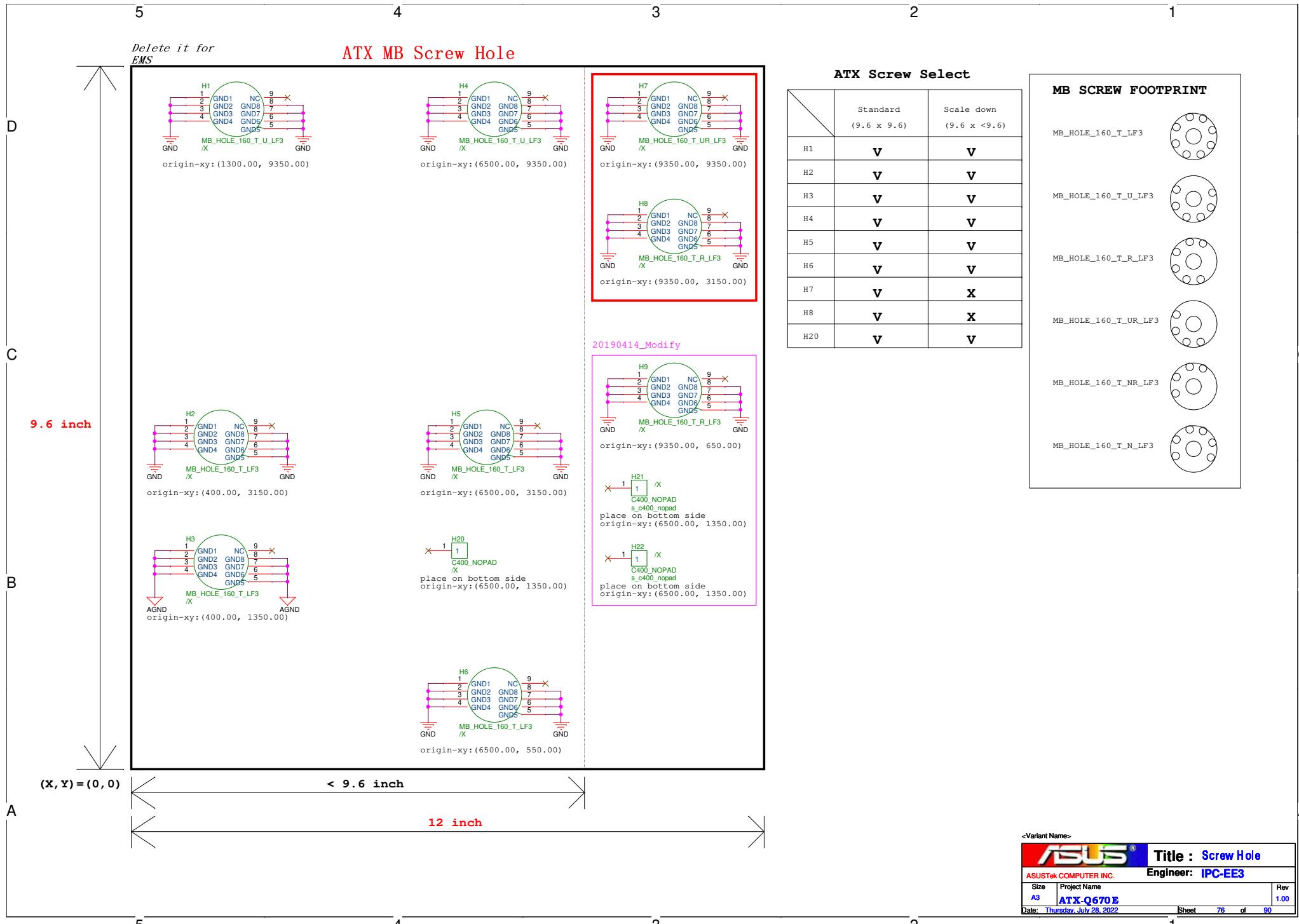






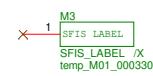




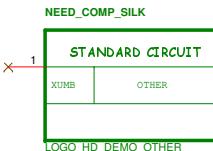


Selling Point

20220104 add no pad_TP for layout request



The U-DIMM Order of Insertion



ATX-Q670A R1.00 PCB-08 :

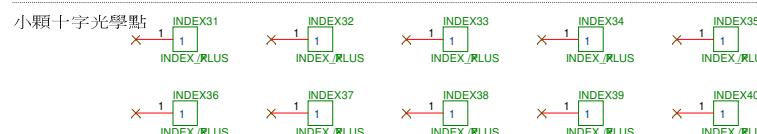
08001-19060100 ATX-Q670A R1.00//GECS 12*9.6,6L(1).1.6,1080
08001-19060200 ATX-Q670A R1.00//TRUSTECH 12*9.6,6L(1).1.6,1080
08001-19060000 ATX-Q670A R1.00//DF 12*9.6,6L(1).1.6,1080

Fiducial Mask (光學點)

大顆十字光學點

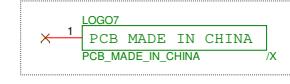
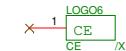
光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除。

2012/09/11

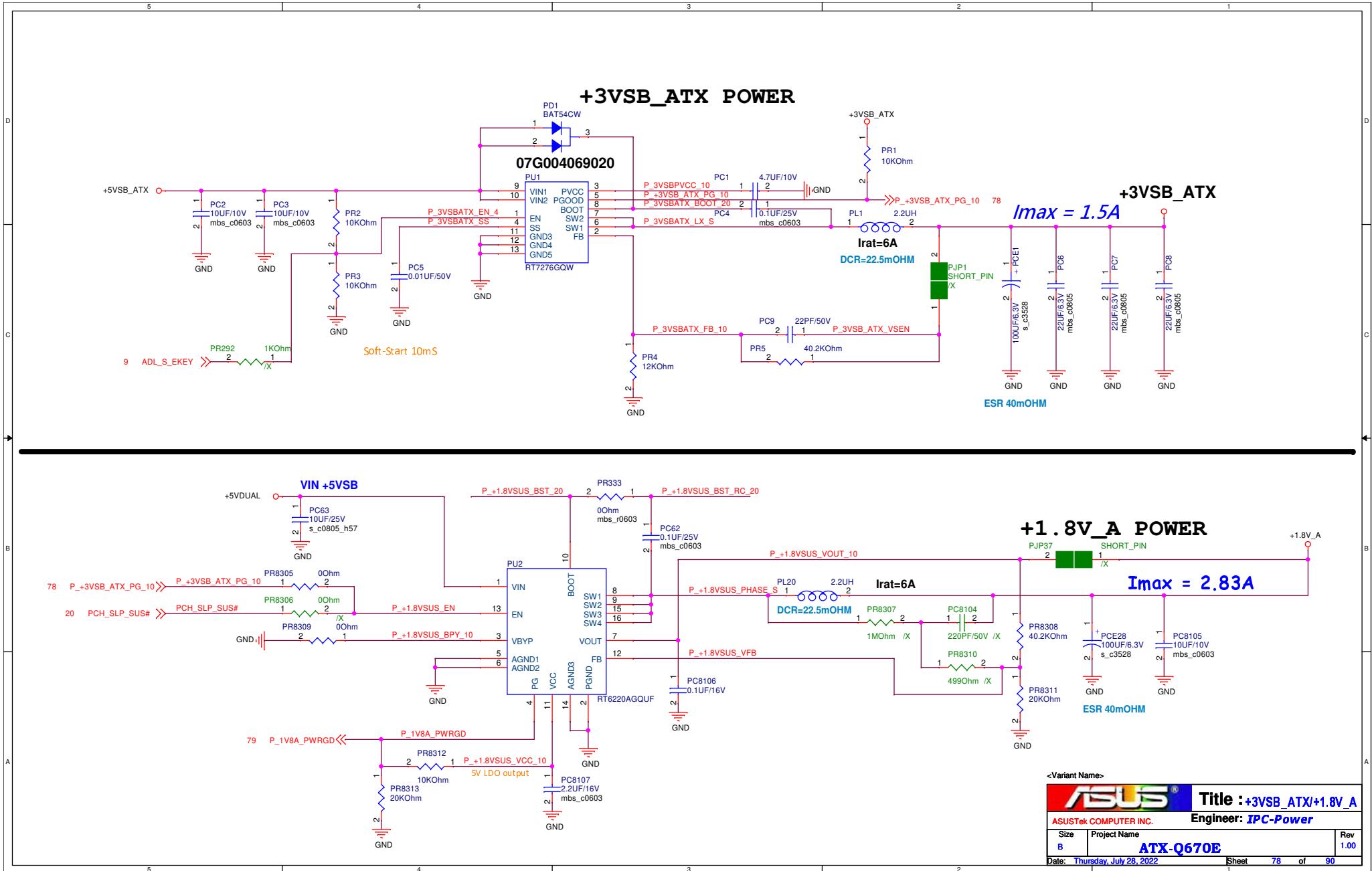


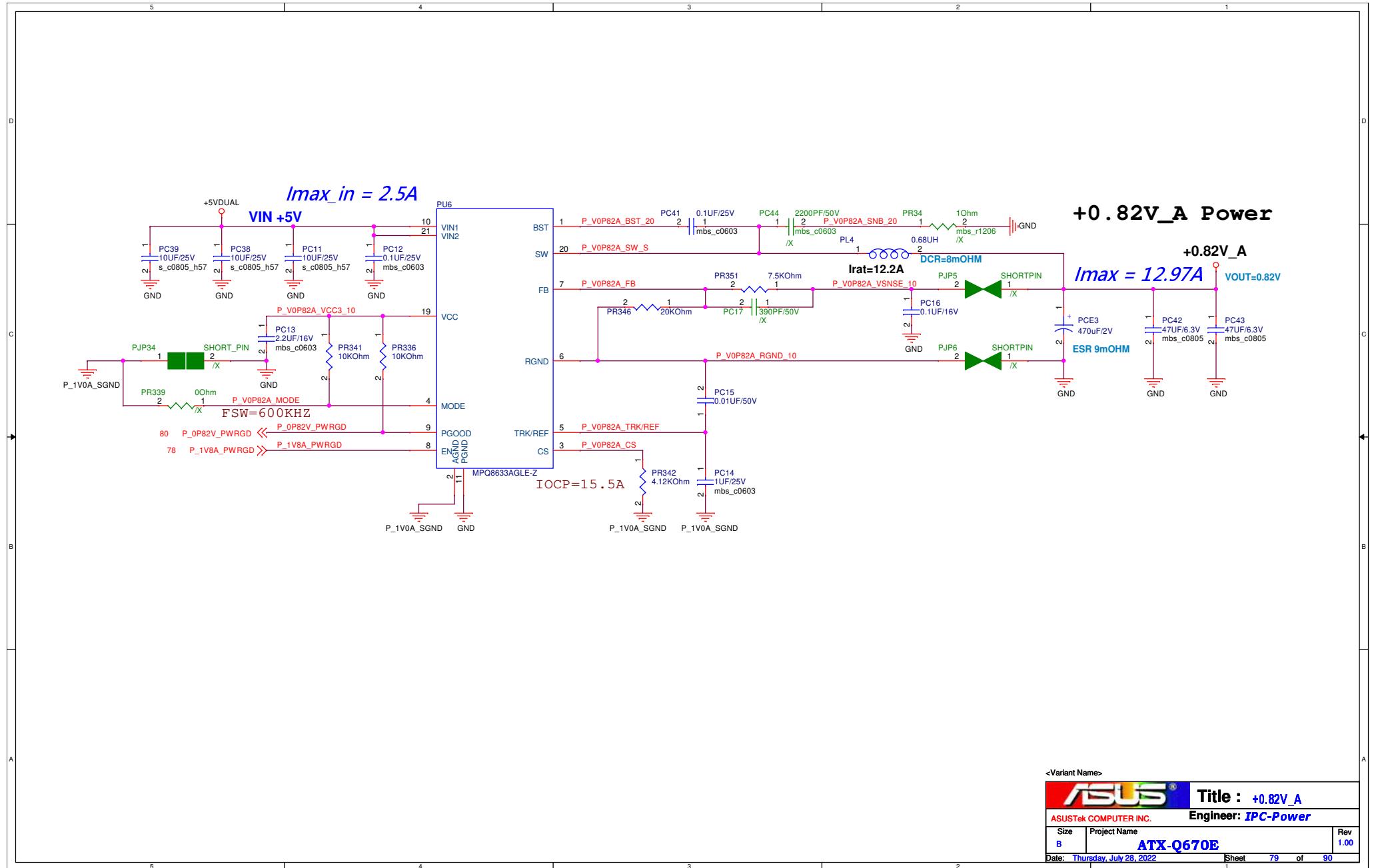
Logo

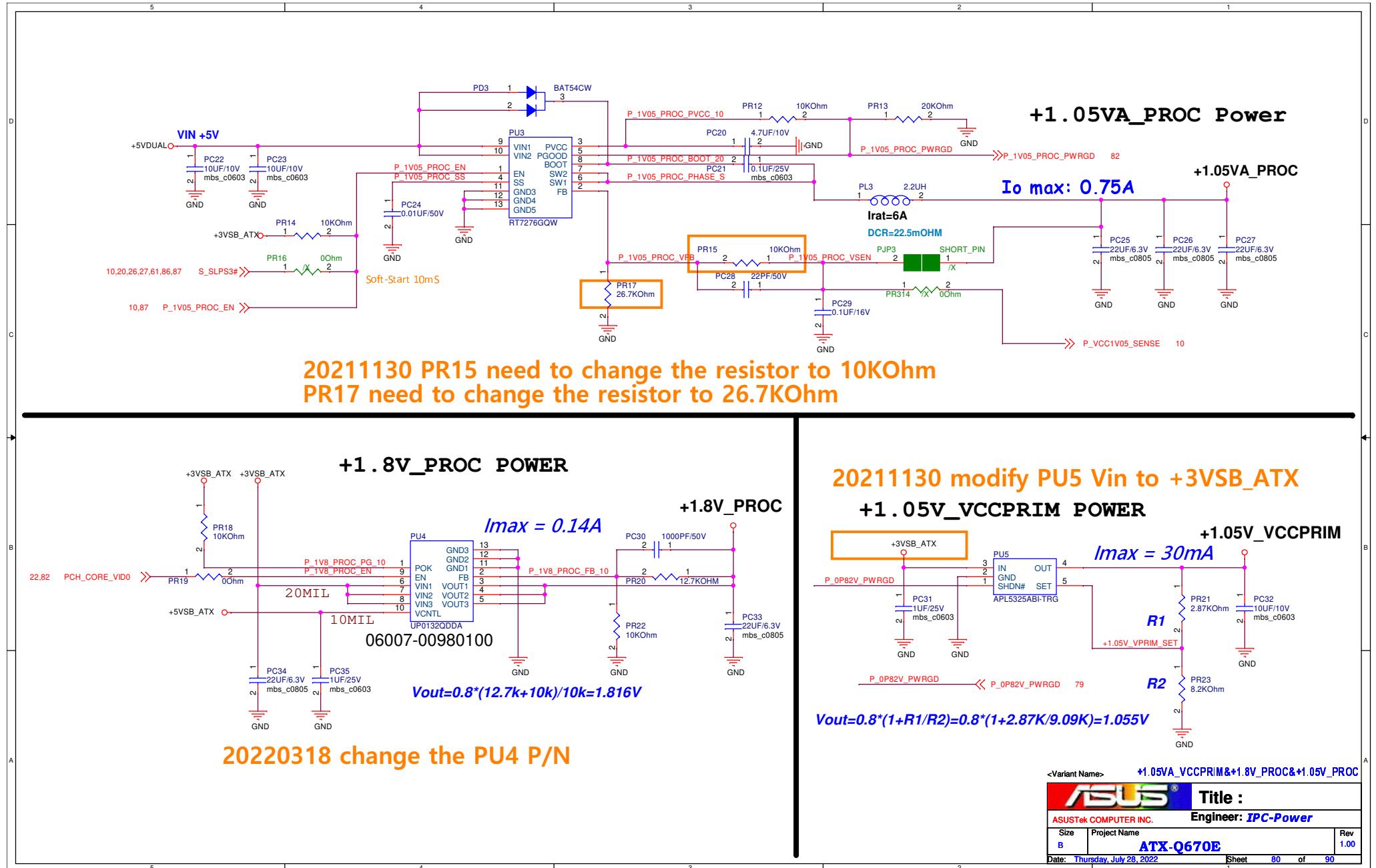
common Logo for all projects



| Title : Selling Point_Logo | | |
|-------------------------------|----------------------------------|-------------------|
| ASUSTek COMPUTER INC. | | Engineer: IPC-EE3 |
| Size A3 | Project Name ATX_Q670E | Rev 1.00 |
| Date: Thursday, July 28, 2022 | Sheet 77 | of 90 |

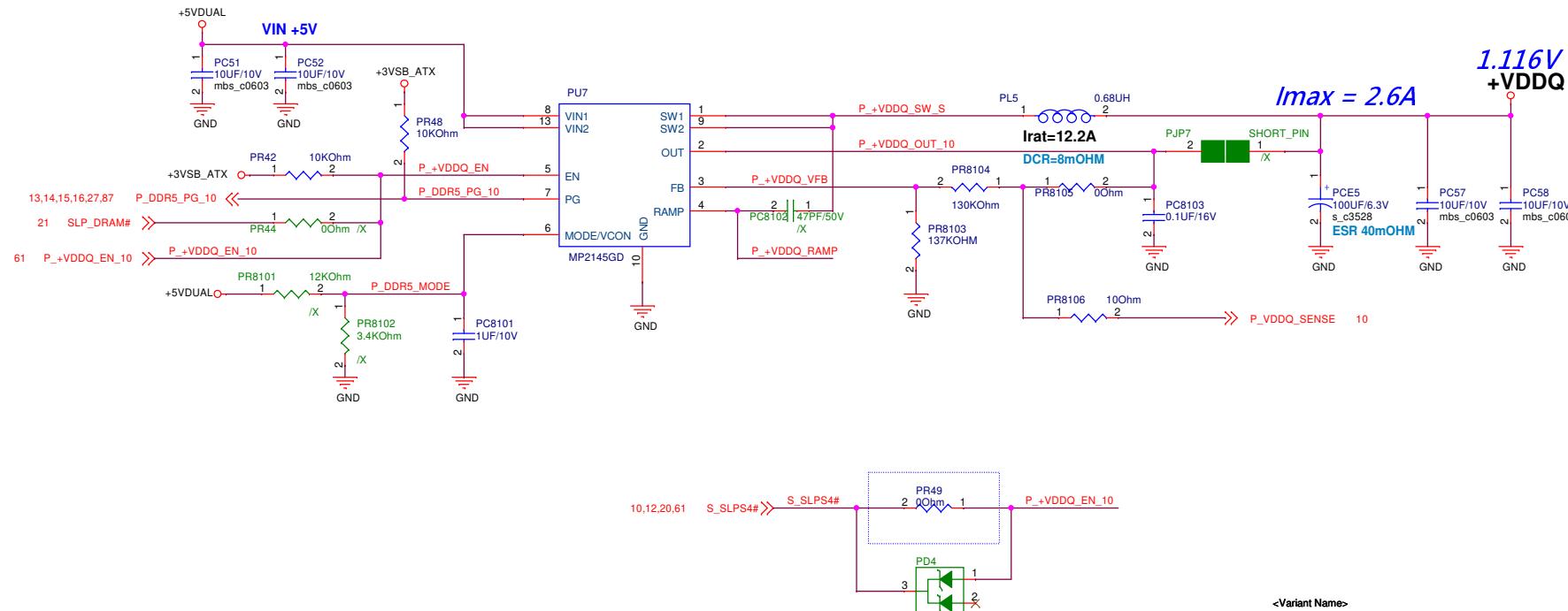
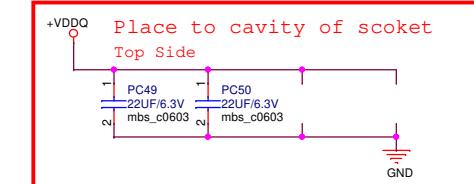
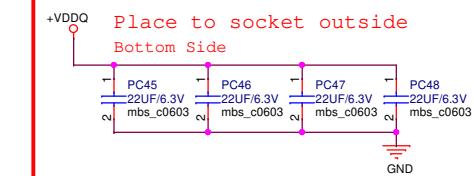




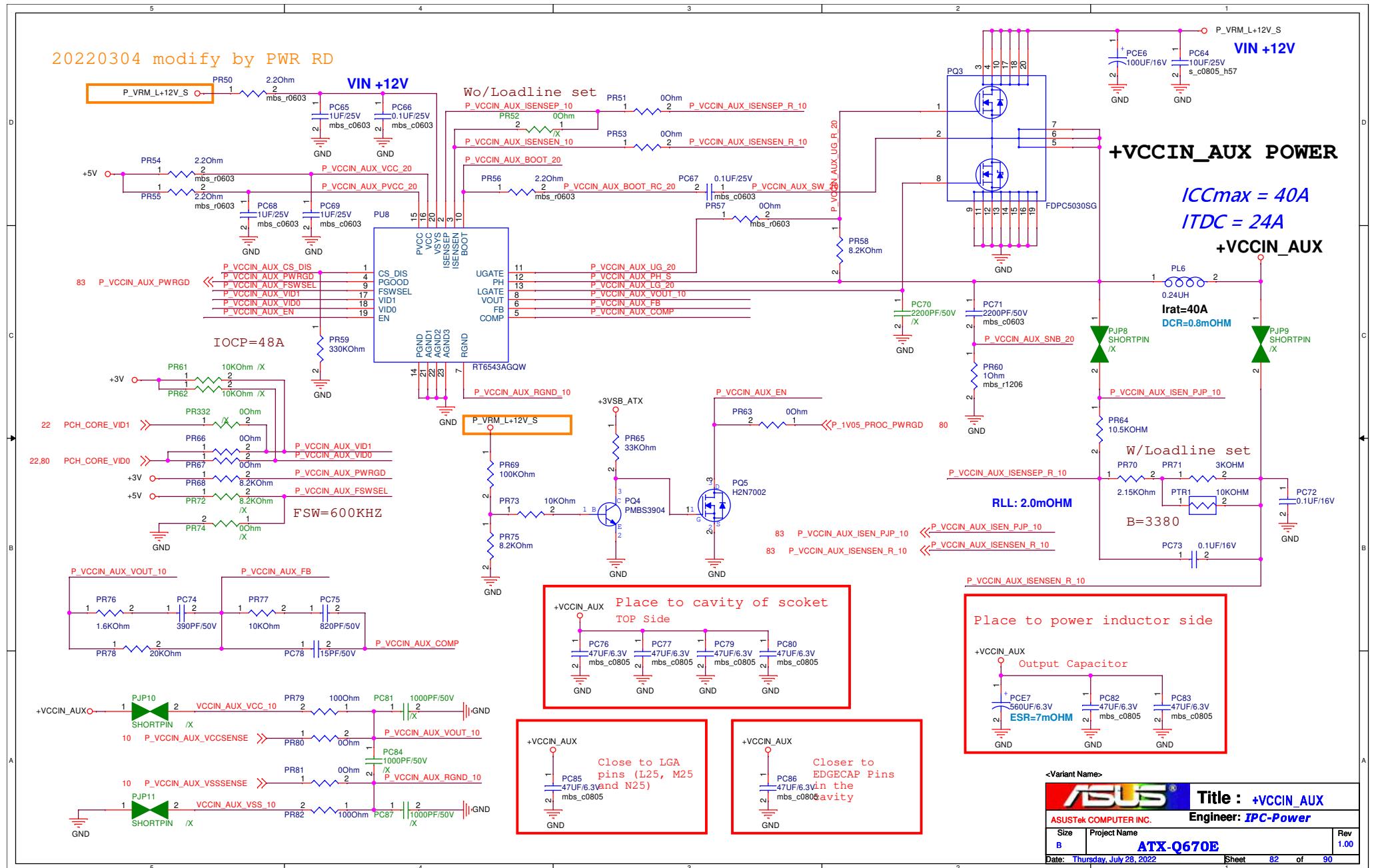


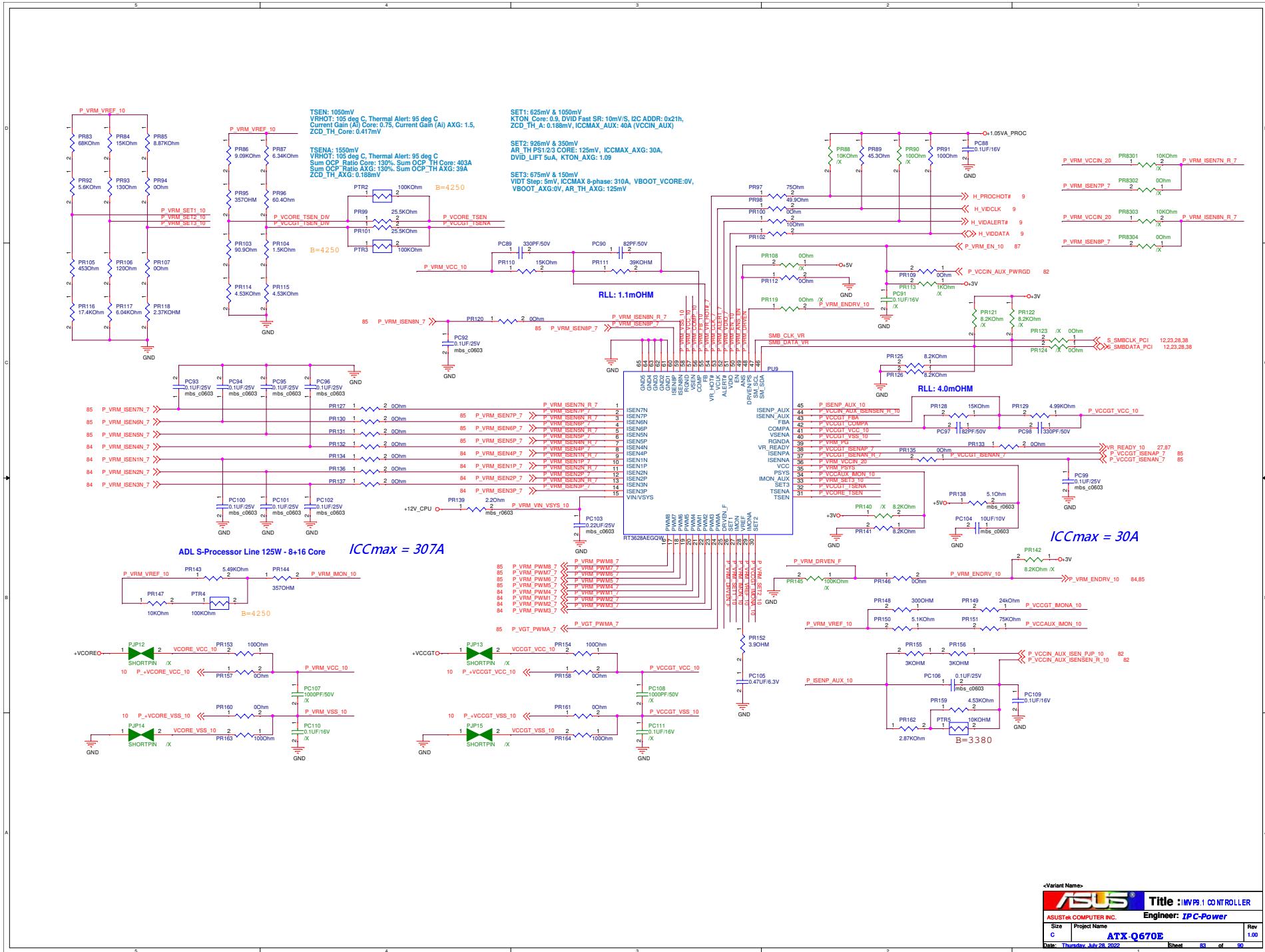
+VPPDDR POWER

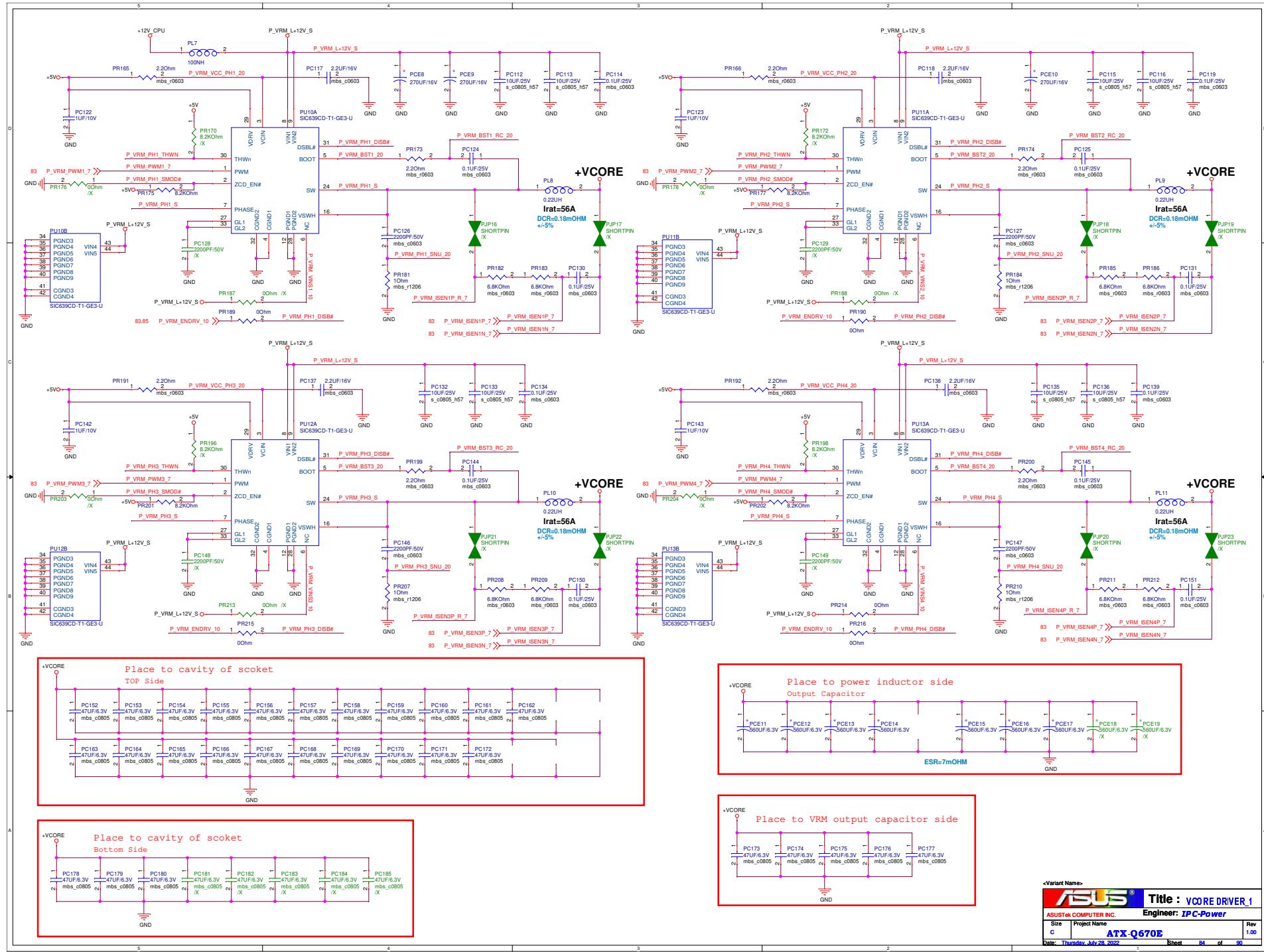
Delete +VPPDDR Power, It is directly powered by DDR5 DIMM.

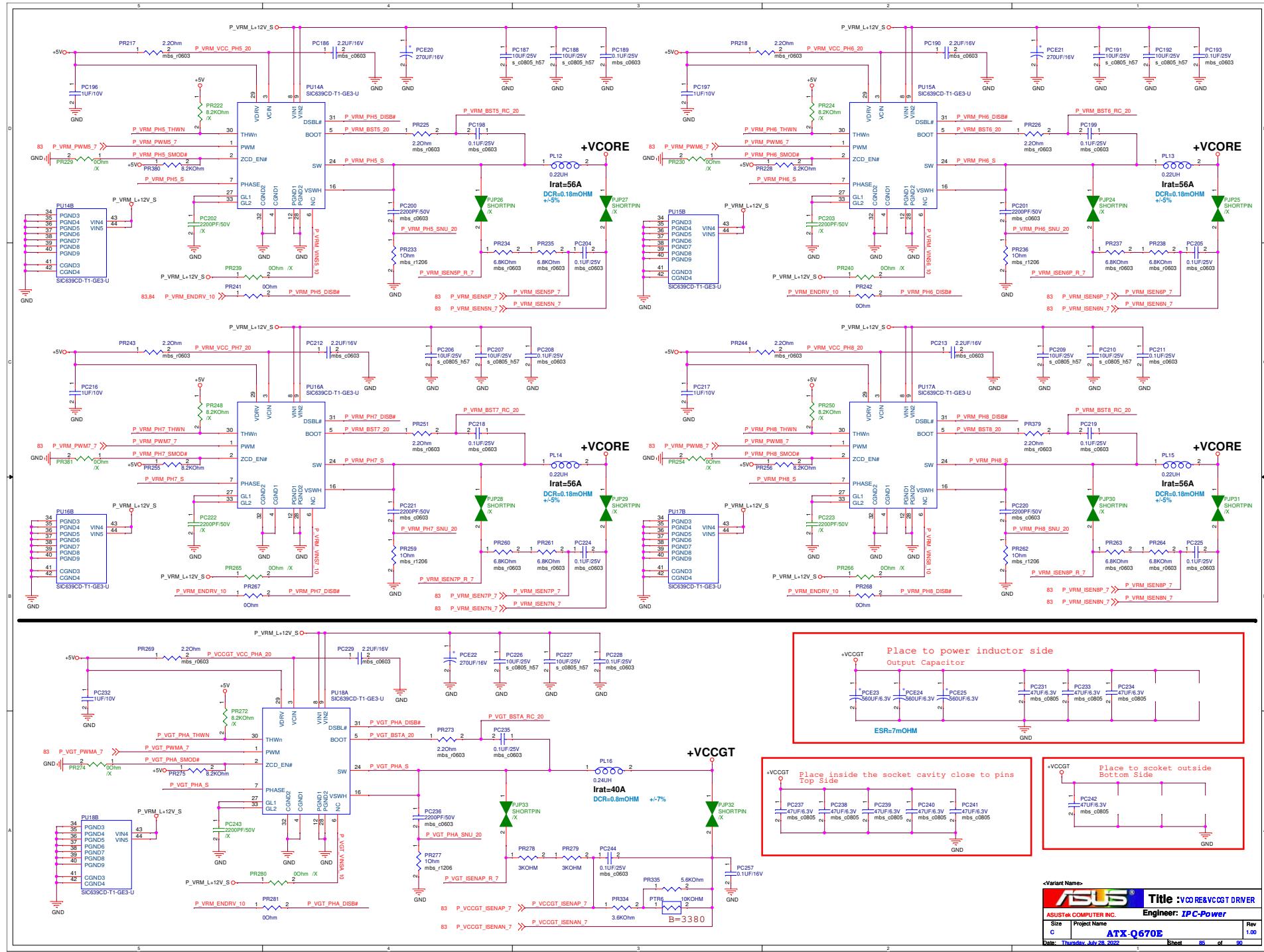


| <Variant Name> | | Title : +VDDQ | |
|-----------------------|--------------|-------------------------------|----------------|
| ASUSTek COMPUTER INC. | | Engineer: IPC-Power | |
| Size | Project Name | Rev | 1.00 |
| B | ATX-Q670E | Date: Thursday, July 28, 2022 | Sheet 81 of 90 |

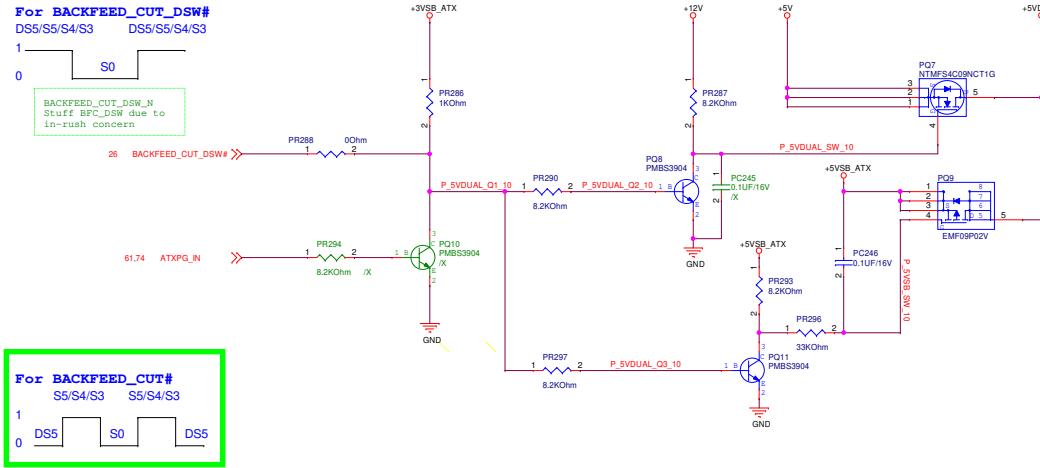








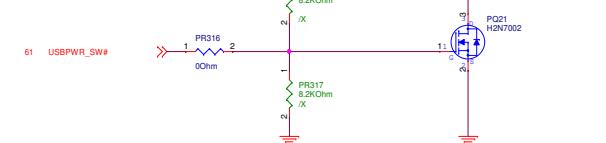
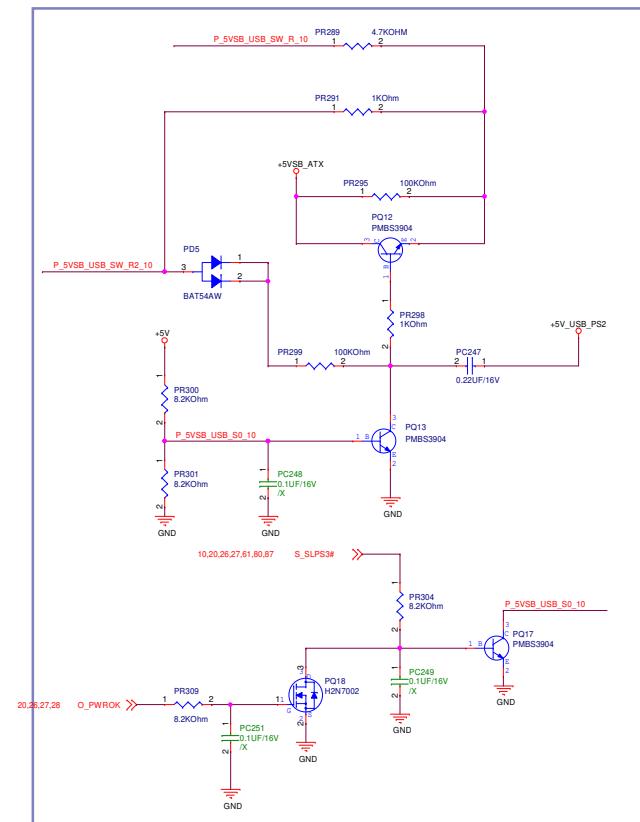
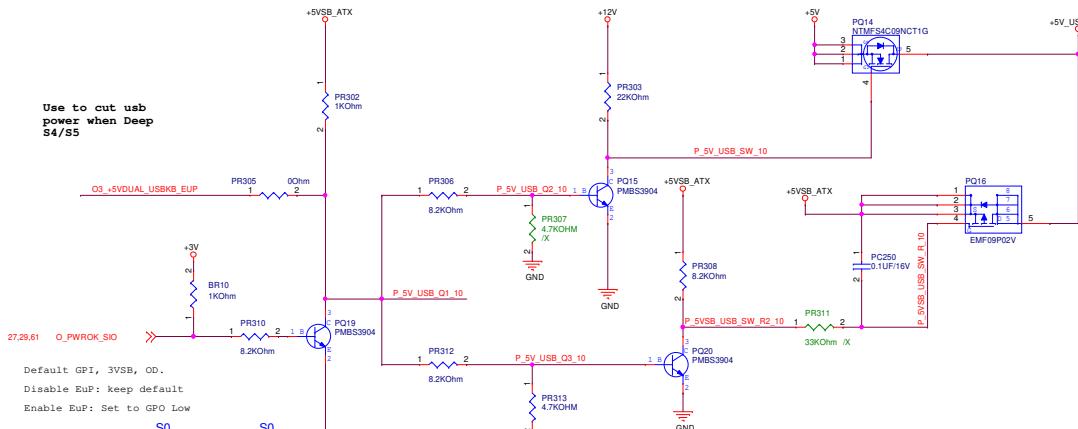
+5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT

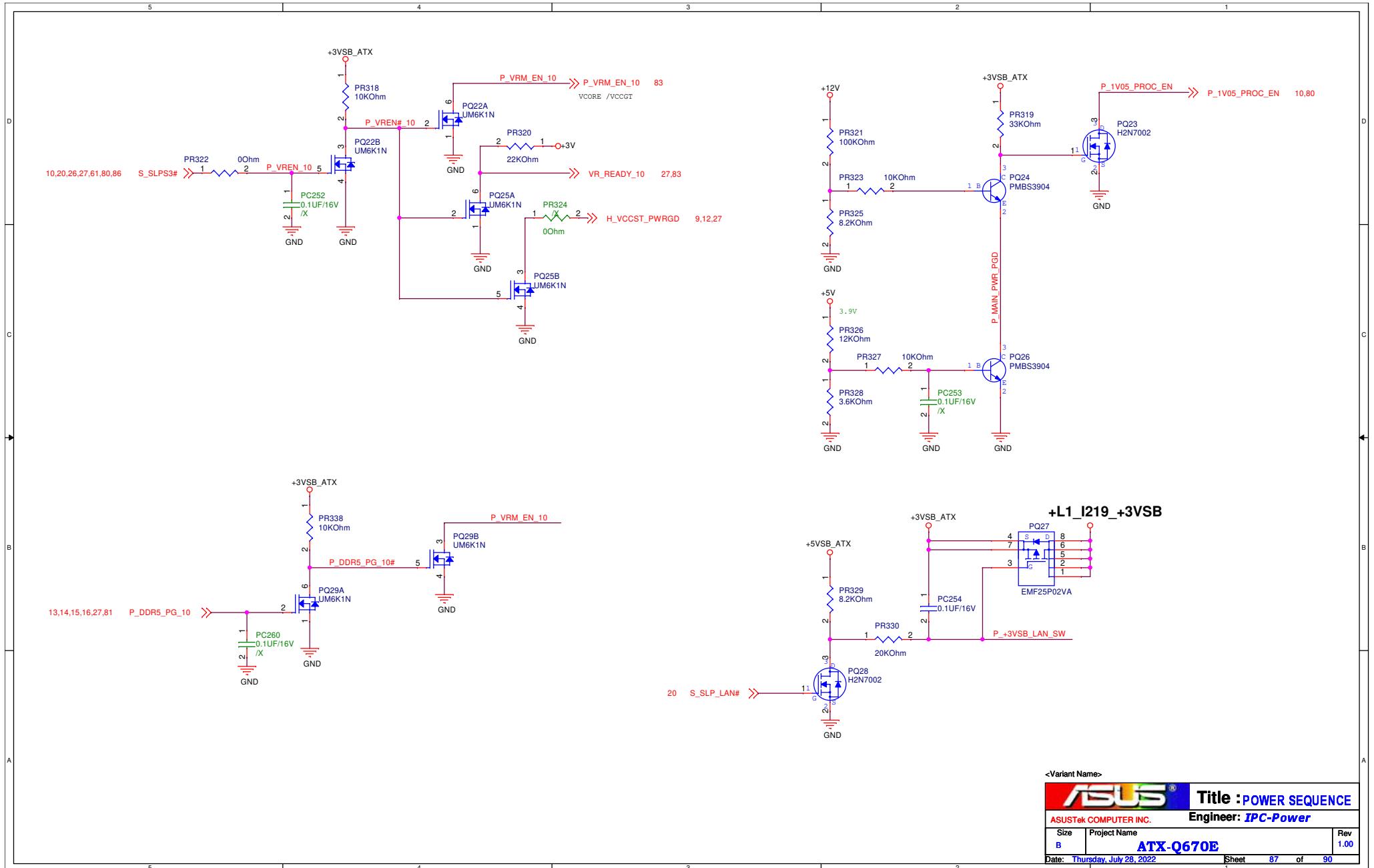


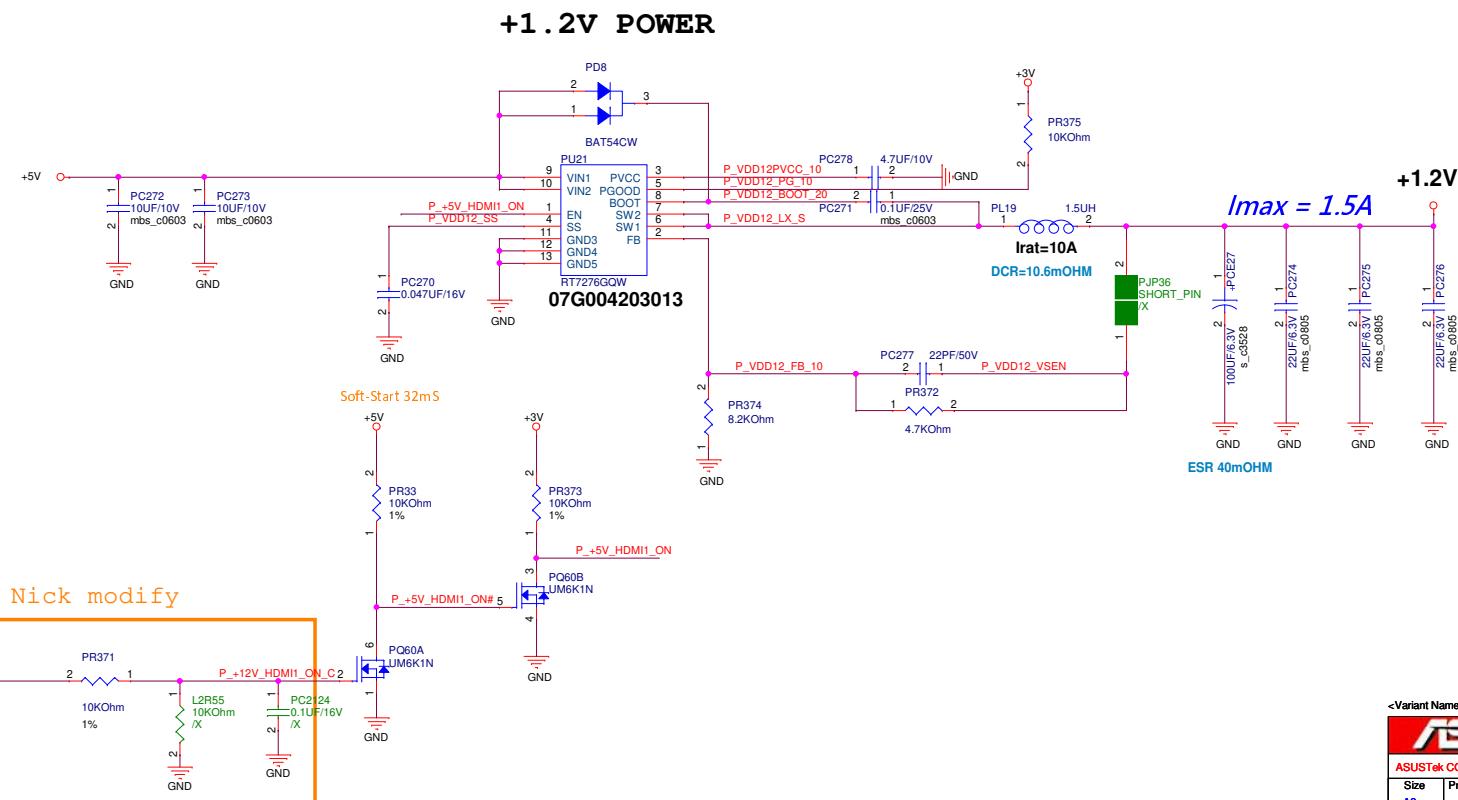
+5VDUAL_USBKB_UVP CIRCUIT



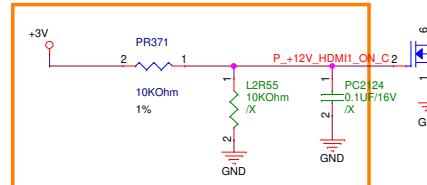
+5VSB_USBKB VOLTAGE & POWER CIRCUIT







20211206 Nick modify



<Variant N

 **ASUS**[®]
 ASUSTek COMPUTER INC. **ATX-Q670E** Title : +3VA_EC/+12V
Engineer: IPC-Power

| | | |
|---|--------------|--|
| History 2022/6/24 | R1.10 | |
| 01) modify the VCO Power IC pin35 (PVSY) mount PR41, unmount PR140, p83 | | |
| 02) modify the SPI termination resistance FR30 and change to 750ohm, p29 | | |
| 03) modify the re-driver strapping resistance; Unmount the S-IO port reserved for eSPI, p34 | | |
| 04) Mount the TR98 for TPM VDO_P14 power, p30 | | |
| 05) Mount the OR417, SR151 for PCI REQ, p17 | | |
| 06) Unmount the OR145, mount the OR100 for RESET BUTTON, p74 | | |
| 07) modify the COM2 pin define, follow MAX-Q470A, p72 | | |
| 08) modify the COM2/COM4/COM5/COM6 pin define, follow MAX-Q470A, p73 | | |
| History 2022/6/24 | R1.10 | |
| 01) Add the ODM(PTR14) for TPM pin2 connect to GND, p30 | | |
| History 2022/6/28 | R1.10 | |
| 01) Change the +1.8V_A power solution due to IC EOL, follow FMC-H610, p78 | | |
| History 2022/6/29 | R1.10 | |
| 01) US820 Type-A port change to PWR_SW, p62 | | |
| 02) modify the OC pin HW design to avoid leakage current, p56/p57/p58/p59 | | |
| 03) Add CBA_FAN3 for M6S, p61/p68 | | |
| 04) M2_TYPE_M1 change to PCIE 1 lane for M6S, p19/p63 | | |
| 05) Mini-PCIE change the HSIO port and remove SATA for M6S, p19/p55 | | |
| 06) LAN1_1215M change the HSIO port, p19/p46 | | |
| 07) LAN3_1225M change the HSIO port, p19/p50 | | |
| 08) PCIE1X1 change the HSIO port, p19/p36 | | |
| 09) remove ASMG061 (PCIE to 2xSATA), p67 | | |
| 10) SATA_M3 change the HSIO port, p19/p67 | | |
| 11) SATA_M2 change the HSIO port, p19/p65 | | |
| 12) SATA_M2 change the HSIO port, p19/p65 | | |
| 13) Mount XRT5 for M2_SSD02A, p64 | | |
| 14) PCIE1X1_2 change the HSIO port, the HW route from PCH side, p19/p33 | | |
| 15) M2_TYPE_M1 change the HSIO port, the HW route from CPU side, p5/p64 | | |
| 16) Combine the AMQ5002A with AMQ5003B, p53 | | |
| History 2022/7/4 | R1.10 | |
| 01) modify the OC pin HW design to avoid leakage current , p22/p60 | | |
| 02) modify the OC pin HW design to avoid leakage current , p22/p62 | | |
| 03) Unmount HRS5/HG8/HG4/HN/HQ5/HQ6, for Vcext override no use, p10 | | |
| 04) [S-IO] reserved a test point, p10 | | |
| 05) Unmount AHC_PWR_ON HW Circuits, p72 | | |
| 06) modify the net name for CLKOUT_PCIE1_perts, p17 | | |
| 07) Unmount SR1805/SR1804/SR182/SR184/SR1843, for CLKREQ# no use, p17 | | |
| 08) modify the SRTCC0 pin and combine with SIO_ATX_PSON, p61 | | |
| History 2022/7/4 | R1.10 | |
| 01) [S-IO] reserved a test point, OI110/OI112/OI113/OI110/OI115/OI111/OI114/OI117/OI103/OI105/OI106 , p12 | | |
| 02) SCL, SC11 change to SFP, for XIAI_X1 , p17 | | |
| 03) L3C2, L3C5 change to 6_HPF, for XIAI_L3X1 , p50 | | |
| 08) modify the SRTCC0 pin and combine with SIO_ATX_PSON, p61 | | |
| History 2022/7/7 | R1.10 | |
| 01) mount SR238 for SPI0_CLK 3.3V signaling mode, p20 | | |
| 01) Correct the PD resistance(SR232) net name for U2_P5_ON, p23 | | |
| History 2022/7/12 | R1.10 | |
| 01) Unmount M6S (device side), for CLKEQ# no use, p45 | | |
| History 2022/7/28 | R1.10 | |
| 01) GD4105/GD105 change to A21045-04F for HDMI DDC DATA/CLK signals ,p41/p42 | | |
| History 2021/12/15 | | |
| 01) Modify the Power CAP of PS8405A for HDMI2.0, p41/42 | | |
| 02) Add the CLK REQ pin: PCIE1X6_2/PCIE4X1_2/PCIE1X1_2/PCI Slot , p17 | | |
| 03) modify the S-IO CLKRN pin, PU 8.2Kohm(reserved OR253) via +3V , p61 | | |
| History 2021/12/16 | | |
| 01) Add US820 for laying route, p59 | | |
| 02) modify US821/US8215 for layout route, p59 | | |
| 03) modify the M.2_B-key "CLK_EQ1X2_2_XMM4W" pin, p17/p45 | | |
| 04) reserved the M.2_B-key "M2_B_DEV1P" pin, p17/p45 | | |
| 05) reserved the M.2_B-key "M2_WAN_D1S" pin, p18/p45 | | |
| 06) Add PLL circuits at PCH side, p18 | | |
| 07) mount OR372 for SIO *O_CIECX1_RST#* pin, p61 | | |
| 08) Modify the DDI-C port to choose the VGA or DP-2, via BOM options, p6 | | |
| History 2021/12/20 | | |
| 01) modify the pin of "O_CIECX1_RST#*" | | |
| mapping the BIOS posting setting between AUXFANIN1 and AUXFANOUT1, p61 | | |
| 02) modify the pin106 of S-IO to connect the +1.05V_VCCPRIM(need to use standby power) , follow T708MD, p61 | | |
| 03) [S-IO] modify the pin2 net name, p61 | | |
| 04) [F812EDU] Unmount XRT5/XRT5 for reduplicate elements, p53/p67 | | |
| 05) [AMG061] modify the page#4 BOM option type, and color, p67 | | |
| 06) [CLKOUT] modify the CLKOUT port, p17 | | |
| History 2021/12/21 | | |
| 01) Add the SIO PWR sequence circuits at page 44, p44/p61 | | |
| 02) *SRCKEKR14#* and *SRCKEQL7#* change the PU Voltage to +1.8V_A (GPP_J group) , p17 | | |
| 03) [S-IO] Connect ATXP1_IN to "pin95 of VPP_EN" to enable VDDQ_EN,p61 | | |
| History 2021/12/22 | | |
| 01) SIO) NCT6798D change to NCT6126D, p61 | | |
| 02) [S-IO] remove XDP Connector and replace by tye point, p12 | | |
| History 2021/12/27 | | |
| 01) [ASMG063] Add PCI Slot3 and remove "PCIE1X2_2", p36/p38 | | |
| 02) [NCM6126D] *O_NEW_CPU*:reserved a test point, p66 | | |
| History 2021/12/28 | | |
| 01) [F812EDU] Remove 4-COM port solution of F812EDU , p70 | | |
| 02) [PCB] ESP1_L2019 / ESP1_ALERTIN1, reserved a test point, p18 | | |
| 03) [S-IO] S10_PLAT_SEL# +VSB_ATX PU change to +3V PU, p44 | | |
| 04) [S-IO] reserved AT_ATX_SEL pin and connect to ATMDRE_DET#, it should replace auto per function,p44 | | |
| 05) [S-IO] Unmount Q2R5 for ATX_PSON, p61 | | |
| History 2021/12/29 | | |
| 01) [PCB] Unmount SR140 , p17 | | |
| 02) [PCB] reserved a test point for net *M2_B_UNLOCK* , p22 | | |
| 03) [PCB] Unmount "PR42" for _VUVDQ2_EN10, p62 | | |
| 04) [S-IO] modify DDM power sequence circuits, p61 | | |
| 05) [DMS Sequences] "#_VUQD_EN_10" connect to "#_SL2P34*", p61 | | |
| History 2022/01/03 | | |
| 01) [DMS Sequences] remove reserved circuit: H2N7002, SR1813 and 08477, p61 | | |
| 02) [DMS Sequences] Re-mount PR42, modify PR49 to 0Ohm(10Kohm change to 0Ohm), p81 | | |
| History 2022/01/04 | | |
| 01) [S-IO] set a jumper/header "ATX_AT1" to choose ATX/AT mode to reduce the VBIOS circuits, p77 | | |
| 02) [S-IO] modify the net name "*_SPR_BAT_S0D" change to "*_VU_BAT*", p61 | | |
| 04) [S-IO] modify the KTD function pinT7, follow MIX-EHDL1, p74 | | |
| 05) [S-IO] Add the note for thermal sensor placement, p68 | | |
| 06) [S-IO] modify the eSPT_CLK/eSPT_10[0:3]'s resistances to follow the eSPI 1-Load topology, p18/p61 | | |
| 07) [S-IO] Remove +3V/+3VSB_ATX/SYS_ROV LED, p61 | | |
| History 2022/01/15 | | |
| 01) [PWR Sequn.] remove MIX-EHDL1's PWR Sequence reserved circuits, p67 | | |
| 02) [WIC fun.] mount OR140, unmount OR145, due to satisfy same power piance for FPU1 logic IC, p74 | | |
| History 2022/01/16 | | |
| 01) [Front Panel.] change the Front Panel CONN. to add the LAN1/LAN2/LAN3 LED control signals, p74 | | |
| 02) [LAN LED] add the LAN1/LAN2/LAN3 LED control signals, p47, p51 | | |
| 03) [VGA HD] modify net "L_DV2VA_HPD" and set BOM option for VGA port-A or port-C, p22, p32 | | |
| History 2022/01/25 | | |
| 01) [HDMI2.0] modify the passive MOS of HDMI DDC CLK/DATA: UM6K33N change to UM6K1IN, p41/p42 | | |
| 02) [+1.2V] 2x18 Power bead(0603) change to ODM(0603), p41/p42 | | |
| 03) [HDMI2.0] reserved the ODM for CEC_EN pin of PS8409A, p41/p42 | | |
| 04) [HDMI2.0] BSV pin modify to "NC" for PS8409A, p41/p42 | | |
| 05) [PCIE1X1_1] change the PCIE1X1 slot to IV part, p31 | | |
| History 2022/01/26 | | |
| 01) [S-IO] modify the HV monitor SID-pin98, +5VSB_ATX replace to +3V, p61 | | |
| History 2022/02/15 | | |
| 01) [De-bounce] modify the de-bounce circuits for RST button: mount FP818/08145; unmount FP01/FR100, p74 | | |
| 02) [S-IO] modify the AT_ATX_SEL circuits to reduce the jumper/header, p44 | | |
| 03) [S-IO] unmount the eSPT_GLK PD resistance:Q2R39(470ohm), p61 | | |
| 04) [S-IO] pin89 of VTT pin, remove the MOSFET, p61 | | |
| History 2022/02/16 | | |
| 01) [+1.2V] modify the 1.2V(FU21) EN pin: change the +5V_HDMI1 to +12V for PG60A's gate pin, p88 | | |
| 02) [SIO] reserved the SMIH pin to PCH side, p21/p61 | | |
| History 2022/02/21 | | |
| 01) [Audio] Add Audio AAFF and AMP circuits, p53 | | |
| History 2022/02/22 | | |
| 01) [PWR] PWR RD remove the unmount CAP/Resistance, p84/p85 | | |
| 02) [PWR] PWR RD remove the header: VRM_RESET_SW1, p83 | | |
| History 2022/02/24 | | |
| 01) [ESD] ESD swap for layout request: UDB316/UDB317/ULB323/ULB323/ULB324/ULB3401, p58 | | |
| 02) [VGA] Unmount GR420/GR421/GR422, GR407/GR408/GR419 change to 750hm, for vendor recommend, p54 | | |
| 03) remove SR1813/SR13, use, p12/p23 | | |
| History 2022/03/01 | | |
| 01) [PANEL] change the S-IO_PANEL_CONN., use the header for external LAN LED, p74 | | |
| History 2022/03/02 | | |
| 01) [Swap] CBA_FAN1/FAN2 modify the S-IO_FAN port mapping: CHA_FAN1-SIO_SFANP; CHA_FAN2-SIO_SFANR, p41/p68 | | |
| 02) [S-IO] change to 0603, p61 | | |
| 03) [S-IO] screw hole "H3" change to AGND, p61 | | |
| 04) [S-IO] Net "#VRL1_VCPW" connect to PR69 pin1, and change net name to "#_VRL1_L-12V_ST", p82 | | |
| 05) [PWR] Net "#VRL2_VCPW" connect to PR69 pin1, and change net name to "#_VRL2_L-12V_ST", p82 | | |
| History 2022/03/08 | | |
| 01) [Swap] Swap the connector between SATAG6_6 and SATAG6_7, p67 | | |
| 02) [Swap] Swap the ESD component for layout request: GD105/UD2024/UDB5510/ULB314, p42/p56/p59 | | |
| 03) [Swap] Swap the ESD component for layout request: GD105/UDB465/UDB315/ULB320, p39/p40/p59 | | |
| History 2022/03/10 | | |
| 01) [VQDQ] Update VQD Power solution, p81 | | |
| 02) [PWR] Update VCORE/VCCGT Power solution for entry level, p83/p84/p85 | | |
| History 2022/03/14 | | |
| 01) [PCIE Gen4 Swap] Swap between M.2 2280 SSD #02, and PCIE4X Slot #01 for other length, p19 | | |
| 02) [+1.2V] Unmount PR8101, PR8102 for power RD request, p81 | | |
| History 2022/03/16 | | |
| 01) [Log] Add "M4" for rev1.00, p77 | | |
| History 2022/03/17 | | |
| 01) [BOM] LGA1700: 12001-00300300 change to 12001-00300400 | | |
| 02) [BOM] TPN: 06120-00080400 change to 06120-00140000 | | |
| 03) [BOM] P04: 06007-00980000 change to 06007-00980100 | | |
| History 2022/03/29 | | |
| 01) [BOM] PR28/PR29/PR31/PR32:2-Load topology, 33ohm change to 75ohm(for 3.3V), p29 | | |

