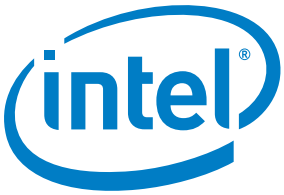

Apollo Lake Platform — Juniper Hill Customer Reference Board (CRB)

User Guide

July 2019

Revision 1.7

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Document Number: 566724-1.7

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Revision History

Date	Revision	Description
July 2019	1.7	- Updated Chapter 6 - Rework to Enable SPI dTPM
April 2019	1.6	- Updated Chapter 6 - Optional Rework
June 2016	1.5	- Added note on HDMI dongle support - Added HDMI cable in the boot kit list - Added note to mention use the supplied HDMI cable - Added Chapter 6 Optional Rework - Updated Table 11 to add in J6C1 - Indicated an alternate SPI part in section 3.2
March 2016	1.0	Initial release.

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1.0 Introduction

This user guide describes the typical hardware setup procedures, features and use of the Apollo Lake Juniper Hill Customer Reference Board (CRB) platform. The CRB is a dual channel DDR3L ECC SODIMM platform.

Note: In this document, the term CRB is synonymous with Apollo Lake Juniper Hill CRB.

Note: It is important to read this document in its entirety before powering on the board.

The Quick Start section provides quick-start procedures. It is recommended that you have both the schematic and CRB present when using this document.

Note: The references in this document correlate to the reference designators and board properties of the Apollo Lake Juniper Hill CRB.

Note: All diagrams displayed in this document are for illustration purposes only. The board you received may look different from the one shown in this document.

Note: MIPI CSI camera AIC is supported in the DSS and transportation solutions segments only.

1.1 Terminology

The following terms are used in this document.

Table 1. Terminology

Term	Definition
AIC	Add-In Card
BSP	Board Support Package
CMOS	Complementary Metal-Oxide Semiconductor (transistor type)
CRB	Customer Reference Board
DSS	Digital Security Surveillance
ECC	Error Correcting Code
eDP	Embedded DisplayPort*
eMMC*	Embedded MultiMediaCard
GPIO	General Purpose Input Output

Term	Definition
HD	High Definition
HDMI*	High-Definition Multimedia Interface
HSUART	High-Speed Universal Asynchronous Receiver/Transmitter
I2C*	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
IPU	Image Processing Unit
IOTG	Intel Internet of Things Group
JTAG	Joint Test Action Group (developer of IEEE Standard 1149.1-1990)
LED	Light Emitting Diode
LPC	Low Pin Count
Mini-ITX	Mini Information Technology eXtended
MIPI* CSI	MIPI* Camera Interface Specification
MSDK	Media Software Development Kit
PCB	Printed Circuit Board
PCIe*	Peripheral Component Interconnect Express
PMIC	Power Management Integrated Circuit
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SATA HDD	SATA Hard Disk Drive
SDIO	Secure Digital Input Output
SMBus	System Management Bus
SoC	System on Chip
SODIMM	Small Outline Dual In-line Memory Module
SPI	Serial Peripheral Interface
SSD	Solid State Drive
SVID	Serial Voltage Identification

Term	Definition
TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
dTPM	Discrete Trusted Platform Module
SPI	Serial Peripheral Interface
IRQ	Interrupt Request
PTT	Platform Trust Technology
CSE	Converged Security Engine
XML	eXtensible Markup Language
FIT	Intel® Flash Image Tool

1.2 Reference Documents/Links

The following table lists the associated reference documents.

Table 2. Reference Documents

Document	Document No./Location
IOTG Apollo Lake Platform Juniper Hill CRB (DDR3L-ECC) - Board File	*562547*
IOTG Apollo Lake Platform Juniper Hill CRB (DDR3L-ECC) - Schematics	*562548*
Best Known Configuration BKC of Windows OS for IOTG Apollo Lake	*564423*
North Star Sensor AIC Kit - Schematics	*559570*
North Star Sensor AIC Kit - Board File	*559571*
North Star Sensor AIC Kit - User Guide	*559483*

To report board issues, go to http://goto/CRMprod

1.3 Board and Boot Kit Package List

The Board and Boot Kit Package contains the following:

- Juniper Hill CRB
- Boot kits

The following table provides details on the contents of the package list.

Table 3. CRB, Boot Kit: Package List

BIL	Intel PN/Model #	Description	Qty	Photo
1	H72225-2xx	Juniper Hill CRB	1	
2	H97855-001/ KVR16LSE11/4	4G DDR3L ECC SODIMM	1	
3	FSP084-DIBAN2/ H98082-001 WS-001+002/ H36593-001	Power adapter and power cord	1	
4	G51041-001/ 4808K-ND	Board standoff	4	
5	726260-001/ 4C25PPMZB	Board standoff screw	4	
6	GL39-00121A	HDMI cable	1	

1.4 Feature Set

The following table describes the CRB features.

Table 4. CRB Feature List

Feature	Description
Form Factor	Mini-ITX
PCB Stackup	6 layers, Type-3 board
SoC Mounting Type	Soldered down
Supported SoC	Apollo Lake-I

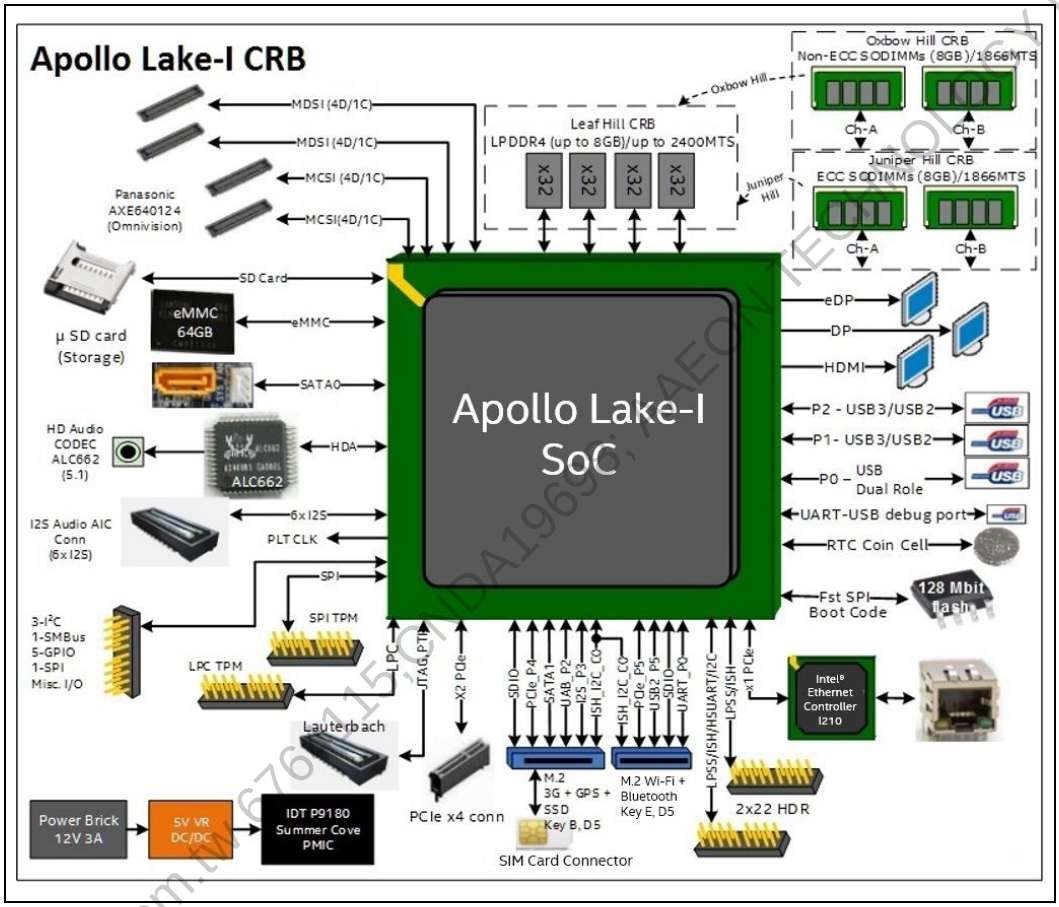
Feature	Description
Power Delivery	IDT* P9180 PMIC
Memory	Supports 2x DDR3L ECC SODIMMs up to a total of 8 GB, 1867 MT/s
Display[1]	1x HDMI*, 1x DisplayPort* and 1x eDP
USB 2.0/3.0	2x USB 3.0/2.0 ports, 1x USB 3.0/2.0 dual role connector, 3x USB 2.0 front-panel header
SATA	1x SATA with cable connect; 1x SATA using an M.2 Key B card
Ethernet	On-board Intel® Ethernet Controller I210 port (RJ45) - x1 PCIe*
SDIO	MicroSD* card slot
eMMC*	On-board 64 GB eMMC device
Audio	Intel® High Definition Audio (Intel® HD Audio) 5.1 audio codec
MIPI* CSI	Camera support through AIC (supported in the DSS and transportation solutions segments only)
PCIe*	x4 open-end PCIe card slot with x2 PCIe lanes; PCIe x1 lane (muxed on USB 3.0 lanes) connected to an M.2 connector
Fast SPI	SPI flash device with in-circuit programming capability
I2C*	8x I2C
LPC	LPC signals connected to a 20-pin header
Debug	JTAG on Lauterbach*, POST codes on LPC TPM, console UART USB interface
I2S	6x I2S can be supported through AIC
External Power Supply	A 90W DC brick can be used with input voltage of 12V

Note: 1. DP++ mode (DP to HDMI dongle) is supported on Juniper Hill Fab B. CRBs earlier than this version will not support DP++ mode.

1.5 Block Diagram

The following figure shows the CRB block diagram.

Figure 1. CRB Block Diagram



1.6 Add-In Cards/Peripherals

The AICs/peripherals in this table are not supplied in the boot kit. You can order the parts through the reference links.

Table 5. AIC/Peripheral

AIC/Peripheral	Description	Reference Link
Mondello* ADV748X Evaluation Kit	Integrated video decoder	http://datasheet.octopart.com/EVAL-ADV748XEBZ-Analog-Devices-datasheet-27841383.pdf
PCIe* Wi-Fi* and USB Bluetooth® (M.2 Module)	M.2 Wi-Fi/Bluetooth module	http://www.amazon.com/s/ref=nb_sb_noss?url=search-alias%3Daps&field-keywords=AW-CE123H+
Samsung* SM951 AHCI 128GB QS	PCIe SSD module	http://www.newegg.com/Product/ProductList.aspx?Submit=ENE&DEPA=0&Order=BESTMATCH&Description=Samsung+SM951&N=-1&isNodeId=15
Samsung* SM951 AHCI 512GB QS assembly	PCIe SSD module	http://www.harddrivesplus.com/product/2185699/
Samsung SM951 NVMe 128GB QS	PCIe SSD module	http://www.newegg.com/Product/ProductList.aspx?Submit=ENE&DEPA=0&Order=BESTMATCH&Description=Samsung+SM951&N=-1&isNodeId=1
Samsung* SM951 NVMe 512GB QS	PCIe SSD module	http://www.harddrivesplus.com/product/2185699/
Micro SATA Cables PLP4F-P4F-10IN	SATA cable	TBD
Digi-Key* SATA + power cable AE10084-ND	SATA + power cable	http://www.digikey.com/product-detail/en/assmann-wsw-components/AK-SATA-SP-050/AE10084-ND/951594

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2.0 Reference Layout

This section describes the CRB layout.

2.1 CRB Layout

Figure 2 shows the CRB top layer view (without the heat sink). Table 6 describes the CRB top layer components.

Figure 2. CRB Top Layer View

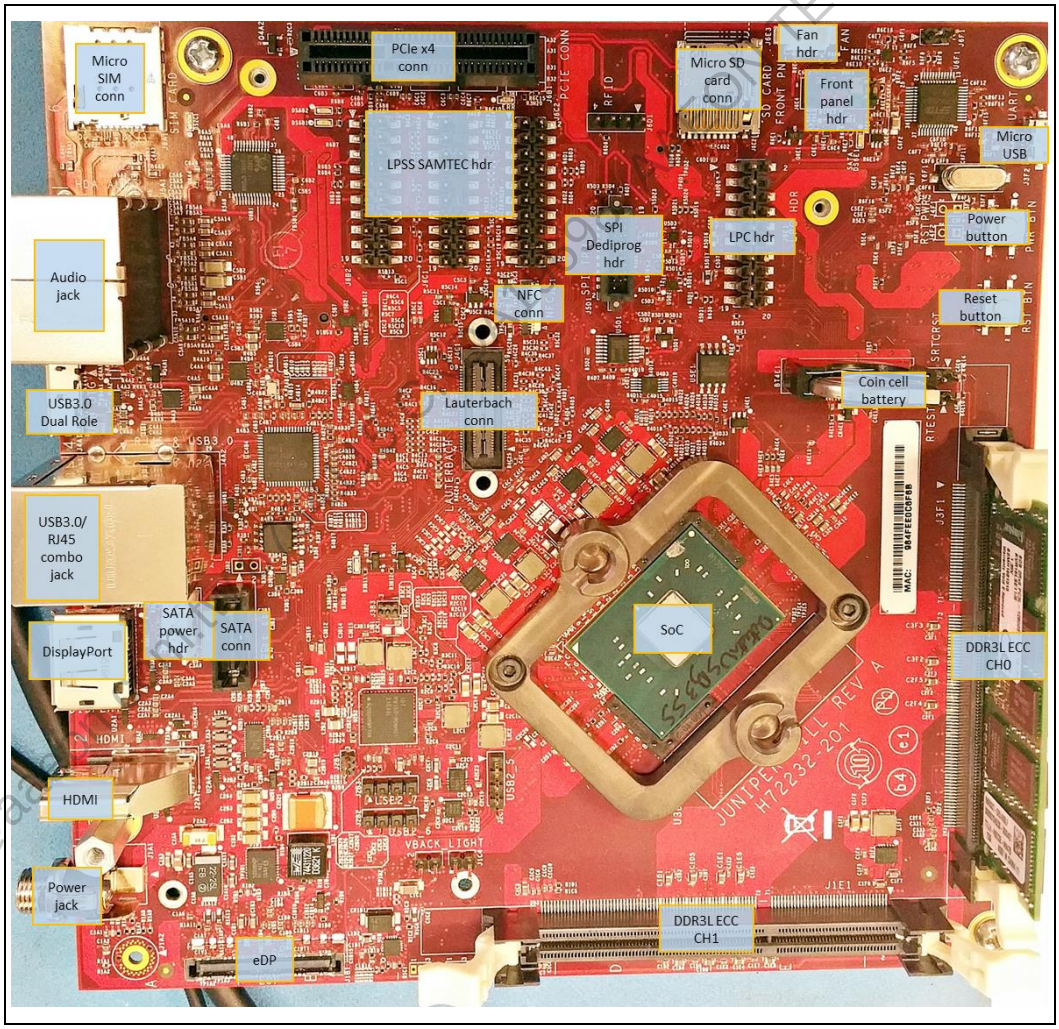

Table 6. Legend — CRB Top Layer View

Part/Component	Location/Jumper
Power jack	J1A1
DisplayPort*	J2A2
eDP	J1B1
HDMI*	J2A1
USB 3.0/RJ45 combo jack	J4A2
USB 3.0 dual role connector	J4A1
Intel® HD Audio 5.1 audio jack	J5A1
PCIe* x4 connector	J6B1
LPC header	J6E1
JTAG (Lauterbach*) connector	J4C1
Reset button	S5F1
Power button	S5F2
Front-panel header	J6E4
Micro USB port	J6F2
DDR3L ECC SODIMM-CH 1	J1E1
DDR3L ECC SODIMM-CH 0	J3F1
Apollo Lake-I SoC	U3D1
Fan header	J6E3
LPSS SAMTEC* headers (I2C*/UART/PWM/GPIO)	J6C2/J6B2/J6C1
Micro SIM connector	J6A1
SATA power connector	J3A1
SATA connector	J3B1
SPI Dediprog* header	J5D1
Coin cell battery	BT4E1
MicroSD* card connector	J6E2
S0 LED	DS2C1
S5 LED	DS6B1

Part/Component	Location/Jumper
PWROK LED	DS6B2
NFC connector	J5C1

Figure 3 shows the CRB bottom layer view. Table 7 describes the CRB bottom layer components.

Figure 3. CRB Bottom Layer View

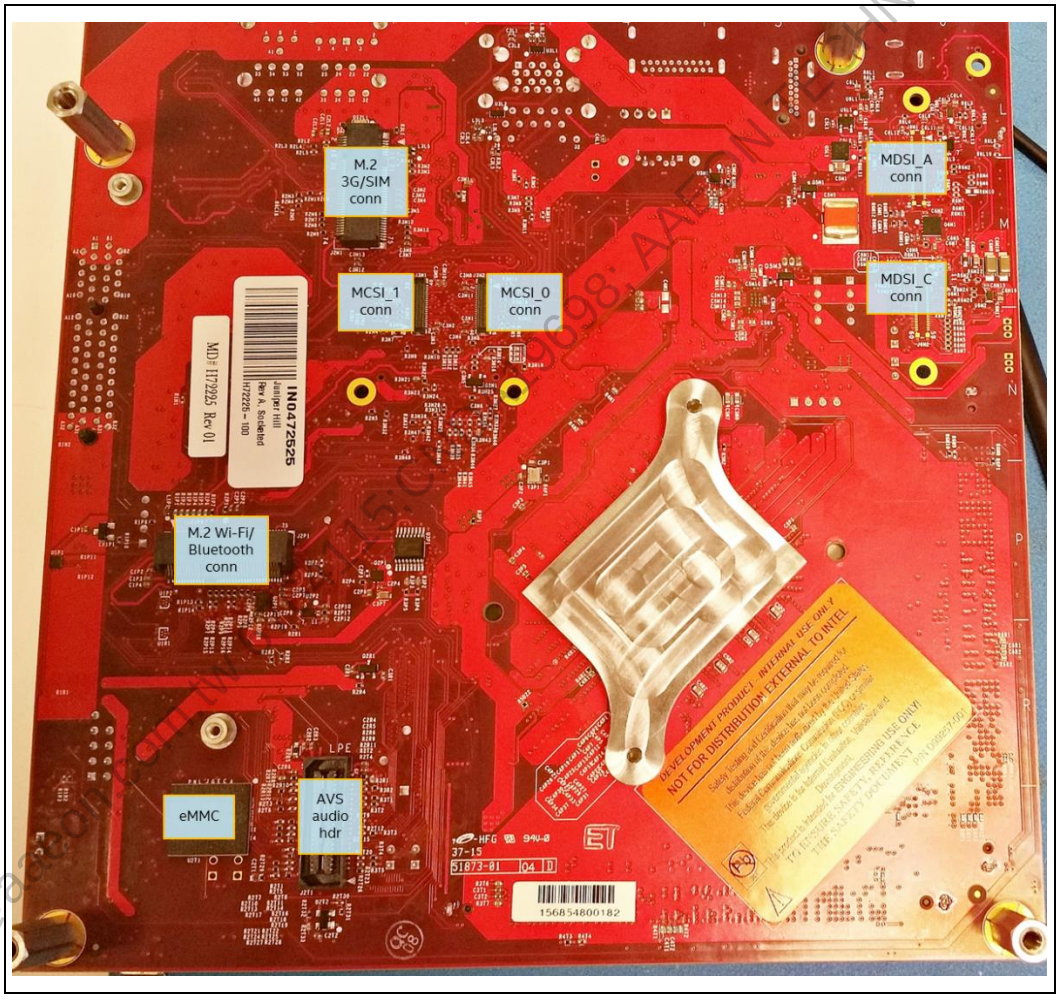

Table 7. Legend — CRB Bottom Layer View

Part/Component	Location/Jumper
Camera AIC connector (MCSI connector) (supported in the DSS and transportation solutions segments only)	J3M1, J3M2

Part/Component	Location/Jumper
M.2 3G/SIM/SATA connector	J2M1
M.2 Wi-Fi*/Bluetooth® connector	J2P1
MDSI connector	J6M1, J6M2
eMMC*	U2T1
AVS audio header	J2T1

2.2 CRB Back Panel Layout

Figure 4 shows the CRB back panel layout. Table 8 describes the CRB back panel components.

Figure 4. CRB Back Panel Layout

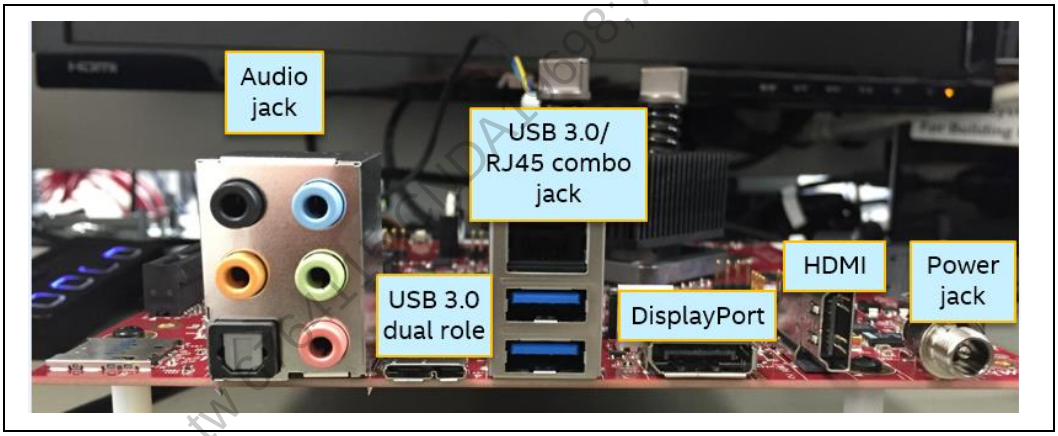

Table 8. Legend — CRB Back Panel Layout

Part/Component	Location/Jumper
USB 3.0/RJ45 combo jack	J4A2
HDMI*	J2A1
DisplayPort*	J2A2
Power jack	J1A1
USB 3.0 dual role connector	J4A1
Intel® HD Audio 5.1 audio jack	J5A1

2.3 Platform LEDs

Table 9 lists the platform LEDs.

Table 9. List of Platform LEDs

REF DES	Purpose
DS6B1	S5 indicator
DS2C1	S0 indicator
DS6B2	PWROK indicator
D5L1	S0ix indicator

2.4 Buttons

Table 10 lists the buttons.

Table 10. List of Buttons

REF DES	Purpose
S5F2	Power
S5F1	Reset

2.5 Jumper Settings

Table 11 lists the jumpers and default settings.

Table 11. List of Jumpers and Default Settings

REF DES	Function	Default Setting	Remark
J6B2	Enable SPI Boot	5-7	For SPI boot: place the jumper on pin 5-7 to disable eMMC* as the boot device.
J6C1	Enable SPI boot	10-12	Place the jumper on pin 10-12 to enable SPI boot. (Refer section 6.2 for the preferred way to strap GPIO_111 to low through a pull down resistor).
J4E2	Clear CMOS	1-x (normal operation)	Set to 1-2 to clear CMOS.

REF DES	Function	Default Setting	Remark
J4E1	RTC test	1-x (normal operation)	Set to 1-2 to emulate low RTC battery voltage.

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3.0 Quick Start

This chapter provides the quick-start steps.

3.1 Boot Ingredients

The boot ingredients are as follows:

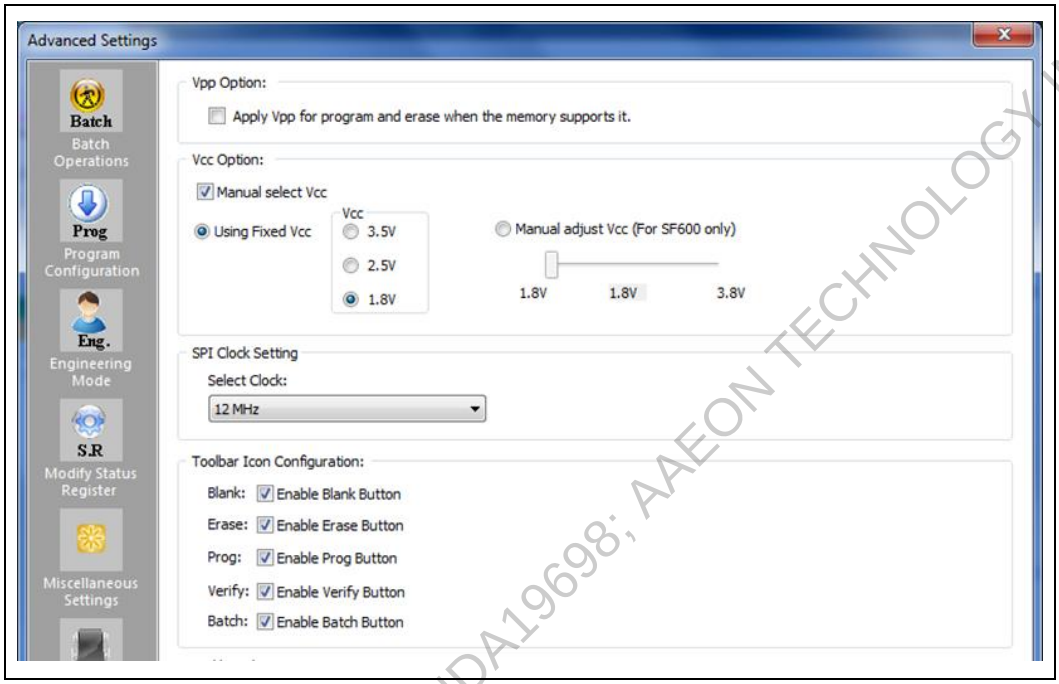
- DDR3L ECC SODIMM (part of the boot kit).
- Power adapter (AC brick, part of the boot kit).
- Keyboard and mouse (USB based, not supplied by Intel).
- SATA hard drive (not supplied by Intel), cable (not supplied by Intel).
- BIOS image (pre-programmed on the SPI NOR chip).
- Dediprog* SF600 with adapter to flash images (not supplied by Intel).
- External display (i.e., HDMI*/DisplayPort*/eDP, not supplied by Intel), HDMI cable (part of the boot kit).

3.2 Programming BIOS SPI

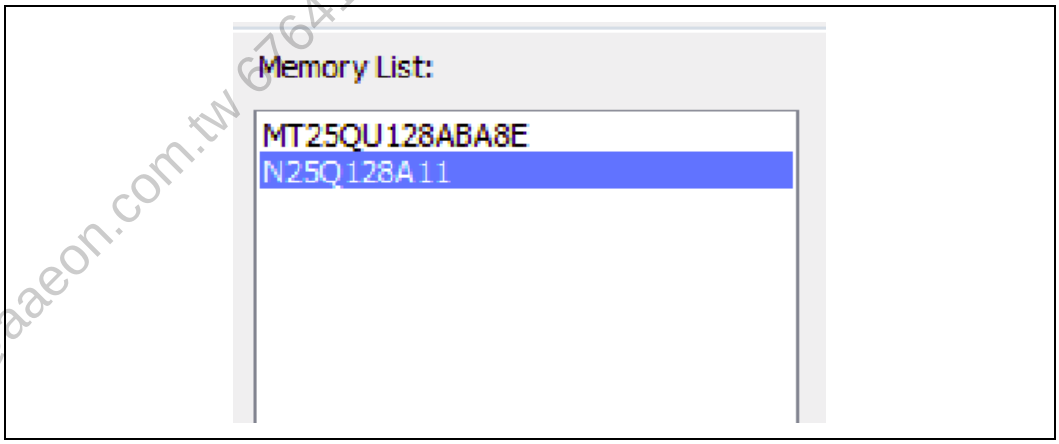
The Dediprog SF600 programmer can be used to program the SPI flash device.

1. Install the latest Dediprog software from the Dediprog website (http://www.dediprog.com) onto your host system.
2. Connect the USB cable of the Dediprog programmer to the system on which you have installed the software.
3. Connect the FRC cable to the SPI Dediprog header on the CRB at J5D1.

4. Set the Vcc option to 1.8V prior to auto detect. This makes the programmer's pin header output 1.8V.



5. When prompted for the SPI part selection, choose **N25Q128A11**.



Note: Alternate SPI part (W25Q128FW) may be used in different batch of CRB.

6. Remove all power supply to the board.
7. Flash the .bin image that corresponds to SPI-0 and verify the image.
8. Manually close the Dediprog software. The settings are saved.
9. Remove the Dediprog connector.

Note: No jumper setting is required for SPI programming.

3.3 Powering Up the CRB

1. Plug in DDR3L ECC SODIMM (supplied in the boot kit) to the CH0 SODIMM connector (J3F1).
2. Connect the DisplayPort, HDMI or eDP panel for output display. HDMI (J2A1) is enabled on DDI0, DisplayPort (J2A2) is enabled on DDI1, and eDP (J1B1) is enabled on eDP lanes.

Note: Connect the external graphics option to the PCIe x4 connector (J6B1) in case external graphics is desired.

Note: Use the HDMI cable supplied by Intel in case HDMI display is being used.

3. Connect the SATA HDD with OS installed to SATA connector J3B1 and SATA power connector J3A1 through the SATA cable.
4. Connect the USB mouse and keyboard to J4A2.
5. Connect the power adapter (AC brick) to power jack J1A1.
6. Press the power button at S5F2.
7. Observe the S0 status LED (DS2C1), S5 status LED (DS6B1), and PWROK LED (DS6B2). Verify that these LEDs light up in green.
8. As the system boots, press **F2** to enter the BIOS setup screen.
9. Check the time, date, and configuration settings. The default settings should be sufficient for most users.
10. Exit the BIOS setup.

The system boots up and is ready for use.

3.4 Powering Down the CRB

1. Shut down the OS.
2. Turn off and remove the AC brick power adapter.

Note: Intel does not recommend powering down the board by simply shutting off power at the AC brick power adapter, unplugging the power adapter from the CRB's power jack, or holding down the power button.

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4.0 Yocto Project* BSP

For further information, refer to the Intel Atom® Processor E900 series, Intel® Celeron® Processor N3350, Intel® Pentium® Processor N4200, Intel® Celeron® Processor J3355 and J3455 Board Support Package for Yocto* Project (Linux* Kernel 4.14.67) MR4 Release Notes (Document #595926 on RDC).

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5.0 Interface Implementation

This section provides information about the interface implementation.

5.1 Interface Port Mapping

The following tables provide detailed port mapping information.

Table 12. Port Mapping 1

Target Device	Interface	CRB Port Mapping	Remark
Memory	DDR3L ECC - CH 0 DDR3L ECC - CH 1	2-ECC SODIMM Inline Vertical connectors	
Display	DDI0 DDI1 eDP MDSI_A MDSI_C	DDI0 - HDMI* (Active Level Shifter) DDI1 - DisplayPort* eDP - eDP MDSI_A – MIPI* DSI MDSI_C - MIPI DSI	
Camera	MIPI_CSI(D-PHY 1.1) MIPI_CSI2(D-PHY 1.2) Camera_GPIO	Add-in card connector	Connect to camera AIC (supported in the DSS and transportation solutions segments only)
Debug	UART - uUSB COM Port	UART2	
Debug	Primary JTAG	60-pin Lauterbach* header supported	
Storage	eMMC*	eMMC	On-board eMMC
Storage	SDIO	M.2 Wi-Fi*/ Bluetooth®	
Storage	SD card	MicroSD* Card	
Storage	SATA - Port0 SATA - Port1	Port0 - Cable Connect Port1 - M.2	
Fast SPI	Fast SPI CS#0	Fast SPI CS#0 - Boot device (flash)	

Table 13. Port Mapping 2

Target Device	Interface	CRB Port Mapping	Remark
PCIe*	PCIe Lane0	P0 - x4 slot (Default - x2 lane support only)	Lane 0 and Lane 1 are connected to the same single x4 slot.
	PCIe Lane1	P1 - x4 slot (Default - x2 lane support only)	
	PCIe Lane2	P2 - LAN	
	PCIe Lane4	P4 - M.2 3G	
	PCIe Lane5	P5 - M.2 Wi-Fi*/ Bluetooth®	
Audio	I2S1	I2S0 - M.2 3G/SIM	Default
	I2S2	I2S2 - AVS header	
	I2S3	I2S2 - M.2 Wi-Fi/ Bluetooth	Default
	I2S4	I2S4 - AVS header	
	I2S5 - Muxed with ISH_GPIO	I2S5 - ISH_GPIO	Default
	I2S6 - Muxed with ISH_GPIO and Intel® HD Audio	I2S6 - Intel® HD Audio	Default
USB Interface	USB3.0-Port0	USB3.0 P0 - Dual role	
	USB3.0-Port1	USB3.0 P1 - Back panel	J4A2
	USB3.0-Port4	USB3.0 P4 - Back panel	J4A2
	USB2.0-Port0	USB2.0 P0 - Dual role	
	USB2.0-Port1	USB2.0 P1 - Back panel	J4A2
	USB2.0-Port2	USB2.0 P2 - M.2 Key B	
	USB2.0-Port3	USB2.0 P3 - M.2 Key E	
	USB2.0-Port4	USB2.0 P4 - Back panel	J4A2
	USB2.0-Port5	USB2.0 P5 - USB header	
	USB2.0-Port6	USB2.0 P6 - USB header	
	USB2.0-Port7	USB2.0 P7 - USB header	
LPC Interface	LPC	LPC add-in card	Optional to connect to external LPC card for Port 80 display
LPSS UART Interface	UART0	Micro USB port	Use as debug port through micro USB
	UART1	LPSS header	External probing/implementation
	UART2	M.2 Bluetooth/Wi-Fi	

Table 14. Port Mapping 3

Target Device	Interface	CRB Port Mapping	Remark
SVID	SVID	PMIC	
I2C*	I2C0	I2C0 - Camera AIC	MIPI CSI 1
	I2C1	I2C1 - NFC	
	I2C2	I2C2 - Camera AIC	MIPI CSI 1
	I2C3	I2C3 - AVS	Audio AIC
	I2C4	I2C4 - Camera AIC	MIPI CSI 2
	I2C5	I2C5 - LPSS header (1.8V) - I210, LPSS header (3.3V)	With 3.3V level shifter
	I2C6	I2C6 - LPSS header (1.8V) - M.2 Wi-Fi*/Bluetooth®, LPSS header (3.3V)	With 3.3V level shifter
	I2C7	I2C7 - Camera AIC (1.8V) - M.2 3G/SIM (3.3V)	With 3.3V level shifter
LPSS SPI	SIO_SPI0 SIO_SPI1 SIO_SPI2	LPSS header	External probing/implementation
PWM	PWM0 PWM1 PWM2 PWM3	LPSS header	External probing/implementation

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6.0 Optional Rework

This section provides information and instructions about optional rework.

6.1 Rework to enable HD audio

This section shows the rework required to enable the HD audio.

6.1.1 Applicability

Applicable to all fab.

6.1.2 Required Components

The following components are required.

Table 15. Rework for HD audio Enablement: Component required

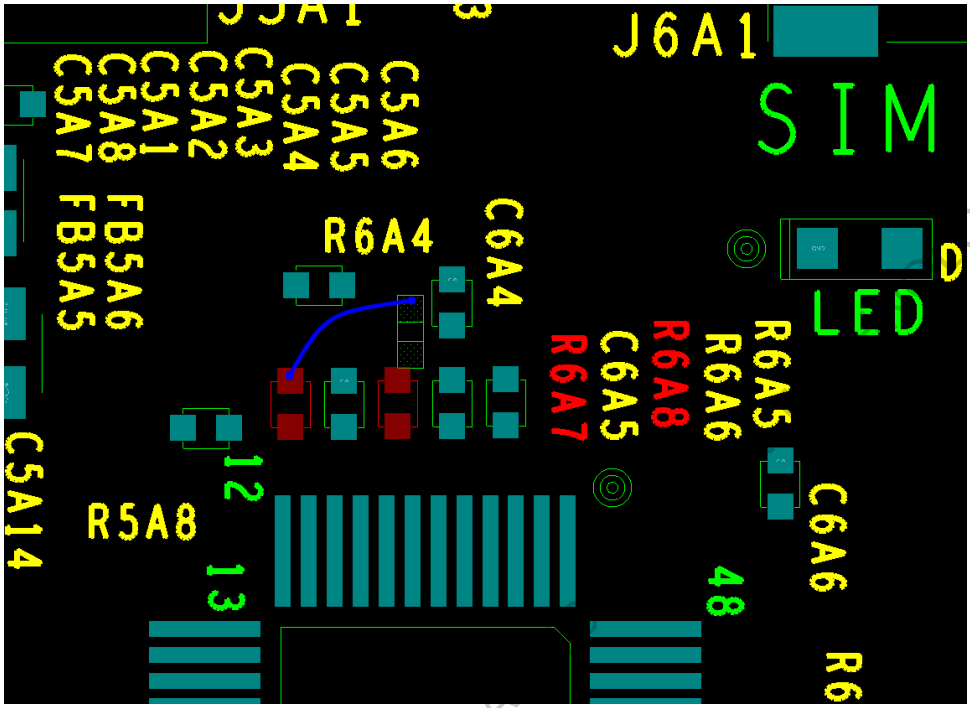
Quantity	Description
2	0 ohms 0402
1	249 ohms 0402
1	1kohms 0402

6.1.3 Rework Steps

Complete the following steps to successfully accomplish this rework.

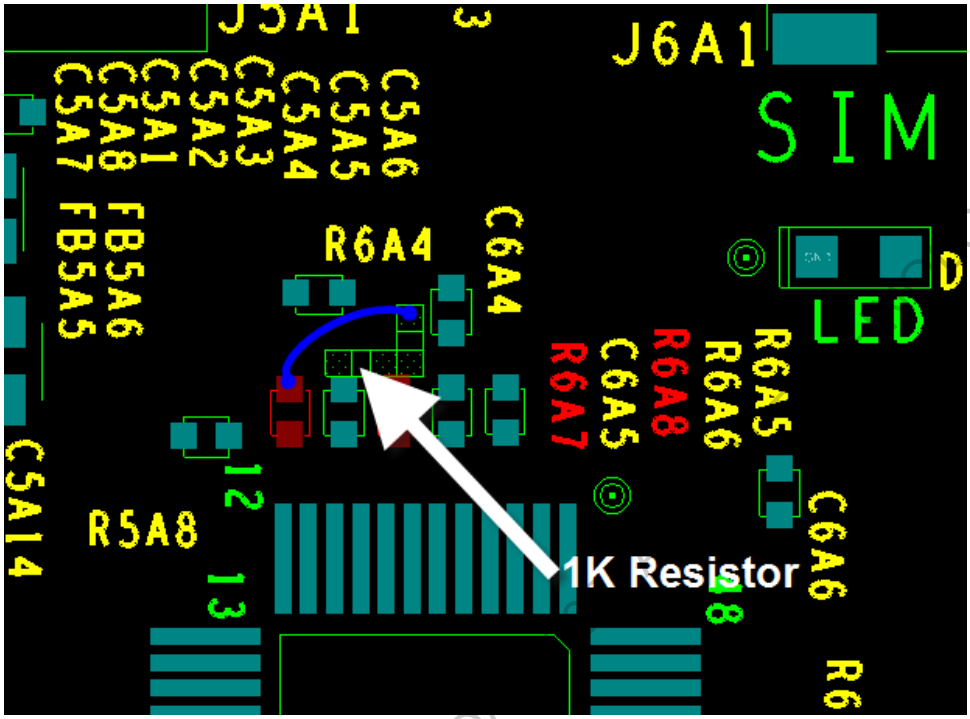
1. Replace R6A7 with a 0402, 0Ω resistor.
2. Replace R6A8 with a 0402, 0Ω resistor
3. Add a 0402, 249Ω resistor to R6A8 pin 2 as shown in Figure 5 below.
4. Add a jumper wire from 249Ω pin 2 to R6A7 pin 1 as shown in Figure 5 below.

Figure 5. Rework to enable HD audio



5. Add a 0402, 1KΩ resistor between R6A8 pin 2 and C6A5 pin 2 (GND) as shown below.

Figure 6. Rework to enable HD audio



6.2 Rework to enable SPI boot

This section shows the rework required to enable SPI boot. For SPI boot design, GPIO_111 (SoC pin F58) needs to be pull low externally with resistor range 3.3kohms to 4.7kohms.

6.2.1 Applicability

Applicable to all fab.

6.2.2 Required Components

The following components are required.

Table 16. Rework for SPI boot Enablement: Component required

Quantity	Description
1	Resistor range from 3.3kohms to 4.7komhs, 0402

6.2.3 Rework Steps

Complete the following steps to successfully accomplish this rework.

1. Stuff R6C11.
2. Un-stuff R6C13.

6.3 Rework to enable/disable power button push to wake from G3 to S0

This section shows the rework required to enable/disable power button push to wake from G3 to S0. For board designed with IDT PMIC P9180, PMIC_EN on P9180 can be used to configure power button usage to wake from G3 to S0.

6.3.1 Applicability

Applicable to all fab.

6.3.2 Required Components

The following components are required.

Table 17. Rework for SPI boot Enablement: Component required

Quantity	Description
1	10kohms, 0402

6.3.3 Rework Steps

Complete the following steps to successfully accomplish this rework.

Table 18. Rework options for power button usage

Signal	Strap	Rework	Comment (Behavior)
PMIC_EN	PU (10KΩ to V5_A)	stuff R2B26/no stuff R2B27	No power button push required for G3 to S0
PMIC_EN	PD (10KΩ to GND)	stuff R2B27/no stuff R2B26 (IOTG CRB default)	Power button push required for G3 to S0

6.4 Optional Rework

This section provides information and instruction about optional rework.

6.4.1 Rework to Remove I2C5, I2C6, and I2C7 Pull-up Resistors

This section shows the rework required to remove the I2C5, I2C6, and I2C7 pull-up resistors.

6.4.1.1 Description

When adding an add-in-card (ISH add-in-card) to the system, it may be possible to have double pull-up resistors on the I2C5, I2C6, and I2C7 interfaces.

6.4.1.2 Impact of Not Implementing the Rework

In some cases, the add-in-card would fail to be detected by the system.

6.4.2 Applicability

This rework is applicable to Fab C.

Note: No rework is needed for earlier CRB versions.

6.4.3 Required Components

None.

6.4.4 Rework Steps

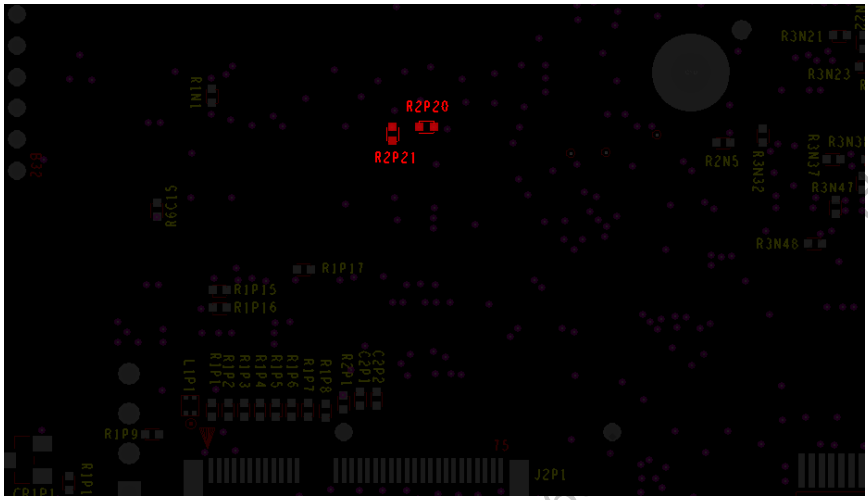
Complete the following steps to successfully accomplish this rework.

Note: Rework instruction should only be applied if the add-in-card includes PU resistors on the I2C interface signals. The card is not reliably detected.

6.4.4.1 I2C5 Rework Instruction (Routed to the J6C2 Header)

Remove R2P20 and R2P21 from the platform as shown in figure Figure 7.

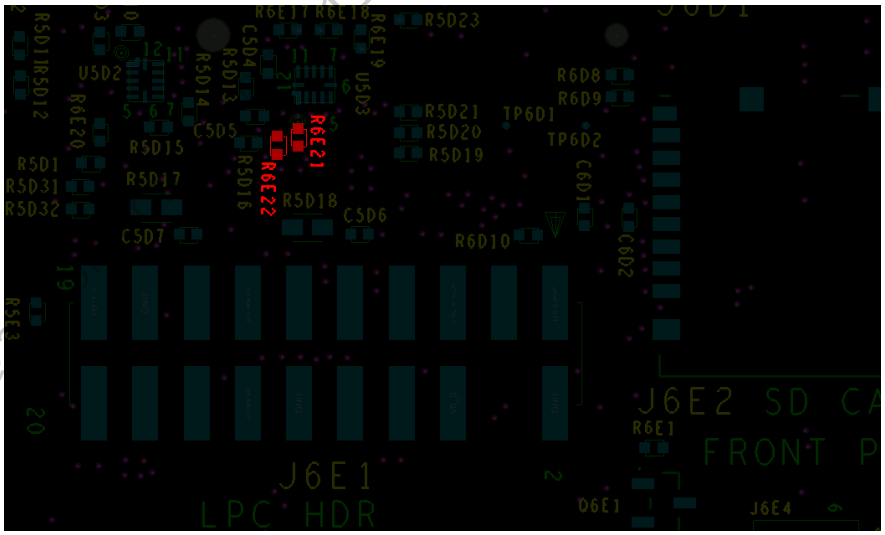
Figure 7. Bottom Layer



6.4.4.2 I2C6 Rework Instruction (Routed to the J6C2 Header)

Remove R6E21 and R6E22 from the platform as shown in Figure 8.

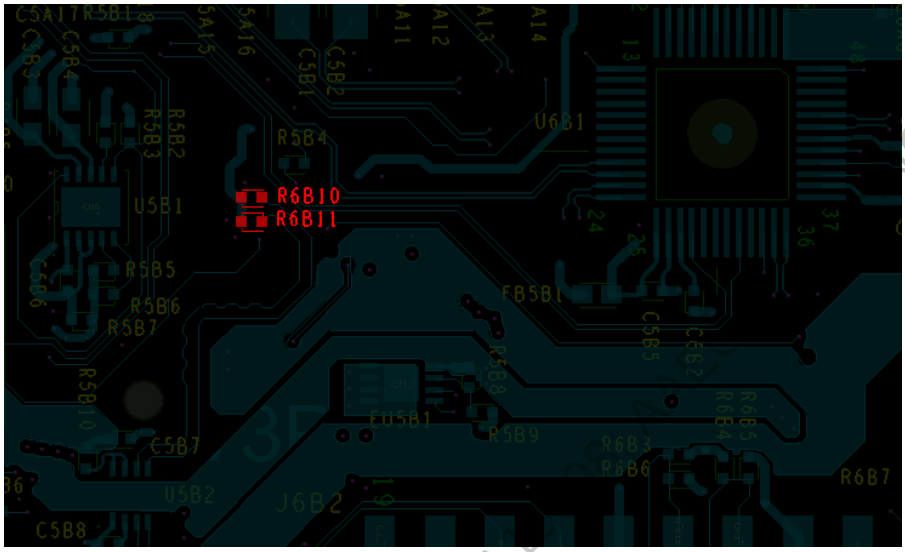
Figure 8. Top Layer



6.4.4.3 I2C7 Rework Instruction (Routed to the J2M1 Connector, M.2, B-Keyed)

Remove R6B11 and R6B10 from the platform as shown in Figure 9.

Figure 9. Top Layer



6.5 Optional S0ix and S3 Rework

6.5.1 Impact of Not Implementing the Rework

The S0ix and S3 functions will not work.

6.5.2 Description

Rework for S0ix and S3 functionality.

6.5.3 Applicability

Applies to the following versions; Juniper Hill Fabs A and B versions.

6.5.4 Required Components

The following components are required.

Table 19. Optional S0ix and S3 Rework: Components Required

Quantity	Description
1	PMIC (IDT P91E0-I5NHGI, Revision H)
1	Resistor (30.1kOhm 1% tolerance, 0402 package)
1	Capacitor (0.22uF 10% tolerance, 0402 package, X7R)
1	Schottky Diode (BAT54A, SOT23 package)

NOTE:

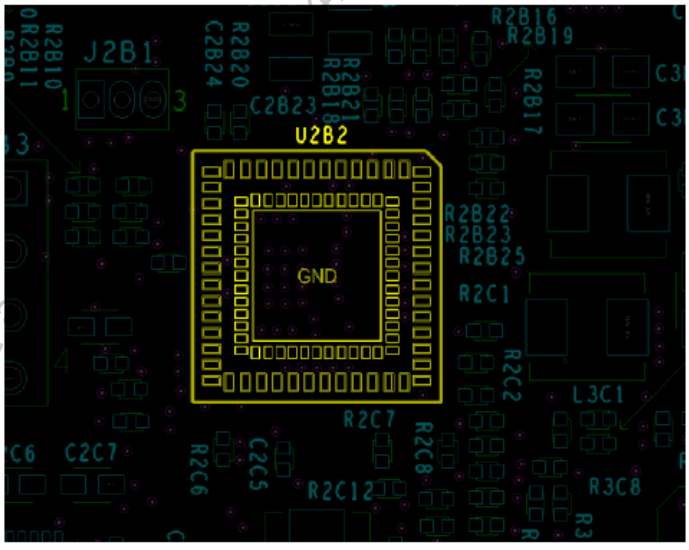
1. The installation for version H of the PMIC is required in the platform.

6.5.5 Rework Steps

Complete the following steps to accomplish this rework.

1. Replace the U2B2 with the PMIC version H (as shown in Figure 10.

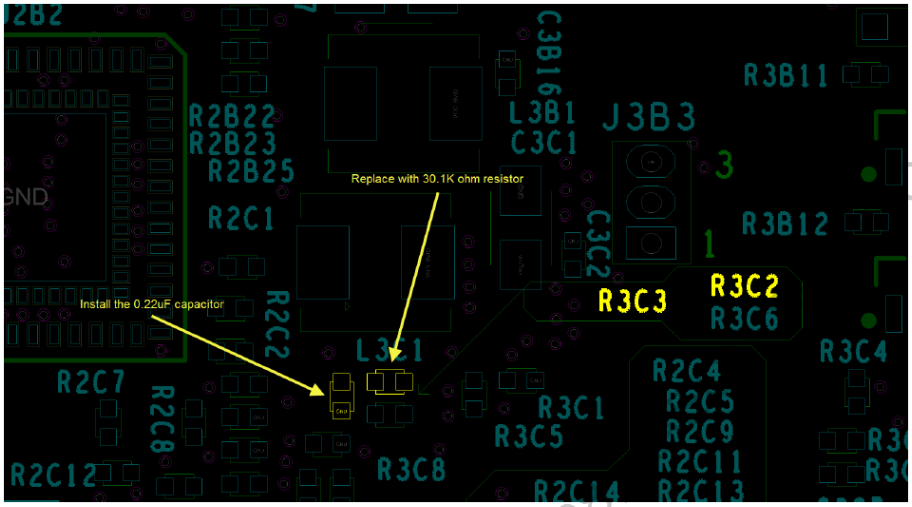
Figure 10. U2B2 Rework Instruction



2. Replace the device at the R3C2 location with the 30.1KΩ, 0402 resistor.

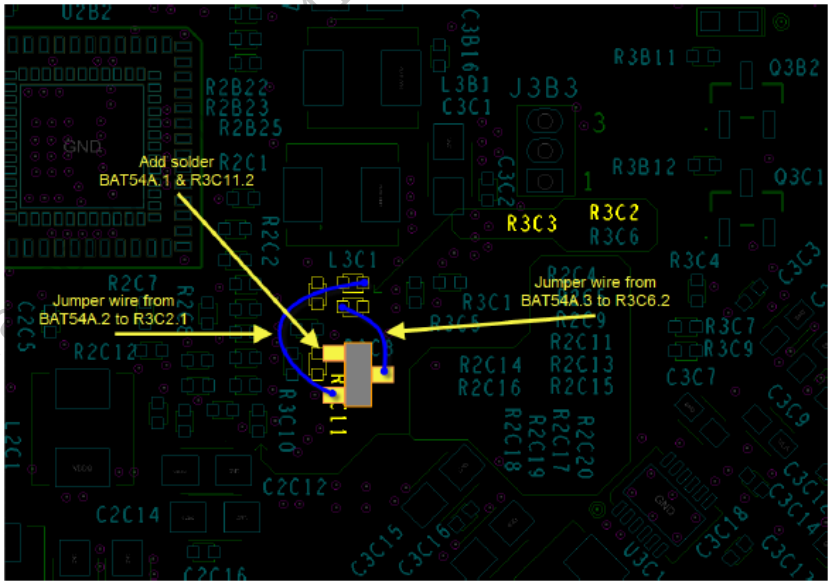
3. Install the 0.22UF, 0402 capacitor at the R3C3 location (EMPTY location in the layout).

Figure 11. R3C2 Rework Instruction



4. Add the BAT54A device at location shown below:
   i. Solder BAT54A pin 1 to R3C11 pin 2.
   ii. Add a jumper wire from BAT54A pin 2 to R3C2 pin 1.
   iii. Add a jumper wire from BAT54A pin 3 to R3C6 pin 2.

Figure 12. BAT54A Rework Instruction



6.6 Rework to Enable SPI dTPM

To enable the SPI dTPM, some reworks on the CRB, and modification of Discrete TPM location are required.

6.6.1 Applicability

Applicable to all fab.

6.6.2 Hardware Rework

6.6.2.1 TPM Chip Select Number (CS#) Rework

- Blue wire R4C16 Pad 1 to R5D6 Pad 2

- Remove R5D6

6.6.2.2 TPM IRQ Rework

- Unstuff R6D7

- Unstuff R3N32

- Blue wire R6D7 Pad 2 to R4C26 Pad 1

6.6.2.3 TPM Connector Pin 15 Rework

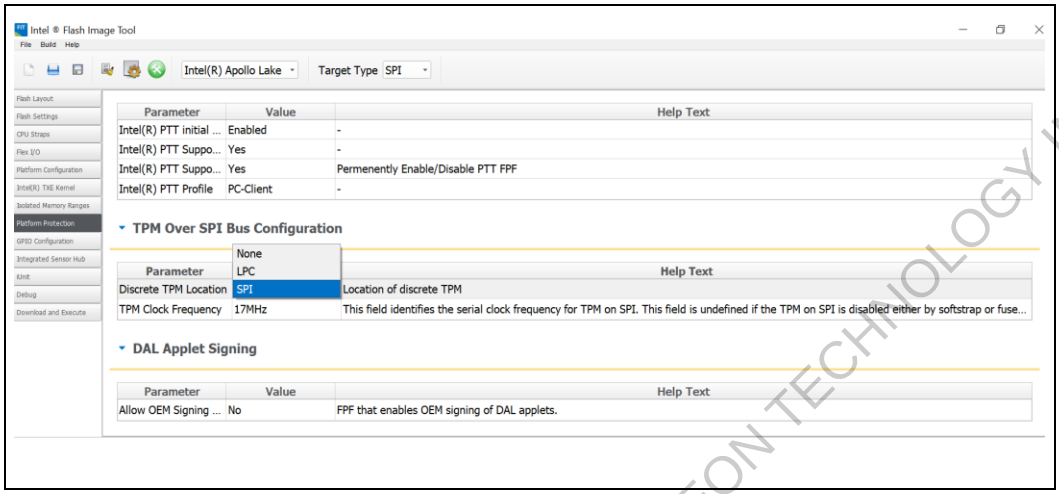
- Unstuff R5D7

6.6.3 Modification of Discrete TPM Location

Modify the Discrete TPM Location of Platform Protection section in BIOS to SPI.

This can be done by modifying the value of “Discrete TPM Location” to SPI using Intel® Flash Image Tool (FIT).

Figure 13. Discrete TPM Location from FIT



6.6.4 BIOS Setting Changes

Populate the Infineon (SLB9670VQ2.0) on the TPM connector on the CRB.

Change the setting in BIOS setup menu to enable dTPM.

Note: dTPM will be disabled if PTT is enabled. Default TPM setting from BIOS is PTT.

1) Boot to BIOS setup menu
2) Change setting:

Device Manager ➔ Security Configuration ➔ TPM Device <dTPM 1.2> or <dTPM 2.0>

6.6.5 Steps to Check for SPI dTPM

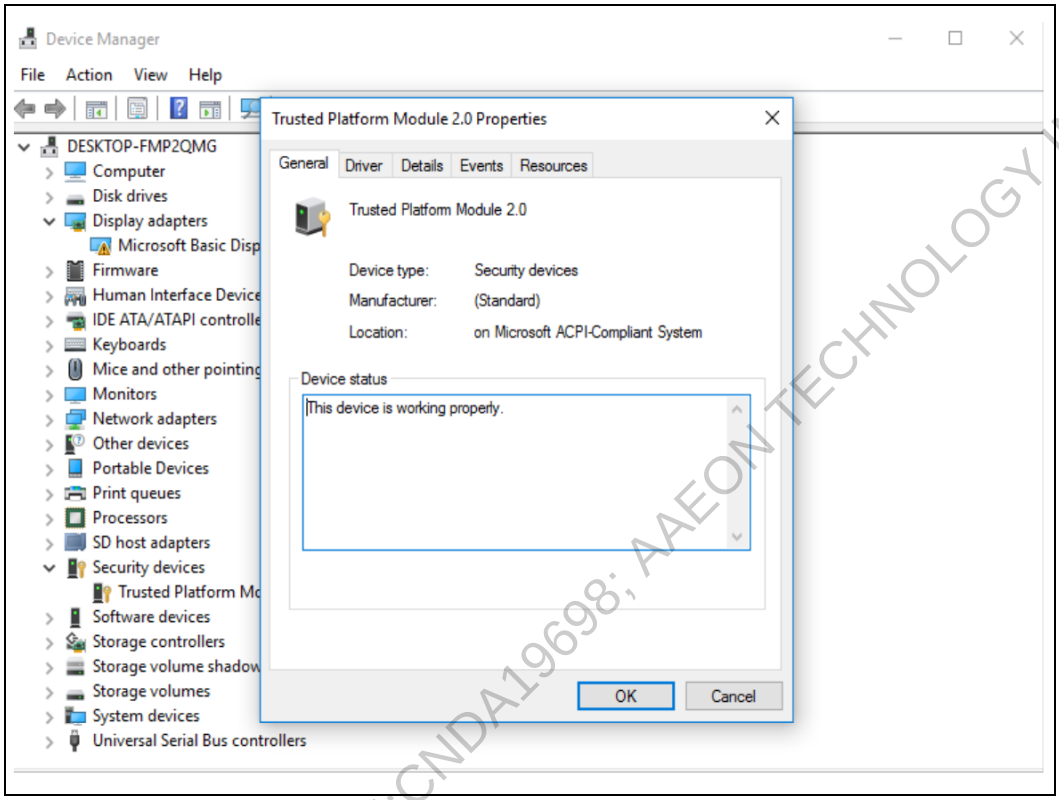
Boot the board into Windows OS.

Check the TPM's Properties from Device Manager:

Device Manager ➔ Security Devices ➔ Trusted Platform Module 2.0.

Ensure the device is working properly displayed.

Figure 14. Properties of TPM 2.0 shows SPI dTPM works fine



After performing the above rework steps, the LPC dTPM will not work on the CRB once SPI dTPM is enabled and it is working fine.

Appendix A Header List

This appendix provides information about the headers.

The following figure shows the CRB headers and board locations.

Figure 15. Headers on the CRB

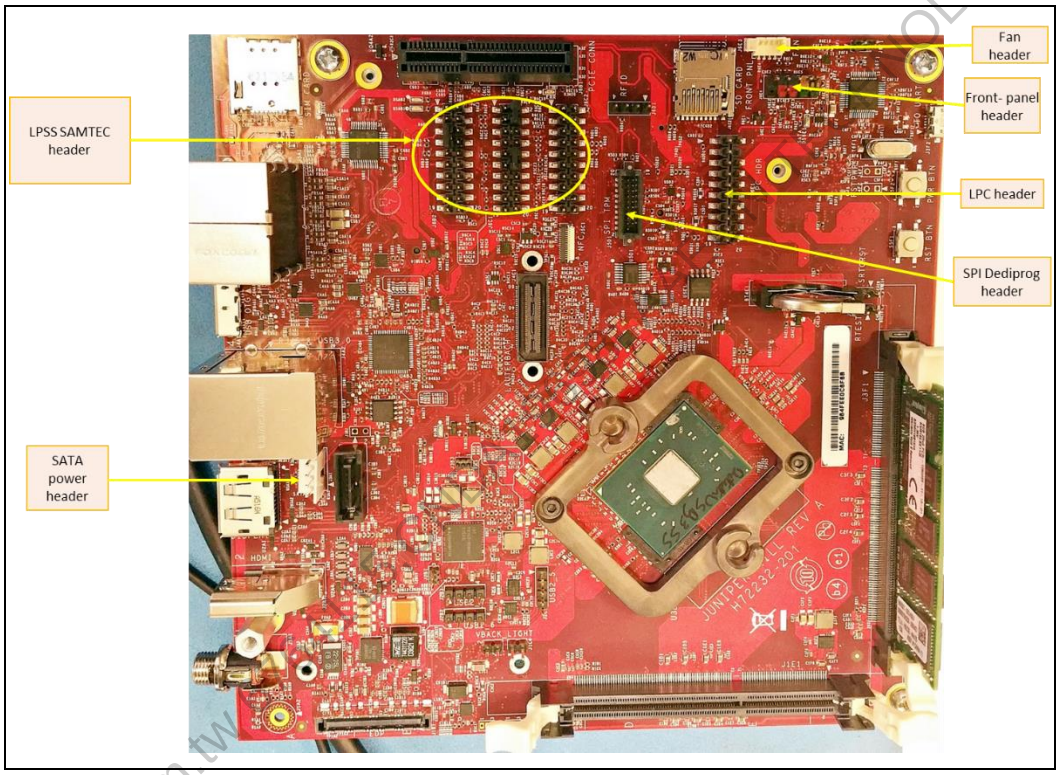
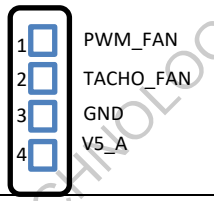
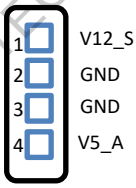
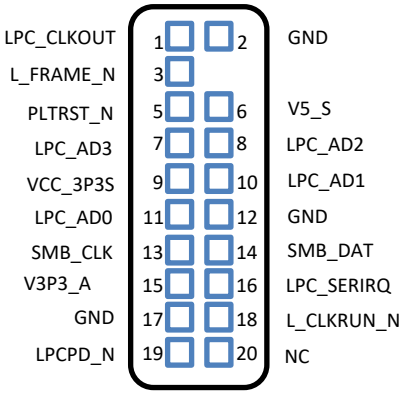
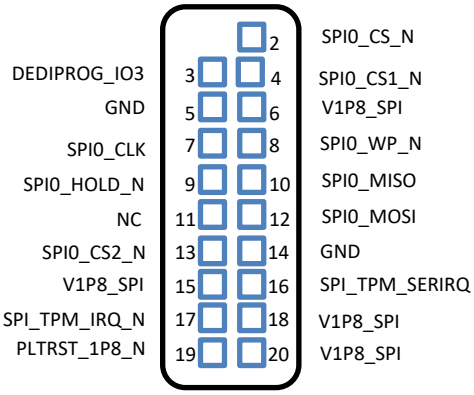
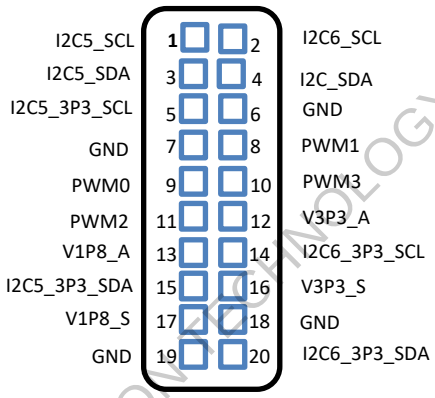
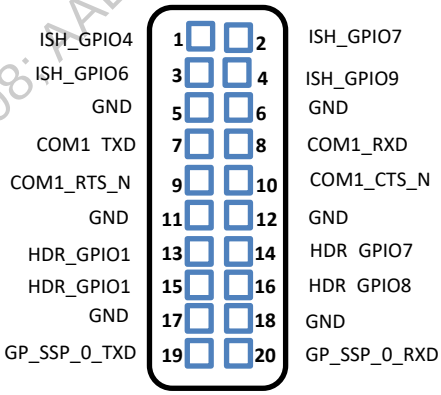
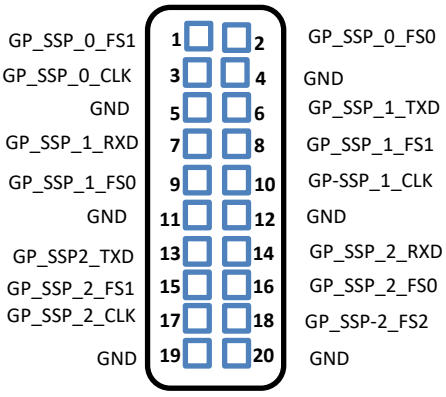
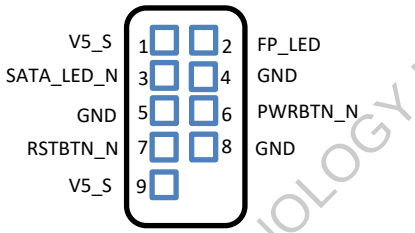


Table 20 shows the functionality and pin-out information for the CRB headers.

Table 20. CRB Headers Legend

Header Name	REF DES	Functionality	Pinout
Fan header	J6E3	CPU fan	
SATA power header	J3A1	SATA HDD power source	
LPC header	J6E1	External Port 80 display	
SPI Dediprog* header	J5D1	BIOS flash in-circuit programming	

Header Name	REF DES	Functionality	Pinout
LPSS header	J6C2	LPSS signals external probing	
LPSS header	J6B2	LPSS signals external probing	
LPSS header	J6C1	LPSS signals external probing	

Header Name	REF DES	Functionality	Pinout
Front-panel header	J6E4	Desktop front-panel button and LED indicator	

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