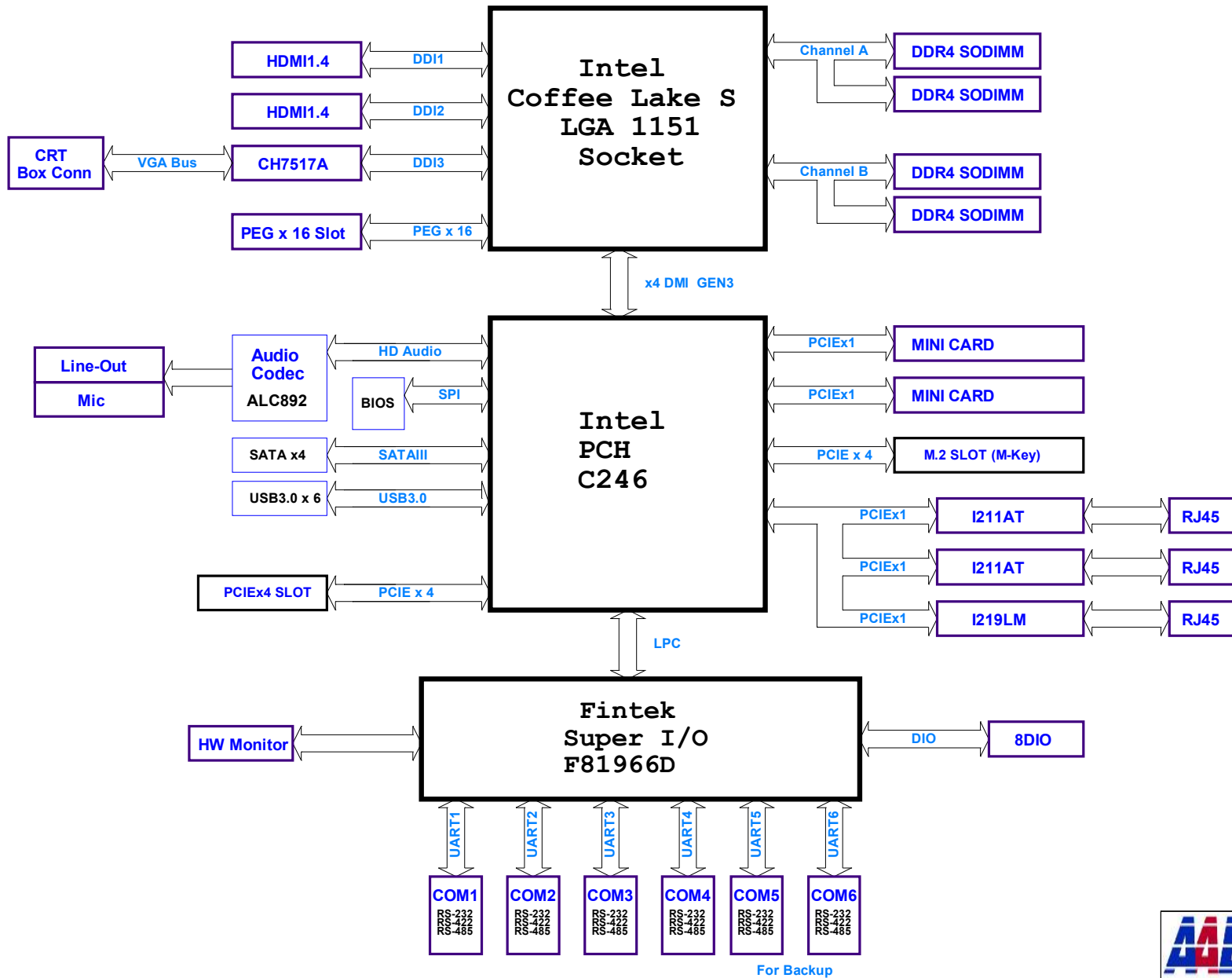


BOXER-6842M BLOCK DIAGRAM



- 01) Cover Sheet
- 02) GPIO Setting
- 03) DC Power Block Diagram
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- 14) DDR4 SO-DIMM-B0
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- 17) PCH 2-CLK
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- 19) PCH 4-DDI/USB3/LPC/eSPI
- 20) PCH 5-PCIE/SATA/FAN
- 21) PCH 6-HDA/SMB/MISC/I2S/RTC
- 22) PCH 7-PWR
- 23) PCH 8-VSS
- 24) PCIe * 16 SLOT
- 25) VGA
- 26) HDMI
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- 30) Backup
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- 32) M.2 (M-Key)
- 33) GPIO F75111RG
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- 52) POWER_VCC CORE & +VCC_GT
- 53) VCC CORE/ VCC_GT
- 54) EXT_GPU PWR
- 55) History



| | | |
|---------------------------------|-------------------------------------|---------------------|
| Title Cover Sheet | | |
| Size B | Document Number PBA-CFL02 | Rev. A1.0 |
| Date: Friday, February 21, 2020 | | Sheet: 1 of 55 |

Super I/O F81966D GPIO Pins :

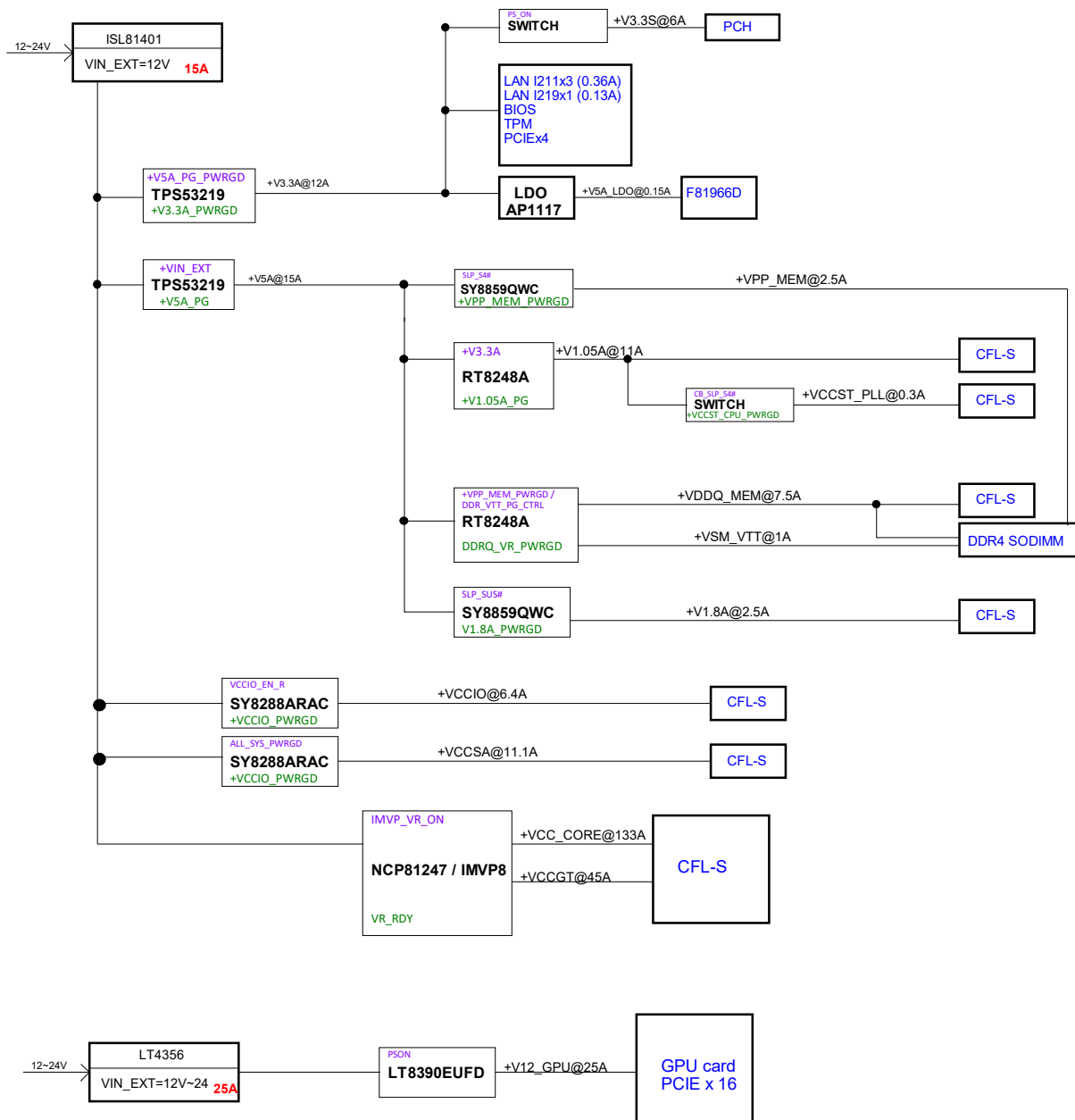
| PIN NO. | PIN Name | Multi-Func | Power Well | GPIO Function | PIN NO. | PIN Name | Multi-Func | Power Well | GPIO Function | PIN NO. | PIN Name | Multi-Func | Power Well | GPIO Function |
|---------|----------|--------------|------------|-----------------|---------|----------|------------|------------|---------------|---------|----------|------------|------------|---------------|
| 52 | GPIO00 | ERP_CTRL0# | SB3V | mSATA_PCl_e_SEL | 36 | GPIO30 | DCD3 | 3VCC | SDCD3X | 17 | GPIO60 | DCD5 | 3VCC | SDCD5X |
| 53 | GPIO01 | ERP_CTRL1# | SB3V | USB_EN | 37 | GPIO31 | RI3 | 3VCC | SRI3X | 18 | GPIO61 | RI5 | 3VCC | SRI5X |
| 54 | GPIO02 | SUS_WARN# | SB3V | SUS_WARN# | 38 | GPIO32 | CTS3 | 3VCC | SCTS3X | 19 | GPIO62 | CTS5 | 3VCC | SCTS5X |
| 55 | GPIO03 | SUSACK# | SB3V | SUSACK# | 39 | GPIO33 | DTR3 | 3VCC | SDTR3X | 20 | GPIO63 | DTR5 | 3VCC | SDTR5X |
| 56 | GPIO04 | SLP_SUS# | SB3V | SLP_SUS# | 40 | GPIO34 | RTS3 | 3VCC | SRTS3X | 21 | GPIO64 | DSR5 | 3VCC | SDSR5X |
| 57 | GPIO05 | SOUT5 | SB3V | STXD5X | 41 | GPIO35 | DSR3 | 3VCC | SDSR3X | 74 | GPIO65 | PME# | SB3V | LPC_PME# |
| 58 | GPIO06 | SIN5 | SB3V | SRXD5X | 42 | GPIO36 | SOUT3 | 3VCC | STXD3X | 86 | GPIO66 | DPWROK | VBAT | DPWROK |
| 59 | GPIO07 | RTS5# | SB3V | SRTS5X | 43 | GPIO37 | SIN3 | 3VCC | SRXD3X | 87 | GPIO67 | S5# | VBAT | SLP_S4# |
| 65 | GPIO10 | LED_VSB | SB3V | NC | 44 | GPIO40 | DCD4 | 3VCC | SDCD4X | 103 | GPIO70 | PE | 3VCC | DIO_0 |
| 66 | GPIO11 | LED_VCC | SB3V | NC | 45 | GPIO41 | RI4 | 3VCC | SRI4X | 104 | GPIO71 | BUSY | 3VCC | DIO_1 |
| 67 | GPIO12 | IRTX/SCL | SB3V | SML1_CLK | 46 | GPIO42 | CTS4 | 3VCC | SCTS4X | 105 | GPIO72 | ACK | 3VCC | DIO_2 |
| 68 | GPIO13 | IRRX/SDA | SB3V | SML1_DATA | 47 | GPIO43 | DTR4 | 3VCC | SDTR4X | 106 | GPIO73 | SLIN | 3VCC | DIO_3 |
| 69 | GPIO14 | ATX_AT_TRAP | SB3V | ATX_AT_TRAP | 48 | GPIO44 | RTS4 | 3VCC | SRTS4X | 107 | GPIO74 | INIT | 3VCC | DIO_4 |
| 70 | GPIO15 | WDRST# | SB3V | WDRST# | 49 | GPIO45 | DSR4 | 3VCC | SDSR4X | 108 | GPIO75 | ERR | 3VCC | DIO_5 |
| 71 | GPIO16 | BEEP/SDA | SB3V | SIO_SPK | 50 | GPIO46 | SOUT4 | 3VCC | STXD4X | 109 | GPIO76 | AFD | 3VCC | DIO_6 |
| 72 | GPIO17 | PECI | SB3V | H_PECI | 51 | GPIO47 | SIN4 | 3VCC | SRXD4X | 110 | GPIO77 | STB | 3VCC | DIO_7 |
| 76 | GPIO20 | ALBERT#/SCL3 | SB3V | NC | 9 | GPIO50 | RTS6 | 3VCC | SRTS6X | 111 | GPIO80 | PD0 | 3VCC | NC |
| 77 | GPIO21 | ATXPG_IN | SB3V | ATXPG_IN | 10 | GPIO51 | SIN6 | 3VCC | SRXD6X | 112 | GPIO81 | PD1 | 3VCC | NC |
| 78 | GPIO22 | PWSIN# | SB3V | PANSWH# | 11 | GPIO52 | SOUT6 | 3VCC | STXD6X | 113 | GPIO82 | PD2 | 3VCC | NC |
| 79 | GPIO23 | PWSOUT# | SB3V | PM_PWRBTN# | 12 | GPIO53 | DCD6 | 3VCC | SDCD6X | 114 | GPIO83 | PD3 | 3VCC | NC |
| 80 | GPIO24 | S3# | SB3V | SLP_S3# | 13 | GPIO54 | RI6 | 3VCC | SRI6X | 115 | GPIO84 | PD4 | 3VCC | NC |
| 81 | GPIO25 | PS_ON# | SB3V | PS_ON# | 14 | GPIO55 | CTS6 | 3VCC | SCTS6X | 116 | GPIO85 | PD5 | 3VCC | NC |
| 82 | GPIO26 | PWOK | VBAT | PWROK | 15 | GPIO56 | DTR6 | 3VCC | SDTR6X | 117 | GPIO86 | PD6 | 3VCC | WLAN_DIS2# |
| 83 | GPIO27 | RSMRST# | VBAT | RSMRST# | 16 | GPIO57 | DSR6 | 3VCC | SDSR6X | 118 | GPIO87 | PD7 | 3VCC | WLAN_DIS3# |

PCH GPIO Pins :

| Group | Name | Power Well | Default | GPIO Function |
|---------|-------------|----------------------|---------|--------------------|
| Group A | GPP_A0 | Primary Core 3.3V | | KBRST |
| | GPP_A1 | | | LPC_A00 |
| | GPP_A2 | | | LPC_A01 |
| | GPP_A3 | | | LPC_A02 |
| | GPP_A4 | | | LPC_A03 |
| | GPP_A5 | | | LPC_FRAME# |
| | GPP_A6 | | | INT_SERIRQ |
| | GPP_A7 | | | PIRQ0# |
| | GPP_A8 | | | PM_CLKRUN# |
| | GPP_A9 | | | PCH_CLK_LPC0 |
| | GPP_A10 | | | CLK_LPC1_R |
| | GPP_A11 | | | LPC_PME# |
| | GPP_A12 | | | |
| | GPP_A13 | | | SUS_WARN# |
| | GPP_A14 | | | PM_SUS_STAT# |
| Group B | GPP_A15 | Primary Core 3.3V | | SUSACK# |
| | GPP_A16 | | | |
| | GPP_A17 | | | |
| | GPP_A18 | | | H_A20GATE |
| | GPP_A19-A23 | | | |
| | GPP_B0-B7 | | | |
| | GPP_B8 | | | CLK_PCIE_LAN# REQ# |
| | GPP_B9 | | | |
| | GPP_B10 | | | |
| | GPP_B11 | | | |
| Group C | GPP_B12 | Primary Core 3.3V | | |
| | GPP_B13 | | | PLT_RST# |
| | GPP_B14 | | | HDA_SPKR |
| | GPP_B15-B21 | | | SDIO0_BIOS_STRAP |
| | GPP_B22 | | | SML1_ALERT# |
| | GPP_C0 | | | SMB_CLK |
| | GPP_C1 | | | SMB_DATA |
| | GPP_C2 | | | SMB_ALERT# |
| | GPP_C3 | | | SML0_CLK |
| | GPP_C4 | | | SML0_DATA |
| Group D | GPP_C5 | Primary Core 3.3V | | SML0_ALERT# |
| | GPP_C6 | | | SML1_CLK |
| | GPP_C7 | | | SML1_DATA |
| | GPP_C8-C15 | | | |
| | GPP_C16 | | | I2C0_SDA |
| | GPP_C17 | | | I2C0_SCL |
| | GPP_C18-C23 | | | |
| | | | | |
| | | | | |
| | | | | |

| Group | Name | Power Well | Default | GPIO Function |
|---------|-------------|--------------------------|---------|---------------------|
| Group D | GPP_D0-8 | Deep Sleep Power 3.3V | | |
| | GPP_D9 | | | |
| | GPP_D10 | | | |
| | GPP_D11 | | | |
| | GPP_D12 | | | |
| Group E | GPP_D13-18 | Primary Core 3.3V | | |
| | GPP_D17-D23 | | | |
| | GPP_E0-2 | | | SATAGP0-SATAGP2 |
| | GPP_E4 | | | |
| | GPP_E5 | | | |
| Group F | GPP_E6-7 | Primary Core 3.3V | | |
| | GPP_E8 | | | |
| | GPP_E9 | | | SATA_LED# |
| | GPP_E10 | | | USB_OC# 0 |
| | GPP_E11 | | | USB_OC# 1 |
| Group G | GPP_E12 | Primary Core 3.3V | | USB_OC# 2 |
| | GPP_F0 | | | USB_OC# 3 |
| | GPP_F15 | | | SATAGP3 |
| | GPP_F16 | | | USB_OC# 4 |
| | GPP_F17 | | | USB_OC# 5 |
| Group H | GPP_F18 | Primary Core 3.3V | | USB_OC# 6 |
| | GPP_F19 | | | USB_OC# 7 |
| | GPP_F20 | | | |
| | GPP_F21 | | | |
| | GPP_F22-23 | | | |
| Group I | GPP_H0-2 | Primary Core 3.3V | | |
| | GPP_H3 | | | |
| | GPP_H4 | | | CLK_PCIE_MINI_REQ#1 |
| | GPP_H5-H23 | | | CLK_PCIE_MINI_REQ#2 |
| | GPP_I0 | | | DPB_HPD |
| Group J | GPP_I1 | Primary Core 3.3V | | DPB_HPD |
| | GPP_I2 | | | DPD_HPD |
| | GPP_I3 | | | DPD_HPD |
| | GPP_I4 | | | DPD_HPD |
| | GPP_I5 | | | DPB_CTRLCLK |
| | GPP_I6 | | | DPB_CTRLCLK |
| | GPP_I7 | | | DPB_CTRLCLK |
| | GPP_I8 | | | DPB_CTRLCLK |
| | GPP_I9 | | | DPD_CTRLCLK |
| | GPP_I10 | | | DPD_CTRLCLK |
| Group K | GPP_I11 | Primary Core 3.3V | | H_SKT0CC_N |
| | GPP_I12-I14 | | | |

| Group | Name | Power Well | Default | GPIO Function |
|---------|-------------|----------------------|---------|---------------------|
| Group J | GPP_J0 | Primary Core 1.8V | | |
| | GPP_J1 | | | CPU_VCCIO_PWR_GATEB |
| | GPP_J2 | | | |
| | GPP_J3 | | | |
| | GPP_J4 | | | GPP_J4 |
| | GPP_J5 | | | |
| | GPP_J6 | | | |
| | GPP_J7 | | | |
| | GPP_J8 | | | |
| | GPP_J9 | | | GPP_J9 |
| Group K | GPP_K0-K23 | Primary Core 3.3V | | |
| | GPP_K1 | | | |
| | GPP_K2 | | | PM_BATLOW# |
| | GPP_K3 | | | AC_PRESENT |
| | GPP_K4 | | | LAN_WAKER# |
| | GPP_K5 | | | PM_PWRBTN# |
| | GPP_K6 | | | SLP_S3# |
| | GPP_K7 | | | SLP_S4# |
| | GPP_K8 | | | PCH_SLP_A_N |
| | GPP_K9 | | | GPP_D_USB_WAKEOUT |
| GPD | GPP_K10-K23 | Primary Core 3.3V | | SLP_CLK |
| | GPP_K11 | | | |
| | GPP_K12 | | | |
| | GPP_K13 | | | |
| | GPP_K14 | | | |
| | GPP_K15 | | | |
| | GPP_K16 | | | |
| | GPP_K17 | | | |
| | GPP_K18 | | | |
| | GPP_K19 | | | SLP_S3# |
| GPE | GPP_K20 | Primary Core 3.3V | | SLP_S3# |
| | GPP_K21 | | | SLP_LAMPHY_ENABLE |



#337345 EDS P126~P132

| | Voltage(V) | Current(A) | Watt(W) | Total |
|--------------|------------|------------|---------|---------|
| +VCORE (80W) | 0~1.52 | 133 | 133 | 225.468 |
| +VCCGT | 0~1.52 | 64 | 64 | |
| +VDDQ | 1.2 | 3.3 | 3.96 | |
| +VCCSA | 1.05 | 11.1 | 11.65 | |
| +VCCIO | 0.95 | 6.4 | 6.08 | |
| +VCCOPC | 1 | 4.2 | 4.2 | |
| +VCCOEPIO | 1 | 2 | 2 | |
| +VCCOPC_1P8 | 1.8 | 0.1 | 0.18 | |
| +VCCST_ | 1.05 | 0.08 | 0.084 | |
| +VCCSTG | 1.05 | 0.02 | 0.021 | |
| +VCCPLL | 1.05 | 0.15 | 0.157 | |
| +VCCPLL OC | 1.2 | 0.13 | 0.156 | |

#571182 EDS P64

| | Voltage (V) | Current (A) | Watt (W) | Total |
|-------------------|-------------|-------------|----------|-------|
| VCCAPLL_1P05 | 1.05 | 0.041 | 0.043 | 8.447 |
| VCCA_BCLK_1P05 | 1.05 | 0.009 | 0.01 | |
| VCCA_SRC_1P05 | 1.05 | 0.169 | 0.177 | |
| VCCA_XTAL_1P05 | 1.05 | 0.005 | 0.005 | |
| VCCAMPHYPLL_1P05 | 1.05 | 0.145 | 0.152 | |
| VCCPRIM_1P05 | 1.05 | 7.169 | 7.527 | |
| VCCPRIM_MPHY_1P05 | 1.05 | 0.106 | 0.111 | |
| VCCDSW_1P05 | 1.05 | 0.01 | 0.01 | |
| VCCDUSB_1P05 | 1.05 | 0.421 | 0.442 | |

| | Voltage (V) | Current (A) | Watt (W) | Total |
|--------------|-------------|-------------|----------|-------|
| VCC8DA | 3.3 | 0.008 | 0.026 | 7.111 |
| VCC8SW 3P3 | 3.3 | 0.113 | 0.373 | |
| VCCPRIM 3P3 | 3.3 | 0.761 | 2.511 | |
| VCCPGPPA | 3.3 | 0.102 | 0.337 | |
| VCCPGPPBC | 3.3 | 0.344 | 1.135 | |
| VCCPGPPD | 3.3 | 0.14 | 0.46 | |
| VCCPGPPFE | 3.3 | 0.175 | 0.577 | |
| VCCPGPPG 3P3 | 3.3 | 0.145 | 0.479 | |
| VCCPGPPHK | 3.3 | 0.263 | 0.868 | |
| VCCRTC | 3.0 | 0.06 | 0.18 | |
| VCCPGPPHK | 3.3 | 0.05 | 0.165 | |



| | Title |
|---|-------|
|---|-------|

DC Power Block Diagram

| |
|--------|
| Size |
| Custom |

Document Number
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Date: Friday, February 21, 2020

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COFFEE LAKE-S BGA PROCESSOR (DMI/PEG)



Title

PROCESSOR 1-DMI/PEG

Size
A

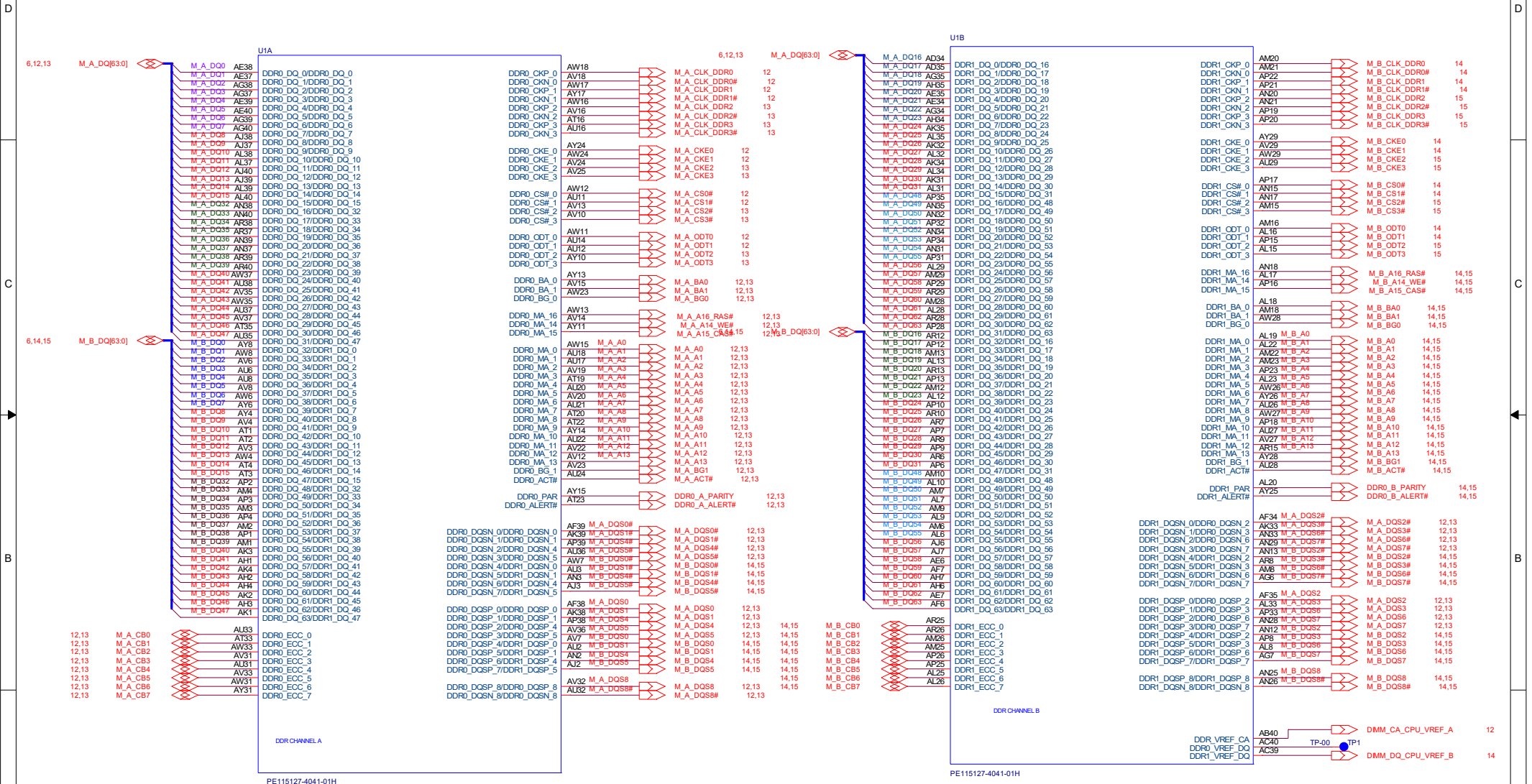
Document Number
PBA-CFL02

Rev:
A0.1

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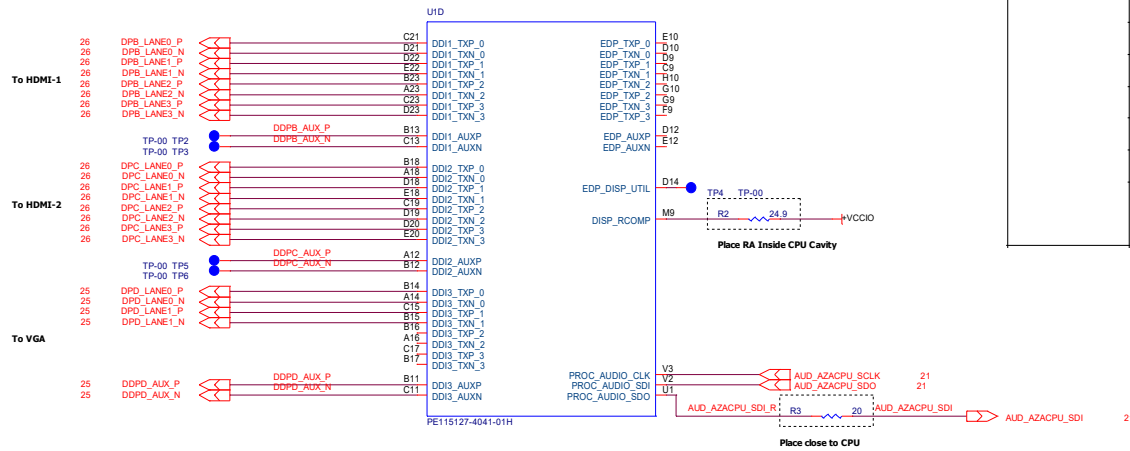
CFL-S Non-Interleave

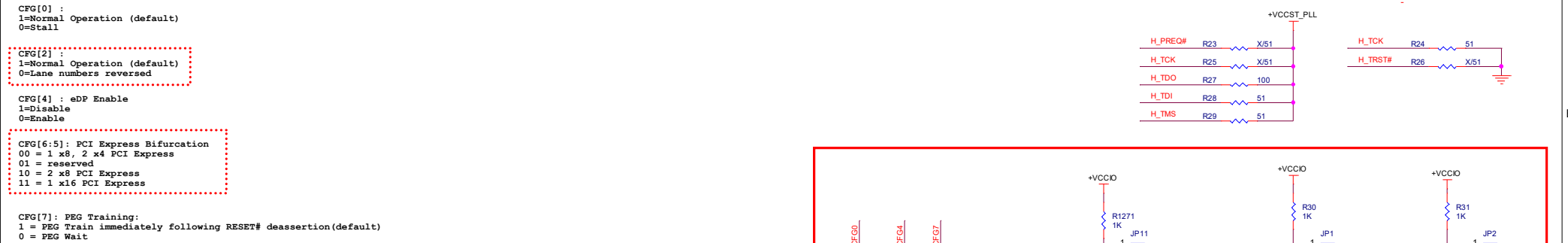


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|-------|---------------------------|------------------|-----------|
| Title | | PROCESSOR 2-DDR4 | |
| Size | A | Document Number | PBA-CFL02 |
| Date: | Friday, February 21, 2020 | Sheet: | 6 of 55 |

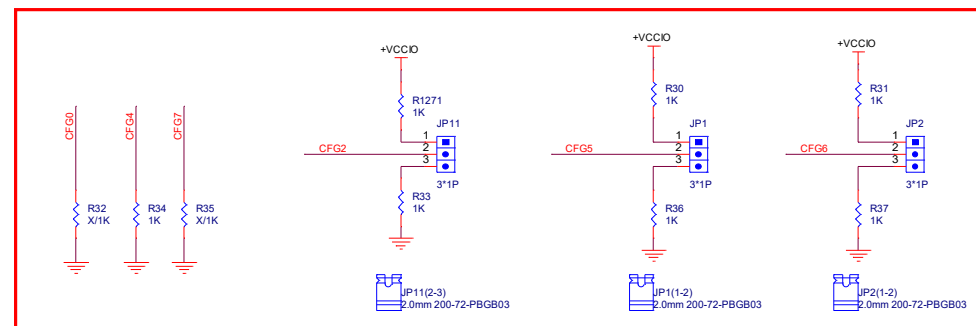
Mapping of HDMI* Signals for DDI Ports

| Port | Digital Display Interface Pins | CRB Digital Display Interface Signals | HDMI* Signals |
|--------|-------------------------------------|---------------------------------------|----------------|
| Port 1 | DDI1_TXP[0] | DDI1_LANE0_DP | HDMIx_TX2_DP |
| | DDI1_TXN[0] | DDI1_LANE0_DN | HDMIx_TX2_DN |
| | DDI1_TXP[1] | DDI1_LANE1_DP | HDMIx_TX1_DP |
| | DDI1_TXN[1] | DDI1_LANE1_DN | HDMIx_TX1_DN |
| | DDI1_TXP[2] | DDI1_LANE2_DP | HDMIx_TX0_DP |
| | DDI1_TXN[2] | DDI1_LANE2_DN | HDMIx_TX0_DN |
| | DDI1_TXP[3] | DDI1_LANE3_DP | HDMIx_CLK_DP |
| | DDI1_TXN[3] | DDI1_LANE3_DN | HDMIx_CLK_DN |
| | Hot plug detect used by HDMI Port 1 | DDPB_HPD | DDI1_HPD_Q |
| Port 2 | HDMI DDC lines for Port 1 | DDPB_CTRLCLK | DDI1_CTRL_CLK |
| | | DDPB_CTRLDATA | DDI1_CTRL_DATA |
| | DDI2_TXP[0] | DDI2_LANE0_DP | HDMIx_TX2_DP |
| | DDI2_TXN[0] | DDI2_LANE0_DN | HDMIx_TX2_DN |
| | DDI2_TXP[1] | DDI2_LANE1_DP | HDMIx_TX1_DP |
| | DDI2_TXN[1] | DDI2_LANE1_DN | HDMIx_TX1_DN |
| | DDI2_TXP[2] | DDI2_LANE2_DP | HDMIx_TX0_DP |
| | DDI2_TXN[2] | DDI2_LANE2_DN | HDMIx_TX0_DN |
| | DDI2_TXP[3] | DDI2_LANE3_DP | HDMIx_CLK_DP |
| Port 2 | HDMI DDC lines for Port 2 | DDPC_HPD | DDI2_HPD_Q |
| | | DDPC_CTRLCLK | DDI2_CTRL_CLK |
| | | DDPC_CTRLDATA | DDI2_CTRL_DATA |

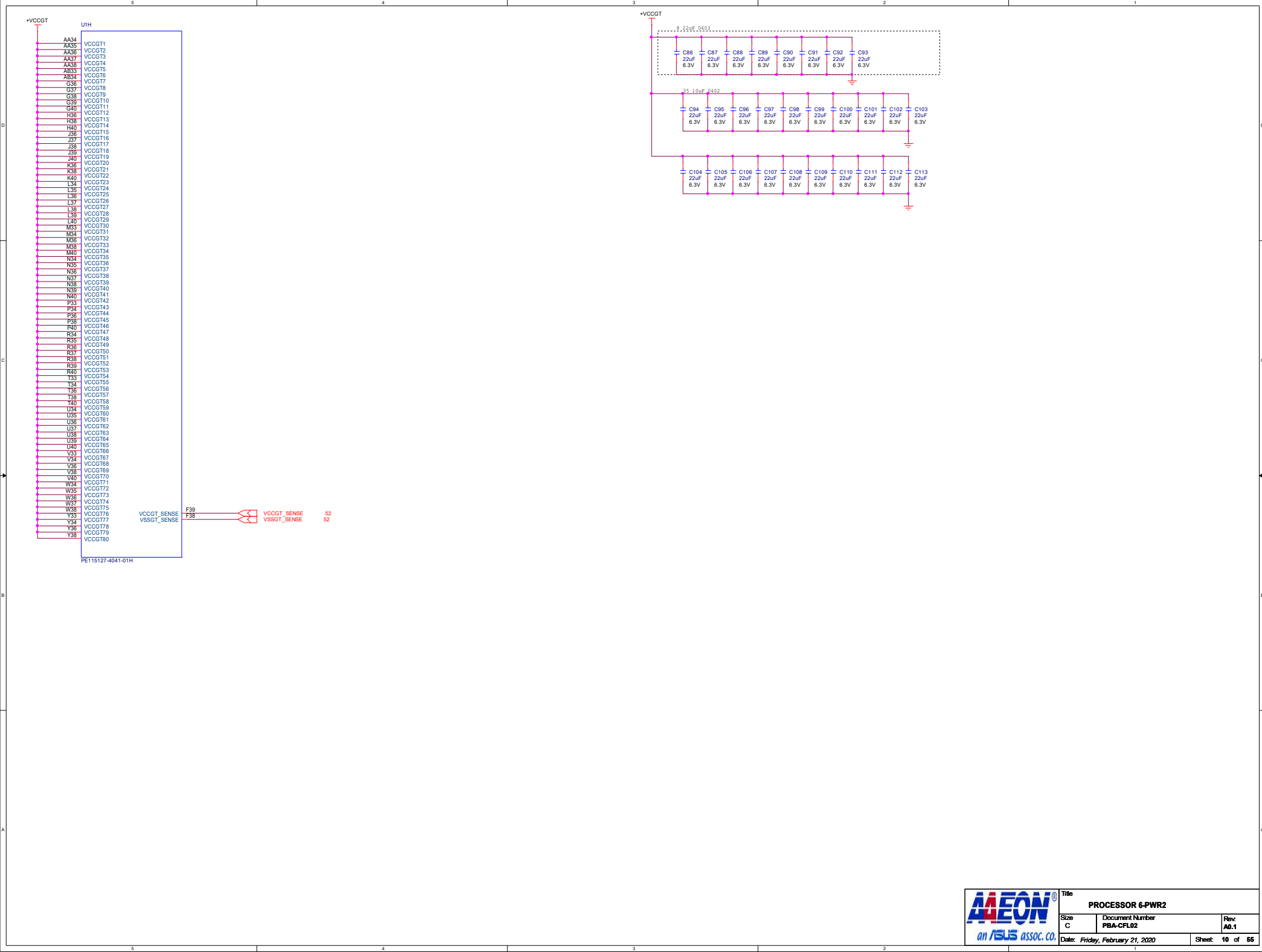


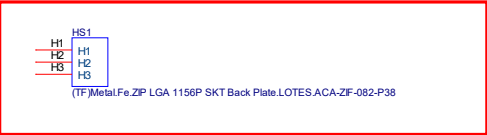


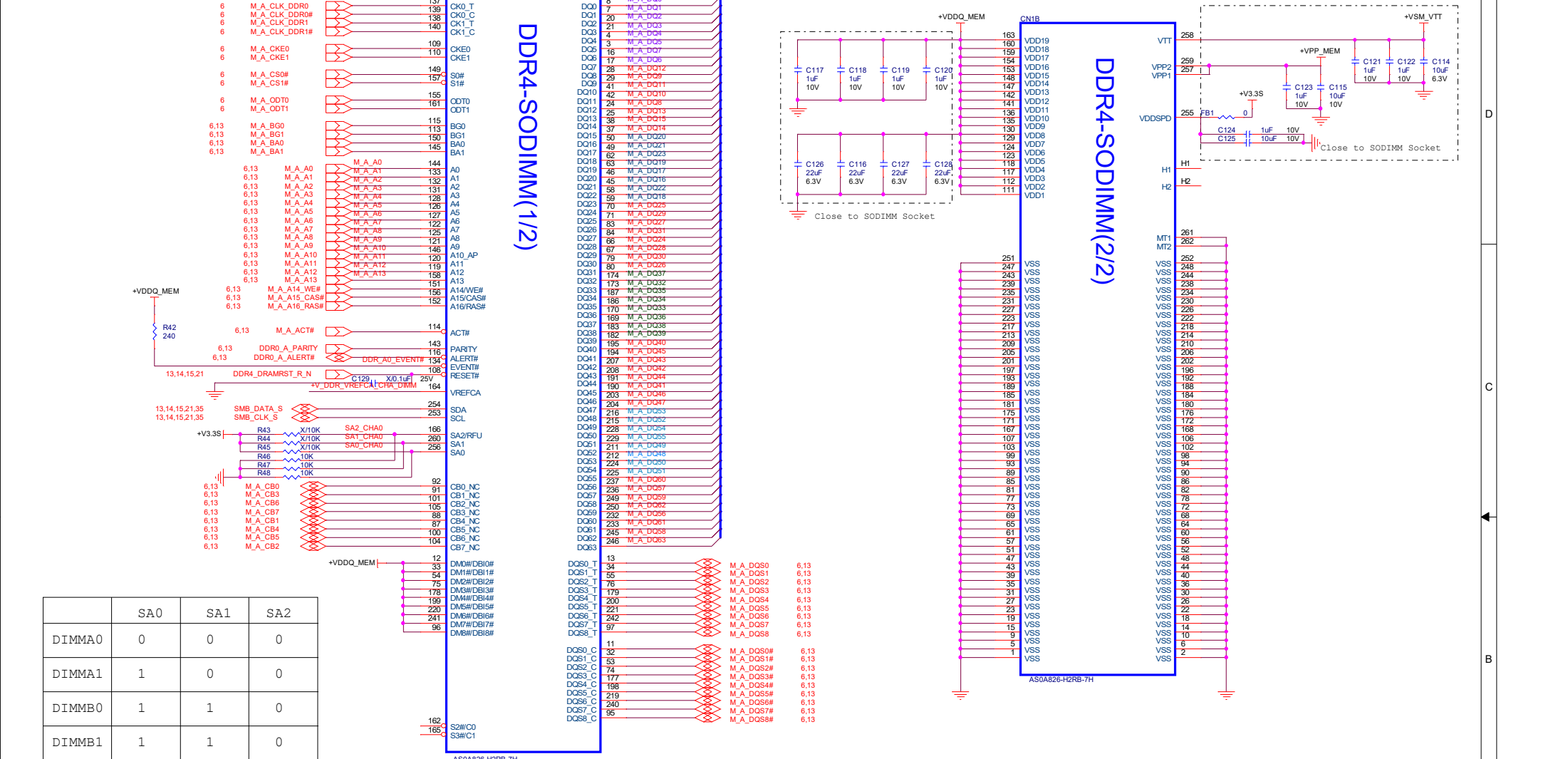
| Bifurcation | Link Width | | | CFG Signals | | | Lanes | | | | | | | | | | | | | | | |
|---------------------|------------|-------|-------|-------------|---------|---------|-------|----|----|----|----|----|---|---|---|---|----|----|----|----|----|----|
| | 0:1:0 | 0:1:1 | 0:1:2 | CFG [6] | CFG [5] | CFG [2] | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 1x16 | x16 | N/A | N/A | 1 | 1 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 1x16 Reversed | x16 | N/A | N/A | 1 | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 2x8 | x8 | x8 | N/A | 1 | 0 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 2x8 Reversed | x8 | x8 | N/A | 1 | 0 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1x8+2x4 | x8 | x4 | x4 | 0 | 0 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 1x8+2x4 Reversed | x8 | x4 | x4 | 0 | 0 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

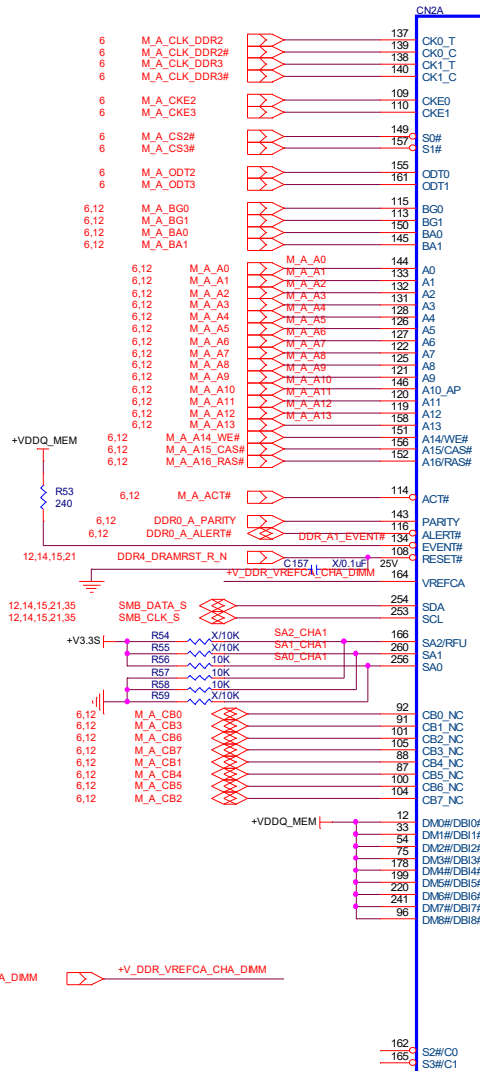


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|--|-------------------------------------|--|------------------------------|
| Title | | | |
| PROCESSOR 4-CLK/CFG/RSVD | | | |
| Size A | Document Number PBA-CFL02 | | Rev: A0.1 |
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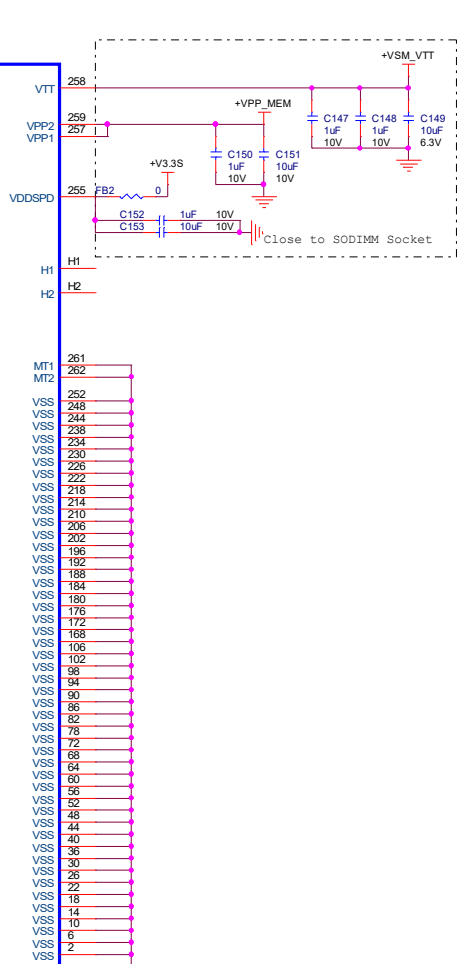
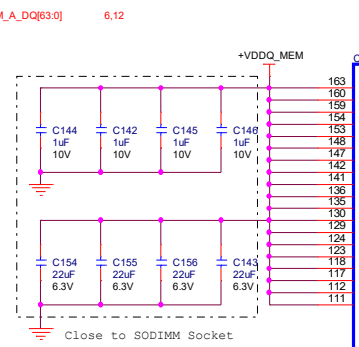
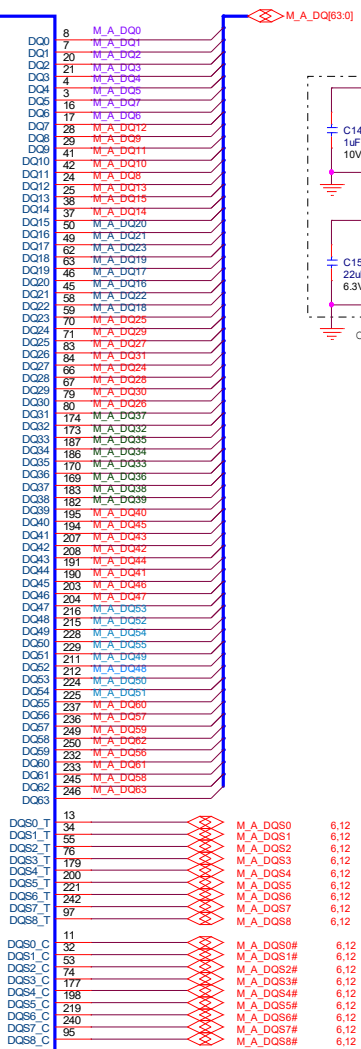




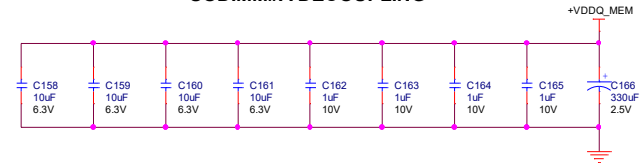


SODIMM#A1

DDR4-SODIMM(1/2)



SODIMM#A DECOUPLING



Title

DDR4 SO-DIMM-A

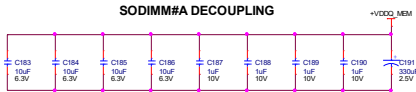
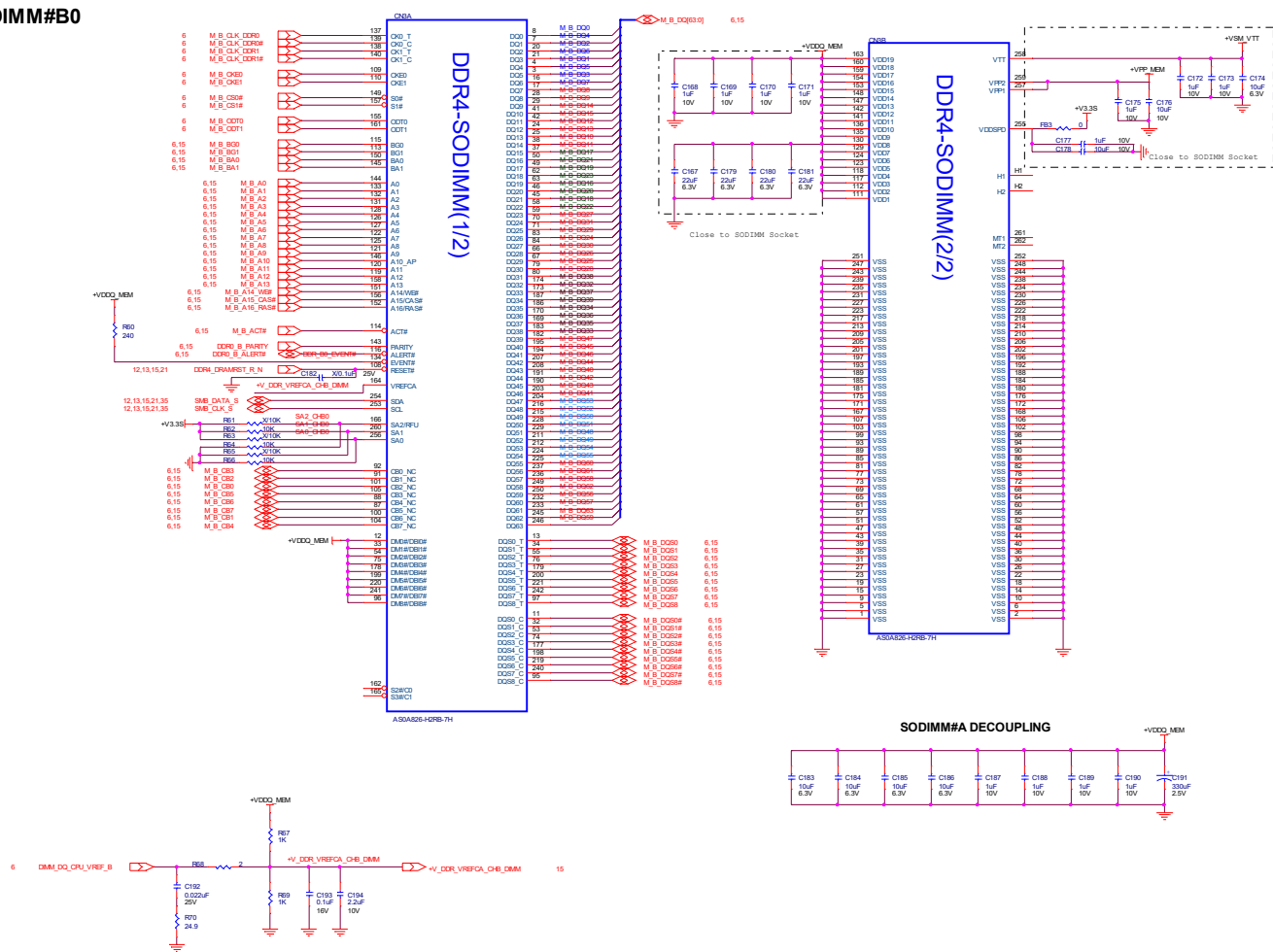
Size
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Document Number
PBA-CFL02

Rev:
A0.1

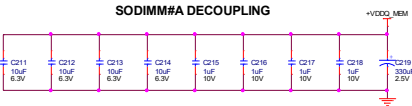
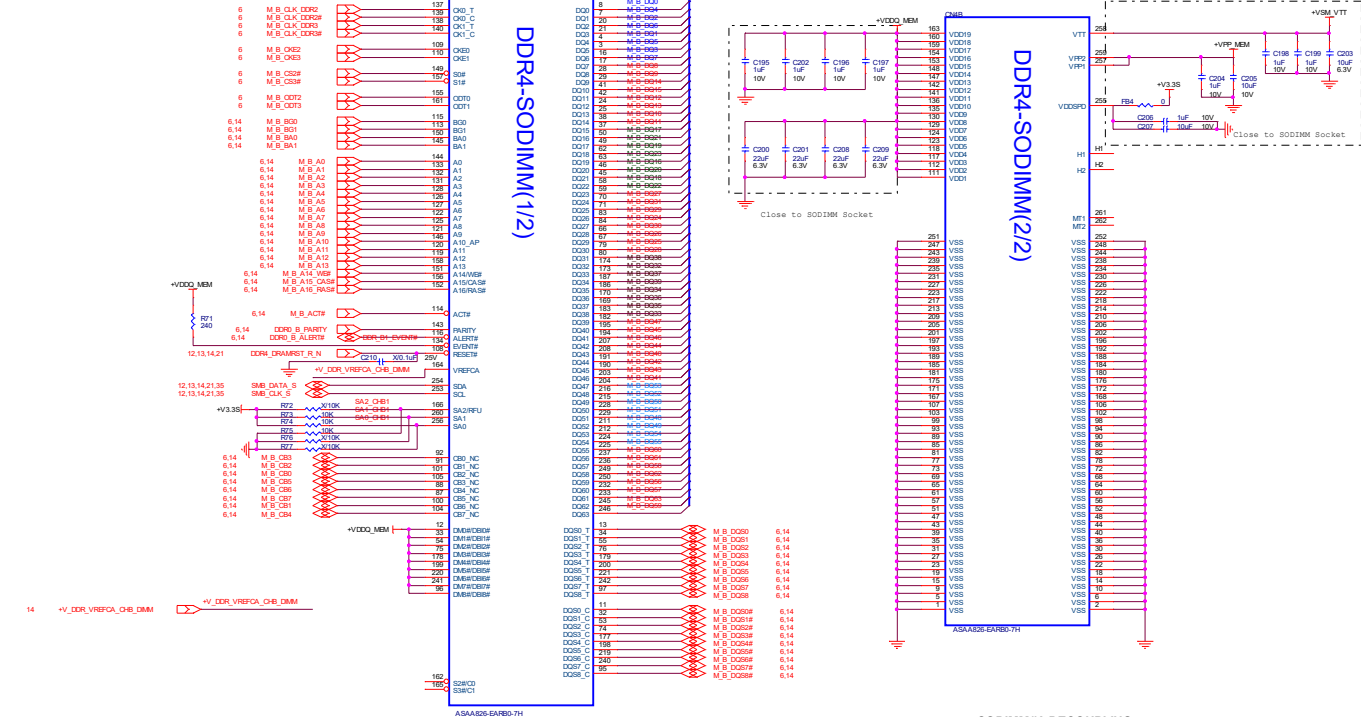
Date: *Friday, February 21, 2020*

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SODIMM#B0

| | | |
|--|-------------------------------------|------------------------|
| Title | | |
| DDR4 SO-DIMM-B | | |
| Size B | Document Number PBA-CFL02 | Rev. A0.1 |
| Date: <i>Friday, February 21, 2020</i> | | Sheet: 14 of 55 |

SODIMM#B1



| | | |
|--|-------------------------------------|-------------------------------|
| Title | | |
| DDR4 SO-DIMM-B | | |
| Size B | Document Number PBA-CFL02 | Rev: A0.1 |
| Date: <i>Friday, February 21, 2020</i> | | Sheet: 15 of 55 |

HW Strap



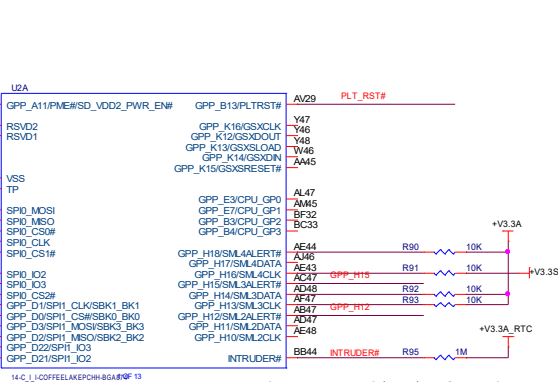
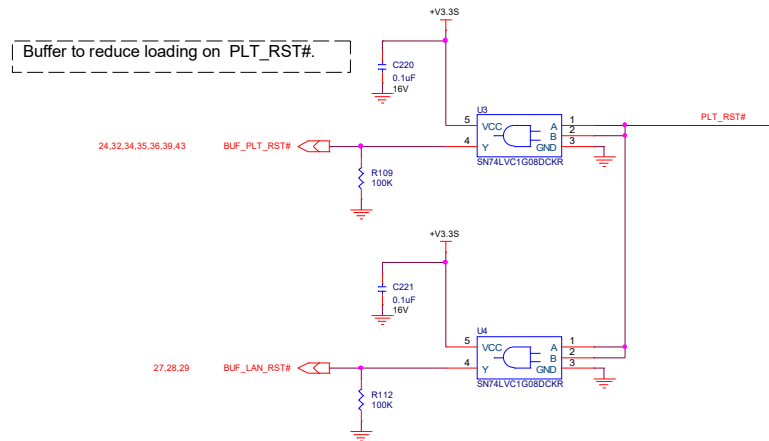
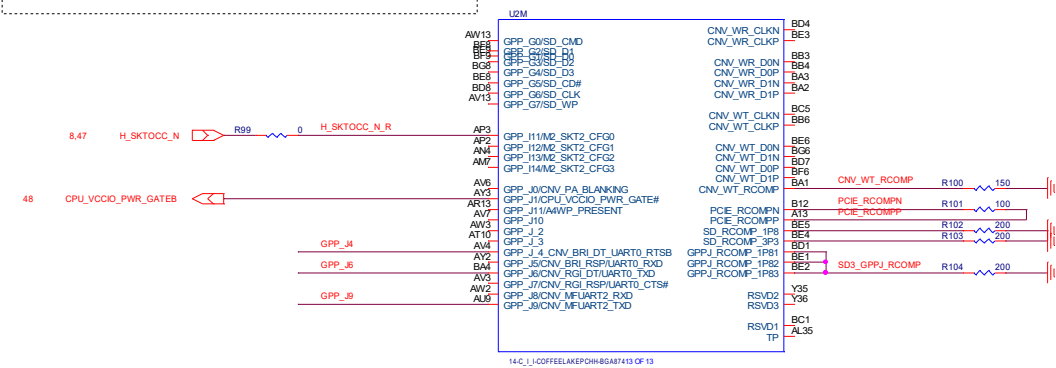
A weak external pull-up is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.



Design note:
XTAL Frequency selection
1 = 24MHz (25MHz when XTAL Freq device non zero)
0 = 38.4/19.2MHz
PCH has internal 20K PD

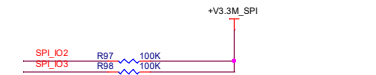


Design note:
Select the SPI BIOS flash interface operating voltage
1 = VCCPSI is connected to 1.8V rail
0 = VCCPSI is connector to 3.3V rail (default)
PCH had internal 20K PD



Intruder Detect: This signal can be set to disable the system if box detected open.

HW Strap



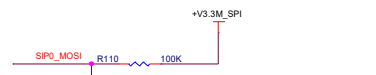
SPI0_IO2/SPI0_IO3
External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V.



External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



ESPI Flash sharing
0 : Master attached flash sharing
1 : Slave attached flash sharing
PCH has internal weak PD



External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



Title

PCH 1-SPI/SMLINK/UART/I2C

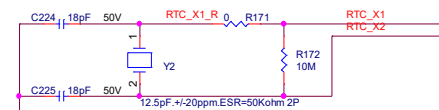
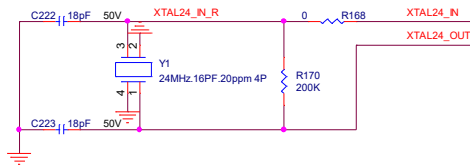
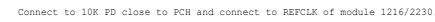
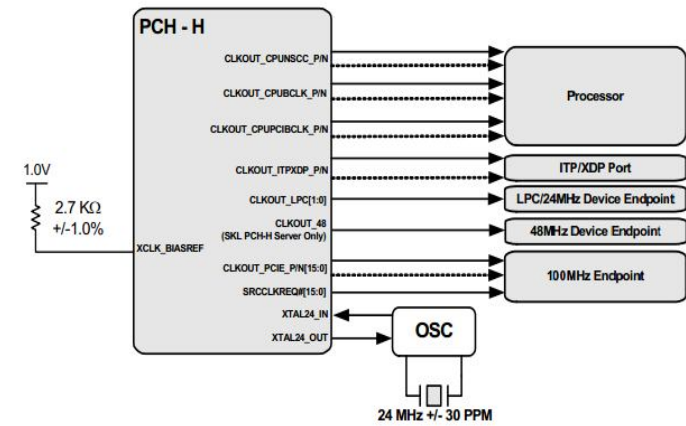
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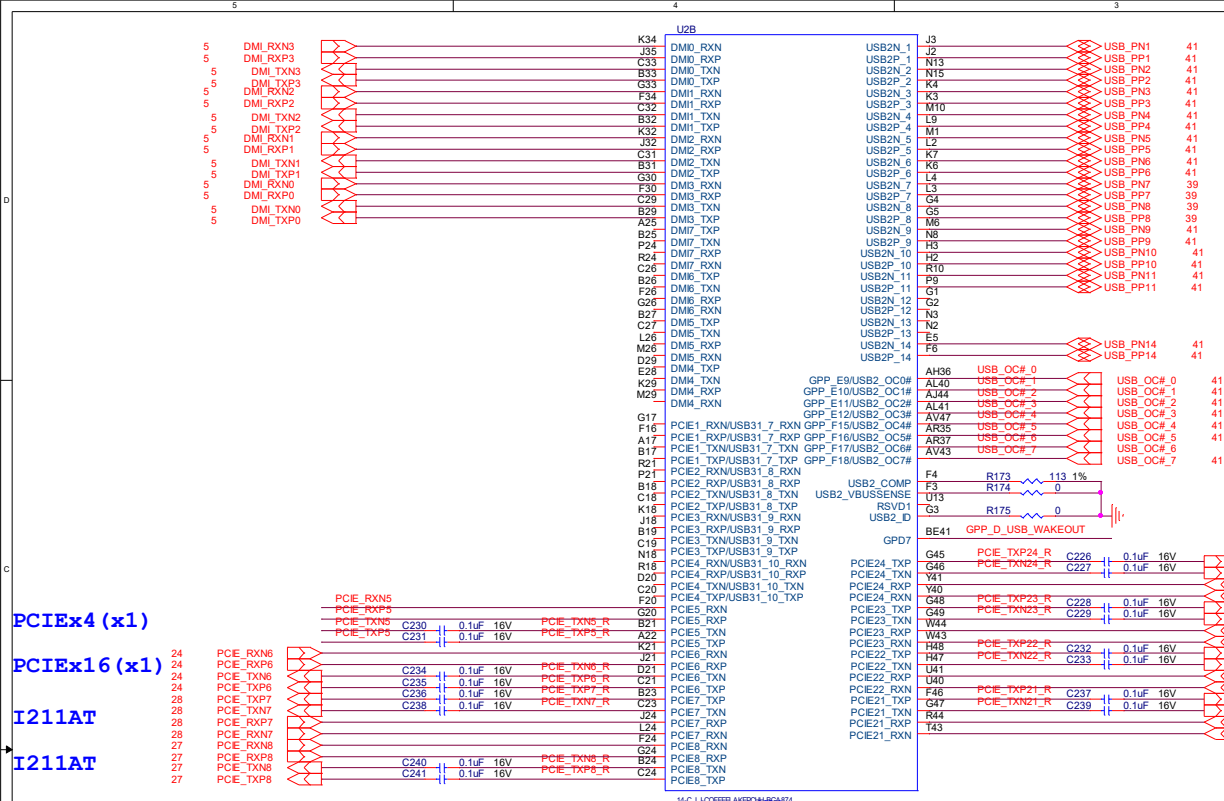
Document Number
PBA-CFL02

Rev:
A0.1

Date: Friday, February 21, 2020

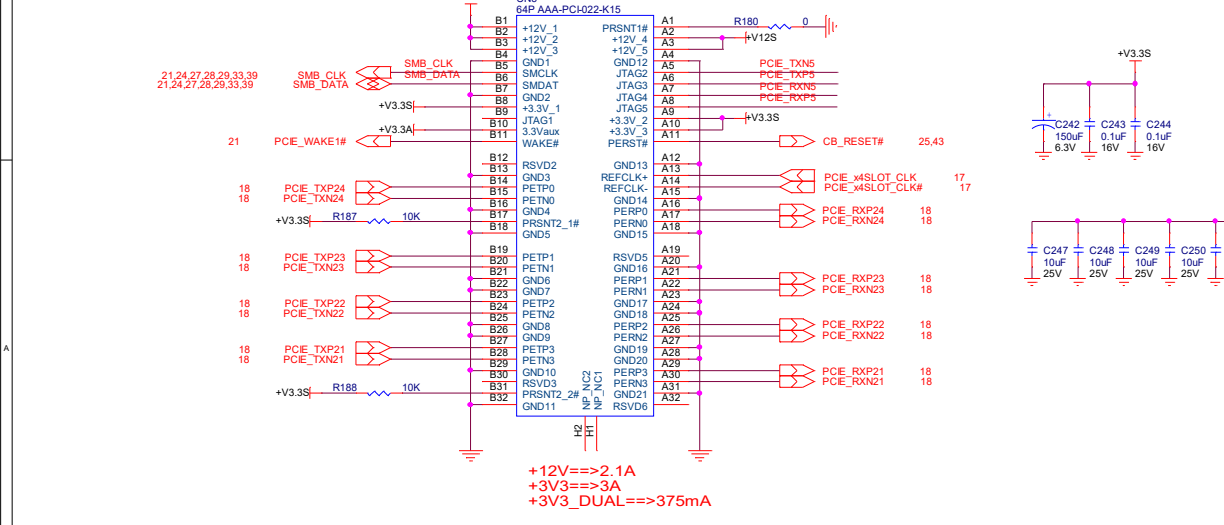
Sheet: 16 of 55





PCIEx4 (x1)
PCIEx16 (x1)
I211AT
I211AT

PCIE_SLOT_4

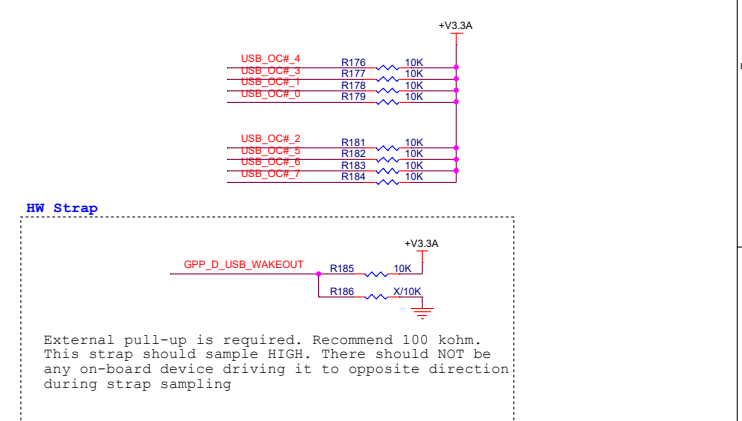


+12V==>2.1A
+3V3==>3A
+3V3_DUAL==>375mA



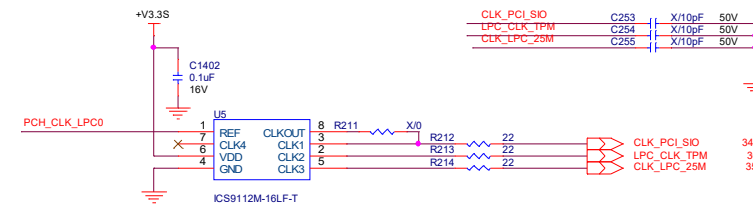
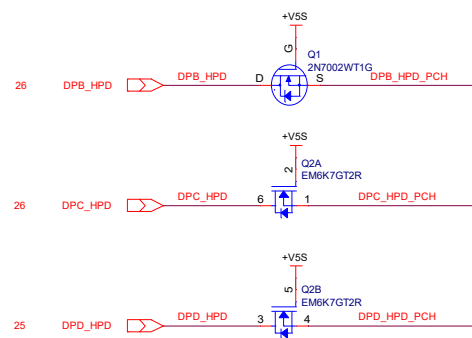
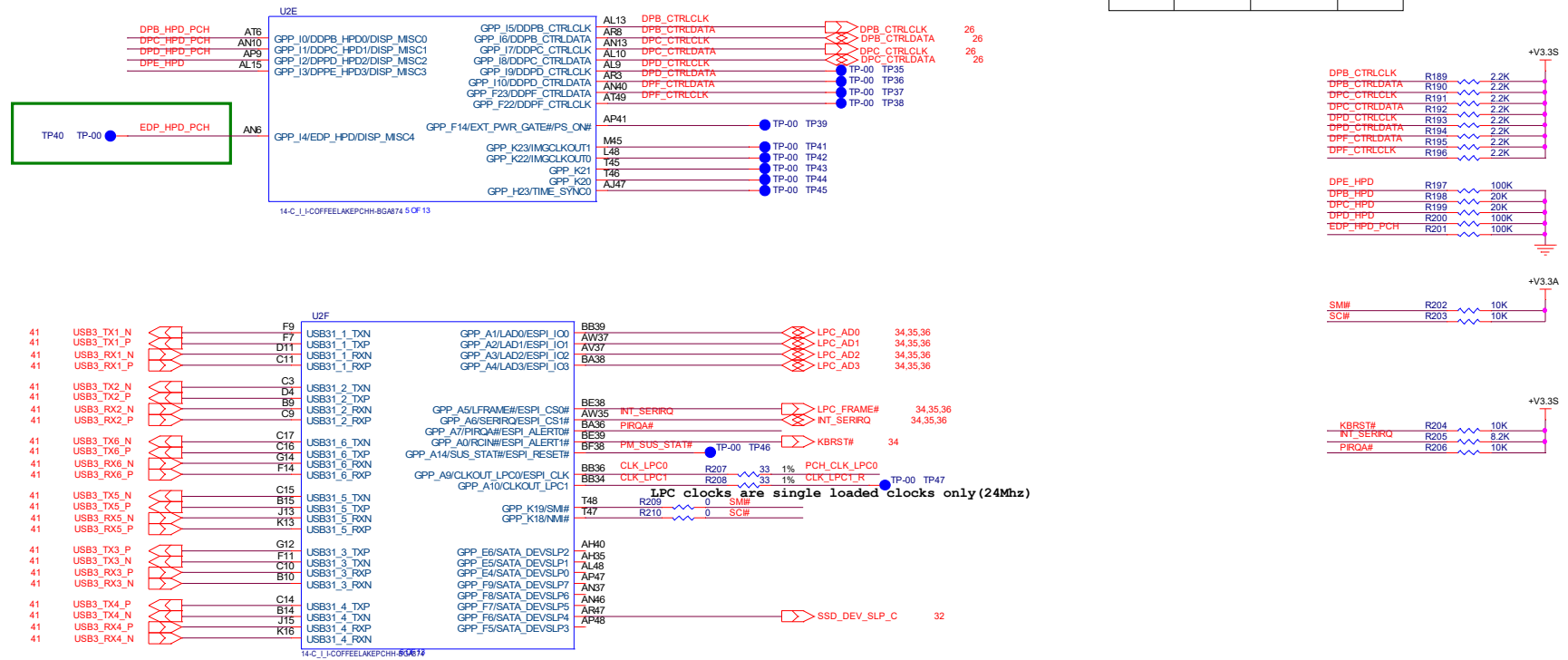
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|-------------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|---------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| High Speed I/O (HSIO) Type and Lane | USB3.1 Gen1/Lane 1 | USB3.1 Gen1/Lane 2 | USB3.1 Gen1/Lane 3 | USB3.1 Gen1/Lane 4 | USB3.1 Gen1/Lane 5 | USB3.1 Gen1/Lane 6 | USB3.1 Gen1/Lane 7 | USB3.1 Gen1/Lane 8 | USB3.1 Gen1/Lane 9 | USB3.1 Gen1/Lane 10 | PCIE# 5 | PCIE# 6 | PCIE# 7 | PCIE# 8 | PCIE# 9 | PCIE# 10 | PCIE# 11 | PCIE# 12 | PCIE# 13 | PCIE# 14 | PCIE# 15 | PCIE# 16 | PCIE# 17 | PCIE# 18 | PCIE# 19 | PCIE# 20 | PCIE# 21 | PCIE# 22 | PCIE# 23 | PCIE# 24 |
| Intel® RST Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support | No Support |

| CHIPSET SKU | Max USB 2.0 Nbr of Ports | USB 2.0 P1 | USB 2.0 P2 | USB 2.0 P3 | USB 2.0 P4 | USB 2.0 P5 | USB 2.0 P6 | USB 2.0 P7 | USB 2.0 P8 | USB 2.0 P9 | USB 2.0 P10 | USB 2.0 P11 | USB 2.0 P12 | USB 2.0 P13 | USB 2.0 P14 (or Intel® Wireless- AC) | USB1 | USB2 | |
|----------------|-----------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|--|------|------|--|
| Q370 | 14 | | | | | | | | | | | | | | | | | |
| H370 | 14 | | | | | | | | | | | | | | | | | |
| B360 | 12 | | | | | | | | | | | | | | | | | |
| H310 | 10 | | | | | | | | | | | | | | | | | |
| CM246 | 14 | | | | | | | | | | | | | | | | | |
| QM370 | 14 | | | | | | | | | | | | | | | | | |
| HM370 | 14 | | | | | | | | | | | | | | | | | |
| CM248 | 14 | | | | | | | | | | | | | | | | | |
| QM375 | 14 | | | | | | | | | | | | | | | | | |
| HM375 | 14 | | | | | | | | | | | | | | | | | |
| C242 | 12 | | | | | | | | | | | | | | | | | |
| C246 | 14 | | | | | | | | | | | | | | | | | |



| | | |
|--|-------------------------------------|---------------------|
| Title PCH 3-DMI/USB2.0/PCIE/USB3 | | |
| Size Custom | Document Number PBA-CFL02 | Rev: A0.1 |
| Date: Friday, February 21, 2020 | | Sheet: 18 of 55 |

| | | | |
|-------|-----------|------|----------|
| | HPD | DDC | DDI(CPU) |
| Port1 | DDPB_HPDP | DDCB | DDI1 |
| Port2 | DDPC_HPDP | DDCC | DDI2 |
| Port3 | DDPD_HPDP | DDCD | DDI3 |



| ID | Title | Author | Date | Status |
|----|--------------|----------|------------|-------------|
| 1 | Introduction | John Doe | 2023-01-01 | Completed |
| 2 | Chapter 1 | John Doe | 2023-01-05 | In Progress |
| 3 | Chapter 2 | John Doe | 2023-01-10 | Not Started |
| 4 | Chapter 3 | John Doe | 2023-01-15 | Not Started |
| 5 | Chapter 4 | John Doe | 2023-01-20 | Not Started |
| 6 | Chapter 5 | John Doe | 2023-01-25 | Not Started |
| 7 | Chapter 6 | John Doe | 2023-02-01 | Not Started |
| 8 | Chapter 7 | John Doe | 2023-02-05 | Not Started |
| 9 | Chapter 8 | John Doe | 2023-02-10 | Not Started |
| 10 | Chapter 9 | John Doe | 2023-02-15 | Not Started |
| 11 | Chapter 10 | John Doe | 2023-02-20 | Not Started |
| 12 | Chapter 11 | John Doe | 2023-02-25 | Not Started |
| 13 | Chapter 12 | John Doe | 2023-03-01 | Not Started |
| 14 | Chapter 13 | John Doe | 2023-03-05 | Not Started |
| 15 | Chapter 14 | John Doe | 2023-03-10 | Not Started |
| 16 | Chapter 15 | John Doe | 2023-03-15 | Not Started |
| 17 | Chapter 16 | John Doe | 2023-03-20 | Not Started |
| 18 | Chapter 17 | John Doe | 2023-03-25 | Not Started |
| 19 | Chapter 18 | John Doe | 2023-03-30 | Not Started |
| 20 | Chapter 19 | John Doe | 2023-04-01 | Not Started |
| 21 | Chapter 20 | John Doe | 2023-04-05 | Not Started |
| 22 | Chapter 21 | John Doe | 2023-04-10 | Not Started |
| 23 | Chapter 22 | John Doe | 2023-04-15 | Not Started |
| 24 | Chapter 23 | John Doe | 2023-04-20 | Not Started |
| 25 | Chapter 24 | John Doe | 2023-04-25 | Not Started |
| 26 | Chapter 25 | John Doe | 2023-04-30 | Not Started |
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PCH 4-DDI/USB3/LPC/eSPI

Size
A

Document Number
PBA-CFL02

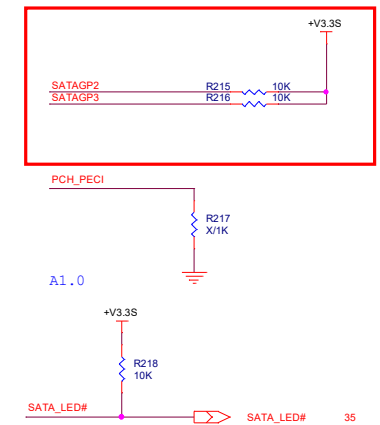
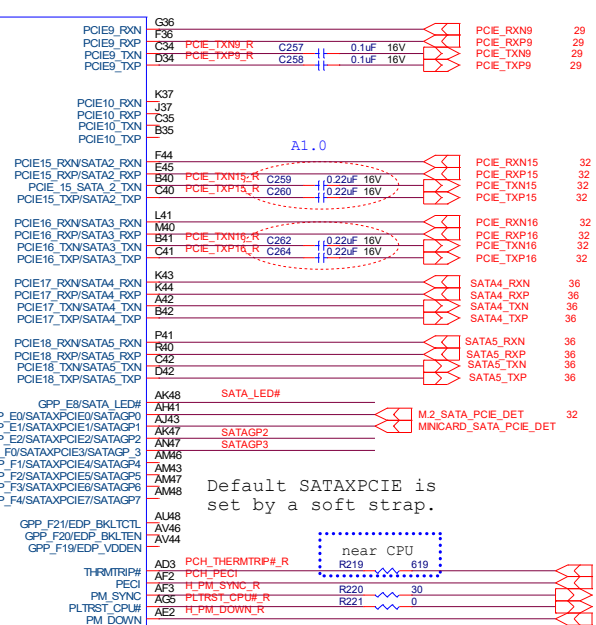
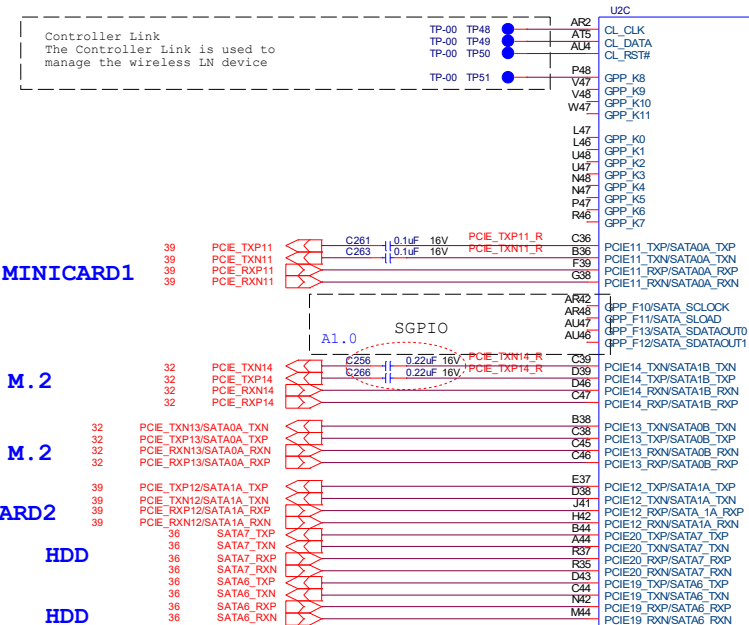
Rev:
A0.1Date: *Friday, February 21, 2020*

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Controller Link
The Controller Link is used to manage the wireless LN device

U2C

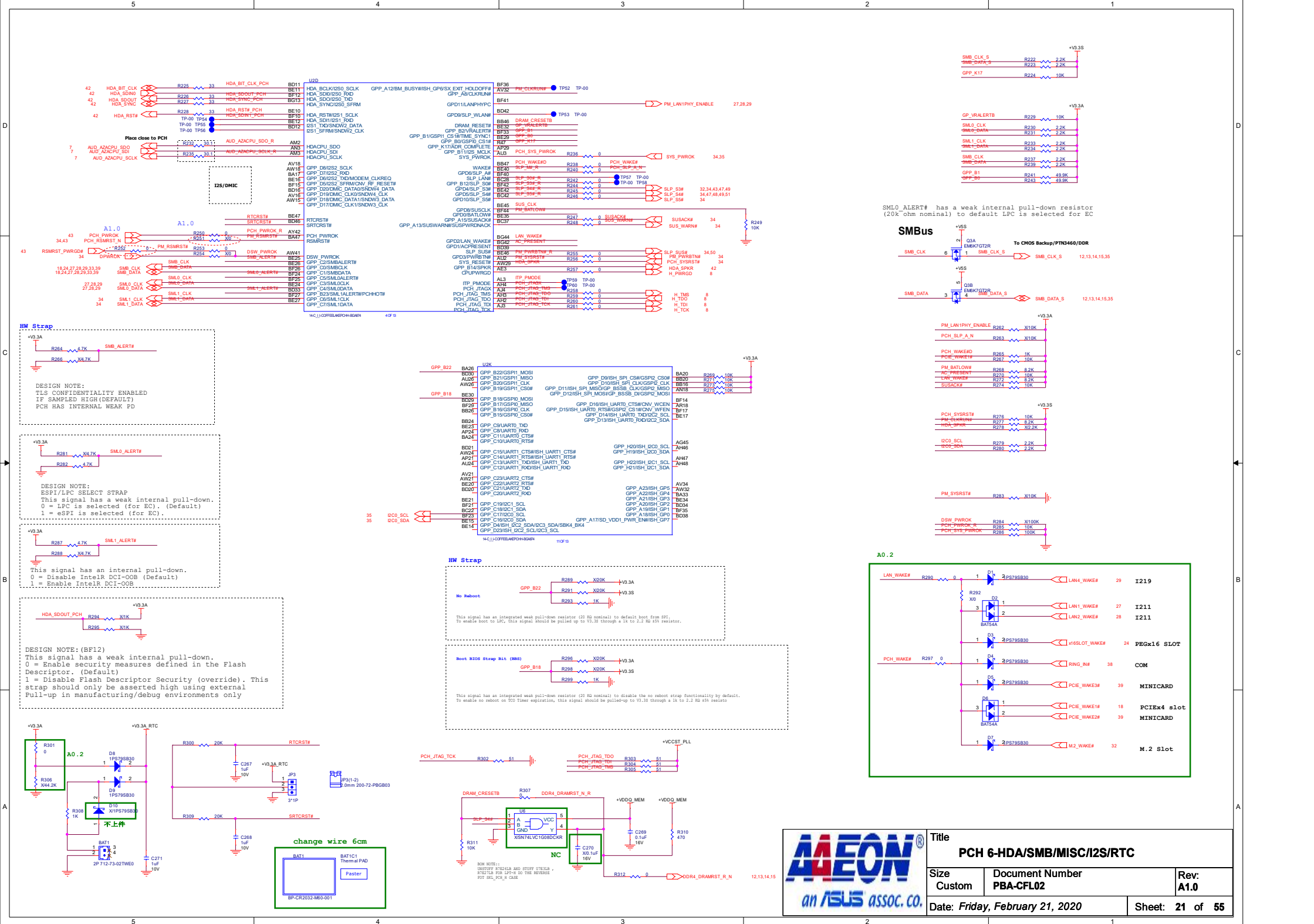
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| TP-00 | TP49 | AT5 |
| TP-00 | TP50 | AD4 |
| TP-00 | TP51 | P48 |
| | | V47 |
| | | CL_CLK |
| | | CL_DATA |
| | | CL_RST# |
| | | GPP_K8 |

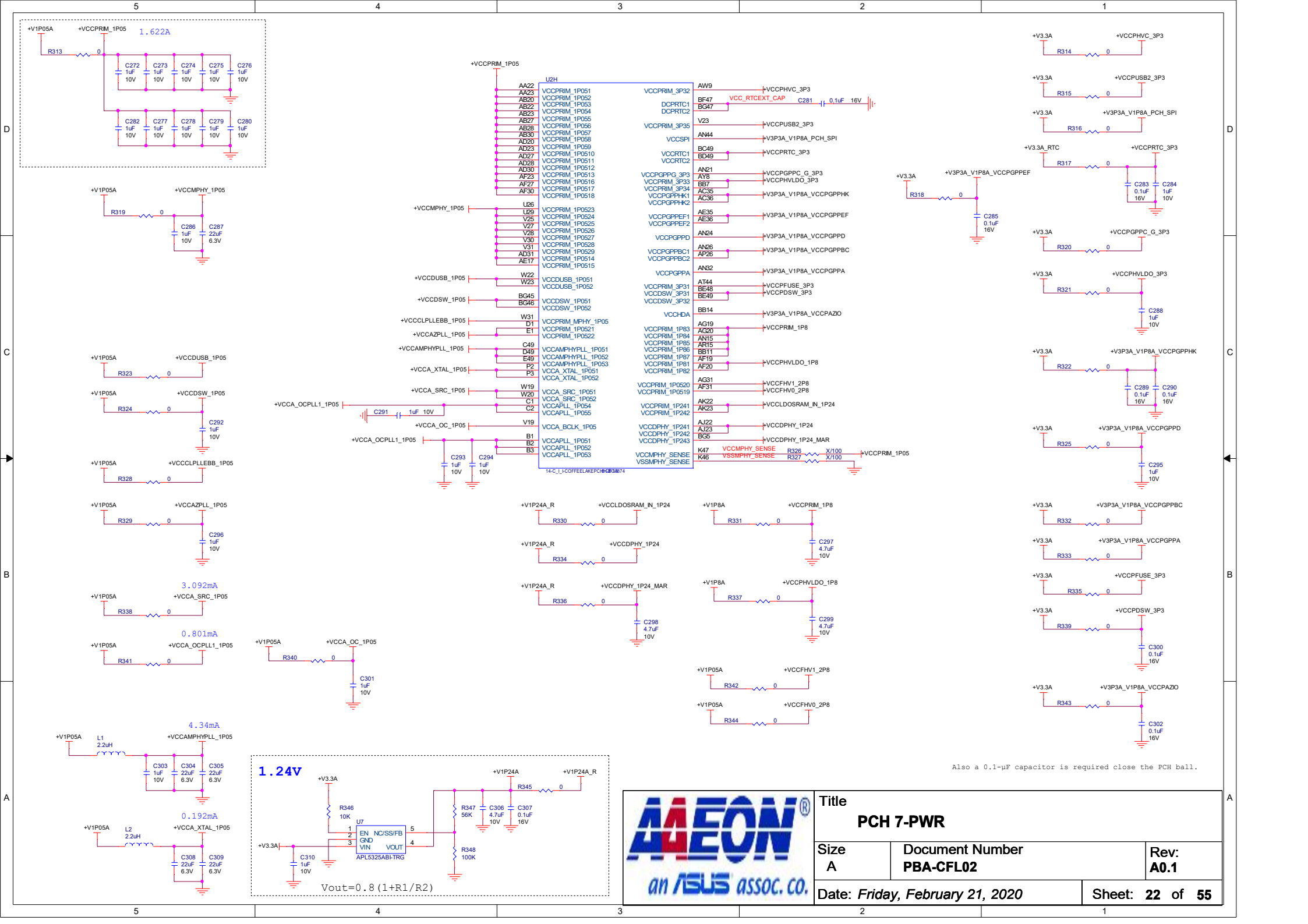


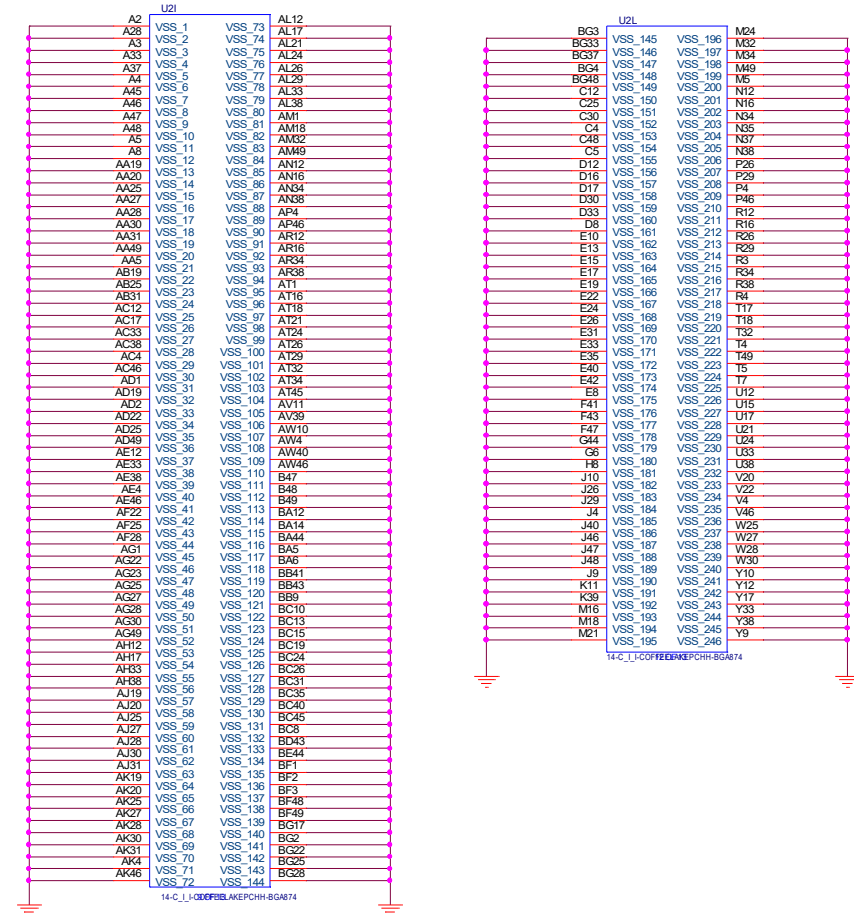
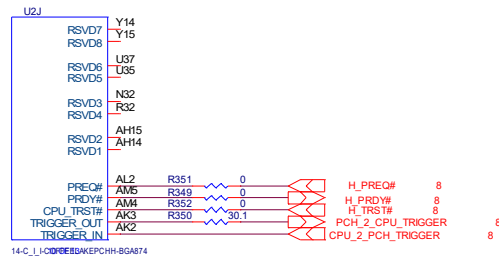
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|--------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|------------|--------|--------|--------|------------------------------|---------|---------|---------|------------|---------|---------|---------|------------------------------|---------|---------|---------|------------------------------|---------|---------|---------|---------|
| | | | | | | | PCIE#1 | PCIE#2 | PCIE#3 | PCIE#4 | GbE | | | | GbE | | SATA_0a | SATA_1a | SATA_0b | SATA_1b | SATA2 | SATA3 | SATA4 | SATA5 | SATA6 | SATA7 | | | | | |
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | |
| H310 | USB3.1 GEN1 | USB3.1 GEN1 | USB3.1 GEN1 | USB3.1 GEN1 | NA | NA | NA | NA | NA | NA | PCIE-5 | PCIE-6 | PCIE-7 | PCIE-8 | GbE | N/A | PCIE-11 | PCIE-12 | SATA_0b | SATA_1b | SATA2 | SATA3 | N/A | N/A | NA | NA | N/A | N/A | N/A | N/A | |
| | | | | | | | | | | | GbE | | | | | | | GbE | GbE | | | | | | | | | | | | |
| Q370 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1 | USB3.1 GEN1 | USB3.1 GEN1 | USB3.1 GEN1 | PCIE-5 | PCIE-6 | PCIE-7 | PCIE-8 | PCIE-9 | PCIE-10 | PCIE-11 | PCIE-12 | PCIE-13 | PCIE-14 | PCIE-15 | PCIE-16 | PCIE-17 | PCIE-18 | | PCIE-19 | PCIE-20 | PCIE-21 | PCIE-22 | PCIE-23 | PCIE-24 |
| | | | | | | | PCIE#1 | PCIE#2 | PCIE#3 | PCIE#4 | GbE | | | | GbE | | SATA_0a | SATA_1a | SATA_0b | SATA_1b | SATA2 | SATA3 | SATA4 | SATA5 | | PCIE-19 | PCIE-20 | PCIE-21 | PCIE-22 | PCIE-23 | PCIE-24 |
| H370 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1 | USB3.1 GEN1 | USB3.1 GEN1 | USB3.1 GEN1 | PCIE#3 | PCIE#4 | PCIE-5 | PCIE-6 | PCIE-7 | PCIE-8 | PCIE-9 | PCIE-10 | PCIE-11 | PCIE-12 | PCIE-13 | PCIE-14 | PCIE-15 | PCIE-16 | | SATA4 | SATA5 | PCIE-19 | PCIE-20 | PCIE-21 | PCIE-22 | PCIE-23 | PCIE-24 |
| | | | | | | | | | | | GbE | | | | GbE | | SATA_0a | SATA_1a | SATA_0b | SATA_1b | SATA2 | SATA3 | | | PCIE-19 | PCIE-20 | PCIE-21 | PCIE-22 | PCIE-23 | PCIE-24 | |
| C246 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | USB3.1 GEN1/2 | PCIE-5 | PCIE-6 | PCIE-7 | PCIE-8 | PCIE-9 | PCIE-10 | PCIE-11 | PCIE-12 | PCIE-13 | PCIE-14 | PCIE-15 | PCIE-16 | PCIE-17 | PCIE-18 | PCIE-19 | PCIE-20 | | PCIE-21 | PCIE-22 | PCIE-23 | PCIE-24 |
| | | | | | | | PCIE#1 | PCIE#2 | PCIE#3 | PCIE#4 | GbE | | | | GbE | | SATA_0a | SATA_1a | SATA_0b | SATA_1b | SATA2 | SATA3 | SATA4 | SATA5 | SATA6 | SATA7 | PCIE-21 | PCIE-22 | PCIE-23 | PCIE-24 | |
| PCIe by 4 | | | | | | | X4 | | | | X4 | | | | X4 | | | | X4 | | | | X4 | | | | X4 | | | | |
| PCIe by 2 | | | | | | | X2 | | | | X2 | | | | X2 | | | | X2 | | | | X2 | | | | X2 | | | | |
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| Title |
|-------|
|-------|

PCH 8-VSS

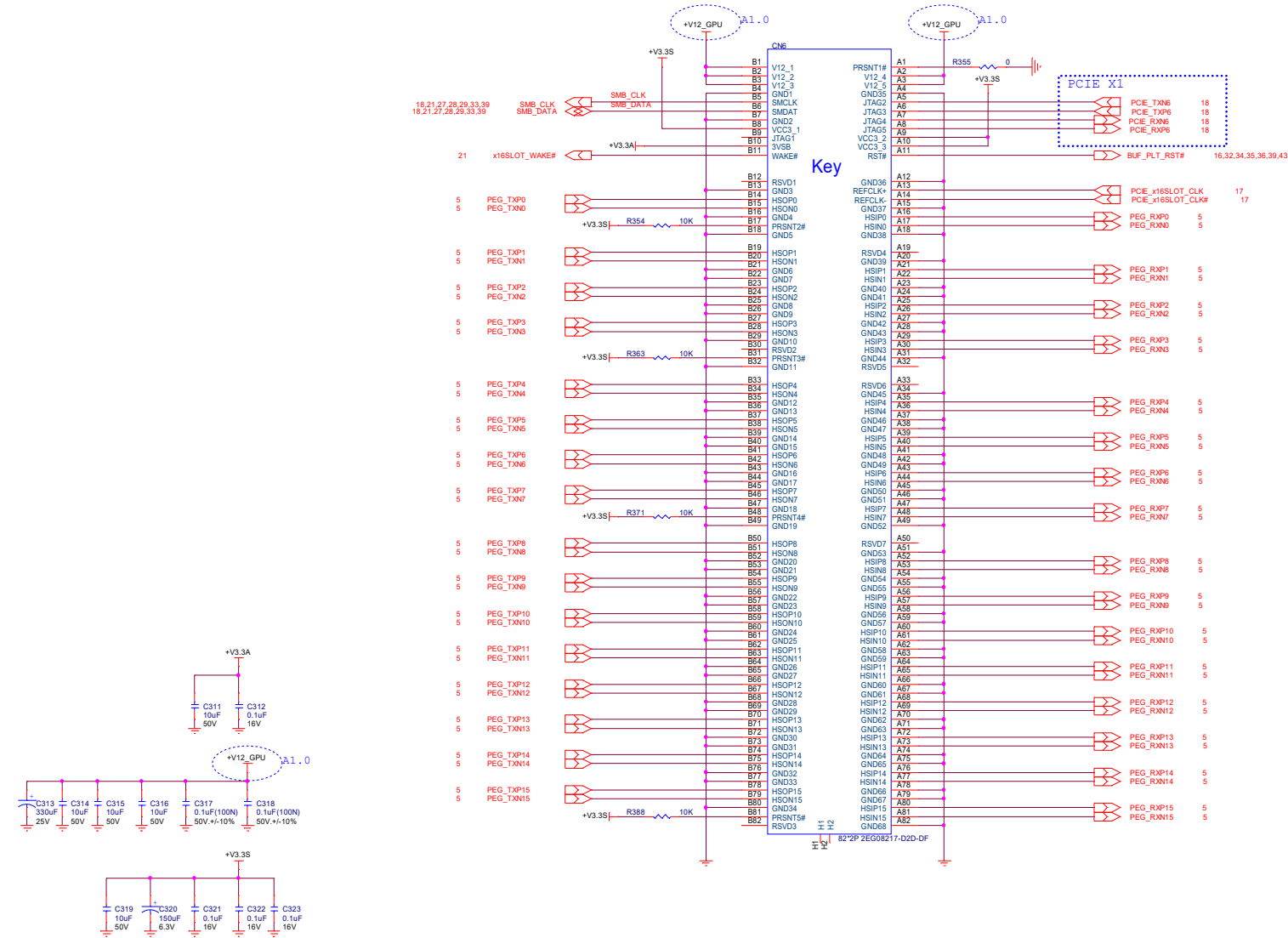
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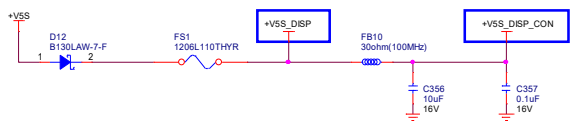
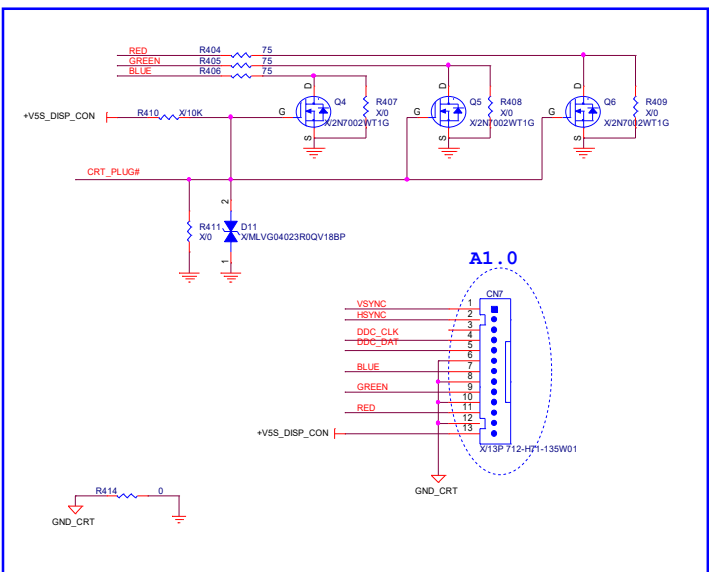
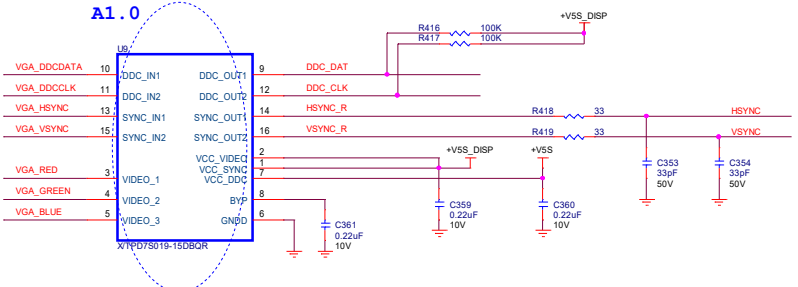
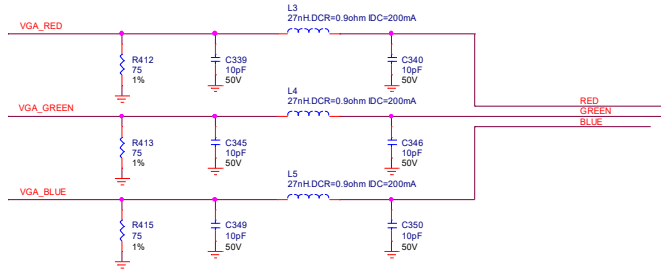
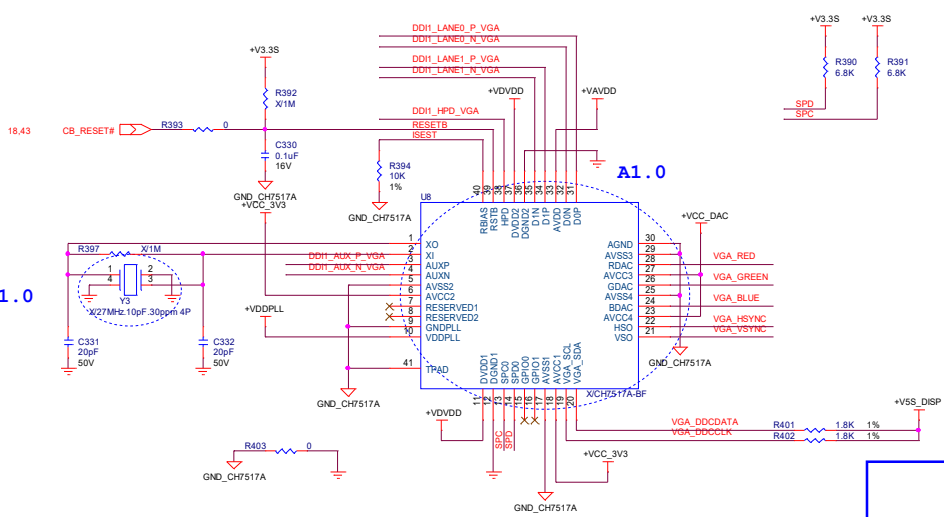
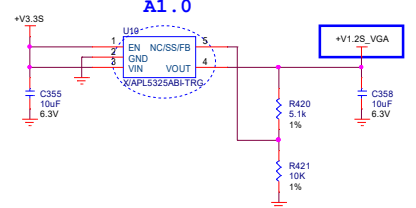
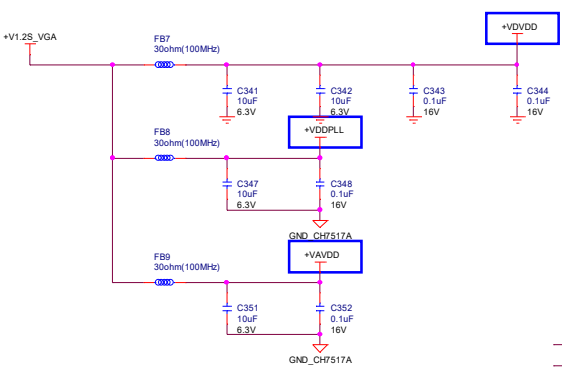
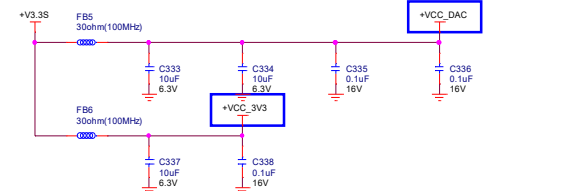
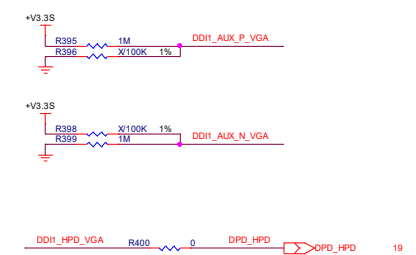
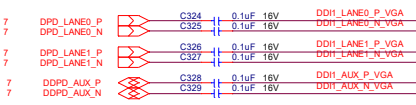
Document Number
PBA-CFL02

Rev:
A0.1

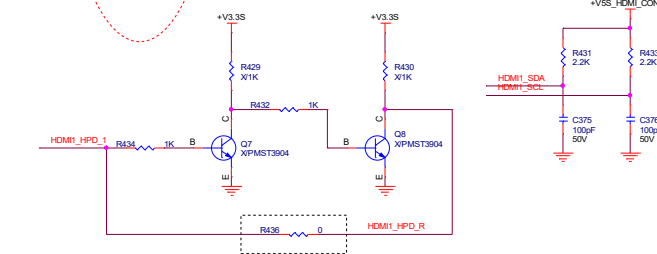
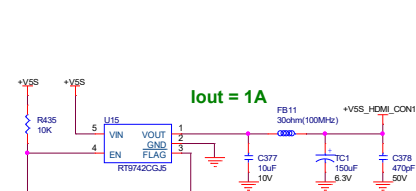
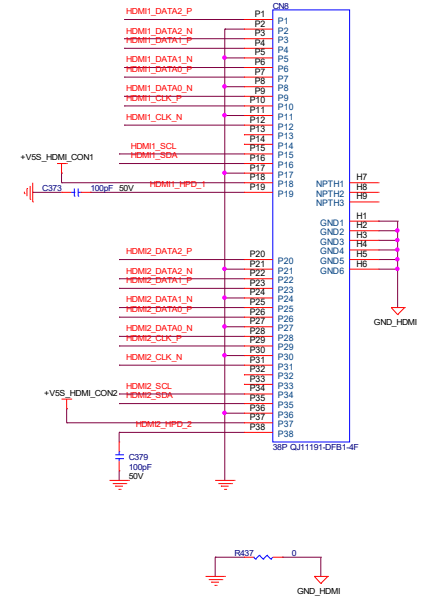
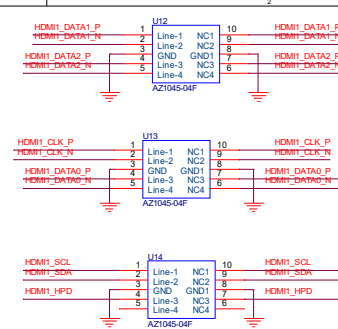
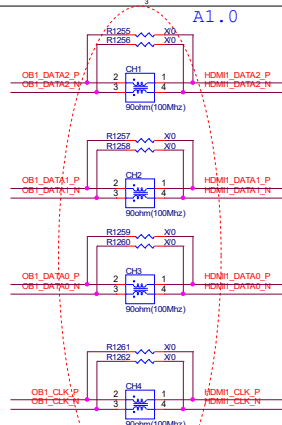
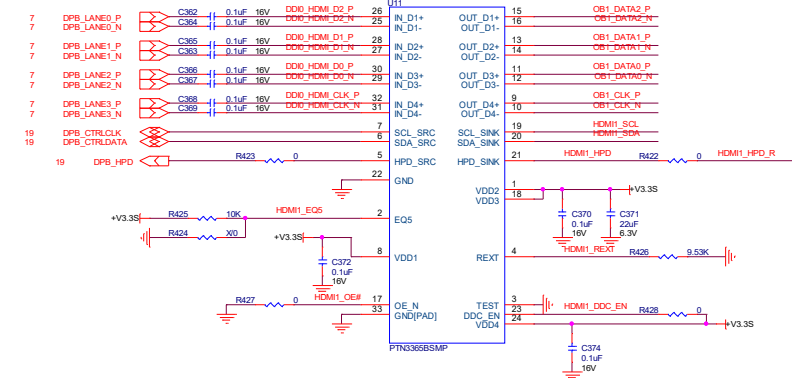
Date: *Friday, February 21, 2020*

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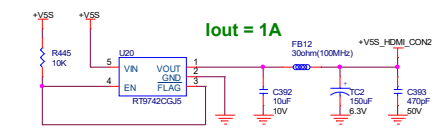
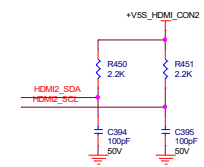
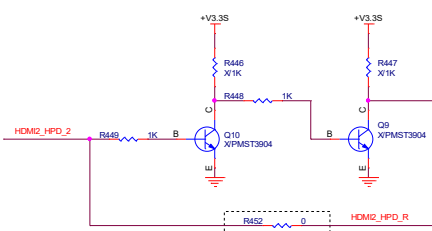
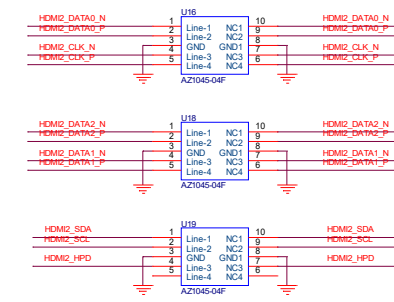
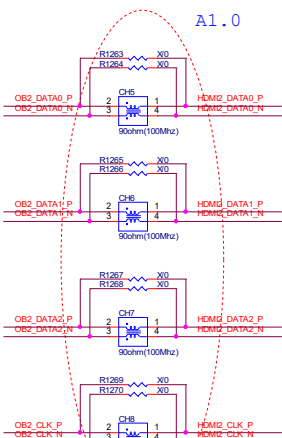
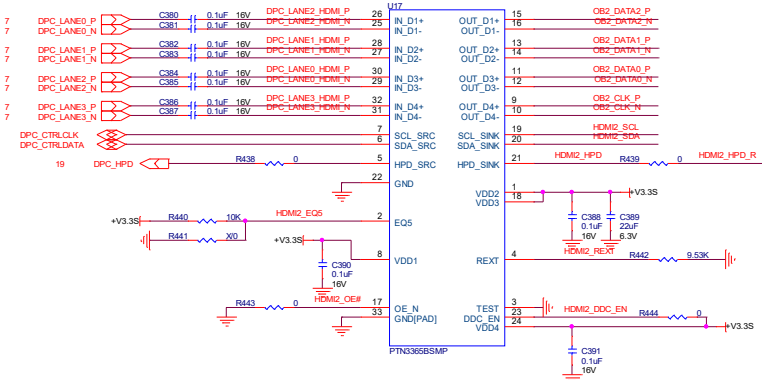




HDMI 1

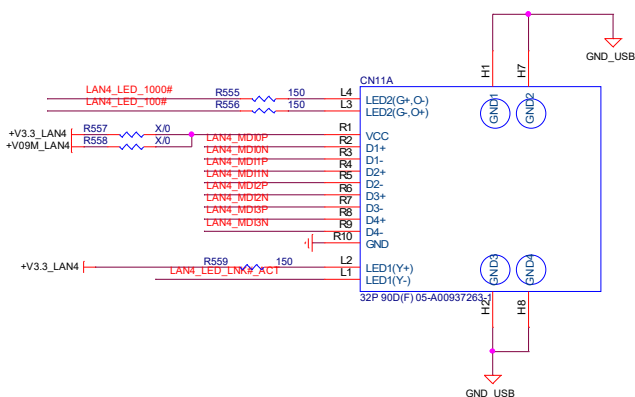
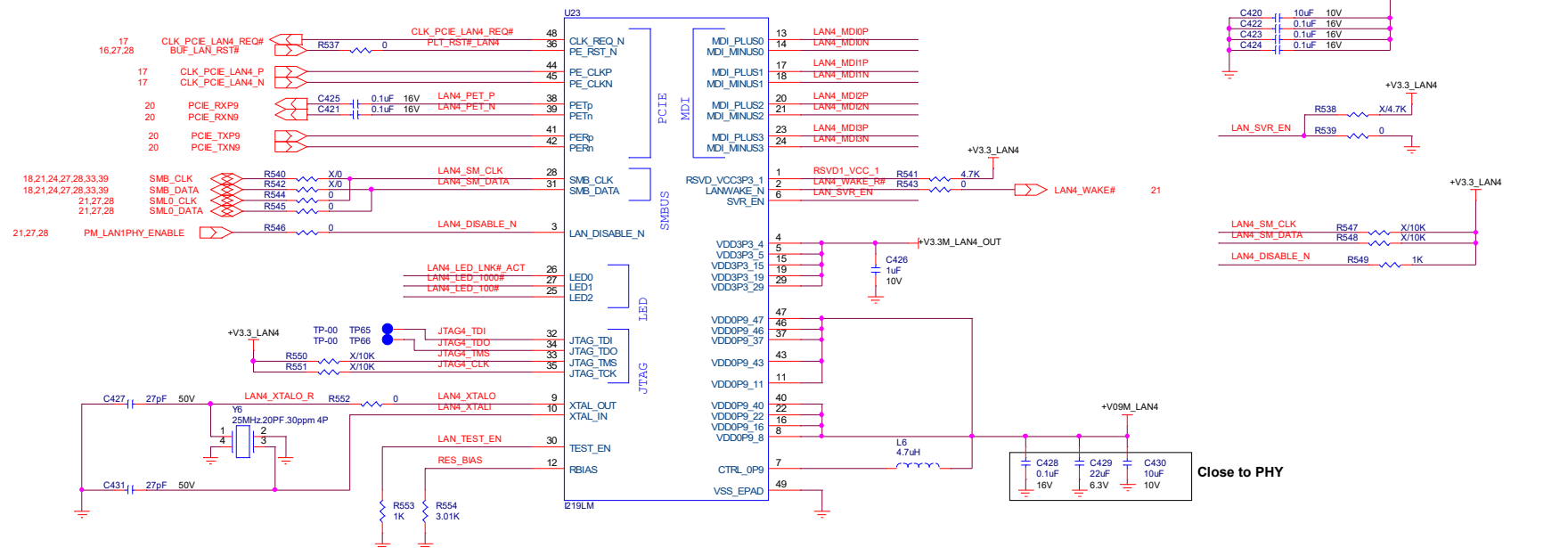


HDMI2



| Inputs | Quinary notation | Equalizer mode |
|-----------------------------------|------------------|----------------|
| EQ5 | | |
| short to GND | 0 ₅ | 0 dB |
| 10 kΩ resistor to GND | 1 ₅ | 2 dB |
| open-circuit | 2 ₅ | 3.5 dB |
| 10 kΩ resistor to V _{DD} | 3 ₅ | 9 dB |
| short to V _{DD} | 4 ₅ | 7 dB |

WGI219LM



ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY

SPEED LED
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps

| LEDs | Mode | Function |
|------|------|---------------|
| LED0 | 0100 | LINK/ACTIVITY |
| LED1 | 0111 | LINK 1000 |
| LED2 | 0110 | LINK 100 |



| | | |
|---------------------------------|-------------------------------------|---------------------|
| Title LAN WGI219LM | | |
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| Date: Friday, February 21, 2020 | | Sheet: 29 of 55 |

D

C

B

A

D

C

B

A



| ID | Title |
|----|--------------|
| 1 | Introduction |
| 2 | Background |
| 3 | Methodology |
| 4 | Results |
| 5 | Conclusion |

Back up

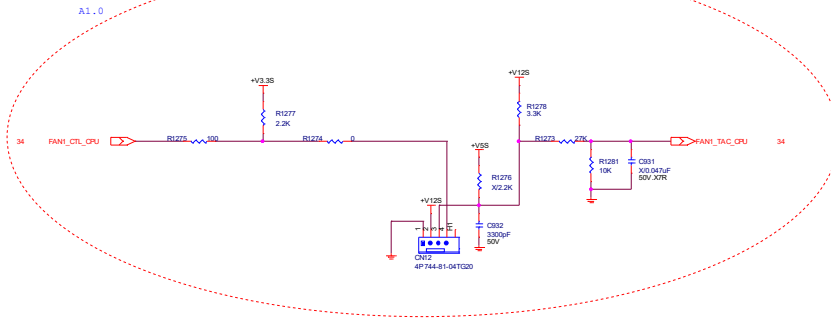
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|------|---|
| Size | A |
|------|---|

Document Number
PBA-CFL02

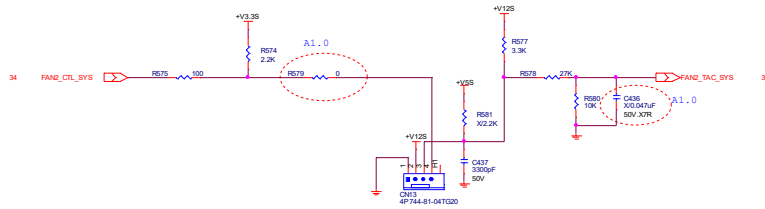
Rev:
A0.1Date: *Friday, February 21, 2020*

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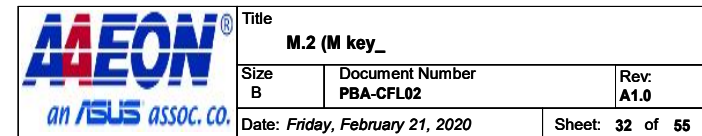
CPU FAN (FAN1)

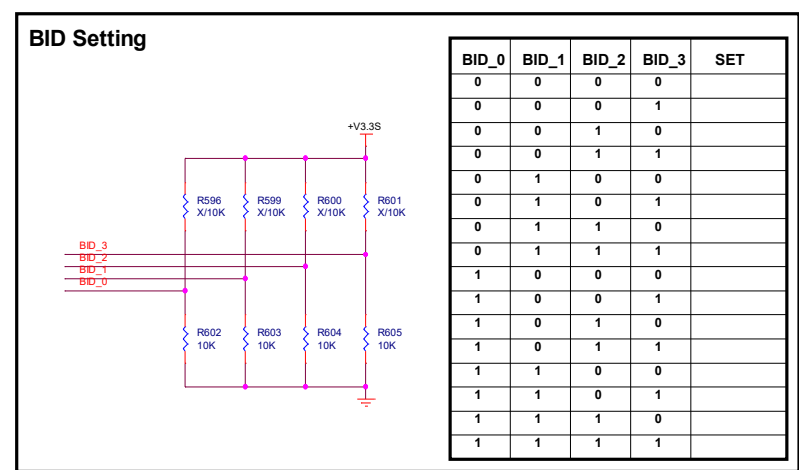
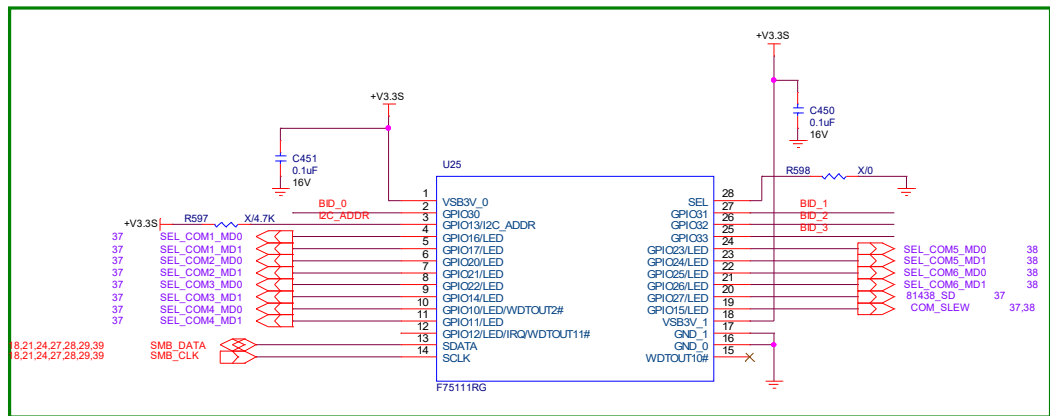


SYS FAN (FAN2)

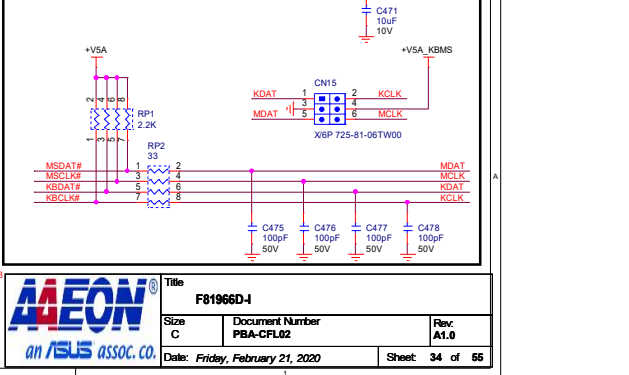
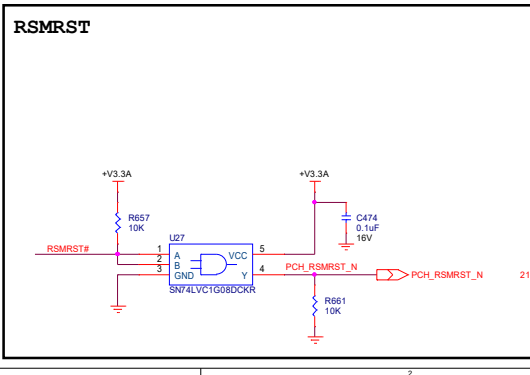
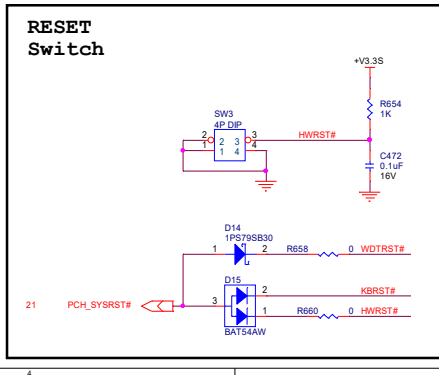
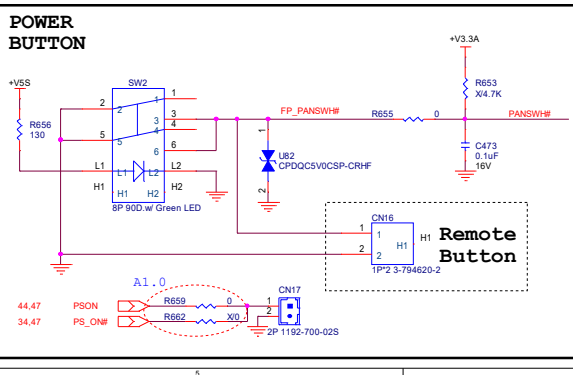
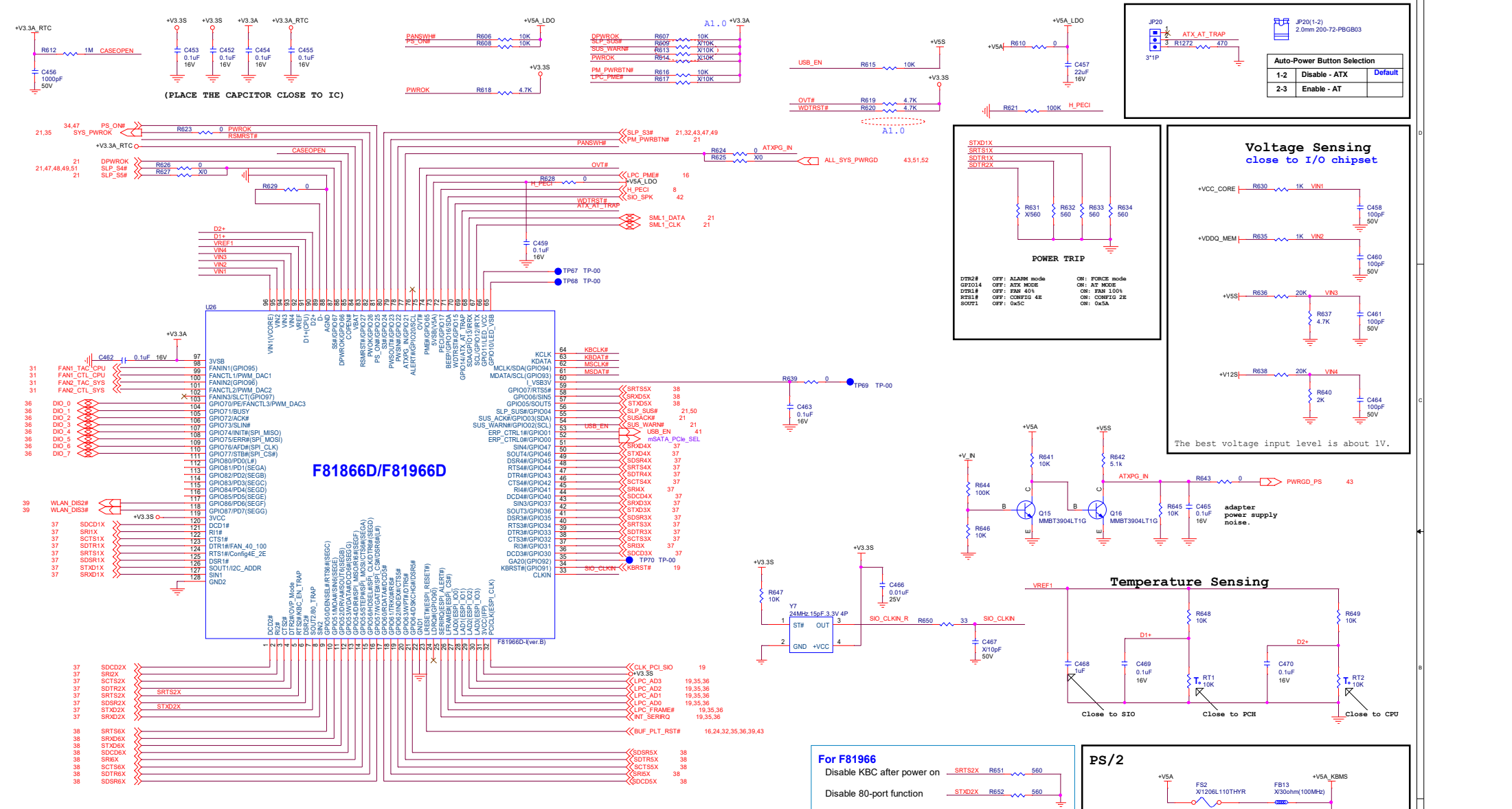


| | | |
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| Title Backup | | |
| Size B | Document Number PBA-CFL02 | Rev. A1.0 |
| Date: Friday, February 21, 2020 | | Sheet: 31 of 55 |

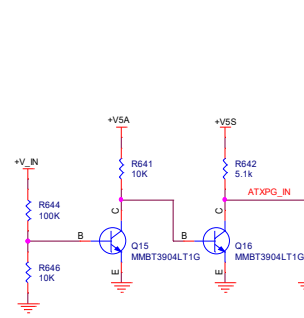
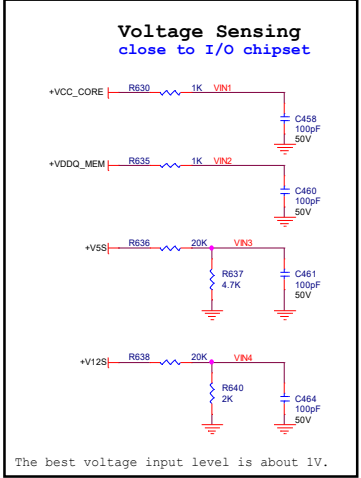
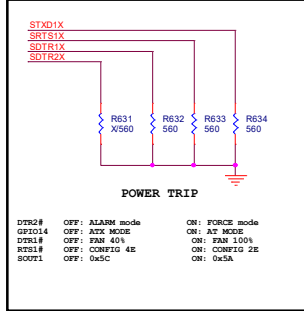




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| Size A | Document Number PBA-CFL02 | Rev: A0.1 |
| Date: <i>Friday, February 21, 2020</i> | | Sheet: 33 of 55 |

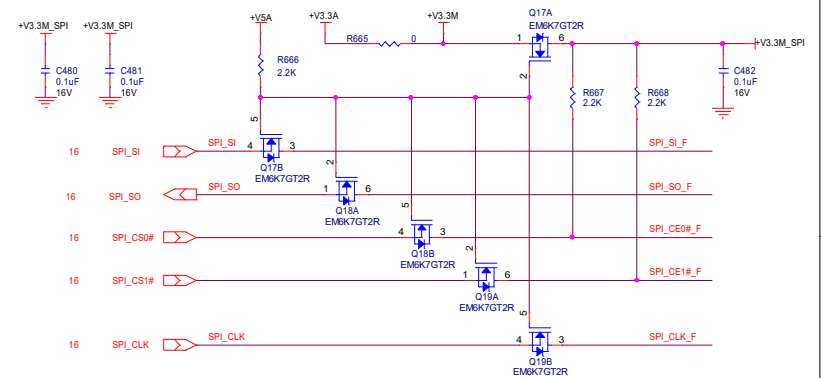
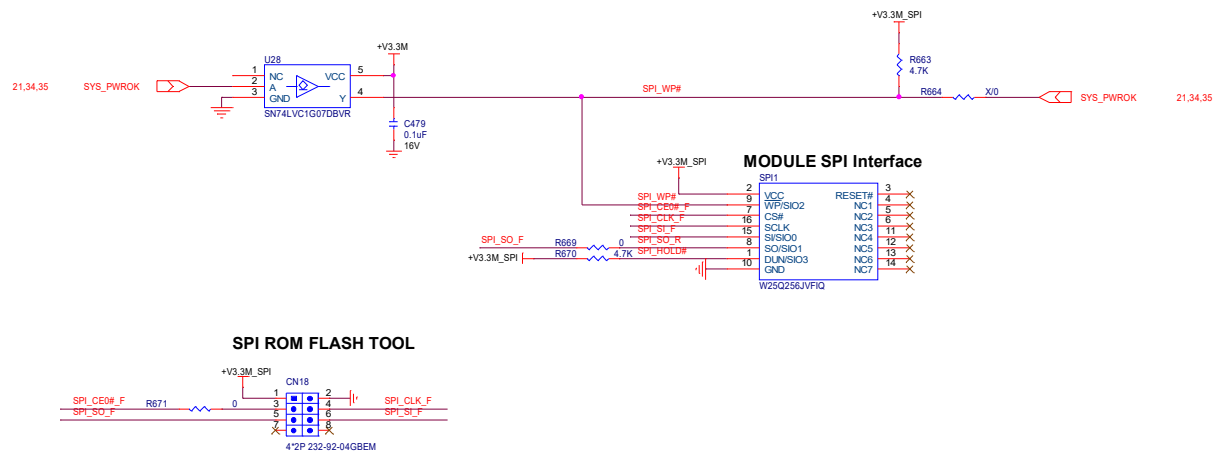


| Auto-Power Button Selection | | |
|-----------------------------|---------------|---------|
| 1-2 | Disable - ATX | Default |
| 2-3 | Enable - AT | |

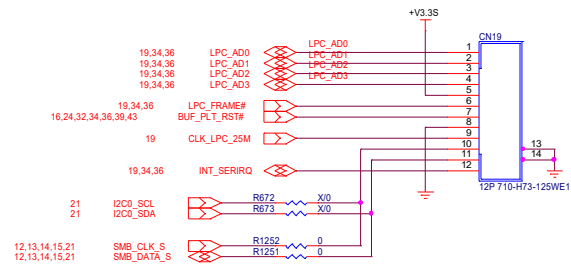


For F81966
Disable KBC after power on SRTS2X R651 560
Disable 80-port function STXD2X R652 560

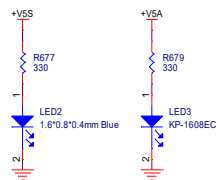
SPI ROM



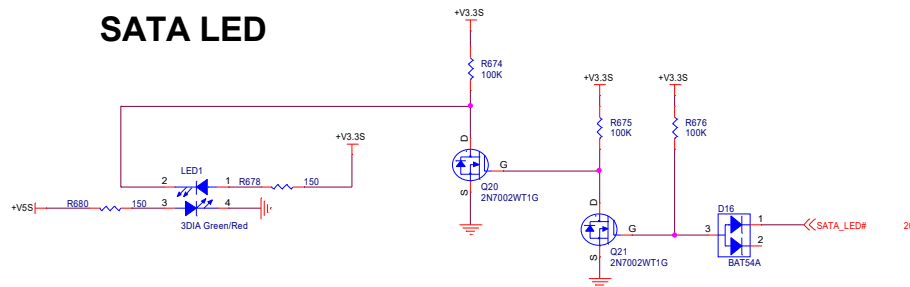
LPC CONN for Debug



POWER LED

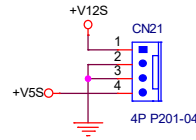
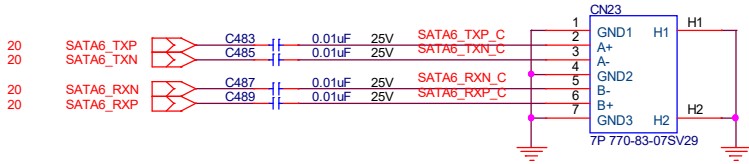


SATA LED

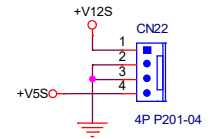
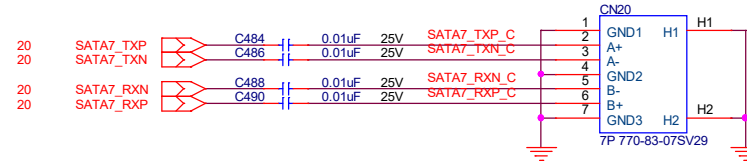


| | | |
|--|-------------------------------------|-------------------------------|
| Title | | |
| SPI_ROM / LED | | |
| Size Custom | Document Number PBA-CFL02 | Rev: A0.1 |
| Date: <i>Friday, February 21, 2020</i> | | Sheet: 35 of 55 |

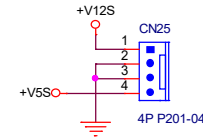
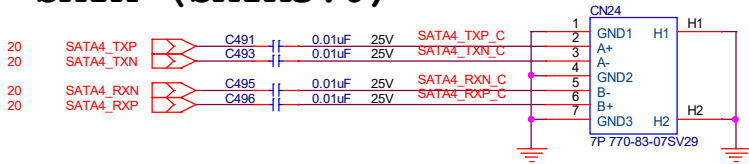
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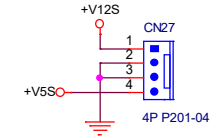
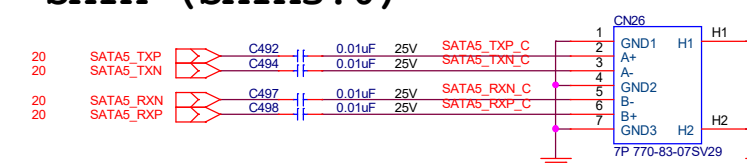
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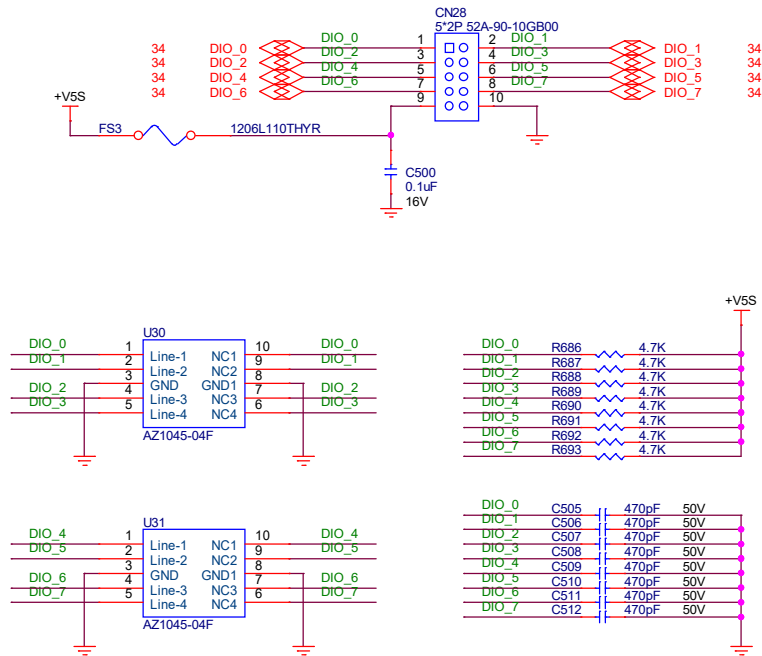
SATA (SATA3.0)



SATA (SATA3.0)

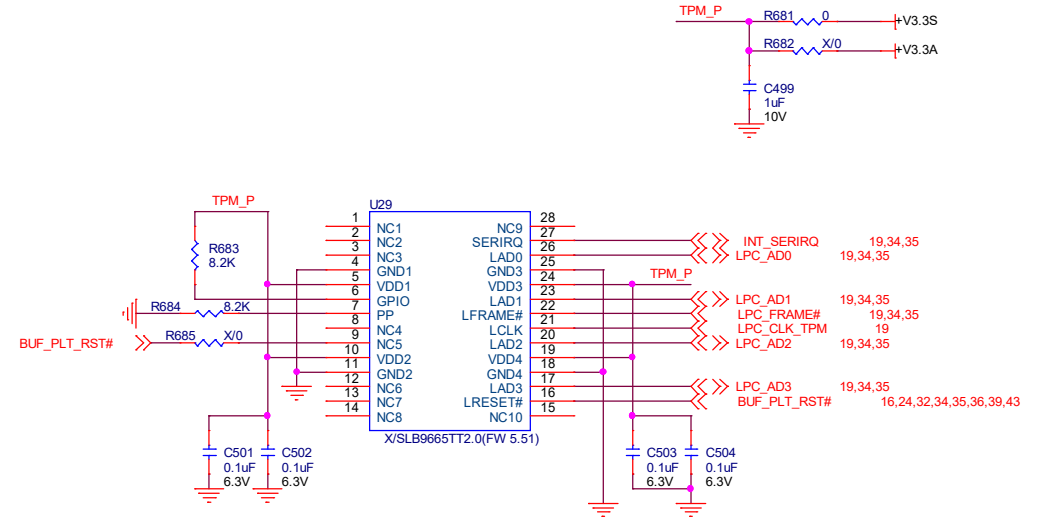


DIO

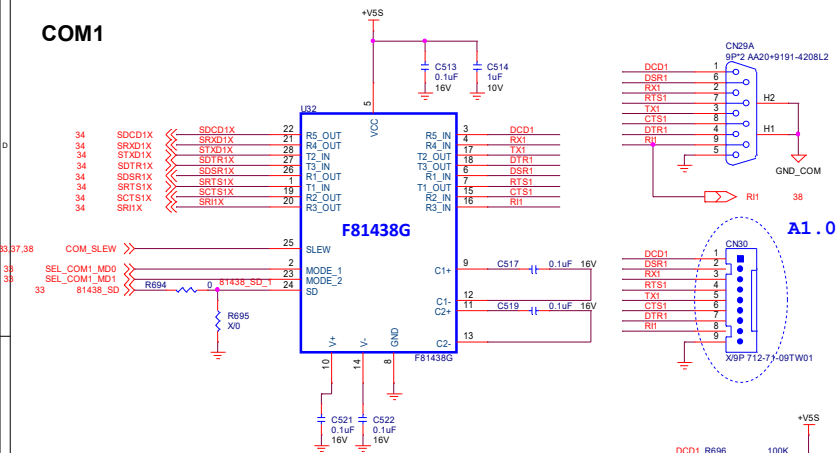


TPM

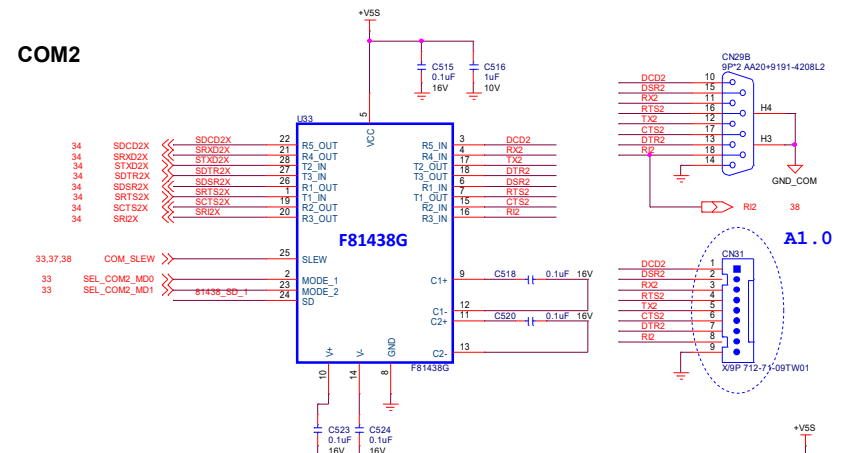
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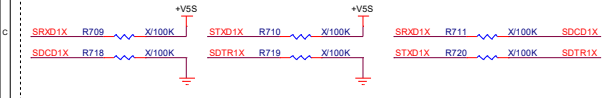
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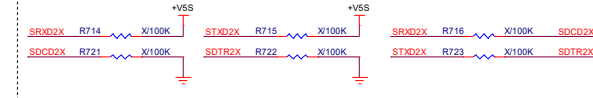
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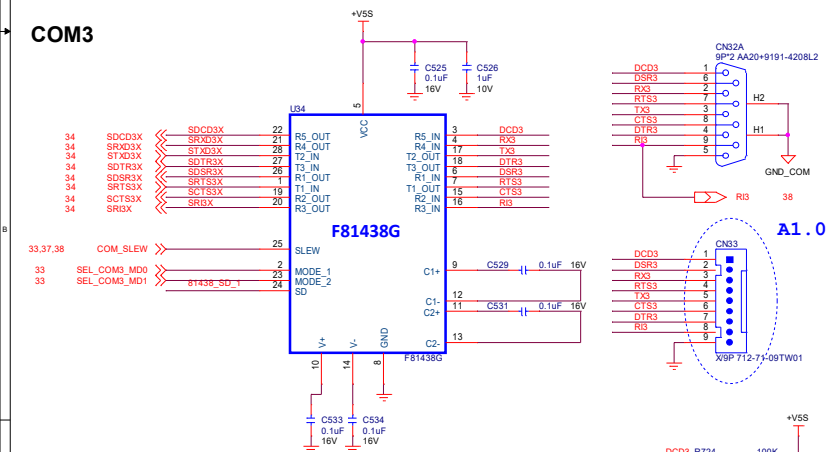
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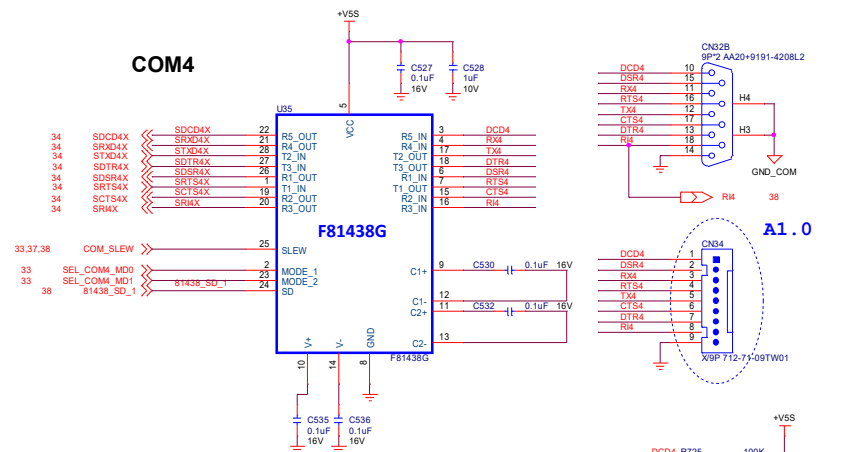
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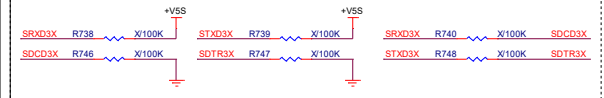
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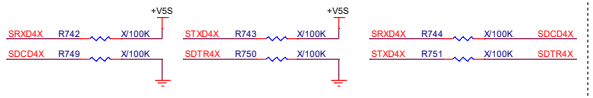
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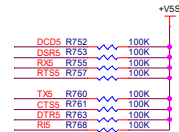
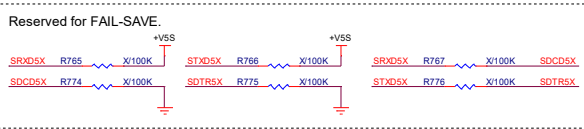
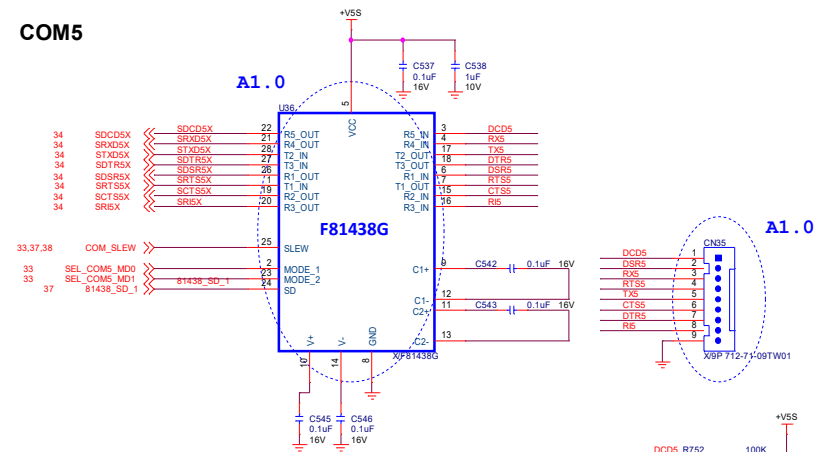
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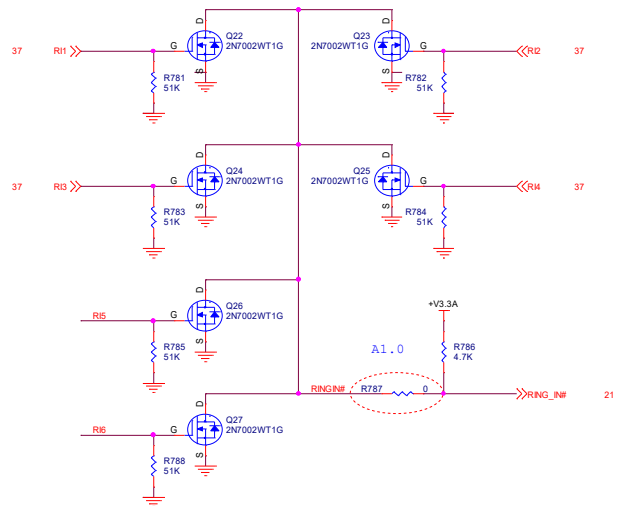
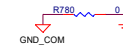
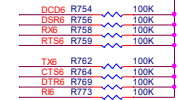
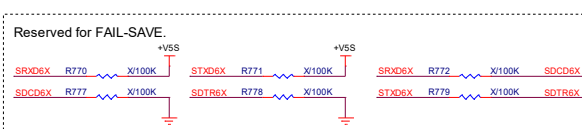
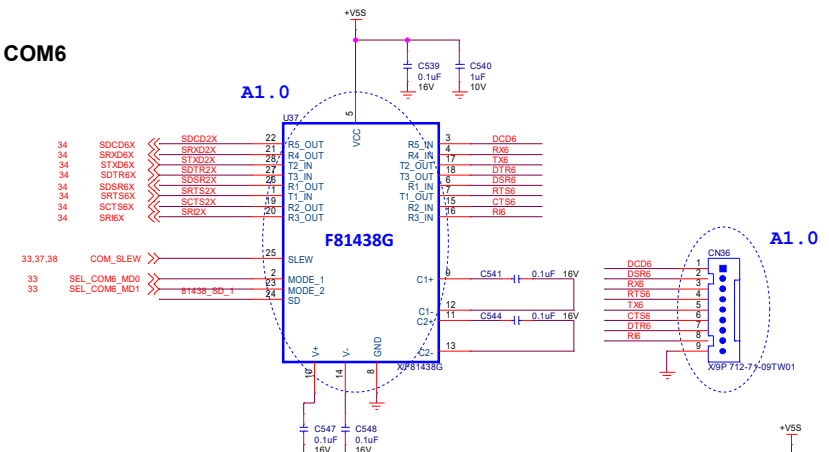
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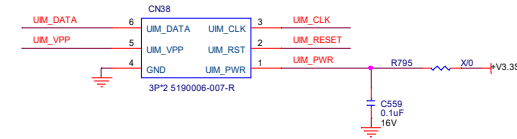
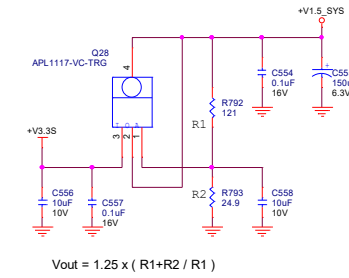
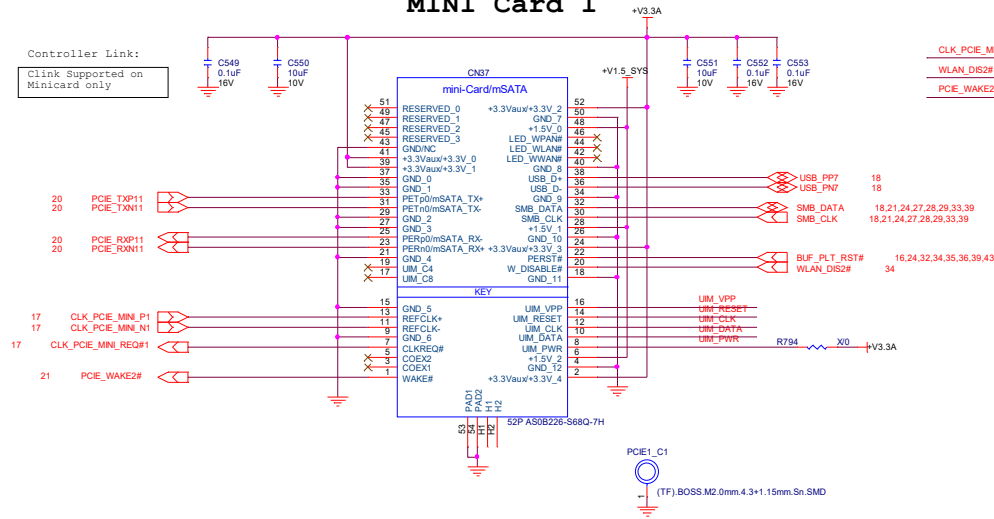
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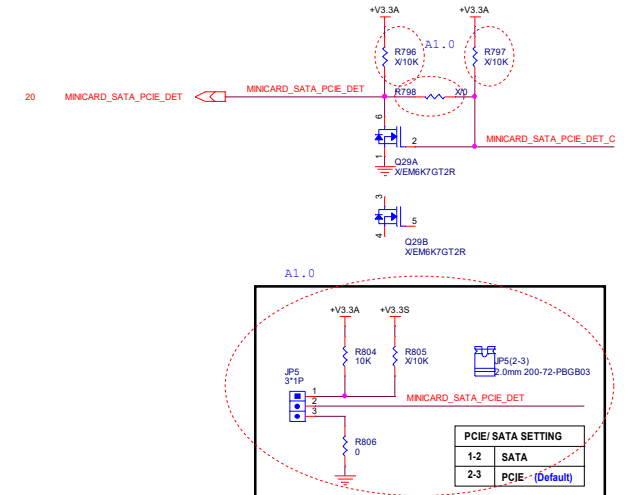
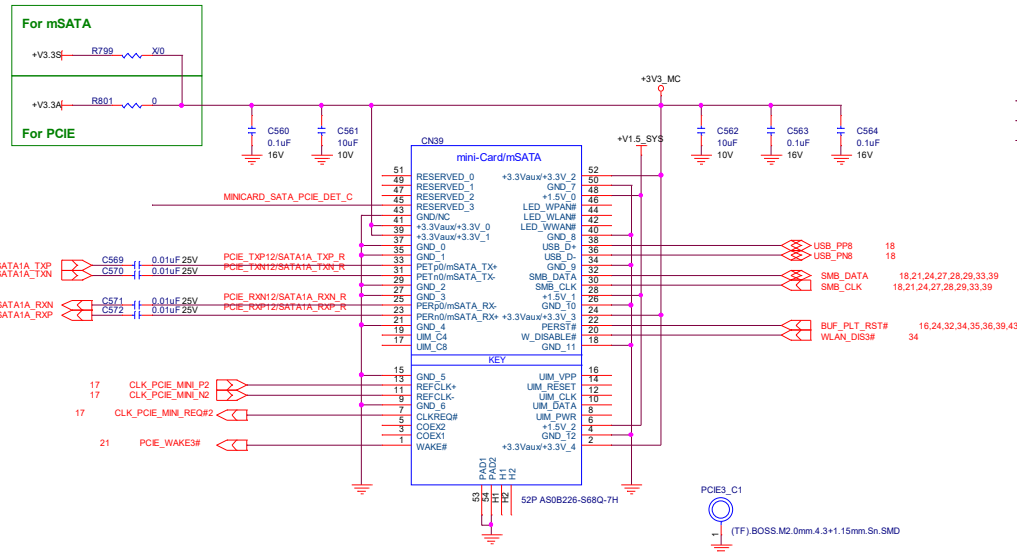
COM6

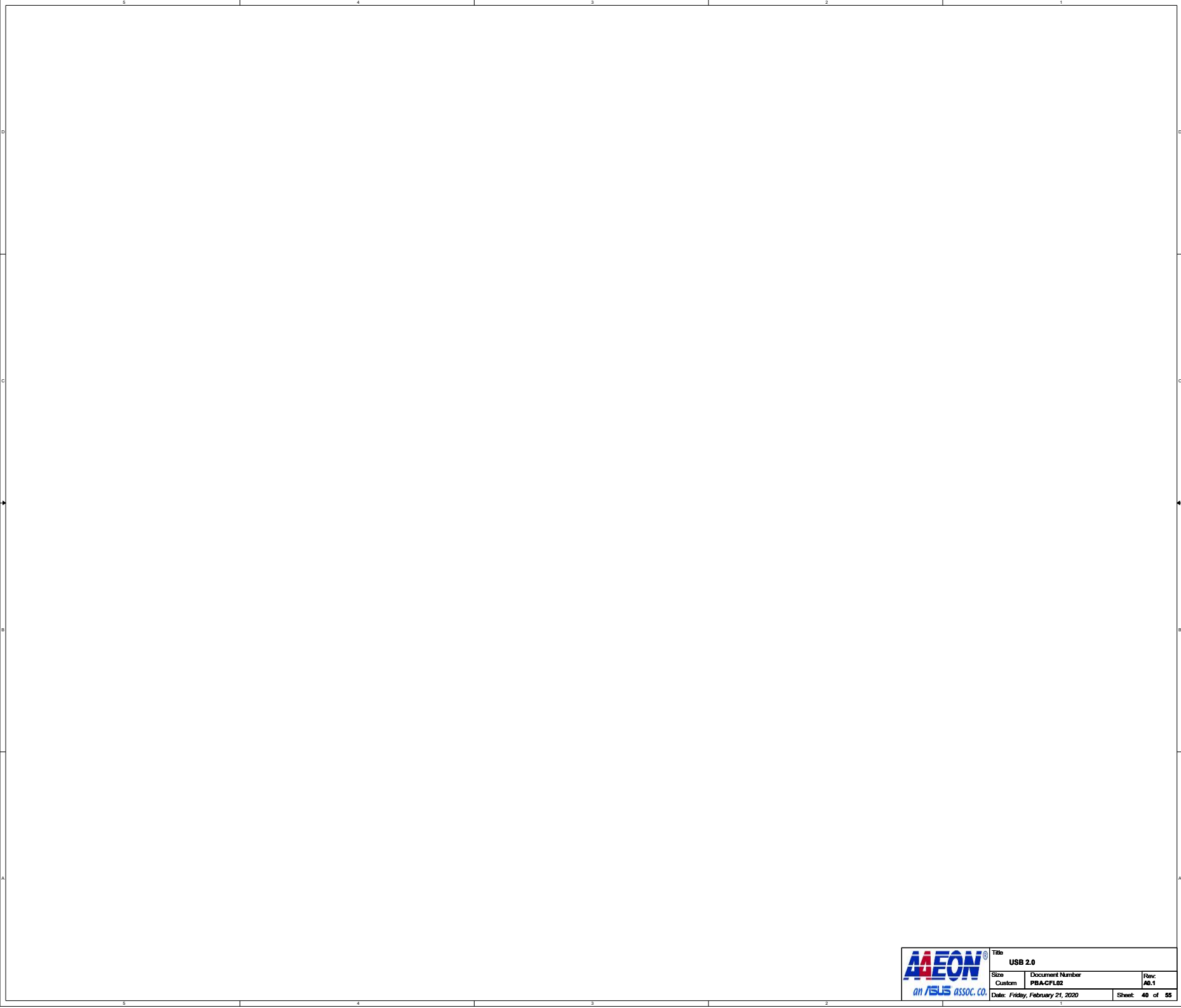



MINI Card 1



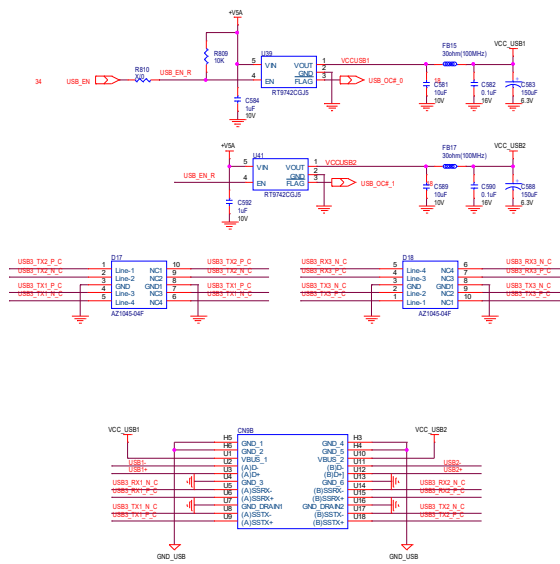
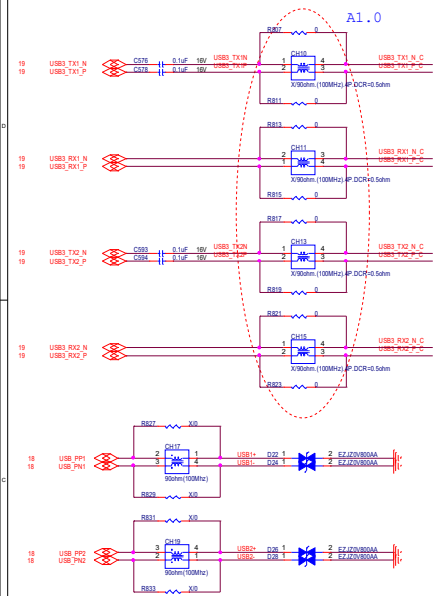
MINI Card 2 PCIe/ mSATA



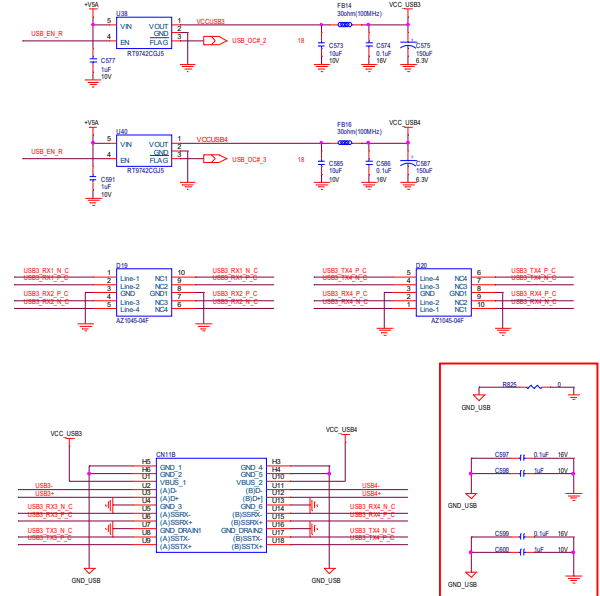
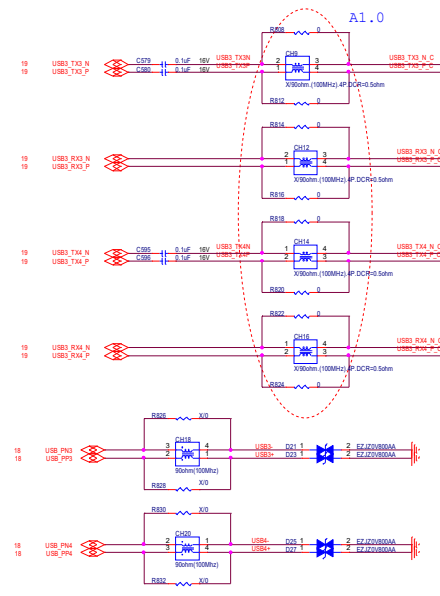


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|  <i>an ASUS ASSOC. CO.</i> | | Title USB 2.0 | |
| | | Size Custom | Document Number PBA-CFL02 |
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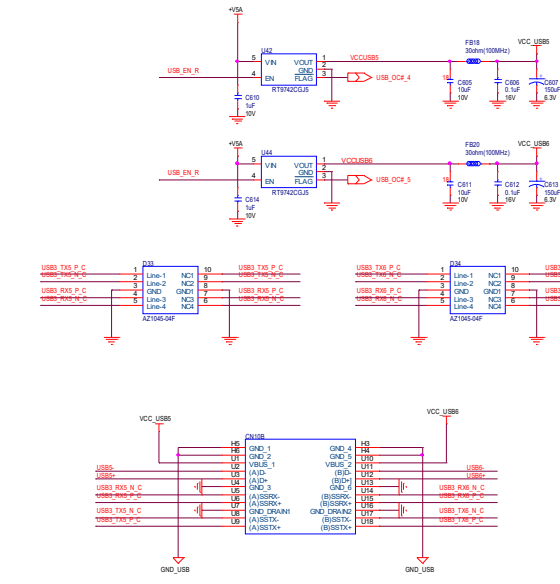
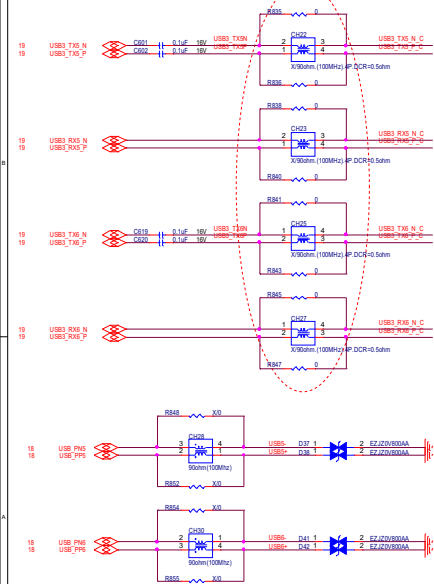
RJ45 (I211) +USB3 .0x2



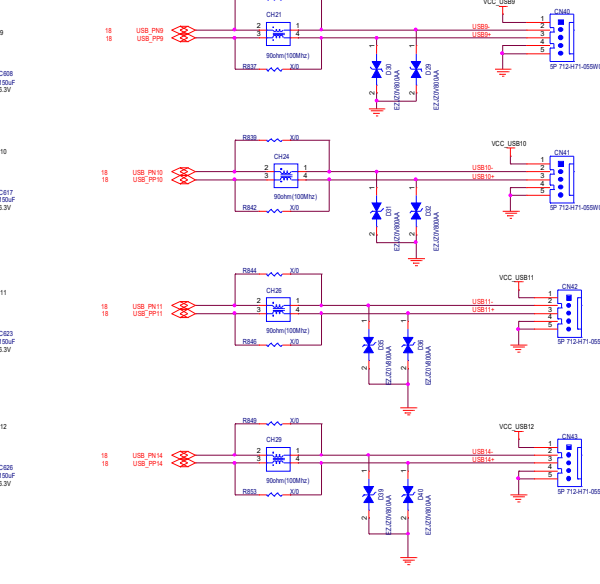
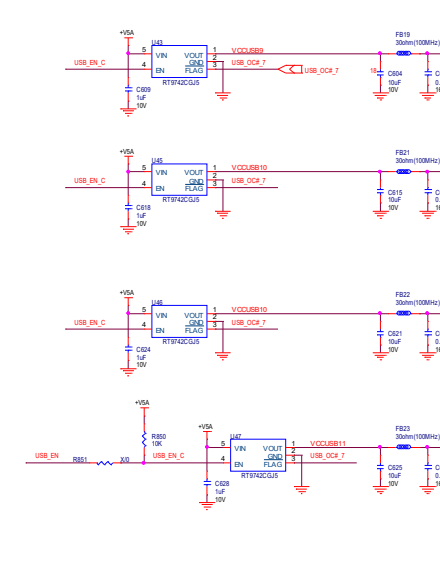
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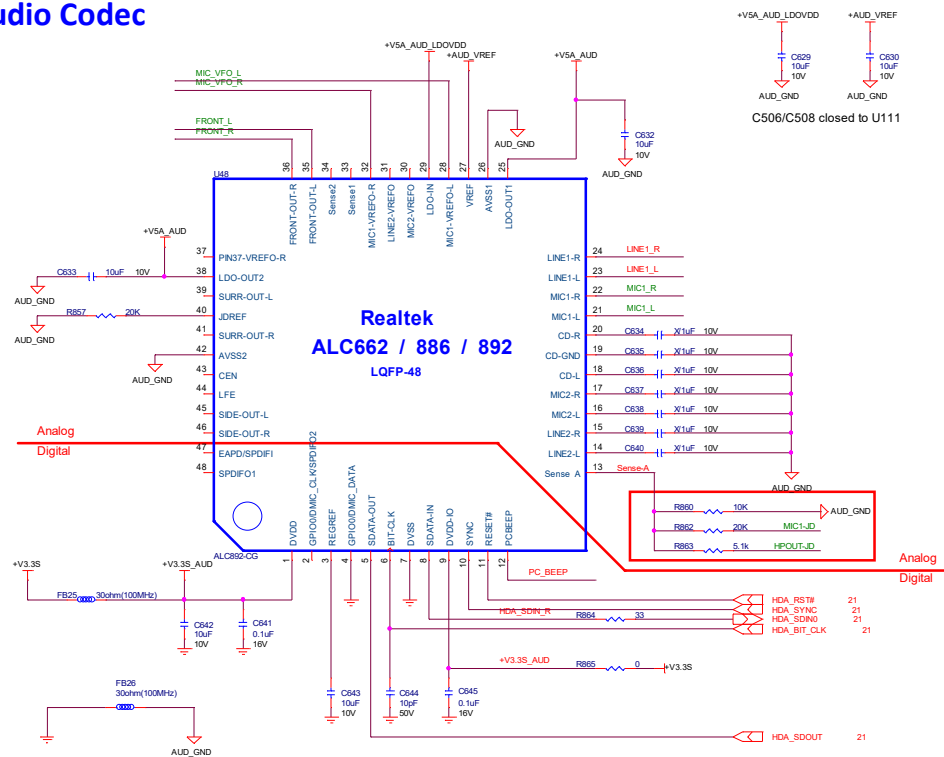
RJ45 (I211) +USB3 .0x2



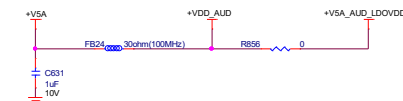
USB2 .0



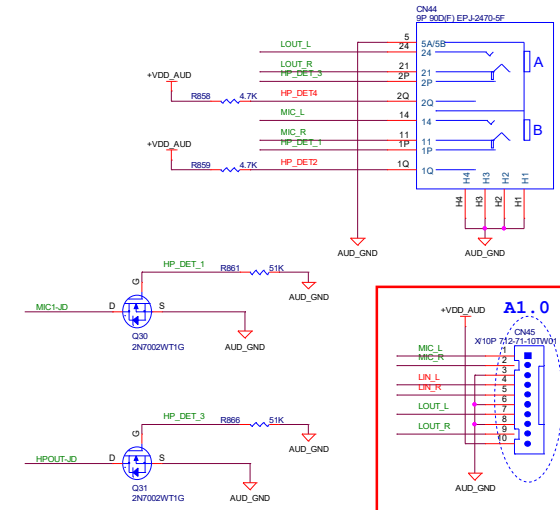
Audio Codec



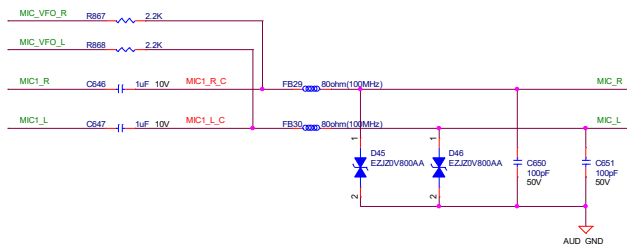
Audio PWR



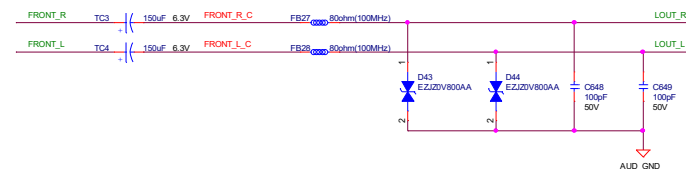
Audio CONN



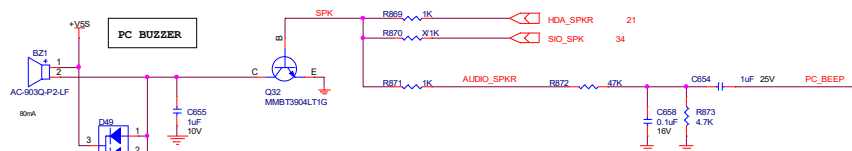
MIC



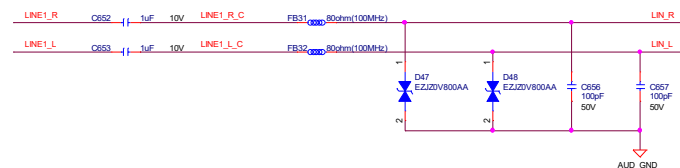
Line-out

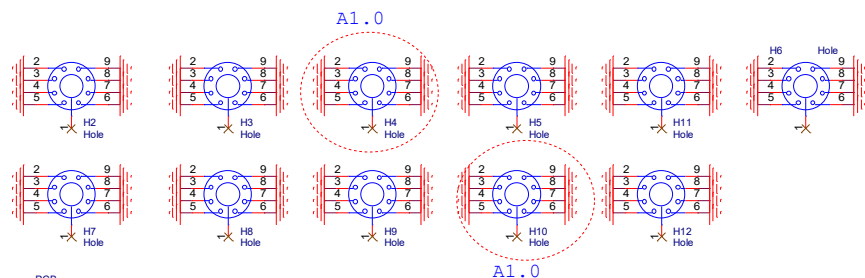
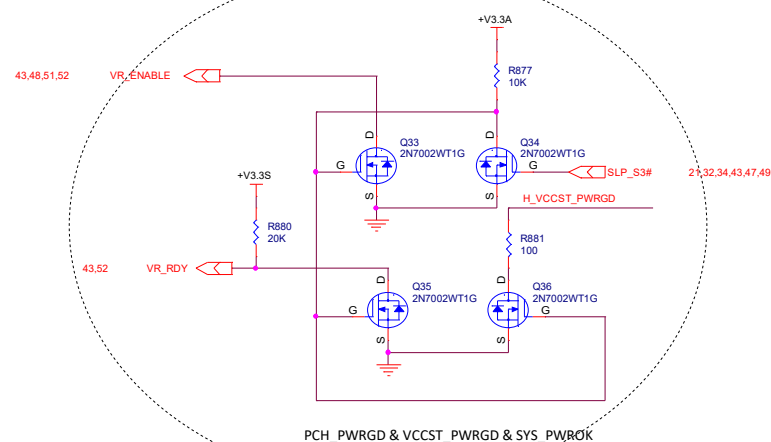
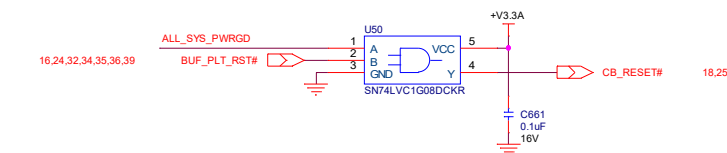
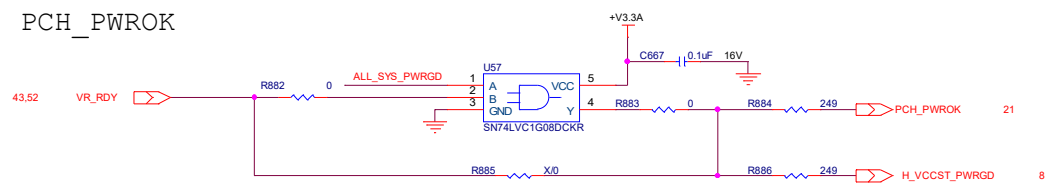
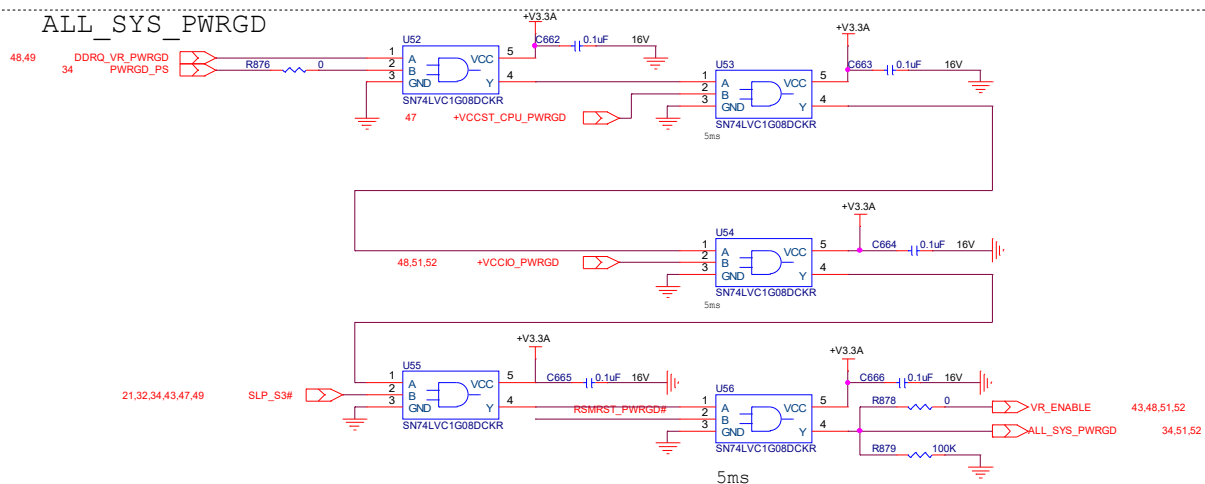
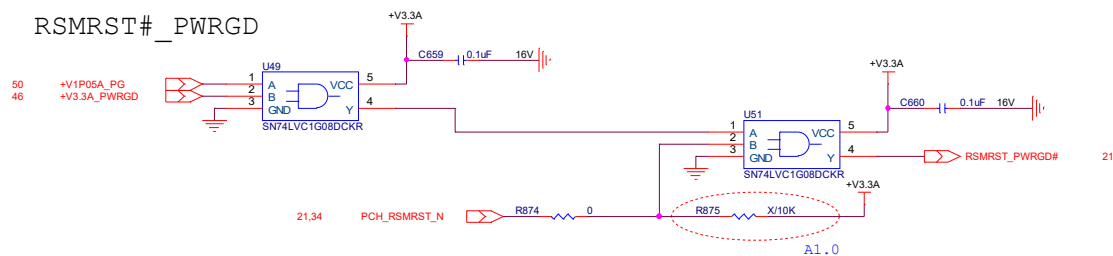


BUZZER



Line-IN





(TF)PCB.PBA-CFLS02 Rev.A1.0 0 0.Non-HDI.8Layers.Green.1*1.270x208x1.8mm



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| 27 | Title | Author | Date | Page |
| 28 | Title | Author | Date | Page |
| 29 | Title | Author | | |

Boot Sequence

Size
A

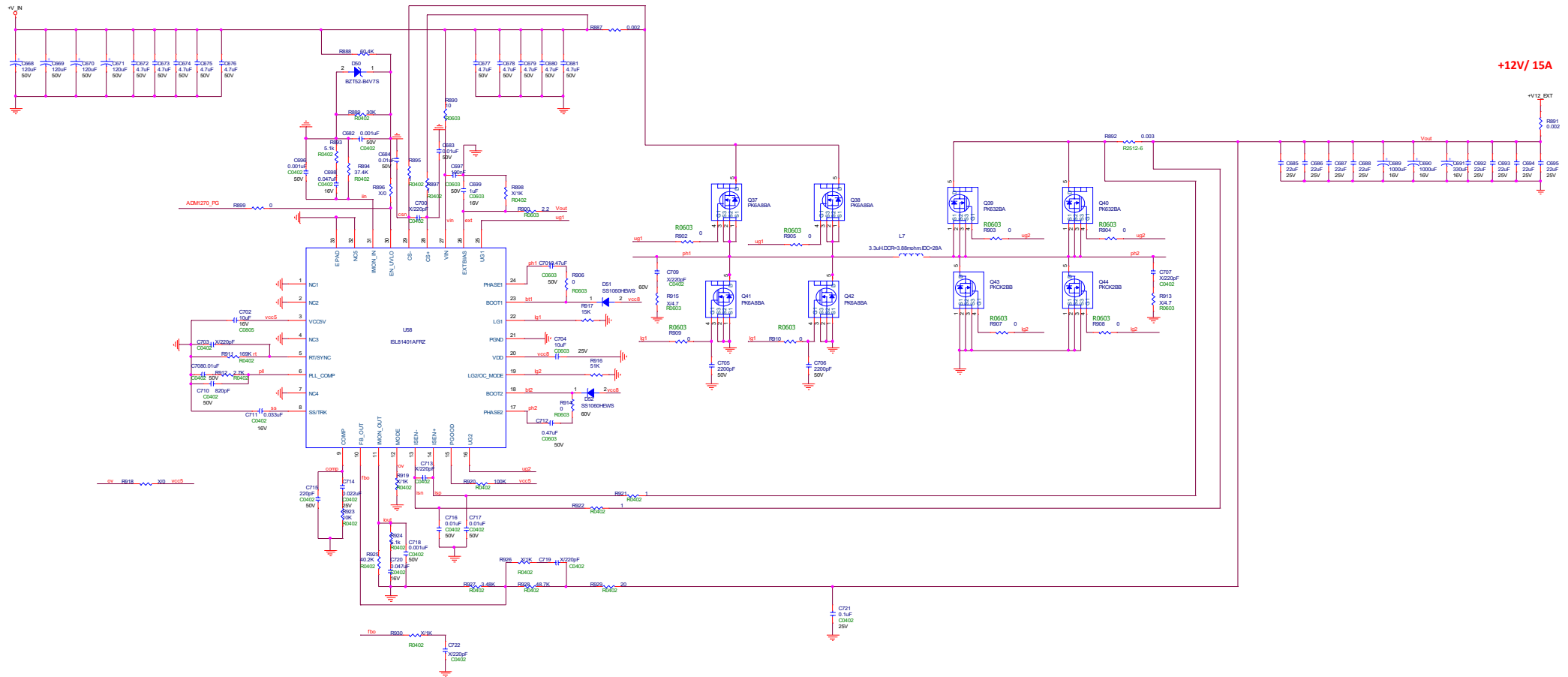
Document Number
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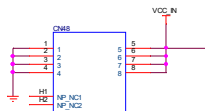
Date: *Friday, February 21, 2020*

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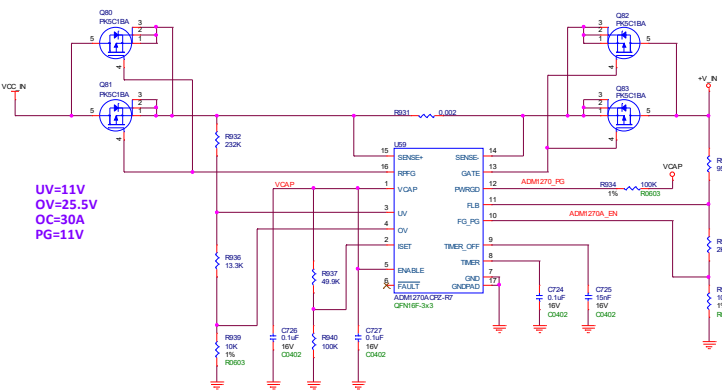
Vin=12-24V



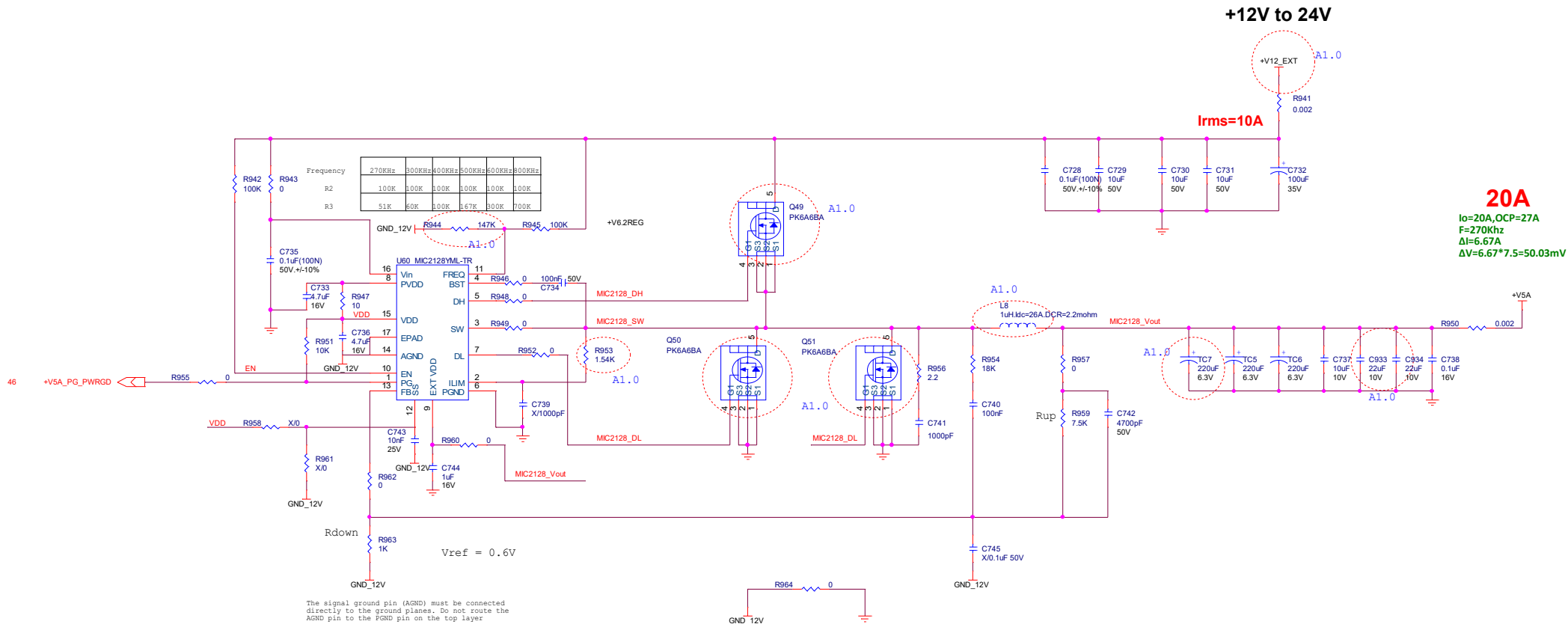
Power Input 12-24V



UV=11V
OV=25.5V
OC=30A
PG=11V



+V5A



| | | | | | | | | | | | |
|-------|------|-------|------|-------|-------|-------|-------|----|-----|-----|--|
| Rdown | 15K | 11.3K | 7.5K | 4.99K | 3.74K | 2.37K | 1.69K | 1K | 392 | 192 | |
| Vout | 0.9V | 1V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | 5V | 12V | 24V | |

The signal ground pin (AGND) must be connected directly to the ground planes. Do not route the AGND pin to the PGND pin on the top layer

The 4.7 μ F ceramic capacitors C10, C11, which are connected to the VDD and PVDD pins, must be located right at the IC. The VDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDD, PVDD and AGND, PGND pins respectively.



| | |
|-------|-------------------|
| Title | POWER_+V5A |
|-------|-------------------|

| |
|--------|
| Size |
| Custom |

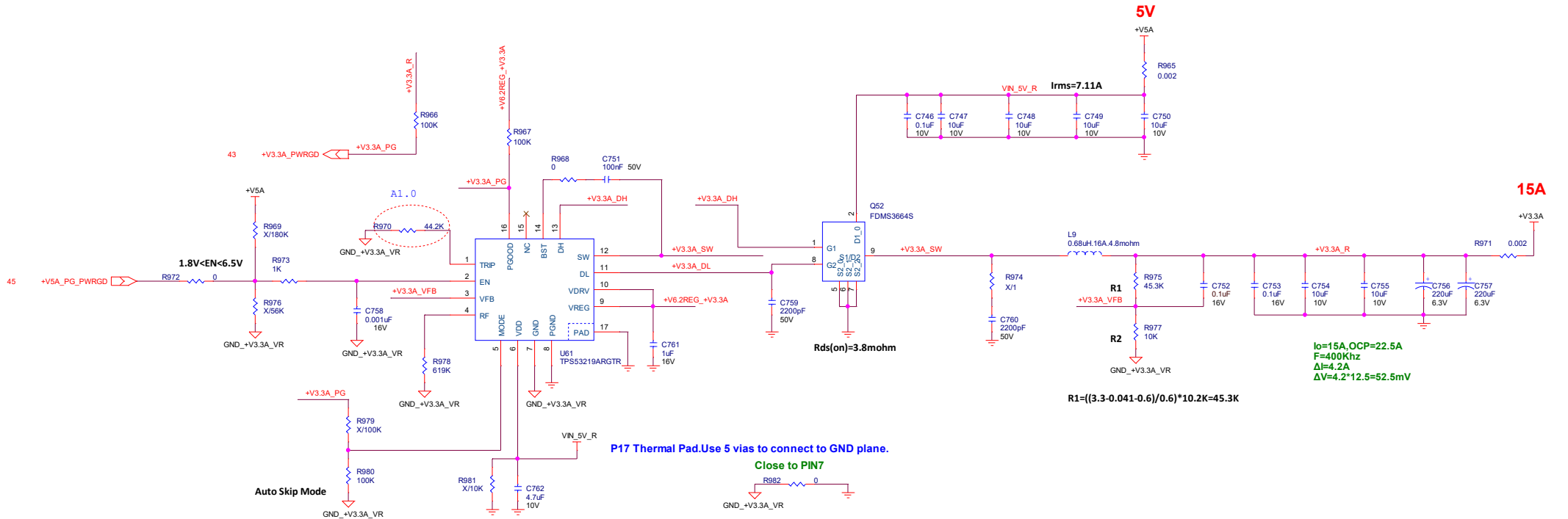
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+V3.3A



P17 Thermal Pad. Use 5 vias to connect to GND plane.
Close to PIN7

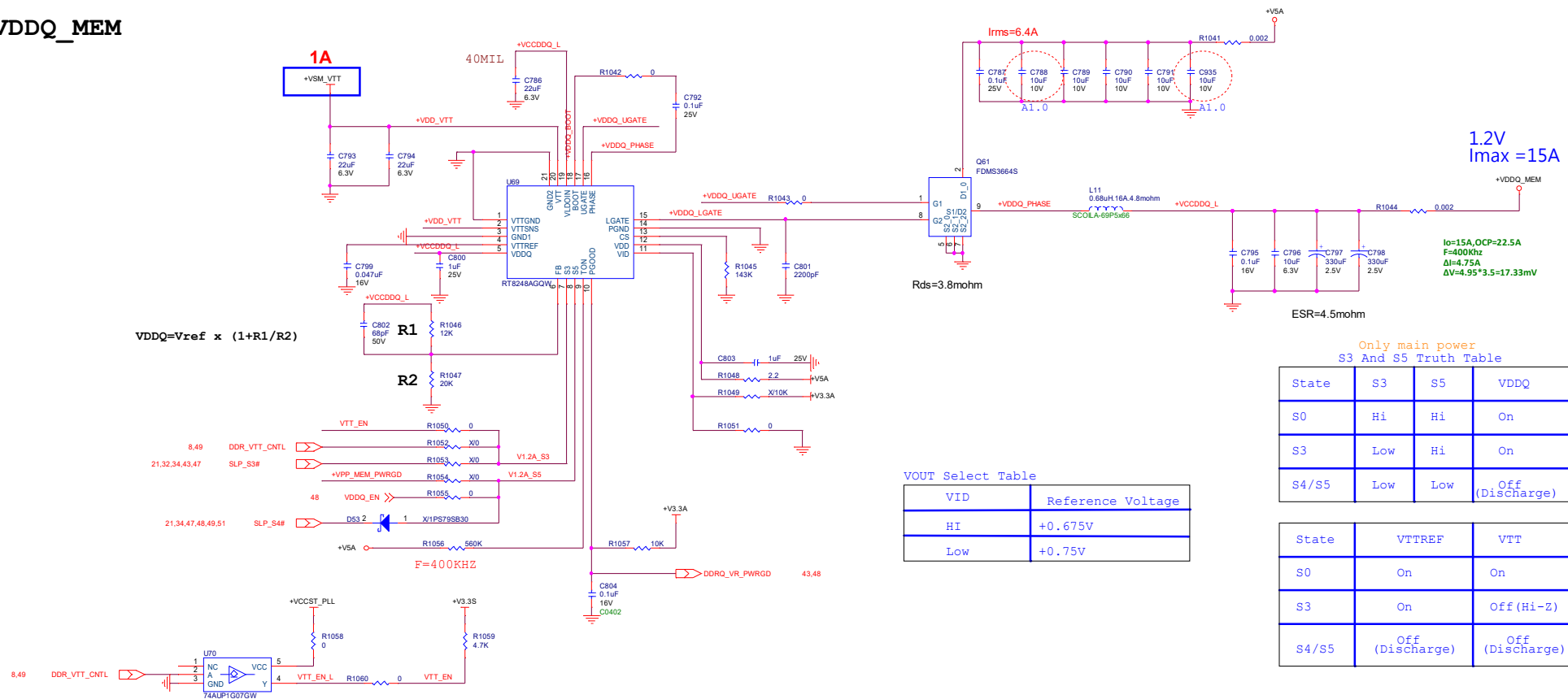
$$R1 = ((3.3 - 0.041 - 0.6) / 0.6) * 10.2K = 45.3K$$

$I_o = 15A, OCP = 22.5A$
 $F = 400KHz$
 $\Delta I = 4.2A$
 $\Delta V = 4.2 * 12.5 = 52.5mV$



| | | |
|---------------------------------|------------------------------|-----------------|
| Title POWER_+V3.3A | | |
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+VDDQ_MEM



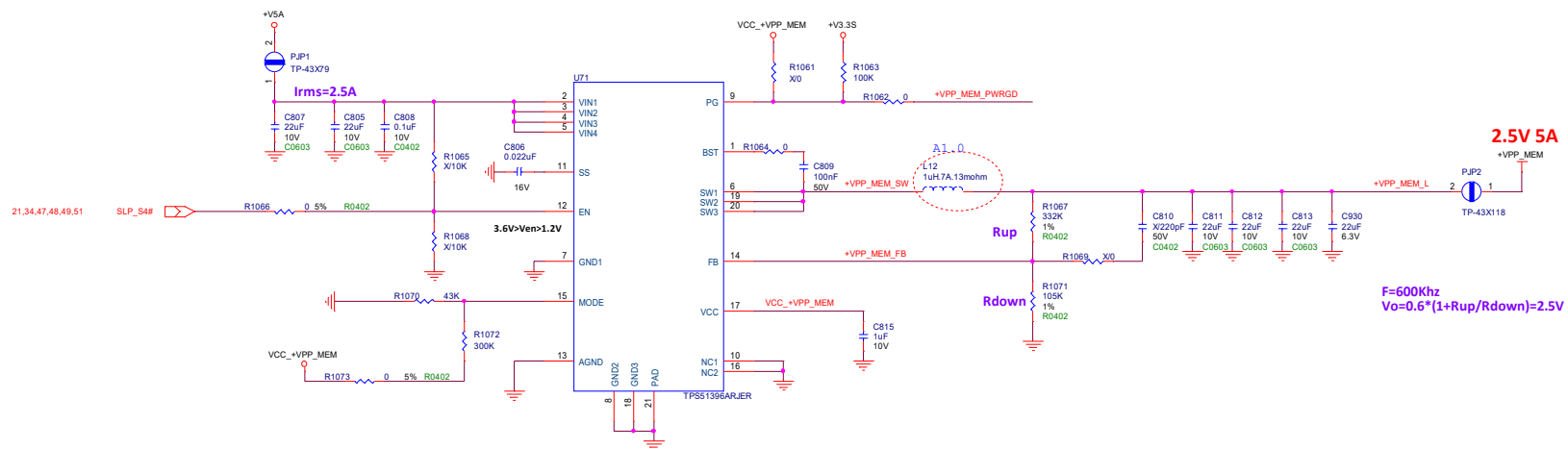
Only main power

S3 And S5 Truth Table

| State | S3 | S5 | VDDQ |
|-------|-----|-----|-----------------|
| S0 | Hi | Hi | On |
| S3 | Low | Hi | On |
| S4/S5 | Low | Low | Off (Discharge) |

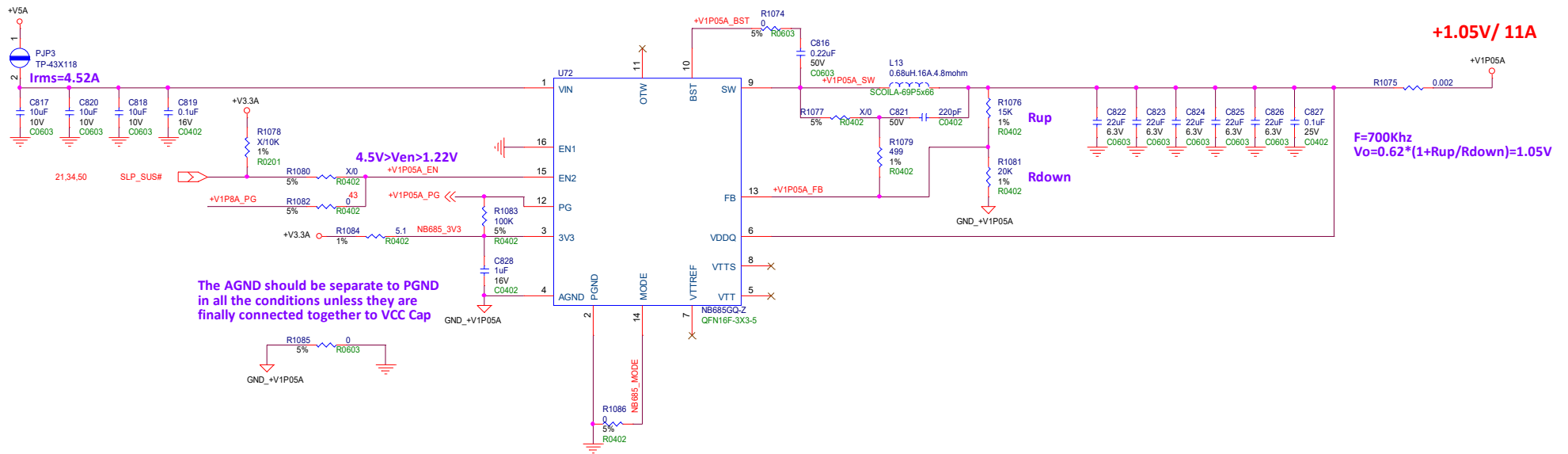
| State | VTTREF | VTT |
|-------|--------------------|--------------------|
| S0 | On | On |
| S3 | On | Off (Hi-Z) |
| S4/S5 | Off (Discharge) | Off (Discharge) |

+VPP MEM

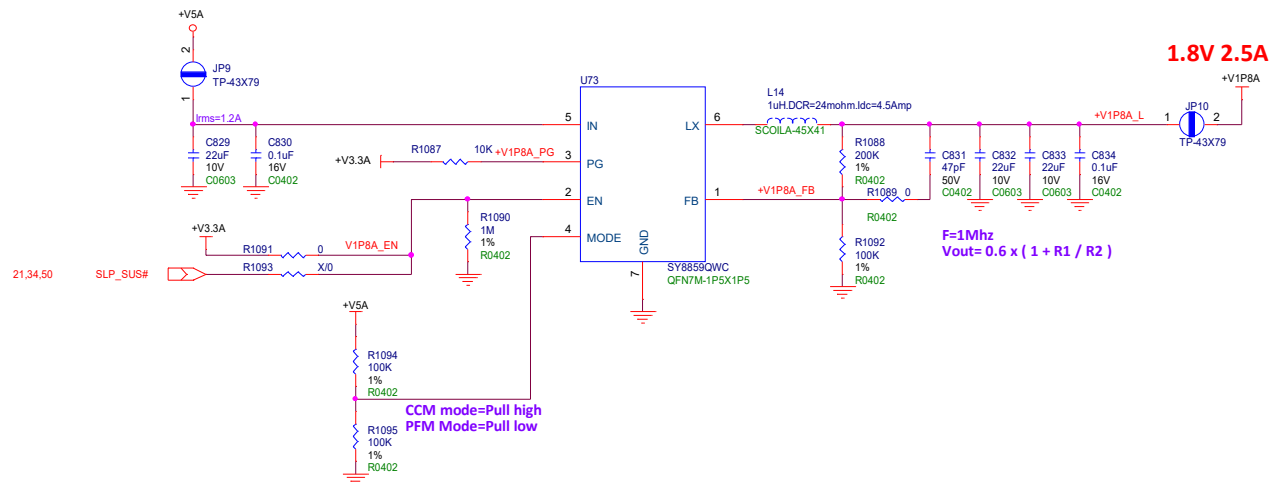


| | RM_H | RM_L | Freq. |
|-----|------|------|--------|
| OOA | 300K | 43K | 600Khz |
| CCM | 110K | 51K | 600Khz |

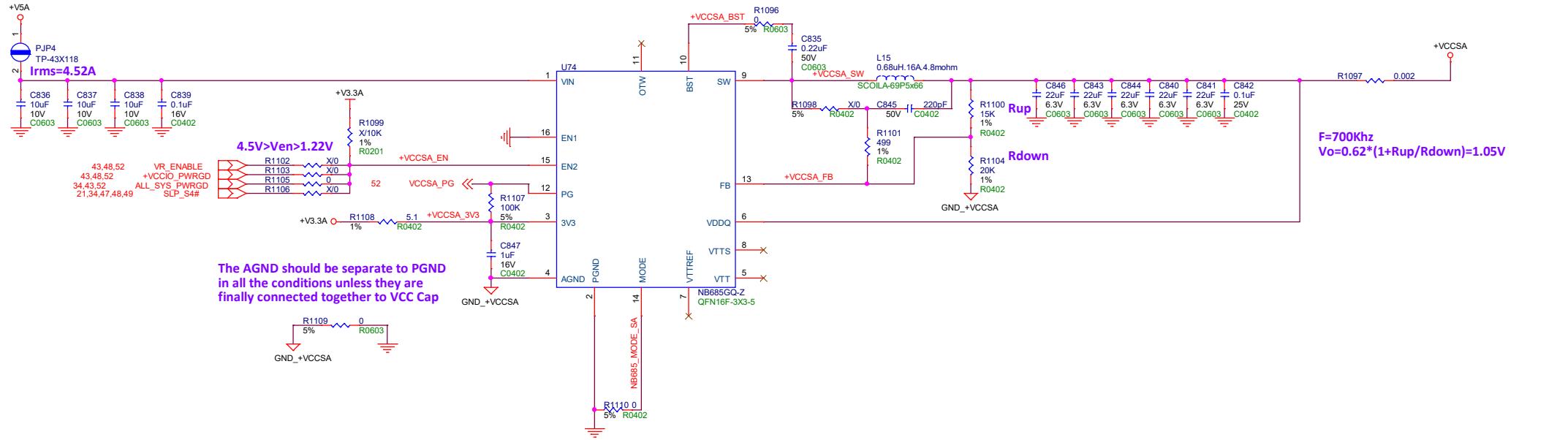
+V1P05A




+V1P8A

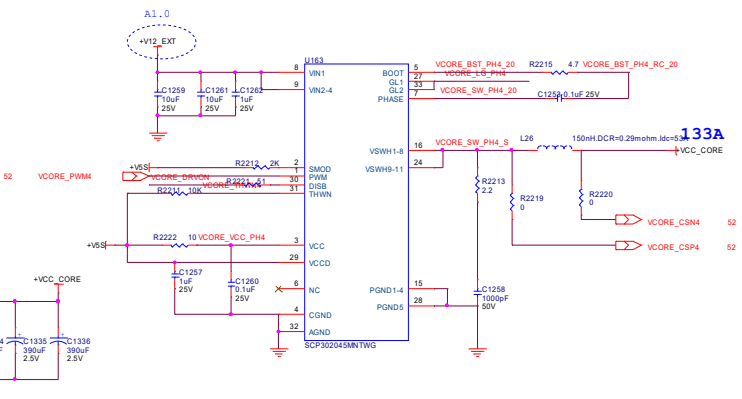
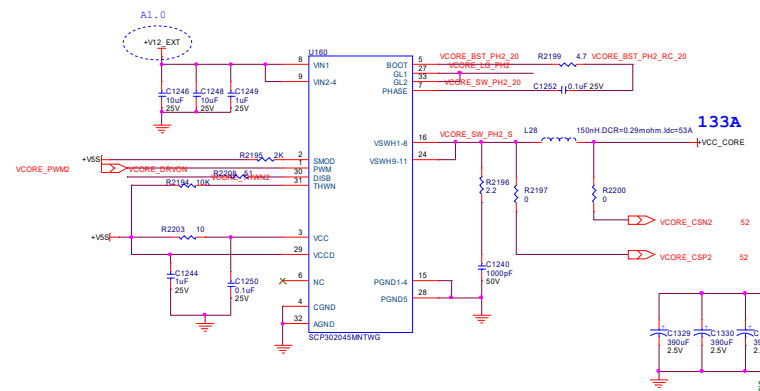
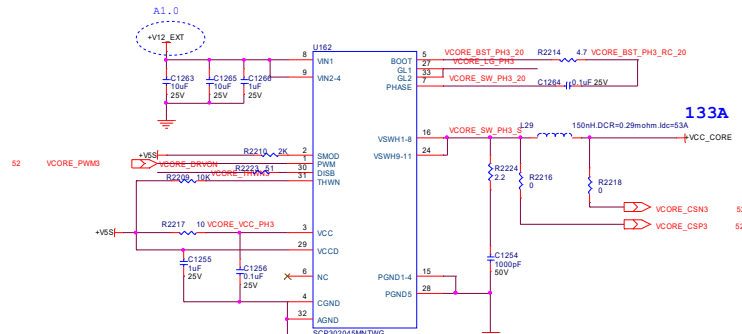
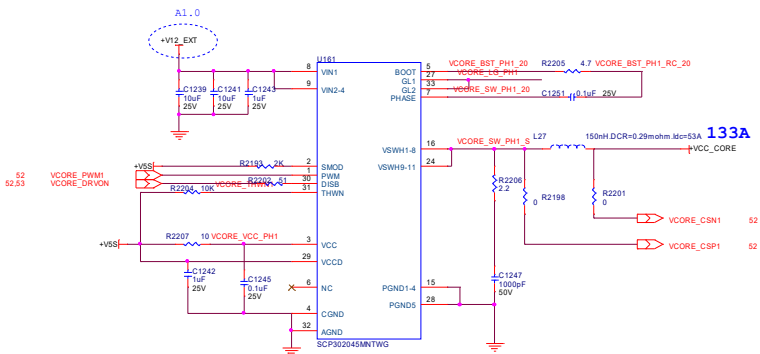


+VCCSA

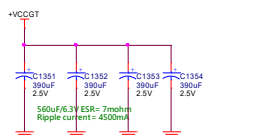
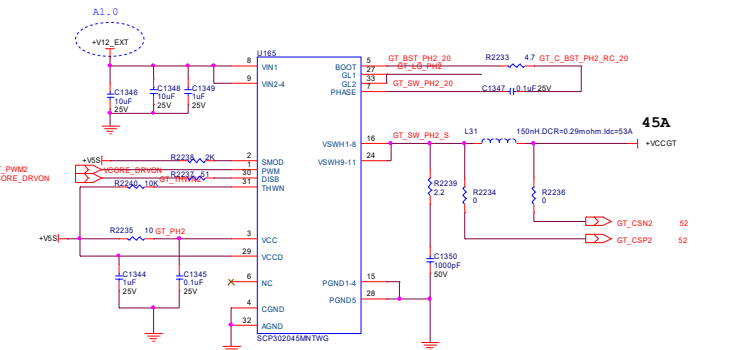
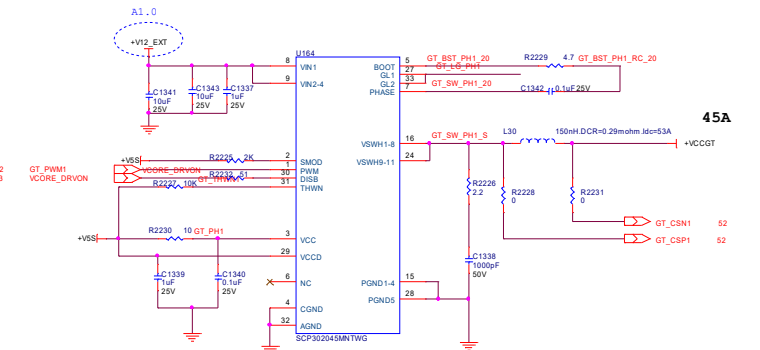


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|---|--------|-----------------|------|
|  | | Title | |
| | | POWER_+VCCSA | |
| Size | Custom | Document Number | Rev: |
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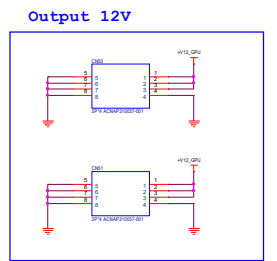
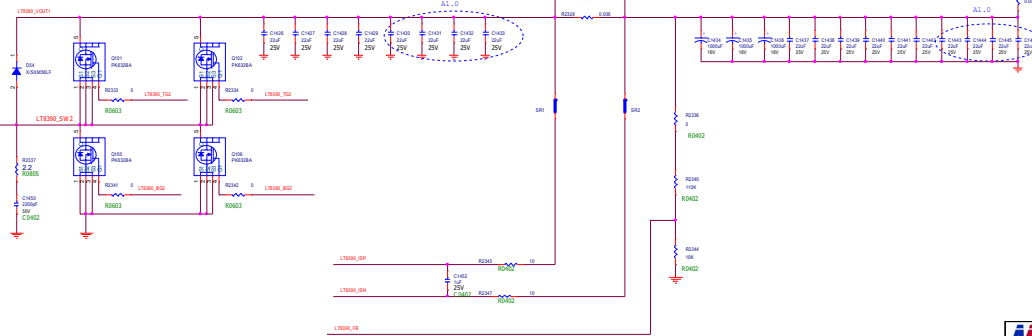
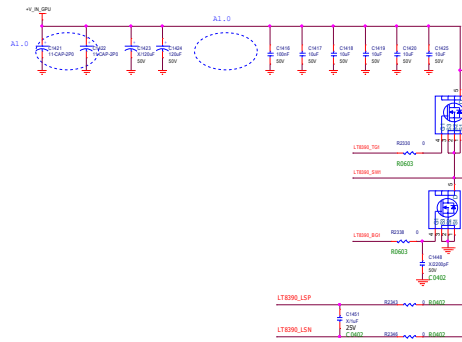
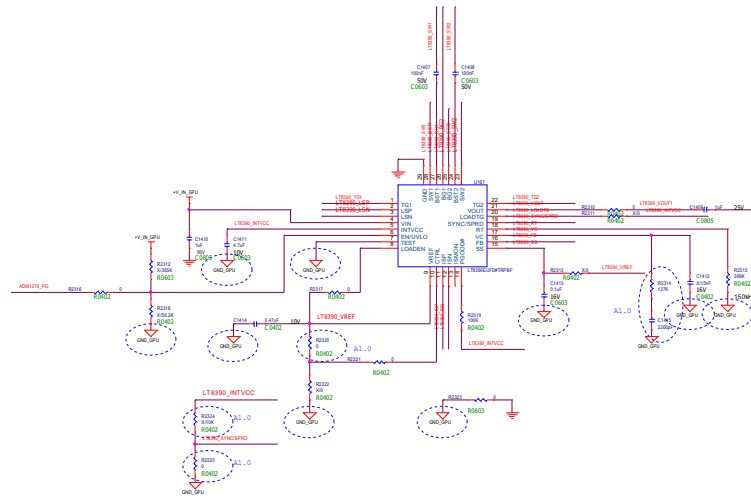
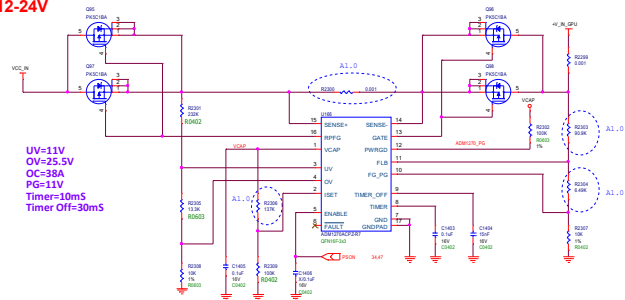
+VCC_CORE




+VCCGT



Vin=12-24V



| | | |
|---|---------------------------------|-----------------|
|  an ASUS assoc. co. | Title | |
| | EXT_GPU_PWR | |
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| | Custom | PBA-CPL2 |
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HISTORY

| Item | Date | Revision | Description | Page | Design By | Approve By |
|------|------------|----------|---|------|-----------|------------|
| 1 | 2019/08/05 | A0.1 | First Realease | | Kevin Yu | Jack Peng |
| 1 | 2019/12/16 | A1.0 | Change C859, C867 to 1124456090 | 52 | Kevin Yu | |
| 2 | | | Change R1195 to 105A540269 | 52 | | |
| 3 | | | change PCIE/ SATA jumper settingm for M.2 | 32 | | |
| 4 | | | change PCIE/ SATA jumper settingm for Minicard | 39 | | |
| 5 | | | De-pop R798, R796,R805, pop R804 | 39 | | |
| 6 | | | De-pop Q14, R587, R582, R592, pop R591 | 32 | | |
| 7 | | | Change R806, R595 to 0 ohm | 39 | | |
| 8 | | | De-pop R662, Pop R659 | 34 | | |
| 9 | | | Change R787 to 0 ohm | 38 | | |
| 10 | | | Change CPU FAN circuit same with SYS FAN | 31 | | |
| 11 | | | De-pop R613 | 34 | | |
| 12 | | | De-pop R251, R875, and pop R252 | 21 | | |
| 13 | | | PCH_RSMRST_N connector to U51 pin2 | 43 | | |
| 14 | | | Pop R807, R811, R813, R815, R817, R819, R821, R823, R808, R812, R814, R816, R818, R820, R822, R824, R835, R836, R838, R840, R841, R843, R845, R857 and de-pop CH10, CH11, CH13, CH15, CH9, CH12, CH14, CH16, CH22, CH23, CH25, CH27 for USB 3.0 Si fail issue | 41 | | |
| | | | Changed R1031 from 20K to 18.7k(1050518744) for Output ripple adjust. | 48 | | |
| | | | Changed L12 from 1.5uH to 1uH(121111007M) for Transient adjust. | 49 | | |
| | | | Changed R970 from 51K to 44.2K(105A544229) for OCP adjust. | 46 | | |
| | | | Chang L8 from 2.2uH to 1uH(121110106Y) for transient adjust. | 45 | | |
| | | | Add 220uf(118A622192)*1 TC7 parallel to TC5 for transient adjust. | 45 | | |
| | | | Add 22uf x2 (11EB522011) C933, C934 parallel to C737 for transient adjust. | 45 | | |
| | | | Changed R944 from 51K to 147K(105A514734) for frequency adjust. | 45 | | |
| | | | Changed Q49 、 Q50 、 Q51 from PK6A6BA to BSC093N04LS G(13150093N0) | 45 | | |
| | | | Changed R953 from 1.87K to 1.54K(105A515419) for OCP adjust. | 45 | | |
| | | | Mount C788 for Vin ripple adjust. | 49 | | |
| | | | Add 10uff(11EB610050) parallel to C791 for Vin ripple adjust. | 49 | | |



| | | |
|---------------------------------|------------------------------|-----------------|
| Title HISTORY | | |
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