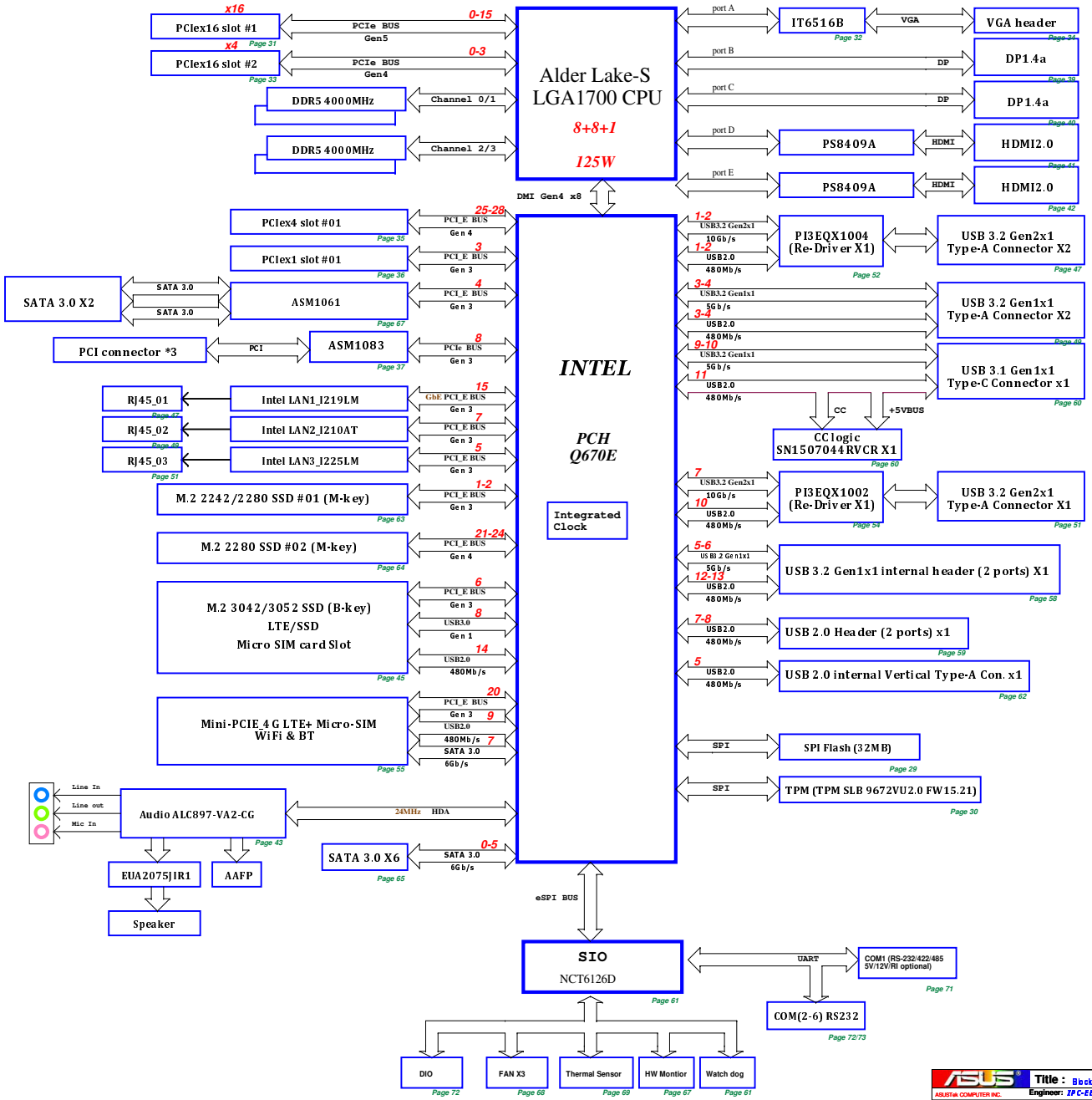
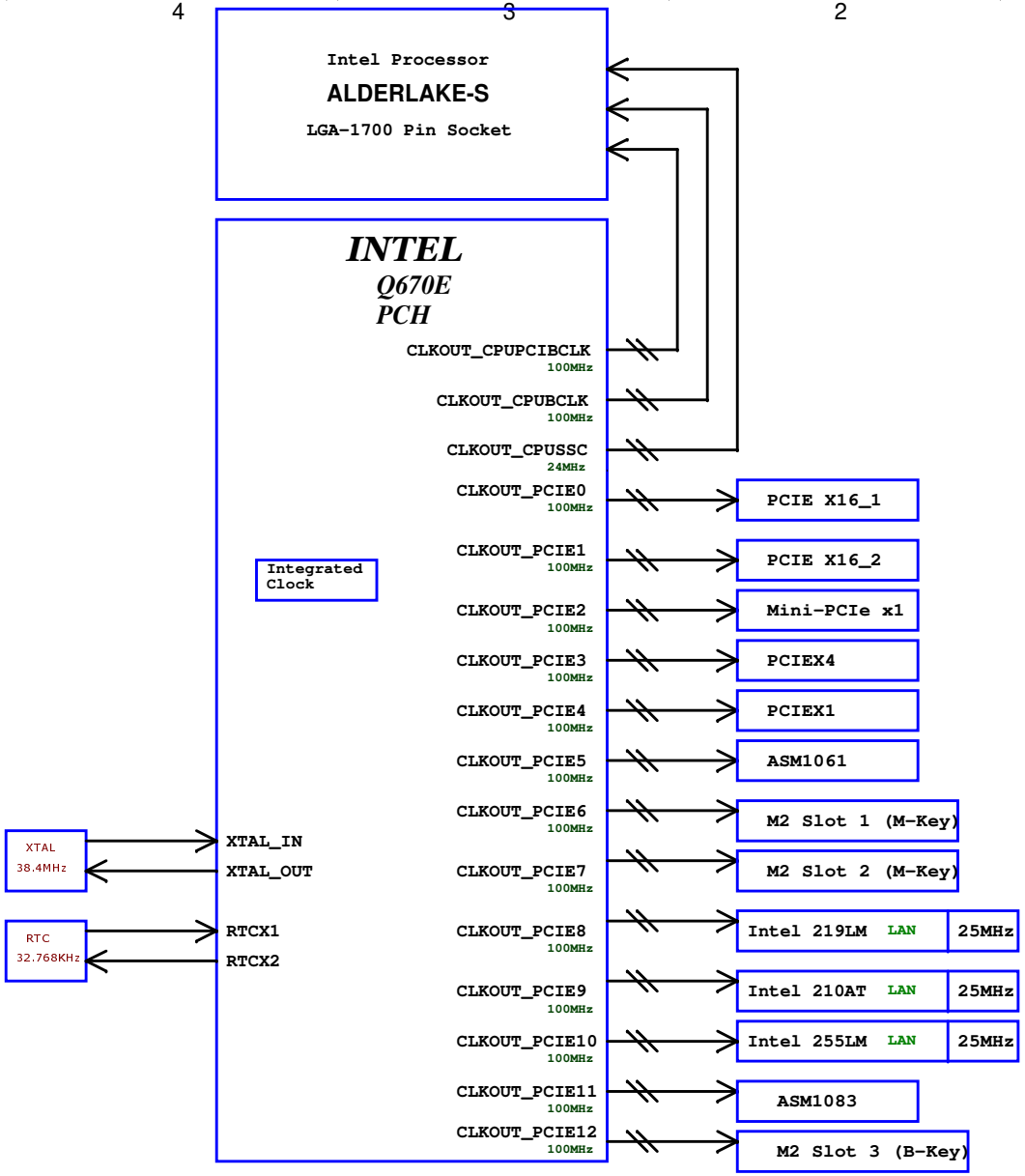
ATX-Q670A
Block Diagram Rev 1.00

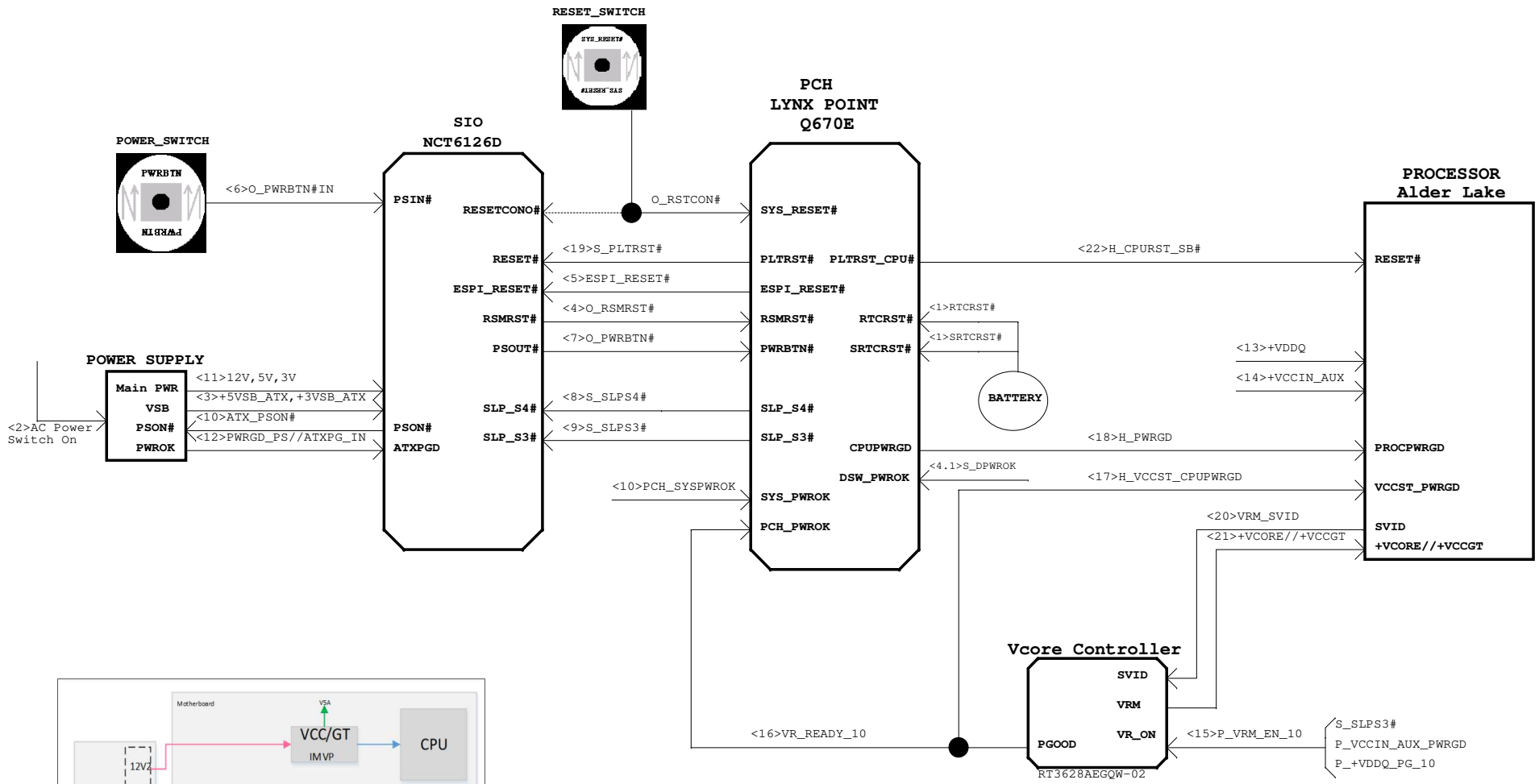


ASUSTeK COMPUTER INC.	Title : Block Diagram
	Engineer: IPC-EE3
Size: Custom	Project Name: ATX-Q670E
	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 1 of 90



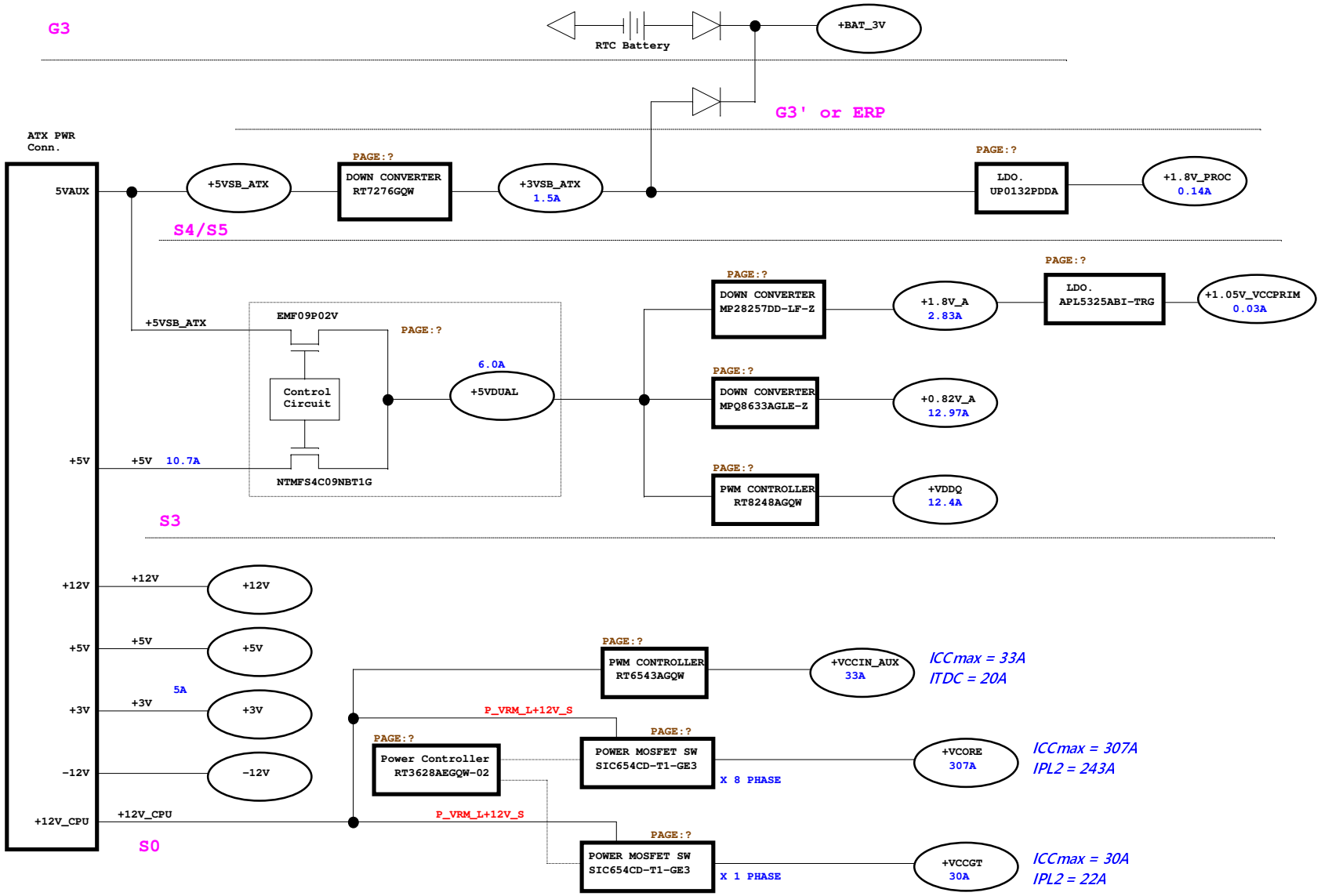
<Variant Name>

ASUS	Title : Clock Distribution	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 2 of 90	



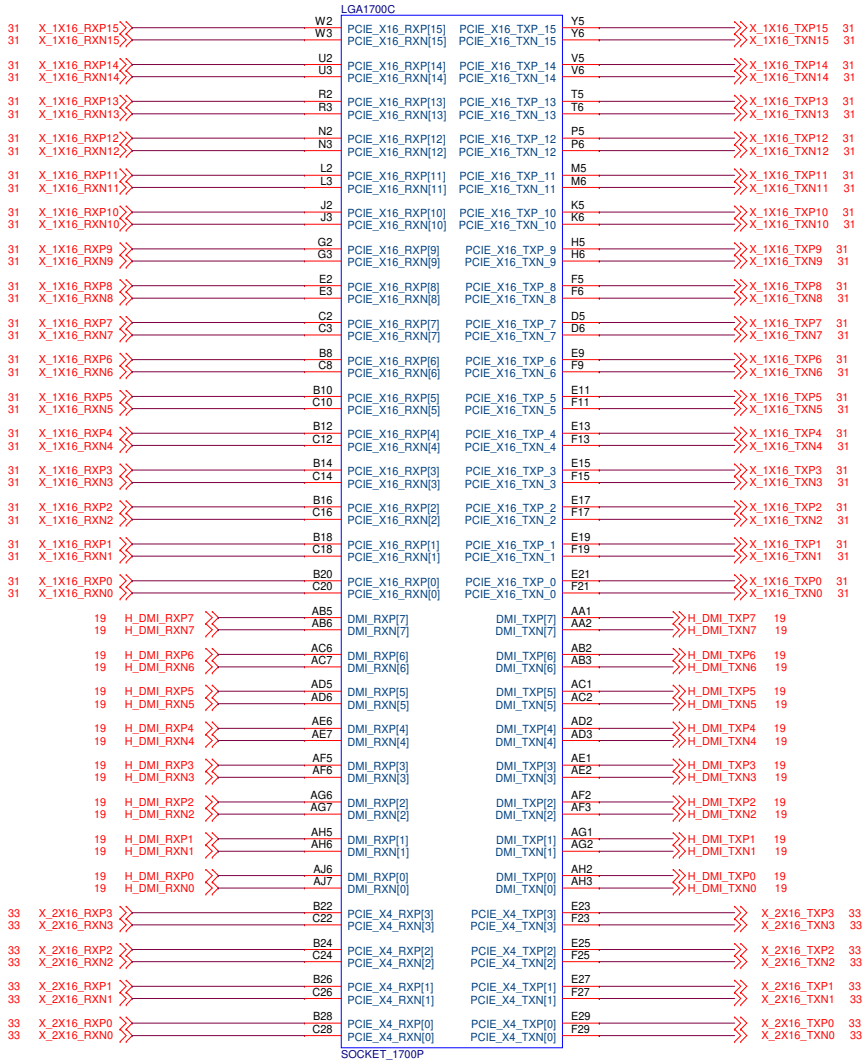
<Variant Name>

ASUS	Title : Signal & Reset map	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 3 of 90	



<Variant Name>

ASUS	Title : Power Flow	
ASUSTek COMPUTER INC.	Engineer: IPC-Power	
Size: Custom	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 4 of 90	



FOXCONN/PE17001-11AJ1-1H

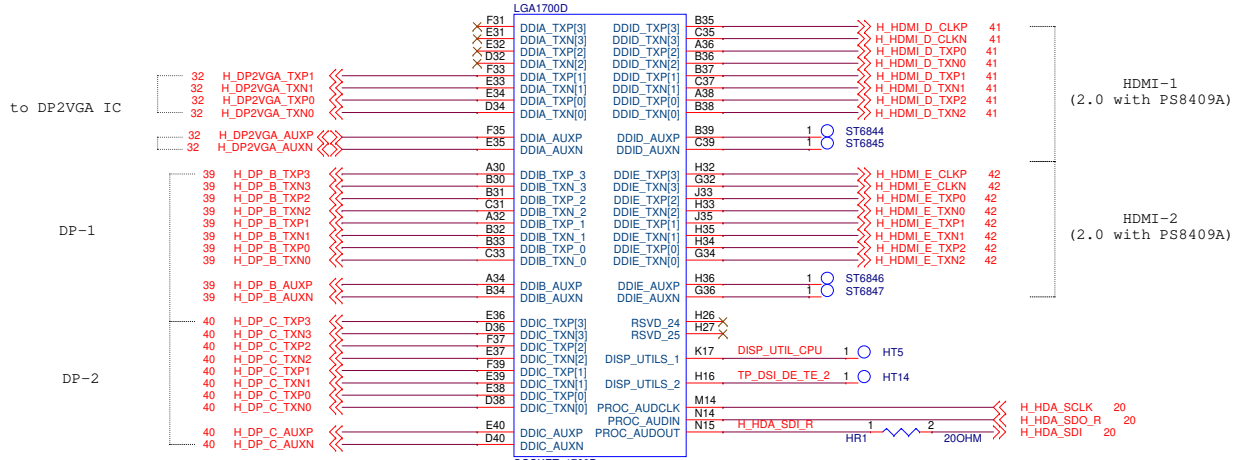
12001-00300400

LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H

2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C

ASUS	Title : LGA1700 (DMI/PCIE)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name ATX-Q670E		Rev 1.00
Date: Friday, May 20, 2022	Sheet 5 of 90		



12001-00300400

LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H

2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C

ASUS	Title: LGA1700 (DISPLAY)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: A3	Project Name: ATX-Q670E		Rev: 1.00
Date: Friday, May 20, 2022	Sheet 6 of 90		

Channel 0/1
6 Layer routing

DDR4 (IL) / DDR4 (NIL) / DDR5 DDR4 / DDR5

LGA1700A

Signal	Pin	Signal	Pin
13,14 D5_DDR1_DQ3[0:7]			
D5_DDR1_DQ34	AM2	DDR0_DQ7[7]/DDR1_DQ5[7]	/DDR1_DQ3[7]
D5_DDR1_DQ35	AL2	DDR0_DQ7[6]/DDR1_DQ5[6]	/DDR1_DQ3[6]
D5_DDR1_DQ36	AL3	DDR0_DQ7[5]/DDR1_DQ5[5]	/DDR1_DQ3[5]
D5_DDR1_DQ37	AL4	DDR0_DQ7[4]/DDR1_DQ5[4]	/DDR1_DQ3[4]
D5_DDR1_DQ32	AP2	DDR0_DQ7[3]/DDR1_DQ5[3]	/DDR1_DQ3[3]
D5_DDR1_DQ31	AN2	DDR0_DQ7[2]/DDR1_DQ5[2]	/DDR1_DQ3[2]
D5_DDR1_DQ33	AP4	DDR0_DQ7[1]/DDR1_DQ5[1]	/DDR1_DQ3[1]
D5_DDR1_DQ30	AP3	DDR0_DQ7[0]/DDR1_DQ5[0]	/DDR1_DQ3[0]
13,14 D5_DDR1_DQ2[0:7]			
D5_DDR1_DQ24	AU2	DDR0_DQ6[7]/DDR1_DQ4[7]	/DDR1_DQ2[7]
D5_DDR1_DQ26	AT2	DDR0_DQ6[6]/DDR1_DQ4[6]	/DDR1_DQ2[6]
D5_DDR1_DQ27	AT4	DDR0_DQ6[5]/DDR1_DQ4[5]	/DDR1_DQ2[5]
D5_DDR1_DQ25	AT3	DDR0_DQ6[4]/DDR1_DQ4[4]	/DDR1_DQ2[4]
D5_DDR1_DQ21	AW2	DDR0_DQ6[3]/DDR1_DQ4[3]	/DDR1_DQ2[3]
D5_DDR1_DQ23	AV2	DDR0_DQ6[2]/DDR1_DQ4[2]	/DDR1_DQ2[2]
D5_DDR1_DQ20	AW4	DDR0_DQ6[1]/DDR1_DQ4[1]	/DDR1_DQ2[1]
D5_DDR1_DQ22	AW3	DDR0_DQ6[0]/DDR1_DQ4[0]	/DDR1_DQ2[0]
13,14 D5_DDR1_DQ1[0:7]			
D5_DDR1_DQ15	BA2	DDR0_DQ5[7]/DDR1_DQ1[7]	/DDR1_DQ1[7]
D5_DDR1_DQ17	BA1	DDR0_DQ5[6]/DDR1_DQ1[6]	/DDR1_DQ1[6]
D5_DDR1_DQ14	BA3	DDR0_DQ5[5]/DDR1_DQ1[5]	/DDR1_DQ1[5]
D5_DDR1_DQ16	BB2	DDR0_DQ5[4]/DDR1_DQ1[4]	/DDR1_DQ1[4]
D5_DDR1_DQ13	BC4	DDR0_DQ5[3]/DDR1_DQ1[3]	/DDR1_DQ1[3]
D5_DDR1_DQ11	BB5	DDR0_DQ5[2]/DDR1_DQ1[2]	/DDR1_DQ1[2]
D5_DDR1_DQ12	BD4	DDR0_DQ5[1]/DDR1_DQ1[1]	/DDR1_DQ1[1]
D5_DDR1_DQ10	BC5	DDR0_DQ5[0]/DDR1_DQ1[0]	/DDR1_DQ1[0]
13,14 D5_DDR1_DQ0[0:7]			
D5_DDR1_DQ07	BA7	DDR0_DQ4[7]/DDR1_DQ0[7]	/DDR1_DQ0[7]
D5_DDR1_DQ06	BC7	DDR0_DQ4[6]/DDR1_DQ0[6]	/DDR1_DQ0[6]
D5_DDR1_DQ04	BC8	DDR0_DQ4[5]/DDR1_DQ0[5]	/DDR1_DQ0[5]
D5_DDR1_DQ05	BB7	DDR0_DQ4[4]/DDR1_DQ0[4]	/DDR1_DQ0[4]
D5_DDR1_DQ02	BB10	DDR0_DQ4[3]/DDR1_DQ0[3]	/DDR1_DQ0[3]
D5_DDR1_DQ00	BA10	DDR0_DQ4[2]/DDR1_DQ0[2]	/DDR1_DQ0[2]
D5_DDR1_DQ01	BC10	DDR0_DQ4[1]/DDR1_DQ0[1]	/DDR1_DQ0[1]
D5_DDR1_DQ03	BC9	DDR0_DQ4[0]/DDR1_DQ0[0]	/DDR1_DQ0[0]
13,14 D5_DDR0_DQ3[0:7]			
D5_DDR0_DQ34	BC45	DDR0_DQ3[7]/DDR0_DQ5[7]	/DDR0_DQ3[7]
D5_DDR0_DQ38	BC44	DDR0_DQ3[6]/DDR0_DQ5[6]	/DDR0_DQ3[6]
D5_DDR0_DQ37	BA44	DDR0_DQ3[5]/DDR0_DQ5[5]	/DDR0_DQ3[5]
D5_DDR0_DQ35	BB44	DDR0_DQ3[4]/DDR0_DQ5[4]	/DDR0_DQ3[4]
D5_DDR0_DQ32	BC47	DDR0_DQ3[3]/DDR0_DQ5[3]	/DDR0_DQ3[3]
D5_DDR0_DQ33	BC46	DDR0_DQ3[2]/DDR0_DQ5[2]	/DDR0_DQ3[2]
D5_DDR0_DQ31	BB47	DDR0_DQ3[1]/DDR0_DQ5[1]	/DDR0_DQ3[1]
D5_DDR0_DQ30	BA47	DDR0_DQ3[0]/DDR0_DQ5[0]	/DDR0_DQ3[0]
13,14 D5_DDR0_DQ2[0:7]			
D5_DDR0_DQ25	BC49	DDR0_DQ2[7]/DDR0_DQ4[7]	/DDR0_DQ2[7]
D5_DDR0_DQ27	BD49	DDR0_DQ2[6]/DDR0_DQ4[6]	/DDR0_DQ2[6]
D5_DDR0_DQ24	BC50	DDR0_DQ2[5]/DDR0_DQ4[5]	/DDR0_DQ2[5]
D5_DDR0_DQ26	BB49	DDR0_DQ2[4]/DDR0_DQ4[4]	/DDR0_DQ2[4]
D5_DDR0_DQ22	BA52	DDR0_DQ2[3]/DDR0_DQ4[3]	/DDR0_DQ2[3]
D5_DDR0_DQ21	BA51	DDR0_DQ2[2]/DDR0_DQ4[2]	/DDR0_DQ2[2]
D5_DDR0_DQ20	AY51	DDR0_DQ2[1]/DDR0_DQ4[1]	/DDR0_DQ2[1]
D5_DDR0_DQ23	AY50	DDR0_DQ2[0]/DDR0_DQ4[0]	/DDR0_DQ2[0]
13,14 D5_DDR0_DQ1[0:7]			
D5_DDR0_DQ15	AV50	DDR0_DQ1[7]/DDR0_DQ1[7]	/DDR0_DQ1[7]
D5_DDR0_DQ17	AV49	DDR0_DQ1[6]/DDR0_DQ1[6]	/DDR0_DQ1[6]
D5_DDR0_DQ14	AU51	DDR0_DQ1[5]/DDR0_DQ1[5]	/DDR0_DQ1[5]
D5_DDR0_DQ16	AV51	DDR0_DQ1[4]/DDR0_DQ1[4]	/DDR0_DQ1[4]
D5_DDR0_DQ12	AR50	DDR0_DQ1[3]/DDR0_DQ1[3]	/DDR0_DQ1[3]
D5_DDR0_DQ13	AR49	DDR0_DQ1[2]/DDR0_DQ1[2]	/DDR0_DQ1[2]
D5_DDR0_DQ10	AR51	DDR0_DQ1[1]/DDR0_DQ1[1]	/DDR0_DQ1[1]
D5_DDR0_DQ11	AT51	DDR0_DQ1[0]/DDR0_DQ1[0]	/DDR0_DQ1[0]
13,14 D5_DDR0_DQ0[0:7]			
D5_DDR0_DQ05	AN50	DDR0_DQ0[7]/DDR0_DQ0[7]	/DDR0_DQ0[7]
D5_DDR0_DQ07	AN49	DDR0_DQ0[6]/DDR0_DQ0[6]	/DDR0_DQ0[6]
D5_DDR0_DQ04	AM51	DDR0_DQ0[5]/DDR0_DQ0[5]	/DDR0_DQ0[5]
D5_DDR0_DQ06	AN51	DDR0_DQ0[4]/DDR0_DQ0[4]	/DDR0_DQ0[4]
D5_DDR0_DQ02	AK50	DDR0_DQ0[3]/DDR0_DQ0[3]	/DDR0_DQ0[3]
D5_DDR0_DQ00	AK49	DDR0_DQ0[2]/DDR0_DQ0[2]	/DDR0_DQ0[2]
D5_DDR0_DQ01	AK51	DDR0_DQ0[1]/DDR0_DQ0[1]	/DDR0_DQ0[1]
D5_DDR0_DQ03	AL51	DDR0_DQ0[0]/DDR0_DQ0[0]	/DDR0_DQ0[0]
	BC40	DDR0_DQ8[7]/DDR0_DQ8[7]/NC	
	BC39	DDR0_DQ8[6]/DDR0_DQ8[6]/NC	
	BA39	DDR0_DQ8[5]/DDR0_DQ8[5]/NC	
	BB39	DDR0_DQ8[4]/DDR0_DQ8[4]/NC	
13,14 D5_DDR0_DQ4[0:3]			
D5_DDR0_DQ40	BC42	DDR0_DQ8[3]/DDR0_DQ8[3]	/DDR0_DQ4[3]
D5_DDR0_DQ42	BC41	DDR0_DQ8[2]/DDR0_DQ8[2]	/DDR0_DQ4[2]
D5_DDR0_DQ43	BA42	DDR0_DQ8[1]/DDR0_DQ8[1]	/DDR0_DQ4[1]
D5_DDR0_DQ41	BB42	DDR0_DQ8[0]/DDR0_DQ8[0]	/DDR0_DQ4[0]
13,14 D5_DDR1_DQ4[0:3]			
D5_DDR1_DQ40	BA13	NC/NC/DDR1_DQ4[3]	
D5_DDR1_DQ42	BA12	NC/NC/DDR1_DQ4[2]	
D5_DDR1_DQ43	BC12	NC/NC/DDR1_DQ4[1]	
D5_DDR1_DQ41	BB12	NC/NC/DDR1_DQ4[0]	
HT3 1 DDR_VREF_CA1	AH50	DDR_VREF_CA1	
HT4 1 DDR_VREF_CA0	AH52	DDR_VREF_CA0	

Signal	Pin	Signal	Pin
		DDR0_CLKP3/DDR1_CLKP0	BC22
		DDR0_CLKN3/DDR1_CLKN0	BB22
		DDR0_CLKP2/DDR1_CLKP1	BD23
		DDR0_CLKN2/DDR1_CLKN1	BC23
		DDR0_CLKP1/DDR0_CLKP1	BC28
		DDR0_CLKN1/DDR0_CLKN1	BB28
		DDR0_CLKP0/DDR0_CLKP0	BD29
		DDR0_CLKN0/DDR0_CLKN0	BC29
		DDR0_CKE3/NC	BD37
		DDR0_CKE2/DDR0_CS1	BB36
		DDR0_CKE1/DDR0_CS3	BA37
		DDR0_CKE0/DDR0_CS0	BC36
		DDR0_CS3/DDR1_CS0	BD15
		DDR0_CS2/DDR1_CA5	BB18
		DDR0_CS1/DDR1_CA0	BB16
		DDR0_CS0/DDR1_CA6	BC18
		DDR0_ODT3/NC	BB14
		DDR0_ODT2/DDR1_CA1	BC16
		DDR0_ODT1/DDR1_CS1	BA16
		DDR0_ODT0/DDR1_CA3	BD17
		DDR0_BA1/DDR1_CA11	BC20
		DDR0_BA0/DDR1_CA9	BA20
		DDR0_BG1/DDR0_CA2	BC35
		DDR0_BG0/DDR0_CA1	BD35
		DDR0_MA16/DDR1_CA8	BD19
		DDR0_MA15/DDR1_CA4	BA18
		DDR0_MA14/DDR1_CA7	BC19
		DDR0_MA13/DDR1_CA2	BC17
		DDR0_MA12/DDR0_CA3	BC34
		DDR0_MA11/DDR0_CA5	BA33
		DDR0_MA10/DDR1_CA10	BB20
		DDR0_MA9/DDR0_CA4	BB34
		DDR0_MA8/DDR0_CA7	BC33
		DDR0_MA7/DDR0_CA6	BD33
		DDR0_MA6/DDR0_CA8	BC32
		DDR0_MA5/DDR0_CA9	BB32
		DDR0_MA4/DDR0_CA10	BA31
		DDR0_MA3/DDR0_CA11	BD31
		DDR0_MA2/NC	BC30
		DDR0_MA1/DDR0_CA12	BC31
		DDR0_MA0/DDR1_CA12	BC21
		DDR0_ACT#/DDR0_CA0	BA35
		DDR0_PAR/NC	BD21
		DDR0_ALERT#	AP25
		DDR4 (IL) / DDR4 (NIL) / DDR5	
DDR0_DQSP7/	AM4	DDR1_DQSP5/DDR1_DQSP3	AN4
DDR0_DQSN7/	AM4	DDR1_DQSN5/DDR1_DQSN3	AU4
DDR0_DQSP6/	AU4	DDR1_DQSP4/DDR1_DQSP2	AV4
DDR0_DQSN6/	AV4	DDR1_DQSN4/DDR1_DQSN2	BA4
DDR0_DQSP5/	BA4	DDR1_DQSP1/DDR1_DQSP1	BA5
DDR0_DQSN5/	BA5	DDR1_DQSN1/DDR1_DQSN1	BA8
DDR0_DQSP4/	BA8	DDR1_DQSP0/DDR1_DQSP0	BA9
DDR0_DQSN4/	BA9	DDR1_DQSN0/DDR1_DQSN0	BA45
DDR0_DQSP3/	BA45	DDR0_DQSP5/DDR0_DQSP3	BA46
DDR0_DQSN3/	BA46	DDR0_DQSN5/DDR0_DQSN3	BA49
DDR0_DQSP2/	BA49	DDR0_DQSP4/DDR0_DQSP2	AY49
DDR0_DQSN2/	AY49	DDR0_DQSN4/DDR0_DQSN2	AU49
DDR0_DQSP1/	AU49	DDR0_DQSP1/DDR0_DQSP1	AT49
DDR0_DQSN1/	AT49	DDR0_DQSN1/DDR0_DQSN1	AM49
DDR0_DQSP0/	AM49	DDR0_DQSP0/DDR0_DQSP0	AL49
DDR0_DQSN0/	AL49	DDR0_DQSN0/DDR0_DQSN0	
DDR0_DQSP8/	BA40	DDR0_DQSP8/DDR0_DQSP4	BA40
DDR0_DQSN8/	BA41	DDR0_DQSN8/DDR0_DQSN4	BA41
		NC/NC/DDR1_DQSP4	BC13
		NC/NC/DDR1_DQSN4	BD13
		NC/DDR3_CS3	AU20
		NC/DDR3_CS2	AV20
		NC/DDR2_CS2	AW33
		NC/DDR1_CS3	BA15
		NC/DDR1_CS2	BC15
		NC/DDR0_CS2	BC37

Signal	Pin
D5_DDR1_CLK0	13
D5_DDR1_CLK#0	13
D5_DDR1_CLK1	13
D5_DDR1_CLK#1	13
D5_DDR0_CLK1	13
D5_DDR0_CLK#1	13
D5_DDR0_CLK0	13
D5_DDR0_CLK#0	13
D5_DDR0_CS#1	13
D5_DDR0_CS#3	14
D5_DDR0_CS#0	13
D5_DDR1_CS#0	13
D5_DDR1_CA5	13,14
D5_DDR1_CA0	13,14
D5_DDR1_CA6	13,14
D5_DDR1_CA1	13,14
D5_DDR1_CS#1	13
D5_DDR1_CA3	13,14
D5_DDR1_CA11	13,14
D5_DDR1_CA9	13,14
D5_DDR0_CA2	13,14
D5_DDR0_CA1	13,14
D5_DDR1_CA8	13,14
D5_DDR1_CA4	13,14
D5_DDR1_CA7	13,14
D5_DDR1_CA2	13,14
D5_DDR0_CA3	13,14
D5_DDR0_CA5	13,14
D5_DDR1_CA10	13,14
D5_DDR0_CA4	13,14
D5_DDR0_CA7	13,14
D5_DDR0_CA6	13,14
D5_DDR0_CA8	13,14
D5_DDR0_CA9	13,14
D5_DDR0_CA10	13,14
D5_DDR0_CA11	13,14
D5_DDR0_CA12	13,14
D5_DDR1_CA12	13,14
D5_DDR0_CA0	13,14
DDR0_ALERT#	13,14
D5_DDR1_DQS3	13,14
D5_DDR1_DQS#3	13,14
D5_DDR1_DQS2	13,14
D5_DDR1_DQS#2	13,14
D5_DDR1_DQS1	13,14
D5_DDR1_DQS#1	13,14
D5_DDR1_DQS0	13,14
D5_DDR1_DQS#0	13,14
D5_DDR0_DQS3	13,14
D5_DDR0_DQS#3	13,14
D5_DDR0_DQS2	13,14
D5_DDR0_DQS#2	13,14
D5_DDR0_DQS1	13,14
D5_DDR0_DQS#1	13,14
D5_DDR0_DQS0	13,14
D5_DDR0_DQS#0	13,14
D5_DDR0_DQS4	13,14
D5_DDR0_DQS#4	13,14
D5_DDR1_DQS4	13,14
D5_DDR1_DQS#4	13,14
D5_DDR3_CS#3	16
D5_DDR3_CS#2	16
D5_DDR2_CS#2	16
D5_DDR1_CS#3	14
D5_DDR1_CS#2	14
D5_DDR0_CS#2	14

NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8
1 2 3 4 5 6 7 8

SOCKET_1700P
FOXCONN/PE17001-11AJ1-1H
12001-00300400

LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H
2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C

ASUS	Title: LGA1700 (DDR5_CH 0/1)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 7 of 90	

Channel 2/3
6 Layer routing

DDR4(IL) / DDR4(NIL) / DDR5 DDR4 / DDR5

LGA1700B

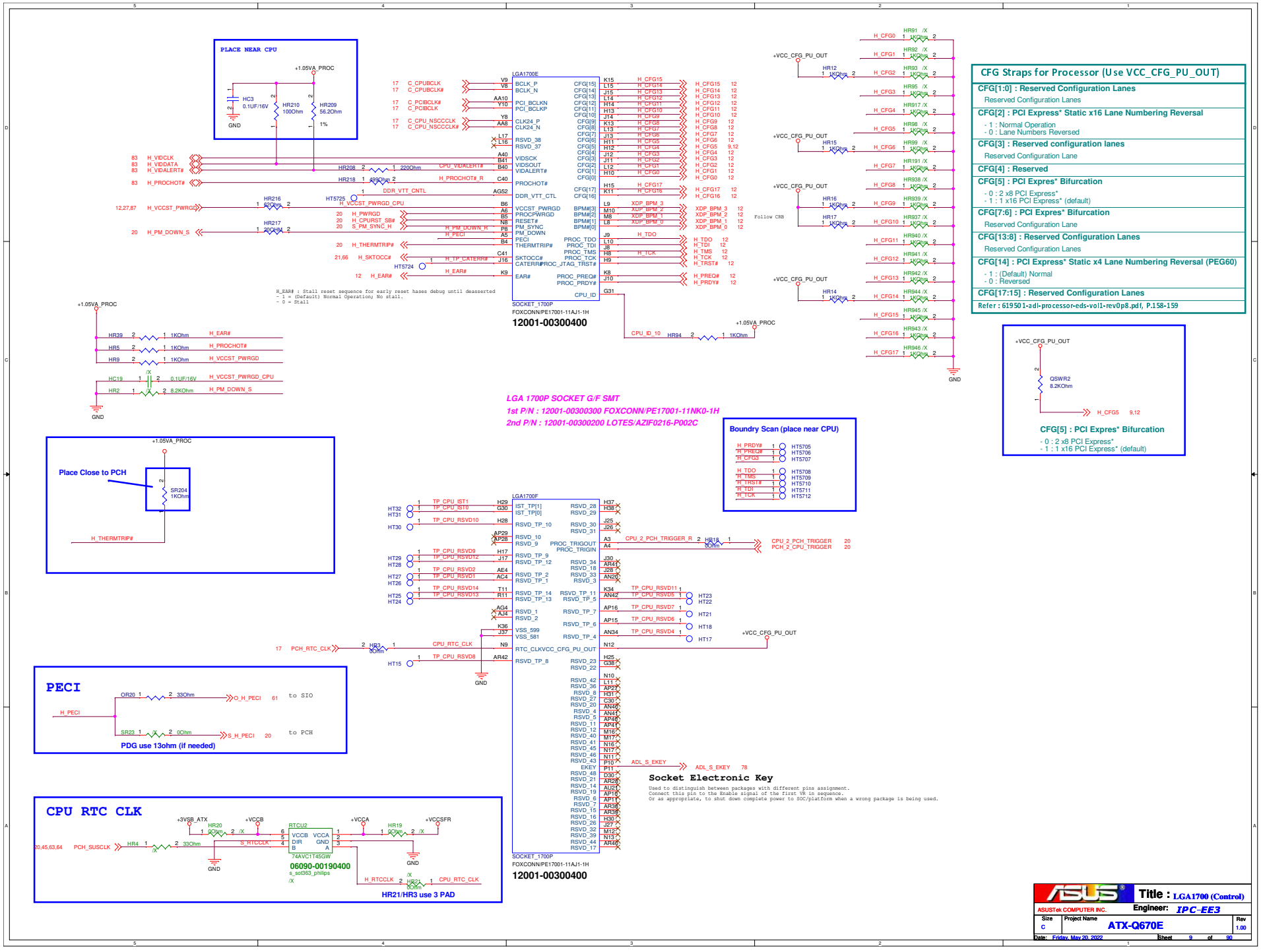
15,16	D5_DDR3_DQ3[0:7]	D5_DDR3_DQ35	AL7	DDR1_DQ7[7]/DDR1_DQ7[7]	/DDR3_DQ3[7]	DDR1_CLKP3/DDR3_CLKP1	BD25
		D5_DDR3_DQ34	AM6	DDR1_DQ7[6]/DDR1_DQ7[6]	/DDR3_DQ3[6]	DDR1_CLKN3/DDR3_CLKN1	BC25
		D5_DDR3_DQ36	AL6	DDR1_DQ7[5]/DDR1_DQ7[5]	/DDR3_DQ3[5]	DDR1_CLKP2/DDR3_CLKP0	BC24
		D5_DDR3_DQ37	AL8	DDR1_DQ7[4]/DDR1_DQ7[4]	/DDR3_DQ3[4]	DDR1_CLKN2/DDR3_CLKN0	BB24
		D5_DDR3_DQ30	AP6	DDR1_DQ7[3]/DDR1_DQ7[3]	/DDR3_DQ3[3]	DDR1_CLKP1/DDR2_CLKP1	BC26
		D5_DDR3_DQ31	AN6	DDR1_DQ7[2]/DDR1_DQ7[2]	/DDR3_DQ3[2]	DDR1_CLKN1/DDR2_CLKN1	BB26
		D5_DDR3_DQ33	AP7	DDR1_DQ7[1]/DDR1_DQ7[1]	/DDR3_DQ3[1]	DDR1_CLKP0/DDR2_CLKP0	BD27
		D5_DDR3_DQ32	AP8	DDR1_DQ7[0]/DDR1_DQ7[0]	/DDR3_DQ3[0]	DDR1_CLKN0/DDR2_CLKN0	BC27
15,16	D5_DDR3_DQ2[0:7]	D5_DDR3_DQ24	AT7	DDR1_DQ6[7]/DDR1_DQ6[7]	/DDR3_DQ2[7]		
		D5_DDR3_DQ25	AT6	DDR1_DQ6[6]/DDR1_DQ6[6]	/DDR3_DQ2[6]	DDR1_CKE3/NC	AV33
		D5_DDR3_DQ26	AV6	DDR1_DQ6[5]/DDR1_DQ6[5]	/DDR3_DQ2[5]	DDR1_CKE2/DDR2_CS1	AT29
		D5_DDR3_DQ27	AU6	DDR1_DQ6[4]/DDR1_DQ6[4]	/DDR3_DQ2[4]	DDR1_CKE1/DDR2_CS3	AU32
		D5_DDR3_DQ23	AW6	DDR1_DQ6[3]/DDR1_DQ6[3]	/DDR3_DQ2[3]	DDR1_CKE0/DDR2_CS0	AV32
		D5_DDR3_DQ22	AV8	DDR1_DQ6[2]/DDR1_DQ6[2]	/DDR3_DQ2[2]		
		D5_DDR3_DQ20	AW8	DDR1_DQ6[1]/DDR1_DQ6[1]	/DDR3_DQ2[1]	DDR1_CS3/DDR3_CS0	AW22
		D5_DDR3_DQ21	AW7	DDR1_DQ6[0]/DDR1_DQ6[0]	/DDR3_DQ2[0]	DDR1_CS2/DDR3_CA5	AU24
15,16	D5_DDR3_DQ1[0:7]	D5_DDR3_DQ14	AW10	DDR1_DQ5[7]/DDR1_DQ3[7]	/DDR3_DQ1[7]	DDR1_CS1/DDR3_CA0	AU22
		D5_DDR3_DQ15	AV10	DDR1_DQ5[6]/DDR1_DQ3[6]	/DDR3_DQ1[6]	DDR1_CS0/DDR3_CA6	AV24
		D5_DDR3_DQ16	AW11	DDR1_DQ5[5]/DDR1_DQ3[5]	/DDR3_DQ1[5]		
		D5_DDR3_DQ17	AU10	DDR1_DQ5[4]/DDR1_DQ3[4]	/DDR3_DQ1[4]	DDR1_ODT3/NC	AW20
		D5_DDR3_DQ12	AT12	DDR1_DQ5[3]/DDR1_DQ3[3]	/DDR3_DQ1[3]	DDR1_ODT2/DDR3_CA1	AR26
		D5_DDR3_DQ10	AU12	DDR1_DQ5[2]/DDR1_DQ3[2]	/DDR3_DQ1[2]	DDR1_ODT1/DDR3_CS1	AW21
		D5_DDR3_DQ11	AW12	DDR1_DQ5[1]/DDR1_DQ3[1]	/DDR3_DQ1[1]	DDR1_ODT0/DDR3_CA3	AW24
		D5_DDR3_DQ13	AV12	DDR1_DQ5[0]/DDR1_DQ3[0]	/DDR3_DQ1[0]		
15,16	D5_DDR3_DQ0[0:7]	D5_DDR3_DQ07	AT14	DDR1_DQ4[7]/DDR1_DQ2[7]	/DDR3_DQ0[7]	DDR1_BA1/DDR3_CA11	AV26
		D5_DDR3_DQ06	AU14	DDR1_DQ4[6]/DDR1_DQ2[6]	/DDR3_DQ0[6]	DDR1_BA0/DDR3_CA9	AW25
		D5_DDR3_DQ05	AW14	DDR1_DQ4[5]/DDR1_DQ2[5]	/DDR3_DQ0[5]		
		D5_DDR3_DQ04	AV14	DDR1_DQ4[4]/DDR1_DQ2[4]	/DDR3_DQ0[4]	DDR1_BG1/DDR2_CA2	AW31
		D5_DDR3_DQ01	AW15	DDR1_DQ4[3]/DDR1_DQ2[3]	/DDR3_DQ0[3]	DDR1_BG0/DDR2_CA1	AW32
		D5_DDR3_DQ00	AU16	DDR1_DQ4[2]/DDR1_DQ2[2]	/DDR3_DQ0[2]		
		D5_DDR3_DQ02	AW16	DDR1_DQ4[1]/DDR1_DQ2[1]	/DDR3_DQ0[1]	DDR1_MA16/DDR3_CA8	AW26
		D5_DDR3_DQ03	AV16	DDR1_DQ4[0]/DDR1_DQ2[0]	/DDR3_DQ0[0]	DDR1_MA15/DDR3_CA4	AW23
15,16	D5_DDR2_DQ3[0:7]	D5_DDR2_DQ39	AW40	DDR1_DQ3[7]/DDR0_DQ7[7]	/DDR2_DQ3[7]	DDR1_MA14/DDR3_CA7	AT25
		D5_DDR2_DQ38	AW39	DDR1_DQ3[6]/DDR0_DQ7[6]	/DDR2_DQ3[6]	DDR1_MA13/DDR3_CA2	AU23
		D5_DDR2_DQ37	AU39	DDR1_DQ3[5]/DDR0_DQ7[5]	/DDR2_DQ3[5]	DDR1_MA12/DDR2_CA3	AU30
		D5_DDR2_DQ35	AV39	DDR1_DQ3[4]/DDR0_DQ7[4]	/DDR2_DQ3[4]	DDR1_MA11/DDR2_CA5	AU29
		D5_DDR2_DQ36	AW42	DDR1_DQ3[3]/DDR0_DQ7[3]	/DDR2_DQ3[3]	DDR1_MA10/DDR3_CA10	AU25
		D5_DDR2_DQ34	AW41	DDR1_DQ3[2]/DDR0_DQ7[2]	/DDR2_DQ3[2]	DDR1_MA9/DDR2_CA4	AV30
		D5_DDR2_DQ31	AV42	DDR1_DQ3[1]/DDR0_DQ7[1]	/DDR2_DQ3[1]	DDR1_MA8/DDR2_CA7	AW29
		D5_DDR2_DQ32	AU42	DDR1_DQ3[0]/DDR0_DQ7[0]	/DDR2_DQ3[0]	DDR1_MA7/DDR2_CA6	AW30
15,16	D5_DDR2_DQ2[0:7]	D5_DDR2_DQ29	AW45	DDR1_DQ2[7]/DDR0_DQ6[7]	/DDR2_DQ2[7]	DDR1_MA6/DDR2_CA8	AV28
		D5_DDR2_DQ27	AW44	DDR1_DQ2[6]/DDR0_DQ6[6]	/DDR2_DQ2[6]	DDR1_MA5/DDR2_CA9	AU26
		D5_DDR2_DQ28	AV44	DDR1_DQ2[5]/DDR0_DQ6[5]	/DDR2_DQ2[5]	DDR1_MA4/DDR2_CA10	AU27
		D5_DDR2_DQ26	AW46	DDR1_DQ2[4]/DDR0_DQ6[4]	/DDR2_DQ2[4]	DDR1_MA3/DDR2_CA11	AW28
		D5_DDR2_DQ24	AW47	DDR1_DQ2[3]/DDR0_DQ6[3]	/DDR2_DQ2[3]	DDR1_MA2/NC	AT27
		D5_DDR2_DQ25	AU44	DDR1_DQ2[2]/DDR0_DQ6[2]	/DDR2_DQ2[2]	DDR1_MA1/DDR2_CA12	AW27
		D5_DDR2_DQ20	AU47	DDR1_DQ2[1]/DDR0_DQ6[1]	/DDR2_DQ2[1]	DDR1_MA0/DDR3_CA12	AU26
		D5_DDR2_DQ22	AV47	DDR1_DQ2[0]/DDR0_DQ6[0]	/DDR2_DQ2[0]		
15,16	D5_DDR2_DQ1[0:7]	D5_DDR2_DQ15	AR45	DDR1_DQ1[7]/DDR0_DQ3[7]	/DDR2_DQ1[7]	DDR1_ACT#/DDR2_CA0	AU31
		D5_DDR2_DQ17	AR44	DDR1_DQ1[6]/DDR0_DQ3[6]	/DDR2_DQ1[6]	DDR1_PAR/NC	AR27
		D5_DDR2_DQ19	AR47	DDR1_DQ1[5]/DDR0_DQ3[5]	/DDR2_DQ1[5]	DDR1_ALERT#	AP26
		D5_DDR2_DQ14	AR46	DDR1_DQ1[4]/DDR0_DQ3[4]	/DDR2_DQ1[4]		
		D5_DDR2_DQ10	AN46	DDR1_DQ1[3]/DDR0_DQ3[3]	/DDR2_DQ1[3]	DDR4(IL)/ DDR4(NIL)/ DDR5	AM8
		D5_DDR2_DQ11	AN45	DDR1_DQ1[2]/DDR0_DQ3[2]	/DDR2_DQ1[2]	DDR1_DQSP7/ DDR1_DQSP7/DDR3_DQSP3	AN8
		D5_DDR2_DQ12	AN47	DDR1_DQ1[1]/DDR0_DQ3[1]	/DDR2_DQ1[1]	DDR1_DQSN7/ DDR1_DQSN7/DDR3_DQSN3	AT8
15,16	D5_DDR2_DQ0[0:7]	D5_DDR2_DQ13	AP47	DDR1_DQ1[0]/DDR0_DQ3[0]	/DDR2_DQ1[0]	DDR1_DQSP6/ DDR1_DQSP6/DDR3_DQSP2	AU8
		D5_DDR2_DQ05	AL45	DDR1_DQ0[7]/DDR0_DQ2[7]	/DDR2_DQ0[7]	DDR1_DQSN6/ DDR1_DQSN6/DDR3_DQSN2	AT10
		D5_DDR2_DQ07	AL46	DDR1_DQ0[6]/DDR0_DQ2[6]	/DDR2_DQ0[6]	DDR1_DQSP5/ DDR1_DQSP3/DDR3_DQSP1	AT11
		D5_DDR2_DQ04	AK47	DDR1_DQ0[5]/DDR0_DQ2[5]	/DDR2_DQ0[5]	DDR1_DQSN5/ DDR1_DQSN3/DDR3_DQSN1	AT15
		D5_DDR2_DQ06	AL47	DDR1_DQ0[4]/DDR0_DQ2[4]	/DDR2_DQ0[4]	DDR1_DQSP4/ DDR1_DQSP2/DDR3_DQSP0	AT16
		D5_DDR2_DQ01	AH47	DDR1_DQ0[3]/DDR0_DQ2[3]	/DDR2_DQ0[3]	DDR1_DQSN4/ DDR1_DQSN2/DDR3_DQSN0	AU40
		D5_DDR2_DQ03	AJ47	DDR1_DQ0[2]/DDR0_DQ2[2]	/DDR2_DQ0[2]	DDR1_DQSP3/ DDR0_DQSP7/DDR2_DQSP3	AU41
		D5_DDR2_DQ00	AH45	DDR1_DQ0[1]/DDR0_DQ2[1]	/DDR2_DQ0[1]	DDR1_DQSN3/ DDR0_DQSN7/DDR2_DQSN3	AU45
		D5_DDR2_DQ02	AH46	DDR1_DQ0[0]/DDR0_DQ2[0]	/DDR2_DQ0[0]	DDR1_DQSP2/ DDR0_DQSP6/DDR2_DQSP2	AU46
						DDR1_DQSN2/ DDR0_DQSN6/DDR2_DQSN2	AP44
			AU35			DDR1_DQSP1/ DDR0_DQSP3/DDR2_DQSP1	AN44
			AV35	DDR1_DQ8[7]/DDR1_DQ8[7]/NC		DDR1_DQSN1/ DDR0_DQSN3/DDR2_DQSN1	AK45
			AW36	DDR1_DQ8[6]/DDR1_DQ8[6]/NC		DDR1_DQSP0/ DDR0_DQSP2/DDR2_DQSP0	AJ45
			AW35	DDR1_DQ8[5]/DDR1_DQ8[5]/NC		DDR1_DQSN0/ DDR0_DQSN2/DDR2_DQSN0	
15,16	D5_DDR2_DQ4[0:3]	D5_DDR2_DQ40	AV37	DDR1_DQ8[4]/DDR1_DQ8[4]/NC			AT35
		D5_DDR2_DQ42	AW37	DDR1_DQ8[3]/DDR1_DQ8[3]	/DDR2_DQ4[3]	DDR1_DQSP8/ DDR1_DQSP8/DDR2_DQSP4	AT36
		D5_DDR2_DQ41	AU37	DDR1_DQ8[2]/DDR1_DQ8[2]	/DDR2_DQ4[2]	DDR1_DQSN8/ DDR1_DQSN8/DDR2_DQSN4	
		D5_DDR2_DQ43	AT37	DDR1_DQ8[1]/DDR1_DQ8[1]	/DDR2_DQ4[1]		
				DDR1_DQ8[0]/DDR1_DQ8[0]	/DDR2_DQ4[0]	NC/NC/DDR3_DQSP4	AR18
15,16	D5_DDR3_DQ4[0:3]	D5_DDR3_DQ41	AV18			NC/NC/DDR3_DQSN4	AR19
		D5_DDR3_DQ42	AU18	NC/NC/DDR3_DQ4[3]			
		D5_DDR3_DQ43	AW18	NC/NC/DDR3_DQ4[2]		NC/DDR3_CLKP3	AP22
		D5_DDR3_DQ40	AT18	NC/NC/DDR3_DQ4[1]		NC/DDR3_CLKN3	AP21
				NC/NC/DDR3_DQ4[0]		NC/DDR3_CLKP2	AR21
HT19	1	DDR_VREF_CA3	AH49			NC/DDR3_CLKN2	AT21
HT20	1	DDR_VREF_CA2	AH51	DDR_VREF_CA3		NC/DDR2_CLKP3	AP32
				DDR_VREF_CA2		NC/DDR2_CLKN3	AP33
						NC/DDR2_CLKP2	AR33
						NC/DDR2_CLKN2	AT33
						NC/DDR1_CLKP3	AP24
						NC/DDR1_CLKN3	AR24
						NC/DDR1_CLKP2	AR23
						NC/DDR1_CLKN2	AT23
						NC/DDR0_CLKP3	AP30
						NC/DDR0_CLKN3	AR30
						NC/DDR0_CLKP2	AR31
						NC/DDR0_CLKN2	AT31

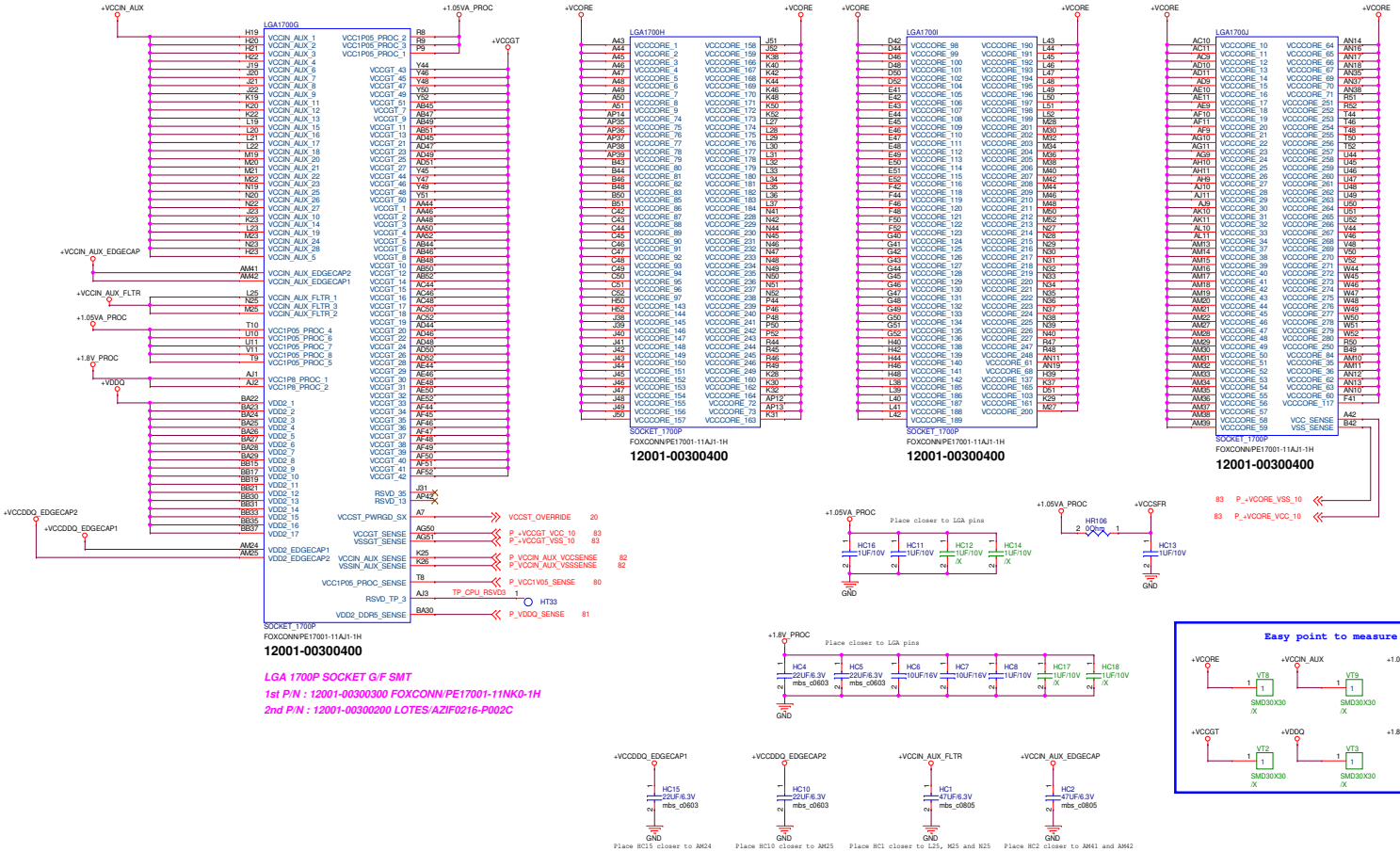
D5_DDR3_CLK1	15	D5_DDR2_CA0	15,16
D5_DDR3_CLK#1	15	DDR1_ALERT#	15,16
D5_DDR3_CLK0	15	D5_DDR3_DQS3	15,16
D5_DDR3_CLK#0	15	D5_DDR3_DQS#3	15,16
D5_DDR2_CLK1	15	D5_DDR3_DQS2	15,16
D5_DDR2_CLK#1	15	D5_DDR3_DQS#2	15,16
D5_DDR2_CLK0	15	D5_DDR3_DQS1	15,16
D5_DDR2_CLK#0	15	D5_DDR3_DQS#1	15,16
D5_DDR2_CS#1	15	D5_DDR3_DQS0	15,16
D5_DDR2_CS#3	16	D5_DDR3_DQS#0	15,16
D5_DDR2_CS#0	15	D5_DDR2_DQS3	15,16
D5_DDR3_CS#0	15	D5_DDR2_DQS#3	15,16
D5_DDR3_CA5	15,16	D5_DDR2_DQS2	15,16
D5_DDR3_CA0	15,16	D5_DDR2_DQS#2	15,16
D5_DDR3_CA6	15,16	D5_DDR2_DQS1	15,16
D5_DDR3_CA1	15,16	D5_DDR2_DQS#1	15,16
D5_DDR3_CS#1	15	D5_DDR2_DQS0	15,16
D5_DDR3_CA3	15,16	D5_DDR2_DQS#0	15,16
D5_DDR3_CA11	15,16	D5_DDR2_DQS4	15,16
D5_DDR3_CA9	15,16	D5_DDR2_DQS#4	15,16
D5_DDR2_CA2	15,16	D5_DDR3_DQS4	15,16
D5_DDR2_CA1	15,16	D5_DDR3_DQS#4	15,16
D5_DDR3_CA8	15,16	D5_DDR3_CLK3	16
D5_DDR3_CA4	15,16	D5_DDR3_CLK#3	16
D5_DDR3_CA7	15,16	D5_DDR3_CLK2	16
D5_DDR3_CA2	15,16	D5_DDR3_CLK#2	16
D5_DDR2_CA3	15,16	D5_DDR2_CLK3	16
D5_DDR2_CA5	15,16	D5_DDR2_CLK#3	16
D5_DDR3_CA10	15,16	D5_DDR2_CLK2	16
D5_DDR2_CA4	15,16	D5_DDR2_CLK#2	16
D5_DDR2_CA7	15,16	D5_DDR1_CLK3	14
D5_DDR2_CA6	15,16	D5_DDR1_CLK#3	14
D5_DDR2_CA8	15,16	D5_DDR1_CLK2	14
D5_DDR2_CA9	15,16	D5_DDR1_CLK#2	14
D5_DDR2_CA10	15,16	D5_DDR0_CLK3	14
D5_DDR2_CA11	15,16	D5_DDR0_CLK#3	14
D5_DDR2_CA12	15,16	D5_DDR0_CLK2	14
D5_DDR3_CA12	15,16	D5_DDR0_CLK#2	14

SOCKET_1700P
FOXCONN/PE17001-11AJ1-1H
12001-00300400

LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H
2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C

ASUS	Title: LGA1700 (DDR5_CH 2/3)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name ATX-Q670E		Rev 1.00
Date: Friday, May 20, 2022	Sheet 8 of 90		


PLACE NEAR CPU
+1.05VA_PROC
HC3 0.1UF/16V
HR210 100Ohm
HR209 56.2Ohm 1%
GND
LGA1700E
SOCKET_1700P
FOXCONN/PE17001-11AJ1-1H
12001-00300400
H_EAR# : Stall reset sequence for early reset hases debug until deasserted
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall
CFG Straps for Processor (Use VCC_CFG_PU_OUT)
CFG[1:0] : Reserved Configuration Lanes
Reserved Configuration Lanes
CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : Normal Operation
- 0 : Lane Numbers Reversed
CFG[3] : Reserved configuration lanes
Reserved Configuration Lane
CFG[4] : Reserved
CFG[5] : PCI Expres* Bifurcation
- 0 : 2 x8 PCI Express*
- 1 : 1 x16 PCI Express* (default)
CFG[7:6] : PCI Expres* Bifurcation
Reserved Configuration Lane
CFG[13:8] : Reserved Configuration Lanes
Reserved Configuration Lanes
CFG[14] : PCI Express* Static x4 Lane Numbering Reversal (PEG60)
- 1 : (Default) Normal
- 0 : Reversed
CFG[17:15] : Reserved Configuration Lanes
Refer : 619501-adl-processor-eds-vol1-rev0p8.pdf, P.158-159
+VCC_CFG_PU_OUT
QSWR2 8.2KOhm
CFG[5] : PCI Expres* Bifurcation
- 0 : 2 x8 PCI Express*
- 1 : 1 x16 PCI Express* (default)
LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H
2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C
Boundry Scan (place near CPU)
Place Close to PCH
SR204 1KOhm
H_THERMTRIP#
LGA1700F
SOCKET_1700P
FOXCONN/PE17001-11AJ1-1H
12001-00300400
PECI
H_PECI
OR20 33Ohm
SR23 0Ohm
to SIO
to PCH
PDG use 13ohm (if needed)
Socket Electronic Key
Used to distinguish between packages with different pins assignment.
Connect this pin to the Enable signal of the first VR in sequance.
Or as appropriate, to shut down complete power to SOC/platform when a wrong package is being used.
CPU RTC CLK
+3VSB_ATX
+VCCB
+VCCA
+VCCSFR
RTCU2
74AVC1T45GW
06090-00190400
s_sot363_philips
HR21/HR3 use 3 PAD
Title : LGA1700 (Control)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 9 of 90



LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H

2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C

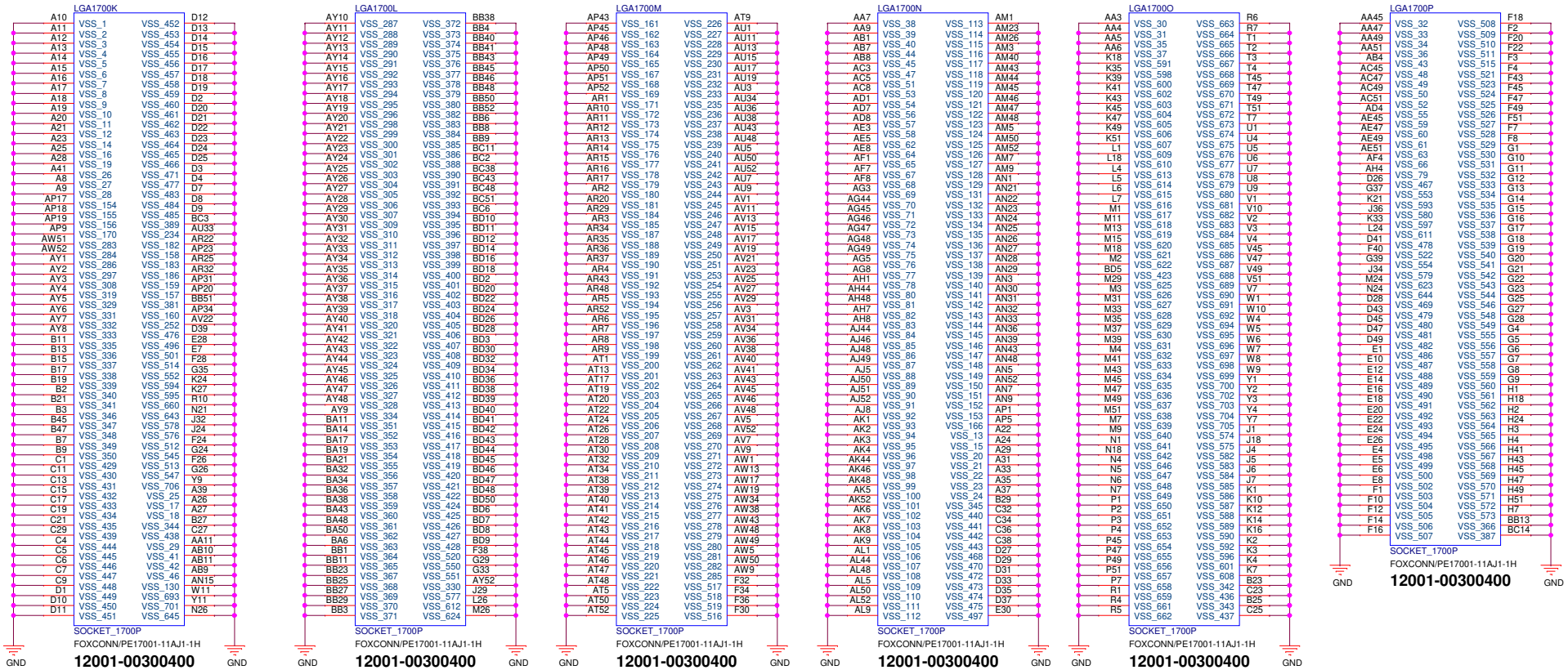
ASUSTeK COMPUTER INC.

Title : LGA1700 (POWER)

Engineer: IPC-EE3

Size	Project Name	Rev
A2	ATX-Q670E	1.00

Date: Friday, May 20, 2022 Sheet 10 of 90

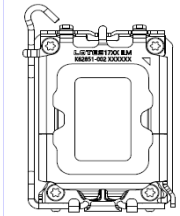


LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300300 FOXCONN/PE17001-11NK0-1H

2nd P/N : 12001-00300200 LOTES/AZIF0216-P002C

ILM



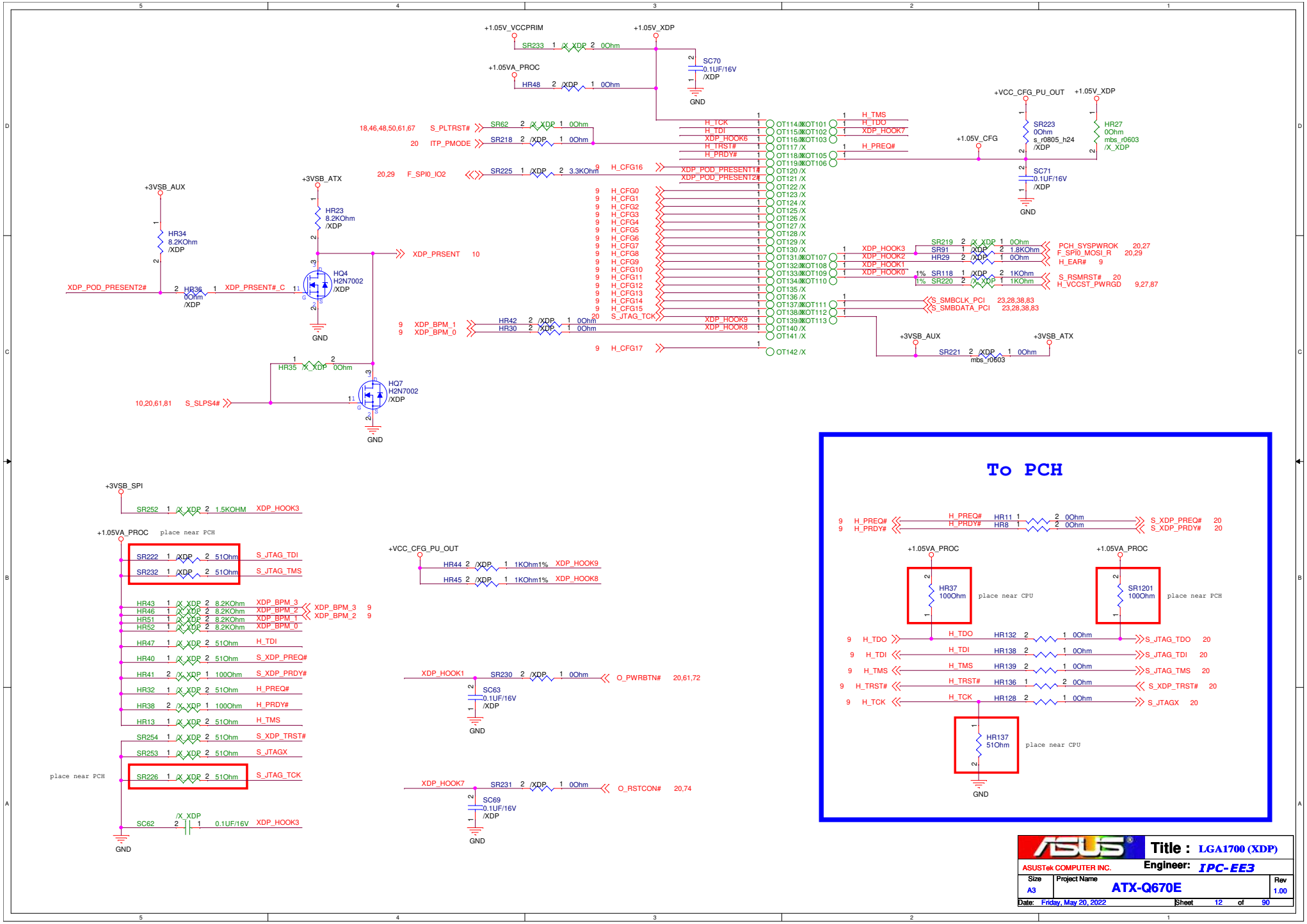
LGA1700_ILM_BP_COVER

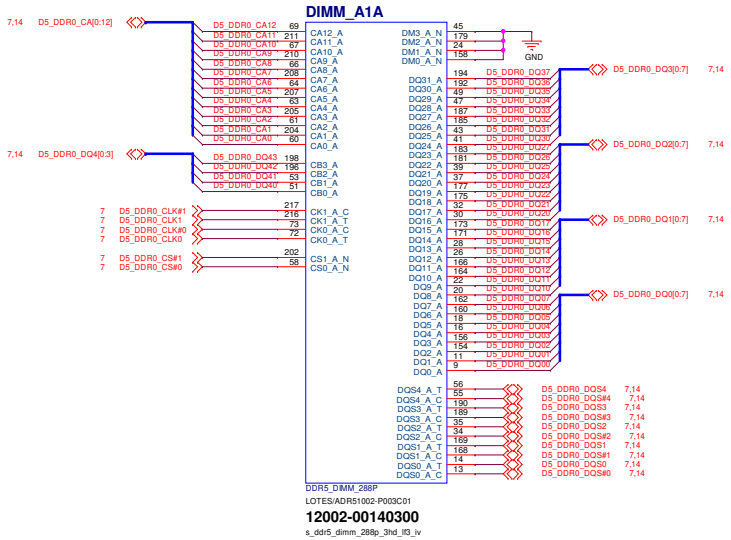
[HF]LOTES/AZIF0239-P001C

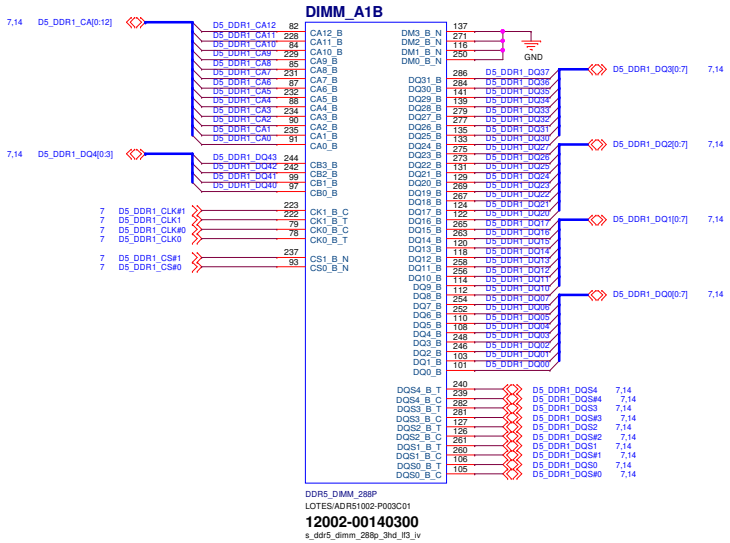
13021-00020100

ILM+COVER+BACKPLATE Module-LGA1700

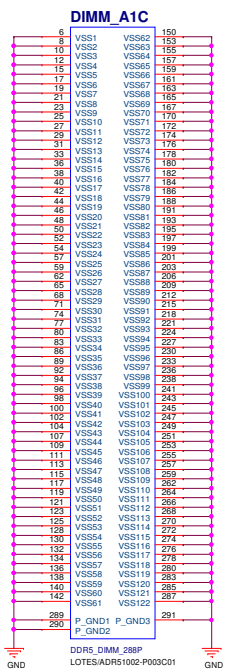
ASUS	Title : LGA1700 (GND)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 11 of 90	

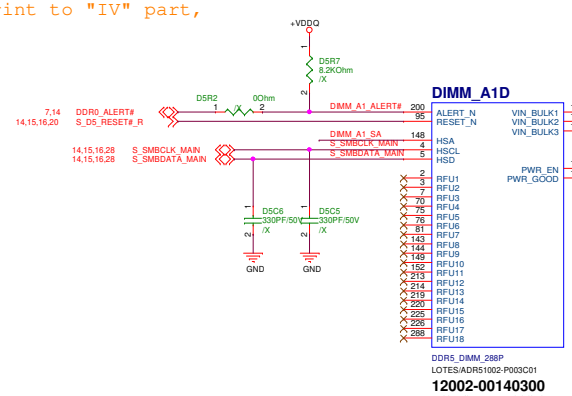

+1.05V_VCCPRIM
+1.05V_XDP
SR233 1 /X_XDP 2 0Ohm
SC70 0.1UF/16V /XDP
+1.05VA_PROC
HR48 2 /XDP 1 0Ohm
GND
+VCC_CFG_PU_OUT
+1.05V_XDP
SR223 0Ohm s_r0805_h24 /XDP
HR27 0Ohm mbs_r0603 /X_XDP
+1.05V_CFG
SC71 0.1UF/16V /XDP
18,46,48,50,61,67 S_PLTRST# SR62 2 /X_XDP 1 0Ohm
20 ITP_PMODE SR218 2 /XDP 1 0Ohm
20,29 F_SPI0_IO2 SR225 1 /XDP 2 3.3KOhm
H_TCK
H_TDI
XDP_HOOK6
H_TRST#
H_PRDY#
H_TMS
H_TDO
XDP_HOOK7
H_PREQ#
H_CFG16
XDP_POD_PRESENT1#
XDP_POD_PRESENT2#
H_CFG0
H_CFG1
H_CFG2
H_CFG3
H_CFG4
H_CFG5
H_CFG6
H_CFG7
H_CFG8
H_CFG9
H_CFG10
H_CFG11
H_CFG12
H_CFG13
H_CFG14
H_CFG15
S_JTAG_TCK
XDP_HOOK3
XDP_HOOK2
XDP_HOOK1
XDP_HOOK0
SR219 2 /X_XDP 1 0Ohm
SR91 1 /XDP 2 1.8KOhm
HR29 2 /XDP 1 0Ohm
PCH_SYSPWROK 20,27
F_SPI0_MOSI_R 20,29
H_EAR# 9
SR118 1 /XDP 2 1KOhm
SR220 2 /X_XDP 1 1KOhm
S_RSMRST# 20
H_VCCST_PWRGD 9,27,87
S_SMBCLK_PCI 23,28,38,83
S_SMBDATA_PCI 23,28,38,83
+3VSB_AUX
+3VSB_ATX
SR221 2 /XDP 1 0Ohm mbs_r0603
9 XDP_BPM_1 HR42 2 /XDP 1 0Ohm
9 XDP_BPM_0 HR30 2 /XDP 1 0Ohm
XDP_HOOK9
XDP_HOOK8
9 H_CFG17
+3VSB_AUX
HR34 8.2KOhm /XDP
+3VSB_ATX
HR23 8.2KOhm /XDP
XDP_PRSENT 10
XDP_POD_PRESENT2#
HR36 0Ohm /XDP
XDP_PRSENT#_C
HQ4 H2N7002 /XDP
GND
HR35 /X_XDP 0Ohm
HQ7 H2N7002 /XDP
10,20,61,81 S_SLPS4#
GND
+3VSB_SPI
SR252 1 /X_XDP 2 1.5KOHM XDP_HOOK3
+1.05VA_PROC place near PCH
SR222 1 /XDP 2 51Ohm S_JTAG_TDI
SR232 1 /XDP 2 51Ohm S_JTAG_TMS
HR43 1 /X_XDP 2 8.2KOhm XDP_BPM_3
HR46 1 /X_XDP 2 8.2KOhm XDP_BPM_2
HR51 1 /X_XDP 2 8.2KOhm XDP_BPM_1
HR52 1 /X_XDP 2 8.2KOhm XDP_BPM_0
XDP_BPM_3 9
XDP_BPM_2 9
HR47 1 /X_XDP 2 51Ohm H_TDI
HR40 1 /X_XDP 2 51Ohm S_XDP_PREQ#
HR41 2 /X_XDP 1 100Ohm S_XDP_PRDY#
HR32 1 /X_XDP 2 51Ohm H_PREQ#
HR38 2 /X_XDP 1 100Ohm H_PRDY#
HR13 1 /X_XDP 2 51Ohm H_TMS
SR254 1 /X_XDP 2 51Ohm S_XDP_TRST#
SR253 1 /X_XDP 2 51Ohm S_JTAGX
place near PCH
SR226 1 /X_XDP 2 51Ohm S_JTAG_TCK
/X_XDP
SC62 2 1 0.1UF/16V XDP_HOOK3
GND
+VCC_CFG_PU_OUT
HR44 2 /XDP 1 1KOhm1% XDP_HOOK9
HR45 2 /XDP 1 1KOhm1% XDP_HOOK8
XDP_HOOK1
SR230 2 /XDP 1 0Ohm O_PWRBTN# 20,61,72
SC63 0.1UF/16V /XDP
GND
XDP_HOOK7
SR231 2 /XDP 1 0Ohm O_RSTCON# 20,74
SC69 0.1UF/16V /XDP
GND
To PCH
9 H_PREQ# H_PREQ# HR11 1 2 0Ohm S_XDP_PREQ# 20
9 H_PRDY# H_PRDY# HR8 1 2 0Ohm S_XDP_PRDY# 20
+1.05VA_PROC
HR37 100Ohm place near CPU
+1.05VA_PROC
SR1201 100Ohm place near PCH
9 H_TDO H_TDO HR132 2 1 0Ohm S_JTAG_TDO 20
9 H_TDI H_TDI HR138 2 1 0Ohm S_JTAG_TDI 20
9 H_TMS H_TMS HR139 2 1 0Ohm S_JTAG_TMS 20
9 H_TRST# H_TRST# HR136 1 2 0Ohm S_XDP_TRST# 20
9 H_TCK H_TCK HR128 2 1 0Ohm S_JTAGX 20
HR137 51Ohm place near CPU
GND
ASUS
Title : LGA1700 (XDP)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 12 of 90

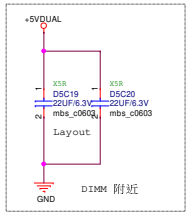


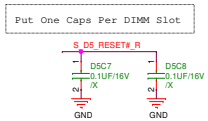


20220120 change the DDR5 Slot PCB Footprint to "IV" part,
let the layer2 DQ/DQS void









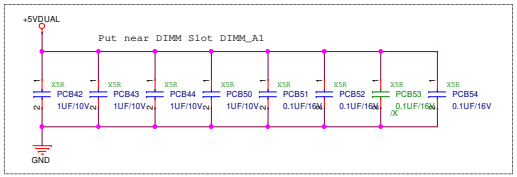


Table 91 — HSA Pin Resistor Value and ID - SPD5 Family

HSA Pin Connection	3-bit HID	Comment
10.0 KΩ to GND	HID = 000	1% Resistor
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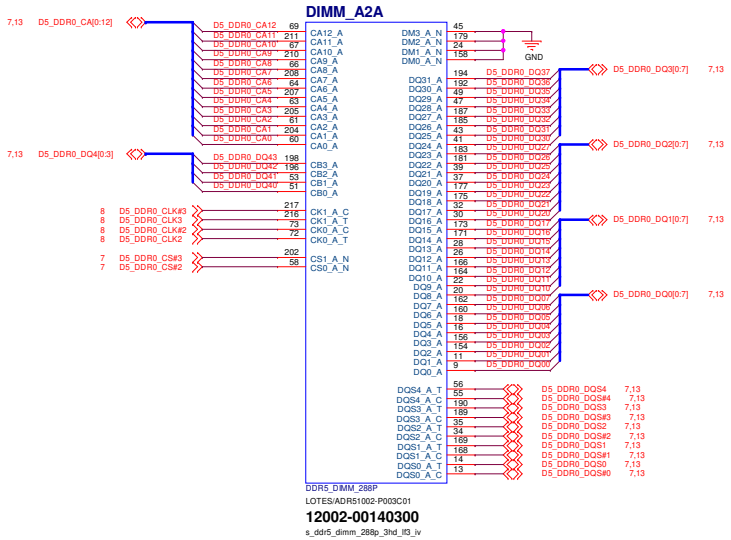
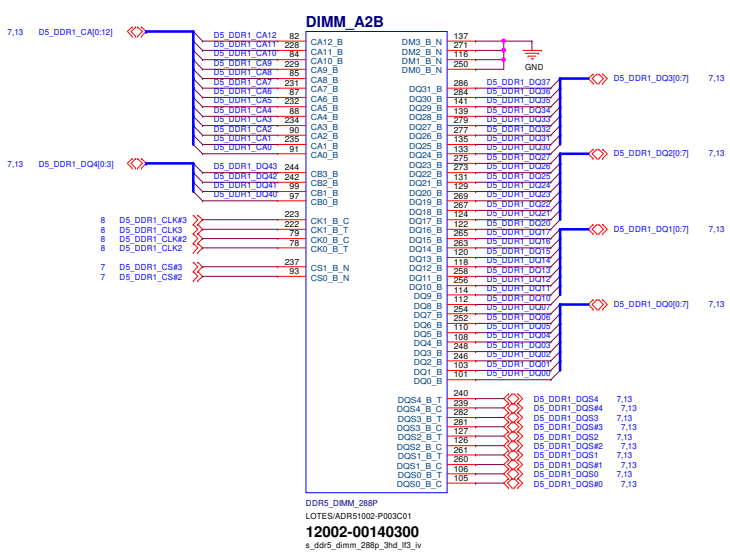
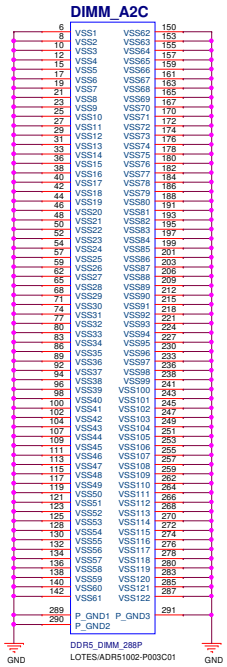
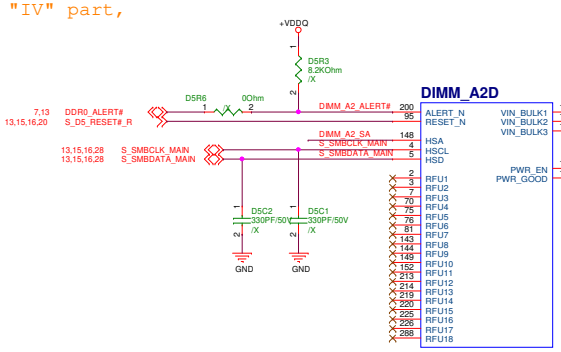
23.2 KΩ to GND	HID = 010	
35.7 KΩ to GND	HID = 011	
54.9 KΩ to GND	HID = 100	
84.5 KΩ to GND	HID = 101	
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

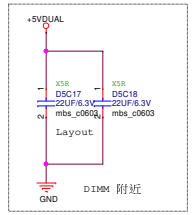


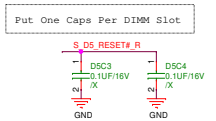


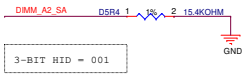
20220120 change the DDR5 Slot PCB Footprint to "IV" part,
let the layer2 DQ/DQS void

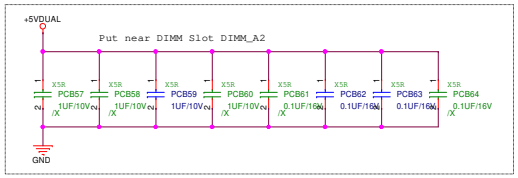












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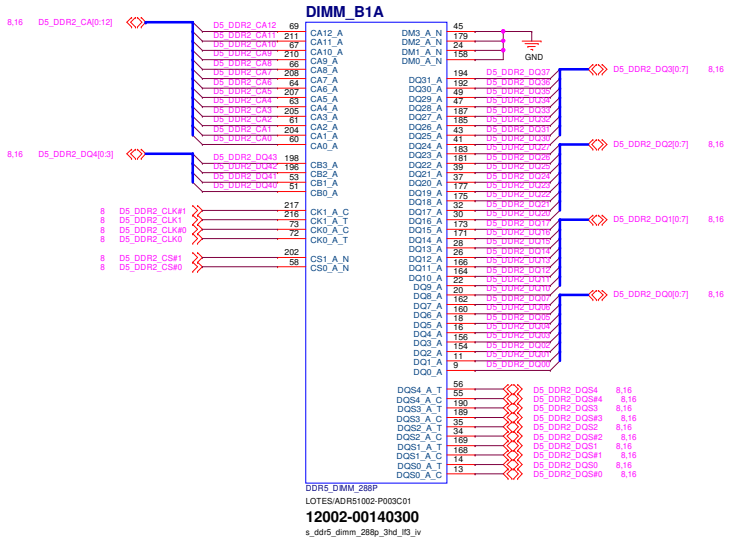
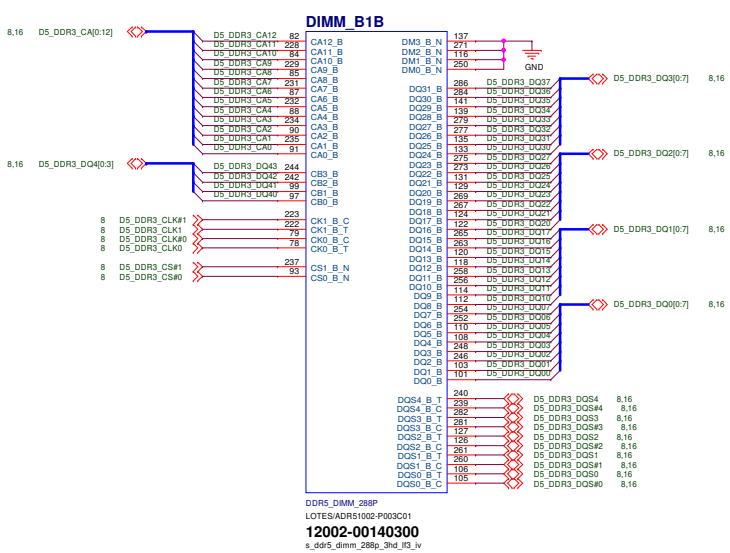
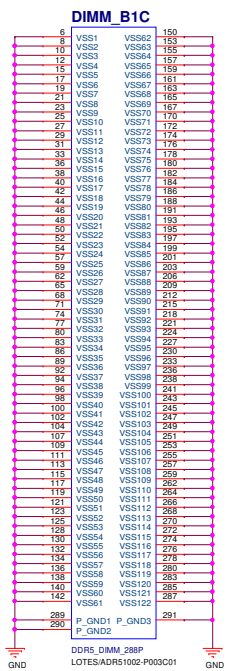
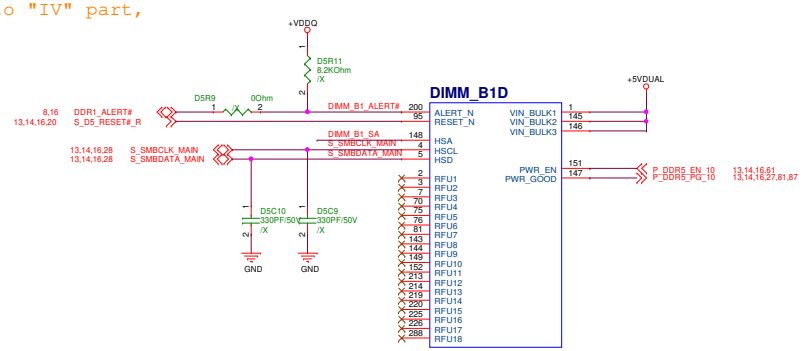
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

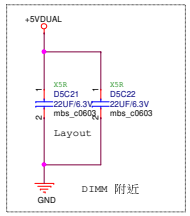


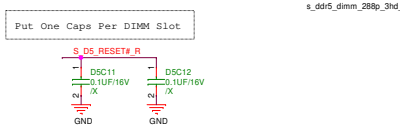


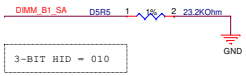
20220120 change the DDR5 Slot PCB Footprint to "IV" part,
let the layer2 DQ/DQS void

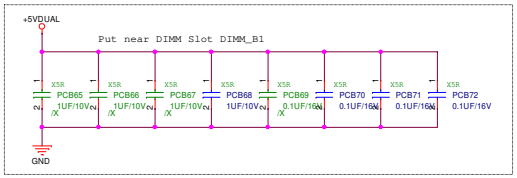












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127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

<Variant Name>

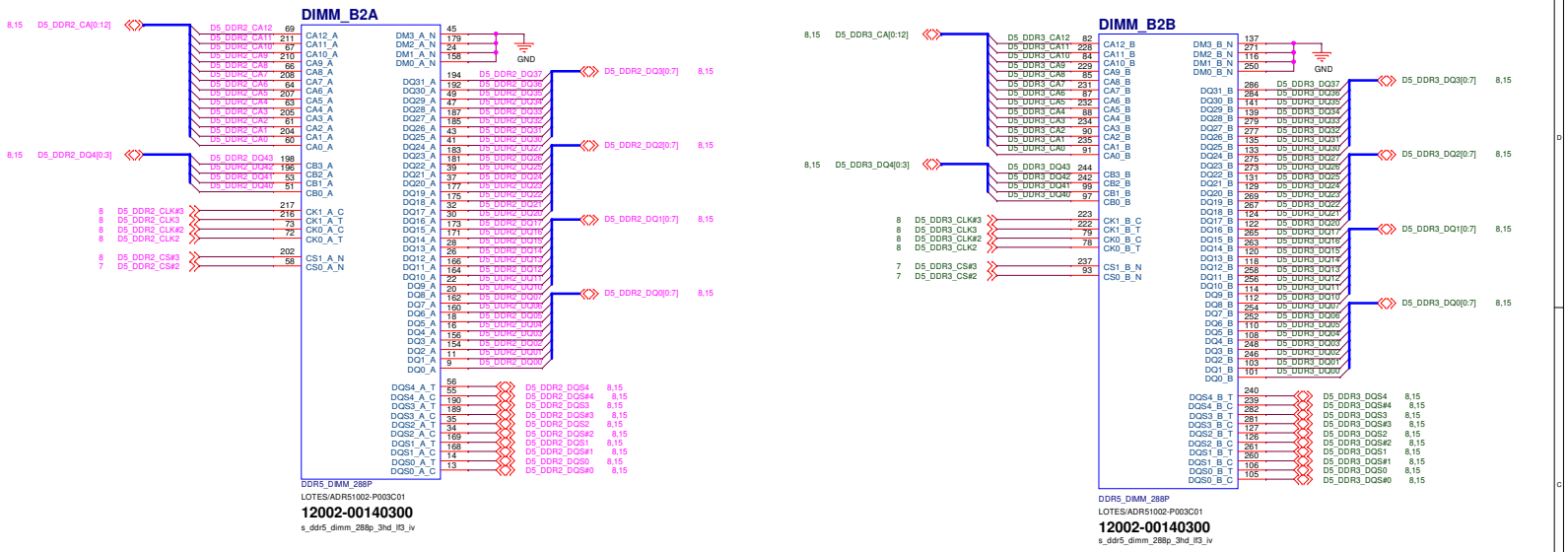
ASUSTeK COMPUTER INC.

Title : DDR5 DIMM B1

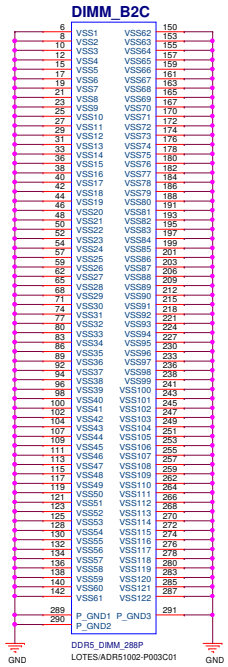
Engineer: IPC-EE3

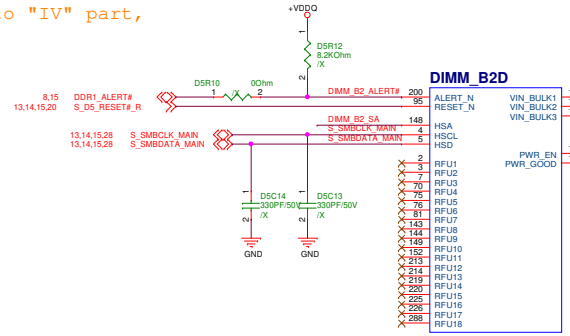
Size	Project Name	Rev
Custom	ATX-Q670E	1.00

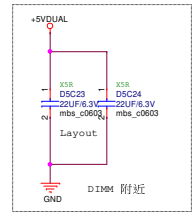
Date: Friday, May 20, 2022 Sheet 15 of 90

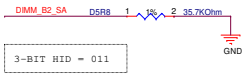


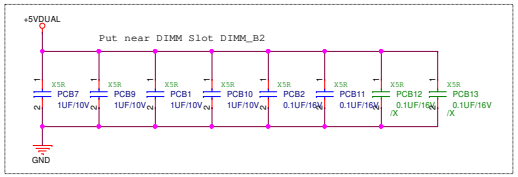
20220120 change the DDR5 Slot PCB Footprint to "IV" part,
let the layer2 DQ/DQS void











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84.5 KΩ to GND	HID = 101	
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

<Variant Name>

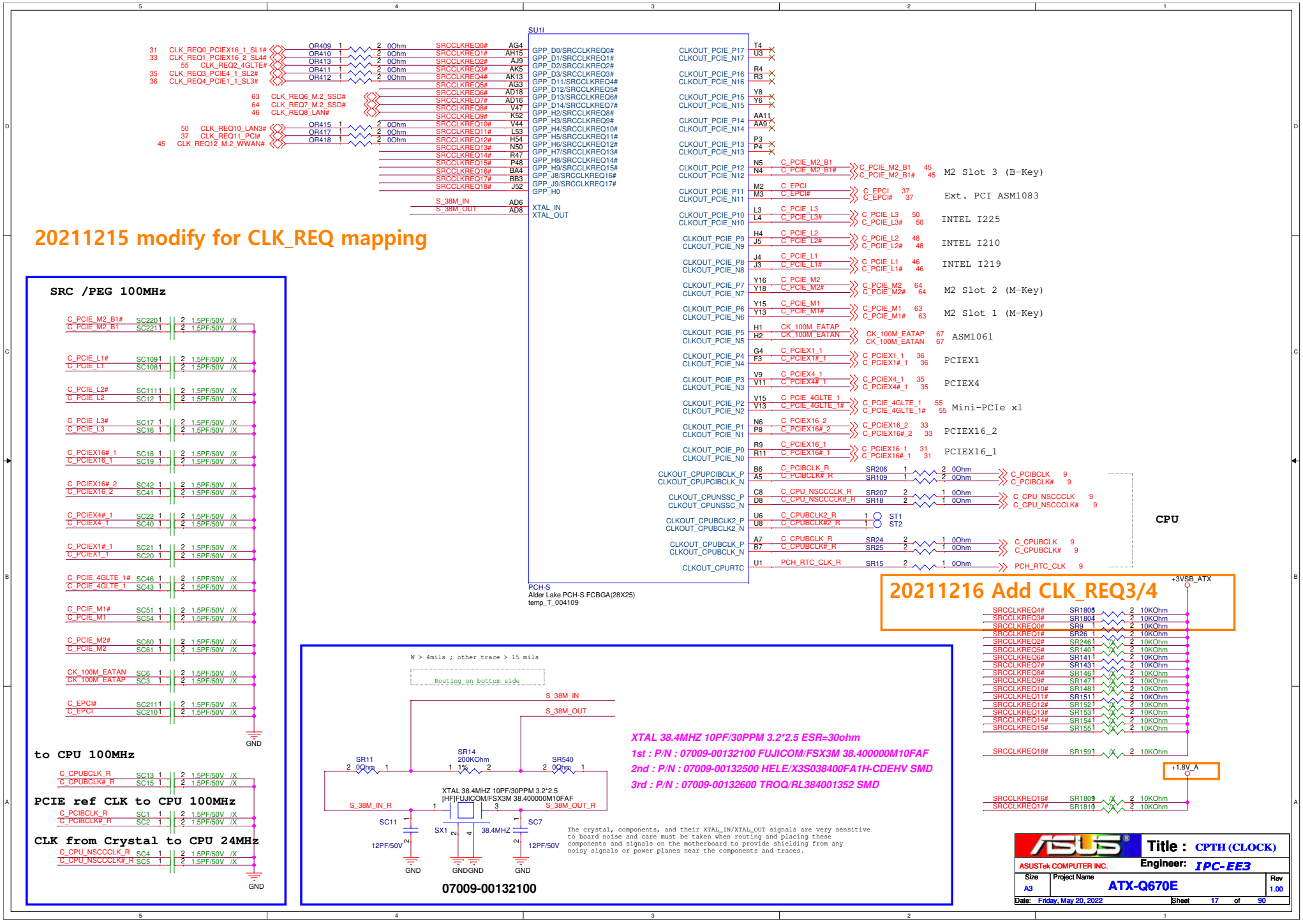
ASUSTeK COMPUTER INC.

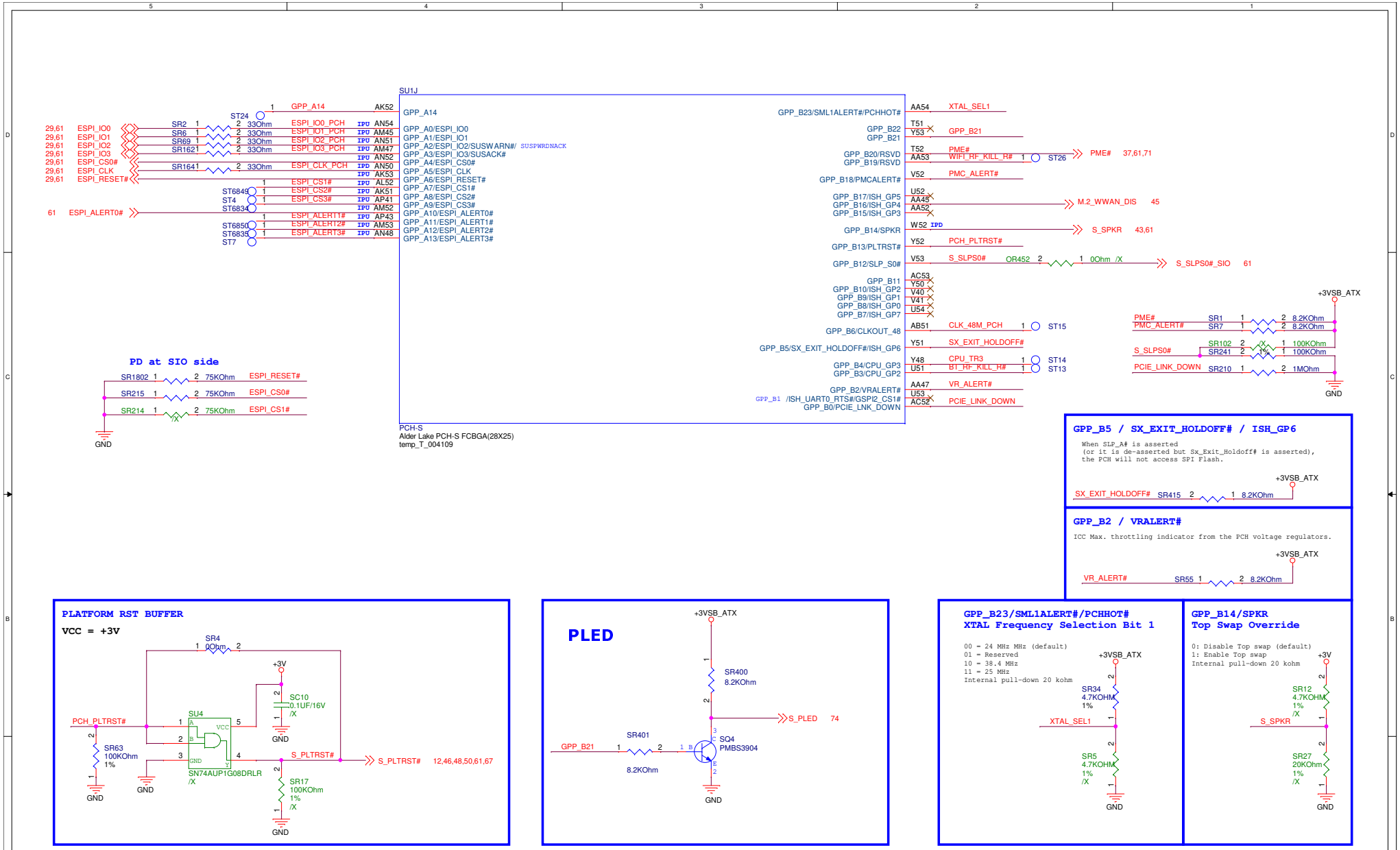
Title : DDR5 DIMM B2

Engineer: IPC-EE3

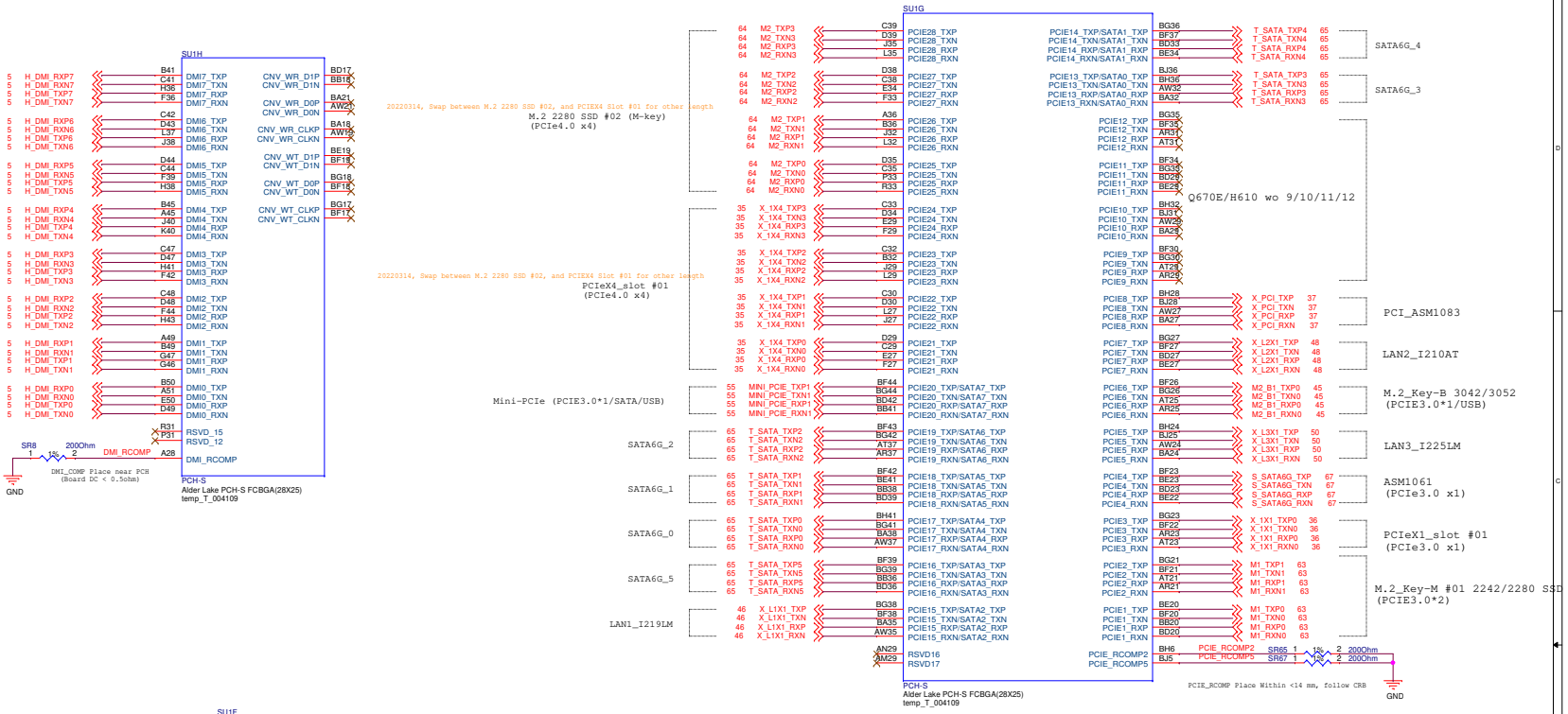
Size	Project Name	Rev
Custom	ATX-Q670E	1.00

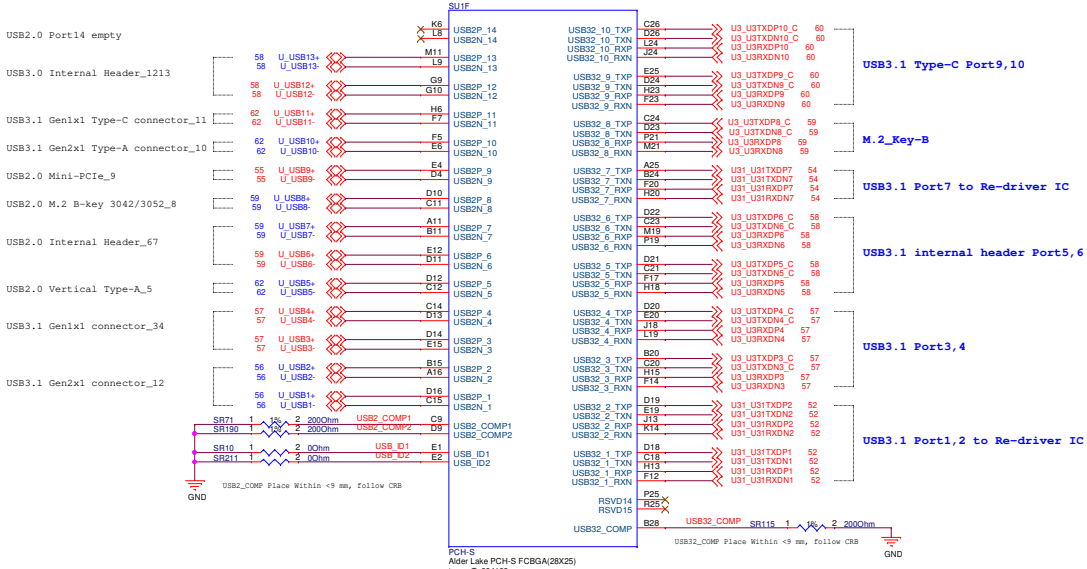
Date: Friday, May 20, 2022 Sheet 16 of 90


20211215 modify for CLK_REQ mapping
SU1I
PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109
M2 Slot 3 (B-Key)
Ext. PCI ASM1083
INTEL I225
INTEL I210
INTEL I219
M2 Slot 2 (M-Key)
M2 Slot 1 (M-Key)
ASM1061
PCIEX1
PCIEX4
Mini-PCIe x1
PCIEX16_2
PCIEX16_1
CPU
20211216 Add CLK_REQ3/4
+3VSB_ATX
+1.8V_A
SRCCLKREQ4# SR1805 2 10KOhm
SRCCLKREQ3# SR1804 2 10KOhm
SRCCLKREQ0# SR9 1 2 10KOhm
SRCCLKREQ1# SR26 1 2 10KOhm
SRCCLKREQ2# SR2461 2 10KOhm
SRCCLKREQ5# SR1401 2 10KOhm
SRCCLKREQ6# SR1411 2 10KOhm
SRCCLKREQ7# SR1431 2 10KOhm
SRCCLKREQ8# SR1461 2 10KOhm
SRCCLKREQ9# SR1471 2 10KOhm
SRCCLKREQ10# SR1481 2 10KOhm
SRCCLKREQ11# SR1511 2 10KOhm
SRCCLKREQ12# SR1521 2 10KOhm
SRCCLKREQ13# SR1531 2 10KOhm
SRCCLKREQ14# SR1541 2 10KOhm
SRCCLKREQ15# SR1551 2 10KOhm
SRCCLKREQ18# SR1591 2 10KOhm
SRCCLKREQ16# SR1809 2 10KOhm
SRCCLKREQ17# SR1810 2 10KOhm
SRC /PEG 100MHz
to CPU 100MHz
PCIE ref CLK to CPU 100MHz
CLK from Crystal to CPU 24MHz
GND
W > 4mils ; other trace > 15 mils
Routing on bottom side
S_38M_IN
S_38M_OUT
SR11 2 0Ohm 1
SR14 200KOhm 1 1% 2
SR540 2 0Ohm 1
XTAL 38.4MHZ 10PF/30PPM 3.2*2.5
[HF]FUJICOM/FSX3M 38.400000M10FAF
S_38M_IN_R
S_38M_OUT_R
SC11
SX1
38.4MHZ
SC7
12PF/50V
XTAL 38.4MHZ 10PF/30PPM 3.2*2.5 ESR=30ohm
1st : P/N : 07009-00132100 FUJICOM/FSX3M 38.400000M10FAF
2nd : P/N : 07009-00132500 HELE/X3S038400FA1H-CDEHV SMD
3rd : P/N : 07009-00132600 TROQ/RL384001352 SMD
The crystal, components, and their XTAL_IN/XTAL_OUT signals are very sensitive to board noise and care must be taken when routing and placing these components and signals on the motherboard to provide shielding from any noisy signals or power planes near the components and traces.
07009-00132100
Title : CPTH (CLOCK)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 17 of 90



ASUSTek COMPUTER INC.	Title : CPTH (eSPI/ISH)		
	Engineer: IPC-EE3		
Size A3	Project Name ATX-Q670E		Rev 1.00
Date: Friday, May 20, 2022	Sheet 18 of 90		

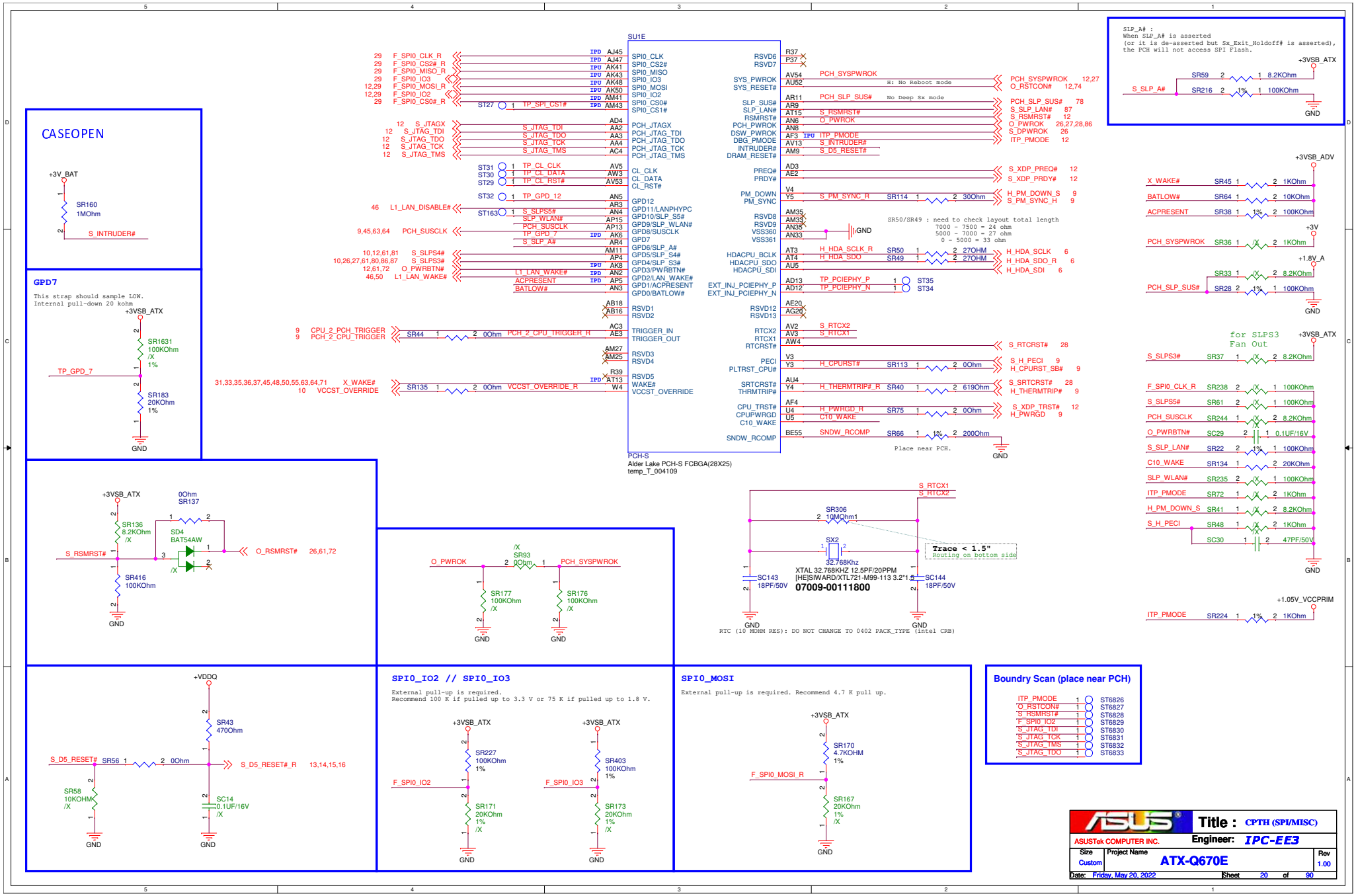


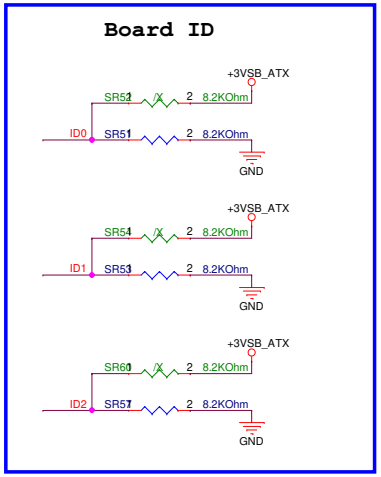


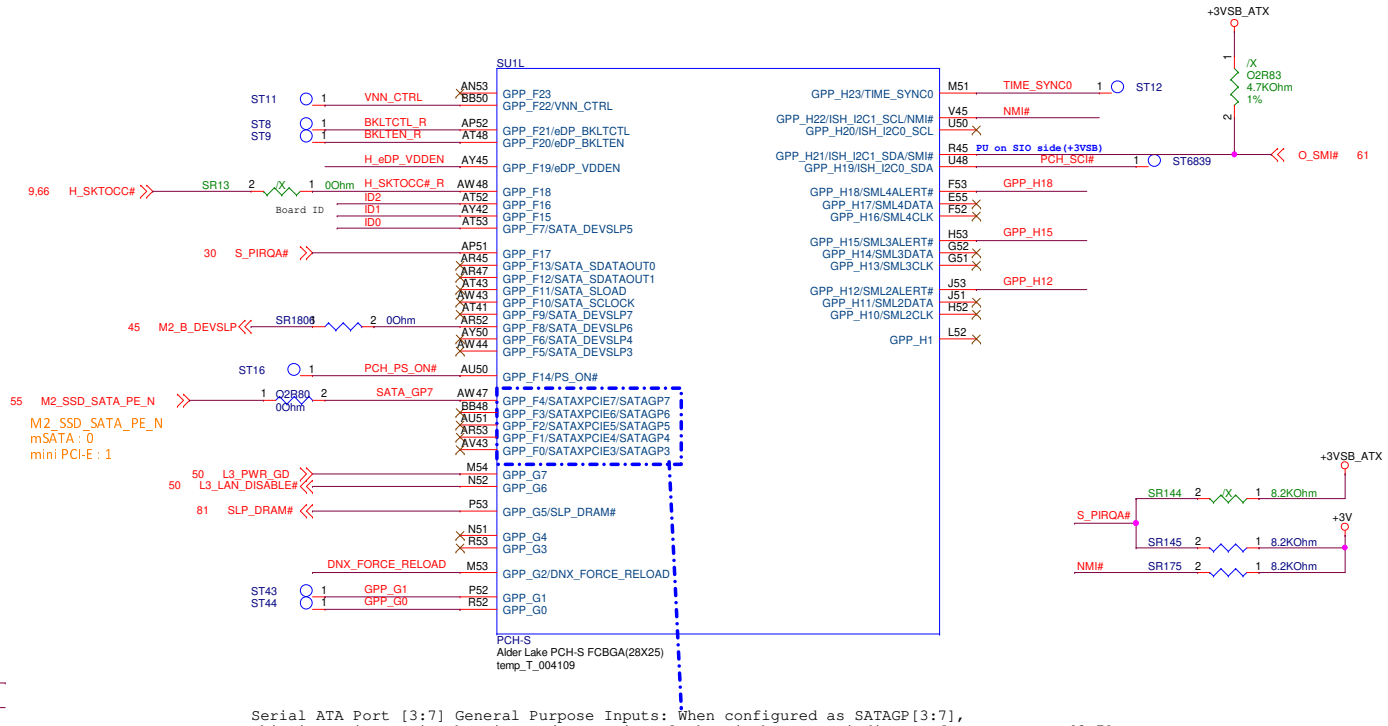
ADL PCH-S Supported PCI Express* Link Configurations

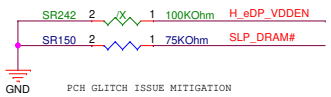
PCH-S	North PGS - Flex HSIO Lanes																				South PD - Flex HSIO Lanes							
Flex I/O Lanes	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
PCIe Controllers	1				2				3				4				5				6				7			
PCIe Max Rate	Gen3				Gen3				Gen3				Gen4				Gen3				Gen4				Gen4			
PCIe Lanes	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Logical Link Lanes: 1x4	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
2x2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2x2 LR	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
4x1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Assigned Root Ports: 1x4	RP1				RP5				RP9				RP13				RP17				RP21				RP25			
1x4 LR	RP1				RP5				RP9				RP13				RP17				RP21				RP25			
2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15		RP17		RP19		RP21		RP23		RP25		RP27	
2x2 LR	RP3		RP1		RP7		RP5		RP11		RP9		RP15		RP13		RP19		RP17		RP23		RP21		RP27		RP25	
1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16	RP17		RP19	RP20	RP21		RP23	RP24	RP25		RP27	RP28
4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18	RP19	RP20	RP21	RP22	RP23	RP24	RP25	RP26	RP27	RP28

ASUS	Title : CPTH (PCIE/DMI/USB/SATA)
ASUSTeK COMPUTER INC.	Engineer: IPC-EE3
Size: C	Project Name: ATX-Q670E
Rev: 1.00	
Date: Friday, May 20, 2022	Sheet 19 of 90


SU1E
PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109
CASEOPEN
+3V_BAT
SR160
1MOhm
S_INTRUDER#
GPD7
This strap should sample LOW.
Internal pull-down 20 kohm
+3VSB_ATX
SR1631
100KOhm
/X
1%
TP_GPD_7
SR183
20KOhm
1%
GND
SLP_A# :
When SLP_A# is asserted
(or it is de-asserted but Sx_Exit_Holdoff# is asserted),
the PCH will not access SPI Flash.
SR59
8.2KOhm
SR216
100KOhm
SR50/SR49 : need to check layout total length
7000 - 7500 = 24 ohm
5000 - 7000 = 27 ohm
0 - 5000 = 33 ohm
Place near PCH.
+3VSB_ADV
+3V
+1.8V_A
+1.05V_VCCPRIM
for SLPS3
Fan Out
SR136
8.2KOhm
SD4
BAT54AW
0Ohm
SR137
SR416
100KOhm
O_PWROK
SR93
0Ohm
PCH_SYSPWROK
SR177
SR176
SR306
10MOhm1
SX2
32.768Khz
XTAL 32.768KHZ 12.5PF/20PPM
[HE]SIWARD/XTL721-M99-113 3.2*1.5
07009-00111800
SC143
18PF/50V
SC144
18PF/50V
Trace < 1.5"
Routing on bottom side
RTC (10 MOHM RES): DO NOT CHANGE TO 0402 PACK_TYPE (intel CRB)
+VDDQ
SR43
470Ohm
SR56
0Ohm
S_D5_RESET#_R
SR58
10KOHM
/X
SC14
0.1UF/16V
SPI0_IO2 // SPI0_IO3
External pull-up is required.
Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V.
SR227
100KOhm
1%
SR171
20KOhm
SR403
SR173
SPI0_MOSI
External pull-up is required. Recommend 4.7 K pull up.
SR170
4.7KOHM
SR167
20KOhm
Boundry Scan (place near PCH)
ITP_PMODE ST6826
O_RSTCON# ST6827
S_RSMRST# ST6828
F_SPI0_IO2 ST6829
S_JTAG_TDI ST6830
S_JTAG_TCK ST6831
S_JTAG_TMS ST6832
S_JTAG_TDO ST6833
ASUS
ASUSTek COMPUTER INC.
Title : CPTH (SPI/MISC)
Engineer: IPC-EE3
Size Custom
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 20 of 90





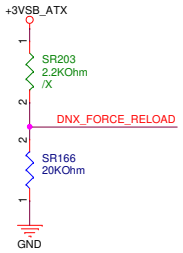


Serial ATA Port [3:7] General Purpose Inputs: When configured as SATAGP[3:7],
this is an input pin that is used as an interlock switch status indicator for SATA Port [3:7].
Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPP_F[0:4]. Pin defaults to Native mode as SATAXPCIE[3:7] depends on soft-strap.

GPP_G2 / DNX_FORCE_RELOAD

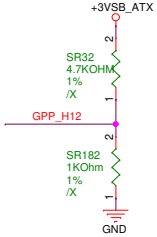
Download and Execute (DnX):IntelR CSME ROM samples this pin any time ROM begins execution.
This includes the following conditions:
- G3 Exit.
- Sx, Moff Exit.
- Cold Reset(Host Reset with Power Cycle) Exit.
- Warm Reset(Host Reset without Power Cycle) Exit if IntelR CSME was shutdown in Warm Reset.

L => No DnX
H => Enter DnX mode
Note : This pin must not be sampled high at the sampling time for normal operation .



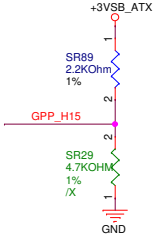
GPP_H12 / SML2ALERT# eSPI Flash Sharing Mode

0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Internal pull-down 20 kohm



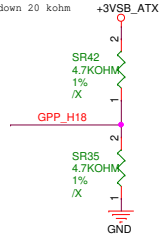
GPP_H15 / SML3ALERT# JTAG ODT Disable

0 = JTAG ODT is disabled (default)
1 = JTAG ODT is enabled
Internal pull-down 20 kohm



GPP_H18 / SML4ALERT# VCCSPI Voltage Configuration

0 = VCCSPI at 3.3 V (Default)
1 = VCCSPI at 1.8 V
Internal pull-down 20 kohm



ASUSTek COMPUTER INC.	Title : CPTH (GPIO_F/G/H)	
	Engineer: IPC-EE3	
Size: Custom	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 21 of 90	

GPP_R2 / HDA_SDO / HDACPU_SDO
Flash Descriptor Security Override

0: Enable security measures defined in the Flash Descriptor. (Default)
1: Disable Flash Descriptor Security (override).

This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
Internal pull-down 20 kohm

/X
DIS_ME(1-2)
MINI_JUMPER
+3VSB_ATX
ME_UNLOCK_R
HEADER_1X3P
DIS_ME
SR104 1KOhm 1%
O_ME_UNLOCK
SR98 0Ohm
A_Z_SDOUT_R
SR31 20KOhm 1% /X
ST6851
GND

SR240 2 /X 1 100KOhm GPP_S2
SR239 2 /X 1 100KOhm GPP_R7
SR237 2 /X 1 100KOhm GPP_R8
GND

+1.8V_A
SR88 1 /X 2 8.2KOhm
SR217 1 2 75KOhm CPU_C10_GATE_N_10
GND

+3VSB_ATX
SR2292 1% /X 1 100KOhm
SR2282 1% 1 100KOhm PCH_CORE_VID1
GND

+3VSB_ATX
SR1862 1% /X 1 100KOhm
SR1842 1% 1 100KOhm PCH_CORE_VID0
GND

SU1N

BF48	GPP_S7/SNDW4_DATA/DMIC_DATA0	BA9	DDPA_CTRLDATA
BF47	GPP_S6/SNDW4_CLK/DMIC_CLKA0	AY14	DDPA_CTRLCLK
BG47	GPP_S5/SNDW3_DATA/DMIC_DATA1	BD4	S_DP_C_CTRL_DATA
BE46	GPP_S4/SNDW3_CLK/DMIC_CLKA1	BE1	S_DP_C_CTRL_CLK
BF46	GPP_S3/SNDW2_DATA/DMIC_CLKB1	BE2	S_DP_B_CTRL_DATA
BG45	GPP_S2/SNDW2_CLK/DMIC_CLKB0	BB8	S_DP_B_CTRL_CLK
BH45	GPP_S1/SNDW1_DATA	AW8	S_HDMI_E_CTRL_DATA
BJ45	GPP_S0/SNDW1_CLK	AY6	S_HDMI_E_CTRL_CLK
		AW9	S_HDMI_D_CTRL_DATA
		AV11	S_HDMI_D_CTRL_CLK
		BC9	DDSP_HPDC
		BH7	DDSP_HPDB
		BD3	DDSP_HPDA
		BE6	GPP_R8
		AY11	GPP_R7
		BB6	GPP_R6
		BJ7	HDA_SDI1
		BE7	A_Z_RST#_R
		BF9	A_Z_SDIN0
		BF7	A_Z_SDOUT_R
		BF8	A_Z_SYNC_R
		BG8	A_Z_BITCLK_R

GPP_S2
GPP_R21/DDPA_CTRLDATA
GPP_R20/DDPA_CTRLCLK
GPP_R19/DDP2_CTRLDATA
GPP_R18/DDP2_CTRLCLK
GPP_R17/DDP1_CTRLDATA
GPP_R16/DDP1_CTRLCLK
GPP_R15/ISH_SPI_MOSI /DDP4_CTRLDATA/GSPI2_MOSI
GPP_R14/ISH_SPI_MISO /DDP4_CTRLCLK/GSPI2_MISO
GPP_R13/ISH_SPI_CLK /DDP3_CTRLDATA/GSPI2_CLK
GPP_R12/ISH_SPI_CS# /DDP3_CTRLCLK/GSPI2_CS0#
GPP_R11/DDSP_HPDC/DISP_MISCC
GPP_R10/DDSP_HPDB/DISP_MISCB
GPP_R9/DDSP_HPDA/DISP_MISCA
GPP_R8
GPP_R7
GPP_R6
GPP_R5/HDA_SDI1
GPP_R4/HDA_RST#
GPP_R3/HDA_SDI0/HDACPU_SDI
GPP_R2/HDA_SDO/HDACPU_SDO
GPP_R1/HDA_SYNC
GPP_R0/HDA_BCLK/HDACPU_BCLK

S_DP_C_CTRL_DATA 40
S_DP_C_CTRL_CLK 40
S_DP_B_CTRL_DATA 39
S_DP_B_CTRL_CLK 39
S_HDMI_E_CTRL_DATA 42
S_HDMI_E_CTRL_CLK 42
S_HDMI_D_CTRL_DATA 41
S_HDMI_D_CTRL_CLK 41
SR16 2 1 100KOhm
SR78 2 1 100KOhm
S_DP2VGA_HPD 32
GND
ST28
ST22
SR172 2 1 33Ohm A_Z_RST# 43
A_Z_SDIN0 43
SR168 2 1 33Ohm A_Z_SDOUT 43
SR169 2 1 33Ohm A_Z_SYNC 43
SR165 2 1 33Ohm A_Z_BITCLK 43

PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109

SU1M

AY4	GPP_J11/BSSB_LS_TX	BE15	GPP_I20/GSPI1_CLK
AT8	GPP_J10/BSSB_LS_RX	BF13	GPP_I21/GSPI1_MISO
BB4	GPP_J7/CNV_MFUART2_TXD	BF14	GPP_I10/GSPI1_CS1#/TIME_SYNC1
AV12	GPP_J6/CNV_MFUART2_RXD	BG14	GPP_I19/GSPI1_CS0#
BC4	GPP_J5/CNV_RGI_RSP/UART0_CTS#	BG15	GPP_I22/GSPI1_MOSI
BC5	GPP_J4/CNV_RGI_DT/UART0_TXD	BG11	GPP_I9/GSPI0_CS1#
BA5	GPP_J3/CNV_BRI_RSP/UART0_RXD	BH11	GPP_I16/GSPI0_CLK
AU6	GPP_J2/CNV_BRI_DT/UART0_RTS#	BF10	GPP_I17/GSPI0_MISO
BA3	GPP_J1/CPU_C10_GATE#	BE12	GPP_I18/GSPI0_MOSI
BB2	GPP_J0/CNV_PA_BLANKING	BF11	GPP_I15/GSPI0_CS0#
BB54	GPP_K11	BB13	GPP_I13/USB_OC6#/I2C5_SDA
AW53	GPP_K9/CORE_VID1	BD12	GPP_I14/USB_OC7#/I2C5_SCL
BA51	GPP_K3/GSXSRESET#	BA16	GPP_I11/USB_OC4#/I2C4_SDA
AY52	GPP_K2/GSXDIN	AY16	GPP_I12/USB_OC5#/I2C4_SCL
BA53	GPP_K1/GSXSLOAD	BE10	GPP_I8/DDPC_CTRLDATA
BA52	GPP_K0/GSXDOUT	BG9	GPP_I7/DDPC_CTRLCLK
AW52	GPP_K8/CORE_VID0	BG12	GPP_I6/DDPB_CTRLDATA
BB52	GPP_K4/GSXCLK	BF12	GPP_I5/DDPB_CTRLCLK
AV51	GPP_K5/ADR_COMPLETE	BA13	GPP_I4/DDSP_HPD4/DISP_MISC4
		BB15	GPP_I3/DDSP_HPD3/DISP_MISC3
		BD14	GPP_I2/DDSP_HPD2/DISP_MISC2
		BH15	GPP_I1/DDSP_HPD1/DISP_MISC1
		BJ16	GPP_I0/EXT_PWR_GATE#

GPP_J4
GPP_J2
CPU_C10_GATE_N_10
PCH_CORE_VID1
PCH_CORE_VID0
ST23 1 ADR_COMPLETE
For Intel DnX LED at CRB.

82 PCH_CORE_VID1
80,82 PCH_CORE_VID0

GPP_I22
GPP_I18
U_USBOC#7 59
U_USBOC#910 60
U_USBOC#5 62
DDPC_CTRLDATA
DDPC_CTRLCLK
DDPB_CTRLDATA
DDPB_CTRLCLK
S_HDMI_E_HPD 42
S_HDMI_D_HPD 41
S_DP_C_HPD 40
S_DP_B_HPD 39
EXT_PWR_GATE# 1 ST39
CRB use for PCIe slot PWR Gate.

0: Integrated CNVi enable
1: Integrated CNVi disable

PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109

GPP_R[12:21]_I[5:8] / DDP[1:4,A:C] _CTRLDATA

0: Port [A:E] is not detected. (default)
1: Port [A:E] is detected.

Internal pull-down 15-40 kohm

+3V

S_HDMI_D_CTRL_CLK	SR84	2	2.2KOhm1
S_HDMI_D_CTRL_DATA	SR85	2	2.2KOhm1
S_DP_C_CTRL_CLK	SR80	2	2.2KOhm1
S_DP_C_CTRL_DATA	SR81	2	2.2KOhm1
S_DP_B_CTRL_CLK	SR82	2	2.2KOhm1
S_DP_B_CTRL_DATA	SR83	2	2.2KOhm1
S_HDMI_E_CTRL_CLK	SR87	2	2.2KOhm1
S_HDMI_E_CTRL_DATA	SR199	2	2.2KOhm1
DDPA_CTRLCLK	SR92	2	2.2KOhm1
DDPA_CTRLDATA	SR97	2	2.2KOhm1
DDPB_CTRLCLK	SR100	2	2.2KOhm1
DDPB_CTRLDATA	SR101	2	2.2KOhm1
DDPC_CTRLCLK	SR202	2	2.2KOhm1
DDPC_CTRLDATA	SR86	2	2.2KOhm1

+3VSB_ATX

U_USBOC#910	SR117	1	8.2KOhm2
U_USBOC#5	SR124	1	8.2KOhm2
U_USBOC#7	SR121	1	8.2KOhm2
USB2_OCB_7	SR122	1	8.2KOhm2

GPP_J2 / CNV_BRI_DT / UART0_RTS#
XTAL Frequency Selection Bit 0

+1.8V_A
00 = 24 MHz MHz (default)
01 = Reserved
10 = 38.4 MHz
11 = 25 MHz
Internal pull-down 20 kohm
SR181 4.7KOHM 1% /X
GPP_J2
SR174 20KOhm 1% /X
GND

GPP_J4 / CNV_RGI_DT / UART0_TXD
M.2 CNVi Mode Select

+1.8V_A
0: Integrated CNVi enable
1: Integrated CNVi disable
SR180 4.7KOHM 1%
GPP_J4
SR105 20KOhm 1% /X
GND

GPP_I18 / GSPI0_MOSI
No Reboot

+3VSB_ATX
0: Disable "No Reboot" mode. (Default)
1: Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).
Internal pull-down 20 kohm
This function is useful when running ITP/ XDP.
SR213 4.7KOHM 1% /X
GPP_I18
SR30 1KOhm 1% /X
GND

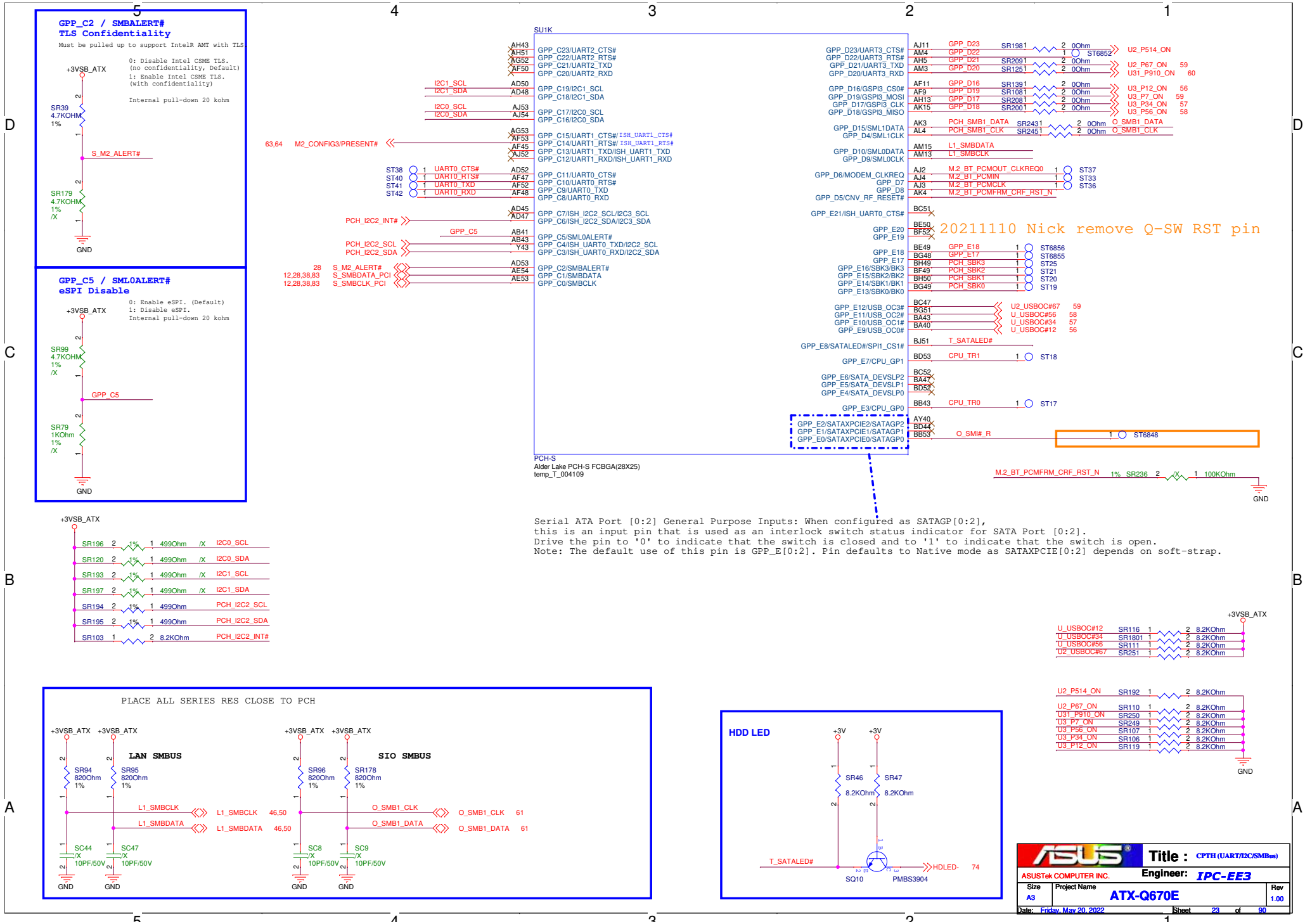
GPP_I22 / GSPI1_MOSI
Boot BIOS Strap (BBS)

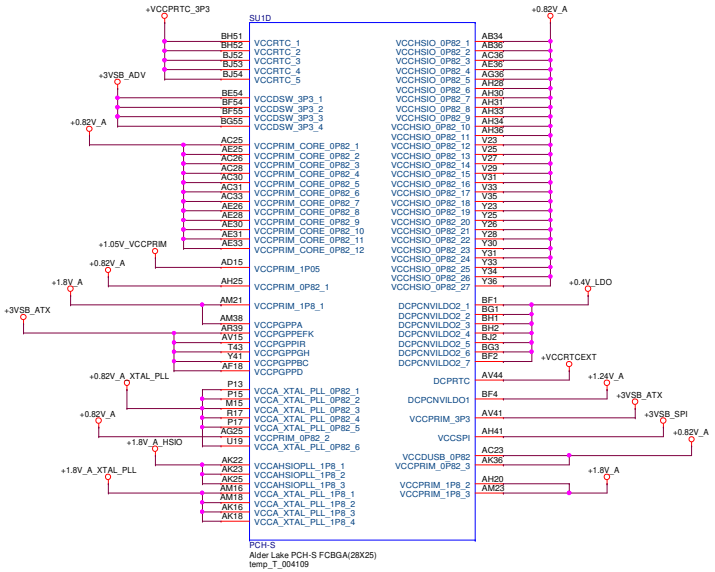
+3VSB_ATX
0: BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF)
1: BIOS fetches are routed to the eSPI Peripheral Channel
Internal pull-down 20 kohm
SR185 4.7KOHM 1% /X
GPP_I22
SR201 20KOhm 1% /X
GND

ASUS
ASUSTek COMPUTER INC.
Title : CPTH (AUDIO/DISPLAY/CNVi)
Engineer: IPC-EE3

Size	Project Name	Rev
A3	ATX-Q670E	1.00

Date: Friday, May 20, 2022 Sheet 22 of 90


GPP_C2 / SMBALERT#
TLS Confidentiality
Must be pulled up to support IntelR AMT with TLS
0: Disable Intel CSME TLS. (no confidentiality, Default)
1: Enable Intel CSME TLS. (with confidentiality)
Internal pull-down 20 kohm
+3VSB_ATX
SR39 4.7KOHM 1%
S_M2_ALERT#
SR179 4.7KOHM 1% /X
GND
GPP_C5 / SML0ALERT#
eSPI Disable
0: Enable eSPI. (Default)
1: Disable eSPI.
Internal pull-down 20 kohm
SR99 4.7KOHM 1% /X
GPP_C5
SR79 1KOhm 1% /X
SU1K
PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109
20211110 Nick remove Q-SW RST pin
Serial ATA Port [0:2] General Purpose Inputs: When configured as SATAGP[0:2],
this is an input pin that is used as an interlock switch status indicator for SATA Port [0:2].
Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPP_E[0:2]. Pin defaults to Native mode as SATAXPCIE[0:2] depends on soft-strap.
PLACE ALL SERIES RES CLOSE TO PCH
LAN SMBUS
SIO SMBUS
HDD LED
ASUSTek COMPUTER INC.
Title : CPTH (UART/I2C/SMBus)
Engineer: IPC-EE3
Size A3
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 23 of 90

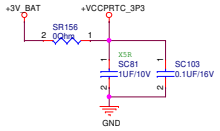


GPIO Voltage Level

Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+1.8V_A
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSB_ATX
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSB_ATX
GPP_D	VCCPGPPD	1.8V or 3.3V	+3VSB_ATX
GPP_E	VCCPGPPEFK	1.8V or 3.3V	+3VSB_ATX
GPP_F	VCCPGPPEFK	1.8V or 3.3V	+3VSB_ATX
GPP_G	VCCPGPPGH	1.8V or 3.3V	+3VSB_ATX
GPP_H	VCCPGPPGH	1.8V or 3.3V	+3VSB_ATX
GPP_I	VCCPGPPIR	1.8V or 3.3V	+3VSB_ATX
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPP_K	VCCPGPPEFK	1.8V or 3.3V	+3VSB_ATX
GPP_R	VCCPGPPIR	1.8V or 3.3V	+3VSB_ATX
GPP_S	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPD	VCCDSW_3P3	3.3V Only	+3VSB_ATX

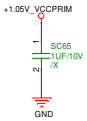
Other Power

SC81, SC103 Place close to the PCH package edge, <10mm



SC31 Place close to the PCH package edge, <5mm
Plan width need >3mm

SC65 Place close to the PCH package edge, <5mm

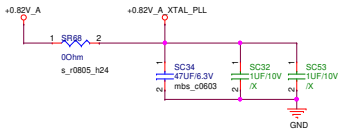


SC27 Place close to the PCH package edge, <5mm
Plan width need >2mm

SC28 Place close to the PCH package edge, <5mm
Plan width need >2mm

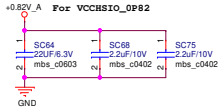
+0.82A

SC34 Place close to the PCH package edge, <10mm
Plan width need >4mm
Need GND shielding.



SC32, SC53 Place close to the PCH package edge, <5mm

SC64 Place close to the PCH package edge, <10mm

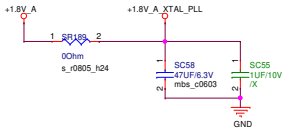


SC68, SC75 Place close to the PCH package edge, <5mm

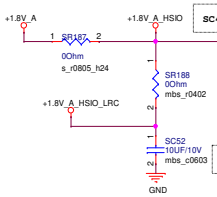
SC35 Place close to the PCH package edge, <10mm
Plan width need >8mm

+1.8V_A

SC58 Place close to the PCH package edge, <10mm
Plan width need >3mm
Need GND shielding.



SC55 Place close to the PCH package edge, <5mm



SC48 Place close to the PCH package edge, <5mm

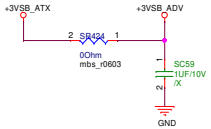
SC52 Place close to the PCH package edge, <10mm

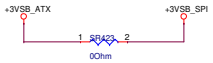
SC66 Place close to the PCH package edge, <5mm
Plan width in package need >3mm, outside need >8mm

+3VSB_ATX

SC67 Place close to the PCH package edge, <5mm
Plan width need >5mm

SC59 Place close to the PCH package edge, <10mm





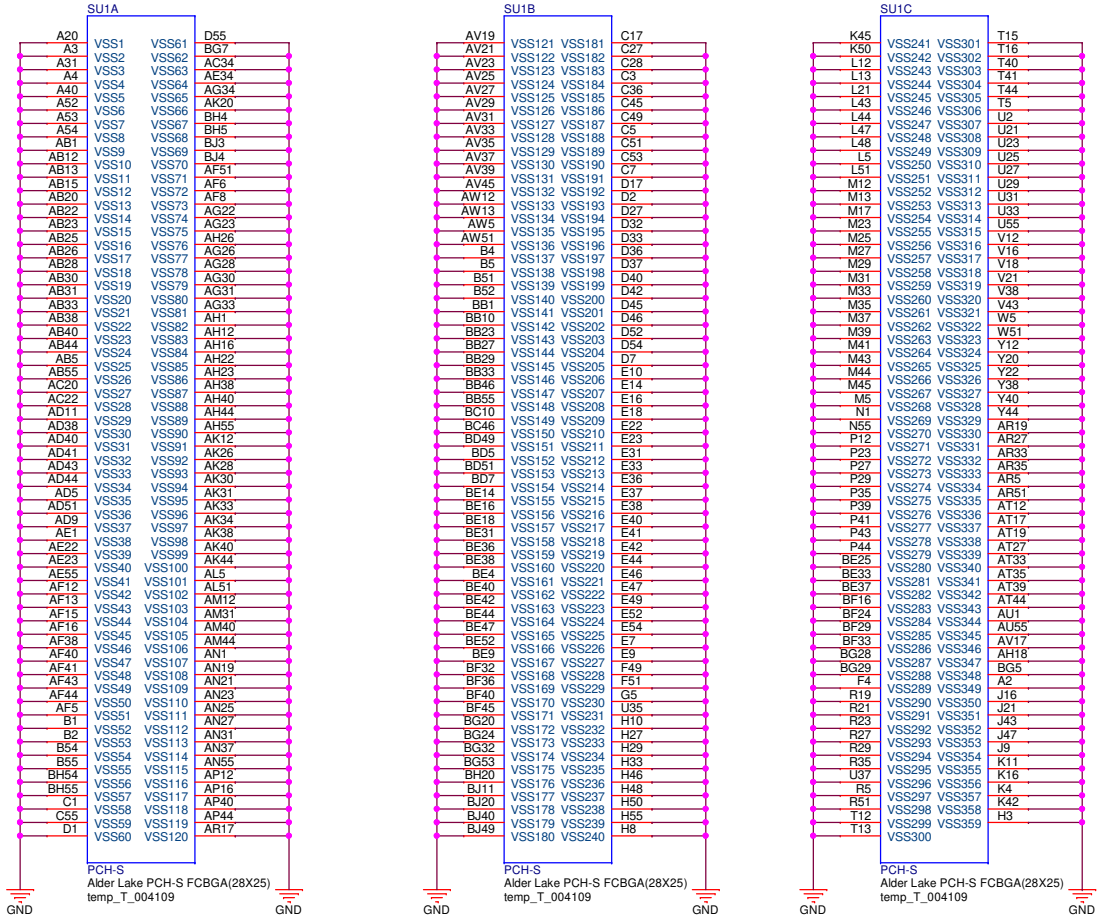
ASUSTek COMPUTER INC.

Title : KPTH (POWER)

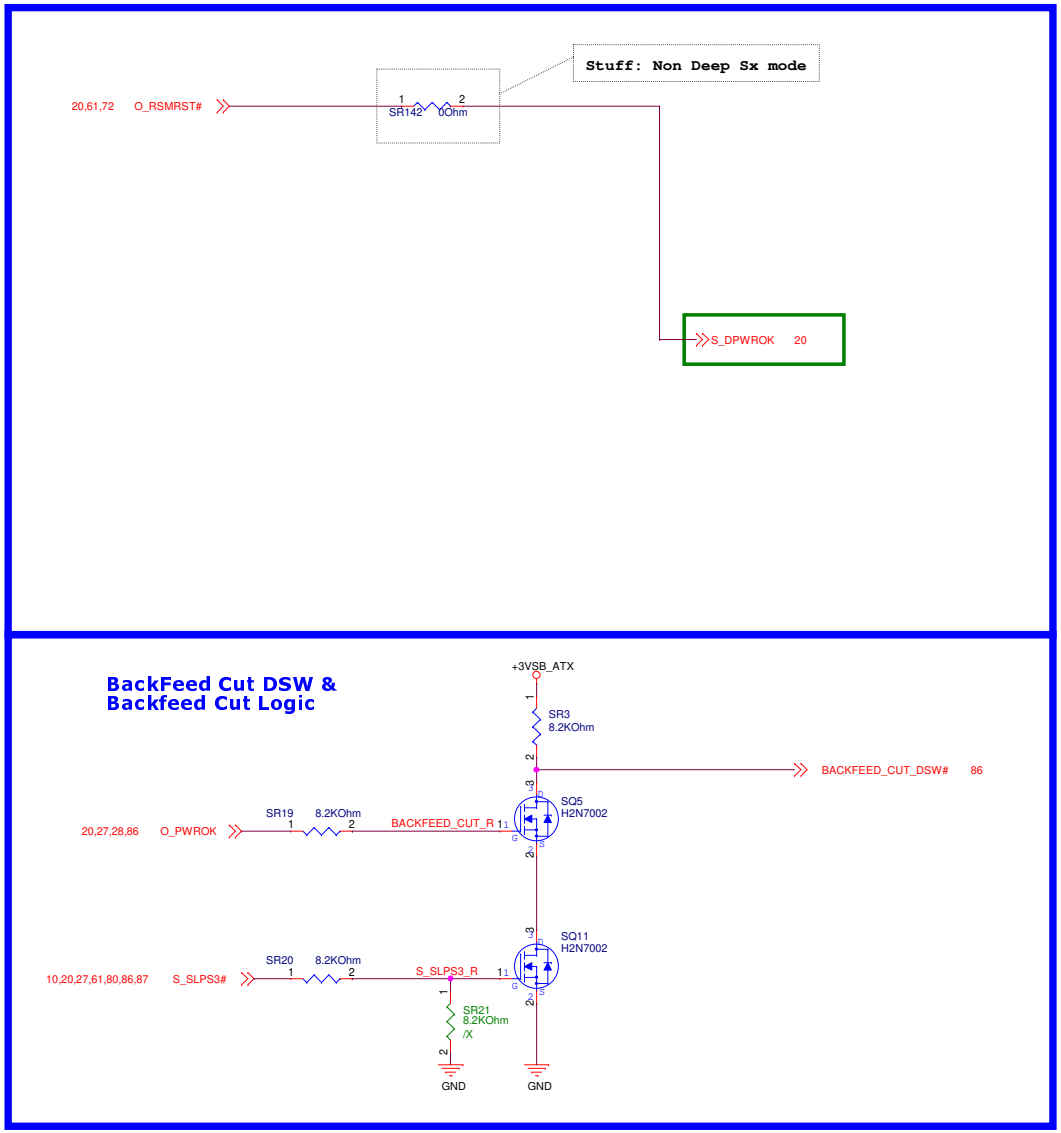
Engineer: IPC-EE3

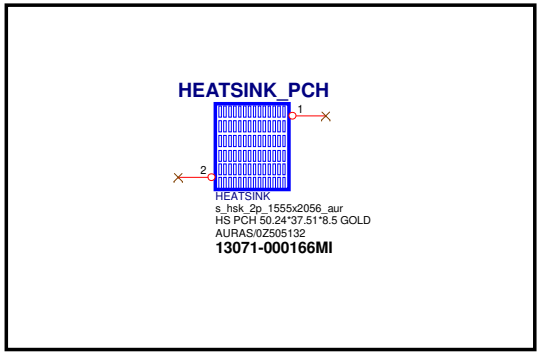
Size	Project Name	Rev
C	ATX-Q670E	1.00

Date: Friday, May 20, 2022 Sheet 24 of 90



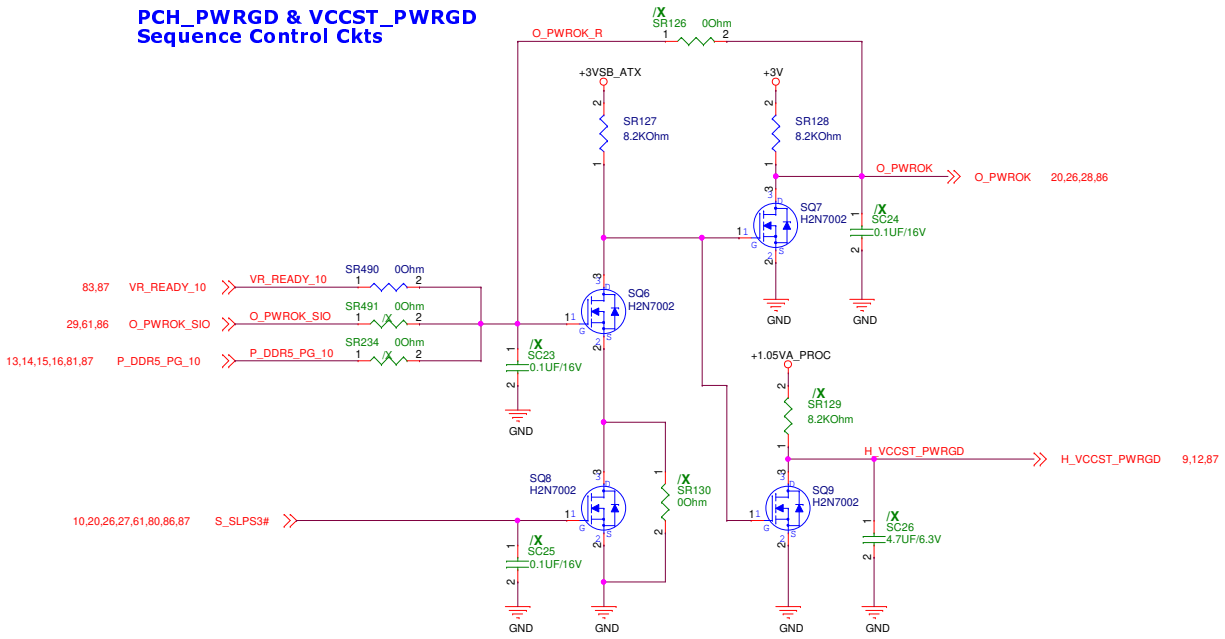
ASUSTek COMPUTER INC.	Title : CPTH (GND)		
	Engineer: IPC-EE3		
Size B	Project Name ATX-Q670E		Rev 1.00
Date: Friday, May 20, 2022	Sheet 25 of 90		



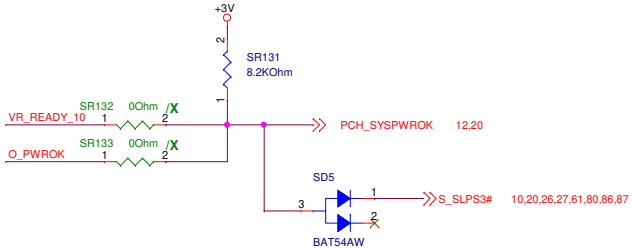


ASUS	Title : CPTH (DSW SEQUENCE)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 26 of 90	

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



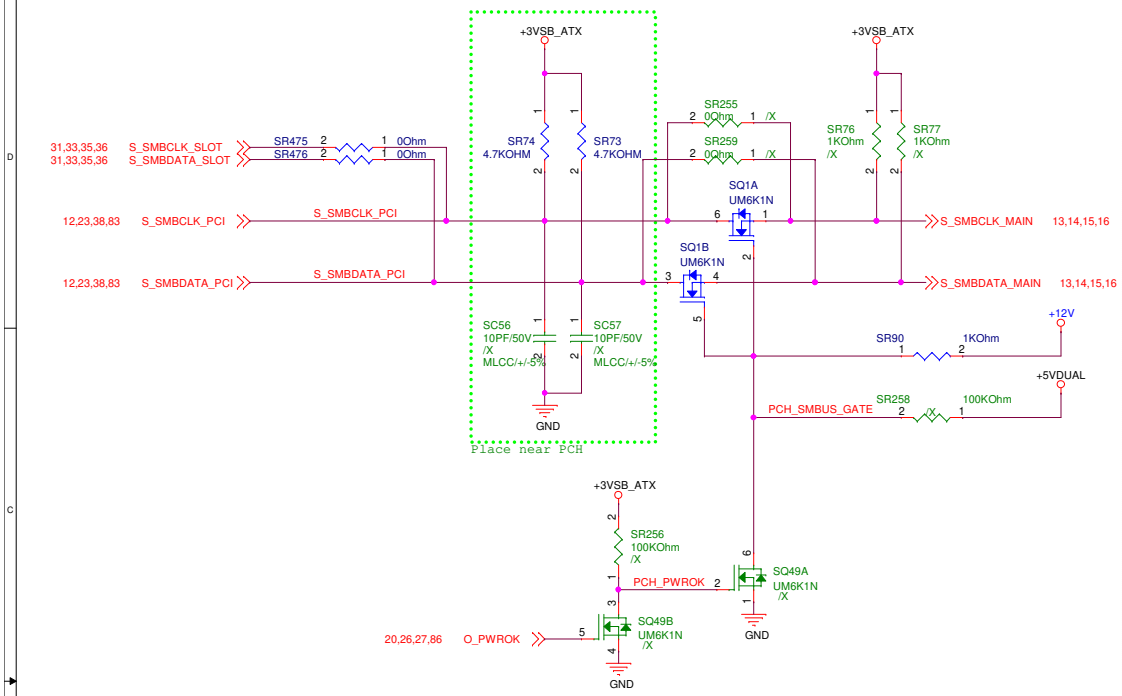
1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

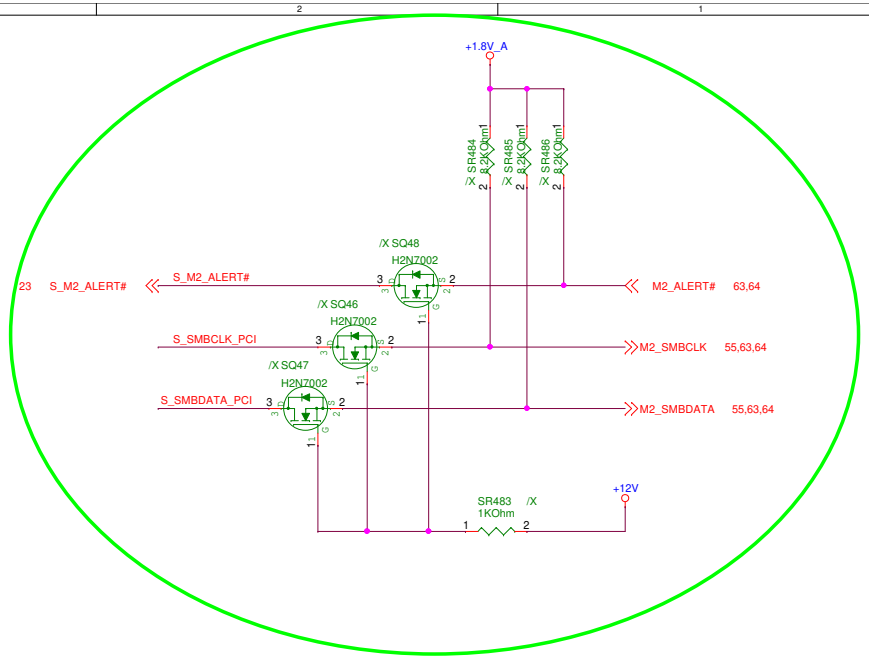
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

ASUSTek COMPUTER INC.	Title : CETH (PCH/SYS/PROC_PWROK)	
	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 27 of 90	



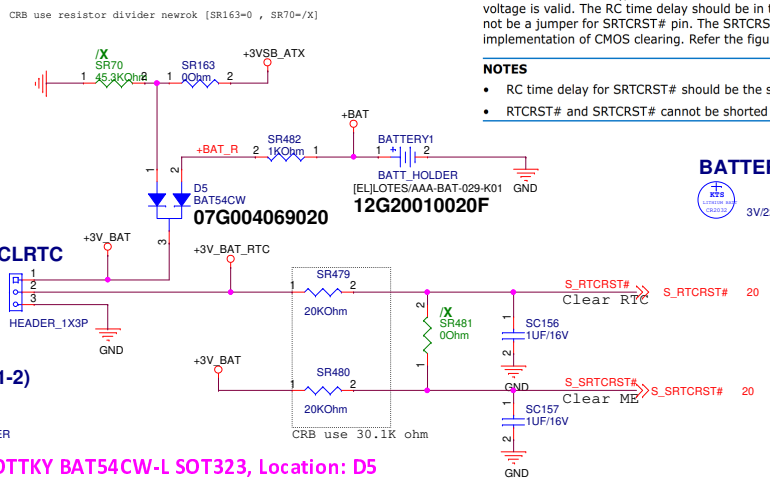


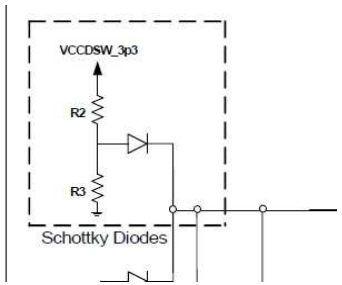
RTC External SRTCRST# Circuit

The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18~25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer the figure above external circuit for PCH RTC.

NOTES

- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.

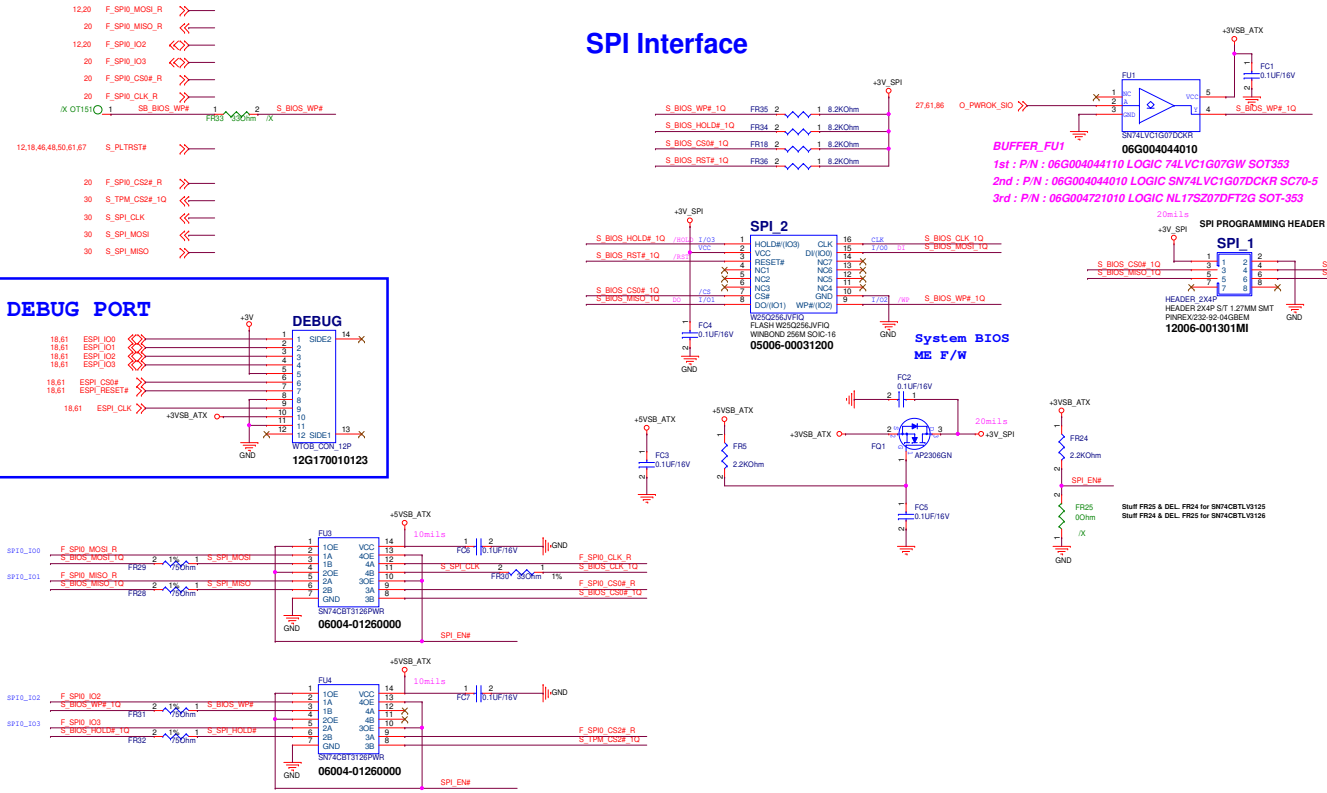




SCHOTTKY BAT54CW-L SOT323, Location: D5
1st : 07G004203013 PANJIT
2nd : 07G004069020 PANJIT
3rd : 07G004145011 PHILIPS

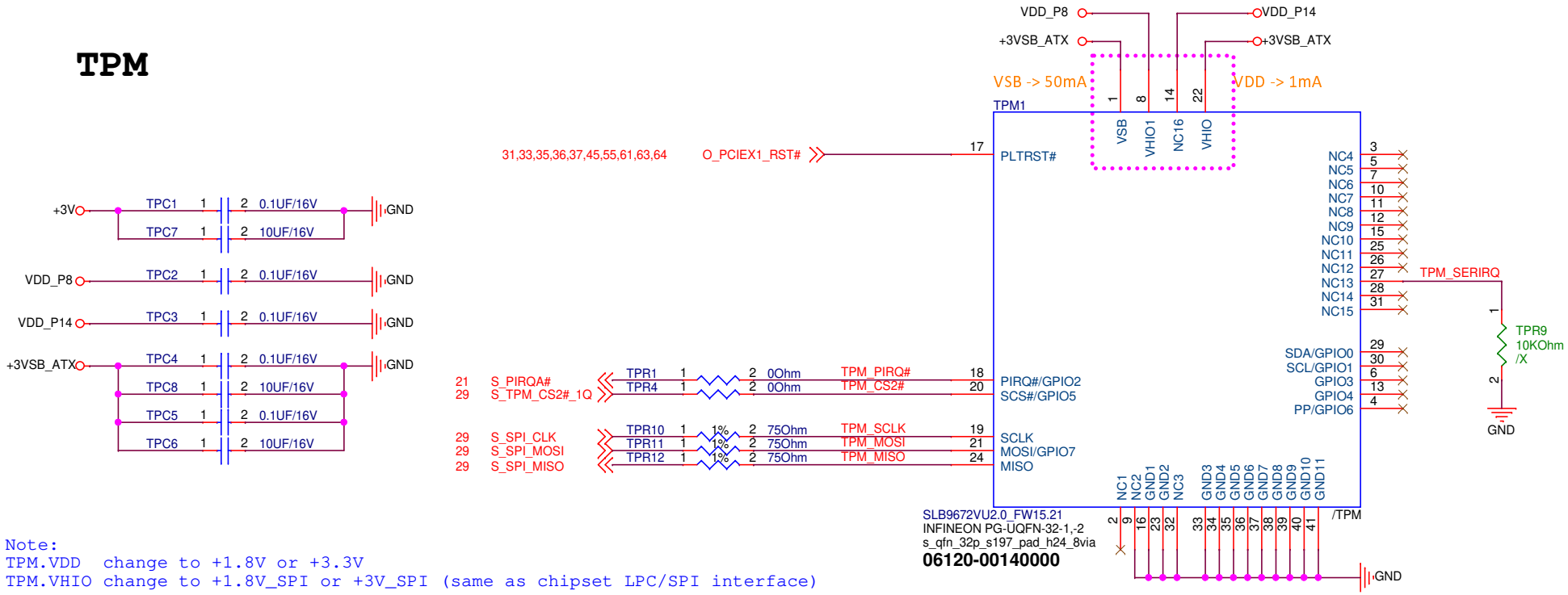
ASUS	Title : CPTH (SMBUS/CLRTC)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 28 of 90	

SPI Interface



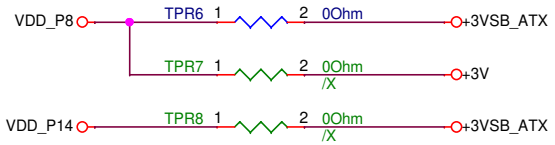
Note: Continuous channel current is 128mA(max.)

TPM



Note:
TPM.VDD change to +1.8V or +3.3V
TPM.VHIO change to +1.8V_SPI or +3V_SPI (same as chipset LPC/SPI interface)

TPM need to change the component(INFINEON FW7.85)
P/N: 06120-00140000



	NPCT650	NPCT750
TPR6	x	v
TPR7	v	x
TPR8	v	x
TPR9	v	x

(Pin.18) PIRQ#
It should be connected to one of PIRQ[A:D]# of Chipset inputs

(Pin.27) SERIRQ
for LPC interface use only

(Pin.17) SPI_RST#
PCI system reset used for LPC/SPI bus (Hardware reset)

(Pin.4) PP (Physical Presense Input)
By default the PP functionality is disabled.

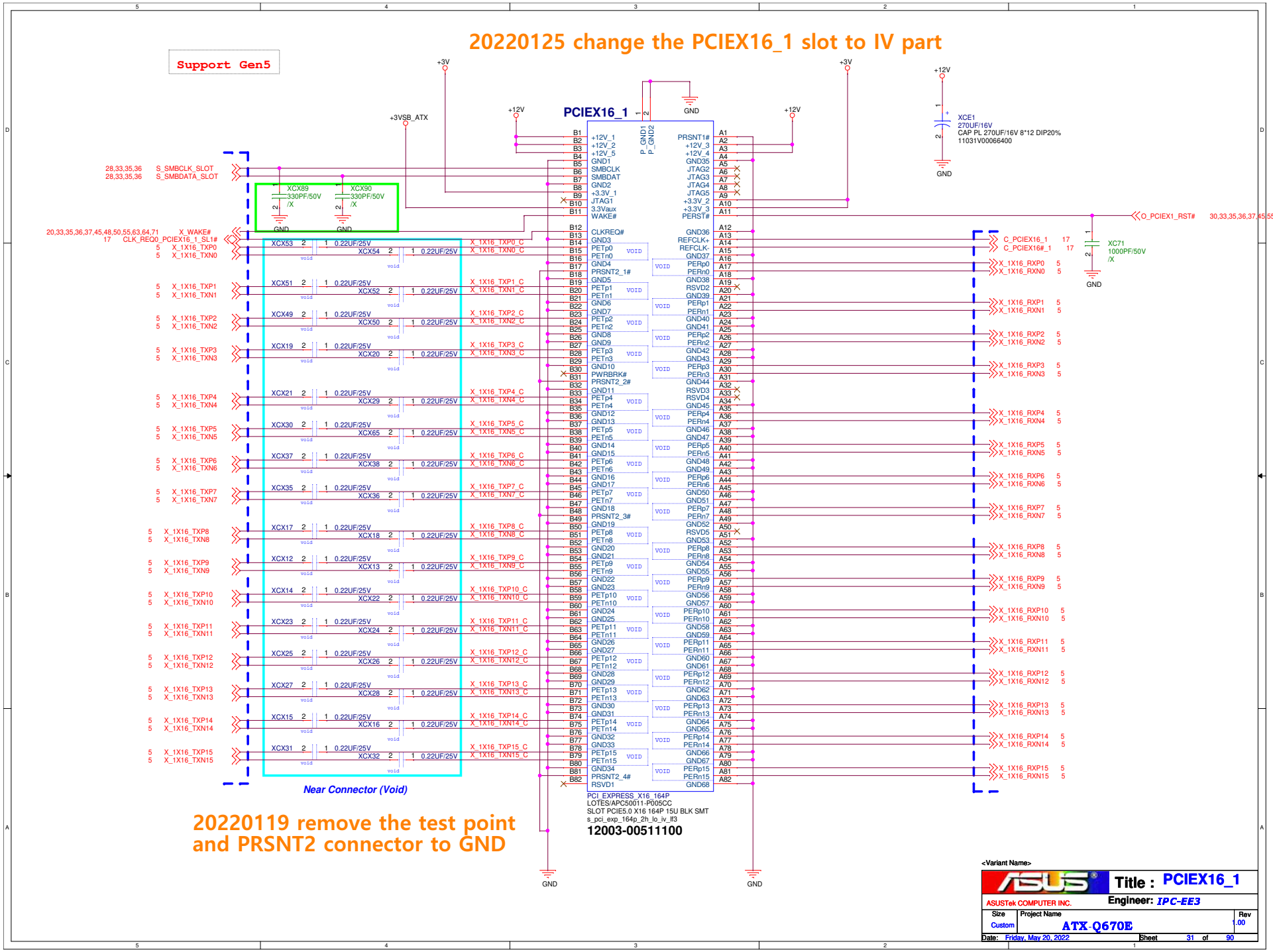
GPIO[0:6] and PP are optional.
Leave them open if not used.

GPIO[0] contact to SLP_S0# for Connected Standby, if supported.

Windows10 Hardware Compatibility Specifications for RS3
Mandatory: The TPM must support driven communication.
Mandatory: The TPM interrupt pin must be connected to an interrupt controller.

<Variant Name>

ASUS	Title : TPM_NPCT750AADYX	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A4	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 30 of 90	


20220125 change the PCIEX16_1 slot to IV part
Support Gen5
PCIEX16_1
PCI_EXPRESS_X16_164P
LOTES/APC50011-P005CC
SLOT PCIE5.0 X16 164P 15U BLK SMT
s_pci_exp_164p_2h_lo_iv_lf3
12003-00511100
Near Connector (Void)
20220119 remove the test point and PRSNT2 connector to GND
XCE1
270UF/16V
CAP PL 270UF/16V 8*12 DIP20%
11031V00066400
XC71
1000PF/50V
/X
XCX89
330PF/50V
/X
XCX90
330PF/50V
/X
+3V
+3VSB_ATX
+12V
GND
S_SMBCLK_SLOT
S_SMBDATA_SLOT
X_WAKE#
CLK_REQ0_PCIEX16_1_SL1#
O_PCIEX1_RST#
C_PCIEX16_1
C_PCIEX16#_1
Title : PCIEX16_1
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size
Custom
Project Name
ATX-Q670E
Rev
1.00
Date: Friday, May 20, 2022
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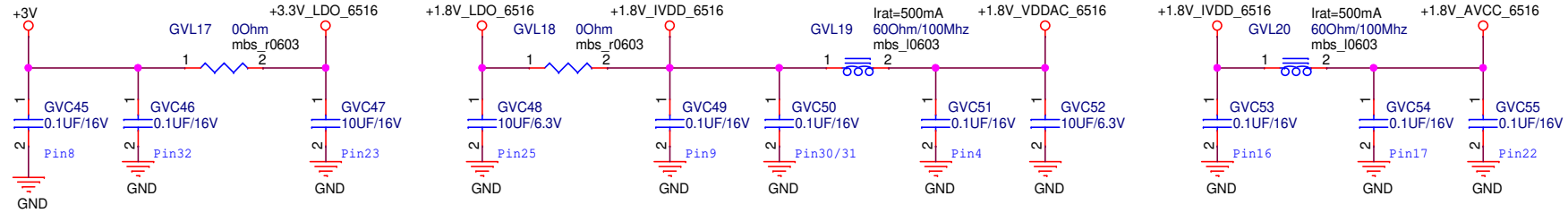
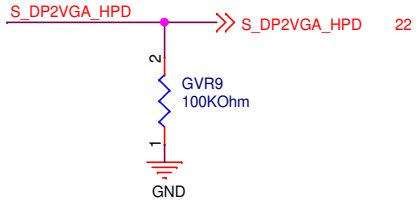
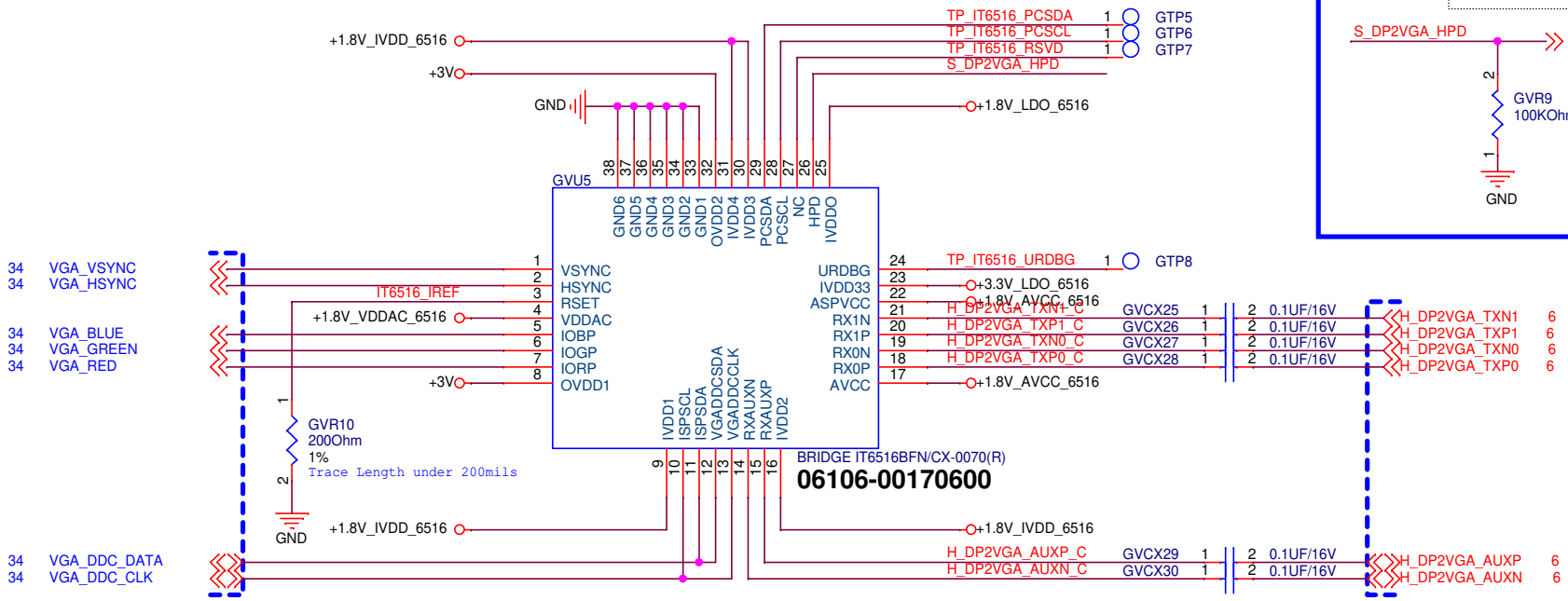
IT6516B Power Caps and Beads



Hot-Plug Detect

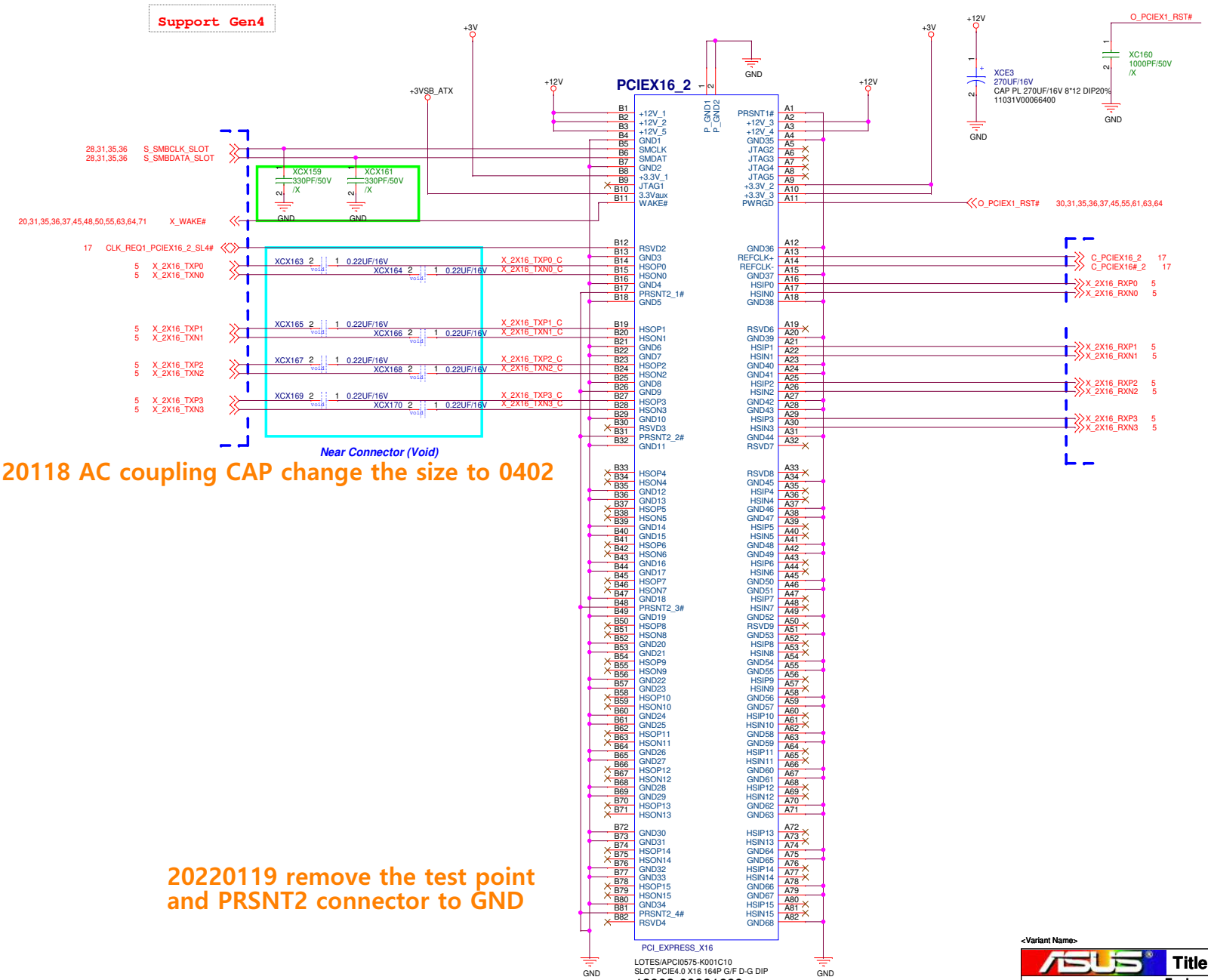
Voltage Level +3.3V





<Variant Name>

ASUSTek COMPUTER INC.	Title : VGA_IT6516B (Port A)	
	Engineer: IPC-EE3	
Size A4	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 32 of 86	



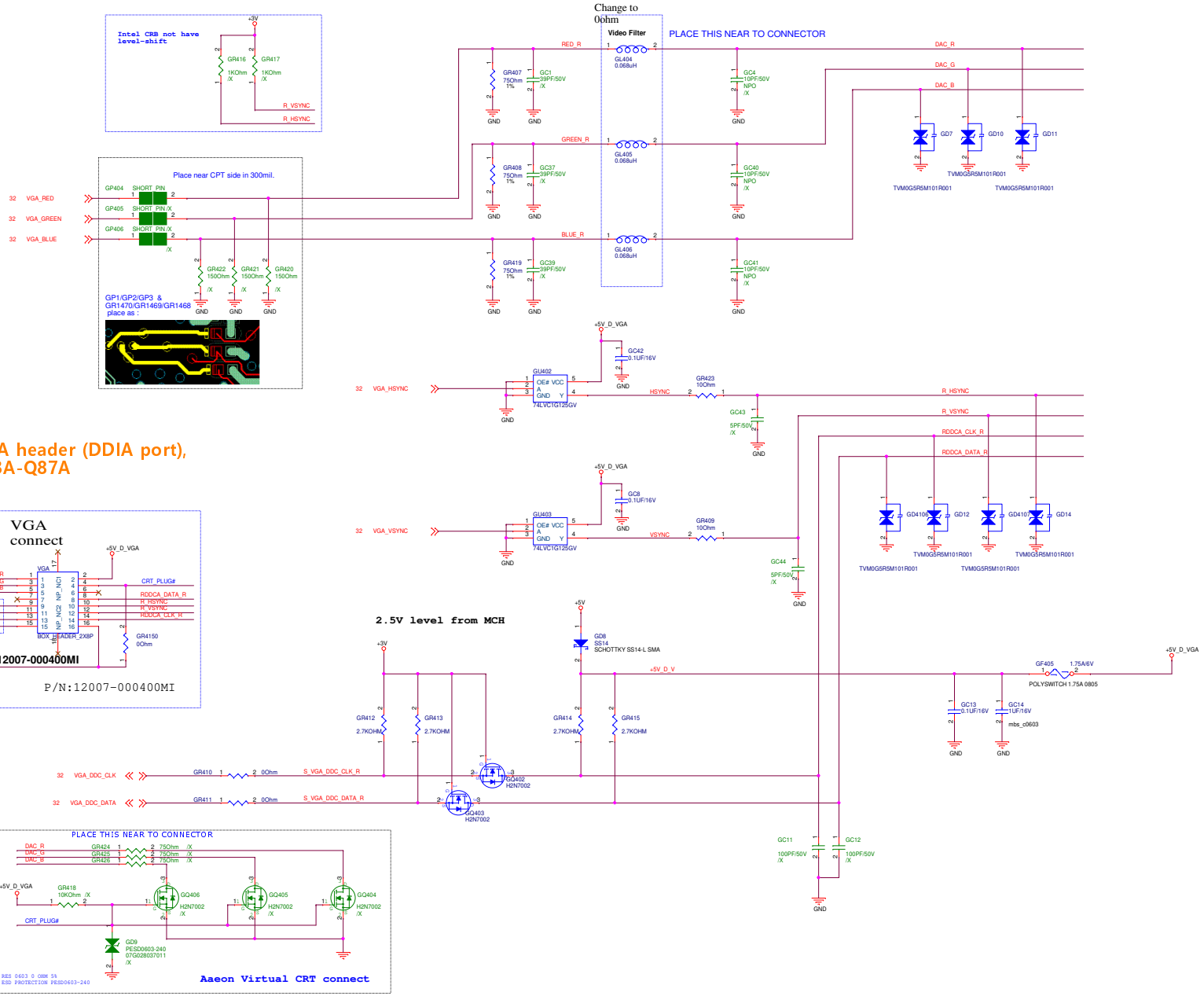
20220118 AC coupling CAP change the size to 0402

20220119 remove the test point and PRSNT2 connector to GND

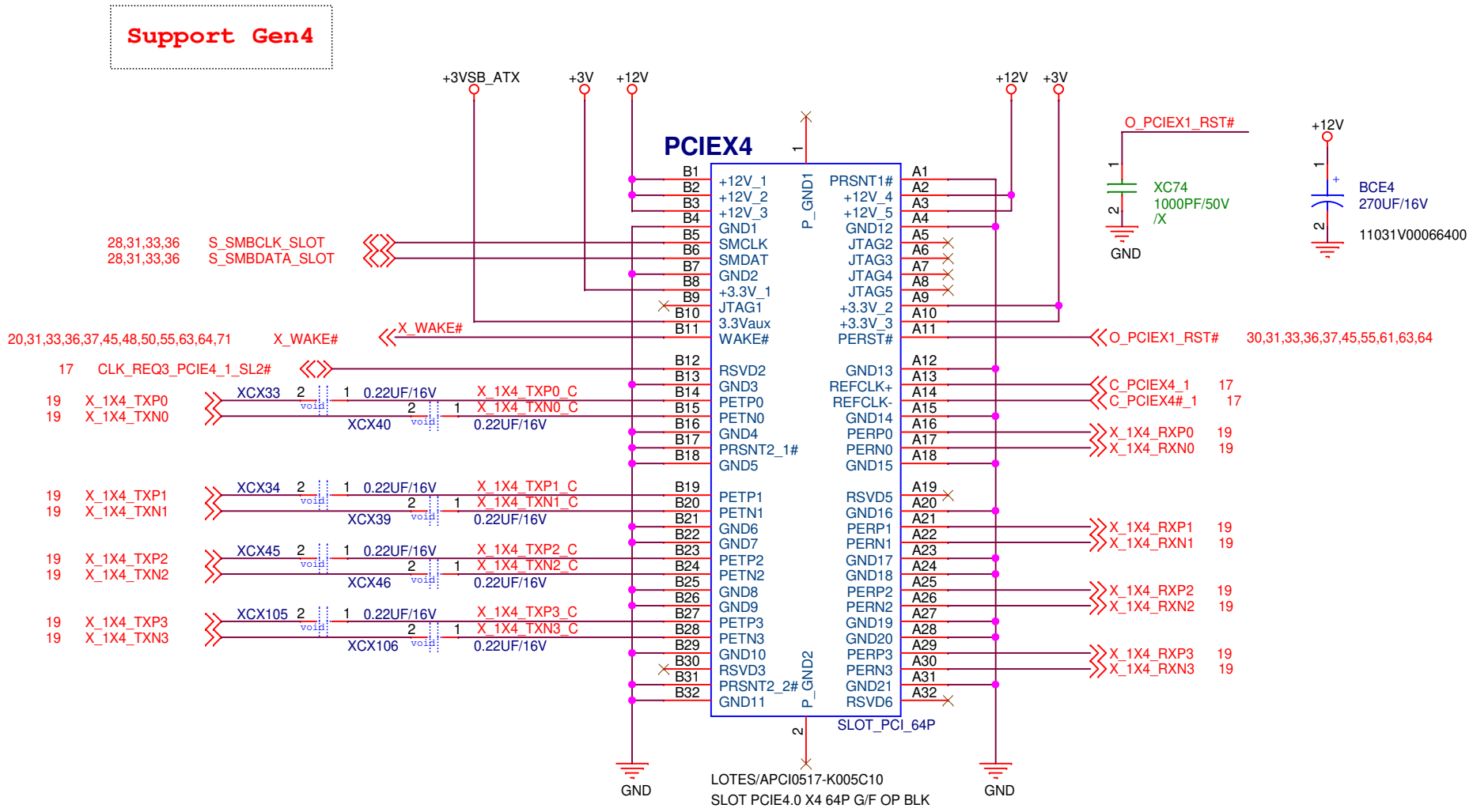
<Variant Name>

ASUS	Title : PCIEX16_2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 33 of 90	

20211118 VGA (DDIA port), reference MAX-Q470A



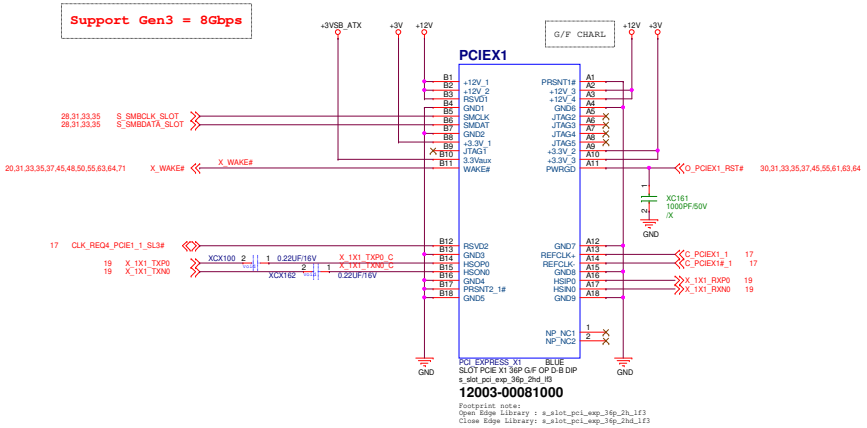
20211118 VGA header (DDIA port), reference IMBA-Q87A



<Variant Name>

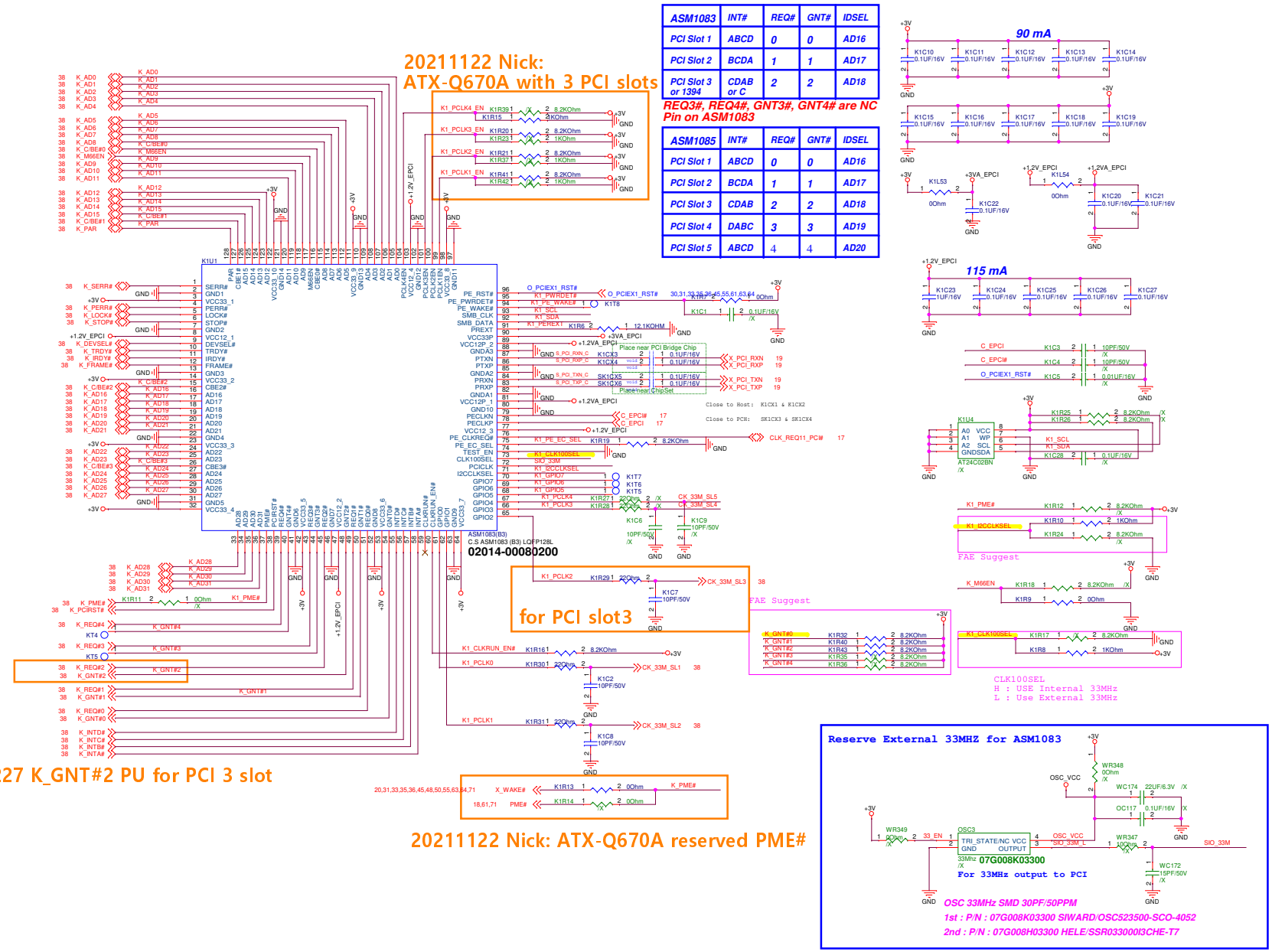
ASUSTek COMPUTER INC.	Title : PCIEX4_1	Engineer: IPC-EE3
Size: A	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 35 of 90	

20211110 Nick modify, reference ATX-C246A, PCIex1_1



20211227 remove PCIEX1_2

Support Gen3 = 8Gbps



ASM1083	INT#	REQ#	GNT#	IDSEL
PCI Slot 1	ABCD	0	0	AD16
PCI Slot 2	BCDA	1	1	AD17
PCI Slot 3 or 1394	CDAB or C	2	2	AD18

REQ3#, REQ4#, GNT3#, GNT4# are NC Pin on ASM1083

ASM1085	INT#	REQ#	GNT#	IDSEL
PCI Slot 1	ABCD	0	0	AD16
PCI Slot 2	BCDA	1	1	AD17
PCI Slot 3	CDAB	2	2	AD18
PCI Slot 4	DABC	3	3	AD19
PCI Slot 5	ABCD	4	4	AD20

<Variant Name>

ASUSTek COMPUTER INC.

Title : PCI_ASM1083

Engineer: IPC-EE3

Size	Project Name	Rev
C	ATX-Q670E	1.00

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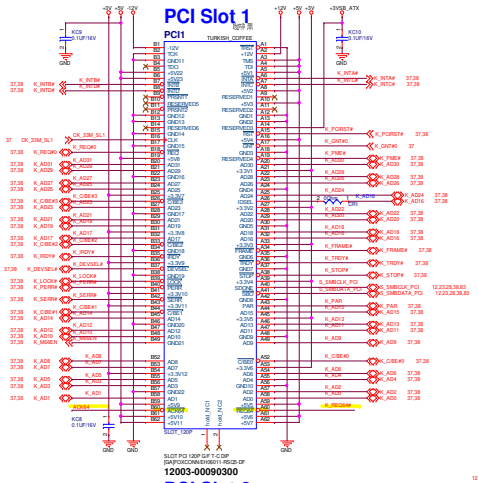
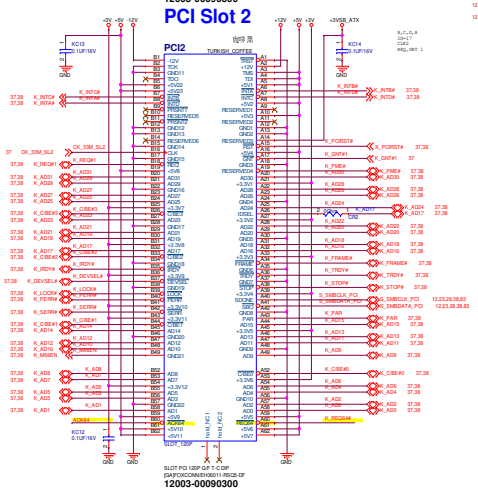
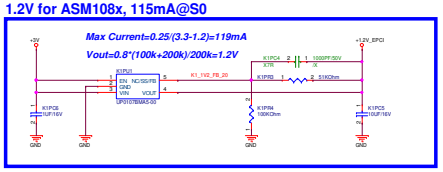
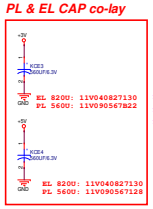


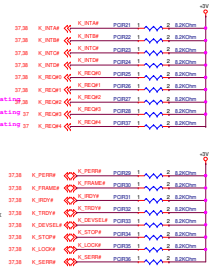


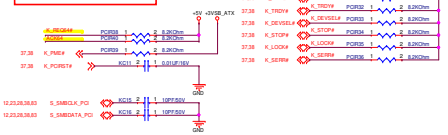
1.2V for ASM108x, 115mA@S0



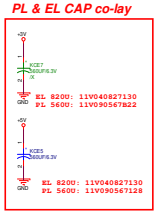
PL & EL CAP co-lay



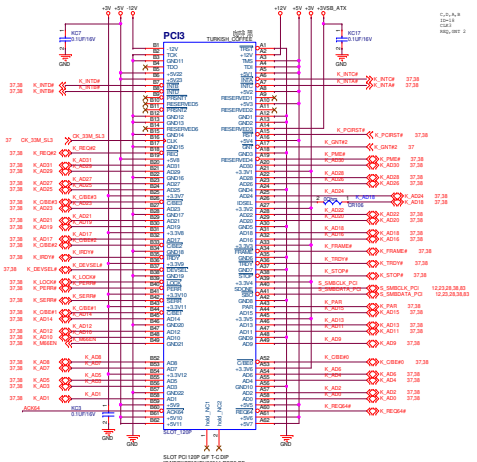




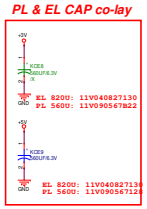
PL & EL CAP co-lay



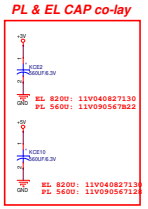
PCI Slot 3



PL & EL CAP co-lay

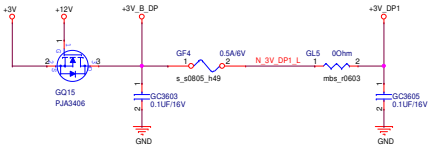


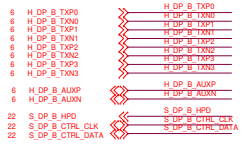
PL & EL CAP co-lay

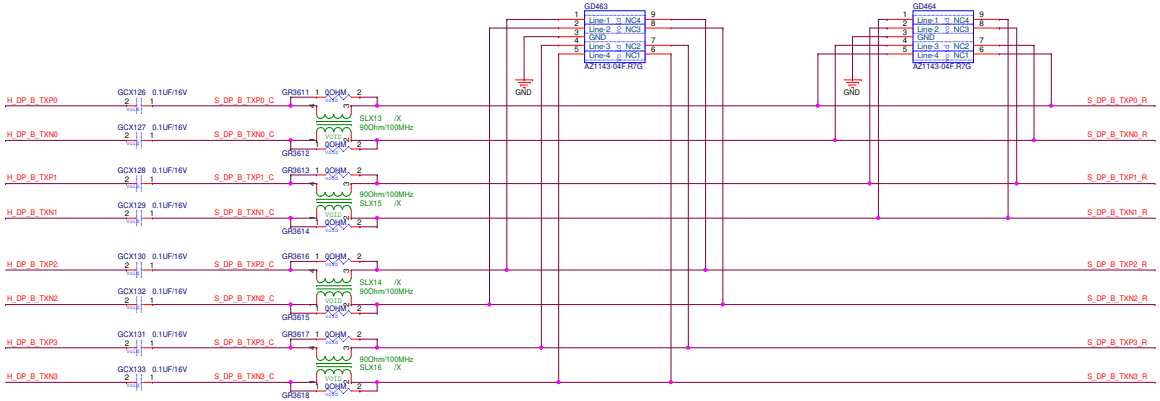


-Variant Name-

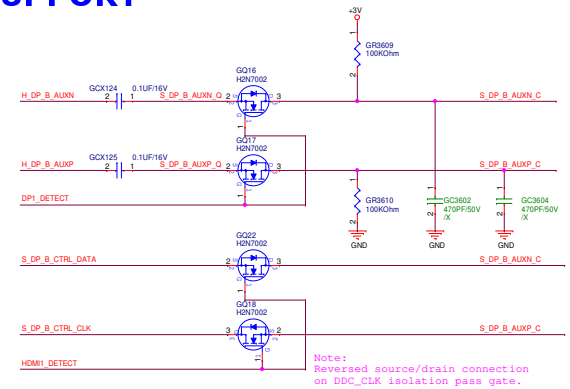
ASUSTeK COMPUTER INC.		Title : SLOT_EXT_PCI_1_3	
		Engineer: IPC-EE3	
Size: A1	Project Name: ATX-Q670B		Rev: 1.00
Date: Friday, May 30, 2008		Sheet 38 of 50	



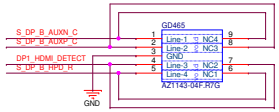




DP/HDMI INTEROPERABILITY SUPPORT

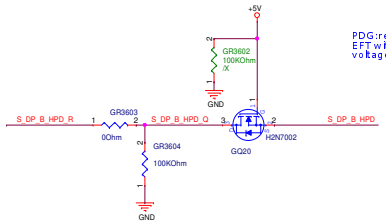


ESD

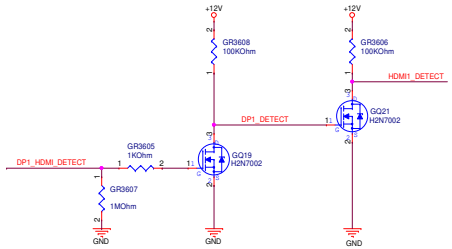


HPD

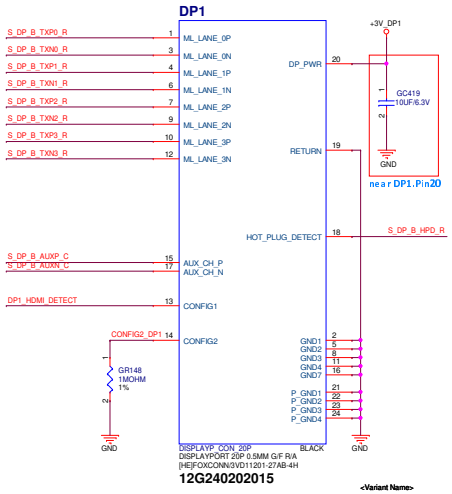
PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V



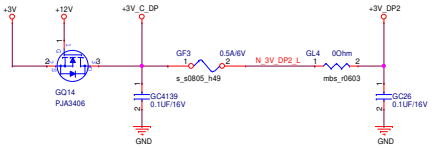
For HDMI/DP detect

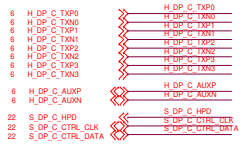


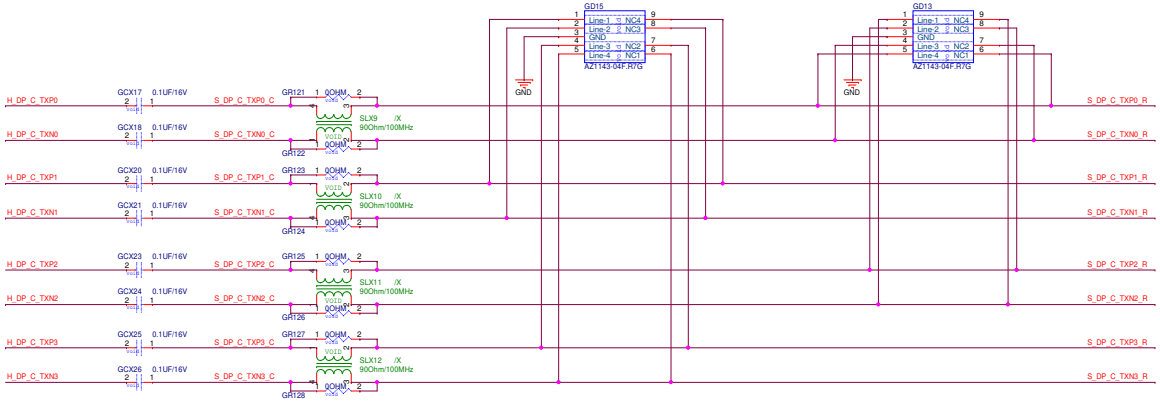
DP-1 (Port B)



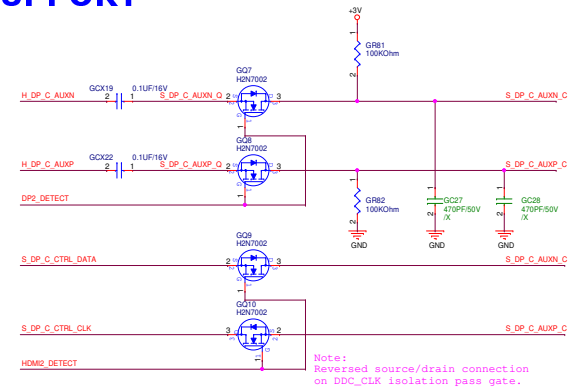
connector



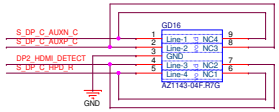




DP/HDMI INTEROPERABILITY SUPPORT

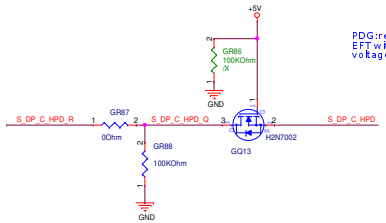


ESD

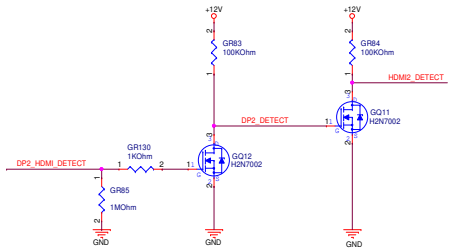


HPD

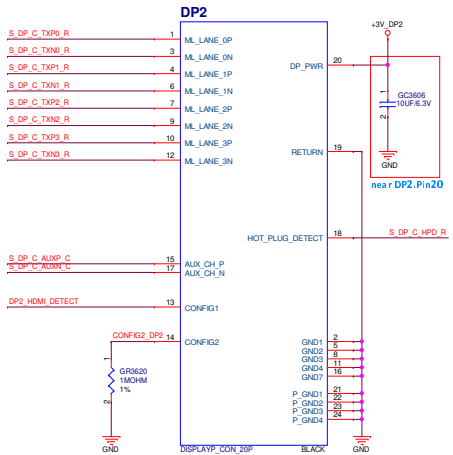
PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V

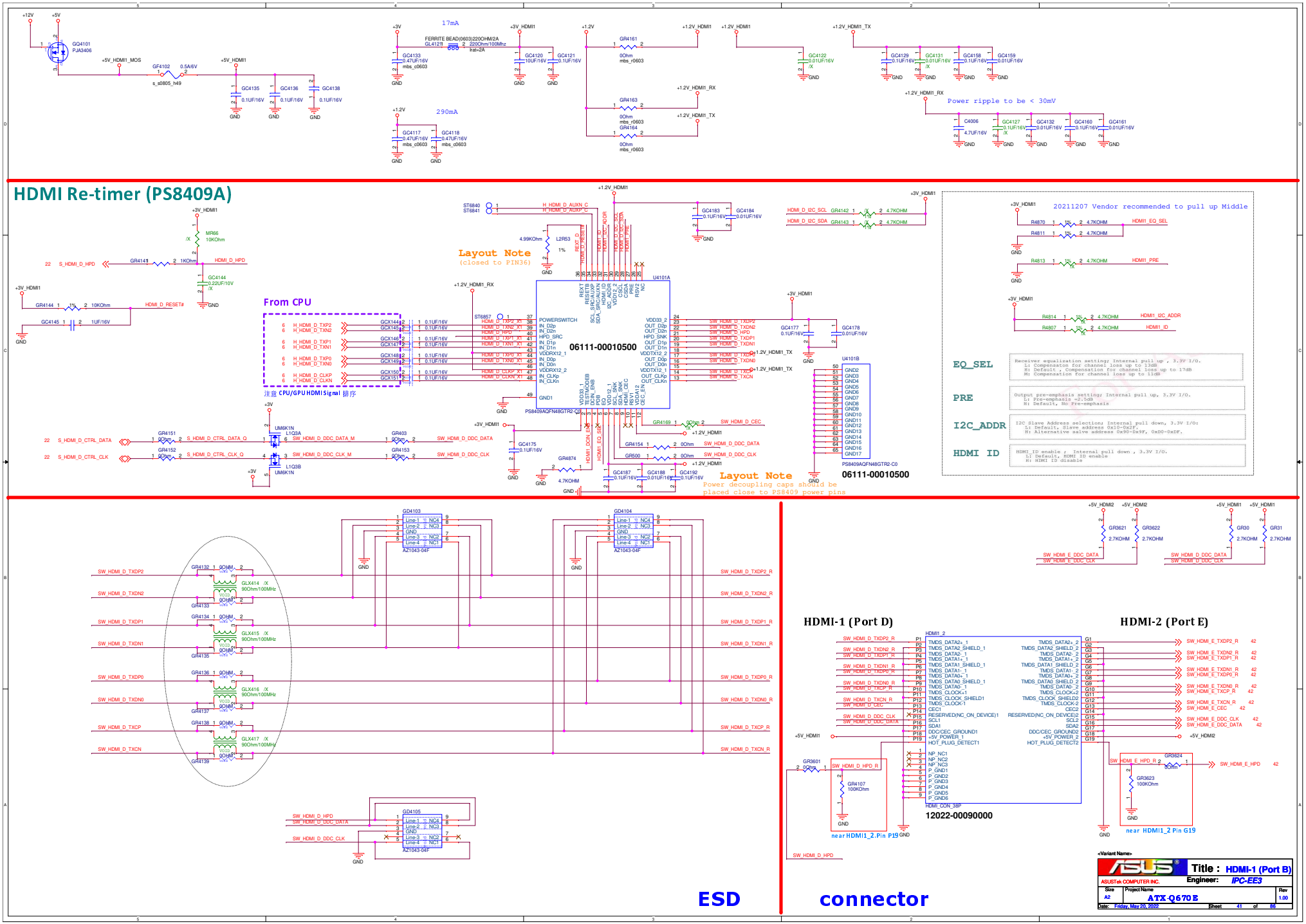


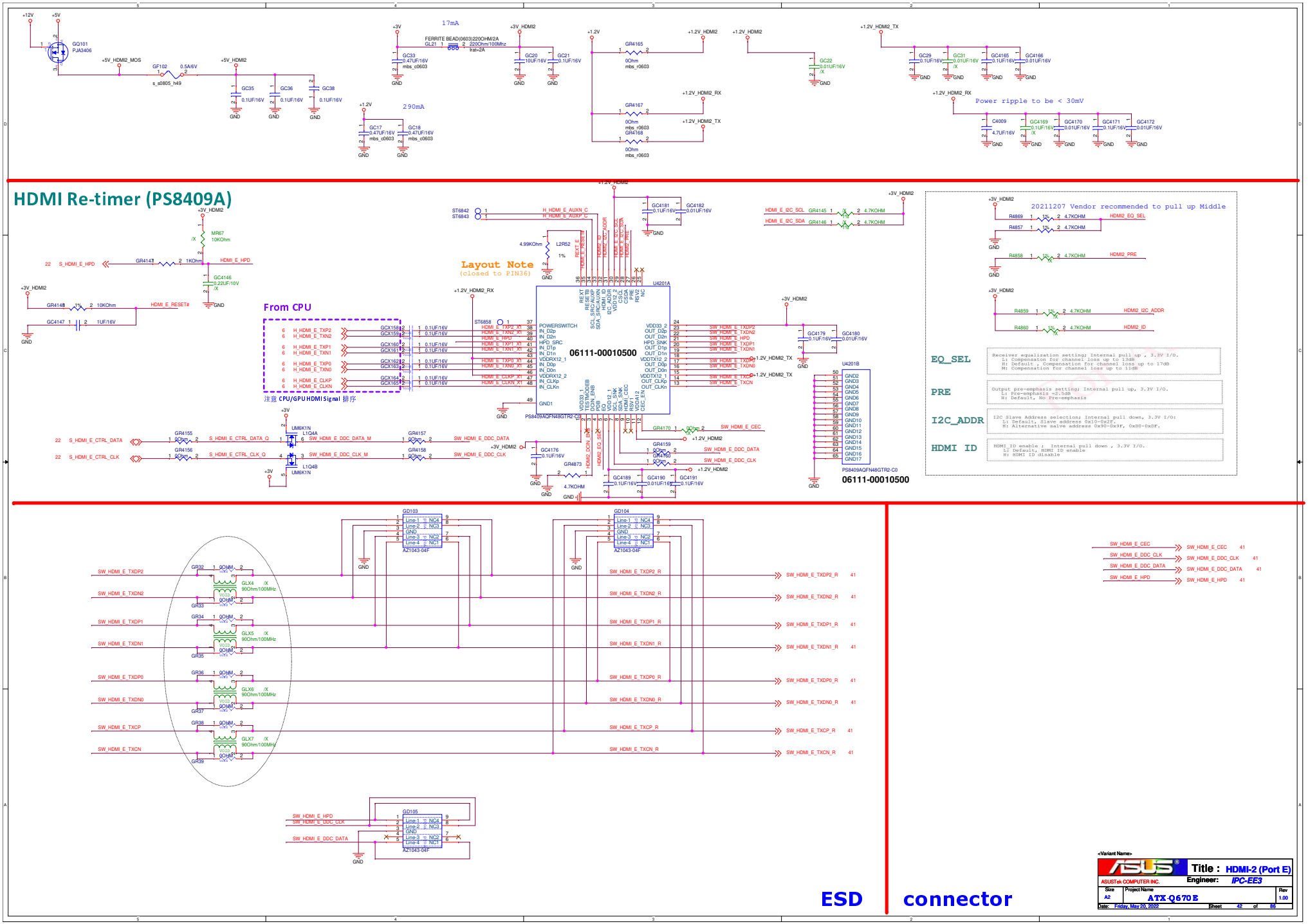
For HDMI/DP detect

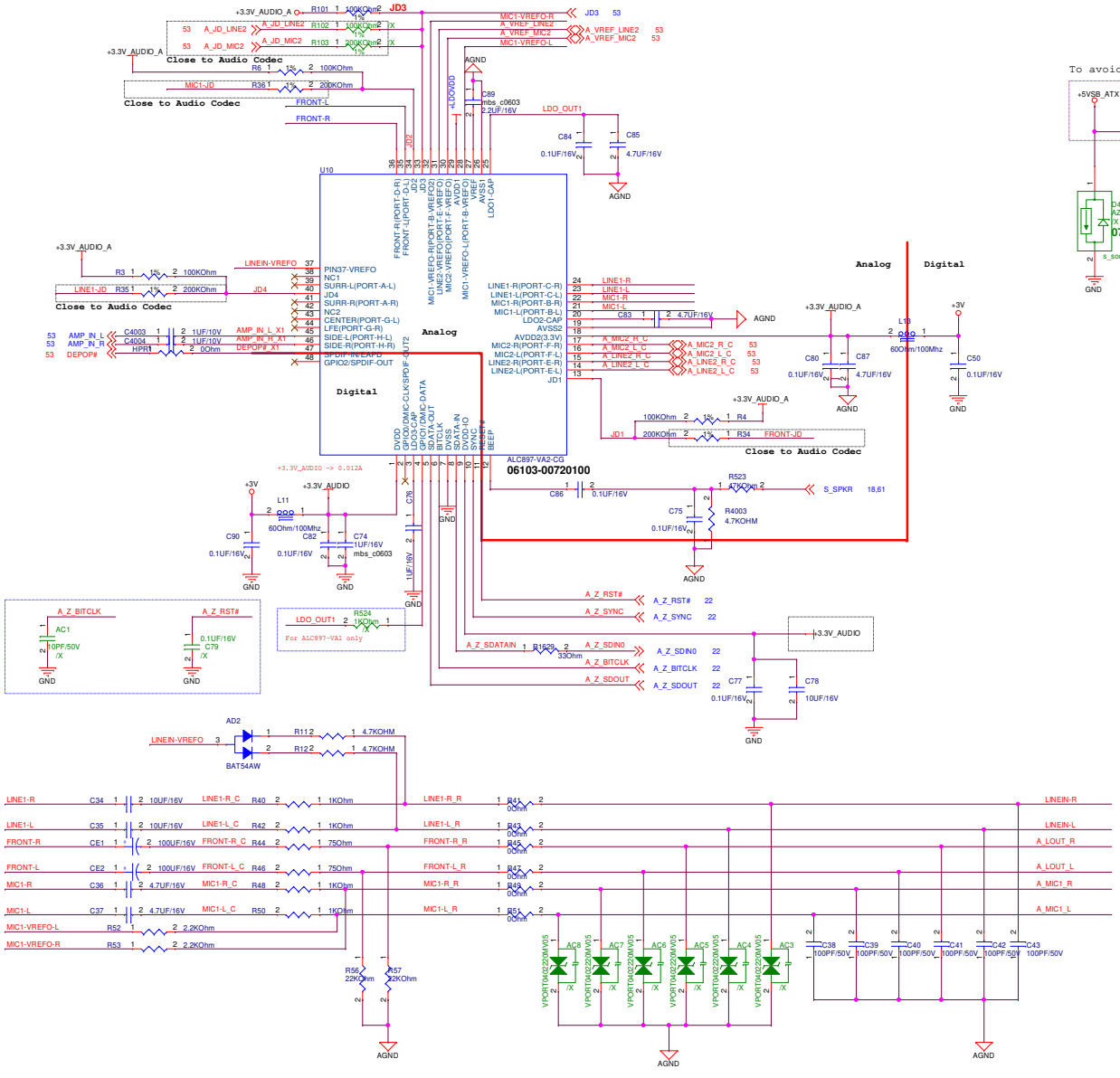


DP-2 (Port C)



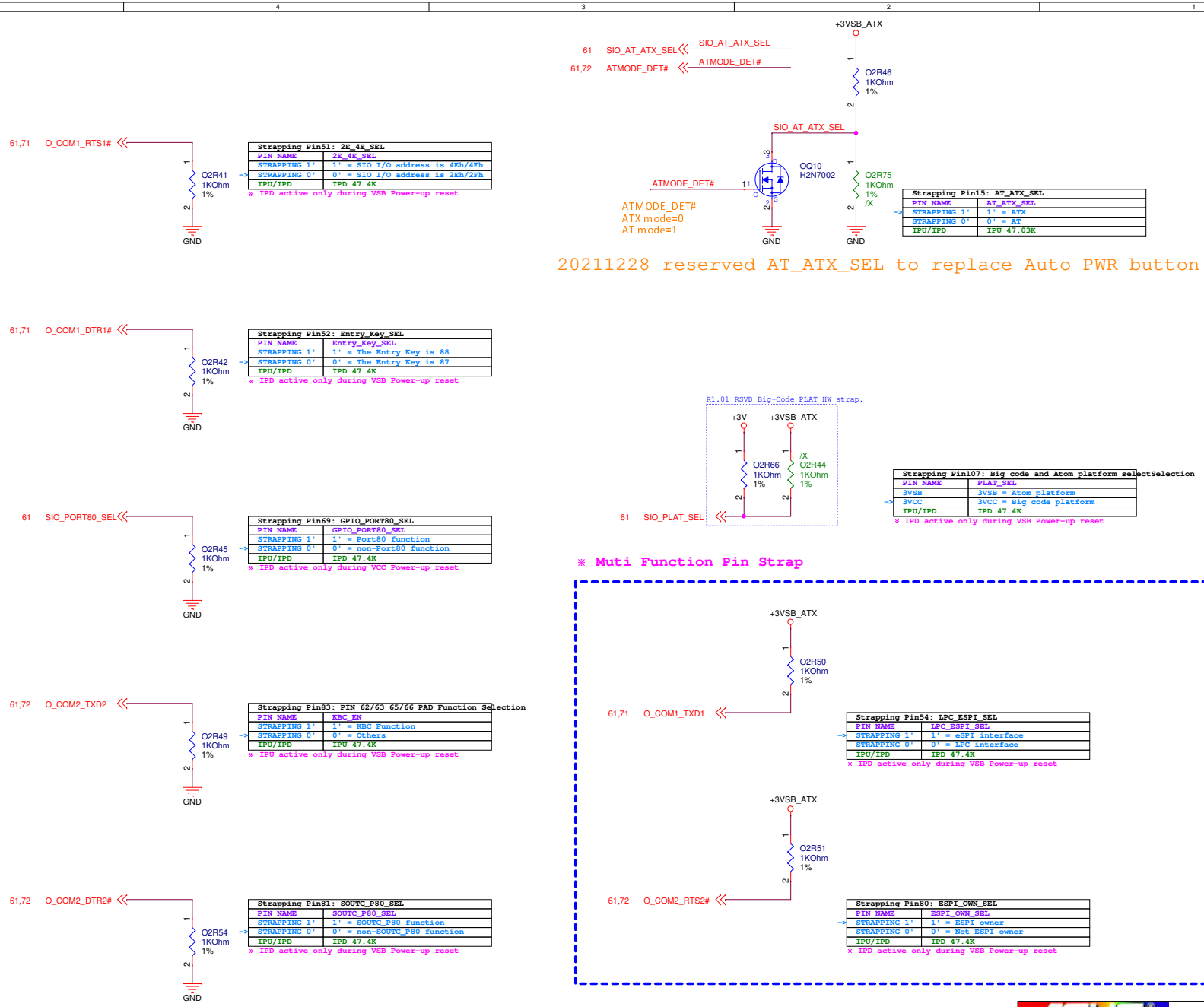

HDMI Re-timer (PS8409A)
17mA
290mA
Power ripple to be < 30mV
Layout Note
(closed to PIN36)
From CPU
注意 CPU/GPU HDMI Signal 排序
06111-00010500
PS8409AQFN48GTR2-C0
Layout Note
Power decoupling caps should be placed close to PS8409 power pins
20211207 Vendor recommended to pull up Middle
EQ_SEL
PRE
I2C_ADDR
HDMI ID
ESD
HDMI-1 (Port D)
HDMI-2 (Port E)
12022-00090000
connector
ASUS
Title : HDMI-1 (Port B)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size A2
Project Name ATX-Q670 E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 41 of 86


HDMI Re-timer (PS8409A)
Layout Note
(closed to PIN36)
From CPU
注意 CPU/GPU HDMI Signal 排序
06111-00010500
PS8409AQFN48GTR2-C0
20211207 Vendor recommended to pull up Middle
EQ_SEL
PRE
I2C_ADDR
HDMI ID
Power ripple to be < 30mV
17mA
290mA
ESD
connector
Title : HDMI-2 (Port E)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
ATX-Q670 E
Date: Friday, May 20, 2022
Sheet 42 of 86



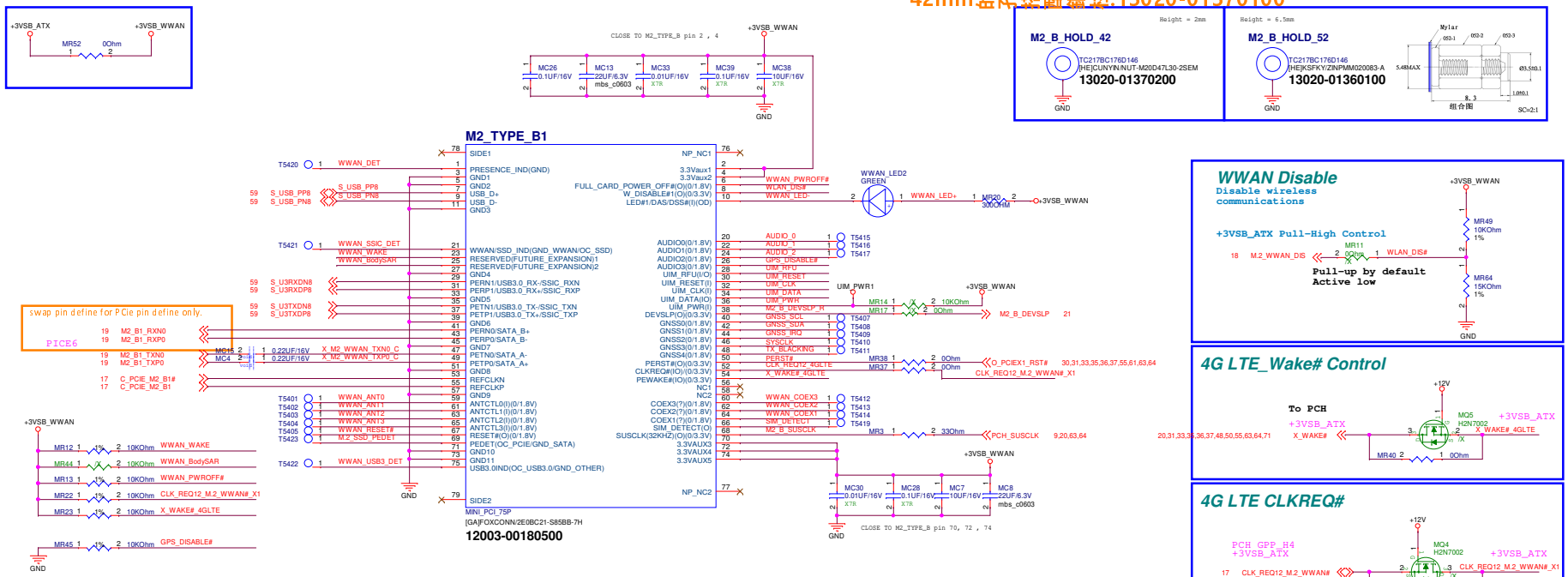
<Variant Name>

ASUSTeK COMPUTER INC.	Title : AUDIO CODEC ALC897	
	Engineer: IPC-EE3	
Size: C	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 43 of 90	

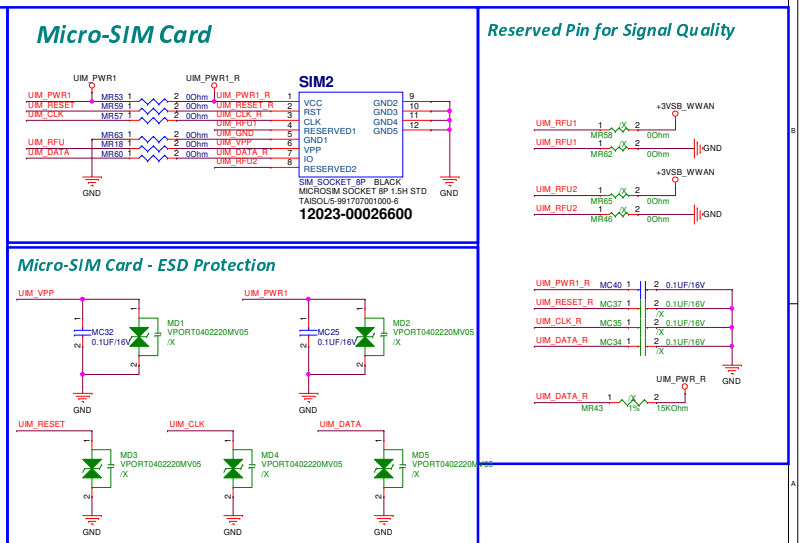


ASUSTek COMPUTER INC.	Title : SIO PIN STRAP
	Engineer: IPC-EE3
Size: A3	Project Name: ATX-Q670E
Rev: R1.02	
Date: Friday, May 20, 2022	Sheet 44 of 90

42mm密合螺距要求:13020-01370100



20220118 remove the SATA/PCIE DET circuits



<Variant Name>

ASUSTeK COMPUTER INC.	Title : M.2_Key-B_LTE	Engineer: IPC-EE3
Size C	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 45 of 86	

若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.

R1.00
Ref to page.104 +5VDUAL/5V_DUAL_USBKB*

+L1_I218_+3VSB
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.

1.3

Standard Circuit	
LAN	I218V
REV.	L1_1.3

/X

I218V

PCIE IF
勿接在chipset PCIE port0

17 C_PCIE_L1
17 C_PCIE_L1#
19 X_L1X1_RXP
19 X_L1X1_RXN
19 X_L1X1_TXP
19 X_L1X1_TXN

L1CX1 2 1 0.1UF/16V X_L1X1_RXP_C 38 PETp
L1CX2 2 1 0.1UF/16V X_L1X1_RXN_C 39 PETn
SL1CX3 2 1 0.1UF/16V X_L1X1_TXP_C 41 PERp
SL1CX4 2 1 0.1UF/16V X_L1X1_TXN_C 42 PERn
Close to PHY

23,50 L1_SMBCLK 28 SMB_CLK
23,50 L1_SMBDATA 31 SMB_DATA

L1C1 2 1 15PF/50V NPO /X
L1C2 2 1 15PF/50V NPO /X
GND Close to PHY

20 L1_LAN_DISABLE# 3 LAN_DISABLE_N

L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.

L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

L1R100 1 2 8.2KOhm /X
L1R101 1 2 8.2KOhm /X
+L1_I219_+3VSB

+L1_I219_+3VSB
LT1 LT2 GND
L1R18 1 8.2KOhm 2 /X L1_TP_JDI 32 JTAG_TDI
L1R19 1 8.2KOhm 2 /X L1_TP_TDO 34 JTAG_TDO
L1_TMS 33 JTAG_TMS
L1_TCK 35 JTAG_TCK

L1R20 1 2.7KOHM 2 L1_TESTEN 30 TEST_EN
GND
CRB 1K

+L1_I219_+3VSB CRB : L1R3 UNSTUFF FOR LPT-H
L1R9 10KOhm 1 2 L1_CLKREQN 48 CLK_REQ_N
L1R3 0Ohm 2 1
17 CLK_REQ8_LAN#

12,18,48,50,61,67 S_PLTRST# 36 PE_RST_N
L1C29 2 1 10PF/50V NPO /X
GND

Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0

+L1_I219_0.9V
L1U1C8 0.1UF/16V /X
L1U1C16 0.1UF/16V /X
L1U1C40 0.1UF/16V /X
L1U1C47 0.1UF/16V /X
GND

46 VDD0P9_46
47 VDD0P9_47
37 VDD0P9_37
43 VDD0P9_43
11 VDD0P9_11
8 VDD0P9_8
40 VDD0P9_40
22 VDD0P9_22
16 VDD0P9_16

L1L1 4.7UH 1 2 L1_CTRLP 7 CTRL0P9
L1U1C50 10UF/16V /X
L1U1C49 0.1UF/16V /X
L1U1C7 22UF/6.3V X5R
GND
L1L1
Idc_min=500 mA
Rdc_max=100 mohm
Placement rule:
1.Place close to L1U1
2.Trace length < 500mil
3.Trace wide > 20mil

L1_CTRLP
請注意灰框net為Switching power noise較大的地方
1. 所有訊號需距離灰框net至少30 mil
2. 所有訊號請勿reference該power plane
3. 該power net請reference GND plane並與其他GND切割,
   follow switching power phase的做法
4. L1L1元件中間請勿走線
5. L1_CTRLP長度勿超過100mil,越短越好

L1U1
PE_CLKP 44
PE_CLKN 45
WGI219LM
06112-00020100
GND1 50 GND2 51 GND3 52 GND4 53
GND

MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch

MDI_PLUS[0] 13 L1_MDI_0+ 47
MDI_MINUS[0] 14 L1_MDI_0- 47
MDI_PLUS[1] 17 L1_MDI_1+ 47
MDI_MINUS[1] 18 L1_MDI_1- 47
MDI_PLUS[2] 20 L1_MDI_2+ 47
MDI_MINUS[2] 21 L1_MDI_2- 47
MDI_PLUS[3] 23 L1_MDI_3+ 47
MDI_MINUS[3] 24 L1_MDI_3- 47

XTAL_OUT 9 L1_XOUT
XTAL_IN 10 L1_XIN
L1X1 25Mhz XTAL 25MHZ SMD 10PF/20PPM [GA]EPSON/FA-238
L1C7 12PF/50V NPO
L1C8 10PF/50V NPO
GND

L1X1,L1C7,L1C8
Placement rule:
1.Place close to L1U1
2.Trace length <1inch

+L1_I219_+3VSB
L1R2 300OHM
L1_ACTLEDP 47

LED2 25 L1_LED2 L1R1 1 2 300OHM L1_LINK100# 47
LED1 27 L1_LINK1000# 47
LED0 26 L1_ACTLEDN 47

CRB pull up 4.7Kohm
VDD3P3_IN 5 Close to pin5
L1U1C5 0.1UF/16V
L1U1C48 22UF/6.3V X5R
GND
+L1_I219_+3VSB
L1R21 8.2KOhm
L1R4 4.7KOHM /X
L1R22 8.2KOhm

RSVD1_VCC3P3 1 L1_RSVD
LANWAKE_N 2
SVR_EN_N 6 L1_SVR_EN
L1R26 0Ohm
GND
L1_LAN_WAKE# 20,50

L1_LAN_WAKE#
Must be connected to PCH's LANWAKE

L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電

+L1_I219_+3VSB
VDD3P3_4 4
VDD3P3_15 15
VDD3P3_19 19
VDD3P3_29 29
L1U1C4 1UF/16V
GND

RBIAS 12 L1_RBIAS L1R16 1 3.01KOHM 1% 2
GND_EPAD 49
GND

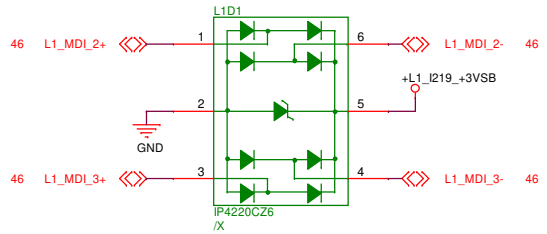
L1R16
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch

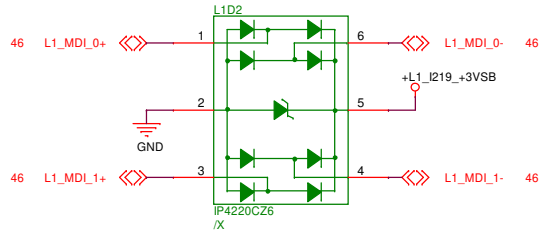
06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)

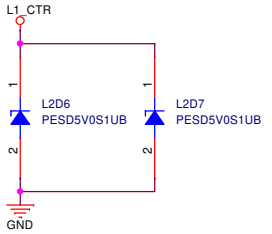
06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)

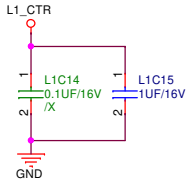
<Variant Name>

ASUS	Title :	L1_I219V
ASUSTek COMPUTER INC.	Engineer:	IPC-EE3
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 46 of 90	

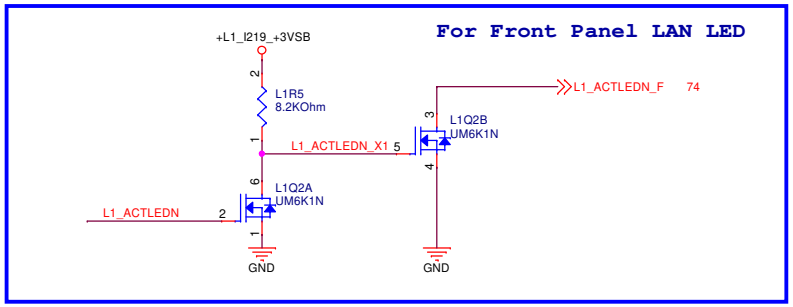


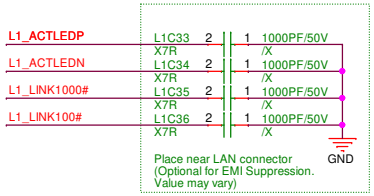


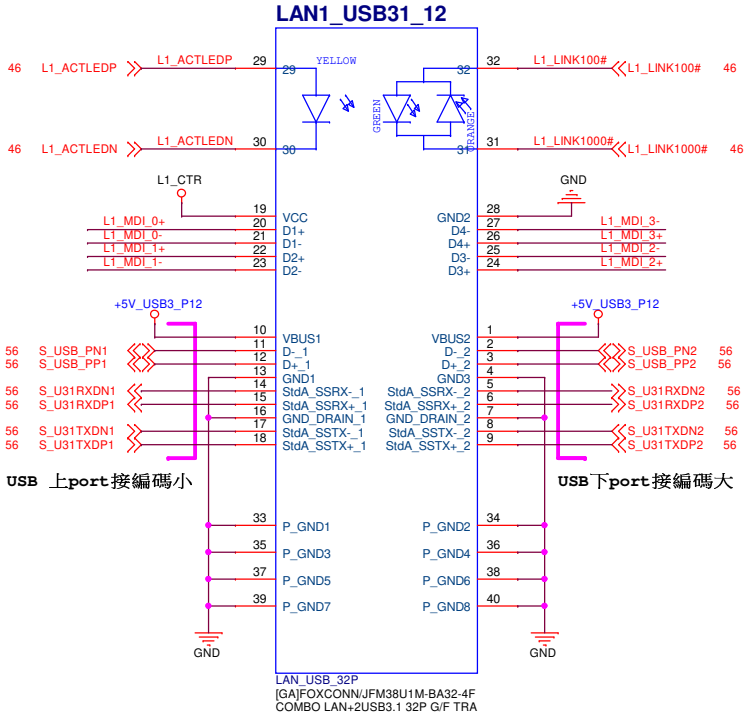


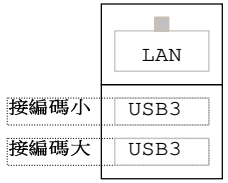


202120106 Add L1_ACTLEDN_F to front panel



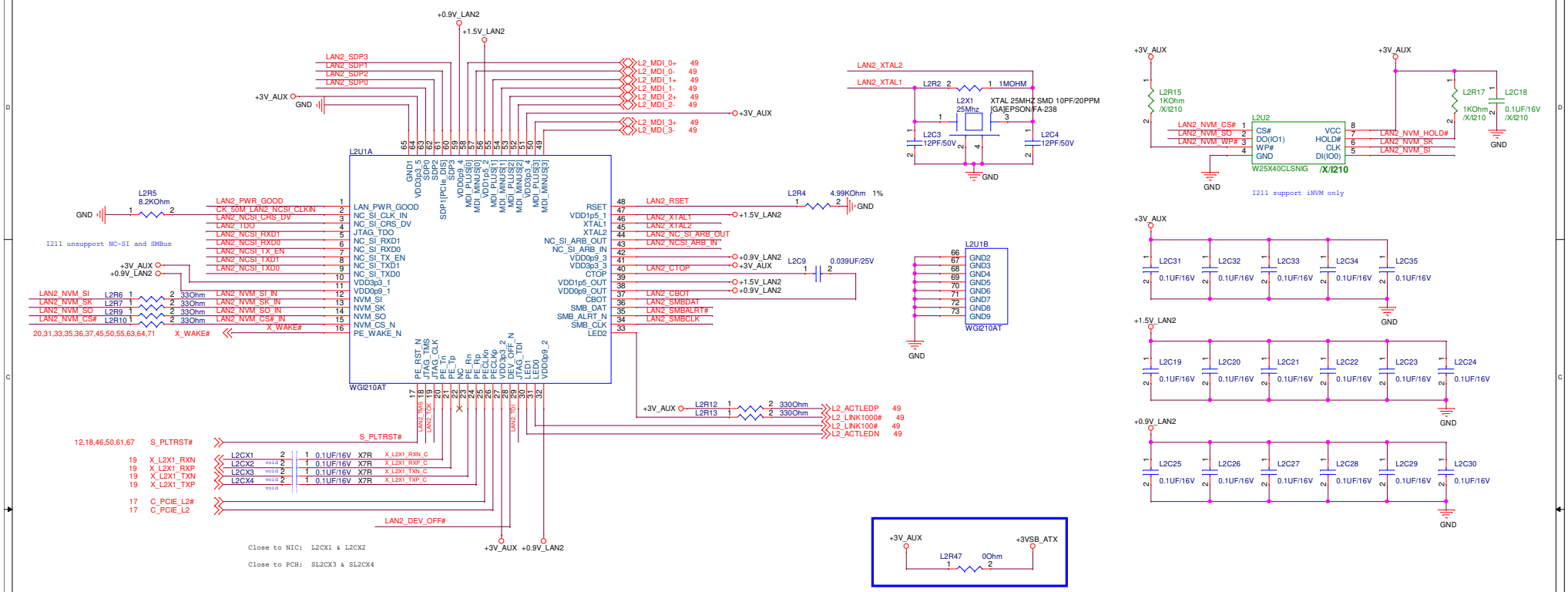




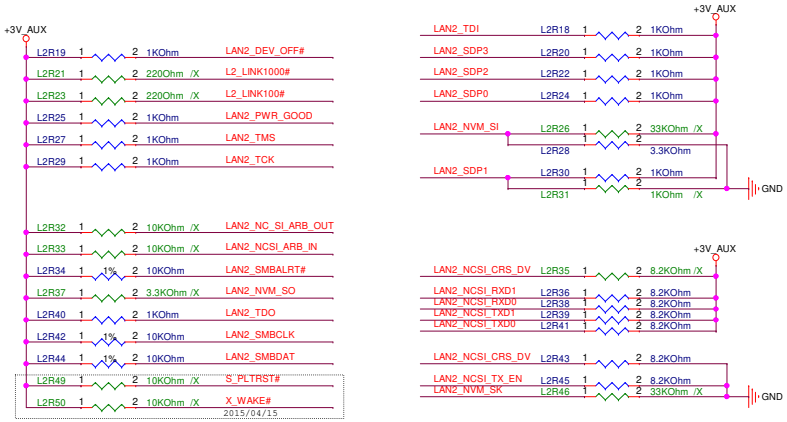


<Variant Name>

ASUSTek COMPUTER INC.	Title : L1_I219LM (Connector)	
	Engineer: IPC-EE3	
Size B	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 47 of 90	

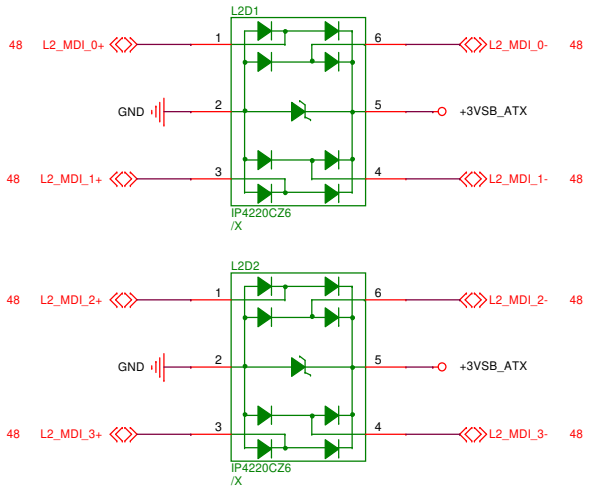


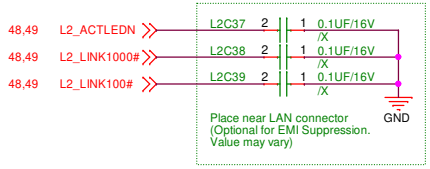
Follow CRB A.B.



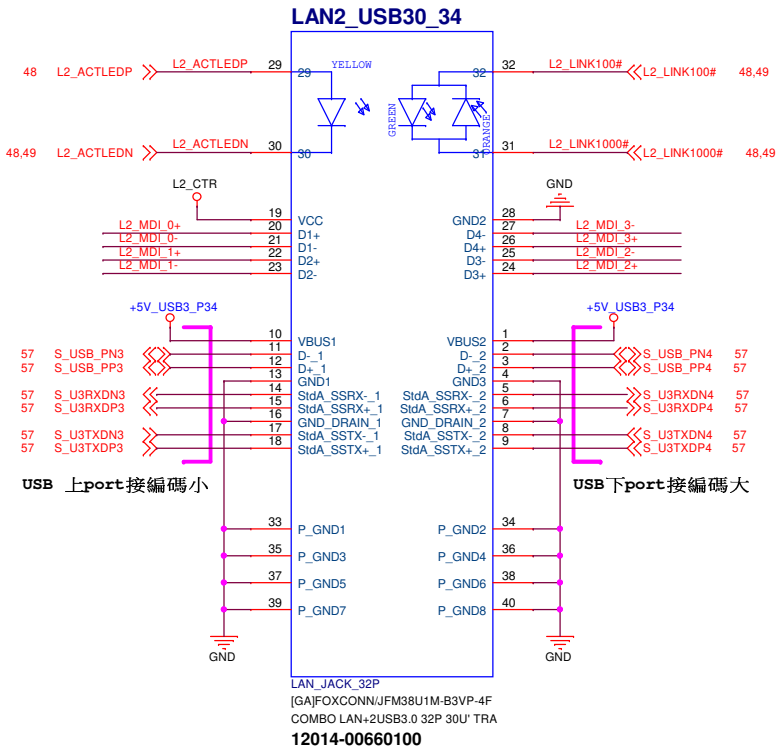
Strapping Options

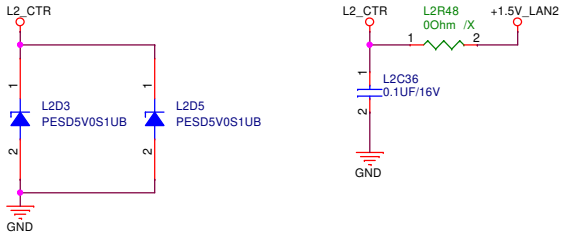
```
DEV_OFF_N
 I210.28 (DEV_OFF_N)
   1: Exit Device off mode (Default)
   0: Enter Device off mode


AUX_PWR
 I210.28 (DEV_OFF_N)
 I210.60 (SDP3)
   11: Enable AUX power mode (Default)


Security_EN
 I210.12 (NVM_SI)
   1: Enable Flash security
   0: Disable Flash security (Default)


PCIE_DIS_N
 I210.61 (SDP1[PCIe_DIS])
   1: Enable PCIe function (Default)
   0: Disable PCIe function
```



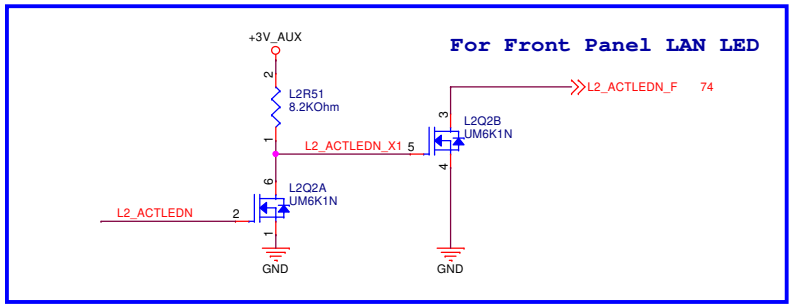


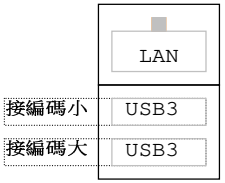
20211111 Nick modify, with I210





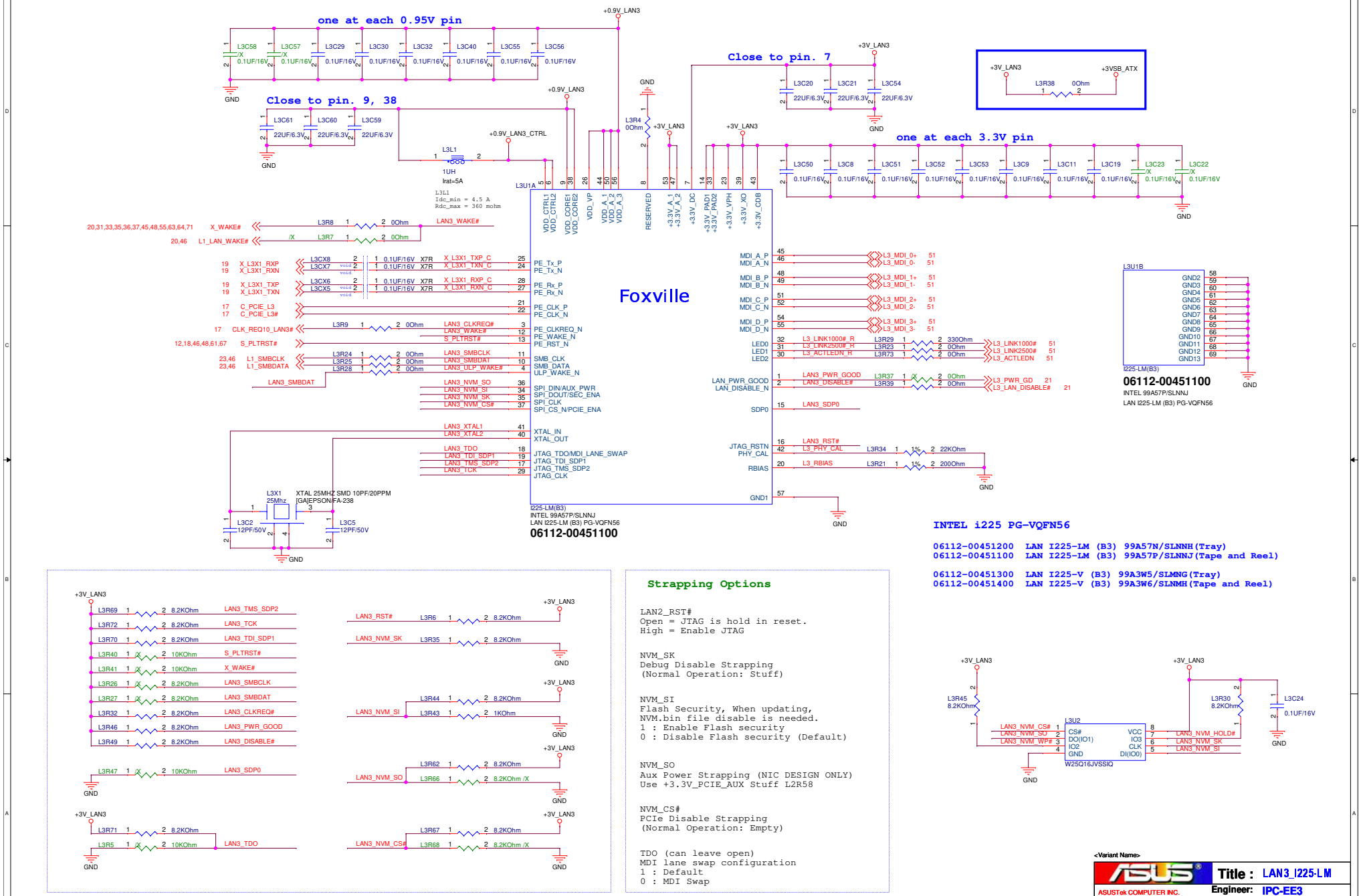
202120106 Add L2_ACTLEDN_F to front panel

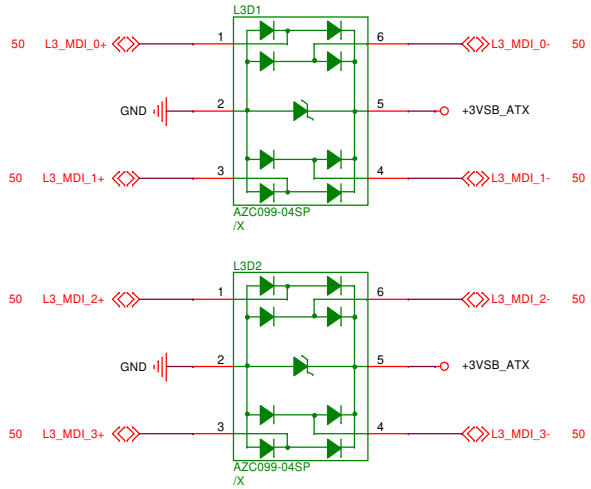


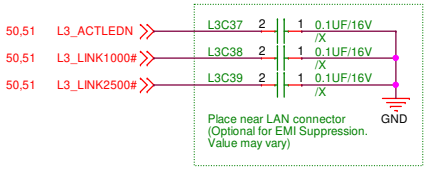


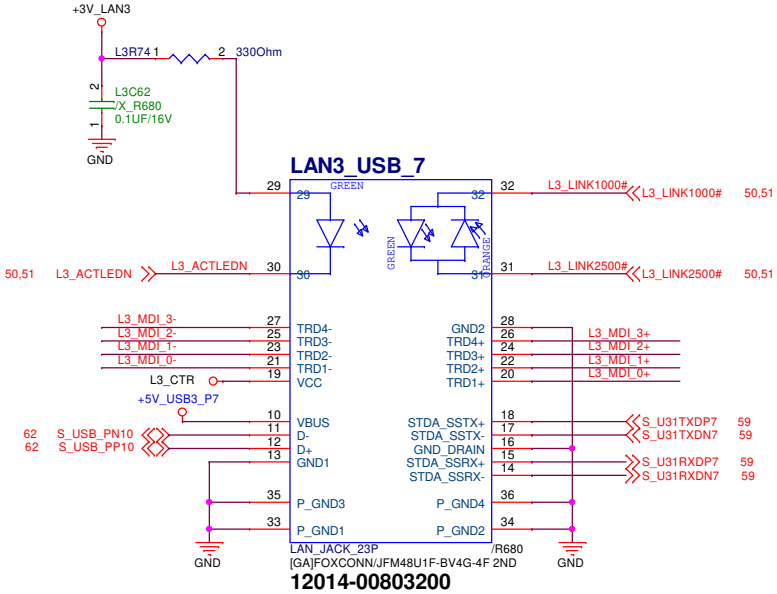
<Variant Name>

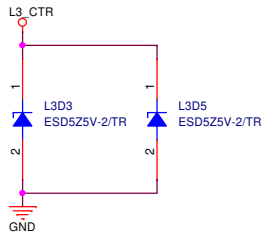
ASUSTek COMPUTER INC.	Title : LAN2_RJ45	
	Engineer: IPC-EE3	
Size: Custom	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 49 of 90	

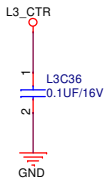

one at each 0.95V pin
Close to pin. 9, 38
Close to pin. 7
one at each 3.3V pin
Foxville
06112-00451100
INTEL 99A57P/SLNNJ
LAN I225-LM (B3) PG-VQFN56
L3U1A
L3U1B
L3U2
W25Q16JVSSIQ
L3X1 25Mhz
XTAL 25MHZ SMD 10PF/20PPM
[GA]EPSON/FA-238
L3L1
1UH
Irat=5A
L3L1
Idc_min = 4.5 A
Rdc_max = 360 mohm
+0.9V_LAN3
+3V_LAN3
+3VSB_ATX
+0.9V_LAN3_CTRL
GND
X_WAKE#
L1_LAN_WAKE#
LAN3_WAKE#
CLK_REQ10_LAN3#
S_PLTRST#
L1_SMBCLK
L1_SMBDATA
LAN3_SMBDAT
LAN3_NVM_SO
LAN3_NVM_SI
LAN3_NVM_SK
LAN3_NVM_CS#
LAN3_XTAL1
LAN3_XTAL2
LAN3_TDO
LAN3_TDI_SDP1
LAN3_TMS_SDP2
LAN3_TCK
LAN3_CLKREQ#
LAN3_PWR_GOOD
LAN3_DISABLE#
LAN3_SDP0
LAN3_RST#
LAN3_PHY_CAL
LAN3_RBIAS
LAN3_LINK1000#
LAN3_LINK2500#
LAN3_ACTLEDN
L3_LAN_DISABLE#
L3_PWR_GD
INTEL i225 PG-VQFN56
06112-00451200 LAN I225-LM (B3) 99A57N/SLNNH(Tray)
06112-00451100 LAN I225-LM (B3) 99A57P/SLNNJ(Tape and Reel)
06112-00451300 LAN I225-V (B3) 99A3W5/SLMNG(Tray)
06112-00451400 LAN I225-V (B3) 99A3W6/SLNMH(Tape and Reel)
Strapping Options
LAN2_RST#
Open = JTAG is hold in reset.
High = Enable JTAG
NVM_SK
Debug Disable Strapping
(Normal Operation: Stuff)
NVM_SI
Flash Security, When updating,
NVM.bin file disable is needed.
1 : Enable Flash security
0 : Disable Flash security (Default)
NVM_SO
Aux Power Strapping (NIC DESIGN ONLY)
Use +3.3V_PCIE_AUX Stuff L2R58
NVM_CS#
PCIe Disable Strapping
(Normal Operation: Empty)
TDO (can leave open)
MDI lane swap configuration
1 : Default
0 : MDI Swap
Title : LAN3_I225-LM
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 50 of 90



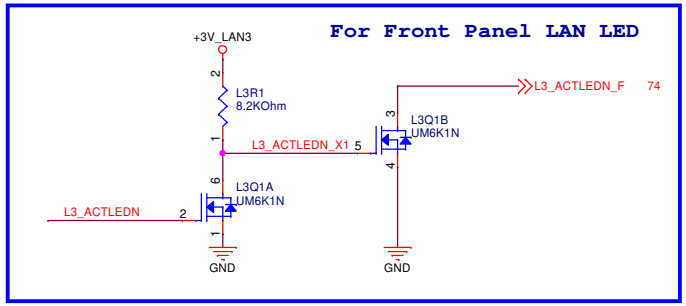








202120106 Add L3_ACTLEDN_F to front panel

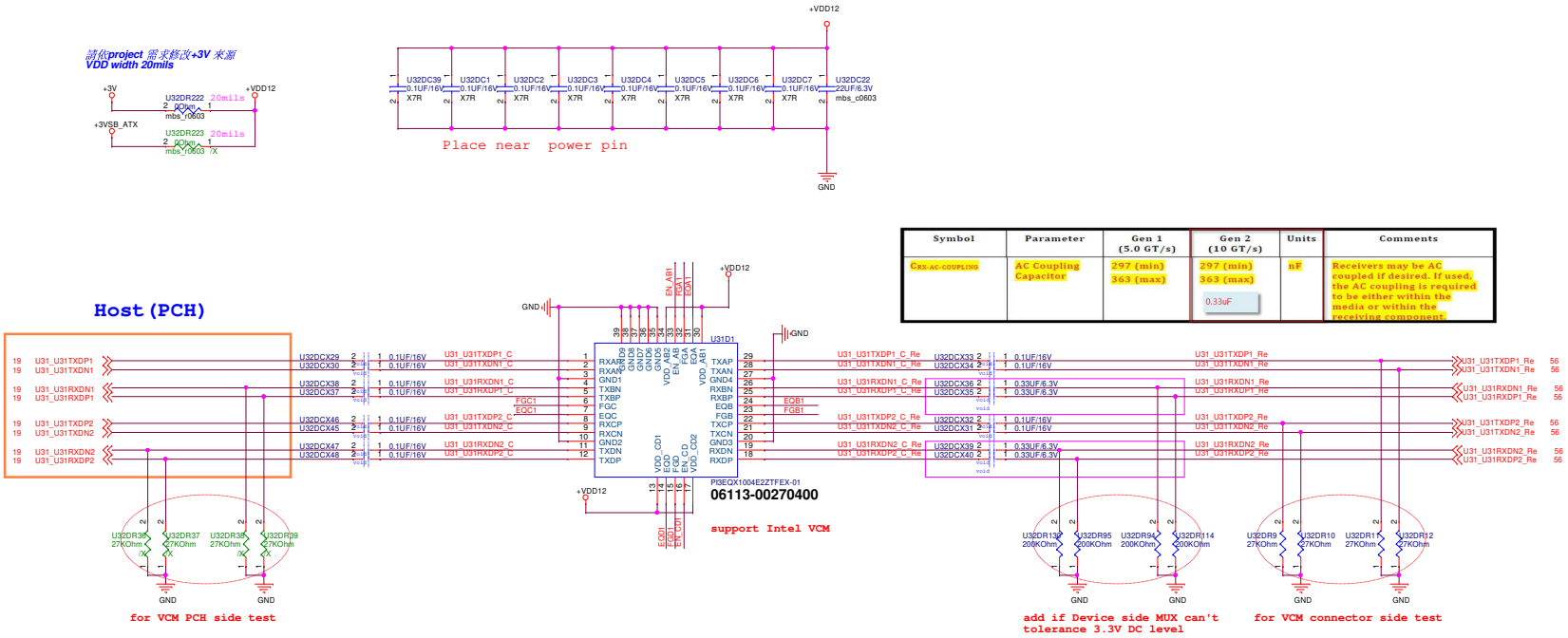


LED Configuration #1 Expected Behavior

Speed LED		
10 Mbps	OFF	
100 Mbps	OFF	
1000 Mbps	Yellow	←2nd Highest Speed
2500 Mbps	Green	←Highest Speed
Link-Activity LED		
Link-up	Green	
Tx/Rx Activity	Blinking Green	

<Variant Name>

ASUSTek COMPUTER INC.	Title : LAN3_RJ45	
	Engineer: IPC-EE3	
Size: Custom	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 51 of 90	



Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
CRX-AC-COUPLING	AC Coupling Capacitor	297 (min) 363 (max)	297 (min) 363 (max) 0.33uF	nF	Receivers may be AC coupled if desired. If used, the AC coupling is required to be either within the media or within the receiving component.

Strapping pin

FGA1/B1/C1/D1	Flat Gain(db)
pull up	+2.7
pull down	-0.5
F(Leave oprn)	1.0(Default)
R (Tie Rext to Gnd)	-1.6

Strapping pin

EQA1/B1/C1/D1	Equalizer 2.5G/5G (db)
pull up	8.4/14.6
pull down	6.7/12.4
F(Leave oprn)	5.3/10.6(Default)
R (Tie Rext to Gnd)	3.5/8

Channel Enable

EN	Setting
Pull up (Internal P-U)	Enable(Default)
pull down	Disable

Post-channel / Pre-channel	less than 2inch		2inch to 4inch		up to 4inch	
For PI3EQX1004/B1	TX	RX	TX	RX	TX	RX
under 7inch	EQA=68kohm to GND FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Pull low to GND	EQA=68kohm to GND FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Pull low to GND	EQA=68kohm to GND FGA=Floating	EQB=Floating FGB=Pull low to GND
7inch to 9inch	EQA=Floating FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Floating	EQA=Floating FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Floating	EQA=Floating FGA=Floating	EQB=Floating FGB=Floating
up to 12inch	EQA=1kohm to VDD FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=1kohm to VDD	EQA=1kohm to VDD FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=1kohm to VDD	EQA=1kohm to VDD FGA=Floating	EQB=Floating FGB=1kohm to VDD

<Variant Name>

ASUSTeK COMPUTER INC.

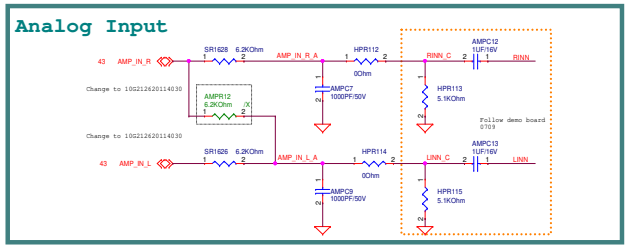
Title : U31 Ford 1,2 Re-driver IC

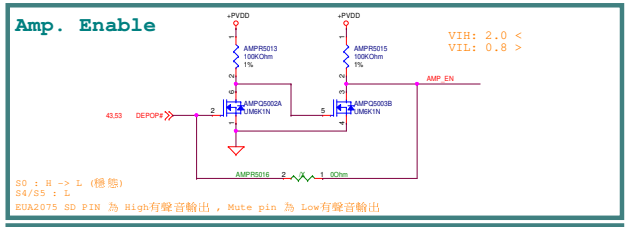
Engineer: IPC-EE3

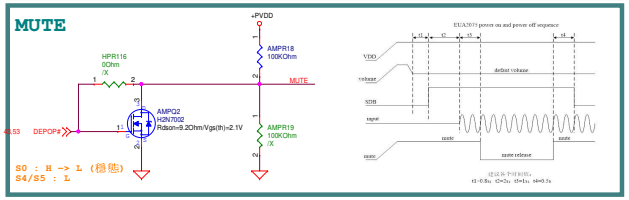
Size	Project Name	Rev
C	ATX-Q670E	1.00

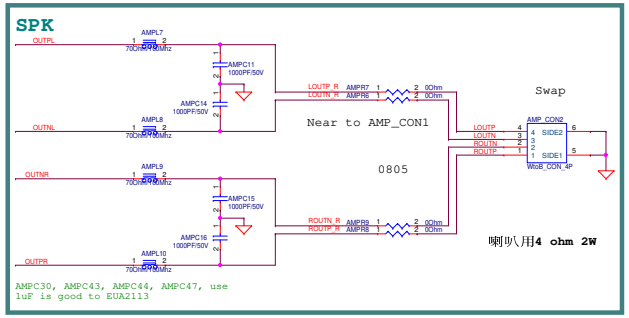
Date: Friday, May 20, 2022 Sheet 52 of 90

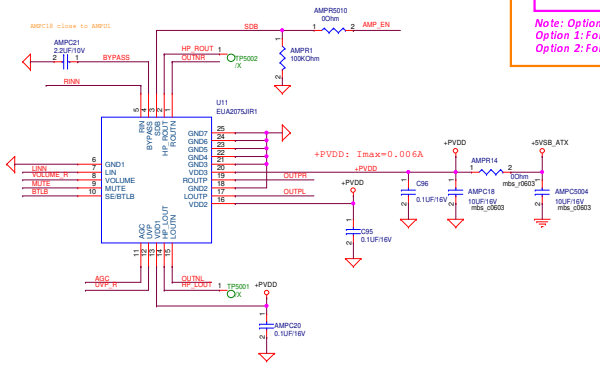
AMP - EUA2075JIR1 (Only Speaker)

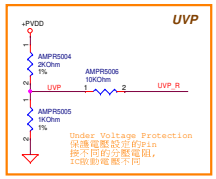




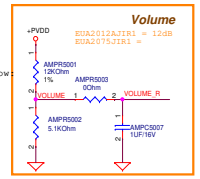








The thresholds can be determined as below:
With the condition: R3 >> R1//R2
V UVP =[1.2~(5.7μA×R3)]×(R1+R2)/R2
Hysteresis=(4.6μA×R3)×(R1+R2)/R2



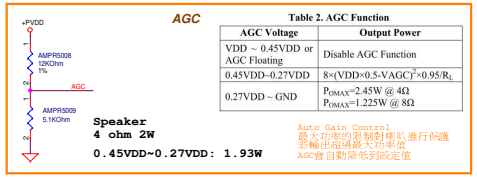
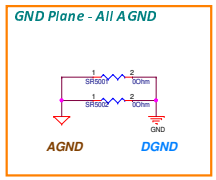


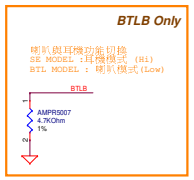
Table 2. AGC Function

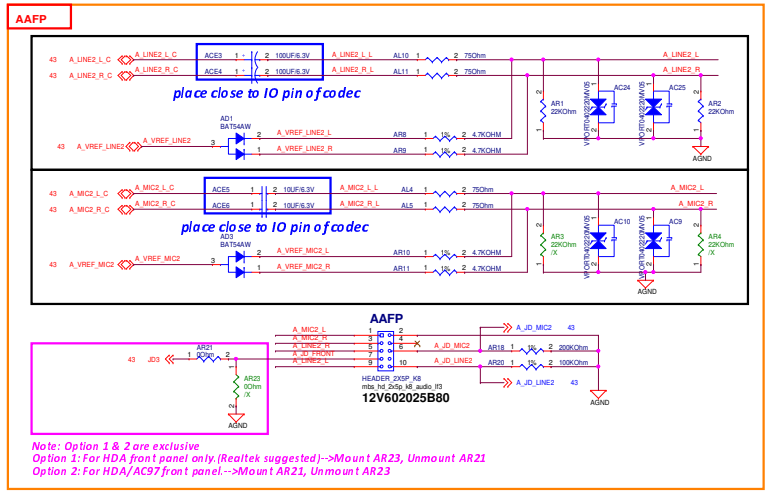
AGC Voltage	Output Power
VDD ~ 0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$8\times(VDD\times0.5-V_{AGC})^2\times0.95/R_L$
0.27VDD ~ GND	P_{OMAX}=2.45W @ 4Ω P_{OMAX}=1.225W @ 8Ω

Table 1. DC Volume Control

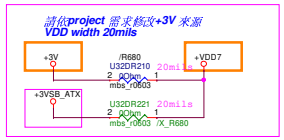
Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)
1	0.0 - 3.4	2.4 - 0.0	20.0
2	3.4 - 4.8	3.8 - 2.4	19.6
3	4.8 - 6.2	5.2 - 3.8	19.2
4	6.2 - 7.6	6.6 - 5.2	18.8
5	7.6 - 9.0	8.0 - 6.6	18.4
6	9.0 - 10.4	9.4 - 8.0	18.0
7	10.4 - 11.8	10.8 - 9.4	17.6
8	11.8 - 13.2	12.2 - 10.8	17.2
9	13.2 - 14.6	13.6 - 12.2	16.8
10	14.6 - 16.0	15.0 - 13.6	16.4
11	16.0 - 17.4	16.4 - 15.0	16.0
12	17.4 - 18.8	17.8 - 16.4	15.6
13	18.8 - 20.2	19.2 - 17.8	15.2
14	20.2 - 21.6	20.6 - 19.2	14.8
15	21.6 - 23.0	22.0 - 20.6	14.4
16	23.0 - 24.4	23.4 - 22.0	14.0
17	24.4 - 25.8	24.8 - 23.4	13.6
18	25.8 - 27.2	26.2 - 24.8	13.2
19	27.2 - 28.6	27.6 - 26.2	12.8
20	28.6 - 30.0	29.0 - 27.6	12.4
21	30.0 - 31.4	30.4 - 29.0	12.0

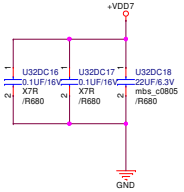




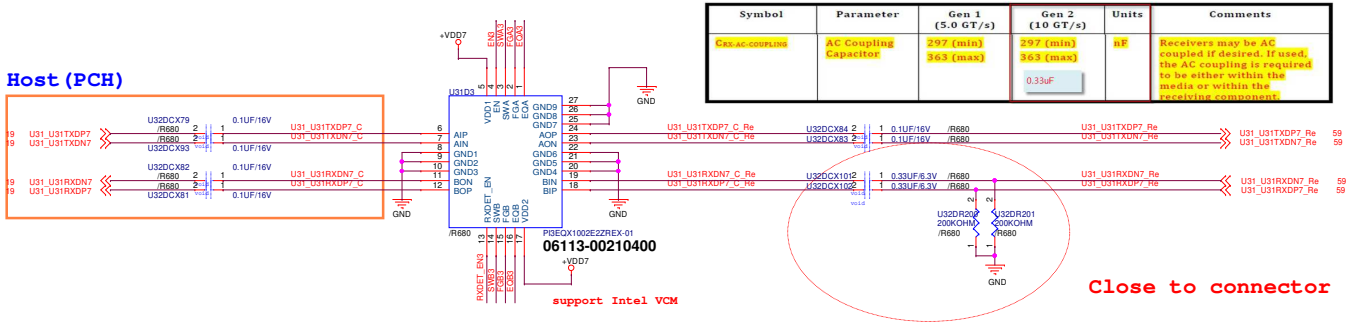


ASUSTEK COMPUTER INC	Title : AUDIO_AAFP_AMP		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: ATX-Q670E		Rev: 2.01
Date: Friday, May 20, 2022	Sheet 53 of 67		





Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$C_{TX-AC-COUPLING}$	AC Coupling Capacitor	297 (min) 363 (max)	297 (min) 363 (max) 0.33uF	nF	Receivers may be AC coupled if desired. If used, the AC coupling is required to be either within the media or within the receiving component.



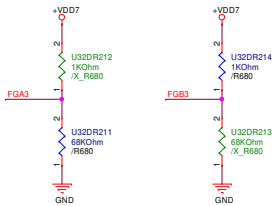
Post-channel / Pre-channel	less than 2inch		2inch to 4inch		up to 4inch	
For PI3EQX1002B/B1	TX	RX	TX	RX	TX	RX
under 7inch	EQA=68kohm to GND FGA=Pull low to 68kohm SWA=Floating	EQB=68kohm to GND FGB=Pull low to GND SWB=Floating	EQA=68kohm to GND FGA=Pull low to 68kohm SWA=Floating	EQB=68kohm to GND FGB=Pull low to GND SWB=Floating	EQA=68kohm to GND FGA=Floating SWA=Floating	EQB=68kohm to GND FGB=Pull low to GND SWB=Floating
7inch to 9inch	EQA=Floating FGA=Pull low to 68kohm SWA=Floating	EQB=68kohm to GND FGB=Floating SWB=Floating	EQA=Floating FGA=Pull low to 68kohm SWA=Floating	EQB=68kohm to GND FGB=Floating SWB=Floating	EQA=Floating FGA=Floating SWA=Floating	EQB=Floating FGB=Floating SWB=Floating
up to 12inch	EQA=1kohm to VDD FGA=Pull low to 68kohm SWA=Floating	EQB=68kohm to GND FGB=1kohm to VDD SWB=Floating	EQA=1kohm to VDD FGA=Pull low to 68kohm SWA=Floating	EQB=68kohm to GND FGB=1kohm to VDD SWB=Floating	EQA=1kohm to VDD FGA=Floating SWA=Floating	EQB=Floating FGB=1kohm to VDD SWB=Floating

Strapping pin

FGA3/B3	Flat Gain(db)
pull up	+2.7
pull down	-1.6
F(Leave oprn)	1.0(Default)
R(Tie Rext to Gnd)	-0.5

Rext = 68Kohm

Rext = 1Kohm for Current Limit

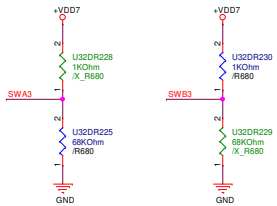


Strapping pin

SWA3/B3	Output Linear Swing Settings (mVppd)
pull up	1100
pull down	800
F(Leave oprn)	1000(Default)
R(Tie Rext to Gnd)	1200

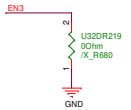
Rext = 68Kohm

Rext = 1Kohm for Current Limit



Channel Enable

EN3	Setting
Pull up (Internal PU)	Enable(Default)
pull down	Disable



Receiver Detection Setting

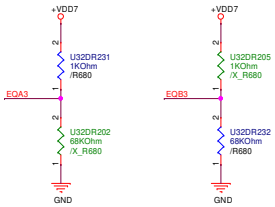
RXDET_EN3	Setting
Pull up (Internal PU)	Enable(Default)
pull down	Disable

Strapping pin

EQA3/B3	Equalizer 2.5G/5G (db)
pull up	8.4/14.6
pull down	6.7/12.4
F(Leave oprn)	5.3/10.6(Default)
R(Tie Rext to Gnd)	3.5/8

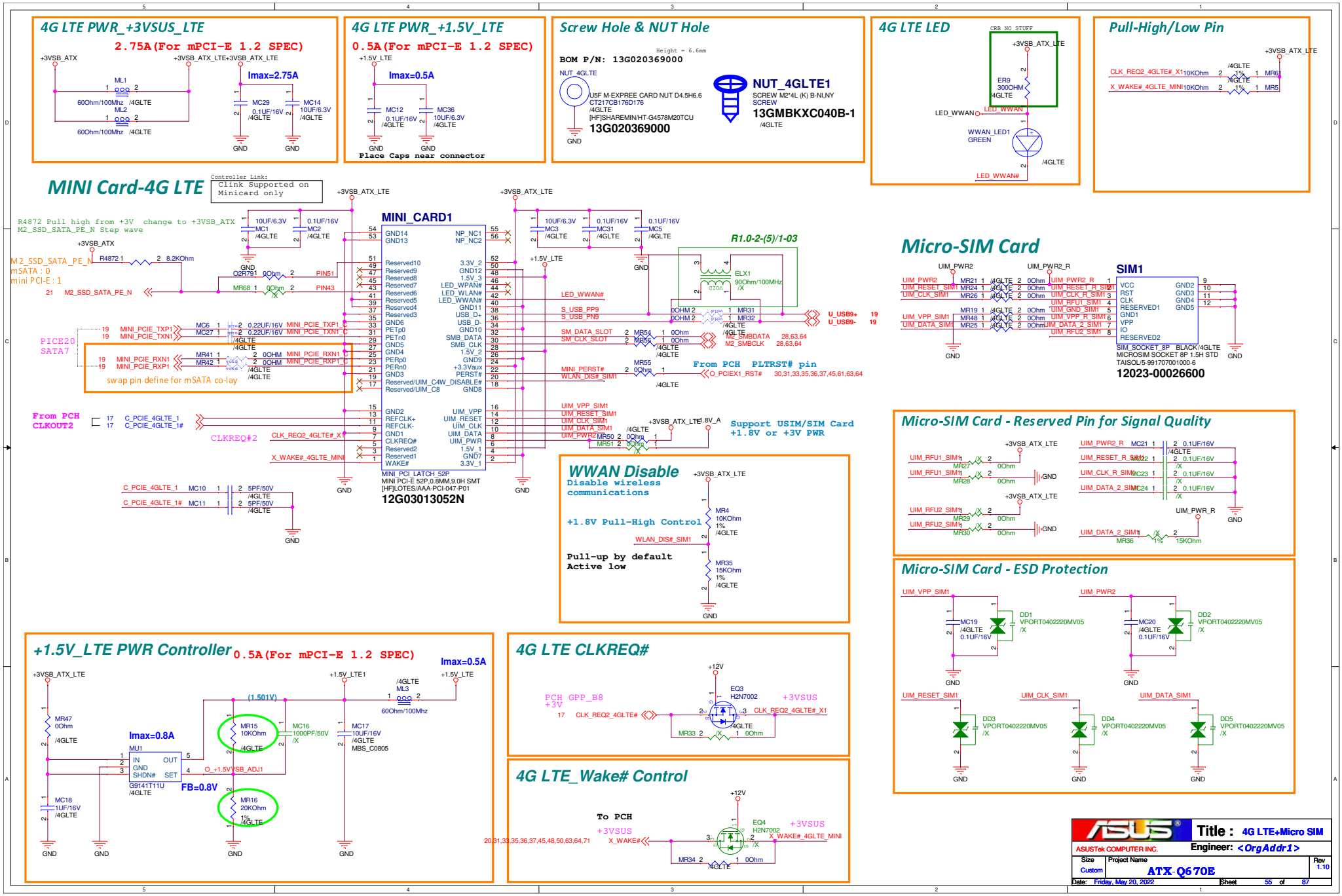
Rext = 68Kohm

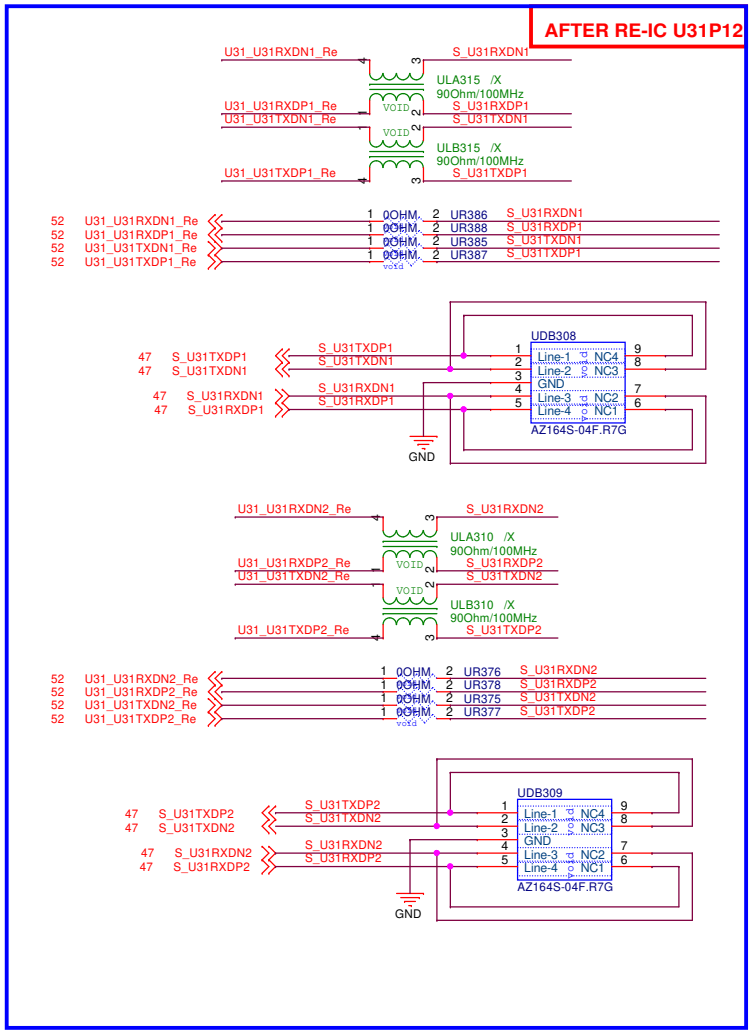
Rext = 1Kohm for Current Limit

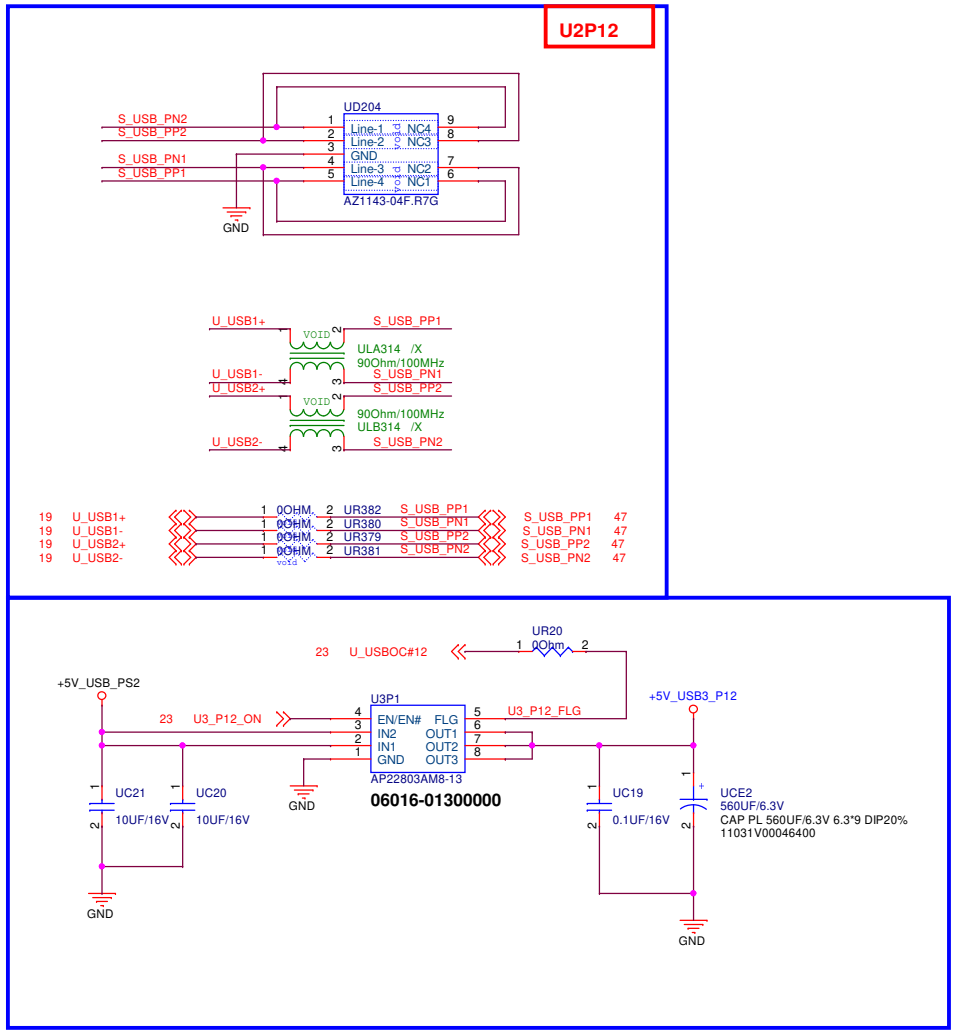


<Variant Name>

ASUS	Title : U31 Port5,6 Redriver IC	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size C	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 54 of 89	

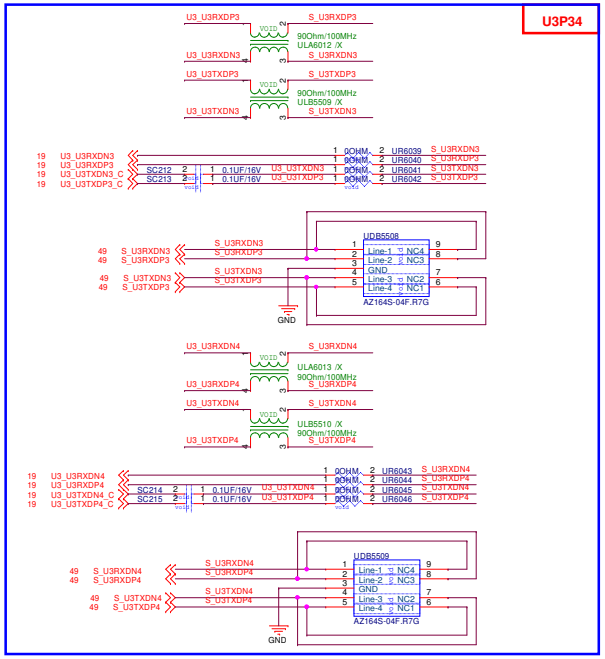

4G LTE PWR_+3VSUS_LTE
2.75A(For mPCI-E 1.2 SPEC)
Imax=2.75A
4G LTE PWR_+1.5V_LTE
0.5A(For mPCI-E 1.2 SPEC)
Imax=0.5A
Place Caps near connector
Screw Hole & NUT Hole
BOM P/N: 13G020369000
NUT_4GLTE1
13GMBKXC040B-1
13G020369000
4G LTE LED
Pull-High/Low Pin
MINI Card-4G LTE
MINI_CARD1
12G03013052N
R1.0-2-(5)/1-03
Micro-SIM Card
SIM1
12023-00026600
From PCH PLTRST# pin
Support USIM/SIM Card +1.8V or +3V PWR
WWAN Disable
Disable wireless communications
+1.8V Pull-High Control
Pull-up by default Active low
Micro-SIM Card - Reserved Pin for Signal Quality
Micro-SIM Card - ESD Protection
+1.5V_LTE PWR Controller
0.5A(For mPCI-E 1.2 SPEC)
Imax=0.5A
Imax=0.8A
FB=0.8V
4G LTE CLKREQ#
4G LTE_Wake# Control
Title : 4G LTE+Micro SIM
ASUSTek COMPUTER INC.
Engineer: <OrgAddr1>
Size Custom
Project Name ATX-Q670E
Rev 1.10
Date: Friday, May 20, 2022
Sheet 55 of 67

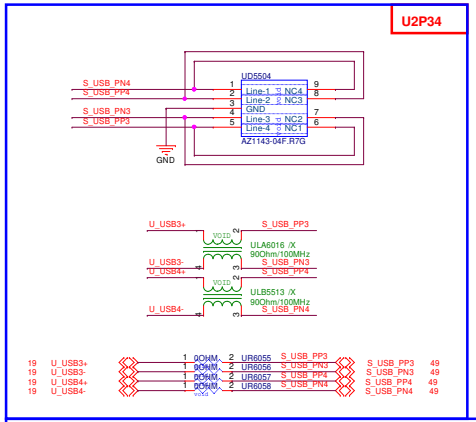


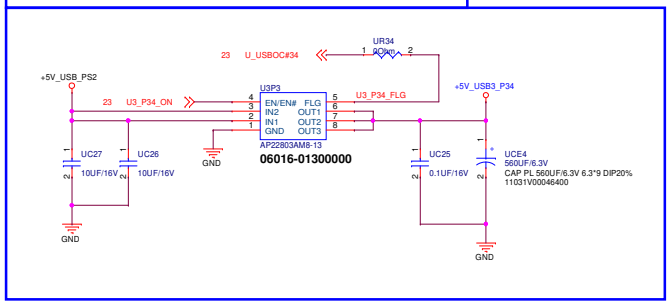


<Variant Name>

ASUS	Title : U31_Port1,2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 56 of 90	

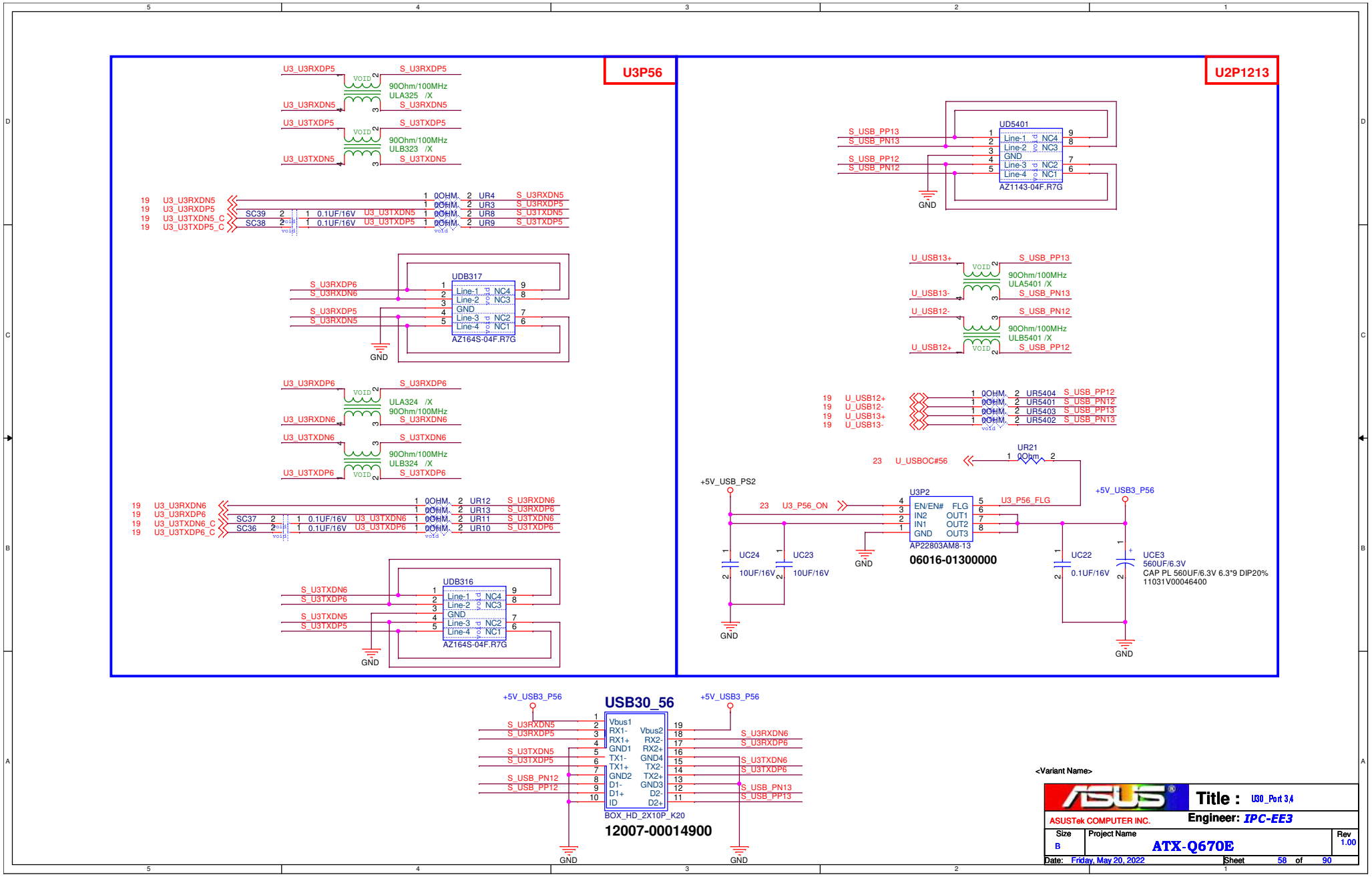


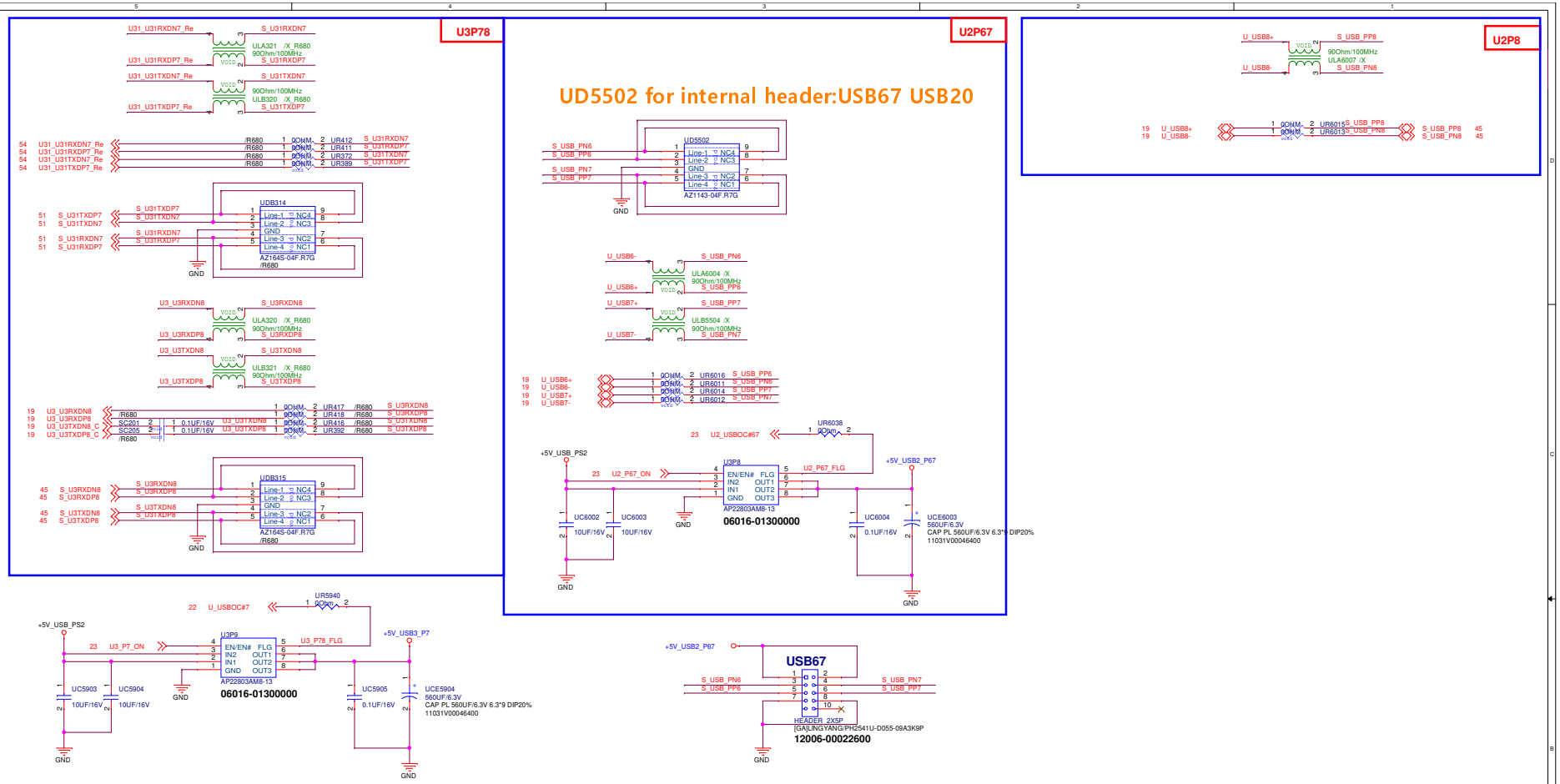


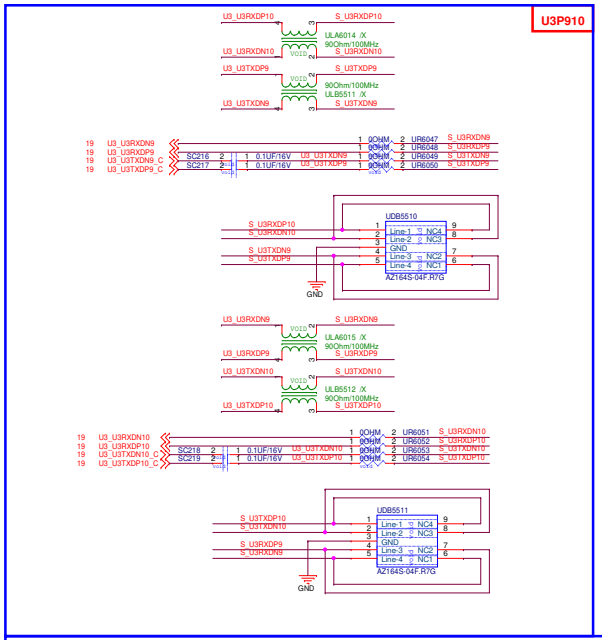


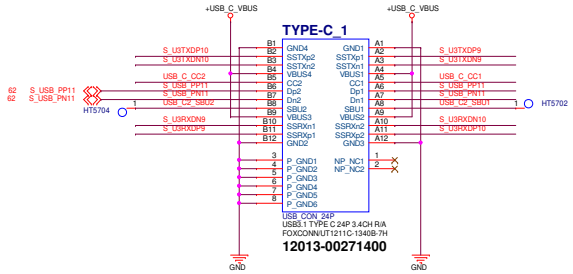
<Variant Name>

ASUSTeK COMPUTER INC.	Title : USB31 Port 5,6	
	Engineer: IPC-EE3	
Size C	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 57 of 90	

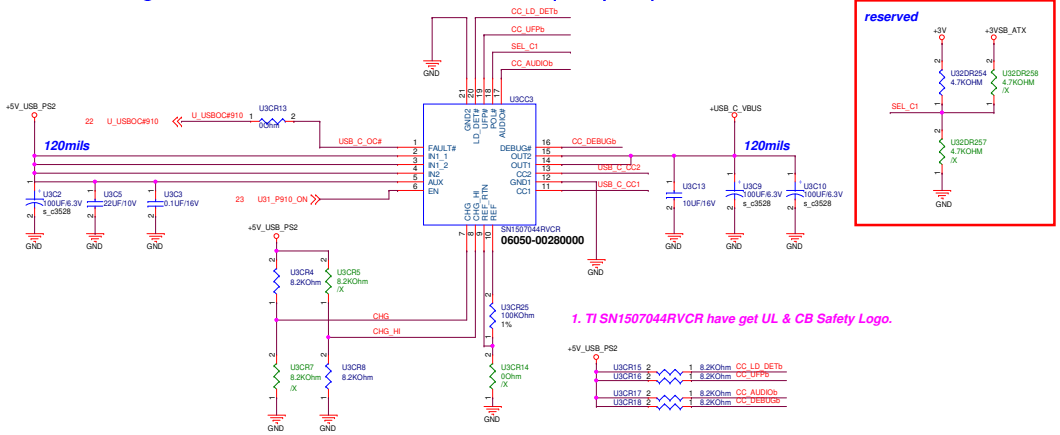

U3P56
U3_U3RXDP5
S_U3RXDP5
VOID
90Ohm/100MHz
ULA325 /X
U3_U3RXDN5
S_U3RXDN5
U3_U3TXDP5
S_U3TXDP5
90Ohm/100MHz
ULB323 /X
U3_U3TXDN5
S_U3TXDN5
19 U3_U3RXDN5
19 U3_U3RXDP5
19 U3_U3TXDN5_C
19 U3_U3TXDP5_C
SC39 0.1UF/16V U3_U3TXDN5
SC38 0.1UF/16V U3_U3TXDP5
0OHM. UR4 S_U3RXDN5
0OHM. UR3 S_U3RXDP5
0OHM. UR8 S_U3TXDN5
0OHM. UR9 S_U3TXDP5
UDB317
S_U3RXDP6
S_U3RXDN6
S_U3RXDP5
S_U3RXDN5
Line-1 NC4
Line-2 NC3
GND
Line-3 NC2
Line-4 NC1
AZ164S-04F.R7G
GND
U3_U3RXDP6
S_U3RXDP6
ULA324 /X
90Ohm/100MHz
U3_U3RXDN6
S_U3RXDN6
U3_U3TXDN6
S_U3TXDN6
90Ohm/100MHz
ULB324 /X
U3_U3TXDP6
S_U3TXDP6
19 U3_U3RXDN6
19 U3_U3RXDP6
19 U3_U3TXDN6_C
19 U3_U3TXDP6_C
SC37 0.1UF/16V U3_U3TXDN6
SC36 0.1UF/16V U3_U3TXDP6
0OHM. UR12 S_U3RXDN6
0OHM. UR13 S_U3RXDP6
0OHM. UR11 S_U3TXDN6
0OHM. UR10 S_U3TXDP6
UDB316
S_U3TXDN6
S_U3TXDP6
S_U3TXDN5
S_U3TXDP5
Line-1 NC4
Line-2 NC3
GND
Line-3 NC2
Line-4 NC1
AZ164S-04F.R7G
GND
U2P1213
UD5401
S_USB_PP13
S_USB_PN13
S_USB_PP12
S_USB_PN12
Line-1 NC4
Line-2 NC3
GND
Line-3 NC2
Line-4 NC1
AZ1143-04F.R7G
GND
U_USB13+
S_USB_PP13
VOID
90Ohm/100MHz
ULA5401 /X
U_USB13-
S_USB_PN13
U_USB12-
S_USB_PN12
90Ohm/100MHz
ULB5401 /X
U_USB12+
S_USB_PP12
19 U_USB12+
19 U_USB12-
19 U_USB13+
19 U_USB13-
0OHM. UR5404 S_USB_PP12
0OHM. UR5401 S_USB_PN12
0OHM. UR5403 S_USB_PP13
0OHM. UR5402 S_USB_PN13
UR21
0Ohm
23 U_USBOC#56
+5V_USB_PS2
23 U3_P56_ON
U3P2
EN/EN# FLG
IN2 OUT1
IN1 OUT2
GND OUT3
AP22803AM8-13
06016-01300000
U3_P56_FLG
+5V_USB3_P56
UC24 10UF/16V
UC23 10UF/16V
GND
UC22 0.1UF/16V
UCE3
560UF/6.3V
CAP PL 560UF/6.3V 6.3*9 DIP20%
11031V00046400
GND
USB30_56
+5V_USB3_P56
S_U3RXDN5
S_U3RXDP5
S_U3TXDN5
S_U3TXDP5
S_USB_PN12
S_USB_PP12
Vbus1
RX1- Vbus2
RX1+ RX2-
GND1 RX2+
TX1- GND4
TX1+ TX2-
GND2 TX2+
D1- GND3
D1+ D2-
ID D2+
BOX_HD_2X10P_K20
12007-00014900
S_U3RXDN6
S_U3RXDP6
S_U3TXDN6
S_U3TXDP6
S_USB_PN13
S_USB_PP13
GND
GND
<Variant Name>
ASUSTek COMPUTER INC.
Title : USB_Port 3,4
Engineer: IPC-EE3
Size B
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 58 of 90


U3P78
U2P67
U2P8
UD5502 for internal header:USB67 USB20
U31_U31RXDN7_Re
S_U31RXDN7
ULA321 /X R680
90Ohm/100MHz
U31_U31RXDP7_Re
S_U31RXDP7
U31_U31TXDN7_Re
S_U31TXDN7
ULB320 /X R680
U31_U31TXDP7_Re
S_U31TXDP7
UDB314
AZ164S-04F.R7G
/R680
GND
U3_U3RXDN8
S_U3RXDN8
ULA320 /X R680
U3_U3RXDP8
S_U3RXDP8
U3_U3TXDN8
S_U3TXDN8
ULB321 /X R680
U3_U3TXDP8
S_U3TXDP8
UDB315
UD5502
AZ1143-04F.R7G
S_USB_PN6
S_USB_PP6
S_USB_PN7
S_USB_PP7
U_USB6-
U_USB6+
U_USB7+
U_USB7-
ULA6004 /X
ULB5504 /X
U_USB8+
U_USB8-
S_USB_PP8
S_USB_PN8
ULA6007 /X
+5V_USB_PS2
U2_P67_ON
U2_P67_FLG
+5V_USB2_P67
U2_USBOC#67
UR6038
U3P8
AP22803AM8-13
06016-01300000
UC6002
UC6003
UC6004
UC6003
560UF/6.3V
CAP PL 560UF/6.3V 6.3*9 DIP20%
11031V00046400
U_USBOC#7
UR5940
U3P9
U3_P7_ON
U3_P78_FLG
+5V_USB3_P7
UC5903
UC5904
UC5905
UCE5904
USB67
HEADER_2X5P
[GA]LINGYANG/PH2541U-D055-09A3K9P
12006-00022600
Title : USB31 Port 7
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name ATX-Q670E
Rev 1.00
Date: Friday, May 20, 2022
Sheet 59 of 90





TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A



1. TI SN1507044RVCR have get UL & CB Safety Logo.

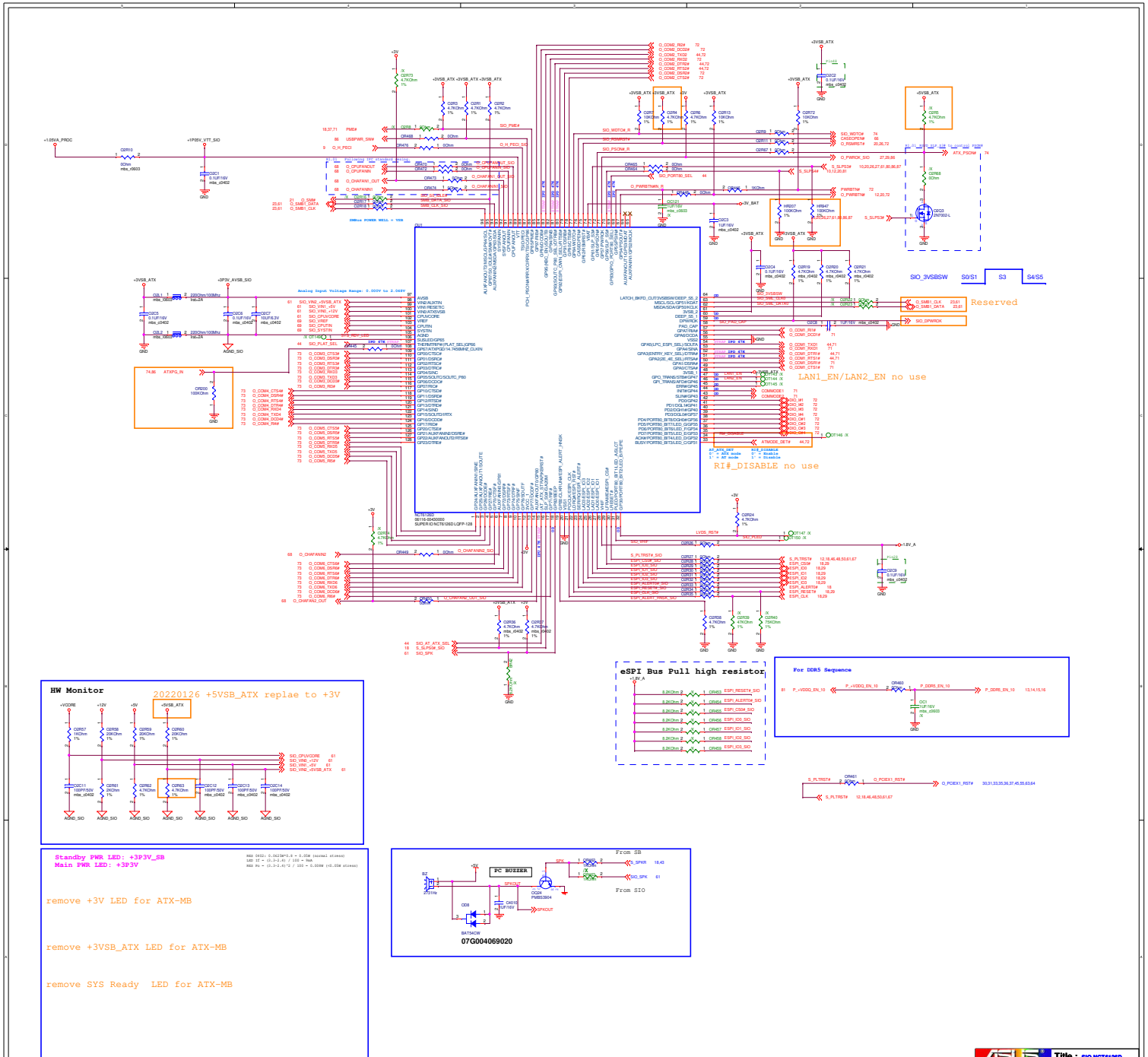
Set CC
I limit = 1.7A

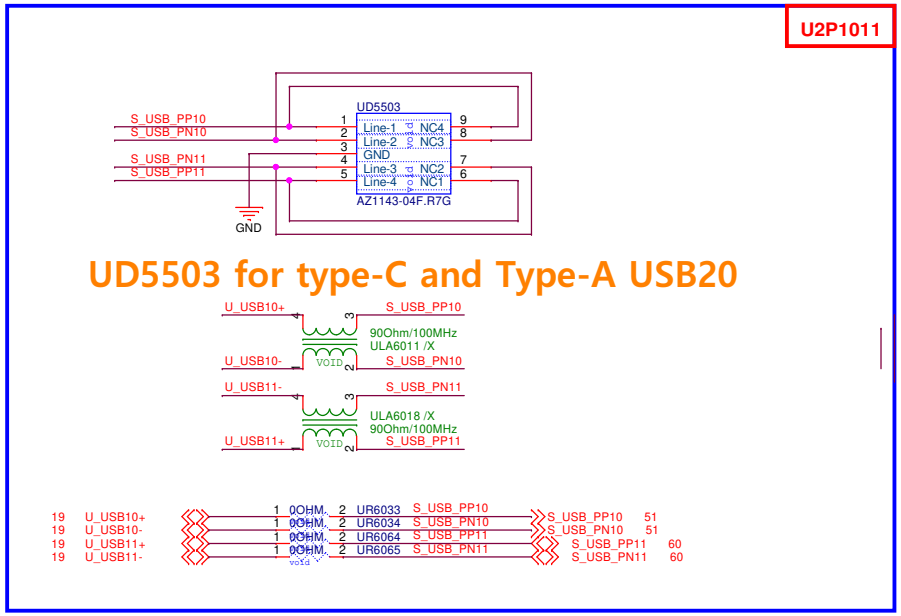
Table 3. USB Type-C Current Advertisement

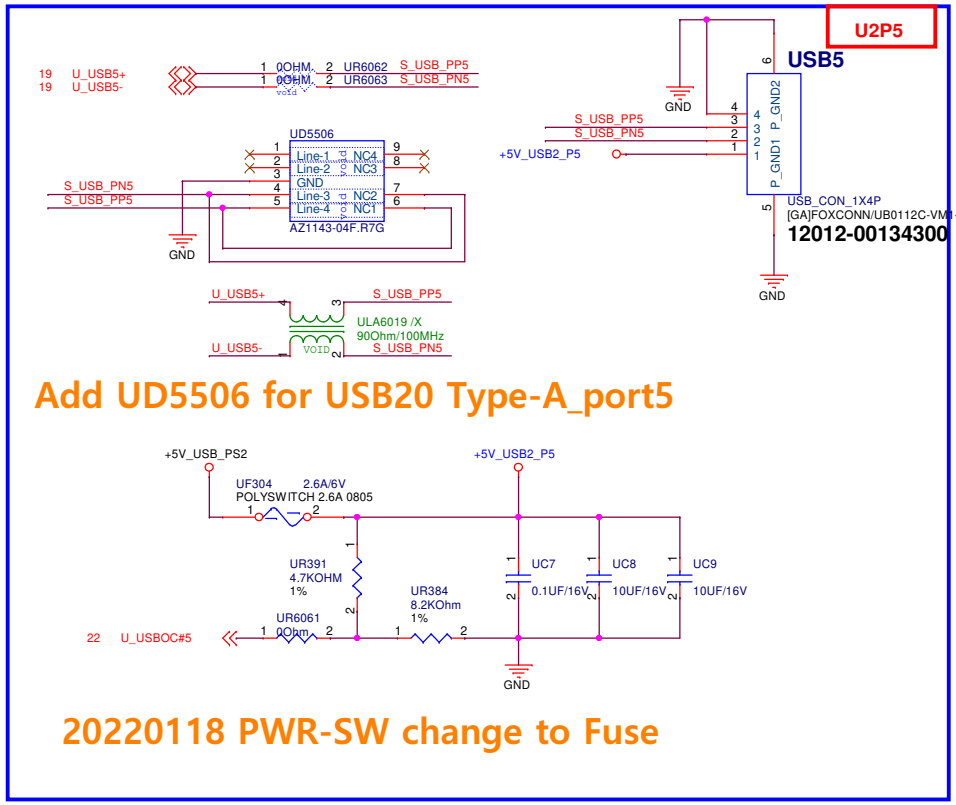
CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

<Variant Name>

ASUSTeK COMPUTER INC.
Title : USB11 Port 1
Engineer: IPC-EE3
Size: Custom | Project Name: ATX-Q670E | Rev: 1.00
Date: Friday, May 20, 2022 | Sheet 60 of 90

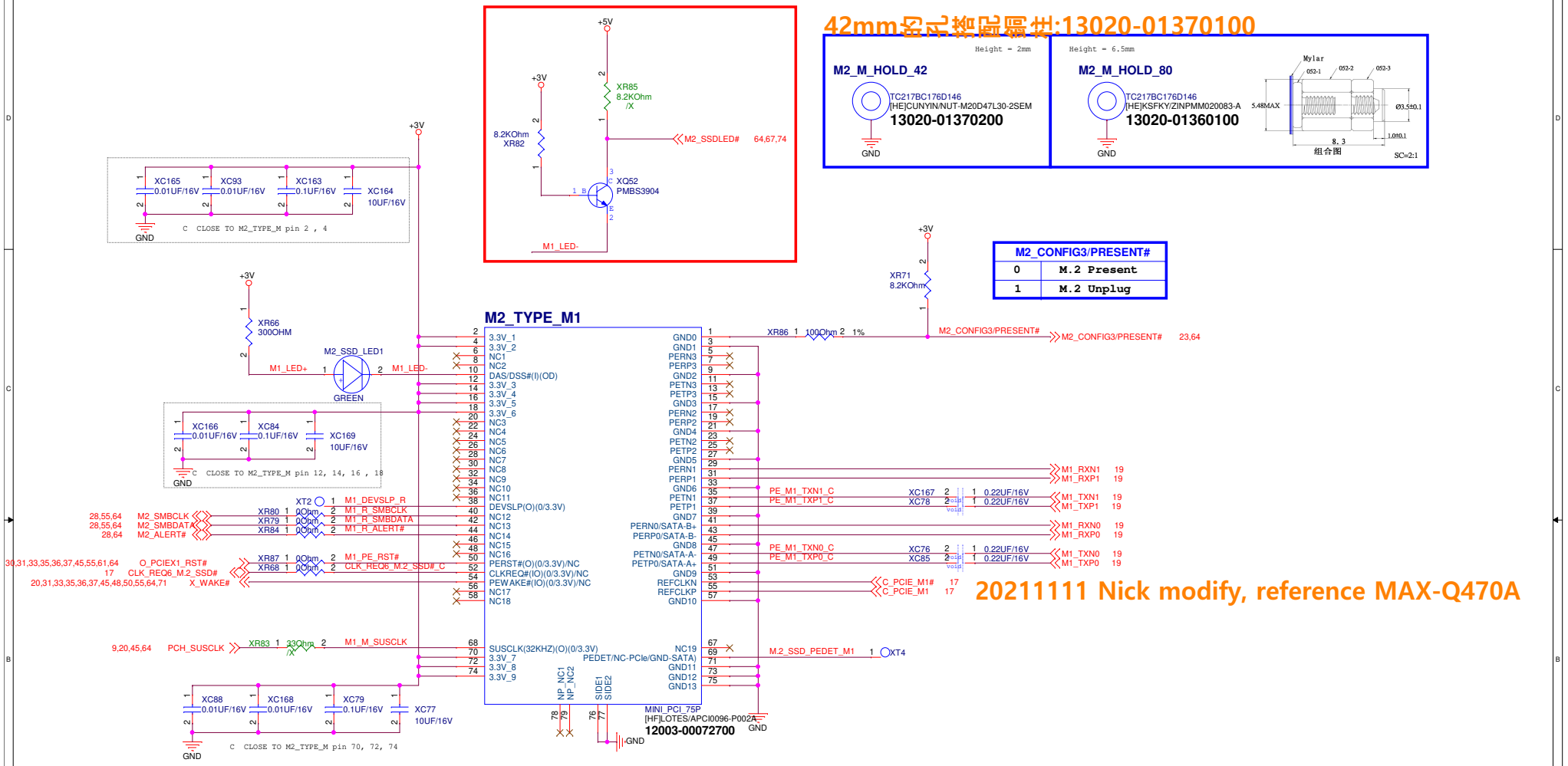

SIO_3VSBSW
S0/S1
S3
S4/S5
Reserved
LAN1_EN/LAN2_EN no use
RI#_DISABLE no use
HW Monitor
20220126 +5VSB_ATX replae to +3V
eSPI Bus Pull high resistor
For DDR5 Sequence
PC BUZZER
From SB
From SIO
07G004069020
Standby PWR LED: +3P3V_SB
Main PWR LED: +3P3V
remove +3V LED for ATX-MB
remove +3VSB_ATX LED for ATX-MB
remove SYS Ready LED for ATX-MB
Title : SIO NCT6126D
Engineer: IPC-E23
ASUSTeK COMPUTER INC.
Size
Project Name
Rev
Custom
ATX-Q670E
R1.00
Date: Friday, May 20, 2022
Sheet 61 of 99





<Variant Name>

ASUSTek COMPUTER INC.	Title :	USB2 Port X 1 Internal
	Engineer:	IPC-EE3
Size B	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 62 of 90	



M2_CONFIG3/PRESENT#	
0	M.2 Present
1	M.2 Unplug

<Variant Name>

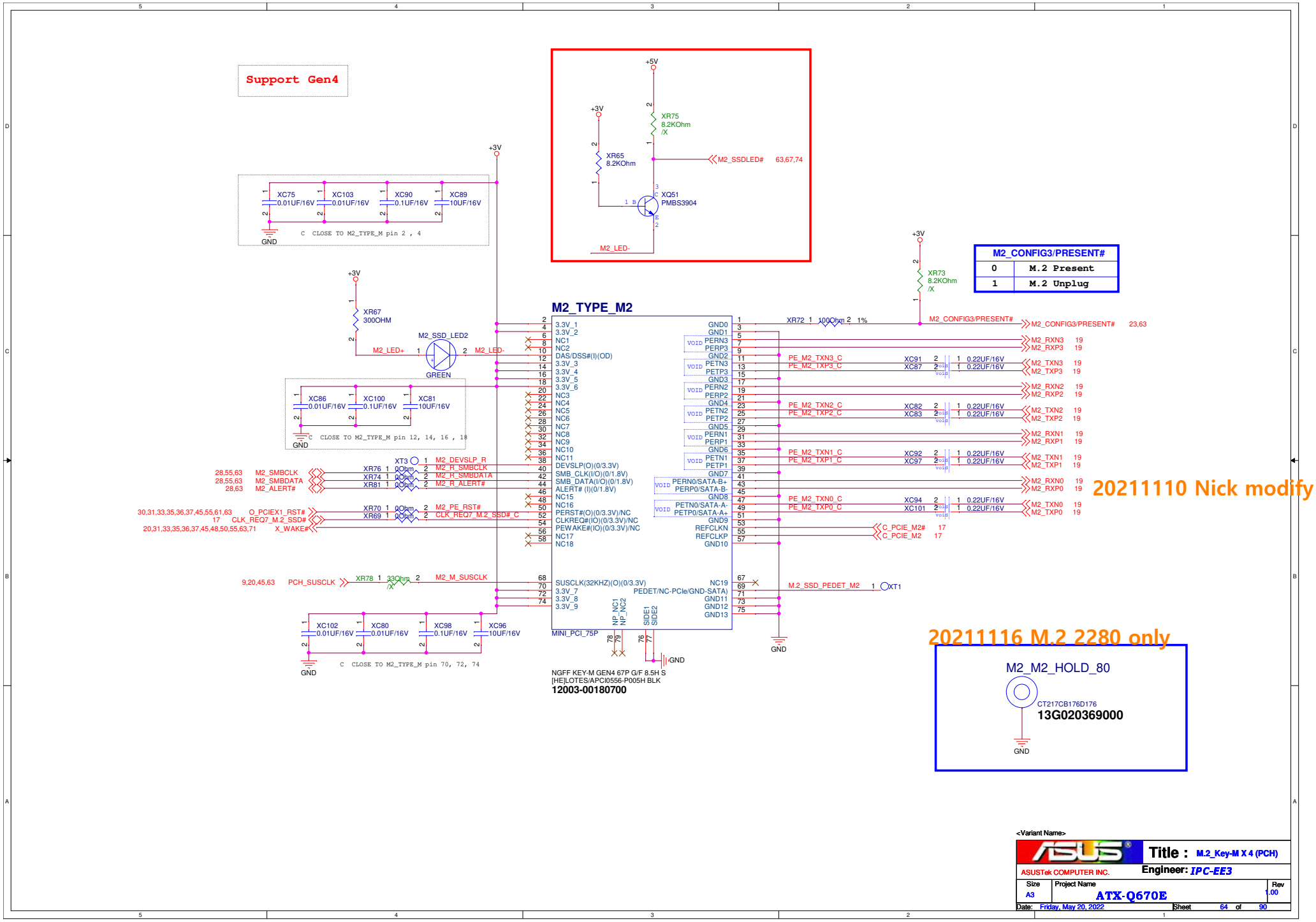
Title : M.2_Key-M X 2 (PCH)

ASUSTek COMPUTER INC.

Engineer: IPC-EE3

Size	Project Name	Rev
A3	ATX-Q670E	1.00

Date: Friday, May 20, 2022 Sheet 63 of 86



<Variant Name>

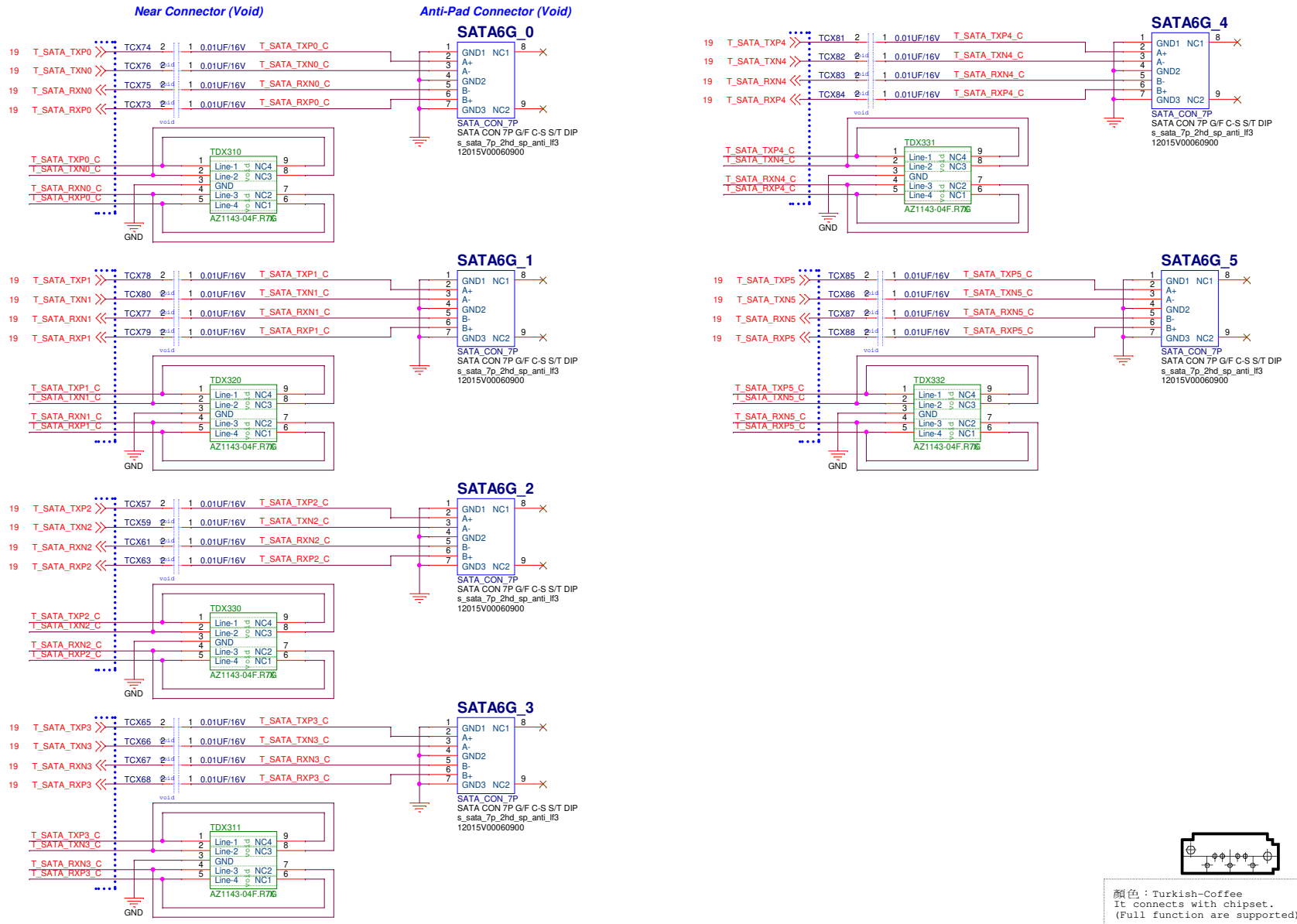
Title : M.2_Key-M X 4 (PCH)

ASUSTek COMPUTER INC.

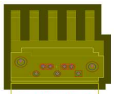
Engineer: IPC-EE3

Size	Project Name	Rev
A3	ATX-Q670E	1.00

Date: Friday, May 20, 2022 Sheet 64 of 90



顏色：Turkish-Coffee
It connects with chipset.
(Full function are supported)



Height Limited
355 mils
for SATA cable routing

New Color		
SATA 6G:	12015V00060900	Cornsilk
SATA 3G:	12015V00060800	Turkish-Coffee

Old Color		
SATA 6G:	12V702200A00	LIGHT GRAY
SATA 3G:	12V702200L00	LIGHT BLUE

<Variant Name>

ASUSTek COMPUTER INC.

Title : SATA6G_0-3 (CHIPSET)

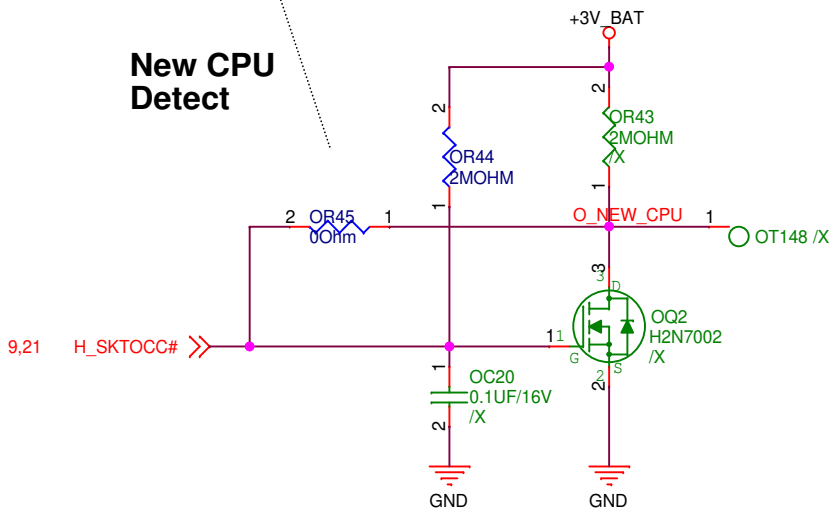
Engineer: IPC-EE3

Size	Project Name	Rev
A3	ATX-Q670E	1.00

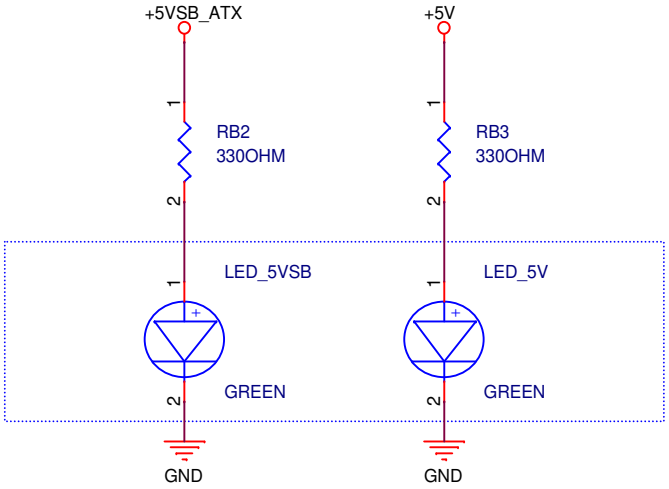
Date: Friday, May 20, 2022 Sheet 65 of 90

if there is pull-high@CPU side,remove OR31

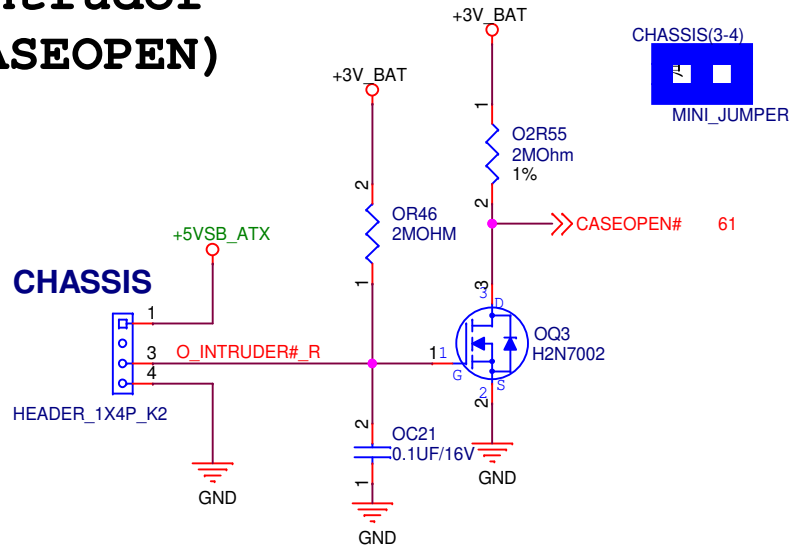
New CPU Detect



POWER_PWR



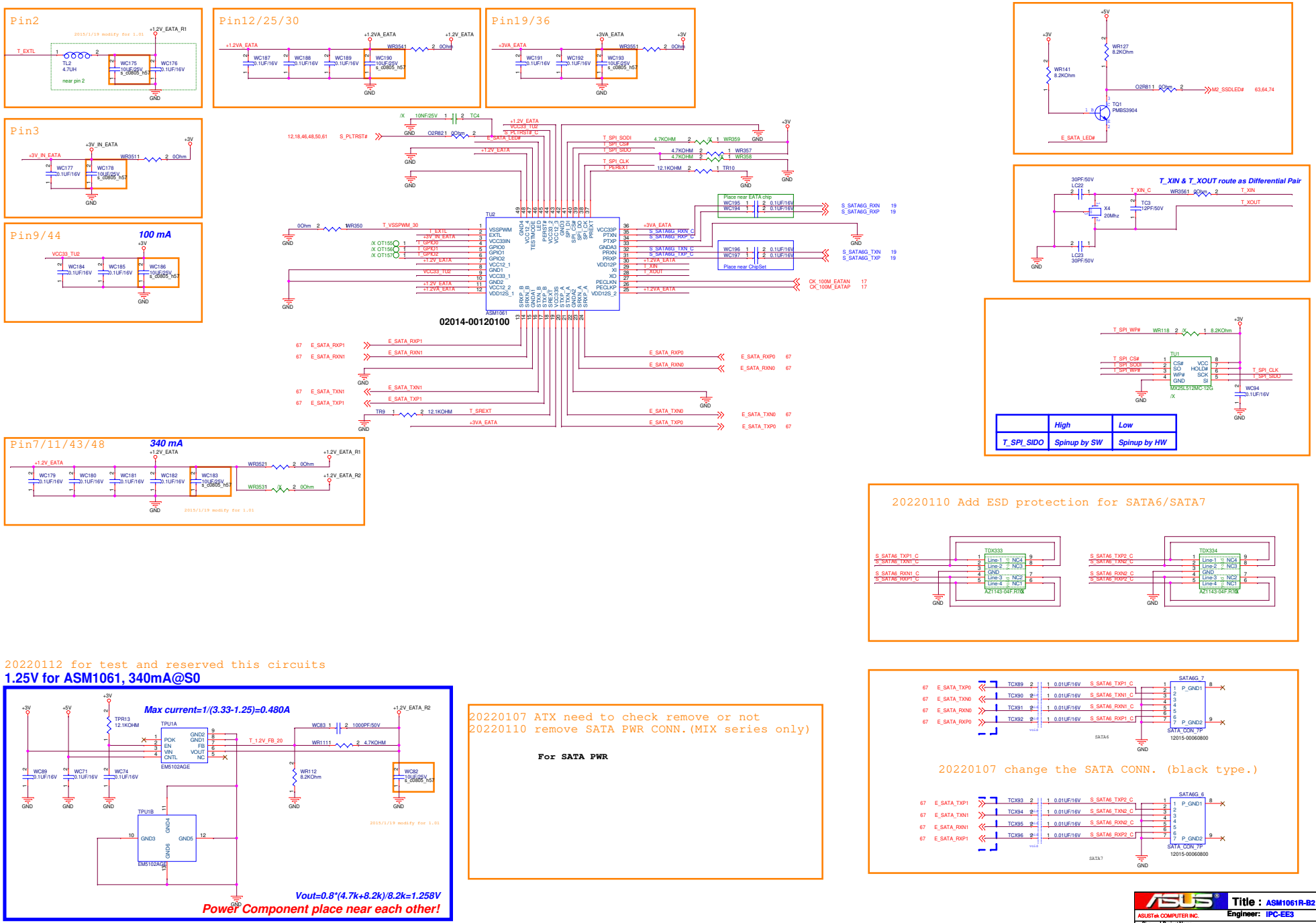
Intrudor (CASEOPEN)



To SIO

<Variant Name>

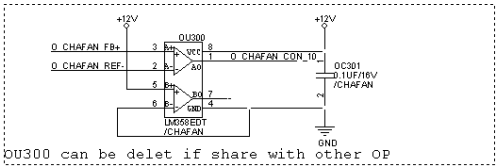
ASUSTek COMPUTER INC.	Title : CPU detect/PWR LED		
	Engineer: IPC-EE3		
Size A	Project Name ATX-Q670E		Rev 1.00
Date: Friday, May 20, 2022	Sheet 66 of 90		


Pin2
Pin12/25/30
Pin19/36
Pin3
Pin9/44
100 mA
Pin7/11/43/48
340 mA
T_XIN & T_XOUT route as Differential Pair
TU2
ASM1061
02014-00120100
TU1
MX25L512MC-12G
High
Low
T_SPI_SIDO
Spinup by SW
Spinup by HW
20220110 Add ESD protection for SATA6/SATA7
TDX333
TDX334
AZ1143-04F-R7G
20220112 for test and reserved this circuits
1.25V for ASM1061, 340mA@S0
Max current=1/(3.33-1.25)=0.480A
TPU1A
EM5102AGE
TPU1B
Vout=0.8*(4.7k+8.2k)/8.2k=1.258V
Power Component place near each other!
20220107 ATX need to check remove or not
20220110 remove SATA PWR CONN.(MIX series only)
For SATA PWR
SATA6G_7
SATA6G_6
SATA_CON_7P
12015-00060800
20220107 change the SATA CONN. (black type.)
ASUSTek COMPUTER INC.
Title : ASM1061R-B2
Engineer: IPC-EE3
Size A2
Project Name ATX-Q670E
Rev R1.00
Date: Friday, May 20, 2022
Sheet 67 of 90

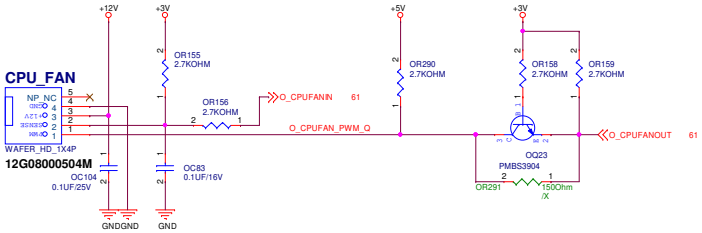
FAN CONTROL

PWM FAN CONTROL(New)

Pin Number	Signal
1	Control
2	Sense
3	+12V
4	GND

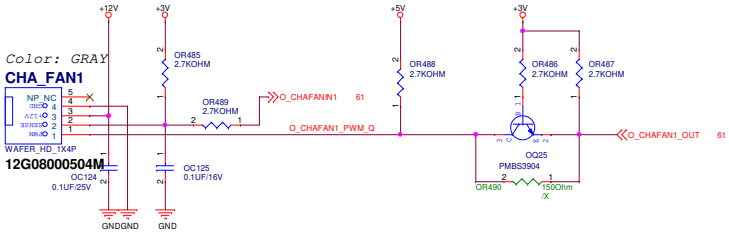


CHASSIS Q-FAN

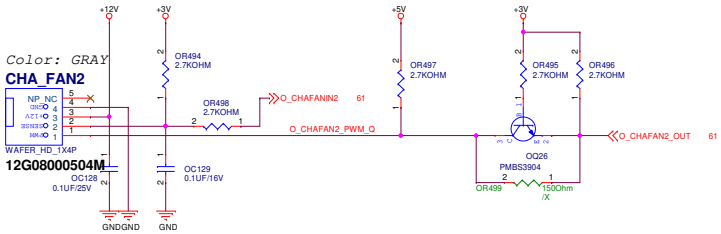


20220112 remove Q Chassis Q-FAN

20220112 CHA_FAN1 change to PWM FAN (mapping S-IO SYSFAN)

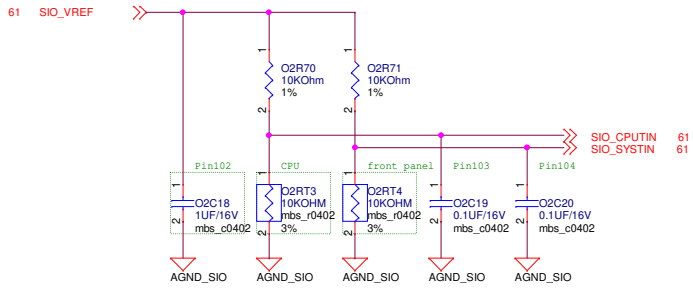


20220112 CHA_FAN2 change to PWM FAN (mapping S-IO AUXFAN0)



<Variant Name>

ASUSTeK COMPUTER INC.	Title : CPU/SYS/PWR_FAN	
	Engineer: IPC-EE3	
Size C	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 68 of 90	



Thermal sensor placement

O2C18: Place near S-IO pin102

O2RT3: Place near CPU

O2RT4: Place near front panel

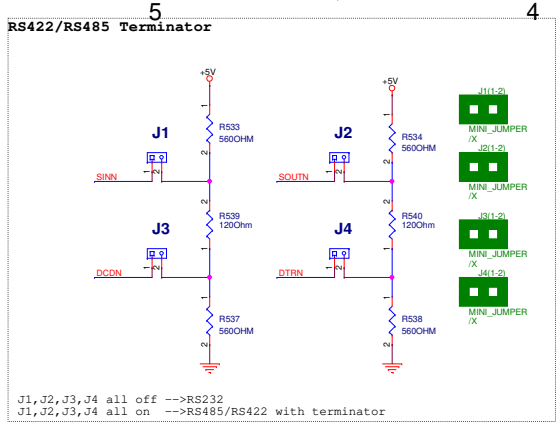
O2C19: Place near S-IO pin103

O2C20: Place near S-IO pin104

ASUSTek COMPUTER INC.	Title : Thermal Sensor		
	Engineer: IPC-EE3		
Size A3	Project Name ATX-Q670E		Rev 1.00
Date: Friday, May 20, 2022	Sheet 69 of 90		

<Variant Name>

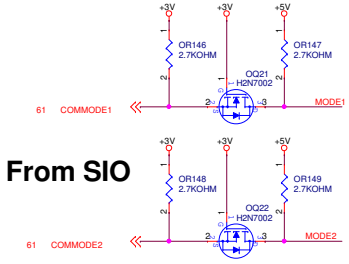
ASUSTek COMPUTER INC.	Title : F81216 COM	
	Engineer: IPC-EE3	
Size B	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 70 of 90	



Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ.
As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.

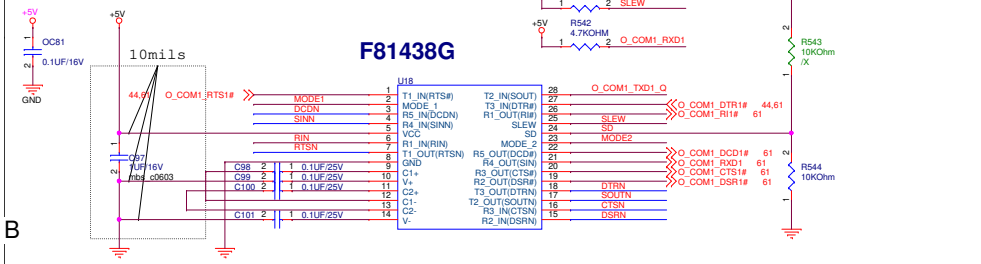


(VDD = +5.0V ± 5%)

Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01.		2	30	mA
Supply Current (RS-485)	No Load, MODE = 10, 11.		2		mA
Supply Current (RS-422)	MODE = 00.		2		mA
Operating Temperature *	Symbol: T	-40		85	◦ C

(VDD = +5.0V ± 5%)

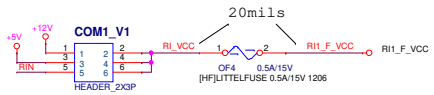
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V_{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	μA	
Driver Input Pull High Current	I_{IT}			±15	μA	

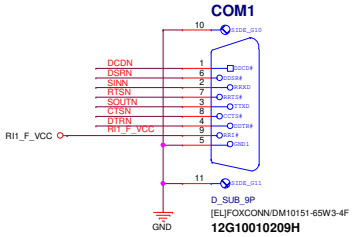


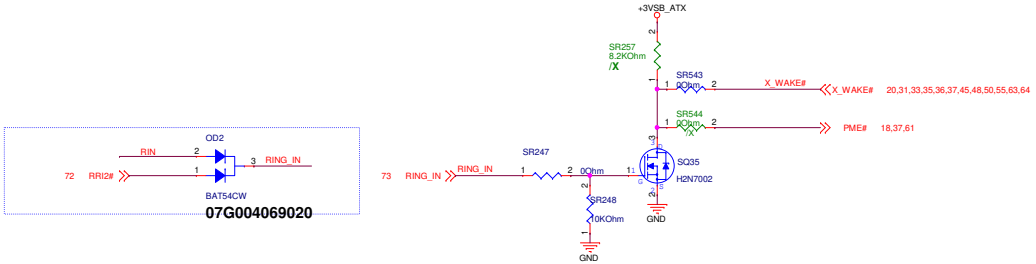
COM1_V1(5-6)	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

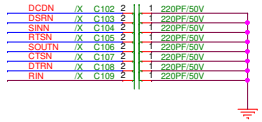
COM1_V1(5-6)

MINI_JUMPER

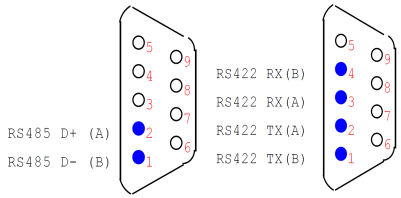




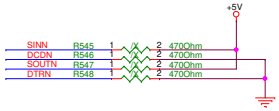




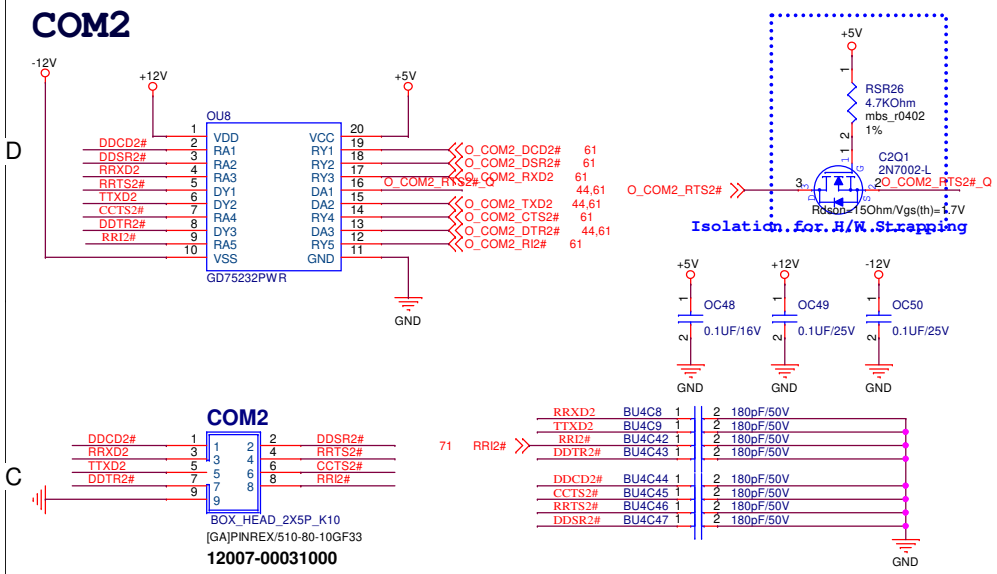
Close to COM port connector



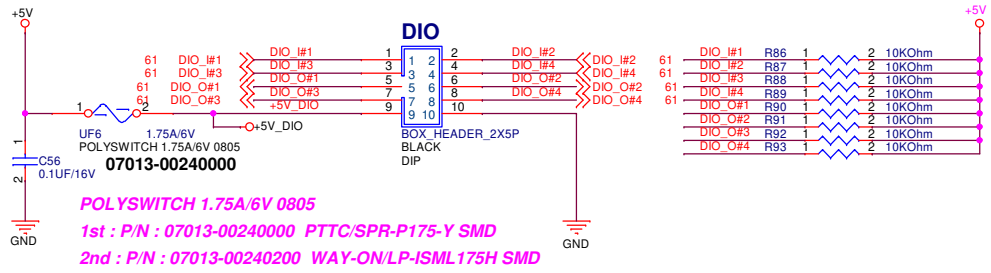
Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps



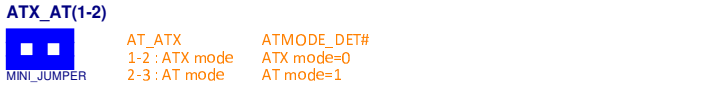
Note:Reserved for FAIL-SAFE

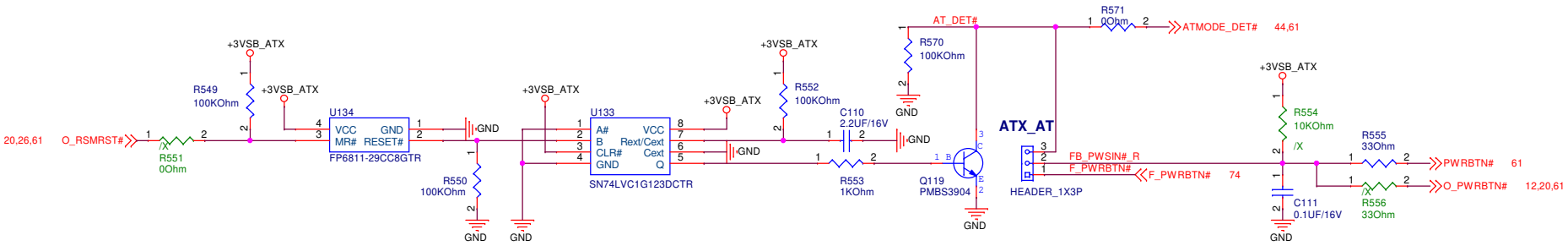


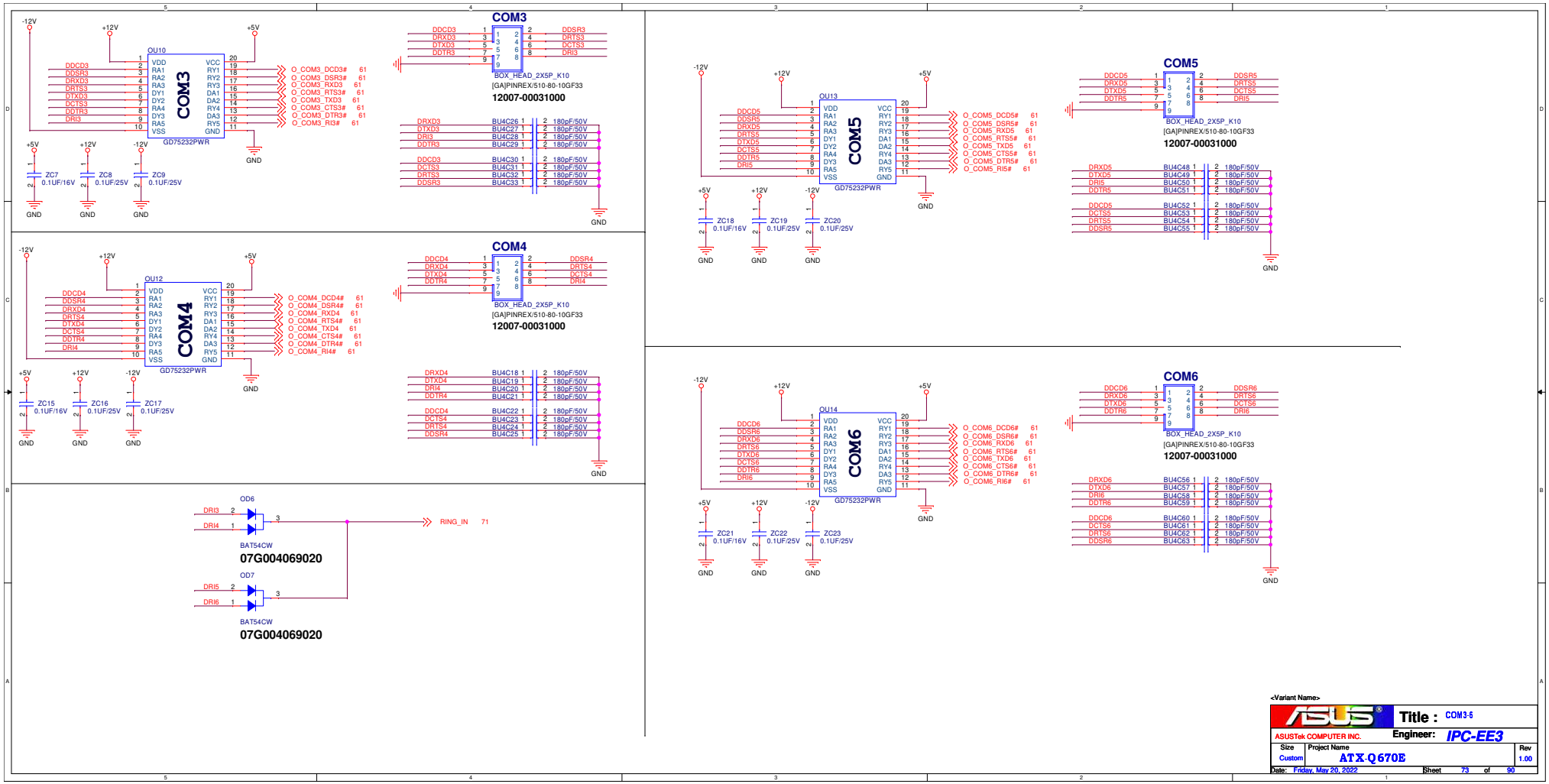
Digitial I/O from SIO



Auto Power Button







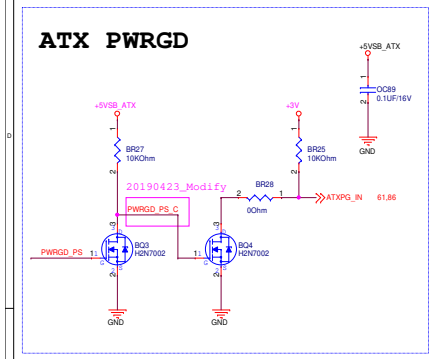
<Variant Name>

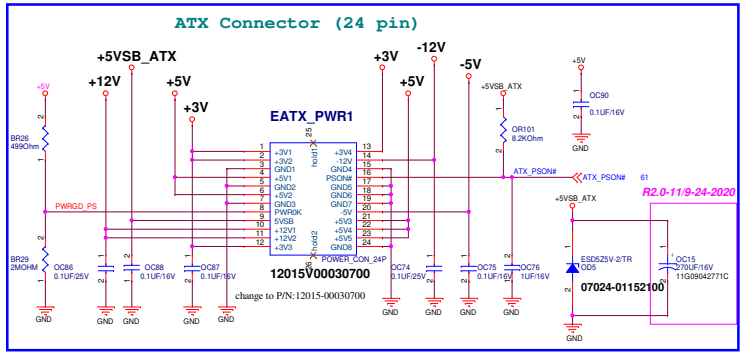
Title : COM3-6

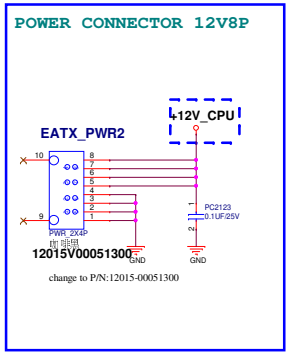
ASUSTek COMPUTER INC. Engineer: IPC-EE3

Size	Project Name	Rev
Custom	ATX-Q670E	1.00

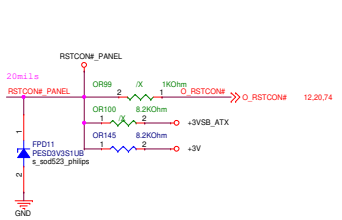
Date: Friday, May 20, 2022 Sheet 73 of 90

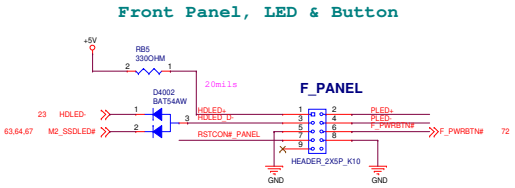


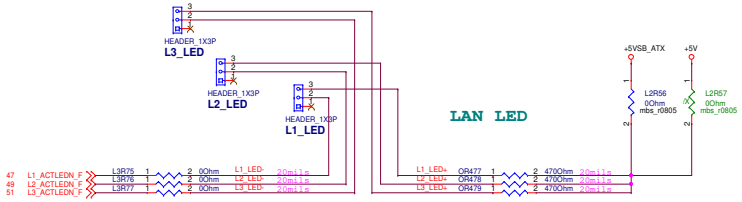




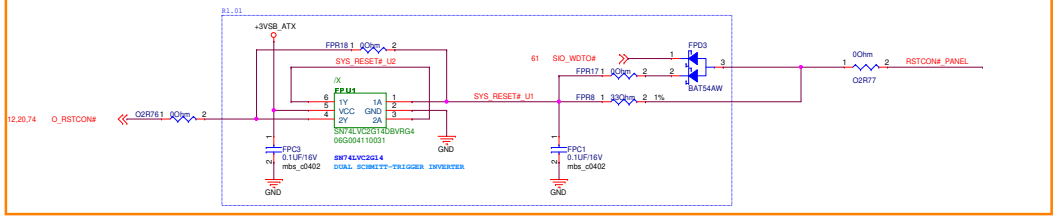
20220106 Change the F_PANEL CONN. to add the LAN LED control signals

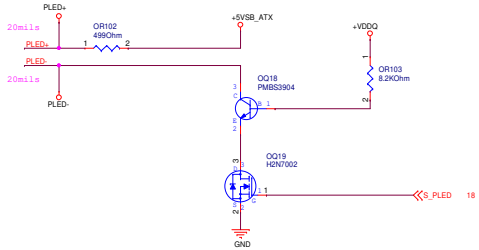


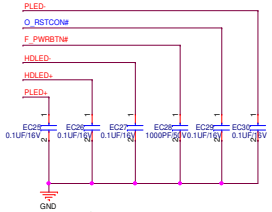




20220104 For de-bounce Circuits

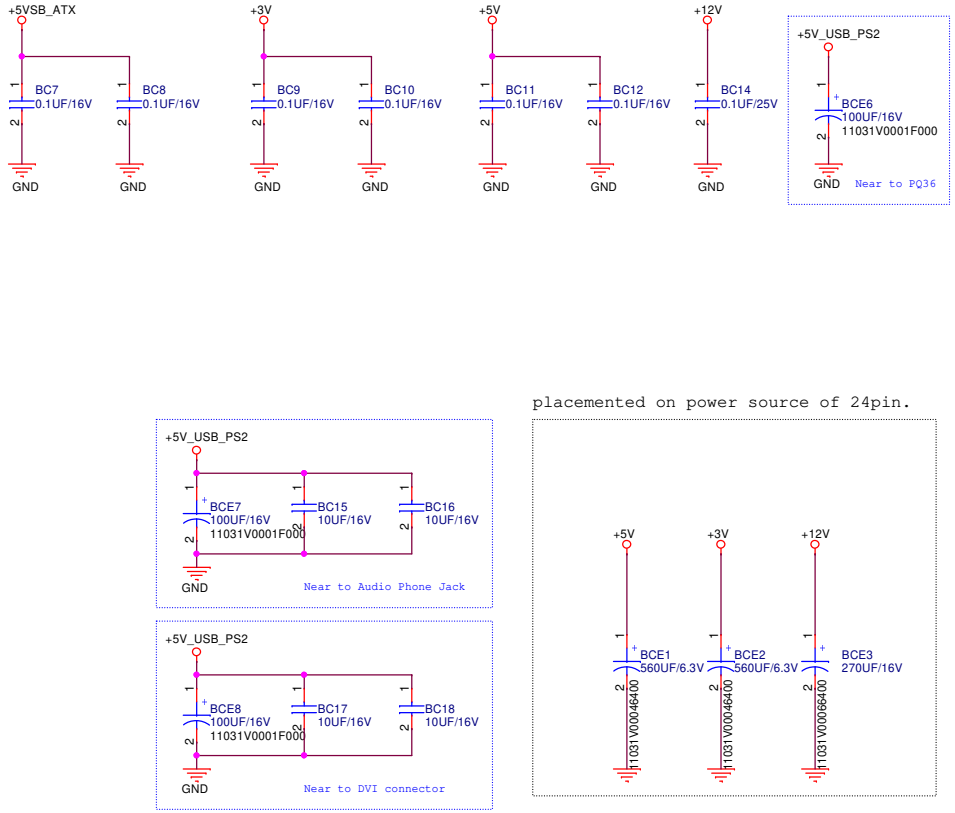






Close to Panel/F_PANEL

Bypass/EMI Capacitor

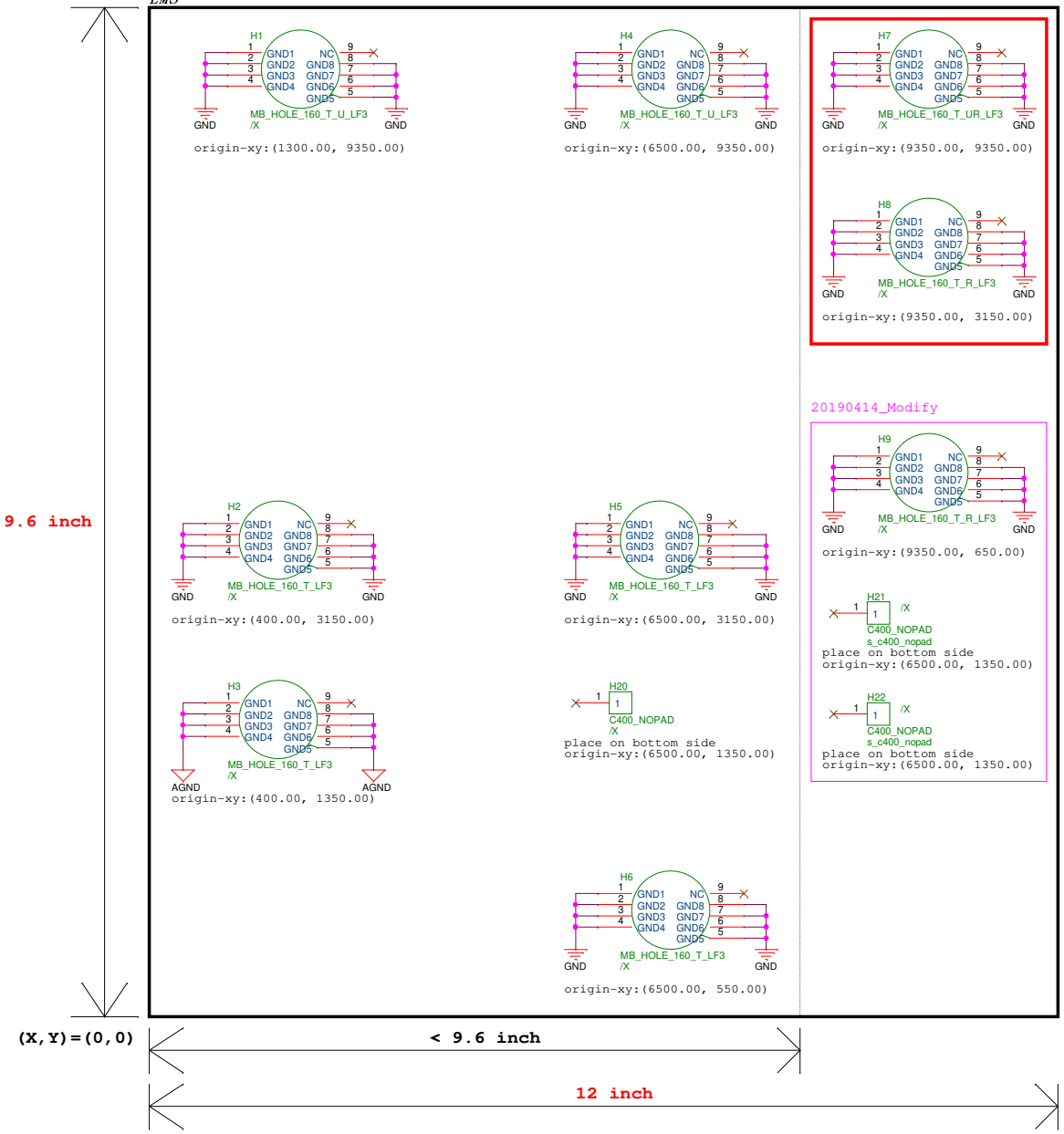


<Variant Name>

ASUS	Title : EMICap	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 75 of 90	

Delete it for EMS

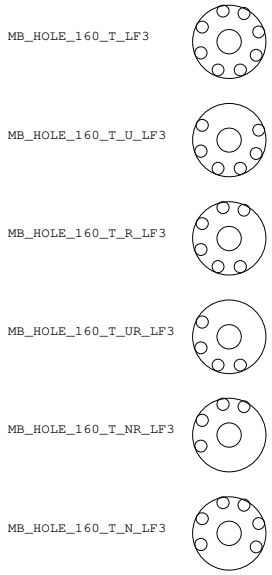
ATX MB Screw Hole



ATX Screw Select

	Standard (9.6 x 9.6)	Scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H20	V	V

MB SCREW FOOTPRINT

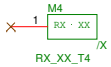


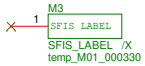
<Variant Name>

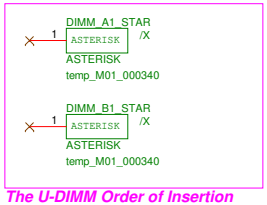
ASUSTek COMPUTER INC.	Title : Screw Hole	
	Engineer: IPC-EE3	
Size A3	Project Name ATX-Q670E	Rev 1.00
Date: Friday, May 20, 2022	Sheet 76 of 90	

Selling Point

20220104 add no pad_TP for layout request

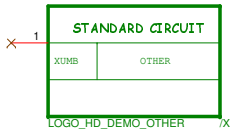


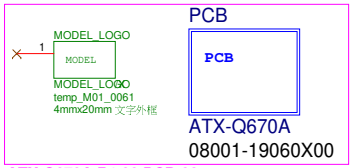




The U-DIMM Order of Insertion

NEED_COMP_SILK





ATX-Q670A R1.00 PCB-08 :

*08001-19060100 ATX-Q670A R1.00//GECS 12*9.6,6L(1)1.6,1080*

*08001-19060200 ATX-Q670A R1.00//TRUSTECH 12*9.6,6L(1)1.6,1080*

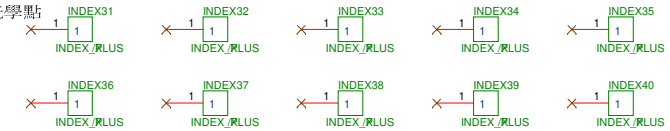
*08001-19060000 ATX-Q670A R1.00//DF 12*9.6,6L(1)1.6,1080*

Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

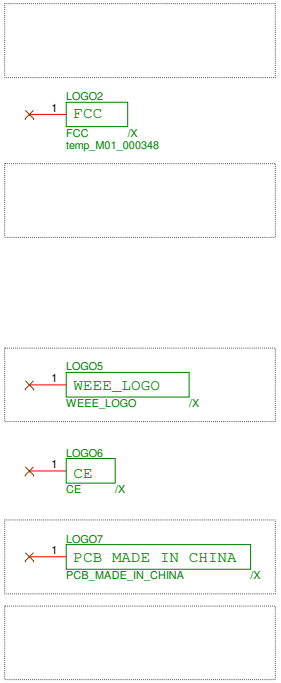
小顆十字光學點



2012/09/11

Logo

common Logo for all projects



<Variant Name>

ASUS	Title :	Selling Point_Logo
ASUSTek COMPUTER INC.	Engineer:	IPC-EE3
Size: A3	Project Name: ATX-Q670E	Rev: 1.00
Date: Friday, May 20, 2022	Sheet 77 of 90	