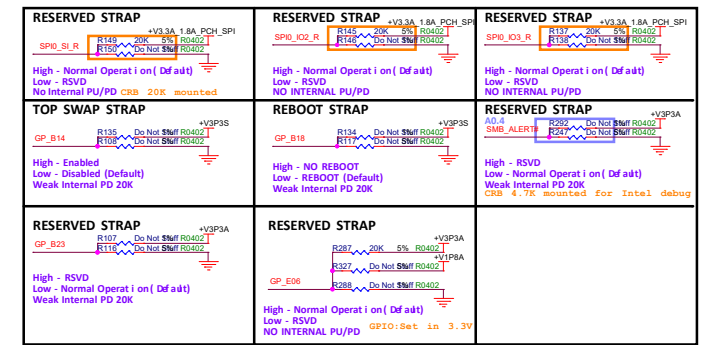
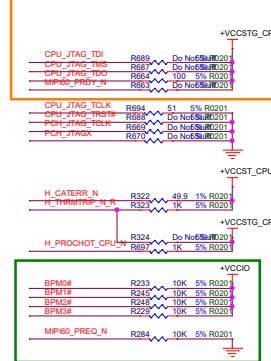
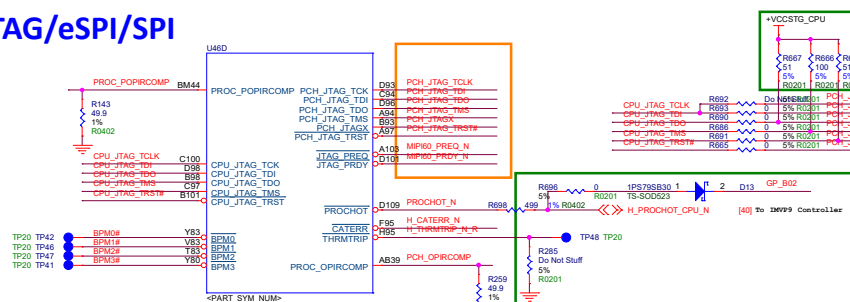
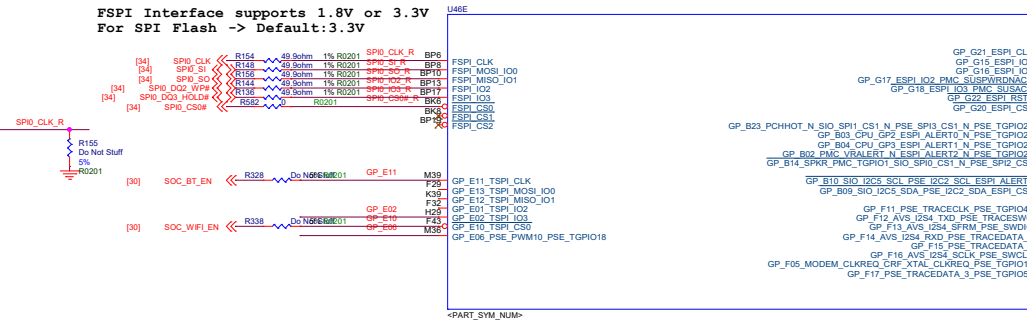


SoC JTAG/eSPI/SPI

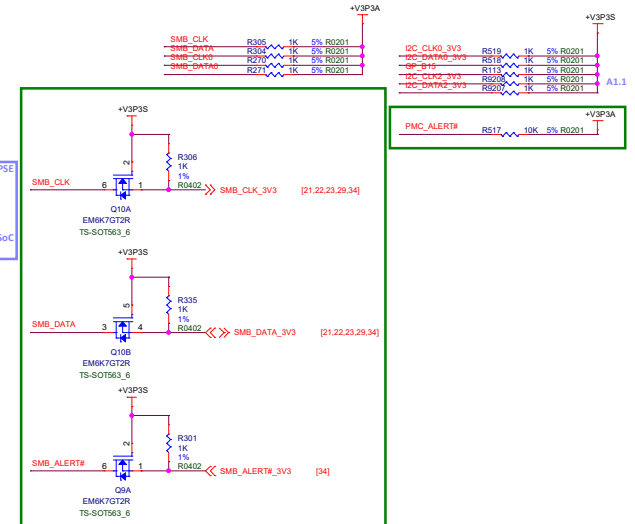
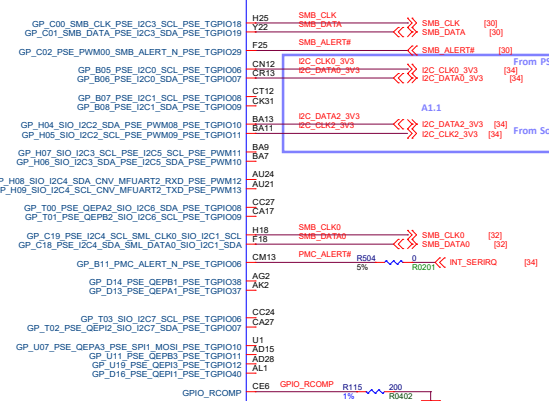
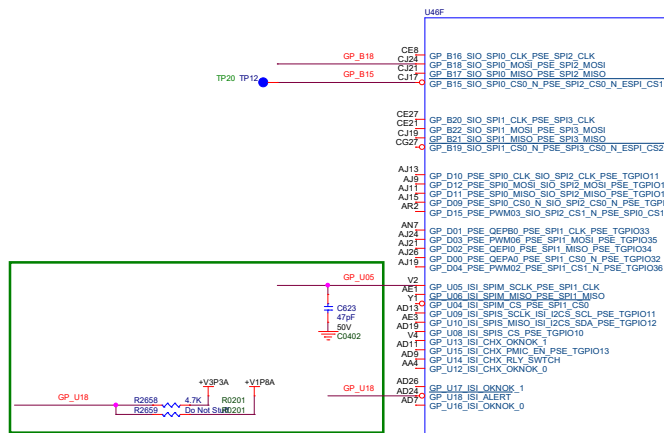
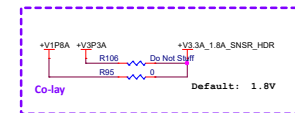
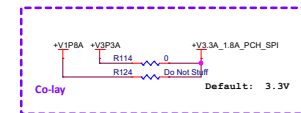
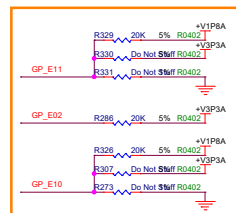
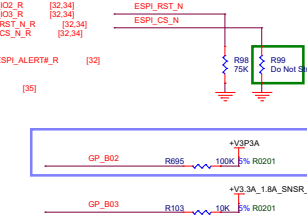
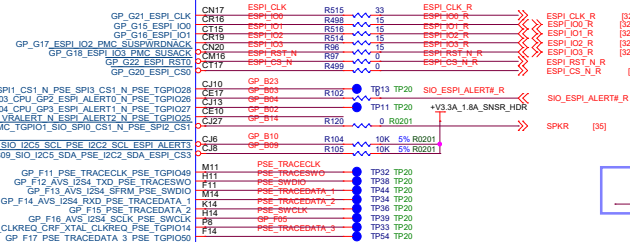


For GP E06:
The pull-up rail will be V1P8A or V3P3A,
depending on what I/O voltage the GPIO is configured to.

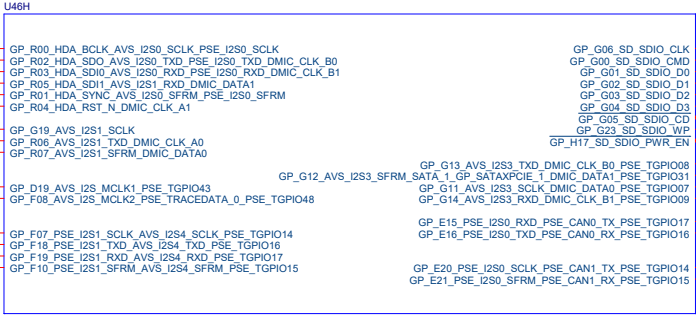
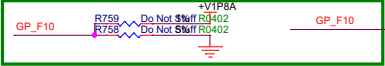
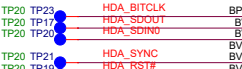
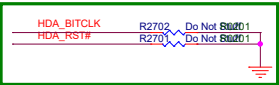
FSPI Interface supports 1.8V or 3.3V
For SPI Flash -> Default:3.3V



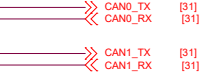
eSPI Interface supports 1.8V only



SoC HDA/CAN/RGMII



CAN Bus such as GPIO 1.8V/3.3V



UART2 for Debug



RESERVED STRAP

GP_F07 R213 Do Not Solder R205 Do Not Solder

High - RSVD
Low - Normal Operat i on(Default)
Weak Internal PD 20K

BOOT STRAP BIT0

GP_C05 R291 Do Not Solder R246 Do Not Solder

High - RSVD
Low - BOOT FROM UFS
Low - BOOT FROM SPI (Default)
Weak Internal PD 20K

BOOT STRAP BIT1

GP_H00 R195 Do Not Solder R194 Do Not Solder

High - RSVD
Low - Normal Operat i on(Default)
Weak Internal PD 20K
PU to DISABLE ESP

BOOT STRAP BIT2

GP_H01 R187 Do Not Solder R186 Do Not Solder

High - RSVD
Low - Normal Operat i on(Default)
Weak Internal PD 20K

BOOT STRAP BIT3

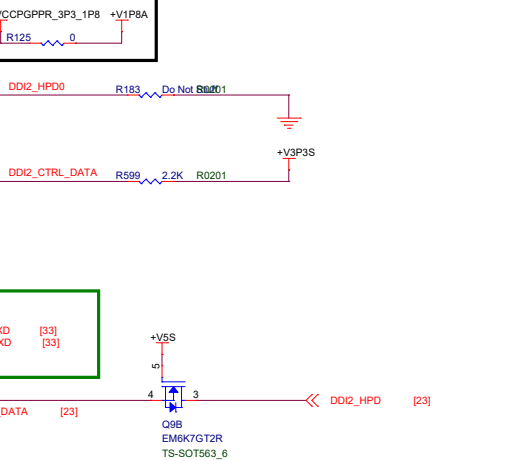
GP_H02 R178 Do Not Solder R173 Do Not Solder

High - RSVD
Low - Normal Operat i on(Default)
Weak Internal PD 20K

FLASH DESCRIPTOR SECURITY OVERRIDE

HDA_SDOOUT R126 Do Not Solder

High - Override
Low - Security Measures Not Override (Default)
Weak Internal PD 20K



PICOEHL(A11)

AAEON Technology INC.

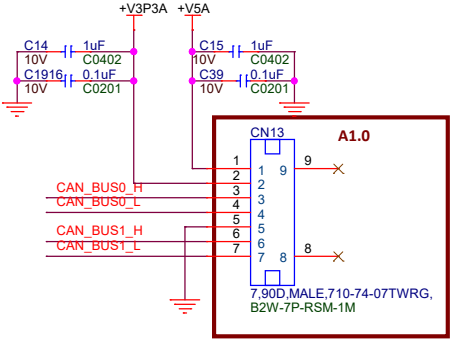
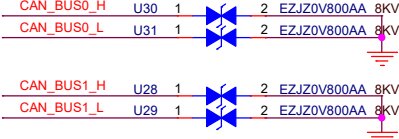
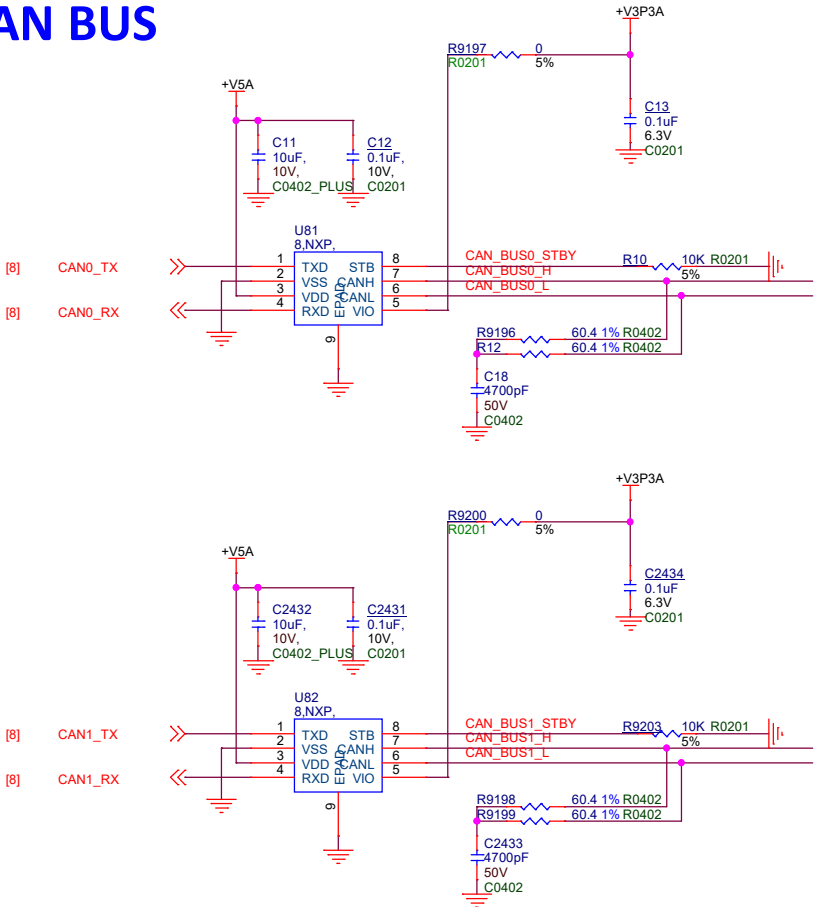
SoC HDA/CAN/RGMII

Size Document Number Rev

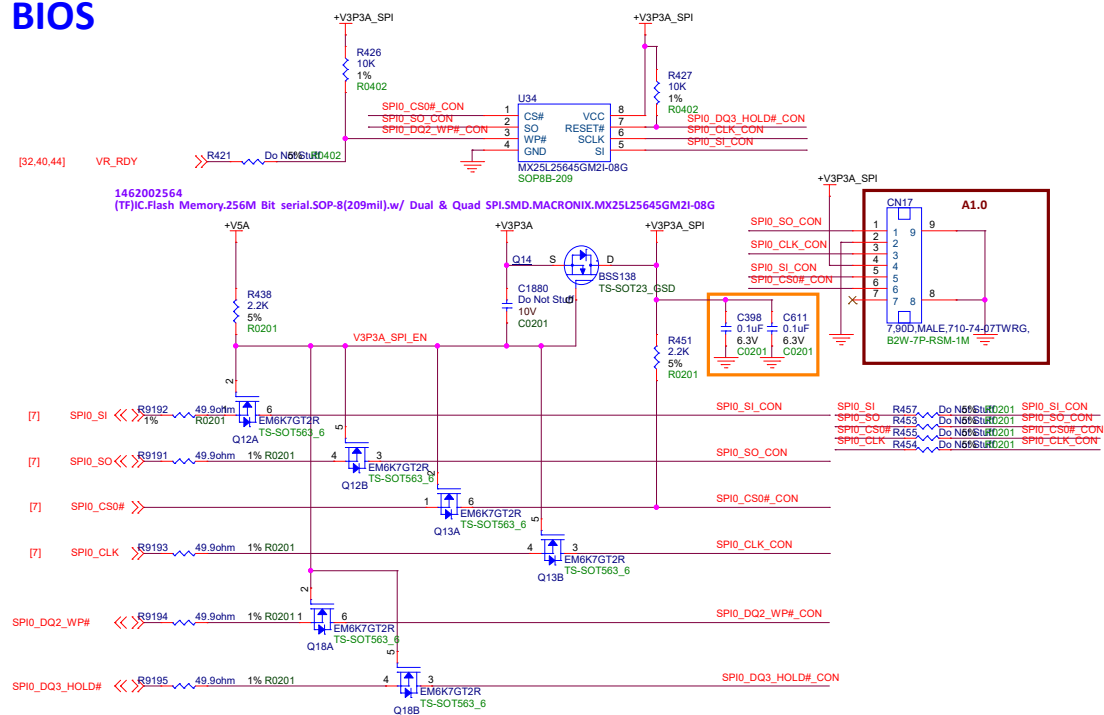
Custom PICO-EHL4 A1.1_0_0

Date: Tuesday, May 31, 2022 Sheet 8 of 45

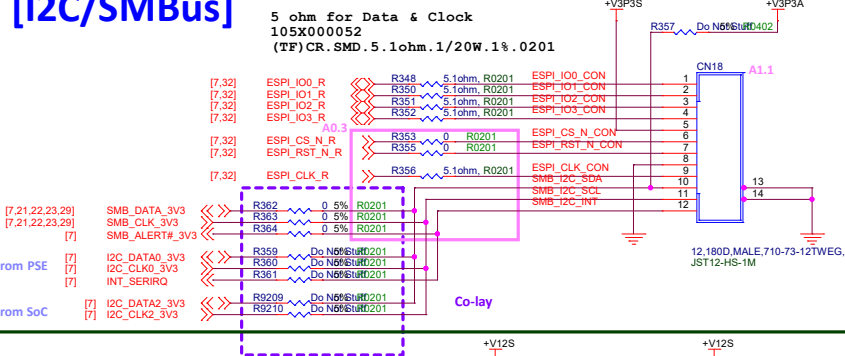
CAN BUS



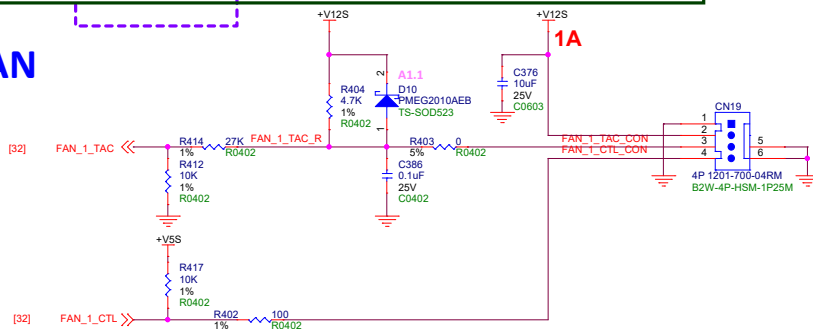
BIOS



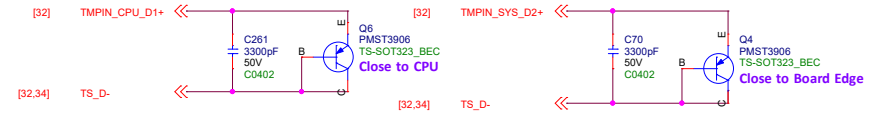
eSPI Connector (Debug Card)



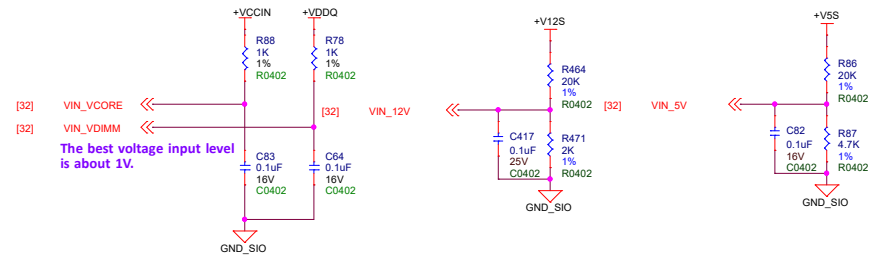
Smart FAN



Temperature Monitor(CPU, SYS)



Voltage Monitor



Discharge Circuit

