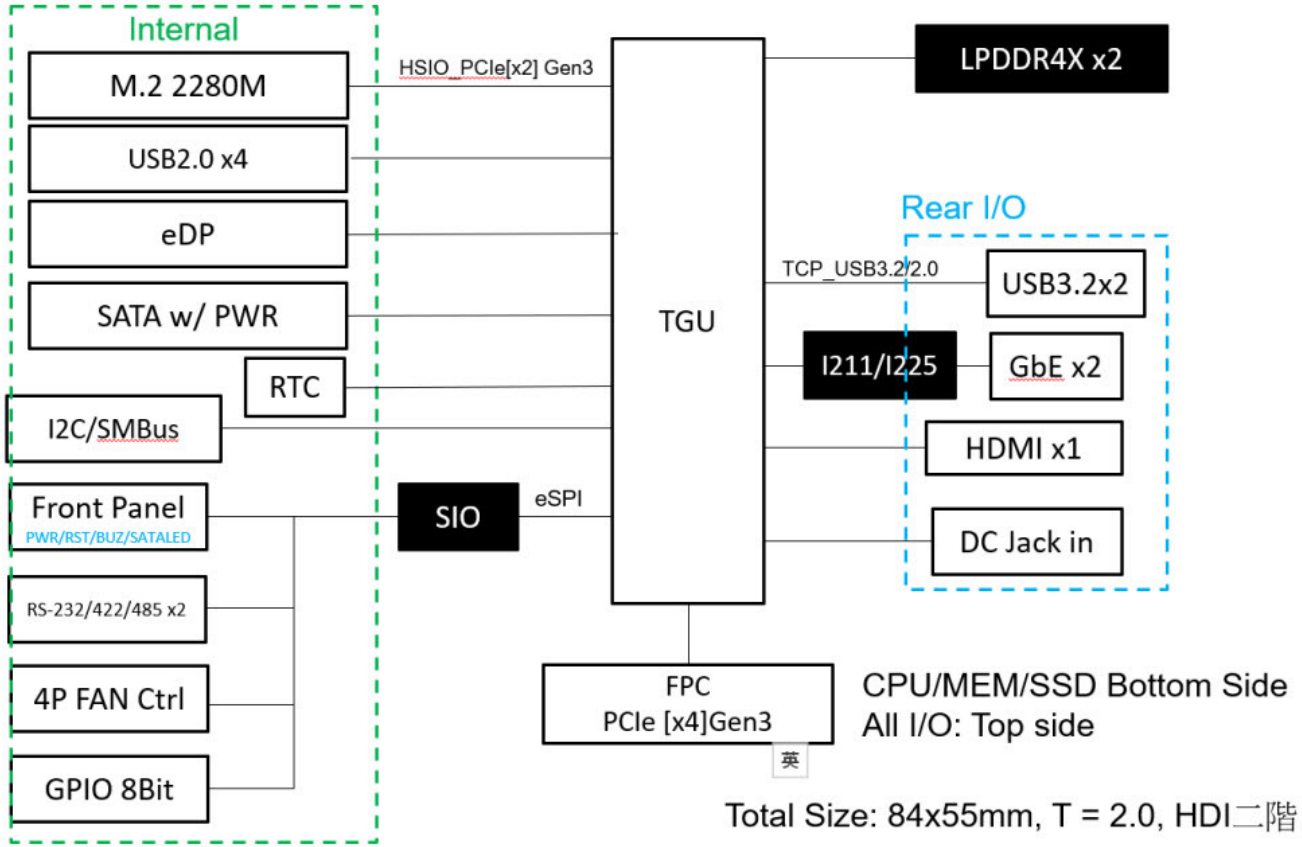
Project Name : DN-TGU8
Project Number:
Version: A0.3_0_0



<Variant Name>

AAEON Technology INC.

Title: Cover Sheet

Size | Document Number: DN-TGU8 | Rev: A0.3_0_0

Date: Tuesday, January 04, 2022 | Sheet 1 of 37

SoC GPIO Pins :

Name	Power Well	Default	GPIO Function	Location
GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	+V3P3S	PD	DDI3_HPD	DH52
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK	+V3P3S	PD	DDI4_HPD	DK45
GPP_E4/DEVSLP0	+V3P3A	PU	USB2_OC2#	DG8
GPP_E5/DEVSLP1	+V3P3A	PU	USB2_OC1#	DN6
GPP_E3/CPU_GP0	+V3P3A	PU	SMI#	DU5
GPP_E7/CPU_GP1	+V3P3A	PU	SCI#	DF8
GPP_T2	+V3P3A	PD	BOARD_ID1	DT35
GPP_T3	+V3P3A	PD	BOARD_ID0	DN33
GPP_U4	+V3P3A	PD	BOARD_ID3	DG19
GPP_U5	+V3P3A	PD	BOARD_ID2	DG17
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#	+V3P3A	PU	ESPI_ALT#	CY50
GPP_H19/TIME_SYNC0	+V3P3S	PU	EC_KBRST#	DJ27

EC GPIO Pins :

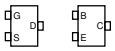
Name	Power Well	Default	GPIO Function	Location	Note
KSI1/AFD#	+V3P3A	Input	I_RSMRST	J13	
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7	+V3P3A	Output	O_RSMRST	A1	When J13 active HIGH, then PU A1 after 10ms
KSO5/PD5	+V3P3A	Output	ESPI_EN#	J8	PU to Enable COM eSPI out
L80HLAT/BAO/WUI24/GPE0	+V3P3A	Input	GPI0	N2	
EGAD/WUI25/GPE1	+V3P3A	Input	GPI1	A13	
EGCS#/WUI26/GPE2	+V3P3A	Input	GPI2	A12	
EGCLK/WUI27/GPE3	+V3P3A	Input	GPI3	B12	
HSCE#/GPH3/ID3	+V3P3A	Output	GPO0	A9	
HSCK/GPH4/ID4	+V3P3A	Output	GPO1	B8	
HMISO/GPH5/ID5	+V3P3A	Output	GPO2	A8	
HMOSI/GPH6/ID6	+V3P3A	Output	GPO3	B7	

SMBus/I2C Addresses :

Device	address
I219	0XC8
PTN3460BS/F6	0C0h

PCB Footprints

MOSFET BJT



PCB STACK :

Board: TU883
Impedence: 50ohm +/-10%
Thickness: 2.0mm +-10%

- Layer 1 : Component (Top)
- Layer 2 : GND (GND1)
- Layer 3 : Signal (IN1)
- Layer 4 : GND (GND2)
- Layer 5 : Signal (IN2)
- Layer 6 : GND (GND3)
- Layer 7 : Signal (IN3)
- Layer 8 : POWER (VCC)
- Layer 9 : POWER (VCC)
- Layer 10 : Signal (IN4)
- Layer 11 : GND (GND4)
- Layer 12 : Signal (IN5)
- Layer 13 : GND (GND5)
- Layer 14 : Signal (IN6)
- Layer 15 : GND (GND6)
- Layer 16 : Solder (Bottom)

<Variant Name>

AAEON An ASUS Company

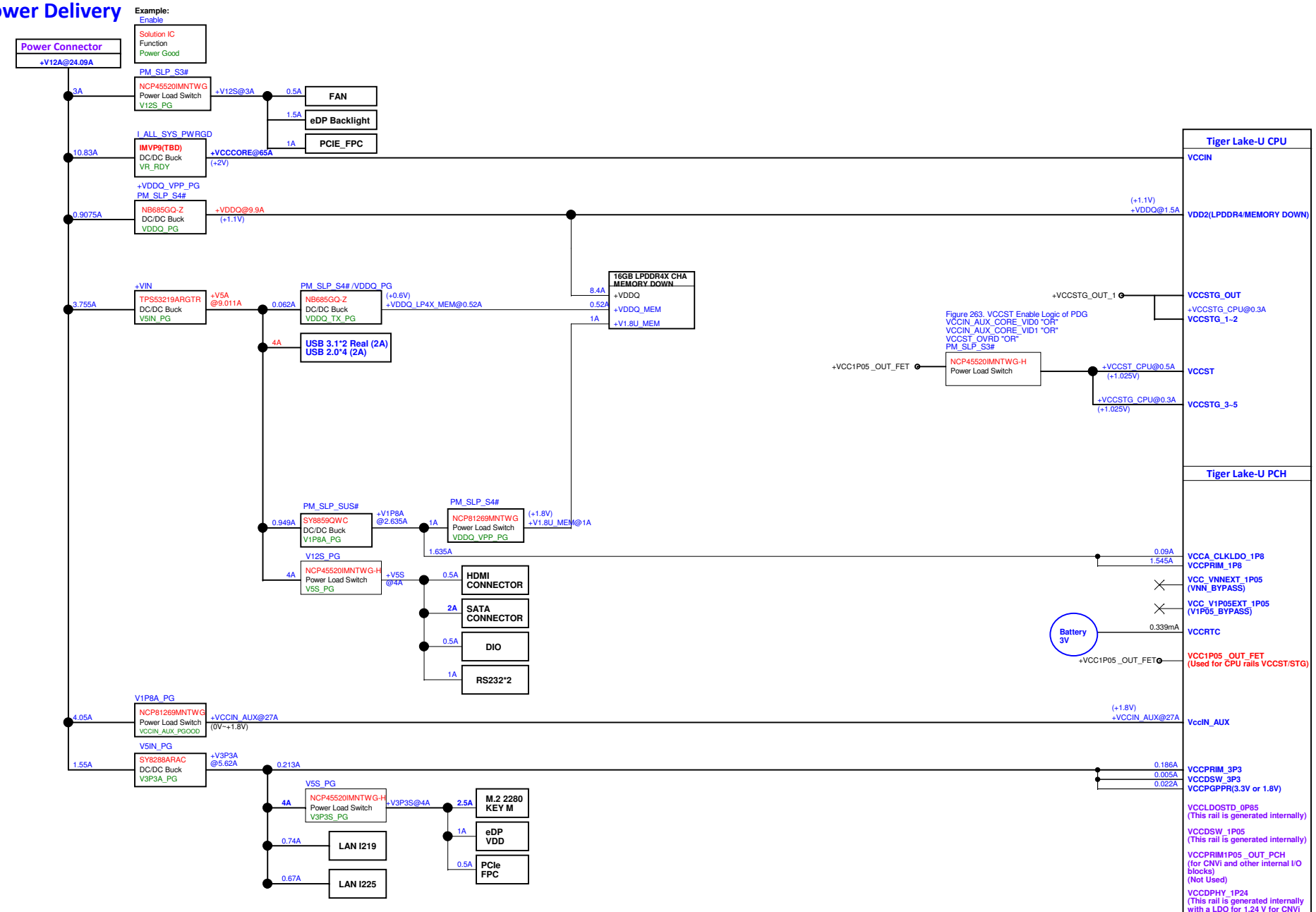
AAEON Technology INC.

Title: System Setting

Size | Document Number: DN-TGU8 | Rev: A0.3_0_0

Date: Tuesday, January 04, 2022 | Sheet 2 of 37

Power Delivery



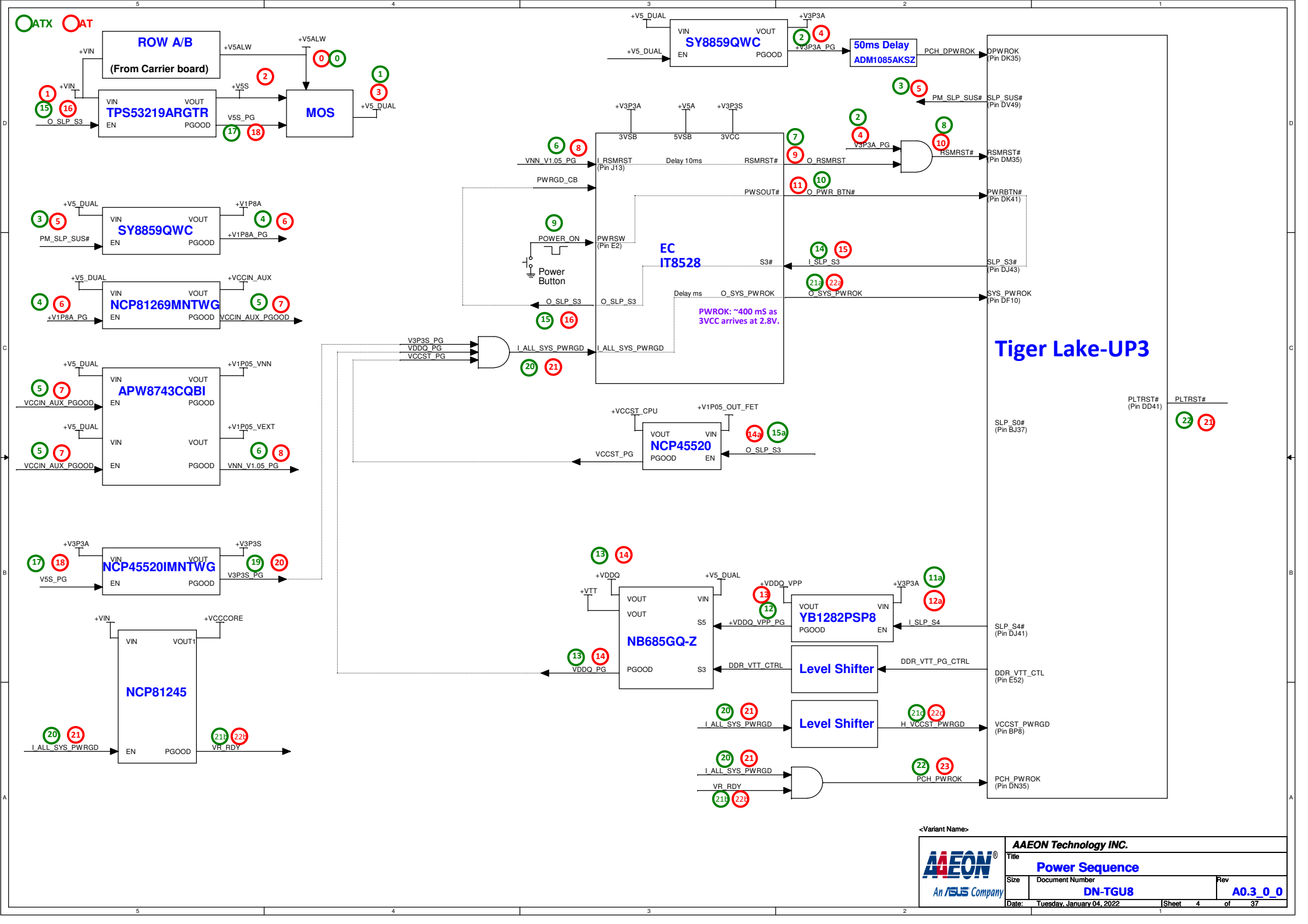
<Variant Name>

AAEON Technology INC.

Title: Power Delivery

Size | Document Number: DNI-TGU8 | Rev: A0.3_0_0

Date: Tuesday, January 04, 2022 | Sheet 3 of 37


ATX
AT
ROW A/B
(From Carrier board)
+VIN
+V5ALW
+V5S
+V5S_PG
O_SLP_S3
TPS53219ARGTR
MOS
+V5_DUAL
SY8859QWC
+V1P8A
+V1P8A_PG
PM_SLP_SUS#
NCP81269MNTWG
+VCCIN_AUX
VCCIN_AUX_PGOOD
APW8743CQBI
+V1P05_VNN
+V1P05_VEXT
VNN_V1.05_PG
NCP45520IMNTWG
+V3P3A
+V3P3S
V5S_PG
V3P3S_PG
NCP81245
+VCCCORE
I_ALL_SYS_PWRGD
VR_RDY
SY8859QWC
+V3P3A_PG
50ms Delay
ADM1085AKSZ
PCH_DPWROK
DPWROK
(Pin DK35)
PM_SLP_SUS#
SLP_SUS#
(Pin DV49)
+V3P3A
+V5A
+V3P3S
3VSB
5VSB
3VCC
VNN_V1.05_PG
I_RSMRST
(Pin J13)
Delay 10ms
RSMRST#
O_RSMRST
RSMRST#
(Pin DM35)
PWRGD_CB
PWSOUT#
O_PWR_BTN#
PWRBTN#
(Pin DK41)
POWER_ON
PWRSW
(Pin E2)
Power
Button
EC
IT8528
S3#
I_SLP_S3
SLP_S3#
(Pin DJ43)
Delay ms
O_SYS_PWROK
SYS_PWROK
(Pin DF10)
PWROK: ~400 mS as
3VCC arrives at 2.8V.
V3P3S_PG
VDDQ_PG
VCCST_PG
I_ALL_SYS_PWRGD
Tiger Lake-UP3
+VCCST_CPU
+V1P05_OUT_FET
NCP45520
VCCST_PG
O_SLP_S3
PLTRST#
(Pin DD41)
SLP_S0#
(Pin BJ37)
+VDDQ
+VTT
+V5_DUAL
NB685GQ-Z
+VDDQ_VPP_PG
YB1282PSP8
+VDDQ_VPP
I_SLP_S4
SLP_S4#
(Pin DJ41)
DDR_VTT_CTRL
Level Shifter
DDR_VTT_PG_CTRL
DDR_VTT_CTL
(Pin E52)
H_VCCST_PWRGD
VCCST_PWRGD
(Pin BP8)
PCH_PWROK
PCH_PWROK
(Pin DN35)
<Variant Name>
AAEON Technology INC.
Title
Power Sequence
Size
Document Number
DN-TGU8
Rev
A0.3_0_0
Date: Tuesday, January 04, 2022
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GPP_D10	TBT LSX #2 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

The internal pull-down 20k is disabled after RSMRST# de-asserts.

+V3P3A — R1 4.7K 5% R0201 — DDI3_CTRL_DATA

GPP_D12	TBT LSX #3 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

The internal pull-down 20k is disabled after RSMRST# de-asserts.

+V3P3A — R2 4.7K 5% R0201 — GPP_D12

TBT_LSX0_RXD	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R4 4.7K 5% R0201 — GPP_E19

TBT_LSX1_RXD	TBT LSX #1 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

This strap has a 20 kohm ± 30% internal pull-down

+V3P3A — R7 4.7K 5% R0201 — DDI2_CTRL_DATA

+V3P3S — R9 2.2K 5% R0201 — DDI1_CTRL_CLK; R10 2.2K 5% R0201 — DDI1_CTRL_DATA

EDP

HDMI 1.65G

Setting as GPIO

CPU1A

1 OF 21

[19] DDI0_LANE3_DP AC2 DDIA_TXP_3
[19] DDI0_LANE3_DN AC1 DDIA_TXN_3
[19] DDI0_LANE2_DP AD2 DDIA_TXP_2
[19] DDI0_LANE2_DN AD1 DDIA_TXN_2
[19] DDI0_LANE1_DP AF1 DDIA_TXP_1
[19] DDI0_LANE1_DN AF2 DDIA_TXN_1
[19] DDI0_LANE0_DP AG2 DDIA_TXP_0
[19] DDI0_LANE0_DN AG1 DDIA_TXN_0

[19] DDI0_AUX_DP AJ2 DDIA_AUX_P
[19] DDI0_AUX_DN AJ1 DDIA_AUX

DN4 DT8 GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA

[19] DDI0_HPD — DDI0_HPD — DR5 GPP_E14/DDSP_HPDA/DISP_MISCA

R3 100K 5% R0201

[20] DDI1_LANE3_DP T12 DDIB_TXP_3
[20] DDI1_LANE3_DN T11 DDIB_TXN_3
[20] DDI1_LANE2_DP Y11 DDIB_TXP_2
[20] DDI1_LANE2_DN Y9 DDIB_TXN_2
[20] DDI1_LANE1_DP T9 DDIB_TXP_1
[20] DDI1_LANE1_DN P9 DDIB_TXN_1
[20] DDI1_LANE0_DP V11 DDIB_TXP_0
[20] DDI1_LANE0_DN V9 DDIB_TXN_0

AB9 AD9 DDIB_AUX_P
DDIB_AUX

[20] DDI1_CTRL_CLK — DDI1_CTRL_CLK — DM29 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
[20] DDI1_CTRL_DATA — DDI1_CTRL_DATA — DK27 GPP_H17/DDPB_CTRLDATA

[20] DDI1_HPD — DDI1_HPD — DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

DG47 DJ45 GPP_A21/DDPC_CTRLCLK/I2S5_TXD
GPP_A22/DDPC_CTRLDATA/I2S5_RXD

GPP_E19 — DU8 DV8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

DDI2_CTRL_DATA — DF6 DD6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

DDI3_CTRL_DATA — DN23 DM23 GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

TP1 TP20 — GPP_D11 DK23 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12 DN21 GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

DF43 DF45 DF47 GPP_A17/DISP_MISCC/I2S4_TXD
GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

DH52 DK45 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

[19] DDI0_VDDEN — DDI0_VDDEN — DM8 EDP_VDDEN
[19] DDI0_BKLTEN — DDI0_BKLTEN — DN8 EDP_BKLTEN
[19] DDI0_BKLTCTL — DDI0_BKLTCTL — DG10 EDP_BKLTCTL

<TOLERANCE>

TCP0_TXRX_P1 AY2
TCP0_TXRX_N1 AY1
TCP0_TXRX_P0 BB2
TCP0_TXRX_N0 BB1
TCP0_TX_P1 AM5
TCP0_TX_N1 AM7
TCP0_TX_P0 AT7
TCP0_TX_N0 AT5
TCP0_AUX_P AP7
TCP0_AUX AP5

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX AF5

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX BK7

TC_RCOMP_P AN2 TCRCOMP_DP — R6 150 1% R0402 — AN1 TCRCOMP_DN
TC_RCOMP

DSI_DE_TE_2 — M8 DSI_DE_TE_2 — TP2 TP20

DDI_RCOMP — AB1 EDP_RCOMP

DISP_UTILS/DSI_DE_TE_1 — CE4 DSI_DE_TE_1 — TP3 TP20 — R8 150 1% R0402

USB3/USB2 Port Pairing for USB-C* Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	0
PCH USB2 port#	2	3	4	0

20210519, A02, Change USB3.2 Port 1/2 from TCP to PCH HSIO.

USB 3.2 PORT 1/2

<Variant Name>

AAEON Technology INC.

Title: SoC DDI

Size | Document Number: DN-TGU8 | Rev: A0.3_0_0

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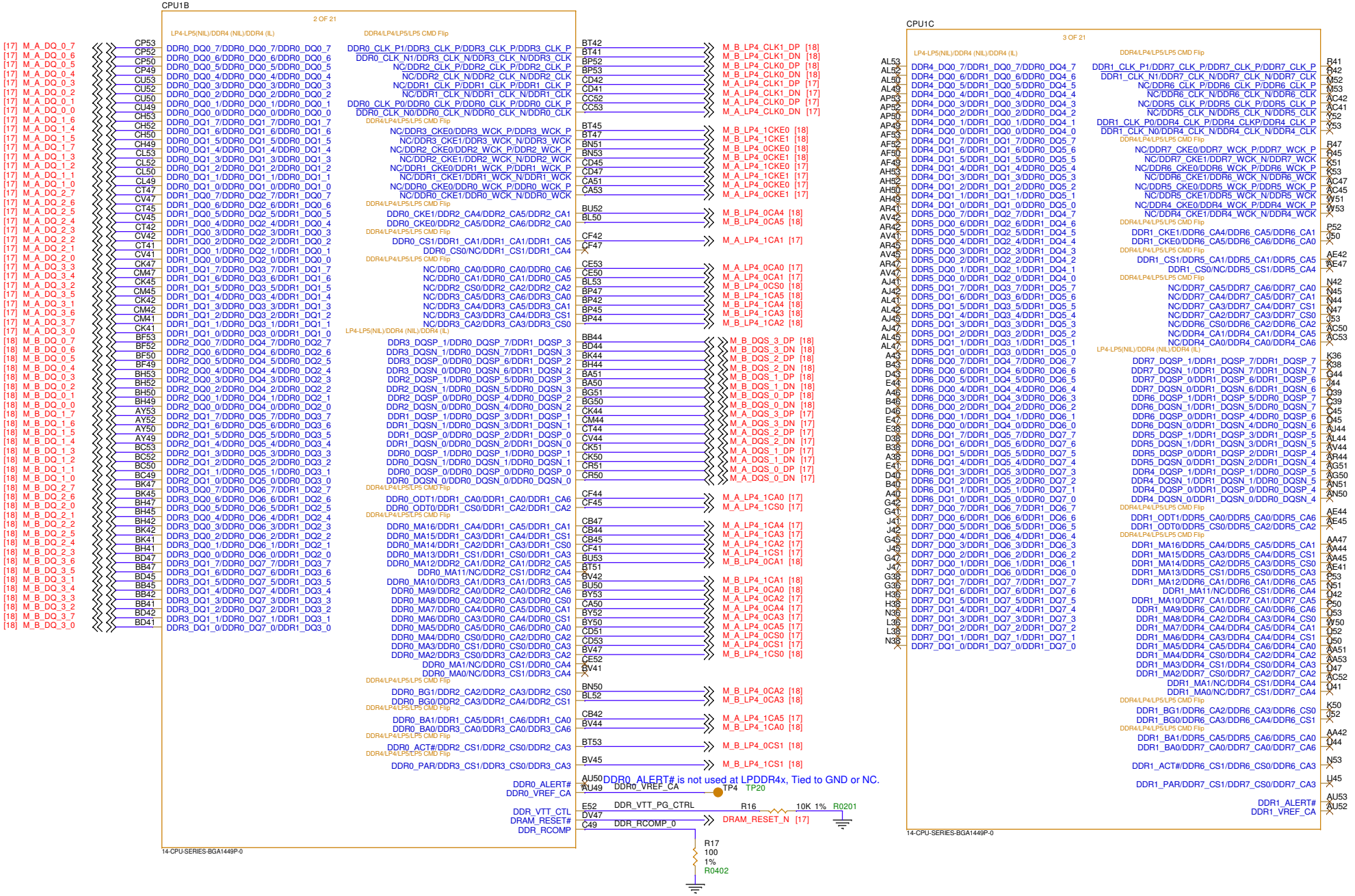
SoC LPDDR4x x32



<Variant Name>

AAEON Technology INC.

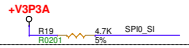
An ASUS Company

Title	SoC LPDDR4x	
Size	Document Number: DN-TGU8	Rev: A0.3_0_0
Date: Tuesday, January 04, 2022	Sheet 6 of 37	

SoC SPI/LPC/SMBus

SPI0_MOSI	Reserved
	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on- board device driving it to opposite direction during strap sampling.

External pull-up is required. Recommend 4.7 kohm pull up.



SPI0_IO2	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

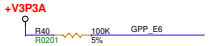
External pull-up is required.

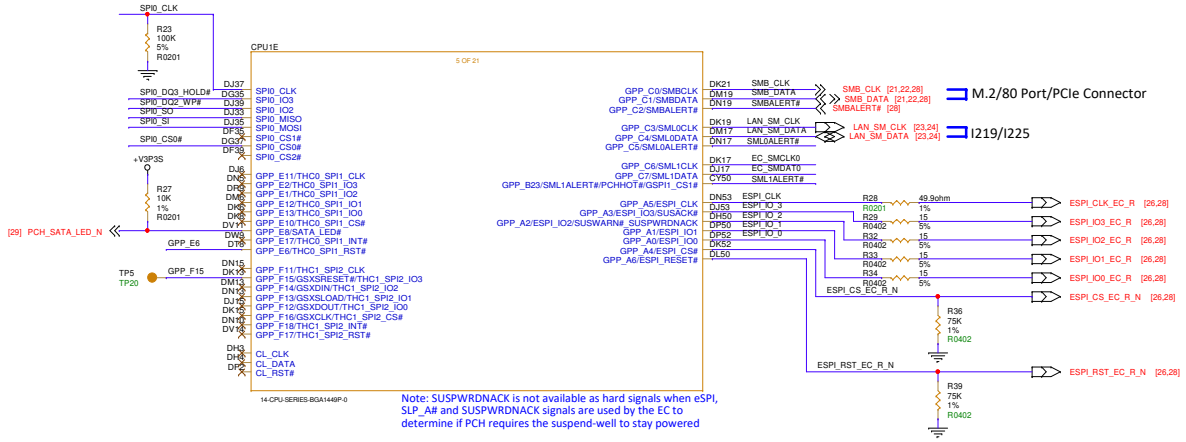
SPI0_IO3	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

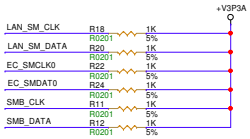
External pull-up is required.

GPP_E6	JTAG ODT Disable
0	JTAG ODT is disabled
1 *	JTAG ODT is enabled

This strap does not have an internal pull-up or pull-down. External pull-up is recommended





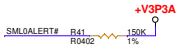


SMBALERT#	TLS confidentiality
0	Disable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 *	Enable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to pupport IntelR AMT with TLS.

* Default, Internal Pull-Down 20K

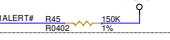
SML0ALERT#	This is bit 0 (LSB) of a total of 4-bit boot strap configuration encodings
0 *	
1	

* Default, Internal Pull-Down 20K

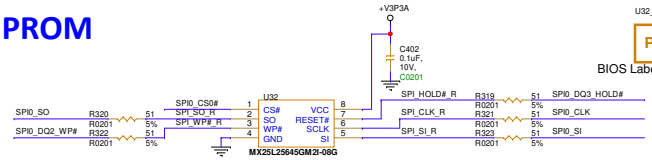


SML1ALERT#	CPUNSSC CLOCK FREQ
0 *	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

* Default, Internal Pull-Down 20k
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.



BIOS EEPROM



1462002564 / (TF)IC.Flash Memory.256M Bit serial.SOP-8(209mil).w/ Dual & Quad SPI.SMD.MACRONIX.MX25L25645GM2I-08G

BIOS Header (Colay),remove this part at PVT.

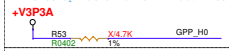
A03, 20210831, Remove JP1

DBG_PMODE	Reserved
	This strap should sample high. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-up.

GPP_H0	BFX STRAP 1- BIT 2
	0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled

This strap has a 20 kohm ± 30% internal pull-down.

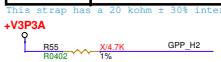


GPP_H1	BFX STRAP 2- BIT 3

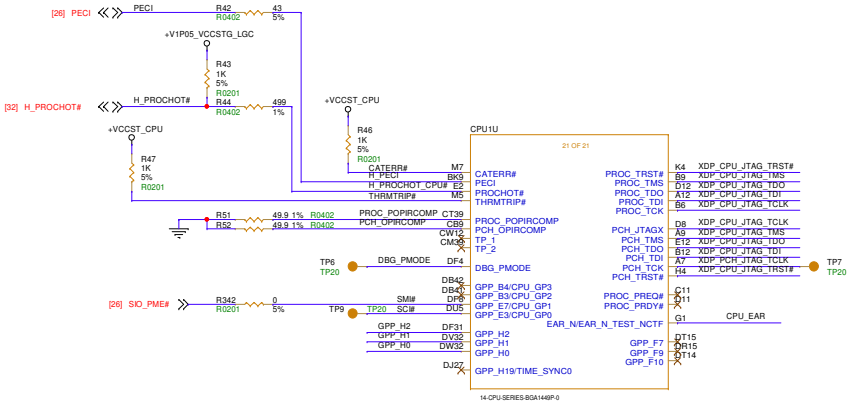
This strap has a 20 kohm ± 30% internal pull-down.

GPP_H2	BFX STRAP 3- BIT 4

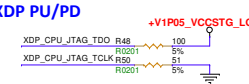
This strap has a 20 kohm ± 30% internal pull-down.



XDP



XDP PU/PD



GPP_F7	Reserved
	This strap should sample LOW. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

GPP_F10	Reserved
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

CPU_EAR	Stall CPU reset sequence until de-asserted:
1 *	(Default) Normal Operation; No stall.
0	Stall

<Variant Name>

AAEON Technology INC.

Title	SoC SPI/LPC/SMBus	
Size	Document Number	Rev
	DN-TGU8	A0.3_0_0
Date: Tuesday, January 04, 2022	Sheet 7 of 37	

SoC HDA/SD

HDA_SDO	Flash Descriptor Security Override
0 *	Disabled (Default)
1	Enable (Disable ME)(debug ONLY)

* Default, Internal Pull-Down 20K

R361 1K 5% R0201 — HDA_SDO

A02, 20210407, add R361 and remove TP13 for intel ME disable issue.

All HDA R close to SOC

Disabling and Termination Guidelines for High Definition Audio Interface

When HDA_SDIN[1:0] interface is not implemented on the platform the signal pin(s) may be left unconnected.

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HDA_SDO — DR38 GPP_R0/HDA_BCLK/I2S0_SCLK; DU37 GPP_R1/HDA_SYNC/I2S0_SFRM; DT37 GPP_R2/HDA_SDO/I2S0_TXD; DV37 GPP_R3/HDA_SDI0/I2S0_RXD

DV41 GPP_R4/HDA_RST#

DL53 GPP_A7/I2S2_SCLK/DMIC_CLK_A0

DG51 GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0

DG50 GPP_A10/I2S2_RXD/DMIC_DATA1

DL49 GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1

DL52 GPP_A11/PMC_I2C_SDA/I2S3_SCLK

DH49 GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0

R57 200 1% R0201 — SNDW_RCOMP — DF33 SNDW_RCOMP

DW15 GPP_F8/I2S_MCLK2_INOUT; DW24 GPP_D19/I2S_MCLK1

DG41 GPP_A23/I2S1_SCLK; DT38 GPP_R7/I2S1_SFRM; DV38 GPP_R6/I2S1_TXD; DW38 GPP_R5/HDA_SDI1/I2S1_RXD

DN31 GPP_S6/SNDW3_CLK/DMIC_CLK_A0; DM31 GPP_S7/SNDW3_DATA/DMIC_DATA0

DK33 GPP_S4/SNDW2_CLK/DMIC_CLK_A1; DK31 GPP_S5/SNDW2_DATA/DMIC_DATA1

DW35 GPP_S2/SNDW1_CLK/DMIC_CLK_B0; DV35 GPP_S3/SNDW1_DATA/DMIC_CLK_B1

DT32 GPP_S0/SNDW0_CLK; DR35 GPP_S1/SNDW0_DATA

14-CPU-SERIES-BGA1449P-0

GSPI1_MOSI	No Reboot
0 *	REBOOT ENABLED
1	NO REBOOT

* Default, Internal Pull-Down 20K

SPKR	Top Swap Override
0 *	Disabled
1	Enable

* Default, Internal Pull-Down 20K
CRB: PULL UP 100K RESISTOR PRESENT ON THIS NET

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TP14 — TP20 GSPI0_MOSI — DC53 GPP_B16/GSPI0_CLK; DA51 GPP_B18/GSPI0_MOSI; DC49 GPP_B17/GSPI0_MISO

[29] SPKR — SPKR — DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#; DC52 GPP_B15/GSPI0_CS0#

CY49 GPP_B20/GSPI1_CLK; CY53 GPP_B22/GSPI1_MOSI; CY52 GPP_B21/GSPI1_MISO; DA50 GPP_B19/GSPI1_CS0#

TP15 — TP20 GPP_C9 — DV21 GPP_C9/UART0_TXD

TP16 — TP20 GPP_C8 — DT21 GPP_C8/UART0_RXD

DR21 GPP_C11/UART0_CTS#; DW21 GPP_C10/UART0_RTS#

20200717, A02, Add TP30~TP33 for BIOS request.

DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD; DT19 GPP_C12/UART1_RXD/ISH_UART1_RXD; DR18 GPP_C15/UART1_CTS#/ISH_UART1_CTS#; DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#

TP17 — TP20 GPP_C21 — DJ21 GPP_C21/UART2_TXD

TP18 — TP20 GPP_C20 — DG23 GPP_C20/UART2_RXD

DJ19 GPP_C23/UART2_CTS#; DF21 GPP_C22/UART2_RTS#

DV18 GPP_C17/I2C0_SCL; DW18 GPP_C16/I2C0_SDA

DJ23 GPP_C19/I2C1_SCL; DT18 GPP_C18/I2C1_SDA

[28] I2C2_SCL — I2C2_SCL — DJ29 GPP_H5/I2C2_SCL

[28] I2C2_SDA — I2C2_SDA — DJ31 GPP_H4/I2C2_SDA

DF29 GPP_H7/I2C3_SCL; DG29 GPP_H6/I2C3_SDA

DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD; DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

DR27 GPP_D14/ISH_UART0_TXD; DW27 GPP_D13/ISH_UART0_RXD; DV25 GPP_D16/ISH_UART0_CTS#; DT25 GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5

DB45 GPP_B6/ISH_I2C0_SCL; DB44 GPP_B5/ISH_I2C0_SDA

CY39 GPP_B8/ISH_I2C1_SCL; DB47 GPP_B7/ISH_I2C1_SDA

DD47 GPP_B10/I2C5_SCL/ISH_I2C2_SCL; DD44 GPP_B9/I2C5_SDA/ISH_I2C2_SDA

DJ8 GPP_E16/ISH_GP7; DR7 GPP_E15/ISH_GP6; DR24 GPP_D18/ISH_GP5; DU25 GPP_D17/ISH_GP4; DV31 GPP_D3/ISH_GP3/BK3/SBK3; DU31 GPP_D2/ISH_GP2/BK2/SBK2; DT27 GPP_D1/ISH_GP1/BK1/SBK1; DV27 GPP_D0/ISH_GP0/BK0/SBK0

GPP_RCOMP — DR51 GPPC_RCOMP R58 1% 200 R0201

GPP_T3 — DN33 BOARD_ID0

GPP_T2 — DT35 BOARD_ID1

GPP_U5 — DG17 BOARD_ID2

GPP_U4 — DG19 BOARD_ID3

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+V3P3S — R59 1K 5% R0201 — I2C2_SCL; R60 1K 5% R0201 — I2C2_SDA

80 PORT

+V3P3A — BOARD_ID0 — R61 X/2.2K 5% R0201; R62 20K 1% R0201

+V3P3A — BOARD_ID1 — R63 X/2.2K 5% R0201; R64 20K 1% R0201

+V3P3A — BOARD_ID2 — R65 X/2.2K 5% R0201; R66 20K 1% R0201

+V3P3A — BOARD_ID3 — R67 X/2.2K 5% R0201; R68 20K 1% R0201

BOARD ID

Memory Down Select		
BID0	BID1	Memory Size

<Variant Name>

AAEON Technology INC.

Title: SoC HDA/I2C

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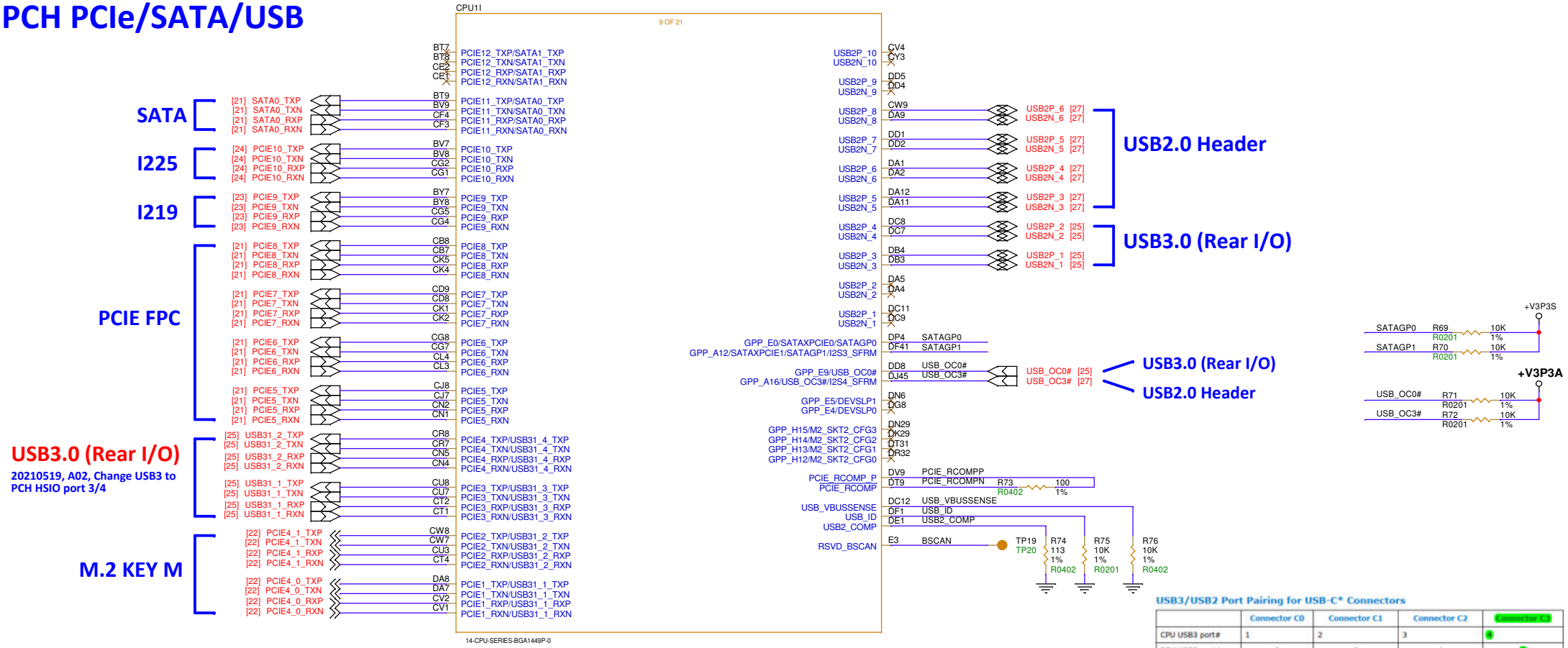
PCH PCIe/SATA/USB



USB3/USB2 Port Pairing for USB-C* Connectors

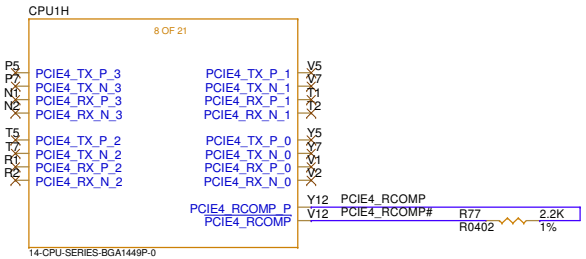
	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

Figure 70. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4			GbE	GbE	GbE		SATA 0	SATA 1

<Variant Name>

PROC PCIe



AAEON® An ASUS Company	AAEON Technology INC.	
	Title: SoC PCIe/SATA/USB	
	Size	Document Number: DN-TGU8 — Rev: A0.3_0_0
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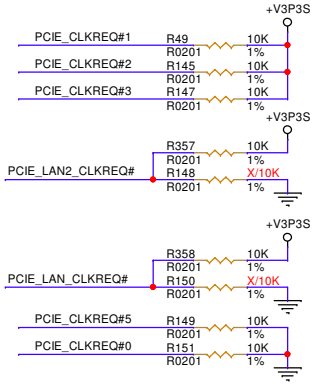
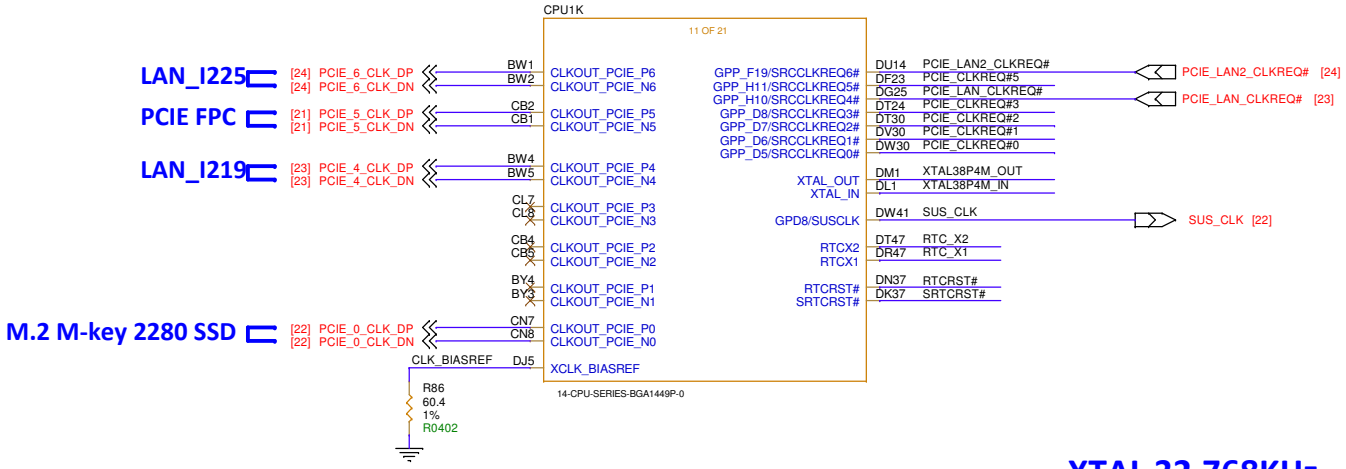
SoC PCIE_CLK/ RTC/ XTAL

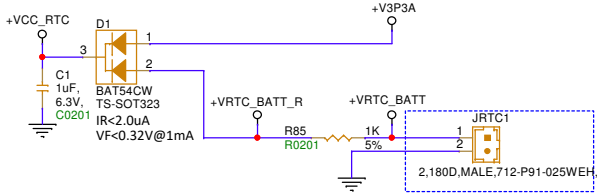




CLKOUT_PCIE_P /N [6:4, 2:1] = Support up to PCIe Gen3
CLKOUT_PCIE_P /N [3, 0] = Support up to PCIe Gen4

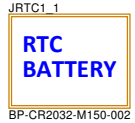
+VCC_RTC

VCC_RTC level can't over 3.2V

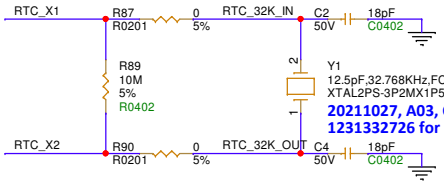


20210831, A03, Change P/N of JRTC1 from 1655902034 to 1655X00019 by PE suggestion.

20220104, A03, Change Part's TYPE from DIP to SMD by PE request.

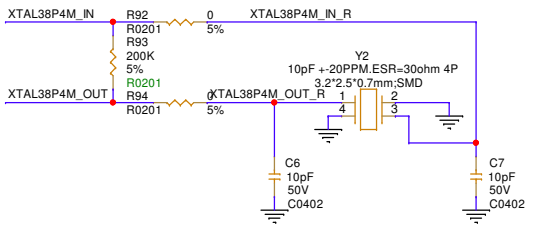


XTAL 32.768KHz

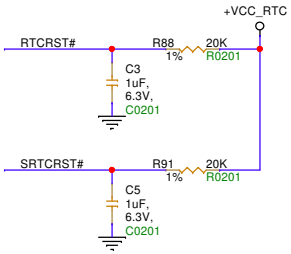


20211027, A03, Change P/N Y1 from 1231327631 to 1231332726 for change vendor

XTAL 38.4MHz



RTC_RESET



<Variant Name>

AAEON Technology INC.

Title	SoC PCIE_CLK/ RTC	
Size: A3	Document Number: DN-TGU8	Rev: A0.3_0_0
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SoC CNVi

GPP_F2	M.2 CNVi Mode Select
0 *	Integrated CNVi enabled.
1	Integrated CNVi disabled.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.

+V3P3A

R95 R0201 4.7K 5% GPP_F2

GPP_F0	XTAL SEL1
0 *	38.4/19.2MHZ (DEFAULT)
1	24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

* Default, Internal Pull-Down 20k
24 MHz crystal is not supported

CNVI_WT_RCOMP can be left unconnected if not used.

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DK47 CNVI_WT_D1P
DM47 CNVI_WT_D1N
DN49 CNVI_WT_D0P
DR49 CNVI_WT_D0N
DN45 CNVI_WT_CLKP
DN47 CNVI_WT_CLKN

DU43 CNVI_WR_D1P
DV43 CNVI_WR_D1N
DR44 CNVI_WR_D0P
DT43 CNVI_WR_D0N
DV44 CNVI_WR_CLKP
DW44 CNVI_WR_CLKN

TP20 TP20 CNV_WT_RCOMP DN51 CNVI_WT_RCOMP

DJ13 GPP_F3/CNV_RGI_RSP/UART0_CTS#
GPP_F2 DG13 GPP_F2/CNV_RGI_DT/UART0_TXD
DF15 GPP_F1/CNV_BRI_RSP/UART0_RXD
TP21 TP20 GPP_F0 DF17 GPP_F0/CNV_BRI_DT/UART0_RTS#

DJ10 GPP_F5/MODEM_CLKREQ/CRF_XTAL_CLKREQ
DV15 GPP_F6/CNV_PA_BLANKING
DK10 GPP_F4/CNV_RF_RESET#

CSI_F_DP_1 D22
CSI_F_DN_1 B22
CSI_F_DP_0 E22
CSI_F_DN_0 D20
CSI_F_CLK_P A20
CSI_F_CLK B20

CSI_E_DP_1/CSI_F_DP_2 B18
CSI_E_DN_1/CSI_F_DN_2 A18
CSI_E_DP_0/CSI_F_DP_3 D18
CSI_E_DN_0/CSI_F_DN_3 E18
CSI_E_CLK_P C16
CSI_E_CLK D16

CSI_C_DP_2 D15
CSI_C_DN_2 E15
CSI_C_DP_3 A15
CSI_C_DN_3 B15

CSI_C_DP_1 L18
CSI_C_DN_1 N18
CSI_C_DP_0 L20
CSI_C_DN_0 N20
CSI_C_CLK_P G20
CSI_C_CLK H20

CSI_B_DP_1 H16
CSI_B_DN_1 G16
CSI_B_DP_0 G18
CSI_B_DN_0 H18
CSI_B_CLK_P L16
CSI_B_CLK N16

CSI_B_DP_2 G14
CSI_B_DN_2 H14
CSI_B_DP_3 L14
CSI_B_DN_3 N14

CSI_RCOMP K14 CSI_RCOMP

R96 150 1% R0402

GPP_H23/IMGCLKOUT4 DK25
GPP_H22/IMGCLKOUT3 DM25
GPP_H21/IMGCLKOUT2 DN25
GPP_H20/IMGCLKOUT1 DJ25
GPP_D4/IMGCLKOUT_0/BK4/SBK4 DR30

14-CPU-SERIES-BGA1449P-0

<Variant Name>

AAEON An ASUS Company

AAEON Technology INC.

Title: SoC CNVi

Size | Document Number: DN-TGU8 | Rev: A0.3_0_0

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SoC System

GPD7	Reserved
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R78 R0201 100K 5% — SLP_S0#

PDG: DSW_PWROK and RSMRST# are always separate power good signals

SIO SPEC: DSW_PWROK is power good signal of 5VSB which is delayed 66ms as 5VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.

[26] PCH_DPWROK — D5 (2, 1) 1PS79SB30 TS-SOD523 — PCH_DPWROK

[26,30] V5IN_PG

20210929, A03, ADD D5 to find tune power down sequence issue (tPCH14 timing).

SPIVCCIOSEL	STRAP FOR SPI 1.8V/3.3V SELECTION
0 *	3.3 V
1	1.8 V

An external resistor is required.

R109 R0201 4.7K 5% SPIVCCIOSEL

+VCC_RTC — R110 R0201 1M 5% SM_INTRUDER#

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[26,34] PM_SLP_SUS# — PM_SLP_SUS# DV49 — SLP_SUS#

[26] PM_SLP_S5# — DM43 — GPD10/SLP_S5#

[26,31,35] PM_SLP_S4# — DJ41 — GPD5/SLP_S4#

[26,35,36] PM_SLP_S3# — DJ43 — GPD4/SLP_S3#

DR41 — GPD6/SLP_A#

DT42 — GPD9/SPL_WLAN#

[35] SLP_S0# — SLP_S0# DD42 — GPP_B12/SLP_S0#

DN39 — SLP_LAN#

RSMRST# DM35 — RSMRST#

PCH_SYSRST# DD10 — SYS_RESET#

PLTRST# DD41 — GPP_B13/PLTRST#

PCH_DPWROK DK35 — DSW_PWROK

[35] SYS_PWROK — SYS_PWROK DF10

[35] PCH_PWROK — PCH_PWROK DN35

SM_INTRUDER# DM37 — INTRUDER#

SPIVCCIOSEL DT49 — SPIVCCIOSEL

PROCPWRGD — BM9

GPD3/PWRBTN# — DK41 O_PWR_BTN# — O_PWR_BTN# [26]

GPD0/BATLOW# — DN41 O_BATLOW#

GPD1/ACPRESENT — DK43 AC_PRESENT

GPP_B11/PMCALERT# — CW40 PMCALERT#

GPP_H18/CPU_C10_GATE# — DN27 CPU_C10_GATE# — CPU_C10_GATE# [35]

GPP_H3/SX_EXIT_HOLDOFF# — DG31 SX_EXIT_HOLDOFF#

WAKE# — DK39 PCIE_WAKE# — PCIE_WAKE# [22,24,27]

GPD2/LAN_WAKE# — DM41 LAN_WAKE# — LAN_WAKE# [23]

GPD11/LANPHYPC/DSWLDO_MON — DT41 PM_LAN1PHY_ENABLE — PM_LAN1PHY_ENABLE [23]

GPD7 — DN43

VCCSTPWRGOOD_TCSS — CE5 VCCSTPWRGOOD

VCCST_PWRGD — BP8 VCCST_PWRGOOD — R106 R0402 60.4 1% — H_VCCST_PWRGD [35]

VCCST_OVERRIDE — BP9 VCCST_OVERRIDE

GPP_F20/EXT_PWR_GATE# — DR12 EXT_PWR_GATE#

GPP_F21/EXT_PWR_GATE2# — DW12 EXT_PWR_GATE2#

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+V3P3A

PCIE_WAKE# — R97 R0201 1K 5%

LAN_WAKE# — R98 R0201 X/10K 1%

O_BATLOW# — R99 R0402 8.2K 1%

AC_PRESENT — R100 R0201 10K 1%

O_PWR_BTN# — R101 R0402 8.2K 1%

EXT_PWR_GATE# — R102 R0201 100K 5%

EXT_PWR_GATE2# — R103 R0201 100K 5%

PMCALERT# — R104 R0201 10K 1%

SX_EXIT_HOLDOFF# — R105 R0201 10K 1%

VCCSTPWRGOOD — R107 R0201 0 5% — VCCST_OVERRIDE_R [35]

VCCST_OVERRIDE — R108 R0201 0 5%

UAL BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

+V3P3A — C8 0.1uF, 10V, C0201

+V3P3A — R347 1K 5% R0201

PLTRST# — U1 (1 NC, 2 A, 3 GND, 5 VCC, 4 Y) SN74AUP1G07DRLR — BUF_PLT_RST# [21,22,23,24]

HDMI
PCIE FPC
M.2(Key E)
M.2 M-key
LAN-I219
LAN-I211
eSPI Connector

PCIE SSD

RSMRST# Control

NOTE:
PDG PAGE422, RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band. This is true for all power states transitions including emergency power loss.

RSMRST# is power good signal of 3VSB, which is delayed 66ms as 3VSB arrives at 2.8V bY SIO.

[26] SIO_RSMRST# — R112 R0201 0 5% — SIO_RSMRST#_R

C9 X/0.1uF, 10V, C0201

[30] V3P3A_EN

[34] VCCIN_AUX_PGOOD — R113 R0201 0 5% — VCCIN_AUX_PGOOD_R

U2 (1 A, 2 GND, 3 B, 6 C, 5 VCC, 4 Y) NC7SZ11P6X

+V3P3A — C10 0.1uF, 10V, C0201

RSMRST# — R114 100K 5% R0201

From ECD HW RSMRST# design

SYSRST#

+V3P3A — R111 10K 1% R0201

PCH_SYSRST# — D2 (1, 2, 3) BAT54AW TS-SOT323

1 WDT_RST# — WDT_RST# [26]

2 HWRST# — HWRST# [29]

<Variant Name>

AAEON Technology INC.

Title: SoC System

Size: A3 | Document Number: DN-TGU8 | Rev: A0.3_0_0

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SoC Strap

CFG14	PEG* Static x4 Lane Numbering Reversal
0	Lane numbers reversed
1 *	Normal operation

The CFG signals have a default value of '1'

+VCCIO_OUT

R116	1K		CFG1
R0201	5%		
R115	1K		CFG2
R0201	5%		
R117	1K		CFG3
R0201	5%		
R118	1K		CFG9
R0201	5%		
R119	1K		CFG10
R0201	5%		
R120	1K		CFG11
R0201	5%		

CFG4	eDP Presence
0 *	ENABLE
1	DISABLE

The CFG signals have a default value of '1'

R123 1K CFG4
R0201 5%

CFG7	PEG Training
0	PEG Wait for BIOS for training
1 *	PEG Train immediately following RESET# de assertion

The CFG signals have a default value of '1'

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TP29	TP20	CFG15	T15	CFG_15	RSVD_TP_7	A51	
TP31	TP20	CFG14	V17	CFG_14	RSVD_TP_8	B51	
		CFG13	U15	CFG_13			
TP32	TP20	CFG12	K11	CFG_12	RSVD_TP_9	C1	
TP33	TP20	CFG11	K12	CFG_11	RSVD_TP_10	D2	
		CFG10	K9	CFG_10			
		CFG9	T17	CFG_9	RSVD_TP_11	CP39	
		CFG8	K7	CFG_8	RSVD_TP_12	CU40	
TP30	TP20	CFG7	H7	CFG_7	RSVD_12	AK9	
TP34	TP20	CFG6	K8	CFG_6			
TP35	TP20	CFG5	H9	CFG_5	RSVD_13	AH9	
TP36	TP20	CFG4	E6	CFG_4			
		CFG3	H5	CFG_3	RSVD_14	DW6	
		CFG2	E9	CFG_2	RSVD_15	DV6	
		CFG1	D9	CFG_1			
		CFG0	E7	CFG_0			
TP37	TP20				RSVD_TP_13	DV4	
R121	49.9ohm	CFG_RCOMP	B5	CFG_RCOMP	RSVD_TP_14	DW3	
R0201	1%						
TP38	TP20	CFG17	U17	CFG_17	RSVD_TP_15	DU1	
TP39	TP20	CFG16	H11	CFG_16	RSVD_TP_16	DT2	
TP40	TP20	BPM3	Y1	BPM#_3	RSVD_TP_17	DW2	
TP41	TP20	BPM2	M4	BPM#_2	RSVD_TP_18	DV2	
TP42	TP20	BPM1	AB4	BPM#_1	RSVD_TP_19	E1	
TP43	TP20	BPM0	Y2	BPM#_0	RSVD_TP_20	F1	
			A3	RSVD_6	RSVD_16	AB2	
			B3	RSVD_7			
R122	2.2K	TCP0_MBIAS_RCOMP	AR2	TCP0_MBIAS_RCOMP	RSVD_TP_21	DR1	
R0402	1%				RSVD_TP_22	DR2	
			AL10	RSVD_TP_2			
			AM12	RSVD_TP_3	RSVD_TP_23	DR53	
			AH12	RSVD_TP_4	RSVD_TP_24	DW5	
			AJ10	RSVD_TP_5			
			AR1	RSVD_TP_6	VSS_1	DV51	VSS_1 TP44 TP20
					TP_3	DW52	
			BN10		TP_4	DV53	
			BM12	RSVD_8	RSVD_17	W34	
			DD13	RSVD_9	RSVD_18	V35	
			DF13	RSVD_10			
				RSVD_11	SKTOCC#	D52	SKTOCC# TP45 TP20

14-CPU-SERIES-BGA1449P-0

<Variant Name>

AAEON® An ASUS Company

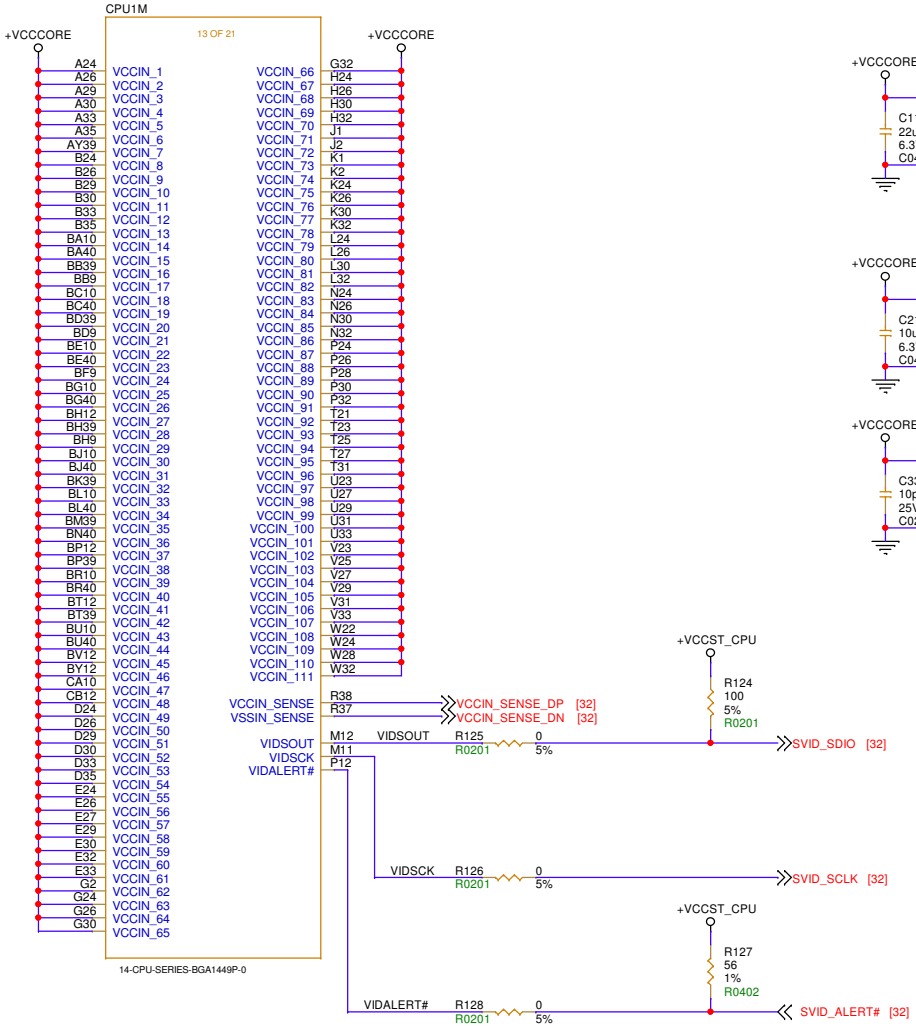
AAEON Technology INC.

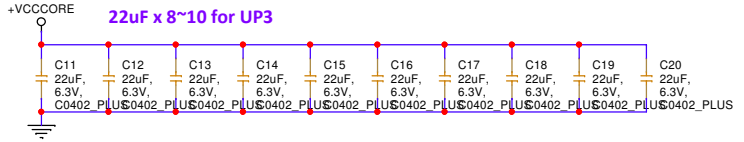
Title: SoC Strap

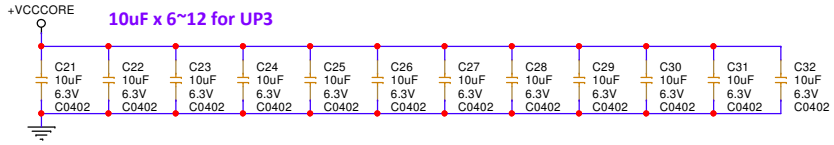
Size	Document Number	Rev
A4	DN-TGU8	A0.3_0_0

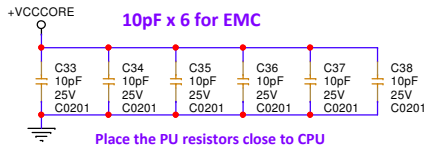
Date: Tuesday, January 04, 2022 Sheet 13 of 37

SoC Power









<variant_name>

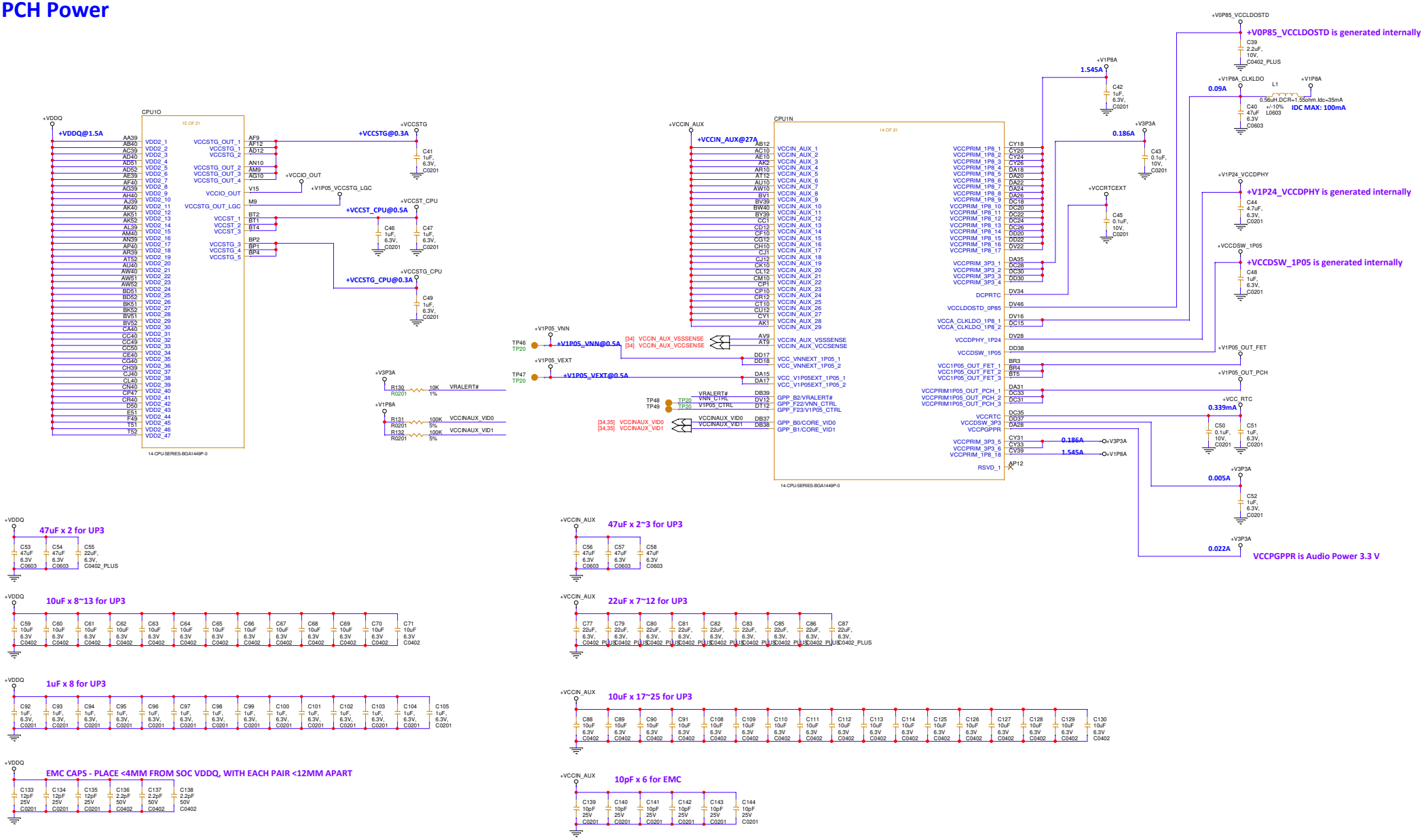
AAEON Technology INC.

Title: SoC Power

Size | Document Number: DN-TGU8 | Rev: A0.3_0_0

Date: Tuesday, January 04, 2022 | Sheet 14 of 37

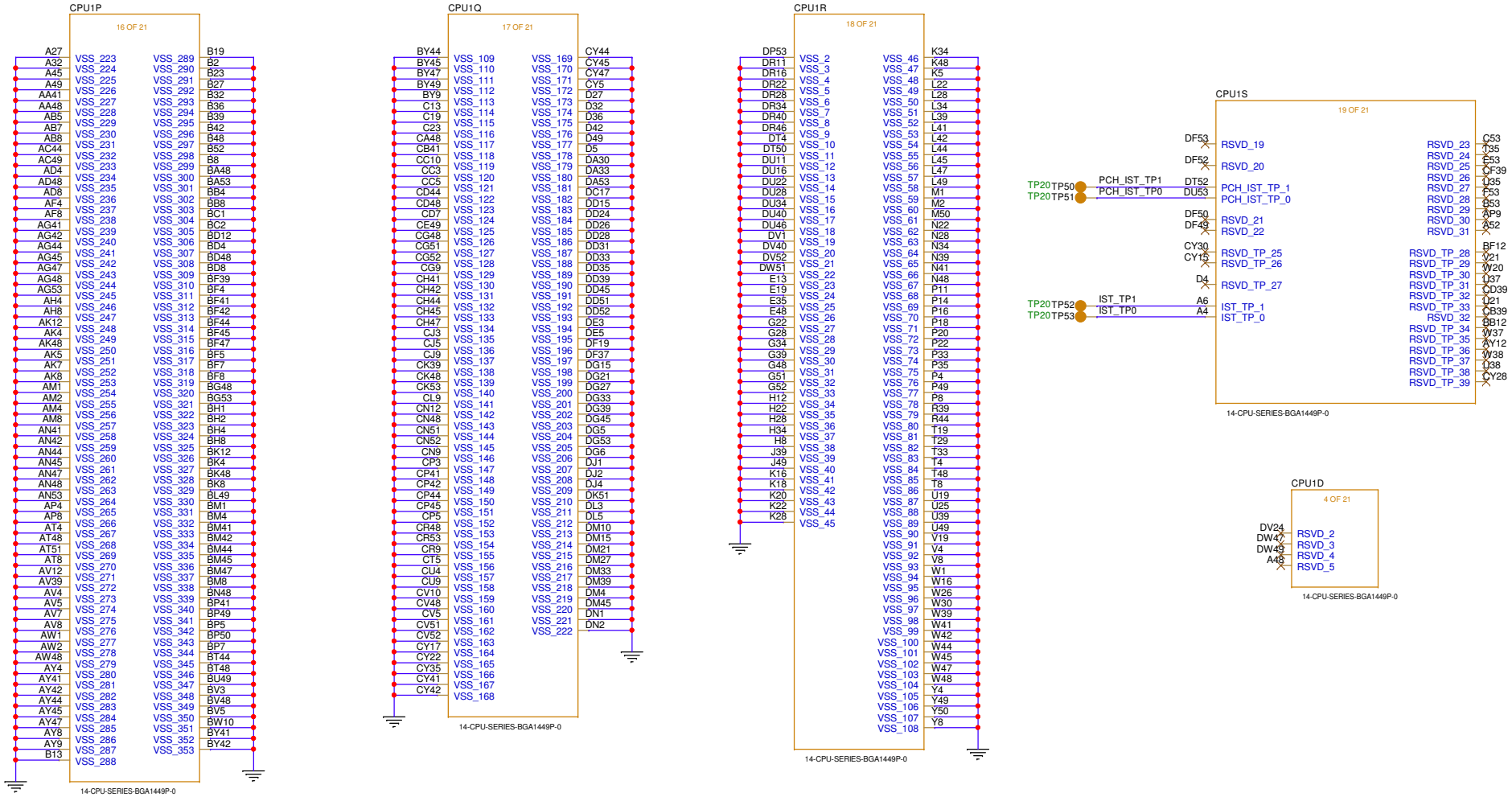
PCH Power



<variant_name>

AAEON Technology INC.			
Title: PCH Power			
Size: A2	Document Number: DN-TGU8		Rev: A0.3_0_0
Date: Tuesday, January 04, 2022	Sheet 15 of 37		

SoC GND



<Variant Name>

AAEON Technology INC.

Title	SoC GND	
Size	Document Number: DN-TGU8	Rev: A0.3_0_0
Date: Tuesday, January 04, 2022	Sheet 16 of 37	

LPDDR4x CHA

20201005 Run out of PCB space for DDR4 Memory down
Change design from DDR4 to 2*LPDDR4x

+VDDQ **1.1V**

C145 22uF, 6.3V, C0402 | C146 22uF, 6.3V, C0402 | C147 10uF 6.3V C0402 | C148 10uF 6.3V C0402 | C149 1uF, 6.3V, C0201

+VDDQ_LP4X_MEM **0.6V**

C151 22uF, 6.3V, C0402 | C152 22uF, 6.3V, C0402 | C153 10uF 6.3V C0402 | C154 10uF 6.3V C0402 | C150 1uF, 6.3V, C0201

*Layout note: Ecah 8 bits could swap

+V1.8U_MEM

C155 22uF, 6.3V, C0402 | C156 22uF, 6.3V, C0402 | C157 10uF 6.3V C0402 | C158 10uF 6.3V C0402 | C159 1uF, 6.3V, C0201

U3

[6] M_A_DQ_0_0	B2	DQ0_A
[6] M_A_DQ_0_1	C2	DQ1_A
[6] M_A_DQ_0_2	E2	DQ2_A
[6] M_A_DQ_0_3	F2	DQ3_A
[6] M_A_DQ_0_7	F4	DQ4_A
[6] M_A_DQ_0_6	E4	DQ5_A
[6] M_A_DQ_0_5	C4	DQ6_A
[6] M_A_DQ_0_4	B4	DQ7_A
[6] M_A_DQ_1_7	B11	DQ8_A
[6] M_A_DQ_1_6	C11	DQ9_A
[6] M_A_DQ_1_5	E11	DQ10_A
[6] M_A_DQ_1_4	F11	DQ11_A
[6] M_A_DQ_1_3	F9	DQ12_A
[6] M_A_DQ_1_2	E9	DQ13_A
[6] M_A_DQ_1_1	C9	DQ14_A
[6] M_A_DQ_1_0	B9	DQ15_A
[6] M_A_DQ_2_0	AA2	DQ0_B
[6] M_A_DQ_2_2	Y2	DQ1_B
[6] M_A_DQ_2_5	V2	DQ2_B
[6] M_A_DQ_2_1	U2	DQ3_B
[6] M_A_DQ_2_3	U4	DQ4_B
[6] M_A_DQ_2_7	V4	DQ5_B
[6] M_A_DQ_2_6	Y4	DQ6_B
[6] M_A_DQ_2_4	AA4	DQ7_B
[6] M_A_DQ_3_7	AA11	DQ8_B
[6] M_A_DQ_3_6	Y11	DQ9_B
[6] M_A_DQ_3_5	V11	DQ10_B
[6] M_A_DQ_3_4	U11	DQ11_B
[6] M_A_DQ_3_3	U9	DQ12_B
[6] M_A_DQ_3_2	V9	DQ13_B
[6] M_A_DQ_3_1	Y9	DQ14_B
[6] M_A_DQ_3_0	AA9	DQ15_B
[6] M_A_DQS_0_DP	D3	DQS0_t_A
[6] M_A_DQS_0_DN	E3	DQS0_c_A
[6] M_A_DQS_1_DP	D10	DQS1_t_A
[6] M_A_DQS_1_DN	E10	DQS1_c_A
[6] M_A_DQS_2_DP	W3	DQS0_t_B
[6] M_A_DQS_2_DN	V3	DQS0_c_B
[6] M_A_DQS_3_DP	W10	DQS1_t_B
[6] M_A_DQS_3_DN	V10	DQS1_c_B
DDR4_DRAMRST_R_N	T11	RESET_n

CA0_A	H2	M_A_LP4_0CA0 [6]
CA1_A	J2	M_A_LP4_0CA1 [6]
CA2_A	H9	M_A_LP4_0CA2 [6]
CA3_A	H10	M_A_LP4_0CA3 [6]
CA4_A	H11	M_A_LP4_0CA4 [6]
CA5_A	J11	M_A_LP4_0CA5 [6]
CA0_B	R2	M_A_LP4_1CA0 [6]
CA1_B	P2	M_A_LP4_1CA1 [6]
CA2_B	R9	M_A_LP4_1CA2 [6]
CA3_B	R10	M_A_LP4_1CA3 [6]
CA4_B	R11	M_A_LP4_1CA4 [6]
CA5_B	P11	M_A_LP4_1CA5 [6]
CK_t_A	J8	M_A_LP4_CLK0_DP [6]
CK_c_A	J9	M_A_LP4_CLK0_DN [6]
CK_t_B	P8	M_A_LP4_CLK1_DP [6]
CK_c_B	P9	M_A_LP4_CLK1_DN [6]
DMI0_A	C3	
DMI1_A	C10	
DMI0_B	Y3	
DMI1_B	Y10	
CS0_A	H4	M_A_LP4_0CS0 [6]
CS1_A	H3	M_A_LP4_0CS1 [6]
CS2_A	K5	
CS0_B	R4	M_A_LP4_1CS0 [6]
CS1_B	R3	M_A_LP4_1CS1 [6]
CS2_B	N5	
CKE0_A	J4	M_A_LP4_0CKE0 [6]
CKE1_A	J5	M_A_LP4_0CKE1 [6]
CKE2_A	K8	
CKE0_B	P4	M_A_LP4_1CKE0 [6]
CKE1_B	P5	M_A_LP4_1CKE1 [6]
CKE2_B	N8	
ZQ0	A5	ZQ0_CHA_0 R133 240 1% R0201
ZQ1	A8	ZQ1_CHA_0 R134 240 1% R0201
ZQ2	G11	
ODT_CA_A	G2	ODT_A_CHA_0 R135 0 5% R0201
ODT_CA_B	T2	ODT_B_CHA_0 R136 0 5% R0201
DNU1	A1	
DNU2	A2	
DNU3	A11	
DNU4	A12	
DNU5	B1	
DNU6	B12	
DNU7	AA1	
DNU8	AA12	
DNU9	AB1	
DNU10	AB2	
DNU11	AB11	
DNU12	AB12	

+VDDQ_LP4X_MEM

+VDDQ

200P,MT53E2G32D4DT-046 WT:A,

+VDDQ

*Layout note: CPU->CA_VREF Circuit-->DRAM0-->DRAM1

R137 470 1% R0402

[6] DRAM_RESET_N >> R138 0 5% R0201 >> DDR4_DRAMRST_R_N >> DDR4_DRAMRST_R_N [18]

C160 X/0.1uF, 10V, C0201

+VDDQ

C161 1uF, 6.3V, C0201 | C162 1uF, 6.3V, C0201 | C163 1uF, 6.3V, C0201 | C164 1uF, 6.3V, C0201 | C165 1uF, 6.3V, C0201

1uF x 6 for UP3
10uF x 2 for UP3

+VDDQ_LP4X_MEM

C166 1uF, 6.3V, C0201 | C167 1uF, 6.3V, C0201 | C168 1uF, 6.3V, C0201 | C169 1uF, 6.3V, C0201 | C170 1uF, 6.3V, C0201

1uF x 6 for UP3
10uF x 2 for UP3

+V1.8U_MEM

C171 1uF, 6.3V, C0201 | C172 1uF, 6.3V, C0201 | C173 1uF, 6.3V, C0201

1uF x 4 for UP3
10uF x 2 for UP3

<Core Design>

AAEON Technology INC.

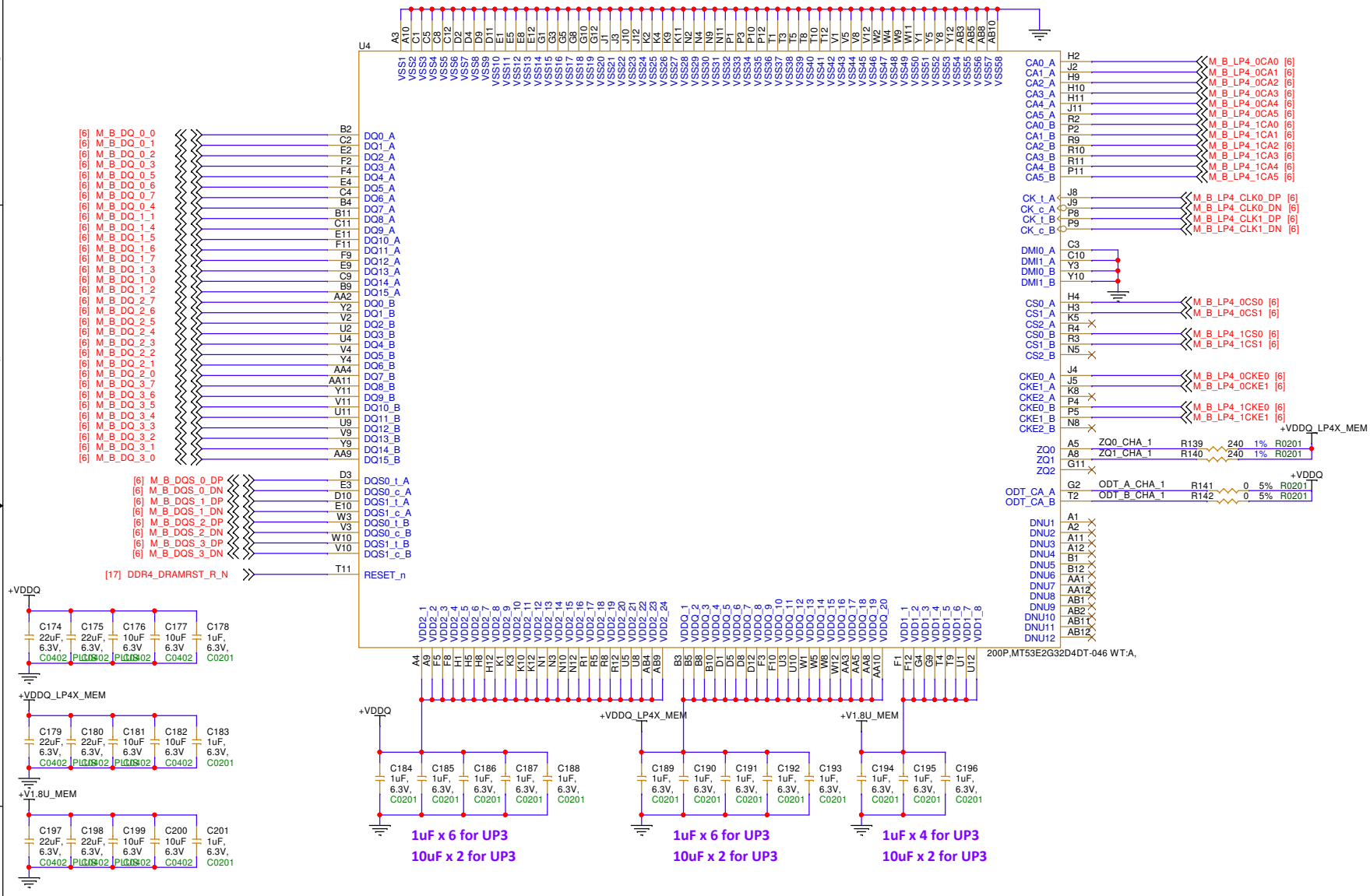
Title: LPDDR4x (1/2)

Size: A3 | Document Number: DN-TGU8 | Rev: A0.3_0_0

Date: Tuesday, January 04, 2022 | Sheet 17 of 37

LPDDR4x CHB

20201005 Run out of PCB space for DDR4 Memory down
Change design from DDR4 to 2*LPDDR4x

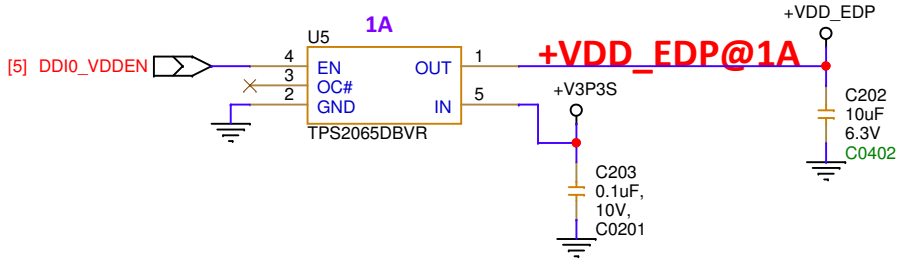


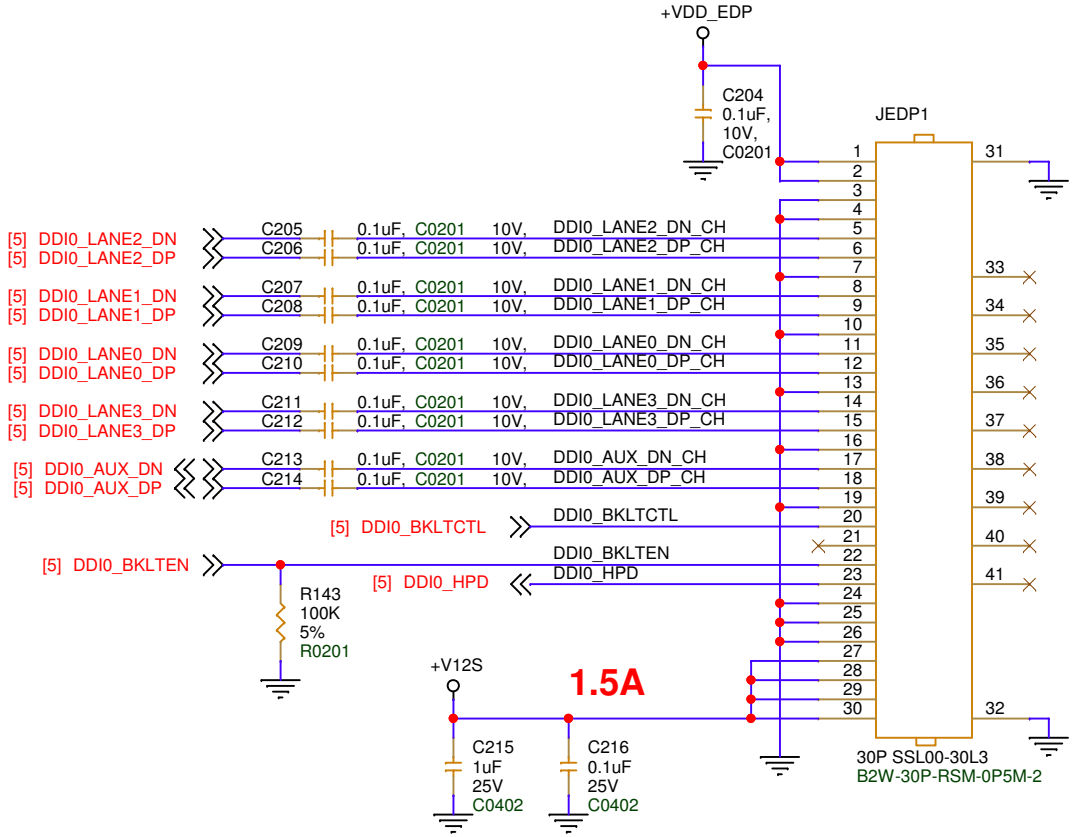
<Core Design>

AAEON Technology INC.			
Title: LPDDR4x (2/2)			
Size: A3	Document Number: DN-TGU8		Rev: A0.3_0_0
Date: Tuesday, January 04, 2022	Sheet 18 of 37		

eDP

+VDD_EDP@1A

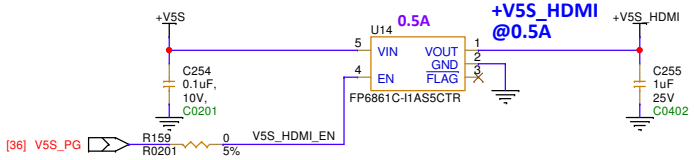




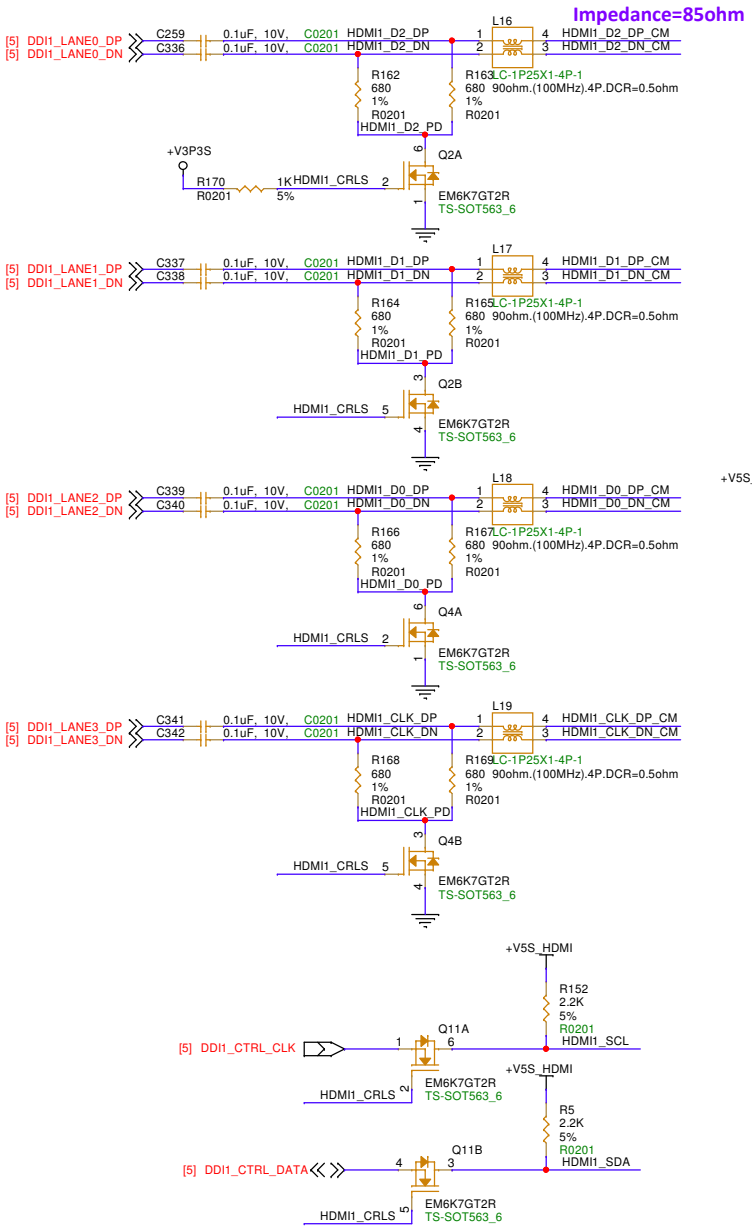
<Core Design>

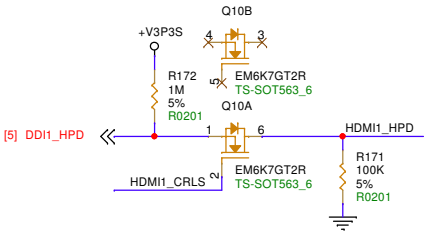
AAEON An ASUS Company	AAEON Technology INC.		
	Title: eDP		
	Size: A4	Document Number: DN-TGU8	Rev: A0.3_0_0
	Date: Tuesday, January 04, 2022	Sheet 19 of 37	

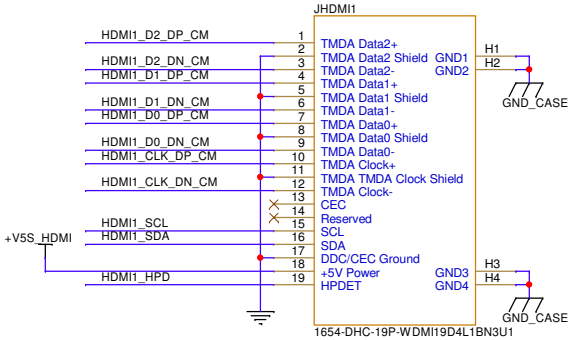
DDI1 to HDMI1

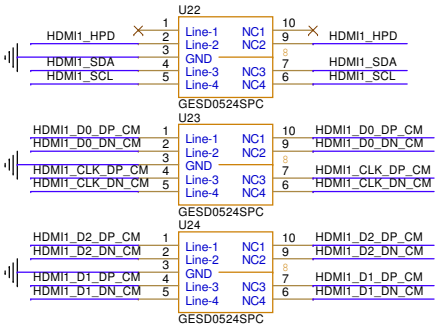


20210106, A01, Add V5S_PG for HW suggestion.







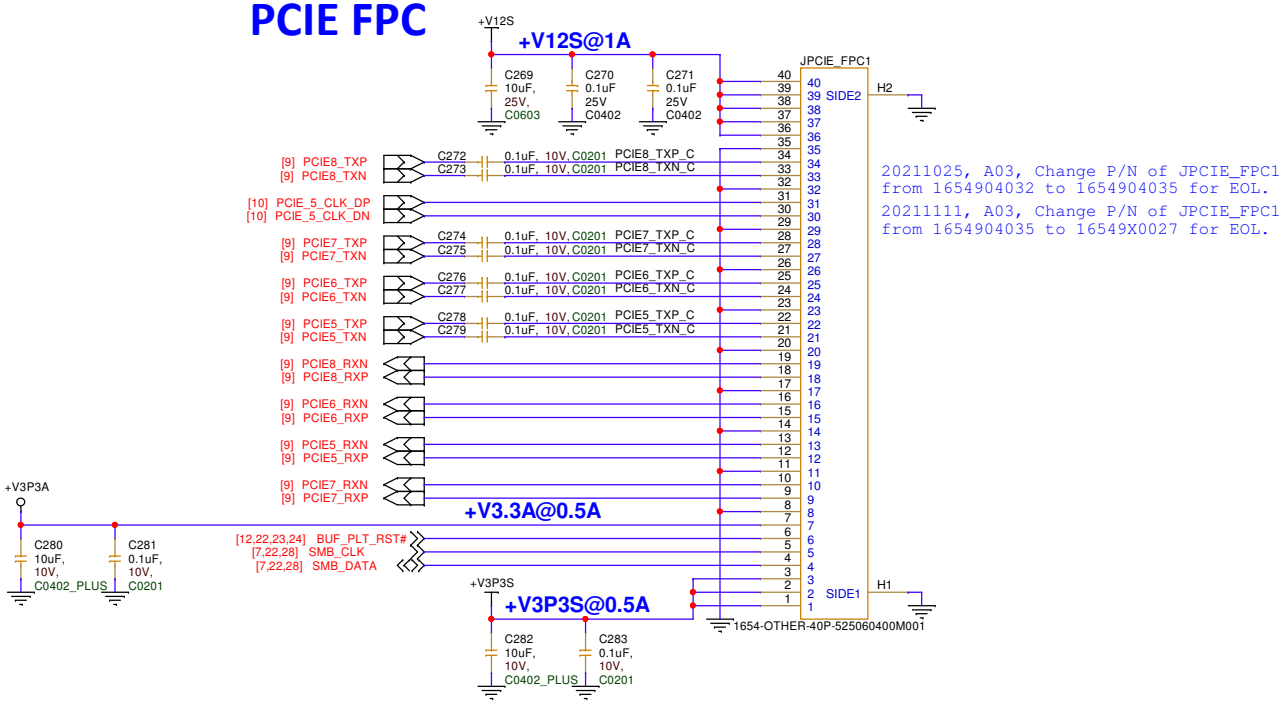


20211111, A03, U22~U24 EOL, Change P/N from 130505ESD0 to 1305Q00022

<Core Design>

AAEON An ASUS Company	AAEON Technology INC.		
	Title: HDMI		
	Size: A3	Document Number: DN-TGU8	Rev: A0.3_0_0
	Date: Tuesday, January 04, 2022	Sheet 20 of 37	

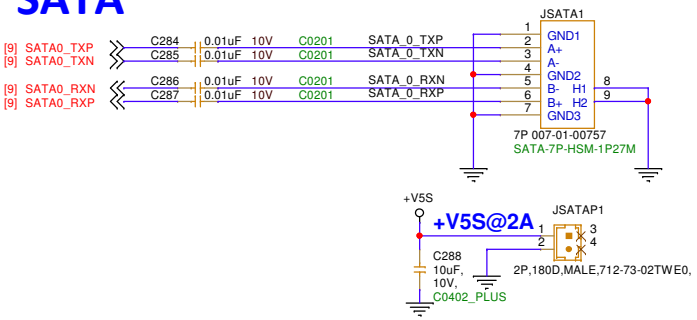
PCIE FPC



20211025, A03, Change P/N of JPCIE_FPC1 from 1654904032 to 1654904035 for EOL.

20211111, A03, Change P/N of JPCIE_FPC1 from 1654904035 to 16549X0027 for EOL.

SATA

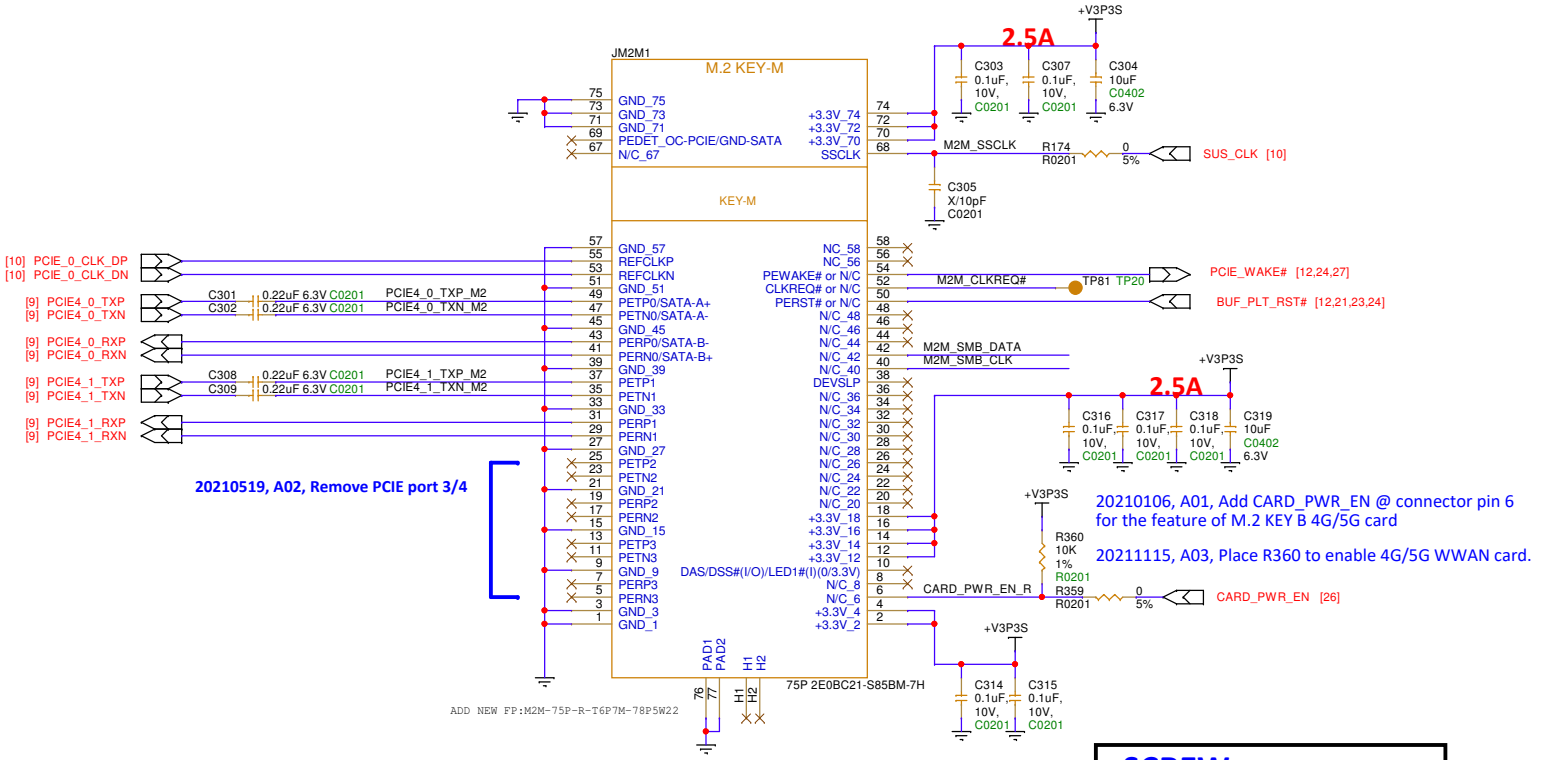


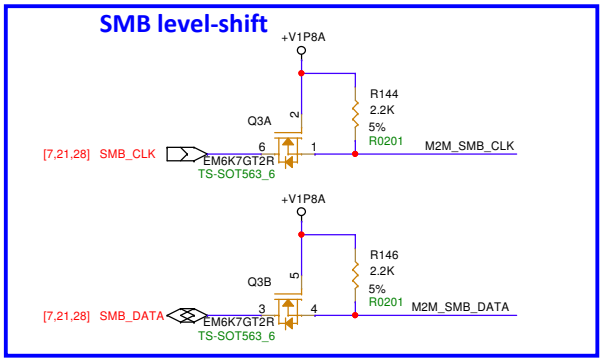
<Variant Name>

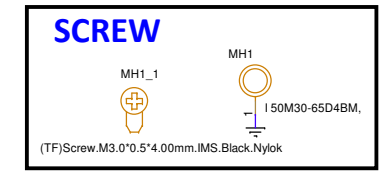
AAEON An ASUS Company

Title: PCIE FPC/SATA		
Size: A3	Document Number: DN-TGU8	Rev: A0.3_0_0
Date: *Tuesday, January 04, 2022*	Sheet: 21 of 37	

M.2 M-key 2280 SSD







<Core Design>

AAEON Technology INC.			
Title: M.2(Key B)			
Size: A3	Document Number: DN-TGU8		Rev: A0.3_0_0
Date: Tuesday, January 04, 2022	Sheet 22 of 37		

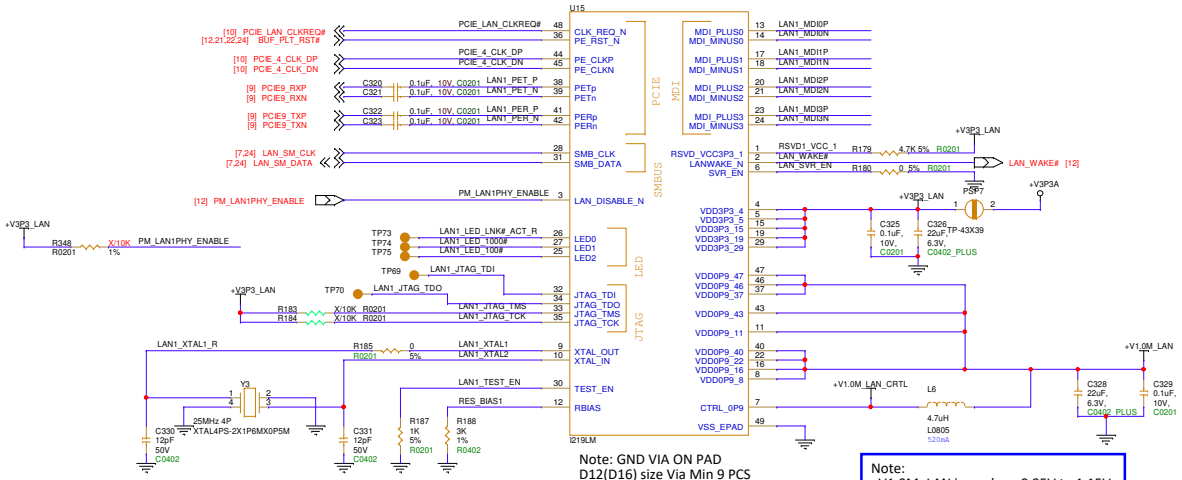
LAN-I219

ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY

SPEED LED
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps

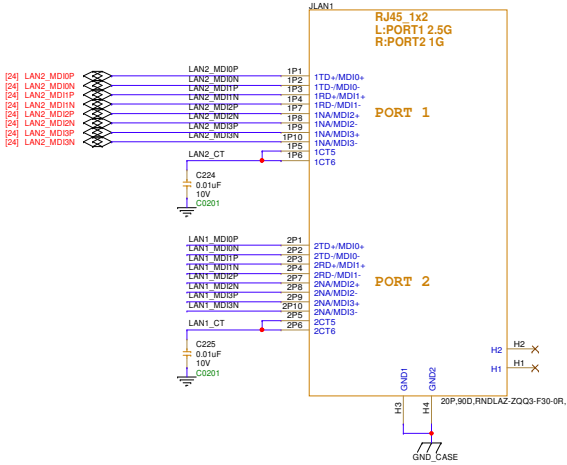
LEDs	Mode	Function
LED0	0100	LINK/ACTIVITY
LED1	0111	LINK 1000
LED2	0110	LINK 100

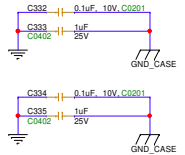
SMBus Device Addresses
0xC8



Note: GND VIA ON PAD
D12(D16) size Via Min 9 PCS

Note:
+V1.0M_LAN is work on 0.95V to 1.15V





20211103, A03,
1. Change P/N of Y3 from 12310025A5 to 12310025AE
2. Change value of C330 and C331 from 15pF to 12pF, by FAE test result.

20211220, A03, Change P/N of Y3 from 12310025AE to 12310025A5 by buyer Tina issue.

<Variant Name>

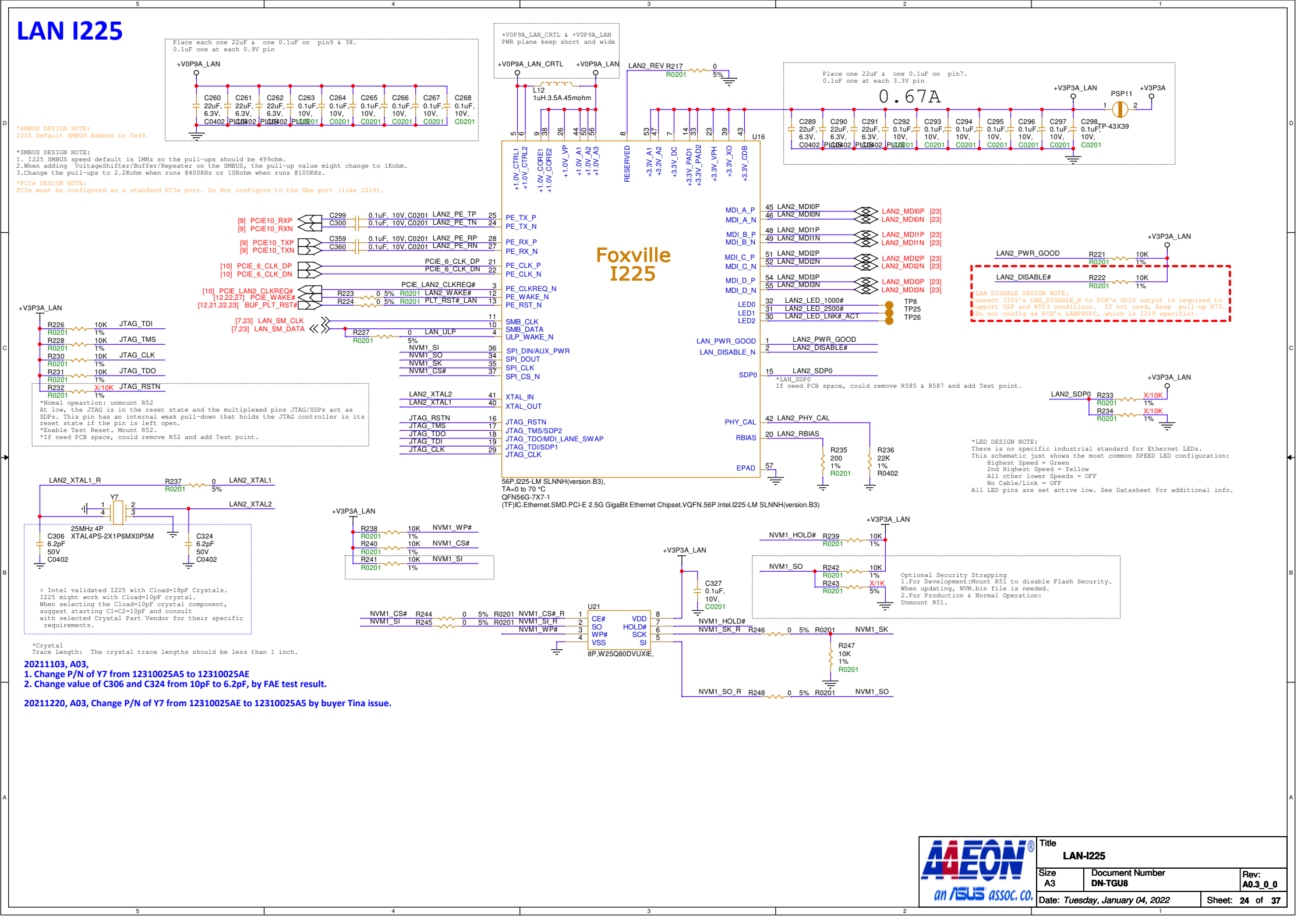
AAEON Technology INC.

Title: LAN-I219

Size: A2 | Document Number: DN-TGU8 | Rev: A0.3_0_0

Date: Tuesday, January 04, 2022 | Sheet 23 of 37

LAN I225

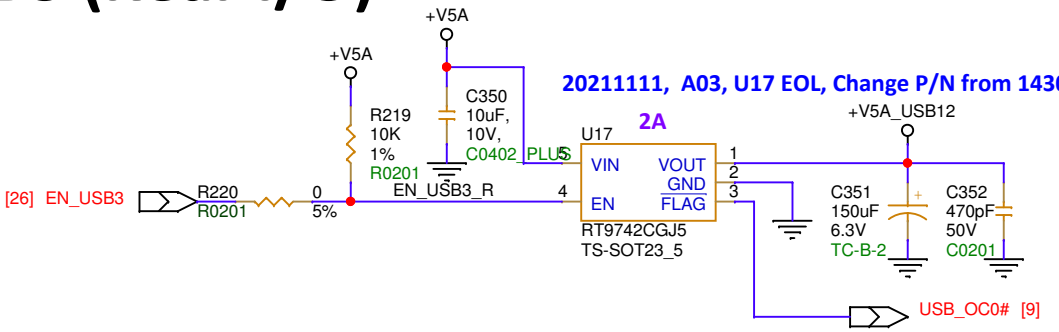


20211103, A03,
1. Change P/N of Y7 from 12310025A5 to 12310025AE
2. Change value of C306 and C324 from 10pF to 6.2pF, by FAE test result.

20211220, A03, Change P/N of Y7 from 12310025AE to 12310025A5 by buyer Tina issue.

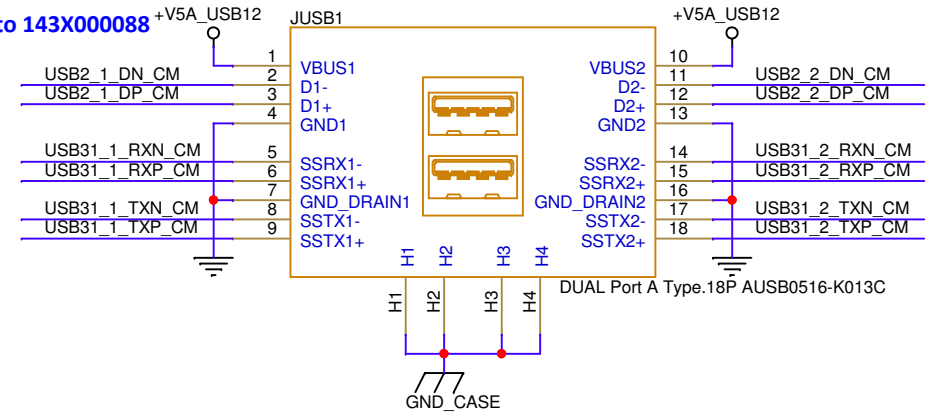
AAEON an ASUS assoc. co.	Title: LAN-I225	
	Size: A3	Document Number: DN-TGU8
	Rev: A0.3_0_0	
	Date: Tuesday, January 04, 2022	Sheet: 24 of 37

USB3 (Rear I/O)



USB3 *2(Rear I/O)

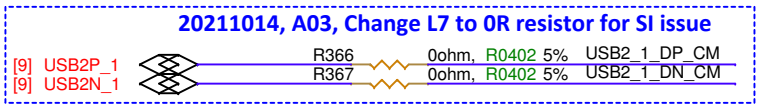
USB3.1 GEN2

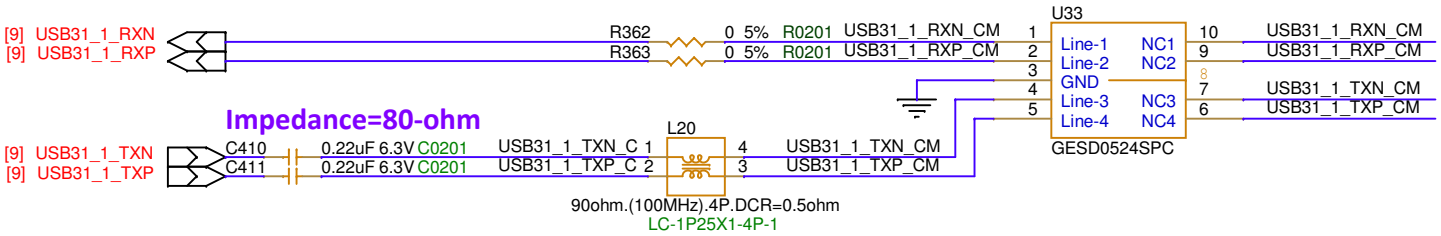


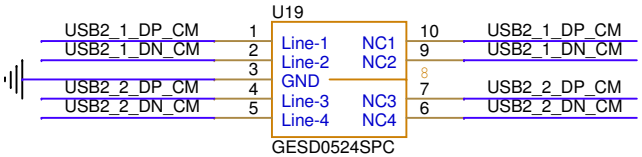
USB3 PORT 1

20210519, A02, Change USB3 port1/2 to PCH HSIO port 3/4

20211014, A03, Change L7 to 0R resistor for SI issue





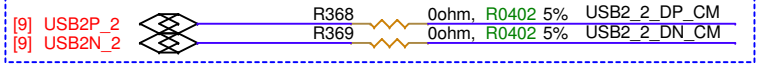


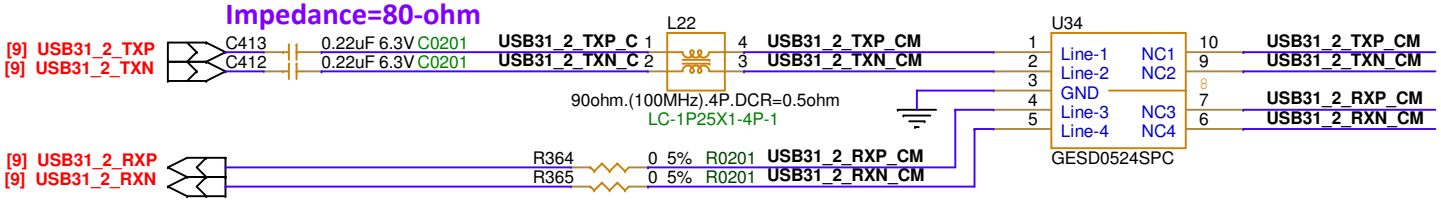
20210601, A02, Change P/N of U19, U33, U34 from 130505ESD0 to 13055V0SP0 for EOL

20211111, A03, U19, U33, U34 EOL, Change P/N from 13055V0SP0 to 1305Q00022

USB3 PORT 2

20211014, A03, Change L9 to 0R resistor for SI issue





<Core Design>

AAEON Technology INC.

Title: USB3.1

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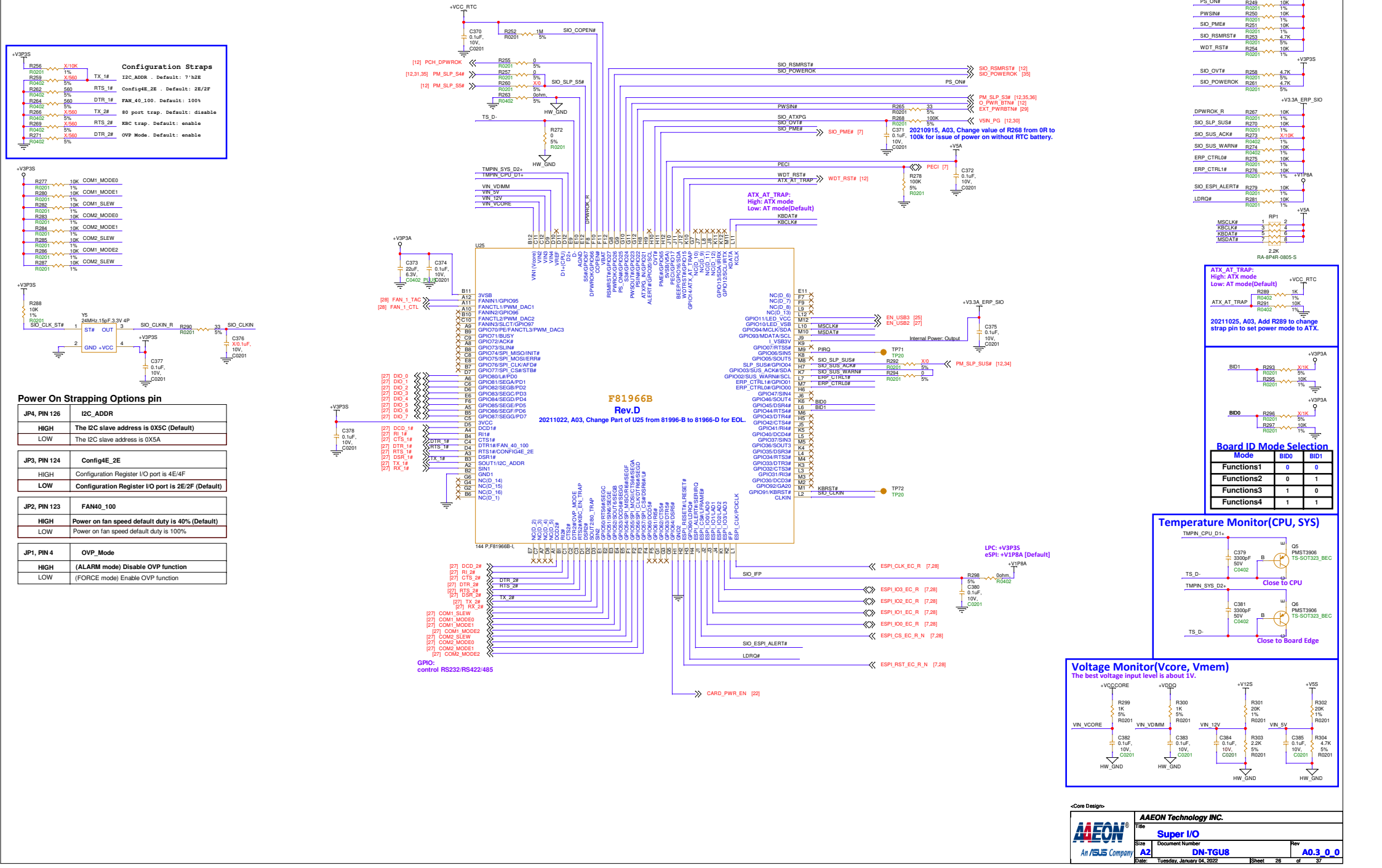
Super I/O F81966



Power On Strapping Options pin

JP4, PIN 126	I2C_ADDR
HIGH	The I2C slave address is 0X5C (Default)
LOW	The I2C slave address is 0X5A

JP3, PIN 124	Config4E_2E
HIGH	Configuration Register I/O port is 4E/4F
LOW	Configuration Register I/O port is 2E/2F (Default)

JP2, PIN 123	FAN40_100
HIGH	Power on fan speed default duty is 40% (Default)
LOW	Power on fan speed default duty is 100%

JP1, PIN 4	OVP_Mode
HIGH	(ALARM mode) Disable OVP function
LOW	(FORCE mode) Enable OVP function

Mode	BID0	BID1
Functions1	0	0
Functions2	0	1
Functions3	1	0
Functions4	1	1

<Core Design>
AAEON Technology INC.
An /SUS Company

Title	Super I/O	
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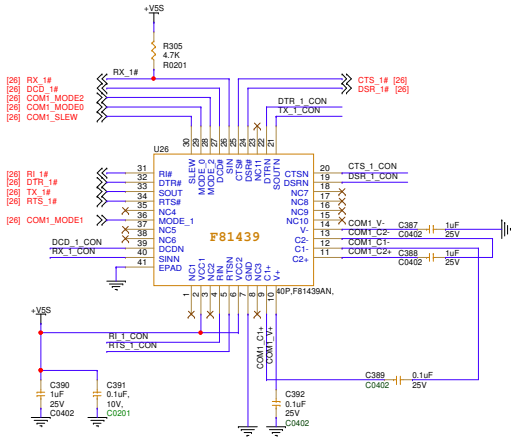
COM1-RS232/RS422/RS485 F81439 is for RS232/422/485



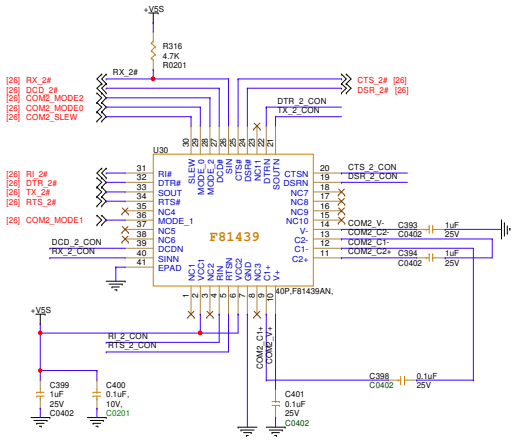
Maximum Data Rate

SLEW	RS233	RS422/RS485
1	250kbps	250kbps
0	1Mbps	10Mbps

Serial Port 1 Mode Selection

Mode	MODE_0	MODE_1	MODE_2
RS-422	0	0	0
RS-232	0	0	1
RS-485 (Driver Half Duplex)	0	1	0
RS-485 (Receiver Half Duplex)	0	1	1
Shutdown MODE	1	X	X

COM2-RS232/RS422/RS485



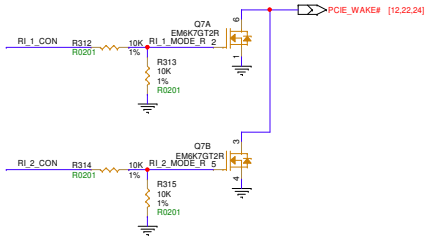
Maximum Data Rate

SLEW	RS233	RS422/RS485
1	250kbps	250kbps
0	1Mbps	10Mbps

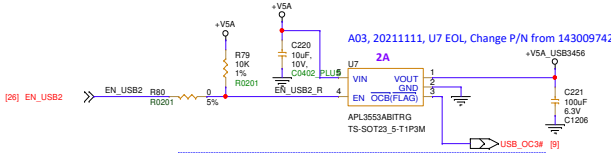
Serial Port 1 Mode Selection

Mode	MODE_0	MODE_1	MODE_2
RS-422	0	0	0
RS-232	0	0	1
RS-485 (Driver Half Duplex)	0	1	0
RS-485 (Receiver Half Duplex)	0	1	1
Shutdown MODE	1	X	X

Wake on Modem

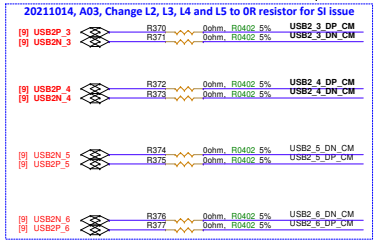


USB2.0 *4 (Pin Header)

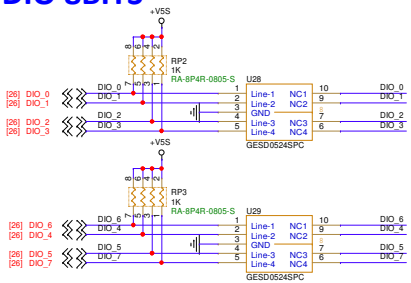


A03, 20211111, U7 EOL, Change P/N from 1430097420 to 143X000115

20211014, A03, Change L2, L3, L4 and L5 to 0R resistor for SI issue



DIO 8BITS



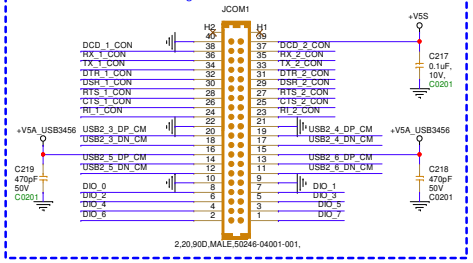
A02, 20210601, Change P/N of U28, U29 from 130505ESD0 to 13055V0SP0 for EOL

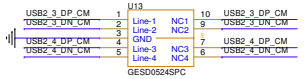
20211111, A03, U28, U29 EOL, Change P/N from 13055V0SP0 to 1305Q00022

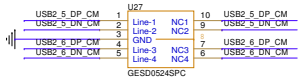
COM Port pin mapping

PIN		RS422	RS485	DB-9 Con.
7	DCD1	TX1-	DATA1-	COM1_1
9	RX1	TX1+	DATA1+	COM1_2
11	TX1	RX1+		COM1_3
13	DTR1	RX1-		COM1_4
15	DSR1			COM1_6
17	RTS1			COM1_7
19	CTS1			COM1_8
21	RI1			COM1_9
8	DCD2	TX2-	DATA2-	COM2_1
10	RX2	TX2+	DATA2+	COM2_2
12	TX2	RX2+		COM2_3
14	DTR2	RX2-		COM2_4
16	DSR2			COM2_6
18	RTS2			COM2_7
20	CTS2			COM2_8
22	RI2			COM2_9

A02, 20210528, Change P/N of JCOM1 from 16535X0003 to 16535X0019 for change connector from 180D to 90D







A02, 20210601, Change P/N of U13, U27 from 130505ESD0 to 13055V0SP0 for EOL

20211111, A03, U13, U27 EOL, Change P/N from 13055V0SP0 to 1305Q00022

<Core Design>

AAEON Technology INC.

Title: RS232_422_485/DIO/USB2.0

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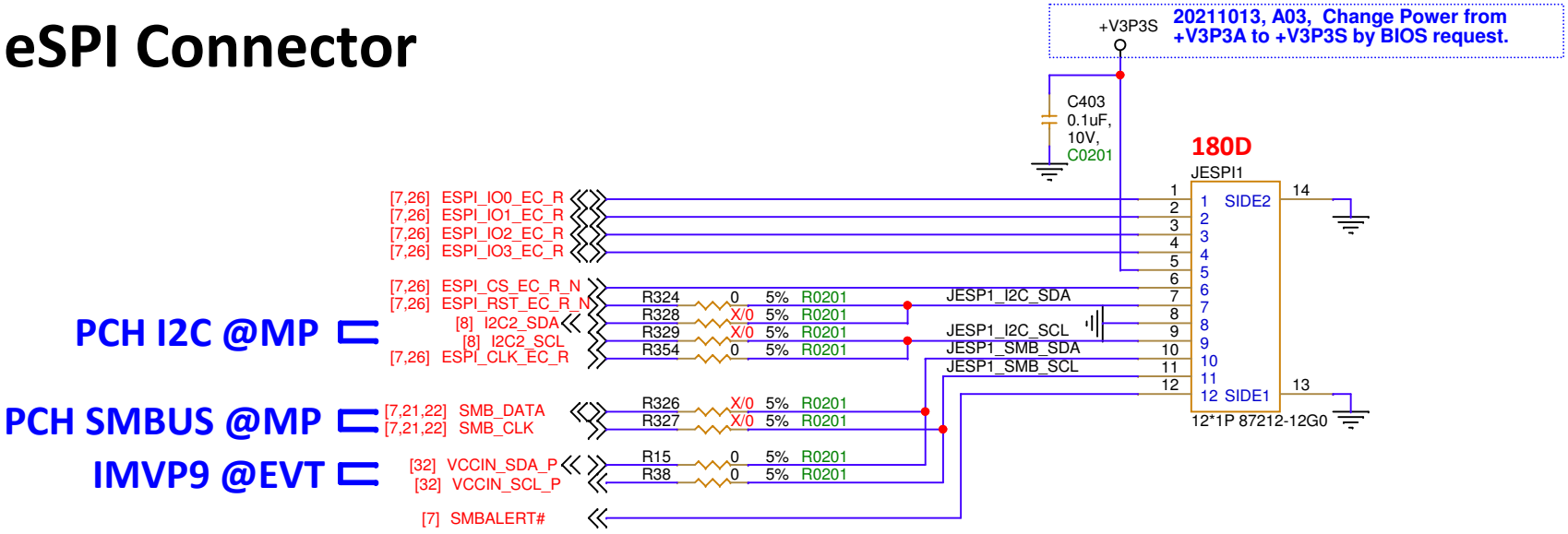
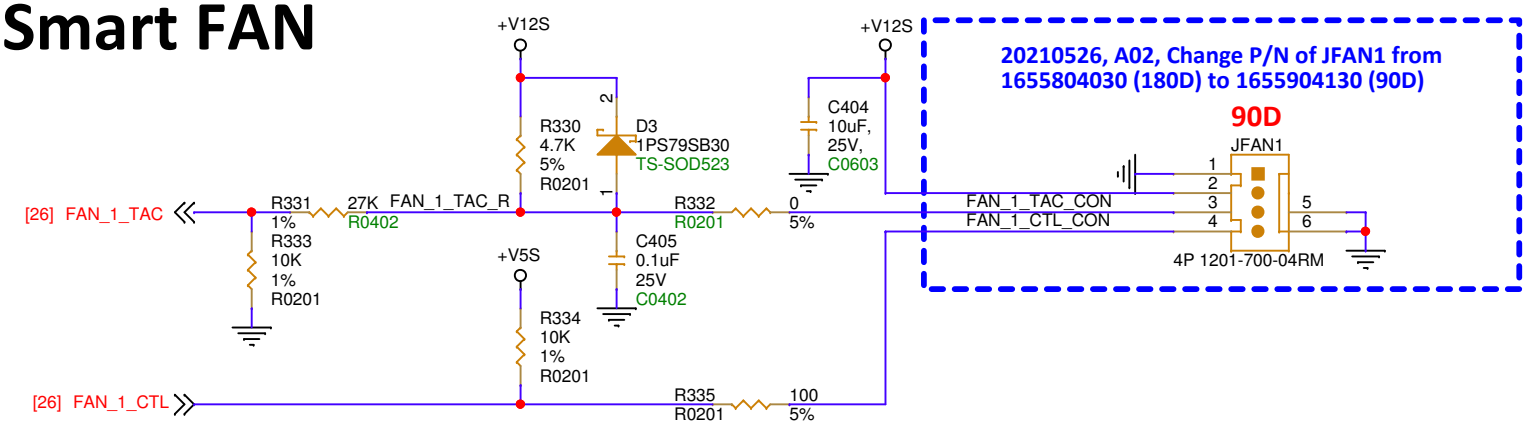
eSPI Connector

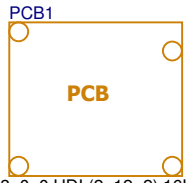


Smart FAN



PCB

20210520, A02, Update P/N of PCB1 from 1907TGU800 to 1907TGU801



PCB.DN-TGU8.Rev.A0.3_0_0.HDI.(2+12+2).16Layers.Matt Black.1*2.84*55*2.0mm

<Core Design>

AAEON Technology INC.

Title: SMBus/I2C/FAN

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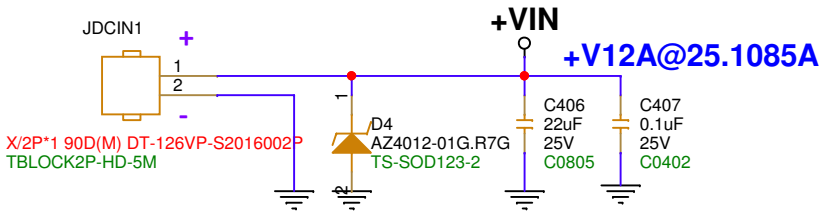
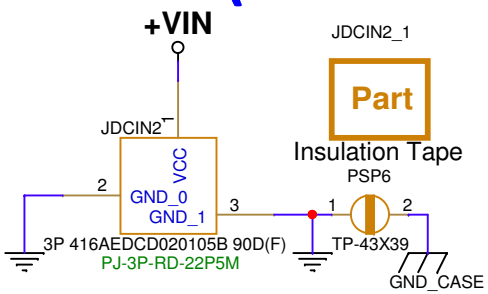
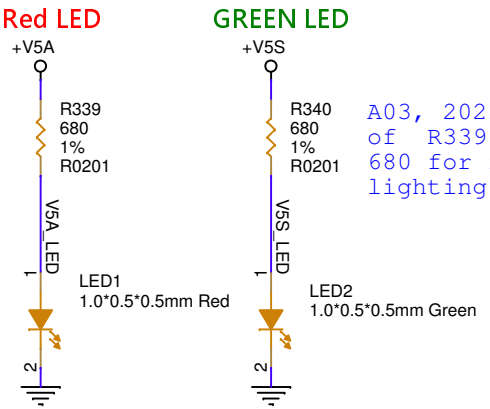
Power Input 12V



DC Jack (JDCIN2 Colay JDCIN1)

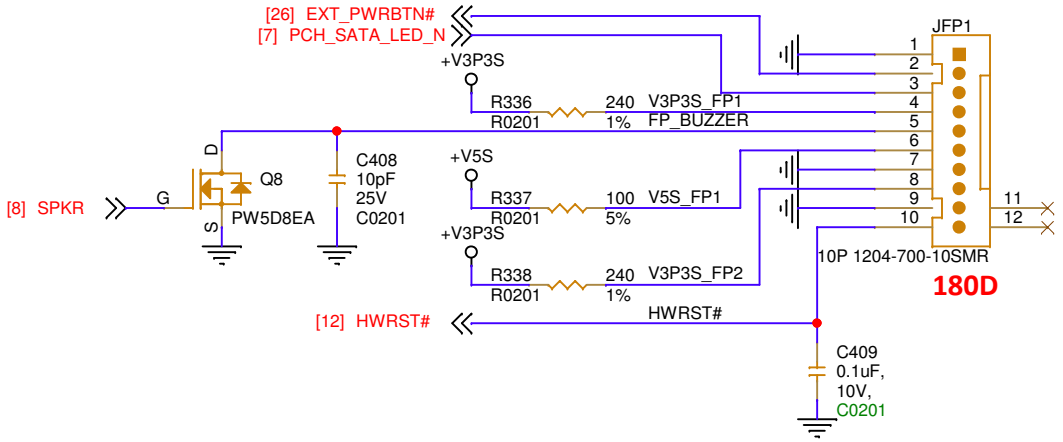


LED

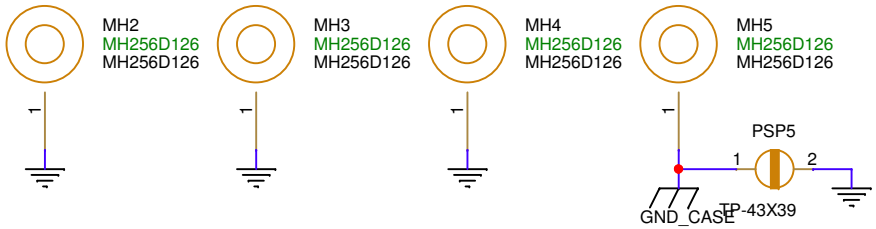


A03, 20210910, Change values of R339 and R340 from 240 to 680 for find tune the LED lighting.

Front Panel



Mounting Holes / Non-PTH



<Core Design>

AAEON Technology INC.

Title	DC IN/MISC	
Size: A4	Document Number: DN-TGU8	Rev: A0.3_0_0
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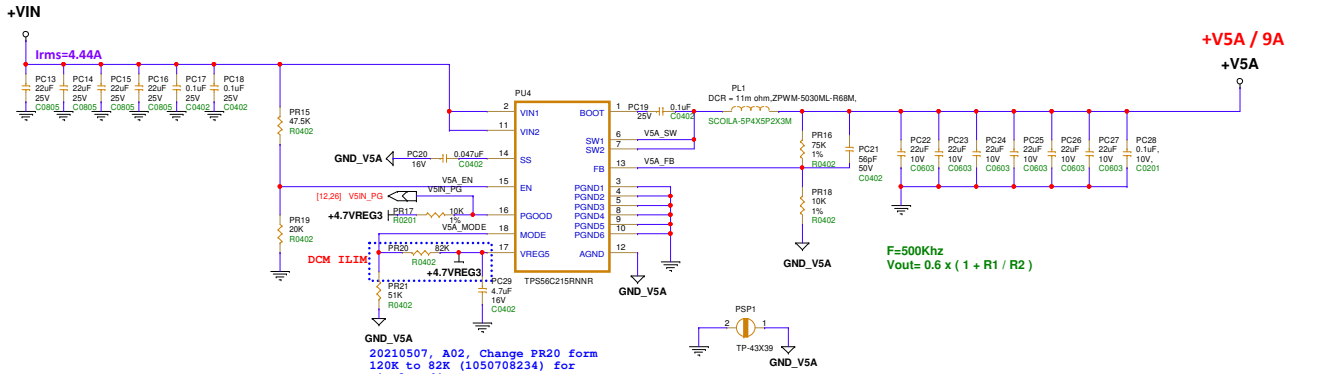
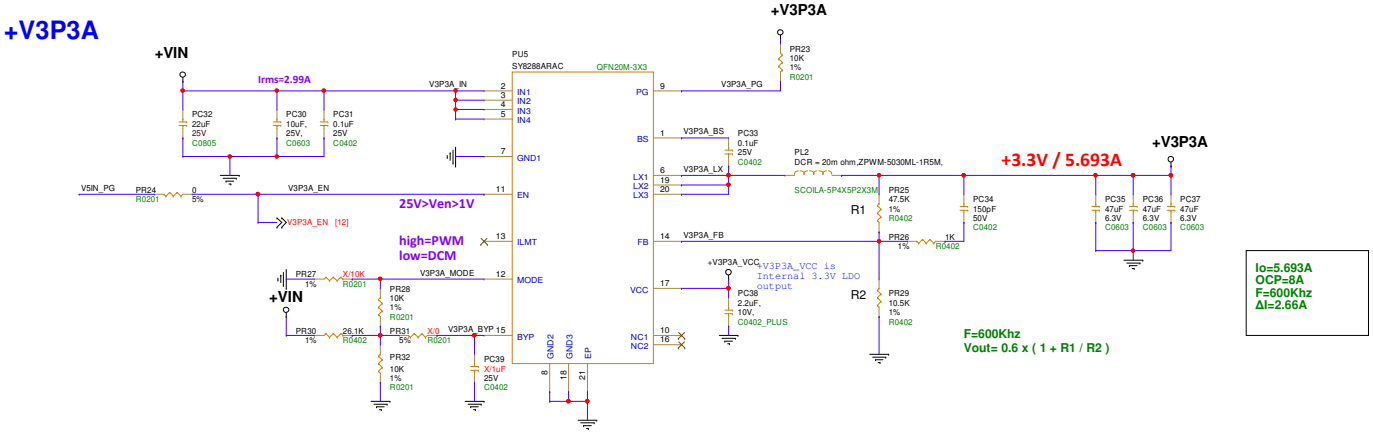
+V5A



+V3P3A



<Variant Name>

AAEON An ASUS Company

Title: POWER_+V5S_+V3P3A		
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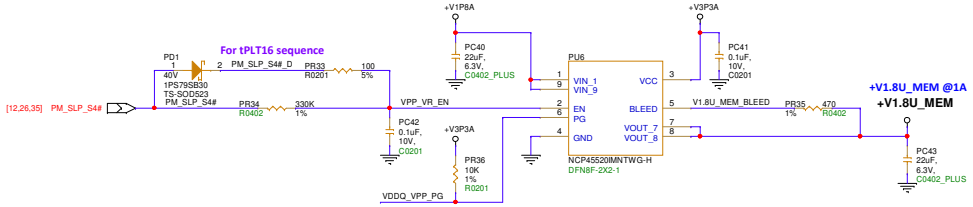
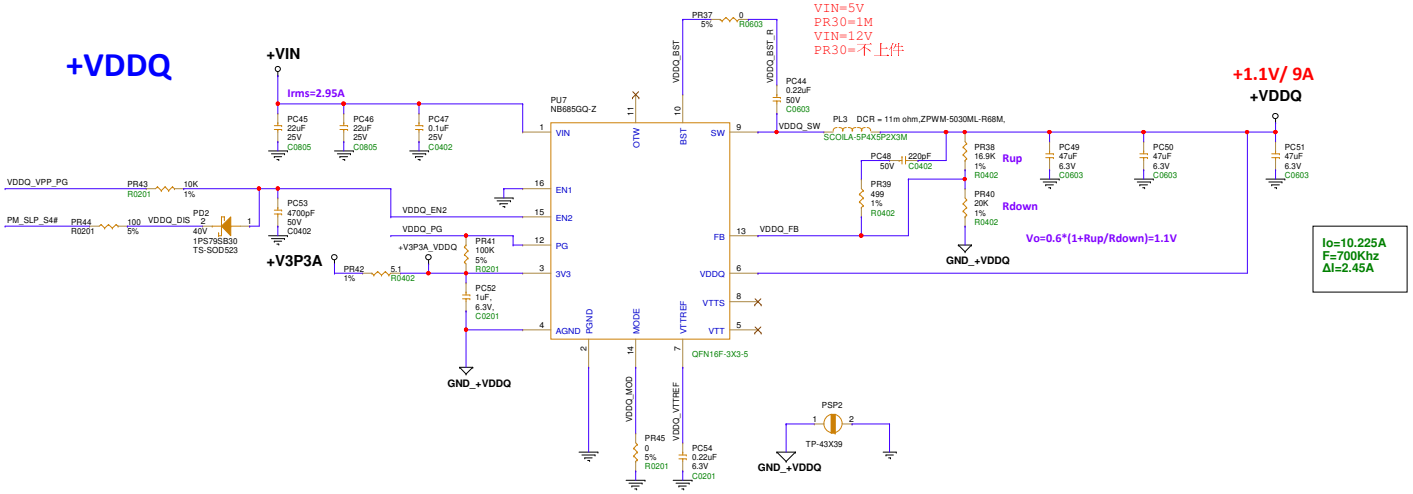
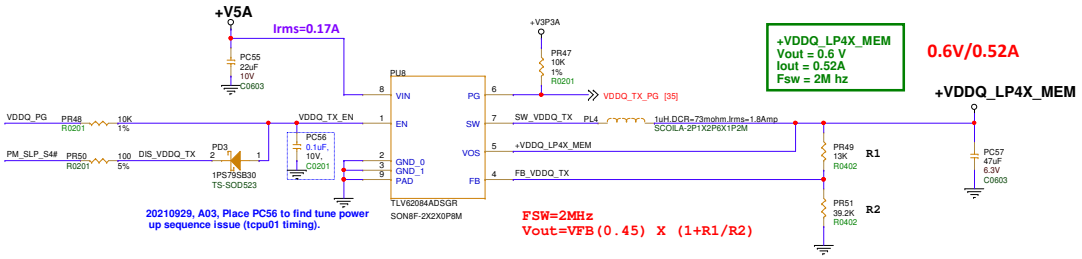
+V1.8U_MEM



+VDDQ



+VDDQ_LP4X_MEM



<Variant Name>

AAEON Technology INC.

Title	PWR_+VDDQ/ +VDDQ_VPP/ +V1P8A	
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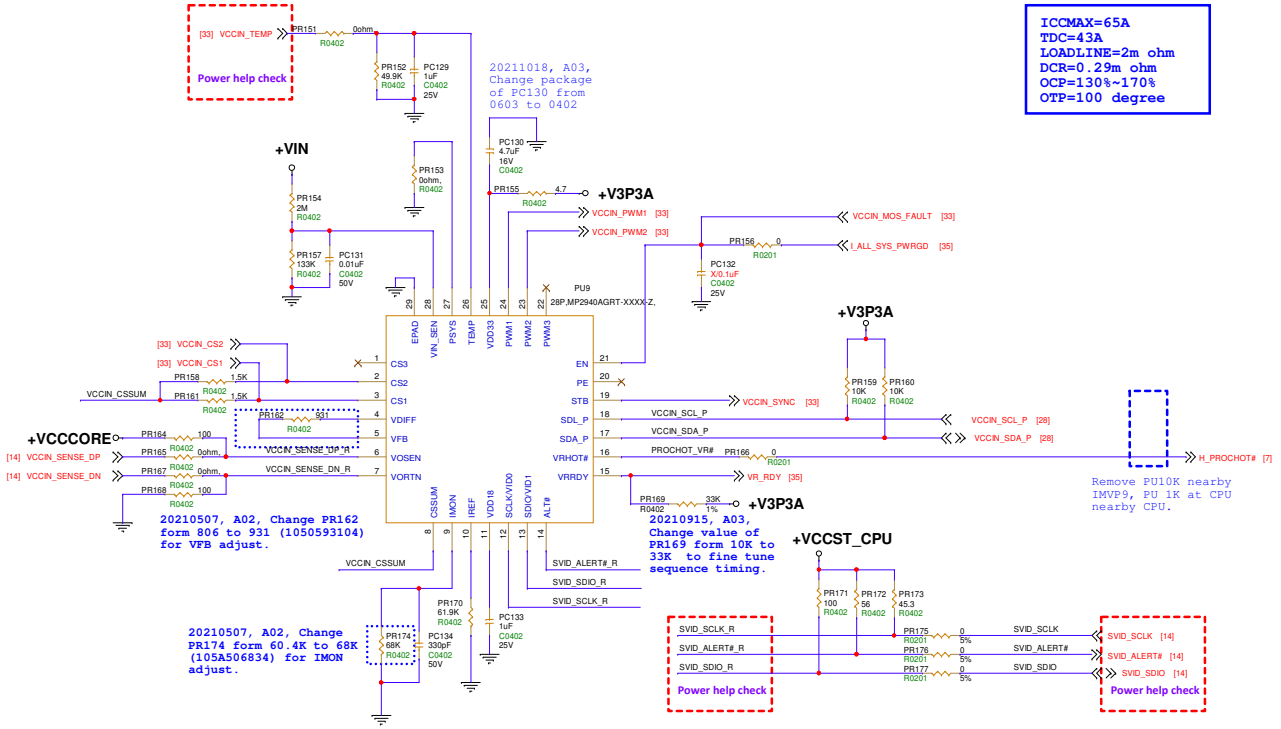
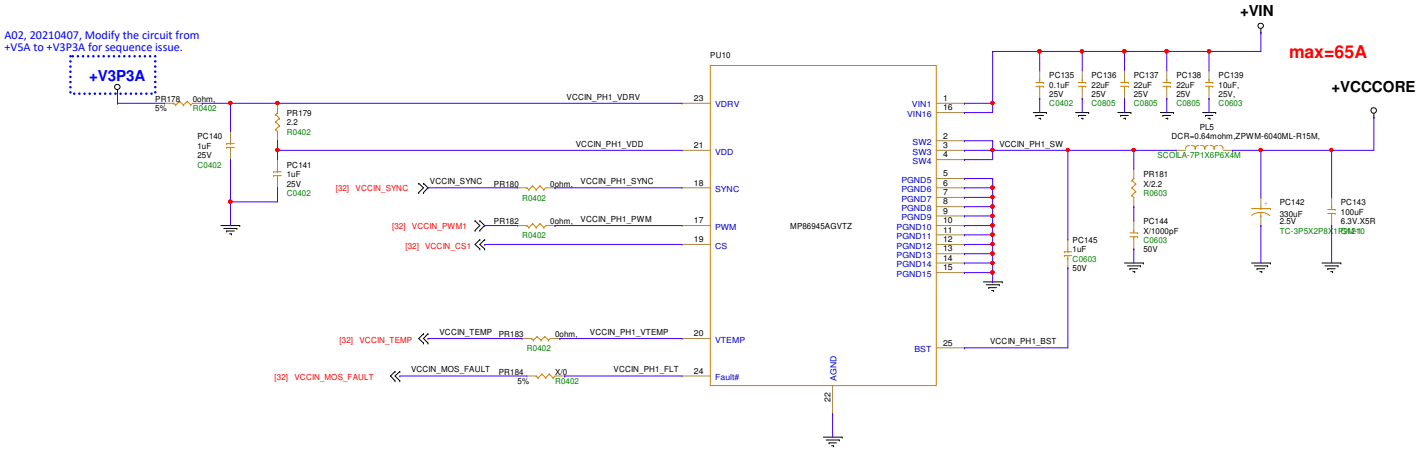
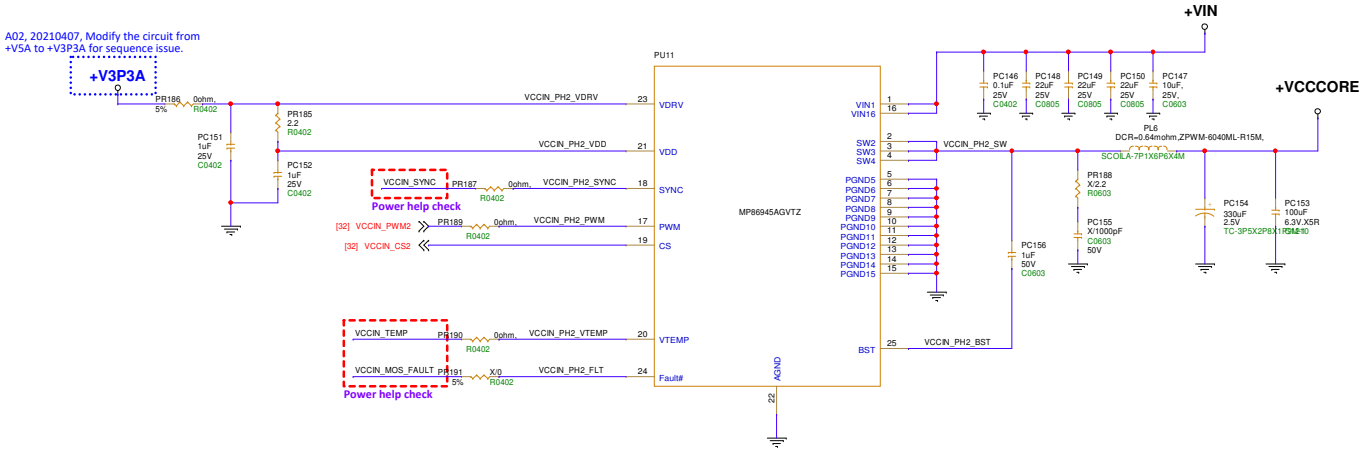
Tiger Lake IMVP9



+VCCCORE





<Variant Name>

AAEON Technology INC.

Title	PWR_+VCCCORE	
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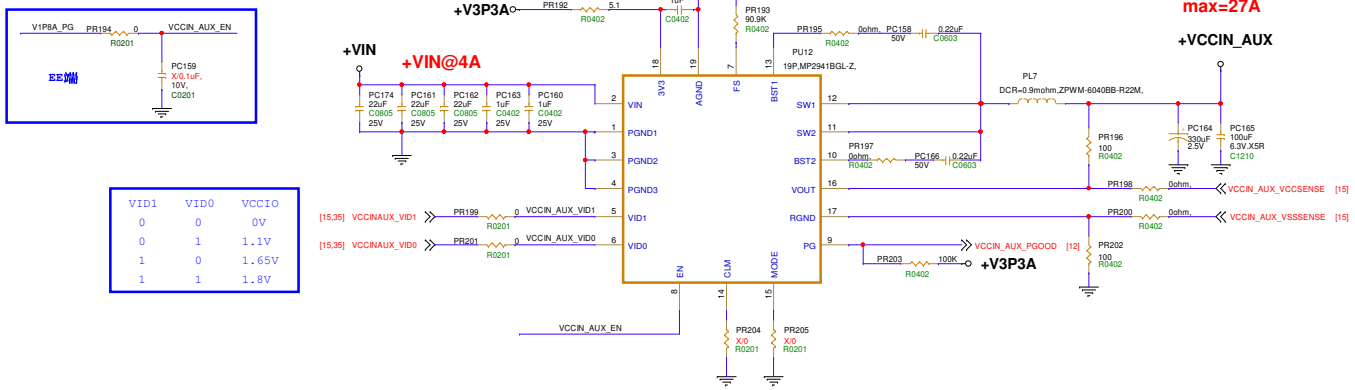
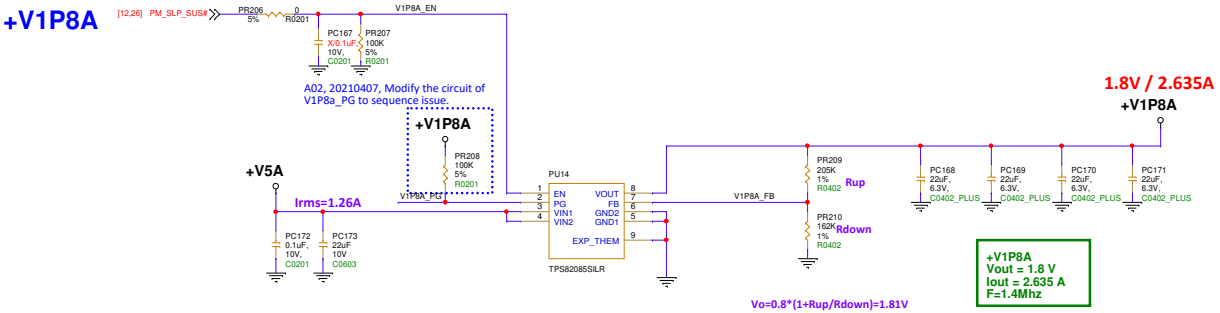
+VCCIN_AUX



VID1	VID0	VCCIO
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

+V1P8A



<Variant Name>

AAEON Technology INC.

Title: PWR_+VCCIN_AUX/+V1P8A

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#632245
CUI:Due to improper initialization of logic on the VCCST power domain in the Tiger Lake-UP3, the system may fail to exit S3.
Workaround:Intel recommends a rework of the platform by keeping the VCCST enabled during S3. Unmount PR6 & mount PR155.

A03, 20210901, Remove PR128 and place PR126 for Tiger lake resume from G3 issue.

+VCCST_CPU

+V3P3A
PR126 10K 1% R0201
[12,26,31] PM_SLP_S4# PR127 X/0 5% R0201
[12,26,36] PM_SLP_S3# PR128 X/0 5% R0201
O_SLP_S3_S4_VCCST# 3P3VCCST_OVERRIDE
PU15 SN74AUP1G32DRLR
PC108 0.1uF, 10V, C0201
PM_SLP_VCCST_OVRD
VCCINAUX_PRESENT
PU16 SN74AUP1G32DRLR
PC110 0.1uF, 10V, C0201
VCCST_EN
+V3P3A
PR131 10K 1% R0201
VCCST_PG
+V1P05_OUT_FET
PC111 10uF 6.3V C0402
VIN: 0.5V~13.5V
PU17 NCP45520IMNTWG-H DFN8F-2X2-1
+V5A
PC109 0.1uF, 10V, C0201
VCCST_CPU_DISCHARGE
PR129 300 1% R0402
+VCCST_CPU

+VCCST_CPU@0.5A

If VccST has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal Rdischarge <= VccST Rdischarge.
VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal Rdischarge <= 300 Ohms to GND.

[12] VCCST_OVERRIDE_R
VIH of VCCST_OVERRIDE_R is 1.5V
PR132 100K 5% R0201
+V1P8A
PC113 0.1uF, 10V, C0201
[15,34] VCCINAUX_VID0
[15,34] VCCINAUX_VID1
PU19 SN74AUP1G32DRLR
VCCINAUX_PRESENT_1P8
PU18 SN74LVC2G07DCKR
PR130 100K 5% R0201 3P3VCCST_OVERRIDE
+V1P8A
PC112 0.1uF, 10V, C0201
PR133 1K 5% R0201 VCCINAUX_PRESENT

+VCCSTG_CPU

[12] SLP_S0# PR134 X/0 5% R0201
[12] CPU_C10_GATE# PR135 0 5% R0201
CPU_C10_GATE_R# 3P3VCCST_OVERRIDE
PU20 SN74AUP1G32DRLR
PC114 0.1uF, 10V, C0201
VCCSTG_DIS
VCCINAUX_PRESENT
PU22 SN74AUP1G32DRLR
PC116 0.1uF, 10V, C0201
VCCSTG_EN
+V3P3A
PR137 10K 1% R0201
VCCSTG_PG
+V1P05_OUT_FET
PC117 10uF 6.3V C0402
VIN: 0.5V~13.5V
PU21 NCP45520IMNTWG-H DFN8F-2X2-1
+V5A
PC115 0.1uF, 10V, C0201
A03, 20210903, Change P/N of PC115 from 11E9510490 to 11EB510450 for detating issue
VCCSTG_CPU_DISCHARGE
PR136 300 1% R0402
+VCCSTG_CPU

+VCCSTG_CPU@ 0.3A

VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal Rdischarge <= 300 Ohms to GND.

ALL_SYS_PWRGD

[31] VDDQ_TX_PG
[36] V3P3S_PG
VCCST_PG
PU23 NC7SZ11P6X
PC118 0.1uF, 10V, C0201
I_ALL_SYS_PWRGD
I_ALL_SYS_PWRGD [32]

VCCST_PWRGD

PU24 SN74AUP1G07DRLR
PC119 0.1uF, 10V, C0201
+VCCST_CPU
PR138 1K 5% R0201
H_VCCST_PWRGD [12]

PCH_PWRGD

[32] VR_RDY
PR139 0 5% R0201
IMVP9_VR_READY
PC121 0.1uF, 10V, C0201
PU25 SN74LVC1G08DCKR
PC120 0.1uF, 10V, C0201
PR140 10K 1% R0201
PCH_PWROK [12]

20210915, A03, add PC121 to fine tune sequence timing.

SYS_PWROK

[26] SIO_POWEROK
PU26 SN74LVC1G08DCKR
PC122 0.1uF, 10V, C0201
PR141 100K 5% R0201
SYS_PWROK [12]

<Variant Name>

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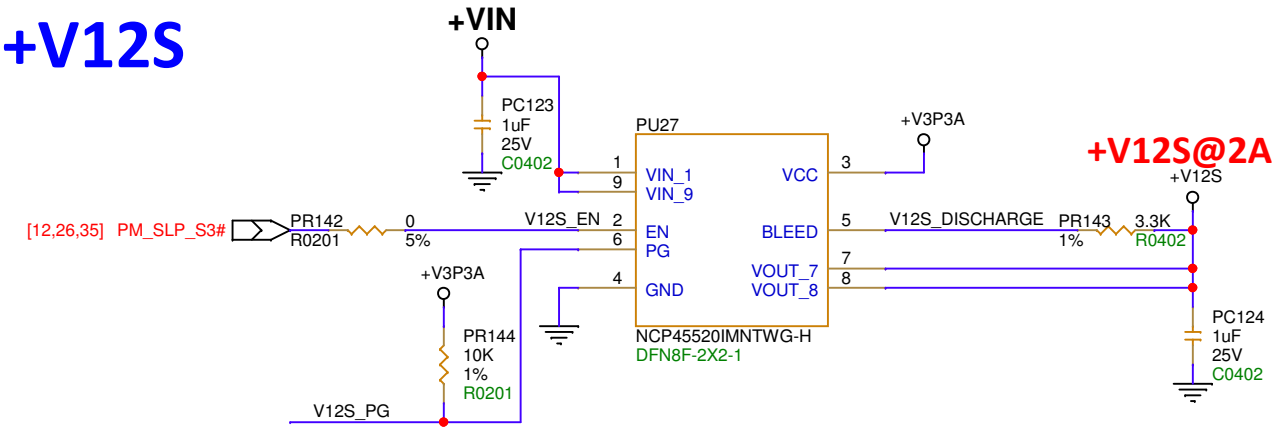
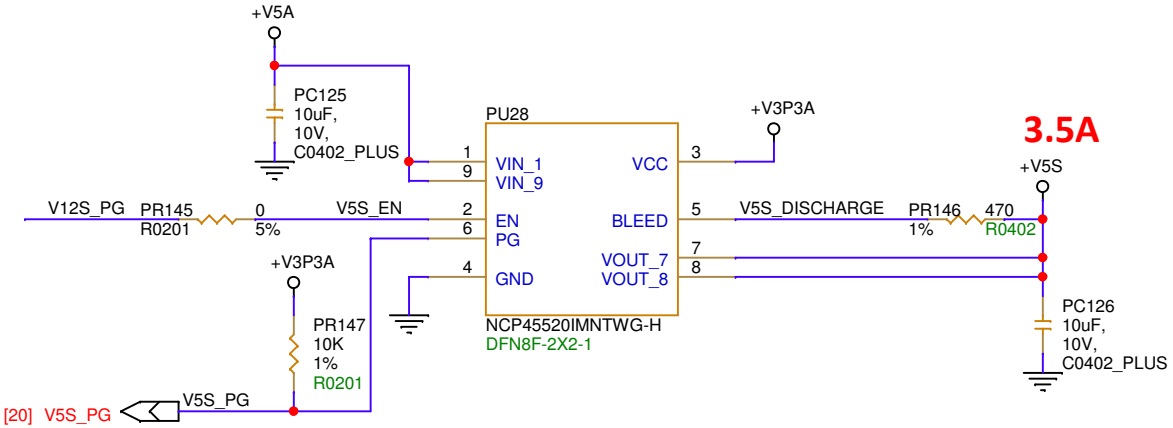
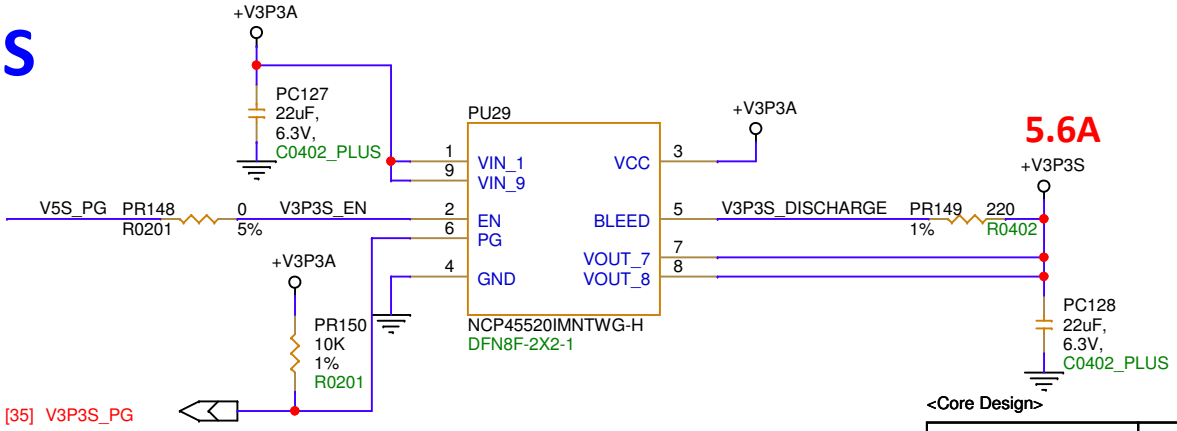
+V12S



+V5S



+V3P3S



<Core Design>

AAEON An ASUS Company	AAEON Technology INC.		
	Title: PWR_+V12S/ +V5S/ +V3P3S		
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DN-TGU8 Revision History

01. Project code: E201009
02. Model name: DN-TUG8
03. Model revision: A0.3_0_0
04. 96-Level: 9697TGU808~
05. PCB 料號: 1907TGU802
06. PCB 厚度: 2.0 mm
07. PCB 層數: 16 Layer
08. 連板數量: 2 pcs
09. PCB VIA: HDI/2+12+2
10. Material: TU-883
11. PCB Dimension: 86x55mm

DN-TGU8 A0.1_0_0 PCB: 1907TGU800 BOM: 9697TGU800~9697TGU803 Date: 2020/12/16 (TF)PCB.DN-TGU8.Rev.A0.1_0_0.HDI.(2+N+2).16L.GREEN.1*2.84*55mm
DN-TGU8 A0.2_0_0 PCB: 1907TGU801 BOM: 9697TGU804~9697TGU807 Date: 2021/05/20 (TF)PCB.DN-TGU8.Rev.A0.2_0_0.HDI.(2+12+2).16Layers.Green.1*2.84*55*2.0mm
DN-TGU8 A0.3_0_0 PCB: 1907TGU802 BOM: 9697TGU808~9697TGU80B Date: 2021/12/13 (TF)PCB.DN-TGU8.Rev.A0.3_0_0.HDI.(2+12+2).16Layers.Matt Black.1*2.84*55*2.0mm

(TF)SMD ASS'Y.DN-TGU8.Rev.A0.3_0_0.INTEL Tigerlake-UP3

BOM NUMBER	CPU	P/N
9697TGU808	i7-1185G7E	1441185G70
9697TGU809	i5-1145G7E	1441145G70
9697TGU80A	i3-1115G4E	1441115G40
9697TGU80B	i3-1115GRE	144X000096

Revision History Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.	Bug ID
1	5, 9, 22, 25	USB3	20210519	HW	Intel TCP doesn't support USB3 TYPE A	Change USB3.2 Port 1/2 from TCP to PCH HSIO	A02	
2	8	I2C	20200717	HW	Request of BIOS for test.	Add TP30~TP33 for BIOS request	A02	
3	8	Strap	20210407	HW	Issue of ME disable because the level isn't low enougth at the strap pin.	Add R361 and remove TP13 for intel ME disable issue.	A02	
4	30	Power	20210507	Power	Power ripple adjust.	Change PR20 form 120K to 82K (1050708234) for ripple adjust.	A02	
5	32	Power	20210507	Power	Power VFB adjust.	Change PR162 form 806 to 931 (1050593104) for VFB adjust.	A02	
6	32	Power	20210507	Power	Power IMON adjust.	Change PR174 form 60.4K to 68K (105A506834) for IMON adjust.	A02	
7	33	Power	20210407	Power	Power sequence issue	Modify the circuit from +V5A to +V3P3A for sequence issue	A02	
8	07	SPI	20210831	HW	Remove JP1 for PE request.	Remove JP1	A03	
9	10	RTC	20210831	HW	Change P/N of JRTC1 from 1655902034 to 1655X00019 by PE suggestion	Change P/N of JRTC1 from 1655902034 to 1655X00019	A03	
10	12, 30	SEQUENCE	20210929	HW	tPCH14 timing fail	1. ADD D5 2. Change package of PR17 from 0402 to 0201 3. turn the package of PSP1 180 drgee to fit layout Request	A03	
11	21	PCIE	20211025	HW	1654904032 EOL	Change P/N of JPCIE_FPC1 from 1654904032 to 1654904035	A03	
12	25, 27	USB	20211014	HW	USB 2.0 SI fail	Change L7, L9, L2~L5 to 0R resistor	A03	
13	26	SIO	20210915	HW	power on without RTC battery fail	Change value of R268 from 0R to 100k	A03	
14	26	SIO	20211022	HW	81996-B EOL	Change Part of U25 from 81996-B to 81966-D	A03	
15	26	SIO	20211025	HW	Change strap pin to set power mode to ATX.	ADD R289	A03	
16	28	eSPI	20211013	HW	Change Power from +V3P3A to +V3P3S by BIOS request.	Change Power at JESPI.5 from +V3P3A to +V3P3S	A03	
17	29	LED	20210910	HW	find tune the LED lighting	Change values of R339 and R340 from 240 to 680	A03	
18	31	SEQUENCE	20210929	HW	tcpu01 timing fail	Place PC56 to find tune power up sequence issue	A03	
19	32	SEQUENCE	20210915	HW	fine tune sequence timing	Change value of PR169 form 10K to 33K	A03	
20	32	POWER	20211018	HW	Change package of PC130 from 0603 to 0402	Change package of PC130 from 0603 to 0402	A03	
21	35	POWER	20210901	HW	Tiger lake resume from G3 issue.	Remove PR128 and place PR126	A03	
22	35	POWER	20210903	HW	detating issue	Change P/N of PC115 from 11E9510490 to 11EB510450	A03	
23	35	SEQUENCE	20210915	HW	fine tune sequence timing	add PC121	A03	
24	24	I225	20211103	HW	Fine tune xtal frequence by FAE test result	1. Change P/N of Y7 from 12310025A5 to 12310025AE 2. Change value of C306 and C324 from 10pF to 6.2pF, by FAE test result.	A03	
25	10	Xtal	20211027	HW	change vendor	Change P/N Y1 from 1231327631 to 1231332726	A03	
26	23	LAN	20211103	HW	Fine tune xtal frequence by FAE test result	1. Change P/N of Y3 from 12310025A5 to 12310025AE 2. Change value of C330 and C331 from 15pF to 12pF, by FAE test result.	A03	
27	20, 25, 27	TVR	20211111	HW	13055V0SP0 EOL	Change P/N from 13055V0SP0 to 1305Q00022 for U22~U24, U19, U33, U34, U13, U27, U28, U29	A03	
28	27	USB	20211111	HW	1430097420 EOL	U7 EOL, Change P/N from 1430097420 to 143X000115	A03	
29	21	PCIE	20211111	HW	JPCIE_FPC1 EOL	Change P/N of JPCIE_FPC1 from 1654904035 to 16549X0027	A03	
30	25	USB	20211111	HW	U17 EOL	Change P/N from 1430097420 to 143X000088	A03	
31	22	M.2	20211115	HW	to enable 4G/5G WWAN card	Place R360	A03	

<Variant Name>

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