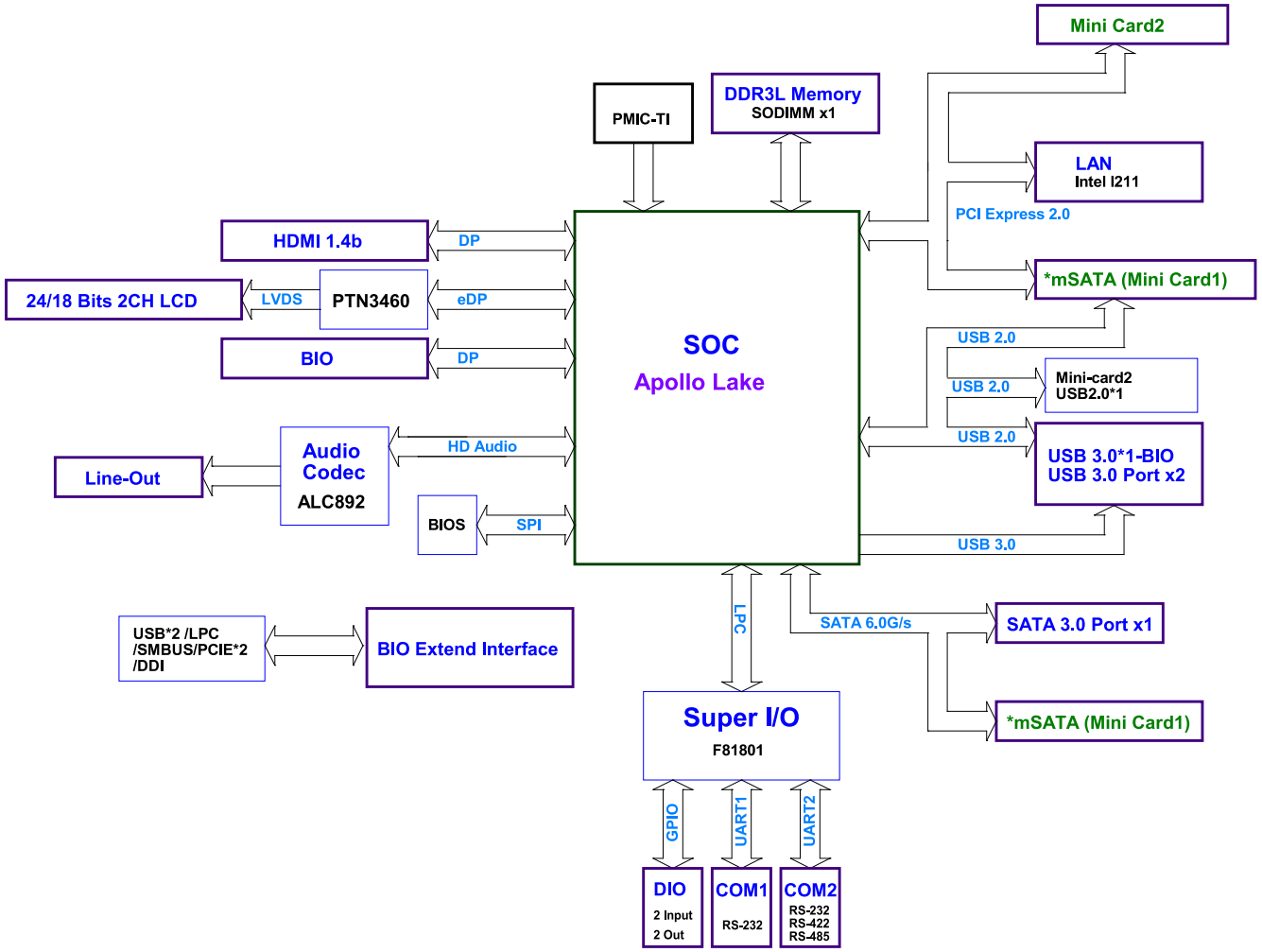
PICO-APL2 Rev.A1.0_0_0

Apollo Lake SoC Platform Cross Compatibility



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Project Number : E161107

Production Line : Sub.EPI.AA2M

<Variant Name>

Title: Cover Sheet		
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SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	
GPIO_1	1.8V	20K PD/I	
GPIO_2	1.8V	20K PD/I	
GPIO_3	1.8V	20K PD/I	
GPIO_4	1.8V	20K PD/I	LVDS_RBIT0
GPIO_5	1.8V	20K PD/I	LVDS_RBIT1
GPIO_6	1.8V	20K PD/I	LVDS_RBIT2
GPIO_7	1.8V	20K PD/I	LVDS_RBIT3
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	WAKE_RI#
GPIO_15	1.8V	20K PD/I	EN_USB
GPIO_16	1.8V	20K PD/I	LAN1_DISABLE#
GPIO_17	1.8V	20K PD/I	W_DISABLE0#
GPIO_18	1.8V	20K PD/I	W_DISABLE1#
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GP[0]
GPIO_23	1.8V	20K PD/I	SATA_GP[1]
GPIO_24	1.8V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	1.8V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/IO	
GPIO_217	1.8V	20K PD/IO	
GPIO_218	1.8V	20K PD/IO	
GPIO_219	1.8V	20K PD/IO/OP	

The Mapping Table For Super I/O F81801U GPIOs :

Name	PIN No.	Power	Type	Description & setting
GPIO[6]	42	+3.3V_ALW	I/OOD12t	
GPIO[12]	35	+3.3V	I/OOD12t	WDTRST#
GPIO[15]	36	+3.3V	I/OOD12,st,lv	None
GPIO[16]	37	+3.3V	I/OOD12,st,lv	
GPIO[20]	38	+3.3V	I/OOD12,st,lv	
GPIO[21]	39	+3.3V	I/OOD12t	
GPIO[22]	40	+3.3V	I/OOD12t	
GPIO[23]	41	+3.3V	I/OOD12t	
GPIO[30]	9	+3.3V	I/OOD12t	DCDB#
GPIO[31]	10	+3.3V	I/OOD12t	RIB#
GPIO[32]	11	+3.3V	I/OOD12t	CTSB#
GPIO[33]	13	+3.3V	I/OOD12t	DTRB#
GPIO[34]	14	+3.3V	I/OOD12t	RTSB#
GPIO[35]	15	+3.3V	I/OOD12t	DSRB#
GPIO[36]	16	+3.3V	I/OOD12t	TXB#
GPIO[37]	17	+3.3V	I/OOD12t	RXB#

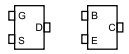
I/OOD12st,lv : Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.

I/OOD12t : TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability

F75111RG GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO10	5V	VSB3V	Native	BOARDID_BIT0
GPIO11	5V	VSB3V	Native	ADM213_EN
GPIO12	5V	VSB3V	Native	81438_SD
GPIO13	5V	VSB3V	Native	
GPIO14	5V	VSB3V	Native	BOARDID_BIT1
GPIO15	5V	VSB3V	Native	
GPIO16	5V	VSB3V	Native	
GPIO17	5V	VSB3V	Native	
GPIO20	5V	VSB3V	Native	SEL_COM2_MD0
GPIO21	5V	VSB3V	Native	SEL_COM2_MD1
GPIO22	5V	VSB3V	Native	COM2_SLEW
GPIO23	5V	VSB3V	Native	BIO-GPIO
GPIO24	5V	VSB3V	Native	DIO_P0
GPIO25	5V	VSB3V	Native	DIO_P1
GPIO26	5V	VSB3V	Native	DIO_P2
GPIO27	5V	VSB3V	Native	DIO_P3
GPIO30	5V	VSB3V	GPIO	LVDS_EN
GPIO31	5V	VSB3V	GPIO	
GPIO32	5V	VSB3V	GPIO	
GPIO33	5V	VSB3V	GPIO	LVDS_PD#

PCB Footprints



SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
GPIO IC	6Eh
PTN3460 Slave	C0h

PCB STACK :

Impedence 50ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : GND
- Layer 5 : Signal
- Layer 6 : VCC
- Layer 7 : Signal
- Layer 4 : Signal
- Layer 9 : GND
- Layer 10 : Solder

<Variant Name>

AAEON an ASUS assoc. co.

Title: System Settings

Size: B | Document Number: PICO-APL2 | Rev: A1.0_0_0

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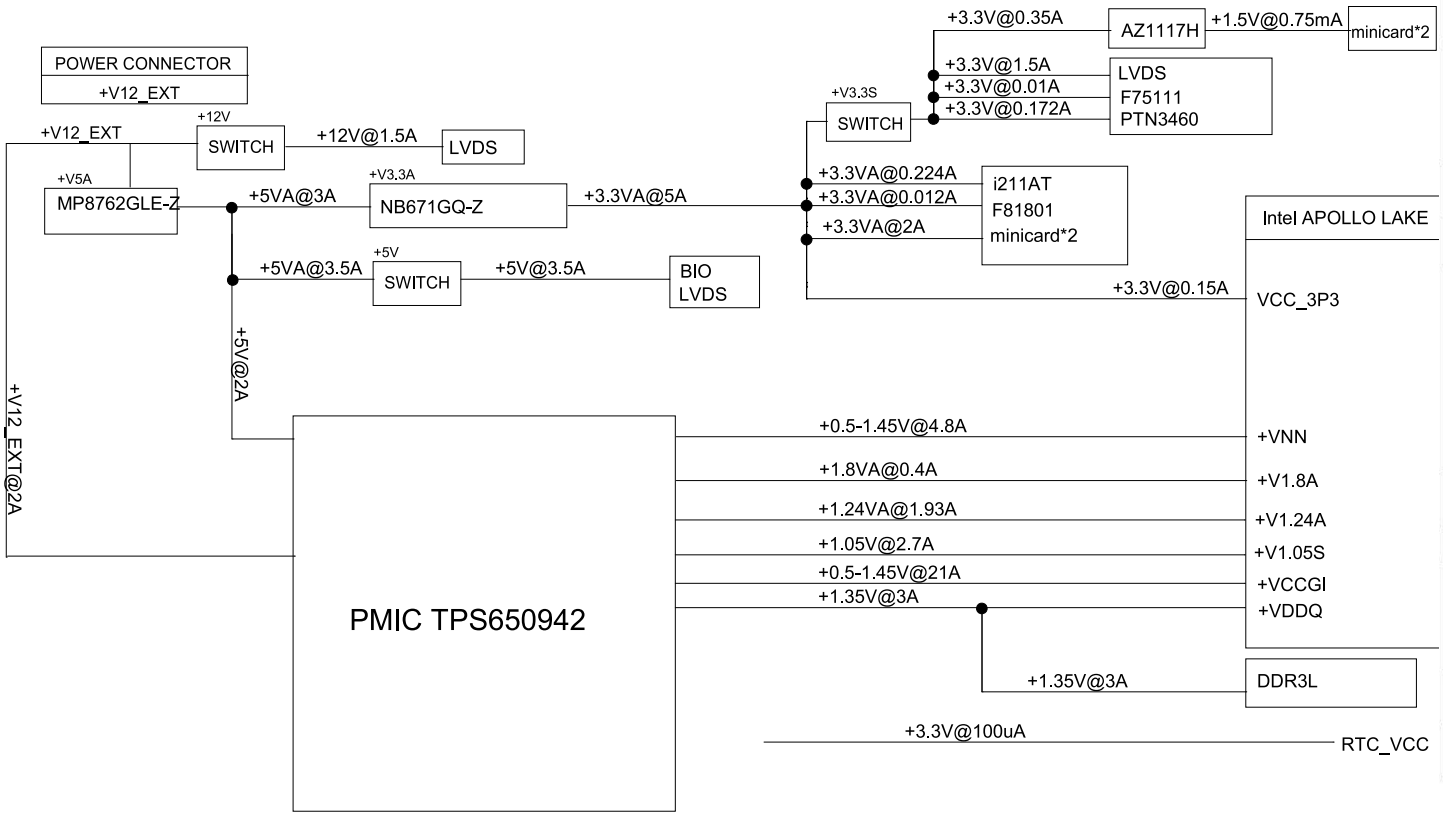

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Iccmax (A)
VCC_VCGI	0.45-1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	21
VNN	0.45-1.3	+/-50mV	4.8
VCC_V1P05	1.05	+/-5%	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	1.3
VCC_V1P24_A	1.24	+/-5%	TBD
VCC_V1P8V_A	1.8	+/-5%	0.4
VDDQ	1.35	+/-5%	2.8 (excluding DRAM)
	1.24	+/-5%	
VCC_3P3V_A	3.3	+/-5%	0.15
VCC_RTC_3P3V	2-3.47	N/A	TBD

+V5A -> +V3.3A -> +VNN -> +VCC -> +V1P8A- > +V1P24A -> +V1P8U -> +VDDQ
+V1.05S -> +VCC_VCGI

<Core Design>

AAEON an ASUS assoc. co.

Title: Power Tree

Size: Custom | Document Number: PICO-APL2 | Rev: A1.0_0_0

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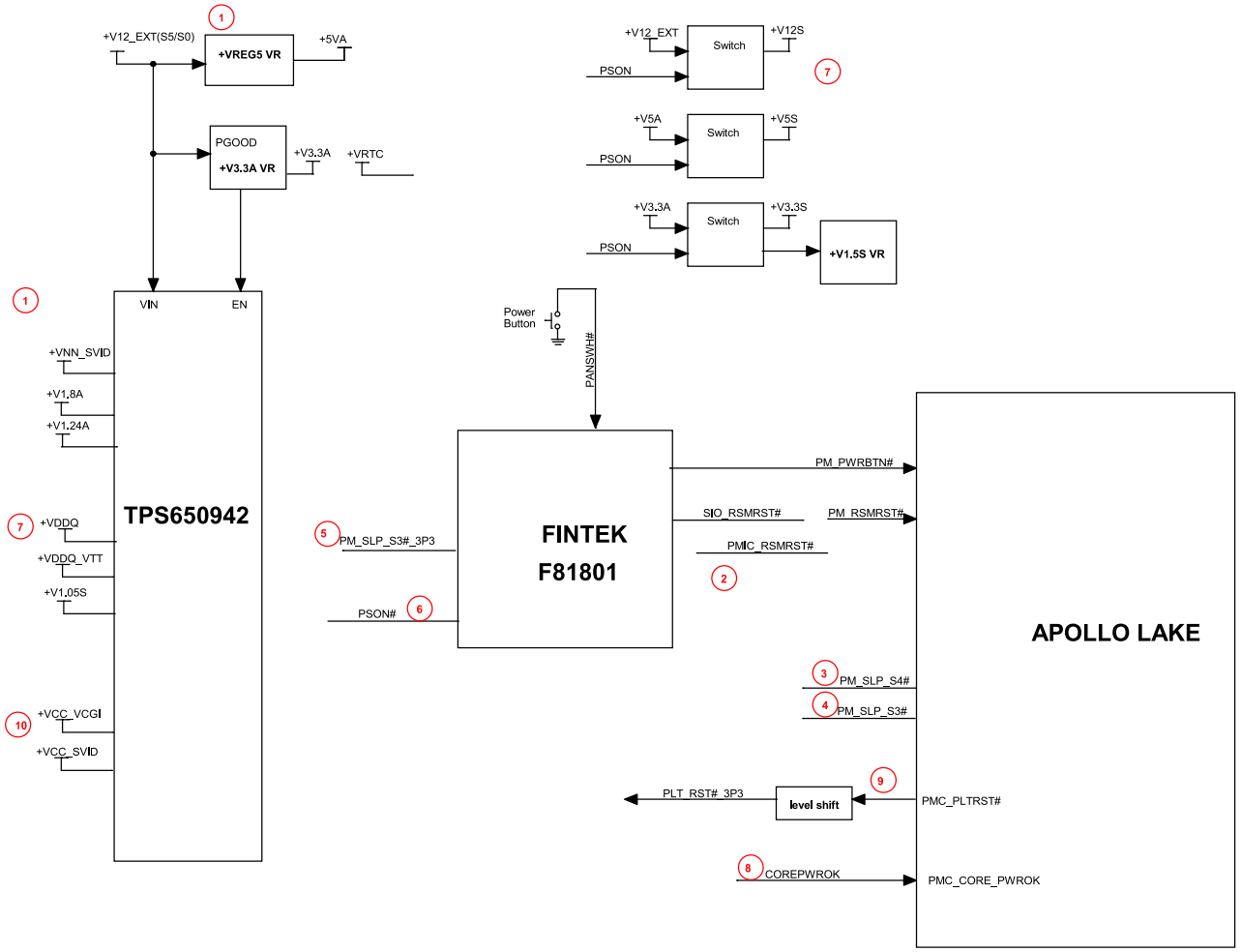
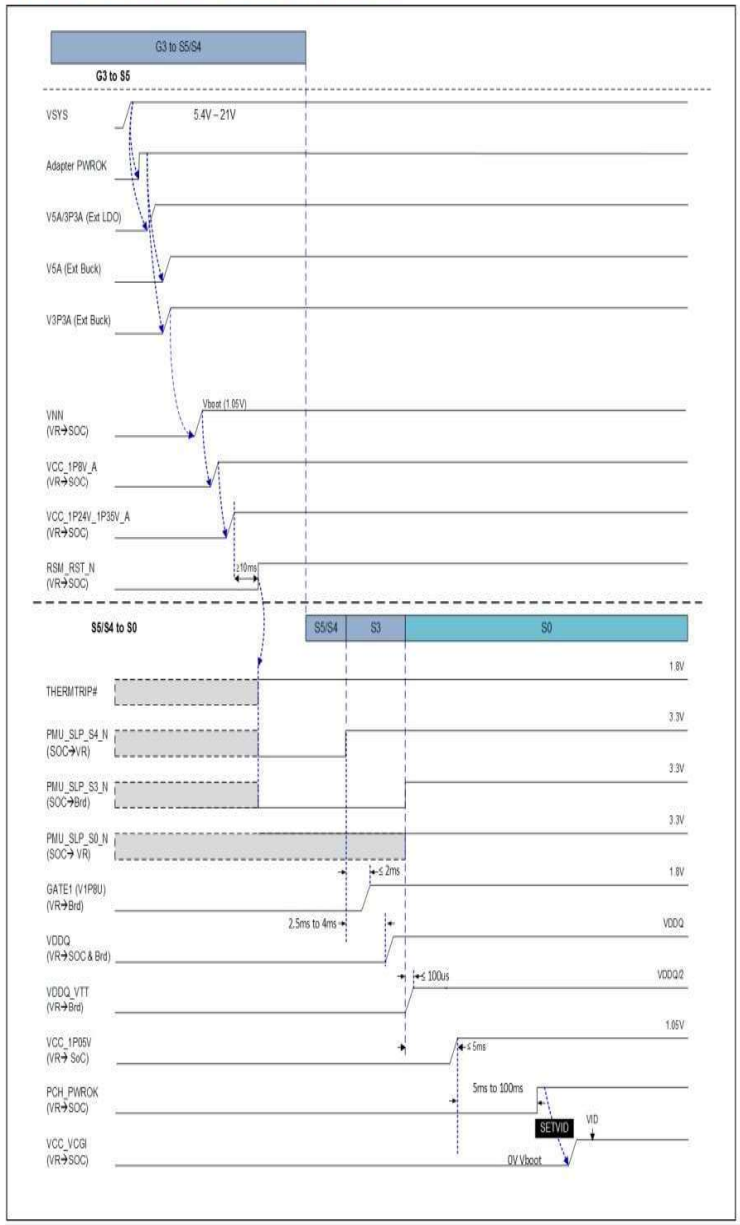


Power-Up Sequencing (G3 to S0)—Adapter



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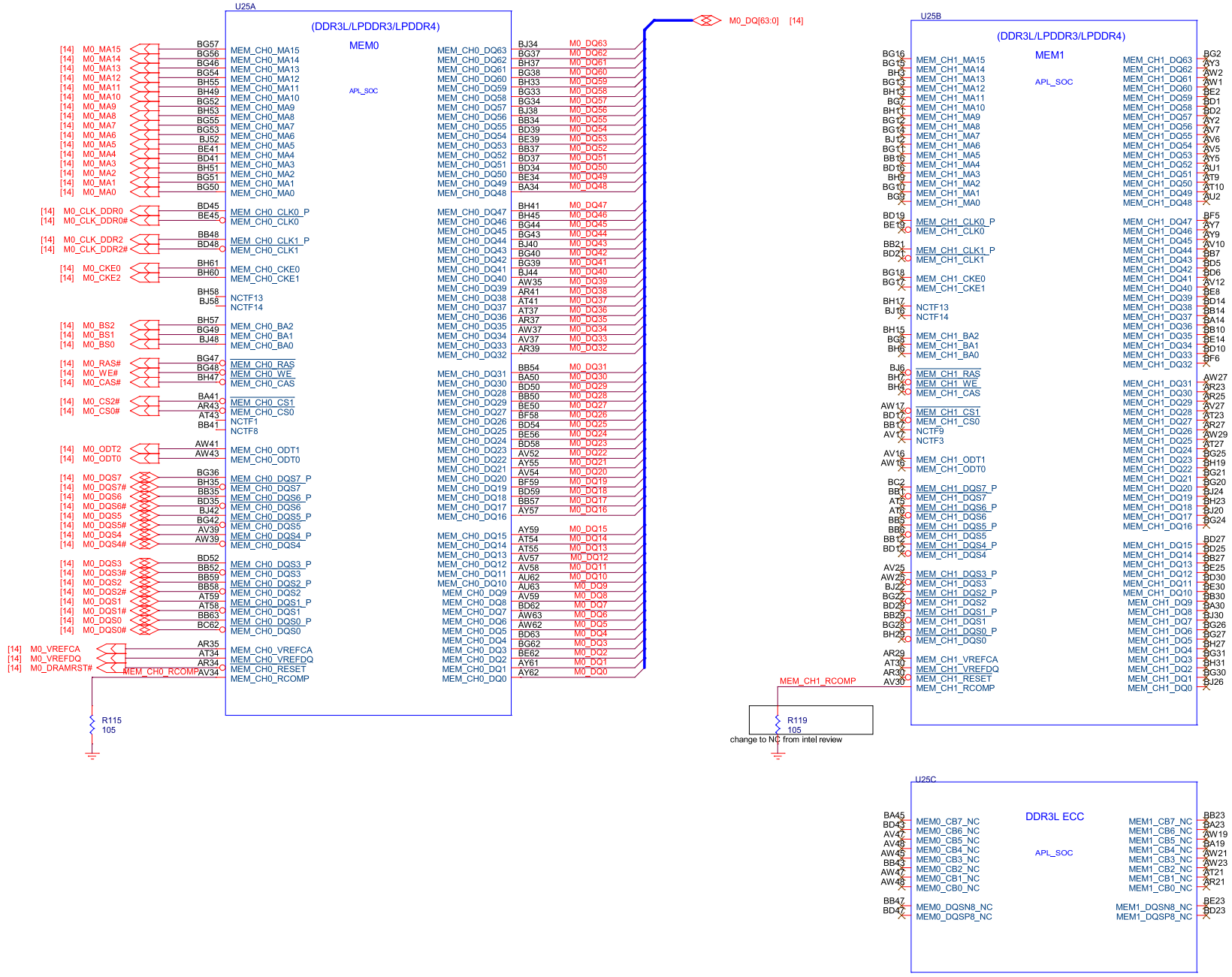

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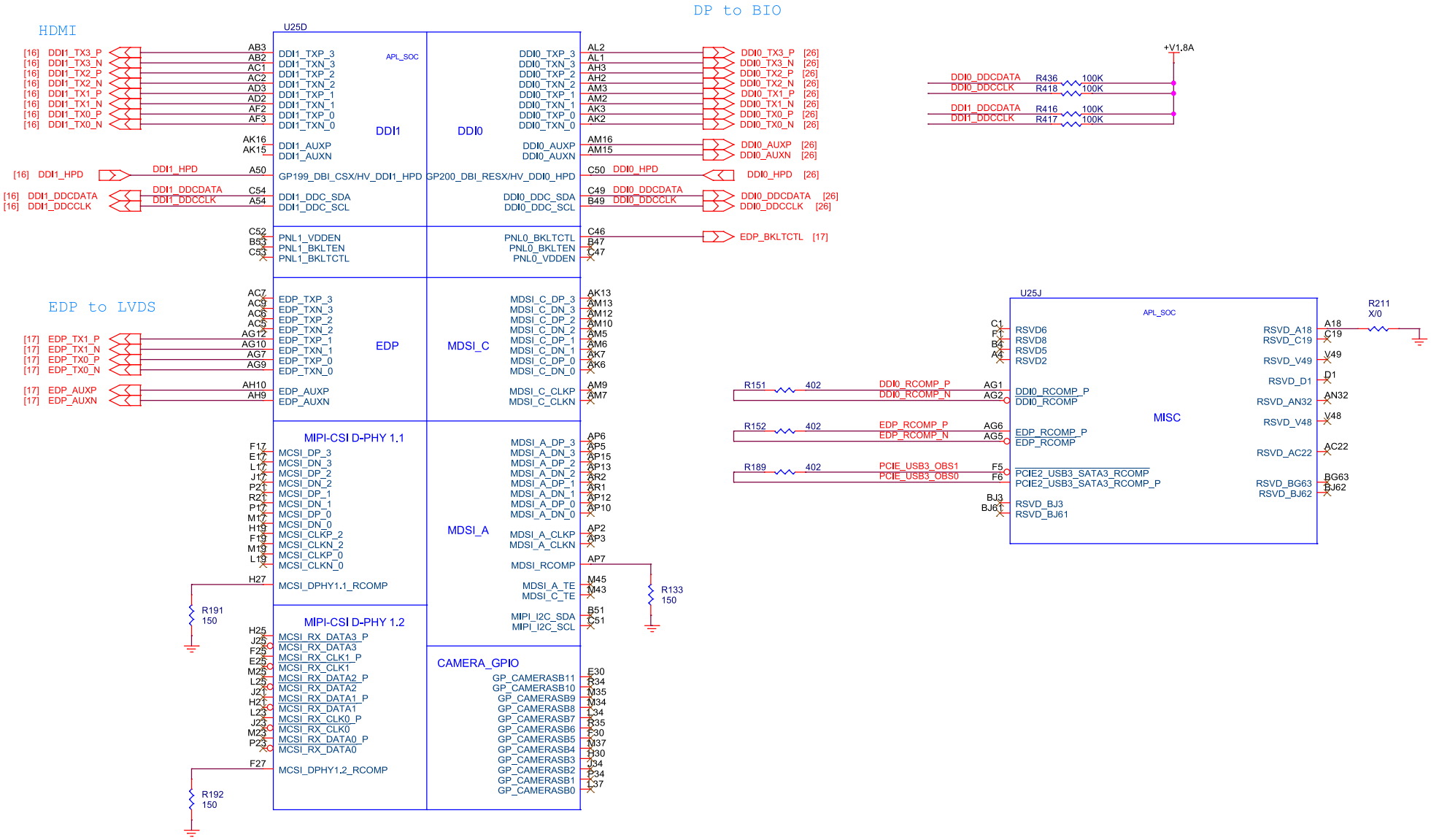

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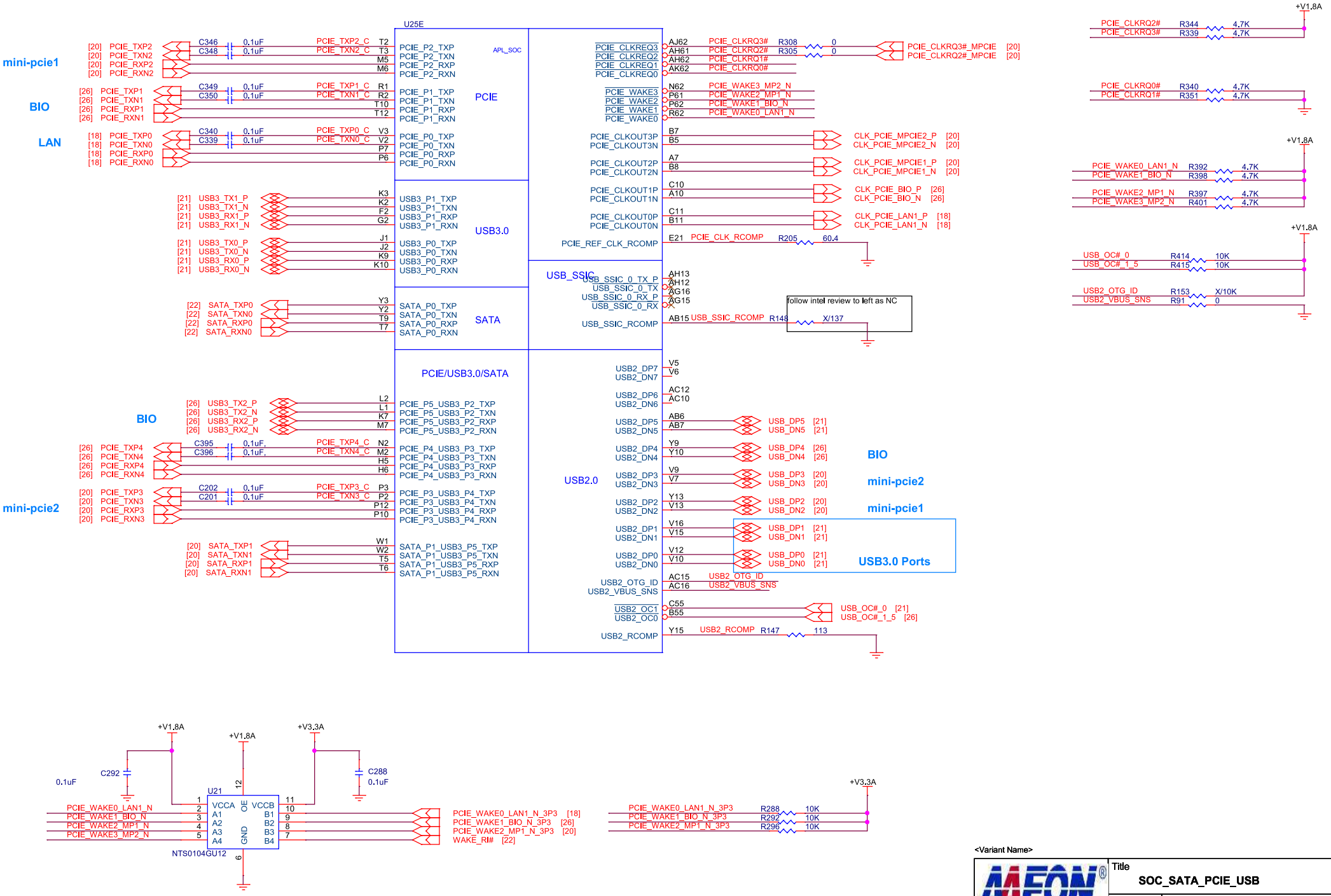

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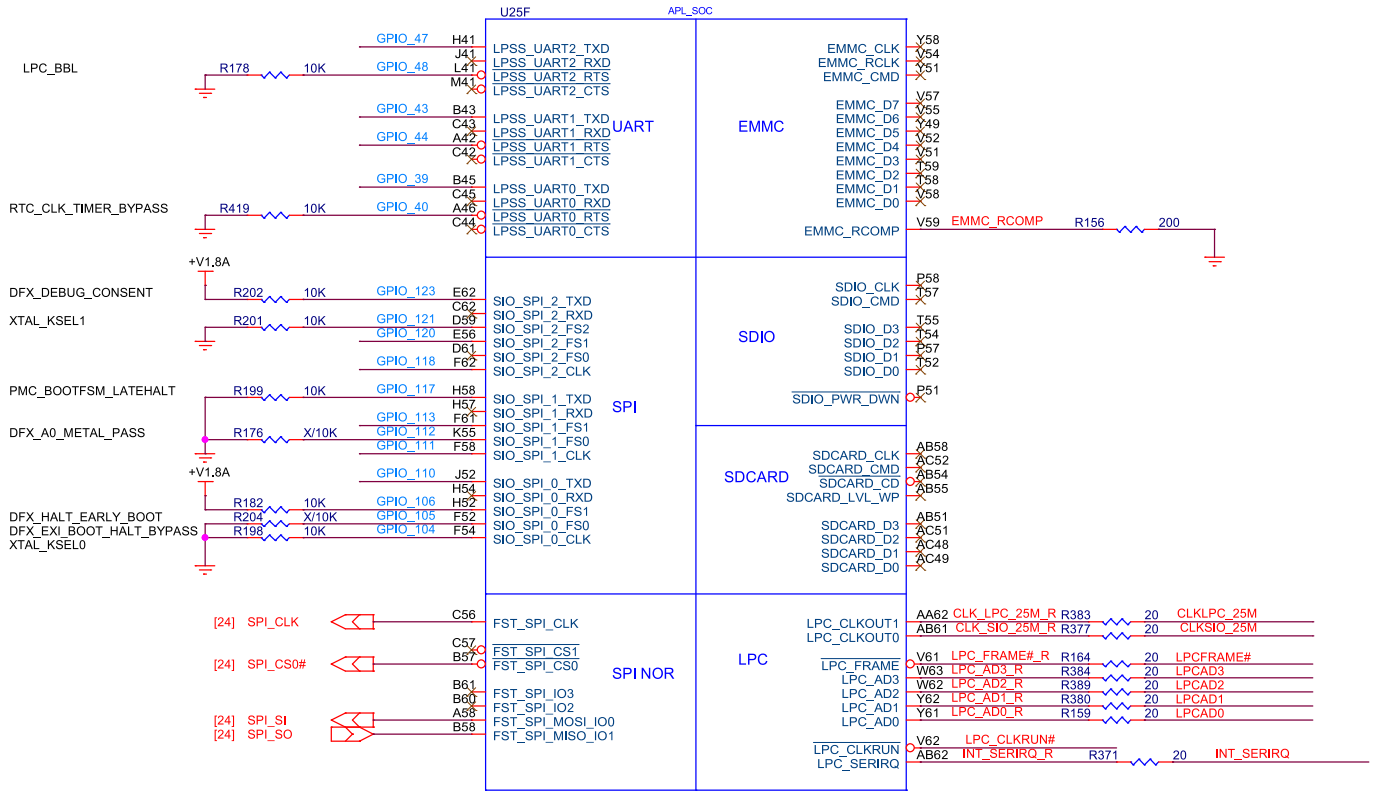
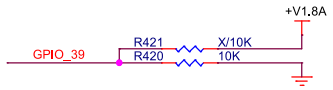
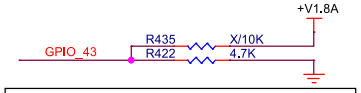
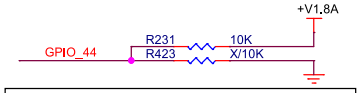




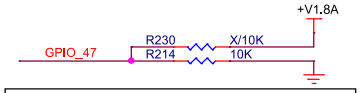
Enable CSE ROM Bypass	
GPIO_39	CSE ROM Bypass
0	Disable bypass (default)
1	Enable Bypass



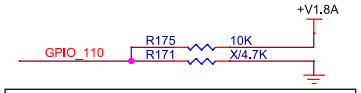
Allow eMMC as a boot source	
GPIO_43	eMMC as a boot
0	Disable
1	Enable (default)



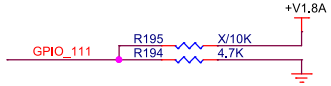
Allow SPI as a boot source	
GPIO_44	SPI as a boot
0	Disable
1	Enable (default)



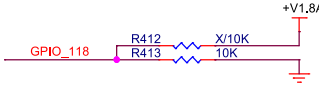
Force DNX FW Load	
GPIO_47	DNX FW Load
0	Do not force (default)
1	Enable



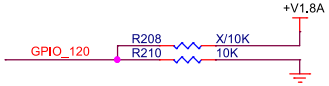
LPC 1.8V/3.3V Mode Select	
GPIO_110	LPC Voltage
0	3.3V mode
1	1.8V mode (default)



Boot BIOS Strap (BBS)	
GPIO_111	
0	Boot from SPI
1	Do not boot from SPI (default)



Flash Descriptor Override	
GPIO_118	
0	No Override (Normal Operation)
1	Override



Top swap override	
GPIO_120	
0	Disable (default)
1	Override

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AAEON an ASUS assoc. co.

Title: SOC_LPC_SPI_EMMC_SD

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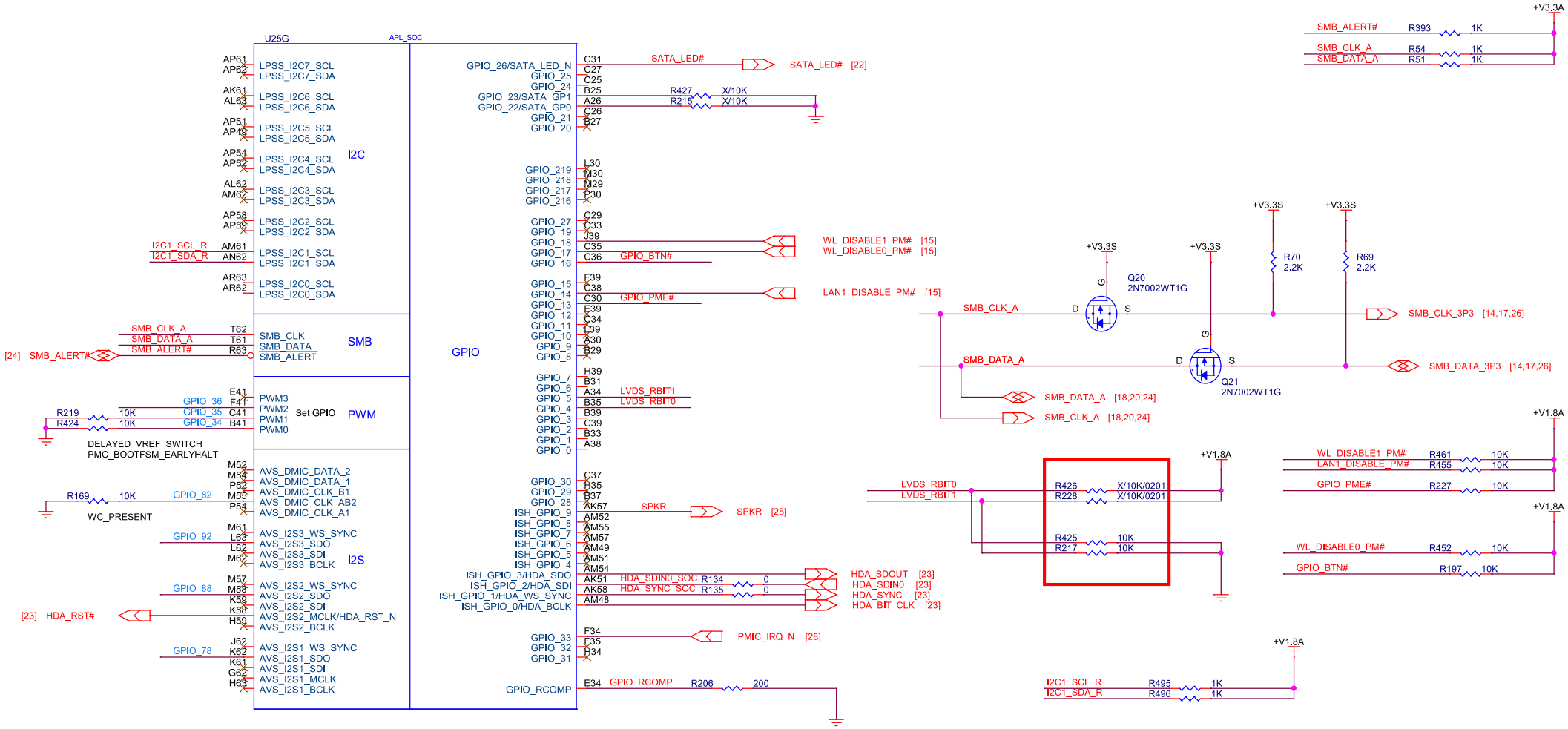
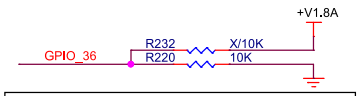
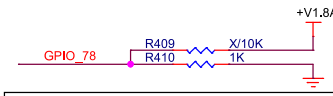
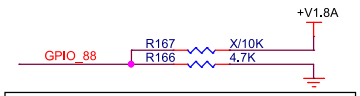




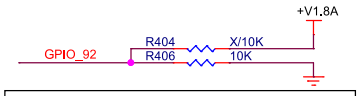
VCC_1P24V_1P35V_A Volt Selection	
GPIO_36	VCC_1P24V_1P35V_A
0	1.24V (default)
1	1.35



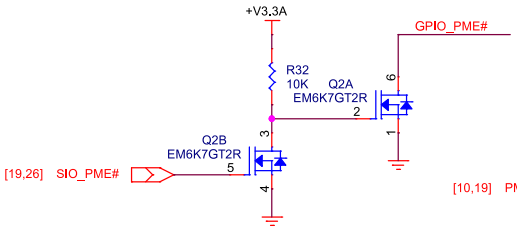
SMBus 1.8V/3.3V mode Select	
GPIO_78	SMBus
0	3.3V
1	1.8V (default)

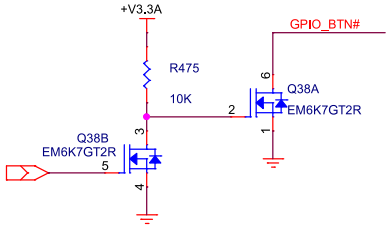


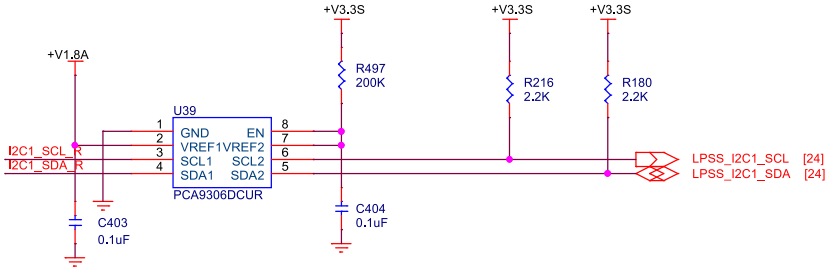
PMU 1.8V/3.3V Mode Select	
GPIO_88	PMU
0	3.3V
1	1.8V (default)



SMBus No Re-Boot	
GPIO_92	No Re-Boot
0	Disable (default)
1	Enable







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AAEON an ASUS assoc. co.

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SOC_SMBUS_GPIO		
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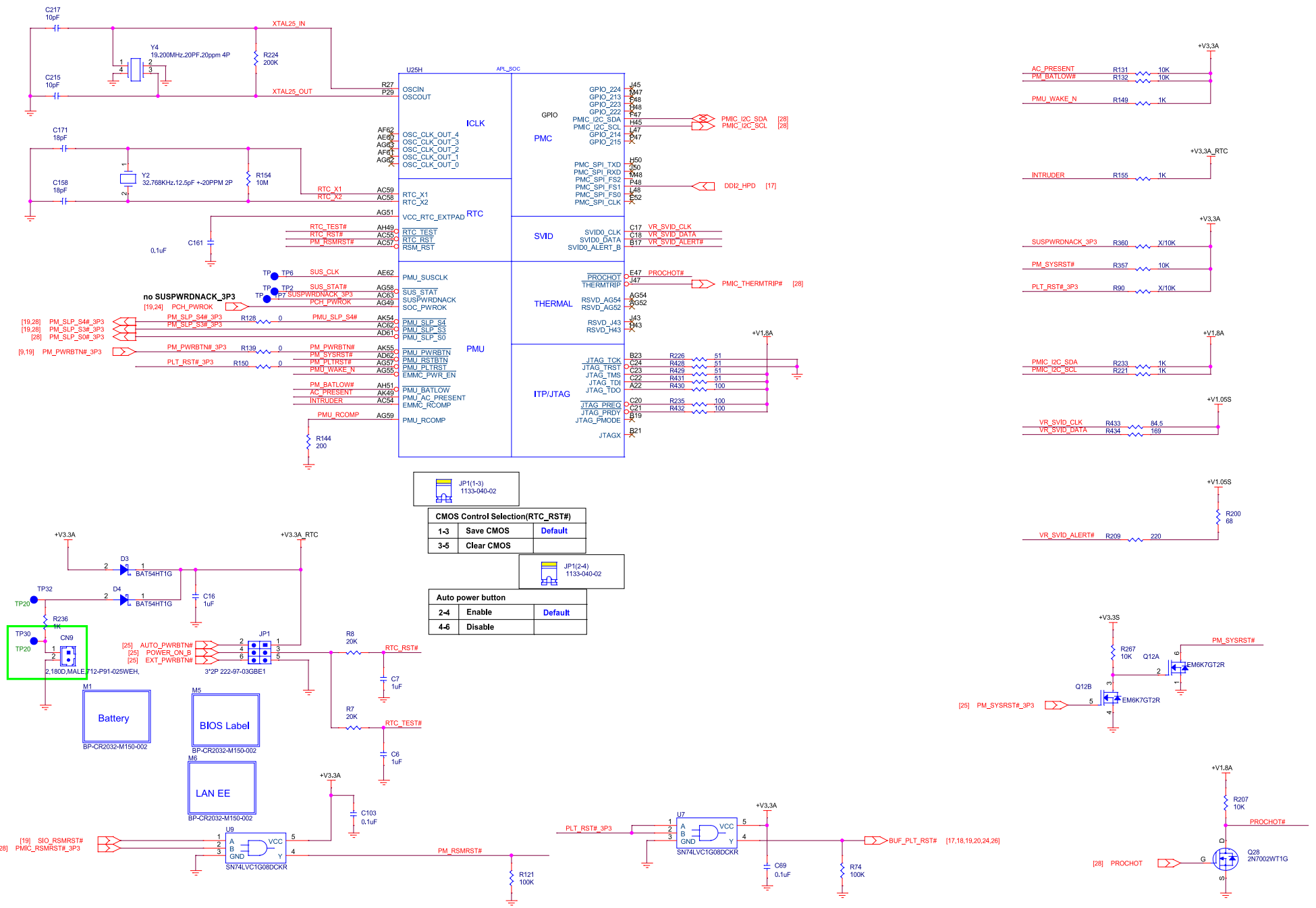

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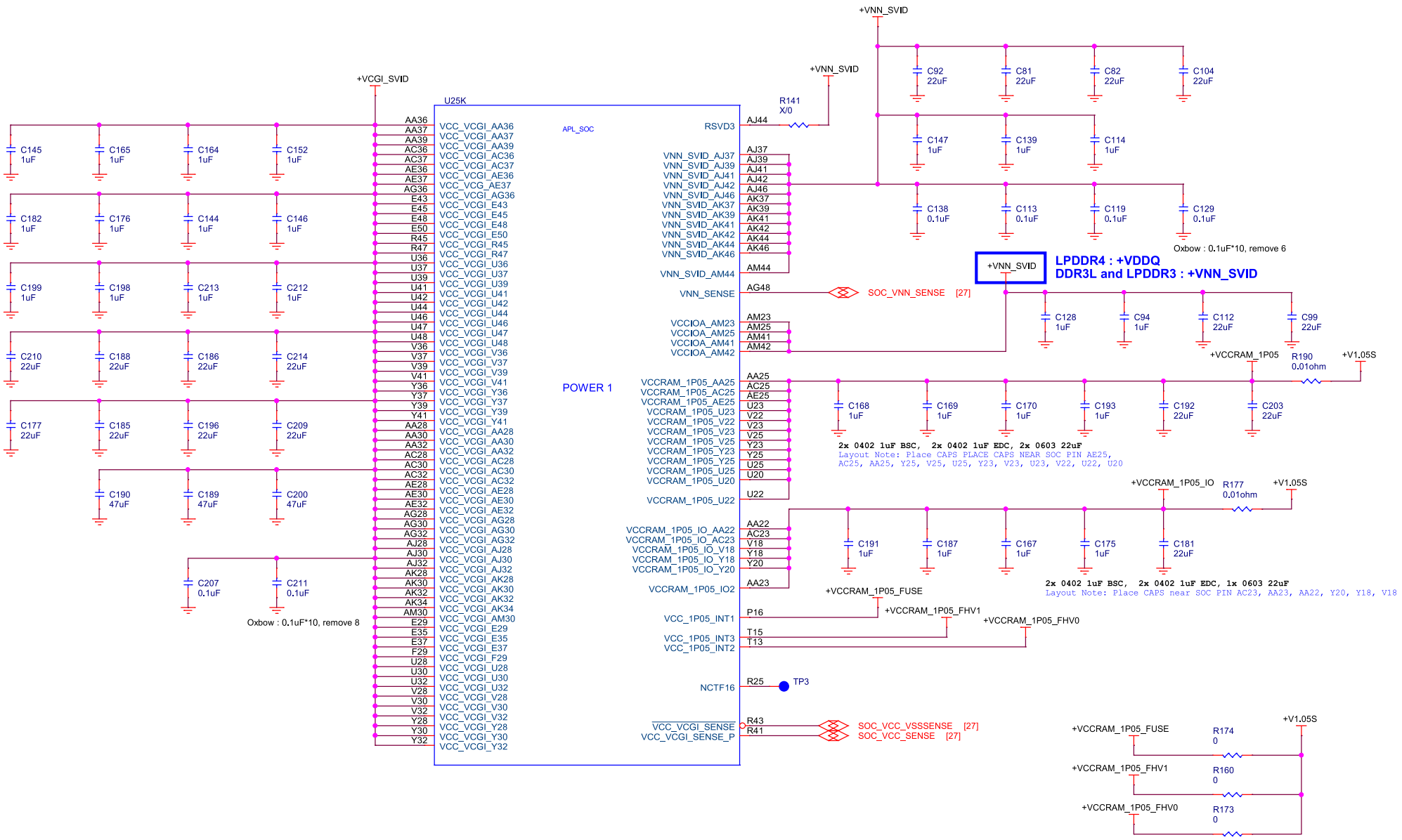

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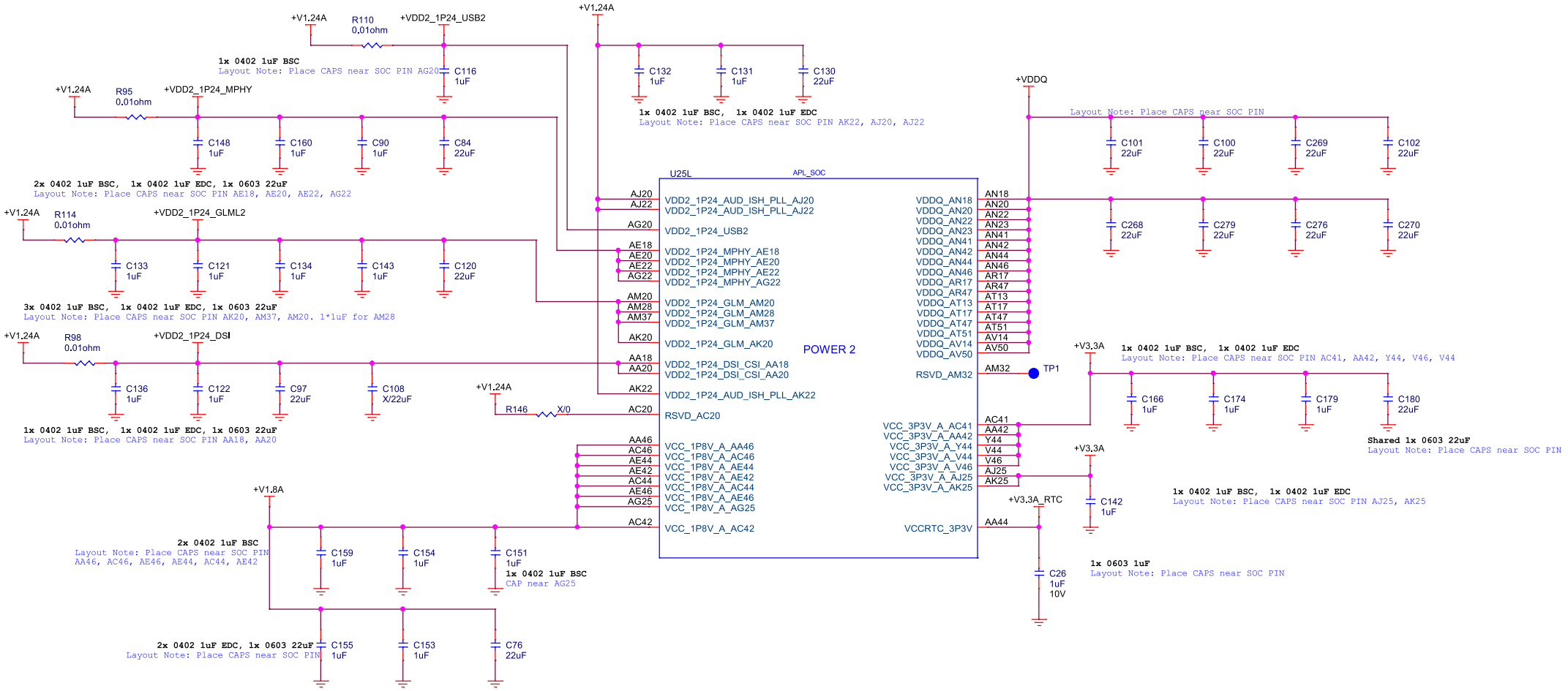

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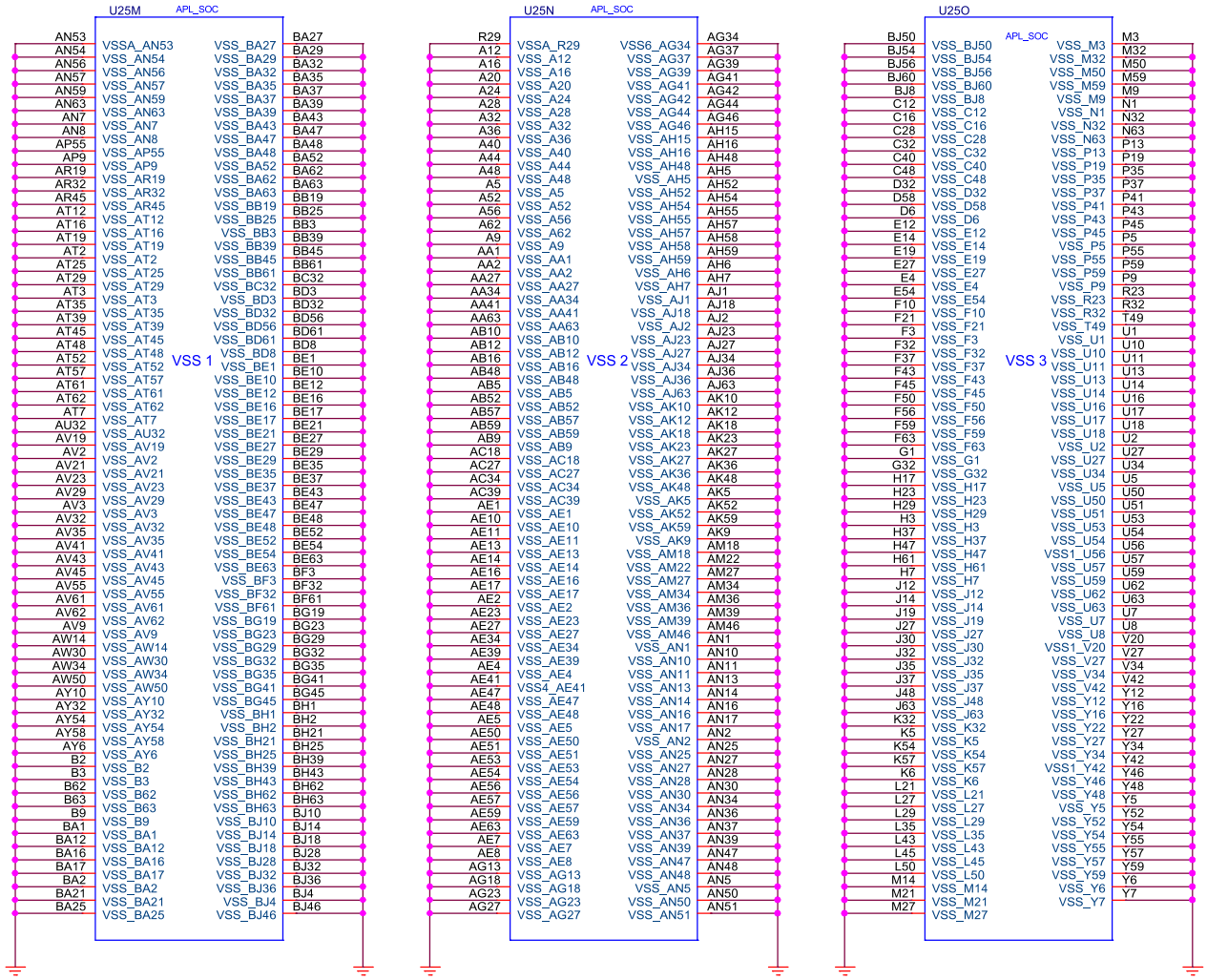

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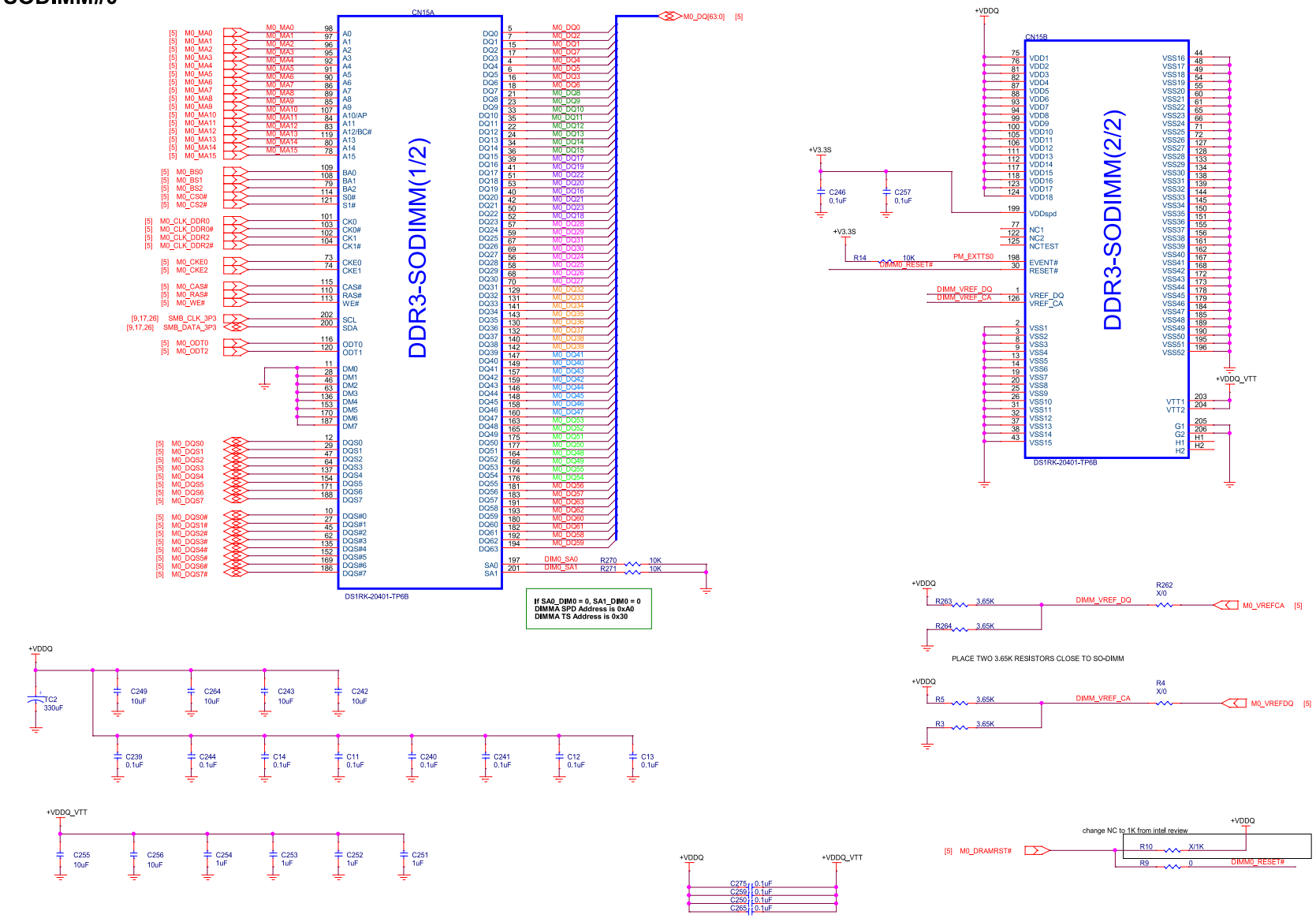
SODIMM#0



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AAEON an ASUS assoc. co.

Title: DDR3L SODIMM

Size	Document Number	Rev:
C	PICO-APL2	A1.0_0_0

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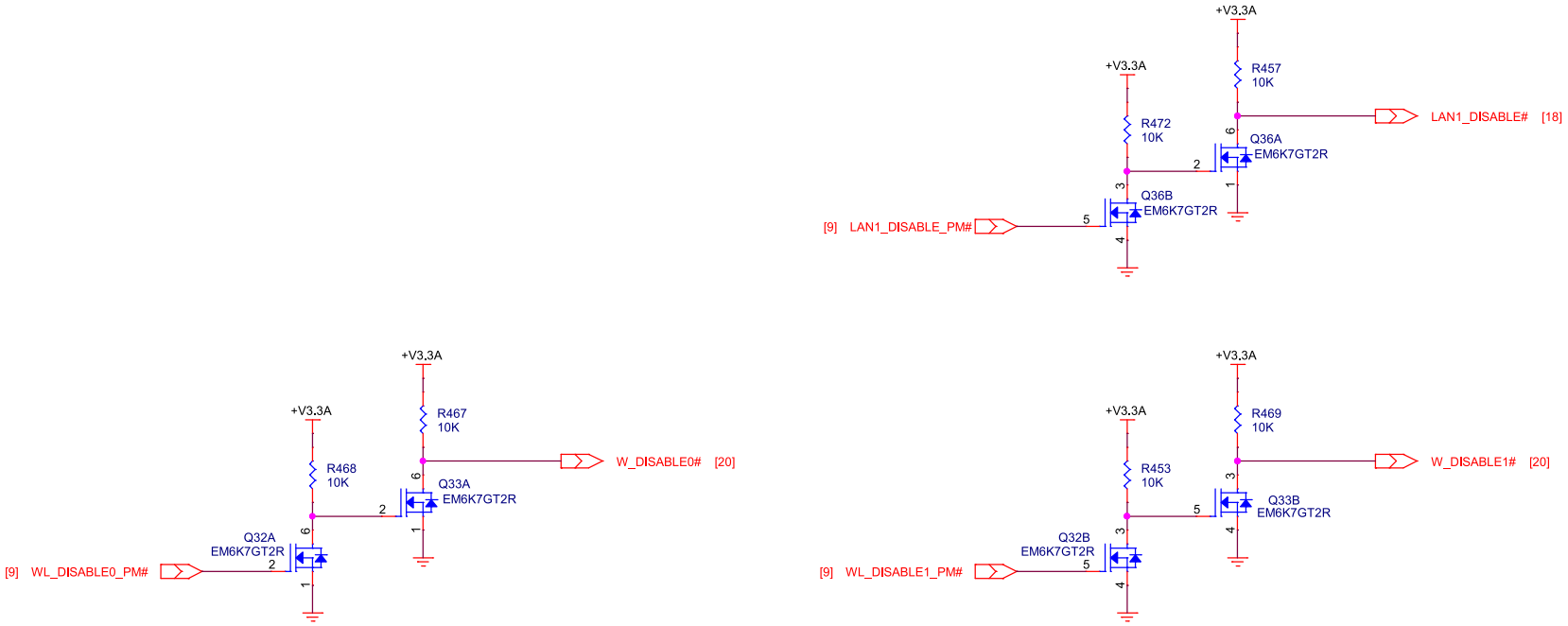
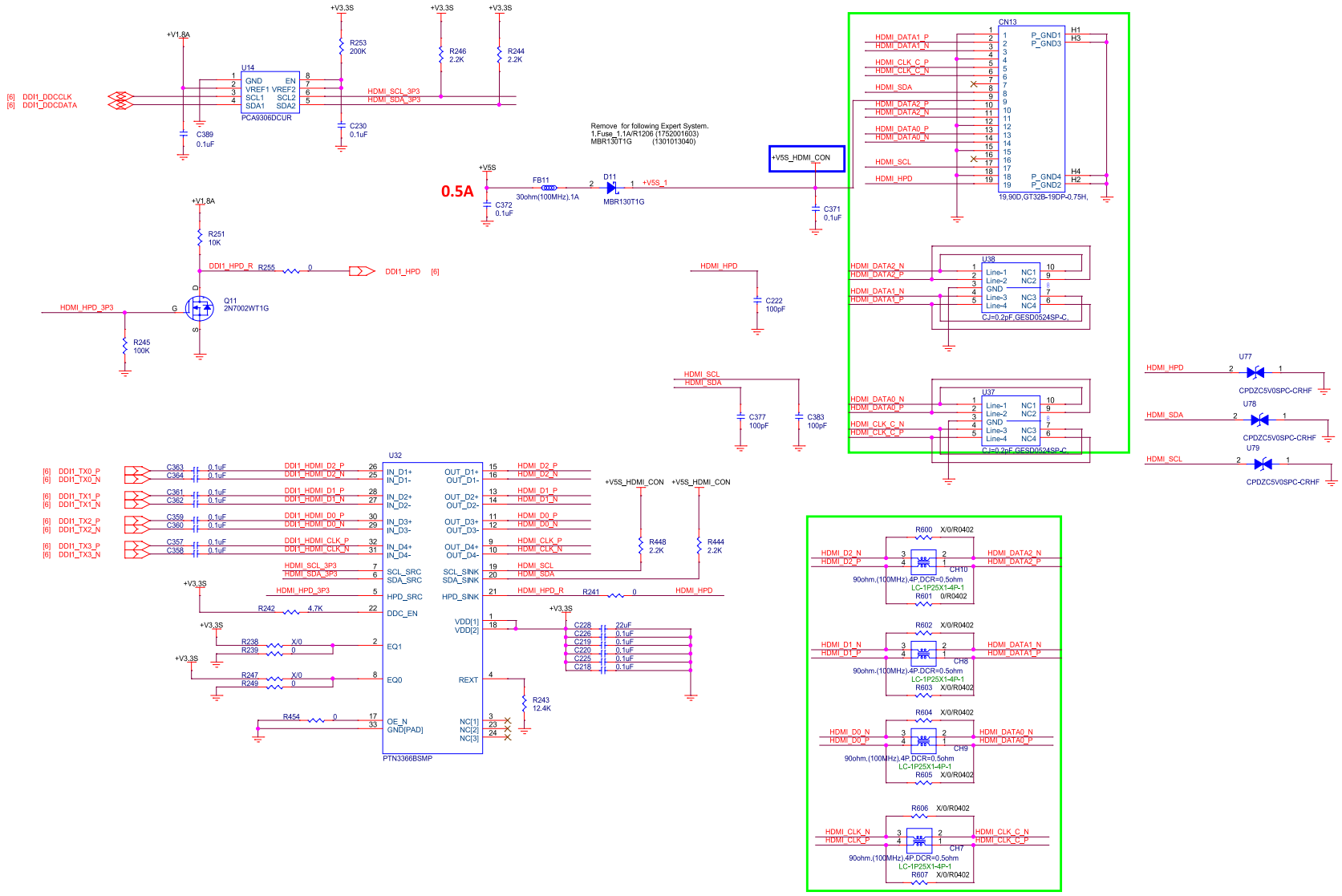


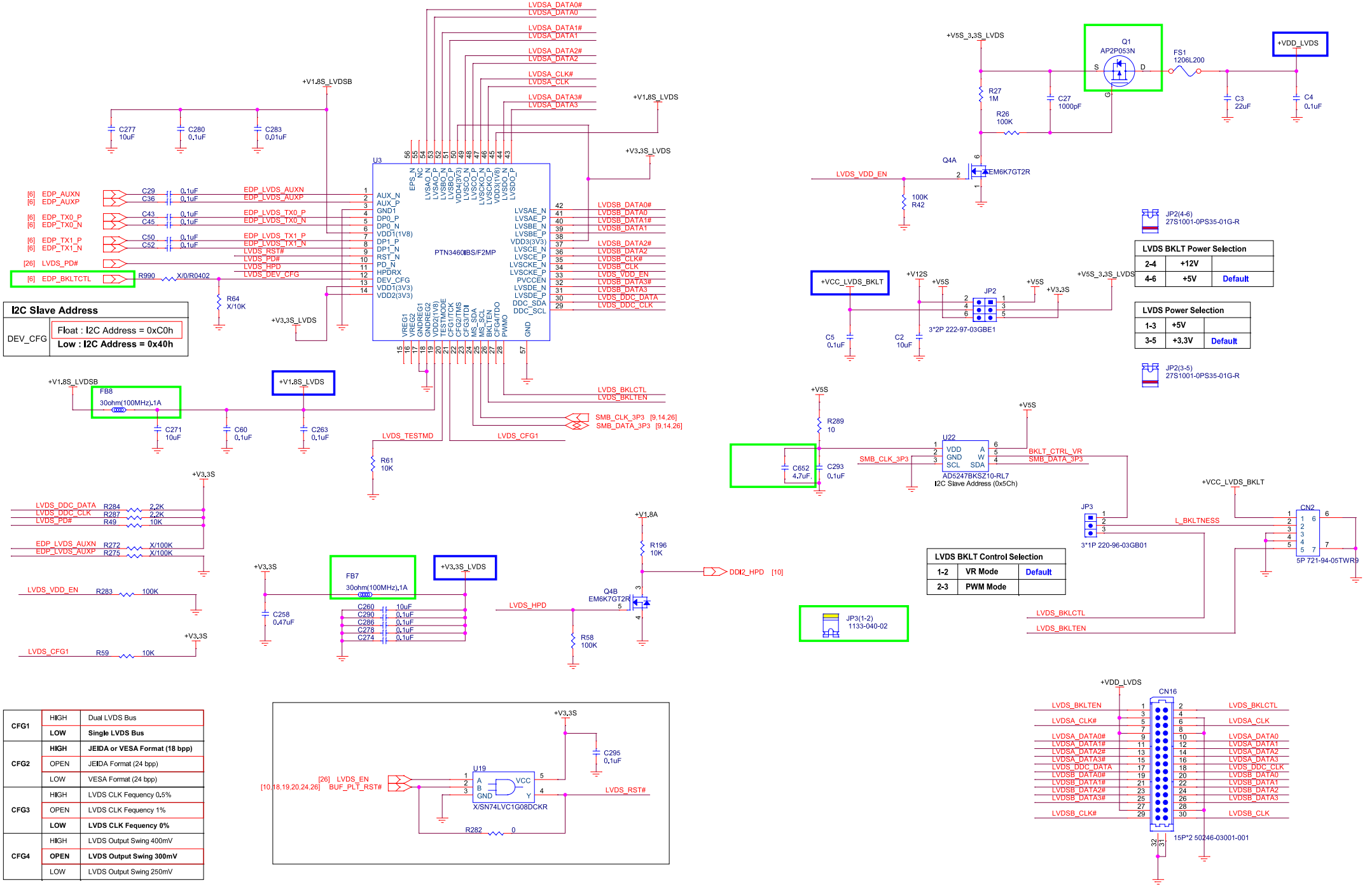
<Variant Name>

AAEON an ASUS assoc. co.	Title: **Level Shift**		
	Size: B	Document Number: **PICO-APL2**	Rev: **A1.0_0_0**
	Date: *Monday, September 26, 2022*		Sheet: **15** of **32**

HDMI

APL2 A1.0





CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

<Variant Name>

AAEON an ASUS assoc. co.

Title: PTN3460 eDP to LVDS		
Size: Custom	Document Number: PICO-APL2	Rev: A1.0_0_0
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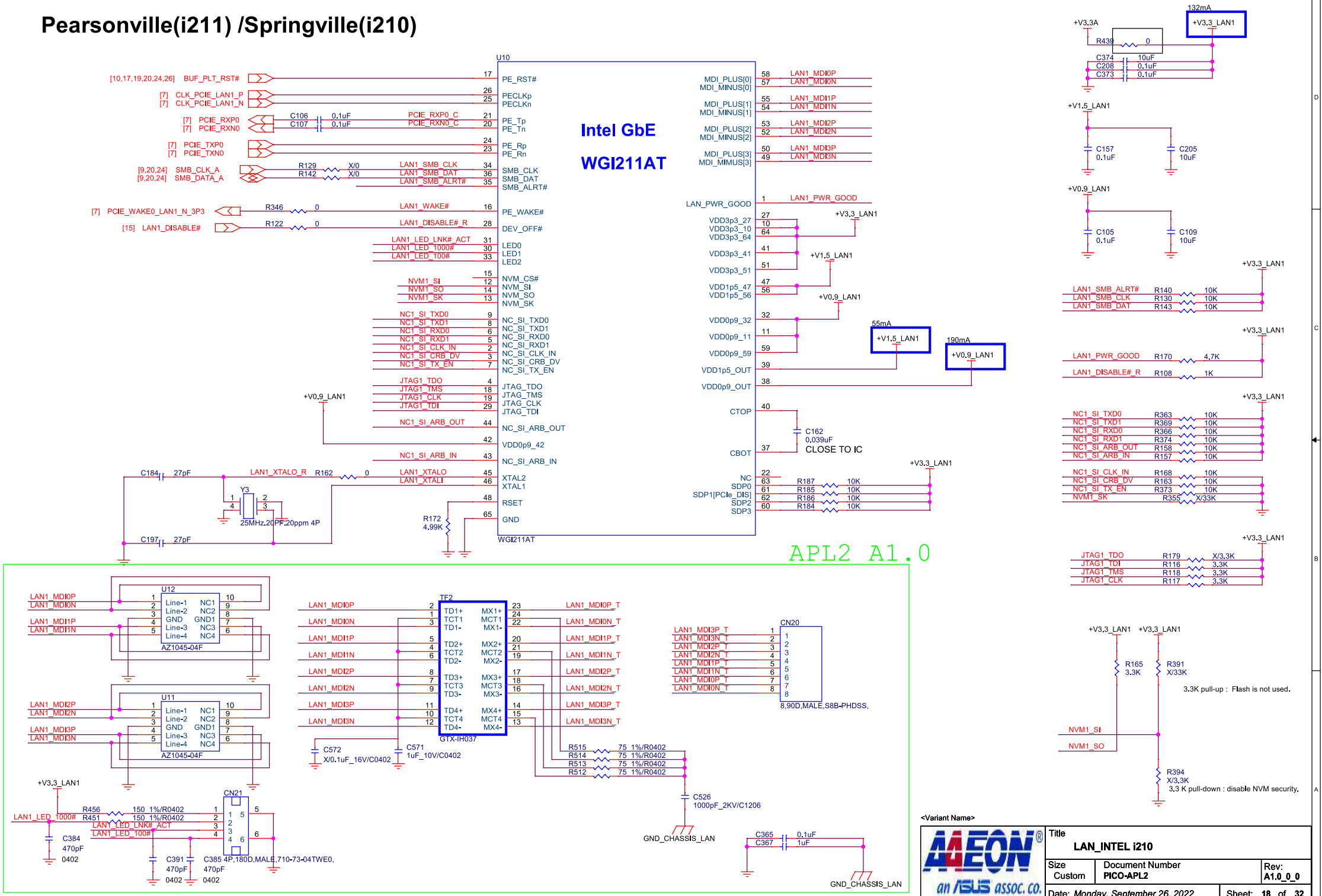
Pearsonville(i211) /Springville(i210)



<Variant Name>

AAEON an ASUS assoc. co.	Title: LAN_INTEL i210	
Size: Custom	Document Number: PICO-APL2	Rev: A1.0_0_0
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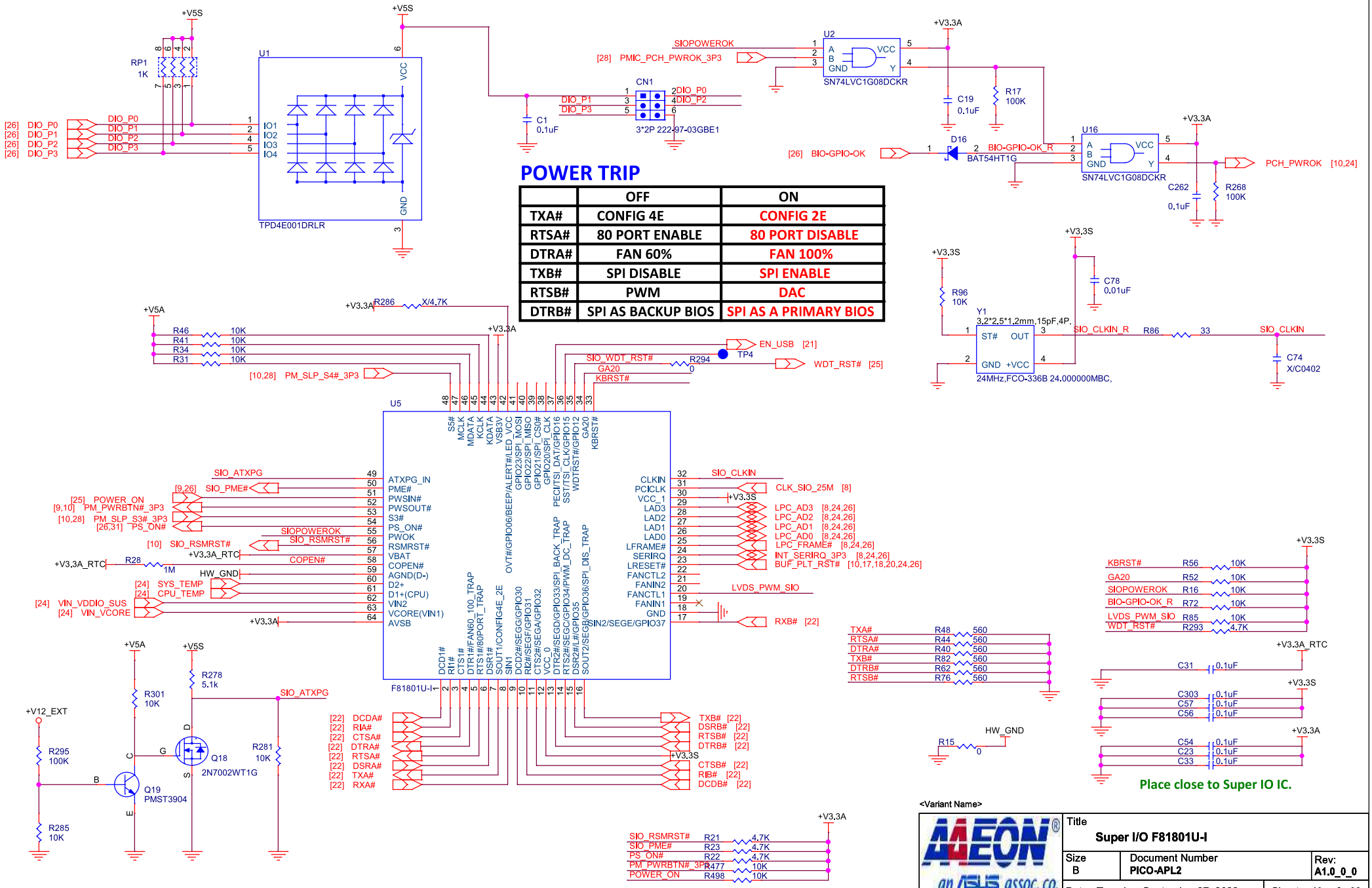
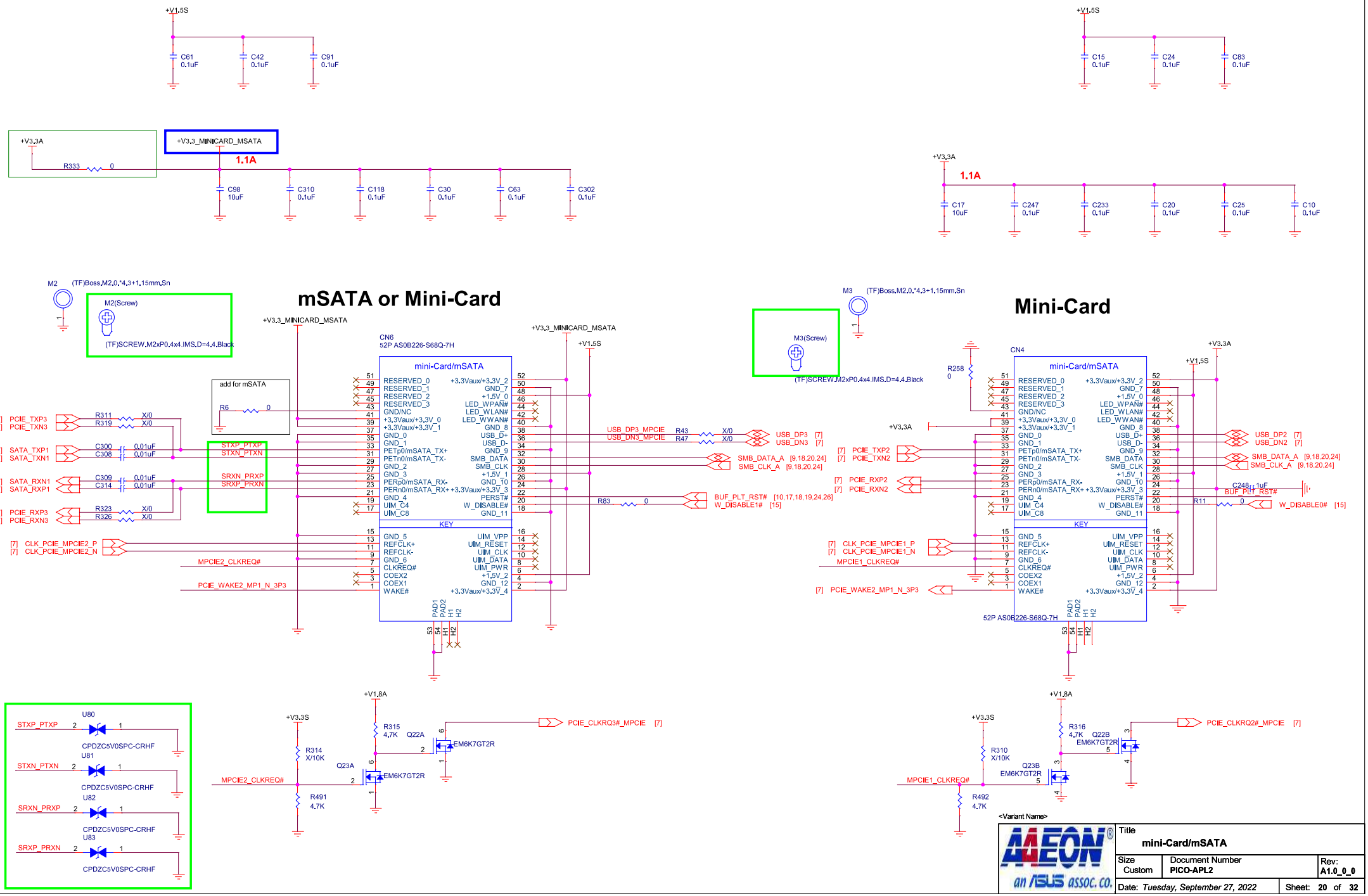


POWER TRIP

	OFF	ON
TXA#	CONFIG 4E	CONFIG 2E
RTSA#	80 PORT ENABLE	80 PORT DISABLE
DTRA#	FAN 60%	FAN 100%
TXB#	SPI DISABLE	SPI ENABLE
RTSB#	PWM	DAC
DTRB#	SPI AS BACKUP BIOS	SPI AS A PRIMARY BIOS


mSATA or Mini-Card
Mini-Card
+V1.5S
C61 0.1uF
C42 0.1uF
C91 0.1uF
C15 0.1uF
C24 0.1uF
C83 0.1uF
+V3.3A
R333 0
+V3.3_MINICARD_MSATA
1.1A
C98 10uF
C310 0.1uF
C118 0.1uF
C30 0.1uF
C63 0.1uF
C302 0.1uF
C17 10uF
C247 0.1uF
C233 0.1uF
C20 0.1uF
C25 0.1uF
C10 0.1uF
M2 (TF)Boss.M2.0.*4.3+1.15mm.Sn
M2(Screw)
(TF)SCREW.M2xP0.4x4.IMS.D=4.4.Black
M3 (TF)Boss.M2.0.*4.3+1.15mm.Sn
M3(Screw)
(TF)SCREW.M2xP0.4x4.IMS.D=4.4.Black
CN6
52P AS0B226-S68Q-7H
CN4
mini-Card/mSATA
add for mSATA
R6 0
R258 0
[7] PCIE_TXP3
[7] PCIE_TXN3
R311 X/0
R319 X/0
[7] SATA_TXP1
[7] SATA_TXN1
C300 0.01uF
C308 0.01uF
[7] SATA_RXN1
[7] SATA_RXP1
C309 0.01uF
C314 0.01uF
[7] PCIE_RXP3
[7] PCIE_RXN3
R323 X/0
R326 X/0
STXP_PTXP
STXN_PTXN
SRXN_PRXP
SRXP_PRXN
[7] CLK_PCIE_MPCIE2_P
[7] CLK_PCIE_MPCIE2_N
MPCIE2_CLKREQ#
PCIE_WAKE2_MP1_N_3P3
USB_DP3_MPCIE
USB_DN3_MPCIE
R43 X/0
R47 X/0
USB_DP3 [7]
USB_DN3 [7]
SMB_DATA_A [9,18,20,24]
SMB_CLK_A [9,18,20,24]
R83 0
BUF_PLT_RST# [10,17,18,19,24,26]
W_DISABLE1# [15]
[7] PCIE_TXP2
[7] PCIE_TXN2
[7] PCIE_RXP2
[7] PCIE_RXN2
USB_DP2 [7]
USB_DN2 [7]
SMB_DATA_A [9,18,20,24]
SMB_CLK_A [9,18,20,24]
C248 1uF
BUF_PLT_RST#
R11 0
W_DISABLE0# [15]
[7] CLK_PCIE_MPCIE1_P
[7] CLK_PCIE_MPCIE1_N
MPCIE1_CLKREQ#
[7] PCIE_WAKE2_MP1_N_3P3
+V3.3_MINICARD_MSATA
+V1.5S
+V3.3A
U80
STXP_PTXP
CPDZC5V0SPC-CRHF
U81
STXN_PTXN
CPDZC5V0SPC-CRHF
U82
SRXN_PRXP
CPDZC5V0SPC-CRHF
U83
SRXP_PRXN
CPDZC5V0SPC-CRHF
+V1.8A
+V3.3S
R315 4.7K
Q22A
EM6K7GT2R
PCIE_CLKRQ3#_MPCIE [7]
R314 X/10K
Q23A
EM6K7GT2R
MPCIE2_CLKREQ#
R491 4.7K
R316 4.7K
Q22B
EM6K7GT2R
PCIE_CLKRQ2#_MPCIE [7]
R310 X/10K
Q23B
EM6K7GT2R
MPCIE1_CLKREQ#
R492 4.7K
<Variant Name>
AAEON
an ASUS assoc. co.
Title
mini-Card/mSATA
Size Custom
Document Number PICO-APL2
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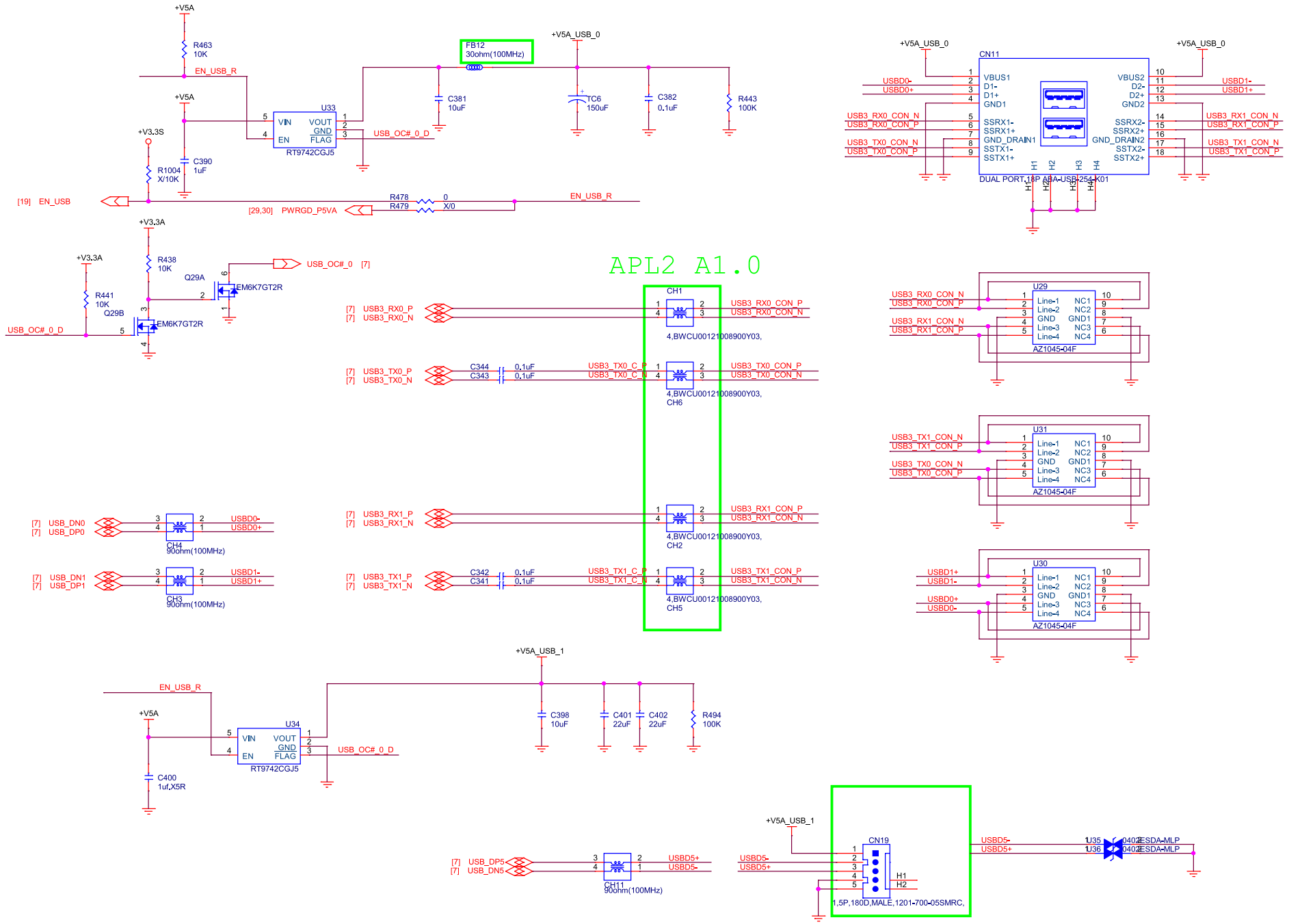
USB3.0 x 2



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AAEON an ASUS assoc. co.	Title: USB 3.0/2.0 PORT	
Size: Custom	Document Number: PICO-APL2	Rev: A1.0_0_0
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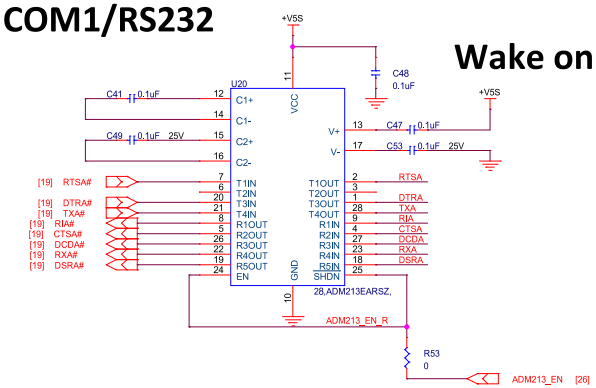
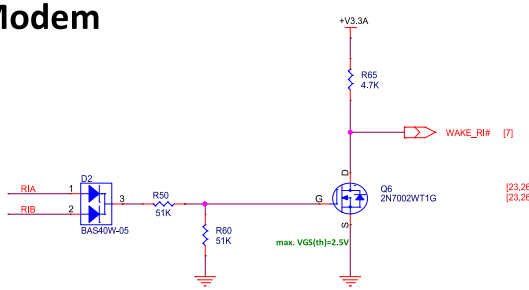
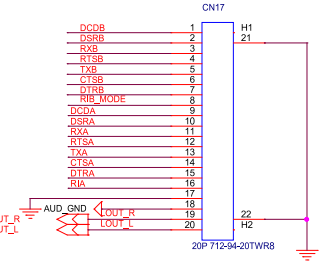
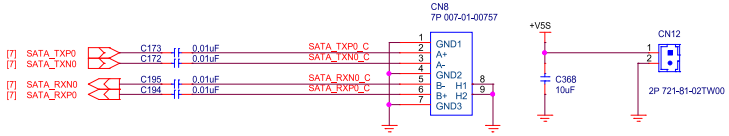
COM1/RS232

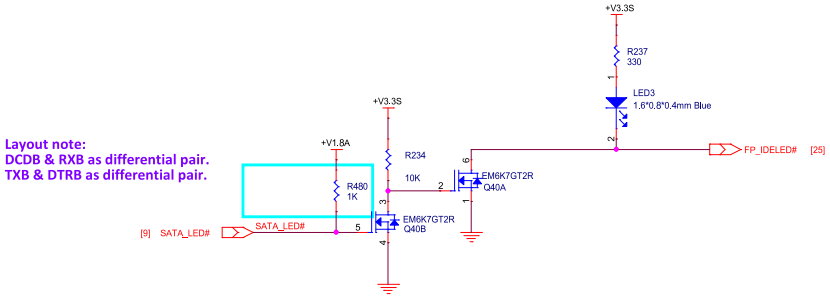


Wake on Modem



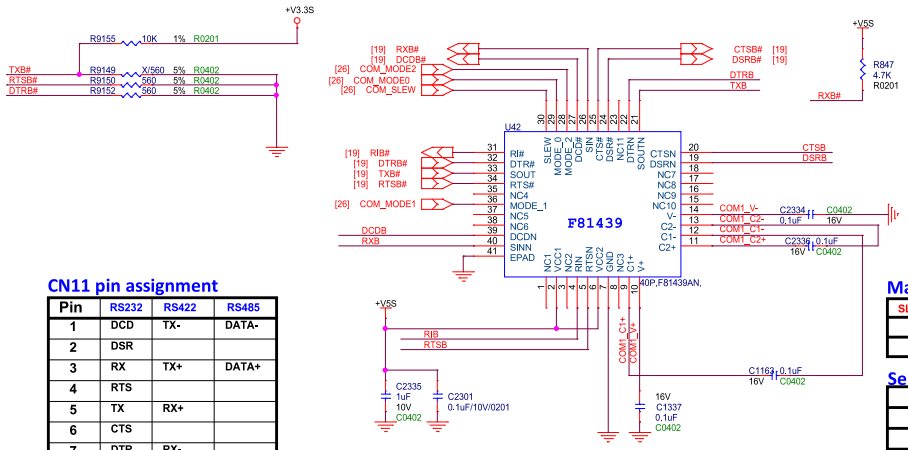




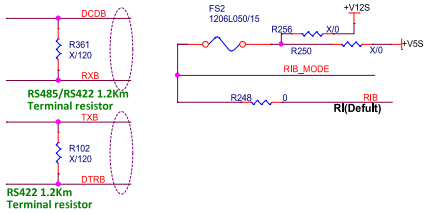


Layout note:
DCDB & RXB as differential pair.
TXB & DTRB as differential pair.

COM2/ RS232/RS422/RS485



Change to F81439 for RS232/422/485
F81437 for RS232 only



CN2 COM Port pin mapping

CN2		RS422	RS485	DB-9 Con.
5	DCD1	TX1-	DATA1-	COM1_1
7	RX1	TX1+	DATA1+	COM1_2
9	TX1	RX1+		COM1_3
11	DTR1	RX1-		COM1_4
3	GND			COM1_5
13	DSR1			COM1_6
15	RTS1			COM1_7
17	CTS1			COM1_8
19	RI1			COM1_9
6	DCD2	TX2-	DATA2-	COM2_1
8	RX2	TX2+	DATA2+	COM2_2
10	TX2	RX2+		COM2_3
12	DTR2	RX2-		COM2_4
3	GND			COM2_5
14	DSR2			COM2_6
16	RTS2			COM2_7
18	CTS2			COM2_8
20	RI2			COM2_9

CN11 pin assignment

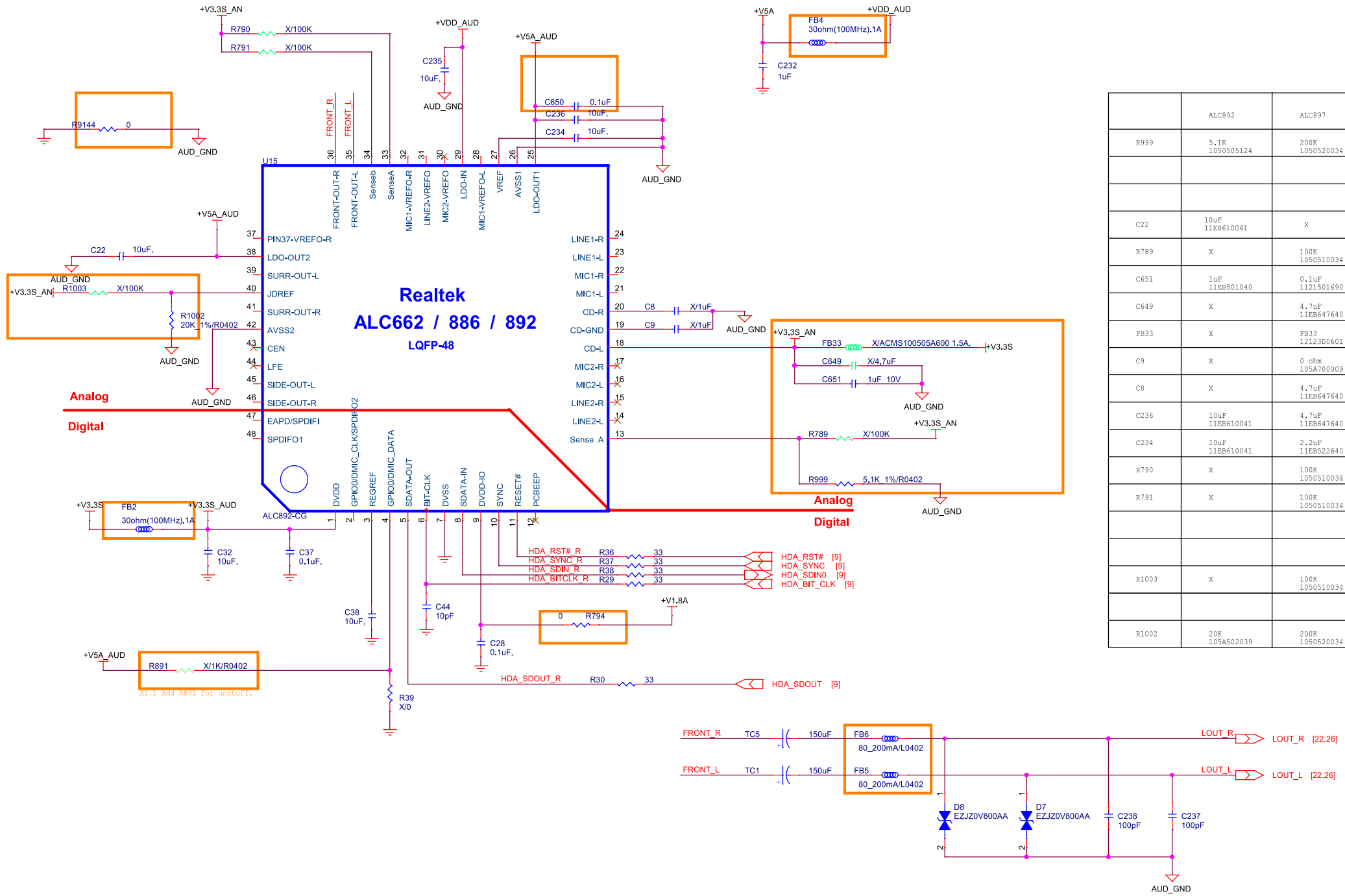
Pin	RS232	RS422	RS485
1	DCD	TX-	DATA-
2	DSR		
3	RX	TX+	DATA+
4	RTS		
5	TX	RX+	
6	CTS		
7	DTR	RX-	
8	RI		

Maximum Data Rate

SLEW	RS232	RS422/RS485
0	250kbps	250kbps
1	1.5Mbps	10Mbps

Serial Port 1 Mode Selection

Mode	MODE_0	MODE_1	MODE_2
RS-422	0	0	0
RS-232	0	0	1
RS-485 (Driver Half Duplex)	0	1	0
RS-485 (Receiver Half Duplex)	0	1	1
Shutdown MODE	1	X	X



	ALC892	ALC897
R999	5.1K 1050505124	200K 1050520034
C22	10uF 11EB610041	X
R789	X	100K 1050510034
C651	1uF 11EB501040	0.1uF 1121501690
C649	X	4.7uF 11EB647640
FB33	X	FB33 12123D0601
C9	X	0 ohm 105A700009
C8	X	4.7uF 11EB647640
C236	10uF 11EB610041	4.7uF 11EB647640
C234	10uF 11EB610041	2.2uF 11EB522640
R790	X	100K 1050510034
R791	X	100K 1050510034
R1003	X	100K 1050510034
R1002	20K 105A502039	200K 1050520034

<Variant Name>

AAEON an ASUS assoc. co.

Title: HD Audio - ALC892

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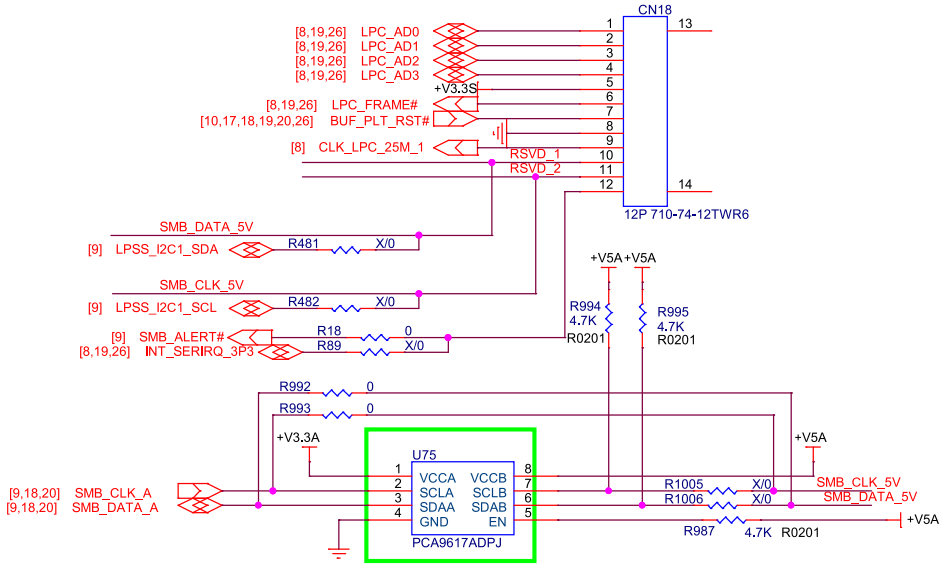
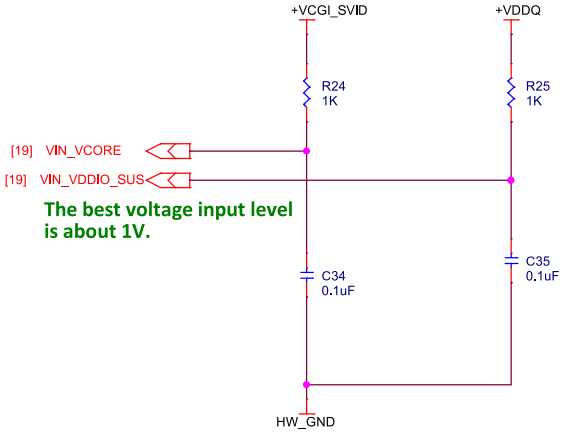
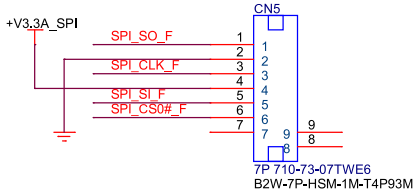
LPC Debug Connector

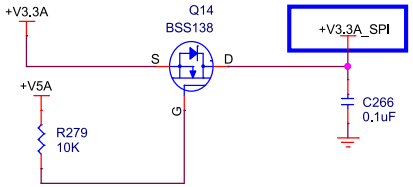


Voltage Monitor(Vcore, Vmem)

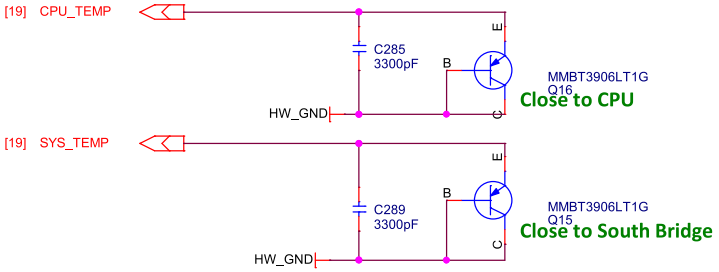


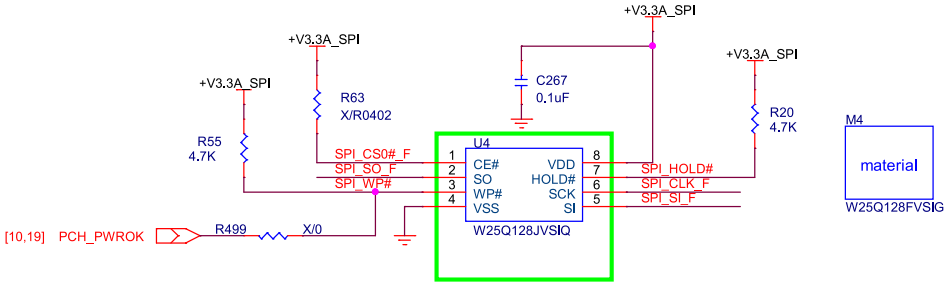
The best voltage input level is about 1V.



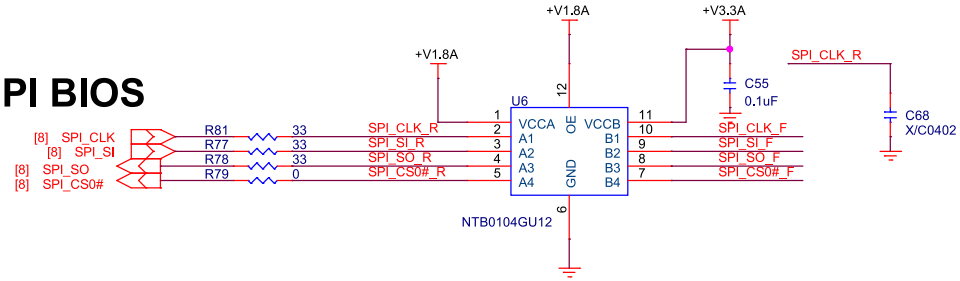


Temperature Monitor(CPU, SYS)





SPI BIOS



8 pin : 1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0
1462001280 (TF)IC.Flash Memory.128M Bit serial.SOIC-8(208mil).SMD.w/ Dual & Quad SPI.Winbond.W25Q128FVSIG

<Variant Name>

AAEON an ASUS assoc. co.	Title: H/W Mon/ Debug /CMOS		
	Size: B	Document Number: PICO-APL2	Rev: A1.0_0_0
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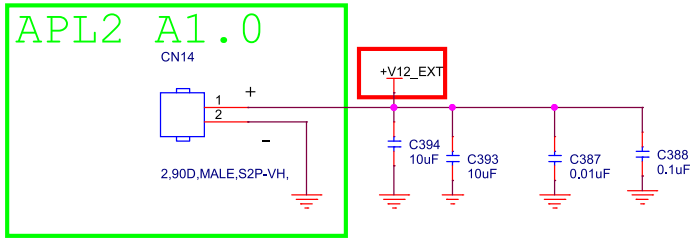
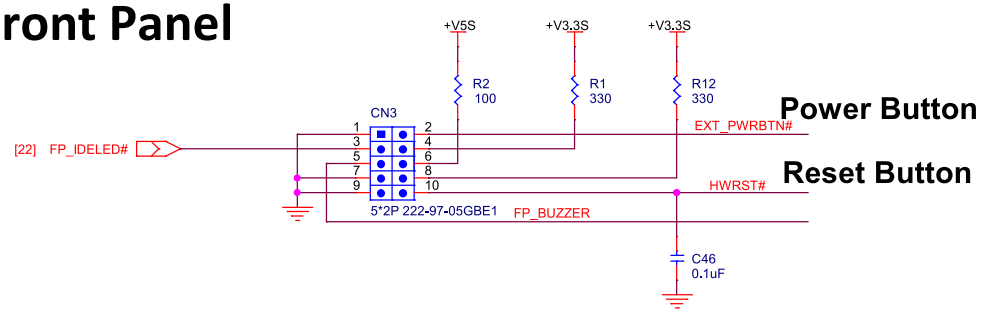
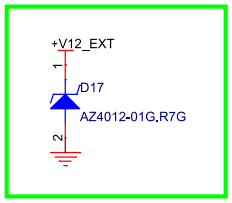
+12V Power Input

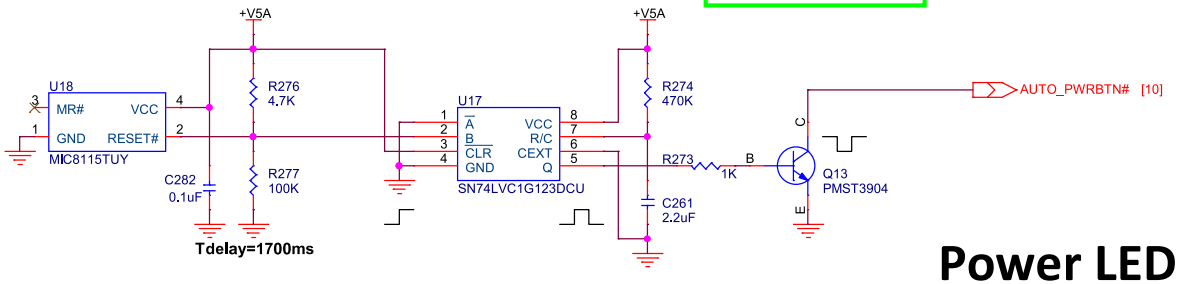


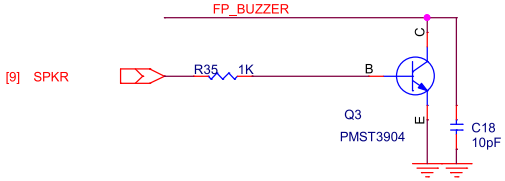
Front Panel



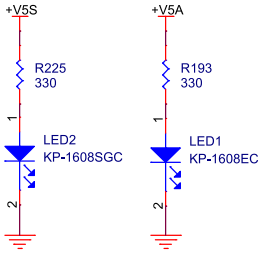


Auto Power Button

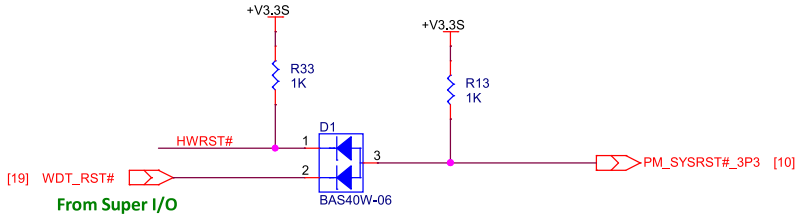


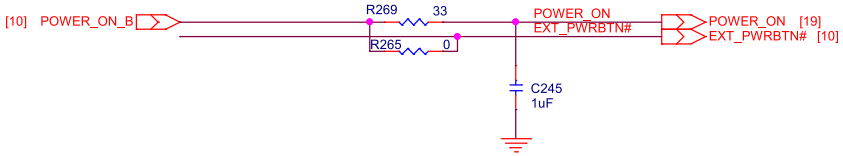


Power LED

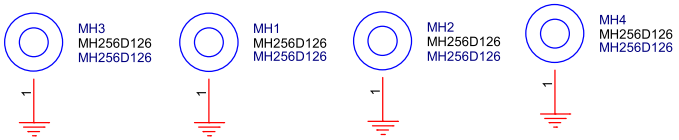


System Reset





Mounting Holes / Non-PTH



<Core Design>

AAEON an ASUS assoc. co.	Title: Auto Power Button/Power in		
	Size: B	Document Number: PICO-APL2	Rev: A1.0_0_0
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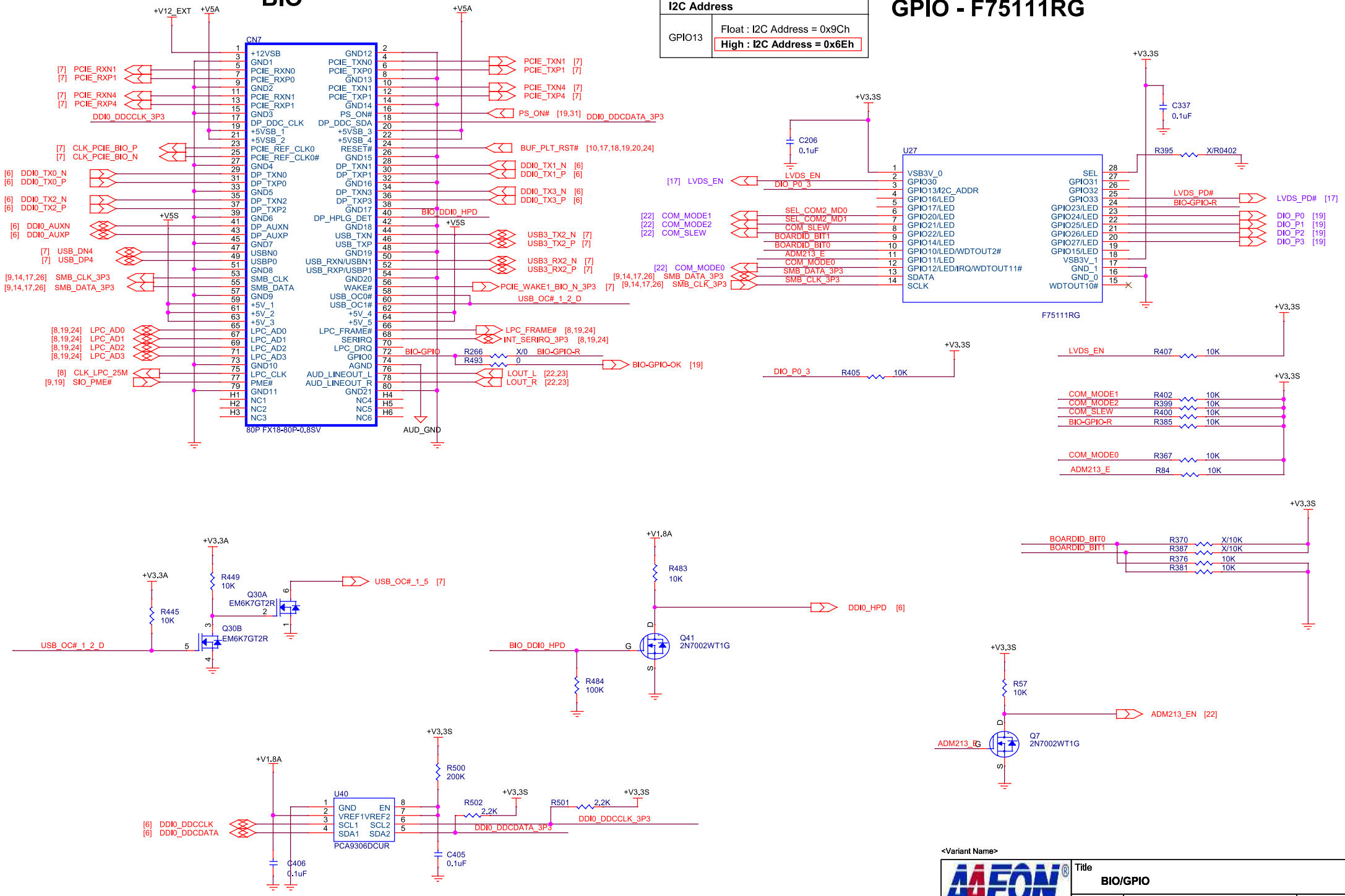
BIO

GPIO - F75111RG

I2C Address	
GPIO13	Float : I2C Address = 0x9Ch **High : I2C Address = 0x6Eh**



<Variant Name>

AAEON an ASUS assoc. co.	Title: BIO/GPIO	
Size: Custom	Document Number: PICO-APL2	Rev: A1.0_0_0
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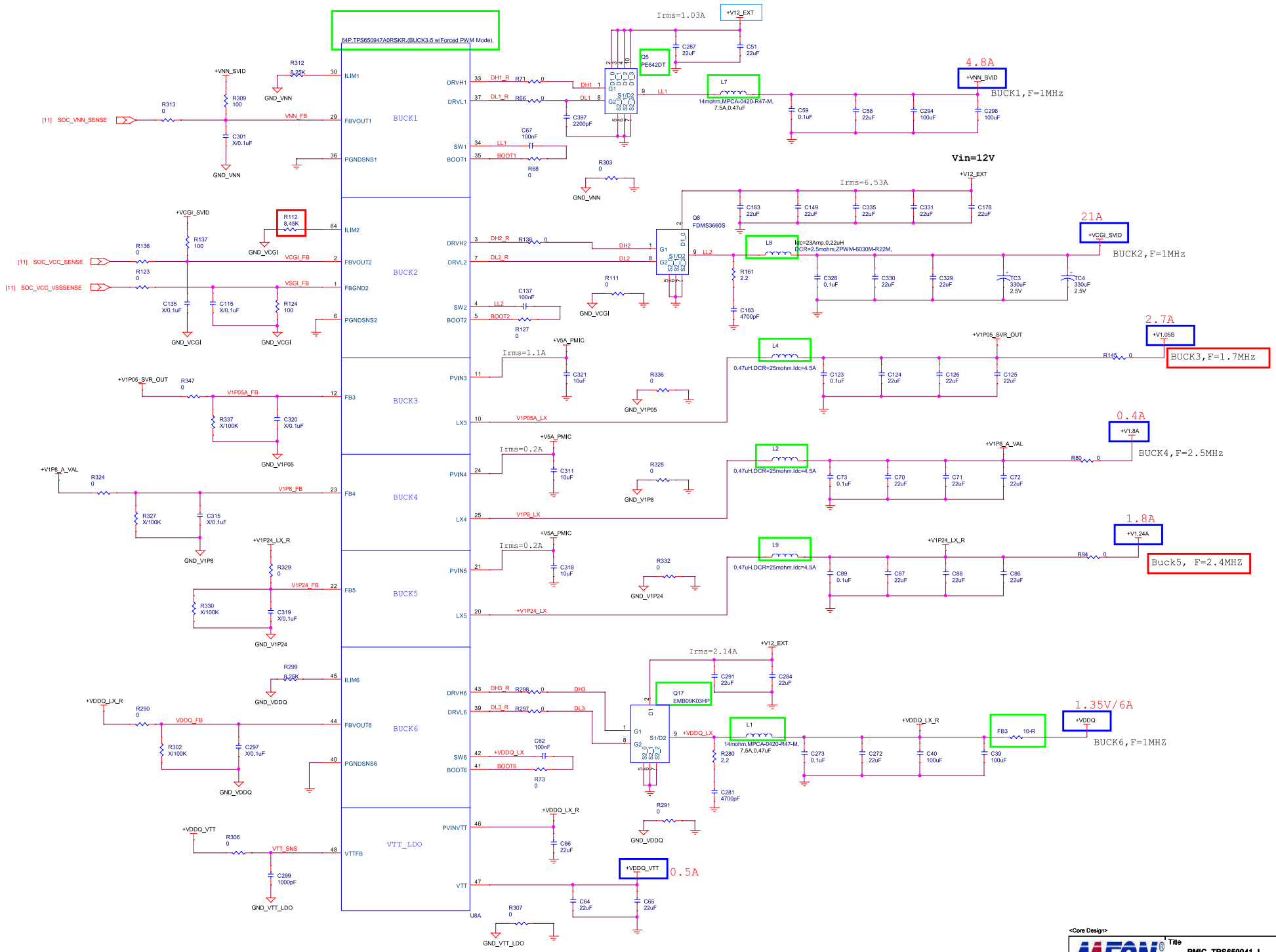

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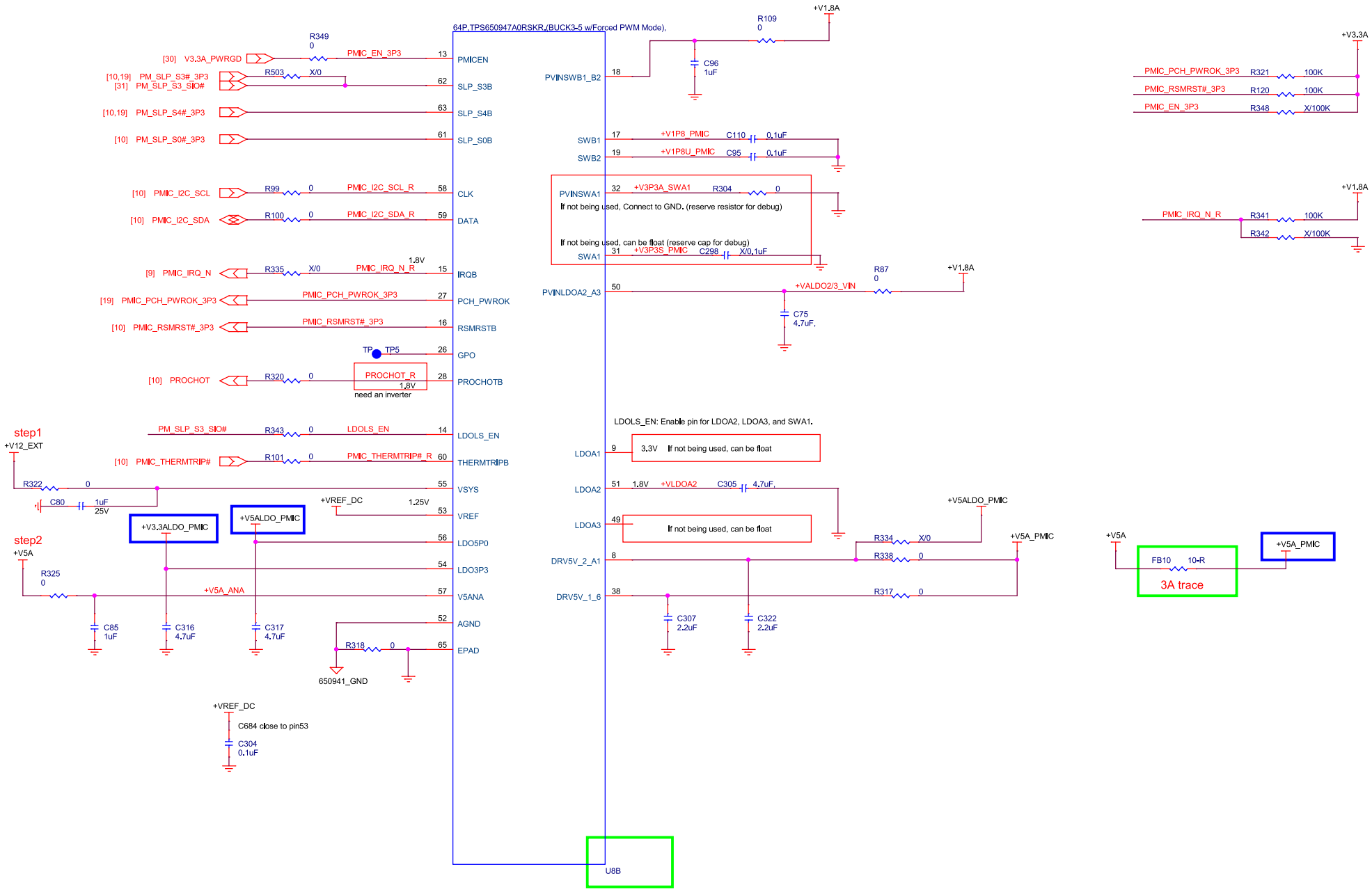

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