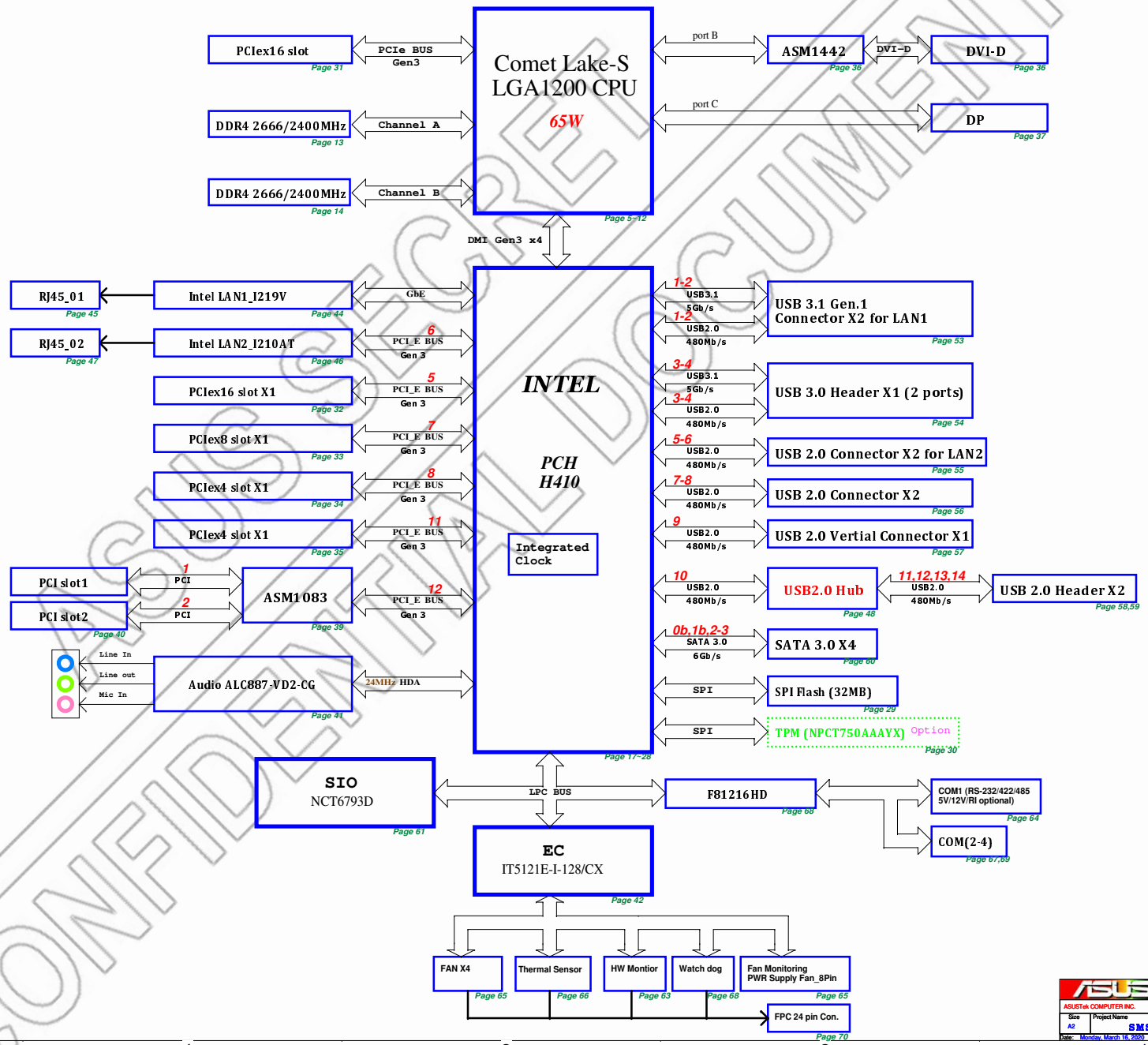
# SMS-H410-A10
# Block Diagram

Rev 1.00

| SMS-H410 EVT SKU | 60 BOM P/N | CPU P/N | PCH P/N |
|---|---|---|---|
| SMS-H410-A10 | Location | LGA1200 | SU1 |
| | | 12001-00280300 | 02001-00751700 |

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CONFIDENTIAL DOCUMENT

Title : Block Diagram
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size A2 | Project Name SMS-H410 | Rev 1.00
Date: Monday, March 16, 2020 | Sheet 1 of 87

## CML-S PCH-V H410_CPU GPIO

Intel CML PCH-V C.0 FH80HH10 A0 B1A8E 0S
1st : P/N : 03001-00751700 INTEL CML H410 QTAW-9998MSA

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_A0 | SCI#0 | Native | O_KB_RST# | | PU 8.2K | +3V |
| GPP_A1 | LAD0 | Native | F_LAD0 | | PU 2.7K(/x) | +3V |
| GPP_A2 | LAD1 | Native | F_LAD1 | | PU 2.7K(/x) | +3V |
| GPP_A3 | LAD2 | Native | F_LAD2 | | PU 2.7K(/x) | +3V |
| GPP_A4 | LAD3 | Native | F_LAD3 | | PU 2.7K(/x) | +3V |
| GPP_A5 | LFRAME# | Native | F_FRAME# | | | |
| GPP_A6 | SERIRQ | Native | F_SERIRQ# | | PU 8.2K | +3V |
| GPP_A7 | PIRQA# | Native | S_PIRQA# (MBC750/IRM) | | PU 8.2K | +3V |
| GPP_A8 | CLKRUN# | Native | S_CLKRUN# | | PU 8.2K(/x) | +3V |
| GPP_A9 | CLKOUT_LPC0 | Native | C_24M_CLK_R | | | |
| GPP_A10 | CLKOUT_LPC1 | Native | C_24M_CLK2_R(TP_HT147) | | | |
| GPP_A11 | PME# | GPO | PME# | | PU 10K | +3VSB_ATX |
| GPP_A12 | GPI | Native | SX_EXIT_HOLDOFF# | | PU 10K | +3VSB_ATX |
| GPP_A13 | SUSWARN# | Native | SUSWARN# | | PU 10K | +3VSB_ATX |
| GPP_A14 | SUS_STAT# | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A15 | SUS_ACK# | Native | SUSACK# | | | |
| GPP_A16 | Native/GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A17 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A18 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A19 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A20 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A21 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A22 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_A23 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_B0 | GPO | GPO | TP_GPP_B0(TP_ST110) Set GPO Low | | | |
| GPP_B1 | GPI | GPO | TP_GPP_B1(TP_ST109) Set GPO Low | | | |
| GPP_B2 | GPI | GPO | VR_ALERT# Set GPO Low | | PU 8.2K | +3VSB_ATX |
| GPP_B3 | GPI | GPO | NA (No Use) | | | |
| GPP_B4 | GPI | GPO | EXTT5_PRI_DRV1_PCH | | PU 8.2K | +3V |
| GPP_B5 | GPI | Native | SRCCLKREQ0# | | PU 8.2K | +3VSB_ATX |
| GPP_B6 | GPI | Native | SRCCLKREQ1# | | PU 8.2K | +3V |
| GPP_B7 | GPI | Native | SRCCLKREQ2# | | PU 8.2K | +3V |
| GPP_B8 | GPI | GPO | CLK_REQ3_4GLTE# | | PU 8.2K | +3V |
| GPP_B9 | GPI | Native | SRCCLKREQ4# | | PU 8.2K | +3V |
| GPP_B10 | GPI | GPO | SRCCLKREQ5# Mobile/PC | | PU 10K | +3VSB_ATX |
| GPP_B11 | GPO | GPO | TP_GPP_B11(TP_ST112) Set GPO Low | | | |
| GPP_B12 | SLP_S0# | Native | SLP_S0#(TP_ST113) | | | |
| GPP_B13 | PLTRST# | Native | S_PLTRST# | | PU 10K(/x) | +3V |
| GPP_B14 | GPO | GPO | S_SPEN Mobile | | PU 10K(/x) Mobile | +3V |
| GPP_B15 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_B16 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_B17 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_B18 | GPO | GPO | LPSS_GSPI0_MOSI | PD | PD 15K(/x) Mobile/PC | +3V |
| GPP_B19 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_B20 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_B21 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_B22 | GPO | GPO | LPSS_GSPI1_MOSI | PD | PD 15K(/x) Mobile/PC | +3V |
| GPP_B23 | GPO | Native | PCH_BUZ# | PD | PD 15K(/x) Mobile/PC | +3VSB_ATX |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_C0 | SMBCLK | Native | S_SMBCLK_PCH | | PU 2.7K(/x) | +3VSB_ATX |
| GPP_C1 | SMBDATA | Native | S_SMBDATA_PCH | | PU 1K | +3VSB_ATX |
| GPP_C2 | GPO | GPO | S_WG_ALERT# | PD | PU 4.7K | +3VSB_ATX |
| GPP_C3 | SMLOCLK | Native | L1_SMBCLK Mobile/PC | | PU 499 | +3VSB_ATX |
| GPP_C4 | SMLODATA | Native | L1_SMBDATA Mobile/PC | | PU 499 | +3VSB_ATX |
| GPP_C5 | GPO | GPO | ESPI_LPC#_SEL | PD | PD 8.2K(/x) Mobile/PC | +3VSB_ATX |
| GPP_C6 | SMLICLK | Native | O_SMBL_CLK MCTS750 | | PU 8.2K | +3VSB_ATX |
| GPP_C7 | SMLIDATA | Native | O_SMBL_DATA MCTS750 | | PU 8.2K | +3VSB_ATX |
| GPP_C8 | GPI | GPO | LPSS_UART0_RXD NA (No Use) Set GPO Low | | PU 49.9K | +3V |
| GPP_C9 | GPI | GPO | LPSS_UART0_TXD NA (No Use) Set GPO Low | | PU 49.9K | +3V |
| GPP_C10 | GPI | GPO | LPSS_UART0_RTS# NA (No Use) Set GPO Low | | PU 49.9K | +3V |
| GPP_C11 | GPI | GPO | LPSS_UART0_CTS# NA (No Use) Set GPO Low | | PU 49.9K | +3V |
| GPP_C12 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C13 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C14 | GPI | GPO | M2_CONFIG1/PRESENT# 2280 M.2 SSD_M Type | | PU 8.2K | +3V |
| GPP_C15 | GPI | Native | GPP_H15 | PU 100K | PU10K Mobile/PC | +3VSB_ATX |
| GPP_C16 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C17 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C18 | GPI | GPO | 12C1_SDA NA (No Use) Set GPO Low | | PU 4.7K | +3V |
| GPP_C19 | GPI | GPO | 12C1_SCL NA (No Use) Set GPO Low | | PU 4.7K | +3V |
| GPP_C20 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C21 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C22 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_C23 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_D0 | GPI | GPO | GPP_D0 Set GPO Low | | | |
| GPP_D1 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D3 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D4 | GPI | GPO | 12C3_SDA NA (No Use) Set GPO Low | | PU 4.7K | +3V |
| GPP_D5 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D6 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D7 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D8 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D9 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D10 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D11 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D12 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D13 | GPI | GPO | 12C2_SDA NA (No Use) Set GPO Low | | PU 4.7K | +3V |
| GPP_D14 | GPI | GPO | 12C2_SCL NA (No Use) Set GPO Low | | PU 4.7K | +3V |
| GPP_D15 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D16 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D17 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D18 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D19 | GPI Mobile | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D20 | GPI Mobile | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D21 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D22 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_D23 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_E0 | GPI | GPO | O_SMI# | | PU 8.2K(/x) | +3V |
| GPP_E1 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_E2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_E3 | GPI | GPI | EXTT5_SRI_DRV0_PCH | | PU 8.2K | +3V |
| GPP_E4 | GPI | GPO | NA (Reserved 1R63) | | | |
| GPP_E5 | GPO | GPO | NA (No Use) | | | |
| GPP_E6 | GPI | GPO | O_PME# | | PU 8.2K | +3V |
| GPP_E7 | GPI | GPI | NA (TCO_PLDS_EVENT_NO2 | | PU 3.3K(/x) | +3V |
| GPP_E8 | GPI | GPO | T_SATALED# | | PU 8.2K | +3V |
| GPP_E9 | GPI | GPI | U_USBOC#12 | | PU 4.7K | +5V |
| GPP_E10 | GPI | GPI | U_USBOC#14 | | PU 4.7K | +5V |
| GPP_E11 | GPI | GPI | U_USBOC#16 | | PU 4.7K | +5V |
| GPP_E12 | GPI | GPI | U_USBOC#18 | | PU 4.7K | +5V |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_F0 | GPI | Native | SATA_GP3 NA (No Use) Set GPO Low | | PU 8.2K | +3V |
| GPP_F1 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F3 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F4 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F5 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F6 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F7 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F8 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F9 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F10 | GPI | GPO | CRB_PCH_CPU_IP(Reserved TP_ST71) | | | |
| GPP_F11 | GPI | GPO | CRB_PCH_RSVD(Reserved TP_ST72) | | | |
| GPP_F12 | GPI | GPO | CRB_PCH_STYLE Intel CRB:High | | PU8.2K Mobile/PC | +3V |
| GPP_F13 | GPI | GPO | CRB_GFX_SEL Intel CRB:Low | | PU8.2K Mobile/PC | +3V |
| GPP_F14 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F15 | GPI | GPO | U_USBOC#3 USB3.Port | | PU 4.7K | +5V |
| GPP_F16 | GPI | GPO | USB3_OCB_5 | | PU 8.2K | +3VSB_ATX |
| GPP_F17 | GPI | GPO | USB3_OCB_6 | | PU 8.2K | +3VSB_ATX |
| GPP_F18 | GPI | GPO | USB3_OCB_7 | | PU 8.2K | +3VSB_ATX |
| GPP_F19 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F20 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F21 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_F22 | GPI | GPI | R_SATOCC# | | PU 2K | +3V_BAT |
| GPP_F23 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_G0 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G1 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G3 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G4 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G5 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G6 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_G7 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_H0 | GPI | Native | SRCCLKREQ6# | | PU 8.2K | +3V |
| GPP_H1 | GPI | Native | CLK_REQ7_M.2_SSD# M.2 SSD | | PU 8.2K | +3V |
| GPP_H2 | GPI | Native | SRCCLKREQ8# | | PU 8.2K | +3V |
| GPP_H3 | GPI | Native | SRCCLKREQ9# | | PU 8.2K | +3V |
| GPP_H4 | GPI | Native | SRCCLKREQ10# | | PU 8.2K | +3V |
| GPP_H5 | GPI | Native | SRCCLKREQ11# | | PU 8.2K | +3V |
| GPP_H6 | GPI | Native | SRCCLKREQ12# | | PU 8.2K | +3V |
| GPP_H7 | GPI | Native | SRCCLKREQ13# | | PU 8.2K | +3V |
| GPP_H8 | GPI | Native | SRCCLKREQ14# | | PU 8.2K | +3V |
| GPP_H9 | GPI | Native | SRCCLKREQ15# | | PU 8.2K | +3V |
| GPP_H10 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H11 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H12 | GPO | GPO | GPP_R_12 | PD 20K | PU8.2K(/x) Mobile/PC | +3VSB_ATX |
| GPP_H13 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H14 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H15 | GPI | Native | GPP_H15 | PU 100K | PU10K Mobile/PC | +3VSB_ATX |
| GPP_H16 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H17 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H18 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H19 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H20 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H21 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H22 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_H23 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_I0 | GPI | GPO | S_BP_R_HPD | | | |
| GPP_I1 | GPI | GPO | S_HDMI_C_HPD HDMI | | | |
| GPP_I2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_I3 | GPI | GPI | S_DP2VGA_HPD VGA | | PD 100K | |
| GPP_I4 | GPO | GPO | TP_GPP_I4(TP-HT158) | | | |
| GPP_I5 | GPI | Native | S_TM_R_CTRL_DATA | | PU 8.2K | +3V |
| GPP_I6 | GPO | Native | S_DP_R_CTRL_DATA | | PU 8.2K | +3V |
| GPP_I7 | GPI | Native | S_HDMI_C_CTRL_DATA | | PU 8.2K | +3V |
| GPP_I8 | GPO | Native | S_TMDI_C_CTRL_DATA | | PU 8.2K | +3V |
| GPP_I9 | GPI | GPO | S_DVI_D_CTRL_CLK(TP-HT151) | | PU 8.2K | +3V |
| GPP_I10 | GPI | GPO | S_DVI_D_CTRL_DATA(TP-HT152) | | PU 8.2K | +3V |
| GPP_I11 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_I12 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_I13 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_I14 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_J0 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_J1 | GPI | GPO | GPP_J1 | | PD 47K | |
| GPP_J2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_J3 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_J4 | CNV_RGI_DT | Native | GPP_J4 CNVi WLAN | | PD 20K(/x) Mobile/PC | +3V_SVSB_LDO |
| GPP_J5 | CNV_RGI_RSP | Native | NA (No Use) Set GPO Low | | | |
| GPP_J6 | CNV_BGI_DT | Native | GPP_J6 CNVi BT | | PD 20K(/x) Mobile/PC | +3V_SVSB_LDO |
| GPP_J7 | CNV_BGI_RSP | Native | NA (No Use) Set GPO Low | | | |
| GPP_J8 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_J9 | GPO | GPO | NA (No Use) Set GPO Low | | | |
| GPP_J10 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_J11 | A4WP_PRESENT | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPP_K0 | GPI | GPO | GPP_GPP_K0 | | PU 8.2K | +3V |
| GPP_K1 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K2 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K3 | GPI | GPO | CRB_GC_SCI# | | PU 8.2K | +3V |
| GPP_K4 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K5 | GPI | GPO | GPP_SV_DET | | PD15K(/x) Mobile/PC | |
| GPP_K6 | GPI | GPO | PCH_GPP_K6_SM | | PU 8.2K | +3V |
| GPP_K7 | GPI | GPO | TP_GPP_K7 | | PU8.2K | +3V |
| GPP_K8 | Reserved | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K9 | Reserved | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K10 | Reserved | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K11 | Reserved | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K12 | GPI | GPO | S_TCO_NO_EXT_HDD | | PU 3.3K(/x) | +3V |
| GPP_K13 | GPI | GPO | TP_SVCAM_RST#(TP-ST41) | | | |
| GPP_K14 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K15 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K16 | GPI | GPO | CRB_PPC_PWR_EN1 | | PU 3.3K(/x) | +3V |
| GPP_K17 | GPI | GPO | GPP_K17(TP-HT113) | | | |
| GPP_K18 | GPI | GPO | GPP_K18(TP-HT148) | | PU 8.2K(/x) | +3V |
| GPP_K19 | GPI | GPO | GPP_K19(TP-HT149) | | PU8.2K(/x) | +3V |
| GPP_K20 | Reserved | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K21 | Reserved | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K22 | GPI | GPO | NA (No Use) Set GPO Low | | | |
| GPP_K23 | GPI | GPO | NA (No Use) Set GPO Low | | | |

| | Default | Use As | Signal Name | INT PUPD | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| GPD0 | BATLOW# | Native | BATLOW# | | PU 8.2K | +3VSB_ADV |
| GPD1 | ACPRESENT | Native | TP_USB_SDW_OD | | PU 8.2K | +3VSB_ADV |
| GPD2 | LAN_WAKE# | Native | L1_LAN_WAKE# Mobile/PC | | PU 4.7K | +3VSB_ATX |
| GPD3 | PWRBTN# | Native | O_PWRBTN# | | PU 1K | +3VSB_ATX |
| GPD4 | SLP_S3# | Native | S_SLP3# | | PU 8.2K(/x) | +3VSB_ATX |
| GPD5 | SLP_S4# | Native | S_SLP34# | | | |
| GPD6 | SLP_A# | Native | S_SLP_A#(TP-ST172) | | | |
| GPD7 | GPO | GPO | PCH_GPD7 | | PU10K Mobile/PC | +3VSB_ATX |
| GPD8 | SUSCLK | Native | PCH_SUSCLK | | PU 8.2K | |
| GPD9 | SLP_WLAN# | GPO | NA (No Use) Set GPO Low | | | |
| GPD10 | SLP_S5# | GPO | S_SLP55#(TP-ST163) | | | |
| GPD11 | LANPHYPC | Native | L1_LAN_DISABLE# Mobile/PC | | PU 10K(/x) | +3VSB_ATX |

## Super IO NCT6793D GPIO

SUPER IO NCT6793D LQFP-128
1st : P/N : 06116-00060000 NUVOTON/SUPER IO NCT6793D LQFP-128

| | ID Port0 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| CMA_FAN2 Control | Pin121 | AUXFANOUT0 | AUXFANOUT0 | O_CHAFAN2_PWR2 | PU 8.2K | +3V |
| | Pin122 | AUXFANOUT1 | DIO_O#1 | DIO_O#1 | PU 10K | +5V |
| | Pin123 | AUXFANOUT2 | DIO_O#2 | DIO_O#2 | PU 10K | +5V |
| | Pin2 | OVT# | DIO_O#3 | DIO_O#3 | PU 10K | +5V |
| CMA_FAN2 RPM | Pin3 | AUXFANIN0 | AUXFANIN0 | O_CHAFANIN0 | Series4.7k+PU 4.7K | +3V |
| | Pin4 | AUXFANIN1 | DIO_O#4 | DIO_O#4 | PU 10K | +5V |
| KB_LED_PWM | Pin5 | AUXFANIN2 | DIO_I#1 | DIO_I#1 | PU 10K | +5V |
| DCR_PWRGD | Pin6 | VFP_PG | DCR_PG | P_+5VPDDR_PG_10 | PU 10K | +3VSB_ATX |

| | ID Port1 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| | Pin14 | GPI | RIB# | O_COM2_RIB# | | |
| COM2 Port | Pin13 | GPI | DCDB# | O_COM2_DCDB# | | |
| COM2 Port | Pin12 | GPI | SOUT2/IRTX | O_COM2_TXD2 | | |
| COM2 Port | Pin11 | GPI | SIN2/IRRX | O_COM2_RXD2 | | |
| COM2 Port | Pin10 | GPI | DTRB# | O_COM2_DTRB# | | |
| COM2 Port | Pin9 | GPI | RTSB# | O_COM2_RTSB# | | |
| COM2 Port | Pin8 | GPI | DSRB# | O_COM2_DSRB# | | |
| COM2 Port | Pin7 | GPI | CTSB# | O_COM2_CTSB# | | |

| | ID Port2 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| Keyboard | Pin59 | KDAT | KDAT | O_KB_DATA (TP-CI48) | | |
| Keyboard | Pin58 | KCLK | KCLK | O_KB_CLK (TP-CI47) | | |
| Mouse | Pin57 | MDAT | MDAT | O_MS_DATA (TP-CI46) | | |
| Mouse | Pin56 | MCLK | MCLK | O_MS_CLK (TP-CI45) | | |
| USBPWR_SWB | Pin95 | CIRRX | GPO | USBPWR_SWB | PU8.1K +3VSB_ATX | +3VSB_ATX |
| | Pin96 | CIRTX | GPO | AMDGPIO_EN (Unused) | PU 1K(/x) | +3VSB_ATX |
| | Pin118 | GPI26 | GPO | GPI26_AD (Unused) | | |
| | Pin98 | GPI27 | DTR_IR# | GPIO_IR# | | |

| | ID Port3 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| ACPI (Unused) | Pin83 | GPI/CIRWUI# | GPO | GPI/CIRWU_PANEXE1 | PU 8.2K | +3V |
| SMBUS | Pin76 | SDA | SDA | SMBUS_DATA | PU 8.2K | +3VSB_ATX |
| SMBUS | Pin75 | SCL | SCL | O_SMBUS_CLK | PU 8.2K | +3VSB_ATX |
| ACPI (Unused) | Pin84 | SWINDW# | GPO | NC (Unused) | | |
| | Pin85 | GPI34 | DIO_I#3 | DIO_I#3 | PU10K | +3V |
| | Pin54 | GPI35 | GPO | NC (Unused) | | +3V |
| Unused | Pin53 | GPI6/ISA | GPO | N21873197 (TP-CI17) | | |

| | ID Port4 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| Unused | Pin103 | GPI40 | GPO | GC/CORESELFIN_R | PD 8K2K | |
| Unused | Pin102 | TMR1/SI/MSCL | GPO | N21872726 (TP-CI72) | | |
| Unused | Pin101 | SIN0/SI/MSDA | GPO | N21872871 (TP-CI73) | | |
| Unused | Pin41 | ACK#/SO/SCL# | GPO | N21873316 (TP-CI74) | | |
| Unused | Pin40 | BUSY/SO/MSDA# | GPO | N21873673 (TP-CI75) | | |
| Unused | Pin39 | PE/SI/TXM_EN | GPO | N21873661 (TP-CI76) | | |
| Unused | Pin38 | MC_UNLOCK | GPO | O_MC_UNLOCK | | |
| Reset | Pin37 | RESETCONS# | GPO | ORSTCON# | PU 8.2K | +3V |

| | ID Port5 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| Unused | Pin62 | SUSWARN# | GPO | S_SUSWARN# | | |
| Unused | Pin52 | SYNCAL | GPO | NC (Unused) | | |
| Unused | Pin51 | ERROCK# | GPO | P_SUSACK# | PU 8.2K(/x) | +3VSB_ATX |
| Unused | Pin44 | PCH_WAKE_EXCUAL | GPO | O_SUS_WAKE_DCUAL | PU Dcuae | |
| | Pin40 | SLP_SUS# | DIO_I#4 | DIO_I#4 | PU 8K2K | +5V |
| Unused | Pin39 | SLP_SUS_FET | GPO | O_PWRFET | | |
| VDDQ_EN | Pin38 | VDDQ_EN | VDDQ_EN | P_VDDQ_EN_10 | PU 10K | +3VSB_ATX |
| VPP_EN | Pin37 | VPP_EN | VPP_EN | P_+VPPDDR_EN | PU 10K | +3VSB_ATX |

| | ID Port6 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| | Pin50 | PWM1(ATXGP/LED_A | GPO | IDO | PU 1K | |
| | Pin49 | PWM2(ATXGP/LED_B | GPO | IDI | PU 1K | |
| | Pin48 | PWM3(ATXGP/LED_C | GPO | LED | PU 1K | |
| | Pin47 | PWM4(ATXGP/LED_D | GPO | PCIMODE | PU 2.7K | +3V |
| | Pin45 | PWM5(ATXGP/LED_E | GPO | CONFIG2 | PU 2.7K | +3V |
| | Pin44 | PWM6(ATXGP/LED_F | GPO | ATXPG_DET# (ATX mode: PU Dual:) | PU 100K | |
| Unused | Pin43 | PWM7(ATXGP/LED_G | GPO | NC BIOSWP# (Unused) | | |
| Unused | Pin42 | PWM8(ATXGP/TACH8 | GPO | N21873316 (TP-CI11) | | |

| | ID Port7 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| | Pin69 | BCLKOUT0(S) | GPI | DSW_EN | PD 1K | |
| | Pin68 | BCLKOUT1(S) | GPO | NC (Unused) | | |
| | Pin67 | BCLKIN0(S) | 5V_VSB_PWRGD | O_5VSUSBPS2_IN | PU 20K/PU3.3K+100kpF | +5VSB_ATX |
| | Pin66 | BCLKIN1(S) | GPO | NC (Unused) | | +3V |
| | Pin79 | RSTOUT4# | GPO | SIO_SPK | PU8.1K(/x) Mobile/PC | +3VSB_ATX |
| | Pin78 | RSTOUT1# | RSTOUT1# | O_PCIEX1_RST# | PD 100K | |
| | Pin77 | RSTOUT2# | GPO | N21873354 (PD DR41=8.2K) | PD 8.2K | |

| | ID Port8 | Default | Use As | Signal Name | EXT PUPD | Power |
|---|---|---|---|---|---|---|
| COM1 Port | Pin29 | GPI0 | CTSA# | O_COM1_CTSA# | | |
| COM1 Port | Pin30 | GPI1 | DSRA# | O_COM1_DSRA# | | |
| COM1 Port | Pin31 | GPI2 | RTSA# | O_COM1_RTSA# | | |
| COM1 Port | Pin32 | GPI3 | DTRA | O_COM1_DTRA# | | |
| COM1 Port | Pin33 | GPI4 | SIN1 | O_COM1_RXD1 | PU 4.7K | +5V |
| COM1 Port | Pin34 | GPI5/SOUT1_IRMX | SOUT1 | O_COM1_TXD1 | | |
| COM1 Port | Pin35 | GPI6 | DCDA# | O_COM1_DCD1# | | |
| COM1 Port | Pin36 | GPI7 | RIA# | O_COM1_RI1# | | |

## SMS-H410A Source:

SM BUS ADDRESS :

| PCI Master | |
|---|---|
| SM-Bus Device | SM-Bus Address |
| DIMM(0 ON_MB_1A ) | A0h |
| DIMM(1 ON_MB_1A ) | A4h |
| NCT6793D Master (SMB-MAIN) | SM-Bus Address |
| SM-Bus Device | |
| PMC(-IE) SUV-H12 (PCI B:1) | 40h |
| PCI Master(SMB-EXT) | SM-Bus Address |
| PCI 0x15 Slot1 [PCI 0x_0] | |
| PCI 0x4 Slot2 [PCI 0x_0] | |
| PCI 0x4 Slot3 [PCI 0x_0] | |
| PCI 0x4 Slot4 [PCI 0x_0] | |
| PCI Master(SMB PCI) | SM-Bus Address |
| SM-Bus Device | |
| | |
| | |
| | |

Device Identification

| Type-C CC/SBU OVP USB3 | |
|---|---|
| ID | 0001B-0018100 / 0D0D3000AMBER-TI |
| PMC | |
| PMC-H3231-W02-PUTON | |
| ID | 0B40-0074000 / 0B40-0174-MELLAN MELLAN 0B46 |
| PCI | |

SMS-H410A PCIE & USB Function define
Comet Lake-PCH-V H410

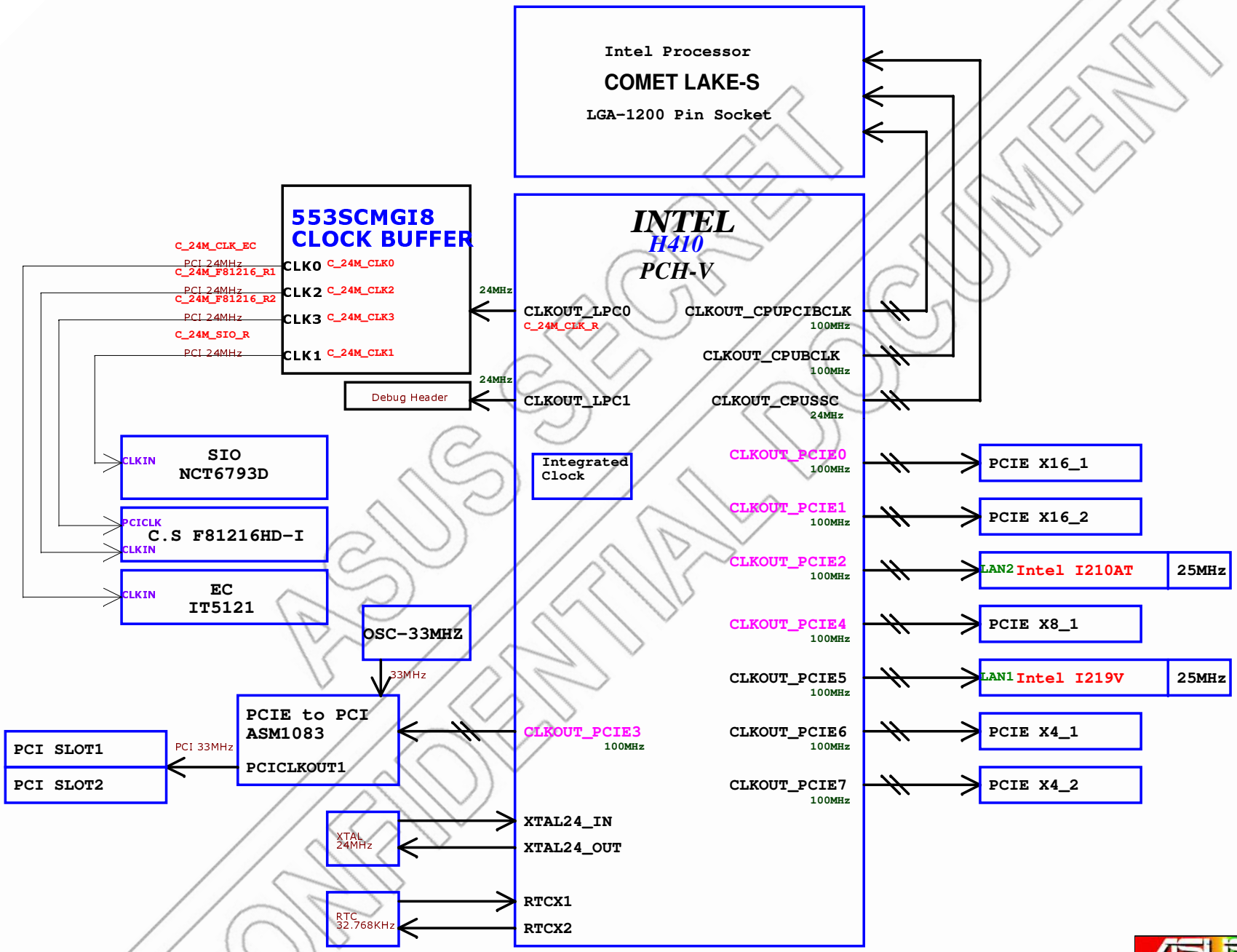
USB3.1/PCIE/SATA Setting

| | | | |
|---|---|---|---|
| 0 | USB3.1#1 | (port1) LAN+USB31 Gen1-5G#01 | |
| 1 | USB3.1#2 | (port2) LAN+USB31 Gen1-5G#02 | |
| 2 | USB3.1#3 | (port3) USB30 Internal Header#01 | |
| 3 | USB3.1#4 | (port4) USB30 Internal Header#02 | |
| 4 | USB3.1#5 | N/A | |
| 5 | USB3.1#6 | N/A | |
| 6 | USB3.1#7 PCIE#1 | N/A | |
| 7 | USB3.1#8 PCIE#2 | N/A | |
| 8 | USB3.1#9 PCIE#3 | N/A | |
| 9 | USB3.1#10 PCIE#4 | N/A | |
| 10 | PCIE#1 | #01 | PCIeX1_2 slot#02 (PCIEX1) |
| 11 | PCIE#4 | #02 | LAN2_I210AT#01 |
| 12 | PCIE#7 | #03 | Asmedia1083_PCIE to PCIe3 |
| 13 | PCIE#8 | #04 | PCIeX8_1 slot#01 (PCIEX1) |
| 14 | PCIE#9 | GbE | LAN1_I219V |
| 15 | PCIE#10 | | N/A |
| 16 | PCIE#11 | #05 | PCIeX4_1 slot#01 (PCIEX1) |
| 17 | PCIE#12(SATA1A) | #06 | PCIeX4_2 slot#02 (PCIEX1) |
| 18 | PCIE#13(SATA0B) | | SATA6G_1 |
| 19 | PCIE#14(SATA1B) | | SATA6G_2 |
| 20 | PCIE#15(SATA2) | | SATA6G_3 |
| 21 | PCIE#16(SATA3) | | SATA6G_4 |
| 22 | PCIE#17(SATA4) | | |
| 23 | PCIE#18(SATA5) | | N/A |
| 24 | PCIE#19(SATA6) | | |
| 25 | PCIE#20(SATA7) | | |
| 26 | PCIE#21 | | |
| 27 | PCIE#22 | | N/A |
| 28 | PCIE#23 | | |
| 29 | PCIE#24 | | |

USB2.0 Setting

| | | |
|---|---|---|
| 1 | USB2#1 | LAN+USB31 Gen1-5G#01 |
| 2 | USB2#2 | LAN+USB31 Gen1-5G#02 |
| 3 | USB2#3 | USB30 Internal Header#01 |
| 4 | USB2#4 | USB30 Internal Header#02 |
| 5 | USB2#5 | LAN2+USB2#05 |
| 6 | USB2#6 | LAN2+USB2#06 |
| 7 | USB2#7 | USB20 Only_#1 Type A |
| 8 | USB2#8 | USB20 Only_#2 Type A |
| 9 | USB2#9 | USB20 Vertital Type A |
| 10 | USB2#10 | USB20 HUB to 4Ports |
| 11 | USB2#11 | N/A |
| 12 | USB2#12 | N/A |
| 13 | USB2#13 | N/A |
| 14 | USB2#14 | N/A |

| HSIO | Q370 Device ID: A306 | H310 Device ID: A303 | | | IRST for PCIE Storage |
|---|---|---|---|---|---|
| 0 | USB3.1 Gen1/Gen2 #1 | USB3.1 Gen1 #1 | | | |
| 1 | USB3.1 Gen1/Gen2 #2 | USB3




ASUS SECRET
CONFIDENTIAL DOCUMENT

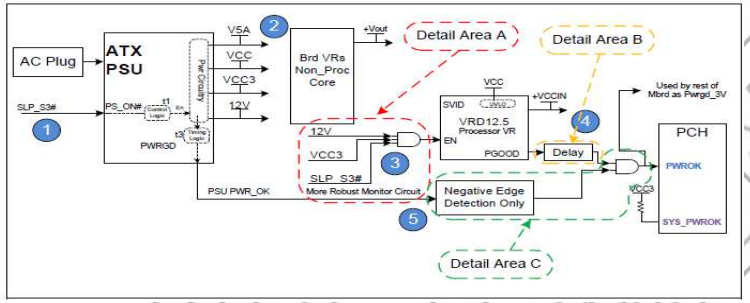
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| A3 | SMS-H410 | 1.00 |

Date: Wednesday, March 18, 2020 Sheet 3 of 87




RESET_SWITCH

POWER_SWITCH

SIO
NCT6793D

PCH
PCH-V H410

PROCESSOR
Comet Lake

<5>O_PWRBTN#IN

PSIN#

RESETCONO#

For EVT Test0314

O_RSTCON#

SYS_RESET#

LRESET# <16>S_PLTRST#

PLTRST# PLTRST_CPU# *4 <19>H_CPURST_SB#

RESET#

KBRST# O_KB_RST#

RCIN#

RSMRST# <4>O_RSMRST#

RSMRST# RTCRST# <1>RTCRST#

SRTCRST# <1>SRTCRST#

PSOUT# <6>O_PWRBTN#

PWRBTN#

BATTERY

POWER SUPPLY

Main PWR
VSB
PSON#
PWROK

<10>12V,5V,3V

<3>+5VSB_ATX,+3VSB_ATX

<9>ATX_PSON#

<11>PWRGD_PS//ATXPG_IN

<2>AC Power Switch On

SLP_S5# <8>S_SLPS4#

SLP_S4#

<11>+VCCIO

<12>+VCCSA

PSON# *1

ATXPGD *2

SLP_S3# <9>S_SLPS3#

SLP_S3#

<15>H_PWRGD

PROCPWRGD

CPUPWRGD

<4.1>S_DPWROK

DSW_PWROK

<14>H_VCCST_CPUPWRGD

VCCST_PWRGD

<10>PCH_SYSPWROK

SYS_PWROK

<17>VRM_SVID

SVID

<18>+VCCCORE//+VCCGT

+VCCCORE//+VCCGT

PCH_PWROK

Vcore Controller

SVID

VCORE

VR_ON

PGOOD

RT3609BEGQW

<13>VR_READY_10

*3 S_SLPS3#

P_+VCCIO_PG_10

*1
PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2
PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3
Come with +3VSB_ATX and gated by SLP_S3#, P_+VCCIO_PG_10

*4
PLTRST_CPU#=PLTRST#, voltage=1V, directly connect to CPU

CHIP

SOCKET or SLOT

ASUS SECRET
CONFIDENTIAL DOCUMENT

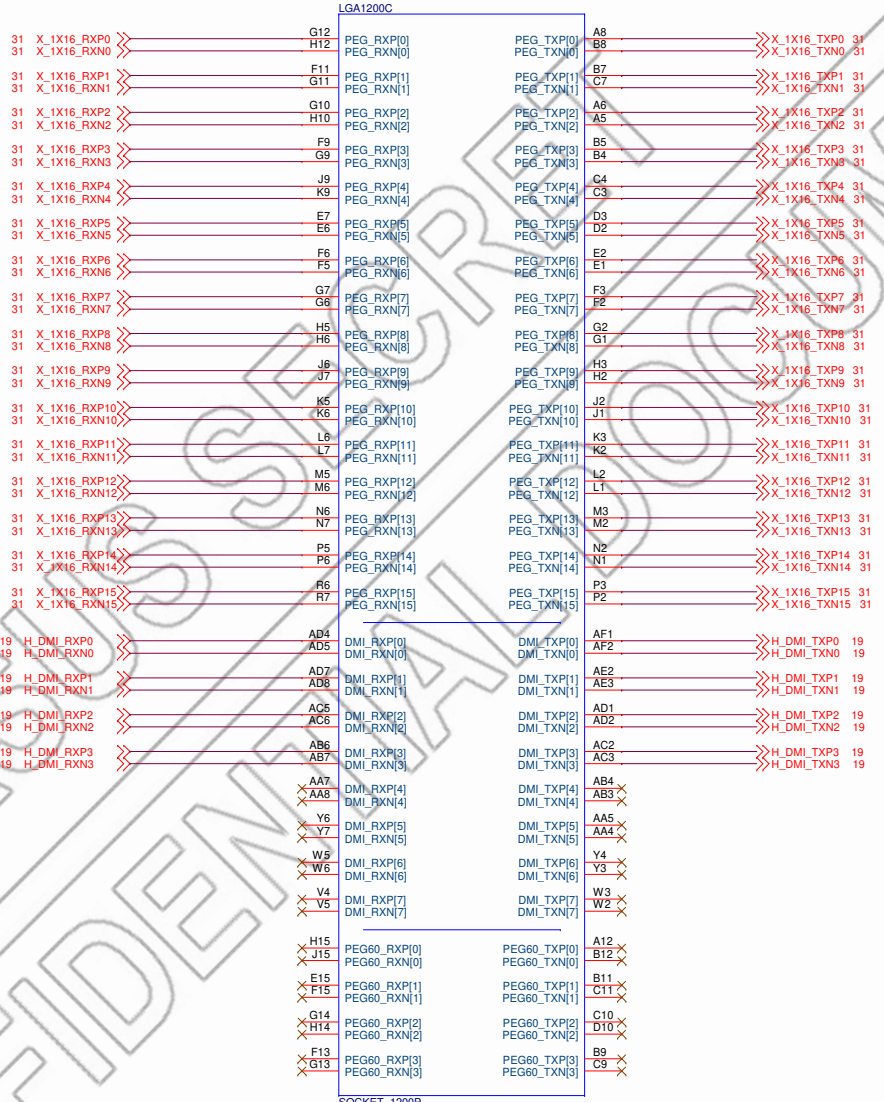
ASUS
ASUSTek COMPUTER INC.

Title : Signal & Reset map

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| A3 | SMS-H410 | 1.00 |

Date: Wednesday, March 18, 2020 Sheet 4 of 87




[GA]FOXCONN/PE12001-11AJ1-1H

**12001-00280400**

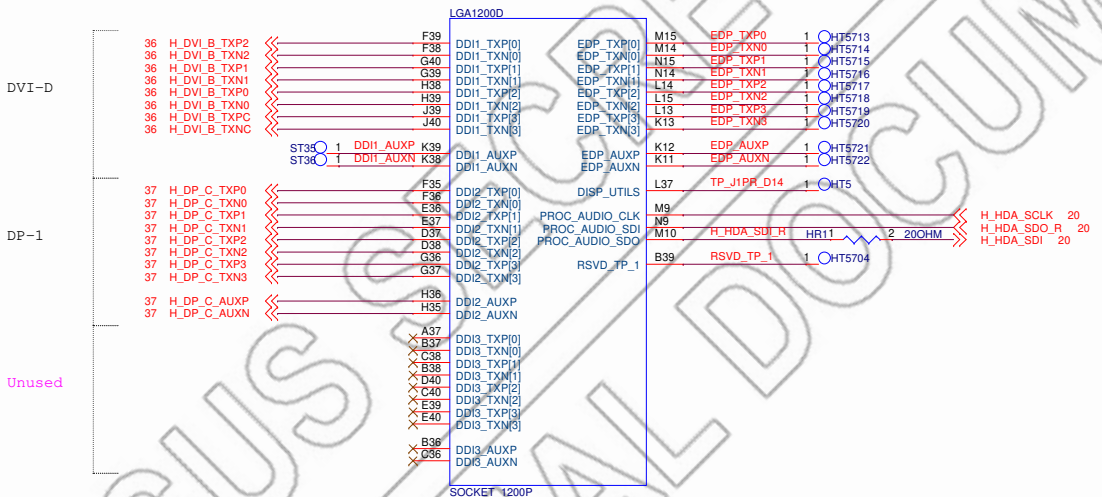
*LGA1200 LGA 1200P SOCKET 15U SMT*

*1st : P/N : 12001-00280400 FOXCONN/PE12001-11AJ1-1H*

*2nd : P/N : 12001-00280300 LOTES/AZIF0181-P001C*

ASUS SECRET
CONFIDENTIAL DOCUMENT

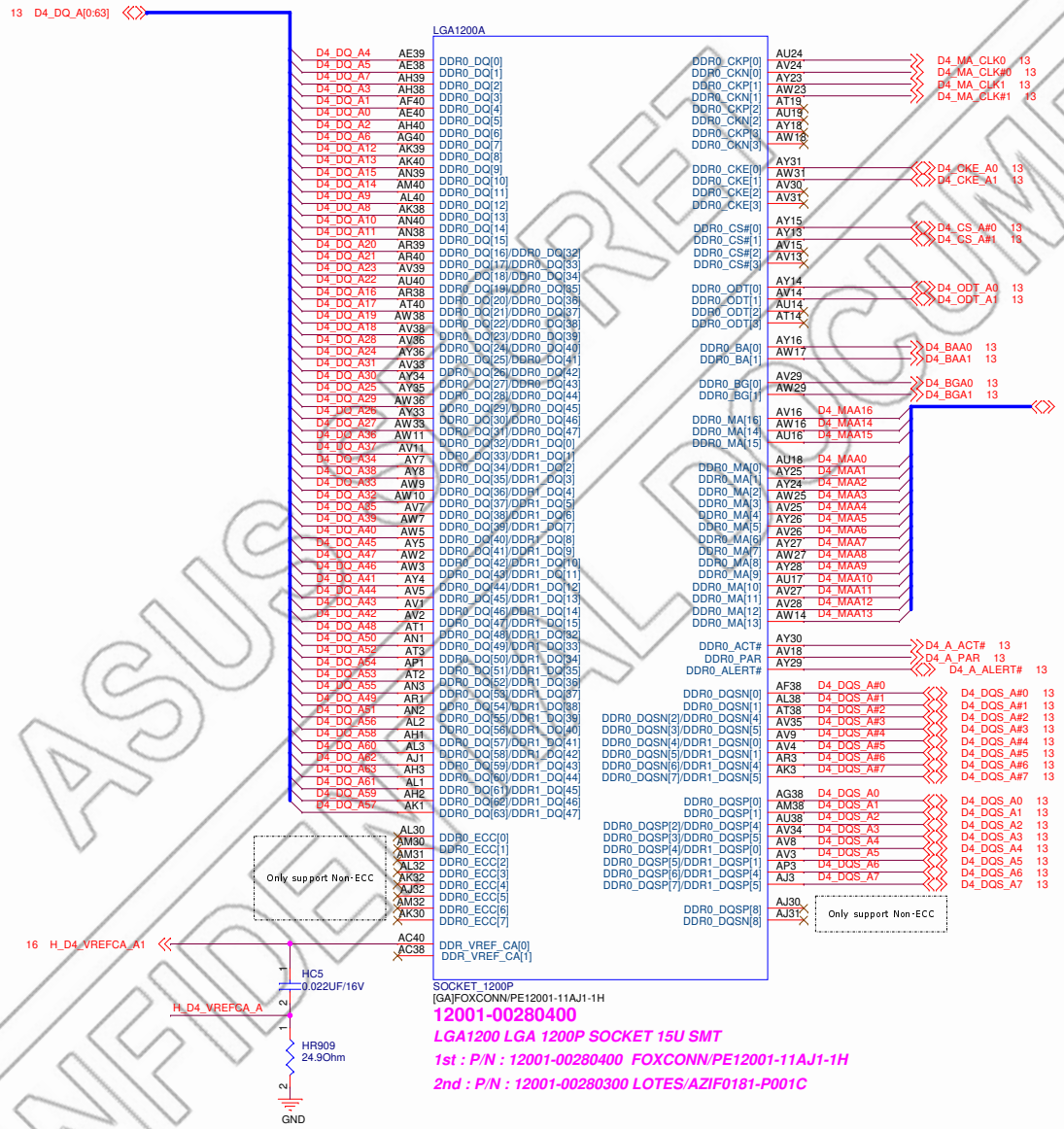
| | | |
|---|---|---|
| ASUS | Title : LGA1200 (DMI/PEG) | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 5 of 87 | |




ASUS SECRET
CONFIDENTIAL DOCUMENT

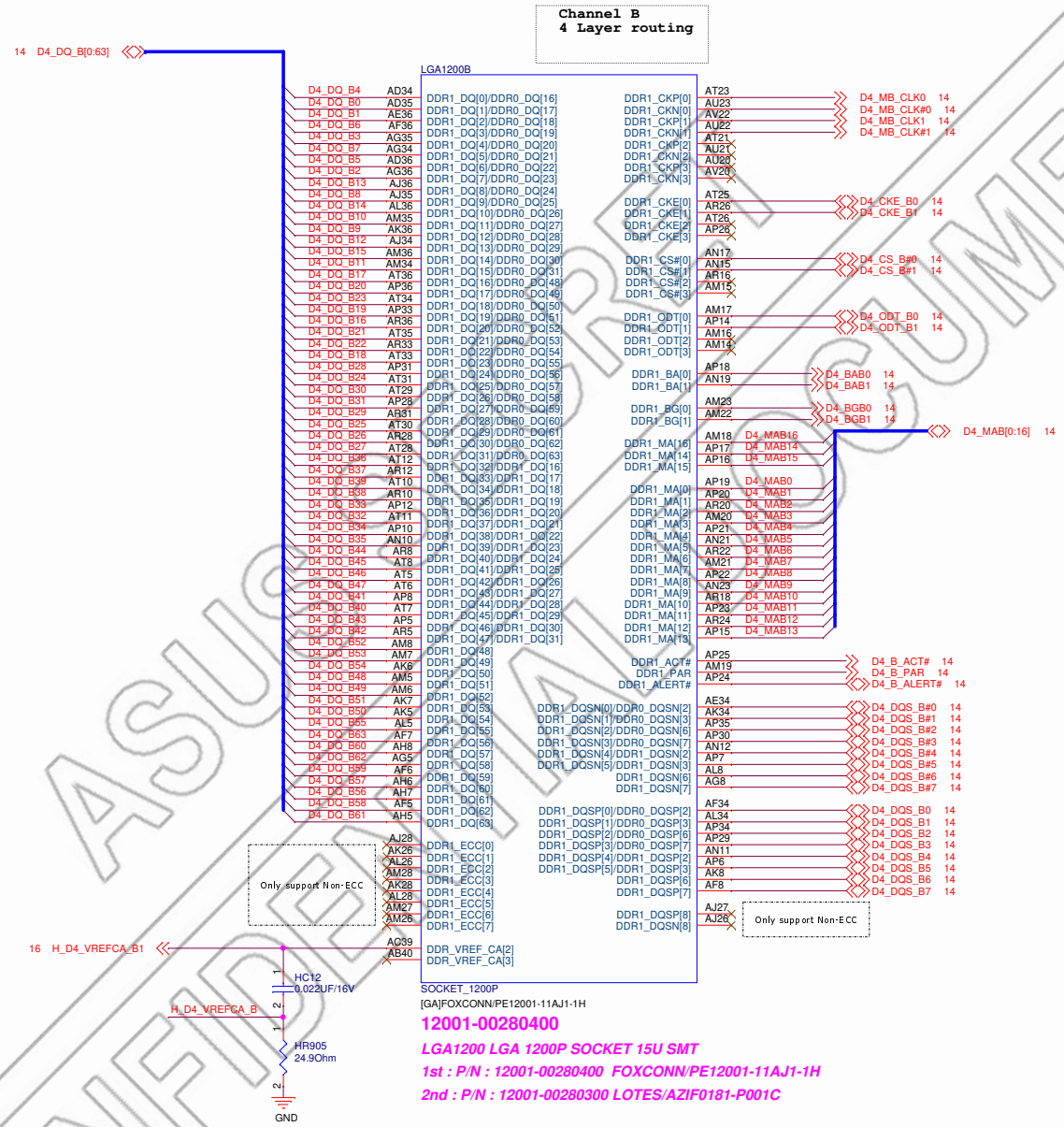
| | | | |
|---|---|---|---|
| ASUS | Title: LGA1200 (FDI/DISPLAY) | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 6 of 87 | | |

Channel A
4 Layer routing



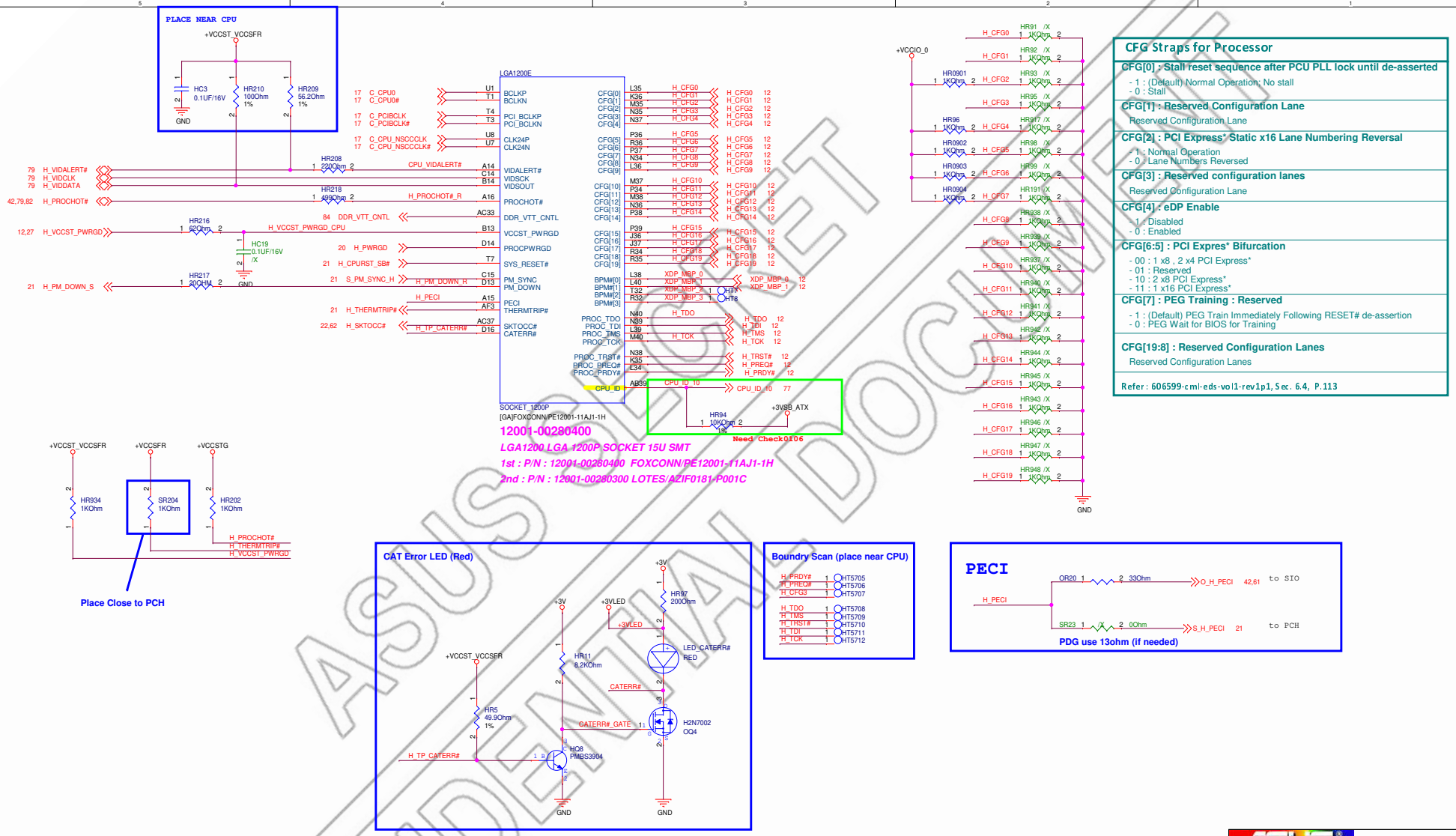

ASUS CONFIDENTIAL DOCUMENT

| | | | |
|---|---|---|---|
| ASUS | Title: LGA1200 (DDR4_A Control) | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 7 of 87 | | |

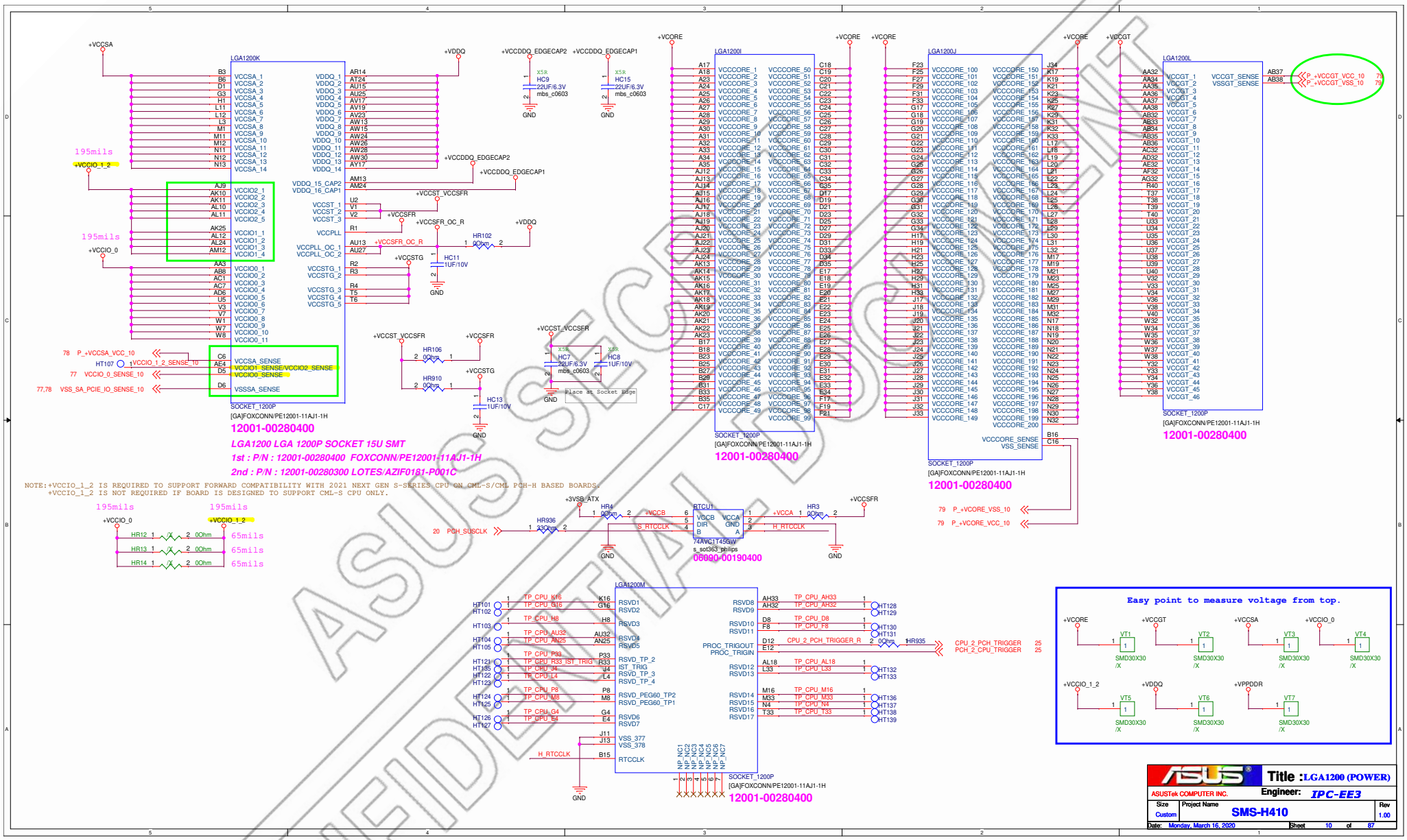



ASUS CONFIDENTIAL DOCUMENT

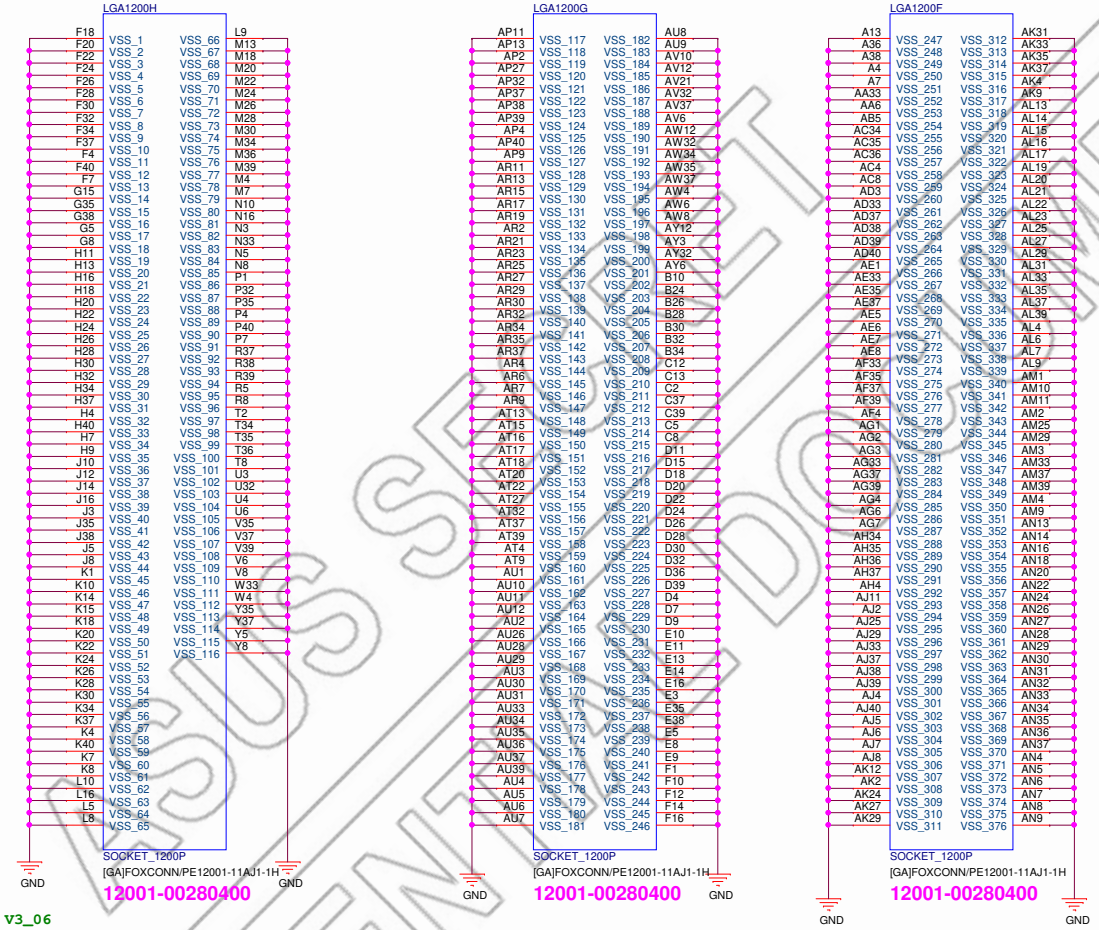
| | | | |
|---|---|---|---|
| ASUS | Title: LGA1200 (DDR4_B Control) | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 8 of 87 | | |



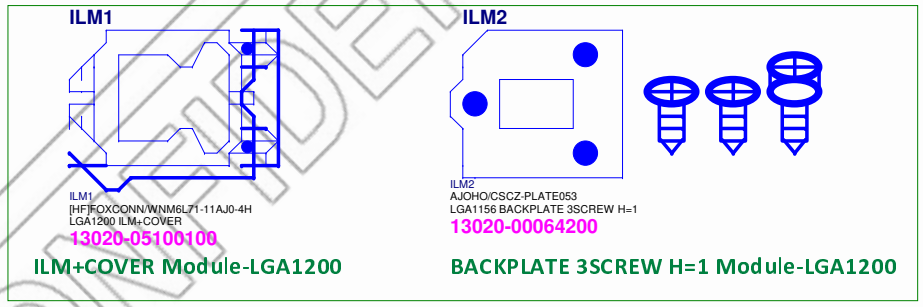

ASUS CONFIDENTIAL DOCUMENT




ASUS SECRET
CONFIDENTIAL DOCUMENT

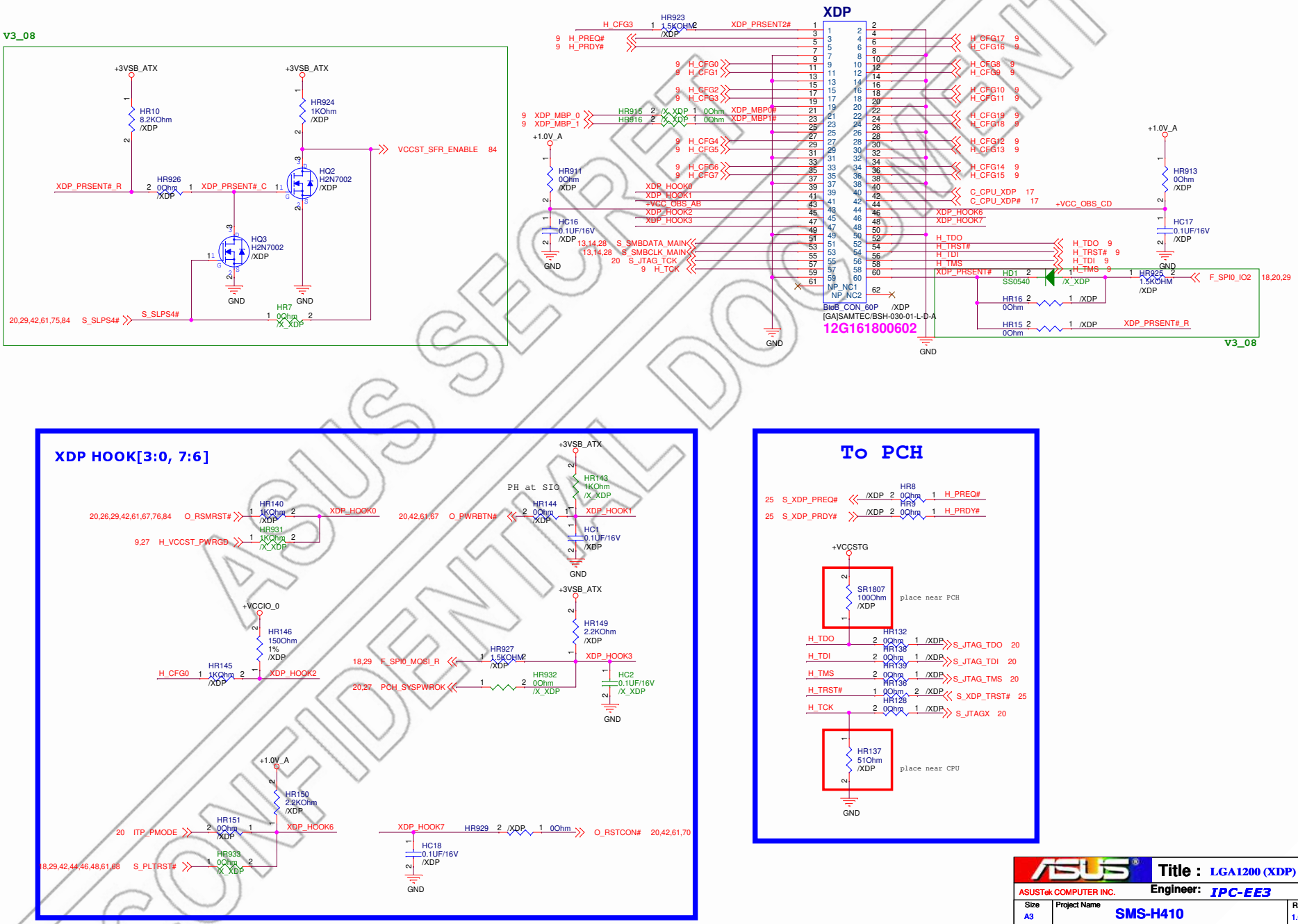



V3_06

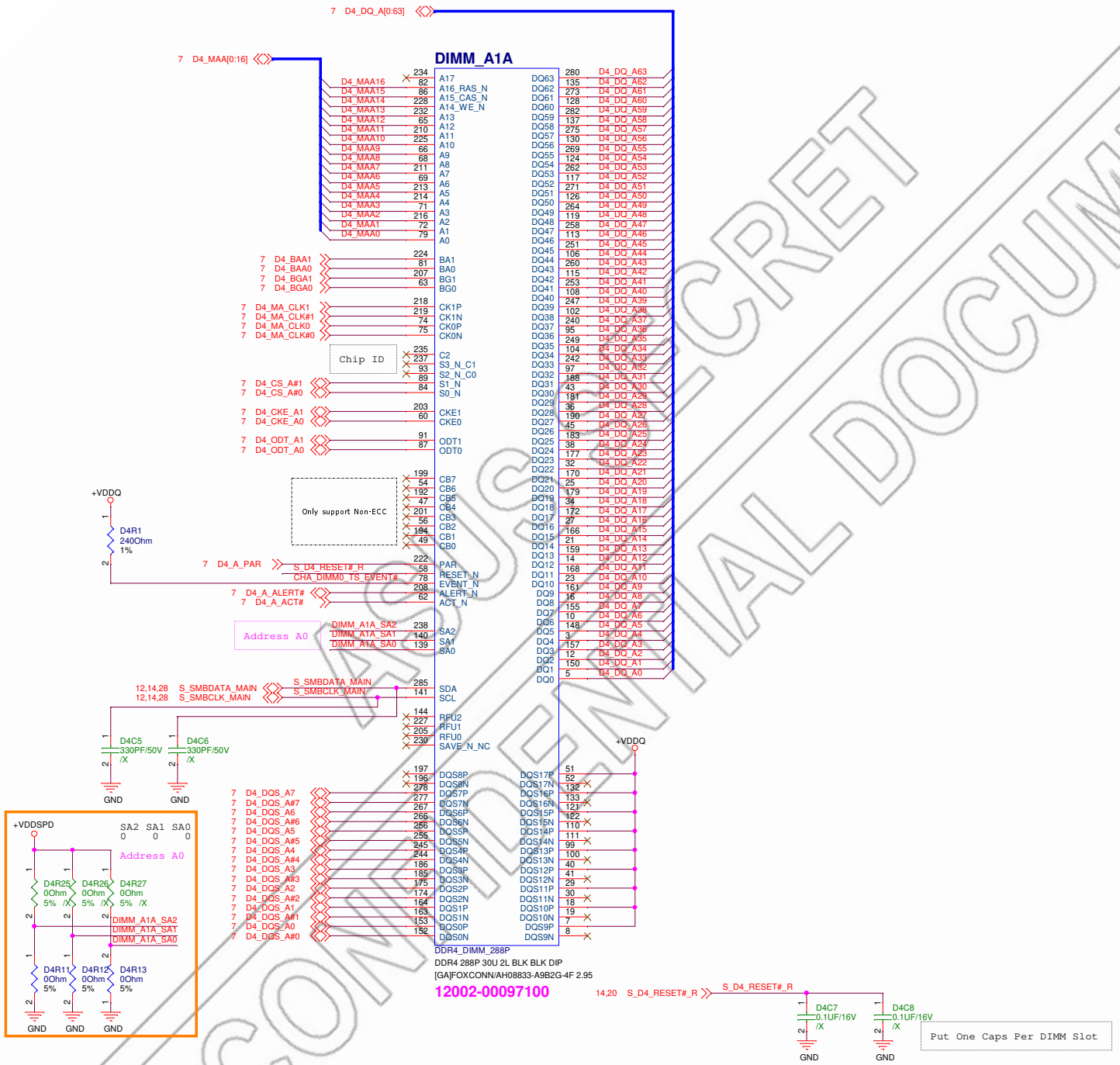



| | | | |
|---|---|---|---|
| ASUSTek COMPUTER INC. | Title : LGA1200 (GND) | | |
| | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 11 of 87 | | |

ASUS CONFIDENTIAL DOCUMENT

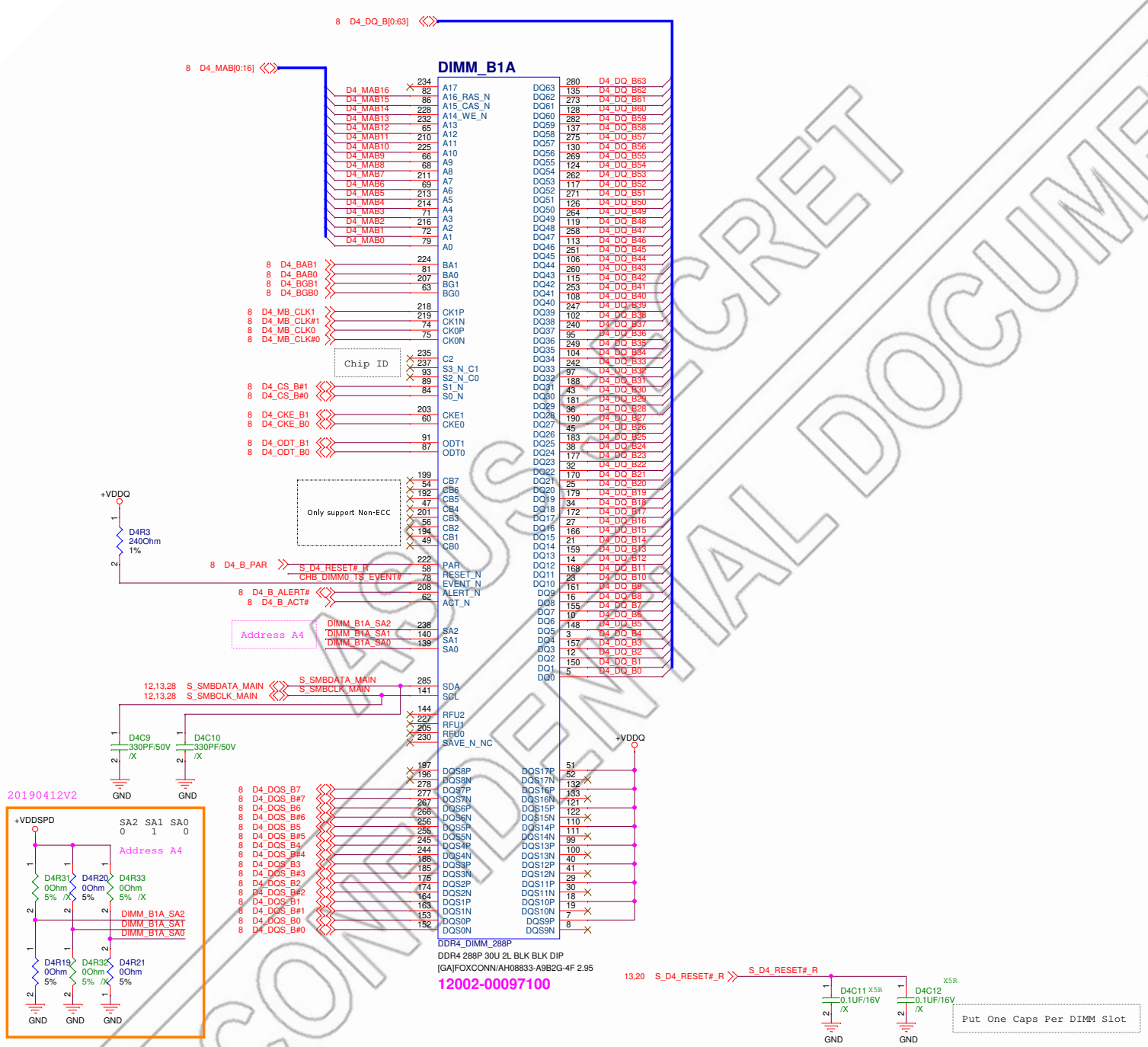



ASUS SECRET
CONFIDENTIAL DOCUMENT




| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : DDR4 Channel A | Engineer: IPC-EE3 |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 13 of 87 | |

ASUS SECRET
CONFIDENTIAL DOCUMENT




CONFIDENTIAL DOCUMENT
ASUS SECRET

ASUS

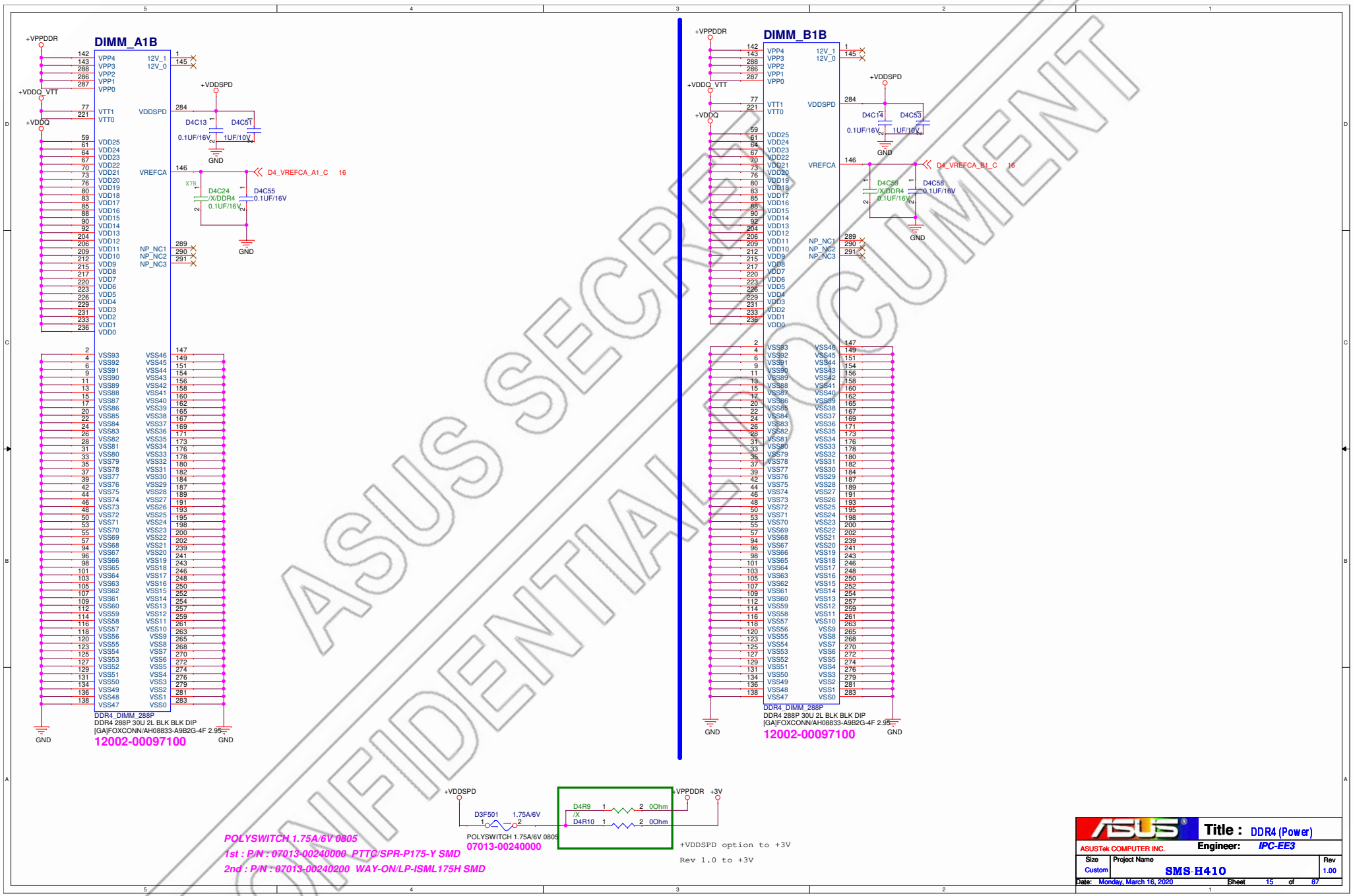
ASUSTek COMPUTER INC.

Title : DDR4 Channel B

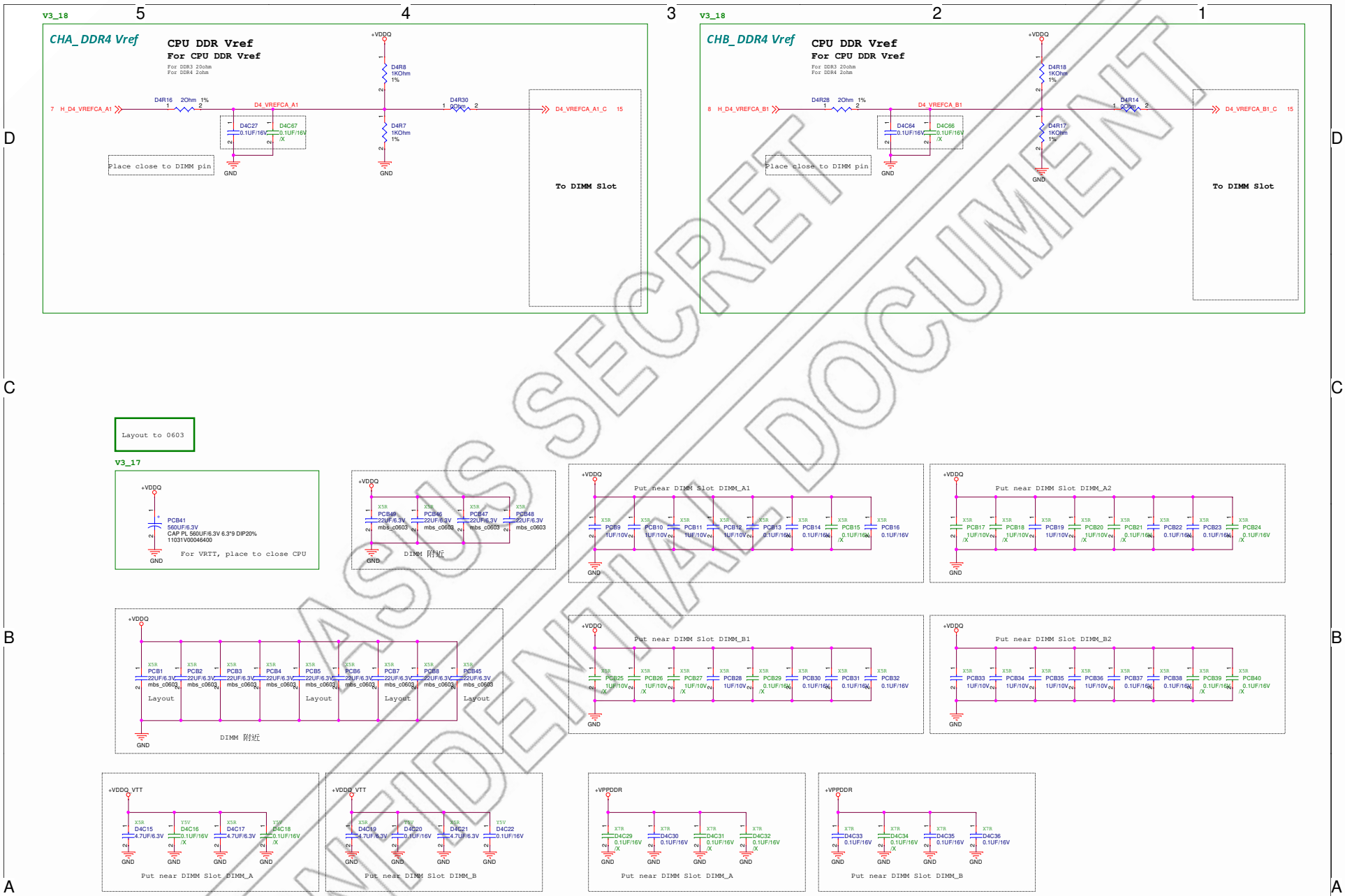
Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| A3 | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 14 of 87




ASUS SECRET
CONFIDENTIAL DOCUMENT




ASUS SECRET
CONFIDENTIAL DOCUMENT

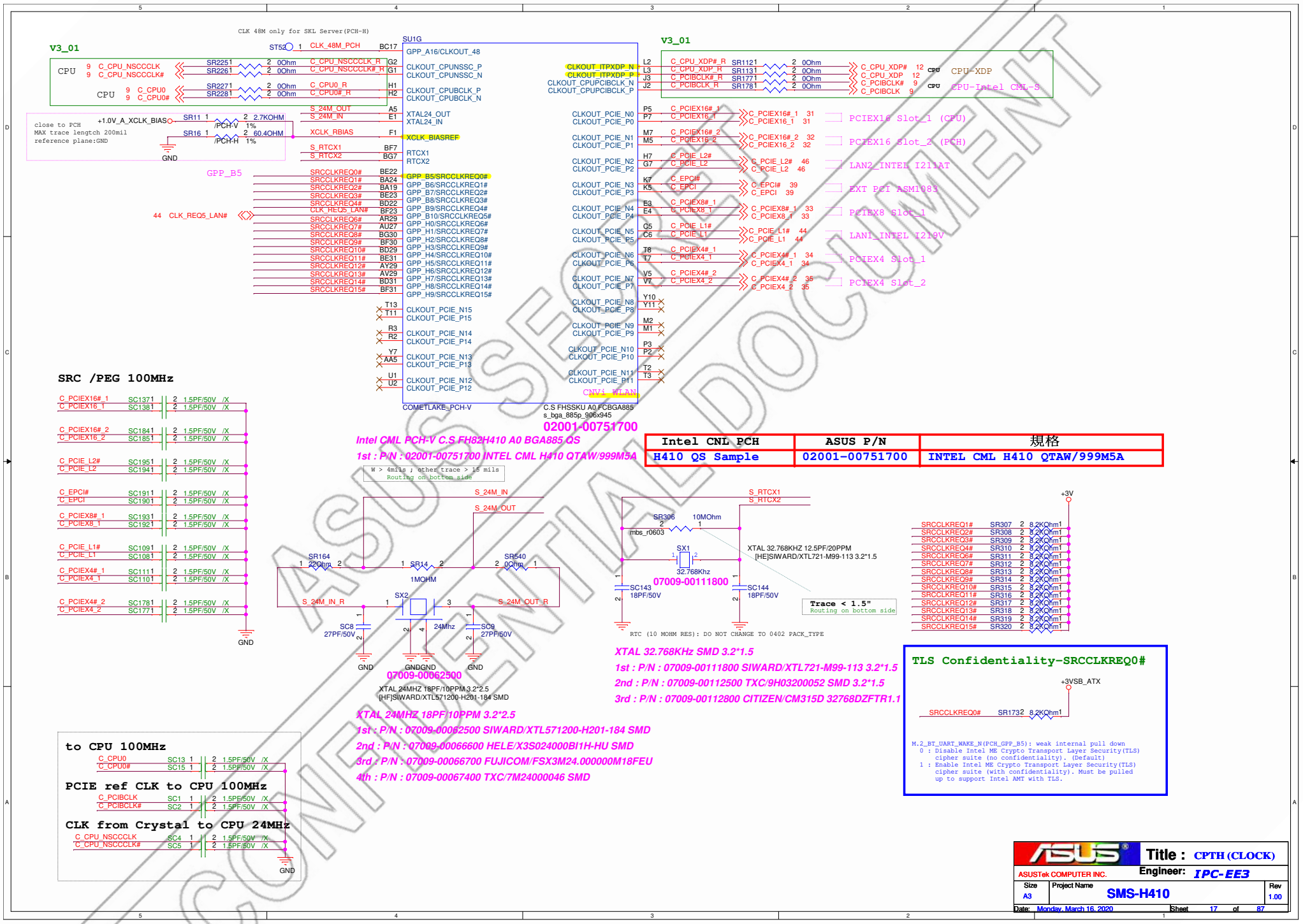
ASUS ASUSTeK COMPUTER INC.

Title : DDR4 (Power CAPs)

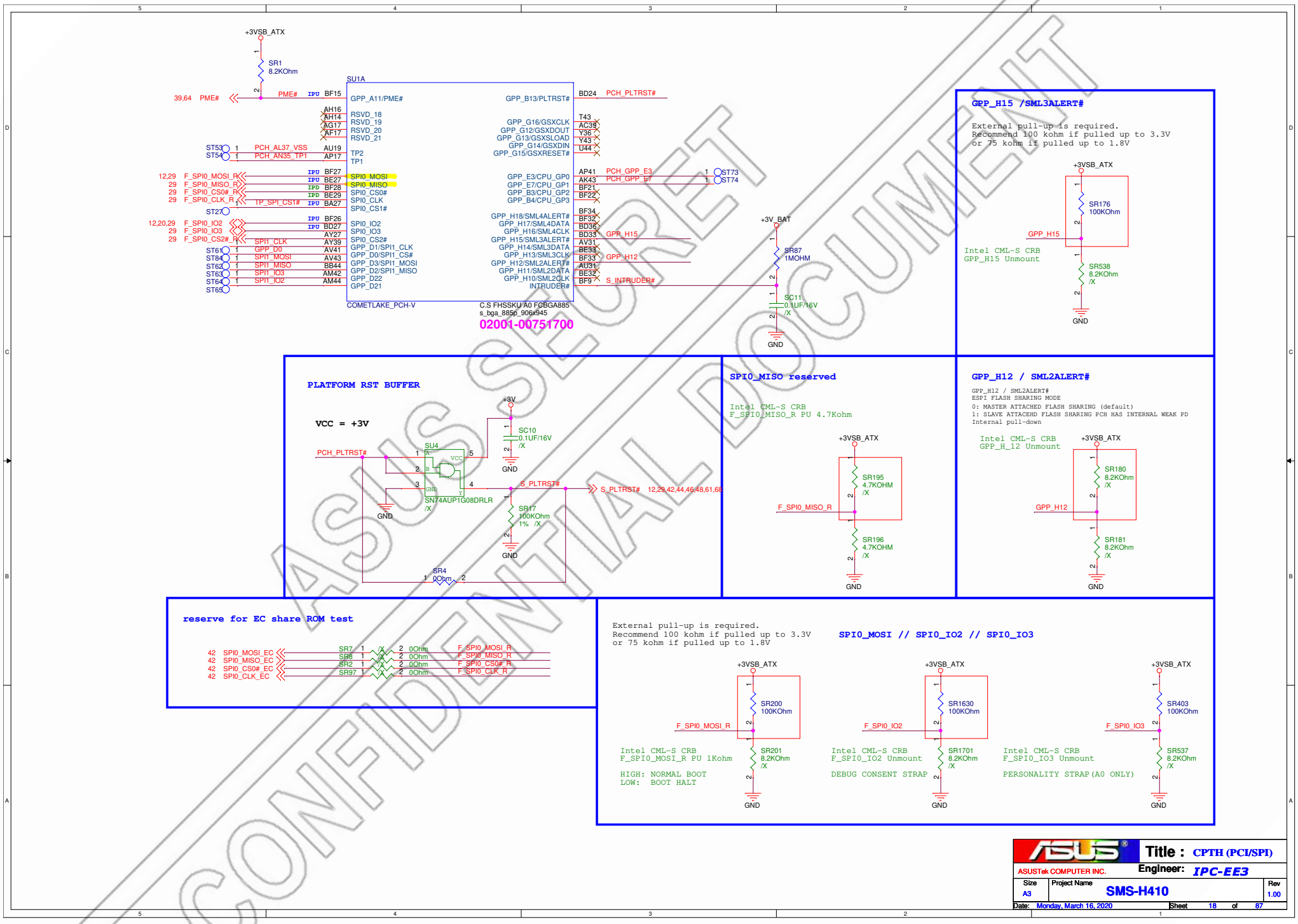
Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| C | SMS-H4 10 | 1.00 |

Date: Monday, March 16, 2020 Sheet 16 of 87




| Intel CNL PCH | ASUS P/N | 規格 |
|---|---|---|
| H410 QS Sample | 02001-00751700 | INTEL CML H410 QTAW/999M5A |


+3VSB_ATX
SR1
8.2KOhm
39,64 PME#
PME# IPU BF15
SU1A
GPP_A11/PME#
AH16
AH14 RSVD_18
AG17 RSVD_19
AF17 RSVD_20
RSVD_21
ST53 1 PCH_AL37_VSS AU19
ST54 1 PCH_AN35_TP1 AP17
TP2
TP1
12,29 F_SPI0_MOSI_R IPU BF27
29 F_SPI0_MISO_R IPU BE27
29 F_SPI0_CS0#_R IPD BF28
29 F_SPI0_CLK_R IPD BE29
1 TP_SPI_CS1# IPU BA27
ST27
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
12,20,29 F_SPI0_IO2 IPU BF26
29 F_SPI0_IO3 IPU BD27
29 F_SPI0_CS2#_R AY27
1 SPI1_CLK AY39
ST61 1 GPP_D0 AV41
ST84 1 SPI1_MOSI AV43
ST62 1 SPI1_MISO BB44
ST63 1 SPI1_IO3 AM42
ST64 1 SPI1_IO2 AM44
ST65
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22
GPP_D21
COMETLAKE_PCH-V
GPP_B13/PLTRST# BD24 PCH_PLTRST#
T43
GPP_G16/GSXCLK AC39
GPP_G12/GSXDOUT Y36
GPP_G13/GSXSLOAD Y43
GPP_G14/GSXDIN U44
GPP_G15/GSXRESET#
AP41 PCH_GPP_E3 1 ST73
AK43 PCH_GPP_E7 1 ST74
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2 BF21
GPP_B4/CPU_GP3 BF22
BF34
GPP_H18/SML4ALERT# BF32
GPP_H17/SML4DATA BD34
GPP_H16/SML4CLK BD33 GPP_H15
GPP_H15/SML3ALERT# AV31
GPP_H14/SML3DATA BE33
GPP_H13/SML3CLK BF33 GPP_H12
GPP_H12/SML2ALERT# AU31
GPP_H11/SML2DATA BE32
GPP_H10/SML2CLK BF9 S_INTRUDER#
INTRUDER#
C.S FHSSKU A0 FCBGA885
s_bga_8850_906x945
02001-00751700
+3V_BAT
SR87
1MOHM
SC11
0.1UF/16V
/X
GND
GPP_H15 /SML3ALERT#
External pull-up is required.
Recommend 100 kohm if pulled up to 3.3V
or 75 kohm if pulled up to 1.8V
+3VSB_ATX
SR176
100KOhm
GPP_H15
Intel CML-S CRB
GPP_H15 Unmount
SR538
8.2KOhm
/X
GND
PLATFORM RST BUFFER
VCC = +3V
+3V
SC10
0.1UF/16V
/X
GND
PCH_PLTRST#
SU4
VCC
GND
SN74AUP1G08DRLR
/X
S_PLTRST#
S_PLTRST# 12,29,42,44,46,48,61,68
SR17
100KOhm
1% /X
GND
SR4
0Ohm
SPI0_MISO reserved
Intel CML-S CRB
F_SPI0_MISO_R PU 4.7Kohm
+3VSB_ATX
SR195
4.7KOHM
/X
F_SPI0_MISO_R
SR196
4.7KOHM
/X
GND
GPP_H12 / SML2ALERT#
GPP_H12 / SML2ALERT#
ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING (default)
1: SLAVE ATTACEHD FLASH SHARING PCH HAS INTERNAL WEAK PD
Internal pull-down
Intel CML-S CRB
GPP_H_12 Unmount
+3VSB_ATX
SR180
8.2KOhm
/X
GPP_H12
SR181
8.2KOhm
/X
GND
reserve for EC share ROM test
42 SPI0_MOSI_EC SR7 1 /X 2 0Ohm F_SPI0_MOSI_R
42 SPI0_MISO_EC SR6 1 /X 2 0Ohm F_SPI0_MISO_R
42 SPI0_CS0#_EC SR2 1 /X 2 0Ohm F_SPI0_CS0#_R
42 SPI0_CLK_EC SR97 1 /X 2 0Ohm F_SPI0_CLK_R
External pull-up is required.
Recommend 100 kohm if pulled up to 3.3V
or 75 kohm if pulled up to 1.8V
SPI0_MOSI // SPI0_IO2 // SPI0_IO3
+3VSB_ATX
SR200
100KOhm
F_SPI0_MOSI_R
SR201
8.2KOhm
/X
Intel CML-S CRB
F_SPI0_MOSI_R PU 1Kohm
HIGH: NORMAL BOOT
LOW: BOOT HALT
GND
+3VSB_ATX
SR1630
100KOhm
F_SPI0_IO2
SR1701
8.2KOhm
/X
Intel CML-S CRB
F_SPI0_IO2 Unmount
DEBUG CONSENT STRAP
GND
+3VSB_ATX
SR403
100KOhm
F_SPI0_IO3
SR537
8.2KOhm
/X
Intel CML-S CRB
F_SPI0_IO3 Unmount
PERSONALITY STRAP(A0 ONLY)
GND
ASUS
Title : CPTH (PCI/SPI)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name SMS-H410
Rev 1.00
Date: Monday, March 16, 2020
Sheet 18 of 87
ASUS SECRET
CONFIDENTIAL DOCUMENT

# SMS-H410 Port Assignment

## Comet Lake PCH-V H410

### USB Setting

| USB 2.0 | Function |
|---|---|
| USB2_01 | LAN1+USB31 Gen1-5G#01 |
| USB2_02 | LAN1+USB31 Gen1-5G#02 |
| USB2_03 | USB30 Internal Header#03 |
| USB2_04 | USB30 Internal Header#04 |
| USB2_05 | LAN2+USB20#05 |
| USB2_06 | LAN2+USB20#06 |
| USB2_07 | USB20 2X2 Connector#07 |
| USB2_08 | USB20 2X2 Connector#08 |
| USB2_09 | USB20 Vertical Type A#09 |
| USB2_10 | USB20 HUB to 4 ports_#10 |
| USB2_11 | N/A |
| USB2_12 | N/A |
| USB2_13 | N/A |
| USB2_14 | N/A |

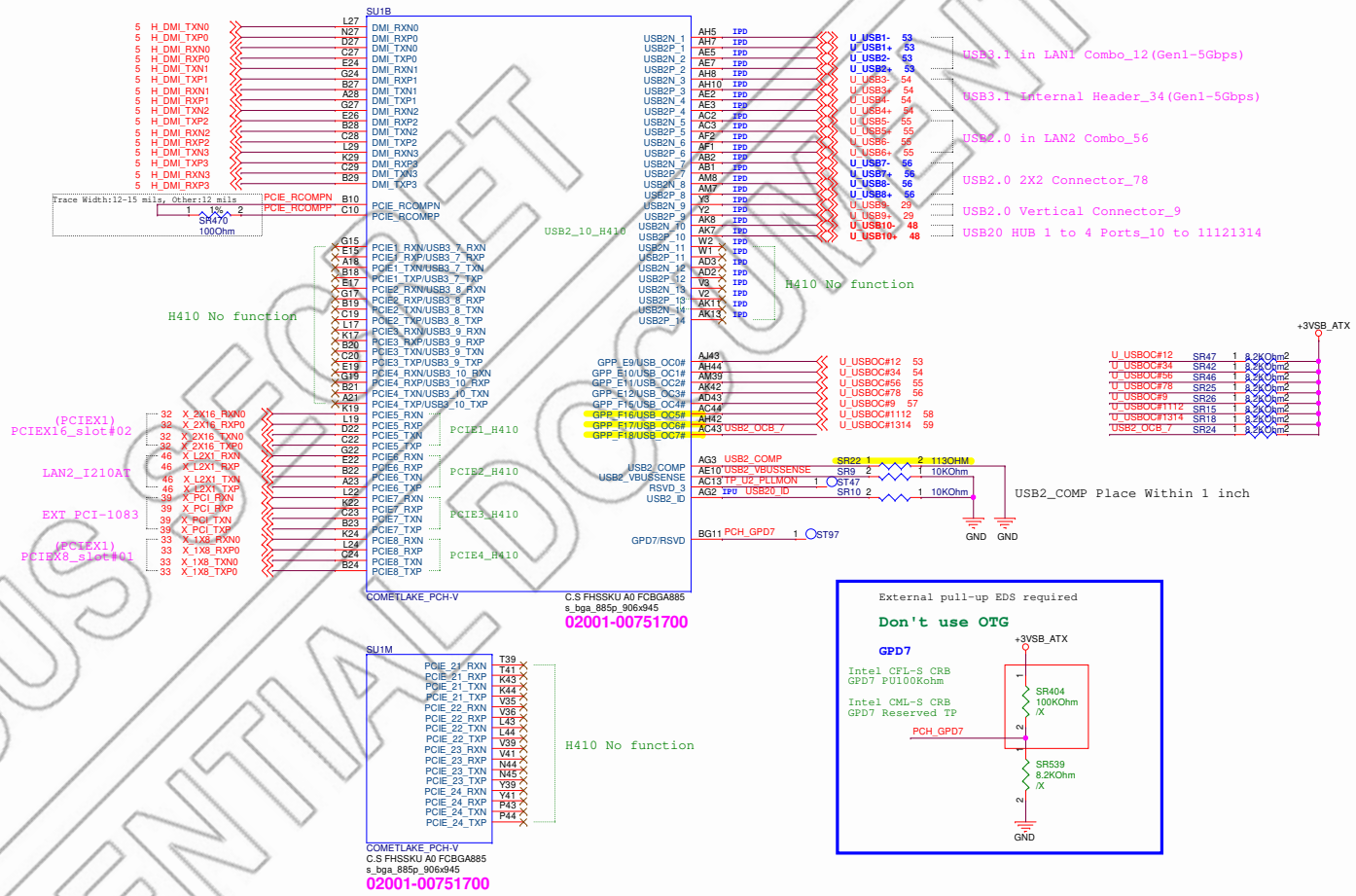
| USB 3.1 | Function |
|---|---|
| USB31_01 | LAN1+USB31 Gen1-5G#01 |
| USB31_02 | LAN1+USB31 Gen1-5G#02 |
| USB31_03 | USB30 Internal Header#03 |
| USB31_04 | USB30 Internal Header#04 |
| USB31_05 | N/A |
| USB31_06 | N/A |
| USB30_07 | N/A |
| USB30_08 | N/A |
| USB30_09 | N/A |
| USB30_10 | N/A |

### PCIE/SATA Function Define

| | Function |
|---|---|
| PCIE-01(USB3#7) | N/A |
| PCIE-02(USB3#8) | N/A |
| PCIE-03(USB3#9) | N/A |
| PCIE-04(USB3#10) | N/A |
| PCIE-05(PCIE#1) | PCIeX16_solt#02 |
| PCIE-06(PCIE#2) | LAN2_I210AT |
| PCIE-07(PCIE#3) | PCIx3-ASM1083 |
| PCIE-08(PCIE#4) | PCIeX8_solt#01 |
| PCIE-09(GbE) | LAN1_I219V |
| PCIE-10 | N/A |
| PCIE-11(PCIE#5) | PCIeX4_solt#01 |
| PCIE-12(PCIE#6) | PCIeX4_solt#02 |

| | Function |
|---|---|
| PCIE-13 (SATA-0b) | SATA6G_1 |
| PCIE-14 (SATA-1b) | SATA6G_2 |
| PCIE-15 (SATA-2) | SATA6G_3 |
| PCIE-16 (SATA-3) | SATA6G_4 |
| PCIE-17 (SATA-4) | N/A |
| PCIE-18 (SATA-5) | |
| PCIE-19 (SATA-6) | |
| PCIE-20 (SATA-7) | |
| PCIE-21 | N/A |
| PCIE-22 | |
| PCIE-23 | |
| PCIE-24 | |

| | Function |
|---|---|
| CLKREQ-0 | M.2_BT_UART_WAKE# |
| CLKREQ-1 | |
| CLKREQ-2 | |
| CLKREQ-3 | |
| CLKREQ-4 | |
| CLKREQ-5 | CLK_REQ5_LAN# |
| CLKREQ-6 | |
| CLKREQ-7 | |
| CLKREQ-8 | |
| CLKREQ-9 | |
| CLKREQ-10 | |
| CLKREQ-11~15 | |




CONFIDENTIAL DOCUMENT
ASUS SECRET

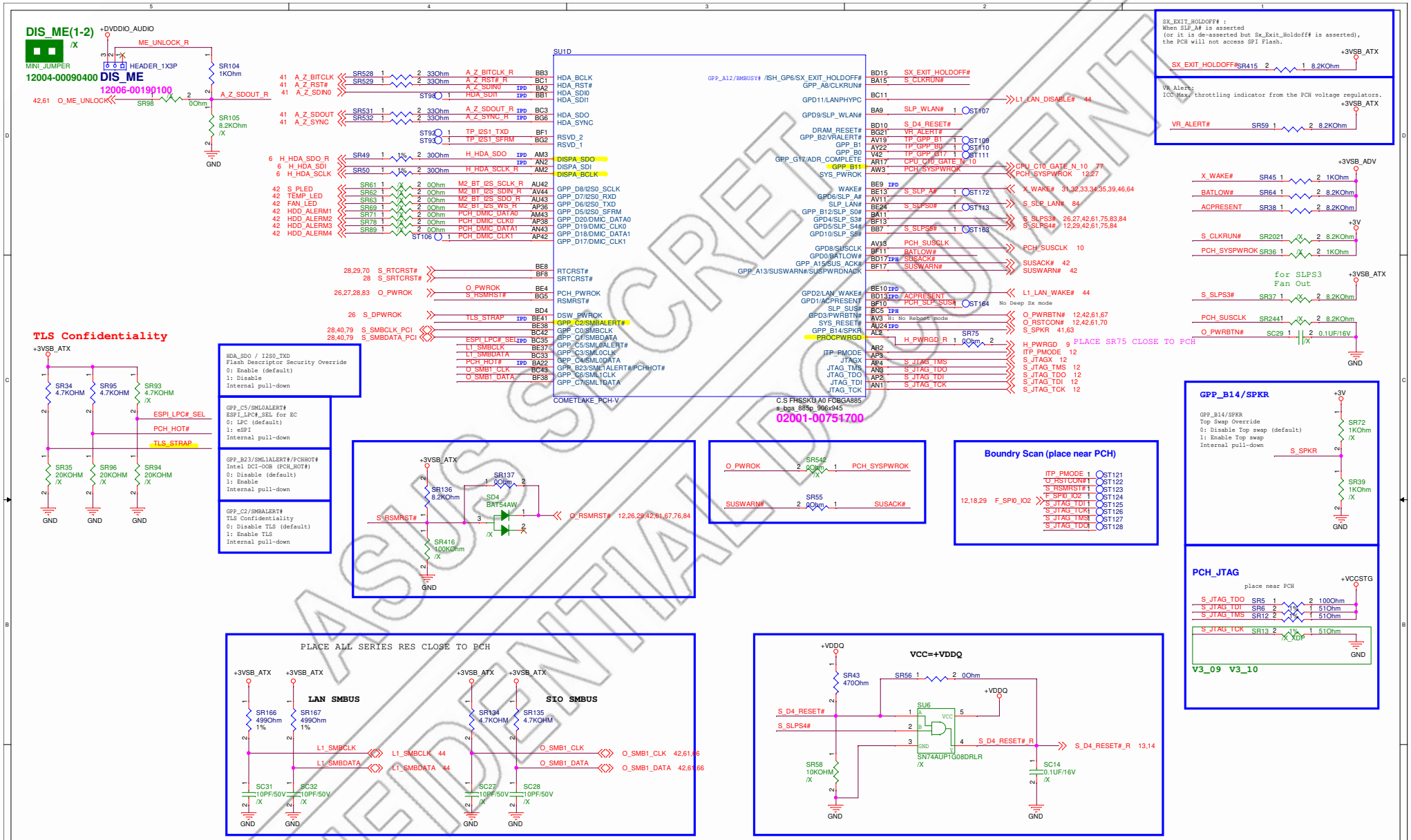
ASUS ASUSTek COMPUTER INC.

Title : CPTH (PCIE/DMI/USB)

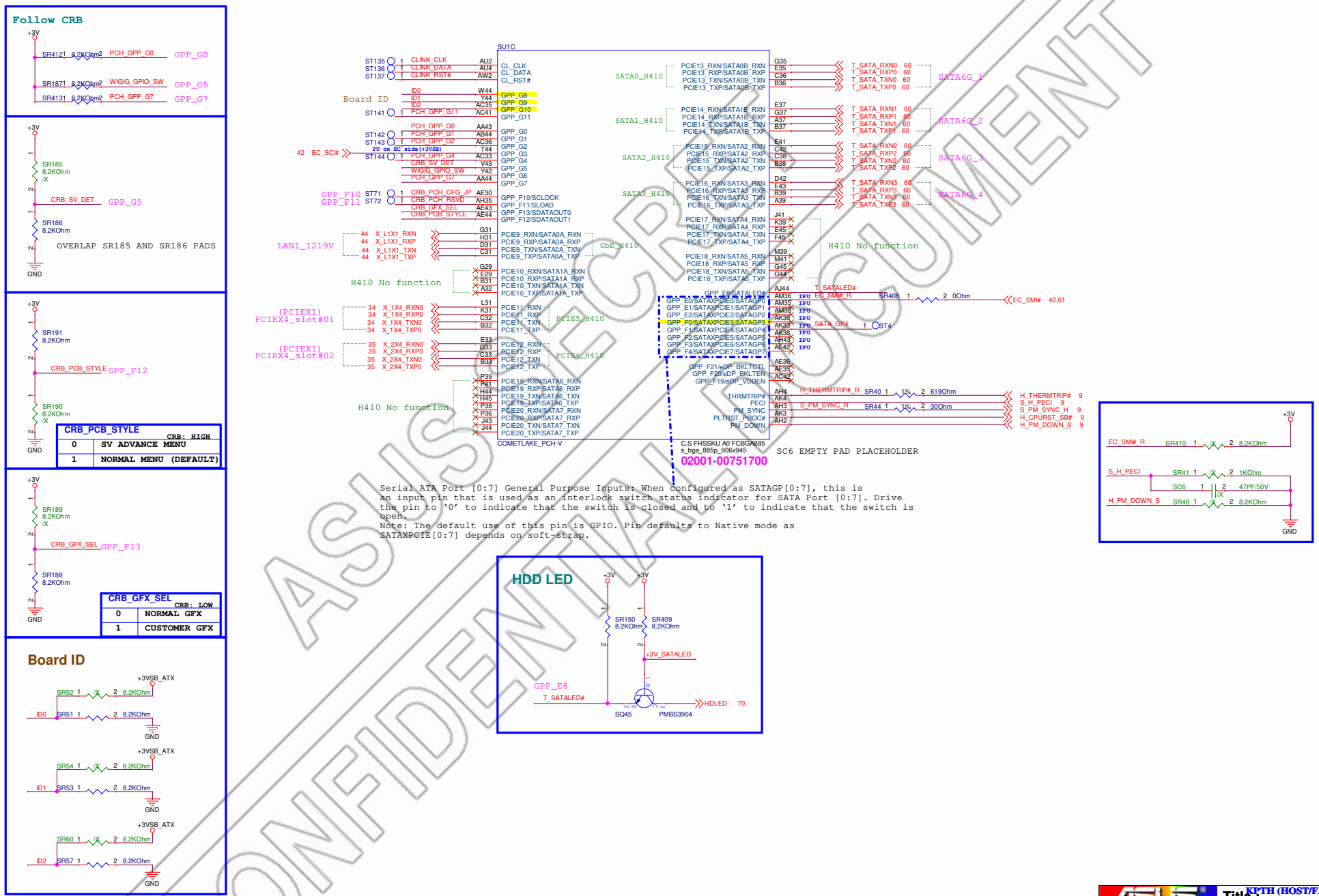
Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| Custom | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 19 of 87




| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : KPTH (AUDIO/SMBUS/MISC) | Engineer: IPC-EE3 |
| Size: Custom | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 20 of 87 | |




ASUS CONFIDENTIAL DOCUMENT

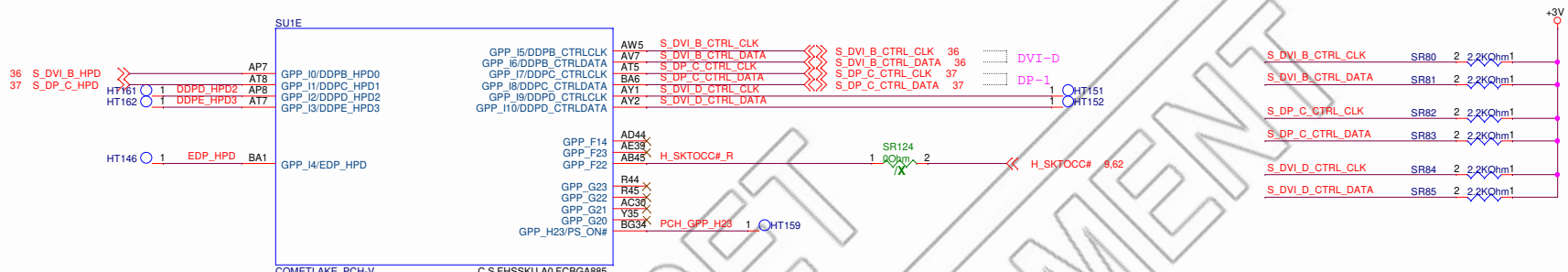
ASUSTek COMPUTER INC.

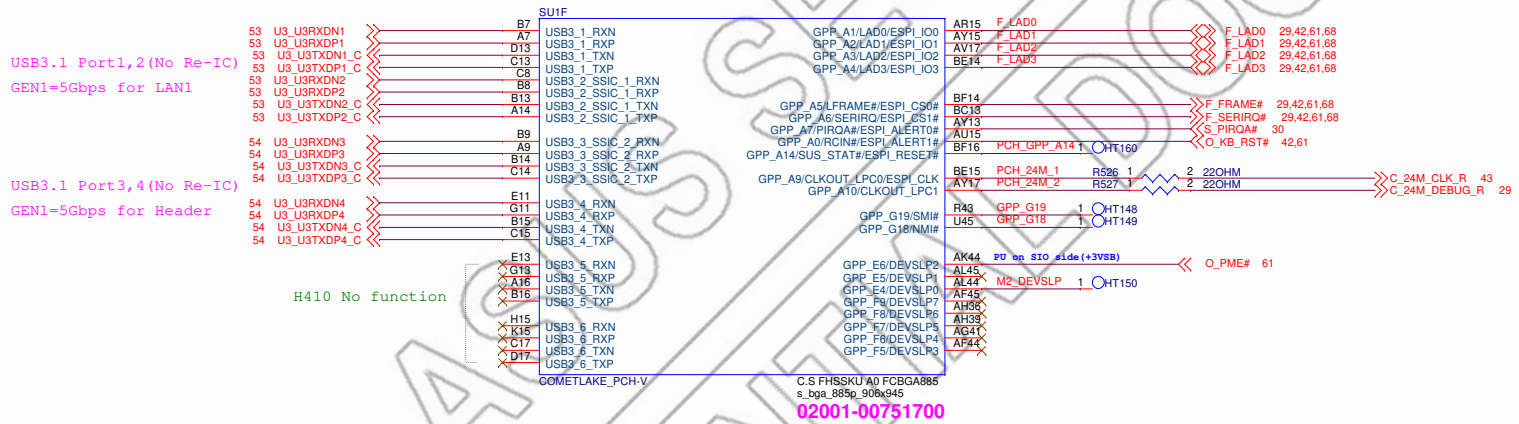
Title : KPTH (HOST/FAN/SATA)

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| Custom | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 21 of 87

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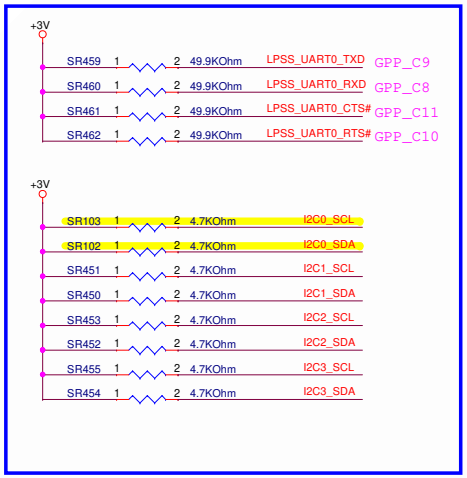
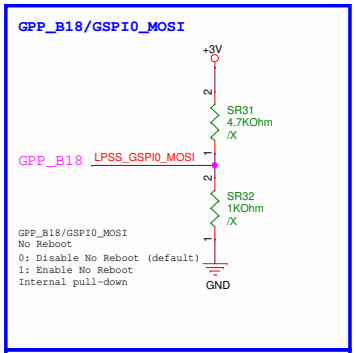
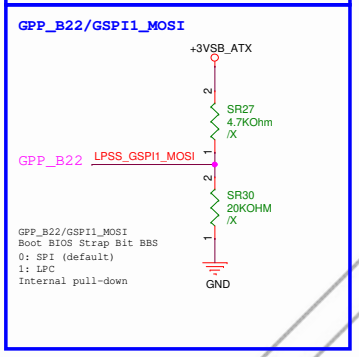
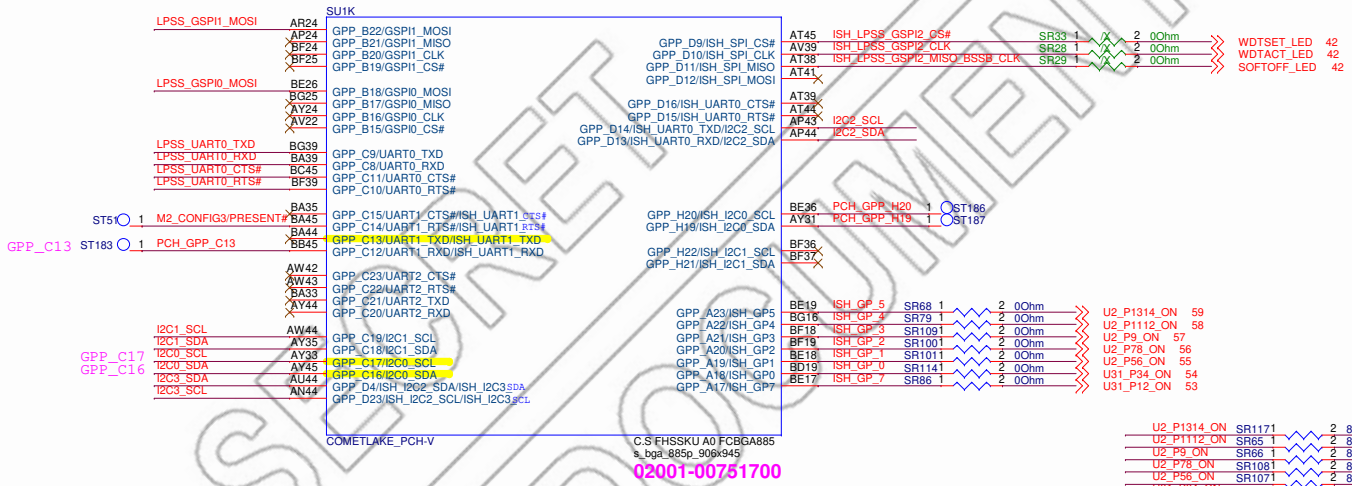
ASUS SECRET

| | | | |
|---|---|---|---|
| ASUS | Title : KPTH (DISPLAY/USB3) | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 22 of 87 | | |

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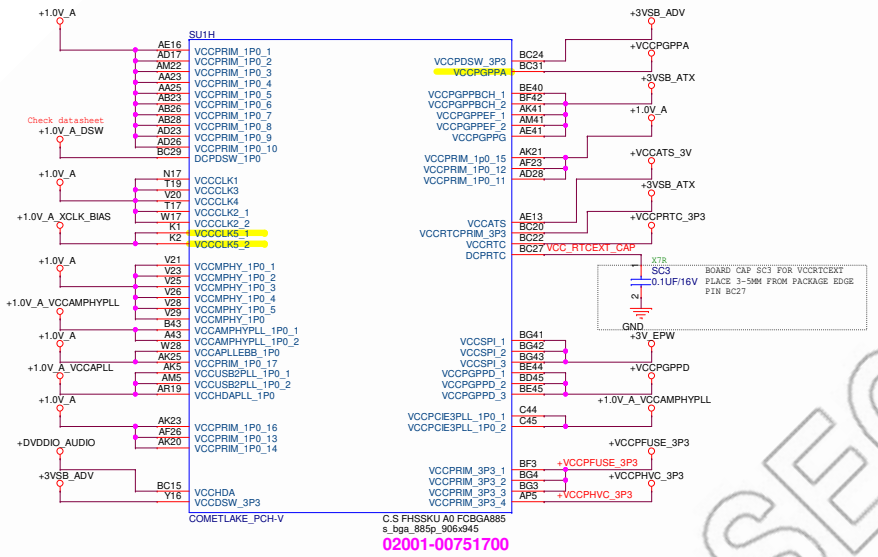
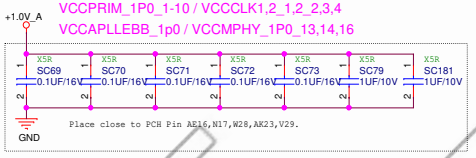
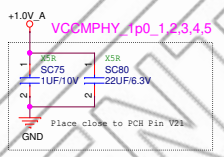
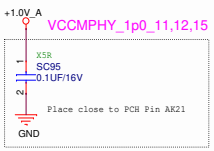
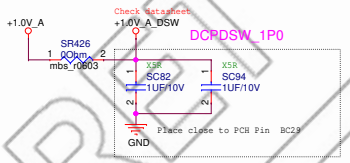
| | | |
|---|---|---|
| ASUS | Title : CPTH (GPIO) | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 23 of 87 | |

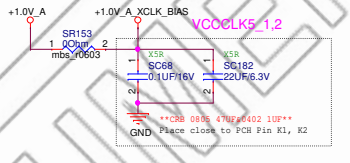


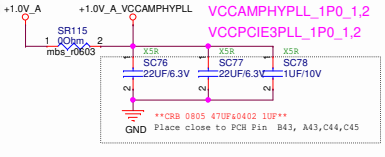



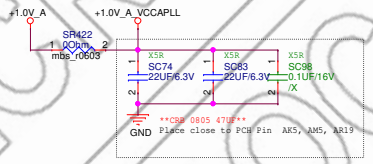



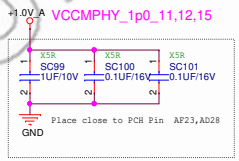



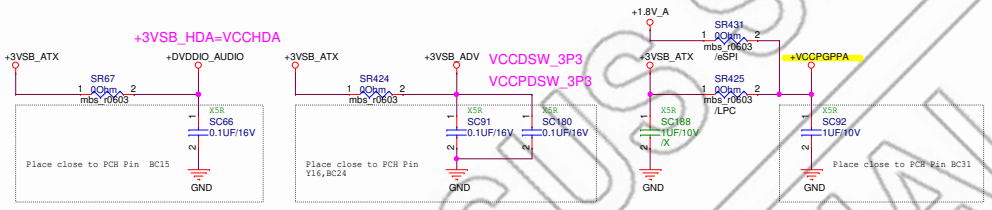



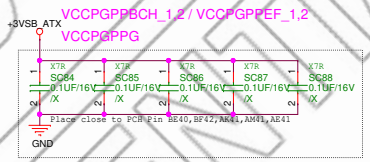



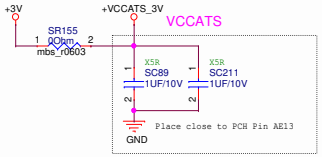

V3_12

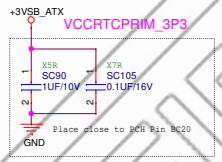
**CML PCH-V GPIO Voltage Level-SMS-H410**

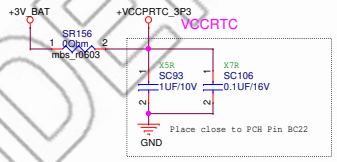
| Group | Power pin | Power option | Power plane |
|---|---|---|---|
| GPP_A | VCCPGPPA | 1.8V or 3.3V | +3VSB_ATX |
| GPP_B | VCCPGPPBCH | 1.8V or 3.3V | +3VSB_ATX |
| GPP_C | VCCPGPPBCH | 1.8V or 3.3V | +3VSB_ATX |
| GPP_D | VCCPGPPD | 1.8V or 3.3V | +3VSB_ATX |
| GPP_E | VCCPGPPEF | 1.8V or 3.3V | +3VSB_ATX |
| GPP_F | VCCPGPPEF | 1.8V or 3.3V | +3VSB_ATX |
| GPP_G | VCCPGPPG | 1.8V or 3.3V | +3VSB_ATX |
| GPP_H | VCCPGPPBCH | 1.8V or 3.3V | +3VSB_ATX |
| GPP_I | VCCPRIM_3P3 | 3.3V Only | +3VSB_ATX |
| GPD | VCCDSW_3P3 | 3.3V Only | +3VSB_ATX |

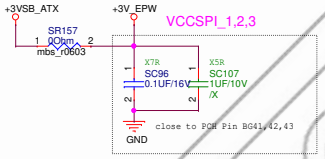
**PCH-V SPEC : GPP A~H,K 1.8V or 3.3V (+3VSB_ATX)**
**PCH-V SPEC : GPP I only 3.3V (VCCPRIM_3P3)**
**Deep Sleep Well Group (GPD) only 3.3V (VCCDSW_3P3)**

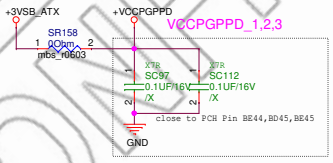


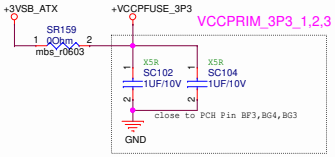



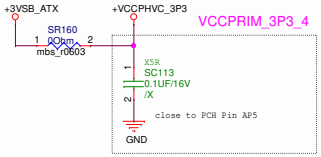




ASUS SECRET
CONFIDENTIAL DOCUMENT

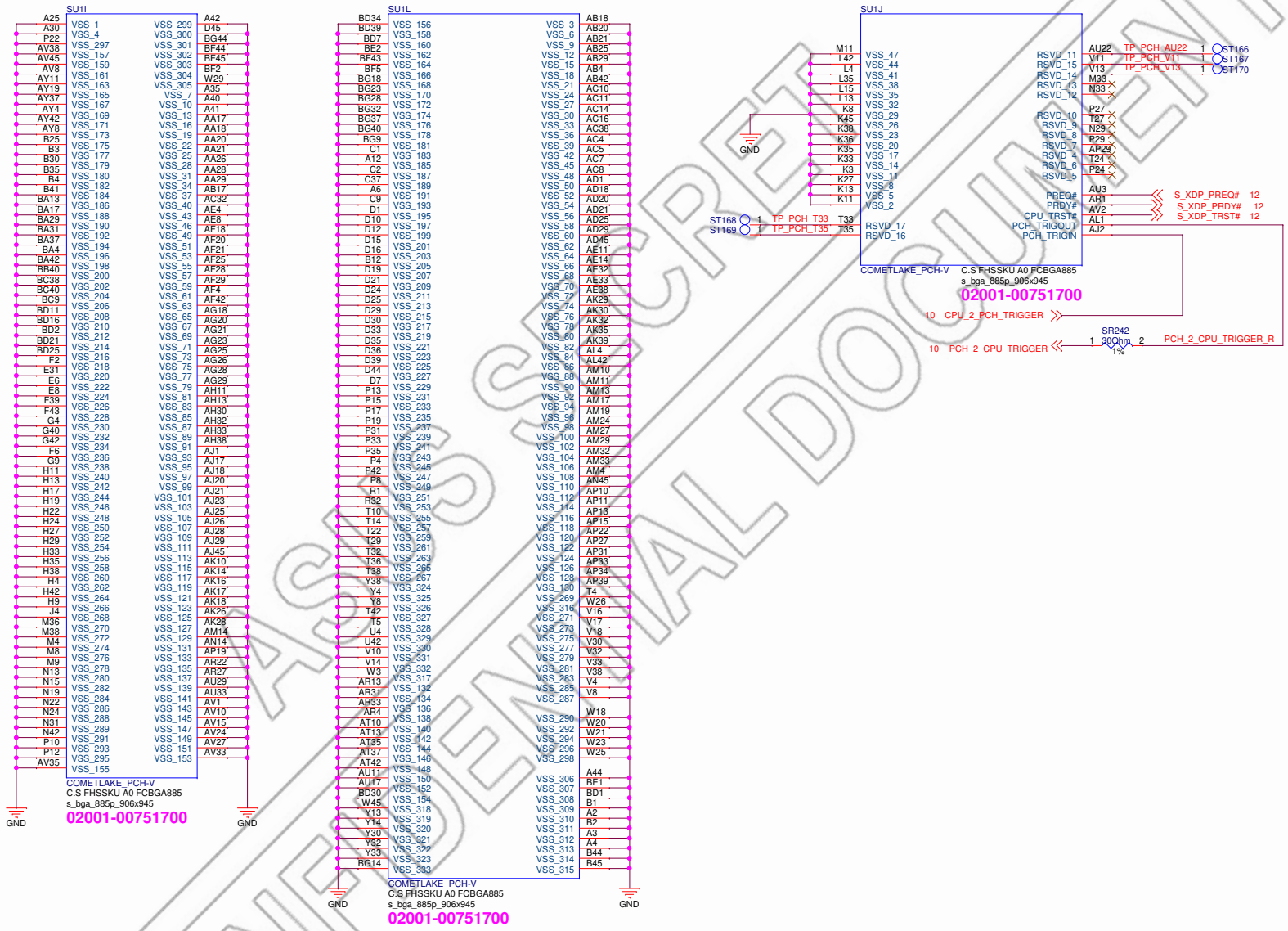
ASUSTek COMPUTER INC.

Title : KPTH (POWER)

Engineer: IPC-EE3

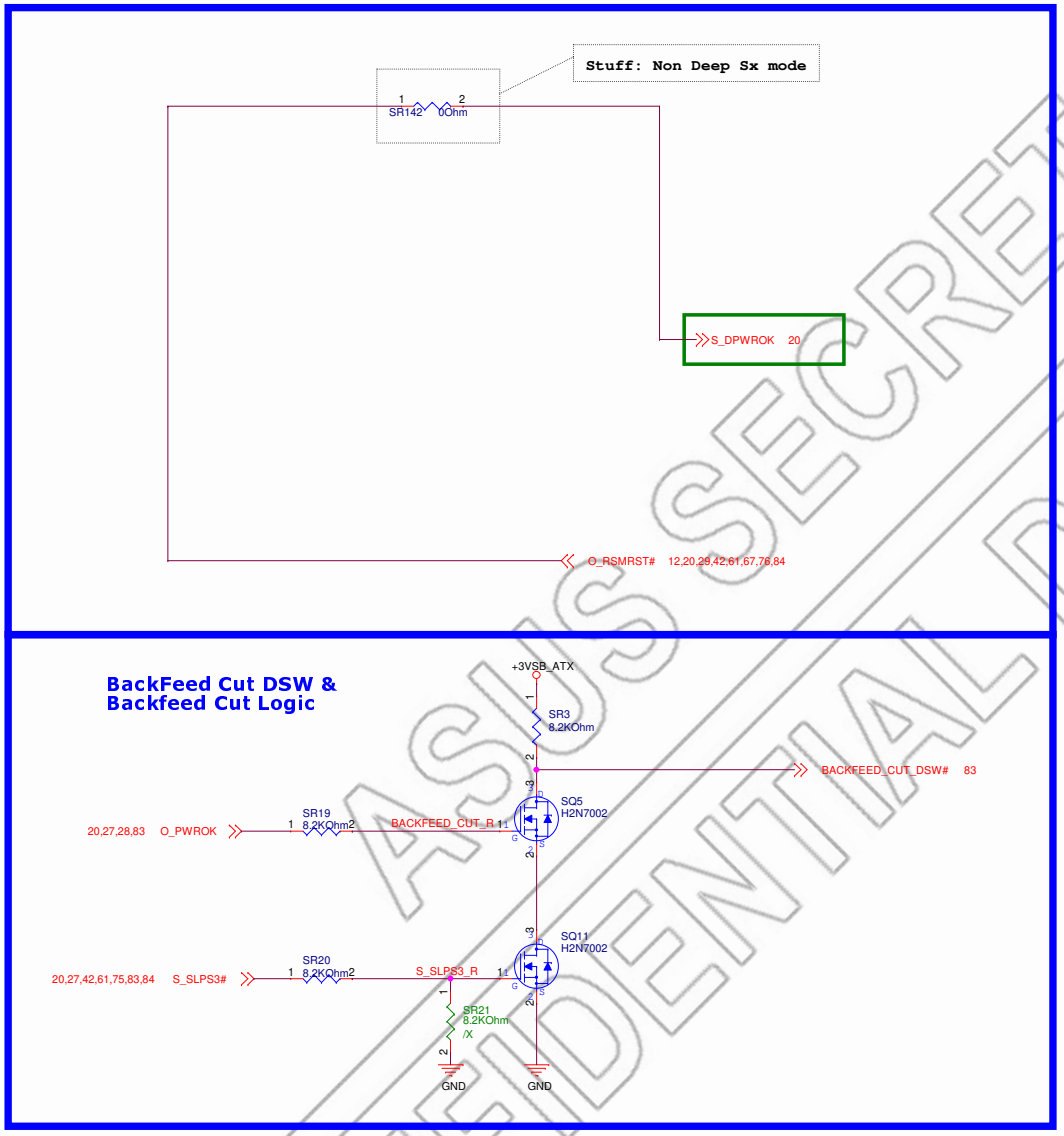
Size: Custom | Project Name: SMS-H410 | Rev: 1.00

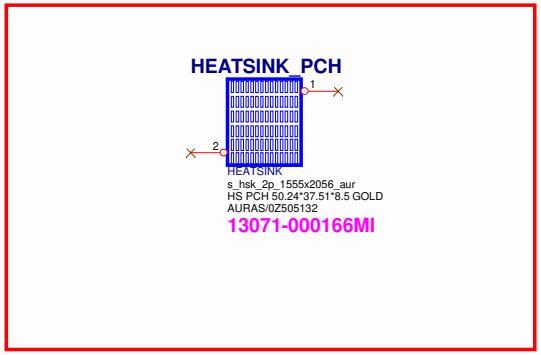
Date: Monday, March 16, 2020 | Sheet 24 of 87




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : CPTH (GND) | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 25 of 87 | |

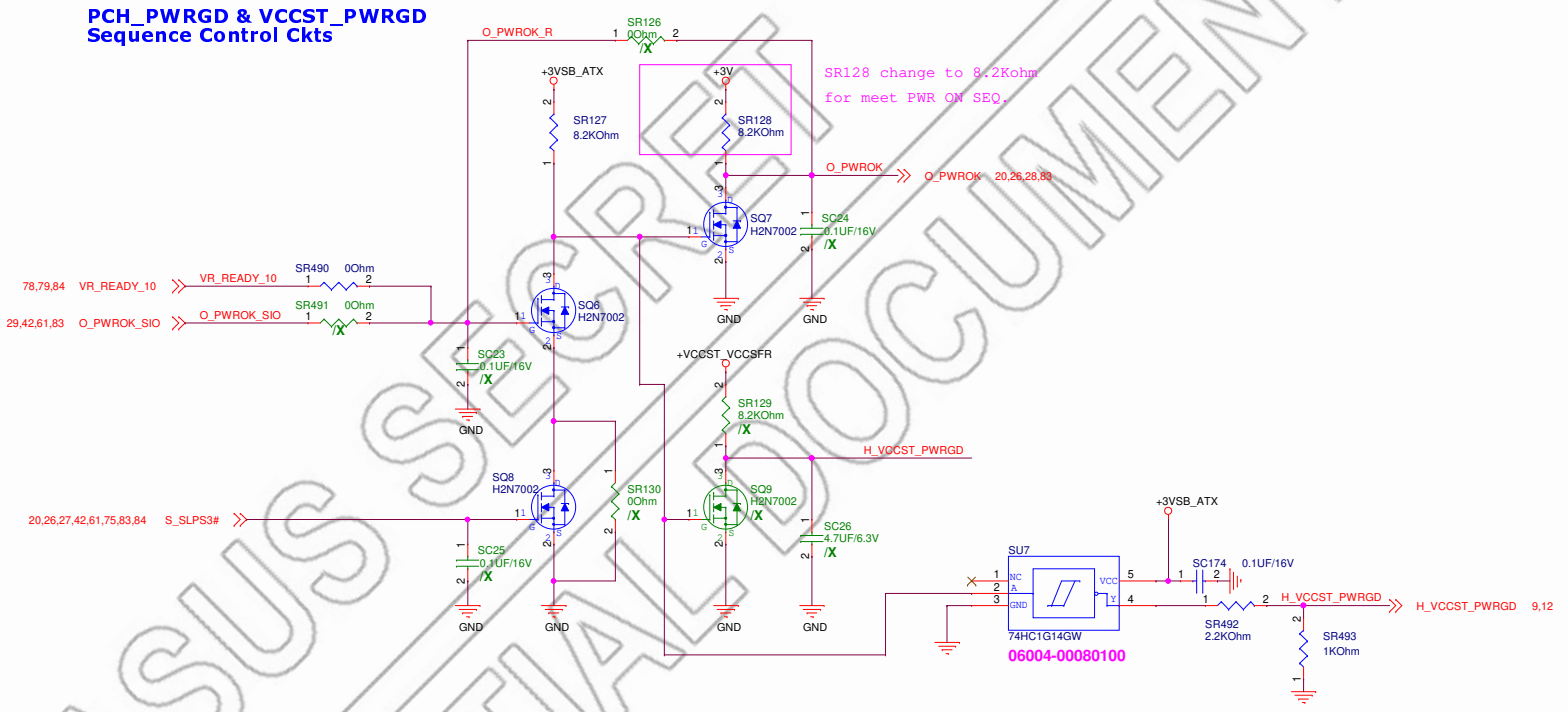


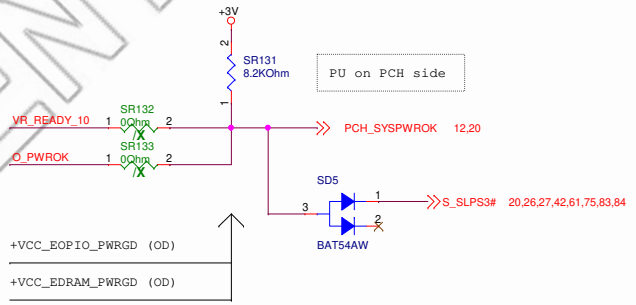

ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : CPTH (DSW SEQUENCE) | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 26 of 87 | |

## PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts




## PCH_SYSPWROK Sequence Control Ckts




1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

ASUS SECRET
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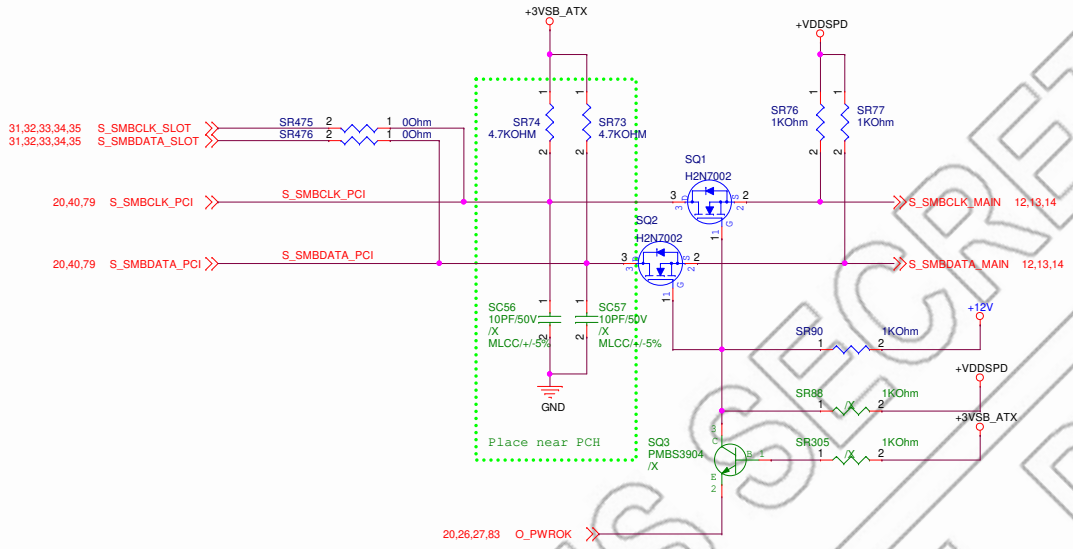
| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : CPTH (PCH/SYS/PROC_PWROK) | |
| | Engineer: IPC-EE3 | |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 27 of 87 | |

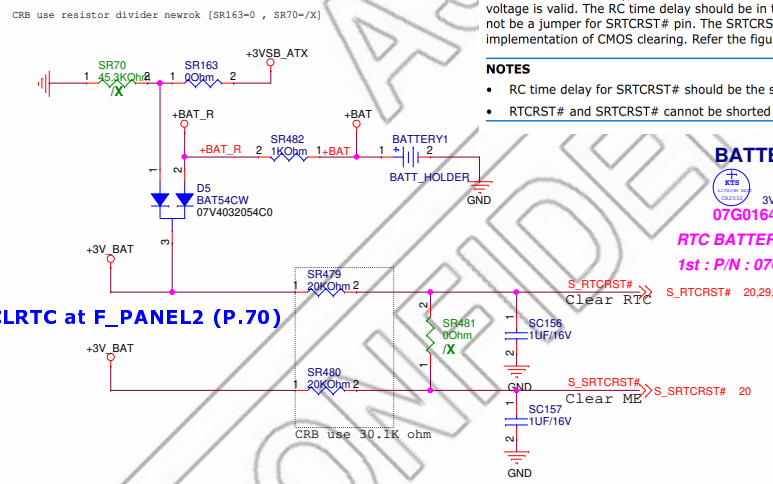



## RTC External SRTCRST# Circuit

The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18–25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer the figure above external circuit for PCH RTC.

**NOTES**

- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.



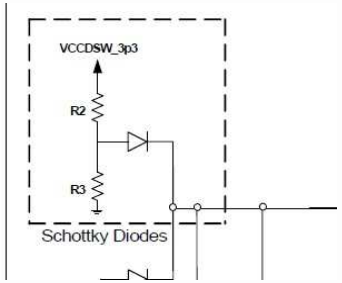

**BATTERY2**

3V/220mAh

07G016402032

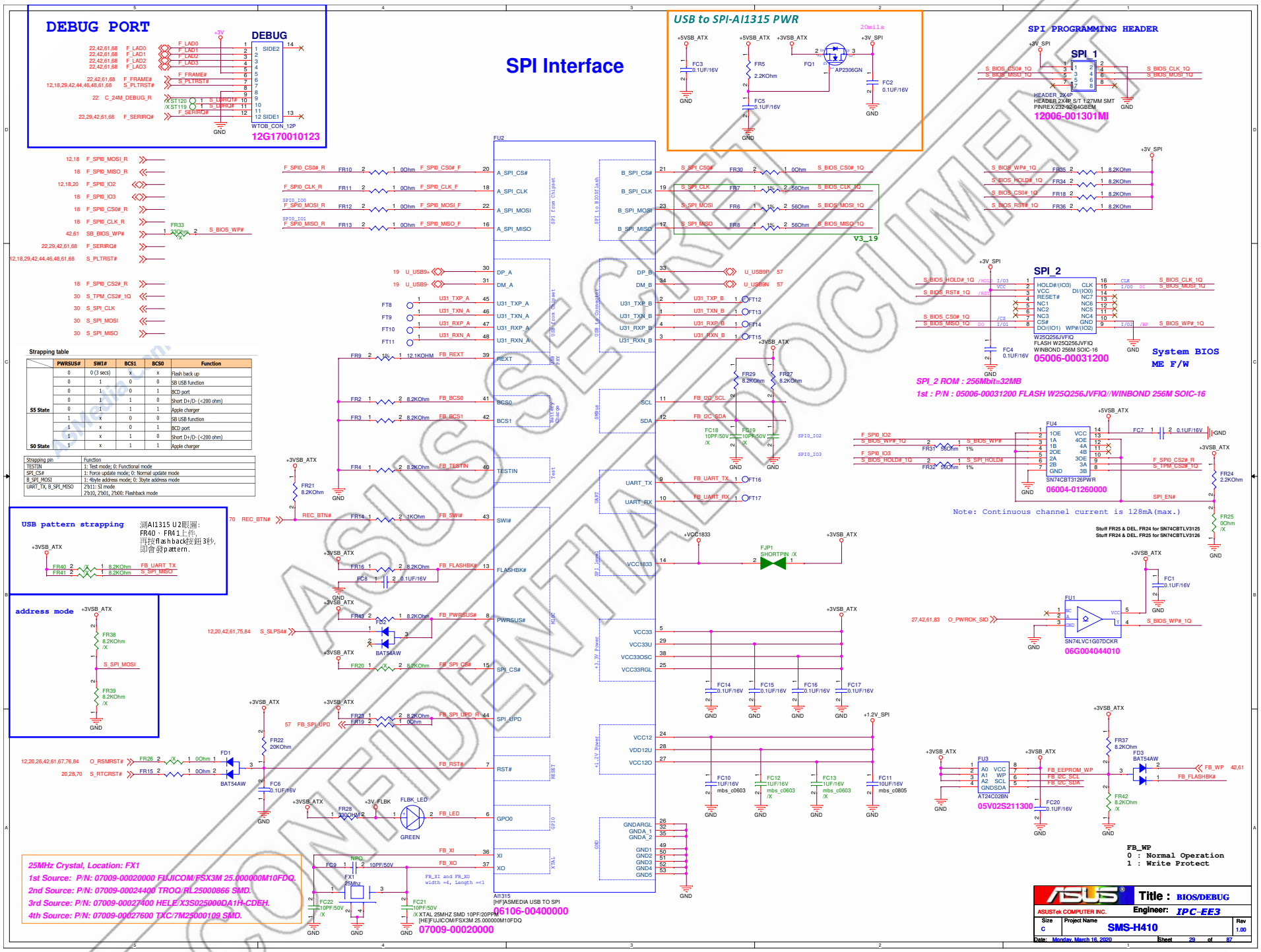
*RTC BATTERY2 Only*

*1st : P/N : 07G016402032 CR2032 3V/220mAh*



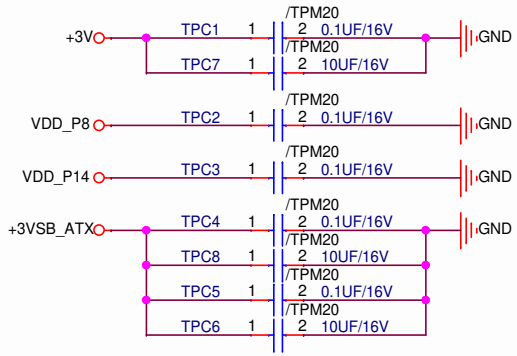

ASUS SECRET
CONFIDENTIAL DOCUMENT

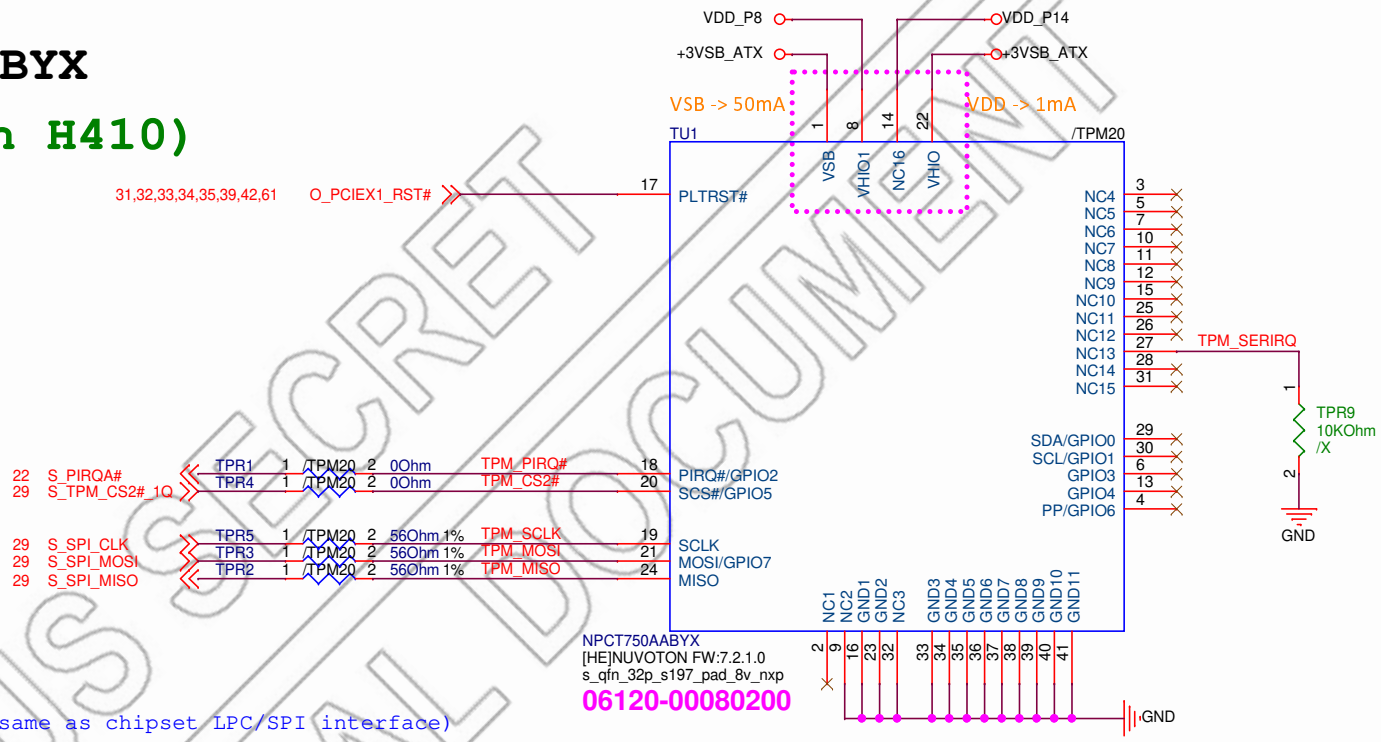
| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : CPTH (SMBUS/CLRTC) | Engineer: IPC-EE3 |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 28 of 87 | |


DEBUG PORT
DEBUG
WTOB_CON_12P
12G170010123
SPI Interface
USB to SPI-AI1315 PWR
AP2306GN
SPI PROGRAMMING HEADER
SPI_1
HEADER_2X4P
HEADER_2X4P S/T 1.27MM SMT
PINREX:232-92-04GBEM
12006-001301MI
SPI_2
W25Q256JVFIQ
FLASH W25Q256JVFIQ
WINBOND 256M SOIC-16
05006-00031200
System BIOS
ME F/W
SPI_2 ROM : 256Mbit=32MB
1st : P/N : 05006-00031200 FLASH W25Q256JVFIQ//WINBOND 256M SOIC-16
FU4
SN74CBT3126PWR
06004-01260000
Note: Continuous channel current is 128mA(max.)
Stuff FR25 & DEL. FR24 for SN74CBTLV3125
Stuff FR24 & DEL. FR25 for SN74CBTLV3126
FU1
SN74LVC1G07DCKR
06G004044010
FU3
AT24C02BN
05V02S211300
FB_WP
0 : Normal Operation
1 : Write Protect
Strapping table
USB pattern strapping
測AI1315 U2眼圖:
FR40、FR41上件,
再按flashback按鈕3秒,
即會發pattern.
address mode
FU2
AI1315
[HF]ASMEDIA USB TO SPI
06106-00400000
25MHz Crystal, Location: FX1
1st Source: P/N: 07009-00020000 FUJICOM FSX3M 25.000000M10FDQ.
2nd Source: P/N: 07009-00024400 TROQ/RL25000866 SMD.
3rd Source: P/N: 07009-00027400 HELE X3S025000DA1H-CDEH.
4th Source: P/N: 07009-00027600 TXC/7M25000109 SMD.
07009-00020000
ASUS CONFIDENTIAL DOCUMENT
Title : BIOS/DEBUG
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name SMS-H410
Rev 1.00
Date: Monday, March 16, 2020
Sheet 29 of 87

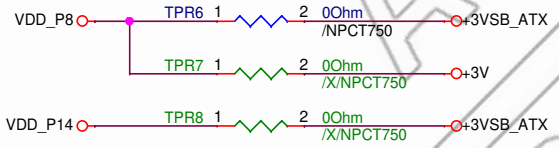
# TPM2.0_ NPCT750AABYX

## (Option /TPM20 in H410)




Note:
TPM.VDD change to +1.8V or +3.3V
TPM.VHIO change to +1.8V_SPI or +3V_SPI (same as chipset LPC/SPI interface)




| | NPCT650 | NPCT750 |
|---|---|---|
| TPR6 | x | v |
| TPR7 | v | x |
| TPR8 | v | x |
| TPR9 | v | x |

06120-00010800 NPCT650ABBYX TPM2.0 F/W:1.3.1.0
06120-00080200 NPCT750AABYX TPM2.0 F/W:7.2.1.0

(Pin.18) PIRQ#
It should be connected to one of PIRQ[A:D]# of Chipset inputs

(Pin.27) SERIRQ
for LPC interface use only

(Pin.17) SPI_RST#
PCI system reset used for LPC/SPI bus (Hardware reset)

(Pin.4) PP (Physical Presense Input)
By default the PP functionality is disabled.

GPIO[0:6] and PP are optional.
Leave them open if not used.

GPIO[0] contact to SLP_S0# for Connected Standby, if supported.

Windows10 Hardware Compatibility Specifications for RS3
Mandatory: The TPM must support driven communication.
Mandatory: The TPM interrupt pin must be connected to an interrupt controller.

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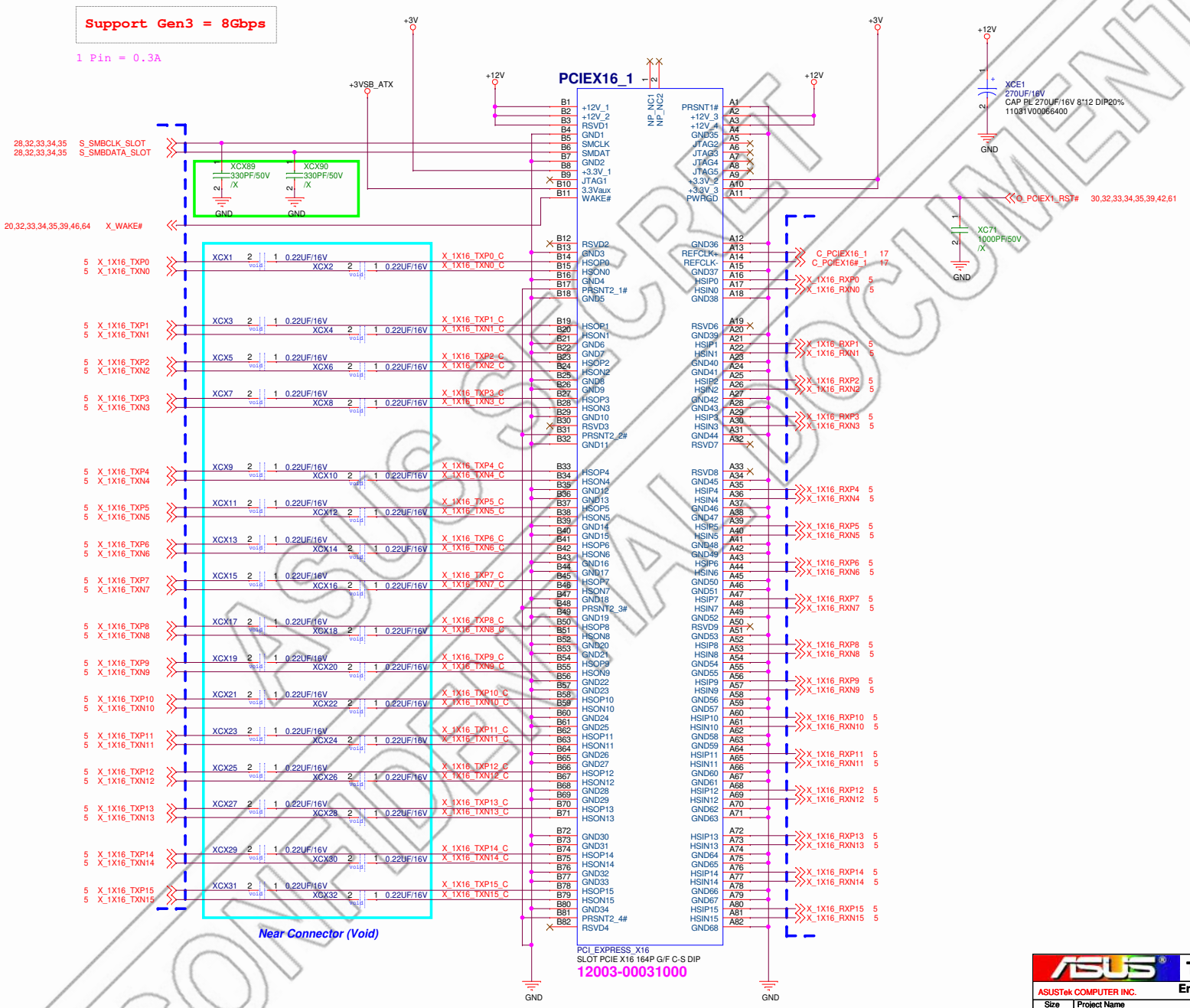
| | | |
|---|---|---|
| ASUS | Title : TPM_NPCT650ABBYX | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size A4 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 30 of 87 | |

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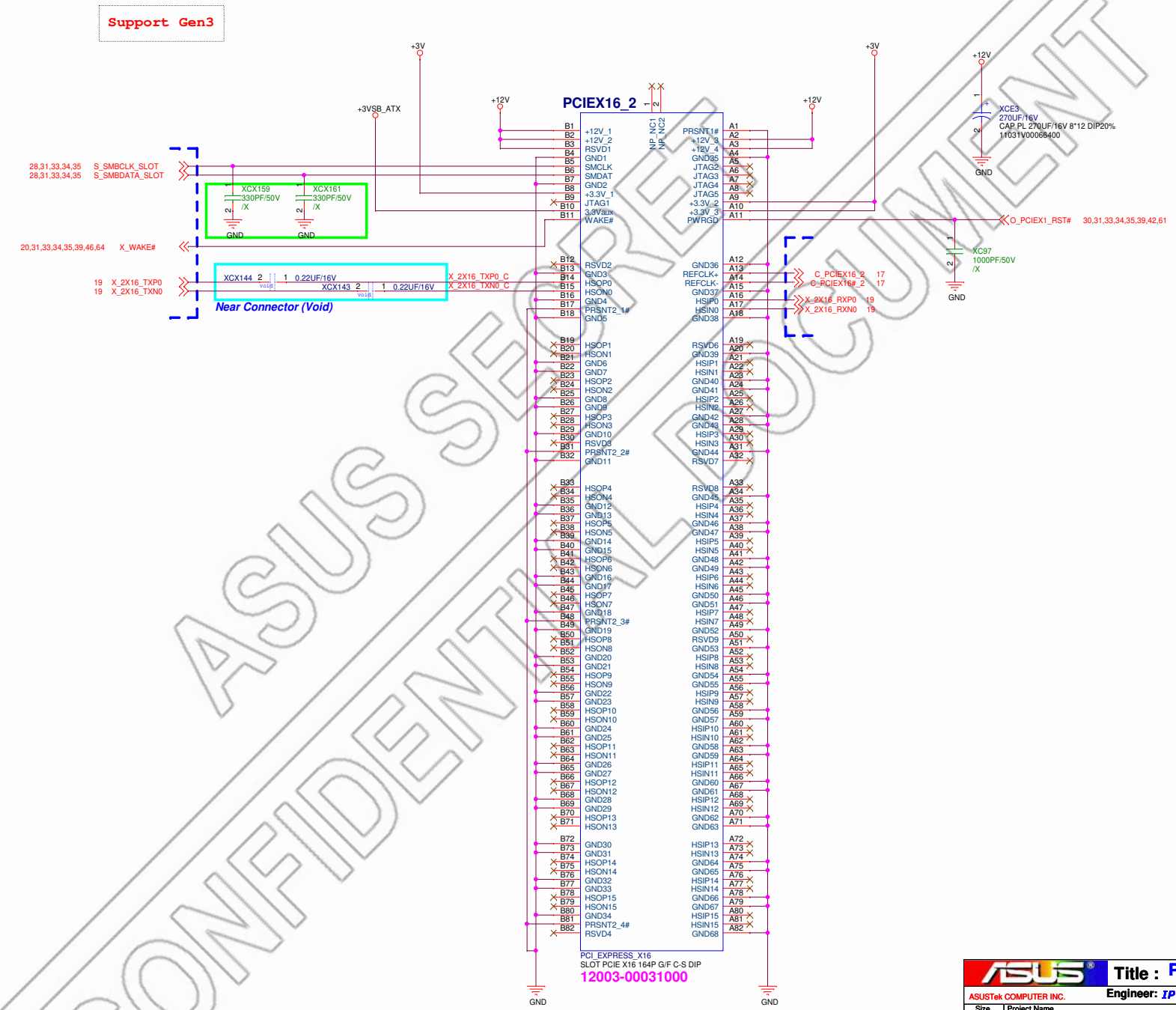
| | | | |
|---|---|---|---|
| ASUS | Title : PCIEX16_1 | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size: Custom | Project Name: SMS-H410 | | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 31 of 87 | | |




ASUS SECRET DOCUMENT
CONFIDENTIAL DOCUMENT

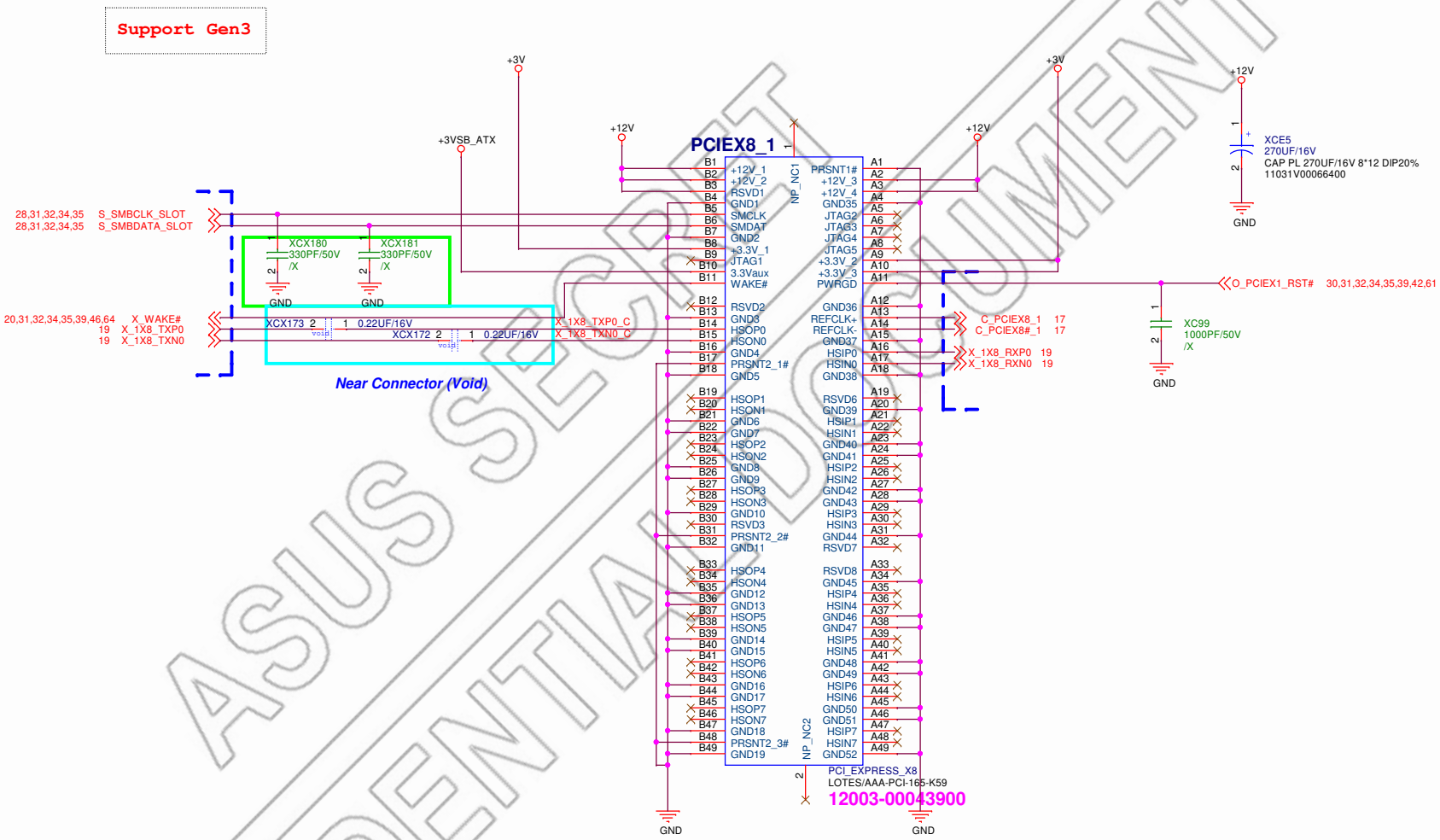
ASUSTek COMPUTER INC.

Title : PCIEX16_2

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| Custom | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 32 of 87




*SLOT PCIE X8 98P G/F BLK DIP*

*1st : P/N : 12003-00043900 LOTES/AAA-PCI-165-K59*

*2nd : P/N : 12003-00040000 FOXCONN/2EG04911-A7D-DF*

| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : PCIEX8 | |
| | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 33 of 87 | |

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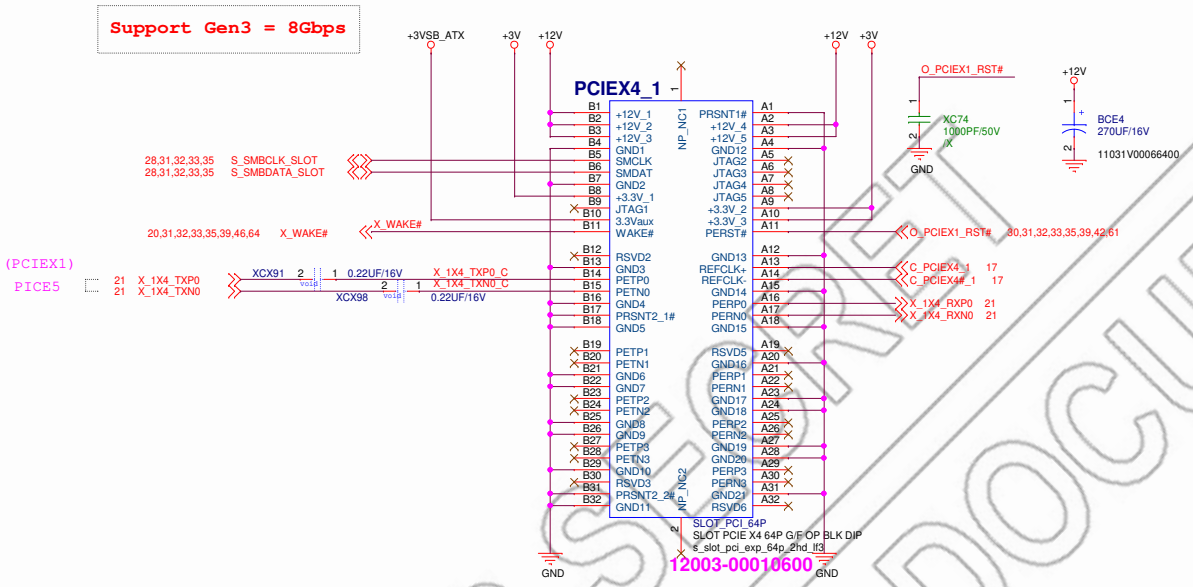


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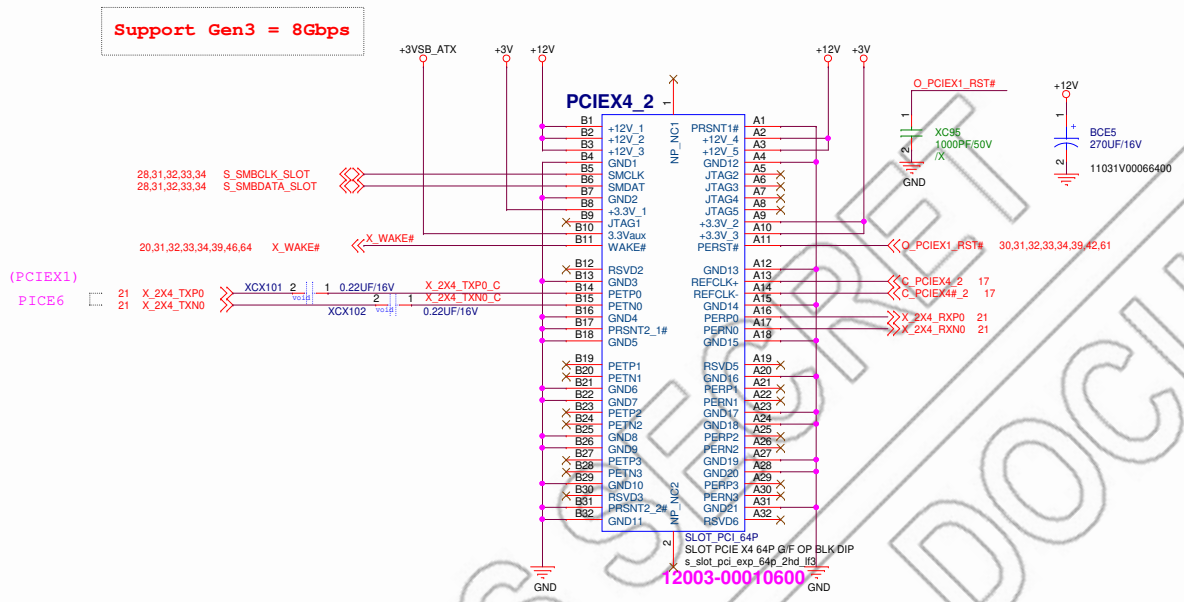
| | | |
|---|---|---|
| ASUS | Title : PCIEX4_1 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size: Custom | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 34 of 87 | |

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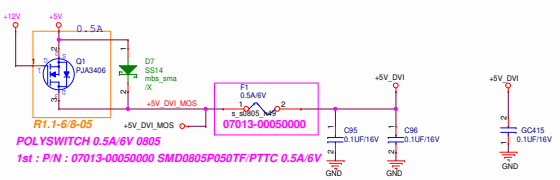
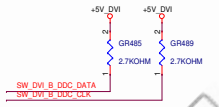
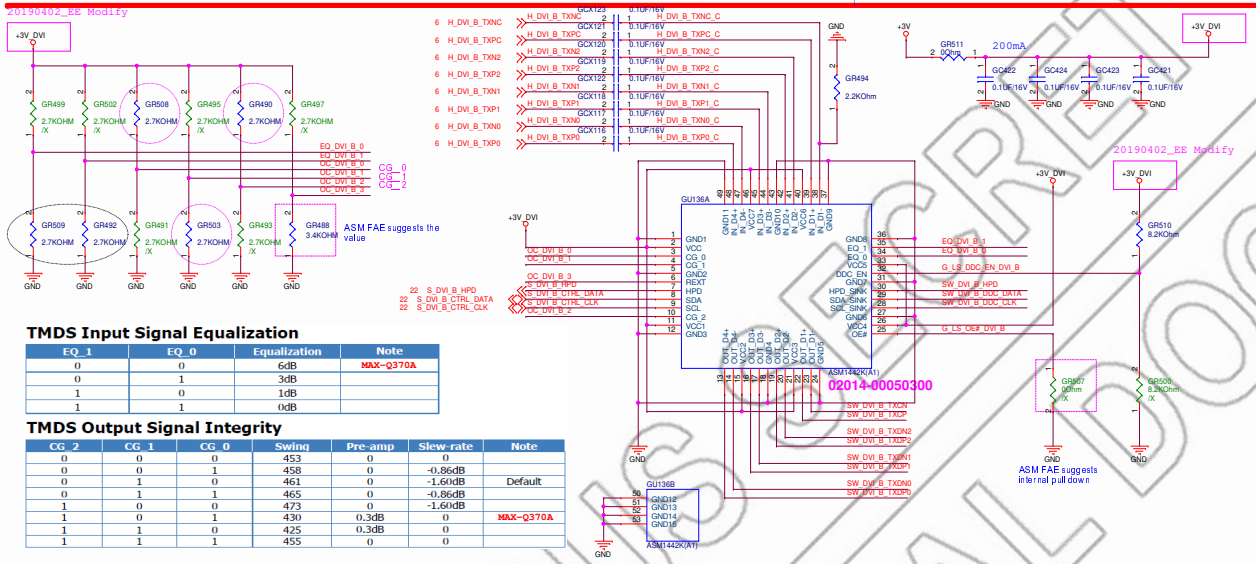
| | | |
|---|---|---|
| ASUS | Title : PCIEX4_2 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size: Custom | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 35 of 87 | |

# DVI PWR




# DVI DDC CLK/DAT



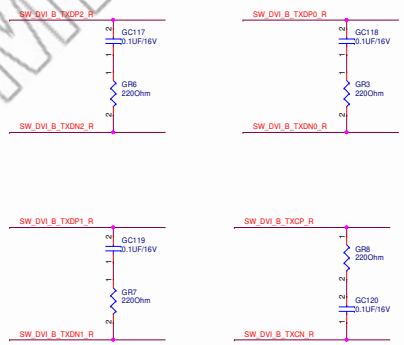

## TMDS Input Signal Equalization

| EQ_1 | EQ_0 | Equalization | Note |
|---|---|---|---|
| 0 | 0 | 6dB | MAX-Q370A |
| 0 | 1 | 3dB | |
| 1 | 0 | 1dB | |
| 1 | 1 | 0dB | |

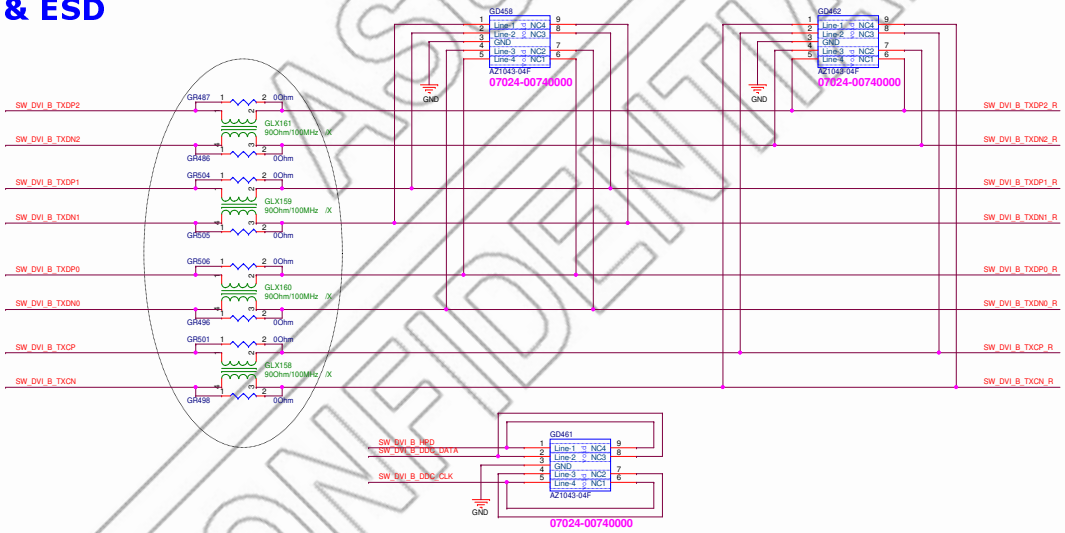
## TMDS Output Signal Integrity

| CG_2 | CG_1 | CG_0 | Swing | Pre-amp | Slew-rate | Note |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 453 | 0 | 0 | |
| 0 | 0 | 1 | 458 | 0 | -0.86dB | |
| 0 | 1 | 0 | 461 | 0 | -1.60dB | Default |
| 0 | 1 | 1 | 465 | 0 | -0.86dB | |
| 1 | 0 | 0 | 473 | 0 | -1.60dB | |
| 1 | 0 | 1 | 430 | 0.3dB | 0 | MAX-Q370A |
| 1 | 1 | 0 | 425 | 0.3dB | 0 | |
| 1 | 1 | 1 | 455 | 0 | 0 | |

# EMI



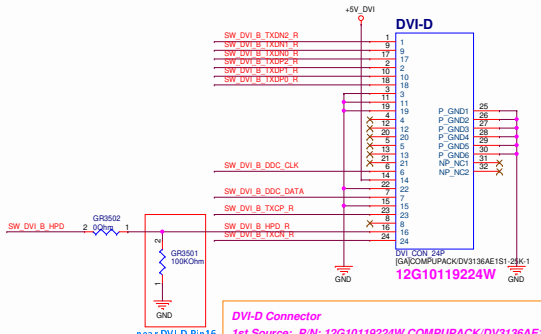

# EMI & ESD




ESD PROTECTION AZ1043-04F_Group : 07024V00740000
1st : P/N : 07024-00740000 AMAZING DFN2510P10E
2nd : P/N : 07024-00970000 AMAZING DFN2510P10E
3rd : P/N : 07024-01730500 WILLSEMI/ESD73044D-10/TR

# DVI Connector

DVI-D (Port B)




DVI-D Connector
1st Source: P/N: 12G10119224W COMPUPACK/DV3136AE1S1-25K-1.
2nd Source: P/N: 12010-00031100 LINGYANG/DVI024W-B003-00A3F2B.
3rd Source: P/N: 12010-00030900 FOXCONN/QH11121-2B5D-4F.

| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. | Title : DVI-D (Port B) | | |
| | Engineer: IPC-EE3 | | |
| Size: A2 | Project Name: SMS-H4 10 | | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 36 of 87 | | |

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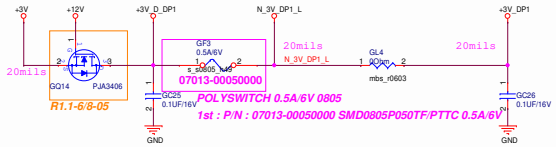
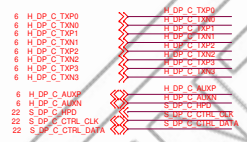
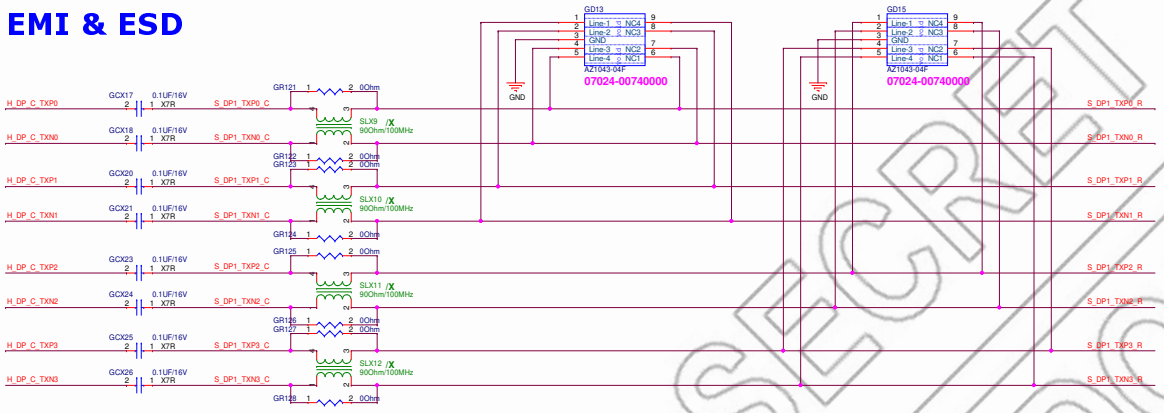
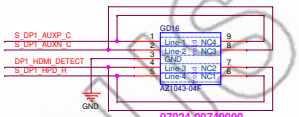
# DP PWR



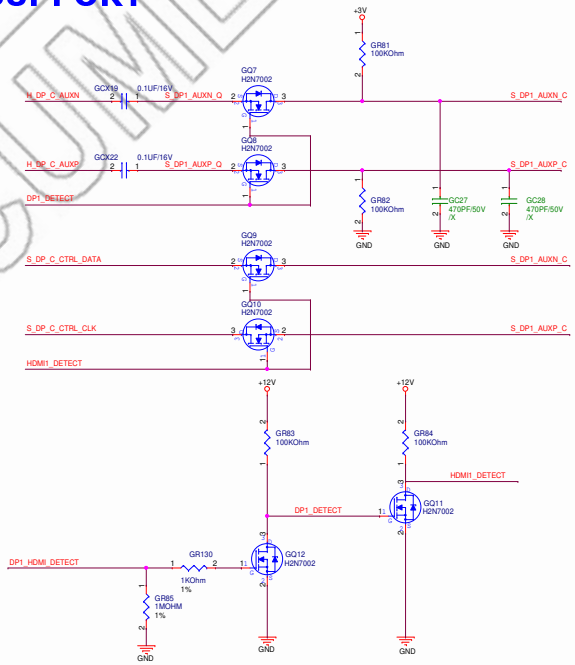

# EMI & ESD



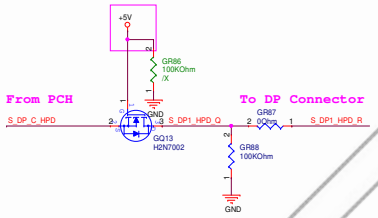

ESD PROTECTION AZ1043-04F_Group : 07024V00740000
1st : P/N : 07024-00740000 AMAZING DFN2510P10E
2nd : P/N : 07024-00970000 AMAZING DFN2510P10E
3rd : P/N : 07024-01730500 WILLSEMI/ESD7304D-10/TR

# DP/HDMI INTEROPERABILITY SUPPORT

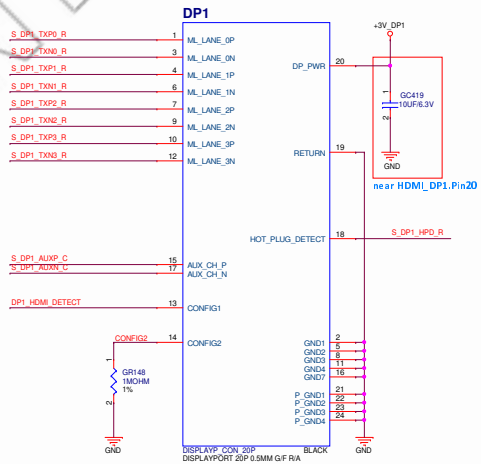



# DP_HPD

PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V 20191205_EE Modify




# DP Connector




| | |
|---|---|
| ASUSTeK COMPUTER INC. | Title : DP1 (Port C) |
| | Engineer: IPC-EE3 |
| Size: A2 | Project Name: SMS-H410 |
| Rev: 1.00 | |
| Date: Monday, March 16, 2020 | Sheet 37 of 87 |

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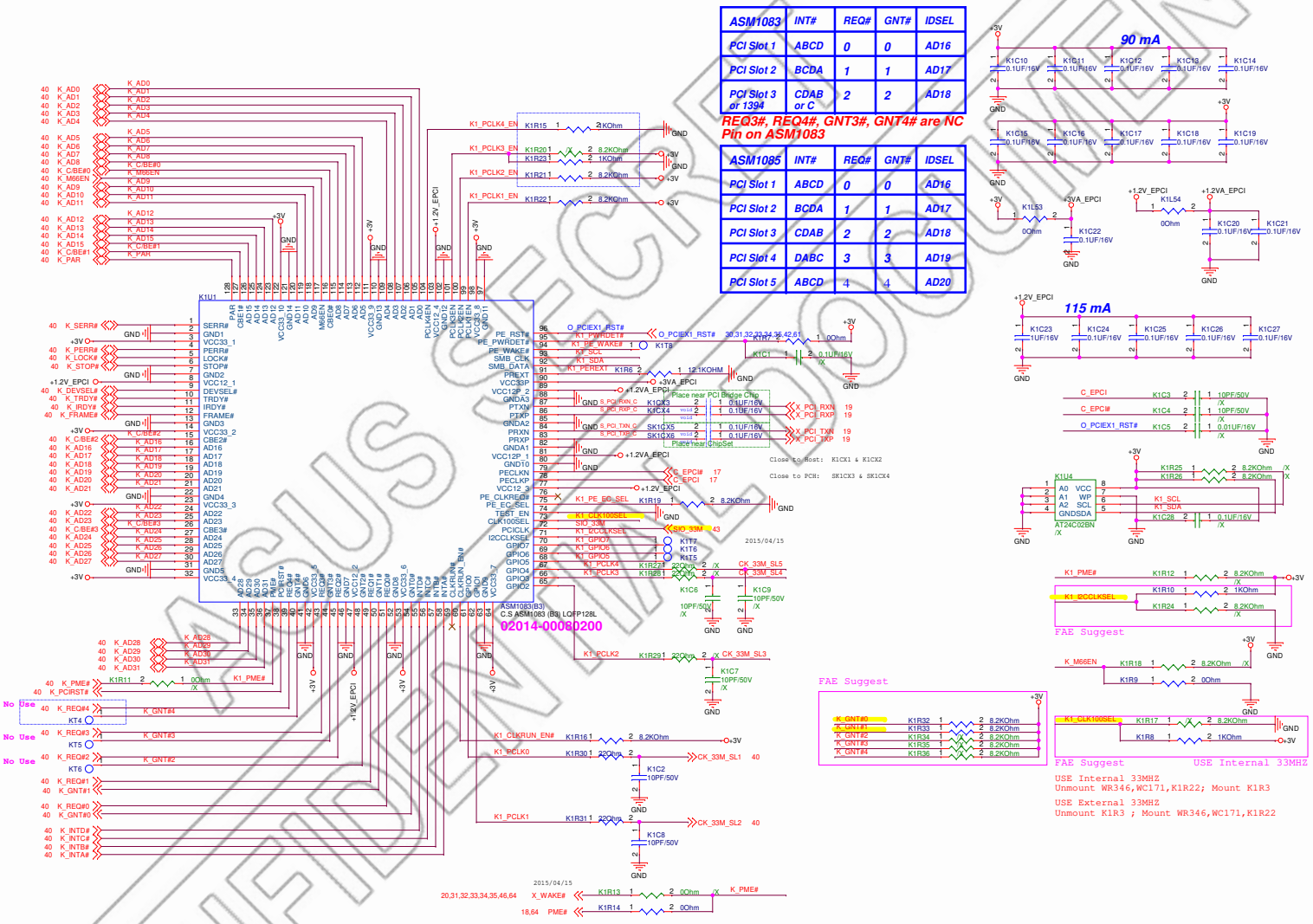
| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : xxxxx | |
| | Engineer: IPC-EE3 | |
| Size: Custom | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 38 of 87 | |

| ASM1083 | INT# | REQ# | GNT# | IDSEL |
|---|---|---|---|---|
| PCI Slot 1 | ABCD | 0 | 0 | AD16 |
| PCI Slot 2 | BCDA | 1 | 1 | AD17 |
| PCI Slot 3 or 1394 | CDAB or C | 2 | 2 | AD18 |

REQ3#, REQ4#, GNT3#, GNT4# are NC Pin on ASM1083

| ASM1085 | INT# | REQ# | GNT# | IDSEL |
|---|---|---|---|---|
| PCI Slot 1 | ABCD | 0 | 0 | AD16 |
| PCI Slot 2 | BCDA | 1 | 1 | AD17 |
| PCI Slot 3 | CDAB | 2 | 2 | AD18 |
| PCI Slot 4 | DABC | 3 | 3 | AD19 |
| PCI Slot 5 | ABCD | 4 | 4 | AD20 |




ASUSTek COMPUTER INC.

Title : EXT_PCI_ASM1083

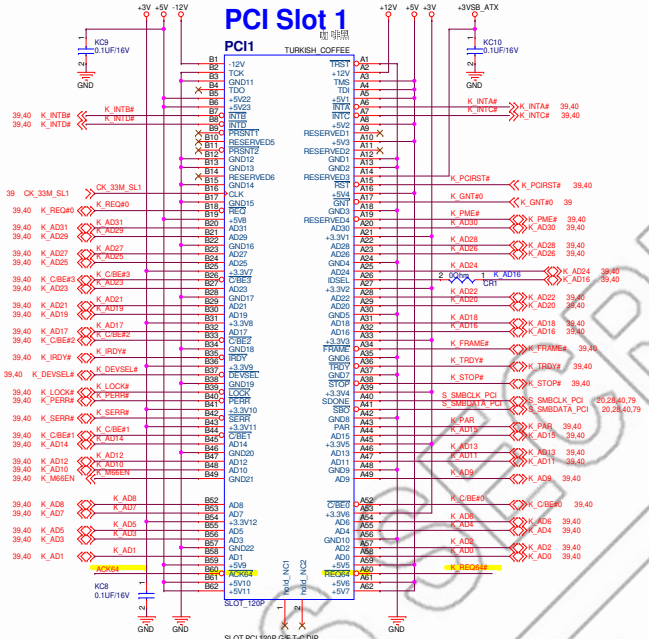
Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| C | SMS-H410 | 1.00 |

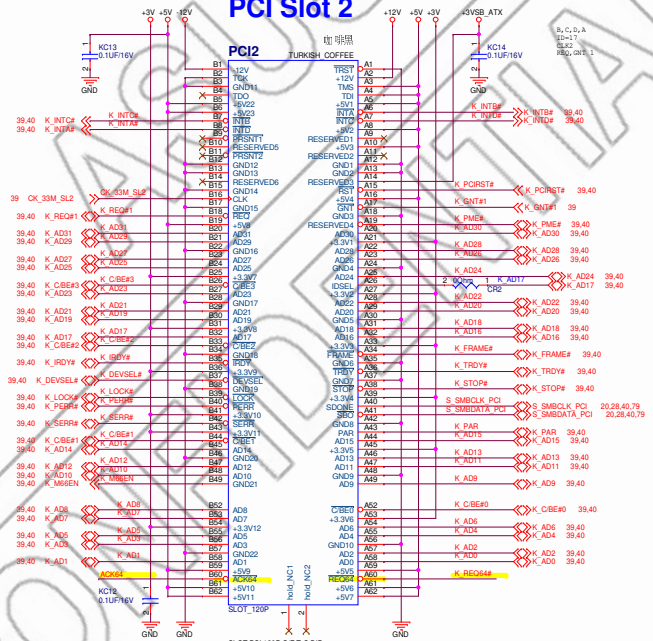
Date: Monday, March 16, 2020 Sheet 39 of 87

ASUS SECRET
CONFIDENTIAL DOCUMENT

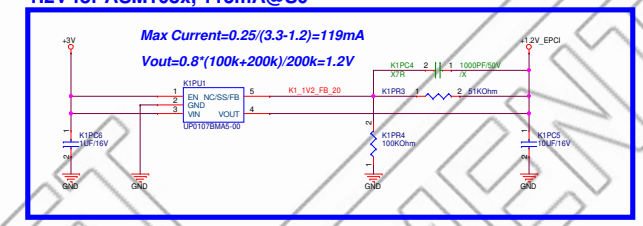
# PCI Slot 1



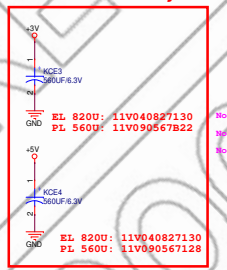

# PCI Slot 2

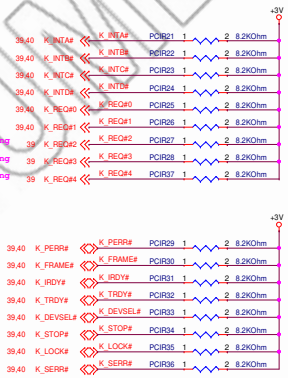


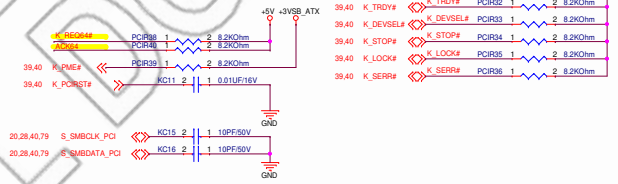

## 1.2V for ASM108x, 115mA@S0



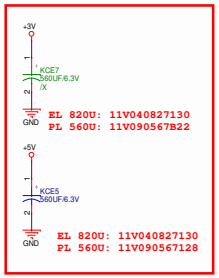

## PL & EL CAP co-lay



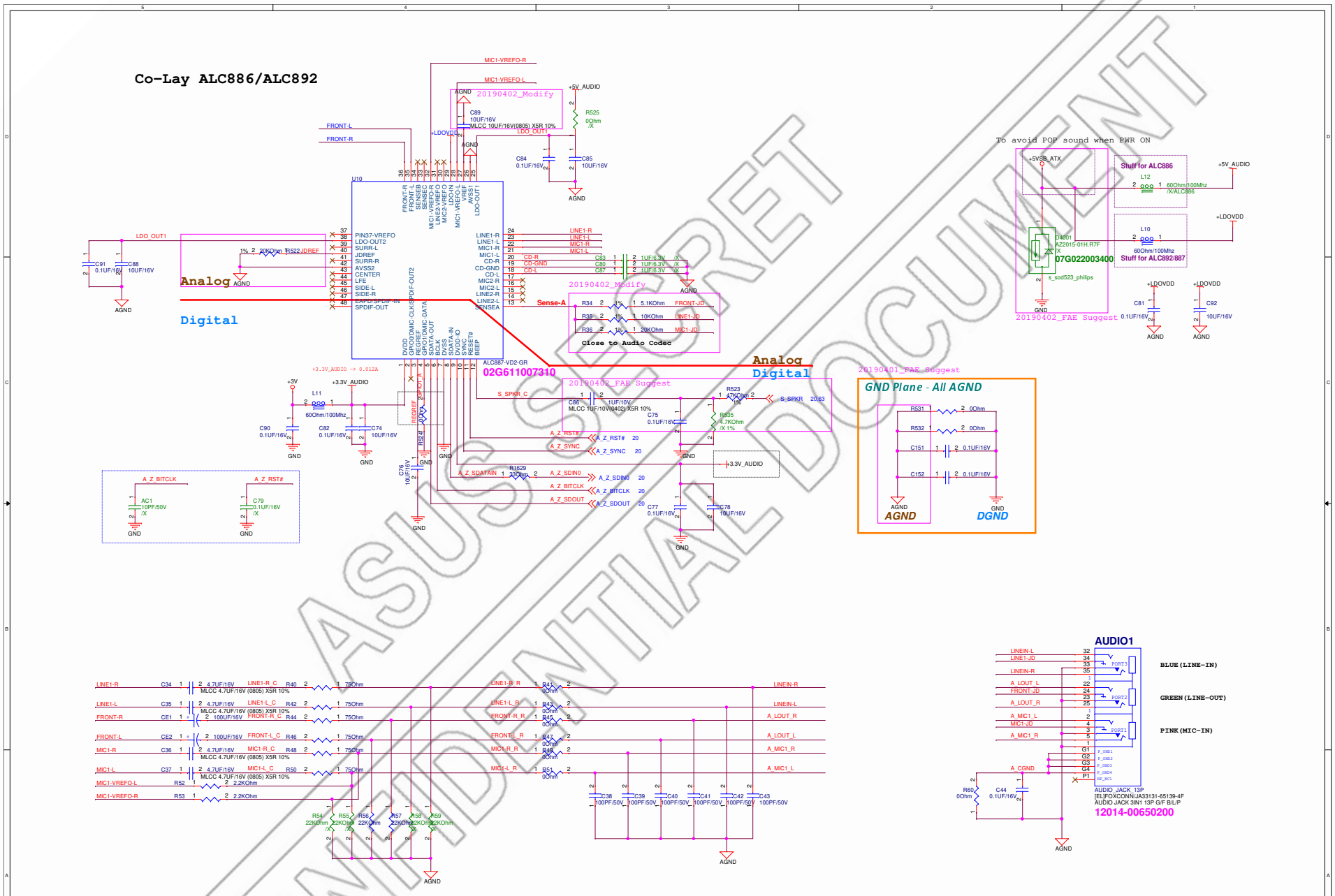



## PL & EL CAP co-lay




ASUSTeK COMPUTER INC. CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : SLOT_EXT_PCI_1_2 | Engineer: IPC-EE3 |
| Size A2 | Project Name SMS-H4 10 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 40 of 87 | |




CONFIDENTIAL DOCUMENT
ASUS SECRET

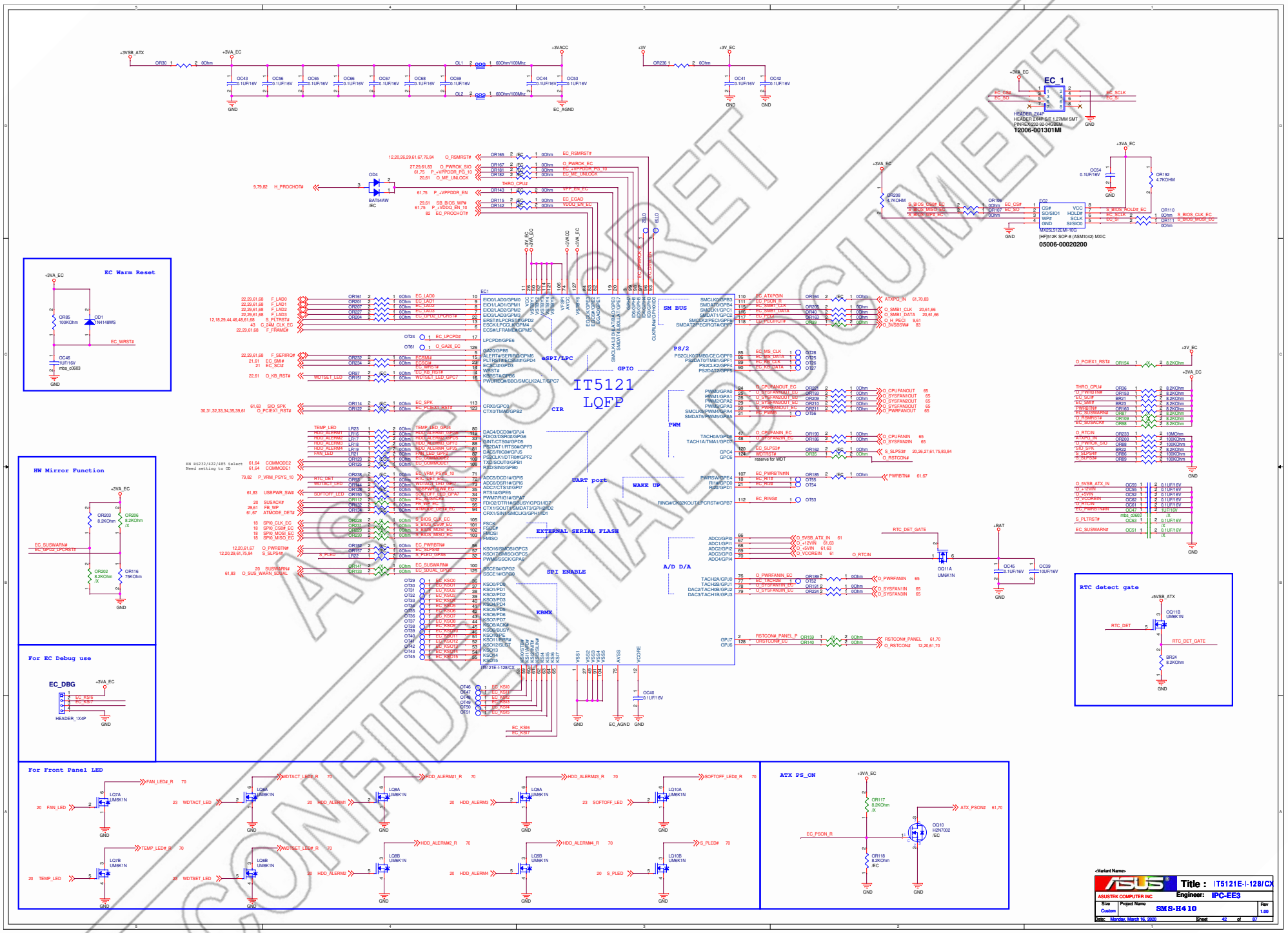
ASUSTek COMPUTER INC.

Title : AUDIO CODEC ALC887

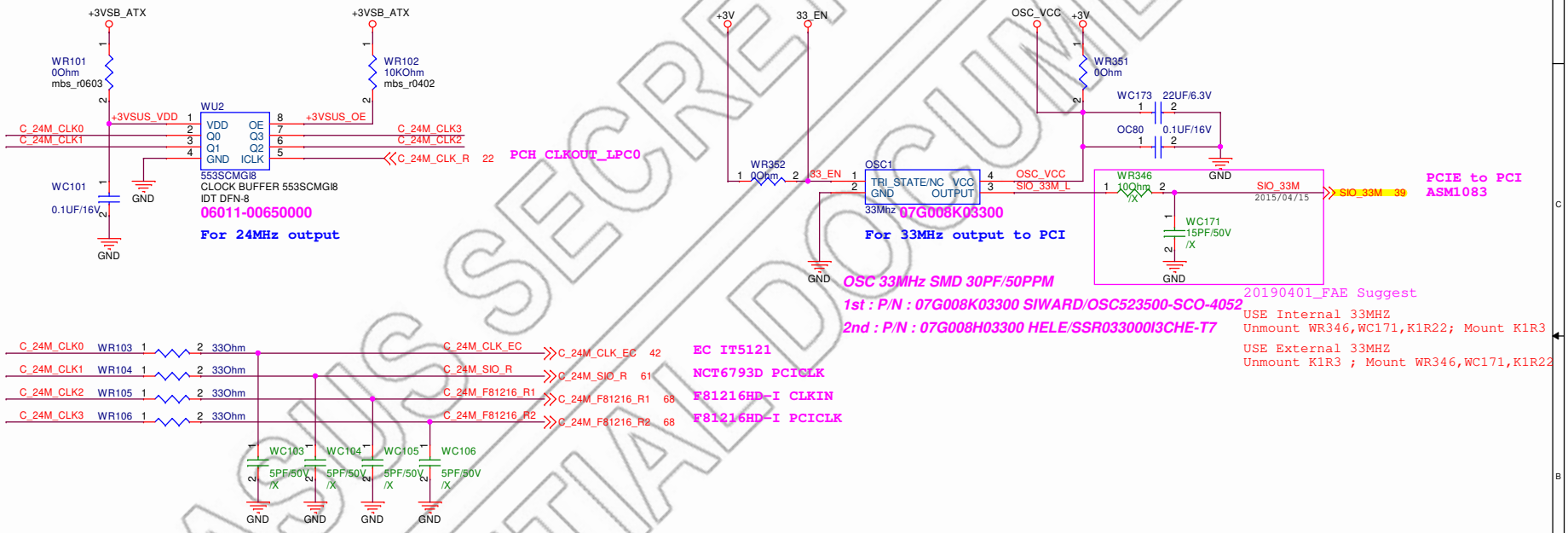
Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| C | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 41 of 87




CONFIDENTIAL DOCUMENT




| | | |
|---|---|---|
| ASUS | Title : Clock Buffer | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 43 of 87 | |

ASUS SECRET
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若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.

R1.00
Ref to page.104 +5VDUAL/5V_DUAL_USBKB*

**+L1_I218_+3VSB**
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.

LAN1_WGI219LM-25MHz Crystal, Location: L1X1
1st Source: P/N: 07009-00020000 FUJICOM/FSX3M 25.000000M10FDQ.
2nd Source: P/N: 07009-00024400 TROQ/RL25000866 SMD.
3rd Source: P/N: 07009-00027400 HELE/X3S025000DA1H-CDEH.
4th Source: P/N: 07009-00027600 TXC/7M25000109 SMD.

| Standard Circuit | |
|---|---|
| LAN | I218V |
| REV. | L1_1.3 |

1.3

**PCIE IF**
勿接在chipset PCIE port0

**L1_SMBCLK & L1_SMBDATA**
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.

**L1_LAN_DISABLE#**
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

**Internal SVR**
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0

**L1_CTRLP**
請注意灰框net為Switching power noise較大的地方
1. 所有訊號需距離灰框net至少30 mil
2. 所有訊號請勿reference該power plane
3. 該power net請reference GND plane並與其他GND切割, follow switching power phase的做法
4. L1L1元件中間請勿走線
5. L1_CTRLP長度勿超過100mil,越短越好

**L1_LAN_WAKE# pull-up**
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電

**L1_LAN_WAKE#**
Must be connected to PCH's LANWAKE

**L1X1,L1C7,L1C8**
Placement rule:
1.Place close to L1U1
2.Trace length <1inch

07009-00020000

**L1R16**
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch

LAN WGI219V 936401
[HF]INTEL QFN48 SLKJ5 TRAY
06112-00020000

06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)

06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)

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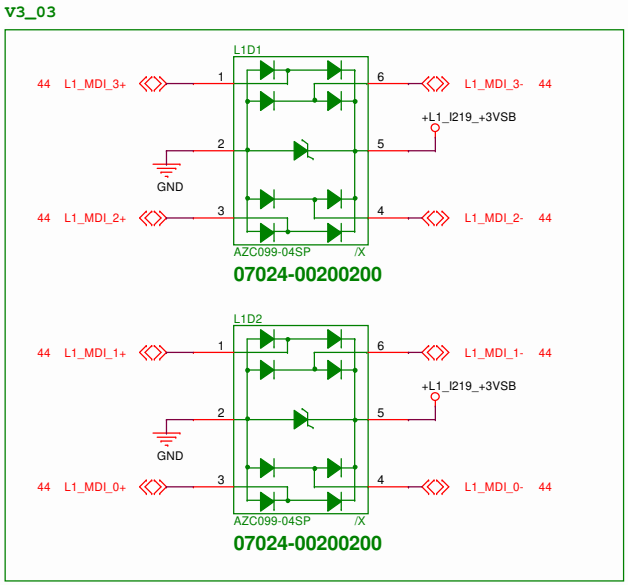
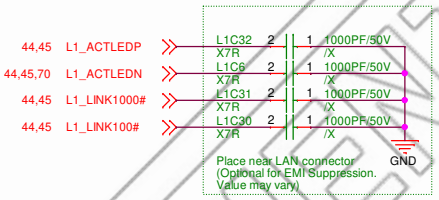
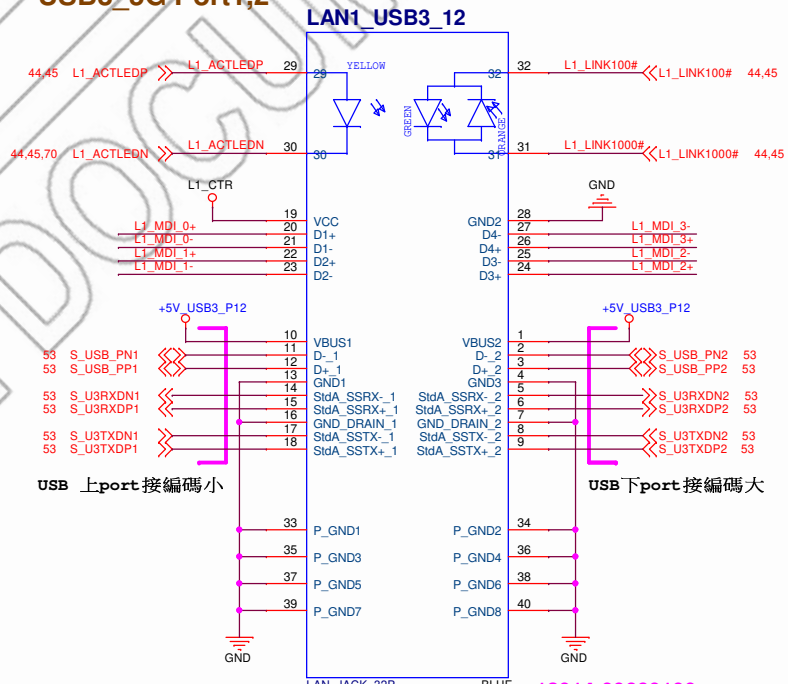
CONFIDENTIAL DOCUMENT

ASUSTek COMPUTER INC.
Title : L1_I219V
Engineer: IPC-EE3
Size A3 | Project Name SMS-H410 | Rev 1.00
Date: Monday, March 16, 2020 | Sheet 44 of 87



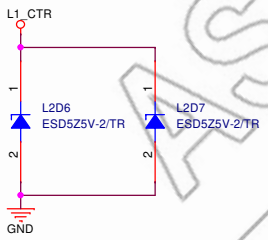



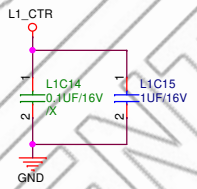

## USB3_5G Port1,2

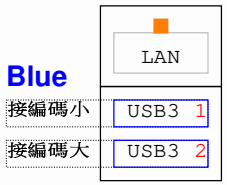



12014-00660100

IPC BU Pool List :
LAN+USB2 CONN: 12014-00670800
LAN+USB3 CONN: 12014-00660100




| | | | |
|---|---|---|---|
| ASUS ASUSTek COMPUTER INC. | Title : L1_I219V (Connector) | Engineer: IPC-EE3 | |
| Size: Custom | Project Name: SMS-H410 | | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 45 of 87 | | |

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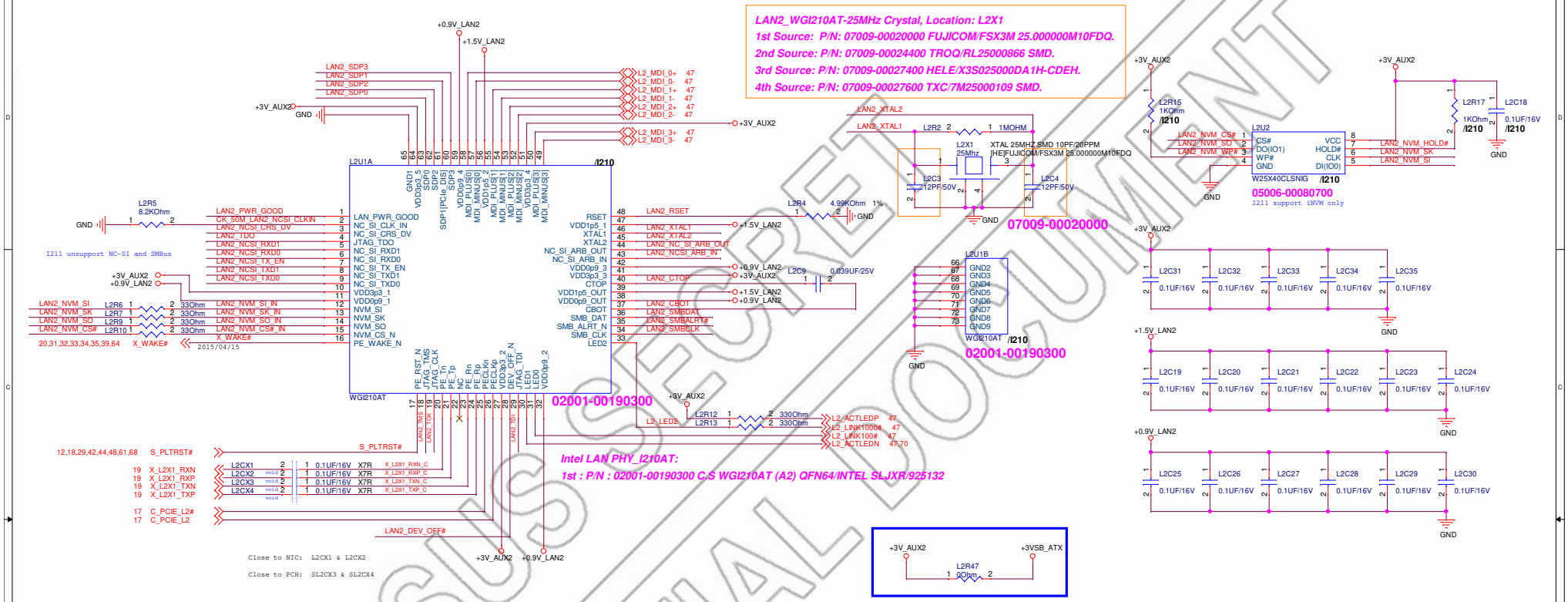
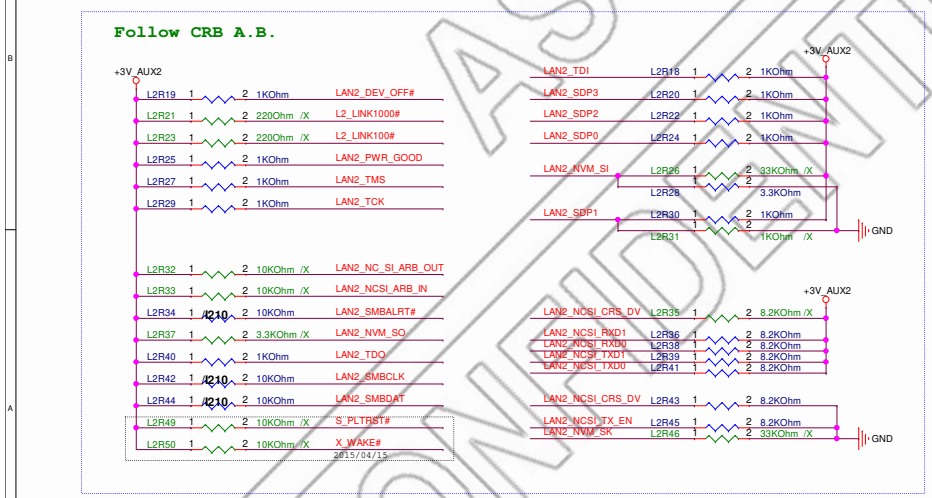
CONFIDENTIAL DOCUMENT



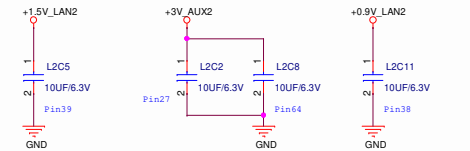

## Strapping Options

```
DEV_OFF_N
 I210.28 (DEV_OFF_N)
   1: Exit Device off mode (Default)
   0: Enter Device off mode

AUX_PWR
 I210.28 (DEV_OFF_N)
 I210.60 (SDP3)
   11: Enable AUX power mode (Default)

Security_EN
 I210.12 (NVM_SI)
   1: Enable Flash security
   0: Disable Flash security (Default)

PCIE_DIS_N
 I210.61 (SDP1[PCIe_DIS])
   1: Enable PCIe function (Default)
   0: Disable PCIe function
```



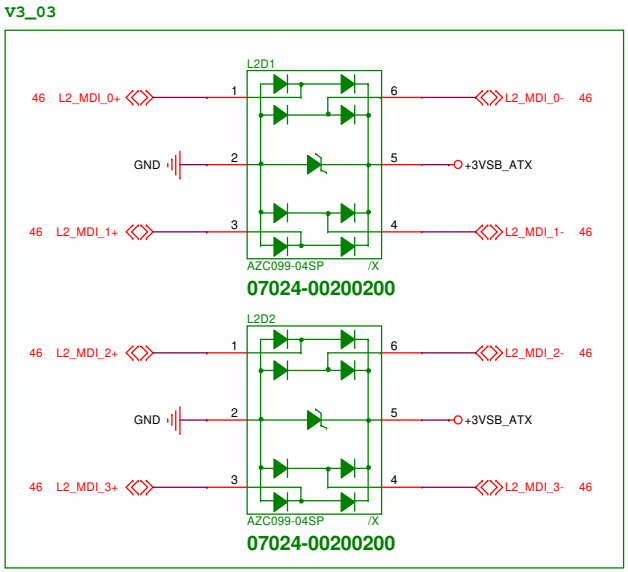

## 3.4 Voltage Regulator

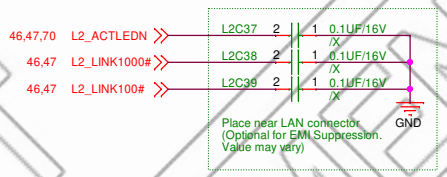
To reduce Bill of Material (BOM) cost, the I211 supports generating the 1.5V and 0.9V power supplies from the 3.3V supply using an on-chip Switching Capacitor Voltage Regulator (SVR) control circuit, which requires only an external capacitor component.

Refer to Section 10.6.4 for more details.

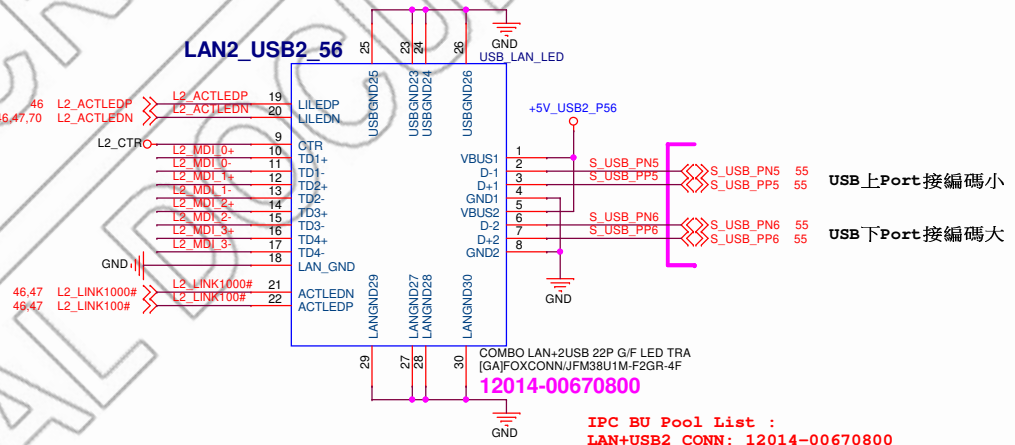
| | | | |
|---|---|---|---|
| ASUS | Title : LAN2_I210-AT_Port12 | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size: Custom | Project Name: SMS-H410 | | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 46 of 87 | | |

ASUS SECRET
CONFIDENTIAL DOCUMENT

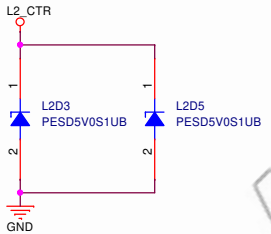


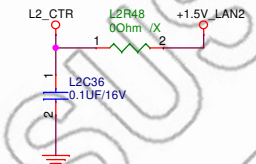



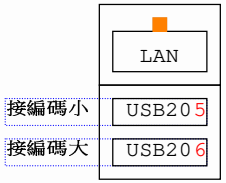

## USB20_Port5,6




IPC BU Pool List :
LAN+USB2 CONN: 12014-00670800
LAN+USB3 CONN: 12014-00660100




*LAN2_USB2_56*
*1st Source: P/N:12014-00670800 FOXCONN/JFM38U1M-F2GR-4F.*
*2nd Source: P/N:12014-00061700 SPEEDTECH/RUA1JB-4VD1-DC0-0R.*

| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : LAN2_RJ45 | |
| | Engineer: IPC-EE3 | |
| Size: Custom | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 47 of 87 | |

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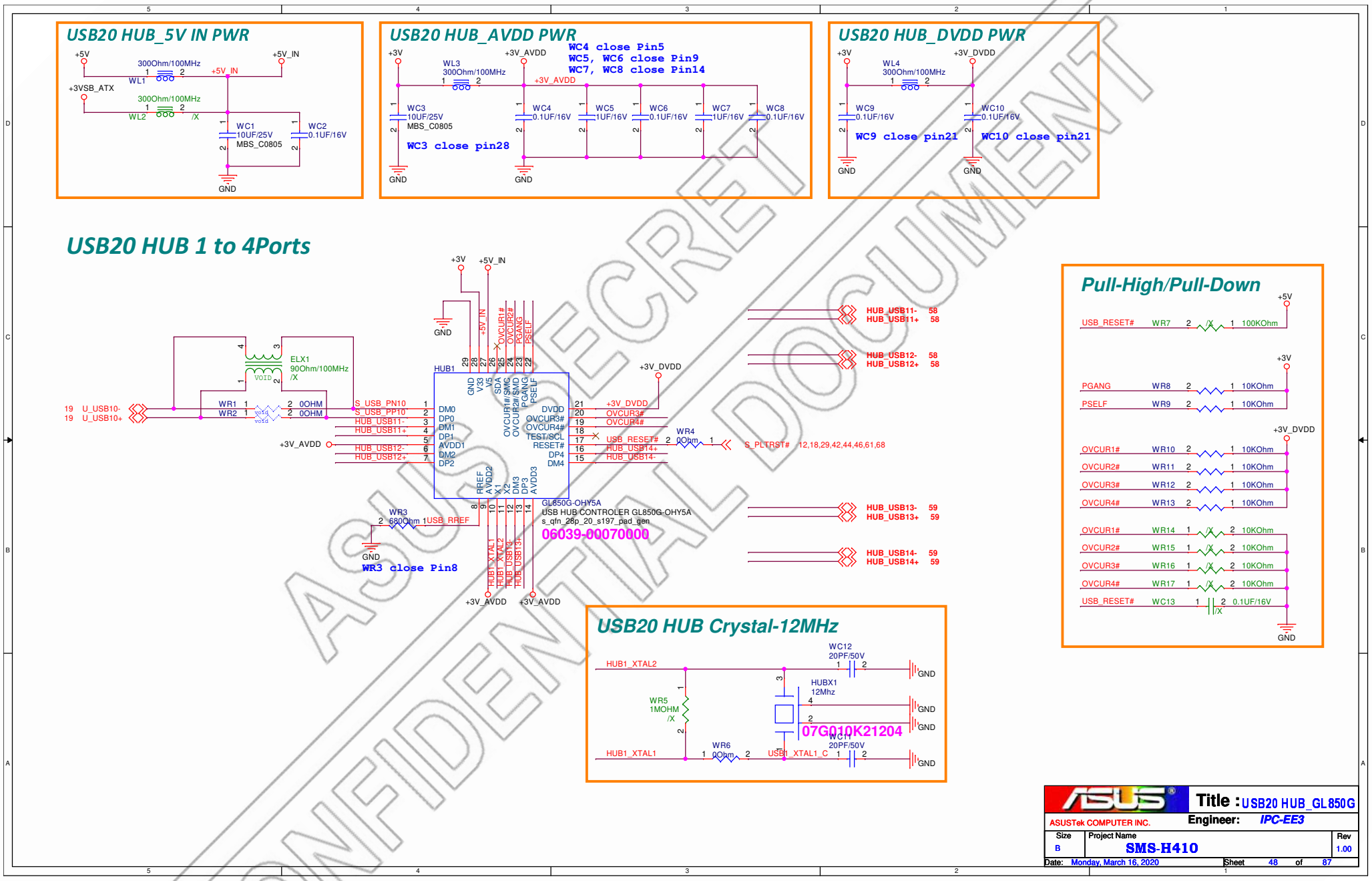
USB20 HUB_5V IN PWR
+5V
300Ohm/100MHz
WL1
+5V_IN
+3VSB_ATX
WL2
/X
WC1
10UF/25V
MBS_C0805
WC2
0.1UF/16V
GND
USB20 HUB_AVDD PWR
+3V
WL3
300Ohm/100MHz
+3V_AVDD
WC4 close Pin5
WC5, WC6 close Pin9
WC7, WC8 close Pin14
WC3
10UF/25V
MBS_C0805
WC3 close pin28
WC4
0.1UF/16V
WC5
1UF/16V
WC6
0.1UF/16V
WC7
1UF/16V
WC8
0.1UF/16V
USB20 HUB_DVDD PWR
+3V_DVDD
WL4
300Ohm/100MHz
WC9
0.1UF/16V
WC9 close pin21
WC10
0.1UF/16V
WC10 close pin21
USB20 HUB 1 to 4Ports
ELX1
90Ohm/100MHz
/X
VOID
WR1
WR2
0OHM
U_USB10-
U_USB10+
S_USB_PN10
S_USB_PP10
HUB_USB11-
HUB_USB11+
HUB_USB12-
HUB_USB12+
HUB1
DM0
DP0
DM1
DP1
AVDD1
DM2
DP2
DVDD
OVCUR3#
OVCUR4#
TEST/SCL
RESET#
DP4
DM4
RREF
AVDD2
X1
X2
DM3
DP3
AVDD3
HUB1_XTAL1
HUB1_XTAL2
HUB_USB13-
HUB_USB13+
WR3
680Ohm
USB_RREF
WR3 close Pin8
GL850G-OHY5A
USB HUB CONTROLER GL850G-OHY5A
s_qfn_28p_20_s197_pad_gen
06039-00070000
HUB_USB11-
HUB_USB11+
HUB_USB12-
HUB_USB12+
HUB_USB13-
HUB_USB13+
HUB_USB14-
HUB_USB14+
WR4
0Ohm
S_PLTRST#
12,18,29,42,44,46,61,68
Pull-High/Pull-Down
USB_RESET#
WR7
100KOhm
PGANG
WR8
10KOhm
PSELF
WR9
OVCUR1#
WR10
OVCUR2#
WR11
OVCUR3#
WR12
OVCUR4#
WR13
WR14
WR15
WR16
WR17
WC13
0.1UF/16V
USB20 HUB Crystal-12MHz
WC12
20PF/50V
HUB1_XTAL2
WR5
1MOHM
/X
HUBX1
12Mhz
07G010K21204
WC11
20PF/50V
WR6
0Ohm
HUB1_XTAL1
USB1_XTAL1_C
ASUS
Title : USB20 HUB_GL850G
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size B
Project Name SMS-H410
Rev 1.00
Date: Monday, March 16, 2020
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ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : XXXXX | |
| | Engineer: IPC-EE3 | |
| Size: C | Project Name: SMS-H4 10 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 49 of 87 | |

ASUS SECRET
CONFIDENTIAL DOCUMENT

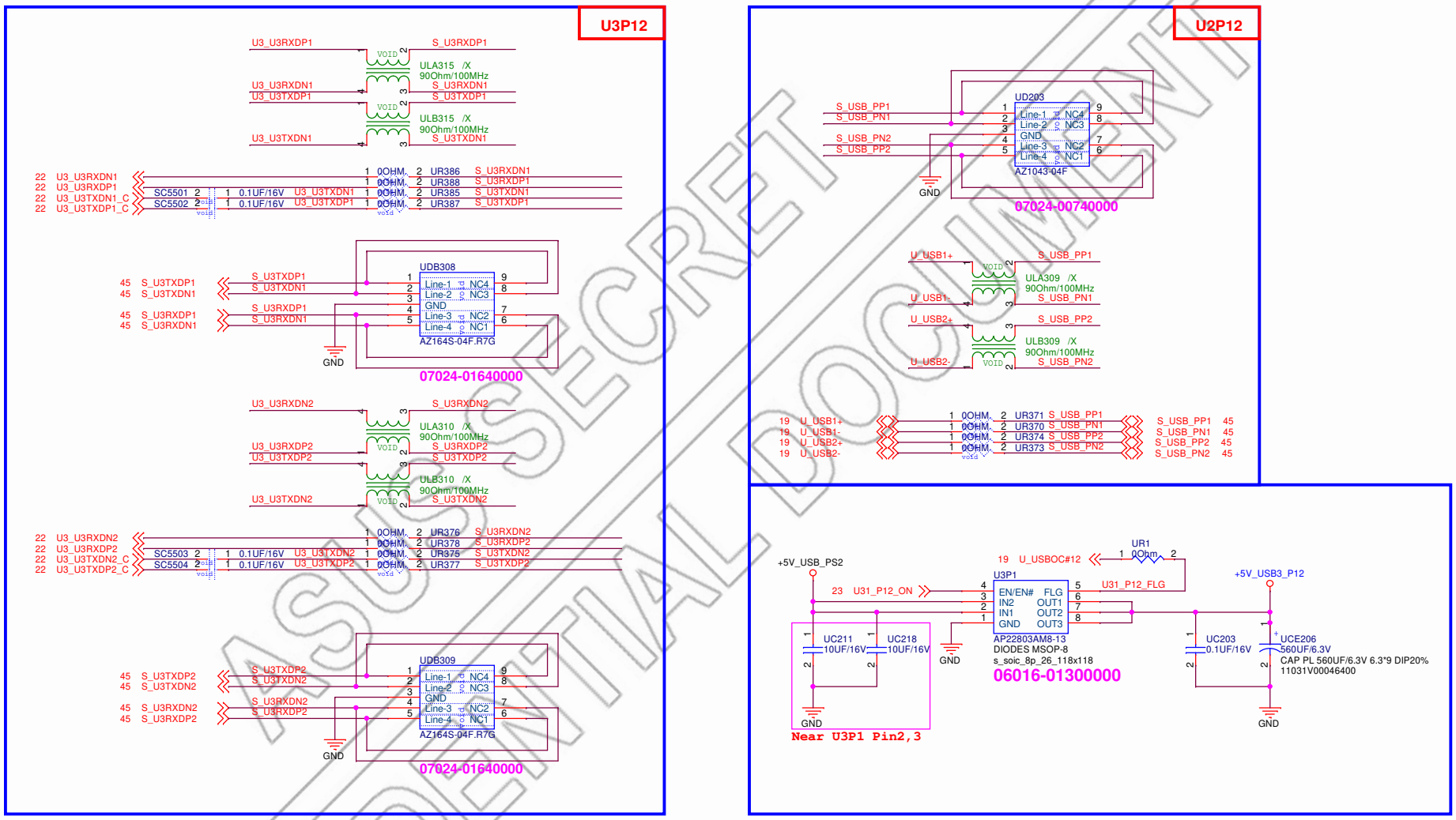
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : XXXXX | |
| | Engineer: IPC-EE3 | |
| Size: C | Project Name: SMS-H4 10 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 50 of 87 | |

ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : XXXXX | |
| | Engineer: IPC-EE3 | |
| Size: C | Project Name: SMS-H4 10 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 51 of 87 | |

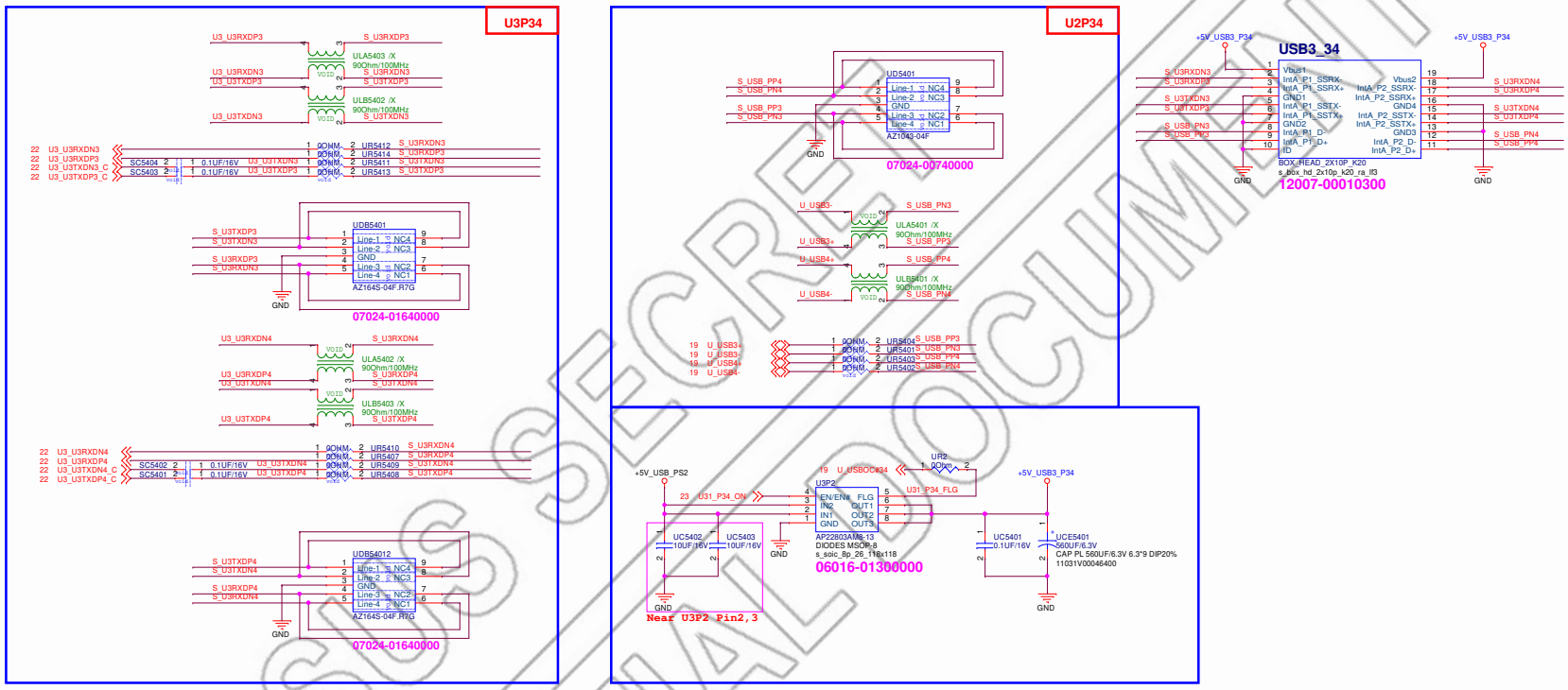
ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : xxxxx | |
| | Engineer: IPC-EE3 | |
| Size: C | Project Name: SMS-H4 10 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 52 of 87 | |




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : USB30 Port 1,2 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 53 of 87 | |

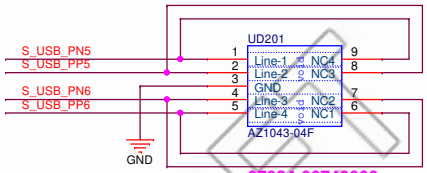



CONFIDENTIAL DOCUMENT
ASUS SECRET

| | | |
|---|---|---|
| ASUS | Title : USB3 Port 3,4_Header | |
| ASUSTeK COMPUTER INC. | Engineer: IPC-EE3 | |
| Size: C | Project Name: SMS-H4 10 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 54 of 87 | |

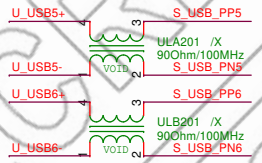
# LAN2-I211_USB20 Port

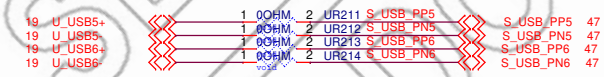
U2P56

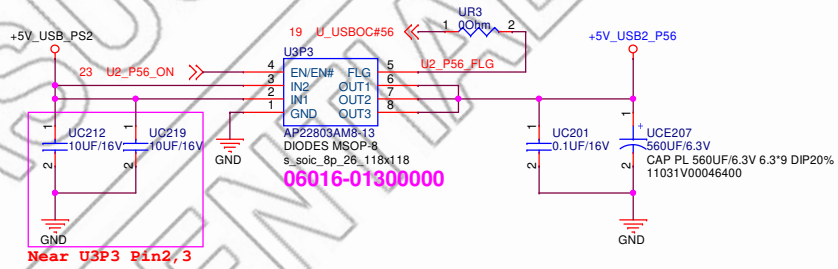



07024-00740000

2013/10/04



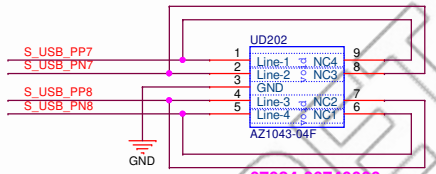




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : USB20 Port5,6_LAN2-I211 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 55 of 87 | |

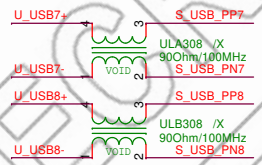
# USB20 Type-A X2 Ports

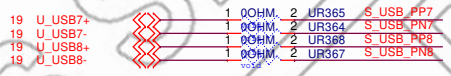
U2P78

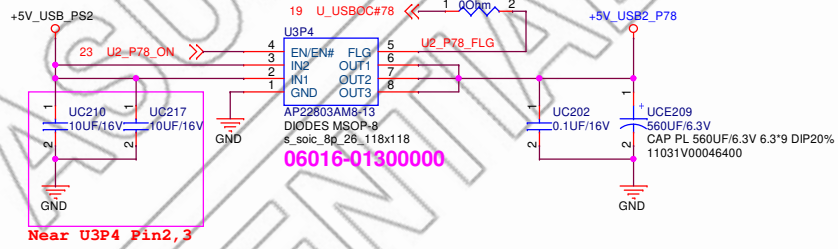


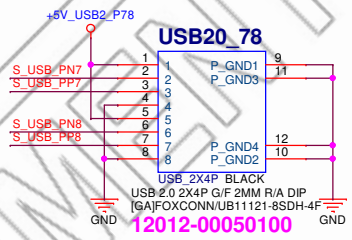

07024-00740000

2013/10/04



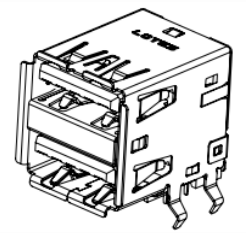

12012-00050100

*USB20_78 :*

*1st : P/N : 12012-00050100 FOXCONN/UB11121-8SDH-4F*

*2nd : P/N : 12012-00050800 LINGYANG/UB2022W-B001-20DAS0B*

| | |
|---|---|
| 接編碼小 | USB207 |
| 接編碼大 | USB208 |



ASUS SECRET
CONFIDENTIAL DOCUMENT

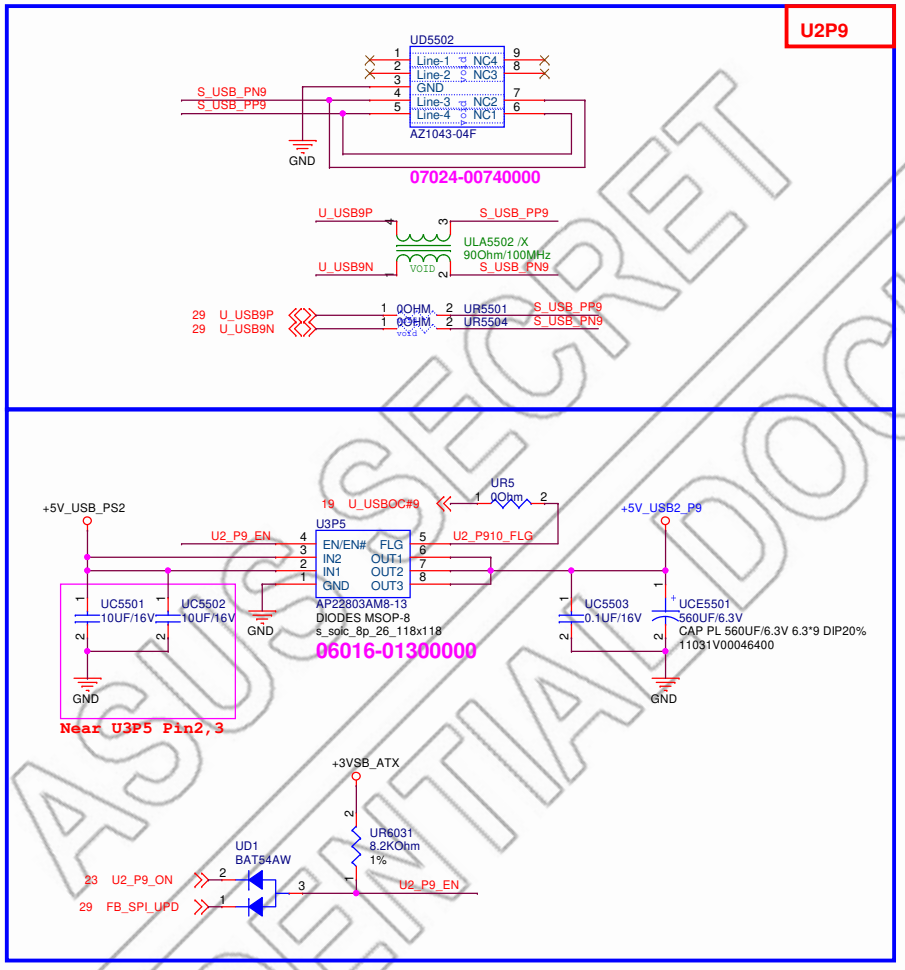
ASUSTek COMPUTER INC.

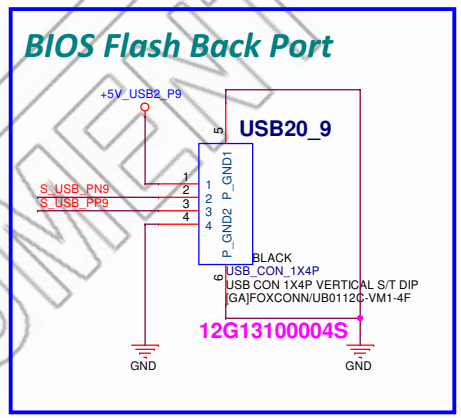
Title : USB20 Type-A X2 Ports

Engineer: *IPC-EE3*

| Size | Project Name | Rev |
|---|---|---|
| B | SMS-H410 | 1.00 |

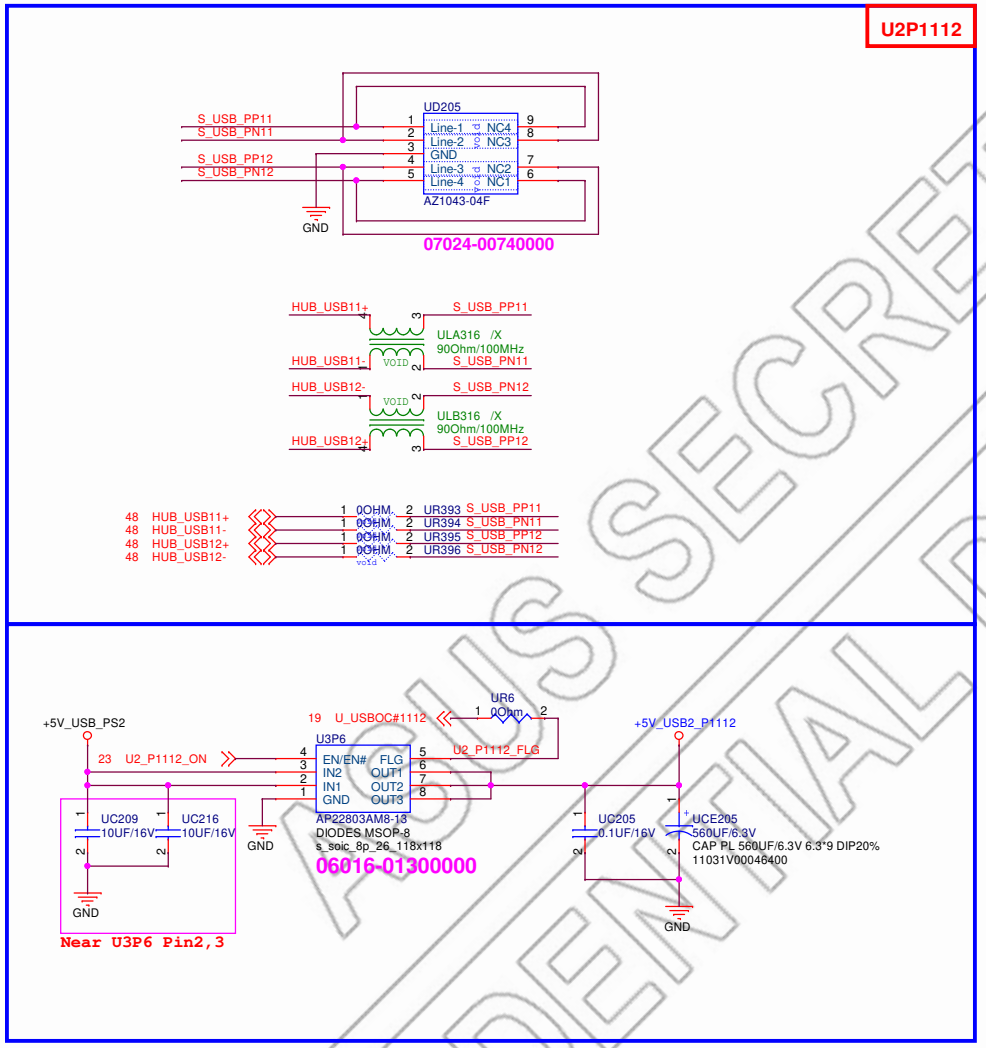
Date: Monday, March 16, 2020 Sheet 56 of 87



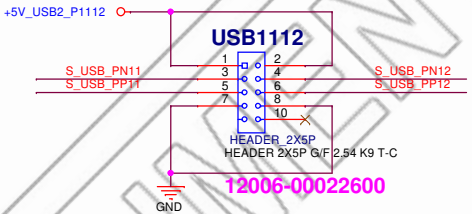




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : USB20 Port 9 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 57 of 87 | |




## USB20 Header Port11,12



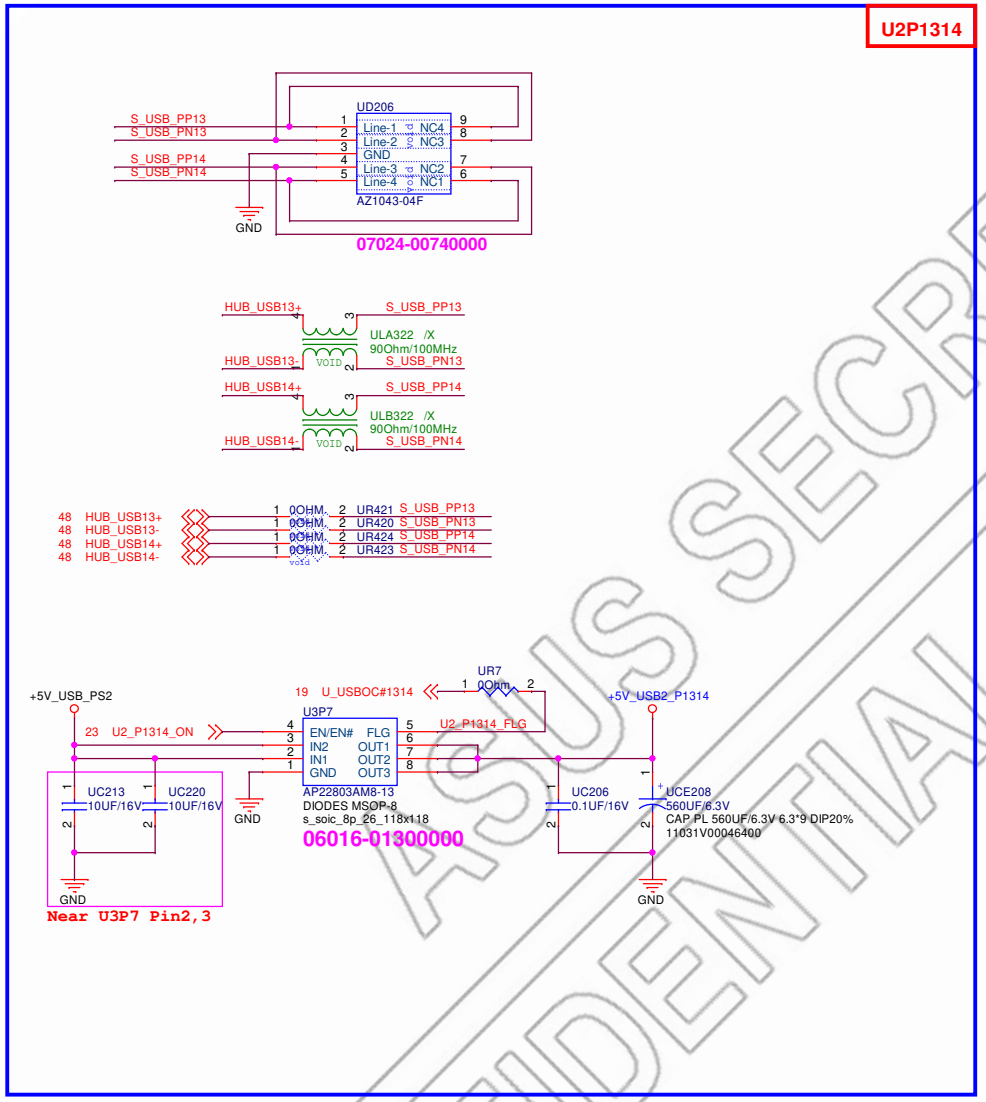

*HEADER 2X5P G/F 2.54 K9 T-C_Group : 12006V00022300*

*1st Source: P/N: 12006-00022600 LINGYANG/PH2541U-D055-09A3K9P.*

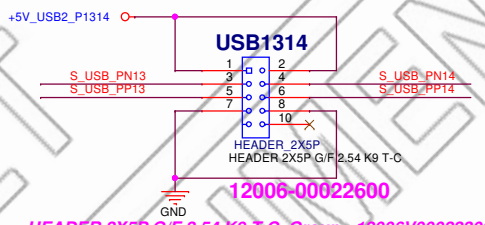
*2nd Source: P/N: 12006-00022300 PINREX/210-82-05GF24.*

ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : USB2 Header Port11,12 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size: B | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 58 of 87 | |




## USB20 Header Port13,14



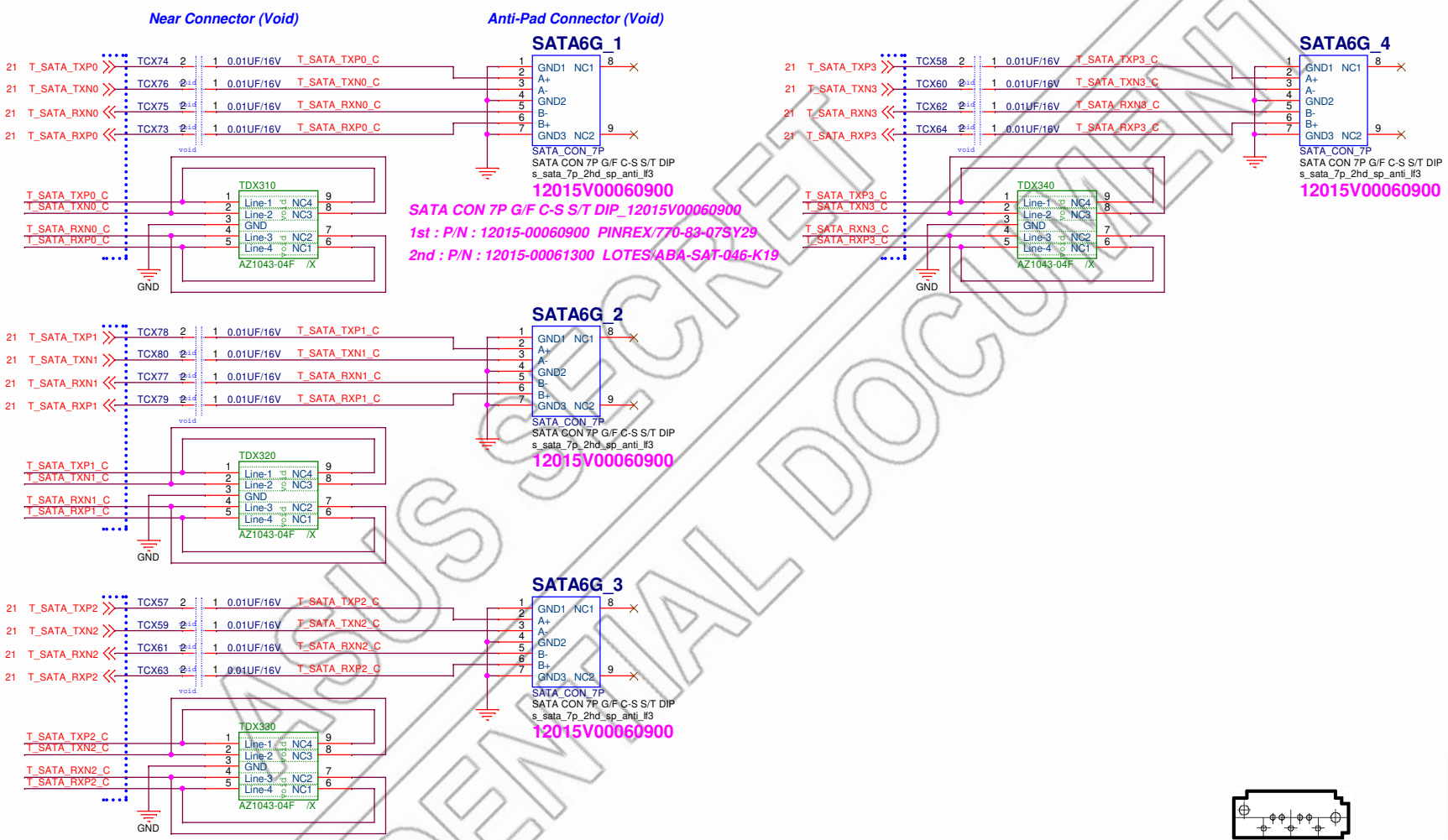

*HEADER 2X5P G/F 2.54 K9 T-C_Group : 12006V00022300*

*1st Source: P/N: 12006-00022600 LINGYANG/PH2541U-D055-09A3K9P.*

*2nd Source: P/N: 12006-00022300 PINREX/210-82-05GF24.*

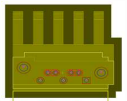
ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : USB2 Header Port13,14 | Engineer: IPC-EE3 |
| Size: B | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 59 of 87 | |






顏色：Turkish-Coffee
It connects with chipset.
(Full function are supported)




| New Color | | |
|---|---|---|
| SATA 6G: | 12015V00060900 | Cornsilk |
| SATA 3G: | 12015V00060800 | Turkish-Coffee |

| Old Color | | |
|---|---|---|
| SATA 6G: | 12V702200A00 | LIGHT GRAY |
| SATA 3G: | 12V702200L00 | LIGHT BLUE |

ASUSTek COMPUTER INC.

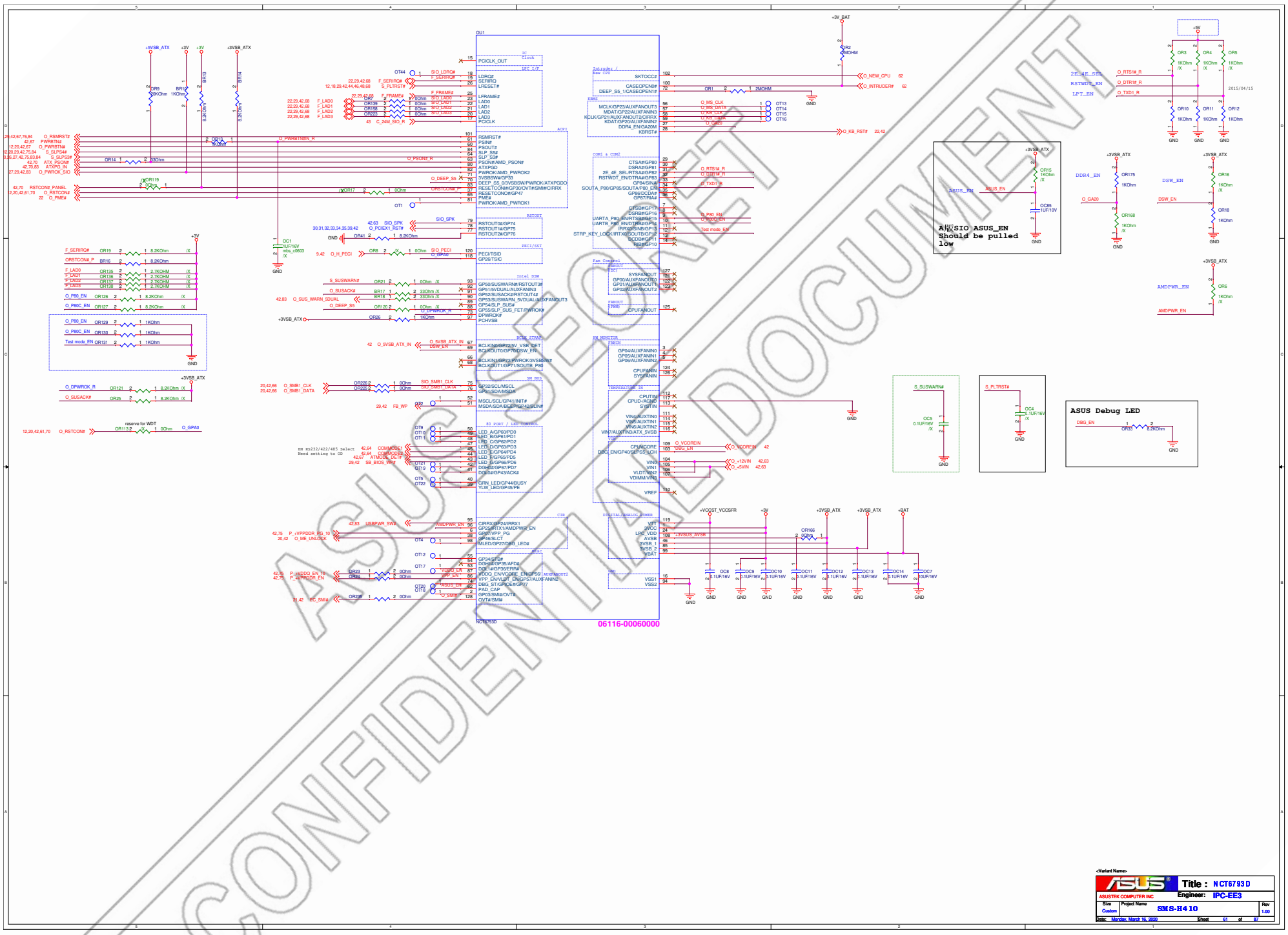
Title : SATA6G_12345(CHIPSET)

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| B | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 60 of 87

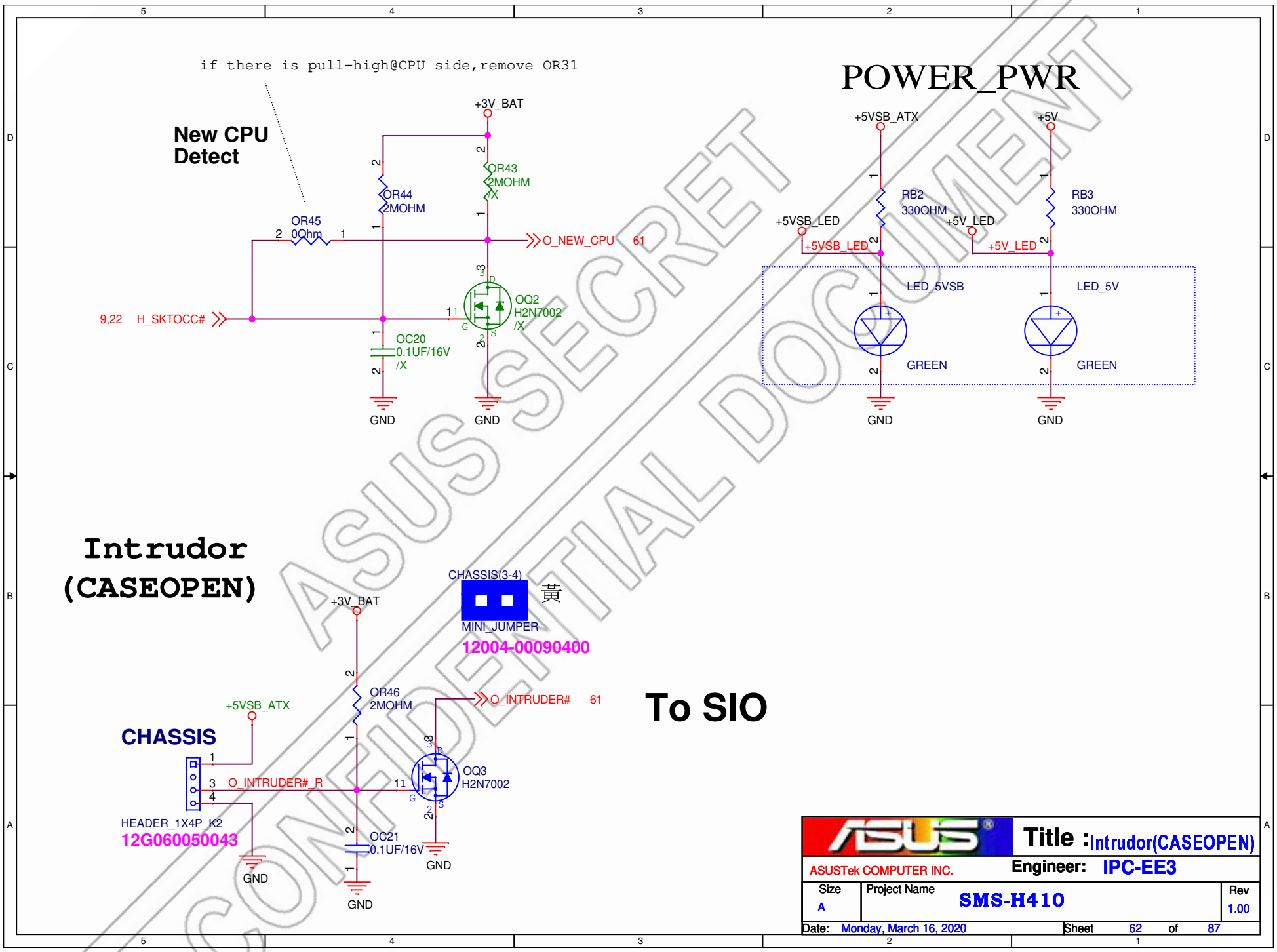
ASUS SECRET
CONFIDENTIAL DOCUMENT

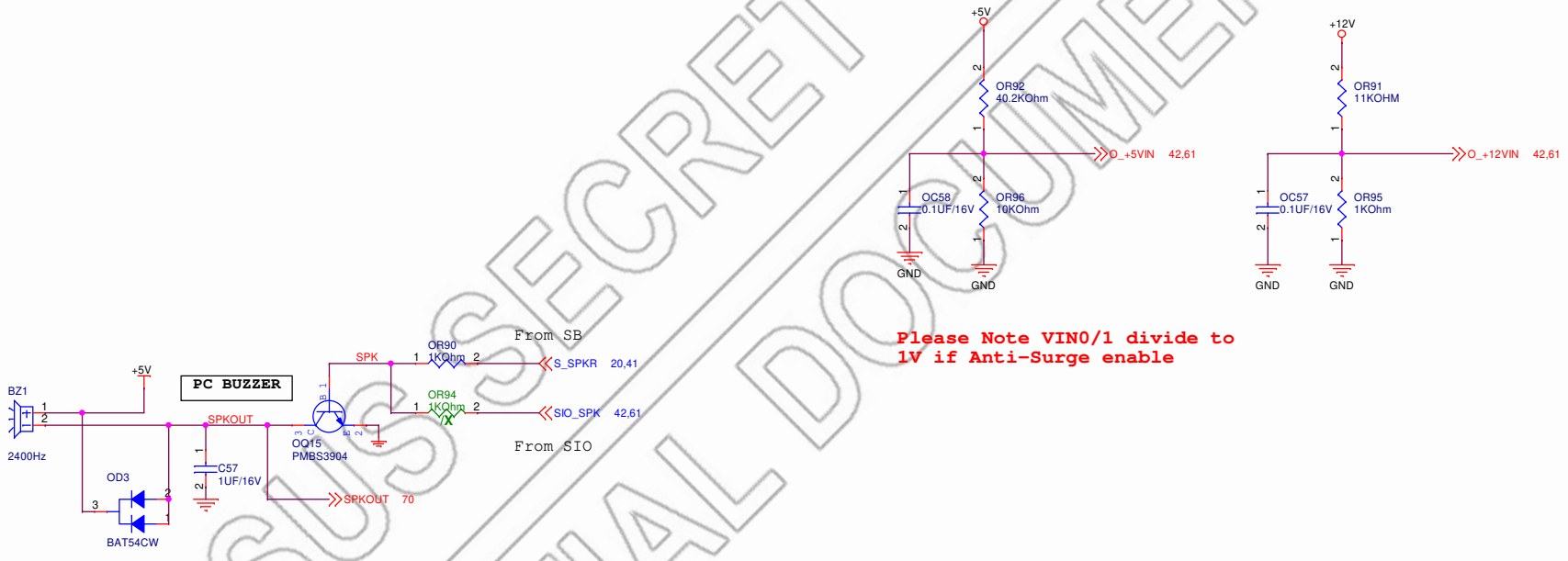



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

| | | |
|---|---|---|
| ASUS | Title : | NCT6793D |
| ASUSTEK COMPUTER INC | Engineer: | IPC-EE3 |
| Size: Custom | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 61 of 87 | |


if there is pull-high@CPU side,remove OR31
New CPU Detect
+3V_BAT
OR43
2MOHM
/X
OR44
2MOHM
OR45
0Ohm
O_NEW_CPU
61
9,22
H_SKTOCC#
OQ2
H2N7002
/X
OC20
0.1UF/16V
/X
GND
GND
POWER_PWR
+5VSB_ATX
+5V
RB2
330OHM
RB3
330OHM
+5VSB_LED
+5V_LED
LED_5VSB
LED_5V
GREEN
GREEN
GND
GND
Intrudor
(CASEOPEN)
CHASSIS(3-4)
黃
MINI_JUMPER
12004-00090400
+3V_BAT
OR46
2MOHM
O_INTRUDER#
61
To SIO
+5VSB_ATX
CHASSIS
O_INTRUDER#_R
OQ3
H2N7002
HEADER_1X4P_K2
12G060050043
OC21
0.1UF/16V
GND
GND
GND
ASUS SECRET
CONFIDENTIAL DOCUMENT
Title : Intrudor(CASEOPEN)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size
A
Project Name
SMS-H410
Rev
1.00
Date: Monday, March 16, 2020
Sheet 62 of 87

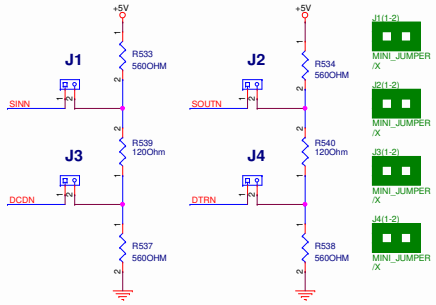



**Please Note VIN0/1 divide to 1V if Anti-Surge enable**

ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : HW MONITOR | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 63 of 87 | |

## RS422/RS485 Terminator

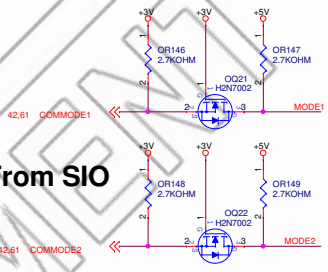



J1,J2,J3,J4 all off -->RS232
J1,J2,J3,J4 all on -->RS485/RS422 with terminator

| Mode Selection | | | |
|---|---|---|---|
| SD | MODE_1 | MODE_2 | MODE |
| 0 | 0 | 0 | RS-422 |
| 0 | 0 | 1 | RS-232 |
| 0 | 1 | 0 | RS-485 (Driver Half Duplex) |
| 0 | 1 | 1 | RS-485 (Receiver Half Duplex) |
| 1 | X | X | Shutdown MODE |

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ.
As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.



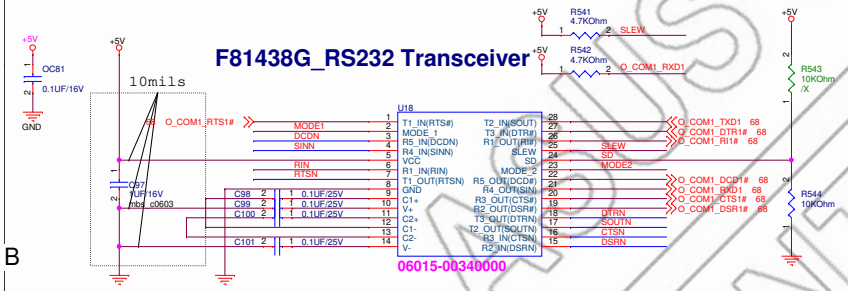

(VDD = +5.0V ± 5% )

| Parameter | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Supply Current (RS-232) | No Load, MODE = 01. | | 2 | 30 | mA |
| Supply Current (RS-485) | No Load, MODE = 10, 11. | | 2 | | mA |
| Supply Current (RS-422) | MODE = 00. | | 2 | | mA |
| Operating Temperature * | Symbol: T | -40 | | 85 | ◦ C |

(VDD = +5.0V ± 5% )

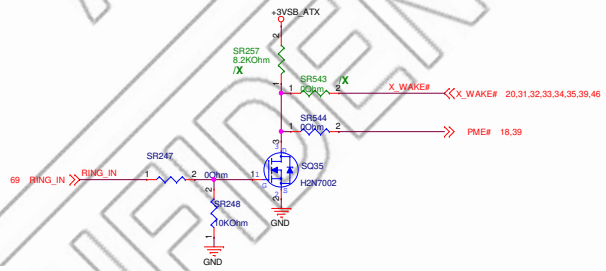
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28 | | | | | | |
| Logic Input Voltage HIGH | $V_{IL}$ | 2.4 | | | V | VDD = 5.0 V |
| Logic Input Voltage LOW | - | | | 0.8 | V | |
| Logic Input Pull-up Current | - | | | ±15 | μA | |
| Driver Input Pull High Current | $I_{IT}$ | | | ±15 | μA | |

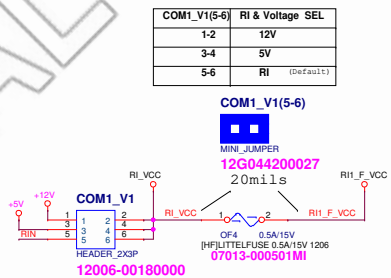
## F81438G_RS232 Transceiver



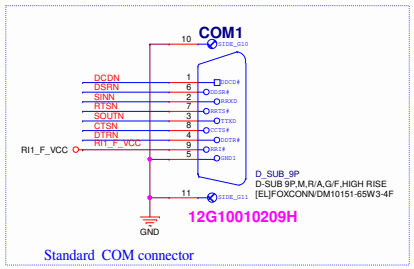






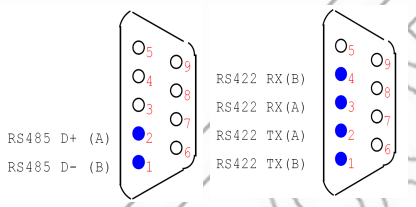




| COM1_V1(5-6) | RI & Voltage SEL |
|---|---|
| 1-2 | 12V |
| 3-4 | 5V |
| 5-6 | RI (Default) |

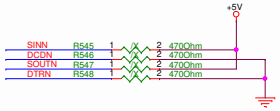



Standard COM connector

Close to COM port connector



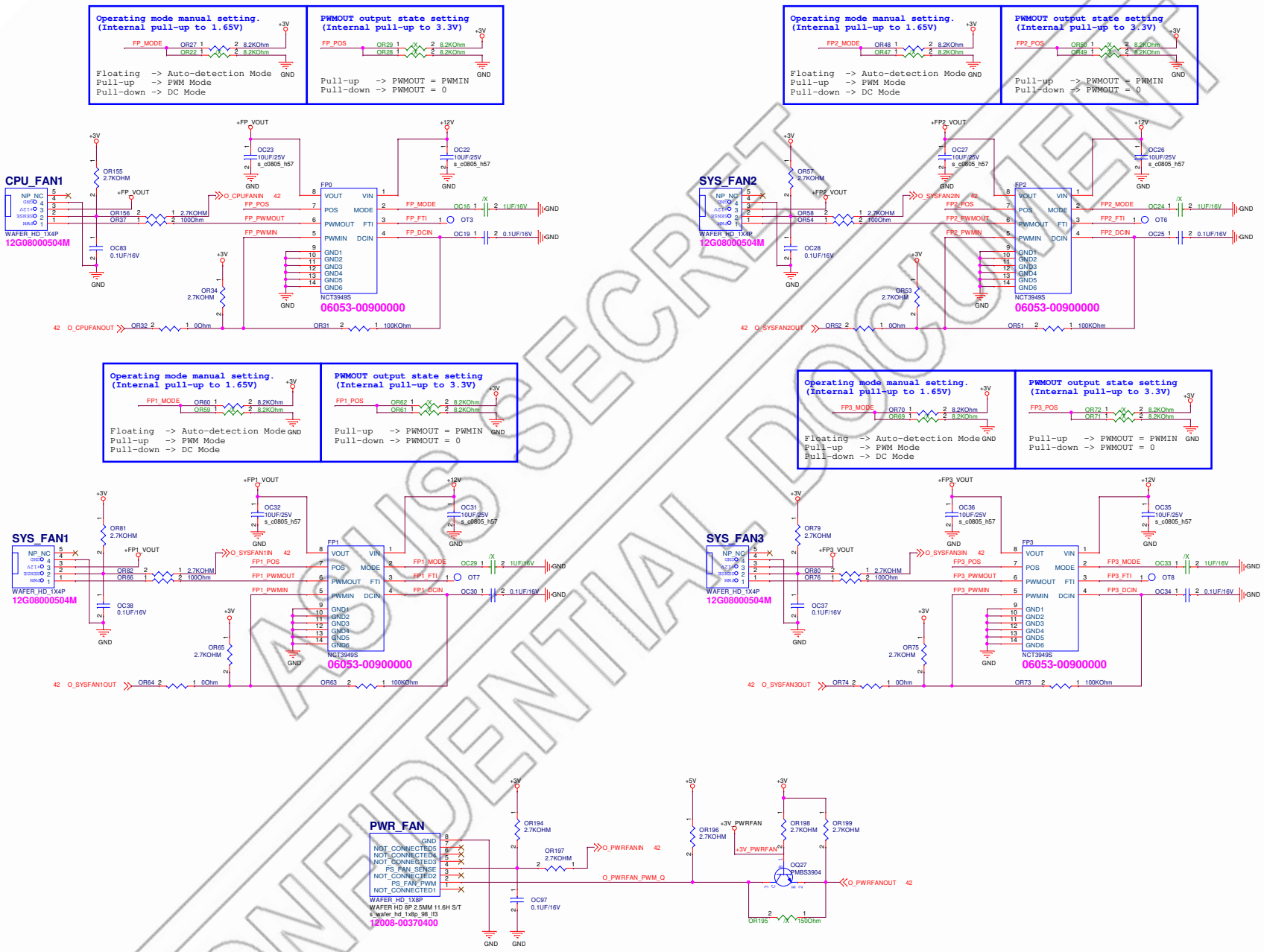

| Maximum Slew rate control | | |
|---|---|---|
| SLEW | RS-232 | RS-485/RS-422 |
| 0 | 1Mbps | 10Mbps |
| 1 | 250Kbps | 250Kbps |




Note:Reserved for FAIL-SAVE

| | |
|---|---|
| ASUS | Title : COM1_RS232/422/485 |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 |
| Size: Custom | Project Name: SMS-H410 |
| Rev: 1.00 | |
| Date: Monday, March 16, 2020 | Sheet 64 of 87 |

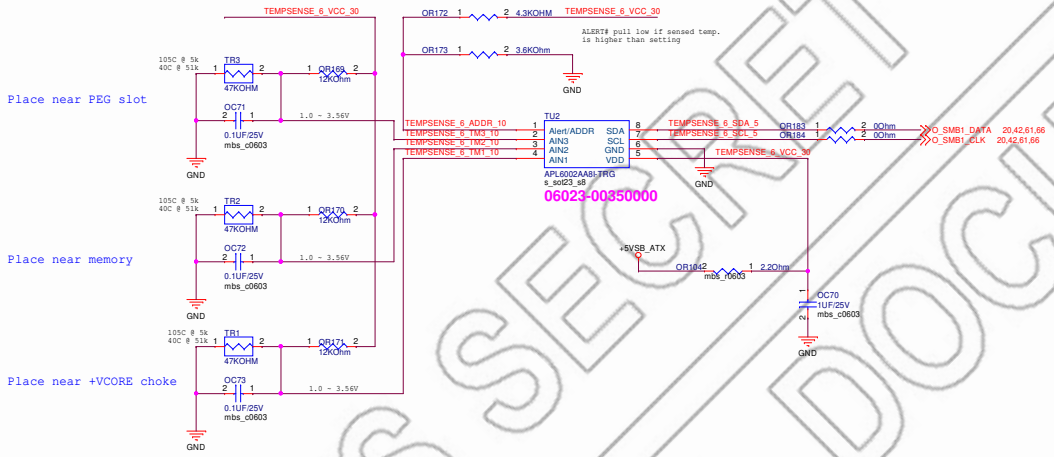
ASUS SECRET CONFIDENTIAL DOCUMENT


Operating mode manual setting. (Internal pull-up to 1.65V)
Floating -> Auto-detection Mode
Pull-up -> PWM Mode
Pull-down -> DC Mode
PWMOUT output state setting (Internal pull-up to 3.3V)
Pull-up -> PWMOUT = PWMIN
Pull-down -> PWMOUT = 0
CPU_FAN1
12G08000504M
WAFER_HD_1X4P
FP0
NCT3949S
06053-00900000
SYS_FAN2
FP2
SYS_FAN1
FP1
SYS_FAN3
FP3
PWR_FAN
WAFER_HD_1X8P
WAFER HD 8P 2.5MM 11.6H S/T
12008-00370400
ASUS SECRET
CONFIDENTIAL DOCUMENT
Title : CPU/SYS/PWR_FAN
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name SMS-H410
Rev 1.00
Date: Monday, March 16, 2020
Sheet 65 of 87

## For EC

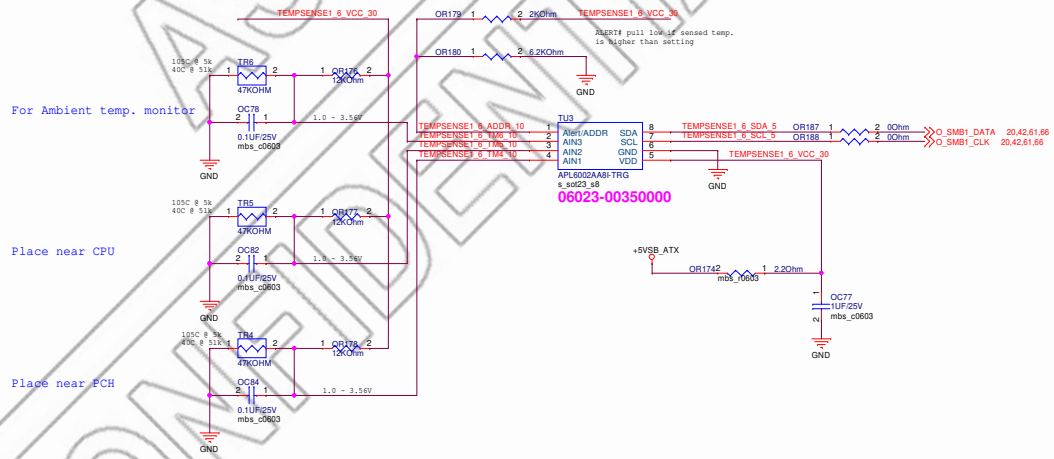
### Address Selection Table

| Address | 0x7E | 0x7C | 0x7A | 0x78 | 0x76 | 0x74 | 0x72 | 0x70 |
|---|---|---|---|---|---|---|---|---|
| OR172 | 10k | 1.5k | 2k | 3.6k | 3.9k | 4.3k | 5.1k | 6k |
| OR173 | Open | 8.2k | 6.2k | 6.8k | 4.7k | 3.6k | 2.7k | 2k |




### Address Selection Table

| Address | 0x7E | 0x7C | 0x7A | 0x78 | 0x76 | 0x74 | 0x72 | 0x70 |
|---|---|---|---|---|---|---|---|---|
| OR179 | 10k | 1.5k | 2k | 3.6k | 3.9k | 4.3k | 5.1k | 6k |
| OR180 | Open | 8.2k | 6.2k | 6.8k | 4.7k | 3.6k | 2.7k | 2k |




ASUS SECRET
CONFIDENTIAL DOCUMENT

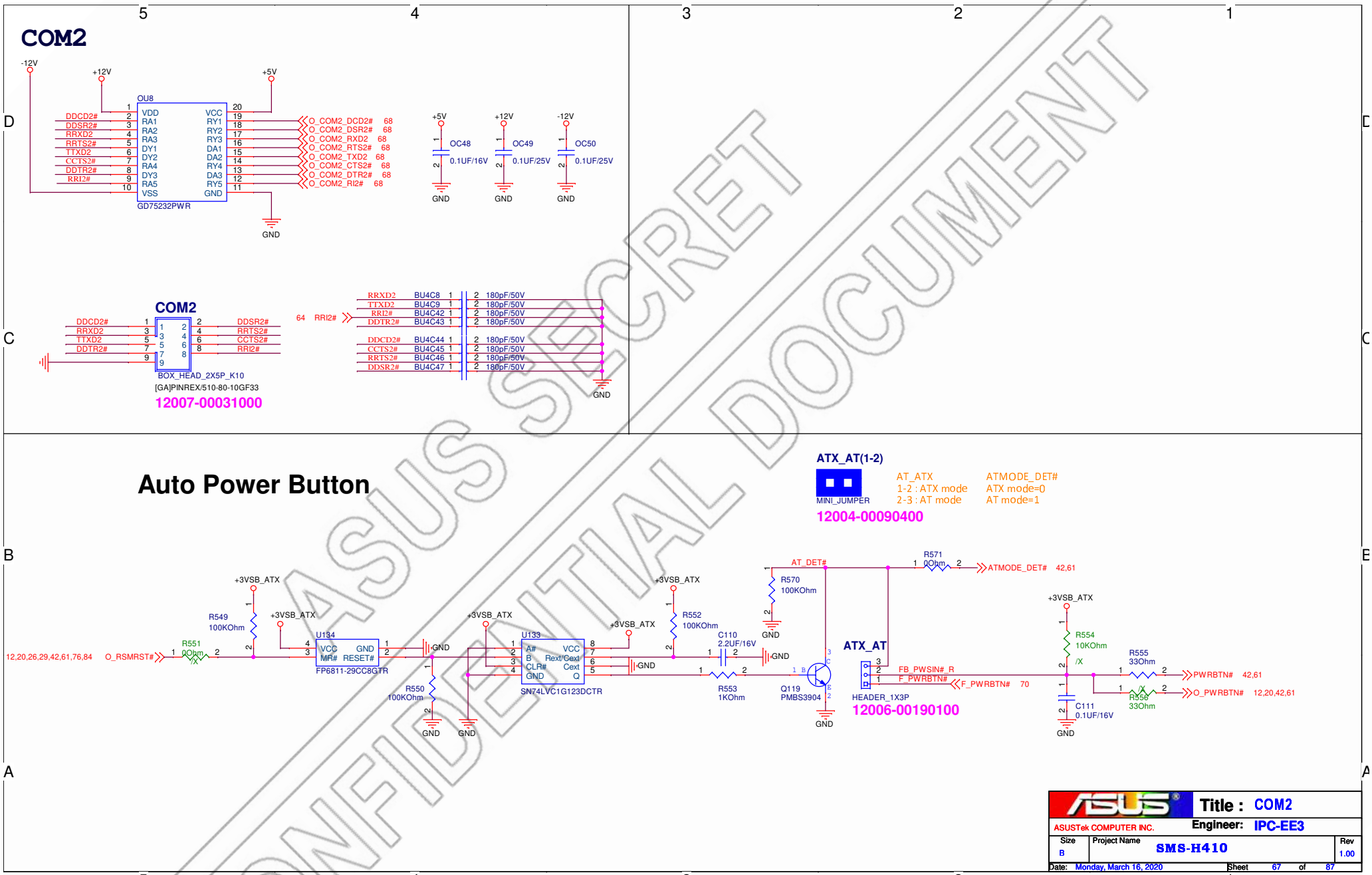
ASUSTEK COMPUTER INC

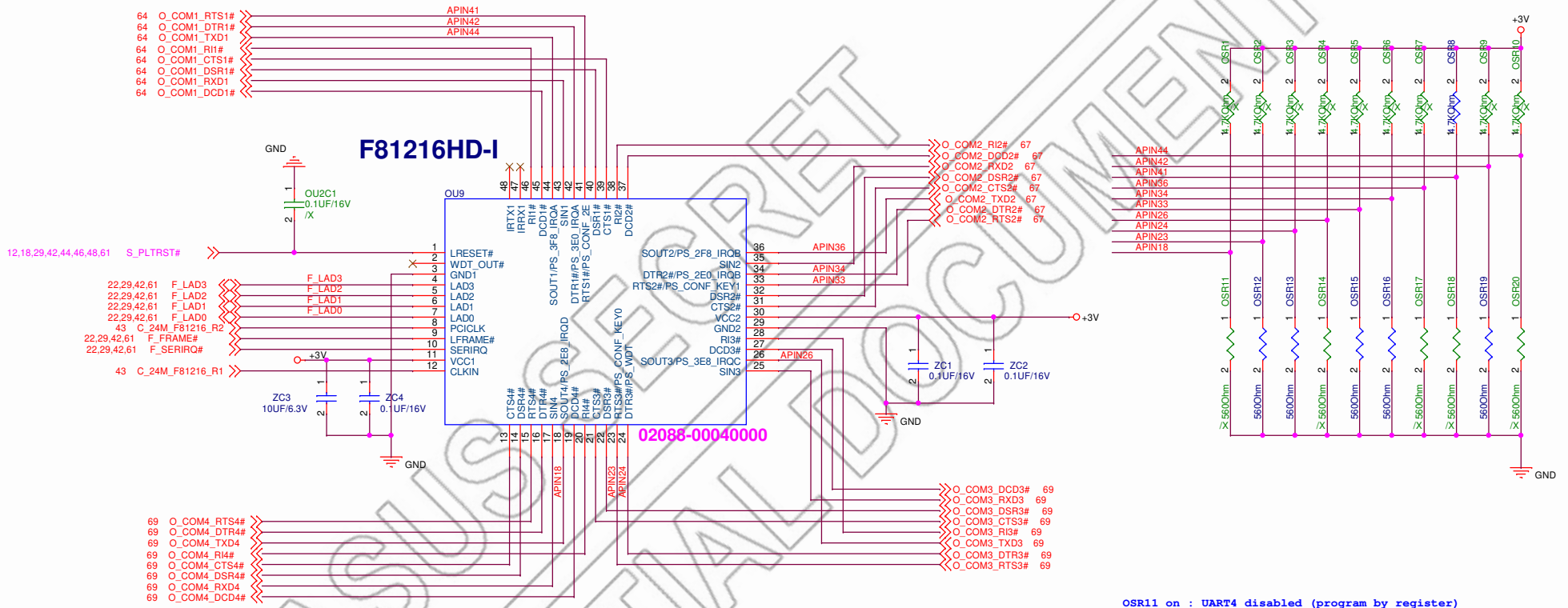
Title : Thermal Sensor

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| C | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 66 of 87


COM2
-12V
+12V
+5V
OU8
VDD
RA1
RA2
RA3
DY1
DY2
RA4
DY3
RA5
VSS
VCC
RY1
RY2
RY3
DA1
DA2
RY4
DA3
RY5
GND
GD75232PWR
DDCD2#
DDSR2#
RRXD2
RRTS2#
TTXD2
CCTS2#
DDTR2#
RRI2#
O_COM2_DCD2# 68
O_COM2_DSR2# 68
O_COM2_RXD2 68
O_COM2_RTS2# 68
O_COM2_TXD2 68
O_COM2_CTS2# 68
O_COM2_DTR2# 68
O_COM2_RI2# 68
OC48
0.1UF/16V
OC49
0.1UF/25V
OC50
0.1UF/25V
GND
COM2
BOX_HEAD_2X5P_K10
[GA]PINREX/510-80-10GF33
12007-00031000
64 RRI2#
BU4C8
BU4C9
BU4C42
BU4C43
BU4C44
BU4C45
BU4C46
BU4C47
180pF/50V
Auto Power Button
ATX_AT(1-2)
MINI_JUMPER
12004-00090400
AT_ATX
1-2 : ATX mode
2-3 : AT mode
ATMODE_DET#
ATX mode=0
AT mode=1
+3VSB_ATX
R549
100KOhm
R551
0Ohm
/X
12,20,26,29,42,61,76,84
O_RSMRST#
U134
VCC
GND
MR#
RESET#
FP6811-29CC8GTR
R550
100KOhm
U133
A#
B
CLR#
GND
VCC
Rext/Cext
Cext
Q
SN74LVC1G123DCTR
R552
100KOhm
C110
2.2UF/16V
R553
1KOhm
Q119
PMBS3904
AT_DET#
R570
100KOhm
R571
0Ohm
ATMODE_DET# 42,61
ATX_AT
HEADER_1X3P
12006-00190100
FB_PWSIN#_R
F_PWRBTN#
F_PWRBTN# 70
R554
10KOhm
C111
0.1UF/16V
R555
33Ohm
R556
33Ohm
PWRBTN# 42,61
O_PWRBTN# 12,20,42,61
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUSTek COMPUTER INC.
Title : COM2
Engineer: IPC-EE3
Size B
Project Name SMS-H410
Rev 1.00
Date: Monday, March 16, 2020
Sheet 67 of 87




| OSR15 | OSR12 | OSR18 | Address | Entry Key |
|---|---|---|---|---|
| 0 | 0 | 0 | 0x4e/0x4f | 0x77 |
| 0 | 0 | 1 | 0x2e/0x2f | 0x77 |
| 0 | 1 | 0 | 0x4e/0x4f | 0xa0 |
| 0 | 1 | 1 | 0x2e/0x2f | 0xa0 |
| 1 | 0 | 0 | 0x4e/0x4f | 0x87 |
| 1 | 0 | 1 | 0x2e/0x2f | 0x87 |
| 1 | 1 | 0 | 0x4e/0x4f | 0x87 |
| 1 | 1 | 1 | 0x2e/0x2f | 0x87 |

OSR11 on : UART4 disabled (program by register)
OSR11 off : UART 4 address : 0x2e8 IRQ9

OSR14 on : UART3 disabled (program by register)
OSR14 off : UART 3 address : 0x3e8 IRQ5

OSR16 on and OSR17 off : UART 2 address : 0x2f8 IRQ4
OSR16 off and OSR17 on : UART 2 address : 0x2e0 IRQ4;
OSR16 and OSR17 on :UART 2 disabled (program by register).

OSR19 on and OSR20 off : UART 1 address : 0x3f8 IRQ3;
OSR19 off and OSR20 on : UART 1 address : 0x3e0 IRQ3;
OSR19 and OSR20 on :UART 1 disabled (program by register).

OSR13 on : disabled
OSR13 off : Watch Dog Timer enabled and setting to 10 second when the clock input is 24Mhz. If the clock input is 48Mhz , the timer is setting to 5 second.

<Variant Name>

ASUSTEK COMPUTER INC

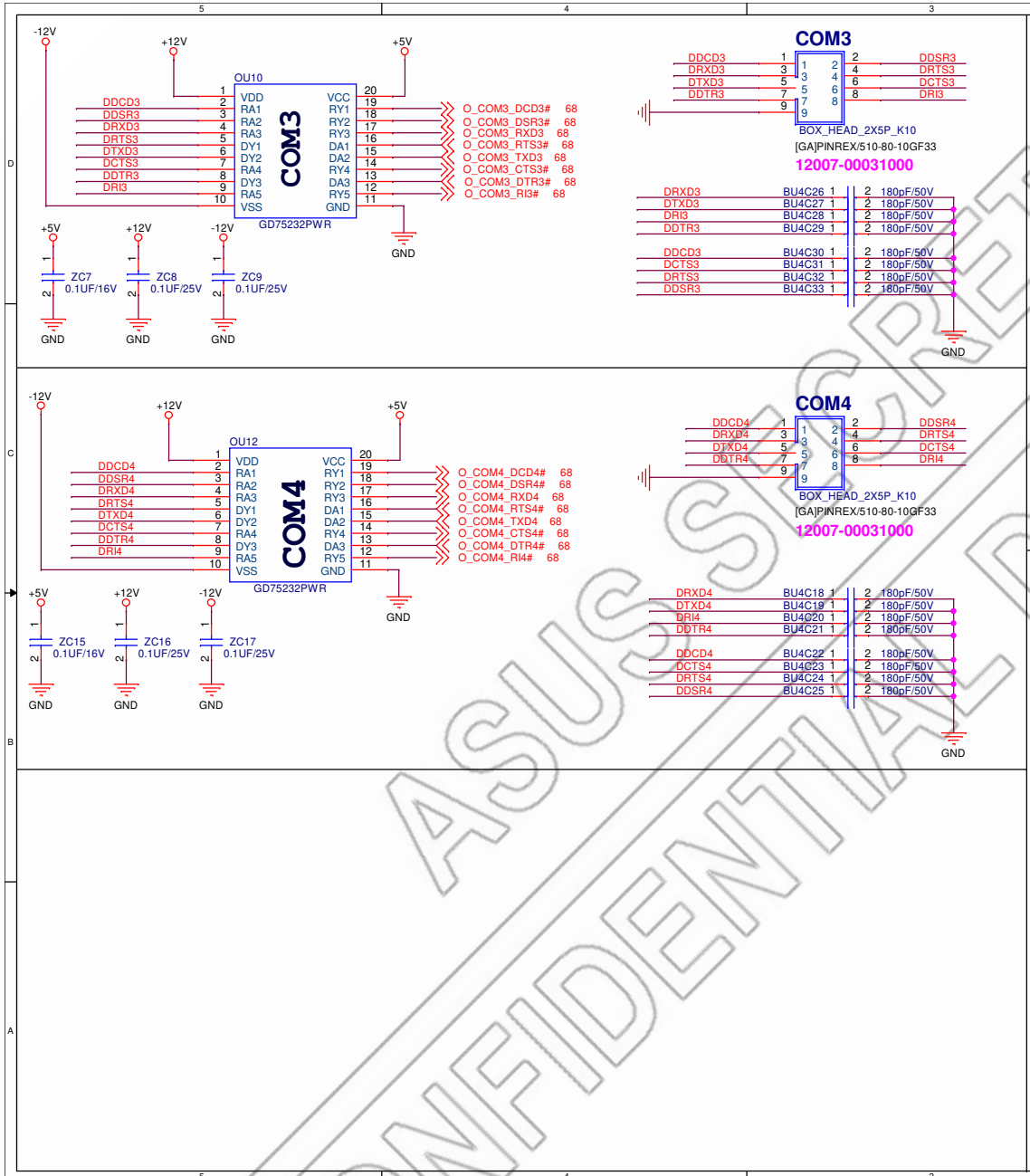
Title : F81216 COM

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| B | SMS-H410 | 1.00 |

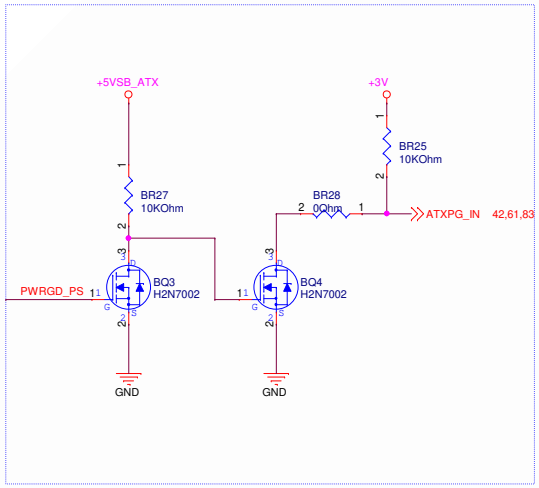
Date: Monday, March 16, 2020 Sheet 68 of 87

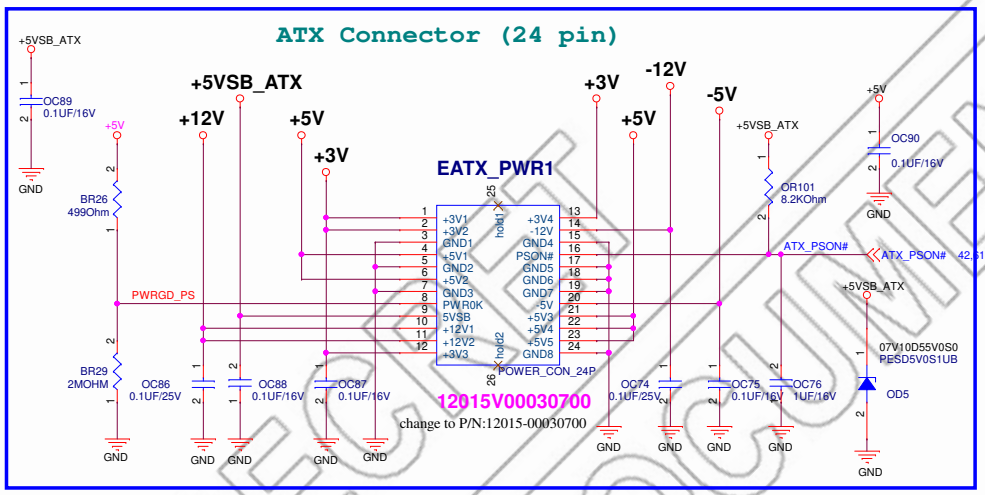
ASUS SECRET
CONFIDENTIAL DOCUMENT

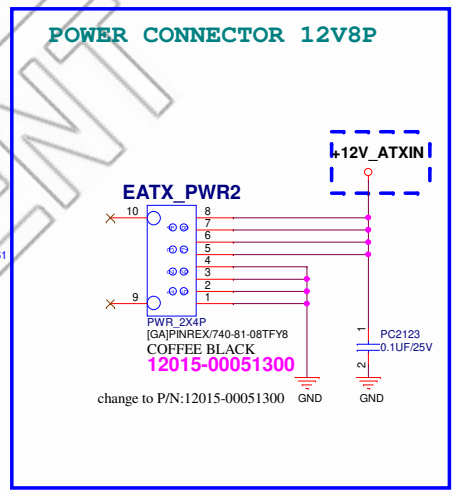


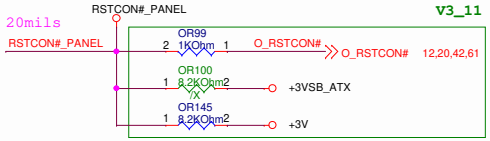

ASUS SECRET
CONFIDENTIAL DOCUMENT

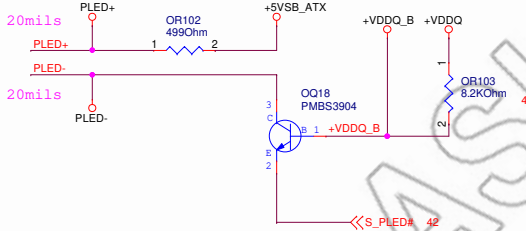
| | | |
|---|---|---|
| ASUSTEK COMPUTER INC | Title : COM3-4 | |
| | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 69 of 87 | |

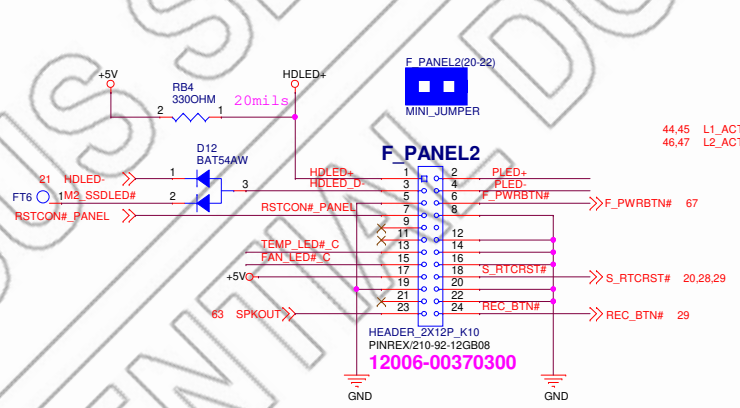


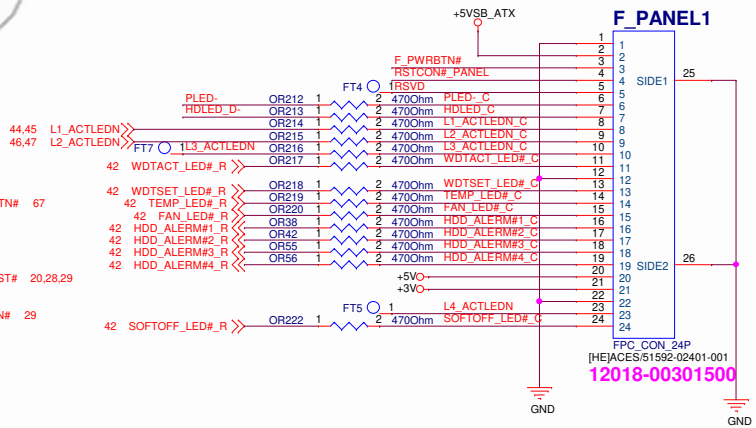



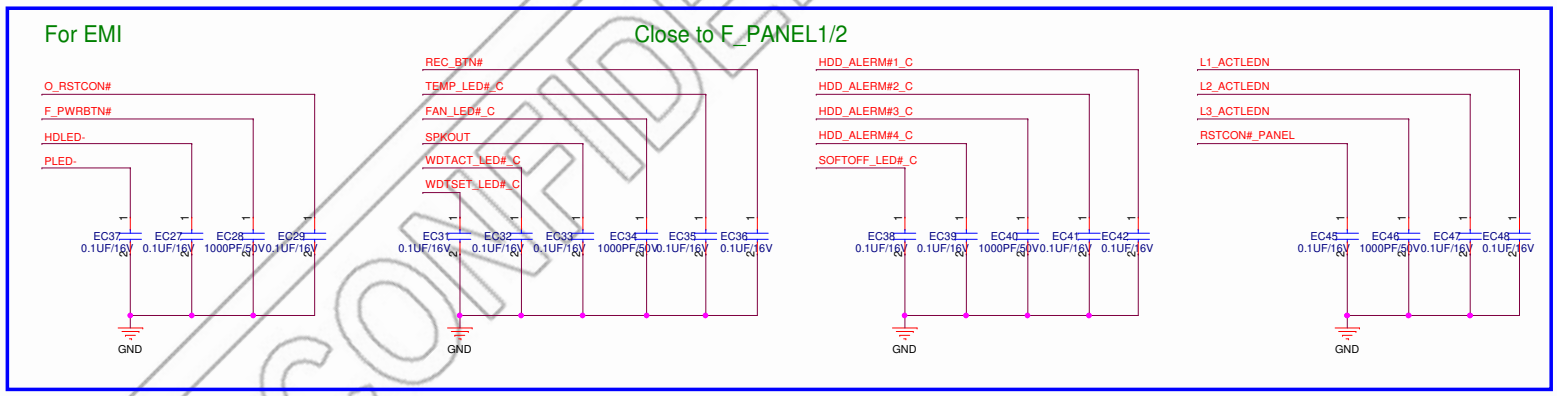



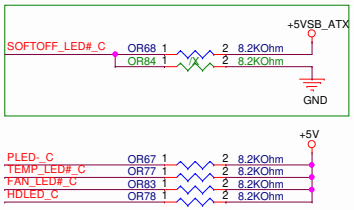



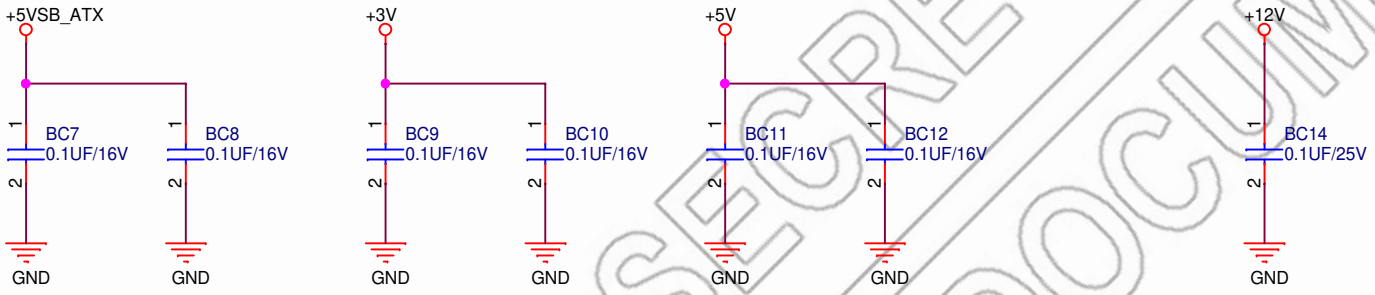



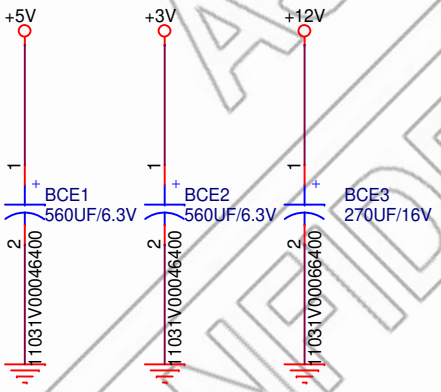

| | | | |
|---|---|---|---|
| ASUSTek COMPUTER INC. | Title : FRONT PANEL | | |
| | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 70 of 87 | | |

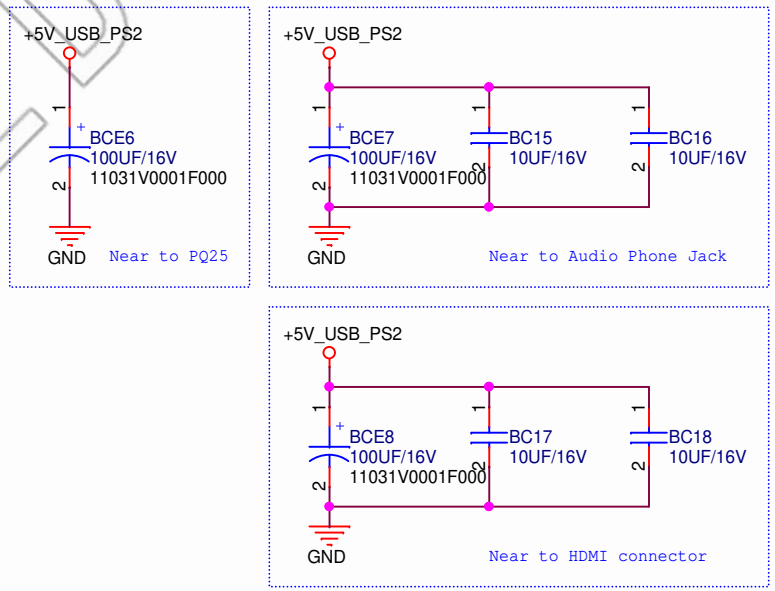
ASUS SECRET
CONFIDENTIAL DOCUMENT

# Bypass/EMI Capacitor




placemented on power source of 24pin.

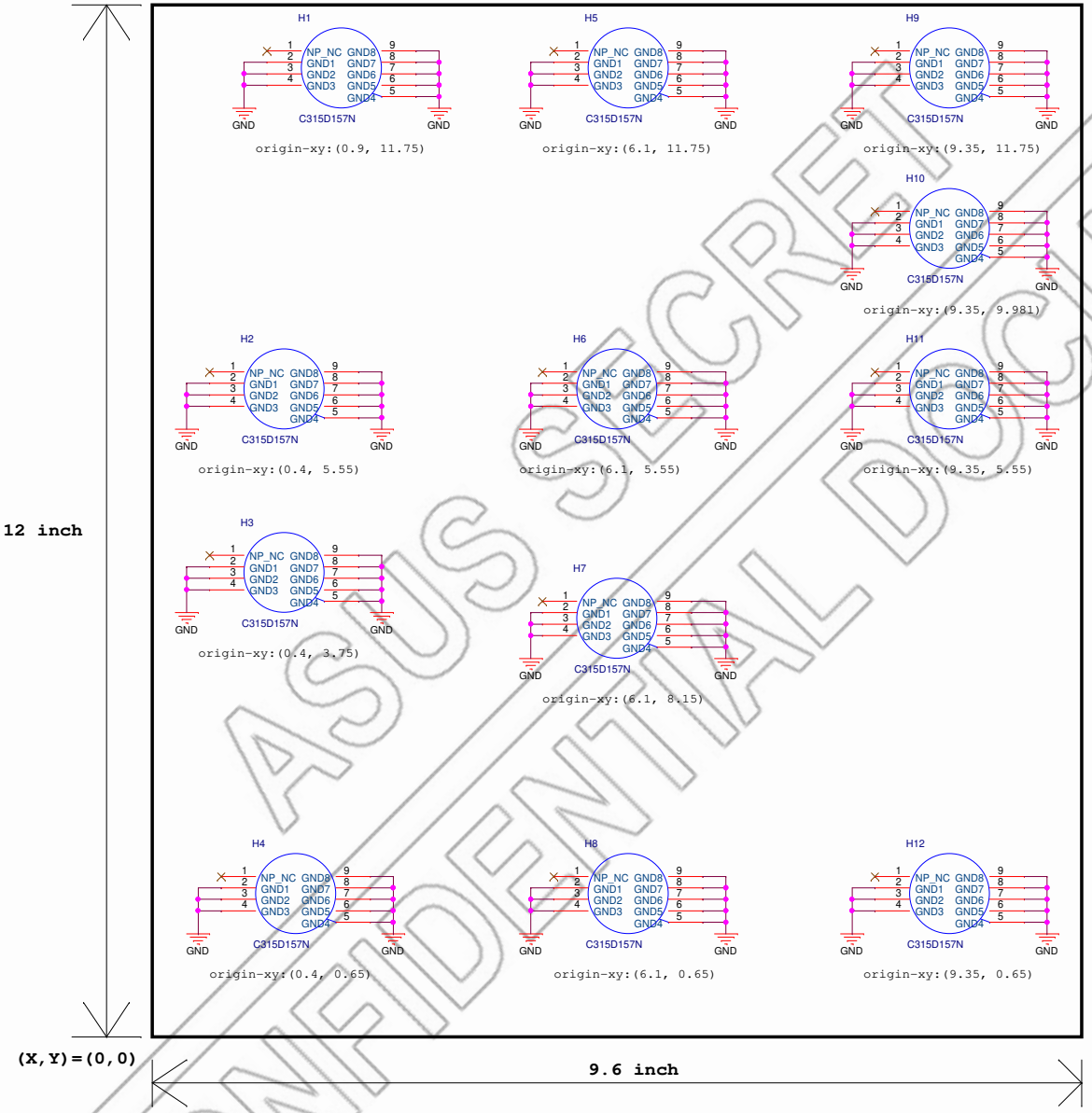



ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : EMI Cap | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size: A | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 71 of 87 | |

# ATX Screw Hole




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : Screw Hole | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size A3 | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 72 of 87 | |

# Selling Point

M3
SFIS_LABEL
SFIS_LABEL /X
temp_M01_000330

M2
SHORT_GND
Short_GND /X
temp_M05_0031

M1
SHORT_GND1
Short_GND1 /X
temp_M05_0029

DIMM_A1_STAR
ASTERISK /X
ASTERISK
temp_M01_000340

DIMM_B1_STAR
ASTERISK /X
ASTERISK
temp_M01_000340

*The U-DIMM Order of Insertion*

NEED_COMP_SILK
STANDARD CIRCUIT
NUMB OTHER
LOGO_HD_DEMO_OTHER /X

MODEL_LOGO
MODEL
MODEL_LOGO
temp_M01_0061
4mmx20mm 文字外框

PCB
PCB
SMS-H410
08001-15160X00

*SMS-H410 R1.00 PCB-08 :*

R1.00 PCB_ : 08001-15160000 DF 12*9.6,6L(1)1.6,1080
R1.00 PCB_ : 08001-15160100 TRUSTECH 12*9.6,6L(1)1.6,1080
R1.00 PCB_ : 08001-15160200 VICTORY 12*9.6,6L(1)1.6,1080

## Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

小顆十字光學點

INDEX31 INDEX_PLUS
INDEX32 INDEX_PLUS
INDEX33 INDEX_PLUS
INDEX34 INDEX_PLUS
INDEX35 INDEX_PLUS
INDEX36 INDEX_PLUS
INDEX37 INDEX_PLUS
INDEX38 INDEX_PLUS
INDEX39 INDEX_PLUS
INDEX40 INDEX_PLUS

2012/09/11

# Logo

*common Logo for all projects*

LOGO2
FCC
FCC /X
temp_M01_000348

LOGO5
WEEE_LOGO
WEEE_LOGO /X

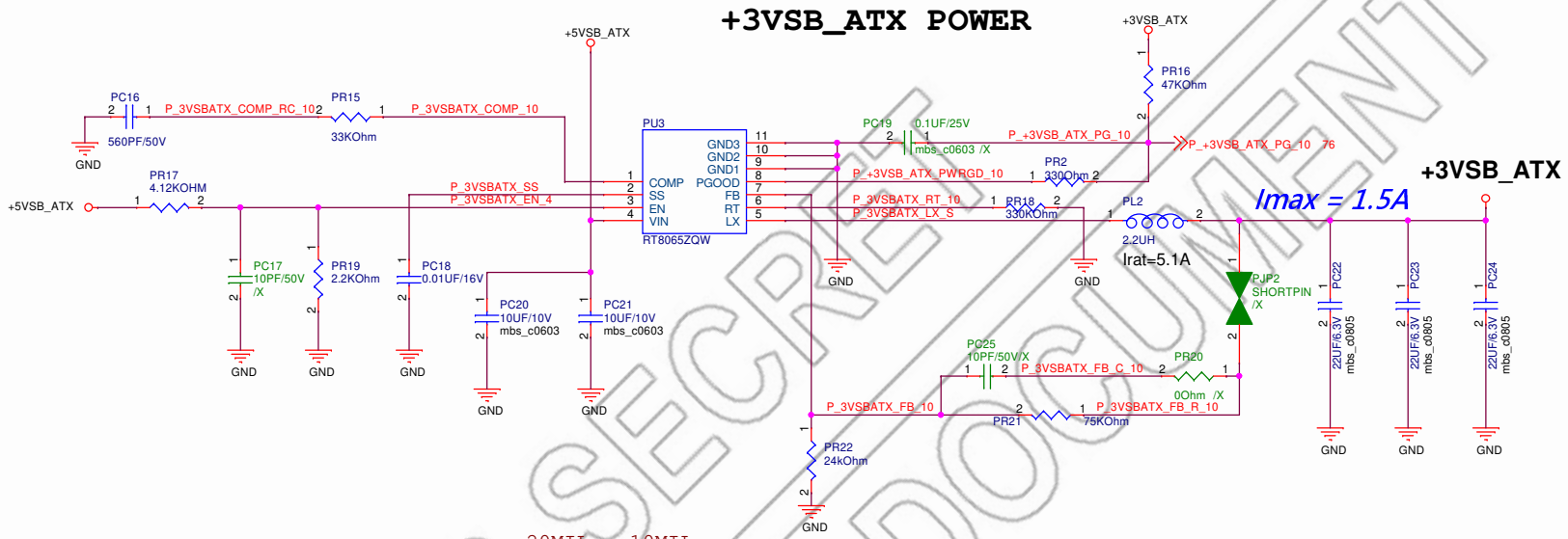
LOGO6
CE
CE /X

LOGO7
PCB MADE IN CHINA
PCB_MADE_IN_CHINA /X

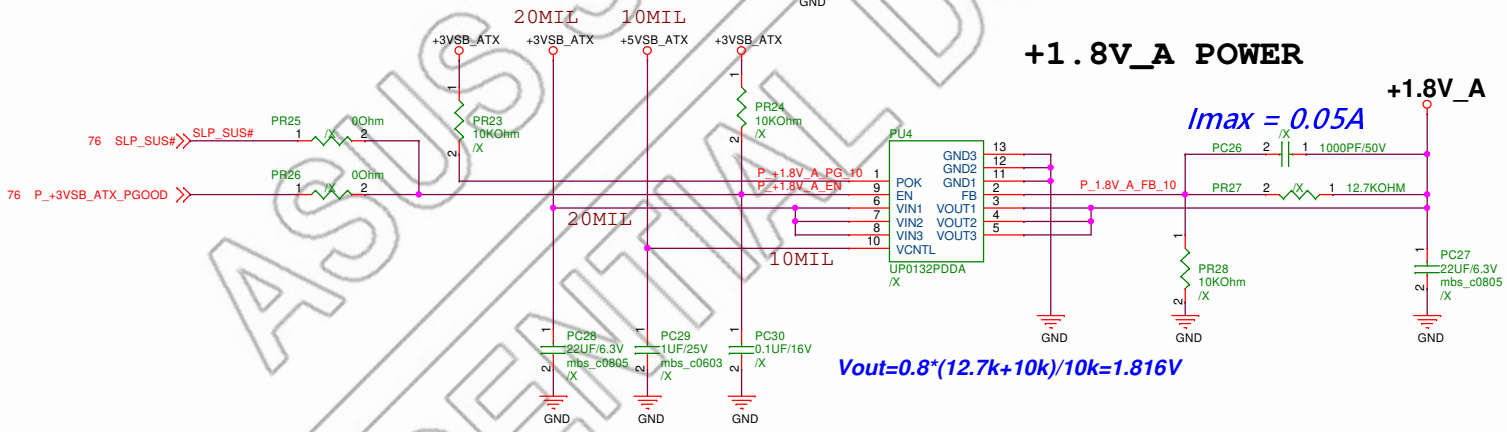
ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | | |
|---|---|---|---|
| ASUS | Title : Selling Point_Logo | | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | | |
| Size A3 | Project Name SMS-H410 | | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 73 of 87 | | |

# +3VSB_ATX POWER




# +1.8V_A POWER

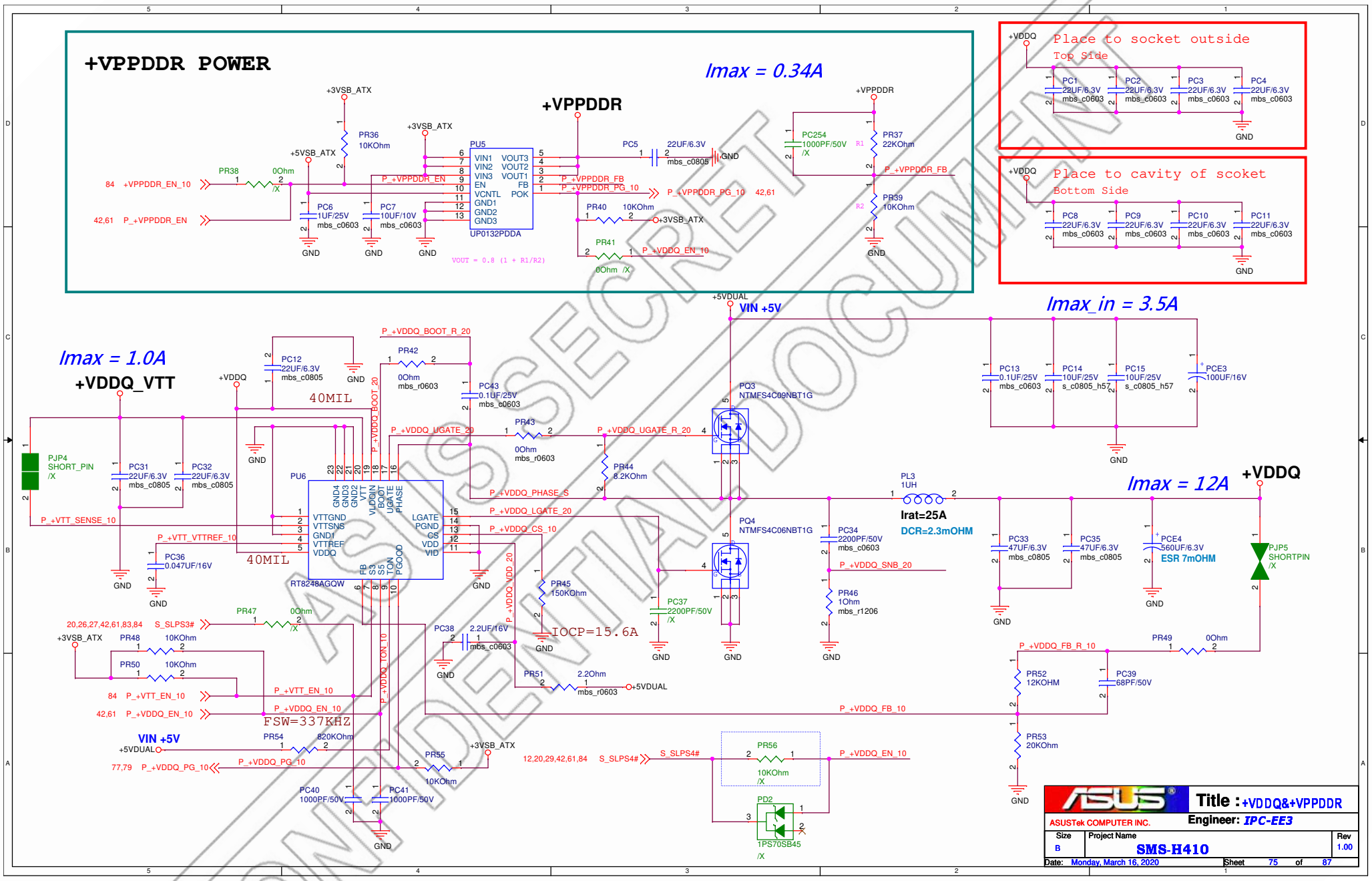



Vout=0.8*(12.7k+10k)/10k=1.816V

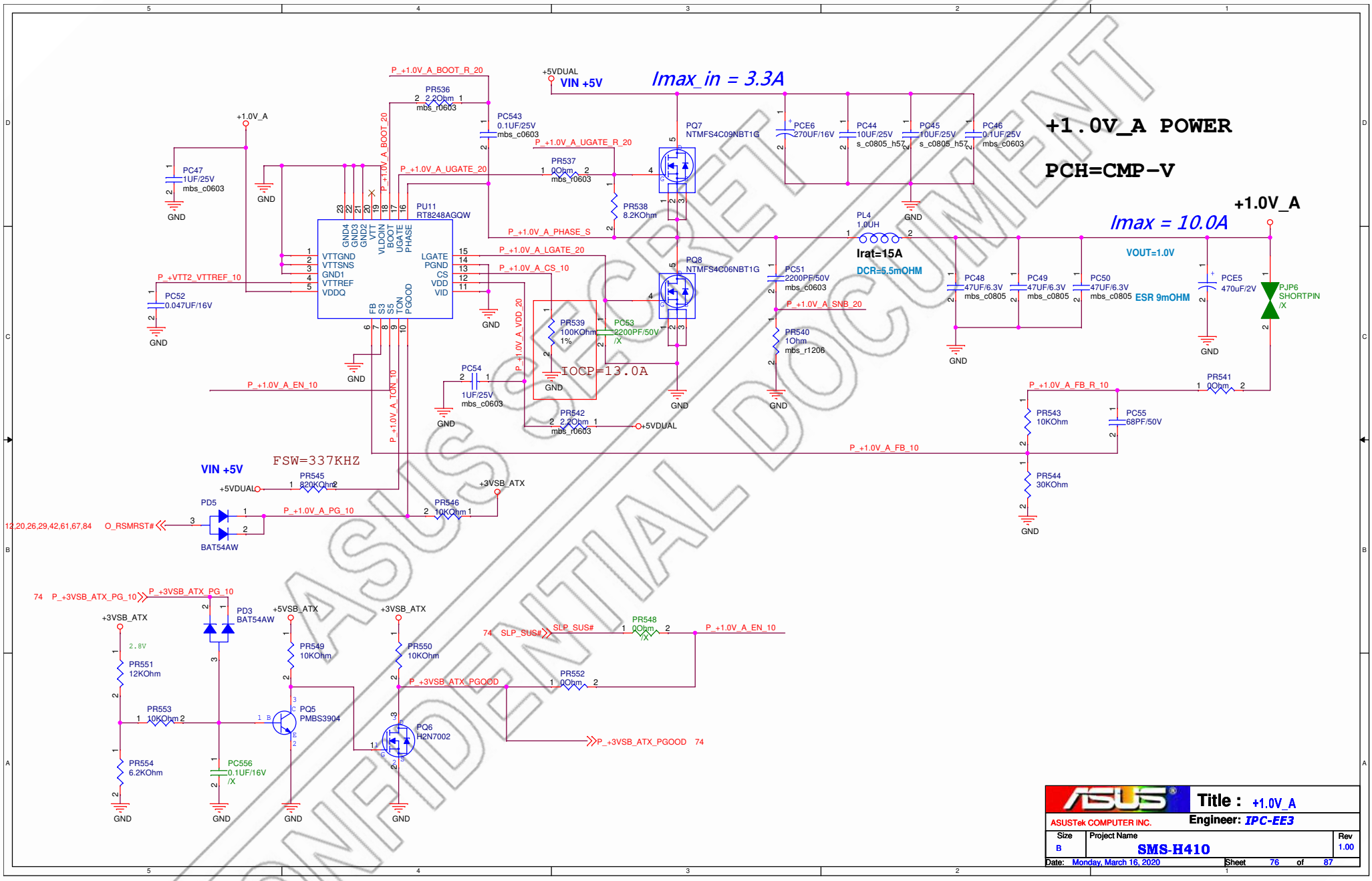
ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

| | | |
|---|---|---|
| ASUS | Title : +3VSB_ATX/+1.8V | |
| ASUSTek COMPUTER INC. | Engineer: IPC-Power | |
| Size B | Project Name SMS-W480 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 74 of 87 | |




ASUS SECRET
CONFIDENTIAL DOCUMENT




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUSTek COMPUTER INC. | Title : +1.0V_A | Engineer: IPC-EE3 |
| Size: B | Project Name: SMS-H410 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 76 of 87 | |

# +VCCIO_0 POWER

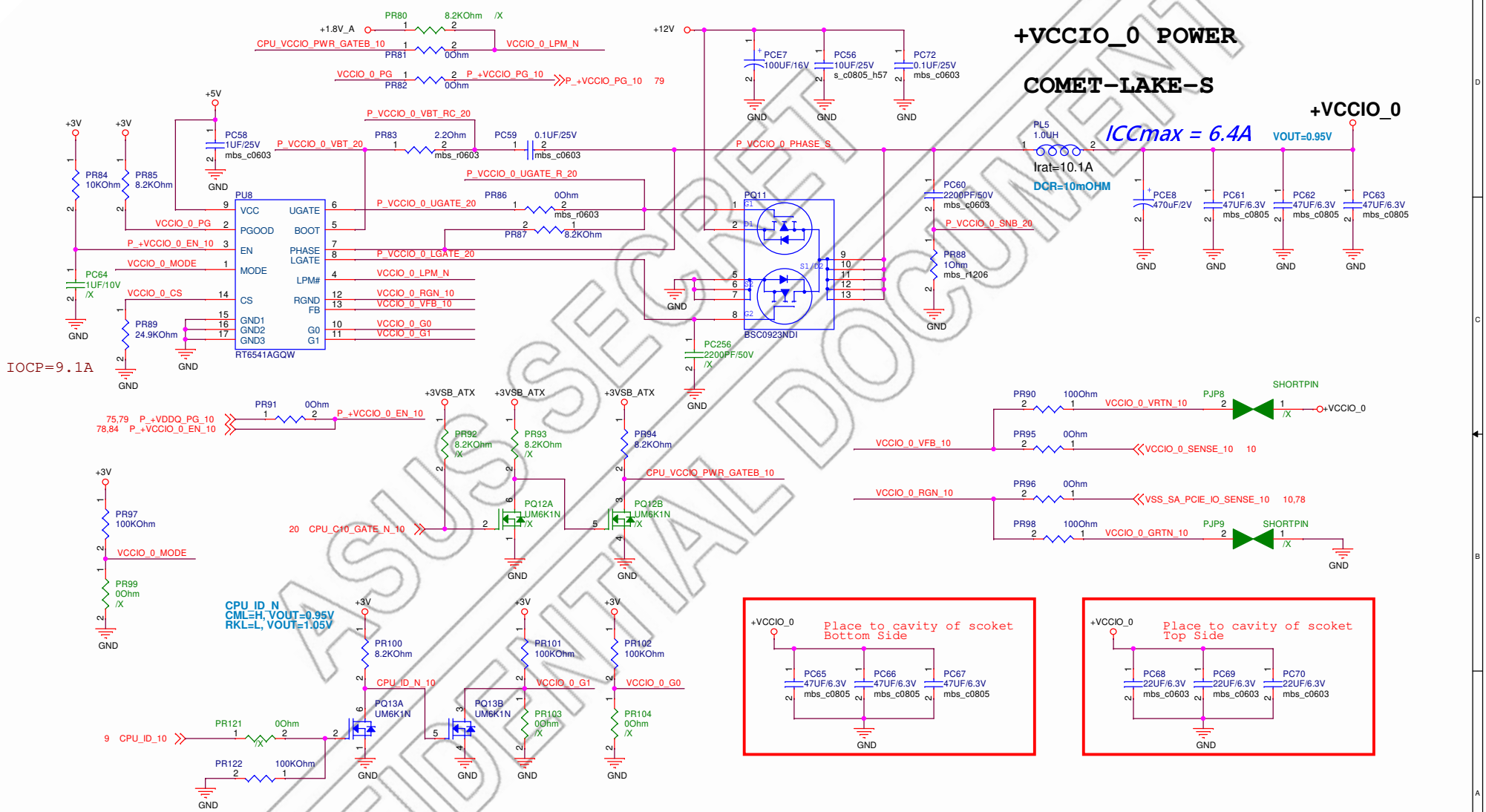
## COMET-LAKE-S

+VCCIO_0

ICCmax = 6.4A

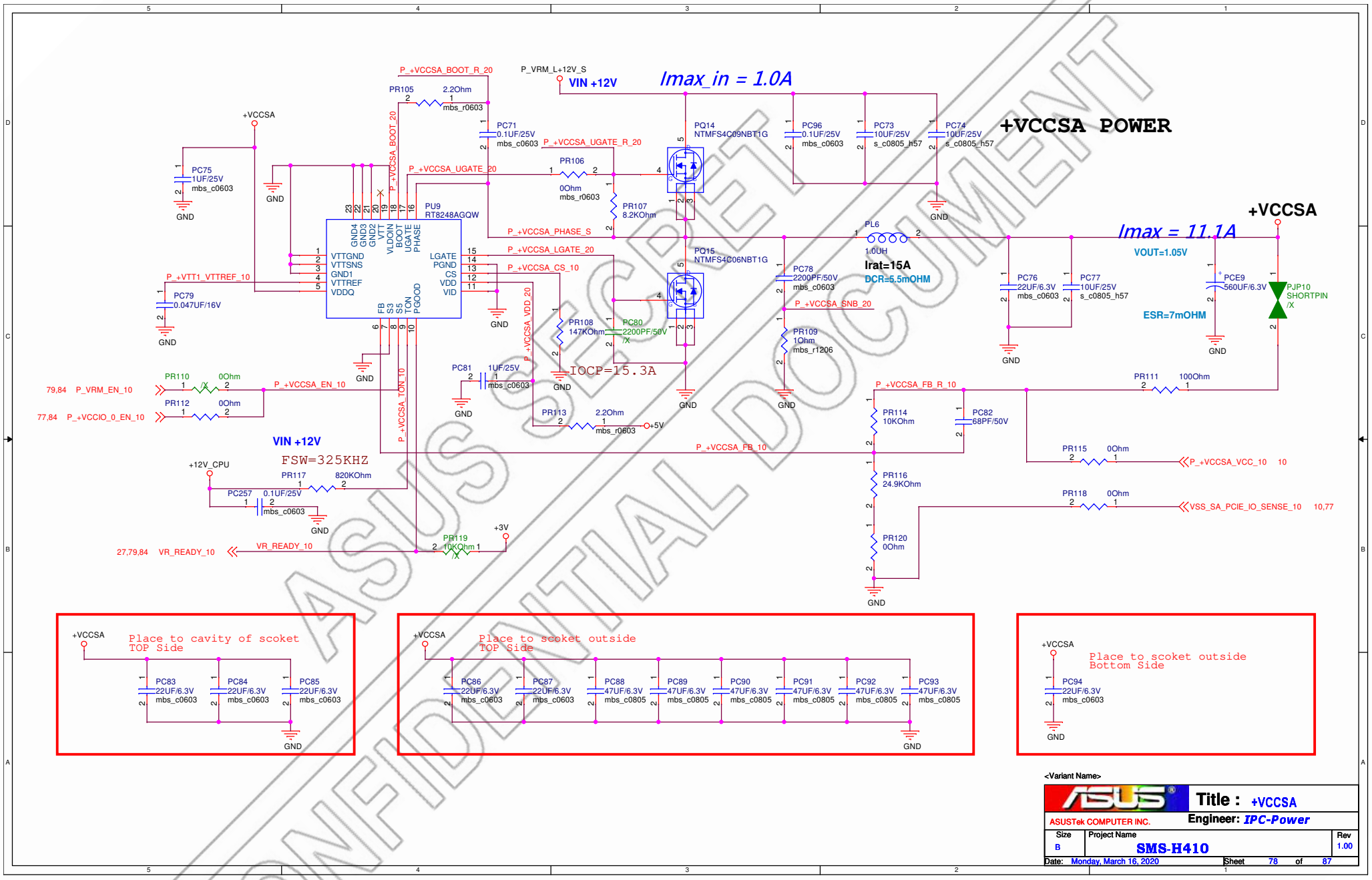
VOUT=0.95V

IOCP=9.1A

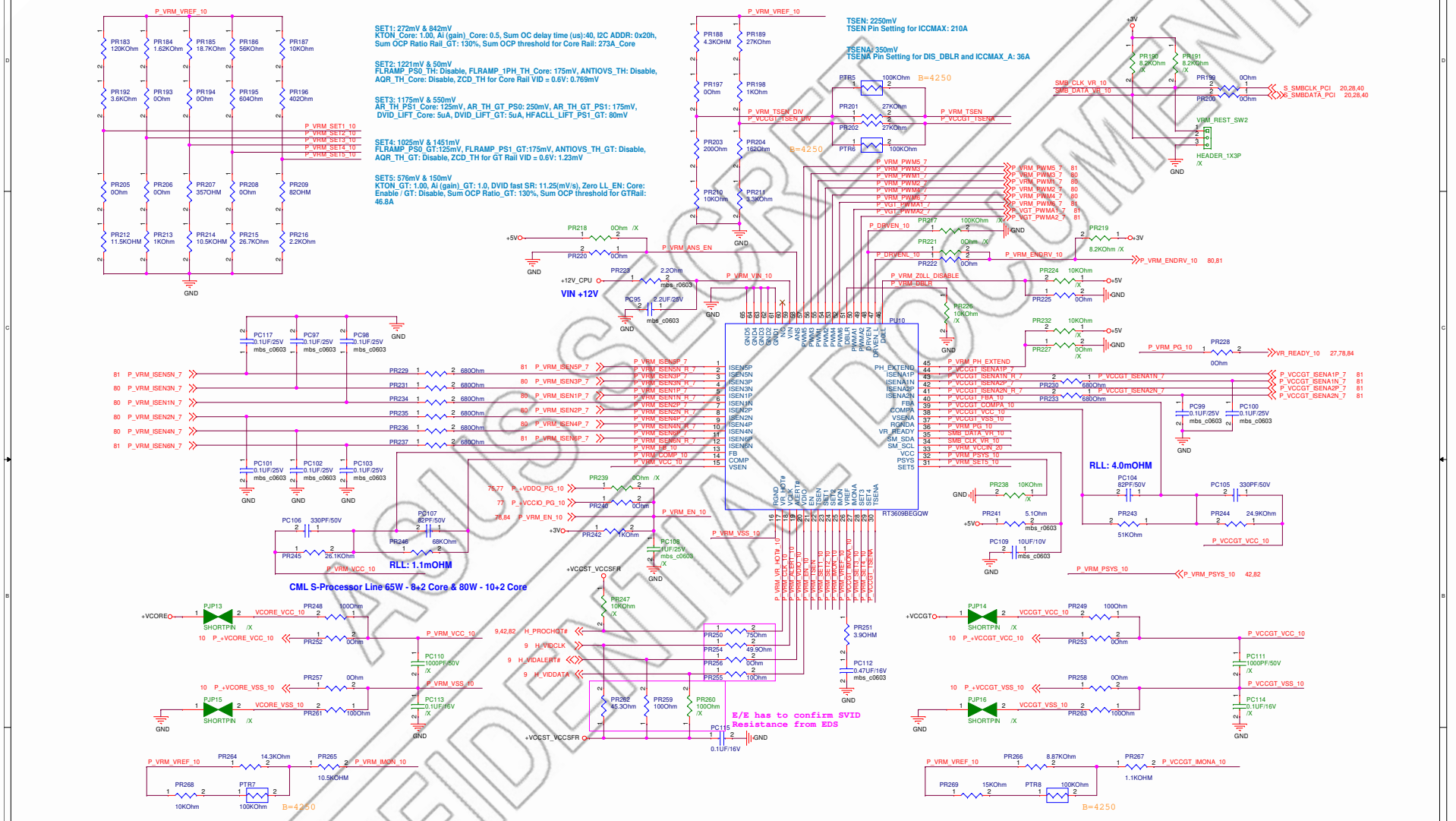



ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : +VCCIO_0 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size B | Project Name SMS-H410 | Rev 1.00 |
| Date: Monday, March 16, 2020 | Sheet 77 of 87 | |




ASUS SECRET
CONFIDENTIAL DOCUMENT




CONFIDENTIAL DOCUMENT

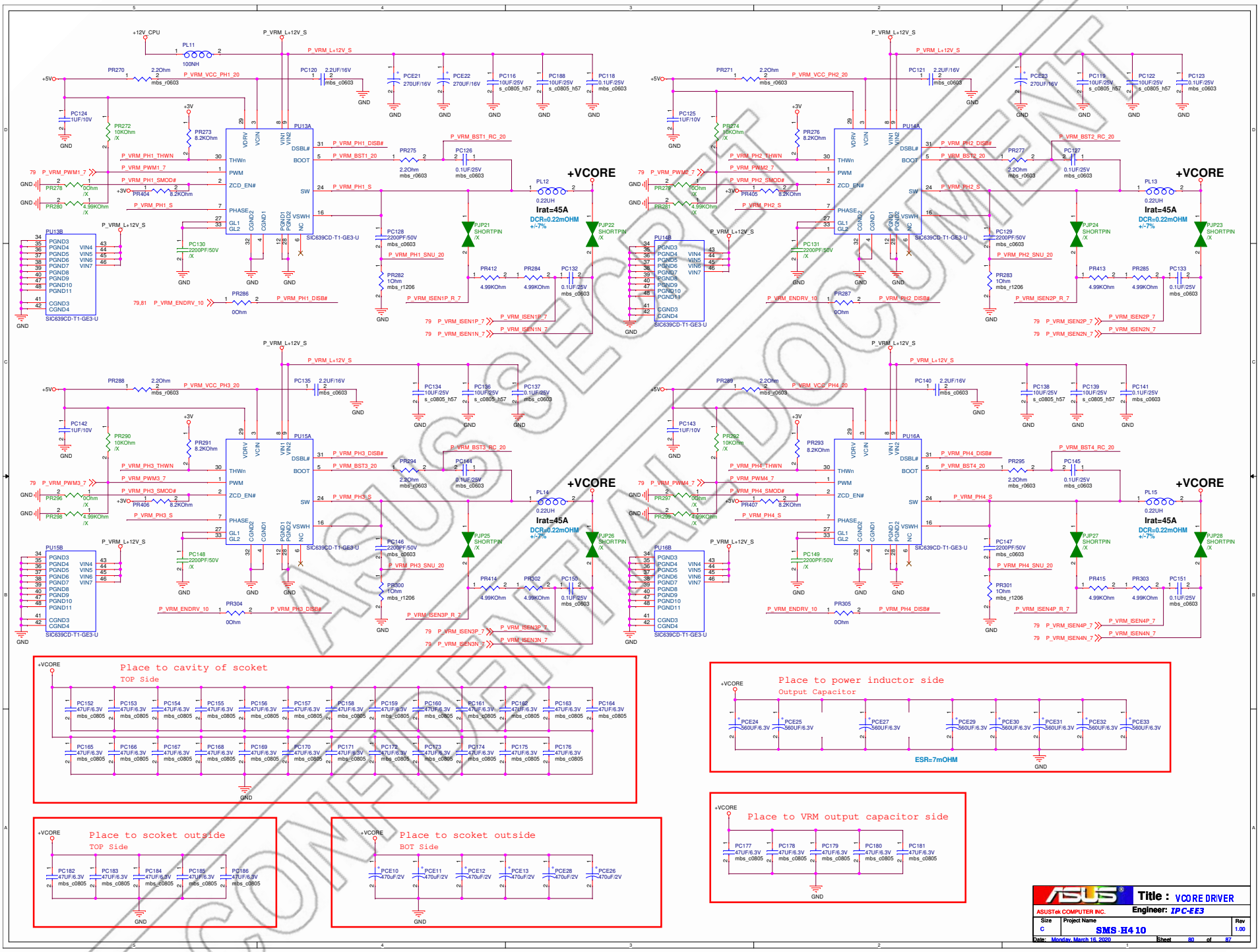
ASUSTeK COMPUTER INC.

Title : VCORE CONTROLLOR

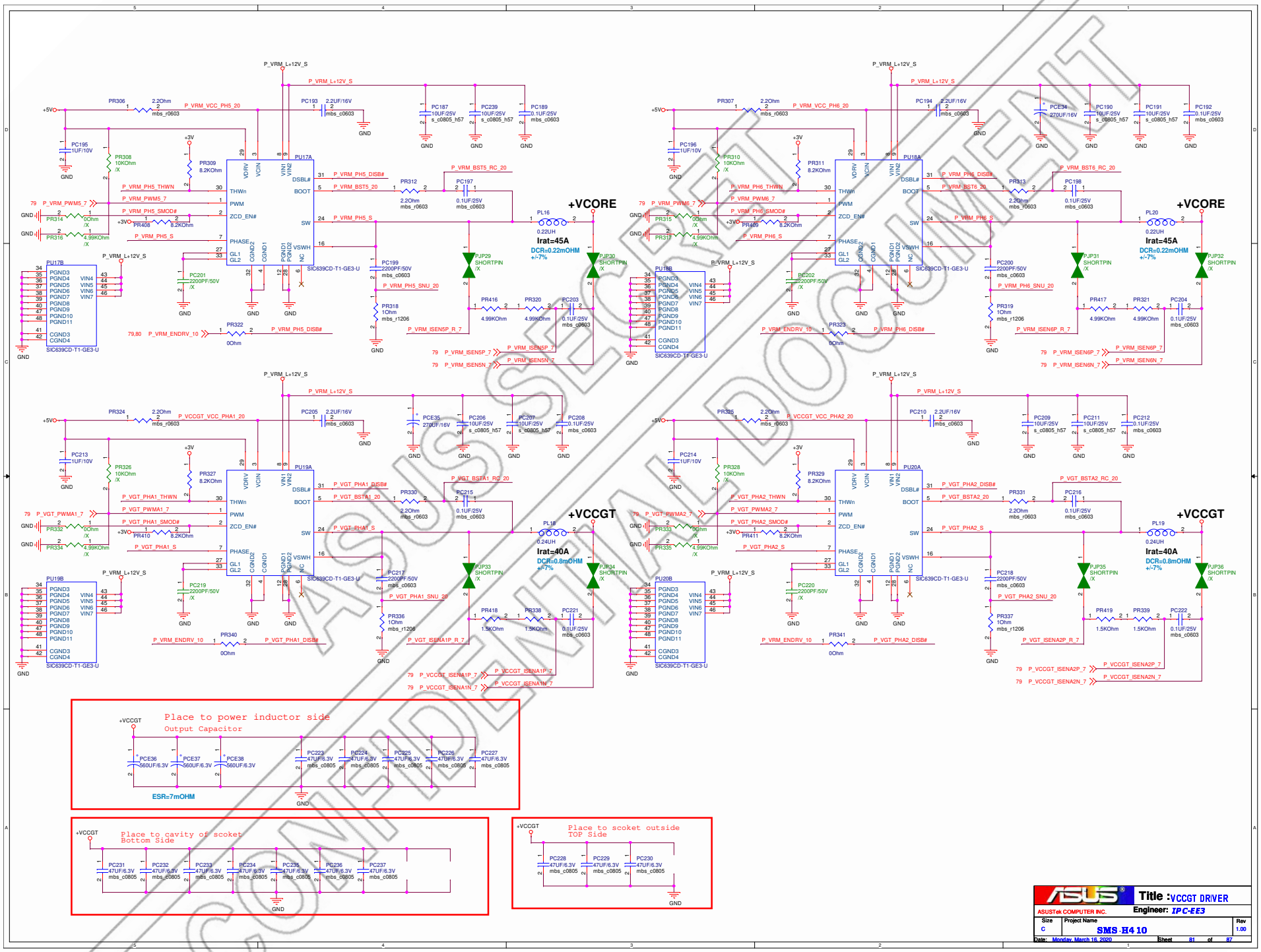
Engineer: IPC-Power

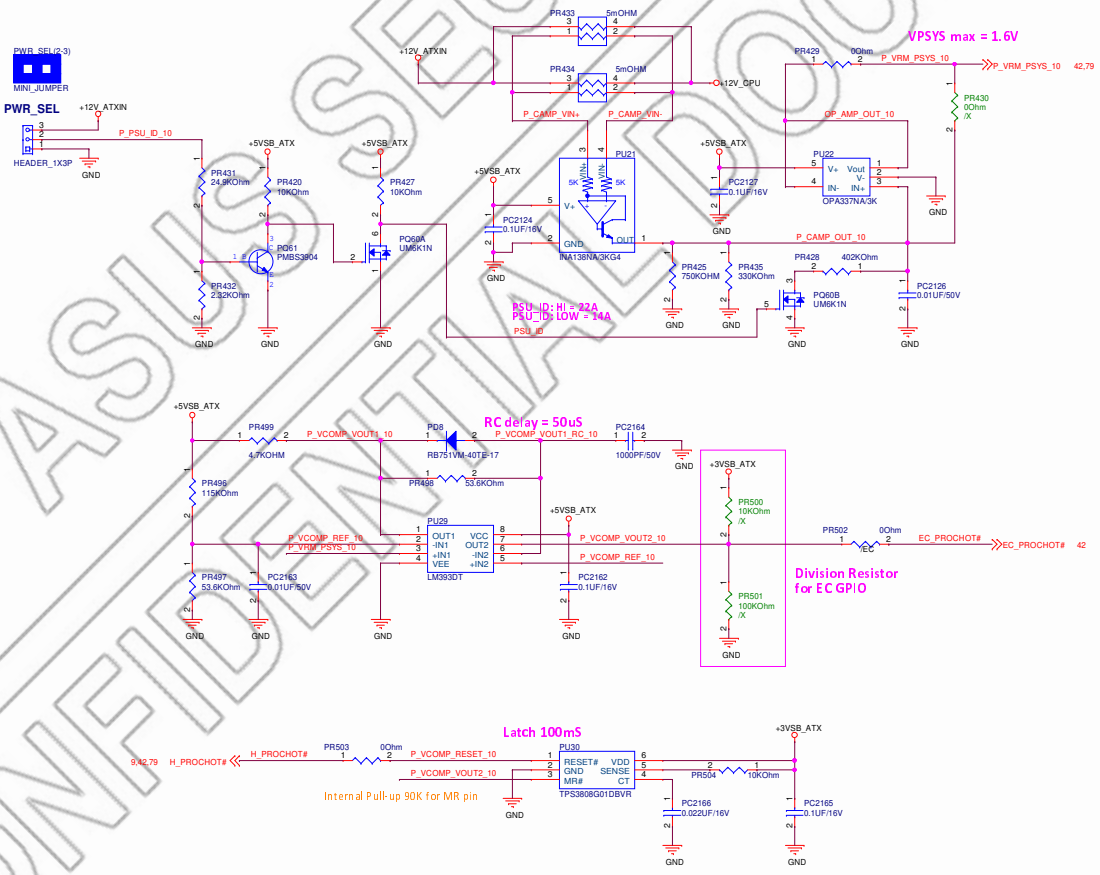
| Size | Project Name | Rev |
|---|---|---|
| C | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 79 of 87



ASUS SECRET
CONFIDENTIAL DOCUMENT


+VCORE
Irat=45A
DCR=0.22mOHM
+/-7%
+VCCGT
Irat=40A
DCR=0.8mOHM
+/-7%
Place to power inductor side
Output Capacitor
ESR=7mOHM
Place to cavity of scoket
Bottom Side
Place to scoket outside
TOP Side
Title :VCCGT DRIVER
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name SMS-H410
Rev 1.00
Date: Monday, March 16, 2020
Sheet 81 of 87




ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUSTeK COMPUTER INC.

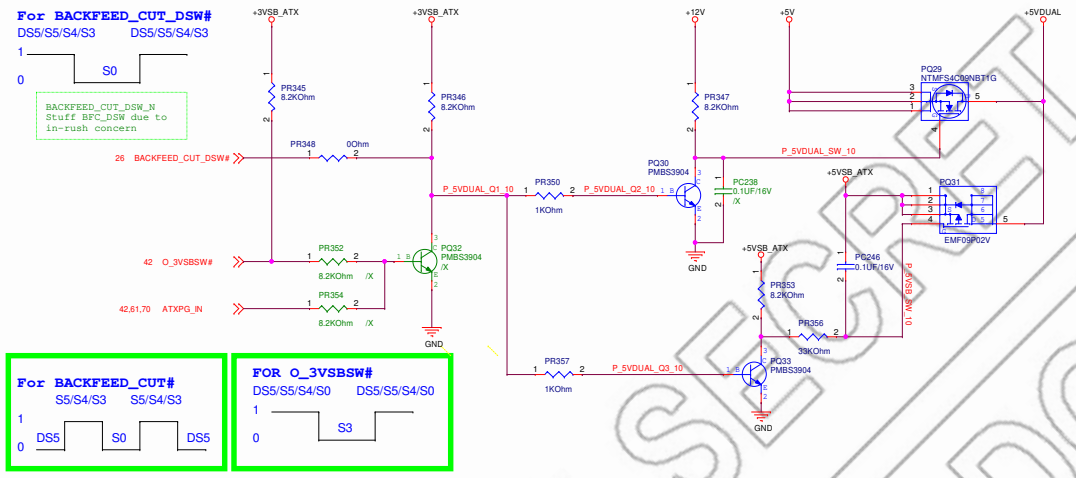
Title : External Power Sense

Engineer: IPC-Power

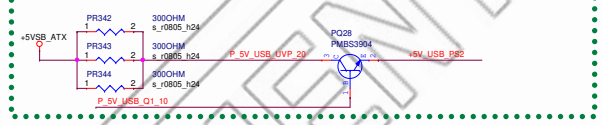
| Size | Project Name | Rev |
|---|---|---|
| C | SMS-H4 10 | 1.00 |

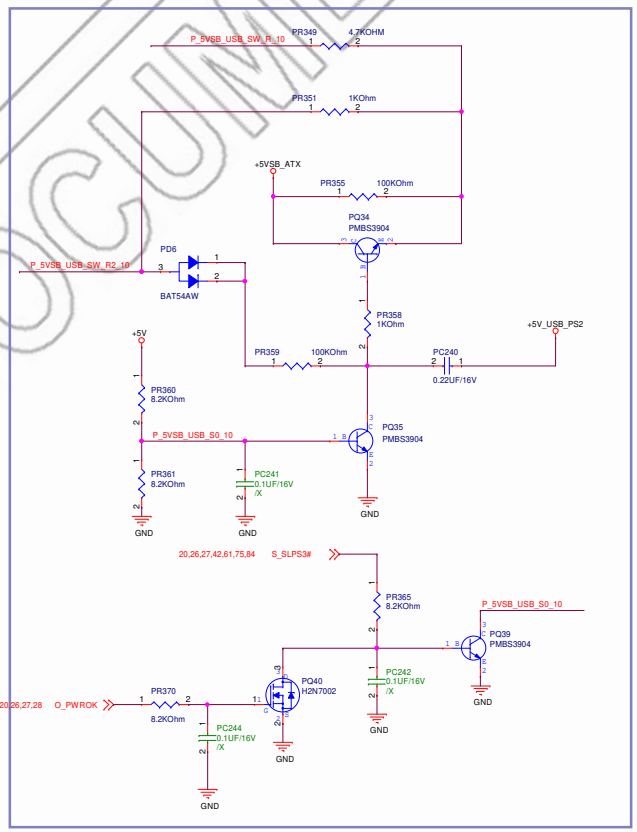
Date: Monday, March 16, 2020 Sheet 82 of 87

# +5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT

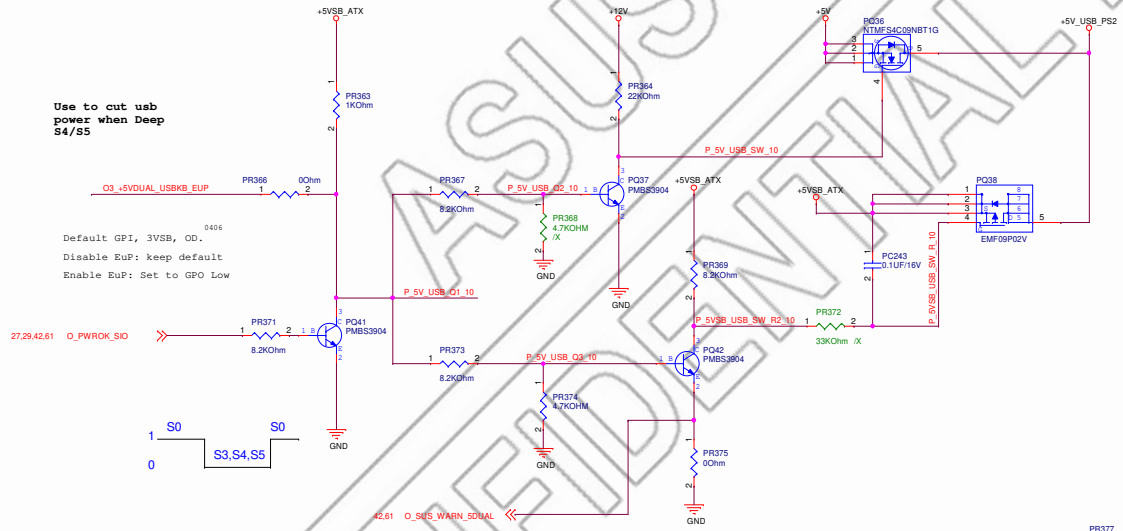


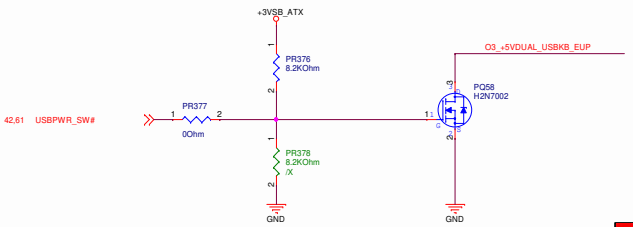

# +5VDUAL_USBKB UVP CIRCUIT



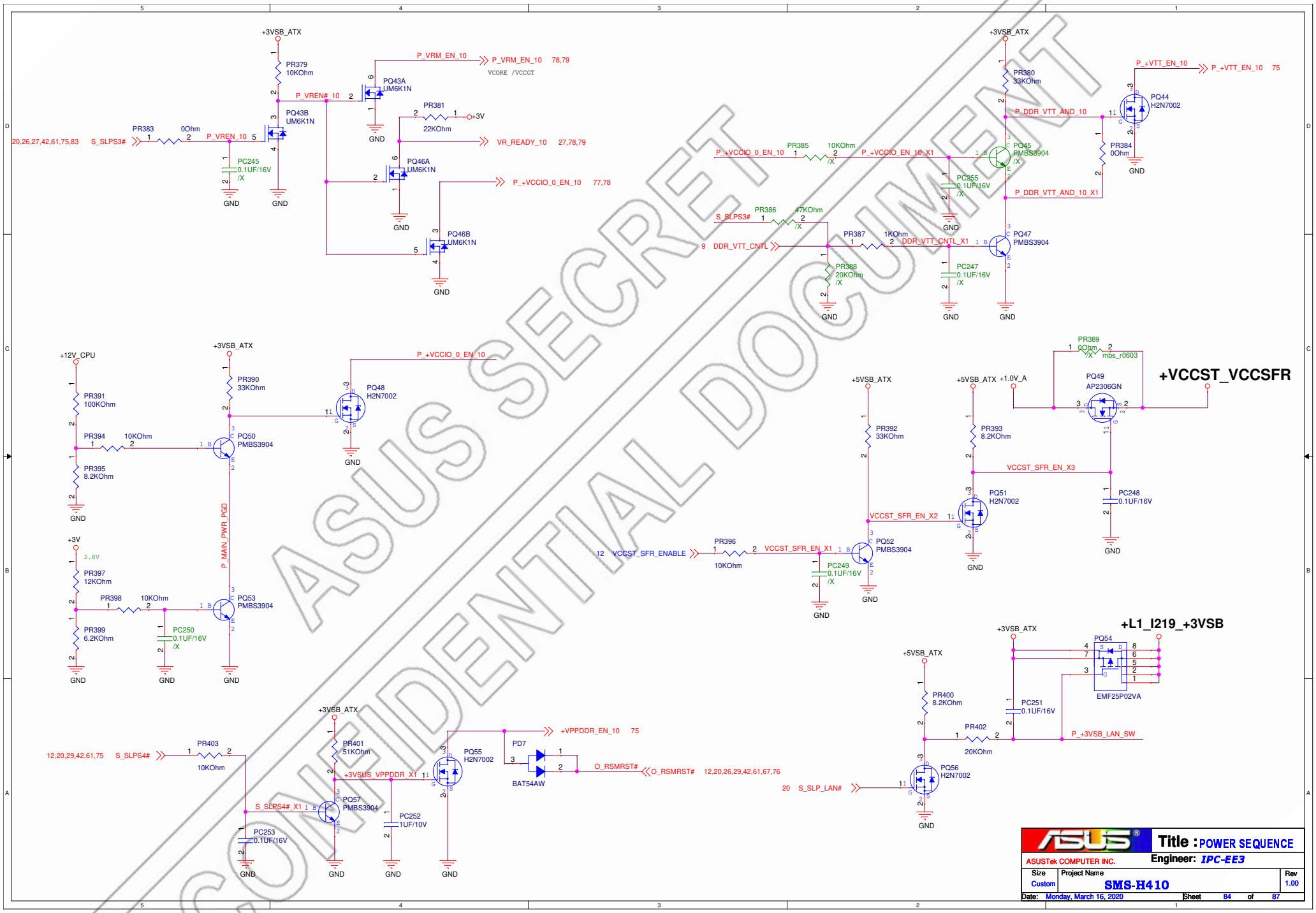

# +5VSB_USBKB VOLTAGE & POWER CIRCUIT




ASUS SECRET
CONFIDENTIAL DOCUMENT

| | | |
|---|---|---|
| ASUS | Title : +5VDUAL/+5V_USB_PS2 | |
| ASUSTek COMPUTER INC. | Engineer: IPC-EE3 | |
| Size: C | Project Name: SMS-H4 10 | Rev: 1.00 |
| Date: Monday, March 16, 2020 | Sheet 83 of 87 | |




ASUS SECRET
CONFIDENTIAL DOCUMENT

## ATX Connector (8 pin)
## EATX_PWR2 for CPU

| | |
|---|---|
| +12V_ATXIN | +12V_ATXIN 70,82 |
| +12V_CPU | +12V_CPU 78,79,80,82,84 |
| P_VRM_L+12V_S | P_VRM_L+12V_S 78,80,81 |

## ATX Connector (24 pin)
## EATX_PWR1 for System

| | |
|---|---|
| +12V | +12V 28,31,32,33,34,35,36,37,40,63,64,65,67,69,70,71,77,83 |
| -12V | -12V 40,67,69,70 |
| +5VSB_ATX | +5VSB_ATX 29,41,42,61,62,66,70,71,74,75,76,82,83,84 |
| +5V | +5V 36,37,40,48,61,62,63,64,65,67,69,70,71,77,78,79,80,81,83 |
| -5V | -5V 70 |
| +5VDUAL | +5VDUAL 75,76,83 |
| +3V | +3V 9,15,17,18,20,21,22,23,24,27,29,30,31,32,33,34,35,36,37,39,40,41,42,43,48,61,64,65,68,70,71,77,78,79,80,81,84 |
| +3VSB_ATX | +3VSB_ATX 9,10,12,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,40,42,43,46,47,48,57,61,64,67,70,74,75,76,77,82,83,84 |

| | | |
|---|---|---|
| +VCORE | +VCORE | 10,79,80,81 |
| +VCCGT | +VCCGT | 10,79,81 |
| +VCCSA | +VCCSA | 10,78 |
| +VCCIO_0 | +VCCIO_0 | 9,10,12,77 |
| +VCCIO_0 +VCCIO_1_2 | +VCCIO_1_2 | 10 |
| +VCCST_VCCSFR | +VCCST_VCCSFR | 9,10,27,61,79,84 |
| +VCCSFR | +VCCSFR | 9,10 |
| +VCCSTG | +VCCSTG | 9,10,12,20 |
| +VDDQ | +VDDQ | 10,13,14,15,16,20,70,75 |
| +VDDQ_VTT | +VDDQ_VTT | 15,16,75 |
| +VPPDDR | +VPPDDR | 10,15,16,75 |
| +3V +VDDSPD | +VDDSPD | 13,14,15,28 |
| +VCCDDQ_EDGECAP2 | +VCCDDQ_EDGECAP2 | 10 |
| +VCCDDQ_EDGECAP1 | +VCCDDQ_EDGECAP1 | 10 |
| +VCCSFR_OC_R | +VCCSFR_OC_R | 10 |
| +1.0V_A | +1.0V_A | 12,24,76,84 |
| +1.0V_A_DSW | +1.0V_A_DSW | 24 |
| +1.0V_A_XCLK_BIAS | +1.0V_A_XCLK_BIAS | 17,24 |
| +1.0V_A_VCCAMPHYPLL | +1.0V_A_VCCAMPHYPLL | 24 |
| +1.0V_A_VCCAPLL | +1.0V_A_VCCAPLL | 24 |
| +3VSB_ATX +DVDDIO_AUDIO | +DVDDIO_AUDIO | 20,24 |
| +3VSB_ATX +3VSB_ADV | +3VSB_ADV | 20,24 |
| +3VSB_ATX +VCCPGPPA | +VCCPGPPA | 24 |
| +3V +VCCATS_3V | +VCCATS_3V | 24 |
| +3V_BAT | +3V_BAT | 18,24,28,61,62 |
| +3V_BAT +VCCPRTC_3P3 | +VCCPRTC_3P3 | 24 |
| +3VSB_ATX +3V_EPW | +3V_EPW | 24 |
| +3VSB_ATX +VCCPGPPD | +VCCPGPPD | 24 |
| +3VSB_ATX +VCCPFUSE_3P3 | +VCCPFUSE_3P3 | 24 |
| +3VSB_ATX +VCCPHVC_3P3 | +VCCPHVC_3P3 | 24 |
| +1.8V_A | +1.8V_A | 24,74,77 |

### CAT Error LED PWR. P9

| | | |
|---|---|---|
| +3V +3VLED | +3VLED | 9 |

### RTC PWR. P28

| | | |
|---|---|---|
| +3V_BAT +BAT_R | +BAT_R | 28 |
| +3V_BAT +BAT | +BAT | 28,42,61 |

### System SPI ROM PWR.P29,30

| | | |
|---|---|---|
| +3VSB_ATX +3V_SPI | +3V_SPI | 29 |
| +3V_SPI +3V_FLBK | +3V_FLBK | 29 |
| +3V_SPI +VCC1833 | +VCC1833 | 29 |
| +1.2V_SPI | +1.2V_SPI | 29 |

### TPM2.0_NPCT750AAAYX PWR.P30

| | | |
|---|---|---|
| +3V_SPI VDD_P8 | VDD_P8 | 30 |
| VDD_P14 | VDD_P14 | 30 |

### DP Port PWR. P35

| | | |
|---|---|---|
| +3V +3V_D_DP1 | +3V_D_DP1 | 37 |
| N_3V_DP1_L | N_3V_DP1_L | 37 |
| +3V_DP1 | +3V_DP1 | 37 |

### DVI-D PWR. P36

| | | |
|---|---|---|
| +3V +3V_DVI | +3V_DVI | 36 |
| +5V +5V_DVI_MOS | +5V_DVI_MOS | 36 |
| +5V_DVI | +5V_DVI | 36 |

### PCI_Asmedia1083 PWR. P39,40.

| | | |
|---|---|---|
| +3V +3VA_EPCI | +3VA_EPCI | 39 |
| +3V +1.2V_EPCI | +1.2V_EPCI | 39,40 |
| +1.2V_EPCI +1.2VA_EPCI | +1.2VA_EPCI | 39 |

### LAN PHY_I219V PWR. P44,45.

Enable :P_+3VSB_LAN_SW

| | | |
|---|---|---|
| +3VSB_ATX +L1_I219_+3VSB | +L1_I219_+3VSB | 44,45,84 |
| +L1_I219_0.9V | +L1_I219_0.9V | 44 |
| L1_CTR | L1_CTR | 45 |

### LAN PHY_I210AT PWR. P46,47.

| | | |
|---|---|---|
| +3VSB_ATX +3V_AUX2 | +3V_AUX2 | 46 |
| +1.5V_LAN2 | +1.5V_LAN2 | 46,47 |
| +0.9V_LAN2 | +0.9V_LAN2 | 46 |
| L2_CTR | L2_CTR | 47 |

### Audio ALC887-VD2-GR PWR. P41

| | | |
|---|---|---|
| +3V +3.3V_AUDIO | +3.3V_AUDIO | 41 |
| +5VSB_ATX +5V_AUDIO | +5V_AUDIO | 41 |
| +5VSB_ATX +LDOVDD | +LDOVDD | 41 |

Stuff for ALC886

Stuff for ALC892/887

### USB20 HUB_GL850G PWR. P48

| | | |
|---|---|---|
| +5V +5V_IN | +5V_IN | 48 |
| +3V +3V_AVDD | +3V_AVDD | 48 |
| +3V +3V_DVDD | +3V_DVDD | 48 |

### +5V_USB PWR

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB_PS2 | +5V_USB_PS2 | 53,54,55,56,57,58,59,71,83 |

### USB31 Gen1 Type-A Port PWR in LAN1. P45,53

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB3_P12 | +5V_USB3_P12 | 45,53 |

### USB31 Gen1 Internal Header. P54

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB3_P34 | +5V_USB3_P34 | 54 |

### USB20 Type-A Port PWR in LAN2. P47,55

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB2_P56 | +5V_USB2_P56 | 47,55 |

### USB20 Type-A 2X2 Port PWR. P56

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB2_P78 | +5V_USB2_P78 | 56 |

### USB20 Vertivcal Type-A Port PWR. P57

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB2_P9 | +5V_USB2_P9 | 57 |

### USB20 Header#01 Port PWR. P58

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB2_P1112 | +5V_USB2_P1112 | 58 |

### USB20 Header#02 Port PWR. P59

| | | |
|---|---|---|
| +5V_USB_PS2 +5V_USB2_P1314 | +5V_USB2_P1314 | 59 |

### Power LED PWR. P62

| | | |
|---|---|---|
| +5VSB_ATX +5VSB_LED | +5VSB_LED | 62 |
| +5V +5V_LED | +5V_LED | 62 |

### COM1 Port PWR. P64

| | | |
|---|---|---|
| +12V RI_VCC | RI_VCC | 64 |
| +5V RI1_F_VCC | RI1_F_VCC | 64 |

### CPU&SYS-NCT3949S/Power Fan PWR. P65

| | | |
|---|---|---|
| +12V +FP_VOUT | +FP_VOUT | 65 |
| +12V +FP1_VOUT | +FP1_VOUT | 65 |
| +12V +FP2_VOUT | +FP2_VOUT | 65 |
| +12V +FP3_VOUT | +FP3_VOUT | 65 |
| +3V +3V_PWRFAN | +3V_PWRFAN | 65 |

### Front Panel, LED & Button PWR. P70

| | | |
|---|---|---|
| +3V RSTCON#_PANEL | RSTCON#_PANEL | 42,61,70 |
| +5VSB_ATX PLED+ | PLED+ | 70 |
| +VDDQ PLED- | PLED- | 70 |
| +5V HDLED+ | HDLED+ | 70 |

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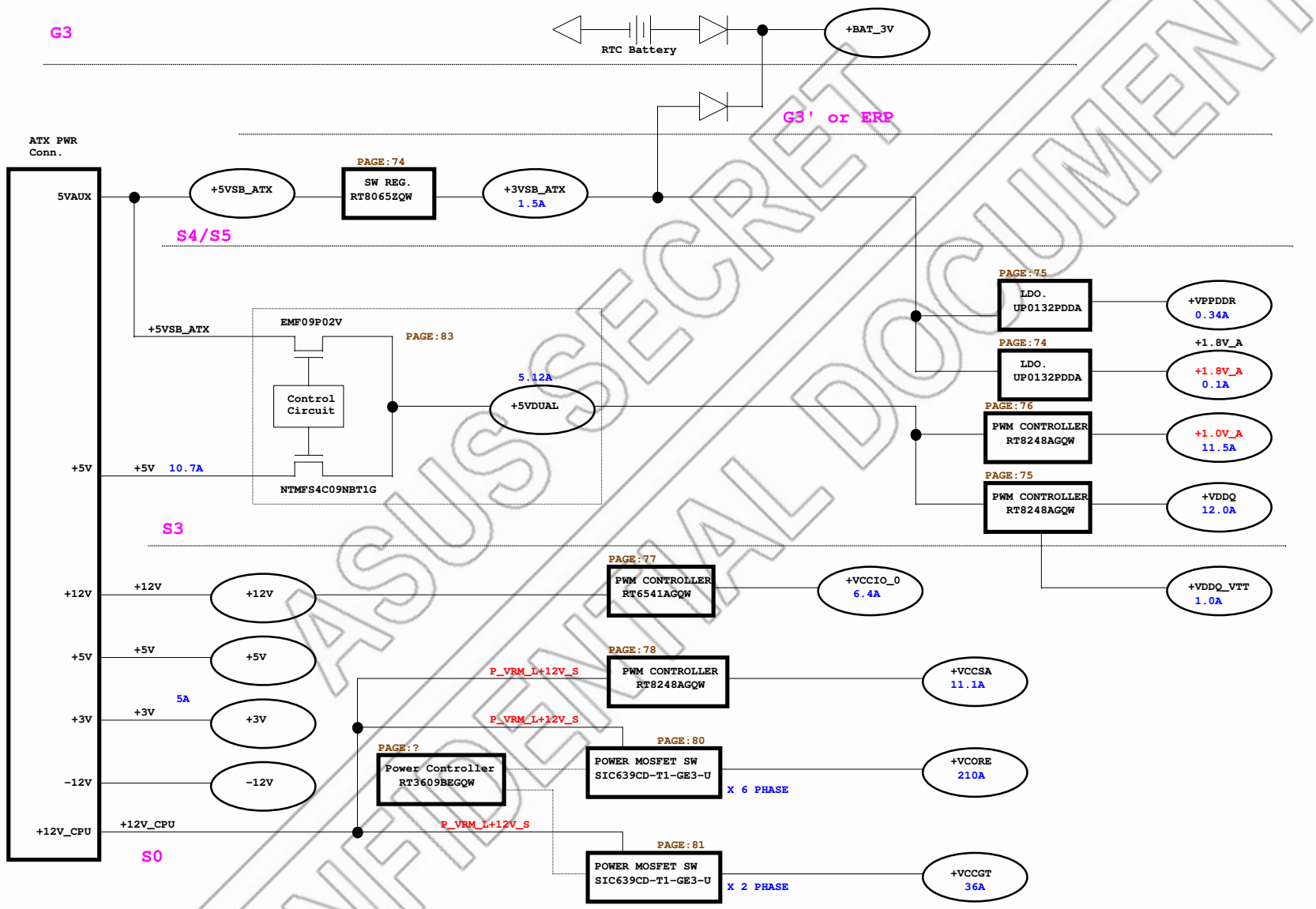
ASUSTek COMPUTER INC.

Title : History - 01

Engineer: IPC-EE3

| Size | Project Name | Rev |
|---|---|---|
| Custom | SMS-H410 | 1.00 |

Date: Monday, March 16, 2020 Sheet 85 of 87

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ASUSTek COMPUTER INC.

Title : Power Flow

Engineer: IPC-EE3

Size: Custom | Project Name: SMS-H410 | Rev: 1.00

Date: Monday, March 16, 2020 | Sheet 86 of 87

| Rev | Date | Description |
|---|---|---|
| V1 | 1/21/2020 | First Release |
| Green | | |
| V2 | 1/22/2020 | 01. Change default to PD at SOFTOFF_LED_C. Page70. |
| Green | | 02. Reserve S_SLPS4# to BIOS Flash Back AI1315. Page29. |
| | | 03. Change USB Power Switch at port 13/14 for BIOS flash back. Page29,58. |
| V3 | 2/07/2020 | 01. Add 0 ohm at PCH to CPU CLK P/N. Page17. (Siemens Request). |
| Green | | 02. Modfiy SPI Power from +3V_SPI to +3VSUS(=+3VSB_ATX). Page 29,30. (Siemens Request). |
| | | 03. Reserve ESD at LAN MDI signal and remove LAN_GND. Page45,47. (Siemens Request). |
| | | 04. ADD ESD Protect at USB_OC# Pin. Page53,54,55,56,57.58.59. (Siemens Request). |
| | | 05. Change Power Switch IC Footprint P/N:06016-01300000 AP22803AM8-13/DIODES SOP8. Page57. |
| | | 06. Change CPU ILM1/ILM2 CML-S LGA1200 Module. Page11. |
| | | 07. Change SIO monitor RTC power rail. Page28,61. (Siemens Request). |
| | | 08. Modify XDP_PRSENT# circuit. Page12. |
| | | 09. Reserve JTAG_TCK PD resister, SR2001. Page20. |
| | | 10. ADD XDP BOM Option:XDP, /X_XDP. Page12,20. |
| | | 11. Remove XDP_HOOK7 PH. Page12. (Becasue already PH OR145 at Page70). |
| | | 12. Modify PCH GPIO Power description. Page24. |
| | | 13. ADD Function Page in Block Diagram. Page01. |
| | | 14. Use SLP_S4# to drive FB_PWRSUS# and modify net name FB_SPI_UPD. Page29. |
| | | 15. Change OR84 to 0ohm for SOFTOFF_LED drive. Page70. |
| | | 16. Modify Thermal Sensor TR4, TR6 Netname. Page61,66. |
| | | 17. ADD PCB41=560uF/6.3V for +VDDQ. Page16. |
| | | 18. Modify DDR VREF circuit : Page16. (Non-compatibility Board with 2021 next gen. design) |
| | | 19. Modify SPI series resister to 56ohm. Page29,30. (Follow CML-S PDG, SPI 2 load topology) |
| | | 20. Follow SMS-W480 Power Solution. Page74,75,77-81,86. (Please refer Siemens_Questions.docx) |
| V4 | 2/24/2020 | 01. Modify CML-S CPU +VCORE Power Circuit. Page79,80,81. |
| Green | | 02. modify DDR4 SMBus Power to +VDDSPD from +3V at p.28 (Siemens advise) |
| | | 03. reserve PC256 at +VCCIO MOS Gate, p.77 |
| | | 04. remove PCH reserve TP for layout request at p.17, 18, 21-23 |
| | | 05. change poly fuse to power switch for USB power and control by PCH at p.19, 23, 53-59 |
| | | 06. change +3VSUS to +3VSB_ATX, follow SMS-W480 |
| | | 07. swap DDR4 DQ at CPU side for layout request at p.7, 8 |
| | | 08. correct +VCORE choke(PL12~PL16, PL20) footprint at p.80, 81 |
| | | 09. add 0.1uF and 220ohm between DVI TX P/N at p.36 |
| | | 10. change +1.8VSUS to +1.8V_A, follow SMS-W480 |
| | | 11. PCE28 chagne to 7343 cap. from DIP package for SMS-W480 layout placement. Page80. |
| | | 12. Correct PCH heatsink footprint for SMS-W480 layout. Page26. |
| | | 13. Modify SMBus pull-high resister (SR73,SR74). Page28. |
| | | 14. add EC IT5125 and modify SIO circuit at p.42 |
| | | 15. modify COM port design at p.61, 64, 68, 69 |
| | | 16. move Temp, Fan relation control to EC form SIO at p.42, 61, 66 |
| | | 17. Swap LPC Clock at p. 22, 43 |
| | | 18. add diode at FB_PWRSUS# for S_SLPS4# control from EC at p.29 |
| | | 19. Change DIO#1~#4 to HDD_ALERT#1~#4 and control by EC. Page42,61,70. |
| | | 20. Change LED control to EC from SIO. Page18,28,42,61,70. |
| | | 21. Reserve LED control from PCH. Page20,23. |
| | | 22. add External Power Sense Circuit at p.79, 82 |
| V5 | 3/16/2020 | 01. ADD 0.1uF cap. PC257 at +12V_CPU for noise concern. Page85. |
| Green | | 02. Move bigger capcitor to USB connector side. Page53-59. |
| | | 03. Modify EC_SCI#/SMI# circuit and add PME# at SIO. Page21,22,42,61. |
| | | 04. Unmount PECI path at SIO. Page61. |
| | | 05. Unmount O_PCIEX1_RST# PH. Page42. |
| | | 06. Reserve 0 ohm at SPI path for EC share ROM test. Page18,42. |
| | | 07. ADD BOM option for EC. Page42. |
| | | 08. modify Power circuit. Page70,73,83. |
| | | 09. Thermal Sensor change to APL6002AA8I-TRG/ANPEC SOT23-8. Page66. |
| | | 10. Modify +1.8V_A Power (for eSPI) to reserve. Page24,74,77. |
| | | 11. Change New TPM20 IC to P/N:06120-00080200 NPCT750AABYX/NUVOTON FW:7.2.1.0. Page30. |
| | | 12. Unused DDI3 Port, so delete ST115,ST116. Page06. |
| | | 13. Swap net name for layout request at Page37,48,53-59. |
| | | 14. Reversed PR92/PR93/PQ12 (Option:/X) for PCH-V doesn't have C10 Power Gate function. Page77. |
| | | 15. Modify & ADD EC/IT5121E-I-128/CX in Block Diagram. Page01. |
| | | 16. ADD External PWR Sense : +12V_ATXIN PWR. Page70,82,85. |
| | | 17. Phase in SMS-H410 R1.00 08 PCB Part Number:08001-15160X00. Page73. |
| | | 18. ADD Fiducial Mask: INDEX37,38,39,40 x4PCS for EMS Facotry SMT. Page73. |
| | | 19. add PROCHOT circuit at p.42, 82 |
| | | 20. remove some TP at PCH for layout request at p.18, 23 |

| Rev | Date | Description |
|---|---|---|

| Rev | Date | Description |
|---|---|---|

| Rev | Date | Description |
|---|---|---|

ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTeK COMPUTER INC.

Title : History - 01

Engineer: IPC-ESS

| Size | Project Name | Rev |
|---|---|---|
| D | BMB-H410 | 1.00 |

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