MIX-TLUD1 Rev 1.00

DC Jack (Screw type)
ATX 4Pin
Two Conn. (+12V power input)

DDR4 SO-DIMM 2666MHz non-ECC — Channel A
DDR4 SO-DIMM 2666MHz non-ECC — Channel B

INTEL Tiger Lake UP3

- DDI-A → eDP 1.4b → eDP
- DDI-B → eDP 1.4b → CH7511B → LVDS → LVDS
- TCP1 → HDMI → SN75DP159 → HDMI 2.0b → HDMI
- TCP2 → HDMI → SN75DP159 → HDMI 2.0b → HDMI
- TCP3 → DisplayPort 1.4a → DP++
- TCP4 → DisplayPort 1.4a → DP++
- PCIe x4 → PCIe Gen4 x4 16GT/s → NGFF M-Key 2280
- PCIe Port 5/6/7/8 → PCIe Gen3 8GT/s → PCIE x4 slot
- SATA Port 0 → SATA 3.0 6Gb/s → SATA3 → SATA PWR
- HDA → HDA → AUDIO ALC887 → Line out / Mic in → AAFP
- SPI0 → SPI0 → TPM 2.0 NPCT750AABYX

RJ45 → INTEL LAN I219-LM → GbE → PCIe Port 9
USB2.0 x2 port → USB2.0 x2 480Mb/s → USB2 Port 5/6

RJ45 → INTEL LAN I225-V → PCIe Gen3 x1 8GT/s → PCIe Port 10
USB3.1 x2 port → USB3.2 Gen2 x2 10Gb/s → USB3 Port 1/2
USB2.0 x1 480Mb/s → USB2 Port 1

SPI flash 256Mb ↔ SPI Interface AI1315 (USB2.0 x1 480Mb/s, SPI) → USB2 Port 2 (SPI0)

USB2.0 x2 port → USB2.0 x2 480Mb/s → USB2 Port 8/9

SIM Card slot ↔ Mini PCI-E card (Full size) → PCIe Gen3 x1 / SATA Gen3 x1 8GT/s 6 Gb/s → PCIe Port 12 / SATA Port 1
USB2.0 x1 480Mb/s → USB2 Port 7

USB3.2 GEN1x 2 port Box header → USB2.0 x2 480Mb/s → USB2 Port 3/4
USB3.2 Gen1 x2 5Gb/s → USB3 Port 3/4

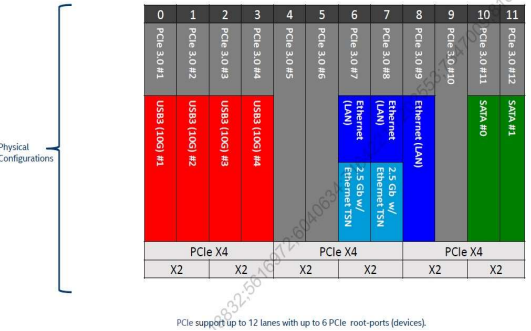
PCH-LP

Debug Port ↔ eSPI ↔ IT5121E

IT5121E → F81438G → COM1 (w/ 5V/12V) RS-232/422/485
IT5121E → COM2 (RS232)
IT5121E → CPU_FAN
IT5121E → SYS_FAN
IT5121E → HW Montior
IT5121E → Digital I/O
IT5121E → WatchDog Timer

Exteranl Connector
Internal Connector

TIGER LAKE-UP3 PCH-LP HSIO LANE ASSIGNMENTS



PCIe support up to 12 lanes with up to 6 PCIe root-ports (devices).

Final configuration will be based on SKU

MIX-TGLD1

ASUSTek COMPUTER INC.

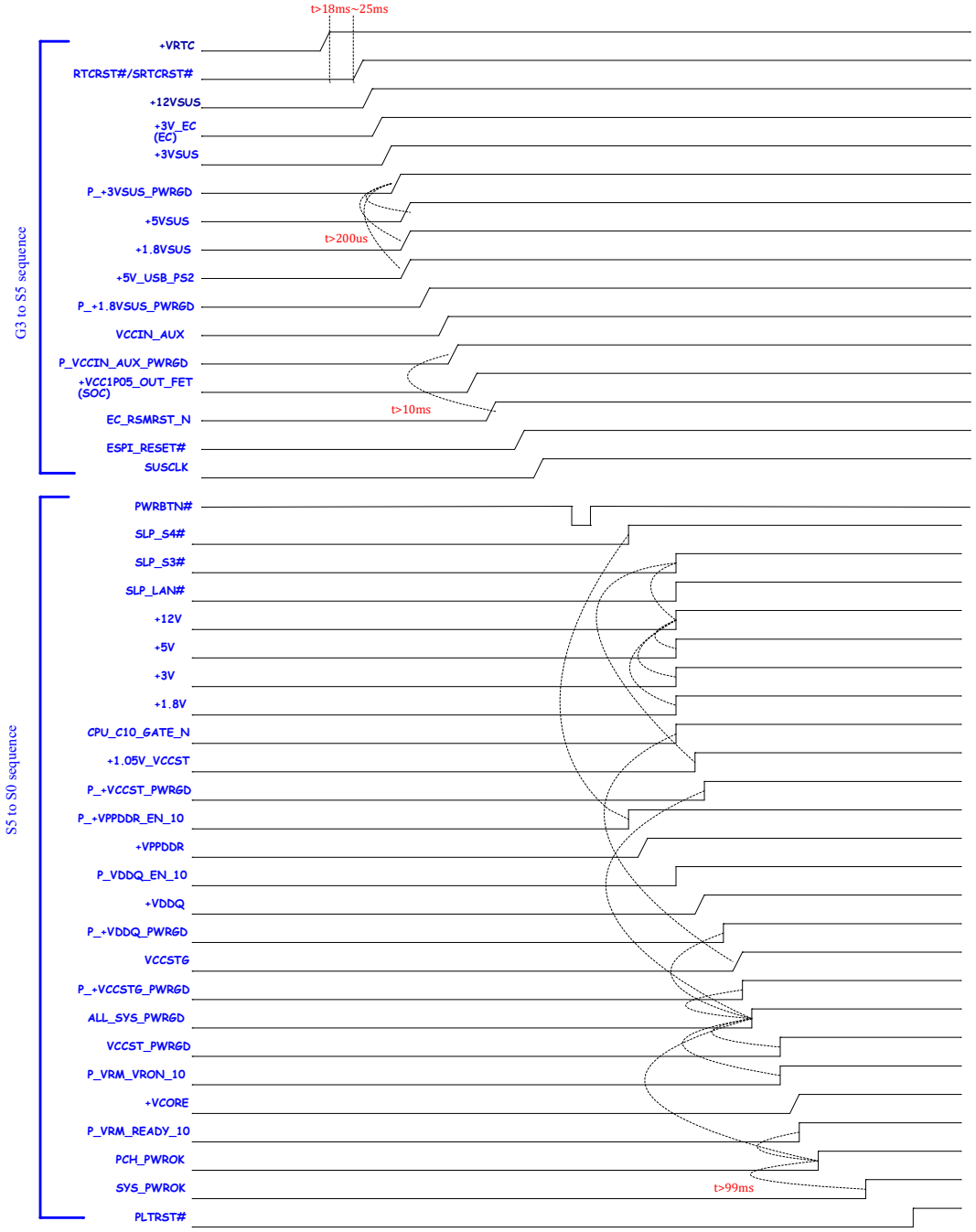
Title : Block Diagram

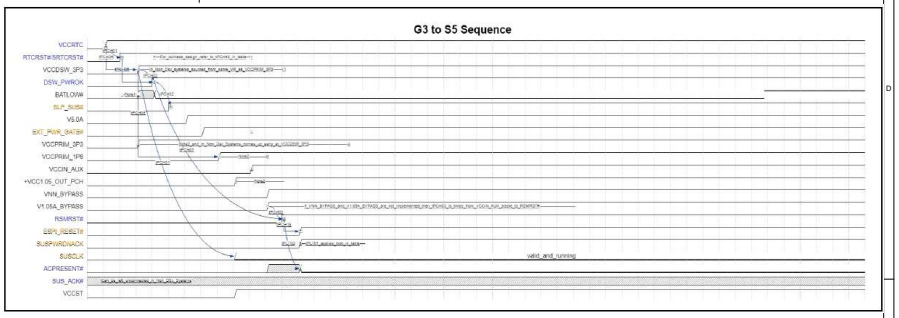
Engineer:

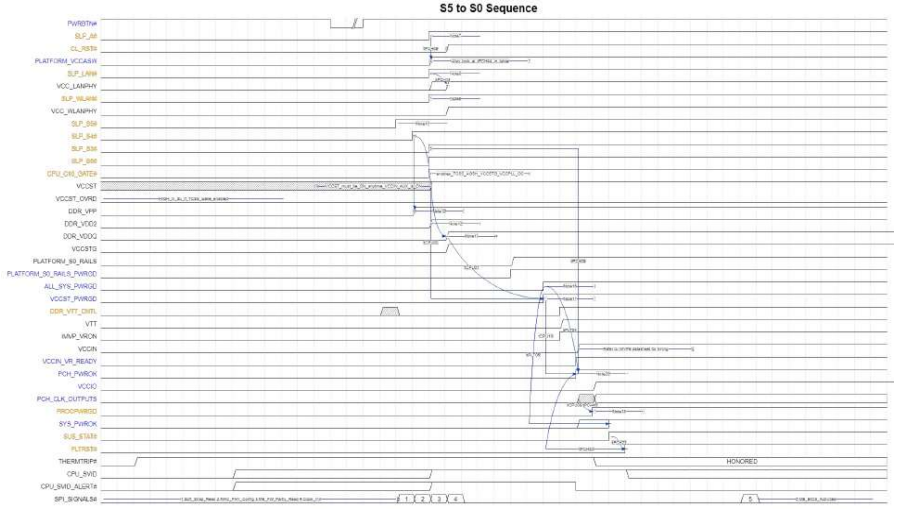
Size	Project Name	Rev
Custom	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 1 of 59

Tiger Lake G3 to S0 power on sequence (Non-Deep Sx Platform)

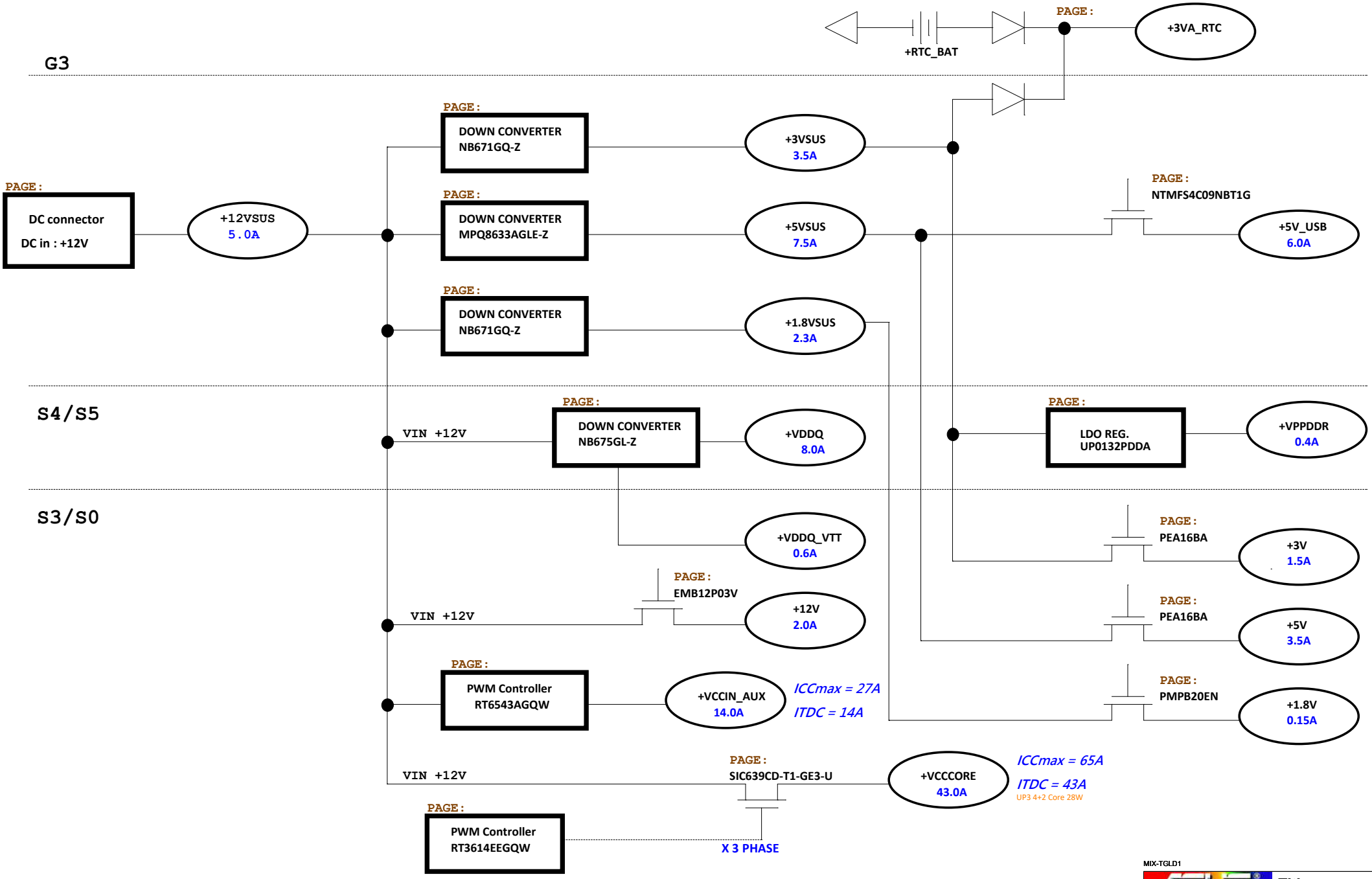






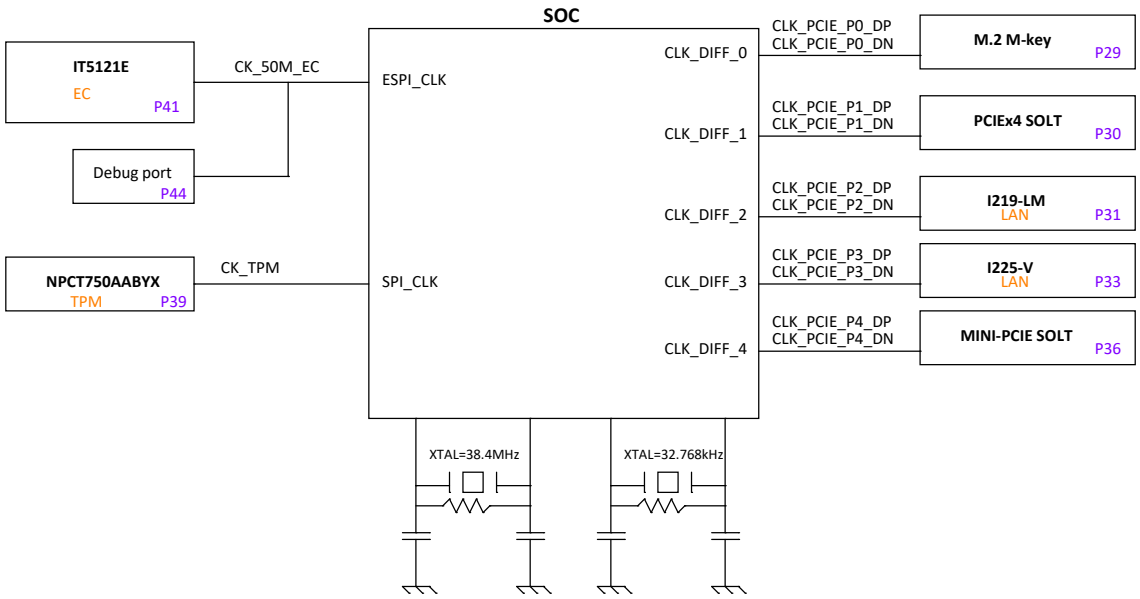
MIX-TGLD1

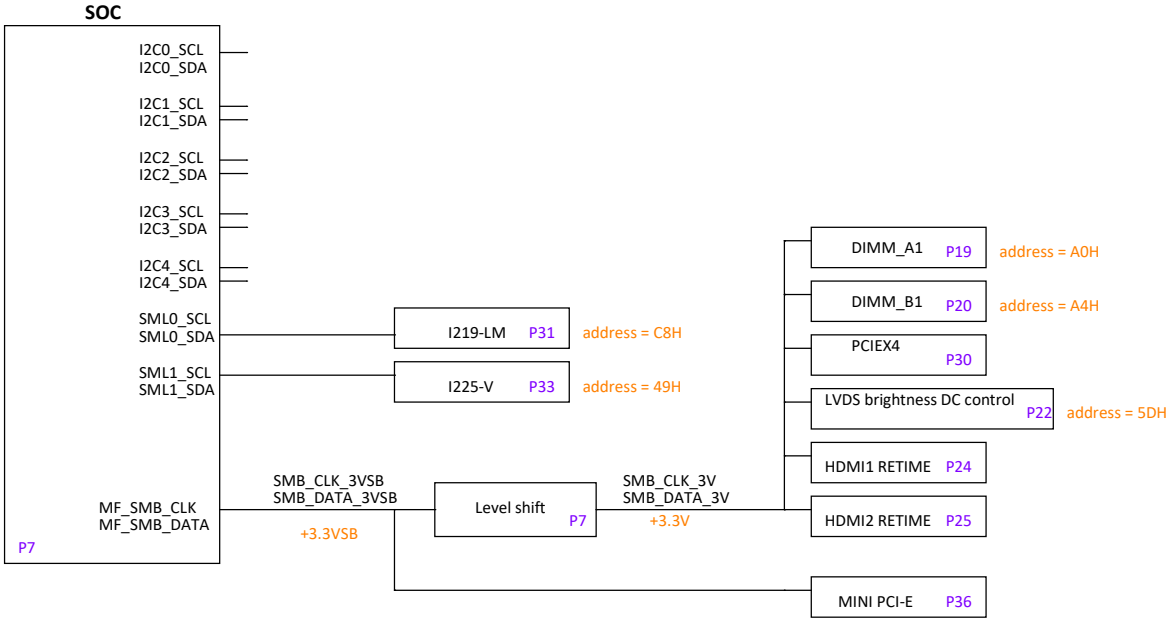
ASUSTek COMPUTER INC.	Title : POWER SEQUENCE FLOW	
	Engineer: <OrgAddr1>	
Size: C	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 2 of 59	



MIX-TGLD1

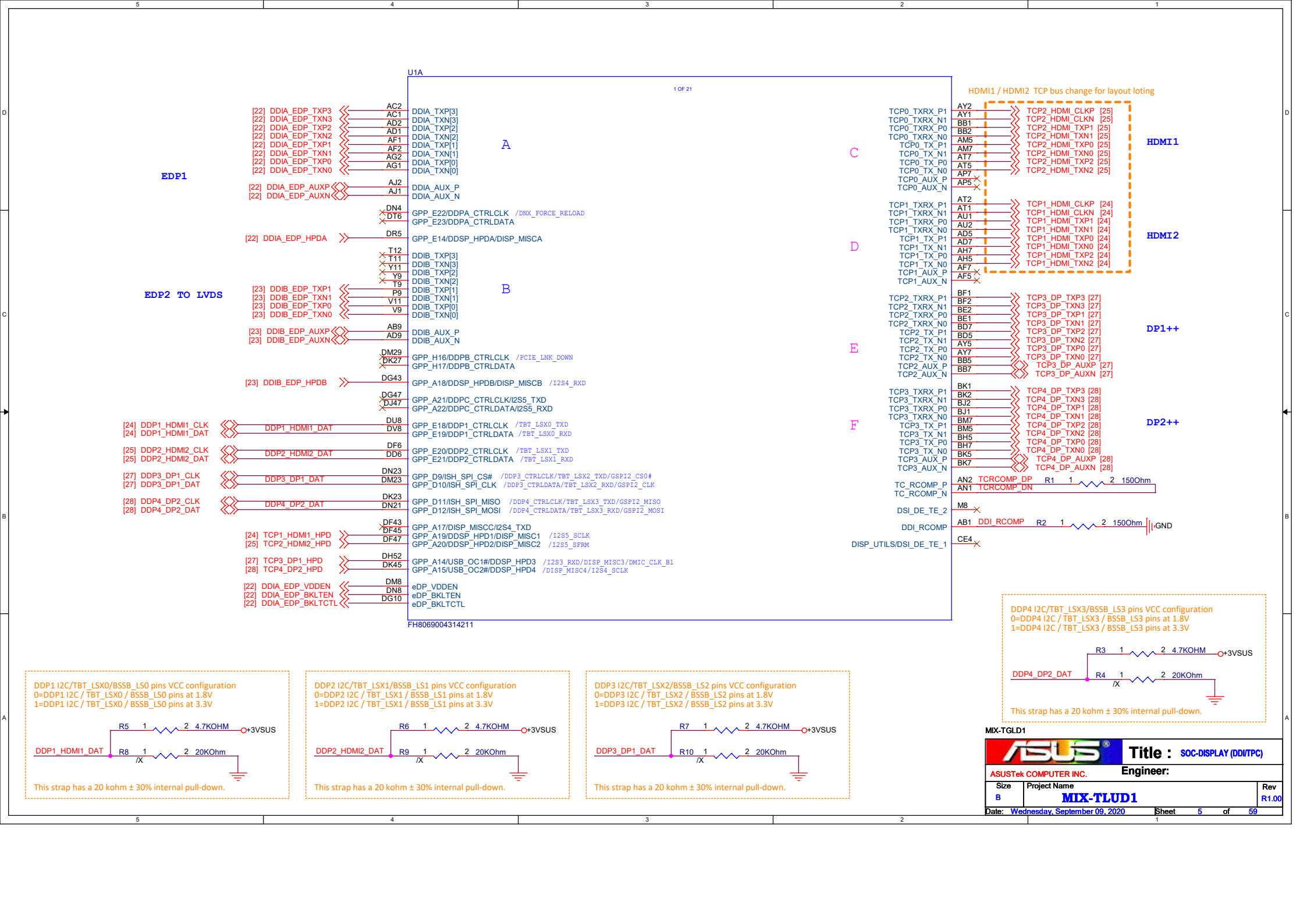
ASUSTEK COMPUTER INC	Title : POWER FLOW	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 3 of 59	



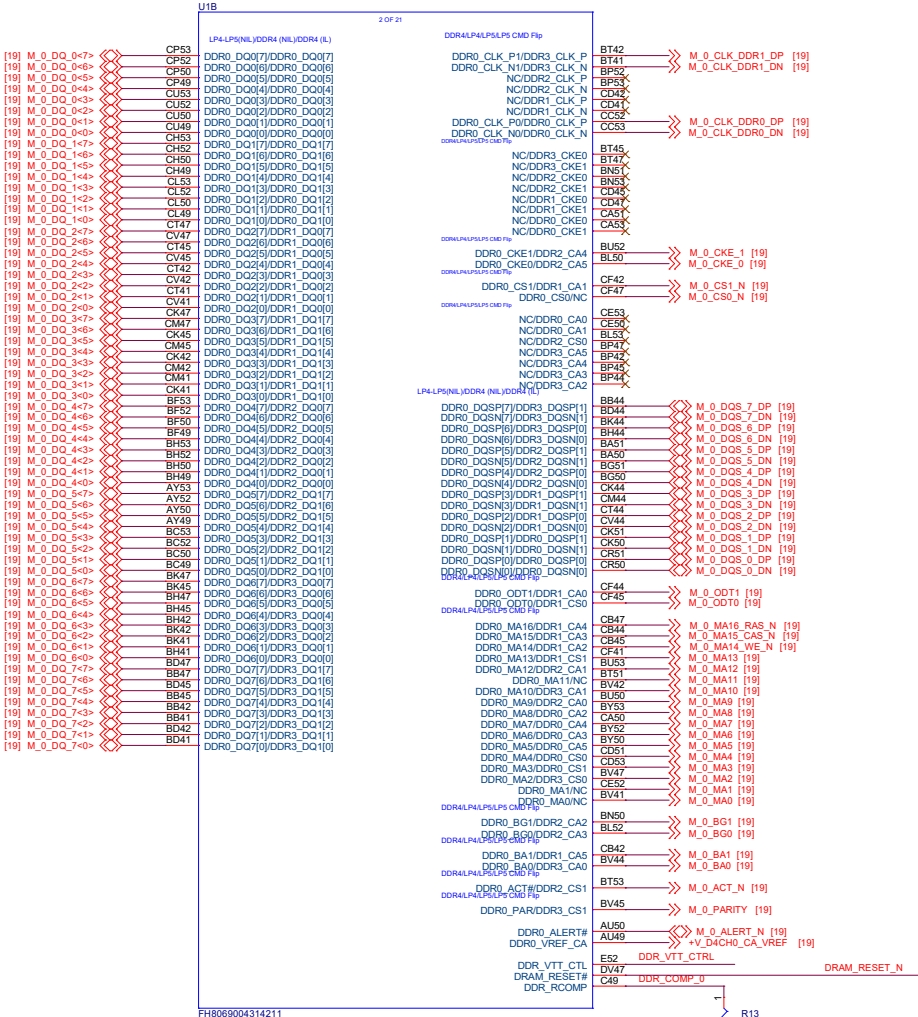


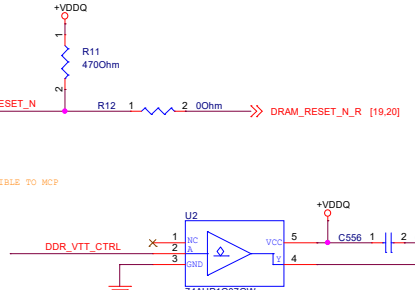
MIX-TGLD1

ASUSTek COMPUTER INC.	Title : CLK DISTRIBUTION	
	Engineer: <OrgAddr1>	
Size: A3	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 4 of 59	


U1A
1 OF 21
EDP1
EDP2 TO LVDS
A
B
C
D
E
F
DDIA_TXP[3]
DDIA_TXN[3]
DDIA_TXP[2]
DDIA_TXN[2]
DDIA_TXP[1]
DDIA_TXN[1]
DDIA_TXP[0]
DDIA_TXN[0]
DDIA_AUX_P
DDIA_AUX_N
GPP_E22/DDPA_CTRLCLK /DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA
GPP_E14/DDSP_HPDA/DISP_MISCA
DDIB_TXP[3]
DDIB_TXN[3]
DDIB_TXP[2]
DDIB_TXN[2]
DDIB_TXP[1]
DDIB_TXN[1]
DDIB_TXP[0]
DDIB_TXN[0]
DDIB_AUX_P
DDIB_AUX_N
GPP_H16/DDPB_CTRLCLK /PCIE_LNK_DOWN
GPP_H17/DDPB_CTRLDATA
GPP_A18/DDSP_HPDB/DISP_MISCB /I2S4_RXD
GPP_A21/DDPC_CTRLCLK/I2S5_TXD
GPP_A22/DDPC_CTRLDATA/I2S5_RXD
GPP_E18/DDP1_CTRLCLK /TBT_LSX0_TXD
GPP_E19/DDP1_CTRLDATA /TBT_LSX0_RXD
GPP_E20/DDP2_CTRLCLK /TBT_LSX1_TXD
GPP_E21/DDP2_CTRLDATA /TBT_LSX1_RXD
GPP_D9/ISH_SPI_CS# /DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK /DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK
GPP_D11/ISH_SPI_MISO /DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI /DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI
GPP_A17/DISP_MISCC/I2S4_TXD
GPP_A19/DDSP_HPD1/DISP_MISC1 /I2S5_SCLK
GPP_A20/DDSP_HPD2/DISP_MISC2 /I2S5_SFRM
GPP_A14/USB_OC1#/DDSP_HPD3 /I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
GPP_A15/USB_OC2#/DDSP_HPD4 /DISP_MISC4/I2S4_SCLK
eDP_VDDEN
eDP_BKLTEN
eDP_BKLTCTL
HDMI1 / HDMI2 TCP bus change for layout loting
HDMI1
HDMI2
DP1++
DP2++
TCP0_TXRX_P1
TCP0_TXRX_N1
TCP0_TXRX_P0
TCP0_TXRX_N0
TCP0_TX_P1
TCP0_TX_N1
TCP0_TX_P0
TCP0_TX_N0
TCP0_AUX_P
TCP0_AUX_N
TCP2_HDMI_CLKP [25]
TCP2_HDMI_CLKN [25]
TCP2_HDMI_TXP1 [25]
TCP2_HDMI_TXN1 [25]
TCP2_HDMI_TXP0 [25]
TCP2_HDMI_TXN0 [25]
TCP2_HDMI_TXP2 [25]
TCP2_HDMI_TXN2 [25]
TCP1_TXRX_P1
TCP1_TXRX_N1
TCP1_TXRX_P0
TCP1_TXRX_N0
TCP1_TX_P1
TCP1_TX_N1
TCP1_TX_P0
TCP1_TX_N0
TCP1_AUX_P
TCP1_AUX_N
TCP1_HDMI_CLKP [24]
TCP1_HDMI_CLKN [24]
TCP1_HDMI_TXP1 [24]
TCP1_HDMI_TXN1 [24]
TCP1_HDMI_TXP0 [24]
TCP1_HDMI_TXN0 [24]
TCP1_HDMI_TXP2 [24]
TCP1_HDMI_TXN2 [24]
TCP2_TXRX_P1
TCP2_TXRX_N1
TCP2_TXRX_P0
TCP2_TXRX_N0
TCP2_TX_P1
TCP2_TX_N1
TCP2_TX_P0
TCP2_TX_N0
TCP2_AUX_P
TCP2_AUX_N
TCP3_DP_TXP3 [27]
TCP3_DP_TXN3 [27]
TCP3_DP_TXP1 [27]
TCP3_DP_TXN1 [27]
TCP3_DP_TXP2 [27]
TCP3_DP_TXN2 [27]
TCP3_DP_TXP0 [27]
TCP3_DP_TXN0 [27]
TCP3_DP_AUXP [27]
TCP3_DP_AUXN [27]
TCP3_TXRX_P1
TCP3_TXRX_N1
TCP3_TXRX_P0
TCP3_TXRX_N0
TCP3_TX_P1
TCP3_TX_N1
TCP3_TX_P0
TCP3_TX_N0
TCP3_AUX_P
TCP3_AUX_N
TCP4_DP_TXP3 [28]
TCP4_DP_TXN3 [28]
TCP4_DP_TXP1 [28]
TCP4_DP_TXN1 [28]
TCP4_DP_TXP2 [28]
TCP4_DP_TXN2 [28]
TCP4_DP_TXP0 [28]
TCP4_DP_TXN0 [28]
TCP4_DP_AUXP [28]
TCP4_DP_AUXN [28]
TC_RCOMP_P
TC_RCOMP_N
TCRCOMP_DP
TCRCOMP_DN
150Ohm
DSI_DE_TE_2
DDI_RCOMP
DDI_RCOMP
150Ohm
GND
DISP_UTILS/DSI_DE_TE_1
[22] DDIA_EDP_TXP3
[22] DDIA_EDP_TXN3
[22] DDIA_EDP_TXP2
[22] DDIA_EDP_TXN2
[22] DDIA_EDP_TXP1
[22] DDIA_EDP_TXN1
[22] DDIA_EDP_TXP0
[22] DDIA_EDP_TXN0
[22] DDIA_EDP_AUXP
[22] DDIA_EDP_AUXN
[22] DDIA_EDP_HPDA
[23] DDIB_EDP_TXP1
[23] DDIB_EDP_TXN1
[23] DDIB_EDP_TXP0
[23] DDIB_EDP_TXN0
[23] DDIB_EDP_AUXP
[23] DDIB_EDP_AUXN
[23] DDIB_EDP_HPDB
[24] DDP1_HDMI1_CLK
[24] DDP1_HDMI1_DAT
DDP1_HDMI1_DAT
[25] DDP2_HDMI2_CLK
[25] DDP2_HDMI2_DAT
DDP2_HDMI2_DAT
[27] DDP3_DP1_CLK
[27] DDP3_DP1_DAT
DDP3_DP1_DAT
[28] DDP4_DP2_CLK
[28] DDP4_DP2_DAT
DDP4_DP2_DAT
[24] TCP1_HDMI1_HPD
[25] TCP2_HDMI2_HPD
[27] TCP3_DP1_HPD
[28] TCP4_DP2_HPD
[22] DDIA_EDP_VDDEN
[22] DDIA_EDP_BKLTEN
[22] DDIA_EDP_BKLTCTL
FH8069004314211
DDP1 I2C/TBT_LSX0/BSSB_LS0 pins VCC configuration
0=DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V
1=DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V
R5 4.7KOHM +3VSUS
R8 20KOhm /X
This strap has a 20 kohm ± 30% internal pull-down.
DDP2 I2C/TBT_LSX1/BSSB_LS1 pins VCC configuration
0=DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8V
1=DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3V
R6 4.7KOHM +3VSUS
R9 20KOhm /X
This strap has a 20 kohm ± 30% internal pull-down.
DDP3 I2C/TBT_LSX2/BSSB_LS2 pins VCC configuration
0=DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8V
1=DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3V
R7 4.7KOHM +3VSUS
R10 20KOhm /X
This strap has a 20 kohm ± 30% internal pull-down.
DDP4 I2C/TBT_LSX3/BSSB_LS3 pins VCC configuration
0=DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 1.8V
1=DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 3.3V
R3 4.7KOHM +3VSUS
R4 20KOhm /X
This strap has a 20 kohm ± 30% internal pull-down.
MIX-TGLD1
Title : SOC-DISPLAY (DDI/TPC)
ASUSTek COMPUTER INC.
Engineer:
Size B
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
Sheet 5 of 59

TGL-U - MEMORY CHANNEL - A





TGL-U - MEMORY CHANNEL - B

MIX-TGLD1

ASUSTek COMPUTER INC.	Title : SOC-MEMORY (CHA/CHB)	
	Engineer:	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 6 of 59	

External pull-up is required. Recommend 4.7 kohm pull up.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling

+3VSUS — R28 1 — 2 4.7KOhm — SPI0_MOSI

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite

+3VSUS — R29 1 — 2 100KOhm — SPI0_IO2

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite

+3VSUS — R30 1 — 2 100KOhm — SPI0_IO3

JTAG ODT Disable
External pull-up is recommended
0=JTAG ODT is disabled
1=JTAG ODT is enabled

R43 2 /X 1 100KOhm +3VSUS
R45 2 /X 1 100KOhm +1.8VSUS
GPP_E6 — R48 1 /X 2 4.7KOHM

This strap does not have an internal pull-up or pull-down

TLS CONFIDENTIALITY
0=>Disable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1=>Enable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support IntelR AMT with TLS.

R1101 1 /X 2 4.7KOHM +3VSUS
R46 1 /X 2 4.7KOHM +1.8VSUS
SMB_ALERT_N — R49 1 /X 2 4.7KOHM

The strap has a 20 kohm ± 30% internal pull-up

CPUNSSC CLOCK FREQ
This strap has a 20 kohm ± 30% internal pull-up.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)

R44 1 /X 2 4.7KOHM +3VSUS
R47 1 /X 2 4.7KOHM +1.8VSUS
SML1ALERT_N — R50 1 /X 2 20KOhm

The strap has a 20 kohm ± 30% internal pull-up

Flash/TPM

Close to device

[39,44] SPI0_BIOS_TPM_CLK — R19 2 — 1 5.1OHM — SPI0_CLK — DJ37
[44] SPI0_BIOS_TPM_IO3 — R15 2 — 1 5.1OHM — SPI0_IO3 — DG35
[44] SPI0_BIOS_TPM_IO2 — R16 2 — 1 5.1OHM — SPI0_IO2 — DJ39
[39,44] SPI0_BIOS_TPM_MISO — R20 2 — 1 5.1OHM — SPI0_MISO — DJ33
[39,44] SPI0_BIOS_TPM_MOSI — R17 2 — 1 5.1OHM — SPI0_MOSI — DJ35
[44] SPI0_BIOS_TPM_CS0_N — R1048 2 — 1 5.1OHM — SPI0_CS0_N — DF35
[39] SPI0_BIOS_TPM_CS2_N — R1047 2 — 1 5.1OHM — SPI0_CS2_N — DG37
DF39

U1E — 5 OF 21

SPI0_CLK
SPI0_IO3
SPI0_IO2
SPI0_MISO
SPI0_MOSI
SPI0_CS1#
SPI0_CS0#
SPI0_CS2#

DJ6 GPP_E11/THC0_SPI1_CLK
DN5 GPP_E2/THC0_SPI1_IO3
DR9 GPP_E1/THC0_SPI1_IO2
DM6 GPP_E12/THC0_SPI1_IO1
DK6 GPP_E13/THC0_SPI1_IO0
DK8 GPP_E10/THC0_SPI1_CS#
SATA_LED_N — DV11 GPP_E8/SATA_LED#
GPP_E6 — DW9 GPP_E17/THC0_SPI1_INT#
DT8 GPP_E6/THC0_SPI1_RST#

DN15 GPP_F11/THC1_SPI2_CLK
DK13 GPP_F15/GSXSRESET# /THC1_SPI2_IO3
DM13 GPP_F14/GSXDIN/THC1_SPI2_IO2
DN13 GPP_F13/GSXSLOAD/THC1_SPI2_IO1
DJ15 GPP_F12/GSXDOUT/THC1_SPI2_IO0
DK15 GPP_F16/GSXCLK/THC1_SPI2_CS#
DN10 GPP_F18/THC1_SPI2_INT#
DV14 GPP_F17/THC1_SPI2_RST#

DH3 CL_CLK
DH4 CL_DATA
DF2 CL_RST#

FH8069004314211

GPP_C0/SMBCLK — DK21 SMB_CLK_3VSB — SMB_CLK_3VSB [36]
GPP_C1/SMBDATA — DM19 SMB_DATA_3VSB — SMB_DATA_3VSB [36]
GPP_C2/SMBALERT# — DN19 SMB_ALERT_N

GPP_C3/SML0CLK — DK19 SML0_CLK — SML0_CLK [31]
GPP_C4/SML0DATA — DM17 SML0_DATA — SML0_DATA [31]
GPP_C5/SML0ALERT# — DN17 SML0ALERT_N

GPP_C6/SML1CLK — DK17 SML1_CLK — SML1_CLK [33]
GPP_C7/SML1DATA — DJ17 SML1_DATA — SML1_DATA [33]
GPP_B23/ SML1ALERT#/PCHHOT#/GSPI1_CS1# — CY50 SML1ALERT_N

EC / Debug

GPP_A5/ESPI_CLK — DN53 ESPI_SOC_CLK — R221 2 — 49.9Ohm — ESPI_CLK [41,44]
GPP_A3/ESPI_IO3/SUSACK# — DJ53 ESPI_SOC_IO3 — R231 2 — 15Ohm — ESPI_IO3 [41,44]
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK — DH50 ESPI_SOC_IO2 — R241 2 — 15Ohm — ESPI_IO2 [41,44]
GPP_A1/ESPI_IO1 — DP50 ESPI_SOC_IO1 — R251 2 — 15Ohm — ESPI_IO1 [41,44]
GPP_A0/ESPI_IO0 — DP52 ESPI_SOC_IO0 — R261 2 — 15Ohm — ESPI_IO0 [41,44]
GPP_A4/ESPI_CS# — DK52 — ESPI_CS_N [41,44]
GPP_A6/ESPI_RESET# — DL50 — ESPI_RESET_N [41,44]

+3VSUS

SML1_CLK — R1088 2 — 1 499OHM /X
SML1_DATA — R1087 2 — 1 499OHM /X
SML0_CLK — R1012 2 — 1 499OHM
SML0_DATA — R1011 2 — 1 499OHM

SPI0_CLK — R1100 2 — 1 100KOhm

SMBus level shift
+3.3VSB <-> +3.3V

+3VSUS — R32 1 — 2 1KOhm — SMB_CLK_3VSB
R31 1 /X 2 0Ohm
Q1 2N7002-L
R33 1 — 2 1KOhm — +3V
SMB_CLK_3V [19,20,23,24,25,30]

+3VSUS — R36 1 — 2 1KOhm — SMB_DATA_3VSB
Q2 2N7002-L
+3V
R37 1 — 2 1KOhm — +3V
SMB_DATA_3V [19,20,23,24,25,30]
R39 1 /X 2 0Ohm

+5V
+3V — R38 10KOhm — SATA_LED_N
+5V — R35 10KOhm
Q3B UM6K1N
R34 10KOhm
Q3A UM6K1N
SOC_SATA_LED_N [45]

This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled
0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved

R40 1 /X 2 4.7KOHM +3VSUS
R41 1 /X 2 4.7KOHM +1.8VSUS
SML0ALERT_N — R42 1 /X 2 20KOhm

The strap has a 20 kohm ± 30% internal pull-up

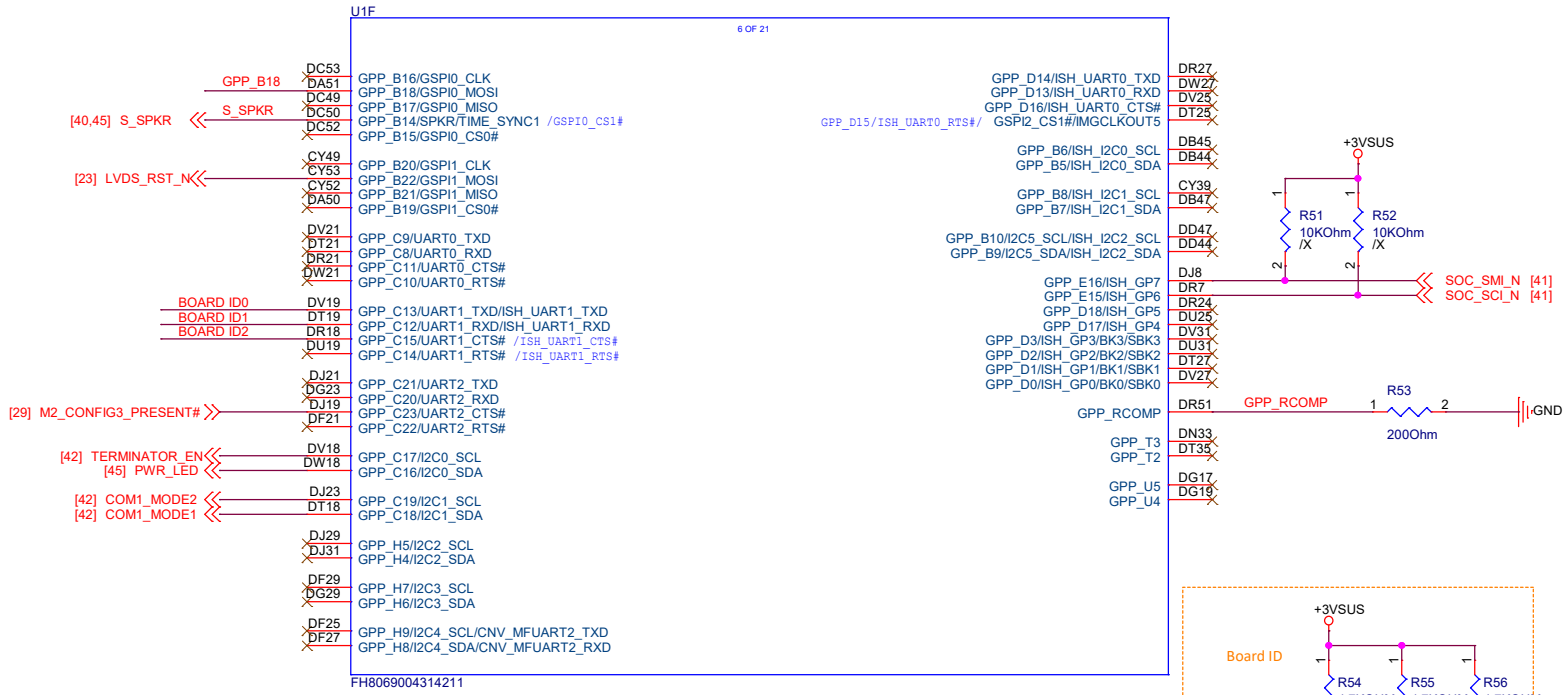
MIX-TGLD1

ASUSTek COMPUTER INC.

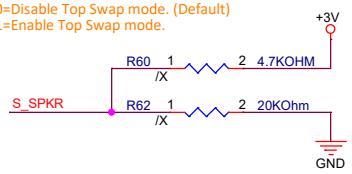
Title : SOC-ESPI/SPI/SMBUS
Engineer:

Size	Project Name	Rev
Custom	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 7 of 59

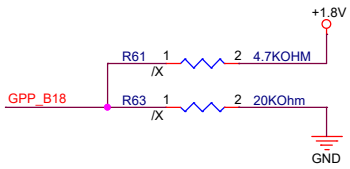


Top Swap Override
This inverts an address on access to SPI and firmware hub
0=Disable Top Swap mode. (Default)
1=Enable Top Swap mode.

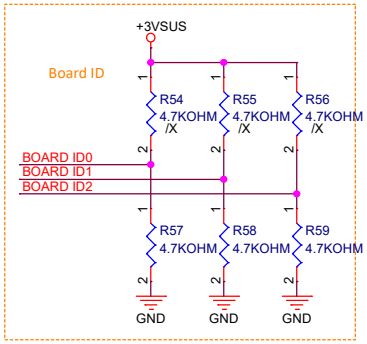


The strap has a 20 kohm ± 30% internal pull-down

NO REBOOT
0=>Disable "No Reboot" mode. (Default)
1=>Enable "No Reboot" mode (PCH will disable the TCO Timersystem reboot feature). This function is useful when running ITP/XDP.



The strap has a 20 kohm ± 30% internal pull-down



MIX-TGLD1

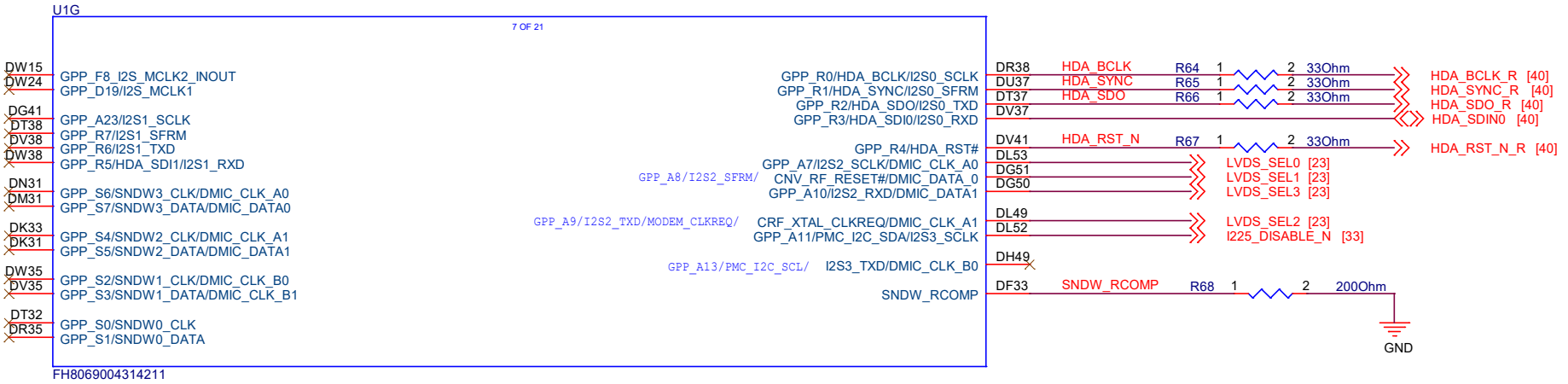
ASUSTek COMPUTER INC.

Title : SOC-GSPI/I2C/UART

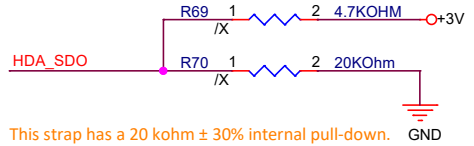
Engineer:

Size	Project Name	Rev
B	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 8 of 59



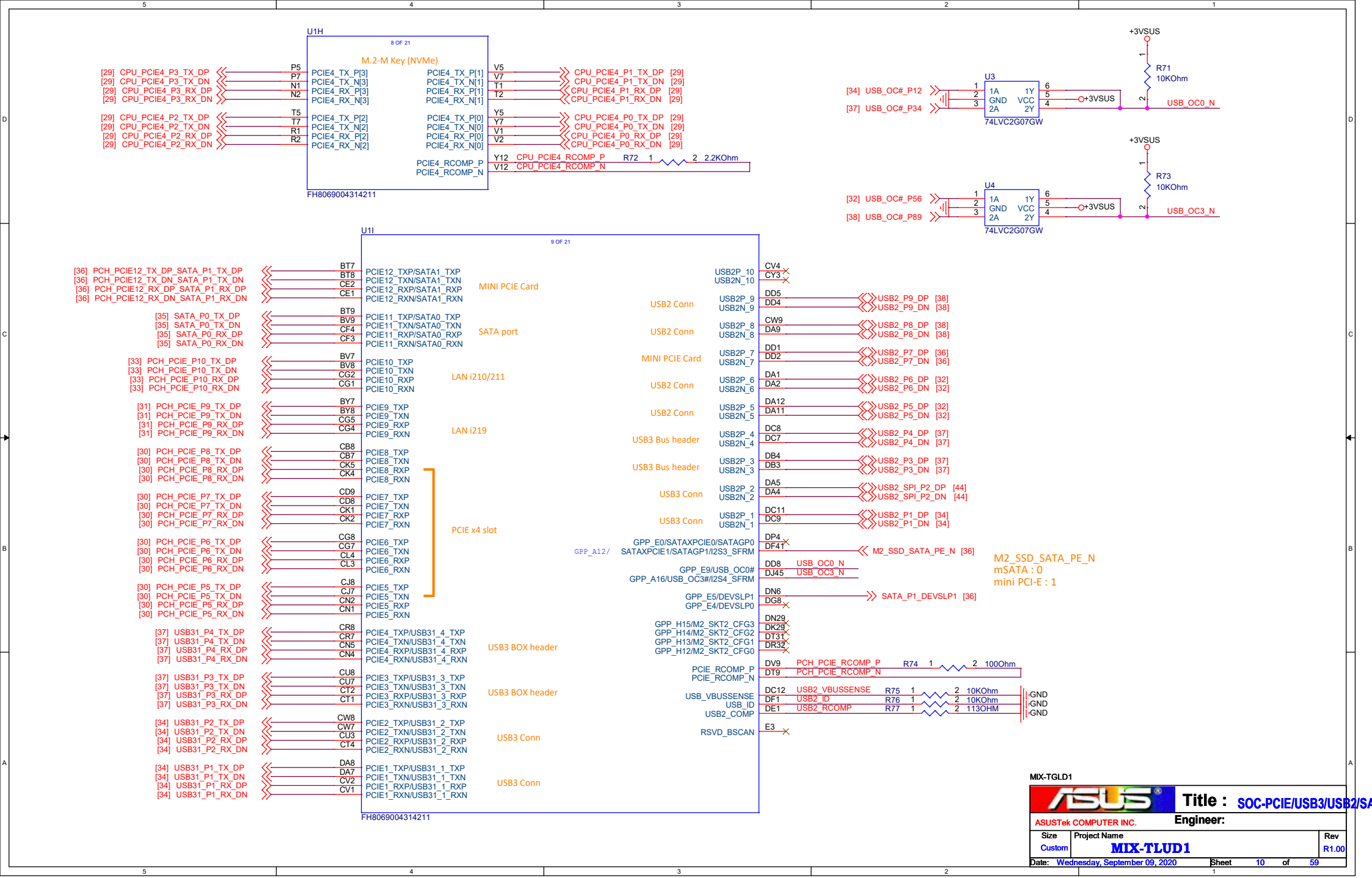
FLASH DESCRIPTOR SECURITY OVERRIDE
0=> Enable security measures defined in the Flash Descriptor.(Default)
1=> Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY



This strap has a 20 kohm ± 30% internal pull-down.

MIX-TGLD1

ASUSTek COMPUTER INC.	Title : SOC-I2S/HDA	
	Engineer:	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 9 of 59	



MIX-TGLD1

ASUSTek COMPUTER INC.	Title : SOC-PCIE/USB3/USB2/SA	
	Engineer:	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 10 of 59	

U1J

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D22	CSI_F_DP[1]	CNVi_WT_D1P	DK47
B22	CSI_F_DN[1]	CNVi_WT_D1N	DM47
E22	CSI_F_DP[0]	CNVi_WT_D0P	DN49
D20	CSI_F_DN[0]	CNVi_WT_D0N	DR49
A20	CSI_F_CLK_P	CNVi_WT_CLKP	DN45
B20	CSI_F_CLK_N	CNVi_WT_CLKN	DN47
B18	CSI_E_DP[1]/CSI_F_DP[2]	CNVi_WR_D1P	DU43
A18	CSI_E_DN[1]/CSI_F_DN[2]	CNVi_WR_D1N	DV43
D18	CSI_E_DP[0]/CSI_F_DP[3]	CNVi_WR_D0P	DR44
E18	CSI_E_DN[0]/CSI_F_DN[3]	CNVi_WR_D0N	DT43
C16	CSI_E_CLK_P	CNVi_WR_CLKP	DV44
D16	CSI_E_CLK_N	CNVi_WR_CLKN	DW44
D15	CSI_C_DP[2]	CNVi_WT_RCOMP	DN51
E15	CSI_C_DN[2]		
A15	CSI_C_DP[3]	GPP_F3/CNV_RGI_RSP/UART0_CTS#	DJ13
B15	CSI_C_DN[3]	GPP_F2/CNV_RGI_DT/UART0_TXD	DG13
L18	CSI_C_DP[1]	GPP_F1/CNV_BRI_RSP/UART0_RXD	DF15
N18	CSI_C_DN[1]	GPP_F0/CNV_BRI_DT/UART0_RTS#	DF17
L20	CSI_C_DP[0]	GPP_F5/ MODEM_CLKREQ/CRF_XTAL_CLKREQ	DJ10
N20	CSI_C_DN[0]	GPP_F6/CNV_PA_BLANKING	DV15
G20	CSI_C_CLK_P	GPP_F4/CNV_RF_RESET#	DK10
H20	CSI_C_CLK_N		
H16	CSI_B_DP[1]		
G16	CSI_B_DN[1]		
G18	CSI_B_DP[0]		
H18	CSI_B_DN[0]		
L16	CSI_B_CLK_P		
N16	CSI_B_CLK_N		
G14	CSI_B_DP[2]		
H14	CSI_B_DN[2]		
L14	CSI_B_DP[3]		
N14	CSI_B_DN[3]		
K14	CSI_RCOMP		
DK25	GPP_H23/IMGCLKOUT4		
DM25	GPP_H22/IMGCLKOUT3		
DN25	GPP_H21/IMGCLKOUT2		
DJ25	GPP_H20/IMGCLKOUT1		
DR30	GPP_D4/IMGCLKOUT_0/BK4/SBK4		

FH8069004314211

R78 CNVI_WT_RCOMP 1 2 150Ohm

GND

GPP_F2

GPP_F0

R79 2 1 150Ohm CSI_RCOMP

GND

M.2 CNVI MODES
A weak external pull-up is required.
0=Integrated CNVi enabled.
1=Integrated CNVi disabled.

R80 1 2 47KOhm +1.8VSUS

GPP_F2

R81 1 2 4.7KOHM /X

This strap does not have an internal pull-up or pull-down.

XTAL SEL1
This strap should not be pulled high since 24 MHz crystal is not supported on the PCH.
0 = 38.4 MHz (default)
1 = 24 MHz

R82 1 2 4.7KOHM /X +1.8VSUS

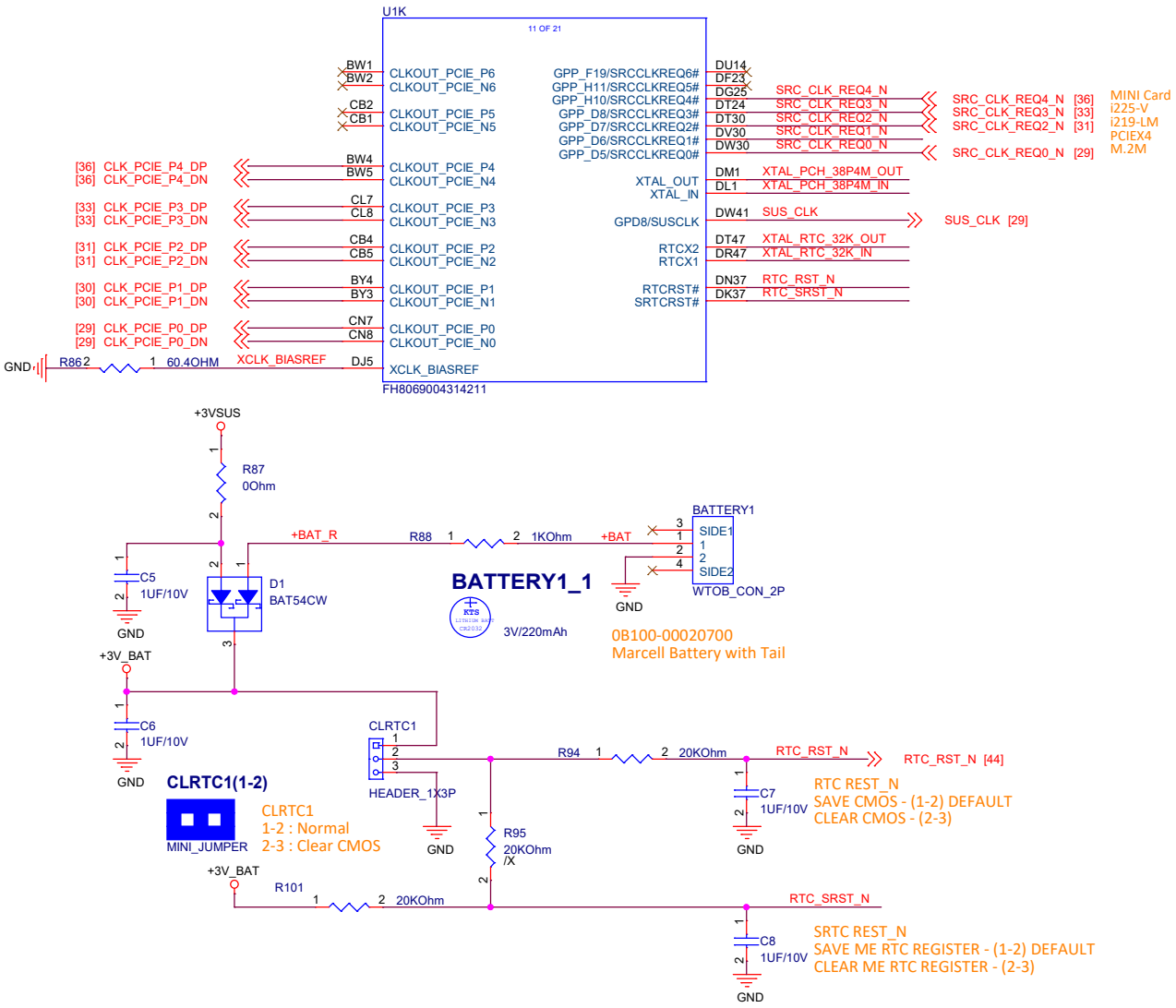
GPP_F0

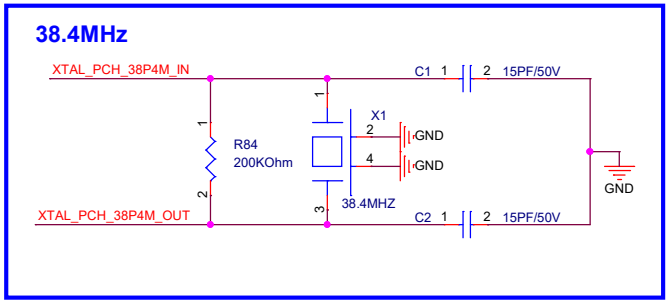
R83 1 2 20KOhm /X

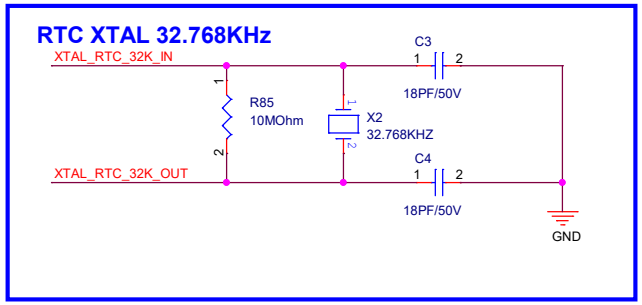
This strap has a 20 kohm ± 30% internal pull-down

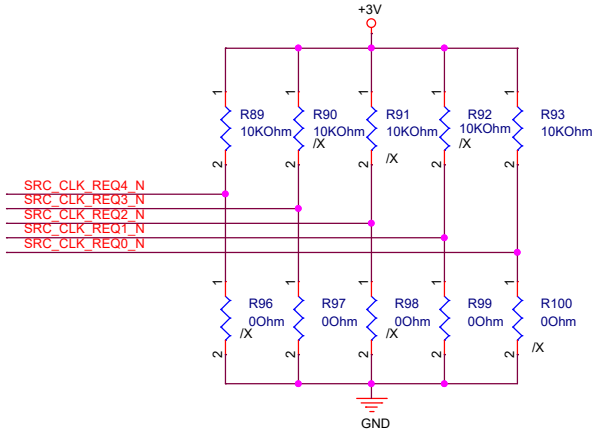
MIX-TGLD1

ASUSTek COMPUTER INC.	Title : SOC-CSI2/EMMC/CNVI	
	Engineer:	
Size: A	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 11 of 59	









MIX-TGLD1

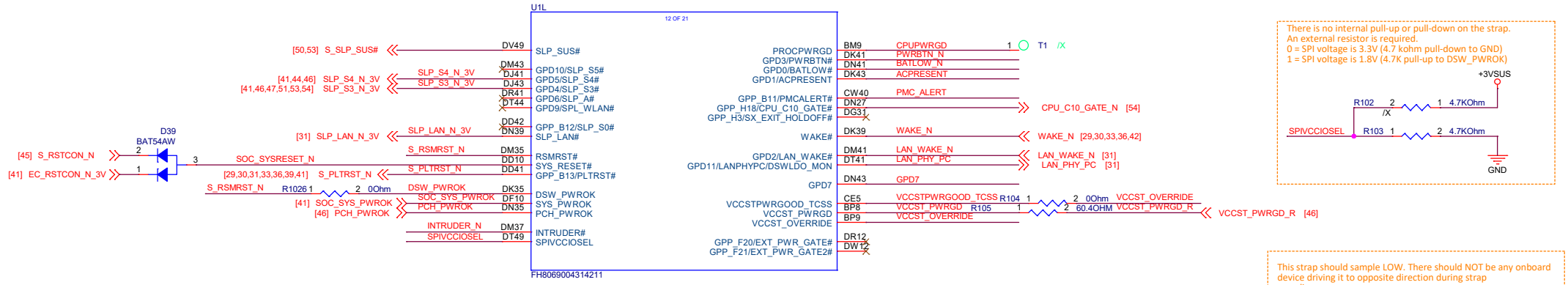
ASUSTek COMPUTER INC.

Title : SOC-CLOCK/SIGNALS/R

Engineer:

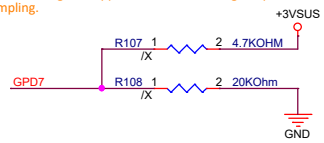
Size	Project Name	Rev
B	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 12 of 59



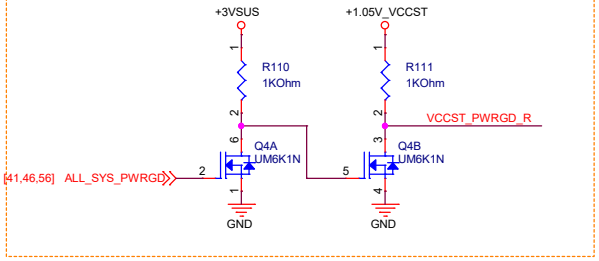
There is no internal pull-up or pull-down on the strap.
An external resistor is required.
0 = SPI voltage is 3.3V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWROK)

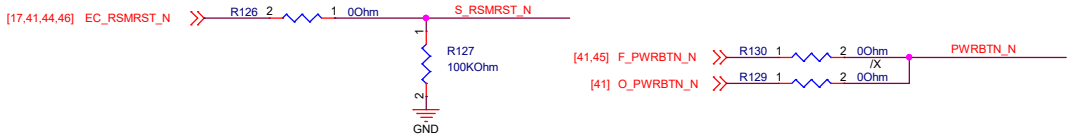
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.



This strap has a 20 kohm ± 30% internal pull-down

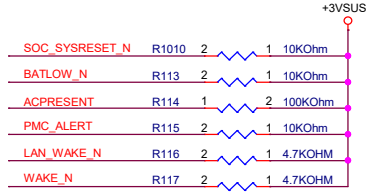
VCCST_PWRGD_LEVEL_SHIFTER

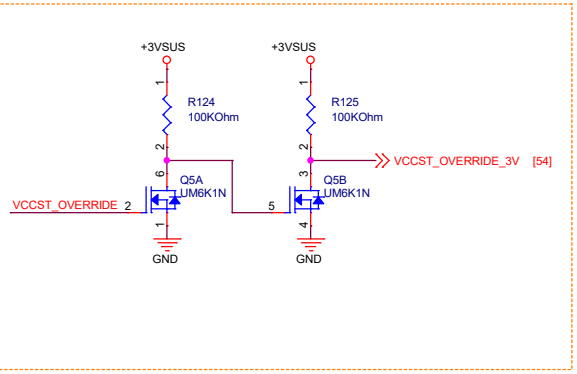




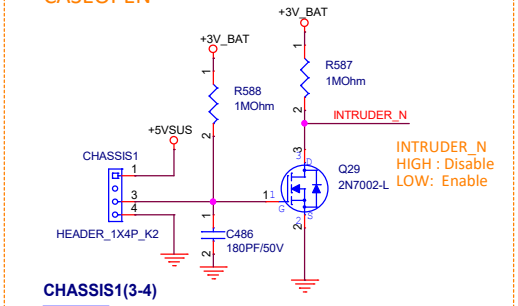
CPU SQ sample PN:

01001-01992900*	TIGER LAKE UP3 B-1 2c BGA 15 W V2 Celeron 48EU 4MB LP4x 3733 IPU 1VDB - Gen Embedded
01001-01993200	TIGER LAKE UP3 B-1 2c BGA 28 W T1 i3 48EU 6MB LP4x 3733 1VDB – Industrial: TCC/TSN, IBECC, Ext Temp
01001-01993500	TIGER LAKE UP3 B-1 2c BGA 28 W T1 i3 48EU 6MB LP4x 3733 IPU 1VDB - Gen Embedded
01001-01993100	TIGER LAKE UP3 B-1 4c BGA 28 W MS1 i5 80EU 8MB LP4x 4266 2VDB – Industrial: TCC/TSN, IBECC, Ext Temp, FSEDP
01001-01993400	TIGER LAKE UP3 B-1 4c BGA 28 W MS1 i5 80EU 8MB LP4x 4266 IPU 2VDB - Gen Embedded
01001-01993000	TIGER LAKE UP3 B-1 4c BGA 28 W MS3 i7 96EU 12MB LP4x 4266 2VDB - Industrial: TCC/TSN, IBECC, Ext Temp, FSEDP
01001-01993300	TIGER LAKE UP3 B-1 4c BGA 28 W MS3 i7 96EU 12MB LP4x 4266 IPU 2VDB-Gen Embedded

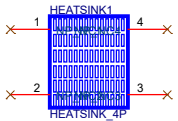


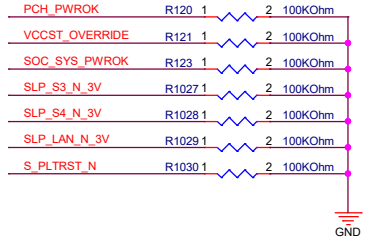


CASEOPEN



CPU HEATSINK(無風扇) for 15W CPU13071-02810000
CPU HEATSINK(有風扇) for 28W CPU13071-02620000





MIX-TGLD1

ASUSTek COMPUTER INC.	Title : SOC-PMU	
	Engineer:	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 13 of 59	

+VCORE

U1M

13 OF 21

+VCORE
Max : 65A

+VDDQ
Max : 1.5A

+VDDQ

U1O

15 OF 21

+VCCSTG_OUT

+VCCIO_OUT

+VCCSTG_OUT_LGC

+1.05V_VCCST

+1.05V_VCCST
Max : 0.5A

+VCCSTG

+VCCSTG
Max : 0.3A

SVID:
PLACE THE PU RESISTORS
CLOSE TO CPU

P_VRM_VDIO_10

P_VRM_CLK_10

P_VRM_ALERT_10

Place to CPU Primary Side

GND

FH8069004314211

MIX-TGLD1

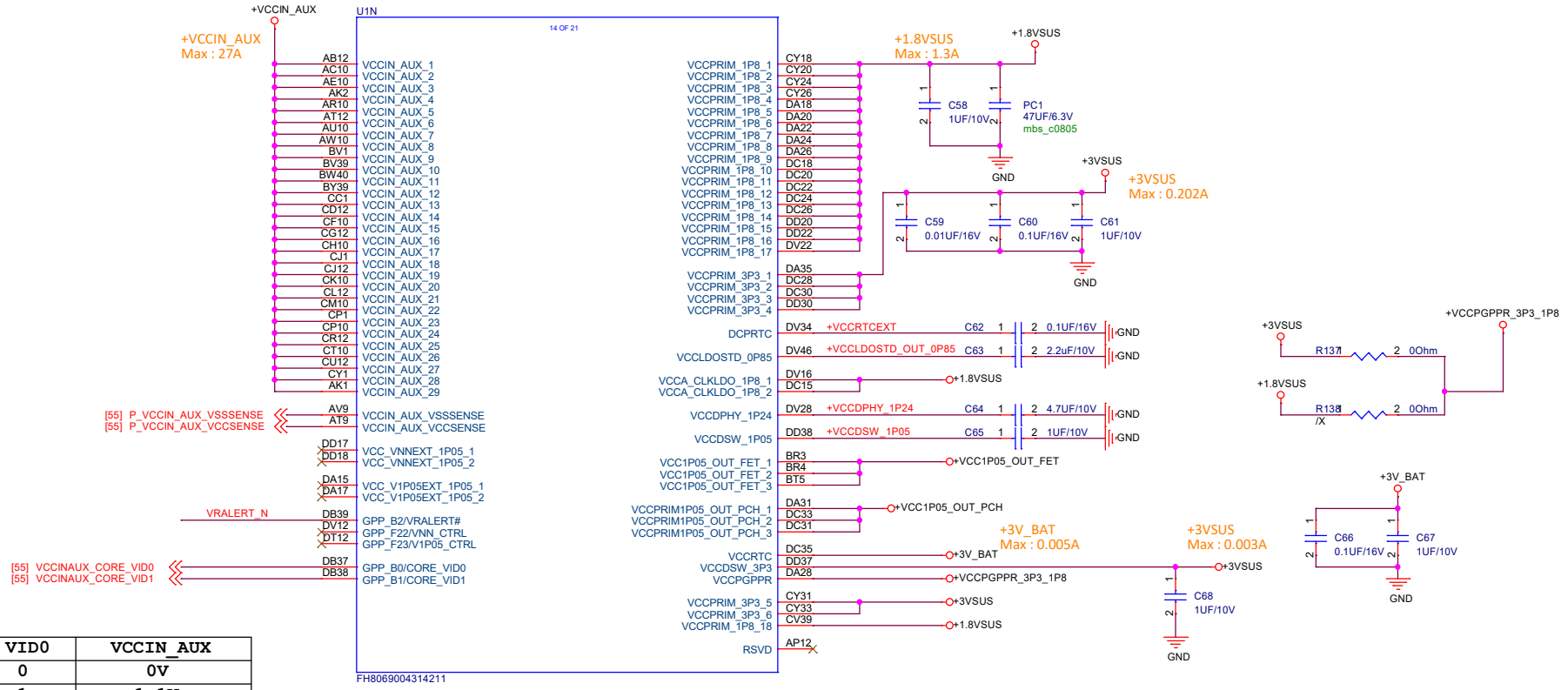
ASUSTek COMPUTER INC.

Title : SOC-CPU POWER

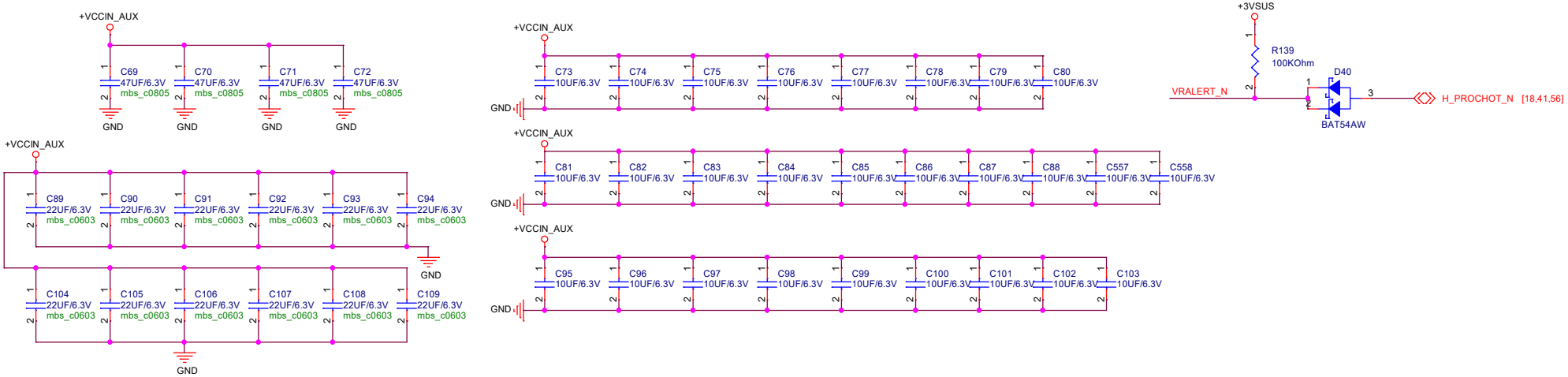
Engineer:

Size	Project Name	Rev
A3	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 14 of 59



VID1	VID0	VCCIN_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V



MIX-TGLD1

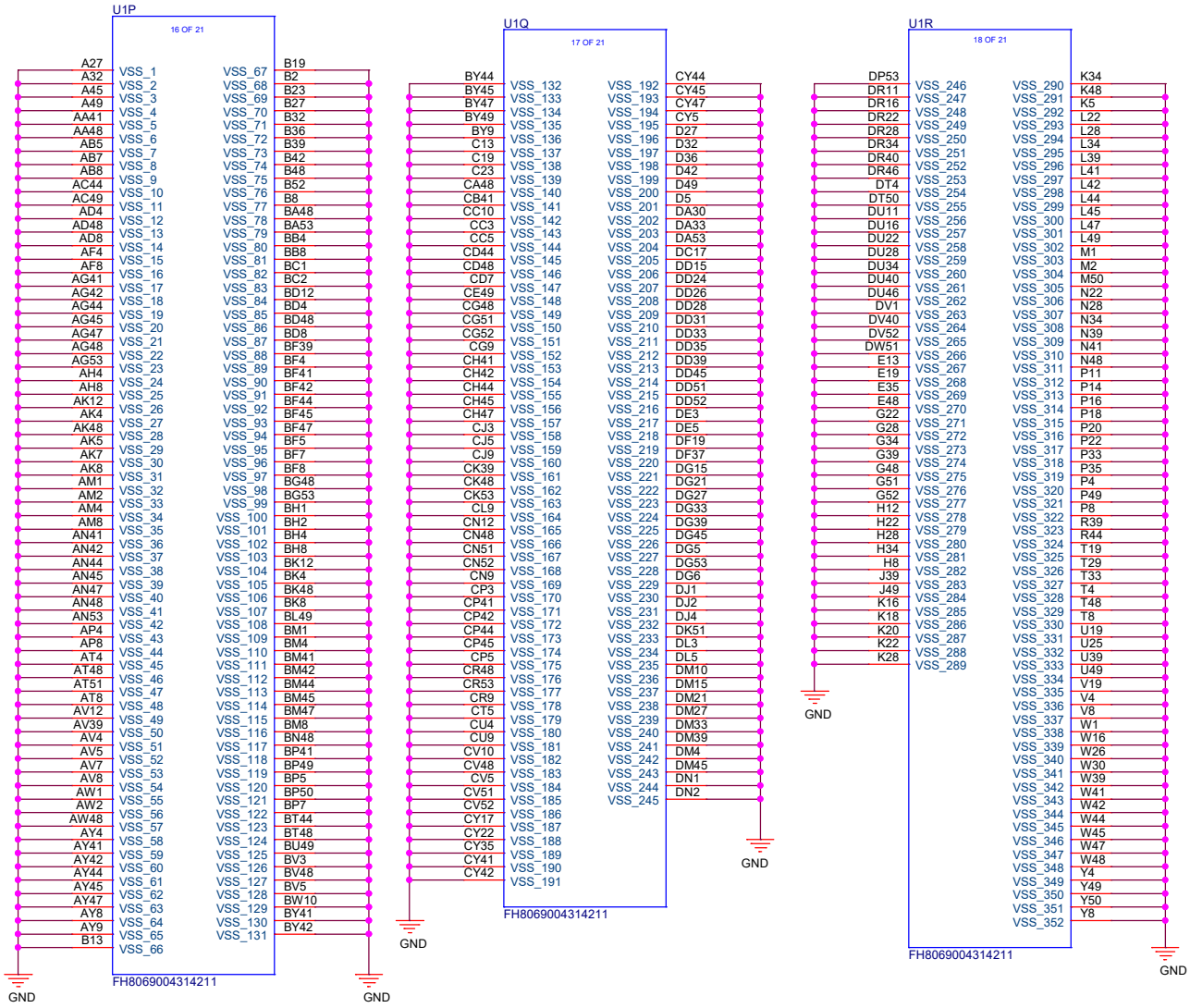
ASUSTek COMPUTER INC.

Title : SOC-PCH POWER

Engineer:

Size	Project Name	Rev
A3	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 15 of 59



MIX-TGLD1

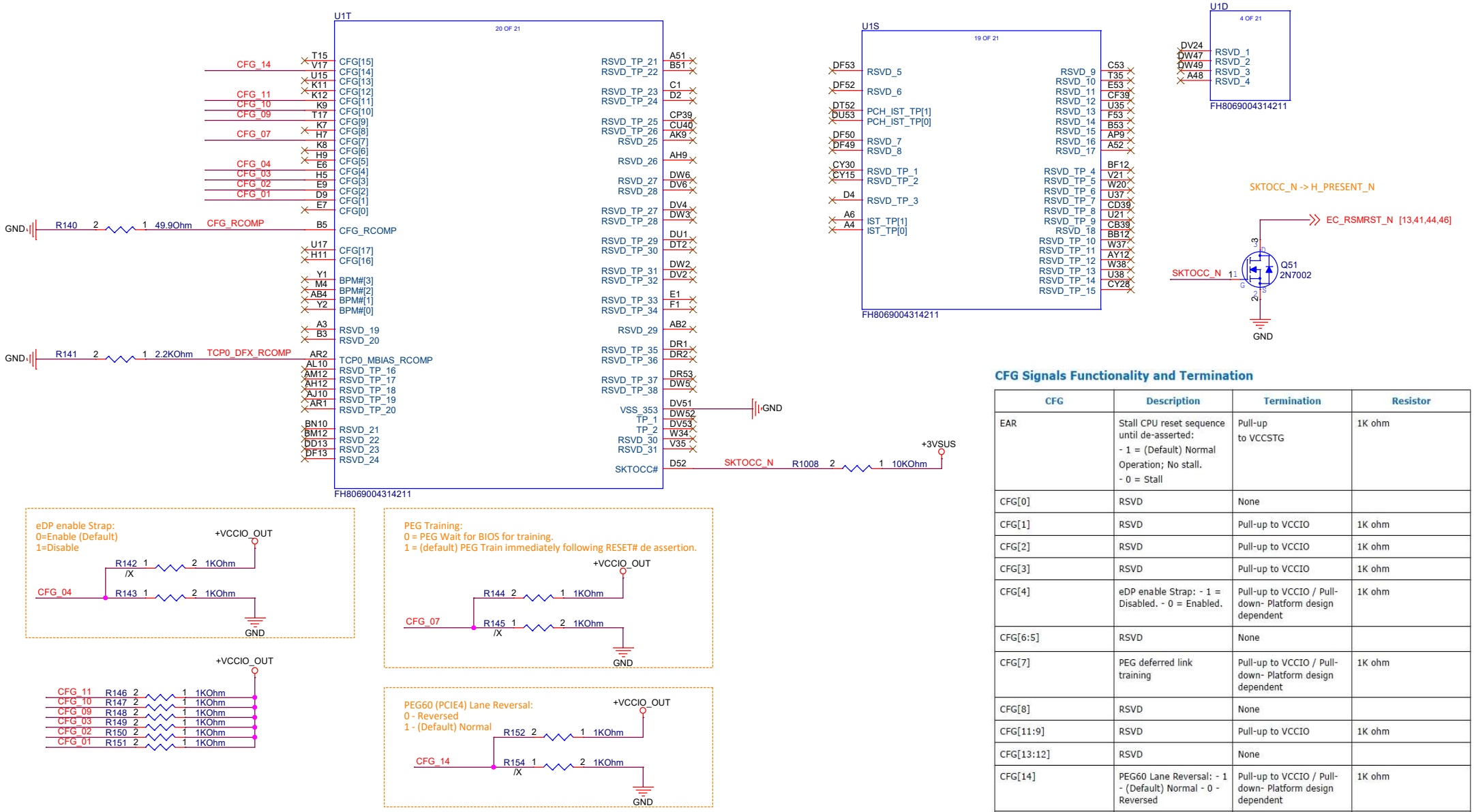
ASUSTek COMPUTER INC.

Title : SOC-GND

Engineer:

Size	Project Name	Rev
B	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 16 of 59



CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

MIX-TGLD1

ASUSTek COMPUTER INC.

Title : SOC-CFG/RSVD

Engineer:

Size	Project Name	Rev
B	MIX-TLUD1	R1.00

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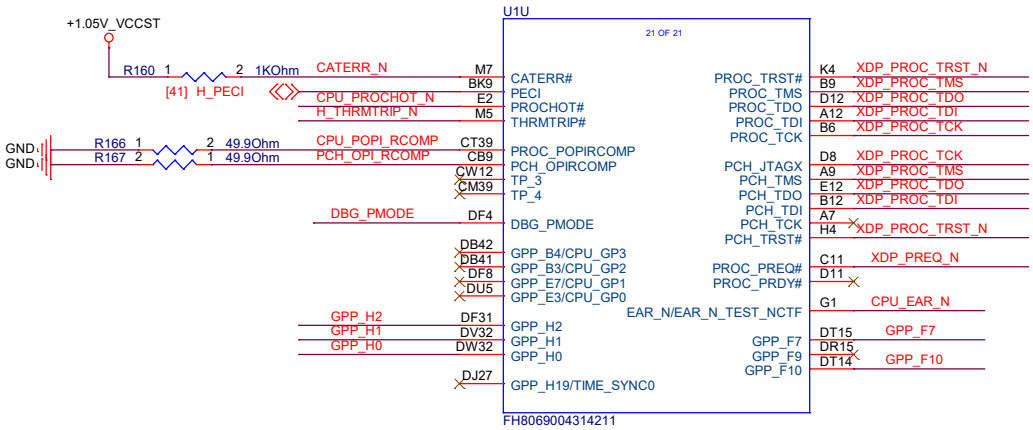
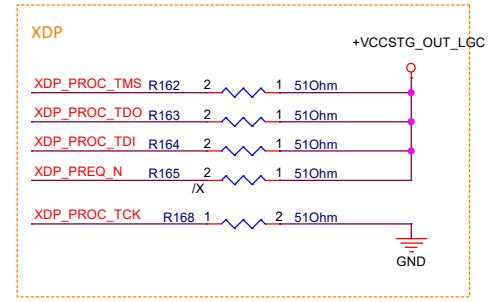
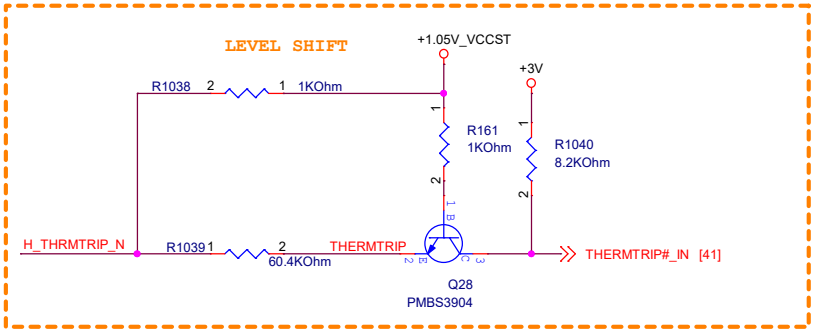
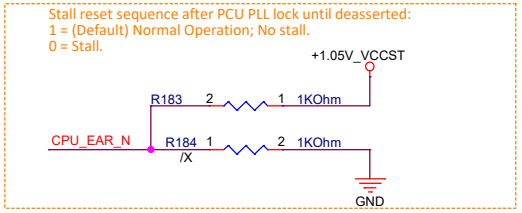
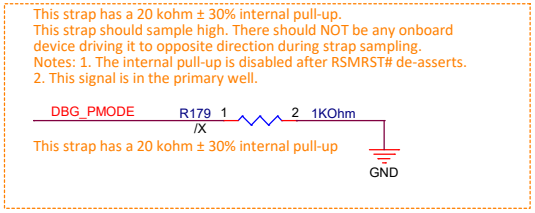
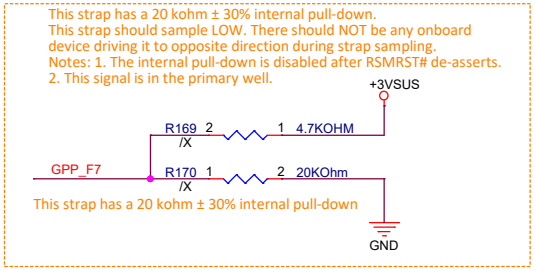


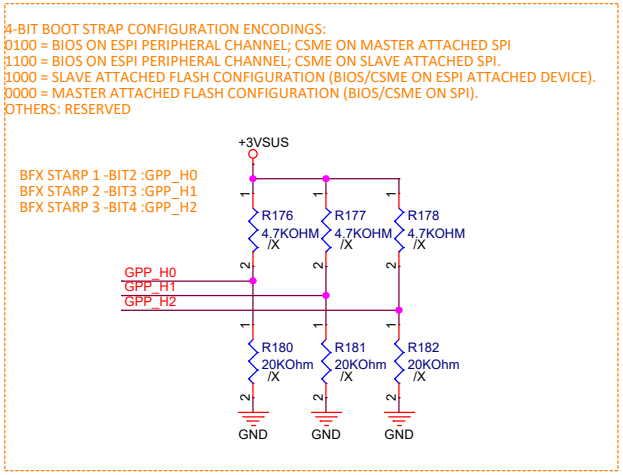


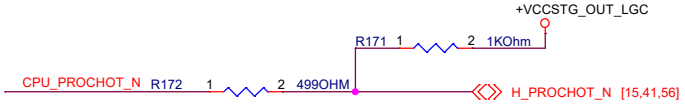


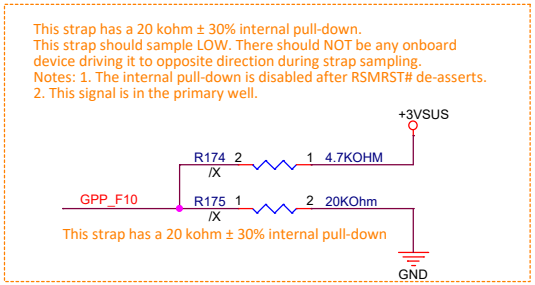








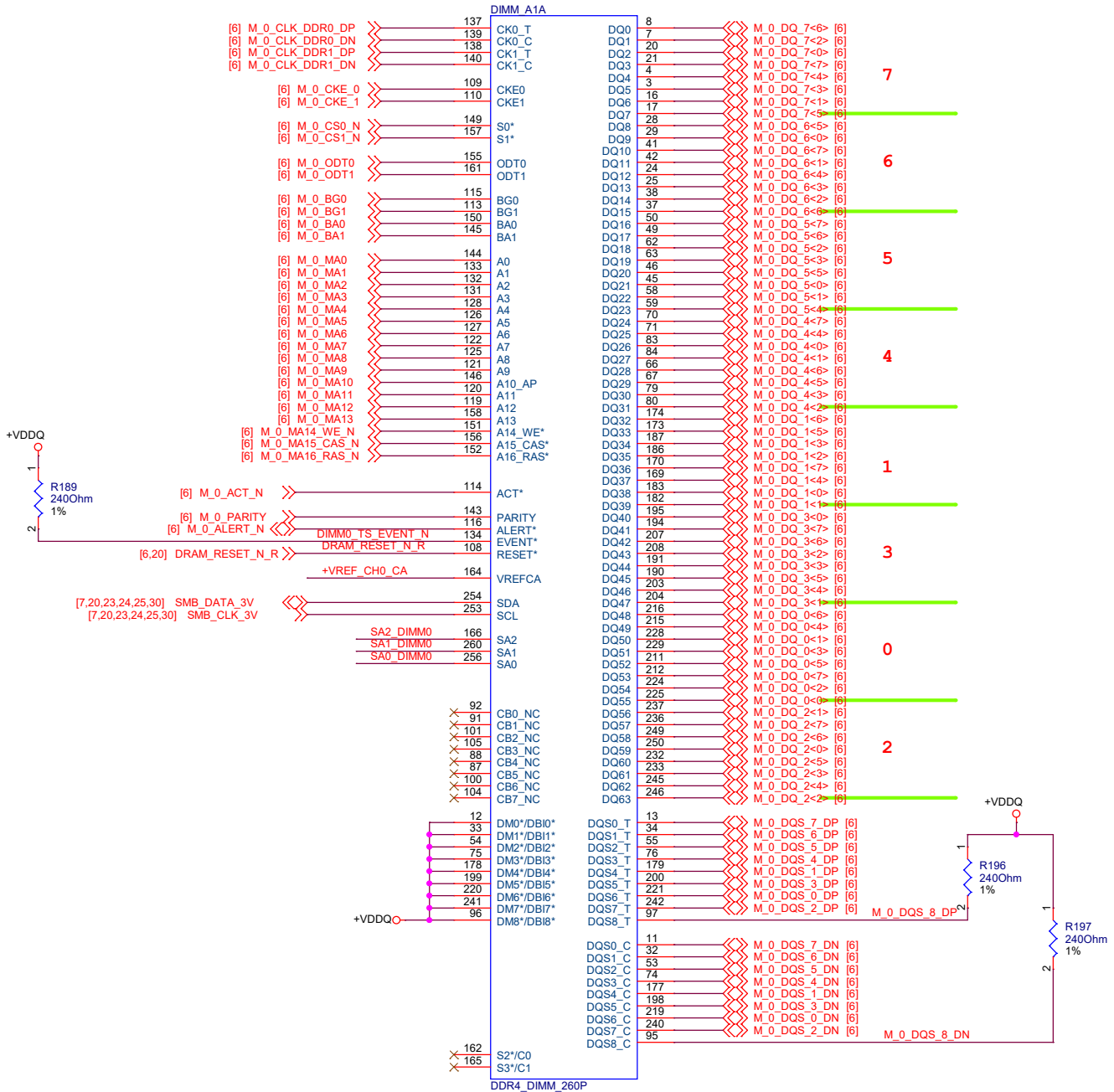


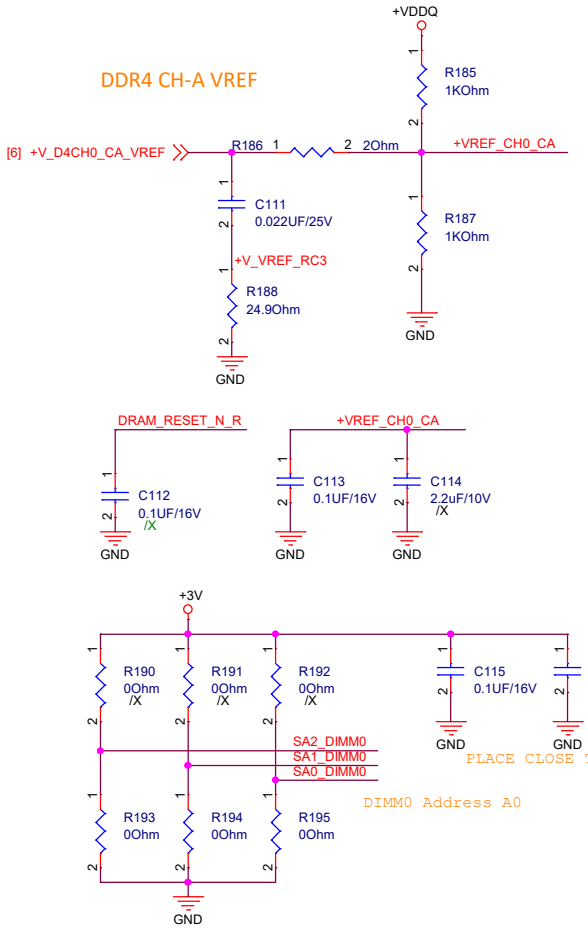


MIX-TGLD1

ASUSTek COMPUTER INC.	Title : SOC-MISC/JTAG	
	Engineer:	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 18 of 59	

DDR4 SODIMM CHANNEL -A

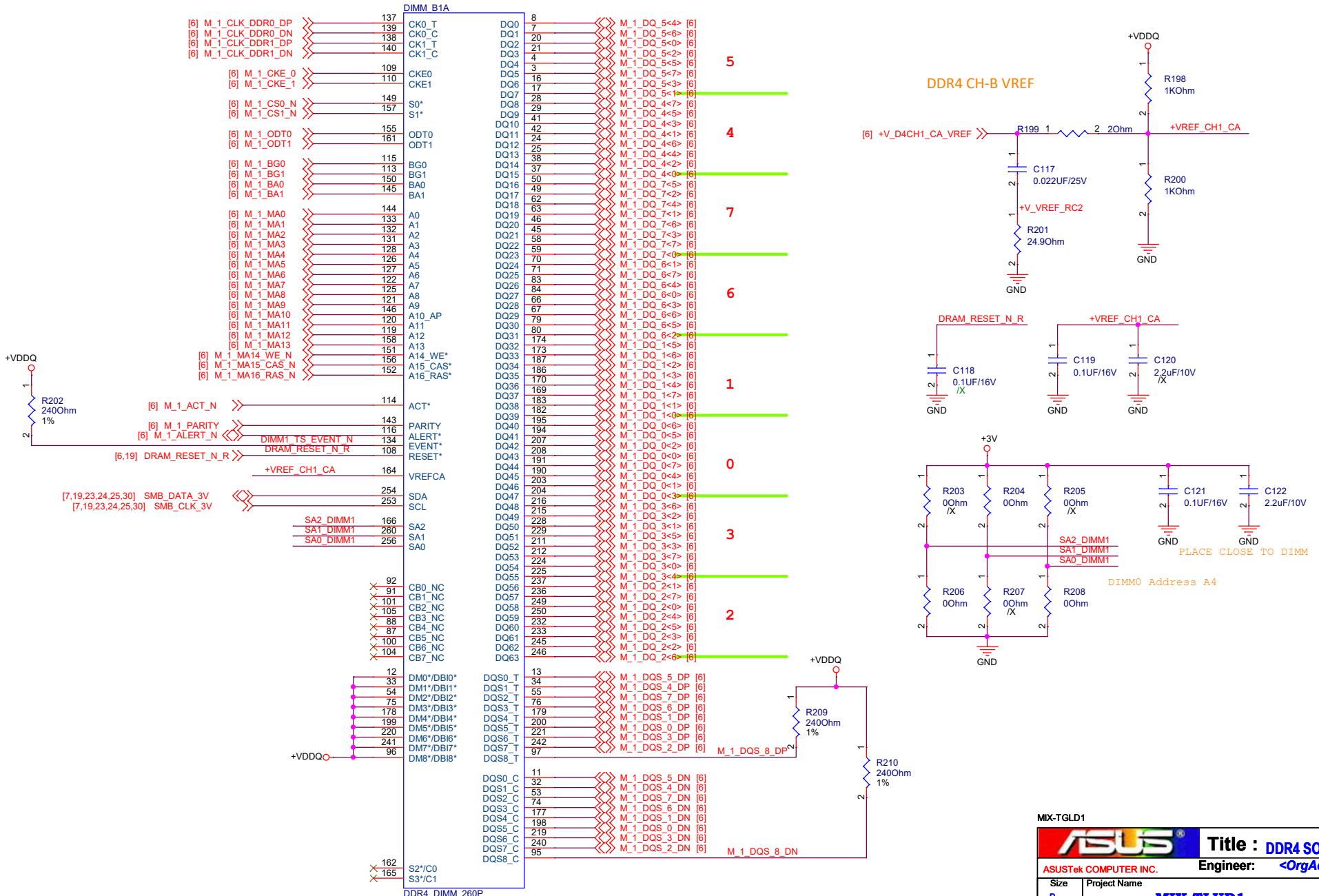




MIX-TGLD1

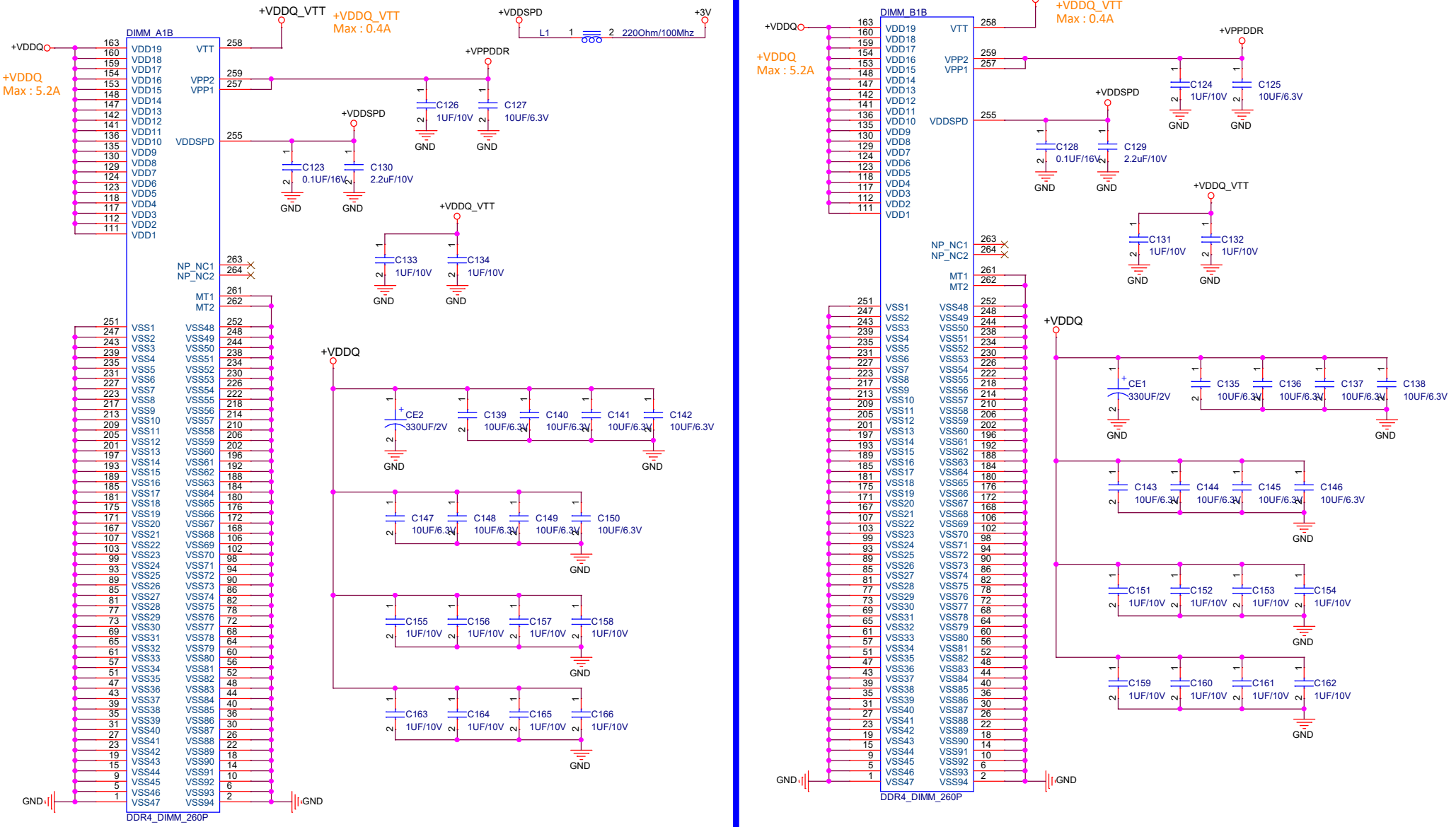
ASUSTek COMPUTER INC.	Title : DDR4 SODIMM-CHA	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 19 of 59	

DDR4 SODIMM CHANNEL -B



MIX-TGLD1

ASUSTek COMPUTER INC.	Title : DDR4 SODIMM-CHB	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 20 of 59	



MIX-TGLD1

ASUSTek COMPUTER INC.	Title : DDR4 SODIM Power	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 21 of 59	

LCD panel Voltage SEL

EDP1_PWR(2-3)

MINI_JUMPER

EDP1_PWR Panel Voltage Select	
1-2	5V
(Default) 2-3	3V

EDP1_PWR1 HEADER_1X3P — 1.5A +5V / +3V → +VEDP1_PANEL_SEL

C167 1UF/10V, C168 0.1UF/16V, GND

Q6 EMF09P02V — +V_PANEL1

C169 10UF/16V, C170 0.1UF/16V, GND

R213 10KOhm, VEDP1_EN, R214 53.6KOhm

Q7 2N7002 — 2N7002 Vth(max) = 2.5V

[5] DDIA_EDP_VDDEN, R215 100KOhm, GND

R211 10KOhm /X, R212 10KOhm /X

[5] DDIA_EDP_BKLTCTL, [5] DDIA_EDP_BKLTEN

R1014 100KOhm, R1013 100KOhm, GND GND

EDP1_HPD

+BLVCC1

+V_PANEL1

EDP1 — WTOB_CON_ 40P

NP_NC2 42, SIDE2 44, SIDE1 43, NP_NC1 41

[5] DDIA_EDP_AUXN, [5] DDIA_EDP_AUXP — C171 0.1UF/16V N/A, C172 0.1UF/16V N/A — eDP1_AUXN_C, eDP1_AUXP_C

[5] DDIA_EDP_TXP0, [5] DDIA_EDP_TXN0 — C173 0.1UF/16V N/A, C174 0.1UF/16V N/A — eDP1_TXP0_C, eDP1_TXN0_C

[5] DDIA_EDP_TXP1, [5] DDIA_EDP_TXN1 — C175 0.1UF/16V N/A, C176 0.1UF/16V N/A — eDP1_TXP1_C, eDP1_TXN1_C

[5] DDIA_EDP_TXP2, [5] DDIA_EDP_TXN2 — C177 0.1UF/16V N/A, C178 0.1UF/16V N/A — eDP1_TXP2_C, eDP1_TXN2_C

[5] DDIA_EDP_TXP3, [5] DDIA_EDP_TXN3 — C179 0.1UF/16V N/A, C180 0.1UF/16V N/A — eDP1_TXP3_C, eDP1_TXN3_C

EDP1_BKL(2-3)

MINI_JUMPER

+BLVCC1 — L2 220Ohm/100Mhz — +BLVCC1_40 — EDP1_BKL1 HEADER_1X3P

+5V 1.5A, +12V

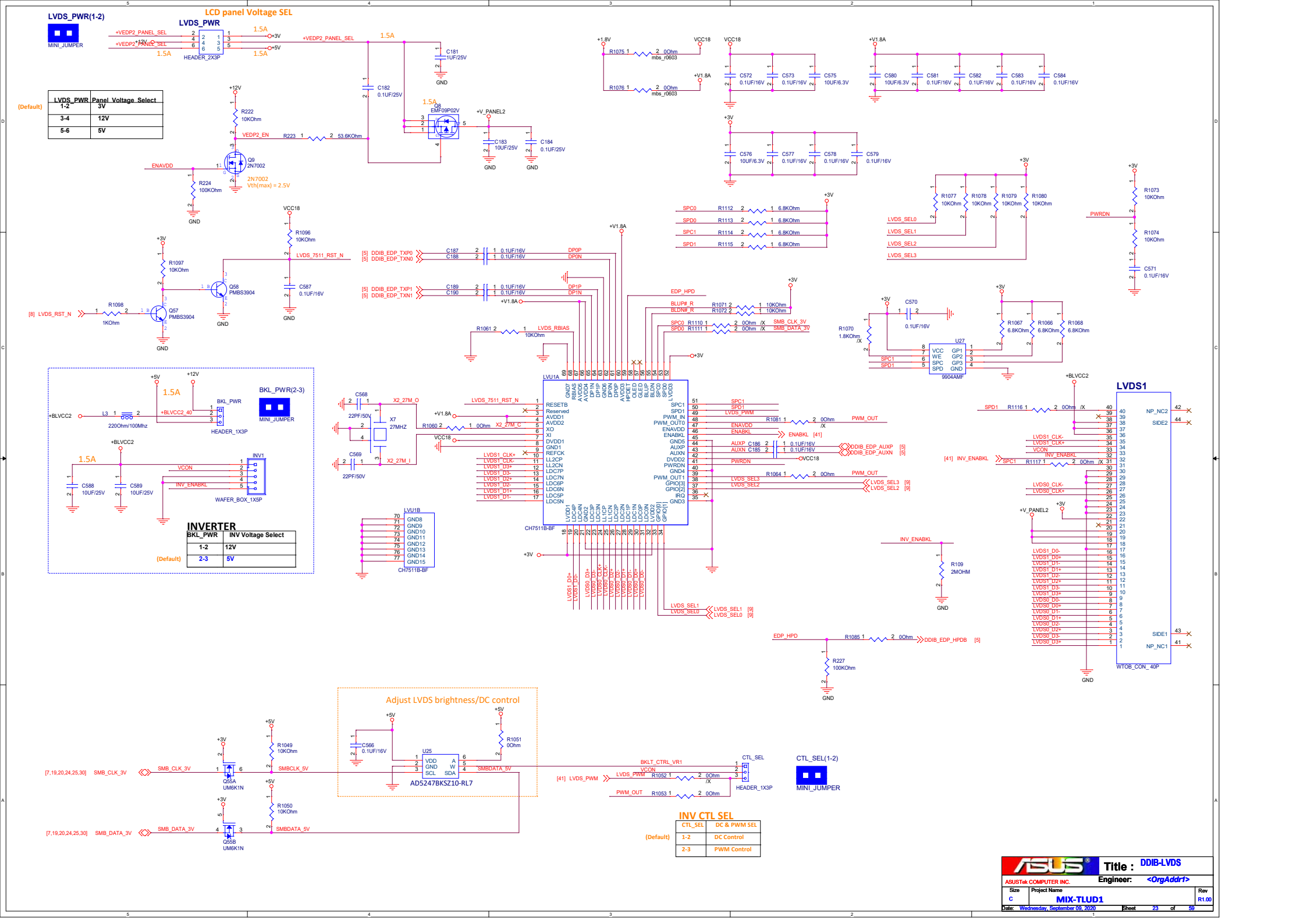
INVERTER

EDP1_BKL	INV Voltage Select
1-2	12V
(Default) 2-3	5V

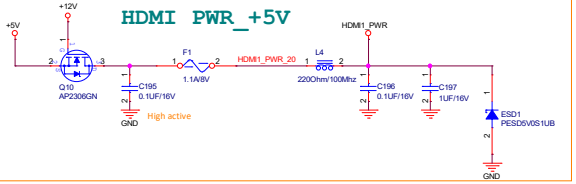
+3V — R216 100KOhm /X — eDP1_AUXN_C, eDP1_AUXP_C — R219 100KOhm /X — GND

EDP1_HPD — R218 100KOhm — Q53 AP2306GN — DDIA_EDP_HPDA [5]

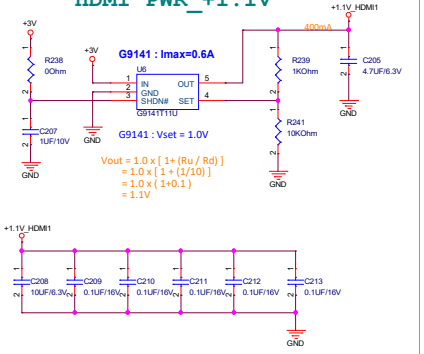
ASUSTek COMPUTER INC.	Title : DDIA-eDP		
	Engineer: <OrgAddr1>		
Size: B	Project Name: MIX-TLUD1		Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 22 of 59		


LVDS_PWR(1-2)
MINI_JUMPER
LCD panel Voltage SEL
LVDS_PWR
HEADER_2X3P
+VEDP2_PANEL_SEL
1.5A
+3V
+5V
+12V
C181 1UF/25V
C182 0.1UF/25V
C183 10UF/25V
C184 0.1UF/25V
R222 10KOhm
R223 53.6KOhm
R224 100KOhm
Q8 EMF09P02V
Q9 2N7002
2N7002 Vth(max) = 2.5V
VEDP2_EN
ENAVDD
+V_PANEL2
GND
(Default)
LVDS_PWR Panel Voltage Select
1-2 3V
3-4 12V
5-6 5V
R1075 0_0Ohm mbs_r0603
R1076 0_0Ohm mbs_r0603
VCC18
+1.8V
+V1.8A
C572 0.1UF/16V
C573 0.1UF/16V
C575 10UF/6.3V
C580 10UF/6.3V
C581 0.1UF/16V
C582 0.1UF/16V
C583 0.1UF/16V
C584 0.1UF/16V
C576 10UF/6.3V
C577 0.1UF/16V
C578 0.1UF/16V
C579 0.1UF/16V
R1096 10KOhm
R1097 10KOhm
R1098 1KOhm
Q58 PMBS3904
Q57 PMBS3904
LVDS_7511_RST_N
[8] LVDS_RST_N
C587 0.1UF/16V
SPC0 R1112 6.8KOhm
SPD0 R1113 6.8KOhm
SPC1 R1114 6.8KOhm
SPD1 R1115 6.8KOhm
R1077 10KOhm
R1078 10KOhm
R1079 10KOhm
R1080 10KOhm
LVDS_SEL0
LVDS_SEL1
LVDS_SEL2
LVDS_SEL3
PWRDN
R1073 10KOhm
R1074 10KOhm
C571 0.1UF/16V
[5] DDIB_EDP_TXP0
[5] DDIB_EDP_TXN0
[5] DDIB_EDP_TXP1
[5] DDIB_EDP_TXN1
C187 0.1UF/16V
C188 0.1UF/16V
C189 0.1UF/16V
C190 0.1UF/16V
DP0P
DP0N
DP1P
DP1N
EDP_HPD
BLUP#_R R1071 10KOhm
BLDN#_R R1072 10KOhm
SPC0 R1110 0Ohm /X SMB_CLK_3V
SPD0 R1111 0Ohm /X SMB_DATA_3V
R1061 LVDS_RBIAS 10KOhm
R1070 1.8KOhm /X
C570 0.1UF/16V
U27 9904AMF
R1067 6.8KOhm
R1066 6.8KOhm
R1068 6.8KOhm
BKL_PWR(2-3)
BKL_PWR
HEADER_1X3P
L3 220Ohm/100Mhz
+BLVCC2
+BLVCC2_40
C588 10UF/25V
C589 10UF/25V
INV1
WAFER_BOX_1X5P
VCON
INV_ENABKL
INVERTER
BKL_PWR INV Voltage Select
1-2 12V
2-3 5V
(Default)
C568 22PF/50V
C569 22PF/50V
X7 27MHZ
X2_27M_O
X2_27M_I
R1060 0Ohm X2_27M_C
LVU1A CH7511B-BF
LVU1B CH7511B-BF
RESETB
Reserved
AVDD1
AVDD2
XO
XI
DVDD1
GND1
REFCK
LL2CP
LL2CN
LDC7P
LDC7N
LDC6P
LDC6N
LDC5P
LDC5N
SPC1
SPD1
PWM_IN
PWM_OUT0
ENAVDD
ENABKL
GND5
AUXP
AUXN
DVDD2
PWRDN
GND4
PWM_OUT1
GPIO[3]
GPIO[2]
IRQ
GND3
GPIO[0]
GPIO[1]
LVDS_7511_RST_N
LVDS1_CLK+
LVDS1_CLK-
LVDS1_D3+
LVDS1_D3-
LVDS1_D2+
LVDS1_D2-
LVDS1_D1+
LVDS1_D1-
LVDS_PWM
PWM_OUT
ENABKL [41]
AUXP C186 0.1UF/16V
AUXN C185 0.1UF/16V
DDIB_EDP_AUXP [5]
DDIB_EDP_AUXN [5]
PWRDN
VCC18
R1081 0Ohm /X
R1064 0Ohm
LVDS_SEL3 [9]
LVDS_SEL2 [9]
LVDS_SEL1
LVDS_SEL0
LVDS1
WTOB_CON_40P
NP_NC2
SIDE2
SIDE1
NP_NC1
SPD1 R1116 0Ohm /X
SPC1 R1117 0Ohm /X
[41] INV_ENABKL
LVDS1_D0-
LVDS1_D0+
LVDS1_D1-
LVDS1_D1+
LVDS1_D2-
LVDS1_D2+
LVDS1_D3-
LVDS1_D3+
LVDS0_CLK-
LVDS0_CLK+
LVDS0_D0-
LVDS0_D0+
LVDS0_D1-
LVDS0_D1+
LVDS0_D2-
LVDS0_D2+
LVDS0_D3-
LVDS0_D3+
R109 2MOHM
EDP_HPD
R1085 0Ohm
DDIB_EDP_HPDB [5]
R227 100KOhm
Adjust LVDS brightness/DC control
U25 AD5247BKSZ10-RL7
C566 0.1UF/16V
R1049 10KOhm
R1050 10KOhm
R1051 0Ohm
Q55A UM6K1N
Q55B UM6K1N
SMB_CLK_3V
SMB_DATA_3V
SMBCLK_5V
SMBDATA_5V
[7,19,20,24,25,30] SMB_CLK_3V
[7,19,20,24,25,30] SMB_DATA_3V
BKLT_CTRL_VR1
VCON
LVDS_PWM R1052 0Ohm /X
PWM_OUT R1053 0Ohm
[41] LVDS_PWM
CTL_SEL
HEADER_1X3P
CTL_SEL(1-2)
MINI_JUMPER
INV CTL SEL
CTL_SEL DC & PWM SEL
(Default) 1-2 DC Control
2-3 PWM Control
ASUSTek COMPUTER INC.
Title : DDIB-LVDS
Engineer: <OrgAddr1>
Size C
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
Sheet 23 of 59

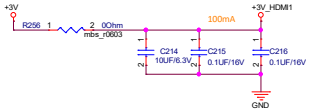
HDMI PWR_+5V



HDMI PWR_+1.1V

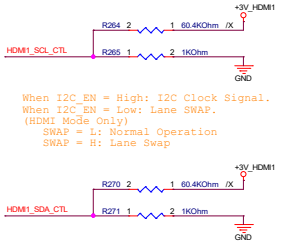


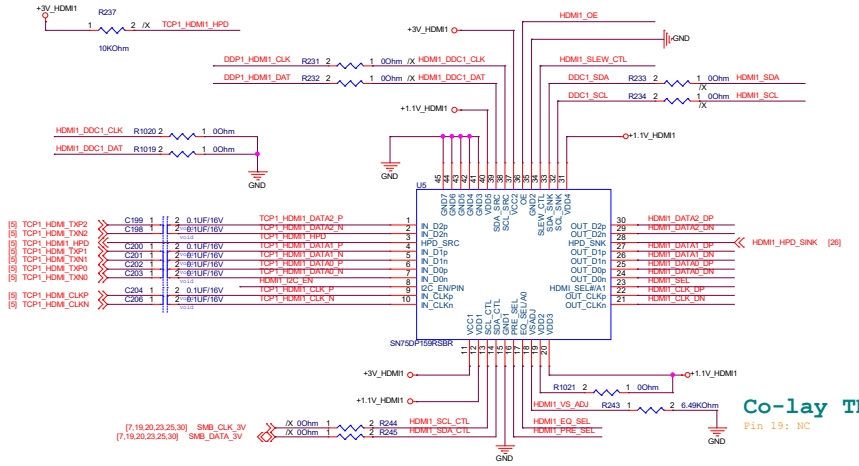
HDMI PWR_+3V



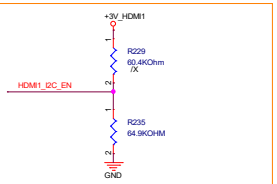
Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

Co-lay TDP158RSB

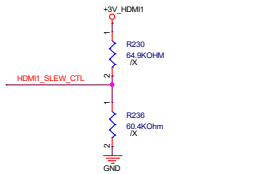




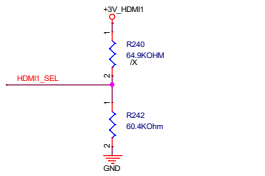
Co-lay TDP158RSB
Pin 19: NC



I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode



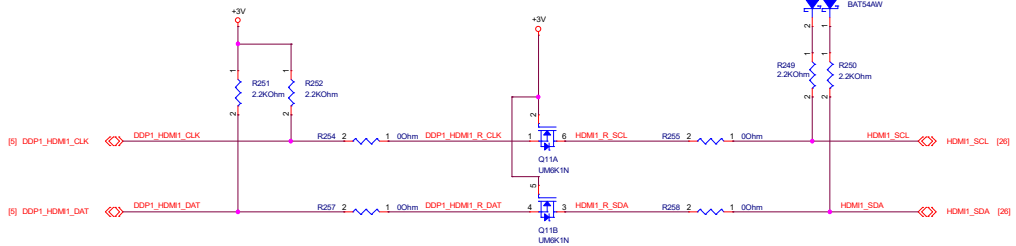
Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

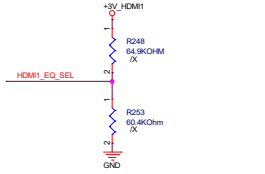


HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Co-lay TDP158RSB
Pin 23: A1/EQ2:
When I2C_EN = High: I2C Address Bit 2
When I2C_EN = Low: EQ2 Pin Setting
Works in conjunction with A0/EQ1;
See Main Link Inputs for settings

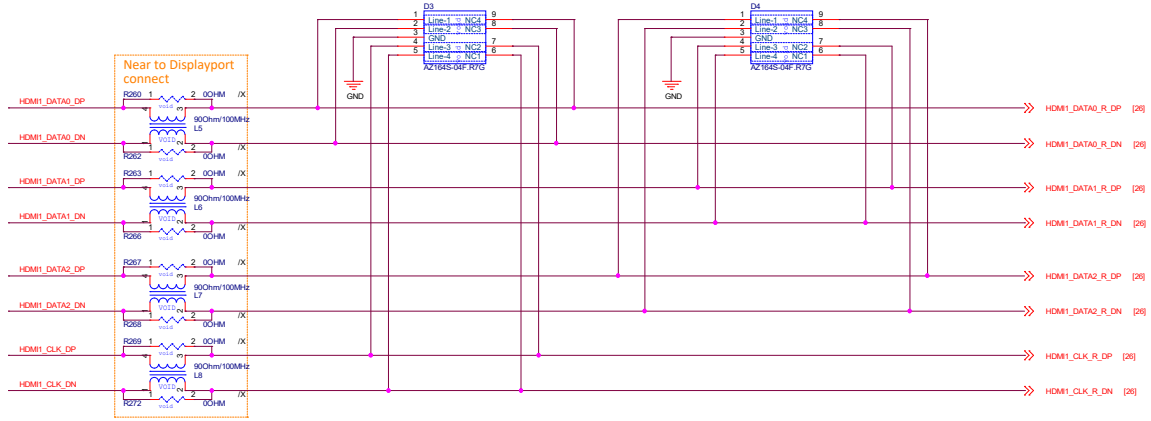
HDMI Active-Level Shift

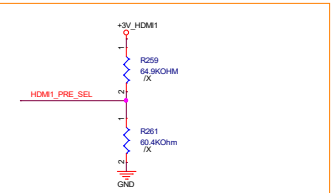




Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

Co-lay TDP158RSB
Pin 17: A0/EQ1:
When I2C_EN = High: I2C Address Bit 1
When I2C_EN = Low: EQ1 Pin Setting
Works in conjunction with A1/EQ2;
See Main Link Inputs for settings





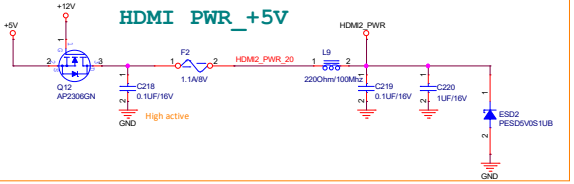
De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: ~ 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

Co-lay TDP158RSB
Pin 16: TERM:
I2C_EN/PIN = High: NA
I2C_EN/PIN = Low: Source Termination Control
TERM = H: 75 Ω ~ 150 Ω
TERM = L: 150 Ω ~ 300 Ω
TERM = NC: No transmit Termination
Note: When TMDS_CLOCK_RATIO_STATUS bit = 1
the TDP158 sets source termination to 75 Ω ~ 150 Ω Automatically

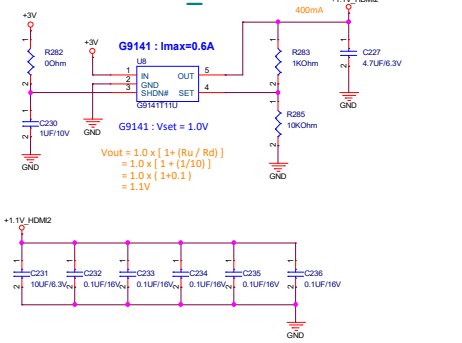
MIX-TGLD1

ASUSTek COMPUTER INC.	Title : TCP1-HDMI1 (PS8409)	
	Engineer:	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 24 of 59	

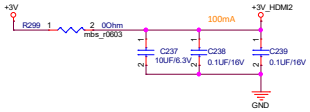
HDMI PWR_+5V



HDMI PWR_+1.1V

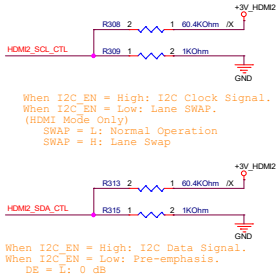


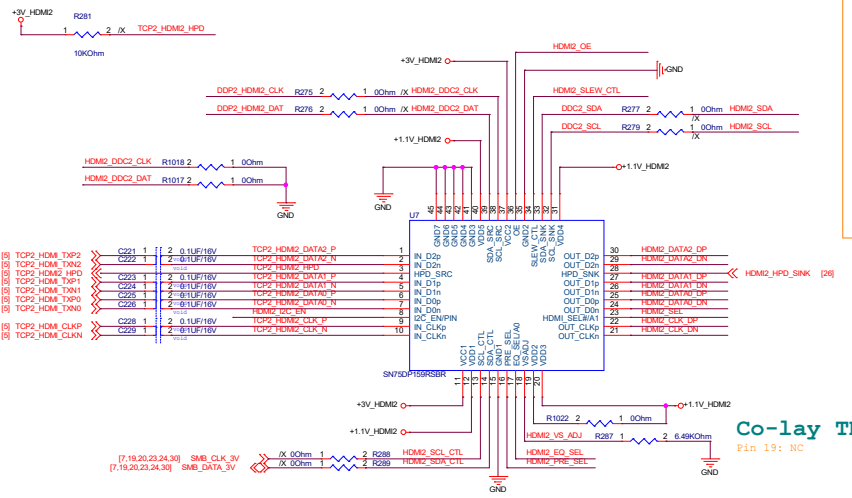
HDMI PWR_+3V



Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

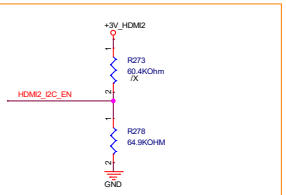
Co-lay TDP158RSB



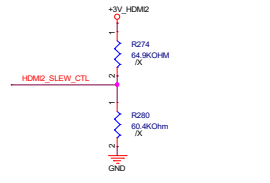


Co-lay TDP158RSB

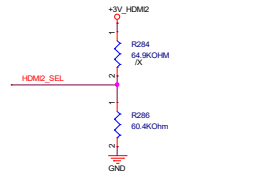
Pin 19: NC



I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode



Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

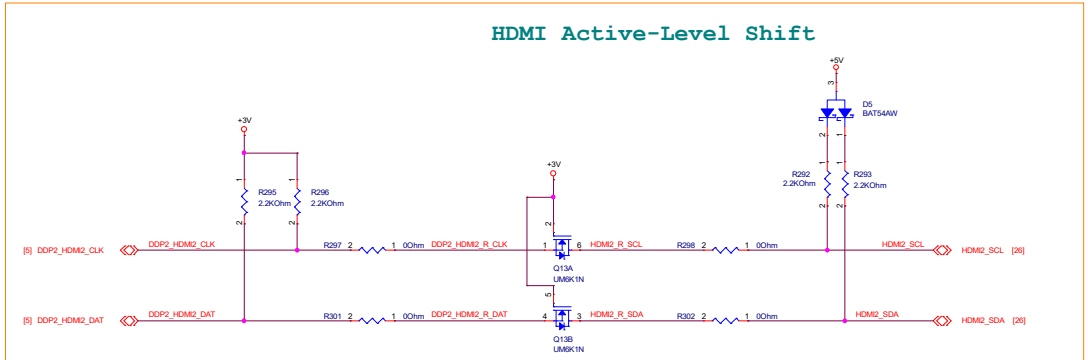


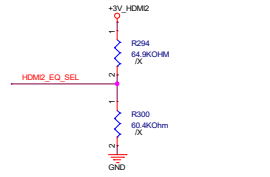
HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Co-lay TDP158RSB

Pin 23: A1/EQ2:
When I2C_EN = High: I2C Address Bit 2
When I2C_EN = Low: EQ2 Pin Setting
Works in conjunction with A0/EQ1;
See Main Link Inputs for settings

HDMI Active-Level Shift

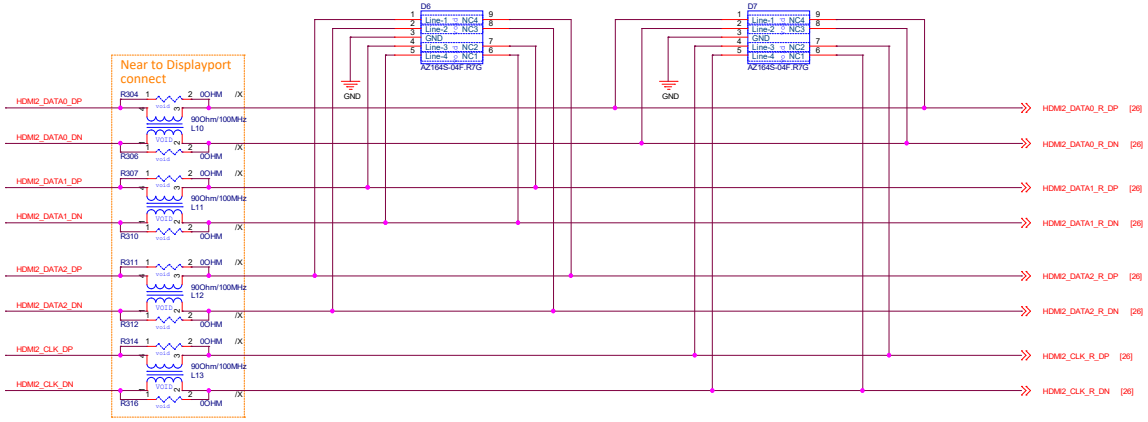


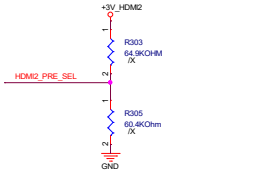


Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

Co-lay TDP158RSB

Pin 17: A0/EQ1:
When I2C_EN = High: I2C Address Bit 1
When I2C_EN = Low: EQ1 Pin Setting
Works in conjunction with A1/EQ2;
See Main Link Inputs for settings





De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

Co-lay TDP158RSB

Pin 16: TERM:
I2C_EN/PIN = High: NA
I2C_EN/PIN = Low: Source Termination Control
TERM = H: 75 Ω ~ 150 Ω
TERM = L: 150 Ω ~ 300 Ω
TERM = NC: No transmit Termination
Note: When TMDS_CLOCK_RATIO_STATUS bit = 1
the TDP158 sets source termination to 75 Ω ~ 150 Ω Automatically

MIX-TGLD1

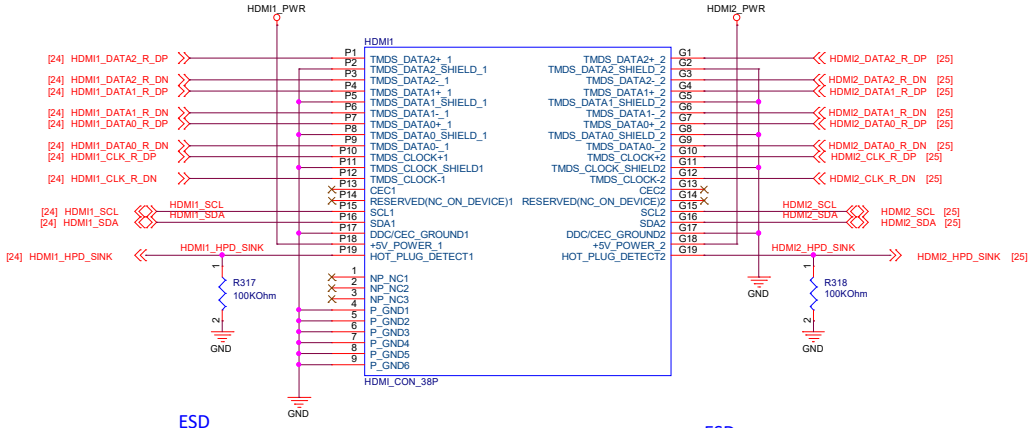
ASUSTek COMPUTER INC.

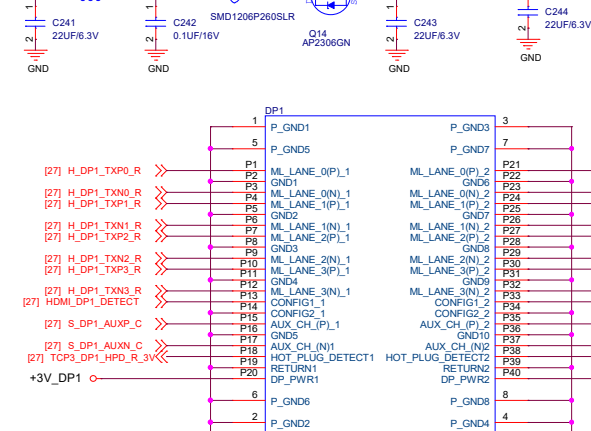
Title : TCP2-HDMI2 (PS8409)

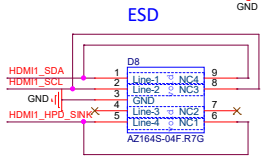
Engineer:

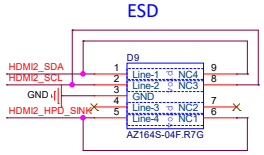
Size	Project Name	Rev
Custom	MIX-TLUD1	R1.00

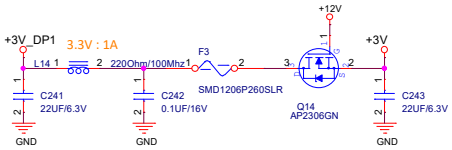
Date: Wednesday, September 09, 2020 Sheet 25 of 59

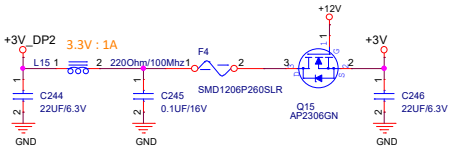


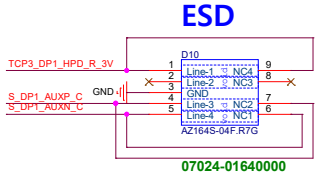


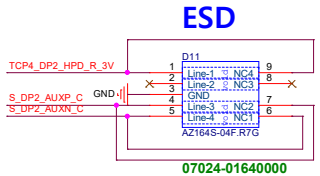












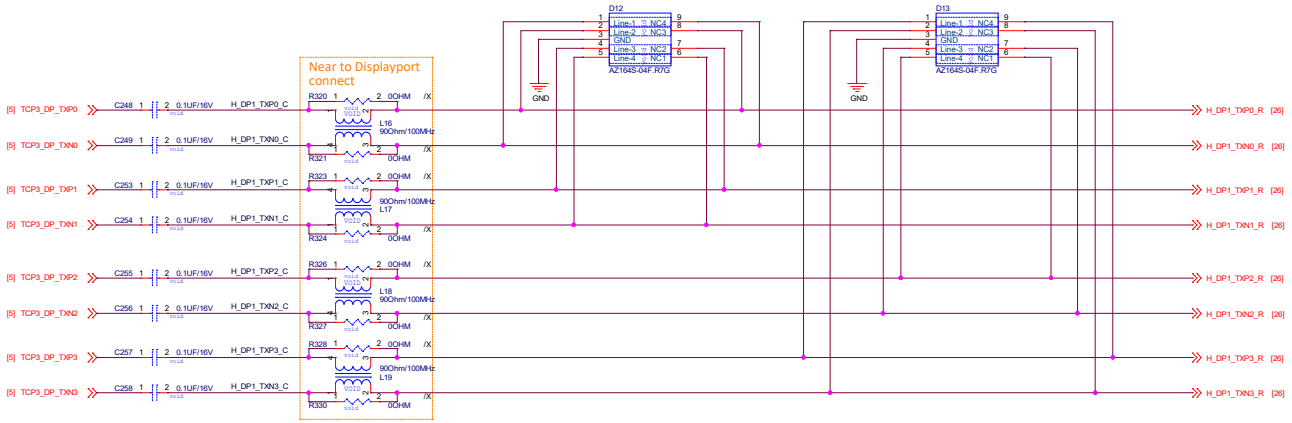
ASUSTek COMPUTER INC.

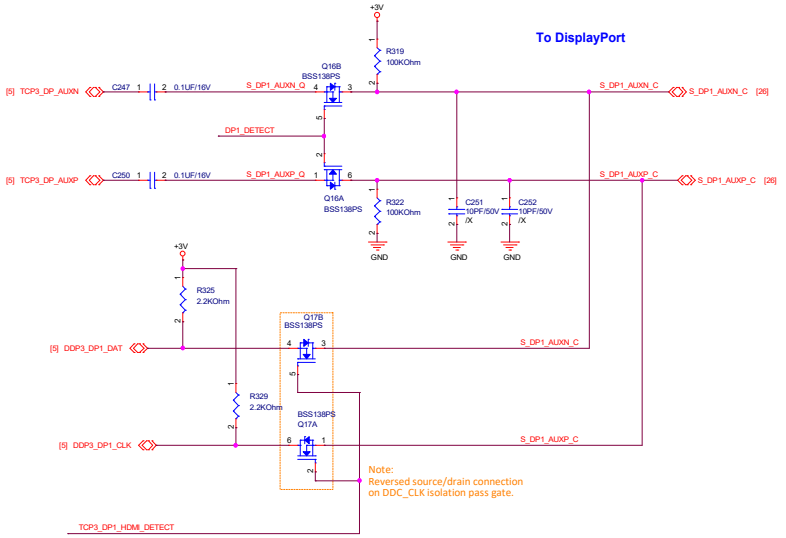
Title : HDMI/DP CONNECTOR

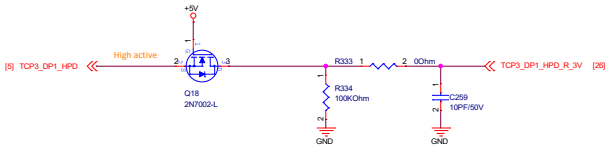
Engineer: <OrgAddr1>

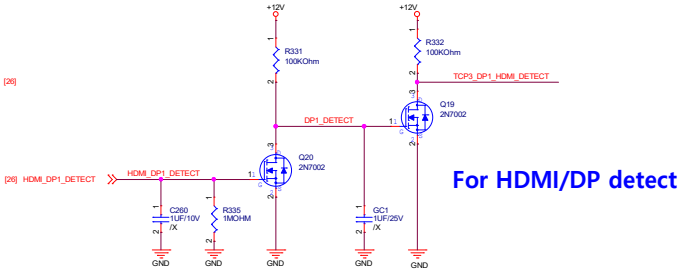
Size	Project Name	Rev
Custom	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 26 of 59

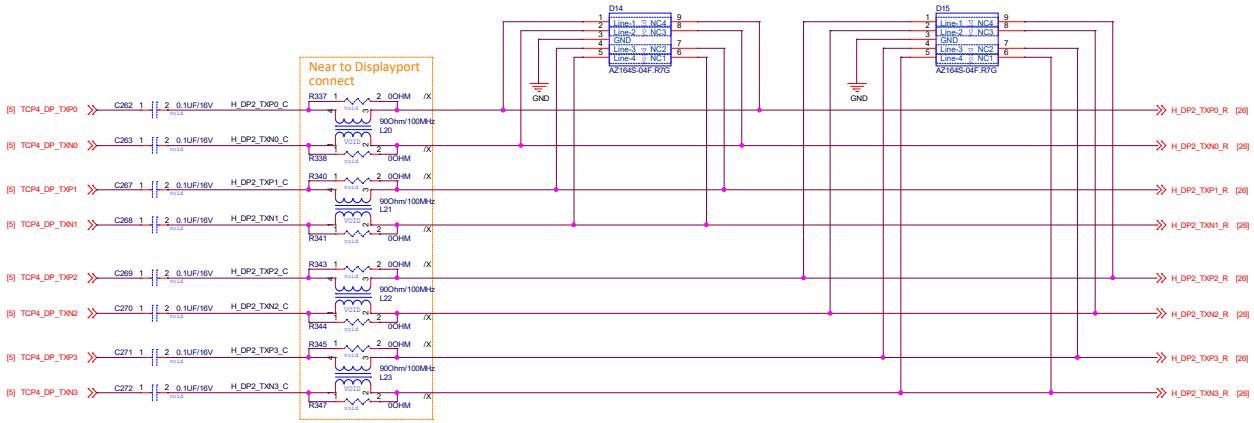


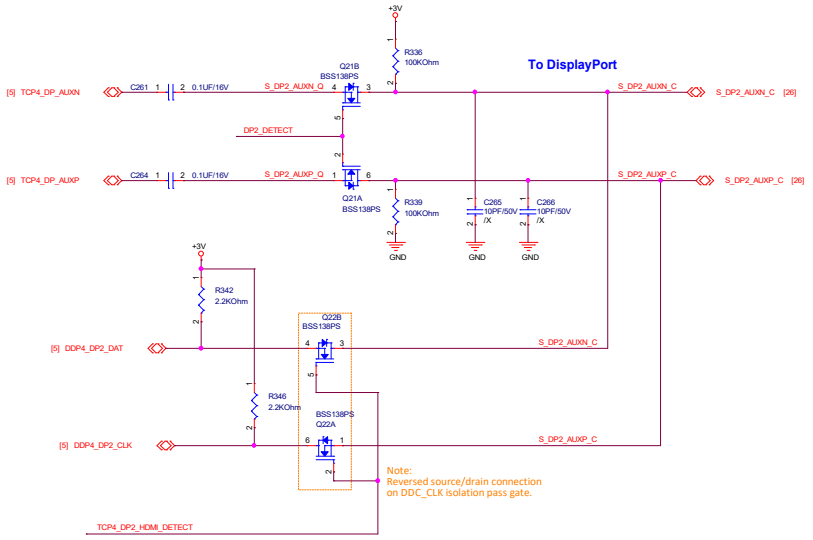


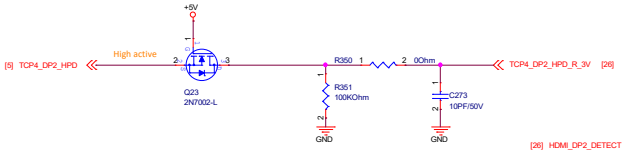


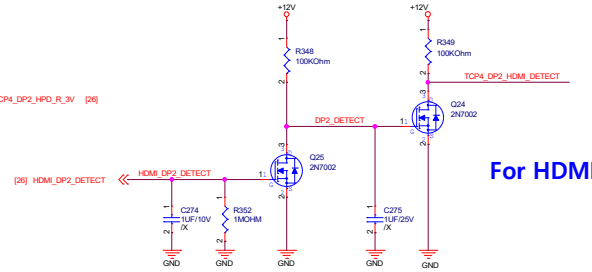


ASUSTek COMPUTER INC.	Title : TCP3 (DP1++)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: MIX-TLUD1		Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 27 of 59		



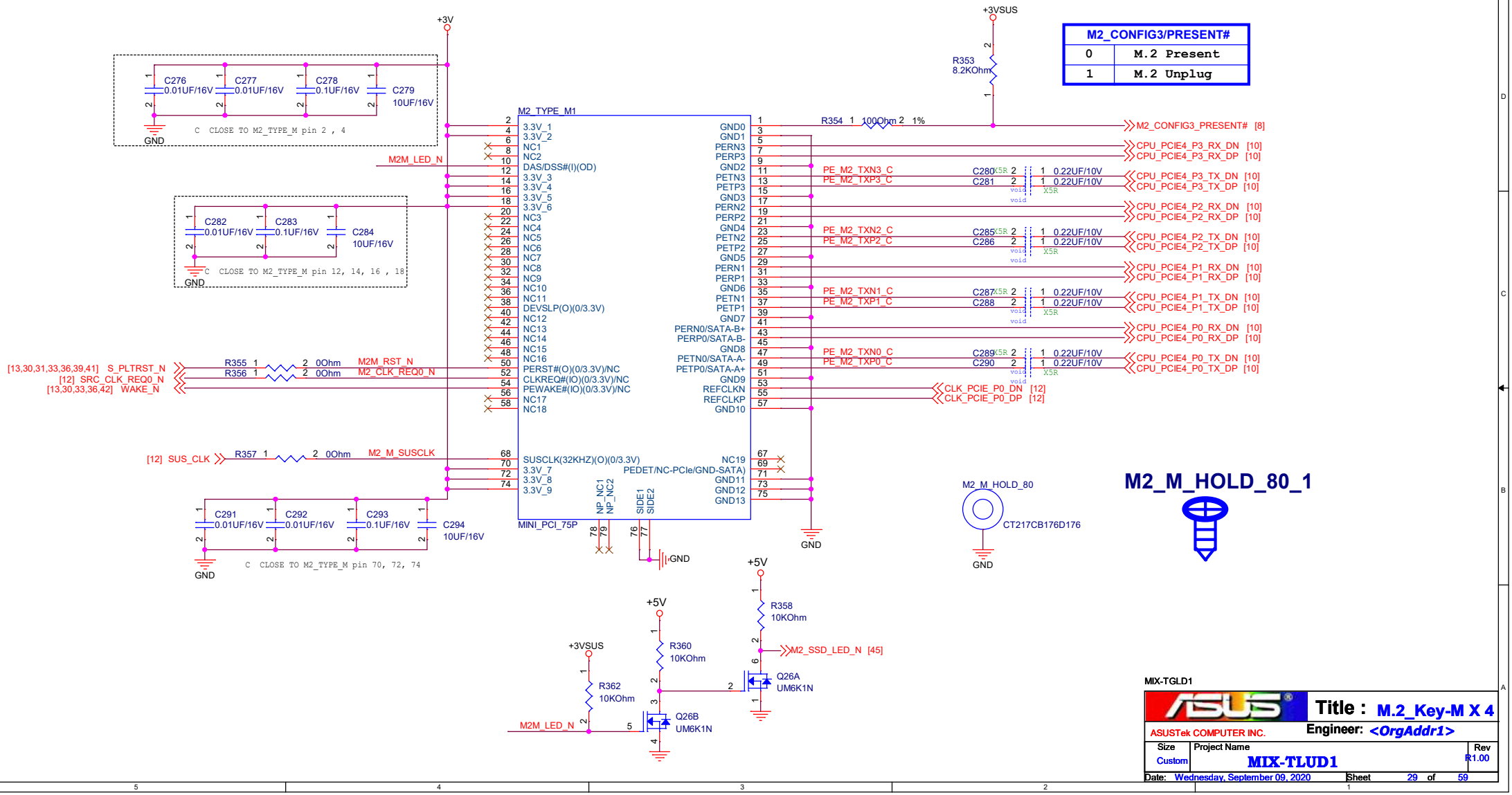






For HDMI/DP detect

ASUSTek COMPUTER INC.	Title : TCP4 (DP2++)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: MIX-TLUD1		Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 26 of 59		


M2_CONFIG3/PRESENT#
0 M.2 Present
1 M.2 Unplug
M2_TYPE_M1
MINI_PCI_75P
M2_M_HOLD_80_1
M2_M_HOLD_80
CT217CB176D176
MIX-TGLD1
Title : M.2_Key-M X 4
ASUSTek COMPUTER INC.
Engineer: <OrgAddr1>
Size Custom
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
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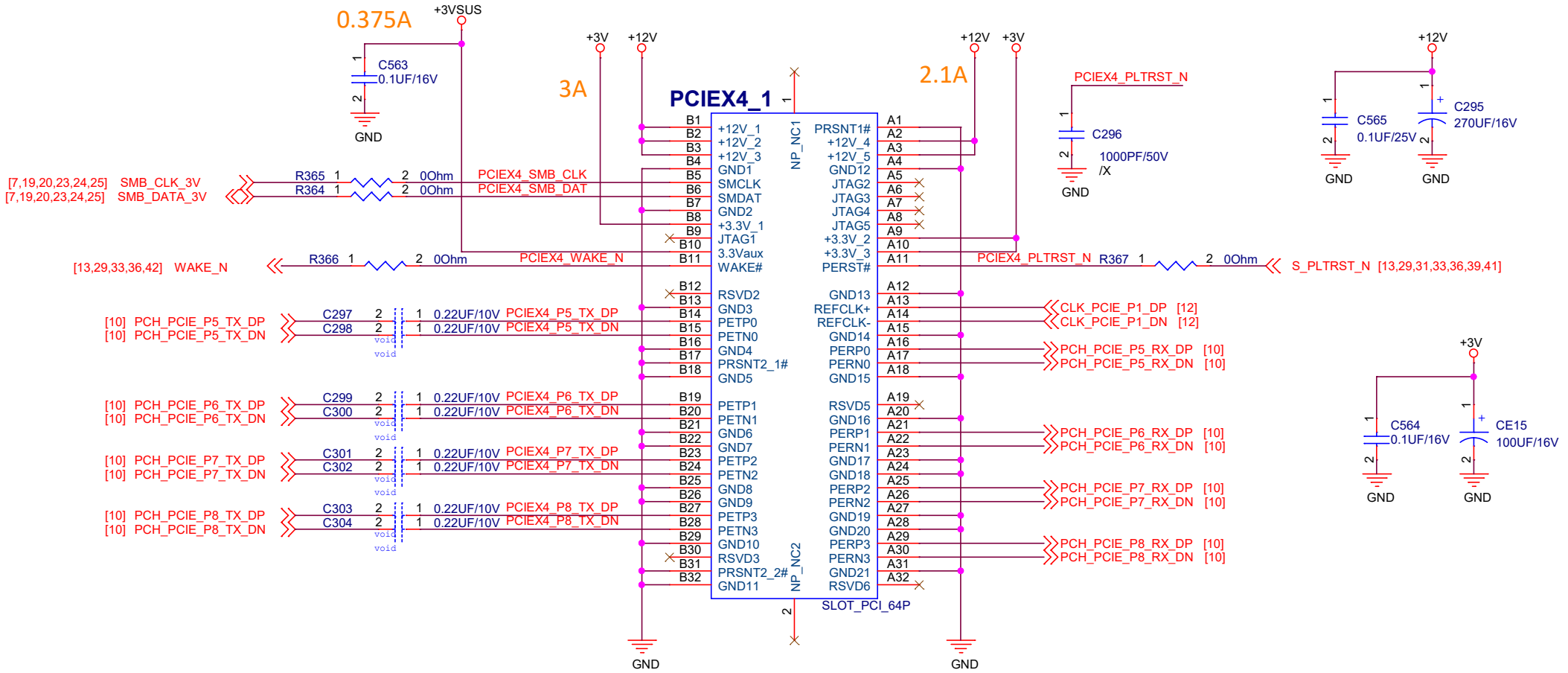
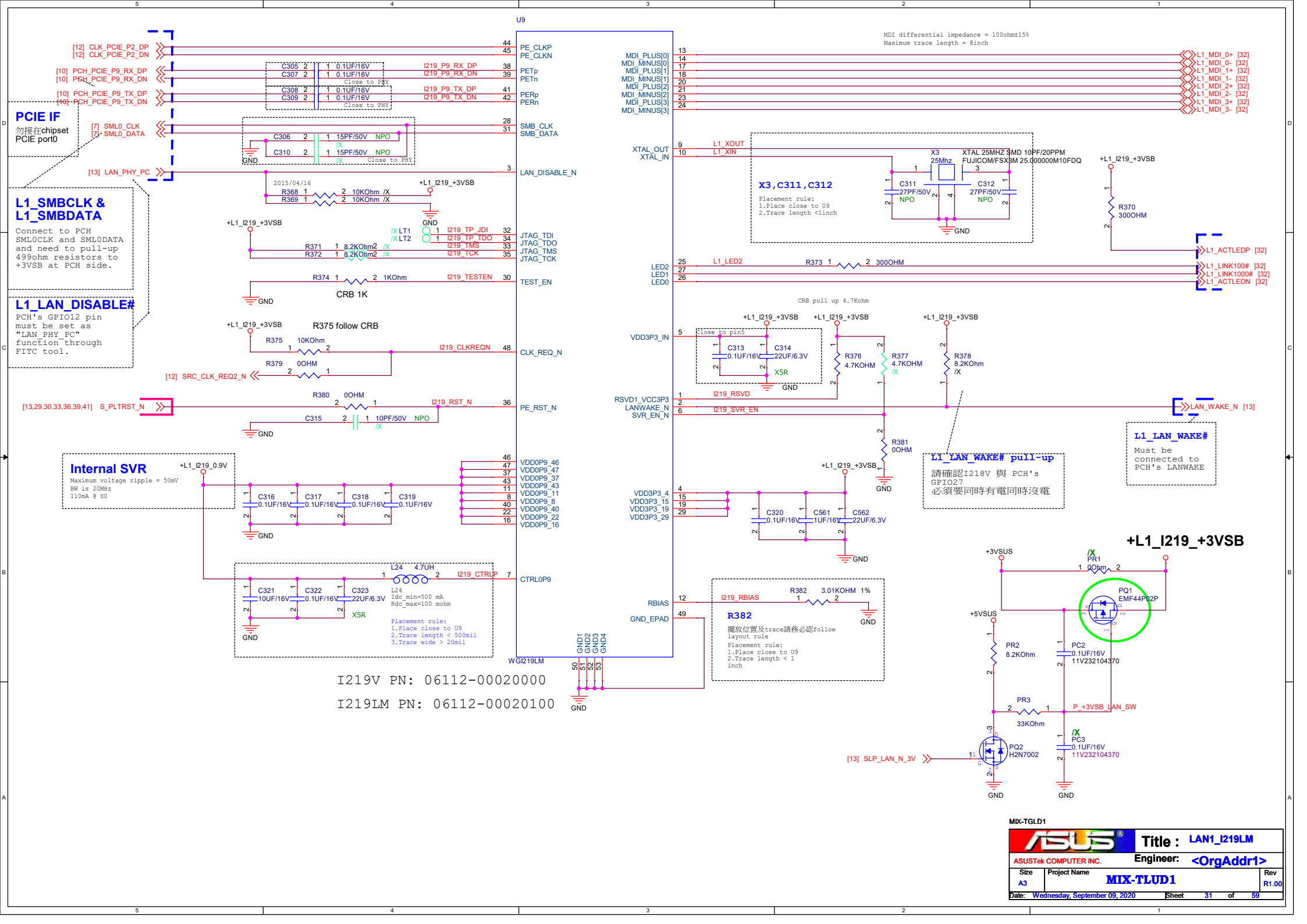


MIX-TGLD1

ASUSTek COMPUTER INC.	Title : PCIEX4_1	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 30 of 59	


U9
PCIE IF
勿接在chipset
PCIE port0
L1_SMBCLK &
L1_SMBDATA
Connect to PCH
SML0CLK and SML0DATA
and need to pull-up
499ohm resistors to
+3VSB at PCH side.
L1_LAN_DISABLE#
PCH's GPIO12 pin
must be set as
"LAN_PHY_PC"
function through
FITC tool.
Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0
R375 follow CRB
CRB 1K
CRB pull up 4.7Kohm
X3,C311,C312
Placement rule:
1.Place close to U9
2.Trace length <1inch
L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電
L1_LAN_WAKE#
Must be
connected to
PCH's LANWAKE
R382
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to U9
2.Trace length < 1 inch
+L1_I219_+3VSB
I219V PN: 06112-00020000
I219LM PN: 06112-00020100
MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch
MIX-TGLD1
Title : LAN1_I219LM
ASUSTek COMPUTER INC.
Engineer: <OrgAddr1>
Size A3
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
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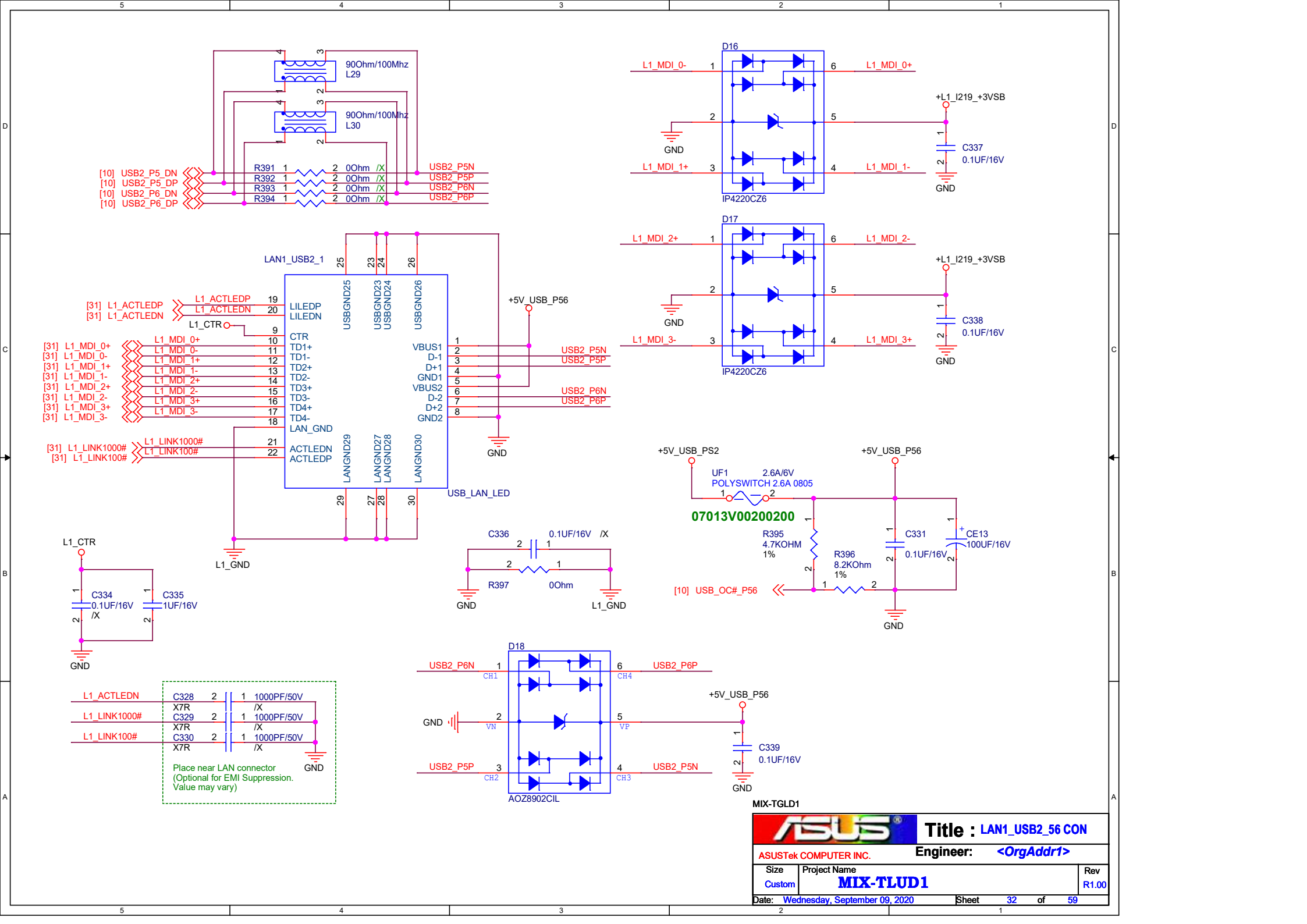

90Ohm/100Mhz
L29
90Ohm/100Mhz
L30
[10] USB2_P5_DN
[10] USB2_P5_DP
[10] USB2_P6_DN
[10] USB2_P6_DP
R391 1 2 0Ohm /X
R392 1 2 0Ohm /X
R393 1 2 0Ohm /X
R394 1 2 0Ohm /X
USB2_P5N
USB2_P5P
USB2_P6N
USB2_P6P
D16
L1_MDI_0-
L1_MDI_0+
L1_MDI_1+
L1_MDI_1-
GND
IP4220CZ6
+L1_I219_+3VSB
C337
0.1UF/16V
D17
L1_MDI_2+
L1_MDI_2-
L1_MDI_3-
L1_MDI_3+
C338
0.1UF/16V
LAN1_USB2_1
[31] L1_ACTLEDP
[31] L1_ACTLEDN
L1_ACTLEDP
L1_ACTLEDN
L1_CTR
[31] L1_MDI_0+
[31] L1_MDI_0-
[31] L1_MDI_1+
[31] L1_MDI_1-
[31] L1_MDI_2+
[31] L1_MDI_2-
[31] L1_MDI_3+
[31] L1_MDI_3-
LILEDP
LILEDN
CTR
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
TD4+
TD4-
LAN_GND
ACTLEDN
ACTLEDP
USBGND25
USBGND23
USBGND24
USBGND26
LANGND29
LANGND27
LANGND28
LANGND30
VBUS1
D-1
D+1
GND1
VBUS2
D-2
D+2
GND2
+5V_USB_P56
USB_LAN_LED
[31] L1_LINK1000#
[31] L1_LINK100#
L1_LINK1000#
L1_LINK100#
L1_GND
C336 0.1UF/16V /X
R397 0Ohm
+5V_USB_PS2
UF1 2.6A/6V
POLYSWITCH 2.6A 0805
07013V00200200
R395 4.7KOHM 1%
R396 8.2KOhm 1%
C331 0.1UF/16V
CE13 100UF/16V
[10] USB_OC#_P56
C334 0.1UF/16V /X
C335 1UF/16V
L1_ACTLEDN
L1_LINK1000#
L1_LINK100#
C328 X7R 1000PF/50V /X
C329 X7R 1000PF/50V /X
C330 X7R 1000PF/50V /X
Place near LAN connector
(Optional for EMI Suppression.
Value may vary)
D18
USB2_P6N
USB2_P6P
USB2_P5P
USB2_P5N
CH1
CH2
CH3
CH4
VN
VP
AOZ8902CIL
C339
0.1UF/16V
MIX-TGLD1
Title : LAN1_USB2_56 CON
ASUSTek COMPUTER INC.
Engineer: <OrgAddr1>
Size Custom
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
Sheet 32 of 59

SMBUS DESIGN NOTE:

> For non-vPro platforms or standard PCIe device: SMBUS is not required (2.2K-10K pull-ups to +3.3V_LAN).
> For vPRO platforms: I225 SMBUS must connect to PCH's SMLINK0
> The pull-up power rail should be same with PCH's SMLINK0 power rail (to avoid leakge current)
> Foxville SMBUS speed default is 1MHz. The pull-ups should be 499ohm for 1MHz.
(Use 2.2Kohm if runing 400KHz speed and 10Kohm if running 100KHz speed).
> I225 Default SMBUS Addess is 0x49.

PCIE DESIGN NOTE:

PCIe must be configured as a standard PCIe port.
Do Not configure to the Gbe port (like I219).

RESET DESIGN NOTE:

If uses a GPIO, make sure its power can support S3 or S5 as required.

LED DESIGN NOTE:

There is no specific industrial standard for Ethernet LEDs.
This schematic just shows the most common SPEED LED configuration:
Highest Speed = Green
2nd Highest Speed = Yellow
All other lower Speeds = OFF
No Cable/Link = OFF
All LED pins are set active low. See Datasheet for additional info.

LAN DISABLE DESIGN NOTE:

Connect I225's LAN_DISABLE_N to PCH's GPIO output is optional.
(Do not config as PCH's LANPHYPC, which is I219 specific).

Foxville

SMBUS Address is 0x49.

one at each 0.95V pin

one at each 3.3V pin

Pin7

Pin9 & 38

Keep short and wide

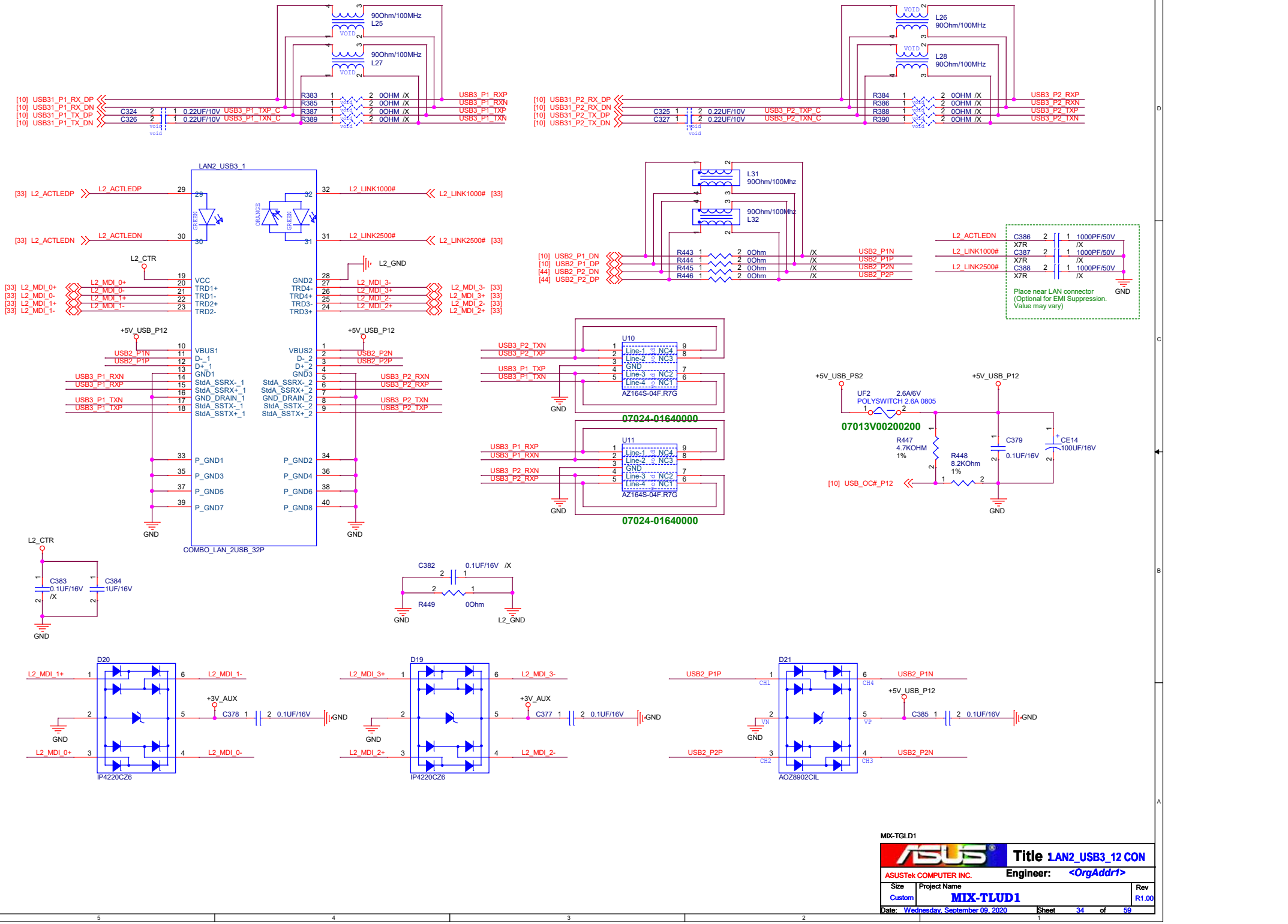
190mA

+0.95V:1.2A

FOR I225-LM

FOR I225-V

MIX-TGLD1			
ASUSTek COMPUTER INC.	Title : LAN2_I255-V		
	Engineer: <OrgAddr1>		
Size: C	Project Name: MIX-TLUD1		Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 33 of 59		


90Ohm/100MHz
L25
90Ohm/100MHz
L27
[10] USB31_P1_RX_DP
[10] USB31_P1_RX_DN
[10] USB31_P1_TX_DP
[10] USB31_P1_TX_DN
C324 0.22UF/10V USB3_P1_TXP_C
C326 0.22UF/10V USB3_P1_TXN_C
R383 R385 R387 R389 0OHM /X
USB3_P1_RXP
USB3_P1_RXN
USB3_P1_TXP
USB3_P1_TXN
L26
90Ohm/100MHz
L28
90Ohm/100MHz
[10] USB31_P2_RX_DP
[10] USB31_P2_RX_DN
[10] USB31_P2_TX_DP
[10] USB31_P2_TX_DN
C325 0.22UF/10V USB3_P2_TXP_C
C327 0.22UF/10V USB3_P2_TXN_C
R384 R386 R388 R390 0OHM /X
USB3_P2_RXP
USB3_P2_RXN
USB3_P2_TXP
USB3_P2_TXN
LAN2_USB3_1
[33] L2_ACTLEDP
L2_ACTLEDP
[33] L2_ACTLEDN
L2_ACTLEDN
L2_CTR
L2_LINK1000#
L2_LINK2500#
L2_GND
[33] L2_MDI_0+
[33] L2_MDI_0-
[33] L2_MDI_1+
[33] L2_MDI_1-
L2_MDI_0+
L2_MDI_0-
L2_MDI_1+
L2_MDI_1-
L2_MDI_3-
L2_MDI_3+
L2_MDI_2-
L2_MDI_2+
VCC
TRD1+
TRD1-
TRD2+
TRD2-
GND2
TRD4-
TRD4+
TRD3-
TRD3+
+5V_USB_P12
USB2_P1N
USB2_P1P
USB2_P2N
USB2_P2P
VBUS1
D-_1
D+_1
GND1
VBUS2
D-_2
D+_2
GND3
USB3_P1_RXN
USB3_P1_RXP
USB3_P1_TXN
USB3_P1_TXP
USB3_P2_RXN
USB3_P2_RXP
USB3_P2_TXN
USB3_P2_TXP
StdA_SSRX-_1
StdA_SSRX+_1
GND_DRAIN_1
StdA_SSTX-_1
StdA_SSTX+_1
StdA_SSRX-_2
StdA_SSRX+_2
GND_DRAIN_2
StdA_SSTX-_2
StdA_SSTX+_2
P_GND1
P_GND3
P_GND5
P_GND7
P_GND2
P_GND4
P_GND6
P_GND8
GND
COMBO_LAN_2USB_32P
L31
90Ohm/100Mhz
90Ohm/100Mhz
L32
[10] USB2_P1_DN
[10] USB2_P1_DP
[44] USB2_P2_DN
[44] USB2_P2_DP
R443 R444 R445 R446 0Ohm /X
USB2_P1N
USB2_P1P
USB2_P2N
USB2_P2P
L2_ACTLEDN
L2_LINK1000#
L2_LINK2500#
C386 C387 C388 1000PF/50V X7R /X
Place near LAN connector
(Optional for EMI Suppression.
Value may vary)
GND
U10
U11
Line-1 NC4
Line-2 NC3
GND
Line-3 NC2
Line-4 NC1
AZ164S-04F.R7G
07024-01640000
07024-01640000
+5V_USB_PS2
+5V_USB_P12
UF2 2.6A/6V
POLYSWITCH 2.6A 0805
07013V00200200
R447 4.7KOHM 1%
R448 8.2KOhm 1%
C379 0.1UF/16V
CE14 100UF/16V
[10] USB_OC#_P12
C383 0.1UF/16V /X
C384 1UF/16V
C382 0.1UF/16V /X
R449 0Ohm
D20
D19
D21
L2_MDI_1+
L2_MDI_1-
L2_MDI_0+
L2_MDI_0-
L2_MDI_3+
L2_MDI_3-
L2_MDI_2+
L2_MDI_2-
+3V_AUX
C378 0.1UF/16V
C377 0.1UF/16V
C385 0.1UF/16V
USB2_P1P
USB2_P1N
USB2_P2P
USB2_P2N
IP4220CZ6
IP4220CZ6
AOZ8902CIL
MIX-TGLD1
Title LAN2_USB3_12 CON
ASUSTek COMPUTER INC.
Engineer: <OrgAddr1>
Size Custom
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
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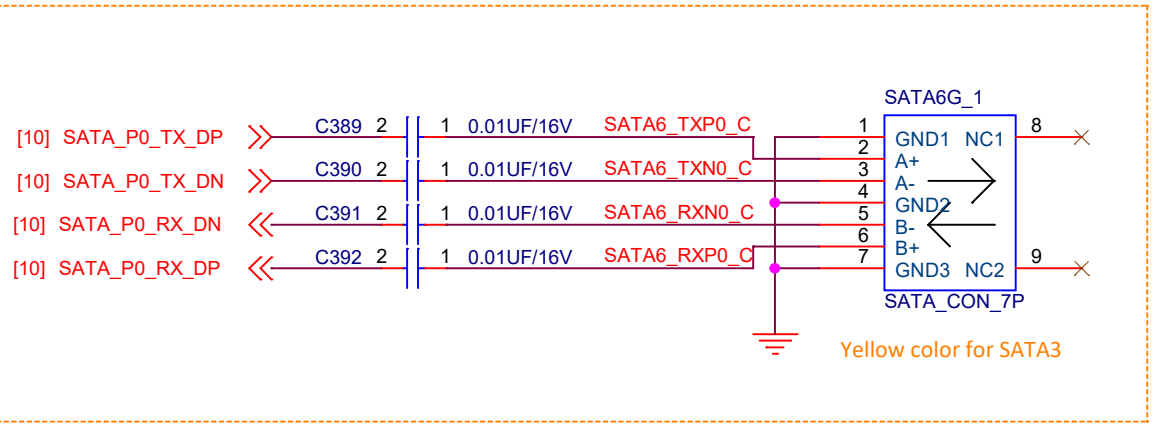
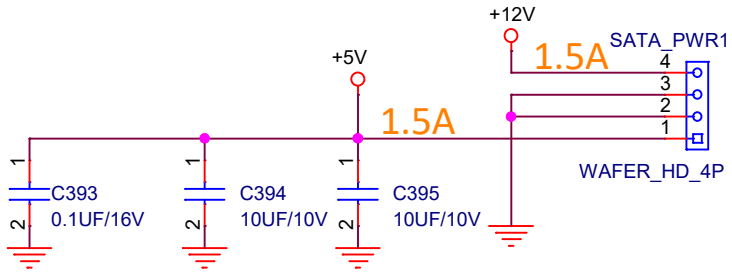
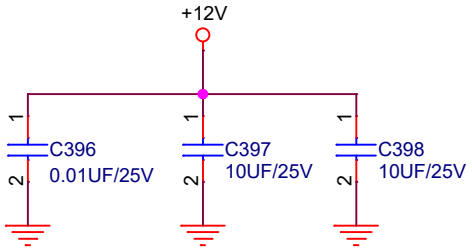


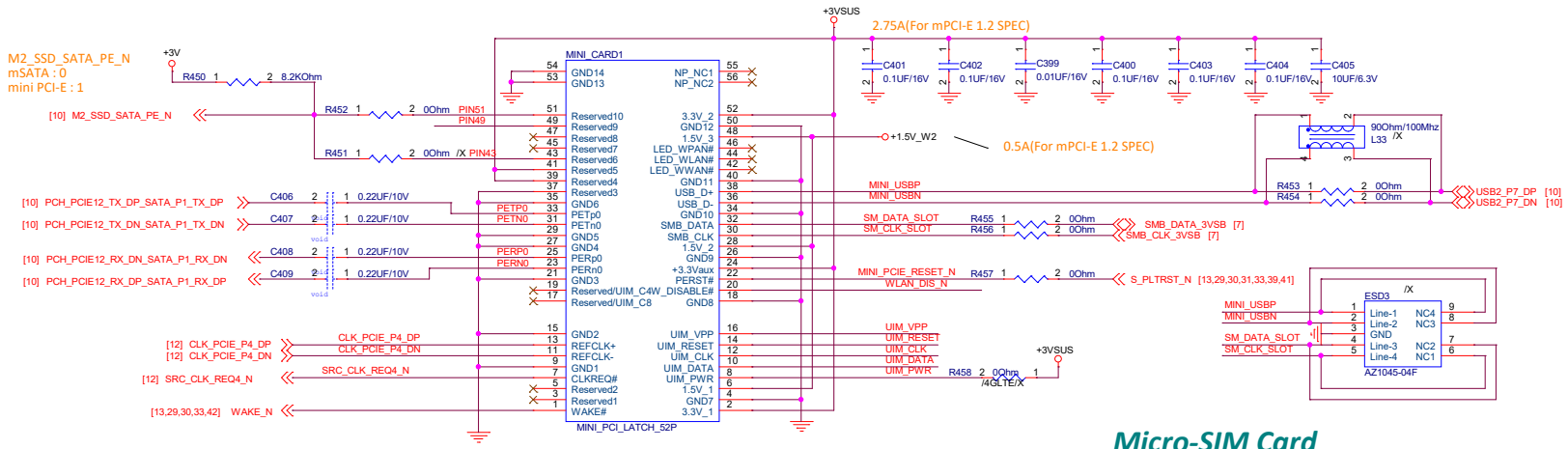
For SATA PWR





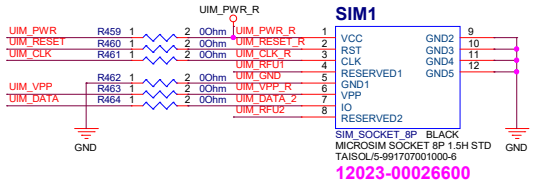
ASUSTek COMPUTER INC.	Title : SATA CON	
	Engineer: <OrgAddr1>	
Size: A	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 35 of 59	

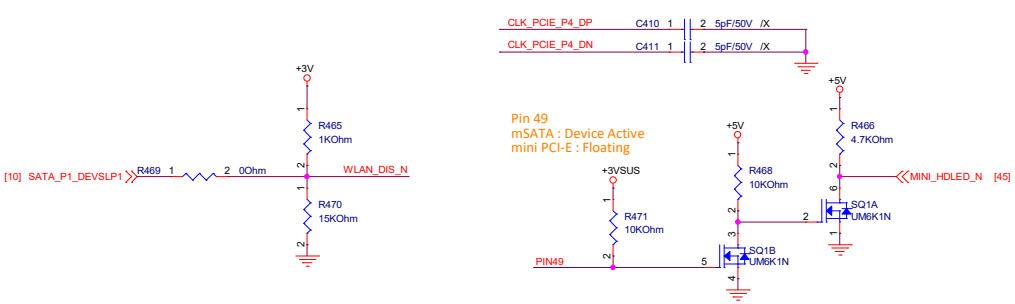
Mini PCI-E Card (Full size)



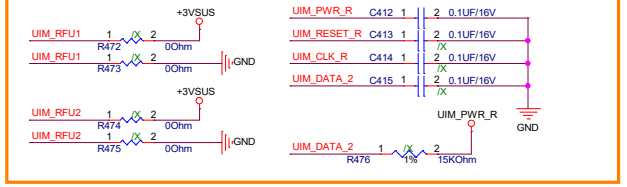
Full Size

Micro-SIM Card

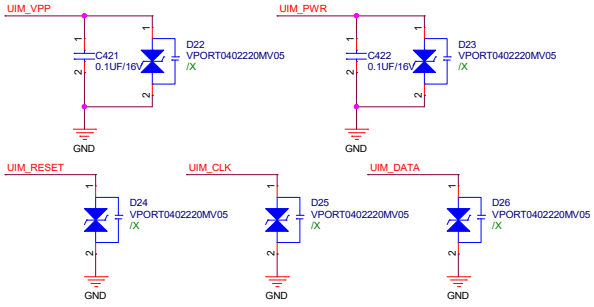


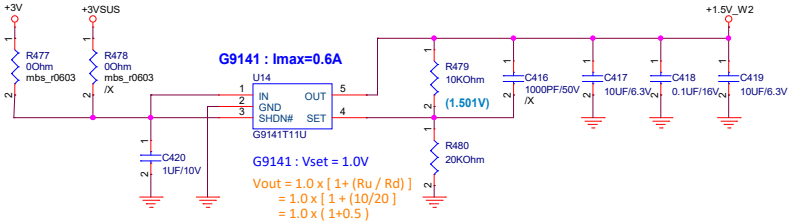


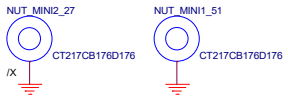
Micro-SIM Card - Reserved Pin for Signal Quality



Micro-SIM Card - ESD Protection

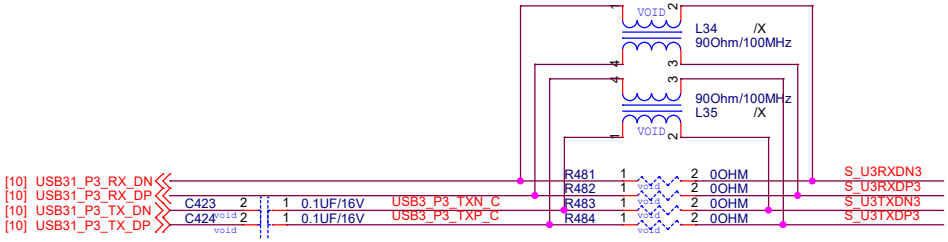


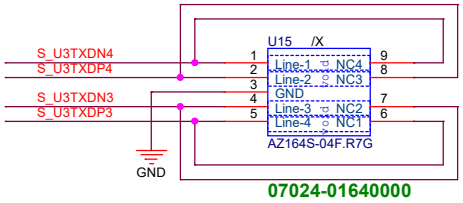




NUT_MINI2_27_1 /X **NUT_MINI1_51_1**

ASUSTeK COMPUTER INC.	Title : SIM/Mini PCIE (Full size)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: MIX-TLUD1		Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 36 of 59		





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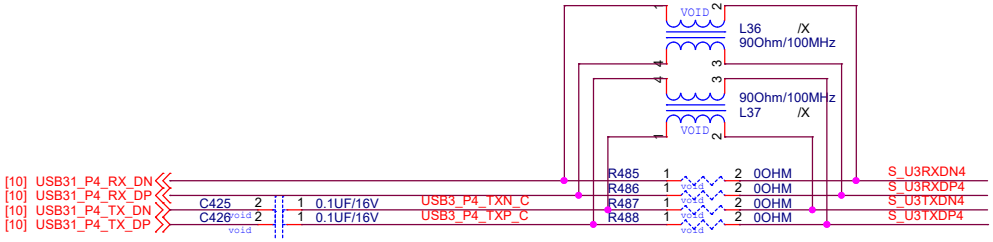

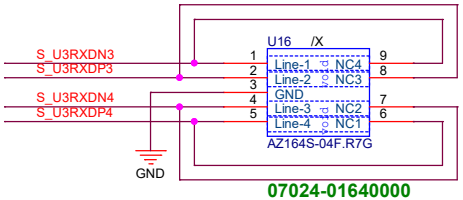

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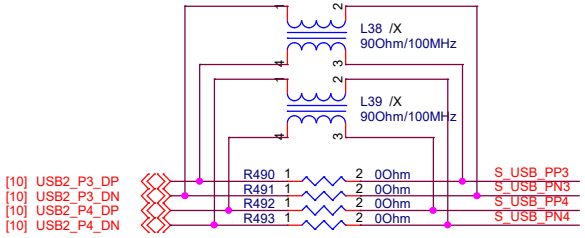
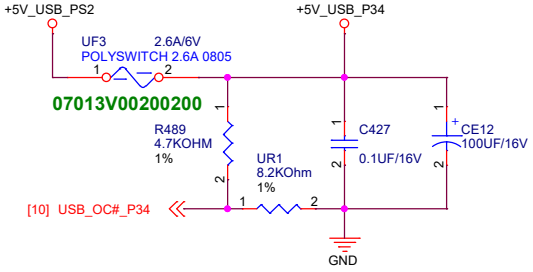
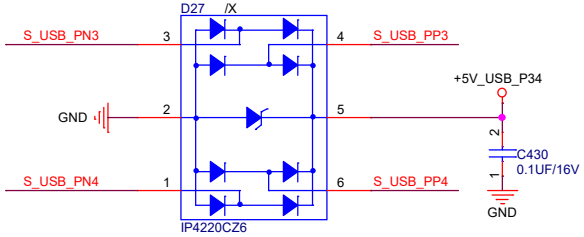
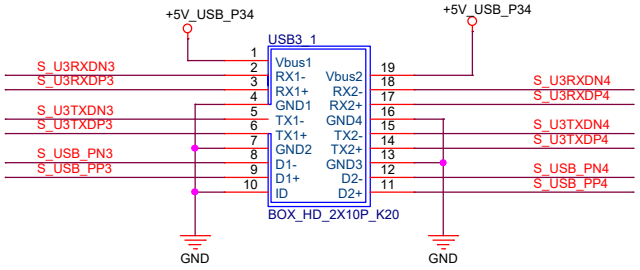




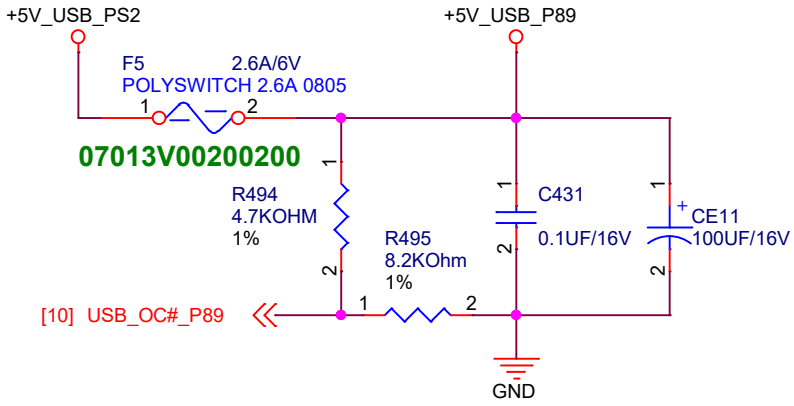
07013V00200200

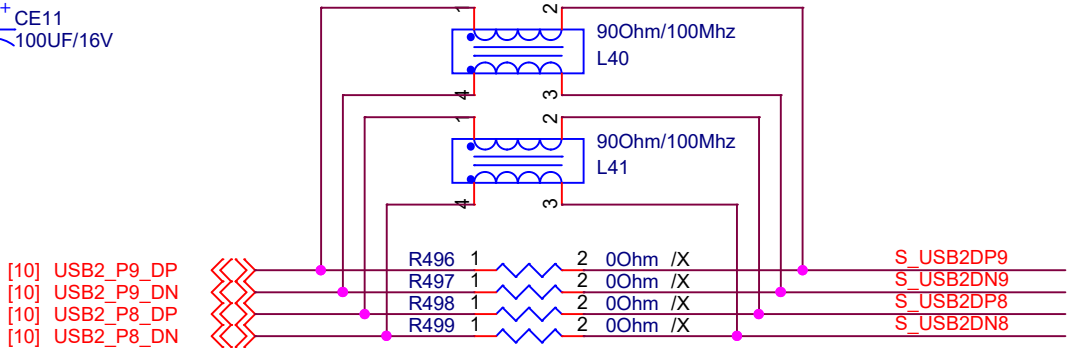


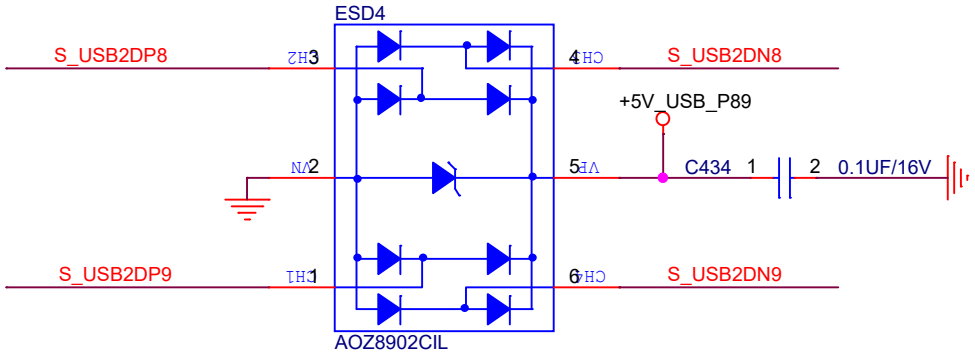


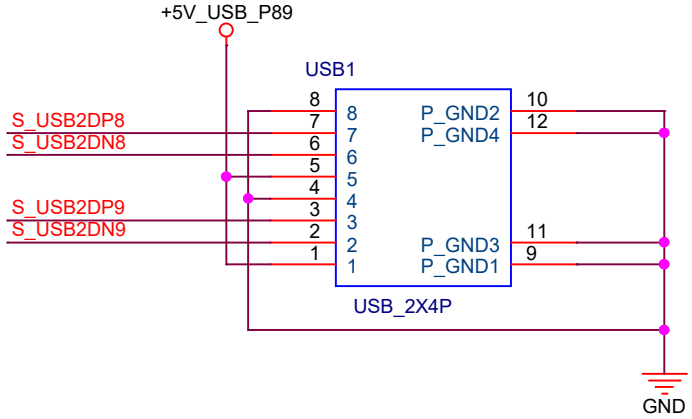
MIX-TGLD1

ASUSTek COMPUTER INC.	Title : USB3_34 BUS HEADER	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 37 of 59	









ASUSTek COMPUTER INC.	Title : USB2_89 CON	
	Engineer: <OrgAddr1>	
Size: A	Project Name: MIX-TLUD1	Rev: R1.00
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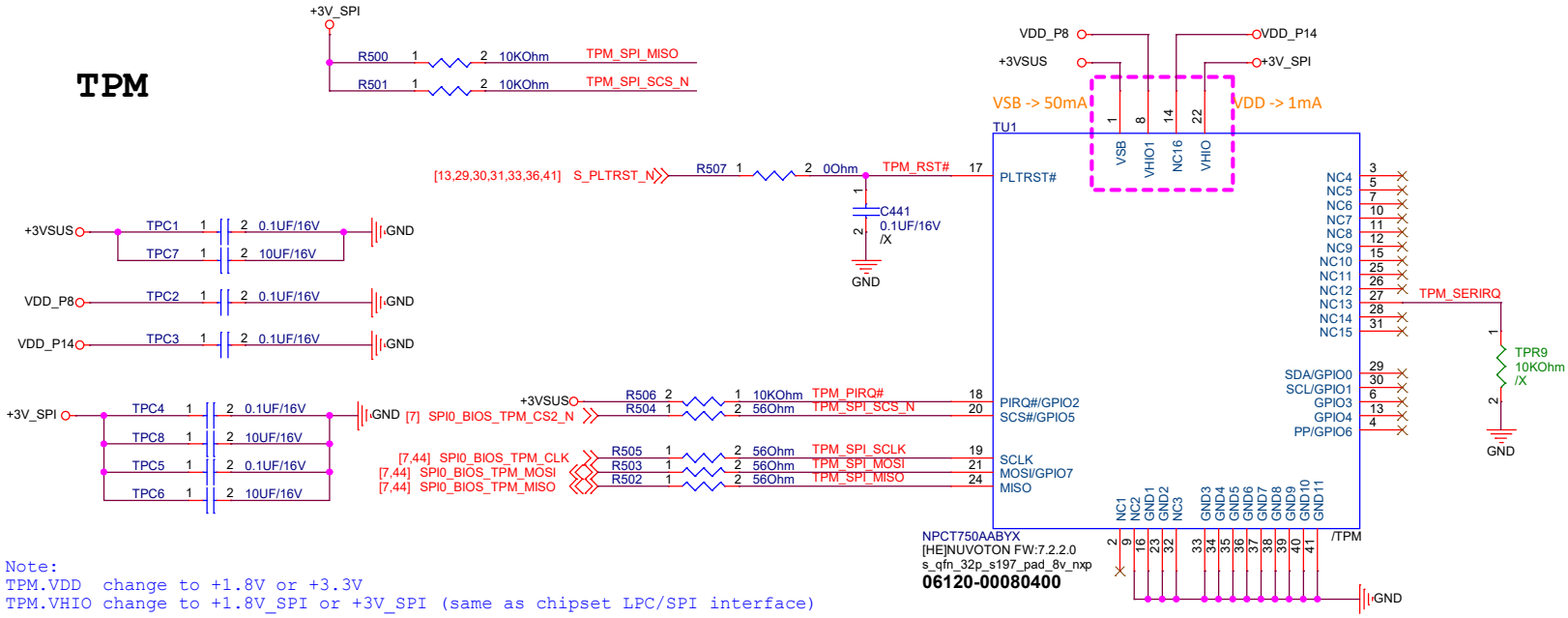
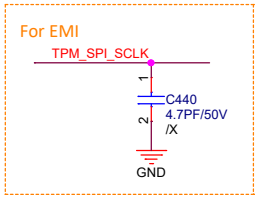
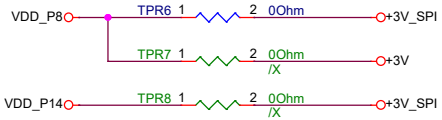
TPM



Note:
TPM.VDD change to +1.8V or +3.3V
TPM.VHIO change to +1.8V_SPI or +3V_SPI (same as chipset LPC/SPI interface)

TPM 2.0





	NPCT650	NPCT750
TPR6	x	v
TPR7	v	x
TPR8	v	x
TPR9	v	x

(Pin.18) PIRQ#
It should be connected to one of PIRQ[A:D]# of Chipset inputs

(Pin.27) SERIRQ
for LPC interface use only

(Pin.17) SPI_RST#
PCI system reset used for LPC/SPI bus (Hardware reset)

(Pin.4) PP (Physical Presense Input)
By default the PP functionality is disabled.

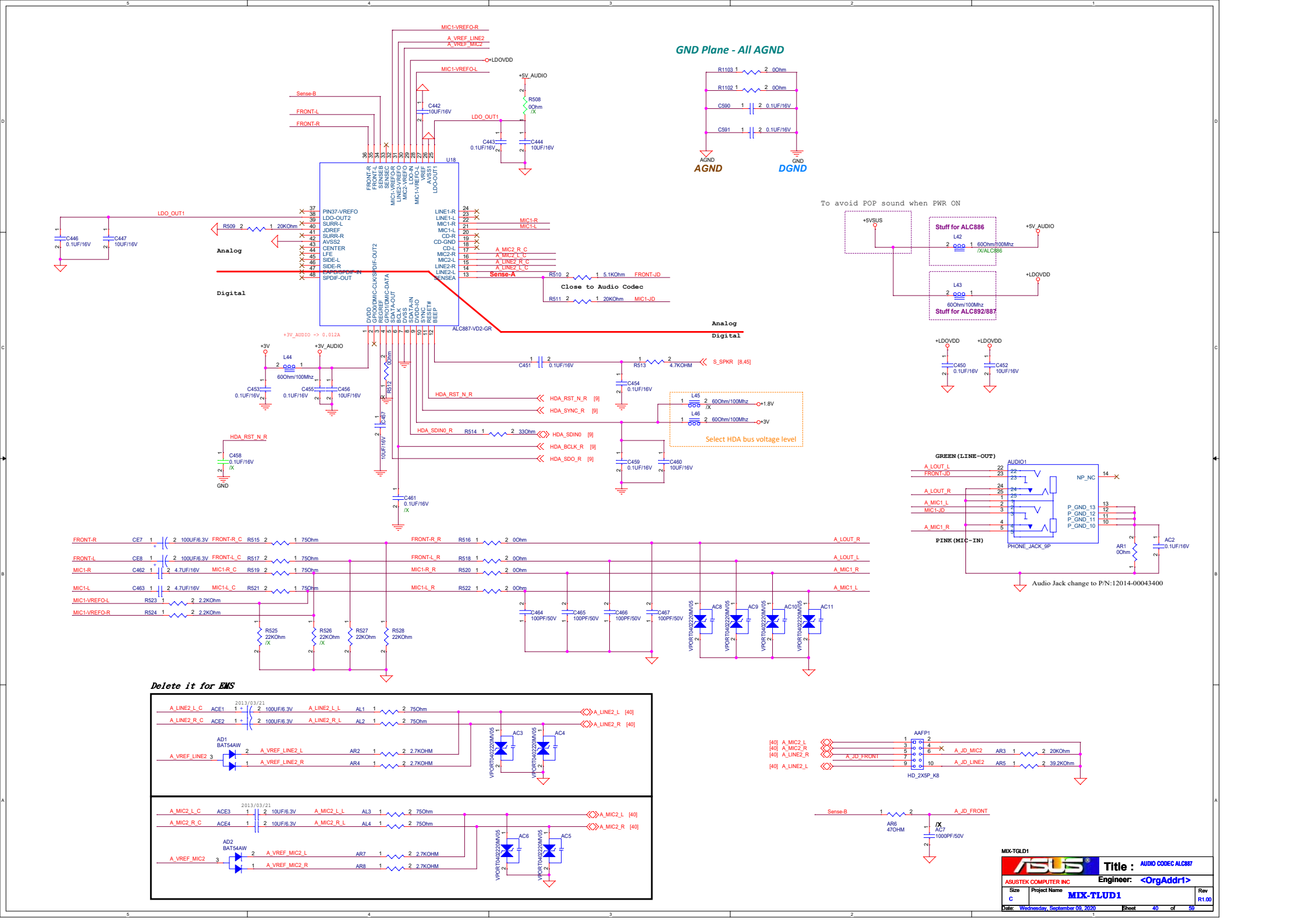
GPIO[0:6] and PP are optional.
Leave them open if not used.

GPIO[0] contact to SLP_S0# for Connected Standby, if supported.

Windows10 Hardware Compatibility Specifications for RS3
Mandatory: The TPM must support driven communication.
Mandatory: The TPM interrupt pin must be connected to an interrupt controller.

06120-00010800 NPCT650ABBYX TPM2.0 F/W:1.3.1.0
06120-00080200 NPCT750AABYX TPM2.0 F/W:7.2.1.0
06120-00080400 NPCT750AABYX TPM2.0 F/W:7.2.2.0

ASUSTek COMPUTER INC.	Title :	TPM2.0 (NPCT750AABY
	Engineer:	<OrgAddr1>
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 39 of 59	


GND Plane - All AGND
AGND
DGND
To avoid POP sound when PWR ON
Stuff for ALC886
Stuff for ALC892/887
Analog
Digital
Close to Audio Codec
Select HDA bus voltage level
GREEN(LINE-OUT)
PINK(MIC-IN)
Audio Jack change to P/N:12014-00043400
Delete it for EMS
ALC887-VD2-GR
PHONE_JACK_9P
HD_2X5P_K8
MIX-TGLD1
Title : AUDIO CODEC ALC887
ASUSTEK COMPUTER INC
Engineer: <OrgAddr1>
Project Name MIX-TLUD1
Size C
Rev R1.00
Date: Wednesday, September 09, 2020
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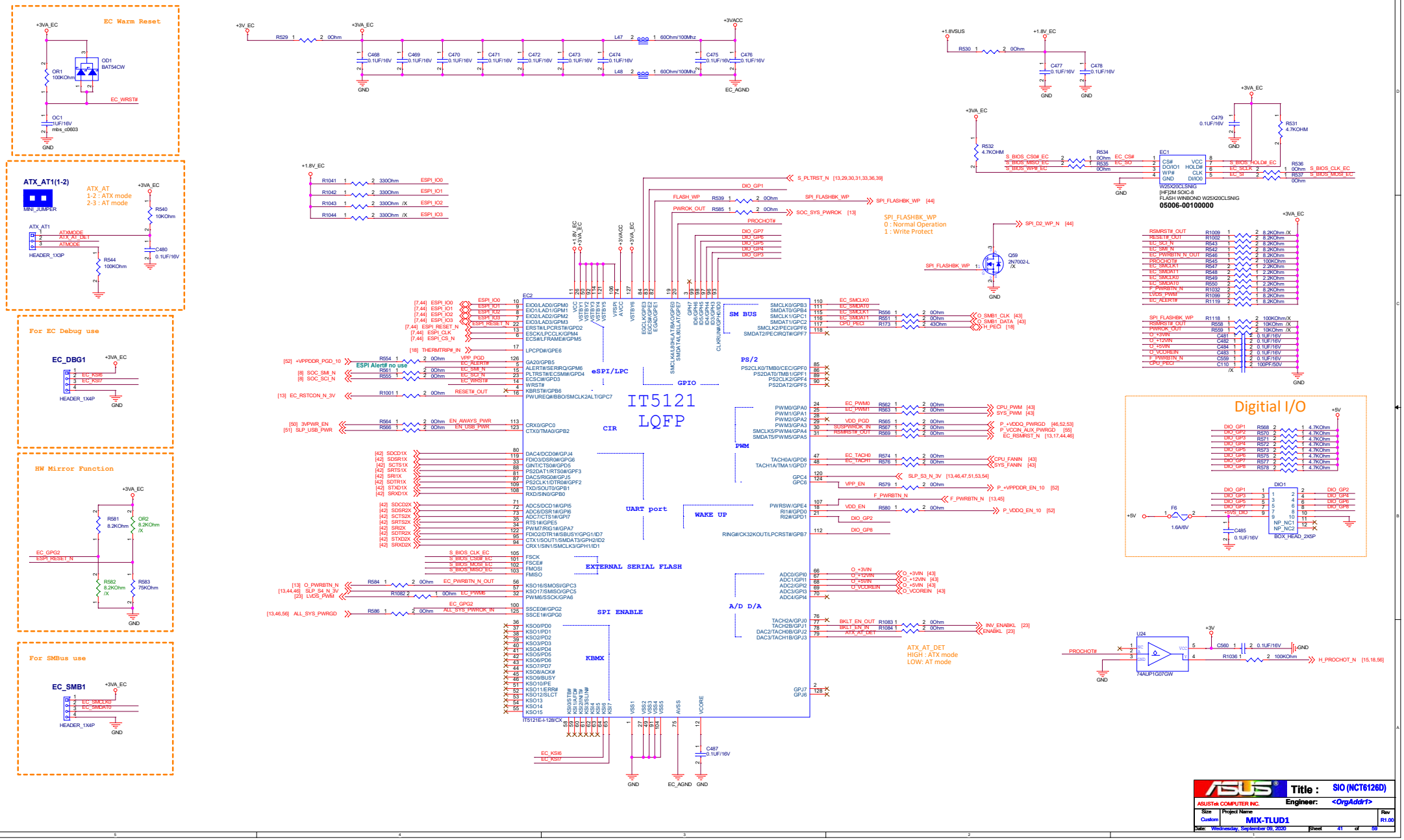

Title :	SIO (NCT6126D)		
ASUSTeK COMPUTER INC.	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: MIX-TLUD1		Rev: R1.00
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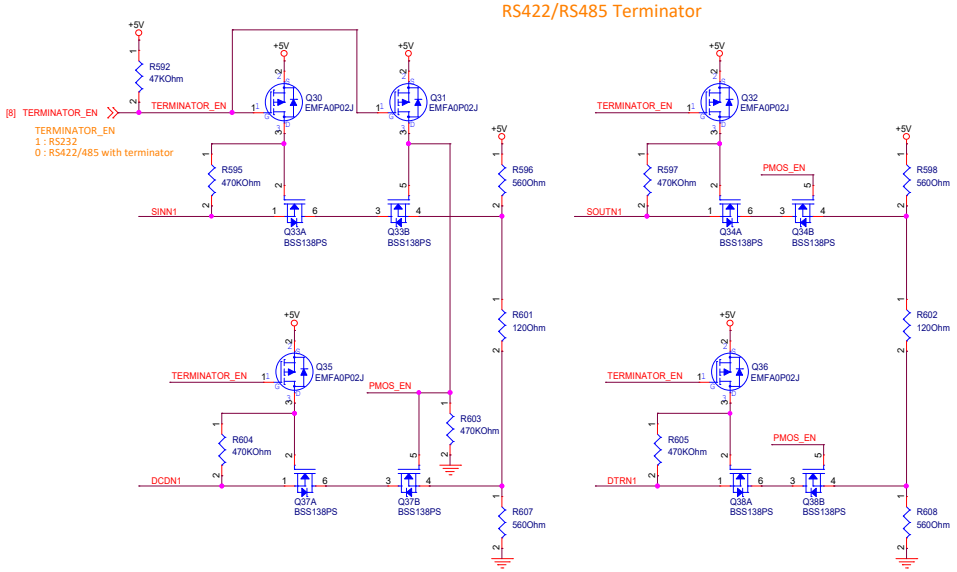
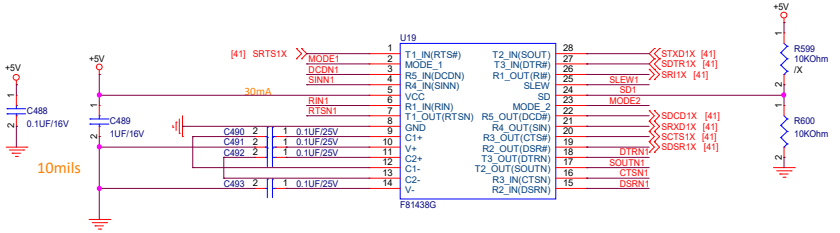
RS422/RS485 Terminator



RS-232/485/422 Pin Assignment			
Pin	RS-232	RS-485	RS-422
1	DCD	RS485_D-	RS422_TX-
2	DSR		
3	RX	RS485_D+	RS422_TX+
4	RTS		
5	TX		RS422_RX+
6	CTS		
7	DTR		RS422_RX-
8	RI		

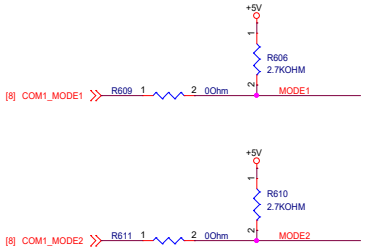
Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

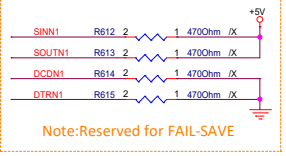


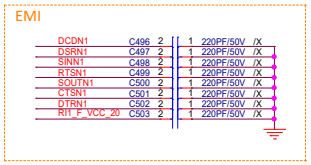
Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

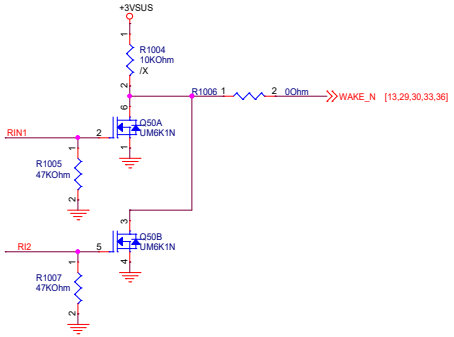
Mode_1 and Mode_2 pin. Internal pull high ≒ 625KΩ. As the current is very small (≒ 15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.



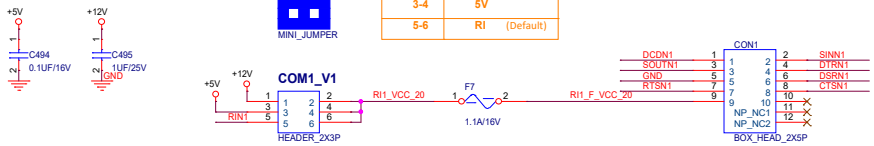




Wake on MODEM

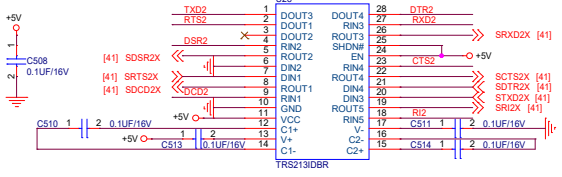


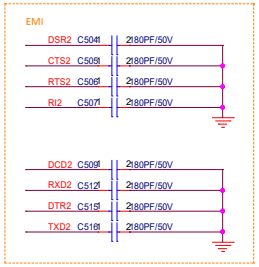
COM1

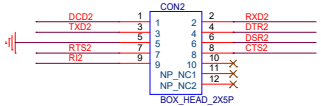


COM1_V1	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

COM2







ASUSTek COMPUTER INC.

Title : COM1/COM2

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	MIX-TLUD1	R1.00

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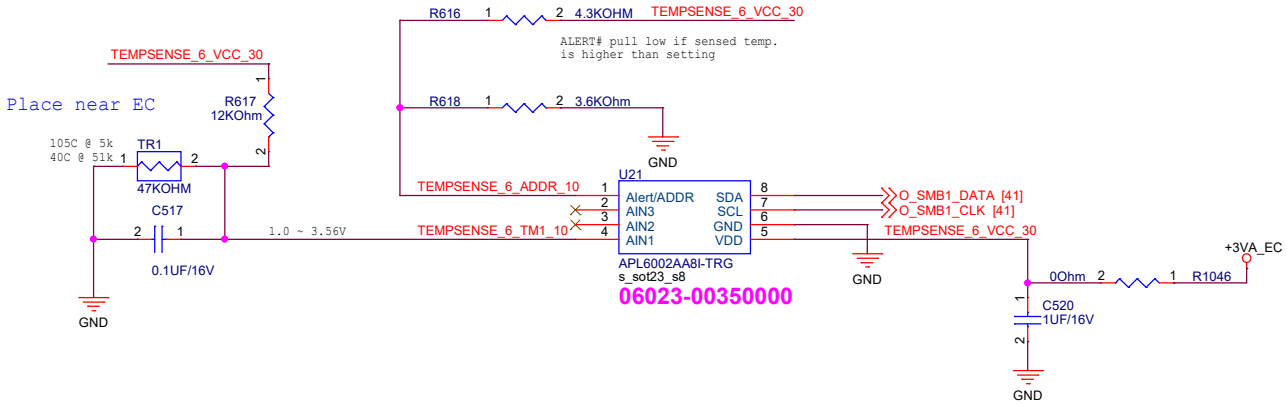
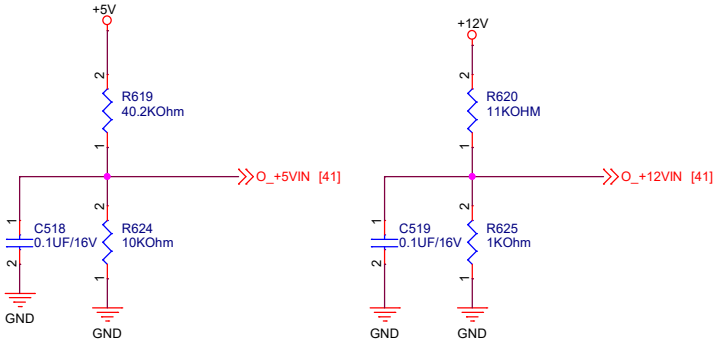
Thermal Sensor

Address Selection Table

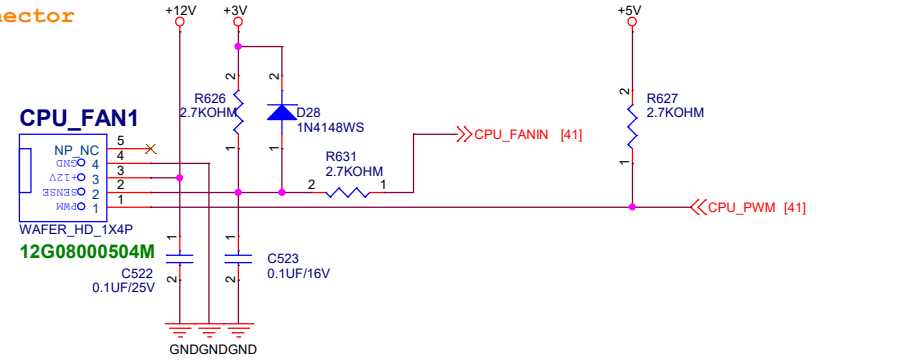
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
OR172	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
OR173	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

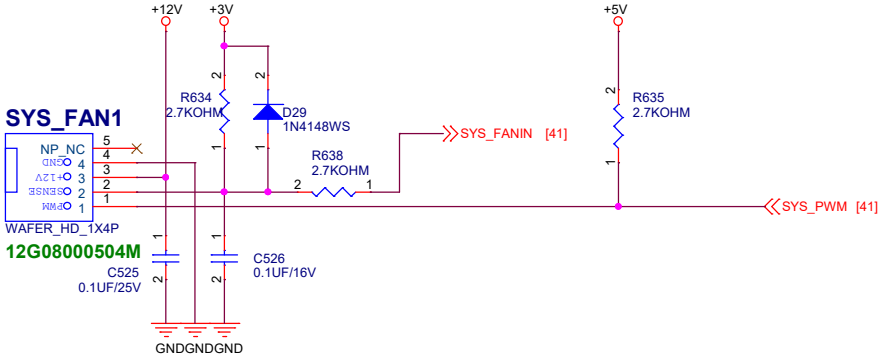


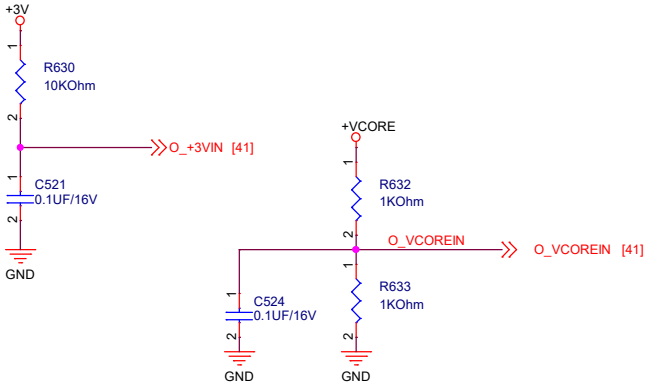
Voltage Monitor



FAN Connector

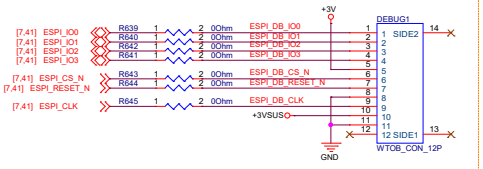






ASUSTek COMPUTER INC.	Title : HW monitor/FAN/Sensor	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 43 of 59	

DEBUG PORT

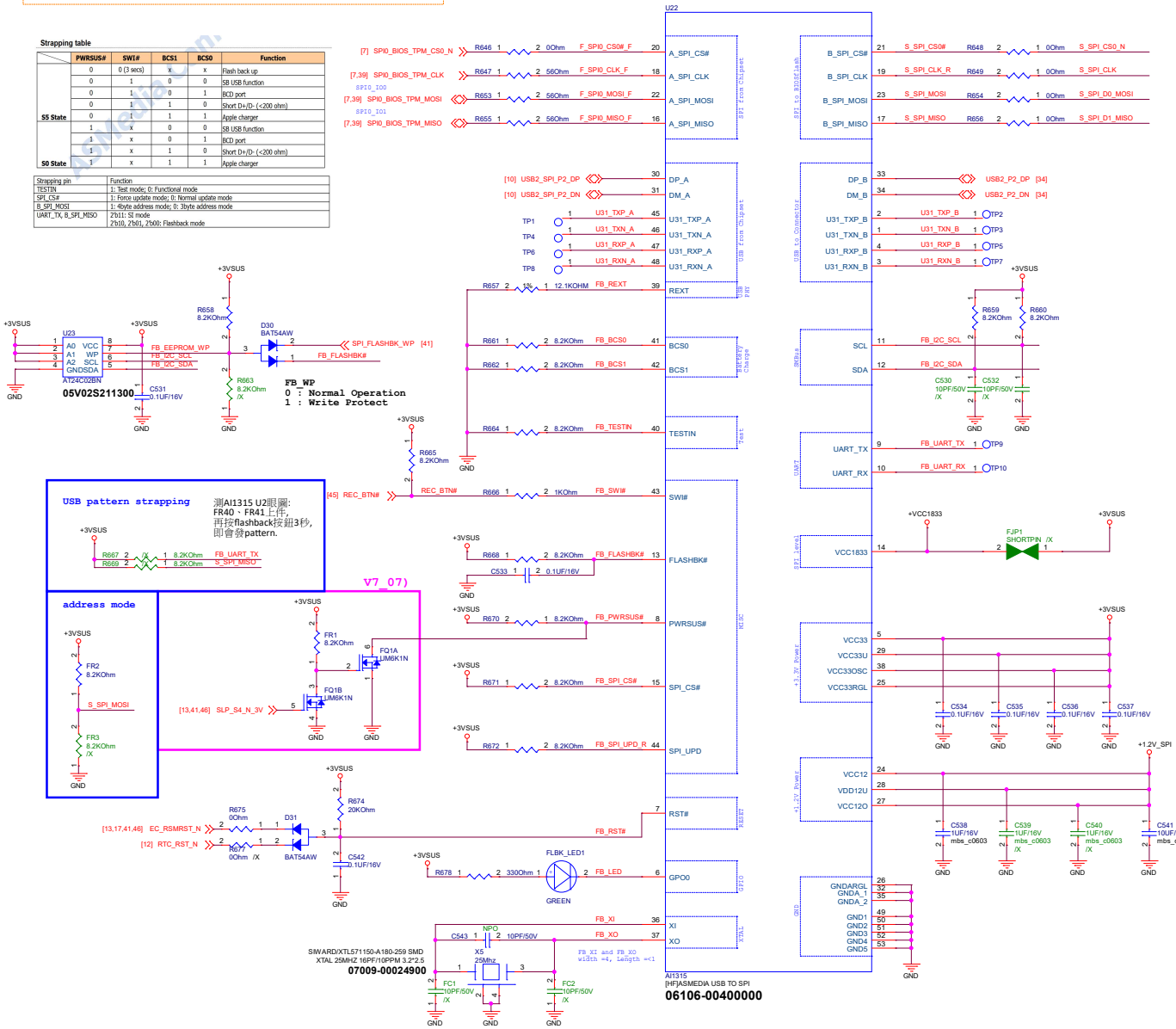


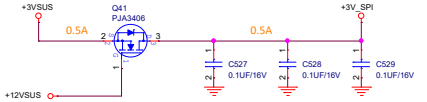
SPI Interface

Strapping table

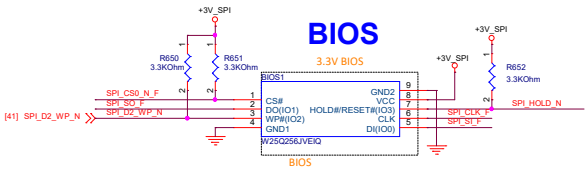
	PWRSUS#	SWI#	BCS1	BCS0	Function
	0	0 (3 secs)	x	x	Flash back up
	0	1	0	0	SB USB function
	0	1	0	1	BCD port
	0	1	1	0	Short D+/D- (<200 ohm)
S5 State	0	1	1	1	Apple charger
	1	x	0	0	SB USB function
	1	x	0	1	BCD port
	1	x	1	0	Short D+/D- (<200 ohm)
S0 State	1	x	1	1	Apple charger

Strapping pin	Function
TESTIN	1: Test mode; 0: Functional mode
SPI_CS#	1: Force update mode; 0: Normal update mode
B_SPI_MOSI	1: 4byte address mode; 0: 3byte address mode
UART_TX, B_SPI_MISO	2'b11: SI mode 2'b10, 2'b01, 2'b00: Flashback mode

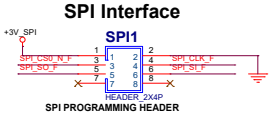


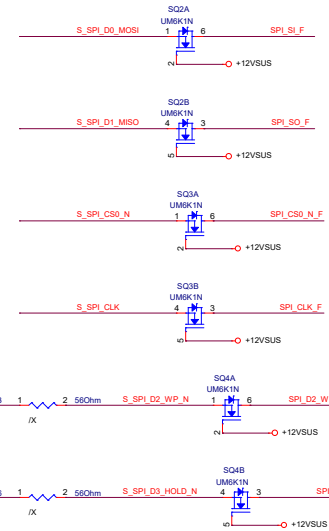


BIOS



SPI Interface





MIX-TGLD1

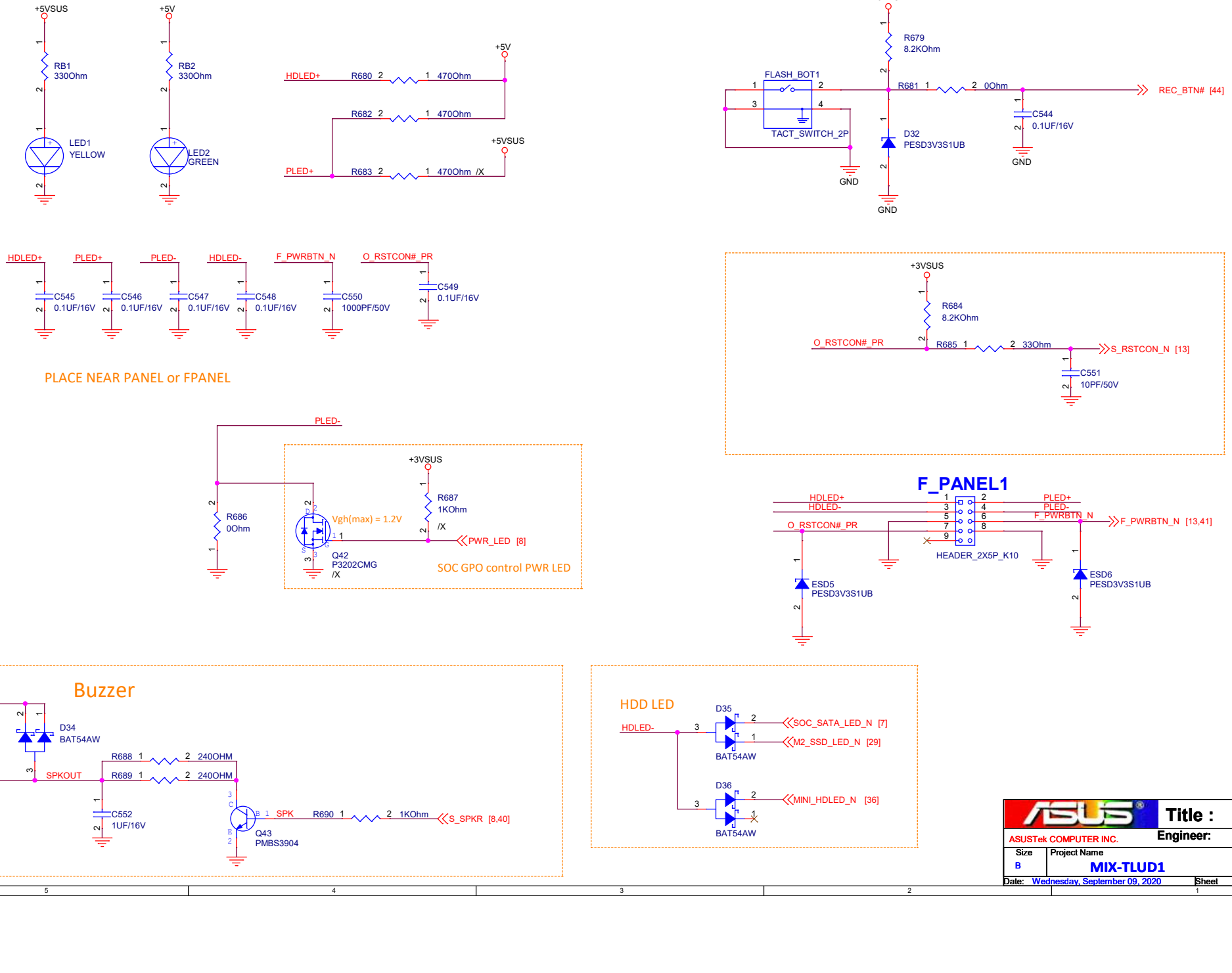
ASUSTeK COMPUTER INC.

Title : BIOS and DEBUG

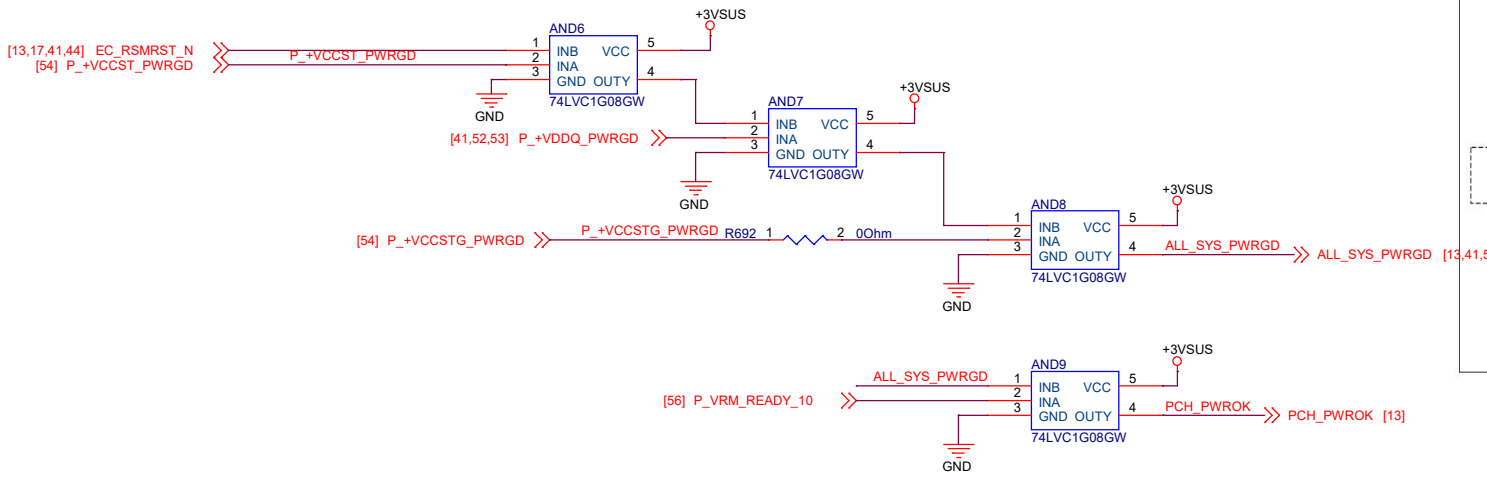
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	MIX-TLUD1	R1.00

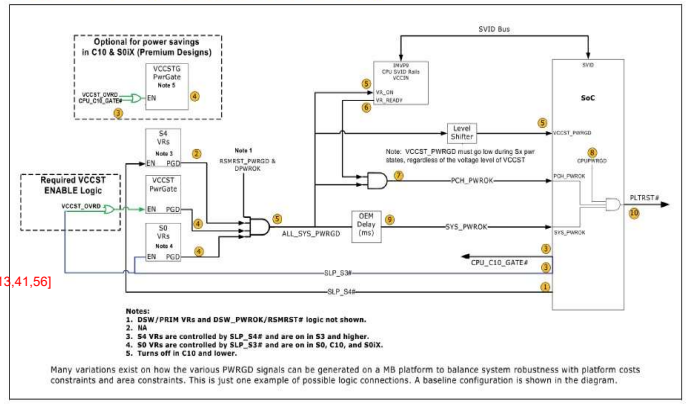
Date: Wednesday, September 09, 2020 Sheet 44 of 59


+5VSUS
RB1
330Ohm
LED1
YELLOW
+5V
RB2
330Ohm
LED2
GREEN
HDLED+
R680 2 1 470Ohm
+5V
R682 2 1 470Ohm
+5VSUS
PLED+
R683 2 1 470Ohm /X
+3VSUS
R679
8.2KOhm
FLASH_BOT1
TACT_SWITCH_2P
R681 1 2 0Ohm
REC_BTN# [44]
C544
0.1UF/16V
GND
D32
PESD3V3S1UB
GND
HDLED+
PLED+
PLED-
HDLED-
F_PWRBTN_N
O_RSTCON#_PR
C545 0.1UF/16V
C546 0.1UF/16V
C547 0.1UF/16V
C548 0.1UF/16V
C550 1000PF/50V
C549 0.1UF/16V
PLACE NEAR PANEL or FPANEL
+3VSUS
R684
8.2KOhm
O_RSTCON#_PR
R685 1 2 33Ohm
S_RSTCON_N [13]
C551
10PF/50V
PLED-
+3VSUS
R686
0Ohm
Vgh(max) = 1.2V
R687
1KOhm
/X
PWR_LED [8]
Q42
P3202CMG
/X
SOC GPO control PWR LED
F_PANEL1
HDLED+
HDLED-
O_RSTCON#_PR
PLED+
PLED-
F_PWRBTN_N
F_PWRBTN_N [13,41]
HEADER_2X5P_K10
ESD5
PESD3V3S1UB
ESD6
PESD3V3S1UB
+5V
Buzzer
D34
BAT54AW
BZ1
2731Hz
SPKOUT
R688 1 2 240OHM
R689 1 2 240OHM
C552
1UF/16V
SPK
R690 1 2 1KOhm
S_SPKR [8,40]
Q43
PMBS3904
HDD LED
HDLED-
D35
SOC_SATA_LED_N [7]
M2_SSD_LED_N [29]
BAT54AW
D36
MINI_HDLED_N [36]
BAT54AW
Title : Front panel
ASUSTek COMPUTER INC.
Engineer: <OrgAddr1>
Size B
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
Sheet 45 of 59

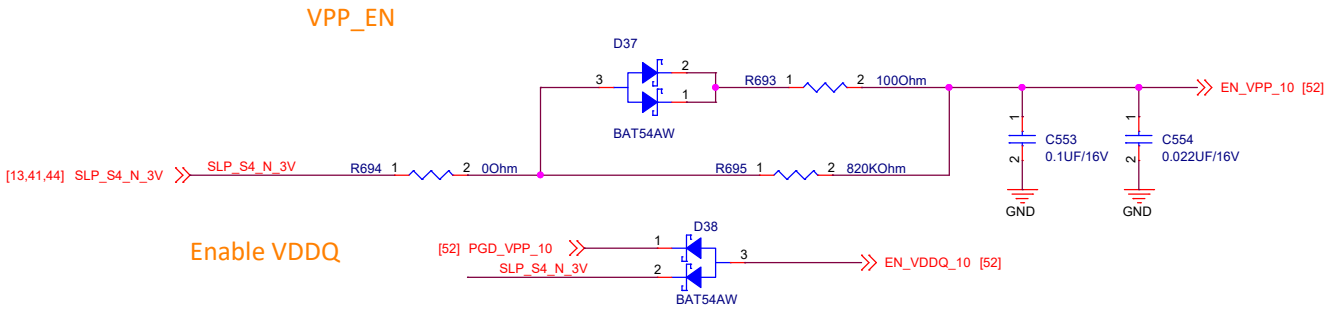
Tiger Lake PWROK Sequence



Premium PWROK Generation Flow Diagram



PWR DDR4 Power Sequence

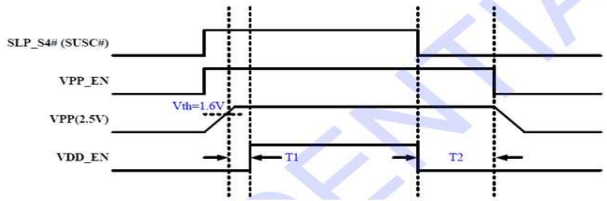


11.21 DDR4 Power Control Specification

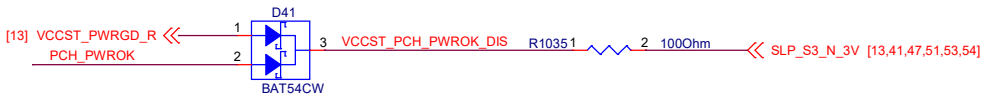
Table 11-5. DDR4Timings Parameter

Symbol	Typ.	Description
T_1	5ms	The rising edge of VPP(2.5V) to rising edge of VDD_EN
T_2	50ms	The falling edge of VDD_EN to rising edge of VPP(2.5V)

Figure11-27. DDR4 Power Control Timings



Power Down Sequence



MIX-TGLD1

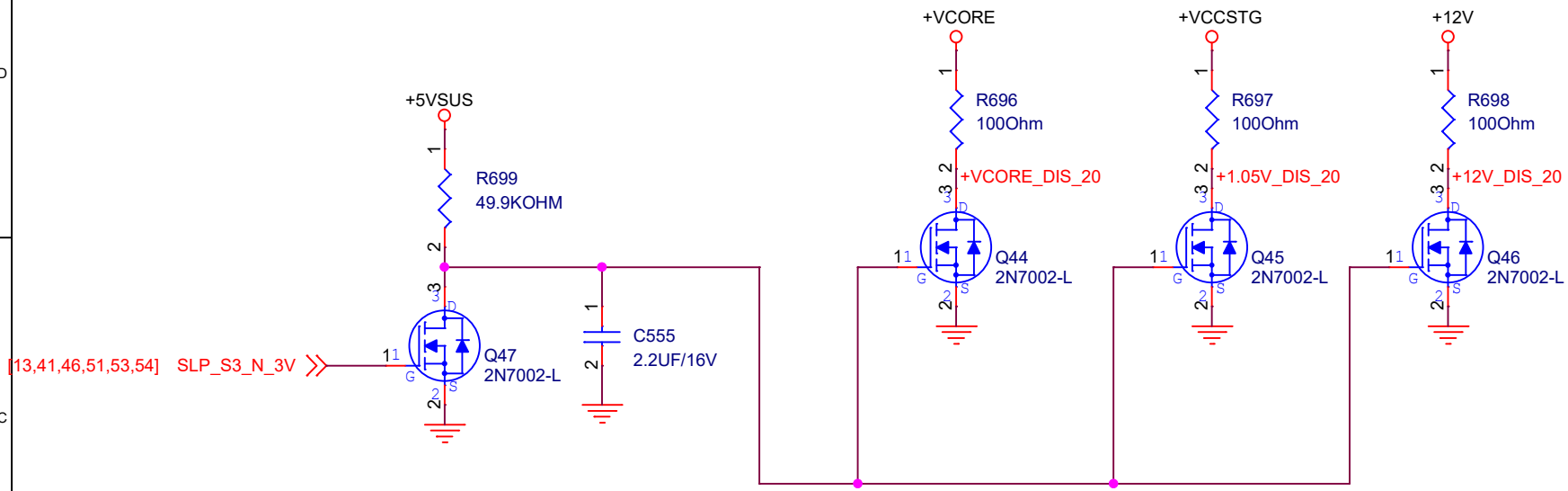
ASUSTek COMPUTER INC.

Title : DDR4/PWROK_SEQUENCE

Engineer: <OrgAddr1>

Size	Project Name	Rev
B	MIX-TLUD1	R1.10

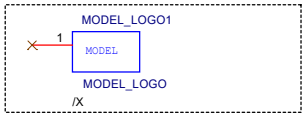
Date: Wednesday, September 09, 2020 Sheet 46 of 59

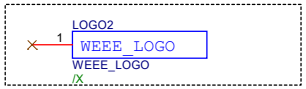


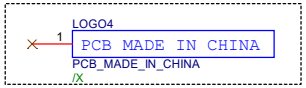
ASUSTek COMPUTER INC.	Title : Discharge circuit	
	Engineer: <OrgAddr1>	
Size: A	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 47 of 59	

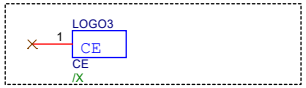
Logo

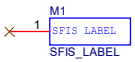
common Logo for all projects

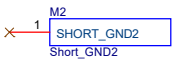


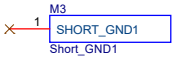


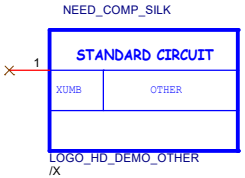










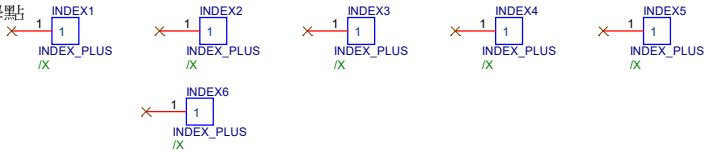


Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

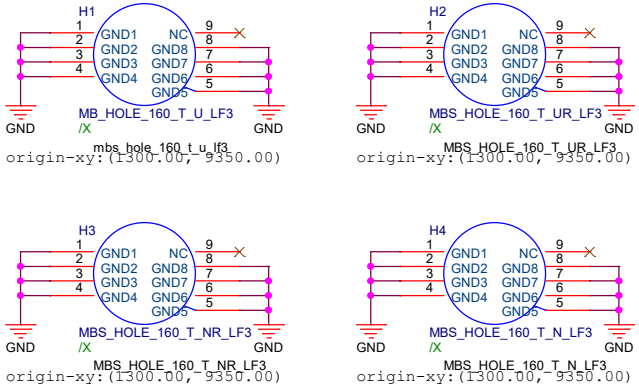
大顆十字光學點

小顆十字光學點



MIX-TGLD1

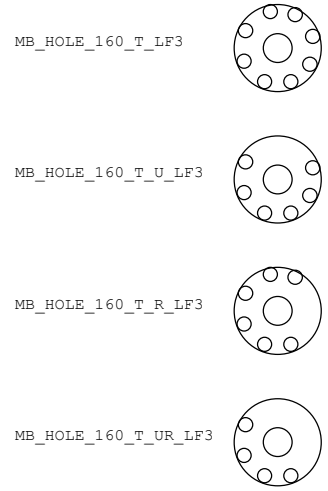
ASUSTek COMPUTER INC.	Title : Selling Point_Logo	
	Engineer: <OrgAddr1>	
Size: A3	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 48 of 59	



m-ATX Screw Select

	Standard (9.6 x 9.6)	Scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H20	V	V

MB SCREW FOOTPRINT



PCB1

PCB

MIX-TLUD1

08001-16030000

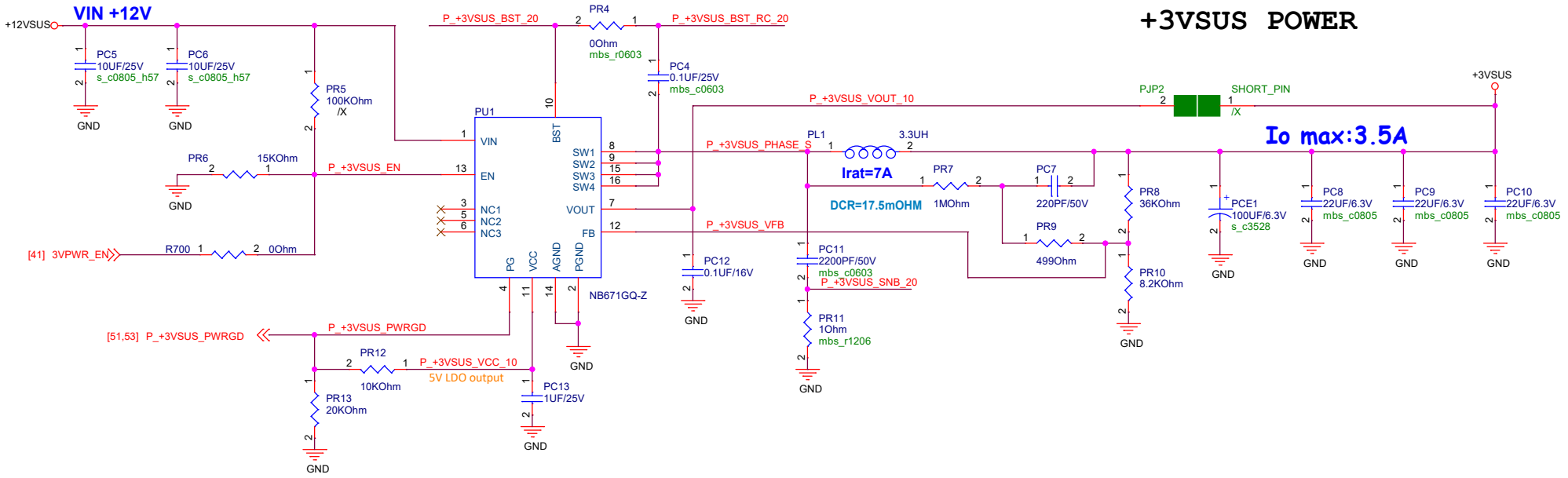
ASUSTek COMPUTER INC.

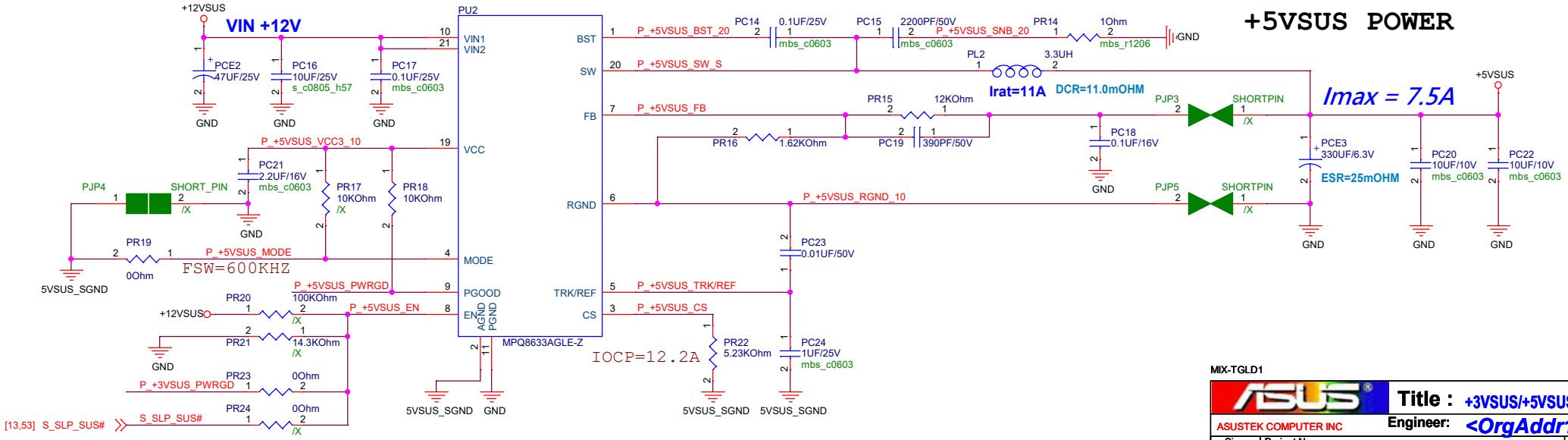
Title : Screw Hole

Engineer: <OrgAddr1>

Size	Project Name	Rev
B	MIX-TLUD1	R1.00

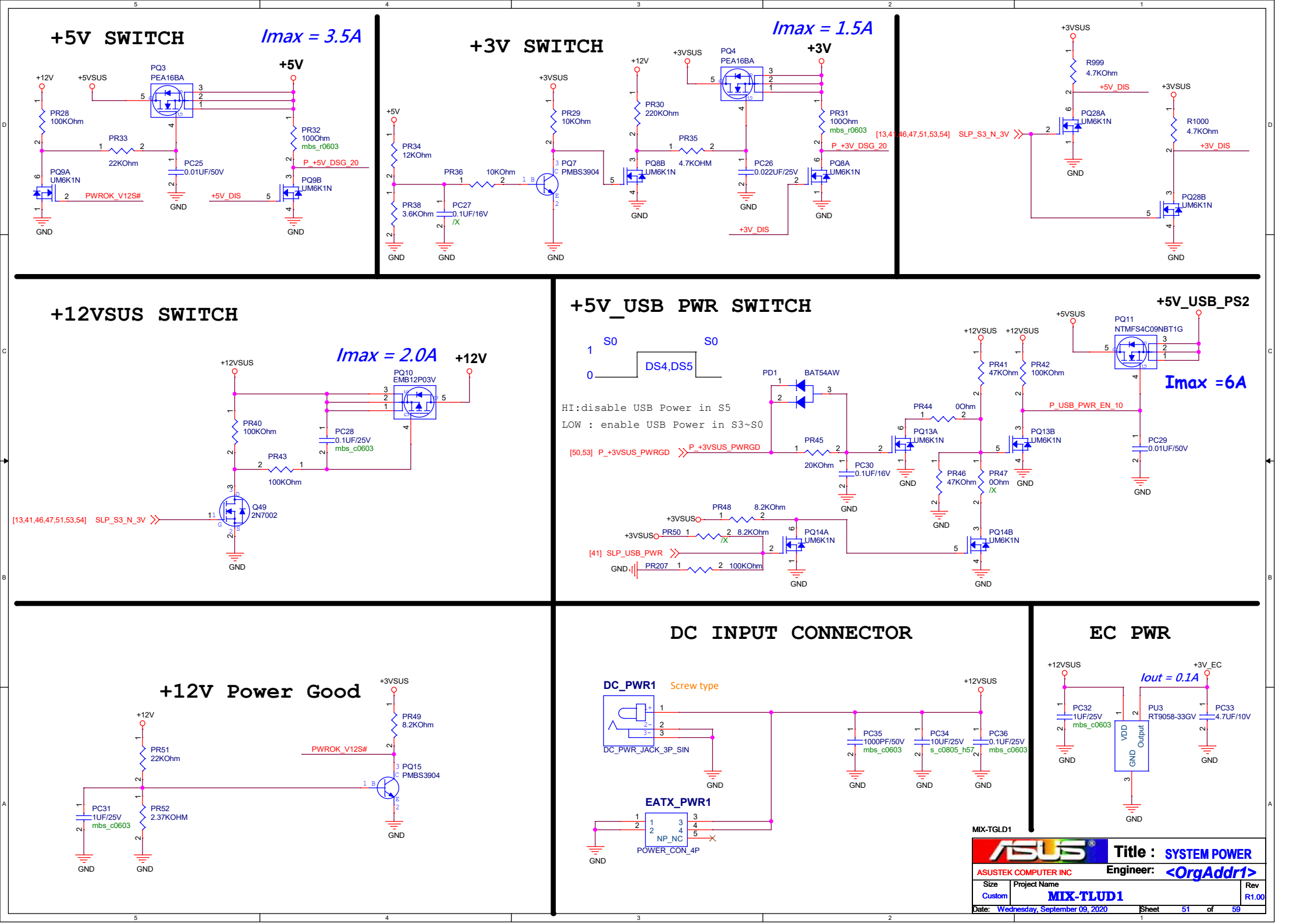
Date: Wednesday, September 09, 2020 Sheet 49 of 59





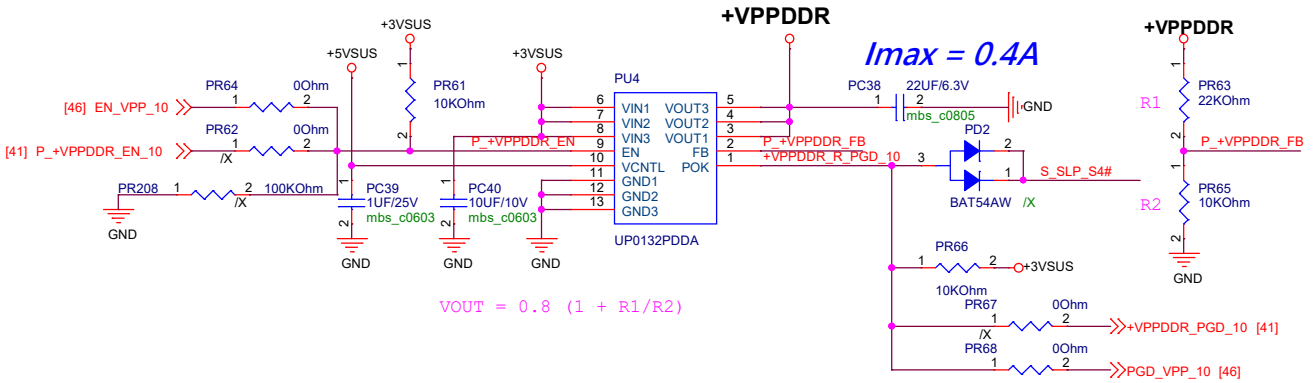
MIX-TGLD1

ASUSTEK COMPUTER INC	Title : +3VSUS/+5VSUS	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 50 of 59	

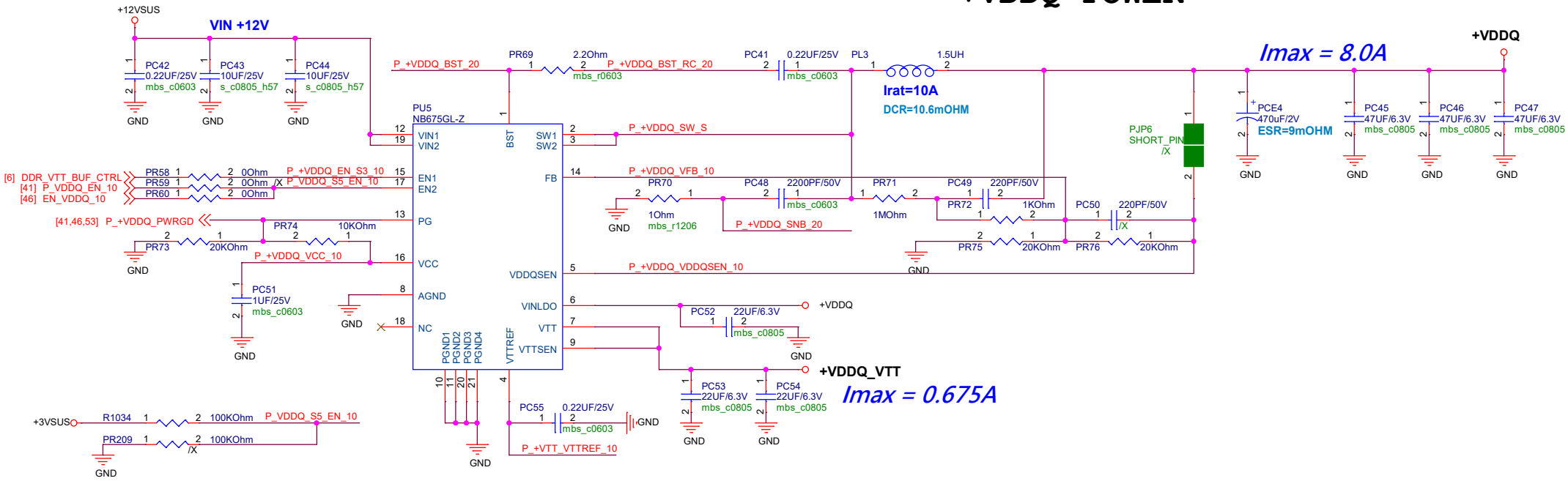

+5V SWITCH
Imax = 3.5A
+12V
+5VSUS
PQ3
PEA16BA
+5V
PR28
100KOhm
PR33
22KOhm
PC25
0.01UF/50V
PQ9A
UM6K1N
PWROK_V12S#
+5V_DIS
PR32
100Ohm
mbs_r0603
P_+5V_DSG_20
PQ9B
UM6K1N
GND
+3V SWITCH
Imax = 1.5A
+5V
+3VSUS
+12V
PQ4
PEA16BA
+3V
PR34
12KOhm
PR36
10KOhm
PR38
3.6KOhm
PC27
0.1UF/16V
/X
PQ7
PMBS3904
PR29
10KOhm
PR30
220KOhm
PR35
4.7KOHM
PQ8B
UM6K1N
PC26
0.022UF/25V
PQ8A
UM6K1N
PR31
100Ohm
mbs_r0603
P_+3V_DSG_20
+3V_DIS
R999
4.7KOhm
+5V_DIS
PQ28A
UM6K1N
[13,41,46,47,51,53,54] SLP_S3_N_3V
R1000
4.7KOhm
+3V_DIS
PQ28B
UM6K1N
+12VSUS SWITCH
Imax = 2.0A
+12V
+12VSUS
PQ10
EMB12P03V
PR40
100KOhm
PR43
100KOhm
PC28
0.1UF/25V
mbs_c0603
Q49
2N7002
[13,41,46,47,51,53,54] SLP_S3_N_3V
+5V_USB PWR SWITCH
+5V_USB_PS2
S0
S0
1
0
DS4,DS5
HI:disable USB Power in S5
LOW : enable USB Power in S3~S0
PD1
BAT54AW
[50,53] P_+3VSUS_PWRGD
PR45
20KOhm
PC30
0.1UF/16V
PR44
0Ohm
PQ13A
UM6K1N
PR41
47KOhm
PR42
100KOhm
PQ13B
UM6K1N
PR46
47KOhm
PR47
0Ohm
/X
P_USB_PWR_EN_10
PC29
0.01UF/50V
PQ11
NTMFS4C09NBT1G
Imax =6A
PR48
8.2KOhm
PR50
8.2KOhm
/X
[41] SLP_USB_PWR
PR207
100KOhm
PQ14A
UM6K1N
PQ14B
UM6K1N
+12V Power Good
+12V
+3VSUS
PR51
22KOhm
PR52
2.37KOHM
PC31
1UF/25V
mbs_c0603
PWROK_V12S#
PR49
8.2KOhm
PQ15
PMBS3904
DC INPUT CONNECTOR
DC_PWR1
Screw type
DC_PWR_JACK_3P_SIN
PC35
1000PF/50V
mbs_c0603
PC34
10UF/25V
s_c0805_h57
PC36
0.1UF/25V
mbs_c0603
EATX_PWR1
NP_NC
POWER_CON_4P
EC PWR
+12VSUS
+3V_EC
Iout = 0.1A
PC32
1UF/25V
mbs_c0603
PU3
RT9058-33GV
VDD
Output
GND
PC33
4.7UF/10V
MIX-TGLD1
Title : SYSTEM POWER
ASUSTEK COMPUTER INC
Engineer: <OrgAddr1>
Size
Custom
Project Name
MIX-TLUD1
Rev
R1.00
Date: Wednesday, September 09, 2020
Sheet 51 of 59

S3 And S5 Truth Table

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off
OTHERS	Hi	Low	Off	Off	Off



+VDDQ POWER



MIX-TGLD1

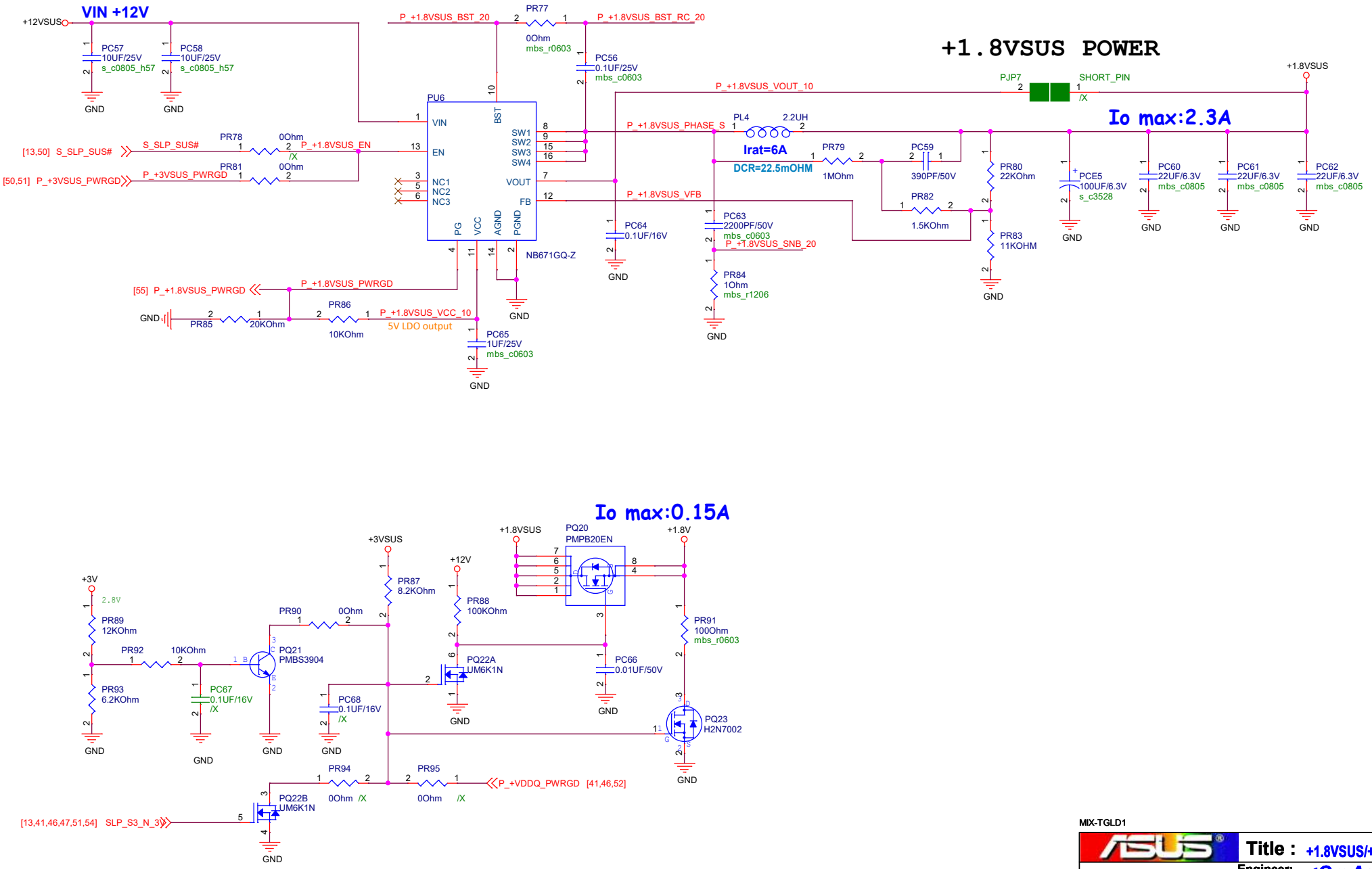
ASUSTEK COMPUTER INC

Title : +VDDQ/+VPPDDR

Engineer: <OrgAddr1>

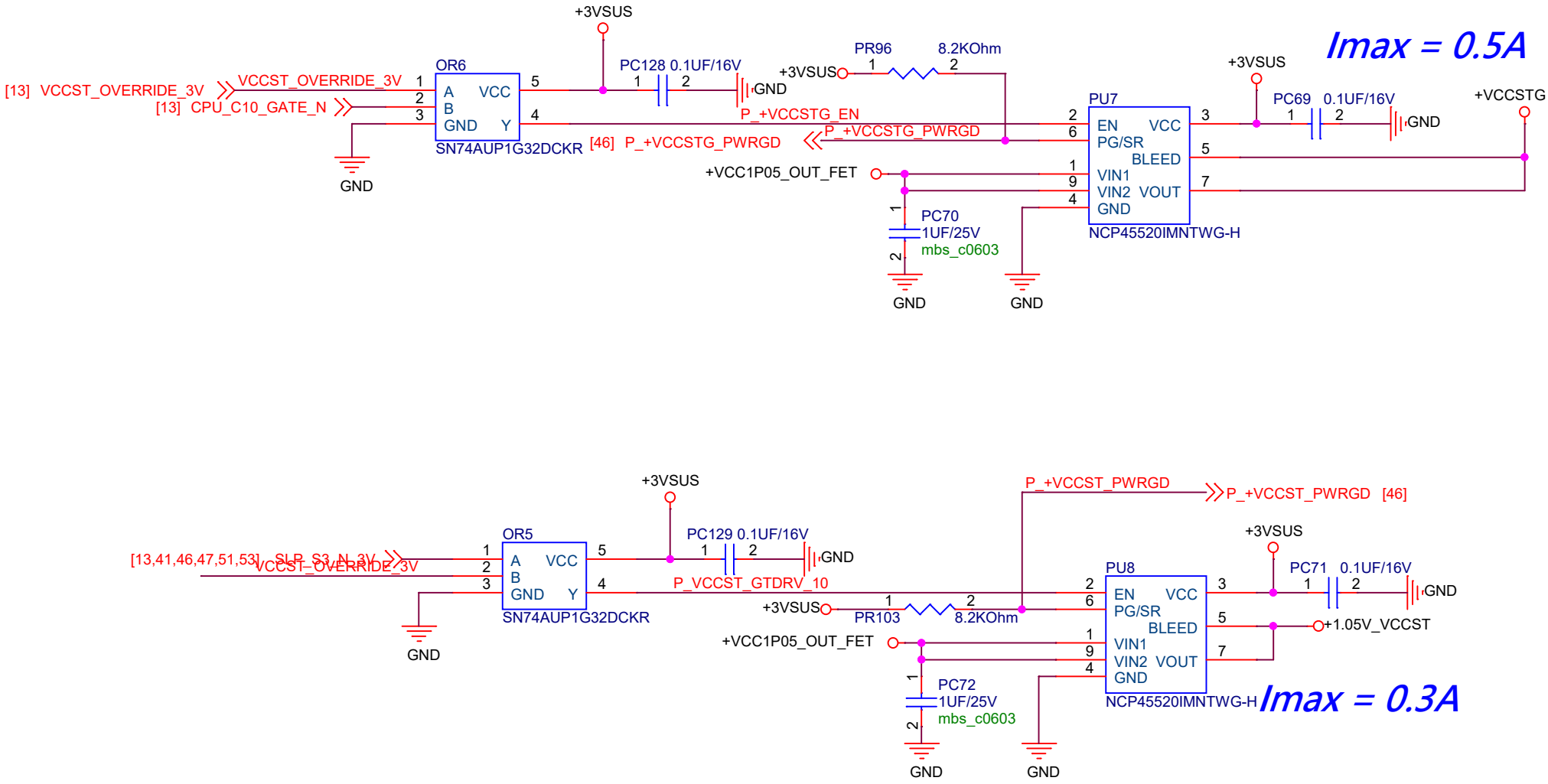
Size	Project Name	Rev
B	MIX-TLUD1	R1.00

Date: Wednesday, September 09, 2020 Sheet 52 of 59



MIX-TGLD1

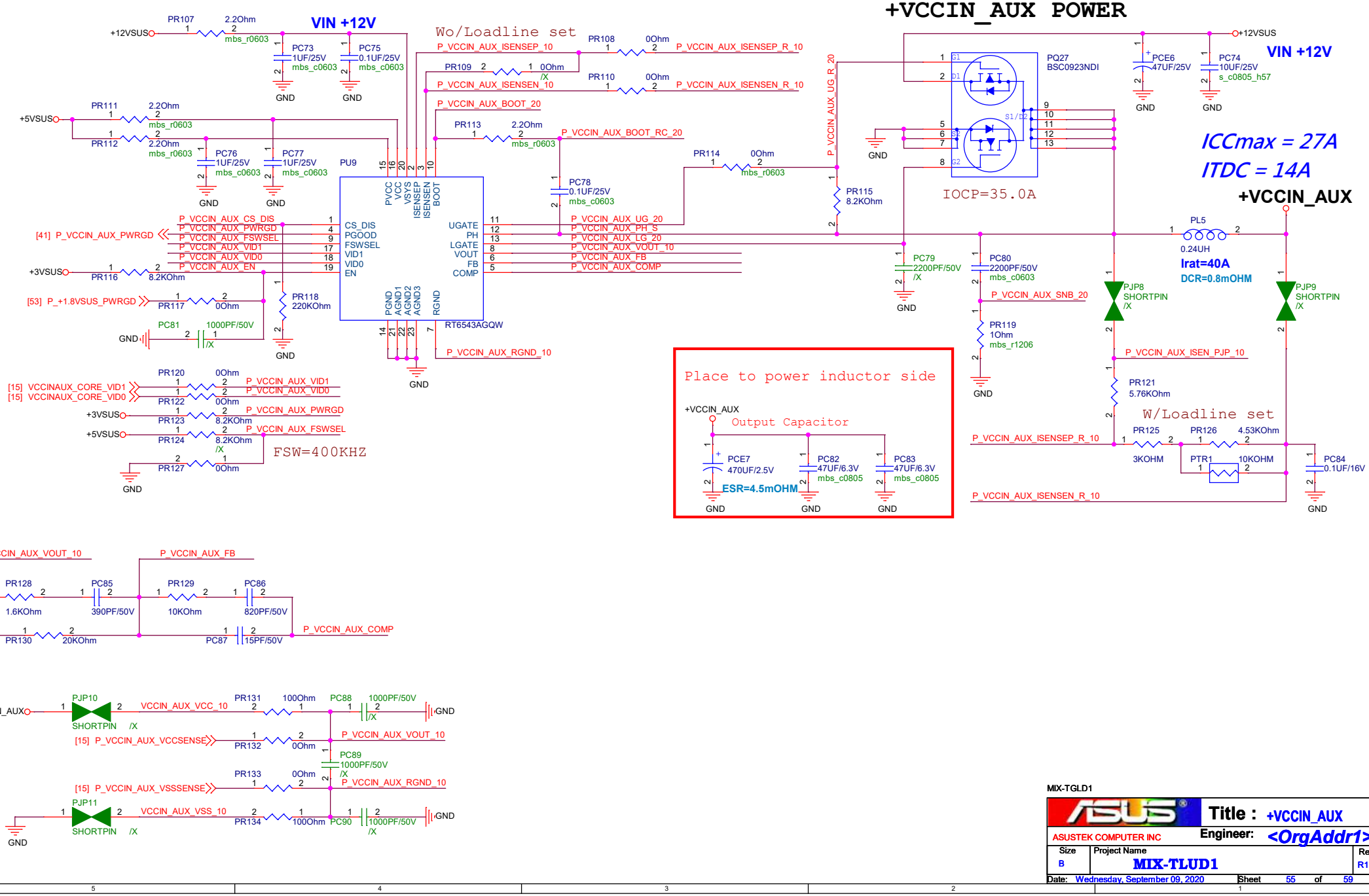
ASUSTEK COMPUTER INC	Title : +1.8VSUS/+1.8V	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 53 of 59	



MIX-TGLD1

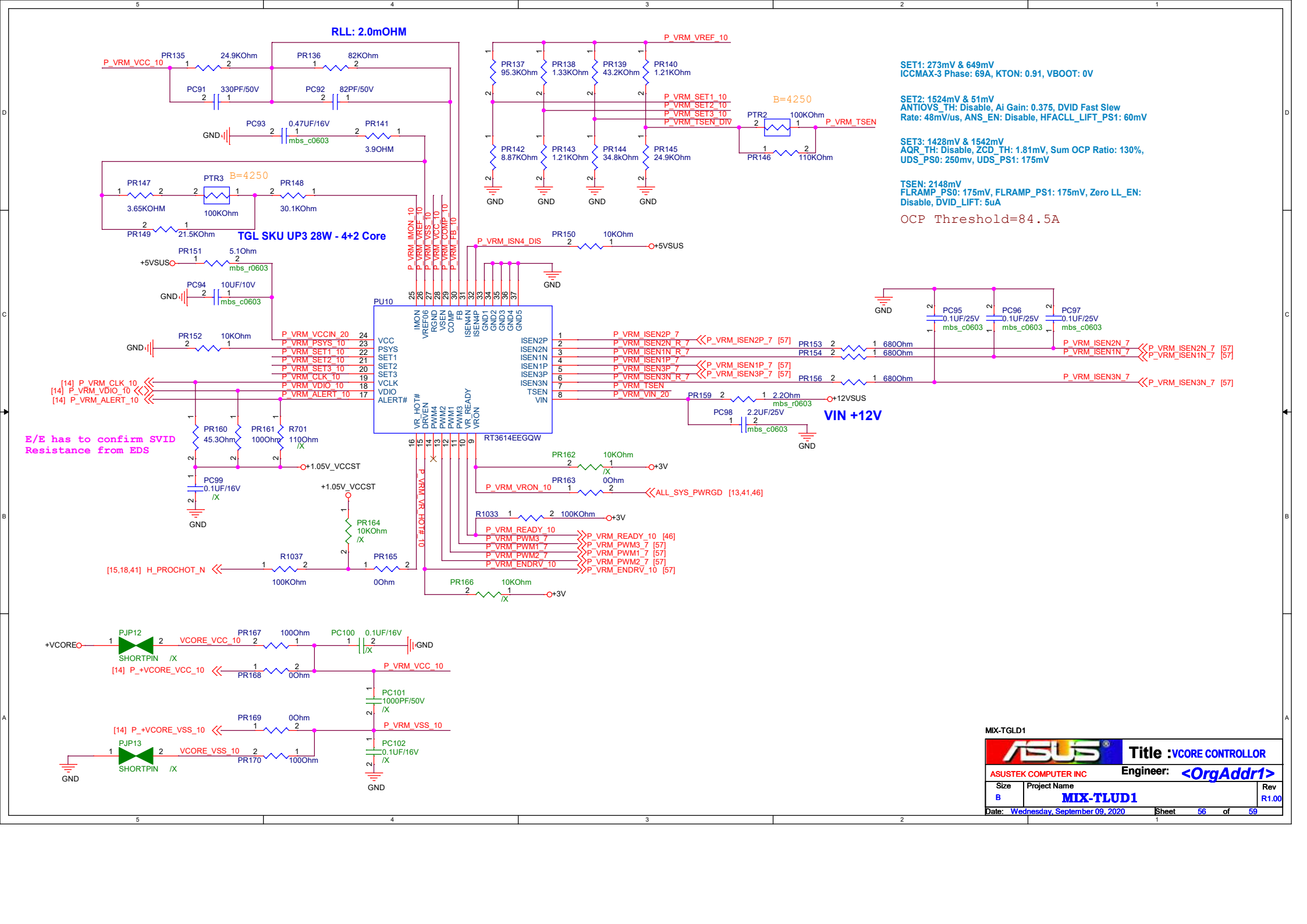
ASUSTEK COMPUTER INC	Title : +VCCSTG/+VCCST	
	Engineer: <OrgAddr1>	
Size: A	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 54 of 59	

+VCCIN_AUX POWER



MIX-TGLD1

ASUSTEK COMPUTER INC	Title : +VCCIN_AUX	
	Engineer: <OrgAddr1>	
Size: B	Project Name: MIX-TLUD1	Rev: R1.00
Date: Wednesday, September 09, 2020	Sheet 55 of 59	


RLL: 2.0mOHM
TGL SKU UP3 28W - 4+2 Core
SET1: 273mV & 649mV
ICCMAX-3 Phase: 69A, KTON: 0.91, VBOOT: 0V
SET2: 1524mV & 51mV
ANTIOVS_TH: Disable, Ai Gain: 0.375, DVID Fast Slew
Rate: 48mV/us, ANS_EN: Disable, HFACLL_LIFT_PS1: 60mV
SET3: 1428mV & 1542mV
AQR_TH: Disable, ZCD_TH: 1.81mV, Sum OCP Ratio: 130%,
UDS_PS0: 250mv, UDS_PS1: 175mV
TSEN: 2148mV
FLRAMP_PS0: 175mV, FLRAMP_PS1: 175mV, Zero LL_EN:
Disable, DVID_LIFT: 5uA
OCP Threshold=84.5A
VIN +12V
E/E has to confirm SVID
Resistance from EDS
RT3614EEGQW
MIX-TGLD1
Title :VCORE CONTROLLOR
ASUSTEK COMPUTER INC
Engineer: <OrgAddr1>
Project Name
MIX-TLUD1
Size
B
Rev
R1.00
Date: Wednesday, September 09, 2020
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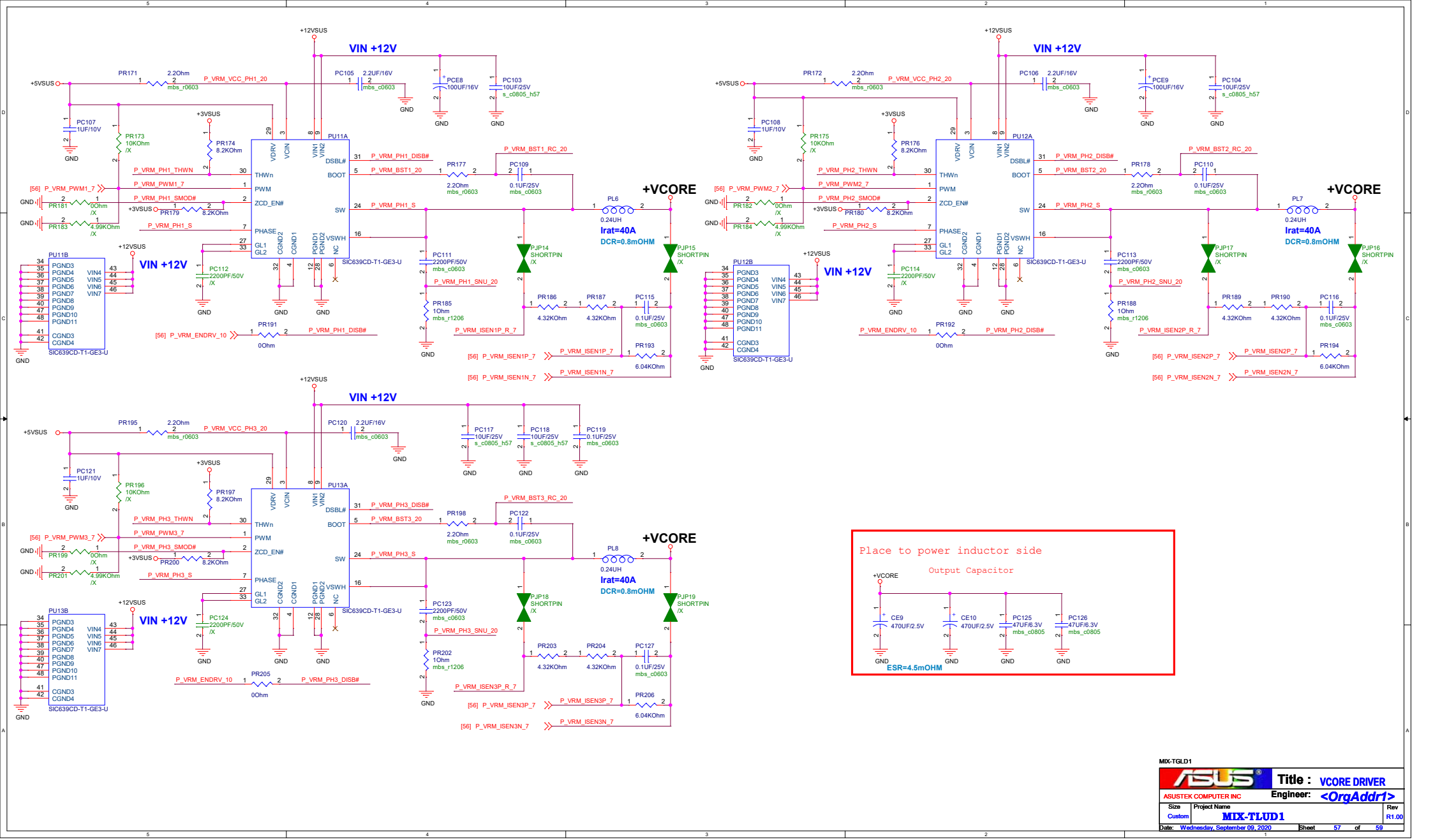
VIN +12V
+VCORE
Irat=40A
DCR=0.8mOHM
SIC639CD-T1-GE3-U
Place to power inductor side
Output Capacitor
ESR=4.5mOHM
MIX-TGLD1
Title : VCORE DRIVER
ASUSTEK COMPUTER INC
Engineer: <OrgAddr1>
Project Name MIX-TLUD1
Rev R1.00
Date: Wednesday, September 09, 2020
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MIX-TGLD1 Power Budget

Name	VccIN	VccIN_AUX	VDD2	VTT	VccST	VccSTG	VCCPRIM_1P8	VCCPRIM_3P3	VCCDSW_3P3	5V_USB_PS2	3VSUS	12V	5V	3V	+1.1V_HDMI1	1.5V
Power Voltage	2V	1.8V	1.2V	0.6V	1.05V	1.05V	1.8V	3.3V	3.3V	5V	3V	12V	5V	3V	1.1V	1.5V
TGL PU3+PCH	65	27	1.5		0.3	0.5	1.3	0.202	0.008							
DDR4 (SO-DIMM) DIMM_A1			5.2	0.4												
DDR3 (SO-DIMM) DIMM_B1			5.2	0.4												
LAN I219											0.3					
LAN I210/I211											1.3					
USB2.0 x9										4.5						
USB3.0 x4										6						
HDMI (SN75DP159) x2														0.084	0.46	
FAN x2												2				
PCIE x4 slot											0.375	2.1		3		
M.2 M-key (2280)														0.4		
Mini PCI-E Card											2.75					0.5
STAT Power												1.5	1.5			
AUDIO ALC887														0.012		
SPI (AI1315)											0.036					
EC (IT5121E)																
TPM 2.0 (NPCT758AAAYX)											0.05					
Voltage (UNIT:V)	2	1.8	1.2	0.6	1.05	1.05	1.8	3.3	3.3	5	3	12	5	3	1.1	1.5
TOTAL CURRENT (UNIT:A)	65	27	11.9	0.8	0.3	0.5	1.3	0.202	0.008	10.5	4.811	5.6	1.5	3.446	0.46	0.5
TOTAL WATT (UNIT : W)	130	48.6	14.28	0.48	0.315	0.525	2.34	0.6666	0.0099	52.5	14.433	67.2	7.5	10.338	0.506	0.75
TRANSFER VOLTAGE	+12VSUS	+12VSUS	+12VSUS	+12VSUS	SOC	SOC	+1.8VSUS	+3VSUS	+3VSUS	+5VSUS	+12VSUS	+12VSUS	+5VSUS	+3VSUS	+3VSUS	+3VSUS
	12VSUS	5VSUS	3VSUS	1.8VSUS												
	275 W	60 W	12.27 W	2.34 W												

Power supply must consumed watts and cuments	
Power Type	DC IN (12V)
Consumed watts (Item: W)	349.61 W
Consumed cuments (Item A)	29.13 A
Actually required cuments (Item A/0.8)	36.4 A

MIX-TGLD1

ASUSTeK COMPUTER INC.

Title : Power Budget

Engineer:

Size	Project Name	Rev
C	MIX-TLUD1	R1.00

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MIX-TGLD1 shematic change list for R1.01

MIX-TGLD1

Title : history

ASUSTek COMPUTER INC.

Engineer:

Size	Project Name	Rev
B	MIX-TLUD1	R1.00

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