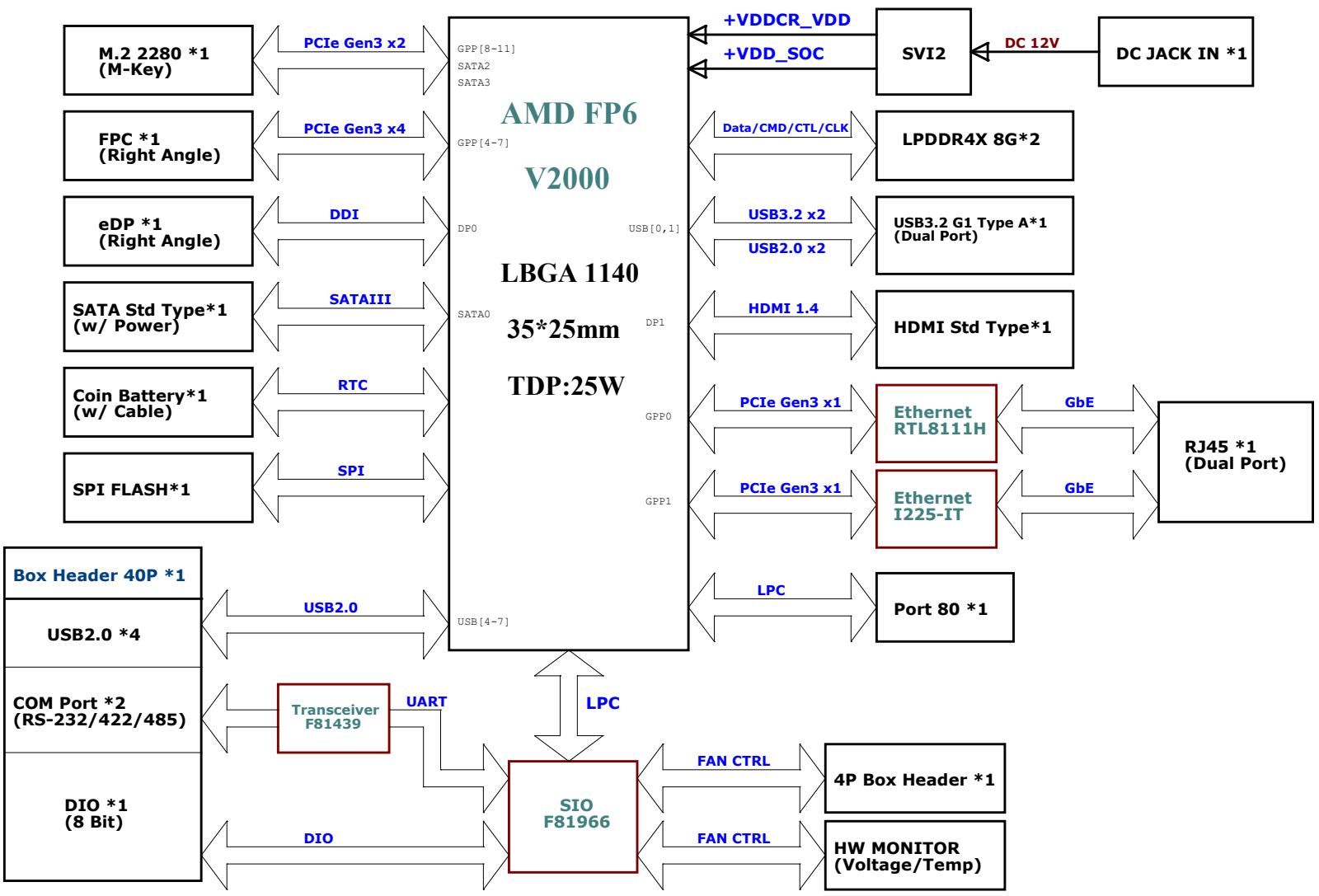
Project Name : DN-V2K8
Project Number: 1907V2K800
Version: A0.1_0_0
Board Size: 84mm*55mm



AAEON an ASUS assoc. co.	Title: TITLE BLOCK		
	Size: C	Document Number: DN-V2K8	Rev: A0.1_0_0
	Date: Monday, December 13, 2021	Sheet: 1 of 39	

SOC AGPIO Pins :

Name	Power Well	Default	GPIO Function
AGPIO0	VDD_33_S5		PM_PWRBTN#
AGPIO1	VDD_33_S5		PM_SYSRST#
AGPIO2	VDD_33_S5		PCIE_WAKE#
AGPIO3	VDD_33_S5		SMB_ALERT#
AGPIO4			APU_AGPIO4(TP)
AGPIO5			
AGPIO6			
AGPIO7			
AGPIO8	VDD_33_S0		SIO_OVT#
AGPIO9			
AGPIO10	VDD_33_S5		S0A3_GPIO
AGPIO11	VDD_33_S5		M2MDET
AGPIO12	VDD_33_S5		
AGPIO16			
AGPIO17	VDD_33_S5		USB_OC#_0
AGPIO18	VDD_33_S5		USB_OC#_1
AGPIO19	VDD_33_S5		I2C3_SCL
AGPIO20	VDD_33_S5		I2C3_SDA
AGPIO21			
AGPIO22	VDD_33_S5		SIO_PME#
AGPIO23	VDD_33_S5		AC_PRES
AGPIO24			
AGPIO29			
AGPIO30			
AGPIO31			
AGPIO32			LPC_RST#_R
AGPIO40			
AGPIO68			
AGPIO69			
AGPIO84			
AGPIO85			
AGPIO86			SPI_CLK2_R
AGPIO87			LPC_SERIRQ
AGPIO88			
AGPIO89			
AGPIO90			
AGPIO91			SPKR
AGPIO92	VDD_33		CLKREQ0#_LAN1
AGPIO115	VDD_33		CLKREQ1#_LAN2
AGPIO116	VDD_33		CLKREQ2#_FPC
AGPIO129	VDD_33/VDD_18		KBRST#
AGPIO130			SATA_ACT#
AGPIO144			
AGPIO256			
AGPIO257			
AGPIO258			
AGPIO259			
AGPIO260			
AGPIO261			
AGPIO262			
AGPIO263			
AGPIO264			
AGPIO265			
AGPIO269			
AGPIO270			

SOC EGPIO Pins :

Name	Power Well	Default	GPIO Function
EGPIO26			PCIE_RST0#
EGPIO27			PCIE_RST1#
EGPIO42			
EGPIO67			SPI_ROM_REQ#
EGPIO70			
EGPIO74			LPCCLK0
EGPIO75			LPCCLK1
EGPIO76			
EGPIO104			LAD0_ESPI1_DATA0
EGPIO105			LAD1_ESPI1_DATA1
EGPIO106			LAD2_ESPI1_DATA2
EGPIO107			LAD3_ESPI1_DATA3
EGPIO108	VDD_33		LPC_DRQ#
EGPIO109			LPC_FRAME#
EGPIO113	VDD_33		SMB_CLK
EGPIO114	VDD_33		SMB_DATA
EGPIO120	VDD_33		
EGPIO121	VDD_33		
EGPIO131	VDD_33		CLKREQ3#_M2M
EGPIO132	VDD_33		
EGPIO140			
EGPIO141			
EGPIO142			
EGPIO143			
EGPIO145	VDD_33		I2C0_CLK_3P3S
EGPIO146	VDD_33		I2C0_DATA_3P3S
EGPIO147	VDD_33		I2C1_CLK_3P3S
EGPIO148	VDD_33		I2C1_DATA_3P3S
EGPIO266			
EGPIO267			
EGPIO268			
EGPIO271			

Advanced GPIO - can be used for interrupt, wake, or GPIO.

Enhanced GPIO - can be used only for GPIO.

F81966D GPIO Pins :

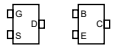
Note:
REV means reserved

Name	Tolerance	Power Well	Default	Function
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#
GPIO001	5V	I_VSB3V	Native	ERP_CTRL1#
GPIO002	5V	I_VSB3V	Native	SIO_SUS_WARN#_R
GPIO003	5V	I_VSB3V	Native	SIO_SUS_ACK#_R
GPIO004	5V	I_VSB3V	Native	SIO_SLP_SUS#
GPIO005	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO006	5V	I_VSB3V	Native	LAN1_DISABLE#
GPIO007	5V	I_VSB3V	Native	BID0
GPIO010	5V	I_VSB3V	Native	EN_USB2
GPIO011	5V	I_VSB3V	Native	EN_USB3
GPIO012	5V	I_VSB3V	Native	
GPIO013	5V	I_VSB3V	Native	
GPIO014	5V	I_VSB3V	Native	ATX_AT_TRAP
GPIO015	5V	I_VSB3V	Native	WDT_RST#
GPIO016	5V	I_VSB3V	Native	
GPIO017	5V	I_VSB3V	Native	PECI
GPIO020	5V	I_VSB3V	Native	ALERT#
GPIO021	5V	I_VSB3V	Native	SIO_ATXPG
GPIO022	5V	I_VSB3V	Native	PWSIN#
GPIO023	5V	I_VSB3V	Native	PM_PWRBTN#
GPIO024	5V	I_VSB3V	Native	PM_SLP_S3#
GPIO025	5V	I_VSB3V	Native	PS_ON#
GPIO026	5V	VBAT	Native	PCH_PWROK
GPIO027	5V	VBAT	Native	SIO_RSMRST#
GPIO030	5V	3VCC	Native	
GPIO031	5V	3VCC	Native	
GPIO032	5V	3VCC	Native	
GPIO033	5V	3VCC	Native	
GPIO034	5V	3VCC	Native	
GPIO035	5V	3VCC	Native	
GPIO036	5V	3VCC	Native	
GPIO037	5V	3VCC	Native	
GPIO040	5V	3VCC	Native	
GPIO041	5V	3VCC	Native	
GPIO042	5V	3VCC	Native	
GPIO043	5V	3VCC	Native	
GPIO044	5V	3VCC	Native	
GPIO045	5V	3VCC	Native	
GPIO046	5V	3VCC	Native	
GPIO047	5V	3VCC	Native	
GPIO050	5V	3VCC	Native	COM1_SLEW
GPIO051	5V	3VCC	Native	COM1_MODE0
GPIO052	5V	3VCC	Native	COM1_MODE1
GPIO053	5V	3VCC	Native	COM1_MODE2
GPIO054	5V	3VCC	Native	COM2_SLEW
GPIO055	5V	3VCC	Native	COM2_MODE0
GPIO056	5V	3VCC	Native	COM2_MODE1
GPIO057	5V	3VCC	Native	COM2_MODE2
GPIO060	5V	3VCC	Native	
GPIO061	5V	3VCC	Native	
GPIO062	5V	3VCC	Native	
GPIO063	5V	3VCC	Native	
GPIO064	5V	3VCC	Native	
GPIO065	5V	I_VSB3V	Native	
GPIO066	5V	VBAT	Native	DPWROK
GPIO067	5V	I_VSB3V	Native	PM_SLP_S5#
GPIO070	5V	3VCC	Native	
GPIO071	5V	3VCC	Native	
GPIO072	5V	3VCC	Native	CARD_PWR_EN
GPIO073	5V	3VCC	Native	
GPIO074	5V	3VCC	Native	
GPIO075	5V	3VCC	Native	
GPIO076	5V	3VCC	Native	
GPIO077	5V	3VCC	Native	
GPIO080	5V	3VCC	Native	DIO_0
GPIO081	5V	3VCC	Native	DIO_1
GPIO082	5V	3VCC	Native	DIO_2
GPIO083	5V	3VCC	Native	DIO_3
GPIO084	5V	3VCC	Native	DIO_4
GPIO085	5V	3VCC	Native	DIO_5
GPIO086	5V	3VCC	Native	DIO_6
GPIO087	5V	3VCC	Native	DIO_7
GPIO090	5V	IFP	Native	LPC_DRQ#
GPIO091	5V	I_VSB3V	Native	KBRST#
GPIO092	5V	I_VSB3V	Native	BID1
GPIO093	5V	I_VSB3V	Native	MSDAT#
GPIO094	5V	I_VSB3V	Native	MSCLK#
GPIO095	5V	3VCC	Native	FAN_1_TAC
GPIO096	5V	3VCC	Native	SIO_BKLCTL
GPIO97	5V	3VCC	Native	

SMBus/I2C Addresses :

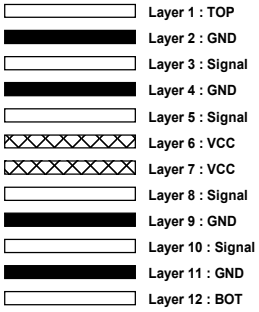
Device	Address
GPIO IC (SIO 81966)	6Eh

PCB Footprints



PCB STACK :

Impedence 50ohm +/-10%.



Function	Imnpedance(Ω)	Trace Segmant
MDI	100	Main
PCIe	85	Main
SATA	85	Main
USB3.2	85	Main
eDP	85	Main
HDMI	85	Main
Diff CLK	85	Main
Mem_DAT STROBE	80	Main
Mem_CLK	72	Main
Mem_CMD	50	Main
Mem_CTL	50	Main
Mem_DAT	50	Main

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Title: **System Setting**

Size	Document Number	Rev:
Custom	DN-V2K8	A0.1_0_0

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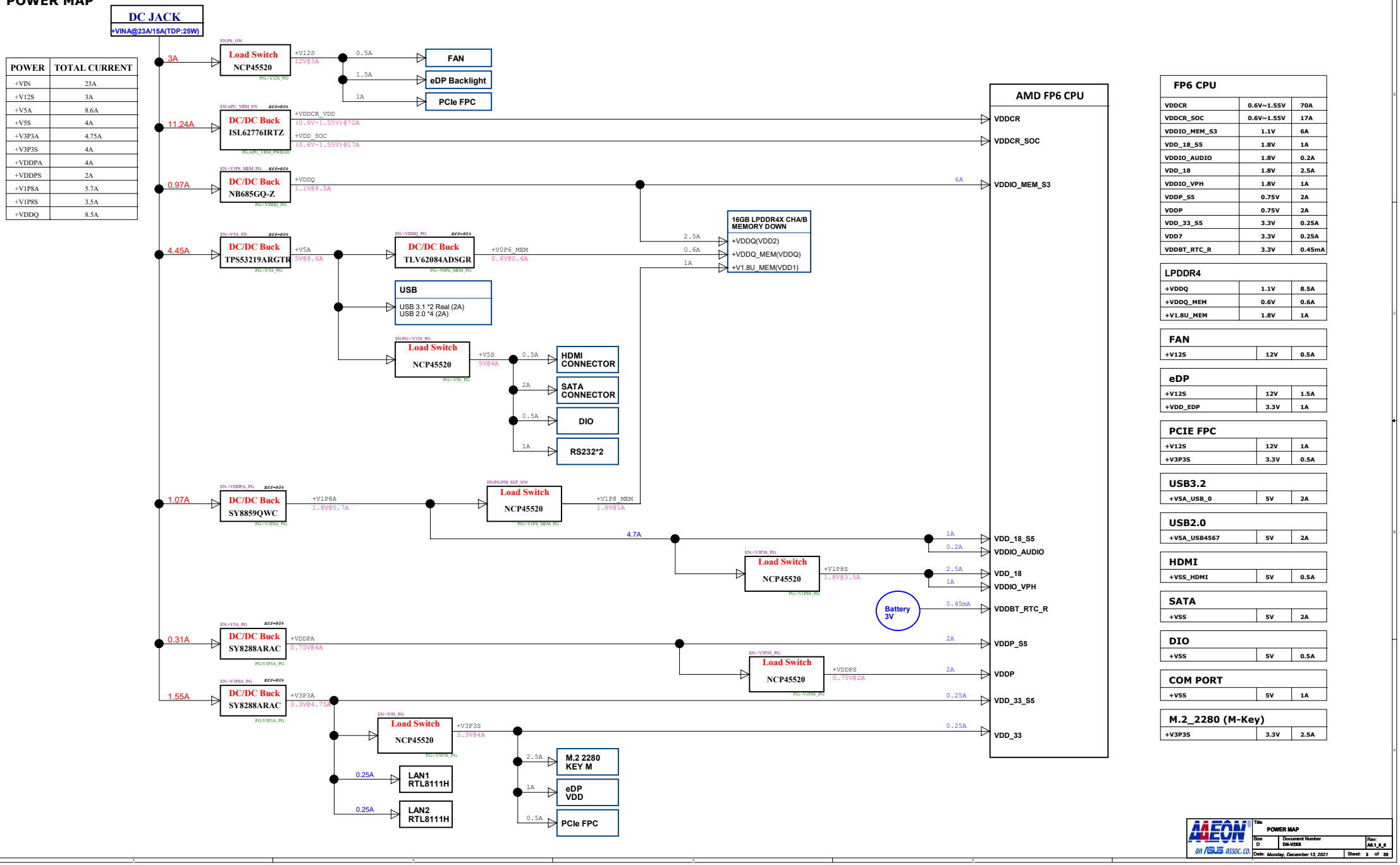
POWER MAP



POWER	TOTAL CURRENT
+VIN	23A
+V12S	3A
+V5A	8.6A
+V5S	4A
+V3P3A	4.75A
+V3P3S	4A
+VDDPA	4A
+VDDPS	2A
+V1P8A	5.7A
+V1P8S	3.5A
+VDDQ	8.5A

FP6 CPU		
VDDCR	0.6V~1.55V	70A
VDDCR_SOC	0.6V~1.55V	17A
VDDIO_MEM_S3	1.1V	6A
VDD_18_S5	1.8V	1A
VDDIO_AUDIO	1.8V	0.2A
VDD_18	1.8V	2.5A
VDDIO_VPH	1.8V	1A
VDDP_S5	0.75V	2A
VDDP	0.75V	2A
VDD_33_S5	3.3V	0.25A
VDD7	3.3V	0.25A
VDDBT_RTC_R	3.3V	0.45mA

LPDDR4		
+VDDQ	1.1V	8.5A
+VDDQ_MEM	0.6V	0.6A
+V1.8U_MEM	1.8V	1A

FAN		
+V12S	12V	0.5A

eDP		
+V12S	12V	1.5A
+VDD_EDP	3.3V	1A

PCIE FPC		
+V12S	12V	1A
+V3P3S	3.3V	0.5A

USB3.2		
+V5A_USB_0	5V	2A

USB2.0		
+V5A_USB4567	5V	2A

HDMI		
+V5S_HDMI	5V	0.5A

SATA		
+V5S	5V	2A

DIO		
+V5S	5V	0.5A

COM PORT		
+V5S	5V	1A

M.2_2280 (M-Key)		
+V3P3S	3.3V	2.5A

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Title: POWER MAP
Size: D
Document Number: DN-V2K8
Rev: A0.1_0_0
Date: Monday, December 13, 2021
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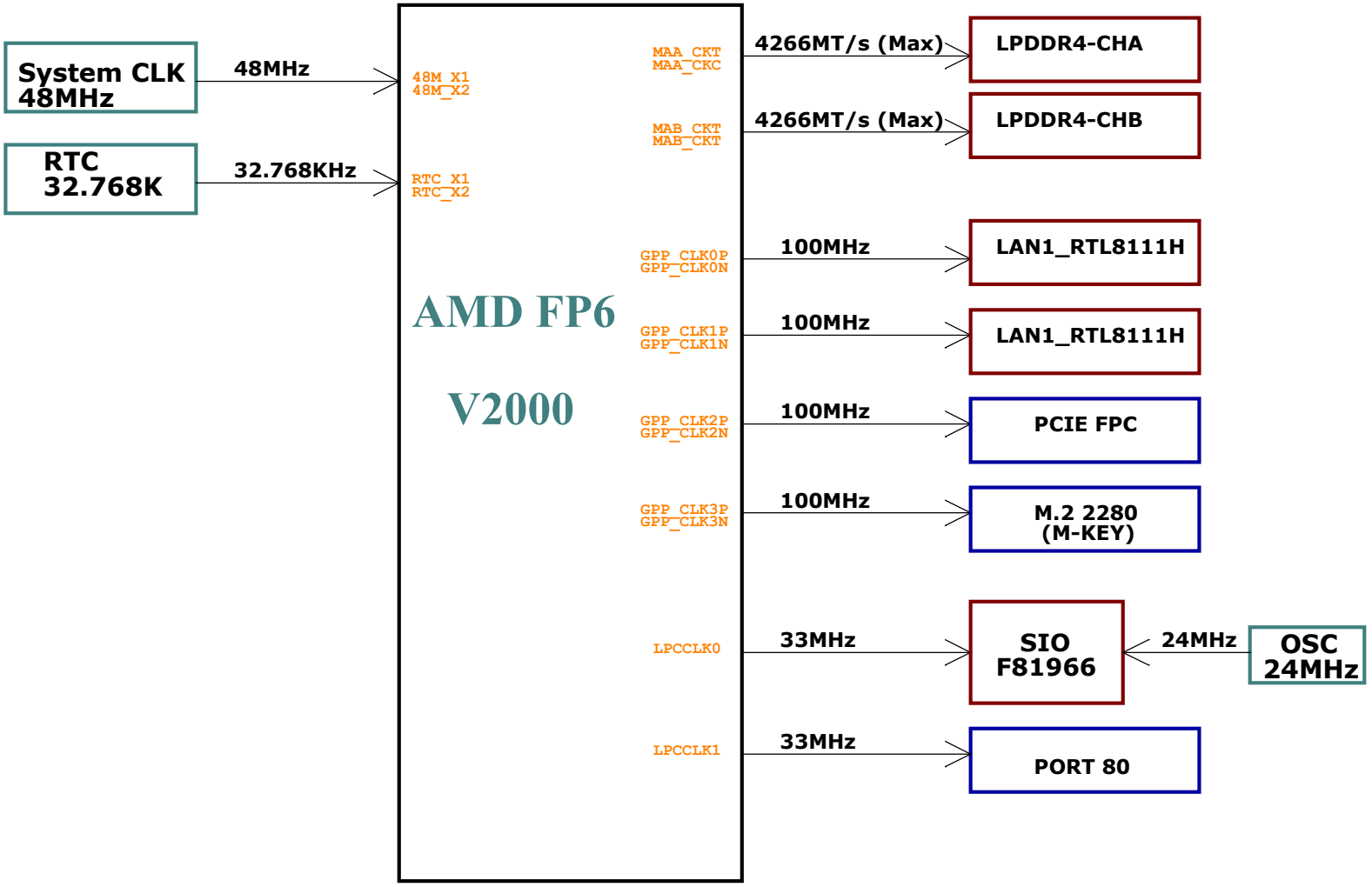
CLOCK MAP



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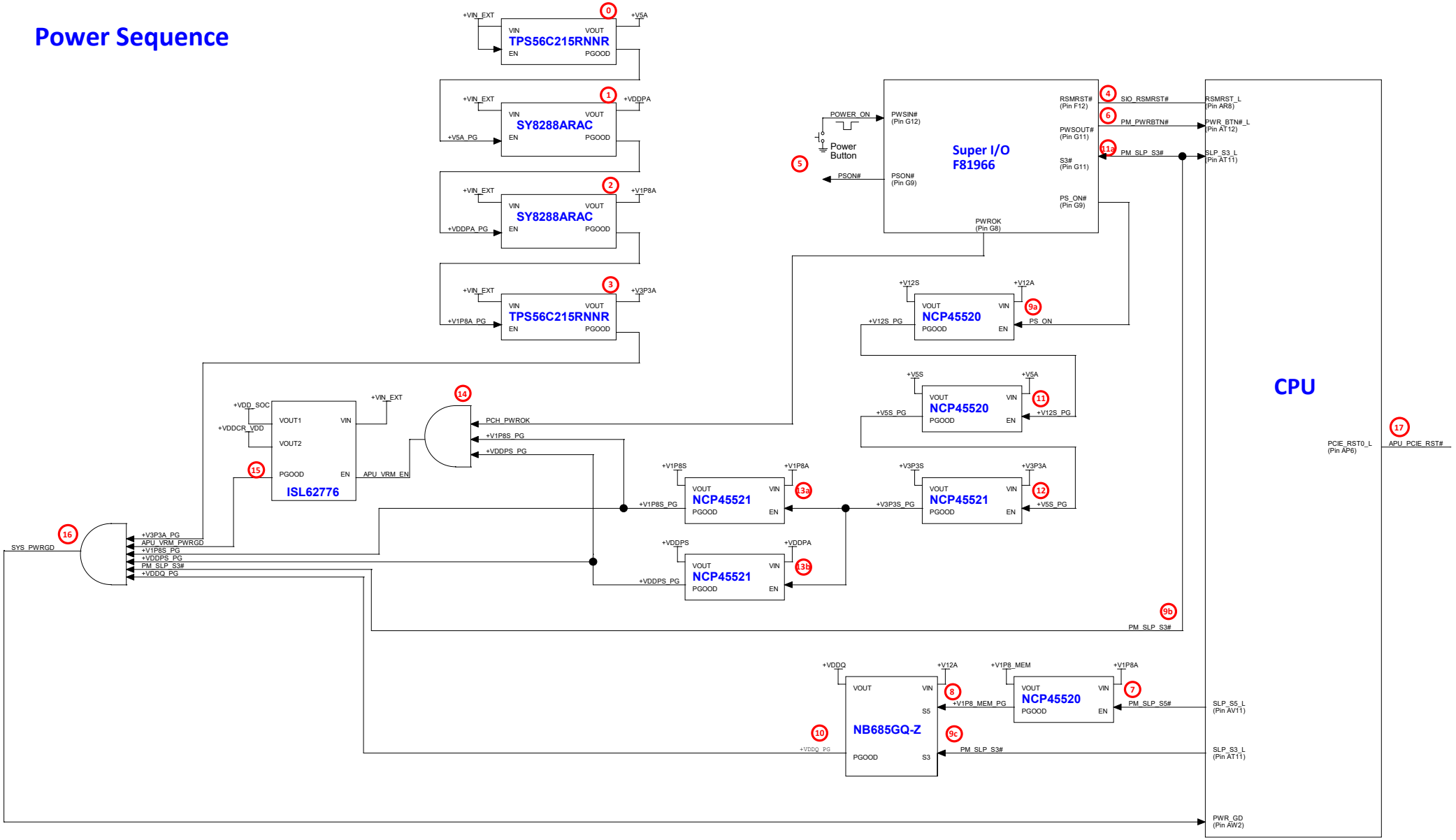
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
Date: *Monday, December 13, 2021*	Sheet: 4 of 39	

Power Sequence



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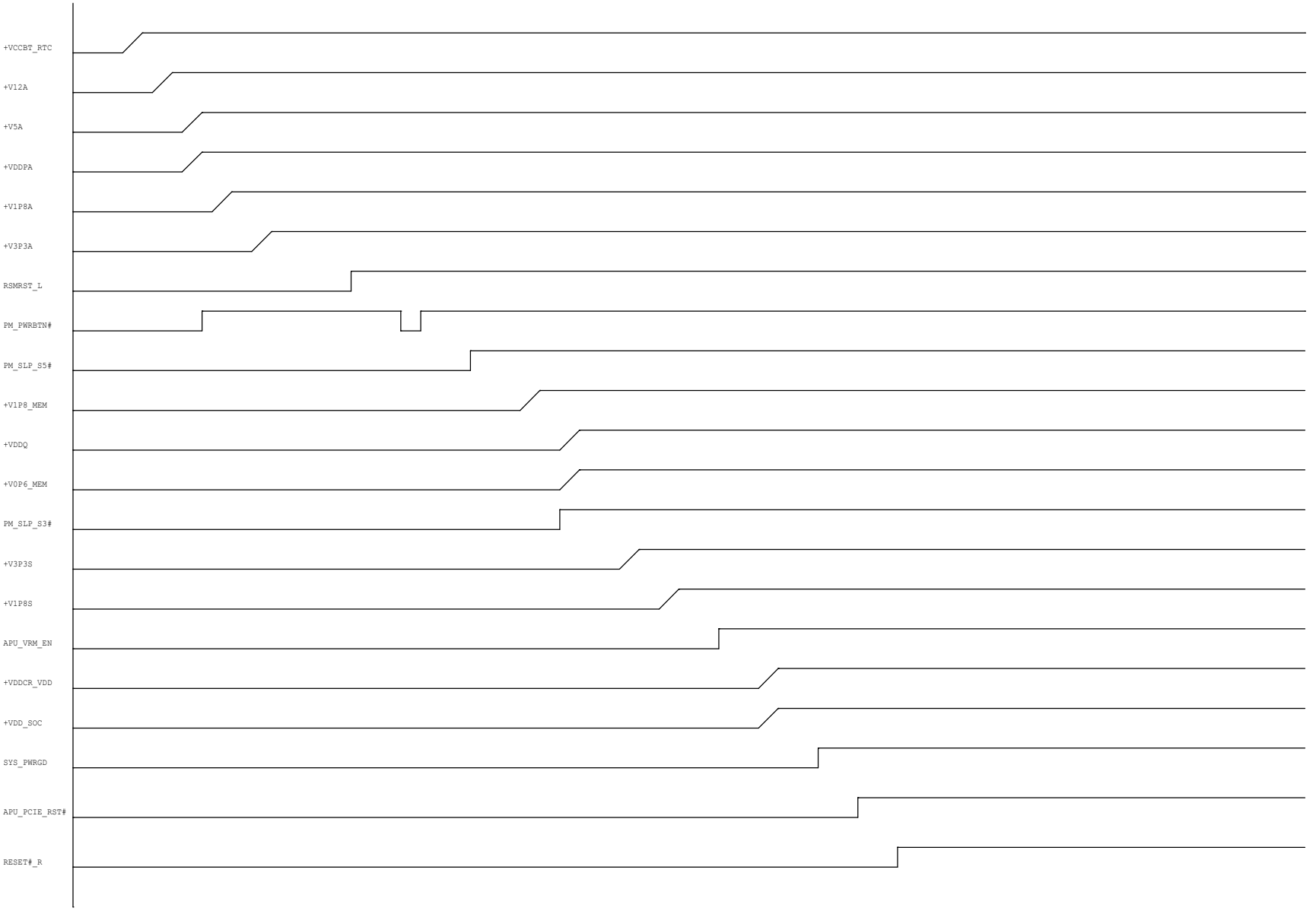
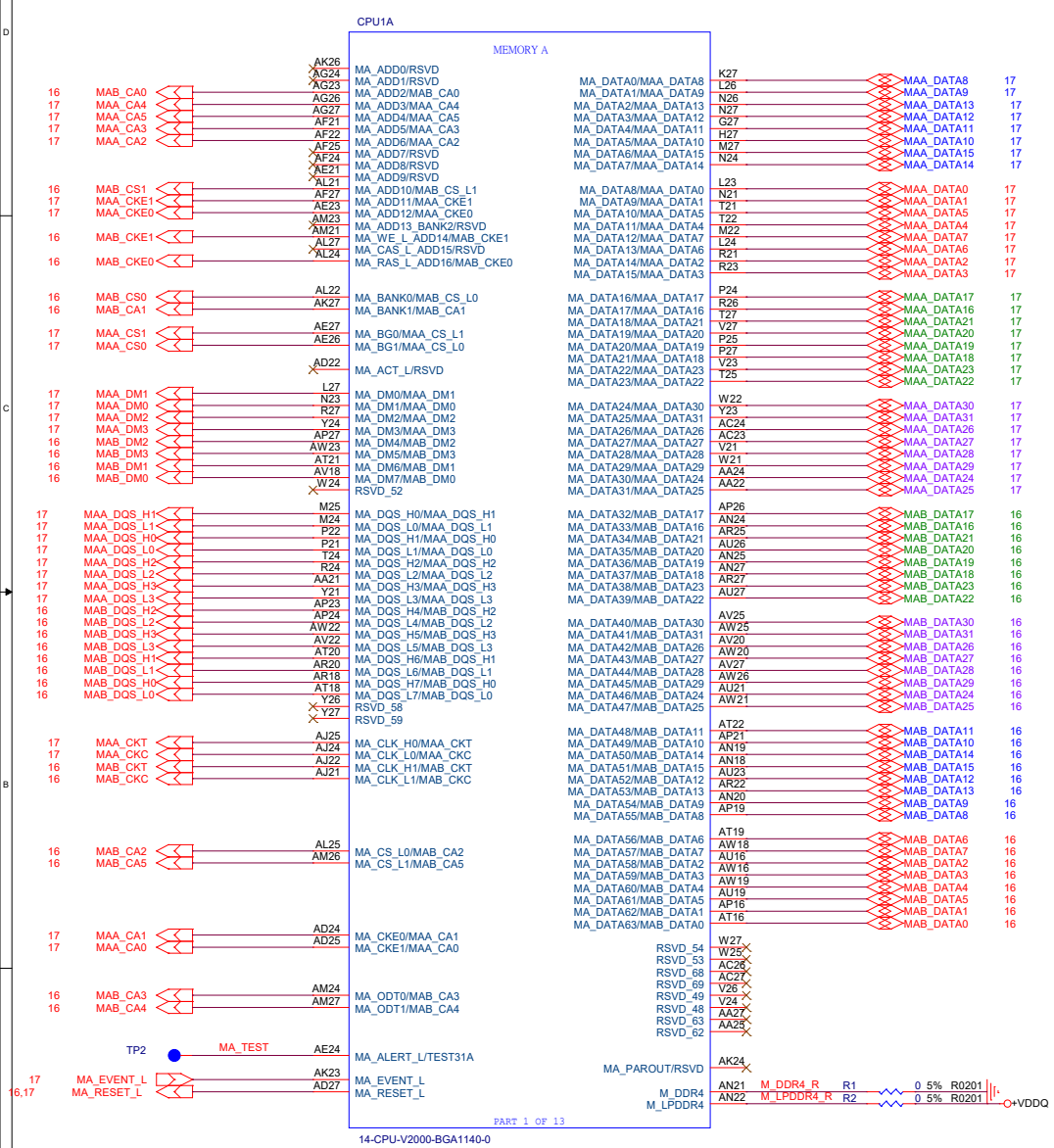
Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
Date: Monday, December 13, 2021	Sheet: 5 of 39	

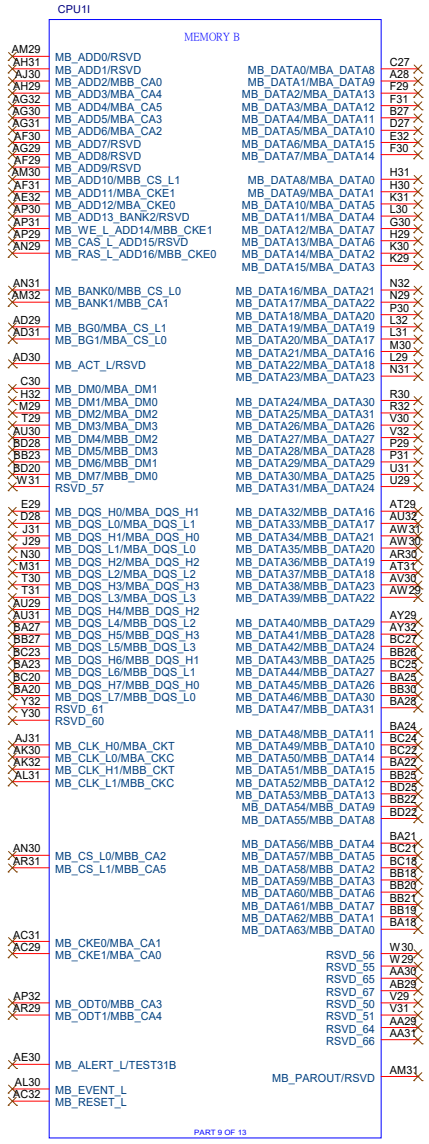


AAEON an ASUS assoc. co.

Title: **Timeing diagram**		
Size: Custom	Document Number: **DN-V2K8**	Rev: **A0.1_0_0**
Date: *Monday, December 13, 2021*	Sheet: **6** of **39**	

PROCESSOR 1-LPDDR4





AAEON an ASUS assoc. co.	Title: PROCESSOR 1 -LPDDR4		
	Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
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PROCESSOR 2-PCIe/SATA

CPU1B

PCIE

Unuse

G13 / F13	P_GFX_RXP0 / P_GFX_RXN0	P_GFX_TXP0 / P_GFX_TXN0	F4 / F2
J14 / H14	P_GFX_RXP1 / P_GFX_RXN1	P_GFX_TXP1 / P_GFX_TXN1	F3 / E4
G15 / F15	P_GFX_RXP2 / P_GFX_RXN2	P_GFX_TXP2 / P_GFX_TXN2	E1 / C1
J15 / K15	P_GFX_RXP3 / P_GFX_RXN3	P_GFX_TXP3 / P_GFX_TXN3	D5 / E6
H16 / J16	P_GFX_RXP4 / P_GFX_RXN4	P_GFX_TXP4 / P_GFX_TXN4	C6 / D6
F18 / G18	P_GFX_RXP5 / P_GFX_RXN5	P_GFX_TXP5 / P_GFX_TXN5	B6 / C7
J18 / K18	P_GFX_RXP6 / P_GFX_RXN6	P_GFX_TXP6 / P_GFX_TXN6	D8 / B8
H19 / G19	P_GFX_RXP7 / P_GFX_RXN7	P_GFX_TXP7 / P_GFX_TXN7	C8 / A8

Unuse

From LAN1

22	GPP_LAN1_RXP0_C	G11	P_GPP_RXP0	P_GPP_TXP0	L3	GPP_TXP0_LAN1_C	C1	0.22uF 10V C0201	GPP_RXP0_LAN1	22	To LAN1
22	GPP_LAN1_RXN0_C	F11	P_GPP_RXN0	P_GPP_TXN0	L1	GPP_TXN0_LAN1_C	C2	0.22uF 10V C0201	GPP_RXN0_LAN1	22	

From LAN2

23	GPP_LAN2_RXP1_C	J10	P_GPP_RXP1	P_GPP_TXP1	L4	GPP_TXP1_LAN2_C	C3	0.22uF 10V C0201	GPP_RXP1_LAN2	23	To LAN2
23	GPP_LAN2_RXN1_C	H10	P_GPP_RXN1	P_GPP_TXN1	L2	GPP_TXN1_LAN2_C	C4	0.22uF 10V C0201	GPP_RXN1_LAN2	23	

From SATA

20	SATA0_RXP	G8	P_GPP_RXP2/SATA0_RXP	P_GPP_TXP2/SATA0_TXP	M4				SATA0_TXP	20	To SATA
20	SATA0_RXN	F8	P_GPP_RXN2/SATA0_RXN	P_GPP_TXN2/SATA0_TXN	M2				SATA0_TXN	20	

		G6	P_GPP_RXP3/SATA1_RXP	P_GPP_TXP3/SATA1_TXP	N3						
		F7	P_GPP_RXN3/SATA1_RXN	P_GPP_TXN3/SATA1_TXN	N1						

From FPC

20	FPC_PCIE_RXP4	M9	P_GPP_RXP4	P_GPP_TXP4	T2	FPC_PCIE_TXP4_C	C5	0.22uF 10V C0201	FPC_PCIE_TXP4	20	To FPC
20	FPC_PCIE_RXN4	M8	P_GPP_RXN4	P_GPP_TXN4	T4	FPC_PCIE_TXN4_C	C6	0.22uF 10V C0201	FPC_PCIE_TXN4	20	
20	FPC_PCIE_RXP5	L7	P_GPP_RXP5	P_GPP_TXP5	R1	FPC_PCIE_TXP5_C	C7	0.22uF 10V C0201	FPC_PCIE_TXP5	20	
20	FPC_PCIE_RXN5	L6	P_GPP_RXN5	P_GPP_TXN5	R3	FPC_PCIE_TXN5_C	C8	0.22uF 10V C0201	FPC_PCIE_TXN5	20	
20	FPC_PCIE_RXP6	K7	P_GPP_RXP6	P_GPP_TXP6	P2	FPC_PCIE_TXP6_C	C9	0.22uF 10V C0201	FPC_PCIE_TXP6	20	
20	FPC_PCIE_RXN6	K8	P_GPP_RXN6	P_GPP_TXN6	P4	FPC_PCIE_TXN6_C	C10	0.22uF 10V C0201	FPC_PCIE_TXN6	20	
20	FPC_PCIE_RXP7	H6	P_GPP_RXP7	P_GPP_TXP7	N2	FPC_PCIE_TXP7_C	C11	0.22uF 10V C0201	FPC_PCIE_TXP7	20	
20	FPC_PCIE_RXN7	H7	P_GPP_RXN7	P_GPP_TXN7	N4	FPC_PCIE_TXN7_C	C12	0.22uF 10V C0201	FPC_PCIE_TXN7	20	

From M.2 M-Key

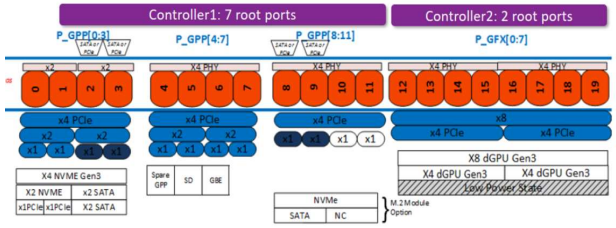
21	GPP_RXP8_SATA2_RXP	L9	P_GPP_RXP8/SATA2_RXP	P_GPP_TXP8/SATA2_TXP	K2	GPP_TXP8_SATA2_TXP_C	C13	0.22uF 10V C0201	GPP_TXP8_SATA2_TXP	21	To M.2 M-Key
21	GPP_RXN8_SATA2_RXN	L10	P_GPP_RXN8/SATA2_RXN	P_GPP_TXN8/SATA2_TXN	K4	GPP_TXN8_SATA2_TXN_C	C14	0.22uF 10V C0201	GPP_TXN8_SATA2_TXN	21	
21	GPP_RXP9_SATA3_RXP	K11	P_GPP_RXP9/SATA3_RXP	P_GPP_TXP9/SATA3_TXP	J4	GPP_TXP9_SATA3_TXP_C	C15	0.22uF 10V C0201	GPP_TXP9_SATA3_TXP	21	
21	GPP_RXN9_SATA3_RXN	J11	P_GPP_RXN9/SATA3_RXN	P_GPP_TXN9/SATA3_TXN	J2	GPP_TXN9_SATA3_TXN_C	C16	0.22uF 10V C0201	GPP_TXN9_SATA3_TXN	21	

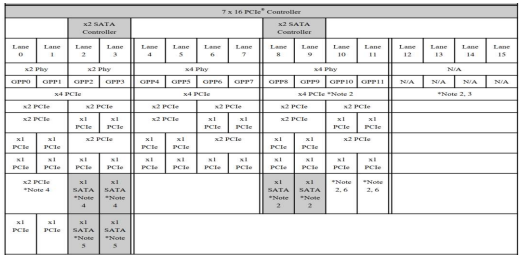
		J12 / H12	P_GPP_RXP10 / P_GPP_RXN10	P_GPP_TXP10 / P_GPP_TXN10	H3 / H1						
		J13 / K13	P_GPP_RXP11 / P_GPP_RXN11	P_GPP_TXP11 / P_GPP_TXN11	H4 / H2						

PART 2 OF 13

14-CPU-V2000-BGA1140-0

Design Note:
AC cap must have close to SoC
At least 500mil





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Title: PROCESSOR 2 -PCIe/SATA		
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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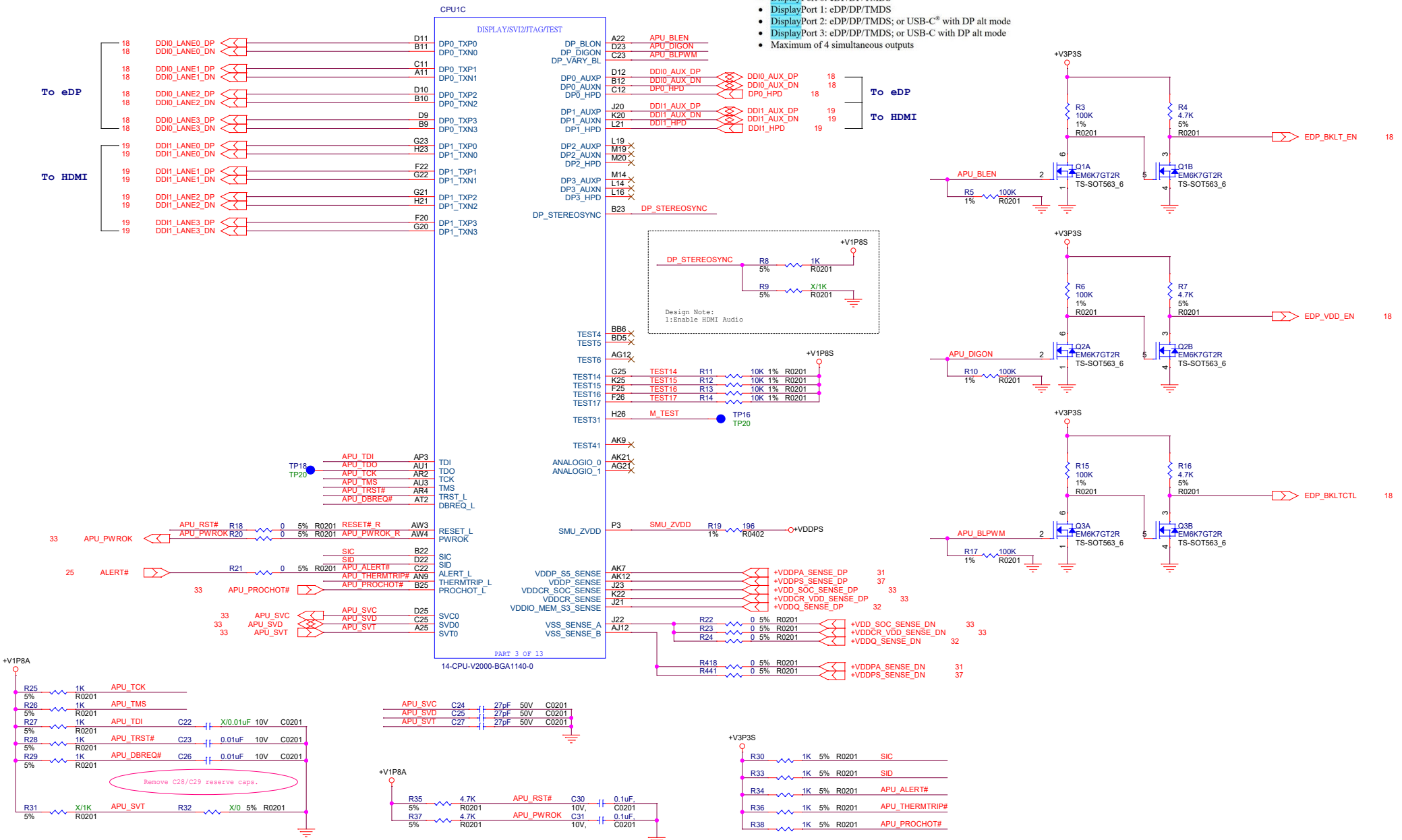
PROCESSOR 3-Display/SVID

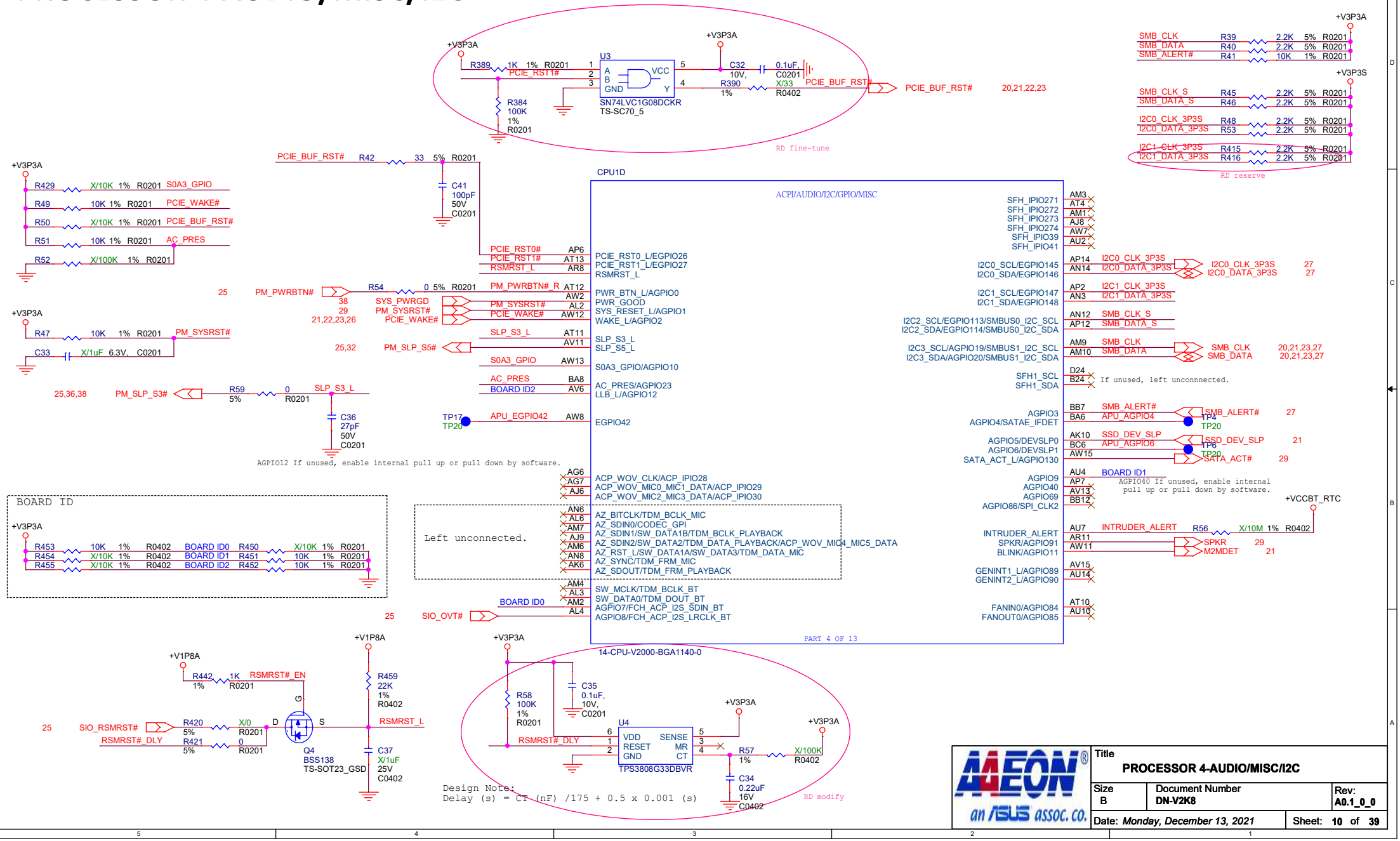
FP6 processor Display Ports

- DisplayPort 0: eDP/DP/TMDS
- DisplayPort 1: eDP/DP/TMDS
- DisplayPort 2: eDP/DP/TMDS; or USB-C® with DP alt mode
- DisplayPort 3: eDP/DP/TMDS; or USB-C with DP alt mode
- Maximum of 4 simultaneous outputs



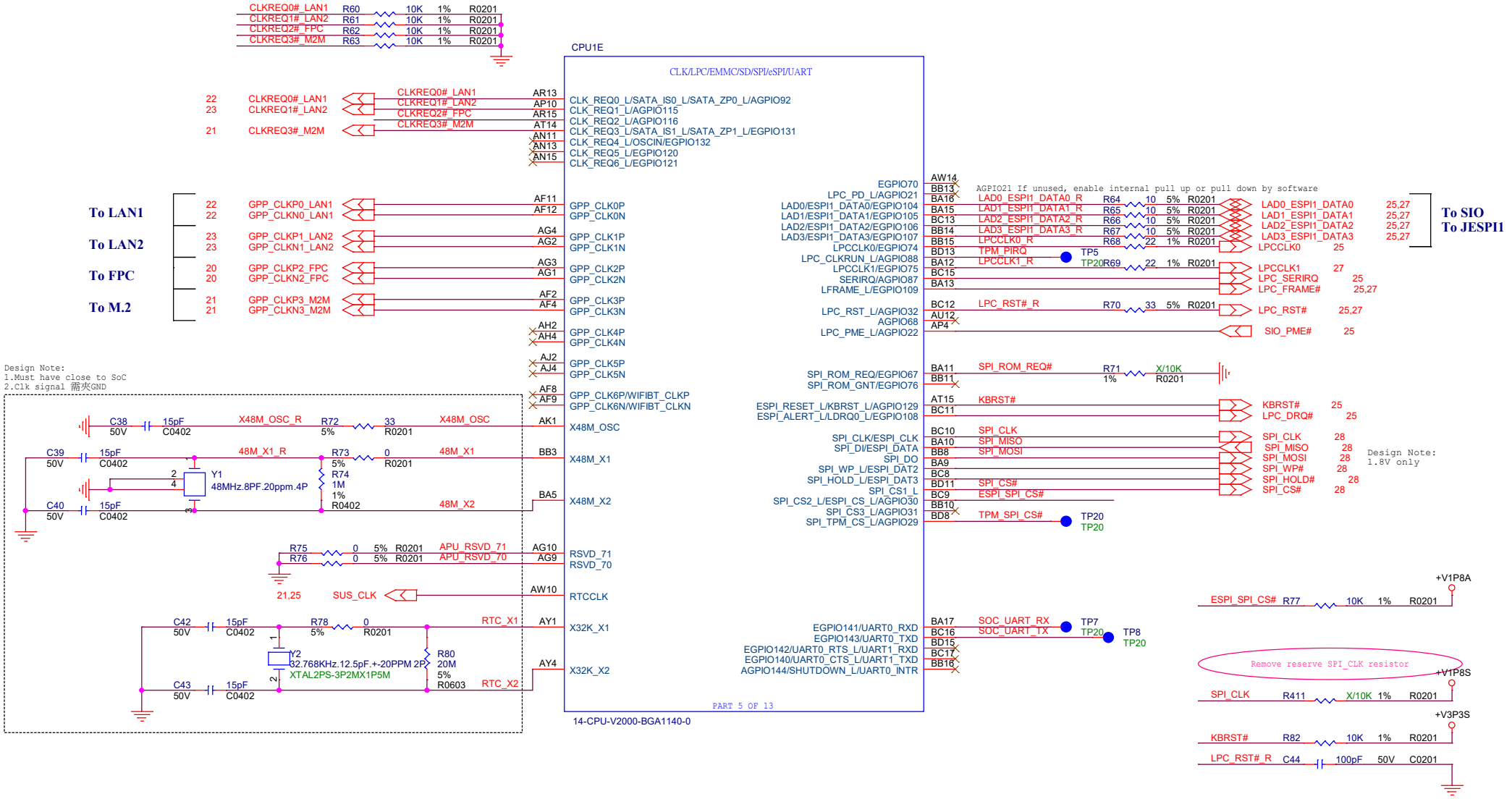
Title	PROCESSOR 3-Display	
Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
Date: Monday, December 13, 2021		Sheet: 9 of 39

PROCESSOR 4-AUDIO/MISC/I2C



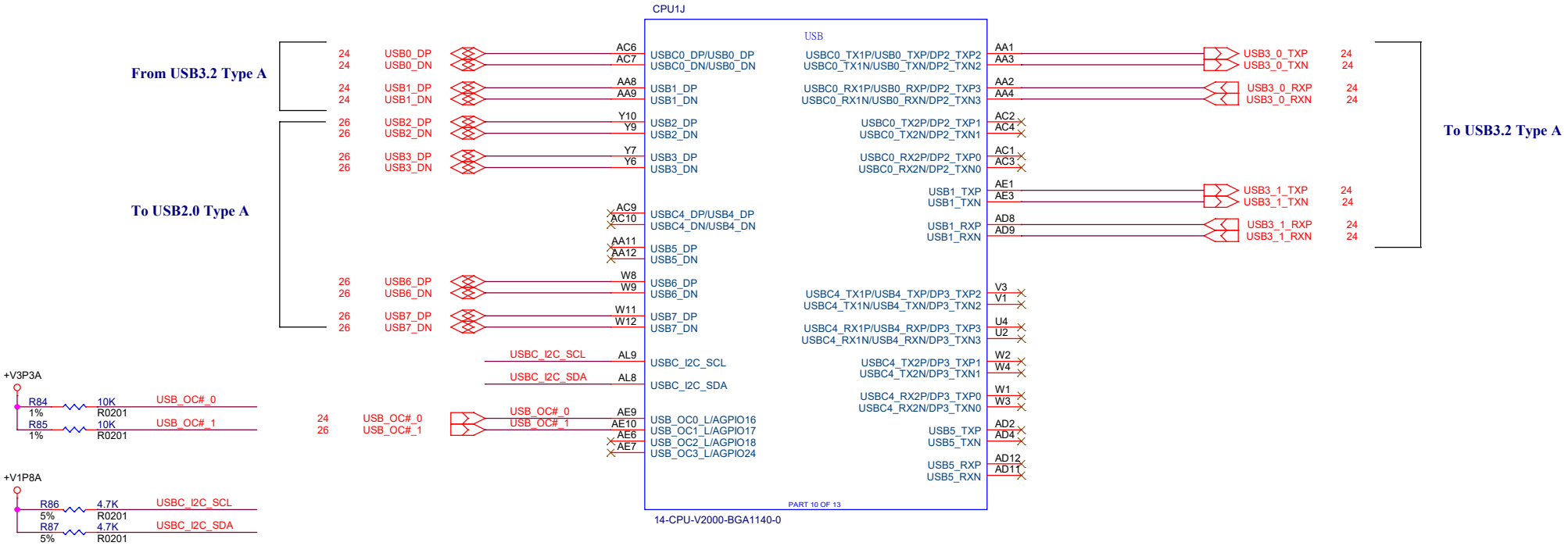
Title	PROCESSOR 4-AUDIO/MISC/I2C	
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
Date: Monday, December 13, 2021		Sheet: 10 of 39

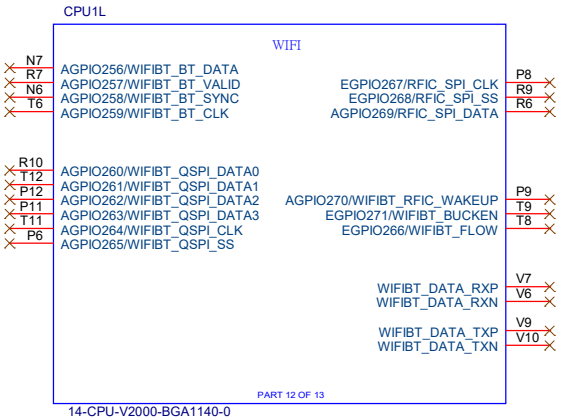
PROCESSOR 5-CLK/LPC/UART



AEON an ASUS assoc. co.	Title: PROCESSOR 5-CLK/LPC/UART	
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
Date: Monday, December 13, 2021	Sheet: 11 of 39	

PROCESSOR 6-USB/WIFI





AAEON an ASUS assoc. co.	Title: PROCESSOR 6-USB/WIFI	
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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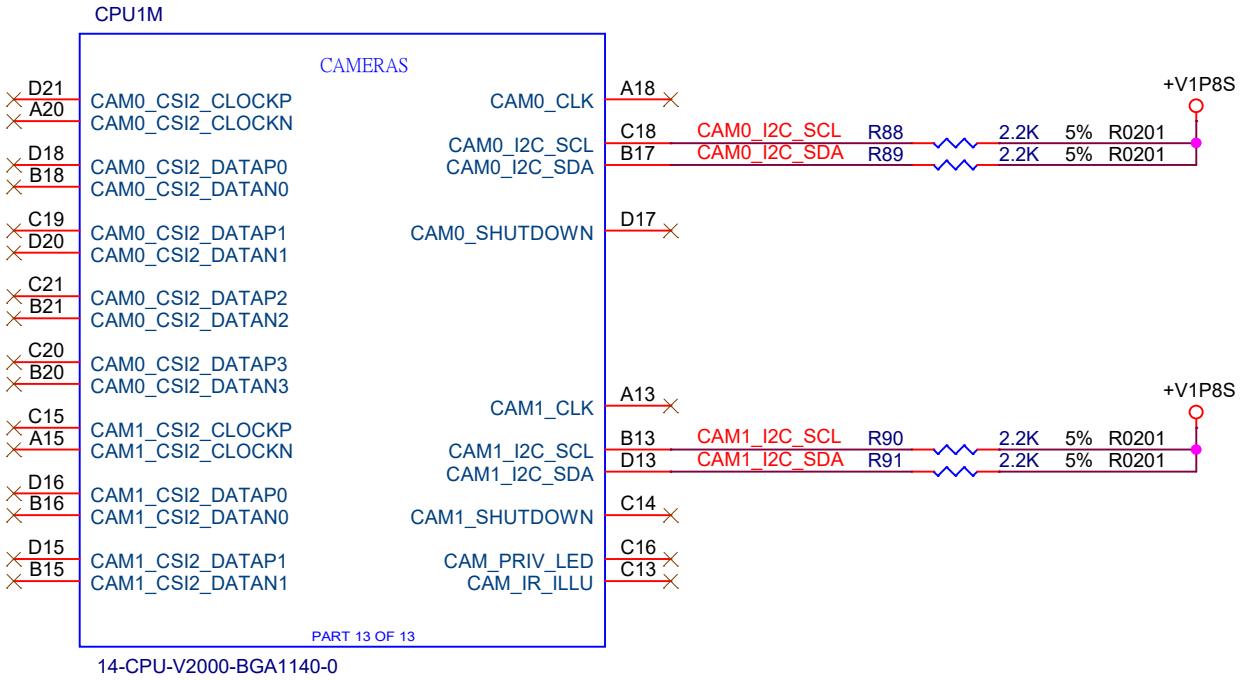
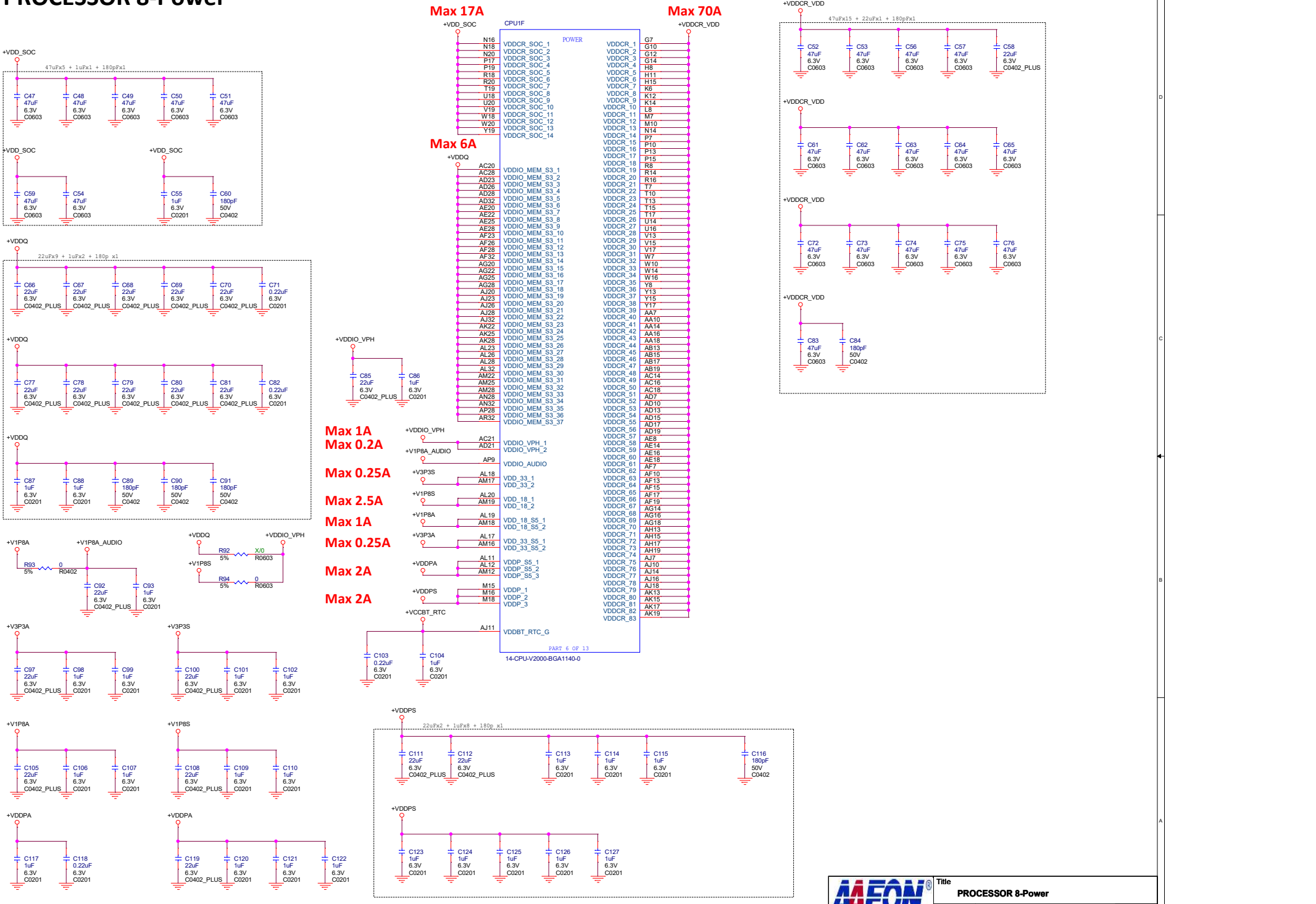
PROCESSOR 7-CAM



AAEON an ASUS assoc. co.	Title: **PROCESSOR 7-CAM**	
Size: A	Document Number: **DN-V2K8**	Rev: **A0.1_0_0**
Date: *Monday, December 13, 2021*	Sheet: **13** of **39**	

PROCESSOR 8-Power



Title	PROCESSOR 8-Power
Size	Custom
Document Number	DN-V2K8
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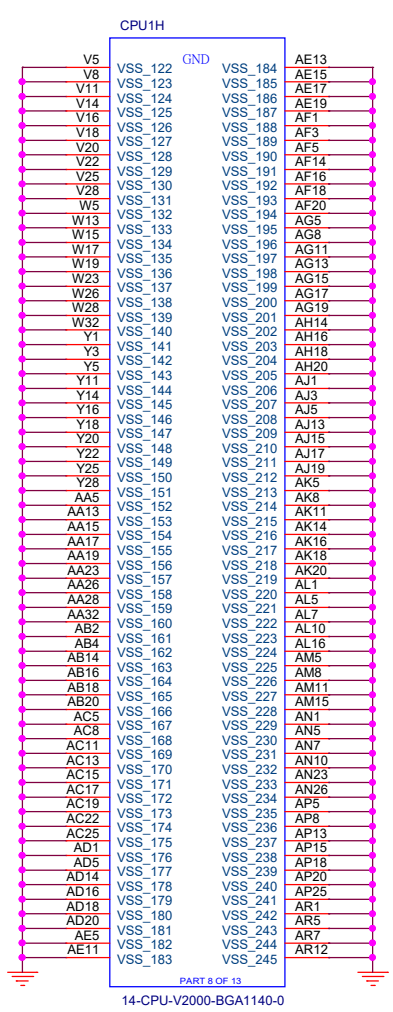
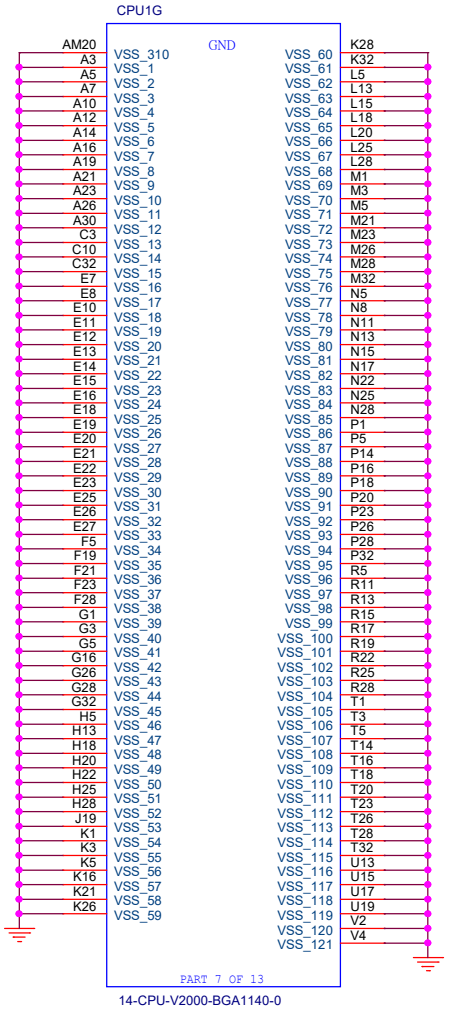
AAEON an ASUS assoc. co.

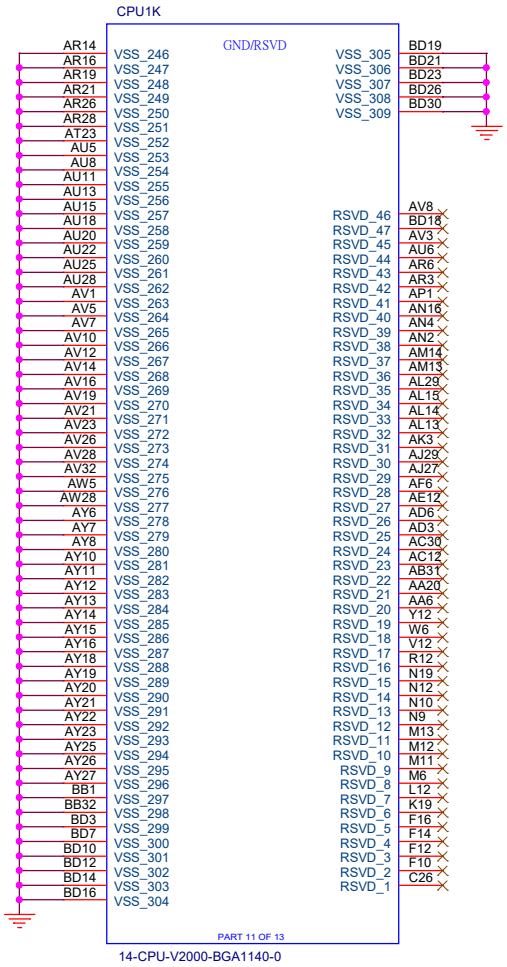
PROCESSOR 9-GND



14-CPU-V2000-BGA1140-0



14-CPU-V2000-BGA1140-0



14-CPU-V2000-BGA1140-0

AAEON an ASUS assoc. co.

Title: PROCESSOR 9-GND		
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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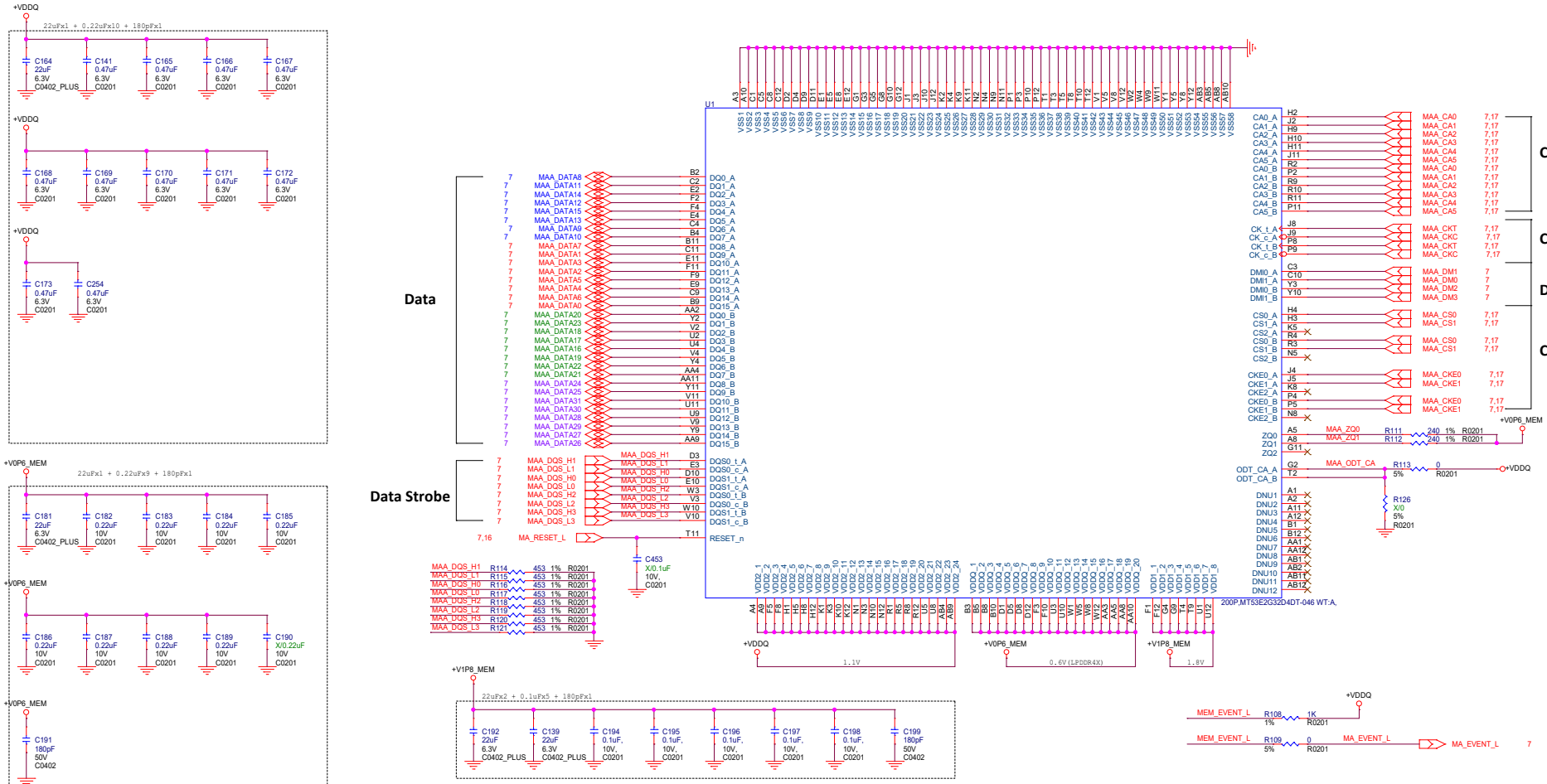
LPDDR4_CHA-A(8GB)



Capacitor		DRAM Configuration	VDD1-VSS	VDD2-VSS	VDDQ -VSS
Value	Package Size / Material		+MEM_1.8V	+APU_VDDIO_SUS	+MEM_VDDQ
		LPDDR4x	1.8V	1.1V	0.6V
		LPDDR4			1.1V
22 µF	0603 X5R	x32	2	1	1
0.22 µF	0402 X5R	x32	–	20	–
0.1 µF	0402 X5R	x32	5	–	15
180 pF	0402 X5R	x32	1	–	1

AAEON an ASUS assoc. co.	Title: LPDDR4_CHA-A		
	Size: C	Document Number: DN-V2K8	Rev: A0.1_0_0
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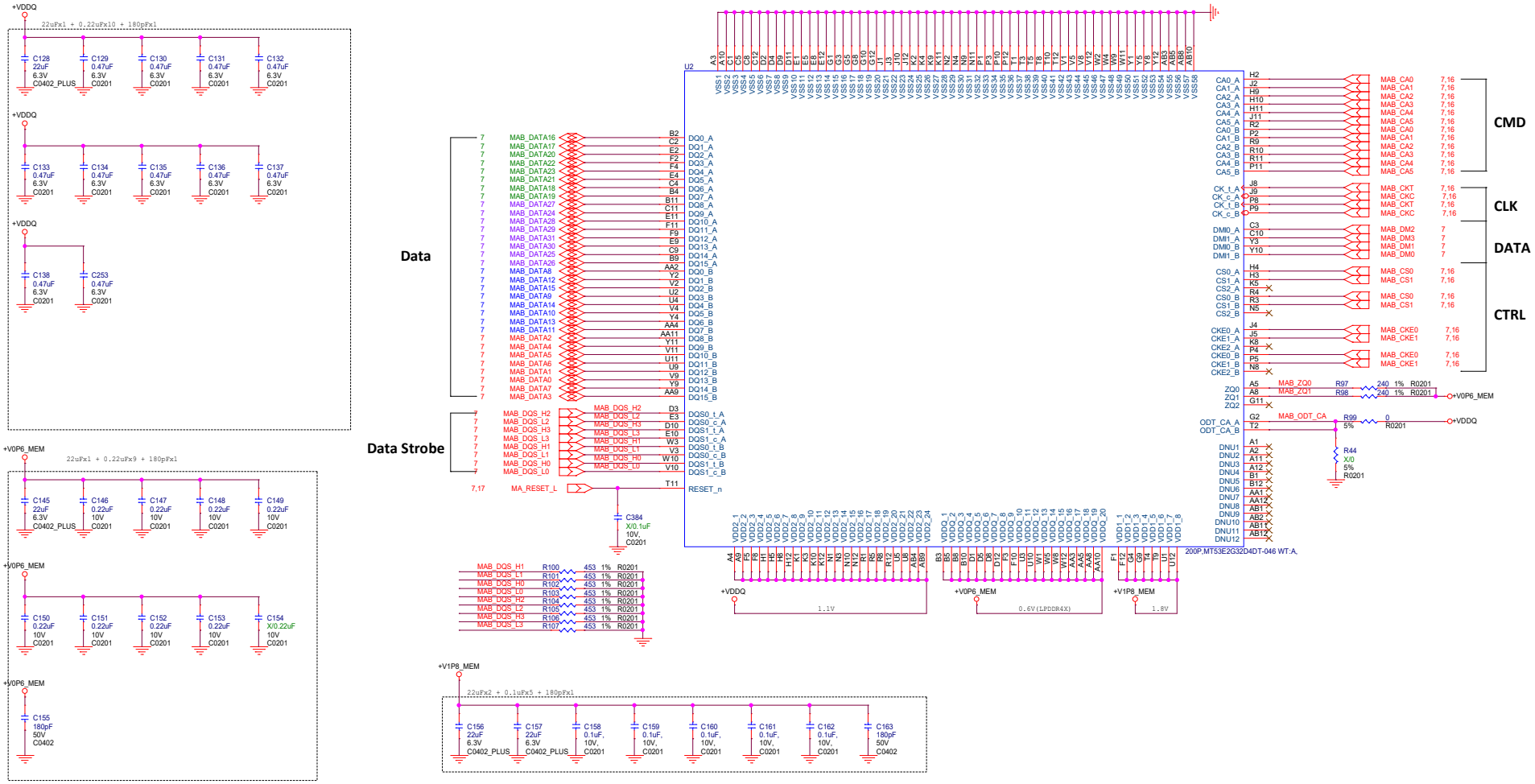
LPDDR4_CHA-B(8GB)



Capacitor		DRAM Configuration	VDD1-VSS	VDD2-VSS	VDDQ -VSS
Value	Package Size / Material		+MEM_1.8V	+APU_VDDIO_SUS	+MEM_VDDQ
		LPDDR4x	1.8V	1.1V	0.6V
		LPDDR4			1.1V
22 µF	0603 X5R	x32	2	1	1
0.22 µF	0402 X5R	x32	–	20	–
0.1 µF	0402 X5R	x32	5	–	15
180 pF	0402 X5R	x32	1	–	1

AAEON an ASUS assoc. co.	Title: LPDDR4_CHA-B		
	Size: C	Document Number: DN-V2K8	Rev: A0.1_0_0
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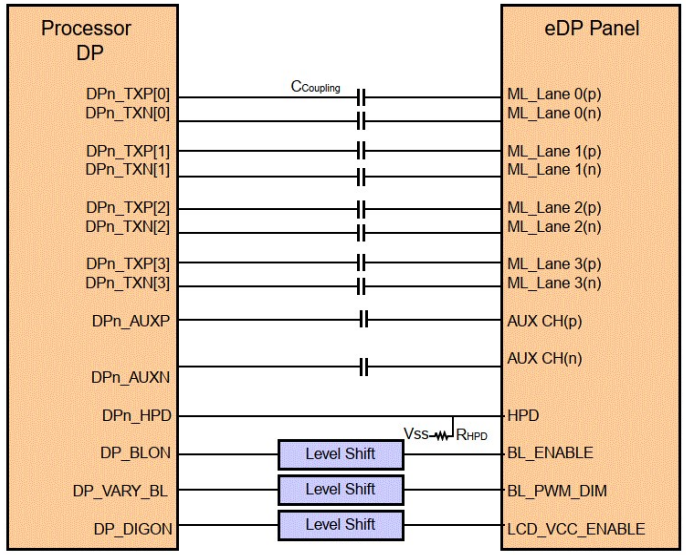
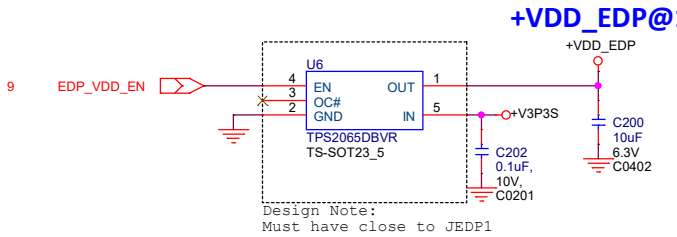
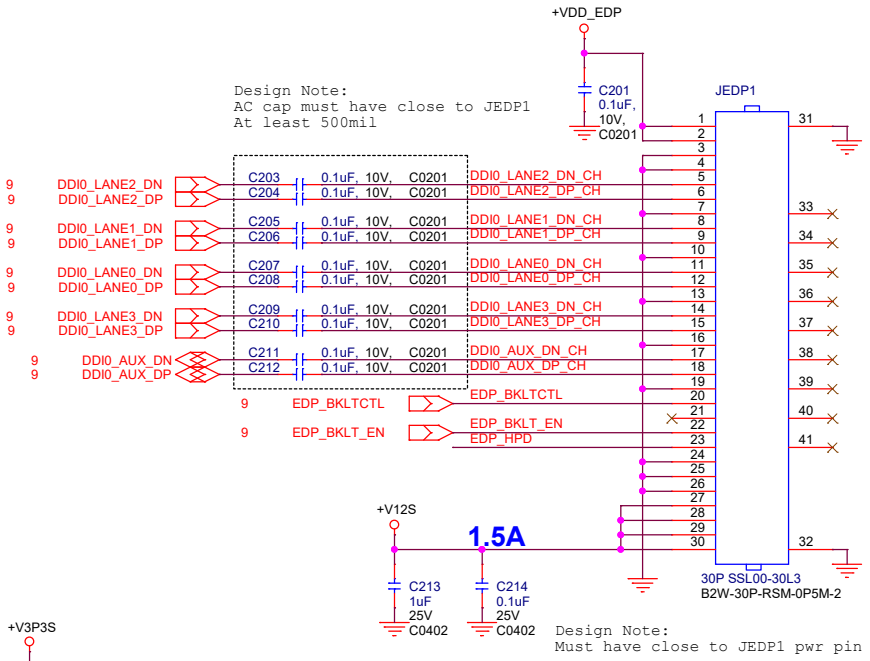
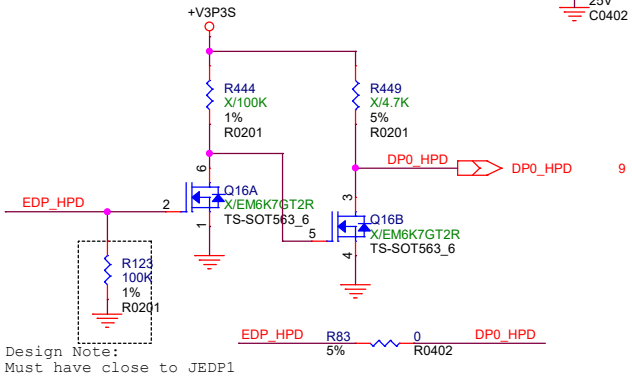
eDP









AAEON an ASUS assoc. co.	Title: eDP		
	Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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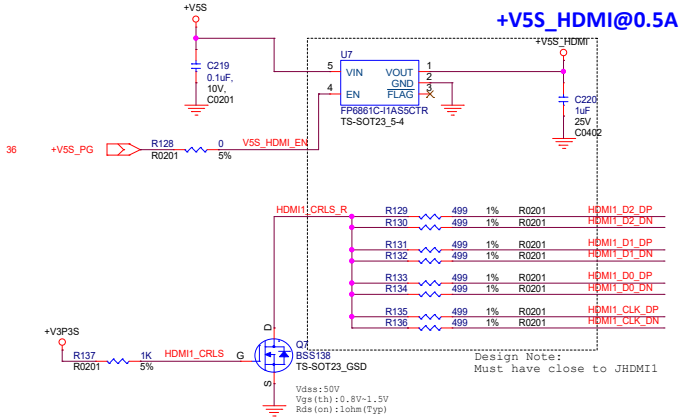
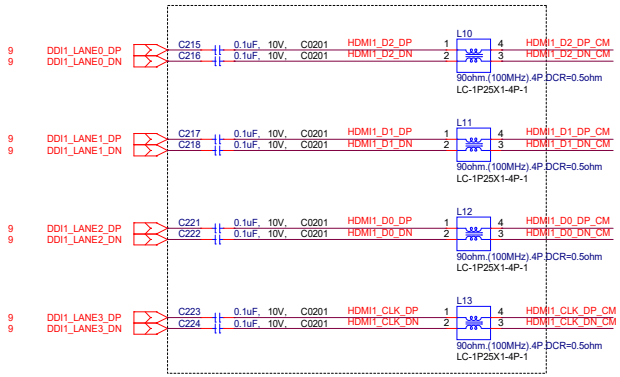
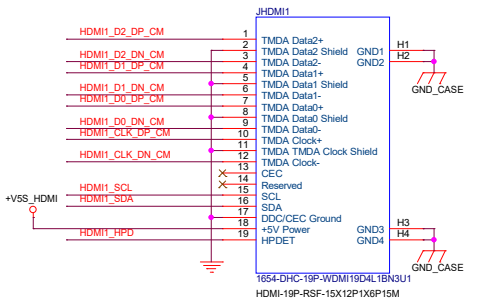
HDMI 1.4

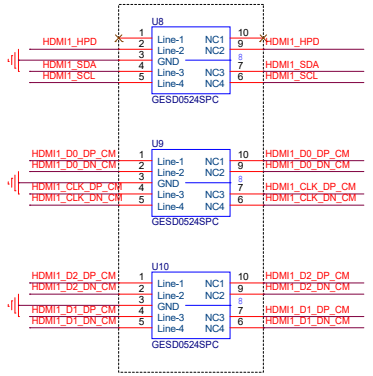


Design No
AC cap must have close to JHDMI1
At least 500mil

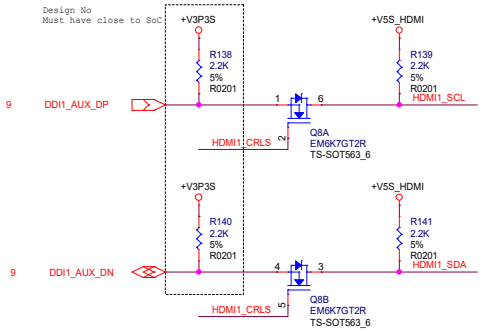


Design Note:
Diff pin of connector were must have to plane void.

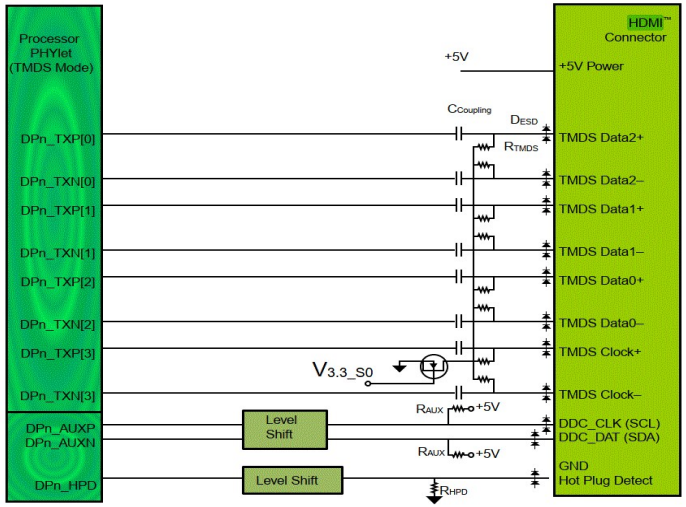


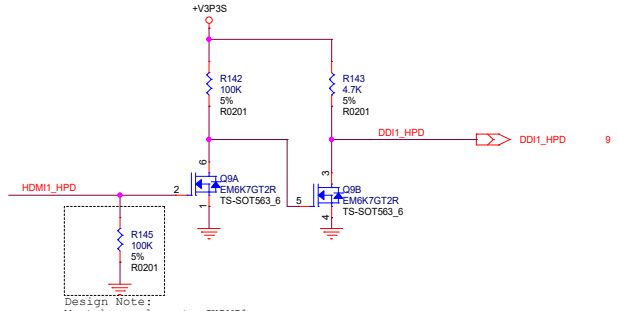


Design No
Must have close to SoC



Design Note:
Must have close to JHDMI1





Design Note:
Must have close to JHDMI1

Title: HDMI 1.4		
Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
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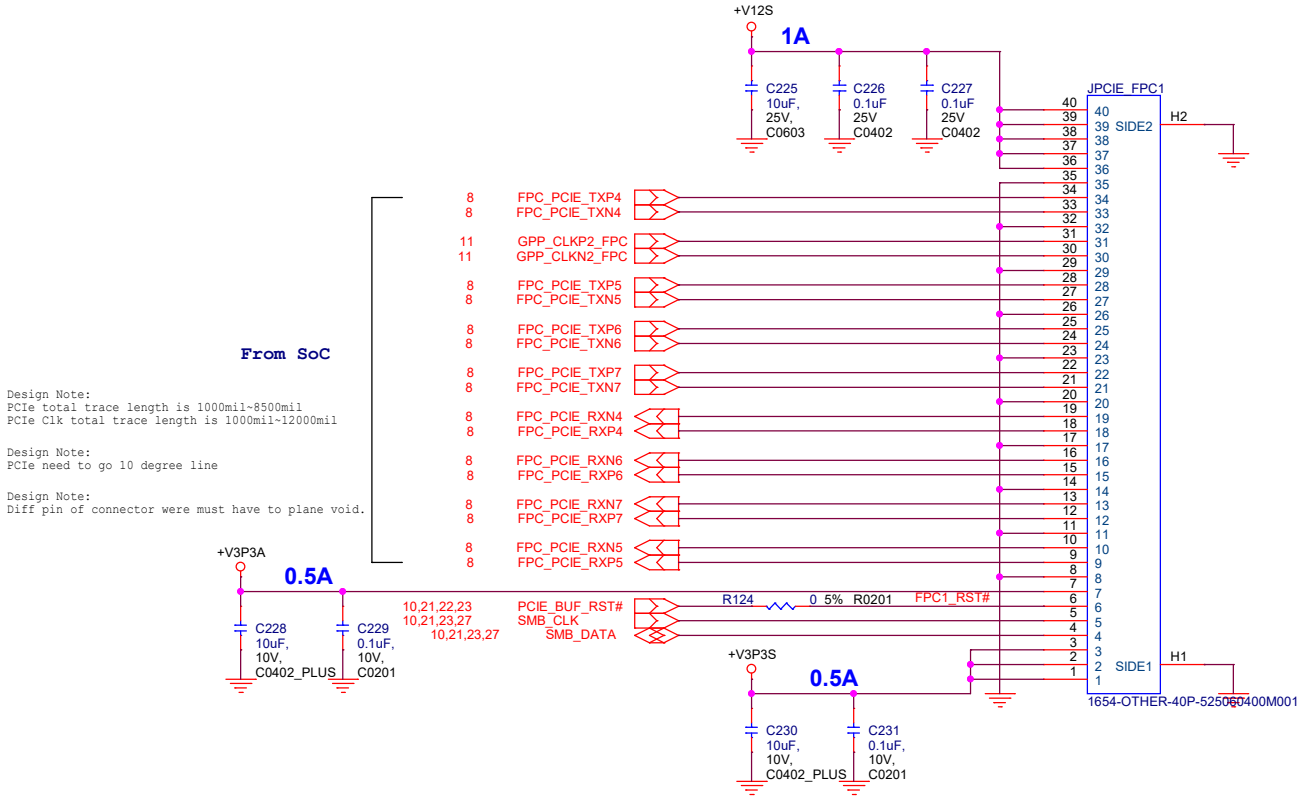
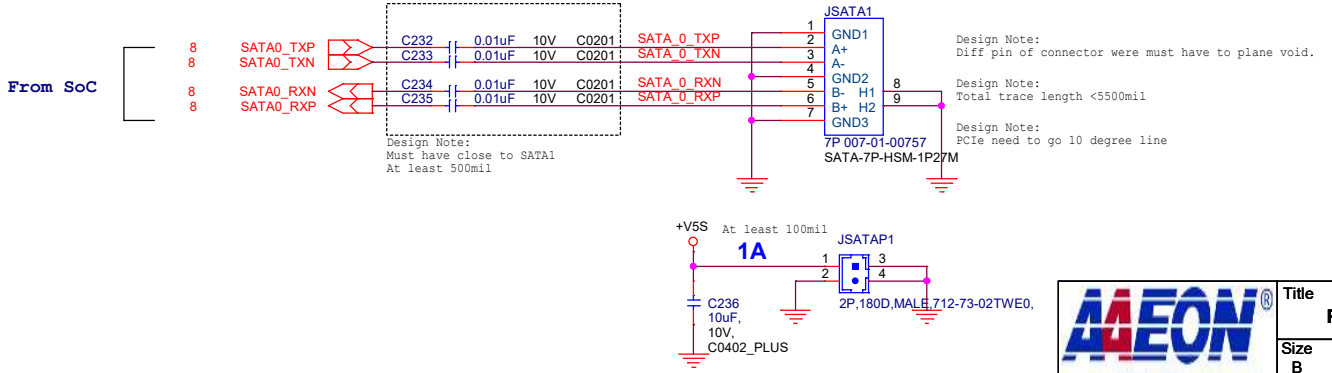
PCIE FPC



SATA



AAEON an ASUS assoc. co.	Title: PCIE FPC/SATA	
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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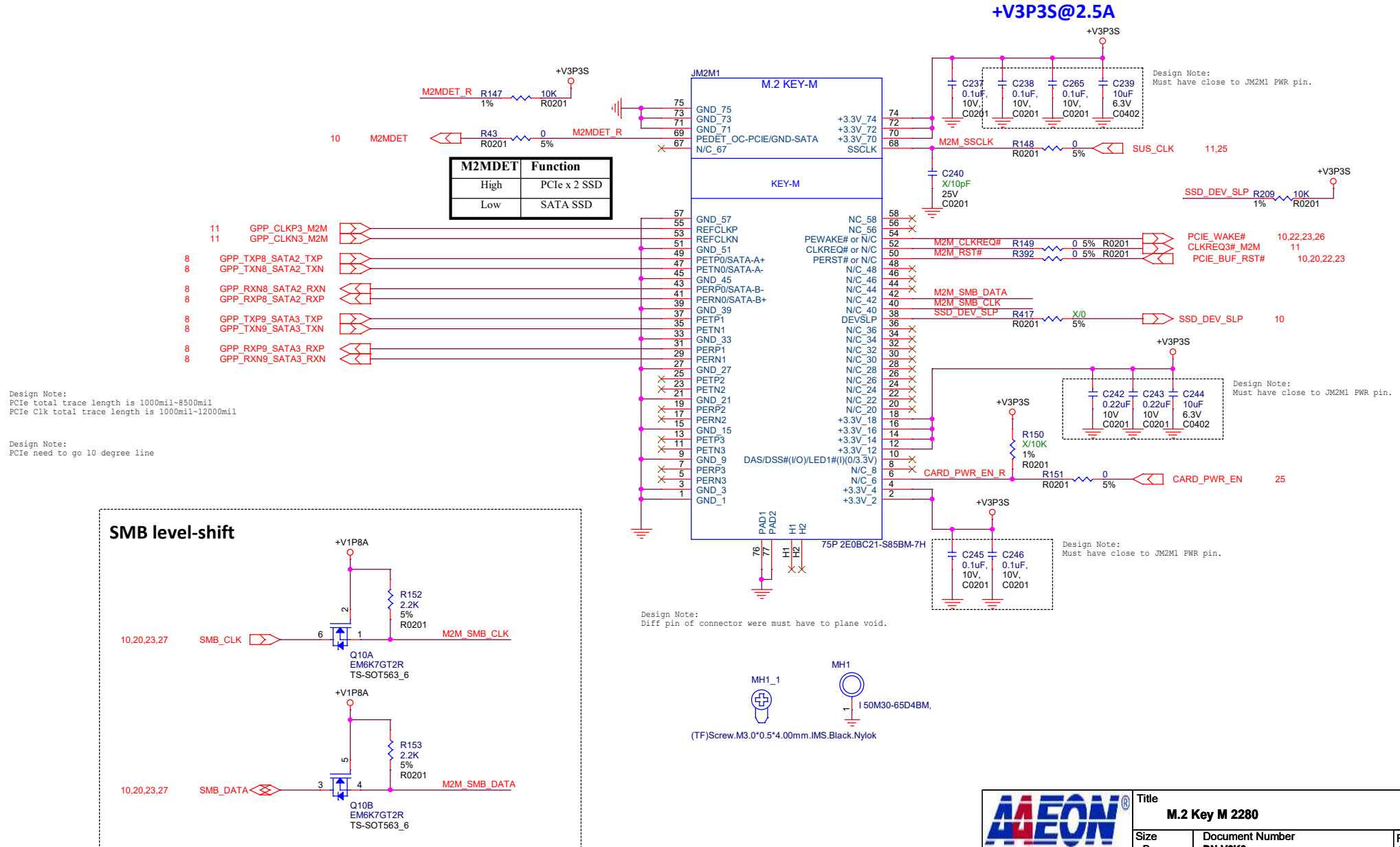
M.2 Key M 2280



M2MDET	Function
High	PCIe x 2 SSD
Low	SATA SSD

Title: M.2 Key M 2280			
Size: B	Document Number: DN-V2K8		Rev: A0.1_0_0
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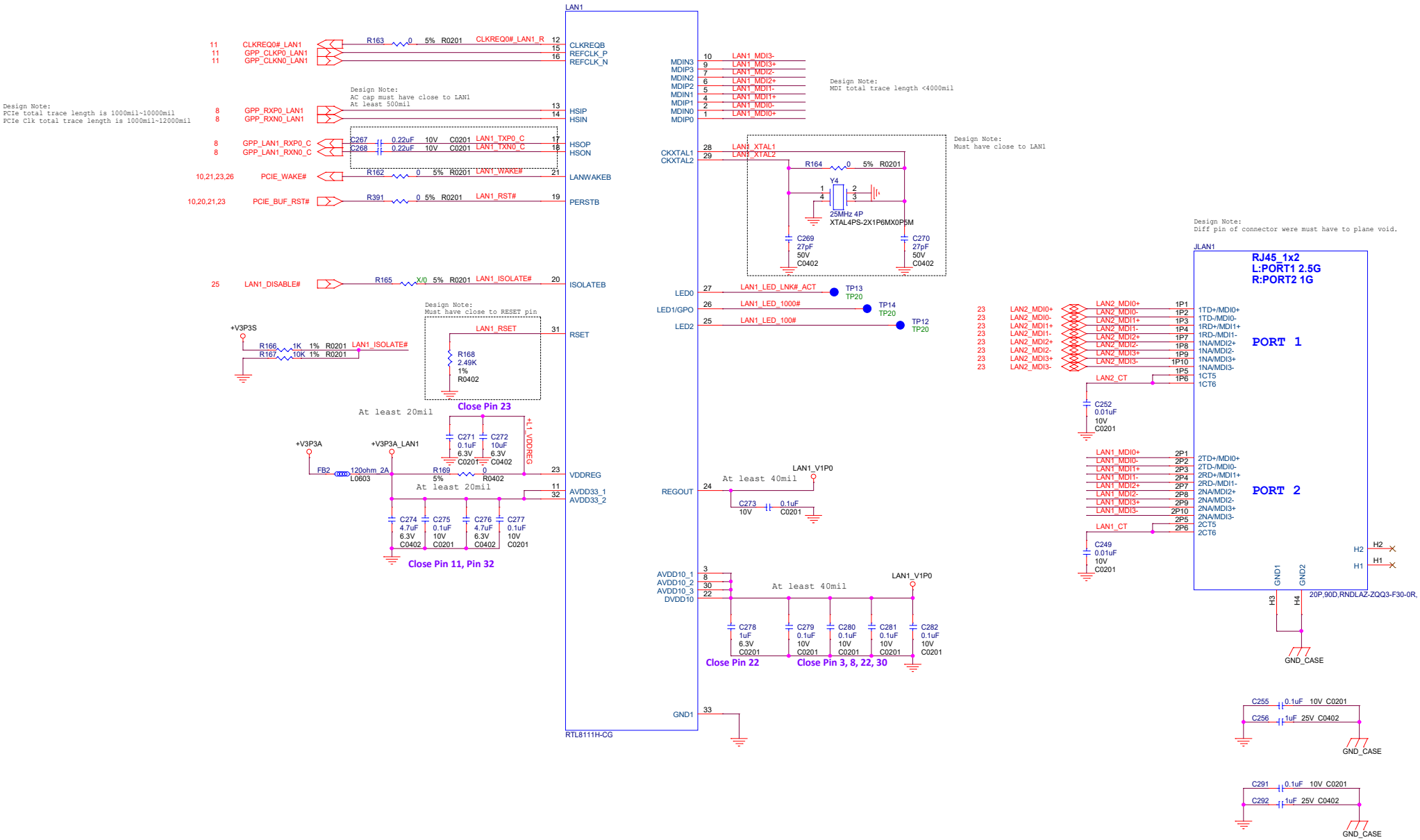
LAN1_RTL8111H



Title: LAN1_RTL8111H		
Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
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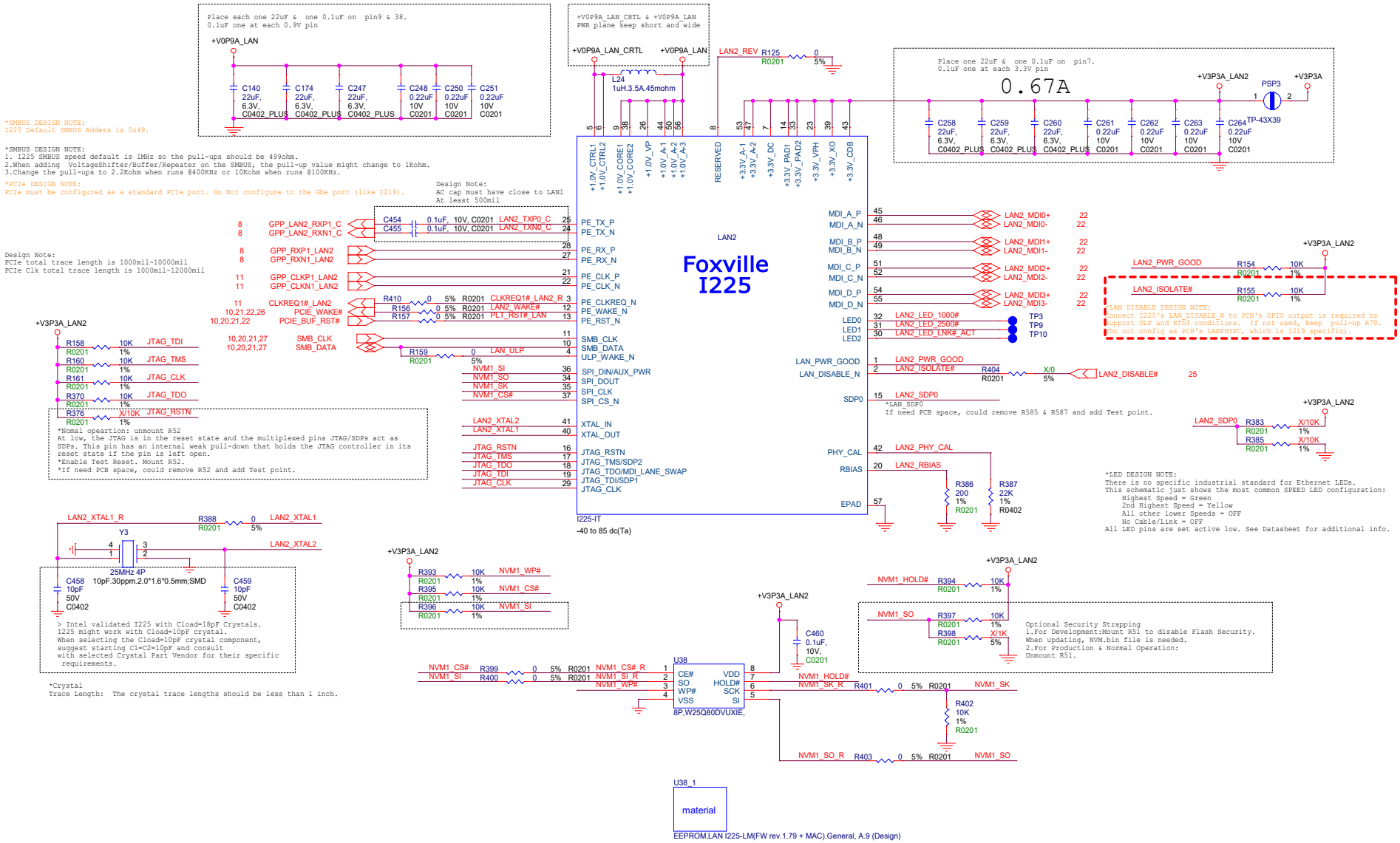
LAN2_I225



Title: LAN2_I225		
Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
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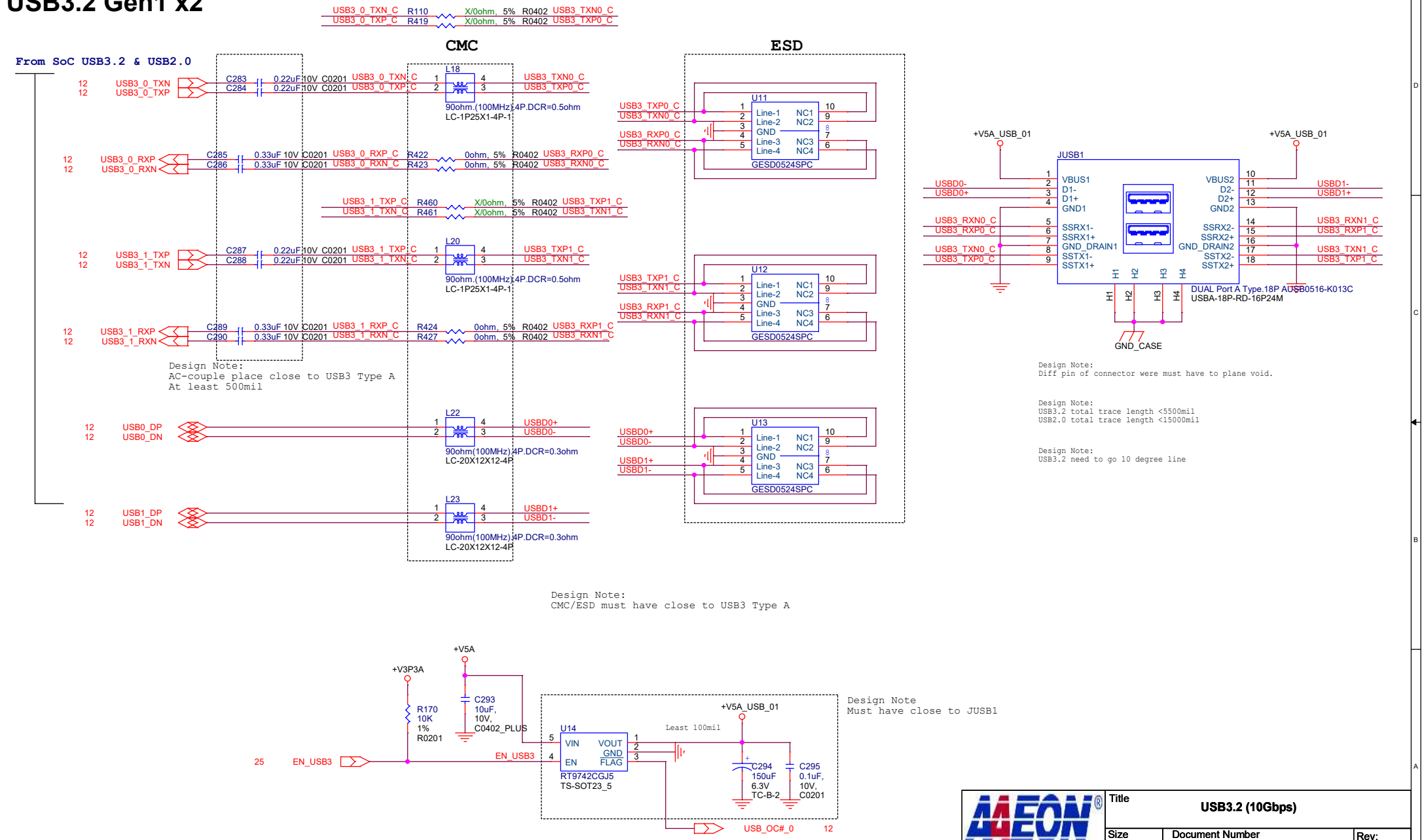
USB3.2 Gen1 x2



AAEON an ASUS assoc. co.	Title: USB3.2 (10Gbps)		
	Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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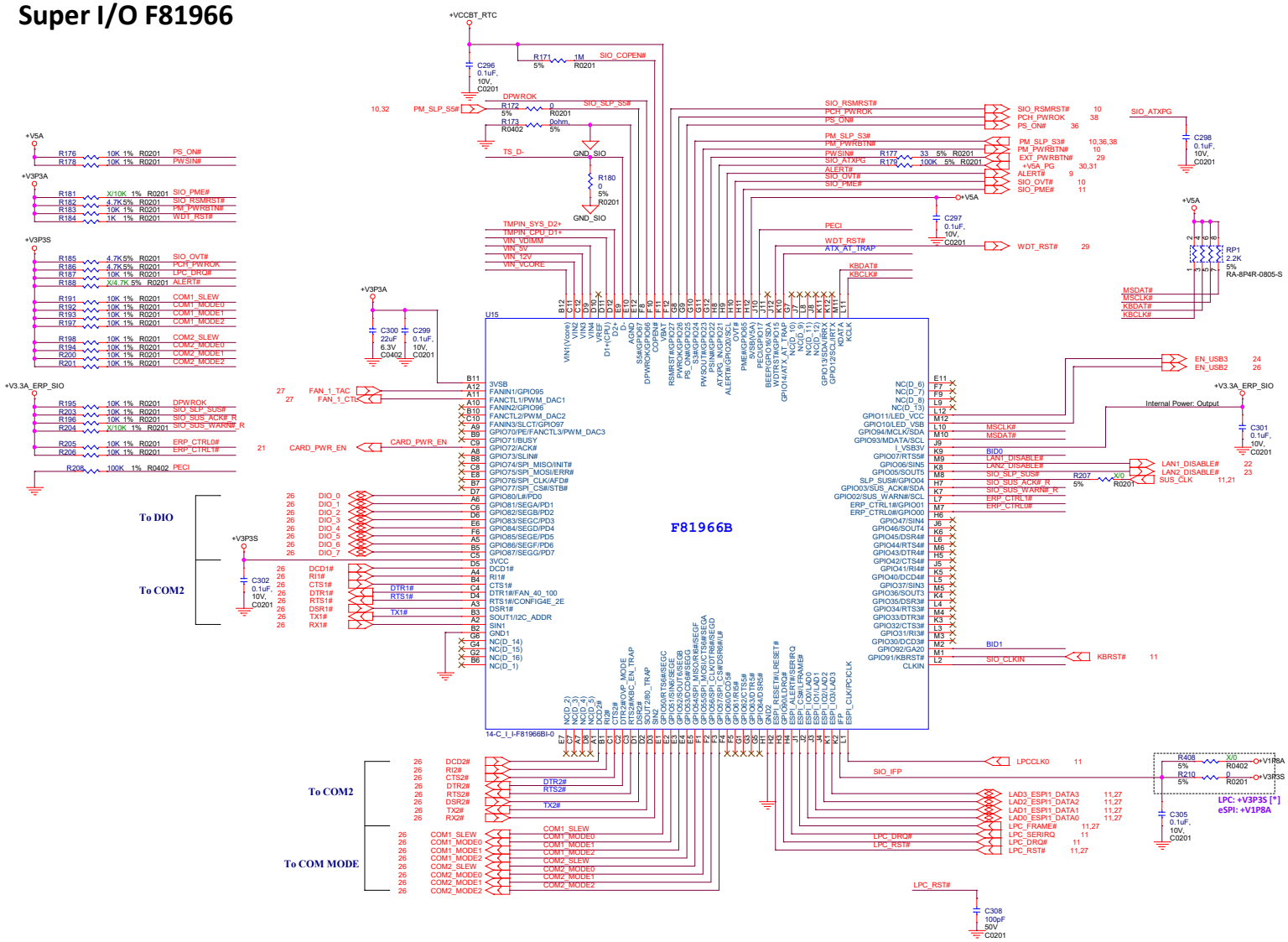
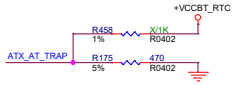
Super I/O F81966

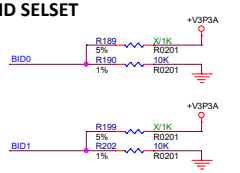


AT/ATX SELECT



PIN69	ATX_AT_TRAP
HIGH	ATX mode (Internal PU_47K)
LOW	AT mode (*)

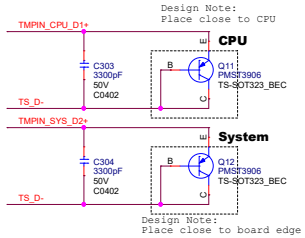
BOARD ID SELSET



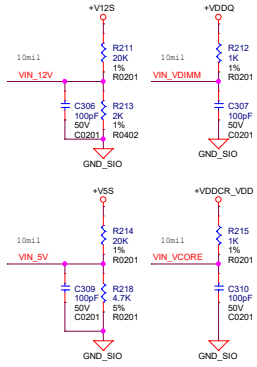
Board ID Mode Selection

Mode	BID0	BID1
Functions1	0 (*)	0 (*)
Functions2	0	1
Functions3	1	0
Functions4	1	1

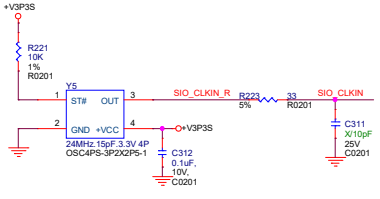
Temperature Monitor



Voltage Monitor



CLOCK Gen.(24MHz)



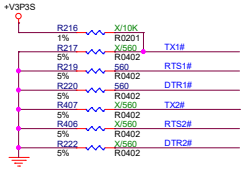
POWER ON OPTION

JP4, B3 (TX1)	I2C_ADDR
HIGH	The I2C slave address is 7h2E.
LOW	The I2C slave address is 7h2D.

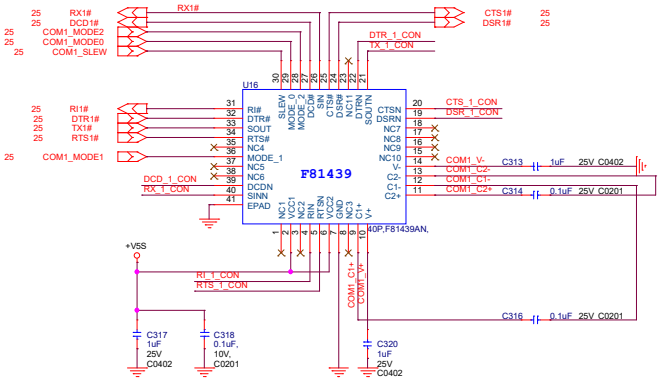
JP3, D4 (RTS1)	Config4E_2E
HIGH	Configuration Register I/O port is 4E/4F.
LOW	**Configuration Register I/O port is 2E/2F.(*)**

JP2, C4 (DTR1)	FAN40_100
HIGH	Power on fan speed default duty is 40%
LOW	**Power on fan speed default duty is 100%.(*)**

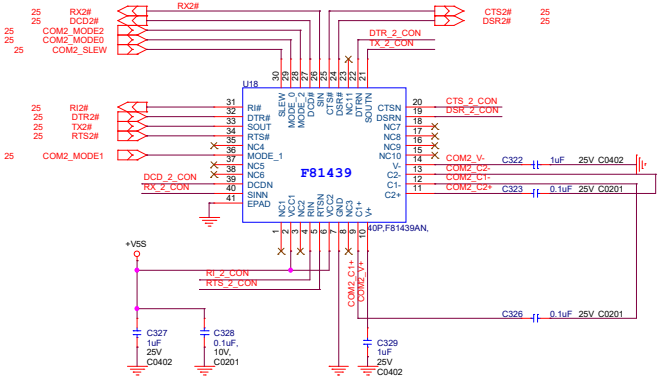
JP1, C2 (DTR2)	OVP_Mode
HIGH	(ALARM mode) Disable OVP function
LOW	(FORCE mode) Enable OVP function



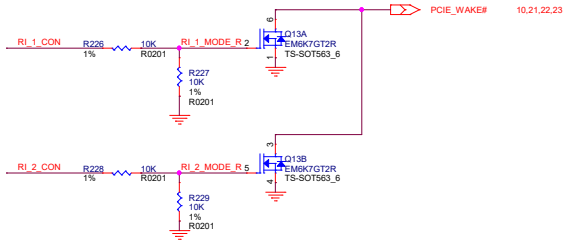
COM1-RS232/RS422/RS485



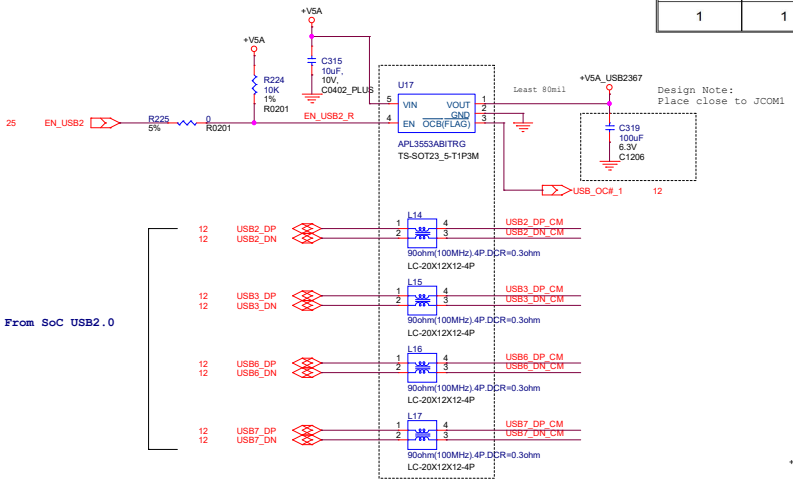
COM2-RS232/RS422/RS485



Wake on Modem



USB2.0 *4 @2A



DIO 8BITS

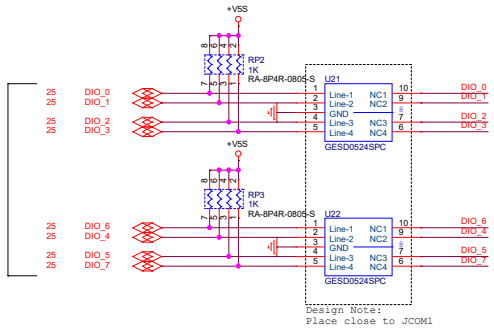
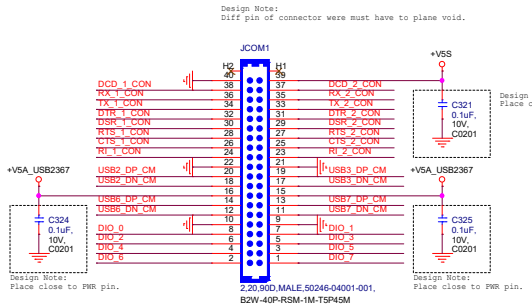


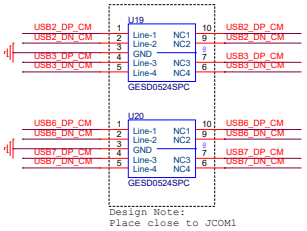
TABLE 1: Mode Select Configuration for F81439

Pin 29 MODE_0	Pin 36 MODE_1	Pin28 MODE_2	Mode	Status
0	0	0	RS-422 Full Duplex	1T/1R RS-422
0	0	1	Pure RS-232	3T/5R RS-232.
0	1	0	RS-485 Half Duplex	1T/1R RS-485, TX ENABLE Low Active
0	1	1	RS-485 Half Duplex	1T/1R RS-485, TX ENABLE High Active
1	0	0	RS-422 Full Duplex	1T/1R RS-422 with termination resistor
1	0	1	Pure RS-232	1T/1R RS-232 co-exists with RS485 application without the need for the bus switch IC (for special usage).
1	1	0	RS-485 Half Duplex	1T/1R RS-485 with termination resistor TX ENABLE Low Active
1	1	1	Low Power Shutdown	All I/O pins are High Impedance

Pin Mapping			
	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps





Title	COM PORT/USB2.0/DIO	
Size: Custom	Document Number: DN-V2K8	Rev: A0.1_0_0
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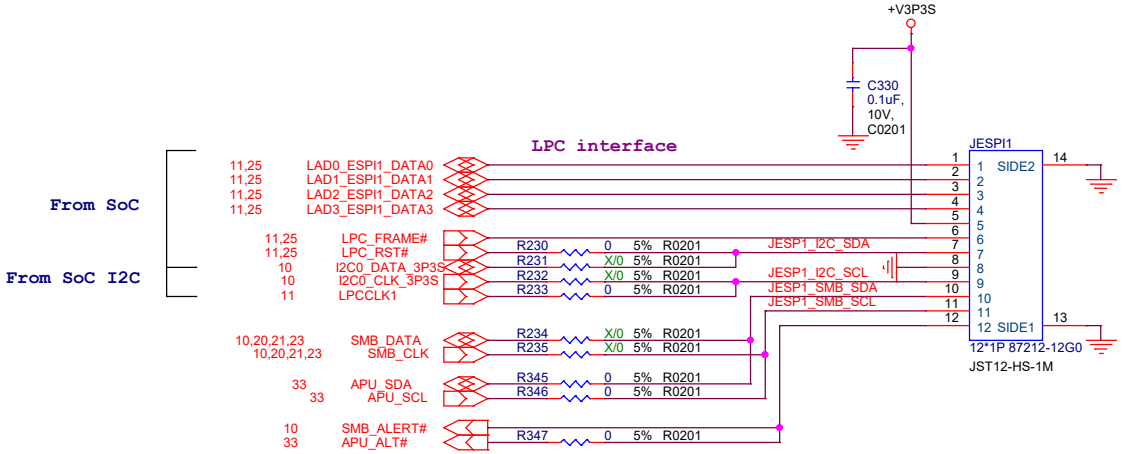
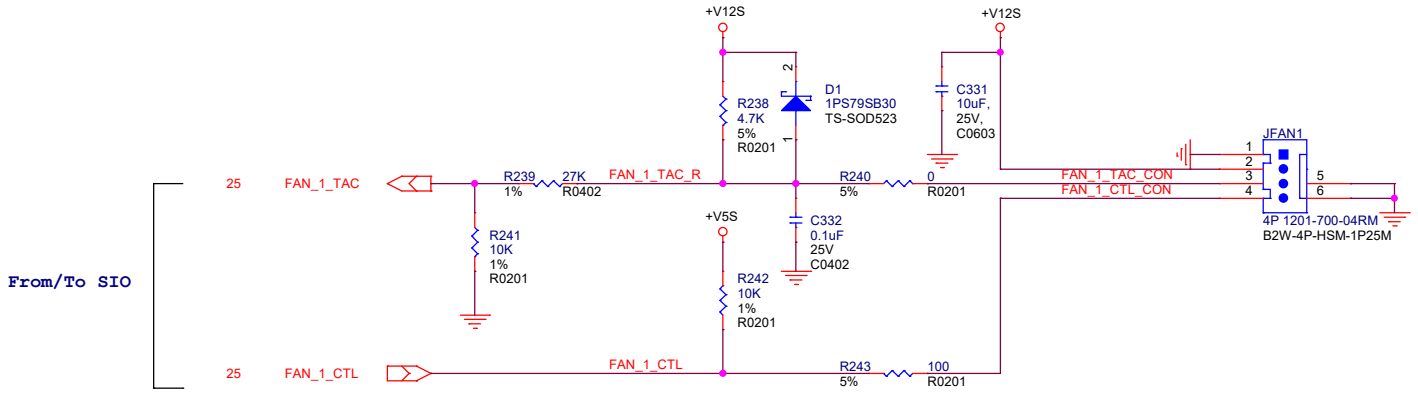
Port 80



Smart FAN



AAEON an ASUS assoc. co.	Title: Port 80 / FAN	
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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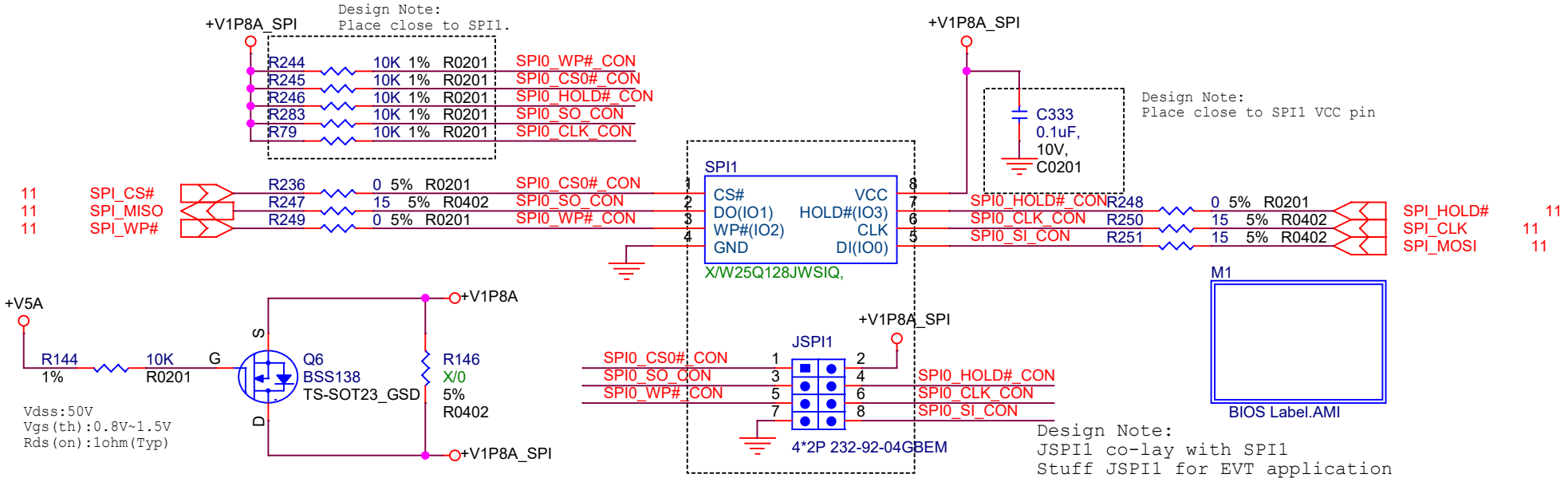
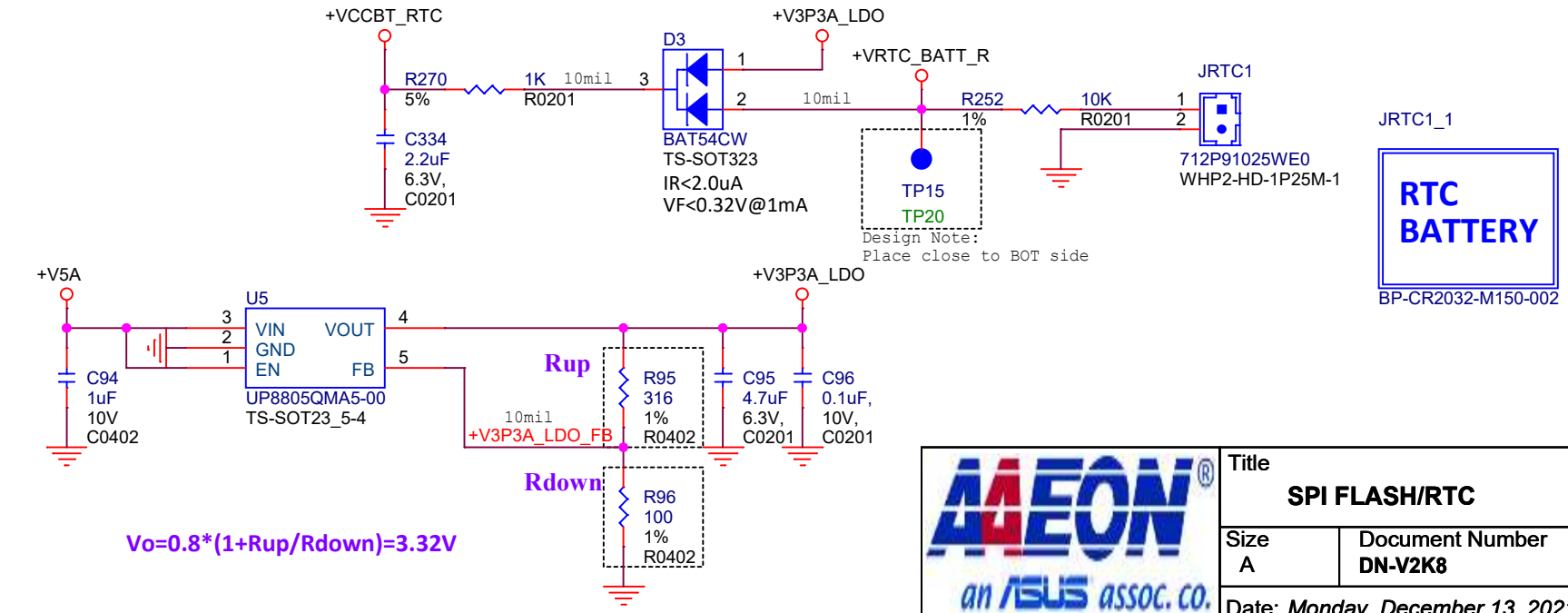
SPI FLASH



RTC



AAEON an ASUS assoc. co.

Title: **SPI FLASH/RTC**		
Size: A	Document Number: **DN-V2K8**	Rev: **A0.1_0_0**
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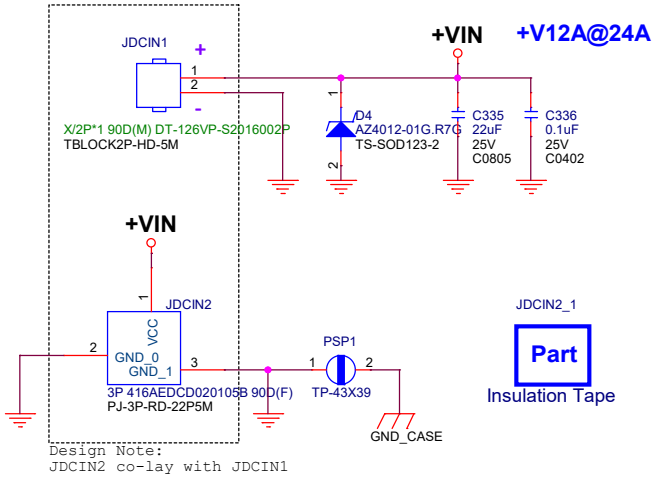
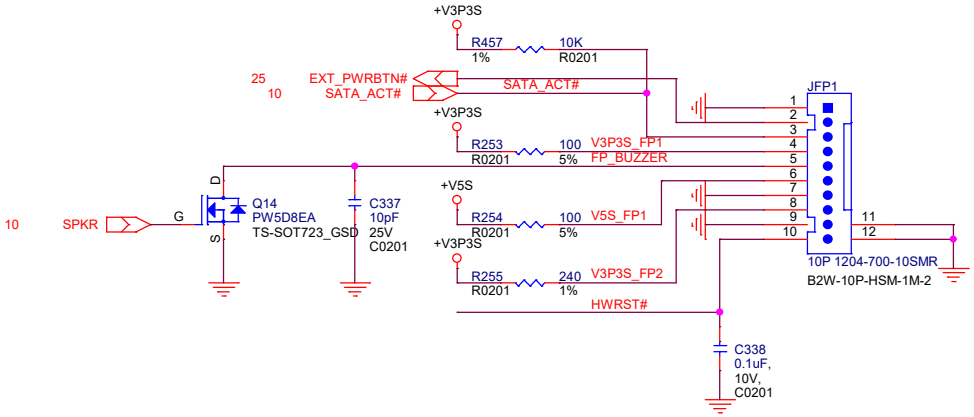
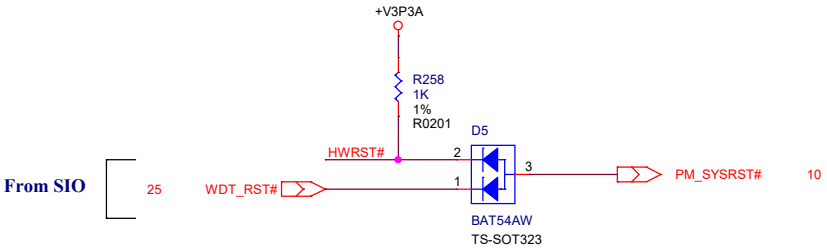
DCIN_12V



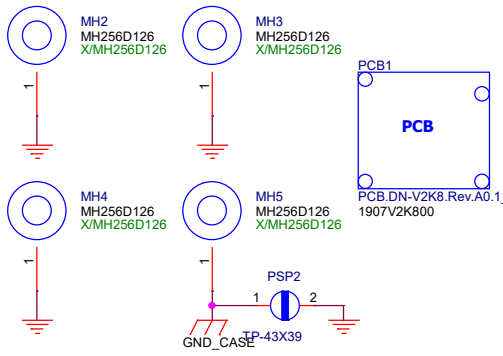
Front Panel



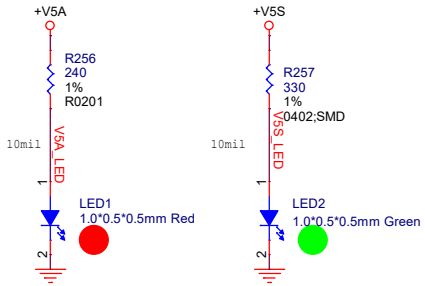
System Reset



Screw Hole(Non-PTH)



LED



AAEON an ASUS assoc. co.	Title: DC IN/MISC	
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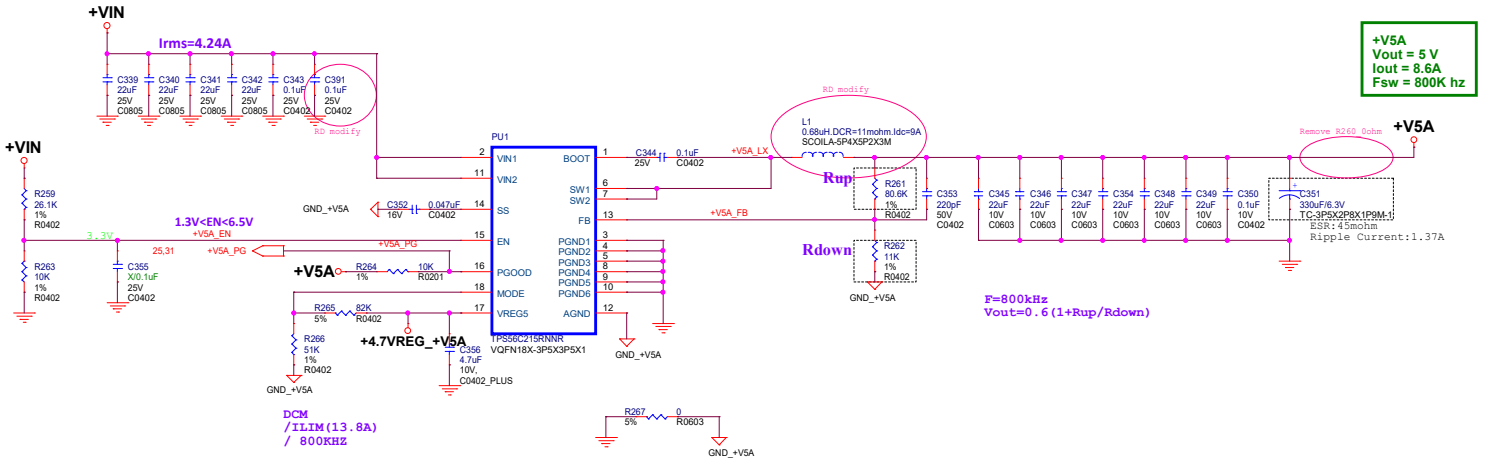
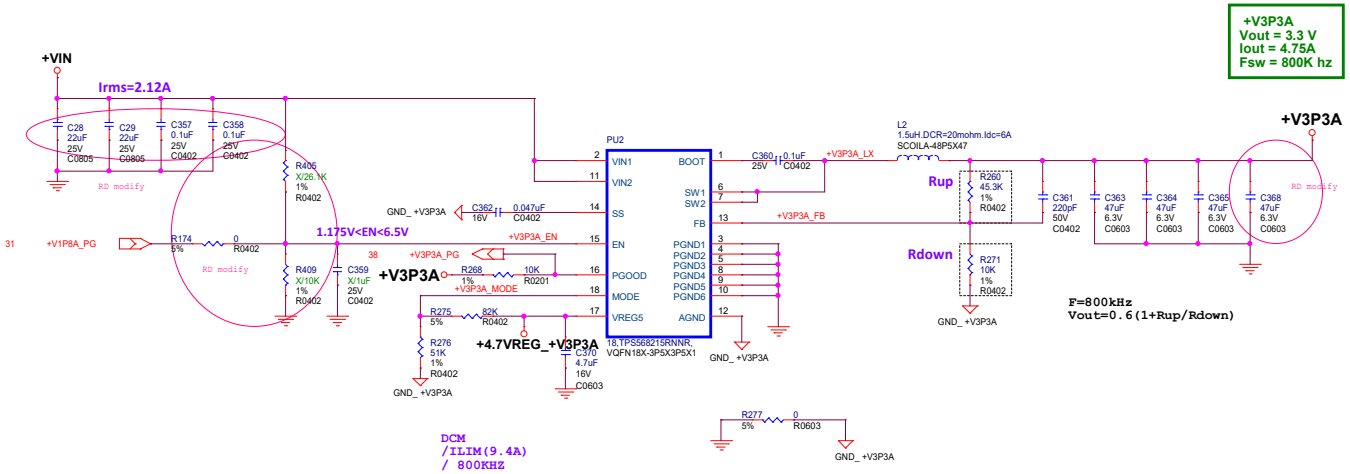
PWR_+V5A@8.6A



PWR_+V3P3A@4.75A



AAEON an ASUS assoc. co.

Title: PWR01_+V3P3A/ +V5A		
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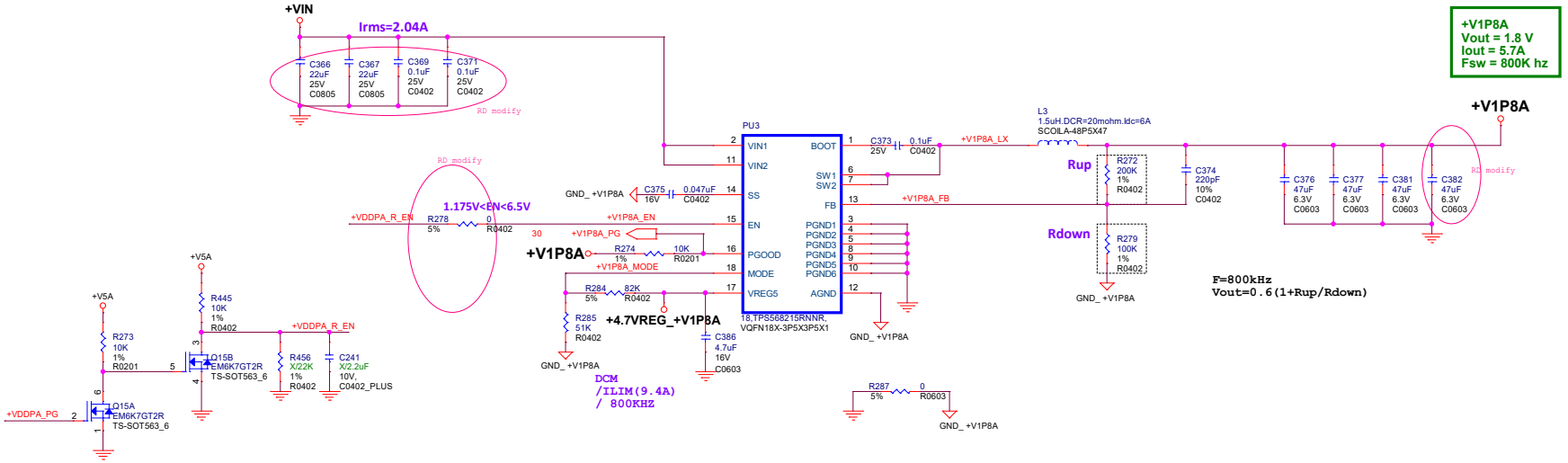
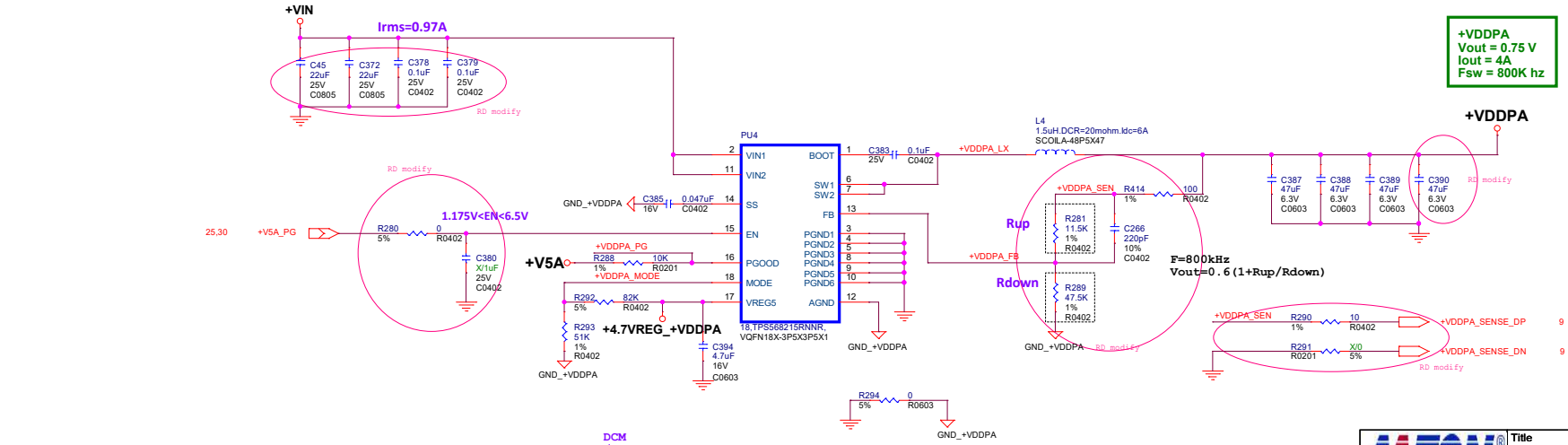
PWR_+V1P8A@5.7A



PWR_+VDDPA@4A



AAEON an ASUS assoc. co.	Title: PWR02_+V1P8A/ +VDDPA(0.75V)	
	Size: Custom	Document Number: DN-V2K8 — Rev: A0.1_0_0
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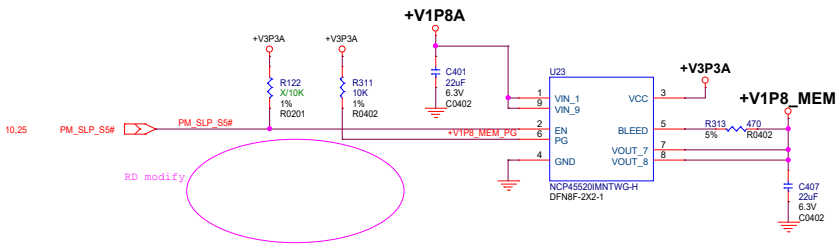
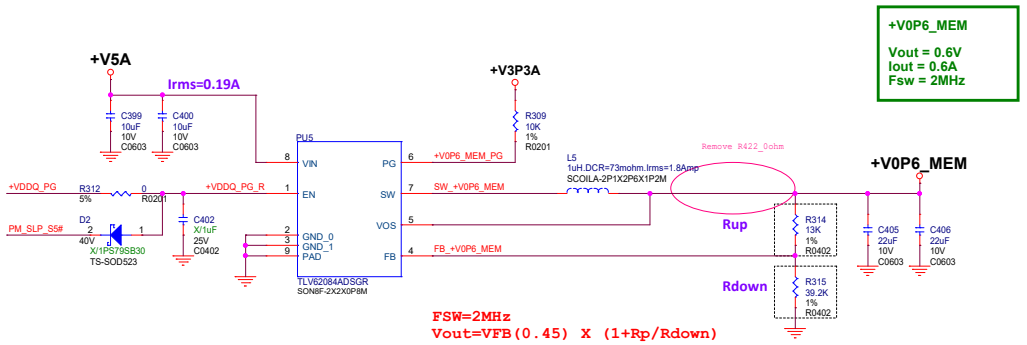
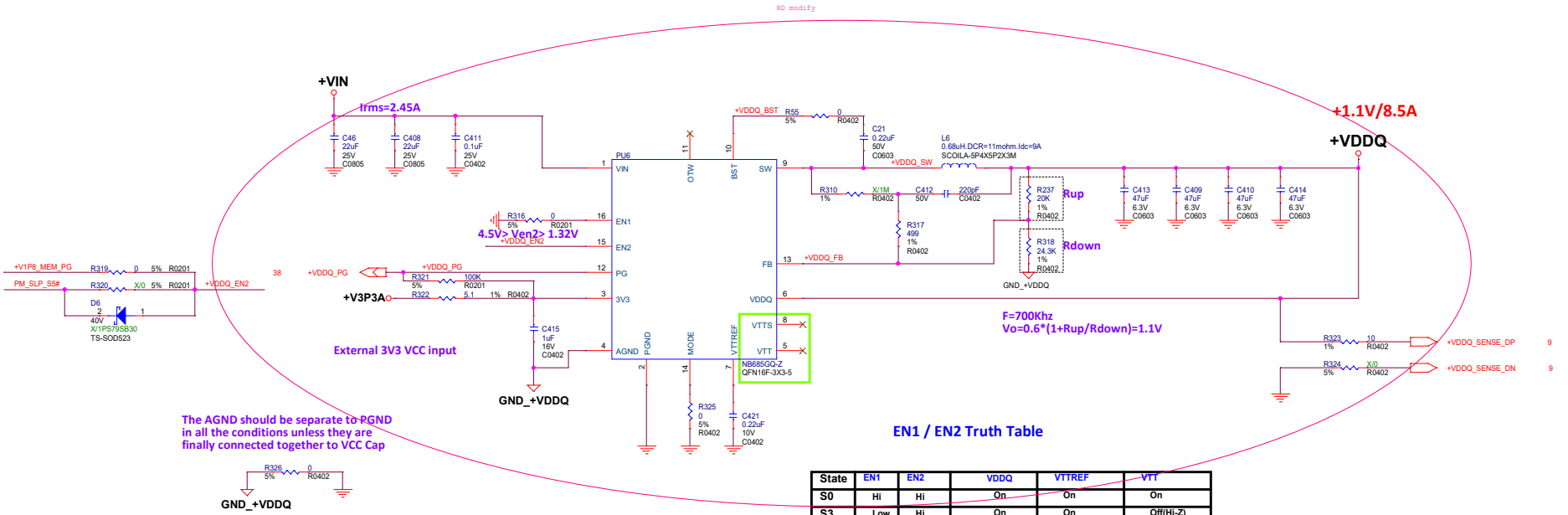
PWR_+V1P8_MEM@1A



PWR_+V0P6_MEM@0.6A



PWR_+VDDQ@8.5A



EN1 / EN2 Truth Table

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off(Hi-Z)
S4/S5	Low	Low	Off(Discharge)	Off(Discharge)	Off(Discharge)

AAEON an ASUS assoc. co.

Title: PWR03_+VDDQ/ +V0P6S_MEM

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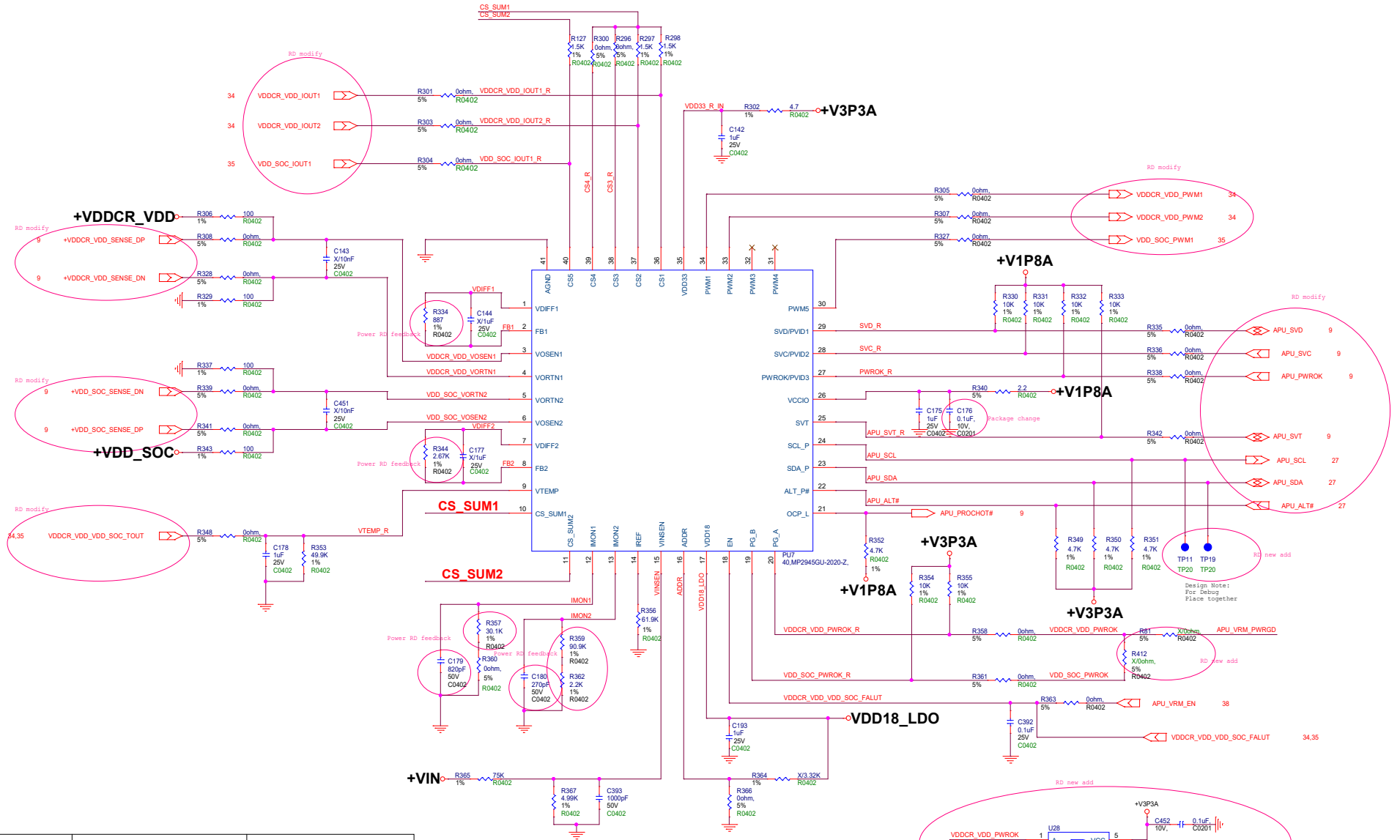
PWR_MP2945GU



	+VDDCR_VDD / 600KHz	+VDD_SOC / 600KHz
TDC		
IccMax	70A	17A
Vboot	Variable	Variable
Load Line	0.7mohm	2.1mohm
AMD SVI2		

AAEON an ASUS assoc. co.	Title: PWR04_ISL62776_VDDCR_VDD&SOC	
	Size: C	Document Number: DN-V2K8 — Rev: A0.1_0_0
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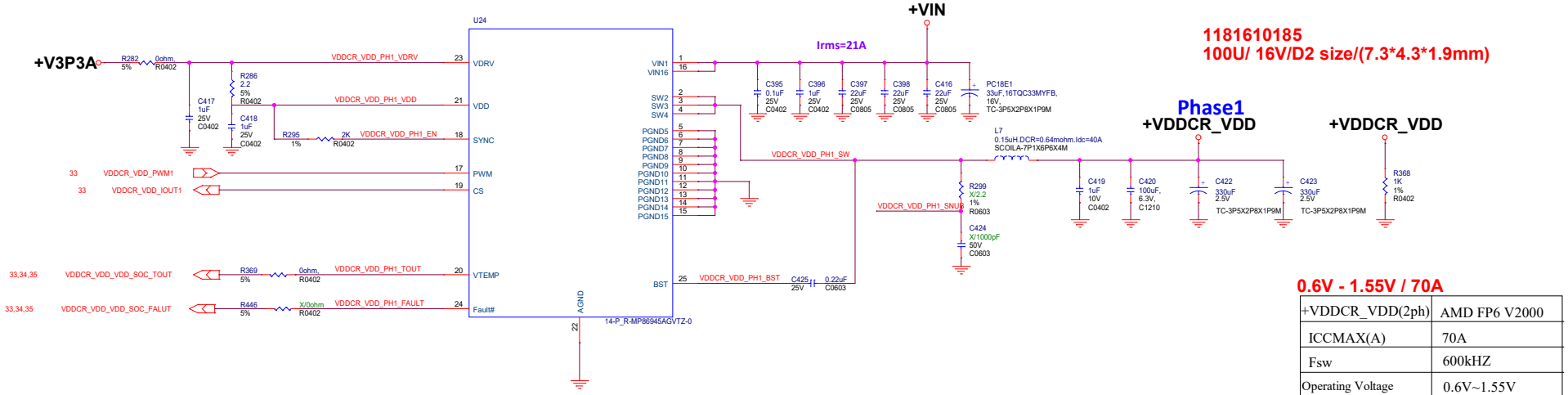
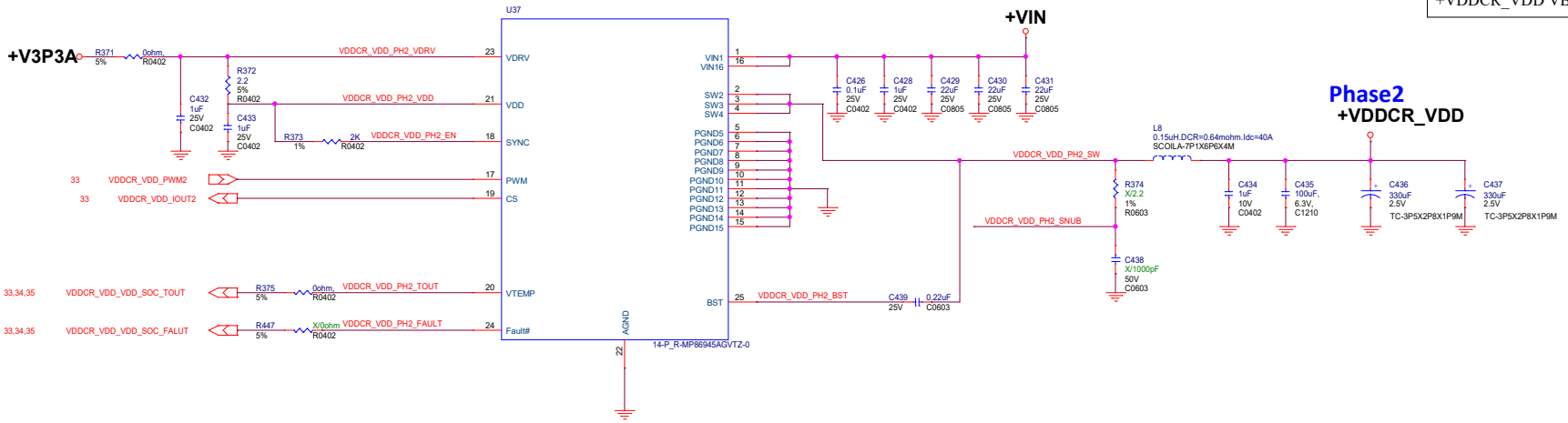
PWR_+VDDCR_VDD@70A



0.6V - 1.55V / 70A	
+VDDCR_VDD(2ph)	AMD FP6 V2000
ICCMAX(A)	70A
Fsw	600kHZ
Operating Voltage	0.6V~1.55V
DC_LL	0.7mohm
DCR	0.64mohm
OCP	70A*130%=91A
OTP	100 Degree
+VDDCR_VDD VBoot setting : Variable	



AAEON an ASUS assoc. co.	Title: PWR05_+VDDCR_VDD_2phase		
	Size: C	Document Number: DN-V2K8	Rev: A0.1_0_0
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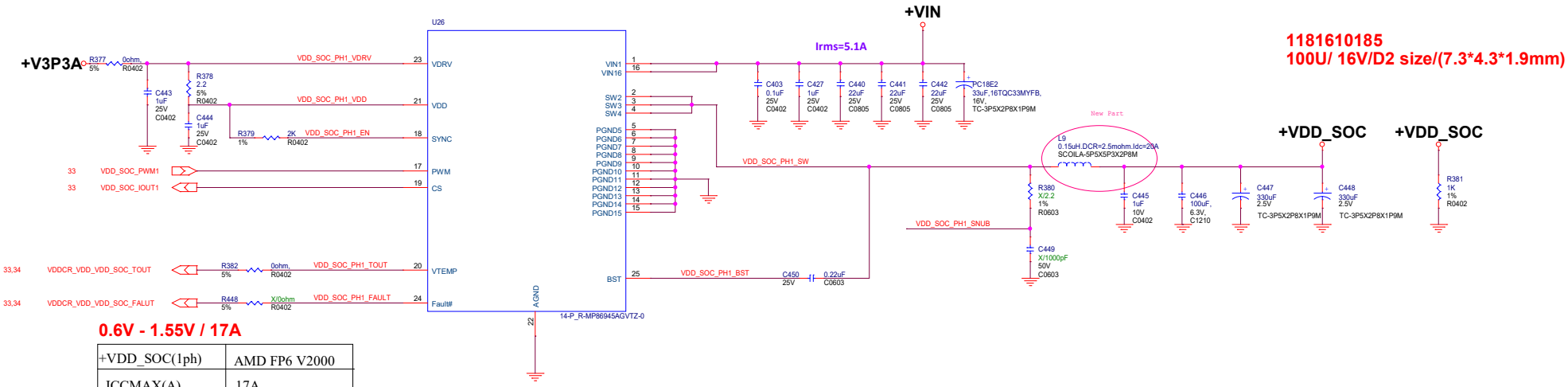
PWR_+VDD_SOC@17A



0.6V - 1.55V / 17A

+VDD_SOC(1ph)	AMD FP6 V2000
ICCMAX(A)	17A
Fsw	600kHZ
Operating Voltage	0.6V~1.55V
DC_LL	2.1mohm
DCR	0.64mohm
OCP	17A*130%=22.1A
OTP	100 Degree
+VDD_SOC VBoot setting : Variable	

AAEON an ASUS assoc. co.

Title: PWR06_+VDD_SOC_1phase

Size: C | Document Number: DN-V2K8 | Rev: A0.1_0_0

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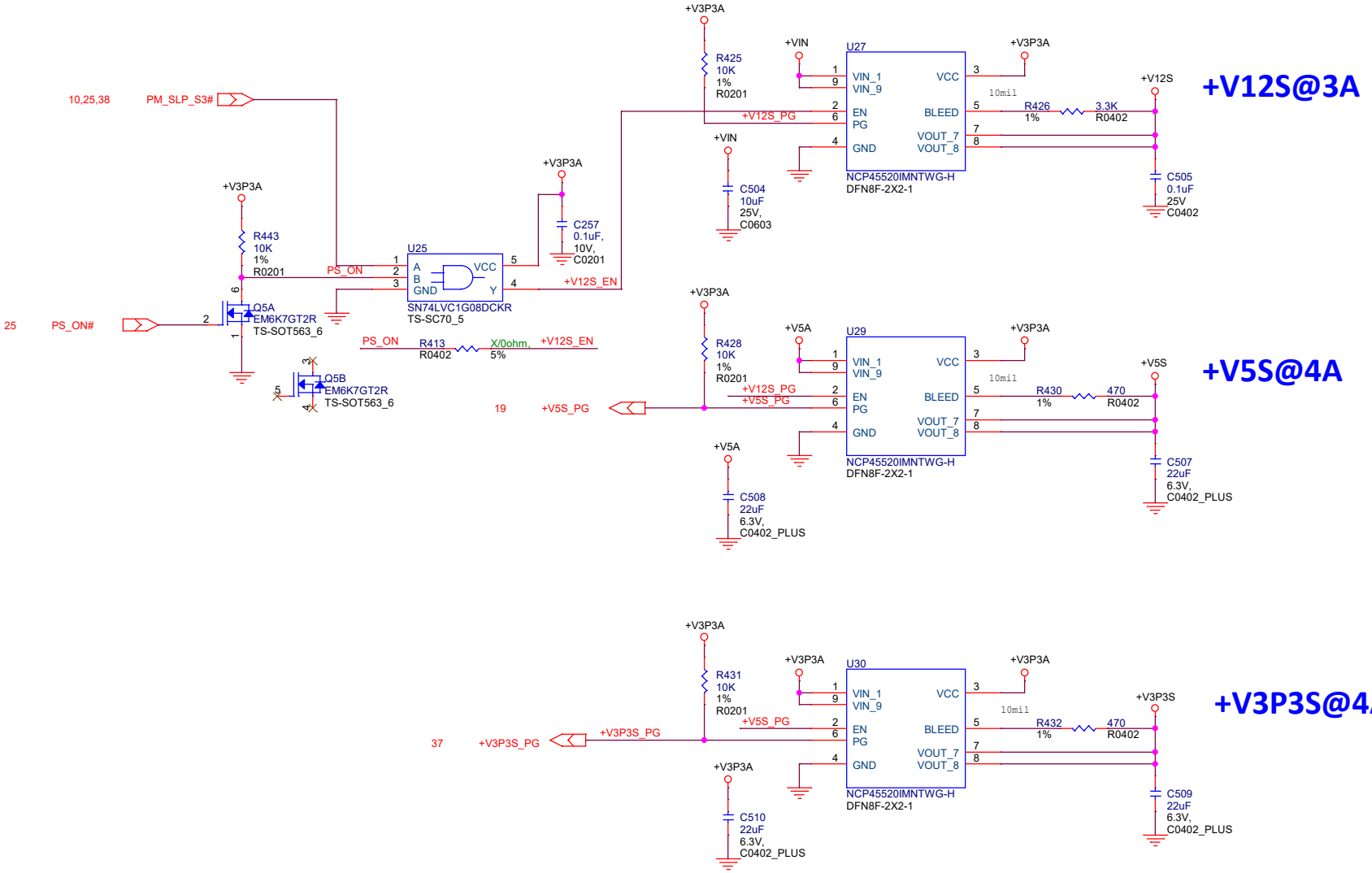
SYSTEM POWER



Title: PWR07_+V12S/+V5S/+V3P3S		
Size: B	Document Number: DN-V2K8	Rev: A0.1_0_0
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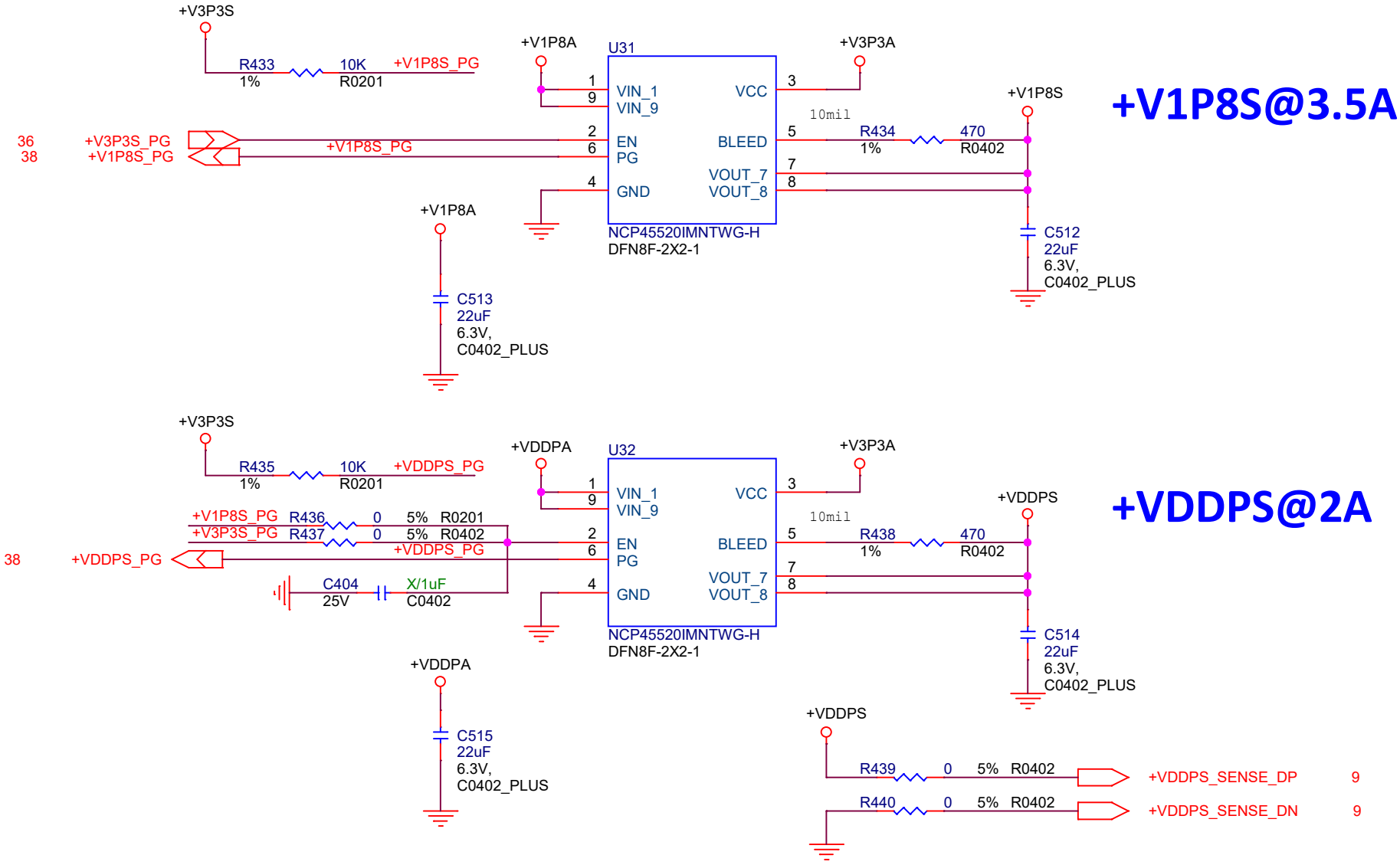

AAEON an ASUS assoc. co.	Title: **PWR08_+V1P8S/ +VDDPS**	
Size: A	Document Number: **DN-V2K8**	Rev: **A0.1_0_0**
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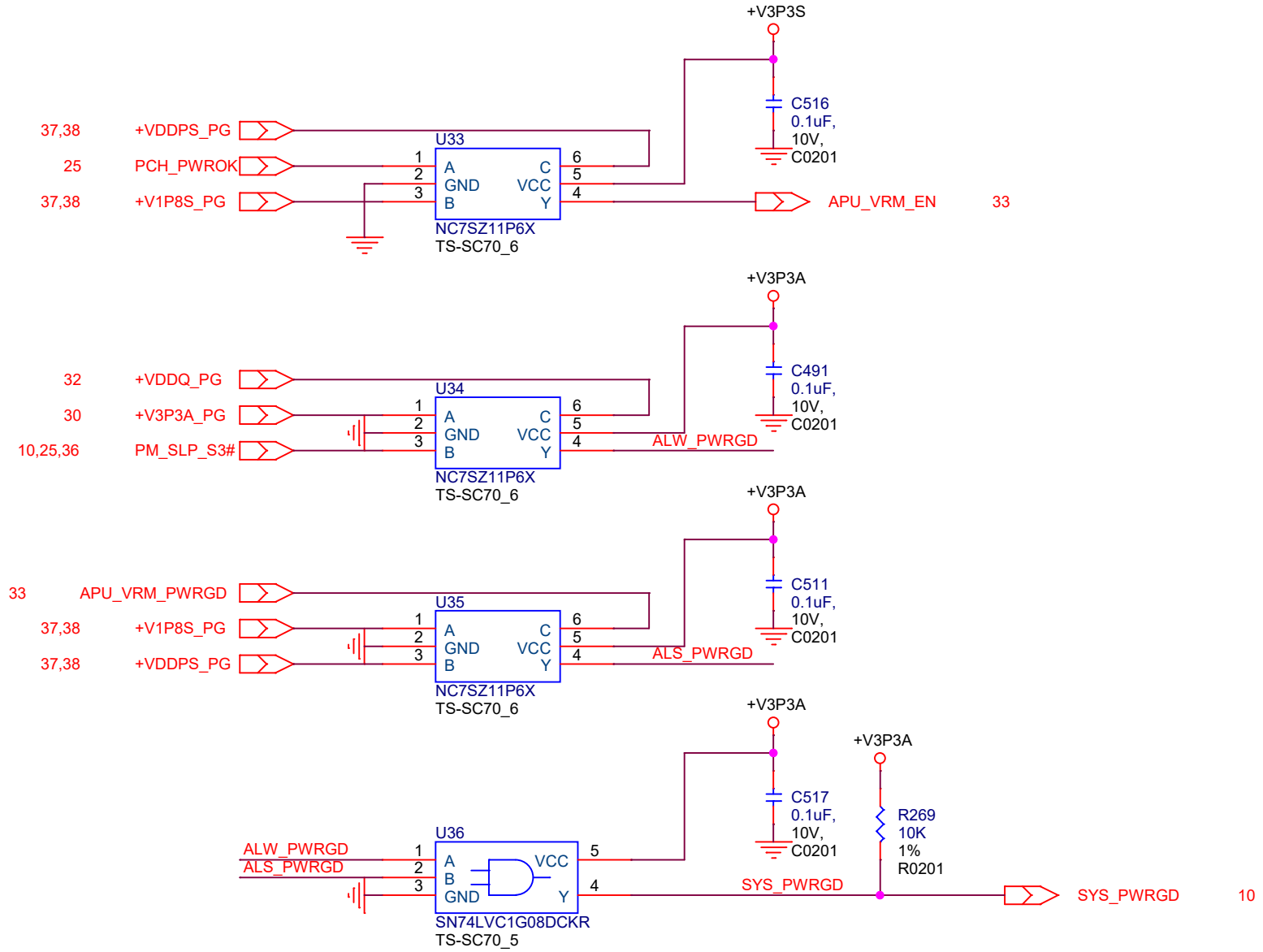
SEQUENCE



AAEON an ASUS assoc. co.	Title: **SEQUENCE**	
Size: A	Document Number: **DN-V2K8**	Rev: **A0.1_0_0**
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Change History

Date	Revision	Page	Modification	Reason
2021/03/12	A0.1	1 ~ 46	First Release.	

AAEON an ASUS assoc. co.	Title: HISTORY		
	Size: C	Document Number: DN-V2K8	Rev: A0.1_0_0
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