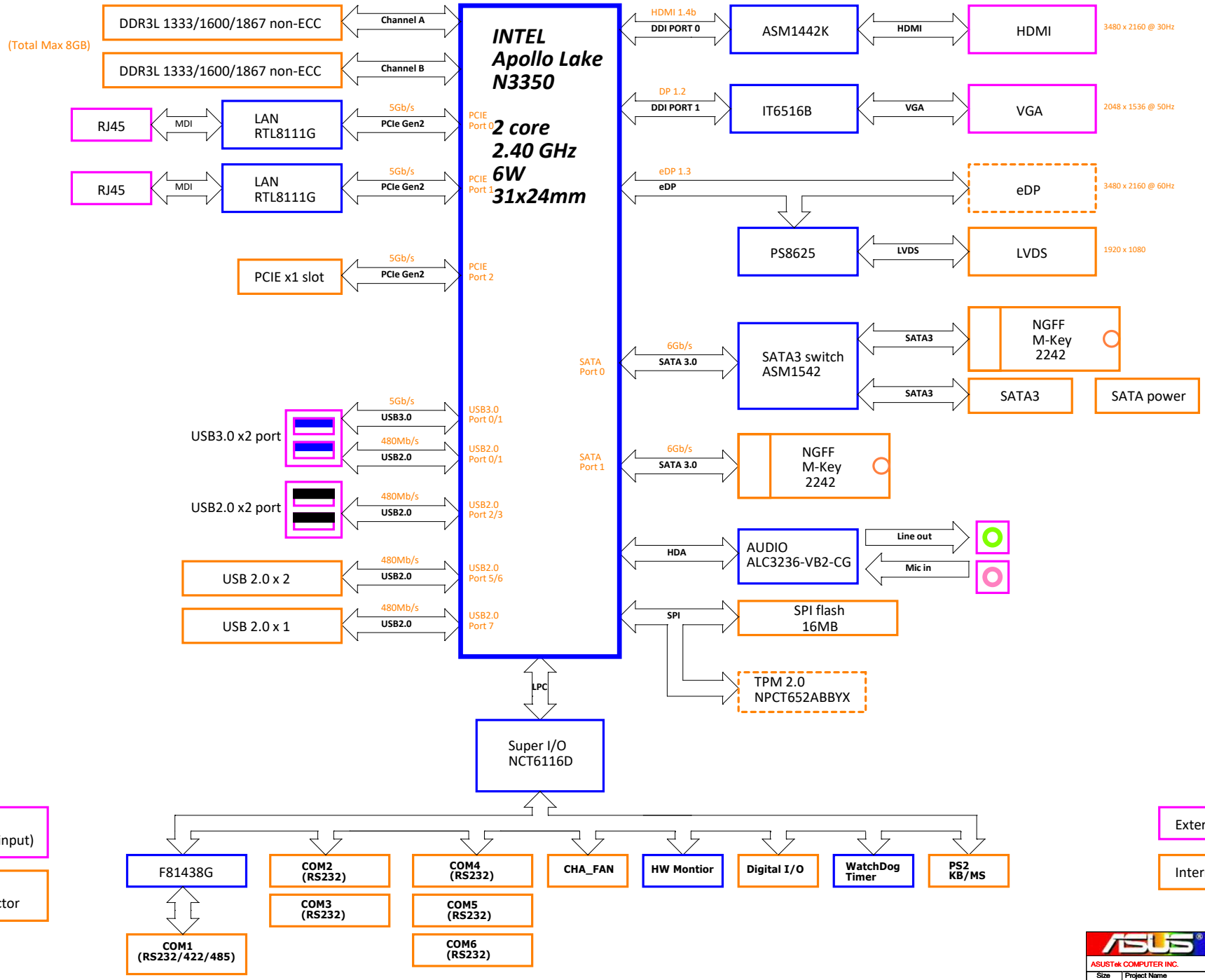
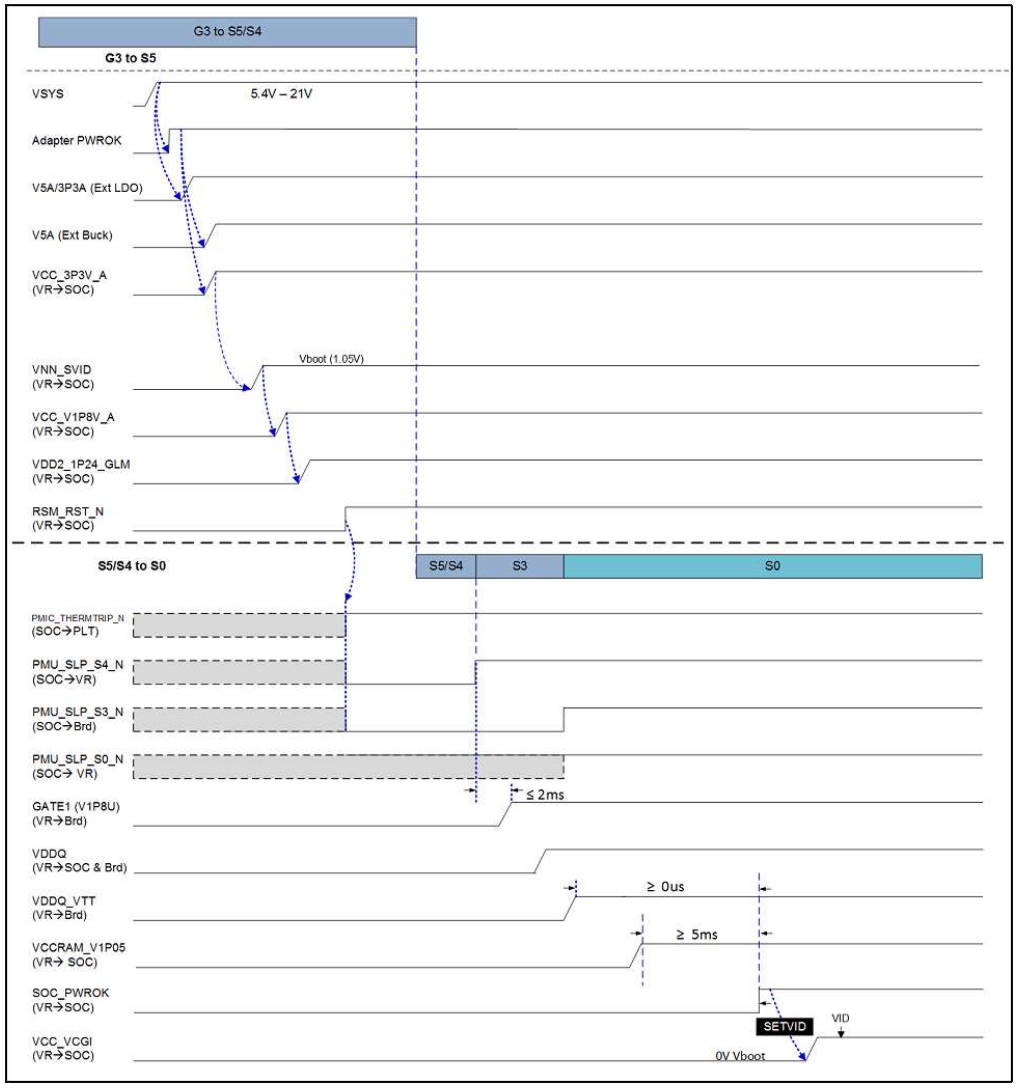
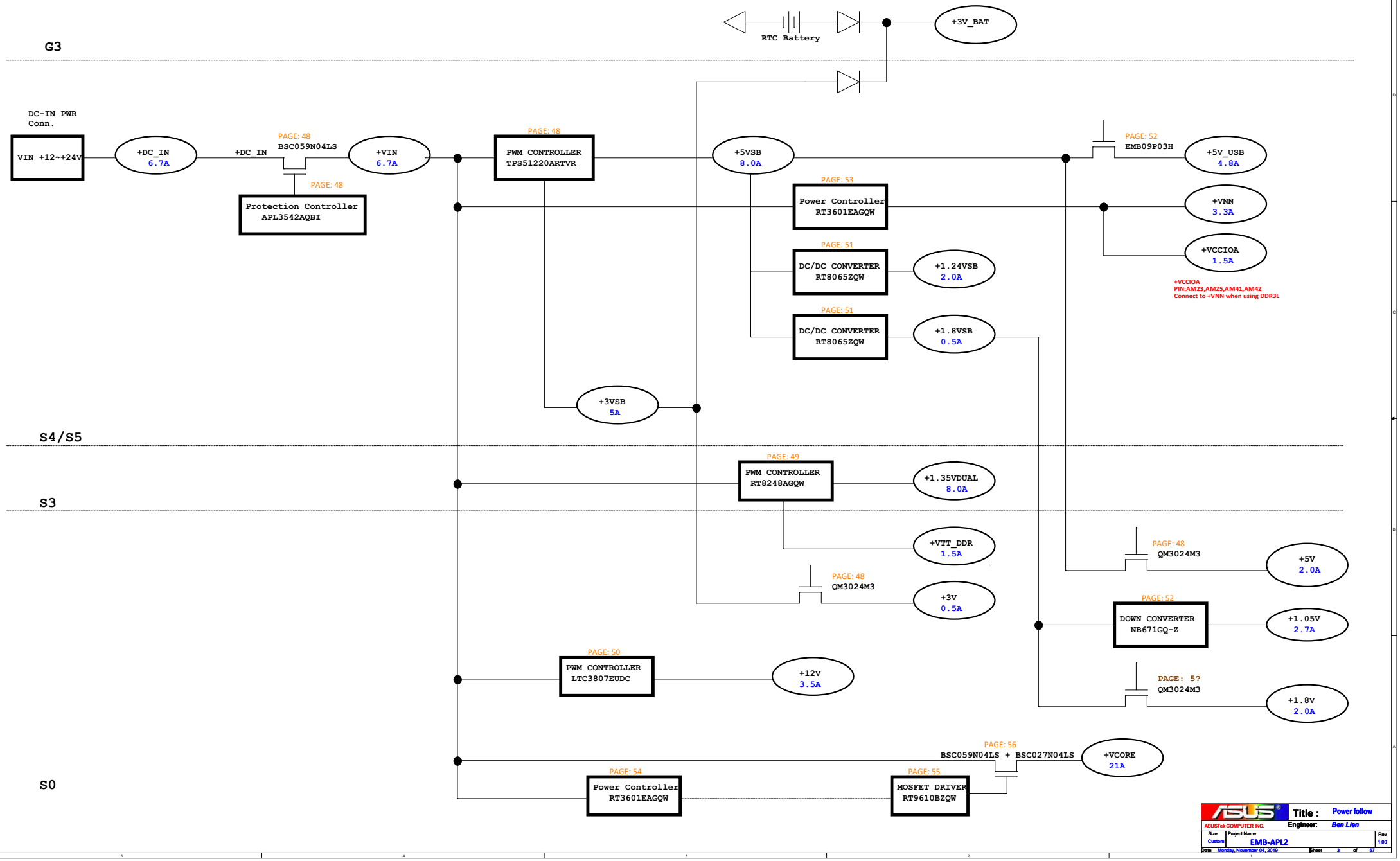
EMB-APL2 (Kumahira)



Title :	Block Diagram
ASUSTek COMPUTER INC.	Engineer: Ben Lien
Size: Custom	Project Name: EMB-APL2
Rev: 1.00	
Date: Monday, November 04, 2019	Sheet 1 of 57



ASUSTek COMPUTER INC.	Title : Power ON seqence	
	Engineer: Ben Lien	
Size: C	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 2 of 57	


G3
RTC Battery
+3V_BAT
DC-IN PWR Conn.
VIN +12~+24V
+DC_IN 6.7A
+DC_IN
PAGE: 48
BSC059N04LS
+VIN 6.7A
PAGE: 48
Protection Controller APL3542AQBI
PAGE: 48
PWM CONTROLLER TPS51220ARTVR
+5VSB 8.0A
PAGE: 53
Power Controller RT3601EAGQW
PAGE: 51
DC/DC CONVERTER RT8065ZQW
+1.24VSB 2.0A
PAGE: 51
DC/DC CONVERTER RT8065ZQW
+1.8VSB 0.5A
+3VSB 5A
PAGE: 52
EMB09P03H
+5V_USB 4.8A
+VNN 3.3A
+VCCIOA 1.5A
+VCCIOA
PIN:AM23,AM25,AM41,AM42
Connect to +VNN when using DDR3L
S4/S5
S3
PAGE: 49
PWM CONTROLLER RT8248AGQW
+1.35VDUAL 8.0A
+VTT_DDR 1.5A
PAGE: 48
QM3024M3
+3V 0.5A
PAGE: 48
QM3024M3
+5V 2.0A
PAGE: 52
DOWN CONVERTER NB671GQ-Z
+1.05V 2.7A
PAGE: 5?
QM3024M3
+1.8V 2.0A
PAGE: 50
PWM CONTROLLER LTC3807EUDC
+12V 3.5A
S0
PAGE: 56
BSC059N04LS + BSC027N04LS
+VCORE 21A
PAGE: 54
Power Controller RT3601EAGQW
PAGE: 55
MOSFET DRIVER RT9610BZQW
ASUSTek COMPUTER INC.
Title : Power follow
Engineer: Ben Lien
Size Custom
Project Name EMB-APL2
Rev 1.00
Date: Monday, November 04, 2019
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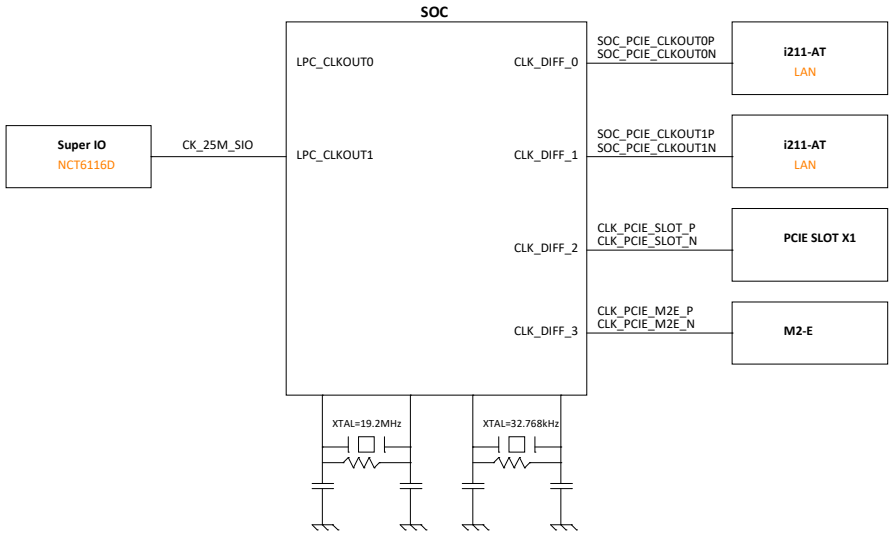

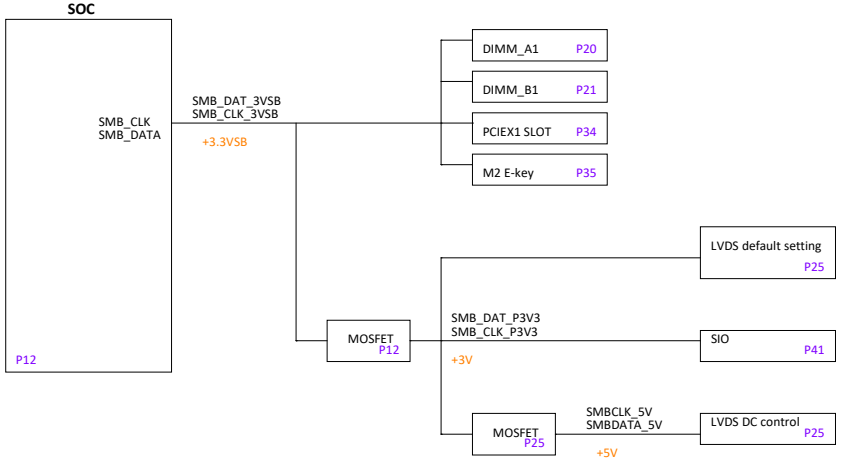

ASUSTek COMPUTER INC.	Title : CLK/I2C map	
	Engineer: Ben Lien	
Size: C	Project Name: EMB-APL2	Rev: 1.00
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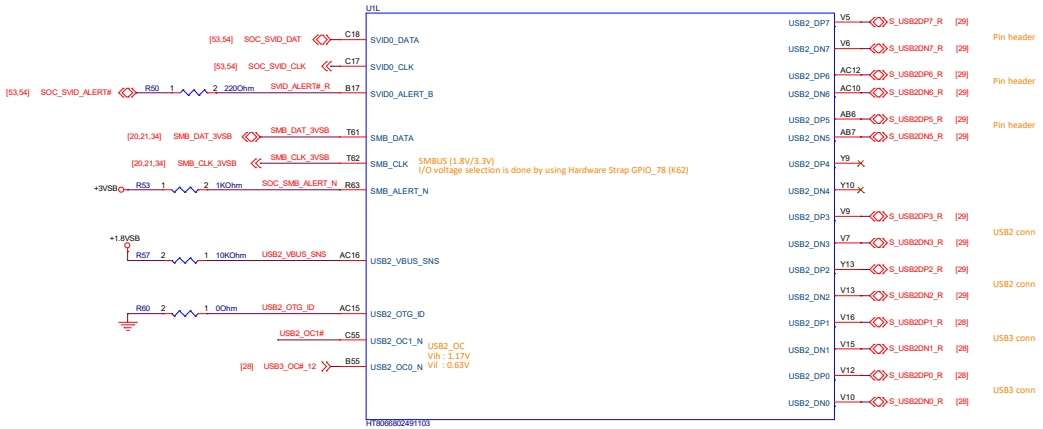
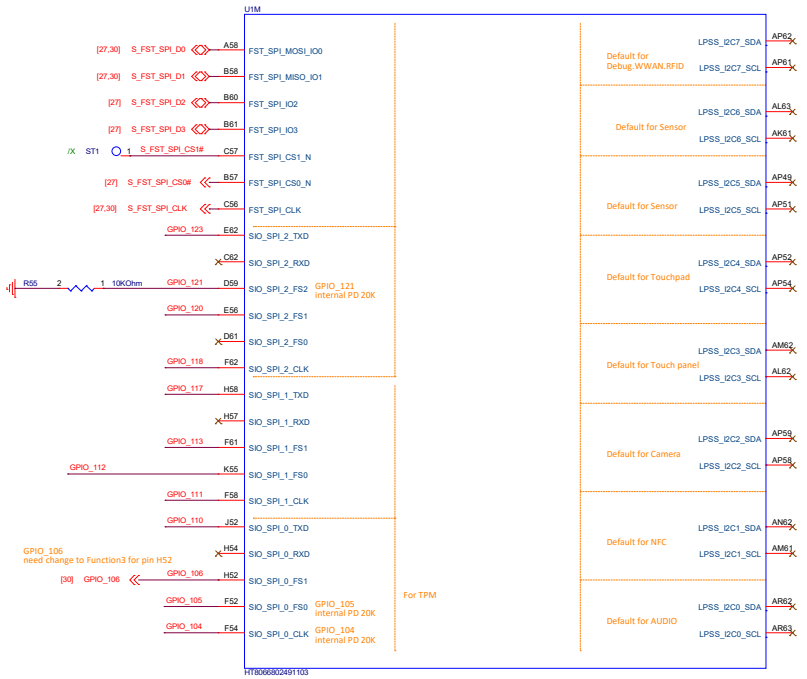
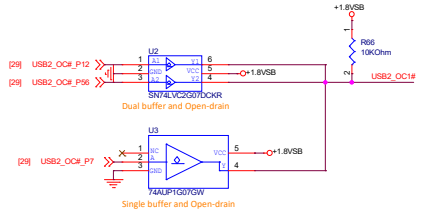
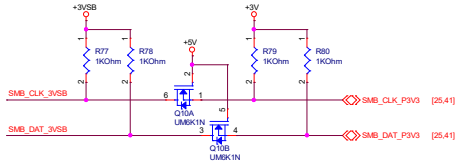
CORE - SOC - SVID/SMBUS/USB2

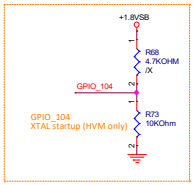


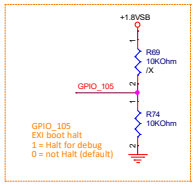
CORE - SOC - SPI/I2C

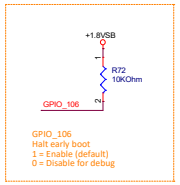


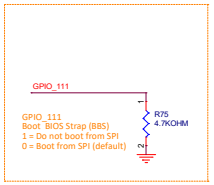


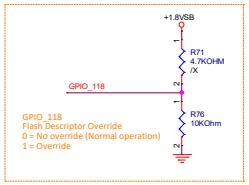


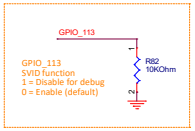


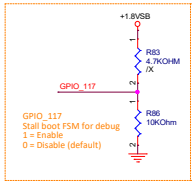


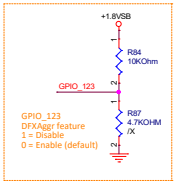


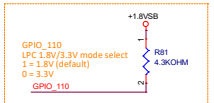


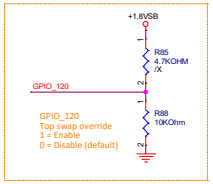


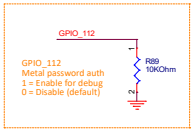












ASUSTek COMPUTER INC.

Title : SOC-8(SVID/SMBUS/USB2/I2C)

Engineer: Ben Lien

Size	Project Name	Rev
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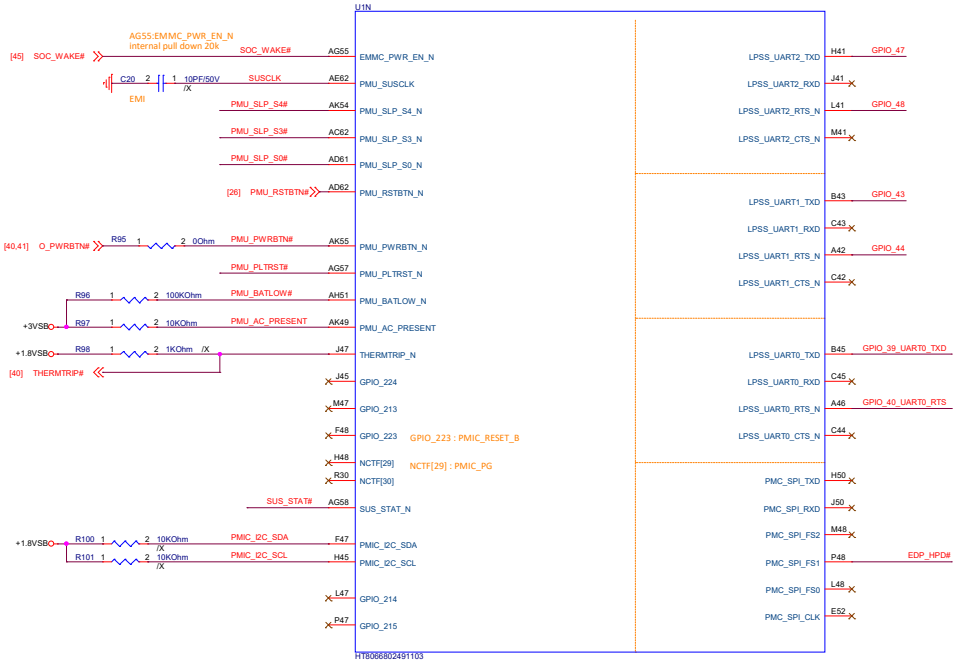
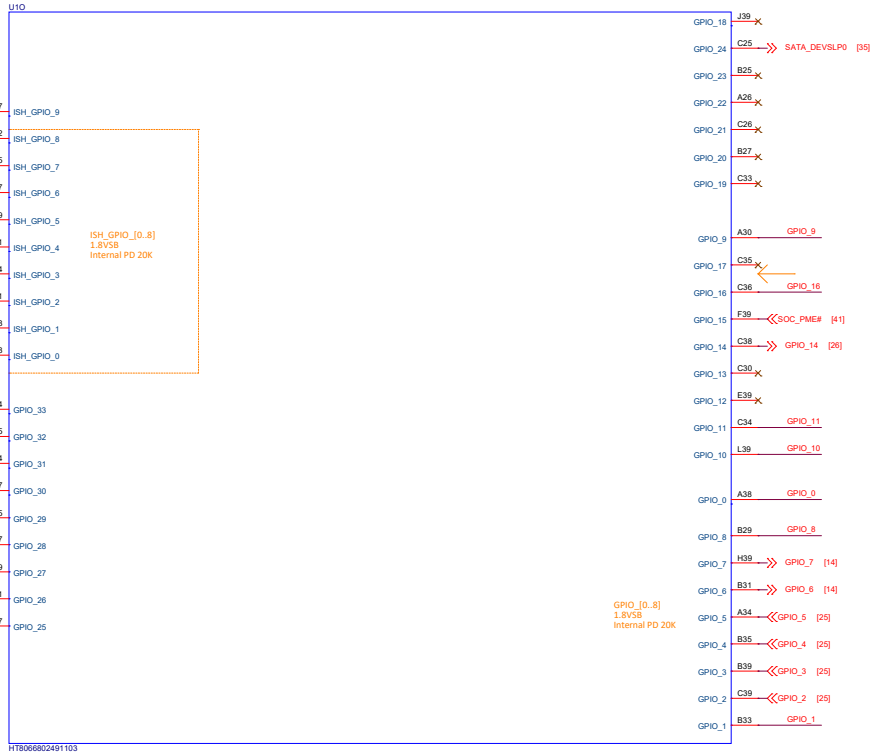
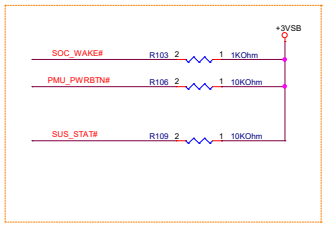
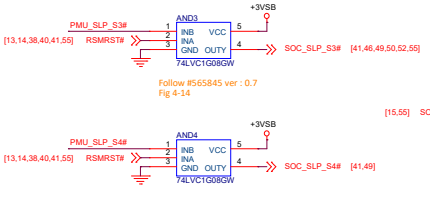
CORE - SOC - PMU/UART

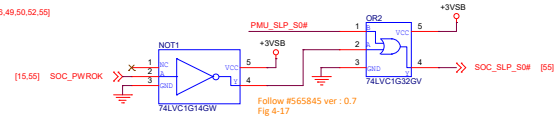


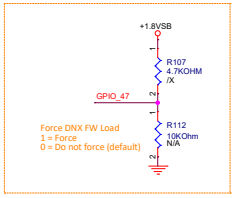
CORE - SOC - GPIO/ISH

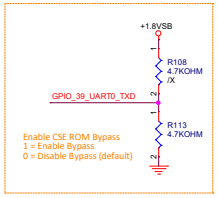


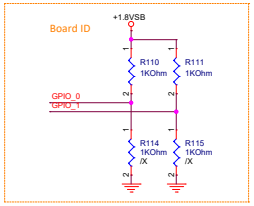


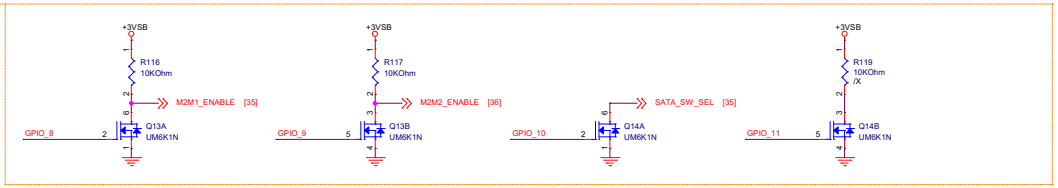


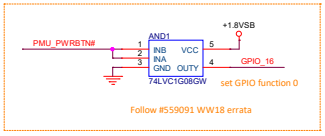


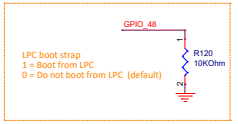


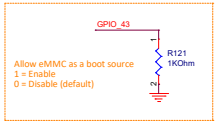


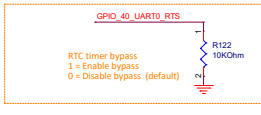


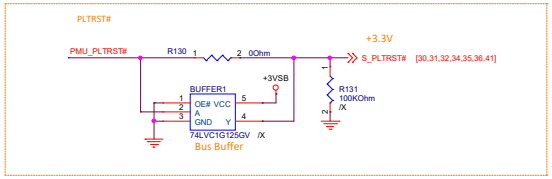


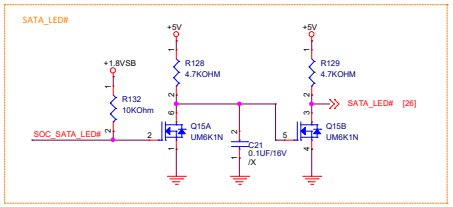


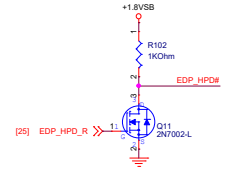


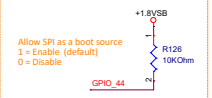


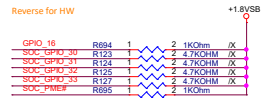












ASUSTeK COMPUTER INC.	Title :	SOC-9(UART/GPIO)
	Engineer:	Ben Lien
Size: Custom	Project Name: EMB-APL2	Rev: 1.00
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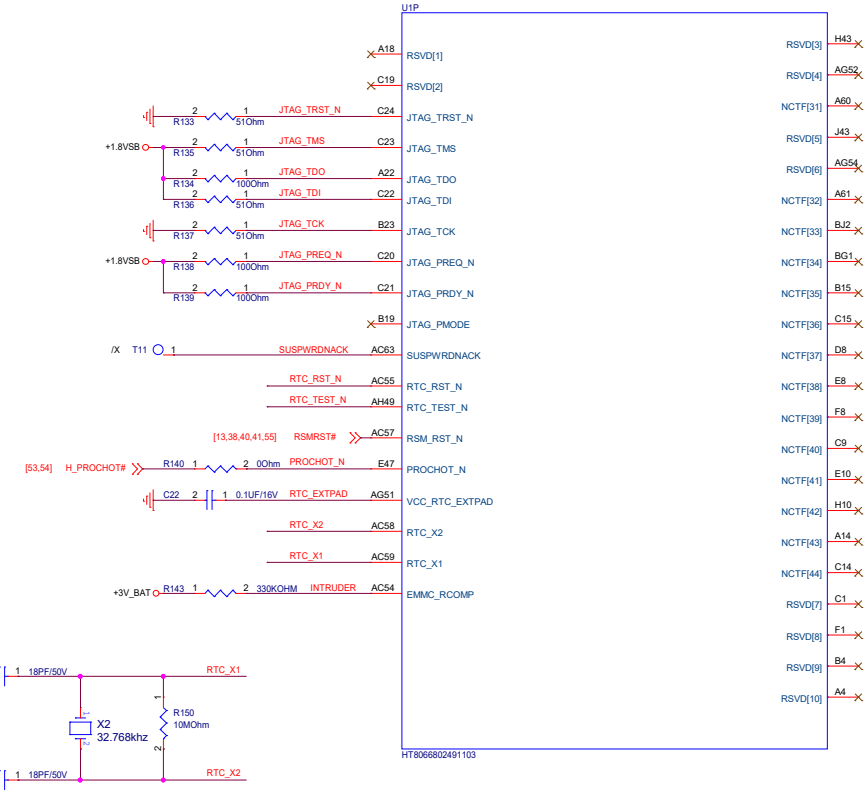
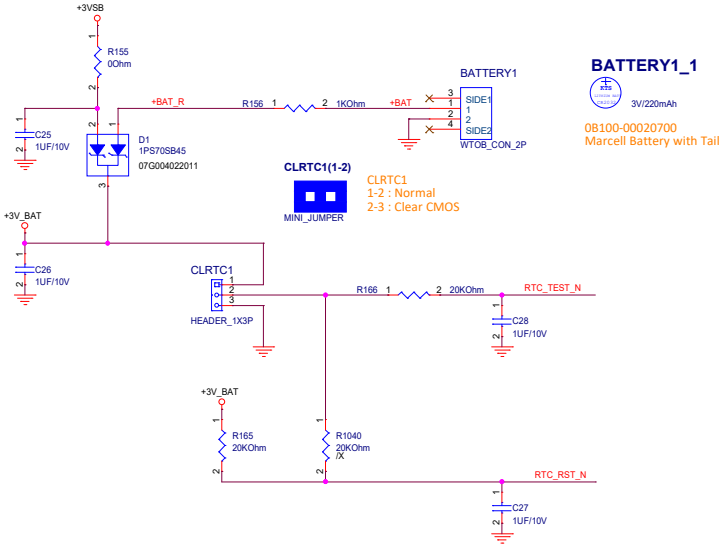
CORE - SOC - JTAG/OBS/THERMAL



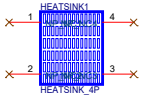


CLRTC1(1-2)

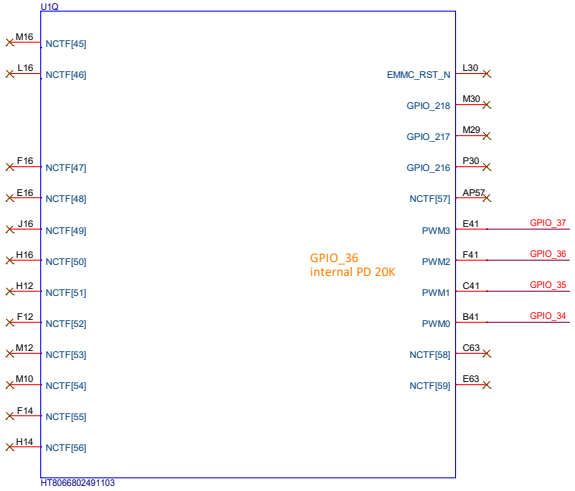
CLRTC1
1-2 : Normal
2-3 : Clear CMOS

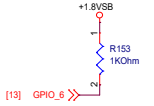
BATTERY1_1

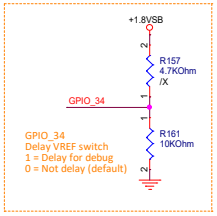
0B100-00020700
Marcell Battery with Tail

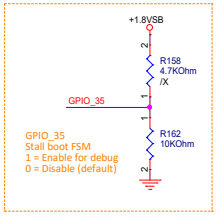


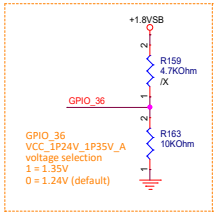
CORE - SOC - CNV, PWM

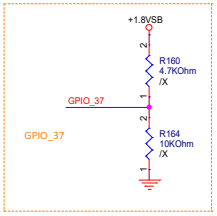




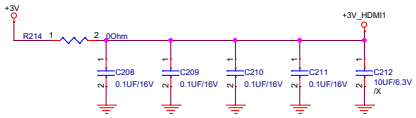


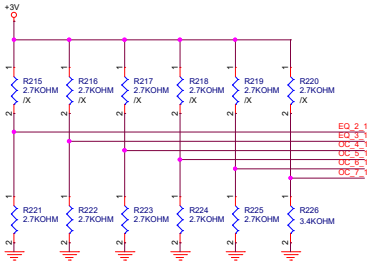






ASUSTek COMPUTER INC.	Title : SOC-10(JTAG)	
	Engineer: Ben Lien	
Size: C	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 14 of 57	



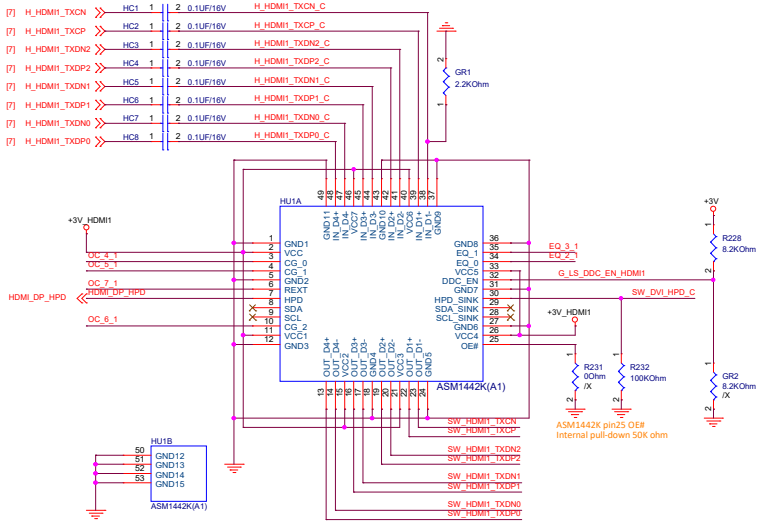


ASM1442K EQ_[1:0]
Integrate internal pull-up resistor.

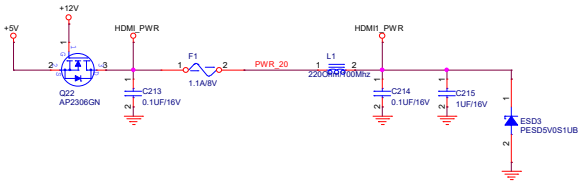
ASM1442K CG_[2:0]
Integrate internal pull-up resistor.

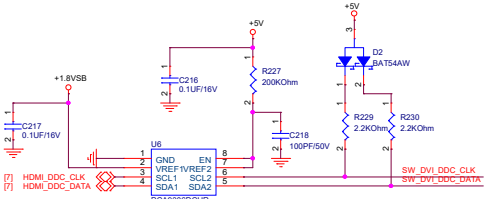
EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

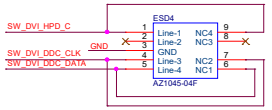
CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	1	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		

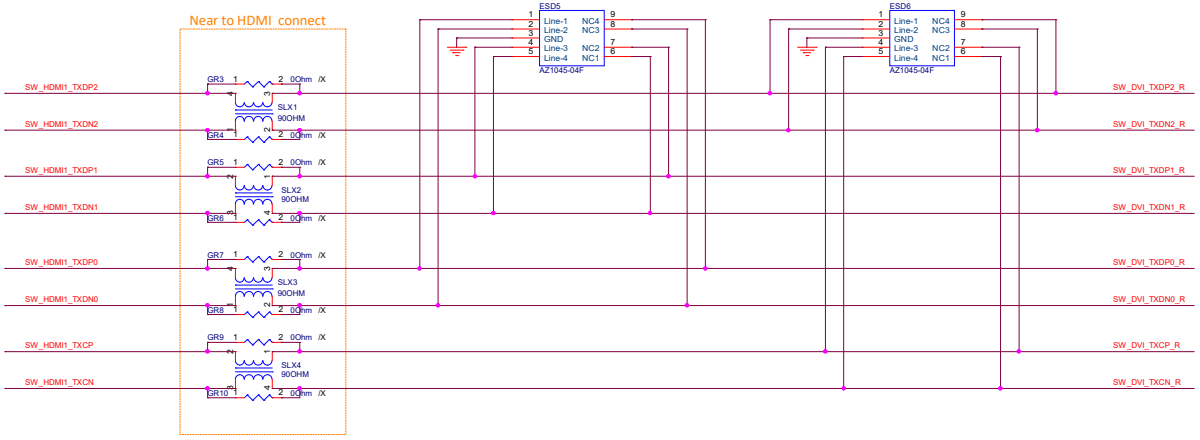


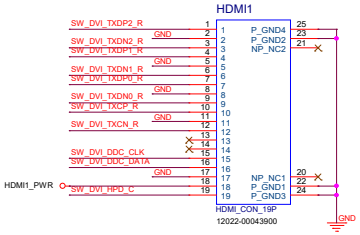
Level Shifter











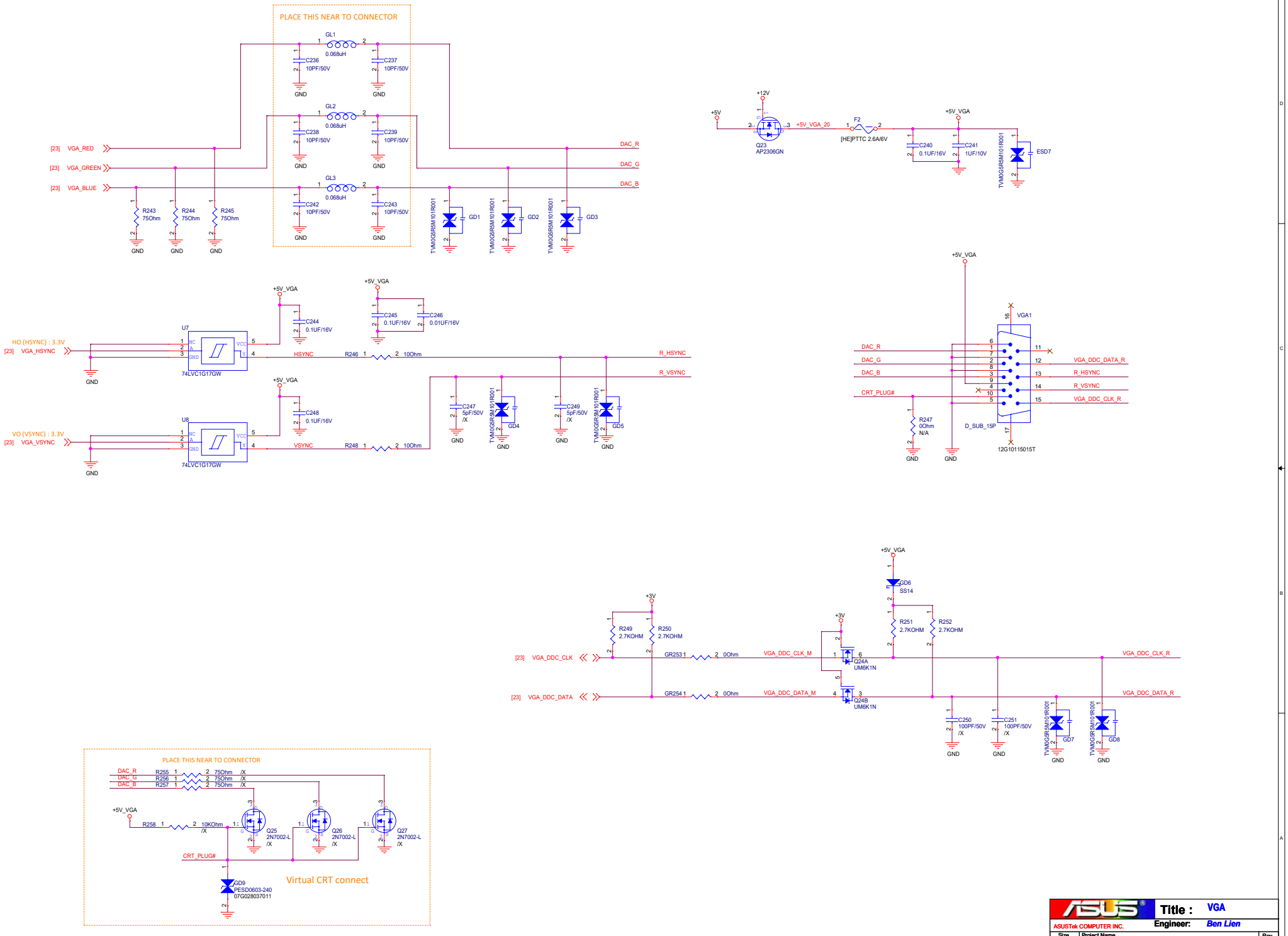
ASUSTek COMPUTER INC.

Title : DDI0(HDMI)

Engineer: Ben Lien

Size	Project Name	Rev
Custom	EMB-APL2	1.00

Date: Monday, November 04, 2019 Sheet 22 of 57



ASUSTek COMPUTER INC.	Title : VGA	
	Engineer: Ben Lien	
Size: C	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 24 of 57	

LCD panel Voltage SEL

LVDS_PWR	Panel Voltage Select
1-2	5V
(Default) 2-3	3V

INVERTER

BKL_PWR	INV Voltage Select
1-2	12V
(Default) 2-3	5V

INV CTL SEL

J3	DC & PWM SEL
(Default) 1-2	DC Control
2-3	PWM Control

Co-layout
Pad overlap

LVDS resolution
(reserve setting by HW)

Default eDP1

PS8625
3.3V : 119 mA
2.5V : 131 mA

LVDS_ENAVDD/I2C_ADDR
(IPD : 80K)
Low : 0x10 ~ 0x1FH
High : 0x90 ~ 0x9FH

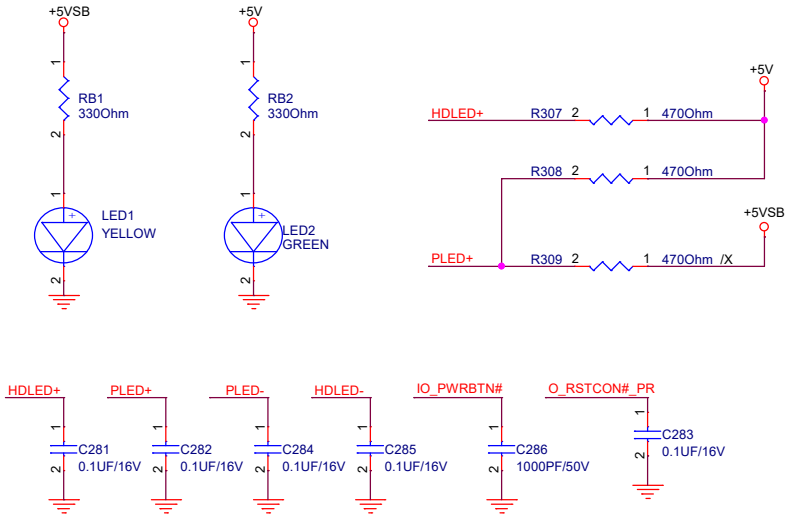
RLV_CFG
(IPD : 80K)
Low : 8-bit LVDS, VESA mapping
Mid : 8-bit LVDS, JEIDA mapping
High : 6-bit LVDS, both VESA & JEIDA mapping

RLV_LINK
(IPD : 80K)
Low : Single Link LVDS
High : Dual Link LVDS

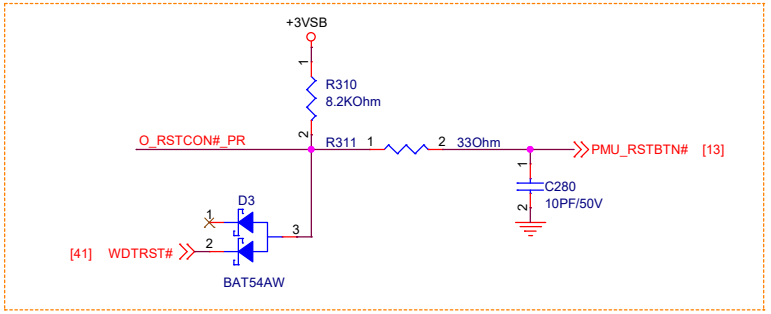
Initial Code EEPROM

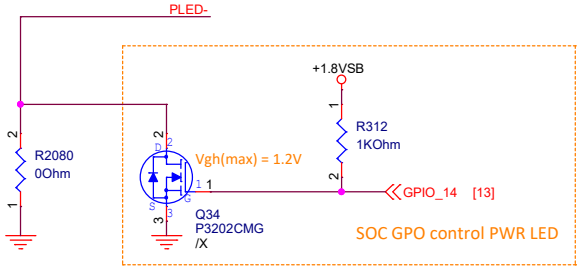
Adjust LVDS brightness/DC control

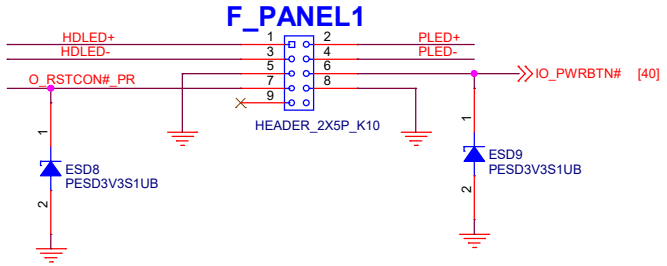
Title :	eDP(LVDS & eDP)
ASUSTeK COMPUTER INC.	Engineer: Ben Lian
Size: Custom	Project Name: EMB-APL2
Rev: 1.00	
Date: Monday, November 04, 2019	Sheet 25 of 57

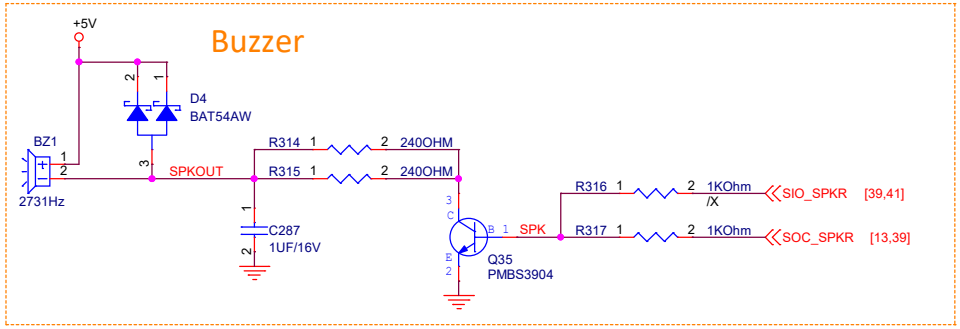


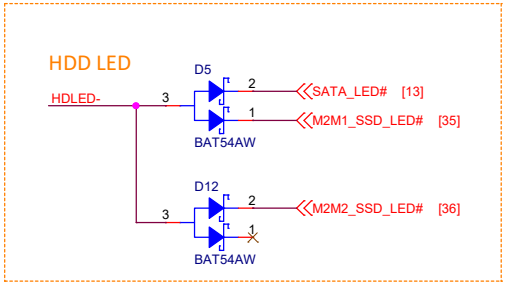
PLACE NEAR PANEL or FPANEL



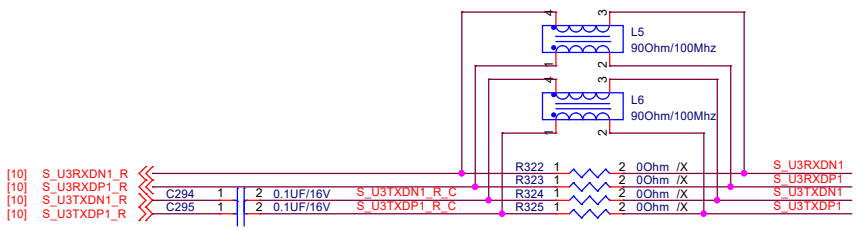


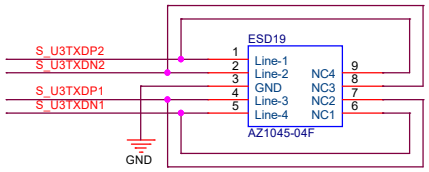


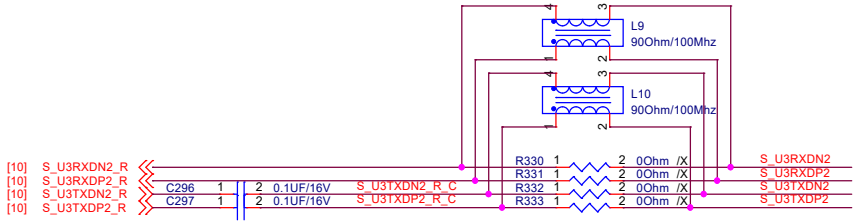


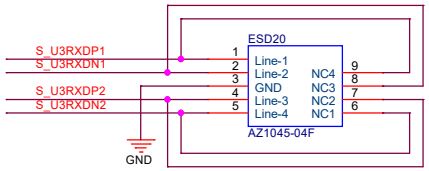


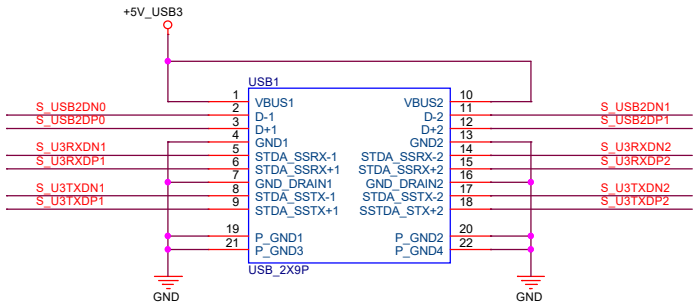
ASUSTek COMPUTER INC.	Title : Front panel	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 26 of 57	

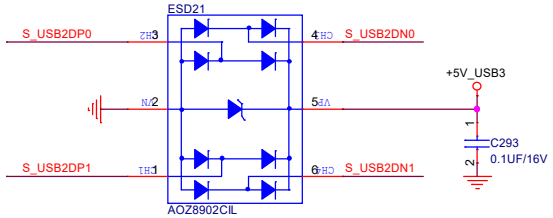


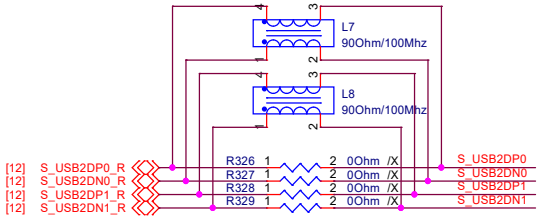


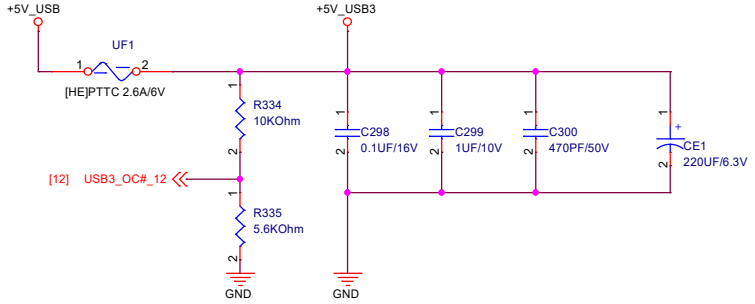




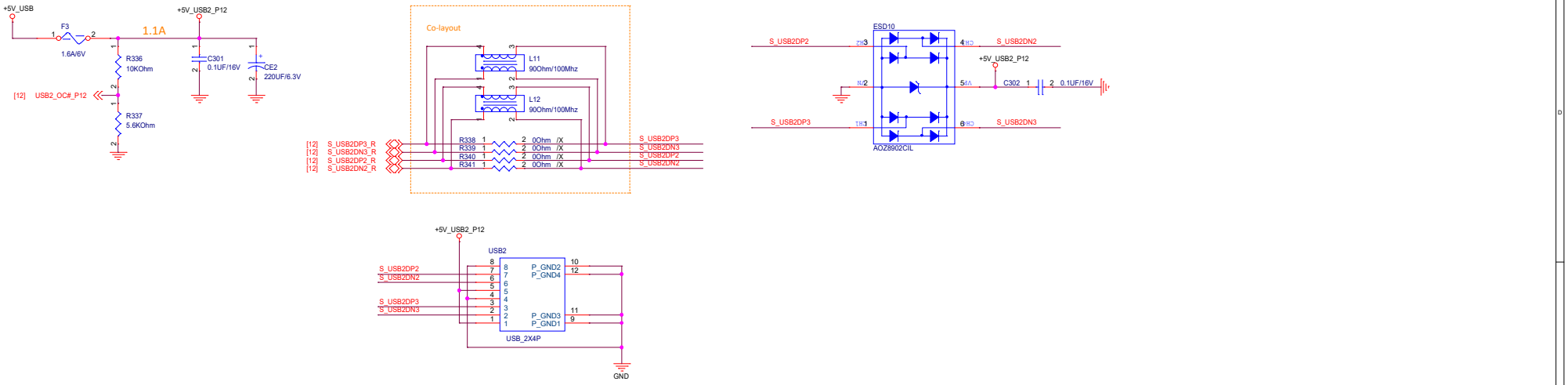


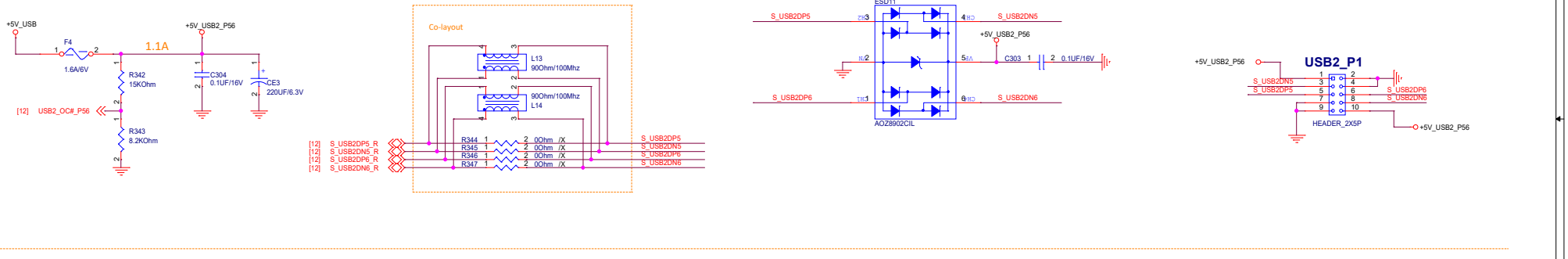


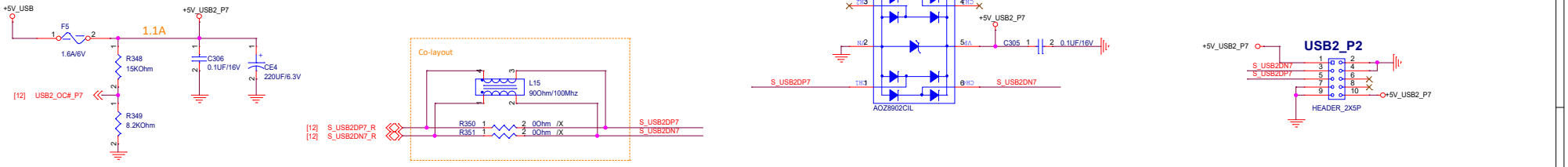




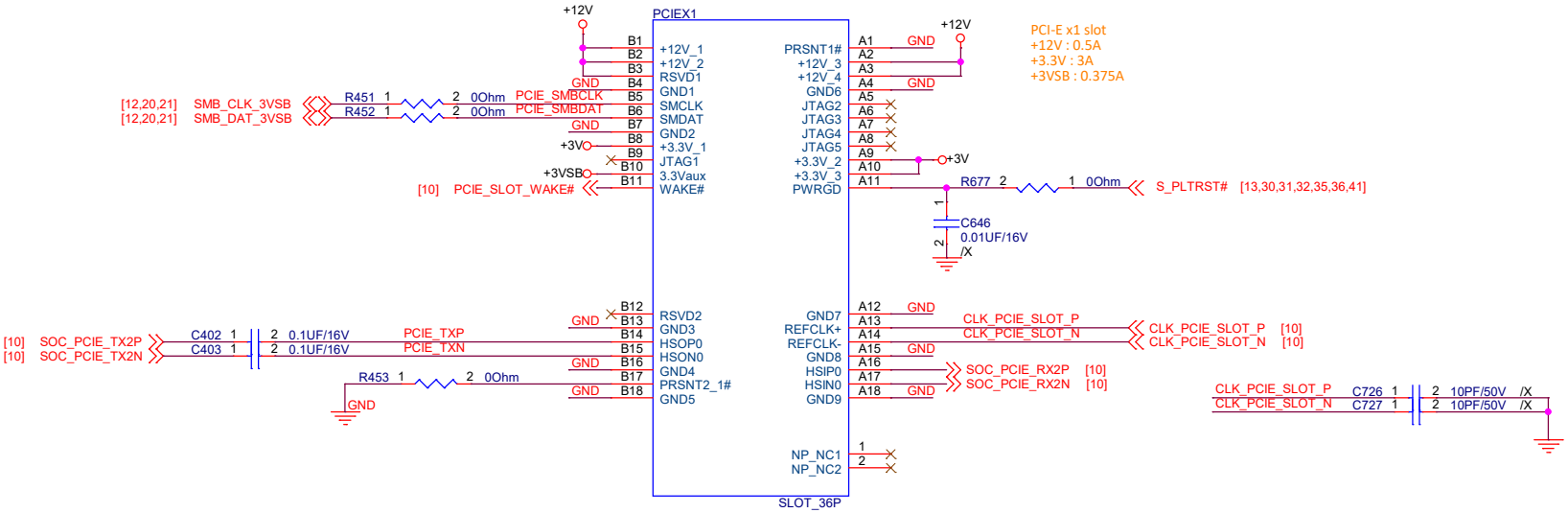
ASUSTek COMPUTER INC.	Title : USB3.0 x2	
	Engineer: Ben Lien	
Size: A3	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 28 of 57	

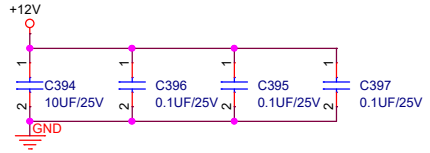


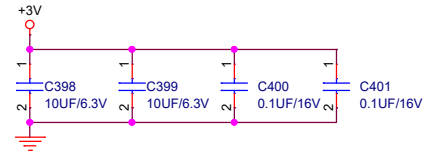


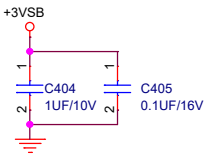


ASUSTek COMPUTER INC.	Title : USB2.0 x2	
	Engineer: Ben Lien	
Size: C	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 29 of 57	

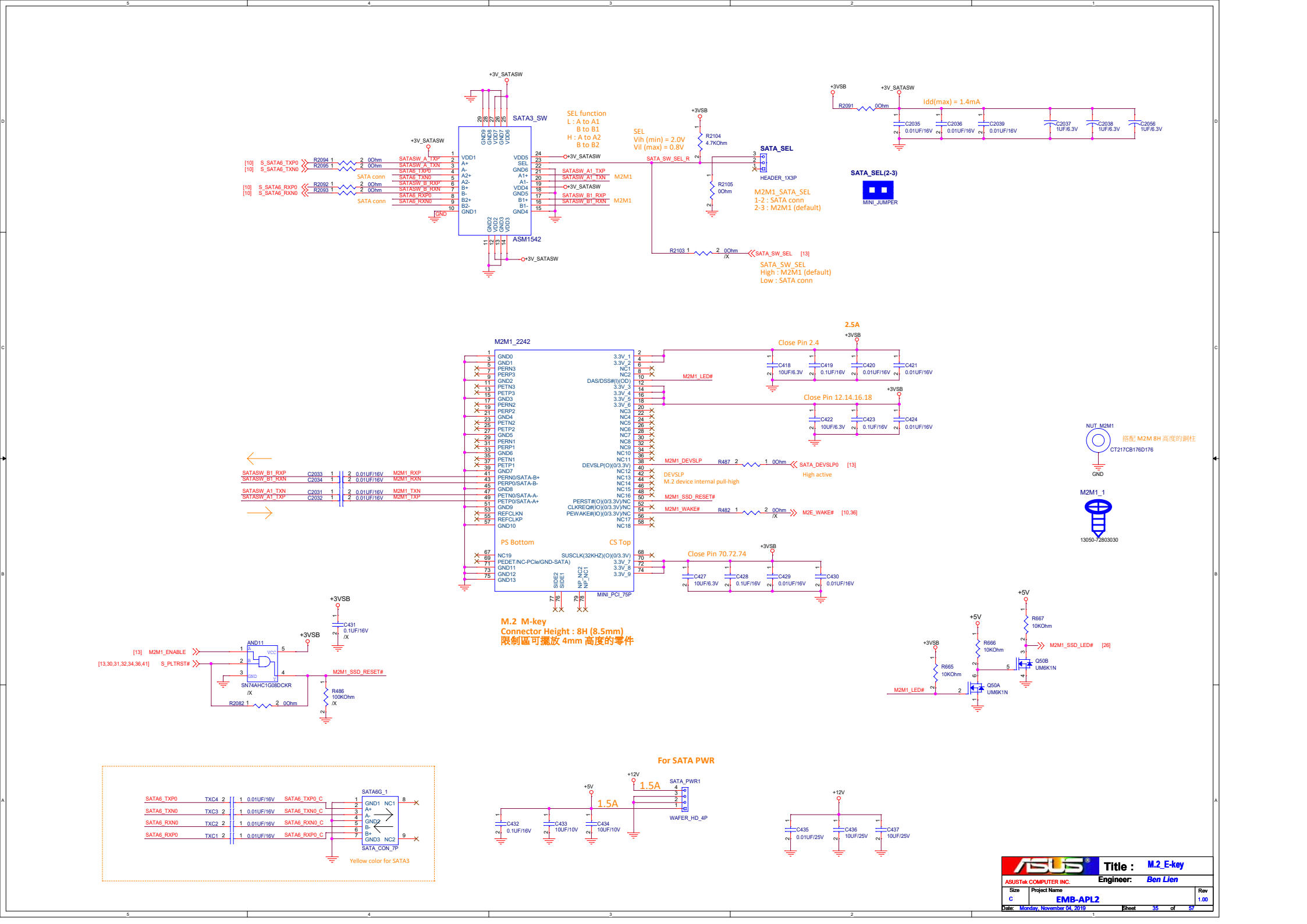




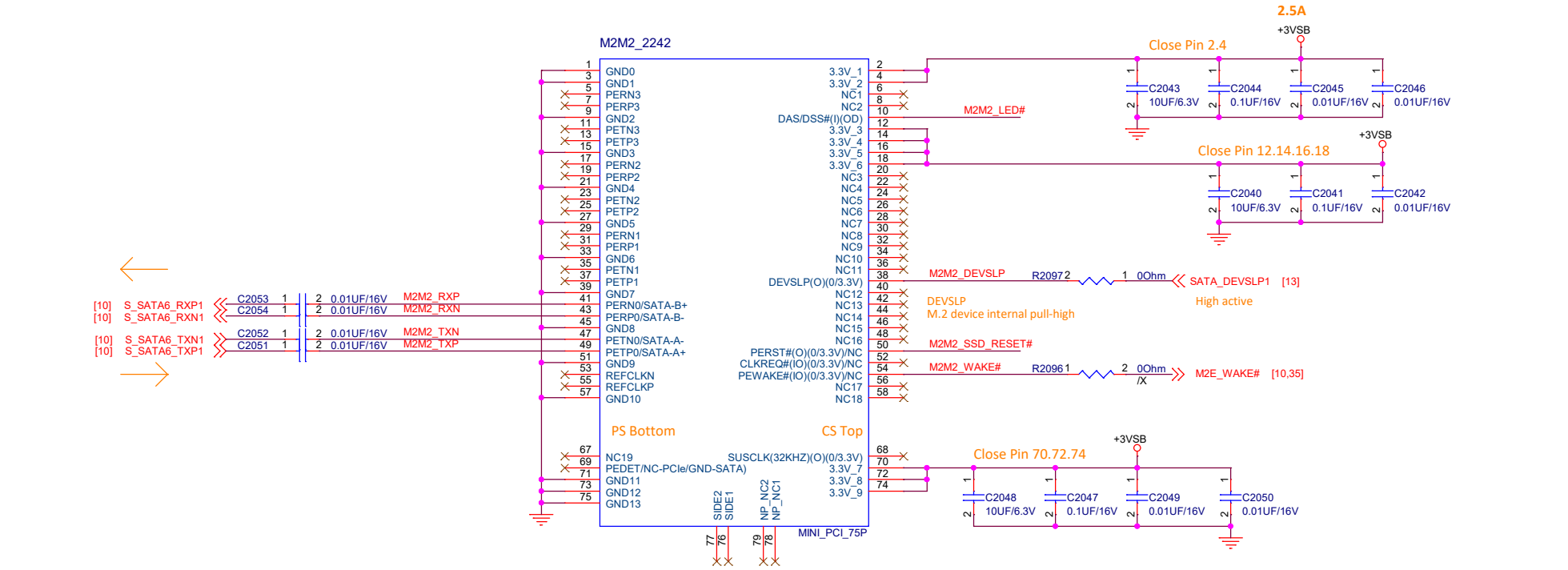


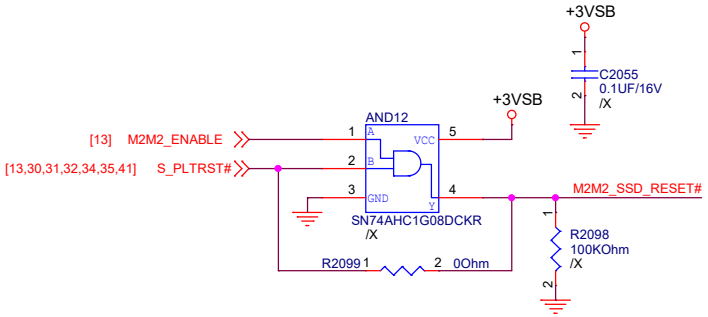


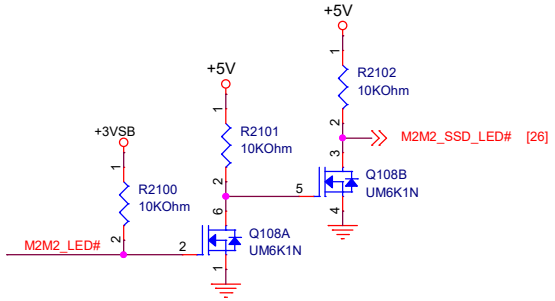
ASUSTek COMPUTER INC.	Title : PCI-E x1 slot	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 34 of 57	

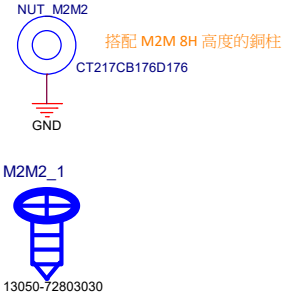


ASUSTek COMPUTER INC.	Title :	M.2_E-key	
	Engineer:	Ben Lien	
Size: C	Project Name: EMB-APL2		Rev: 1.00
Date: Monday, November 04, 2019	Sheet 35 of 57		









ASUSTek COMPUTER INC.	Title : M.2_M-key	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
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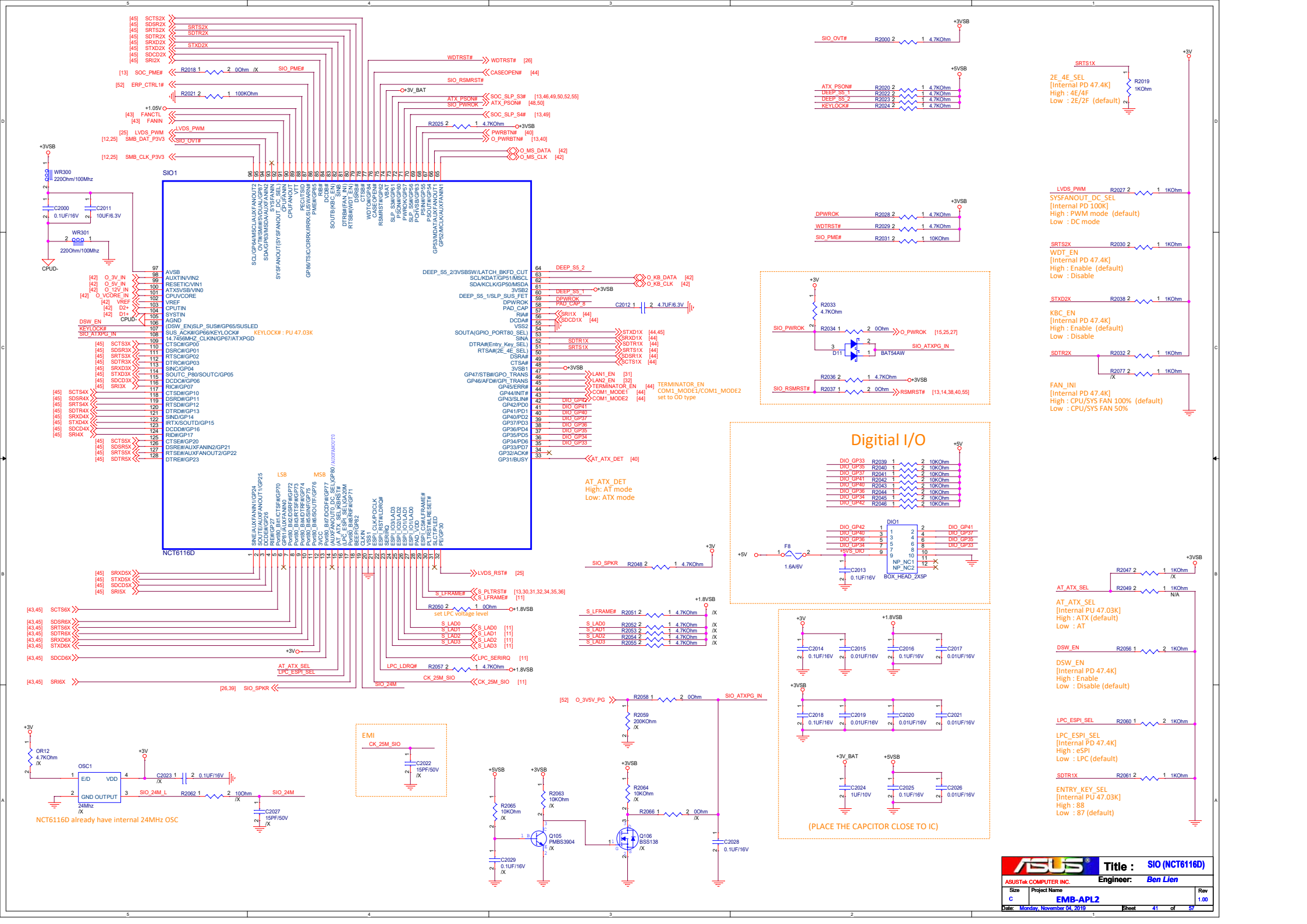
SIO1
NCT6116D
Digitial I/O
DIO1
BOX_HEAD_2X5P
BAT54AW
Q105 PMBS3904
Q106 BSS138
OSC1
24Mhz
NCT6116D already have internal 24MHz OSC
EMI
(PLACE THE CAPCITOR CLOSE TO IC)
2E_4E_SEL
[Internal PD 47.4K]
High : 4E/4F
Low : 2E/2F (default)
SYSFANOUT_DC_SEL
[Internal PD 100K]
High : PWM mode (default)
Low : DC mode
WDT_EN
[Internal PD 47.4K]
High : Enable (default)
Low : Disable
KBC_EN
[Internal PD 47.4K]
High : Enable (default)
Low : Disable
FAN_INI
[Internal PD 47.4K]
High : CPU/SYS FAN 100% (default)
Low : CPU/SYS FAN 50%
AT_ATX_SEL
[Internal PU 47.03K]
High : ATX (default)
Low : AT
DSW_EN
[Internal PD 47.4K]
High : Enable
Low : Disable (default)
LPC_ESPI_SEL
[Internal PD 47.4K]
High : eSPI
Low : LPC (default)
ENTRY_KEY_SEL
[Internal PU 47.03K]
High : 88
Low : 87 (default)
KEYLOCK# : PU 47.03K
AT_ATX_DET
High: AT mode
Low: ATX mode
TERMINATOR_EN
COM1_MODE1/COM1_MODE2
set to OD type
set LPC voltage level
ASUSTek COMPUTER INC.
Title : SIO (NCT6116D)
Engineer: Ben Lien
Size C
Project Name EMB-APL2
Rev 1.00
Date: Monday, November 04, 2019
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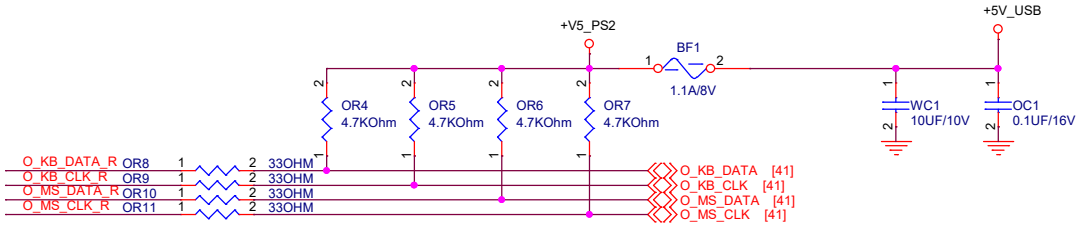
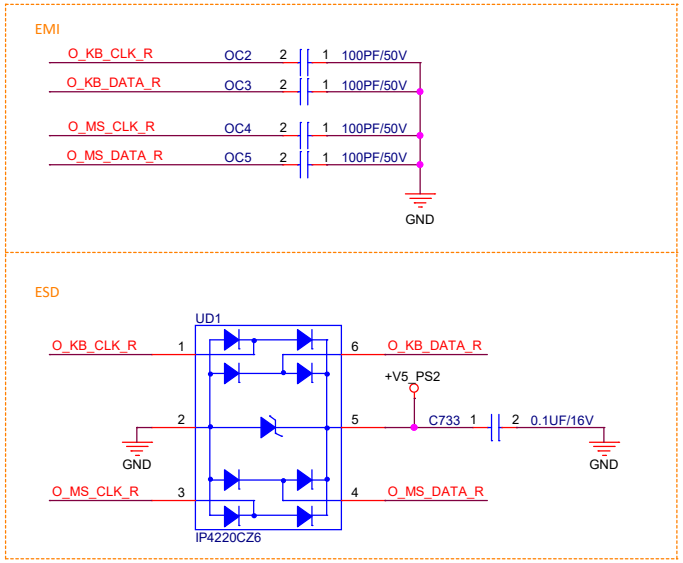
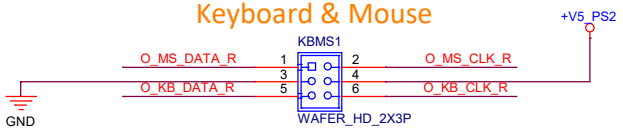
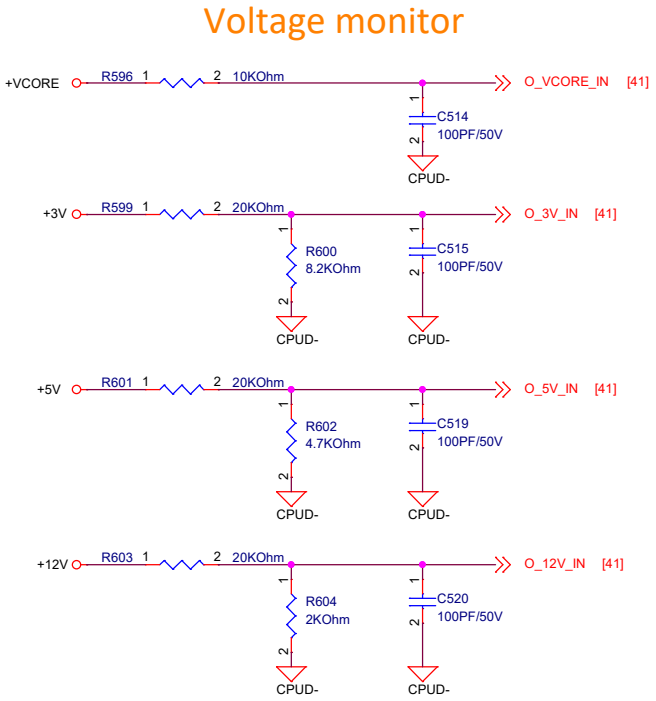
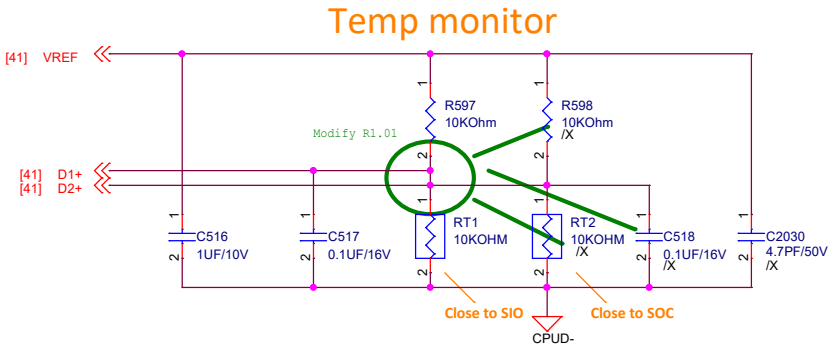


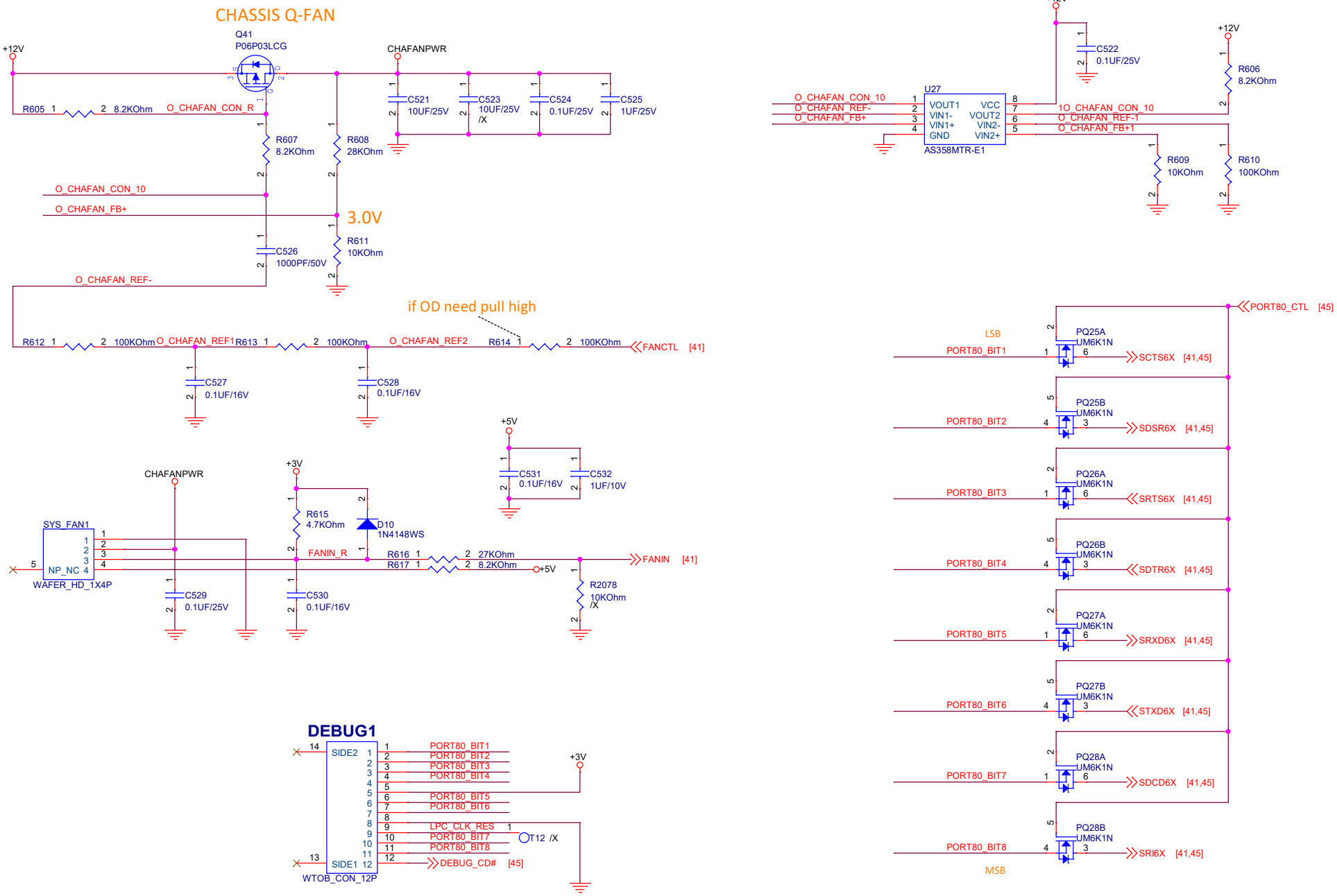






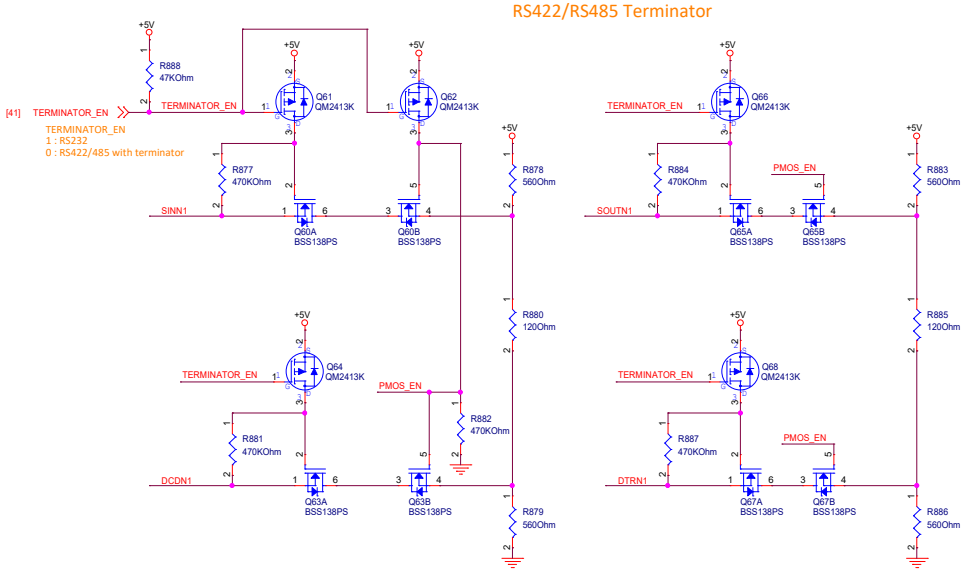


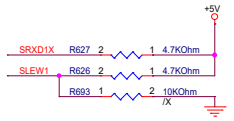
ASUSTek COMPUTER INC.	Title : HW monitor /PS2	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 42 of 57	

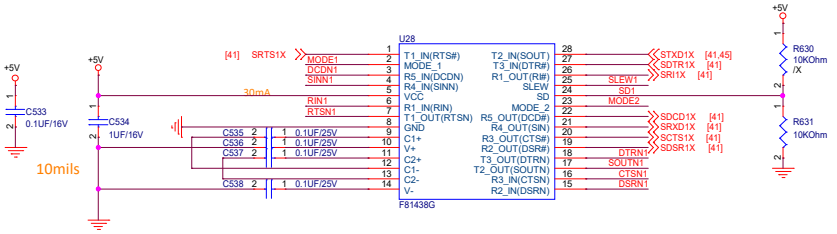


ASUSTek COMPUTER INC.	Title :	FAN
	Engineer:	Ben Lien
Size: Custom	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 43 of 57	

RS422/RS485 Terminator



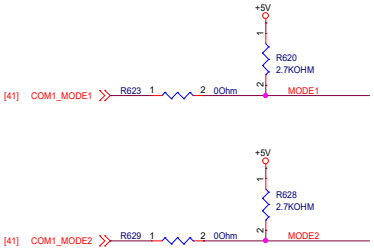




Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

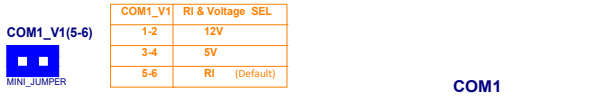
Note:

Mode_1 and Mode_2 pin. Internal pull high ≒ 625KΩ. As the current is very small (≒ 15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.

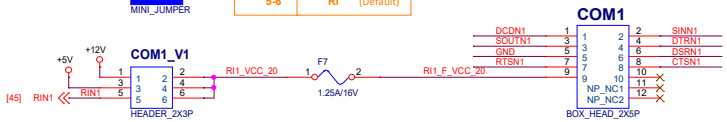


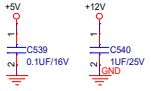
RS-232/485/422 Pin Assignment			
Pin	RS-232	RS-485	RS-422
1	DCD	RS485_D-	RS422_TX-
2	DSR		
3	RX	RS485_D+	RS422_TX+
4	RTS		
5	TX		RS422_RX+
6	CTS		
7	DTR		RS422_RX-
8	RI		

Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

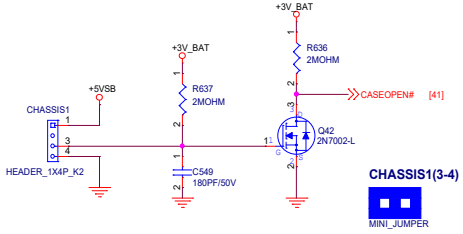


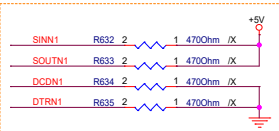
COM1_V1	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)





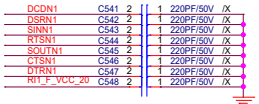
CASEOPEN





Note:Reserved for FAIL-SAVE

EMI



ASUSTek COMPUTER INC.

Title : COM1(RS232/422/485)

Engineer: Ben Lien

Size	Project Name	Rev
C	EMB-APL2	1.00

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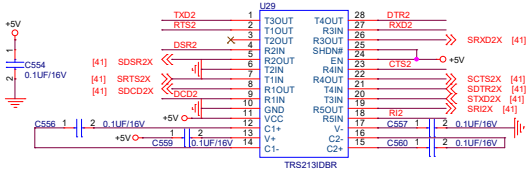
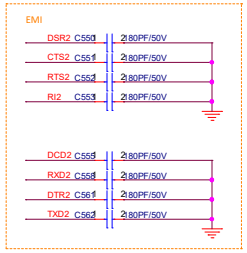
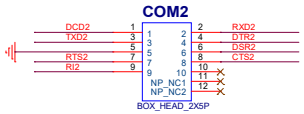
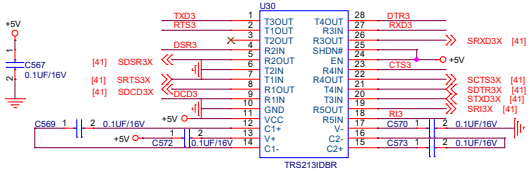
COM2

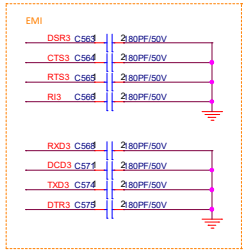


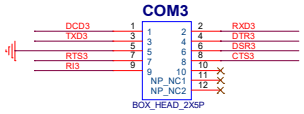




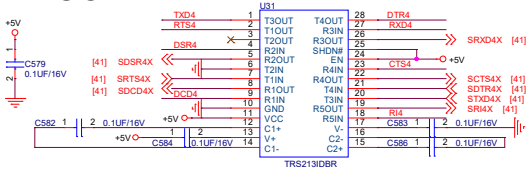
COM3

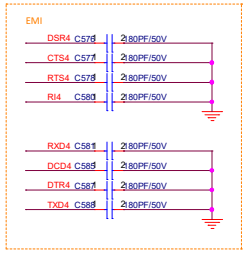


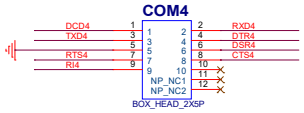




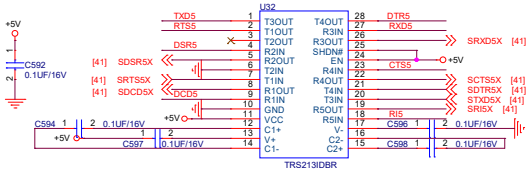
COM4

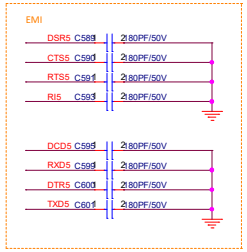


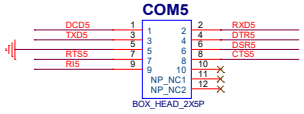




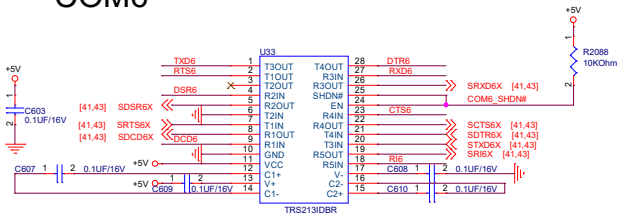
COM5

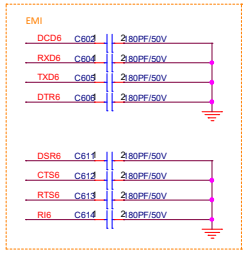


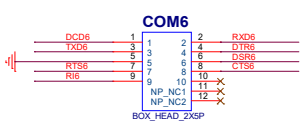




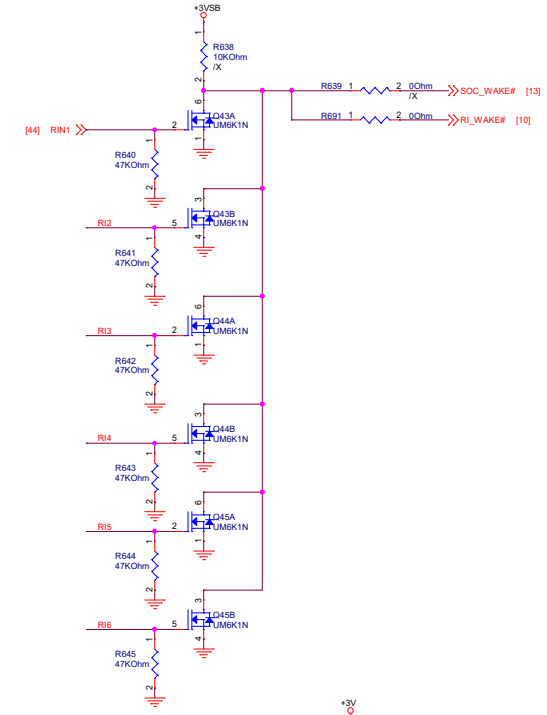
COM6

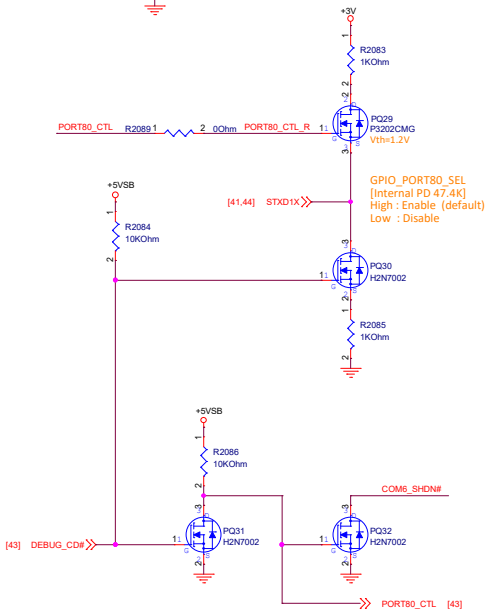




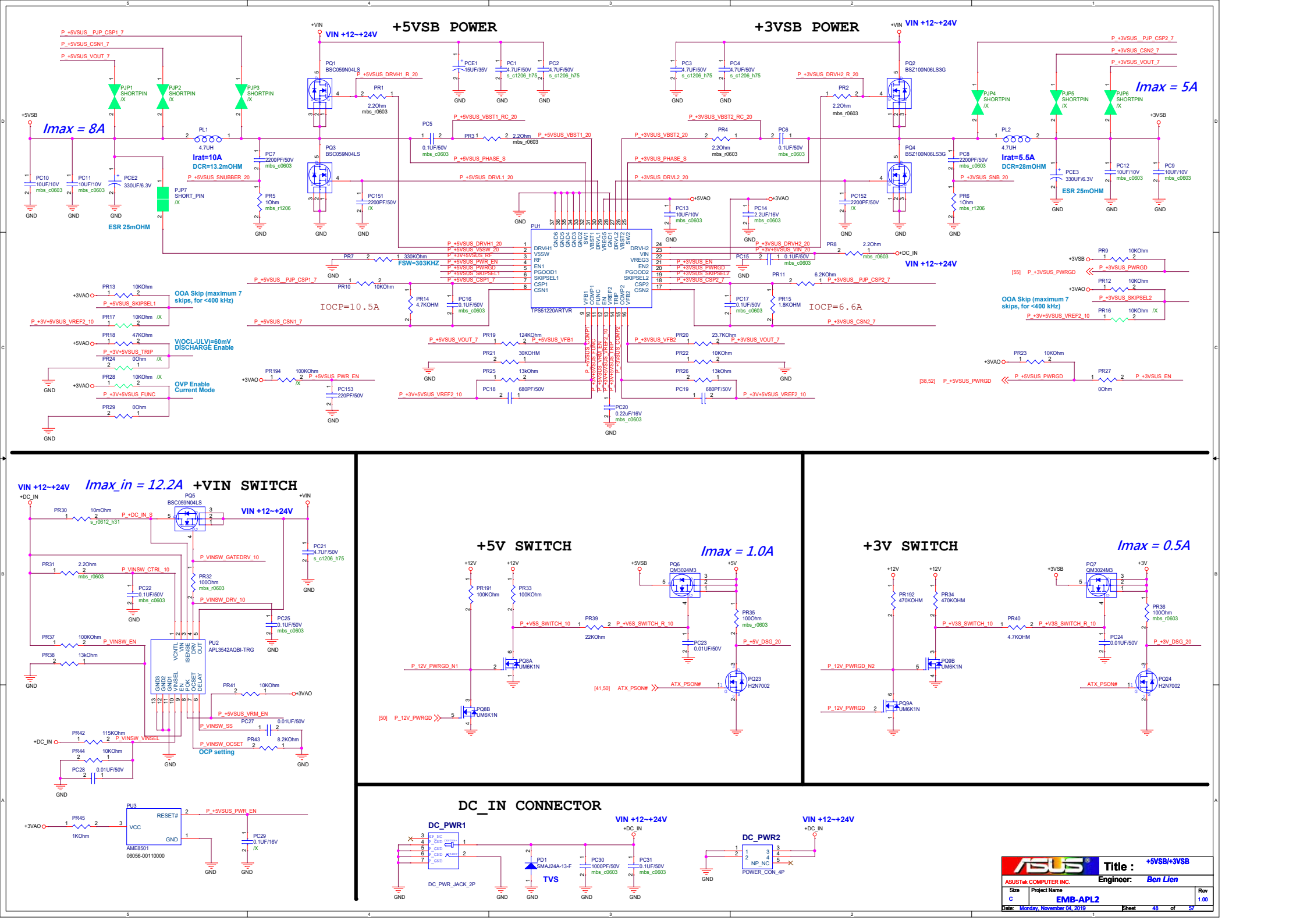


Wake on MODEM





ASUSTek COMPUTER INC.	Title :	COM2 to 6	
	Engineer:	Ben Lien	
Size: Custom	Project Name: EMB-APL2		Rev: 1.00
Date: Monday, November 04, 2019	Sheet 45 of 57		


+5VSB POWER
+3VSB POWER
VIN +12~+24V
Imax = 8A
Imax = 5A
Irat=10A
DCR=13.2mOHM
Irat=5.5A
DCR=28mOHM
ESR 25mOHM
FSW=303KHZ
TPS51220ARTVR
IOCP=10.5A
IOCP=6.6A
OOA Skip (maximum 7 skips, for <400 kHz)
V(OCL-ULV)=60mV DISCHARGE Enable
OVP Enable Current Mode
Imax_in = 12.2A
+VIN SWITCH
APL3542AQBI-TRG
OCP setting
+5V SWITCH
Imax = 1.0A
+3V SWITCH
Imax = 0.5A
DC_IN CONNECTOR
DC_PWR1
DC_PWR_JACK_2P
TVS
DC_PWR2
POWER_CON_4P
Title : +5VSB/+3VSB
Engineer: Ben Lien
ASUSTek COMPUTER INC.
Project Name EMB-APL2
Size C
Rev 1.00
Date: Monday, November 04, 2019
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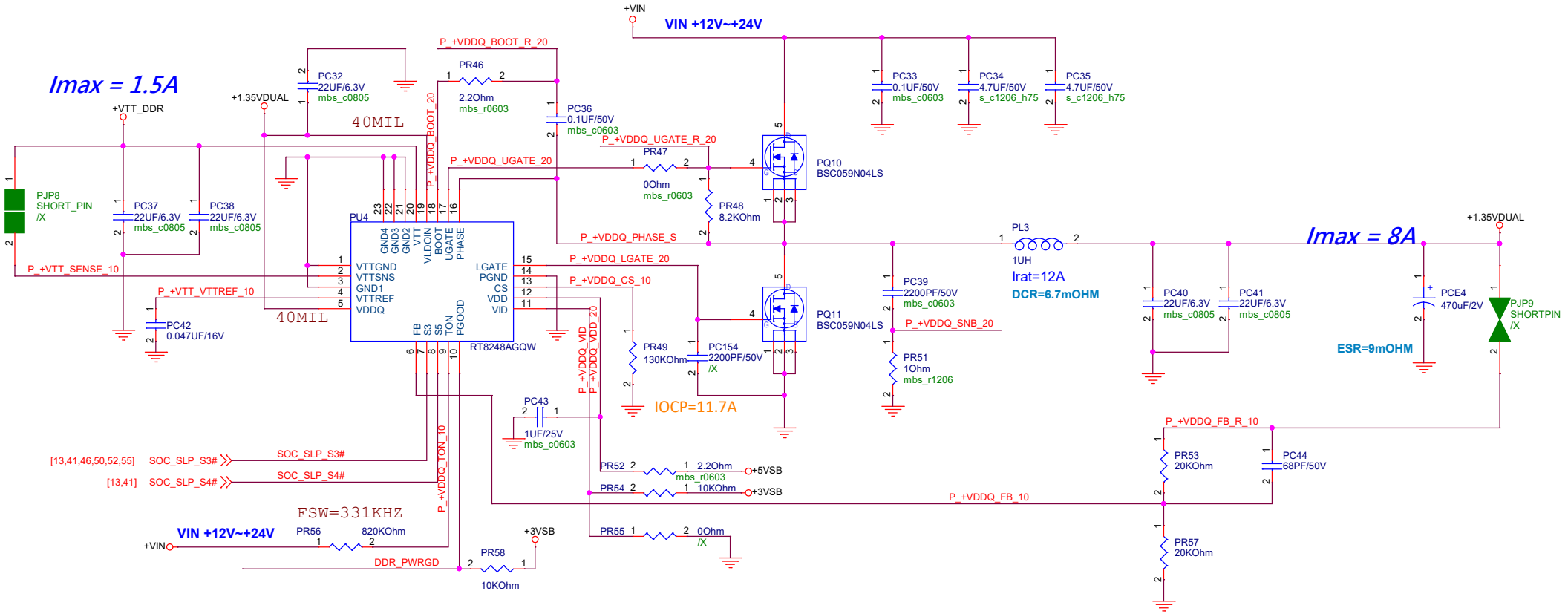

Only main power

S3 And S5 Truth Table

State	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Low	Hi	On
S4/S5	Low	Low	Off (Discharge)

VOUT Select Table

P_+VDDQ_VID	VOUT
Low	+1.5V
Hi	+1.35V

State	VTTREF	VTT
S0	On	On
S3	On	Off(Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)

<Variant Name>

Title : +1.35VDUAL

ASUSTeK COMPUTER INC.

Engineer:

Size	Project Name	Rev
B	EMB-APL2	1.00

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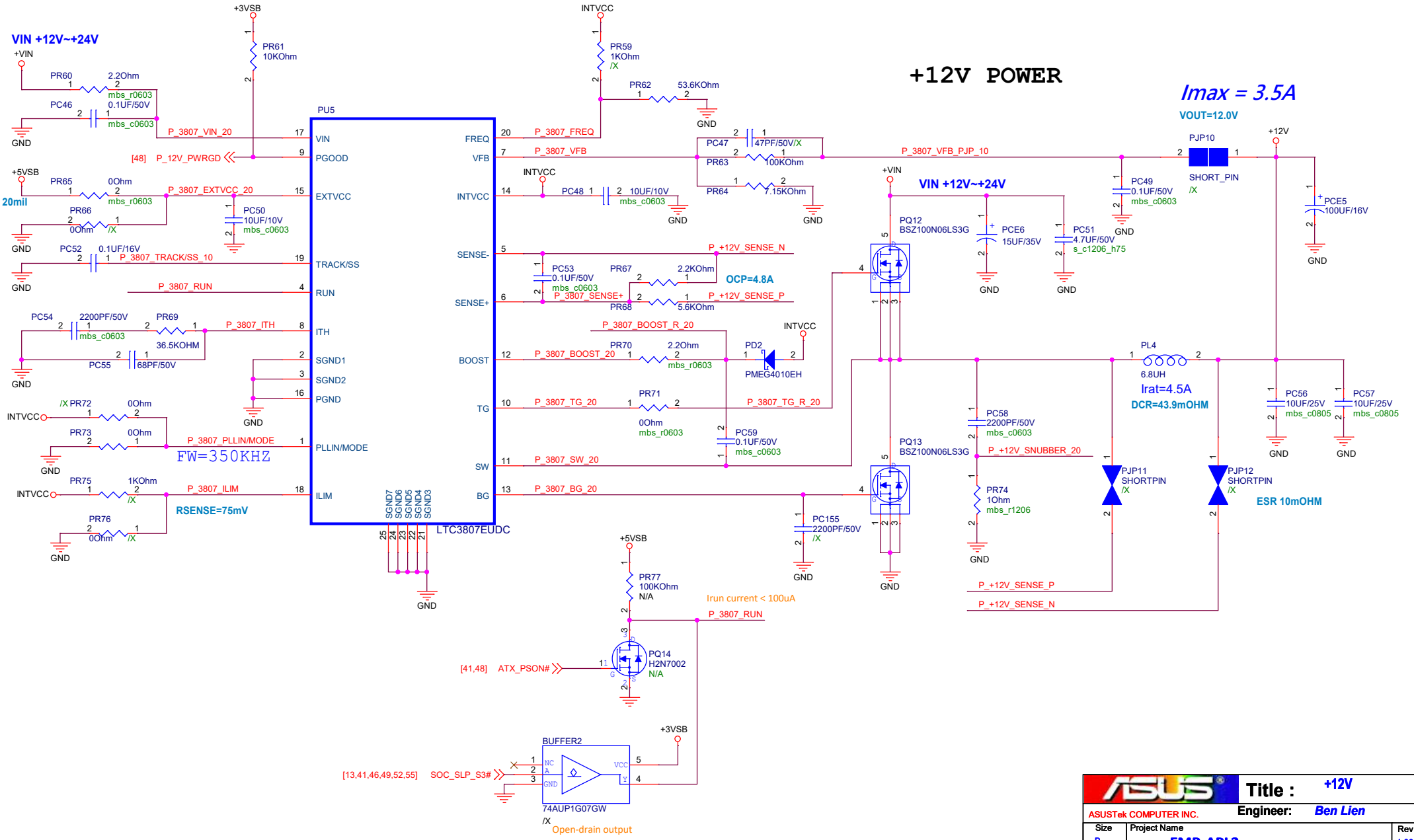
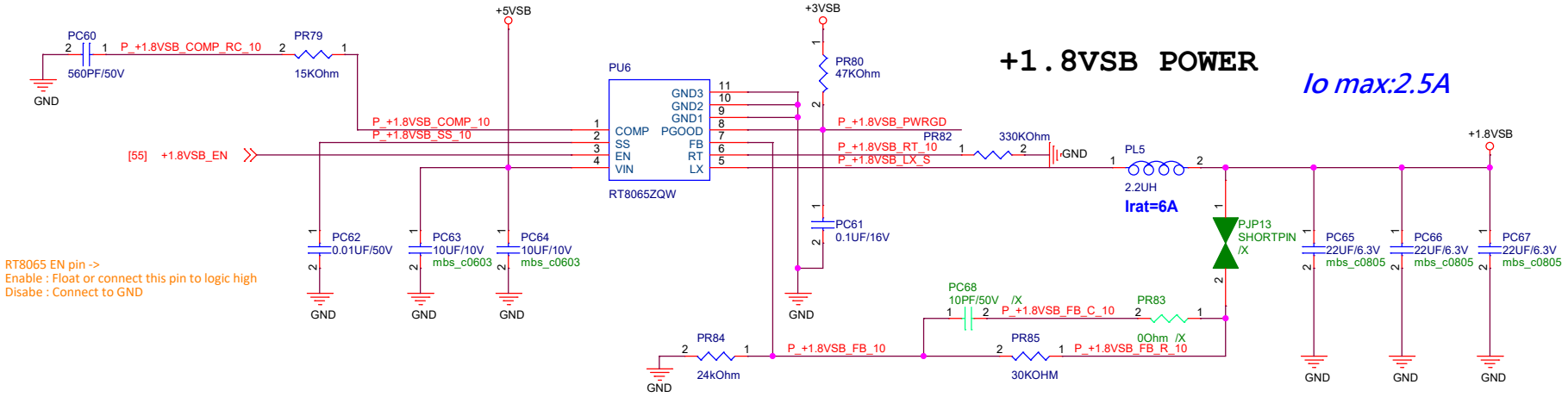
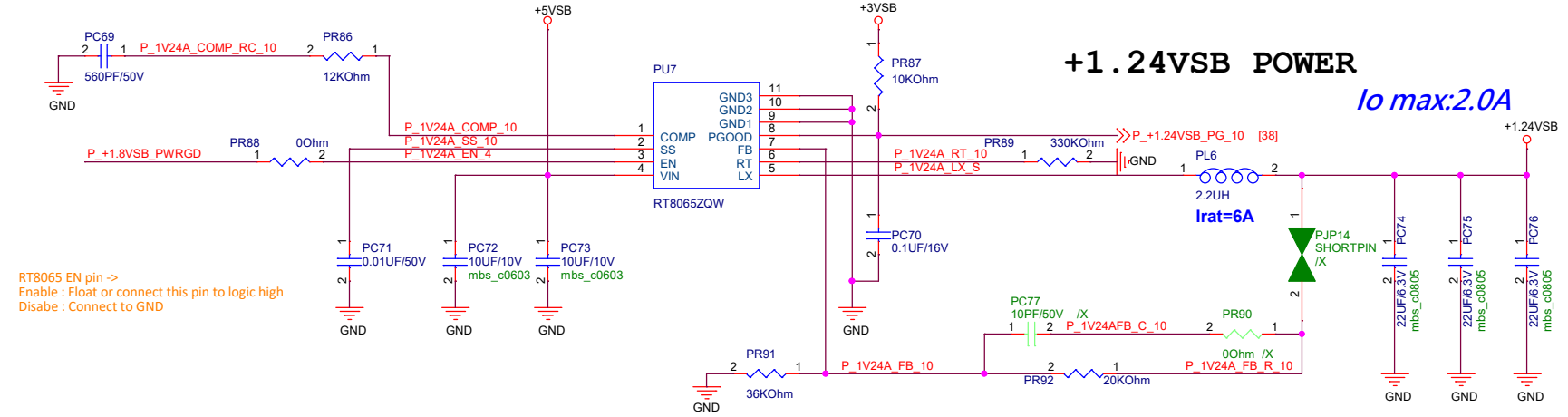
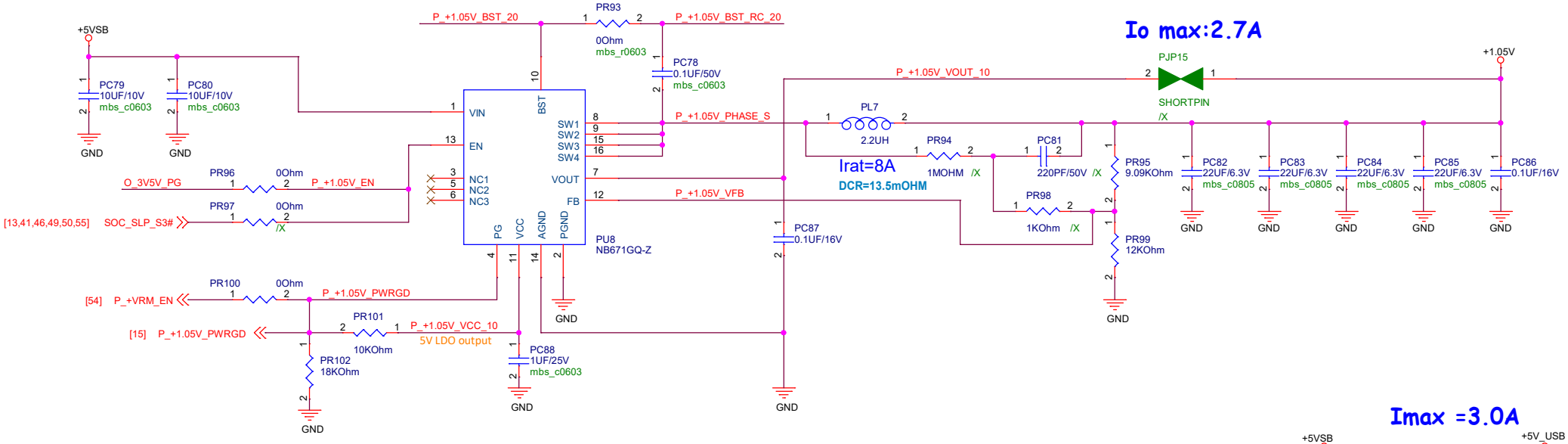


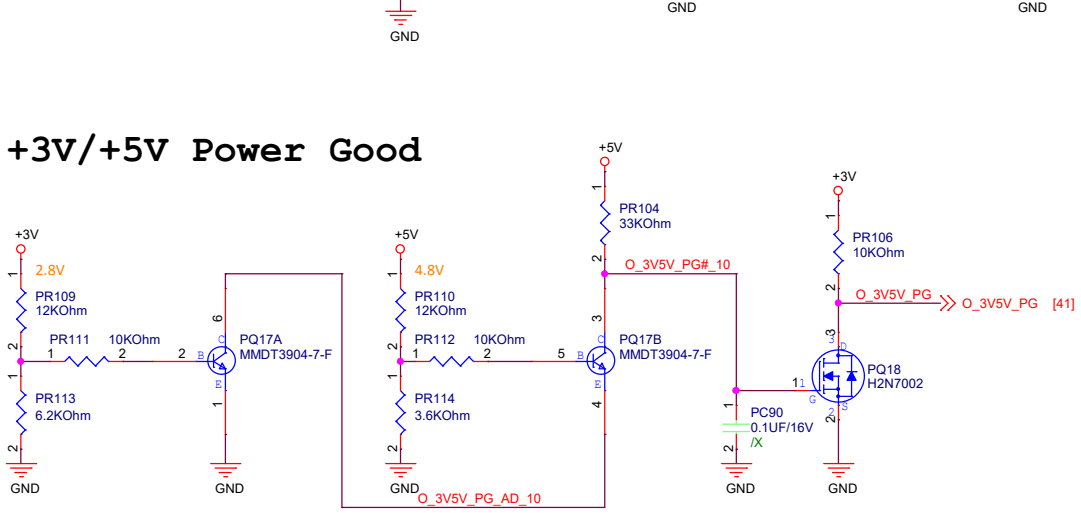
ASUSTek COMPUTER INC.	Title : +12V		
	Engineer: Ben Lien		
Size: B	Project Name: EMB-APL2		Rev: 1.00
Date: Monday, November 04, 2019	Sheet 50 of 57		

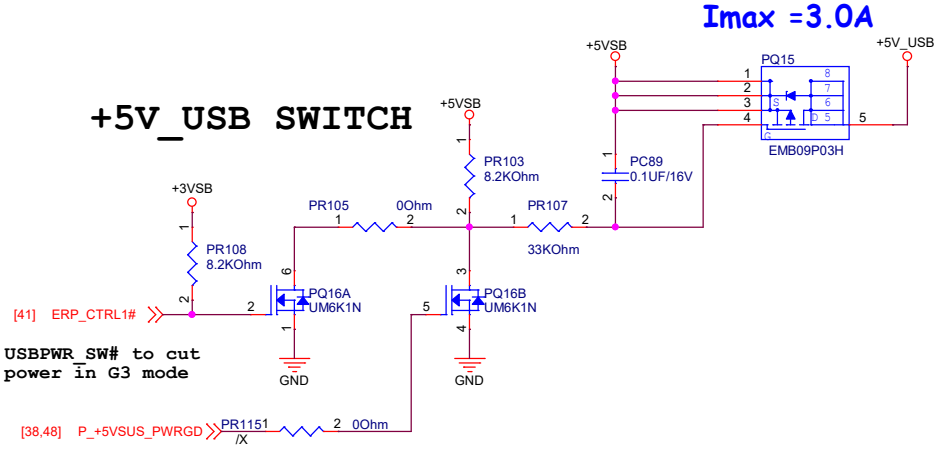




ASUSTek COMPUTER INC.	Title : +1.8VSB & +1.24VSB	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 51 of 57	







ASUSTek COMPUTER INC.	Title : +1.05V, USB_PWR	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
Date: Monday, November 04, 2019	Sheet 52 of 57	

+VNN POWER

TSEN: 150mV
DVID_TH 15mV, VBOOT 1.05V

SET1: 123mV & 907mV
ICCMax 6A, AI Gain 20, PSYS Disable,
DVID_Width 5.36 uS

SET2: 1427mV & 846mV
TONSET 7KTON, OCS 120% ICCMAX,
VR Address 0x02, Zero Load-Line
Disable, ANTIOVS Disable.

SET3: 1581mV & 1055mV
QR_TH 40(mV), QR_WIDTH 70% of On-Time,
IPSK 50mV / Avgain, ANTIOVS_TH 30mV.

PR120 form 82 ohm to 160 ohm
PR122 from 162 ohm to 240 ohm
Follow PDG Ver:3.0

VIN +12V~+24V

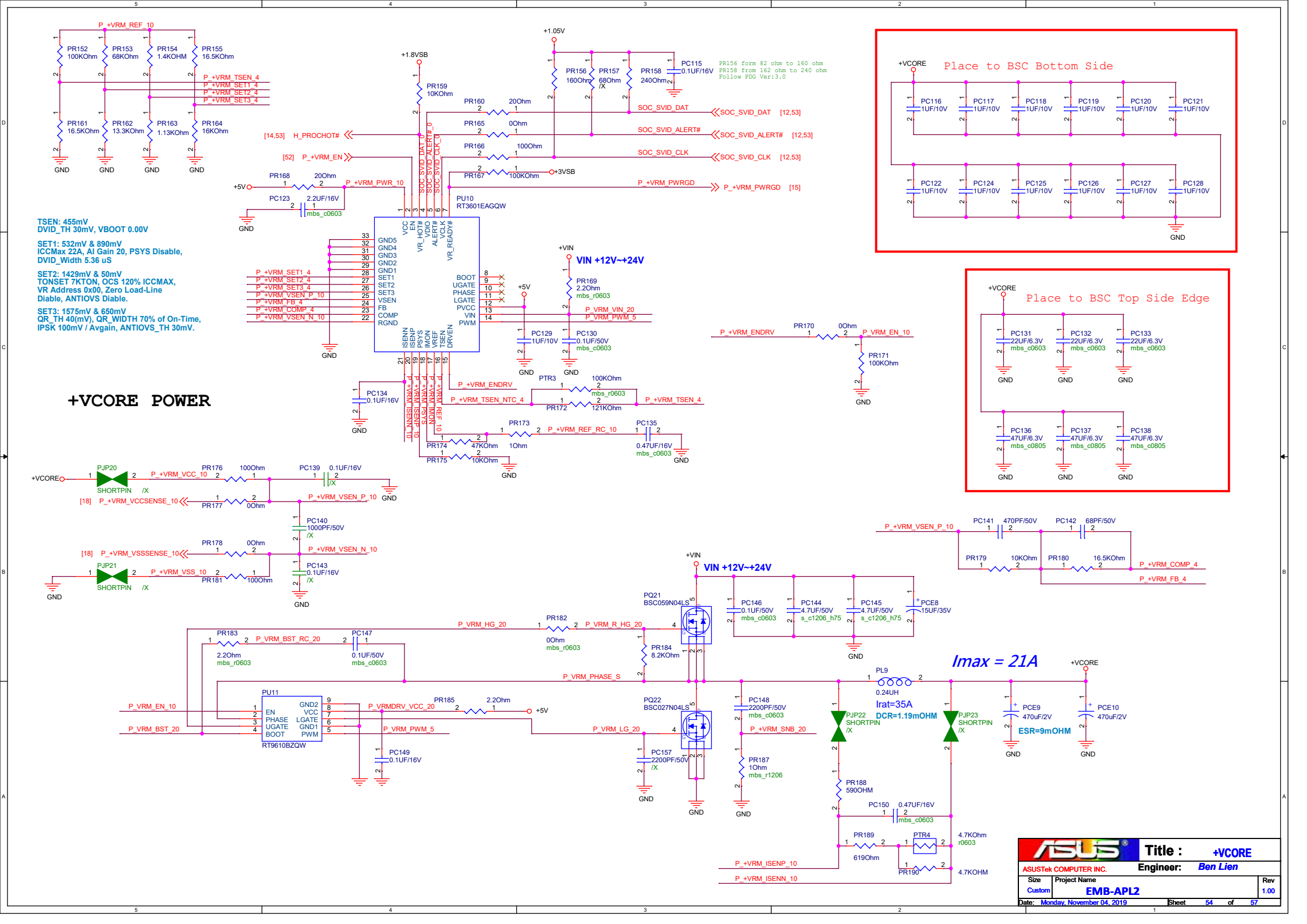
Imax = 4.8A

Irat=16A
DCR=4.8mOHM
ESR=9mOHM

Place to BSC Bottom Side

Place to BSC Top Side Edge

ASUSTek COMPUTER INC.	Title : +VNN		
	Engineer: Ben Lien		
Size: Custom	Project Name: EMB-APL2		Rev: 1.00
Date: Monday, November 04, 2019	Sheet 53 of 57		


+VCORE POWER
TSEN: 455mV
DVID_TH 30mV, VBOOT 0.00V
SET1: 532mV & 890mV
ICCMax 22A, AI Gain 20, PSYS Disable,
DVID_Width 5.36 uS
SET2: 1429mV & 50mV
TONSET 7KTON, OCS 120% ICCMAX,
VR Address 0x00, Zero Load-Line
Diable, ANTIOVS Diable.
SET3: 1575mV & 650mV
QR_TH 40(mV), QR_WIDTH 70% of On-Time,
IPSK 100mV / Avgain, ANTIOVS_TH 30mV.
PU10
RT3601EAGQW
PU11
RT9610BZQW
VIN +12V~+24V
Imax = 21A
Irat=35A
DCR=1.19mOHM
ESR=9mOHM
Place to BSC Bottom Side
Place to BSC Top Side Edge
PR156 form 82 ohm to 160 ohm
PR158 from 162 ohm to 240 ohm
Follow PDG Ver:3.0
ASUSTek COMPUTER INC.
Title : +VCORE
Engineer: Ben Lien
Size Custom
Project Name EMB-APL2
Rev 1.00
Date: Monday, November 04, 2019
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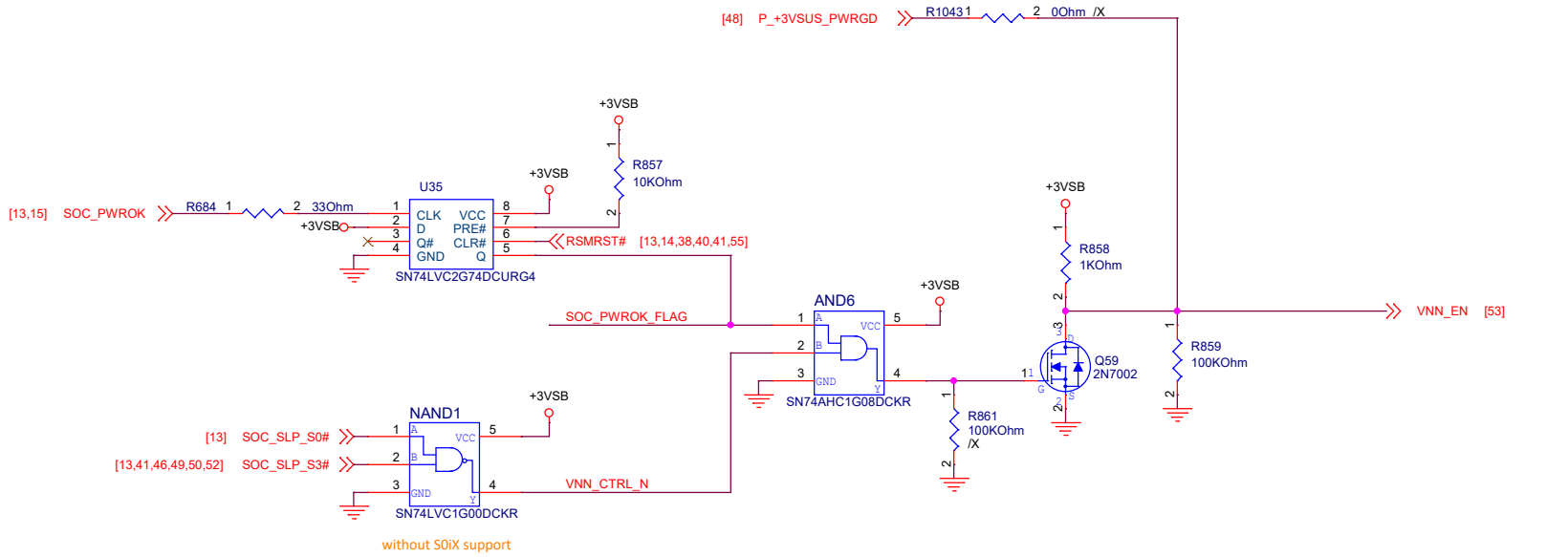

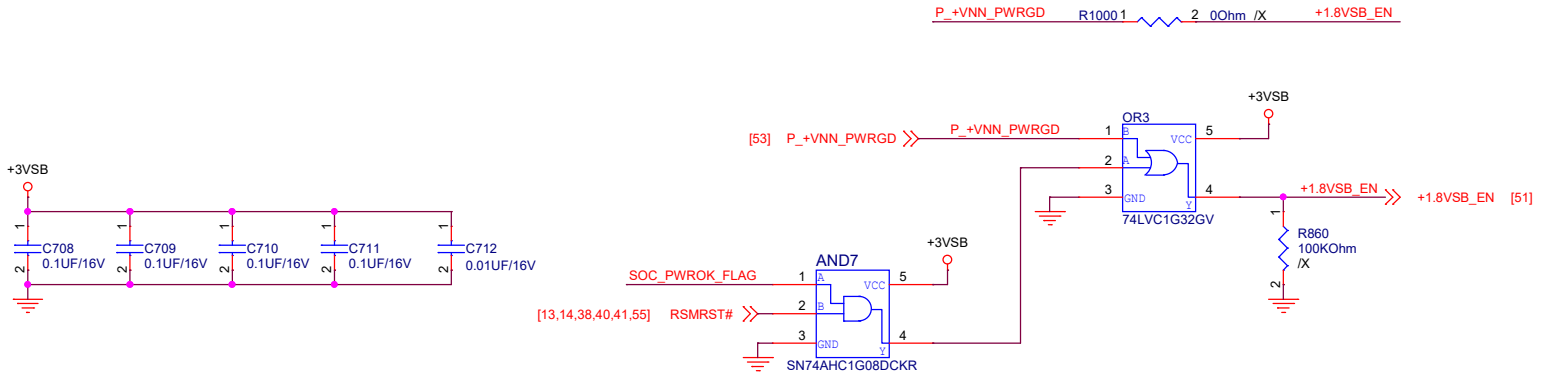

ASUSTek COMPUTER INC.	Title : VNN_CTRL	
	Engineer: Ben Lien	
Size: B	Project Name: EMB-APL2	Rev: 1.00
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