

MAX-Q370C Port Assignment

Cannon Lake PCH Q370 (MP)

USB Setting

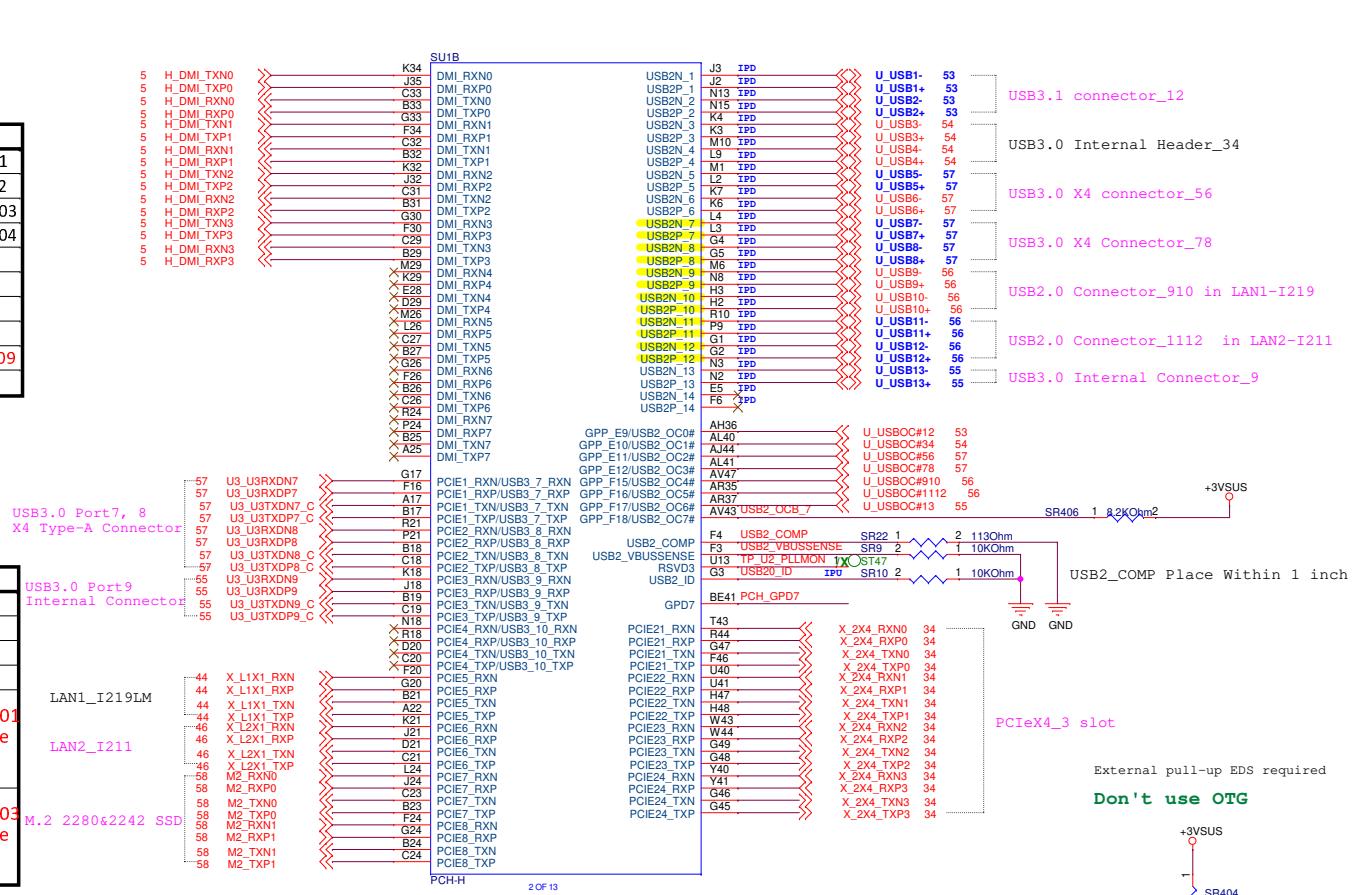
USB 2.0	Function
USB2_01	PS2+USB31 Gen2-10G#01
USB2_02	PS2+USB31 Gen2-10G#02
USB2_03	Internal Header USB30 #03
USB2_04	Internal Header USB30 #04
USB2_05	USB31-Gen1_5G #05
USB2_06	USB31-Gen1_5G #06
USB2_07	USB31-Gen1_5G #07
USB2_08	USB31-Gen1_5G #08
USB2_09	LAN1-I219+USB20#09
USB2_10	LAN1-I219+USB20#10
USB2_11	LAN2-I211+USB20#11
USB2_12	LAN2-I211+USB20#12
USB2_13	Internal Type-A USB31 #13
USB2_14	N/A

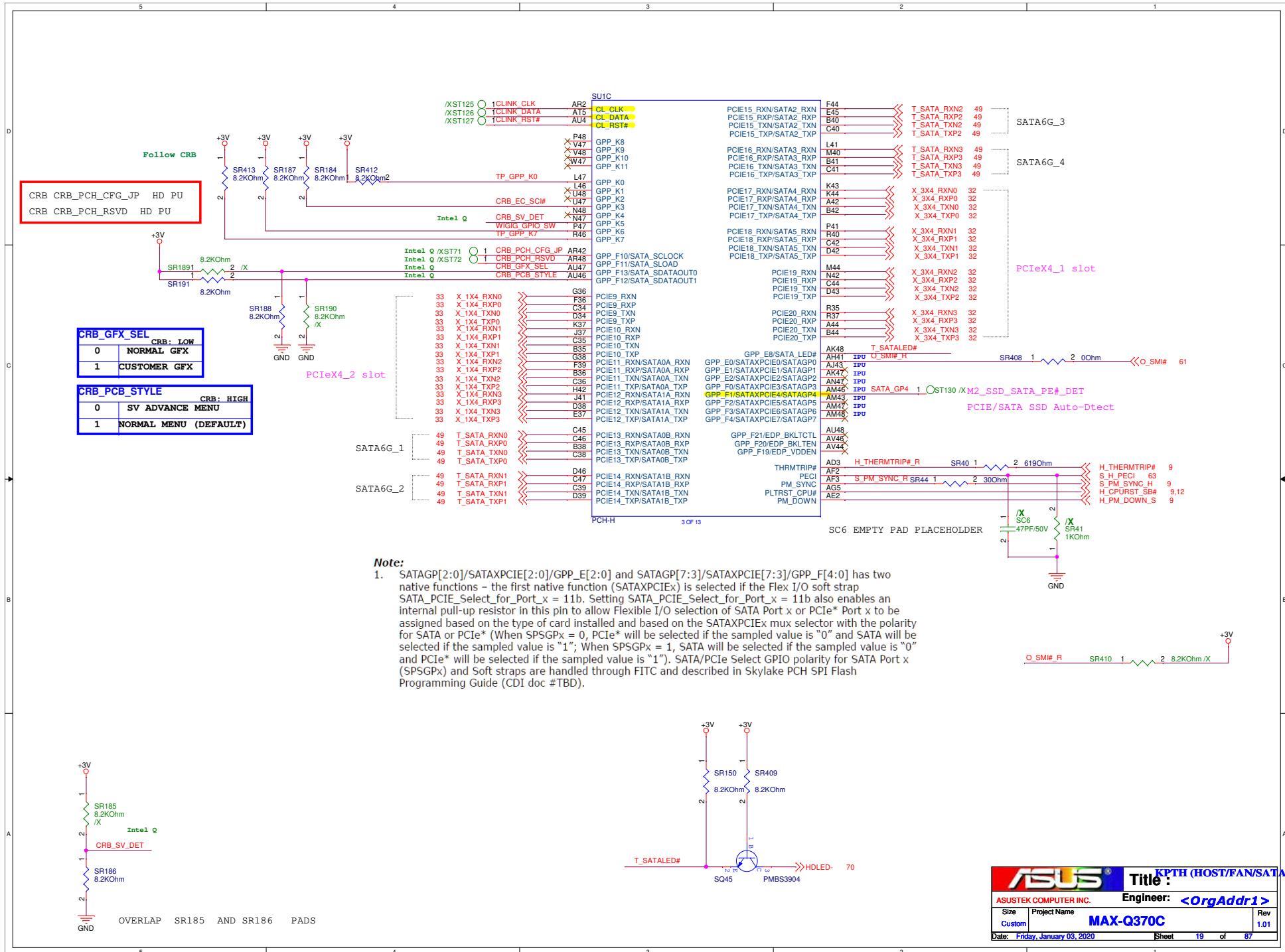
USB 3.1	Function
USB31_01	PS2+USB31 Gen2-10G#01
USB31_02	PS2+USB31 Gen2-10G#02
USB31_03	Internal Header USB30 #03
USB31_04	Internal Header USB30 #04
USB31_05	USB31-Gen1_5G #05
USB31_06	USB31-Gen1_5G #06
USB31_07	USB31-Gen1_5G #07
USB30_08	USB31-Gen1_5G #08
USB30_09	Internal Type-A USB31 #09
USB30_10	N/A

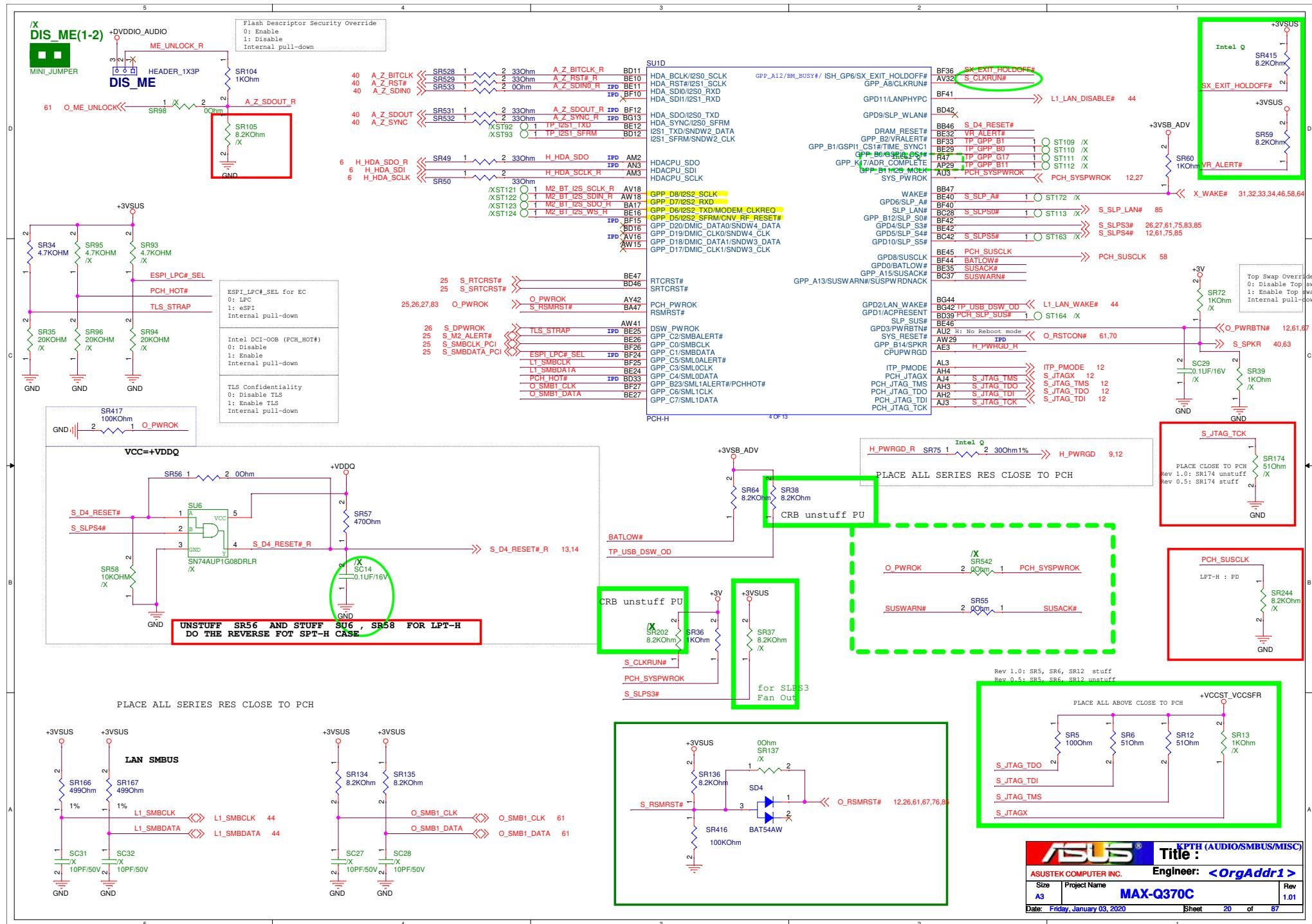
PCIE/SATA Function Define

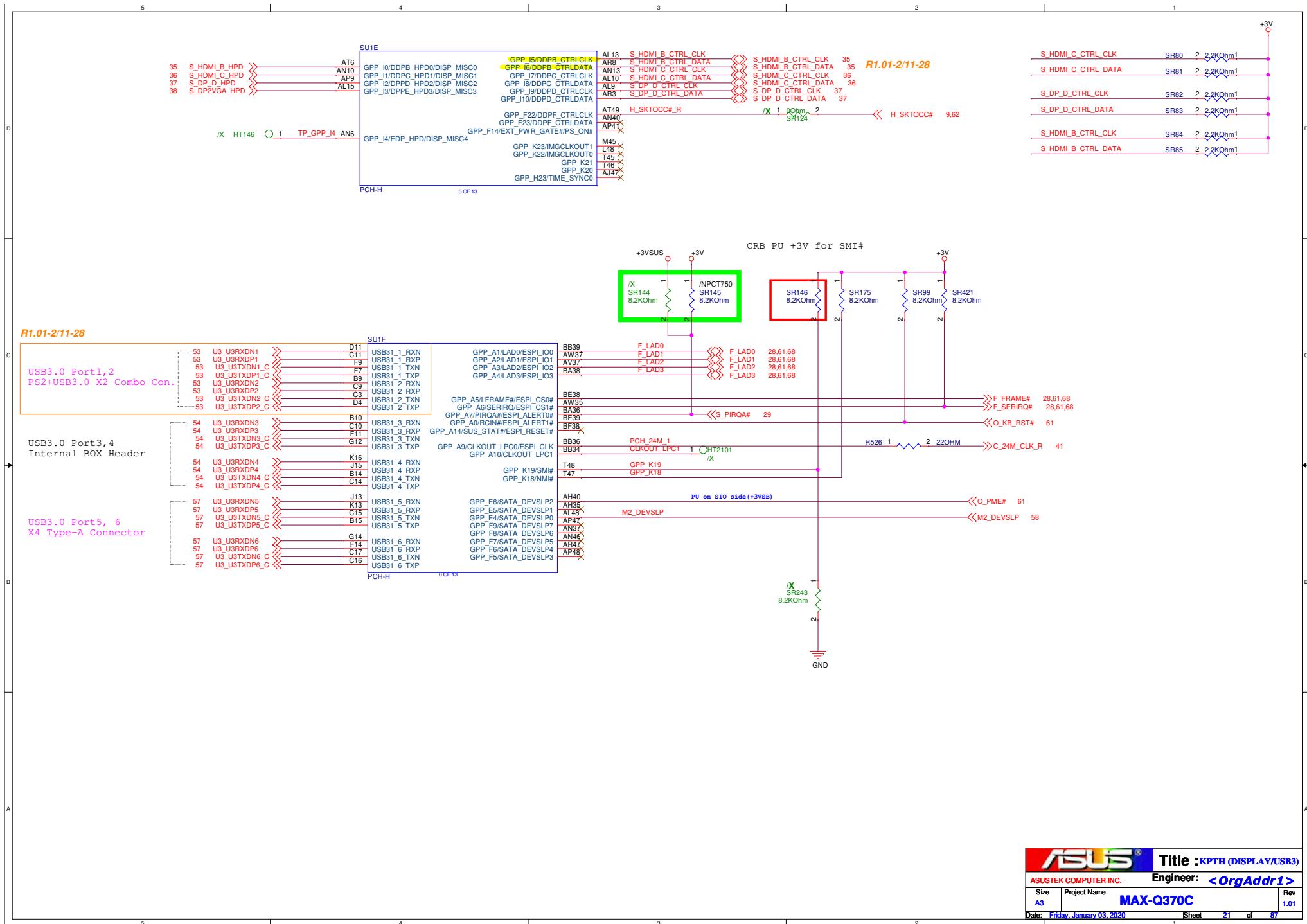
	Function
PCIE-01 (USB3#7)	USB31-Gen1 #07
PCIE-02 (USB3#8)	USB31-Gen1 #08
PCIE-03 (USB3#9)	Internal USB31 #09
PCIE-04 (USB3#10)	N/A
PCIE-05	LAN1_I219LM
PCIE-06	LAN2_I211
PCIE-07	M.2_Key-M SSD (PCIe2x Only)
PCIE-08	
PCIE-09	
PCIE-10	PCIeX4_2 slot#02 Support Optane
PCIE-11 (SATA-0a)	(IRST)
PCIE-12 (SATA-1a)	
PCIE-13 (SATA-0b)	SATA6G_1
PCIE-14 (SATA-1b)	SATA6G_2
PCIE-15 (SATA-2)	SATA6G_3
PCIE-16 (SATA-3)	SATA6G_4
PCIE-17 (SATA-4)	
PCIE-18 (SATA-5)	PCIeX4_1 slot#01 Support Optane
PCIE-19 (SATA-6)	(IRST)
PCIE-20 (SATA-7)	
PCIE-21	
PCIE-22	PCIeX4_3 slot#03 Support Optane
PCIE-23	(IRST)
PCIE-24	

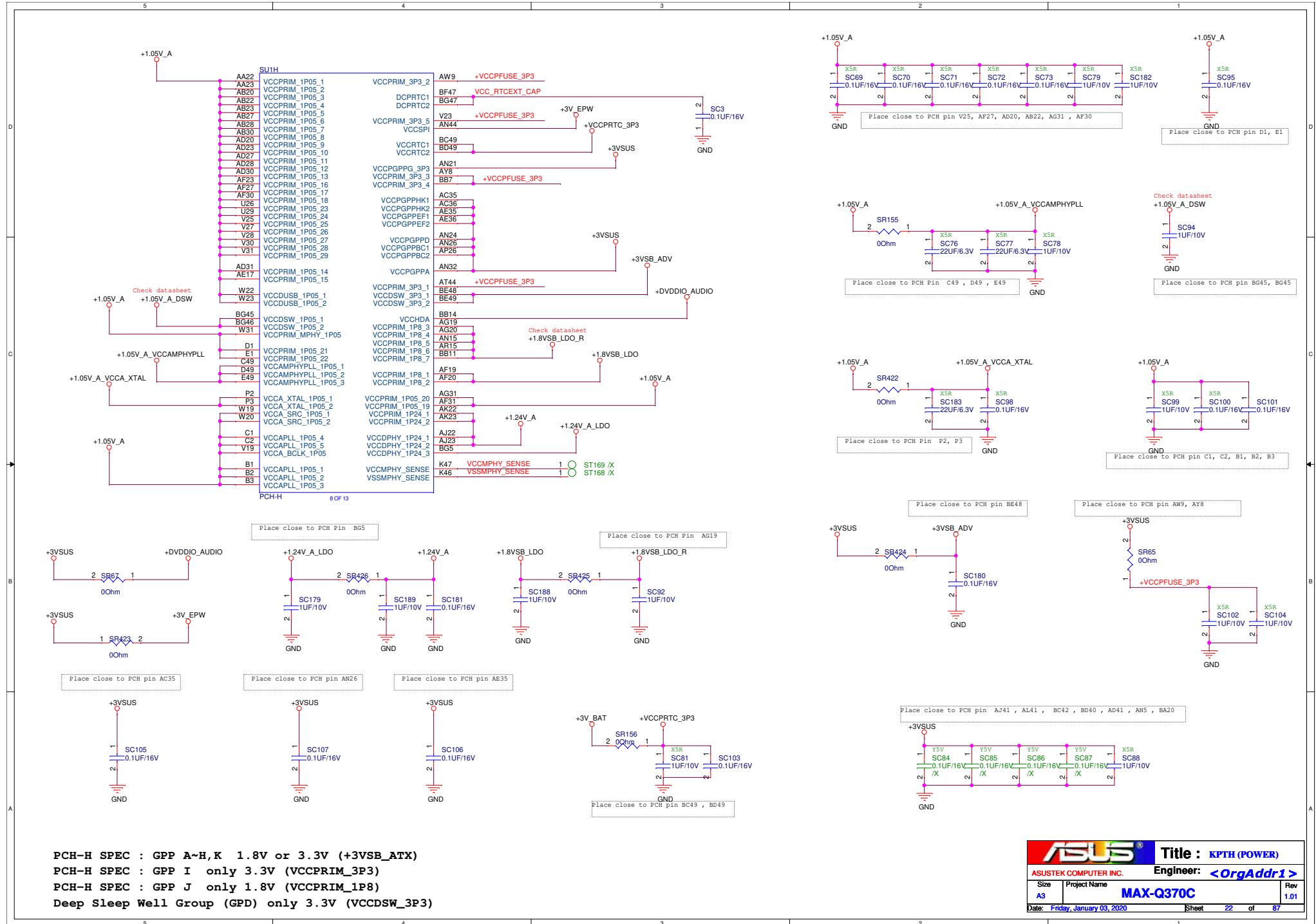
	Function
CLKREQ-0	M.2_BT_UART_WAKE#
CLKREQ-1	
CLKREQ-2	CLK_REQ2_LAN#
CLKREQ-3	
CLKREQ-4	
CLKREQ-5	
CLKREQ-6	
CLKREQ-7	
CLKREQ-8	CLK_REQ8_M.2_SSD#
CLKREQ-9	
CLKREQ-10~15	

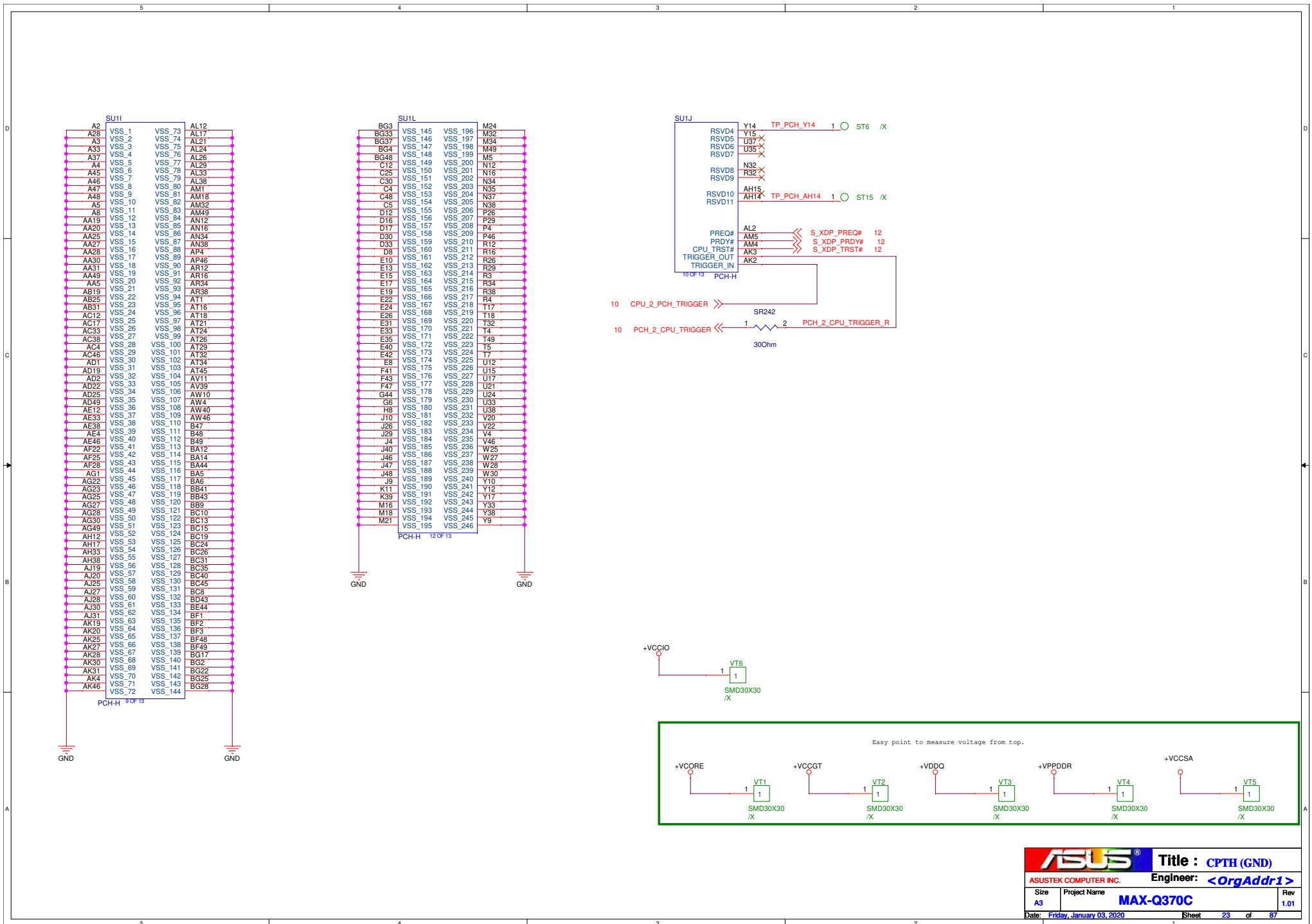


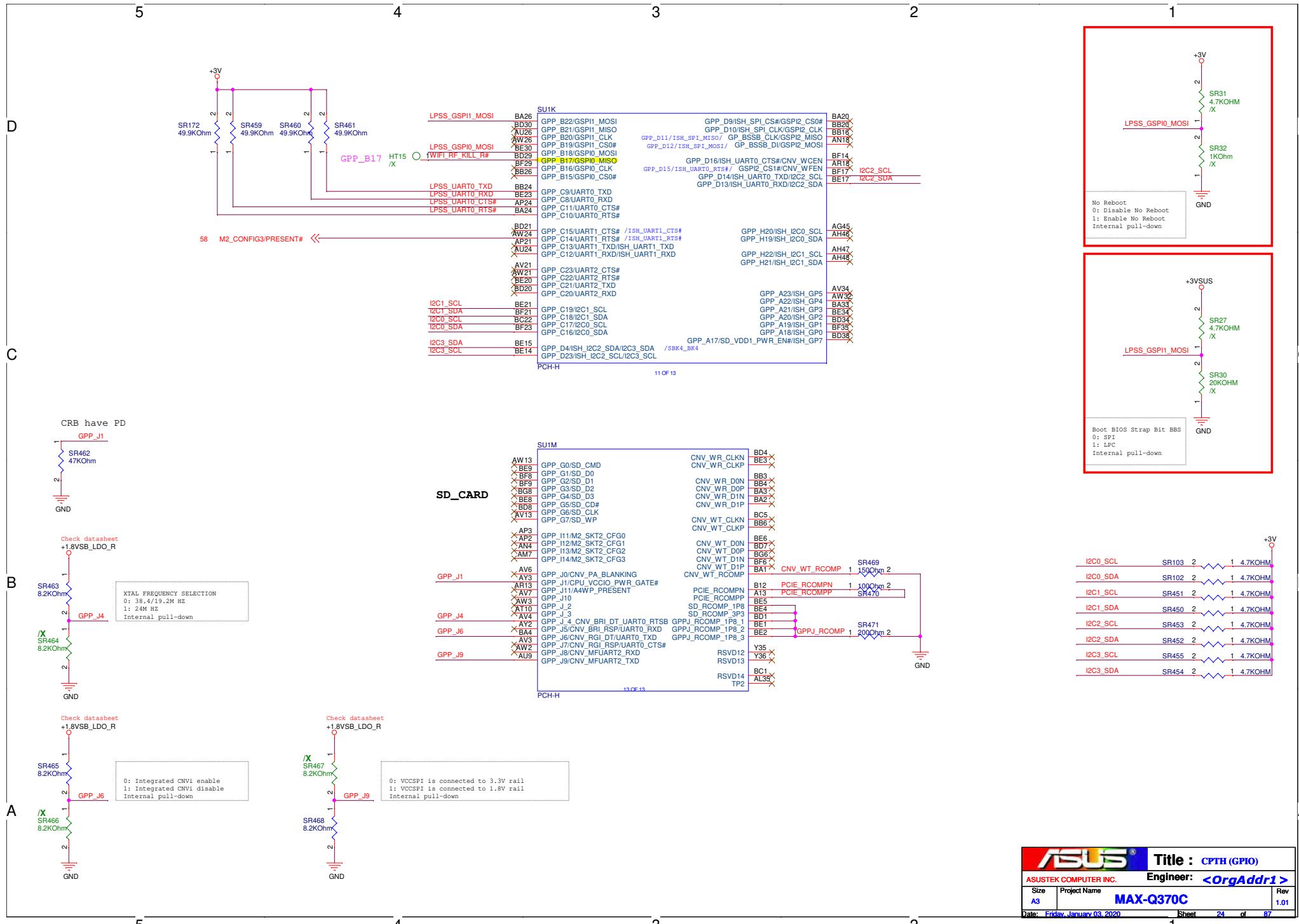


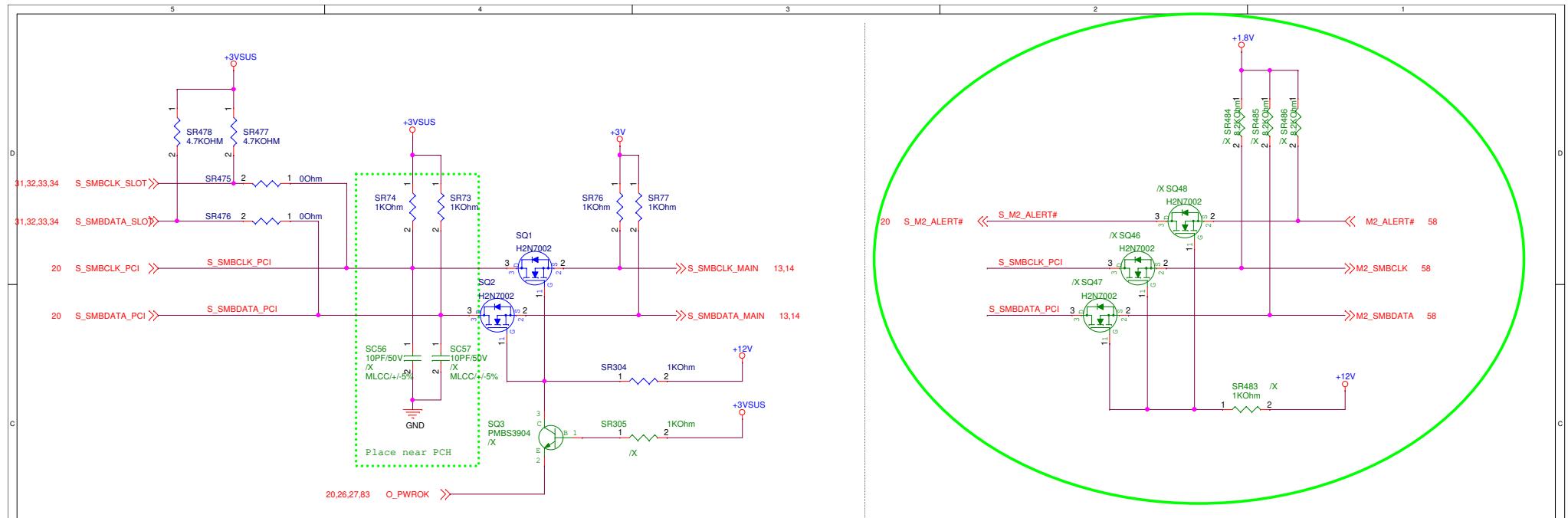






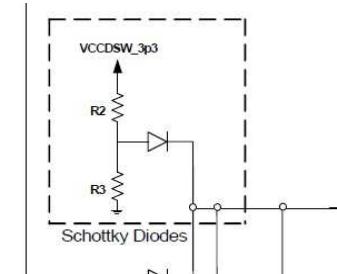
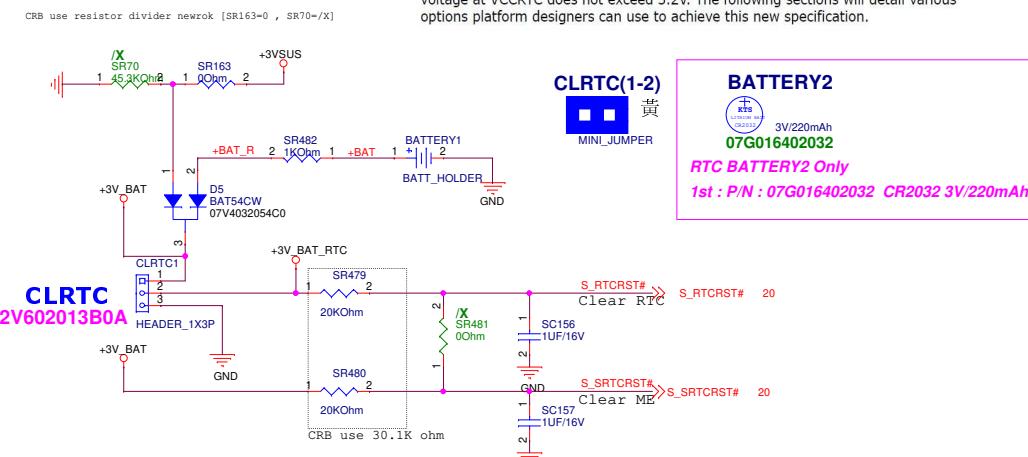


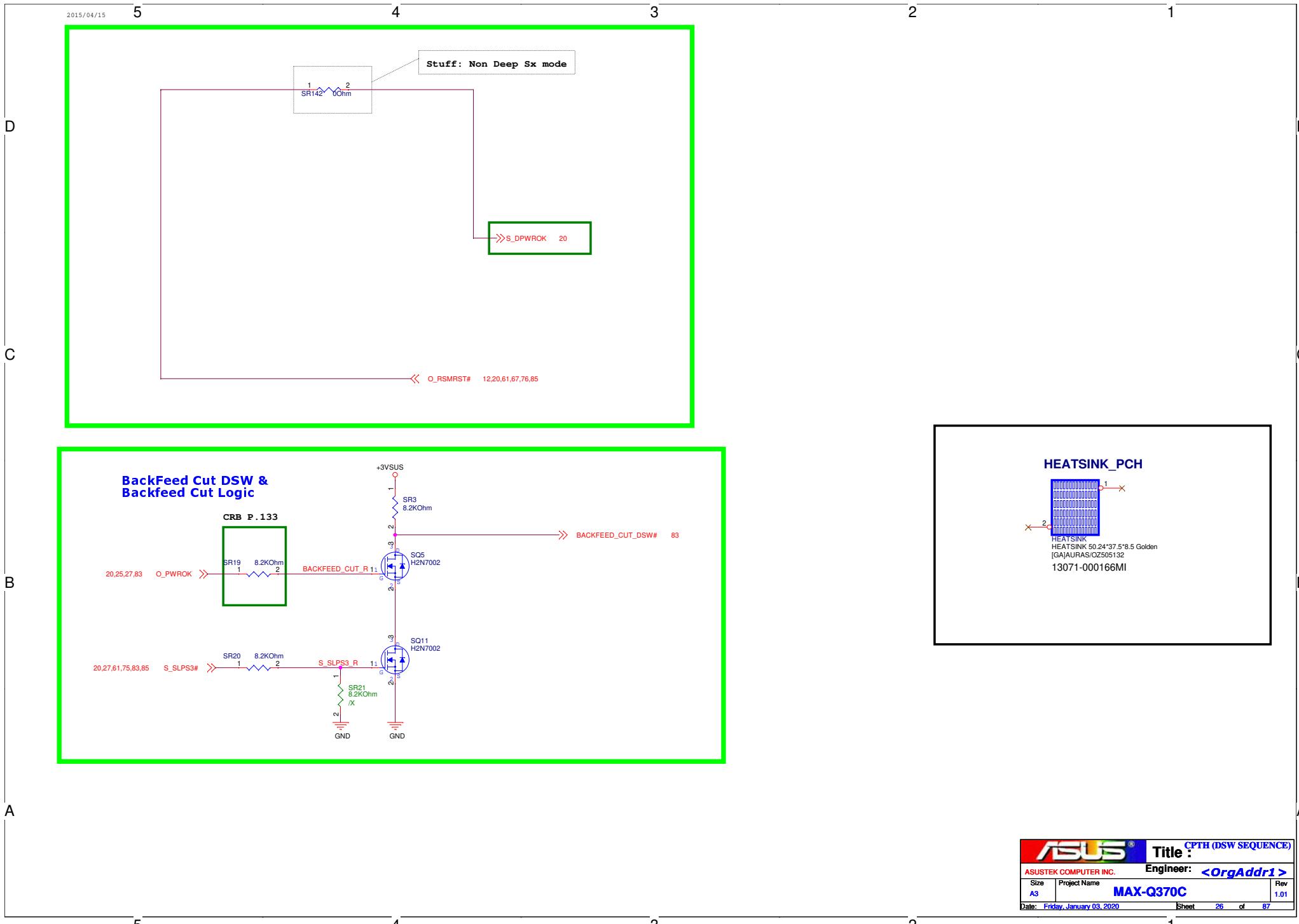




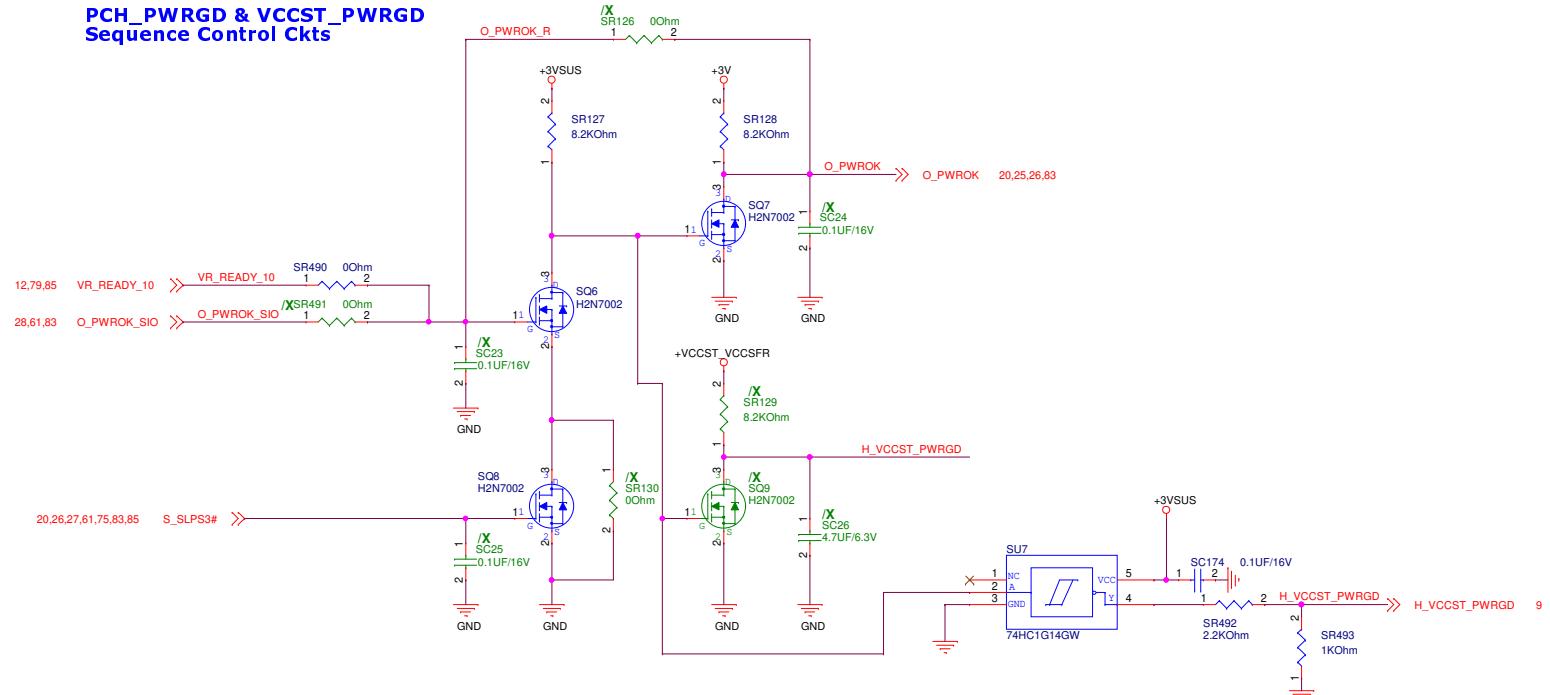
VCCRTC External Circuit

On SKL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

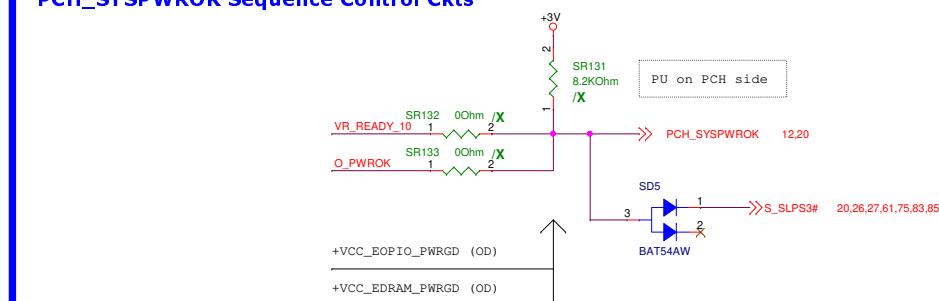




PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPOWEROK Sequence Control Ckts

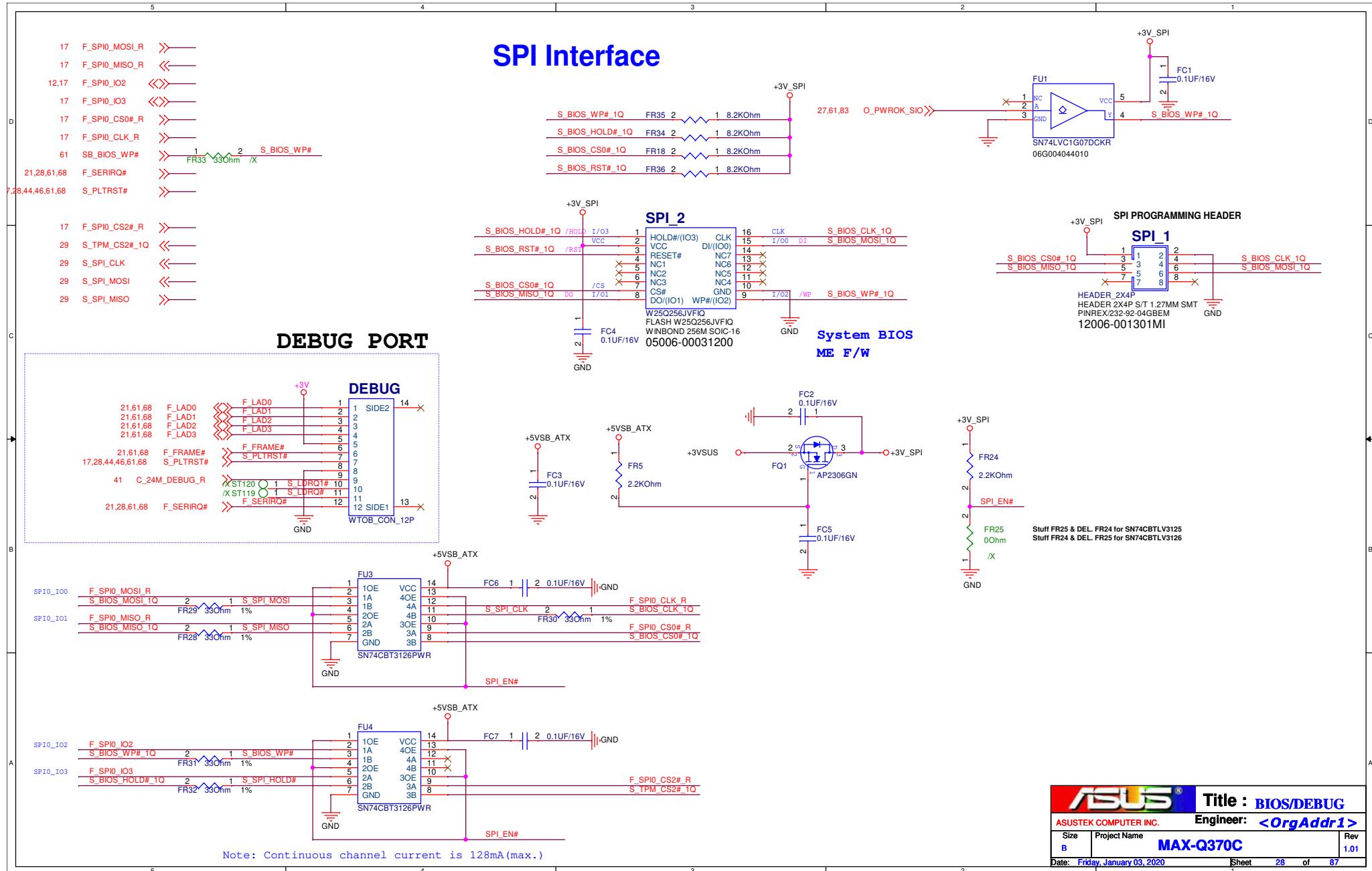


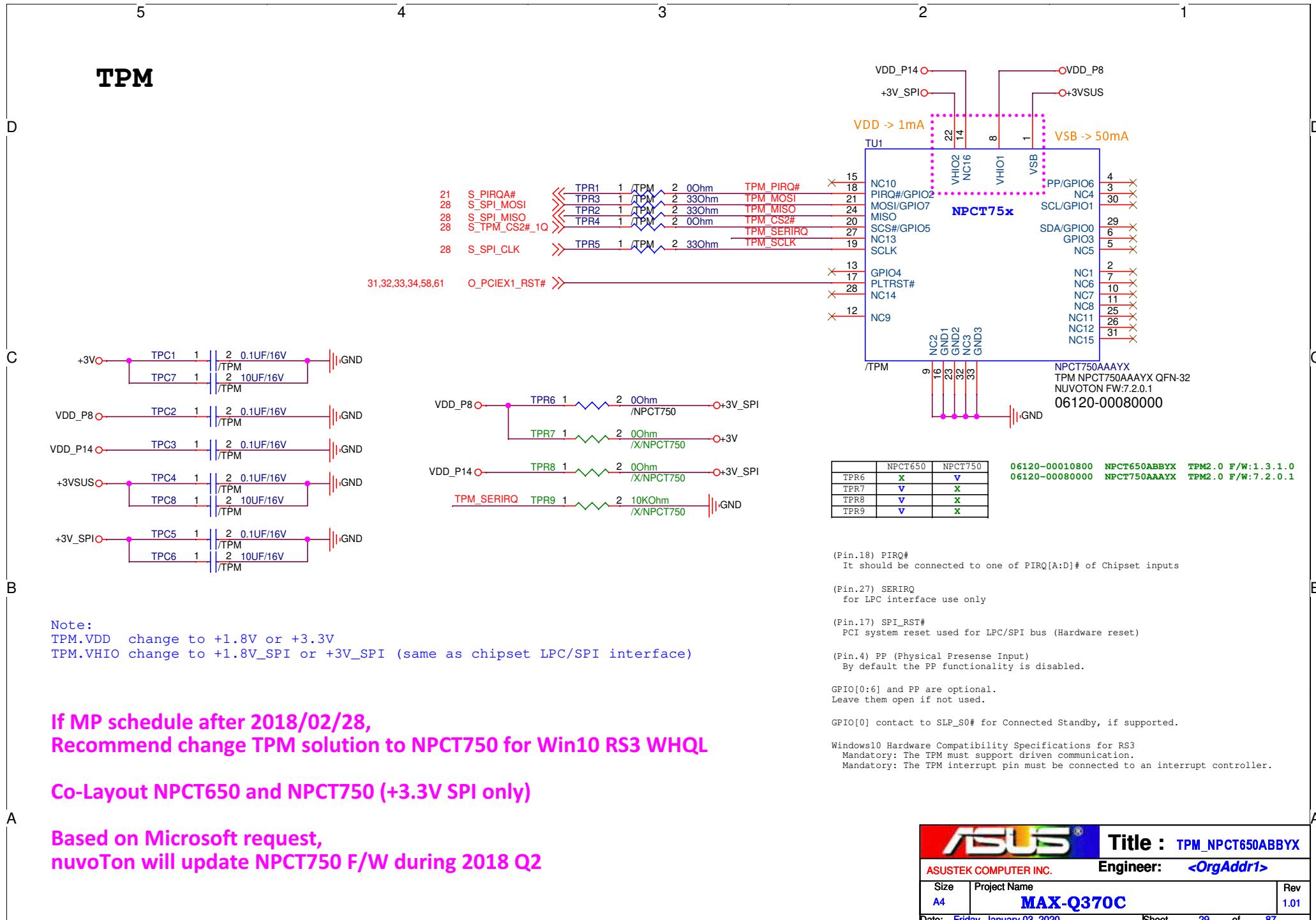
1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

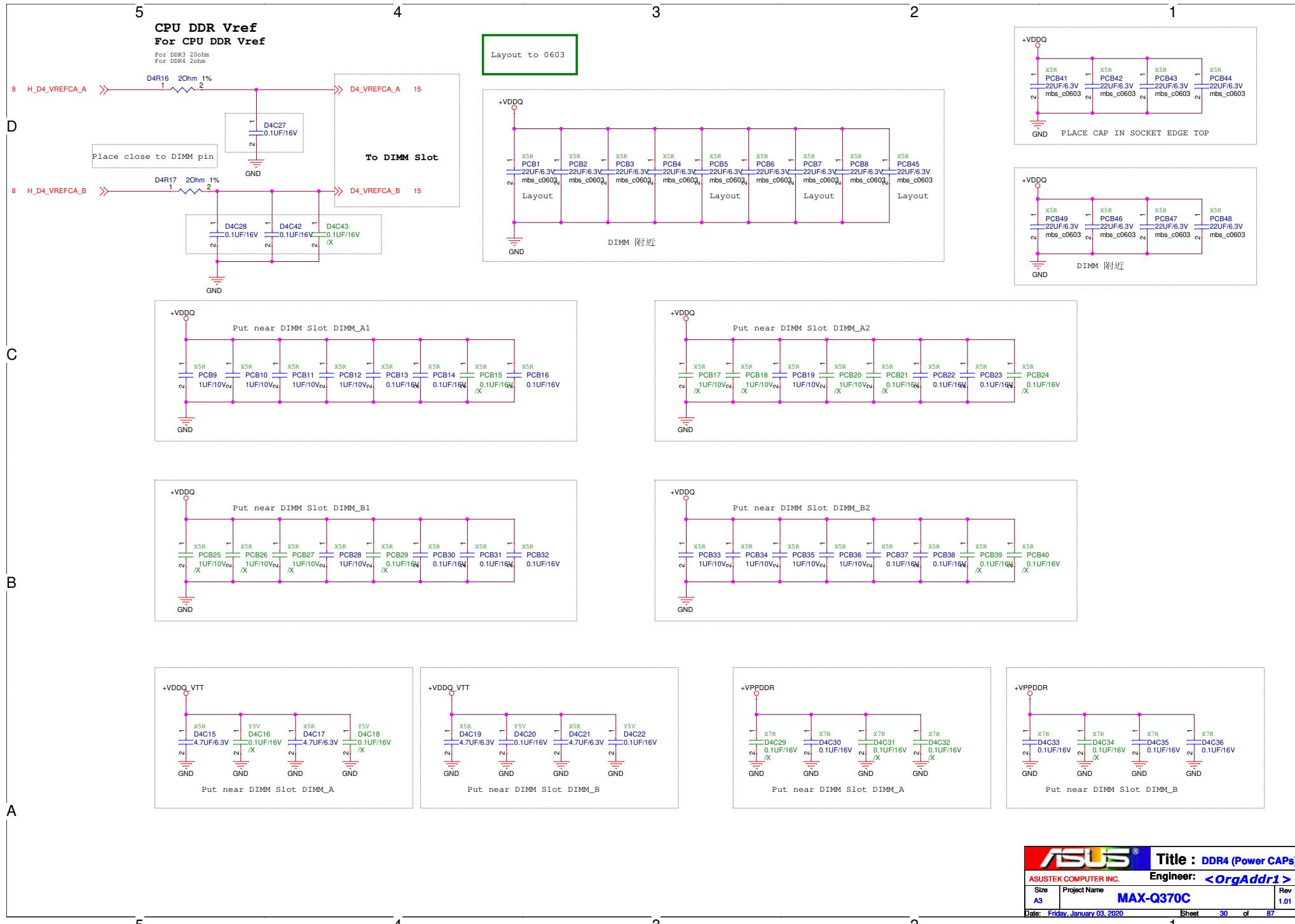
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

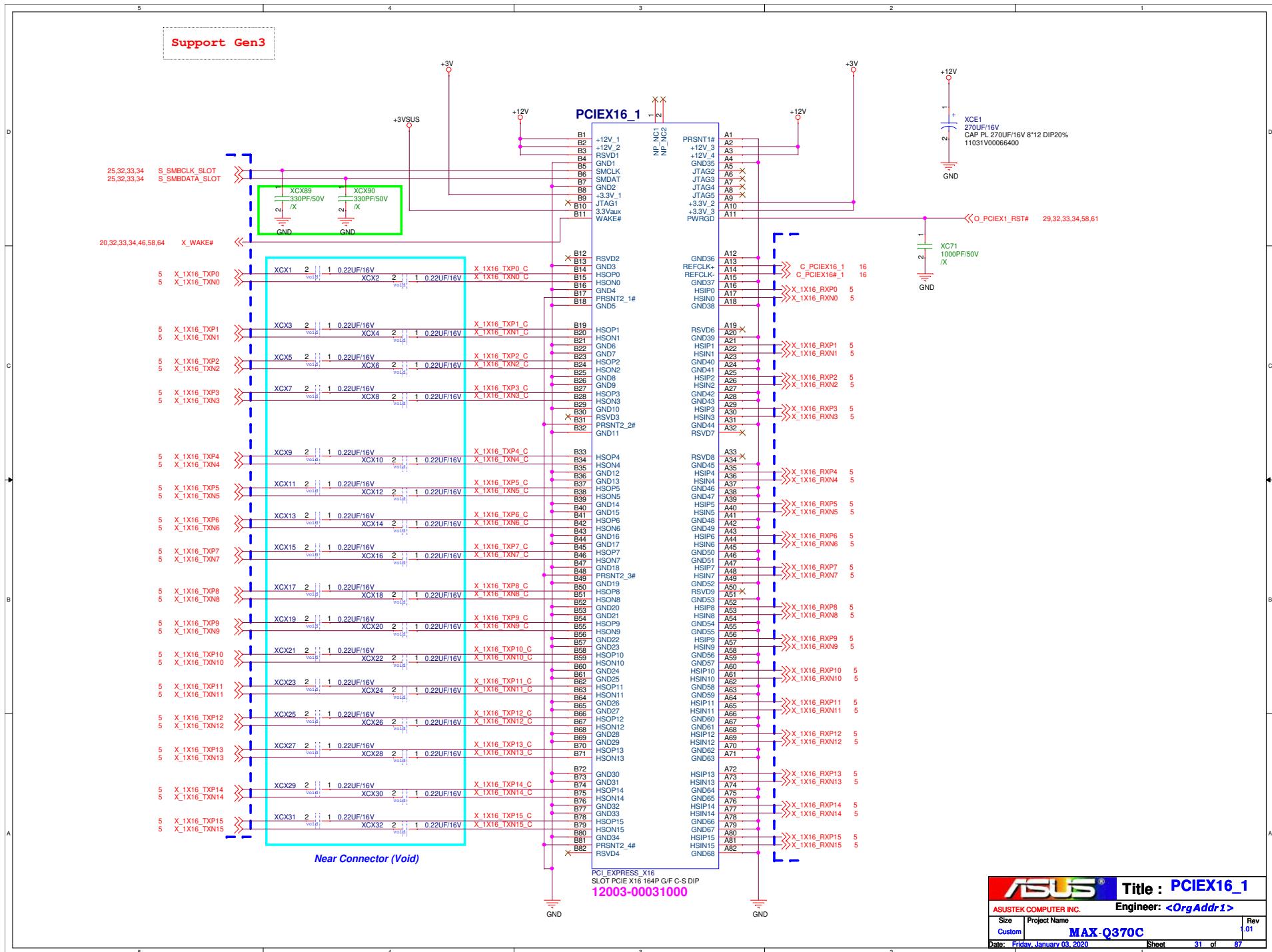
3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

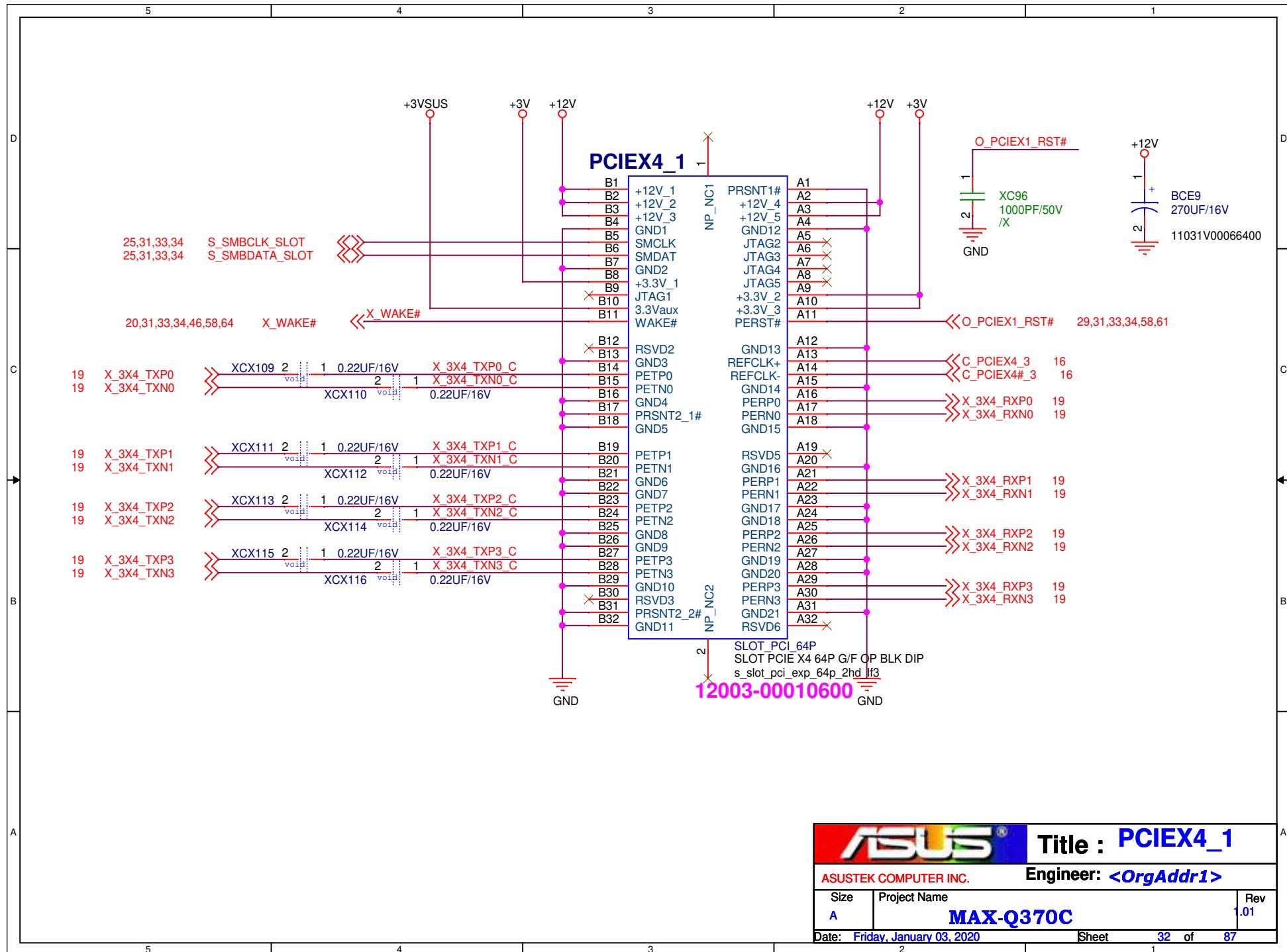
4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.









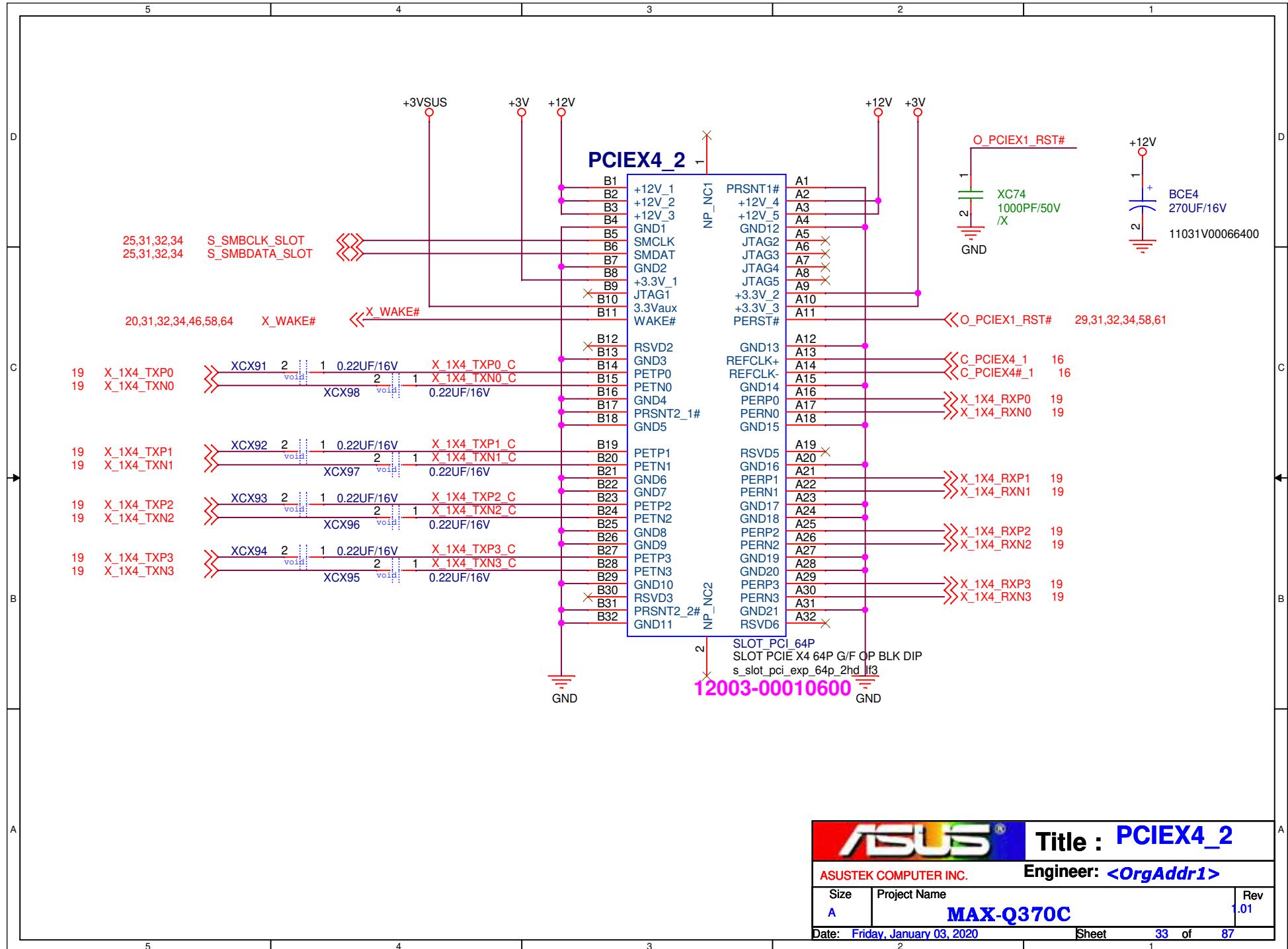


Title : PCIEX4_1

ASUSTEK COMPUTER INC.

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	MAX-Q370C	1.01
Date: Friday, January 03, 2020	Sheet 32 of 87	

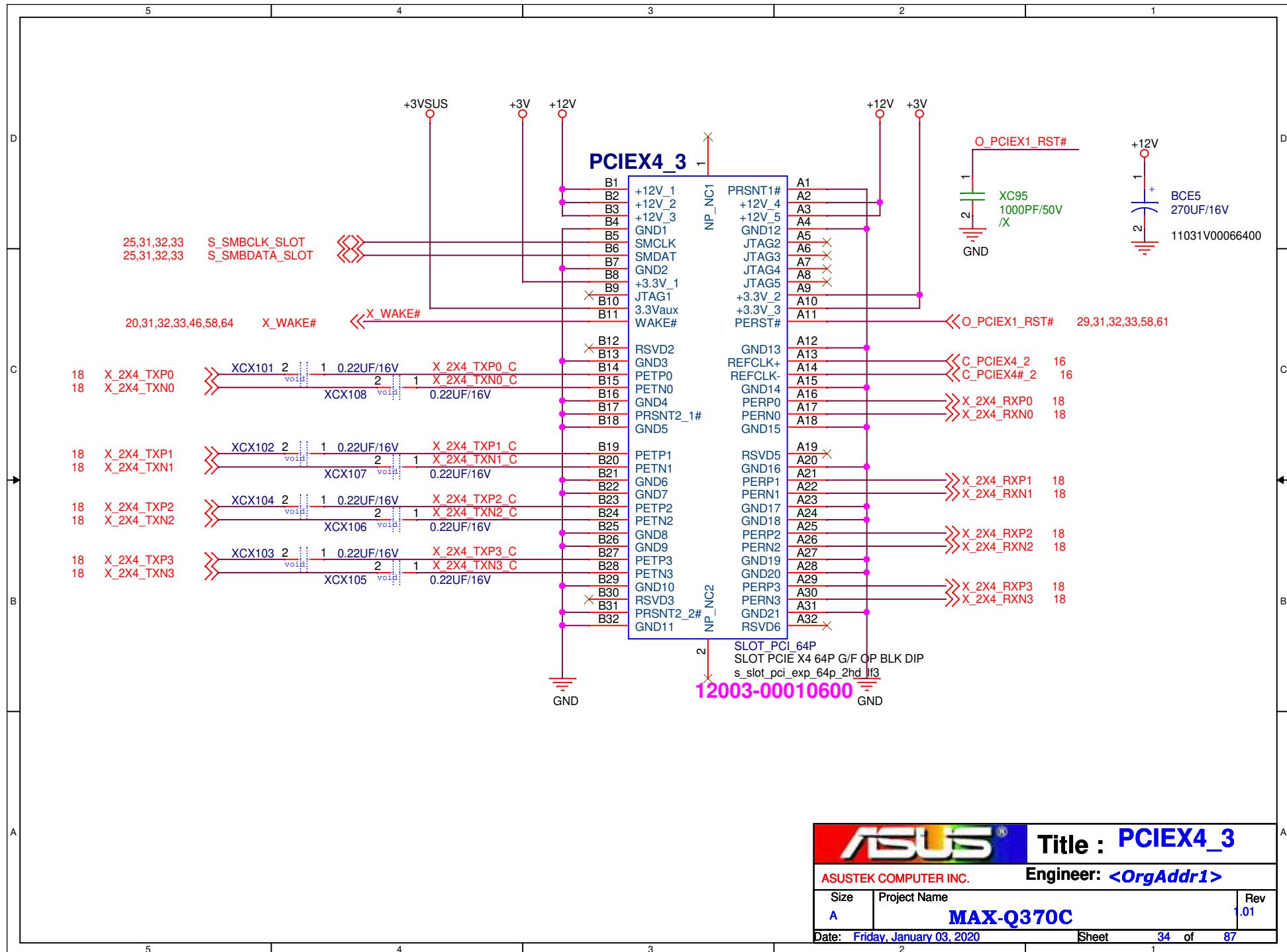


Title : PCIEX4_2

ASUSTEK COMPUTER INC.

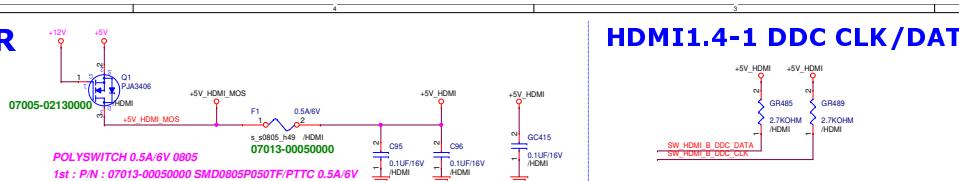
Engineer: <OrgAddr1>

Size	Project Name	Rev
A	MAX-Q370C	1.01
Date: Friday, January 03, 2020	Sheet 33 of 87	

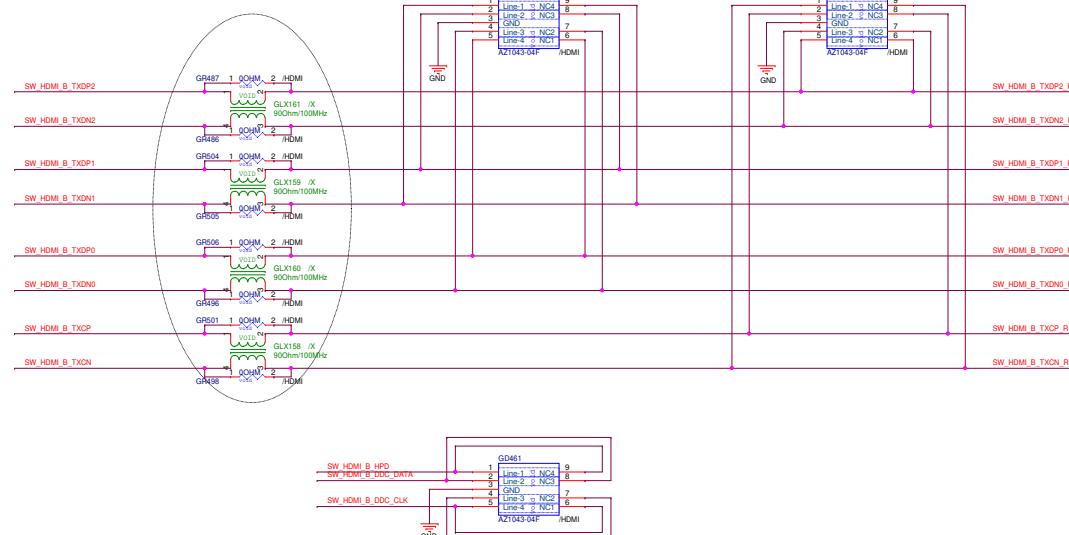
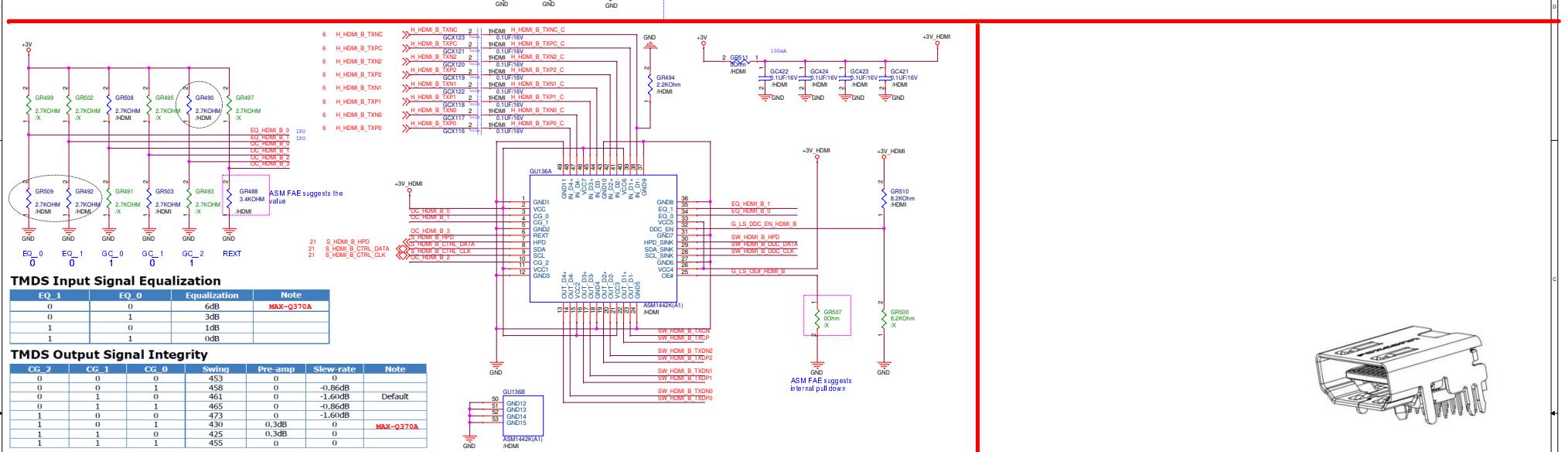


HDMI1.4-1 PWR

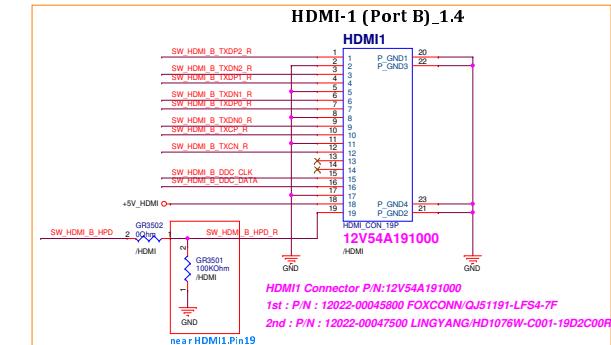
R1.01-1/11-28

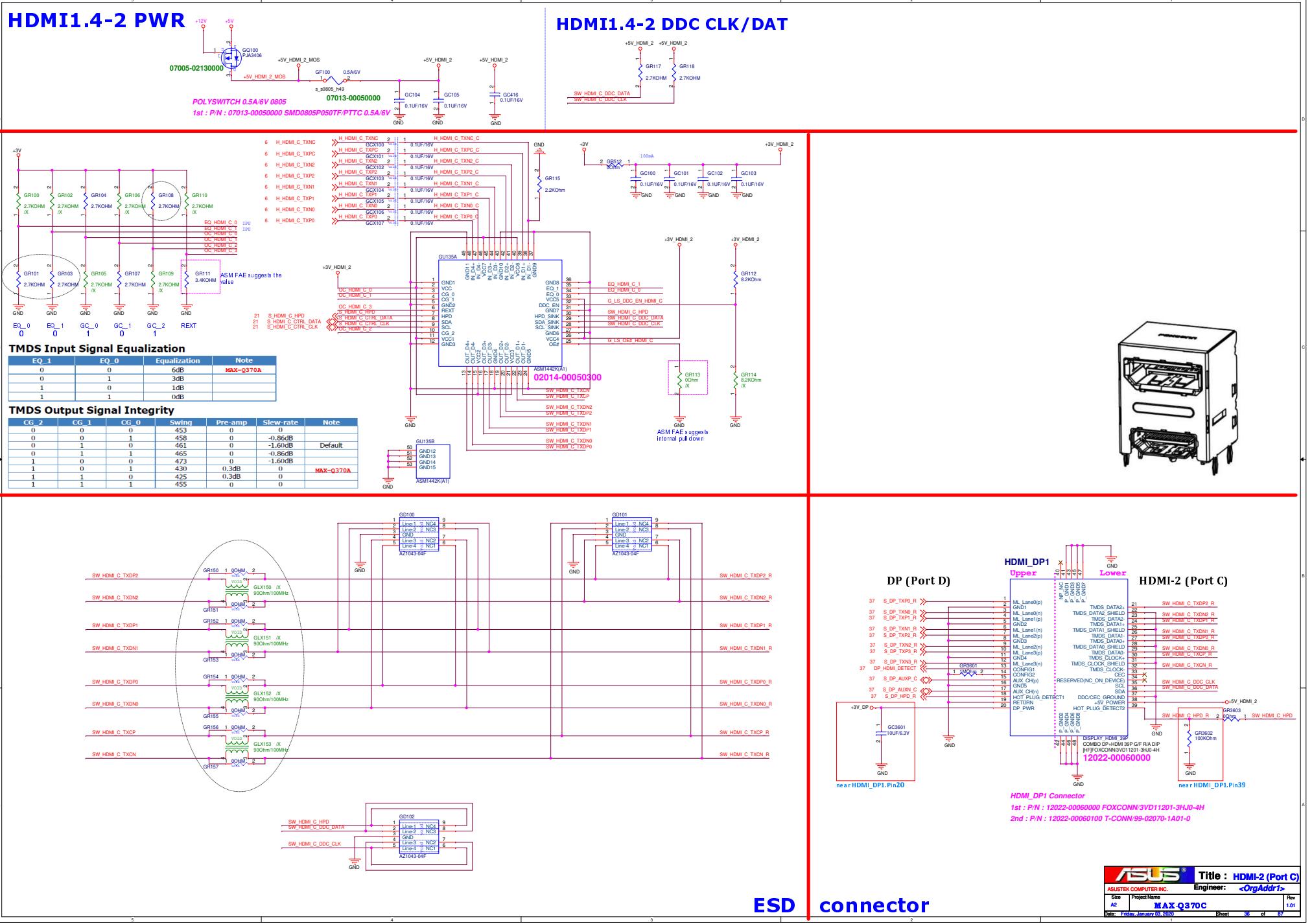


HDMI1.4-1 DDC CLK/DAT

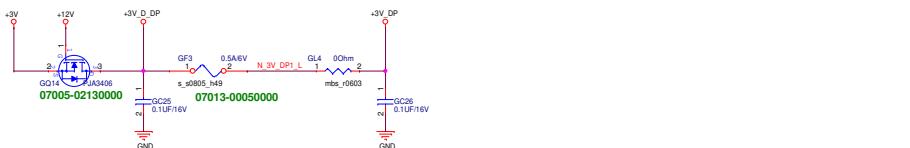


R1.01-2/11-28



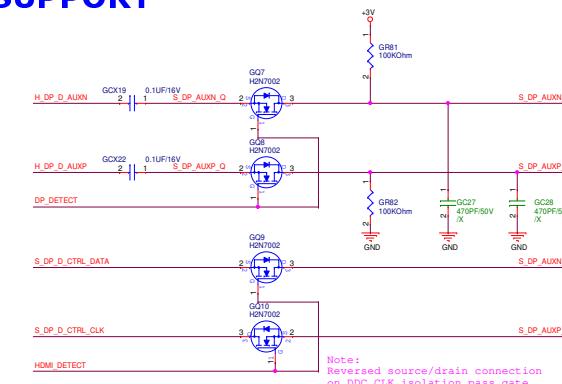


DP1.4 PWR



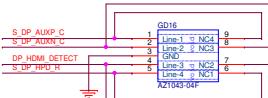
Legend for component types:
 6 H_D_P_D_TXP0
 6 H_D_P_D_TXN0
 6 H_D_P_D_TXP1
 6 H_D_P_D_TXN1
 6 H_D_P_D_TXP2
 6 H_D_P_D_TXN2
 6 H_D_P_D_TXP3
 6 H_D_P_D_TXN3
 6 H_D_P_D_AUXP
 6 H_D_P_D_AUXN
 21 S_D_P_D_HPD
 21 S_D_P_D_CTRL_CLK
 21 S_D_P_D_CTRL_DATA

DP/HDMI INTEROPERABILITY SUPPORT



For DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit

ESD

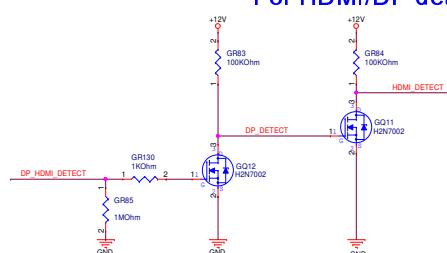


HPD

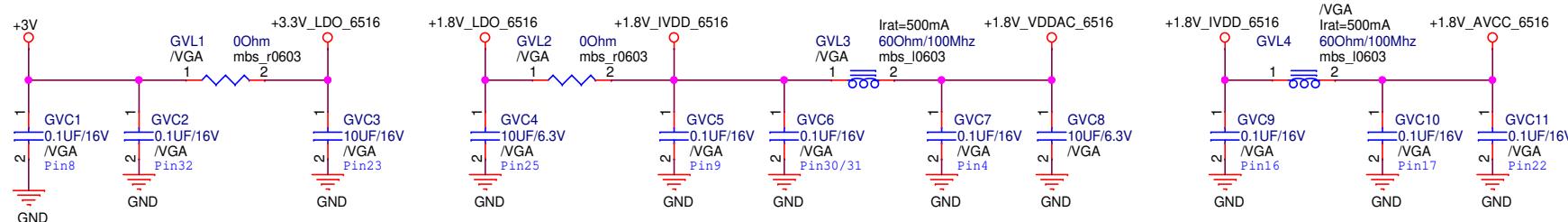


S_D_P_TXP0_R
S_D_P_TXP1_R
S_D_P_TXN0_R
S_D_P_TXN1_R
S_D_P_TXP2_R
S_D_P_TXN2_R
S_D_P_TXP3_R
S_D_P_TXN3_R
S_D_P_AUXP_C
S_D_P_AUXN_C
DP_DETECT
S_D_P_HPD_R

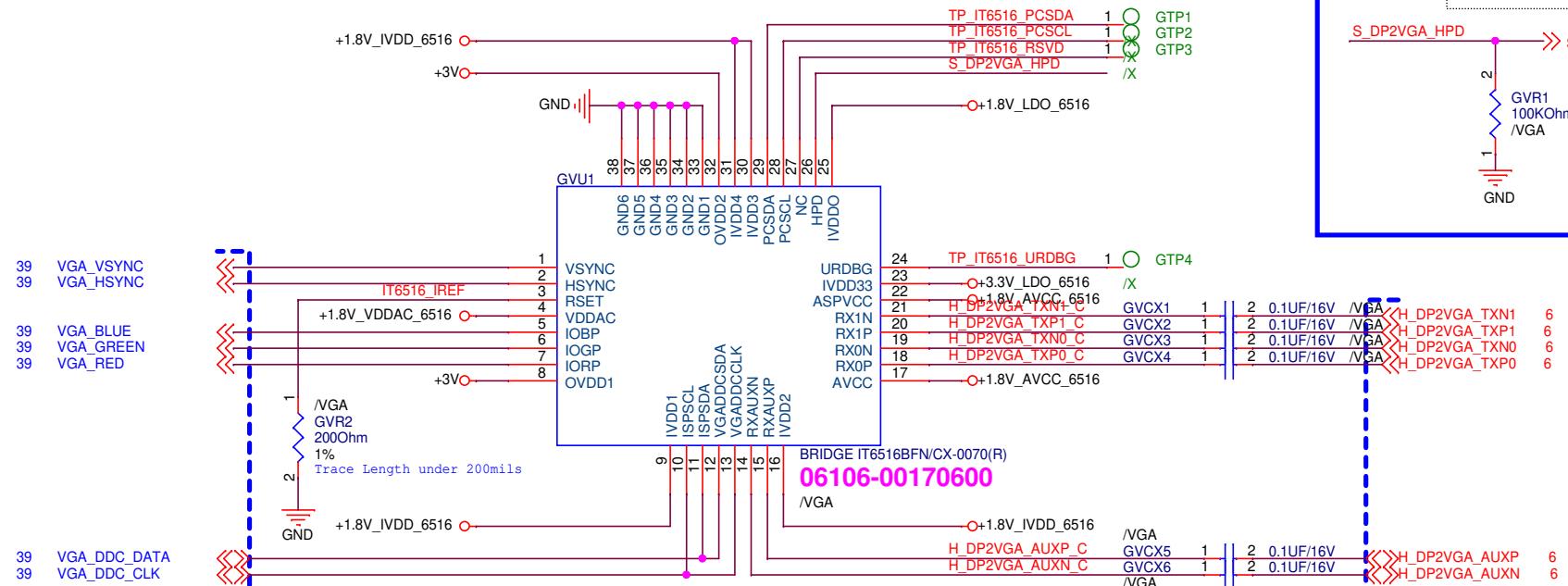
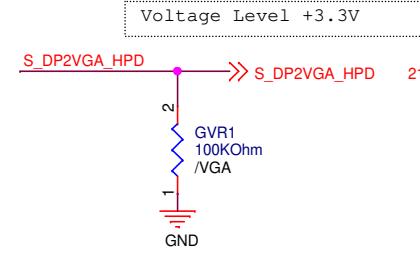
For HDMI/DP detect



IT6516B Power Caps and Beads



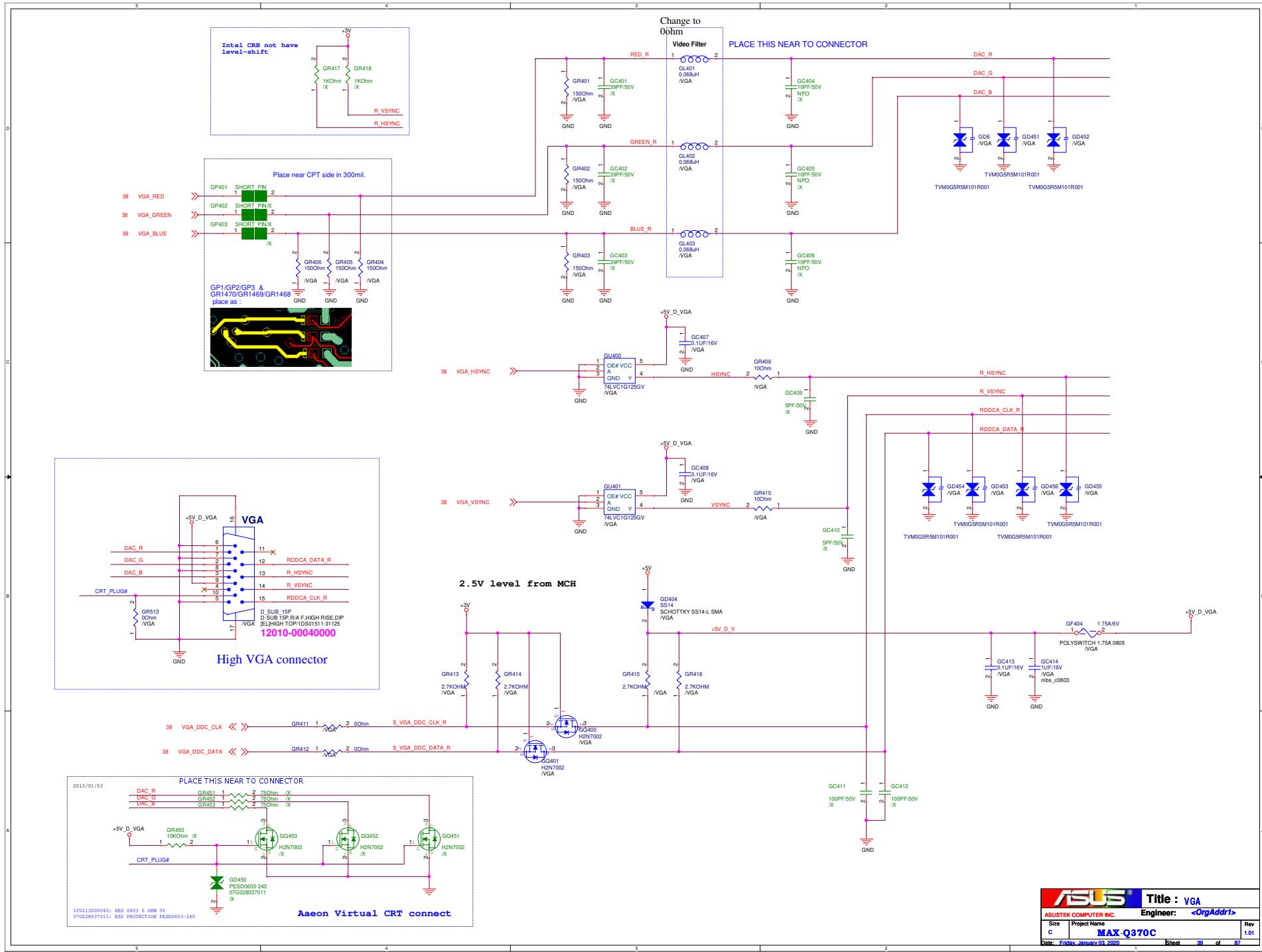
Hot-Plug Detect



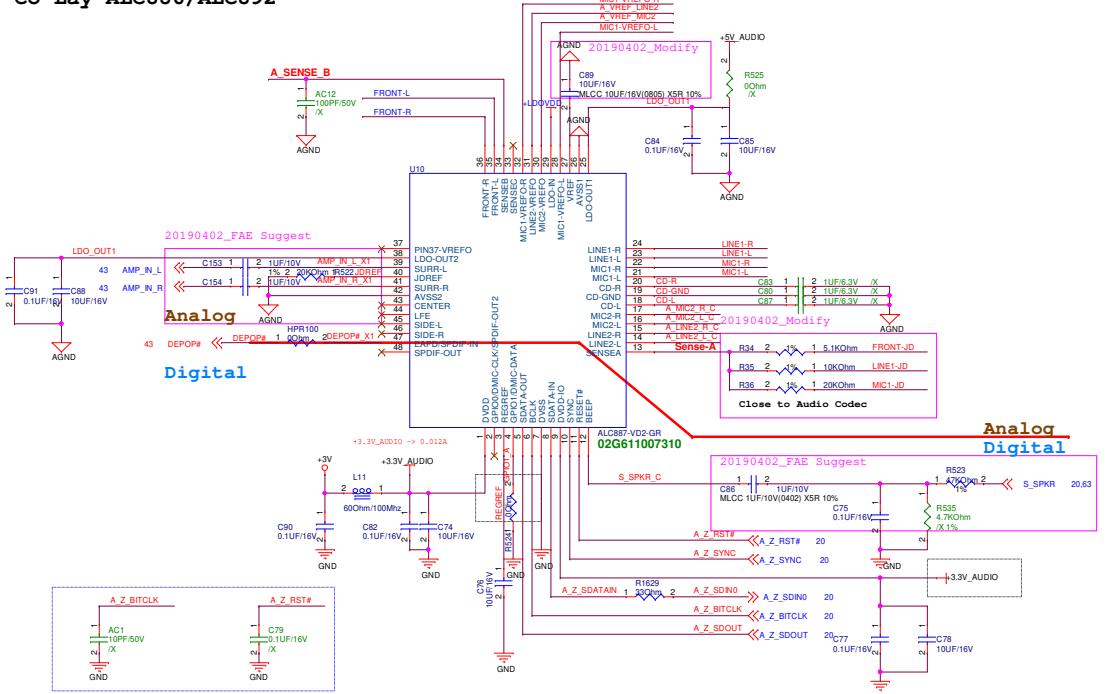
Title : DP to VGA_IT6516B

Engineer: <OrgAddr1>

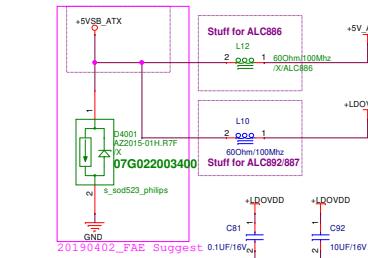
Size	Project Name	Rev
A4	MAX-Q370C	1.01
Date: Friday, January 03, 2020	Sheet 38	of 87



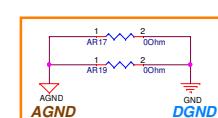
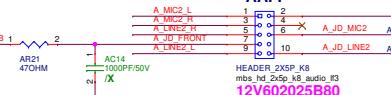
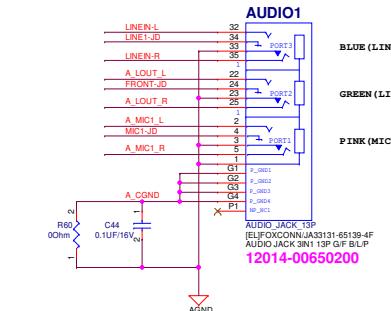
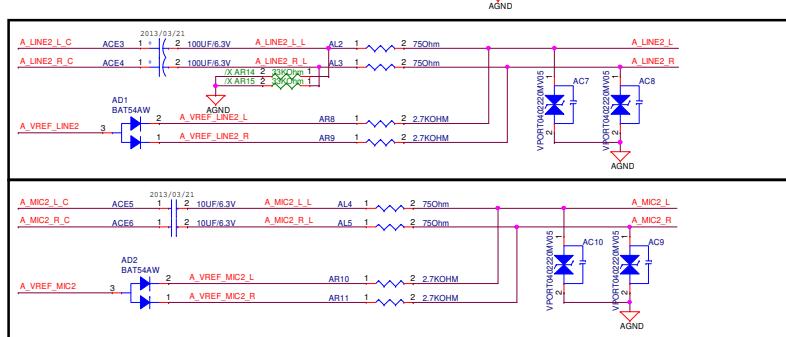
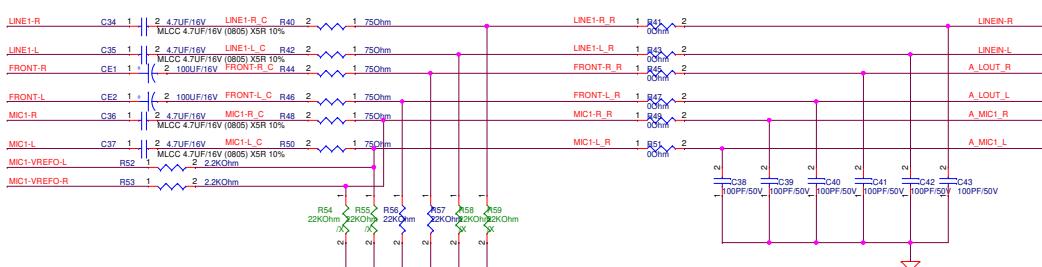
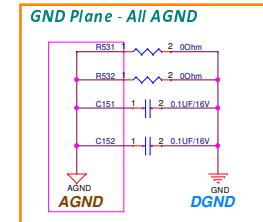
Co-Lay ALC886/ALC892

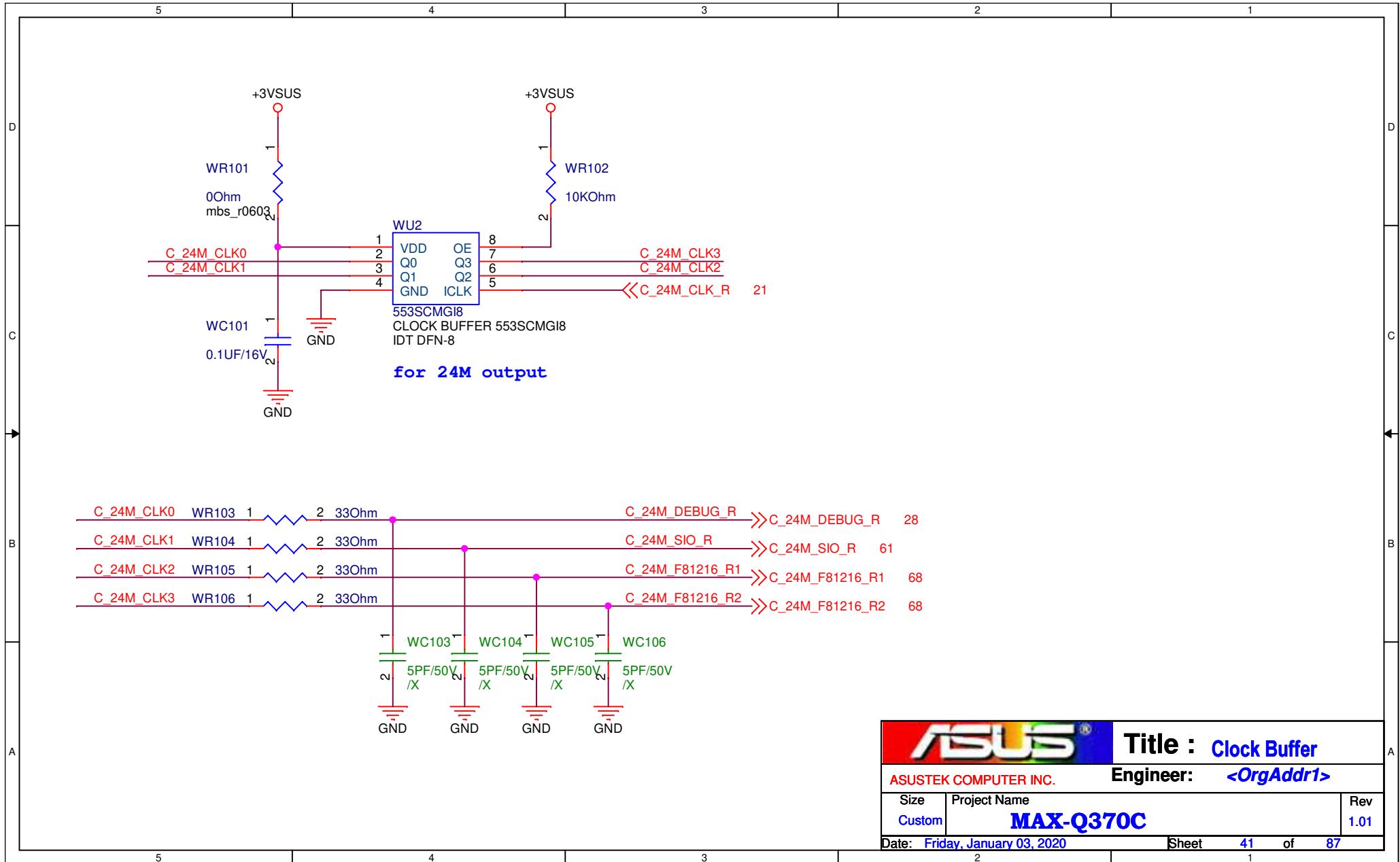


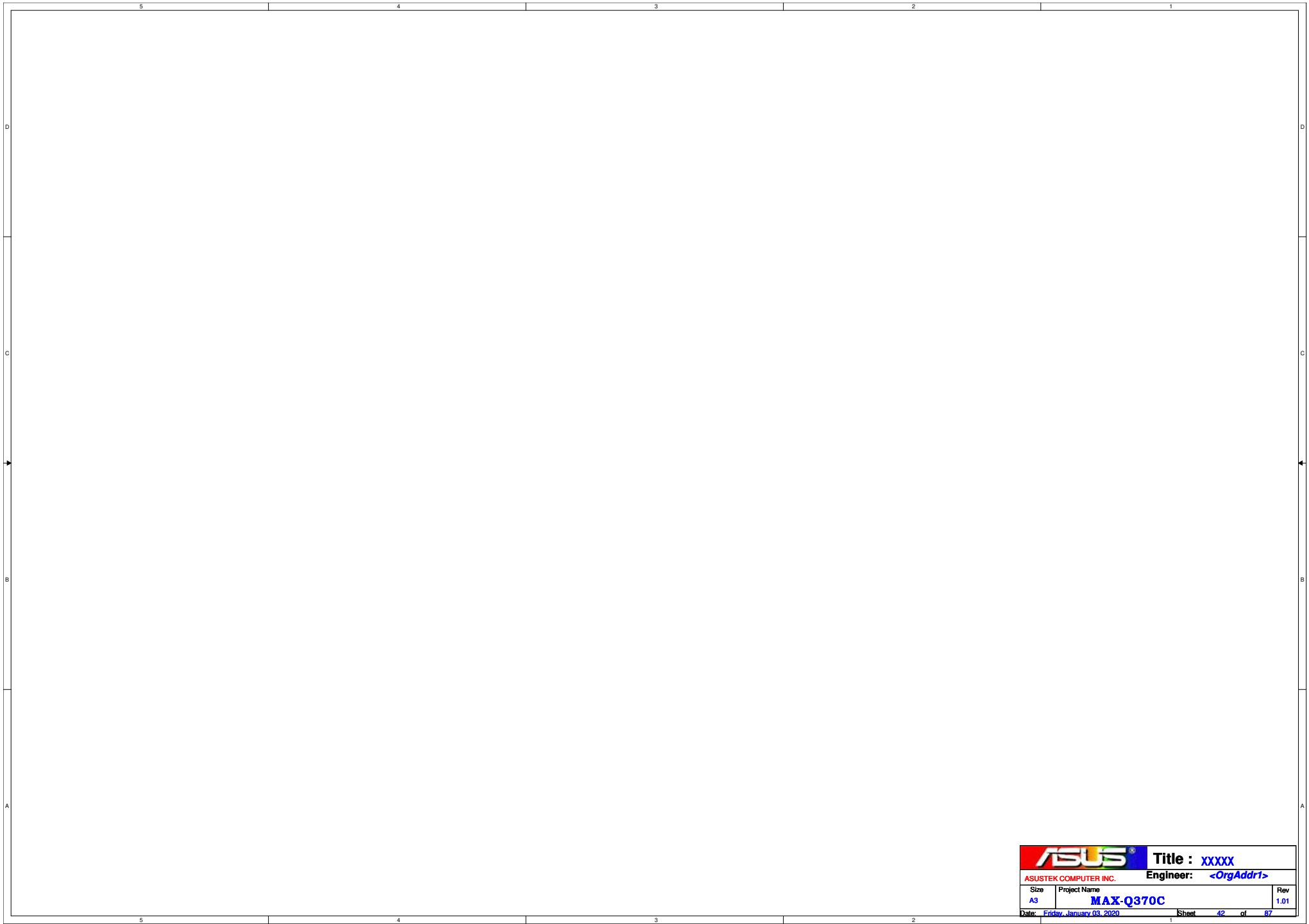
To avoid POP sound when PWR ON

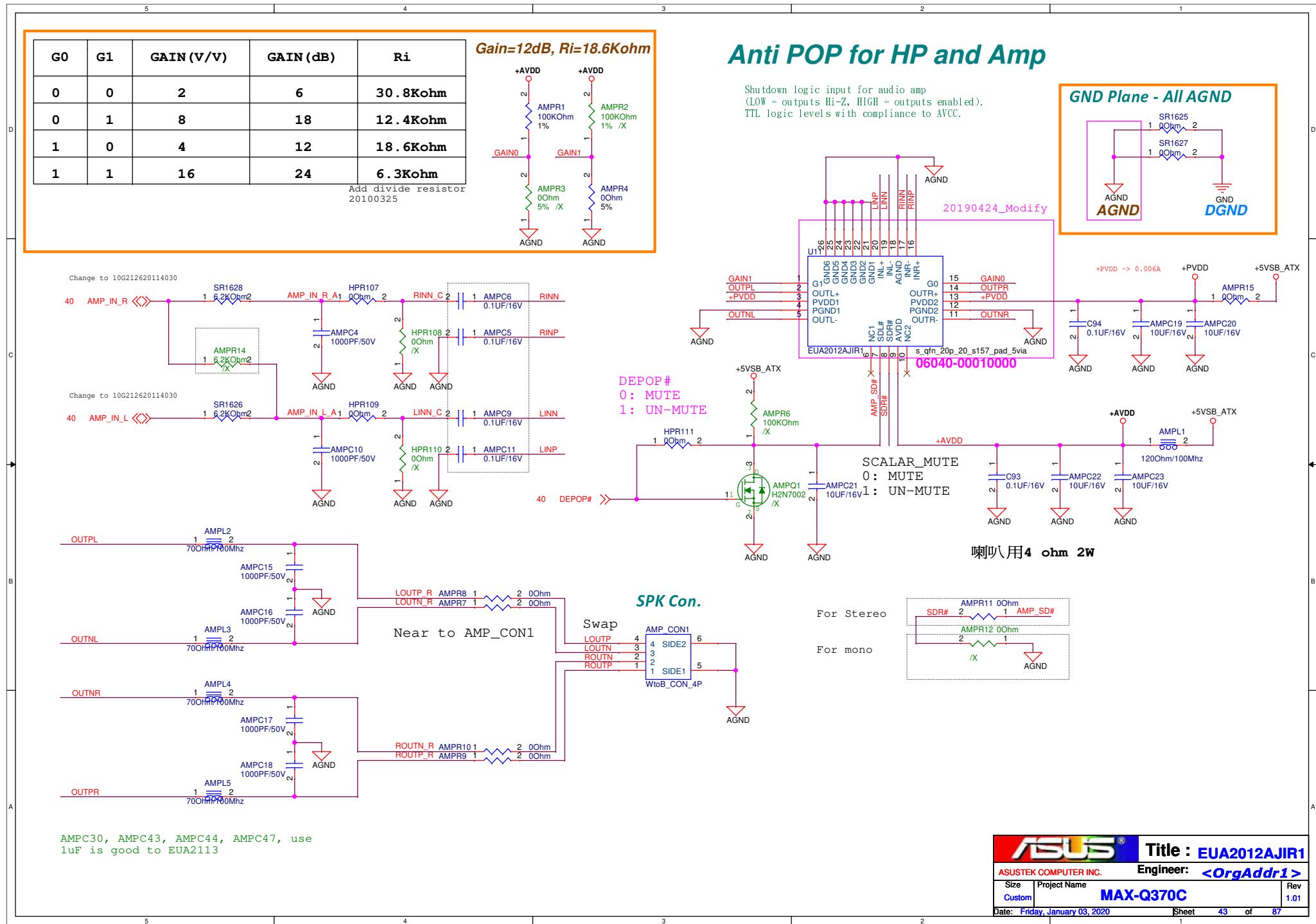


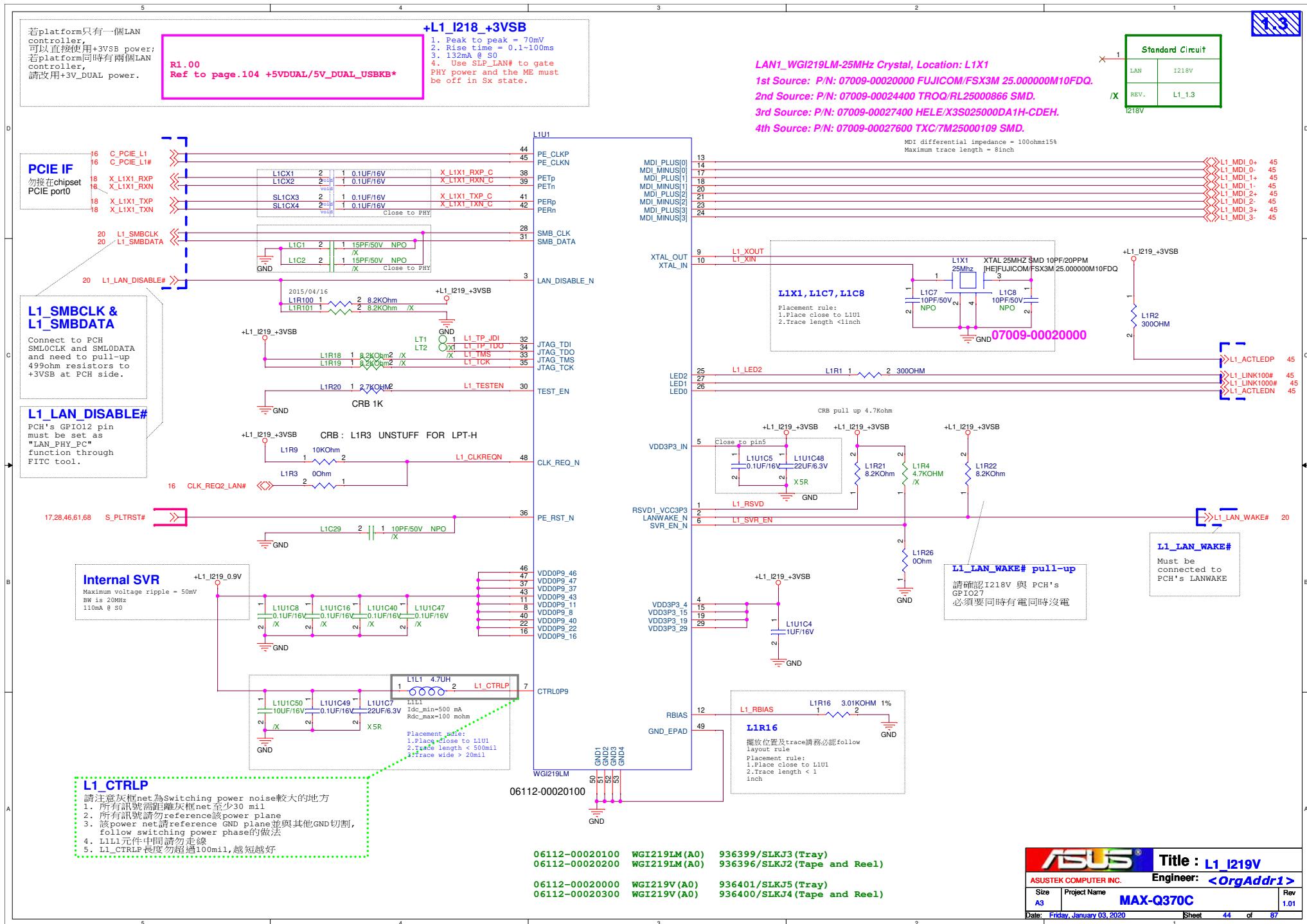
20190402_FAE Suggest

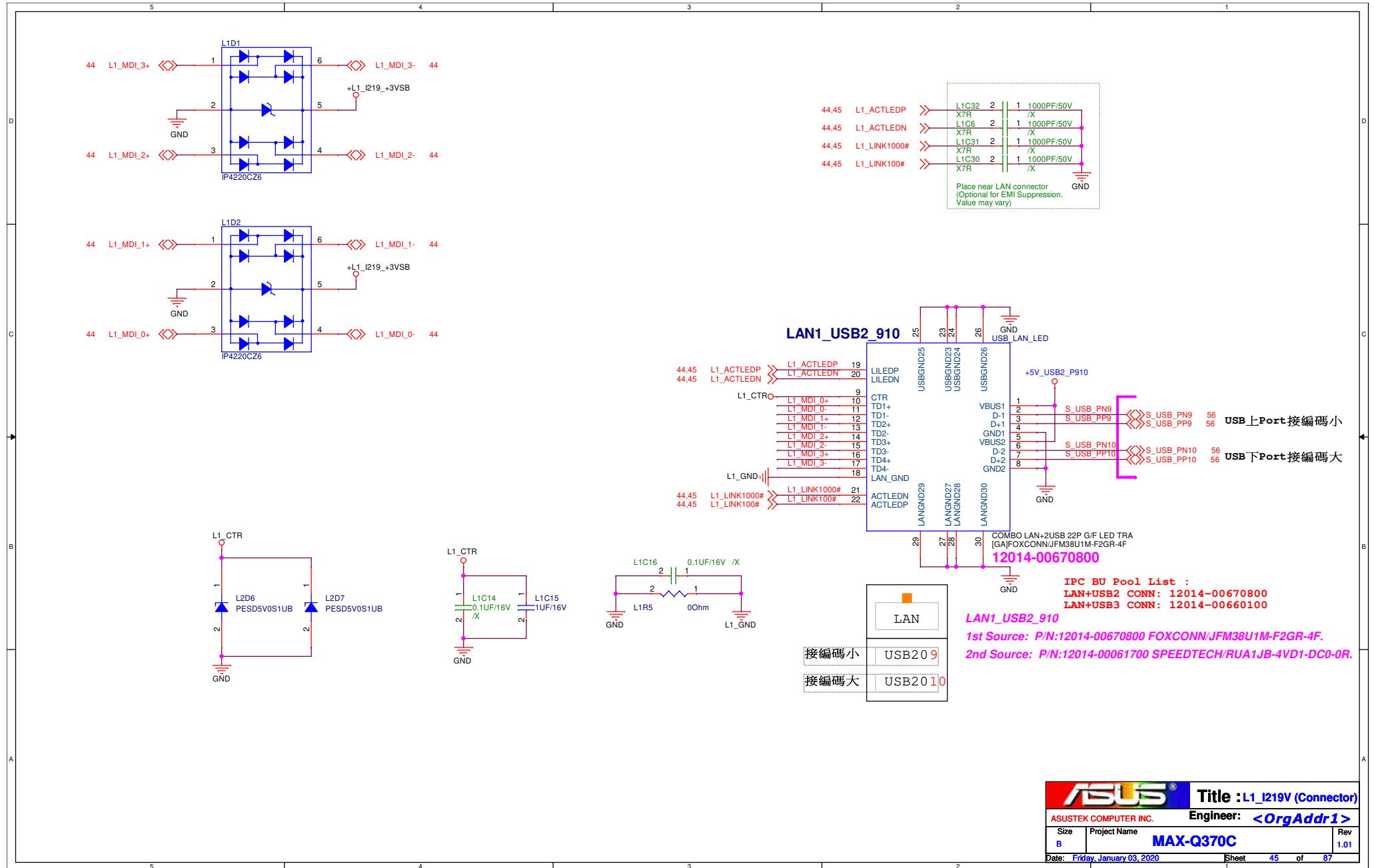


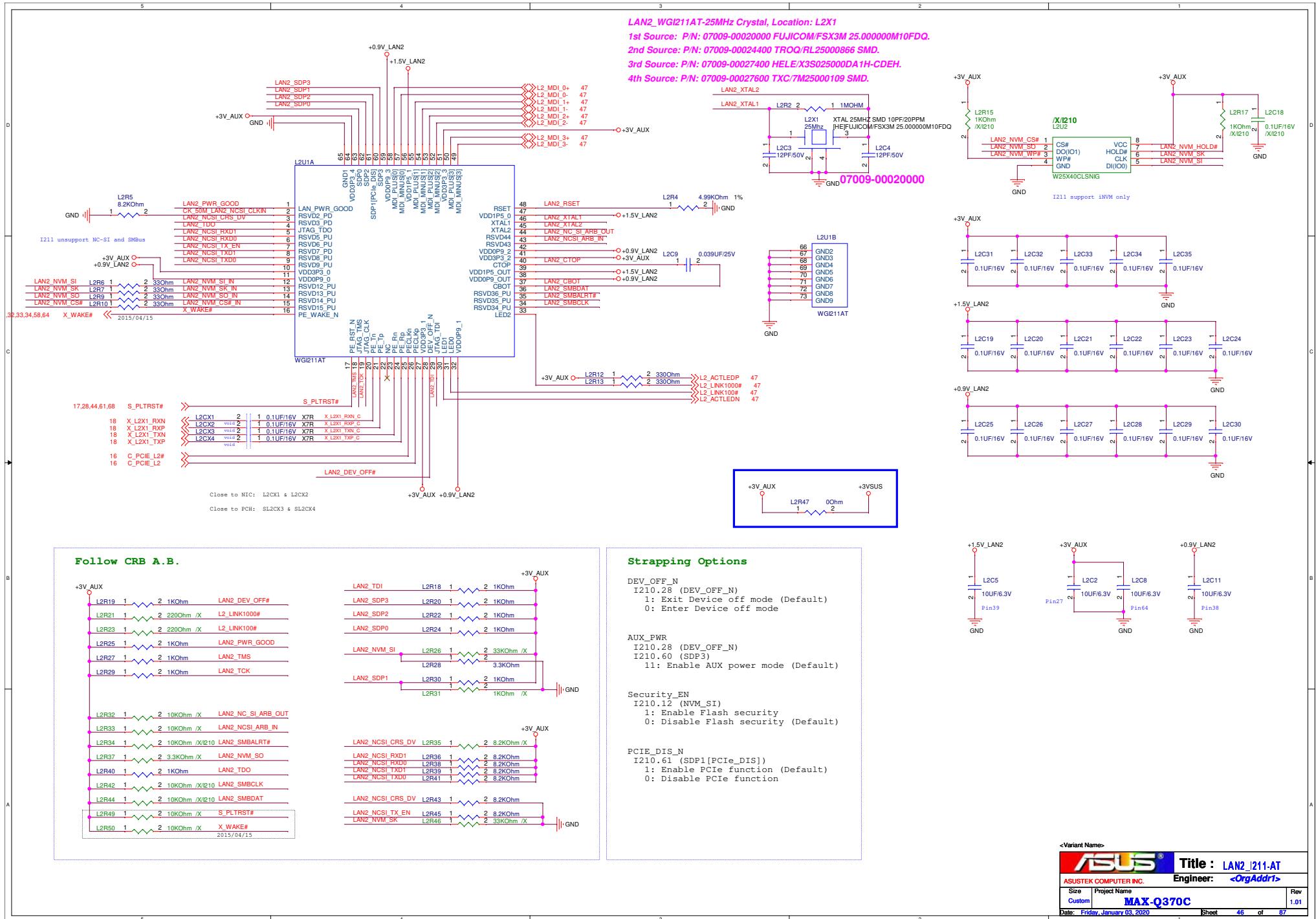


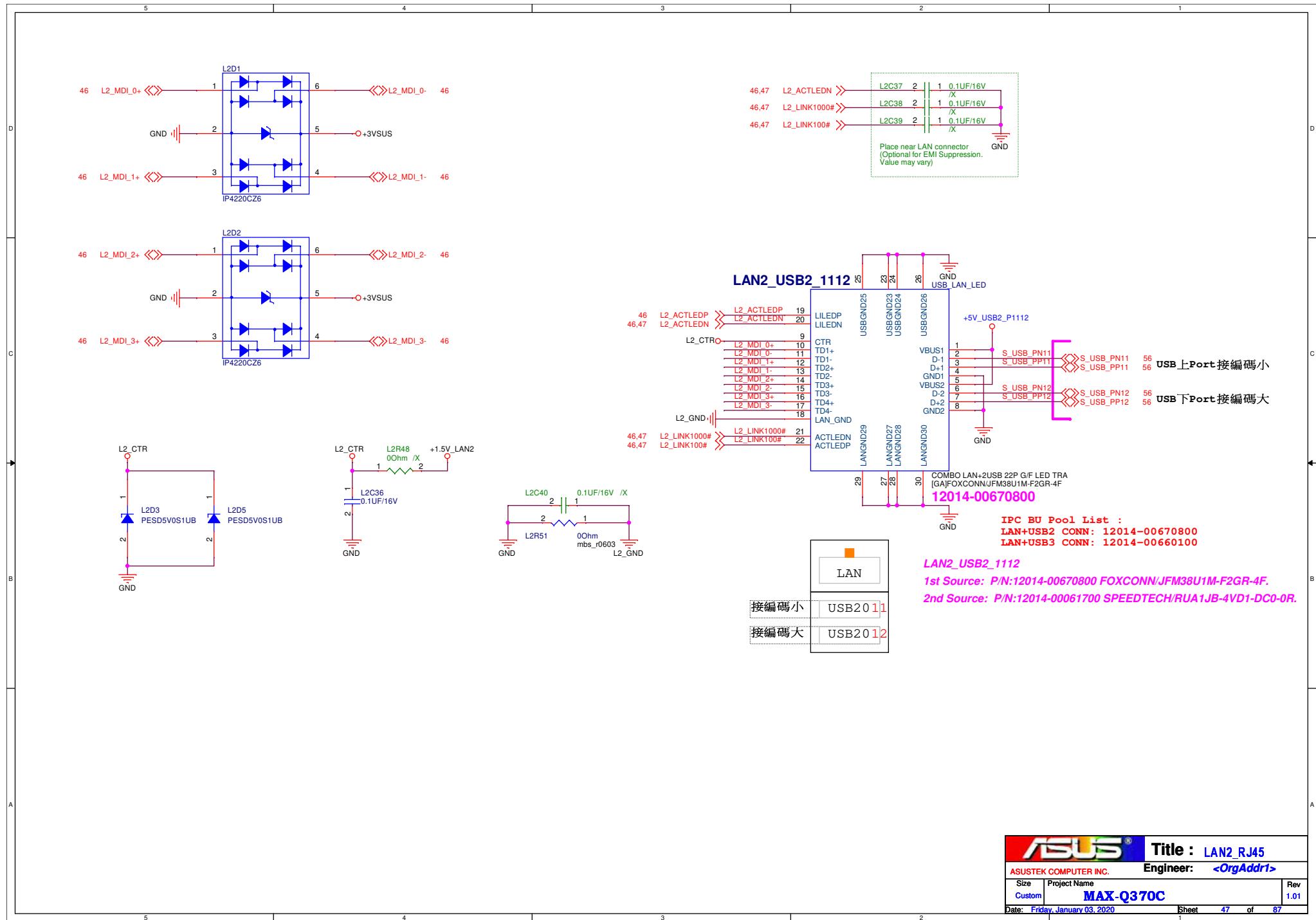












D

D

C

C

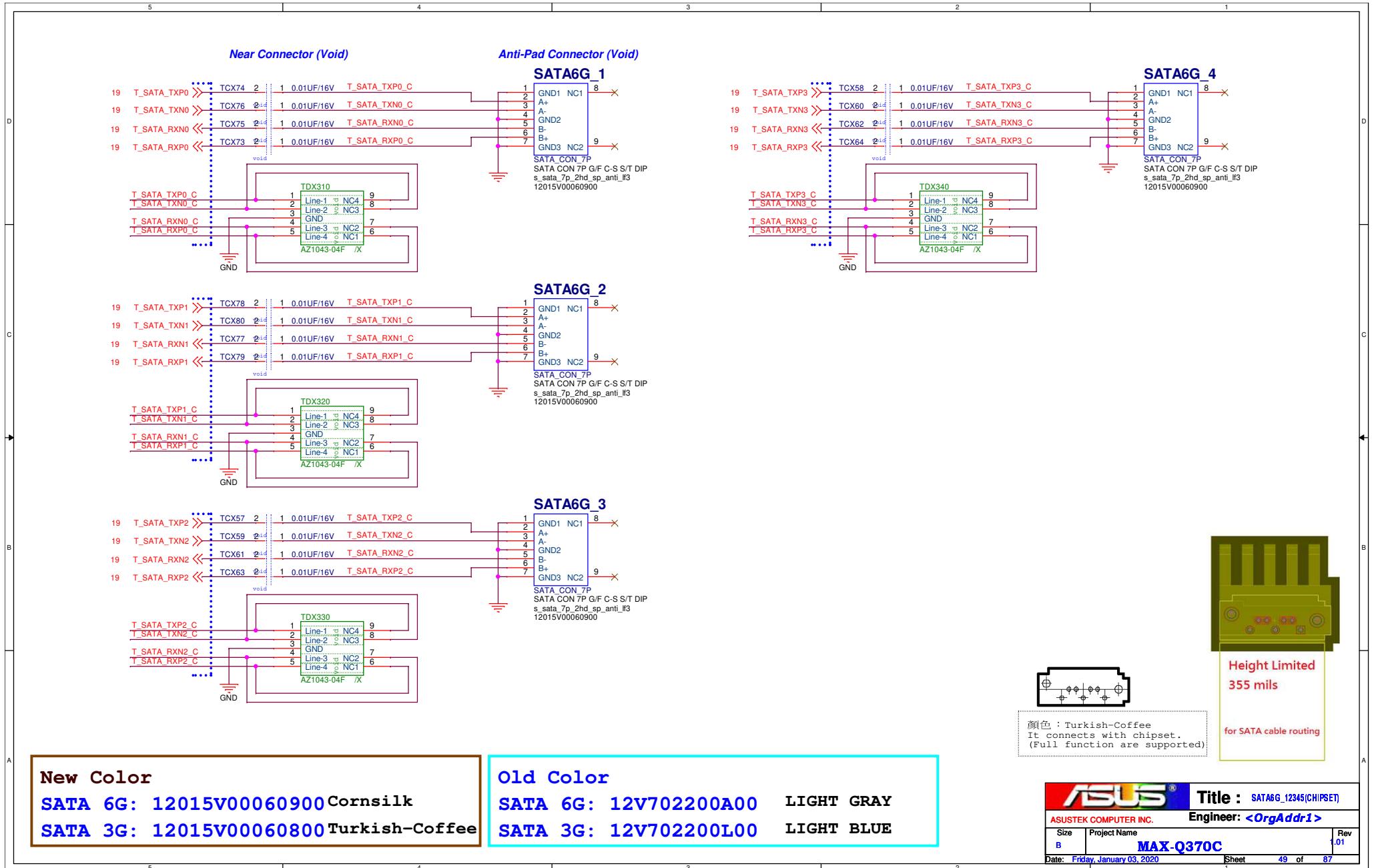
B

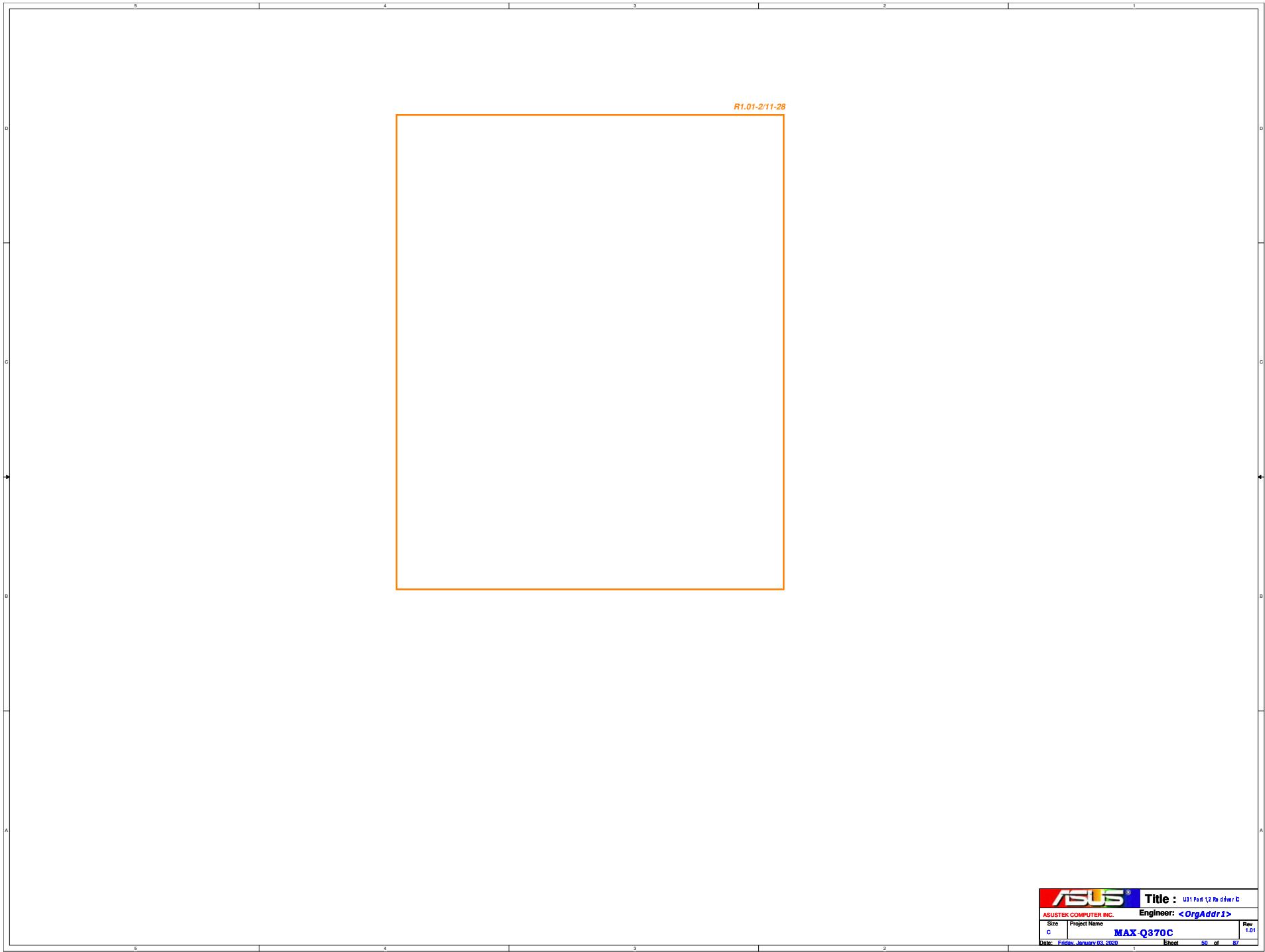
B

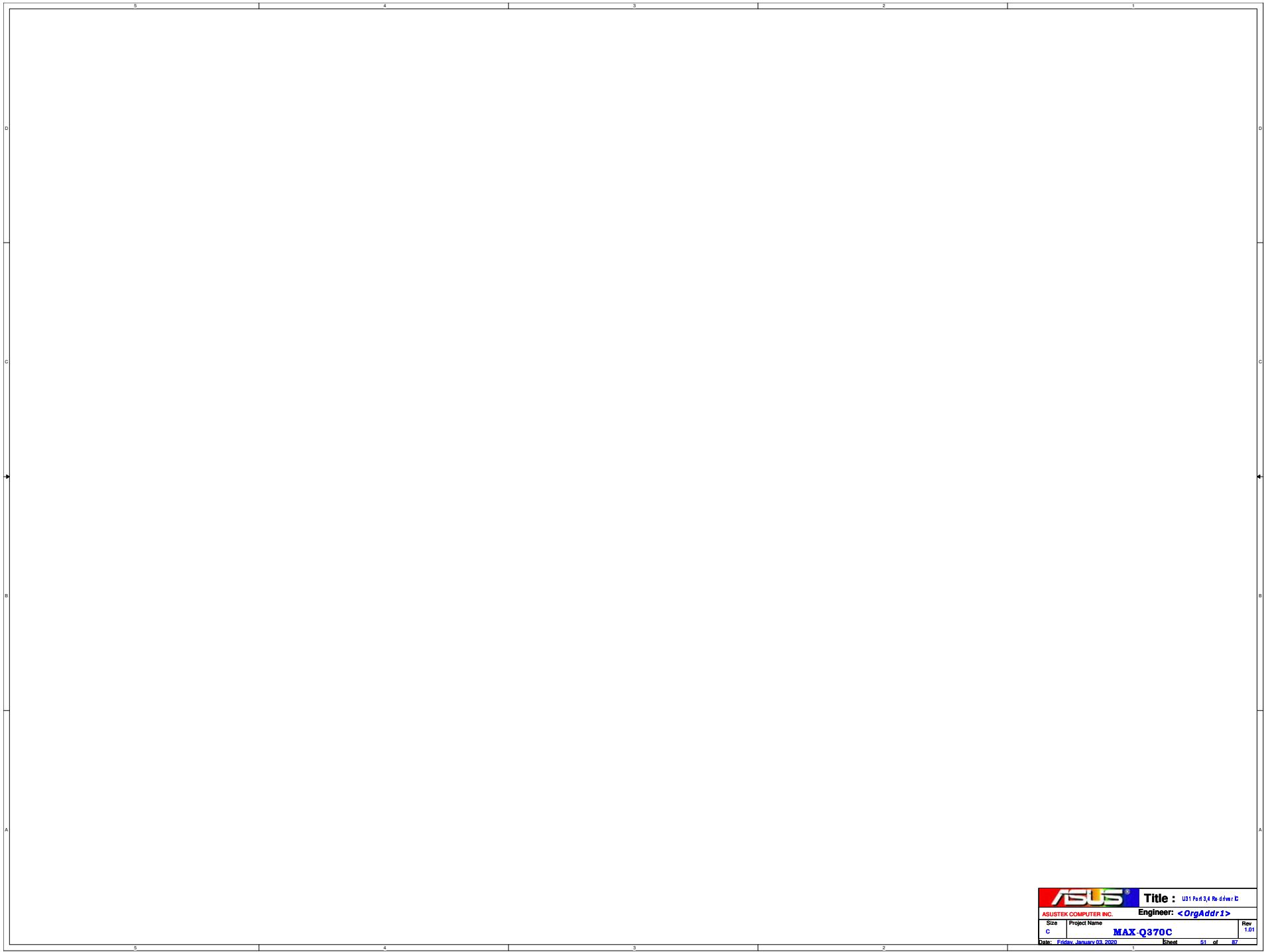
A

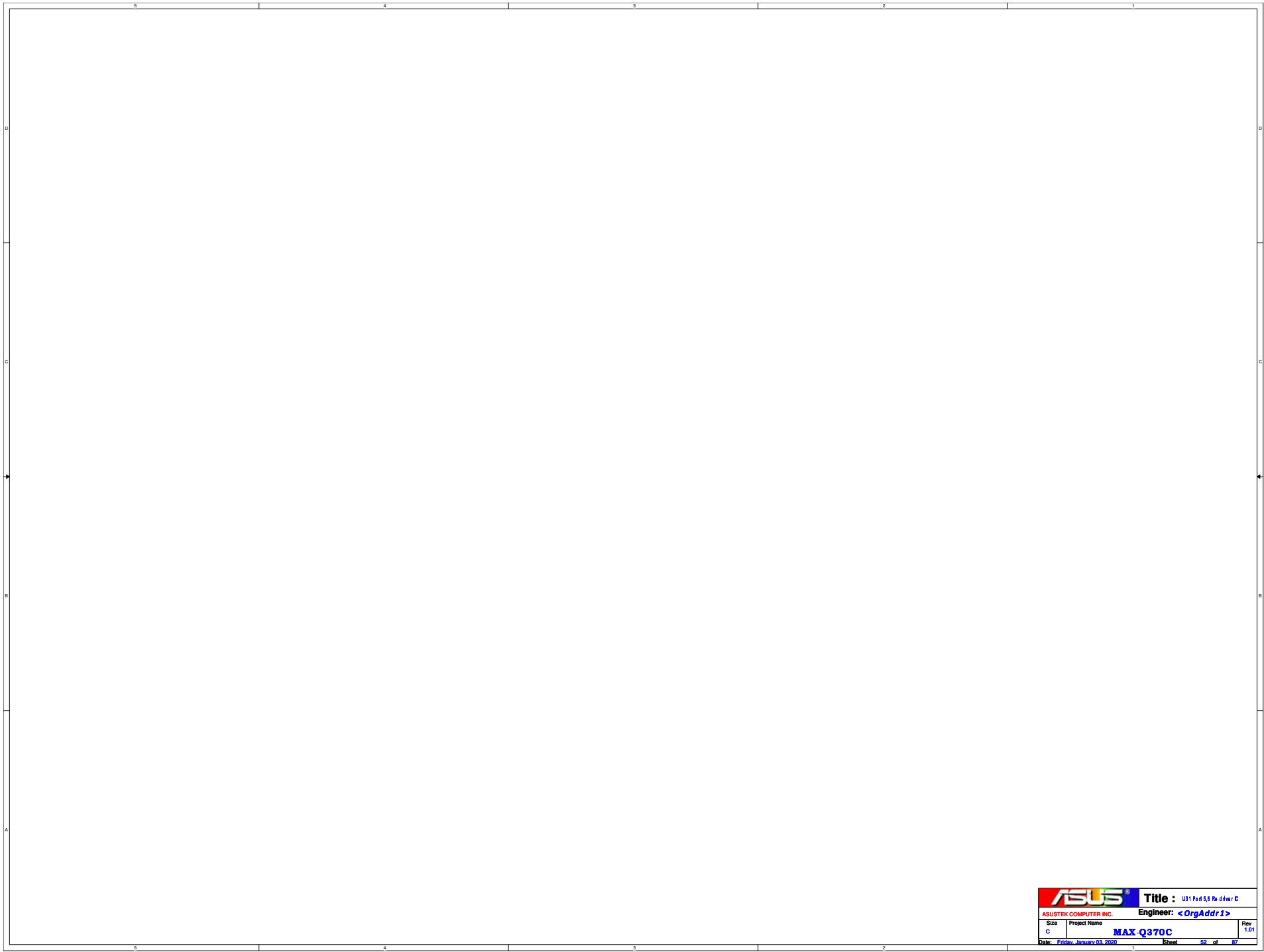
A

 Title : XXXXX		
ASUSTEK COMPUTER INC. Engineer: <OrgAddr1>		
Size A	Project Name MAX-Q370C	Rev 1.01
Date: Friday, January 03, 2020	Sheet 48 of 87	

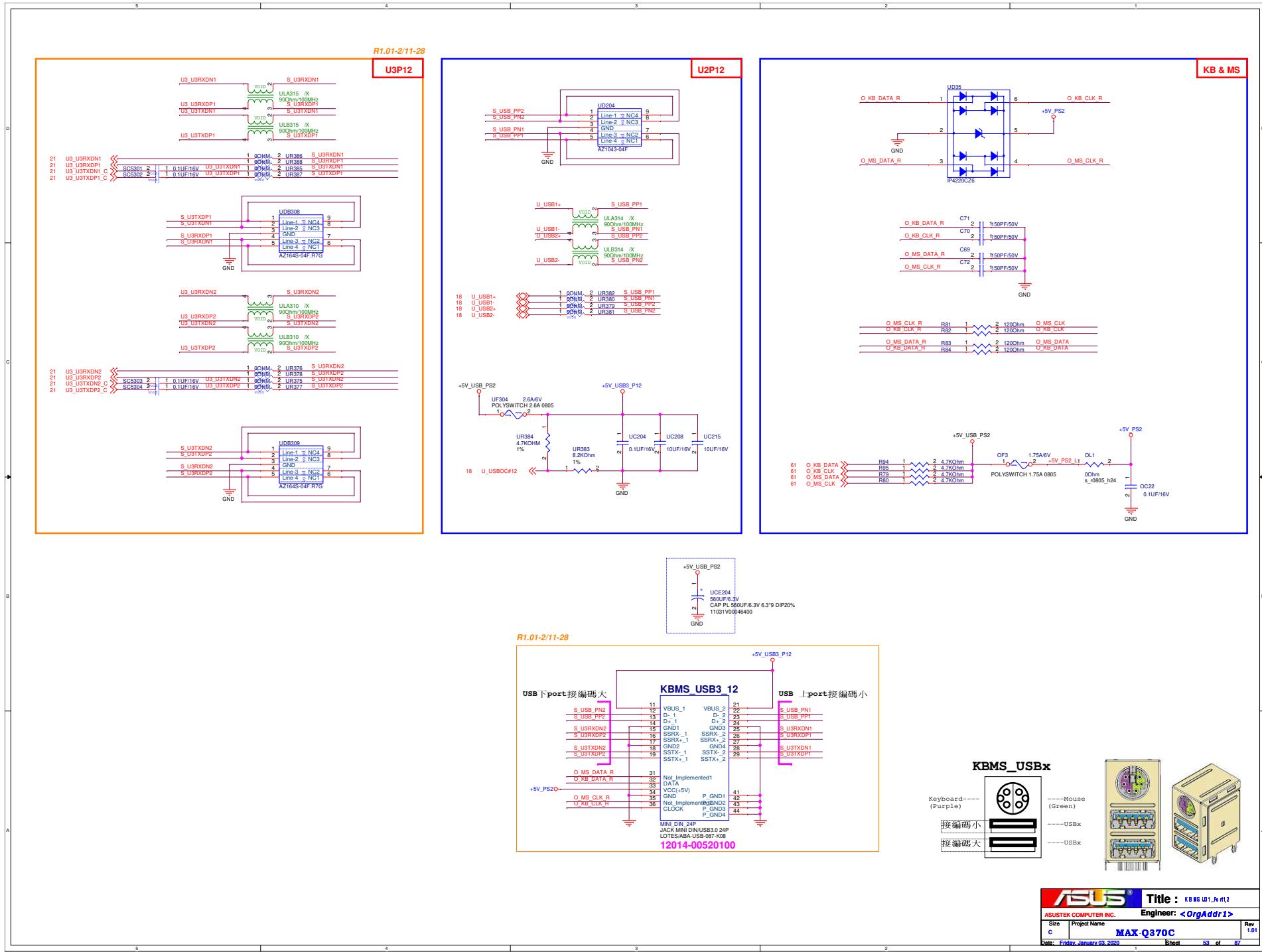


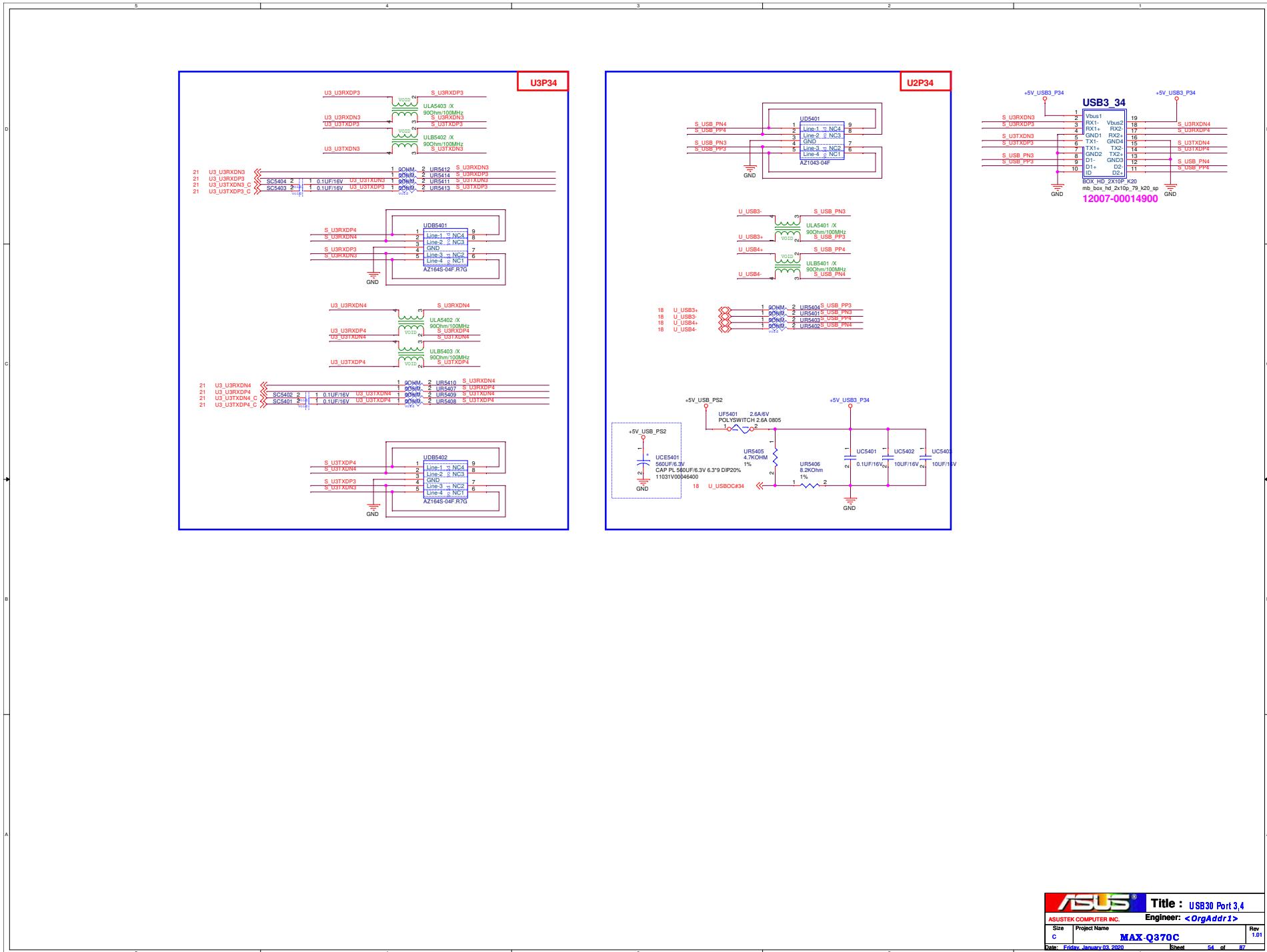


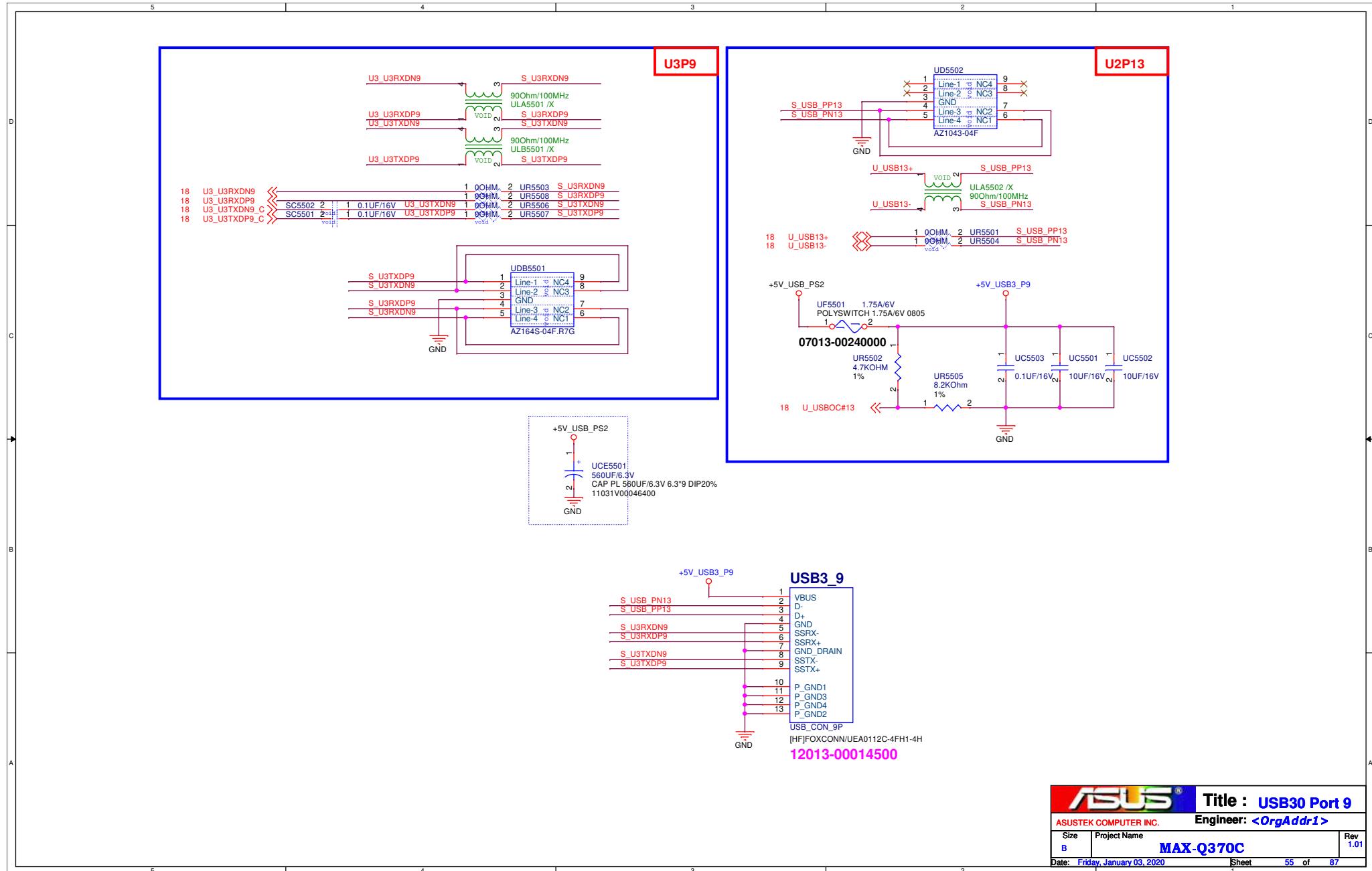


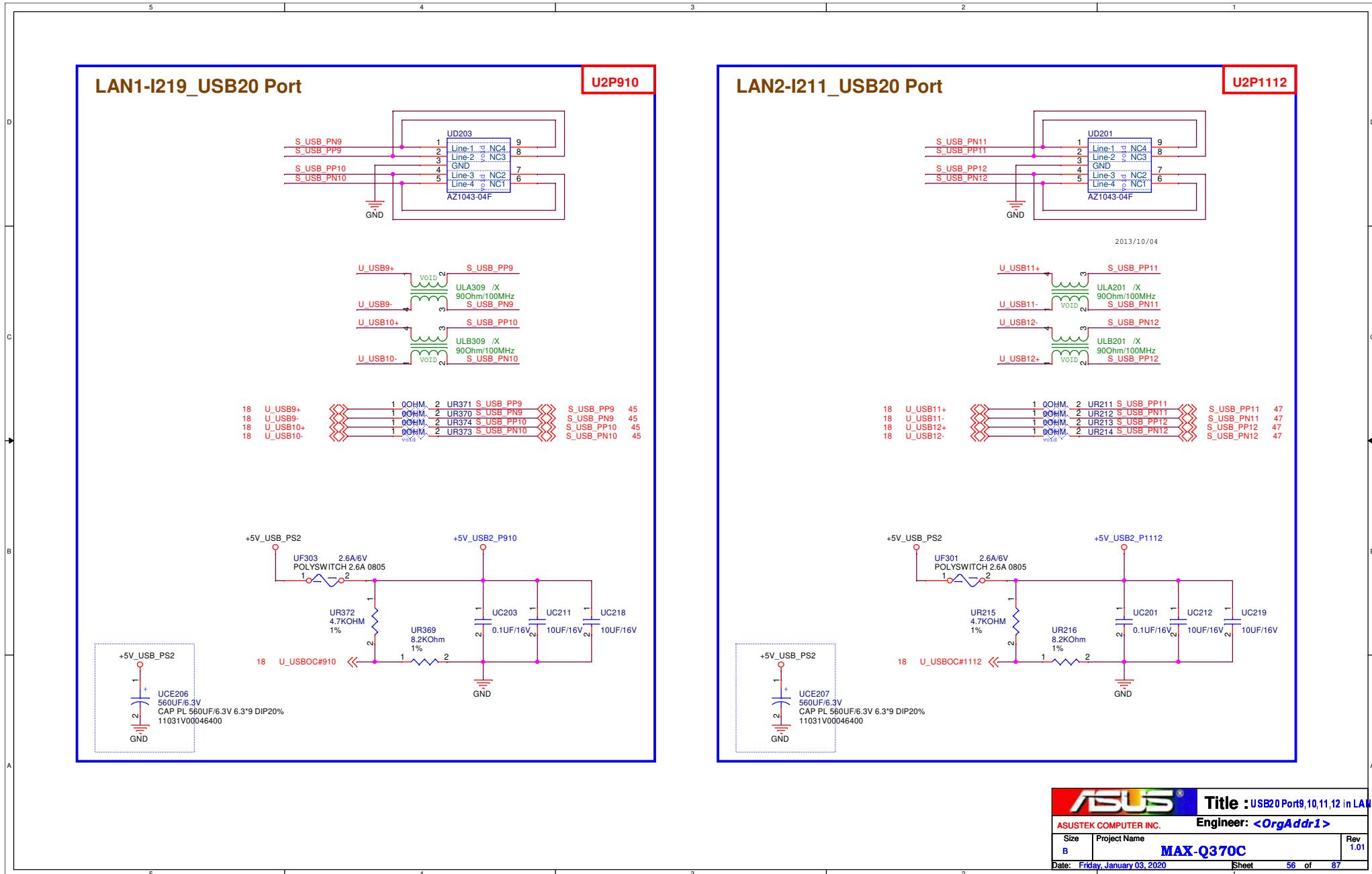


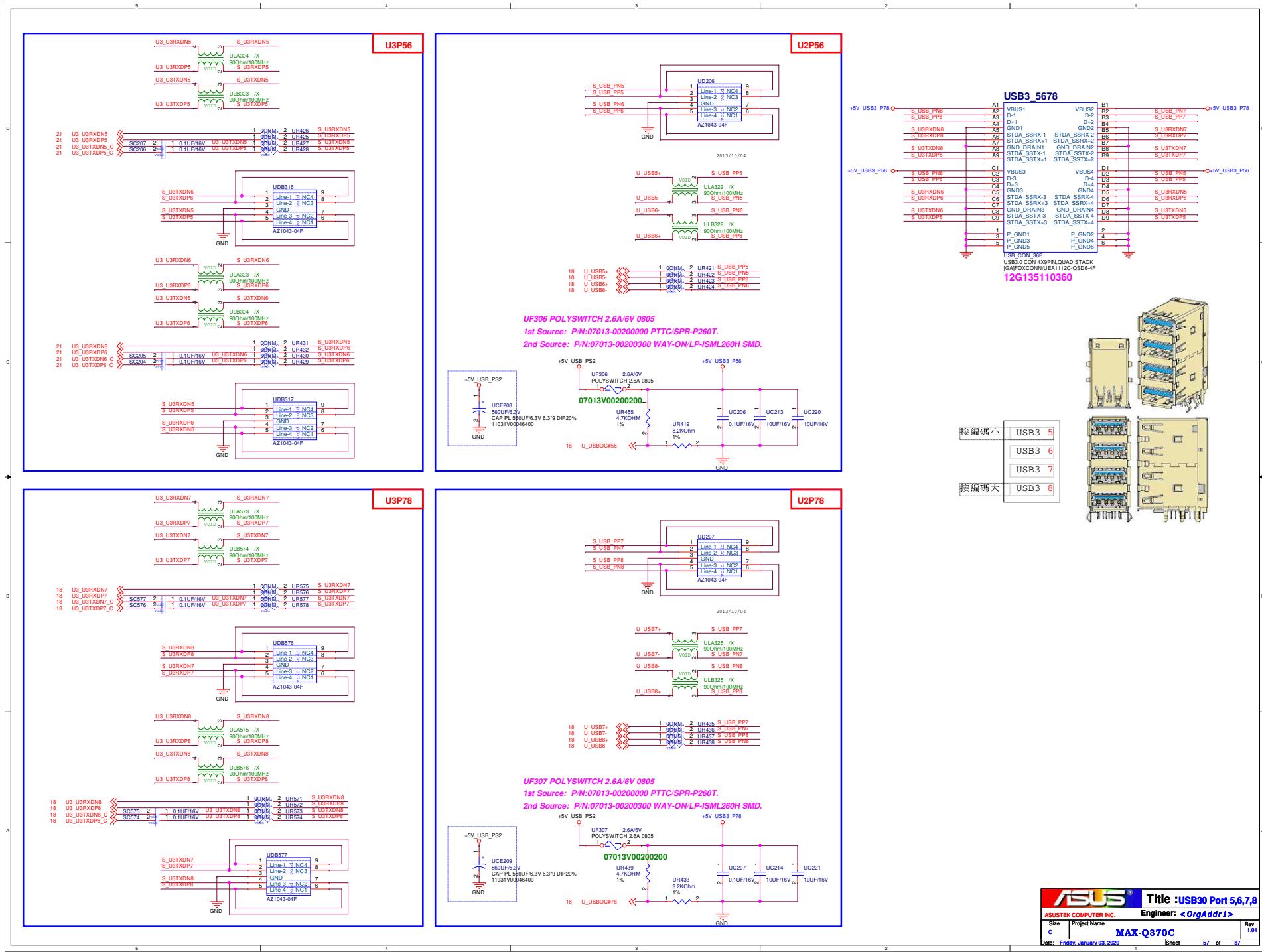
		Title : U31 Pad S,8 Re-draw v12	
ASUSTEK COMPUTER INC.		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
C	MAX-Q370C	1.01	











ASUS

Title :USB30 Port 5,6,7,8

Engineer: <OrgAddr1>

ASUSTEK COMPUTER INC.

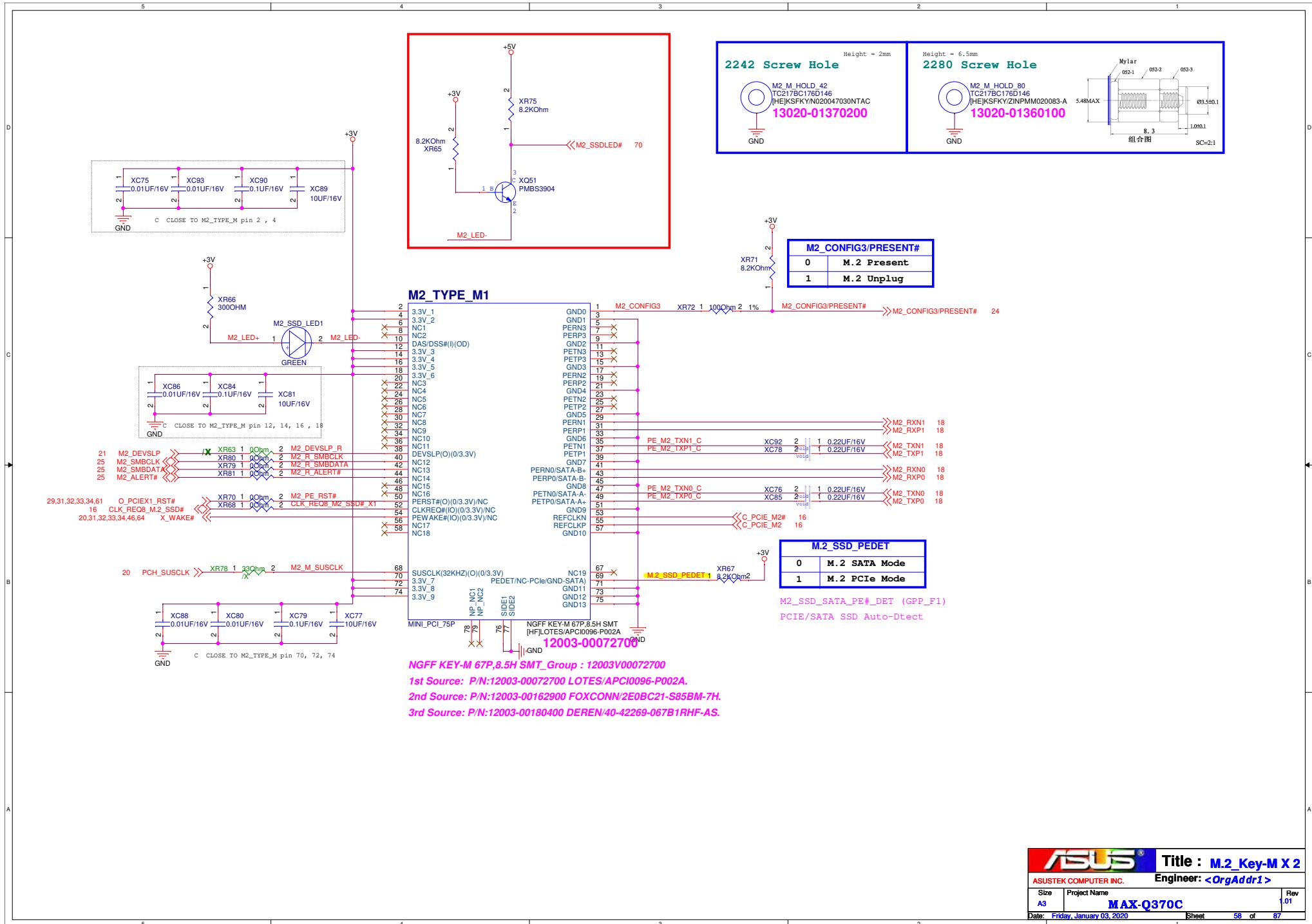
Size Project Name

c MAX-Q370C

Rev 1.01

Date: Friday, January 03, 2020

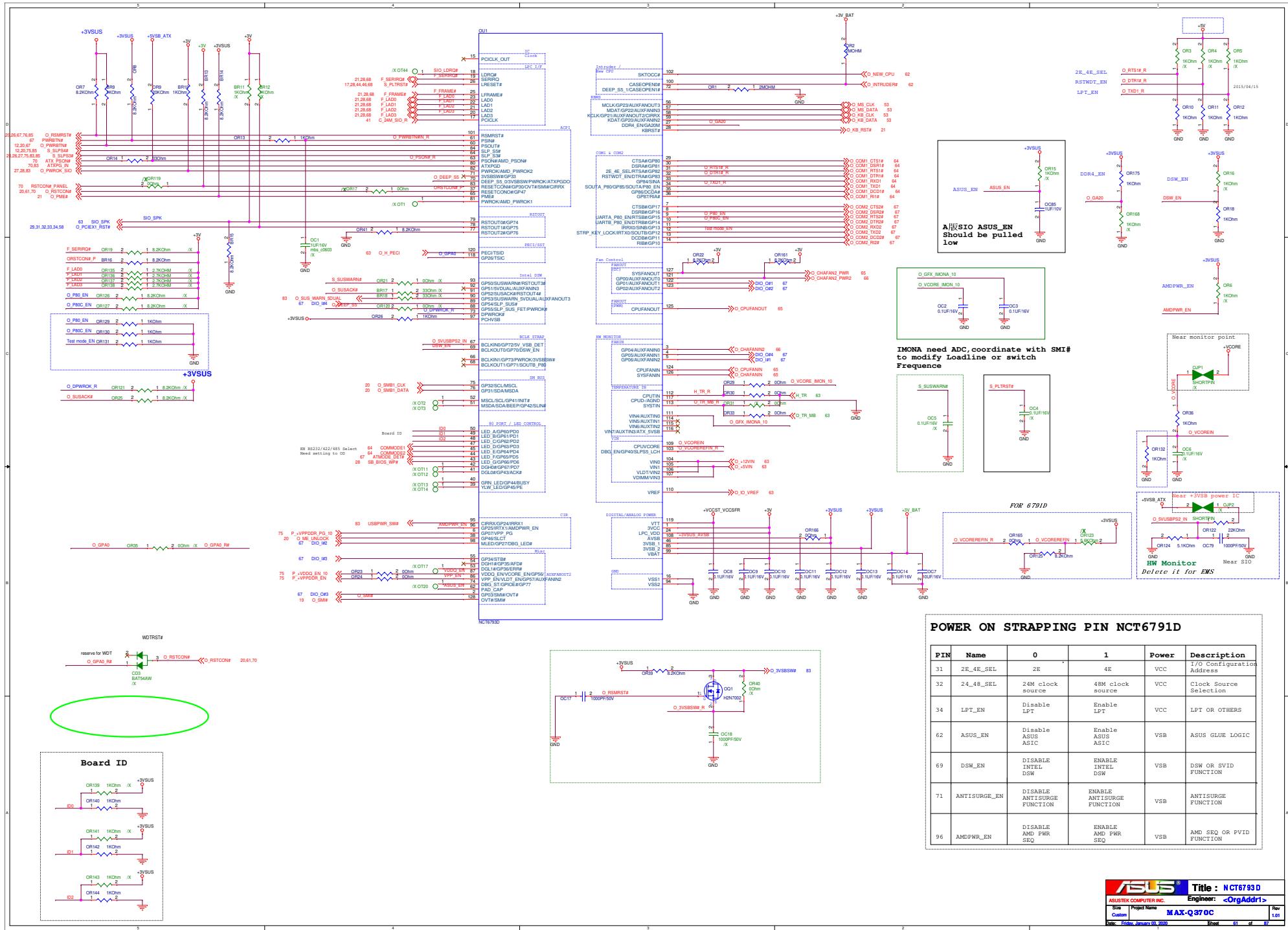
Sheet 57 of 87

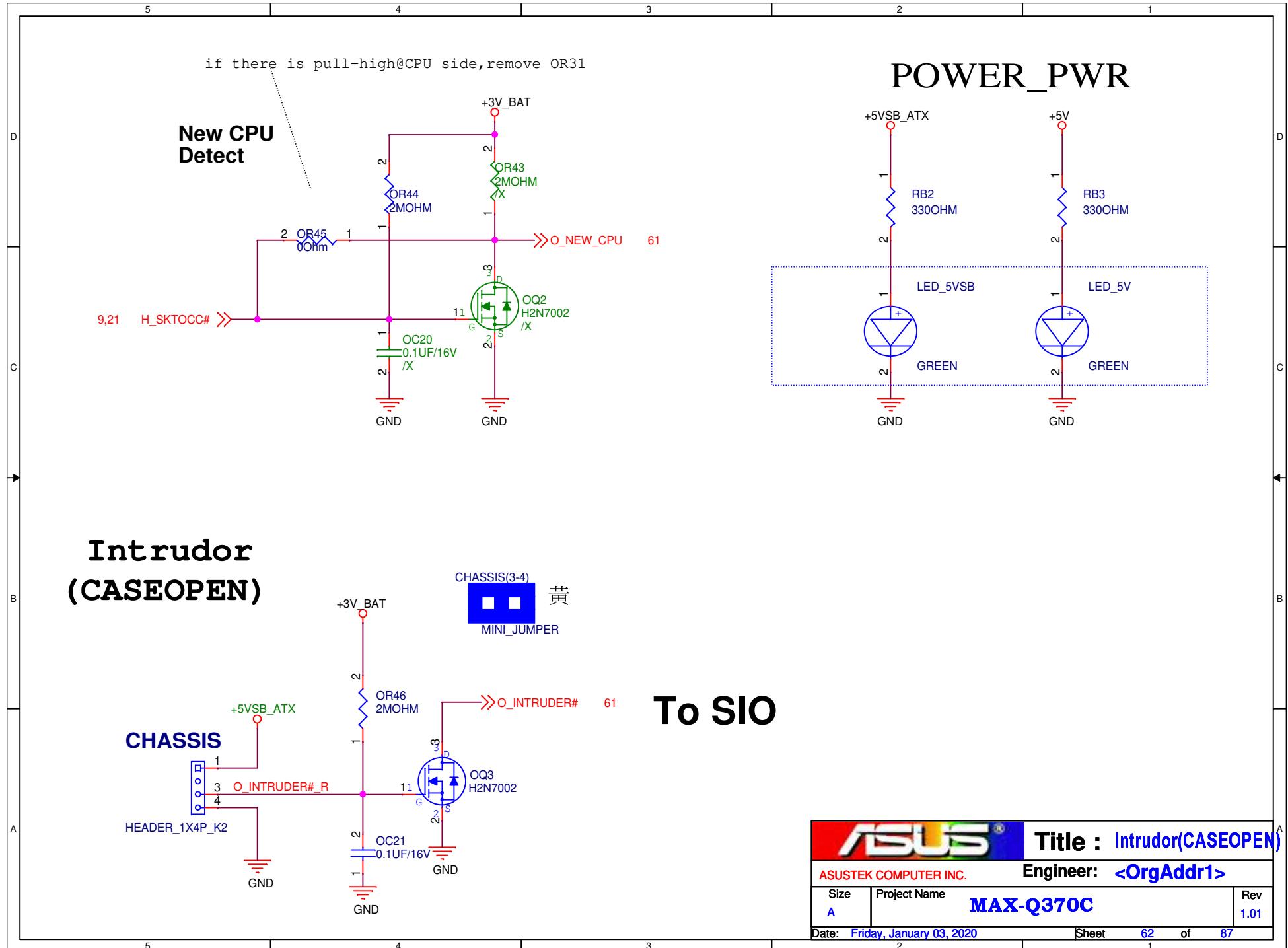


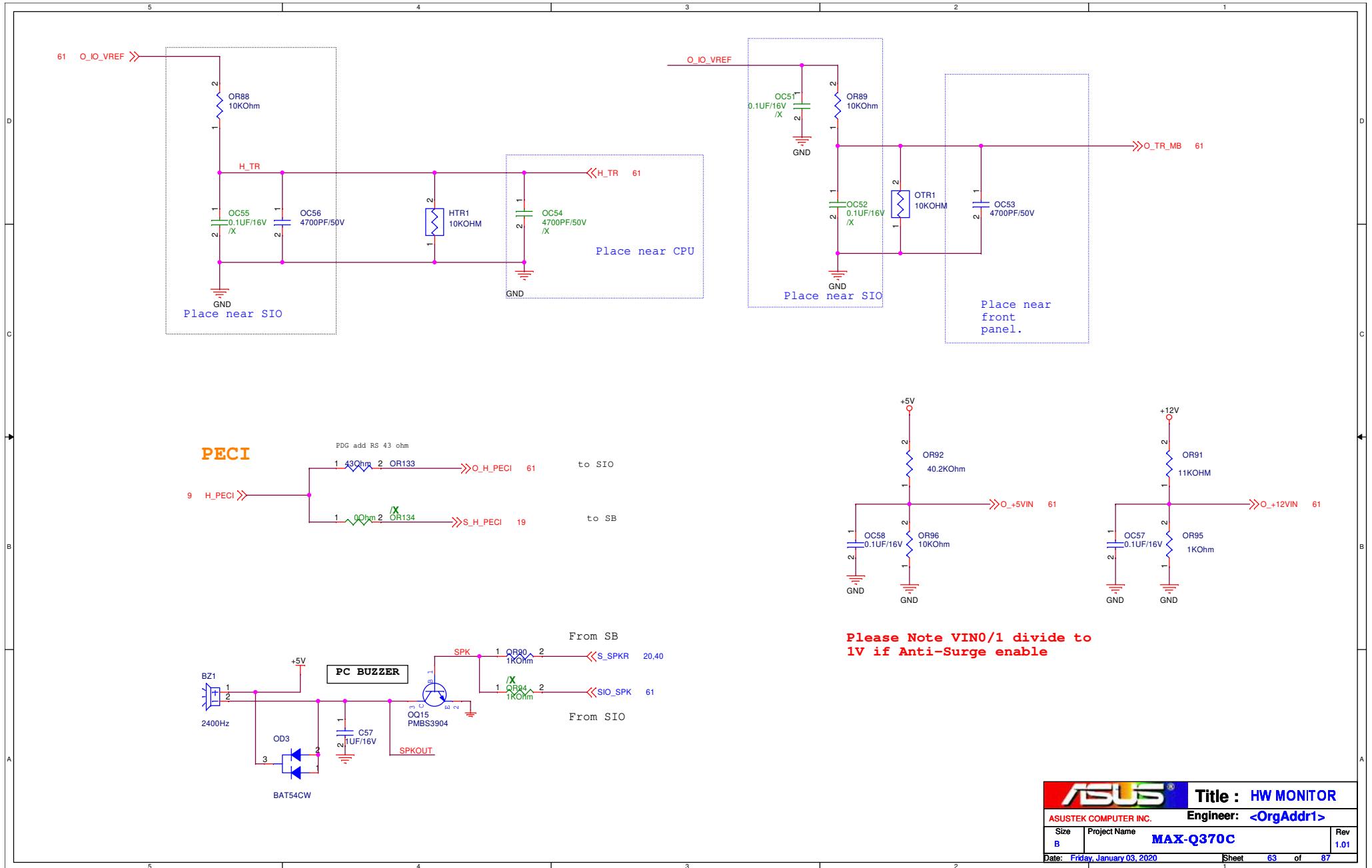




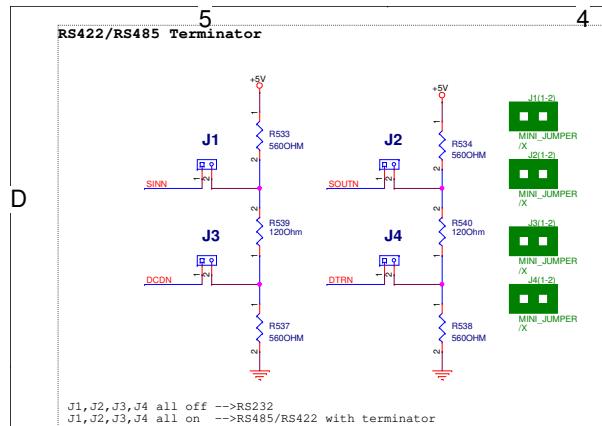
 ASUSTEK COMPUTER INC.		Title : XXXX	Engineer: <OrgAddr1>
Size B	Project Name MAX-Q370C	Rev 1.01	
Date: Friday, January 03, 2020	Sheet 60	of 87	







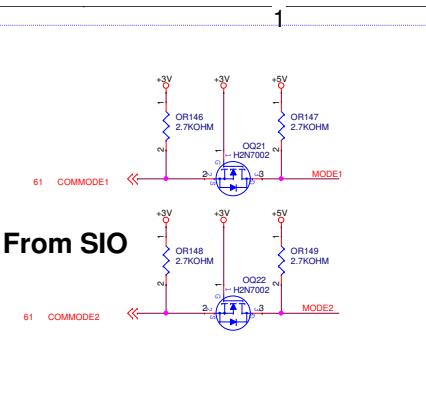
ASUS		Title : HW MONITOR
ASUSTEK COMPUTER INC.	Engineer: <OrgAddr1>	
Size B	Project Name MAX-Q370C	Rev 1.01
Date: Friday, January 03, 2020	Sheet 63 of 87	



Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

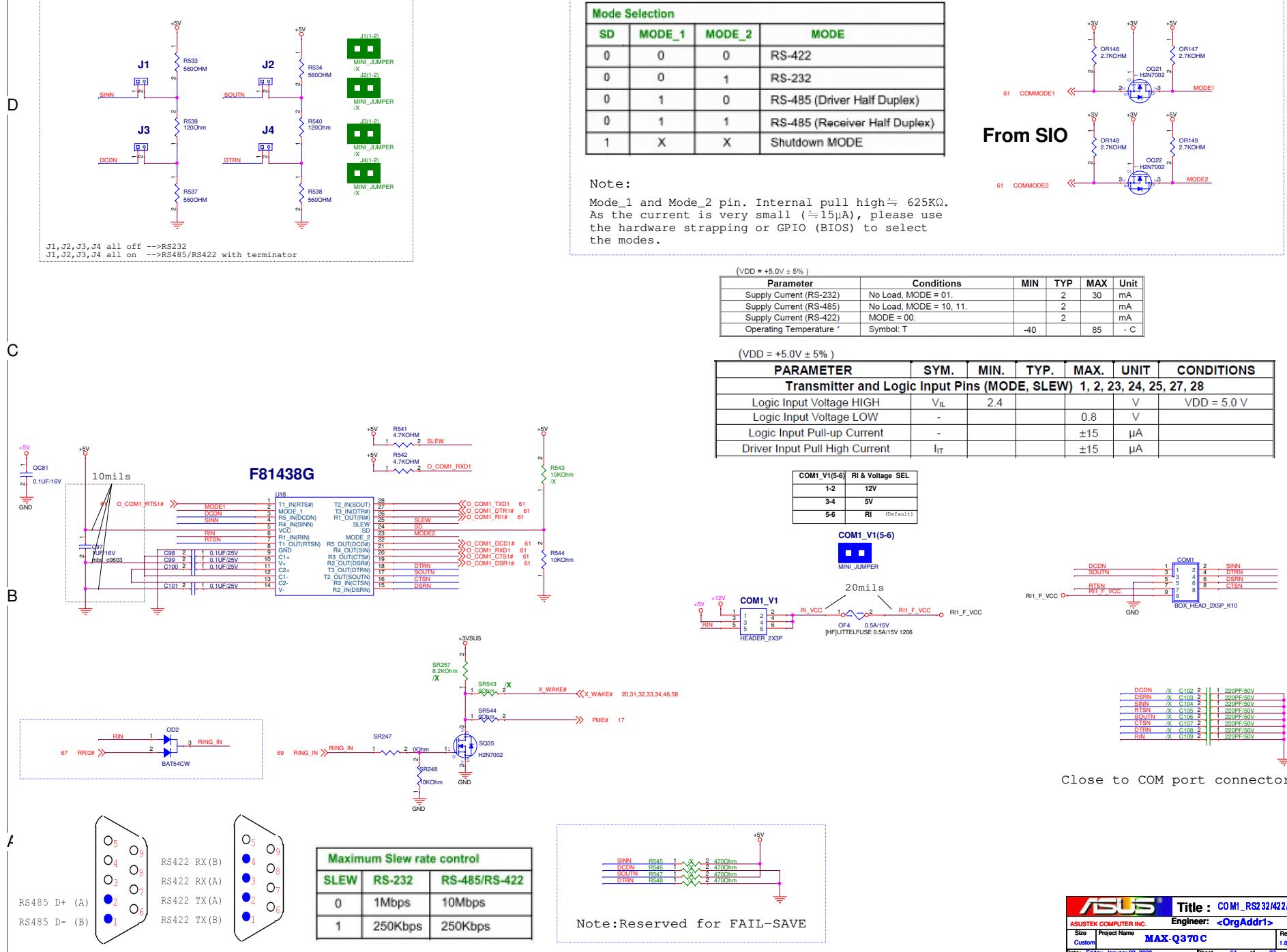
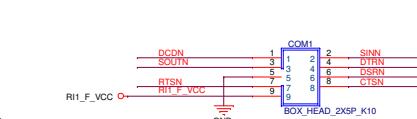
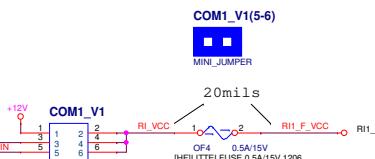
Mode_1 and Mode_2 pin. Internal pull high = 625KΩ. As the current is very small ($\approx 15\mu A$), please use the hardware strapping or GPIO (BIOS) to select the modes.

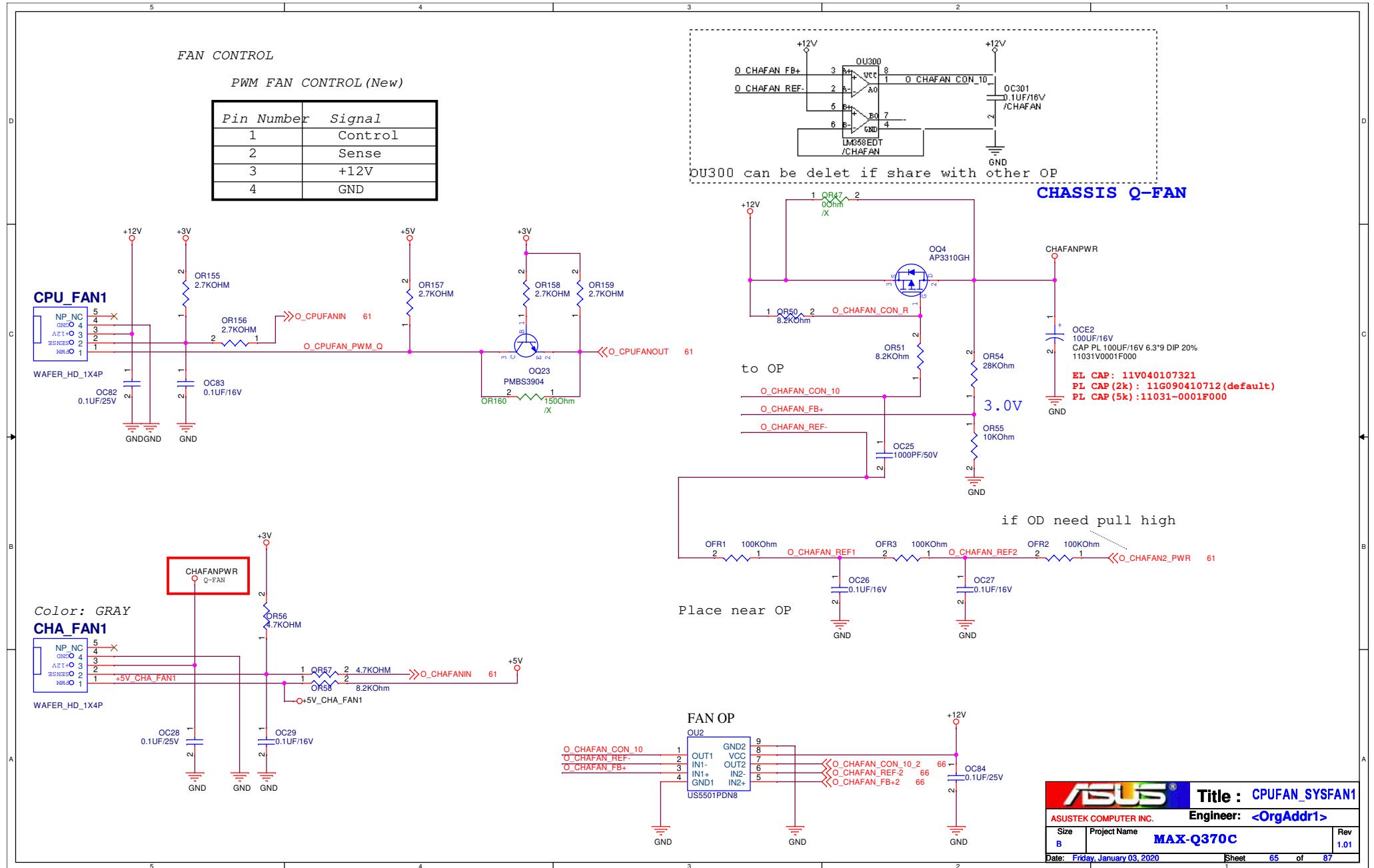


(VDD = +5.0V ± 5%)					
Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01,	2	30	mA	
Supply Current (RS-485)	No Load, MODE = 10, 11.	2	2	mA	
Supply Current (RS-422)	MODE = 00.	2	2	mA	
Operating Temperature *	Symbol: T	-40	85	° C	

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V _{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-	-	-	0.8	V	
Logic Input Pull-up Current	-	-	-	±15	μA	
Driver Input Pull High Current	I _{IT}	-	-	±15	μA	

COM1_V1(5-6)	Ri & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

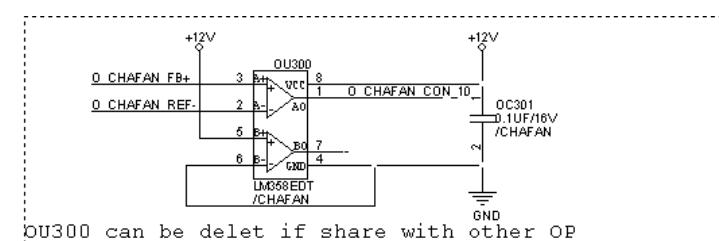
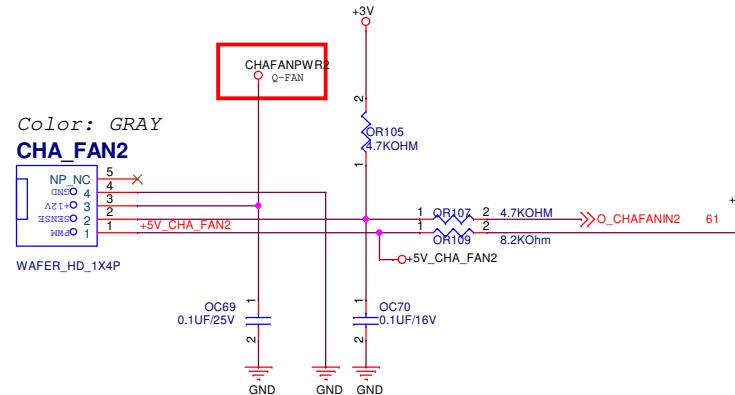




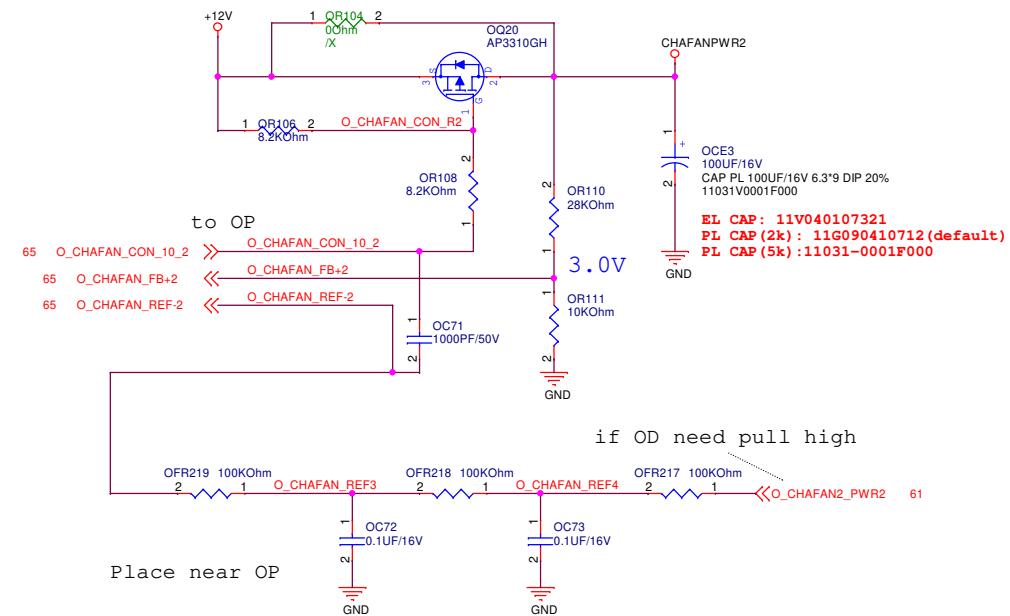
FAN CONTROL

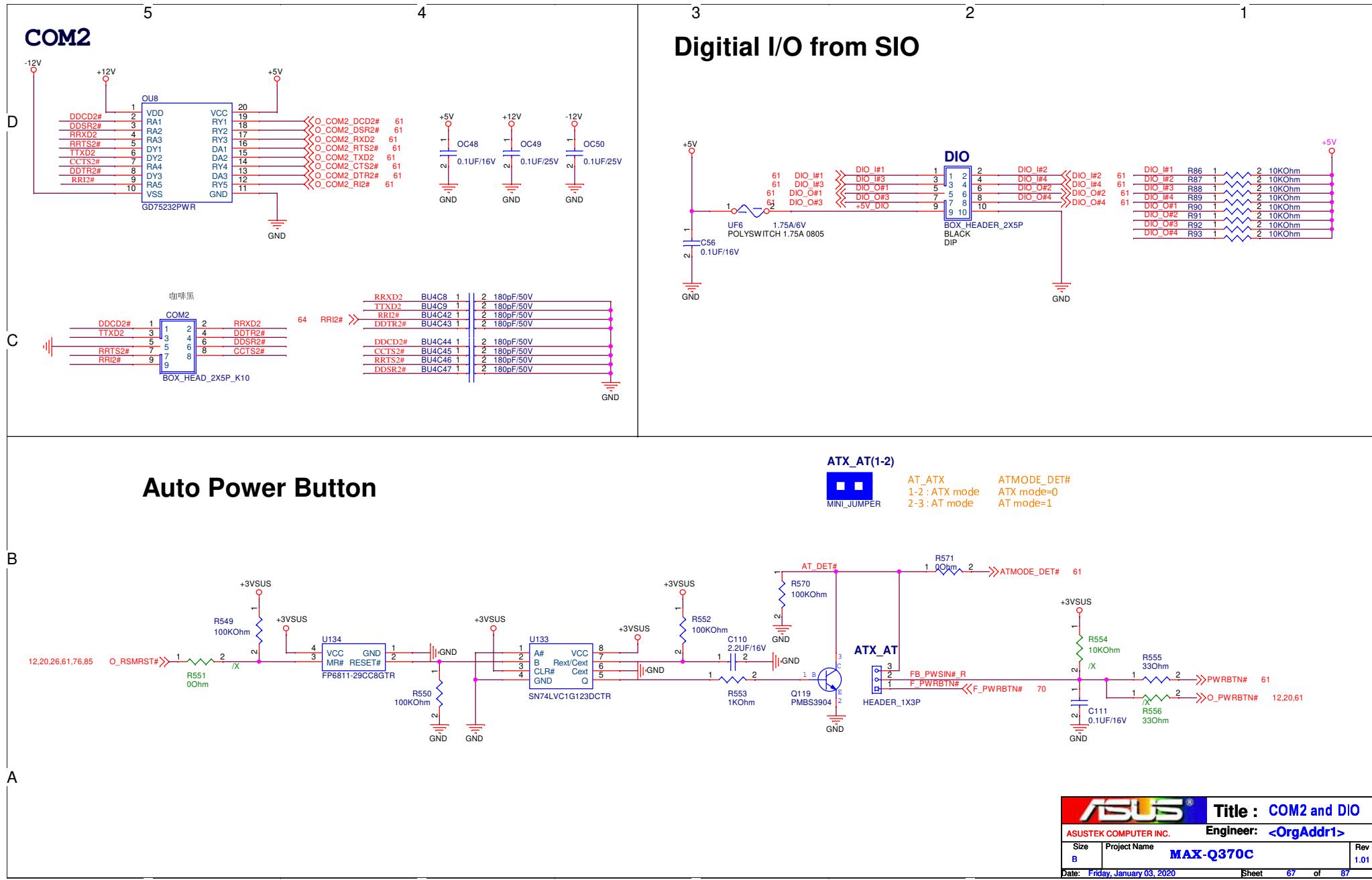
PWM FAN CONTROL (New)

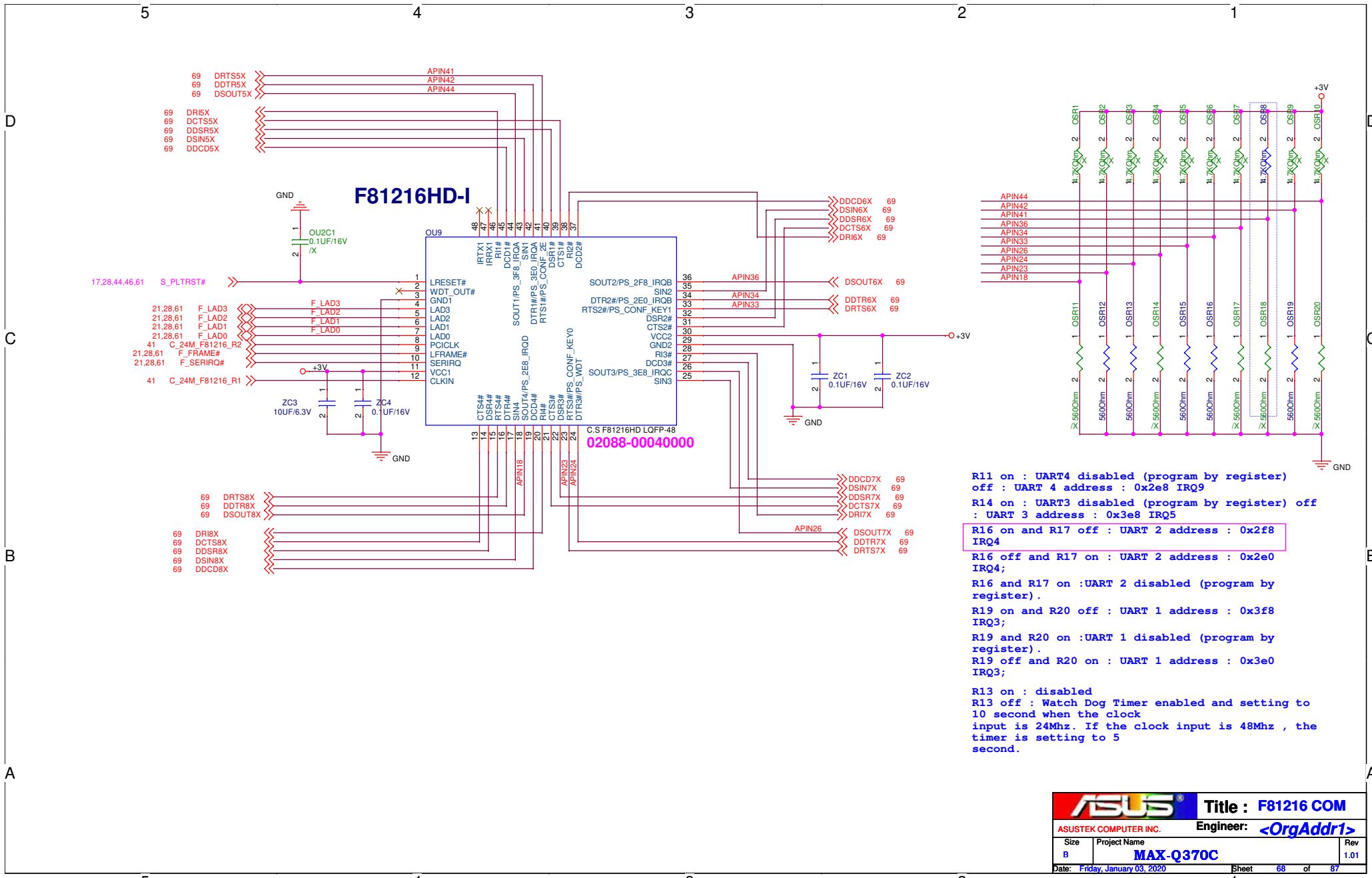
Pin Number	Signal
1	Control
2	Sense
3	+12V
4	GND

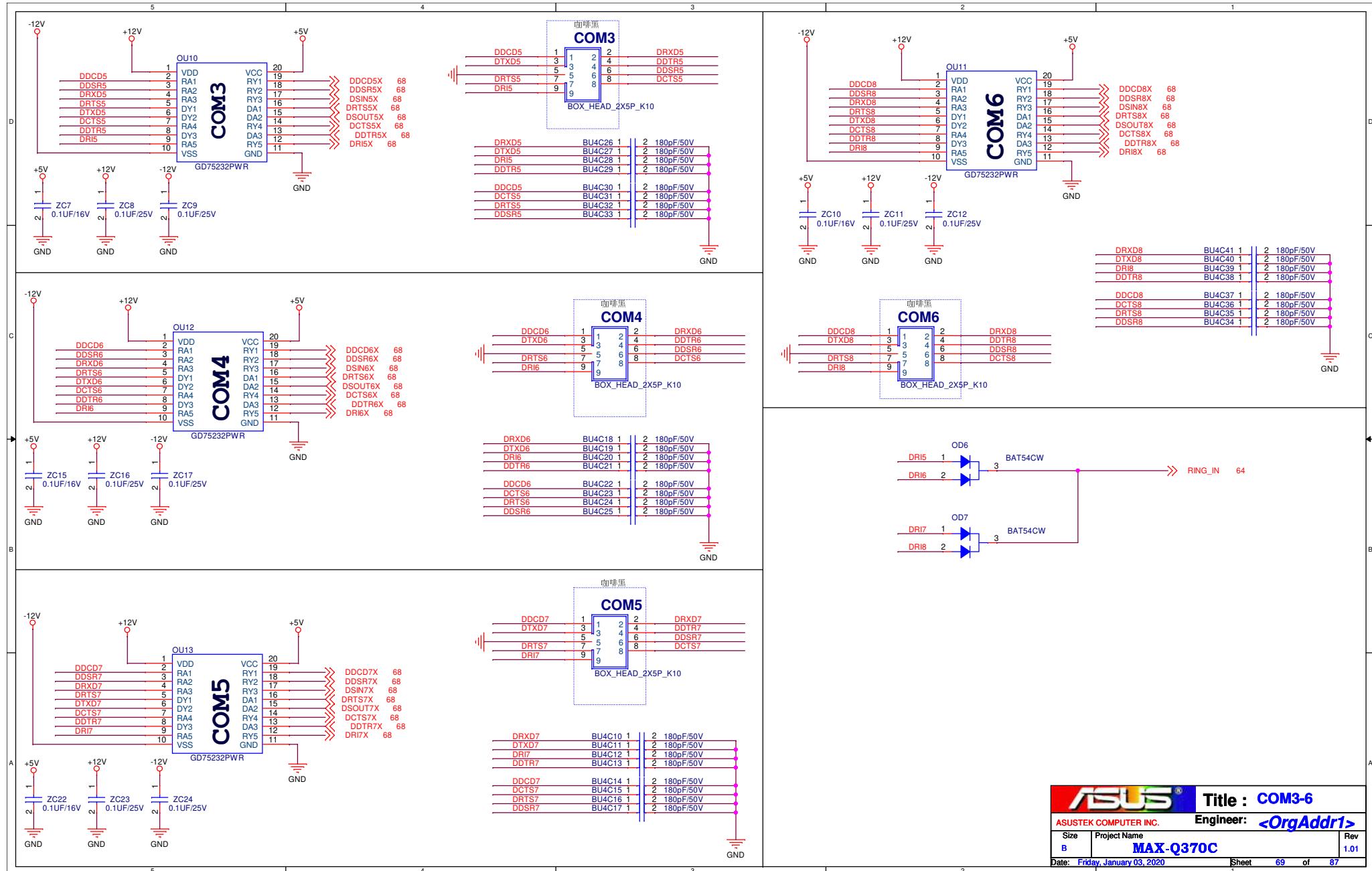


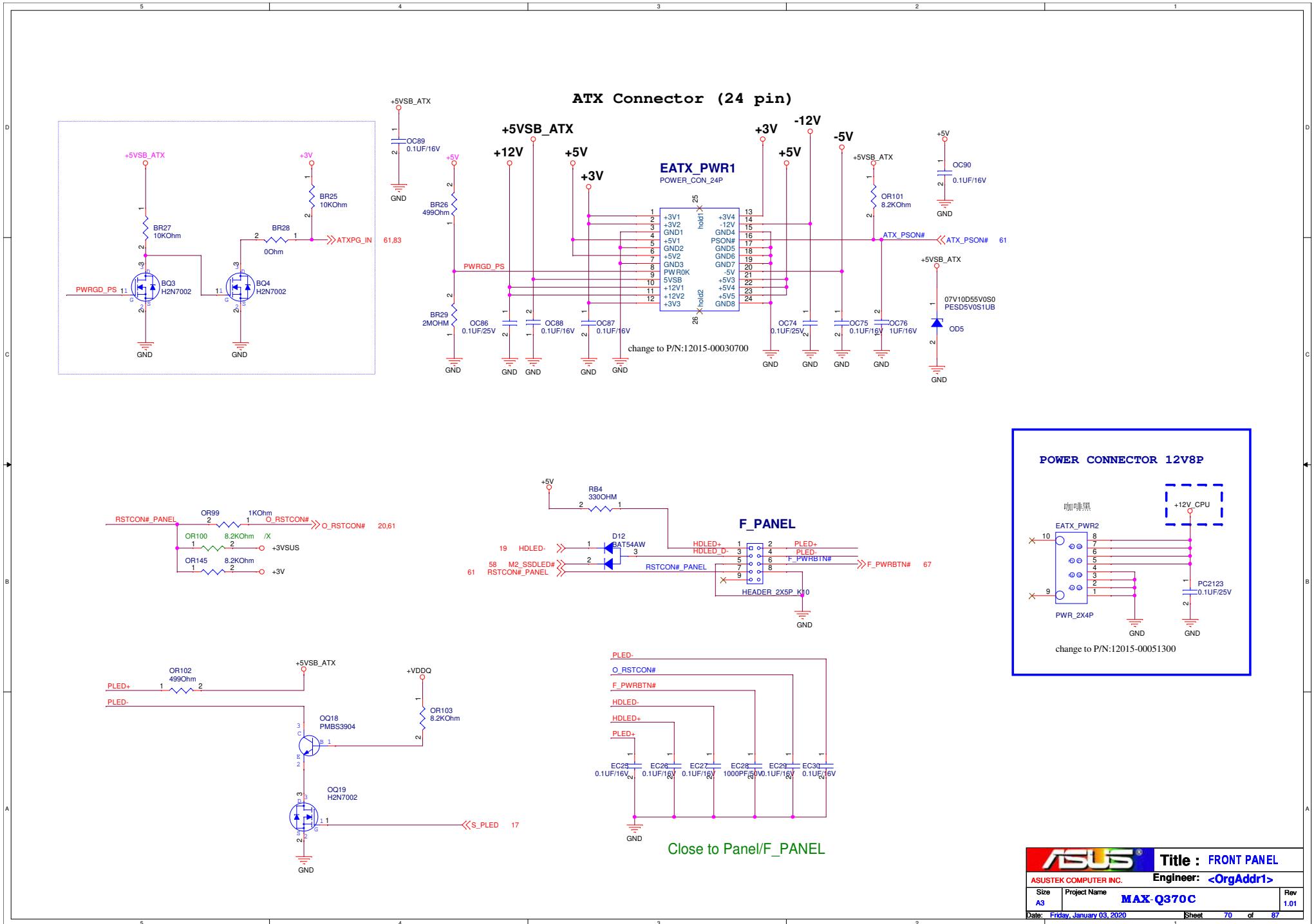
CHASSIS Q-FAN

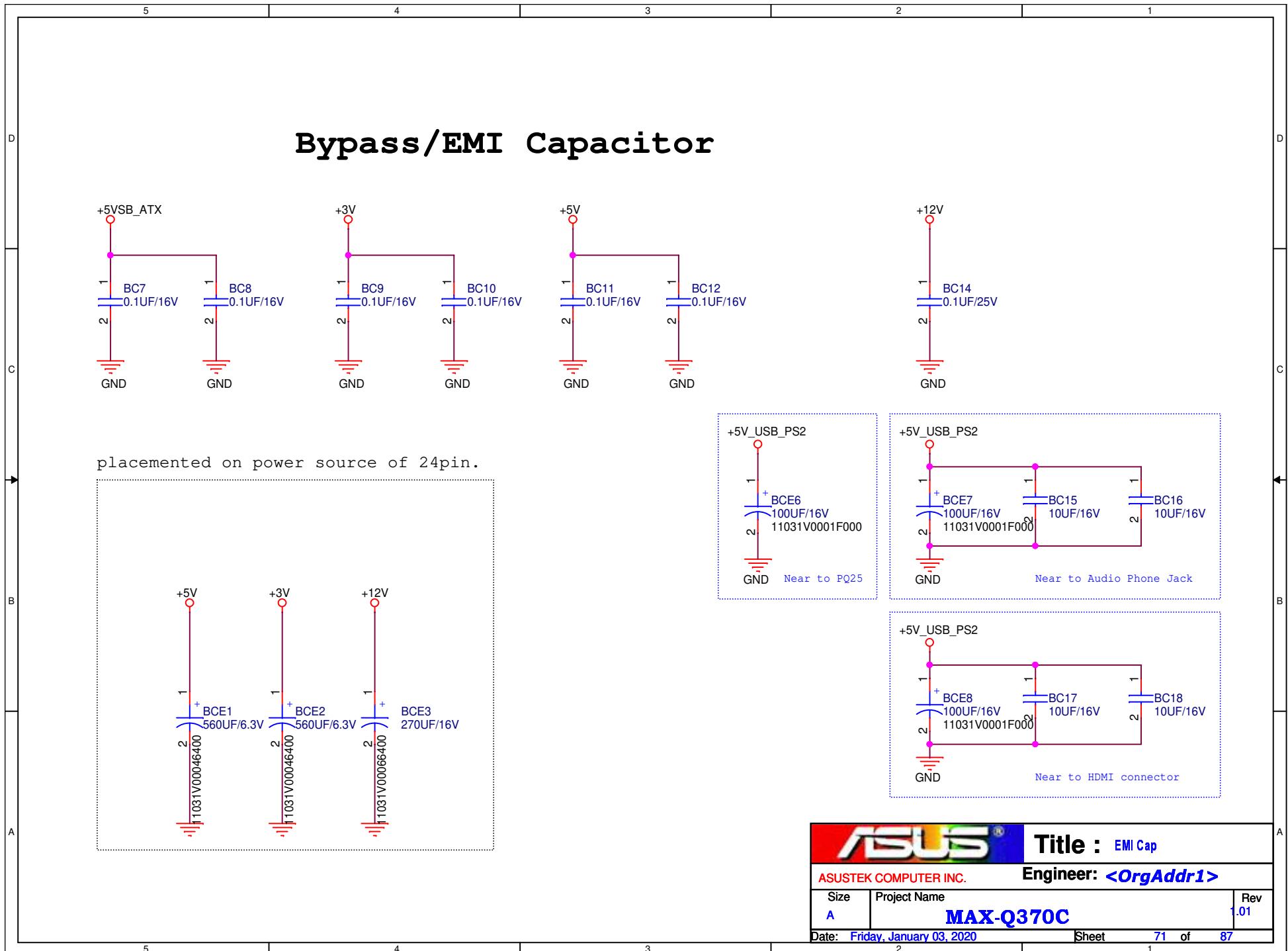


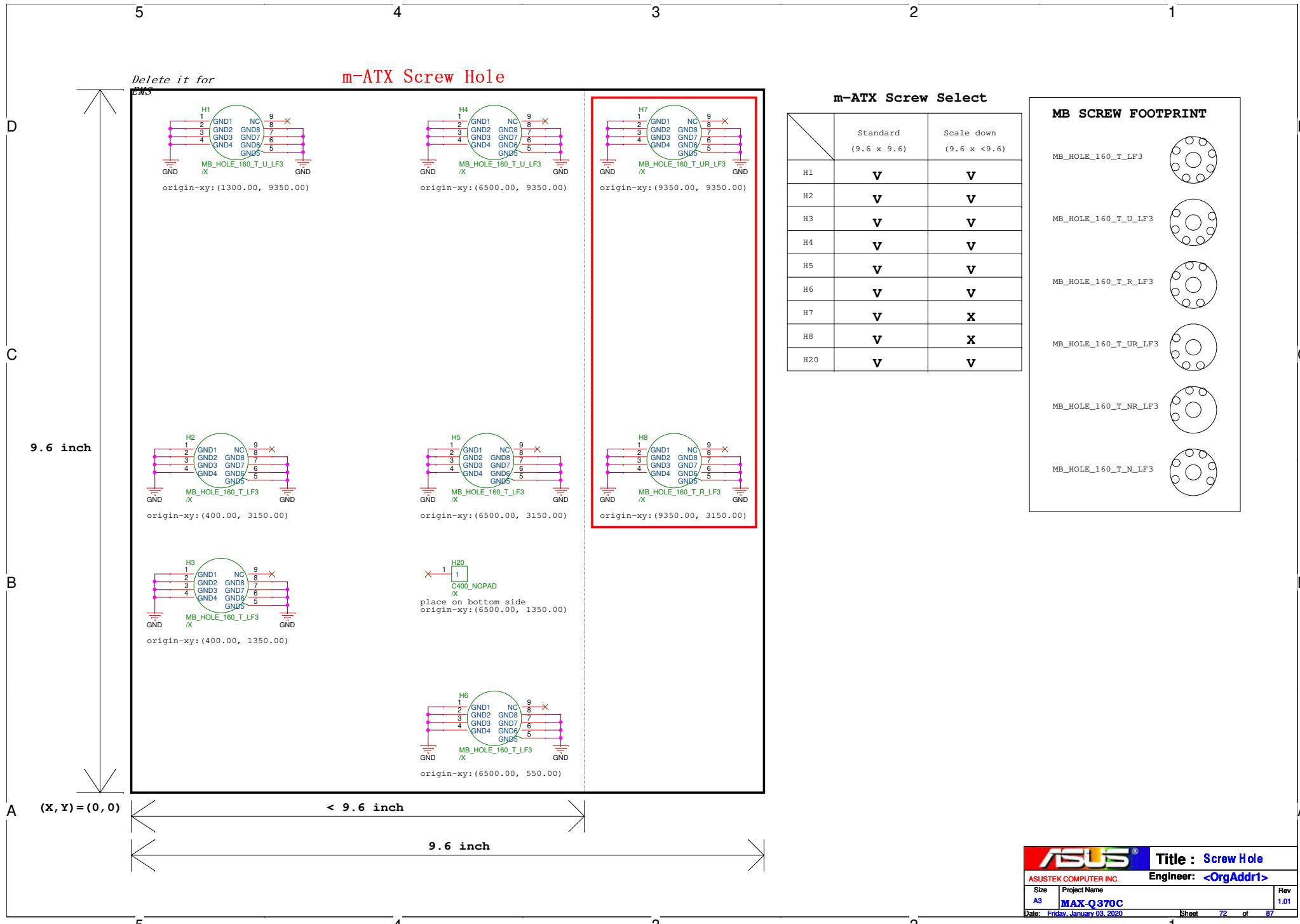












Selling Point

M3
SFIS LABEL
SFIS_LABEL /X
temp_M01_000330

M2
SHORT_GND
Short_GND /X
temp_M05_0031

M1
SHORT_GND1
Short_GND1 /X
temp_M05_0029

DIMM A1 STAR
ASTERISK /X
temp_M01_000340

DIMM B1 STAR
ASTERISK /X
temp_M01_000340

The U-DIMM Order of Insertion

NEED_COMP_SILK

STANDARD CIRCUIT

XUMB OTHER

LOGO_HD_DEMO_OTHER

R1.01-1/1-03

R1.01-1/12-25

PCB

PCB

MAX-Q370C

08001-14301X00

Check PCB P/N

MAX-Q370C R1.01 PCB-08:

R1.01 PCB_DF : 08001-14301000

R1.01 PCB_GECS : 08001-14301100

R1.01 PCB_Trustech : 08001-14301200

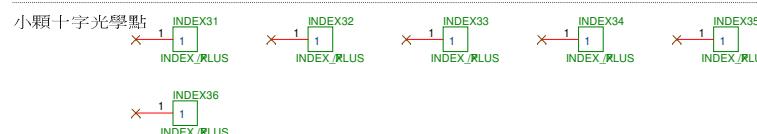
R1.01 PCB_CIRCUIT : 08001-14301300

Fiducial Mask (光學點)

大顆十字光學點

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除。

小顆十字光學點



2012/09/11

Logo

common Logo for all projects



LOGO2
FCC
FCC /X
temp_M01_000348



LOGO5
WEEE_LOGO
WEEE_LOGO /X

LOGO6
CE
CE /X

LOGO7
PCB MADE IN CHINA
PCB MADE IN CHINA /X



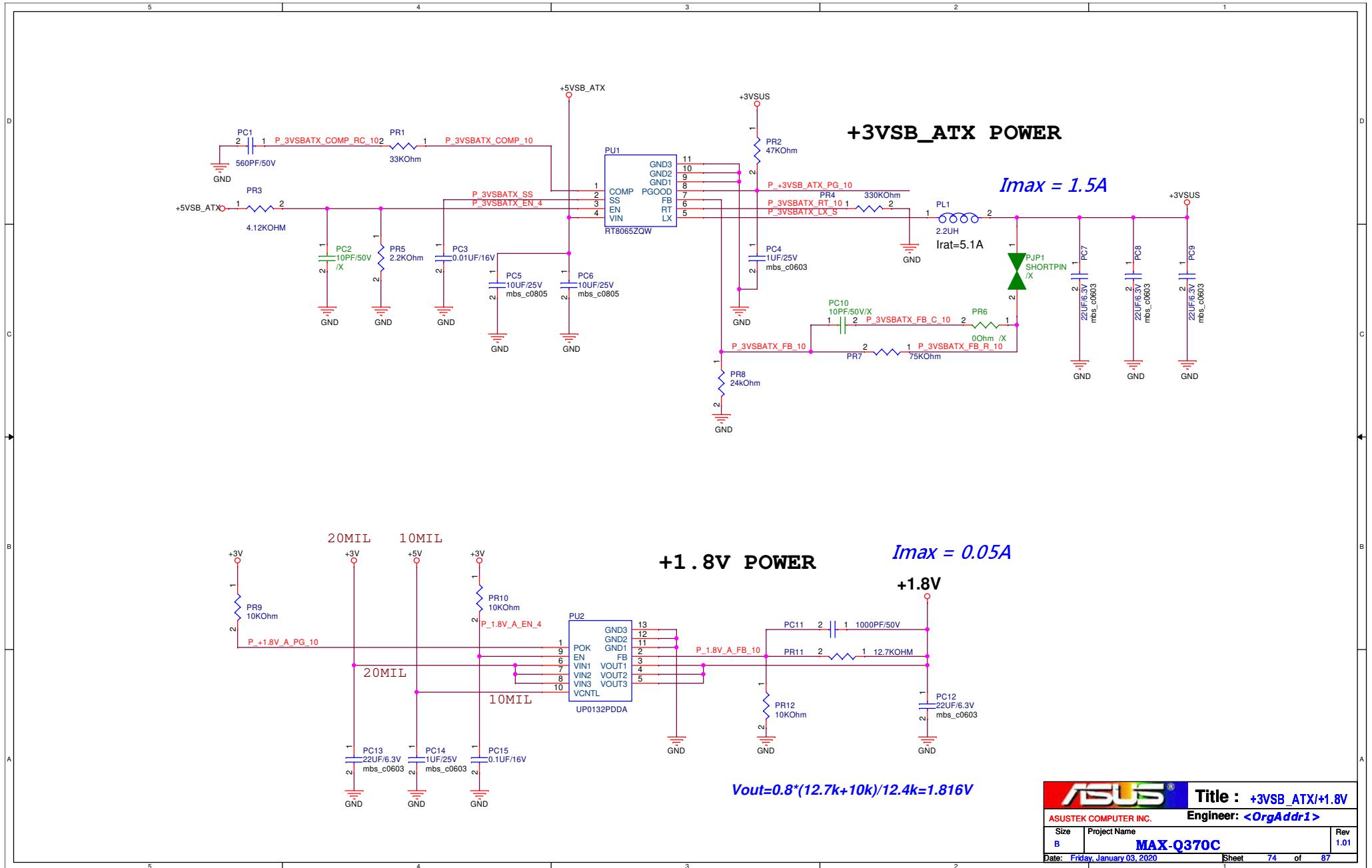
Title : Selling Point_Logo

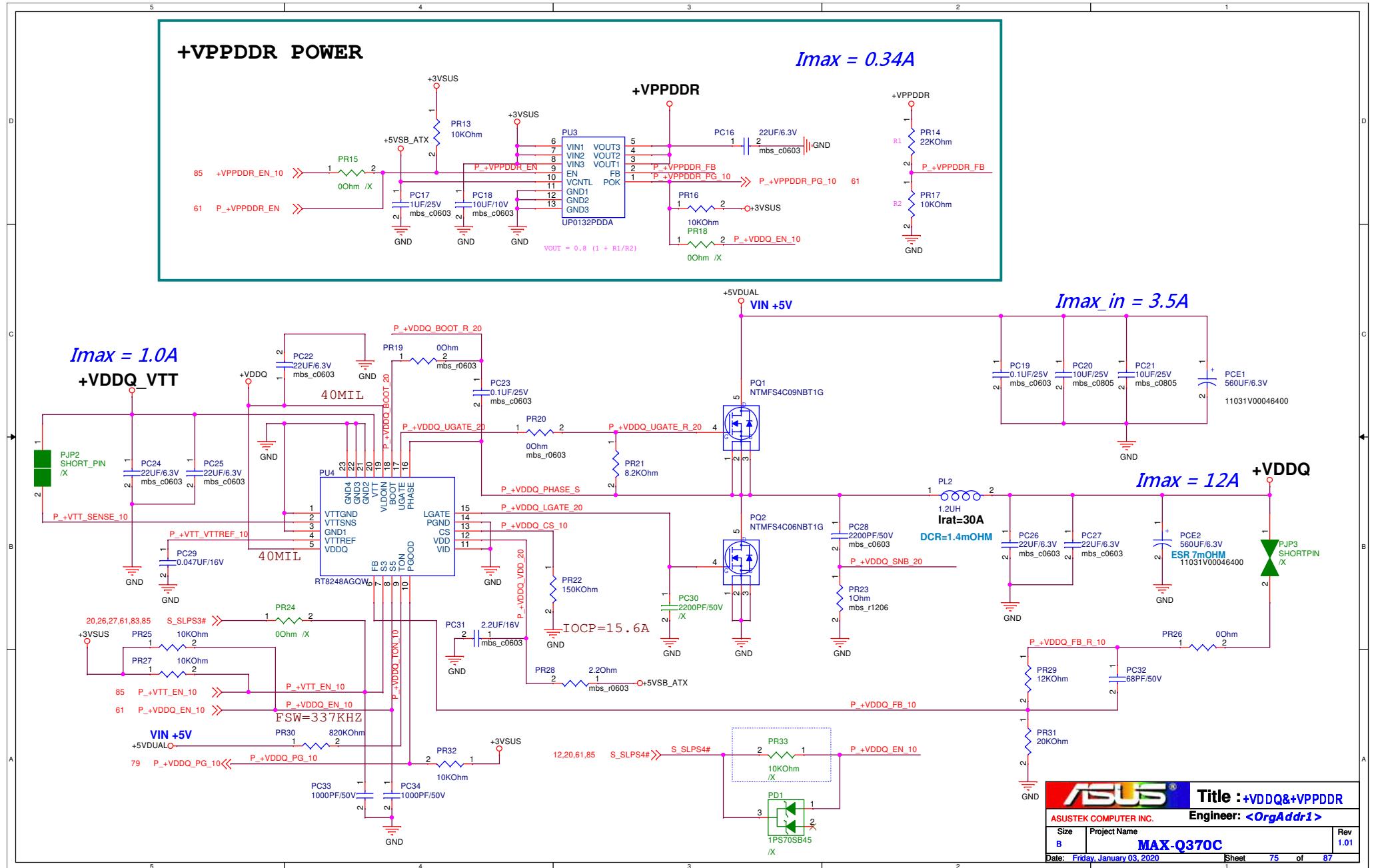
Engineer: <OrgAddr1>

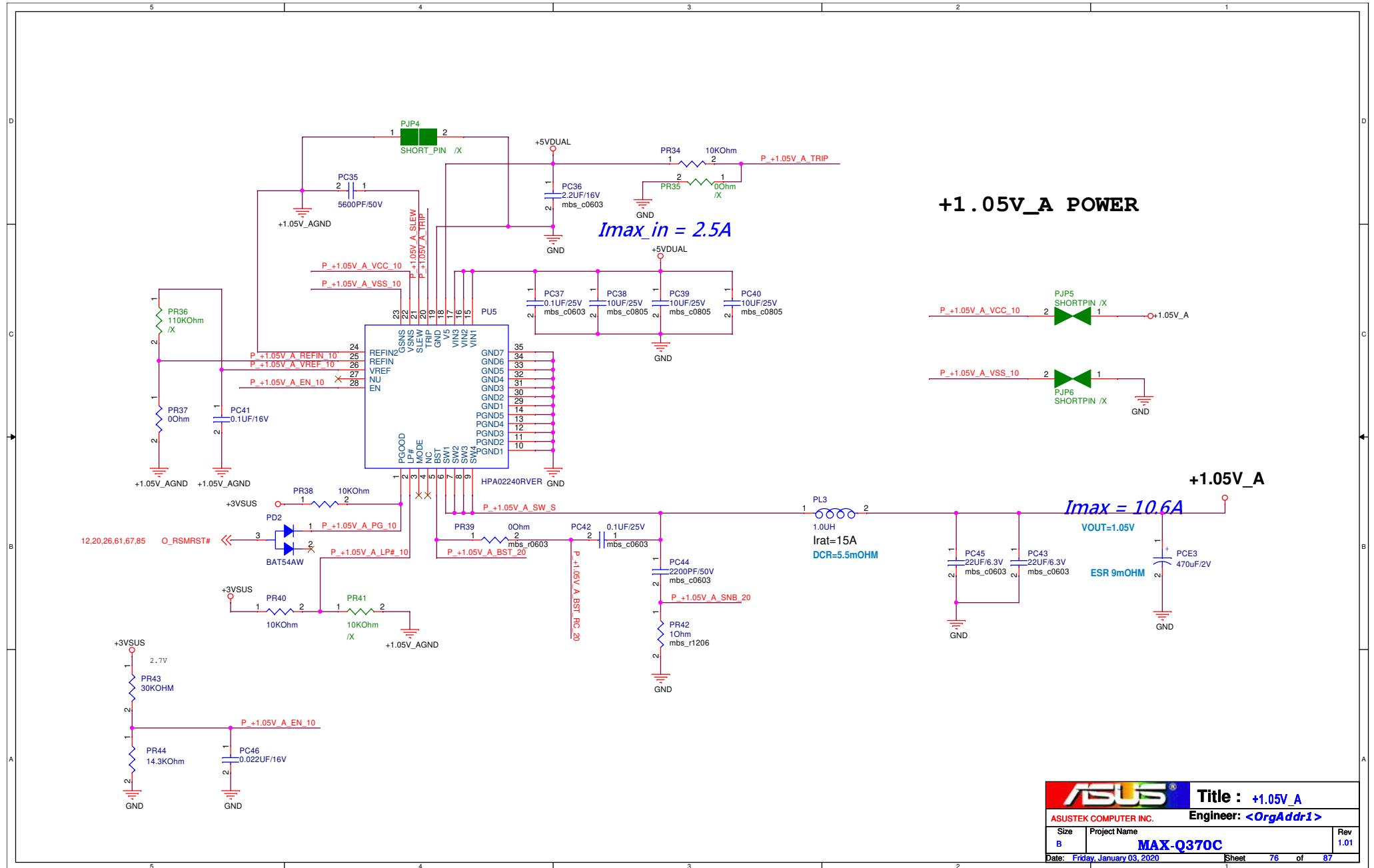
Size	Project Name	Rev
A3	MAX-Q370C	1.01

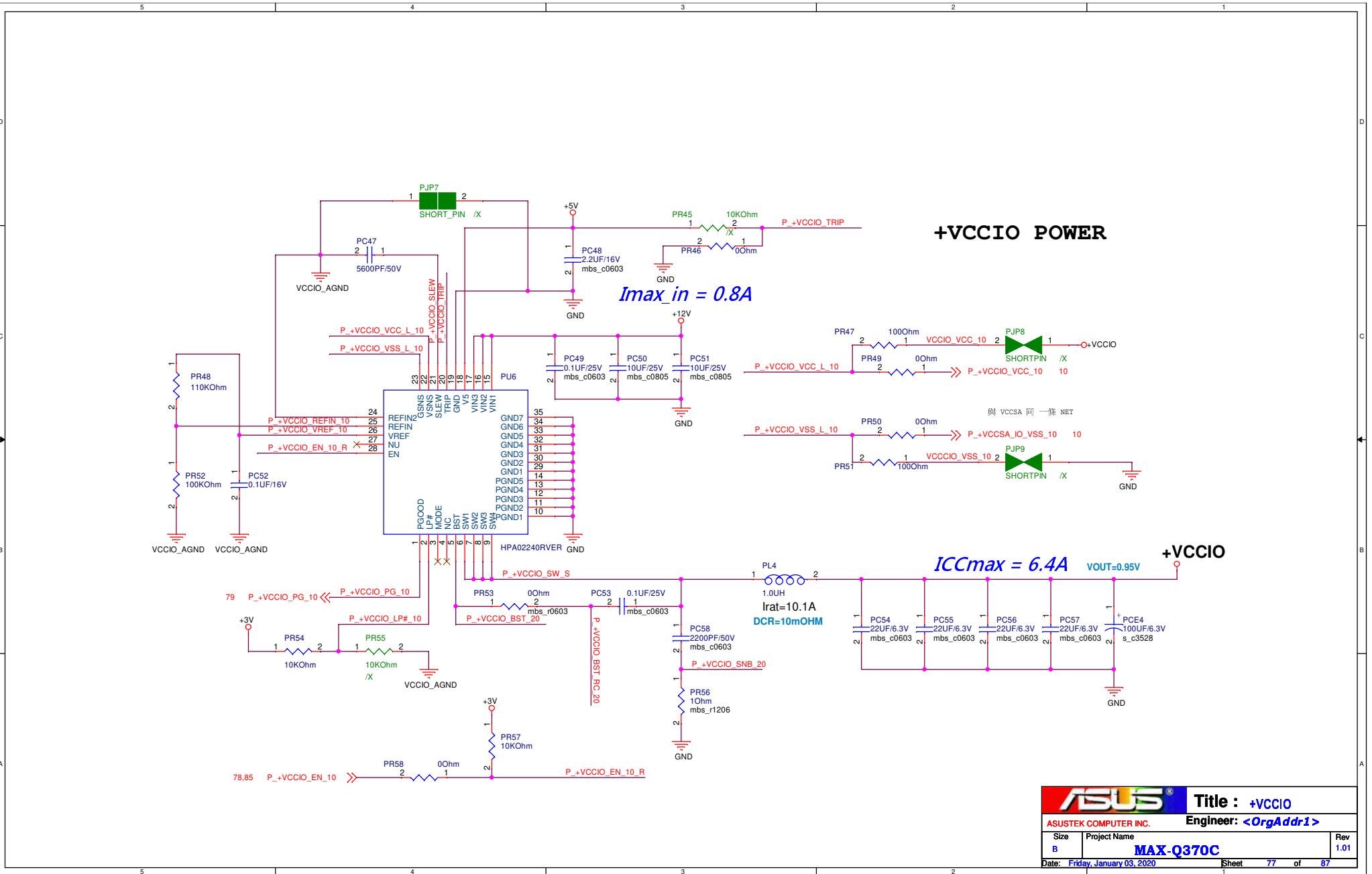
Date: Friday, January 03, 2020

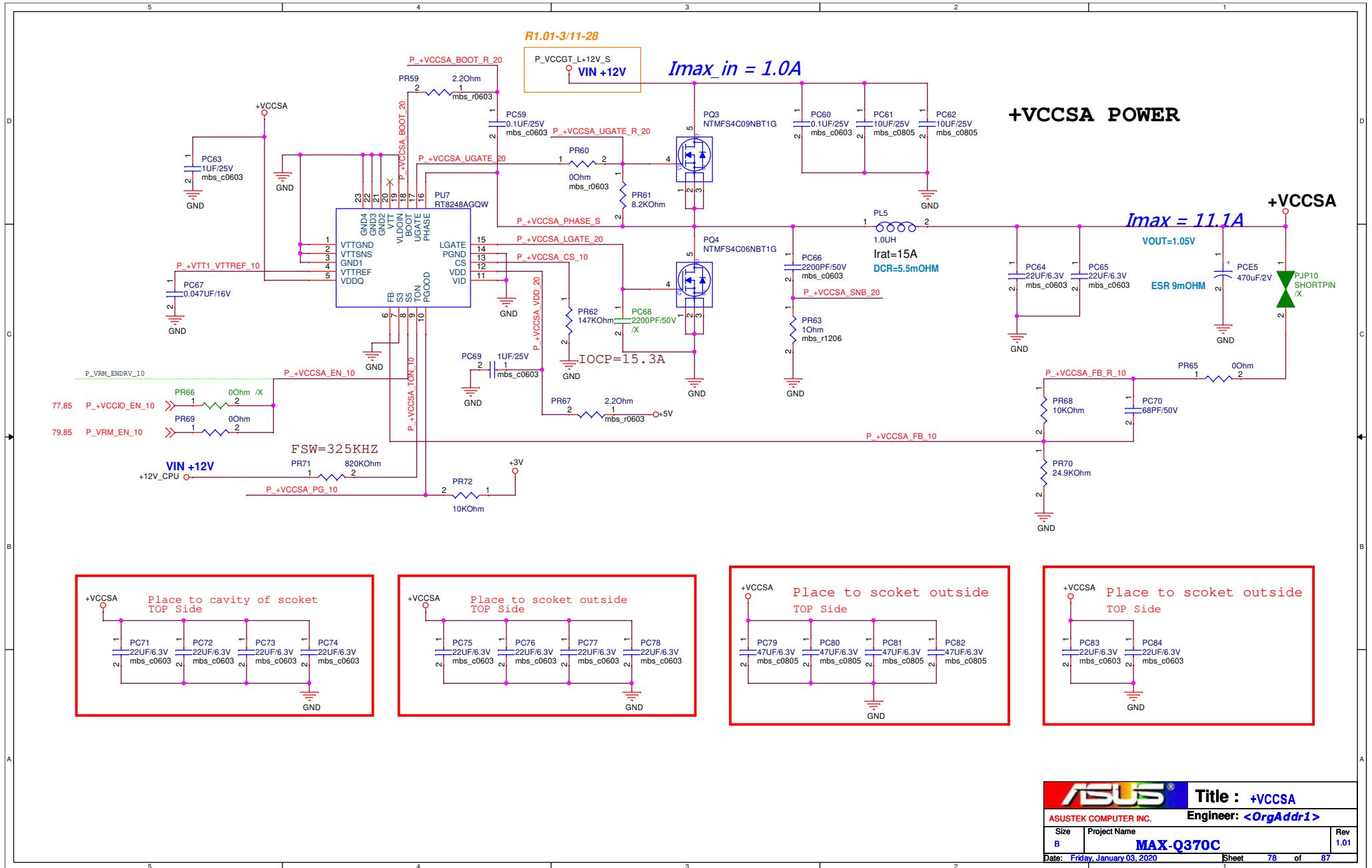
Sheet 73 of 87

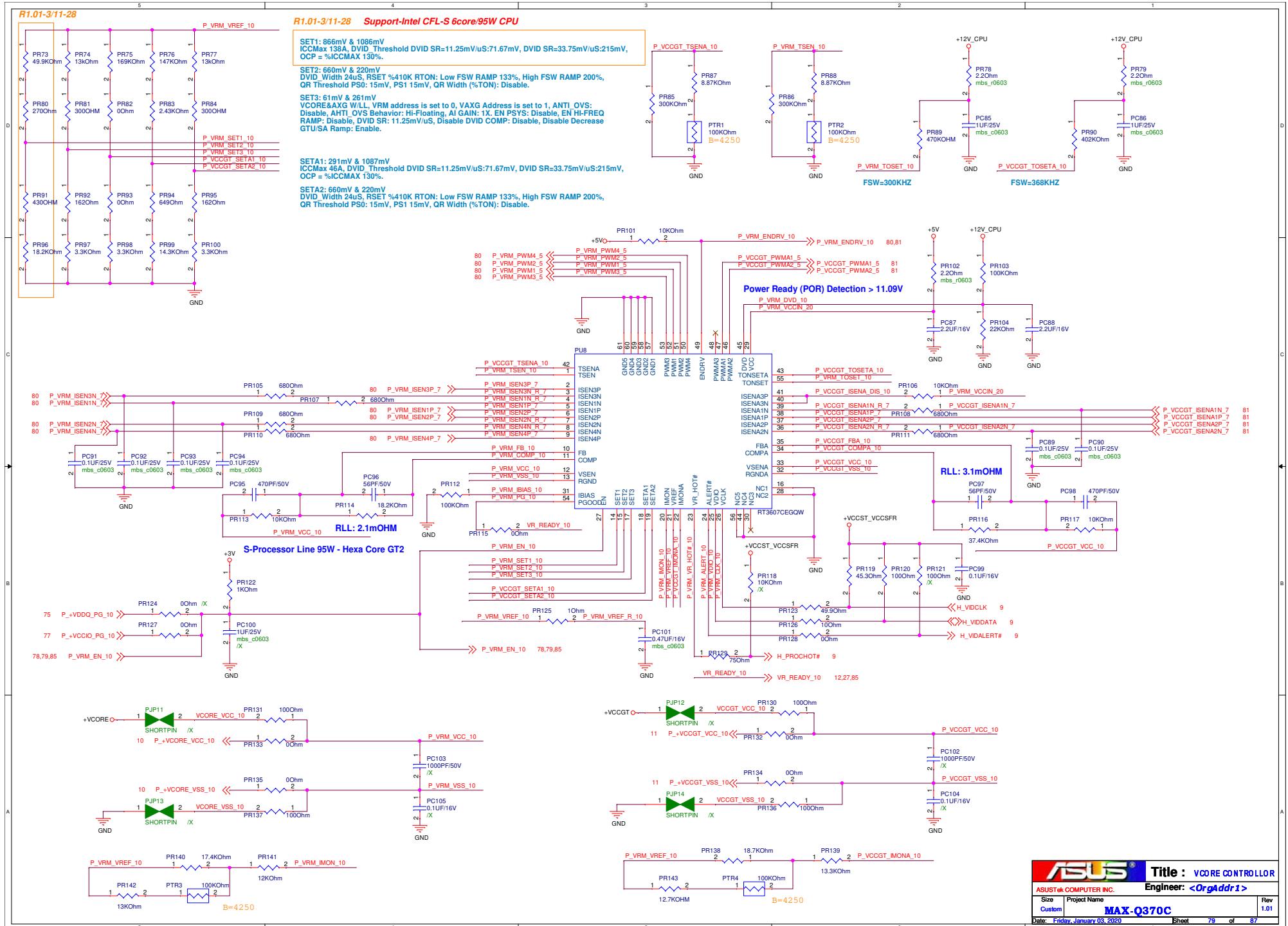


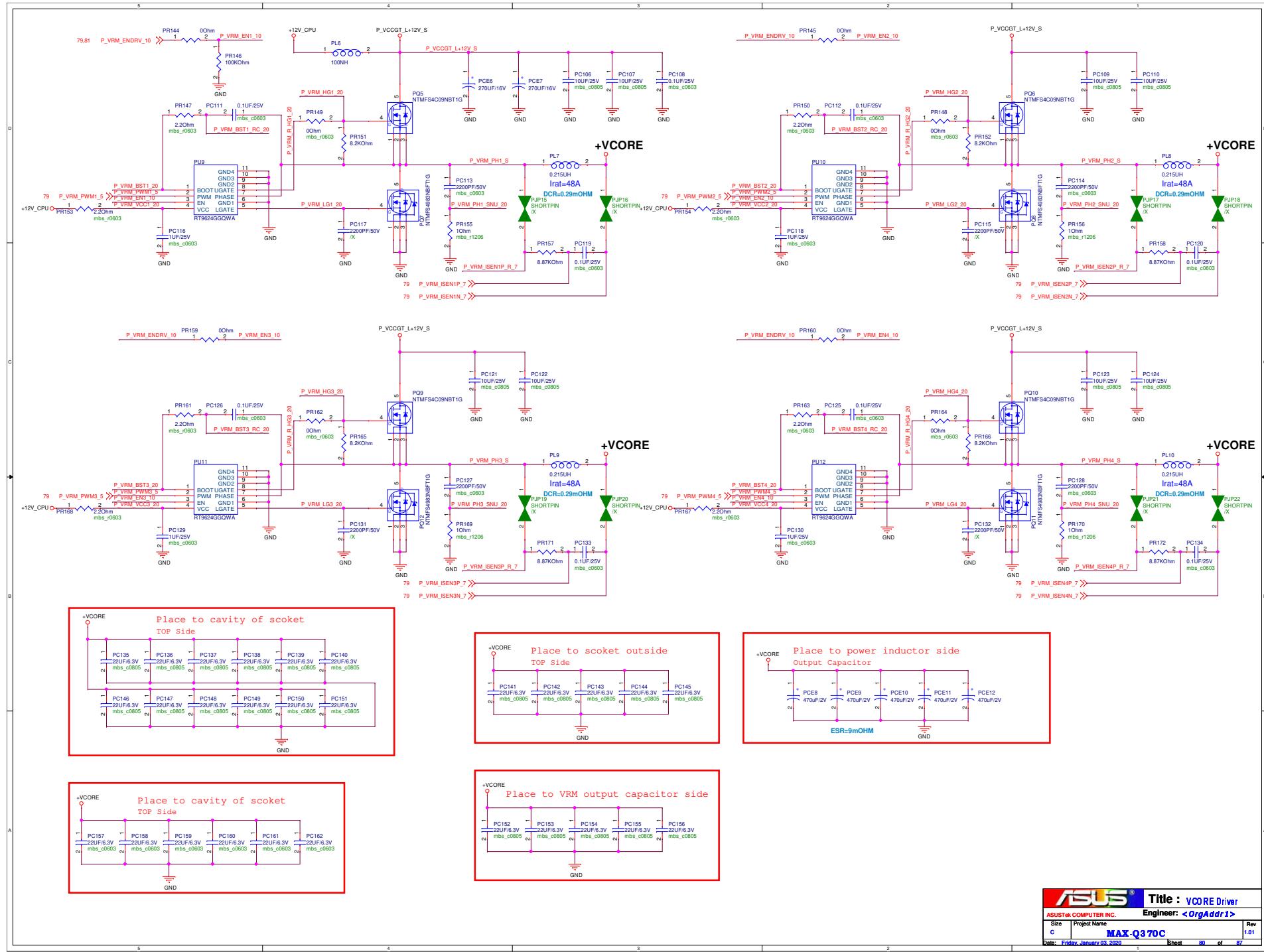


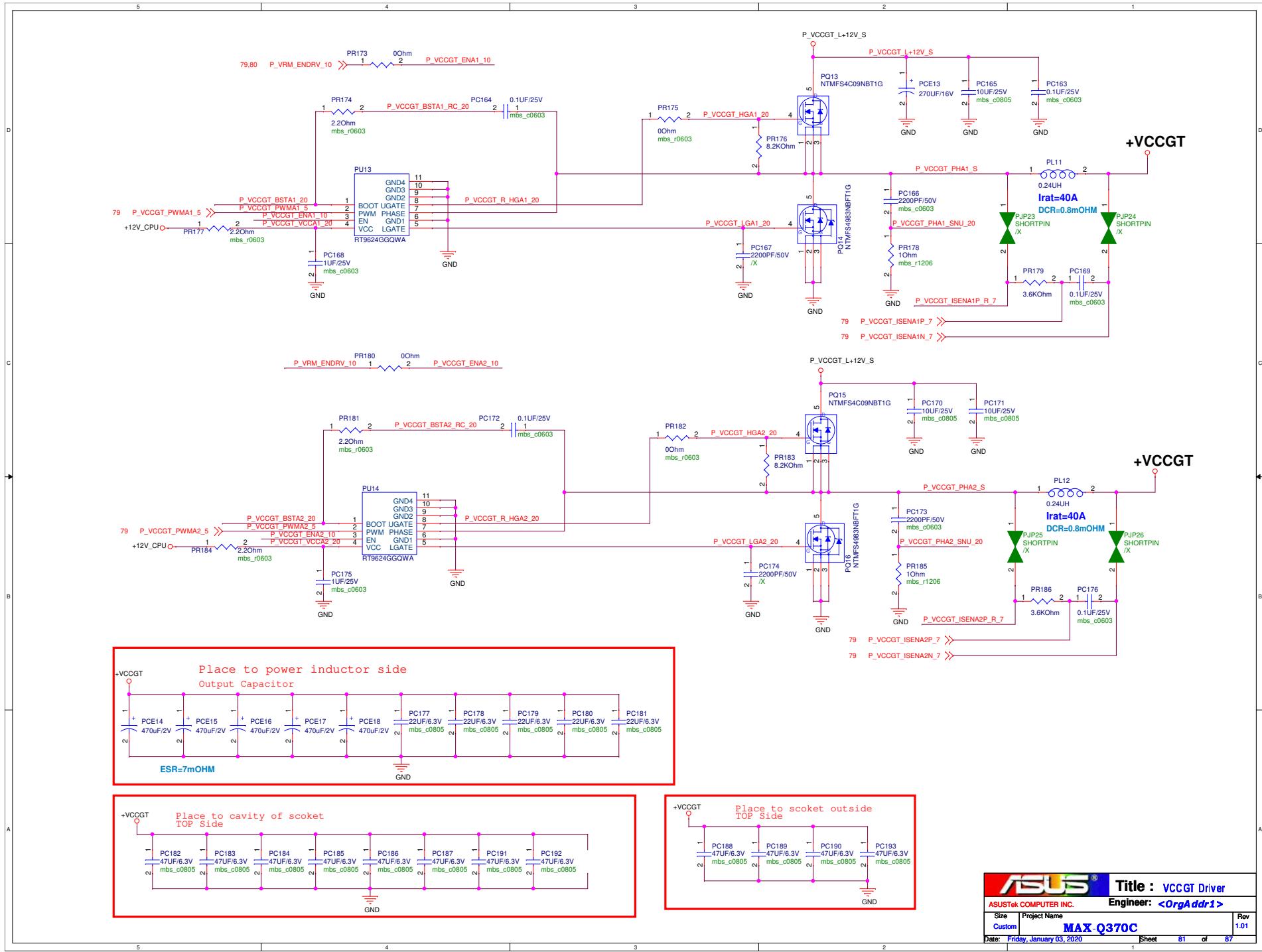


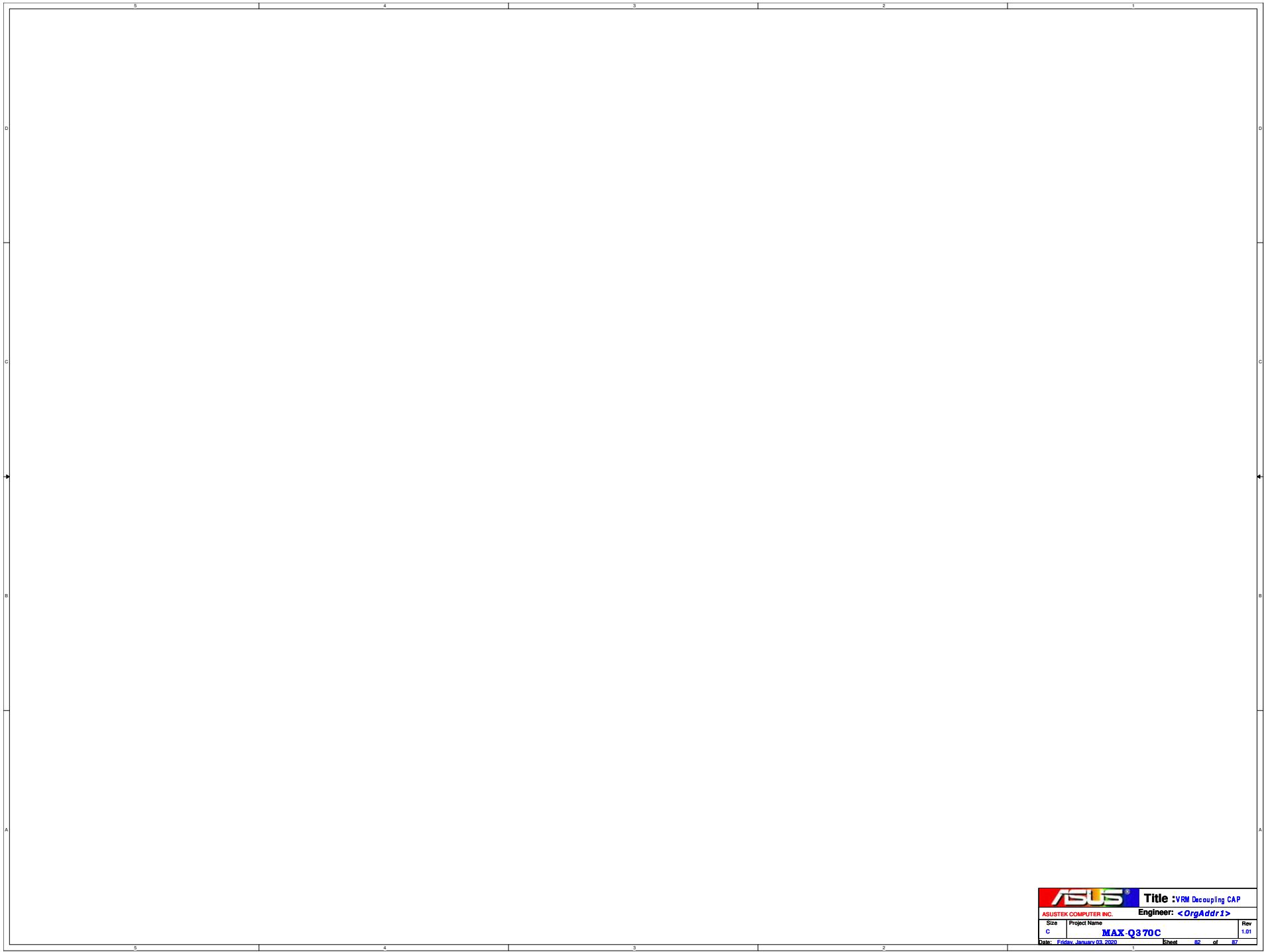




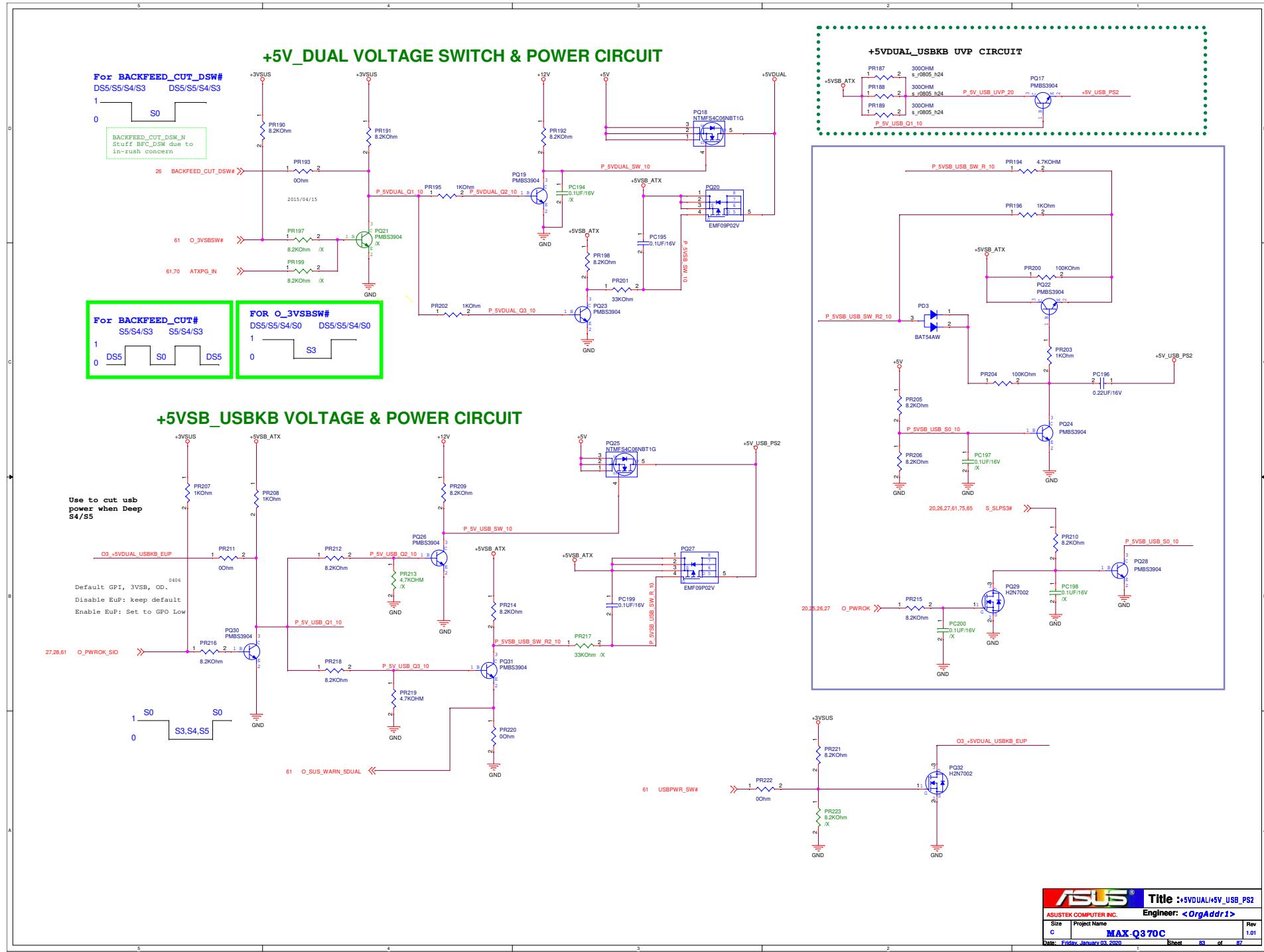


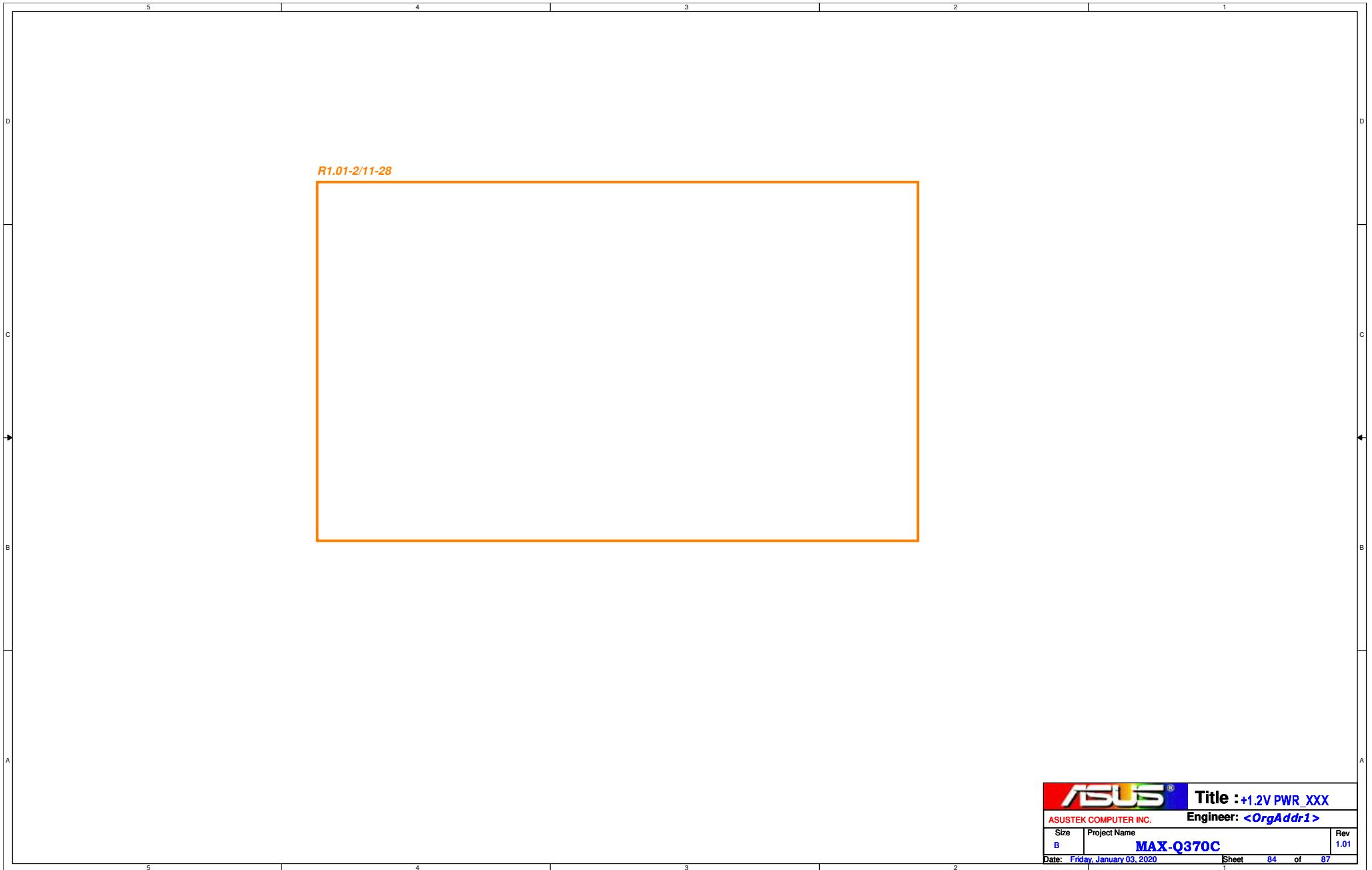




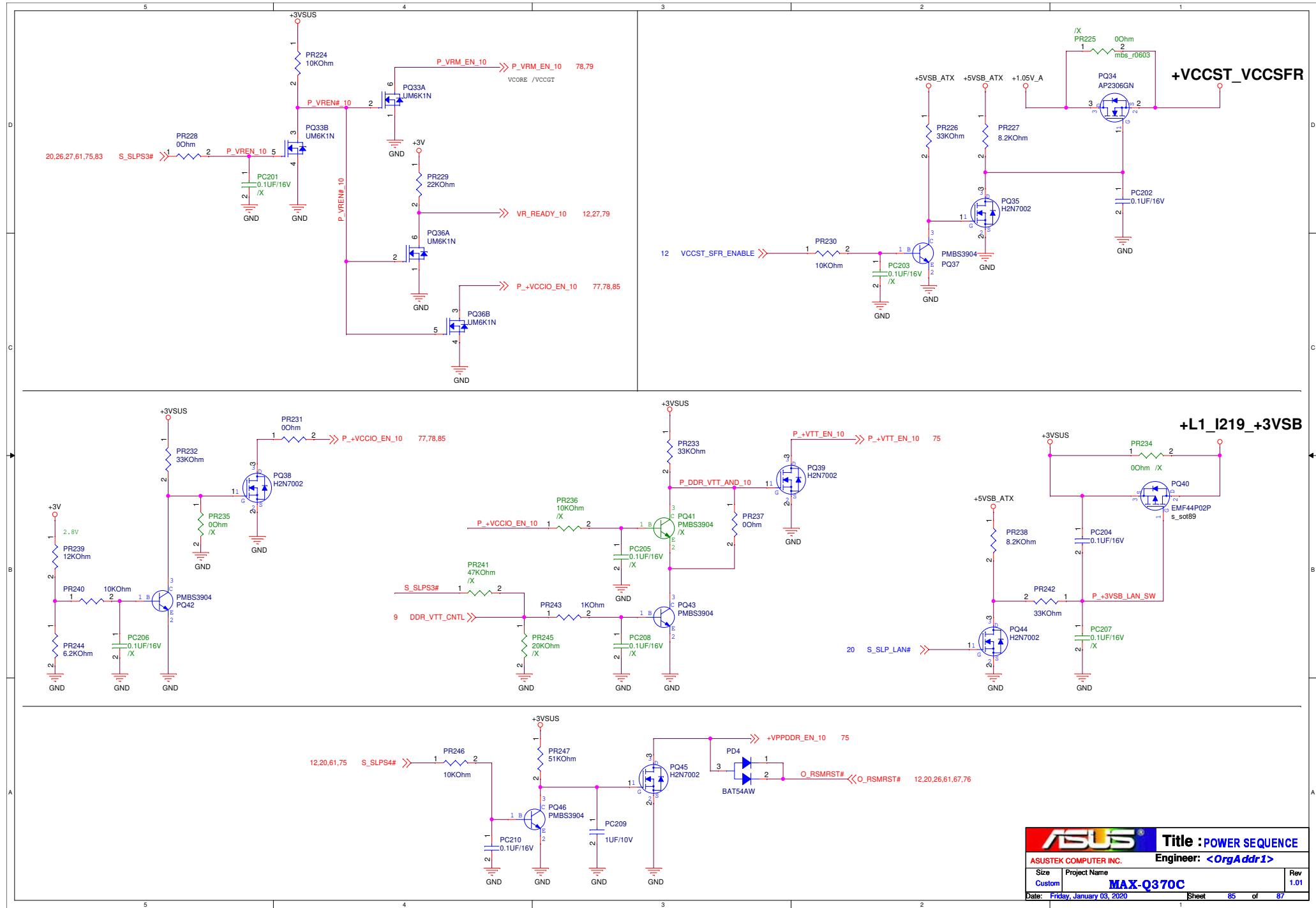


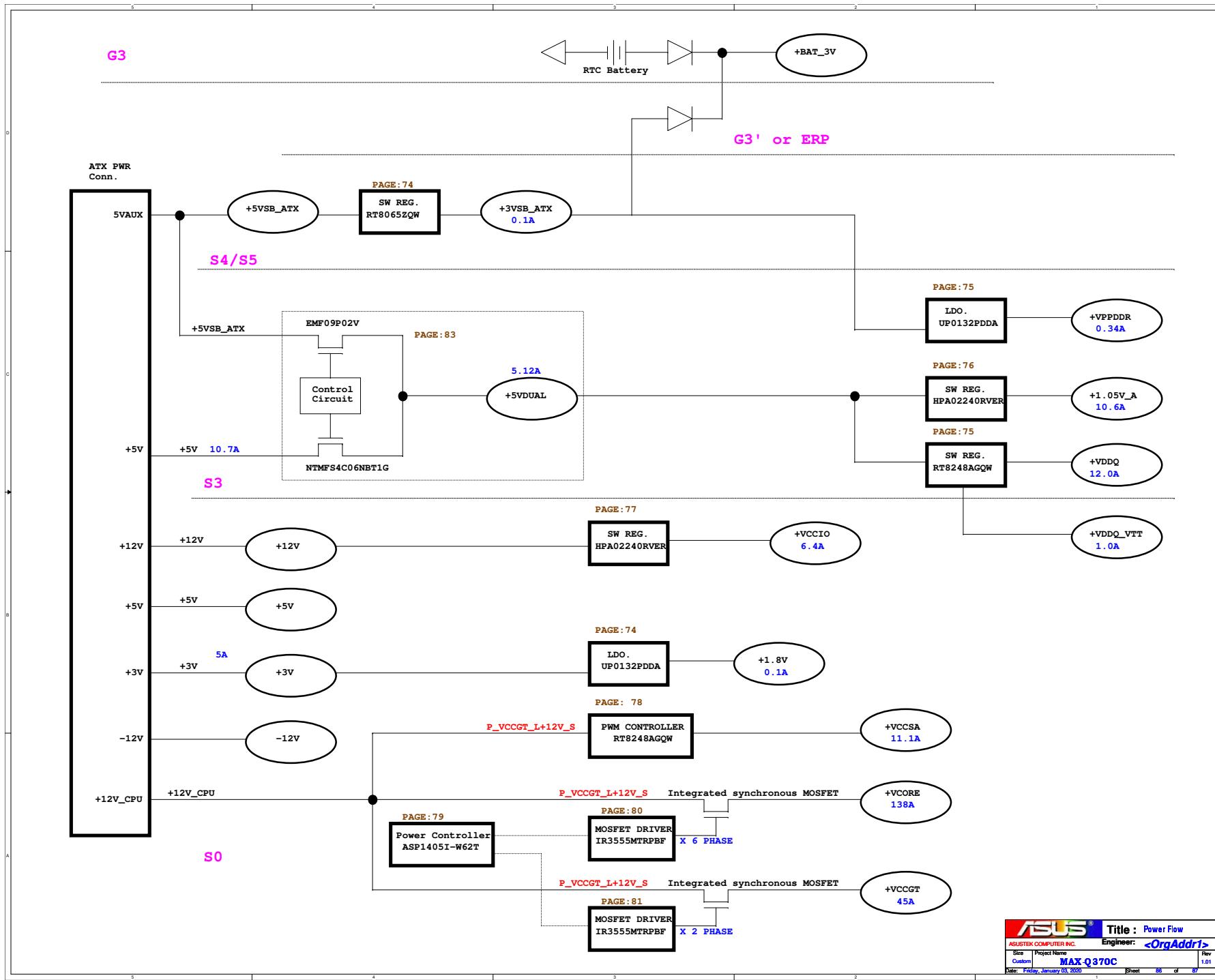
ASUS®		Title : VRM Decoupling CAP	
ASUSTEK COMPUTER INC.		Engineer: <OrgAdd1>	
Size	Project Name	Rev	
C	MAX-Q370C	1.01	
Date:	Friday, January 03, 2020	Sheet	82 of 87





		Title : +1.2V PWR_XXX	
ASUSTEK COMPUTER INC.		Engineer: <OrgAddr1>	
Size B	Project Name MAX-Q370C	Rev 1.01	
Date: Friday, January 03, 2020	Sheet 84	of 87	





Rev	Date	Description	Rev	Date	Description	Rev	Date	Description	Rev	Date	Description
1.0 Green	10/03/2019	First Release									
	10/08/2019	1. Change PCIE4 Slot Name for IPC MB Rule. Page18,19,32,33,34. 2. Change LAN4+USB20 Connector P/N:2014-0062100 /FOXCONN/JFM38U1M-F1GR-4F. Page45,47.									
	10/14/2019	1. Change USB20 Port_79 for USB20x4 Port Connector. Page57. 2. Change LAN1+USB20 Port_910, LANG+USB20 Port1112. Page45,47.									
	10/15/2019	3. Support PCIE2 SSD Only : Del M.2_SSD_PEDET Symbol. Page58.									
	10/21/2019	1. ADD Systems GPIO/SIO Setting Table. Page2. 2. ADD System HSIO Table. Page18.									
	10/21/2019	3. ADD MAX-Q370C EVT REV.1.0 PCB Number : 08001-14300X00. Page73.									
	10/21/2019	1. SWAP USB30 X4 Ports. 5678. Page57. 2. Change LAN1_USB2_910,LANE_USB2_1112 Pin27,28,29,30 from L_GND to GND. Page45,47.									
	10/23/2019	1. Follow LSPCON-HDM2.0 Level Shift Design Guide : GU33 Ball_G1:SW_HDMI_B_HPD unmount GR3501=100Kohm pull-down. Page35.									
	10/24/2019	1. Follow MAX-Q370B PWR SEO : Change HPA (XDP_PRSENTA) from 8.2Kohm to 100Kohm Pull-High +3VSUS. Page12. 2. ADD DIO PWR Nethname => PWR. Page57.									
	10/28/2019	1. Release EVT R1.00 69 Final BOM: 60M040X3-MBA01									
1.01 Orange	11/26/2019	1. Change HDMI1 Port from HDMI2.0 to HDMI1.4. Page08,21,35,84. 2. Change PS2_KBMS_USBS3_12 Connector from USB31_Gen2 to Gen1-50bps. Page50,53. 3. Change PWR Solution from CFL-S_8core95W to 8core95W. Page78,79,80,81,82.									
	12/25/2019	1. Release MAX-Q370B Rev.1.01 35 PCB Part Number: 08001-14301X00. Page73. (1) R1.01 PCB: 08001-14301000 (2) R1.01 PCB_GECS: 08001-14301100 (3) R1.01 PCB_Trustech: 08001-14301200 (4) R1.01 PCB_CIRCUIT: 08001-14301300									
	1/03/2020	1. Follow IPC HW Leader Define : Remove PCB_VENDOR_LOGO. Page73.									