

## SATA (SATA3.0)

The schematic diagram illustrates the SATA3.0 signal traces and power supply for a SATA controller chip (CN11, 7P 770-83-07SV29). The chip is connected to a SATA connector (CN42, 2P 1192-700-02S) via a +V5S power supply.

**Signal Traces:**

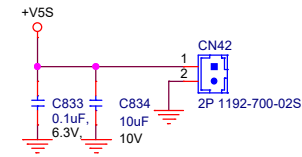
- SATA0\_TXP** and **SATA0\_TXN** are connected to **C832** and **C831** (0.01uF, 25V) capacitors, which are then connected to **SATA0\_TXP\_C** and **SATA0\_TXN\_C** respectively.
- SATA0\_RXN** and **SATA0\_RXP** are connected to **C830** and **C829** (0.01uF, 25V) capacitors, which are then connected to **SATA0\_RXN\_C** and **SATA0\_RXP\_C** respectively.

**Power Supply:**

- The **+V5S** power supply is connected to the **GND1** pin of the chip.
- The **GND2** pin is connected to the **GND3** pin, which is then connected to the **H2** pin of the chip.
- The **H1** pin is connected to the **H2** pin.
- The **GND3** pin is connected to the **H2** pin.
- The **H1** pin is connected to the **H2** pin.

**Capacitors:**

- C832** and **C831** are 0.01uF, 25V capacitors.
- C830** and **C829** are 0.01uF, 25V capacitors.
- C833** is a 0.1uF, 6.3V capacitor.
- C834** is a 10uF, 10V capacitor.



# DIO

**CN45 X15'2P 52A-90-10GB00**

Pin	Signal	Value
1	DIO_0	24
2	DIO_1	24
3	DIO_2	24
4	DIO_3	24
5	DIO_4	24
6	DIO_5	24
7	DIO_6	24
8	DIO_7	24

+V5S  
FS5  
X1206L110THYR  
C500 X0.1uF 16V

**U23 X10,AZ1045-04F**

Line	Signal	Value
1	DIO_4	24
2	DIO_5	24
3	DIO_6	24
4	DIO_7	24

**U24 X10,AZ1045-04F**

Line	Signal	Value
1	DIO_0	24
2	DIO_1	24
3	DIO_2	24
4	DIO_3	24

**R530-R537 4.7K**

Signal	Resistor	Value
DIO_0	R530	4.7K
DIO_1	R531	4.7K
DIO_2	R532	4.7K
DIO_3	R533	4.7K
DIO_4	R534	4.7K
DIO_5	R535	4.7K
DIO_6	R536	4.7K
DIO_7	R537	4.7K

**C336-C343 470pF 50V**

Signal	Capacitor	Value
DIO_0	C336	470pF 50V
DIO_1	C337	470pF 50V
DIO_2	C338	470pF 50V
DIO_3	C339	470pF 50V
DIO_4	C340	470pF 50V
DIO_5	C341	470pF 50V
DIO_6	C342	470pF 50V
DIO_7	C343	470pF 50V

# TPM

**SPI\_SO R521 X10K**

**SPI\_CS2\_TPM# R522 10K**

**V3P3A**

**R527 10K**

**NPCT75x**

**NC10 PIRQ#/GPIO2**

**NC18 MISO/GPIO7**

**NC21 MISO**

**NC20 SCS#/GPIO5**

**NC27 SCLK**

**NC13 GPIO4**

**NC17 PLTRST#**

**NC14 NC14**

**NC12 NC12**

**NC15 NC15**

**NC4 PP/GPIO6**

**NC3 SCL/GPIO1**

**NC29 SDA/GPIO0**

**NC6 GPIO3**

**NC5 NC5**

**NC1 NC1**

**NC6 NC6**

**NC7 NC7**

**NC8 NC8**

**NC11 NC11**

**NC12 NC12**

**NC15 NC15**

**NC2 GND1**

**NC3 GND2**

**NC4 GND3**

**NC9 NC9**

**NC10 PIRQ#/GPIO2**

**NC18 MISO/GPIO7**

**NC21 MISO**

**NC20 SCS#/GPIO5**

**NC27 SCLK**

**NC13 GPIO4**

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**NC1 NC1**

**NC6 NC6**

**NC7 NC7**

**NC8 NC8**

**NC11 NC11**

**NC12 NC12**

**NC15 NC15**

**NC2 GND1**

**NC3 GND2**

**NC4 GND3**

**NC9 NC9**

**NC10 PIRQ#/GPIO2**

**NC18 MISO/GPIO7**

**NC21 MISO**

**NC20 SCS#/GPIO5**

**NC27 SCLK**

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**NC1 NC1**

**NC6 NC6**

**NC7 NC7**

**NC8 NC8**

**NC11 NC11**

**NC12 NC12**

**NC15 NC15**

**NC2 GND1**

**NC3 GND2**

**NC4 GND3**

**NC9 NC9**

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**NC6 NC6**

**NC7 NC7**

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**NC2 GND1**

**NC3 GND2**

**NC4 GND3**

**NC9 NC9**

**NC10 PIRQ#/GPIO2**

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**NC20 SCS#/GPIO5**

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**NC17 PLTRST#**

**NC14 NC14**

**NC12 NC12**

**NC15 NC15**

**NC4 PP/GPIO6**

**NC3 SCL/GPIO1**

**NC29 SDA/GPIO0**

**NC6 GPIO3**

**NC5 NC5**

**NC1 NC1**

**NC6 NC6**

**NC7 NC7**

**NC8 NC8**

**NC11 NC11**

**NC12 NC12**

**NC15 NC15**

**NC2 GND1**

**NC3 GND2**

**NC4 GND3**

**NC9 NC9**

**NC10 PIRQ#/GPIO2**

**NC18 MISO/GPIO7**

**NC21 MISO**

**NC20 SCS#/GPIO5**

**NC27 SCLK**

**NC13 GPIO4**

**NC17 PLTRST#**

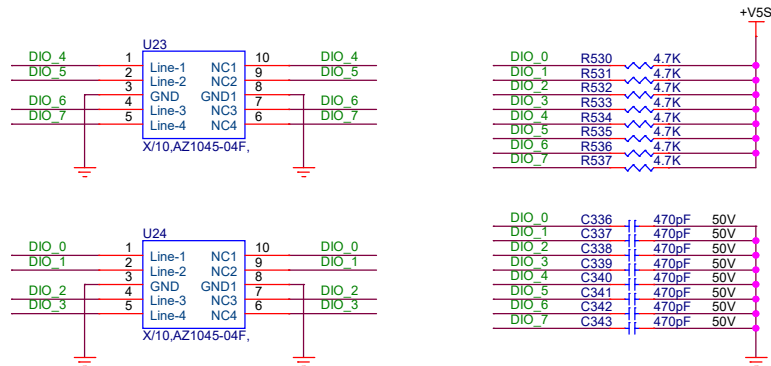
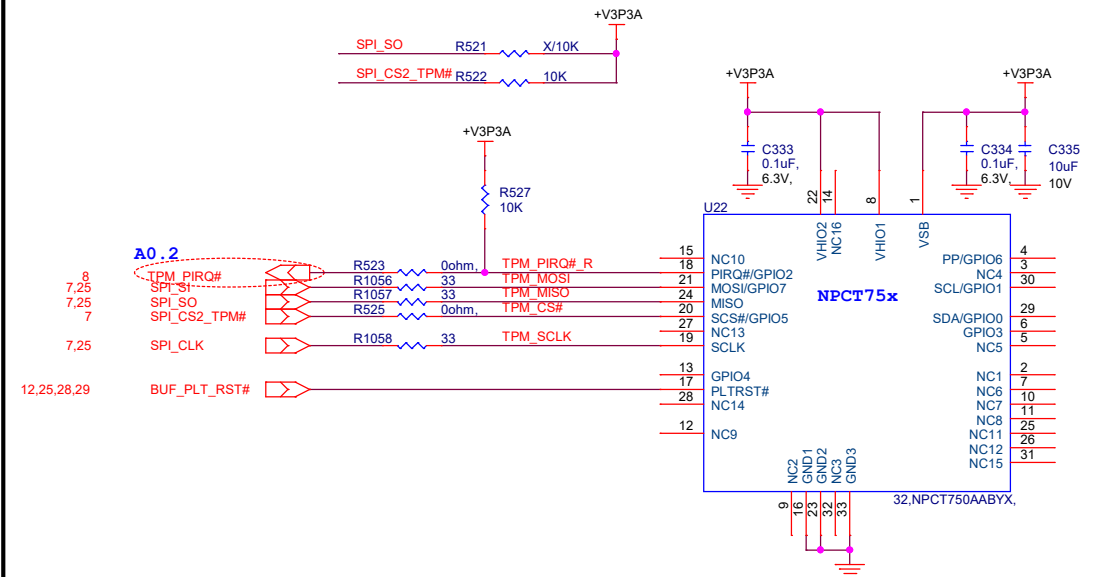
**NC14 NC14**

**NC12 NC12**

**NC15 NC15**

**NC4 PP/GPIO6**

**NC3 SCL/GPIO**

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