AAEON®
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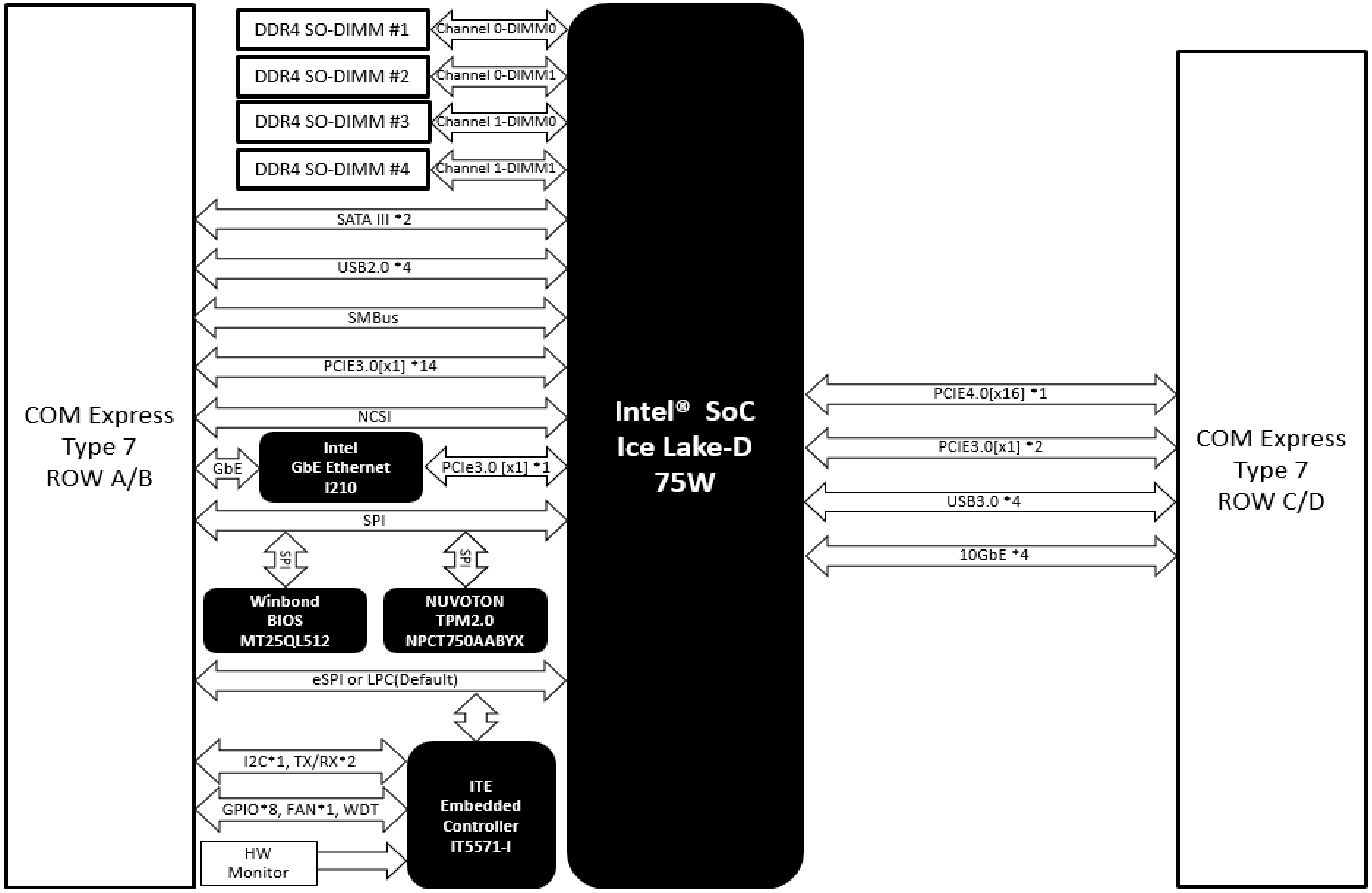
Project Name: COM-ICDB7
Project Number: E210809
Version: A0.3_0_0

System block diagram


COM Express Type 7 ROW A/B
DDR4 SO-DIMM #1
DDR4 SO-DIMM #2
DDR4 SO-DIMM #3
DDR4 SO-DIMM #4
Channel 0-DIMM0
Channel 0-DIMM1
Channel 1-DIMM0
Channel 1-DIMM1
SATA III *2
USB2.0 *4
SMBus
PCIE3.0[x1] *14
NCSI
GbE
Intel GbE Ethernet I210
PCIe3.0 [x1] *1
SPI
SPI
SPI
Winbond BIOS MT25QL512
NUVOTON TPM2.0 NPCT750AABYX
eSPI or LPC(Default)
I2C*1, TX/RX*2
GPIO*8, FAN*1, WDT
HW Monitor
ITE Embedded Controller IT5571-I
Intel® SoC Ice Lake-D 75W
PCIE4.0[x16] *1
PCIE3.0[x1] *2
USB3.0 *4
10GbE *4
COM Express Type 7 ROW C/D

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9	SoC PCIe CPU GEN4
10	SoC PCIE/SATA/USB
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12	SoC ESPI/SMBUS/MISC
13	SoC NCSI/SPI/RTC/PWR MGT
14	SoC PWR1
15	SoC PWR2
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17	SoC VSS1
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19	DDR4 CHA DIMM0
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31	Boot Sequence
32	System Power
33	PWR +V5A/+V3P3A
34	PWR PVCCIN_CPU/P1V8_1
35	PWR PVCCIN_CPU/P1V8_2
36	PWR PVCCIN_CPU/P1V8_3
37	PWR PVCCIN_CPU/P1V8_4
38	PWR PVNN_NAC/ PVCCANA_CPU_1
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40	PWR PVDDQ_ABC_CPU_1
41	PWR PVDDQ_ABC_CPU_2
42	PWR PVPP_CPU_ABC/PVTT_CPU_ABC
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<Core Design>

AAEON® An ASUS Company	***AAEON Technology INC.***
Title	**Block Diagram**
Size	Custom
Document Number	COM-ICDB7
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System Setting

PIN NO.	PIN Name	Multi-Func	Default	GPIO Function
M5	GPA0	PWM0	GPI	EC_AC_PRESENT
N5	GPA1	PWM1	GPI	EC_PROC_PWRGD
M6	GPA2	PWM2	GPI	SUS_PWR_ACK
N6	GPA3	PWM3	GPI	FAN_PWM
K6	GPA4	PWM4	GPI	EC_LPC_PME#
J6	GPA5	PWM5	GPI	MOD_SPI_CSEN0#
M7	GPA6	PWM6/SSCK	GPI	10G_CAP01
K7	GPA7	PWM7/RIG1#	GPI	CAR_SPI_CSEN0#
A4	GPB0	RXD/SIN0	GPI	SRXD1X
A3	GPB1	TXD/SOUT0	GPI	STXD1X
D2	GPB2	CTX0	GPI	EC_SLEEP#
B4	GPB3	SMCLK0	GPI	CB_THRM#
A2	GPB4	SMDAT0	GPI	EC_CPU_RST#
F1	GPB5	GA20	GPO	10G_PHY_01_RST_EC
H4	GPB6	KBRST#	KBRST	CB_WDT
A1	GPB7	RING#/PWRFIL /LPCRST#	GPI	EC_LID#
D1	GPC0	CRX0	GPI	CB_BATLOW#
B3	GPC1	SMCLK1	GPI	EC_CLK_3P3
B2	GPC2	SMDAT1	GPI	EC_DATA_3P3
K13	GPC3	KSO16/SMOSI	GPI	EC_CPU_THRMTRIP
C2	GPC4	TMRI0/WUI2	GPI	BIOS_DIS0#
J10	GPC5	KSO17/SMISO	GPI	10G_CAP23
E1	GPC6	TMR1/WUI3	GPI	BIOS_DIS1#
M2	GPC7	PWUREQ#	GPI	EC_PWRBTN#
E6	GPG0	SSCE1#/TM	GPI	
A5	GPG1	DTR1#/ID7	GPI	SYS_RESET#
E7	GPG2	SSCE0#	GPI	
D6	GPG6	DSR0#	GPI	

PIN NO.	PIN Name	Multi-Func	Default	GPIO Function
N1	GPD0	RI1#/WUI0	GPI	SLP_S3#
N3	GPD1	RI2#/WUI1	GPI	SLP_S4#
M4	GPD2	LPCRST#/WUI4	LPCRST#	BUF_PLT_RST#
N4	GPD3	ECSCI#	GPI	EC_SCI#
L2	GPD4	ECSMI#	GPI	EC_SMI#
N7	GPD5	GINT/CTS0#	GPI	EC_KBRST#
M11	GPD6	TACH0	GPI	EC_CPUFAN_TACH
M12	GPD7	TACH1	GPI	SLP_LAN#_EC
N2	GPE0	L80HLAT/WUI24	GPI	GPO0
A13	GPE1	EGAD	GPI	GPO1
A12	GPE2	EGCS#	GPI	GPO2
B12	GPE3	EGCLK	GPI	GPO3
E2	GPE4	PWRSW	GPI	FPANSWH#
N8	GPE5	WUI5/RTS1#	GPI	EC_PROCHOT
M1	GPE6	LPCRD#/WUI6	GPI	EC_NMI#
M3	GPE7	L80LLAT/WUI7	GPI	PS_ON#
A11	GPF0	PS2CLK0/TMB0	GPI	GPI0
B11	GPF1	PS2DAT0TMB1	GPI	GPI1
A10	GPF2	PS2CLK1/DTR0#	GPI	SUSACK#
B10	GPF3	PS2DAT1/RTS0#	GPI	Remove EC_A20GATE
D9	GPF4	PS2CLK2/WUI20	GPI	GPI2
B9	GPF5	PS2DAT2/WUI21	GPI	GPI3
B1	GPF6	SMCLK2/WUI22	GPI	PECI_EC
C1	GPF7	SMDAT2/WUI23	GPI	RSMRST_PWRGD#

PIN NO.	PIN Name	Multi-Func	Default	GPIO Function
D8	GPH0	CLKRUN#/ID0	GPI/ID0	EC_RSMRST#
E8	GPH1	CRX1/SIN1/SUI17	GPI/ID1	SRXD2X
D7	GPH2	CTX1/SOUT1/WUI19	GPI/ID2	STXD2X
A9	GPH3	ID3	GPI/ID3	PCH_PWROK
B8	GPH4	ID4	GPI/ID4	PWRGD_PS
A8	GPH5	ID5	GPI/ID5	EC_DPWROK
B7	GPH6	ID6	GPI/ID6	SYS_PWROK
G10	GPI0	ADC0	GPI ONLY	TH1_CPU
G13	GPI1	ADC1	GPI ONLY	TH2_COM
G12	GPI2	ADC2	GPI ONLY	VIN_SEN
F9	GPI3	ADC3	GPI ONLY	V5ALW_SEN
F13	GPI4	ADC4/WUI28	GPI ONLY	VDDR4_SEN
F10	GPI5	ADC5/DCD1#	GPI ONLY	
F12	GPI6	ADC6/DSR1#	GPI ONLY	VCORE_SEN
E13	GPI7	ADC7/CTS1#	GPI ONLY	VGT_SEN
E12	GPJ0	DAC0	GPI	SLP_SUS#
D13	GPJ1	DAC1	GPI	AutoBtn#
D12	GPJ2	DAC2	GPI	CB_SLP_S3#
C13	GPJ3	DAC3	GPI	CB_SLP_S4#
B13	GPJ4	DAC4/DCD0#	GPI	10G_PHY_23_RST_EC
C12	GPJ5	DAC5/RIG0#	GPI	GP_WAKE#

PCH GPIO Pins :

Group	Name	Power Well	Default	GPIO Function
Group A	GPP_A0			
	GPP_A1			
	GPP_A2			
	GPP_A3			
	GPP_A4			
	GPP_A5			
	GPP_A6			
	GPP_A7			
	GPP_A8			
	GPP_A9			
	GPP_A10			
	GPP_A11			
	GPP_A12			
	GPP_A13			
	GPP_A14			
	GPP_A15			
	GPP_A16			
	GPP_A17~A23			
Group B	GPP_B0			
	GPP_B1			
	GPP_B2			
	GPP_B3			
	GPP_B4			
	GPP_B5			
	GPP_B6~10			
	GPP_B11			
	GPP_B12			
	GPP_B13			
	GPP_B14			
	GPP_B15~22			
	GPP_B23			
Group C	GPP_C0			
	GPP_C1			
	GPP_C2			
	GPP_C3			
	GPP_C4			
	GPP_C5			
	GPP_C6			
	GPP_C7			
	GPP_C8~23			

PCH GPIO Pins :

Group	Name	Power Well	Default	GPIO Function
	GPP_D0~8			
	GPP_D9			
	GPP_D10			
	GPP_D11			
	GPP_D12			
	GPP_D13~16			
	GPP_D17~D23			
	GPP_E0~3			
	GPP_E4			
	GPP_E5			
	GPP_E6~7			
	GPP_E8			
	GPP_E9			
	GPP_E10			
	GPP_E11			
	GPP_E12			
	GPP_F0~14			
	GPP_F15			
	GPP_F16			
	GPP_F17			
	GPP_F18			
	GPP_F19			
	GPP_F20			
	GPP_F21			
	GPP_F22~23			
Group G	GPP_G0~23			
Group H	GPP_H0~23			
Group I	GPP_I0			
	GPP_I1			
	GPP_I2			
	GPP_I3			
	GPP_I4			
	GPP_I5			
	GPP_I6			
	GPP_I7			
	GPP_I8			
	GPP_I9			
	GPP_I10			

<Core Design>

AAEON Technology INC.
Title: System Setting
Size: C
Document Number: COM-ICDB7
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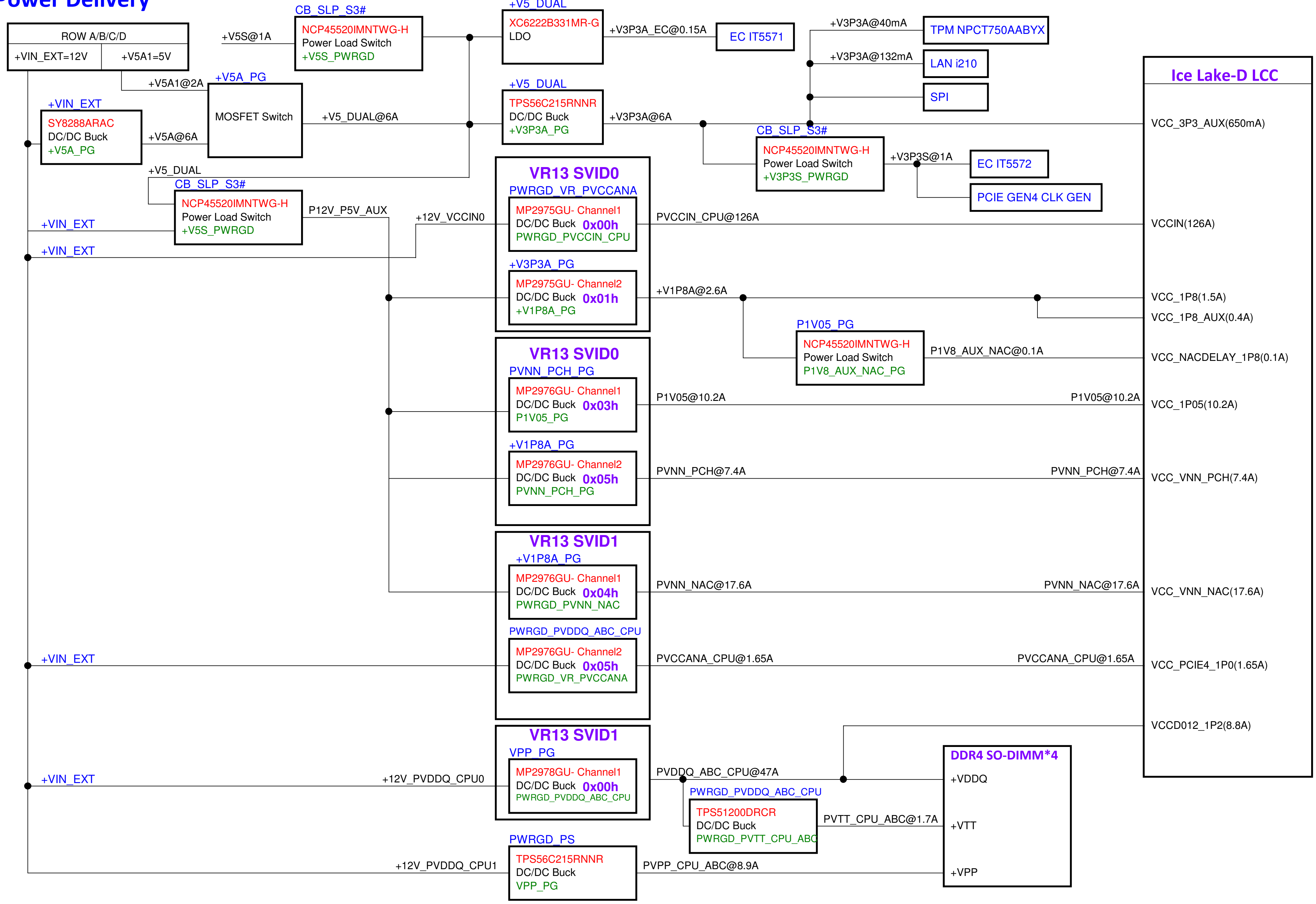
Power Delivery


ROW A/B/C/D
+VIN_EXT=12V
+V5A1=5V
+V5S@1A
CB_SLP_S3#
NCP45520IMNTWG-H
Power Load Switch
+V5S_PWRGD
+V5_DUAL
XC6222B331MR-G
LDO
+V3P3A_EC@0.15A
EC IT5571
+V3P3A@40mA
TPM NPCT750AABYX
+V3P3A@132mA
LAN i210
SPI
+V5A1@2A
+V5A_PG
MOSFET Switch
+V5_DUAL@6A
+VIN_EXT
SY8288ARAC
DC/DC Buck
+V5A_PG
+V5A@6A
+V5_DUAL
TPS56C215RNNR
DC/DC Buck
+V3P3A_PG
+V3P3A@6A
CB_SLP_S3#
NCP45520IMNTWG-H
Power Load Switch
+V3P3S_PWRGD
+V3P3S@1A
EC IT5572
PCIE GEN4 CLK GEN
Ice Lake-D LCC
VCC_3P3_AUX(650mA)
+V5_DUAL
CB_SLP_S3#
NCP45520IMNTWG-H
Power Load Switch
+V5S_PWRGD
P12V_P5V_AUX
+VIN_EXT
+VIN_EXT
+12V_VCCIN0
VR13 SVID0
PWRGD_VR_PVCCANA
MP2975GU- Channel1
DC/DC Buck 0x00h
PWRGD_PVCCIN_CPU
PVCCIN_CPU@126A
VCCIN(126A)
+V3P3A_PG
MP2975GU- Channel2
DC/DC Buck 0x01h
+V1P8A_PG
+V1P8A@2.6A
VCC_1P8(1.5A)
VCC_1P8_AUX(0.4A)
P1V05_PG
NCP45520IMNTWG-H
Power Load Switch
P1V8_AUX_NAC_PG
P1V8_AUX_NAC@0.1A
VCC_NACDELAY_1P8(0.1A)
VR13 SVID0
PVNN_PCH_PG
MP2976GU- Channel1
DC/DC Buck 0x03h
P1V05_PG
P1V05@10.2A
P1V05@10.2A
VCC_1P05(10.2A)
+V1P8A_PG
MP2976GU- Channel2
DC/DC Buck 0x05h
PVNN_PCH_PG
PVNN_PCH@7.4A
PVNN_PCH@7.4A
VCC_VNN_PCH(7.4A)
VR13 SVID1
+V1P8A_PG
MP2976GU- Channel1
DC/DC Buck 0x04h
PWRGD_PVNN_NAC
PVNN_NAC@17.6A
PVNN_NAC@17.6A
VCC_VNN_NAC(17.6A)
PWRGD_PVDDQ_ABC_CPU
+VIN_EXT
MP2976GU- Channel2
DC/DC Buck 0x05h
PWRGD_VR_PVCCANA
PVCCANA_CPU@1.65A
PVCCANA_CPU@1.65A
VCC_PCIE4_1P0(1.65A)
VCCD012_1P2(8.8A)
VR13 SVID1
VPP_PG
+VIN_EXT
+12V_PVDDQ_CPU0
MP2978GU- Channel1
DC/DC Buck 0x00h
PWRGD_PVDDQ_ABC_CPU
PVDDQ_ABC_CPU@47A
DDR4 SO-DIMM*4
+VDDQ
PWRGD_PVDDQ_ABC_CPU
TPS51200DRCR
DC/DC Buck
PWRGD_PVTT_CPU_ABC
PVTT_CPU_ABC@1.7A
+VTT
PWRGD_PS
+12V_PVDDQ_CPU1
TPS56C215RNNR
DC/DC Buck
VPP_PG
PVPP_CPU_ABC@8.9A
+VPP

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Title
Power Delivery

Size C
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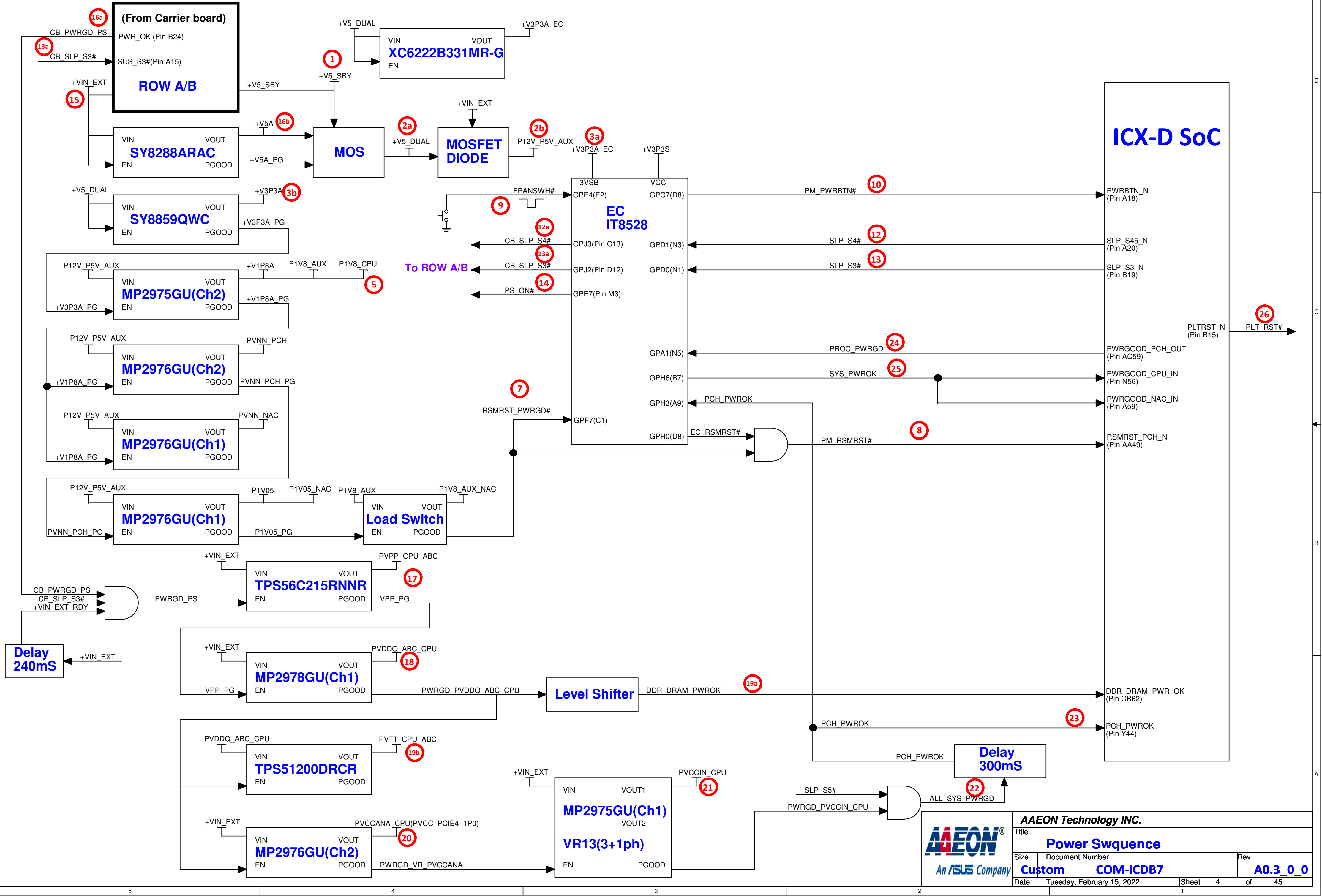
Power Sequence


(From Carrier board)
PWR_OK (Pin B24)
SUS_S3#(Pin A15)
ROW A/B
16a
CB_PWRGD_PS
13a
CB_SLP_S3#
+VIN_EXT
15
+V5_SBY
+V5_DUAL
VIN
VOUT
XC6222B331MR-G
EN
+V3P3A_EC
1
+V5_SBY
+V5A
16b
SY8288ARAC
PGOOD
+V5A_PG
MOS
2a
+V5_DUAL
+VIN_EXT
MOSFET DIODE
2b
P12V_P5V_AUX
3a
+V3P3A_EC
+V3P3S
3VSB
VCC
+V5_DUAL
+V3P3A
3b
SY8859QWC
+V3P3A_PG
FPANSWH#
GPE4(E2)
GPC7(D8)
9
EC
IT8528
PM_PWRBTN#
10
12a
CB_SLP_S4#
GPJ3(Pin C13)
GPD1(N3)
SLP_S4#
12
13a
To ROW A/B
CB_SLP_S3#
GPJ2(Pin D12)
GPD0(N1)
SLP_S3#
13
14
PS_ON#
GPE7(Pin M3)
P12V_P5V_AUX
+V1P8A
P1V8_AUX
P1V8_CPU
5
MP2975GU(Ch2)
+V3P3A_PG
+V1P8A_PG
P12V_P5V_AUX
PVNN_PCH
MP2976GU(Ch2)
+V1P8A_PG
PVNN_PCH_PG
P12V_P5V_AUX
PVNN_NAC
MP2976GU(Ch1)
+V1P8A_PG
7
RSMRST_PWRGD#
GPF7(C1)
GPA1(N5)
PROC_PWRGD
24
GPH6(B7)
SYS_PWROK
25
GPH3(A9)
PCH_PWROK
GPH0(D8)
EC_RSMRST#
PM_RSMRST#
8
P12V_P5V_AUX
P1V05
P1V05_NAC
P1V8_AUX
P1V8_AUX_NAC
MP2976GU(Ch1)
PVNN_PCH_PG
P1V05_PG
Load Switch
ICX-D SoC
PWRBTN_N
(Pin A18)
SLP_S45_N
(Pin A20)
SLP_S3_N
(Pin B19)
PLTRST_N
(Pin B15)
PLT_RST#
26
PWRGOOD_PCH_OUT
(Pin AC59)
PWRGOOD_CPU_IN
(Pin N56)
PWRGOOD_NAC_IN
(Pin A59)
RSMRST_PCH_N
(Pin AA49)
+VIN_EXT
PVPP_CPU_ABC
TPS56C215RNNR
17
CB_PWRGD_PS
CB_SLP_S3#
+VIN_EXT_RDY
PWRGD_PS
VPP_PG
Delay
240mS
+VIN_EXT
+VIN_EXT
PVDDQ_ABC_CPU
18
MP2978GU(Ch1)
VPP_PG
PWRGD_PVDDQ_ABC_CPU
Level Shifter
DDR_DRAM_PWROK
19a
DDR_DRAM_PWR_OK
(Pin CB62)
PCH_PWROK
23
PCH_PWROK
(Pin Y44)
PVDDQ_ABC_CPU
PVTT_CPU_ABC
19b
TPS51200DRCR
Delay
300mS
PCH_PWROK
+VIN_EXT
PVCCIN_CPU
21
MP2975GU(Ch1)
VOUT1
VOUT2
VR13(3+1ph)
SLP_S5#
ALL_SYS_PWRGD
22
PWRGD_PVCCIN_CPU
+VIN_EXT
PVCCANA_CPU(PVCC_PCIE4_1P0)
20
MP2976GU(Ch2)
PWRGD_VR_PVCCANA

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Title	**Power Swquence**	
Size	Document Number	Rev
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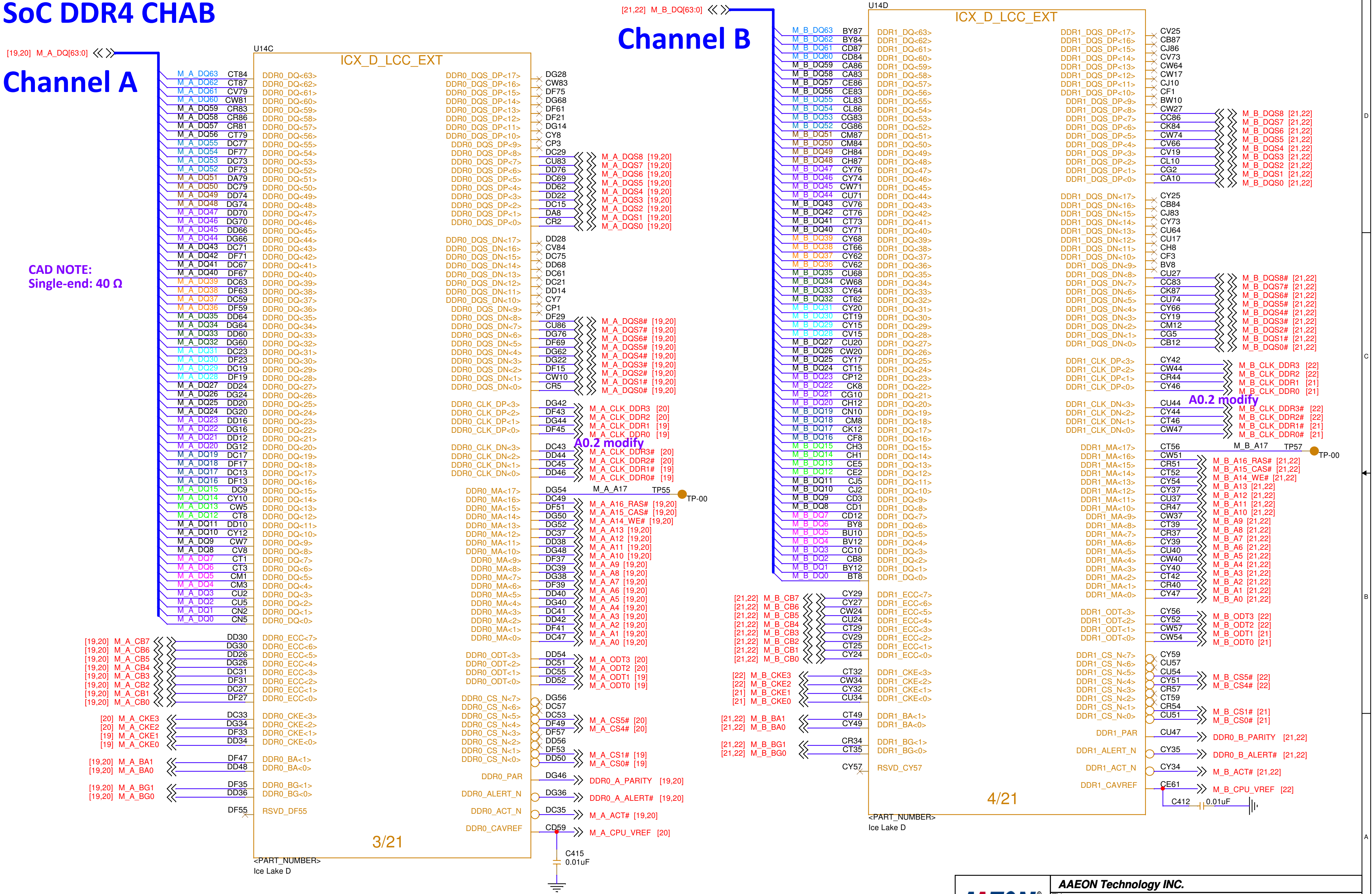
SoC DDR4 CHAB


Channel A
Channel B
[19,20] M_A_DQ[63:0]
[21,22] M_B_DQ[63:0]
U14C
ICX_D_LCC_EXT
3/21
<PART_NUMBER>
Ice Lake D
U14D
ICX_D_LCC_EXT
4/21
<PART_NUMBER>
Ice Lake D
CAD NOTE:
Single-end: 40 Ω
A0.2 modify
A0.2 modify
DDR0_DQ<63..0>
DDR0_DQS_DP<17..0>
DDR0_DQS_DN<17..0>
DDR0_CLK_DP<3..0>
DDR0_CLK_DN<3..0>
DDR0_MA<17..0>
DDR0_ECC<7..0>
DDR0_ODT<3..0>
DDR0_CS_N<7..0>
DDR0_CKE<3..0>
DDR0_BA<1..0>
DDR0_BG<1..0>
DDR0_PAR
DDR0_ALERT_N
DDR0_ACT_N
DDR0_CAVREF
RSVD_DF55
M_A_DQS8..M_A_DQS0 [19,20]
M_A_DQS8#..M_A_DQS0# [19,20]
M_A_CLK_DDR3 [20]
M_A_CLK_DDR2 [20]
M_A_CLK_DDR1 [19]
M_A_CLK_DDR0 [19]
M_A_CLK_DDR3# [20]
M_A_CLK_DDR2# [20]
M_A_CLK_DDR1# [19]
M_A_CLK_DDR0# [19]
M_A_A17
TP55
TP-00
M_A_A16_RAS# [19,20]
M_A_A15_CAS# [19,20]
M_A_A14_WE# [19,20]
M_A_A13..M_A_A0 [19,20]
M_A_ODT3 [20]
M_A_ODT2 [20]
M_A_ODT1 [19]
M_A_ODT0 [19]
M_A_CS5# [20]
M_A_CS4# [20]
M_A_CS1# [19]
M_A_CS0# [19]
DDR0_A_PARITY [19,20]
DDR0_A_ALERT# [19,20]
M_A_ACT# [19,20]
M_A_CPU_VREF [20]
C415
0.01uF
[19,20] M_A_CB7..M_A_CB0
[20] M_A_CKE3
[20] M_A_CKE2
[19] M_A_CKE1
[19] M_A_CKE0
[19,20] M_A_BA1
[19,20] M_A_BA0
[19,20] M_A_BG1
[19,20] M_A_BG0
DDR1_DQ<63..0>
DDR1_DQS_DP<17..0>
DDR1_DQS_DN<17..0>
DDR1_CLK_DP<3..0>
DDR1_CLK_DN<3..0>
DDR1_MA<17..0>
DDR1_ECC<7..0>
DDR1_ODT<3..0>
DDR1_CS_N<7..0>
DDR1_CKE<3..0>
DDR1_BA<1..0>
DDR1_BG<1..0>
DDR1_PAR
DDR1_ALERT_N
DDR1_ACT_N
DDR1_CAVREF
RSVD_CY57
M_B_DQS8..M_B_DQS0 [21,22]
M_B_DQS8#..M_B_DQS0# [21,22]
M_B_CLK_DDR3 [22]
M_B_CLK_DDR2 [22]
M_B_CLK_DDR1 [21]
M_B_CLK_DDR0 [21]
M_B_CLK_DDR3# [22]
M_B_CLK_DDR2# [22]
M_B_CLK_DDR1# [21]
M_B_CLK_DDR0# [21]
M_B_A17
TP57
TP-00
M_B_A16_RAS# [21,22]
M_B_A15_CAS# [21,22]
M_B_A14_WE# [21,22]
M_B_A13..M_B_A0 [21,22]
M_B_ODT3 [22]
M_B_ODT2 [22]
M_B_ODT1 [21]
M_B_ODT0 [21]
M_B_CS5# [22]
M_B_CS4# [22]
M_B_CS1# [21]
M_B_CS0# [21]
DDR0_B_PARITY [21,22]
DDR0_B_ALERT# [21,22]
M_B_ACT# [21,22]
M_B_CPU_VREF [22]
C412
0.01uF
[21,22] M_B_CB7..M_B_CB0
[22] M_B_CKE3
[22] M_B_CKE2
[21] M_B_CKE1
[21] M_B_CKE0
[21,22] M_B_BA1
[21,22] M_B_BA0
[21,22] M_B_BG1
[21,22] M_B_BG0

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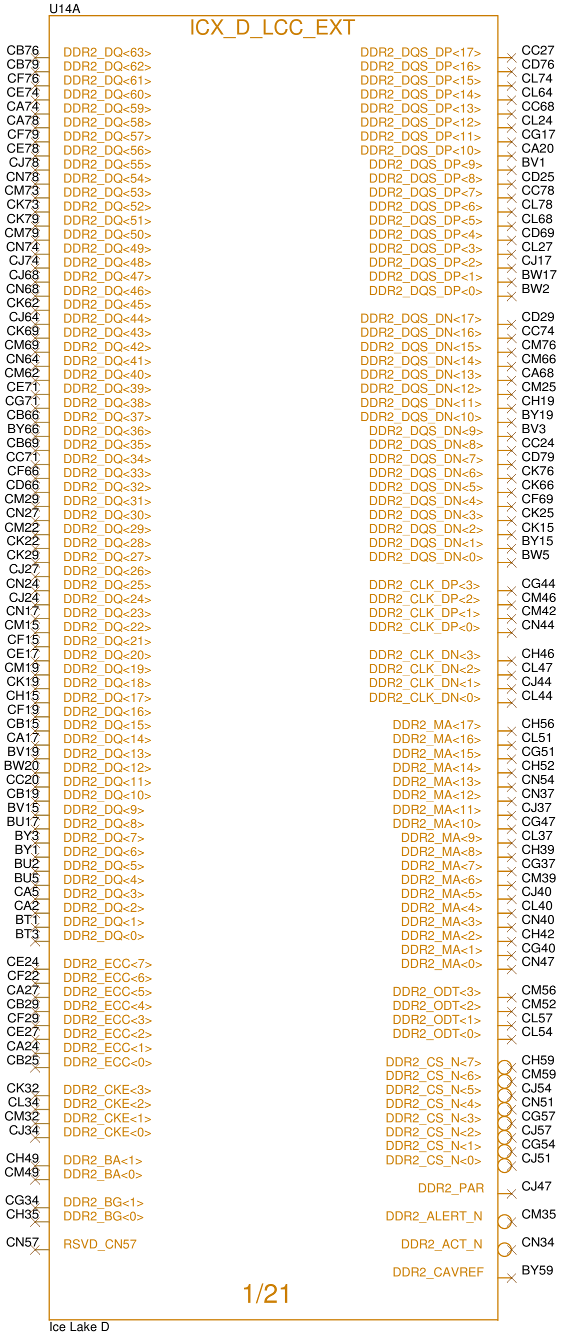
SoC DDR4 CHC

Channel C


U14A
ICX_D_LCC_EXT
CB76 DDR2_DQ<63>
CB79 DDR2_DQ<62>
CF76 DDR2_DQ<61>
CE74 DDR2_DQ<60>
CA74 DDR2_DQ<59>
CA78 DDR2_DQ<58>
CF79 DDR2_DQ<57>
CE78 DDR2_DQ<56>
CJ78 DDR2_DQ<55>
CN78 DDR2_DQ<54>
CM73 DDR2_DQ<53>
CK73 DDR2_DQ<52>
CK79 DDR2_DQ<51>
CM79 DDR2_DQ<50>
CN74 DDR2_DQ<49>
CJ74 DDR2_DQ<48>
CJ68 DDR2_DQ<47>
CN68 DDR2_DQ<46>
CK62 DDR2_DQ<45>
CJ64 DDR2_DQ<44>
CK69 DDR2_DQ<43>
CM69 DDR2_DQ<42>
CN64 DDR2_DQ<41>
CM62 DDR2_DQ<40>
CE71 DDR2_DQ<39>
CG71 DDR2_DQ<38>
CB66 DDR2_DQ<37>
BY66 DDR2_DQ<36>
CB69 DDR2_DQ<35>
CC71 DDR2_DQ<34>
CF66 DDR2_DQ<33>
CD66 DDR2_DQ<32>
CM29 DDR2_DQ<31>
CN27 DDR2_DQ<30>
CM22 DDR2_DQ<29>
CK22 DDR2_DQ<28>
CK29 DDR2_DQ<27>
CJ27 DDR2_DQ<26>
CN24 DDR2_DQ<25>
CJ24 DDR2_DQ<24>
CN17 DDR2_DQ<23>
CM15 DDR2_DQ<22>
CF15 DDR2_DQ<21>
CE17 DDR2_DQ<20>
CM19 DDR2_DQ<19>
CK19 DDR2_DQ<18>
CH15 DDR2_DQ<17>
CF19 DDR2_DQ<16>
CB15 DDR2_DQ<15>
CA17 DDR2_DQ<14>
BV19 DDR2_DQ<13>
BW20 DDR2_DQ<12>
CC20 DDR2_DQ<11>
CB19 DDR2_DQ<10>
BV15 DDR2_DQ<9>
BU17 DDR2_DQ<8>
BY3 DDR2_DQ<7>
BY1 DDR2_DQ<6>
BU2 DDR2_DQ<5>
BU5 DDR2_DQ<4>
CA5 DDR2_DQ<3>
CA2 DDR2_DQ<2>
BT1 DDR2_DQ<1>
BT3 DDR2_DQ<0>
CE24 DDR2_ECC<7>
CF22 DDR2_ECC<6>
CA27 DDR2_ECC<5>
CB29 DDR2_ECC<4>
CF29 DDR2_ECC<3>
CE27 DDR2_ECC<2>
CA24 DDR2_ECC<1>
CB25 DDR2_ECC<0>
CK32 DDR2_CKE<3>
CL34 DDR2_CKE<2>
CM32 DDR2_CKE<1>
CJ34 DDR2_CKE<0>
CH49 DDR2_BA<1>
CM49 DDR2_BA<0>
CG34 DDR2_BG<1>
CH35 DDR2_BG<0>
CN57 RSVD_CN57
DDR2_DQS_DP<17> CC27
DDR2_DQS_DP<16> CD76
DDR2_DQS_DP<15> CL74
DDR2_DQS_DP<14> CL64
DDR2_DQS_DP<13> CC68
DDR2_DQS_DP<12> CL24
DDR2_DQS_DP<11> CG17
DDR2_DQS_DP<10> CA20
DDR2_DQS_DP<9> BV1
DDR2_DQS_DP<8> CD25
DDR2_DQS_DP<7> CC78
DDR2_DQS_DP<6> CL78
DDR2_DQS_DP<5> CL68
DDR2_DQS_DP<4> CD69
DDR2_DQS_DP<3> CL27
DDR2_DQS_DP<2> CJ17
DDR2_DQS_DP<1> BW17
DDR2_DQS_DP<0> BW2
DDR2_DQS_DN<17> CD29
DDR2_DQS_DN<16> CC74
DDR2_DQS_DN<15> CM76
DDR2_DQS_DN<14> CM66
DDR2_DQS_DN<13> CA68
DDR2_DQS_DN<12> CM25
DDR2_DQS_DN<11> CH19
DDR2_DQS_DN<10> BY19
DDR2_DQS_DN<9> BV3
DDR2_DQS_DN<8> CC24
DDR2_DQS_DN<7> CD79
DDR2_DQS_DN<6> CK76
DDR2_DQS_DN<5> CK66
DDR2_DQS_DN<4> CF69
DDR2_DQS_DN<3> CK25
DDR2_DQS_DN<2> CK15
DDR2_DQS_DN<1> BY15
DDR2_DQS_DN<0> BW5
DDR2_CLK_DP<3> CG44
DDR2_CLK_DP<2> CM46
DDR2_CLK_DP<1> CM42
DDR2_CLK_DP<0> CN44
DDR2_CLK_DN<3> CH46
DDR2_CLK_DN<2> CL47
DDR2_CLK_DN<1> CJ44
DDR2_CLK_DN<0> CL44
DDR2_MA<17> CH56
DDR2_MA<16> CL51
DDR2_MA<15> CG51
DDR2_MA<14> CH52
DDR2_MA<13> CN54
DDR2_MA<12> CN37
DDR2_MA<11> CJ37
DDR2_MA<10> CG47
DDR2_MA<9> CL37
DDR2_MA<8> CH39
DDR2_MA<7> CG37
DDR2_MA<6> CM39
DDR2_MA<5> CJ40
DDR2_MA<4> CL40
DDR2_MA<3> CN40
DDR2_MA<2> CH42
DDR2_MA<1> CG40
DDR2_MA<0> CN47
DDR2_ODT<3> CM56
DDR2_ODT<2> CM52
DDR2_ODT<1> CL57
DDR2_ODT<0> CL54
DDR2_CS_N<7> CH59
DDR2_CS_N<6> CM59
DDR2_CS_N<5> CJ54
DDR2_CS_N<4> CN51
DDR2_CS_N<3> CG57
DDR2_CS_N<2> CJ57
DDR2_CS_N<1> CG54
DDR2_CS_N<0> CJ51
DDR2_PAR CJ47
DDR2_ALERT_N CM35
DDR2_ACT_N CN34
DDR2_CAVREF BY59
1/21
Ice Lake D

AAEON Technology INC.

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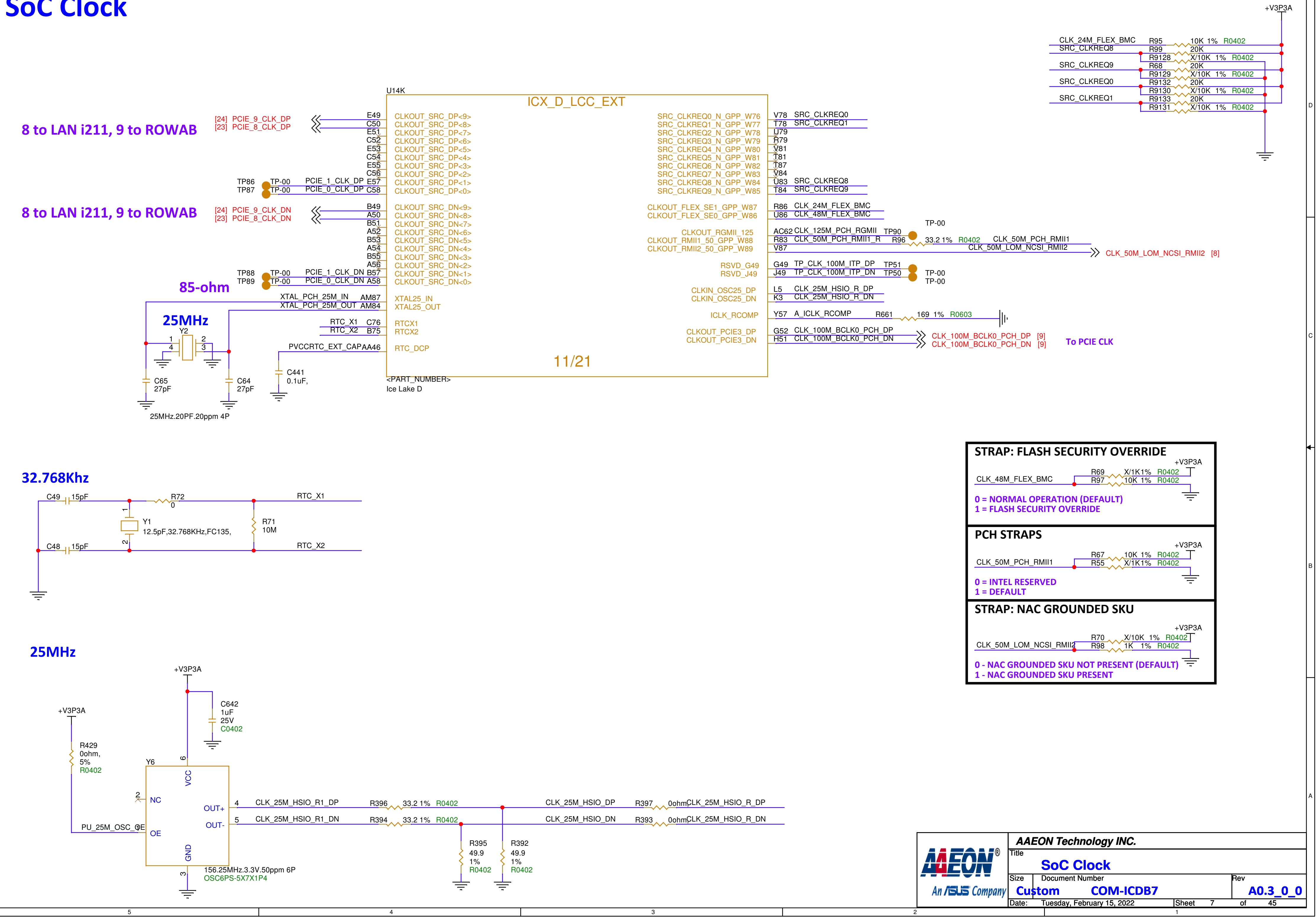
SoC Clock



U14K
ICX_D_LCC_EXT
8 to LAN i211, 9 to ROWAB
[24] PCIE_9_CLK_DP
[23] PCIE_8_CLK_DP
E49 CLKOUT_SRC_DP<9>
C50 CLKOUT_SRC_DP<8>
E51 CLKOUT_SRC_DP<7>
C52 CLKOUT_SRC_DP<6>
E53 CLKOUT_SRC_DP<5>
C54 CLKOUT_SRC_DP<4>
E55 CLKOUT_SRC_DP<3>
C56 CLKOUT_SRC_DP<2>
TP86 TP-00 PCIE_1_CLK_DP E57 CLKOUT_SRC_DP<1>
TP87 TP-00 PCIE_0_CLK_DP C58 CLKOUT_SRC_DP<0>
8 to LAN i211, 9 to ROWAB
[24] PCIE_9_CLK_DN
[23] PCIE_8_CLK_DN
B49 CLKOUT_SRC_DN<9>
A50 CLKOUT_SRC_DN<8>
B51 CLKOUT_SRC_DN<7>
A52 CLKOUT_SRC_DN<6>
B53 CLKOUT_SRC_DN<5>
A54 CLKOUT_SRC_DN<4>
B55 CLKOUT_SRC_DN<3>
A56 CLKOUT_SRC_DN<2>
TP88 TP-00 PCIE_1_CLK_DN B57 CLKOUT_SRC_DN<1>
TP89 TP-00 PCIE_0_CLK_DN A58 CLKOUT_SRC_DN<0>
85-ohm
XTAL_PCH_25M_IN AM87 XTAL25_IN
XTAL_PCH_25M_OUT AM84 XTAL25_OUT
25MHz
Y2
RTC_X1 C76 RTCX1
RTC_X2 B75 RTCX2
PVCCRTC_EXT_CAPA AA46 RTC_DCP
C441 0.1uF,
C65 27pF
C64 27pF
25MHz.20PF.20ppm 4P
11/21
<PART_NUMBER>
Ice Lake D
SRC_CLKREQ0_N_GPP_W76 V78 SRC_CLKREQ0
SRC_CLKREQ1_N_GPP_W77 T78 SRC_CLKREQ1
SRC_CLKREQ2_N_GPP_W78 U79
SRC_CLKREQ3_N_GPP_W79 R79
SRC_CLKREQ4_N_GPP_W80 V81
SRC_CLKREQ5_N_GPP_W81 T81
SRC_CLKREQ6_N_GPP_W82 T87
SRC_CLKREQ7_N_GPP_W83 V84
SRC_CLKREQ8_N_GPP_W84 U83 SRC_CLKREQ8
SRC_CLKREQ9_N_GPP_W85 T84 SRC_CLKREQ9
CLKOUT_FLEX_SE1_GPP_W87 R86 CLK_24M_FLEX_BMC
CLKOUT_FLEX_SE0_GPP_W86 U86 CLK_48M_FLEX_BMC
TP-00
CLKOUT_RGMII_125 AC62 CLK_125M_PCH_RGMII TP90
CLKOUT_RMII1_50_GPP_W88 R83 CLK_50M_PCH_RMII1_R R96 33.2 1% R0402 CLK_50M_PCH_RMII1
CLKOUT_RMII2_50_GPP_W89 V87 CLK_50M_LOM_NCSI_RMII2
CLK_50M_LOM_NCSI_RMII2 [8]
RSVD_G49 G49 TP_CLK_100M_ITP_DP TP51
RSVD_J49 J49 TP_CLK_100M_ITP_DN TP50
TP-00
TP-00
CLKIN_OSC25_DP L5 CLK_25M_HSIO_R_DP
CLKIN_OSC25_DN K3 CLK_25M_HSIO_R_DN
ICLK_RCOMP Y57 A_ICLK_RCOMP R661 169 1% R0603
CLKOUT_PCIE3_DP G52 CLK_100M_BCLK0_PCH_DP
CLKOUT_PCIE3_DN H51 CLK_100M_BCLK0_PCH_DN
CLK_100M_BCLK0_PCH_DP [9]
CLK_100M_BCLK0_PCH_DN [9]
To PCIE CLK
+V3P3A
CLK_24M_FLEX_BMC R95 10K 1% R0402
SRC_CLKREQ8 R99 20K
R9128 X/10K 1% R0402
SRC_CLKREQ9 R68 20K
R9129 X/10K 1% R0402
SRC_CLKREQ0 R9132 20K
R9130 X/10K 1% R0402
SRC_CLKREQ1 R9133 20K
R9131 X/10K 1% R0402
32.768Khz
C49 15pF
R72 0
RTC_X1
Y1 12.5pF,32.768KHz,FC135,
R71 10M
C48 15pF
RTC_X2
25MHz
+V3P3A
C642 1uF 25V C0402
+V3P3A
R429 0ohm, 5% R0402
Y6
VCC
NC
OE
OUT+
OUT-
GND
PU_25M_OSC_OE
4 CLK_25M_HSIO_R1_DP R396 33.2 1% R0402
5 CLK_25M_HSIO_R1_DN R394 33.2 1% R0402
CLK_25M_HSIO_DP R397 0ohm CLK_25M_HSIO_R_DP
CLK_25M_HSIO_DN R393 0ohm CLK_25M_HSIO_R_DN
R395 49.9 1% R0402
R392 49.9 1% R0402
156.25MHz.3.3V.50ppm 6P
OSC6PS-5X7X1P4
STRAP: FLASH SECURITY OVERRIDE
+V3P3A
CLK_48M_FLEX_BMC R69 X/1K1% R0402
R97 10K 1% R0402
0 = NORMAL OPERATION (DEFAULT)
1 = FLASH SECURITY OVERRIDE
PCH STRAPS
+V3P3A
CLK_50M_PCH_RMII1 R67 10K 1% R0402
R55 X/1K1% R0402
0 = INTEL RESERVED
1 = DEFAULT
STRAP: NAC GROUNDED SKU
+V3P3A
CLK_50M_LOM_NCSI_RMII2 R70 X/10K 1% R0402
R98 1K 1% R0402
0 - NAC GROUNDED SKU NOT PRESENT (DEFAULT)
1 - NAC GROUNDED SKU PRESENT

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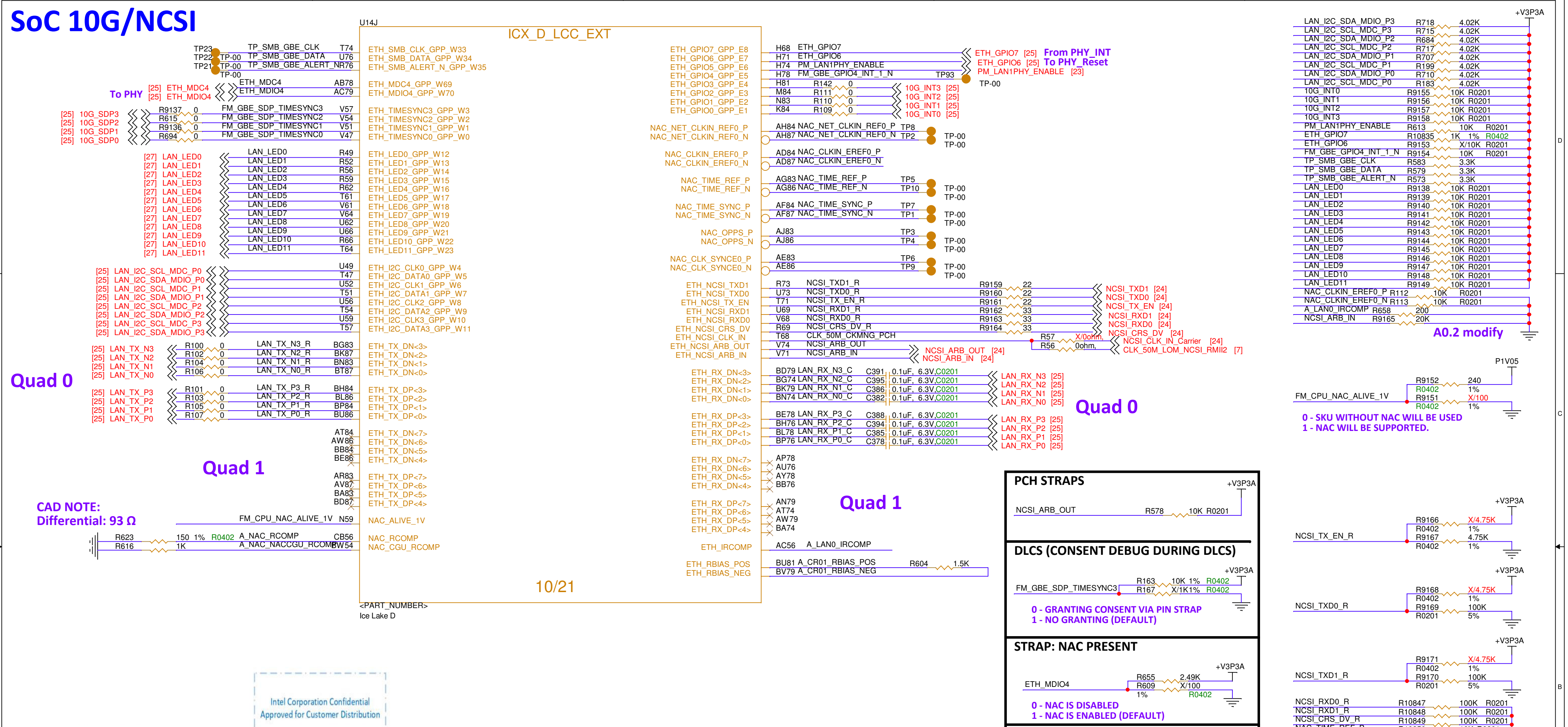
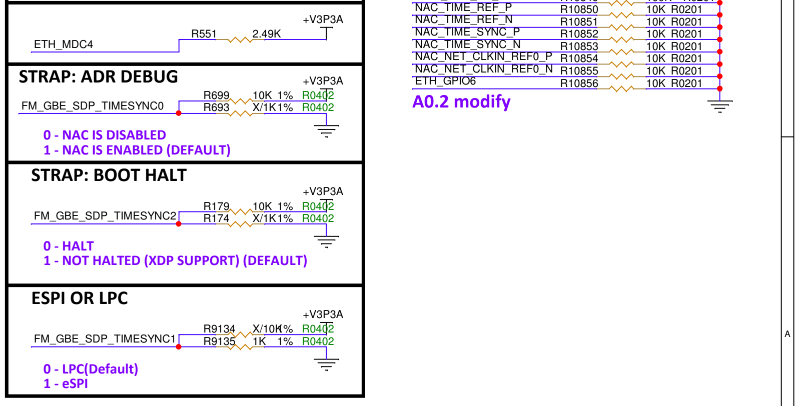
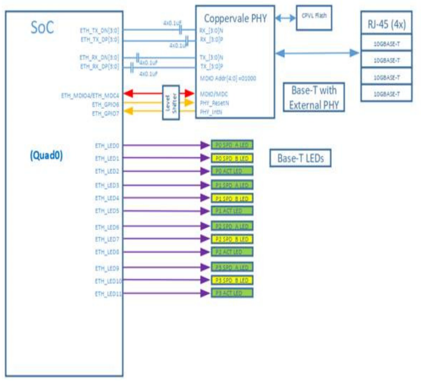
SoC 10G/NCSI


U14J
ICX_D_LCC_EXT
TP23 TP_SMB_GBE_CLK T74 ETH_SMB_CLK_GPP_W33
TP22 TP-00 TP_SMB_GBE_DATA U76 ETH_SMB_DATA_GPP_W34
TP21 TP-00 TP_SMB_GBE_ALERT_NR76 ETH_SMB_ALERT_N_GPP_W35
TP-00
To PHY [25] ETH_MDC4 ETH_MDC4 AB78 ETH_MDC4_GPP_W69
[25] ETH_MDIO4 ETH_MDIO4 AC79 ETH_MDIO4_GPP_W70
[25] 10G_SDP3 R9137 0 FM_GBE_SDP_TIMESYNC3 V57 ETH_TIMESYNC3_GPP_W3
[25] 10G_SDP2 R615 0 FM_GBE_SDP_TIMESYNC2 V54 ETH_TIMESYNC2_GPP_W2
[25] 10G_SDP1 R9136 0 FM_GBE_SDP_TIMESYNC1 V51 ETH_TIMESYNC1_GPP_W1
[25] 10G_SDP0 R694 0 FM_GBE_SDP_TIMESYNC0 V47 ETH_TIMESYNC0_GPP_W0
[27] LAN_LED0 LAN_LED0 R49 ETH_LED0_GPP_W12
[27] LAN_LED1 LAN_LED1 R52 ETH_LED1_GPP_W13
[27] LAN_LED2 LAN_LED2 R56 ETH_LED2_GPP_W14
[27] LAN_LED3 LAN_LED3 R59 ETH_LED3_GPP_W15
[27] LAN_LED4 LAN_LED4 R62 ETH_LED4_GPP_W16
[27] LAN_LED5 LAN_LED5 T61 ETH_LED5_GPP_W17
[27] LAN_LED6 LAN_LED6 V61 ETH_LED6_GPP_W18
[27] LAN_LED7 LAN_LED7 V64 ETH_LED7_GPP_W19
[27] LAN_LED8 LAN_LED8 U62 ETH_LED8_GPP_W20
[27] LAN_LED9 LAN_LED9 U66 ETH_LED9_GPP_W21
[27] LAN_LED10 LAN_LED10 R66 ETH_LED10_GPP_W22
[27] LAN_LED11 LAN_LED11 T64 ETH_LED11_GPP_W23
[25] LAN_I2C_SCL_MDC_P0 U49 ETH_I2C_CLK0_GPP_W4
[25] LAN_I2C_SDA_MDIO_P0 T47 ETH_I2C_DATA0_GPP_W5
[25] LAN_I2C_SCL_MDC_P1 U52 ETH_I2C_CLK1_GPP_W6
[25] LAN_I2C_SDA_MDIO_P1 T51 ETH_I2C_DATA1_GPP_W7
[25] LAN_I2C_SCL_MDC_P2 U56 ETH_I2C_CLK2_GPP_W8
[25] LAN_I2C_SDA_MDIO_P2 T54 ETH_I2C_DATA2_GPP_W9
[25] LAN_I2C_SCL_MDC_P3 U59 ETH_I2C_CLK3_GPP_W10
[25] LAN_I2C_SDA_MDIO_P3 T57 ETH_I2C_DATA3_GPP_W11
[25] LAN_TX_N3 R100 0 LAN_TX_N3_R BG83 ETH_TX_DN<3>
[25] LAN_TX_N2 R102 0 LAN_TX_N2_R BK87 ETH_TX_DN<2>
[25] LAN_TX_N1 R104 0 LAN_TX_N1_R BN83 ETH_TX_DN<1>
[25] LAN_TX_N0 R106 0 LAN_TX_N0_R BT87 ETH_TX_DN<0>
Quad 0
[25] LAN_TX_P3 R101 0 LAN_TX_P3_R BH84 ETH_TX_DP<3>
[25] LAN_TX_P2 R103 0 LAN_TX_P2_R BL86 ETH_TX_DP<2>
[25] LAN_TX_P1 R105 0 LAN_TX_P1_R BP84 ETH_TX_DP<1>
[25] LAN_TX_P0 R107 0 LAN_TX_P0_R BU86 ETH_TX_DP<0>
AT84 ETH_TX_DN<7>
AW86 ETH_TX_DN<6>
BB84 ETH_TX_DN<5>
BE86 ETH_TX_DN<4>
Quad 1
AR83 ETH_TX_DP<7>
AV87 ETH_TX_DP<6>
BA83 ETH_TX_DP<5>
BD87 ETH_TX_DP<4>
CAD NOTE:
Differential: 93 Ω
FM_CPU_NAC_ALIVE_1V N59 NAC_ALIVE_1V
R623 150 1% R0402 A_NAC_RCOMP CB56 NAC_RCOMP
R616 1K A_NAC_NACCGU_RCOMP BW54 NAC_CGU_RCOMP
10/21
<PART_NUMBER>
Ice Lake D
ETH_GPIO7_GPP_E8 H68 ETH_GPIO7 ETH_GPIO7 [25] From PHY_INT
ETH_GPIO6_GPP_E7 H71 ETH_GPIO6 ETH_GPIO6 [25] To PHY_Reset
ETH_GPIO5_GPP_E6 H74 PM_LAN1PHY_ENABLE PM_LAN1PHY_ENABLE [23]
ETH_GPIO4_GPP_E5 H78 FM_GBE_GPIO4_INT_1_N TP93 TP-00
ETH_GPIO3_GPP_E4 H81 R142 0 10G_INT3 [25]
ETH_GPIO2_GPP_E3 M84 R111 0 10G_INT2 [25]
ETH_GPIO1_GPP_E2 N83 R110 0 10G_INT1 [25]
ETH_GPIO0_GPP_E1 K84 R109 0 10G_INT0 [25]
NAC_NET_CLKIN_REF0_P AH84 NAC_NET_CLKIN_REF0_P TP8 TP-00
NAC_NET_CLKIN_REF0_N AH87 NAC_NET_CLKIN_REF0_N TP2 TP-00
NAC_CLKIN_EREF0_P AD84 NAC_CLKIN_EREF0_P
NAC_CLKIN_EREF0_N AD87 NAC_CLKIN_EREF0_N
NAC_TIME_REF_P AG83 NAC_TIME_REF_P TP5 TP-00
NAC_TIME_REF_N AG86 NAC_TIME_REF_N TP10 TP-00
NAC_TIME_SYNC_P AF84 NAC_TIME_SYNC_P TP7 TP-00
NAC_TIME_SYNC_N AF87 NAC_TIME_SYNC_N TP1 TP-00
NAC_OPPS_P AJ83 TP3 TP-00
NAC_OPPS_N AJ86 TP4 TP-00
NAC_CLK_SYNCE0_P AE83 TP6 TP-00
NAC_CLK_SYNCE0_N AE86 TP9 TP-00
ETH_NCSI_TXD1 R73 NCSI_TXD1_R R9159 22 NCSI_TXD1 [24]
ETH_NCSI_TXD0 U73 NCSI_TXD0_R R9160 22 NCSI_TXD0 [24]
ETH_NCSI_TX_EN T71 NCSI_TX_EN_R R9161 22 NCSI_TX_EN [24]
ETH_NCSI_RXD1 U69 NCSI_RXD1_R R9162 33 NCSI_RXD1 [24]
ETH_NCSI_RXD0 V68 NCSI_RXD0_R R9163 33 NCSI_RXD0 [24]
ETH_NCSI_CRS_DV R69 NCSI_CRS_DV_R R9164 33 NCSI_CRS_DV [24]
ETH_NCSI_CLK_IN T68 CLK_50M_CKMNG_PCH R57 X/0ohm, NCSI_CLK_IN_Carrier [24]
R56 0ohm, CLK_50M_LOM_NCSI_RMII2 [7]
ETH_NCSI_ARB_OUT V74 NCSI_ARB_OUT NCSI_ARB_OUT [24]
ETH_NCSI_ARB_IN V71 NCSI_ARB_IN NCSI_ARB_IN [24]
ETH_RX_DN<3> BD79 LAN_RX_N3_C C391 0.1uF, 6.3V,C0201 LAN_RX_N3 [25]
ETH_RX_DN<2> BG74 LAN_RX_N2_C C395 0.1uF, 6.3V,C0201 LAN_RX_N2 [25]
ETH_RX_DN<1> BK79 LAN_RX_N1_C C386 0.1uF, 6.3V,C0201 LAN_RX_N1 [25]
ETH_RX_DN<0> BN74 LAN_RX_N0_C C382 0.1uF, 6.3V,C0201 LAN_RX_N0 [25]
Quad 0
ETH_RX_DP<3> BE78 LAN_RX_P3_C C388 0.1uF, 6.3V,C0201 LAN_RX_P3 [25]
ETH_RX_DP<2> BH76 LAN_RX_P2_C C394 0.1uF, 6.3V,C0201 LAN_RX_P2 [25]
ETH_RX_DP<1> BL78 LAN_RX_P1_C C385 0.1uF, 6.3V,C0201 LAN_RX_P1 [25]
ETH_RX_DP<0> BP76 LAN_RX_P0_C C378 0.1uF, 6.3V,C0201 LAN_RX_P0 [25]
ETH_RX_DN<7> AP78
ETH_RX_DN<6> AU76
ETH_RX_DN<5> AY78
ETH_RX_DN<4> BB76
Quad 1
ETH_RX_DP<7> AN79
ETH_RX_DP<6> AT74
ETH_RX_DP<5> AW79
ETH_RX_DP<4> BA74
ETH_IRCOMP AC56 A_LAN0_IRCOMP
ETH_RBIAS_POS BU81 A_CR01_RBIAS_POS R604 1.5K
ETH_RBIAS_NEG BV79 A_CR01_RBIAS_NEG
+V3P3A
LAN_I2C_SDA_MDIO_P3 R718 4.02K
LAN_I2C_SCL_MDC_P3 R715 4.02K
LAN_I2C_SDA_MDIO_P2 R684 4.02K
LAN_I2C_SCL_MDC_P2 R717 4.02K
LAN_I2C_SDA_MDIO_P1 R707 4.02K
LAN_I2C_SCL_MDC_P1 R199 4.02K
LAN_I2C_SDA_MDIO_P0 R710 4.02K
LAN_I2C_SCL_MDC_P0 R183 4.02K
10G_INT0 R9155 10K R0201
10G_INT1 R9156 10K R0201
10G_INT2 R9157 10K R0201
10G_INT3 R9158 10K R0201
PM_LAN1PHY_ENABLE R613 10K R0201
ETH_GPIO7 R10835 1K 1% R0402
ETH_GPIO6 R9153 X/10K R0201
FM_GBE_GPIO4_INT_1_N R9154 10K R0201
TP_SMB_GBE_CLK R583 3.3K
TP_SMB_GBE_DATA R579 3.3K
TP_SMB_GBE_ALERT_N R573 3.3K
LAN_LED0 R9138 10K R0201
LAN_LED1 R9139 10K R0201
LAN_LED2 R9140 10K R0201
LAN_LED3 R9141 10K R0201
LAN_LED4 R9142 10K R0201
LAN_LED5 R9143 10K R0201
LAN_LED6 R9144 10K R0201
LAN_LED7 R9145 10K R0201
LAN_LED8 R9146 10K R0201
LAN_LED9 R9147 10K R0201
LAN_LED10 R9148 10K R0201
LAN_LED11 R9149 10K R0201
NAC_CLKIN_EREF0_P R112 10K R0201
NAC_CLKIN_EREF0_N R113 10K R0201
A_LAN0_IRCOMP R658 200
NCSI_ARB_IN R9165 20K
A0.2 modify
P1V05
FM_CPU_NAC_ALIVE_1V R9152 240 R0402 1%
R9151 X/100 R0402 1%
0 - SKU WITHOUT NAC WILL BE USED
1 - NAC WILL BE SUPPORTED.
PCH STRAPS
+V3P3A
NCSI_ARB_OUT R578 10K R0201
DLCS (CONSENT DEBUG DURING DLCS)
+V3P3A
FM_GBE_SDP_TIMESYNC3 R163 10K 1% R0402
R167 X/1K1% R0402
0 - GRANTING CONSENT VIA PIN STRAP
1 - NO GRANTING (DEFAULT)
STRAP: NAC PRESENT
+V3P3A
ETH_MDIO4 R655 2.49K
R609 X/100 1% R0402
0 - NAC IS DISABLED
1 - NAC IS ENABLED (DEFAULT)
+V3P3A
NCSI_TX_EN_R R9166 X/4.75K R0402 1%
R9167 4.75K R0402 1%
+V3P3A
NCSI_TXD0_R R9168 X/4.75K R0402 1%
R9169 100K R0201 5%
+V3P3A
NCSI_TXD1_R R9171 X/4.75K R0402 1%
R9170 100K R0201 5%
NCSI_RXD0_R R10847 100K R0201
NCSI_RXD1_R R10848 100K R0201
NCSI_CRS_DV_R R10849 100K R0201

Intel Corporation Confidential
Approved for Customer Distribution


NAC_TIME_REF_P R10850 10K R0201
NAC_TIME_REF_N R10851 10K R0201
NAC_TIME_SYNC_P R10852 10K R0201
NAC_TIME_SYNC_N R10853 10K R0201
NAC_NET_CLKIN_REF0_P R10854 10K R0201
NAC_NET_CLKIN_REF0_N R10855 10K R0201
ETH_GPIO6 R10856 10K R0201
A0.2 modify
+V3P3A
ETH_MDC4 R551 2.49K
STRAP: ADR DEBUG
+V3P3A
FM_GBE_SDP_TIMESYNC0 R699 10K 1% R0402
R693 X/1K1% R0402
0 - NAC IS DISABLED
1 - NAC IS ENABLED (DEFAULT)
STRAP: BOOT HALT
+V3P3A
FM_GBE_SDP_TIMESYNC2 R179 10K 1% R0402
R174 X/1K1% R0402
0 - HALT
1 - NOT HALTED (XDP SUPPORT) (DEFAULT)
ESPI OR LPC
+V3P3A
FM_GBE_SDP_TIMESYNC1 R9134 X/10K% R0402
R9135 1K 1% R0402
0 - LPC(Default)
1 - eSPI

CFG2.1 CPVL (X557-AT4) (Quad0)


SoC
Coppervale PHY
CPVL flash
RJ-45 (4x)
10GBASE-T
10GBASE-T
10GBASE-T
10GBASE-T
Base-T with External PHY
(Quad0)
Base-T LEDs

AAEON Technology INC.

Title: SoC 10G/NCSI

Size	Document Number	Rev
Custom	COM-ICDB7	A0.3_0_0

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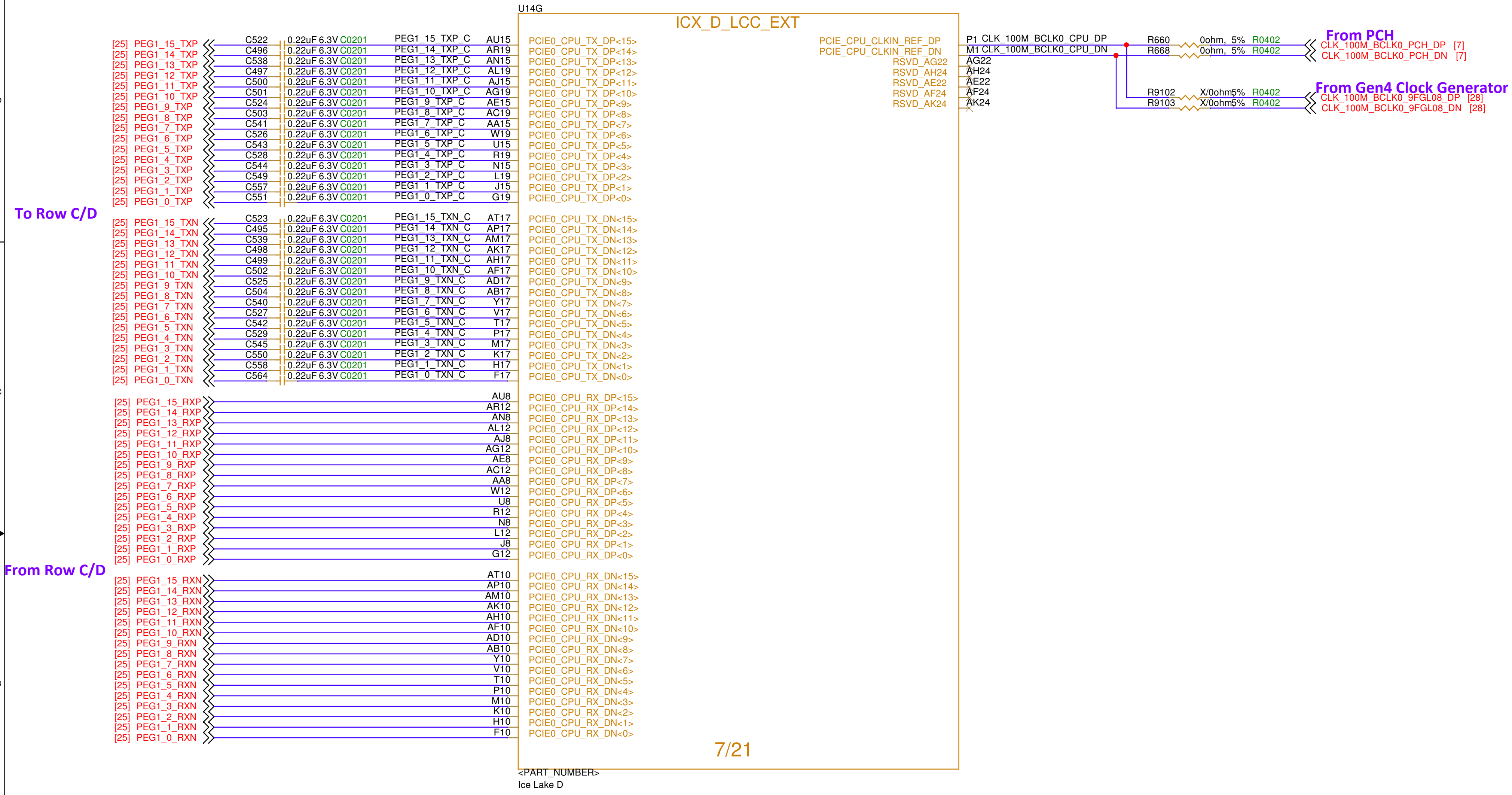
SoC PCIe CPU GEN4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PCIE_CPU_CLKIN_REF_DN M1 CLK_100M_BCLK0_CPU_DN
RSVD_AG22 AG22
RSVD_AH24 AH24
RSVD_AE22 AE22
RSVD_AF24 AF24
RSVD_AK24 AK24
R660 0ohm, 5% R0402
R668 0ohm, 5% R0402
From PCH
CLK_100M_BCLK0_PCH_DP [7]
CLK_100M_BCLK0_PCH_DN [7]
R9102 X/0ohm5% R0402
R9103 X/0ohm5% R0402
From Gen4 Clock Generator
CLK_100M_BCLK0_9FGL08_DP [28]
CLK_100M_BCLK0_9FGL08_DN [28]
7/21
<PART_NUMBER>
Ice Lake D

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AAEON Technology INC.

Title
SoC PCIe CPU GEN4

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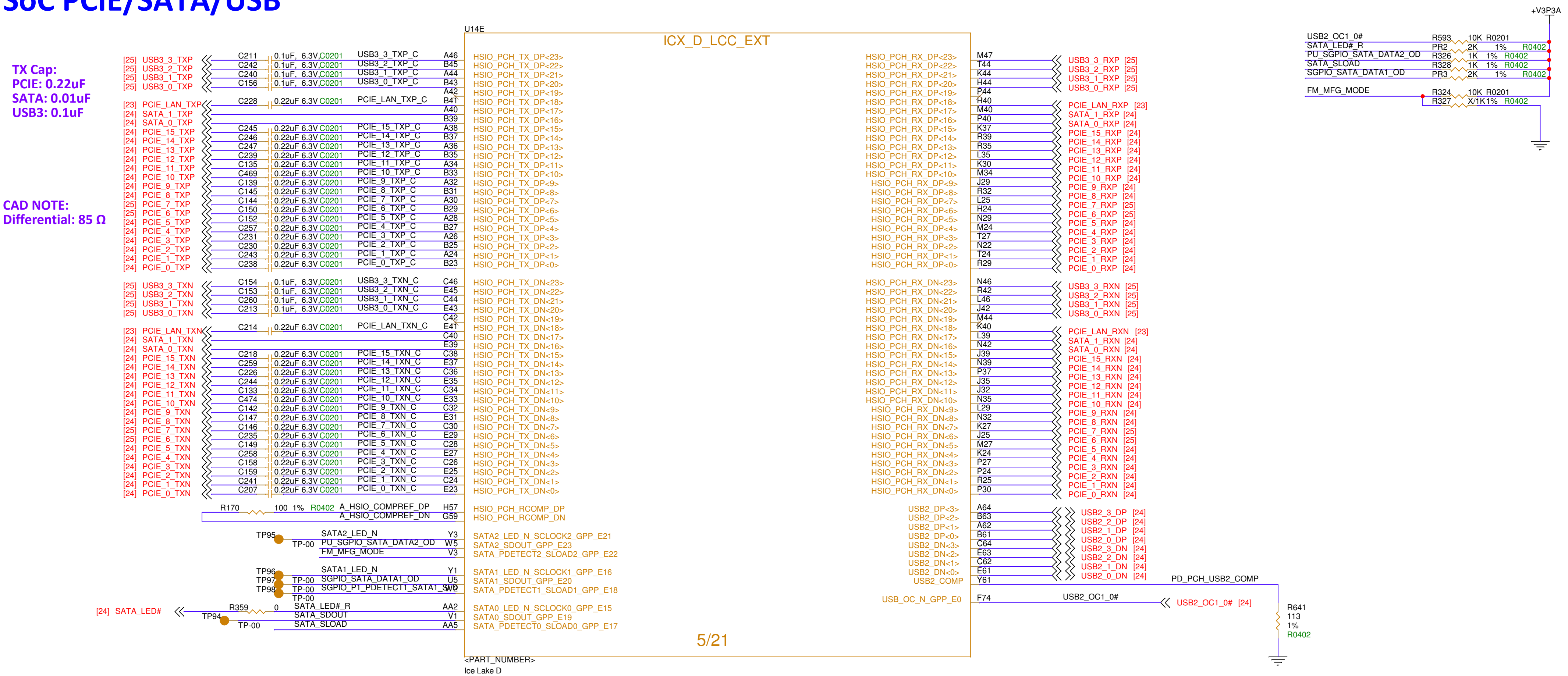
SoC PCIE/SATA/USB



TX Cap:
PCIE: 0.22uF
SATA: 0.01uF
USB3: 0.1uF

CAD NOTE:
Differential: 85 Ω

U14E
ICX_D_LCC_EXT
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PU_SGPIO_SATA_DATA2_OD W5 SATA2_SDOUT_GPP_E23
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5/21
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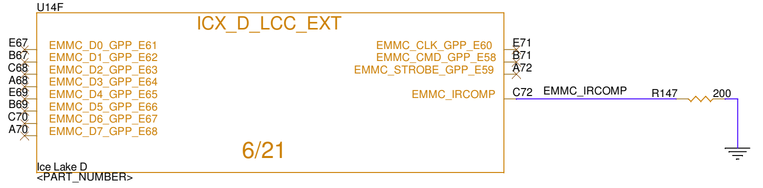
Ice Lake D
+V3P3A
USB2_OC1_0# R593 10K R0201
SATA_LED#_R PR2 2K 1% R0402
PU_SGPIO_SATA_DATA2_OD R326 1K 1% R0402
SATA_SLOAD R328 1K 1% R0402
SGPIO_SATA_DATA1_OD PR3 2K 1% R0402
FM_MFG_MODE R324 10K R0201
R327 X/1K 1% R0402



U14F
ICX_D_LCC_EXT
E67 EMMC_D0_GPP_E61
B67 EMMC_D1_GPP_E62
C68 EMMC_D2_GPP_E63
A68 EMMC_D3_GPP_E64
E69 EMMC_D4_GPP_E65
B69 EMMC_D5_GPP_E66
C70 EMMC_D6_GPP_E67
A70 EMMC_D7_GPP_E68
EMMC_CLK_GPP_E60 E71
EMMC_CMD_GPP_E58 B71
EMMC_STROBE_GPP_E59 A72
EMMC_IRCOMP C72 EMMC_IRCOMP R147 200
6/21
Ice Lake D
<PART_NUMBER>

HSIO lanes 0-7							
Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
SATA Controller 0							
SATA 0	SATA 1	SATA 2	SATA 3	SATA 4	SATA 5	SATA 6	SATA 7
PCIE Cluster 0 PCIe x8							
PCIe x4				PCIe x4			
PCIe x2		PCIe x2		PCIe x2		PCIe x2	
PCIe x1		PCIe x1		PCIe x1		PCIe x1	

HSIO lanes 8-15							
Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
SATA Controller 1							
SATA 8	SATA 9	SATA 10	SATA 11	SATA 12	SATA 13	SATA 14	SATA 15
PCIe Cluster 1 PCIe x8							
PCIe x4				PCIe x4			
PCIe x2		PCIe x2		PCIe x2		PCIe x2	
PCIe x1		PCIe x1		PCIe x1		PCIe x1	

HSIO lanes 16-24							
Lane 16	Lane 17	Lane 18	Lane 19	Lane 20	Lane 21	Lane 22	Lane 23
SATA Controller 2							
SATA 16	SATA 17	SATA 18	SATA 19	SATA 20	SATA 21	SATA 22	SATA 23
PCIe Cluster 2 PCIe x8							
PCIe x4				PCIe x4			
PCIe x2		PCIe x2		PCIe x2		PCIe x2	
PCIe x1		PCIe x1		PCIe x1		PCIe x1	
				USB3.0 Port 0	USB3.0 Port 1	USB3.0 Port 2	USB3.0 Port 3

Ice Lake-D LCC SoC				COM-ICDB7
LANE0		SATA #0	PCIe #0	PCIe #0(ROW A/B)
LANE1		SATA #1	PCIe #1	PCIe #1(ROW A/B)
LANE2		SATA #2	PCIe #2	PCIe #2(ROW A/B)
LANE3		SATA #3	PCIe #3	PCIe #3(ROW A/B)
LANE4		SATA #4	PCIe #4	PCIe #4(ROW A/B)
LANE5		SATA #5	PCIe #5	PCIe #5(ROW A/B)
LANE6		SATA #6	PCIe #6	PCIe #6(ROW C/D)
LANE7		SATA #7	PCIe #7	PCIe #7(ROW C/D)
LANE8		SATA #8	PCIe #8	PCIe #8(ROW A/B)
LANE9		SATA #9	PCIe #9	PCIe #9(ROW A/B)
LANE10		SATA #10	PCIe #10	PCIe #10(ROW A/B)
LANE11		SATA #11	PCIe #11	PCIe #11(ROW A/B)
LANE12		SATA #12	PCIe #12	PCIe #12(ROW A/B)
LANE13		SATA #13	PCIe #13	PCIe #13(ROW A/B)
LANE14		SATA #14	PCIe #14	PCIe #14(ROW A/B)
LANE15		SATA #15	PCIe #15	PCIe #15(ROW A/B)
LANE16		SATA #16	PCIe #16	SATA #0(ROW A/B)
LANE17		SATA #17	PCIe #17	SATA #1(ROW A/B)
LANE18		SATA #18	PCIe #18	PCIe for LAN (ROW A/B)
LANE19		SATA #19	PCIe #19	
LANE20	USB3 #0	SATA #20	PCIe #20	USB 3.0 #0(ROW C/D)
LANE21	USB3 #1	SATA #21	PCIe #21	USB 3.0 #1(ROW C/D)
LANE22	USB3 #2	SATA #22	PCIe #22	USB 3.0 #2(ROW C/D)
LANE23	USB3 #3	SATA #23	PCIe #23	USB 3.0 #3(ROW C/D)

Ice Lake-D LCC SoC	COM-ICDB7
USB2 #0	USB 2.0 #0(ROW A/B)
USB2 #1	USB 2.0 #1(ROW A/B)
USB2 #2	USB 2.0 #2(ROW A/B)
USB2 #3	USB 2.0 #3(ROW A/B)

AAEON Technology INC.
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SoC PCIE/SATA/USB
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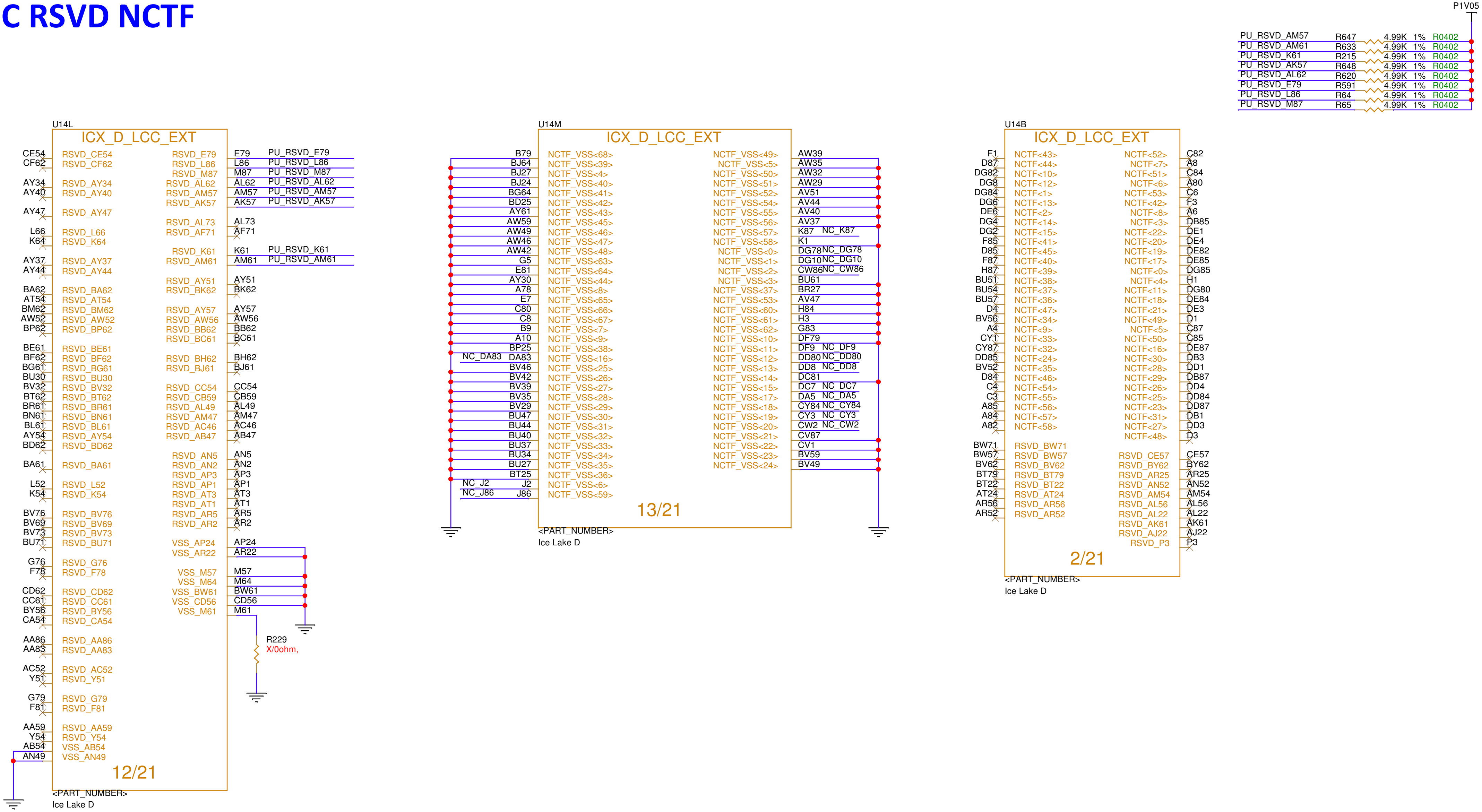
SoC RSVD NCTF



P1V05
PU_RSVD_AM57 R647 4.99K 1% R0402
PU_RSVD_AM61 R633 4.99K 1% R0402
PU_RSVD_K61 R215 4.99K 1% R0402
PU_RSVD_AK57 R648 4.99K 1% R0402
PU_RSVD_AL62 R620 4.99K 1% R0402
PU_RSVD_E79 R591 4.99K 1% R0402
PU_RSVD_L86 R64 4.99K 1% R0402
PU_RSVD_M87 R65 4.99K 1% R0402
U14L
ICX_D_LCC_EXT
CE54 RSVD_CE54
CF62 RSVD_CF62
AY34 RSVD_AY34
AY40 RSVD_AY40
AY47 RSVD_AY47
L66 RSVD_L66
K64 RSVD_K64
AY37 RSVD_AY37
AY44 RSVD_AY44
BA62 RSVD_BA62
AT54 RSVD_AT54
BM62 RSVD_BM62
AW52 RSVD_AW52
BP62 RSVD_BP62
BE61 RSVD_BE61
BF62 RSVD_BF62
BG61 RSVD_BG61
BU30 RSVD_BU30
BV32 RSVD_BV32
BT62 RSVD_BT62
BR61 RSVD_BR61
BN61 RSVD_BN61
BL61 RSVD_BL61
AY54 RSVD_AY54
BD62 RSVD_BD62
BA61 RSVD_BA61
L52 RSVD_L52
K54 RSVD_K54
BV76 RSVD_BV76
BV69 RSVD_BV69
BV73 RSVD_BV73
BU71 RSVD_BU71
G76 RSVD_G76
F78 RSVD_F78
CD62 RSVD_CD62
CC61 RSVD_CC61
BY56 RSVD_BY56
CA54 RSVD_CA54
AA86 RSVD_AA86
AA83 RSVD_AA83
AC52 RSVD_AC52
Y51 RSVD_Y51
G79 RSVD_G79
F81 RSVD_F81
AA59 RSVD_AA59
Y54 RSVD_Y54
AB54 VSS_AB54
AN49 VSS_AN49
RSVD_E79 E79 PU_RSVD_E79
RSVD_L86 L86 PU_RSVD_L86
RSVD_M87 M87 PU_RSVD_M87
RSVD_AL62 AL62 PU_RSVD_AL62
RSVD_AM57 AM57 PU_RSVD_AM57
RSVD_AK57 AK57 PU_RSVD_AK57
RSVD_AL73 AL73
RSVD_AF71 AF71
RSVD_K61 K61 PU_RSVD_K61
RSVD_AM61 AM61 PU_RSVD_AM61
RSVD_AY51 AY51
RSVD_BK62 BK62
RSVD_AY57 AY57
RSVD_AW56 AW56
RSVD_BB62 BB62
RSVD_BC61 BC61
RSVD_BH62 BH62
RSVD_BJ61 BJ61
RSVD_CC54 CC54
RSVD_CB59 CB59
RSVD_AL49 AL49
RSVD_AM47 AM47
RSVD_AC46 AC46
RSVD_AB47 AB47
RSVD_AN5 AN5
RSVD_AN2 AN2
RSVD_AP3 AP3
RSVD_AP1 AP1
RSVD_AT3 AT3
RSVD_AT1 AT1
RSVD_AR5 AR5
RSVD_AR2 AR2
VSS_AP24 AP24
VSS_AR22 AR22
VSS_M57 M57
VSS_M64 M64
VSS_BW61 BW61
VSS_CD56 CD56
VSS_M61 M61
R229
X/0ohm,
12/21
<PART_NUMBER>
Ice Lake D
U14M
ICX_D_LCC_EXT
B79 NCTF_VSS<68>
BJ64 NCTF_VSS<39>
BJ27 NCTF_VSS<4>
BJ24 NCTF_VSS<40>
BG64 NCTF_VSS<41>
BD25 NCTF_VSS<42>
AY61 NCTF_VSS<43>
AW59 NCTF_VSS<45>
AW49 NCTF_VSS<46>
AW46 NCTF_VSS<47>
AW42 NCTF_VSS<48>
G5 NCTF_VSS<63>
E81 NCTF_VSS<64>
AY30 NCTF_VSS<44>
A78 NCTF_VSS<8>
E7 NCTF_VSS<65>
C80 NCTF_VSS<66>
C8 NCTF_VSS<67>
B9 NCTF_VSS<7>
A10 NCTF_VSS<9>
BP25 NCTF_VSS<38>
NC_DA83 DA83 NCTF_VSS<16>
BV46 NCTF_VSS<25>
BV42 NCTF_VSS<26>
BV39 NCTF_VSS<27>
BV35 NCTF_VSS<28>
BV29 NCTF_VSS<29>
BU47 NCTF_VSS<30>
BU44 NCTF_VSS<31>
BU40 NCTF_VSS<32>
BU37 NCTF_VSS<33>
BU34 NCTF_VSS<34>
BU27 NCTF_VSS<35>
BT25 NCTF_VSS<36>
NC_J2 J2 NCTF_VSS<6>
NC_J86 J86 NCTF_VSS<59>
NCTF_VSS<49> AW39
NCTF_VSS<5> AW35
NCTF_VSS<50> AW32
NCTF_VSS<51> AW29
NCTF_VSS<52> AV51
NCTF_VSS<54> AV44
NCTF_VSS<55> AV40
NCTF_VSS<56> AV37
NCTF_VSS<57> K87 NC_K87
NCTF_VSS<58> K1
NCTF_VSS<0> DG78 NC_DG78
NCTF_VSS<1> DG10 NC_DG10
NCTF_VSS<2> CW86 NC_CW86
NCTF_VSS<3> BU61
NCTF_VSS<37> BR27
NCTF_VSS<53> AV47
NCTF_VSS<60> H84
NCTF_VSS<61> H3
NCTF_VSS<62> G83
NCTF_VSS<10> DF79
NCTF_VSS<11> DF9 NC_DF9
NCTF_VSS<12> DD80 NC_DD80
NCTF_VSS<13> DD8 NC_DD8
NCTF_VSS<14> DC81
NCTF_VSS<15> DC7 NC_DC7
NCTF_VSS<17> DA5 NC_DA5
NCTF_VSS<18> CY84 NC_CY84
NCTF_VSS<19> CY3 NC_CY3
NCTF_VSS<20> CW2 NC_CW2
NCTF_VSS<21> CV87
NCTF_VSS<22> CV1
NCTF_VSS<23> BV59
NCTF_VSS<24> BV49
13/21
<PART_NUMBER>
Ice Lake D
U14B
ICX_D_LCC_EXT
F1 NCTF<43>
D87 NCTF<44>
DG82 NCTF<10>
DG8 NCTF<12>
DG84 NCTF<1>
DG6 NCTF<13>
DE6 NCTF<2>
DG4 NCTF<14>
DG2 NCTF<15>
F85 NCTF<41>
D85 NCTF<45>
F87 NCTF<40>
H87 NCTF<39>
BU51 NCTF<38>
BU54 NCTF<37>
BU57 NCTF<36>
D4 NCTF<47>
BV56 NCTF<34>
A4 NCTF<9>
CY1 NCTF<33>
CY87 NCTF<32>
DD85 NCTF<24>
BV52 NCTF<35>
D84 NCTF<46>
C4 NCTF<54>
C3 NCTF<55>
A85 NCTF<56>
A84 NCTF<57>
A82 NCTF<58>
BW71 RSVD_BW71
BW57 RSVD_BW57
BV62 RSVD_BV62
BT79 RSVD_BT79
BT22 RSVD_BT22
AT24 RSVD_AT24
AR56 RSVD_AR56
AR52 RSVD_AR52
NCTF<52> C82
NCTF<7> A8
NCTF<51> C84
NCTF<6> A80
NCTF<53> C6
NCTF<42> F3
NCTF<8> A6
NCTF<3> DB85
NCTF<22> DE1
NCTF<20> DE4
NCTF<19> DE82
NCTF<17> DE85
NCTF<0> DG85
NCTF<4> H1
NCTF<11> DG80
NCTF<18> DE84
NCTF<21> DE3
NCTF<49> D1
NCTF<5> C87
NCTF<50> C85
NCTF<16> DE87
NCTF<30> DB3
NCTF<28> DD1
NCTF<29> DB87
NCTF<26> DD4
NCTF<25> DD84
NCTF<23> DD87
NCTF<31> DB1
NCTF<27> DD3
NCTF<48> D3
RSVD_CE57 CE57
RSVD_BY62 BY62
RSVD_AR25 AR25
RSVD_AN52 AN52
RSVD_AM54 AM54
RSVD_AL56 AL56
RSVD_AL22 AL22
RSVD_AK61 AK61
RSVD_AJ22 AJ22
RSVD_P3 P3
2/21
<PART_NUMBER>
Ice Lake D

AAEON Technology INC.

An ASUS Company

Title	SoC SVID/RSVD/JTAG	
Size: Custom	Document Number: COM-ICDB7	Rev: A0.3_0_0
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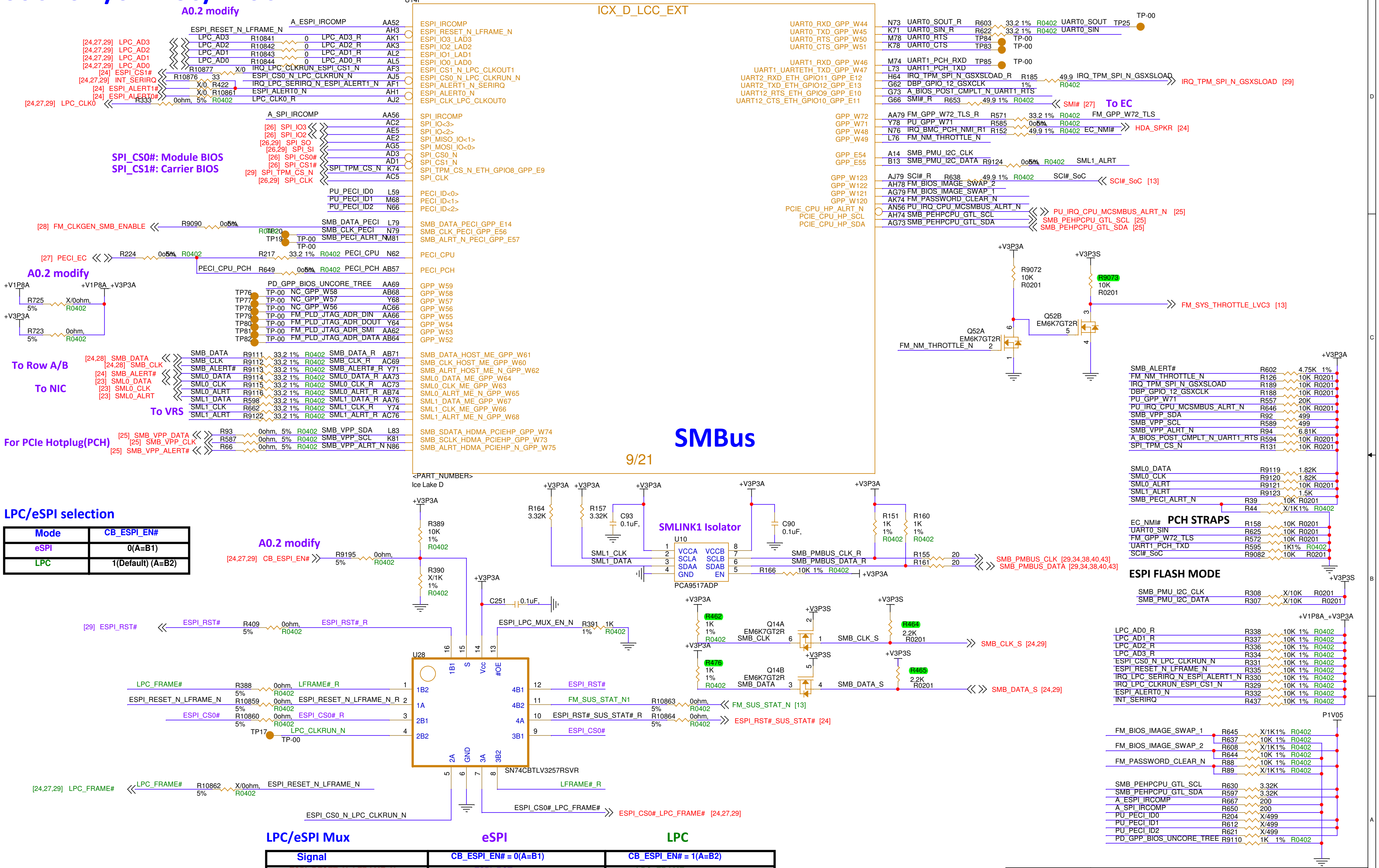
SoC ESPI/SMBUS/MISC


A0.2 modify
U14I
ICX_D_LCC_EXT
SPI_CS0#: Module BIOS
SPI_CS1#: Carrier BIOS
A0.2 modify
To Row A/B
To NIC
To VRS
For PCIe Hotplug(PCH)
To EC
SMBus
9/21
<PART_NUMBER>
Ice Lake D
SMLINK1 Isolator
U10
PCA9517ADP
PCH STRAPS
ESPI FLASH MODE
A0.2 modify
U28
SN74CBTLV3257RSVR
ESPI_IRCOMP
ESPI_RESET_N_LFRAME_N
ESPI_CS0_N_LPC_CLKRUN_N
SMB_PMBUS_CLK [29,34,38,40,43]
SMB_PMBUS_DATA [29,34,38,40,43]
SMB_CLK_S [24,29]
SMB_DATA_S [24,29]
FM_SYS_THROTTLE_LVC3 [13]
IRQ_TPM_SPI_N_GSXSLOAD [29]
HDA_SPKR [24]
SCI#_SoC [13]
ESPI_CS0#_LPC_FRAME# [24,27,29]
ESPI_RST#_SUS_STAT# [24]
FM_SUS_STAT_N [13]
[24,27,29] CB_ESPI_EN#
[29] ESPI_RST#
[24,27,29] LPC_FRAME#

LPC/eSPI selection

Mode	CB_ESPI_EN#
eSPI	0(A=B1)
LPC	1(Default) (A=B2)

LPC/eSPI Mux

Signal	eSPI CB_ESPI_EN# = 0(A=B1)	LPC CB_ESPI_EN# = 1(A=B2)
ESPI_RESET_N_LFRAME_N	ESPI_RST#	LPC_FRAME#
ESPI_CS0_N_LPC_CLKRUN_N	ESPI_CS0#	LPC_CLKRUN_N
ESPI_CS0#_LPC_FRAME#	ESPI_CS0#	LPC_FRAME#
ESPI_RST#_SUS_STAT#	ESPI_RST#	FM_SUS_STAT_N

INPUTS		FUNCTION
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

AAEON Technology INC.
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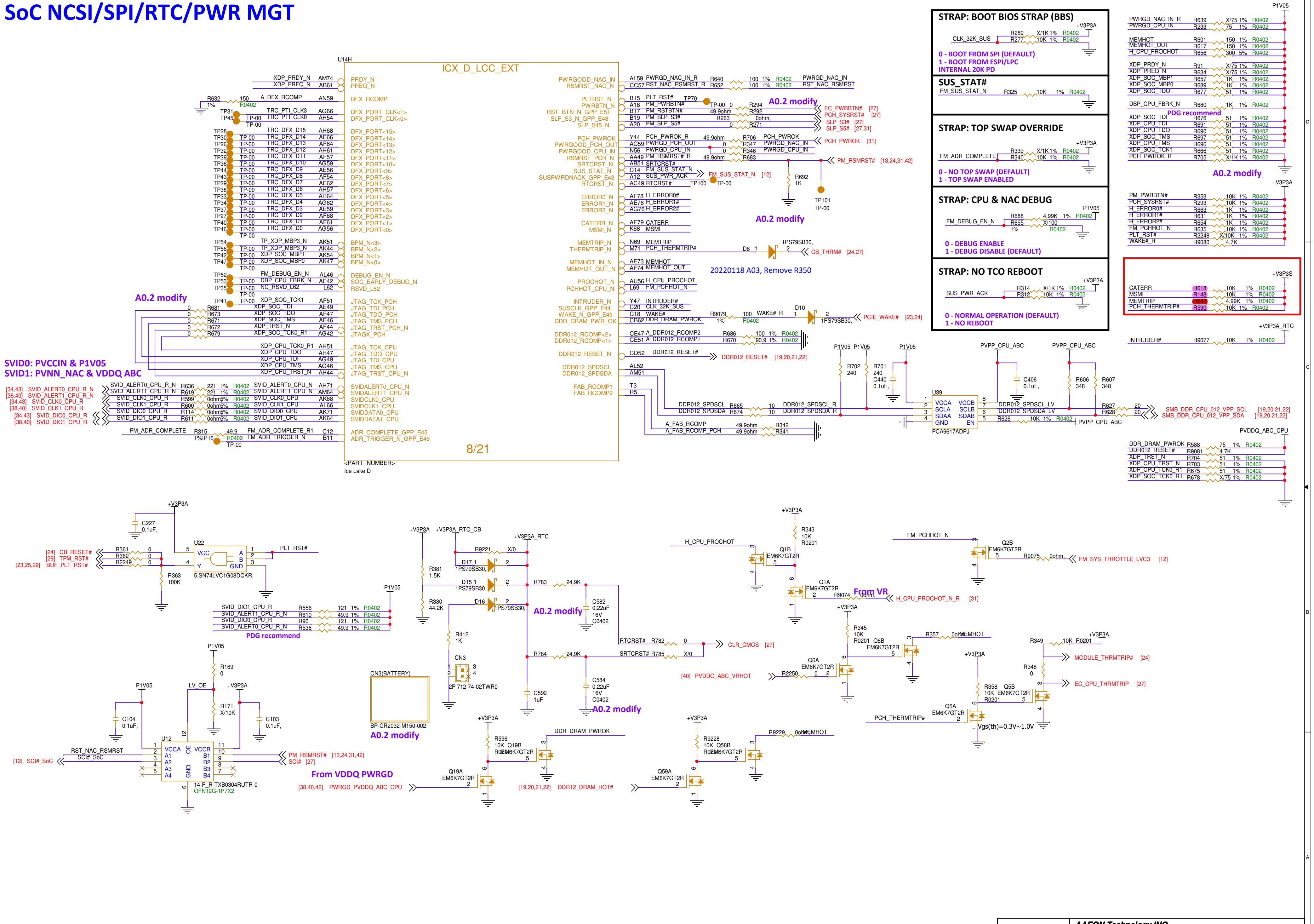
SoC NCSI/SPI/RTC/PWR MGT



U14H
ICX_D_LCC_EXT
8/21
<PART_NUMBER>
Ice Lake D
XDP_PRDY_N
XDP_PREQ_N
PRDY_N
PREQ_N
DFX_RCOMP
DFX_PORT_CLK<1>
DFX_PORT_CLK<0>
PWRGOOD_NAC_IN
RSMRST_NAC_N
PLTRST_N
PWRBTN_N
RST_BTN_N_GPP_E51
SLP_S3_N_GPP_E48
SLP_S45_N
PCH_PWROK
PWRGOOD_PCH_OUT
PWRGOOD_CPU_IN
RSMRST_PCH_N
SRTCRST_N
SUS_STAT_N
SUSPWRDNACK_GPP_E43
RTCRST_N
ERROR0_N
ERROR1_N
ERROR2_N
CATERR_N
MSMI_N
MEMTRIP_N
THERMTRIP_N
MEMHOT_IN_N
MEMHOT_OUT_N
PROCHOT_N
PCHHOT_CPU_N
INTRUDER_N
SUSCLK_GPP_E44
WAKE_N_GPP_E49
DDR_DRAM_PWR_OK
DDR012_RCOMP<2>
DDR012_RCOMP<1>
DDR012_RESET_N
DDR012_SPDSCL
DDR012_SPDSDA
FAB_RCOMP1
FAB_RCOMP2
BPM_N<3>
BPM_N<2>
BPM_N<1>
BPM_N<0>
DEBUG_EN_N
SOC_EARLY_DEBUG_N
RSVD_L62
JTAG_TCK_PCH
JTAG_TDI_PCH
JTAG_TDO_PCH
JTAG_TMS_PCH
JTAG_TRST_PCH_N
JTAGX_PCH
JTAG_TCK_CPU
JTAG_TDO_CPU
JTAG_TDI_CPU
JTAG_TMS_CPU
JTAG_TRST_CPU_N
SVIDALERT0_CPU_N
SVIDALERT1_CPU_N
SVIDCLK0_CPU
SVIDCLK1_CPU
SVIDDATA0_CPU
SVIDDATA1_CPU
ADR_COMPLETE_GPP_E45
ADR_TRIGGER_N_GPP_E46
A0.2 modify
SVID0: PVCCIN & P1V05
SVID1: PVNN_NAC & VDDQ ABC
20220118 A03, Remove R350
A0.2 modify
PM_RSMRST# [13,24,31,42]
EC_PWRBTN# [27]
PCH_SYSRST# [27]
SLP_S3# [27]
SLP_S5# [27,31]
PCH_PWROK [31]
FM_SUS_STAT_N [12]
CB_THRM# [24,27]
PCIE_WAKE# [23,24]
DDR012_RESET# [19,20,21,22]
SMB_DDR_CPU_012_VPP_SCL [19,20,21,22]
SMB_DDR_CPU_012_VPP_SDA [19,20,21,22]
U39
PCA9617ADPJ
STRAP: BOOT BIOS STRAP (BBS)
0 - BOOT FROM SPI (DEFAULT)
1 - BOOT FROM ESPI/LPC
INTERNAL 20K PD
SUS_STAT#
STRAP: TOP SWAP OVERRIDE
0 - NO TOP SWAP (DEFAULT)
1 - TOP SWAP ENABLED
STRAP: CPU & NAC DEBUG
0 - DEBUG ENABLE
1 - DEBUG DISABLE (DEFAULT)
STRAP: NO TCO REBOOT
0 - NORMAL OPERATION (DEFAULT)
1 - NO REBOOT
PDG recommend
A0.2 modify
U22
5,SN74LVC1G08DCK,
[24] CB_RESET#
[29] TPM_RST#
[23,25,29] BUF_PLT_RST#
PLT_RST#
PDG recommend
U12
14-P_R-TXB0304RUTR-0
QFN12G-1P7X2
[12] SCI#_SoC
PM_RSMRST# [13,24,31,42]
SCI# [27]
From VDDQ PWRGD
[38,40,42] PWRGD_PVDDQ_ABC_CPU
CN3(BATTERY)
BP-CR2032-M150-002
A0.2 modify
CN9
2P 712-74-02TWR0
A0.2 modify
A0.2 modify
CLR_CMOS [27]
[19,20,21,22] DDR012_DRAM_HOT#
From VR
H_CPU_PROCHOT_N_R [31]
FM_SYS_THROTTLE_LVC3 [12]
[40] PVDDQ_ABC_VRHOT
MODULE_THRMTRIP# [24]
EC_CPU_THRMTRIP [27]
Vgs(th)=0.3V~1.0V

AAEON Technology INC.

Title: SoC NCSI/SPI/RTC

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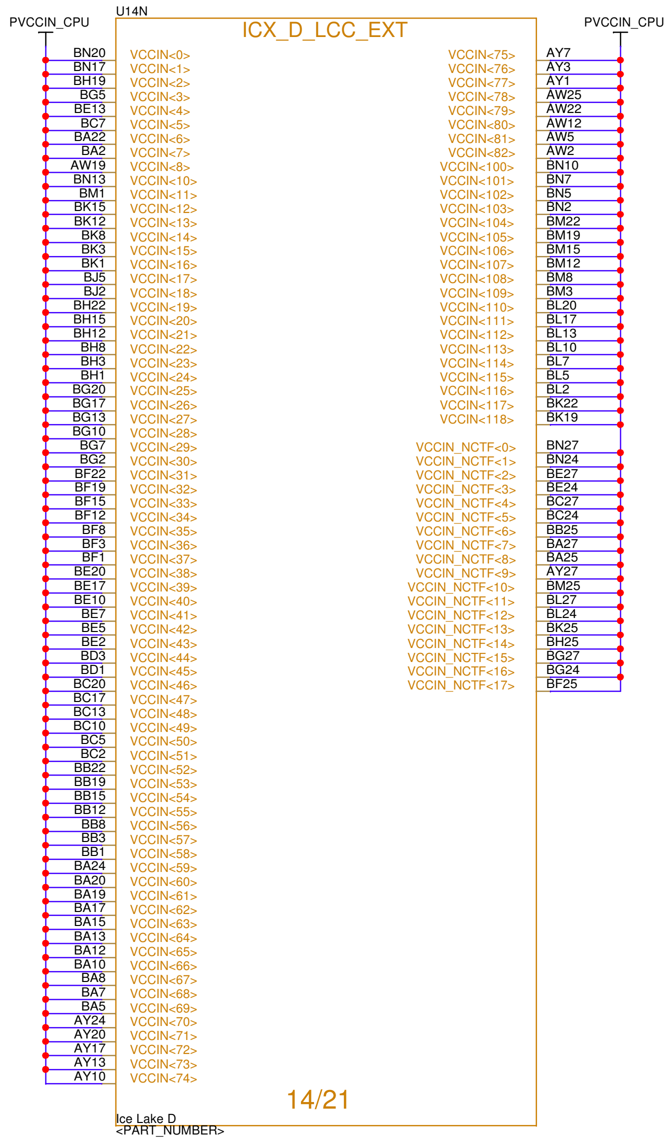
SoC PWR1


U14N
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PVCCIN_CPU
BN20 VCCIN<0>
BN17 VCCIN<1>
BH19 VCCIN<2>
BG5 VCCIN<3>
BE13 VCCIN<4>
BC7 VCCIN<5>
BA22 VCCIN<6>
BA2 VCCIN<7>
AW19 VCCIN<8>
BN13 VCCIN<10>
BM1 VCCIN<11>
BK15 VCCIN<12>
BK12 VCCIN<13>
BK8 VCCIN<14>
BK3 VCCIN<15>
BK1 VCCIN<16>
BJ5 VCCIN<17>
BJ2 VCCIN<18>
BH22 VCCIN<19>
BH15 VCCIN<20>
BH12 VCCIN<21>
BH8 VCCIN<22>
BH3 VCCIN<23>
BH1 VCCIN<24>
BG20 VCCIN<25>
BG17 VCCIN<26>
BG13 VCCIN<27>
BG10 VCCIN<28>
BG7 VCCIN<29>
BG2 VCCIN<30>
BF22 VCCIN<31>
BF19 VCCIN<32>
BF15 VCCIN<33>
BF12 VCCIN<34>
BF8 VCCIN<35>
BF3 VCCIN<36>
BF1 VCCIN<37>
BE20 VCCIN<38>
BE17 VCCIN<39>
BE10 VCCIN<40>
BE7 VCCIN<41>
BE5 VCCIN<42>
BE2 VCCIN<43>
BD3 VCCIN<44>
BD1 VCCIN<45>
BC20 VCCIN<46>
BC17 VCCIN<47>
BC13 VCCIN<48>
BC10 VCCIN<49>
BC5 VCCIN<50>
BC2 VCCIN<51>
BB22 VCCIN<52>
BB19 VCCIN<53>
BB15 VCCIN<54>
BB12 VCCIN<55>
BB8 VCCIN<56>
BB3 VCCIN<57>
BB1 VCCIN<58>
BA24 VCCIN<59>
BA20 VCCIN<60>
BA19 VCCIN<61>
BA17 VCCIN<62>
BA15 VCCIN<63>
BA13 VCCIN<64>
BA12 VCCIN<65>
BA10 VCCIN<66>
BA8 VCCIN<67>
BA7 VCCIN<68>
BA5 VCCIN<69>
AY24 VCCIN<70>
AY20 VCCIN<71>
AY17 VCCIN<72>
AY13 VCCIN<73>
AY10 VCCIN<74>
PVCCIN_CPU
VCCIN<75> AY7
VCCIN<76> AY3
VCCIN<77> AY1
VCCIN<78> AW25
VCCIN<79> AW22
VCCIN<80> AW12
VCCIN<81> AW5
VCCIN<82> AW2
VCCIN<100> BN10
VCCIN<101> BN7
VCCIN<102> BN5
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VCCIN<104> BM22
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VCCIN_NCTF<3> BE24
VCCIN_NCTF<4> BC27
VCCIN_NCTF<5> BC24
VCCIN_NCTF<6> BB25
VCCIN_NCTF<7> BA27
VCCIN_NCTF<8> BA25
VCCIN_NCTF<9> AY27
VCCIN_NCTF<10> BM25
VCCIN_NCTF<11> BL27
VCCIN_NCTF<12> BL24
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VCCIN_NCTF<14> BH25
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14/21
Ice Lake D
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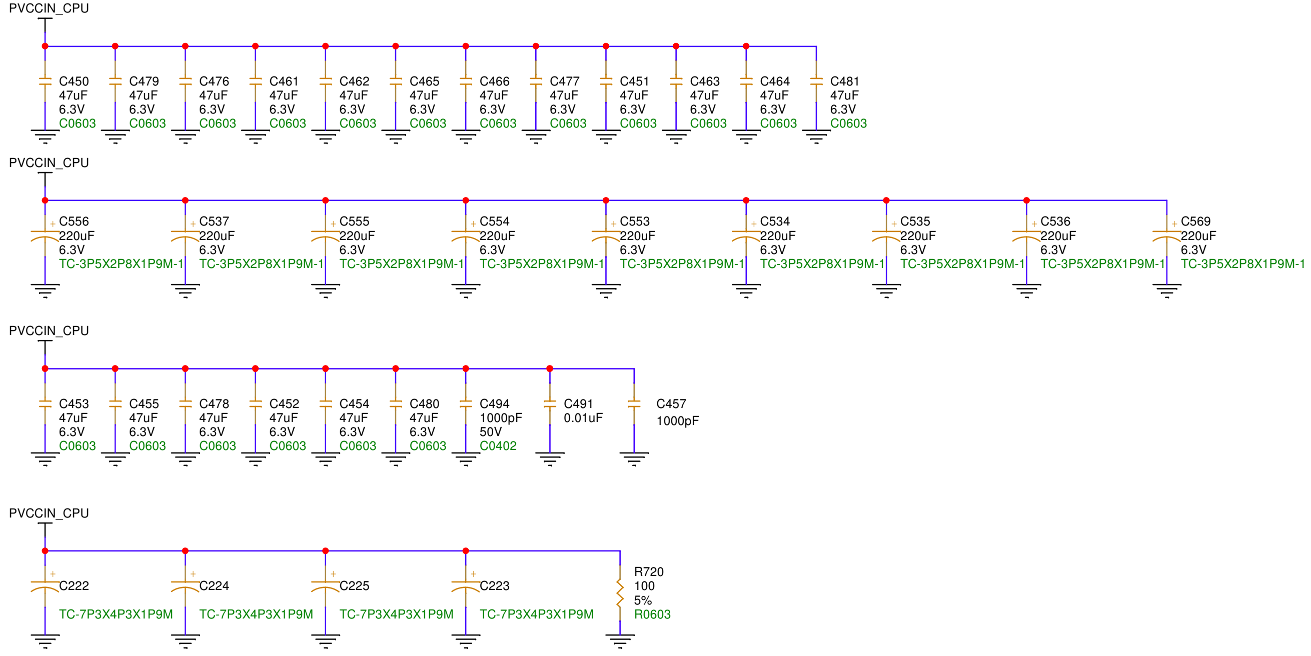
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C479 47uF 6.3V C0603
C476 47uF 6.3V C0603
C461 47uF 6.3V C0603
C462 47uF 6.3V C0603
C465 47uF 6.3V C0603
C466 47uF 6.3V C0603
C477 47uF 6.3V C0603
C451 47uF 6.3V C0603
C463 47uF 6.3V C0603
C464 47uF 6.3V C0603
C481 47uF 6.3V C0603
PVCCIN_CPU
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C537 220uF 6.3V TC-3P5X2P8X1P9M-1
C555 220uF 6.3V TC-3P5X2P8X1P9M-1
C554 220uF 6.3V TC-3P5X2P8X1P9M-1
C553 220uF 6.3V TC-3P5X2P8X1P9M-1
C534 220uF 6.3V TC-3P5X2P8X1P9M-1
C535 220uF 6.3V TC-3P5X2P8X1P9M-1
C536 220uF 6.3V TC-3P5X2P8X1P9M-1
C569 220uF 6.3V TC-3P5X2P8X1P9M-1
PVCCIN_CPU
C453 47uF 6.3V C0603
C455 47uF 6.3V C0603
C478 47uF 6.3V C0603
C452 47uF 6.3V C0603
C454 47uF 6.3V C0603
C480 47uF 6.3V C0603
C494 1000pF 50V C0402
C491 0.01uF
C457 1000pF
PVCCIN_CPU
C222 TC-7P3X4P3X1P9M
C224 TC-7P3X4P3X1P9M
C225 TC-7P3X4P3X1P9M
C223 TC-7P3X4P3X1P9M
R720 100 5% R0603

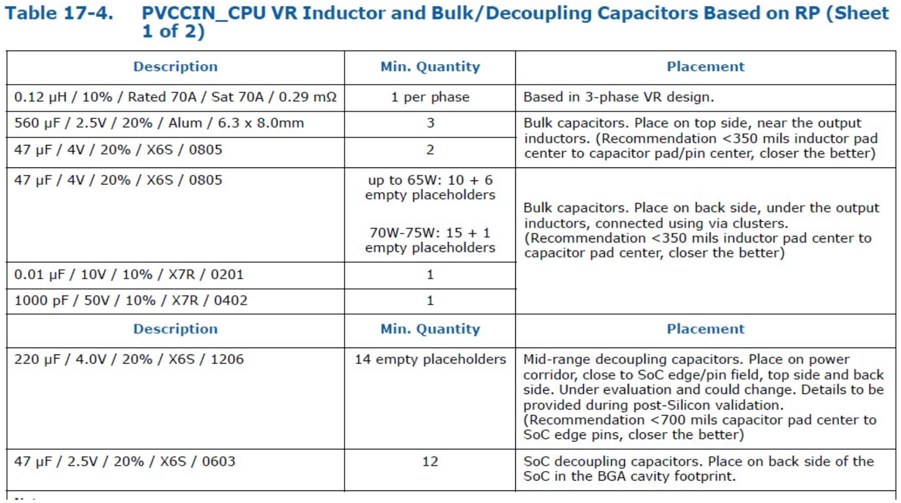

Table 17-4. PVCCIN_CPU VR Inductor and Bulk/Decoupling Capacitors Based on RP (Sheet 1 of 2)

Description	Min. Quantity	Placement
0.12 µH / 10% / Rated 70A / Sat 70A / 0.29 mΩ	1 per phase	Based in 3-phase VR design.
560 µF / 2.5V / 20% / Alum / 6.3 x 8.0mm	3	Bulk capacitors. Place on top side, near the output inductors. (Recommendation <350 mils inductor pad center to capacitor pad/pin center, closer the better)
47 µF / 4V / 20% / X6S / 0805	2	
47 µF / 4V / 20% / X6S / 0805	up to 65W: 10 + 6 empty placeholders 70W-75W: 15 + 1 empty placeholders	Bulk capacitors. Place on back side, under the output inductors, connected using via clusters. (Recommendation <350 mils inductor pad center to capacitor pad center, closer the better)
0.01 µF / 10V / 10% / X7R / 0201	1	
1000 pF / 50V / 10% / X7R / 0402	1	
Description	**Min. Quantity**	**Placement**
220 µF / 4.0V / 20% / X6S / 1206	14 empty placeholders	Mid-range decoupling capacitors. Place on power corridor, close to SoC edge/pin field, top side and back side. Under evaluation and could change. Details to be provided during post-Silicon validation. (Recommendation <700 mils capacitor pad center to SoC edge pins, closer the better)
47 µF / 2.5V / 20% / X6S / 0603	12	SoC decoupling capacitors. Place on back side of the SoC in the BGA cavity footprint.

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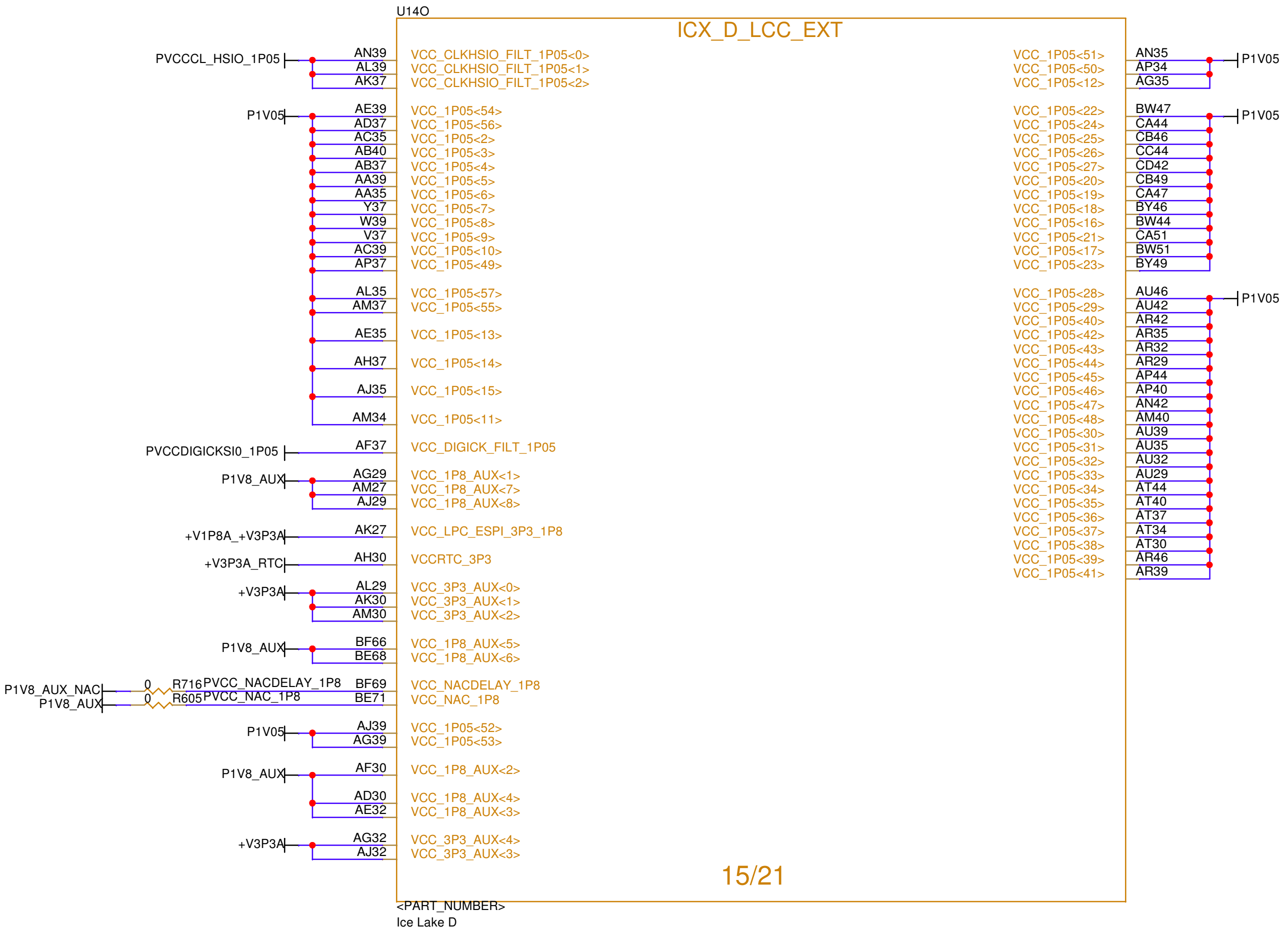
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PVCCCL_HSIO_1P05
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AL39 VCC_CLKHSIO_FILT_1P05<1>
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AE39 VCC_1P05<54>
AD37 VCC_1P05<56>
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V37 VCC_1P05<9>
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AM37 VCC_1P05<55>
AE35 VCC_1P05<13>
AH37 VCC_1P05<14>
AJ35 VCC_1P05<15>
AM34 VCC_1P05<11>
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AF37 VCC_DIGICK_FILT_1P05
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AG29 VCC_1P8_AUX<1>
AM27 VCC_1P8_AUX<7>
AJ29 VCC_1P8_AUX<8>
+V1P8A_+V3P3A
AK27 VCC_LPC_ESPI_3P3_1P8
+V3P3A_RTC
AH30 VCCRTC_3P3
+V3P3A
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AK30 VCC_3P3_AUX<1>
AM30 VCC_3P3_AUX<2>
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BF66 VCC_1P8_AUX<5>
BE68 VCC_1P8_AUX<6>
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P1V8_AUX
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BF69 VCC_NACDELAY_1P8
BE71 VCC_NAC_1P8
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AJ39 VCC_1P05<52>
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AD30 VCC_1P8_AUX<4>
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+V3P3A
AG32 VCC_3P3_AUX<4>
AJ32 VCC_3P3_AUX<3>
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VCC_1P05<22> BW47
VCC_1P05<24> CA44
VCC_1P05<25> CB46
VCC_1P05<26> CC44
VCC_1P05<27> CD42
VCC_1P05<20> CB49
VCC_1P05<19> CA47
VCC_1P05<18> BY46
VCC_1P05<16> BW44
VCC_1P05<21> CA51
VCC_1P05<17> BW51
VCC_1P05<23> BY49
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VCC_1P05<46> AP40
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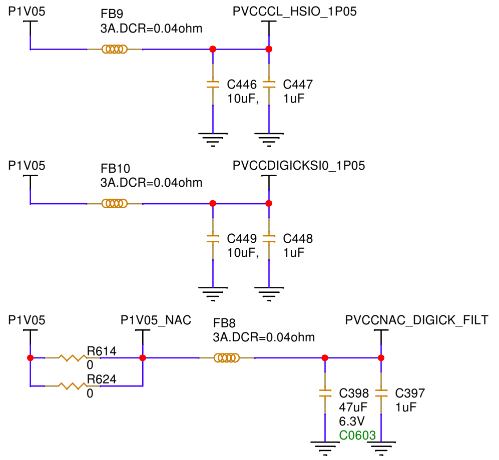
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C447
1uF
P1V05
FB10
3A.DCR=0.04ohm
PVCCDIGICKSI0_1P05
C449
10uF,
C448
1uF
P1V05
P1V05_NAC
R614
0
R624
0
FB8
3A.DCR=0.04ohm
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C398
47uF
6.3V
C0603
C397
1uF

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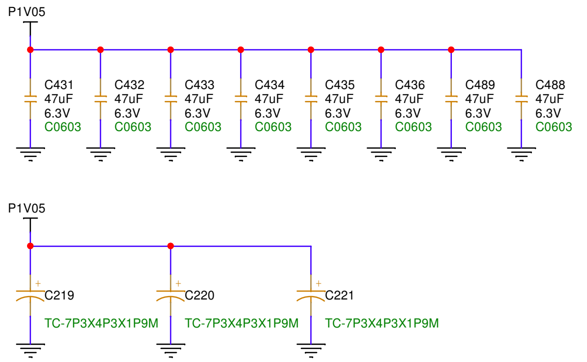
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C433 47uF 6.3V C0603
C434 47uF 6.3V C0603
C435 47uF 6.3V C0603
C436 47uF 6.3V C0603
C489 47uF 6.3V C0603
C488 47uF 6.3V C0603
P1V05
C219
TC-7P3X4P3X1P9M
C220
TC-7P3X4P3X1P9M
C221
TC-7P3X4P3X1P9M

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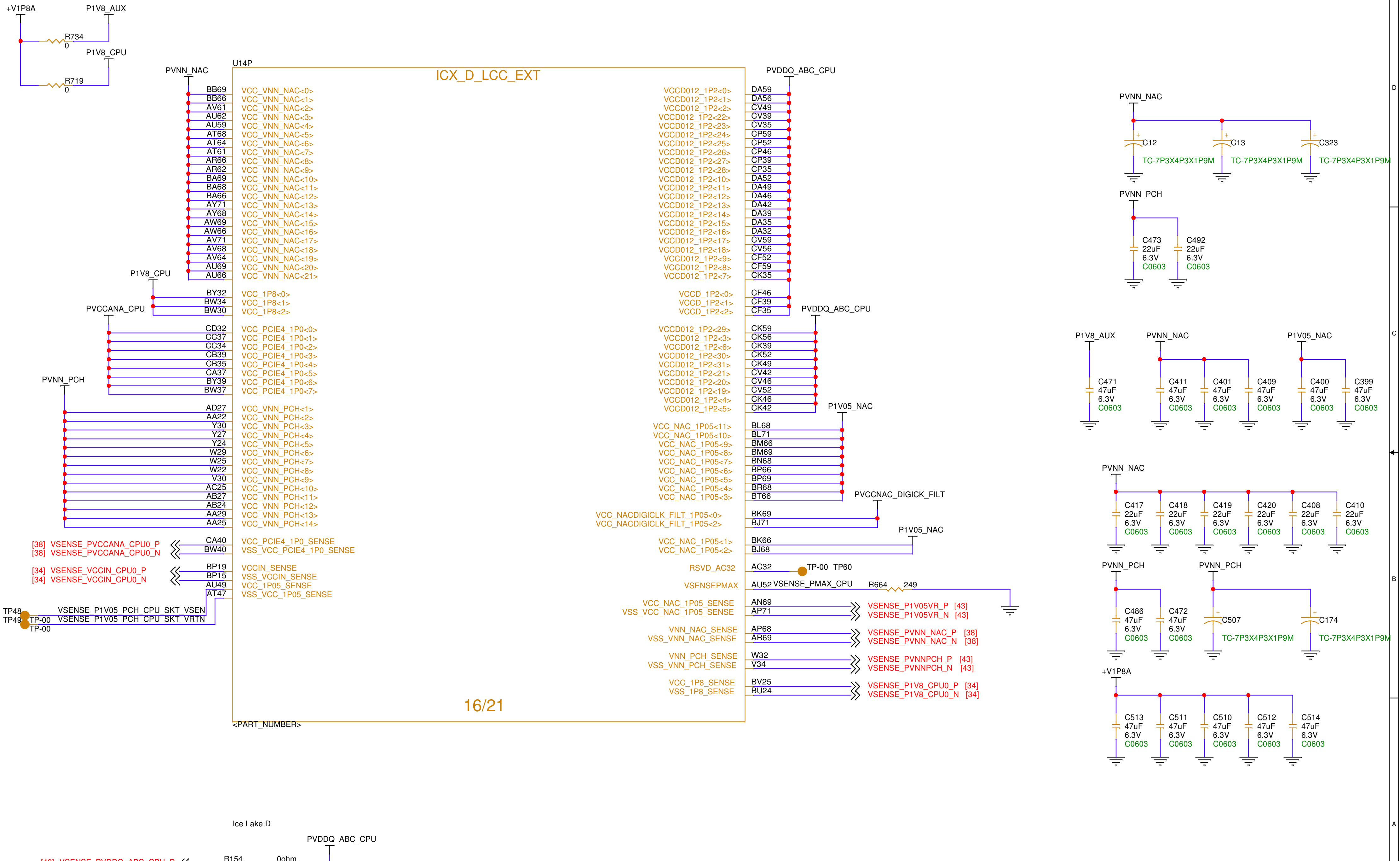
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0
P1V8_CPU
R719
0
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TP-00
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C492 22uF 6.3V C0603
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PVNN_NAC
P1V05_NAC
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C419 22uF 6.3V C0603
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C472 47uF 6.3V C0603
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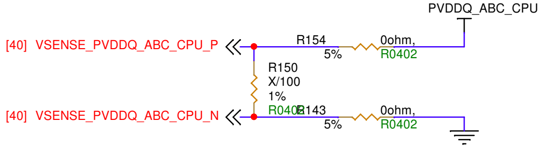
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R143
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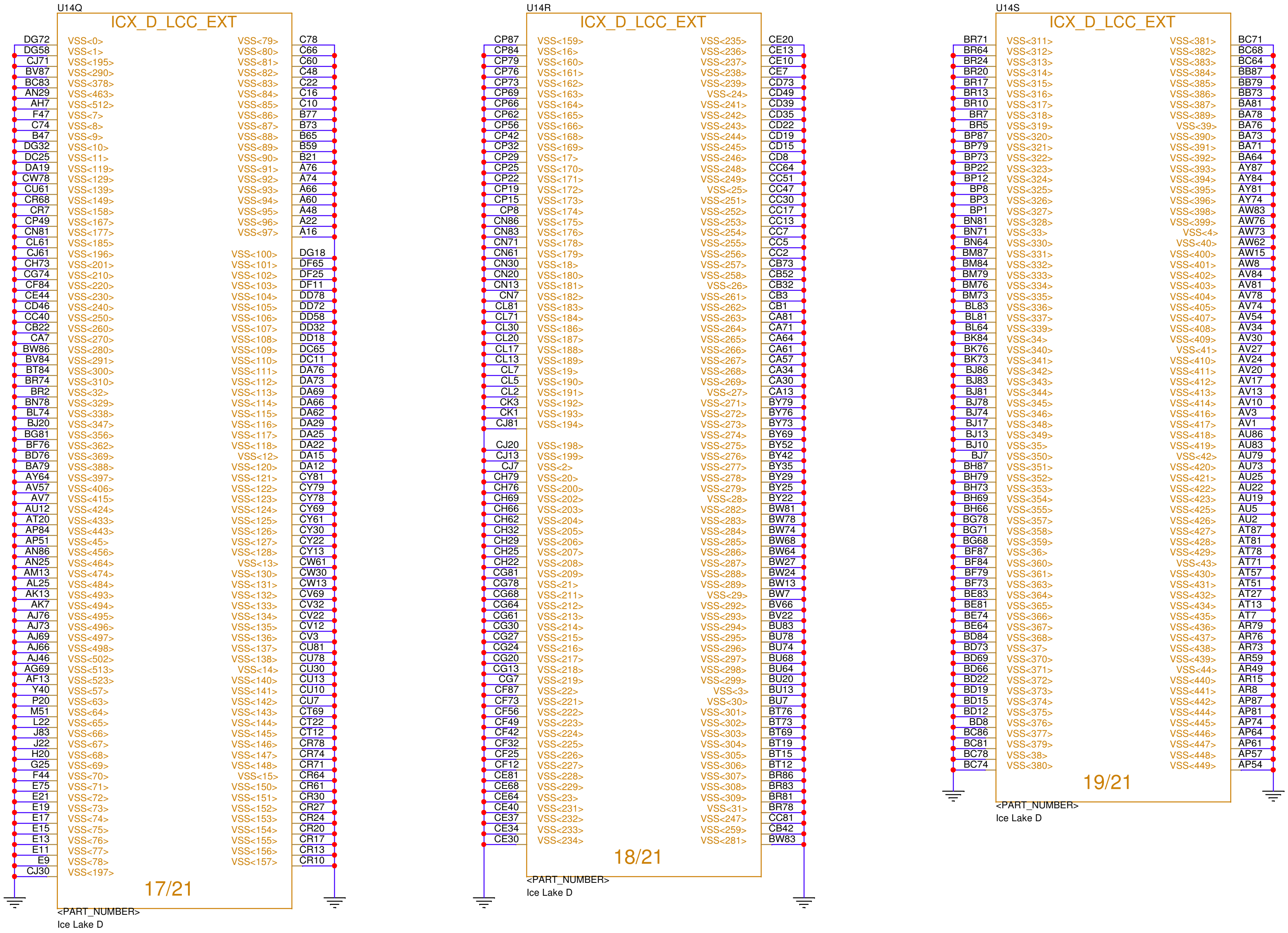
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AAEON Technology INC.

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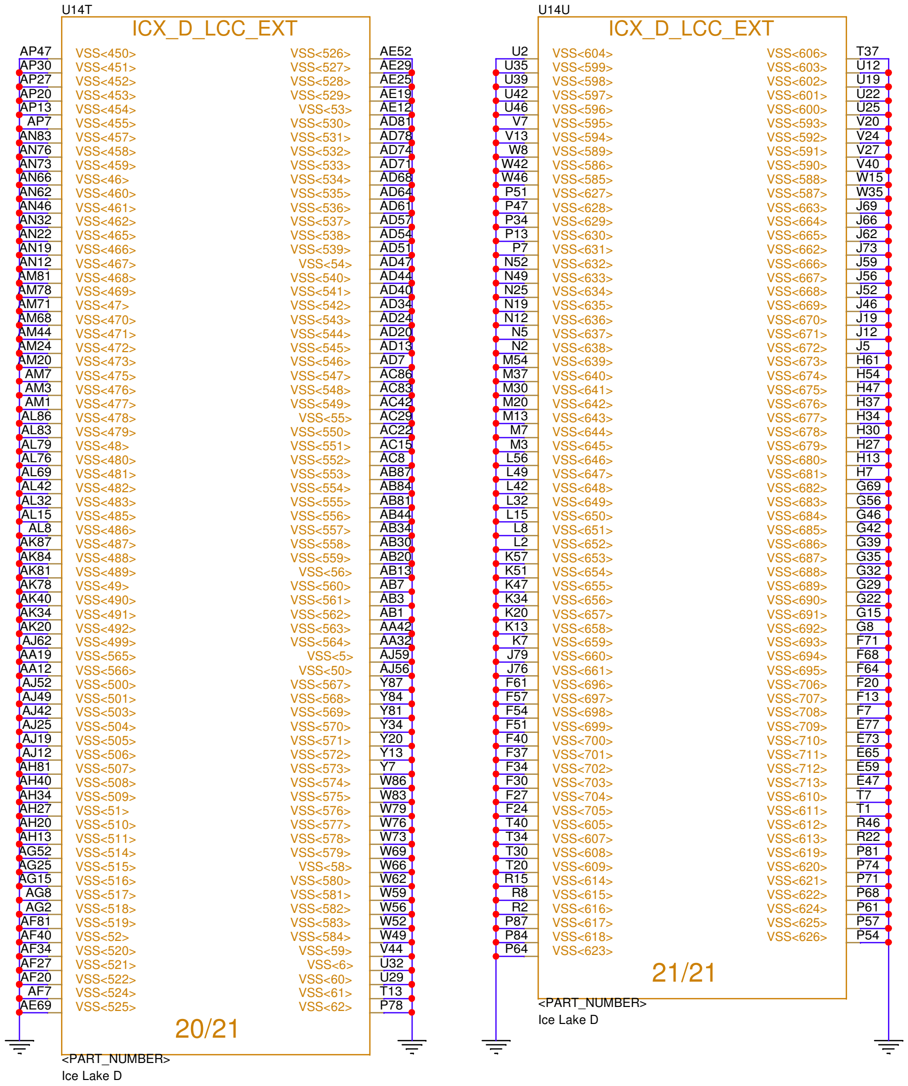
SoC VSS2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AAEON Technology INC.			
Title	**SoC VSS2**		
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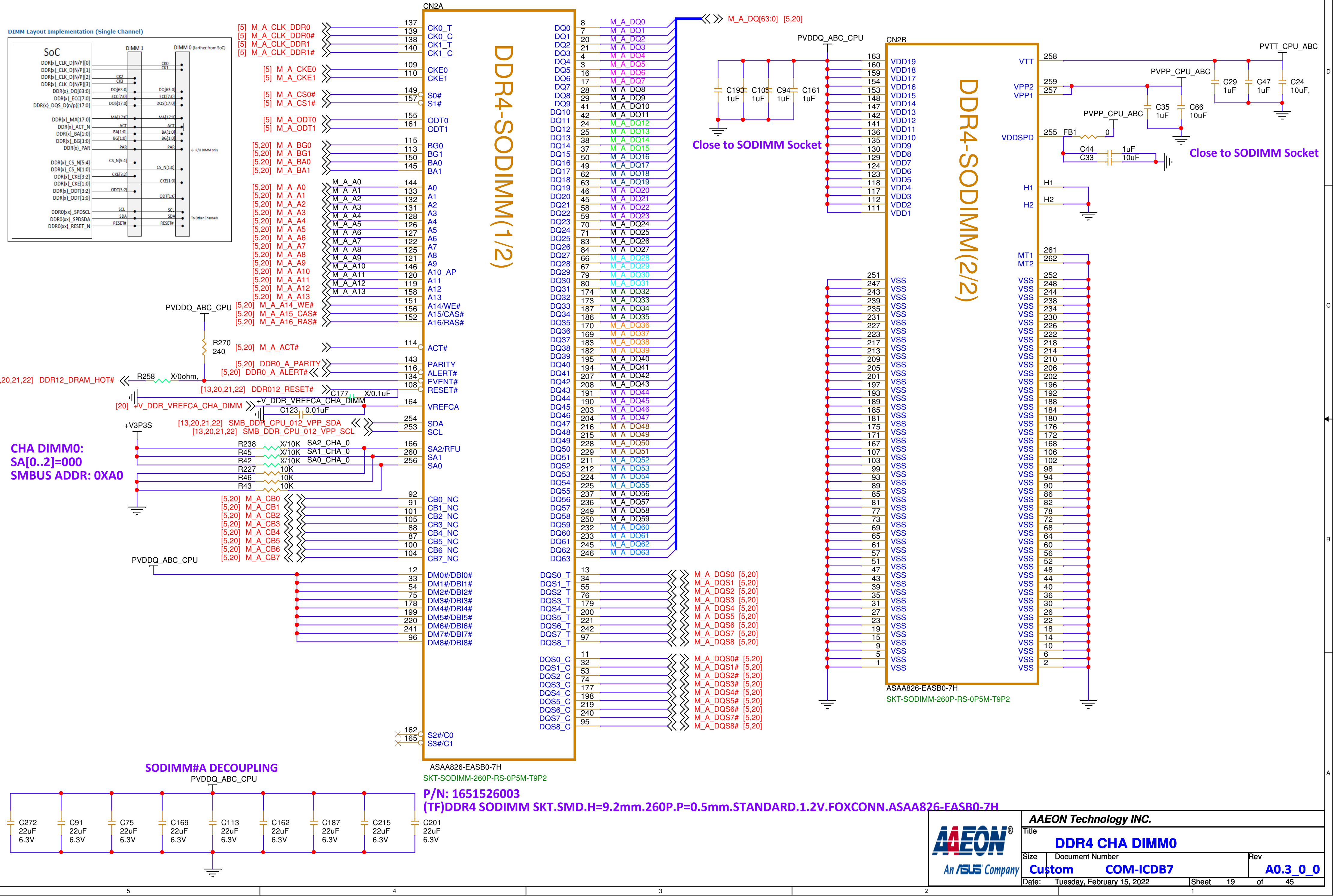
DDR4 CHA DIMM0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SoC
DIMM 1
DIMM 0 (farther from SoC)
R/U DIMM only
To Other Channels
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CK0_C
CK1_T
CK1_C
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S0#
S1#
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ODT1
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[5,20] M_A_BG1
[5,20] M_A_BA0
[5,20] M_A_BA1
BG0
BG1
BA0
BA1
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A0 … A13
A10_AP
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[5,20] M_A_A15_CAS#
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A15/CAS#
A16/RAS#
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R270
240
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[5,20] DDR0_A_ALERT#
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ALERT#
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R258
X/0ohm,
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X/0.1uF
+V_DDR_VREFCA_CHA_DIMM
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0.01uF
VREFCA
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[13,20,21,22] SMB_DDR_CPU_012_VPP_SCL
SDA
SCL
+V3P3S
R238
R45
R42
X/10K
SA2_CHA_0
SA1_CHA_0
SA0_CHA_0
R227
R46
R43
10K
SA2/RFU
SA1
SA0
CHA DIMM0:
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SMBUS ADDR: 0XA0
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S2#/C0
S3#/C1
ASAA826-EASB0-7H
SKT-SODIMM-260P-RS-0P5M-T9P2
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M_A_DQS0 … M_A_DQS8 [5,20]
DQS0_C … DQS8_C
M_A_DQS0# … M_A_DQS8# [5,20]
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C105 1uF
C94 1uF
C161 1uF
Close to SODIMM Socket
CN2B
DDR4-SODIMM(2/2)
VDD1 … VDD19
VTT
PVTT_CPU_ABC
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C47 1uF
C24 10uF,
VPP2
VPP1
PVPP_CPU_ABC
C35 1uF
C66 10uF
VDDSPD
FB1
0
C44 1uF
C33 10uF
Close to SODIMM Socket
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H2
MT1
MT2
VSS
ASAA826-EASB0-7H
SKT-SODIMM-260P-RS-0P5M-T9P2
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PVDDQ_ABC_CPU
C272 22uF 6.3V
C91 22uF 6.3V
C75 22uF 6.3V
C169 22uF 6.3V
C113 22uF 6.3V
C162 22uF 6.3V
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AAEON An ASUS Company	AAEON Technology INC.
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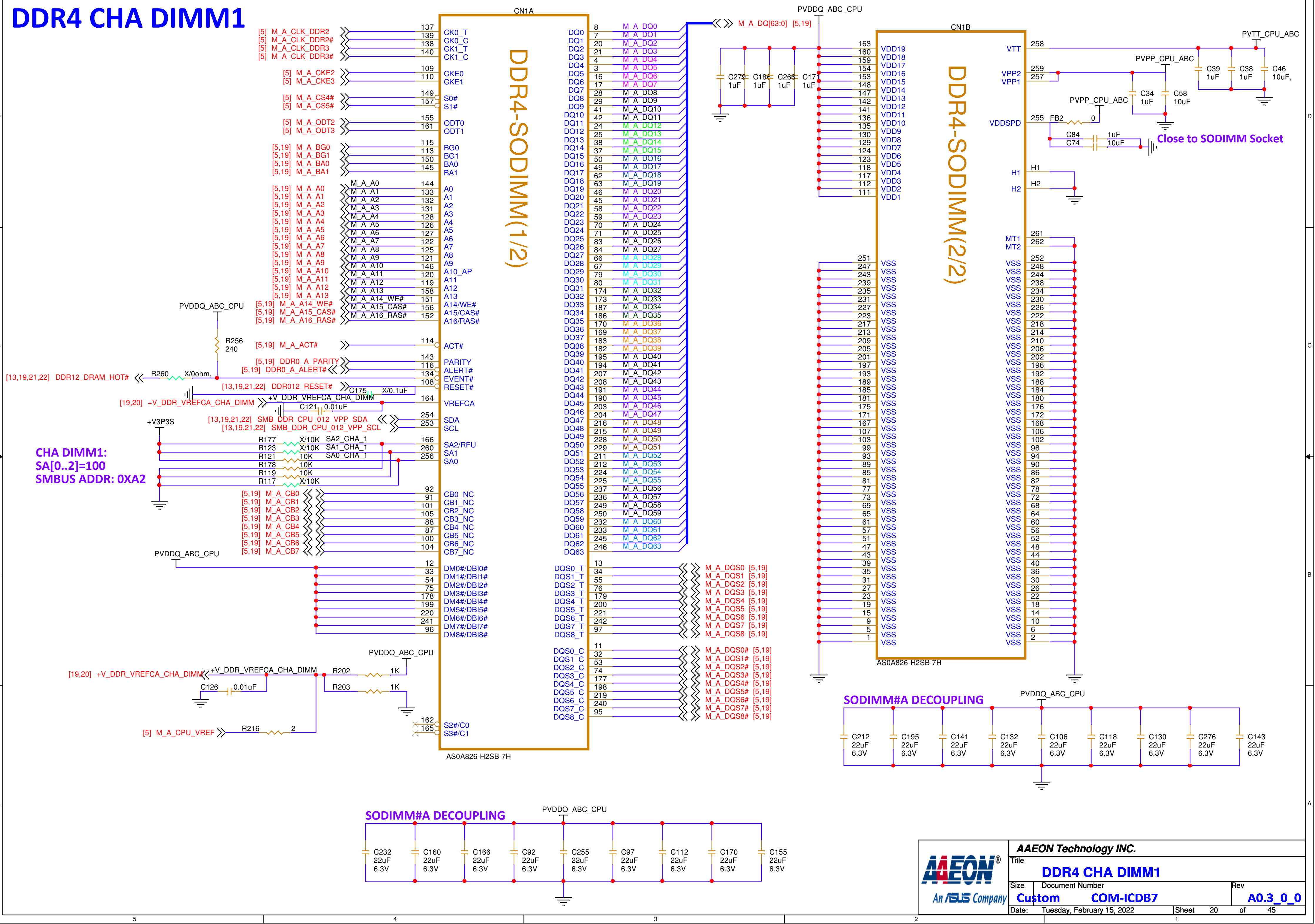
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C121 0.01uF
[13,19,21,22] SMB_DDR_CPU_012_VPP_SDA 254 SDA
[13,19,21,22] SMB_DDR_CPU_012_VPP_SCL 253 SCL
+V3P3S
R177 X/10K SA2_CHA_1 166 SA2/RFU
R123 X/10K SA1_CHA_1 260 SA1
R121 10K SA0_CHA_1 256 SA0
R178 10K
R119 10K
R117 X/10K
CHA DIMM1:
SA[0..2]=100
SMBUS ADDR: 0XA2
[5,19] M_A_CB0 92 CB0_NC
[5,19] M_A_CB1 91 CB1_NC
[5,19] M_A_CB2 101 CB2_NC
[5,19] M_A_CB3 105 CB3_NC
[5,19] M_A_CB4 88 CB4_NC
[5,19] M_A_CB5 87 CB5_NC
[5,19] M_A_CB6 100 CB6_NC
[5,19] M_A_CB7 104 CB7_NC
PVDDQ_ABC_CPU
12 DM0#/DBI0#
33 DM1#/DBI1#
54 DM2#/DBI2#
75 DM3#/DBI3#
178 DM4#/DBI4#
199 DM5#/DBI5#
220 DM6#/DBI6#
241 DM7#/DBI7#
96 DM8#/DBI8#
PVDDQ_ABC_CPU
[19,20] +V_DDR_VREFCA_CHA_DIMM +V_DDR_VREFCA_CHA_DIMM R202 1K
R203 1K
C126 0.01uF
[5] M_A_CPU_VREF R216 2
162 S2#/C0
165 S3#/C1
AS0A826-H2SB-7H
DQ0 8 M_A_DQ0
DQ1 7 M_A_DQ1
DQ2 20 M_A_DQ2
DQ3 21 M_A_DQ3
DQ4 4 M_A_DQ4
DQ5 3 M_A_DQ5
DQ6 16 M_A_DQ6
DQ7 17 M_A_DQ7
DQ8 28 M_A_DQ8
DQ9 29 M_A_DQ9
DQ10 41 M_A_DQ10
DQ11 42 M_A_DQ11
DQ12 24 M_A_DQ12
DQ13 25 M_A_DQ13
DQ14 38 M_A_DQ14
DQ15 37 M_A_DQ15
DQ16 50 M_A_DQ16
DQ17 49 M_A_DQ17
DQ18 62 M_A_DQ18
DQ19 63 M_A_DQ19
DQ20 46 M_A_DQ20
DQ21 45 M_A_DQ21
DQ22 58 M_A_DQ22
DQ23 59 M_A_DQ23
DQ24 70 M_A_DQ24
DQ25 71 M_A_DQ25
DQ26 83 M_A_DQ26
DQ27 84 M_A_DQ27
DQ28 66 M_A_DQ28
DQ29 67 M_A_DQ29
DQ30 79 M_A_DQ30
DQ31 80 M_A_DQ31
DQ32 174 M_A_DQ32
DQ33 173 M_A_DQ33
DQ34 187 M_A_DQ34
DQ35 186 M_A_DQ35
DQ36 170 M_A_DQ36
DQ37 169 M_A_DQ37
DQ38 183 M_A_DQ38
DQ39 182 M_A_DQ39
DQ40 195 M_A_DQ40
DQ41 194 M_A_DQ41
DQ42 207 M_A_DQ42
DQ43 208 M_A_DQ43
DQ44 191 M_A_DQ44
DQ45 190 M_A_DQ45
DQ46 203 M_A_DQ46
DQ47 204 M_A_DQ47
DQ48 216 M_A_DQ48
DQ49 215 M_A_DQ49
DQ50 228 M_A_DQ50
DQ51 229 M_A_DQ51
DQ52 211 M_A_DQ52
DQ53 212 M_A_DQ53
DQ54 224 M_A_DQ54
DQ55 225 M_A_DQ55
DQ56 237 M_A_DQ56
DQ57 236 M_A_DQ57
DQ58 249 M_A_DQ58
DQ59 250 M_A_DQ59
DQ60 232 M_A_DQ60
DQ61 233 M_A_DQ61
DQ62 245 M_A_DQ62
DQ63 246 M_A_DQ63
M_A_DQ[63:0] [5,19]
DQS0_T 13 M_A_DQS0 [5,19]
DQS1_T 34 M_A_DQS1 [5,19]
DQS2_T 55 M_A_DQS2 [5,19]
DQS3_T 76 M_A_DQS3 [5,19]
DQS4_T 179 M_A_DQS4 [5,19]
DQS5_T 200 M_A_DQS5 [5,19]
DQS6_T 221 M_A_DQS6 [5,19]
DQS7_T 242 M_A_DQS7 [5,19]
DQS8_T 97 M_A_DQS8 [5,19]
DQS0_C 11 M_A_DQS0# [5,19]
DQS1_C 32 M_A_DQS1# [5,19]
DQS2_C 53 M_A_DQS2# [5,19]
DQS3_C 74 M_A_DQS3# [5,19]
DQS4_C 177 M_A_DQS4# [5,19]
DQS5_C 198 M_A_DQS5# [5,19]
DQS6_C 219 M_A_DQS6# [5,19]
DQS7_C 240 M_A_DQS7# [5,19]
DQS8_C 95 M_A_DQS8# [5,19]
PVDDQ_ABC_CPU
CN1B
DDR4-SODIMM(2/2)
C279 1uF
C186 1uF
C266 1uF
C17 1uF
163 VDD19
160 VDD18
159 VDD17
154 VDD16
153 VDD15
148 VDD14
147 VDD13
142 VDD12
141 VDD11
136 VDD10
135 VDD9
130 VDD8
129 VDD7
124 VDD6
123 VDD5
118 VDD4
117 VDD3
112 VDD2
111 VDD1
PVTT_CPU_ABC
VTT 258
C39 1uF
C38 1uF
C46 10uF,
PVPP_CPU_ABC
VPP2 259
VPP1 257
PVPP_CPU_ABC
C34 1uF
C58 10uF
VDDSPD 255 FB2 0
C84 1uF
C74 10uF
Close to SODIMM Socket
H1 H1
H2 H2
MT1 261
MT2 262
VSS 251 247 243 239 235 231 227 223 217 213 209 205 201 197 193 189 185 181 175 171 167 107 103 99 93 89 85 81 77 73 69 65 61 57 51 47 43 39 35 31 27 23 19 15 9 5 1
VSS 252 248 244 238 234 230 226 222 218 214 210 206 202 196 192 188 184 180 176 172 168 106 102 98 94 90 86 82 78 72 68 64 60 56 52 48 44 40 36 30 26 22 18 14 10 6 2
AS0A826-H2SB-7H
SODIMM#A DECOUPLING
PVDDQ_ABC_CPU
C212 22uF 6.3V
C195 22uF 6.3V
C141 22uF 6.3V
C132 22uF 6.3V
C106 22uF 6.3V
C118 22uF 6.3V
C130 22uF 6.3V
C276 22uF 6.3V
C143 22uF 6.3V
SODIMM#A DECOUPLING
PVDDQ_ABC_CPU
C232 22uF 6.3V
C160 22uF 6.3V
C166 22uF 6.3V
C92 22uF 6.3V
C255 22uF 6.3V
C97 22uF 6.3V
C112 22uF 6.3V
C170 22uF 6.3V
C155 22uF 6.3V
5 4 3 2 1
D C B A

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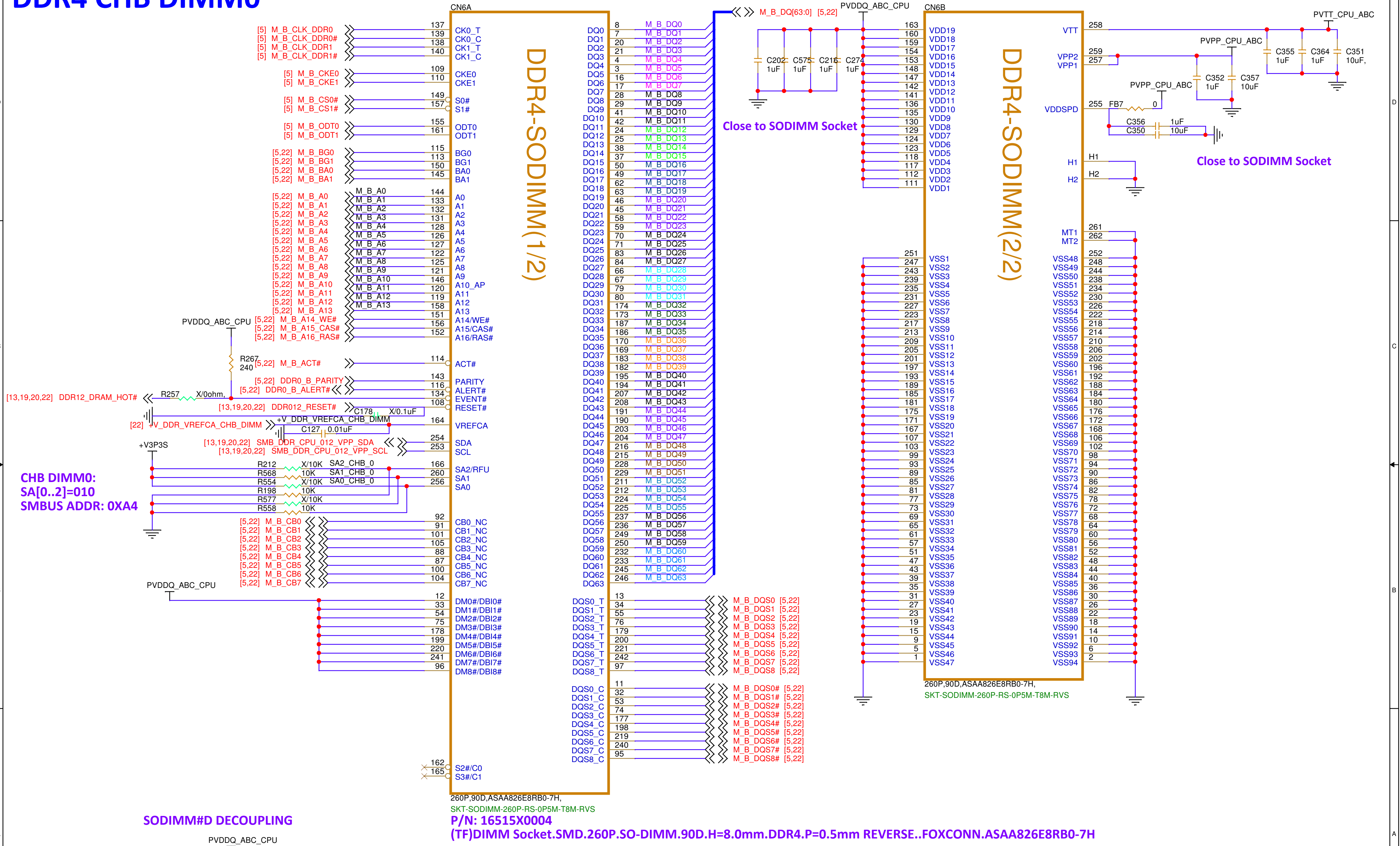
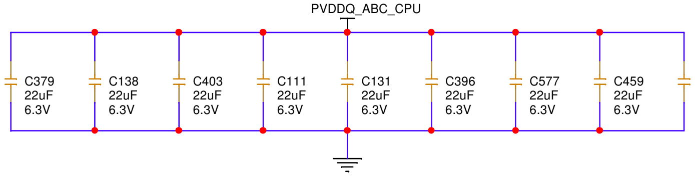

CN6A
DDR4-SODIMM(1/2)
[5] M_B_CLK_DDR0 — 137 CK0_T
[5] M_B_CLK_DDR0# — 139 CK0_C
[5] M_B_CLK_DDR1 — 138 CK1_T
[5] M_B_CLK_DDR1# — 140 CK1_C
[5] M_B_CKE0 — 109 CKE0
[5] M_B_CKE1 — 110 CKE1
[5] M_B_CS0# — 149 S0#
[5] M_B_CS1# — 157 S1#
[5] M_B_ODT0 — 155 ODT0
[5] M_B_ODT1 — 161 ODT1
[5,22] M_B_BG0 — 115 BG0
[5,22] M_B_BG1 — 113 BG1
[5,22] M_B_BA0 — 150 BA0
[5,22] M_B_BA1 — 145 BA1
[5,22] M_B_A0 … M_B_A13 — A0 … A13
[5,22] M_B_A14_WE# — 151 A14/WE#
[5,22] M_B_A15_CAS# — 156 A15/CAS#
[5,22] M_B_A16_RAS# — 152 A16/RAS#
PVDDQ_ABC_CPU
R267 240
[5,22] M_B_ACT# — 114 ACT#
[5,22] DDR0_B_PARITY — 143 PARITY
[5,22] DDR0_B_ALERT# — 116 ALERT#
[13,19,20,22] DDR12_DRAM_HOT# — R257 X/0ohm — 134 EVENT#
[13,19,20,22] DDR012_RESET# — 108 RESET#
C178 X/0.1uF
[22] +V_DDR_VREFCA_CHB_DIMM — 164 VREFCA
C127 0.01uF
[13,19,20,22] SMB_DDR_CPU_012_VPP_SDA — 254 SDA
[13,19,20,22] SMB_DDR_CPU_012_VPP_SCL — 253 SCL
+V3P3S
R212 X/10K SA2_CHB_0 — 166 SA2/RFU
R568 10K SA1_CHB_0 — 260 SA1
R554 X/10K SA0_CHB_0 — 256 SA0
R198 10K
R577 X/10K
R558 10K
CHB DIMM0:
SA[0..2]=010
SMBUS ADDR: 0XA4
[5,22] M_B_CB0 … M_B_CB7 — CB0_NC … CB7_NC
PVDDQ_ABC_CPU — DM0#/DBI0# … DM8#/DBI8#
162 S2#/C0
165 S3#/C1
DQ0 … DQ63 — M_B_DQ0 … M_B_DQ63
M_B_DQ[63:0] [5,22]
DQS0_T … DQS8_T — M_B_DQS0 … M_B_DQS8 [5,22]
DQS0_C … DQS8_C — M_B_DQS0# … M_B_DQS8# [5,22]
260P,90D,ASAA826E8RB0-7H,
SKT-SODIMM-260P-RS-0P5M-T8M-RVS
CN6B
DDR4-SODIMM(2/2)
PVDDQ_ABC_CPU
C202 1uF
C575 1uF
C216 1uF
C274 1uF
VDD1 … VDD19
Close to SODIMM Socket
PVTT_CPU_ABC
258 VTT
C355 1uF
C364 1uF
C351 10uF,
PVPP_CPU_ABC
259 VPP2
257 VPP1
C352 1uF
C357 10uF
PVPP_CPU_ABC
255 VDDSPD FB7 0
C356 1uF
C350 10uF
Close to SODIMM Socket
H1
H2
261 MT1
262 MT2
VSS1 … VSS94
260P,90D,ASAA826E8RB0-7H,
SKT-SODIMM-260P-RS-0P5M-T8M-RVS

P/N: 16515X0004

(TF)DIMM Socket.SMD.260P.SO-DIMM.90D.H=8.0mm.DDR4.P=0.5mm REVERSE..FOXCONN.ASAA826E8RB0-7H

SODIMM#D DECOUPLING


PVDDQ_ABC_CPU
C379 22uF 6.3V
C138 22uF 6.3V
C403 22uF 6.3V
C111 22uF 6.3V
C131 22uF 6.3V
C396 22uF 6.3V
C577 22uF 6.3V
C459 22uF 6.3V
C86 22uF 6.3V

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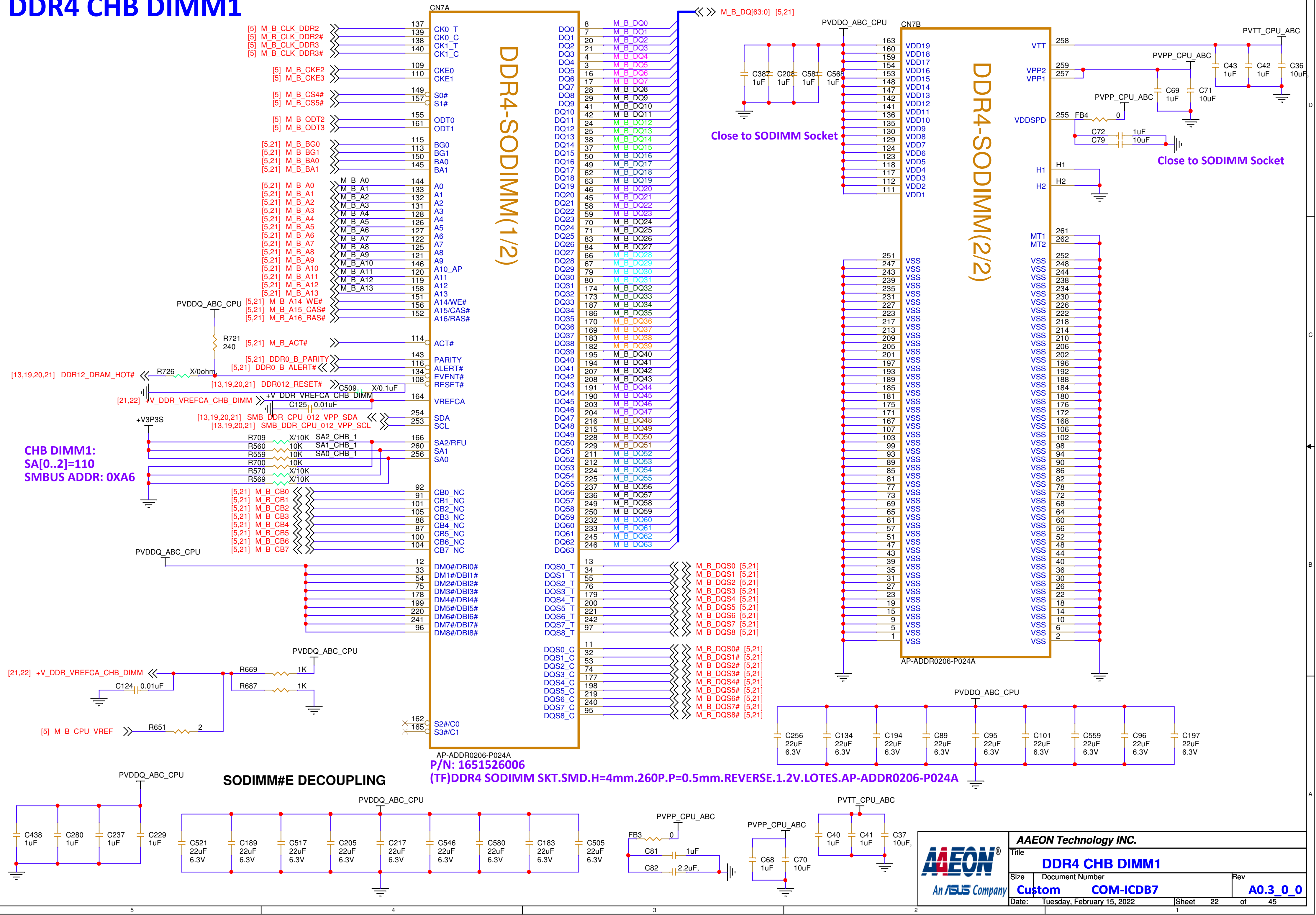
CN7A
DDR4-SODIMM(1/2)
[5] M_B_CLK_DDR2
[5] M_B_CLK_DDR2#
[5] M_B_CLK_DDR3
[5] M_B_CLK_DDR3#
[5] M_B_CKE2
[5] M_B_CKE3
[5] M_B_CS4#
[5] M_B_CS5#
[5] M_B_ODT2
[5] M_B_ODT3
[5,21] M_B_BG0
[5,21] M_B_BG1
[5,21] M_B_BA0
[5,21] M_B_BA1
[5,21] M_B_A0 … M_B_A13
[5,21] M_B_A14_WE#
[5,21] M_B_A15_CAS#
[5,21] M_B_A16_RAS#
[5,21] M_B_ACT#
[5,21] DDR0_B_PARITY
[5,21] DDR0_B_ALERT#
[13,19,20,21] DDR12_DRAM_HOT#
[13,19,20,21] DDR012_RESET#
[21,22] +V_DDR_VREFCA_CHB_DIMM
+V_DDR_VREFCA_CHB_DIMM
[13,19,20,21] SMB_DDR_CPU_012_VPP_SDA
[13,19,20,21] SMB_DDR_CPU_012_VPP_SCL
PVDDQ_ABC_CPU
R721 240
R726 X/0ohm
C509 X/0.1uF
C125 0.01uF
+V3P3S
R709 X/10K SA2_CHB_1
R560 10K SA1_CHB_1
R559 10K SA0_CHB_1
R700 10K
R570 X/10K
R569 X/10K
CHB DIMM1:
SA[0..2]=110
SMBUS ADDR: 0XA6
[5,21] M_B_CB0 … M_B_CB7
CK0_T CK0_C CK1_T CK1_C CKE0 CKE1 S0# S1# ODT0 ODT1 BG0 BG1 BA0 BA1
A0 … A9 A10_AP A11 A12 A13 A14/WE# A15/CAS# A16/RAS#
ACT# PARITY ALERT# EVENT# RESET# VREFCA SDA SCL SA2/RFU SA1 SA0
CB0_NC … CB7_NC
DM0#/DBI0# … DM8#/DBI8#
S2#/C0 S3#/C1
DQ0 … DQ63
M_B_DQ0 … M_B_DQ63
M_B_DQ[63:0] [5,21]
DQS0_T … DQS8_T
M_B_DQS0 … M_B_DQS8 [5,21]
DQS0_C … DQS8_C
M_B_DQS0# … M_B_DQS8# [5,21]
AP-ADDR0206-P024A
P/N: 1651526006
(TF)DDR4 SODIMM SKT.SMD.H=4mm.260P.P=0.5mm.REVERSE.1.2V.LOTES.AP-ADDR0206-P024A
[21,22] +V_DDR_VREFCA_CHB_DIMM
C124 0.01uF
R669 1K
R687 1K
[5] M_B_CPU_VREF
R651 2
CN7B
DDR4-SODIMM(2/2)
PVDDQ_ABC_CPU
VDD1 … VDD19
C387 1uF
C208 1uF
C581 1uF
C568 1uF
Close to SODIMM Socket
PVTT_CPU_ABC
VTT
C43 1uF
C42 1uF
C36 10uF,
PVPP_CPU_ABC
VPP2 VPP1
C69 1uF
C71 10uF
VDDSPD
FB4 0
C72 1uF
C79 10uF
Close to SODIMM Socket
H1 H2
MT1 MT2
VSS
AP-ADDR0206-P024A
PVDDQ_ABC_CPU
C256 22uF 6.3V
C134 22uF 6.3V
C194 22uF 6.3V
C89 22uF 6.3V
C95 22uF 6.3V
C101 22uF 6.3V
C559 22uF 6.3V
C96 22uF 6.3V
C197 22uF 6.3V
SODIMM#E DECOUPLING
PVDDQ_ABC_CPU
C438 1uF
C280 1uF
C237 1uF
C229 1uF
C521 22uF 6.3V
C189 22uF 6.3V
C517 22uF 6.3V
C205 22uF 6.3V
C217 22uF 6.3V
C546 22uF 6.3V
C580 22uF 6.3V
C183 22uF 6.3V
C505 22uF 6.3V
PVPP_CPU_ABC
FB3 0
C81 1uF
C82 2.2uF,
C68 1uF
C70 10uF
PVTT_CPU_ABC
C40 1uF
C41 1uF
C37 10uF,

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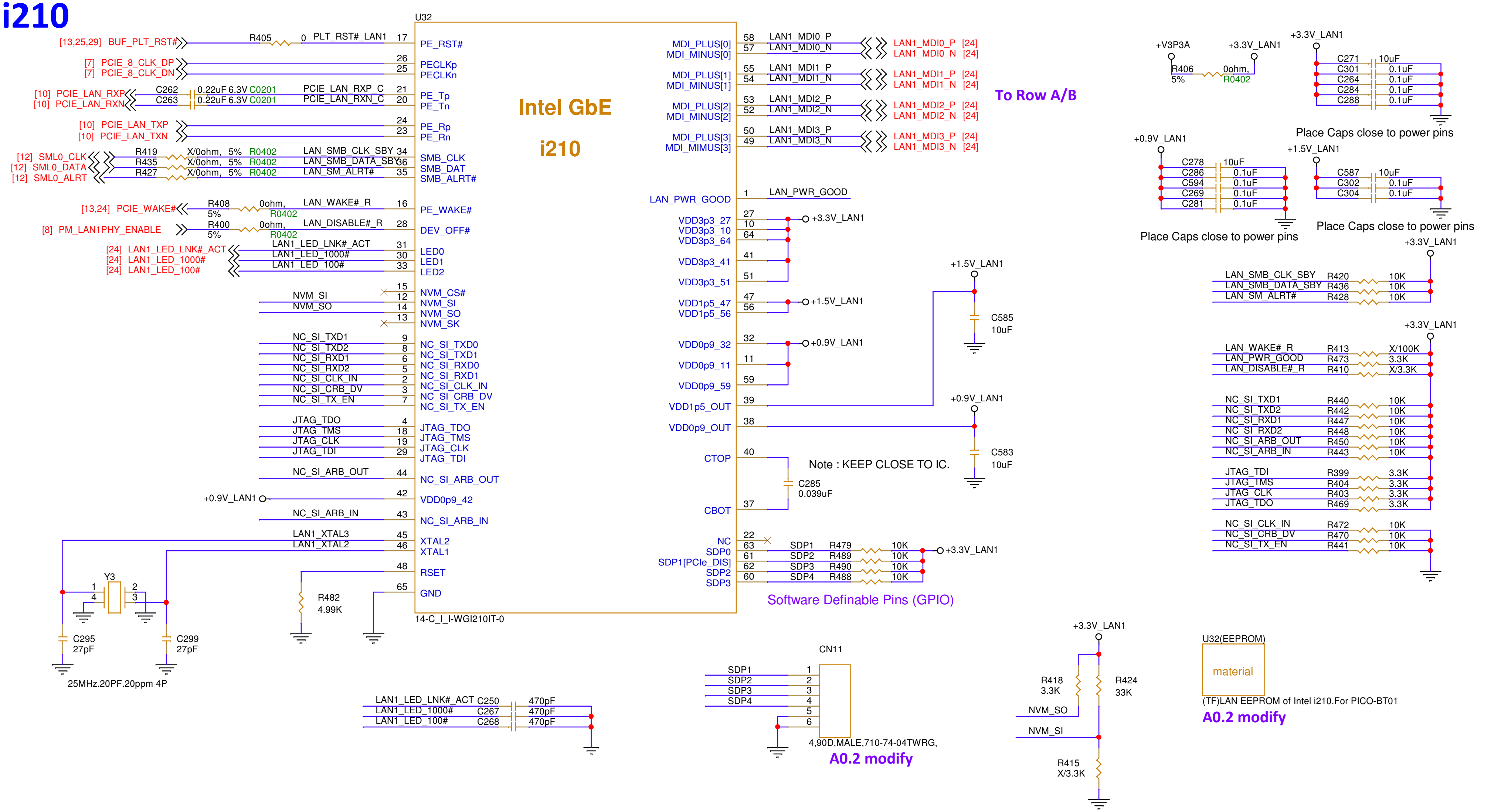
U32
Intel GbE
i210
14-C_I_I-WGI210IT-0
[13,25,29] BUF_PLT_RST#
R405 0 PLT_RST#_LAN1 17 PE_RST#
[7] PCIE_8_CLK_DP
[7] PCIE_8_CLK_DN
26 PECLKp
25 PECLKn
[10] PCIE_LAN_RXP
[10] PCIE_LAN_RXN
C262 0.22uF 6.3V C0201 PCIE_LAN_RXP_C 21 PE_Tp
C263 0.22uF 6.3V C0201 PCIE_LAN_RXN_C 20 PE_Tn
[10] PCIE_LAN_TXP
[10] PCIE_LAN_TXN
24 PE_Rp
23 PE_Rn
[12] SML0_CLK
[12] SML0_DATA
[12] SML0_ALRT
R419 X/0ohm, 5% R0402 LAN_SMB_CLK_SBY 34 SMB_CLK
R435 X/0ohm, 5% R0402 LAN_SMB_DATA_SBY 36 SMB_DAT
R427 X/0ohm, 5% R0402 LAN_SM_ALRT# 35 SMB_ALRT#
[13,24] PCIE_WAKE#
R408 5% 0ohm, R0402 LAN_WAKE#_R 16 PE_WAKE#
[8] PM_LAN1PHY_ENABLE
R400 5% 0ohm, R0402 LAN_DISABLE#_R 28 DEV_OFF#
[24] LAN1_LED_LNK#_ACT 31 LED0
[24] LAN1_LED_1000# 30 LED1
[24] LAN1_LED_100# 33 LED2
15 NVM_CS#
NVM_SI 12 NVM_SI
NVM_SO 14 NVM_SO
13 NVM_SK
NC_SI_TXD1 9 NC_SI_TXD0
NC_SI_TXD2 8 NC_SI_TXD1
NC_SI_RXD1 6 NC_SI_RXD0
NC_SI_RXD2 5 NC_SI_RXD1
NC_SI_CLK_IN 2 NC_SI_CLK_IN
NC_SI_CRB_DV 3 NC_SI_CRB_DV
NC_SI_TX_EN 7 NC_SI_TX_EN
JTAG_TDO 4 JTAG_TDO
JTAG_TMS 18 JTAG_TMS
JTAG_CLK 19 JTAG_CLK
JTAG_TDI 29 JTAG_TDI
NC_SI_ARB_OUT 44 NC_SI_ARB_OUT
+0.9V_LAN1 42 VDD0p9_42
NC_SI_ARB_IN 43 NC_SI_ARB_IN
LAN1_XTAL3 45 XTAL2
LAN1_XTAL2 46 XTAL1
48 RSET
65 GND
R482 4.99K
Y3 1 2 4 3
C295 27pF
C299 27pF
25MHz.20PF.20ppm 4P
MDI_PLUS[0] 58 LAN1_MDI0_P LAN1_MDI0_P [24]
MDI_MINUS[0] 57 LAN1_MDI0_N LAN1_MDI0_N [24]
MDI_PLUS[1] 55 LAN1_MDI1_P LAN1_MDI1_P [24]
MDI_MINUS[1] 54 LAN1_MDI1_N LAN1_MDI1_N [24]
MDI_PLUS[2] 53 LAN1_MDI2_P LAN1_MDI2_P [24]
MDI_MINUS[2] 52 LAN1_MDI2_N LAN1_MDI2_N [24]
MDI_PLUS[3] 50 LAN1_MDI3_P LAN1_MDI3_P [24]
MDI_MIMUS[3] 49 LAN1_MDI3_N LAN1_MDI3_N [24]
To Row A/B
LAN_PWR_GOOD 1 LAN_PWR_GOOD
VDD3p3_27 27
VDD3p3_10 10
VDD3p3_64 64
VDD3p3_41 41
VDD3p3_51 51
+3.3V_LAN1
VDD1p5_47 47
VDD1p5_56 56
+1.5V_LAN1
VDD0p9_32 32
VDD0p9_11 11
VDD0p9_59 59
+0.9V_LAN1
VDD1p5_OUT 39
VDD0p9_OUT 38
CTOP 40
CBOT 37
C285 0.039uF
Note : KEEP CLOSE TO IC.
+1.5V_LAN1 C585 10uF
+0.9V_LAN1 C583 10uF
NC 22
SDP0 63 SDP1 R479 10K
SDP1[PCIe_DIS] 61 SDP2 R489 10K
SDP2 62 SDP3 R490 10K
SDP3 60 SDP4 R488 10K
+3.3V_LAN1
Software Definable Pins (GPIO)
+V3P3A R406 5% 0ohm, R0402 +3.3V_LAN1
+3.3V_LAN1
C271 10uF
C301 0.1uF
C264 0.1uF
C284 0.1uF
C288 0.1uF
Place Caps close to power pins
+0.9V_LAN1
C278 10uF
C286 0.1uF
C594 0.1uF
C269 0.1uF
C281 0.1uF
Place Caps close to power pins
+1.5V_LAN1
C587 10uF
C302 0.1uF
C304 0.1uF
Place Caps close to power pins
+3.3V_LAN1
LAN_SMB_CLK_SBY R420 10K
LAN_SMB_DATA_SBY R436 10K
LAN_SM_ALRT# R428 10K
+3.3V_LAN1
LAN_WAKE#_R R413 X/100K
LAN_PWR_GOOD R473 3.3K
LAN_DISABLE#_R R410 X/3.3K
NC_SI_TXD1 R440 10K
NC_SI_TXD2 R442 10K
NC_SI_RXD1 R447 10K
NC_SI_RXD2 R448 10K
NC_SI_ARB_OUT R450 10K
NC_SI_ARB_IN R443 10K
JTAG_TDI R399 3.3K
JTAG_TMS R404 3.3K
JTAG_CLK R403 3.3K
JTAG_TDO R469 3.3K
NC_SI_CLK_IN R472 10K
NC_SI_CRB_DV R470 10K
NC_SI_TX_EN R441 10K
LAN1_LED_LNK#_ACT C250 470pF
LAN1_LED_1000# C267 470pF
LAN1_LED_100# C268 470pF
CN11
SDP1 1
SDP2 2
SDP3 3
SDP4 4
5
6
4,90D,MALE,710-74-04TWRG,
A0.2 modify
+3.3V_LAN1
R418 3.3K
R424 33K
NVM_SO
NVM_SI
R415 X/3.3K
U32(EEPROM)
material
(TF)LAN EEPROM of Intel i210.For PICO-BT01
A0.2 modify

```
ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY
```

```
SPEED LED
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps
```

LEDs	Mode	Function
LED0	0100	LINK/ACTIVITY
LED1	0111	LINK 1000
LED2	0110	LINK 100

AAEON Technology INC.

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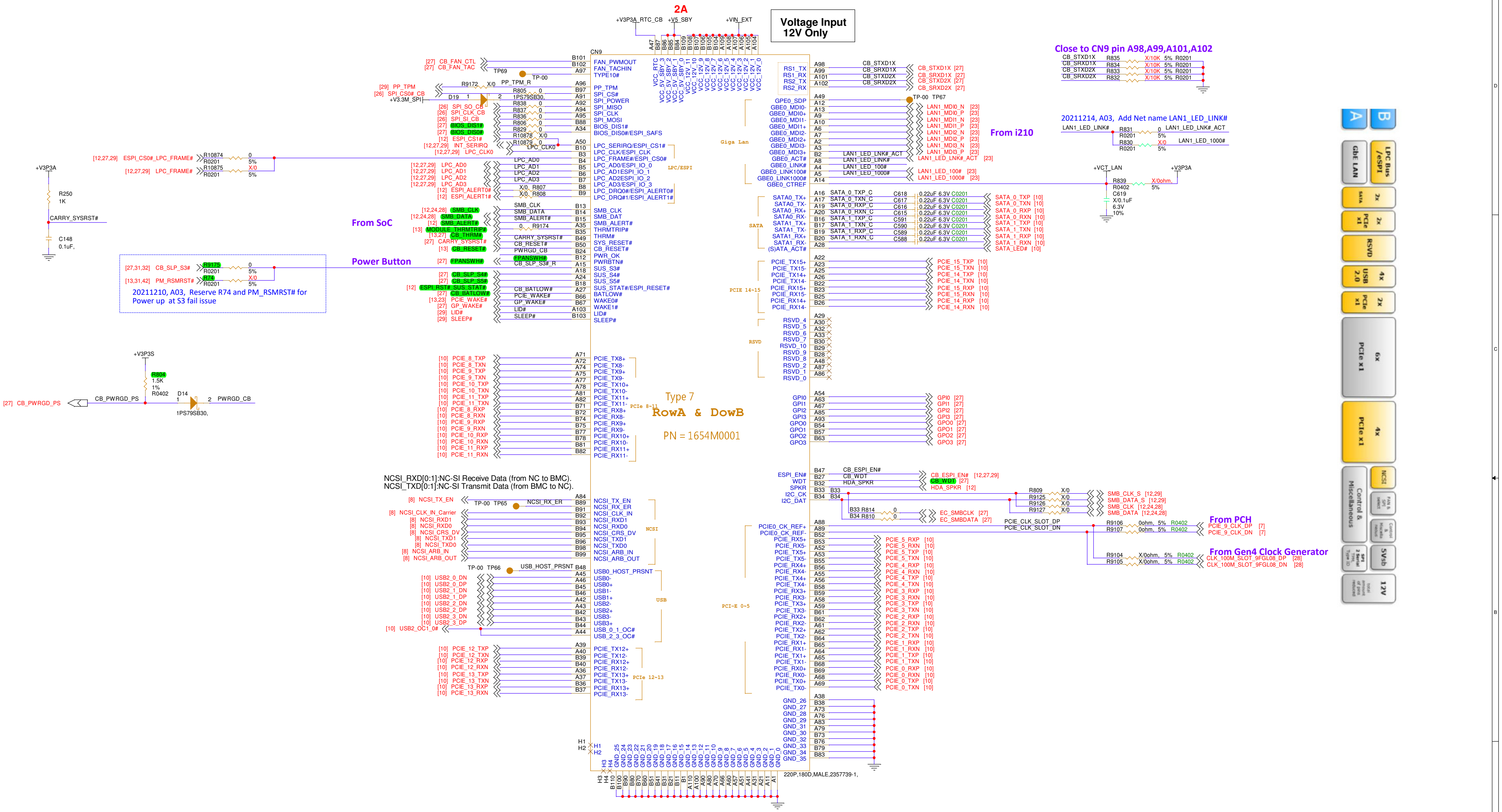
Row A/B


2A
Voltage Input
12V Only
Close to CN9 pin A98,A99,A101,A102
From i210
20211214, A03, Add Net name LAN1_LED_LINK#
From SoC
Power Button
20211210, A03, Reserve R74 and PM_RSMRST# for Power up at S3 fail issue
Type 7
RowA & DowB
PN = 1654M0001
NCSI_RXD[0:1]:NC-SI Receive Data (from NC to BMC).
NCSI_TXD[0:1]:NC-SI Transmit Data (from BMC to NC).
From PCH
From Gen4 Clock Generator
CN9
220P,180D,MALE,2357739-1,
Giga Lan
LPC/ESPI
SATA
PCIE 14~15
RSVD
PCIe 8~11
NCSI
USB
PCI-E 0~5
PCIe 12~13
+V3P3A_RTC_CB
+V5_SBY
+VIN_EXT
+V3P3A
+V3P3S
+VCT_LAN
CARRY_SYSRST#
CB_PWRGD_PS
PWRGD_CB
SMB_CLK_S
SMB_DATA_S
PCIE_9_CLK_DP
PCIE_9_CLK_DN
CLK_100M_SLOT_9FGL08_DP
CLK_100M_SLOT_9FGL08_DN
LAN1_LED_LINK#_ACT
LAN1_LED_1000#
A
B
GbE LAN
LPC Bus /eSPI
SATA
2x
PCIe x1
RSVD
USB 2.0
4x
6x
PCIe x4
NCSI
Control & Miscellaneous
SVsb
12V

AAEON Technology INC.

AAEON An ASUS Company

Title: Row A/B

Size: A2

Document Number: COM-ICDB7

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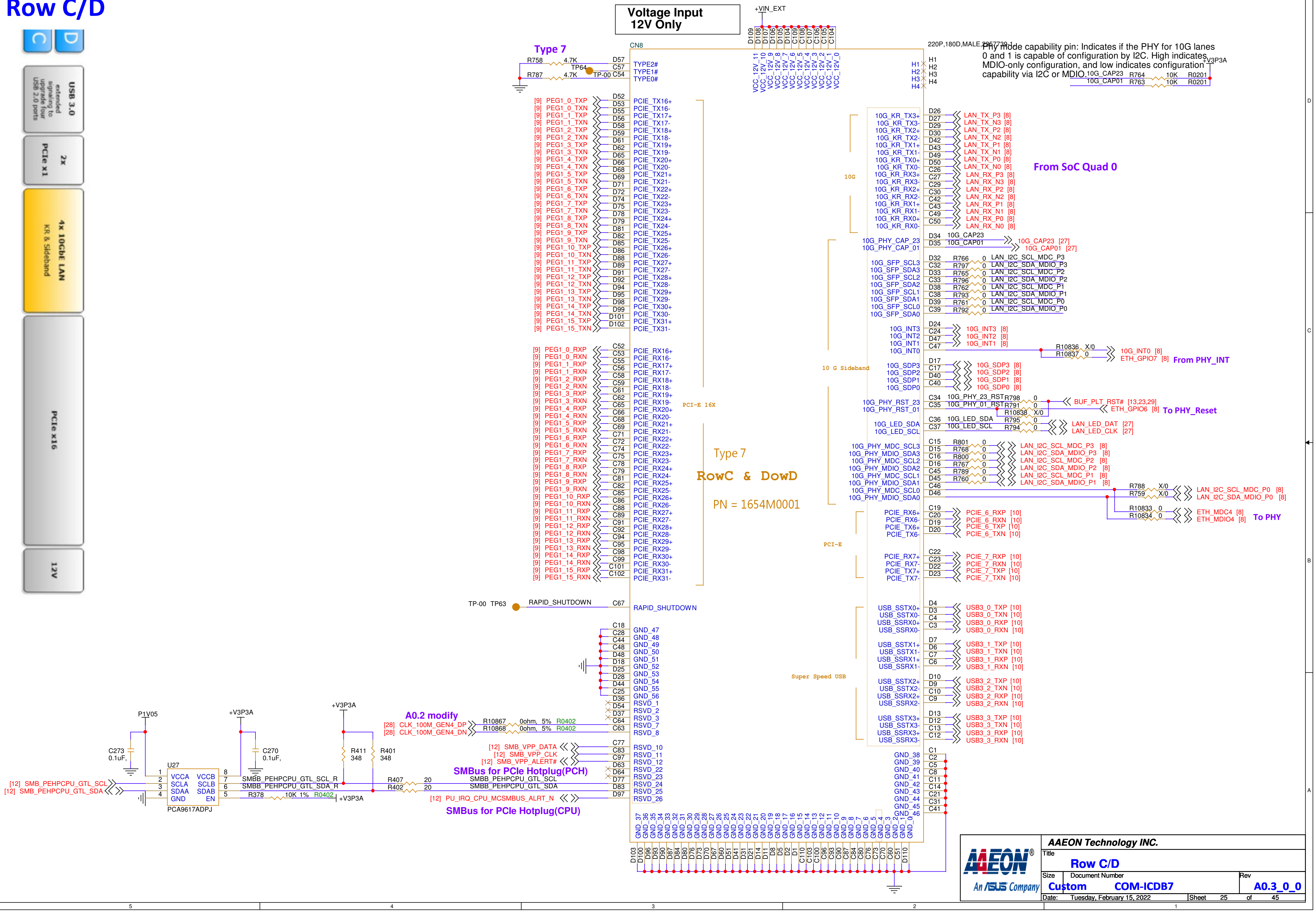
Row C/D


C
D
USB 3.0 extended signaling to upgrade four USB 2.0 ports
2x PCIe x1
4x 10GbE LAN KR & Sideband
PCIe x16
12V
Voltage Input 12V Only
+VIN_EXT
CN8
220P,180D,MALE,2957739
Type 7
R758 4.7K
TP64
R787 4.7K
TP-00
TYPE2#
TYPE1#
TYPE0#
VCC_12V_1 … VCC_12V_11
H1 H2 H3 H4
Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO.
+V3P3A
10G_CAP23 R764 10K R0201
10G_CAP01 R763 10K R0201
[9] PEG1_0_TXP … [9] PEG1_15_TXN
PCIE_TX16+ … PCIE_TX31-
[9] PEG1_0_RXP … [9] PEG1_15_RXN
PCIE_RX16+ … PCIE_RX31-
PCI-E 16X
Type 7
RowC & DowD
PN = 1654M0001
10G
10G_KR_TX3+ … 10G_KR_RX0-
LAN_TX_P3 [8] … LAN_RX_N0 [8]
From SoC Quad 0
10G_PHY_CAP_23
10G_PHY_CAP_01
10G_CAP23 [27]
10G_CAP01 [27]
10G_SFP_SCL3 … 10G_SFP_SDA0
R766 0 LAN_I2C_SCL_MDC_P3
R797 0 LAN_I2C_SDA_MDIO_P3
R765 0 LAN_I2C_SCL_MDC_P2
R796 0 LAN_I2C_SDA_MDIO_P2
R762 0 LAN_I2C_SCL_MDC_P1
R793 0 LAN_I2C_SDA_MDIO_P1
R761 0 LAN_I2C_SCL_MDC_P0
R792 0 LAN_I2C_SDA_MDIO_P0
10 G Sideband
10G_INT3 10G_INT2 10G_INT1 10G_INT0
10G_INT3 [8] 10G_INT2 [8] 10G_INT1 [8]
R10836 X/0 10G_INT0 [8]
R10837 0 ETH_GPIO7 [8]
From PHY_INT
10G_SDP3 … 10G_SDP0 [8]
10G_PHY_RST_23 R798 0 BUF_PLT_RST# [13,23,29]
10G_PHY_01_RST R791 0 ETH_GPIO6 [8]
R10838 X/0
To PHY_Reset
10G_LED_SDA R795 0 LAN_LED_DAT [27]
10G_LED_SCL R794 0 LAN_LED_CLK [27]
10G_PHY_MDC_SCL3 … 10G_PHY_MDIO_SDA0
R801 R768 R800 R767 R789 R760 0
LAN_I2C_SCL_MDC_P3 [8] … LAN_I2C_SDA_MDIO_P1 [8]
R788 X/0 LAN_I2C_SCL_MDC_P0 [8]
R759 X/0 LAN_I2C_SDA_MDIO_P0 [8]
R10833 0 ETH_MDC4 [8]
R10834 0 ETH_MDIO4 [8]
To PHY
PCI-E
PCIE_RX6+ PCIE_RX6- PCIE_TX6+ PCIE_TX6-
PCIE_6_RXP [10] PCIE_6_RXN [10] PCIE_6_TXP [10] PCIE_6_TXN [10]
PCIE_RX7+ PCIE_RX7- PCIE_TX7+ PCIE_TX7-
PCIE_7_RXP [10] PCIE_7_RXN [10] PCIE_7_TXP [10] PCIE_7_TXN [10]
TP-00 TP63 RAPID_SHUTDOWN
RAPID_SHUTDOWN
GND_47 … GND_56
RSVD_1 RSVD_2 RSVD_3 RSVD_7 RSVD_8
Super Speed USB
USB_SSTX0+ … USB_SSRX3-
USB3_0_TXP [10] … USB3_3_RXN [10]
GND_38 … GND_46
GND_37 … GND_0
A0.2 modify
[28] CLK_100M_GEN4_DP R10867 0ohm, 5% R0402
[28] CLK_100M_GEN4_DN R10868 0ohm, 5% R0402
[12] SMB_VPP_DATA
[12] SMB_VPP_CLK
[12] SMB_VPP_ALERT#
SMBus for PCIe Hotplug(PCH)
RSVD_10 RSVD_11 RSVD_12 RSVD_22 RSVD_23 RSVD_24 RSVD_25 RSVD_26
P1V05
+V3P3A
C273 0.1uF,
C270 0.1uF,
R411 348
R401 348
U27
PCA9617ADPJ
VCCA VCCB SCLA SCLB SDAA SDAB GND EN
[12] SMB_PEHPCPU_GTL_SCL
[12] SMB_PEHPCPU_GTL_SDA
SMBB_PEHPCPU_GTL_SCL_R
SMBB_PEHPCPU_GTL_SDA_R
R407 20 SMBB_PEHPCPU_GTL_SCL
R402 20 SMBB_PEHPCPU_GTL_SDA
R378 10K 1% R0402 +V3P3A
[12] PU_IRQ_CPU_MCSMBUS_ALRT_N
SMBus for PCIe Hotplug(CPU)

AAEON Technology INC.
AAEON An ASUS Company

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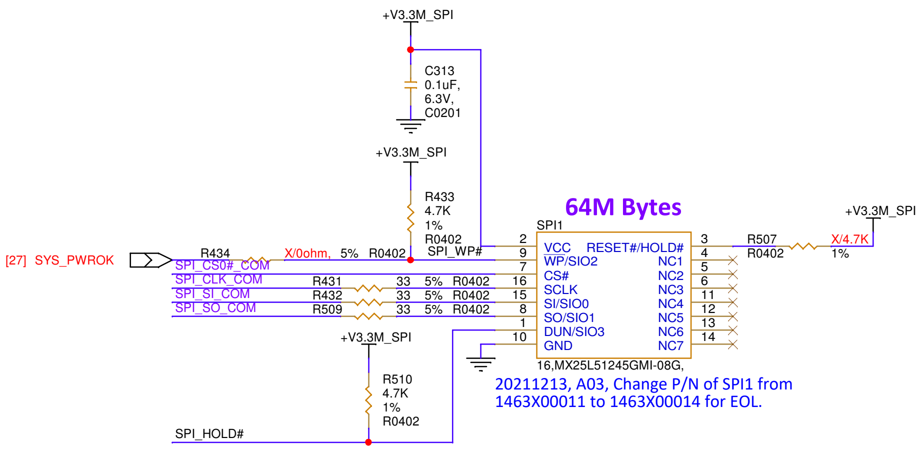
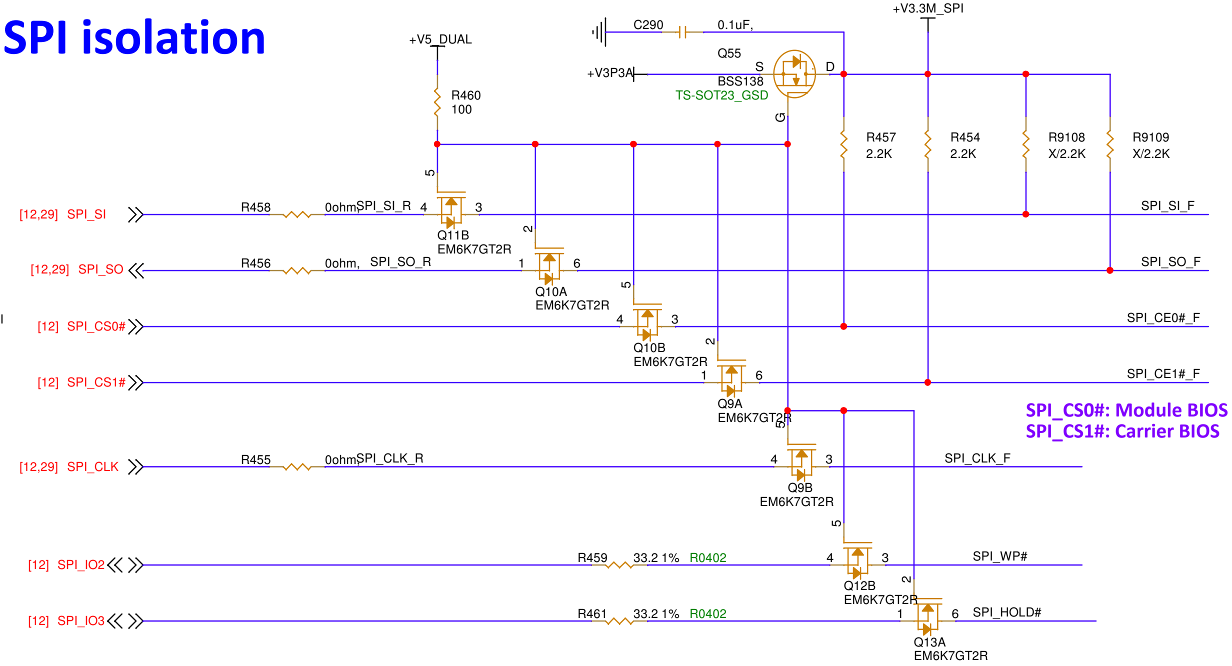
BIOS


+V3.3M_SPI
C313
0.1uF,
6.3V,
C0201
+V3.3M_SPI
R433
4.7K
1%
R0402
64M Bytes
SPI1
+V3.3M_SPI
[27] SYS_PWROK
R434
X/0ohm, 5% R0402
SPI_WP#
SPI_CS0#_COM
SPI_CLK_COM
SPI_SI_COM
SPI_SO_COM
R431 33 5% R0402
R432 33 5% R0402
R509 33 5% R0402
VCC
WP/SIO2
CS#
SCLK
SI/SIO0
SO/SIO1
DUN/SIO3
GND
RESET#/HOLD#
NC1
NC2
NC3
NC4
NC5
NC6
NC7
R507
R0402
X/4.7K
1%
+V3.3M_SPI
R510
4.7K
1%
R0402
SPI_HOLD#
16,MX25L51245GMI-08G,

20211213, A03, Change P/N of SPI1 from 1463X00011 to 1463X00014 for EOL.

SPI isolation


+V3.3M_SPI
C290 0.1uF,
+V5_DUAL
Q55
+V3P3A
BSS138
TS-SOT23_GSD
R460
100
R457 2.2K
R454 2.2K
R9108 X/2.2K
R9109 X/2.2K
[12,29] SPI_SI
R458 0ohm SPI_SI_R
Q11B EM6K7GT2R
SPI_SI_F
[12,29] SPI_SO
R456 0ohm, SPI_SO_R
Q10A EM6K7GT2R
SPI_SO_F
[12] SPI_CS0#
Q10B EM6K7GT2R
SPI_CE0#_F
[12] SPI_CS1#
Q9A EM6K7GT2R
SPI_CE1#_F
[12,29] SPI_CLK
R455 0ohm SPI_CLK_R
Q9B EM6K7GT2R
SPI_CLK_F
[12] SPI_IO2
R459 33.2 1% R0402
Q12B EM6K7GT2R
SPI_WP#
[12] SPI_IO3
R461 33.2 1% R0402
Q13A EM6K7GT2R
SPI_HOLD#

SPI_CS0#: Module BIOS
SPI_CS1#: Carrier BIOS

BIOS Switch

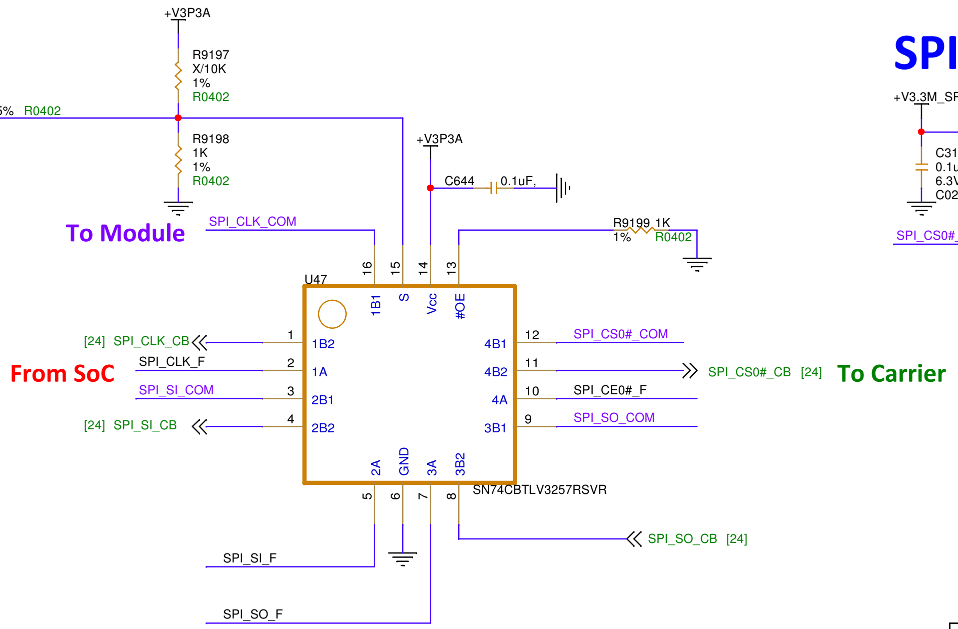
M7
material
(TF)BIOS Label.AMI.AMI-AptioTM DT(C)2006

BIOS selection

Mode	BIOS_SEL0#
Module	0(Default)
Carrier	1

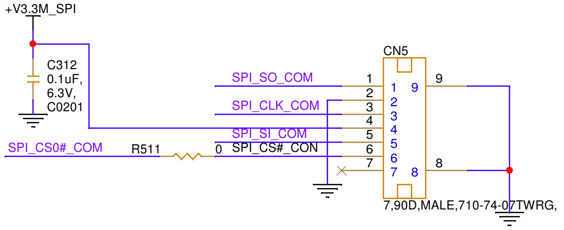
BIOS Source

Signal	BIOS_SEL0# = 0(A=B1)	BIOS_SEL0# = 1(A=B2)
SPI_CLK_F	SPI_CLK_COM	SPI_CLK_CB
SPI_SI_F	SPI_SI_COM	SPI_SI_CB
SPI_SO_F	SPI_SO_COM	SPI_SO_CB
SPI_CE0#_F	SPI_CS0#_COM	SPI_CS0#_CB


+V3P3A
R9197
X/10K
1%
R0402
[27] BIOS_SEL0#
R9205 0ohm, 5% R0402
R9198
1K
1%
R0402
+V3P3A
C644 0.1uF,
To Module
SPI_CLK_COM
R9199 1K
1% R0402
U47
1B1 S Vcc #OE
[24] SPI_CLK_CB
SPI_CLK_F
SPI_SI_COM
[24] SPI_SI_CB
From SoC
1B2
1A
2B1
2B2
4B1
4B2
4A
3B1
SPI_CS0#_COM
SPI_CS0#_CB [24]
To Carrier
SPI_CE0#_F
SPI_SO_COM
2A GND 3A 3B2
SN74CBTLV3257RSVR
SPI_SO_CB [24]
SPI_SI_F
SPI_SO_F

<table>
<tr><th colspan="2">INPUTS</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>OE̅</th><th>S</th></tr>
<tr><td>L</td><td>L</td><td>A port = B1 port</td></tr>
<tr><td>L</td><td>H</td><td>A port = B2 port</td></tr>
<tr><td>H</td><td>X</td><td>Disconnect</td></tr>
</table>

SPI ROM Flash Tool


+V3.3M_SPI
C312
0.1uF,
6.3V,
C0201
CN5
SPI_SO_COM
SPI_CLK_COM
SPI_SI_COM
SPI_CS0#_COM
R511 0
SPI_CS#_CON
7,90D,MALE,710-74-07TWRG,

A0.2 modify

AAEON Technology INC.
Title
BIOS
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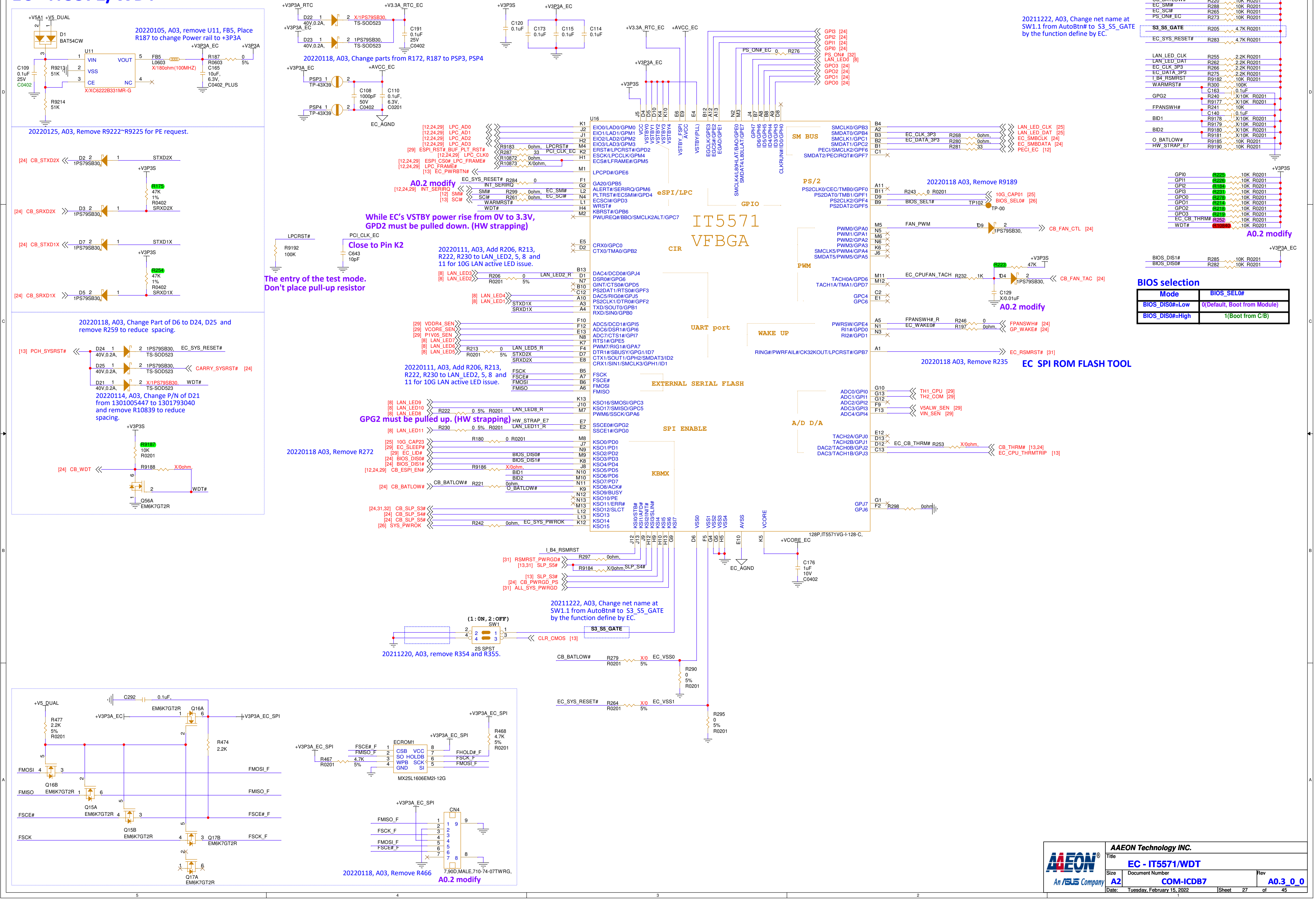
EC - IT5571/WDT



IT5571
VFBGA
U16
128P,IT5571VG-I-128-C,
eSPI/LPC
SM BUS
PS/2
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
U11
XC6222B331MR-G
D1
BAT54CW
SW1
2S SPST
(1:ON,2:OFF)
ECROM1
MX25L1606EM2I-12G
CN4
7,90D,MALE,710-74-07TWRG,
Q16A
Q16B
Q15A
Q15B
Q17A
Q17B
EM6K7GT2R
Q56A
+V3P3A_EC
+V3P3S
+V3P3A_RTC
+V3.3A_RTC_EC
+AVCC_EC
+V5_DUAL
+V3P3A_EC_SPI
+VCORE_EC
EC_AGND
S3_S5_GATE
CLR_CMOS [13]

20220114, A03, Remove D11, R9191, R274, Reserve D22, Add D23

20220105, A03, remove U11, FB5, Place R187 to change Power rail to +3P3A

20220118, A03, Change parts from R172, R187 to PSP3, PSP4

20220125, A03, Remove R9222~R9225 for PE request.

20211222, A03, Change net name at SW1.1 from AutoBtn# to S3_S5_GATE by the function define by EC.

A0.2 modify

While EC's VSTBY power rise from 0V to 3.3V, GPD2 must be pulled down. (HW strapping)

Close to Pin K2

The entry of the test mode. Don't place pull-up resistor

20220111, A03, Add R206, R213, R222, R230 to LAN_LED2, 5, 8 and 11 for 10G LAN active LED issue.

20220118 A03, Remove R9189

A0.2 modify

A0.2 modify

BIOS selection

Mode	BIOS_SEL0#
BIOS_DIS0#=Low	0(Default, Boot from Module)
BIOS_DIS0#=High	1(Boot from C/B)

20220118, A03, Change Part of D6 to D24, D25 and remove R259 to reduce spacing.

20220114, A03, Change P/N of D21 from 1301005447 to 1301793040 and remove R10839 to reduce spacing.

20220111, A03, Add R206, R213, R222, R230 to LAN_LED2, 5, 8 and 11 for 10G LAN active LED issue.

GPG2 must be pulled up. (HW strapping)

20220118 A03, Remove R272

20220118 A03, Remove R235

EC SPI ROM FLASH TOOL

20211222, A03, Change net name at SW1.1 from AutoBtn# to S3_S5_GATE by the function define by EC.

20211220, A03, remove R354 and R355.

20220118, A03, Remove R466

A0.2 modify

AAEON Technology INC.

Title: EC - IT5571/WDT

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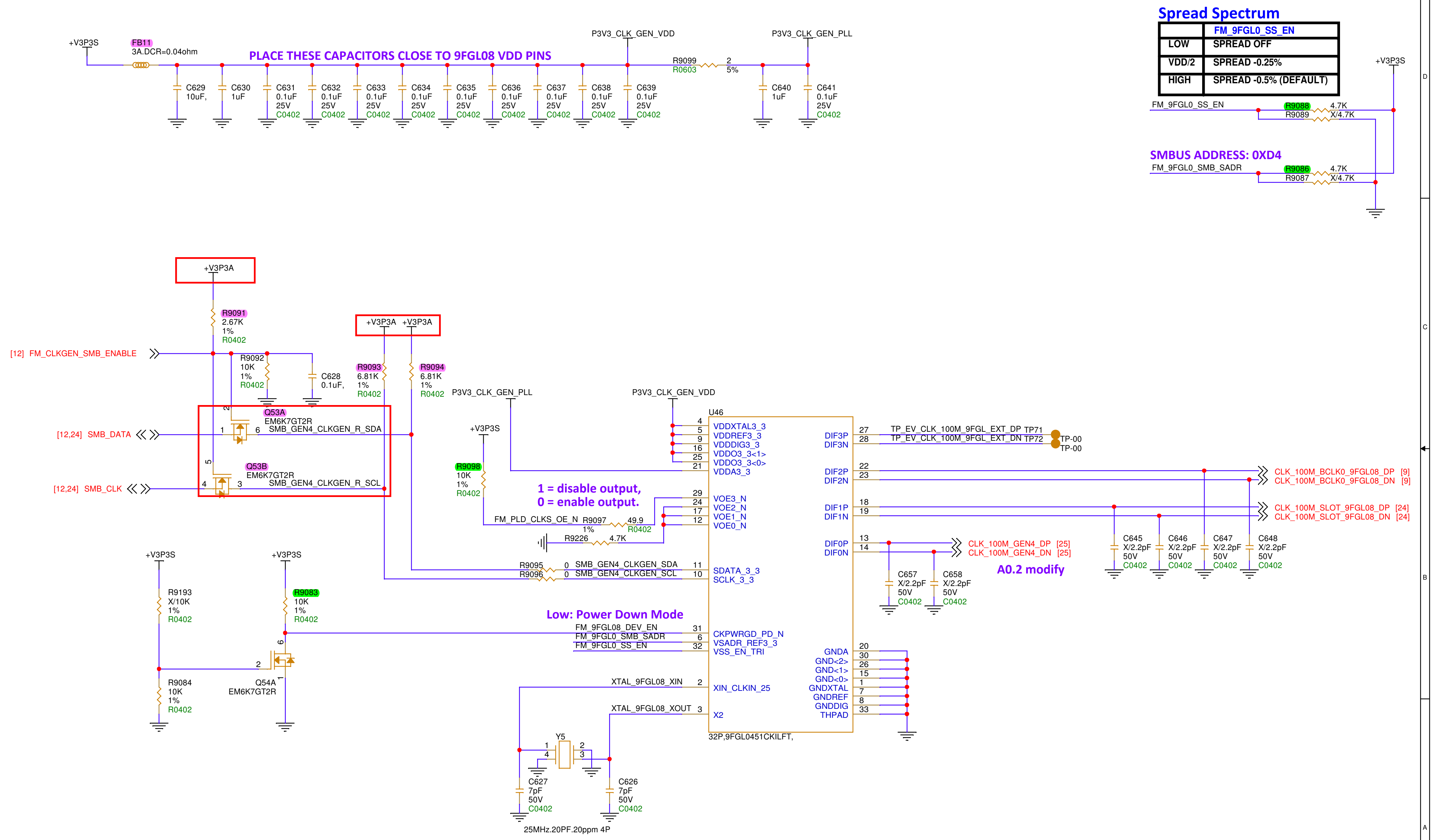
PCIE GEN4 Clock Generator


+V3P3S
FB11
3A.DCR=0.04ohm
PLACE THESE CAPACITORS CLOSE TO 9FGL08 VDD PINS
P3V3_CLK_GEN_VDD
P3V3_CLK_GEN_PLL
R9099
R0603
2
5%
C629 10uF,
C630 1uF
C631 0.1uF 25V C0402
C632 0.1uF 25V C0402
C633 0.1uF 25V C0402
C634 0.1uF 25V C0402
C635 0.1uF 25V C0402
C636 0.1uF 25V C0402
C637 0.1uF 25V C0402
C638 0.1uF 25V C0402
C639 0.1uF 25V C0402
C640 1uF
C641 0.1uF 25V C0402
+V3P3S
FM_9FGL0_SS_EN
R9088 4.7K
R9089 X/4.7K
SMBUS ADDRESS: 0XD4
FM_9FGL0_SMB_SADR
R9086 4.7K
R9087 X/4.7K
+V3P3A
R9091 2.67K 1% R0402
[12] FM_CLKGEN_SMB_ENABLE
R9092 10K 1% R0402
C628 0.1uF,
+V3P3A
+V3P3A
R9093 6.81K 1% R0402
R9094 6.81K 1% R0402
Q53A EM6K7GT2R
2
1
6
SMB_GEN4_CLKGEN_R_SDA
[12,24] SMB_DATA
Q53B EM6K7GT2R
5
4
3
SMB_GEN4_CLKGEN_R_SCL
[12,24] SMB_CLK
P3V3_CLK_GEN_PLL
P3V3_CLK_GEN_VDD
U46
4
5 VDDXTAL3_3
9 VDDREF3_3
16 VDDDIG3_3
25 VDDO3_3<1>
21 VDDO3_3<0>
VDDA3_3
+V3P3S
R9098 10K 1% R0402
1 = disable output,
0 = enable output.
29 VOE3_N
24 VOE2_N
17 VOE1_N
12 VOE0_N
FM_PLD_CLKS_OE_N
R9097 1% 49.9 R0402
R9226 4.7K
R9095 0 SMB_GEN4_CLKGEN_SDA 11 SDATA_3_3
R9096 0 SMB_GEN4_CLKGEN_SCL 10 SCLK_3_3
DIF3P 27 TP_EV_CLK_100M_9FGL_EXT_DP TP71
DIF3N 28 TP_EV_CLK_100M_9FGL_EXT_DN TP72
TP-00
TP-00
DIF2P 22 CLK_100M_BCLK0_9FGL08_DP [9]
DIF2N 23 CLK_100M_BCLK0_9FGL08_DN [9]
DIF1P 18 CLK_100M_SLOT_9FGL08_DP [24]
DIF1N 19 CLK_100M_SLOT_9FGL08_DN [24]
DIF0P 13 CLK_100M_GEN4_DP [25]
DIF0N 14 CLK_100M_GEN4_DN [25]
C645 X/2.2pF 50V C0402
C646 X/2.2pF 50V C0402
C647 X/2.2pF 50V C0402
C648 X/2.2pF 50V C0402
C657 X/2.2pF 50V C0402
C658 X/2.2pF 50V C0402
A0.2 modify
+V3P3S
R9193 X/10K 1% R0402
R9084 10K 1% R0402
+V3P3S
R9083 10K 1% R0402
6
2
1
Q54A EM6K7GT2R
Low: Power Down Mode
FM_9FGL08_DEV_EN 31 CKPWRGD_PD_N
FM_9FGL0_SMB_SADR 6 VSADR_REF3_3
FM_9FGL0_SS_EN 32 VSS_EN_TRI
XTAL_9FGL08_XIN 2 XIN_CLKIN_25
XTAL_9FGL08_XOUT 3 X2
GNDA 20
GND<2> 30
GND<1> 26
GND<0> 15
GNDXTAL 1
GNDREF 7
GNDDIG 8
THPAD 33
32P,9FGL0451CKILFT,
Y5
1
4
2
3
C627 7pF 50V C0402
C626 7pF 50V C0402
25MHz.20PF.20ppm 4P

Spread Spectrum

	FM_9FGL0_SS_EN
LOW	SPREAD OFF
VDD/2	SPREAD -0.25%
HIGH	SPREAD -0.5% (DEFAULT)

<Core Design>

AAEON Technology INC.

An ASUS Company

Title
PCIE GEN4 Clock Generator

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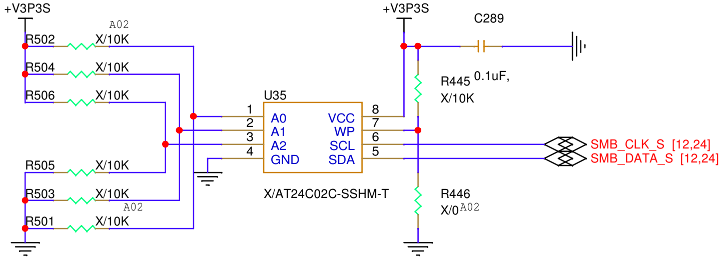
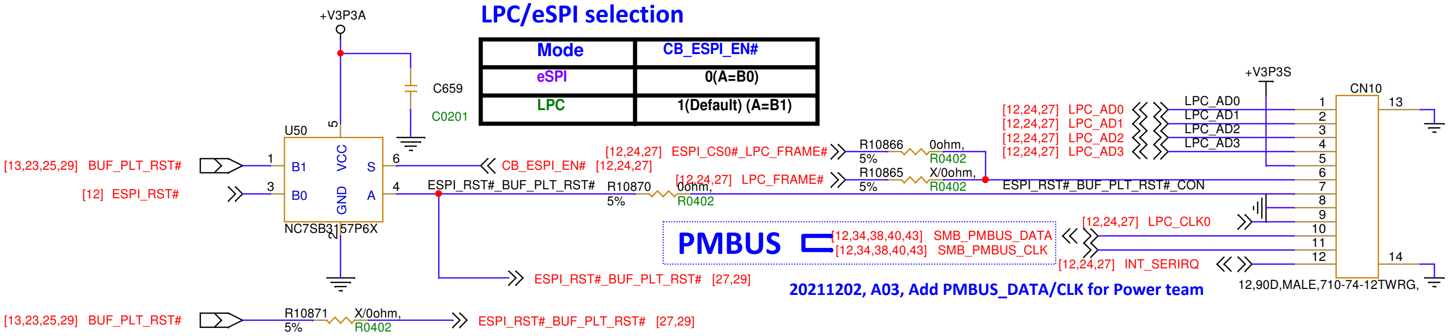
CMOS


+V3P3S
R502 X/10K A02
R504 X/10K
R506 X/10K
R505 X/10K
R503 X/10K A02
R501 X/10K
U35
A0 A1 A2 GND
VCC WP SCL SDA
X/AT24C02C-SSHM-T
+V3P3S
C289
0.1uF,
R445 X/10K
R446 X/0 A02
SMB_CLK_S [12,24]
SMB_DATA_S [12,24]

LPC/eSPI Connector


+V3P3A
C659
C0201
U50
B1 B0 VCC GND S A
NC7SB3157P6X
[13,23,25,29] BUF_PLT_RST#
[12] ESPI_RST#
CB_ESPI_EN# [12,24,27]
ESPI_RST#_BUF_PLT_RST#
R10870 0ohm, 5% R0402
ESPI_RST#_BUF_PLT_RST# [27,29]
[12,24,27] ESPI_CS0#_LPC_FRAME#
R10866 0ohm, 5% R0402
[12,24,27] LPC_FRAME#
R10865 X/0ohm, 5% R0402
ESPI_RST#_BUF_PLT_RST#_CON
[12,24,27] LPC_AD0
[12,24,27] LPC_AD1
[12,24,27] LPC_AD2
[12,24,27] LPC_AD3
+V3P3S
CN10
[12,24,27] LPC_CLK0
PMBUS
[12,34,38,40,43] SMB_PMBUS_DATA
[12,34,38,40,43] SMB_PMBUS_CLK
[12,24,27] INT_SERIRQ
12,90D,MALE,710-74-12TWRG,
[13,23,25,29] BUF_PLT_RST#
R10871 X/0ohm, 5% R0402
ESPI_RST#_BUF_PLT_RST# [27,29]

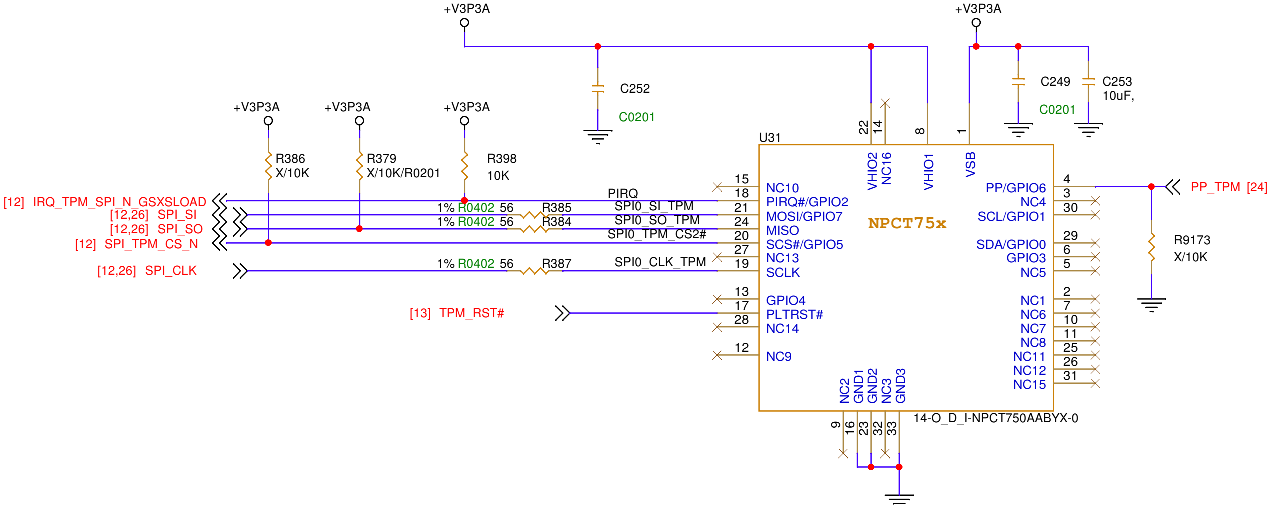
LPC/eSPI selection

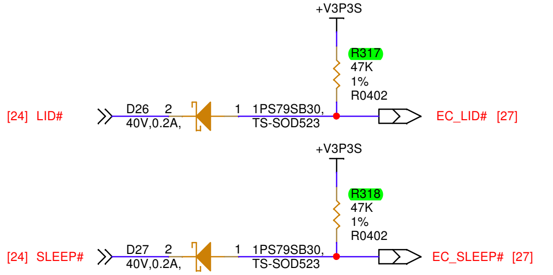
Mode	CB_ESPI_EN#
eSPI	0(A=B0)
LPC	1(Default) (A=B1)

20211202, A03, Add PMBUS_DATA/CLK for Power team

SM BUS ADDRESS 0XAC

TPM

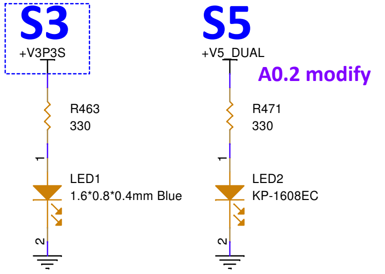

+V3P3A
C252
C0201
C249
C0201
C253 10uF,
R386 X/10K
R379 X/10K/R0201
R398 10K
U31
NPCT75x
[12] IRQ_TPM_SPI_N_GSXSLOAD
[12,26] SPI_SI
[12,26] SPI_SO
[12] SPI_TPM_CS_N
[12,26] SPI_CLK
PIRQ
1% R0402 56 R385 SPI0_SI_TPM
1% R0402 56 R384 SPI0_SO_TPM
SPI0_TPM_CS2#
1% R0402 56 R387 SPI0_CLK_TPM
[13] TPM_RST#
NC10 PIRQ#/GPIO2 MOSI/GPIO7 MISO SCS#/GPIO5 NC13 SCLK GPIO4 PLTRST# NC14 NC9
VHIO2 NC16 VHIO1 VSB
PP/GPIO6 NC4 SCL/GPIO1 SDA/GPIO0 GPIO3 NC5 NC1 NC6 NC7 NC8 NC11 NC12 NC15
NC2 GND1 GND2 NC3 GND3
14-O_D_I-NPCT750AABYX-0
PP_TPM [24]
R9173 X/10K


+V3P3S
R317 47K 1% R0402
[24] LID#
D26 40V,0.2A,
1PS79SB30, TS-SOD523
EC_LID# [27]
+V3P3S
R318 47K 1% R0402
[24] SLEEP#
D27 40V,0.2A,
1PS79SB30, TS-SOD523
EC_SLEEP# [27]

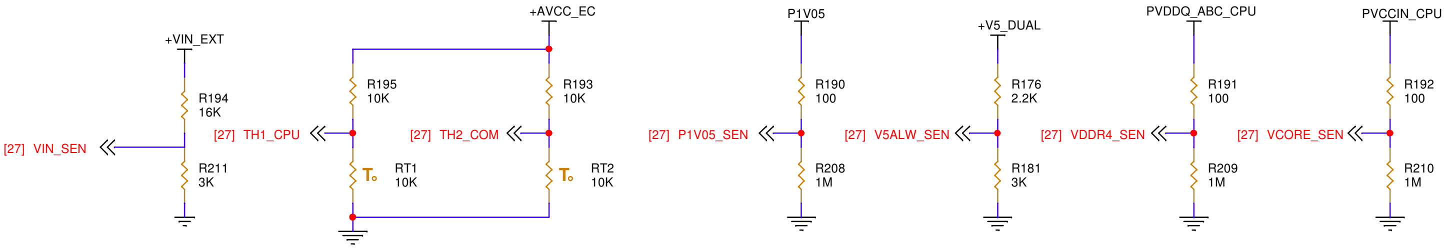
20220118, A03, Change Part of D13, D12 to D26, D27 to reduce spacing.

Power LED

20211210, A03, Change power at R463 from +V5S to +V3P3S.


S3
+V3P3S
R463 330
LED1 1.6*0.8*0.4mm Blue
S5
+V5_DUAL
A0.2 modify
R471 330
LED2 KP-1608EC

H/W Monitor


+VIN_EXT
R194 16K
[27] VIN_SEN
R211 3K
+AVCC_EC
R195 10K
R193 10K
[27] TH1_CPU
[27] TH2_COM
RT1 10K
RT2 10K
P1V05
R190 100
[27] P1V05_SEN
R208 1M
+V5_DUAL
R176 2.2K
[27] V5ALW_SEN
R181 3K
PVDDQ_ABC_CPU
R191 100
[27] VDDR4_SEN
R209 1M
PVCCIN_CPU
R192 100
[27] VCORE_SEN
R210 1M

<Core Design>

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Title	TPM/LPC/H/W Monitor	
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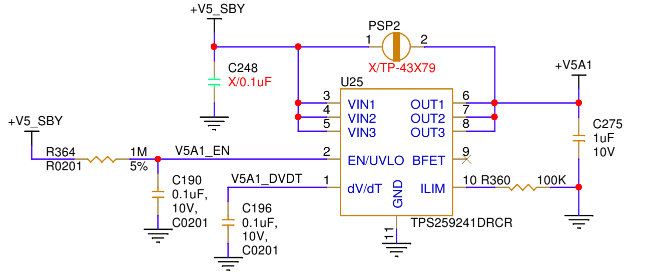
+V5_SBY


+V5_SBY
PSP2
1
2
X/TP-43X79
C248
X/0.1uF
U25
3
4
5
VIN1
VIN2
VIN3
OUT1
OUT2
OUT3
6
7
8
+V5A1
C275
1uF
10V
+V5_SBY
R364
R0201
1M
5%
V5A1_EN
2
EN/UVLO
BFET
9
C190
0.1uF,
10V,
C0201
V5A1_DVDT
1
dV/dT
GND
ILIM
10 R360
100K
C196
0.1uF,
10V,
C0201
11
TPS259241DRCR

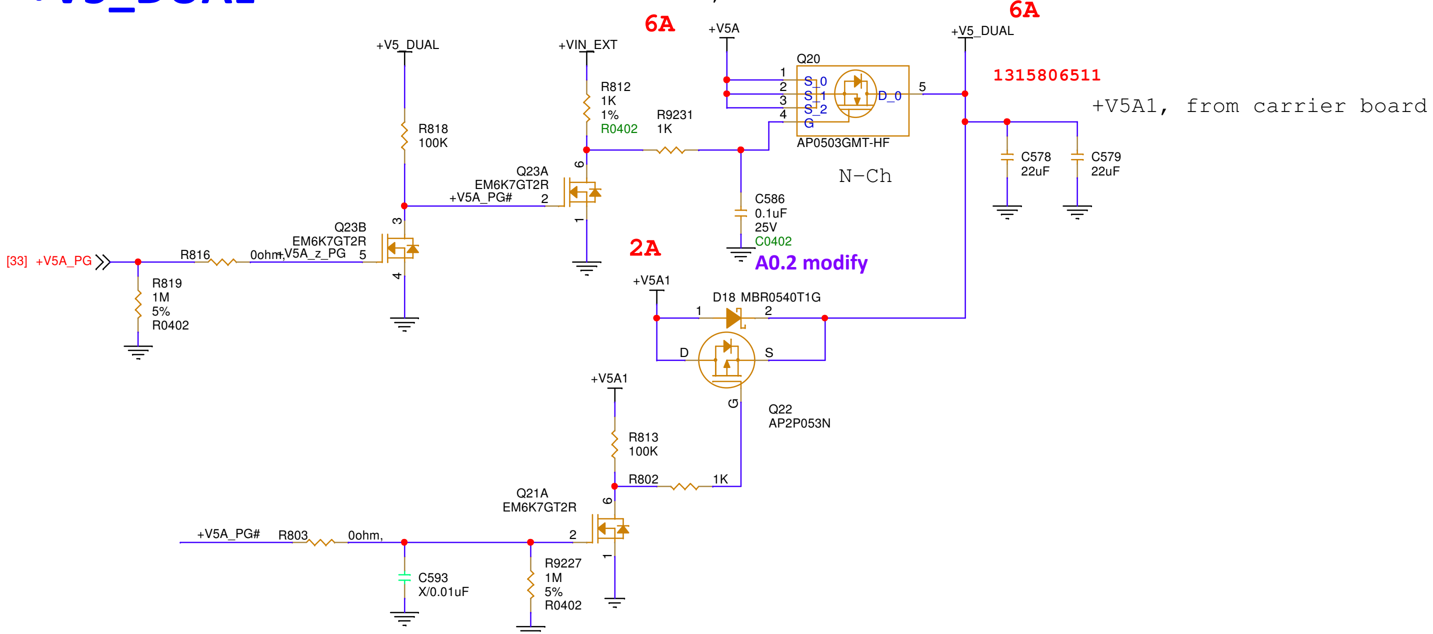
20211222, A03,
1. Add C190 and C196 to soft starting +V5A1 for +V5_SBY ramp up issue.
2. Change FB6 to PSP2 to reduce spacing for layout.

Default: Undervoltage lockout set point = 4.3 V

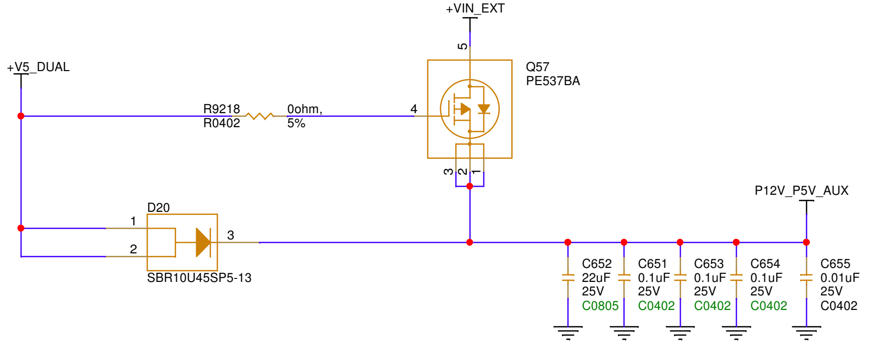
+V5_DUAL

+V5A switch circuit

+V5A1, from carrier board
+V5A, from COM Module


+V5_DUAL
+VIN_EXT
6A
+V5A
6A
+V5_DUAL
Q20
1
2
3
4
S_0
S_1
S_2
G
D_0
5
AP0503GMT-HF
N-Ch
1315806511
+V5A1, from carrier board
R812
1K
1%
R0402
R9231
1K
R818
100K
C578
22uF
C579
22uF
Q23A
EM6K7GT2R
+V5A_PG#
2
6
1
C586
0.1uF
25V
C0402
A0.2 modify
2A
Q23B
EM6K7GT2R
3
4
5
[33] +V5A_PG
R816
0ohm
+V5A_z_PG
R819
1M
5%
R0402
+V5A1
D18 MBR0540T1G
1
2
D
S
G
Q22
AP2P053N
+V5A1
R813
100K
R802
1K
Q21A
EM6K7GT2R
6
2
1
+V5A_PG#
R803
0ohm,
C593
X/0.01uF
R9227
1M
5%
R0402

P12V_P5V_AUX


+VIN_EXT
5
Q57
PE537BA
+V5_DUAL
R9218
R0402
0ohm,
5%
4
3
2
1
P12V_P5V_AUX
D20
1
2
3
SBR10U45SP5-13
C652
22uF
25V
C0805
C651
0.1uF
25V
C0402
C653
0.1uF
25V
C0402
C654
0.1uF
25V
C0402
C655
0.01uF
25V
C0402

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AAEON Technology INC.			
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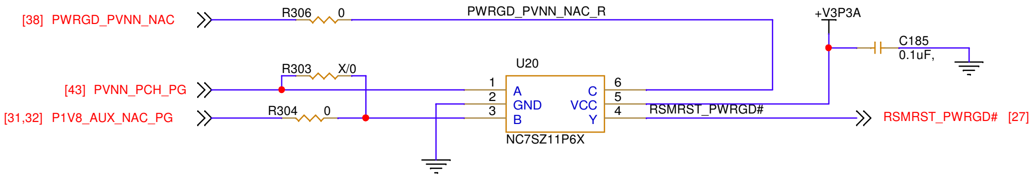
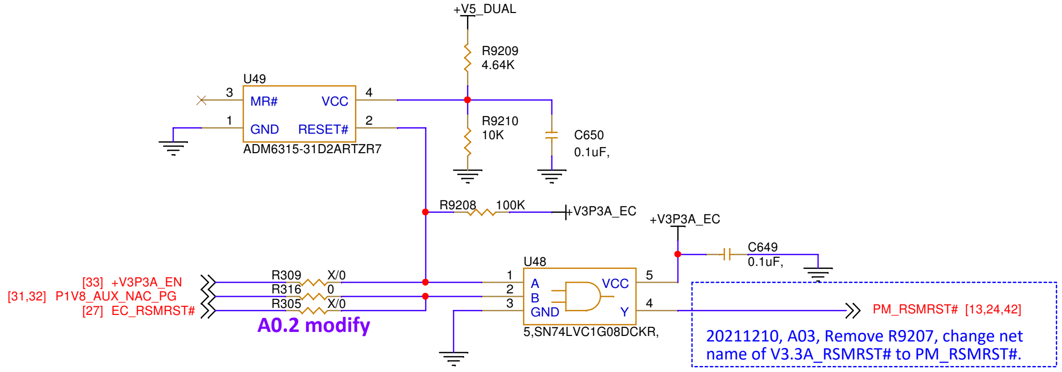
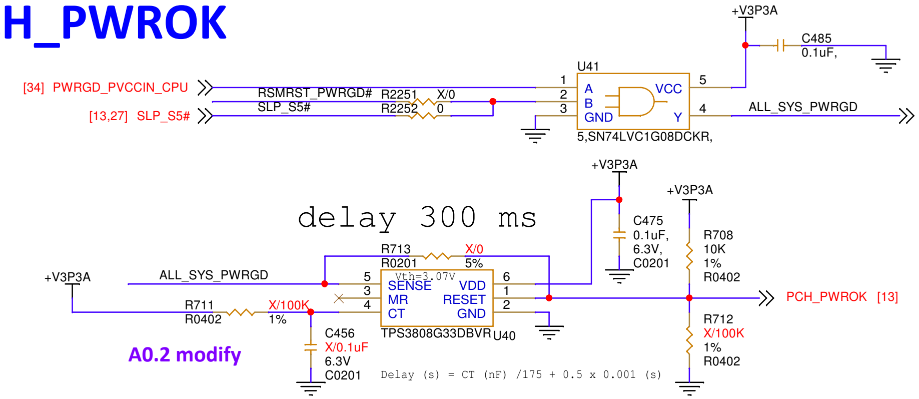
Boot Sequence

RSMRST#


[38] PWRGD_PVNN_NAC
R306 0
PWRGD_PVNN_NAC_R
+V3P3A
C185
0.1uF,
R303 X/0
[43] PVNN_PCH_PG
[31,32] P1V8_AUX_NAC_PG
R304 0
U20
1 A
2 GND
3 B
C 6
VCC 5
Y 4
NC7SZ11P6X
RSMRST_PWRGD#
RSMRST_PWRGD# [27]

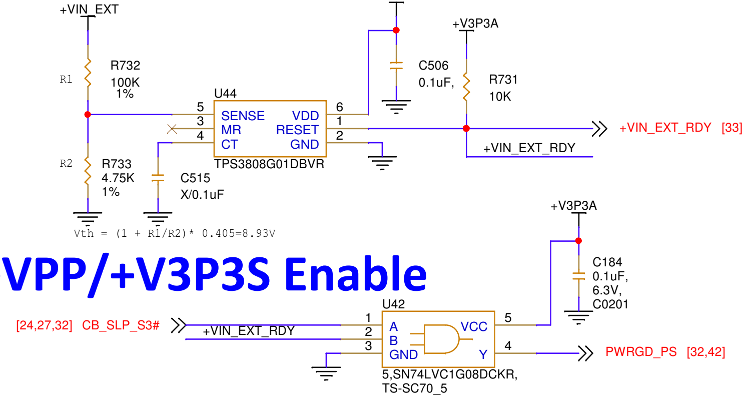

+V5_DUAL
R9209
4.64K
U49
3 MR#
1 GND
VCC 4
RESET# 2
ADM6315-31D2ARTZR7
R9210
10K
C650
0.1uF,
R9208 100K
+V3P3A_EC
+V3P3A_EC
C649
0.1uF,
U48
[33] +V3P3A_EN
[31,32] P1V8_AUX_NAC_PG
[27] EC_RSMRST#
R309 X/0
R316 0
R305 X/0
1 A
2 B
3 GND
VCC 5
Y 4
5,SN74LVC1G08DCKR,
A0.2 modify
PM_RSMRST# [13,24,42]
20211210, A03, Remove R9207, change net name of V3.3A_RSMRST# to PM_RSMRST#.

PCH_PWROK


+V3P3A
C485
0.1uF,
U41
[34] PWRGD_PVCCIN_CPU
[13,27] SLP_S5#
RSMRST_PWRGD#
SLP_S5#
R2251 X/0
R2252 0
1 A
2 B
3 GND
VCC 5
Y 4
5,SN74LVC1G08DCKR,
ALL_SYS_PWRGD
ALL_SYS_PWRGD [27]
+V3P3A
delay 300 ms
+V3P3A
C475
0.1uF,
6.3V,
C0201
R708
10K
1%
R0402
+V3P3A
ALL_SYS_PWRGD
R713 X/0
R0201 5%
Vth=3.07V
5 SENSE
3 MR
4 CT
VDD 6
RESET 1
GND 2
TPS3808G33DBVR
U40
R711 X/100K
R0402 1%
C456
X/0.1uF
6.3V
C0201
PCH_PWROK [13]
R712
X/100K
1%
R0402
A0.2 modify
Delay (s) = CT (nF) /175 + 0.5 x 0.001 (s)

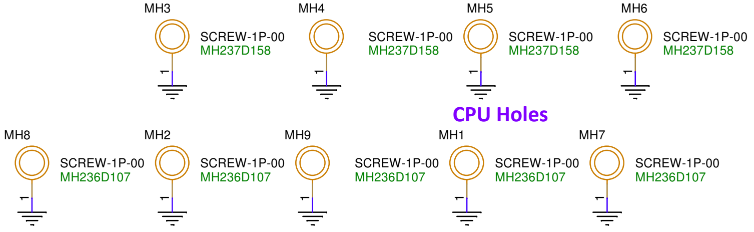
+V5A Enable

+VPP/+V3P3S Enable


+VIN_EXT
R732
100K
1%
R1
+V3P3A
C506
0.1uF,
+V3P3A
R731
10K
U44
5 SENSE
3 MR
4 CT
VDD 6
RESET 1
GND 2
TPS3808G01DBVR
+VIN_EXT_RDY [33]
+VIN_EXT_RDY
R2
R733
4.75K
1%
C515
X/0.1uF
Vth = (1 + R1/R2)* 0.405=8.93V
+V3P3A
C184
0.1uF,
6.3V,
C0201
U42
[24,27,32] CB_SLP_S3#
+VIN_EXT_RDY
1 A
2 B
3 GND
VCC 5
Y 4
5,SN74LVC1G08DCKR,
TS-SC70_5
PWRGD_PS [32,42]

20211210, A03, Change AND GATE from 3 input to 2 input for remove net of CB_PWRGD_PS.

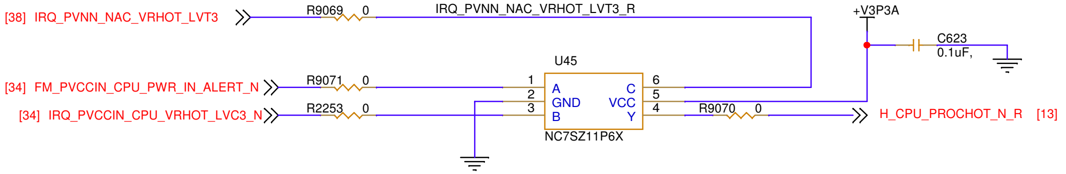
COM Mounting Holes


MH3
SCREW-1P-00
MH237D158
MH4
SCREW-1P-00
MH237D158
MH5
SCREW-1P-00
MH237D158
MH6
SCREW-1P-00
MH237D158
MH8
SCREW-1P-00
MH236D107
MH2
SCREW-1P-00
MH236D107
MH9
SCREW-1P-00
MH236D107
MH1
SCREW-1P-00
MH236D107
MH7
SCREW-1P-00
MH236D107

CPU Holes

COM Express Holes

CPU_PROCHOT


[38] IRQ_PVNN_NAC_VRHOT_LVT3
R9069 0
IRQ_PVNN_NAC_VRHOT_LVT3_R
+V3P3A
C623
0.1uF,
U45
[34] FM_PVCCIN_CPU_PWR_IN_ALERT_N
R9071 0
[34] IRQ_PVCCIN_CPU_VRHOT_LVC3_N
R2253 0
1 A
2 GND
3 B
C 6
VCC 5
Y 4
NC7SZ11P6X
R9070 0
H_CPU_PROCHOT_N_R [13]

PCB1

PCB.COM-ICDB7.Rev.A0.3_0_0.HDI.(2+10+2).14Layers.Green.1*1.125x95x2.0mm
1907ICD702

AAEON Technology INC.

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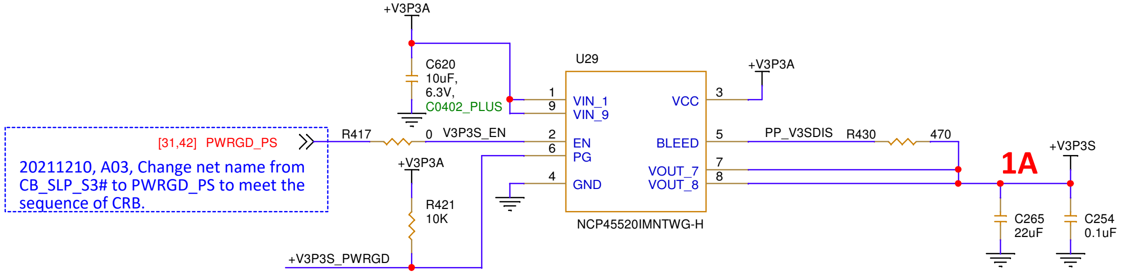
System Power

+V3P3S

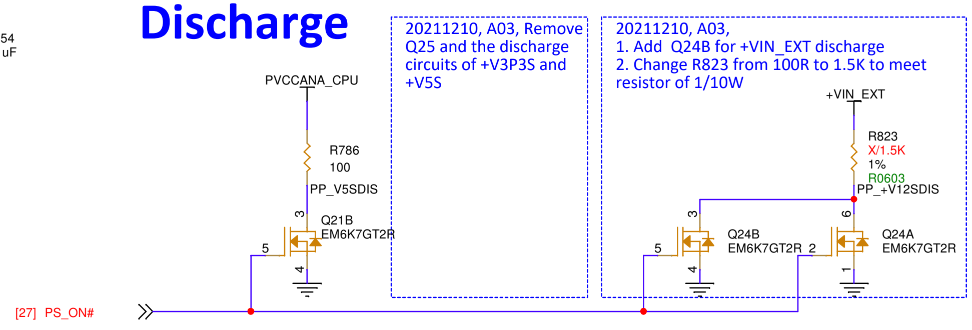

+V3P3A
C620
10uF,
6.3V,
C0402_PLUS
U29
+V3P3A
1
9
VIN_1
VIN_9
VCC
3
[31,42] PWRGD_PS
R417
0
V3P3S_EN
2
6
EN
PG
BLEED
5
PP_V3SDIS
R430
470
+V3P3A
7
8
VOUT_7
VOUT_8
1A
+V3P3S
R421
10K
4
GND
C265
22uF
C254
0.1uF
NCP45520IMNTWG-H
+V3P3S_PWRGD

20211210, A03, Change net name from CB_SLP_S3# to PWRGD_PS to meet the sequence of CRB.

+V5S

20211210, A03, Remove U26 and Power +V5S

Discharge

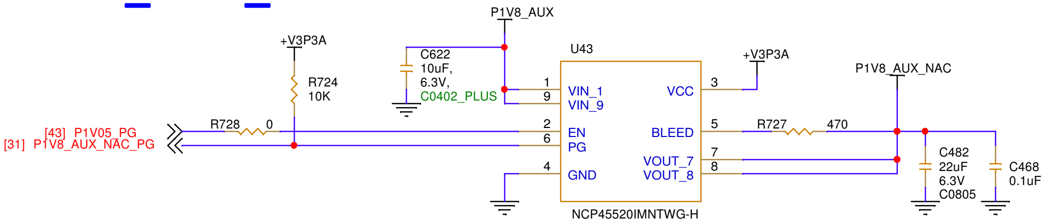

PVCCANA_CPU
R786
100
PP_V5SDIS
3
Q21B
EM6K7GT2R
5
4
+VIN_EXT
R823
X/1.5K
1%
R0603
PP_+V12SDIS
3
6
Q24B
EM6K7GT2R
Q24A
EM6K7GT2R
5
2
4
1
[27] PS_ON#

20211210, A03, Remove Q25 and the discharge circuits of +V3P3S and +V5S

20211210, A03,
1. Add Q24B for +VIN_EXT discharge
2. Change R823 from 100R to 1.5K to meet resistor of 1/10W

20220118 A03, Remove R825

P1V8_AUX_NAC


P1V8_AUX
+V3P3A
C622
10uF,
6.3V,
C0402_PLUS
U43
+V3P3A
R724
10K
1
9
VIN_1
VIN_9
VCC
3
P1V8_AUX_NAC
[43] P1V05_PG
[31] P1V8_AUX_NAC_PG
R728
0
2
6
EN
PG
BLEED
5
R727
470
7
8
VOUT_7
VOUT_8
C482
22uF
6.3V
C0805
C468
0.1uF
4
GND
NCP45520IMNTWG-H

P1V8_NACDELAY is P1V8_AUX gated to SoC via FET or similar after P1V05_NAC is stable

AAEON Technology INC.

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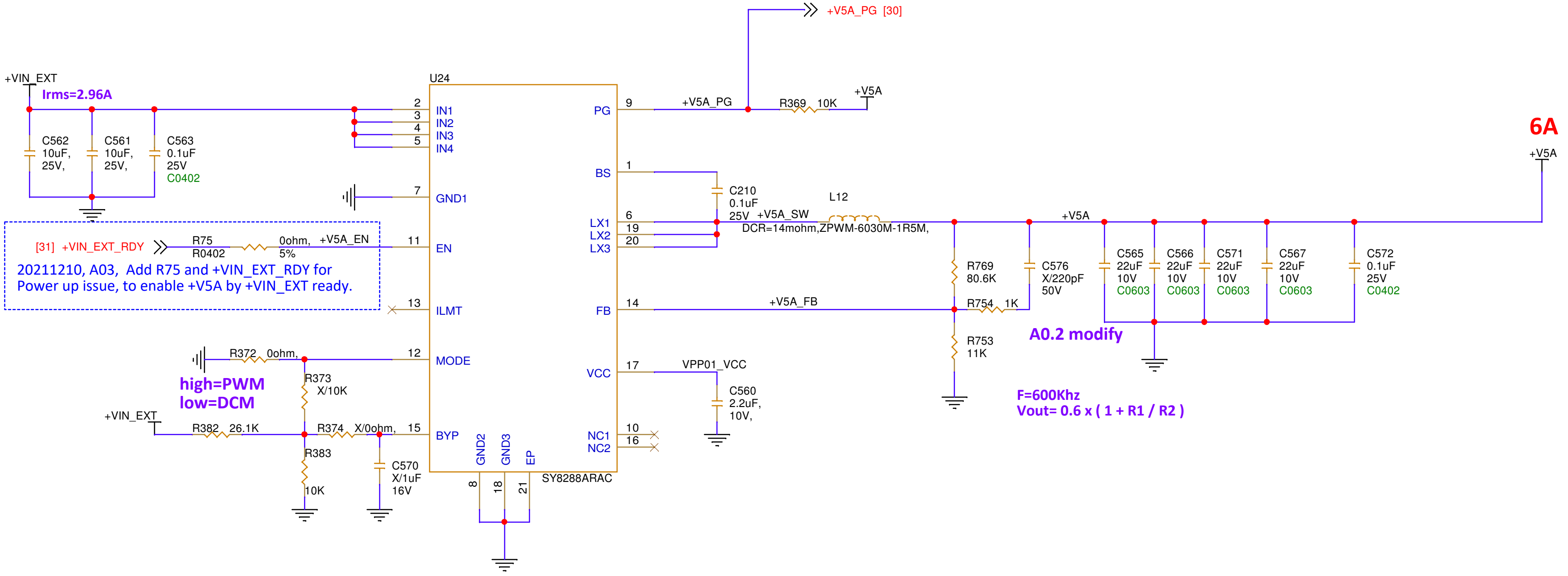
PWR +V5A


+V5A_PG [30]
+VIN_EXT
U24
C562 10uF, 25V,
C561 10uF, 25V,
C563 0.1uF 25V C0402
2 3 4 5
IN1 IN2 IN3 IN4
7 GND1
PG 9 +V5A_PG
R369 10K
+V5A
BS 1
C210 0.1uF 25V
LX1 LX2 LX3 6 19 20
+V5A_SW
L12
DCR=14mohm,ZPWM-6030M-1R5M,
+V5A
+V5A
C565 22uF 10V C0603
C566 22uF 10V C0603
C571 22uF 10V C0603
C567 22uF 10V C0603
C572 0.1uF 25V C0402
R769 80.6K
C576 X/220pF 50V
[31] +VIN_EXT_RDY
R75 R0402 0ohm, 5%
+V5A_EN
11 EN
13 ILMT
FB 14 +V5A_FB
R754 1K
R753 11K
R372 0ohm,
12 MODE
R373 X/10K
VCC 17 VPP01_VCC
C560 2.2uF, 10V,
+VIN_EXT
R382 26.1K
R374 X/0ohm,
15 BYP
R383 10K
C570 X/1uF 16V
GND2 GND3 EP
8 18 21
NC1 NC2 10 16
SY8288ARAC

Irms=2.96A

6A

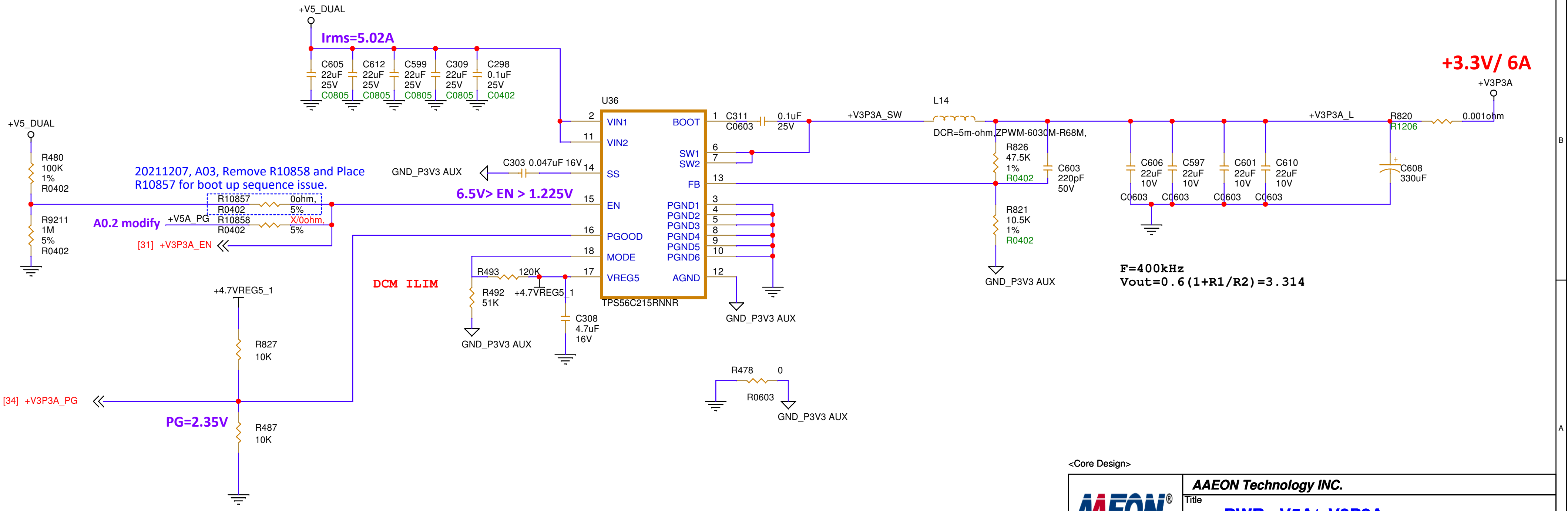
20211210, A03, Add R75 and +VIN_EXT_RDY for Power up issue, to enable +V5A by +VIN_EXT ready.

high=PWM
low=DCM

A0.2 modify

F=600Khz
Vout= 0.6 x (1 + R1 / R2)

PWR +V3P3A


+V5_DUAL
C605 22uF 25V C0805
C612 22uF 25V C0805
C599 22uF 25V C0805
C309 22uF 25V C0805
C298 0.1uF 25V C0402
U36
2 VIN1
11 VIN2
BOOT 1
C311 C0603
0.1uF 25V
+V3P3A_SW
L14
DCR=5m-ohm,ZPWM-6030M-R68M,
+V3P3A_L
R820 R1206
0.001ohm
+V3P3A
SW1 SW2 6 7
FB 13
R826 47.5K 1% R0402
C603 220pF 50V
C606 22uF 10V C0603
C597 22uF 10V C0603
C601 22uF 10V C0603
C610 22uF 10V C0603
C608 330uF
R821 10.5K 1% R0402
GND_P3V3 AUX
+V5_DUAL
R480 100K 1% R0402
R9211 1M 5% R0402
R10857 R0402 0ohm, 5%
+V5A_PG
R10858 R0402 X/0ohm, 5%
[31] +V3P3A_EN
GND_P3V3 AUX
C303 0.047uF 16V
14 SS
15 EN
16 PGOOD
18 MODE
17 VREG5
PGND1 PGND2 PGND3 PGND4 PGND5 PGND6
3 4 5 8 9 10
AGND 12
TPS56C215RNNR
R493 120K
R492 51K
+4.7VREG5_1
C308 4.7uF 16V
GND_P3V3 AUX
GND_P3V3 AUX
+4.7VREG5_1
R827 10K
[34] +V3P3A_PG
R487 10K
R478 0
R0603
GND_P3V3 AUX

Irms=5.02A

+3.3V/ 6A

20211207, A03, Remove R10858 and Place R10857 for boot up sequence issue.

6.5V> EN > 1.225V

A0.2 modify

DCM ILIM

PG=2.35V

F=400kHz
Vout=0.6(1+R1/R2)=3.314

<Core Design>

AAEON Technology INC.

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Title		
PWR +V5A/+V3P3A		
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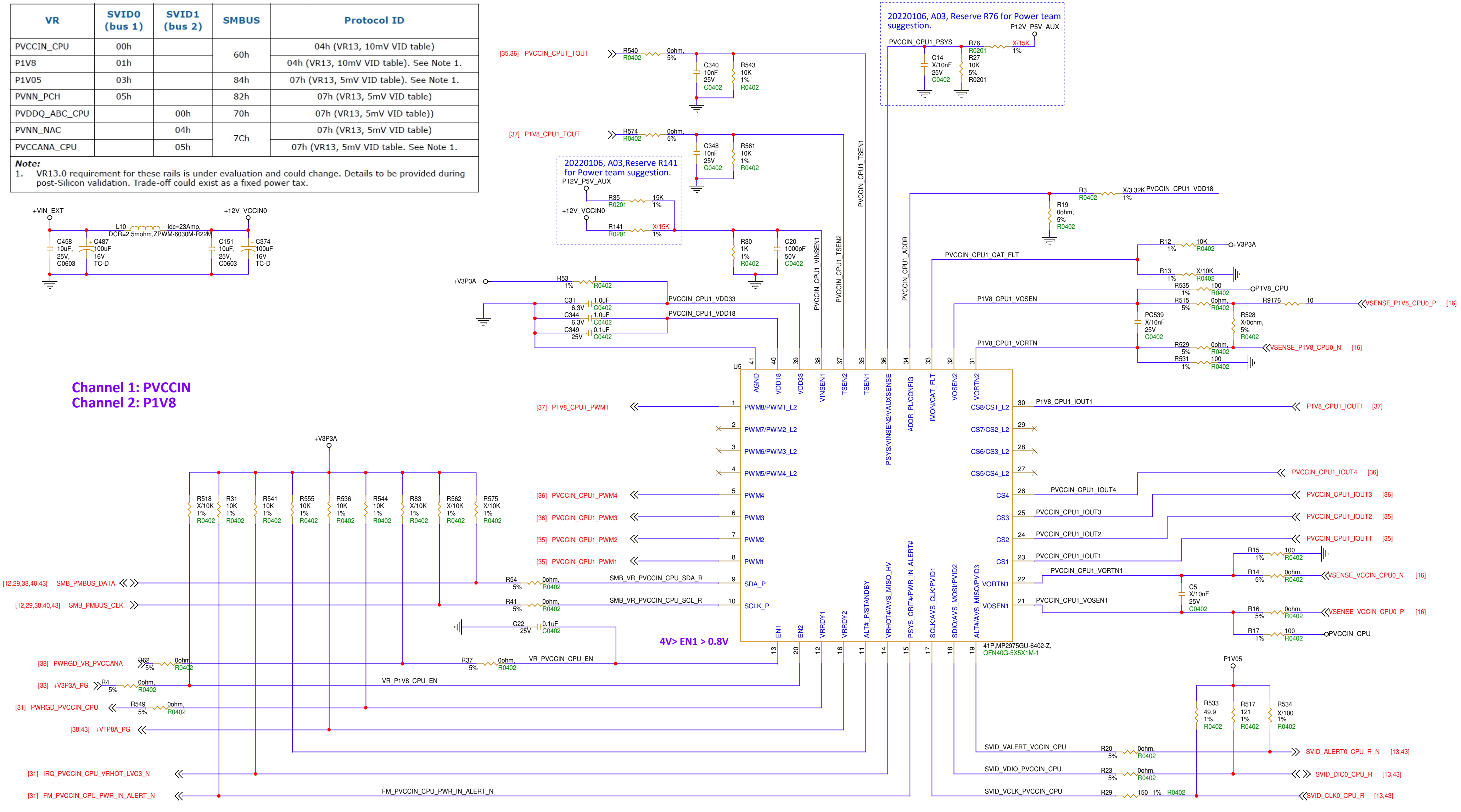
PWR PVCCIN_CPU/P1V8_1

VR13.0 SVID0, SVID1 and SMBUS Addresses - Brighton City RP

VR	SVID0 (bus 1)	SVID1 (bus 2)	SMBUS	Protocol ID
PVCCIN_CPU	00h		60h	04h (VR13, 10mV VID table)
P1V8	01h			04h (VR13, 10mV VID table). See Note 1.
P1V05	03h		84h	07h (VR13, 5mV VID table). See Note 1.
PVNN_PCH	05h		82h	07h (VR13, 5mV VID table)
PVDDQ_ABC_CPU		00h	70h	07h (VR13, 5mV VID table))
PVNN_NAC		04h	7Ch	07h (VR13, 5mV VID table)
PVCCANA_CPU		05h		07h (VR13, 5mV VID table. See Note 1.

Note:
1. VR13.0 requirement for these rails is under evaluation and could change. Details to be provided during post-Silicon validation. Trade-off could exist as a fixed power task.


20220106, A03, Reserve R76 for Power team suggestion.
20220106, A03,Reserve R141 for Power team suggestion.
Channel 1: PVCCIN
Channel 2: P1V8
4V> EN1 > 0.8V
U5
41P,MP2975GU-6402-Z, QFN40G-5X5X1M-1
+VIN_EXT
+12V_VCCIN0
+V3P3A
P12V_P5V_AUX
P1V05
L10 Idc=23Amp, DCR=2.5mohm,ZPWM-6030M-R22M
C458 10uF, 25V, C0603
C487 100uF 16V TC-D
C151 10uF, 25V, C0603
C374 100uF 16V TC-D
[35,36] PVCCIN_CPU1_TOUT
[37] P1V8_CPU1_TOUT
R540 0ohm, 5% R0402
C340 10nF 25V C0402
R543 10K 1% R0402
R574 0ohm, 5% R0402
C348 10nF 25V C0402
R561 10K 1% R0402
PVCCIN_CPU1_PSYS
C14 X/10nF 25V C0402
R76 X/15K 1% R0201
R27 10K 5% R0201
R35 15K 1% R0201
R141 X/15K 1% R0201
R30 1K 1% R0402
C20 1000pF 50V C0402
R3 X/3.32K 1% R0402 PVCCIN_CPU1_VDD18
R19 0ohm, 5% R0402
R53 1 1% R0402
C31 1.0uF 6.3V C0402
C344 1.0uF 6.3V C0402
C349 0.1uF 25V C0402
PVCCIN_CPU1_VDD33
PVCCIN_CPU1_VDD18
PVCCIN_CPU1_VINSEN1
PVCCIN_CPU1_TSEN2
PVCCIN_CPU1_TSEN1
PVCCIN_CPU1_ADDR
PVCCIN_CPU1_CAT_FLT
R12 10K 1% R0402 +V3P3A
R13 X/10K 1% R0402
R535 100 1% R0402 P1V8_CPU
R515 0ohm, 5% R0402
R9176 10 VSENSE_P1V8_CPU0_P [16]
P1V8_CPU1_VOSEN
PC539 X/10nF 25V C0402
R528 X/0ohm, 5% R0402
P1V8_CPU1_VORTN
R529 0ohm, 5% R0402 VSENSE_P1V8_CPU0_N [16]
R531 100 1% R0402
AGND VDD18 VDD33 VINSEN1 TSEN2 TSEN1 PSYS/VINSEN2/VAUXSENSE ADDR_PL/CONFIG IMON/CAT_FLT VOSEN2 VORTN2
[37] P1V8_CPU1_PWM1 — PWM8/PWM1_L2
PWM7/PWM2_L2
PWM6/PWM3_L2
PWM5/PWM4_L2
[36] PVCCIN_CPU1_PWM4 — PWM4
[36] PVCCIN_CPU1_PWM3 — PWM3
[35] PVCCIN_CPU1_PWM2 — PWM2
[35] PVCCIN_CPU1_PWM1 — PWM1
SDA_P
SCLK_P
CS8/CS1_L2 — P1V8_CPU1_IOUT1 — P1V8_CPU1_IOUT1 [37]
CS7/CS2_L2
CS6/CS3_L2
CS5/CS4_L2
CS4 — PVCCIN_CPU1_IOUT4 [36]
CS3 — PVCCIN_CPU1_IOUT3 [36]
CS2 — PVCCIN_CPU1_IOUT2 [35]
CS1 — PVCCIN_CPU1_IOUT1 [35]
VORTN1 — PVCCIN_CPU1_VORTN1
VOSEN1 — PVCCIN_CPU1_VOSEN1
R15 100 1% R0402
R14 0ohm, 5% R0402 VSENSE_VCCIN_CPU0_N [16]
C5 X/10nF 25V C0402
R16 0ohm, 5% R0402 VSENSE_VCCIN_CPU0_P [16]
R17 100 1% R0402 PVCCIN_CPU
EN1 EN2 VRRDY1 VRRDY2 ALT#_P/STANDBY VRHOT#/AVS_MISO_HV PSYS_CRIT#/PWR_IN_ALERT# SCLK/AVS_CLK/PVID1 SDIO/AVS_MOSI/PVID2 ALT#/AVS_MISO/PVID3
R518 X/10K 1% R0402
R31 10K 1% R0402
R541 10K 1% R0402
R555 10K 1% R0402
R536 10K 1% R0402
R544 10K 1% R0402
R83 X/10K 1% R0402
R562 X/10K 1% R0402
R575 X/10K 1% R0402
[12,29,38,40,43] SMB_PMBUS_DATA
[12,29,38,40,43] SMB_PMBUS_CLK
R54 0ohm, 5% R0402 SMB_VR_PVCCIN_CPU_SDA_R
R41 0ohm, 5% R0402 SMB_VR_PVCCIN_CPU_SCL_R
C22 0.1uF 25V C0402
[38] PWRGD_VR_PVCCANA R62 0ohm 5% R0402
R37 0ohm, 5% R0402 VR_PVCCIN_CPU_EN
[33] +V3P3A_PG R4 0ohm, 5% R0402
VR_P1V8_CPU_EN
[31] PWRGD_PVCCIN_CPU R549 0ohm, 5% R0402
[38,43] +V1P8A_PG
[31] IRQ_PVCCIN_CPU_VRHOT_LVC3_N
[31] FM_PVCCIN_CPU_PWR_IN_ALERT_N
FM_PVCCIN_CPU_PWR_IN_ALERT_N
R533 49.9 1% R0402
R517 121 1% R0402
R534 X/100 1% R0402
SVID_VALERT_VCCIN_CPU R20 0ohm, 5% R0402 SVID_ALERT0_CPU_R_N [13,43]
SVID_VDIO_PVCCIN_CPU R23 0ohm, 5% R0402 SVID_DIO0_CPU_R [13,43]
SVID_VCLK_PVCCIN_CPU R29 150 1% R0402 SVID_CLK0_CPU_R [13,43]

	PVCCIN/600KHz	P1V8/600KHz
TDC	50A	2A
IccMax	147A	2.6A
Vboot	1.8V	1.8V
Load Line	1.4mohm	mohm
SVID Address	00h, SVID0 Bus #1	01h, SVID0 Bus#1

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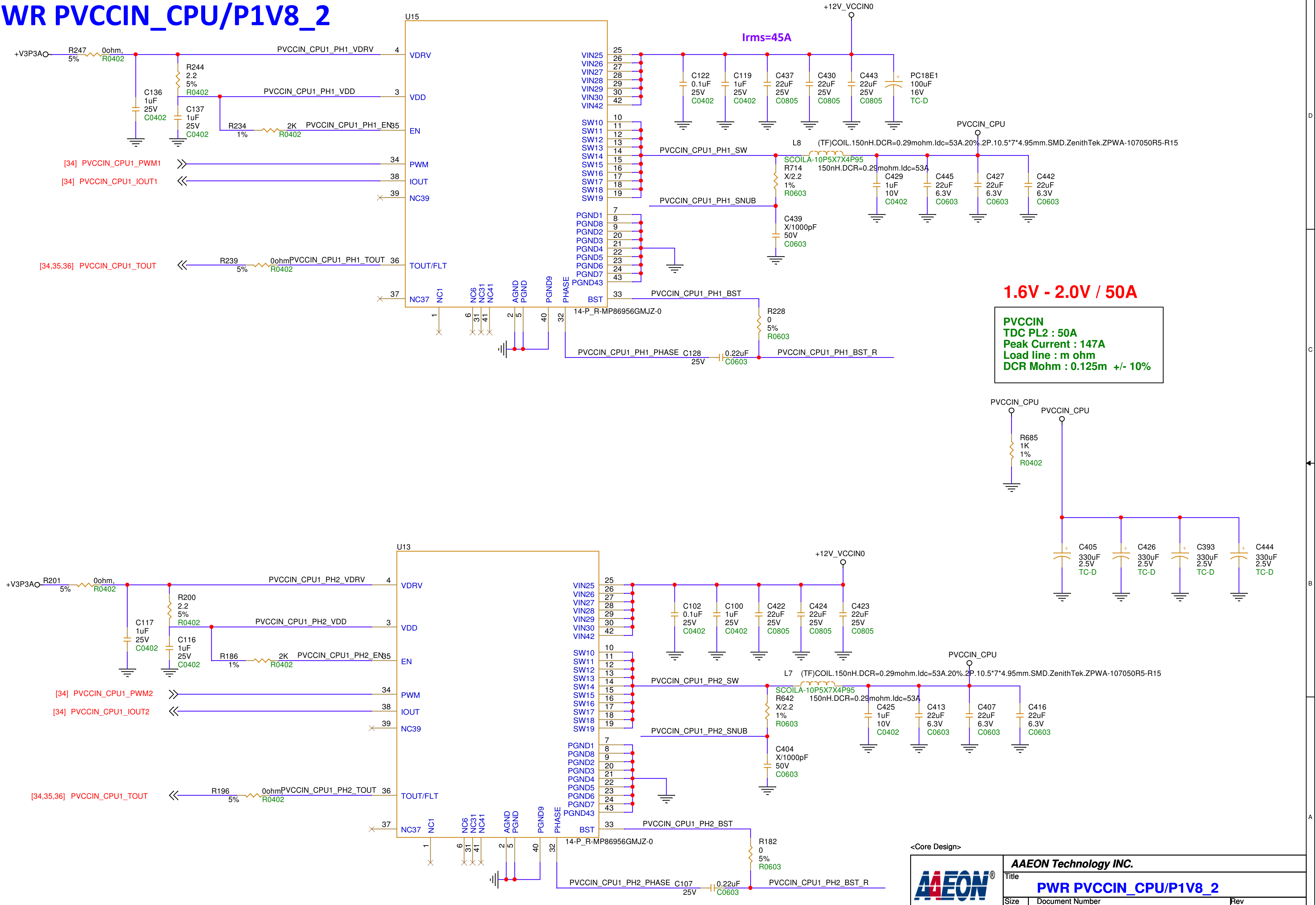
PWR PVCCIN_CPU/P1V8_2


U15
+V3P3A
R247 0ohm, 5% R0402
R244 2.2 5% R0402
C136 1uF 25V C0402
C137 1uF 25V C0402
R234 2K 1% R0402
PVCCIN_CPU1_PH1_VDRV
PVCCIN_CPU1_PH1_VDD
PVCCIN_CPU1_PH1_EN
[34] PVCCIN_CPU1_PWM1
[34] PVCCIN_CPU1_IOUT1
[34,35,36] PVCCIN_CPU1_TOUT
R239 0ohm 5% R0402
PVCCIN_CPU1_PH1_TOUT
VDRV
VDD
EN
PWM
IOUT
NC39
TOUT/FLT
NC37
NC1
NC6
NC31
NC41
AGND
PGND
PGND9
PHASE
BST
VIN25
VIN26
VIN27
VIN28
VIN29
VIN30
VIN42
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
SW19
PGND1
PGND8
PGND2
PGND3
PGND4
PGND5
PGND6
PGND7
PGND43
14-P_R-MP86956GMJZ-0
+12V_VCCIN0
Irms=45A
C122 0.1uF 25V C0402
C119 1uF 25V C0402
C437 22uF 25V C0805
C430 22uF 25V C0805
C443 22uF 25V C0805
PC18E1 100uF 16V TC-D
PVCCIN_CPU
L8
(TF)COIL.150nH.DCR=0.29mohm.Idc=53A.20%.2P.10.5*7*4.95mm.SMD.ZenithTek.ZPWA-107050R5-R15
SCOILA-10P5X7X4P95
150nH.DCR=0.29mohm.Idc=53A
PVCCIN_CPU1_PH1_SW
R714 X/2.2 1% R0603
PVCCIN_CPU1_PH1_SNUB
C439 X/1000pF 50V C0603
C429 1uF 10V C0402
C445 22uF 6.3V C0603
C427 22uF 6.3V C0603
C442 22uF 6.3V C0603
PVCCIN_CPU1_PH1_BST
R228 0 5% R0603
PVCCIN_CPU1_PH1_PHASE
C128 0.22uF 25V C0603
PVCCIN_CPU1_PH1_BST_R
R685 1K 1% R0402
C405 330uF 2.5V TC-D
C426 330uF 2.5V TC-D
C393 330uF 2.5V TC-D
C444 330uF 2.5V TC-D
U13
R201 0ohm, 5% R0402
R200 2.2 5% R0402
C117 1uF 25V C0402
C116 1uF 25V C0402
R186 2K 1% R0402
PVCCIN_CPU1_PH2_VDRV
PVCCIN_CPU1_PH2_VDD
PVCCIN_CPU1_PH2_EN
[34] PVCCIN_CPU1_PWM2
[34] PVCCIN_CPU1_IOUT2
[34,35,36] PVCCIN_CPU1_TOUT
R196 0ohm 5% R0402
PVCCIN_CPU1_PH2_TOUT
C102 0.1uF 25V C0402
C100 1uF 25V C0402
C422 22uF 25V C0805
C424 22uF 25V C0805
C423 22uF 25V C0805
L7
PVCCIN_CPU1_PH2_SW
R642 X/2.2 1% R0603
PVCCIN_CPU1_PH2_SNUB
C404 X/1000pF 50V C0603
C425 1uF 10V C0402
C413 22uF 6.3V C0603
C407 22uF 6.3V C0603
C416 22uF 6.3V C0603
PVCCIN_CPU1_PH2_BST
R182 0 5% R0603
PVCCIN_CPU1_PH2_PHASE
C107 0.22uF 25V C0603
PVCCIN_CPU1_PH2_BST_R

1.6V - 2.0V / 50A

PVCCIN
TDC PL2 : 50A
Peak Current : 147A
Load line : m ohm
DCR Mohm : 0.125m +/- 10%

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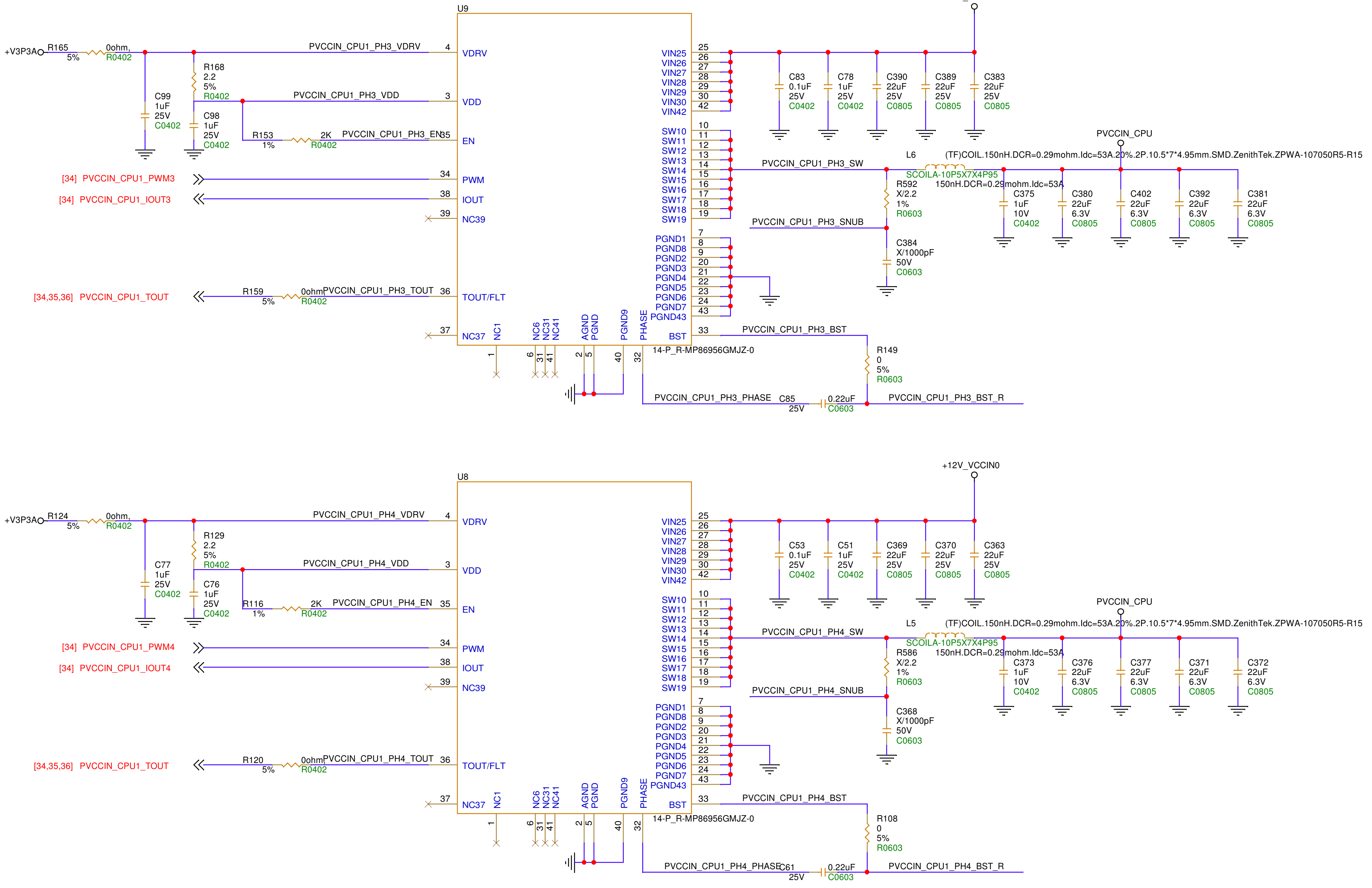
U9
+12V_VCCIN0
+V3P3A
R165 0ohm, 5% R0402
PVCCIN_CPU1_PH3_VDRV
R168 2.2 5% R0402
C99 1uF 25V C0402
C98 1uF 25V C0402
PVCCIN_CPU1_PH3_VDD
R153 2K 1% R0402
PVCCIN_CPU1_PH3_EN
[34] PVCCIN_CPU1_PWM3
[34] PVCCIN_CPU1_IOUT3
R159 0ohm 5% R0402
PVCCIN_CPU1_PH3_TOUT
[34,35,36] PVCCIN_CPU1_TOUT
VDRV
VDD
EN
PWM
IOUT
NC39
TOUT/FLT
NC37
NC1
NC6
NC31
NC41
AGND
PGND
PGND9
PHASE
BST
VIN25 VIN26 VIN27 VIN28 VIN29 VIN30 VIN42
SW10 SW11 SW12 SW13 SW14 SW15 SW16 SW17 SW18 SW19
PGND1 PGND8 PGND2 PGND3 PGND4 PGND5 PGND6 PGND7 PGND43
14-P_R-MP86956GMJZ-0
C83 0.1uF 25V C0402
C78 1uF 25V C0402
C390 22uF 25V C0805
C389 22uF 25V C0805
C383 22uF 25V C0805
PVCCIN_CPU
L6
(TF)COIL.150nH.DCR=0.29mohm.Idc=53A.20%.2P.10.5*7*4.95mm.SMD.ZenithTek.ZPWA-107050R5-R15
SCOILA-10P5X7X4P95
150nH.DCR=0.29mohm.Idc=53A
PVCCIN_CPU1_PH3_SW
R592 X/2.2 1% R0603
PVCCIN_CPU1_PH3_SNUB
C384 X/1000pF 50V C0603
C375 1uF 10V C0402
C380 22uF 6.3V C0805
C402 22uF 6.3V C0805
C392 22uF 6.3V C0805
C381 22uF 6.3V C0805
PVCCIN_CPU1_PH3_BST
R149 0 5% R0603
PVCCIN_CPU1_PH3_PHASE
C85 0.22uF 25V C0603
PVCCIN_CPU1_PH3_BST_R
U8
+12V_VCCIN0
+V3P3A
R124 0ohm, 5% R0402
PVCCIN_CPU1_PH4_VDRV
R129 2.2 5% R0402
C77 1uF 25V C0402
C76 1uF 25V C0402
PVCCIN_CPU1_PH4_VDD
R116 2K 1% R0402
PVCCIN_CPU1_PH4_EN
[34] PVCCIN_CPU1_PWM4
[34] PVCCIN_CPU1_IOUT4
R120 0ohm 5% R0402
PVCCIN_CPU1_PH4_TOUT
[34,35,36] PVCCIN_CPU1_TOUT
14-P_R-MP86956GMJZ-0
C53 0.1uF 25V C0402
C51 1uF 25V C0402
C369 22uF 25V C0805
C370 22uF 25V C0805
C363 22uF 25V C0805
PVCCIN_CPU
L5
(TF)COIL.150nH.DCR=0.29mohm.Idc=53A.20%.2P.10.5*7*4.95mm.SMD.ZenithTek.ZPWA-107050R5-R15
SCOILA-10P5X7X4P95
150nH.DCR=0.29mohm.Idc=53A
PVCCIN_CPU1_PH4_SW
R586 X/2.2 1% R0603
PVCCIN_CPU1_PH4_SNUB
C368 X/1000pF 50V C0603
C373 1uF 10V C0402
C376 22uF 6.3V C0805
C377 22uF 6.3V C0805
C371 22uF 6.3V C0805
C372 22uF 6.3V C0805
PVCCIN_CPU1_PH4_BST
R108 0 5% R0603
PVCCIN_CPU1_PH4_PHASE
C61 0.22uF 25V C0603
PVCCIN_CPU1_PH4_BST_R

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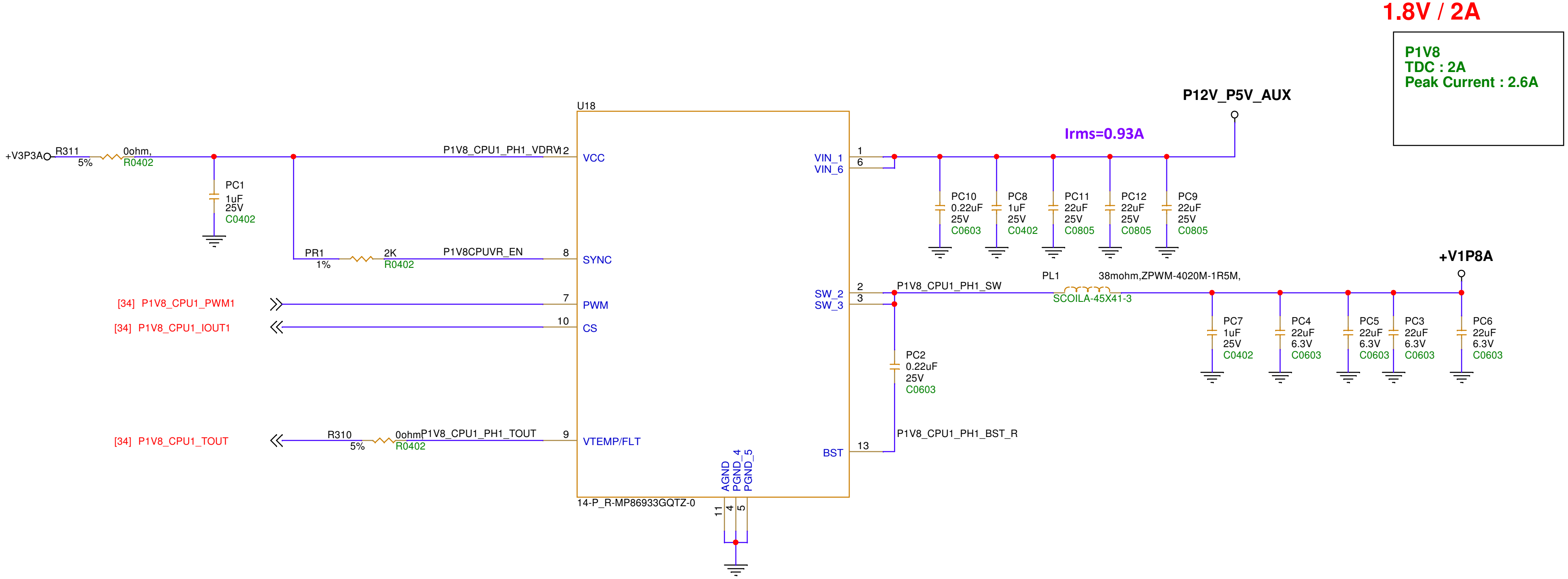

1.8V / 2A

P1V8
TDC : 2A
Peak Current : 2.6A

+V3P3A
R311
0ohm,
5%
R0402
PC1
1uF
25V
C0402
PR1
1%
2K
R0402
P1V8_CPU1_PH1_VDRV
P1V8CPUVR_EN
[34] P1V8_CPU1_PWM1
[34] P1V8_CPU1_IOUT1
[34] P1V8_CPU1_TOUT
R310
5%
0ohm
R0402
P1V8_CPU1_PH1_TOUT
U18
12
VCC
8
SYNC
7
PWM
10
CS
9
VTEMP/FLT
AGND
PGND_4
PGND_5
11
4
5
14-P_R-MP86933GQTZ-0
VIN_1
VIN_6
1
6
SW_2
SW_3
2
3
BST
13
P12V_P5V_AUX
Irms=0.93A
PC10
0.22uF
25V
C0603
PC8
1uF
25V
C0402
PC11
22uF
25V
C0805
PC12
22uF
25V
C0805
PC9
22uF
25V
C0805
P1V8_CPU1_PH1_SW
PL1
38mohm,ZPWM-4020M-1R5M,
SCOILA-45X41-3
+V1P8A
PC7
1uF
25V
C0402
PC4
22uF
6.3V
C0603
PC5
22uF
6.3V
C0603
PC3
22uF
6.3V
C0603
PC6
22uF
6.3V
C0603
PC2
0.22uF
25V
C0603
P1V8_CPU1_PH1_BST_R

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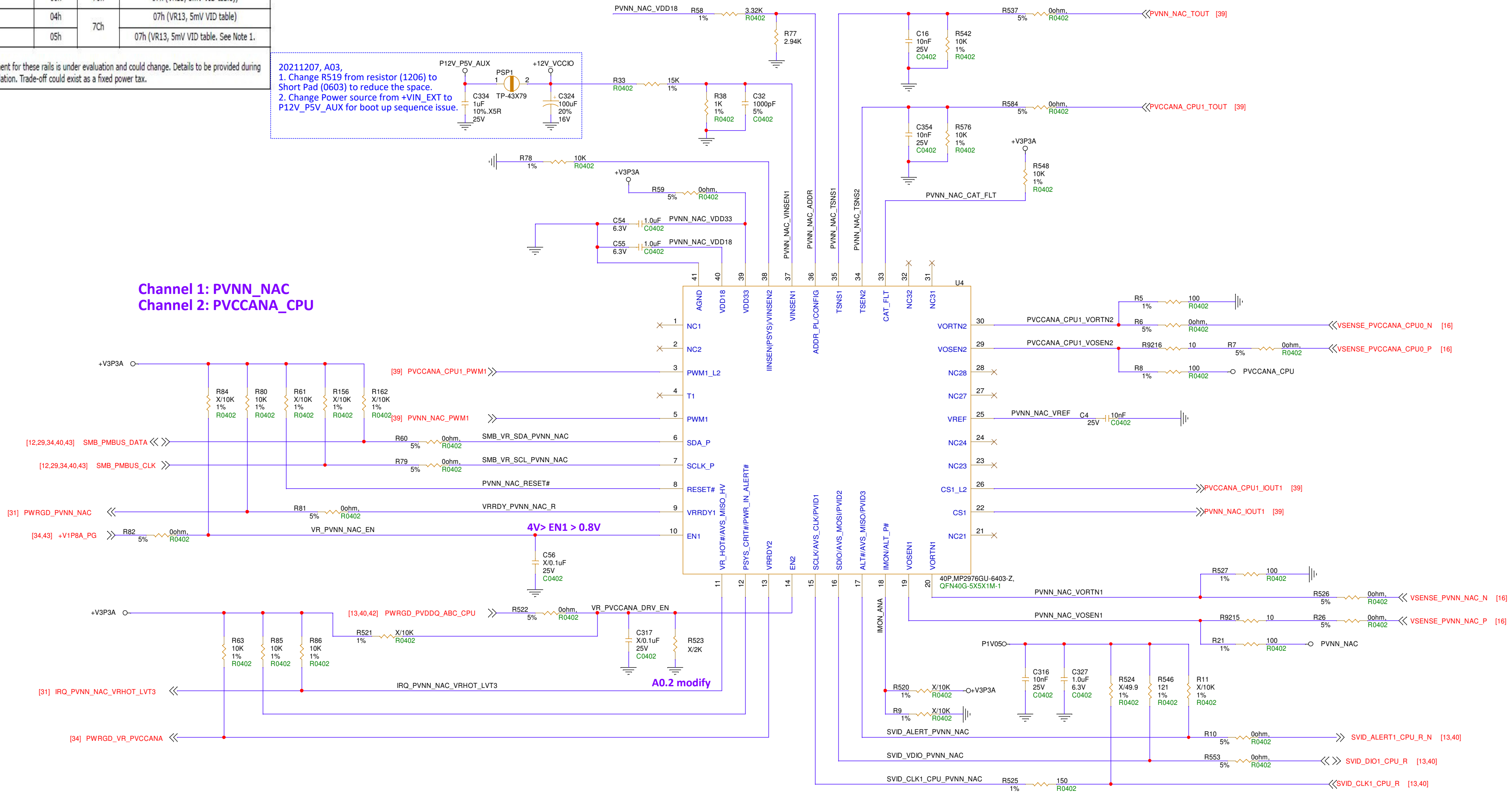
PWR PVNN_NAC/ PVCCANA_CPU_1

Table 17-5. VR13.0 SVID0, SVID1 and SMBUS Addresses - Brighton City RP

VR	SVID0 (bus 1)	SVID1 (bus 2)	SMBUS	Protocol ID
PVCCIN_CPU	00h		60h	04h (VR13, 10mV VID table)
P1V8	01h			04h (VR13, 10mV VID table). See Note 1.
P1V05	03h		84h	07h (VR13, 5mV VID table). See Note 1.
PVNN_PCH	05h		82h	07h (VR13, 5mV VID table)
PVDDQ_ABC_CPU		00h	70h	07h (VR13, 5mV VID table))
PVNN_NAC		04h	7Ch	07h (VR13, 5mV VID table)
PVCCANA_CPU		05h		07h (VR13, 5mV VID table. See Note 1.

Note:

1. VR13.0 requirement for these rails is under evaluation and could change. Details to be provided during post-Silicon validation. Trade-off could exist as a fixed power tax.



20211207, A03,
1. Change R519 from resistor (1206) to Short Pad (0603) to reduce the space.
2. Change Power source from +VIN_EXT to P12V_P5V_AUX for boot up sequence issue.

Channel 1: PVNN_NAC
Channel 2: PVCCANA_CPU

4V> EN1 > 0.8V

A0.2 modify

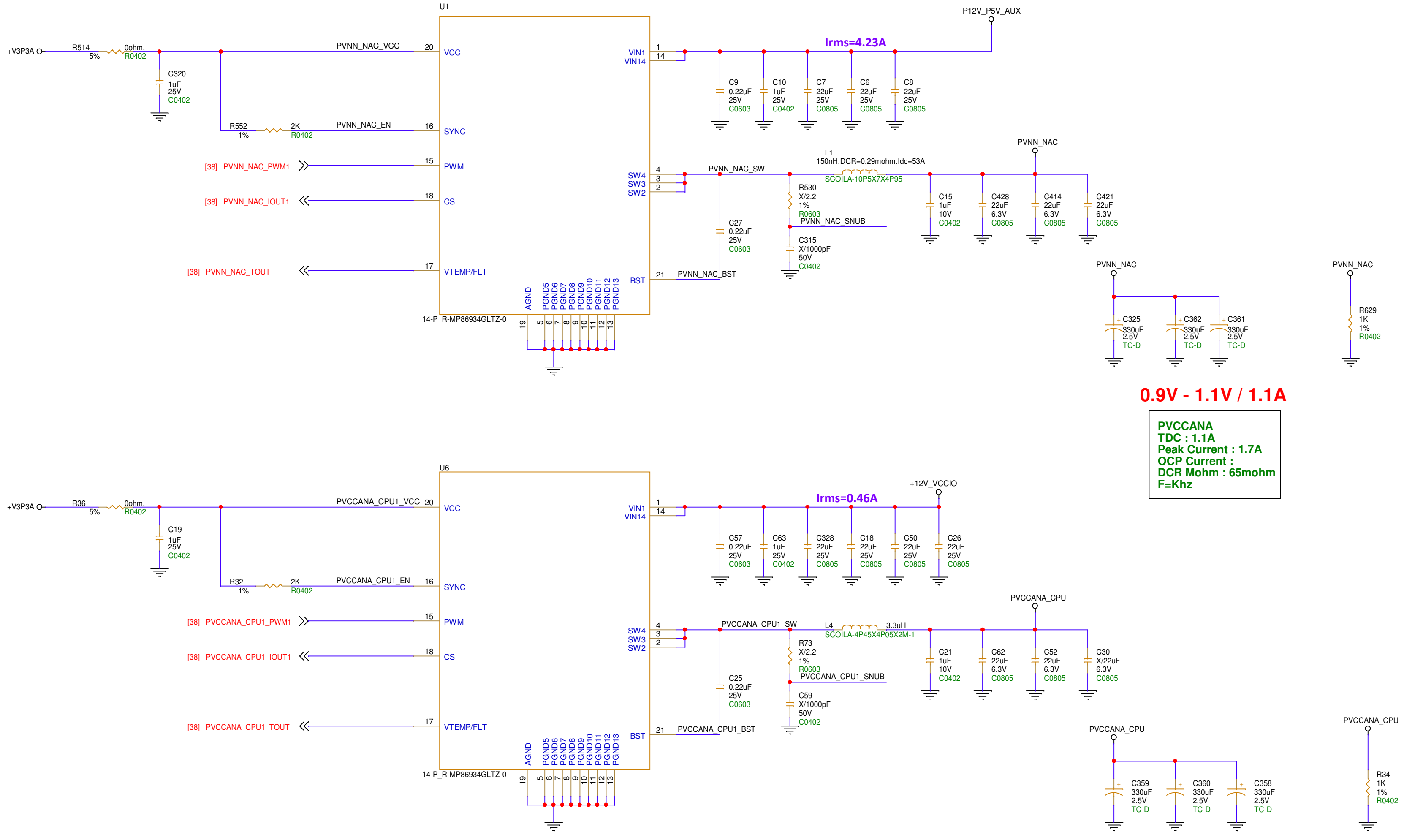
P12V_P5V_AUX
PSP1
1
2
TP-43X79
+12V_VCCIO
C334 1uF 10%.X5R 25V
C324 100uF 20% 16V
PVNN_NAC_VDD18
R58 1% 3.32K R0402
R77 2.94K
R33 R0402 15K 1%
R38 1K 1% R0402
C32 1000pF 5% C0402
R78 1% 10K R0402
+V3P3A
R59 5% 0ohm, R0402
C54 6.3V 1.0uF C0402
PVNN_NAC_VDD33
C55 6.3V 1.0uF C0402
PVNN_NAC_VDD18
PVNN_NAC_VINSEN1
PVNN_NAC_ADDR
PVNN_NAC_TSNS1
PVNN_NAC_TSNS2
R537 5% 0ohm, R0402
PVNN_NAC_TOUT [39]
C16 10nF 25V C0402
R542 10K 1% R0402
R584 5% 0ohm, R0402
PVCCANA_CPU1_TOUT [39]
C354 10nF 25V C0402
R576 10K 1% R0402
+V3P3A
R548 10K 1% R0402
PVNN_NAC_CAT_FLT
U4
41 AGND
40 VDD18
39 VDD33
38 IINSEN(PSYS)/VINSEN2
37 VINSEN1
36 ADDR_PL/CONFIG
35 TSNS1
34 TSEN2
33 CAT_FLT
32 NC32
31 NC31
1 NC1
2 NC2
3 PWM1_L2
4 T1
5 PWM1
6 SDA_P
7 SCLK_P
8 RESET#
9 VRRDY1
10 EN1
11 VR_HOT#/AVS_MISO_HV
12 PSYS_CRIT#/PWR_IN_ALERT#
13 VRRDY2
14 EN2
15 SCLK/AVS_CLK/PVID1
16 SDIO/AVS_MOSI/PVID2
17 ALT#/AVS_MISO/PVID3
18 IMON/ALT_P#
19 VOSEN1
20 VORTN1
30 VORTN2
29 VOSEN2
28 NC28
27 NC27
25 VREF
24 NC24
23 NC23
26 CS1_L2
22 CS1
21 NC21
40P,MP2976GU-6403-Z,
QFN40G-5X5X1M-1
R5 1% 100 R0402
PVCCANA_CPU1_VORTN2
R6 5% 0ohm, R0402
VSENSE_PVCCANA_CPU0_N [16]
PVCCANA_CPU1_VOSEN2
R9216 10
R7 5% 0ohm, R0402
VSENSE_PVCCANA_CPU0_P [16]
R8 1% 100 R0402
PVCCANA_CPU
PVNN_NAC_VREF
C4 25V 10nF C0402
PVCCANA_CPU1_IOUT1 [39]
PVNN_NAC_IOUT1 [39]
+V3P3A
R84 X/10K 1% R0402
R80 10K 1% R0402
R61 X/10K 1% R0402
R156 X/10K 1% R0402
R162 X/10K 1% R0402
[39] PVCCANA_CPU1_PWM1
[39] PVNN_NAC_PWM1
[12,29,34,40,43] SMB_PMBUS_DATA
R60 5% 0ohm, R0402
SMB_VR_SDA_PVNN_NAC
[12,29,34,40,43] SMB_PMBUS_CLK
R79 5% 0ohm, R0402
SMB_VR_SCL_PVNN_NAC
PVNN_NAC_RESET#
[31] PWRGD_PVNN_NAC
R81 5% 0ohm, R0402
VRRDY_PVNN_NAC_R
[34,43] +V1P8A_PG
R82 5% 0ohm, R0402
VR_PVNN_NAC_EN
C56 X/0.1uF 25V C0402
+V3P3A
R63 10K 1% R0402
R85 10K 1% R0402
R86 10K 1% R0402
[13,40,42] PWRGD_PVDDQ_ABC_CPU
R522 5% 0ohm, R0402
VR_PVCCANA_DRV_EN
R521 1% X/10K R0402
C317 X/0.1uF 25V C0402
R523 X/2K
[31] IRQ_PVNN_NAC_VRHOT_LVT3
IRQ_PVNN_NAC_VRHOT_LVT3
[34] PWRGD_VR_PVCCANA
IMON_ANA
R527 1% 100 R0402
PVNN_NAC_VORTN1
R526 5% 0ohm, R0402
VSENSE_PVNN_NAC_N [16]
PVNN_NAC_VOSEN1
R9215 10
R26 5% 0ohm, R0402
VSENSE_PVNN_NAC_P [16]
R21 1% 100 R0402
PVNN_NAC
P1V05
C316 10nF 25V C0402
C327 1.0uF 6.3V C0402
R524 X/49.9 1% R0402
R546 121 1% R0402
R11 X/10K 1% R0402
R520 1% X/10K R0402
+V3P3A
R9 1% X/10K R0402
SVID_ALERT_PVNN_NAC
R10 5% 0ohm, R0402
SVID_ALERT1_CPU_R_N [13,40]
SVID_VDIO_PVNN_NAC
R553 5% 0ohm, R0402
SVID_DIO1_CPU_R [13,40]
SVID_CLK1_CPU_PVNN_NAC
R525 1% 150 R0402
SVID_CLK1_CPU_R [13,40]

CooperLake-300W	*PVNN_NAC/600KHz*	*PVCCANA/600KHz*
TDC	*16.7A*	*1.1A*
IccMax	*17.6A*	*1.7A*
Vboot	*0.74V*	*1.0V*
Load Line	*0mohm*	*0mohm*
SVID Address	*04h, SVID1 Bus #2*	*05h,SVID1 Bus #2*

PWR PVNN_NAC/ PVCCANA_CPU_2

0.74V / 16.7A

PVNN_NAC
TDC : 16.7A
Peak Current : 17.6A
OCP Current :
DCR Mohm : 2.5MOHM
F=Khz


U1
+V3P3A
R514
5%
0ohm,
R0402
PVNN_NAC_VCC
20
VCC
C320
1uF
25V
C0402
R552
1%
2K
R0402
PVNN_NAC_EN
16
SYNC
[38] PVNN_NAC_PWM1
15
PWM
[38] PVNN_NAC_IOUT1
18
CS
[38] PVNN_NAC_TOUT
17
VTEMP/FLT
AGND
PGND5
PGND6
PGND7
PGND8
PGND9
PGND10
PGND11
PGND12
PGND13
19 5 6 7 8 9 10 11 12 13
14-P_R-MP86934GLTZ-0
VIN1
VIN14
1
14
P12V_P5V_AUX
Irms=4.23A
C9
0.22uF
25V
C0603
C10
1uF
25V
C0402
C7
22uF
25V
C0805
C6
22uF
25V
C0805
C8
22uF
25V
C0805
SW4
SW3
SW2
4
3
2
PVNN_NAC_SW
L1
150nH.DCR=0.29mohm.Idc=53A
SCOILA-10P5X7X4P95
PVNN_NAC
R530
X/2.2
1%
R0603
PVNN_NAC_SNUB
C315
X/1000pF
50V
C0402
C27
0.22uF
25V
C0603
C15
1uF
10V
C0402
C428
22uF
6.3V
C0805
C414
22uF
6.3V
C0805
C421
22uF
6.3V
C0805
BST
21
PVNN_NAC_BST
PVNN_NAC
C325
330uF
2.5V
TC-D
C362
330uF
2.5V
TC-D
C361
330uF
2.5V
TC-D
PVNN_NAC
R629
1K
1%
R0402
U6
+V3P3A
R36
5%
0ohm,
R0402
PVCCANA_CPU1_VCC
20
VCC
C19
1uF
25V
C0402
R32
1%
2K
R0402
PVCCANA_CPU1_EN
16
SYNC
[38] PVCCANA_CPU1_PWM1
15
PWM
[38] PVCCANA_CPU1_IOUT1
18
CS
[38] PVCCANA_CPU1_TOUT
17
VTEMP/FLT
AGND
PGND5
PGND6
PGND7
PGND8
PGND9
PGND10
PGND11
PGND12
PGND13
19 5 6 7 8 9 10 11 12 13
14-P_R-MP86934GLTZ-0
VIN1
VIN14
1
14
+12V_VCCIO
Irms=0.46A
C57
0.22uF
25V
C0603
C63
1uF
25V
C0402
C328
22uF
25V
C0805
C18
22uF
25V
C0805
C50
22uF
25V
C0805
C26
22uF
25V
C0805
SW4
SW3
SW2
4
3
2
PVCCANA_CPU1_SW
L4
3.3uH
SCOILA-4P45X4P05X2M-1
PVCCANA_CPU
R73
X/2.2
1%
R0603
PVCCANA_CPU1_SNUB
C59
X/1000pF
50V
C0402
C25
0.22uF
25V
C0603
C21
1uF
10V
C0402
C62
22uF
6.3V
C0805
C52
22uF
6.3V
C0805
C30
X/22uF
6.3V
C0805
BST
21
PVCCANA_CPU1_BST
PVCCANA_CPU
C359
330uF
2.5V
TC-D
C360
330uF
2.5V
TC-D
C358
330uF
2.5V
TC-D
PVCCANA_CPU
R34
1K
1%
R0402

0.9V - 1.1V / 1.1A

PVCCANA
TDC : 1.1A
Peak Current : 1.7A
OCP Current :
DCR Mohm : 65mohm
F=Khz

<Core Design>

AAEON An ASUS Company	*AAEON Technology INC.*
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Size C	Document Number COM-ICDB7	Rev A0.3_0_0
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PWR PVDDQ_ABC_CPU_1

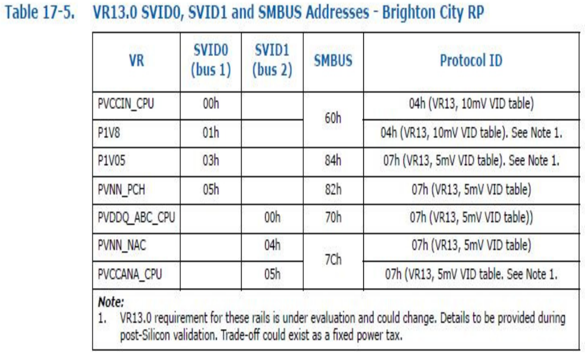
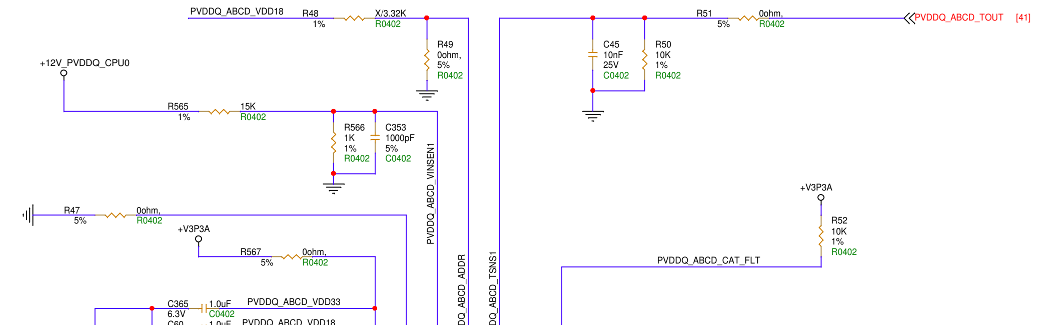


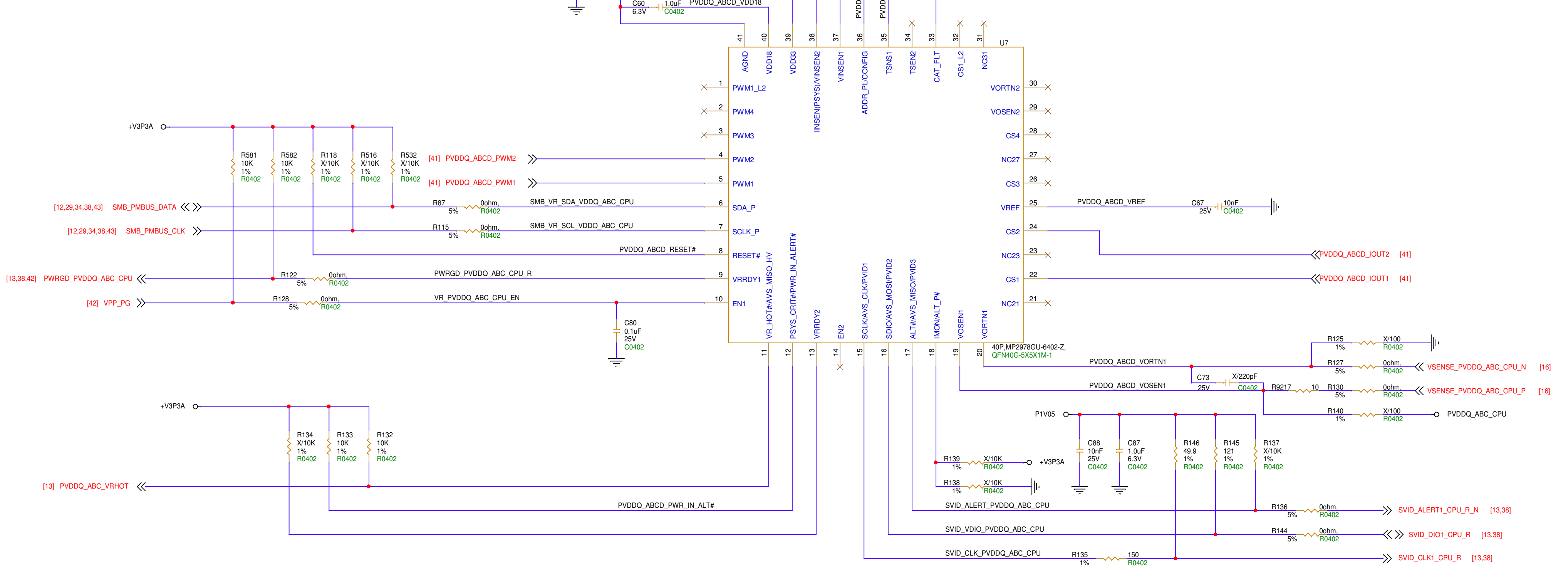
Table 17-5. VR13.0 SVID0, SVID1 and SMBUS Addresses - Brighton City RP

VR	SVID0 (bus 1)	SVID1 (bus 2)	SMBUS	Protocol ID
PVCCIN_CPU	00h		60h	04h (VR13, 10mV VID table)
P1V8	01h			04h (VR13, 10mV VID table). See Note 1.
P1V05	03h		84h	07h (VR13, 5mV VID table). See Note 1.
PVNN_PCH	05h		82h	07h (VR13, 5mV VID table)
PVDDQ_ABC_CPU		00h	70h	07h (VR13, 5mV VID table))
PVNN_NAC		04h	7Ch	07h (VR13, 5mV VID table)
PVCCANA_CPU		05h		07h (VR13, 5mV VID table. See Note 1.

Note:
1. VR13.0 requirement for these rails is under evaluation and could change. Details to be provided during post-Silicon validation. Trade-off could exist as a fixed power tax.

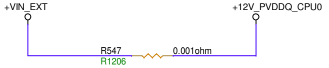


PVDDQ_ABCD_VDD18
R48 1% X/3.32K R0402
R49 0ohm, 5% R0402
+12V_PVDDQ_CPU0
R565 1% 15K R0402
R566 1K 1% R0402
C353 1000pF 5% C0402
PVDDQ_ABCD_VINSEN1
PVDDQ_ABCD_ADDR
PVDDQ_ABCD_TSNS1
R51 5% 0ohm, R0402
PVDDQ_ABCD_TOUT [41]
C45 10nF 25V C0402
R50 10K 1% R0402
+V3P3A
R52 10K 1% R0402
PVDDQ_ABCD_CAT_FLT
R47 5% 0ohm, R0402
+V3P3A
R567 5% 0ohm, R0402
C365 6.3V 1.0uF C0402
PVDDQ_ABCD_VDD33



C60 6.3V 1.0uF C0402
PVDDQ_ABCD_VDD18
U7
41 AGND
40 VDD18
39 VDD33
38 IINSEN(PSYS)/VINSEN2
37 VINSEN1
36 ADDR_PLCONFIG
35 TSNS1
34 TSEN2
33 CAT_FLT
32 CS1_L2
31 NC31
1 PWM1_L2
2 PWM4
3 PWM3
4 PWM2
5 PWM1
6 SDA_P
7 SCLK_P
8 RESET#
9 VRRDY1
10 EN1
30 VORTN2
29 VOSEN2
28 CS4
27 NC27
26 CS3
25 VREF
24 CS2
23 NC23
22 CS1
21 NC21
11 VR_HOT#/AVS_MISO_HV
12 PSYS_CRIT#/PWR_IN_ALERT#
13 VRRDY2
14 EN2
15 SCLK/AVS_CLK/PVID1
16 SDIO/AVS_MOSI/PVID2
17 ALT#/AVS_MISO/PVID3
18 IMON/ALT_P#
19 VOSEN1
20 VORTN1
40P,MP2978GU-6402-Z, QFN40G-5X5X1M-1
+V3P3A
R581 10K 1% R0402
R582 10K 1% R0402
R118 X/10K 1% R0402
R516 X/10K 1% R0402
R532 X/10K 1% R0402
[41] PVDDQ_ABCD_PWM2
[41] PVDDQ_ABCD_PWM1
[12,29,34,38,43] SMB_PMBUS_DATA
[12,29,34,38,43] SMB_PMBUS_CLK
R87 5% 0ohm, R0402
SMB_VR_SDA_VDDQ_ABC_CPU
R115 5% 0ohm, R0402
SMB_VR_SCL_VDDQ_ABC_CPU
PVDDQ_ABCD_RESET#
[13,38,42] PWRGD_PVDDQ_ABC_CPU
R122 5% 0ohm, R0402
PWRGD_PVDDQ_ABC_CPU_R
[42] VPP_PG
R128 5% 0ohm, R0402
VR_PVDDQ_ABC_CPU_EN
C80 0.1uF 25V C0402
PVDDQ_ABCD_VREF
C67 25V 10nF C0402
PVDDQ_ABCD_IOUT2 [41]
PVDDQ_ABCD_IOUT1 [41]
R125 1% X/100 R0402
R127 5% 0ohm, R0402
VSENSE_PVDDQ_ABC_CPU_N [16]
PVDDQ_ABCD_VORTN1
C73 25V X/220pF C0402
PVDDQ_ABCD_VOSEN1
R9217 10
R130 5% 0ohm, R0402
VSENSE_PVDDQ_ABC_CPU_P [16]
R140 1% X/100 R0402
PVDDQ_ABC_CPU
P1V05
C88 10nF 25V C0402
C87 1.0uF 6.3V C0402
R146 49.9 1% R0402
R145 121 1% R0402
R137 X/10K 1% R0402
R139 1% X/10K R0402
+V3P3A
R138 1% X/10K R0402
+V3P3A
R134 X/10K 1% R0402
R133 10K 1% R0402
R132 10K 1% R0402
[13] PVDDQ_ABC_VRHOT
PVDDQ_ABCD_PWR_IN_ALT#
SVID_ALERT_PVDDQ_ABC_CPU
R136 5% 0ohm, R0402
SVID_ALERT1_CPU_R_N [13,38]
SVID_VDIO_PVDDQ_ABC_CPU
R144 5% 0ohm, R0402
SVID_DIO1_CPU_R [13,38]
SVID_CLK_PVDDQ_ABC_CPU
R135 1% 150 R0602
SVID_CLK1_CPU_R [13,38]

	PVDDQ/800KHz	
TDC	39A	
IccMax	47A	
Vboot	1.2V	
Load Line	0.3mohm	
SVID Address	00H, SVID1 Bus #2	



+VIN_EXT
+12V_PVDDQ_CPU0
R547 R1206
0.001ohm

<Core Design>

AAEON Technology INC.

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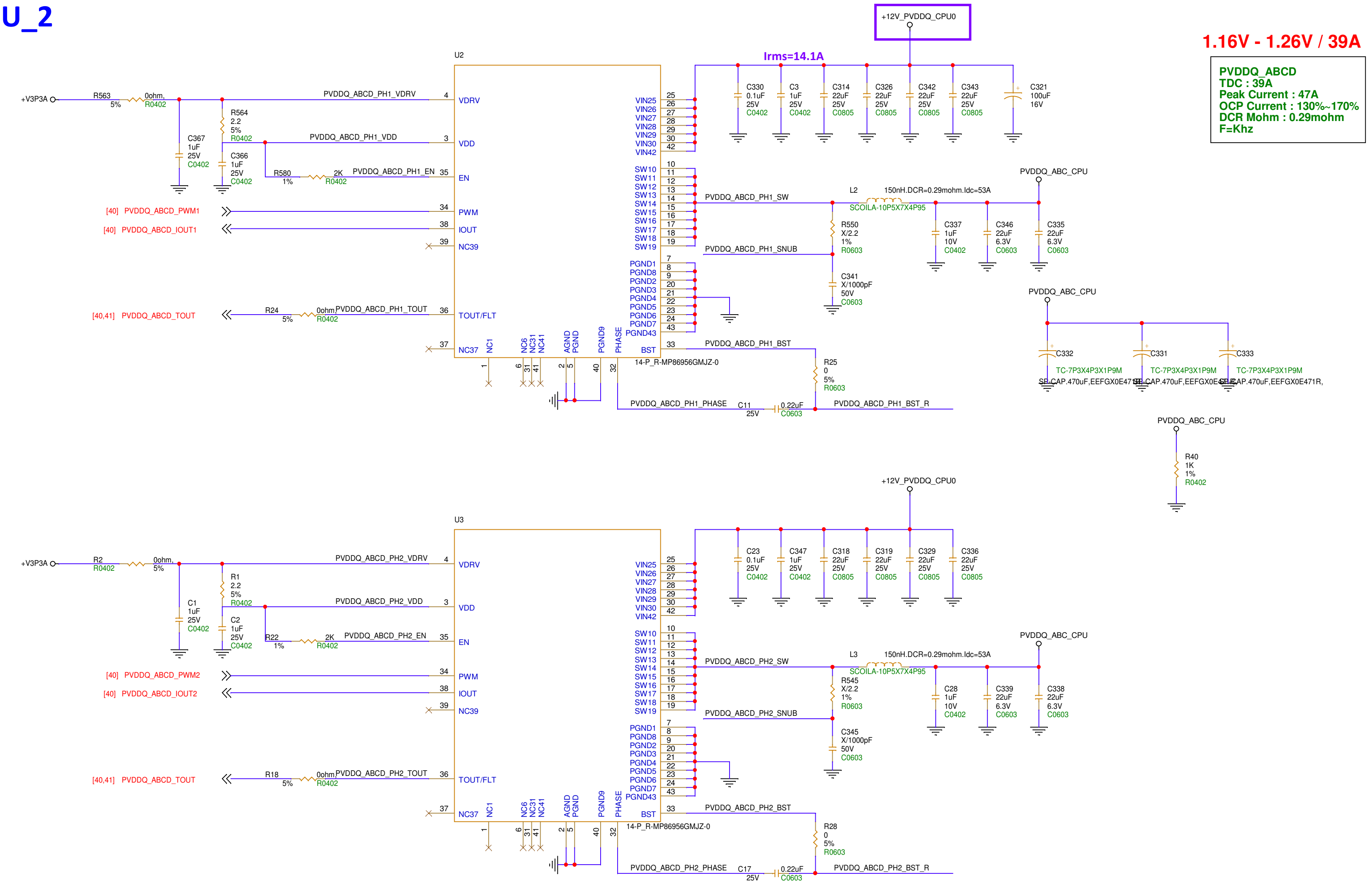
PWR PVDDQ_ABC_CPU_2


+12V_PVDDQ_CPU0
Irms=14.1A
U2
+V3P3A
R563 0ohm. 5% R0402
PVDDQ_ABCD_PH1_VDRV
R564 2.2 5% R0402
C367 1uF 25V C0402
C366 1uF 25V C0402
PVDDQ_ABCD_PH1_VDD
R580 2K 1% R0402
PVDDQ_ABCD_PH1_EN
[40] PVDDQ_ABCD_PWM1
[40] PVDDQ_ABCD_IOUT1
[40,41] PVDDQ_ABCD_TOUT
R24 0ohm 5% R0402
PVDDQ_ABCD_PH1_TOUT
VDRV
VDD
EN
PWM
IOUT
NC39
TOUT/FLT
NC37
NC1
NC6
NC31
NC41
AGND
PGND
PGND9
PHASE
BST
VIN25
VIN26
VIN27
VIN28
VIN29
VIN30
VIN42
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
SW19
PGND1
PGND8
PGND2
PGND3
PGND4
PGND5
PGND6
PGND7
PGND43
14-P_R-MP86956GMJZ-0
C330 0.1uF 25V C0402
C3 1uF 25V C0402
C314 22uF 25V C0805
C326 22uF 25V C0805
C342 22uF 25V C0805
C343 22uF 25V C0805
C321 100uF 16V
PVDDQ_ABCD_PH1_SW
L2 150nH.DCR=0.29mohm.Idc=53A
SCOILA-10P5X7X4P95
PVDDQ_ABC_CPU
R550 X/2.2 1% R0603
C337 1uF 10V C0402
C346 22uF 6.3V C0603
C335 22uF 6.3V C0603
PVDDQ_ABCD_PH1_SNUB
C341 X/1000pF 50V C0603
PVDDQ_ABCD_PH1_BST
R25 0 5% R0603
PVDDQ_ABCD_PH1_PHASE
C11 0.22uF 25V C0603
PVDDQ_ABCD_PH1_BST_R
C332 TC-7P3X4P3X1P9M SP-CAP.470uF,EEFGX0E471R,
C331 TC-7P3X4P3X1P9M SP-CAP.470uF,EEFGX0E471R,
C333 TC-7P3X4P3X1P9M SP-CAP.470uF,EEFGX0E471R,
R40 1K 1% R0402
U3
R2 0ohm. 5% R0402
PVDDQ_ABCD_PH2_VDRV
R1 2.2 5% R0402
C1 1uF 25V C0402
C2 1uF 25V C0402
PVDDQ_ABCD_PH2_VDD
R22 2K 1% R0402
PVDDQ_ABCD_PH2_EN
[40] PVDDQ_ABCD_PWM2
[40] PVDDQ_ABCD_IOUT2
R18 0ohm 5% R0402
PVDDQ_ABCD_PH2_TOUT
C23 0.1uF 25V C0402
C347 1uF 25V C0402
C318 22uF 25V C0805
C319 22uF 25V C0805
C329 22uF 25V C0805
C336 22uF 25V C0805
PVDDQ_ABCD_PH2_SW
L3 150nH.DCR=0.29mohm.Idc=53A
R545 X/2.2 1% R0603
C28 1uF 10V C0402
C339 22uF 6.3V C0603
C338 22uF 6.3V C0603
PVDDQ_ABCD_PH2_SNUB
C345 X/1000pF 50V C0603
PVDDQ_ABCD_PH2_BST
R28 0 5% R0603
PVDDQ_ABCD_PH2_PHASE
C17 0.22uF 25V C0603
PVDDQ_ABCD_PH2_BST_R

1.16V - 1.26V / 39A

PVDDQ_ABCD
TDC : 39A
Peak Current : 47A
OCP Current : 130%~170%
DCR Mohm : 0.29mohm
F=Khz

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AAEON Technology INC.	
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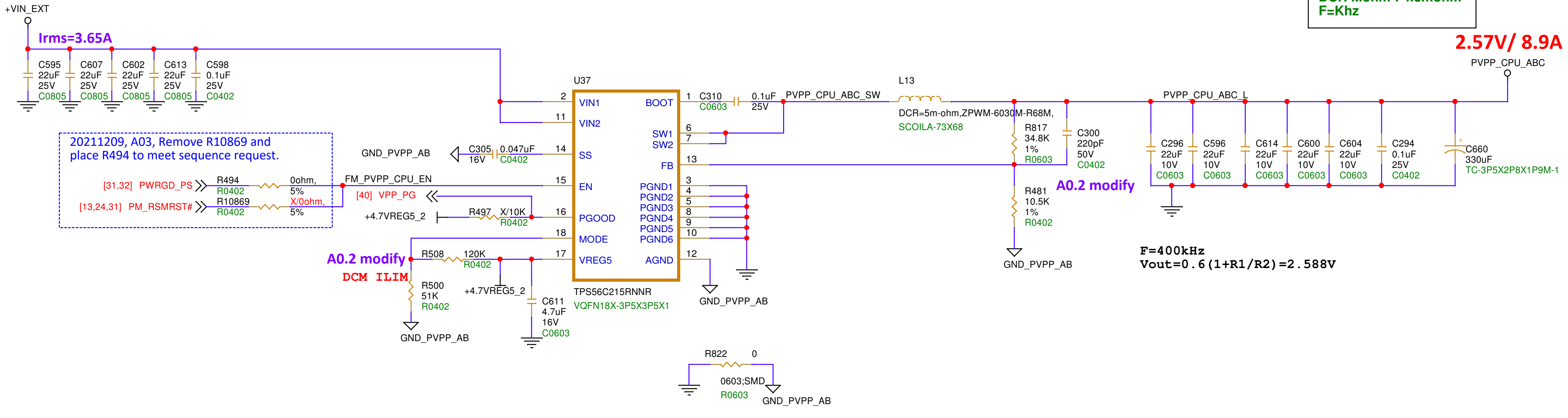
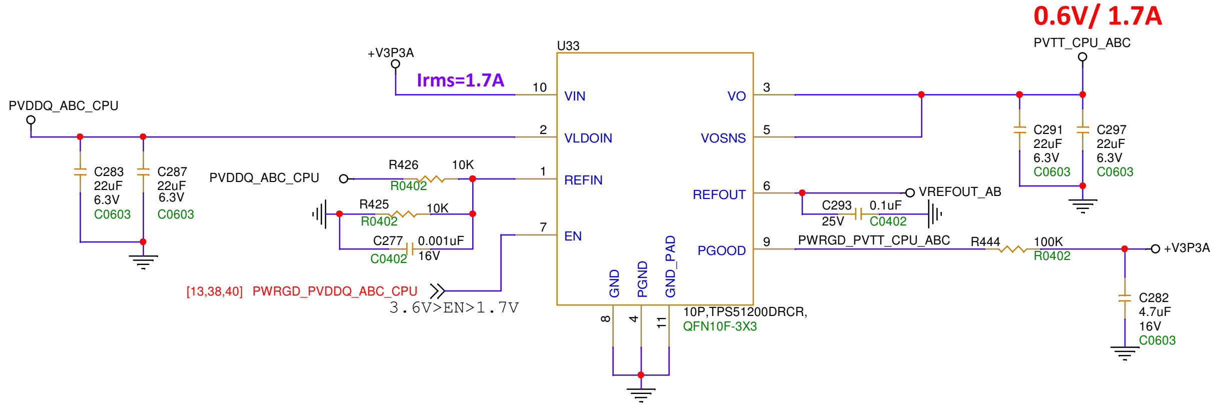
PWR PVPP_CPU_ABC

2.41V - 2.75V / 6.6A

PVPP_ABCD
TDC : 6.6A
Peak Current : 8.9A
OCP Current : NA
DCR Mohm : 4.8mohm
F=Khz


2.57V/ 8.9A
+VIN_EXT
Irms=3.65A
C595 22uF 25V C0805
C607 22uF 25V C0805
C602 22uF 25V C0805
C613 22uF 25V C0805
C598 0.1uF 25V C0402
20211209, A03, Remove R10869 and place R494 to meet sequence request.
[31,32] PWRGD_PS
R494 R0402 0ohm, 5%
[13,24,31] PM_RSMRST#
R10869 R0402 X/0ohm, 5%
FM_PVPP_CPU_EN
[40] VPP_PG
GND_PVPP_AB
C305 16V 0.047uF C0402
+4.7VREG5_2
R497 X/10K R0402
A0.2 modify
DCM ILIM
R508 120K R0402
R500 51K R0402
GND_PVPP_AB
+4.7VREG5_2
C611 4.7uF 16V C0603
U37
VIN1 VIN2 SS EN PGOOD MODE VREG5
BOOT SW1 SW2 FB PGND1 PGND2 PGND3 PGND4 PGND5 PGND6 AGND
TPS56C215RNNR
VQFN18X-3P5X3P5X1
C310 C0603 0.1uF 25V
PVPP_CPU_ABC_SW
L13
DCR=5m-ohm,ZPWM-6030M-R68M,
SCOILA-73X68
R817 34.8K 1% R0603
C300 220pF 50V C0402
A0.2 modify
R481 10.5K 1% R0402
GND_PVPP_AB
GND_PVPP_AB
PVPP_CPU_ABC_L
PVPP_CPU_ABC
C296 22uF 10V C0603
C596 22uF 10V C0603
C614 22uF 10V C0603
C600 22uF 10V C0603
C604 22uF 10V C0603
C294 0.1uF 25V C0402
C660 330uF TC-3P5X2P8X1P9M-1
F=400kHz
Vout=0.6(1+R1/R2)=2.588V
R822 0 0603;SMD R0603
GND_PVPP_AB

PWR PVTT_CPU_ABC


0.6V/ 1.7A
PVTT_CPU_ABC
+V3P3A
Irms=1.7A
U33
VIN VLDOIN REFIN EN
VO VOSNS REFOUT PGOOD
GND PGND GND_PAD
10P,TPS51200DRCR,
QFN10F-3X3
PVDDQ_ABC_CPU
C283 22uF 6.3V C0603
C287 22uF 6.3V C0603
PVDDQ_ABC_CPU
R426 10K R0402
R425 10K R0402
C277 0.001uF C0402 16V
[13,38,40] PWRGD_PVDDQ_ABC_CPU
3.6V>EN>1.7V
C291 22uF 6.3V C0603
C297 22uF 6.3V C0603
VREFOUT_AB
C293 0.1uF 25V C0402
PWRGD_PVTT_CPU_ABC
R444 100K R0402
+V3P3A
C282 4.7uF 16V C0603

<Core Design>

AAEON Technology INC.
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PWR PVNN_PCH/ P1V05_1

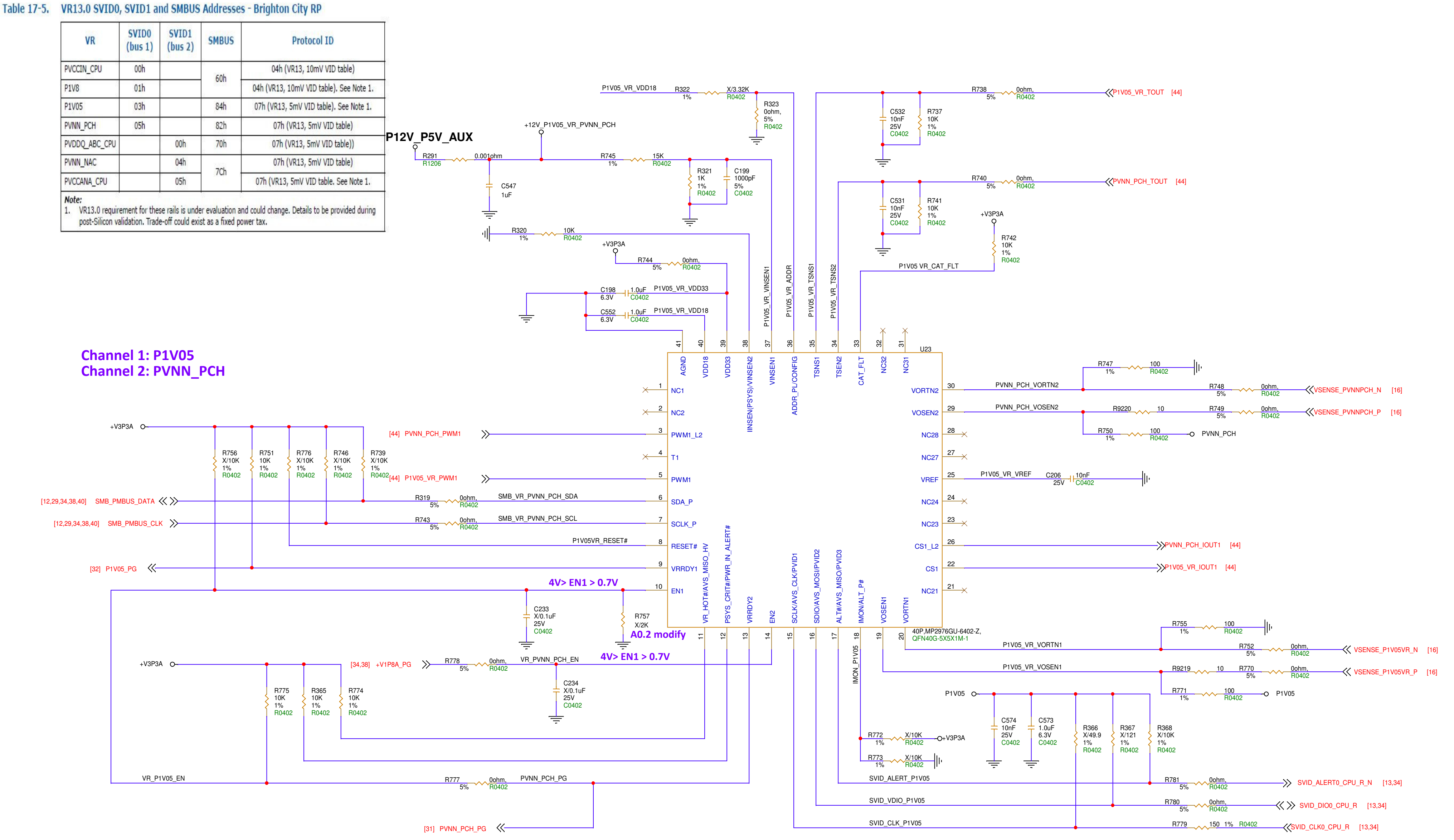

Table 17-5. VR13.0 SVID0, SVID1 and SMBUS Addresses - Brighton City RP

VR	SVID0 (bus 1)	SVID1 (bus 2)	SMBUS	Protocol ID
PVCCIN_CPU	00h		60h	04h (VR13, 10mV VID table)
P1V8	01h			04h (VR13, 10mV VID table). See Note 1.
P1V05	03h		84h	07h (VR13, 5mV VID table). See Note 1.
PVNN_PCH	05h		82h	07h (VR13, 5mV VID table)
PVDDQ_ABC_CPU		00h	70h	07h (VR13, 5mV VID table))
PVNN_NAC		04h	7Ch	07h (VR13, 5mV VID table)
PVCCANA_CPU		05h		07h (VR13, 5mV VID table. See Note 1.

Note:
1. VR13.0 requirement for these rails is under evaluation and could change. Details to be provided during post-Silicon validation. Trade-off could exist as a fixed power tax.

Channel 1: P1V05
Channel 2: PVNN_PCH

4V> EN1 > 0.7V

A0.2 modify

P12V_P5V_AUX
R291
R1206
0.001ohm
C547
1uF
+12V_P1V05_VR_PVNN_PCH
R745
1%
15K
R0402
R321
1K
1%
R0402
C199
1000pF
5%
C0402
P1V05_VR_VDD18
R322
1%
X/3.32K
R0402
R323
0ohm,
5%
R0402
R320
1%
10K
R0402
+V3P3A
R744
5%
0ohm,
R0402
C198
6.3V
1.0uF
C0402
P1V05_VR_VDD33
C552
6.3V
1.0uF
C0402
P1V05_VR_VDD18
P1V05_VR_VINSEN1
P1V05_VR_ADDR
P1V05_VR_TSNS1
P1V05_VR_TSNS2
R738
5%
0ohm,
R0402
P1V05_VR_TOUT [44]
C532
10nF
25V
C0402
R737
10K
1%
R0402
R740
5%
0ohm,
R0402
PVNN_PCH_TOUT [44]
C531
10nF
25V
C0402
R741
10K
1%
R0402
+V3P3A
R742
10K
1%
R0402
P1V05 VR_CAT_FLT
U23
41 AGND
40 VDD18
39 VDD33
38 IINSEN(PSYS)/VINSEN2
37 VINSEN1
36 ADDR_PL/CONFIG
35 TSNS1
34 TSEN2
33 CAT_FLT
32 NC32
31 NC31
1 NC1
2 NC2
3 PWM1_L2
4 T1
5 PWM1
6 SDA_P
7 SCLK_P
8 RESET#
9 VRRDY1
10 EN1
11 VR_HOT#/AVS_MISO_HV
12 PSYS_CRIT#/PWR_IN_ALERT#
13 VRRDY2
14 EN2
15 SCLK/AVS_CLK/PVID1
16 SDIO/AVS_MOSI/PVID2
17 ALT#/AVS_MISO/PVID3
18 IMON/ALT_P#
19 VOSEN1
20 VORTN1
30 VORTN2
29 VOSEN2
28 NC28
27 NC27
25 VREF
24 NC24
23 NC23
26 CS1_L2
22 CS1
21 NC21
40P,MP2976GU-6402-Z,
QFN40G-5X5X1M-1
R747
1%
100
R0402
PVNN_PCH_VORTN2
R748
5%
0ohm,
R0402
VSENSE_PVNPCH_N [16]
PVNN_PCH_VOSEN2
R9220
10
R749
5%
0ohm,
R0402
VSENSE_PVNNPCH_P [16]
R750
1%
100
R0402
PVNN_PCH
P1V05_VR_VREF
C206
25V
10nF
C0402
PVNN_PCH_IOUT1 [44]
P1V05_VR_IOUT1 [44]
+V3P3A
R756
X/10K
1%
R0402
R751
10K
1%
R0402
R776
X/10K
1%
R0402
R746
X/10K
1%
R0402
R739
X/10K
1%
R0402
[44] PVNN_PCH_PWM1
[44] P1V05_VR_PWM1
[12,29,34,38,40] SMB_PMBUS_DATA
R319
5%
0ohm,
R0402
SMB_VR_PVNN_PCH_SDA
[12,29,34,38,40] SMB_PMBUS_CLK
R743
5%
0ohm,
R0402
SMB_VR_PVNN_PCH_SCL
P1V05VR_RESET#
[32] P1V05_PG
C233
X/0.1uF
25V
C0402
R757
X/2K
+V3P3A
R775
10K
1%
R0402
R365
10K
1%
R0402
R774
10K
1%
R0402
[34,38] +V1P8A_PG
R778
5%
0ohm,
R0402
VR_PVNN_PCH_EN
C234
X/0.1uF
25V
C0402
VR_P1V05_EN
R777
5%
0ohm,
R0402
PVNN_PCH_PG
[31] PVNN_PCH_PG
IMON_P1V05
R755
1%
100
R0402
P1V05_VR_VORTN1
R752
5%
0ohm,
R0402
VSENSE_P1V05VR_N [16]
P1V05_VR_VOSEN1
R9219
10
R770
5%
0ohm,
R0402
VSENSE_P1V05VR_P [16]
R771
1%
100
R0402
P1V05
P1V05
C574
10nF
25V
C0402
C573
1.0uF
6.3V
C0402
R366
X/49.9
1%
R0402
R367
X/121
1%
R0402
R368
X/10K
1%
R0402
R772
1%
X/10K
R0402
+V3P3A
R773
1%
X/10K
R0402
SVID_ALERT_P1V05
R781
5%
0ohm,
R0402
SVID_ALERT0_CPU_R_N [13,34]
SVID_VDIO_P1V05
R780
5%
0ohm,
R0402
SVID_DIO0_CPU_R [13,34]
SVID_CLK_P1V05
R779
150 1% R0402
SVID_CLK0_CPU_R [13,34]

	P1V05 VR/800KHz	PVNN PCH/800KHz
TDC	7.8A	7A
IccMax	10.2A	7.4A
Vboot	1.05V	0.8V
Load Line	0mohm	0mohm
SVID Address	03h, SVID0 Bus #1	05h, SVID0 Bus #1

<Core Design>

AAEON Technology INC.	
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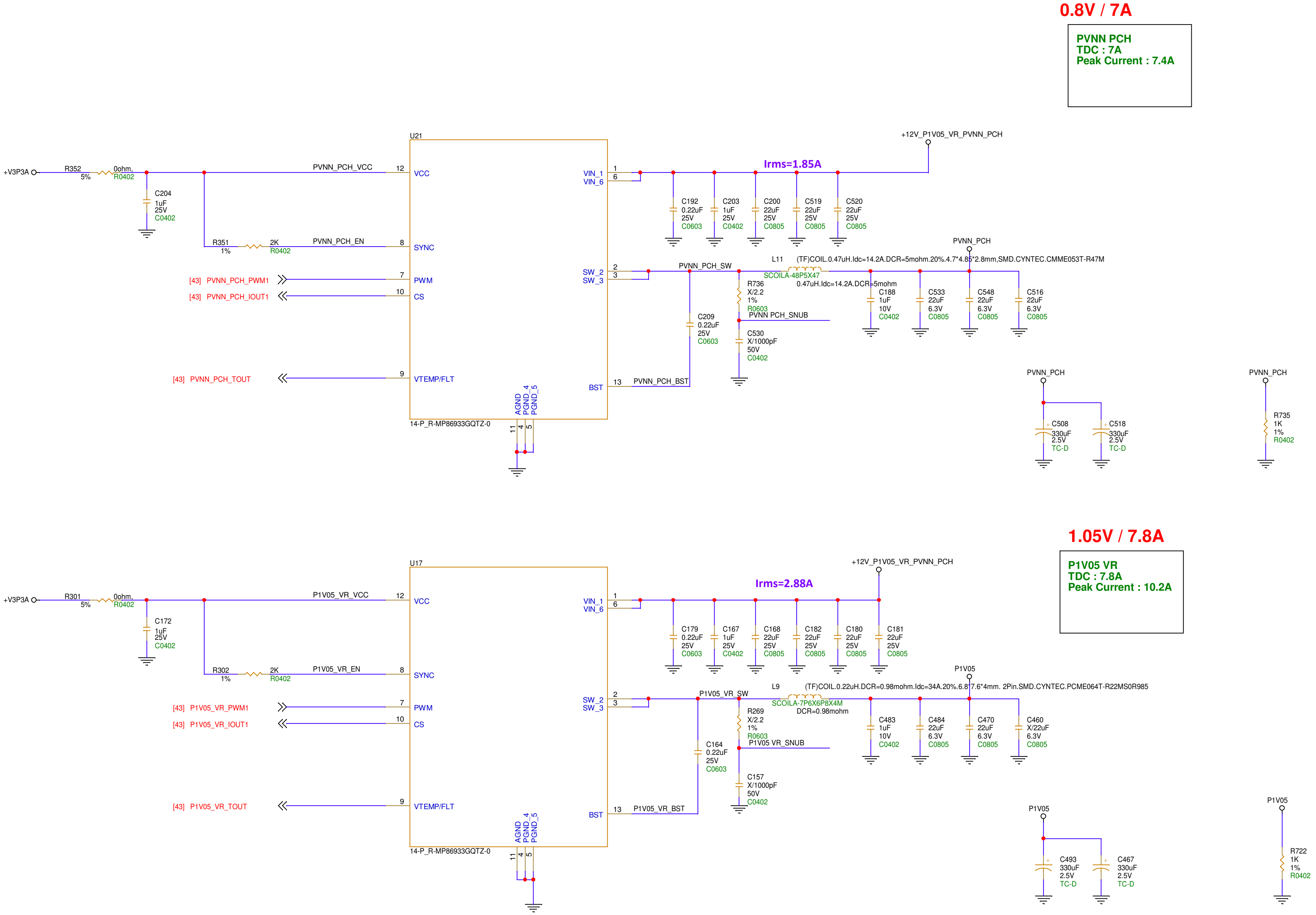
PWR PVNN_PCH/ P1V05_2


0.8V / 7A
PVNN PCH
TDC : 7A
Peak Current : 7.4A
U21
+V3P3A
R352
0ohm,
5%
R0402
C204
1uF
25V
C0402
PVNN_PCH_VCC
12
VCC
R351
2K
1%
R0402
PVNN_PCH_EN
8
SYNC
[43] PVNN_PCH_PWM1
7
PWM
[43] PVNN_PCH_IOUT1
10
CS
[43] PVNN_PCH_TOUT
9
VTEMP/FLT
AGND
PGND_4
PGND_5
11
4
5
14-P_R-MP86933GQTZ-0
VIN_1
VIN_6
1
6
Irms=1.85A
+12V_P1V05_VR_PVNN_PCH
C192
0.22uF
25V
C0603
C203
1uF
25V
C0402
C200
22uF
25V
C0805
C519
22uF
25V
C0805
C520
22uF
25V
C0805
SW_2
SW_3
2
3
PVNN_PCH_SW
L11
(TF)COIL.0.47uH.Idc=14.2A.DCR=5mohm.20%.4.7*4.85*2.8mm,SMD.CYNTEC.CMME053T-R47M
SCOILA-48P5X47
0.47uH.Idc=14.2A.DCR=5mohm
PVNN_PCH
R736
X/2.2
1%
R0603
PVNN PCH_SNUB
C530
X/1000pF
50V
C0402
C209
0.22uF
25V
C0603
C188
1uF
10V
C0402
C533
22uF
6.3V
C0805
C548
22uF
6.3V
C0805
C516
22uF
6.3V
C0805
BST
13
PVNN_PCH_BST
PVNN_PCH
C508
330uF
2.5V
TC-D
C518
330uF
2.5V
TC-D
PVNN_PCH
R735
1K
1%
R0402
1.05V / 7.8A
P1V05 VR
TDC : 7.8A
Peak Current : 10.2A
U17
+V3P3A
R301
0ohm,
5%
R0402
C172
1uF
25V
C0402
P1V05_VR_VCC
12
VCC
R302
2K
1%
R0402
P1V05_VR_EN
8
SYNC
[43] P1V05_VR_PWM1
7
PWM
[43] P1V05_VR_IOUT1
10
CS
[43] P1V05_VR_TOUT
9
VTEMP/FLT
AGND
PGND_4
PGND_5
11
4
5
14-P_R-MP86933GQTZ-0
VIN_1
VIN_6
1
6
Irms=2.88A
+12V_P1V05_VR_PVNN_PCH
C179
0.22uF
25V
C0603
C167
1uF
25V
C0402
C168
22uF
25V
C0805
C182
22uF
25V
C0805
C180
22uF
25V
C0805
C181
22uF
25V
C0805
SW_2
SW_3
2
3
P1V05_VR_SW
L9
(TF)COIL.0.22uH.DCR=0.98mohm.Idc=34A.20%.6.8*7.6*4mm. 2Pin.SMD.CYNTEC.PCME064T-R22MS0R985
SCOILA-7P6X6P8X4M
DCR=0.98mohm
P1V05
R269
X/2.2
1%
R0603
P1V05 VR_SNUB
C157
X/1000pF
50V
C0402
C164
0.22uF
25V
C0603
C483
1uF
10V
C0402
C484
22uF
6.3V
C0805
C470
22uF
6.3V
C0805
C460
X/22uF
6.3V
C0805
BST
13
P1V05_VR_BST
P1V05
C493
330uF
2.5V
TC-D
C467
330uF
2.5V
TC-D
P1V05
R722
1K
1%
R0402

<Core Design>

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PWR PVNN_PCH/ P1V05_2

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Revision History

01. Project code: E210809
02. Model name: COM-ICDB7
03. Model revision: A0.3_0_0
04. 96-Level: 9697ICD709
05. PCB 料號: 1907ICD702
06. PCB 厚度: 2.0 mm
07. PCB 層數: 14 Layer
08. 連板數量: 2 pcs
09. PCB VIA: HDI/2+10+2
10. Material: TU-883
11. PCB Dimension: 125x95mm

COM-ICDB7 A0.3_0_0 PCB: 1907ICD702 BOM: 9697ICD709~ Date: 2022/01/13

(TF)PCB.COM-ICDB7.Rev.A0.3_0_0.HDI.(2+10+2).14Layers.Green.1*1.125x95x2.0mm

(TF)ASS'Y.COM-ICDB7.Rev.A0.3_0_0.INTEL Icelake-D

BOM NUMBER	CPU	P/N
9697ICD709	D-1746TER	144X000246
9697ICD710	D-1732TE	144X000247
9697ICD711	D-1712TR	144X000248
9697ICD712	D-1735TR	144X000249
9697ICD713	D-1715TER	144X000250

Date	Revision	Page	Modification list	Reason
2020/9/27	A0.1_0_0	1-45	First Release	First Release
2021/7/14	A0.2_0_0	1-45	1. Add D21 for WDT# reset 2. Update SoC U14 symbol 3. Add NAC pull down resistor R10850~R10856 4. Modify LPC/eSPI mux function(U28) circuit 5. R705 un-mount 6. R679 mount for DCI 7. Change C582/C584 to 0.22uF for power sequence 8. Add CLK_100M_GEN4_DP/DN for PEG GEN4 clock to carrier board 9. C129 un-mount for FAN TAC 10. R471 net change to +V5_DUAL 11. R305/R711 un-mount for power sequence 12. Add R10858/R10869 for power sequence	Fix A0.1 bug.
20211210	A0.3_0_0	24	Reserve R74 and PM_RSMRST# for Power up at S3 fail issue	Reserve R74 and PM_RSMRST#.
20211214	A0.3_0_0	24	Add Net name LAN1_LED_LINK#	Add Net name LAN1_LED_LINK#
20211213	A0.3_0_0	26	Change P/N of SPI1 from 1463X00011 to 1463X00014 for EOL.	Change P/N of SPI1 from 1463X00011 to 1463X00014.
20211220	A0.3_0_0	27	remove R354 and R355.	remove R354 and R355.
20211222	A0.3_0_0	27	Change net name at SW1.1 from AutoBtn# to S3_S5_GATE	Change net name at SW1.1 from AutoBtn# to S3_S5_GATE by the function define by EC.
20220105	A0.3_0_0	27	remove U11, FB5, Place R187 to change Power rail to +3P3A	remove U11, FB5, Place R187 to change Power rail to +3P3A
20220111	A0.3_0_0	27	Add R206, R213, R222, R230 to LAN_LED2, 5, 8	Add R206, R213, R222, R230 to LAN_LED2, 5, 8 and 11 for 10G LAN active LED issue.
20211202	A0.3_0_0	29	Add PMBUS_DATA/CLK for Power team	Add PMBUS_DATA/CLK for Power team
20211210	A0.3_0_0	29	Change power at R463 from +V5S to +V3P3S.	Change power at R463 from +V5S to +V3P3S.
20211222	A0.3_0_0	30	1. Add C190 and C196 to soft starting +V5A1 for +V5_SBY ramp up issue. 2. Change FB6 to PSP2 to reduce spacing for layout.	1. Add C190 and C196 2. Change FB6 to PSP2
20211210	A0.3_0_0	31	Remove R9207, change net name of V3.3A_RSMRST# to PM_RSMRST#	Remove R9207, change net name of V3.3A_RSMRST# to PM_RSMRST#
20211210	A0.3_0_0	31	Change AND GATE from 3 input to 2 input for remove net of CB_PWRGD_PS.	Change AND GATE from 3 input to 2 input
20211210	A0.3_0_0	32	Change net name from CB_SLP_S3# to PWRGD_PS to meet the sequence of CRB.	Change net name from CB_SLP_S3# to PWRGD_PS
20211210	A0.3_0_0	32	Remove Q25 and the discharge circuits of +V3P3S and +V5S	Remove Q25 and the discharge circuits of +V3P3S and +V5S
20211210	A0.3_0_0	32	1. Add Q24B for +VIN_EXT discharge 2. Change R823 from 100R to 1.5K to meet resistor of 1/10W	1. Add Q24B for +VIN_EXT discharge 2. Change R823 from 100R to 1.5K to meet resistor of 1/10W
20211210	A0.3_0_0	32	Remove U26 and Power +V5S	Remove U26 and Power +V5S
20211207	A0.3_0_0	33	Remove R10858 and Place R10857 for boot up sequence issue.	Remove R10858 and Place R10857
20211210	A0.3_0_0	33	Add R75 and +VIN_EXT_RDY for Power up issue, to enable +V5A by +VIN_EXT ready.	Add R75 and +VIN_EXT_RDY
20220106	A0.3_0_0	34	Reserve R76 for Power team suggestion	Reserve R76
20220106	A0.3_0_0	34	Reserve R141 for Power team suggestion.	Reserve R141
20211207	A0.3_0_0	38	1. Change R519 from resistor (1206) to Short Pad (0603) to reduce the space. 2. Change Power source from +VIN_EXT to P12V_P5V_AUX for boot up sequence issue.	1. Change R519 from resistor (1206) to Short Pad (0603) 2. Change Power source from +VIN_EXT to P12V_P5V_AUX
20211209	A0.3_0_0	42	Remove R10869 and place R494 to meet sequence request.	Remove R10869 and place R494

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