

# PMC-H610 Block Diagram Rev 1.00

D

D

C

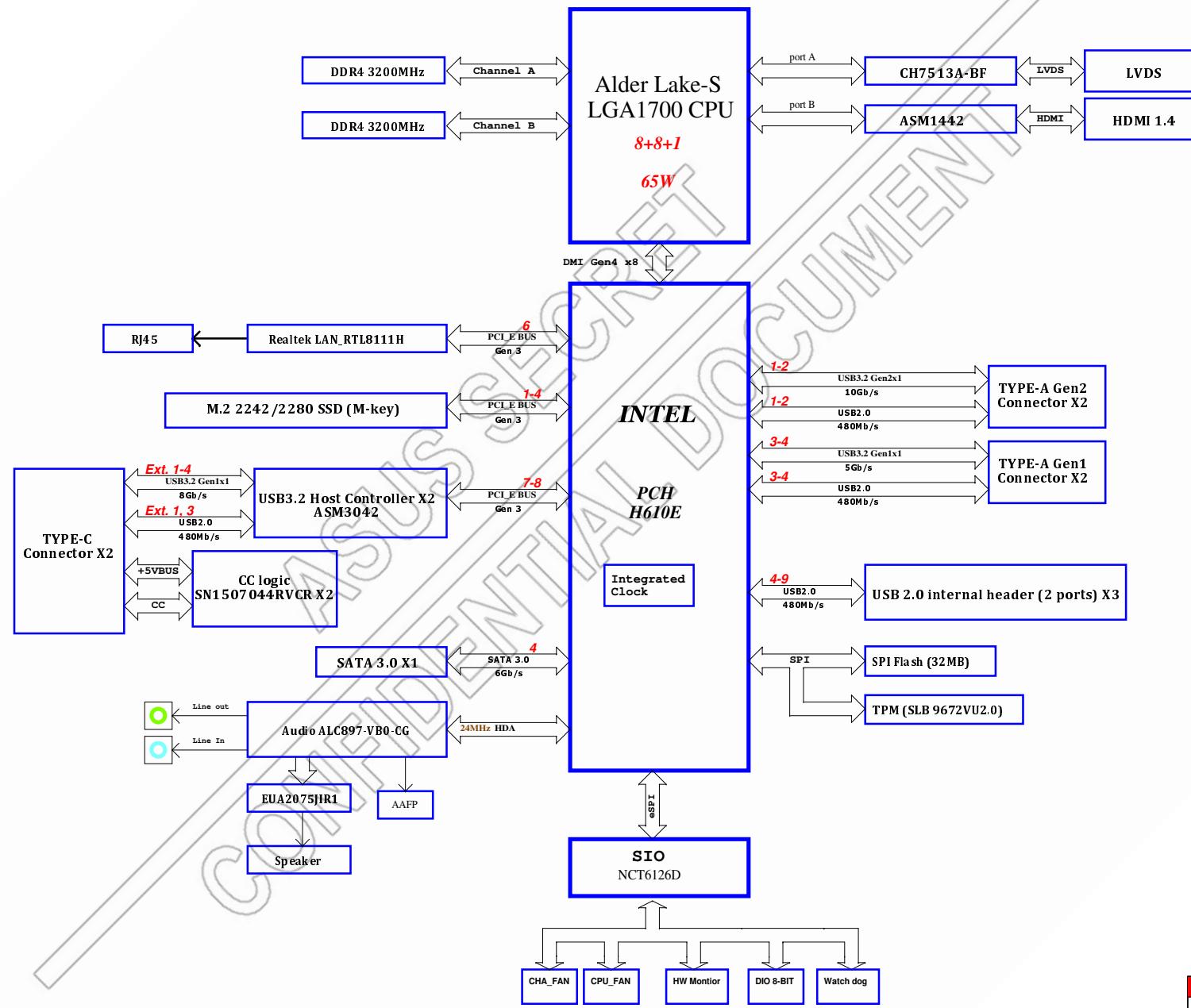
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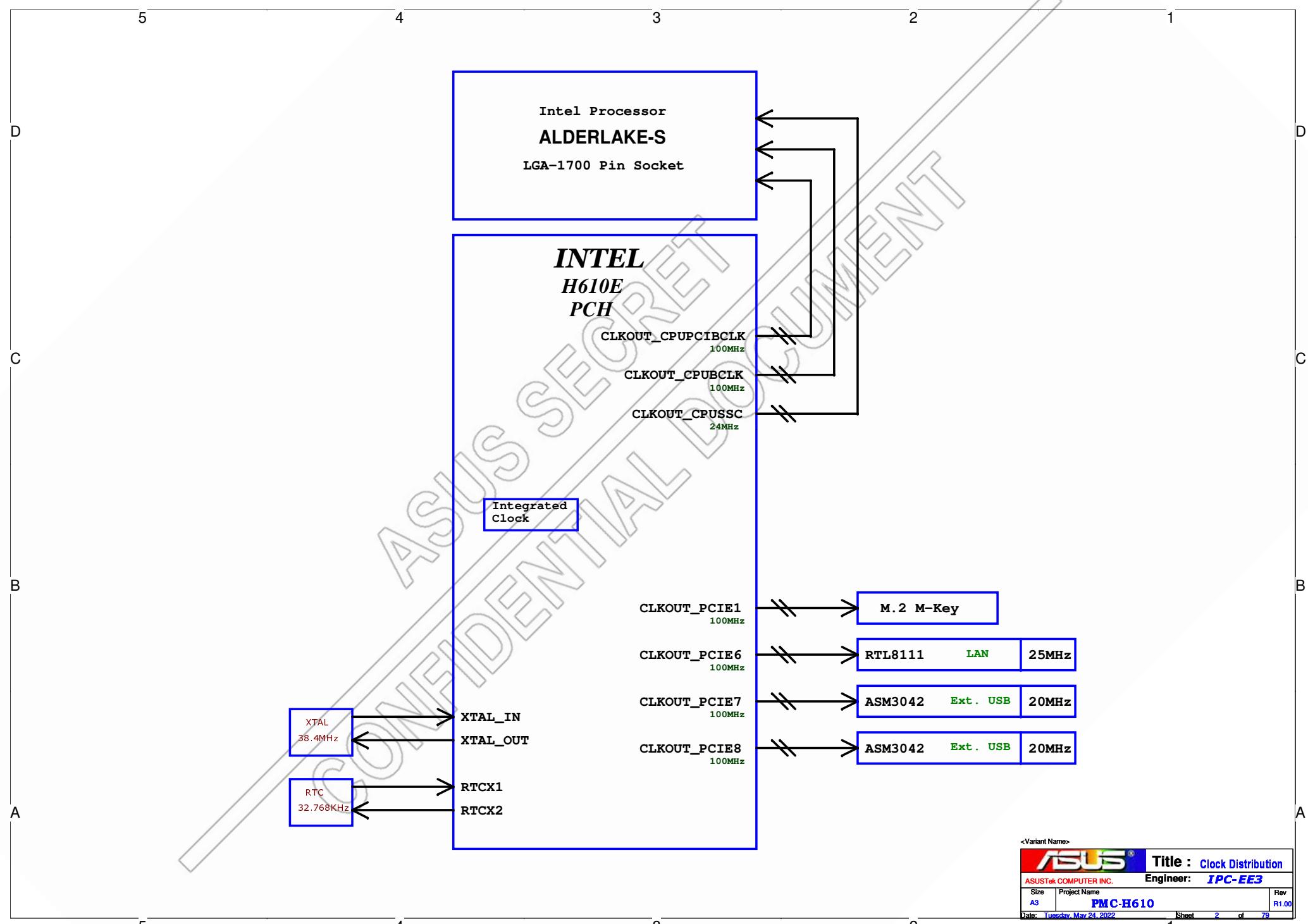
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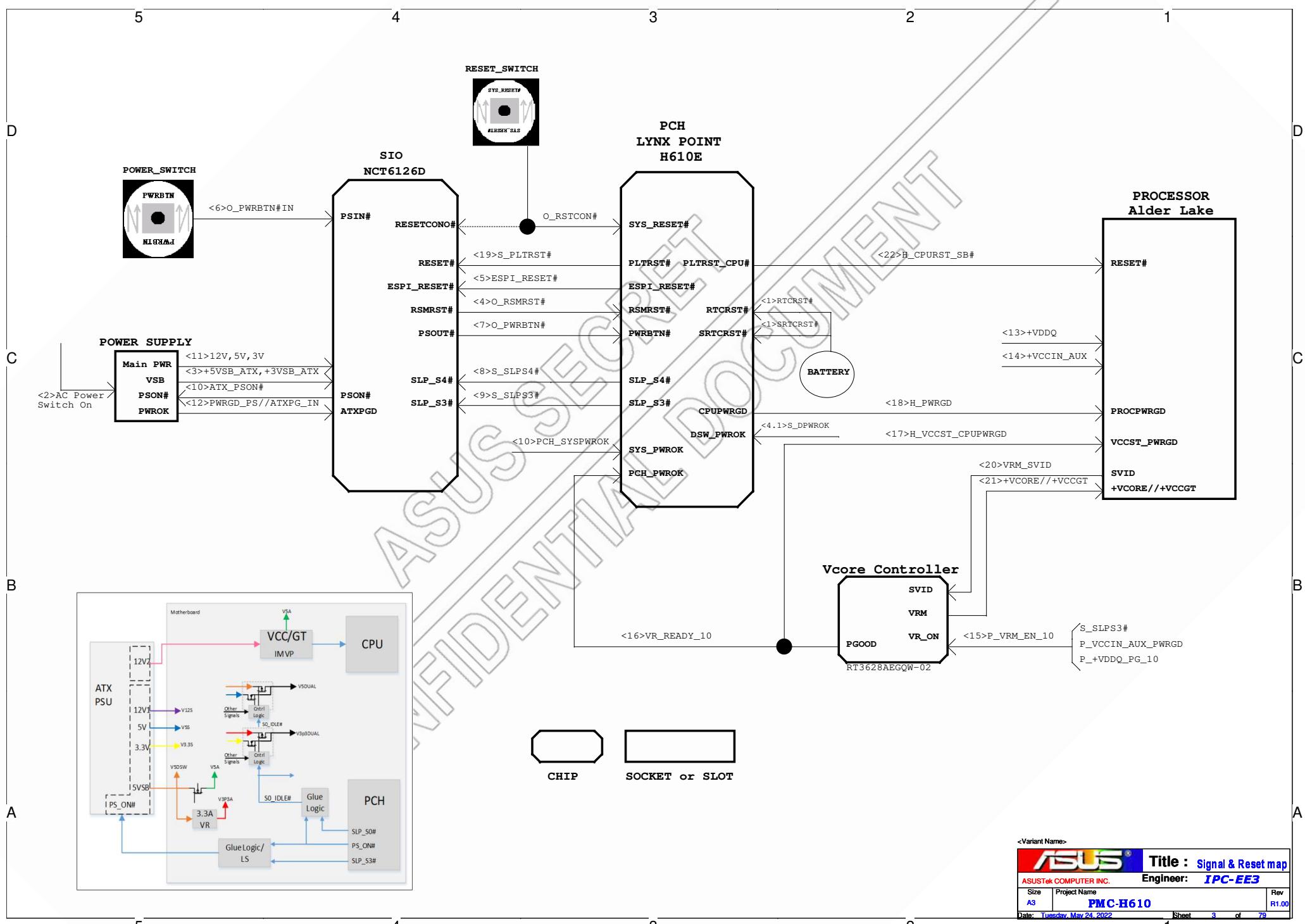
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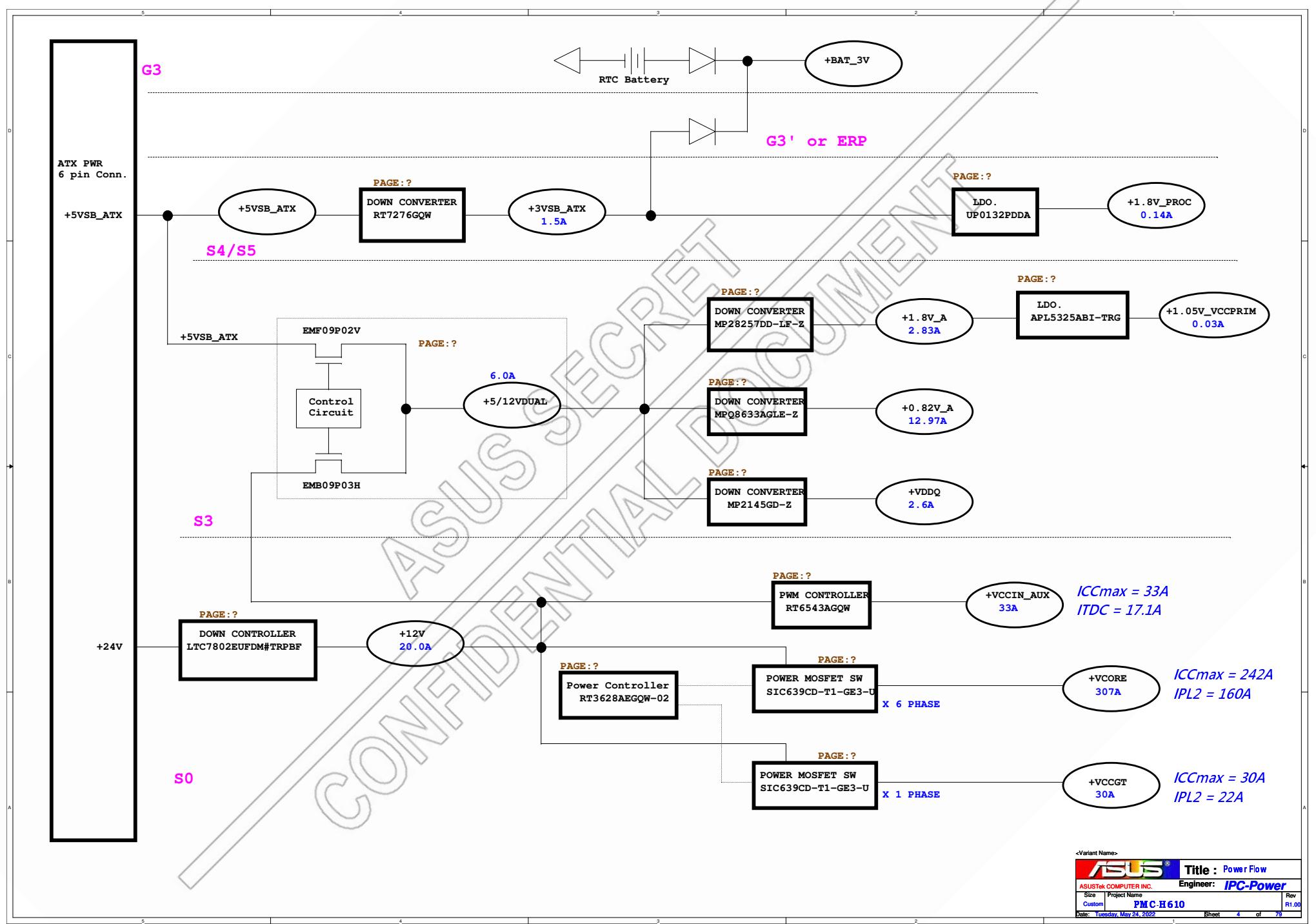
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A



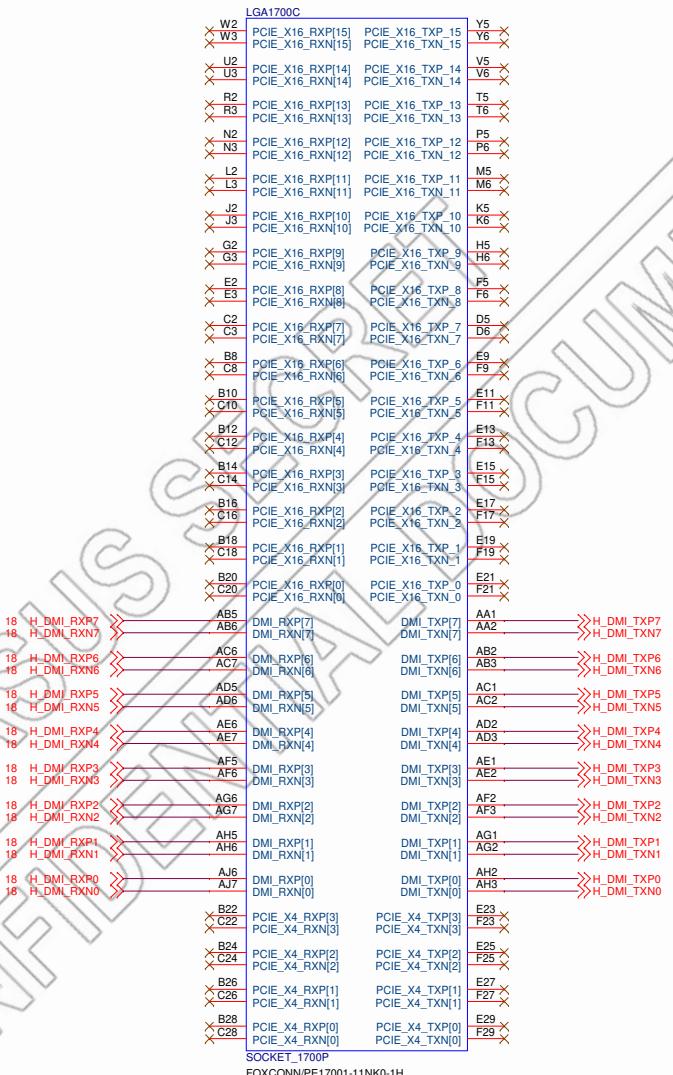






3

1



12001-00300300

LGA 1700P SOCKET G/F SMT

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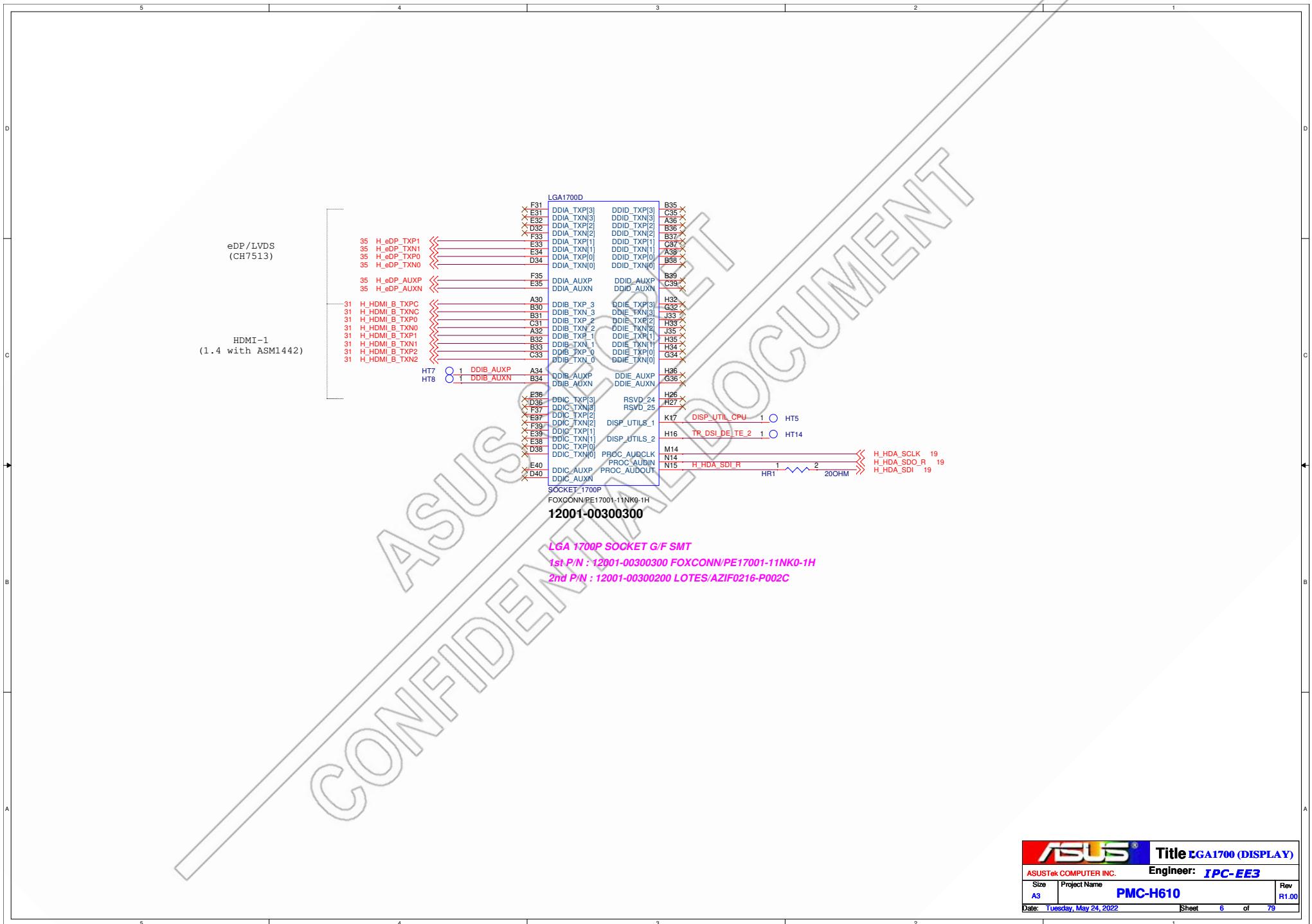
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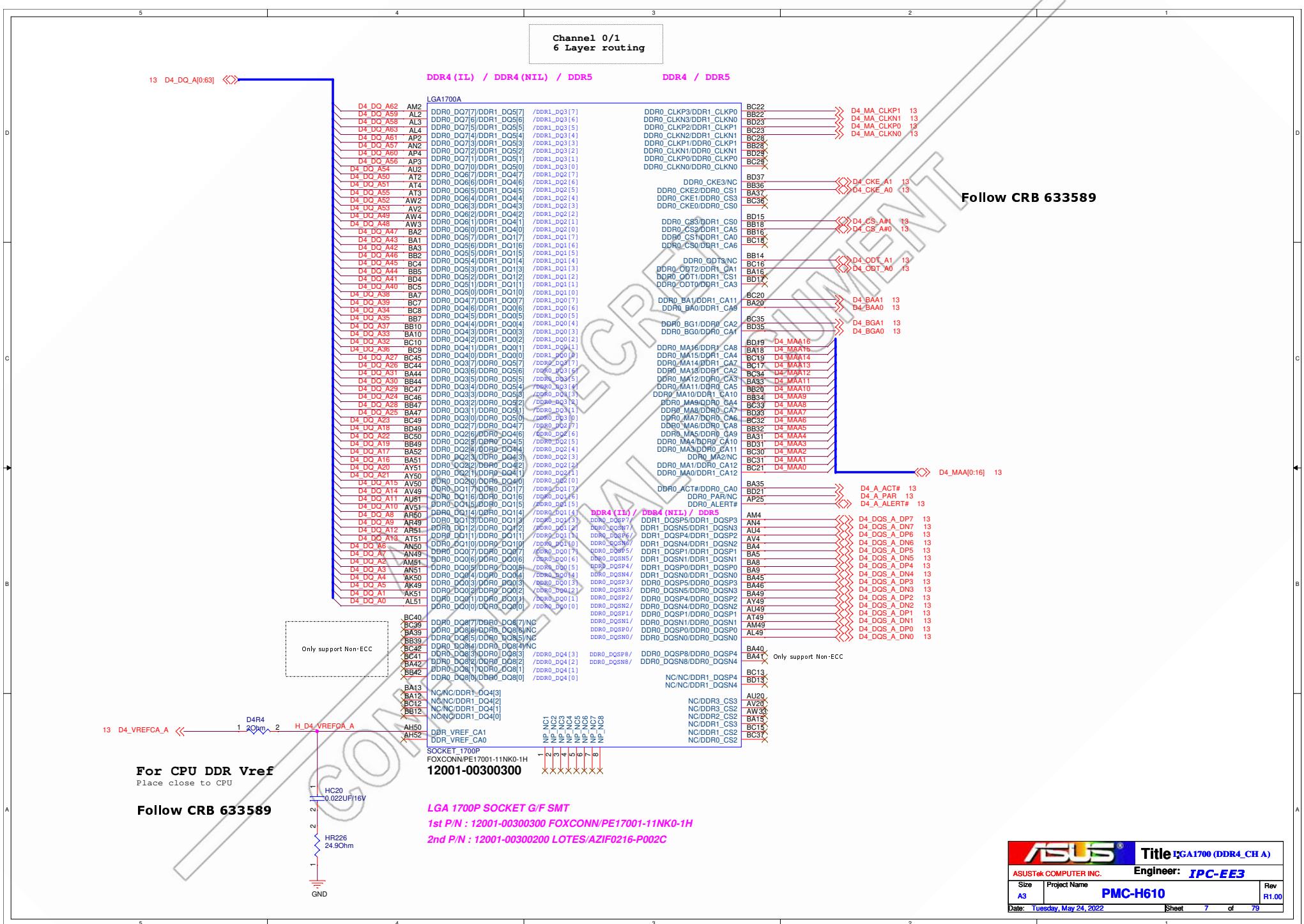


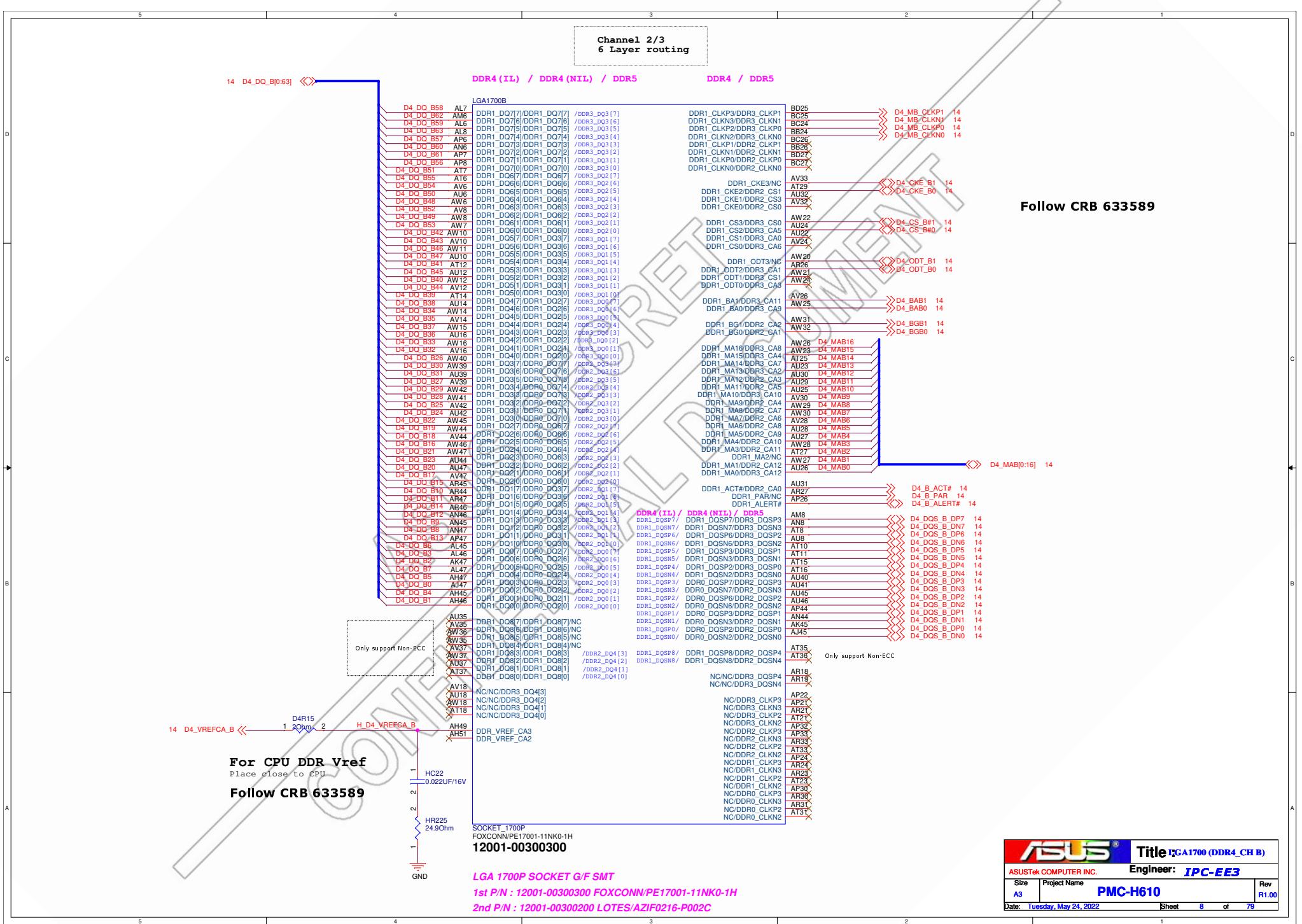
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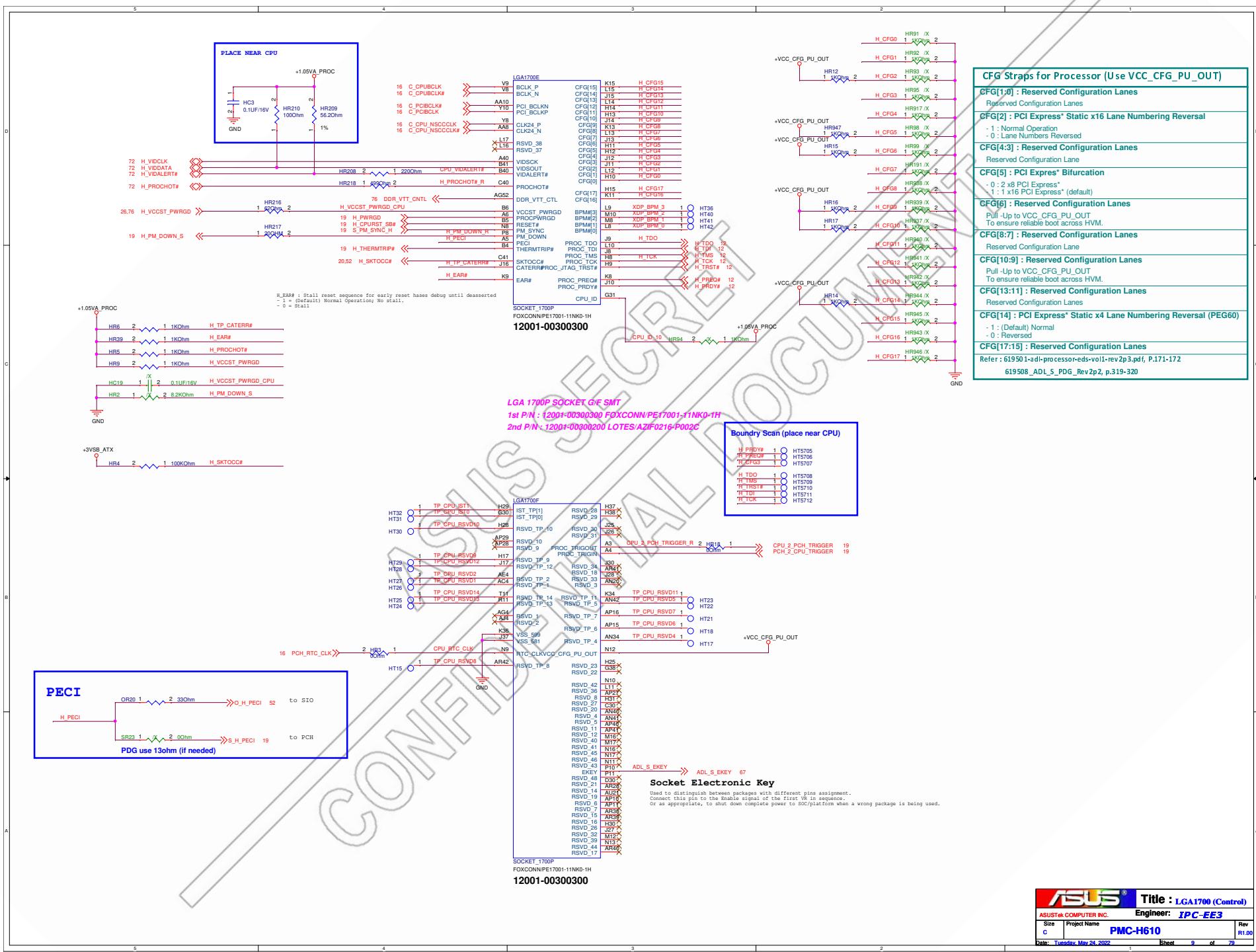
Engineer: **ESG E&C**

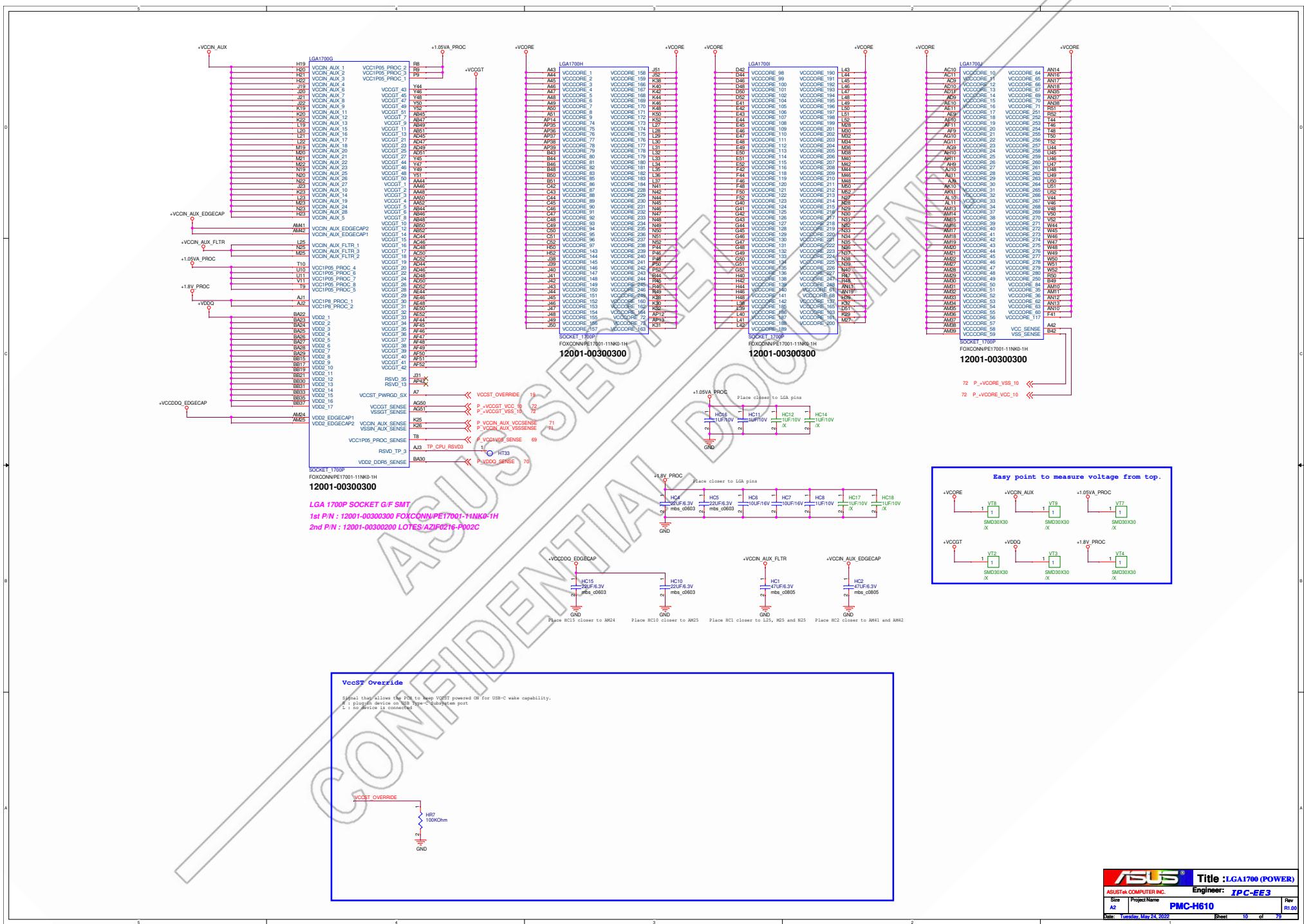
**ASUStek COMPUTER INC.**      Engineer: **IPC-EE3**  
 Size      Project Name      Rev  
**A3**      **PMC-H610**      **R1.00**  
 Date: **Tuesday, May 24, 2022**      Sheet **5** of **79**

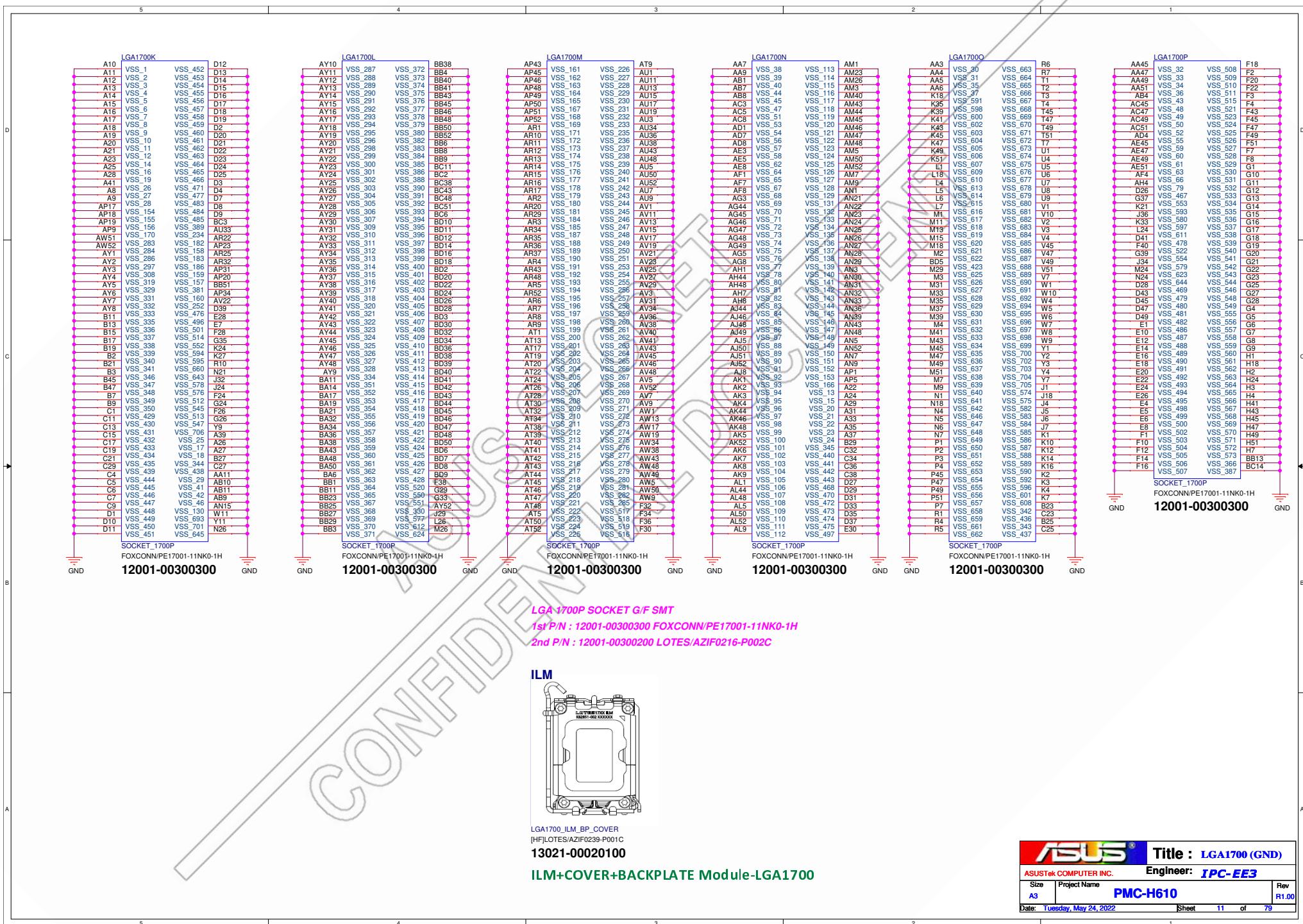


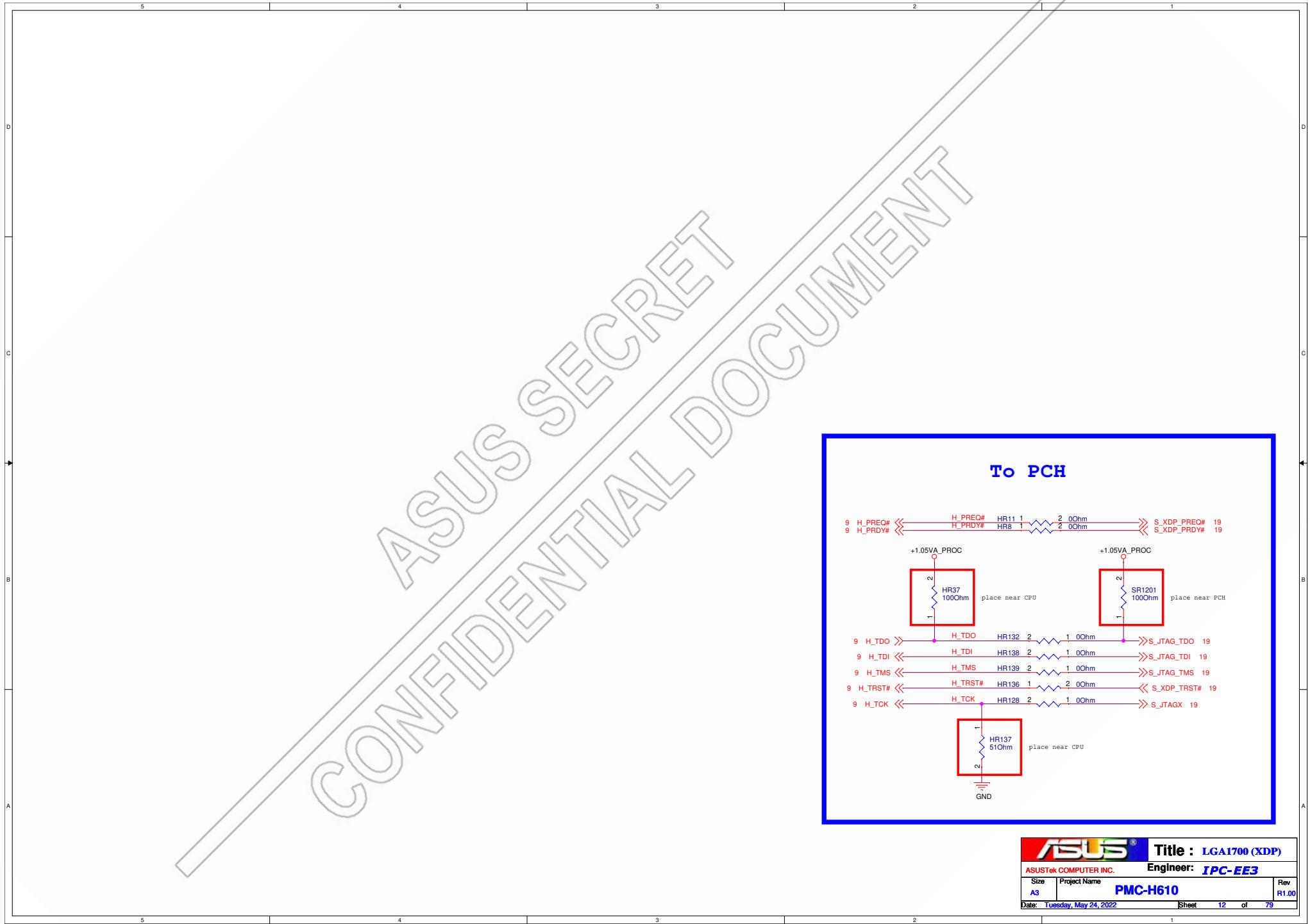


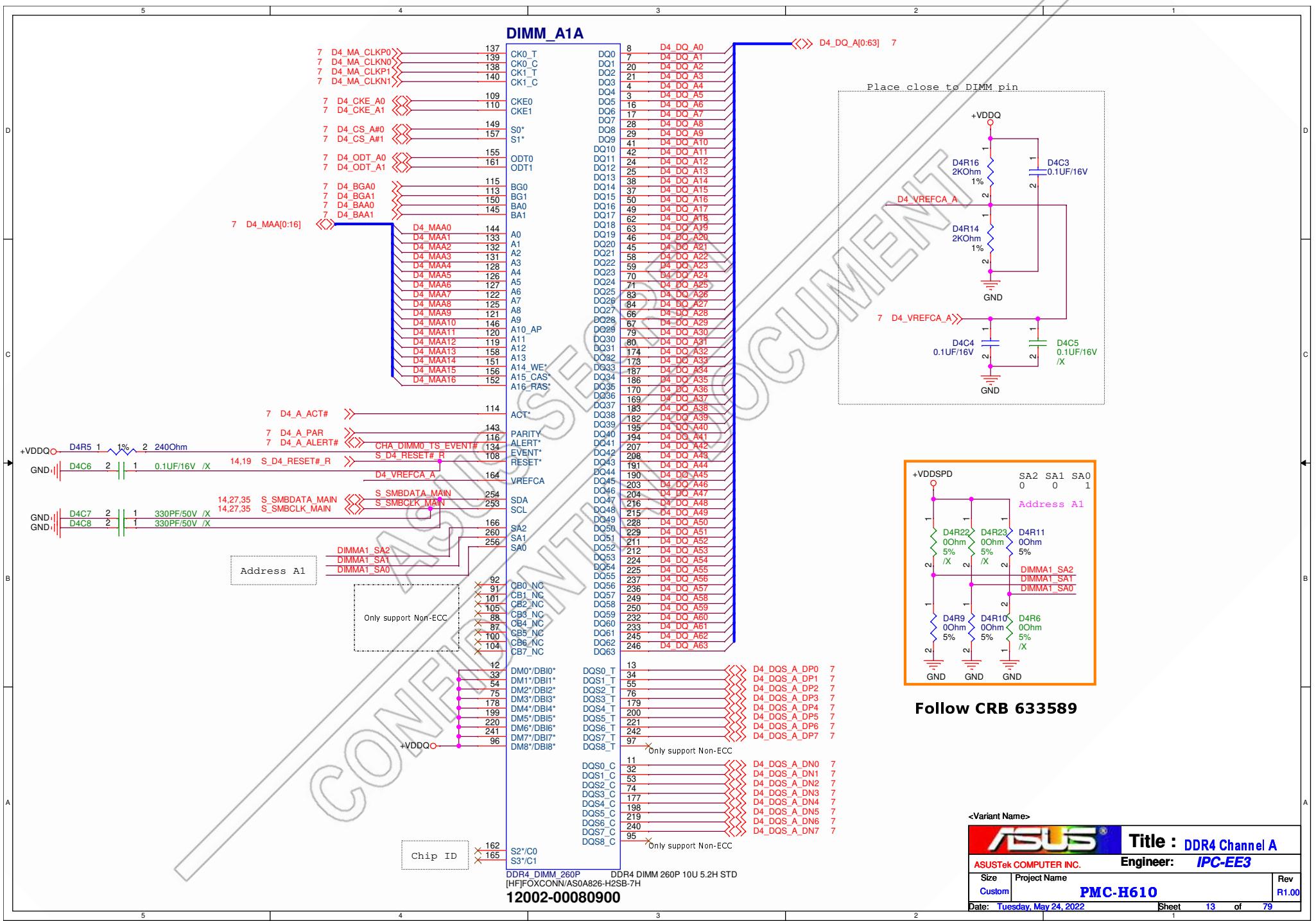


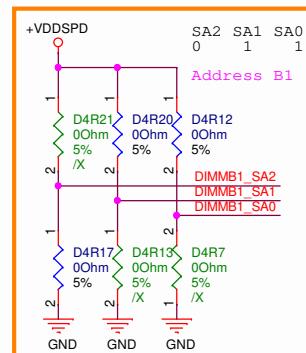
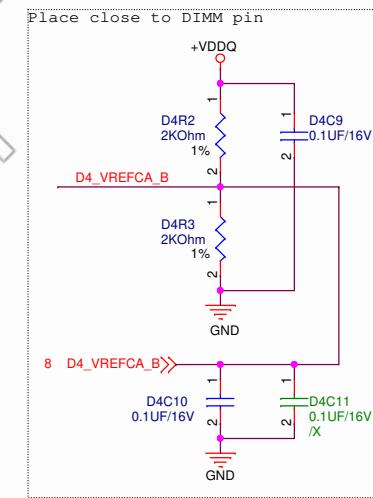
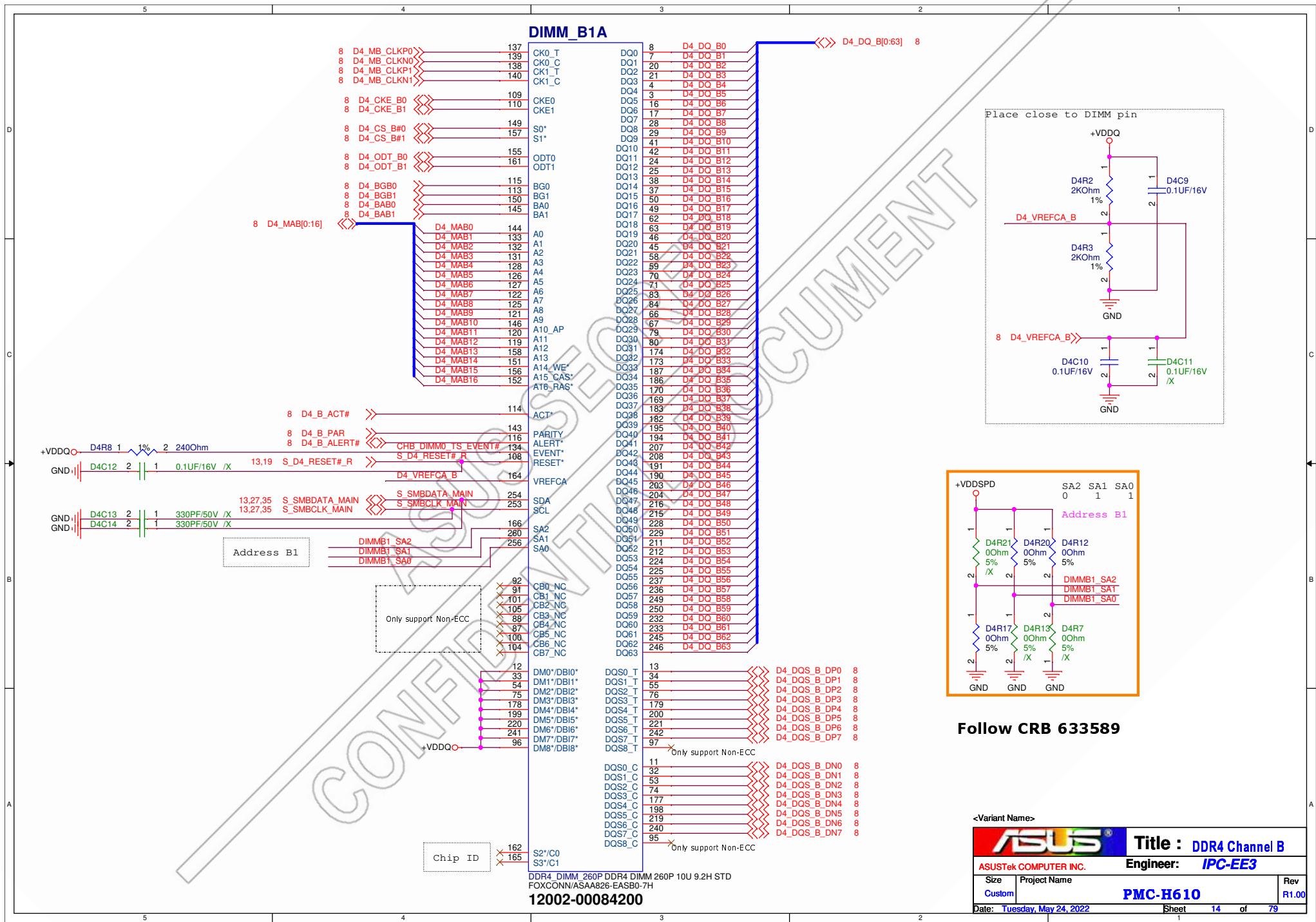












<Variant Name>



Title : DDR4 Channel B

Engineer: IPC-EE3

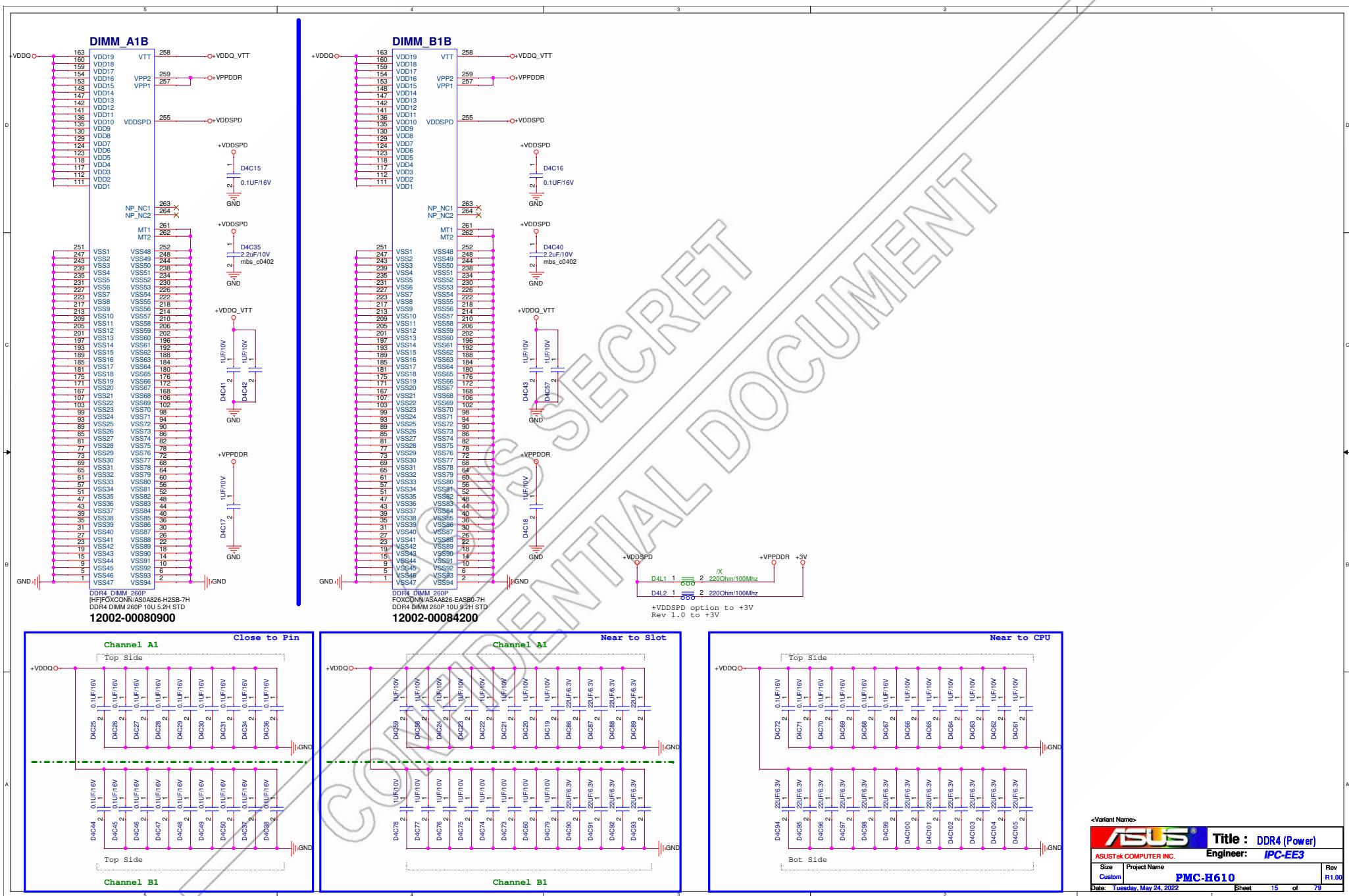
Size	Project Name	Rev
Custom		R1.00
	PMC-H610	

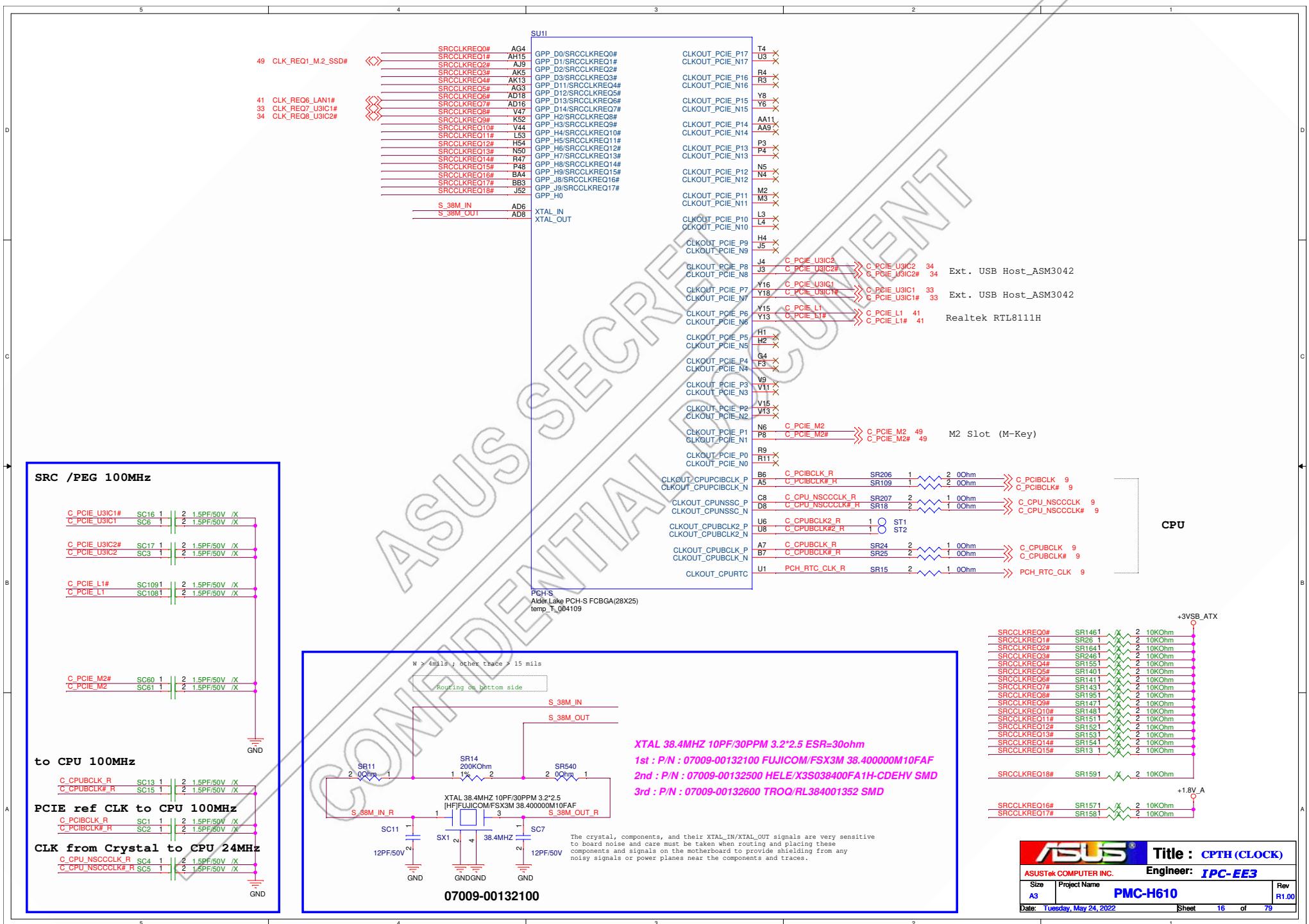
Date: Tuesday, May 24, 2022

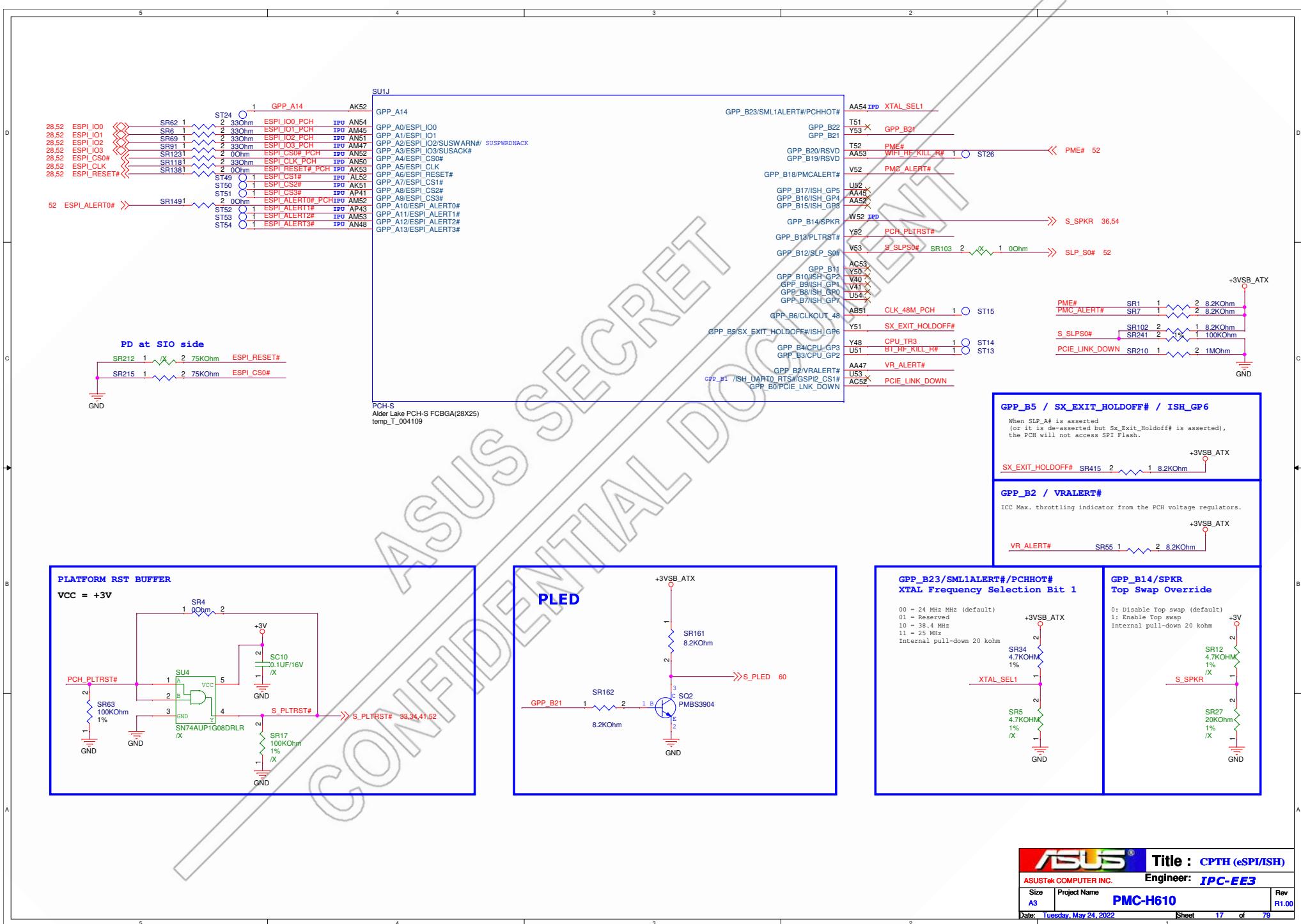
Sheet 14 of 79

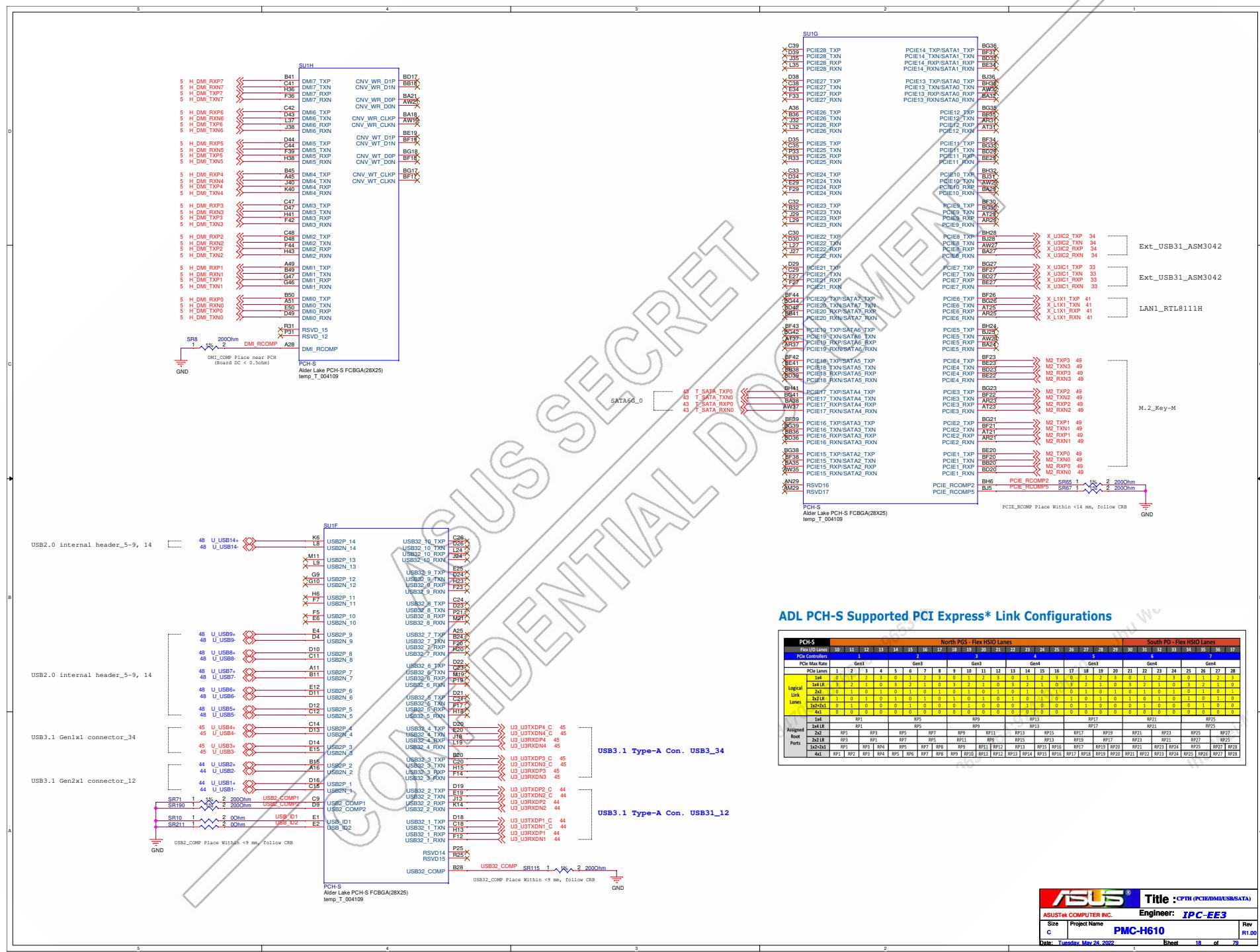
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FOXCONN/ASAA826-EASB0-7H

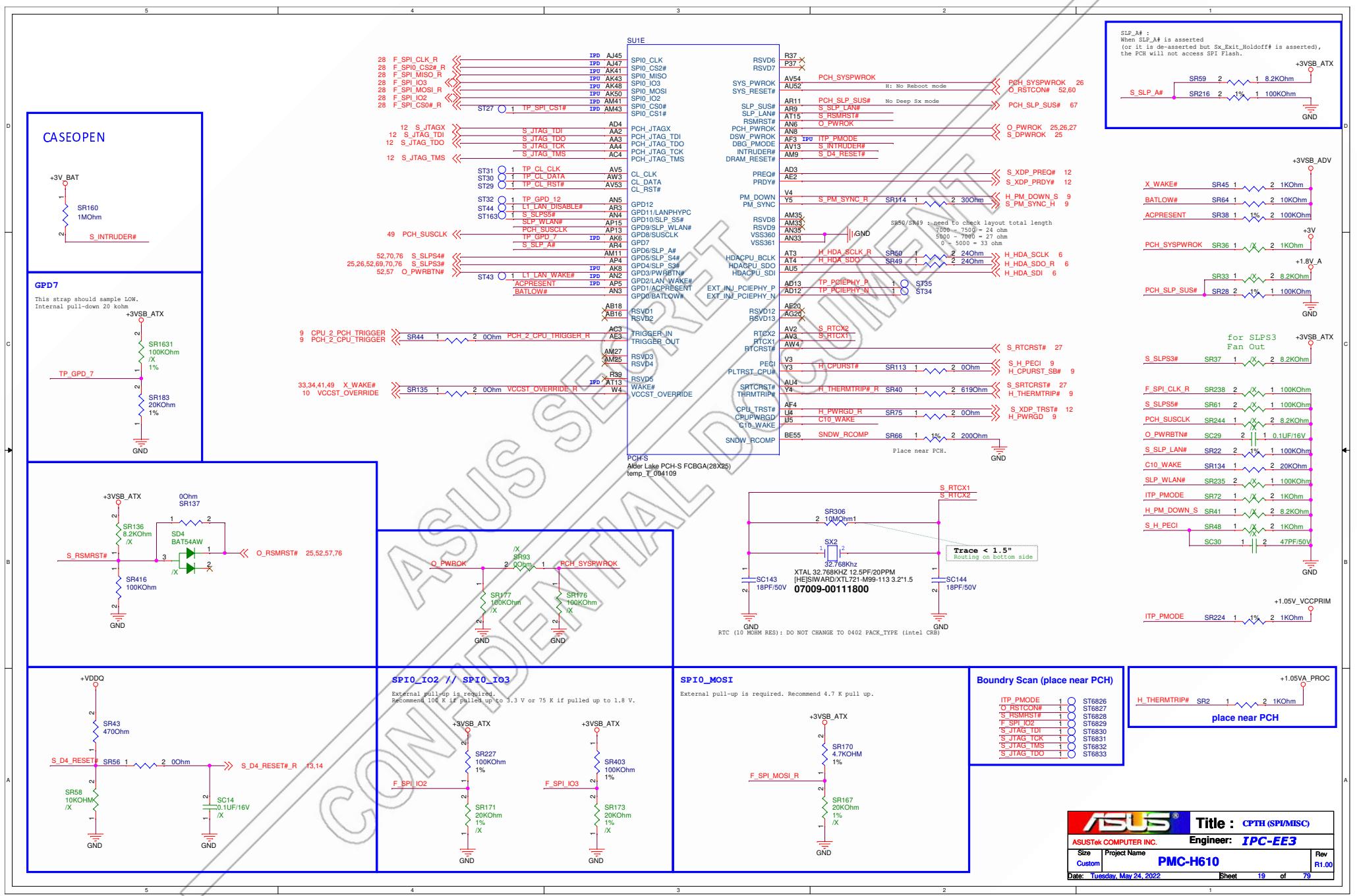
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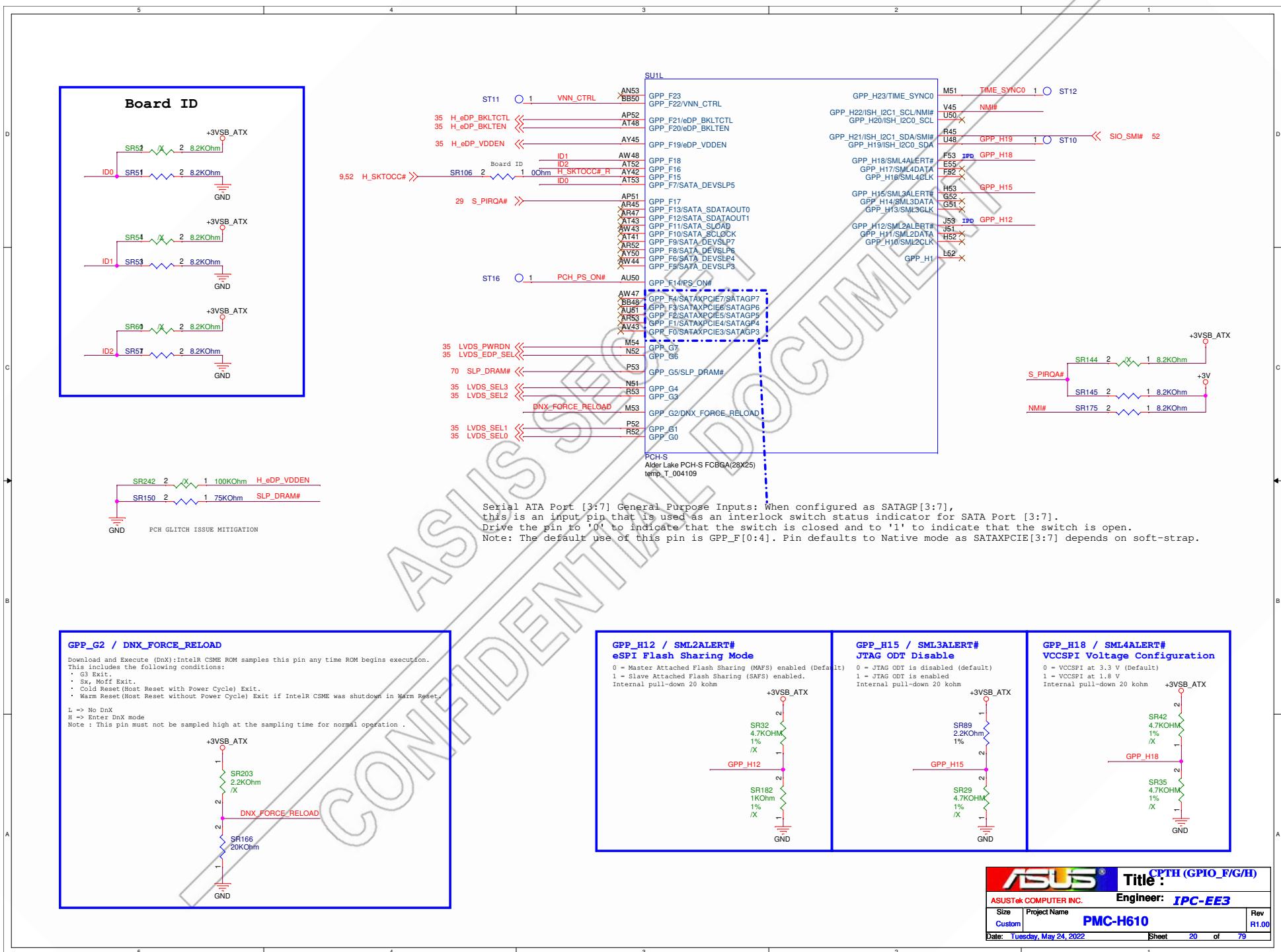








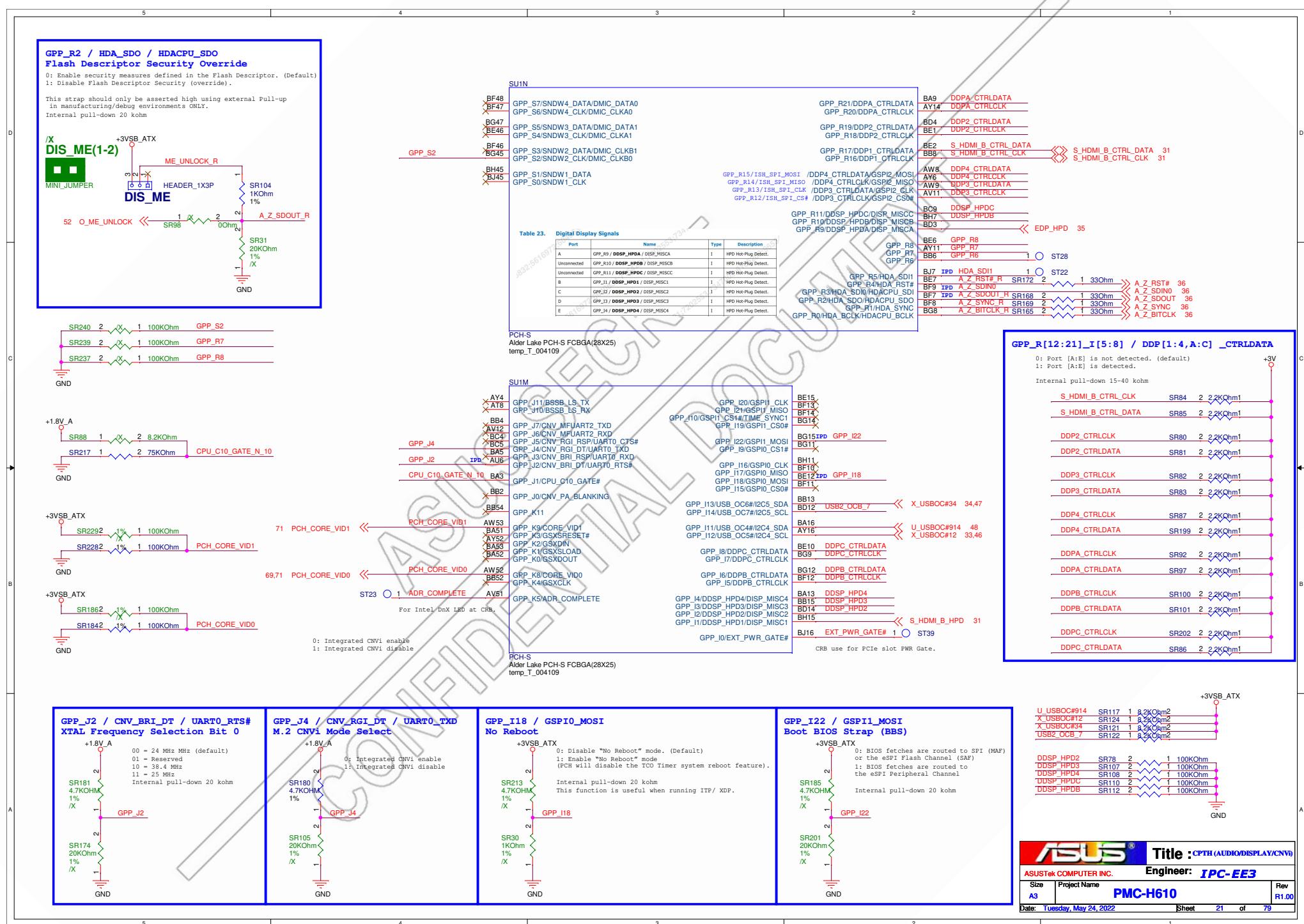


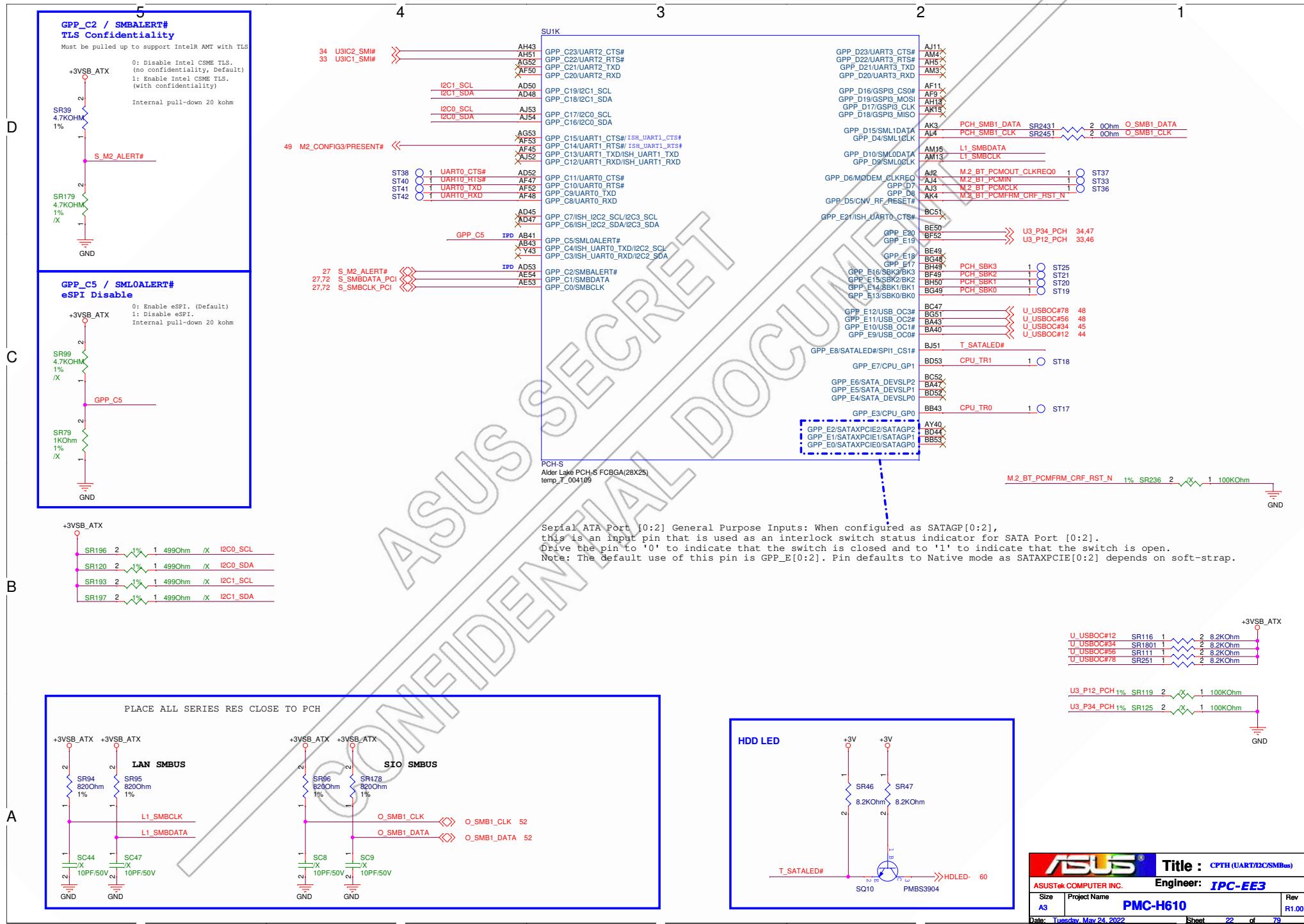


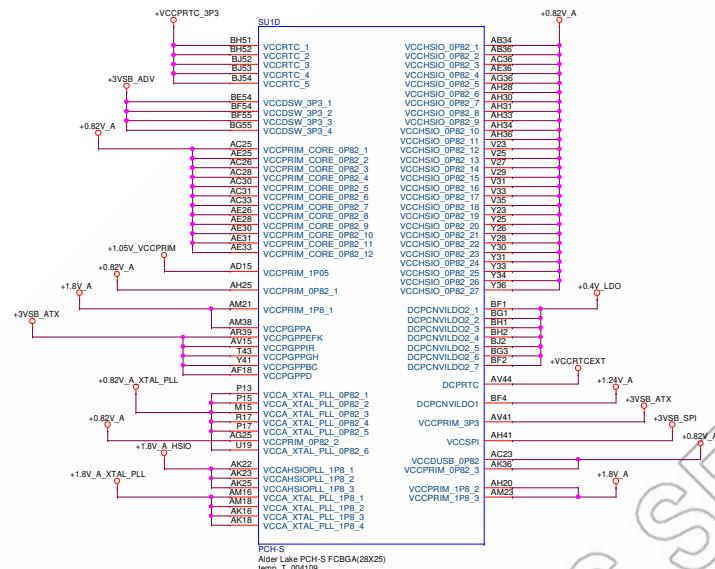
**CPTH (GPIO F/G/H)**

Engineer: **EBC EBC**

ASUSTek COMPUTER INC.		Engineer: <b>IPC-EE3</b>
Size Custom	Project Name <b>PMC-H610</b>	Rev R1.00
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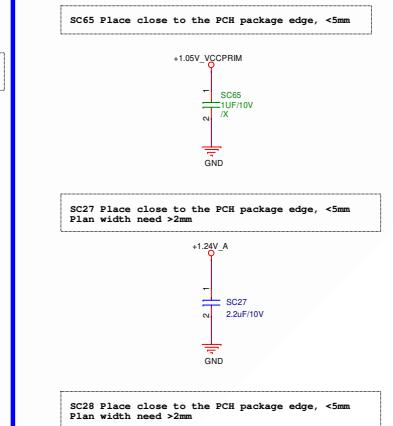
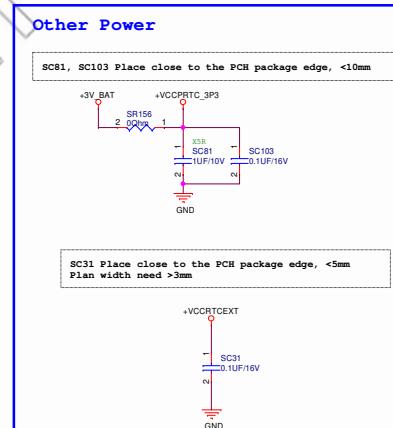




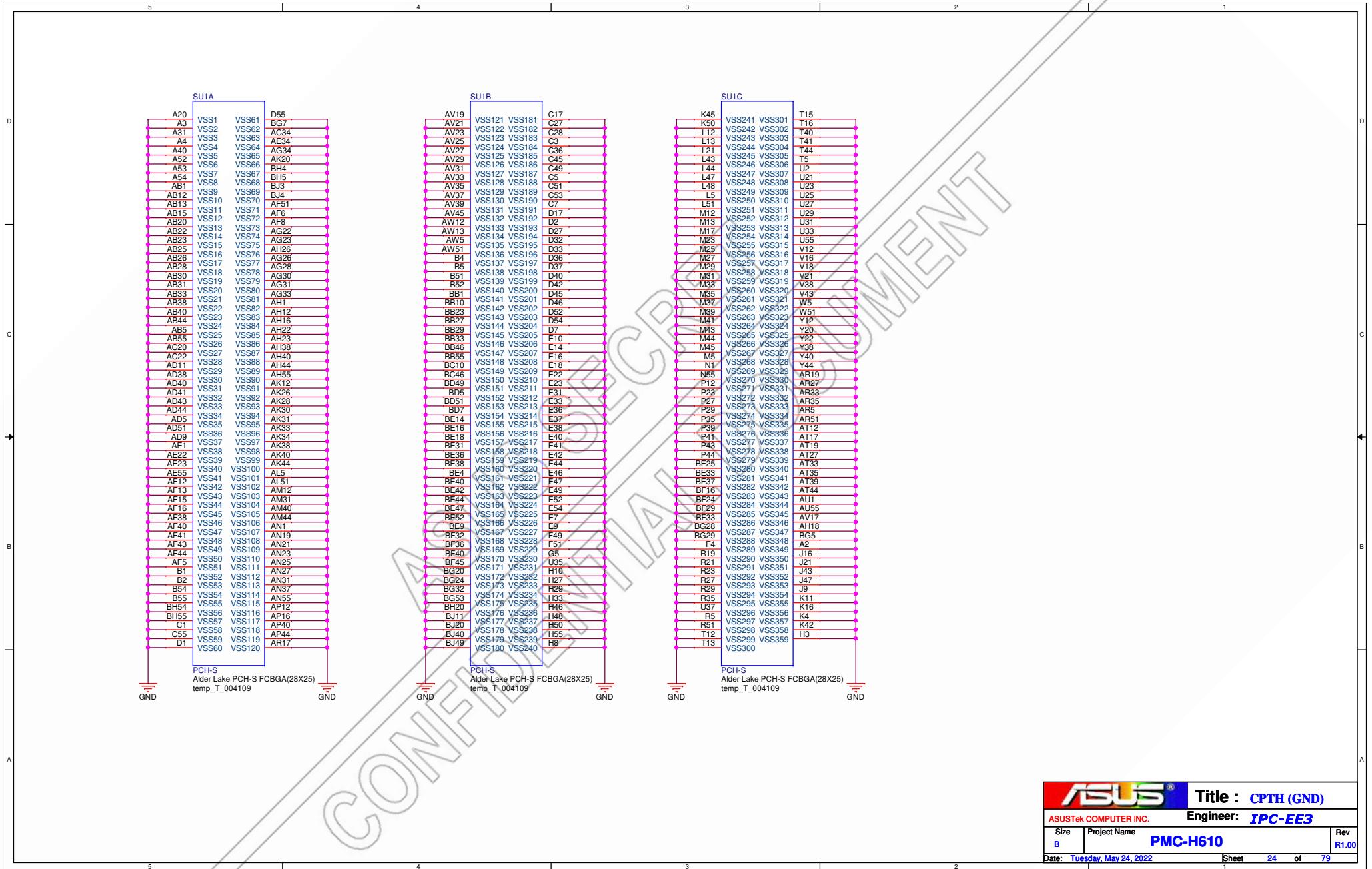


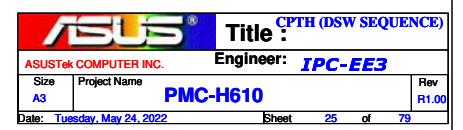
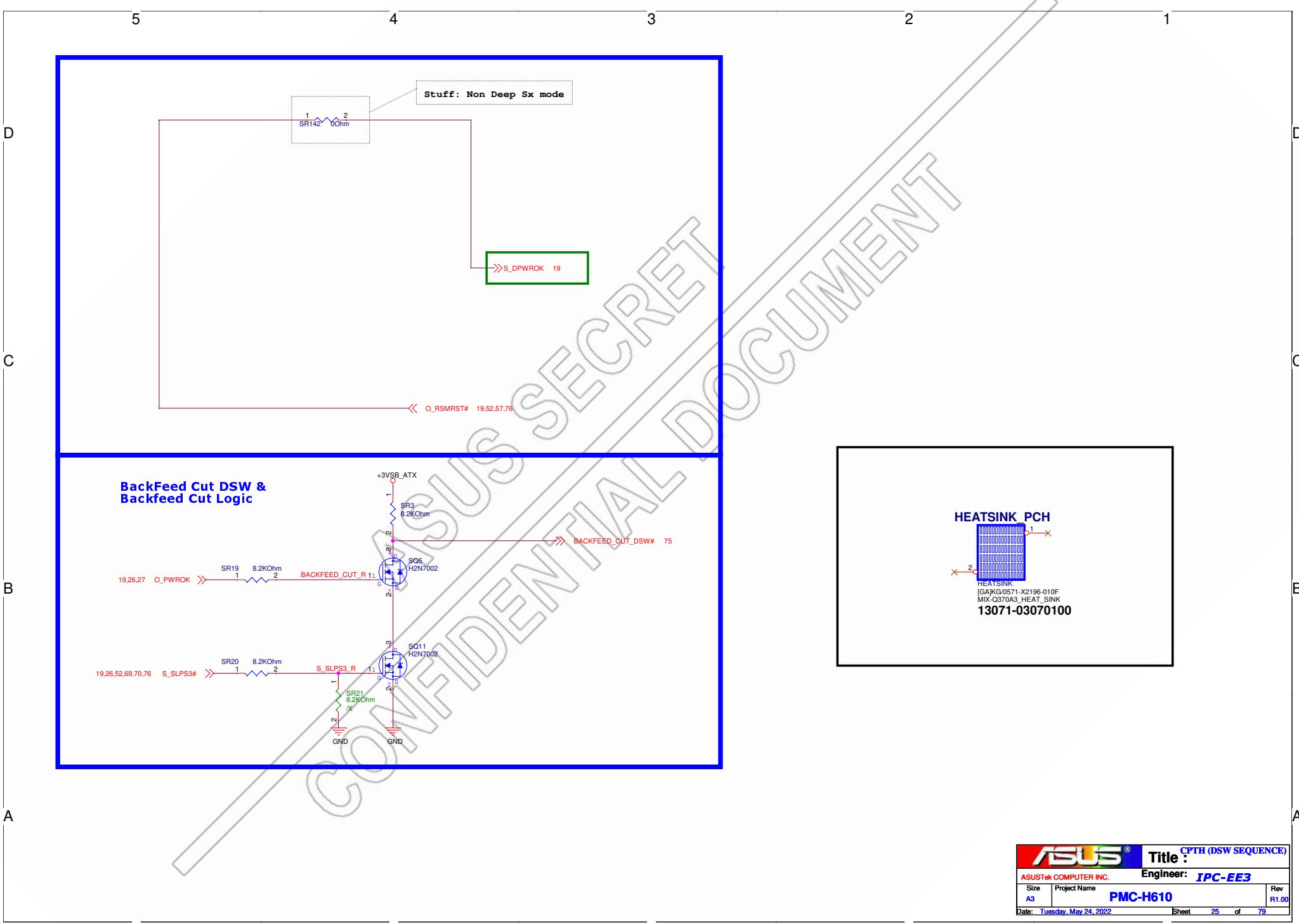
## GPIO Voltage Level

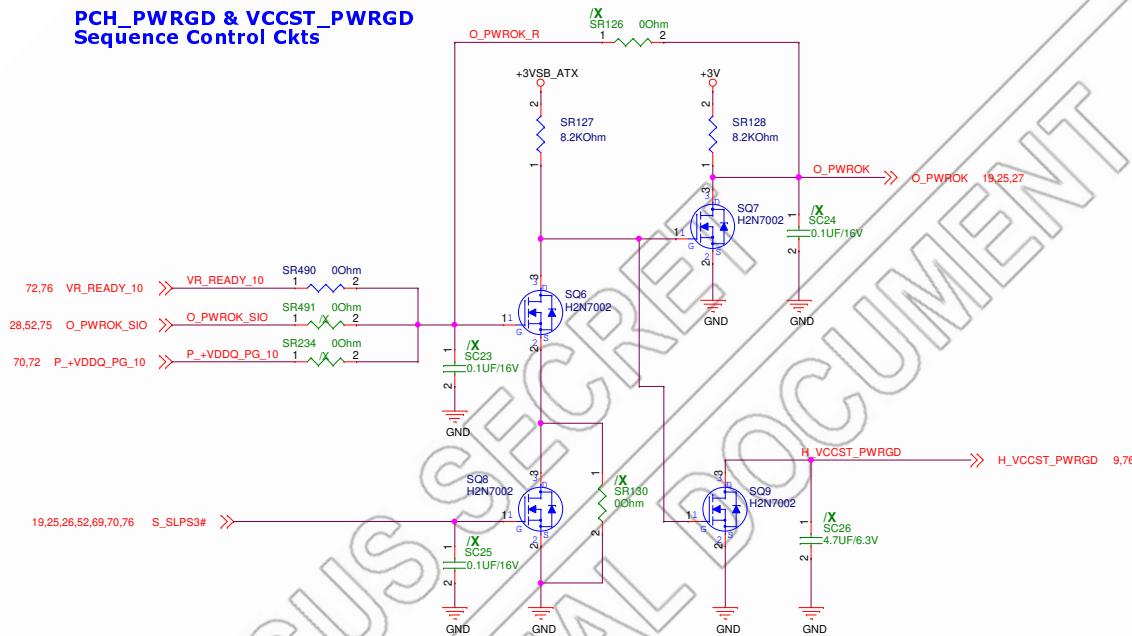
Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+1.8V_A
GPP_B	VCCPGPPB	1.8V or 3.3V	+3VSB_ATX
GPP_C	VCCPGPPB	1.8V or 3.3V	+3VSB_ATX
GPP_D	VCCPGPFD	1.8V or 3.3V	+3VSB_ATX
GPP_E	VCCPGPFEFK	1.8V or 3.3V	+3VSB_ATX
GPP_F	VCCPGPFEFK	1.8V or 3.3V	+3VSB_ATX
GPP_G	VCCPGPGH	1.8V or 3.3V	+3VSB_ATX
GPP_H	VCCPGPGH	1.8V or 3.3V	+3VSB_ATX
GPP_I	VCCPGPPIR	1.8V or 3.3V	+3VSB_ATX
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPP_K	VCCPGPFEFK	1.8V or 3.3V	+3VSB_ATX
GPP_R	VCCPGPPIR	1.8V or 3.3V	+3VSB_ATX
GPP_S	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPD	VCCDSW_3P3	3.3V Only	+3VSB_ATX



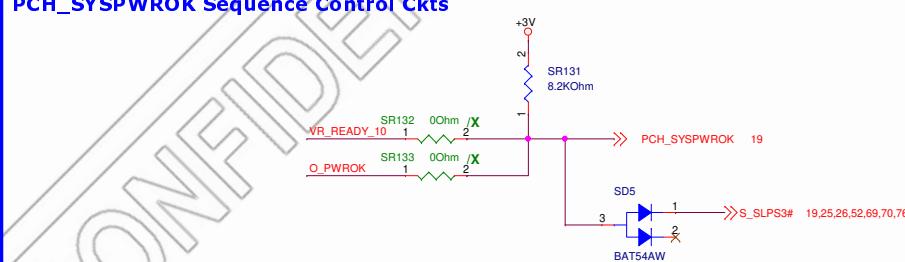
	Title : KPTH (POWER)	
ASUSTek COMPUTER INC.		Engineer: IPC-EE3
Size C	Project Name <b>PMC-H610</b>	Date: Tuesday May 24, 2022 Sheet 23 of







PCH\_SYSPWROK Sequence Control Ckts

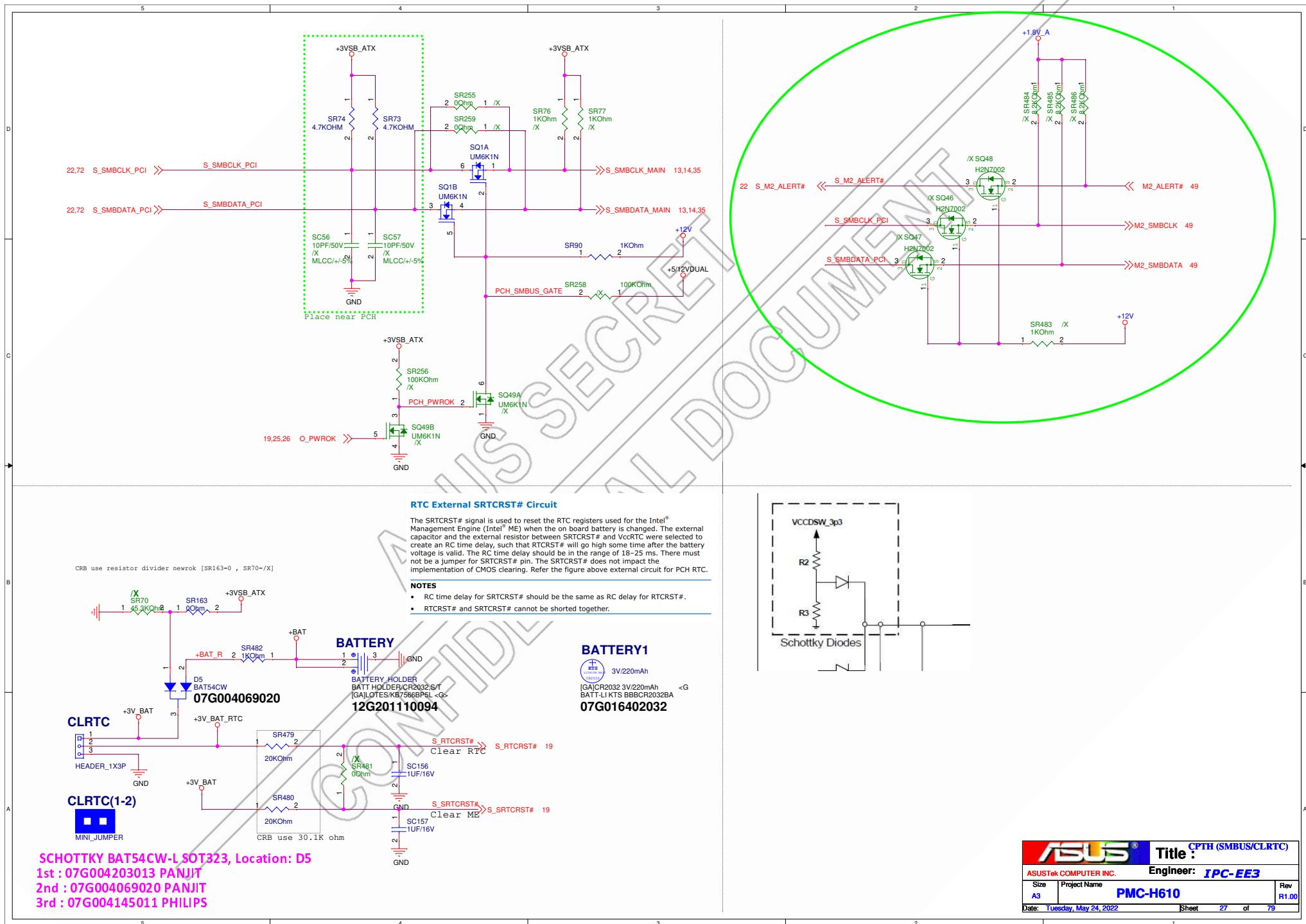


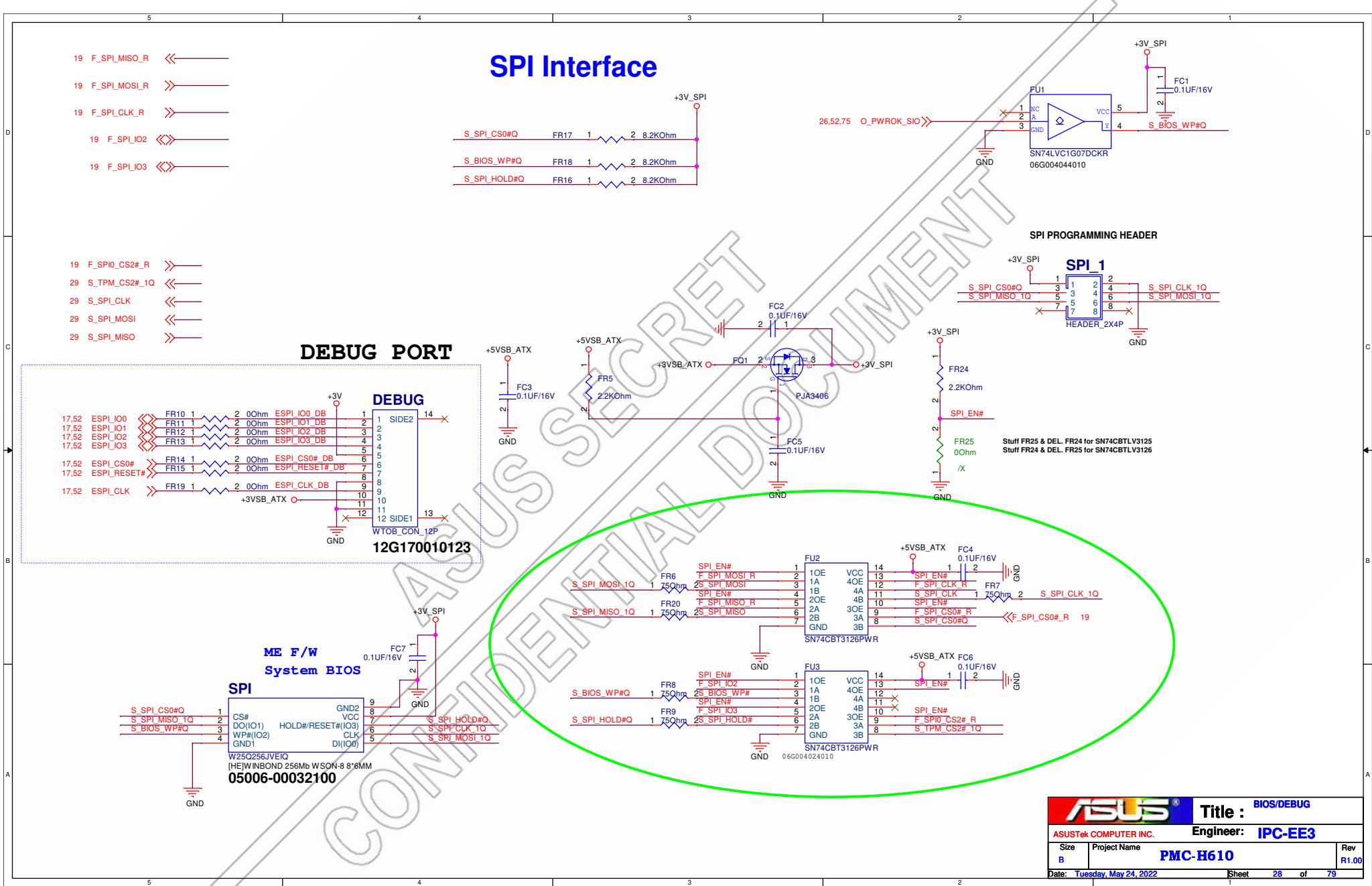
1. PCH will have a minimum of a 1ms delay from PCH\_PWROK to assertion of PROCPWRGD.

2. PLTRST# = AND (PCH\_PWROK, SYS\_PWROK, PROCPWRGD)  
Refer to PDG Figure 40-1 SKL S Flow Diagram for  
SYS\_PWROK/PCH\_PWROK Generation

3. It is recommended that SYS\_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

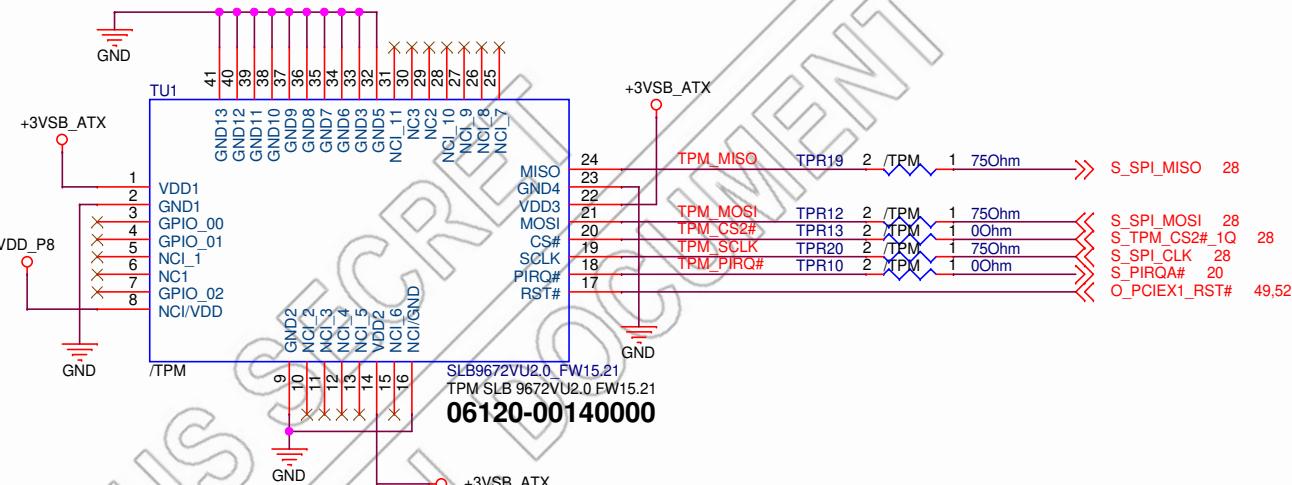
4. PCH\_PWROK and SYS\_PWROK both needs to be high to exit reset, but either signal can come up first. SYS\_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.





# TPM

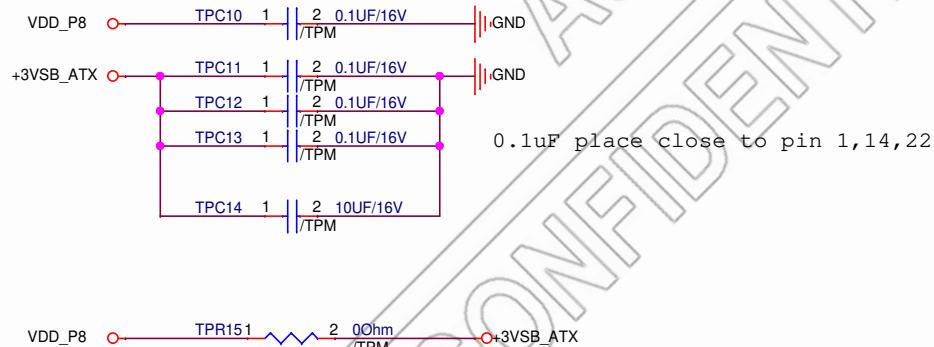
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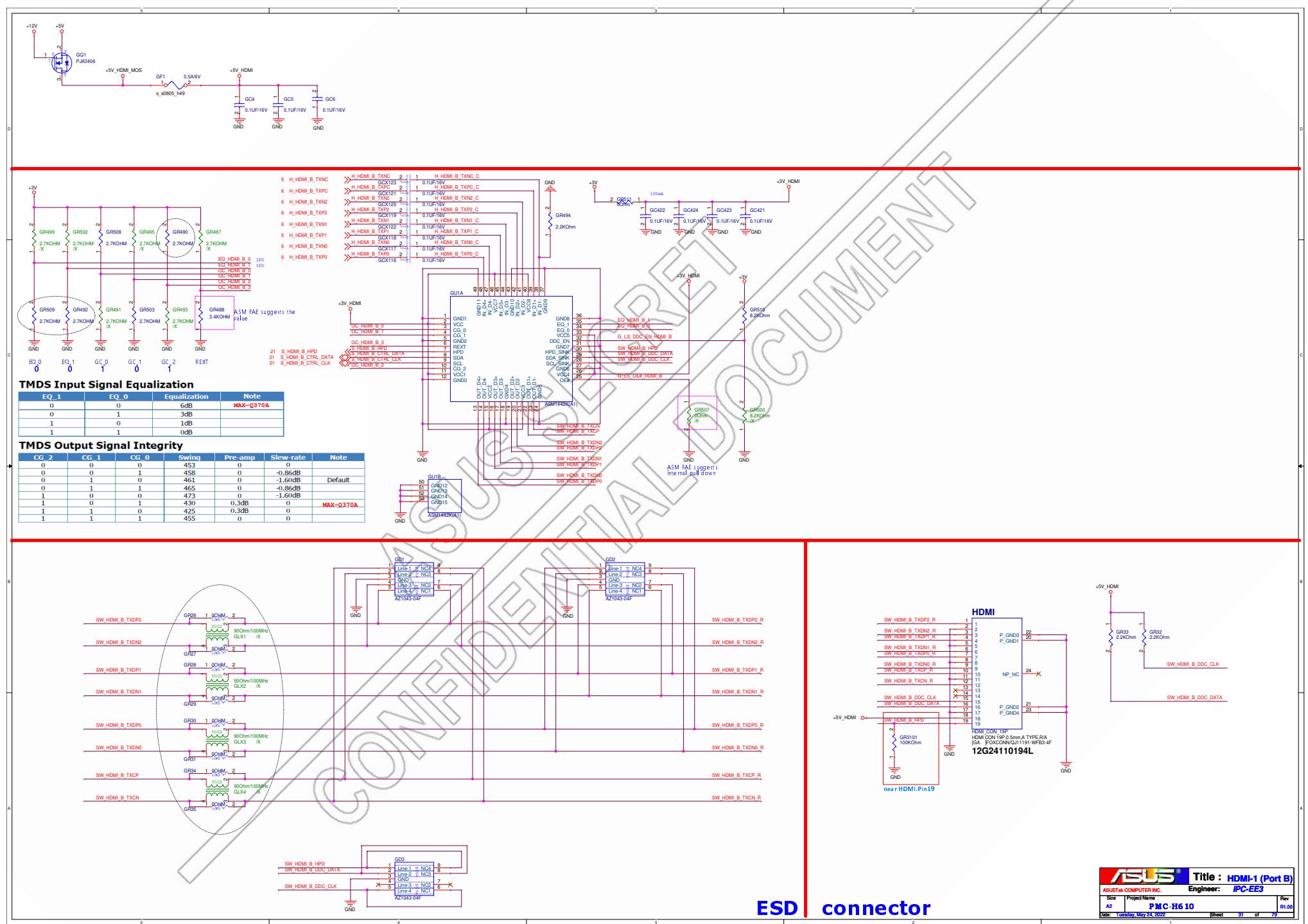
B

A



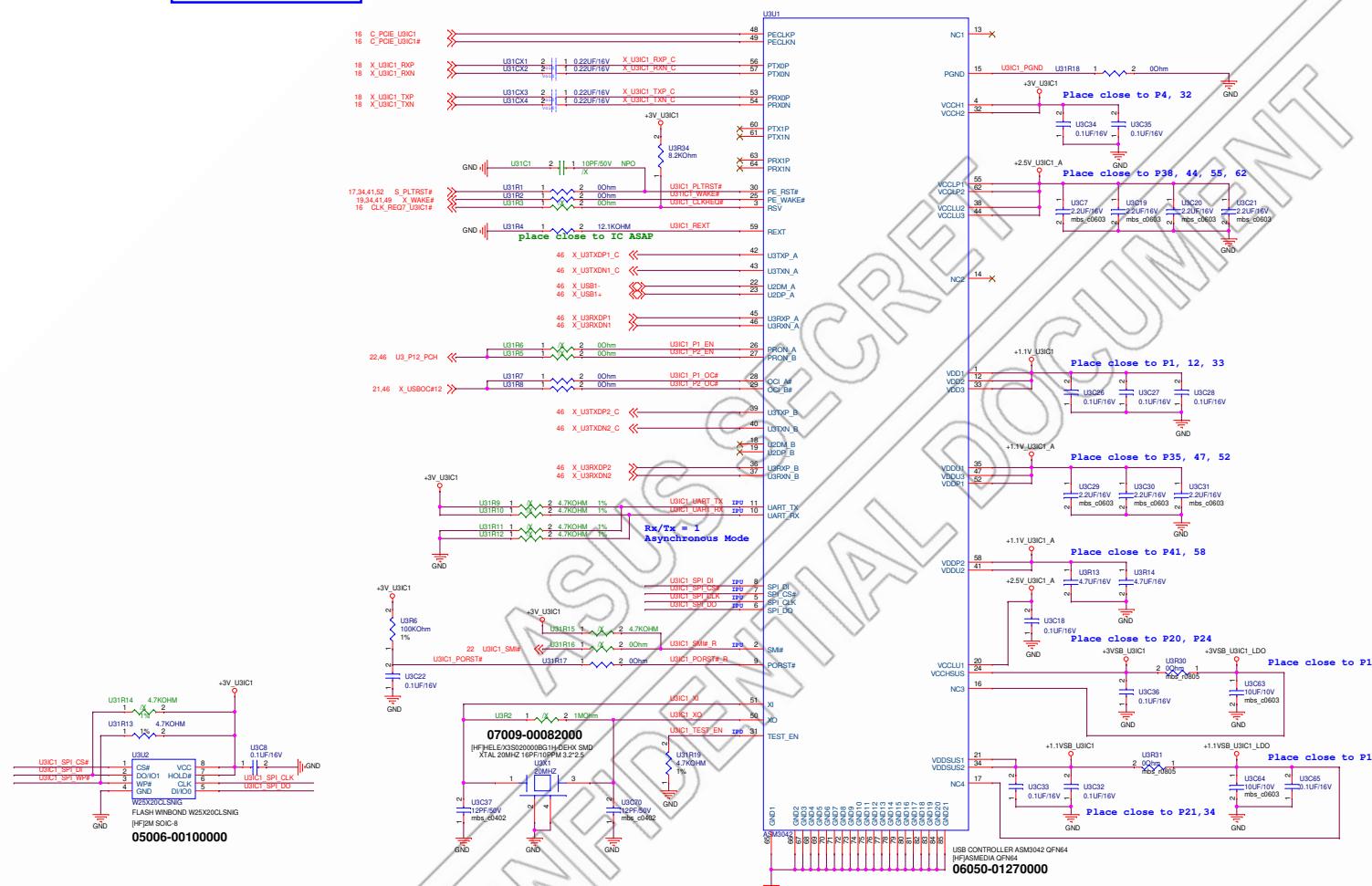
ASUS SECRET  
CONFIDENTIAL DOCUMENT

ASUS		Title : PCIE4_1
ASUSTek COMPUTER INC.		Engineer: IPC-EE3
Size	Project Name	Rev
C	PMC-H610	1.00

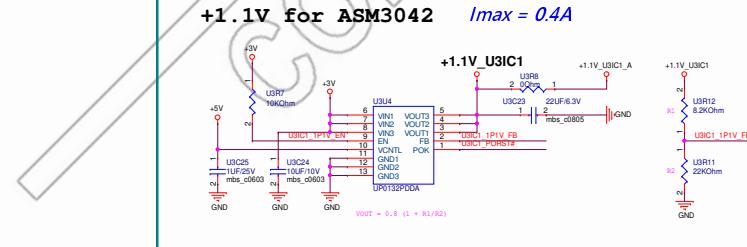


ASUS SECRET  
CONFIDENTIAL DOCUMENT

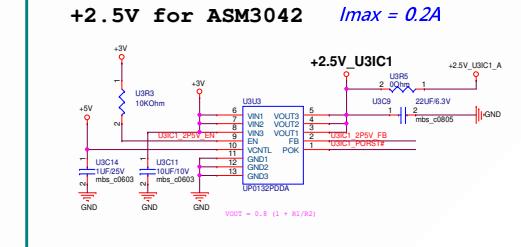
PCIe Gen3 to USB 3.2 Gen1 Host controller (ASM3042)



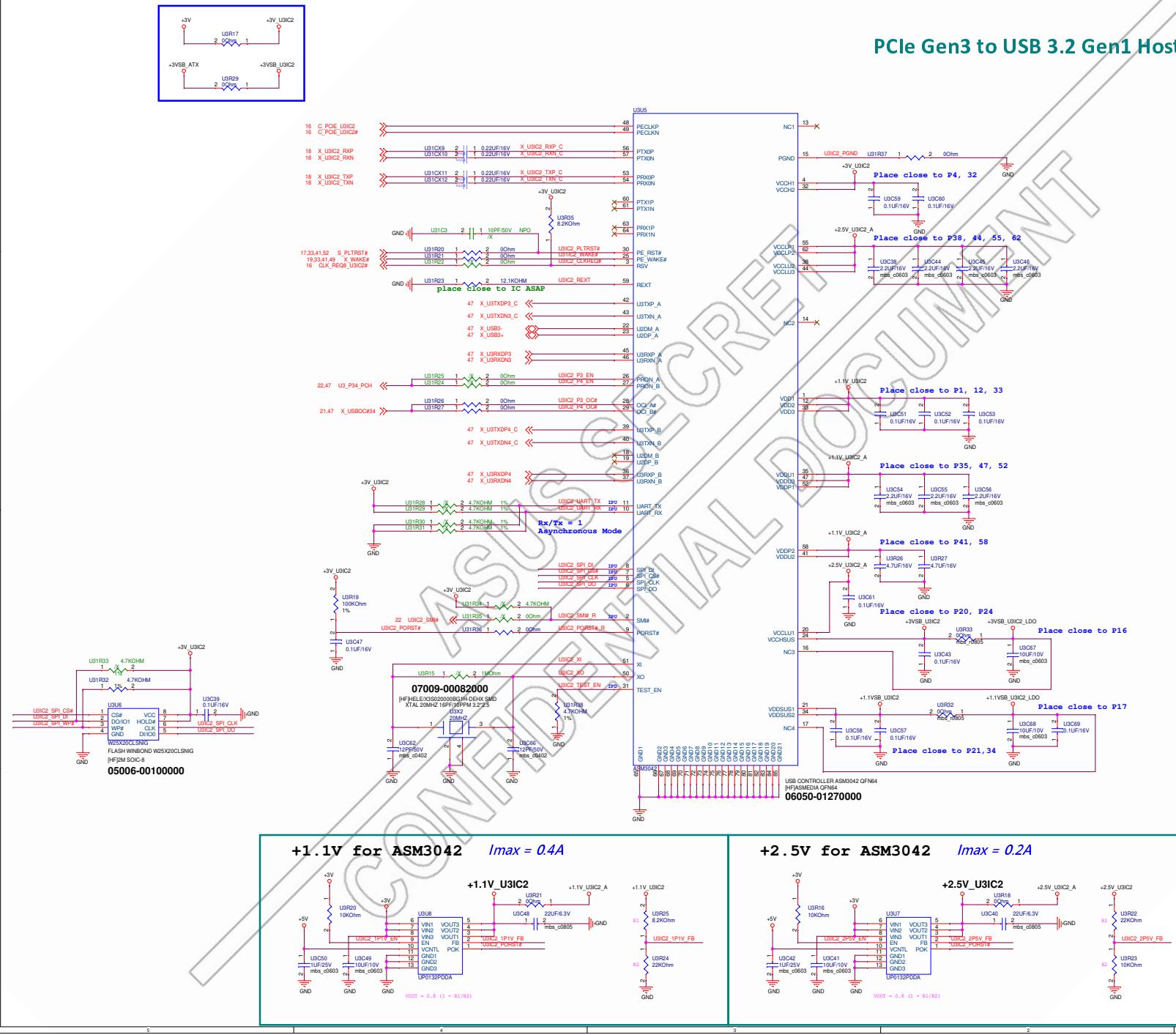
+1.1V for ASM3042       $I_{max} = 0.4A$



+2.5V for ASM3042      *I<sub>max</sub> = 0.2A*

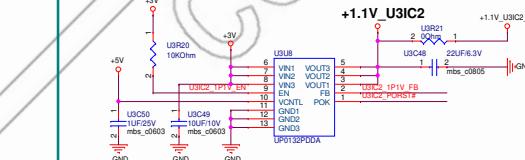


# PCIe Gen3 to USB 3.2 Gen1 Host controller (ASM3042)

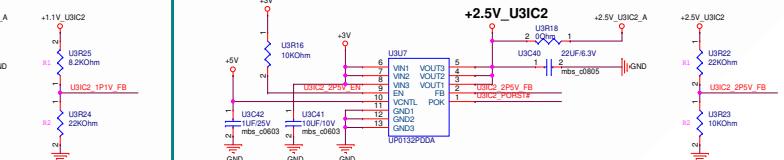


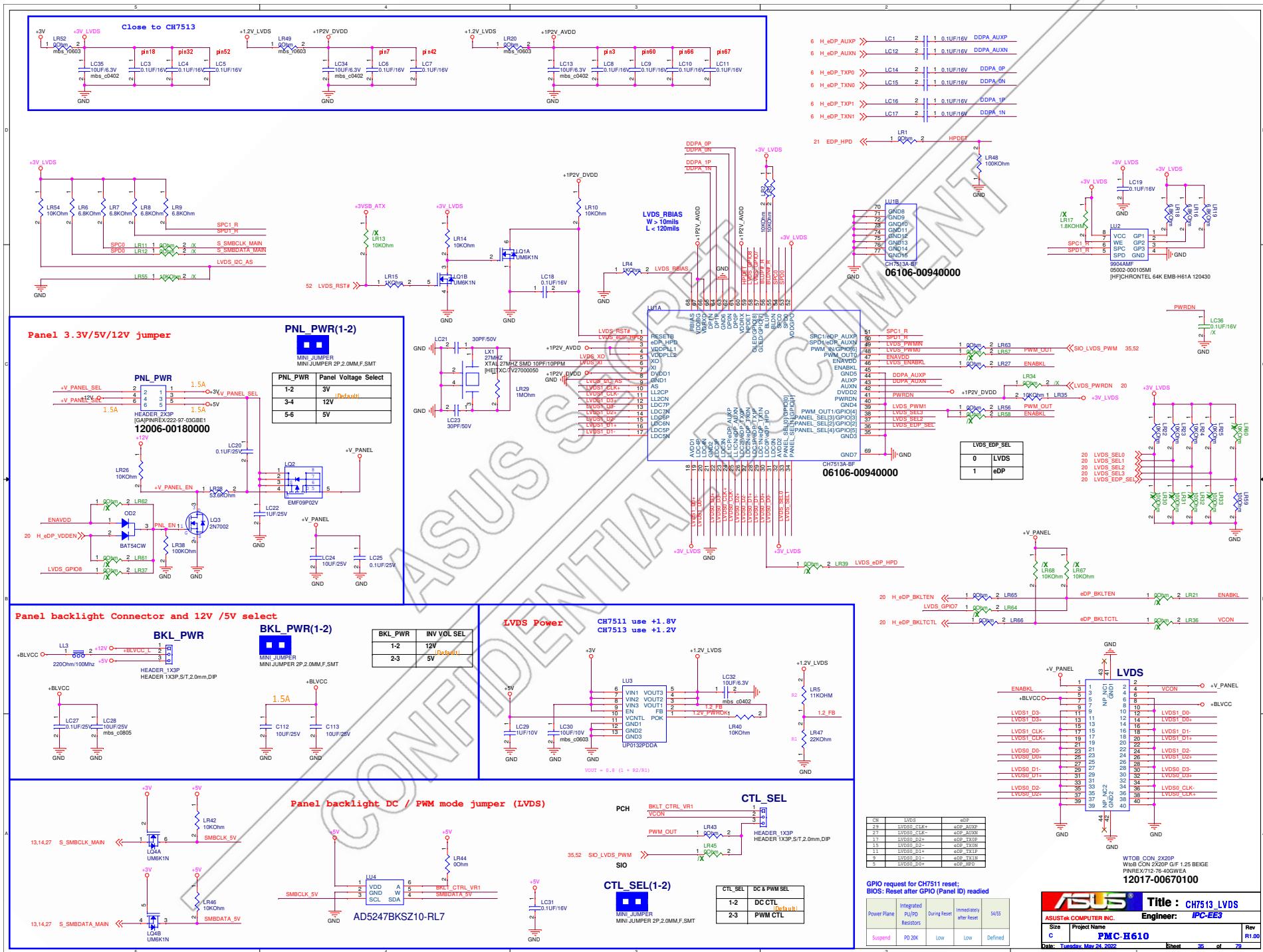
+1.1V for ASM3042       $I_{max} = 0.4A$

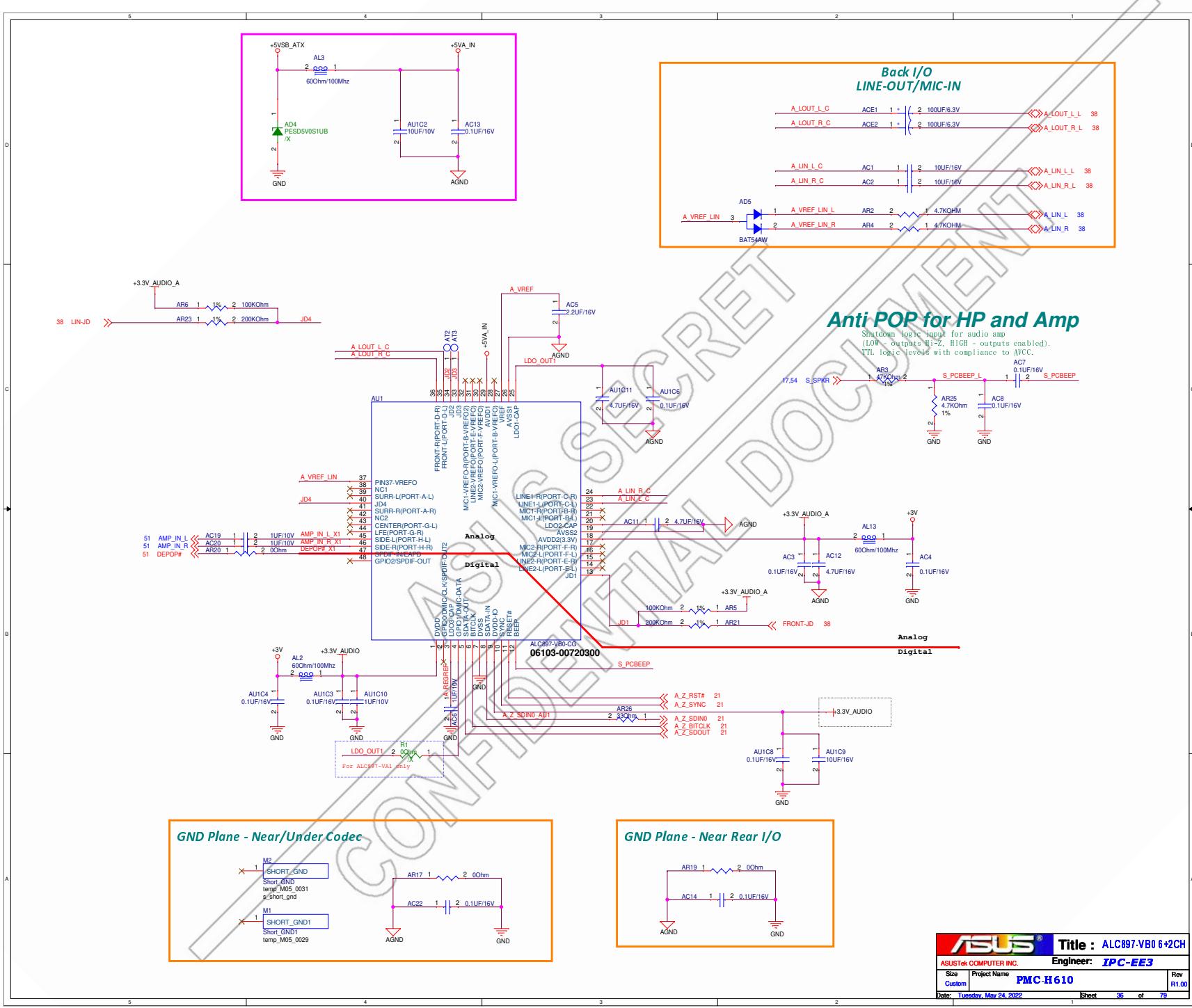
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+2.5V for ASM3042       $I_{max} = 0.2A$







D

D

C

C

B

B

A

A

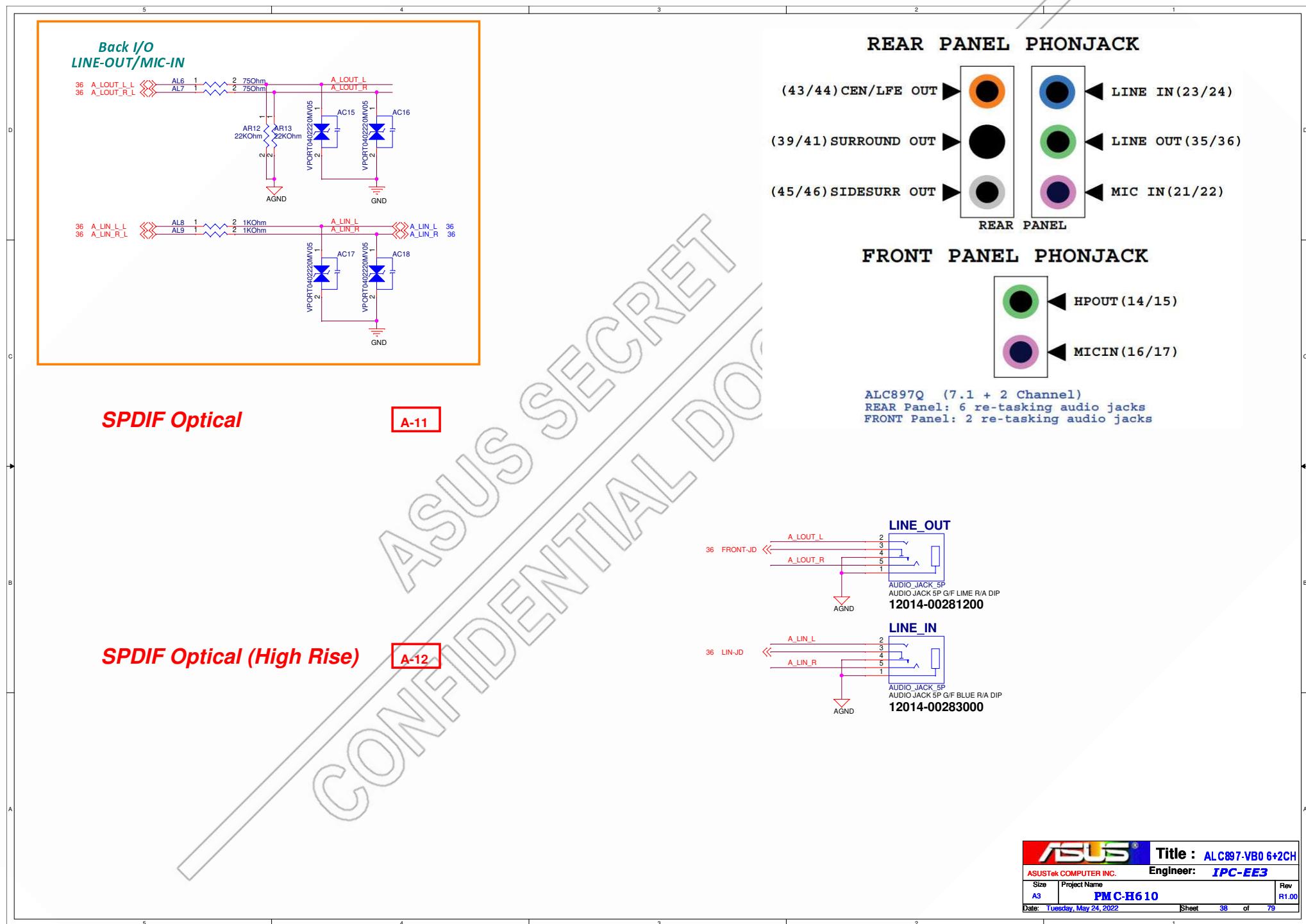
ASUS SECRET  
CONFIDENTIAL DOCUMENT

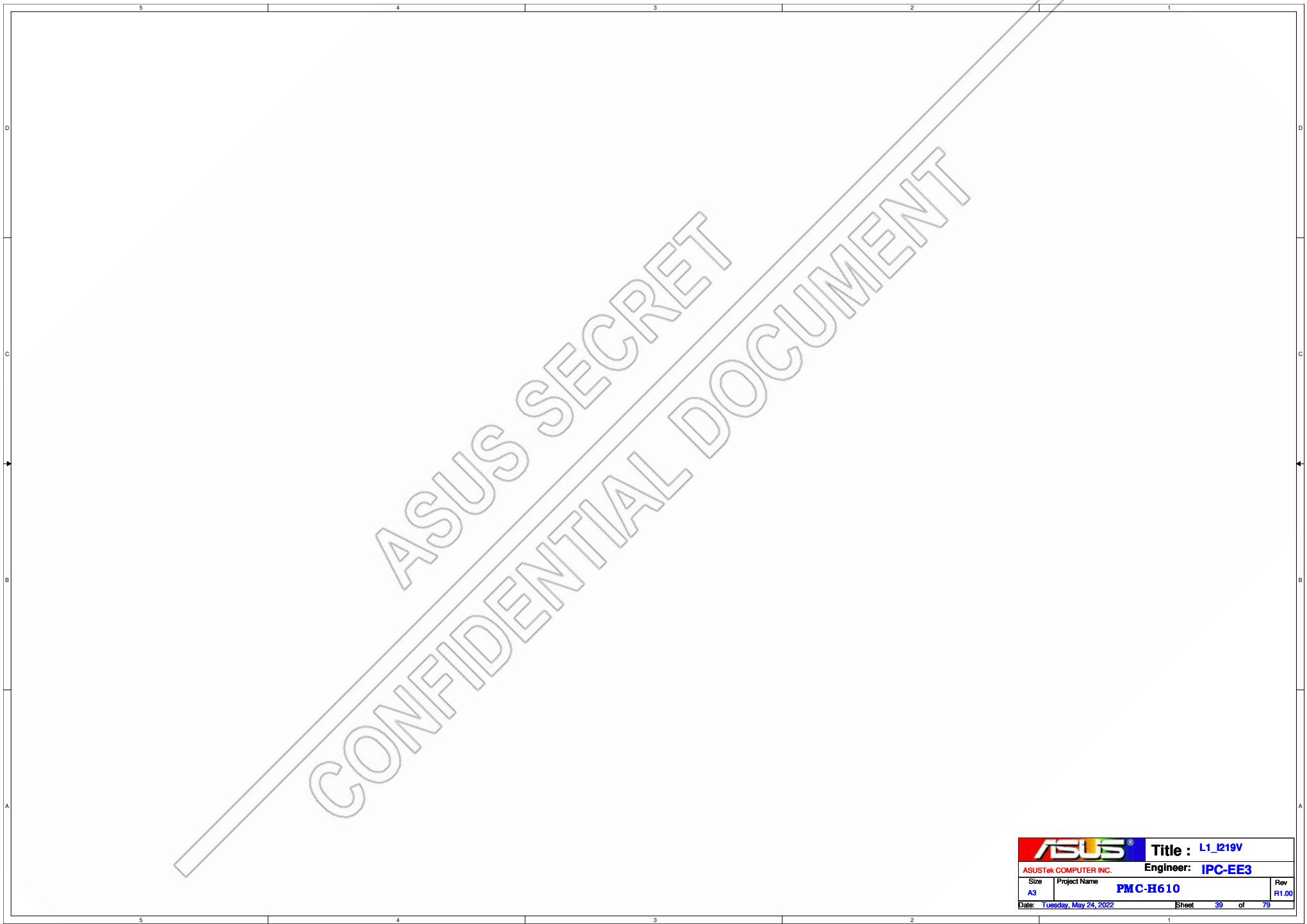


Title : ALC897-VA2 6+2CH

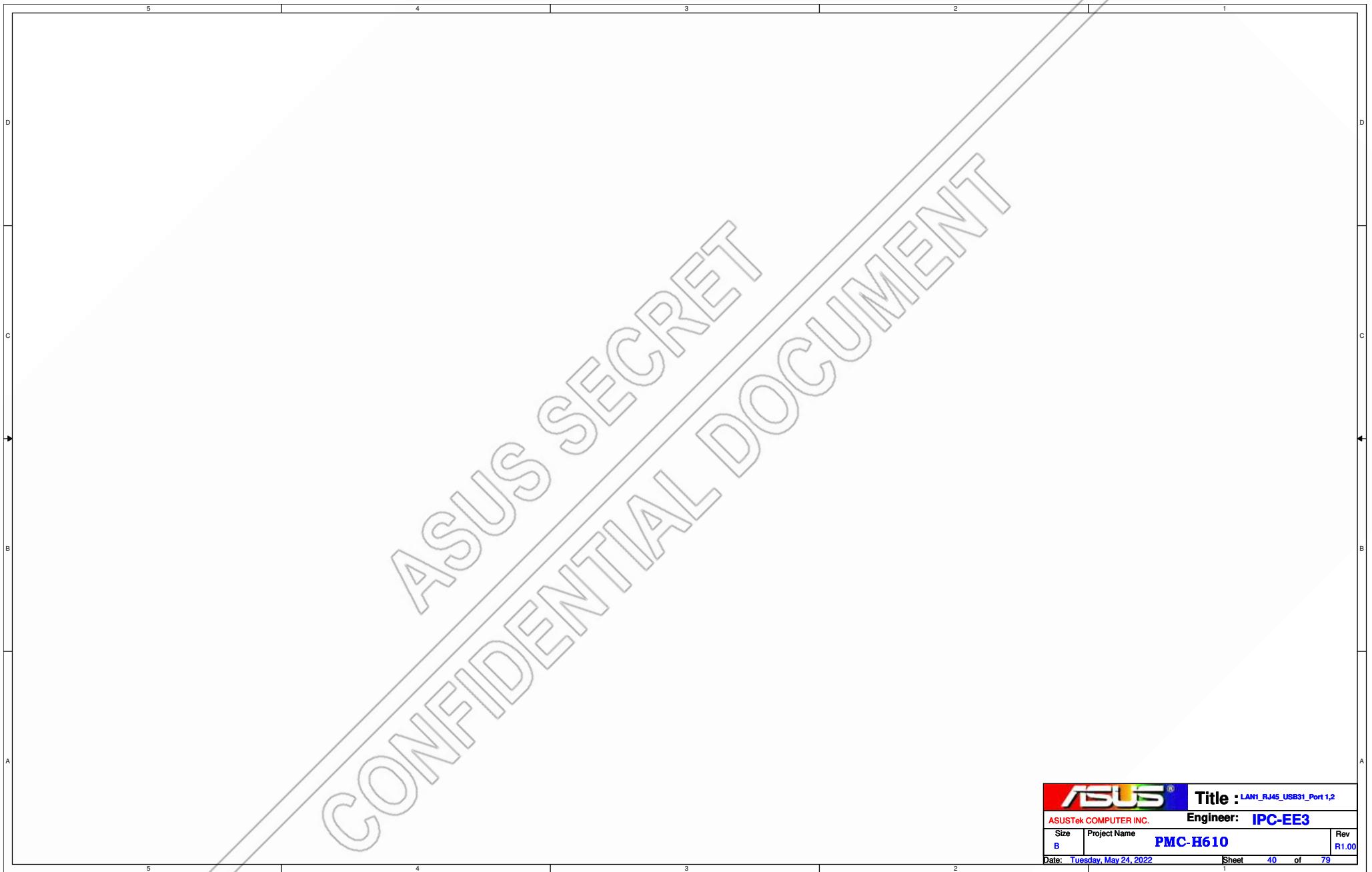
Engineer: IPC-EE3

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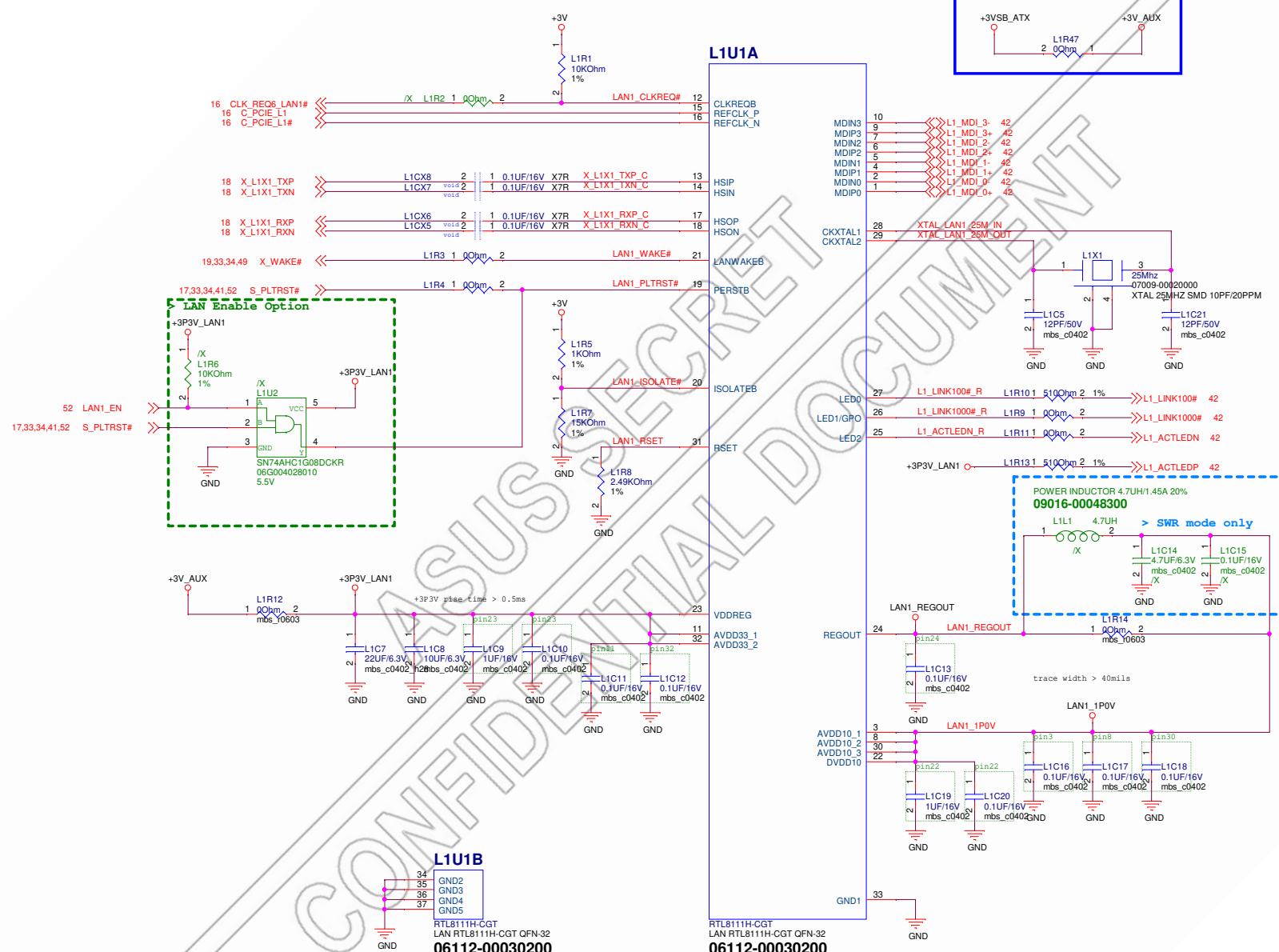




**ASUS**® Title : L1\_I219V  
ASUSTek COMPUTER INC. Engineer: IPC-EE3  
Size Project Name Rev  
A3 PMC-H610 R1.00  
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LAN RTL8111H



BTI 8111H

1st P/N : 06112-00030200 REALTEK/LAN RTL8111H-CGT QFN-32

2nd P/N : 06112-00030500 REALTEK/LAN RTL8111H-VB-CG QFN-32

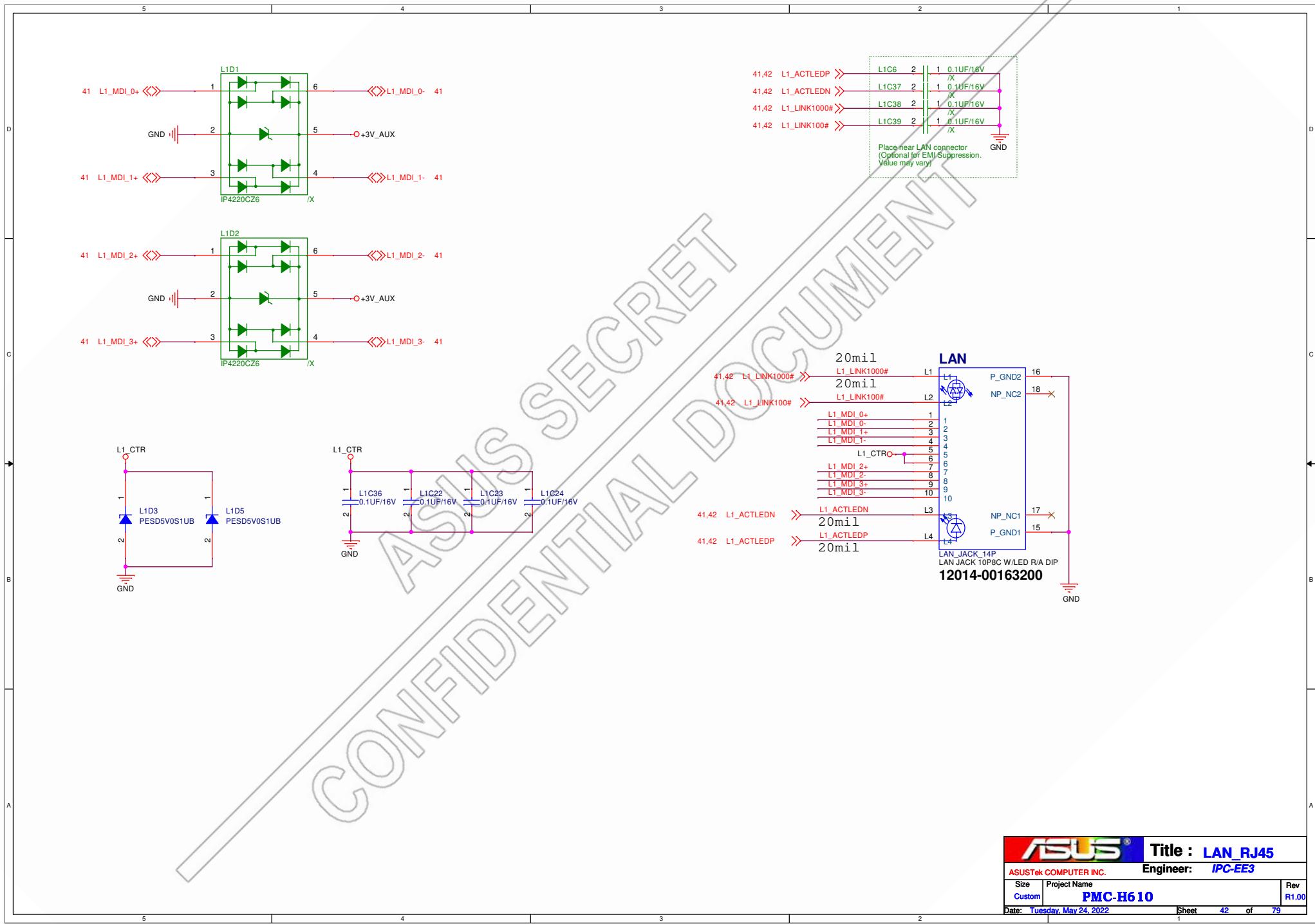
ASUS®

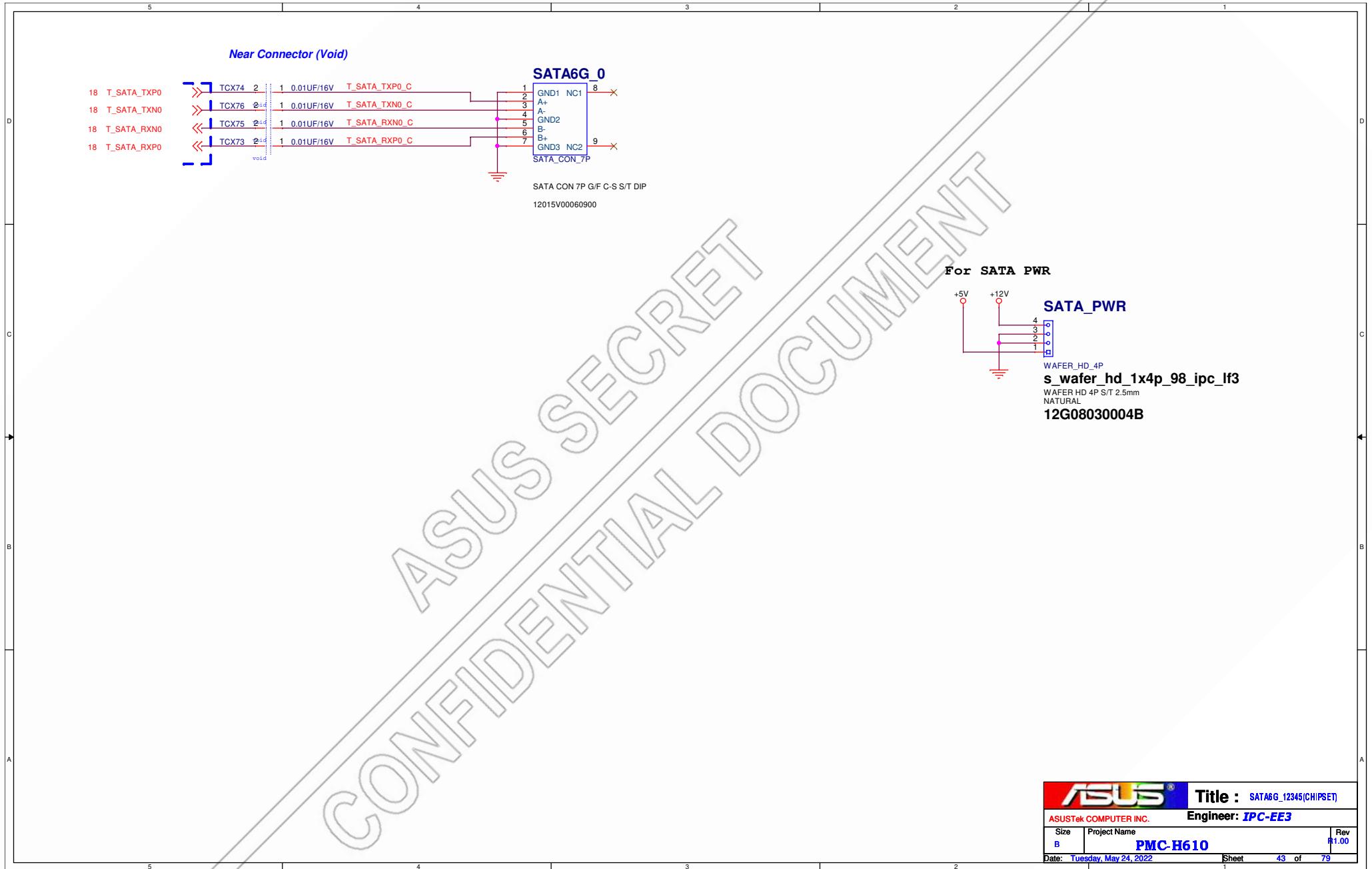
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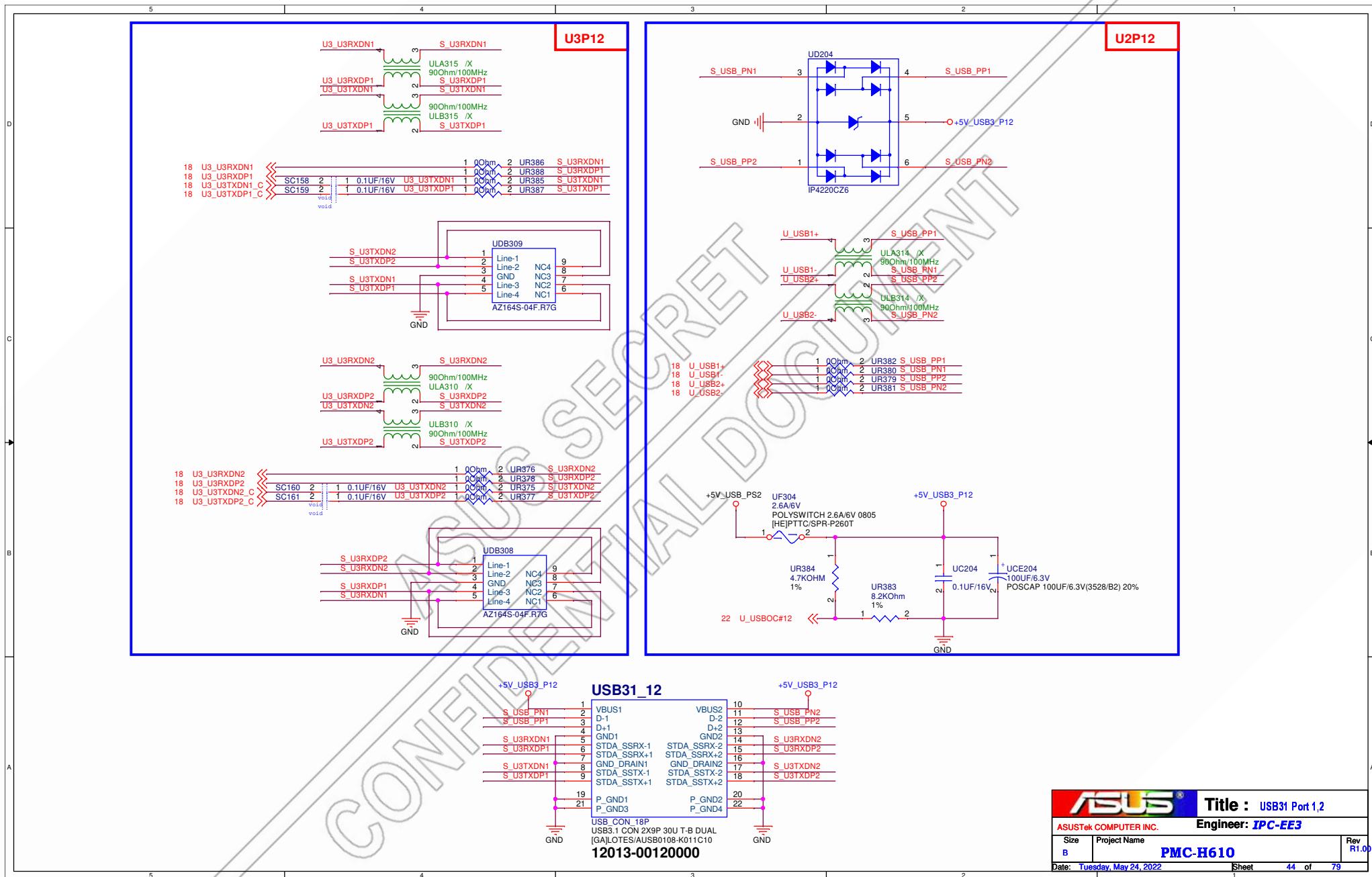
Engineering IPC-650

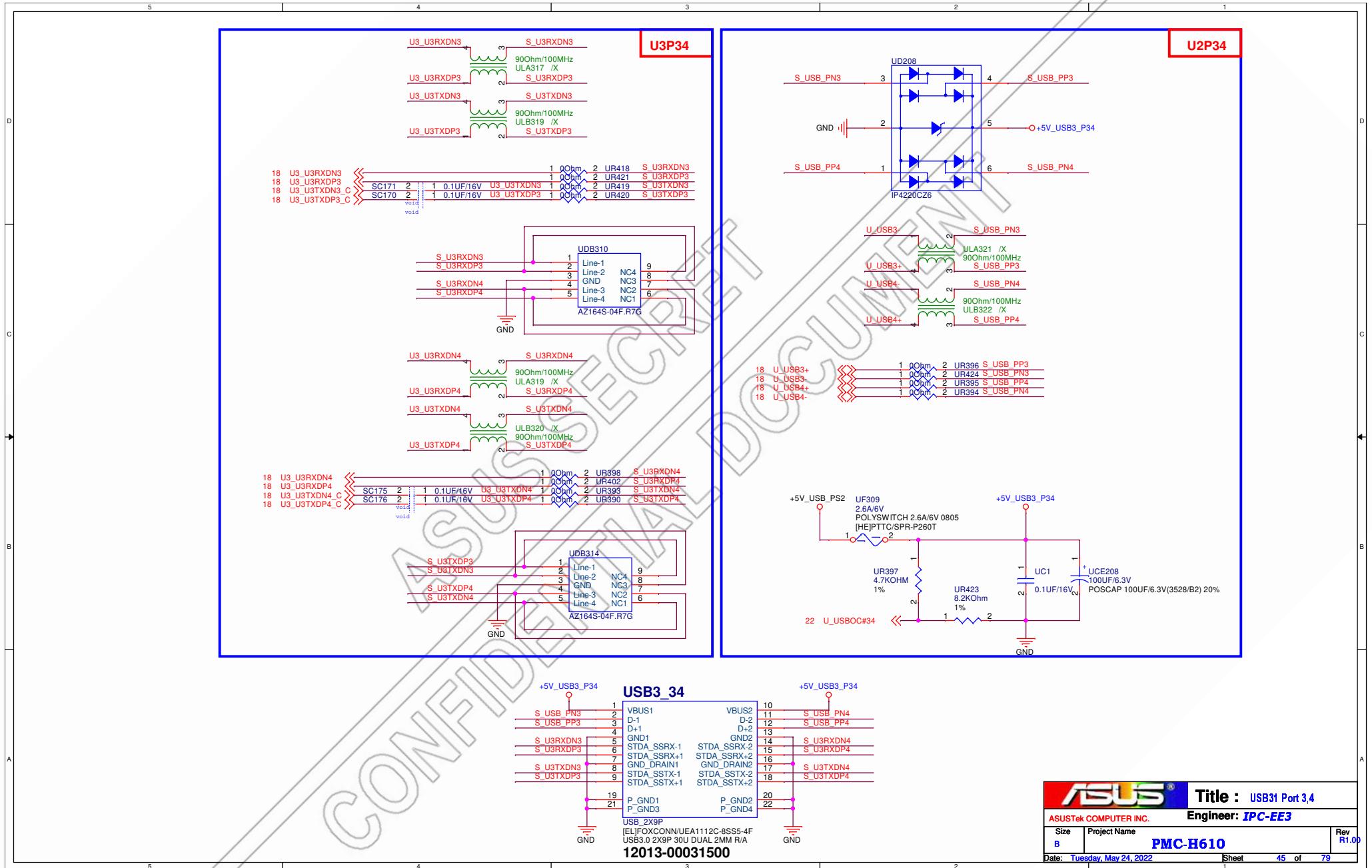
ASUSTek COMPUTER INC.      Engineer: IPC-EEB

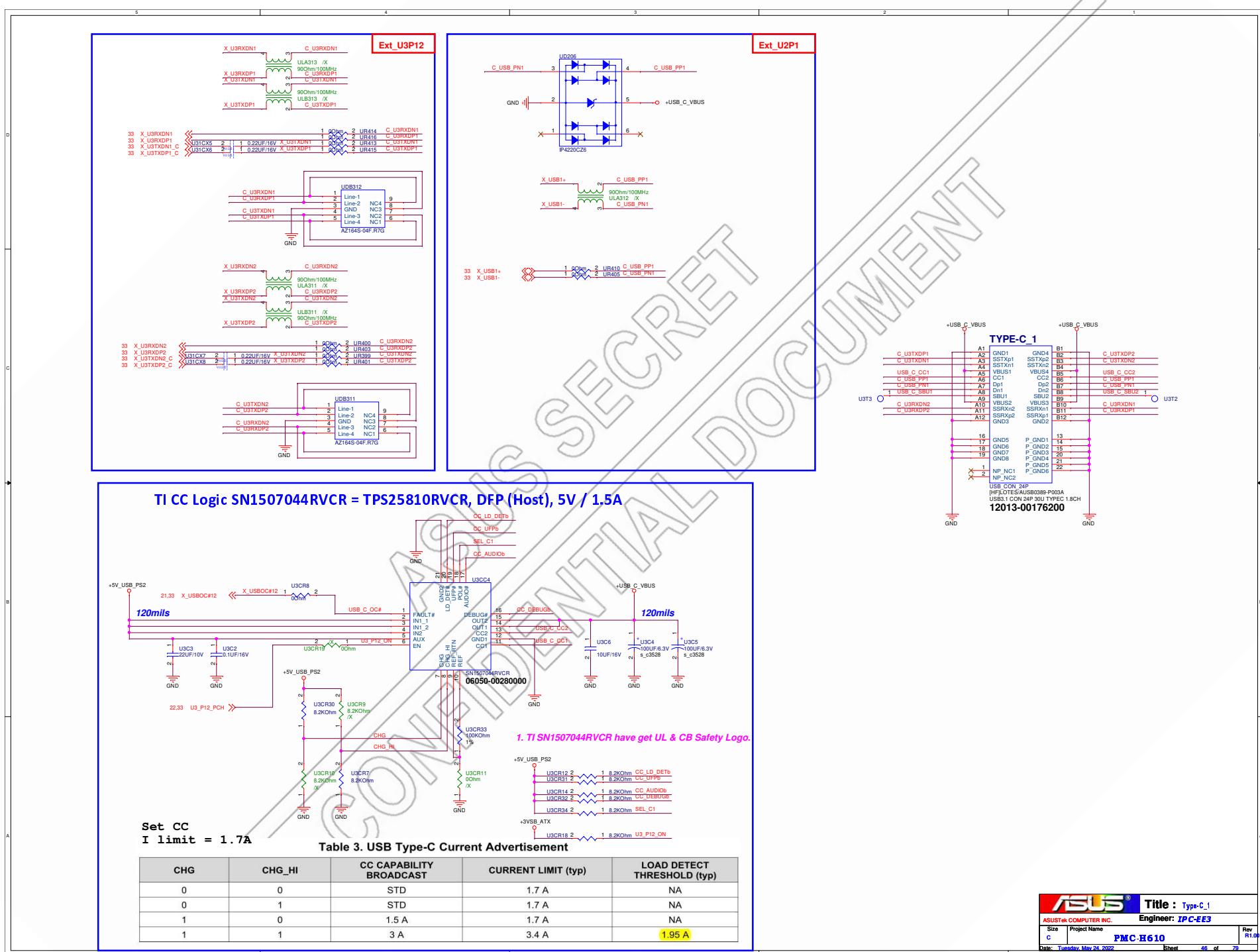
Size	Project Name	Rev
A3	<b>PMC-H610</b>	R1.00
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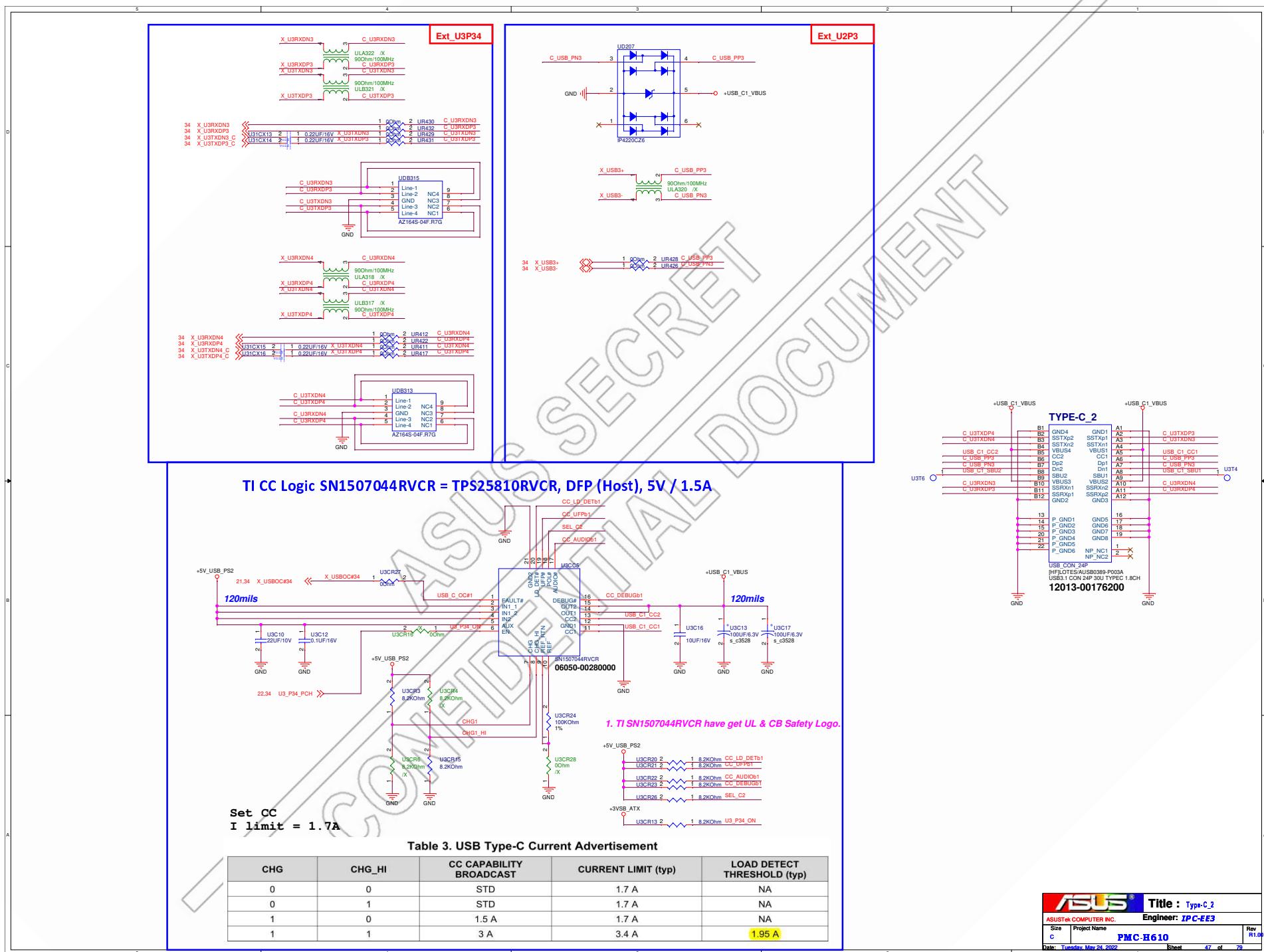


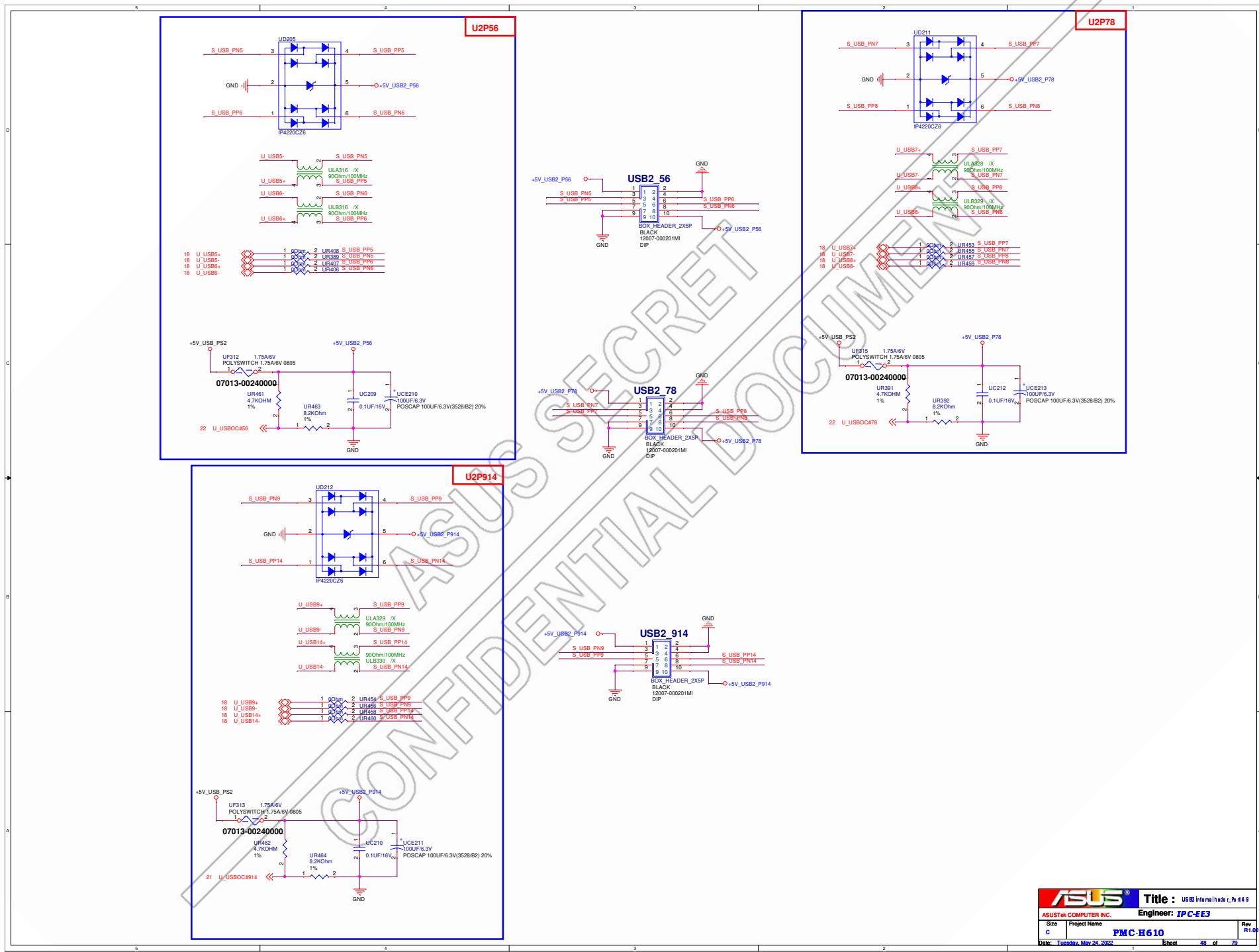


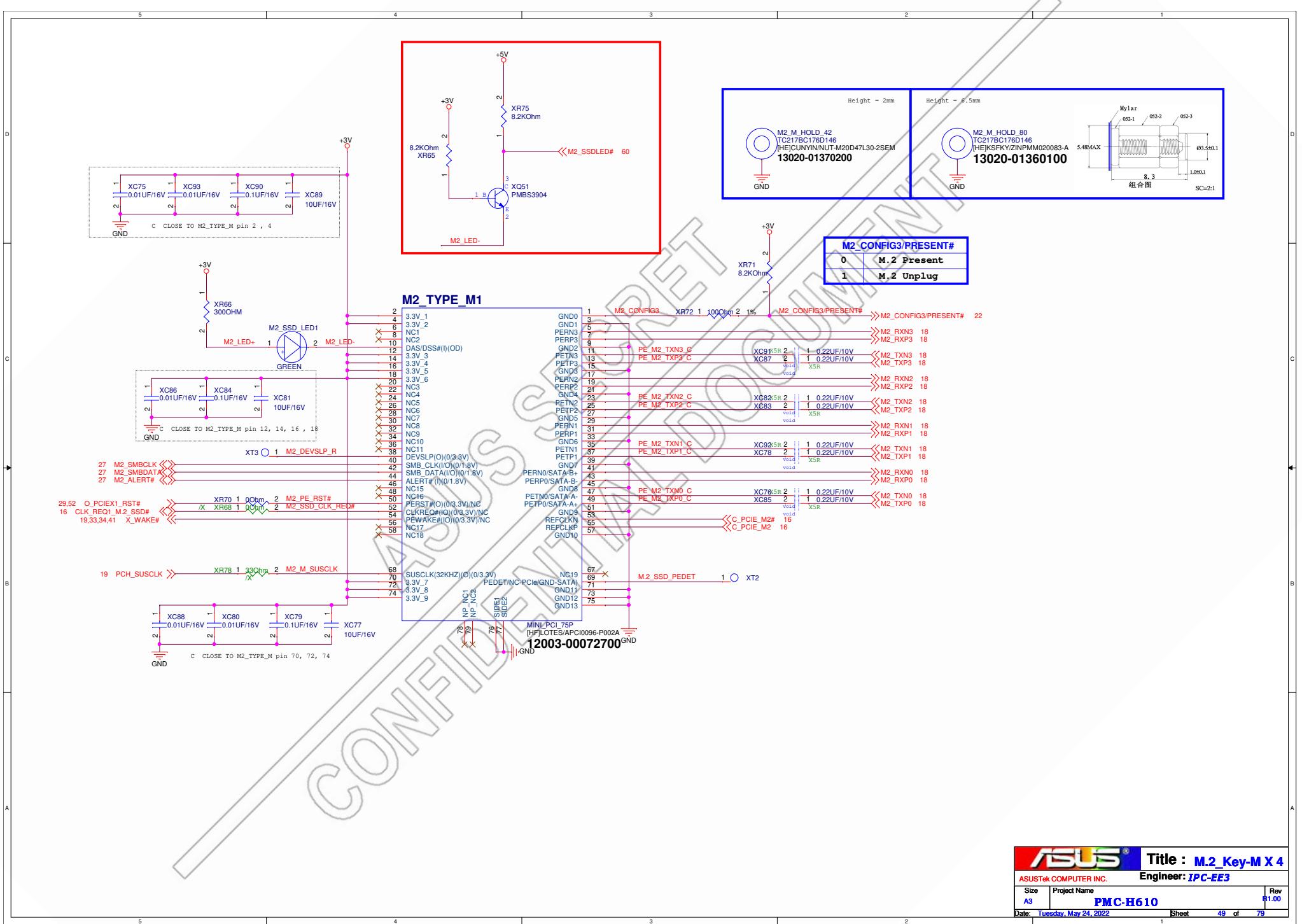












ASUS SECRET  
CONFIDENTIAL DOCUMENT

ASUS		Title : M.2_Key-B_LTE
ASUSTek COMPUTER INC.		Engineer: IPC-EE3
Size	Project Name	Rev
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**AMP - EUA2075JIR1 (Only Speaker)**

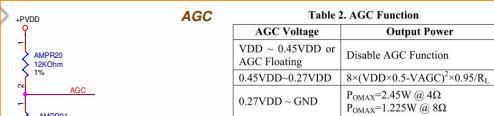
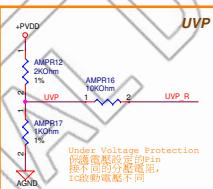
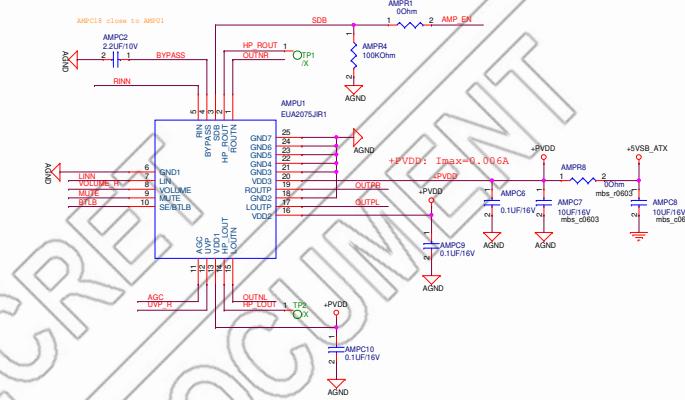
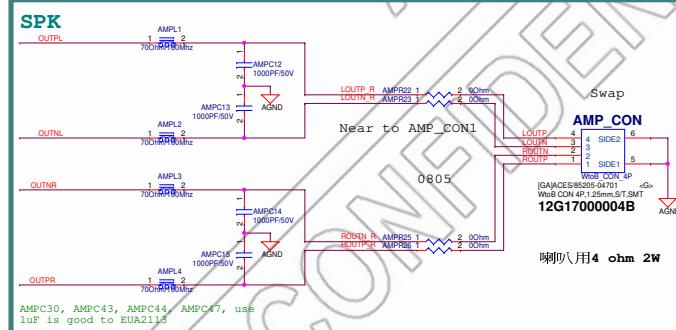
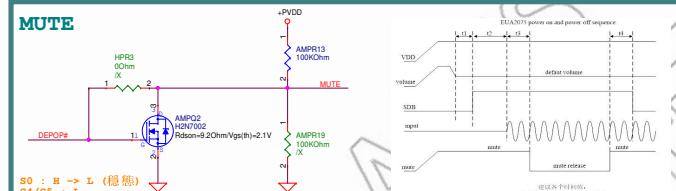
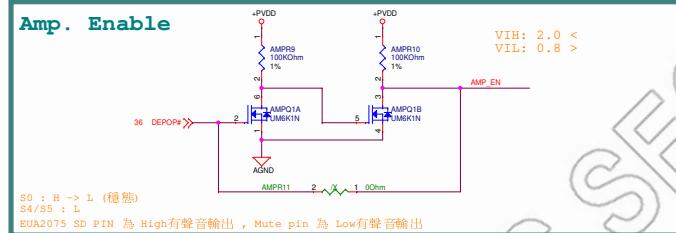
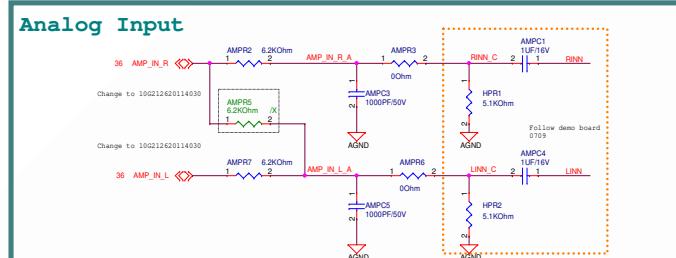


Table 2. AGC Function	
AGC Voltage	Output Power
VDD ~ 0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$8 \times (VDD - 0.5 \cdot VAGC)^3 / 0.95$
0.27VDD ~ GND	$P_{OMAN} = 2.45W @ 4\Omega$ $P_{OMA} = 1.225W @ 8\Omega$

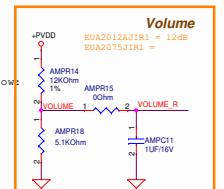
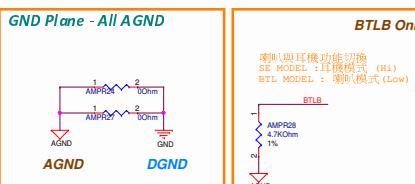
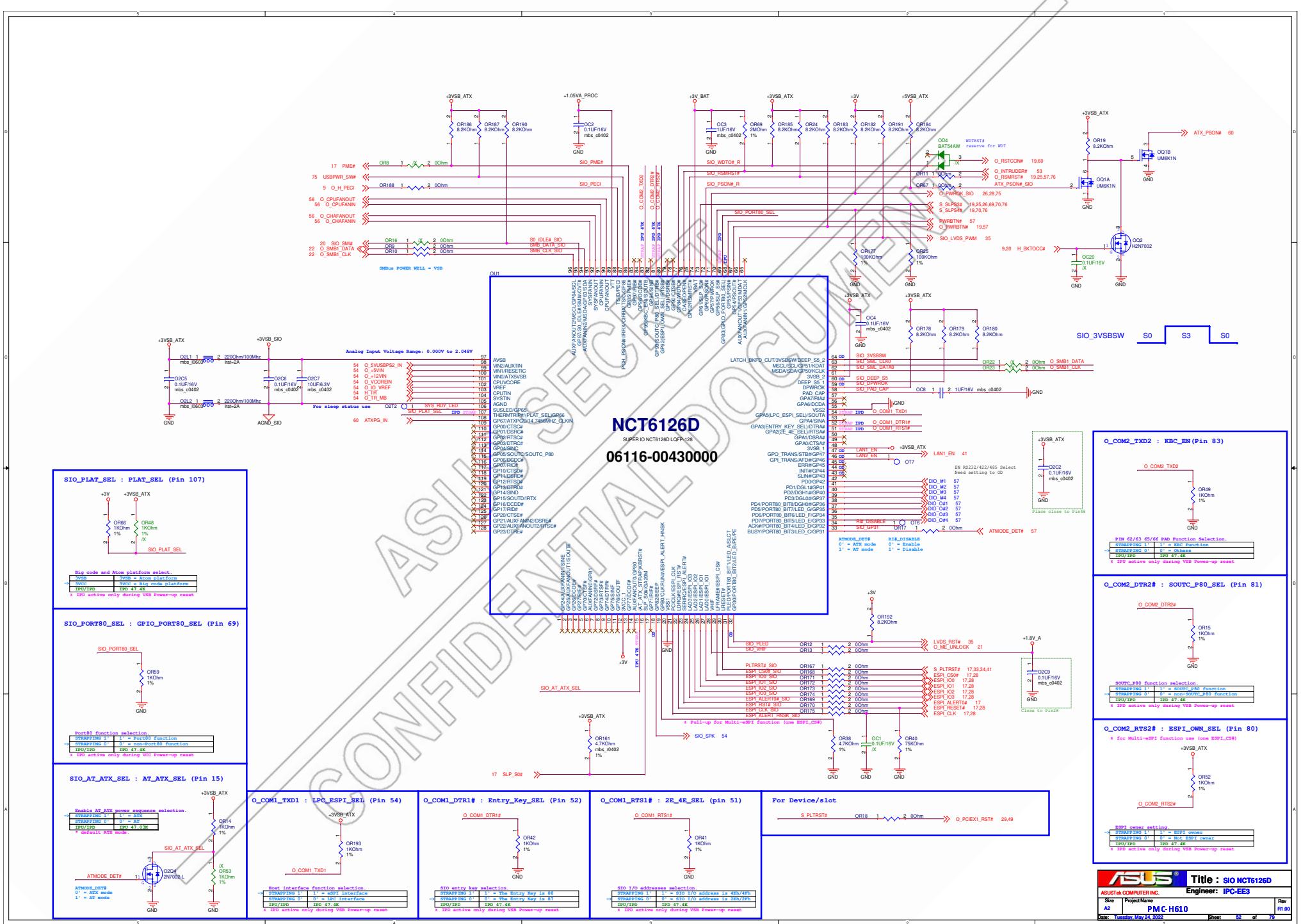


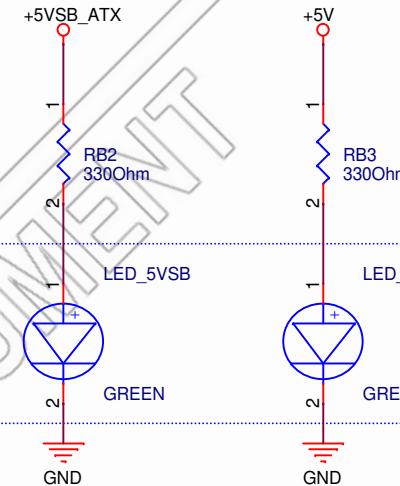
Table 1. DC Volume Control

Step	Decreasing Volume (Volume/Pin Voltage As A Percentage Of VDD) (%)	Increasing Volume (Volume/Pin Voltage As A Percentage Of VDD) (%)	BTL Gain (dB)
1	9.0 - 3.4	2.4 - 0.0	20.0
2	14.4 - 8.4	3.2 - 2.4	19.6
3	4.8 - 6.2	5.2 - 3.8	19.2
4	6.2 - 7.6	6.6 - 5.2	18.8
5	7.6 - 9.0	8.0 - 6.6	18.4
6	9.0 - 10.4	9.4 - 8.0	18.0
7	10.4 - 11.8	10.8 - 9.4	17.6
8	11.8 - 13.2	12.2 - 10.8	17.2
9	13.2 - 14.6	13.6 - 12.2	16.8
10	14.6 - 16.0	15.0 - 13.6	16.4
11	16.0 - 17.4	16.4 - 15.0	16.0
12	17.4 - 18.8	17.8 - 15.4	15.6
13	18.8 - 20.2	19.2 - 17.8	15.2
14	20.2 - 21.6	20.6 - 19.2	14.8
15	21.6 - 23.0	22.0 - 18.8	14.4
16	23.0 - 24.4	23.4 - 22.0	14.0
17	24.4 - 25.8	24.8 - 23.4	13.6
18	25.8 - 27.2	26.2 - 24.8	13.2
19	27.2 - 28.6	27.6 - 26.2	12.8
20	28.6 - 30.0	29.0 - 27.6	12.4
21	30.0 - 31.4	30.4 - 29.0	12.0

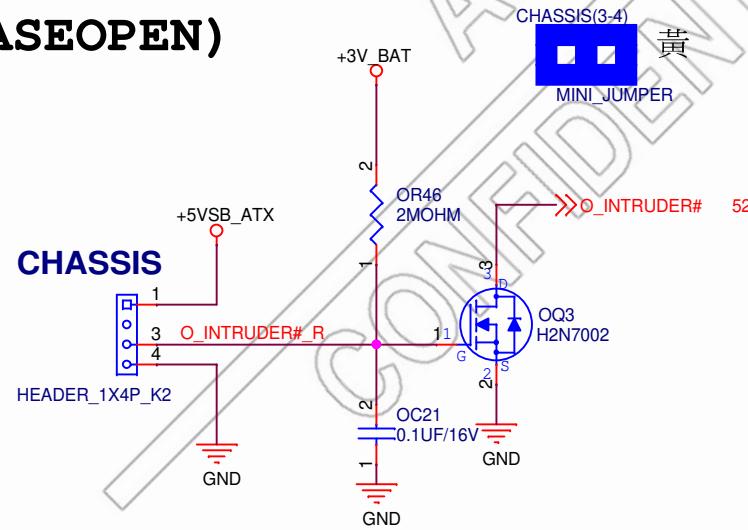




POWER\_PWR



## Intrudor (CASEOPEN)



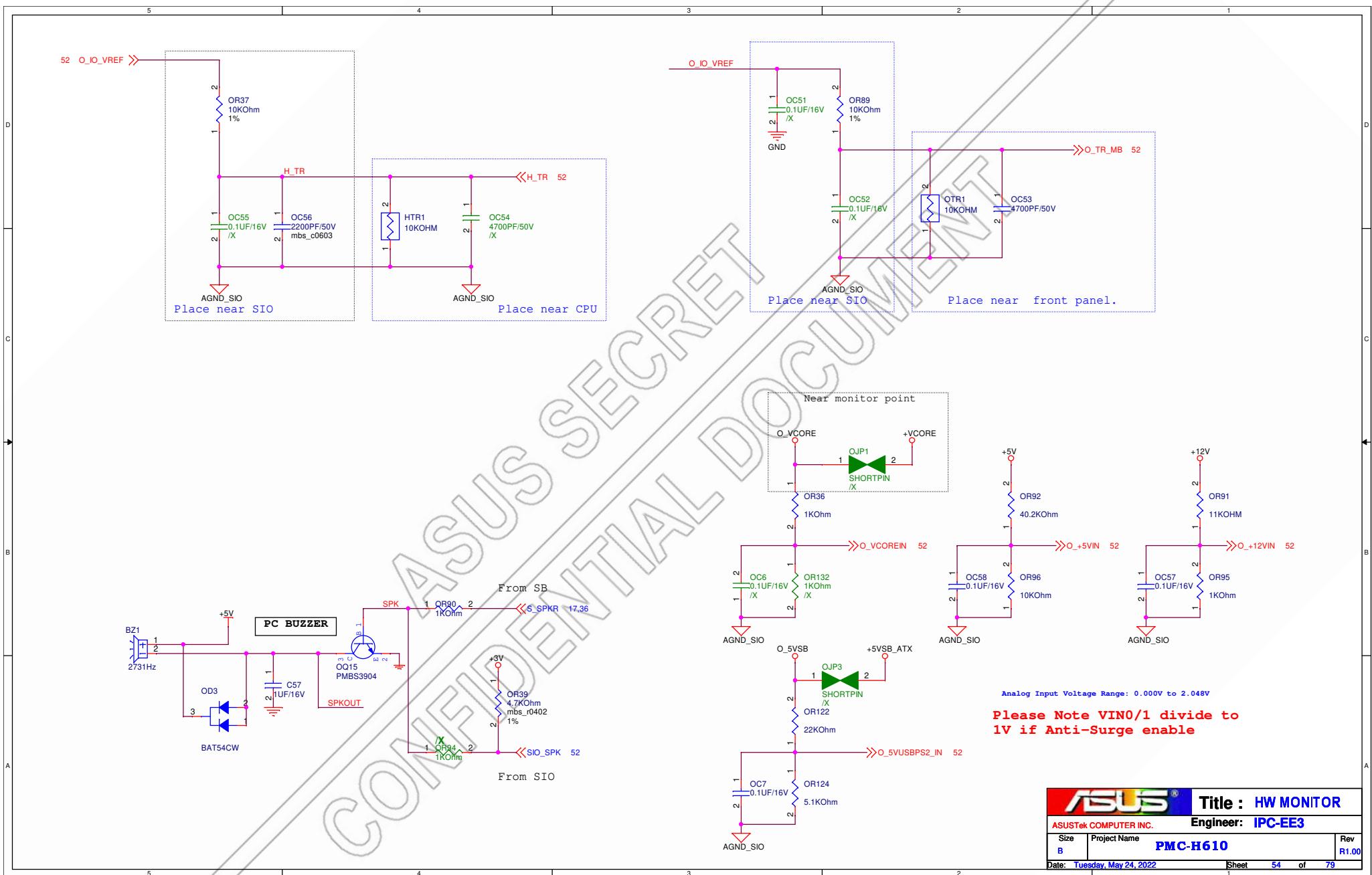
To SIO

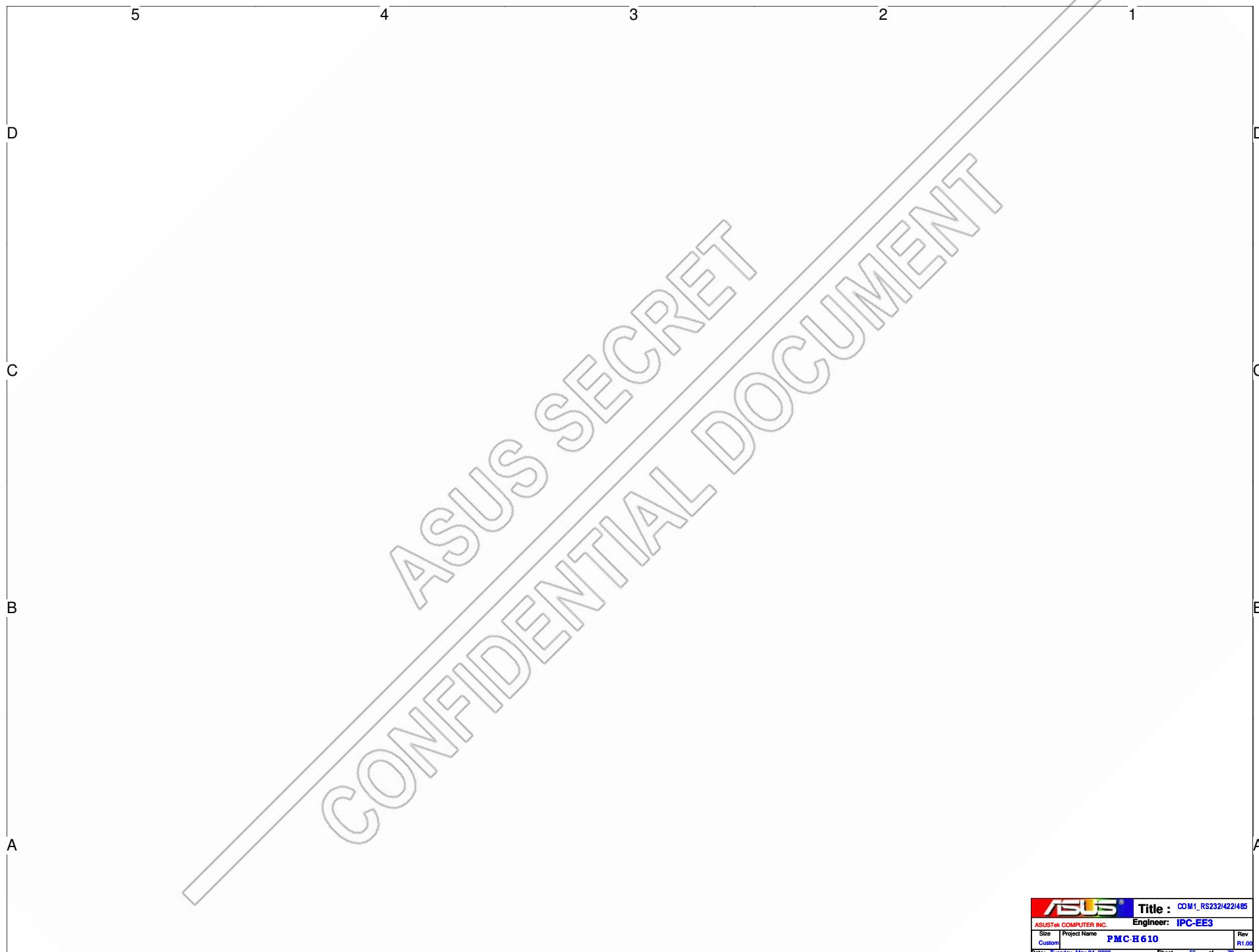


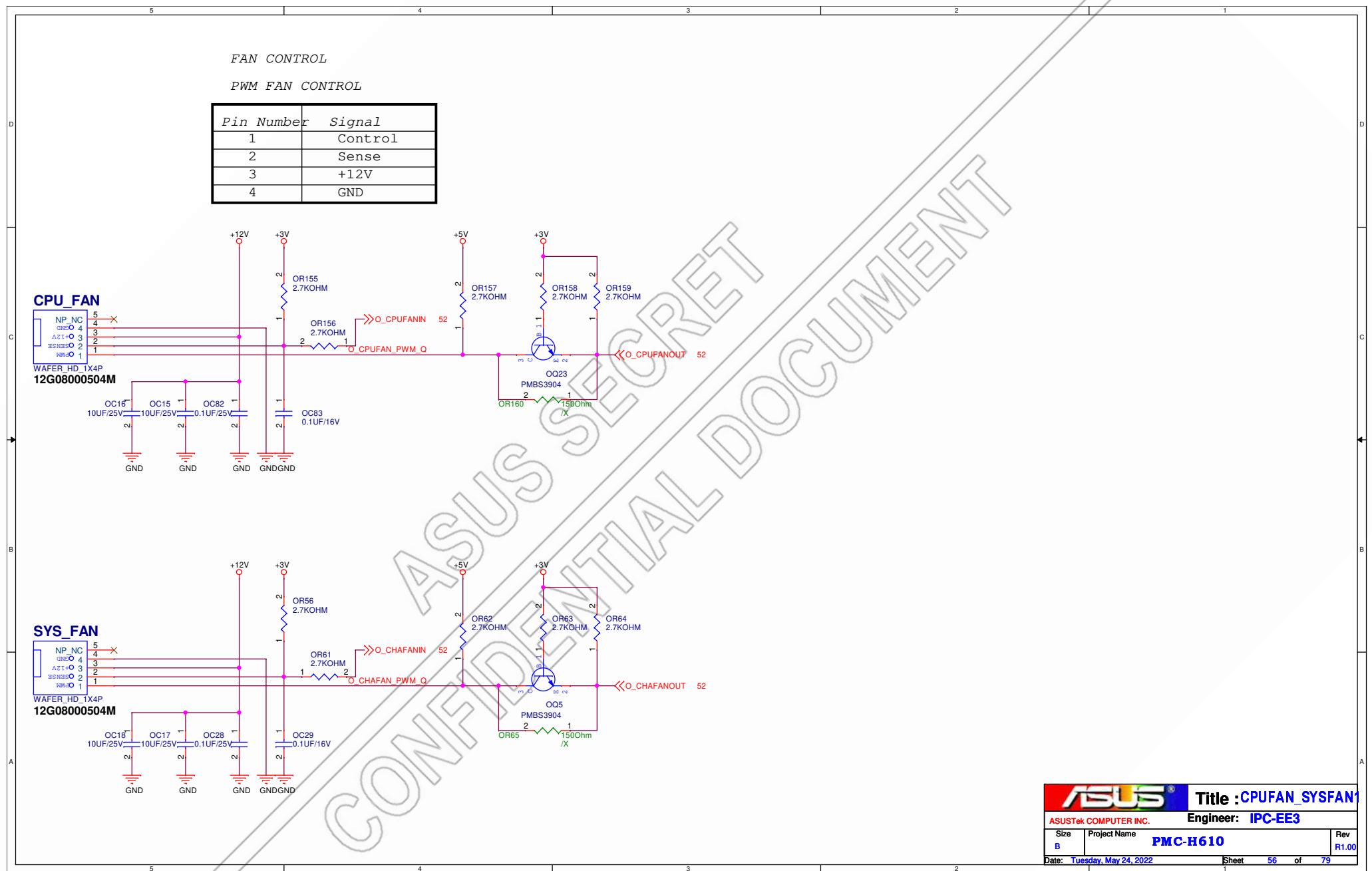
Title : Intrudor(CASEOPEN)

Engineer: IPC-EE3

Size	Project Name	Rev
A	PMC-H610	R1.00
Date: Tuesday, May 24, 2022	Sheet 53 of 79	







Title : CPUFAN\_SYSFAN1

Engineer: IPC-EE3

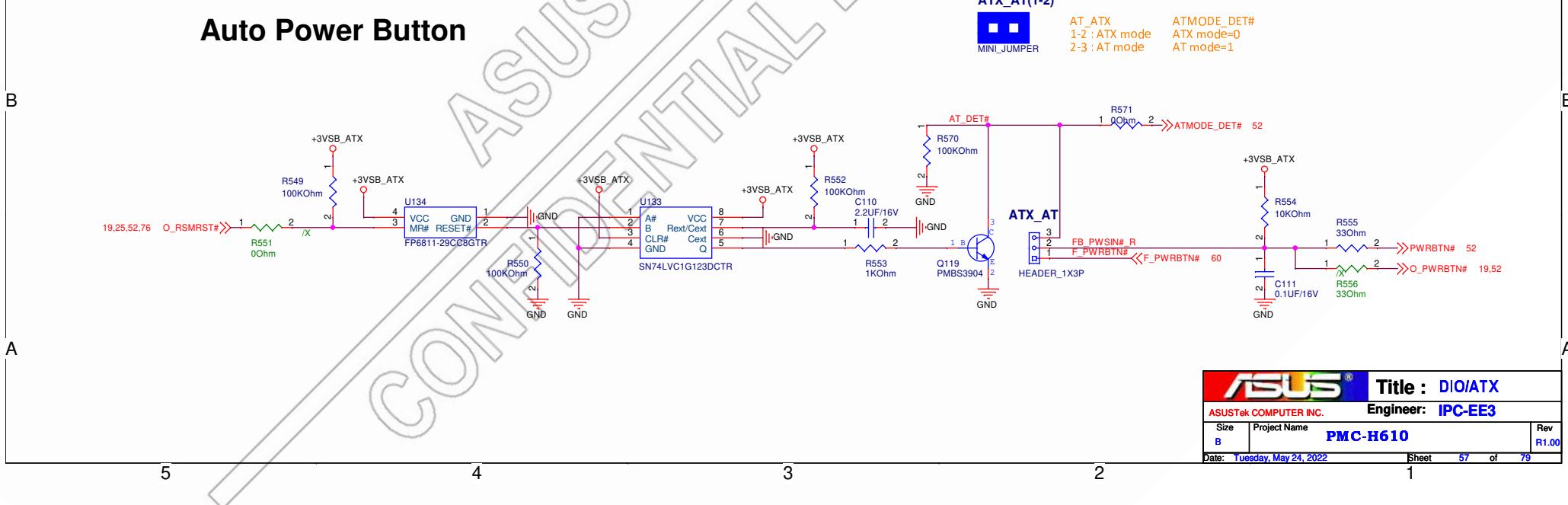
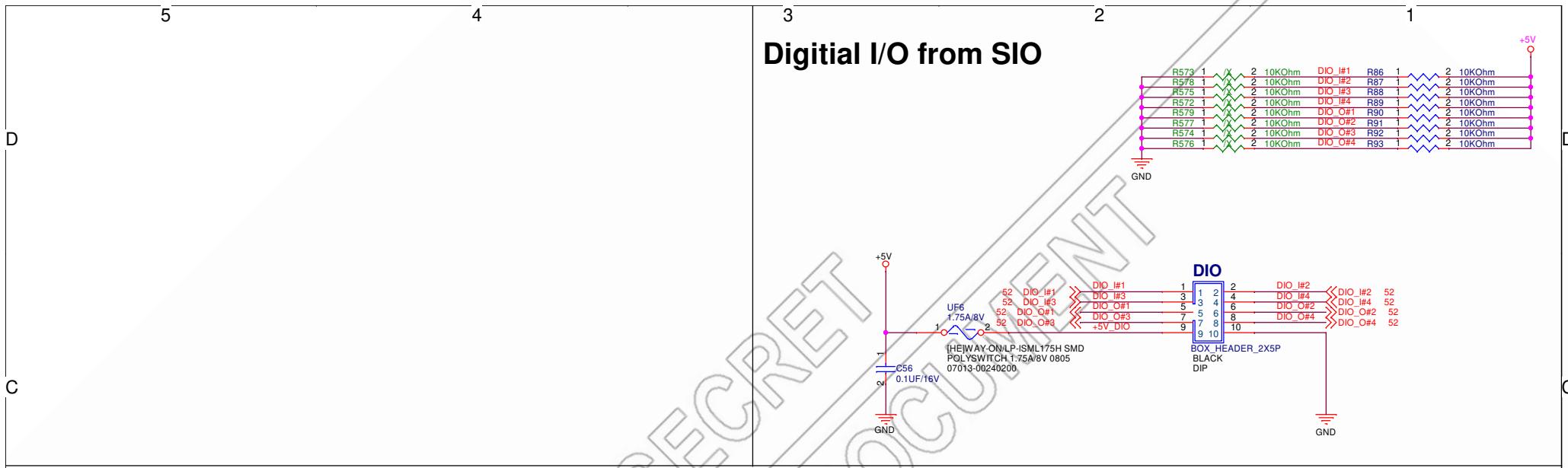
Size	Project Name	Rev
B	PMC-H610	R1.00

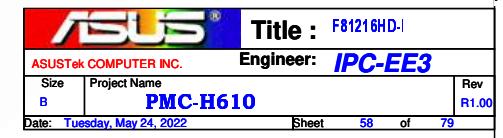
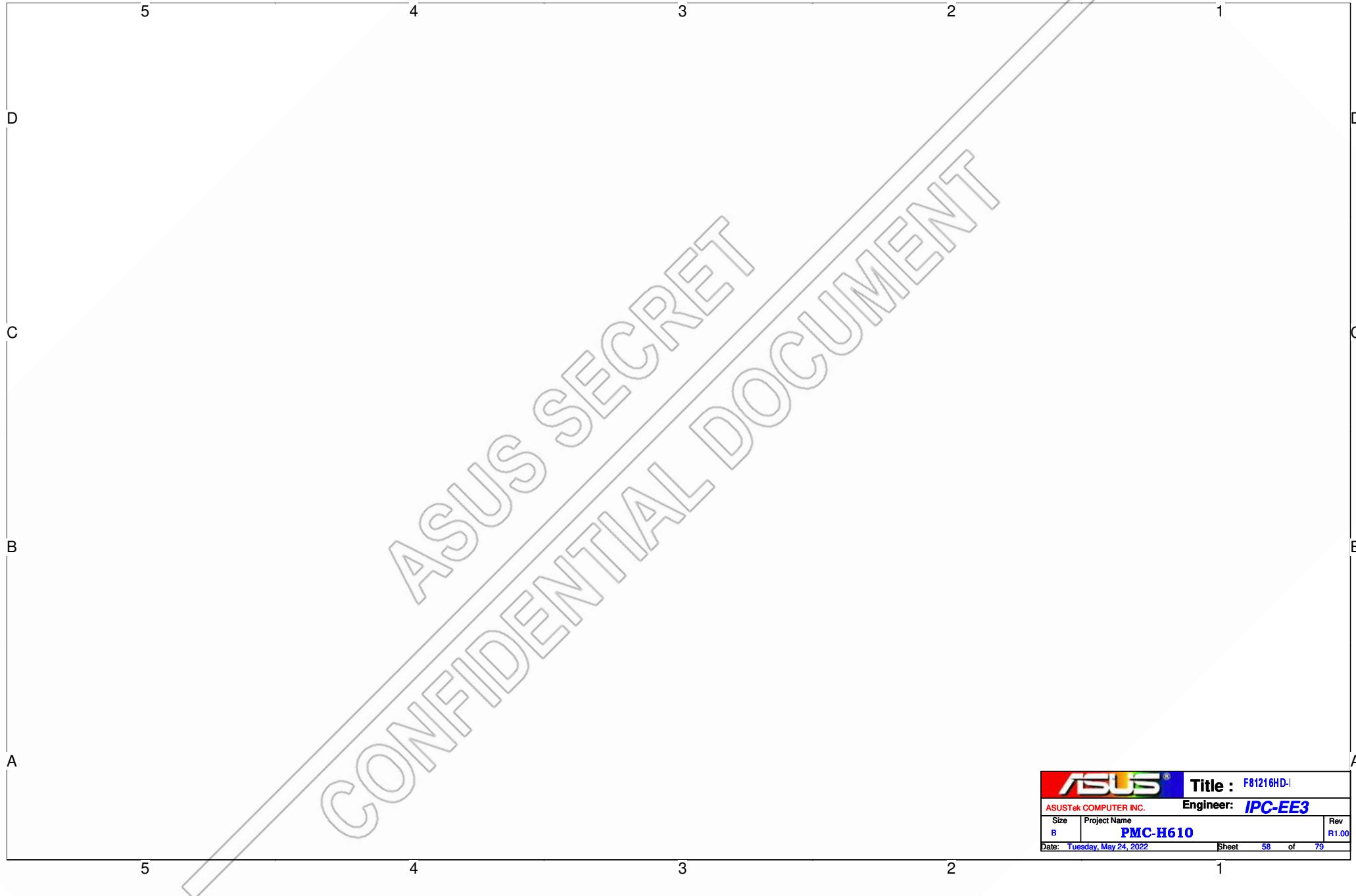
Date: Tuesday, May 24, 2022

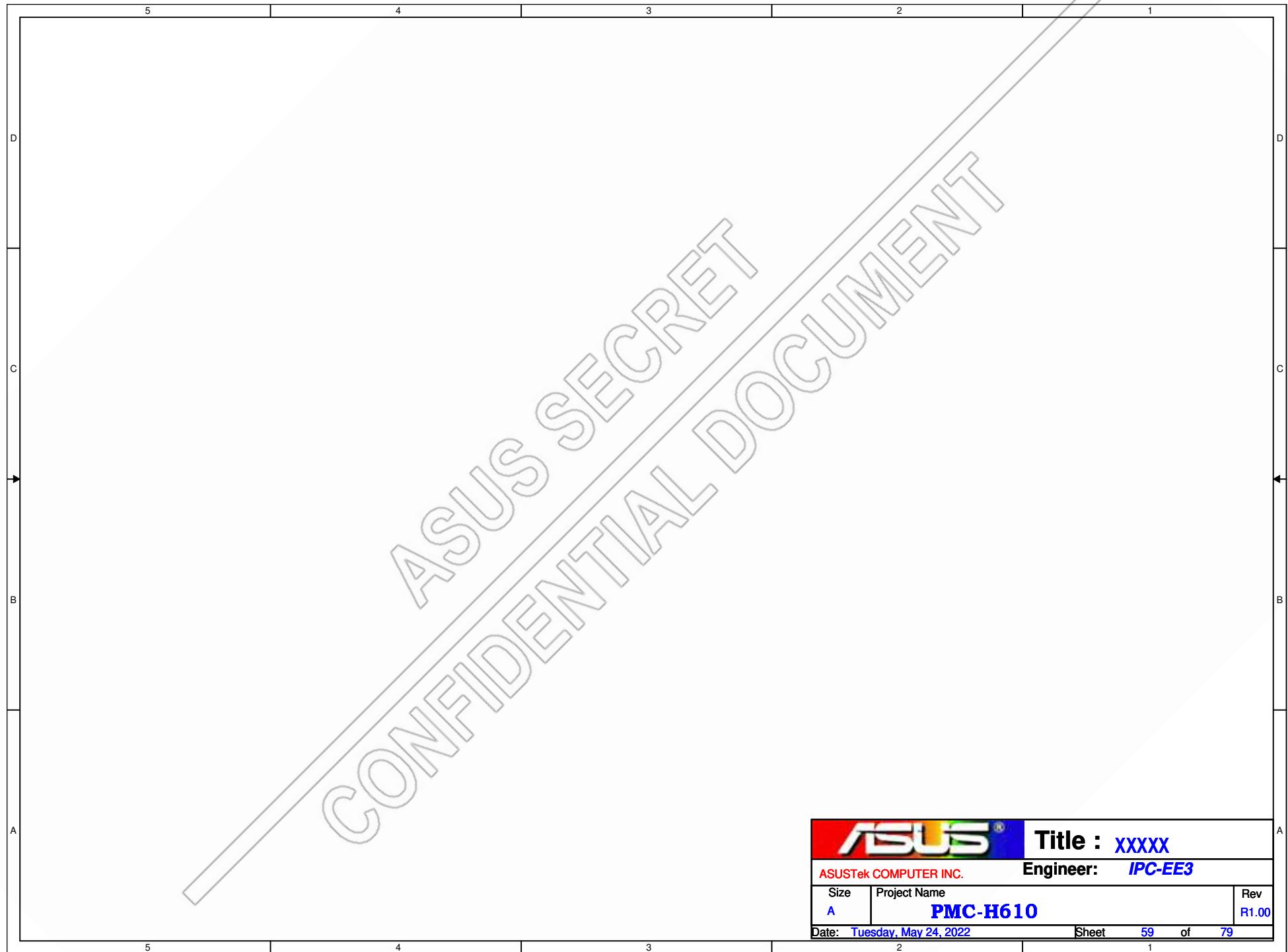
Sheet

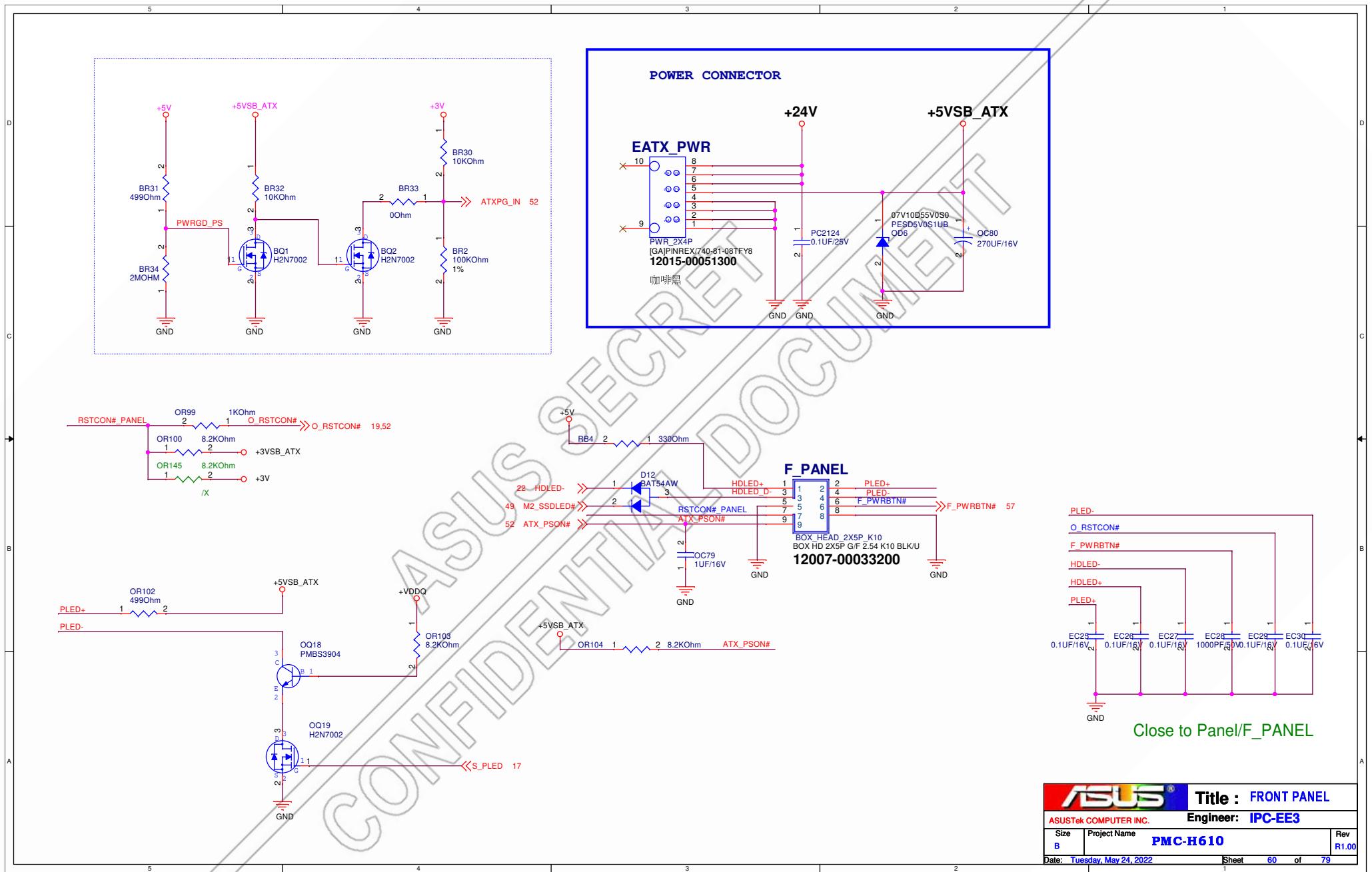
1

of 79









Title : FRONT PANEL	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3
Size B	Project Name <b>PMC-H610</b>
Date: Tuesday, May 24, 2022	Rev R1.00



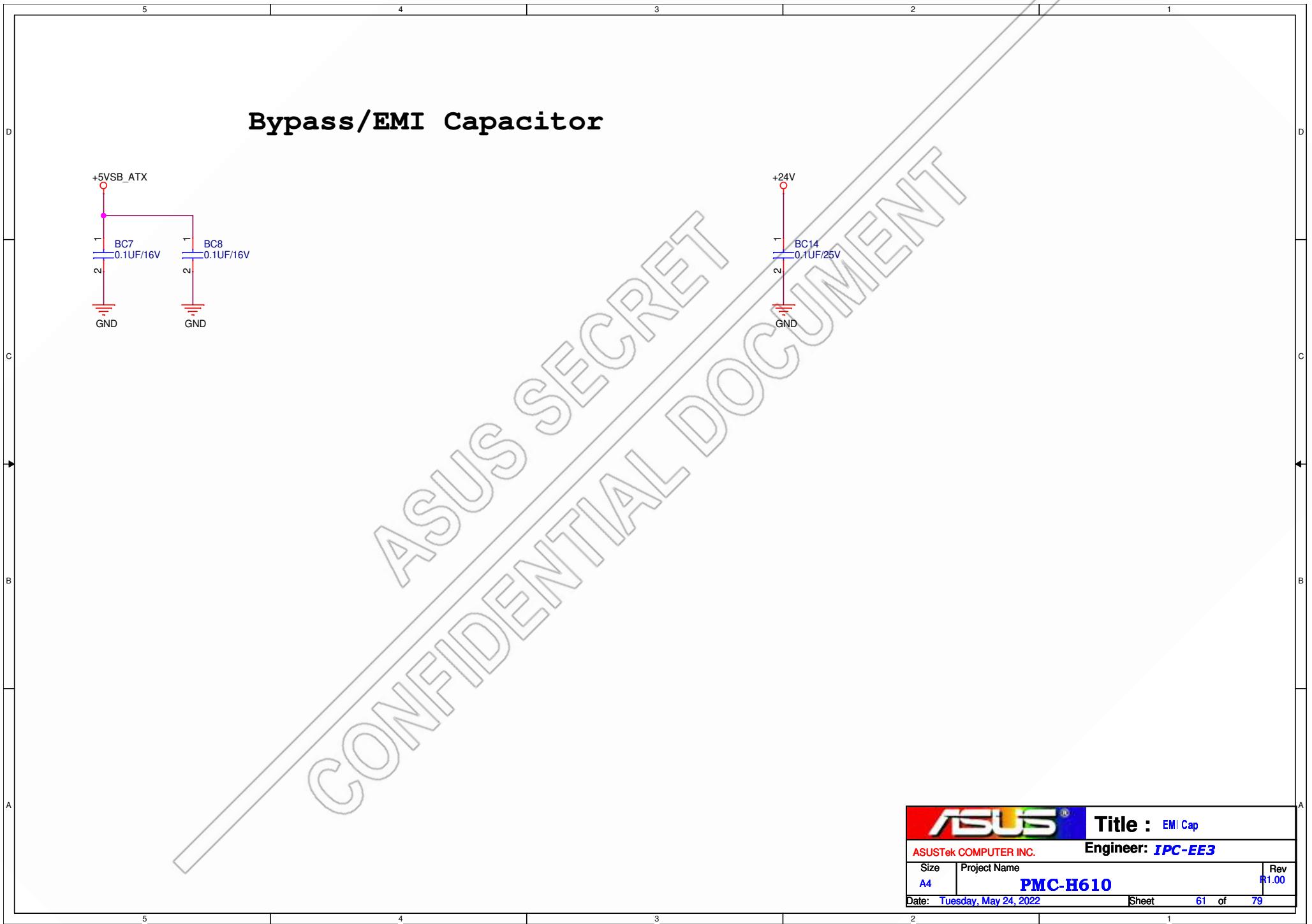
Title : FRONT PANEL

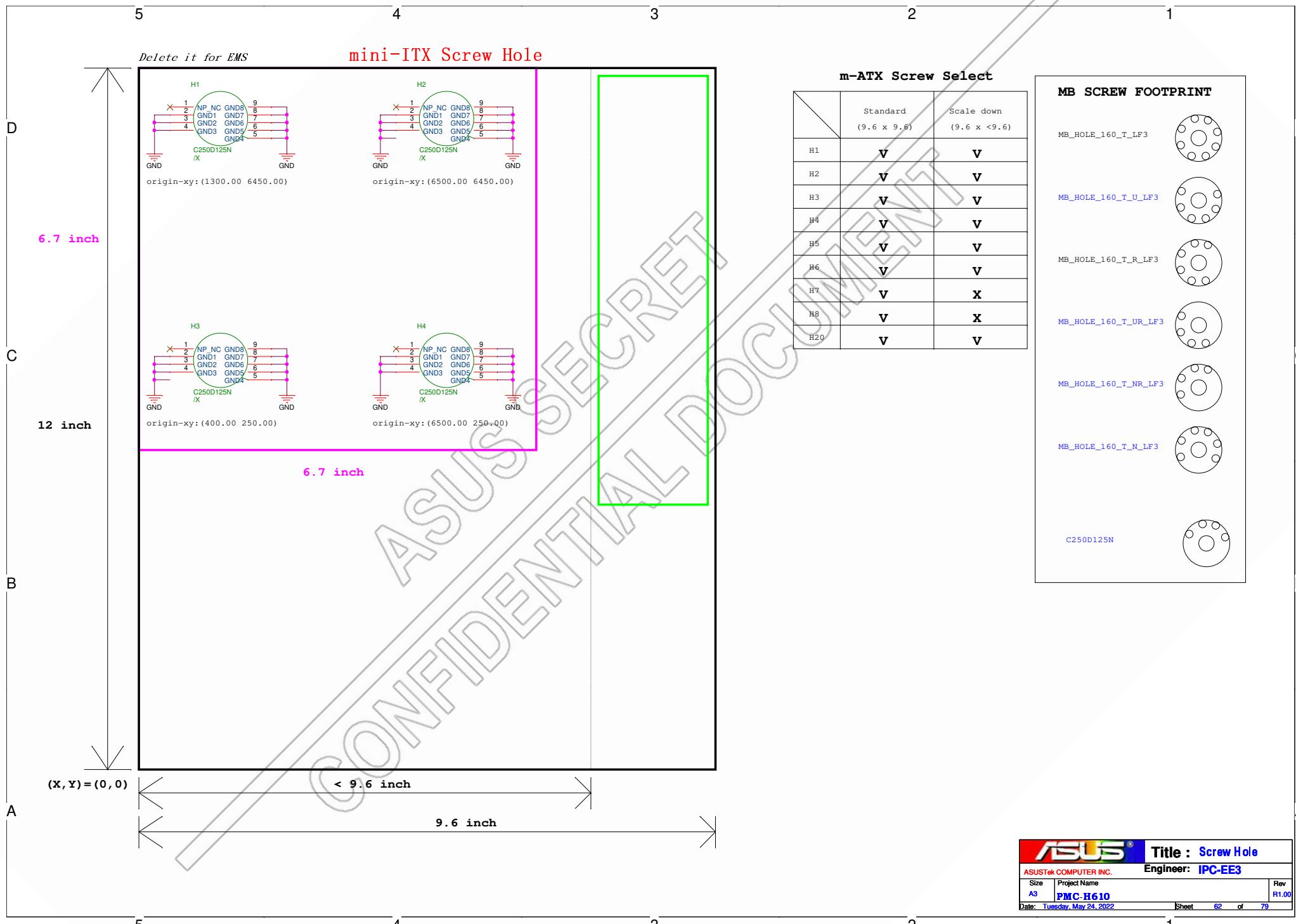
Engineer: IPC-EE3

Size B Project Name **PMC-H610**

Date: Tuesday, May 24, 2022 Rev R1.00

Sheet 1 of 79





# Selling Point

## Logo

common Logo for all projects



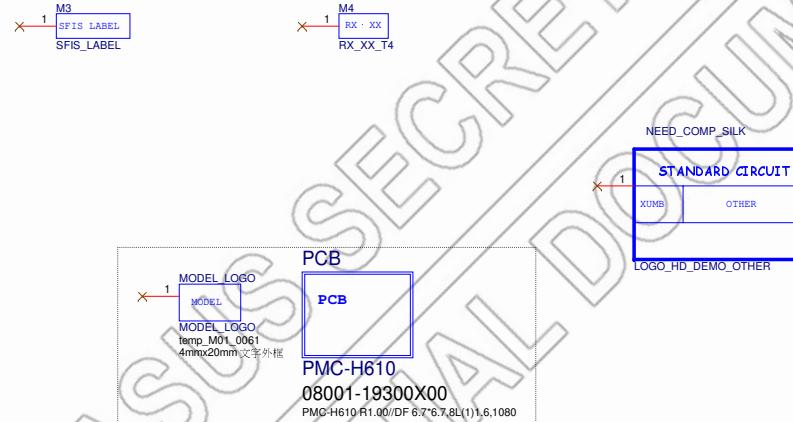
LOGO2  
FCC  
FCC



LOGO5  
WEEE\_LOGO  
WEEE\_LOGO

LOGO6  
CE  
CE

LOGO7  
PCB MADE IN CHINA  
PCB\_MADE\_IN\_CHINA



### PMC-H610 R1.00 PCB-08 :

R1.00 PCB\_DF : 08001-19300Q00 // DF 6.7\*6.7,8L(1)1.6,1080

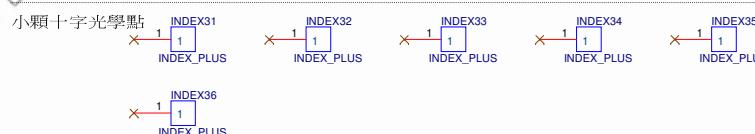
R1.00 PCB\_GECS : 08001-19300100 // GECS 6.7\*6.7,8L(1)1.6,1080

R1.00 PCB\_TRUSTECH : 08001-19300200 // TRUSTECH 6.7\*6.7,8L(1)1.6,1080

## Fiducial Mask (光學點)

大顆十字光學點

光學點需要 6 ~ 10 顆,  
LayoutRD會依空間大小及版本需求  
擺放所需的光學點  
所以兩種光學點都需畫入線路中,  
最後再做刪除。



2012/09/11

Title : Selling Point_Logo			
ASUSTek COMPUTER INC.			
Size	Project Name	Engineer:	IPC-EE3
A3	PMC-H610		Rev
			R1.00
Date: Tuesday, May 24, 2022	Sheet	63	of 79