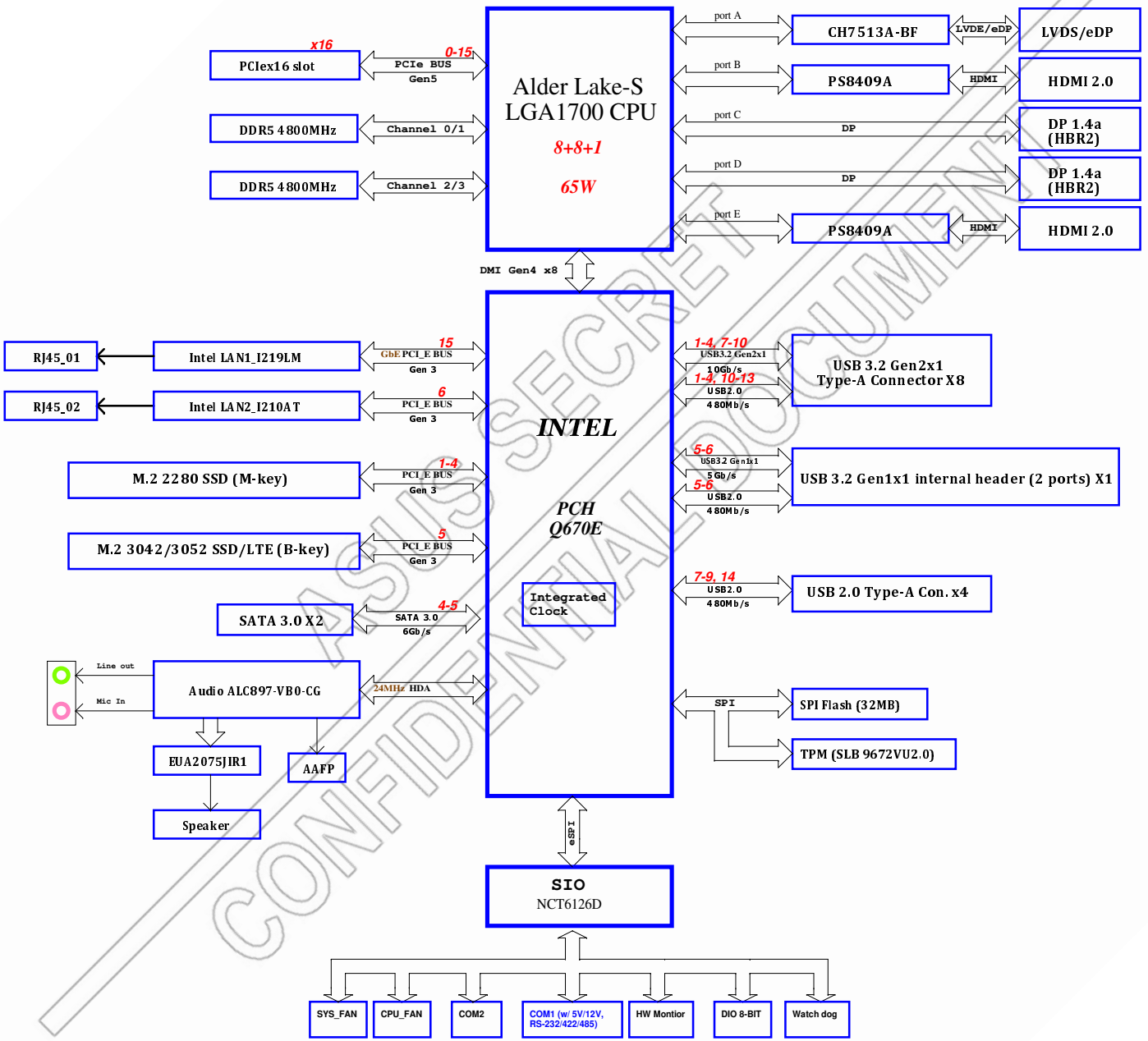
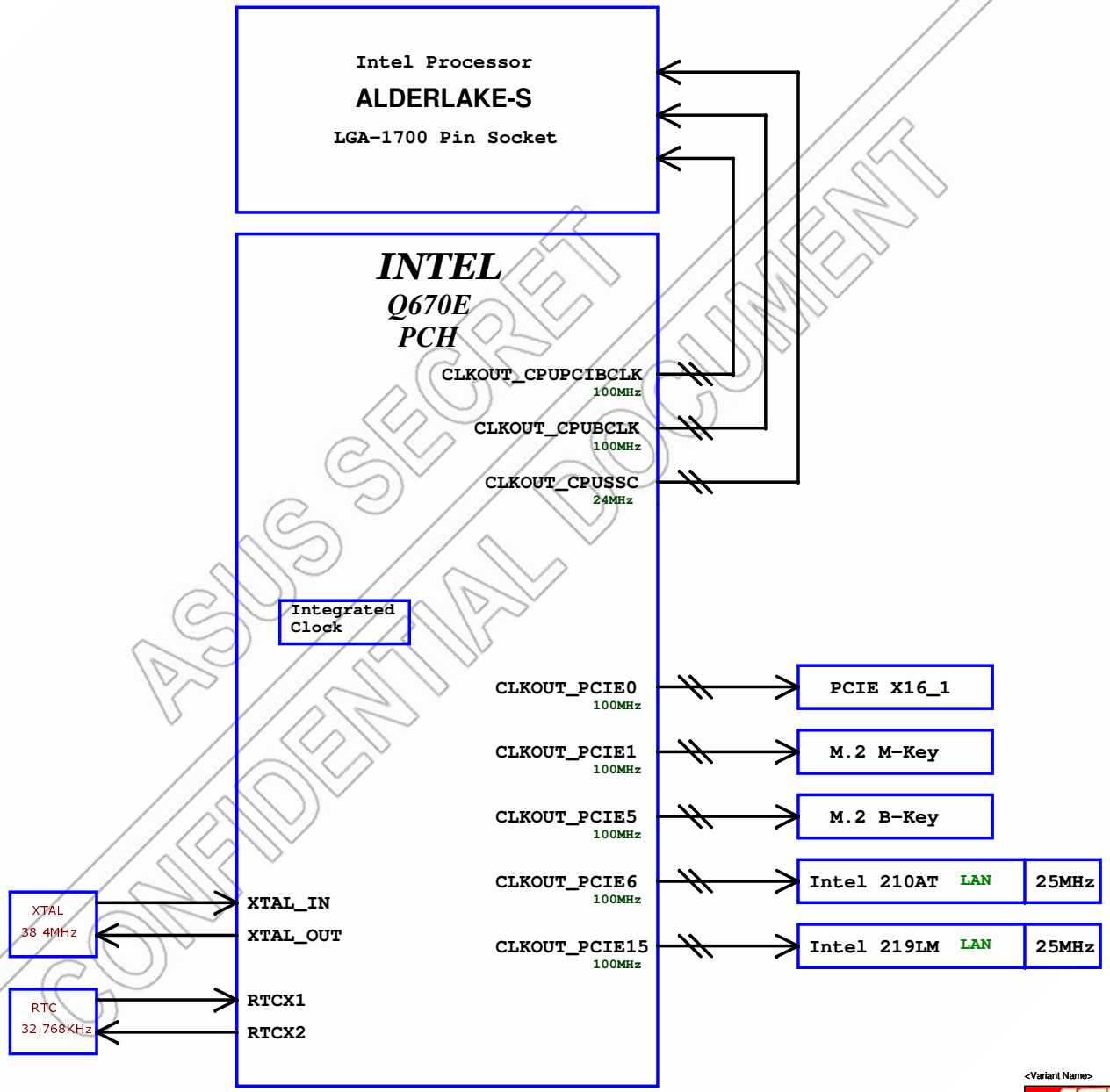
MIX-Q670A1
Block Diagram Rev 1.00



ASUS SECRET
CONFIDENTIAL DOCUMENT

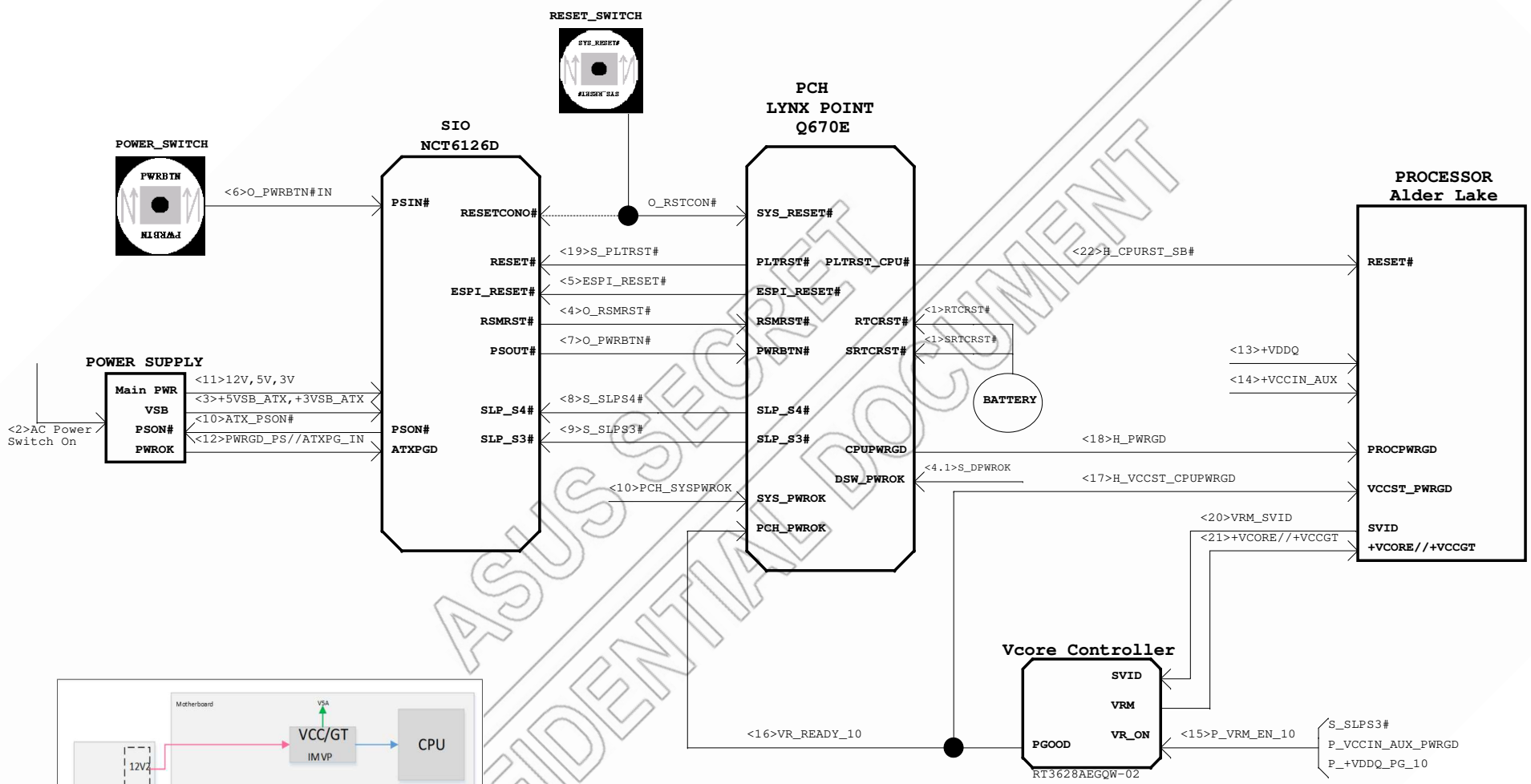
ASUS	Title : Block Diagram		
ASUSTeK COMPUTER INC.	Engineer: IPC-EE3		
Size A2	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 1 of 77		



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS	Title : Clock Distribution	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 2 of 77	



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS

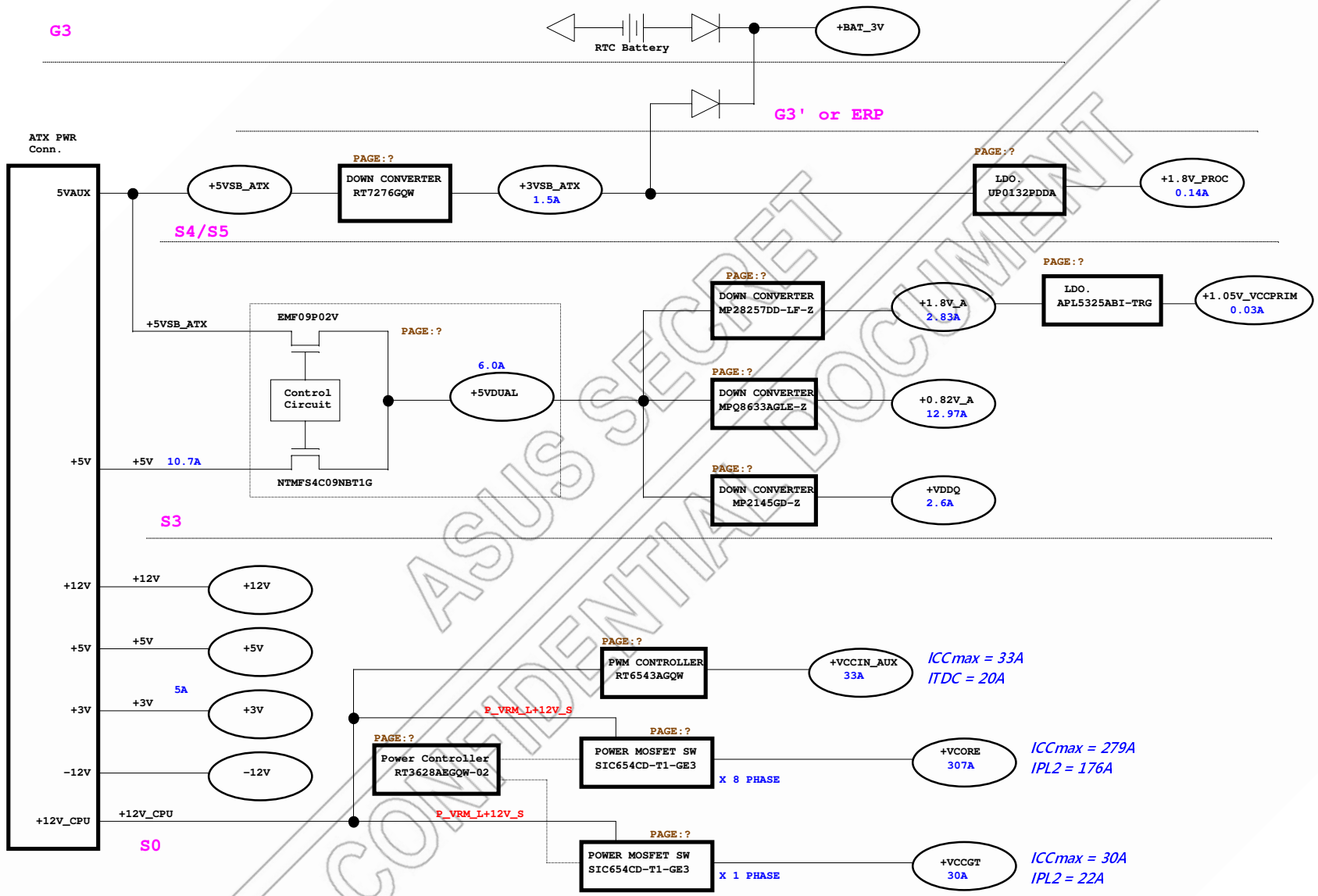
ASUSTek COMPUTER INC.

Title : Signal & Reset map

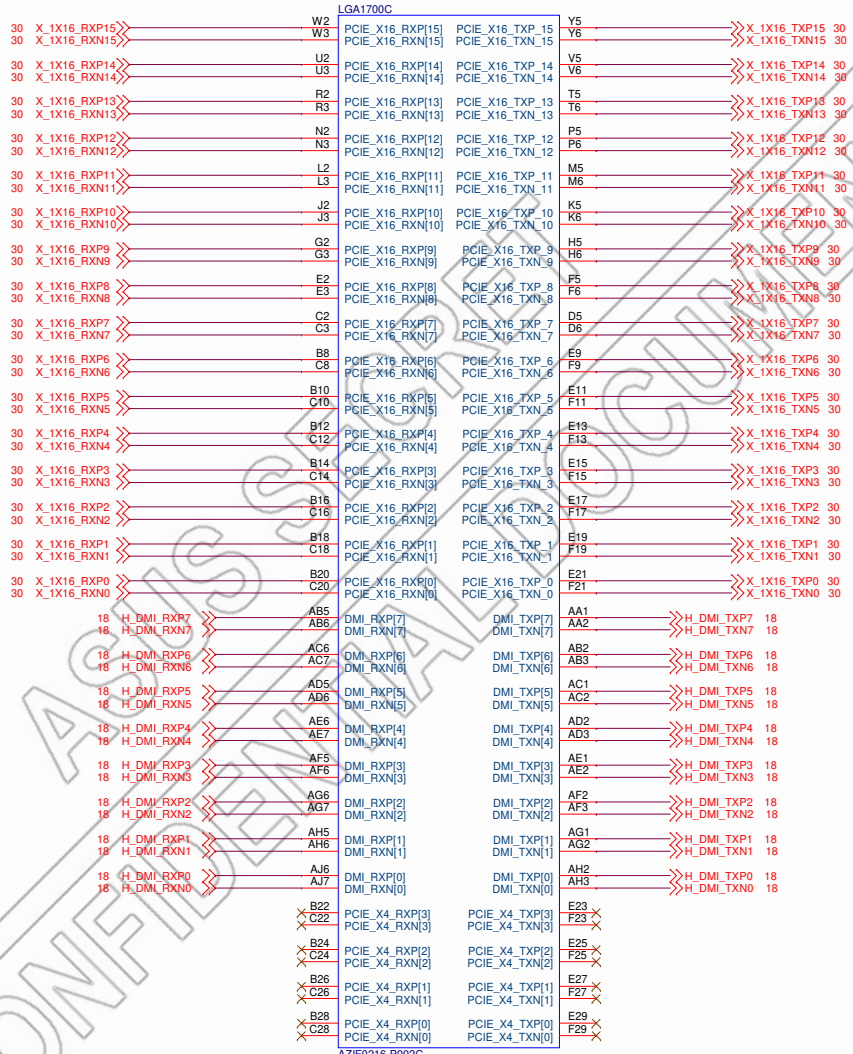
Engineer: IPC-EE3

Size	Project Name	Rev
A3	MIX-Q670A1	R1.00

Date: Monday, July 18, 2022 Sheet 3 of 77



ASUS SECRET
CONFIDENTIAL DOCUMENT



LOTES/AZIF0216-P002C

12001-00300200

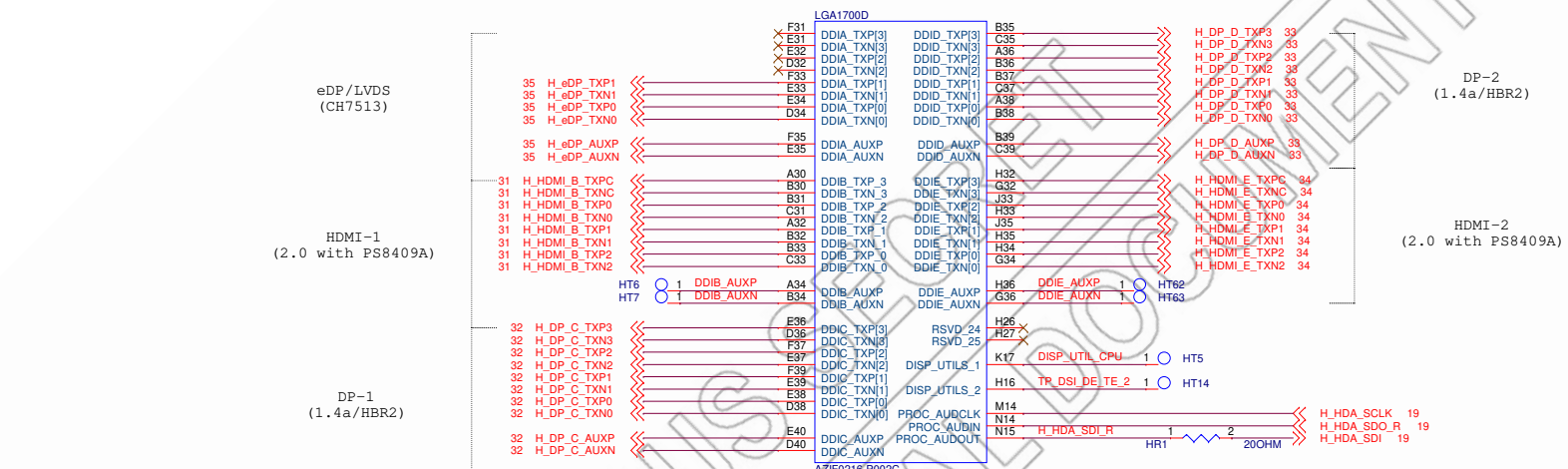
LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : LGA1700 (DMI/PCIE)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 5 of 77		



12001-00300200

LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title: LGA1700 (DISPLAY)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: A3	Project Name: MIX-Q670A1		Rev: R1.00
Date: Monday, July 18, 2022	Sheet 6 of 77		

Channel 0/1
6 Layer routing

DDR4(IL) / DDR4(NIL) / DDR5 DDR4 / DDR5

LGA1700A

13 D5_DDR1_DQ3[0:7]	D5_DDR1_DQ34 AM2	DDR0_DQ7[7]/DDR1_DQ5[7]	/DDR1_DQ3[7]	DDR0_CLKP3/DDR1_CLKP0	BC22 D5_DDR1_CLK0 13
	D5_DDR1_DQ35 AL2	DDR0_DQ7[6]/DDR1_DQ5[6]	/DDR1_DQ3[6]	DDR0_CLKN3/DDR1_CLKN0	BB22 D5_DDR1_CLK#0 13
	D5_DDR1_DQ36 AL3	DDR0_DQ7[5]/DDR1_DQ5[5]	/DDR1_DQ3[5]	DDR0_CLKP2/DDR1_CLKP1	BD23 D5_DDR1_CLK1 13
	D5_DDR1_DQ37 AL4	DDR0_DQ7[4]/DDR1_DQ5[4]	/DDR1_DQ3[4]	DDR0_CLKN2/DDR1_CLKN1	BC23 D5_DDR1_CLK#1 13
	D5_DDR1_DQ32 AP2	DDR0_DQ7[3]/DDR1_DQ5[3]	/DDR1_DQ3[3]	DDR0_CLKP1/DDR0_CLKP1	BC28 D5_DDR0_CLK1 13
	D5_DDR1_DQ31 AN2	DDR0_DQ7[2]/DDR1_DQ5[2]	/DDR1_DQ3[2]	DDR0_CLKN1/DDR0_CLKN1	BB28 D5_DDR0_CLK#1 13
	D5_DDR1_DQ33 AP4	DDR0_DQ7[1]/DDR1_DQ5[1]	/DDR1_DQ3[1]	DDR0_CLKP0/DDR0_CLKP0	BD29 D5_DDR0_CLK0 13
13 D5_DDR1_DQ2[0:7]	D5_DDR1_DQ30 AP3	DDR0_DQ7[0]/DDR1_DQ5[0]	/DDR1_DQ3[0]	DDR0_CLKN0/DDR0_CLKN0	BC29 D5_DDR0_CLK#0 13
	D5_DDR1_DQ24 AU2	DDR0_DQ6[7]/DDR1_DQ4[7]	/DDR1_DQ2[7]		
	D5_DDR1_DQ26 AT2	DDR0_DQ6[6]/DDR1_DQ4[6]	/DDR1_DQ2[6]	DDR0_CKE3/NC	BD37
	D5_DDR1_DQ25 AT4	DDR0_DQ6[5]/DDR1_DQ4[5]	/DDR1_DQ2[5]	DDR0_CKE2/DDR0_CS1	BB36 D5_DDR0_CS#1 13
	D5_DDR1_DQ27 AT3	DDR0_DQ6[4]/DDR1_DQ4[4]	/DDR1_DQ2[4]	DDR0_CKE1/DDR0_CS3	BA37
	D5_DDR1_DQ23 AW2	DDR0_DQ6[3]/DDR1_DQ4[3]	/DDR1_DQ2[3]	DDR0_CKE0/DDR0_CS0	BC36 D5_DDR0_CS#0 13
	D5_DDR1_DQ21 AV2	DDR0_DQ6[2]/DDR1_DQ4[2]	/DDR1_DQ2[2]		
	D5_DDR1_DQ20 AW4	DDR0_DQ6[1]/DDR1_DQ4[1]	/DDR1_DQ2[1]	DDR0_CS3/DDR1_CS0	BD15 D5_DDR1_CS#0 13
	D5_DDR1_DQ22 AW3	DDR0_DQ6[0]/DDR1_DQ4[0]	/DDR1_DQ2[0]	DDR0_CS2/DDR1_CA5	BB18 D5_DDR1_CS#1 13
13 D5_DDR1_DQ1[0:7]	D5_DDR1_DQ14 BA2	DDR0_DQ5[7]/DDR1_DQ1[7]	/DDR1_DQ1[7]	DDR0_CS1/DDR1_CA0	BB16 D5_DDR1_CA5 13
	D5_DDR1_DQ16 BA1	DDR0_DQ5[6]/DDR1_DQ1[6]	/DDR1_DQ1[6]	DDR0_CS0/DDR1_CA6	BC18 D5_DDR1_CA0 13
	D5_DDR1_DQ17 BA3	DDR0_DQ5[5]/DDR1_DQ1[5]	/DDR1_DQ1[5]		D5_DDR1_CA6 13
	D5_DDR1_DQ15 BB2	DDR0_DQ5[4]/DDR1_DQ1[4]	/DDR1_DQ1[4]	DDR0_ODT3/NC	BB14
	D5_DDR1_DQ13 BC4	DDR0_DQ5[3]/DDR1_DQ1[3]	/DDR1_DQ1[3]	DDR0_ODT2/DDR1_CA1	BC16 D5_DDR1_CA1 13
	D5_DDR1_DQ11 BB5	DDR0_DQ5[2]/DDR1_DQ1[2]	/DDR1_DQ1[2]	DDR0_ODT1/DDR1_CS1	BA16 D5_DDR1_CS#1 13
	D5_DDR1_DQ12 BD4	DDR0_DQ5[1]/DDR1_DQ1[1]	/DDR1_DQ1[1]	DDR0_ODT0/DDR1_CA3	BD17 D5_DDR1_CA3 13
	D5_DDR1_DQ10 BC5	DDR0_DQ5[0]/DDR1_DQ1[0]	/DDR1_DQ1[0]		
13 D5_DDR1_DQ0[0:7]	D5_DDR1_DQ05 BA7	DDR0_DQ4[7]/DDR1_DQ0[7]	/DDR1_DQ0[7]	DDR0_BA1/DDR1_CA11	BC20 D5_DDR1_CA11 13
	D5_DDR1_DQ06 BC7	DDR0_DQ4[6]/DDR1_DQ0[6]	/DDR1_DQ0[6]	DDR0_BA0/DDR1_CA9	BA20 D5_DDR1_CA9 13
	D5_DDR1_DQ04 BC8	DDR0_DQ4[5]/DDR1_DQ0[5]	/DDR1_DQ0[5]		
	D5_DDR1_DQ07 BB7	DDR0_DQ4[4]/DDR1_DQ0[4]	/DDR1_DQ0[4]	DDR0_BG1/DDR0_CA2	BC35 D5_DDR0_CA2 13
	D5_DDR1_DQ02 BB10	DDR0_DQ4[3]/DDR1_DQ0[3]	/DDR1_DQ0[3]	DDR0_BG0/DDR0_CA1	BD35 D5_DDR0_CA1 13
	D5_DDR1_DQ00 BA10	DDR0_DQ4[2]/DDR1_DQ0[2]	/DDR1_DQ0[2]		
	D5_DDR1_DQ03 BC10	DDR0_DQ4[1]/DDR1_DQ0[1]	/DDR1_DQ0[1]	DDR0_MA16/DDR1_CA8	BD19 D5_DDR1_CA8 13
	D5_DDR1_DQ01 BC9	DDR0_DQ4[0]/DDR1_DQ0[0]	/DDR1_DQ0[0]	DDR0_MA15/DDR1_CA4	BA18 D5_DDR1_CA4 13
13 D5_DDR0_DQ3[0:7]	D5_DDR0_DQ37 BC45	DDR0_DQ3[7]/DDR0_DQ5[7]	/DDR0_DQ3[7]	DDR0_MA14/DDR1_CA7	BC19 D5_DDR1_CA7 13
	D5_DDR0_DQ35 BC44	DDR0_DQ3[6]/DDR0_DQ5[6]	/DDR0_DQ3[6]	DDR0_MA13/DDR1_CA2	BC17 D5_DDR1_CA2 13
	D5_DDR0_DQ36 BA44	DDR0_DQ3[5]/DDR0_DQ5[5]	/DDR0_DQ3[5]	DDR0_MA12/DDR0_CA3	BC34 D5_DDR0_CA3 13
	D5_DDR0_DQ34 BB44	DDR0_DQ3[4]/DDR0_DQ5[4]	/DDR0_DQ3[4]	DDR0_MA11/DDR0_CA5	BA33 D5_DDR0_CA5 13
	D5_DDR0_DQ32 BC47	DDR0_DQ3[3]/DDR0_DQ5[3]	/DDR0_DQ3[3]	DDR0_MA10/DDR1_CA10	BB20 D5_DDR1_CA10 13
	D5_DDR0_DQ31 BC46	DDR0_DQ3[2]/DDR0_DQ5[2]	/DDR0_DQ3[2]	DDR0_MA9/DDR0_CA4	BB34 D5_DDR0_CA4 13
	D5_DDR0_DQ33 BB47	DDR0_DQ3[1]/DDR0_DQ5[1]	/DDR0_DQ3[1]	DDR0_MA8/DDR0_CA7	BC33 D5_DDR0_CA7 13
	D5_DDR0_DQ30 BA47	DDR0_DQ3[0]/DDR0_DQ5[0]	/DDR0_DQ3[0]	DDR0_MA7/DDR0_CA6	BD33 D5_DDR0_CA6 13
13 D5_DDR0_DQ2[0:7]	D5_DDR0_DQ25 BC49	DDR0_DQ2[7]/DDR0_DQ4[7]	/DDR0_DQ2[7]	DDR0_MA6/DDR0_CA8	BC32 D5_DDR0_CA8 13
	D5_DDR0_DQ27 BD49	DDR0_DQ2[6]/DDR0_DQ4[6]	/DDR0_DQ2[6]	DDR0_MA5/DDR0_CA9	BB32 D5_DDR0_CA9 13
	D5_DDR0_DQ24 BC50	DDR0_DQ2[5]/DDR0_DQ4[5]	/DDR0_DQ2[5]	DDR0_MA4/DDR0_CA10	BA31 D5_DDR0_CA10 13
	D5_DDR0_DQ26 BB49	DDR0_DQ2[4]/DDR0_DQ4[4]	/DDR0_DQ2[4]	DDR0_MA3/DDR0_CA11	BD31 D5_DDR0_CA11 13
	D5_DDR0_DQ22 BA52	DDR0_DQ2[3]/DDR0_DQ4[3]	/DDR0_DQ2[3]	DDR0_MA2/NC	BC30
	D5_DDR0_DQ21 BA51	DDR0_DQ2[2]/DDR0_DQ4[2]	/DDR0_DQ2[2]	DDR0_MA1/DDR0_CA12	BC31 D5_DDR0_CA12 13
	D5_DDR0_DQ20 AY51	DDR0_DQ2[1]/DDR0_DQ4[1]	/DDR0_DQ2[1]	DDR0_MA0/DDR1_CA12	BC21 D5_DDR1_CA12 13
	D5_DDR0_DQ23 AY50	DDR0_DQ2[0]/DDR0_DQ4[0]	/DDR0_DQ2[0]		
13 D5_DDR0_DQ1[0:7]	D5_DDR0_DQ15 AV50	DDR0_DQ1[7]/DDR0_DQ1[7]	/DDR0_DQ1[7]	DDR0_ACT#/DDR0_CA0	BA35 BD21 D5_DDR0_CA0 13
	D5_DDR0_DQ17 AV49	DDR0_DQ1[6]/DDR0_DQ1[6]	/DDR0_DQ1[6]	DDR0_PAR/NC	AP25
	D5_DDR0_DQ14 AU51	DDR0_DQ1[5]/DDR0_DQ1[5]	/DDR0_DQ1[5]	DDR0_ALERT#	DDR0_ALERT# 13
	D5_DDR0_DQ16 AV51	DDR0_DQ1[4]/DDR0_DQ1[4]	/DDR0_DQ1[4]	DDR4(IL) / DDR4(NIL) / DDR5	AM4
	D5_DDR0_DQ12 AR50	DDR0_DQ1[3]/DDR0_DQ1[3]	/DDR0_DQ1[3]	DDR0_DQSP7/ DDR1_DQSP5/DDR1_DQSP3	AN4 D5_DDR1_DQS3 13
	D5_DDR0_DQ13 AR49	DDR0_DQ1[2]/DDR0_DQ1[2]	/DDR0_DQ1[2]	DDR0_DQSN7/ DDR1_DQSN5/DDR1_DQSN3	AU4 D5_DDR1_DQS#3 13
	D5_DDR0_DQ10 AR51	DDR0_DQ1[1]/DDR0_DQ1[1]	/DDR0_DQ1[1]	DDR0_DQSP6/ DDR1_DQSP4/DDR1_DQSP2	AV4 D5_DDR1_DQS2 13
	D5_DDR0_DQ11 AT51	DDR0_DQ1[0]/DDR0_DQ1[0]	/DDR0_DQ1[0]	DDR0_DQSN6/ DDR1_DQSN4/DDR1_DQSN2	BA4 D5_DDR1_DQS#2 13
13 D5_DDR0_DQ0[0:7]	D5_DDR0_DQ06 AN50	DDR0_DQ0[7]/DDR0_DQ0[7]	/DDR0_DQ0[7]	DDR0_DQSP5/ DDR1_DQSP1/DDR1_DQSP1	BA5 D5_DDR1_DQS1 13
	D5_DDR0_DQ04 AN49	DDR0_DQ0[6]/DDR0_DQ0[6]	/DDR0_DQ0[6]	DDR0_DQSN5/ DDR1_DQSN1/DDR1_DQSN1	BA8 D5_DDR1_DQS#1 13
	D5_DDR0_DQ05 AM51	DDR0_DQ0[5]/DDR0_DQ0[5]	/DDR0_DQ0[5]	DDR0_DQSP4/ DDR1_DQSP0/DDR1_DQSP0	BA9 D5_DDR1_DQS0 13
	D5_DDR0_DQ07 AN51	DDR0_DQ0[4]/DDR0_DQ0[4]	/DDR0_DQ0[4]	DDR0_DQSN4/ DDR1_DQSN0/DDR1_DQSN0	BA45 D5_DDR1_DQS#0 13
	D5_DDR0_DQ00 AK50	DDR0_DQ0[3]/DDR0_DQ0[3]	/DDR0_DQ0[3]	DDR0_DQSP3/ DDR0_DQSP5/DDR0_DQSP3	BA46 D5_DDR0_DQS3 13
	D5_DDR0_DQ02 AK49	DDR0_DQ0[2]/DDR0_DQ0[2]	/DDR0_DQ0[2]	DDR0_DQSN3/ DDR0_DQSN5/DDR0_DQSN3	BA49 D5_DDR0_DQS#3 13
	D5_DDR0_DQ01 AK51	DDR0_DQ0[1]/DDR0_DQ0[1]	/DDR0_DQ0[1]	DDR0_DQSP2/ DDR0_DQSP4/DDR0_DQSP2	AY49 D5_DDR0_DQS2 13
	D5_DDR0_DQ03 AL51	DDR0_DQ0[0]/DDR0_DQ0[0]	/DDR0_DQ0[0]	DDR0_DQSN2/ DDR0_DQSN4/DDR0_DQSN2	AU49 D5_DDR0_DQS#2 13
				DDR0_DQSP1/ DDR0_DQSP1/DDR0_DQSP1	AT49 D5_DDR0_DQS1 13
	BC40			DDR0_DQSN1/ DDR0_DQSN1/DDR0_DQSN1	AM49 D5_DDR0_DQS#1 13
	BC39	DDR0_DQ8[7]/DDR0_DQ8[7]/NC		DDR0_DQSP0/ DDR0_DQSP0/DDR0_DQSP0	AL49 D5_DDR0_DQS0 13
	BA39	DDR0_DQ8[6]/DDR0_DQ8[6]/NC		DDR0_DQSN0/ DDR0_DQSN0/DDR0_DQSN0	D5_DDR0_DQS#0 13
	BB39	DDR0_DQ8[5]/DDR0_DQ8[5]/NC			
	BC42	DDR0_DQ8[4]/DDR0_DQ8[4]/NC			BA40
	BC41	DDR0_DQ8[3]/DDR0_DQ8[3]	/DDR0_DQ4[3]	DDR0_DQSP8/ DDR0_DQSP4	BA41
	BA42	DDR0_DQ8[2]/DDR0_DQ8[2]	/DDR0_DQ4[2]	DDR0_DQSN8/ DDR0_DQSN4	
	BB42	DDR0_DQ8[1]/DDR0_DQ8[1]	/DDR0_DQ4[1]		BC13
		DDR0_DQ8[0]/DDR0_DQ8[0]	/DDR0_DQ4[0]	NC/NC/DDR1_DQSP4	BD13
	BA13			NC/NC/DDR1_DQSN4	
	BA12	NC/NC/DDR1_DQ4[3]			AU20
	BC12	NC/NC/DDR1_DQ4[2]		NC/DDR3_CS3	AV20
	BB12	NC/NC/DDR1_DQ4[1]		NC/DDR3_CS2	AW33
		NC/NC/DDR1_DQ4[0]		NC/DDR2_CS2	BA15
				NC/DDR1_CS3	BC15
	AH50			NC/DDR1_CS2	BC37
	AH52	DDR_VREF_CA1	NP_NC1	NC/DDR0_CS2	
		DDR_VREF_CA0	NP_NC2		
			NP_NC3		
			NP_NC4		
			NP_NC5		
			NP_NC6		
			NP_NC7		
			NP_NC8		

AZIF0216-P002C
LOTES/AZIF0216-P002C
12001-00300200

1 2 3 4 5 6 7 8

LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300200 LOTES/AZIF0216-P002C
2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

CONFIDENTIAL CREATIVE MATERIAL DOCUMENT

ASUS	Title: LGA1700 (DDR5_CH 0/1)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 7 of 77	

Channel 2/3
6 Layer routing

DDR4(IL) / DDR4(NIL) / DDR5 DDR4 / DDR5

LGA1700B

14	D5_DDR3_DQ3[0:7]	D5_DDR3_DQ36	AL7	DDR1_DQ7[7]/DDR1_DQ7[7]	/DDR3_DQ3[7]	DDR1_CLKP3/DDR3_CLKP1	BD25
		D5_DDR3_DQ34	AM6	DDR1_DQ7[6]/DDR1_DQ7[6]	/DDR3_DQ3[6]	DDR1_CLKN3/DDR3_CLKN1	BC25
		D5_DDR3_DQ37	AL6	DDR1_DQ7[5]/DDR1_DQ7[5]	/DDR3_DQ3[5]	DDR1_CLKP2/DDR3_CLKP0	BC24
		D5_DDR3_DQ35	AL8	DDR1_DQ7[4]/DDR1_DQ7[4]	/DDR3_DQ3[4]	DDR1_CLKN2/DDR3_CLKN0	BB24
		D5_DDR3_DQ32	AP6	DDR1_DQ7[3]/DDR1_DQ7[3]	/DDR3_DQ3[3]	DDR1_CLKP1/DDR2_CLKP1	BC26
		D5_DDR3_DQ30	AN6	DDR1_DQ7[2]/DDR1_DQ7[2]	/DDR3_DQ3[2]	DDR1_CLKN1/DDR2_CLKN1	BB26
		D5_DDR3_DQ33	AP7	DDR1_DQ7[1]/DDR1_DQ7[1]	/DDR3_DQ3[1]	DDR1_CLKP0/DDR2_CLKP0	BD27
		D5_DDR3_DQ31	AP8	DDR1_DQ7[0]/DDR1_DQ7[0]	/DDR3_DQ3[0]	DDR1_CLKN0/DDR2_CLKN0	BC27
14	D5_DDR3_DQ2[0:7]	D5_DDR3_DQ24	AT7	DDR1_DQ6[7]/DDR1_DQ6[7]	/DDR3_DQ2[7]		
		D5_DDR3_DQ25	AT6	DDR1_DQ6[6]/DDR1_DQ6[6]	/DDR3_DQ2[6]	DDR1_CKE3/NC	AV33
		D5_DDR3_DQ26	AV6	DDR1_DQ6[5]/DDR1_DQ6[5]	/DDR3_DQ2[5]	DDR1_CKE2/DDR2_CS1	AT29
		D5_DDR3_DQ27	AU6	DDR1_DQ6[4]/DDR1_DQ6[4]	/DDR3_DQ2[4]	DDR1_CKE1/DDR2_CS3	AU32
		D5_DDR3_DQ20	AW6	DDR1_DQ6[3]/DDR1_DQ6[3]	/DDR3_DQ2[3]	DDR1_CKE0/DDR2_CS0	AV32
		D5_DDR3_DQ23	AV8	DDR1_DQ6[2]/DDR1_DQ6[2]	/DDR3_DQ2[2]		
		D5_DDR3_DQ21	AW8	DDR1_DQ6[1]/DDR1_DQ6[1]	/DDR3_DQ2[1]	DDR1_CS3/DDR3_CS0	AW22
		D5_DDR3_DQ22	AW7	DDR1_DQ6[0]/DDR1_DQ6[0]	/DDR3_DQ2[0]	DDR1_CS2/DDR3_CA5	AU24
14	D5_DDR3_DQ1[0:7]	D5_DDR3_DQ14	AW10	DDR1_DQ5[7]/DDR1_DQ3[7]	/DDR3_DQ1[7]	DDR1_CS1/DDR3_CA0	AU22
		D5_DDR3_DQ17	AV10	DDR1_DQ5[6]/DDR1_DQ3[6]	/DDR3_DQ1[6]	DDR1_CS0/DDR3_CA6	AV24
		D5_DDR3_DQ16	AW11	DDR1_DQ5[5]/DDR1_DQ3[5]	/DDR3_DQ1[5]		
		D5_DDR3_DQ15	AU10	DDR1_DQ5[4]/DDR1_DQ3[4]	/DDR3_DQ1[4]	DDR1_ODT3/NC	AW20
		D5_DDR3_DQ13	AT12	DDR1_DQ5[3]/DDR1_DQ3[3]	/DDR3_DQ1[3]	DDR1_ODT2/DDR3_CA1	AR26
		D5_DDR3_DQ11	AU12	DDR1_DQ5[2]/DDR1_DQ3[2]	/DDR3_DQ1[2]	DDR1_ODT1/DDR3_CS1	AW21
		D5_DDR3_DQ10	AW12	DDR1_DQ5[1]/DDR1_DQ3[1]	/DDR3_DQ1[1]	DDR1_ODT0/DDR3_CA3	AW24
		D5_DDR3_DQ12	AV12	DDR1_DQ5[0]/DDR1_DQ3[0]	/DDR3_DQ1[0]		
14	D5_DDR3_DQ0[0:7]	D5_DDR3_DQ05	AT14	DDR1_DQ4[7]/DDR1_DQ2[7]	/DDR3_DQ0[7]	DDR1_BA1/DDR3_CA11	AV26
		D5_DDR3_DQ06	AU14	DDR1_DQ4[6]/DDR1_DQ2[6]	/DDR3_DQ0[6]	DDR1_BA0/DDR3_CA9	AW25
		D5_DDR3_DQ04	AW14	DDR1_DQ4[5]/DDR1_DQ2[5]	/DDR3_DQ0[5]		
		D5_DDR3_DQ07	AV14	DDR1_DQ4[4]/DDR1_DQ2[4]	/DDR3_DQ0[4]	DDR1_BG1/DDR2_CA2	AW31
		D5_DDR3_DQ00	AW15	DDR1_DQ4[3]/DDR1_DQ2[3]	/DDR3_DQ0[3]	DDR1_BG0/DDR2_CA1	AW32
		D5_DDR3_DQ01	AU16	DDR1_DQ4[2]/DDR1_DQ2[2]	/DDR3_DQ0[2]		
		D5_DDR3_DQ03	AW16	DDR1_DQ4[1]/DDR1_DQ2[1]	/DDR3_DQ0[1]	DDR1_MA16/DDR3_CA8	AW26
		D5_DDR3_DQ02	AV16	DDR1_DQ4[0]/DDR1_DQ2[0]	/DDR3_DQ0[0]	DDR1_MA15/DDR3_CA4	AW23
14	D5_DDR2_DQ3[0:7]	D5_DDR2_DQ34	AW40	DDR1_DQ3[7]/DDR0_DQ7[7]	/DDR2_DQ3[7]	DDR1_MA14/DDR3_CA7	AT25
		D5_DDR2_DQ35	AW39	DDR1_DQ3[6]/DDR0_DQ7[6]	/DDR2_DQ3[6]	DDR1_MA13/DDR3_CA2	AU23
		D5_DDR2_DQ37	AU39	DDR1_DQ3[5]/DDR0_DQ7[5]	/DDR2_DQ3[5]	DDR1_MA12/DDR2_CA3	AU30
		D5_DDR2_DQ36	AV39	DDR1_DQ3[4]/DDR0_DQ7[4]	/DDR2_DQ3[4]	DDR1_MA11/DDR2_CA5	AU29
		D5_DDR2_DQ30	AW42	DDR1_DQ3[3]/DDR0_DQ7[3]	/DDR2_DQ3[3]	DDR1_MA10/DDR3_CA10	AU25
		D5_DDR2_DQ33	AW41	DDR1_DQ3[2]/DDR0_DQ7[2]	/DDR2_DQ3[2]	DDR1_MA9/DDR2_CA4	AV30
		D5_DDR2_DQ31	AV42	DDR1_DQ3[1]/DDR0_DQ7[1]	/DDR2_DQ3[1]	DDR1_MA8/DDR2_CA7	AW29
		D5_DDR2_DQ32	AU42	DDR1_DQ3[0]/DDR0_DQ7[0]	/DDR2_DQ3[0]	DDR1_MA7/DDR2_CA6	AW30
14	D5_DDR2_DQ2[0:7]	D5_DDR2_DQ24	AW45	DDR1_DQ2[7]/DDR0_DQ6[7]	/DDR2_DQ2[7]	DDR1_MA6/DDR2_CA8	AV28
		D5_DDR2_DQ27	AW44	DDR1_DQ2[6]/DDR0_DQ6[6]	/DDR2_DQ2[6]	DDR1_MA5/DDR2_CA9	AU26
		D5_DDR2_DQ26	AV44	DDR1_DQ2[5]/DDR0_DQ6[5]	/DDR2_DQ2[5]	DDR1_MA4/DDR2_CA10	AU27
		D5_DDR2_DQ22	AW46	DDR1_DQ2[4]/DDR0_DQ6[4]	/DDR2_DQ2[4]	DDR1_MA3/DDR2_CA11	AW28
		D5_DDR2_DQ20	AW47	DDR1_DQ2[3]/DDR0_DQ6[3]	/DDR2_DQ2[3]	DDR1_MA2/NC	AT27
		D5_DDR2_DQ25	AU44	DDR1_DQ2[2]/DDR0_DQ6[2]	/DDR2_DQ2[2]	DDR1_MA1/DDR2_CA12	AW27
		D5_DDR2_DQ21	AU47	DDR1_DQ2[1]/DDR0_DQ6[1]	/DDR2_DQ2[1]	DDR1_MA0/DDR3_CA12	AU26
		D5_DDR2_DQ23	AV47	DDR1_DQ2[0]/DDR0_DQ6[0]	/DDR2_DQ2[0]		
14	D5_DDR2_DQ1[0:7]	D5_DDR2_DQ15	AR45	DDR1_DQ1[7]/DDR0_DQ3[7]	/DDR2_DQ1[7]	DDR1_ACT#/DDR2_CA0	AU31
		D5_DDR2_DQ17	AR44	DDR1_DQ1[6]/DDR0_DQ3[6]	/DDR2_DQ1[6]	DDR1_PAR/NC	AR27
		D5_DDR2_DQ16	AR47	DDR1_DQ1[5]/DDR0_DQ3[5]	/DDR2_DQ1[5]	DDR1_ALERT#	AP26
		D5_DDR2_DQ14	AR46	DDR1_DQ1[4]/DDR0_DQ3[4]	/DDR2_DQ1[4]		
		D5_DDR2_DQ10	AN46	DDR1_DQ1[3]/DDR0_DQ3[3]	/DDR2_DQ1[3]	DDR4(IL)/ DDR4(NIL)/ DDR5	AM8
		D5_DDR2_DQ11	AN45	DDR1_DQ1[2]/DDR0_DQ3[2]	/DDR2_DQ1[2]	DDR1_DQSP7/ DDR1_DQSP7/DDR3_DQSP3	AN8
		D5_DDR2_DQ12	AN47	DDR1_DQ1[1]/DDR0_DQ3[1]	/DDR2_DQ1[1]	DDR1_DQSN7/ DDR1_DQSN7/DDR3_DQSN3	AT8
		D5_DDR2_DQ13	AP47	DDR1_DQ1[0]/DDR0_DQ3[0]	/DDR2_DQ1[0]	DDR1_DQSP6/ DDR1_DQSP6/DDR3_DQSP2	AU8
14	D5_DDR2_DQ0[0:7]	D5_DDR2_DQ05	AL45	DDR1_DQ0[7]/DDR0_DQ2[7]	/DDR2_DQ0[7]	DDR1_DQSN6/ DDR1_DQSN6/DDR3_DQSN2	AT10
		D5_DDR2_DQ07	AL46	DDR1_DQ0[6]/DDR0_DQ2[6]	/DDR2_DQ0[6]	DDR1_DQSP5/ DDR1_DQSP3/DDR3_DQSP1	AT11
		D5_DDR2_DQ04	AK47	DDR1_DQ0[5]/DDR0_DQ2[5]	/DDR2_DQ0[5]	DDR1_DQSN5/ DDR1_DQSN3/DDR3_DQSN1	AT15
		D5_DDR2_DQ06	AL47	DDR1_DQ0[4]/DDR0_DQ2[4]	/DDR2_DQ0[4]	DDR1_DQSP4/ DDR1_DQSP2/DDR3_DQSP0	AT16
		D5_DDR2_DQ01	AH47	DDR1_DQ0[3]/DDR0_DQ2[3]	/DDR2_DQ0[3]	DDR1_DQSN4/ DDR1_DQSN2/DDR3_DQSN0	AU40
		D5_DDR2_DQ00	AJ47	DDR1_DQ0[2]/DDR0_DQ2[2]	/DDR2_DQ0[2]	DDR1_DQSP3/ DDR0_DQSP7/DDR2_DQSP3	AU41
		D5_DDR2_DQ03	AH45	DDR1_DQ0[1]/DDR0_DQ2[1]	/DDR2_DQ0[1]	DDR1_DQSN3/ DDR0_DQSN7/DDR2_DQSN3	AU45
		D5_DDR2_DQ02	AH46	DDR1_DQ0[0]/DDR0_DQ2[0]	/DDR2_DQ0[0]	DDR1_DQSP2/ DDR0_DQSP6/DDR2_DQSP2	AU46
						DDR1_DQSN2/ DDR0_DQSN6/DDR2_DQSN2	AP44
		AU35				DDR1_DQSP1/ DDR0_DQSP3/DDR2_DQSP1	AN44
		AV35		DDR1_DQ8[7]/DDR1_DQ8[7]/NC		DDR1_DQSN1/ DDR0_DQSN3/DDR2_DQSN1	AK45
		AW36		DDR1_DQ8[6]/DDR1_DQ8[6]/NC		DDR1_DQSP0/ DDR0_DQSP2/DDR2_DQSP0	AJ45
		AW35		DDR1_DQ8[5]/DDR1_DQ8[5]/NC		DDR1_DQSN0/ DDR0_DQSN2/DDR2_DQSN0	
		AV37		DDR1_DQ8[4]/DDR1_DQ8[4]/NC			
		AW37		DDR1_DQ8[3]/DDR1_DQ8[3]	/DDR2_DQ4[3]	DDR1_DQSP8/ DDR1_DQSP8/DDR2_DQSP4	AT35
		AU37		DDR1_DQ8[2]/DDR1_DQ8[2]	/DDR2_DQ4[2]	DDR1_DQSN8/ DDR1_DQSN8/DDR2_DQSN4	AT36
		AT37		DDR1_DQ8[1]/DDR1_DQ8[1]	/DDR2_DQ4[1]		
				DDR1_DQ8[0]/DDR1_DQ8[0]	/DDR2_DQ4[0]	NC/NC/DDR3_DQSP4	AR18
						NC/NC/DDR3_DQSN4	AR19
		AV18					
		AU18		NC/NC/DDR3_DQ4[3]		NC/DDR3_CLKP3	AP22
		AW18		NC/NC/DDR3_DQ4[2]		NC/DDR3_CLKN3	AP21
		AT18		NC/NC/DDR3_DQ4[1]		NC/DDR3_CLKP2	AR21
				NC/NC/DDR3_DQ4[0]		NC/DDR3_CLKN2	AT21
						NC/DDR2_CLKP3	AP32
		AH49		DDR_VREF_CA3		NC/DDR2_CLKN3	AP33
		AH51		DDR_VREF_CA2		NC/DDR2_CLKP2	AR33
						NC/DDR2_CLKN2	AT33
						NC/DDR1_CLKP3	AP24
						NC/DDR1_CLKN3	AR24
						NC/DDR1_CLKP2	AR23
						NC/DDR1_CLKN2	AT23
						NC/DDR0_CLKP3	AP30
						NC/DDR0_CLKN3	AR30
						NC/DDR0_CLKP2	AR31
						NC/DDR0_CLKN2	AT31

D5_DDR3_CLK1	14	D5_DDR2_CA0	14
D5_DDR3_CLK#1	14	DDR1_ALERT#	14
D5_DDR3_CLK0	14	D5_DDR3_DQS3	14
D5_DDR3_CLK#0	14	D5_DDR3_DQS#3	14
D5_DDR2_CLK1	14	D5_DDR3_DQS2	14
D5_DDR2_CLK#1	14	D5_DDR3_DQS#2	14
D5_DDR2_CLK0	14	D5_DDR3_DQS1	14
D5_DDR2_CLK#0	14	D5_DDR3_DQS#1	14
D5_DDR2_CS#1	14	D5_DDR3_DQS0	14
D5_DDR2_CS#0	14	D5_DDR3_DQS#0	14
D5_DDR3_CS#0	14	D5_DDR2_DQS3	14
D5_DDR3_CA5	14	D5_DDR2_DQS#3	14
D5_DDR3_CA0	14	D5_DDR2_DQS2	14
D5_DDR3_CA6	14	D5_DDR2_DQS#2	14
D5_DDR3_CA1	14	D5_DDR2_DQS1	14
D5_DDR3_CS#1	14	D5_DDR2_DQS#1	14
D5_DDR3_CA3	14	D5_DDR2_DQS0	14
D5_DDR3_CA11	14	D5_DDR2_DQS#0	14
D5_DDR3_CA9	14		
D5_DDR2_CA2	14		
D5_DDR2_CA1	14		
D5_DDR3_CA8	14		
D5_DDR3_CA4	14		
D5_DDR3_CA7	14		
D5_DDR3_CA2	14		
D5_DDR2_CA3	14		
D5_DDR2_CA5	14		
D5_DDR3_CA10	14		
D5_DDR2_CA4	14		
D5_DDR2_CA7	14		
D5_DDR2_CA6	14		
D5_DDR2_CA8	14		
D5_DDR2_CA9	14		
D5_DDR2_CA10	14		
D5_DDR2_CA11	14		
D5_DDR2_CA12	14		
D5_DDR3_CA12	14		

AZIF0216-P002C
LOTES/AZIF0216-P002C

12001-00300200

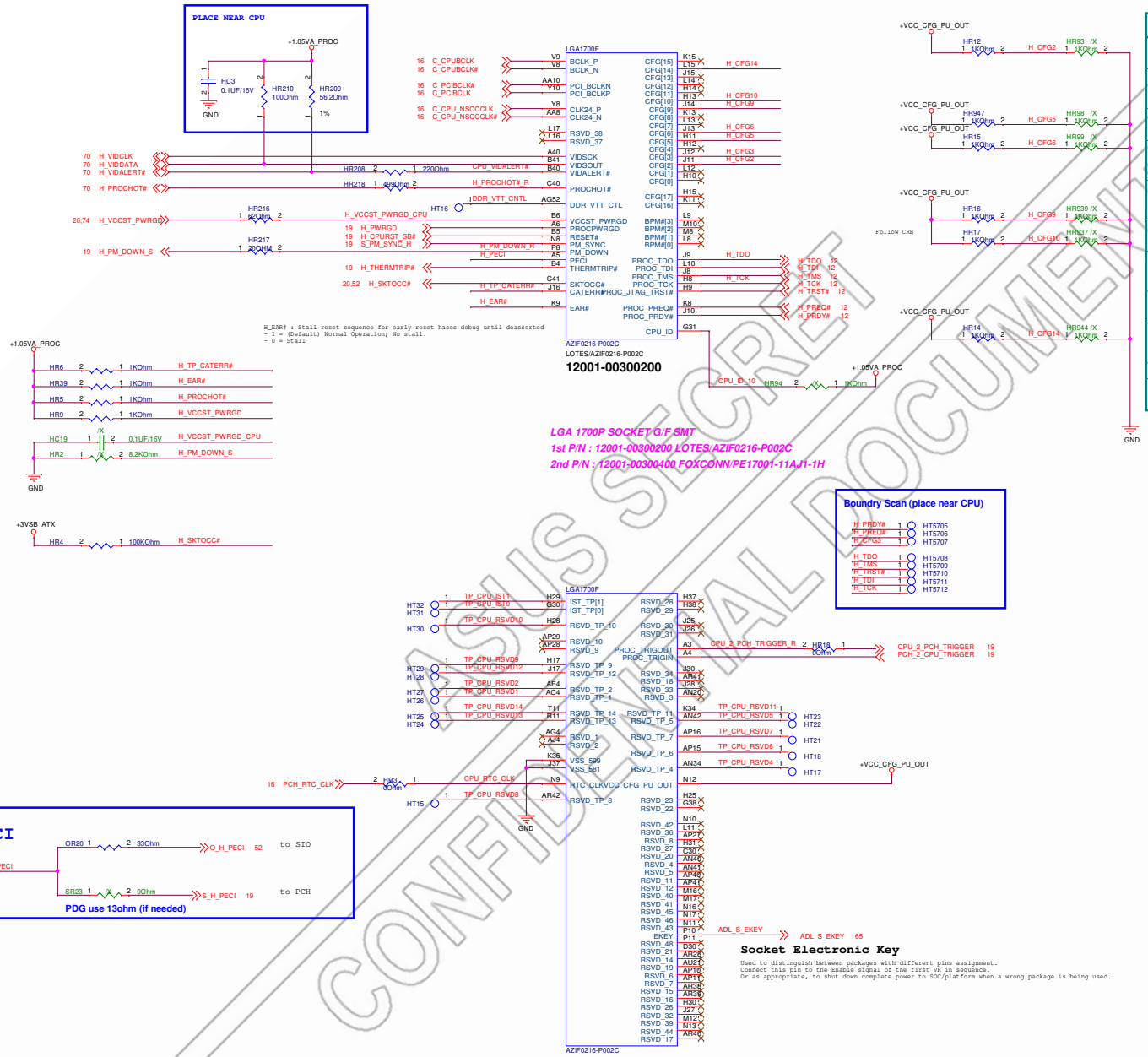
LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

CONFIDENTIAL DOCUMENT

ASUS	Title: LGA1700 (DDR5_CH 2/3)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 8 of 77		



CFG Straps for Processor (Use VCC_CFG_PU_OUT)

CFG[1:0] : Reserved Configuration Lanes
Reserved Configuration Lanes

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : Normal Operation
- 0 : Lane Numbers Reversed

CFG[4:3] : Reserved Configuration Lanes
Reserved Configuration Lane

CFG[5] : PCI Expres* Bifurcation
- 0 : 2 x8 PCI Express*
- 1 : 1 x16 PCI Express* (default)

CFG[6] : Reserved Configuration Lanes
Pull -Up to VCC_CFG_PU_OUT
To ensure reliable boot across HVM.

CFG[8:7] : Reserved Configuration Lane
Reserved Configuration Lane

CFG[10:9] : Reserved Configuration Lanes
Pull -Up to VCC_CFG_PU_OUT
To ensure reliable boot across HVM.

CFG[13:11] : Reserved Configuration Lanes
Reserved Configuration Lanes

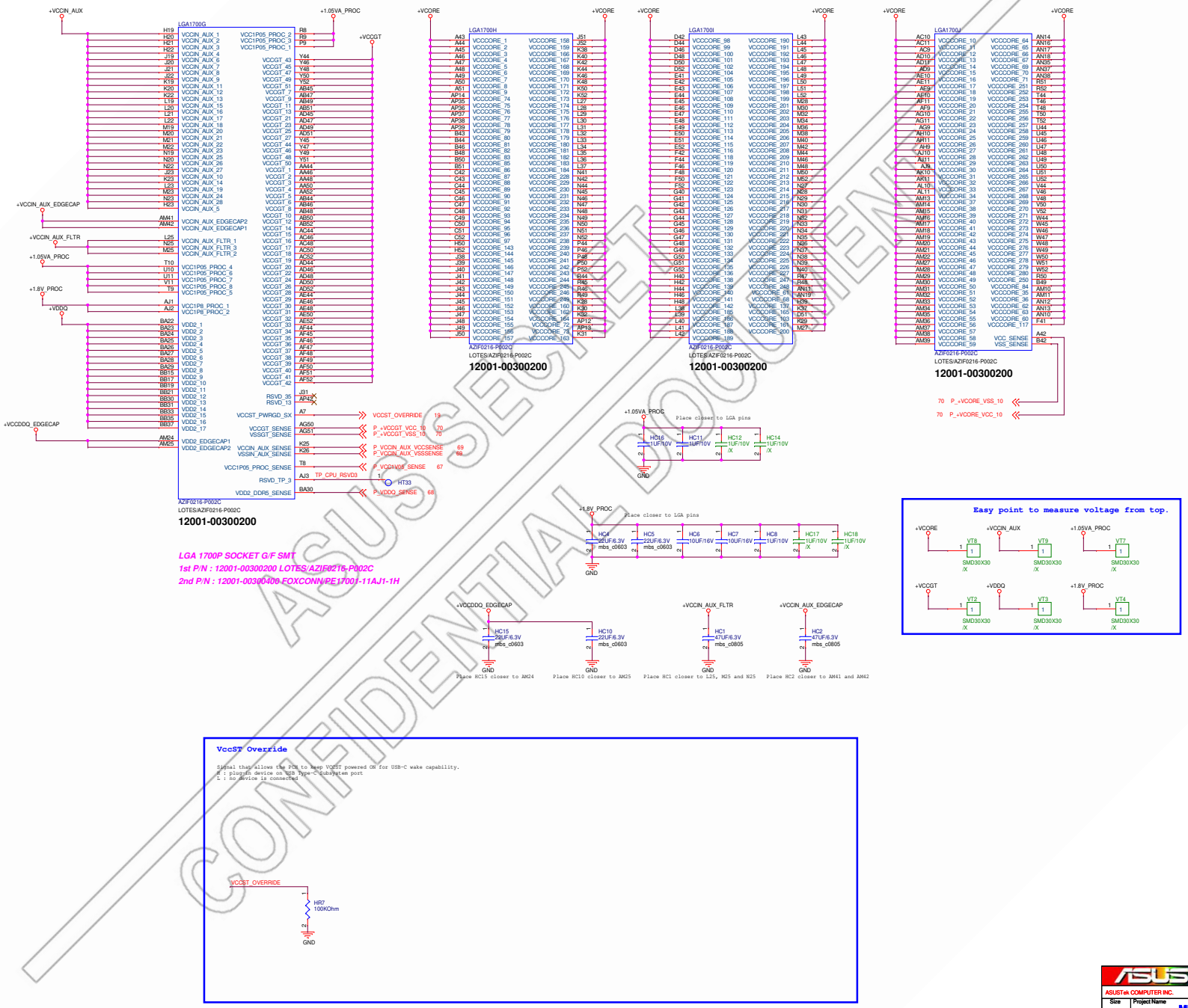
CFG[14] : PCI Express* Static x4 Lane Numbering Reversal (PEG60)
- 1 : (Default) Normal
- 0 : Reversed

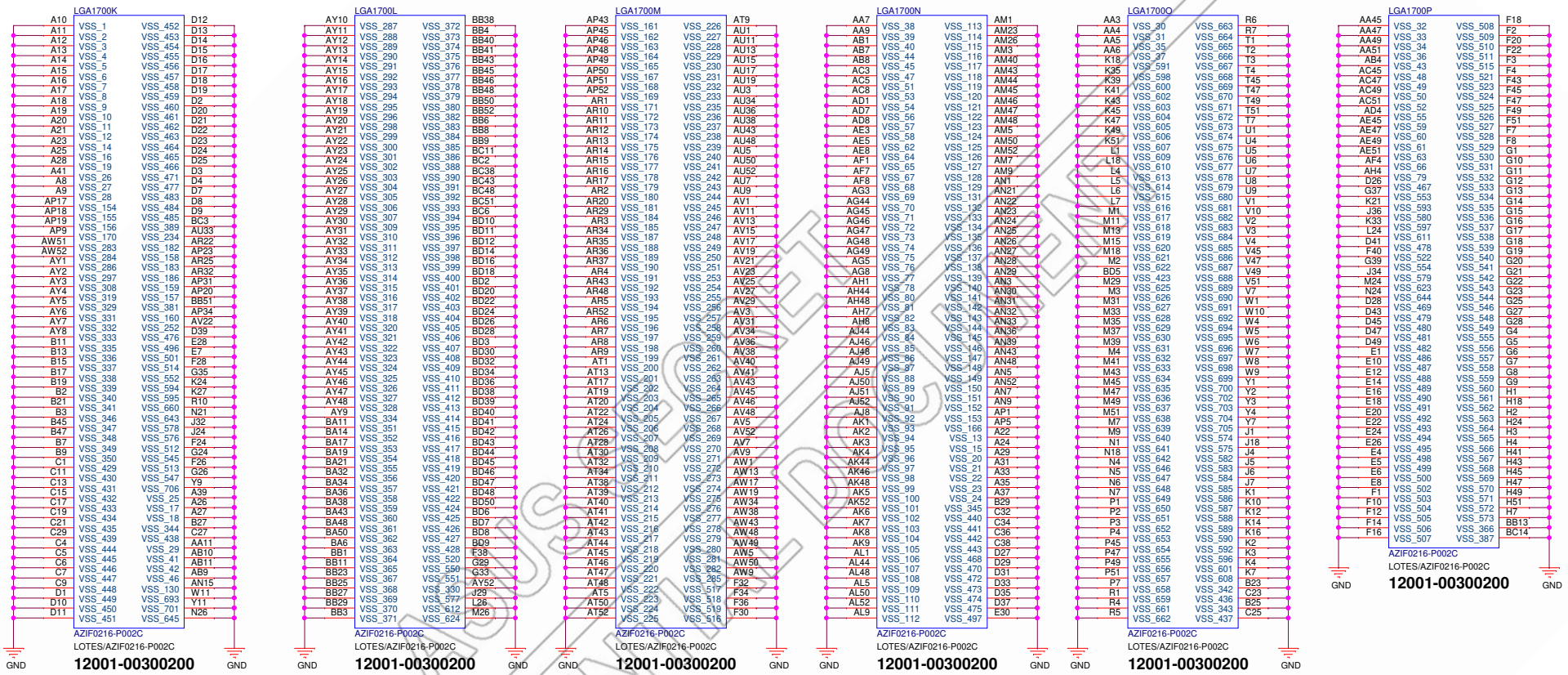
CFG[17:15] : Reserved Configuration Lanes

Refer : 619501-adl-processor-eds-vol1-rev2p3.pdf, P.171-172
619508_ADL_S_PDG_Rev2p2, p.319-320

ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTeK COMPUTER INC.	Title : LGA1700 (Control)		
	Engineer: IPC-EE3		
Size C	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 9 of 77		


LGA1700G
LGA1700H
LGA1700I
LGA1700J
AZIF0216-P002C
LOTES/AZIF0216-P002C
12001-00300200
+VCCIN_AUX
+1.05VA_PROC
+VCORE
+VCCGT
+VCCIN_AUX_EDGECAP
+VCCIN_AUX_FLTR
+1.8V_PROC
+VDDQ
+VCCDDQ_EDGECAP
VCCST_OVERRIDE
P_+VCCGT_VCC_10
P_+VCCGT_VSS_10
P_VCCIN_AUX_VCCSENSE
P_VCCIN_AUX_VSSSENSE
P_VCC1V8_SENSE
P_VDDQ_SENSE
TP_CPU_RSVD3
HT33
P_+VCORE_VSS_10
P_+VCORE_VCC_10
VCC_SENSE
VSS_SENSE
Place closer to LGA pins
HC16 1UF/10V
HC11 1UF/10V
HC12 1UF/10V /X
HC14 1UF/10V /X
HC4 22UF/6.3V mbs_c0603
HC5 22UF/6.3V mbs_c0603
HC6 10UF/16V
HC7 10UF/16V
HC8 1UF/10V
HC17 1UF/10V /X
HC18 1UF/10V /X
HC15 22UF/6.3V mbs_c0603
HC10 22UF/6.3V mbs_c0603
HC1 47UF/6.3V mbs_c0805
HC2 47UF/6.3V mbs_c0805
Place HC15 closer to AM24
Place HC10 closer to AM25
Place HC1 closer to L25, M25 and N25
Place HC2 closer to AM41 and AM42
Easy point to measure voltage from top.
VT8
VT9
VT7
VT2
VT3
VT4
SMD30X30 /X
HR7 100KOhm
GND
LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300200 LOTES AZIF0216-P002C
2nd P/N : 12001-00300400 FOXCONN PE17001-11AJ1-1H
VccST Override
Signal that allows the PCH to keep VCCST powered ON for USB-C wake capability.
H : plug-in device on USB Type-C subsystem port
L : no device is connected
ASUS SECRET DOCUMENT
CONFIDENTIAL DOCUMENT
Title : LGA1700 (POWER)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size A2
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 10 of 77

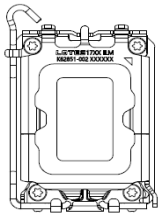


LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ILM



LGA1700_ILM_BP_COVER

[HF]LOTES/AZIF0239-P001C

13021-00020100

ILM+COVER+BACKPLATE Module-LGA1700

1st P/N : 13021-00020100 LOTES/AZIF0049-P001CC

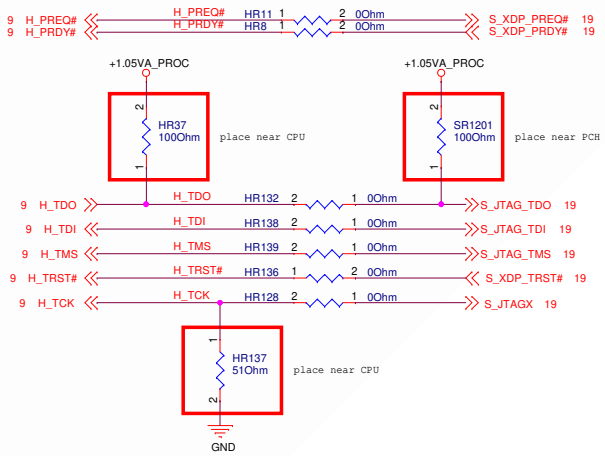
2nd P/N : 13021-00020000 FOXCONN/PMVA161-11AJ1-4H

CONFIDENTIAL DOCUMENT
ASUS

ASUS	Title : LGA1700 (GND)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A3	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 11 of 77	

ASUS SECRET
CONFIDENTIAL DOCUMENT

To PCH



ASUS	Title : LGA1700 (XDP)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 12 of 77	

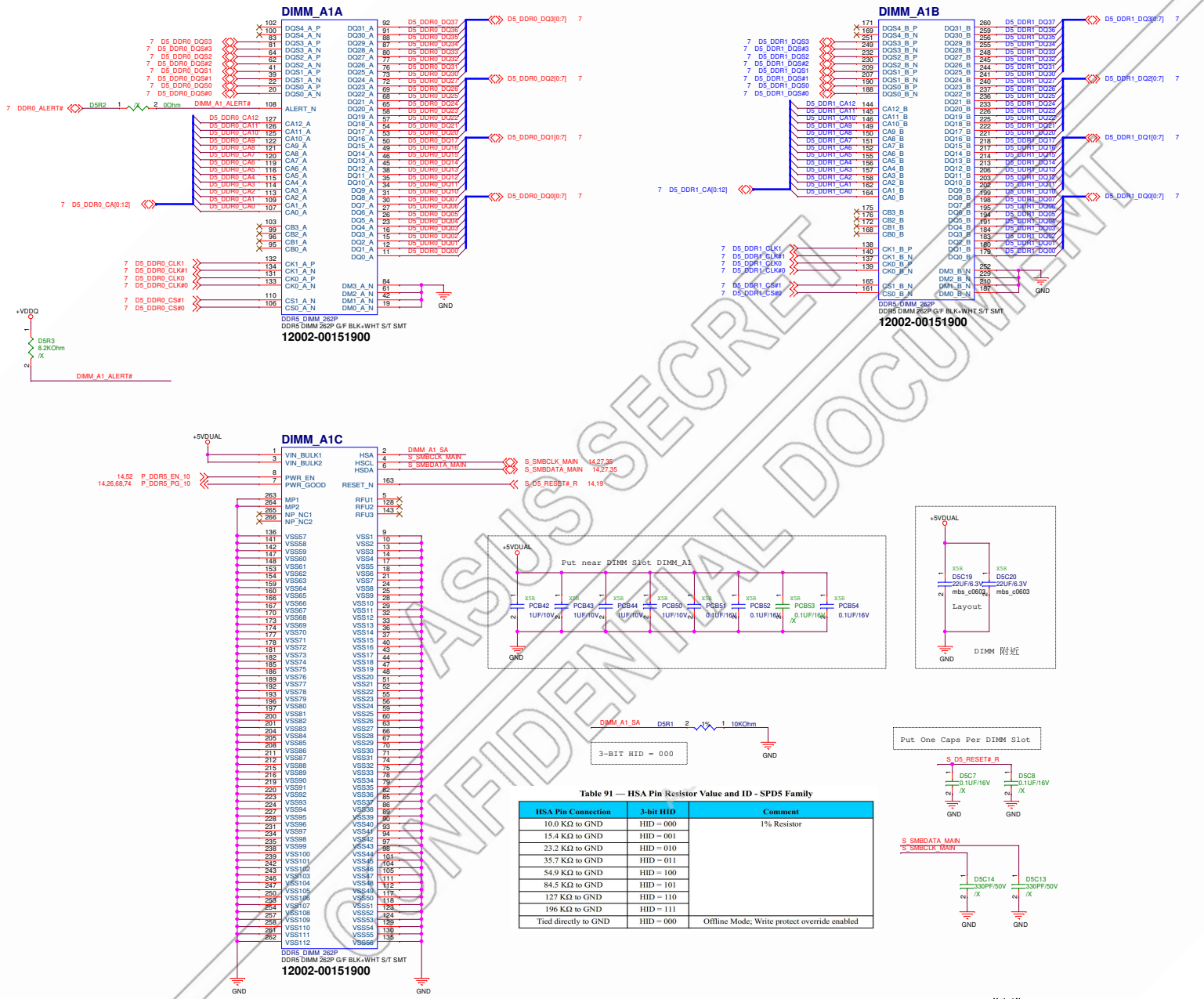
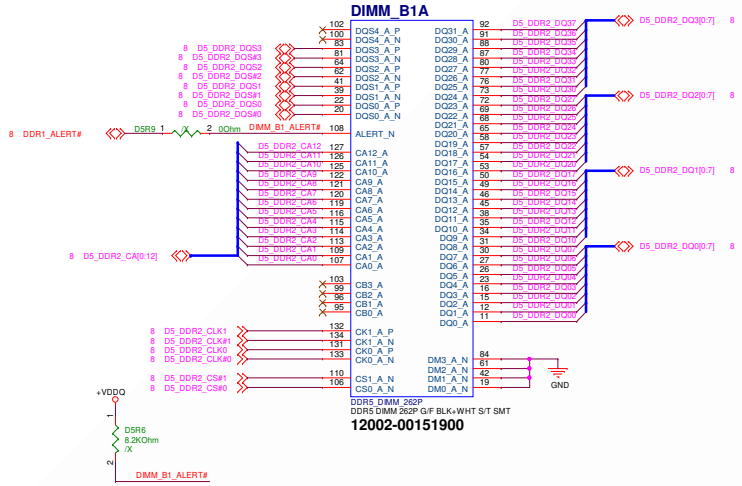
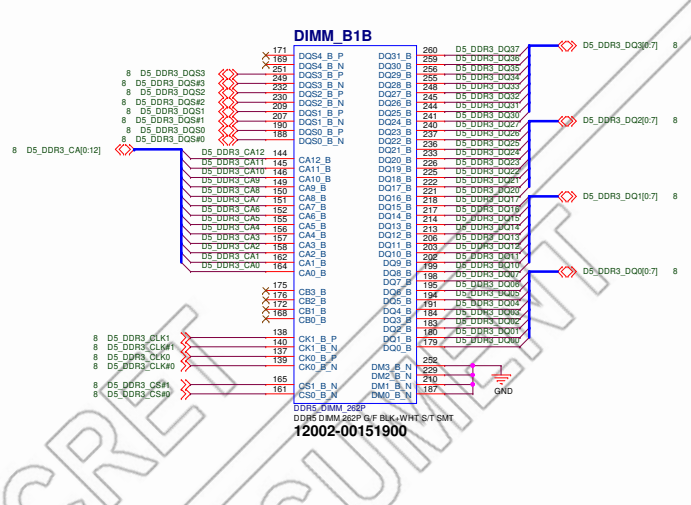


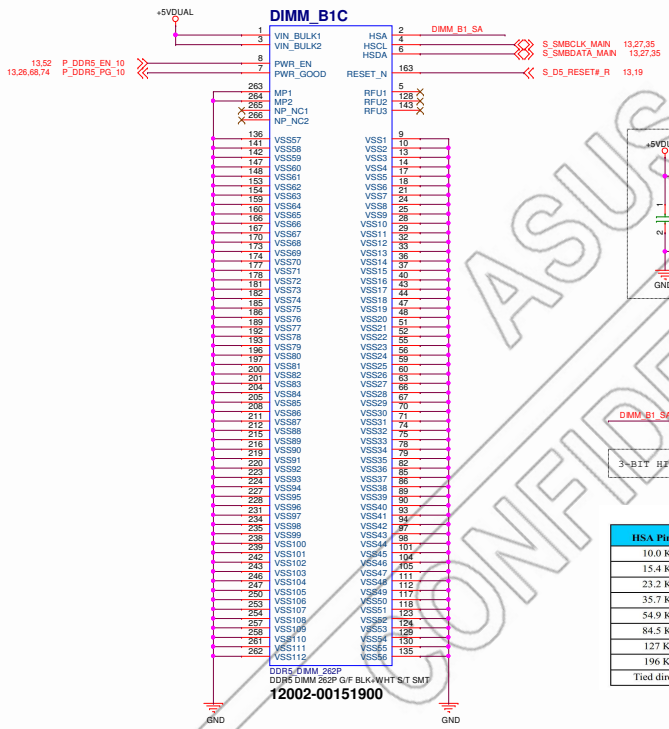
Table 91 — HSA Pin Resistor Value and ID - SPD5 Family

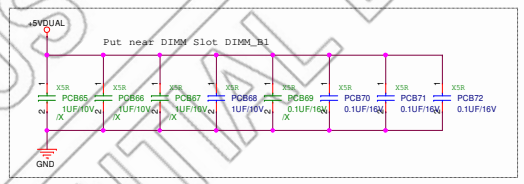
HSA Pin Connection	3-bit HID	Comment
10.0 KΩ to GND	HID = 000	1% Resistor
15.4 KΩ to GND	HID = 001	
23.2 KΩ to GND	HID = 010	
35.7 KΩ to GND	HID = 011	
54.9 KΩ to GND	HID = 100	
84.5 KΩ to GND	HID = 101	
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

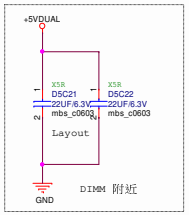
ASUS SECRET
CONFIDENTIAL DOCUMENT











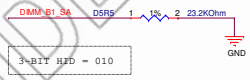
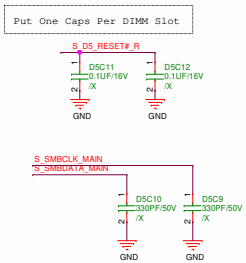


Table 91 — HSA Pin Resistor Value and ID - SPD5 Family

HSA Pin Connection	3-bit HID	Comment
10.0 KΩ to GND	HID = 000	1% Resistor
15.4 KΩ to GND	HID = 001	
23.2 KΩ to GND	HID = 010	
35.7 KΩ to GND	HID = 011	
54.9 KΩ to GND	HID = 100	
84.5 KΩ to GND	HID = 101	
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUSTeK COMPUTER INC.

Title : DDR5 DIMM B1

Engineer: IPC-EE3

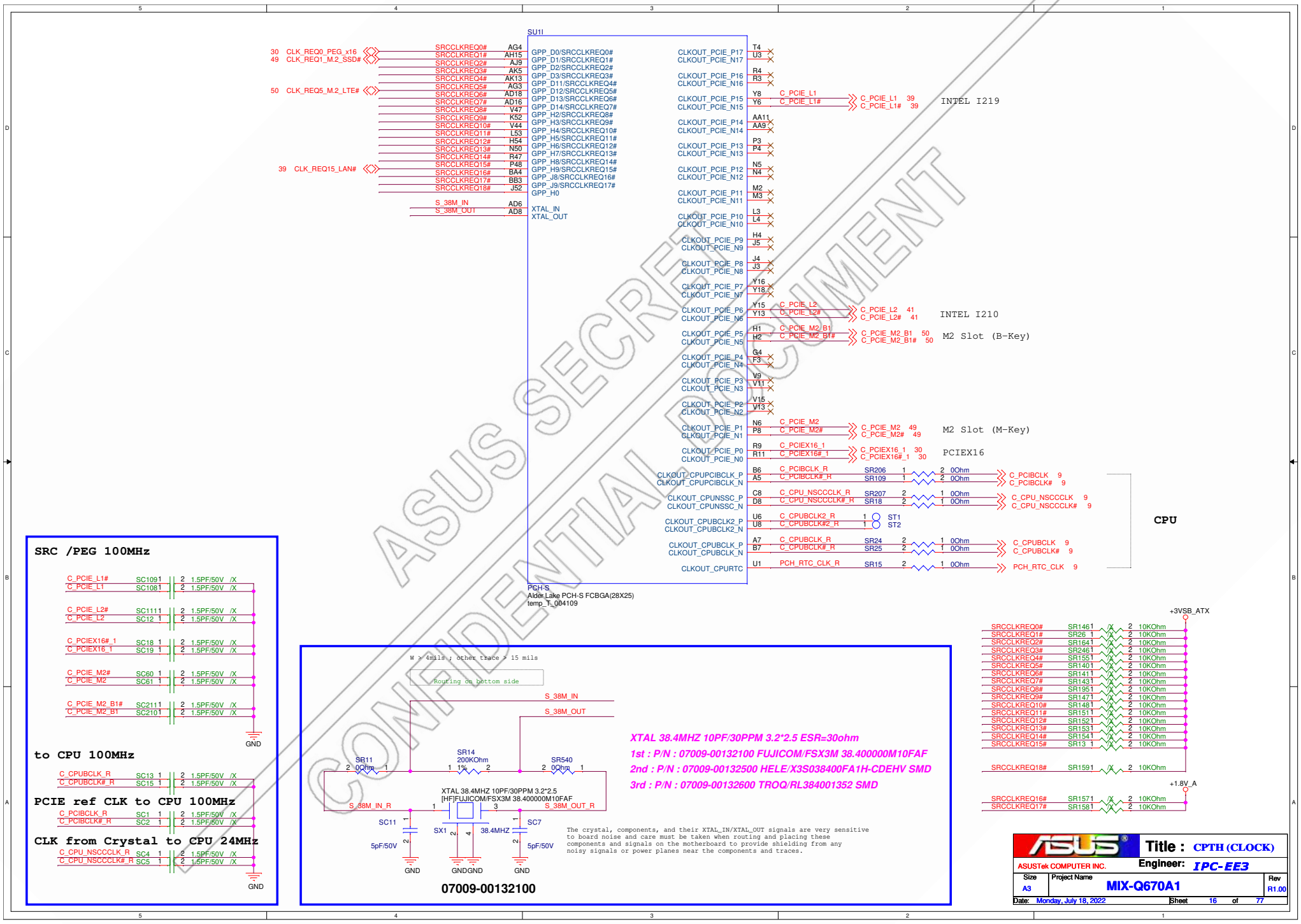
Size	Project Name	Rev
Custom	MIX-Q670A1	R1.00

Date: Monday, July 18, 2022 Sheet 14 of 77

ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUSTek COMPUTER INC.	Title : DDR4 (Power)	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 15 of 77	



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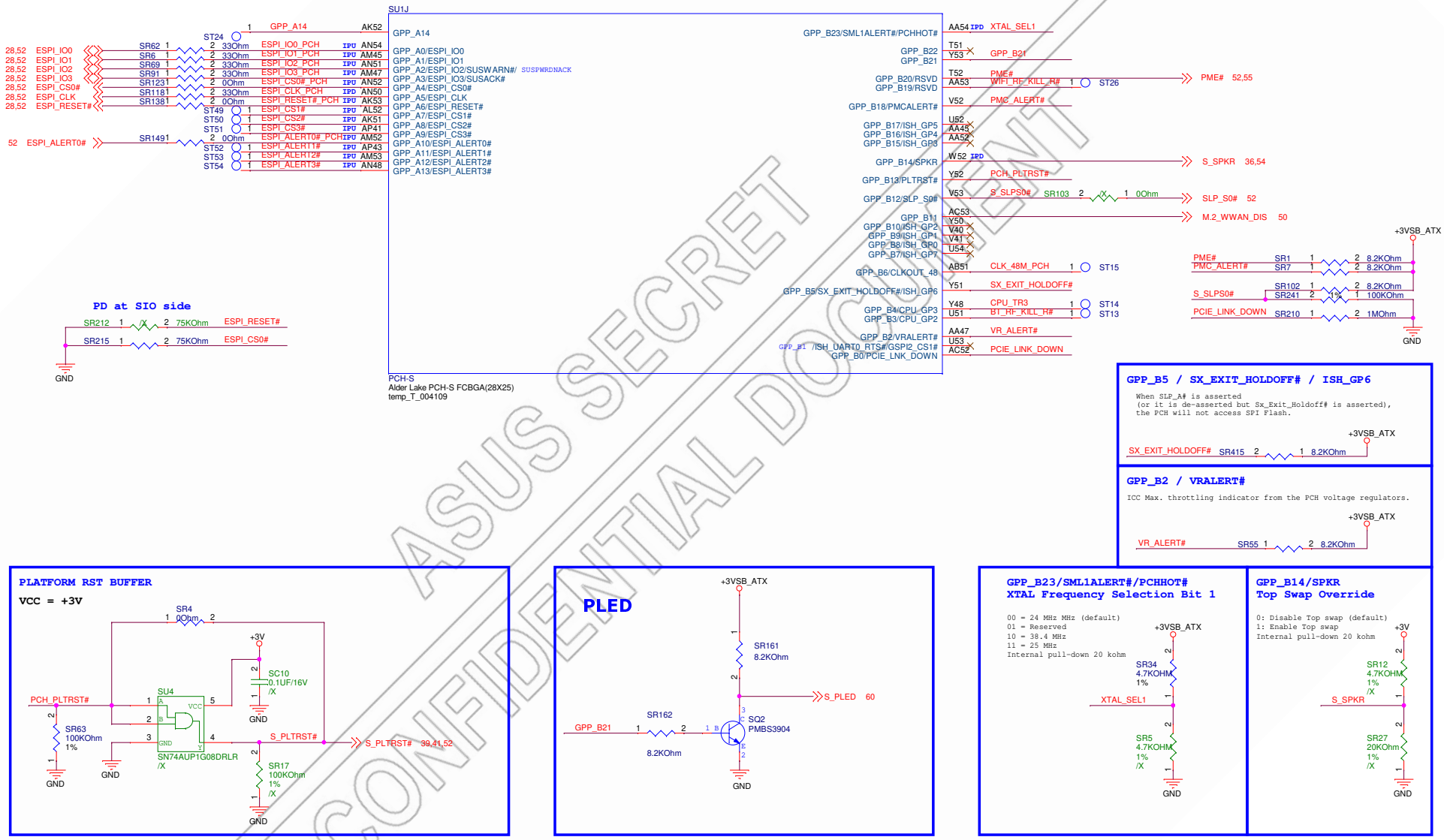
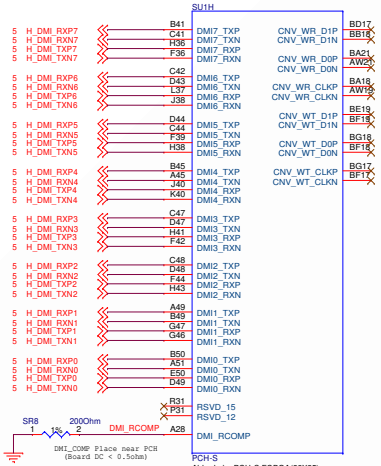
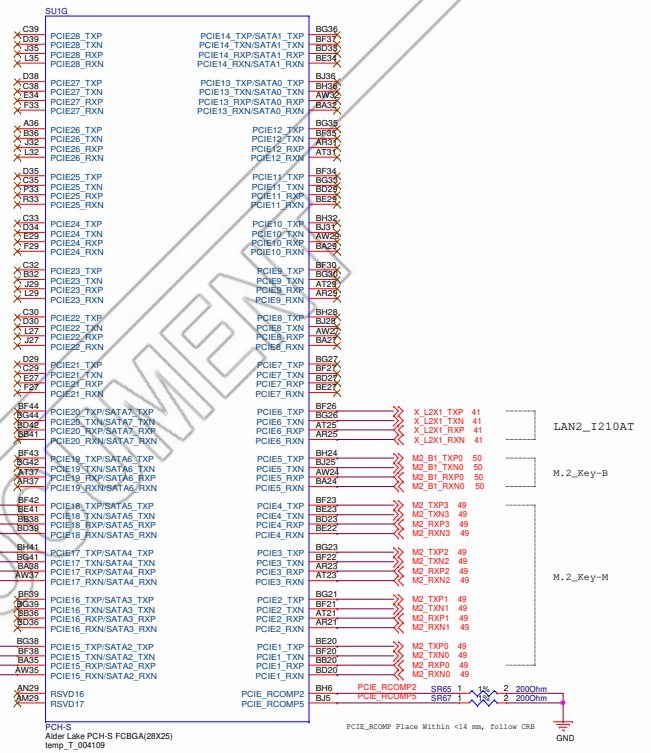
CONFIDENTIAL DOCUMENT

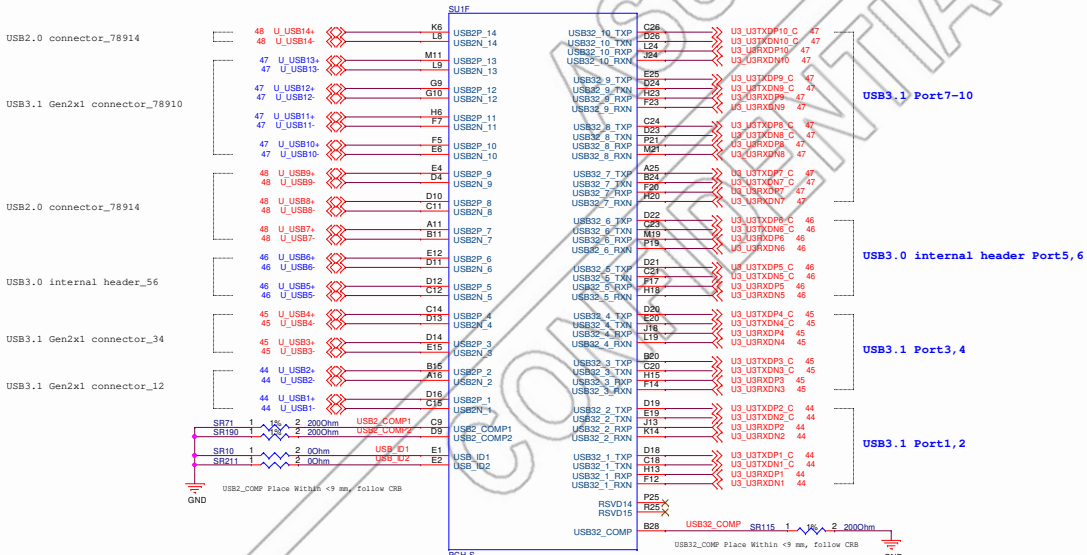


ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title :	CPTH (eSPI/ISH)
ASUSTek COMPUTER INC.	Engineer:	IPC-EE3
Size: A3	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 17 of 77	







ADL PCH-S Supported PCI Express* Link Configurations

PCH-S	North PGS - Flex HSIO Lanes																				South PD - Flex HSIO Lanes							
Flex I/O Lanes	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
PCIe Controllers	1				2				3				4				5				6				7			
PCIe Max Rate	Gen3				Gen3				Gen3				Gen4				Gen3				Gen4				Gen4			
PCIe Lanes	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Logical Link Lanes: 1x4	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Logical Link Lanes: 1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Logical Link Lanes: 2x2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Logical Link Lanes: 2x2 LR	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Logical Link Lanes: 1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
Logical Link Lanes: 4x1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Assigned Root Ports: 1x4	RP1				RP5				RP9				RP13				RP17				RP21				RP25			
Assigned Root Ports: 1x4 LR	RP1				RP5				RP9				RP13				RP17				RP21				RP25			
Assigned Root Ports: 2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15		RP17		RP19		RP21		RP23		RP25		RP27	
Assigned Root Ports: 2x2 LR	RP3		RP1		RP7		RP5		RP11		RP9		RP15		RP13		RP19		RP17		RP23		RP21		RP27		RP25	
Assigned Root Ports: 1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16	RP17		RP19	RP20	RP21		RP23	RP24	RP25		RP27	RP28
Assigned Root Ports: 4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18	RP19	RP20	RP21	RP22	RP23	RP24	RP25	RP26	RP27	RP28

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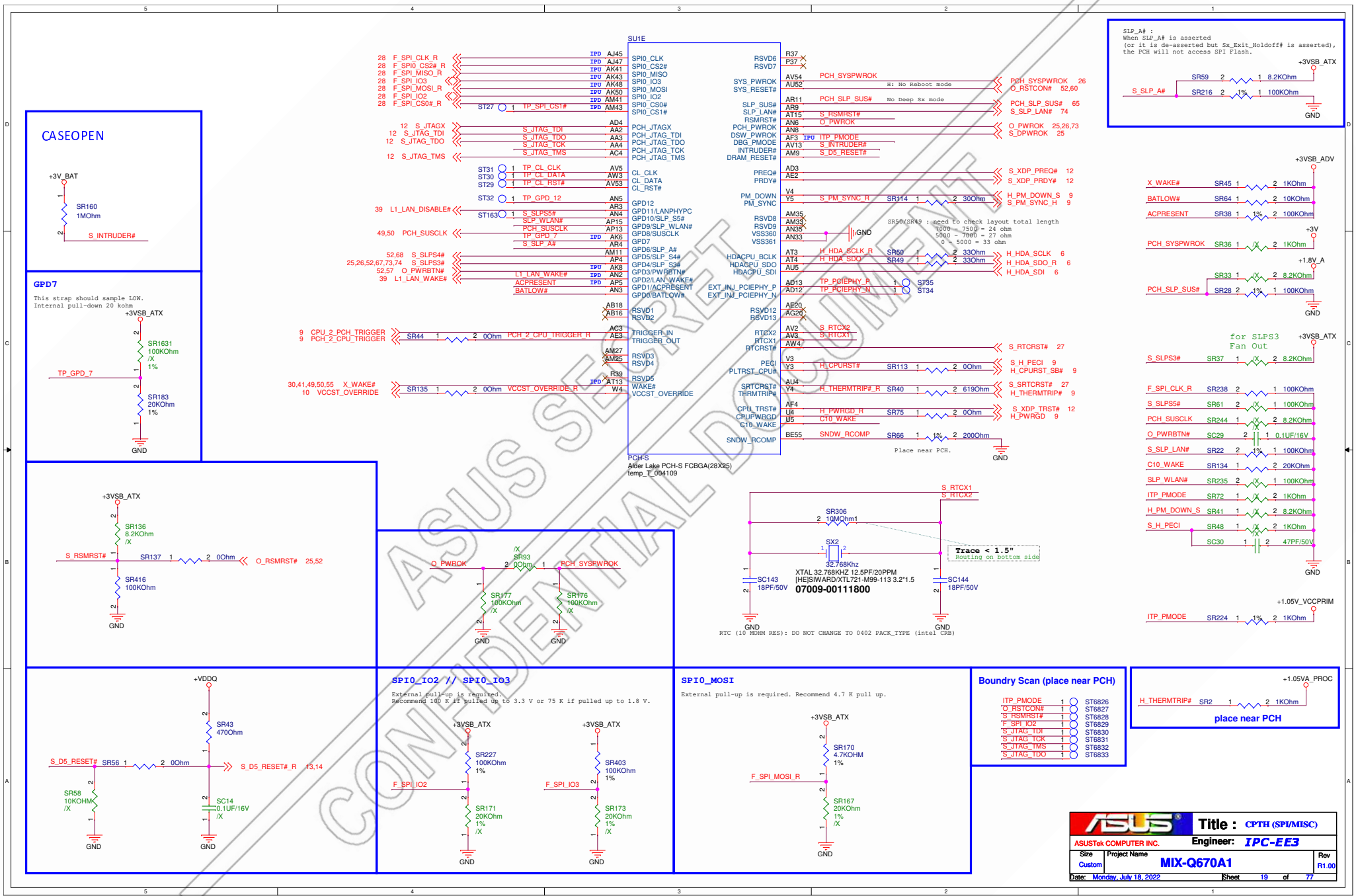
ASUSTeK COMPUTER INC.

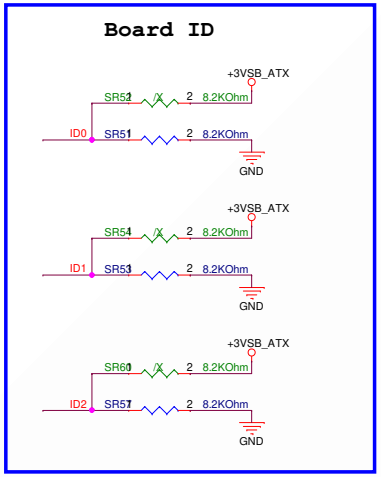
Title : CPTH (PCIE/DMI/USB/SATA)

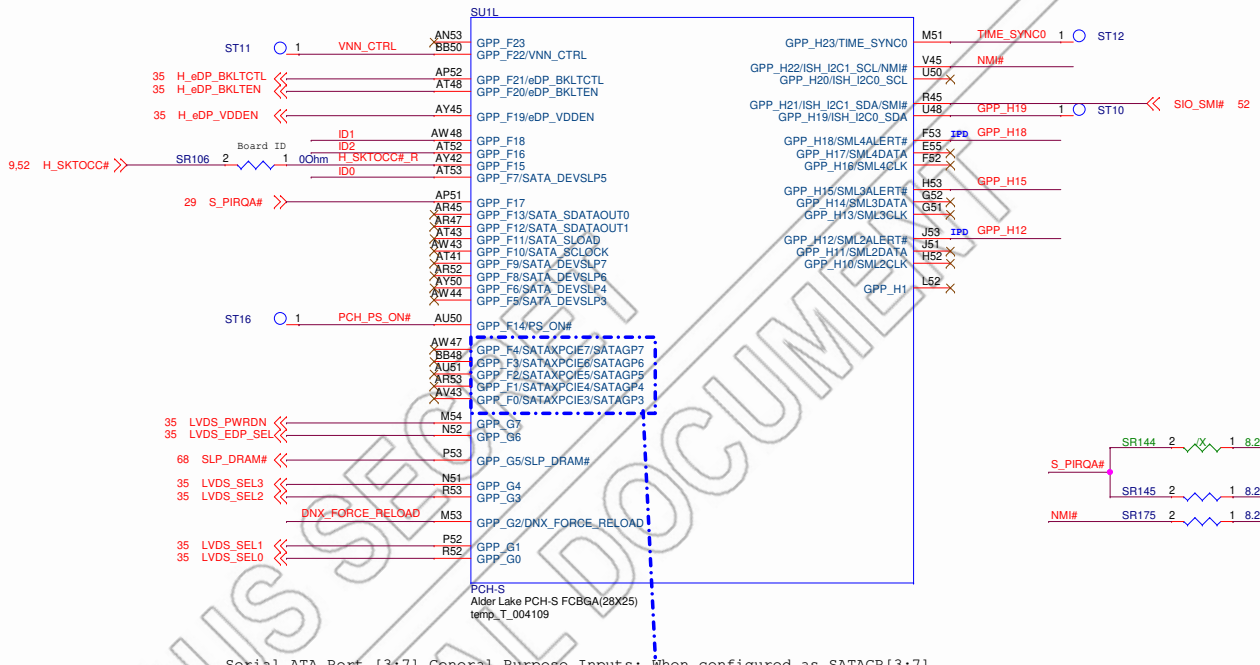
Engineer: IPC-EE3

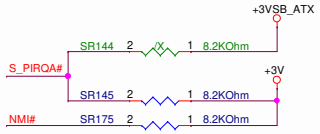
Size	Project Name	Rev
C	MIX-Q670A1	R1.00

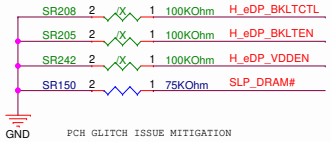
Date: Monday, July 18, 2022 Sheet 18 of 77


SU1E
PCH-S
Alder Lake PCH-S FCBGA(28X25)
Temp_T_004109
CASEOPEN
+3V_BAT
SR160
1MOhm
S_INTRUDER#
GPD7
This strap should sample LOW.
Internal pull-down 20 kohm
+3VSB_ATX
SR1631
100KOhm
/X
1%
TP_GPD_7
SR183
20KOhm
1%
GND
+3VSB_ATX
SR136
8.2KOhm
/X
S_RSMRST#
SR137
0Ohm
O_RSMRST# 25,52
SR416
100KOhm
GND
O_PWROK
/X
SR93
0Ohm
PCH_SYSPWROK
SR177
100KOhm
/X
SR176
100KOhm
/X
GND
GND
SLP_A# :
When SLP_A# is asserted
(or it is de-asserted but Sx_Exit_Holdoff# is asserted),
the PCH will not access SPI Flash.
+3VSB_ATX
SR59
8.2KOhm
S_SLP_A#
SR216
1%
100KOhm
GND
+3VSB_ADV
X_WAKE#
SR45
1KOhm
BATLOW#
SR64
10KOhm
ACPRESENT
SR38
1%
100KOhm
+3V
PCH_SYSPWROK
SR36
/X
1KOhm
+1.8V_A
SR33
/X
8.2KOhm
PCH_SLP_SUS#
SR28
1%
100KOhm
GND
for SLPS3
Fan Out
+3VSB_ATX
S_SLPS3#
SR37
/X
8.2KOhm
F_SPI_CLK_R
SR238
100KOhm
S_SLPS5#
SR61
/X
100KOhm
PCH_SUSCLK
SR244
/X
8.2KOhm
O_PWRBTN#
SC29
0.1UF/16V
S_SLP_LAN#
SR22
1%
100KOhm
C10_WAKE
SR134
20KOhm
SLP_WLAN#
SR235
/X
100KOhm
ITP_PMODE
SR72
/X
1KOhm
H_PM_DOWN_S
SR41
/X
8.2KOhm
S_H_PECI
SR48
/X
1KOhm
SC30
47PF/50V
GND
+1.05V_VCCPRIM
ITP_PMODE
SR224
1%
1KOhm
S_RTCX1
S_RTCX2
SR306
10MOhm1
SX2
32.768Khz
Trace < 1.5"
Routing on bottom side
XTAL 32.768KHZ 12.5PF/20PPM
[HE]SIWARD/XTL721-M99-113 3.2*1.5
07009-00111800
SC143
18PF/50V
SC144
18PF/50V
GND
GND
RTC (10 MOHM RES): DO NOT CHANGE TO 0402 PACK_TYPE (intel CRB)
+VDDQ
SR43
470Ohm
S_D5_RESET#
SR56
0Ohm
S_D5_RESET#_R 13,14
SR58
10KOHM
/X
SC14
0.1UF/16V
/X
GND
GND
SPI0_IO2 // SPI0_IO3
External pull-up is required.
Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V.
+3VSB_ATX
SR227
100KOhm
1%
F_SPI_IO2
SR171
20KOhm
1%
/X
GND
+3VSB_ATX
SR403
100KOhm
1%
F_SPI_IO3
SR173
20KOhm
1%
/X
GND
SPI0_MOSI
External pull-up is required. Recommend 4.7 K pull up.
+3VSB_ATX
SR170
4.7KOHM
1%
F_SPI_MOSI_R
SR167
20KOhm
1%
/X
GND
Boundry Scan (place near PCH)
ITP_PMODE ST6826
O_RSTCON# ST6827
S_RSMRST# ST6828
F_SPI_IO2 ST6829
S_JTAG_TDI ST6830
S_JTAG_TCK ST6831
S_JTAG_TMS ST6832
S_JTAG_TDO ST6833
+1.05VA_PROC
H_THERMTRIP#
SR2
1KOhm
place near PCH
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUSTek COMPUTER INC.
Title : CPTH (SPI/MISC)
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 19 of 77









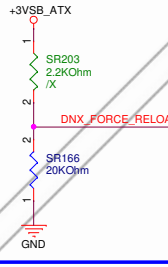
PCH GLITCH ISSUE MITIGATION

Serial ATA Port [3:7] General Purpose Inputs: When configured as SATAGP[3:7],
this is an input pin that is used as an interlock switch status indicator for SATA Port [3:7].
Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPP_F[0:4]. Pin defaults to Native mode as SATAXPCIE[3:7] depends on soft-strap.

GPP_G2 / DNX_FORCE_RELOAD

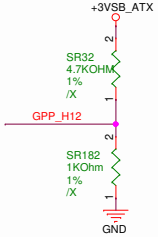
Download and Execute (DnX):IntelR CSME ROM samples this pin any time ROM begins execution.
This includes the following conditions:
- G3 Exit.
- Sx, Moff Exit.
- Cold Reset(Host Reset with Power Cycle) Exit.
- Warm Reset(Host Reset without Power Cycle) Exit if IntelR CSME was shutdown in Warm Reset.

L => No DnX
H => Enter DnX mode
Note : This pin must not be sampled high at the sampling time for normal operation .



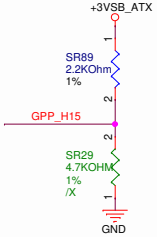
GPP_H12 / SML2ALERT# eSPI Flash Sharing Mode

0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Internal pull-down 20 kohm



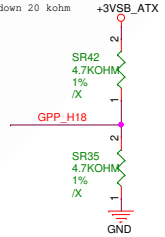
GPP_H15 / SML3ALERT# JTAG ODT Disable

0 = JTAG ODT is disabled (default)
1 = JTAG ODT is enabled
Internal pull-down 20 kohm



GPP_H18 / SML4ALERT# VCCSPI Voltage Configuration

0 = VCCSPI at 3.3 V (Default)
1 = VCCSPI at 1.8 V
Internal pull-down 20 kohm



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTek COMPUTER INC.	Title : CPTH (GPIO_F/G/H)	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q670A1		Rev: R1.00
Date: Monday, July 18, 2022	Sheet 20 of 77		

GPP_R2 / HDA_SDO / HDACPU_SDO
Flash Descriptor Security Override

0: Enable security measures defined in the Flash Descriptor. (Default)
1: Disable Flash Descriptor Security (override).

This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
Internal pull-down 20 kohm

/X
DIS_ME(1-2)
MINI_JUMPER
+3VSB_ATX
ME_UNLOCK_R
HEADER_1X3P
DIS_ME
SR104 1KOhm 1%
52 O_ME_UNLOCK
SR98 0Ohm
A_Z_SDOUT_R
SR31 20KOhm 1% /X
GND

SU1N

Pin	Signal	Pin	Signal
BF48	GPP_S7/SNDW4_DATA/DMIC_DATA0	BA9	DDPA_CTRLDATA
BF47	GPP_S6/SNDW4_CLK/DMIC_CLKA0	AY14	DDPA_CTRLCLK
BG47	GPP_S5/SNDW3_DATA/DMIC_DATA1	BD4	S_DP_C_CTRL_DATA
BE46	GPP_S4/SNDW3_CLK/DMIC_CLKA1	BE1	S_DP_C_CTRL_CLK
BF46	GPP_S3/SNDW2_DATA/DMIC_CLKB1	BE2	S_HDMI_B_CTRL_DATA
BG45	GPP_S2/SNDW2_CLK/DMIC_CLKB0	BB8	S_HDMI_B_CTRL_CLK
BH45	GPP_S1/SNDW1_DATA	AW8	S_HDMI_E_CTRL_DATA
BJ45	GPP_S0/SNDW1_CLK	AY6	S_HDMI_E_CTRL_CLK
		AW9	S_DP_D_CTRL_DATA
		AV11	S_DP_D_CTRL_CLK
		BC9	DDSP_HPDC
		BH7	DDSP_HPDB
		BD3	EDP_HPD
		BE6	GPP_R8
		AY11	GPP_R7
		BB6	GPP_R6
		BJ7	HDA_SDI1
		BE7	A_Z_RST#_R
		BF9	A_Z_SDIN0
		BF7	A_Z_SDOUT_R
		BF8	A_Z_SYNC_R
		BG8	A_Z_BITCLK_R

GPP_S2
GPP_R21/DDPA_CTRLDATA
GPP_R20/DDPA_CTRLCLK
GPP_R19/DDP2_CTRLDATA
GPP_R18/DDP2_CTRLCLK
GPP_R17/DDP1_CTRLDATA
GPP_R16/DDP1_CTRLCLK
GPP_R15/ISH_SPI_MOSI /DDP4_CTRLDATA/GSPI2_MOSI
GPP_R14/ISH_SPI_MISO /DDP4_CTRLCLK/GSPI2_MISO
GPP_R13/ISH_SPI_CLK /DDP3_CTRLDATA/GSPI2_CLK
GPP_R12/ISH_SPI_CS# /DDP3_CTRLCLK/GSPI2_CS0#
GPP_R11/DDSP_HPDC/DISP_MISCC
GPP_R10/DDSP_HPDB/DISP_MISCB
GPP_R9/DDSP_HPDA/DISP_MISCA
GPP_R8
GPP_R7
GPP_R6
GPP_R5/HDA_SDI1
GPP_R4/HDA_RST#
GPP_R3/HDA_SDI0/HDACPU_SDI
GPP_R2/HDA_SDO/HDACPU_SDO
GPP_R1/HDA_SYNC
GPP_R0/HDA_BCLK/HDACPU_BCLK

S_DP_C_CTRL_DATA 32
S_DP_C_CTRL_CLK 32
S_HDMI_B_CTRL_DATA 31
S_HDMI_B_CTRL_CLK 31
S_HDMI_E_CTRL_DATA 34
S_HDMI_E_CTRL_CLK 34
S_DP_D_CTRL_DATA 33
S_DP_D_CTRL_CLK 33
SR16 2 1 100KOhm
SR78 2 1 100KOhm
GND
ST28
ST22
SR172 2 1 33Ohm
SR168 2 1 33Ohm
SR169 2 1 33Ohm
SR165 2 1 33Ohm
A_Z_RST# 36
A_Z_SDIN0 36
A_Z_SDOUT 36
A_Z_SYNC 36
A_Z_BITCLK 36

PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109

SR240 2 /X 1 100KOhm GPP_S2
SR239 2 /X 1 100KOhm GPP_R7
SR237 2 /X 1 100KOhm GPP_R8
GND

+1.8V_A
SR88 1 /X 2 8.2KOhm
SR217 1 2 75KOhm CPU_C10_GATE_N_10
GND

+3VSB_ATX
SR2292 1% /X 1 100KOhm
SR2282 1% 1 100KOhm PCH_CORE_VID1
GND

+3VSB_ATX
SR1862 1% /X 1 100KOhm
SR1842 1% 1 100KOhm PCH_CORE_VID0
GND

SU1M

Pin	Signal	Pin	Signal
AY4	GPP_J11/BSSB_LS_TX	BE15	GPP_I20/GSPI1_CLK
AT8	GPP_J10/BSSB_LS_RX	BF13	GPP_I21/GSPI1_MISO
BB4	GPP_J7/CNV_MFUART2_TXD	BF14	GPP_I10/GSPI1_CS1#/TIME_SYNC1
AV12	GPP_J6/CNV_MFUART2_RXD	BG14	GPP_I19/GSPI1_CS0#
BC4	GPP_J5/CNV_RGI_RSP/UART0_CTS#	BG15 IPD	GPP_I22/GSPI1_MOSI
BC5	GPP_J4/CNV_RGI_DT/UART0_TXD	BG11	GPP_I9/GSPI0_CS1#
BA5	GPP_J3/CNV_BRI_RSP/UART0_RXD	BH11	GPP_I16/GSPI0_CLK
AU6	GPP_J2/CNV_BRI_DT/UART0_RTS#	BF10	GPP_I17/GSPI0_MISO
BA3	GPP_J1/CPU_C10_GATE#	BE12 IPD	GPP_I18/GSPI0_MOSI
BB2	GPP_J0/CNV_PA_BLANKING	BF11	GPP_I15/GSPI0_CS0#
BB54	GPP_K11	BB13	GPP_I13/USB_OC6#/I2C5_SDA
AW53	GPP_K9/CORE_VID1	BD12	GPP_I14/USB_OC7#/I2C5_SCL
BA51	GPP_K3/GSXSRESET#	BA16	GPP_I11/USB_OC4#/I2C4_SDA
AY52	GPP_K2/GSXDIN	AY16	GPP_I12/USB_OC5#/I2C4_SCL
BA53	GPP_K1/GSXSLOAD	BE10	GPP_I8/DDPC_CTRLDATA
BA52	GPP_K0/GSXDOUT	BG9	GPP_I7/DDPC_CTRLCLK
AW52	GPP_K8/CORE_VID0	BG12	GPP_I6/DDPB_CTRLDATA
BB52	GPP_K4/GSXCLK	BF12	GPP_I5/DDPB_CTRLCLK
AV51	GPP_K5/ADR_COMPLETE	BA13	GPP_I4/DDSP_HPD4/DISP_MISC4
		BB15	GPP_I3/DDSP_HPD3/DISP_MISC3
		BD14	GPP_I2/DDSP_HPD2/DISP_MISC2
		BH15	GPP_I1/DDSP_HPD1/DISP_MISC1
		BJ16	GPP_I0/EXT_PWR_GATE#

GPP_J4
GPP_J2
CPU_C10_GATE_N_10
PCH_CORE_VID1
PCH_CORE_VID0
ST23 1 ADR_COMPLETE
69 PCH_CORE_VID1
67,69 PCH_CORE_VID0
For Intel DnX LED at CRB.

0: Integrated CNVi enable
1: Integrated CNVi disable

GPP_I22 GPP_I18
U2_USBOC#914 48
U_USBOC#910 47
U2_USBOC#78 48
DDPC_CTRLDATA
DDPC_CTRLCLK
DDPB_CTRLDATA
DDPB_CTRLCLK
S_HDMI_E_HPD 34
S_DP_D_HPD 33
S_DP_C_HPD 32
S_HDMI_B_HPD 31
EXT_PWR_GATE# 1 ST39
CRB use for PCIe slot PWR Gate.

PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109

GPP_R[12:21]_I[5:8] / DDP[1:4,A:C] _CTRLDATA

0: Port [A:E] is not detected. (default)
1: Port [A:E] is detected.

Internal pull-down 15-40 kohm

+3V

S_HDMI_B_CTRL_CLK	SR84	2	2.2KOhm1
S_HDMI_B_CTRL_DATA	SR85	2	2.2KOhm1
S_DP_C_CTRL_CLK	SR80	2	2.2KOhm1
S_DP_C_CTRL_DATA	SR81	2	2.2KOhm1
S_DP_D_CTRL_CLK	SR82	2	2.2KOhm1
S_DP_D_CTRL_DATA	SR83	2	2.2KOhm1
S_HDMI_E_CTRL_CLK	SR87	2	2.2KOhm1
S_HDMI_E_CTRL_DATA	SR199	2	2.2KOhm1
DDPA_CTRLCLK	SR92	2	2.2KOhm1
DDPA_CTRLDATA	SR97	2	2.2KOhm1
DDPB_CTRLCLK	SR100	2	2.2KOhm1
DDPB_CTRLDATA	SR101	2	2.2KOhm1
DDPC_CTRLCLK	SR202	2	2.2KOhm1
DDPC_CTRLDATA	SR86	2	2.2KOhm1

GPP_J2 / CNV_BRI_DT / UART0_RTS#
XTAL Frequency Selection Bit 0

+1.8V_A
00 = 24 MHz MHz (default)
01 = Reserved
10 = 38.4 MHz
11 = 25 MHz
Internal pull-down 20 kohm
SR181 4.7KOHM 1% /X
GPP_J2
SR174 20KOhm 1% /X
GND

GPP_J4 / CNV_RGI_DT / UART0_TXD
M.2 CNVi Mode Select

+1.8V_A
0: Integrated CNVi enable
1: Integrated CNVi disable
SR180 4.7KOHM 1%
GPP_J4
SR105 20KOhm 1% /X
GND

GPP_I18 / GSPI0_MOSI
No Reboot

+3VSB_ATX
0: Disable "No Reboot" mode. (Default)
1: Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).
Internal pull-down 20 kohm
This function is useful when running ITP/ XDP.
SR213 4.7KOHM 1% /X
GPP_I18
SR30 1KOhm 1% /X
GND

GPP_I22 / GSPI1_MOSI
Boot BIOS Strap (BBS)

+3VSB_ATX
0: BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF)
1: BIOS fetches are routed to the eSPI Peripheral Channel
Internal pull-down 20 kohm
SR185 4.7KOHM 1% /X
GPP_I22
SR201 20KOhm 1% /X
GND

+3VSB_ATX
USB2_OCB_7 SR122 1 8.2KOhm 2

ASUSTek COMPUTER INC.	Title : CPTH (AUDIO/DISPLAY/CNVi)		
	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 21 of 77		

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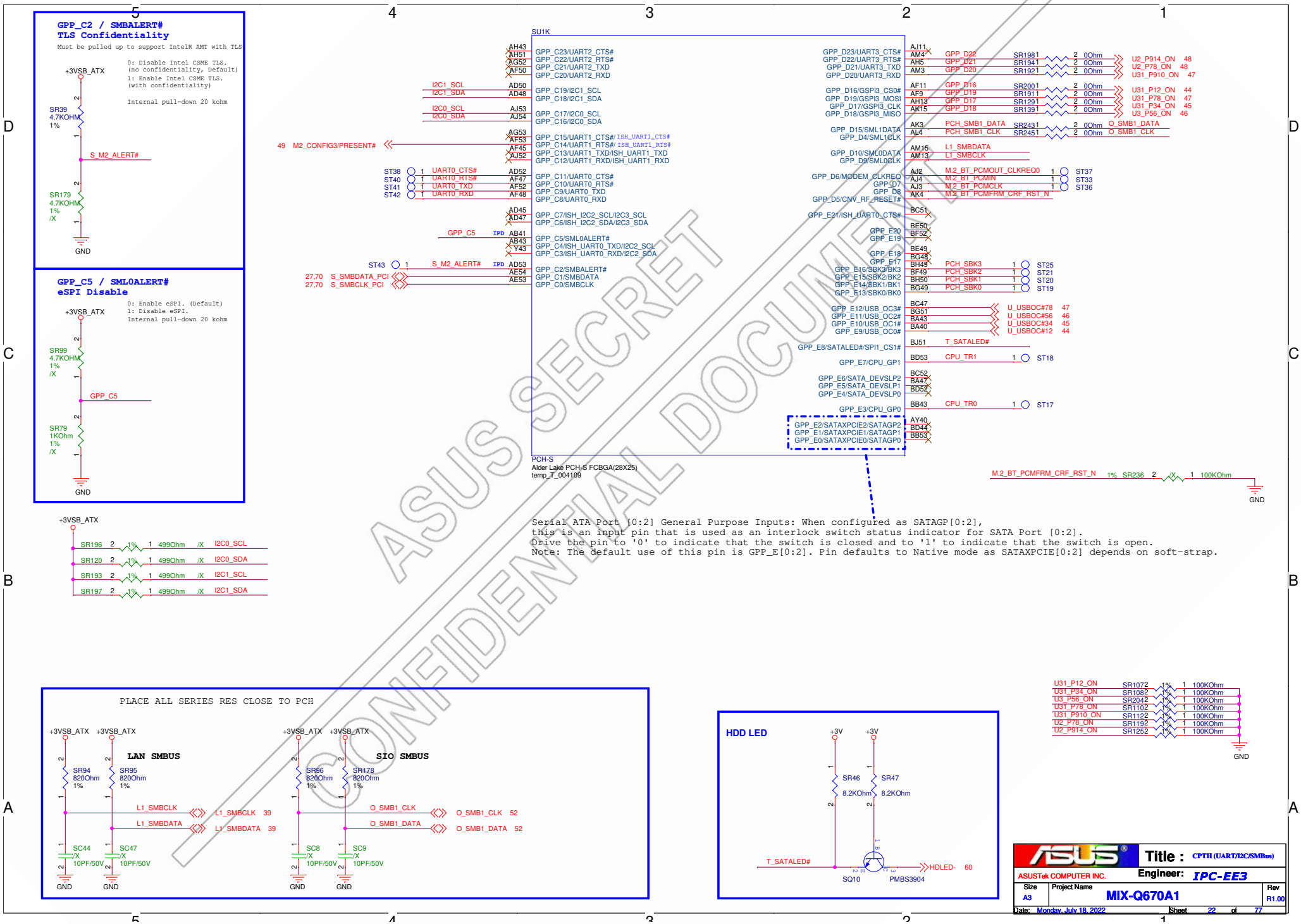
GPP_C2 / SMBALERT#
TLS Confidentiality
Must be pulled up to support IntelR AMT with TLS
0: Disable Intel CSME TLS. (no confidentiality, Default)
1: Enable Intel CSME TLS. (with confidentiality)
Internal pull-down 20 kohm
+3VSB_ATX
SR39 4.7KOHM 1%
S_M2_ALERT#
SR179 4.7KOHM 1% /X
GND
GPP_C5 / SML0ALERT#
eSPI Disable
0: Enable eSPI. (Default)
1: Disable eSPI.
Internal pull-down 20 kohm
SR99 4.7KOHM 1% /X
GPP_C5
SR79 1KOhm 1% /X
SU1K
PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C7/ISH_I2C2_SCL/I2C3_SCL
GPP_C6/ISH_I2C2_SDA/I2C3_SDA
GPP_C5/SML0ALERT#
GPP_C4/ISH_UART0_TXD/I2C2_SCL
GPP_C3/ISH_UART0_RXD/I2C2_SDA
GPP_C2/SMBALERT#
GPP_C1/SMBDATA
GPP_C0/SMBCLK
GPP_D23/UART3_CTS#
GPP_D22/UART3_RTS#
GPP_D21/UART3_TXD
GPP_D20/UART3_RXD
GPP_D16/GSPI3_CS0#
GPP_D19/GSPI3_MOSI
GPP_D17/GSPI3_CLK
GPP_D18/GSPI3_MISO
GPP_D15/SML1DATA
GPP_D4/SML1CLK
GPP_D10/SML0DATA
GPP_D9/SML0CLK
GPP_D6/MODEM_CLKREQ
GPP_D7
GPP_D8
GPP_D5/CNV_RF_RESET#
GPP_E21/ISH_UART0_CTS#
GPP_E20
GPP_E19
GPP_E18
GPP_E17
GPP_E16/SBK3/BK3
GPP_E15/SBK2/BK2
GPP_E14/SBK1/BK1
GPP_E13/SBK0/BK0
GPP_E12/USB_OC3#
GPP_E11/USB_OC2#
GPP_E10/USB_OC1#
GPP_E9/USB_OC0#
GPP_E8/SATALED#/SPI1_CS1#
GPP_E7/CPU_GP1
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_E3/CPU_GP0
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E0/SATAXPCIE0/SATAGP0
M2_CONFIG3/PRESENT#
S_SMBDATA_PCI
S_SMBCLK_PCI
M.2_BT_PCMOUT_CLKREQ0
M.2_BT_PCMIN
M.2_BT_PCMCLK
M.2_BT_PCMFRM_CRF_RST_N
PCH_SBK3
PCH_SBK2
PCH_SBK1
PCH_SBK0
U_USBOC#78
U_USBOC#56
U_USBOC#34
U_USBOC#12
T_SATALED#
CPU_TR1
CPU_TR0
O_SMB1_DATA
O_SMB1_CLK
Serial ATA Port [0:2] General Purpose Inputs: When configured as SATAGP[0:2],
this is an input pin that is used as an interlock switch status indicator for SATA Port [0:2].
Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPP_E[0:2]. Pin defaults to Native mode as SATAXPCIE[0:2] depends on soft-strap.
PLACE ALL SERIES RES CLOSE TO PCH
LAN SMBUS
SIO SMBUS
SR94 820Ohm 1%
SR95 820Ohm 1%
SR96 820Ohm 1%
SR178 820Ohm 1%
L1_SMBCLK
L1_SMBDATA
O_SMB1_CLK
O_SMB1_DATA
SC44 /X 10PF/50V
SC47 /X 10PF/50V
SC8 /X 10PF/50V
SC9 /X 10PF/50V
HDD LED
SR46 8.2KOHM
SR47 8.2KOHM
SQ10 PMBS3904
HDLED-
ASUSTek COMPUTER INC.
Title : CPTH (UART/I2C/SMBus)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 22 of 77
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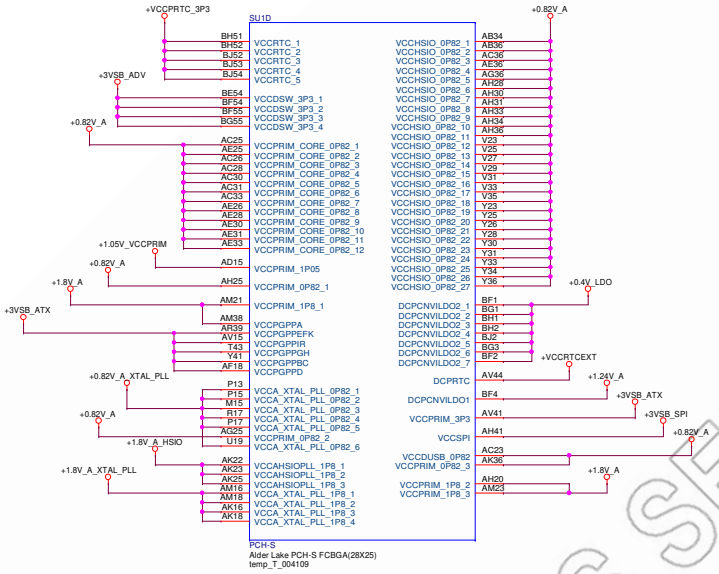
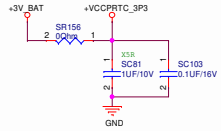


GPIO Voltage Level

Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+1.8V_A
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSB_ATX
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSB_ATX
GPP_D	VCCPGPPD	1.8V or 3.3V	+3VSB_ATX
GPP_E	VCCPGPPEFK	1.8V or 3.3V	+3VSB_ATX
GPP_F	VCCPGPPEFK	1.8V or 3.3V	+3VSB_ATX
GPP_G	VCCPGPPGH	1.8V or 3.3V	+3VSB_ATX
GPP_H	VCCPGPPGH	1.8V or 3.3V	+3VSB_ATX
GPP_I	VCCPGPPIR	1.8V or 3.3V	+3VSB_ATX
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPP_K	VCCPGPPEFK	1.8V or 3.3V	+3VSB_ATX
GPP_R	VCCPGPPIR	1.8V or 3.3V	+3VSB_ATX
GPP_S	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPD	VCCDSW_3P3	3.3V Only	+3VSB_ATX

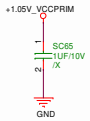
Other Power

SC81, SC103 Place close to the PCH package edge, <10mm



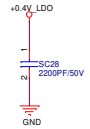
SC31 Place close to the PCH package edge, <5mm
Plan width need >3mm

SC65 Place close to the PCH package edge, <5mm



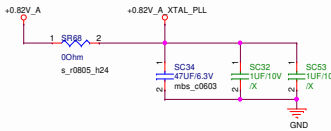
SC27 Place close to the PCH package edge, <5mm
Plan width need >2mm

SC28 Place close to the PCH package edge, <5mm
Plan width need >2mm



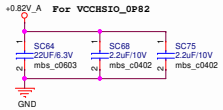
+0.82A

SC34 Place close to the PCH package edge, <10mm
Plan width need >4mm
Need GND shielding.



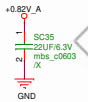
SC32, SC53 Place close to the PCH package edge, <5mm

SC64 Place close to the PCH package edge, <10mm



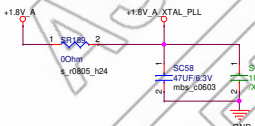
SC68, SC75 Place close to the PCH package edge, <5mm

SC35 Place close to the PCH package edge, <10mm
Plan width need >8mm

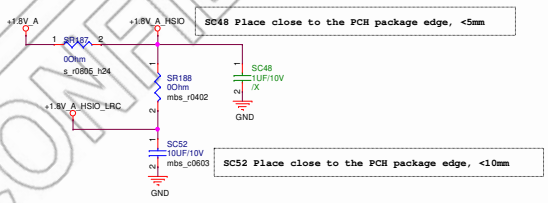


+1.8V_A

SC58 Place close to the PCH package edge, <10mm
Plan width need >3mm
Need GND shielding.



SC55 Place close to the PCH package edge, <5mm



SC48 Place close to the PCH package edge, <5mm

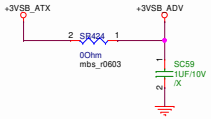
SC52 Place close to the PCH package edge, <10mm

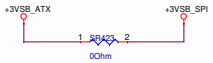
SC66 Place close to the PCH package edge, <5mm
Plan width in package need >3mm, outside need >8mm

+3VSB_ATX

SC67 Place close to the PCH package edge, <5mm
Plan width need >5mm

SC59 Place close to the PCH package edge, <10mm





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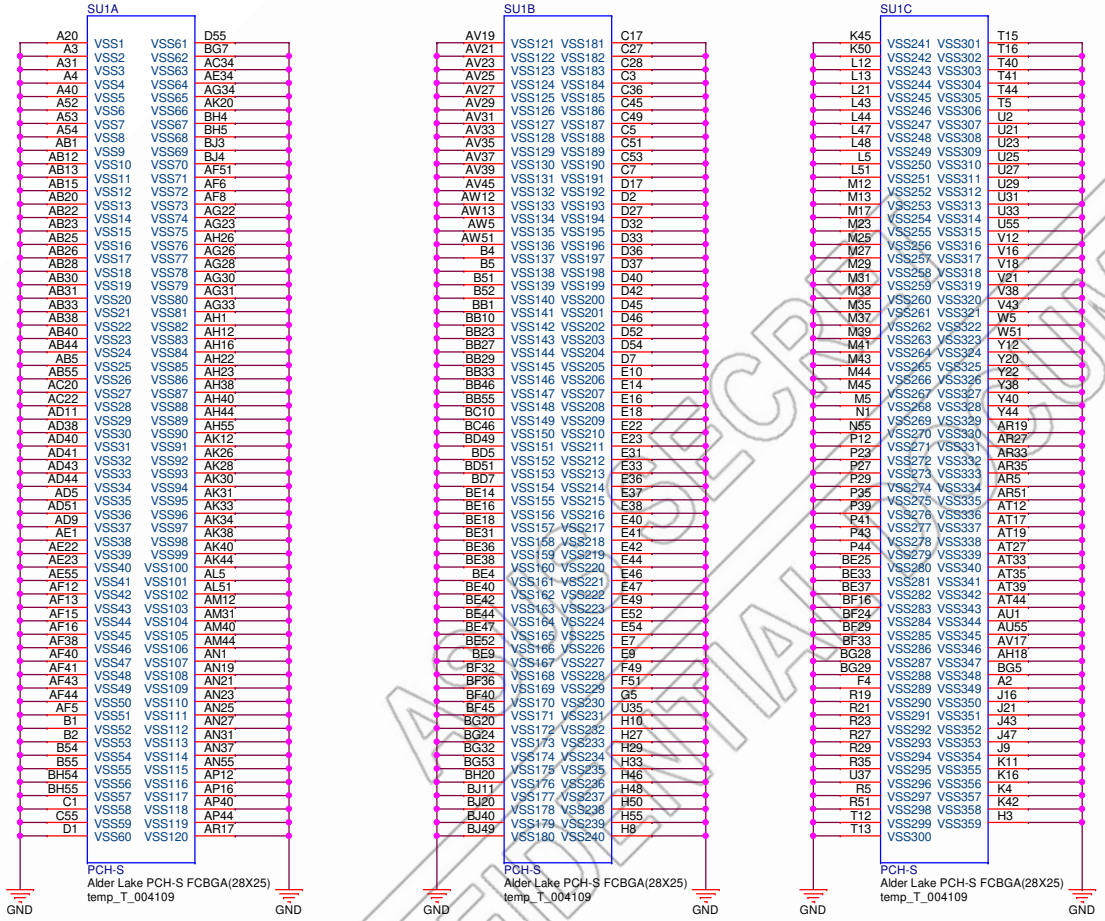
ASUS	Title : KPTH (POWER)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size C	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 23 of 77		



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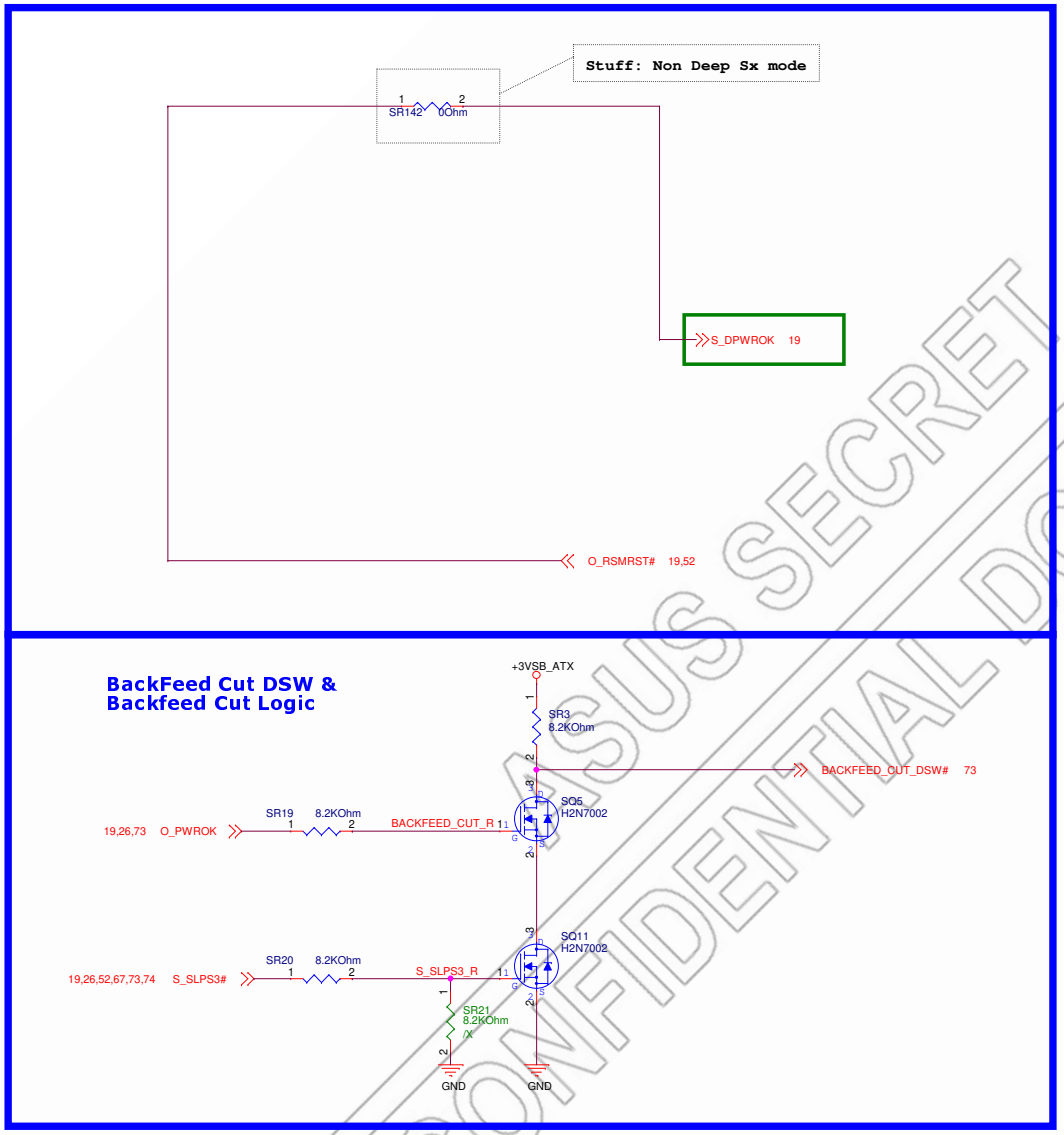
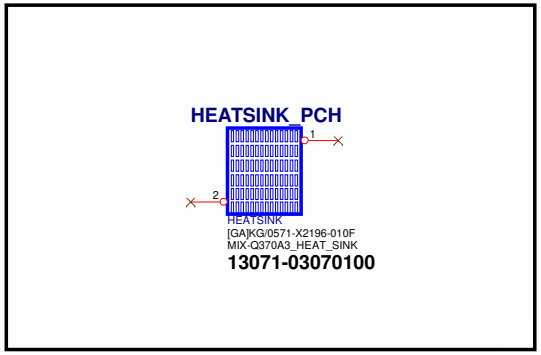
ASUSTek COMPUTER INC.	Title : CPTH (GND)		
	Engineer: IPC-EE3		
Size B	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 24 of 77		

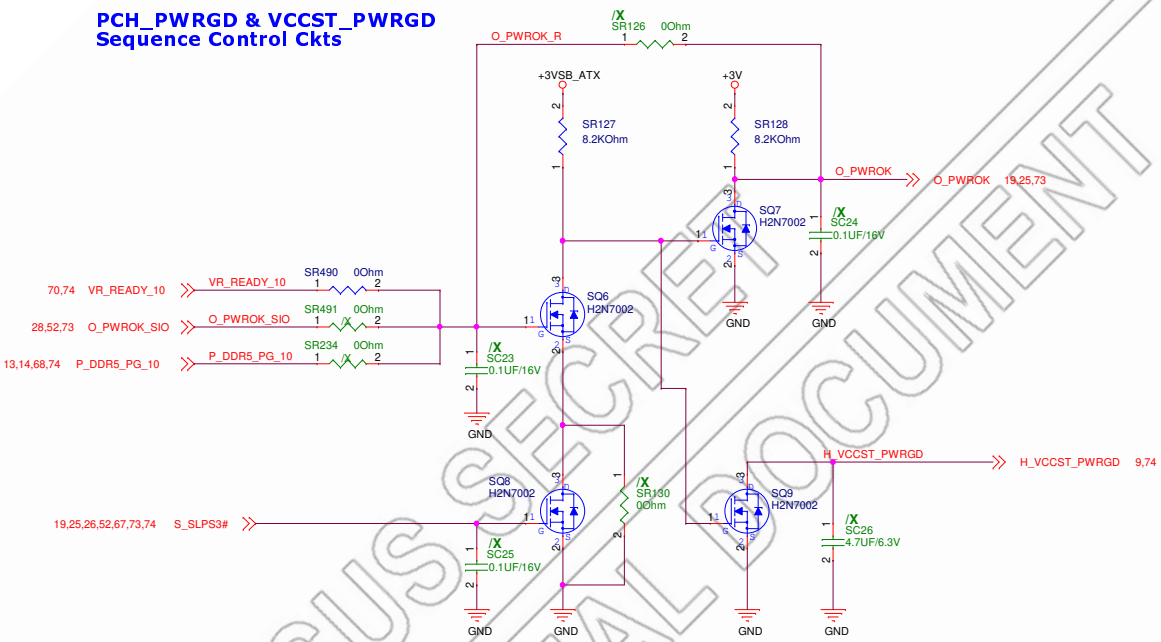




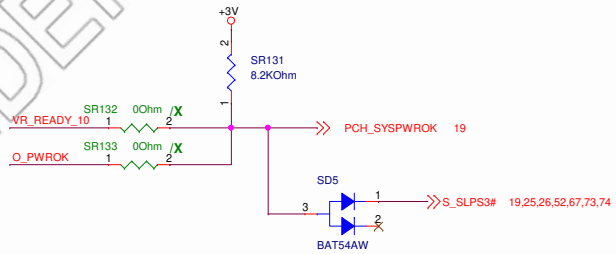
ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : CPTH (DSW SEQUENCE)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 25 of 77	

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

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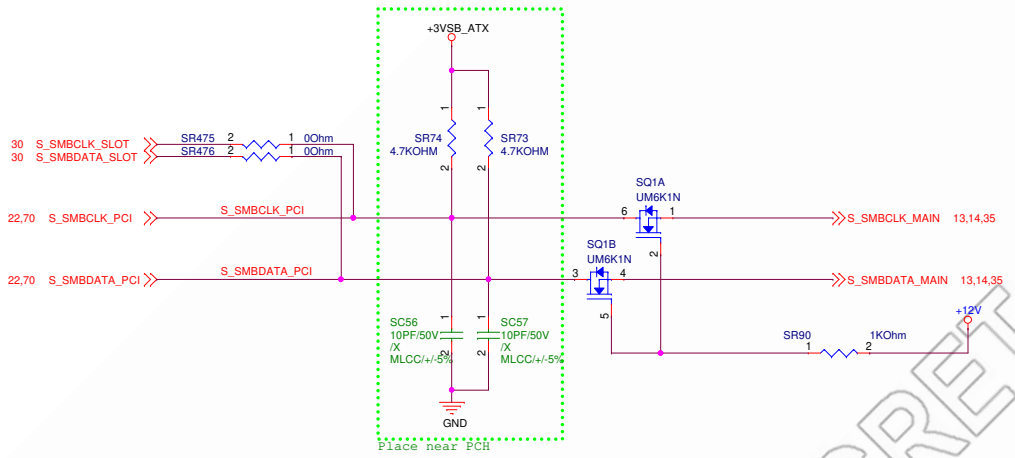
ASUS	Title : CETH (PCH/SYS/PROC_PWROK)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 26 of 77	

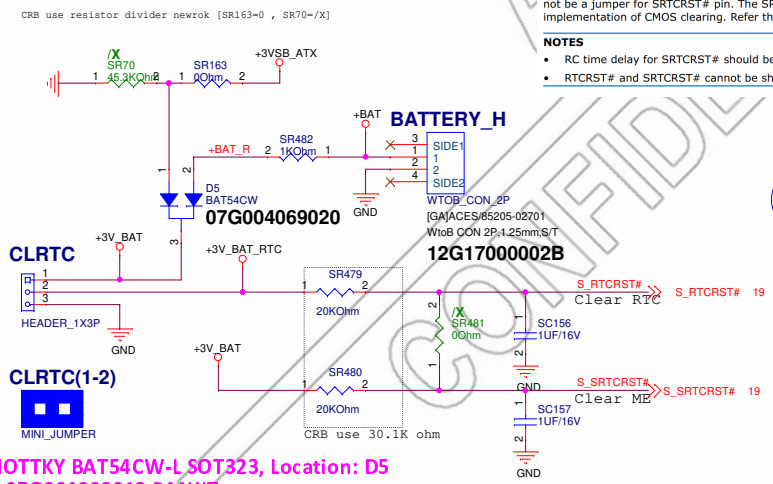


RTC External SRTCRST# Circuit

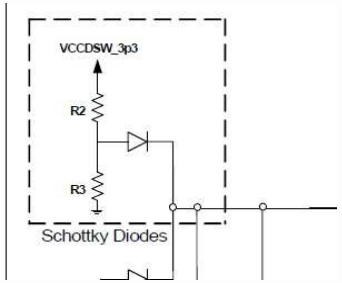
The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18~25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer the figure above external circuit for PCH RTC.

NOTES

- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.



BATTERY
MAXELL/CR2032-HAT00(LF)
0B100-00020700



SCHOTTKY BAT54CW-L SOT323, Location: D5
1st : 07G004203013 PANJIT
2nd : 07G004069020 PANJIT
3rd : 07G004145011 PHILIPS

ASUS SECRET
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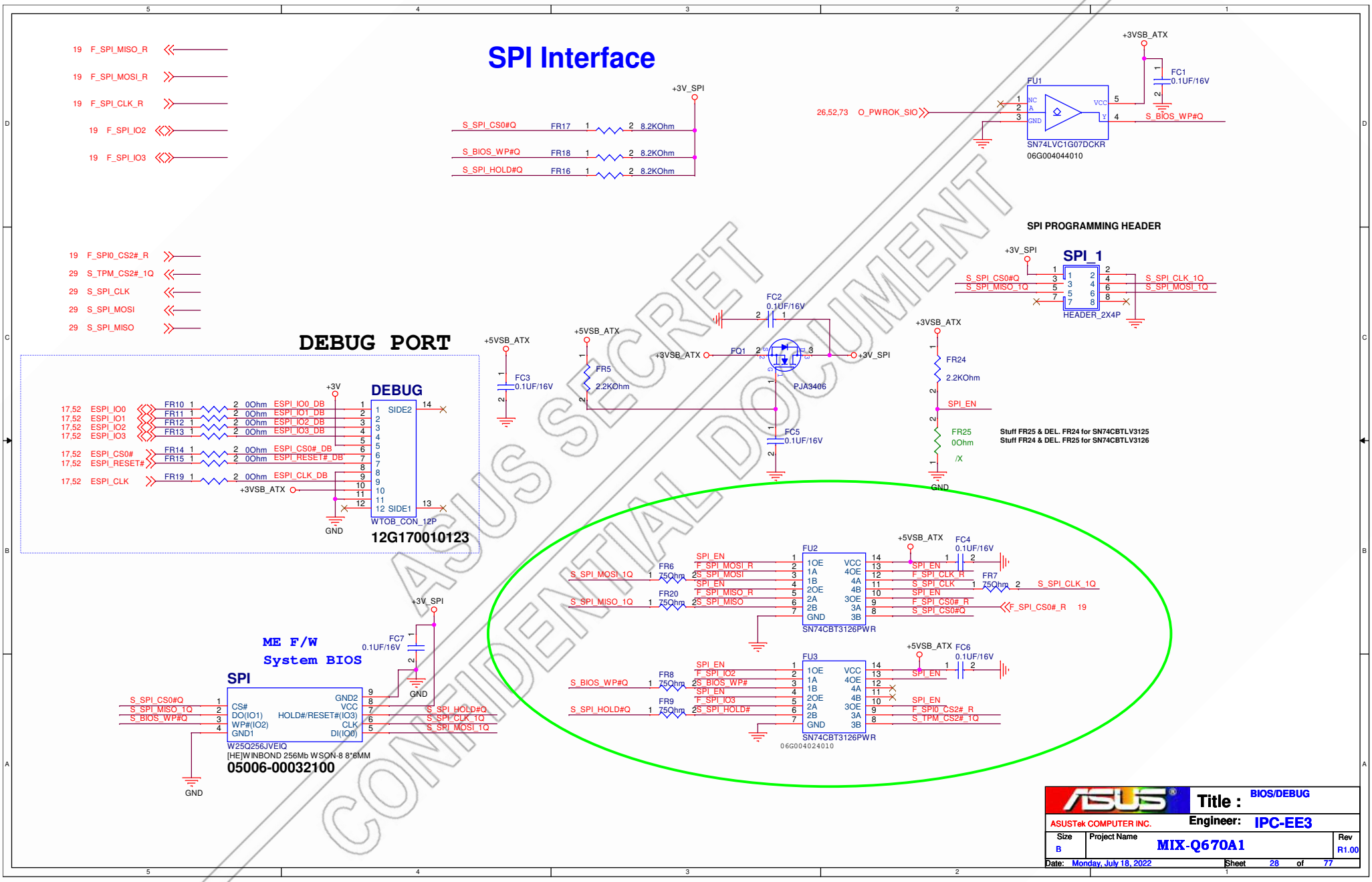
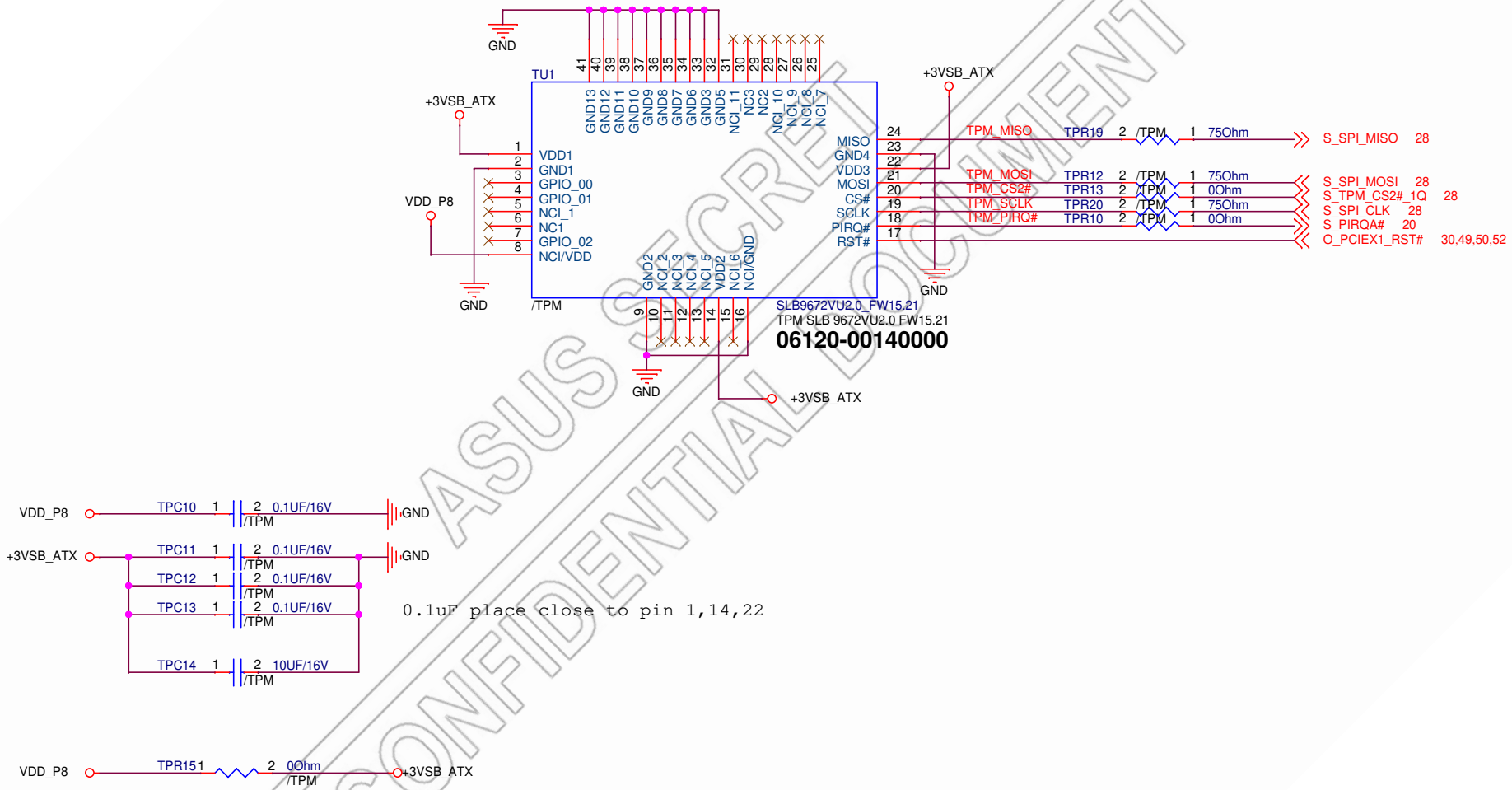
ASUS	Title : CPTH (SMBUS/CLRTC)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 27 of 77		

SPI Interface

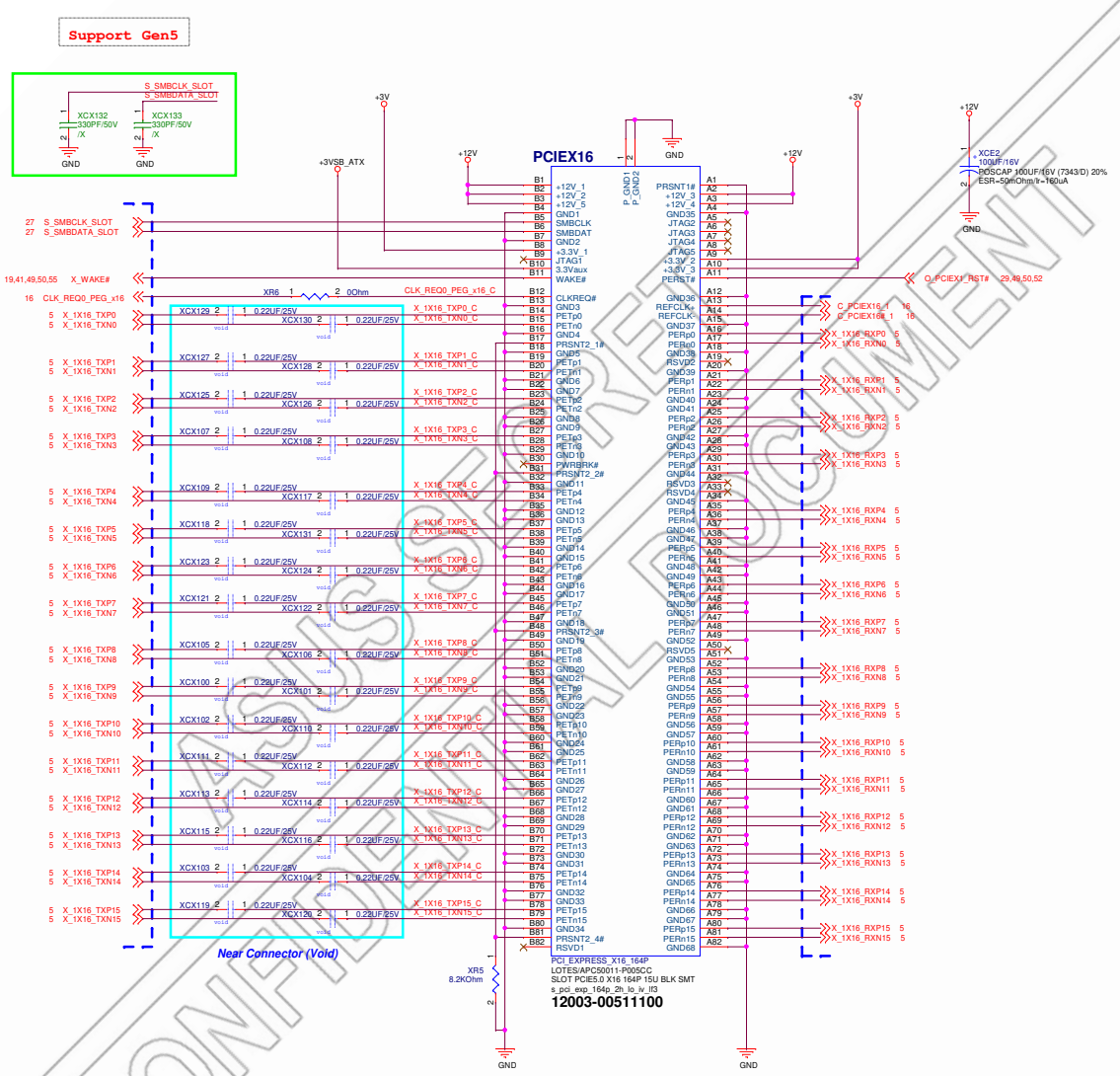


TPM



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : TPM SLB 9672VU2.0		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A4	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 29 of 77		



CONFIDENTIAL DOCUMENT

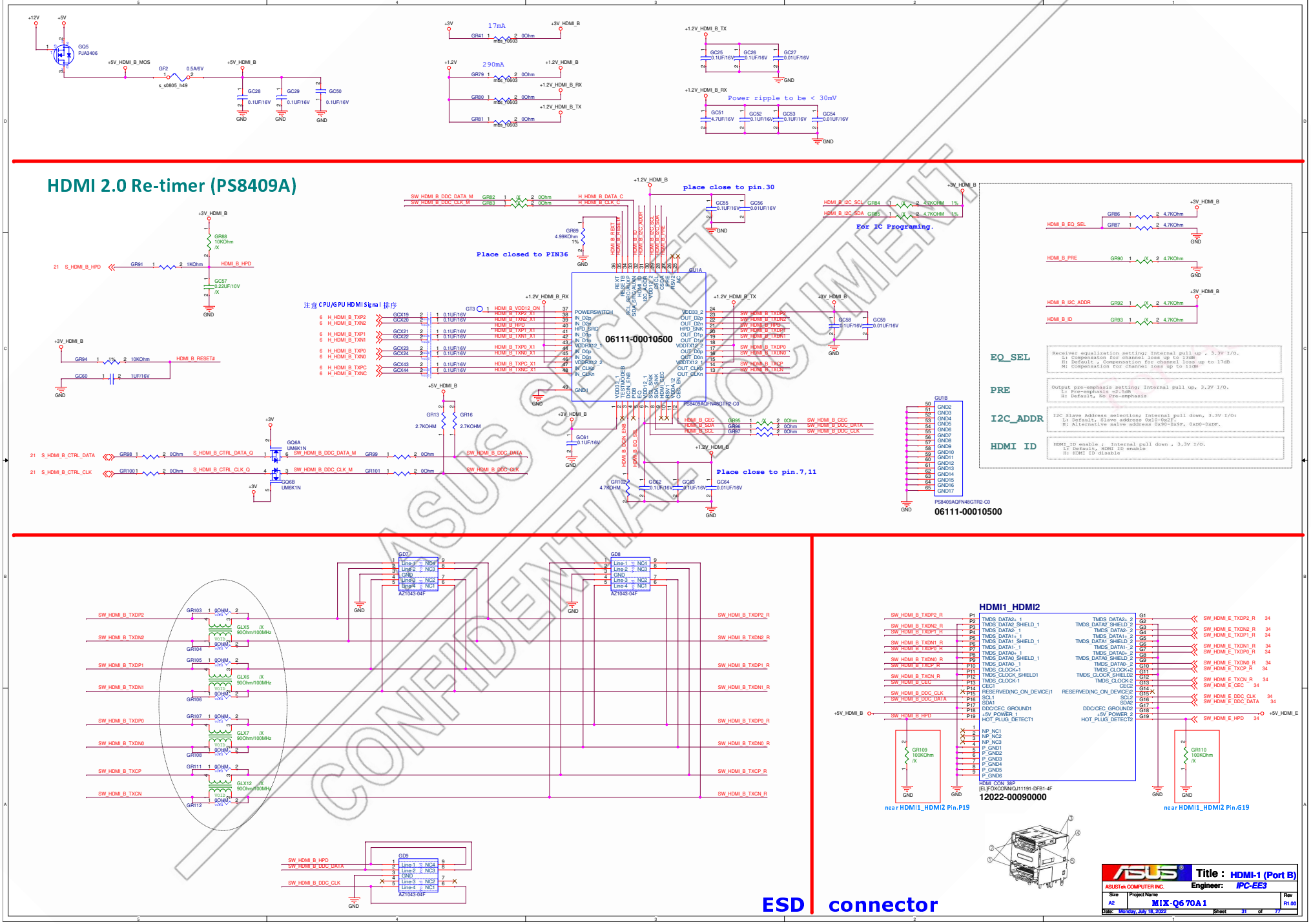
ASUSTeK COMPUTER INC.

Title : PCIEX16

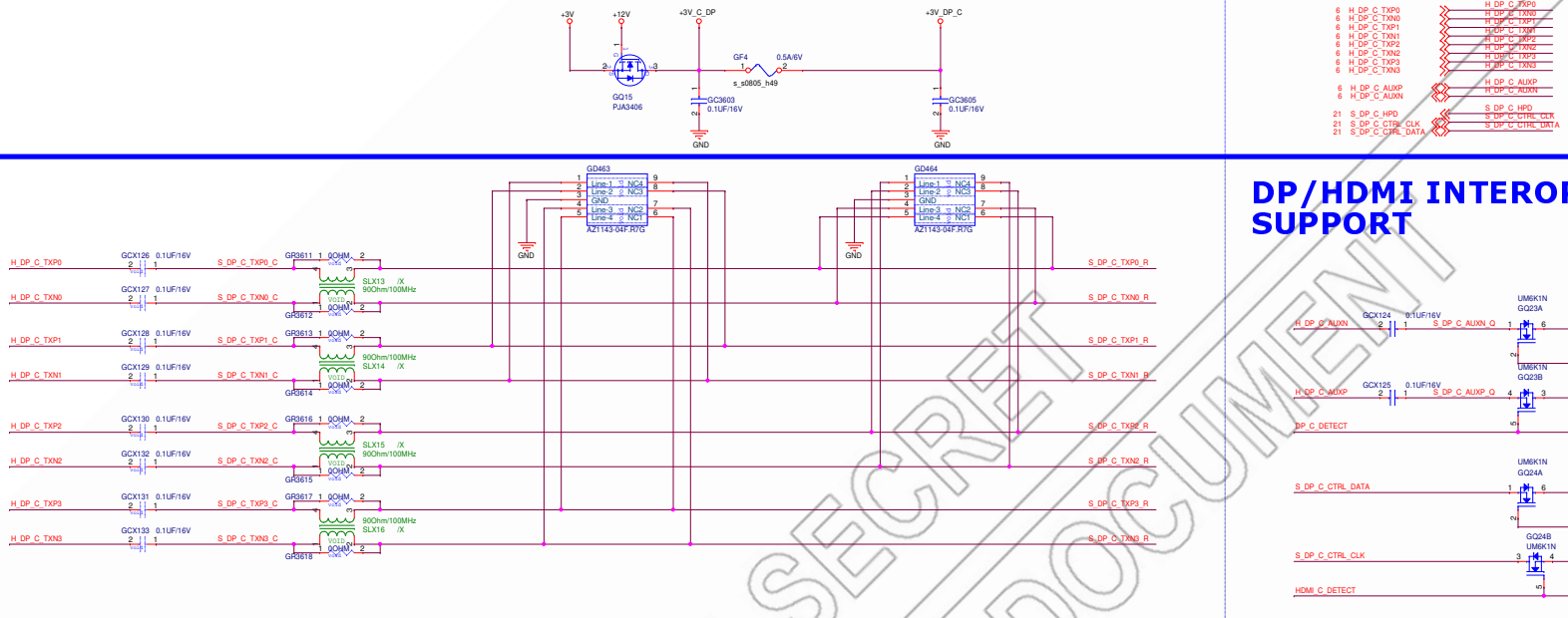
Engineer: IPC-EE3

Size	Project Name	Rev
C	MIX-Q670A1	R1.00

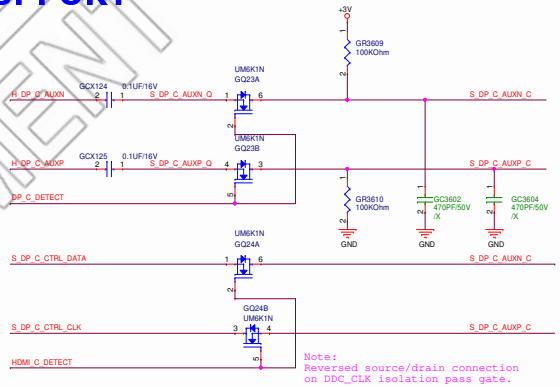
Date: Monday, July 18, 2022 Sheet 30 of 77



ASUS SECRET CONFIDENTIAL DOCUMENT

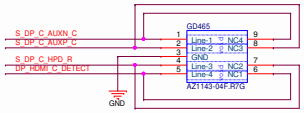


DP/HDMI INTEROPERABILITY SUPPORT

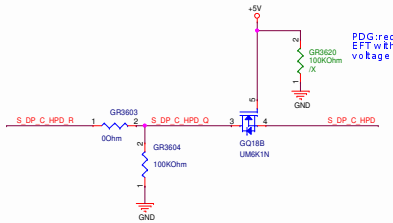


For DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit

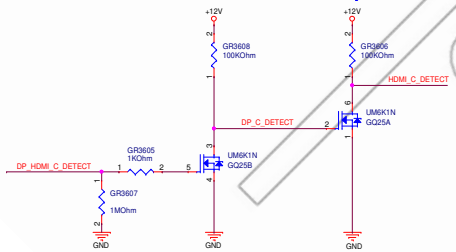
ESD

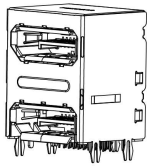


HPD



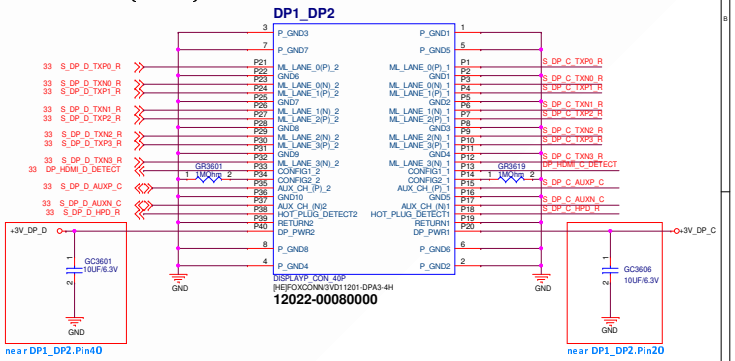
For HDMI/DP detect





DP-2 (Port D)

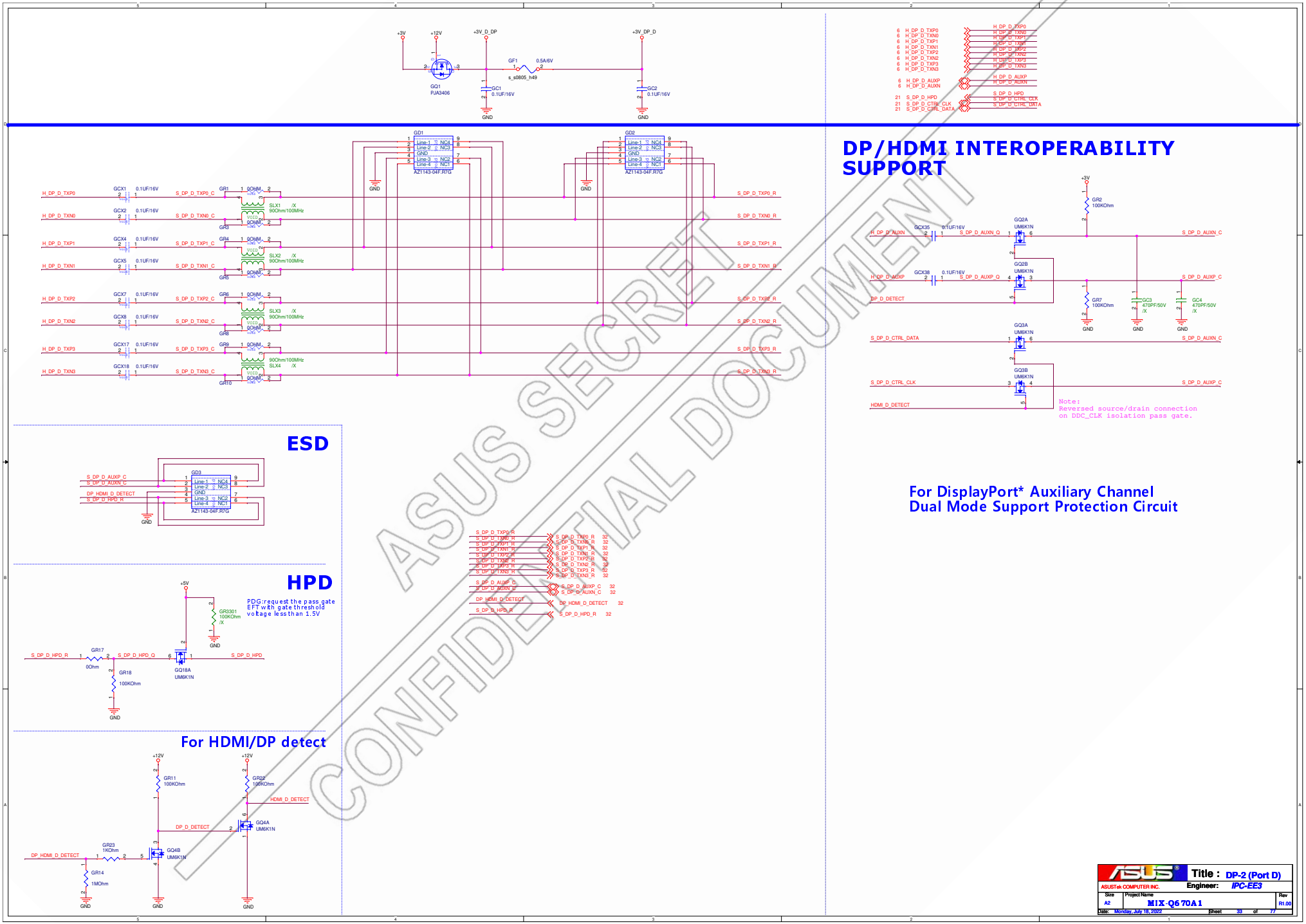
DP-1 (Port C)

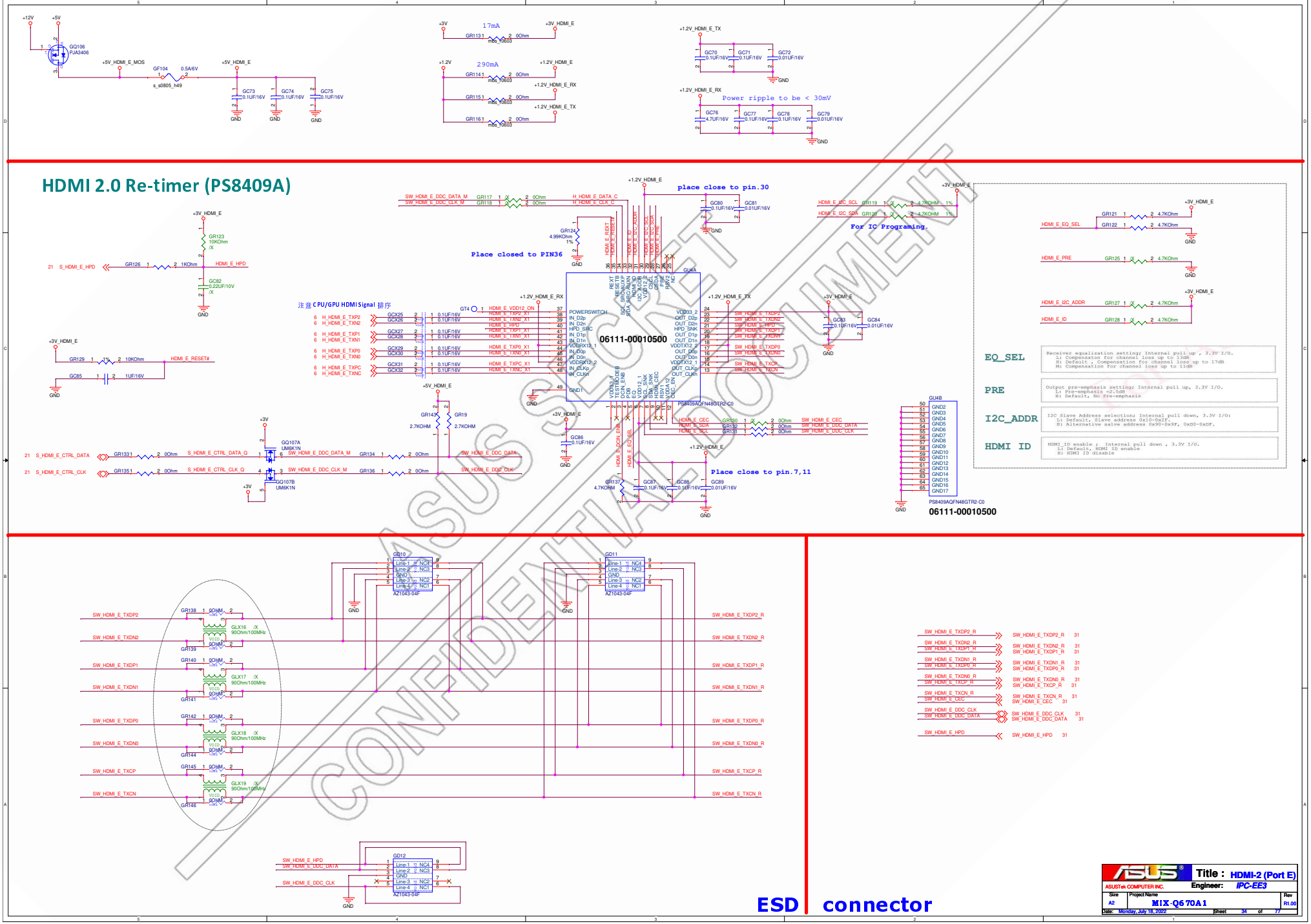


connector

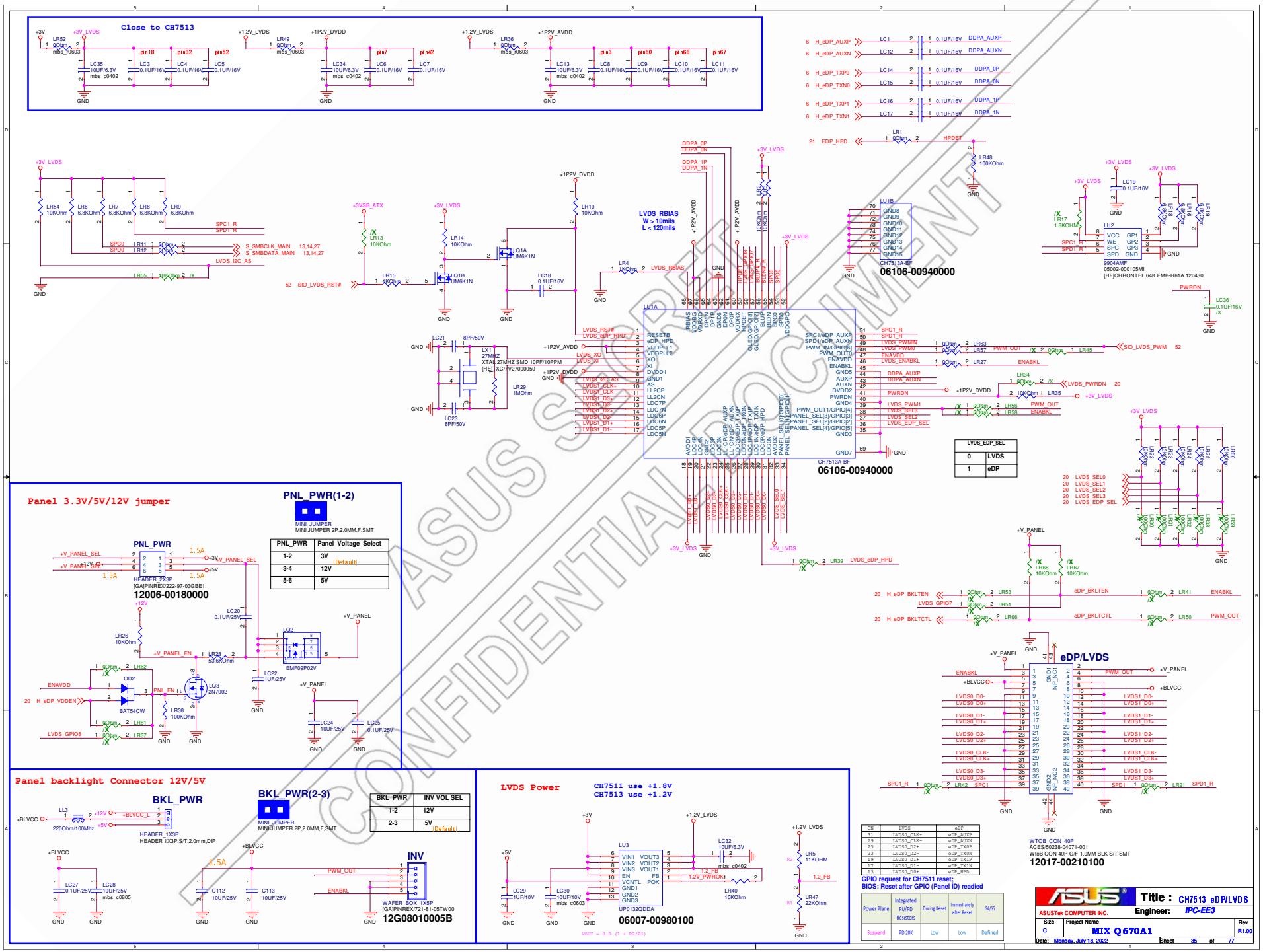
ASUS	Title : DP-1 (Port C)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: A2	Project Name: MIX-Q670A1		Rev: R1.00
Date: Monday, July 18, 2022	Sheet 32 of 77		

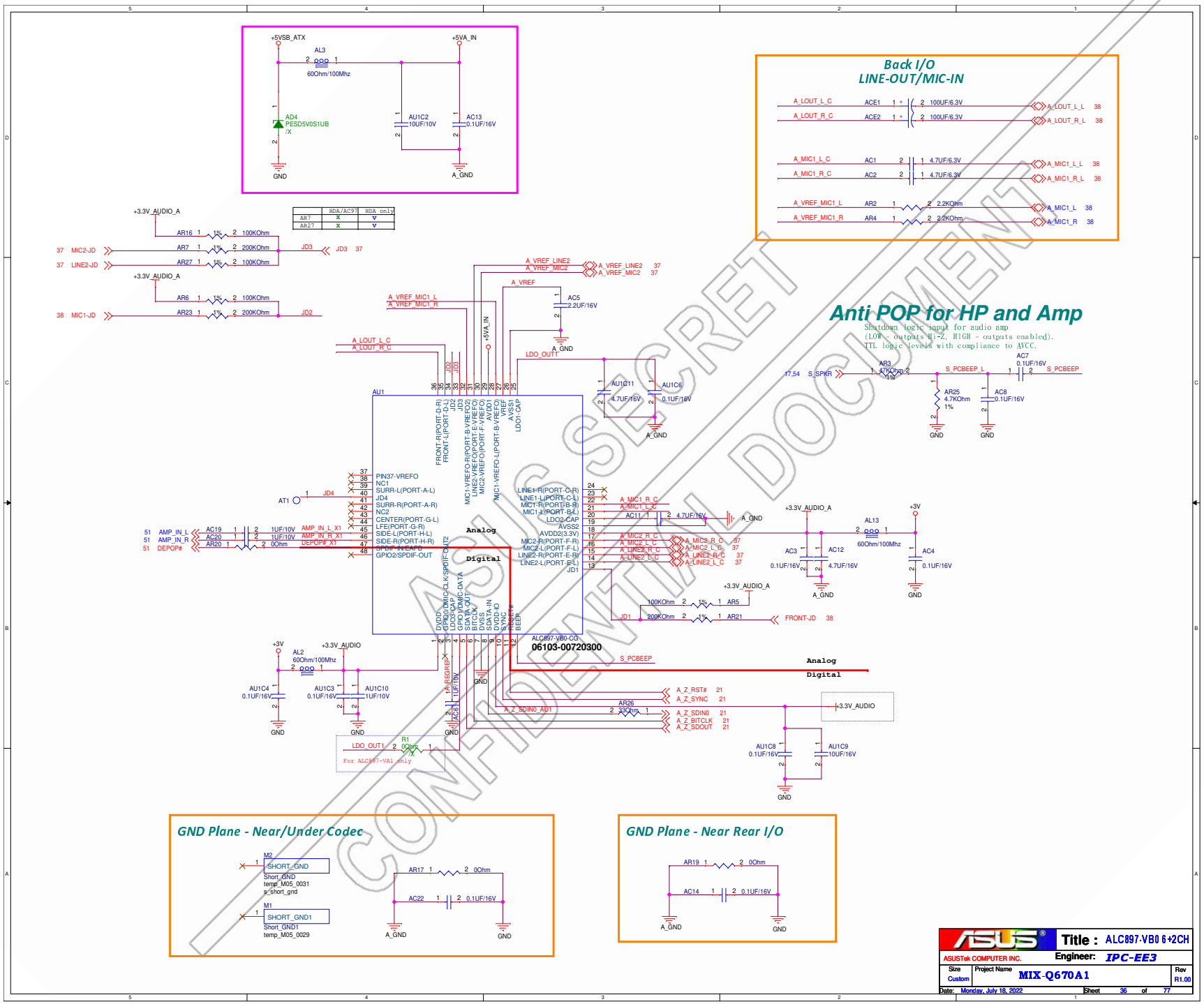
ASUS SECRET
CONFIDENTIAL DOCUMENT


DP/HDMI INTEROPERABILITY SUPPORT
For DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit
ESD
HPD
PDG:request the pass gate EFT with gate threshold voltage lessthan 1.5V
For HDMI/DP detect
Note: Reversed source/drain connection on DDC_CLK isolation pass gate.
ASUS SECRET
CONFIDENTIAL DOCUMENT
Title : DP-2 (Port D)
Engineer: IPC-EE3
ASUSTek COMPUTER INC.
Size A2
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 33 of 77

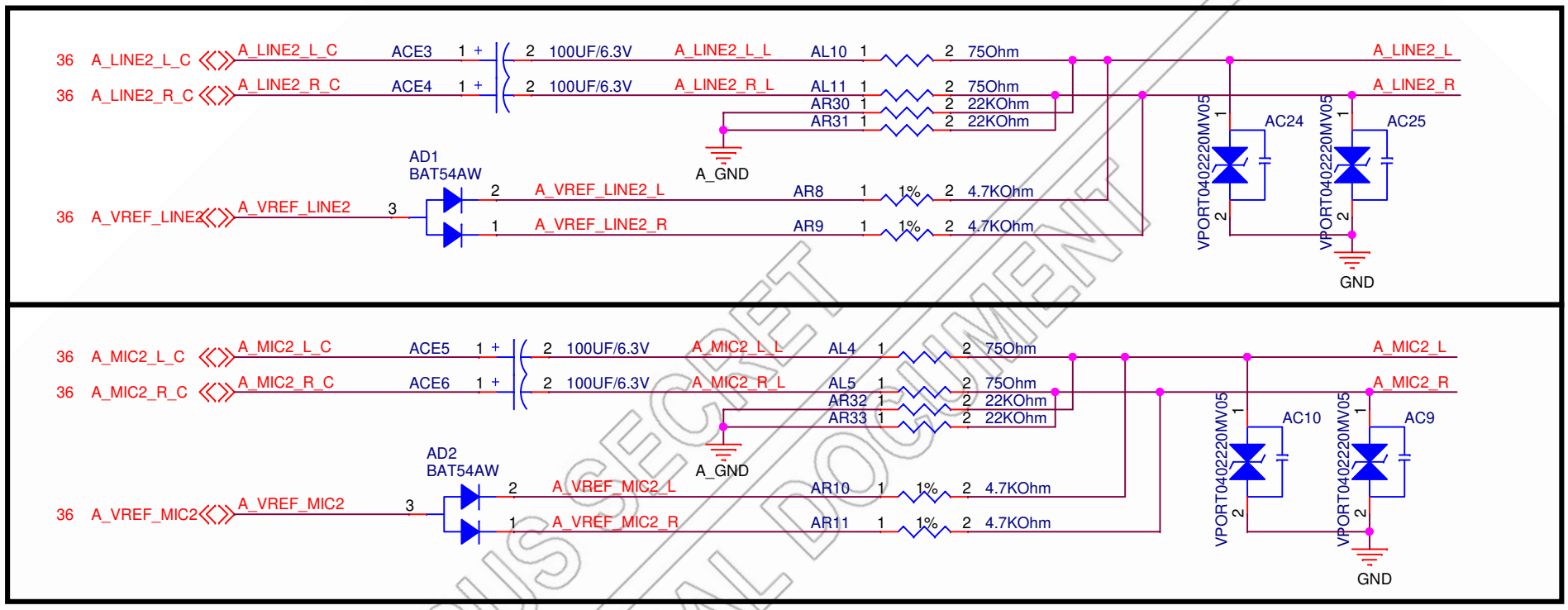


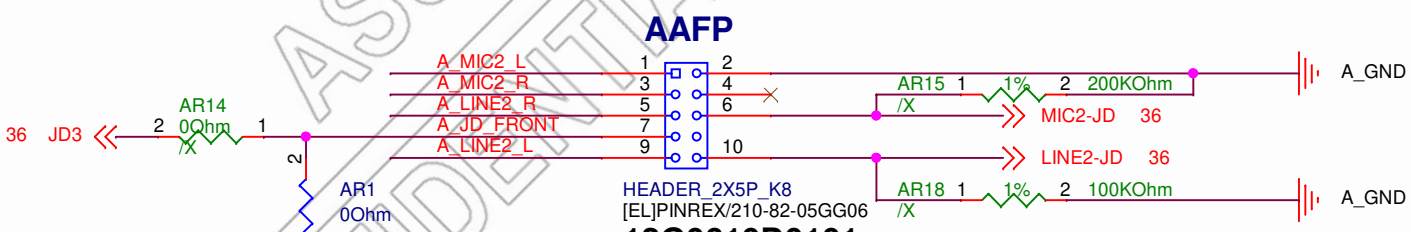
ASUS SECRET DOCUMENT
CONFIDENTIAL


Close to CH7513
Panel 3.3V/5V/12V jumper
PNL_PWR(1-2)
MINI_JUMPER
MINI JUMPER 2P,2.0MM,F,SMT
PNL_PWR
HEADER_2X3P
[GAPINREX]222-97-03GBE1
12006-00180000
PNL_PWR | Panel Voltage Select
1-2 | 3V (Default)
3-4 | 12V
5-6 | 5V
Panel backlight Connector 12V/5V
BKL_PWR
HEADER_1X3P
HEADER 1X3P,S/T,2.0mm,DIP
BKL_PWR(2-3)
MINI_JUMPER
MINI JUMPER 2P,2.0MM,F,SMT
BKL_PWR | INV VOL SEL
1-2 | 12V
2-3 | 5V (Default)
INV
WAFER_BOX_1X5P
[GAPINREX]721-81-05TW00
12G08010005B
LVDS Power
CH7511 use +1.8V
CH7513 use +1.2V
06007-00980100
LVDS_RBIAS
W > 10mils
L < 120mils
CH7513A-BF
06106-00940000
LVDS_EDP_SEL
0 | LVDS
1 | eDP
eDP/LVDS
WTOB_CON_40P
ACES/50238-04071-001
WtoB CON 40P G/F 1.0MM BLK S/T SMT
12017-00210100
GPIO request for CH7511 reset;
BIOS: Reset after GPIO (Panel ID) readied
Power Plane | Integrated PU/PD Resistors | During Reset | Immediately after Reset | S4/S5
Suspend | PD 20K | Low | Low | Defined
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Title : CH7513_eDP/LVDS
Size C
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 35 of 77



ASUS SECRET
CONFIDENTIAL DOCUMENT





	HDA/AC97	HDA only
AR1	x	v
AR14	v	x
AR15	v	x
AR18	v	x

ASUS SECRET
CONFIDENTIAL DOCUMENT

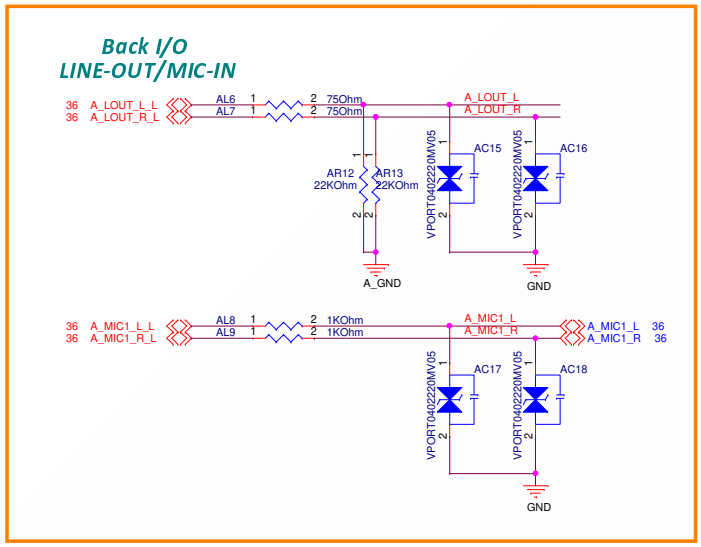
ASUSTek COMPUTER INC.

Title : ALC897-VB0 6+2CH

Engineer: IPC-EE3

Size	Project Name	Rev
Custom	MIX-Q670A1	R1.00

Date: Monday, July 18, 2022 Sheet 37 of 77

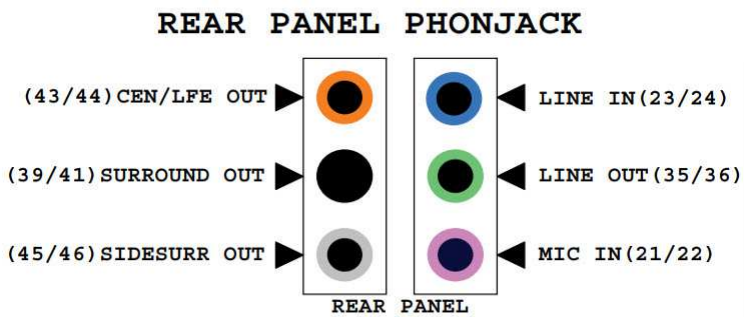


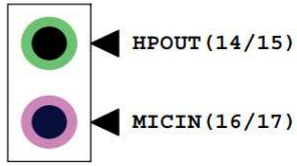
SPDIF Optical

A-11

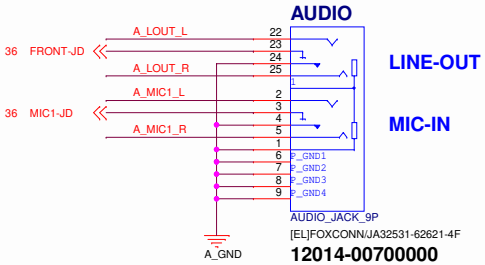
SPDIF Optical (High Rise)

A-12





ALC897Q (7.1 + 2 Channel)
REAR Panel: 6 re-tasking audio jacks
FRONT Panel: 2 re-tasking audio jacks



ASUS SECRET
CONFIDENTIAL DOC

ASUS	Title : ALC897-VB0 6+2CH	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 38 of 77	

若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.

R1.00
Ref to page.104 +5VDUAL/5V_DUAL_USBKB*

+L1_I219_+3VSB
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.

1.3

Standard Circuit	
LAN	I218V
REV.	L1_1.3

/X

I218V

PCIE IF
勿接在chipset PCIE port0

16 C_PCIE_L1
16 C_PCIE_L1#
18 X_L1X1_RXP
18 X_L1X1_RXN
18 X_L1X1_TXP
18 X_L1X1_TXN

L1CX1 2 — 1 0.1UF/16V X7R — X_L1X1_RXP_C
L1CX2 void — 1 0.1UF/16V X7R — X_L1X1_RXN_C
Close to PHY
SL1CX3 2 — 1 0.1UF/16V X7R — X_L1X1_TXP_C
SL1CX4 2 void — 1 0.1UF/16V X7R — X_L1X1_TXN_C
Close to Chipset

22 L1_SMBCLK
22 L1_SMBDATA
L1C1 2 — 1 15PF/50V NPO /X
L1C2 2 — 1 15PF/50V NPO /X
Close to PHY
GND

19 L1_LAN_DISABLE#

2015/04/16
L1R100 1 — 2 8.2KOhm
L1R101 1 — 2 8.2KOhm /X
+L1_I219_+3VSB
GND

L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.

L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

+L1_I219_+3VSB
LT1 LT2
L1R18 1 — 2 8.2KOhm /X — L1_TP_JDI
L1R19 1 — 2 8.2KOhm /X — L1_TP_TDO
L1_TMS
L1_TCK
L1R20 1 — 2 2.7KOHM — L1_TESTEN
CRB 1K
GND

+L1_I219_+3VSB
CRB : L1R3 UNSTUFF FOR LPT-H
L1R9 10KOhm — L1_CLKREQN
L1R3 0Ohm
16 CLK_REQ15_LAN#

17,41,52 S_PLTRST#
L1C29 2 — 1 10PF/50V NPO /X
GND

Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0
+L1_I219_0.9V
L1U1C8 0.1UF/16V /X
L1U1C16 0.1UF/16V /X
L1U1C40 0.1UF/16V /X
L1U1C47 0.1UF/16V /X
GND

09016-00048300
L1L1 4.7UH — L1_CTRLP
L1U1C50 10UF/16V /X
L1U1C49 0.1UF/16V
L1U1C7 22UF/6.3V X5R
GND
L1L1
Idc_min=500 mA
Rdc_max=100 mohm
Placement rule:
1.Place close to L1U1
2.Trace length < 500mil
3.Trace wide > 20mil

L1U1

Pin	Signal
44	PE_CLKP
45	PE_CLKN
38	PETp
39	PETn
41	PERp
42	PERn
28	SMB_CLK
31	SMB_DATA
3	LAN_DISABLE_N
32	JTAG_TDI
34	JTAG_TDO
33	JTAG_TMS
35	JTAG_TCK
30	TEST_EN
48	CLK_REQ_N
36	PE_RST_N
46, 47, 37, 43, 11, 8, 40, 22, 16	VDD0P9_46, VDD0P9_47, VDD0P9_37, VDD0P9_43, VDD0P9_11, VDD0P9_8, VDD0P9_40, VDD0P9_22, VDD0P9_16
7	CTRL0P9
50, 51, 52, 53	GND1, GND2, GND3, GND4
13, 14, 17, 18, 20, 21, 23, 24	MDI_PLUS[0], MDI_MINUS[0], MDI_PLUS[1], MDI_MINUS[1], MDI_PLUS[2], MDI_MINUS[2], MDI_PLUS[3], MDI_MINUS[3]
9	XTAL_OUT
10	XTAL_IN
25	LED2
27	LED1
26	LED0
5	VDD3P3_IN
1	RSVD1_VCC3P3
2	LANWAKE_N
6	SVR_EN_N
4, 15, 19, 29	VDD3P3_4, VDD3P3_15, VDD3P3_19, VDD3P3_29
12	RBIAS
49	GND_EPAD

WGI219LM
06112-00020100

MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch

L1_MDI_0+ 40
L1_MDI_0- 40
L1_MDI_1+ 40
L1_MDI_1- 40
L1_MDI_2+ 40
L1_MDI_2- 40
L1_MDI_3+ 40
L1_MDI_3- 40

L1_XOUT
L1_XIN
L1R6 0Ohm — L1_XOUT_R
L1X1 25MHZ [HF]TROQ/RL25000866 SMD 07009-00024400
L1C3 10PF/50V NPO
L1C4 10PF/50V NPO
GND

L1X1,L1C7,L1C8
Placement rule:
1.Place close to L1U1
2.Trace length <1inch

+L1_I219_+3VSB
L1R2 300OHM
L1_ACTLEDP 40

L1_LED2
L1R1 1 — 2 300OHM
L1_LINK100# 40
L1_LINK1000# 40
L1_ACTLEDN 40

CRB pull up 4.7Kohm
+L1_I219_+3VSB
Close to pin5
L1U1C5 0.1UF/16V
L1U1C48 22UF/6.3V X5R
GND

+L1_I219_+3VSB
L1R21 4.7KOhm 1%
L1R4 4.7KOHM /X

+L1_I219_+3VSB
L1R22 4.7KOhm 1%

L1_RSVD
L1_SVR_EN
L1R26 0Ohm
GND

L1_LAN_WAKE# 19

L1_LAN_WAKE#
Must be connected to PCH's LANWAKE

L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電

+L1_I219_+3VSB
L1U1C4 1UF/16V
GND

L1_RBIAS
L1R16 1 — 2 3.01KOHM 1%
GND

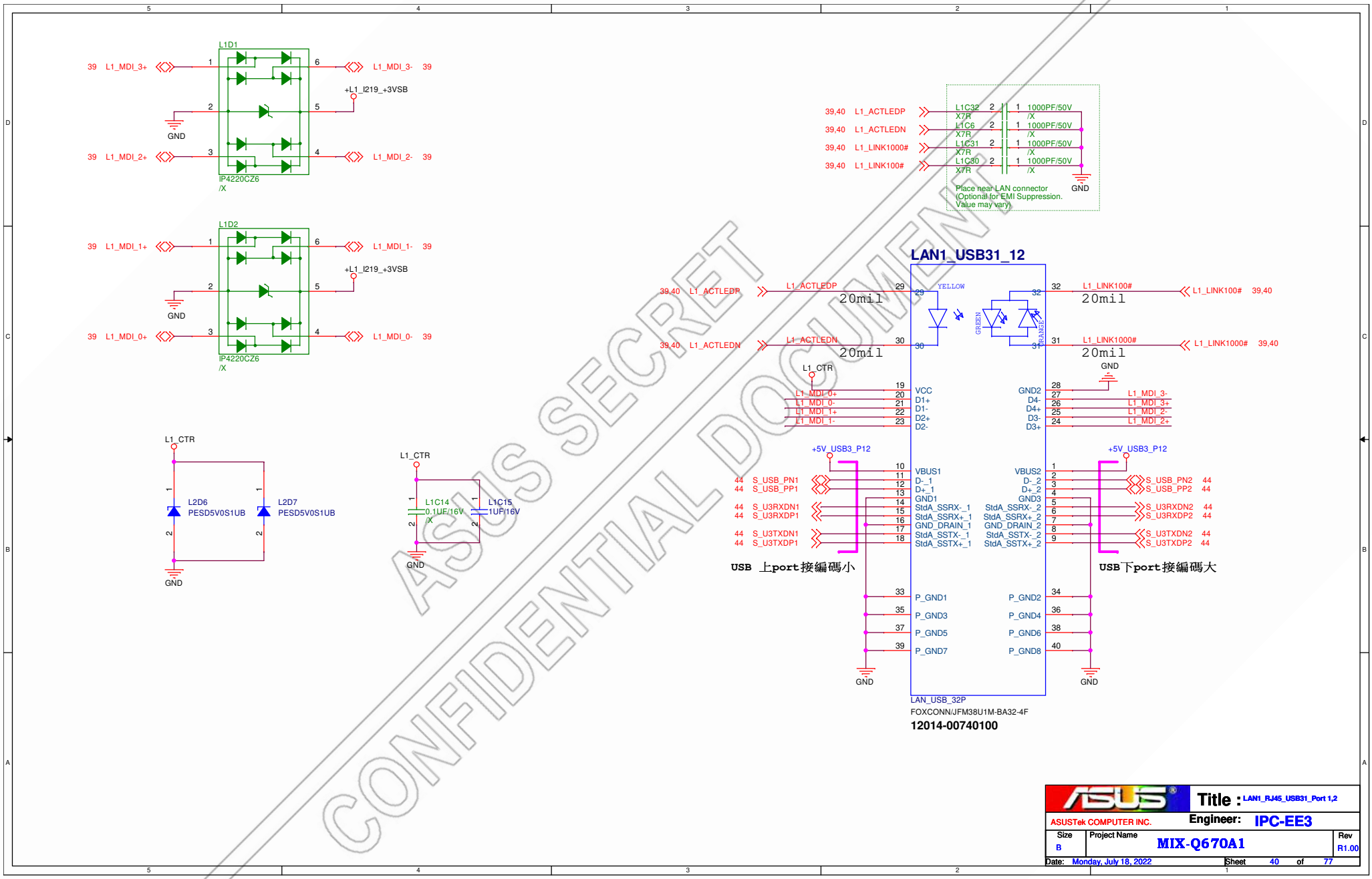
L1R16
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch

06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)

06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)

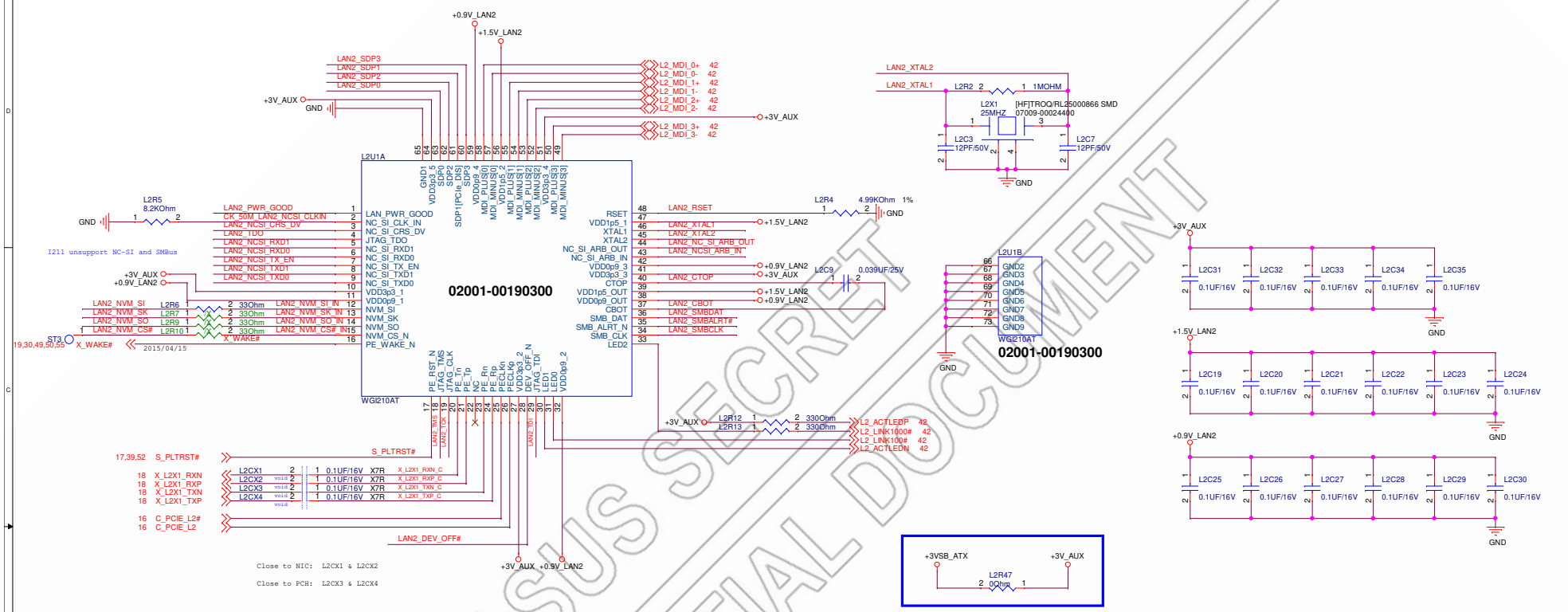
ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS
ASUSTek COMPUTER INC.
Title : L1_I219LM
Engineer: IPC-EE3
Size A3
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 39 of 77

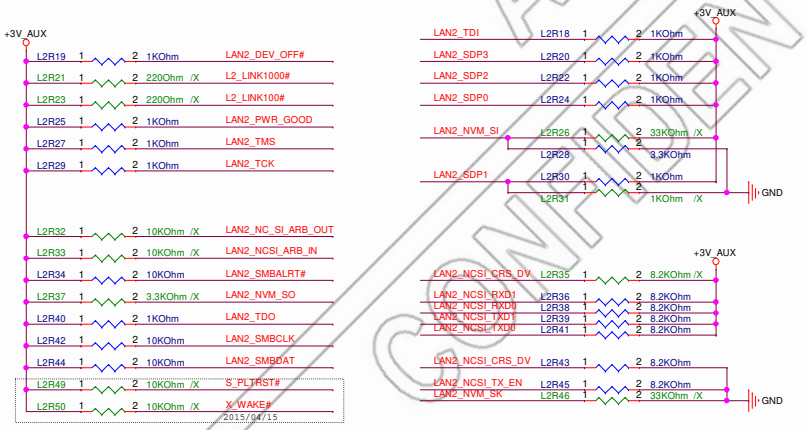


ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : LAN1_RJ45_USB31_Port 1,2		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size B	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 40 of 77		



Follow CRB A.B.



Strapping Options

```
DEV_OFF_N
 I210.28 (DEV_OFF_N)
   1: Exit Device off mode (Default)
   0: Enter Device off mode

AUX_PWR
 I210.28 (DEV_OFF_N)
 I210.60 (SDP3)
   11: Enable AUX power mode (Default)

Security_EN
 I210.12 (NVM_SI)
   1: Enable Flash security
   0: Disable Flash security (Default)

PCIE_DIS_N
 I210.61 (SDP1[PCIe_DIS])
   1: Enable PCIe function (Default)
   0: Disable PCIe function
```

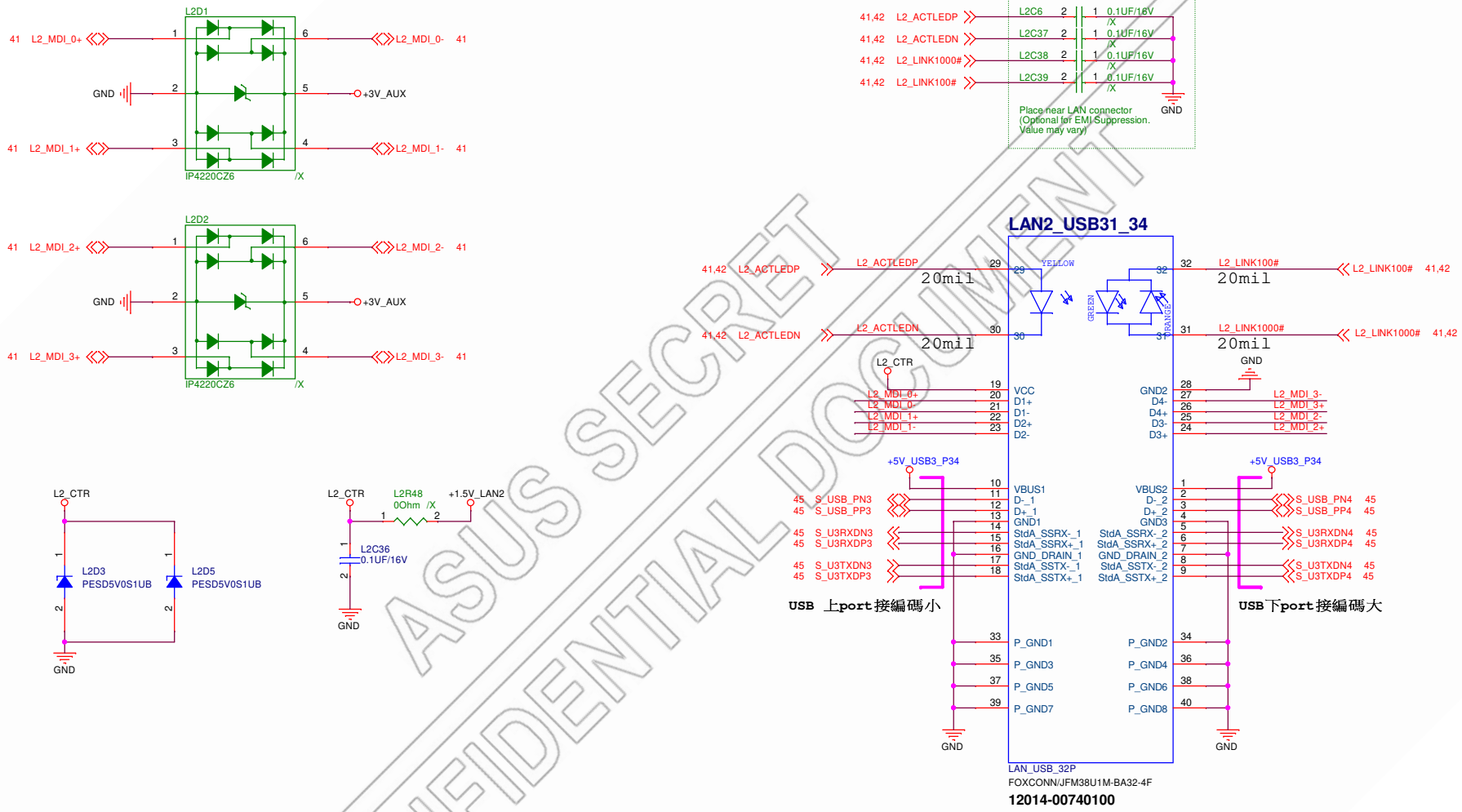
3.4 Voltage Regulator

To reduce Bill of Material (BOM) cost, the I211 supports generating the 1.5V and 0.9V power supplies from the 3.3V supply using an on-chip Switching Capacitor Voltage Regulator (SVR) control circuit, which requires only an external capacitor component.

Refer to Section 10.6.4 for more details.

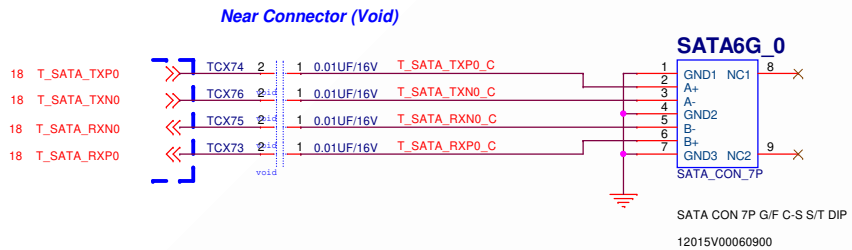
ASUS SECRET
CONFIDENTIAL DOCUMENT

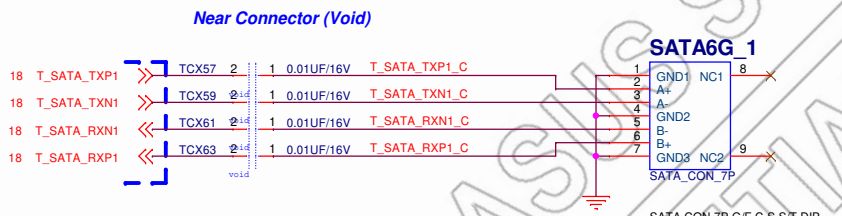
ASUS	Title : LAN2_I210-AT	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 41 of 77	



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : LAN2_RJ45_USB31_Port 3,4	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 42 of 77	





ASUS SECRET
CONFIDENTIAL DOCUMENT

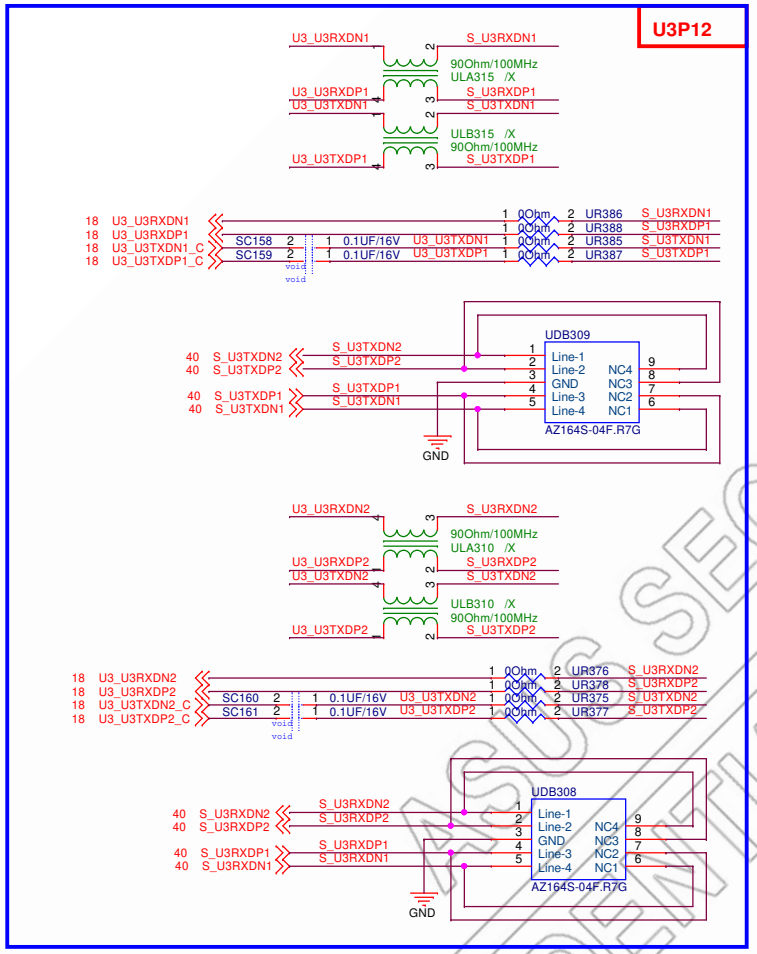
ASUSTek COMPUTER INC.

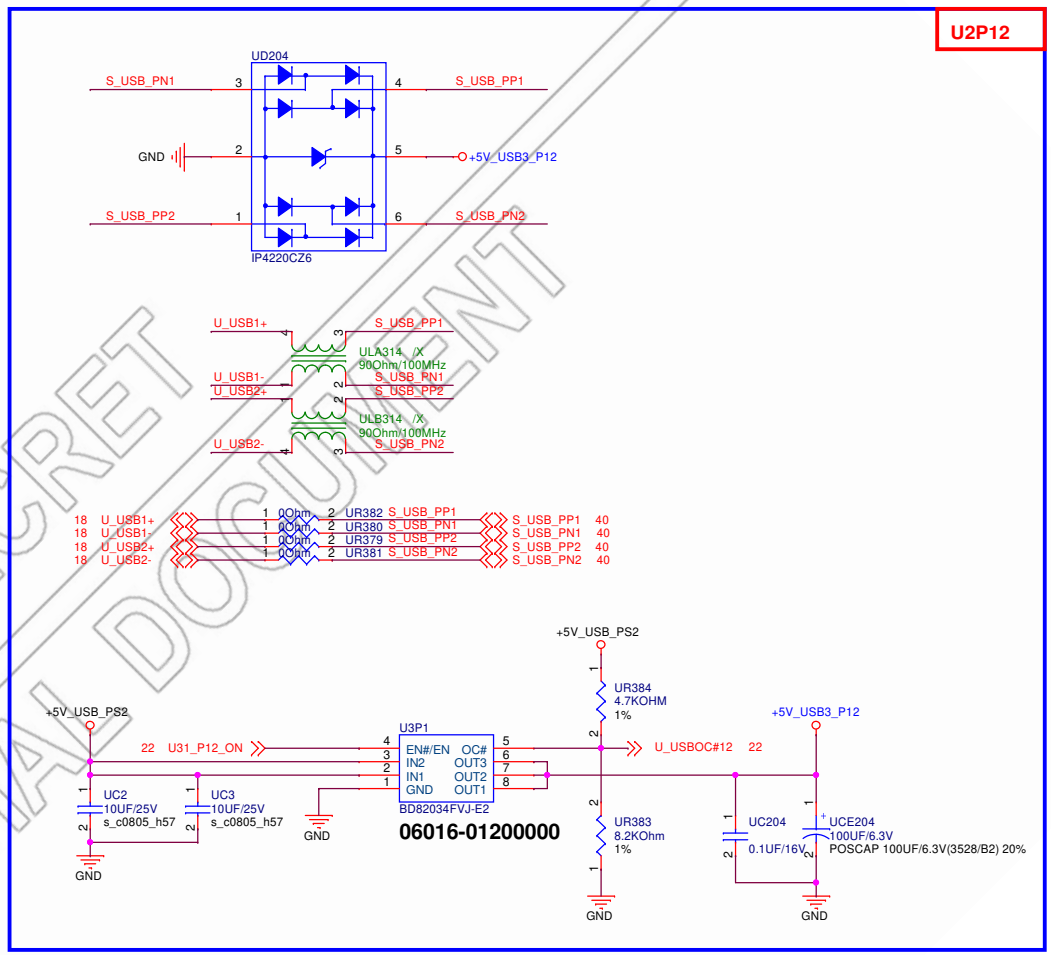
Title : SATA6G_12345(CHIPSET)

Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q670A1	R1.00

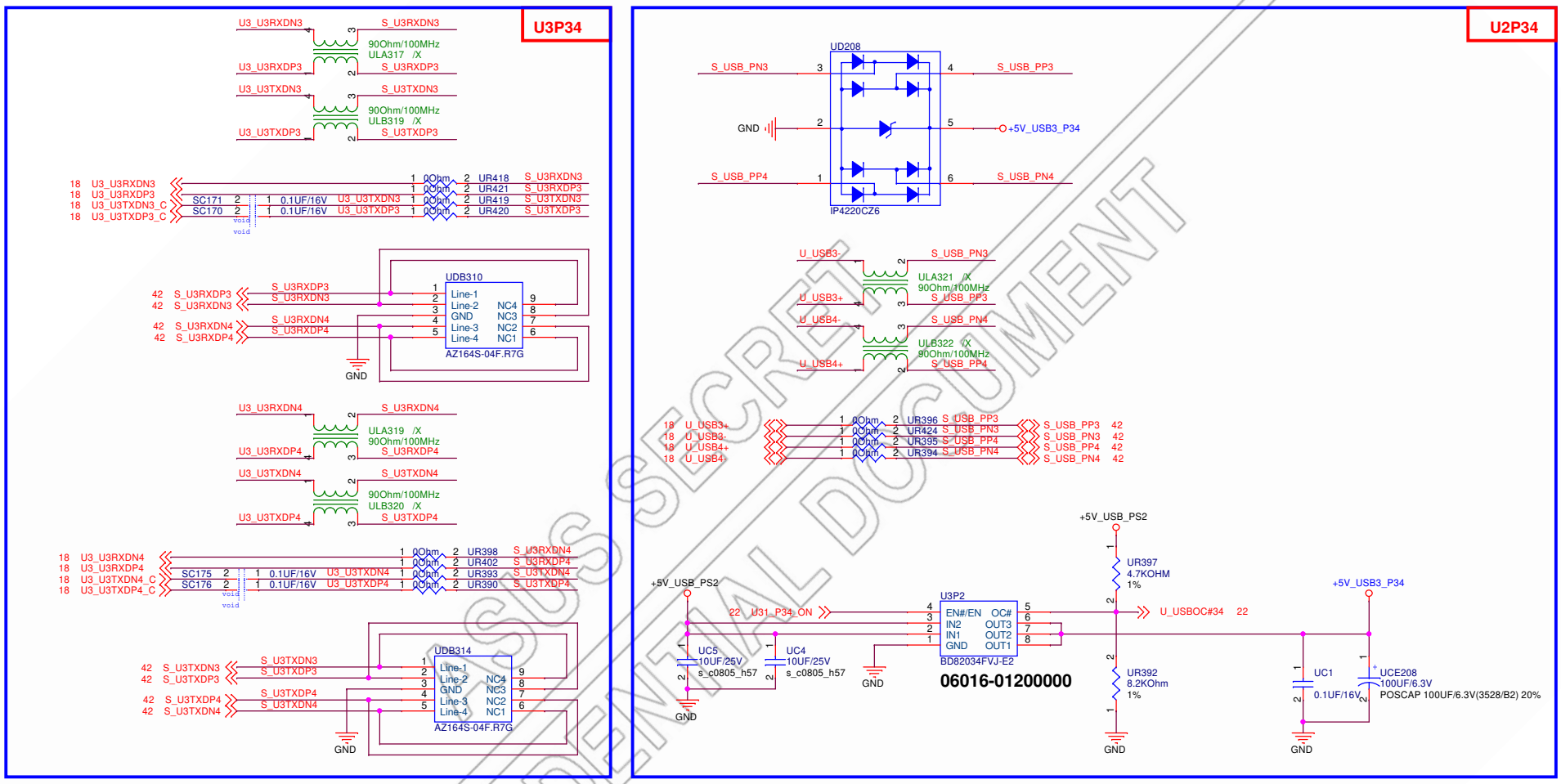
Date: Monday, July 18, 2022 Sheet 43 of 77





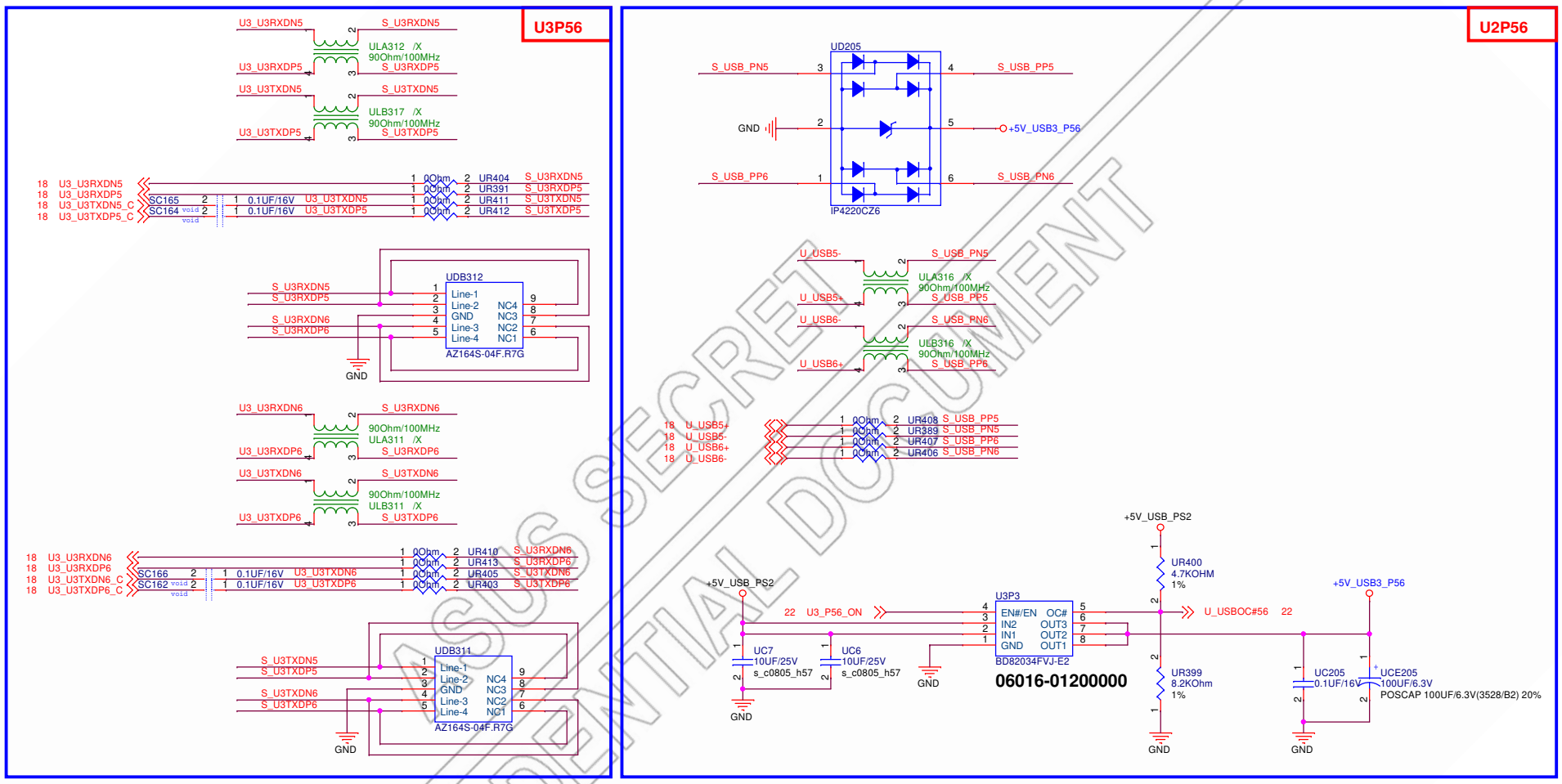
ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : USB31 Port 1,2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 44 of 77	



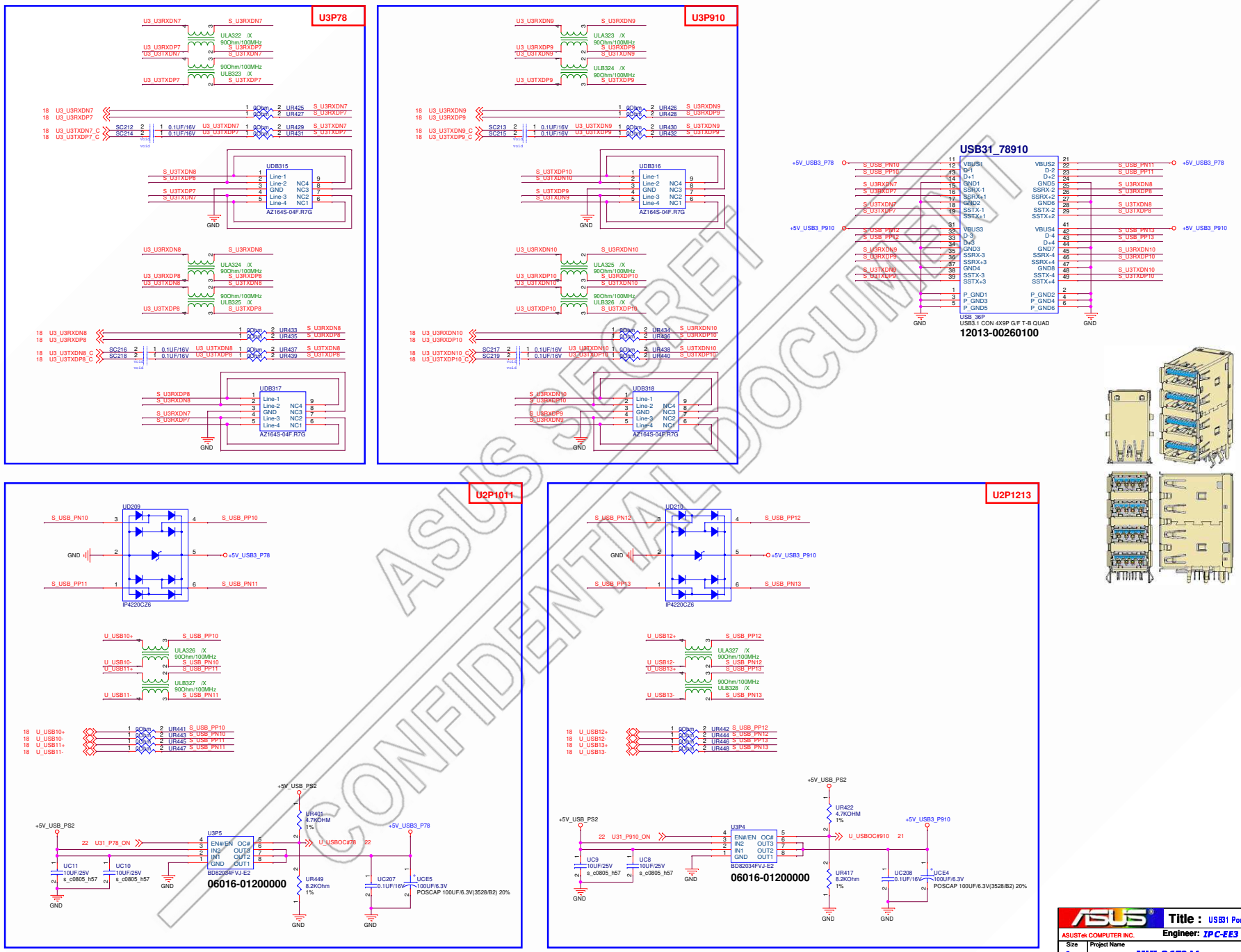
CONFIDENTIAL DOCUMENT
ASUS SECRET

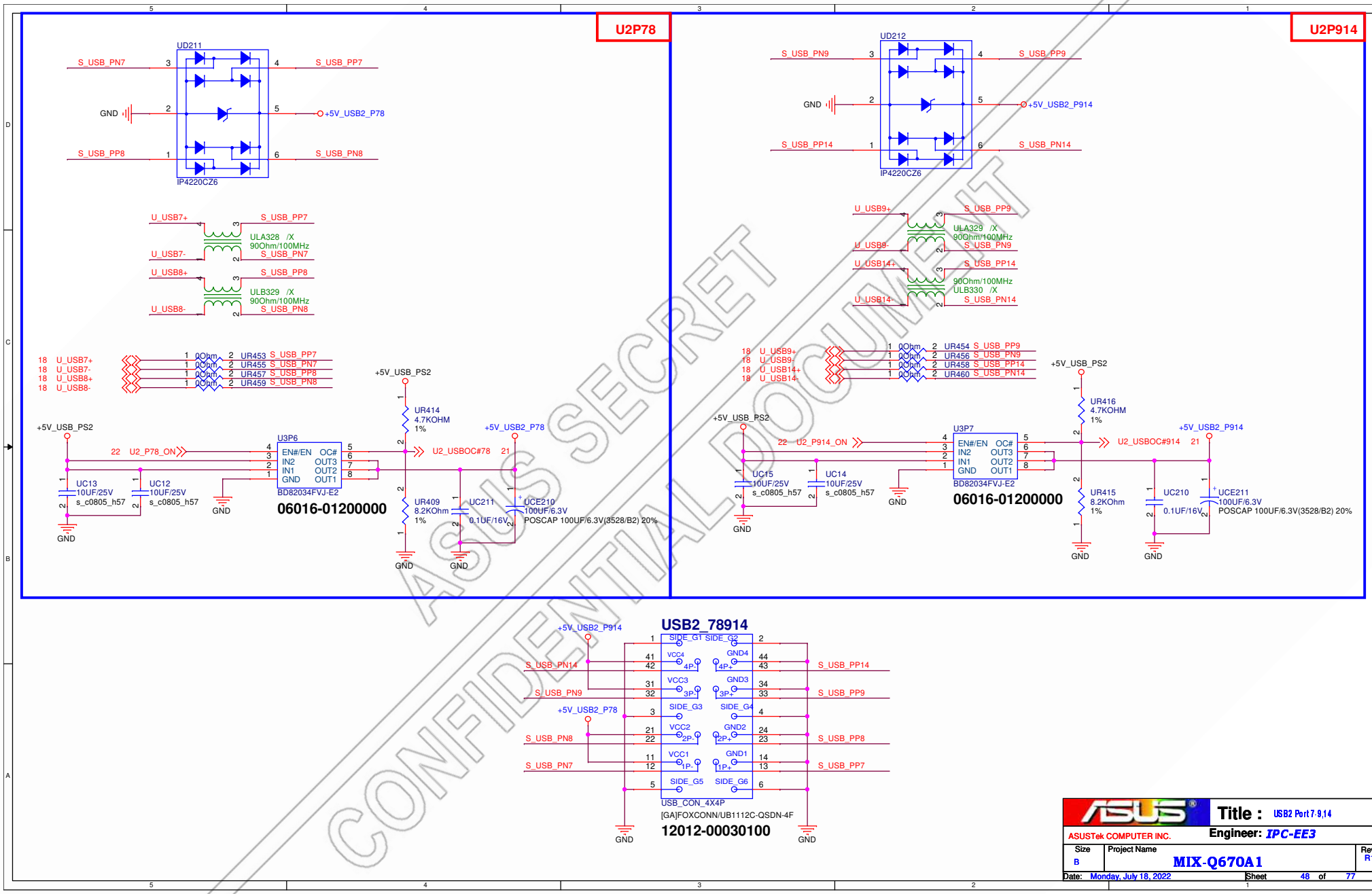
ASUS	Title : USB31 Port 3,4	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 45 of 77	



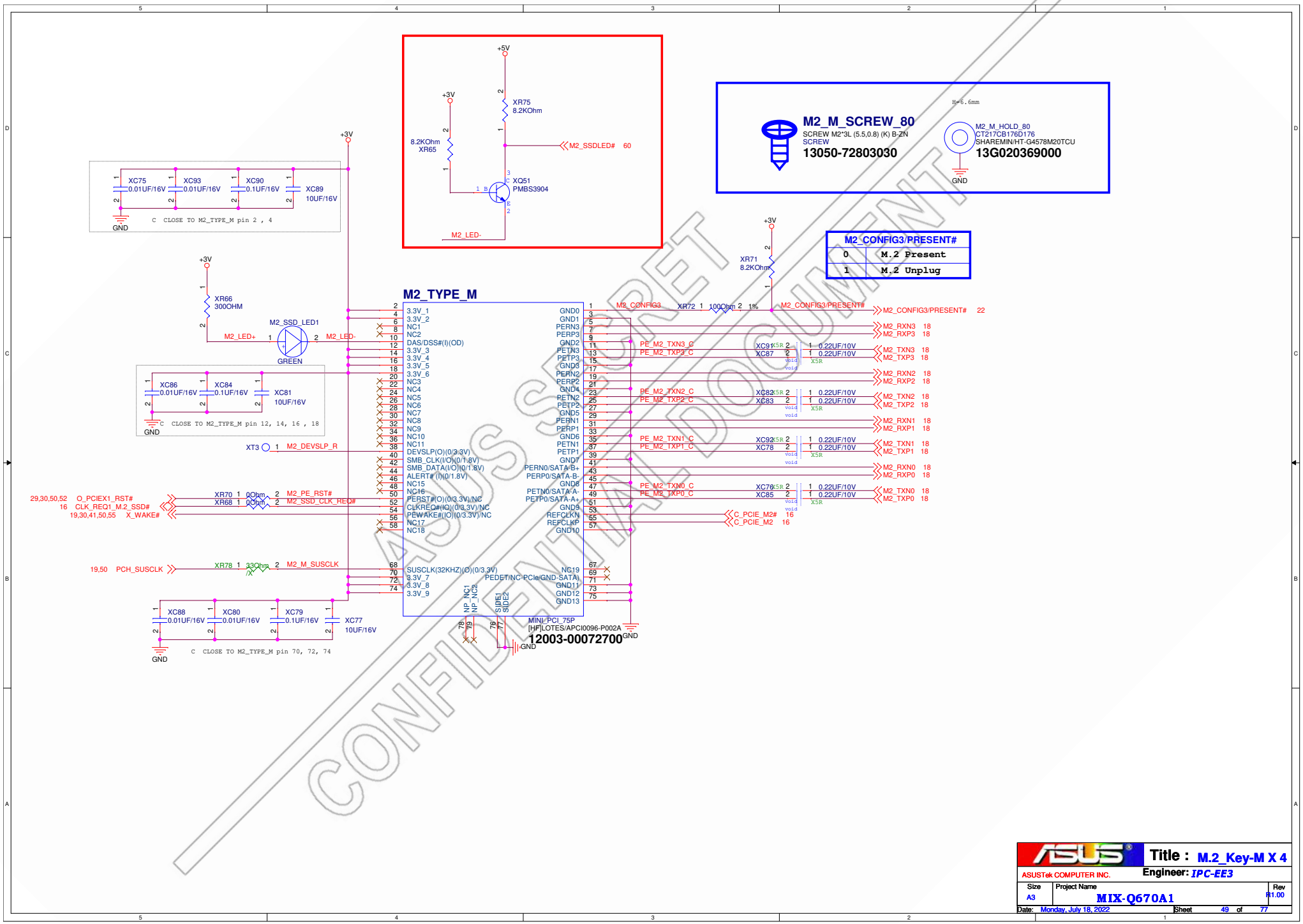
ASUSTek COMPUTER INC.	Title : USB31 Port 5,6	Engineer: IPC-EE3
Size: B	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 46 of 77	

ASUS SECRET
CONFIDENTIAL DOCUMENT


U3P78
U3P910
USB31_78910
12013-00260100
U2P1011
U2P1213
06016-01200000
06016-01200000
ASUS SECRET
CONFIDENTIAL DOCUMENT
Title : USB31 Port 7-10
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 47 of 77



ASUS SECRET
CONFIDENTIAL DOCUMENT


M2_TYPE_M
M2_M_SCREW_80
SCREW M2*3L (5.5,0.8) (K) B-ZN
SCREW
13050-72803030
M2_M_HOLD_80
CT217CB176D176
SHAREMIN/HT-G4578M20TCU
13G020369000
H=6.6mm
M2_CONFIG3/PRESENT#
0 M.2 Present
1 M.2 Unplug
M2_SSDLED# 60
M2_LED-
M2_LED+
M2_SSD_LED1
GREEN
XR75 8.2KOhm
XR65 8.2KOhm
XQ51 PMBS3904
XR66 300OHM
XR71 8.2KOhm
XR72 100Ohm 1%
XC75 0.01UF/16V
XC93 0.01UF/16V
XC90 0.1UF/16V
XC89 10UF/16V
C CLOSE TO M2_TYPE_M pin 2 , 4
XC86 0.01UF/16V
XC84 0.1UF/16V
XC81 10UF/16V
C CLOSE TO M2_TYPE_M pin 12, 14, 16 , 18
XC88 0.01UF/16V
XC80 0.01UF/16V
XC79 0.1UF/16V
XC77 10UF/16V
C CLOSE TO M2_TYPE_M pin 70, 72, 74
XT3 M2_DEVSLP_R
XR70 0Ohm M2_PE_RST#
XR68 0Ohm M2_SSD_CLK_REQ#
29,30,50,52 O_PCIEX1_RST#
16 CLK_REQ1_M.2_SSD#
19,30,41,50,55 X_WAKE#
19,50 PCH_SUSCLK
XR78 33Ohm M2_M_SUSCLK
M2_CONFIG3
M2_CONFIG3/PRESENT# 22
M2_RXN3 18
M2_RXP3 18
M2_TXN3 18
M2_TXP3 18
M2_RXN2 18
M2_RXP2 18
M2_TXN2 18
M2_TXP2 18
M2_RXN1 18
M2_RXP1 18
M2_TXN1 18
M2_TXP1 18
M2_RXN0 18
M2_RXP0 18
M2_TXN0 18
M2_TXP0 18
C_PCIE_M2# 16
C_PCIE_M2 16
PE_M2_TXN3_C
PE_M2_TXP3_C
PE_M2_TXN2_C
PE_M2_TXP2_C
PE_M2_TXN1_C
PE_M2_TXP1_C
PE_M2_TXN0_C
PE_M2_TXP0_C
XC91 0.22UF/10V
XC87 0.22UF/10V
XC82 0.22UF/10V
XC83 0.22UF/10V
XC92 0.22UF/10V
XC78 0.22UF/10V
XC76 0.22UF/10V
XC85 0.22UF/10V
MINI-PCI_75P
[HF]LOTES/APCI0096-P002A
12003-00072700
ASUS SECRET
CONFIDENTIAL DOCUMENT
Title : M.2_Key-M X 4
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 49 of 77

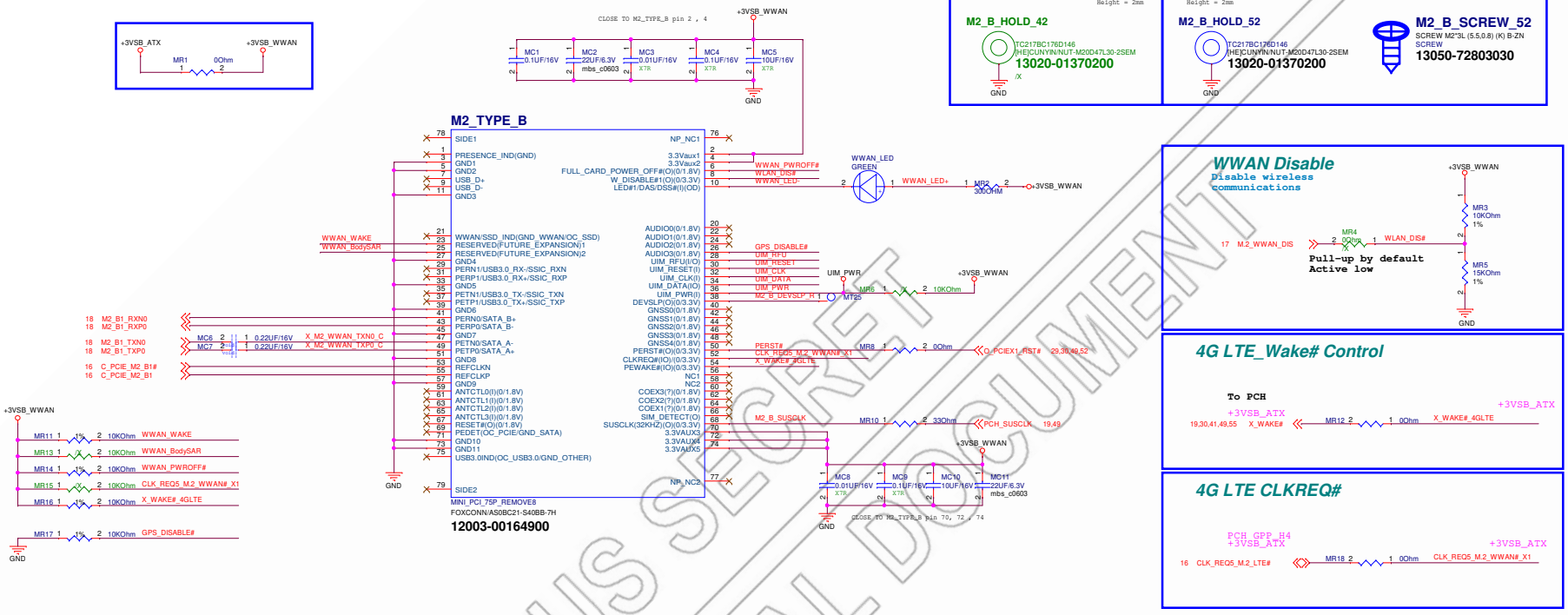


Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
1	0	1	1	RFU	N/A
1	1	1	1	No Module Present	N/A

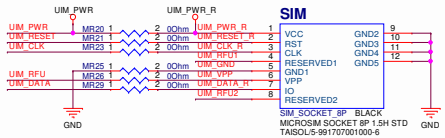
[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
[2] Applicable to WWAN only

Table 26. GPIO pin Function Assignment per Port Configuration

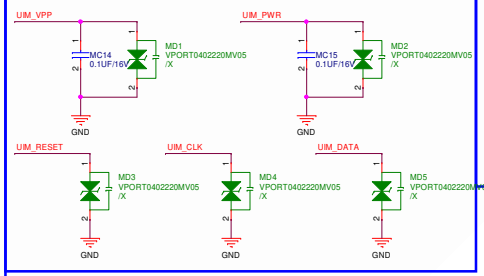
	Pin	Port Config_0[1]	Port Config_1[2]	Port Config_2[3]	Port Config_3[4]
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2	IPC_1
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3
GPIO_9 [5,6]	10	LED_1#	LED_1#	LED_1#	IPC_7
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA

[1] GNSS+Audio version 1
[2] GNSS+Audio version 2
[3] 2nd UIM/SIM Support
[4] HSIC Support
[5] Platform Providers may choose to implement IPC sideband instead of the LED_1# to optimize their design
[6] Some host platforms (ex. tablets) may not require support for SSD. In such configurations, Host Platform Providers may choose to implement IPC_7 on GPIO_9 instead of DAS/DSS

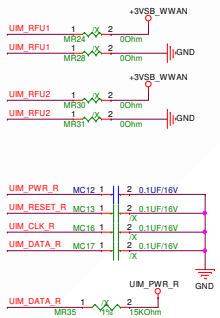
Micro-SIM Card



Micro-SIM Card - ESD Protection



Reserved Pin for Signal Quality



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTeK COMPUTER INC.

Title : M.2_Key-B_LTE

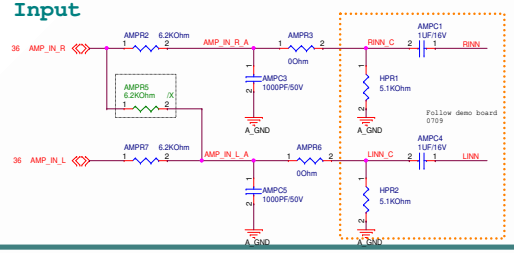
Engineer: IPC-EE3

Size	Project Name	Rev
C	MIX-Q670A1	R1.00

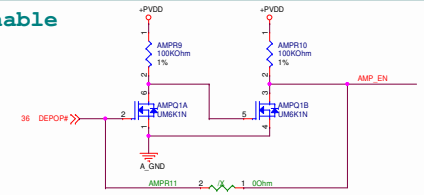
Date: Monday, July 18, 2022 Sheet 50 of 77

AMP - EUA2075JIR1 (Only Speaker)

Analog Input

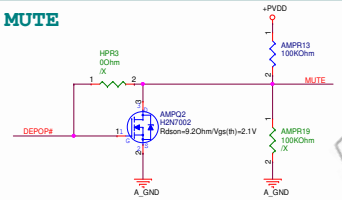


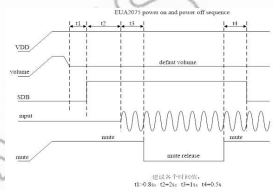
Amp. Enable



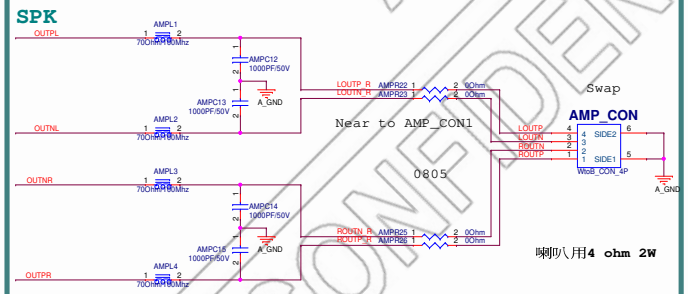
EUA2075 SD PIN 為 High有聲音輸出 , Mute pin 為 Low有聲音輸出

MUTE

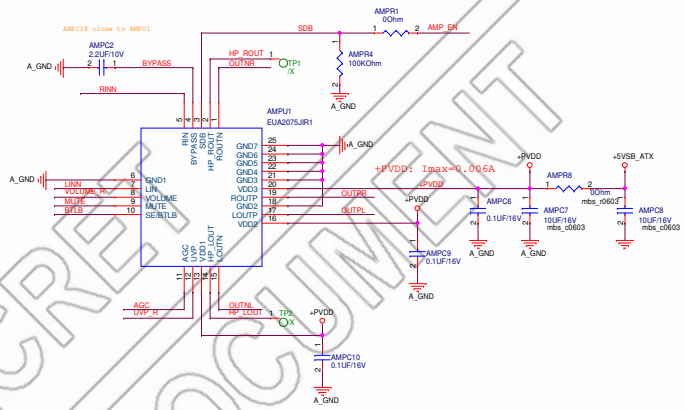




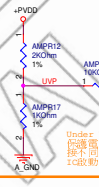
SPK



AMPC30, AMPC43, AMPC44, AMPC47, use 1uF is good to EUA2113



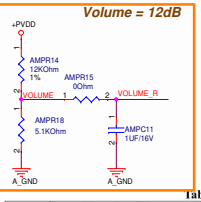
UVP



Under Voltage Protection
低壓電壓設定PIN腳不同的分壓電阻,
IC啟動電壓不同

The thresholds can be determined as below:
With the condition: R3 >> R1//R2
V UVP =[1.2-(5.7μA×R3)]×(R1+R2)/R2
Hysteresis=(4.6μA×R3)×(R1+R2)/R2

Volume = 12dB



AGC

Speaker
4 ohm 2W

0.45VDD~0.27VDD: 1.93W

Table 2. AGC Function

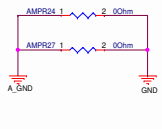
AGC Voltage	Output Power
VDD ~ 0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$8\times(VDD\times0.5-VAGC)^2\times0.95/R_L$
0.27VDD ~ GND	P_{OMAX}=2.45W @ 4Ω P_{OMAX}=1.225W @ 8Ω

Auto Gain Control
最大功率的限制對喇叭進行保護
若輸出超過最大功率值
AGC會 自動降低到設定值

Table 1. DC Volume Control

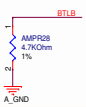
Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)
1	0.0 - 3.4	2.4 - 0.0	20.0
2	3.4 - 4.8	3.8 - 2.4	19.6
3	4.8 - 6.2	5.2 - 3.8	19.2
4	6.2 - 7.6	6.6 - 5.2	18.8
5	7.6 - 9.0	8.0 - 6.6	18.4
6	9.0 - 10.4	9.4 - 8.0	18.0
7	10.4 - 11.8	10.8 - 9.4	17.6
8	11.8 - 13.2	12.2 - 10.8	17.2
9	13.2 - 14.6	13.6 - 12.2	16.8
10	14.6 - 16.0	15.0 - 13.6	16.4
11	16.0 - 17.4	16.4 - 15.0	16.0
12	17.4 - 18.8	17.8 - 16.4	15.6
13	18.8 - 20.2	19.2 - 17.8	15.2
14	20.2 - 21.6	20.6 - 19.2	14.8
15	21.6 - 23.0	22.0 - 20.6	14.4
16	23.0 - 24.4	23.4 - 22.0	14.0
17	24.4 - 25.8	24.8 - 23.4	13.6
18	25.8 - 27.2	26.2 - 24.8	13.2
19	27.2 - 28.6	27.6 - 26.2	12.8
20	[illegible]	[illegible]	[illegible]
21	30.0 - 31.4	30.4 - 29.0	12.0

GND Plane - All A_GND



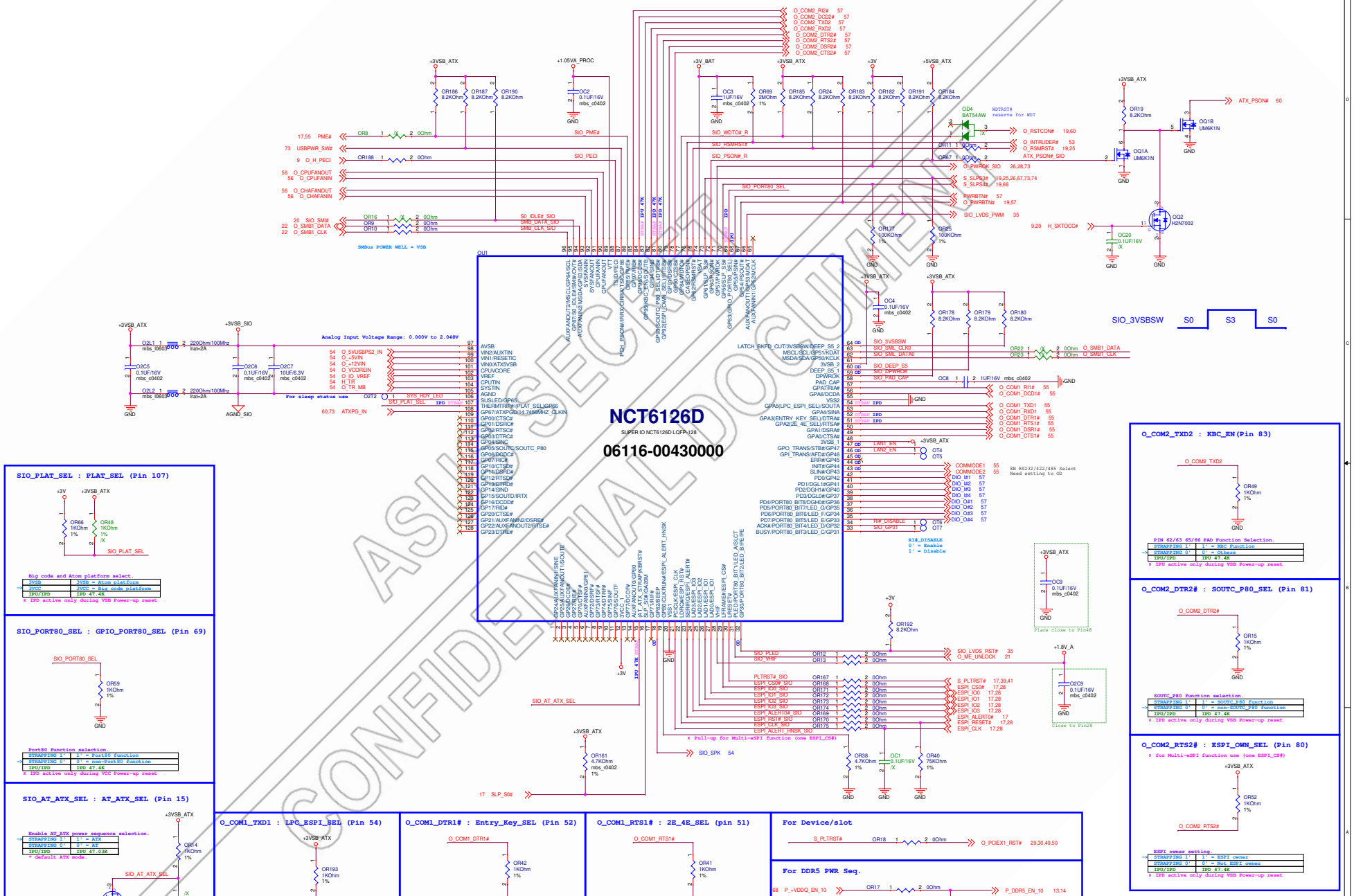
BTLB Only

喇叭與耳機功能切換
SE MODEL :耳機模式 (Hi)
BTL MODEL : 喇叭模式(Low)



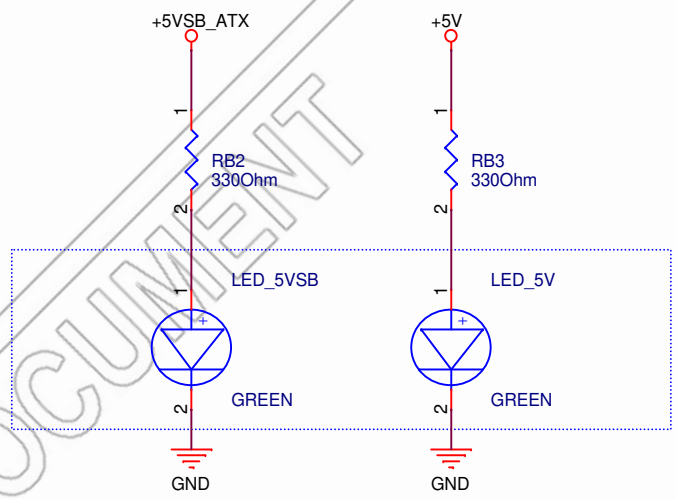
ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTeK COMPUTER INC.
Title : AUDIO_EUA2075JIR1
Engineer: IPC-EE3
Size A2
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 51 of 77

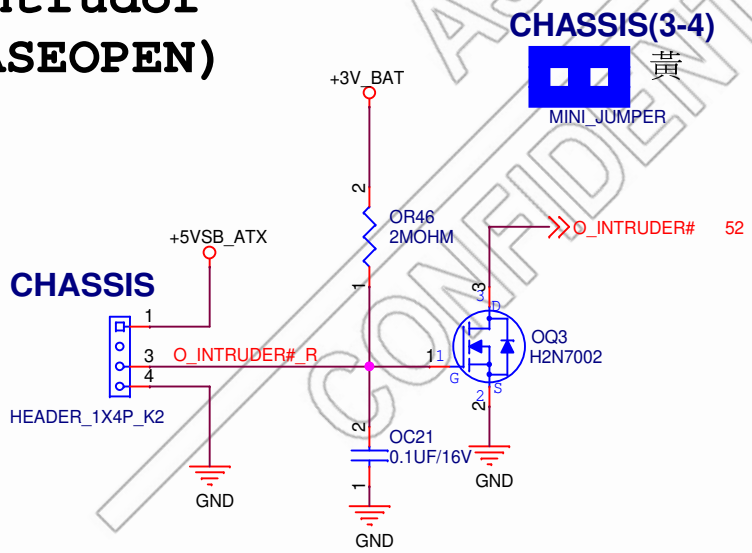


ASUS SECRET DOCUMENT
CONFIDENTIAL DOCUMENT

POWER_PWR



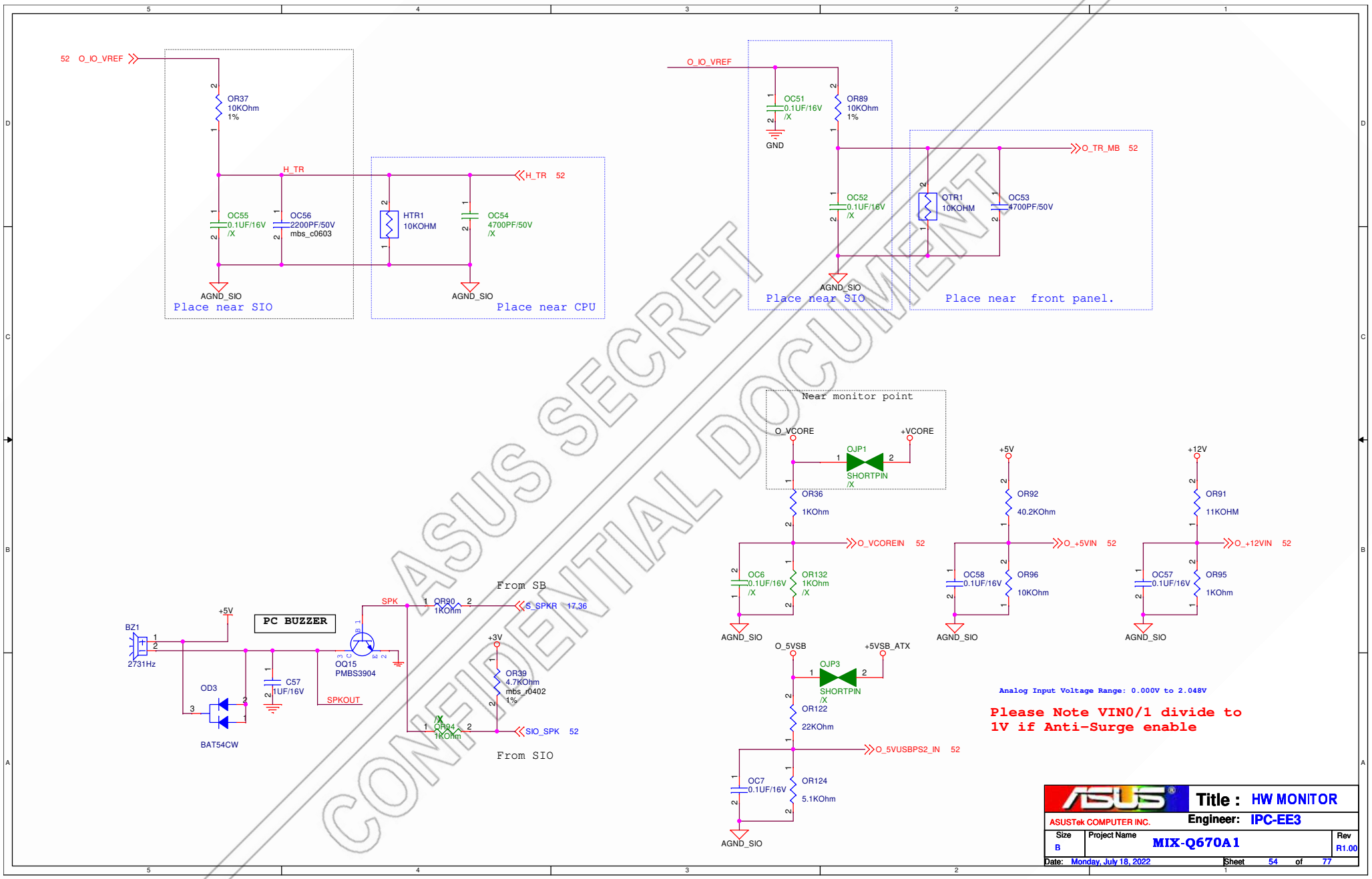
Intrudor (CASEOPEN)



To SIO

ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : Intrudor(CASEOPEN)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 53 of 77		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OR37
10KOhm
1%
H_TR
OC55
0.1UF/16V
/X
OC56
2200PF/50V
mbs_c0603
HTR1
10KOHM
OC54
4700PF/50V
/X
H_TR 52
AGND_SIO
Place near SIO
Place near CPU
O_IO_VREF
OC51
0.1UF/16V
/X
GND
OR89
10KOhm
1%
OC52
0.1UF/16V
/X
QTR1
10KOHM
OC53
4700PF/50V
O_TR_MB 52
Place near SIO
Place near front panel.
Near monitor point
O_VCORE
+VCORE
OJP1
SHORTPIN
/X
OR36
1KOhm
O_VCOREIN 52
OC6
0.1UF/16V
/X
OR132
1KOhm
/X
+5V
OR92
40.2KOhm
O_+5VIN 52
OC58
0.1UF/16V
OR96
10KOhm
+12V
OR91
11KOHM
O_+12VIN 52
OC57
0.1UF/16V
OR95
1KOhm
O_5VSB
+5VSB_ATX
OJP3
SHORTPIN
/X
OR122
22KOhm
O_5VUSBPS2_IN 52
OC7
0.1UF/16V
OR124
5.1KOhm
Analog Input Voltage Range: 0.000V to 2.048V
Please Note VIN0/1 divide to
1V if Anti-Surge enable
BZ1
2731Hz
+5V
PC BUZZER
OD3
BAT54CW
C57
1UF/16V
SPKOUT
SPK
OQ15
PMBS3904
OR90
1KOhm
From SB
S_SPKR 17,36
+3V
OR39
4.7KOhm
mbs_r0402
1%
/X
OR94
1KOhm
SIO_SPK 52
From SIO
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUS
Title : HW MONITOR
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size
B
Project Name
MIX-Q670A1
Rev
R1.00
Date: Monday, July 18, 2022
Sheet 54 of 77

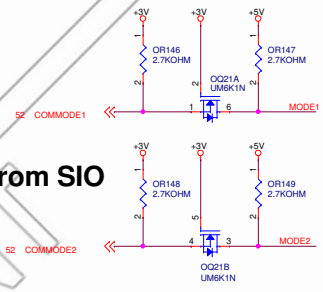
RS422/RS485 Terminator

COM_J1 all off -->RS232
COM_J1 all on -->RS485/RS422 with terminator

Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ.
As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.

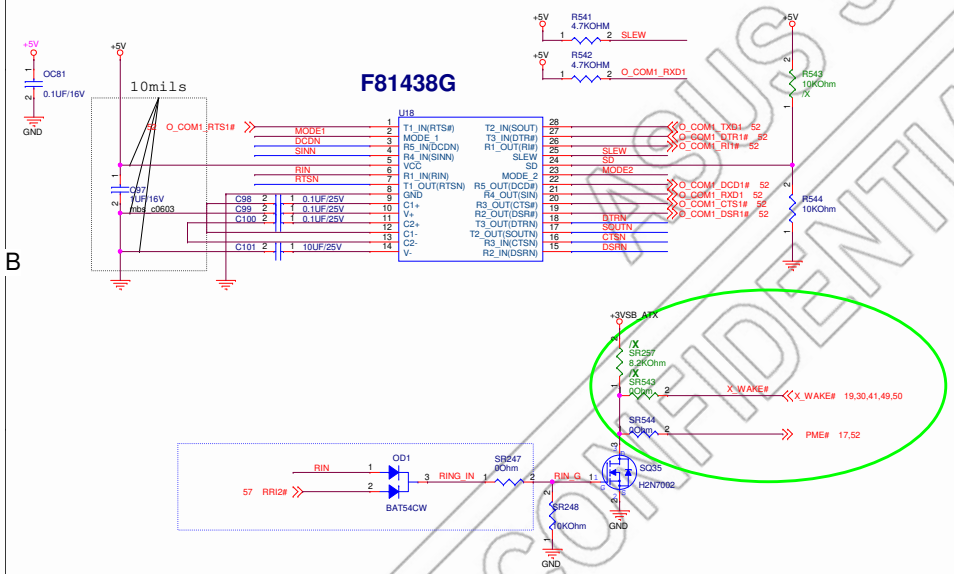


(VDD = +5.0V ± 5%)

Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01.		2	30	mA
Supply Current (RS-485)	No Load, MODE = 10, 11.		2		mA
Supply Current (RS-422)	MODE = 00.		2		mA
Operating Temperature *	Symbol: T	-40		85	◦ C

(VDD = +5.0V ± 5%)

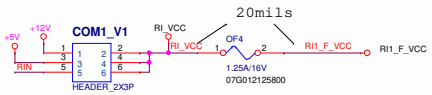
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V_{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	μA	
Driver Input Pull High Current	I_{IT}			±15	μA	

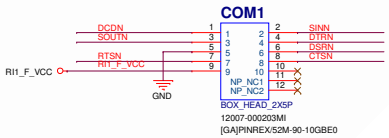


COM1_V1(5-6)	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

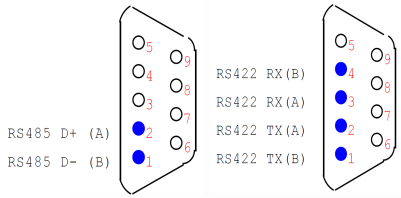
COM1_V1(5-6)

MINI_JUMPER

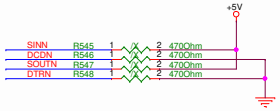




Close to COM port connector



Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps



Note:Reserved for FAIL-SAFE

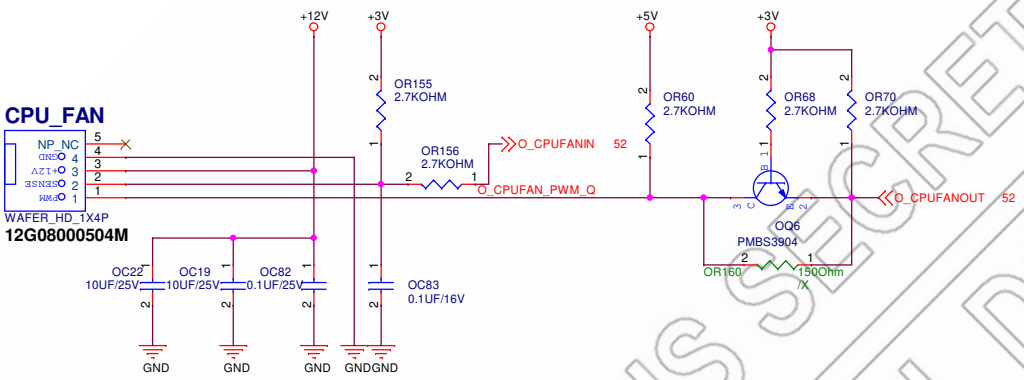
ASUS SECRET
CONFIDENTIAL

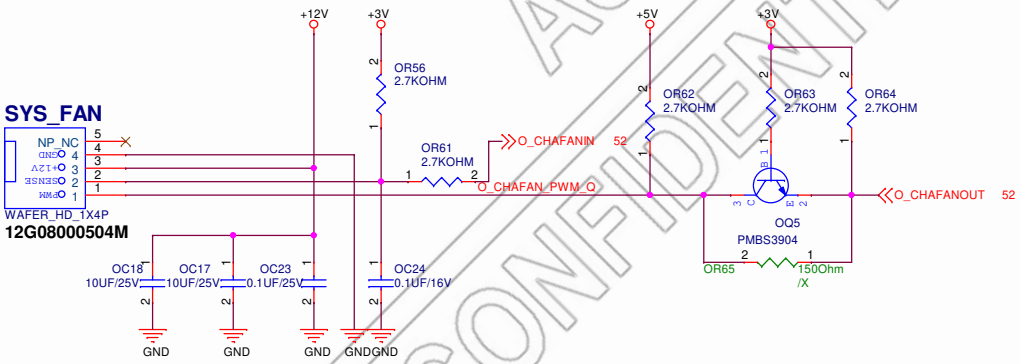
ASUSTek COMPUTER INC.	Title : COM1_RS232/422/485	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 55 of 77	

FAN CONTROL

PWM FAN CONTROL(New)

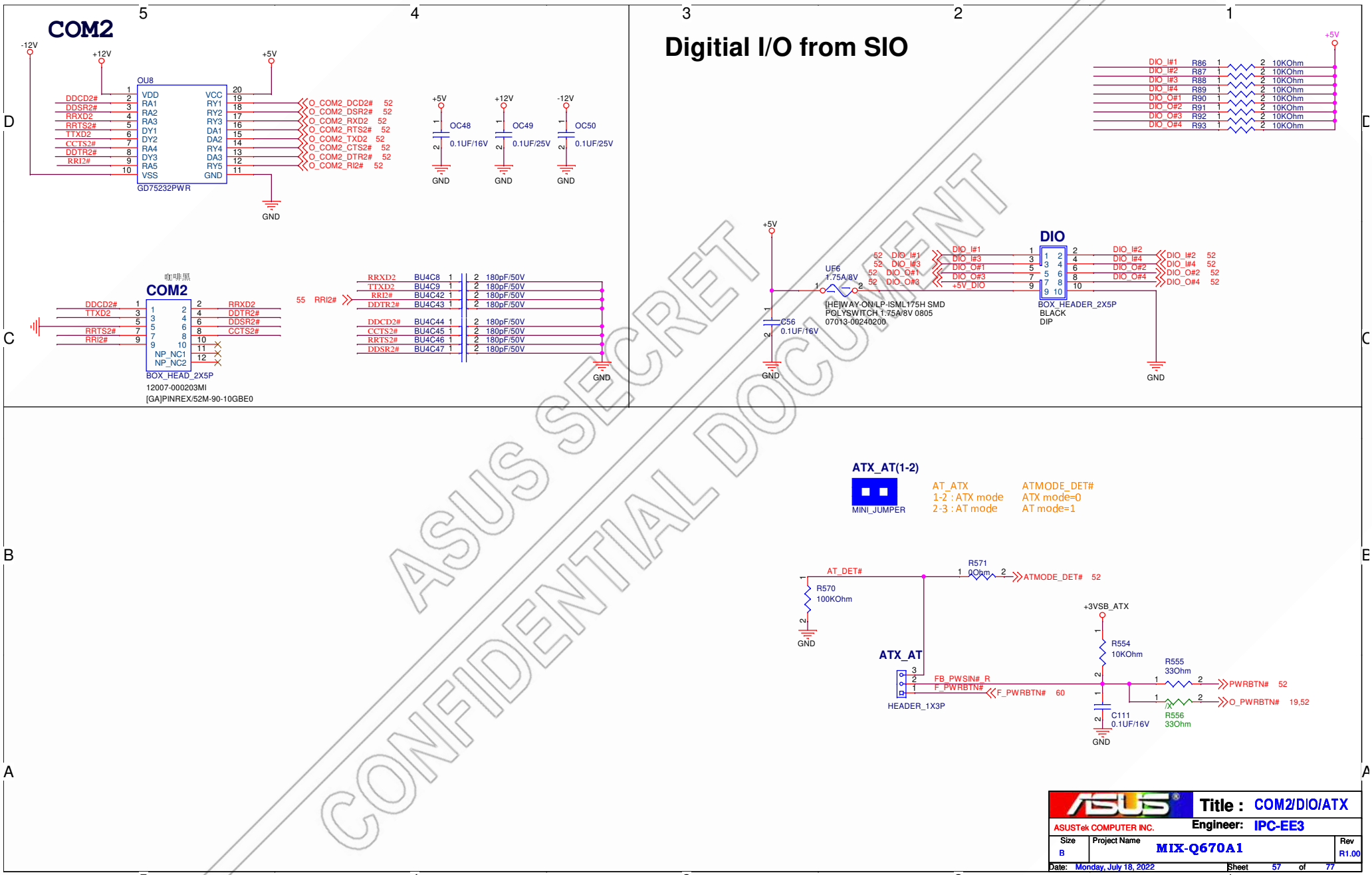
Pin Number	Signal
1	Control
2	Sense
3	+12V
4	GND





ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTek COMPUTER INC.	Title : CPUFAN_SYSFAN1	Engineer: IPC-EE3
Size B	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 56 of 77	


COM2
OU8
GD75232PWR
DDCD2#
DDSR2#
RRXD2
RRTS2#
TTXD2
CCTS2#
DDTR2#
RRI2#
O_COM2_DCD2# 52
O_COM2_DSR2# 52
O_COM2_RXD2 52
O_COM2_RTS2# 52
O_COM2_TXD2 52
O_COM2_CTS2# 52
O_COM2_DTR2# 52
O_COM2_RI2# 52
OC48 0.1UF/16V
OC49 0.1UF/25V
OC50 0.1UF/25V
GND
Digitial I/O from SIO
DIO_I#1 R86 10KOhm
DIO_I#2 R87 10KOhm
DIO_I#3 R88 10KOhm
DIO_I#4 R89 10KOhm
DIO_O#1 R90 10KOhm
DIO_O#2 R91 10KOhm
DIO_O#3 R92 10KOhm
DIO_O#4 R93 10KOhm
UF6 1.75A/8V
[HE]WAY-ON/LP-ISML175H SMD
POLYSWITCH 1.75A/8V 0805
07013-00240200
C56 0.1UF/16V
DIO
BOX_HEADER_2X5P
BLACK
DIP
+5V_DIO
COM2
BOX_HEAD_2X5P
12007-000203MI
[GA]PINREX/52M-90-10GBE0
NP_NC1
NP_NC2
RRI2# 55
BU4C8 180pF/50V
BU4C9 180pF/50V
BU4C42 180pF/50V
BU4C43 180pF/50V
BU4C44 180pF/50V
BU4C45 180pF/50V
BU4C46 180pF/50V
BU4C47 180pF/50V
ATX_AT(1-2)
MINI_JUMPER
AT_ATX
1-2 : ATX mode
2-3 : AT mode
ATMODE_DET#
ATX mode=0
AT mode=1
AT_DET#
R570 100KOhm
R571 0Ohm
ATMODE_DET# 52
+3VSB_ATX
R554 10KOhm
ATX_AT
HEADER_1X3P
FB_PWSIN#_R
F_PWRBTN#
F_PWRBTN# 60
R555 33Ohm
PWRBTN# 52
R556 33Ohm
O_PWRBTN# 19,52
C111 0.1UF/16V
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUSTek COMPUTER INC.
Title : COM2/DIO/ATX
Engineer: IPC-EE3
Size B
Project Name MIX-Q670A1
Rev R1.00
Date: Monday, July 18, 2022
Sheet 57 of 77

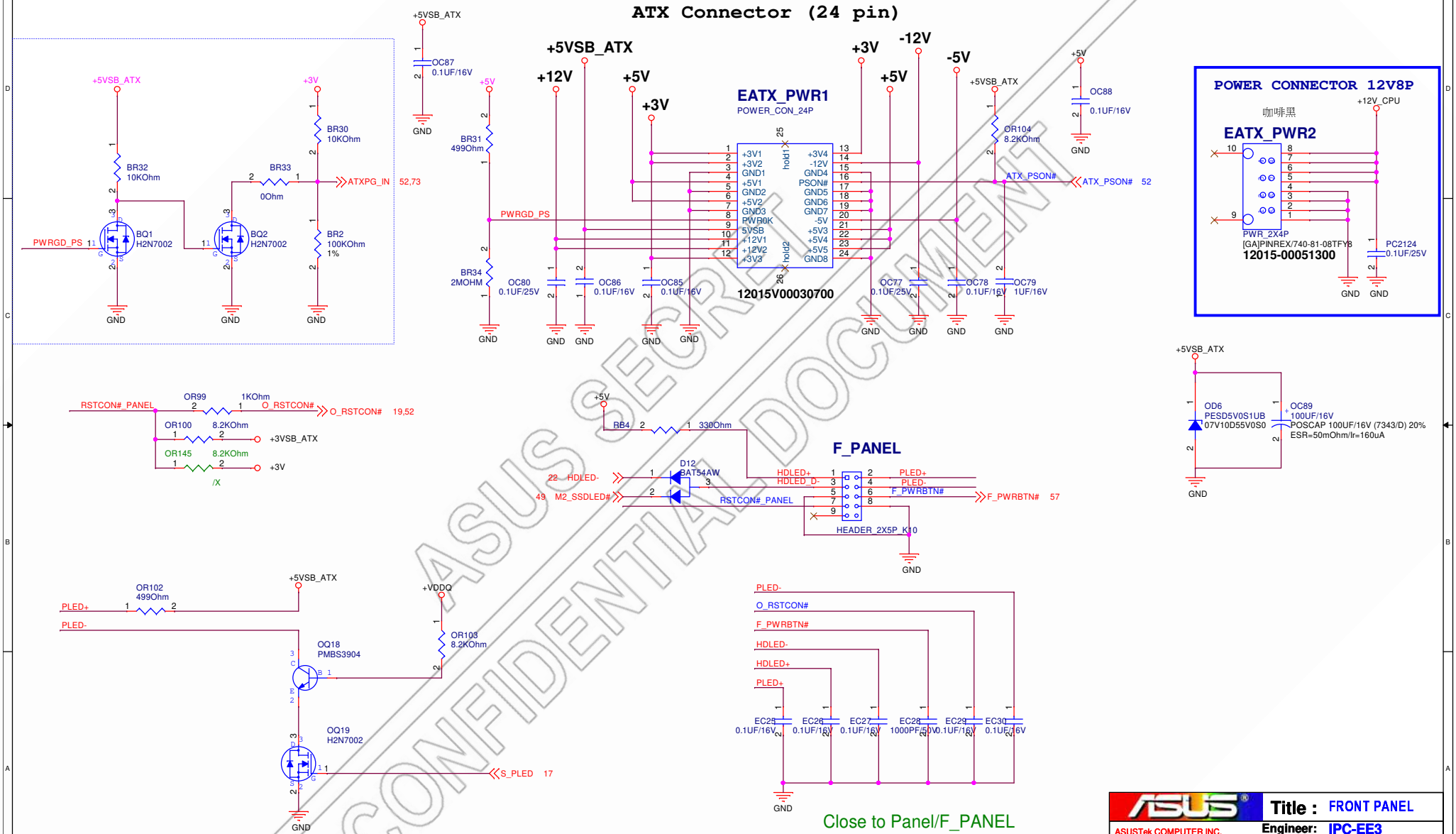
ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : F81216HD-I		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size B	Project Name MIX-Q670A1		Rev R1.00
Date: Monday, July 18, 2022	Sheet 58 of 77		

ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : XXXXX	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 59 of 77	

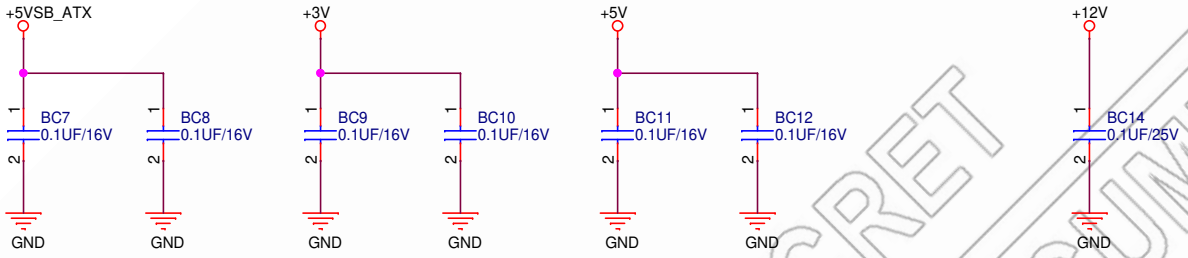
ATX Connector (24 pin)



ASUS SECRET CONFIDENTIAL DOCUMENT

ASUS	Title : FRONT PANEL	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 60 of 77	

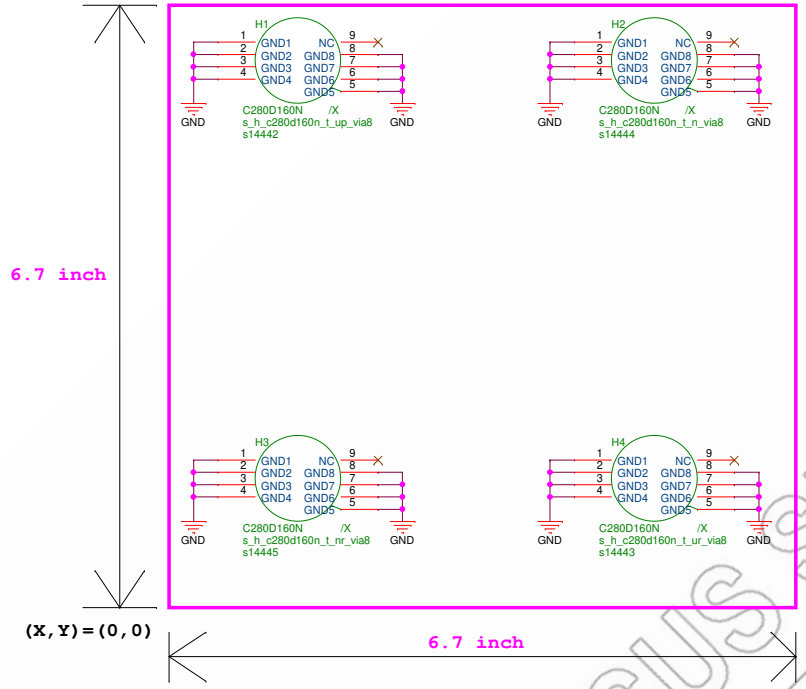
Bypass/EMI Capacitor



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : EMI Cap	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A4	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 61 of 77	

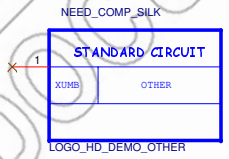
mini-ITX Screw Hole

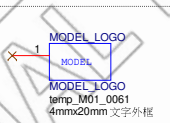


ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : Screw Hole	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q670A1	Rev R1.00
Date: Monday, July 18, 2022	Sheet 62 of 77	

Selling Point





PCB

MIX-Q670A1

08001-19520X00

MIX-Q670A1 R1.00//GECS 6.7*6.7,10L(1)1.6,1080

MIX-Q670A1 R1.00 PCB-08 :

R1.00 PCB_GECS : 08001-19520000

R1.00 PCB_VICTORY : 08001-19520100

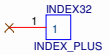
R1.00 PCB_TRUSTECH : 08001-19520200

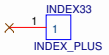
Fiducial Mask (光學點)

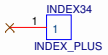
光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

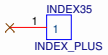
大顆十字光學點

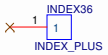
小顆十字光學點







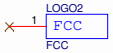


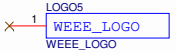


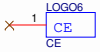
2012/09/11

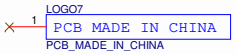
Logo

common Logo for all projects









ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title :	Selling Point_Logo
ASUSTek COMPUTER INC.	Engineer:	IPC-EE3
Size: A3	Project Name: MIX-Q670A1	Rev: R1.00
Date: Monday, July 18, 2022	Sheet 63 of 77	