UP-APL01

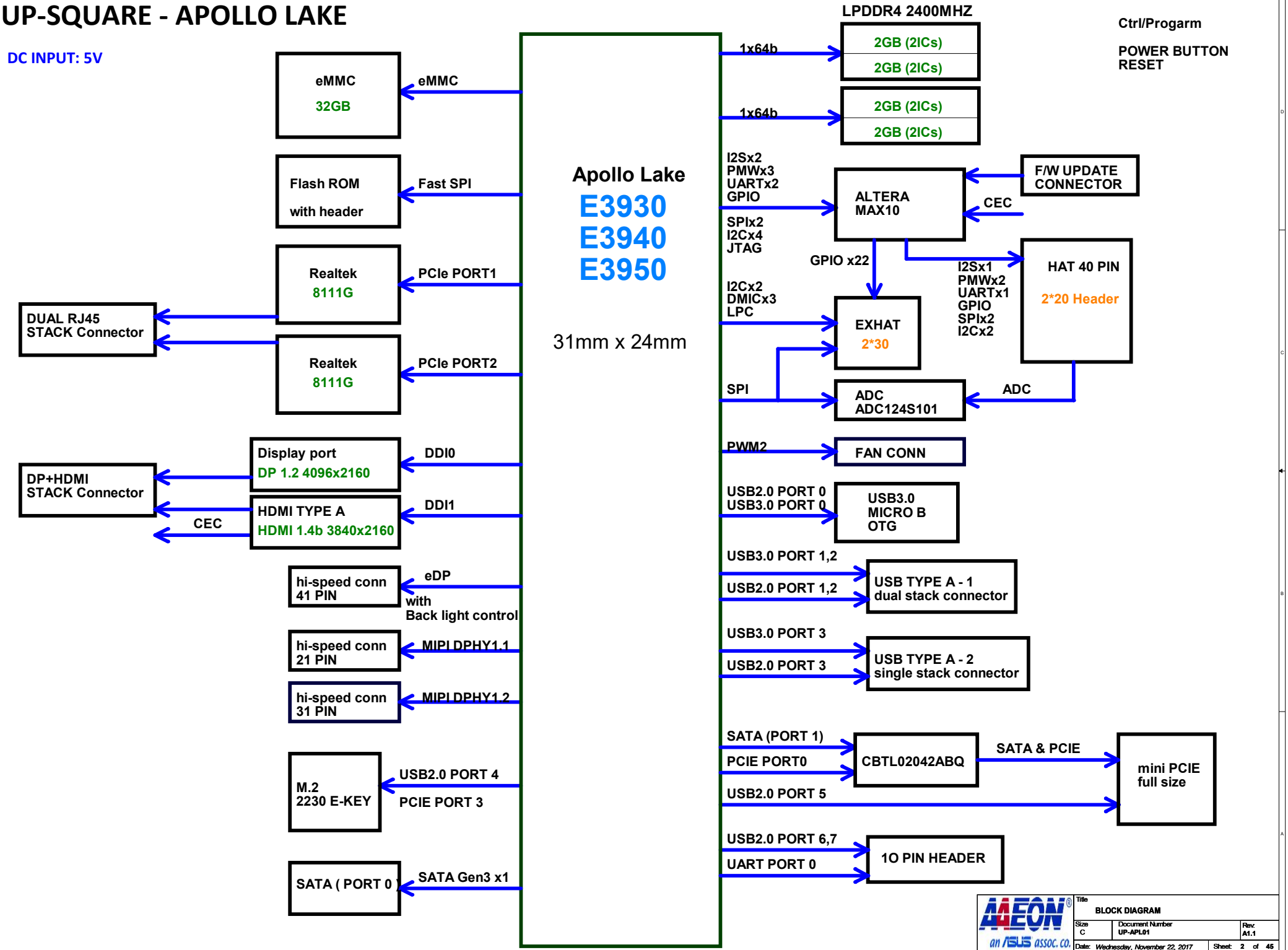
Project Code: D160807

AAEON® an ASUS assoc. co.

Title: **Index**		
Size: A	Document Number: **UP-APL01**	Rev: **A1.1**
Date: *Wednesday, November 22, 2017*	Sheet: **1** of **45**	

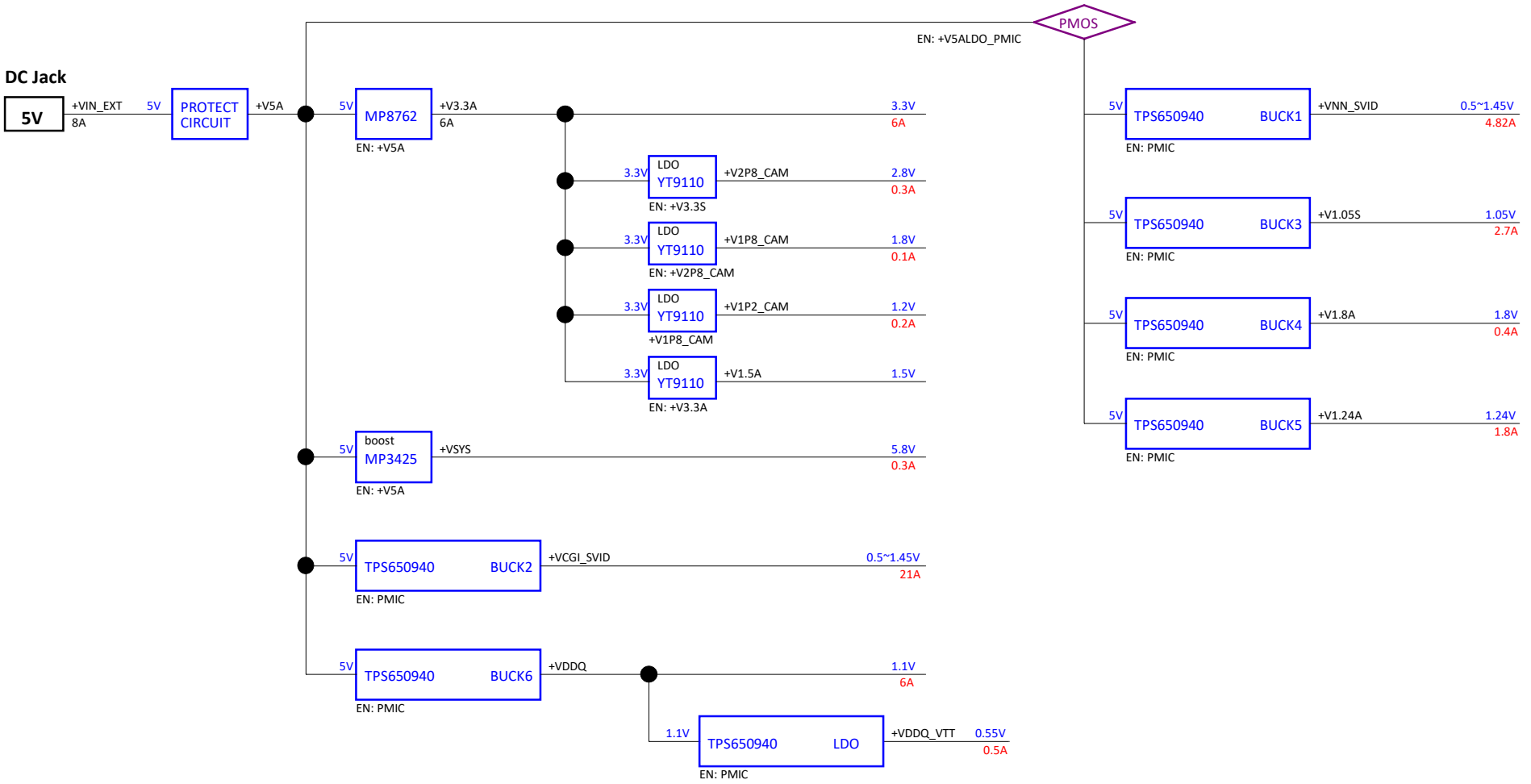
UP-SQUARE - APOLLO LAKE

DC INPUT: 5V



AAEON an ASUS assoc. co.

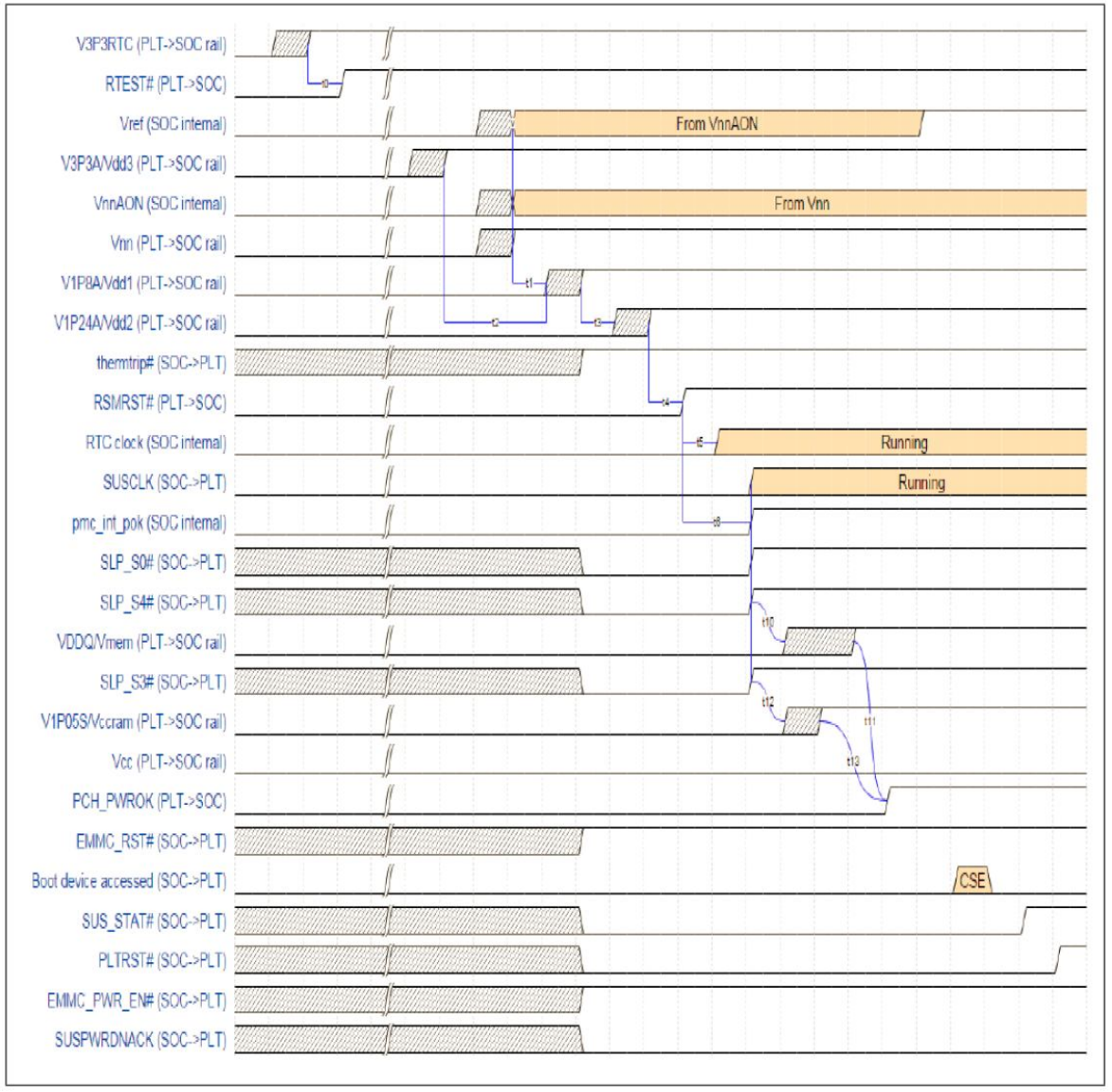
Title: BLOCK DIAGRAM		
Size: C	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 2 of 45	



AAEON an ASUS assoc. co.

Title: POWER TREE		
Size: C	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 3 of 45	

Figure 4-1. Apollo Lake G3 Cold Boot Power-Up



AAEON an ASUS assoc. co.	Title: POWER SEQUENEC		
	Size: C	Document Number: UP-APL01	Rev: A1.1
	Date: Wednesday, November 22, 2017	Sheet: 4 of 45	

EXHAT

Panasonic AXK6S60547YG

MAX10 GPIO/LVDS port	GPIO/EXHAT_LVDS0n	1	2	GPIO/EXHAT_LVDS1n	MAX10 GPIO/LVDS port
	GPIO/EXHAT_LVDS0p	3	4	GPIO/EXHAT_LVDS1p	
	GND	5	6	GND	
	GPIO/EXHAT_LVDS2n	7	8	GPIO/EXHAT_LVDS3n	
	GPIO/EXHAT_LVDS2p	9	10	GPIO/EXHAT_LVDS3p	
	GND	11	12	GND	
	GPIO/EXHAT_LVDS4n	13	14	GPIO/EXHAT_LVDS5n	
	GPIO/EXHAT_LVDS4p	15	16	GPIO/EXHAT_LVDS5p	
	GND	17	18	GND	
	GPIO/EXHAT_LVDS6n	19	20	GPIO/EXHAT_LVDS7n	
	GPIO/EXHAT_LVDS6p	21	22	GPIO/EXHAT_LVDS7p	
	GND	23	24	GND	
	GPIO/EXHAT_PLL1_INn	25	26	GPIO/EXHAT_PLL1_OUTn	
	GPIO/EXHAT_PLL1_INp	27	28	GPIO/EXHAT_PLL1_OUTp	
	GND	29	30	GND	
LPC	INT_SERIRQ_R	31	32	LPC_R_CLKOUT0	LPC
	LPC_CLKRU_N	33	34	GND	
	GND	35	36	LPC_R_AD3	
SPI	SIO_SPI_1_TXD	37	38	LPC_R_AD2	
	SIO_SPI_1_RXD	39	40	LPC_R_AD1	
	SIO_SPI_1_FS0	41	42	LPC_R_AD0	
	SIO_SPI_1_FS1	43	44	GND	
	SIO_SPI_1_CLK	45	46	LPC_FRAME_R	
	GND	47	48	GND	
I2C	~~I2C_SCL3_3V3~~ I2C_SCL6_3V3	49	50	AVS_DMIC_CLK_A1	DMIC
	~~I2C_SDA3_3V3~~ I2C_SDA6_3V3	51	52	AVS_DMIC_CLK_B1	
	GND	53	54	AVS_DMIC_CLK_AB2	
	~~I2C_SCL2_3V3~~/EXHAT_MUX0 I2C_SCL5_3V3	55	56	GND	
	~~I2C_SDA2_3V3~~/EXHAT_MUX1 I2C_SDA5_3V3	57	58	AVS_DMIC_DATA_1	
	GND	59	60	AVS_DMIC_DATA_2	

HAT40

UP2 board (**signal names from schema**)	UP-board			UP-board	UP2 board(**signal names from schema**)
3V3	3V3	1	2	5V	5V
HAT_I2C1_SDA	GPIO1/I2C1_SDA	3	4	5V	5V
HAT_I2C1_SCL	GPIO2/I2C1_SCL	5	6	Ground	Ground
HAT_ANALOG_IN1-HAT_R_GPIO1	GPIO3	7	8	GPIO16/UART_TX	HAT_UART1_TXD
Ground	Ground	9	10	GPIO17/UART_RX	HAT_UART1_RXD
HAT_ANALOG_IN2-HAT_UART1_R_R	GPIO4	11	12	GPIO18/I2S_CLK	HAT_I2S6_BCLK
HAT_ANALOG_IN3-HAT_R_GPIO2	GPIO5	13	14	Ground	Ground
HAT_ANALOG_IN4-HAT_R_GPIO3	GPIO6	15	16	GPIO19	HAT_SPI_1_FS1
3V3	3V3	17	18	GPIO20	HAT_SPI_1_RXD
HAT_SPI_0_TXD	GPIO7/SPI_MOSI	19	20	Ground	Ground
HAT_SPI_0_RXD	GPIO8/SPI_MISO	21	22	GPIO21	HAT_SPI_1_TXD
HAT_SPI_0_CLK	GPIO9/SPI_CLK	23	24	GPIO22/SPI_CS0N	HAT_SPI_0_FS0
Ground	Ground	25	26	GPIO23/SPI_CS1N	HAT_SPI_0_FS1
HAT_I2C0_SDA	GPIO10/I2C0_SDA	27	28	GPIO24/I2C0_SCL	HAT_I2C0_SCL
HAT_GPIO4	GPIO11	29	30	Ground	Ground
HAT_SPI_1_CLK	GPIO12	31	32	GPIO25/PWM0	HAT_PWM0
HAT_PWM1	GPIO13/PWM1	33	34	Ground	Ground
HAT_I2S6_WS_SYNC	GPIO14/I2S_FRM	35	36	GPIO26	HAT_UART1_CTS
HAT_SPI_1_FS0	GPIO15	37	38	GPIO27/I2S_DATAIN	HAT_I2S6_SDI
Ground	Ground	39	40	GPIO28/I2S_DATAOUT	HAT_I2S6_SDO

AAEON an ASUS assoc. co.

Title: **EXHAT, HAT40 Pin Define**

Size: Custom | Document Number: UP-APL01 | Rev: A1.1

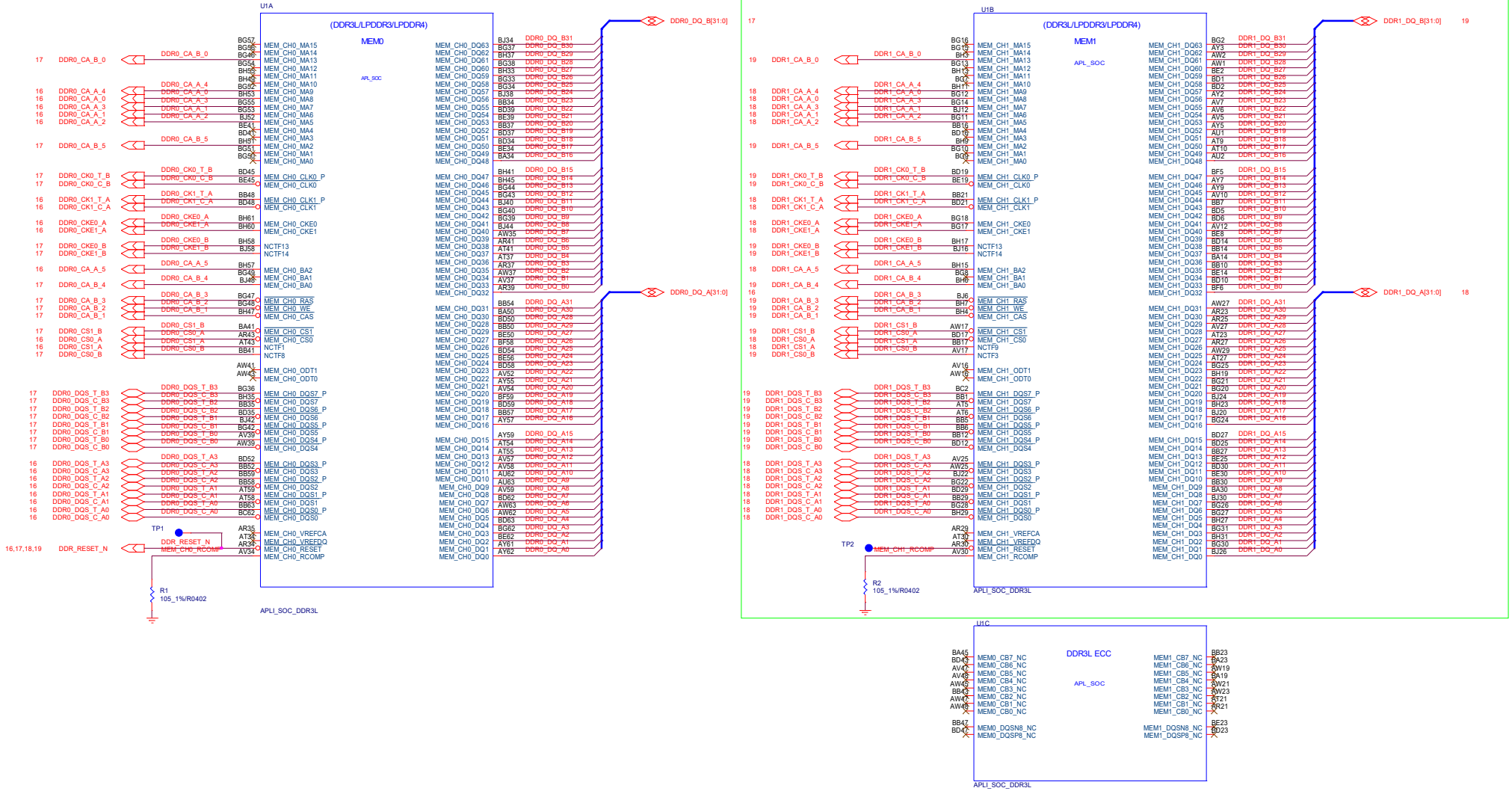
Date: *Wednesday, November 22, 2017* | Sheet: 5 of 45

name on RTL-code	Location	I/O Bank	I/O Standard - VCCIO	VREF Group
AVS_I2S2_MCLK	PIN_F4	1B	1.8 V	B1_N0
BT_HOST_WAKE	PIN_E8	8	1.8 V	B8_N0
nSTATUS	PIN_C4	8	1.8 V	B8_N0
CONF_DONE	PIN_C5	8	1.8 V	B8_N0
CONFIG_SEL	PIN_D7	8	1.8 V	B8_N0
CPU_prog_JTAG_TCK	PIN_G2	1B	1.8 V	B1_N0
CPU_prog_JTAG_TDI	PIN_F5	1B	1.8 V	B1_N0
CPU_prog_JTAG_TDO	PIN_F6	1B	1.8 V	B1_N0
CPU_prog_JTAG_TMS	PIN_G1	1B	1.8 V	B1_N0
enableJTAG	PIN_E5	1B	1.8 V	B1_N0
FPGA_fw_reload	PIN_E7	8	1.8 V	B8_N0
FPGA_OE	PIN_D8	8	1.8 V	B8_N0
FPGA_RST	PIN_B9	8	1.8 V	B8_N0
I2C_SCL0	PIN_A7	8	1.8 V	B8_N0
I2C_SCL1	PIN_A9	8	1.8 V	B8_N0
~~I2C_SCL5~~ I2C_SCL2	PIN_B10	8	1.8 V	B8_N0
~~I2C_SCL6~~ I2C_SCL3	PIN_C10	8	1.8 V	B8_N0
I2C_SDA0	PIN_A8	8	1.8 V	B8_N0
I2C_SDA1	PIN_A10	8	1.8 V	B8_N0
~~I2C_SDA5~~ I2C_SDA2	PIN_A11	8	1.8 V	B8_N0
~~I2C_SDA6~~ I2C_SDA3	PIN_C9	8	1.8 V	B8_N0
ISH_GPIO_0	PIN_D1	1A	1.8 V	B1_N0
ISH_GPIO_1	PIN_C2	1A	1.8 V	B1_N0
ISH_GPIO_2	PIN_C1	1A	1.8 V	B1_N0
ISH_GPIO_3	PIN_B1	1A	1.8 V	B1_N0
ISH_GPIO_4	PIN_E1	1A	1.8 V	B1_N0
ISH_GPIO_5	PIN_E3	1A	1.8 V	B1_N0
ISH_GPIO_6	PIN_E4	1A	1.8 V	B1_N0
ISH_GPIO_7	PIN_F1	1A	1.8 V	B1_N0
ISH_GPIO_8	PIN_G4	1B	1.8 V	B1_N0
ISH_GPIO_9	PIN_H2	1B	1.8 V	B1_N0
ISH_GPIO_10	PIN_H3	1B	1.8 V	B1_N0
ISH_GPIO_11	PIN_H1	1B	1.8 V	B1_N0
ISH_GPIO_12	PIN_B7	8	1.8 V	B8_N0
ISH_GPIO_13	PIN_G10	6	1.8 V	B6_N0
ISH_GPIO_14	PIN_G9	6	1.8 V	B6_N0
ISH_GPIO_15	PIN_A5	8	1.8 V	B8_N0
LPSS_UART1_CTS	PIN_A6	8	1.8 V	B8_N0
LPSS_UART1_RTS	PIN_A4	8	1.8 V	B8_N0
LPSS_UART1_RXD	PIN_A3	8	1.8 V	B8_N0
LPSS_UART1_TXD	PIN_A2	8	1.8 V	B8_N0
OSC_CLK_OUT_0	PIN_E13	6	1.8 V	B6_N0
OSC_CLK_OUT_1	PIN_F13	6	1.8 V	B6_N0
PWM0	PIN_E9	6	1.8 V	B6_N0
PWM1	PIN_D9	6	1.8 V	B6_N0
SDIO_CLK	PIN_B2	8	1.8 V	B8_N0
SDIO_CMD	PIN_D6	8	1.8 V	B8_N0
SDIO_D0	PIN_B3	8	1.8 V	B8_N0
SDIO_D1	PIN_B4	8	1.8 V	B8_N0
SDIO_D2	PIN_B5	8	1.8 V	B8_N0
SDIO_D3	PIN_B6	8	1.8 V	B8_N0
SDIO_PWR_DOWN	PIN_E6	8	1.8 V	B8_N0
SIO_SPI_0_CLK	PIN_C12	6	1.8 V	B6_N0
SIO_SPI_0_FS0	PIN_D11	6	1.8 V	B6_N0
SIO_SPI_0_FS1	PIN_D13	6	1.8 V	B6_N0
SIO_SPI_0_RXD	PIN_B12	6	1.8 V	B6_N0
SIO_SPI_0_TXD	PIN_B13	6	1.8 V	B6_N0
AVS_I2S2_SDI	PIN_C11	6	1.8 V	B6_N0
AVS_I2S2_WS_SYNC	PIN_C13	6	1.8 V	B6_N0
PWM3	PIN_D12	6	1.8 V	B6_N0
AVS_I2S2_SDO	PIN_B11	6	1.8 V	B6_N0
AVS_I2S2_BCLK	PIN_A12	6	1.8 V	B6_N0
SIO_SPI_2_CLK	PIN_F12	6	1.8 V	B6_N0
SIO_SPI_2_FS0	PIN_F10	6	1.8 V	B6_N0
SIO_SPI_2_FS1	PIN_F9	6	1.8 V	B6_N0
SIO_SPI_2_FS2	PIN_F8	6	1.8 V	B6_N0
SIO_SPI_2_RXD	PIN_E12	6	1.8 V	B6_N0
SIO_SPI_2_TXD	PIN_E10	6	1.8 V	B6_N0
GPIO_EXHAT_LVDS0n	PIN_K5	3	3.3V	B3_N0
GPIO_EXHAT_LVDS0p	PIN_J5	3	3.3V	B3_N0
GPIO_EXHAT_LVDS1n	PIN_J6	3	3.3V	B3_N0
GPIO_EXHAT_LVDS1p	PIN_K6	3	3.3V	B3_N0
GPIO_EXHAT_LVDS2n	PIN_J7	3	3.3V	B3_N0
GPIO_EXHAT_LVDS2p	PIN_K7	3	3.3V	B3_N0
GPIO_EXHAT_LVDS3n	PIN_J8	3	3.3V	B3_N0
GPIO_EXHAT_LVDS3p	PIN_K8	3	3.3V	B3_N0
GPIO_EXHAT_LVDS4n	PIN_L5	3	3.3V	B3_N0
GPIO_EXHAT_LVDS4p	PIN_L4	3	3.3V	B3_N0
GPIO_EXHAT_LVDS5n	PIN_M4	3	3.3V	B3_N0
GPIO_EXHAT_LVDS5p	PIN_M5	3	3.3V	B3_N0
GPIO_EXHAT_LVDS6n	PIN_N4	3	3.3V	B3_N0
GPIO_EXHAT_LVDS6p	PIN_N5	3	3.3V	B3_N0
GPIO_EXHAT_LVDS7n	PIN_N6	3	3.3V	B3_N0
GPIO_EXHAT_LVDS7p	PIN_M7	3	3.3V	B3_N0
I2C_VLS_OE0	PIN_N7	3	3.3V	B3_N0
I2C_VLS_OE1	PIN_N8	3	3.3V	B3_N0
GPIO_EXHAT_PLL1_INn	PIN_G5	2	3.3V	B2_N0
GPIO_EXHAT_PLL1_INp	PIN_H6	2	3.3V	B2_N0
GPIO_EXHAT_PLL1_OUTn	PIN_M3	2	3.3V	B2_N0
GPIO_EXHAT_PLL1_OUTp	PIN_L3	2	3.3V	B2_N0
HAT_GPIO4	PIN_N11	3	3.3V	B3_N0
HAT_I2C0_SCL	PIN_J1	2	3.3V	B2_N0
HAT_I2C0_SDA	PIN_J2	2	3.3V	B2_N0
HAT_I2C1_SCL	PIN_J9	5	3.3V	B5_N0
HAT_I2C1_SDA	PIN_J10	5	3.3V	B5_N0
HAT_I2S6_BCLK	PIN_K10	5	3.3V	B5_N0
HAT_I2S6_SDI	PIN_K12	5	3.3V	B5_N0
HAT_I2S6_SDO	PIN_J12	5	3.3V	B5_N0
HAT_I2S6_WS_SYNC	PIN_K11	5	3.3V	B5_N0
HAT_PWM0	PIN_M2	2	3.3V	B2_N0
HAT_PWM1	PIN_L12	5	3.3V	B5_N0
HAT_R_GPIO1	PIN_M13	3	3.3V	B3_N0
HAT_R_GPIO2	PIN_M12	3	3.3V	B3_N0
HAT_R_GPIO3	PIN_N12	3	3.3V	B3_N0
HAT_SPI_0_CLK	PIN_H10	5	3.3V	B5_N0
HAT_SPI_0_FS0	PIN_H8	5	3.3V	B5_N0
HAT_SPI_0_FS1	PIN_H9	5	3.3V	B5_N0
HAT_SPI_0_RXD	PIN_G13	5	3.3V	B5_N0
HAT_SPI_0_TXD	PIN_G12	5	3.3V	B5_N0
HAT_SPI_1_CLK	PIN_M1	2	3.3V	B2_N0
HAT_SPI_1_FS0	PIN_N2	2	3.3V	B2_N0
HAT_SPI_1_FS1	PIN_N3	2	3.3V	B2_N0
HAT_SPI_1_RXD	PIN_K1	2	3.3V	B2_N0
HAT_SPI_1_TXD	PIN_K2	2	3.3V	B2_N0
HAT_UART1_CTS	PIN_L13	5	3.3V	B5_N0
HAT_UART1_R_RTS	PIN_K13	5	3.3V	B5_N0
HAT_UART1_RXD	PIN_J13	5	3.3V	B5_N0
HAT_UART1_TXD	PIN_H13	5	3.3V	B5_N0
LED0_3V3	PIN_H5	2	3.3V	B2_N0
LED1_3V3	PIN_H4	2	3.3V	B2_N0
LED2_3V3	PIN_L1	2	3.3V	B2_N0
LED3_3V3	PIN_L2	2	3.3V	B2_N0
~~*LPC_CLKRU_N*~~ *UART2_CTS_3V3*	PIN_L11	3	3.3V	B3_N0
~~*LPC_FRAME_R*~~ *FPGA_CEC_IN*	PIN_L10	3	3.3V	B3_N0
~~*LPC_R_AD0*~~ *UART2_RTS_3V3*	PIN_M11	3	3.3V	B3_N0
~~*LPC_R_AD1*~~ *FPGA_CEC_OUT*	PIN_M10	3	3.3V	B3_N0
~~*LPC_R_AD2*~~ *EXHAT_MUX1*	PIN_M9	3	3.3V	B3_N0
~~*LPC_R_AD3*~~ *EXHAT_MUX0*	PIN_M8	3	3.3V	B3_N0
~~*LPC_R_CLKOUT0*~~ *UART2_RXD_3V3*	PIN_N9	3	3.3V	B3_N0
~~*INT_SERIRQ_R*~~ *UART2_TXD_3V3*	PIN_N10	3	3.3V	B3_N0

AAEON an ASUS assoc. co.

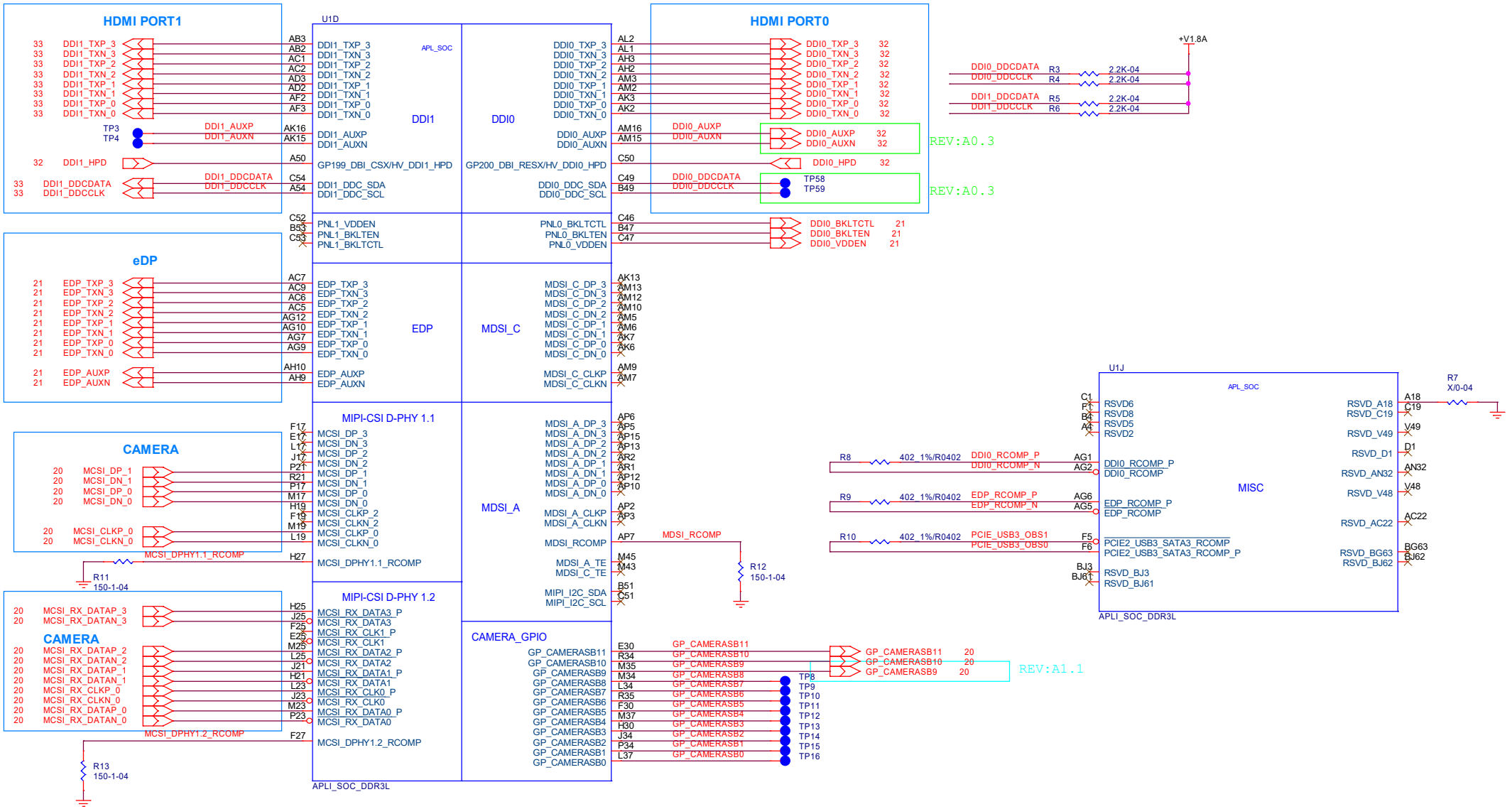
Title: CPLD Pin Define		
Size: C	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 6 of 45	

REV:A0.2



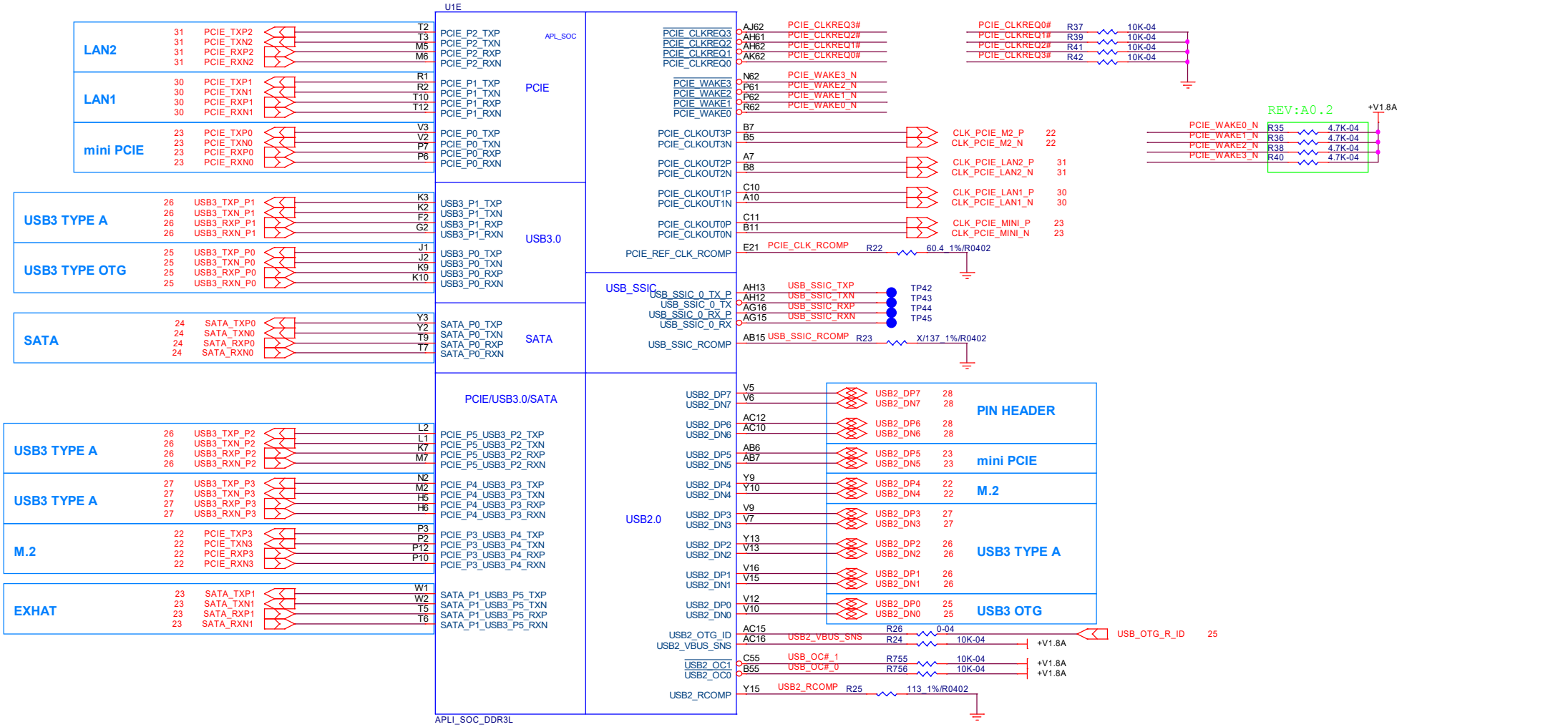
<Core Design>

AAEON an ASUS assoc. co.	Title: SOC_DDR		
	Size: C	Document Number: UP-APL01	Rev: A1.1
	Date: Wednesday, November 22, 2017	Sheet: 7 of 45	



<Core Design>

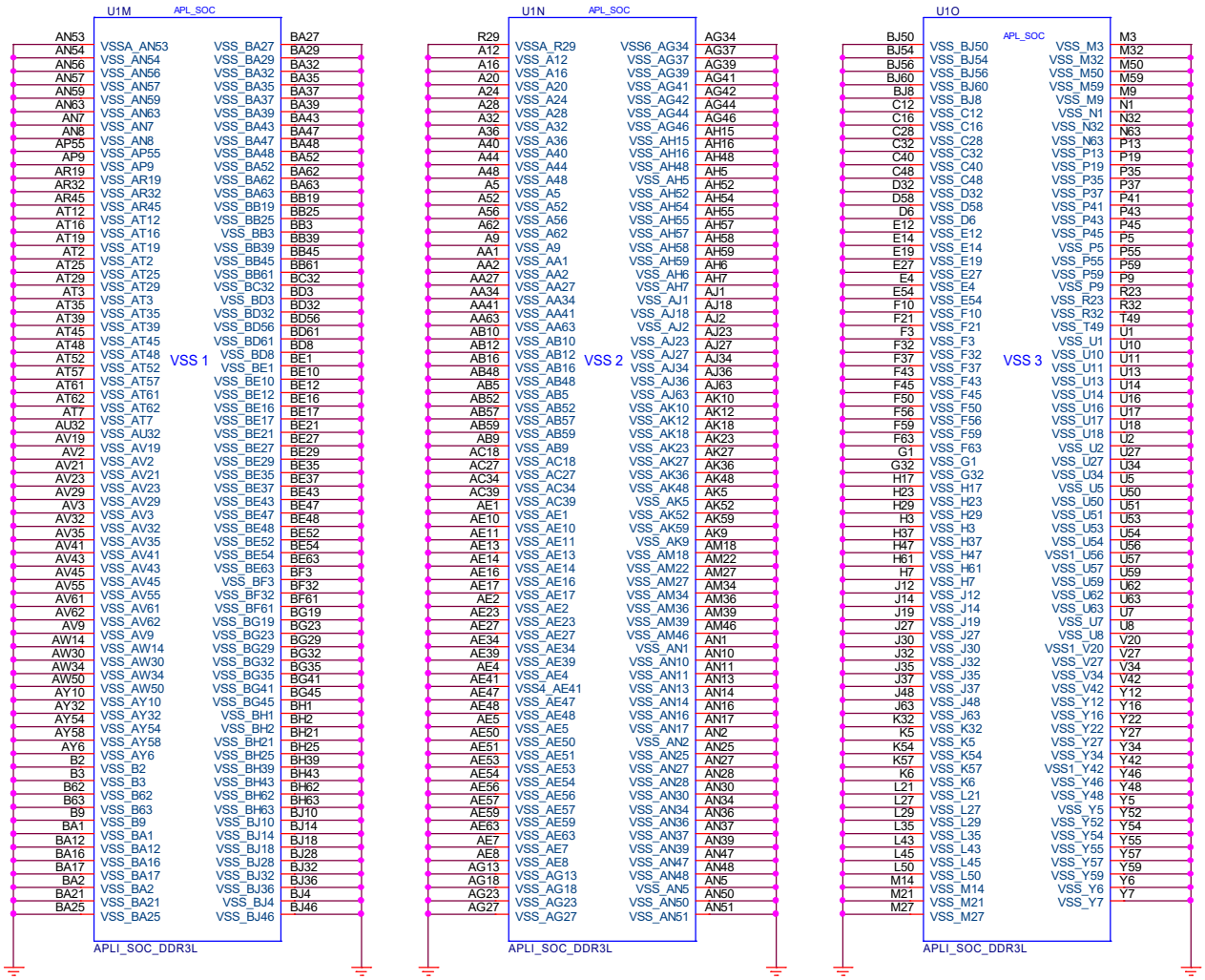
AAEON an ASUS assoc. co.	Title: SOC_DISPLAY	
Size: Custom	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 8 of 45	

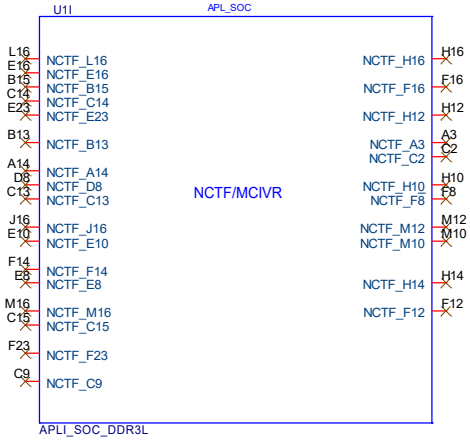


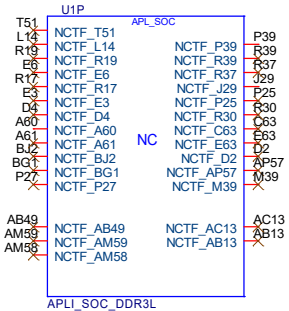
<Core Design>

AAEON an ASUS assoc. co.

Title: SOC_SATA_PCIE_USB		
Size: Custom	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 9 of 45	

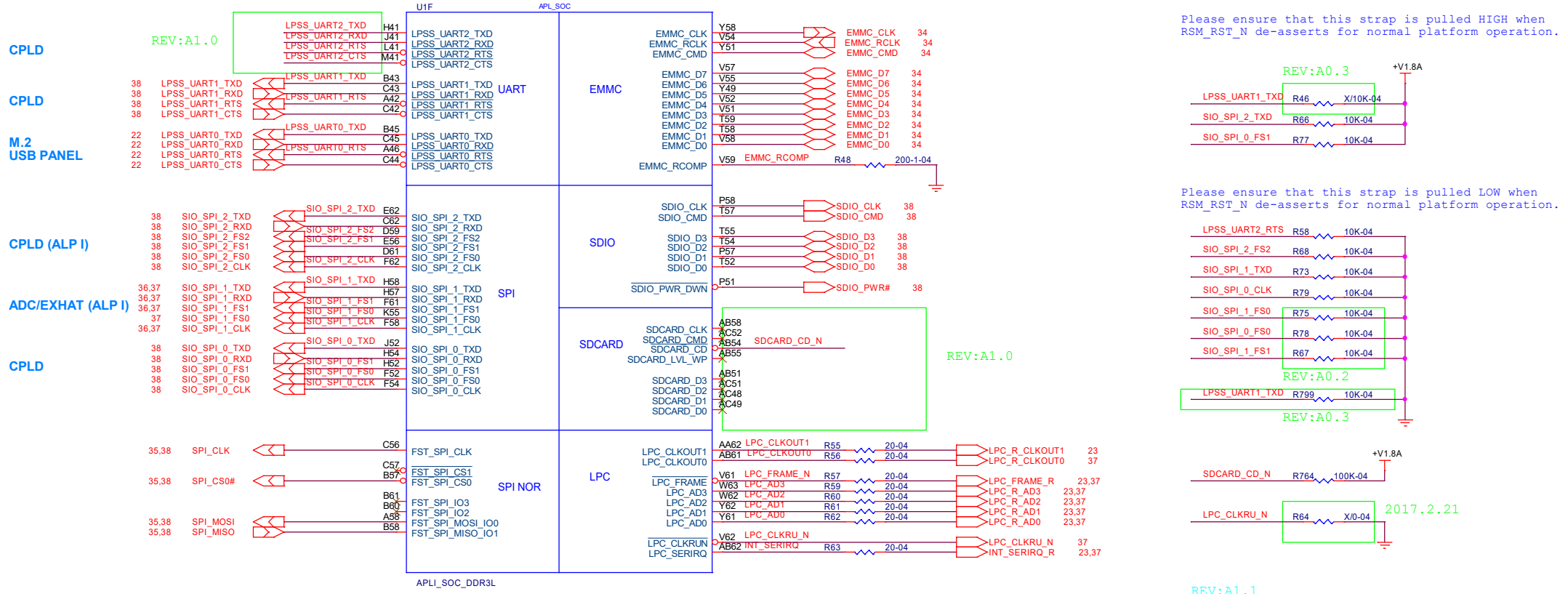




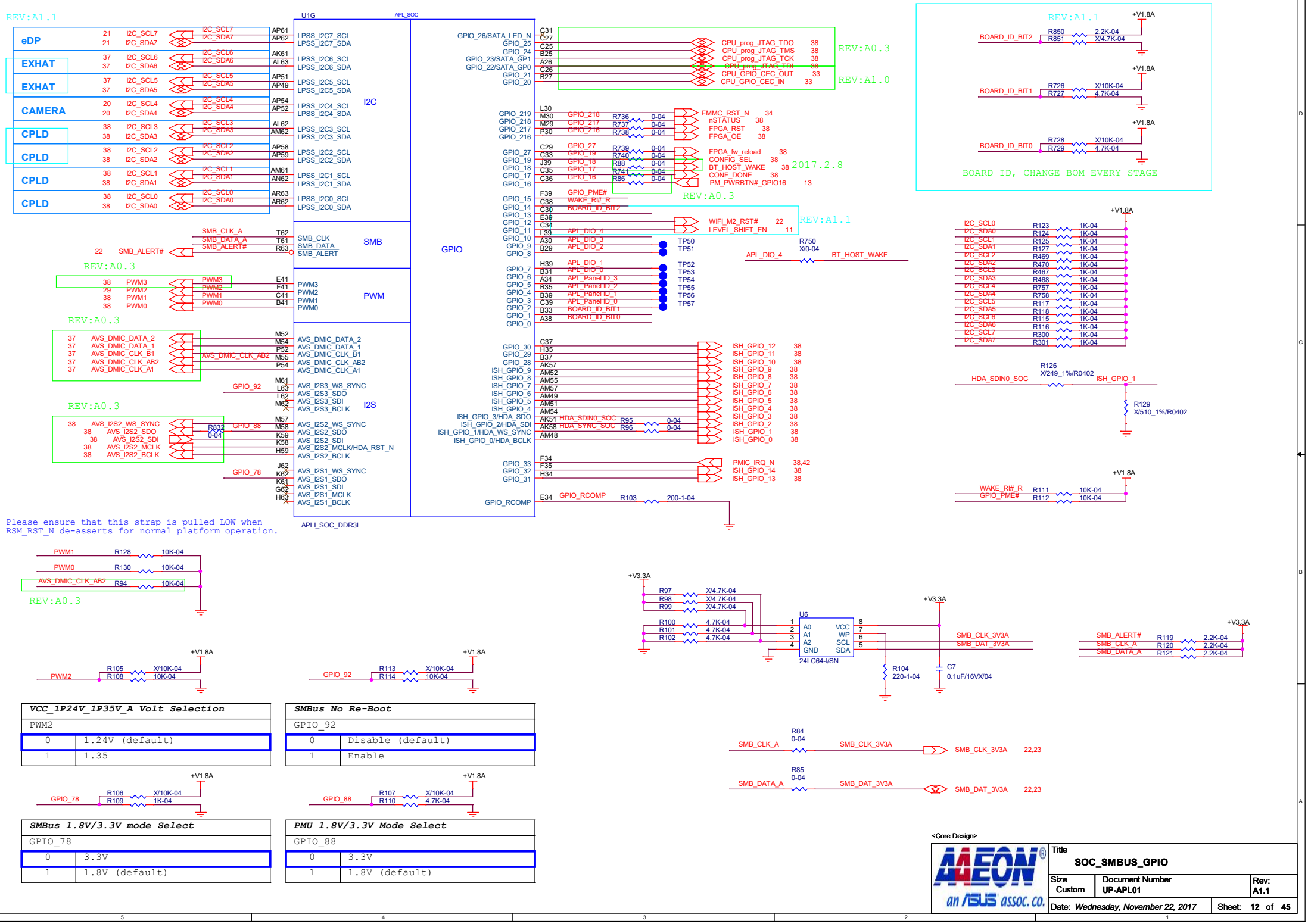


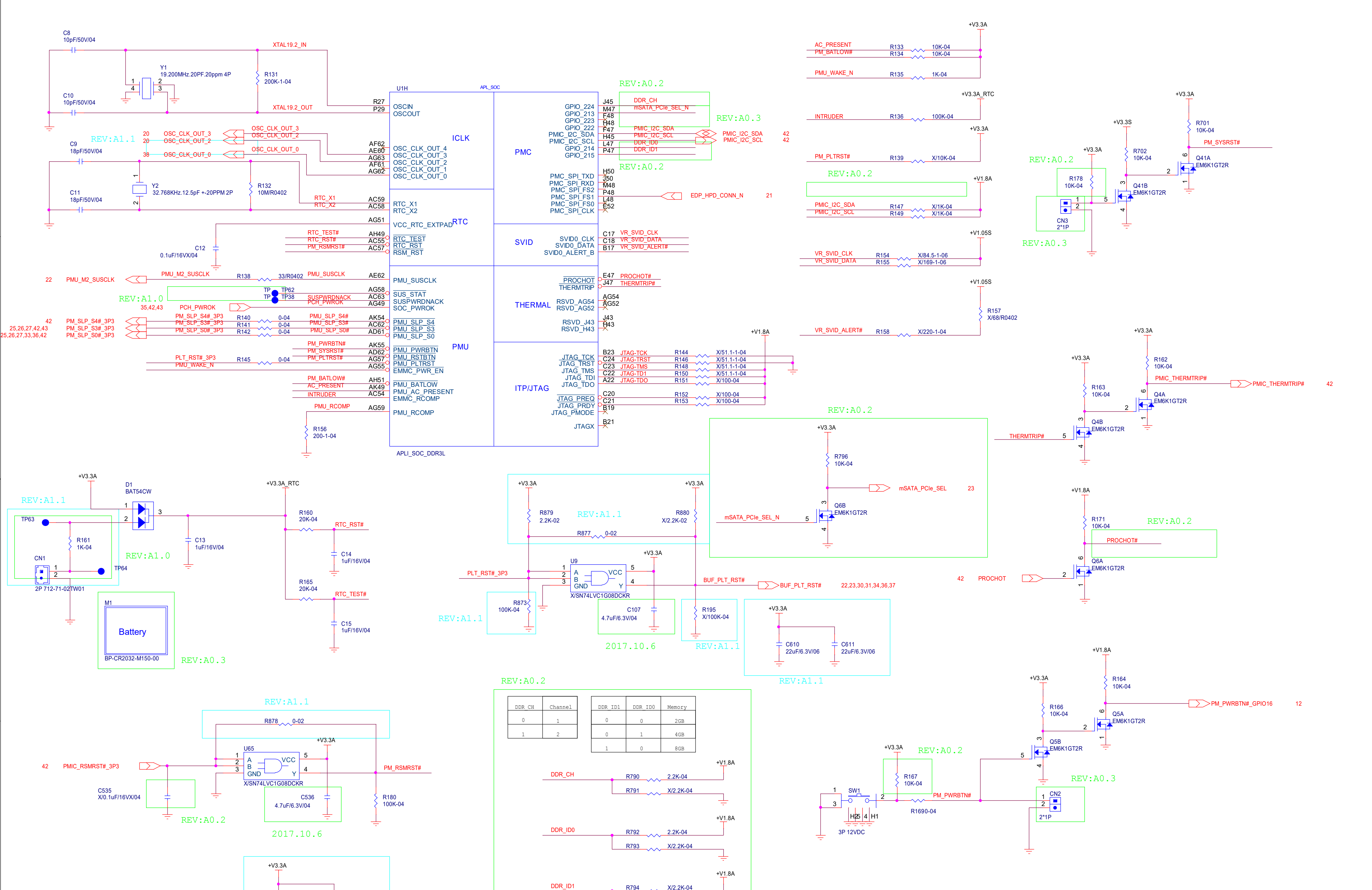
<Core Design>

AAEON an ASUS assoc. co.	Title: SOC_GND	
	Size: Custom	Document Number: UP-APL01
	Date: Wednesday, November 22, 2017	Sheet: 10 of 45



Title	SOC_LPC_SPI_EMMC_SD
Size	Custom
Document Number	UP-APL01
Rev:	A1.1
Date:	Wednesday, November 22, 2017
Sheet:	11 of 45


REV:A1.1
U1G
APL_SOC
eDP
EXHAT
EXHAT
CAMERA
CPLD
CPLD
CPLD
CPLD
I2C
SMB
PWM
I2S
GPIO
APLI_SOC_DDR3L
REV:A0.3
REV:A1.0
REV:A1.1
2017.2.8
BOARD ID, CHANGE BOM EVERY STAGE
Please ensure that this strap is pulled LOW when
RSM_RST_N de-asserts for normal platform operation.
VCC_1P24V_1P35V_A Volt Selection
PWM2
0 1.24V (default)
1 1.35
SMBus No Re-Boot
GPIO_92
0 Disable (default)
1 Enable
SMBus 1.8V/3.3V mode Select
GPIO_78
0 3.3V
1 1.8V (default)
PMU 1.8V/3.3V Mode Select
GPIO_88
0 3.3V
1 1.8V (default)
<Core Design>
Title
SOC_SMBUS_GPIO
Size Custom
Document Number UP-APL01
Rev: A1.1
Date: Wednesday, November 22, 2017
Sheet: 12 of 45

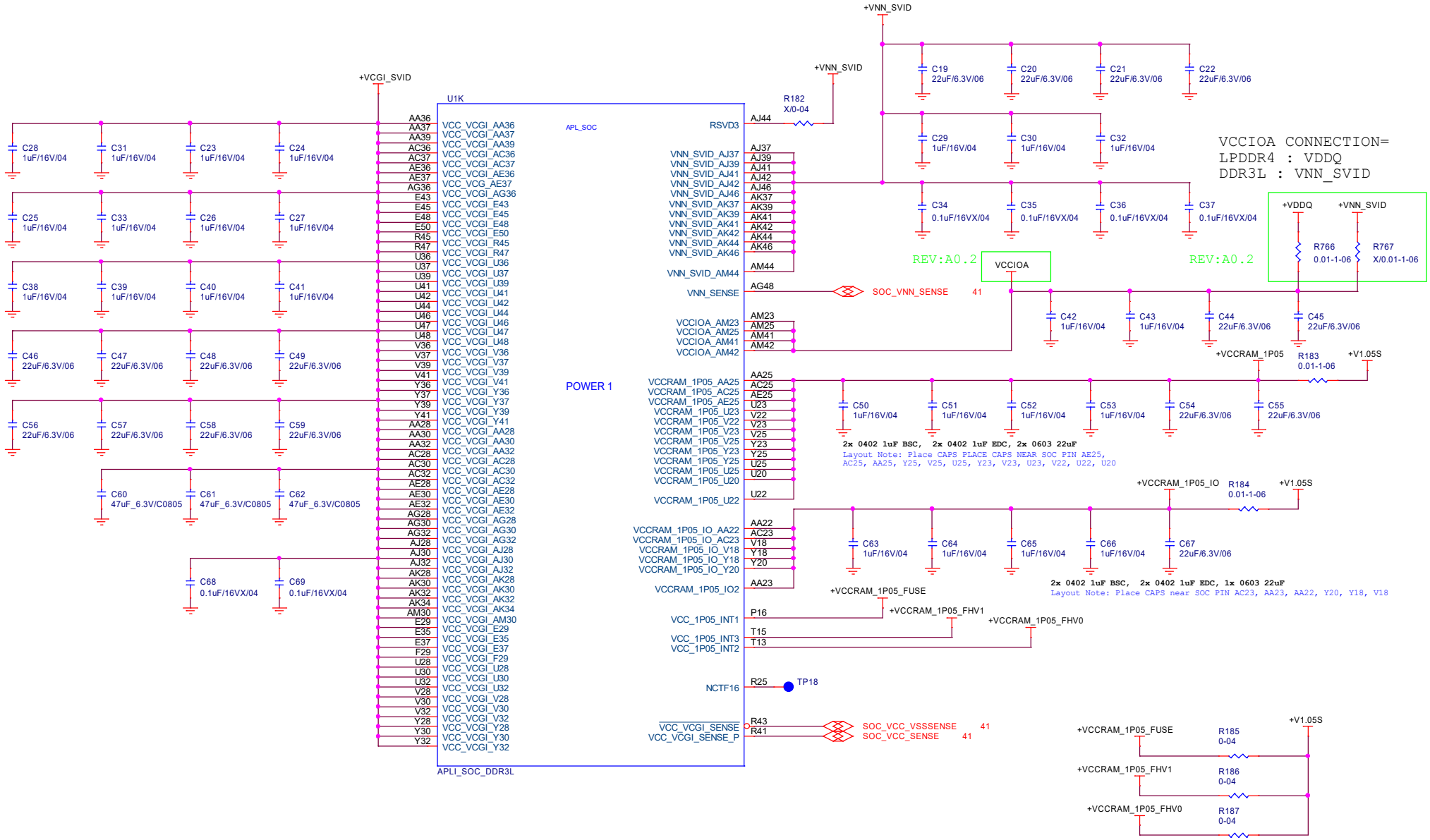


DDR_CH	Channel
0	1
1	2

DDR_ID1	DDR_ID0	Memory
0	0	2GB
0	1	4GB
1	0	8GB

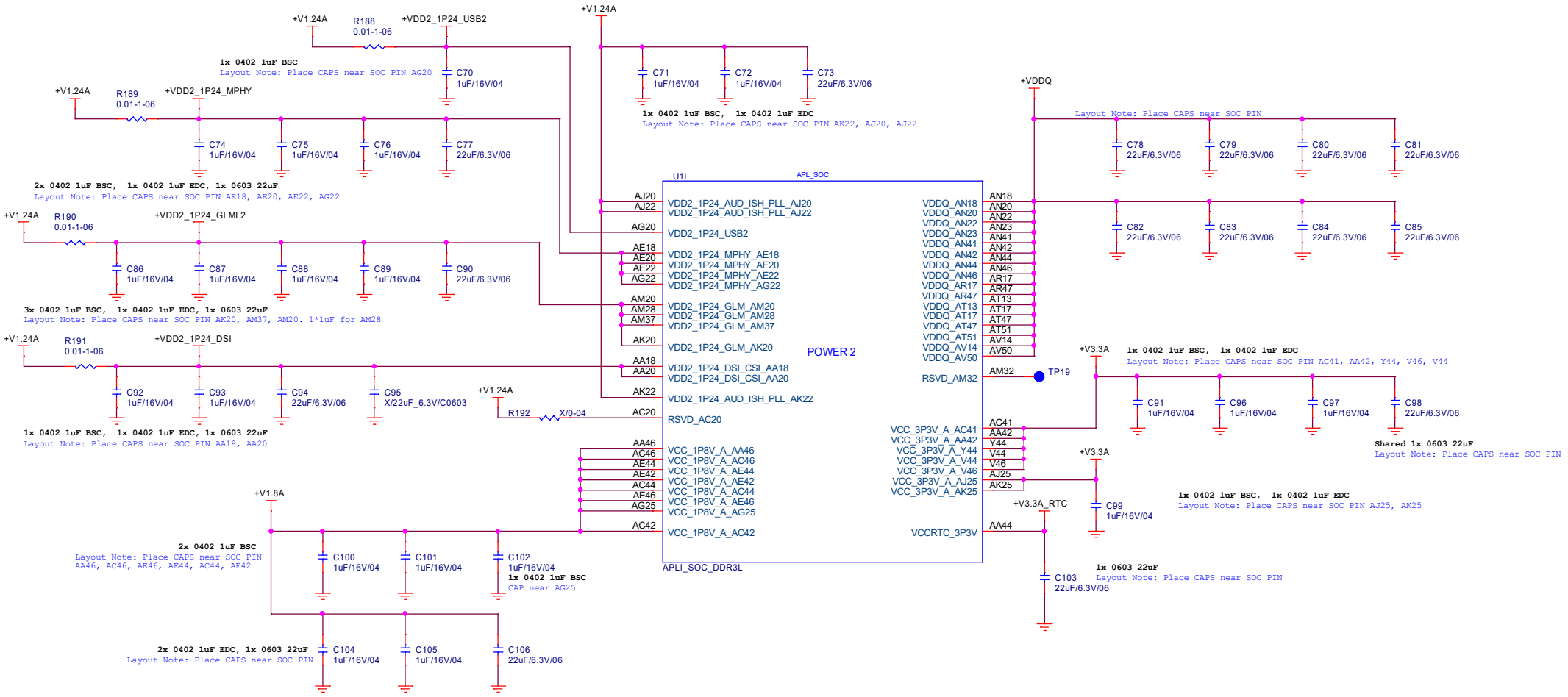
AAEON an ASUS assoc. co.

Title: SOC_CLK_PCU_RTC		
Size: Custom	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 13 of 45	



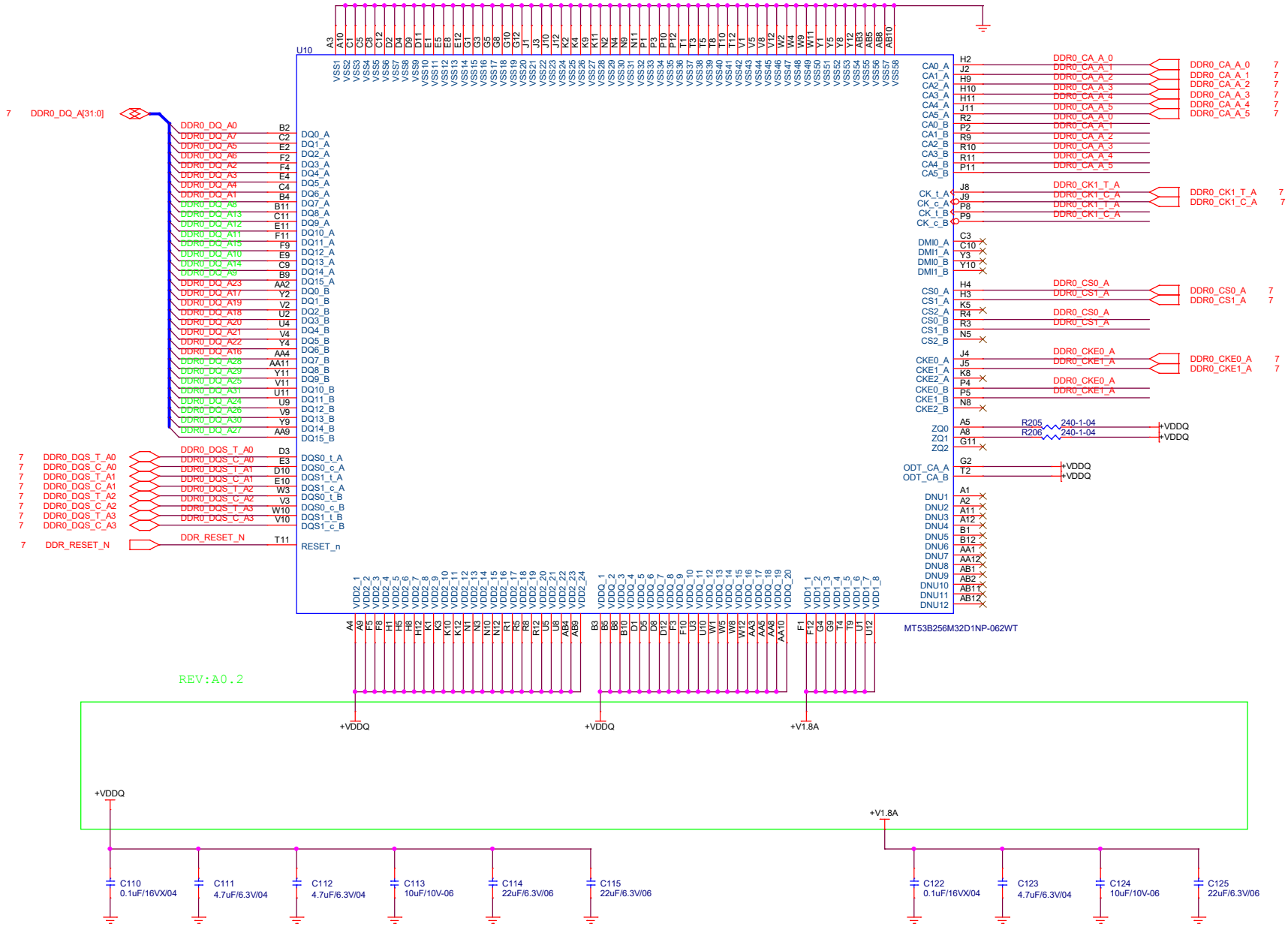
<Core Design>

AAEON an ASUS assoc. co.	Title: SOC_POWER I	
Size: Custom	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 14 of 45	

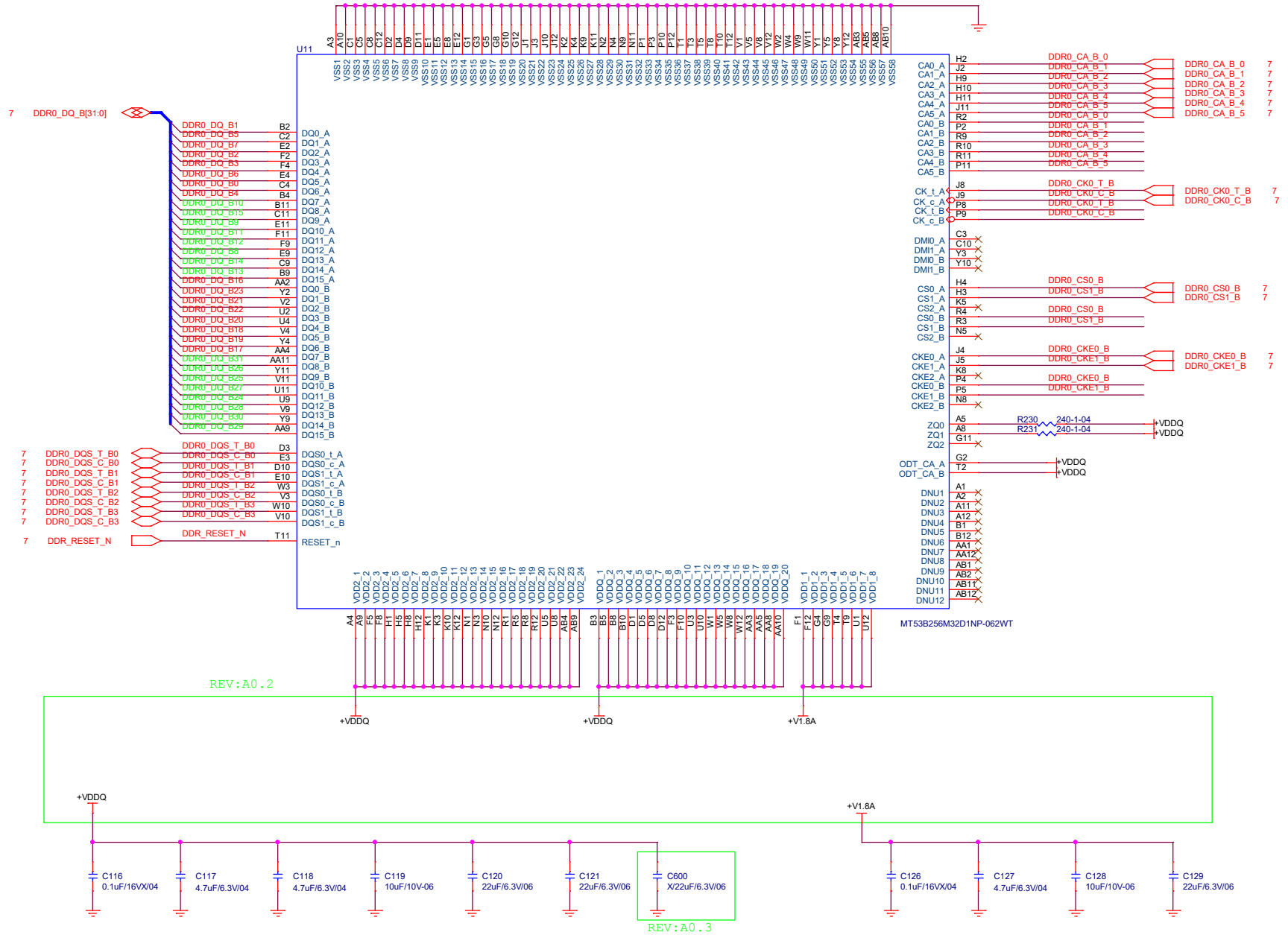


<Core Design>

AAEON an ASUS assoc. co.	Title: SOC_POWER II	
	Size: Custom	Document Number: UP-APL01
	Rev: A1.1	
	Date: Wednesday, November 22, 2017	Sheet: 15 of 45

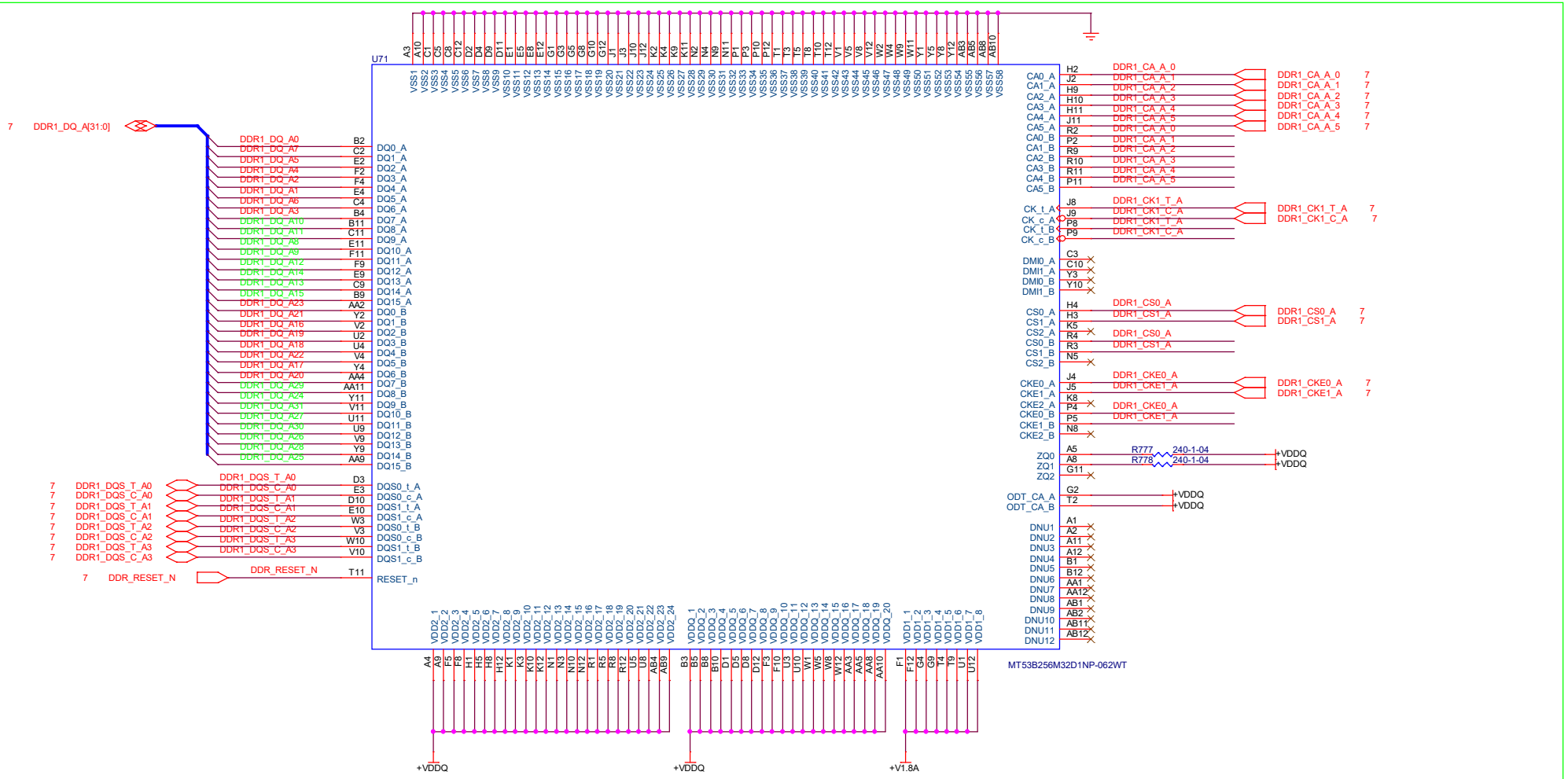


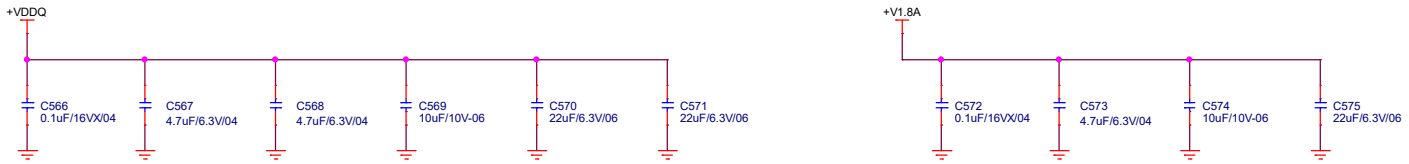
Title	LPDDR4 (1/4)
Size	Custom
Document Number	UP-APL01
Rev:	A1.1
Date:	Wednesday, November 22, 2017
Sheet:	16 of 45



AAEON an ASUS assoc. co.	Title: LPDDR4 (2/4)	
Size: Custom	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 17 of 45	

REV:A0.2

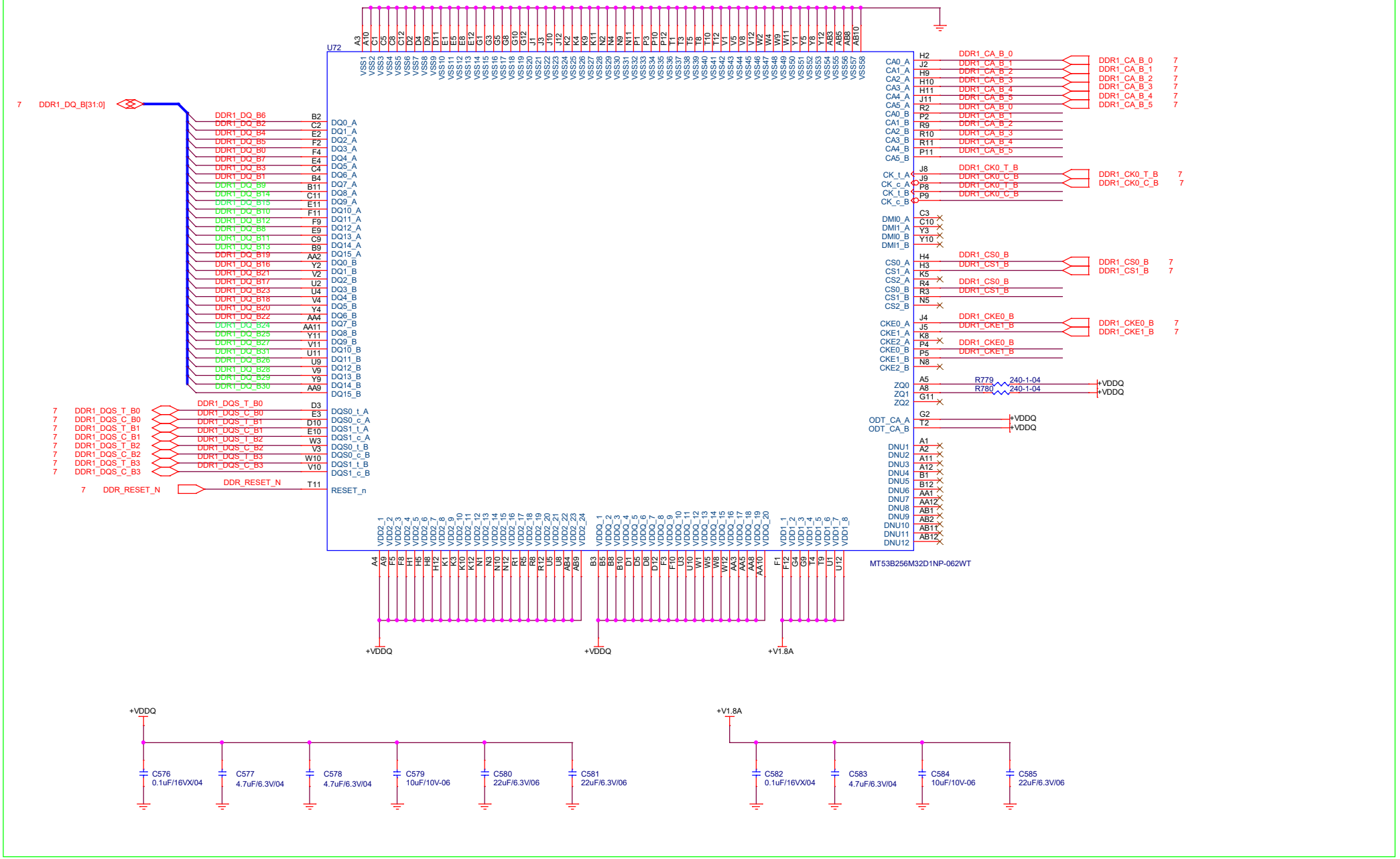




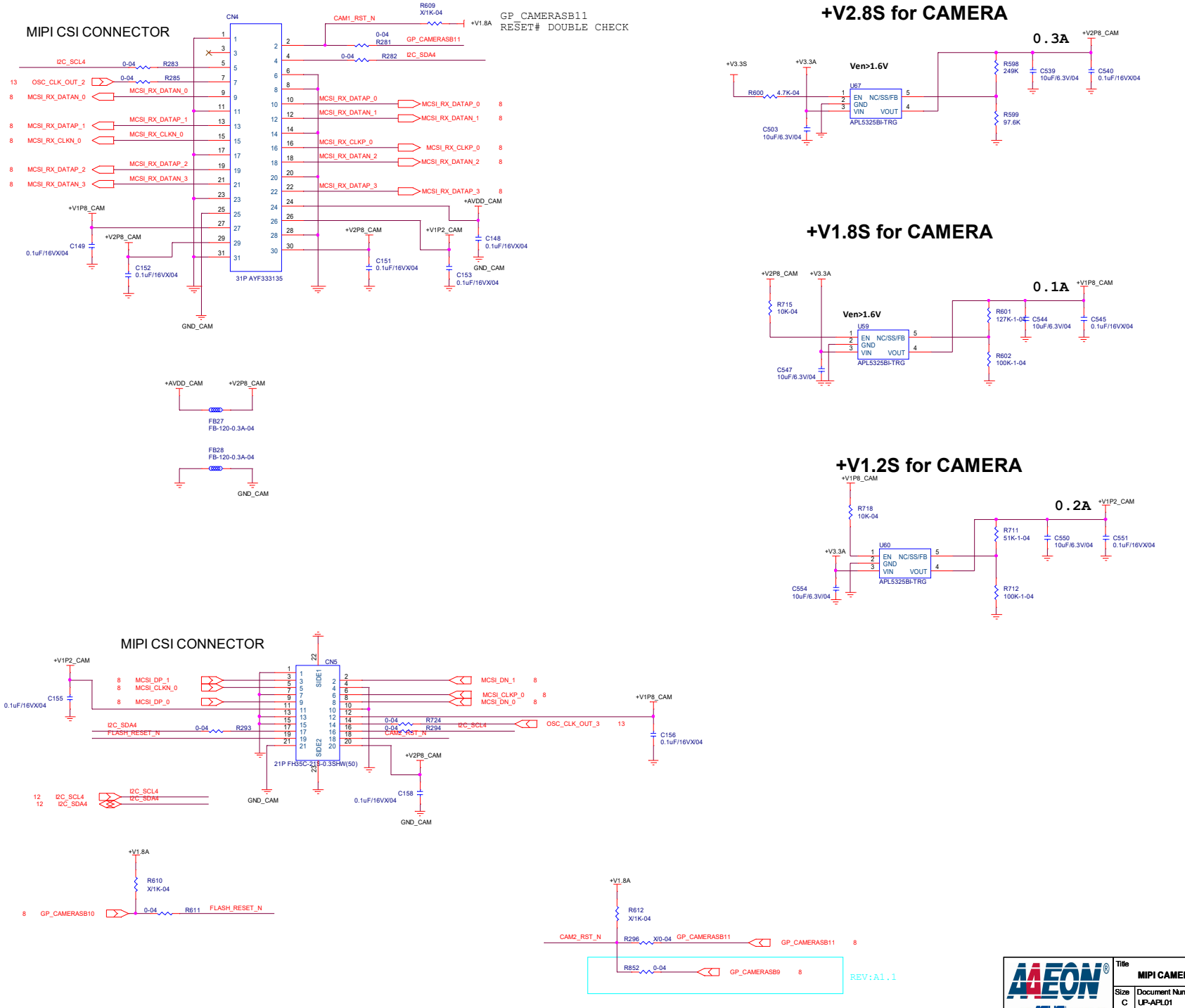
AAEON an ASUS assoc. co.

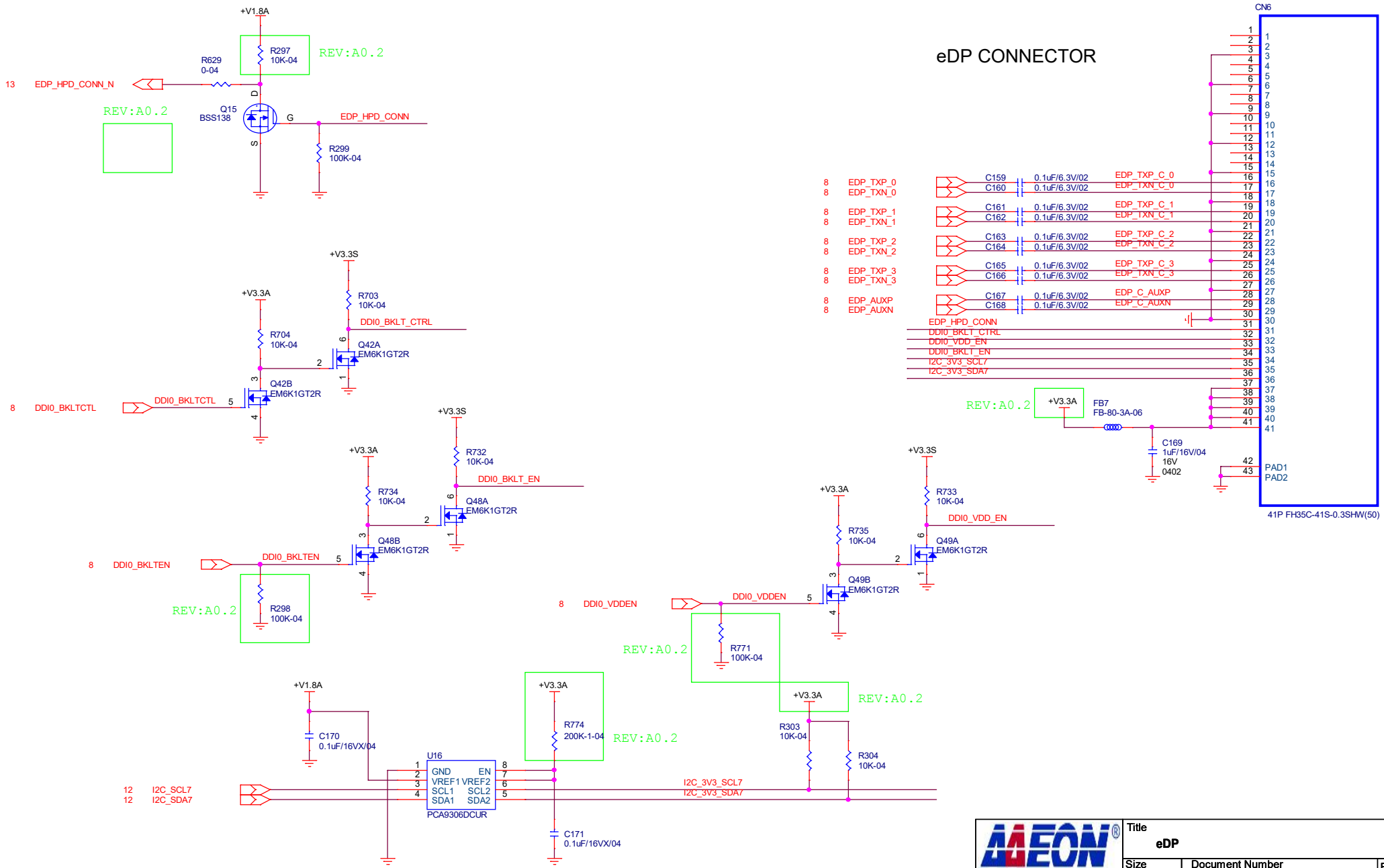
Title: LPDDR4 (3/4)		
Size: Custom	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 18 of 45	

REV:A0.2



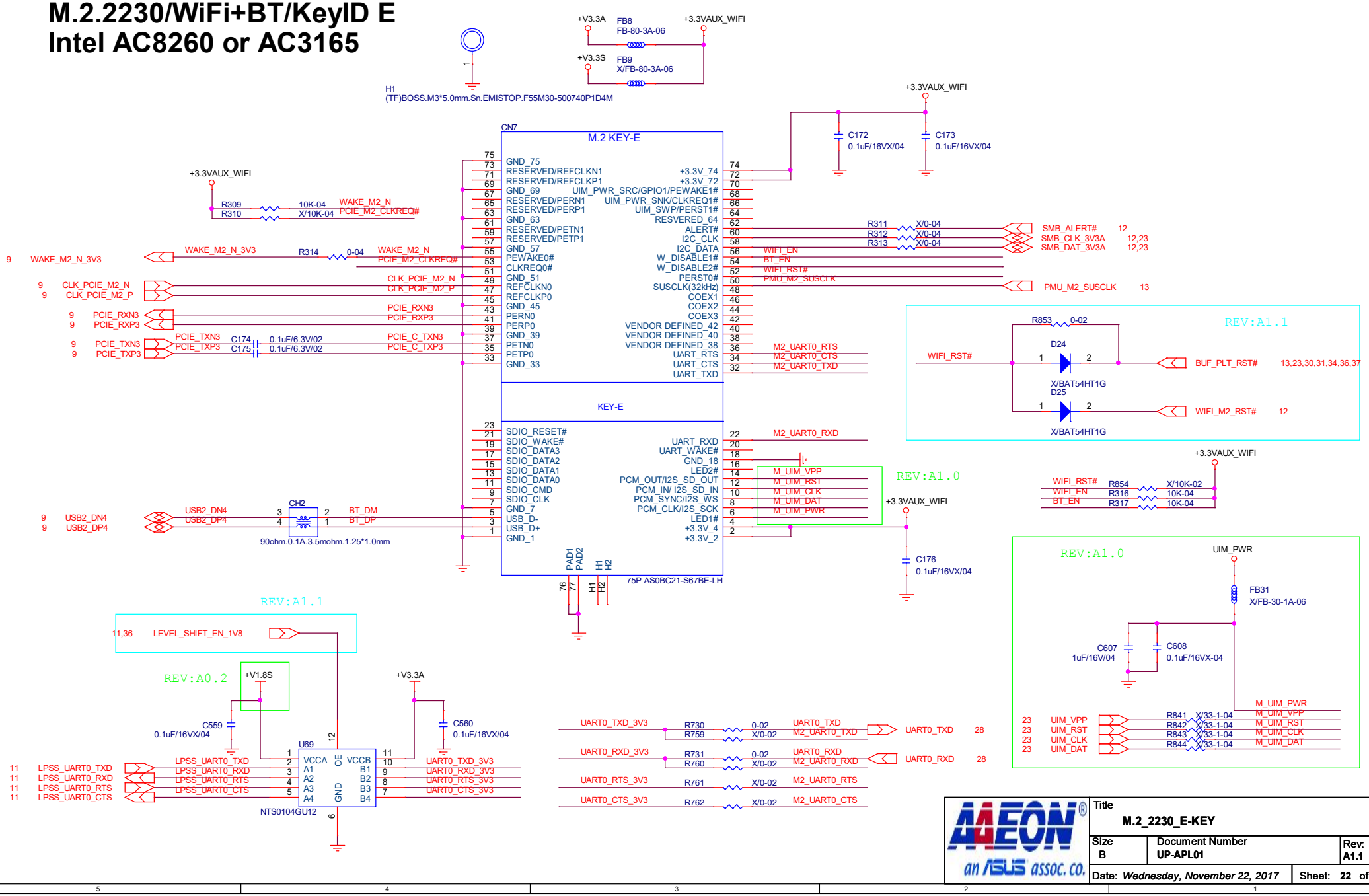
AAEON an ASUS assoc. co.	Title: LPDDR3 (4/4)		
	Size: Custom	Document Number: UP-APL01	Rev: A1.1
	Date: Wednesday, November 22, 2017	Sheet: 19 of 45	


MIPI CSI CONNECTOR
CN4
31P AYF333135
GP_CAMERASB11
RESET# DOUBLE CHECK
+V2.8S for CAMERA
0.3A
Ven>1.6V
U67
APL5325BI-TRG
+V1.8S for CAMERA
0.1A
U59
APL5325BI-TRG
+V1.2S for CAMERA
0.2A
U60
APL5325BI-TRG
MIPI CSI CONNECTOR
CN5
21P FH35C-21S-0.3SHW(50)
REV:A1.1
AAEON
an ASUS assoc. co.
Title
MIPI CAMERA
Size C
Document Number UP-APL01
Rev A1.1
Date: Wednesday, November 22, 2017
Sheet 20 of 45

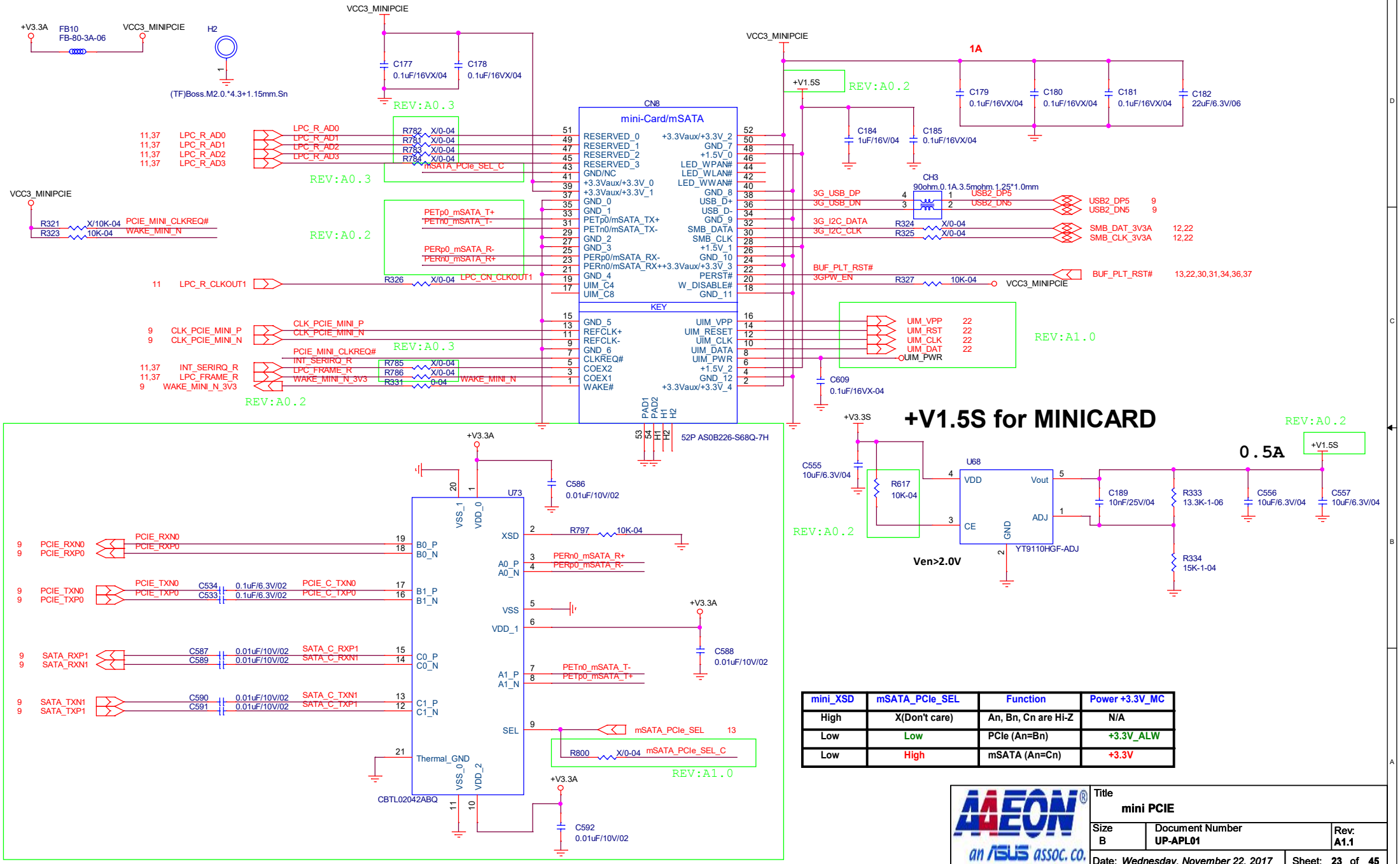


Title: eDP		
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 21 of 45	

M.2.2230/WiFi+BT/KeyID E
Intel AC8260 or AC3165

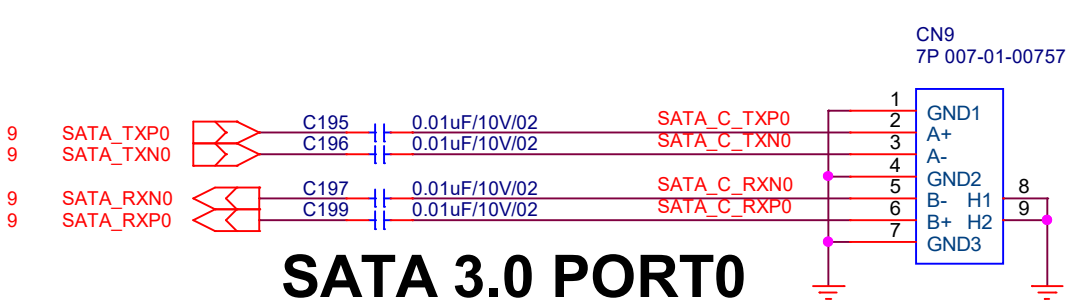


Title: M.2_2230_E-KEY			
Size: B	Document Number: UP-APL01	Rev: A1.1	
Date: Wednesday, November 22, 2017	Sheet: 22 of 45		

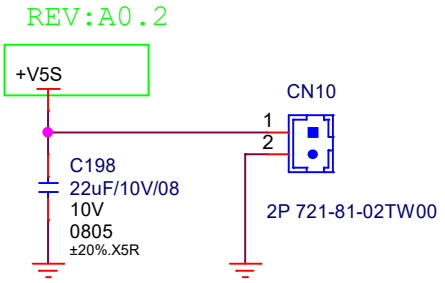


mini_XSD	mSATA_PCIe_SEL	Function	Power +3.3V_MC
High	X(Don't care)	An, Bn, Cn are Hi-Z	N/A
Low	Low	PCIe (An=Bn)	+3.3V_ALW
Low	High	mSATA (An=Cn)	+3.3V

AAEON an ASUS assoc. co.	Title: mini PCIE		
	Size: B	Document Number: UP-APL01	Rev: A1.1
	Date: Wednesday, November 22, 2017	Sheet: 23 of 45	

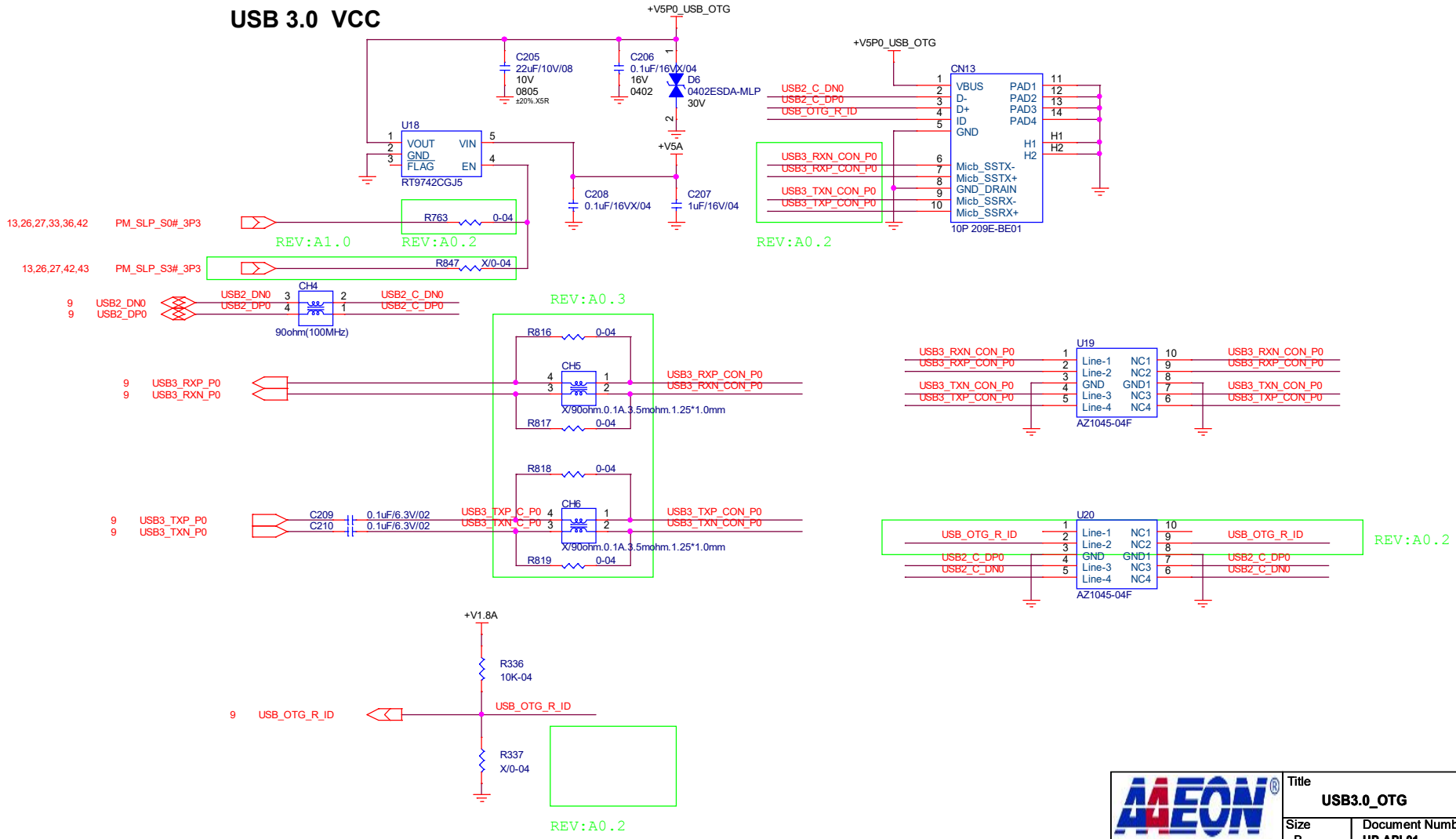


SATA 3.0 PORT0

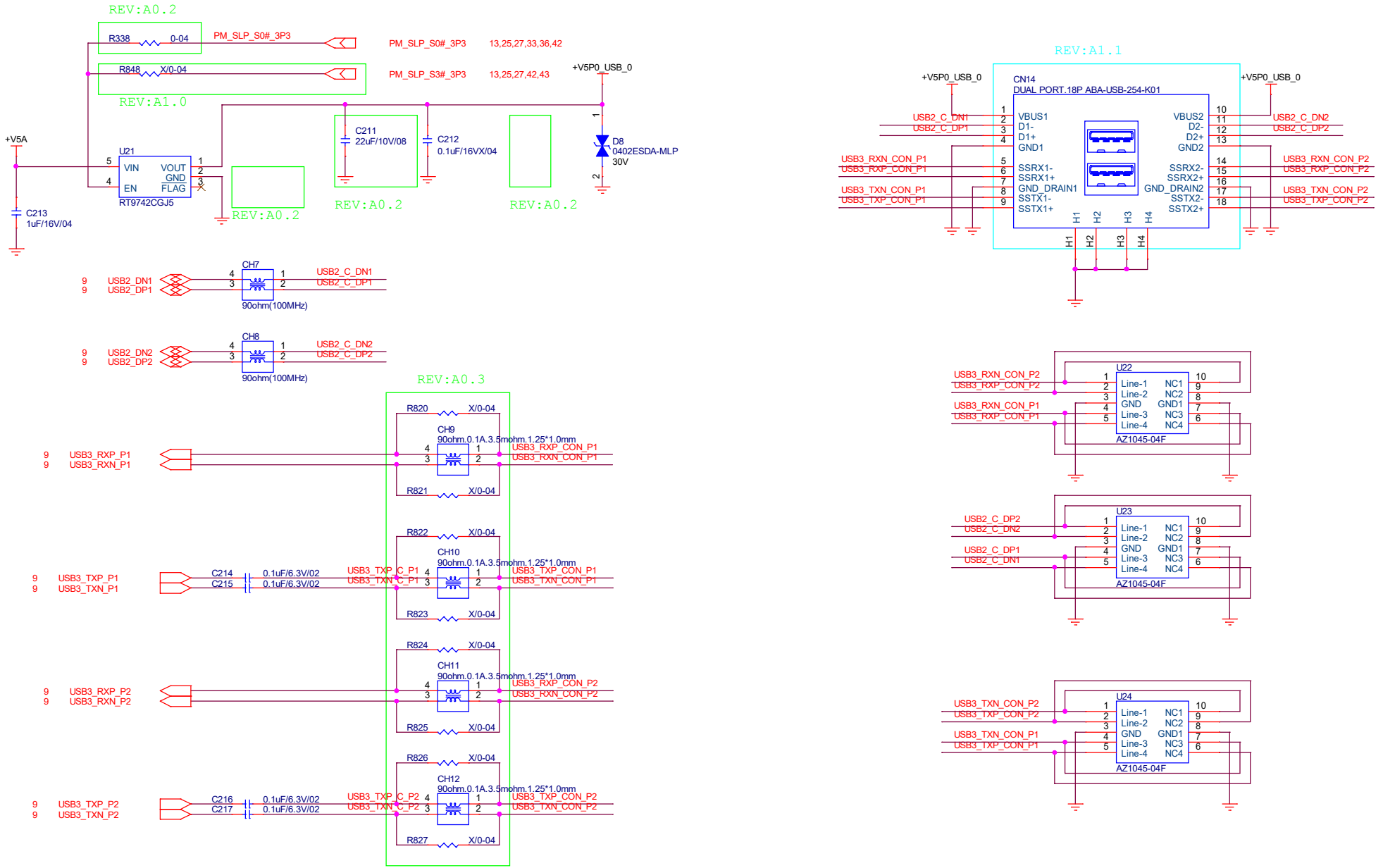


AAEON an ASUS assoc. co.	Title: **SATA**	
Size: A	Document Number: **UP-APL01**	Rev: **A1.1**
Date: *Wednesday, November 22, 2017*	Sheet: **24** of **45**	

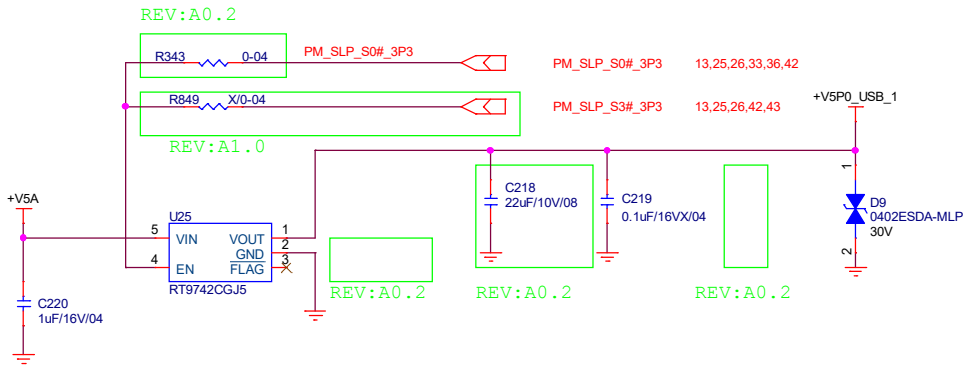
USB 3.0 VCC

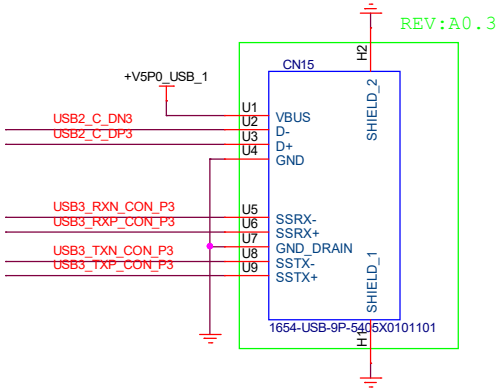


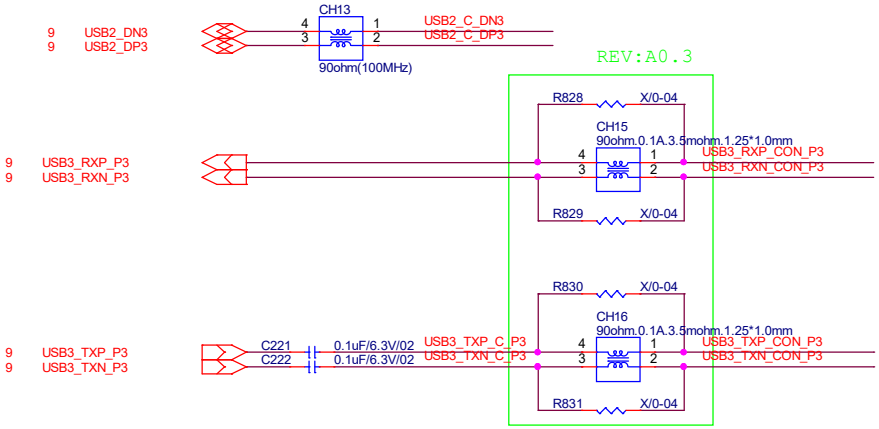
AAEON an ASUS assoc. co.	Title: USB3.0_OTG	
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 25 of 45	

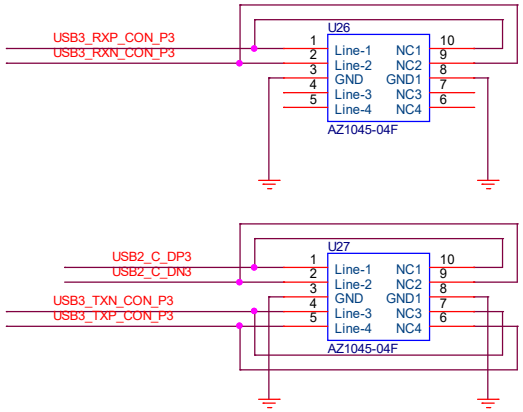


AAEON an ASUS assoc. co.	Title: USB3.0_TYPE-A (1/2)	
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 26 of 45	

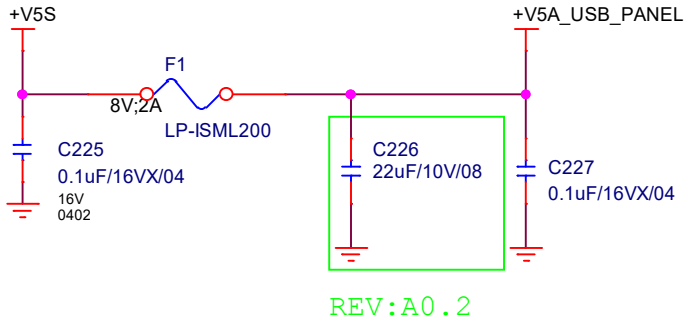


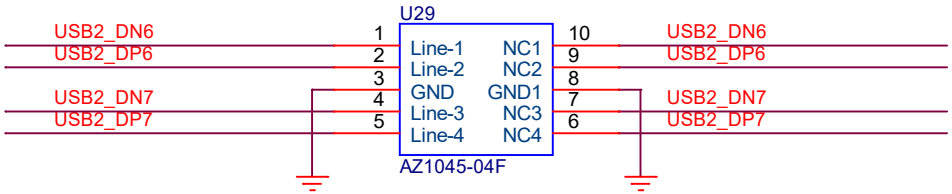


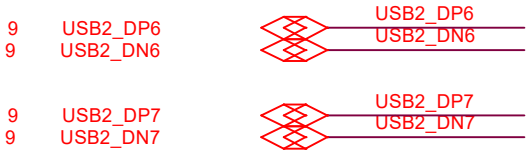


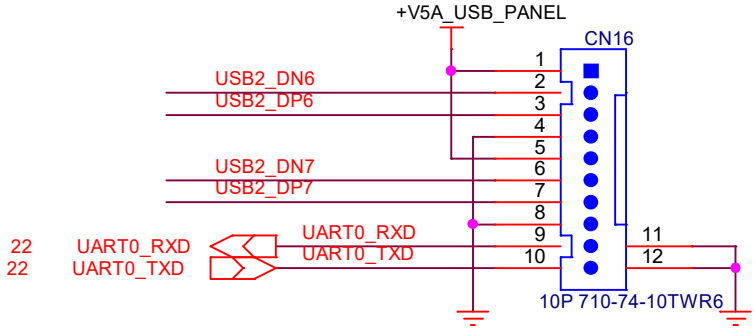


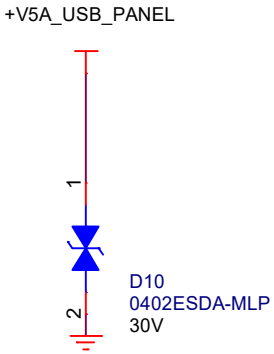
Title: USB3.0_TYPE-A (2/2)		
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 27 of 45	









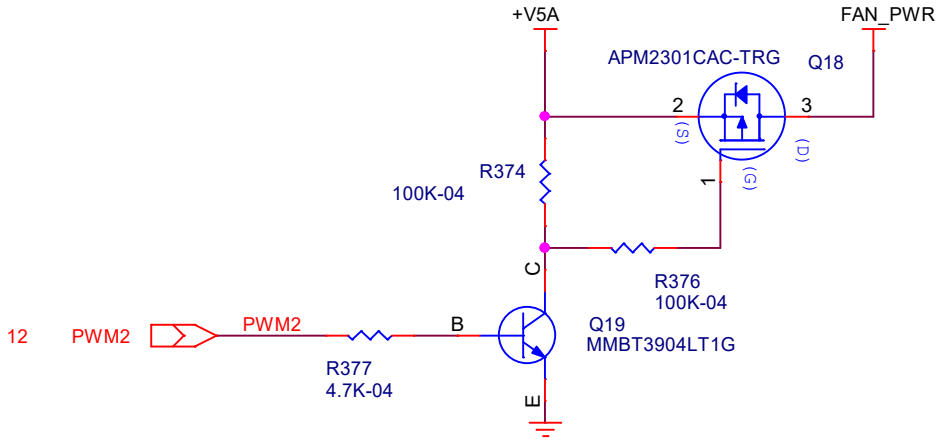


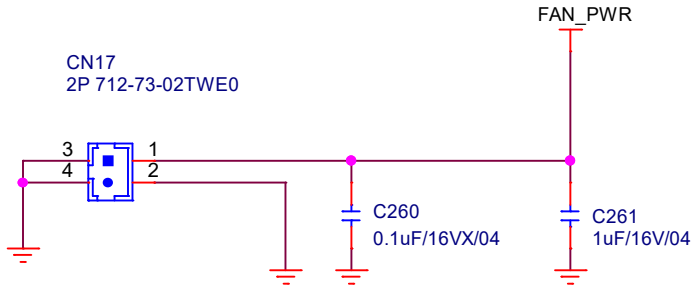
AAEON an ASUS assoc. co.

Title
USB PIN HEADER

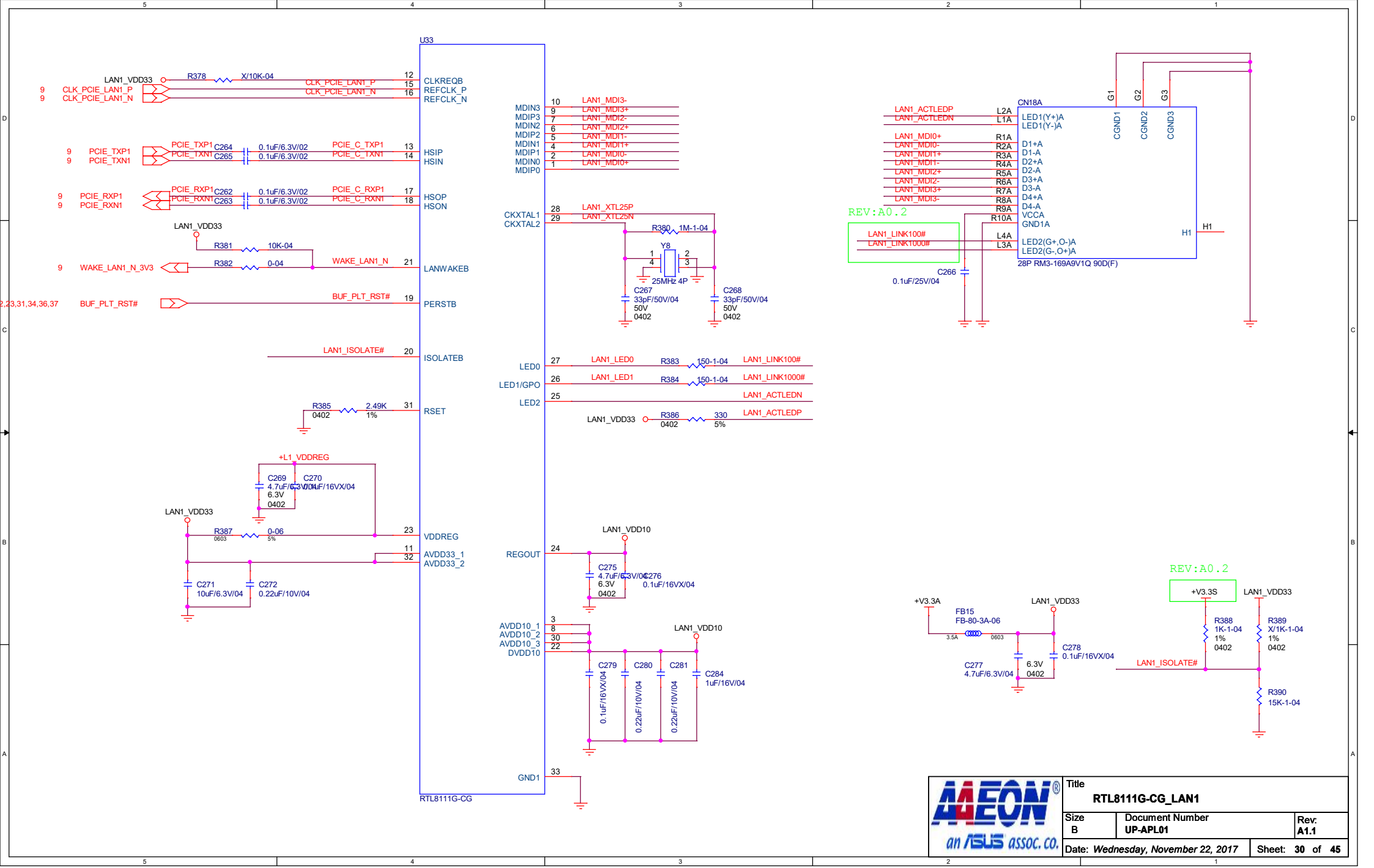
Size	Document Number	Rev:
A	**UP-APL01**	**A1.1**

Date: *Wednesday, November 22, 2017* Sheet: **28** of **45**

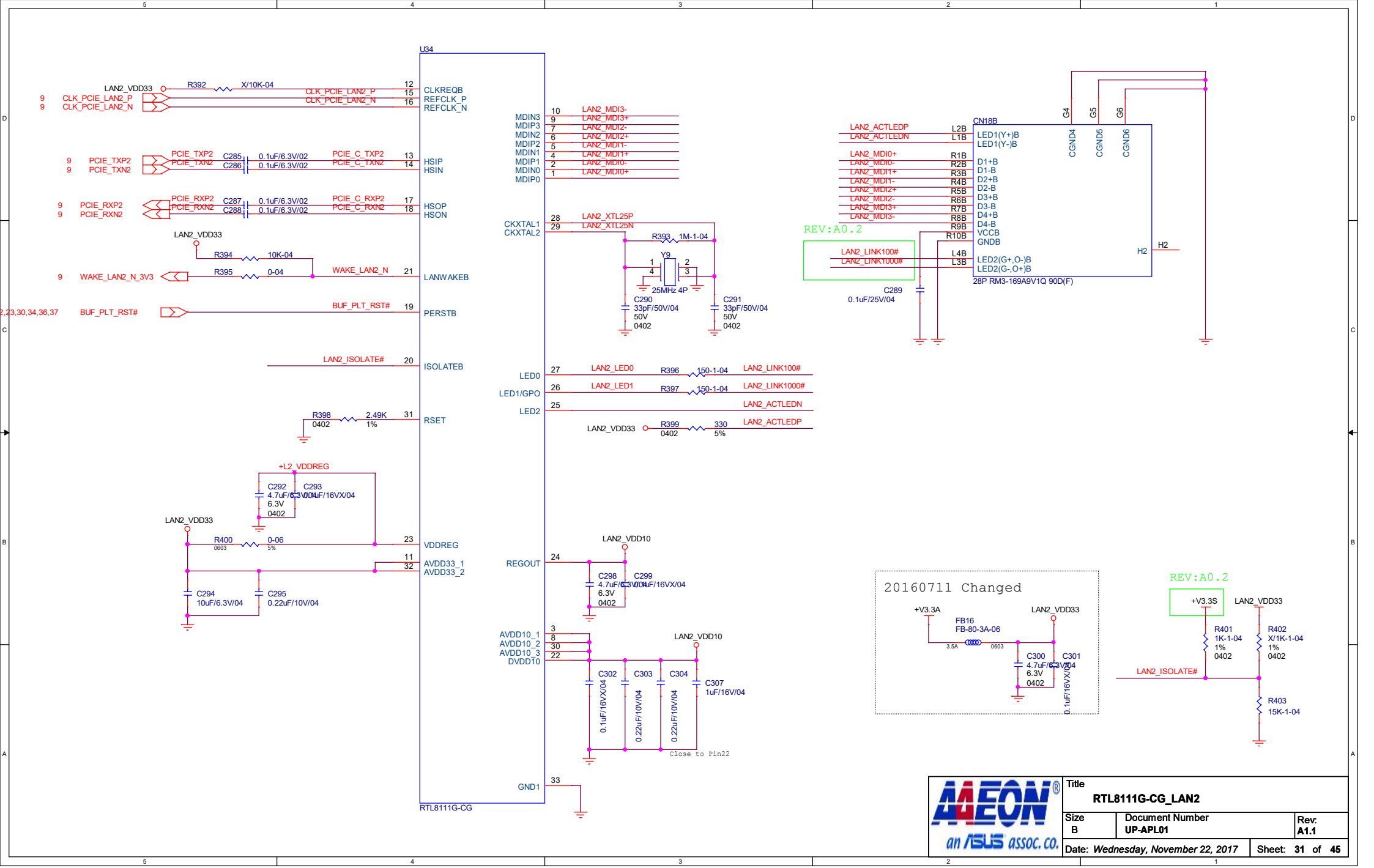




Title: **FAN**		
Size: A	Document Number: **UP-APL01**	Rev: **A1.1**
Date: *Wednesday, November 22, 2017*	Sheet: **29** of **45**	

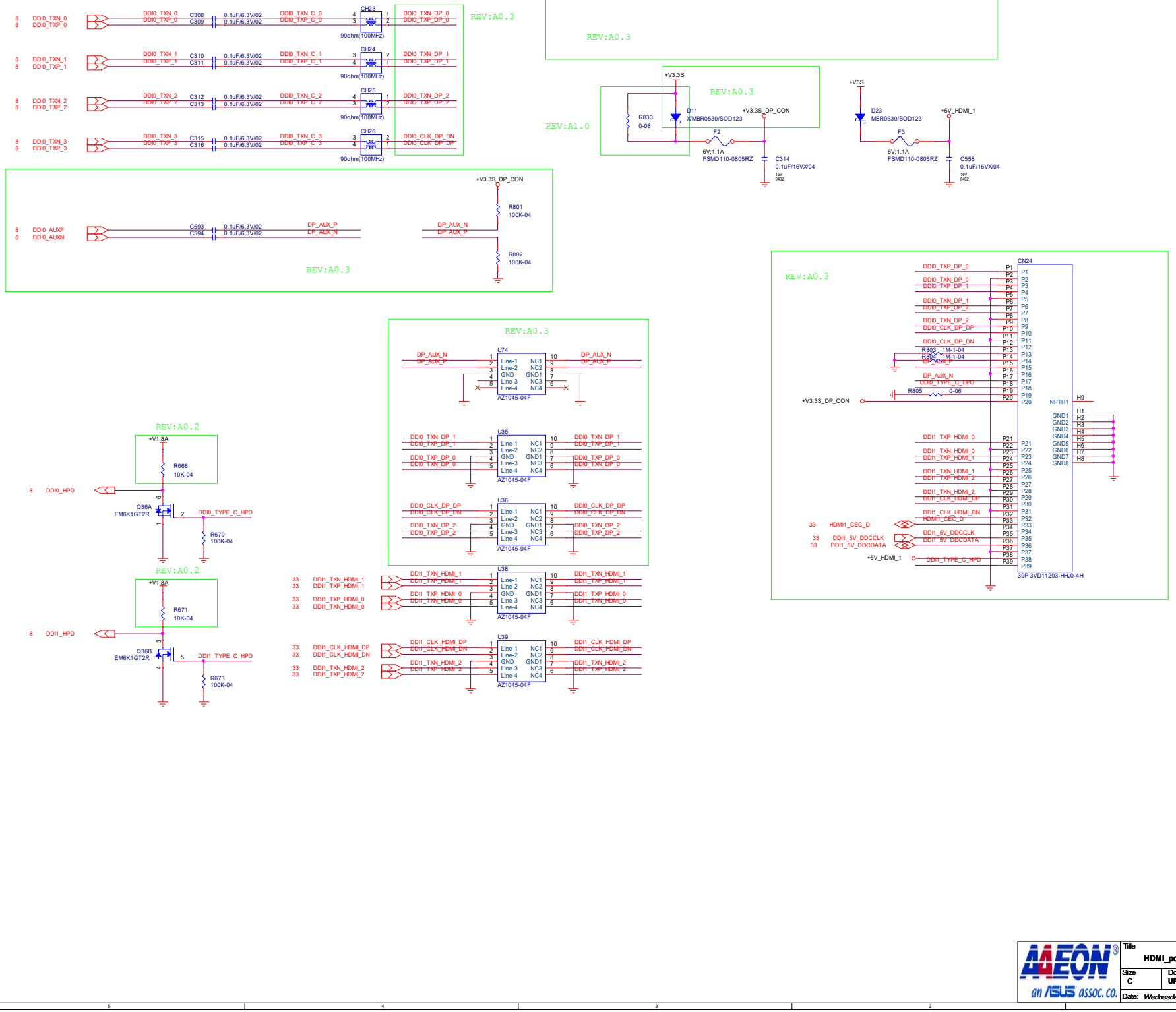


Title: RTL8111G-CG_LAN1		
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 30 of 45	



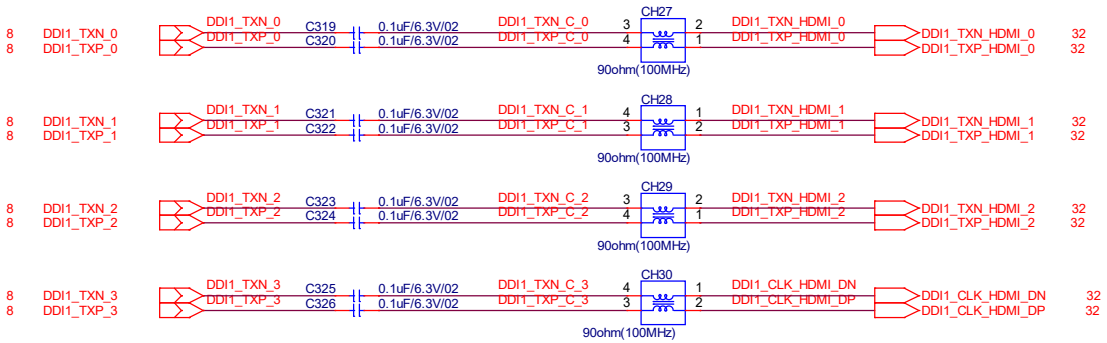
Title	RTL8111G-CG_LAN2	
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 31 of 45	

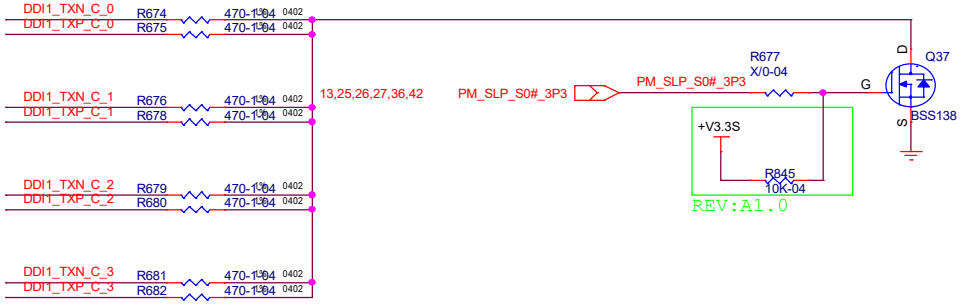
HDMI CHOKE SECTION



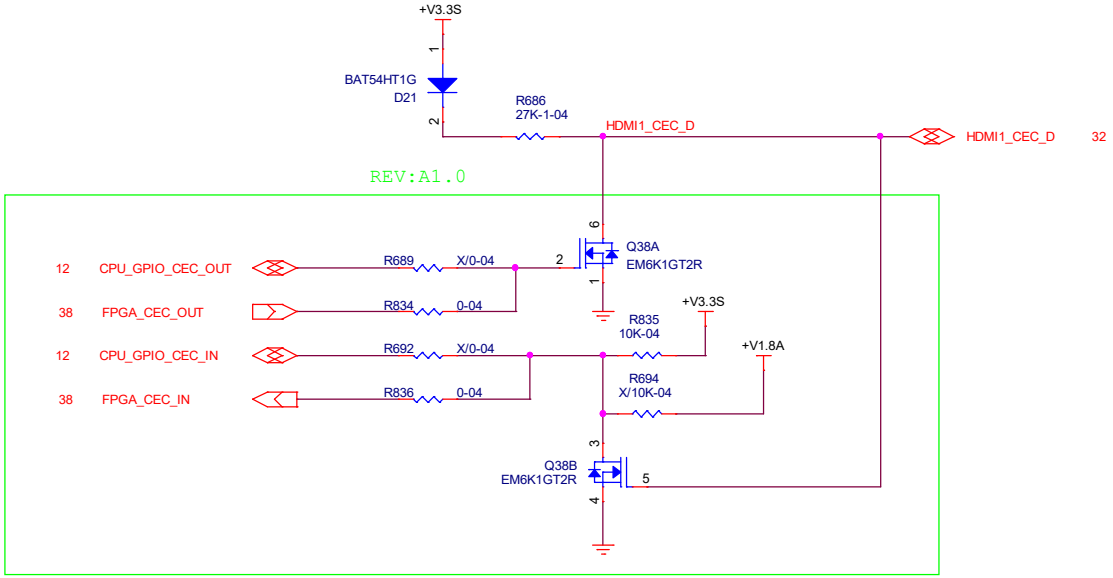
Title	HDMI_port0		
Size C	Document Number UP-APL01		Rev. A1.1
Date: Wednesday, November 22, 2017		Sheet: 32 of 45	

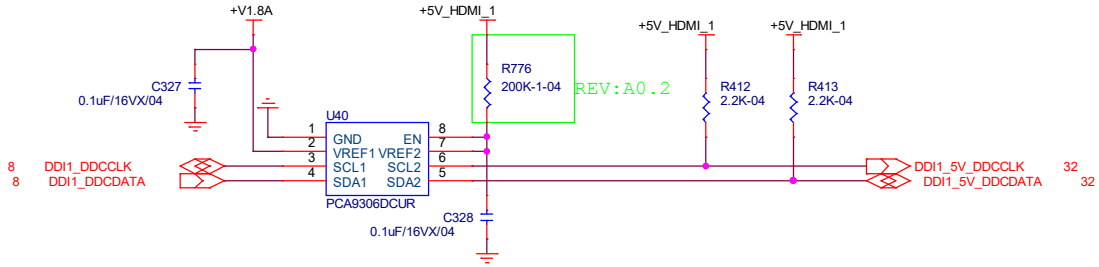
HDMI CHOKE SECTION





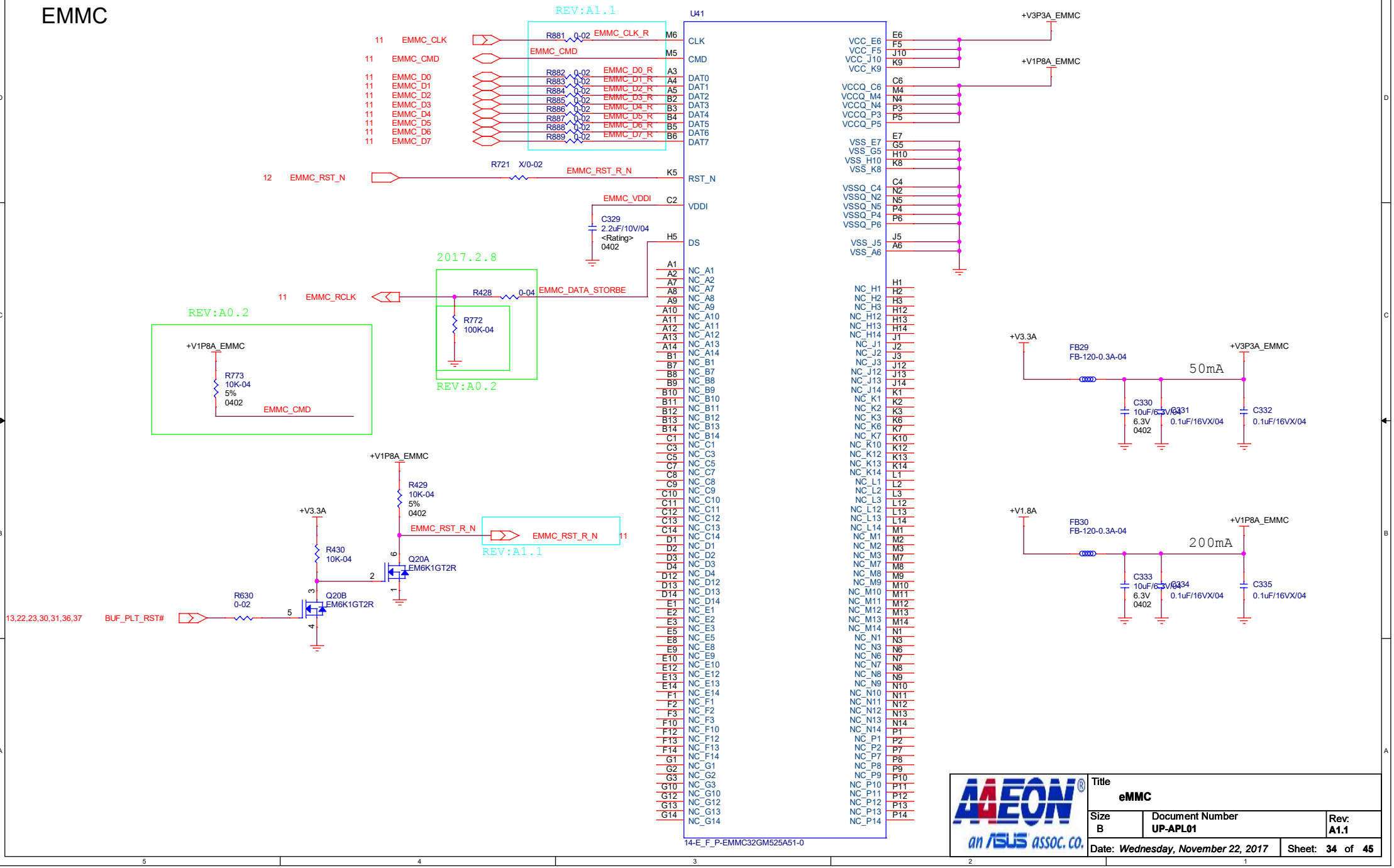
REV:A0.3



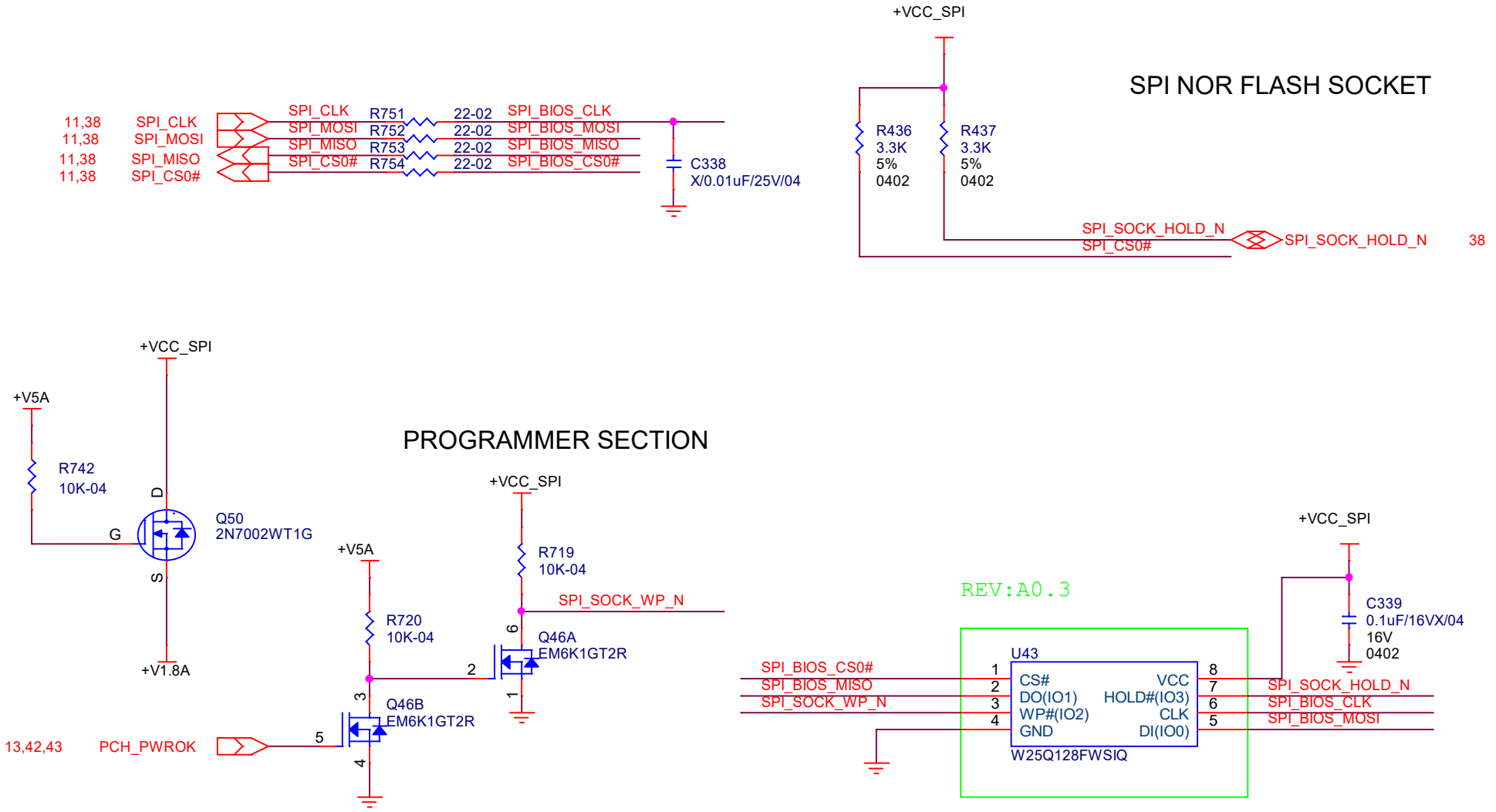


AAEON an ASUS assoc. co.	Title: HDMI_port1	
	Size: B	Document Number: UP-APL01 / Rev: A1.1
	Date: Wednesday, November 22, 2017	Sheet: 33 of 45

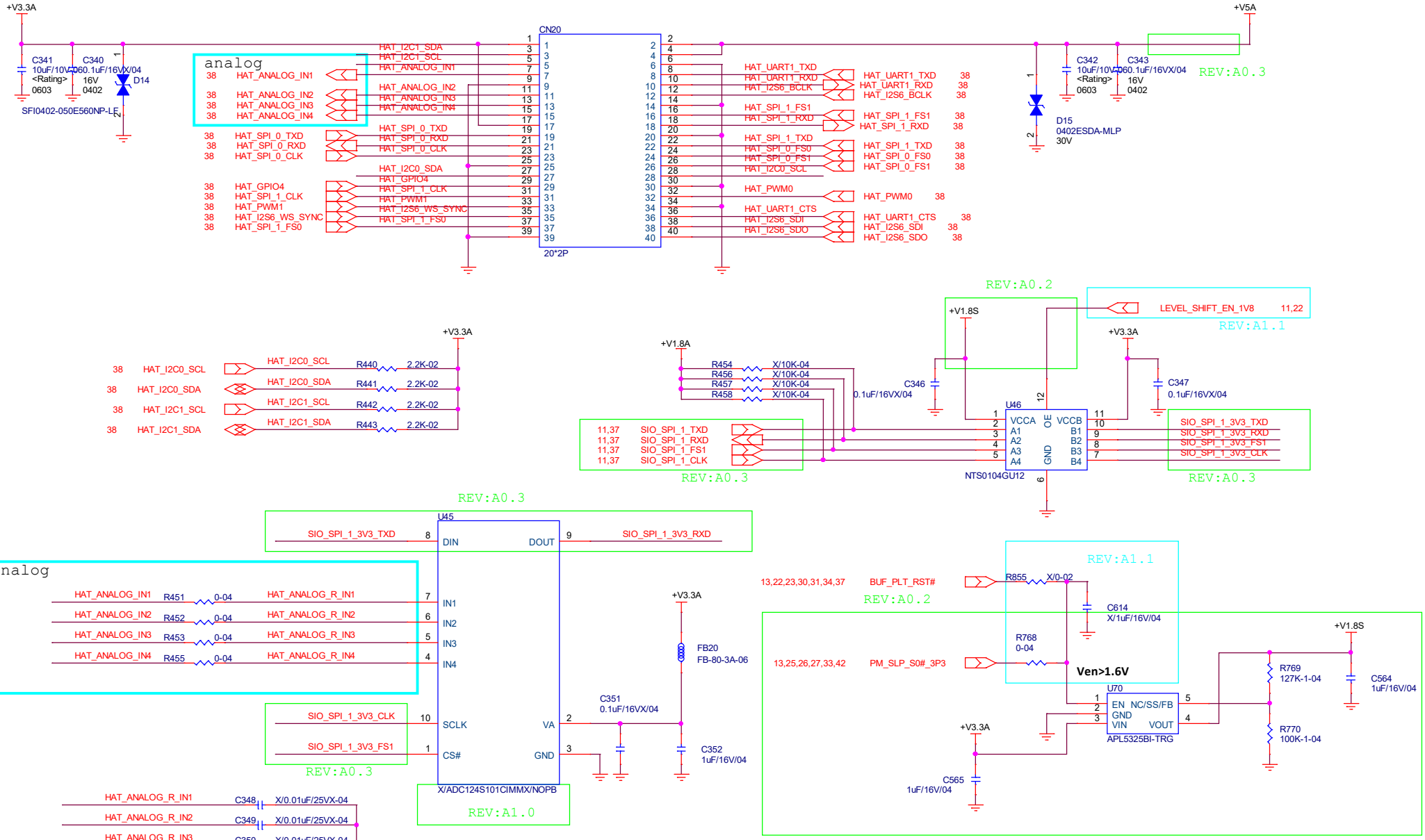
EMMC



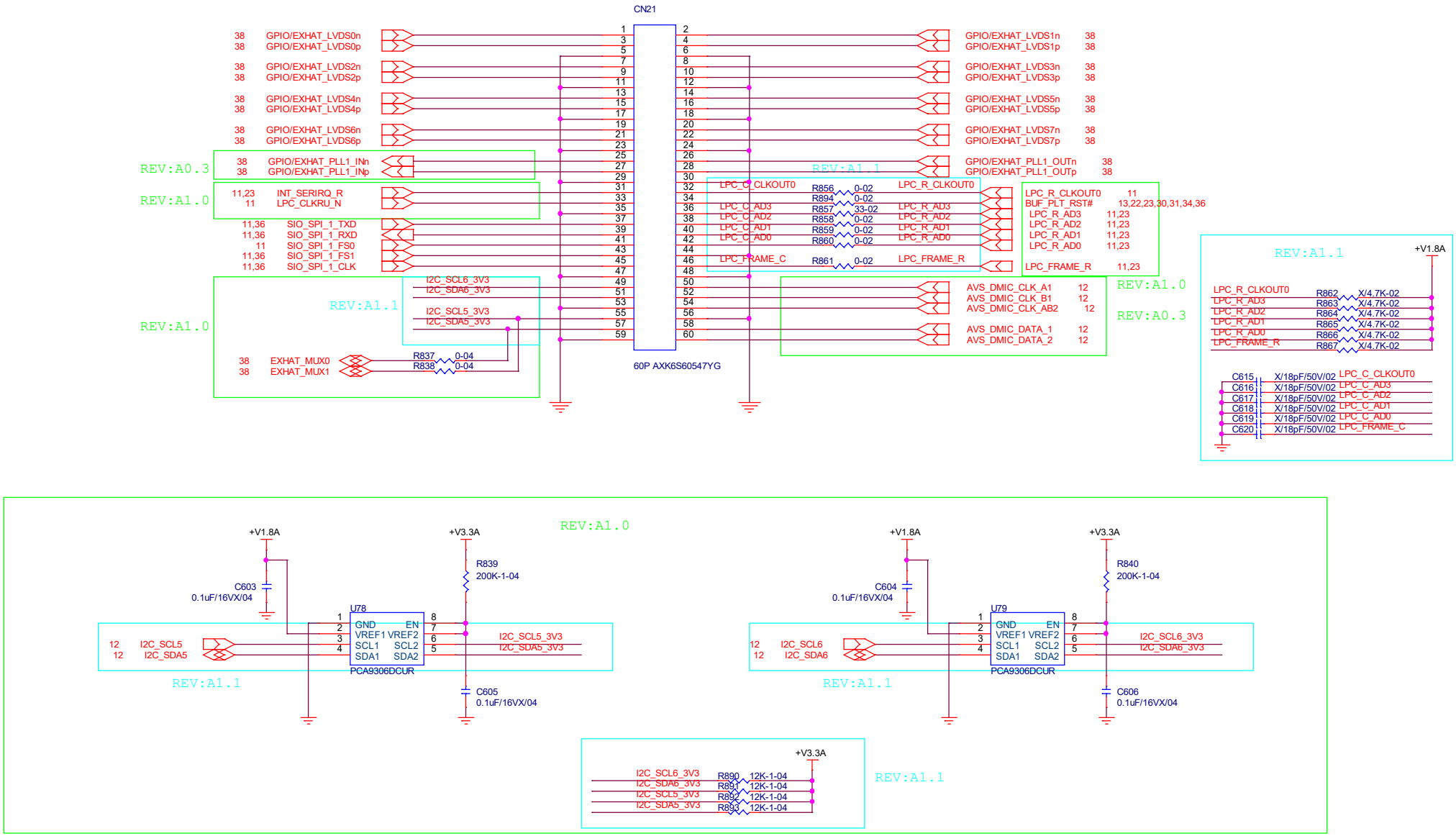
Title: eMMC		
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 34 of 45	



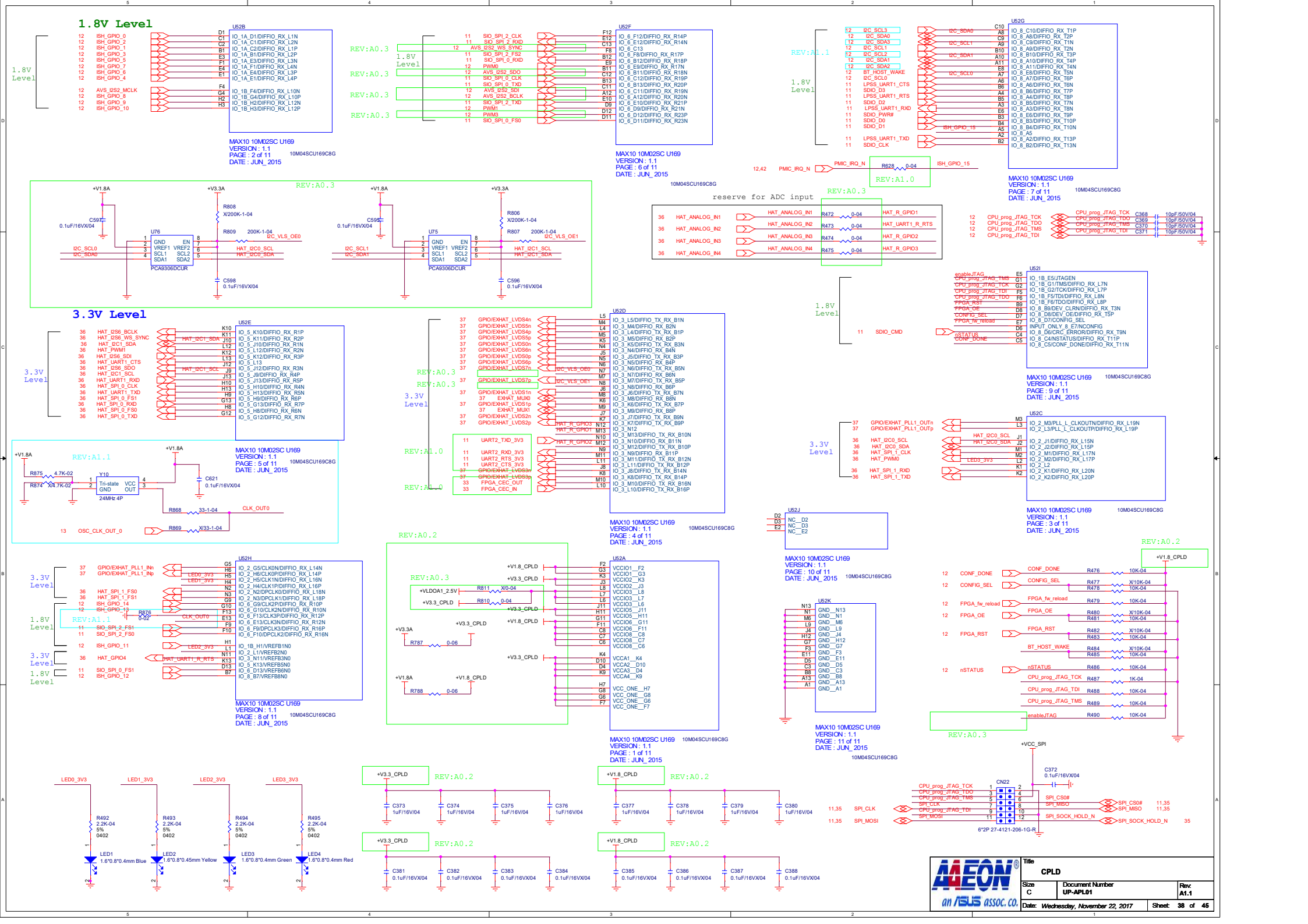
AAEON an ASUS assoc. co.	Title: **SPI flash**	
Size: A	Document Number: **UP-APL01**	Rev: **A1.1**
Date: *Wednesday, November 22, 2017*	Sheet: **35** of **45**	



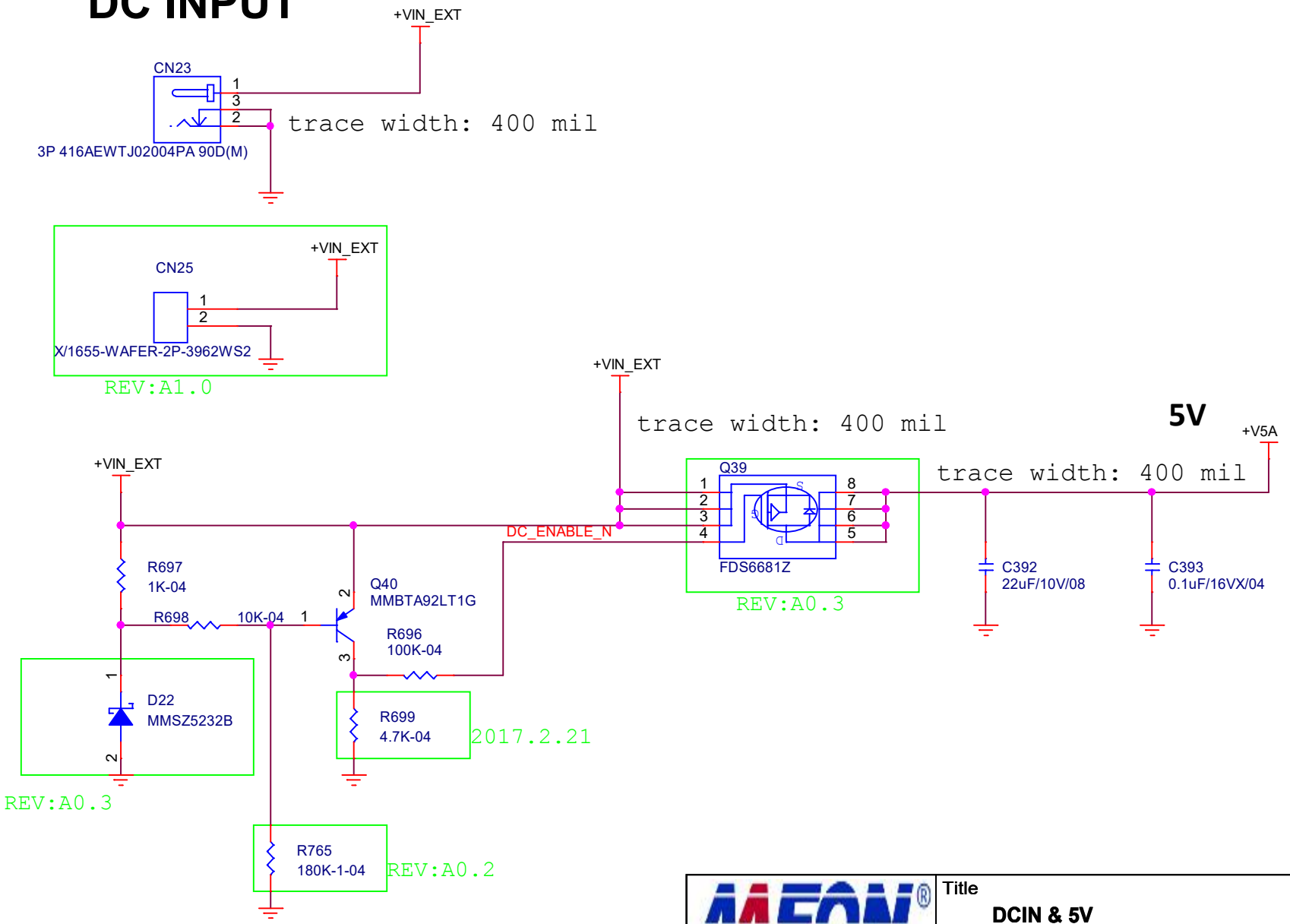
AAEON an ASUS assoc. co.	Title: HAT	
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: Wednesday, November 22, 2017	Sheet: 36 of 45	



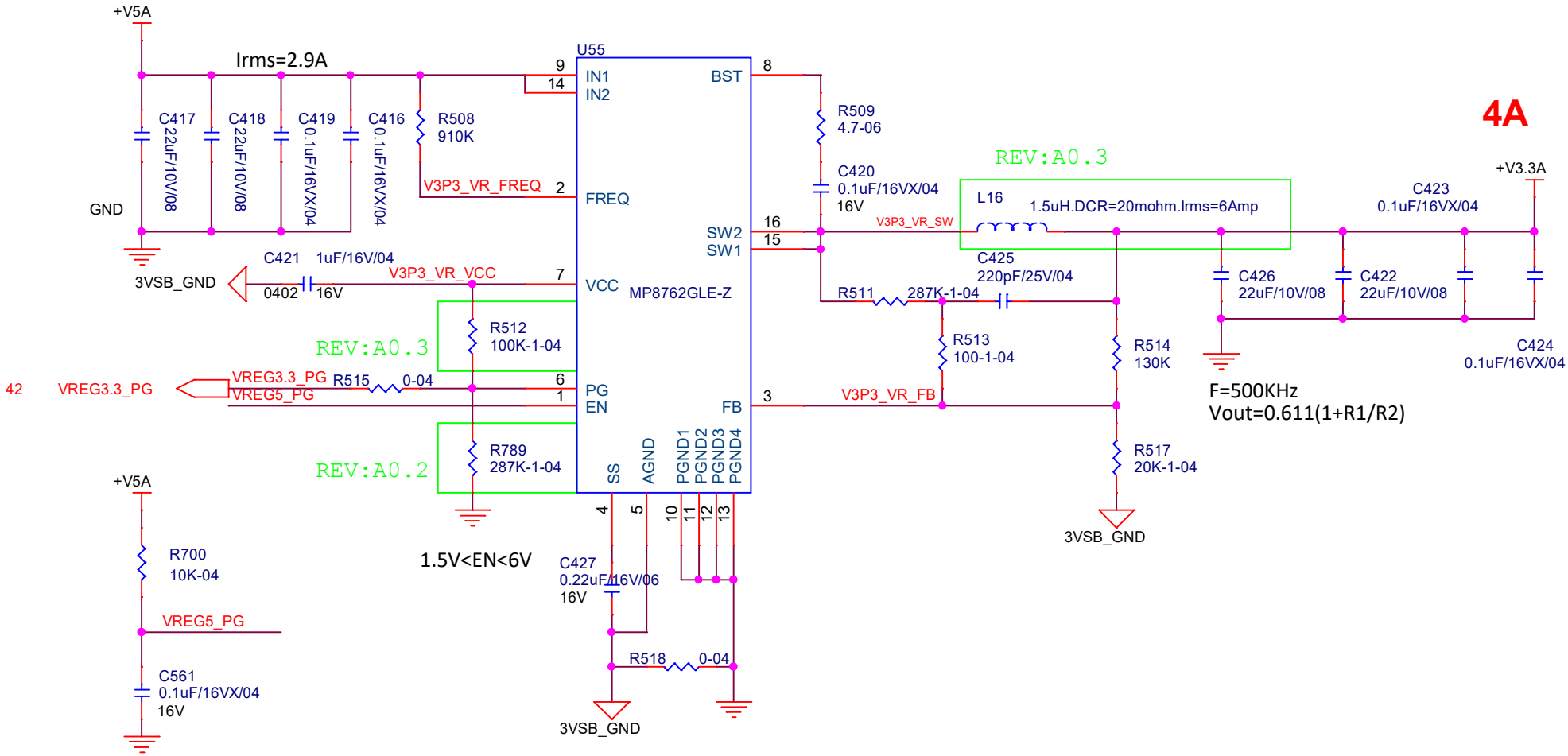
AAEON an ASUS assoc. co.	Title: EXHAT	
Size: B	Document Number: UP-APL01	Rev: A1.1
Date: *Wednesday, November 22, 2017*	Sheet: 37 of 45	


1.8V Level
U52B
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 2 of 11
DATE : JUN_ 2015
10M04SCU169C8G
REV:A0.3
U52F
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 6 of 11
DATE : JUN_ 2015
REV:A1.1
U52G
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 7 of 11
DATE : JUN_ 2015
PMIC_IRQ_N
R628 0-04
ISH_GPIO_15
REV:A1.0
reserve for ADC input
HAT_ANALOG_IN1
HAT_ANALOG_IN2
HAT_ANALOG_IN3
HAT_ANALOG_IN4
R472 0-04
R473 0-04
R474 0-04
R475 0-04
HAT_R_GPIO1
HAT_UART1_R_RTS
HAT_R_GPIO2
HAT_R_GPIO3
CPU_prog_JTAG_TCK
CPU_prog_JTAG_TDO
CPU_prog_JTAG_TMS
CPU_prog_JTAG_TDI
C368 10pF/50V/04
C369 10pF/50V/04
C370 10pF/50V/04
C371 10pF/50V/04
U76
U75
PCA9306DCUR
R808 X/200K-1-04
R809 200K-1-04
R806 X/200K-1-04
R807 200K-1-04
I2C_VLS_OE0
I2C_VLS_OE1
HAT_I2C0_SCL
HAT_I2C0_SDA
HAT_I2C1_SCL
HAT_I2C1_SDA
C597 0.1uF/16V/X04
C598 0.1uF/16V/X04
C595 0.1uF/16V/X04
C596 0.1uF/16V/X04
3.3V Level
U52E
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 5 of 11
DATE : JUN_ 2015
U52D
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 4 of 11
DATE : JUN_ 2015
U52I
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 9 of 11
DATE : JUN_ 2015
U52C
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 3 of 11
DATE : JUN_ 2015
U52J
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 10 of 11
DATE : JUN_ 2015
U52K
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 11 of 11
DATE : JUN_ 2015
REV:A1.1
Y10
24MHz 4P
R875 4.7K-02
R874 4.7K-02
C621 0.1uF/16V/X04
R868 33-1-04
R869 X33-1-04
CLK_OUT0
OSC_CLK_OUT_0
U52H
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 8 of 11
DATE : JUN_ 2015
REV:A0.2
U52A
MAX10 10M02SC U169
VERSION : 1.1
PAGE : 1 of 11
DATE : JUN_ 2015
+VLDOA1_2.5V
R811 X/0-04
R810 0-04
R787 0-06
R788 0-06
CONF_DONE
CONFIG_SEL
FPGA_fw_reload
FPGA_OE
FPGA_RST
BT_HOST_WAKE
nSTATUS
CPU_prog_JTAG_TCK
CPU_prog_JTAG_TDI
CPU_prog_JTAG_TMS
enableJTAG
R476 10K-04
R477 X/10K-04
R478 10K-04
R479 10K-04
R480 X/10K-04
R481 10K-04
R482 X/10K-04
R483 10K-04
R484 X/10K-04
R485 10K-04
R486 10K-04
R487 1K-04
R488 10K-04
R489 10K-04
R490 10K-04
LED0_3V3
LED1_3V3
LED2_3V3
LED3_3V3
R492 2.2K-04 5% 0402
R493 2.2K-04 5% 0402
R494 2.2K-04 5% 0402
R495 2.2K-04 5% 0402
LED1 1.6*0.8*0.4mm Blue
LED2 1.6*0.8*0.45mm Yellow
LED3 1.6*0.8*0.4mm Green
LED4 1.6*0.8*0.4mm Red
C373 1uF/16V/04
C374 1uF/16V/04
C375 1uF/16V/04
C376 1uF/16V/04
C377 1uF/16V/04
C378 1uF/16V/04
C379 1uF/16V/04
C380 1uF/16V/04
C381 0.1uF/16V/X04
C382 0.1uF/16V/X04
C383 0.1uF/16V/X04
C384 0.1uF/16V/X04
C385 0.1uF/16V/X04
C386 0.1uF/16V/X04
C387 0.1uF/16V/X04
C388 0.1uF/16V/X04
CN22
6*2P 27-4121-206-1G-R
C372 0.1uF/16V/X04
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_SOCK_HOLD_N
AAEON
an ASUS assoc. co.
Title
CPLD
Size C
Document Number UP-APL01
Rev. A1.1
Date: Wednesday, November 22, 2017
Sheet: 38 of 45

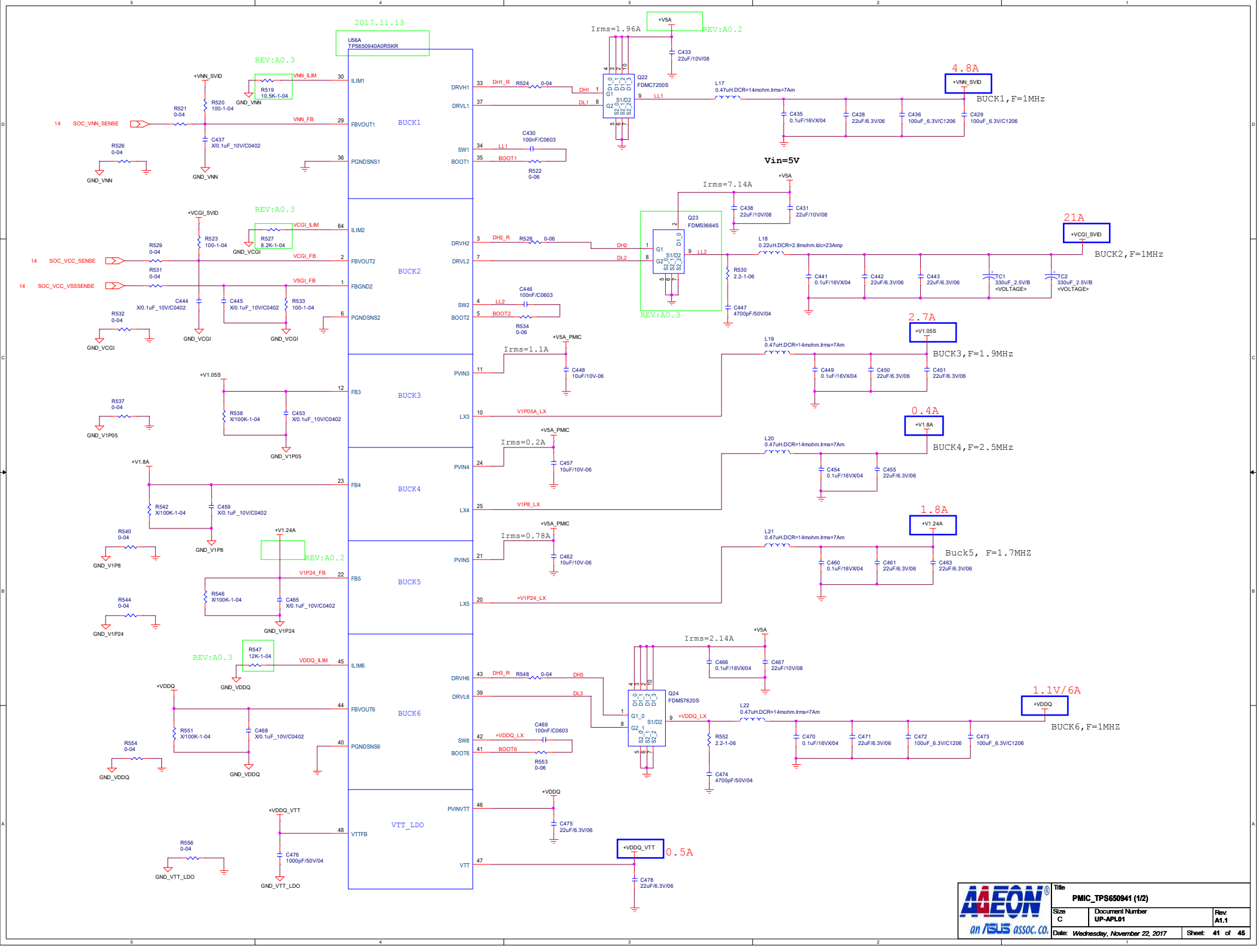
DC INPUT



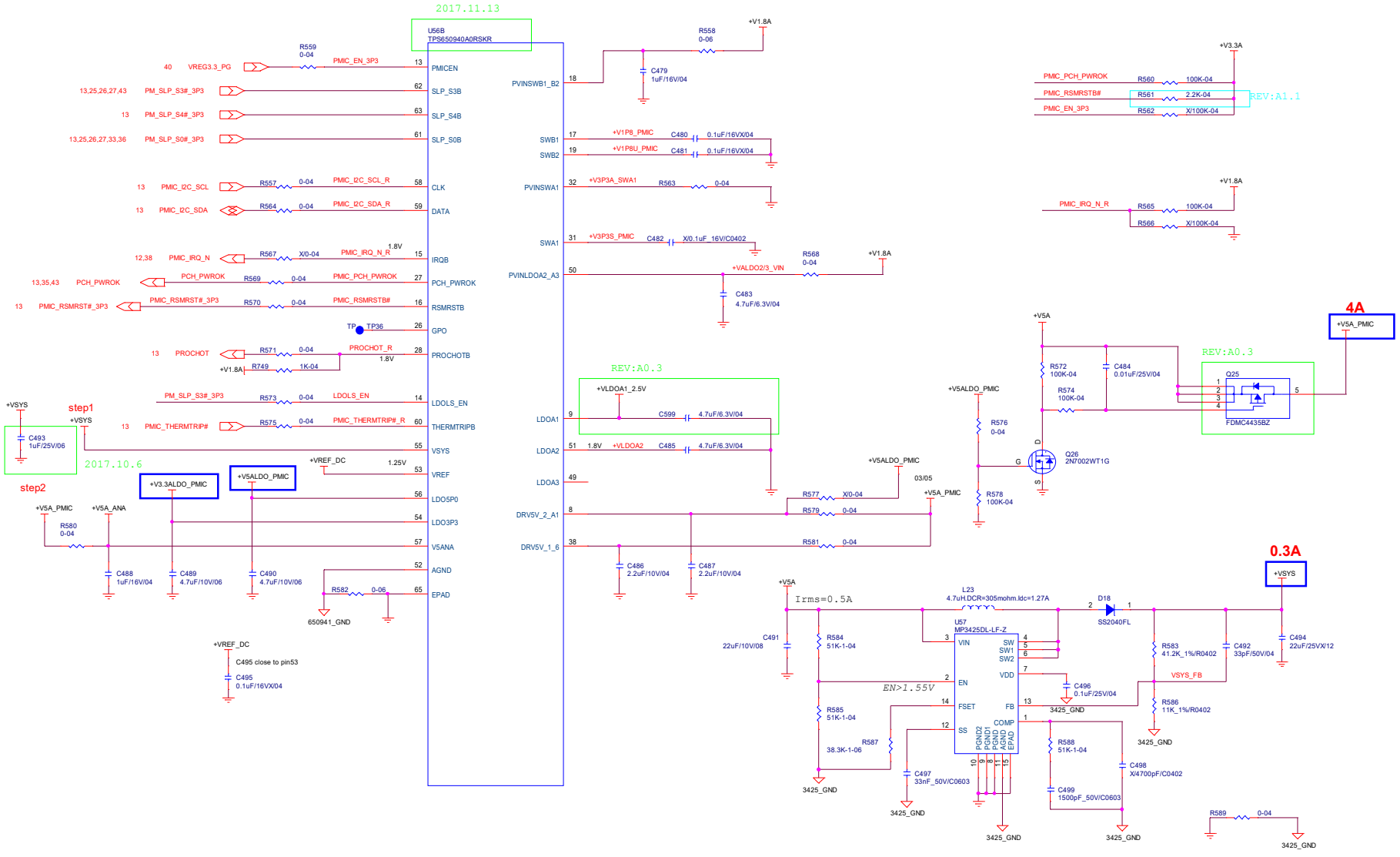
AAEON an ASUS assoc. co.	Title: **DCIN & 5V**	
Size: A	Document Number: **UP-APL01**	Rev: **A1.1**
Date: *Wednesday, November 22, 2017*	Sheet: **39** of **45**	



AAEON an ASUS assoc. co.	Title: 3.3V	
Size: A	Document Number: UP-APL01	Rev: A1.1
Date: *Wednesday, November 22, 2017*	Sheet: 40 of 45	



Title	PMIC_TPS650941 (1/2)
Size	C
Document Number	UP-APL01
Rev.	A1.1
Date:	Wednesday, November 22, 2017
Sheet:	41 of 45



Title	PMIE_TPS650941 (2/2)		
Size C	Document Number UP-APL01		Rev. A1.1
Date: Wednesday, November 22, 2017		Sheet: 42 of 45	

REV:A0.2

+V5A

FDMC4435BZ

+V5S

C562

0.1uF/16VX/04

R590
10K-04

R591

10K-04

Q27

C500
22uF/25VX/12

13,25,26,27,42 PM_SLP_S3#_3P3

PM_SLP_S3#_3P3 G

Q28
2N7002WT1G

+V3.3A

+V3.3S

FDMC4435BZ

+V3.3S

R798
2.2K-04

C563

0.1uF/16VX/04

R594
10K-04

R595

10K-04

Q29

C501
22uF/6.3V/06

LED5
1.6*0.8*0.4mm Blue

REV:A1.0

PCH_PWROK

R846
X/0-04

Q51
X/2N7002WT1G

R815
0-04

PM_SLP_S3#_3P3 G

Q30
2N7002WT1G

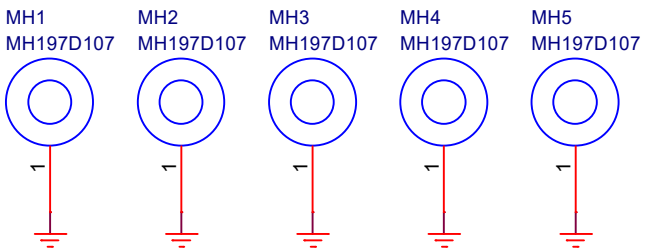
AAEON an ASUS assoc. co.

Title
System Power

Size	Document Number	Rev:
A	**UP-APL01**	**A1.1**

Date: *Wednesday, November 22, 2017* Sheet: **43** of **45**

SCREW HOLE

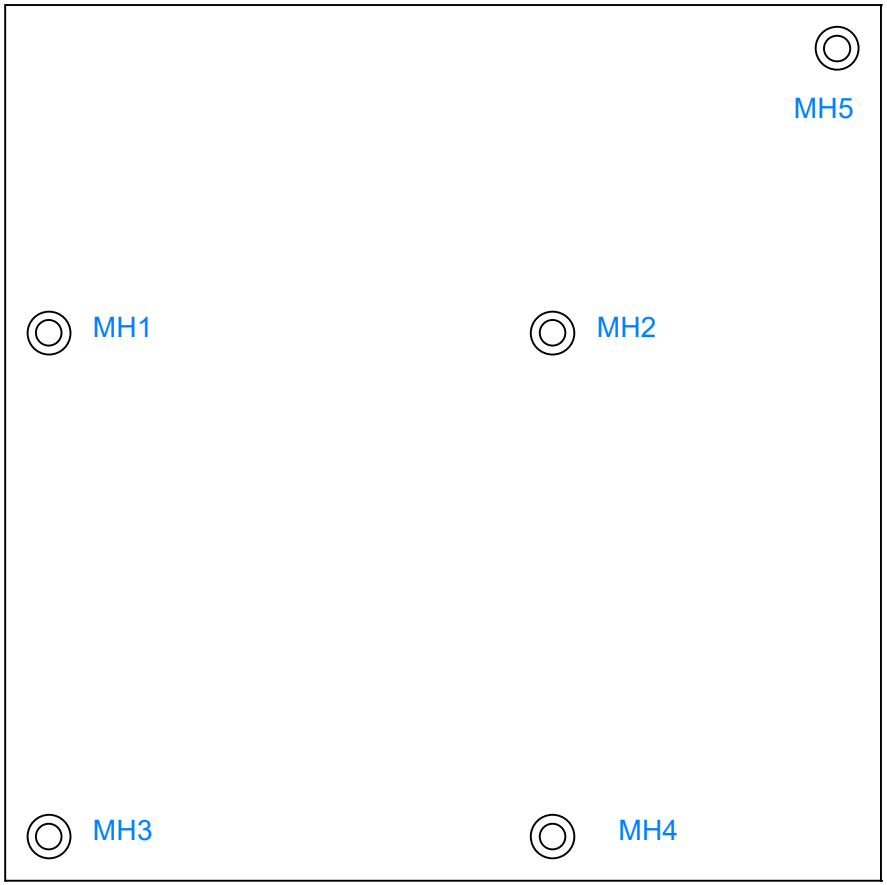


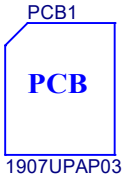
MOUNT HOLE

REAR CAM BOSS

FRONT CAM BOSS

Buttom View





AAEON an ASUS assoc. co.

Title
Mechanical C omponent

Size	Document Number	Rev:
A	**UP-APL01**	**A1.1**

Date: *Wednesday, November 22, 2017* Sheet: **44** of **45**

HISTORY

DATE	Revision	Description
2016.10.19	A02	1. Add LPDDR4 x2 on page 7,18,19.
		2. Remove R47 and R46,R75,R78,R67,R728 mount on page 11,12.
		3. R178 Change to 10K on page 13.
		4. VCCIOA Change to +VDDQ on page 14.
		5. Remove VDDQ resistor on page 16,17.
		6. Add HPD pull high resistor on page 21,32.
		7. Add DDI0_BKLTEN and DDI0_VDDEN pull down resistor on page 21.
		8. Add U16, U37 and U40 enable pin of pull high resistor on page 21,32.
		9. Change I2C_3V3_SCL7 of pull high resistor connect to +V3.3A on page 21.
		10. CN6 power Change to +V3.3A on page 21.
		11. U69 and U46 power Change to +V1.8S on page 22,36.
		12. Add LPC resistor on page 23.
		13. CN15 change to SMD package on page 27.
		14. Add EMMC_ CMO pull high resistor on page 34.
		15. Add R765 for over voltage protection on page 39.
		16. R35,R36,R38,R40 change to 4,7K on page 9.
		17. Add DDR ID strap pin on page 12.
		18. Add SATA and PCIE control function pin on page 12,23.
		19. Add +V1,5S for mini card on page 23.
		20. SATA power change to +V5S on page 24.
		21. Swap USB3.0 signals on CN13 on page 25.
		22. C211,C218,C226 change to 22uF on page 26,27,28.
		23. Modify LAN LED signal on page 30,31.
		24. LAN ISOLATEB power change to +V3.3S on page 30,31.
		25. Remove SATA signal in CN21 on page 37.
		26. Add CPLD 1.8V and 3.3V bypass resistor on page 38.
		27. Add pull down resistor for VREG3.3_PG on page 40.
		28. Change Q22 high side power to +V5A on page 41.
		29. Modify +V5S and +V3.3S power switch circuit on page 43.

DATE	Revision	Description
2016.12.23	A03	1. Remove HDMI0 and add DP port on page 8,32.
		2. Add LPSS_UART1_TXD H/W strap pin of pull down resistor on page 11.
		3. Add enableJTAG control by SOC on page 12.
		4. Add power LED control by SUS_STAT# on page 13,43.
		5. Add Mini SATA & Mini PCIE of select pin on page 13,23.
		6. Add USB3.0 bypass resistor on page 25,26.
		7. Change CN15 to DIP package on page 27.
		8. Add U45 CS control pin by ISH_GPIO_2 on page 36.
		9. Remove GPIO/EXHAT_LVDS8n/p on page 37.
		10. Add I2C0 and I2C1of level shift IC on page 38.
		11. Add +VLDOA1_2.5V for CPLD on page 38,42.
		12. Change Q39 to FDS6681Z on page 39.
		13. Change D22 to MMSZ5232B on page 39.
		14. Change L16 package on page 40.
		15. Change Q23 to FDMS3664S on page 41.
		16. Change Q25 to FDMC4435BZ on page 42.
		17. Remove UART2 and add SIO_SPI1,PMW3,DMIC,I2S6 CPLD JTAG on page 11,12,37,38.
		18. Change R519,R527,R547 value for OCP on page 41.
2017.03.29	A10	1. Change HDMI_CEC control by FPGA on page 12,33,38.
		2. Add UART2 bus connect to FPGA on page 11,38.
		3. Delete SD Card function on page 11.
		4. Remove R800 and control by BIOS on page 23.
		5. Add R833 for DP power on page 32.
		6. Add I2C level shift for EXHAT on page 37.
		7. Change LPC bus connect to EXHAT on page 37.
		8. R628 mount for ISH_GPIO_15 on page 38.
		9. Change LPC to 1.8V mode on page 11.
		10. Add UIM bus on page 22,23.
2017.04.20	A10	11. Add DC wafer on page 39.
		12. Reserved PM_SLP_S3#_3P3 control for USB power on page 25,26,27.
2017.10.13	A11	1. Add reset for 2M camera on page 8,20.
		2. U77 mounted on page 11.
		3. Add BOARD_ID_BIT2 on page 12.
		4. Add WIFI_M2_RST# for WIFI on page 12,22.
		5. Changed USB connector package on page 26.
		6. Modify OE pin of U77, U69, U46 by LEVEL_SHIFT_EN_1V8 on page 11,22,36.
		7. Swap I2C5 & 6 with I2C2 & 3 on page 37,38.
		8. Add resistor and Capacitance for LPC on page 37.
		9. Add OSC 24MHz for FPGA on page 38.
2017.11.22	A11	10. Changed pad of test point (TP63,TP64) on page 13.
		11. Add BUF_PLT_RST# on EXHAT on page 37.

AAEON an ASUS assoc. co.

Title: CHANGE_REVISION HISTORY

Size: Custom | Document Number: UP-APL01 | Rev: A1.1

Date: Wednesday, November 22, 2017 | Sheet: 45 of 45