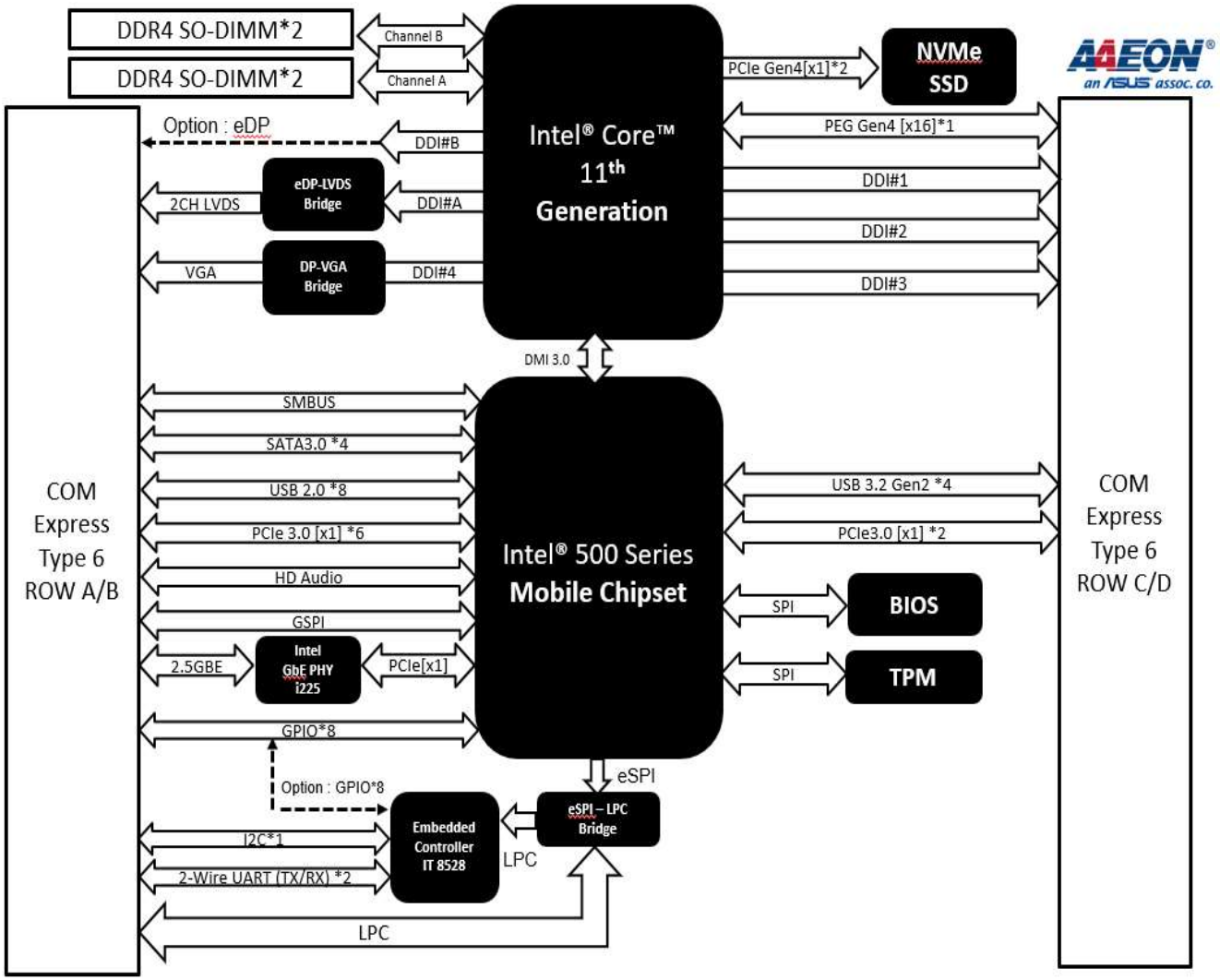
Project Name : COM-TGHB6
Project Number:
Version: A0.1_0_0



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<Variant Name>

AAEON Technology INC.

Title	Cover Sheet	
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
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CPU GPIO Pins :

Name	Power Well	Default	GPIO Function	Location
	+V3P3S	PD	DDI1_HPD	AE8
	+V3P3S	PD	DDI2_HPD	AH11
	+V3P3S	PD	DDI3_HPD	AK13
	+V3P3S	PD	DDI4_HPD	AK15
	+V3P3A	PU	USB2_OC3#	K46
	+V3P3A	PU	USB2_OC2#	K47
	+V3P3A	PU	USB2_OC1#	L45
	+V3P3A	PU	USB2_OC0#	L46
	+V3P3A	PU	SCI#	N46
	+V3P3A	PU	SMI#	M48

POWER :

Name		
LVDS	+V3P3S	200mA
LAN*1	+V3P3A	670mA
		0.87A

Name		
+VCCIN_AUX	+V5_DUAL	7.63A
+VCCIN AUX_PCH	+V5_DUAL	4.3A
+VDDQ_MEM	+V5_DUAL	3.12A
+VDDQ_VPP	+V3P3A	1A
+VCCIN	+V12S	12.5A
		28.55A

Name		
+VREG5	+V12S	6.87A
+V3P3A	+V5_DUAL	2A
+V1P8A	+V5_DUAL	1A
+V2P5S_SS	V5_DUAL	0.49A
+V1P0S_SS	V5_DUAL	0.36A
+V0P9S_SS	V5_DUAL	0.38A
		11.1A

EC GPIO Pins :

	Power Well	Default	GPIO Function	Location	Note
	+V3P3A	Input	I_RSMRST	J13	
	+V3P3A	Output	O_RSMRST	A1	When J13 active HIGH, then PU A1 after 10ms
	+V3P3S	Input	GPI0	N2	
	+V3P3S	Input	GPI1	A13	
	+V3P3S	Input	GPI2	A12	
	+V3P3S	Input	GPI3	B12	
	+V3P3S	Output	GPO0	A9	
	+V3P3S	Output	GPO1	B8	
	+V3P3S	Output	GPO2	A8	
	+V3P3S	Output	GPO3	B7	

PCH GPIO Pins :

	Power Well	Default	GPIO Function	Location	Note
	+V3P3A	Output	GPP_E4_CFG6	N47	
	+V3P3A	Output	GPP_E5_CFG5	M45	When J13 active HIGH, then PU A1 after 10ms
	+V3P3A	Input	GPP_R16_GPI0	BA48	co-lay EC GPIO_Default PCH
	+V3P3A	Input	GPP_R17_GPI1	BA45	co-lay EC GPIO_Default PCH
	+V3P3A	Input	GPP_R18_GPI	AY45	co-lay EC GPIO_Default PCH
	+V3P3A	Input	GPP_R19_GPI3	AW47	co-lay EC GPIO_Default PCH
	+V3P3A	Output	GPP_R11_GPO0	AV43	co-lay EC GPIO_Default PCH
	+V3P3A	Output	GPP_R13_GPO1	BC49	co-lay EC GPIO_Default PCH
	+V3P3A	Output	GPP_R14_GPO2	BB47	co-lay EC GPIO_Default PCH
	+V3P3A	Output	GPP_R15_GPO3	BA47	co-lay EC GPIO_Default PCH

SMBus/I2C Addresses :

Device	address
I225	0xC0h
PTN3460BS/IF6	0xC0h

PCB Footprints

MOSFET BJT

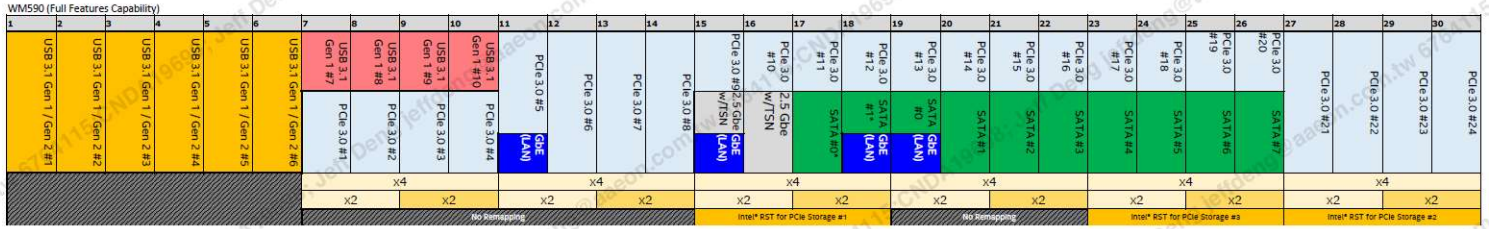
PCB STACK : HDI

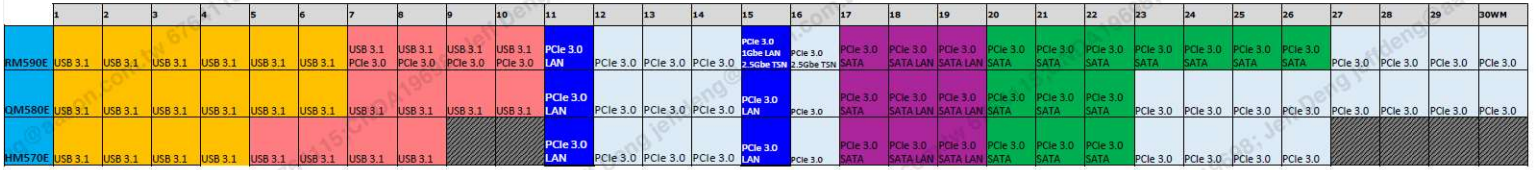
Board: FR4
Impedence: 50ohm +/-10%
Thickness: 2.0mm +-10%

- Layer 1 : Component (Top)
- Layer 2 : GND (GND1)
- Layer 3 : Signal (IN1)
- Layer 4 : GND (GND2)
- Layer 5 : Signal (IN2)
- Layer 6 : GND (GND3)
- Layer 7 : Signal (IN3)
- Layer 8 : POWER (VCC1)
- Layer 9 : POWER (VCC2)
- Layer 10 : Signal (IN4)
- Layer 11 : GND (GND4)
- Layer 12 : Signal (IN5)
- Layer 13 : GND (GND5)
- Layer 14 : Signal (IN6)
- Layer 15 : GND (GND6)
- Layer 16 : Component (Bot)

PCH HSIO

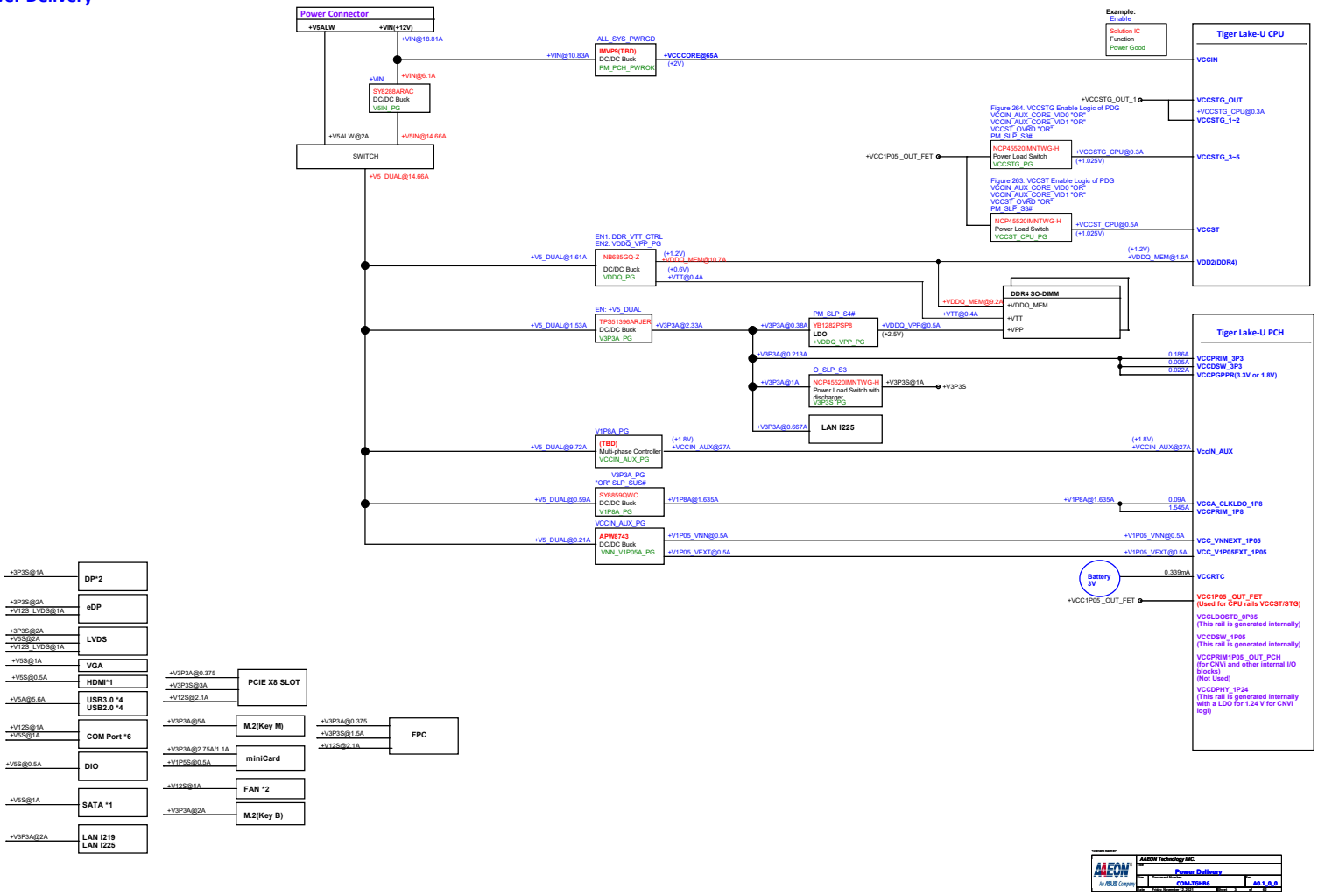
PROPOSED HSIO LANE ASSIGNMENTS – TIGER LAKE PCH-H



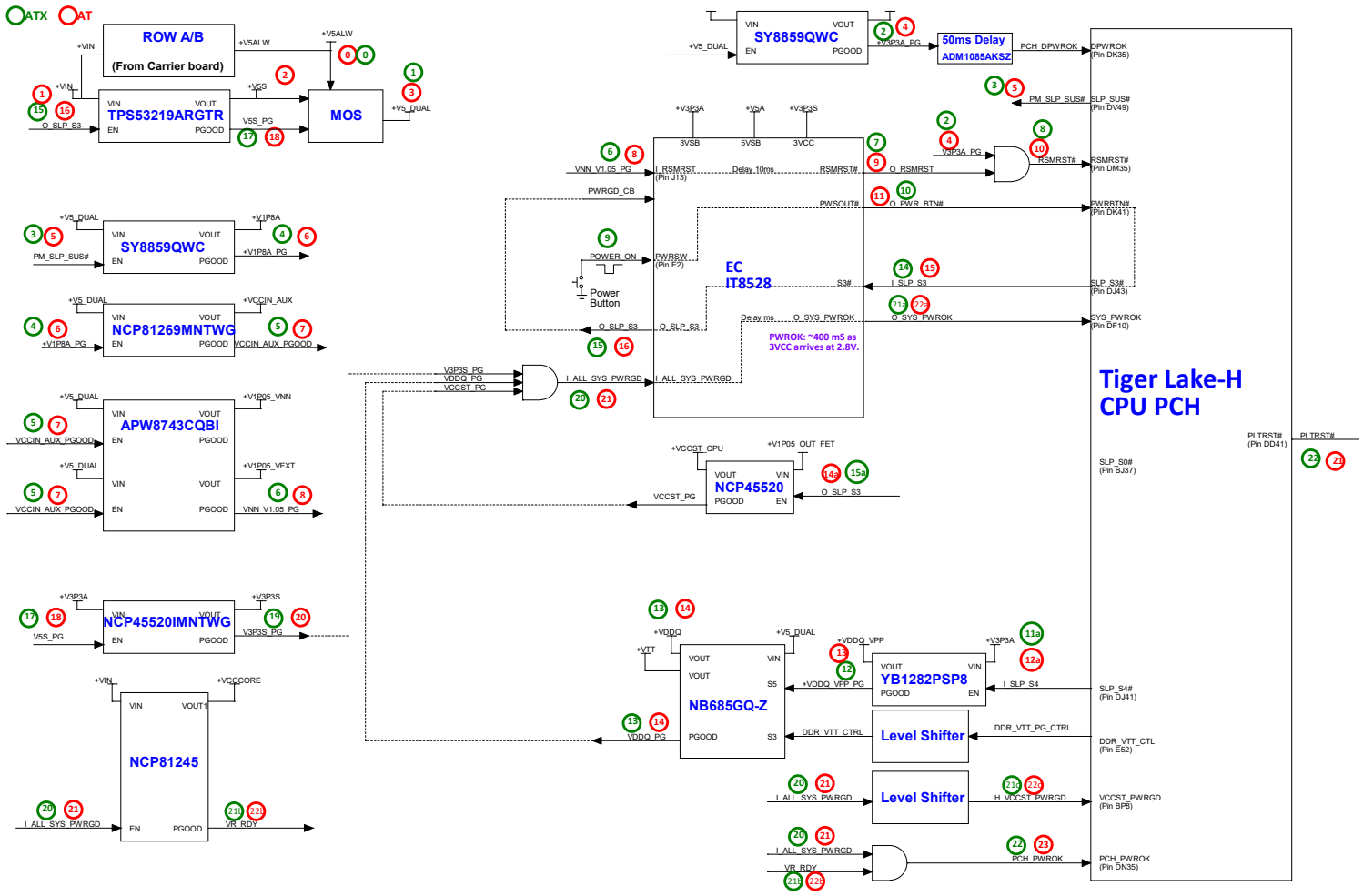


The number of HSIO remain same as Comet Lake; Pin locations and Mux options optimized to Tiger Lake program

Power Delivery



Power Sequence



<Variant Name>

AAEON Technology INC.

Title	Power Sequence	
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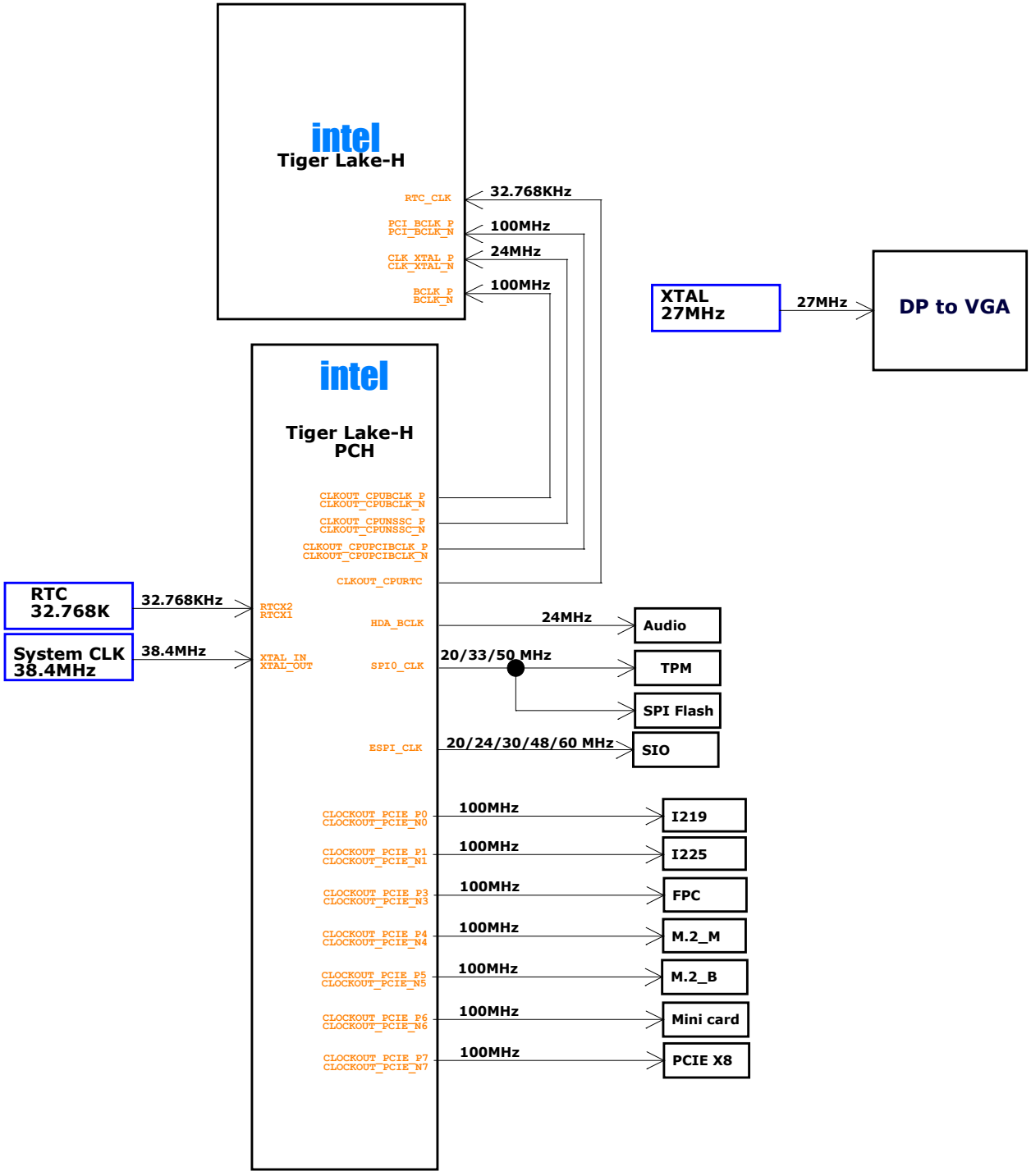
CLK Tree



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AAEON Technology INC.

Title	CLK Tree	
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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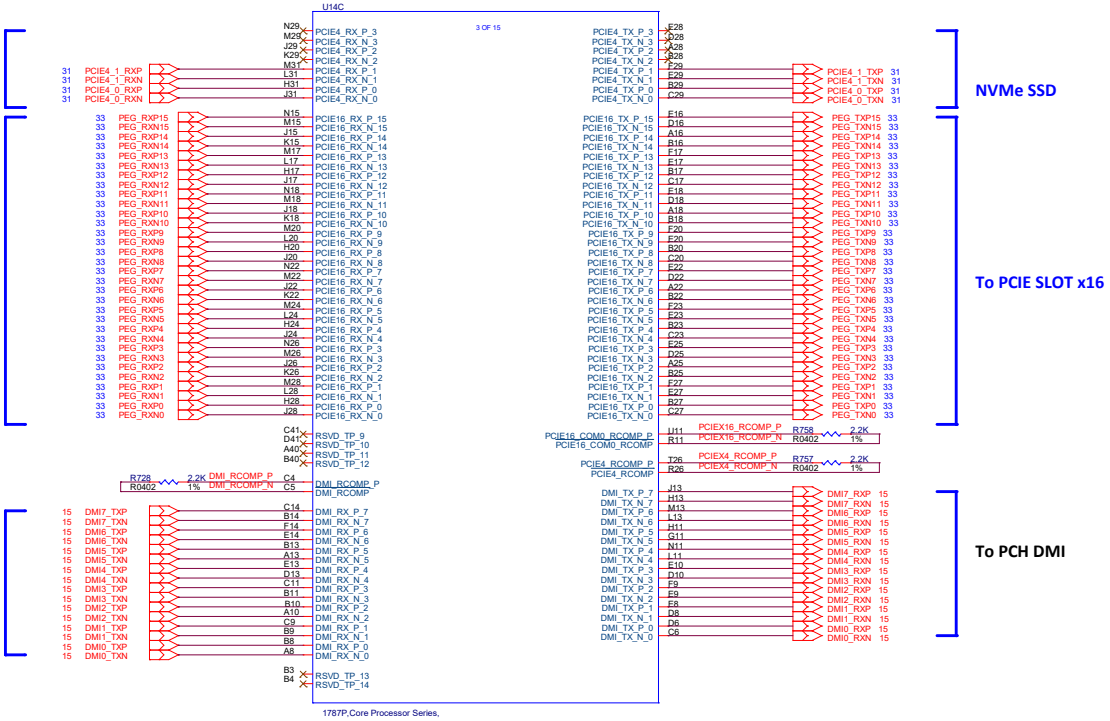
CPU_DMI/PEG



<Variant Name>

AAEON Technology INC.

Title: CPU_DMI/PEG

Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0

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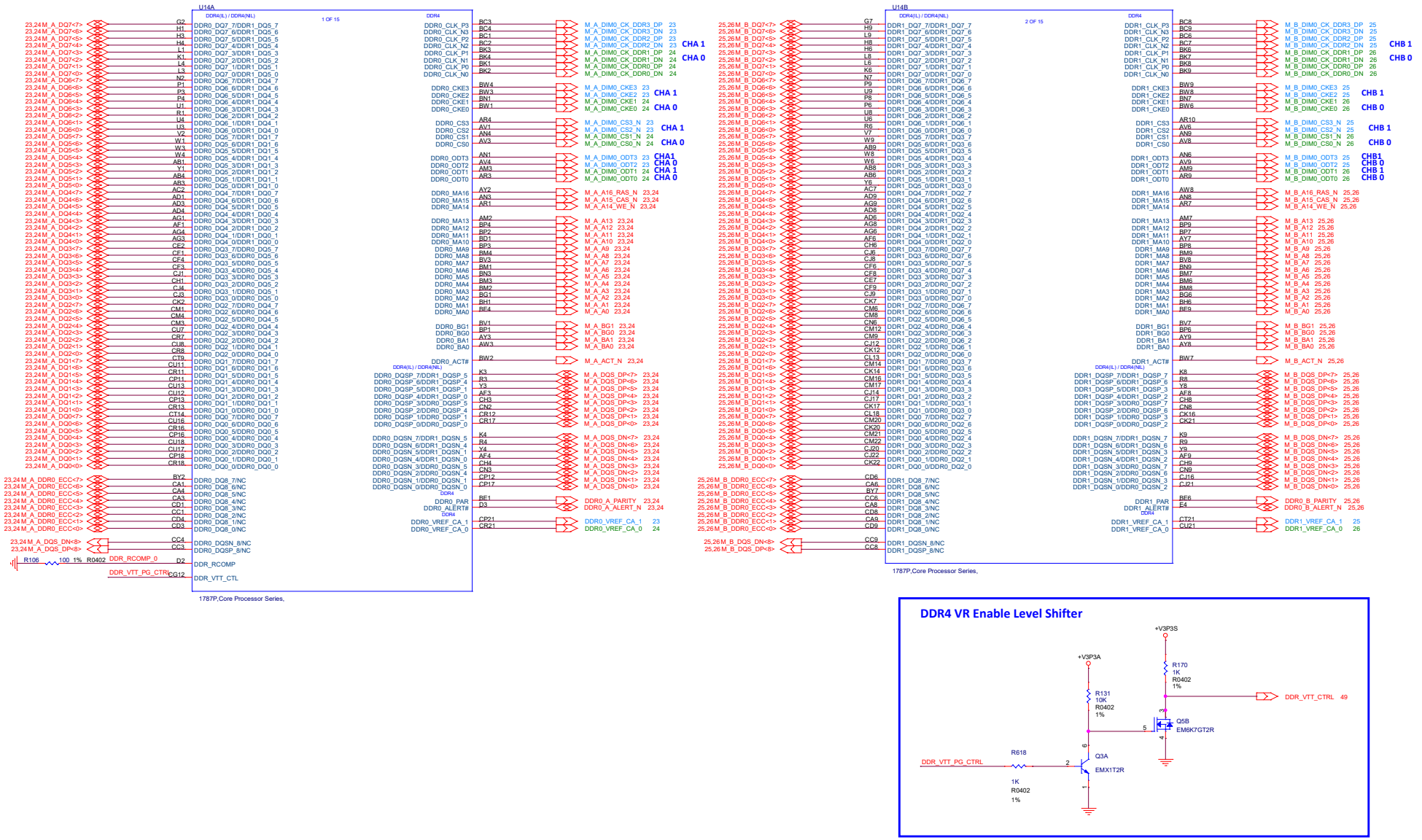
CPU_DDR4 for CHA_0 , 1 & CHB_0 , 1



DDR4 VR Enable Level Shifter

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AAEON Technology INC.		
Title: CPU_DDR4 for CHA_0 , 1 & CHB_0 , 1		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
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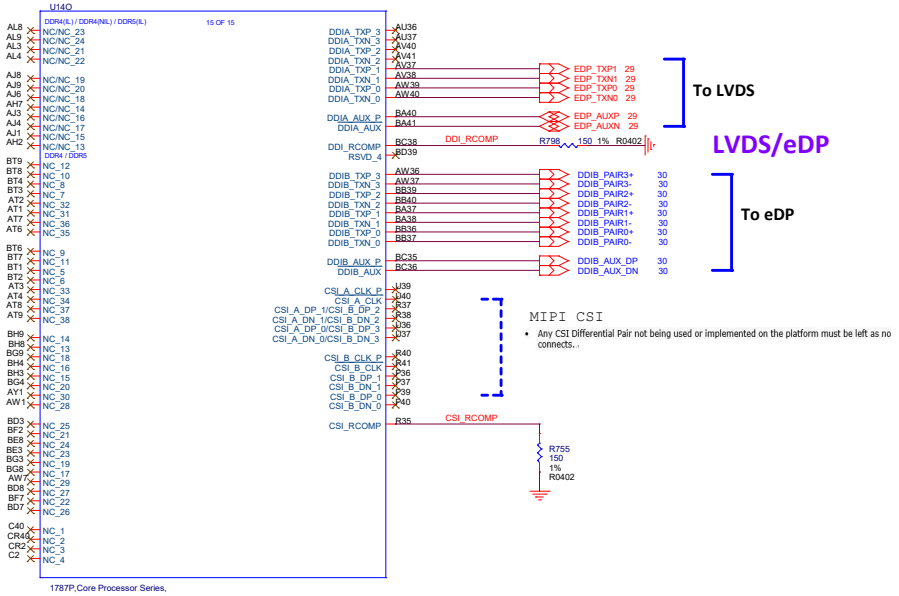
CPU_DDIA/B_eDP/LVDS



<Variant Name>

AAEON Technology INC.

Title: CPU_DDIA/B_eDP/LVDS

Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0

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CPU_DP++1~4

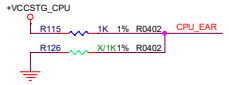
TCP Port Signal Mapping For DisplayPort*

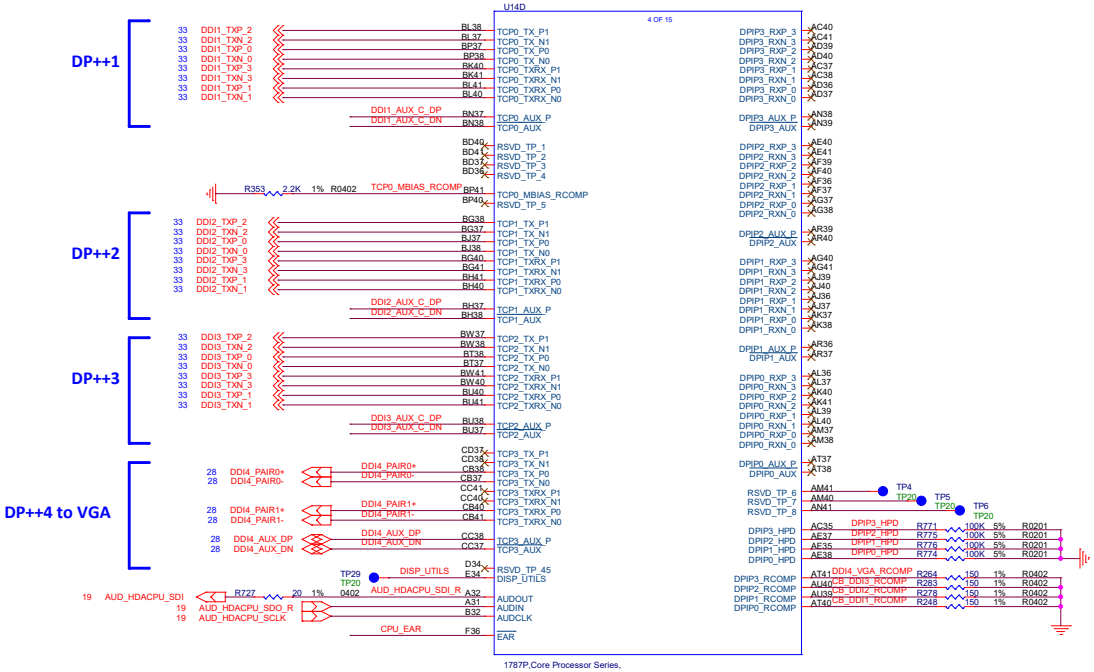
Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3
Note: Apply to TCP ports only.		

DDI Ports Availability

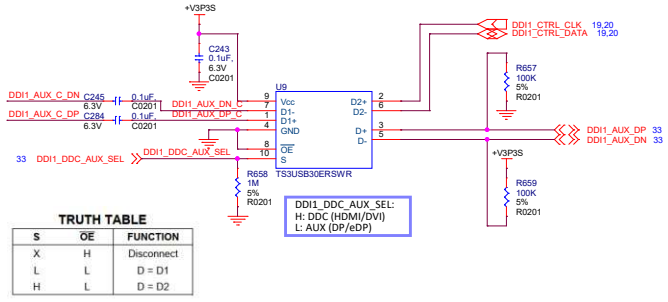
SKU	H Processor Line
DDI A	eDP*
DDI B	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*
TCP1	DP*/HDMI*
TCP2	DP*/HDMI*
TCP3	DP*/HDMI*
DPIP 0	DP*
DPIP 1	DP*
DPIP 2	DP*
DPIP 3	DP*

CPU_EAR	Stall CPU reset sequence until de-asserted:
1 (*)	Normal Operation; No stall.
0	Stall





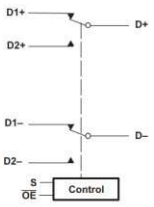
DDI1 / AUX Switch



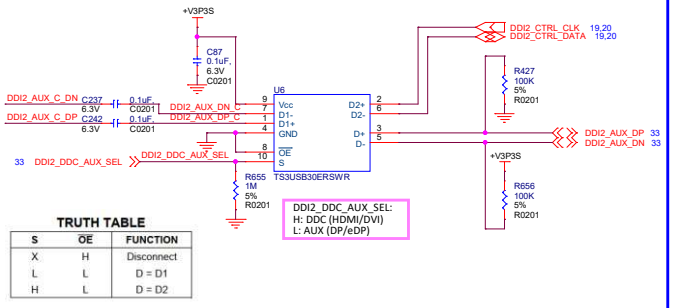
TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM



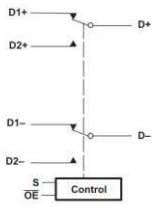
DDI2 / AUX Switch



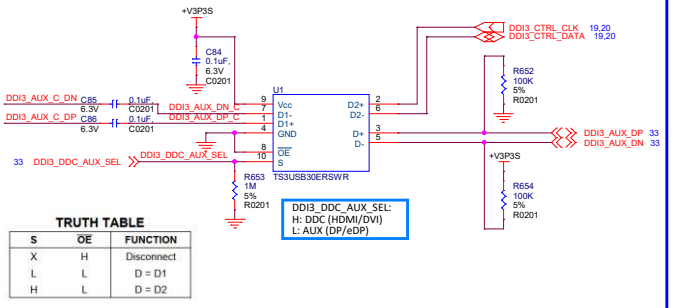
TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM



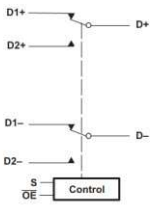
DDI3 / AUX Switch



TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM



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AAEON Technology INC.

Title	CPU_DP++1~4	
Size	Document Number	Rev
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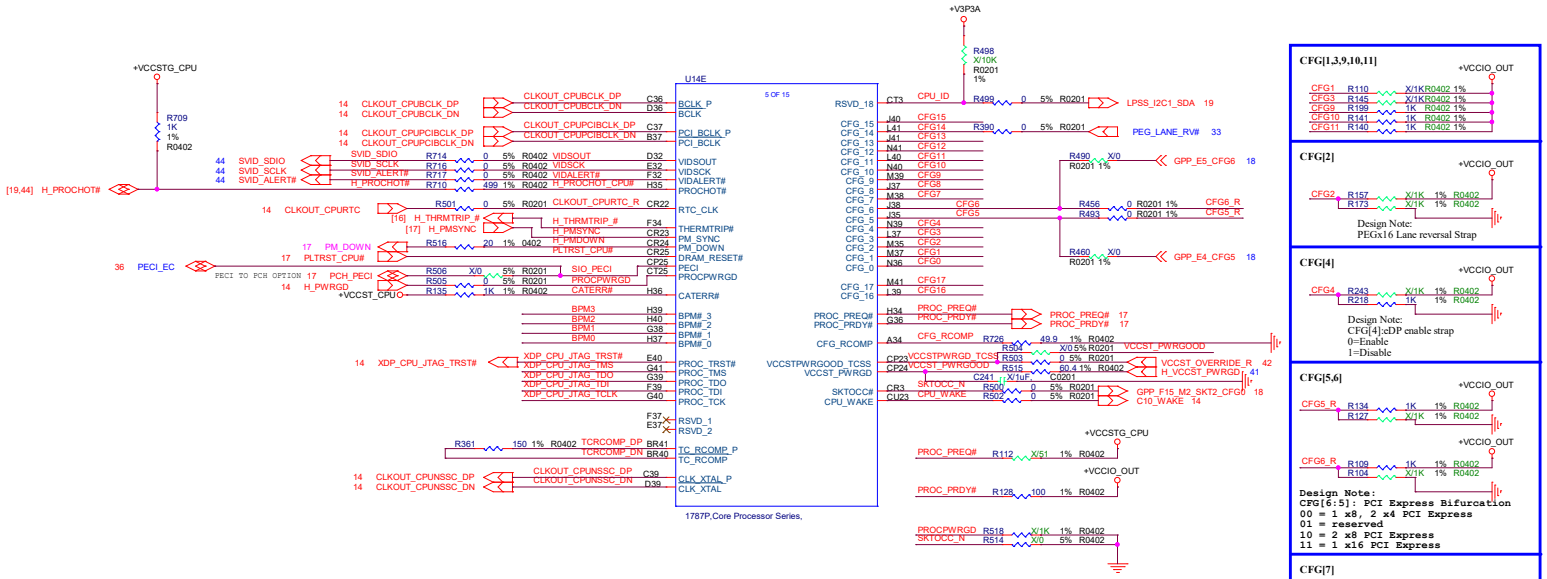
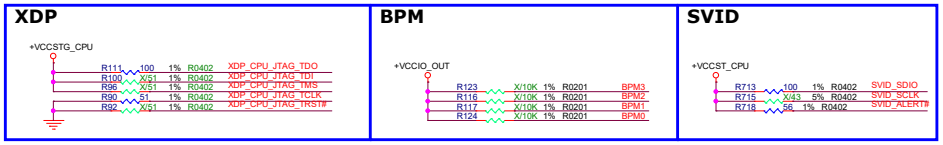
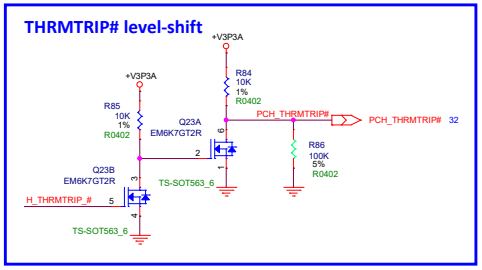
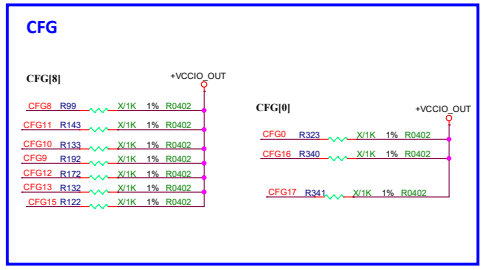
CPU_CLK/CFG/RSVD

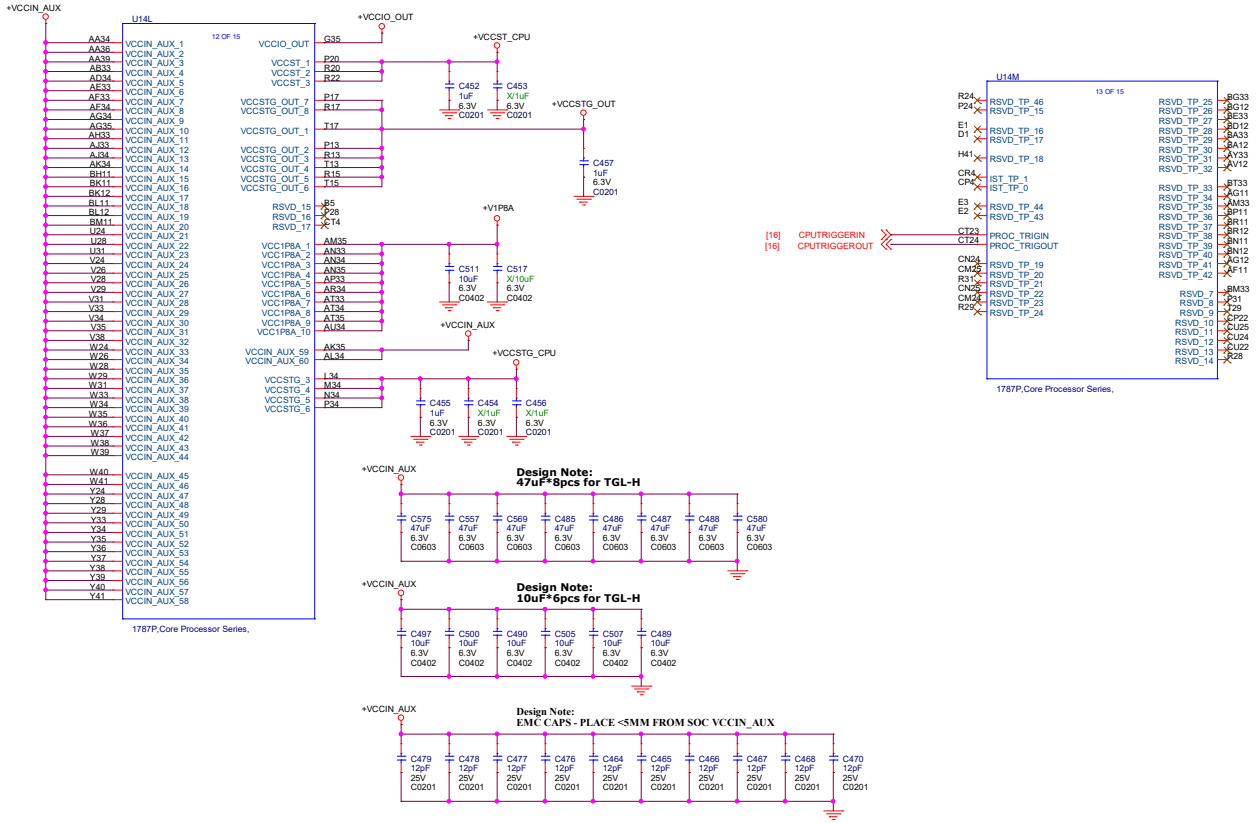








CPU_PWR1



<Variant Name>

AAEON Technology INC.		
Title: CPU_PWR1		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
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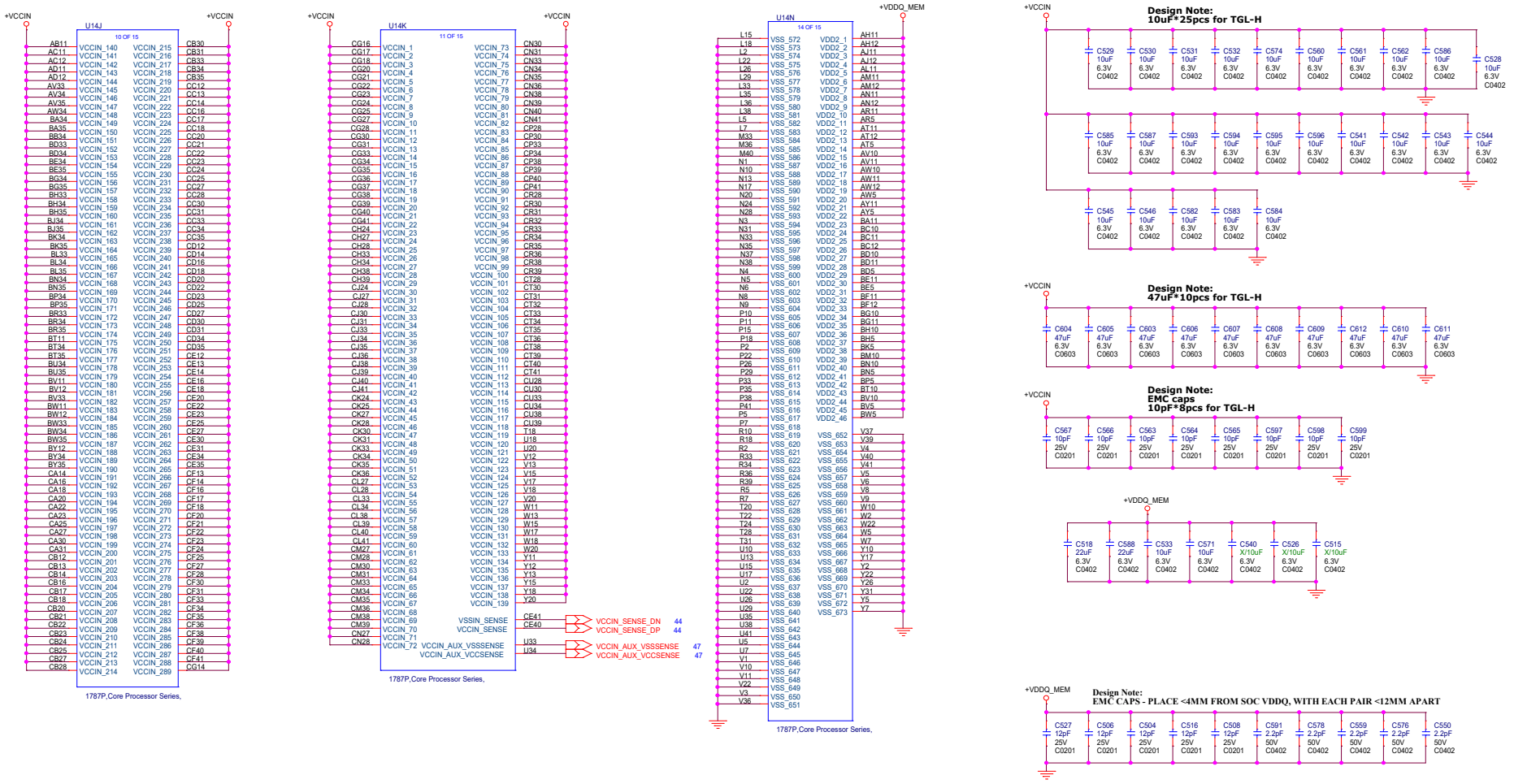
CPU_PWR2



<Variant Name>

AAEON Technology INC.

Title	CPU_PWR2	
Size	Document Number	Rev
	COM-TGHB6	A0.1_0_0
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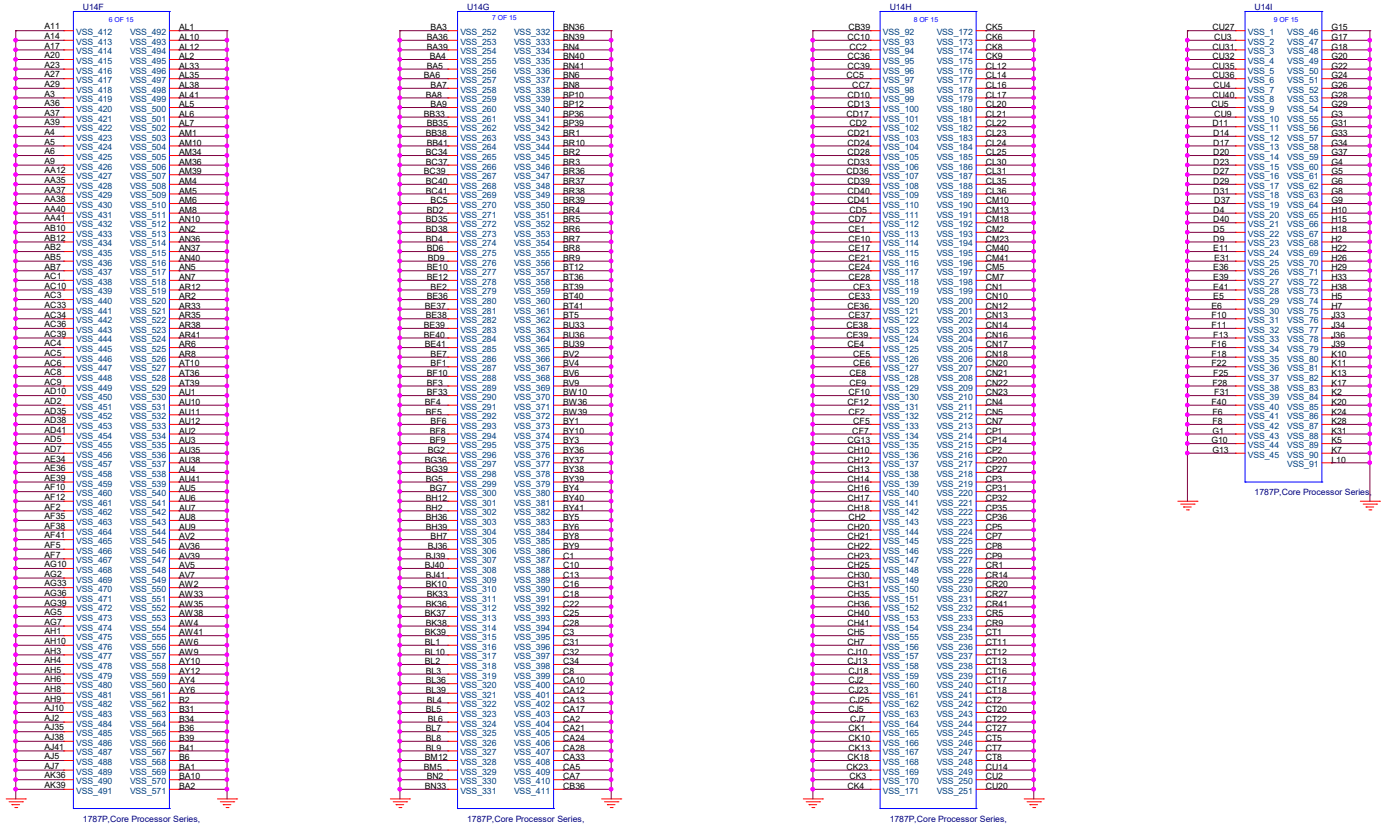
CPU_VSS



<Variant Name>

AAEON Technology INC.

Title: CPU_VSS

Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0

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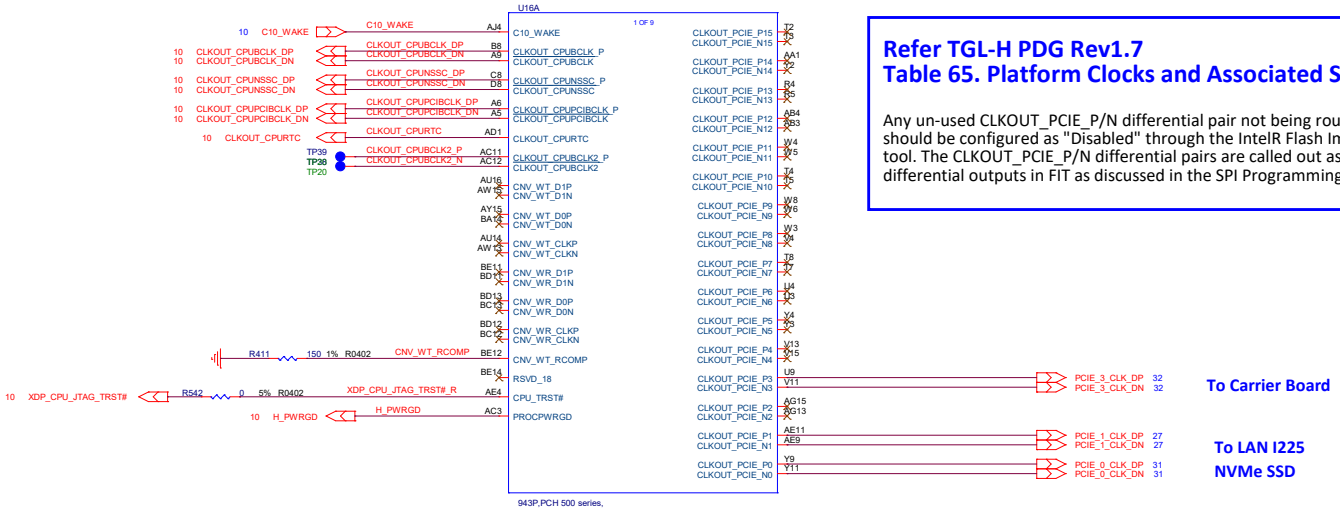
PCH_CLK



Refer TGL-H PDG Rev1.7
Table 65. Platform Clocks and Associated Signal Details and Descriptions

Any un-used CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the IntelR Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.

To Carrier Board

To LAN I225
NVMe SSD

Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support
			• CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

<Variant Name>

AAEON Technology INC.

Title	PCH_CLK	
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
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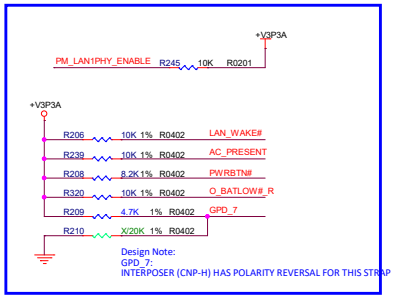
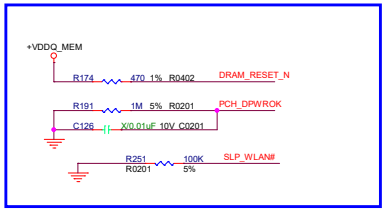
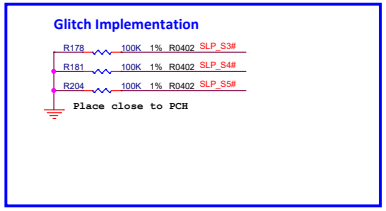
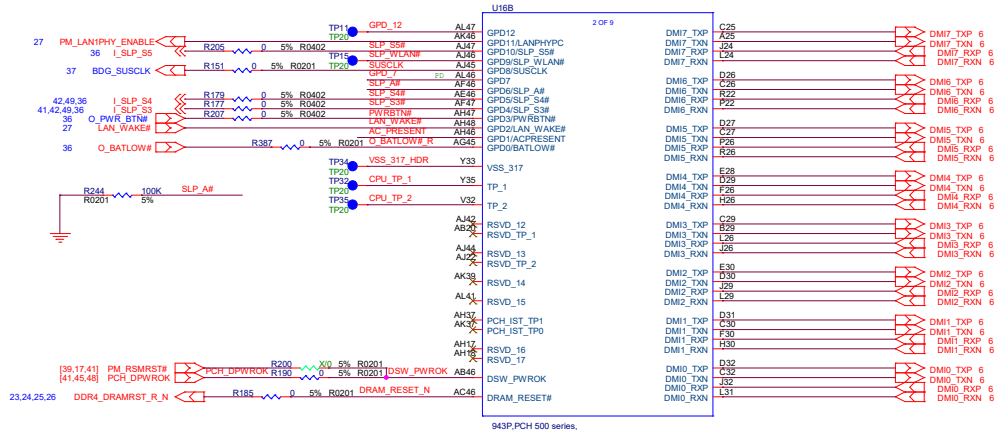
PCH_DMI/MISC









DSW_PWROK	I	**Deep Sx Well PWROK:** Power OK Indication for the VCCDSW_3P3 voltage rail. *Note:* This signal is in the RTC well. This signal cannot tie with RSMRST#.

PDG: DSW_PWROK and RSMRST# are always separate power good signals

<Variant Name>

AAEON Technology INC.		
Title: PCH_DMU/MISC		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
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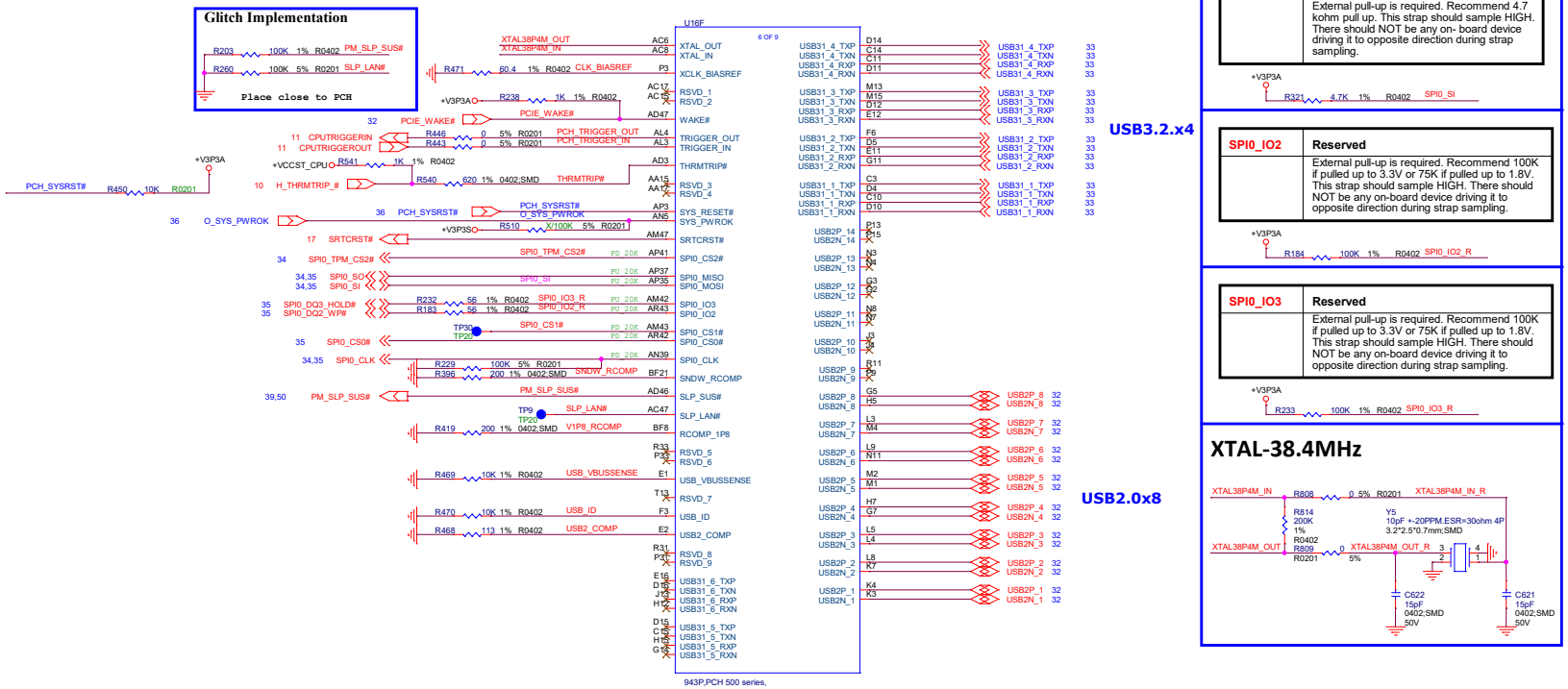
PCH_USB3/USB2/SPI



<Variant Name>

AAEON Technology INC.

Title	PCH_USB3/USB2/SPI	
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
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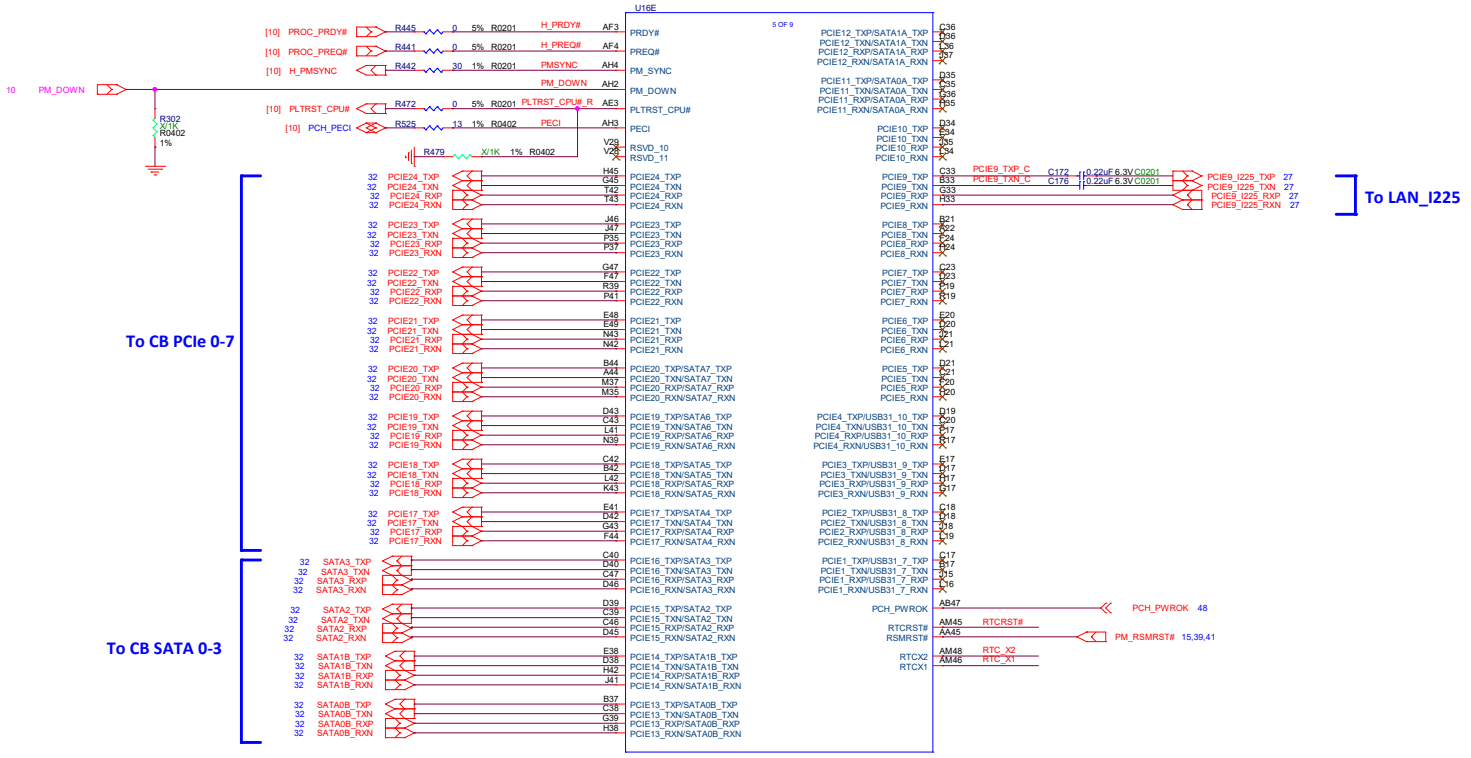
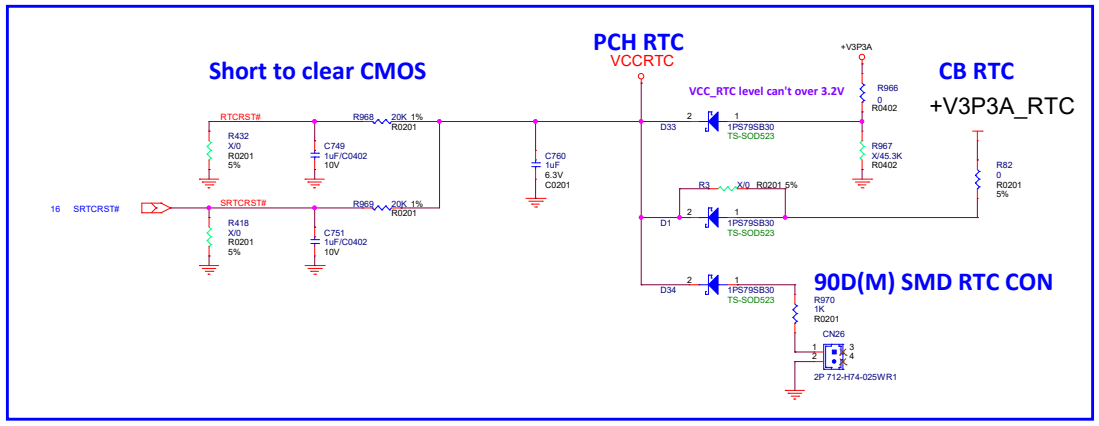
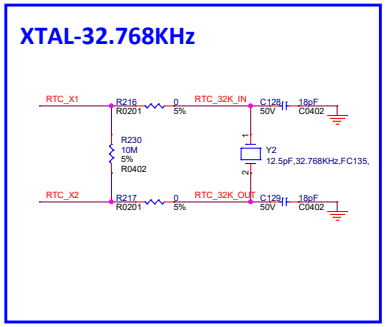
PCH_PCIE/SATA/RTC







<variant_name>

AAEON Technology INC.

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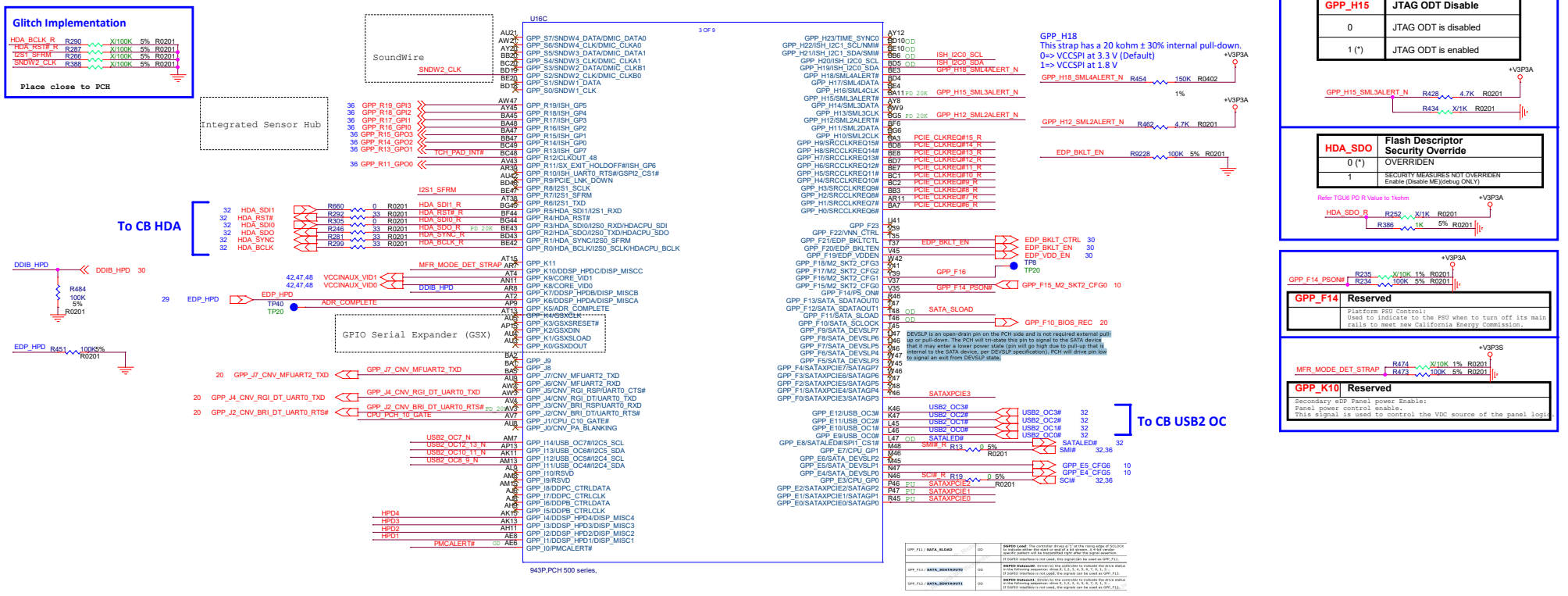
PCH_ISH/DMIC/HDA/SMLINK/I2S



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AAEON Technology INC.	
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PCH_UART/GPIO/eSPI/JTAG/SMB

SMBALERT#	TLS confidentiality
0	TLS CONFIDENTIALITY DISABLE
1 (*)	TLS CONFIDENTIALITY ENABLE

+V3P3A — R351 4.7K 1% R0402 SMBALERT#

SML0ALERT#	ESPI
0 (*)	Enable eSPI
1	Disable eSPI

+V3P3A — R379 X/4.7K 1% R0402 SML0ALERT# — R365 20K 1% 0402:SMD

SML1ALERT#	CPUNSSC CLOCK FREQ
0 (*)	38.4MHZ CLOCK FROM DIRECT CRYSTAL
1	19.2MHZ CLOCK FROM DIVIDER

Design Note:
When used as PCHHOT# and strap low, a 150 kohm pull-up is needed to ensure it does not override the internal pull-down strap sampling.

+V3P3A — R268 150K 1% R0402 SML1ALERT#

GSPI1_MOSI	BOOT BIOS STRAP
0 (*)	SPI SELECTED
1	eSPI SELECTED FOR SYSTEM FLASH

+V3P3A — R242 X/4.7K 1% R0402 GSPI1_MOSI

GSPI0_MOSI	No Reboot
0 (*)	REBOOT ENABLED
1	NO REBOOT

+V3P3A — R211 X/4.7K 1% R0402 GSPI0_MOSI

SPKR	Top Swap Override
0 (*)	Disabled
1	Enable

+V3P3A — R325 X/20K 1% 0402:SMD SPKR

Glitch Implementation

+V3P3S — R294 100K 1% R0402 SLP_S0#

U16D — 4 OF 9 — 943P,PCH 500 series,

Touch Host Controller (THC)

GPP_D23/UART3_CTS#/THC1_SPI2_INT#
GPP_D22/UART3_RTS#/THC1_SPI2_RST#
GPP_D21/UART3_TXD/THC1_SPI2_IO3
GPP_D20/UART3_RXD/THC1_SPI2_IO2
GPP_D19/GSPI3_MOSI/THC1_SPI2_IO1
GPP_D18/GSPI3_MISO/THC1_SPI2_IO0
GPP_D17/GSPI3_CLK/THC1_SPI2_CLK
GPP_D16/GSPI3_CS0#/THC1_SPI2_CS#
GPP_D15/SML1DATA
GPP_D14/THC0_SPI1_IO3
GPP_D13/THC0_SPI1_IO2
GPP_D12/ISH_UART0_CTS#
GPP_D11
GPP_D10/SML0DATA
GPP_D9/SML0CLK
GPP_D8/I2S2_SCLK/THC0_SPI1_INT#
GPP_D7/I2S2_RXD/THC0_SPI1_RST#
GPP_D6/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D4/SML1CLK
GPP_D3/THC0_SPI1_IO0/SBK3/BK3
GPP_D2/THC0_SPI1_IO1/SBK2/BK2
GPP_D1/THC0_SPI1_CLK/SBK1/BK1
GPP_D0/THC0_SPI1_CS#/SBK0/BK0

GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C7/ISH_I2C2_SCL/I2C3_SCL
GPP_C6/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
GPP_C5/SML0ALERT#
GPP_C4/ISH_UART0_TXD/I2C2_SCL
GPP_C3/ISH_UART0_RXD/I2C2_SDA
GPP_C2/SMBALERT#
GPP_C1/SMBDATA
GPP_C0/SMBCLK

GPP_B23/SML1ALERT#/PCHHOT#
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#
GPP_B14/SPKR
GPP_B13/PLTRST#
GPP_B12/SLP_S0#
GPP_B11/I2S_MCLK
GPP_B10/SRCCLKREQ5#
GPP_B9/SRCCLKREQ4#
GPP_B8/SRCCLKREQ3#
GPP_B7/SRCCLKREQ2#
GPP_B6/SRCCLKREQ1#
GPP_B5/SRCCLKREQ0#
GPP_B4/CPU_GP3
GPP_B3/CPU_GP2
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#/IMGCLKOUT1

GPP_A14/IMGCLKOUT0
GPP_A13/ESPI_ALERT3#
GPP_A12/ESPI_ALERT2#
GPP_A11/ESPI_ALERT1#
GPP_A10/ESPI_ALERT0#
GPP_A9/ESPI_CS3#
GPP_A8/ESPI_CS2#
GPP_A7/ESPI_CS1#
GPP_A6/ESPI_RESET#
GPP_A5/ESPI_CLK
GPP_A4/ESPI_CS0#
GPP_A3/ESPI_IO3/SUSACK#
GPP_A2/ESPI_IO2/SUSWARN#/SUSPWRDNACK
GPP_A1/ESPI_IO1
GPP_A0/ESPI_IO0

GPP_G15/DDP2_CTRLDATA/TBT_LSX1_RXD/BSSB_LS1_TX
GPP_G14/DDP2_CTRLCLK/TBT_LSX1_TXD/BSSB_LS1_RX
GPP_G13/DDP1_CTRLDATA/TBT_LSX0_RXD/BSSB_LS0_TX
GPP_G12/DDP1_CTRLCLK/TBT_LSX0_TXD/BSSB_LS0_RX
GPP_G11/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI/TBT_LSX3_RXD/BSSB_LS3_TX
GPP_G10/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO/TBT_LSX3_TXD/BSSB_LS3_RX
GPP_G9/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK/TBT_LSX2_RXD/BSSB_LS2_TX
GPP_G8/ISH_SPI_CS#/DDP3_CTRLCLK/GSPI2_CS0#/TBT_LSX2_TXD/BSSB_LS2_RX

GPP_G7/RSVD
GPP_G6/RSVD
GPP_G5/SLP_DRAM#
GPP_G4
GPP_G3
GPP_G2/DNX_FORCE_RELOAD
GPP_G1/DDPA_CTRLDATA
GPP_G0/DDPA_CTRLCLK

GPP_RCOMP
PCIE_RCOMPP
PCIE_RCOMPN

CL_RST#
CL_DATA
CL_CLK

PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK

DBG_PMODE
INTRUDER#
HDACPU_SDO
HDACPU_SDI
HDACPU_BCLK

ESPI_RESET# — R182 75K 1% R0402 — R196 75K 1% R0402
ESPI_ALERT0 R9259 0_5% R0201 — BDG_ESPI_ALT_1P8# 37
ESPI_CS3 TP13
ESPI_CS2 TP20 TP14
ESPI_CS1 TP20 TP12
ESPI_RESET# R407 0_5% R0201 TP20 — BDG_ESPI_RST# 37
ESPI_CLK R413 10 1% 0402:SMD — BDG_ESPI_CLK 37
ESPI_CS# R405 0_5% R0201 — BDG_ESPI_CS# 37
ESPI_IO_3 R149 10 1% 0402:SMD — BDG_ESPI_IO_3 37
ESPI_IO_2 R148 10 1% 0402:SMD — BDG_ESPI_IO_2 37
ESPI_IO_1 R146 10 1% 0402:SMD — BDG_ESPI_IO_1 37
ESPI_IO_0 R147 10 1% 0402:SMD — BDG_ESPI_IO_0 37

DDI2_CTRL_DATA 20,9
DDI2_CTRL_CLK 20,9
DDI1_CTRL_DATA 20,9
DDI1_CTRL_CLK 20,9
DDI4_CTRL_DATA 20,9
DDI4_CTRL_CLK 20,9
DDI3_CTRL_DATA 20,9
DDI3_CTRL_CLK 20,9

TP27 TP20 TP24 TP20 TP23 TP20
DDPA_CTRLDATA R393 2/2.2K 5% R0201
DDPA_CTRLCLK R400 2/2.2K 5% R0201 — +V3P3S
GPP_RCOMP R420 200 1% 0402:SMD
MPHY_RCOMPP R409 100 1% 0402:SMD
MPHY_RCOMPN

PCH_JTAGX R482 X/51 1% 0402:SMD
PCH_JTAG_TMS R543 51 1% 0402:SMD
PCH_JTAG_TDO R544 100 1% 0402:SMD
PCH_JTAG_TDI R545 51 1% 0402:SMD
PCH_JTAG_TCK R483 X/51 1% 0402:SMD — +VCCSTG_CPU
DBG_PMODE PU 20K
SM_INTRUDER# R267 1M 1% R0402 — VCCRTC
AUD_HDACPU_SDO R440 30 1% R0201 — AUD_HDACPU_SDO_R 9
AUD_HDACPU_SDO_R R444 30 1% R0201 — AUD_HDACPU_SDI 9
AUD_HDACPU_SCLK 9
Place close to PCH

SML1DATA — SML1DATA
LAN_SM_DATA — LAN_SM_DATA
LAN_SM_CLK — LAN_SM_CLK
SML1CLK — SML1CLK
LPSS_UART2_TXD
LPSS_UART2_RXD
LPSS_I2C1_SCL
LPSS_I2C1_SDA — I2C0_SCL — I2C0_SDA
TPM_PIRQ#
LPSS_UART1_TXD
LPSS_UART1_RXD
LPSS_UART0_TXD
LPSS_UART0_RXD
ISH_I2C2_SCL
ISH_I2C2_SDA
SMBALERT# PD 20K
ISH_UART0_TXD
ISH_UART0_RXD
SMBALERT# PD 20K
SMB_DATA
SMB_CLK
SML1ALERT# PD 20K
GSPI1_MOSI PD 20K
GSPI0_MOSI PD 20K
SPKR PD 20K
PLTRST#
R301 0_5% R0201 SLP_S0#
PCIE_CLKREQ#5_R
PCIE_CLKREQ#4_R
PCIE_CLKREQ#3_R
PCIE_CLKREQ#2_R
PCIE_CLKREQ#1
PCIE_CLKREQ#0
I225
SSD
R334 X/0 5% R0201 VRALERT#
H_PROCHOT#
R309 10K 1% R0201 — +V3P3S
KBRST# — R343 0 5% R0201 — RCIN#

SMBALERT# Level Shift

SMBus Level Shift

+V3P3S — R403 2.2K 5% R0201 — Q14B EM6K7GT2R TS-SOT563_6 — SMB_DATA_S2 [23,24,27,33,34,38,43]
SMB_DATA
SMB_CLK
+V3P3S — R397 2.2K 5% R0201 — Q14A EM6K7GT2R TS-SOT563_6 — SMB_CLK_S2 [23,24,27,33,34,38,43]

+V3P3A
R357 X/4.7K 1% R0402 ISH_UART0_TXD
R395 X/4.7K 1% R0402 ISH_UART0_RXD
R347 499 1% R0402 LAN_SM_CLK
R350 499 1% R0402 LAN_SM_DATA
R337 1K 5% R0201 SML1CLK
R348 1K 5% R0201 SML1DATA
R358 1K 5% R0201 SMB_CLK
R354 1K 5% R0201 SMB_DATA
+V3P3S
R383 1K 5% R0201 I2C0_SCL
R372 1K 5% R0201 I2C0_SDA
R366 1K 5% R0201 LPSS_I2C1_SCL
R380 1K 5% R0201 LPSS_I2C1_SDA
R356 X/2.7K 1% 0402:SMD ISH_I2C2_SCL
R362 X/2.7K 1% 0402:SMD ISH_I2C2_SDA

Dual Bus Buffer Gate with 3-State Outputs

+V3P3A — C195 0.1uF, 6.3V C0201
U13 SN74LVC2G125DCUR (1OE, 1A, 2Y, GND, VCC, 2OE, 1Y, 2A)
PLTRST# — R195 100K 5% R0201
BUF_CB_RST# — BUF_CB_RST# 32 — R360 100K 1% R0402
PLTRST#
PCIE_RST COMe is RSVD , R Default Empty
BUF_PLT_RST# — BUF_PLT_RST# 27,28,29,31,34,36,37 — R186 100K 1% R0402

Carry Board
PCIE_RST*2

eSPI to LPC
eDP to LVDS
DDI to VGA
LAN
EC
TPM

DBG_PMODE	Reserved
	This strap should sample high. There should NOT be any on- board device driving it to opposite direction during strap sampling.

+V1P05_OUT_FET — R9260 1K 5% R0201 — DBG_PMODE — X/1K 1% R0402 R480

VRALERT#	Reserved
	VR Alert: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PNC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.

VRALERT# — R332 100K 1% R0402 — +V3P3A

PCIe CLKOUT Req PD

PCIE_CLKREQ#5_R R310 1K 5% R0201
PCIE_CLKREQ#4_R R311 1K 5% R0201
PCIE_CLKREQ#3_R R312 1K 5% R0201
PCIE_CLKREQ#2_R R375 1K 5% R0201
PCIE_CLKREQ#1 R313 1K 5% R0201
PCIE_CLKREQ#0 R314 1K 5% R0201

PCIe CLKOUT Req PU

Placement Simplify

Refer TGL-H PDG Rev1.7
Figure 80. SRC Request Signal Topology

9. Any un-used SRCCLKRQ# signal must be left as no connects

BIOS Disabled setting : CLKOUT_PCIE 2,4,5

<Variant Name>

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An ASUS Company

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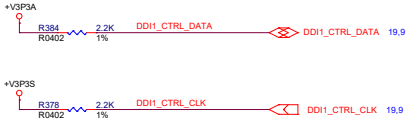
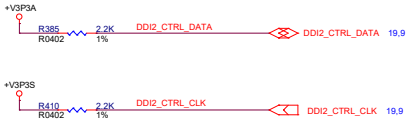
PCH_OTHER STRAP

DDI1-4 DATA/CLK

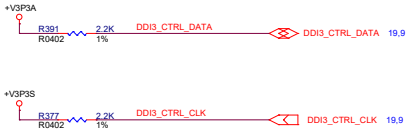
TBT_LSX0	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



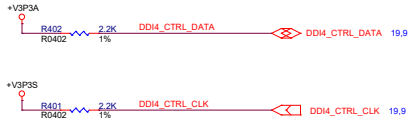
TBT_LSX1	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



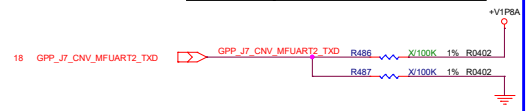
TBT_LSX2	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



TBT_LSX3	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



GPP_J7	Reserved
	For CNVi and discrete connectivity : Optional WLAN/Bluetooth* WWAN co-existence signal (Output)



GPP_J4	CNVI STRAP
0	CNVI ENABLE
1 (*)	CNVI DISABLE

GPP_J2	XTAL SELECT
0 (*)	38.4/19.2MHZ
1	24MHZ

GPP_F10	Reserved
	SGPIO Reference Clock: The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. The SClock frequency supported is 32 kHz. If SGPIO interface is not used, this signal can be used as GPP_F10.

<Variant Name>

AAEON Technology INC.

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PCH_PWR

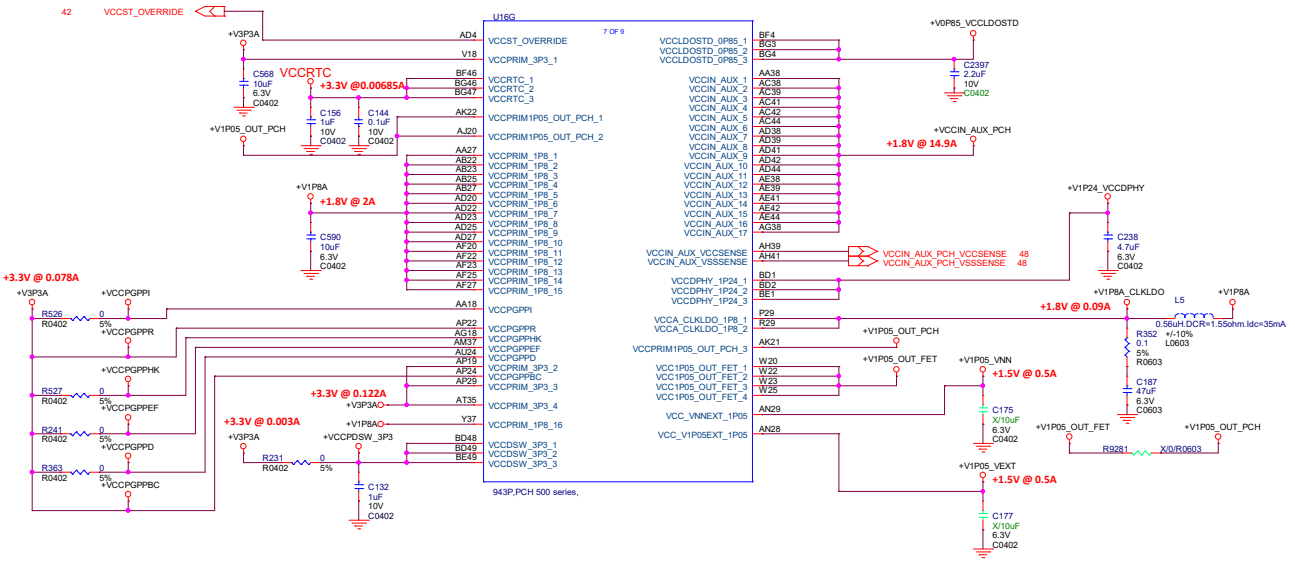
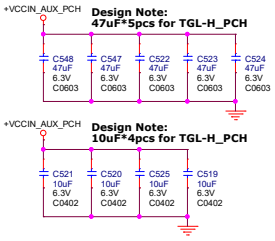
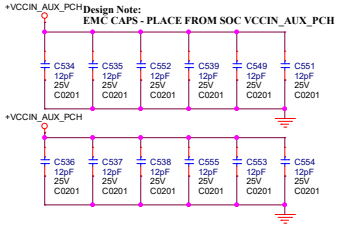


Table 39. GPIO Group Summary

GPIO Group	Power Pins or Power Wells	Voltage
Primary Well Group A (GPP_A)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPPBC	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group D (GPP_D)	VCCPGPPD	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group G (GPP_G)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group I (GPP_I)	VCCPGPPI	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8 V Only
Primary Well Group R (GPP_R)	VCCPGPPR	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group S (GPP_S)	VCCPRIM_1P8	1.8 V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only





<Variant Name>

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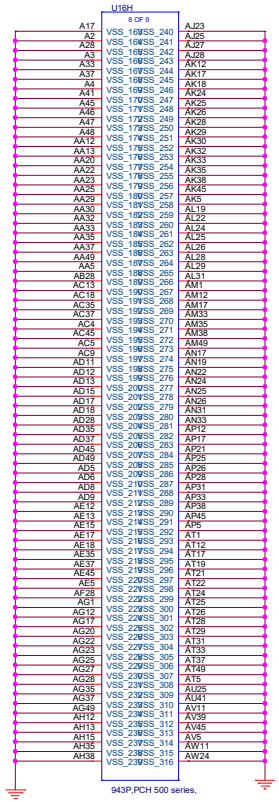
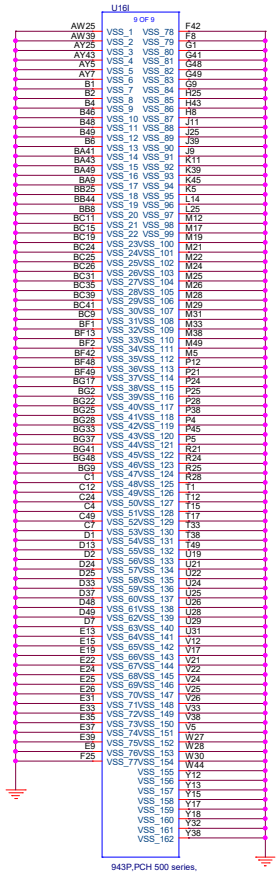
PCH_VSS





<Variant Name>

AAEON Technology INC.

Title: PCH_VSS

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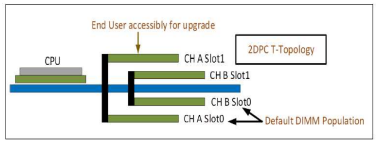
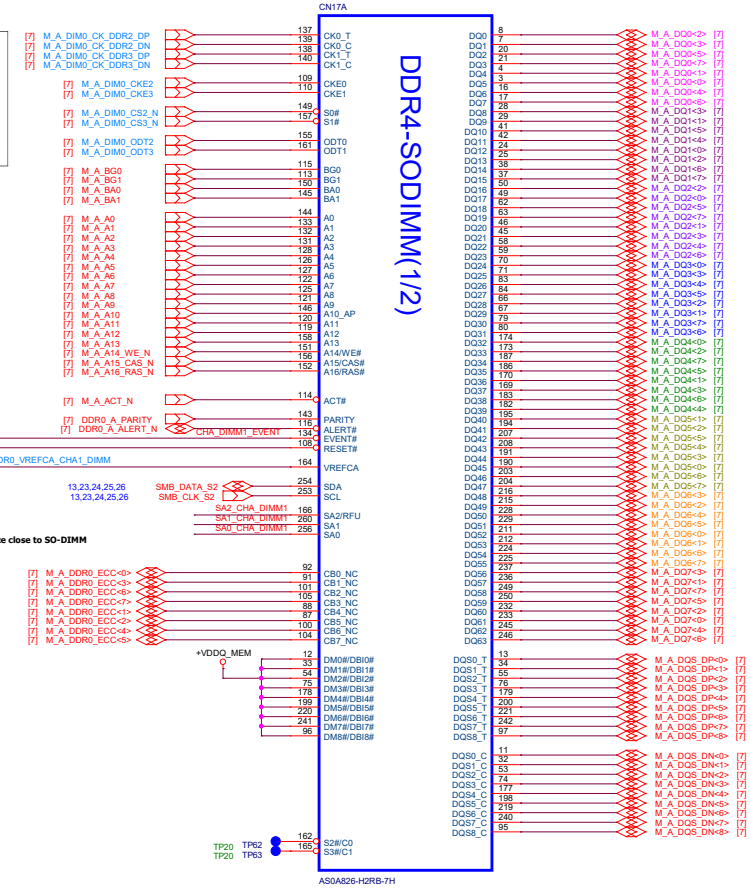
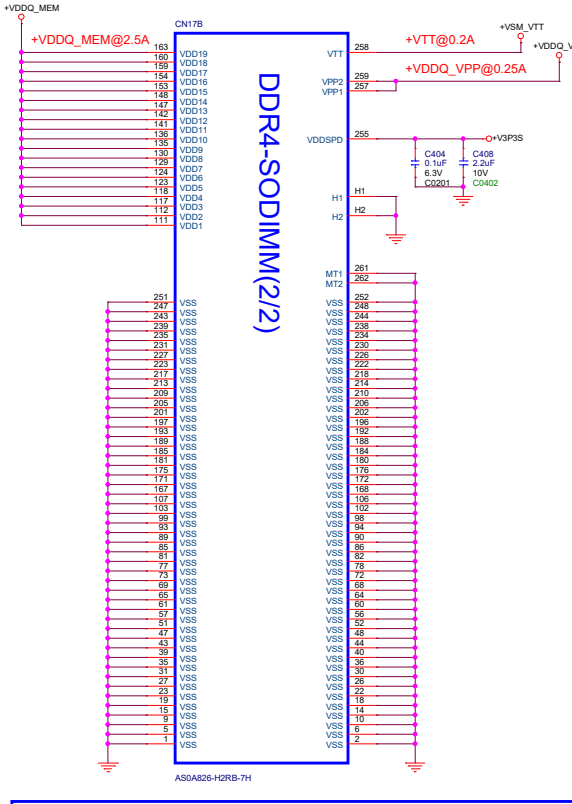
DDR4
2DPC T-Topology
CH A_DIMM1 Top Layer

CHA Slot1
1651526000 / (TF)DDR4 SODIMM SKT.SMD.H=5.2mm.260P.P=0.5mm.REVERSE.1.2V.FOXCONN.AS0A826-H2RB-7H

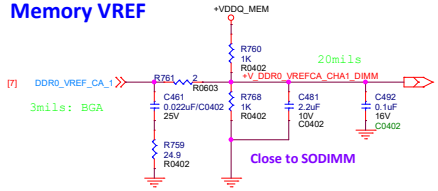


refer 618429_TGL_H_PDG_Rev1.7 --- 2021/04
ps. 618697_TGL_H_DDR4_SCH_REV1p5 --- 2020/08
Slot 0/1 reverse PDG

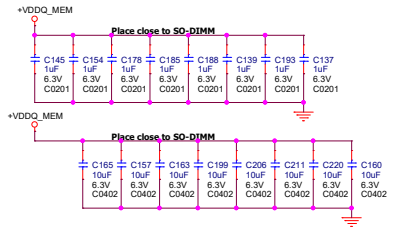




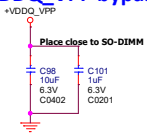
Memory VREF



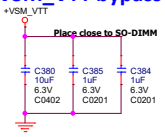
+VDDQ_MEM bypass Cap



+VDDQ_VPP bypass Cap



+VSM_VTT bypass Cap

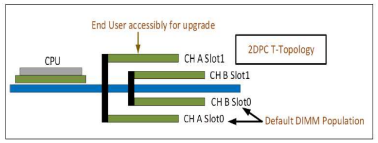


<Variant Name>

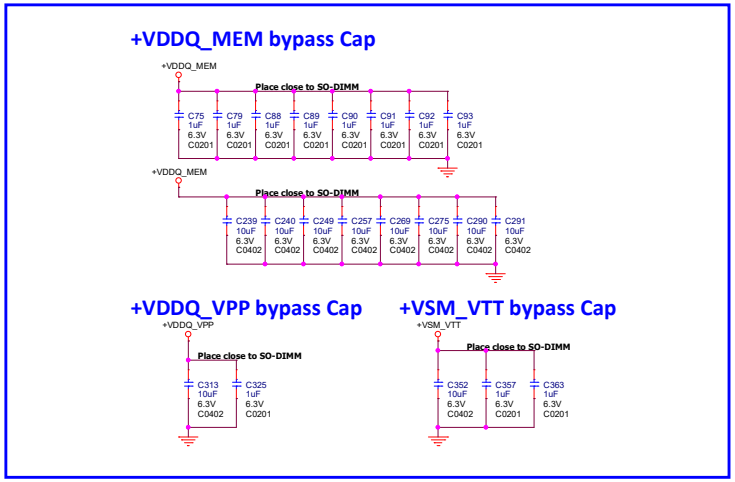
AAEON Technology INC.
Title: DDR4-CHA DIMM1
Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0
Date: Friday, November 12, 2021 | Sheet 23 of 51

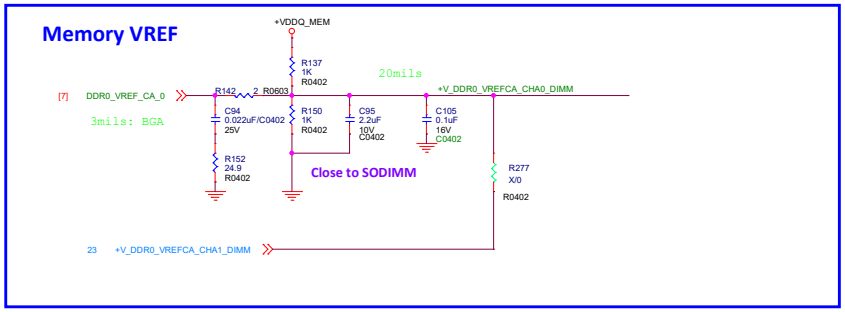
DDR4
2DPC T-Topology
CH A_DIMM0 Bot Layer

CHA Slot0
1651526007 / (TF)DDR4 SODIMM SKT.90D.SMD.H=4mm.260P.P=0.5mm.STANDARD. 1.2V.FOXCONN.AS0A826-H4SB-7H

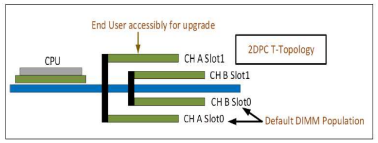


refer 618429_TGL_H_PDG_Rev1.7 --- 2021/04
ps. 618697_TGL_H_DDR4_SCH_REV1p5 --- 2020/08
Slot 0/1 reverse PDG





DDR4
2DPC T-Topology
CH B DIMM1 Top Layer



refer 618429_TGL_H_PDG_Rev1.7 --- 2021/04
ps. 618697_TGL_H_DDR4_SCH_REV1p5 --- 2020/08
Slot 0/1 reverse PDG

CHB Slot1
1651526001 / (TF)DDR4 SODIMM SKT.SMD.H=9.2mm.260P.P=0.5mm.REVERSE.1.2V.FOXCONN.ASAA826-EARB0-7H

CN9A

DDR4-SODIMM(1/2)

ASAA826-EARB0-7H

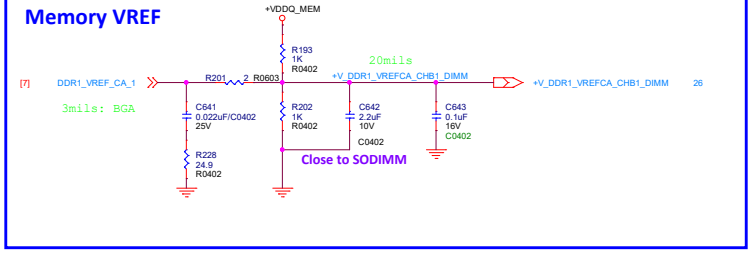
Place the CAP within 200mils from the SODIMM

CN9B

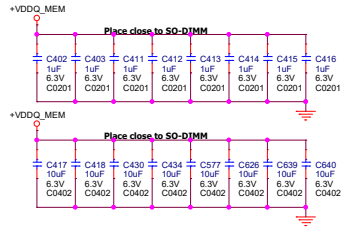
DDR4-SODIMM(2/2)

ASAA826-EARB0-7H

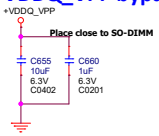
Memory VREF



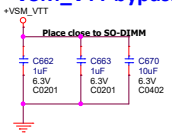
+VDDQ_MEM bypass Cap



+VDDQ_VPP bypass Cap



+VSM_VTT bypass Cap



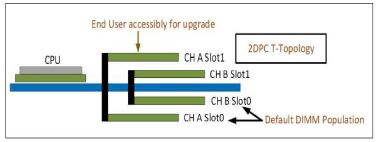
<Variant Name>

AAEON Technology INC.

Title	DDR4-CHB DIMM1	
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 25 of 51	

DDR4
2DPC T-Topology
CH B DIMM0 Bot Layer

CHB Slot0
1651526008 / (TF)DDR4 SODIMM SKT.90D.SMD.H=8mm.260P.P=0.5mm.STANDARD. 1.2V.FOXCONN.ASAA826-E8SB0-7H



refer 618429_TGL_H_PDG_Rev1.7 --- 2021/04
ps. 618697_TGL_H_DDR4_SCH_REV1p5 --- 2020/08
Slot 0/1 reverse PDG

CN40A

DDR4-SODIMM(1/2)

[7] M_B_DIM0_CK_DDR0_DP
[7] M_B_DIM0_CK_DDR0_DN
[7] M_B_DIM0_CK_DDR1_DP
[7] M_B_DIM0_CK_DDR1_DN
[7] M_B_DIM0_CKE0
[7] M_B_DIM0_CKE1
[7] M_B_DIM0_CS0_N
[7] M_B_DIM0_CS1_N
[7] M_B_DIM0_ODT0
[7] M_B_DIM0_ODT1
[7] M_B_BG0
[7] M_B_BG1
[7] M_B_BA0
[7] M_B_BA1
[7] M_B_A0
[7] M_B_A1
[7] M_B_A2
[7] M_B_A3
[7] M_B_A4
[7] M_B_A5
[7] M_B_A6
[7] M_B_A7
[7] M_B_A8
[7] M_B_A9
[7] M_B_A10
[7] M_B_A11
[7] M_B_A12
[7] M_B_A13
[7] M_B_A14_WE_N
[7] M_B_A15_CAS_N
[7] M_B_A16_RAS_N
[7] M_B_ACT_N
[7] DDR0_B_PARITY
[7] DDR0_B_ALERT_N
CHB_DIMM0_EVENT
+VDDQ_MEM
R374 240 R0402
15,23,24,25 DDR4_DRAMRST_R_N
+V_DDR1_VREFCA_CHB0_DIMM
C579 X/0.1uF 10V C0402
Place the CAP within 200mils from the SODIMM
13,23,24,25,26 SMB_DATA_S2
13,23,24,25,26 SMB_CLK_S2
SA2_CHB_DIMM0
SA1_CHB_DIMM0
SA0_CHB_DIMM0
+V3P3S
R671 0 5% R0201 SA1_CHB_DIMM0
R673 0 5% R0201 SA2_CHB_DIMM0
R675 0 5% R0201 SA0_CHB_DIMM0
[7] M_B_DDR0_ECC<2>
[7] M_B_DDR0_ECC<4>
[7] M_B_DDR0_ECC<3>
[7] M_B_DDR0_ECC<1>
[7] M_B_DDR0_ECC<0>
[7] M_B_DDR0_ECC<7>
[7] M_B_DDR0_ECC<6>
[7] M_B_DDR0_ECC<5>
+VDDQ_MEM
TP20 TP66
TP20 TP67

ASAA826-E8SB0-7H

+VDDQ_MEM +1.2V @ 2.5A

CN40B

DDR4-SODIMM(2/2)

+VSM_VTT +0.6V @ 0.2A
+VDDQ_VPP +2.5V @ 0.25A
VDDSPD
C386 0.1uF 6.3V C0201
C381 2.2uF 10V C0402
+V3P3S
H1
H2
MT1
MT2

ASAA826-E8SB0-7H

Memory VREF

+VDDQ_MEM
R778 1K R0402
20mils
[7] DDR1_VREF_CA_0
R784 2 R0603
+V_DDR1_VREFCA_CHB0_DIMM
3mils: BGA
C502 0.022uF/C0402 25V
R789 1K R0402
C512 2.2uF 10V C0402
C509 0.1uF 16V C0402
R777 24.9 R0402
Close to SODIMM
R598 X/0 R0402
25 +V_DDR1_VREFCA_CHB1_DIMM

+VDDQ_MEM bypass Cap

+VDDQ_MEM
Place close to SO-DIMM
C482 1uF 6.3V C0201
C460 1uF 6.3V C0201
C480 1uF 6.3V C0201
C503 1uF 6.3V C0201
C463 1uF 6.3V C0201
C498 1uF 6.3V C0201
C491 1uF 6.3V C0201
C494 1uF 6.3V C0201
+VDDQ_MEM
Place close to SO-DIMM
C615 10uF 6.3V C0402
C613 10uF 6.3V C0402
C600 10uF 6.3V C0402
C441 10uF 6.3V C0402
C619 10uF 6.3V C0402
C446 10uF 6.3V C0402
C450 10uF 6.3V C0402
C458 10uF 6.3V C0402

+VDDQ_VPP bypass Cap

+VDDQ_VPP
Place close to SO-DIMM
C83 10uF 6.3V C0402
C100 1uF 6.3V C0201

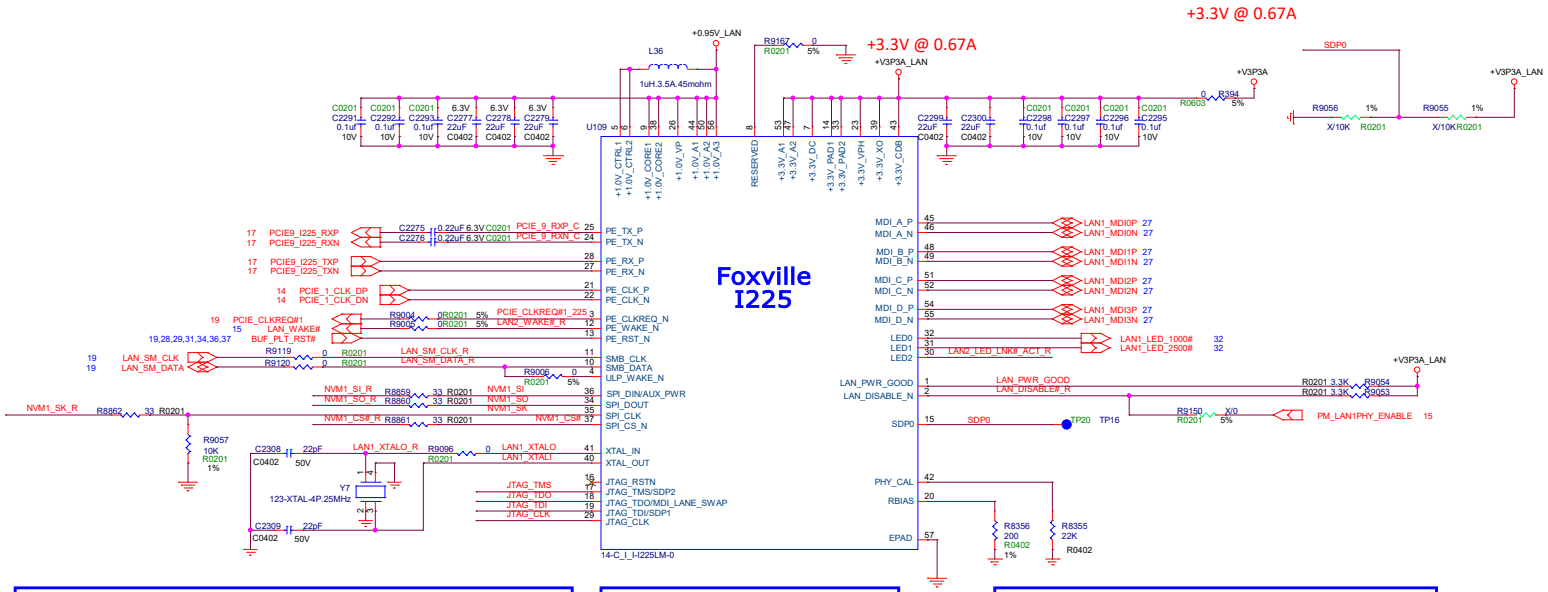
+VSM_VTT bypass Cap

+VSM_VTT
Place close to SO-DIMM
C383 1uF 6.3V C0201
C382 1uF 6.3V C0201
C379 10uF 6.3V C0402

<Variant Name>

AAEON Technology INC.
Title: DDR4-CHB DIMM0
Size: Document Number: COM-TGHB6 Rev: A0.1_0_0
Date: Friday, November 12, 2021 Sheet 26 of 51

LAN I225

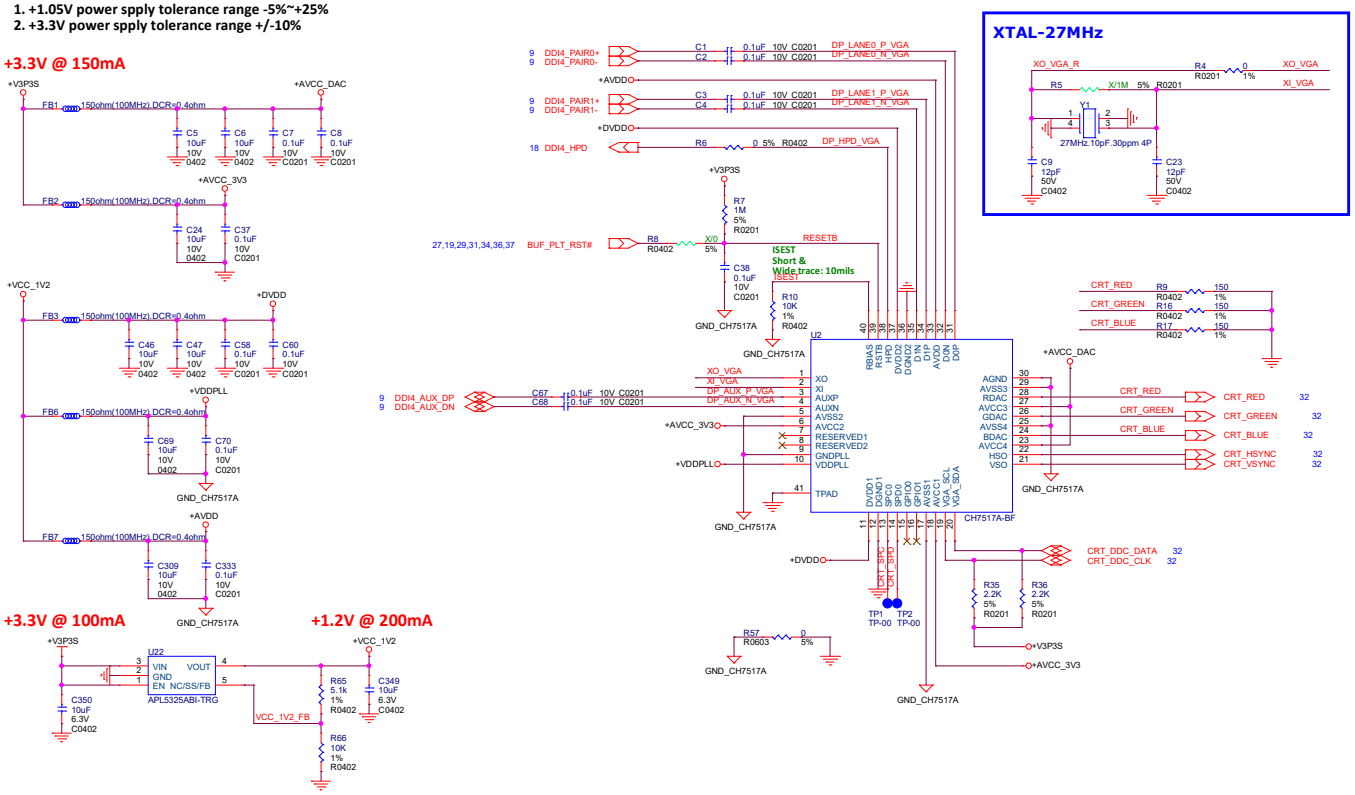


<Variant Name>

AAEON® An ASUS Company	AAEON Technology INC.		
	Title: LAN_INTEL i225LM		
	Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
	Date: Friday, November 12, 2021	Sheet 27 of 51	

DP to VGA (CH7517)

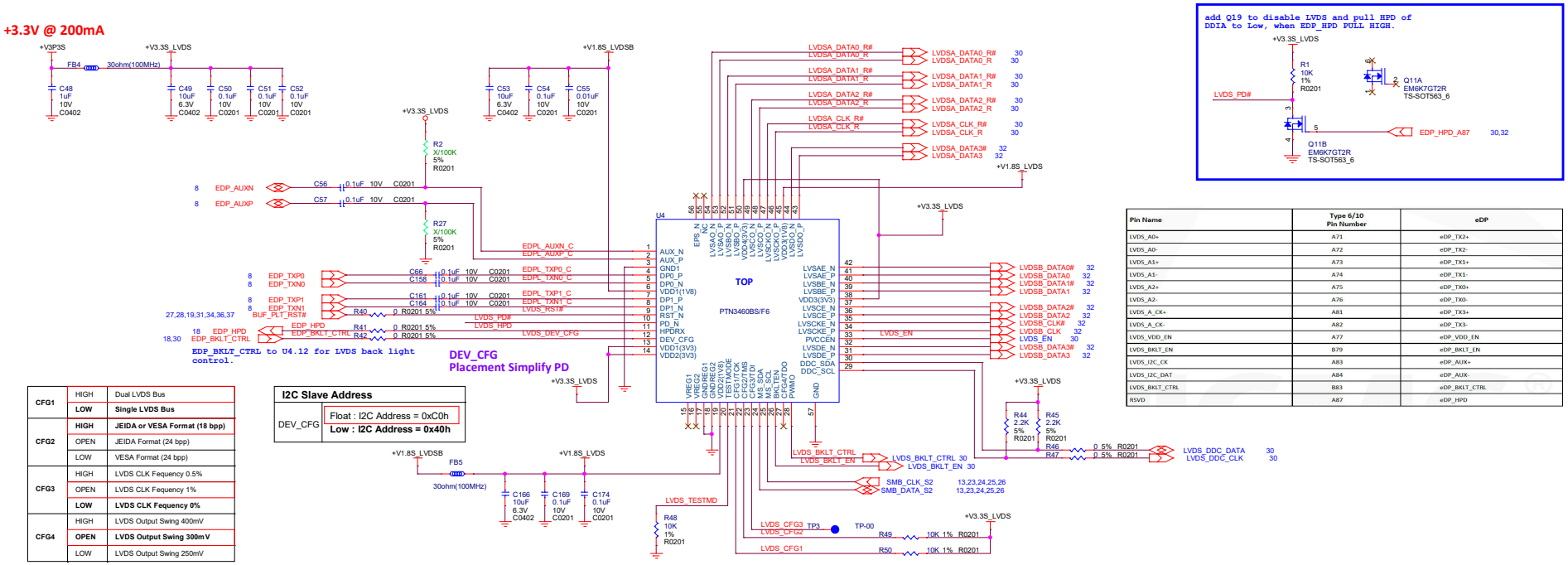
Note:
1. +1.05V power spply tolerance range -5%~+25%
2. +3.3V power spply tolerance range +/-10%



<Variant Name>

AAEON Technology INC.			
Title: DP to VGA			
Size	Document Number: COM-TGHB6		Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 28 of 51		

eDP to LVDS_PTN3460



Pin Name	Type 6/10 Pin Number	eDP
LVDS_A0+	A71	eDP_TX2+
LVDS_A0-	A72	eDP_TX2-
LVDS_A1+	A73	eDP_TX1+
LVDS_A1-	A74	eDP_TX1-
LVDS_A2+	A75	eDP_TX0+
LVDS_A2-	A76	eDP_TX0-
LVDS_A_CK+	A81	eDP_TX3+
LVDS_A_CK-	A82	eDP_TX3-
LVDS_VDD_EN	A77	eDP_VDD_EN
LVDS_BKLT_EN	B79	eDP_BKLT_EN
LVDS_I2C_CK	A83	eDP_AUX+
LVDS_I2C_DAT	A84	eDP_AUX-
LVDS_BKLT_CTRL	B83	eDP_BKLT_CTRL
RSVD	A87	eDP_HPD

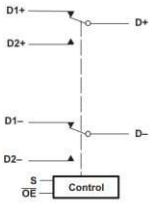
CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

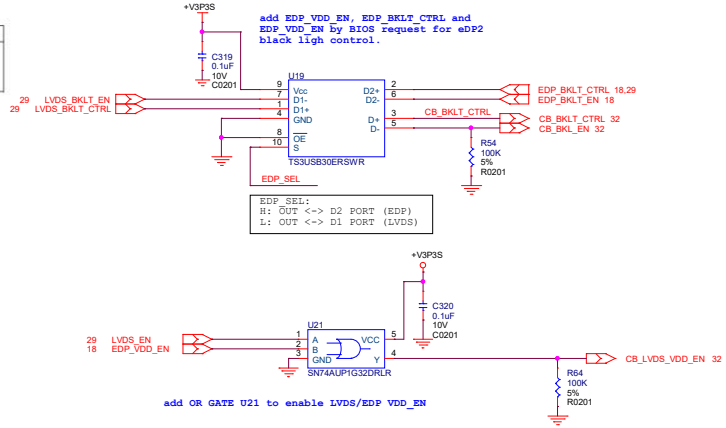
eDP / LVDS CONTROL SWITCH

TRUTH TABLE

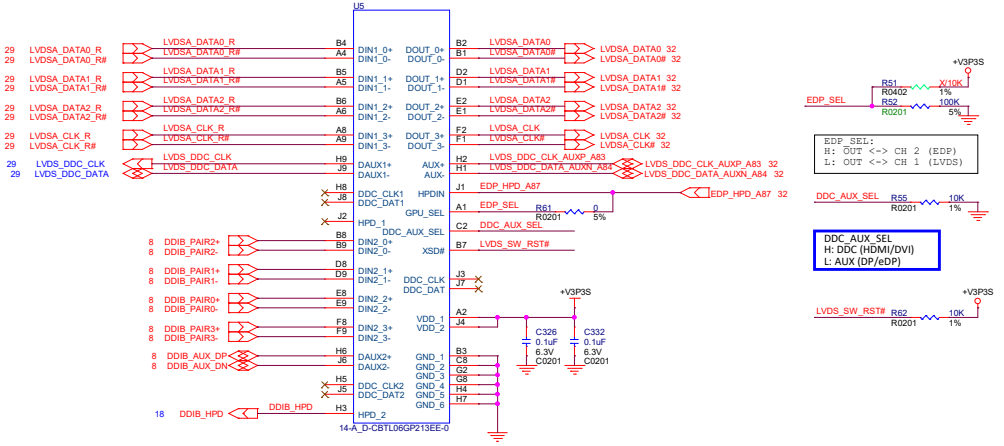
S	OE	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM





eDP to LVDS SWITCH



<Variant Name>

AAEON Technology INC.

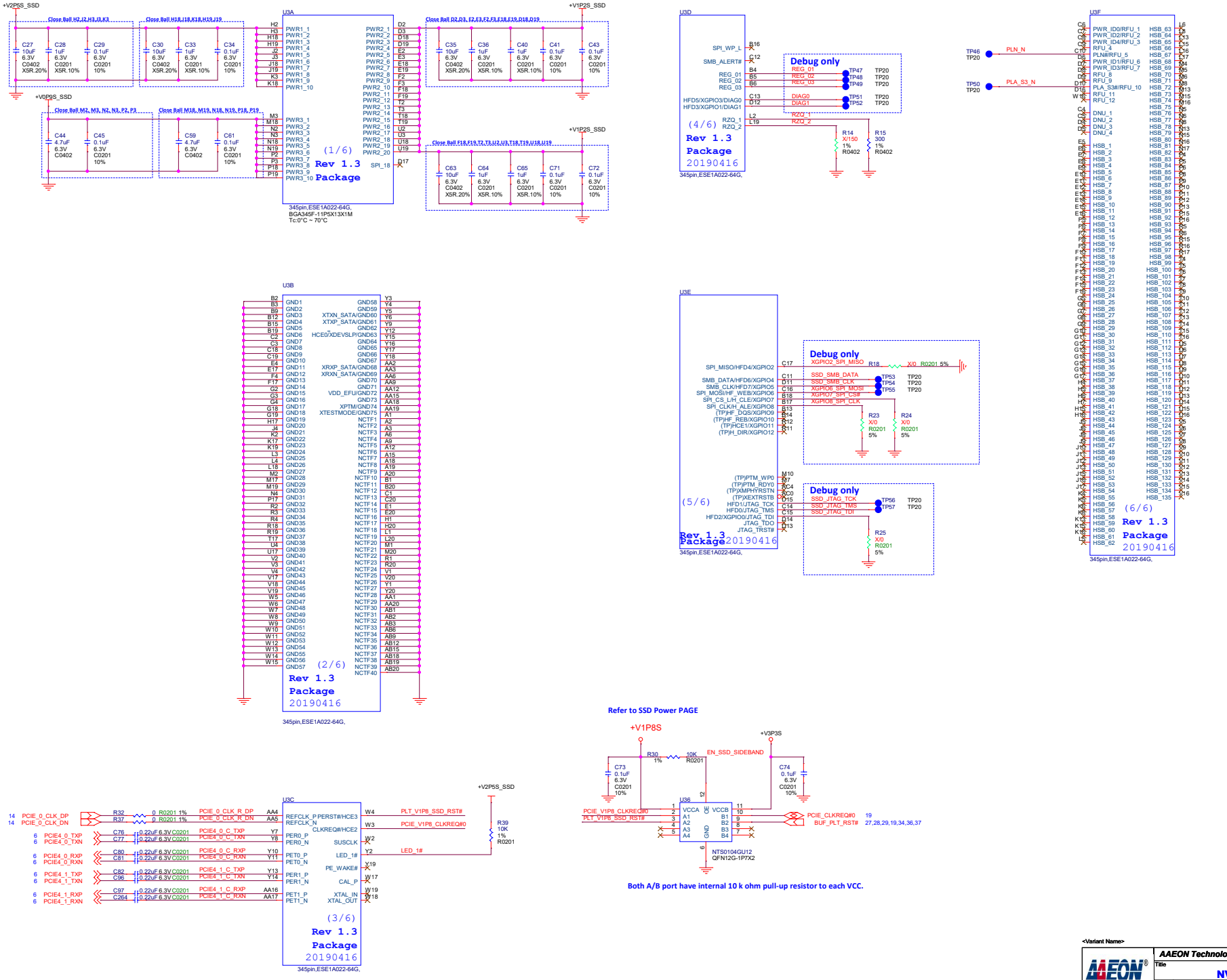
Title: eDP to LVDS

Size	Document Number	Rev
	COM-TGHB6	A0.1_0_0

Date: Friday, November 12, 2021 | Sheet 30 of 36

NVMe SSD

DNU: Do not use. Manufacturing purpose only
RFU: Reserved for future use



<Variant Name>

AAEON Technology INC.

Title	NVMe SSD	
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 31 of 51	

+5V @ 2A
+12V @ 19A
+VIN
DC-IN 12V Only
+V5ALW
+V3P3A_RTC

CB_STXD1X R11 R0201 10K 1%
CB_STXD2X R12 R0201 10K 1%
R11,R12 close to pin A98,,A101

To CB From EC FAN ctrl
To CB SPI only
To CB LPC only
To CB 2CH LVDS x1
To CB DDI to VGA x1
To CB USB2.0 x8 From PCH

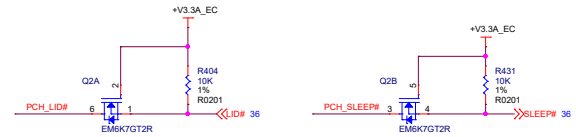
COMAB1
220P,180D,MALE,2357739-1,

To CB COM1(TX/RX only) From EC
To CB COM2(TX/RX only) From EC
To CB Intel I225 x1
To CB From PCH SATA x4
To CB From PCH HDA x1
To CB From EC DIO x8
EC PCH
EC I2C
PCH I2C
PCIE_RST 1 2
x4 IRST
x2
To CB PCIe x8
x2
x4 IRST
x2

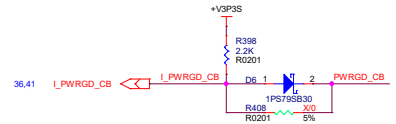
Type 6
RowA & DowB
PN = 1654M0000

COMAB1 P/N : 16540X0015

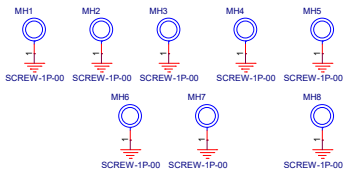
EC LID# & SLEEP#



Carry Board PWRGD



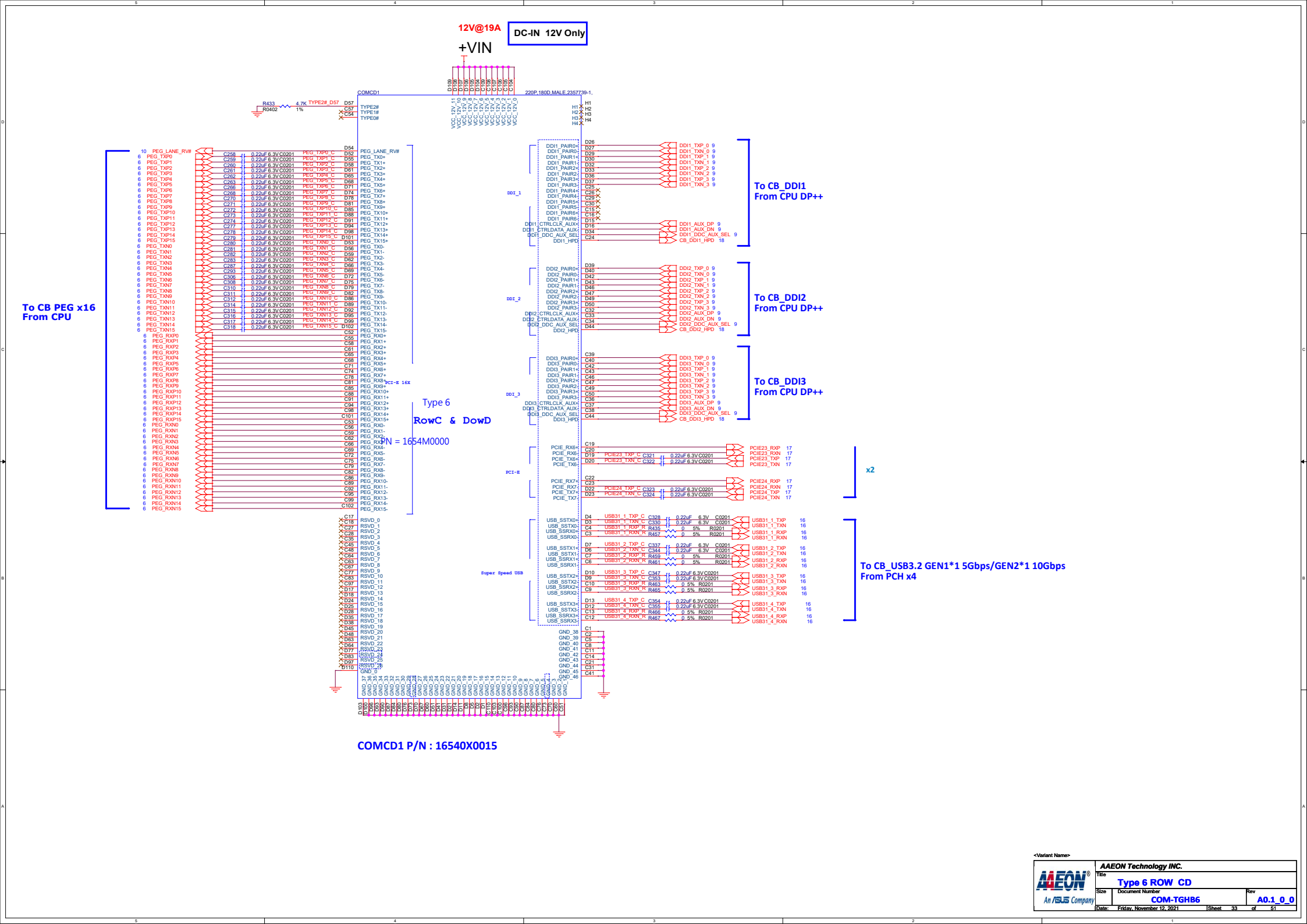
MH 1~5 COMe Standard
MH 6~8 Extra for SOC



<Variant Name>

AAEON Technology INC.
An ASUS Company

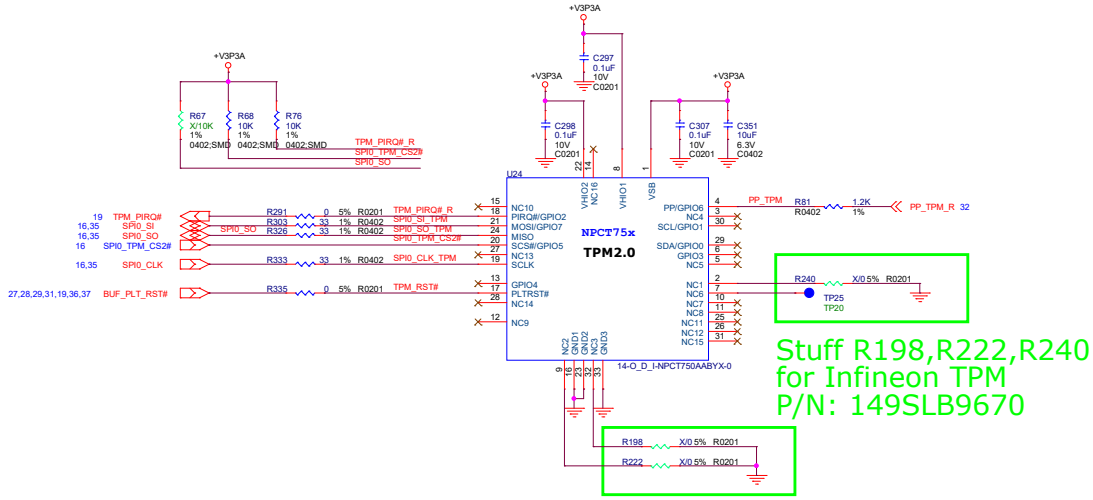
Title	Type 6 ROW AB
Size	Document Number: COM-TGHB6
Rev	A0.1_0_0
Date:	Friday, November 12, 2021
Sheet	32 of 51



<Variant Name>

AAEON Technology INC.		
Title: Type 6 ROW CD		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 33 of 51	

TPM(Option)



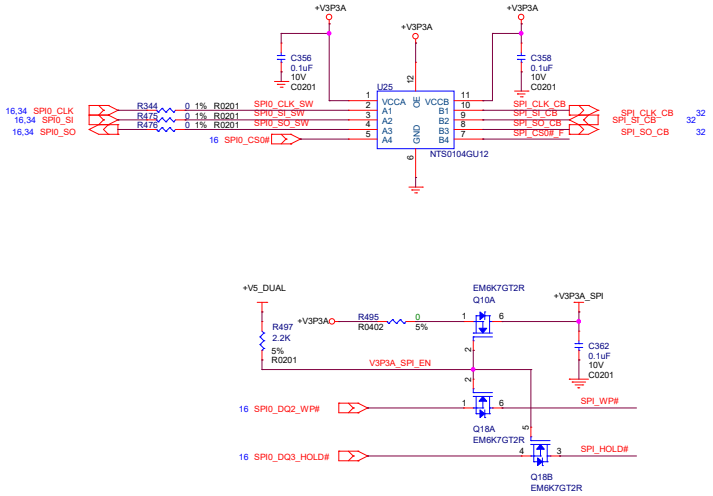
Stuff R198,R222,R240
for Infineon TPM
P/N: 149SLB9670

<Variant Name>

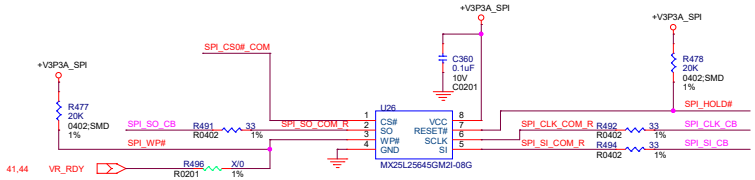
AAEON Technology INC.

Title: TPM		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 34 of 51	

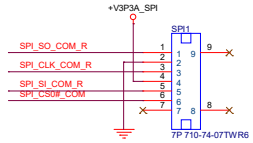
SPI ISO



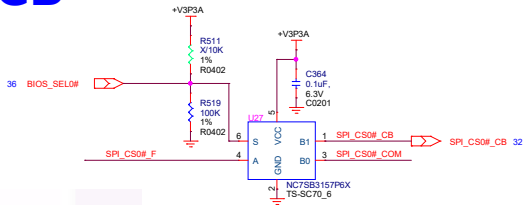
SPI ROM Flash Tool



1462002564 / (TF)IC.Flash Memory.256M Bit serial.SOP-8(209mil).w/ Dual & Quad SPI.SMD.MACRONIX.MX25L25645GM2I-08G



BIOS Switch MB/CB



Function Table

Input (S)	Function
Logic Level Low	B_0 Connected to A
Logic Level High	B_1 Connected to A

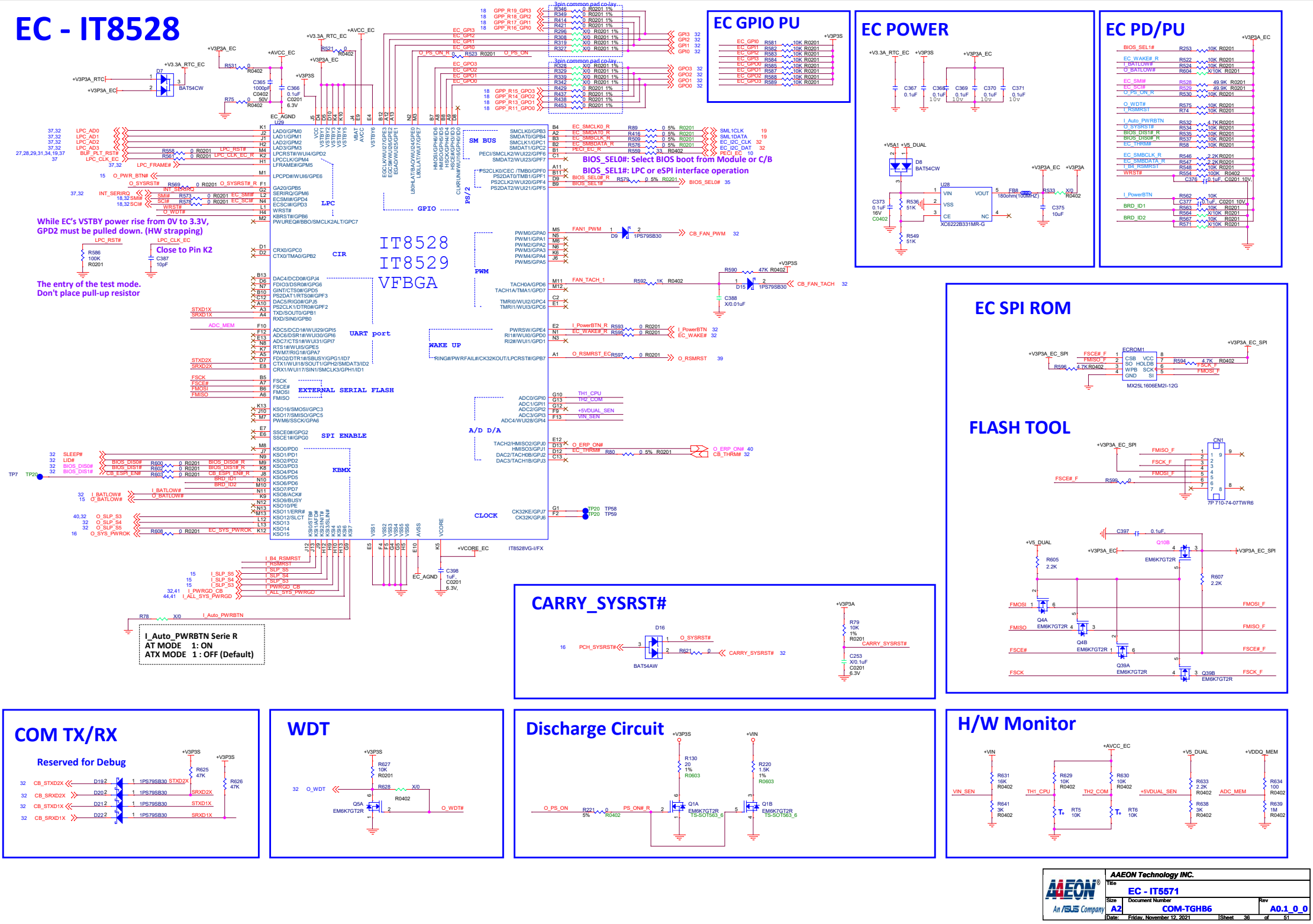
L: Module
H: Carrier

<Variant Name>

AAEON Technology INC.

Title: BIOS / Switch MB CB		
Size: A2	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 35 of 51	

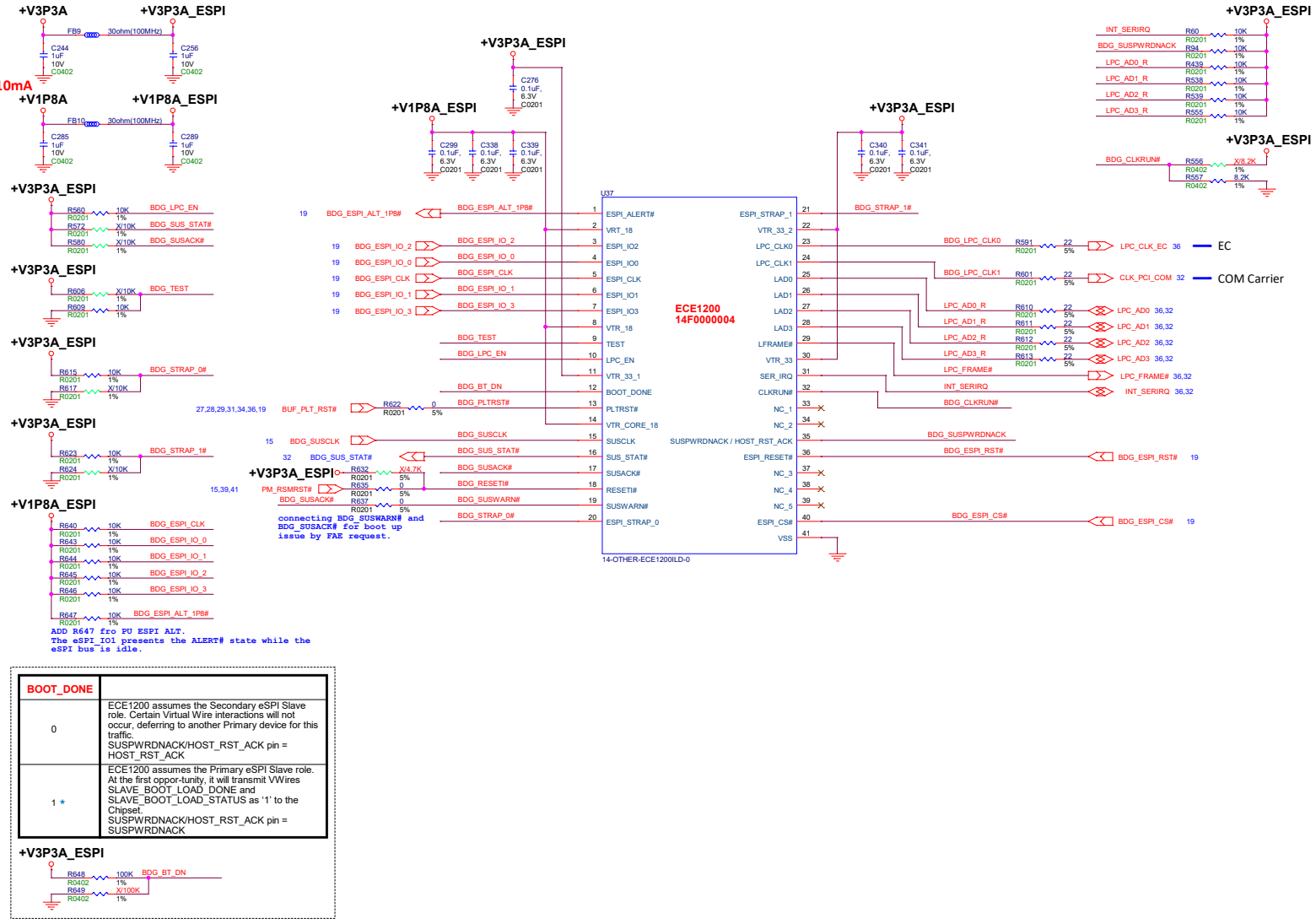
EC - IT8528



AAEON Technology INC.			
Title: EC - IT5571			
Size: A2	Document Number: COM-TGHB6		Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 36 of 51		

+3.3V @ 30mA

+1.8V @ 10mA



BOOT_DONE	
0	ECE1200 assumes the Secondary eSPI Slave role. Certain Virtual Wire interactions will not occur, deferring to another Primary device for this traffic. SUSPWRDNACK/HOST_RST_ACK pin = HOST_RST_ACK
1 *	ECE1200 assumes the Primary eSPI Slave role. At the first oppor-tunity, it will transmit VWires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS as '1' to the Chipset. SUSPWRDNACK/HOST_RST_ACK pin = SUSPWRDNACK

<Variant Name>

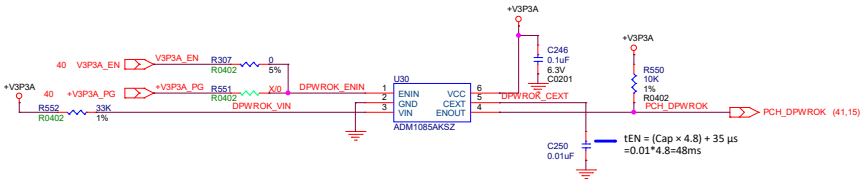
AAEON Technology INC.

Title: eSPI to LPC

Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0

Date: Friday, November 12, 2021 | Sheet 37 of 51

DSW_PWROK Control



3.3V x 10 / (10+33) = 0.767

ENIN VIH = 0.3*VCC+0.2 =1.19V

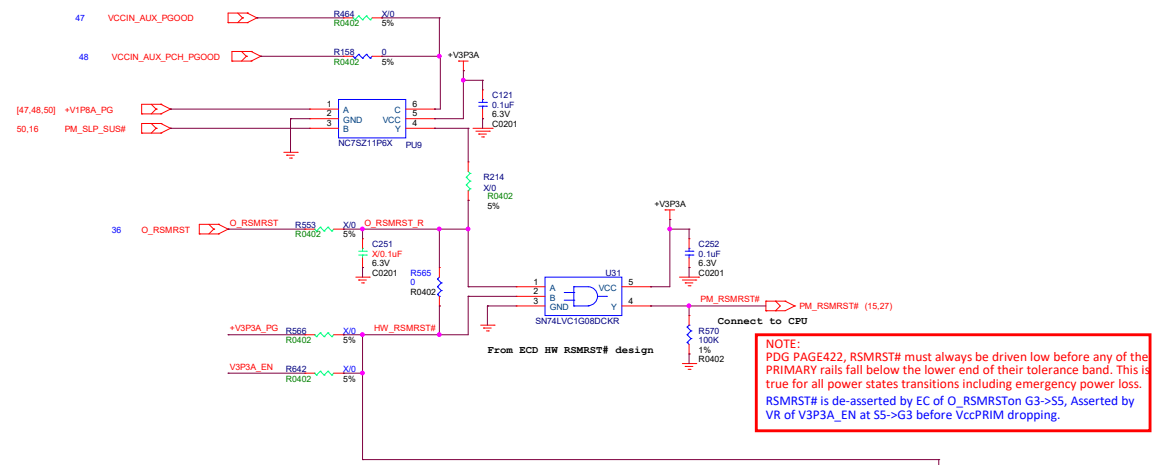
ENIN VIL = 0.3*VCC- 0.2 = 0.79V

ENOUT/ENOUT# Voltage Low (MAX =0.4V),When Vin < Vth_falling (ENOUT) / Vin > Vth_rising (ENOUT#)

Table 2.

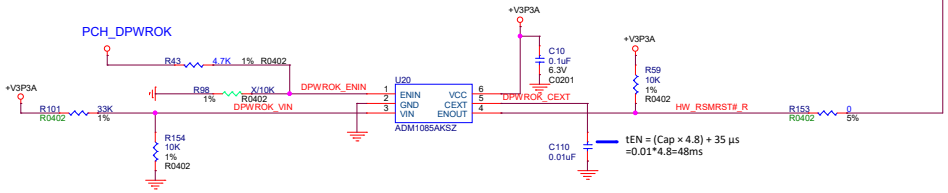
Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	2.25		3.6	V	
V_{IN} Operating Voltage Range	0		22	V	
Supply Current		10	15	µA	
V_{IN} Rising Threshold, V_{TH_RISING}	0.56	0.6	0.64	V	V_{CC} = 3.3 V
V_{IN} Falling Threshold, $V_{TH\_FALLING}$	0.545	0.585	0.625	V	V_{CC} = 3.3 V
V_{IN} Hysteresis		15		mV	

RSMRST# Control



NOTE:
PDG PAGE422, RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band. This is true for all power states transitions including emergency power loss.

RSMRST# is de-asserted by EC of O_RSMRSTon G3->S5, Asserted by VR of V3P3A_EN at S5->G3 before VccPRIM dropping.



3.3V x 10 / (10+33) = 0.767

ENIN VIH = 0.3*VCC+0.2 =1.19V

ENIN VIL = 0.3*VCC- 0.2 = 0.79V

ENOUT/ENOUT# Voltage Low (MAX =0.4V),When Vin < Vth_falling (ENOUT) / Vin > Vth_rising (ENOUT#)

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SUPPLY					
V_{CC} Operating Voltage Range	2.25		3.6	V	
V_{IN} Operating Voltage Range	0		22	V	
Supply Current		10	15	µA	
V_{IN} Rising Threshold, V_{TH_RISING}	0.56	0.6	0.64	V	V_{CC} = 3.3 V
V_{IN} Falling Threshold, $V_{TH\_FALLING}$	0.545	0.585	0.625	V	V_{CC} = 3.3 V
V_{IN} Hysteresis		15		mV	

<Variant Name>

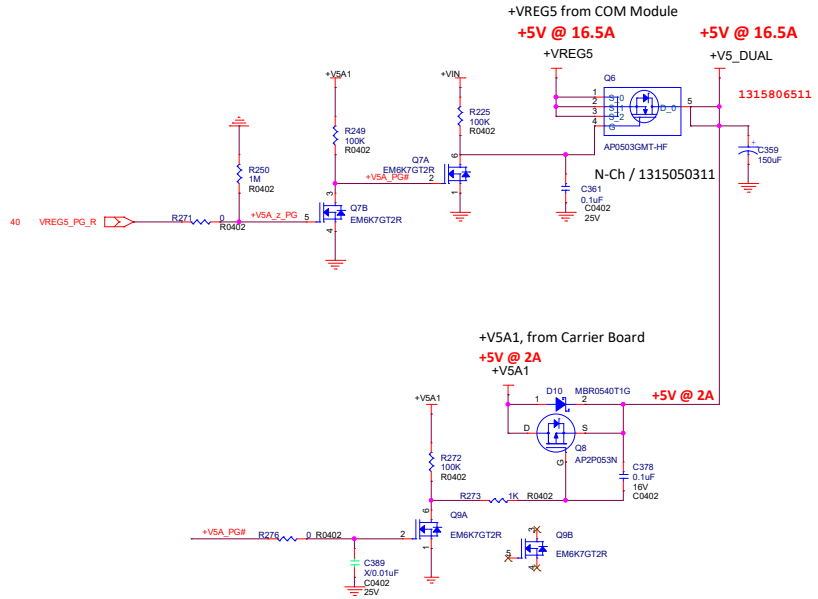
AAEON Technology INC.

Title: DSW_PWROK/RSMRST# Control

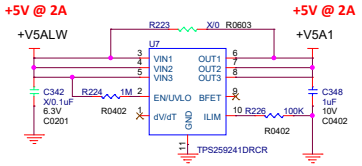
Size: | Document Number: COM-TGHB6 | Rev: A0.1_0_0

Date: Friday, November 12, 2021 | Sheet 38 of 51

+V5_DUAL Switch Circuit

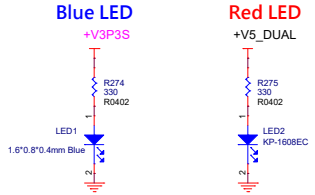


+V5ALW to +V5A1



Default: Undervoltage lockout set point = 4.3 V

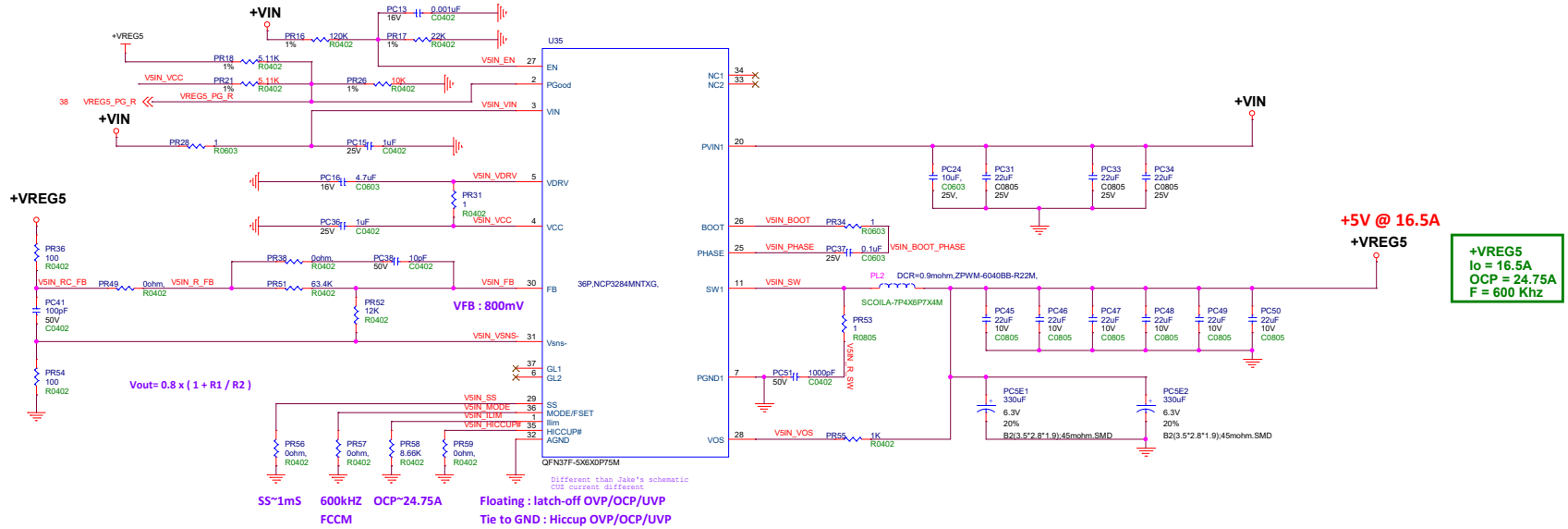
LED



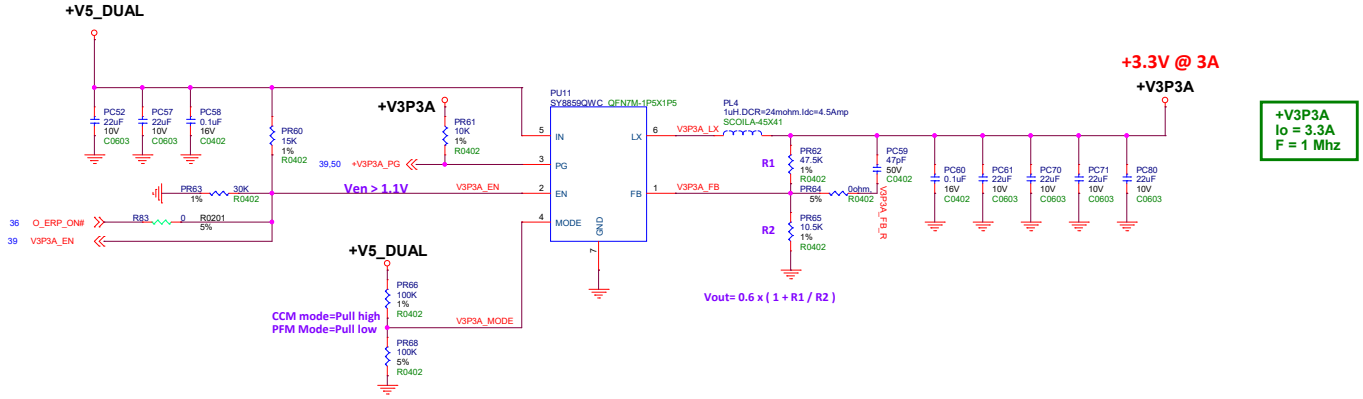
<Variant Name>

AAEON An ASUS Company	Title: +V5_Dual/ +V5A1/ LED	
Size: A2	Document Number: COM-TGHB6	Rev.: A0.1_0_0
Date: Friday, November 12, 2021	Sheet: 38 of 51	

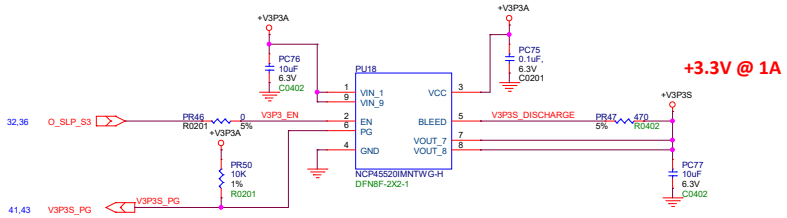
+V5A



+V3P3A

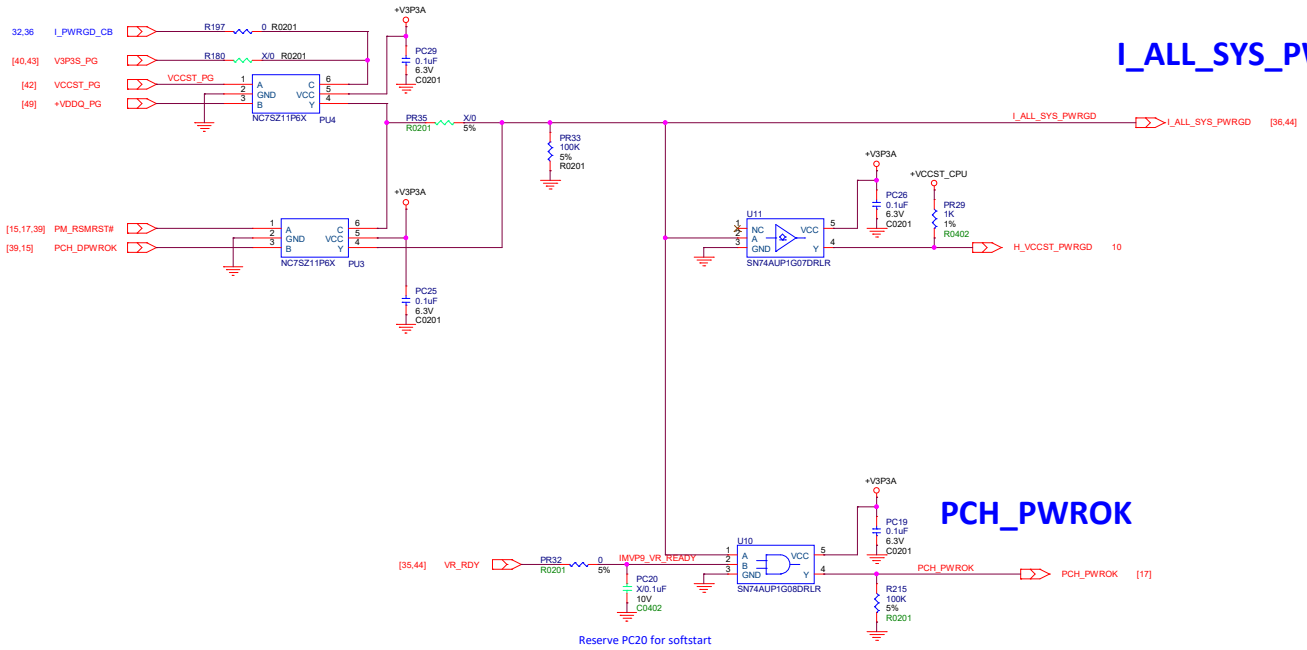


+V3P3S



AAEON Technology INC.			
Title: PWR_+VREG5 / +V3P3A / +V3P3S			
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0	
Date:	Sheet 40 of 51		

PWR SEQ CTRL

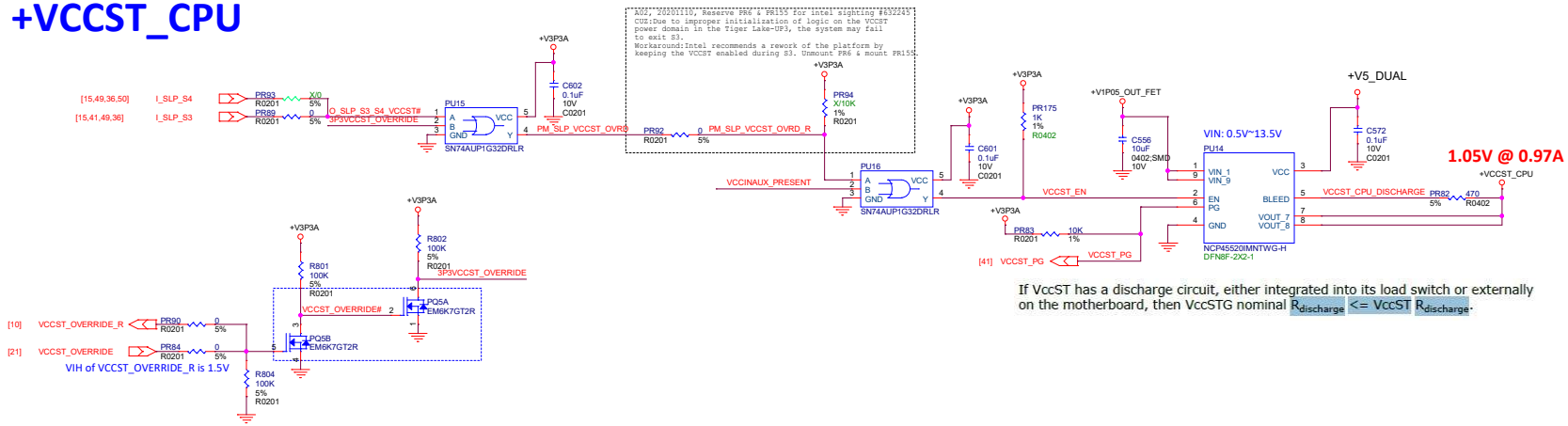


<Variant Name>

AAEON Technology INC.

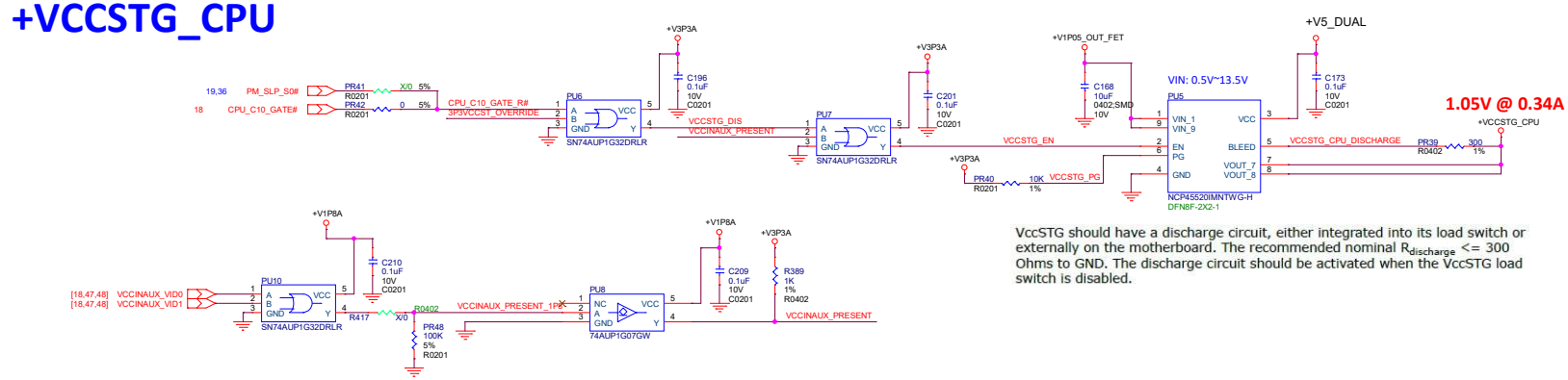
Title	PWR SEQ CTRL	
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date: Friday, November 12, 2021	Sheet 41 of 51	

+VCCST_CPU



If VccST has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal $R_{discharge}$ <= VccST $R_{discharge}$.

+VCCSTG_CPU



VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{discharge}$ <= 300 Ohms to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.

<Variant Name>

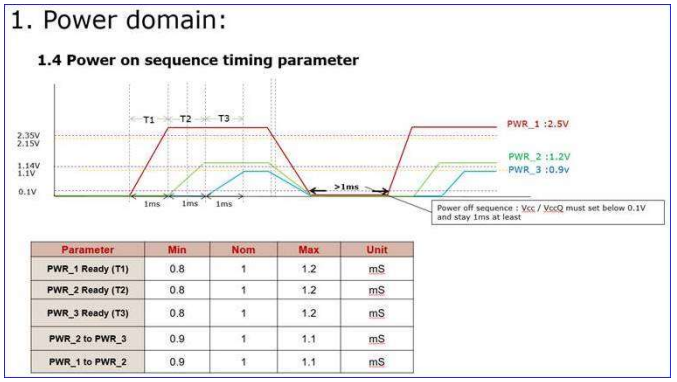
AAEON Technology INC.

Title: PWR_+VCCST_CPU/+VCCSTG_CPU

Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0

Date: Friday, November 12, 2021 | Sheet 42 of 51

PCIe SSD 3* PWR supply



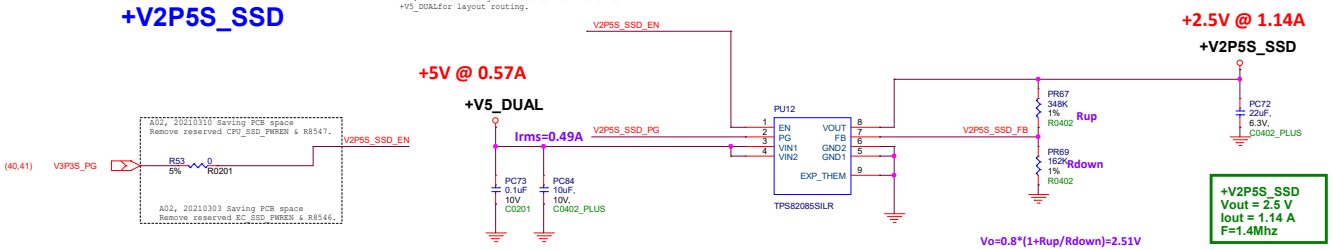
Parameter	Min	Nom	Max	Unit
PWR_1 Ready (T1)	0.8	1	1.2	mS
PWR_2 Ready (T2)	0.8	1	1.2	mS
PWR_3 Ready (T3)	0.8	1	1.2	mS
PWR_2 to PWR_3	0.9	1	1.1	mS
PWR_1 to PWR_2	0.9	1	1.1	mS

+V2P5S_SSD

A02, 20210310 Saving PCB space
CUZ PM adding more spec modification, must narrow 3 PCIe SSD PWR (2.5V/1.2V/0.9V) to saving more PCB space.
Remove whole PCIe SSD PWR circuit to add whole New 3 * Buck ciruits (PU33/PU34/PU35).

20201029 A02 Vendor update PWR consumption spec
20210303 A02 Support 512GB for PM spec update
Change Max. current from 0.588 to 1.14A.

A02, 20210312 Change PWR source from +V3P3A to +V5_DUALfor layout routing.

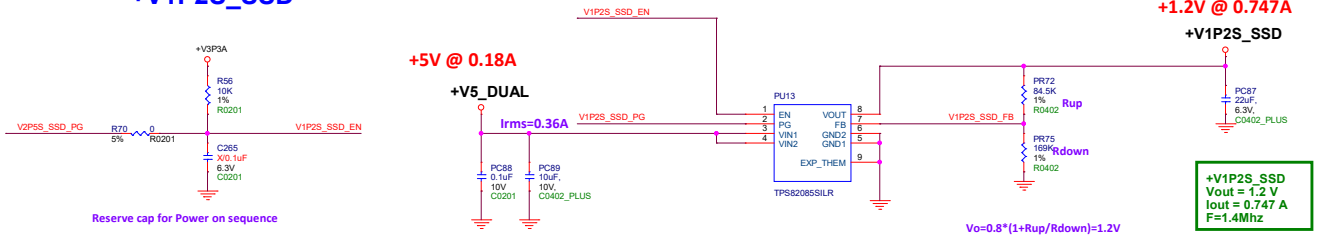


Vendor update PWR consumption spec
Support 512GB for PM spec update
+V2P5S_SSD change Max. current from 0.588 to 0.747A.
+V1P2S_SSD change Max. current from 0.588 to 1.14A.
+V0P9S_SSD change Max. current from 0.664 to 0.996A

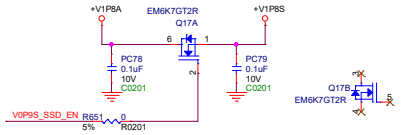
+V1P2S_SSD

A02, 20210312 Change PWR source from +V3P3A to +V5_DUALfor layout routing.

20201029 A02 Vendor update PWR consumption spec
20210303 A02 Support 512GB for PM spec update
Change Max. current from 0.588 to 0.747A.

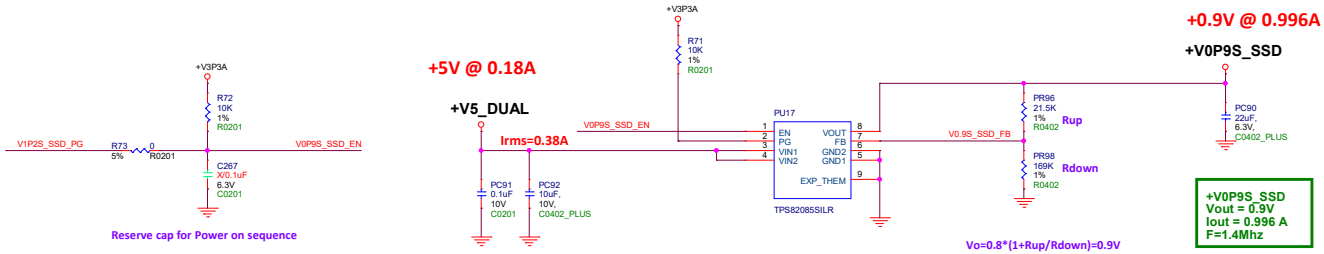


For PCIe SSD 1 Pull high and One Level-shifter use



+V0P9S_SSD

20201029 A02 Vendor update PWR consumption spec
20210303 A02 Support 512GB for PM spec update
Change Max. current from 0.664 to 0.996A



<Variant Name>

AAEON Technology INC.

Title	PWR_+V2P5S/+V1P2S/+V0P9S_SSD	
Size	Document Number	Rev
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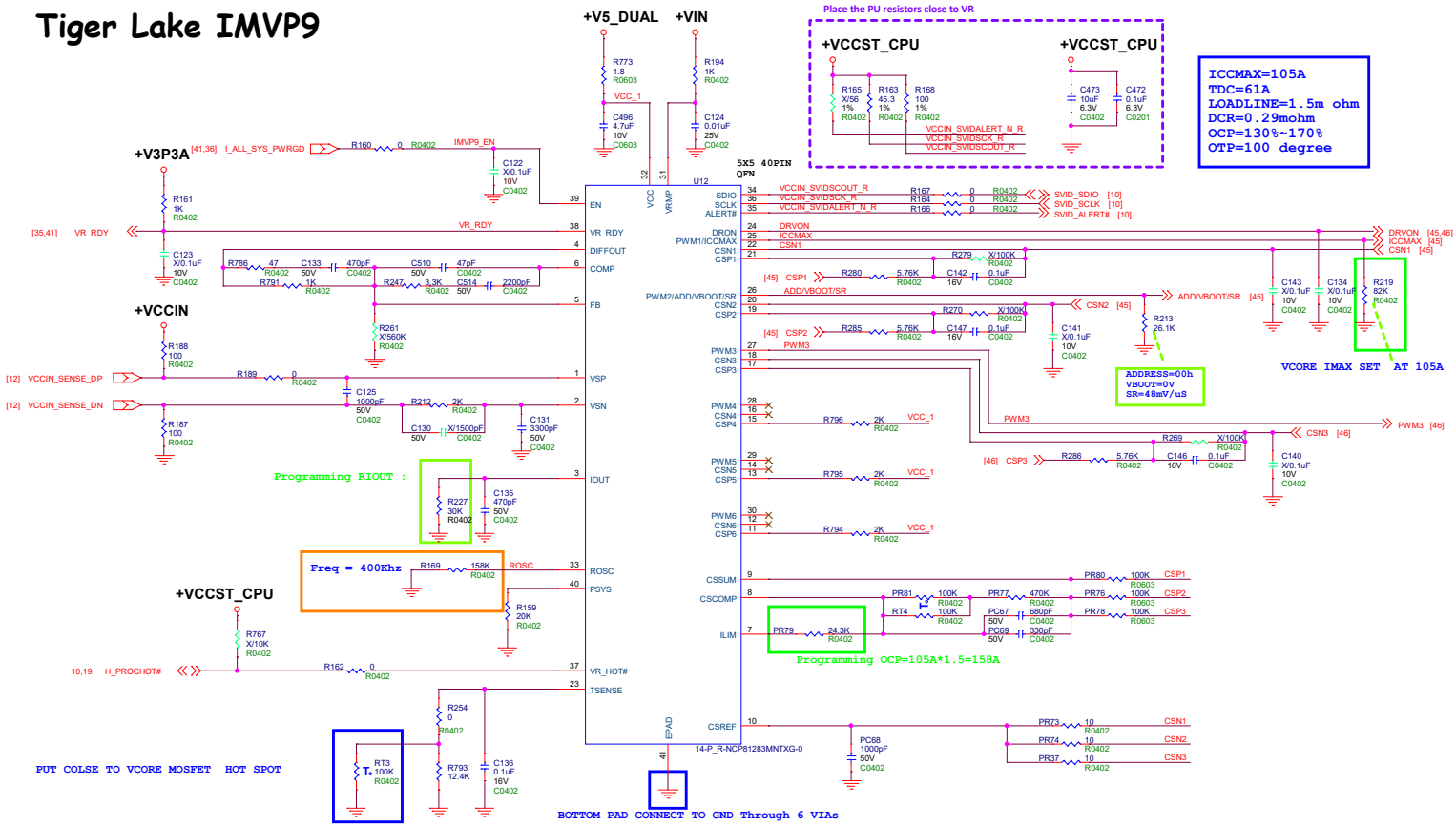
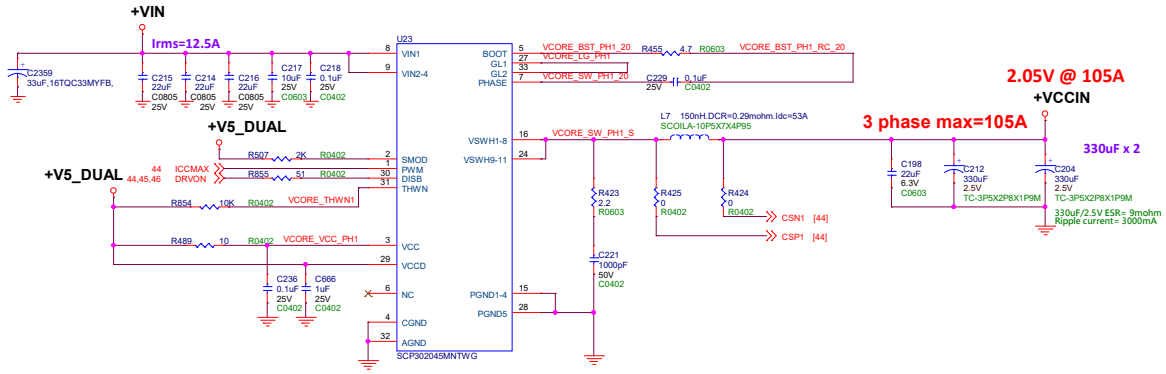
Date: Friday, November 12, 2021	Sheet 43 of 51	

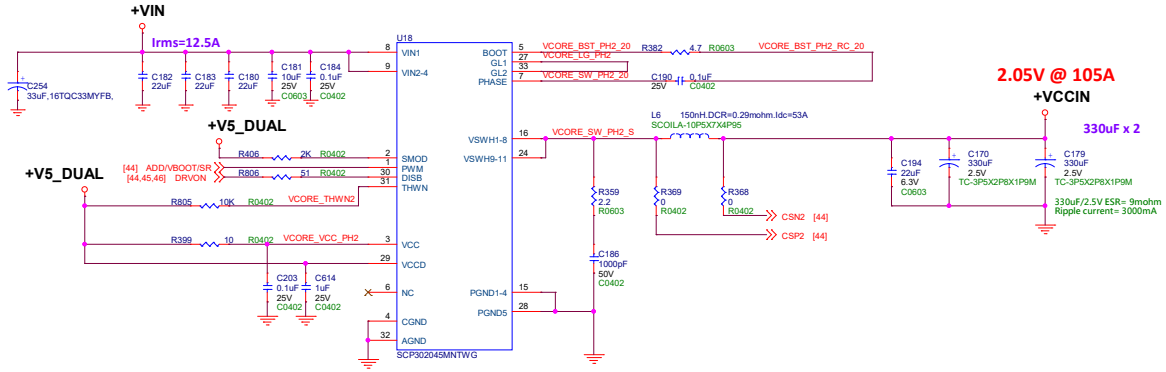
Tiger Lake IMVP9



AAEON Technology INC.	
Title	PWR_IMVP9 Controller
Size	Document Number: COM-TGHB6
Rev	A0.1_0_0
Date:	Sheet 44 of 51

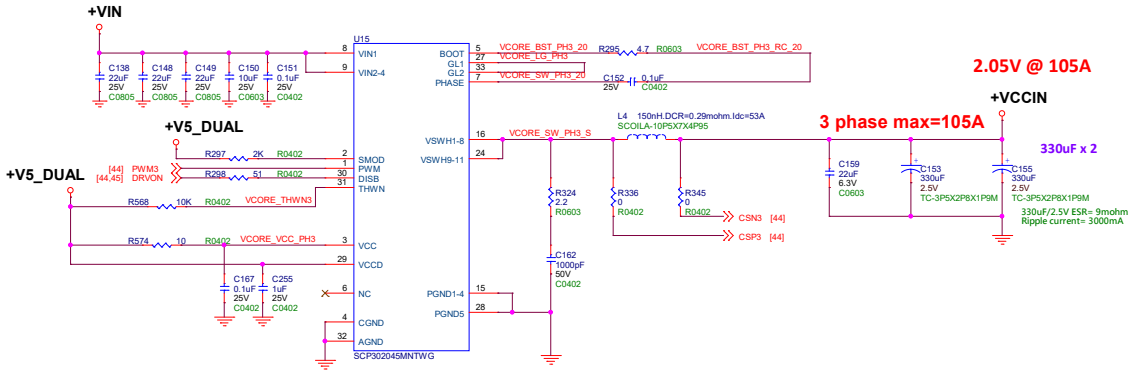
+VCCIN





AAEON Technology INC.		
Title: PWR_+VCCIN		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date:	Sheet 45 of 51	

+VCCIN



Reference the document : 618429_TGL_H_PowerMap_Rev1p5

Tiger Lake-H Processor Line(45 W) 8-Core GT1 design	
PL2(A)	109W
PL4(A)	196W

Reference the document : 575683-tgl-eds-vol1-rev1p4(Page150)

+VCCIN (3ph)	H- Processor Line
ICCMAX(A)	105A
IPL2(A)	61A
Operating Voltage	2.05V
DC_LL/ AC_LL3 (mohm)	1.5mohm / 1.7mohm
DCR	0.29mohm
OCP	105A*150%=158A
OTP	100 Degree
Ripple Tolerance	±15 mv
TOBvcc (PS0, PS1)	±20 mv
VccIN VBoot setting	0V
Reference the document : 618429_TGL_H_ PlatformDoc_Rev1.5(Page386)	

EA:Iload(max)*130%~Iload(max)*170%.

EA Output regulation and ripple
Ripple criteria =±15 mv =30mv

EA transient : Ilow = 25%*Imax A, Ihigh = 100%*Imax A
transient ovs/uvs criteria= ((Imax-Ilow)*DC_LL)+TOBvcc
= ((105A-26.25A)*1.5)+40=198 mv

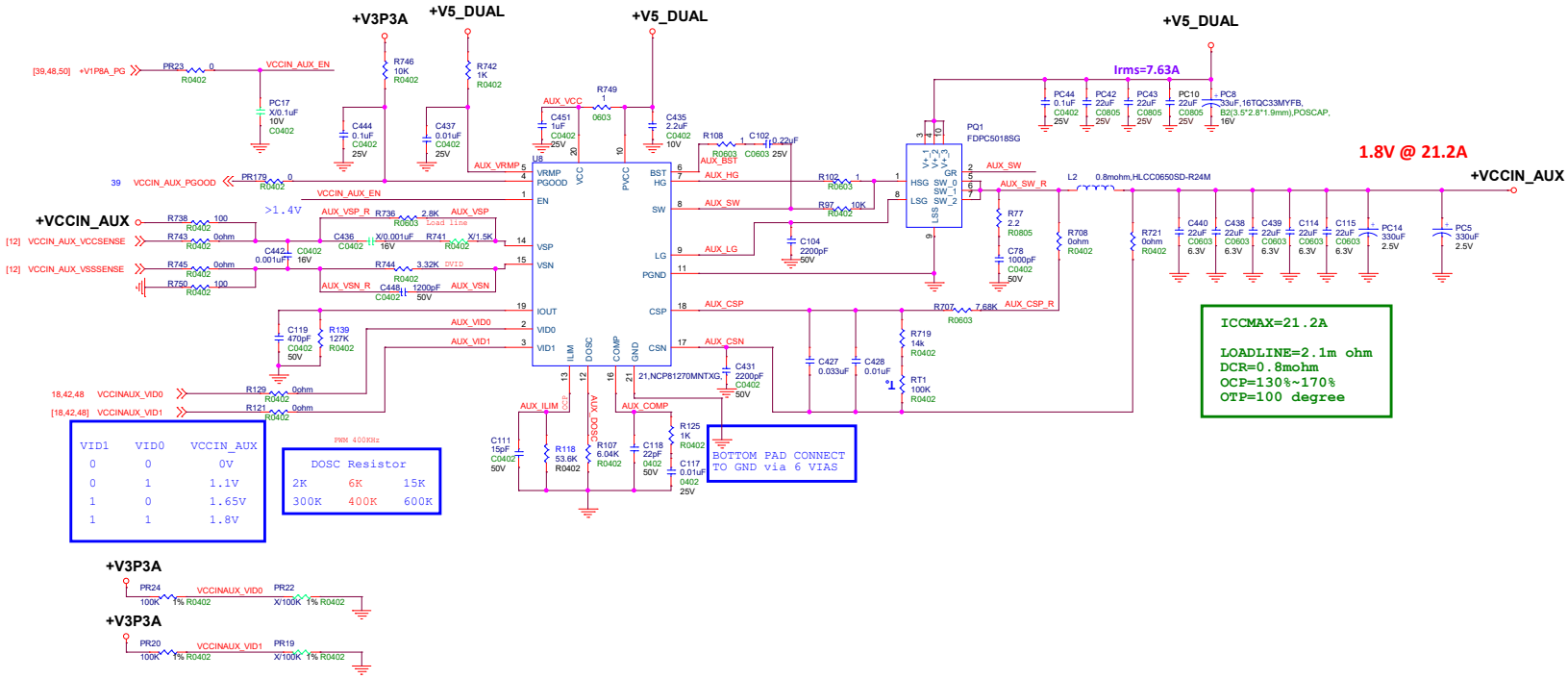
+VCCIN_AUX (1ph)	H- Processor Line
ICCMAX(A)	27A
IPL2(A)	
Operating Voltage	1.8V
DC_LL/ AC_LL3 (mohm)	2.1mohm / 4mohm
DCR	0.8mohm
OCP	27A*150%=40.5A
Ripple Tolerance	TBD if no use 1.8v*3%
TOBvcc (AC+DC)	-5%/ +10 %

EA:Iload(max)*130%~Iload(max)*170%.

EA Output regulation and ripple
Ripple criteria =1.8v*3%=54 mv

EA transient :
transient ov/uv criteria= TOBvcc (AC+DC)=-5%~+10%
=1.8*total_15%=270 mv

+VCCIN_AUX



Company	AAEON Technology INC.
Title	PWR_+VCCIN_AUX
Size	
Document Number	COM-TGHB6
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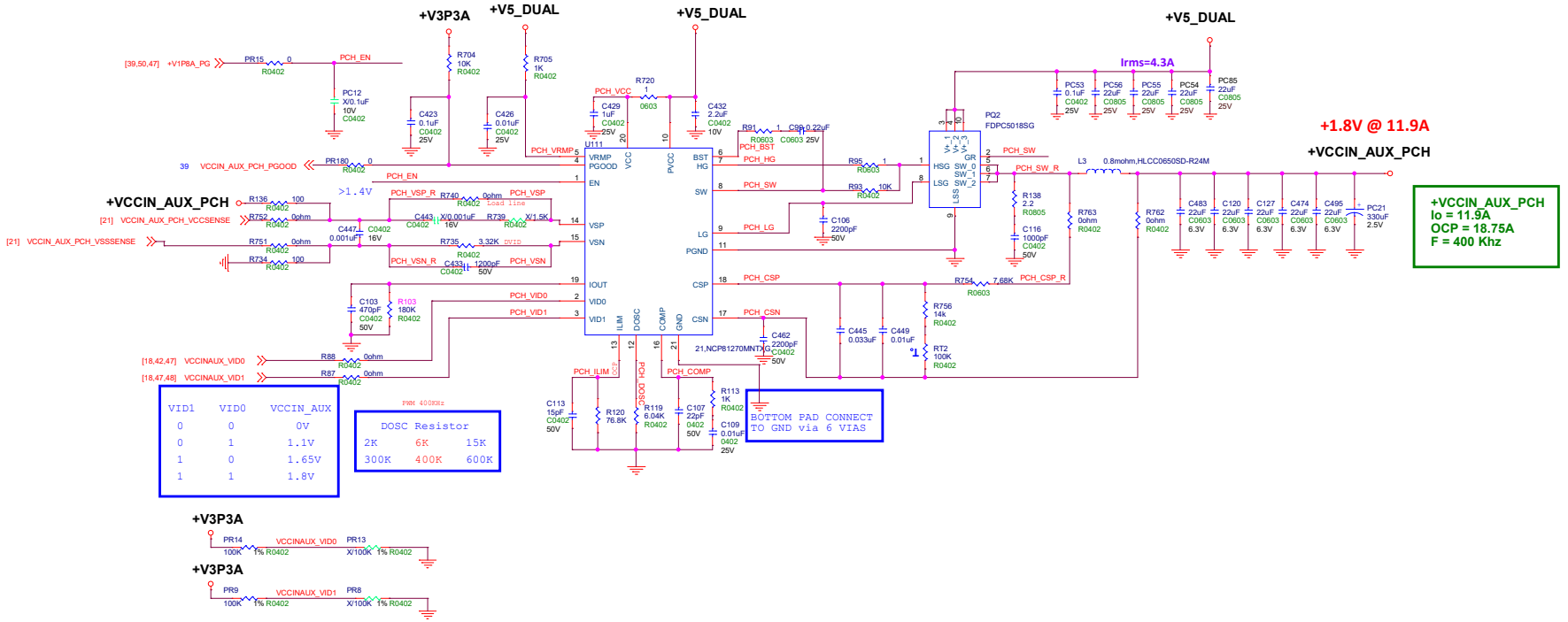
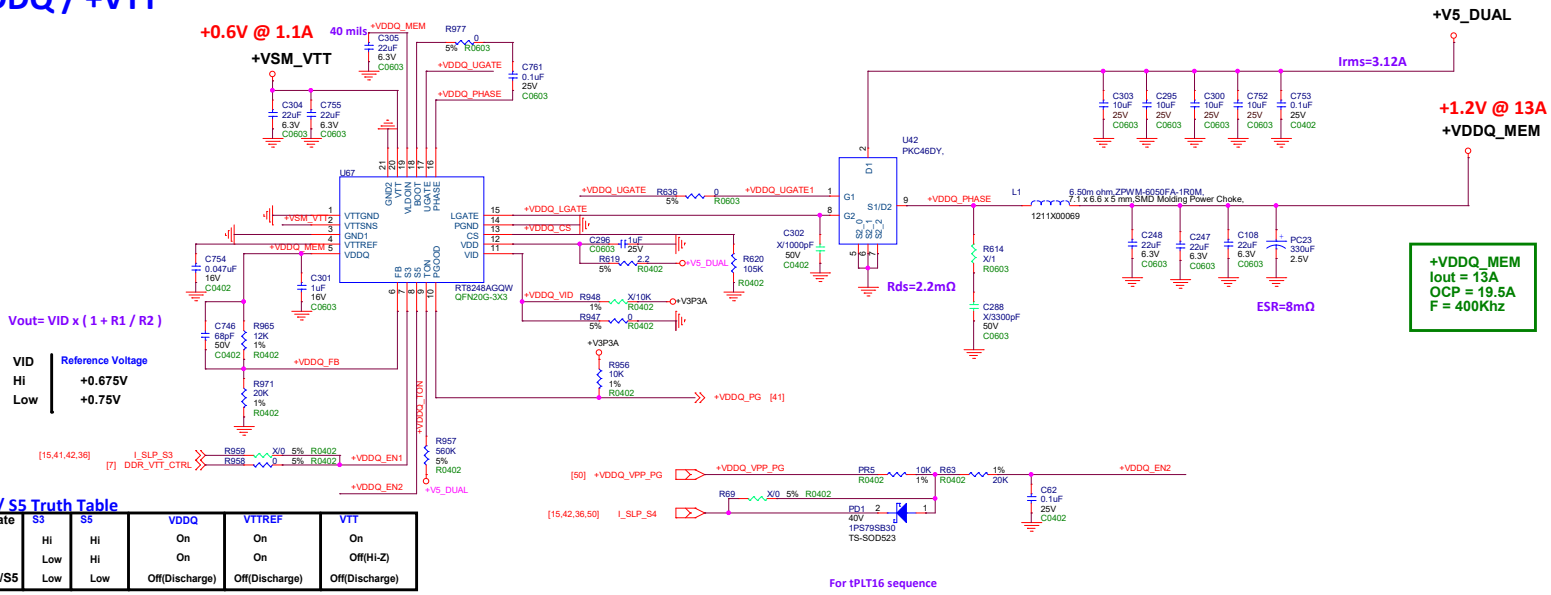
+VCCIN_AUX_PCH



AAEON Technology INC.		
Title: PWR_+VCCIN_AUX_PCH		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date:	Sheet 48 of 51	

+VDDQ / +VTT



S3 / S5 Truth Table

State	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off(Hi-Z)
S4/S5	Low	Low	Off(Discharge)	Off(Discharge)	Off(Discharge)

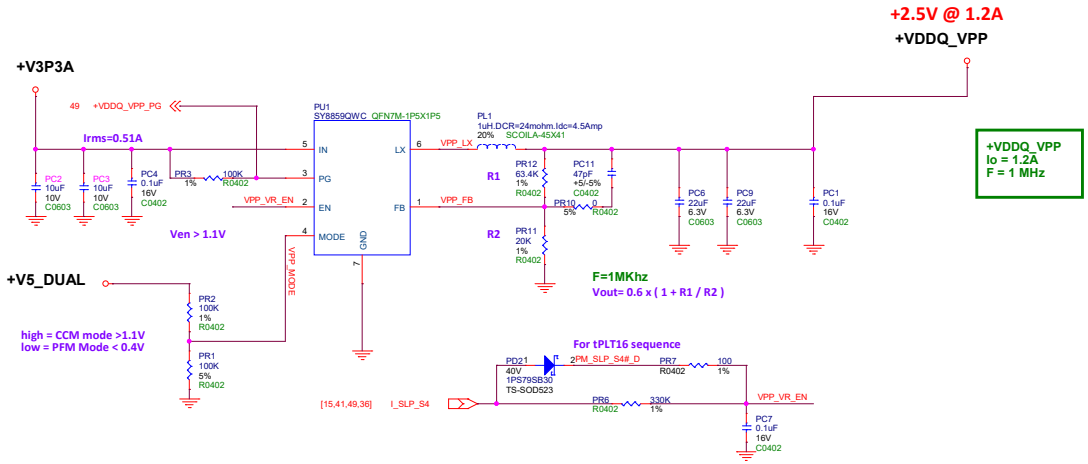
AAEON Technology INC.

Title: PWR_+VDDQ / +VTT / +V3P3SB

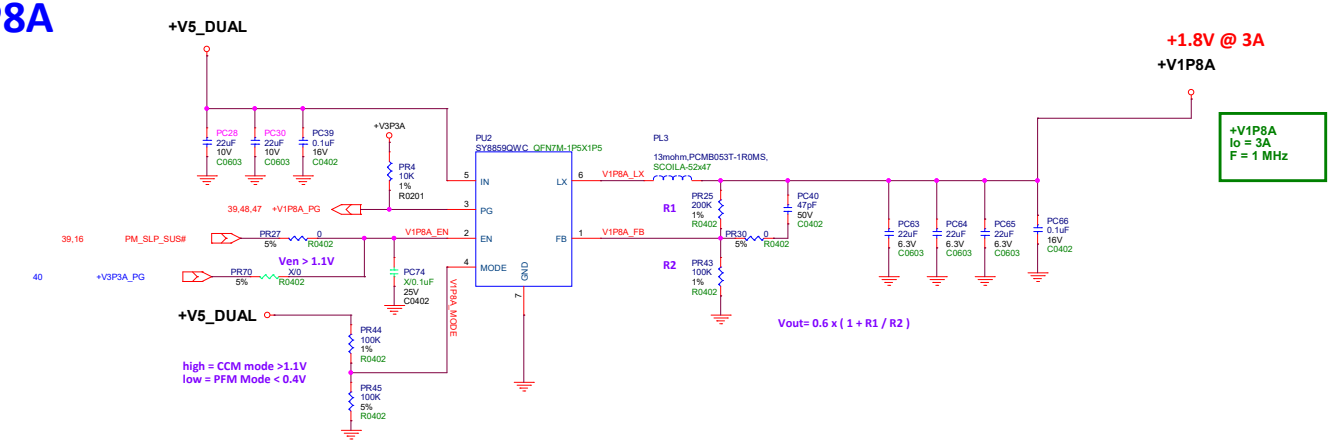
Size | Document Number: COM-TGHB6 | Rev: A0.1_0_0

Date: | Sheet 49 of 51

+VDDQ_VPP



+V1P8A



AAEON Technology INC.		
Title: PWR_+VDDQ_VPP / +V1P8A		
Size	Document Number: COM-TGHB6	Rev: A0.1_0_0
Date:	Sheet 50 of 51	

HISTORY-1

Date	Revision	Page	Issue Description	Solution Description
2021/06/27	A0.1	X	First Release	First Release
2021/08/09	A0.1	7	U14.B pin AM9,AR9 net_name reverse for DDR1_ODT[1:0]	exchange M_B_DIM0_ODT0 & M_B_DIM0_ODT1
	A0.1	7	U34/74AUP1G07GW VCC impact TGU S4 wake fail	add Q3A,Q5B for DDR_VTT_CTRL ,as the same WHL-U
2021/08/13	A0.1	19	BUF_PLT_RST# no PD	add R186 100K for BUF_PLT_RST#
2021/08/17	A0.1	34,35	SPI series R no follow PDG SPEC	R492,R494,R491,R303,R326,R333 from 56R change to 33R .
	A0.1	23,24,25,26	BIOS stop 55	C42,C589,C401,C579 to empty
	A0.1	41	reserved I_PWRGD_CB logic ctrl	I_ALL_SYS_PWRGD logic ctrl ,add R197,R180 to PU4
2021/08/18	A0.1	34	U24 TPM add co-lay Infineon TPM	add R198,R222,R240(Default empty)
	A0.1	50	Reserved +V1P8A EN Ctrl by +V3P3A_PG	add PR70 0R(Default empty)
	A0.1	39	RSMRST# Power down Sequence modify	R43 PU Voltage from +V1P8A to DSW_PWROK
	A0.1	40	Reserved +V3P3A EN Ctrl by VREG5_PG_R	add R282 0R
	A0.1	36	stuff C388 impact FAN_TACH waveform	C388 to empty
	A0.1	47	Power vendor review	add PC5 330uF
	A0.1	47	Power vendor review R139 IOUT = 21.2A / R118 ILIM = 32A	R139 100K to 127K , R118 43K to 53.6k
2021/09/02	A0.1	25,26	SO-DIMM swap for Layout placement	CN9 CN40 Swap pin7,16,17,21,20
2021/09/07	A0.1	36	EC suggest eSPI Bridge confiruration compatibility modify	U29(EC IC) from IT5571VG-I -> IT8528VG-I/FX
2021/09/08	A0.1	18	SMI# SCI# signal repeat	delete R26,R3
2021/09/10	A0.1	27	U109 LAN MDI+- net_name reverse error .	exchange MDI + /- signal
	A0.1	17	Carrier RTC design modify	add R3 , part size change(0402->0201) for R432,R418,R82
	A0.1	28	Design modify for DP to VGA AUX PU/PD	follow internal circuit remove R20,21,28,29
2021/11/12	A0.1	49	U42 EOL for VDDQ MOS	U42 from 1315C50DY0 PKC50DY ->1315Q00032 PKC46DY
	A0.1	x	x	x
	A0.1	x	x	x

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