01	INDEX	21	eDP	41	PMIC_TPS650941 (1/2)	
02	BLOCK DIAGRAM	22	M.2_2230_E-KEY	42	PMIC_TPS650941 (2/2)	
03	POWER TREE	23	mini PCIE	43	system power	
04	POWER SEQUENCE	24	SATA	44	Mechanical Component	
05	EXHAT, HAT40 pin define	25	USB3.0_OTG	45	HISTORY	
06	CPLD pin define	26	USB3.0_TYPE-A (1/2)			
07	SOC_DDR	27	USB3.0_TYPE-A (2/2)			
08	SOC_DISPLAY	28	USB PIN HEADER			
09	SOC_SATA_PCIE_USB	29	FAN			
10	SOC_GND	30	RTL8111G-CG_LAN1			
11	SOC_LPC_SPI_EMMC_SD	31	RTL8111G-CG_LAN2			
12	SOC_SMBUS_GPIO	32	DP+HDMI			
13	SOC_CLK_PCU_RTC	33	HDMI_port1			
14	SOC_POWER I	34	eMMC			
15	SOC_POWER II	35	SPI flash			
16	LPDDR4 (1/4)	36	HAT			
17	LPDDR4 (2/4)	37	EXHAT			
18	LPDDR4 (3/4)	38	CPLD			
19	LPDDR4 (4/4)	39	DCIN & 5V			
20	MIPI CAMERA	40	SYSTEM 3.3V			

UP-APL01

Project Code: D160807

AAEON ®
an ASUS assoc. co.

Title
Index

Size	Document Number	Rev:
A	UP-APL01	A0.3

Date: *Wednesday, January 04, 2017* Sheet: **1** of **45**

UP-SQUARE - APOLLO LAKE

DC INPUT: 5V

LPDDR4 2400MHZ

Ctrl/Progarm

POWER BUTTON
RESET

2GB (2ICs)	
2GB (2ICs)	

1x64b

2GB (2ICs)	
2GB (2ICs)	

1x64b

Apollo Lake

E3930
E3940
E3950

31mm x 24mm

eMMC
32GB

eMMC

Flash ROM
with header

Fast SPI

Realtek
8111G

PCIe PORT1

Realtek
8111G

PCIe PORT2

DUAL RJ45
STACK Connector

I2Sx2
PMWx3
UARTx1
GPIO

LPC
SPIx2
I2Cx4
JTAG

ALTERA
MAX10

F/W UPDATE
CONNECTOR

CEC

GPIO x22

I2Sx1
PMWx2
UARTx1
GPIO
SPIx2
I2Cx2

HAT 40 PIN
2*20 Header

I2Cx2
DMICx3
SD

EXHAT
2*30

SPI

ADC
ADC124S101

ADC

Display port
DP 1.2 4096x2160

DDI0

PWM2

FAN CONN

DP+HDMI
STACK Connector

HDMI TYPE A
HDMI 1.4b 3840x2160

DDI1

CEC

USB2.0 PORT 0
USB3.0 PORT 0

USB3.0
MICRO B
OTG

hi-speed conn
41 PIN

eDP
with
Back light control

USB3.0 PORT 1,2

USB2.0 PORT 1,2

USB TYPE A - 1
dual stack connector

hi-speed conn
21 PIN

MIPI DPHY1.1

hi-speed conn
31 PIN

MIPI DPHY1.2

USB3.0 PORT 3

USB2.0 PORT 3

USB TYPE A - 2
single stack connector

M.2
2230 E-KEY

USB2.0 PORT 4

PCIE PORT 3

SATA (PORT 1)

PCIE PORT0

CBTL02042ABQ

SATA & PCIE

mini PCIE
full size

USB2.0 PORT 5

SATA (PORT 0

SATA Gen3 x1

USB2.0 PORT 6,7

UART PORT 0

1O PIN HEADER

POWER TREE

DC Jack

5V	+VIN_EXT 5V	
	8A	

PROTECT CIRCUIT +V5A

EN: +V5A

MP8762 5V → +V3.3A
6A
3.3V / 6A

LDO YT9110 3.3V → +V2P8_CAM — 2.8V / 0.3A
EN: +V3.3S

LDO YT9110 3.3V → +V1P8_CAM — 1.8V / 0.1A
EN: +V2P8_CAM

LDO YT9110 3.3V → +V1P2_CAM — 1.2V / 0.2A
+V1P8_CAM

LDO YT9110 3.3V → +V1.5A — 1.5V
EN: +V3.3A

boost MP3425 5V → +VSYS — 5.8V / 0.3A
EN: +V5A

TPS650940 BUCK2 5V → +VCGI_SVID — 0.5~1.45V / 21A
EN: PMIC

TPS650940 BUCK6 5V → +VDDQ — 1.1V / 6A
EN: PMIC

TPS650940 LDO 1.1V → +VDDQ_VTT — 0.55V / 0.5A
EN: PMIC

EN: +V5ALDO_PMIC

PMOS

TPS650940 BUCK1 5V → +VNN_SVID — 0.5~1.45V / 4.82A
EN: PMIC

TPS650940 BUCK3 5V → +V1.05S — 1.05V / 2.7A
EN: PMIC

TPS650940 BUCK4 5V → +V1.8A — 1.8V / 0.4A
EN: PMIC

TPS650940 BUCK5 5V → +V1.24A — 1.24V / 1.8A
EN: PMIC

Figure 4-1. Apollo Lake G3 Cold Boot Power-Up
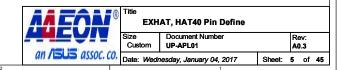
EXHAT

Panasonic AXK6S60547YG

MAX10 GPIO/LVDS port	GPIO/EXHAT_LVDS0n	1	2	GPIO/EXHAT_LVDS1n	MAX10 GPIO/LVDS port
	GPIO/EXHAT_LVDS0p	3	4	GPIO/EXHAT_LVDS1p	
	GND	5	6	GND	
	GPIO/EXHAT_LVDS2n	7	8	GPIO/EXHAT_LVDS3n	
	GPIO/EXHAT_LVDS2p	9	10	GPIO/EXHAT_LVDS3p	
	GND	11	12	GND	
	GPIO/EXHAT_LVDS4n	13	14	GPIO/EXHAT_LVDS5n	
	GPIO/EXHAT_LVDS4p	15	16	GPIO/EXHAT_LVDS5p	
	GND	17	18	GND	
	GPIO/EXHAT_LVDS6n	19	20	GPIO/EXHAT_LVDS7n	
	GPIO/EXHAT_LVDS6p	21	22	GPIO/EXHAT_LVDS7p	
	GND	23	24	GND	
	GPIO/EXHAT_PLL1_INn	25	26	GPIO/EXHAT_PLL1_OUTn	
	GPIO/EXHAT_PLL1_INp	27	28	GPIO/EXHAT_PLL1_OUTp	
	GND	29	30	GND	
SD	SDCARD_CD_N	31	32	SDCARD_CLK	SD CARD
	SDCARD_LVL_WP	33	34	GND	
	GND	35	36	SDCARD_D0	
SPI	SIO_SPI_1_TXD	37	38	SDCARD_D1	
	SIO_SPI_1_RXD	39	40	SDCARD_D2	
	SIO_SPI_1_FS0	41	42	SDCARD_D3	
	SIO_SPI_1_FS1	43	44	GND	
	SIO_SPI_1_CLK	45	46	SDCARD_CMD	
	GND	47	48	GND	
I2C	I2C_SCL3	49	50	AVS_DMIC_CLK_A1	DMIC
	I2C_SDA3	51	52	AVS_DMIC_CLK_B1	
	GND	53	54	AVS_DMIC_CLK_AB2	
	I2C_SCL2	55	56	GND	
	I2C_SDA2	57	58	AVS_DMIC_DATA_1	
	GND	59	60	AVS_DMIC_DATA_2	
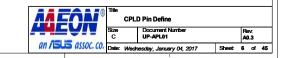
HAT40
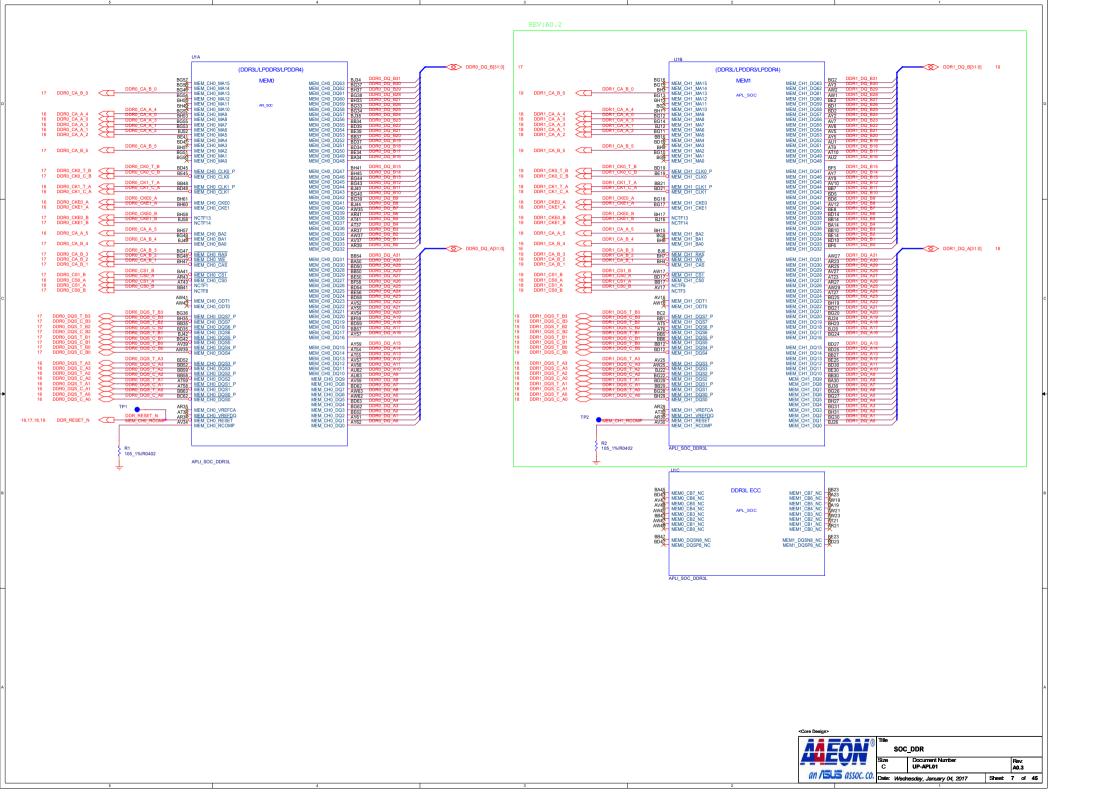
UP2 board (signal names from schema)	UP-board			UP-board	UP2 board (signal names from schema)
3V3	3V3	1	2	5V	5V
HAT_I2C1_SDA	GPIO1/I2C1_SDA	3	4	5V	5V
HAT_I2C1_SCL	GPIO2/I2C1_SCL	5	6	Ground	Ground
HAT_ANALOG_IN1-HAT_R_GPIO1	GPIO3	7	8	GPIO16/UART_TX	HAT_UART1_TXD
Ground	Ground	9	10	GPIO17/UART_RX	HAT_UART1_RXD
HAT_ANALOG_IN2-HAT_UART1_R_R	GPIO4	11	12	GPIO18/I2S_CLK	HAT_I2S6_BCLK
HAT_ANALOG_IN3-HAT_R_GPIO2	GPIO5	13	14	Ground	Ground
HAT_ANALOG_IN4-HAT_R_GPIO3	GPIO6	15	16	GPIO19	HAT_SPI_1_FS1
3V3	3V3	17	18	GPIO20	HAT_SPI_1_RXD
HAT_SPI_0_TXD	GPIO7/SPI_MOSI	19	20	Ground	Ground
HAT_SPI_0_RXD	GPIO8/SPI_MISO	21	22	GPIO21	HAT_SPI_1_TXD
HAT_SPI_0_CLK	GPIO9/SPI_CLK	23	24	GPIO22/SPI_CS0N	HAT_SPI_0_FS0
Ground	Ground	25	26	GPIO23/SPI_CS1N	HAT_SPI_0_FS1
HAT_I2C0_SDA	GPIO10/I2C0_SDA	27	28	GPIO24/I2C0_SCL	HAT_I2C0_SCL
HAT_GPIO4	GPIO11	29	30	Ground	Ground
HAT_SPI_1_CLK	GPIO12	31	32	GPIO25/PWM0	HAT_PWM0
HAT_PWM1	GPIO13/PWM1	33	34	Ground	Ground
HAT_I2S6_WS_SYNC	GPIO14/I2S_FRM	35	36	GPIO26	HAT_UART1_CTS
HAT_SPI_1_FS0	GPIO15	37	38	GPIO27/I2S_DATAIN	HAT_I2S6_SDI
Ground	Ground	39	40	GPIO28/I2S_DATAOUT	HAT_I2S6_SDO
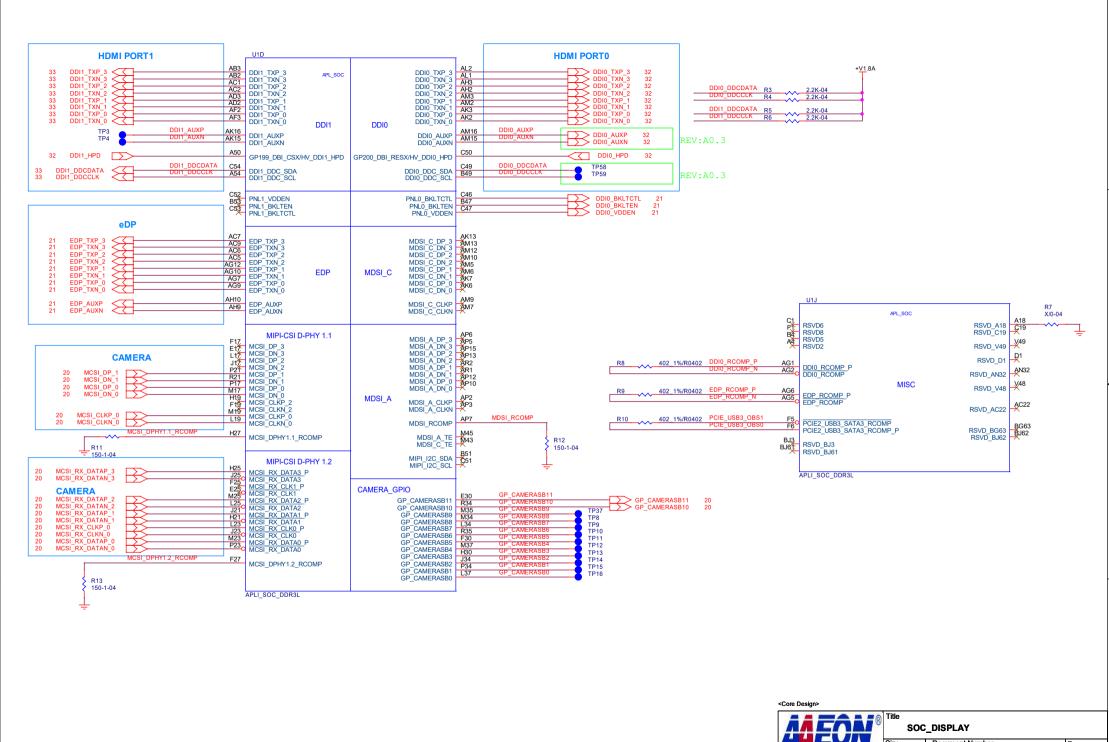
name on schematic	Location	I/O Bank	I/O Standard - VCCIO	VREF Group
AVS_I2S2_MCLK	PIN_F4	1B	1.8 V	B1_N0
BT_HOST_WAKE	PIN_E8	8	1.8 V	B8_N0
nSTATUS	PIN_C4	8	1.8 V	B8_N0
CONF_DONE	PIN_C5	8	1.8 V	B8_N0
CONFIG_SEL	PIN_D7	8	1.8 V	B8_N0
CPU_prog_JTAG_TCK	PIN_G2	1B	1.8 V	B1_N0
CPU_prog_JTAG_TDI	PIN_F5	1B	1.8 V	B1_N0
CPU_prog_JTAG_TDO	PIN_F6	1B	1.8 V	B1_N0
CPU_prog_JTAG_TMS	PIN_G1	1B	1.8 V	B1_N0
enableJTAG	PIN_E5	1B	1.8 V	B1_N0
FPGA_fw_reload	PIN_E7	8	1.8 V	B8_N0
FPGA_OE	PIN_D8	8	1.8 V	B8_N0
FPGA_RST	PIN_B9	8	1.8 V	B8_N0
I2C_SCL0	PIN_A7	8	1.8 V	B8_N0
I2C_SCL1	PIN_A9	8	1.8 V	B8_N0
I2C_SCL5	PIN_B10	8	1.8 V	B8_N0
I2C_SCL6	PIN_C10	8	1.8 V	B8_N0
I2C_SDA0	PIN_A8	8	1.8 V	B8_N0
I2C_SDA1	PIN_A10	8	1.8 V	B8_N0
I2C_SDA5	PIN_A11	8	1.8 V	B8_N0
I2C_SDA6	PIN_C9	8	1.8 V	B8_N0
ISH_GPIO_0	PIN_D1	1A	1.8 V	B1_N0
ISH_GPIO_1	PIN_C2	1A	1.8 V	B1_N0
ISH_GPIO_2	PIN_C1	1A	1.8 V	B1_N0
ISH_GPIO_3	PIN_B1	1A	1.8 V	B1_N0
ISH_GPIO_4	PIN_E1	1A	1.8 V	B1_N0
ISH_GPIO_5	PIN_E3	1A	1.8 V	B1_N0
ISH_GPIO_6	PIN_E4	1A	1.8 V	B1_N0
ISH_GPIO_7	PIN_F1	1A	1.8 V	B1_N0
ISH_GPIO_8	PIN_G4	1B	1.8 V	B1_N0
ISH_GPIO_9	PIN_H2	1B	1.8 V	B1_N0
ISH_GPIO_10	PIN_H3	1B	1.8 V	B1_N0
ISH_GPIO_11	PIN_H1	1B	1.8 V	B1_N0
ISH_GPIO_12	PIN_B7	8	1.8 V	B8_N0
ISH_GPIO_13	PIN_G10	6	1.8 V	B6_N0
ISH_GPIO_14	PIN_G9	6	1.8 V	B6_N0
ISH_GPIO_15	PIN_A5	8	1.8 V	B8_N0
LPSS_UART1_CTS	PIN_A6	8	1.8 V	B8_N0
LPSS_UART1_RTS	PIN_A4	8	1.8 V	B8_N0
LPSS_UART1_RXD	PIN_A3	8	1.8 V	B8_N0
LPSS_UART1_TXD	PIN_A2	8	1.8 V	B8_N0
OSC_CLK_OUT_0	PIN_E13	6	1.8 V	B6_N0
OSC_CLK_OUT_1	PIN_F13	6	1.8 V	B6_N0
PWM0	PIN_E9	6	1.8 V	B6_N0
PWM1	PIN_D9	6	1.8 V	B6_N0
SDIO_CLK	PIN_B2	8	1.8 V	B8_N0
SDIO_CMD	PIN_D6	8	1.8 V	B8_N0
SDIO_D0	PIN_B3	8	1.8 V	B8_N0
SDIO_D1	PIN_B4	8	1.8 V	B8_N0
SDIO_D2	PIN_B5	8	1.8 V	B8_N0
SDIO_D3	PIN_B6	8	1.8 V	B8_N0
SDIO_PWR#	PIN_E6	8	1.8 V	B8_N0
SIO_SPI_0_CLK	PIN_C12	6	1.8 V	B6_N0
SIO_SPI_0_FS0	PIN_D11	6	1.8 V	B6_N0
SIO_SPI_0_FS1	PIN_D13	6	1.8 V	B6_N0
SIO_SPI_0_RXD	PIN_B12	6	1.8 V	B6_N0
SIO_SPI_0_TXD	PIN_B13	6	1.8 V	B6_N0
AVS_I2S2_SDI	PIN_C11	6	1.8 V	B6_N0
AVS_I2S2_WS_SYNC	PIN_C13	6	1.8 V	B6_N0
PWM3	PIN_D12	6	1.8 V	B6_N0
AVS_I2S2_SDO	PIN_B11	6	1.8 V	B6_N0
AVS_I2S2_BCLK	PIN_A12	6	1.8 V	B6_N0
SIO_SPI_2_CLK	PIN_F12	6	1.8 V	B6_N0
SIO_SPI_2_FS0	PIN_F10	6	1.8 V	B6_N0
SIO_SPI_2_FS1	PIN_F9	6	1.8 V	B6_N0
SIO_SPI_2_FS2	PIN_F8	6	1.8 V	B6_N0
SIO_SPI_2_RXD	PIN_E12	6	1.8 V	B6_N0
SIO_SPI_2_TXD	PIN_E10	6	1.8 V	B6_N0
GPIO/EXHAT_LVDS0n	PIN_K5	3	3.3V	B3_N0
GPIO/EXHAT_LVDS0p	PIN_J5	3	3.3V	B3_N0
GPIO/EXHAT_LVDS1n	PIN_J6	3	3.3V	B3_N0
GPIO/EXHAT_LVDS1p	PIN_K6	3	3.3V	B3_N0
GPIO/EXHAT_LVDS2n	PIN_J7	3	3.3V	B3_N0
GPIO/EXHAT_LVDS2p	PIN_K7	3	3.3V	B3_N0
GPIO/EXHAT_LVDS3n	PIN_J8	3	3.3V	B3_N0
GPIO/EXHAT_LVDS3p	PIN_K8	3	3.3V	B3_N0
GPIO/EXHAT_LVDS4n	PIN_L5	3	3.3V	B3_N0
GPIO/EXHAT_LVDS4p	PIN_L4	3	3.3V	B3_N0
GPIO/EXHAT_LVDS5n	PIN_M4	3	3.3V	B3_N0
GPIO/EXHAT_LVDS5p	PIN_M5	3	3.3V	B3_N0
GPIO/EXHAT_LVDS6n	PIN_N4	3	3.3V	B3_N0
GPIO/EXHAT_LVDS6p	PIN_N5	3	3.3V	B3_N0
GPIO/EXHAT_LVDS7n	PIN_N6	3	3.3V	B3_N0
GPIO/EXHAT_LVDS7p	PIN_M7	3	3.3V	B3_N0
I2C_VLS_OE0	PIN_N7	3	3.3V	B3_N0
I2C_VLS_OE1	PIN_N8	3	3.3V	B3_N0
GPIO/EXHAT_PLL1_INn	PIN_G5	2	3.3V	B2_N0
GPIO/EXHAT_PLL1_INp	PIN_H6	2	3.3V	B2_N0
GPIO/EXHAT_PLL1_OUTn	PIN_M3	2	3.3V	B2_N0
GPIO/EXHAT_PLL1_OUTp	PIN_L3	2	3.3V	B2_N0
HAT_GPIO4	PIN_N11	3	3.3V	B3_N0
HAT_I2C0_SCL	PIN_J1	2	3.3V	B2_N0
HAT_I2C0_SDA	PIN_J2	2	3.3V	B2_N0
HAT_I2C1_SCL	PIN_J9	5	3.3V	B5_N0
HAT_I2C1_SDA	PIN_J10	5	3.3V	B5_N0
HAT_I2S6_BCLK	PIN_K10	5	3.3V	B5_N0
HAT_I2S6_SDI	PIN_K12	5	3.3V	B5_N0
HAT_I2S6_SDO	PIN_J12	5	3.3V	B5_N0
HAT_I2S6_WS_SYNC	PIN_K11	5	3.3V	B5_N0
HAT_PWM0	PIN_M2	2	3.3V	B2_N0
HAT_PWM1	PIN_L12	5	3.3V	B5_N0
HAT_R_GPIO1	PIN_M13	3	3.3V	B3_N0
HAT_R_GPIO2	PIN_M12	3	3.3V	B3_N0
HAT_R_GPIO3	PIN_N12	3	3.3V	B3_N0
HAT_SPI_0_CLK	PIN_H10	5	3.3V	B5_N0
HAT_SPI_0_FS0	PIN_H8	5	3.3V	B5_N0
HAT_SPI_0_FS1	PIN_H9	5	3.3V	B5_N0
HAT_SPI_0_RXD	PIN_G13	5	3.3V	B5_N0
HAT_SPI_0_TXD	PIN_G12	5	3.3V	B5_N0
HAT_SPI_1_CLK	PIN_M1	2	3.3V	B2_N0
HAT_SPI_1_FS0	PIN_N2	2	3.3V	B2_N0
HAT_SPI_1_FS1	PIN_N3	2	3.3V	B2_N0
HAT_SPI_1_RXD	PIN_K1	2	3.3V	B2_N0
HAT_SPI_1_TXD	PIN_K2	2	3.3V	B2_N0
HAT_UART1_CTS	PIN_L13	5	3.3V	B5_N0
HAT_UART1_R_RTS	PIN_K13	5	3.3V	B5_N0
HAT_UART1_RXD	PIN_J13	5	3.3V	B5_N0
HAT_UART1_TXD	PIN_H13	5	3.3V	B5_N0
LED0_3V3	PIN_H5	2	3.3V	B2_N0
LED1_3V3	PIN_H4	2	3.3V	B2_N0
LED2_3V3	PIN_L1	2	3.3V	B2_N0
LED3_3V3	PIN_L2	2	3.3V	B2_N0
LPC_CLKRU_N	PIN_L11	3	3.3V	B3_N0
LPC_FRAME_R	PIN_L10	3	3.3V	B3_N0
LPC_R_AD0	PIN_M11	3	3.3V	B3_N0
LPC_R_AD1	PIN_M10	3	3.3V	B3_N0
LPC_R_AD2	PIN_M9	3	3.3V	B3_N0
LPC_R_AD3	PIN_M8	3	3.3V	B3_N0
LPC_R_CLKOUT0	PIN_N9	3	3.3V	B3_N0
INT_SERIRQ_R	PIN_N10	3	3.3V	B3_N0

REV:A0.2

U1A (DDR3L/LPDDR3/LPDDR4) MEM0 — APL_SOC — APLI_SOC_DDR3L

U1B (DDR3L/LPDDR3/LPDDR4) MEM1 — APL_SOC — APLI_SOC_DDR3L

U1C DDR3L ECC — APL_SOC — APLI_SOC_DDR3L

DDR0_DQ_B[31:0]   17
DDR0_DQ_A[31:0]
DDR1_DQ_B[31:0]   19
DDR1_DQ_A[31:0]   18

TP1   R1   105_1%/R0402
TP2   R2   105_1%/R0402

16,17,18,19   DDR_RESET_N

HDMI PORT1

33	DDI1_TXP_3	
33	DDI1_TXN_3	
33	DDI1_TXP_2	
33	DDI1_TXN_2	
33	DDI1_TXP_1	
33	DDI1_TXN_1	
33	DDI1_TXP_0	
33	DDI1_TXN_0	

TP3 TP4 — DDI1_AUXP / DDI1_AUXN

32 DDI1_HPD

33 DDI1_DDCDATA — DDI1_DDCDATA
33 DDI1_DDCCLK — DDI1_DDCCLK

U1D — APL_SOC

DDI1
- AB3 DDI1_TXP_3
- AB2 DDI1_TXN_3
- AC1 DDI1_TXP_2
- AC2 DDI1_TXN_2
- AD3 DDI1_TXP_1
- AD2 DDI1_TXN_1
- AF2 DDI1_TXP_0
- AF3 DDI1_TXN_0
- AK16 DDI1_AUXP
- AK15 DDI1_AUXN
- A50 GP199_DBI_CSX/HV_DDI1_HPD
- C54 DDI1_DDC_SDA
- A54 DDI1_DDC_SCL
- C52 PNL1_VDDEN
- B53 PNL1_BKLTEN
- C53 PNL1_BKLTCTL

DDI0
- AL2 DDI0_TXP_3
- AL1 DDI0_TXN_3
- AH3 DDI0_TXP_2
- AH2 DDI0_TXN_2
- AM3 DDI0_TXP_1
- AM2 DDI0_TXN_1
- AK3 DDI0_TXP_0
- AK2 DDI0_TXN_0
- AM16 DDI0_AUXP
- AM15 DDI0_AUXN
- C50 GP200_DBI_RESX/HV_DDI0_HPD
- C49 DDI0_DDC_SDA
- B49 DDI0_DDC_SCL
- C46 PNL0_BKLTCTL
- B47 PNL0_BKLTEN
- C47 PNL0_VDDEN

HDMI PORT0

DDI0_TXP_3	32	
DDI0_TXN_3	32	
DDI0_TXP_2	32	
DDI0_TXN_2	32	
DDI0_TXP_1	32	
DDI0_TXN_1	32	
DDI0_TXP_0	32	
DDI0_TXN_0	32	

DDI0_AUXP / DDI0_AUXN — DDI0_AUXP 32 / DDI0_AUXN 32 **REV:A0.3**

DDI0_HPD 32

DDI0_DDCDATA / DDI0_DDCCLK — TP58 TP59 **REV:A0.3**

DDI0_BKLTCTL 21
DDI0_BKLTEN 21
DDI0_VDDEN 21

+V1.8A
DDI0_DDCDATA R3 2.2K-04
DDI0_DDCCLK R4 2.2K-04
DDI1_DDCDATA R5 2.2K-04
DDI1_DDCCLK R6 2.2K-04

eDP

21	EDP_TXP_3
21	EDP_TXN_3
21	EDP_TXP_2
21	EDP_TXN_2
21	EDP_TXP_1
21	EDP_TXN_1
21	EDP_TXP_0
21	EDP_TXN_0
21	EDP_AUXP
21	EDP_AUXN

EDP
- AC7 EDP_TXP_3
- AC9 EDP_TXN_3
- AC6 EDP_TXP_2
- AC5 EDP_TXN_2
- AG12 EDP_TXP_1
- AG10 EDP_TXN_1
- AG7 EDP_TXP_0
- AG9 EDP_TXN_0
- AH10 EDP_AUXP
- AH9 EDP_AUXN

MDSI_C
- AK13 MDSI_C_DP_3
- AM13 MDSI_C_DN_3
- AM12 MDSI_C_DP_2
- AM10 MDSI_C_DN_2
- AM5 MDSI_C_DP_1
- AM6 MDSI_C_DN_1
- AK7 MDSI_C_DP_0
- AK6 MDSI_C_DN_0
- AM9 MDSI_C_CLKP
- AM7 MDSI_C_CLKN

CAMERA

20	MCSI_DP_1
20	MCSI_DN_1
20	MCSI_DP_0
20	MCSI_DN_0
20	MCSI_CLKP_0
20	MCSI_CLKN_0

MIPI-CSI D-PHY 1.1
- F17 MCSI_DP_3
- E17 MCSI_DN_3
- L17 MCSI_DP_2
- J17 MCSI_DN_2
- P21 MCSI_DP_1
- R21 MCSI_DN_1
- P17 MCSI_DP_0
- M17 MCSI_DN_0
- H19 MCSI_CLKP_2
- F19 MCSI_CLKN_2
- M19 MCSI_CLKP_0
- L19 MCSI_CLKN_0
- H27 MCSI_DPHY1.1_RCOMP

MCSI_DPHY1.1_RCOMP
R11 150-1-04

MDSI_A
- AP6 MDSI_A_DP_3
- AP5 MDSI_A_DN_3
- AP15 MDSI_A_DP_2
- AP13 MDSI_A_DN_2
- AR2 MDSI_A_DP_1
- AR1 MDSI_A_DN_1
- AP12 MDSI_A_DP_0
- AP10 MDSI_A_DN_0
- AP2 MDSI_A_CLKP
- AP3 MDSI_A_CLKN
- AP7 MDSI_RCOMP
- M45 MDSI_A_TE
- M43 MDSI_C_TE
- B51 MIPI_I2C_SDA
- C51 MIPI_I2C_SCL

MDSI_RCOMP
R12 150-1-04

CAMERA

20	MCSI_RX_DATAP_3
20	MCSI_RX_DATAN_3
20	MCSI_RX_DATAP_2
20	MCSI_RX_DATAN_2
20	MCSI_RX_DATAP_1
20	MCSI_RX_DATAN_1
20	MCSI_RX_CLKP_0
20	MCSI_RX_CLKN_0
20	MCSI_RX_DATAP_0
20	MCSI_RX_DATAN_0

MIPI-CSI D-PHY 1.2
- H25 MCSI_RX_DATA3_P
- F25 MCSI_RX_DATA3
- E25 MCSI_RX_CLK1_P
- M25 MCSI_RX_CLK1
- L25 MCSI_RX_DATA2_P
- J21 MCSI_RX_DATA2
- H21 MCSI_RX_DATA1_P
- L23 MCSI_RX_DATA1
- J23 MCSI_RX_CLK0_P
- M23 MCSI_RX_CLK0
- P23 MCSI_RX_DATA0_P
- H30 MCSI_RX_DATA0
- F27 MCSI_DPHY1.2_RCOMP

MCSI_DPHY1.2_RCOMP
R13 150-1-04

CAMERA_GPIO
- E30 GP_CAMERASB11
- R34 GP_CAMERASB10
- M35 GP_CAMERASB9
- M34 GP_CAMERASB8
- L34 GP_CAMERASB7
- R35 GP_CAMERASB6
- F30 GP_CAMERASB5
- M37 GP_CAMERASB4
- H30 GP_CAMERASB3
- J34 GP_CAMERASB2
- P34 GP_CAMERASB1
- L37 GP_CAMERASB0

GP_CAMERASB11 — GP_CAMERASB11 20
GP_CAMERASB10 — GP_CAMERASB10 20

TP37 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16

APLI_SOC_DDR3L

U1J — APL_SOC

MISC
- C1 RSVD6
- F1 RSVD8
- B4 RSVD5
- A4 RSVD2
- A18 RSVD_A18
- C19 RSVD_C19
- V49 RSVD_V49
- D1 RSVD_D1
- AN32 RSVD_AN32
- V48 RSVD_V48
- AC22 RSVD_AC22
- BG63 RSVD_BG63
- BJ62 RSVD_BJ61
- BJ3 RSVD_BJ3
- BJ61 RSVD_BJ61

R8 402 1%/R0402 DDI0_RCOMP_P — AG1 DDI0_RCOMP_P
DDI0_RCOMP_N — AG2 DDI0_RCOMP

R9 402 1%/R0402 EDP_RCOMP_P — AG6 EDP_RCOMP_P
EDP_RCOMP_N — AG5 EDP_RCOMP

R10 402 1%/R0402 PCIE_USB3_OBS1 — F5 PCIE2_USB3_SATA3_RCOMP
PCIE_USB3_OBS0 — F6 PCIE2_USB3_SATA3_RCOMP_P

R7 X/0-04
C19

APLI_SOC_DDR3L

U1E — APL_SOC / APLI_SOC_DDR3L

PCIE

Pin	Signal		Net
31	PCIE_TXP2	T2	PCIE_P2_TXP
31	PCIE_TXN2	T3	PCIE_P2_TXN
31	PCIE_RXP2	M5	PCIE_P2_RXP
31	PCIE_RXN2	M6	PCIE_P2_RXN
30	PCIE_TXP1	R1	PCIE_P1_TXP
30	PCIE_TXN1	R2	PCIE_P1_TXN
30	PCIE_RXP1	T10	PCIE_P1_RXP
30	PCIE_RXN1	T12	PCIE_P1_RXN
23	PCIE_TXP0	V3	PCIE_P0_TXP
23	PCIE_TXN0	V2	PCIE_P0_TXN
23	PCIE_RXP0	P7	PCIE_P0_RXP
23	PCIE_RXN0	P6	PCIE_P0_RXN

LAN2, LAN1, mini PCIE

USB3.0

Pin	Signal		Net
26	USB3_TXP_P1	K3	USB3_P1_TXP
26	USB3_TXN_P1	K2	USB3_P1_TXN
26	USB3_RXP_P1	F2	USB3_P1_RXP
26	USB3_RXN_P1	G2	USB3_P1_RXN
25	USB3_TXP_P0	J1	USB3_P0_TXP
25	USB3_TXN_P0	J2	USB3_P0_TXN
25	USB3_RXP_P0	K9	USB3_P0_RXP
25	USB3_RXN_P0	K10	USB3_P0_RXN

USB3 TYPE A, USB3 TYPE OTG

SATA

Pin	Signal		Net
24	SATA_TXP0	Y3	SATA_P0_TXP
24	SATA_TXN0	Y2	SATA_P0_TXN
24	SATA_RXP0	T9	SATA_P0_RXP
24	SATA_RXN0	T7	SATA_P0_RXN

PCIE/USB3.0/SATA

Pin	Signal		Net
26	USB3_TXP_P2	L2	PCIE_P5_USB3_P2_TXP
26	USB3_TXN_P2	L1	PCIE_P5_USB3_P2_TXN
26	USB3_RXP_P2	K7	PCIE_P5_USB3_P2_RXP
26	USB3_RXN_P2	M7	PCIE_P5_USB3_P2_RXN
27	USB3_TXP_P3	N2	PCIE_P4_USB3_P3_TXP
27	USB3_TXN_P3	M2	PCIE_P4_USB3_P3_TXN
27	USB3_RXP_P3	H5	PCIE_P4_USB3_P3_RXP
27	USB3_RXN_P3	H6	PCIE_P4_USB3_P3_RXN
22	PCIE_TXP3	P3	PCIE_P3_USB3_P4_TXP
22	PCIE_TXN3	P2	PCIE_P3_USB3_P4_TXN
22	PCIE_RXP3	P12	PCIE_P3_USB3_P4_RXP
22	PCIE_RXN3	P10	PCIE_P3_USB3_P4_RXN
23	SATA_TXP1	W1	SATA_P1_USB3_P5_TXP
23	SATA_TXN1	W2	SATA_P1_USB3_P5_TXN
23	SATA_RXP1	T5	SATA_P1_USB3_P5_RXP
23	SATA_RXN1	T6	SATA_P1_USB3_P5_RXN

USB3 TYPE A, USB3 TYPE A, M.2, EXHAT

PCIE CLKREQ / WAKE

Pin	Signal
AJ62	PCIE_CLKREQ3 / PCIE_CLKREQ3#
AH61	PCIE_CLKREQ2 / PCIE_CLKREQ2#
AH62	PCIE_CLKREQ1 / PCIE_CLKREQ1#
AK62	PCIE_CLKREQ0 / PCIE_CLKREQ0#
N62	PCIE_WAKE3 / PCIE_WAKE3_N
P61	PCIE_WAKE2 / PCIE_WAKE2_N
P62	PCIE_WAKE1 / PCIE_WAKE1_N
R62	PCIE_WAKE0 / PCIE_WAKE0_N

R37 10K-04 PCIE_CLKREQ0#
R39 10K-04 PCIE_CLKREQ1#
R41 10K-04 PCIE_CLKREQ2#
R42 10K-04 PCIE_CLKREQ3#

PCIE CLKOUT

Pin	Signal		Net	
B7	PCIE_CLKOUT3P		CLK_PCIE_M2_P	22
B5	PCIE_CLKOUT3N		CLK_PCIE_M2_N	22
A7	PCIE_CLKOUT2P		CLK_PCIE_LAN2_P	31
B8	PCIE_CLKOUT2N		CLK_PCIE_LAN2_N	31
C10	PCIE_CLKOUT1P		CLK_PCIE_LAN1_P	30
A10	PCIE_CLKOUT1N		CLK_PCIE_LAN1_N	30
C11	PCIE_CLKOUT0P		CLK_PCIE_MINI_P	23
B11	PCIE_CLKOUT0N		CLK_PCIE_MINI_N	23
E21	PCIE_REF_CLK_RCOMP		PCIE_CLK_RCOMP R22 60.4_1%/R0402	

REV:A0.2   +V1.8A
R35 4.7K-04 PCIE_WAKE0_N
R36 4.7K-04 PCIE_WAKE1_N
R38 4.7K-04 PCIE_WAKE2_N
R40 4.7K-04 PCIE_WAKE3_N

USB_SSIC

Pin	Signal		Net	TP
AH13	USB_SSIC_0_TX_P		USB_SSIC_TXP	TP42
AH12	USB_SSIC_0_TX		USB_SSIC_TXN	TP43
AG16	USB_SSIC_0_RX_P		USB_SSIC_RXP	TP44
AG15	USB_SSIC_0_RX		USB_SSIC_RXN	TP45
AB15	USB_SSIC_RCOMP		USB_SSIC_RCOMP R23 X/137_1%/R0402	

USB2.0

Pin	Signal		Net		Header
V5	USB2_DP7		USB2_DP7	28	PIN HEADER
V6	USB2_DN7		USB2_DN7	28	
AC12	USB2_DP6		USB2_DP6	28	
AC10	USB2_DN6		USB2_DN6	28	
AB6	USB2_DP5		USB2_DP5	23	mini PCIE
AB7	USB2_DN5		USB2_DN5	23	
Y9	USB2_DP4		USB2_DP4	22	M.2
Y10	USB2_DN4		USB2_DN4	22	
V9	USB2_DP3		USB2_DP3	27	USB3 TYPE A
V7	USB2_DN3		USB2_DN3	27	
Y13	USB2_DP2		USB2_DP2	26	
V13	USB2_DN2		USB2_DN2	26	
V16	USB2_DP1		USB2_DP1	26	
V15	USB2_DN1		USB2_DN1	26	
V12	USB2_DP0		USB2_DP0	25	USB3 OTG
V10	USB2_DN0		USB2_DN0	25	
AC15	USB2_OTG_ID	R26 0-04			
AC16	USB2_VBUS_SNS	USB2_VBUS_SNS R24 10K-04 +V1.8A	USB_OTG_R_ID	25	
C55	USB2_OC1	USB2_OC#_1 R755 10K-04 +V1.8A			
B55	USB2_OC0	USB2_OC#_0 R756 10K-04 +V1.8A			
Y15	USB2_RCOMP	USB2_RCOMP R25 113_1%/R0402			

U3 — NTS0104GU12

+V1.8A C2 0.1uF/16VX/04
+V1.8A
+V3.3A C3 0.1uF/16VX/04

Pin		Pin	Signal	
2	A1	10	WAKE_MINI_N_3V3	PCIE_WAKE0_N
3	A2	9	WAKE_LAN1_N_3V3	PCIE_WAKE1_N
4	A3	8	WAKE_LAN2_N_3V3	PCIE_WAKE2_N
5	A4	7	WAKE_M2_N_3V3	PCIE_WAKE3_N

VCCA(1) OE(12) VCCB(11) GND(6)
B1 B2 B3 B4

WAKE_MINI_N_3V3 23
WAKE_LAN1_N_3V3 30
WAKE_LAN2_N_3V3 31
WAKE_M2_N_3V3 22

U1M — APL_SOC — APLI_SOC_DDR3L — **VSS 1**

U1N — APL_SOC — APLI_SOC_DDR3L — **VSS 2**

U1O — APL_SOC — APLI_SOC_DDR3L — **VSS 3**

U1I — APL_SOC — **NCTF/MCIVR** — APLI_SOC_DDR3L

U1P — APL_SOC — **NC** — APLI_SOC_DDR3L

<Core Design>

Title	**SOC_GND**
Size: Custom	Document Number: UP-APL01	Rev: A0.3
Date: *Wednesday, January 04, 2017*	Sheet: 10 of 45

REV:A0.3

LPSS_UART2_TXD H41
LPSS_UART2_RTS J41
L41
M41

U1F
APL_SOC

LPSS_UART2_TXD
LPSS_UART2_RXD
LPSS_UART2_RTS
LPSS_UART2_CTS

UART

EMMC

EMMC_CLK   Y58   EMMC_CLK   34
EMMC_RCLK   V54   EMMC_RCLK   34
EMMC_CMD   Y51   EMMC_CMD   34

CPLD

38 LPSS_UART1_TXD   LPSS_UART1_TXD B43
38 LPSS_UART1_RXD   LPSS_UART1_RXD C43
38 LPSS_UART1_RTS   LPSS_UART1_RTS A42
38 LPSS_UART1_CTS   LPSS_UART1_CTS C42

LPSS_UART1_TXD
LPSS_UART1_RXD
LPSS_UART1_RTS
LPSS_UART1_CTS

EMMC_D7   Y57   EMMC_D7   34
EMMC_D6   V55   EMMC_D6   34
EMMC_D5   Y49   EMMC_D5   34
EMMC_D4   V52   EMMC_D4   34
EMMC_D3   V51   EMMC_D3   34
EMMC_D2   T59   EMMC_D2   34
EMMC_D1   T58   EMMC_D1   34
EMMC_D0   V58   EMMC_D0   34

M.2 USB PANEL

22 LPSS_UART0_TXD   LPSS_UART0_TXD B45
22 LPSS_UART0_RXD   LPSS_UART0_RXD C45
22 LPSS_UART0_RTS   LPSS_UART0_RTS A46
22 LPSS_UART0_CTS   LPSS_UART0_CTS C44

LPSS_UART0_TXD
LPSS_UART0_RXD
LPSS_UART0_RTS
LPSS_UART0_CTS

EMMC_RCOMP   V59   EMMC_RCOMP   R48   200-1-04

UART0 Voltage level

CPLD

38 SIO_SPI_2_TXD   SIO_SPI_2_TXD E62
38 SIO_SPI_2_RXD   SIO_SPI_2_RXD C62
38 SIO_SPI_2_FS2   SIO_SPI_2_FS2 D59
38 SIO_SPI_2_FS1   SIO_SPI_2_FS1 E56
38 SIO_SPI_2_FS0   SIO_SPI_2_FS0 D61
38 SIO_SPI_2_CLK   SIO_SPI_2_CLK F62

SIO_SPI_2_TXD
SIO_SPI_2_RXD
SIO_SPI_2_FS2
SIO_SPI_2_FS1
SIO_SPI_2_FS0
SIO_SPI_2_CLK

SPI

SDIO

SDIO_CLK   P58   SDIO_CLK   38
SDIO_CMD   T57   SDIO_CMD   38
SDIO_D3   T55   SDIO_D3   38
SDIO_D2   T54   SDIO_D2   38
SDIO_D1   P57   SDIO_D1   38
SDIO_D0   T52   SDIO_D0   38
SDIO_PWR_DWN P51 SDIO_PWR# 38

36,37 SIO_SPI_1_TXD   SIO_SPI_1_TXD H58
36,37 SIO_SPI_1_RXD   SIO_SPI_1_RXD H57
36,37 SIO_SPI_1_FS1   SIO_SPI_1_FS1 F61
36,37 SIO_SPI_1_FS0   SIO_SPI_1_FS0 K55
37   SIO_SPI_1_FS1   SIO_SPI_1_FS1 F58
36,37 SIO_SPI_1_CLK   SIO_SPI_1_CLK

SIO_SPI_1_TXD
SIO_SPI_1_RXD
SIO_SPI_1_FS1
SIO_SPI_1_FS0
SIO_SPI_1_CLK

SDCARD

SDCARD_CLK   AB58 SDCARD_CLK   37
SDCARD_CMD   AC52 SDCARD_CMD   37
SDCARD_CD   AB54 SDCARD_CD_N   37
SDCARD_LVL_WP AB55 SDCARD_LVL_WP 37

ADC CPLD

38 SIO_SPI_0_TXD   SIO_SPI_0_TXD J52
38 SIO_SPI_0_RXD   SIO_SPI_0_RXD H54
38 SIO_SPI_0_FS1   SIO_SPI_0_FS1 H52
38 SIO_SPI_0_FS0   SIO_SPI_0_FS0 F52
38 SIO_SPI_0_CLK   SIO_SPI_0_CLK F54

SIO_SPI_0_TXD
SIO_SPI_0_RXD
SIO_SPI_0_FS1
SIO_SPI_0_FS0
SIO_SPI_0_CLK

SDCARD_D3   AB51 SDCARD_D3   37
SDCARD_D2   AC51 SDCARD_D2   37
SDCARD_D1   AC48 SDCARD_D1   37
SDCARD_D0   AC49 SDCARD_D0   37

SPI Voltage level

35,38 SPI_CLK   C56   FST_SPI_CLK
35,38 SPI_CS0#   C57   FST_SPI_CS1
                  B57   FST_SPI_CS0

SPI NOR

LPC

LPC_CLKOUT1 AA62 LPC_CLKOUT1 R55 20-04 LPC_R_CLKOUT1 23
LPC_CLKOUT0 AB61 LPC_CLKOUT0 R56 20-04 LPC_R_CLKOUT0 38

                  B61   FST_SPI_IO3
                  B60   FST_SPI_IO2
35,38 SPI_MOSI   A58   FST_SPI_MOSI_IO0
35,38 SPI_MISO   B58   FST_SPI_MISO_IO1

LPC_FRAME   V61 LPC_FRAME_N R57 20-04 LPC_FRAME_R 23,38
LPC_AD3   W63 LPC_AD3   R59 20-04 LPC_R_AD3   23,38
LPC_AD2   W62 LPC_AD2   R60 20-04 LPC_R_AD2   23,38
LPC_AD1   Y62 LPC_AD1   R61 20-04 LPC_R_AD1   23,38
LPC_AD0   Y61 LPC_AD0   R62 20-04 LPC_R_AD0   23,38

LPC_CLKRUN V62 LPC_CLKRU_N   38 LPC_CLKRU_N   38
LPC_SERIRQ AB62 INT_SERIRQ   R63 20-04 INT_SERIRQ_R 23,38

APLI_SOC_DDR3L

Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.

REV:A0.3   +V1.8A

LPSS_UART1_TXD   R46   X/10K-04
SIO_SPI_2_TXD   R66   10K-04
SIO_SPI_0_FS1   R77   10K-04

Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

LPSS_UART2_RTS   R58   10K-04
SIO_SPI_2_FS2   R68   10K-04
SIO_SPI_1_TXD   R73   10K-04
SIO_SPI_0_CLK   R79   10K-04
SIO_SPI_1_FS0   R75   10K-04
SIO_SPI_0_FS0   R78   10K-04
SIO_SPI_1_FS1   R67   10K-04

REV:A0.2

LPSS_UART1_TXD   R799   10K-04

REV:A0.3

+V1.8A

SDCARD_CD_N   R764   100K-04

LPC_CLKRU_N   R64   0-04

Boot BIOS Strap (BBS) — SIO_SPI_1_CLK

+V1.8A
R69   X/10K-04
R71   4.7K-04   SIO_SPI_1_CLK

0	Boot from SPI
1	Do not boot from SPI (default)

Top swap override — SIO_SPI_2_FS1

+V1.8A
SIO_SPI_2_FS1   R74   X/10K-04
                R76   10K-04

0	Disable (default)
1	Override

Force DNX FW Load — LPSS_UART2_TXD

+V1.8A
LPSS_UART2_TXD   R51   X/10K-04
                 R52   10K-04

0	Do not force (default)
1	Enable

RTC Clock Timer Bypass — LPSS_UART0_RTS

+V1.8A
LPSS_UART0_RTS   R45   10K-04

0	Disable bypass (Default)
1	Enable bypass

Flash Descriptor Override — SIO_SPI_2_CLK

+V1.8A
SIO_SPI_2_CLK   R70   X/10K-04
                R72   10K-04

0	No Override (Normal Operation)
1	Override

LPC 1.8V/3.3V Mode Select — SIO_SPI_0_TXD

+V1.8A
SIO_SPI_0_TXD   R53   X/10K-04
                R54   4.7K-04

0	3.3V mode
1	1.8V mode (default)

Allow SPI as a boot source — LPSS_UART1_RTS

+V1.8A
LPSS_UART1_RTS   R49   10K-04
                 R50   X/10K-04

0	Disable
1	Enable (default)

Enable CSE ROM Bypass — LPSS_UART0_TXD

+V1.8A
LPSS_UART0_TXD   R43   X/10K-04
                 R44   10K-04

0	Disable bypass (default)
1	Enable Bypass

SOC_SMBUS_GPIO — U1G APL_SOC

Left block (I2C / interfaces)

Source	Pin	Net		SOC pin	SOC label
eDP	21	I2C_SCL7	I2C_SCL7	AP61	LPSS_I2C7_SCL
eDP	21	I2C_SDA7	I2C_SDA7	AP62	LPSS_I2C7_SDA
CPLD	38	I2C_SCL6	I2C_SCL6	AK61	LPSS_I2C6_SCL
CPLD	38	I2C_SDA6	I2C_SDA6	AL63	LPSS_I2C6_SDA
CPLD	38	I2C_SCL5	I2C_SCL5	AP51	LPSS_I2C5_SCL
CPLD	38	I2C_SDA5	I2C_SDA5	AP49	LPSS_I2C5_SDA
CAMERA	20	I2C_SCL4	I2C_SCL4	AP54	LPSS_I2C4_SCL
CAMERA	20	I2C_SDA4	I2C_SDA4	AP52	LPSS_I2C4_SDA
EXHAT	37	I2C_SCL3	I2C_SCL3	AL62	LPSS_I2C3_SCL
EXHAT	37	I2C_SDA3	I2C_SDA3	AM62	LPSS_I2C3_SDA
EXHAT	37	I2C_SCL2	I2C_SCL2	AP58	LPSS_I2C2_SCL
EXHAT	37	I2C_SDA2	I2C_SDA2	AP59	LPSS_I2C2_SDA
CPLD	38	I2C_SCL1	I2C_SCL1	AM61	LPSS_I2C1_SCL
CPLD	38	I2C_SDA1	I2C_SDA1	AN62	LPSS_I2C1_SDA
CPLD	38	I2C_SCL0	I2C_SCL0	AR63	LPSS_I2C0_SCL
CPLD	38	I2C_SDA0	I2C_SDA0	AR62	LPSS_I2C0_SDA

Block label: I2C / GPIO / APL_SOC / U1G / APLI_SOC_DDR3L

SMB
	Net	Pin	SOC
	SMB_CLK_A	T62	SMB_CLK
	SMB_DATA_A	T61	SMB_DATA
22	SMB_ALERT#	R63	SMB_ALERT

REV:A0.3

PWM
	Net	Pin	SOC
38	PWM3	E41	PWM3
29	PWM2	F41	PWM2
38	PWM1	C41	PWM1
38	PWM0	B41	PWM0

REV:A0.3

AVS DMIC
	Net	Pin	SOC
37	AVS_DMIC_DATA_2	M52	AVS_DMIC_DATA_2
37	AVS_DMIC_DATA_1	M54	AVS_DMIC_DATA_1
37	AVS_DMIC_CLK_B1	P52	AVS_DMIC_CLK_B1
37	AVS_DMIC_CLK_AB2	M55	AVS_DMIC_CLK_AB2
37	AVS_DMIC_CLK_A1	P54	AVS_DMIC_CLK_A1

REV:A0.3

I2S
	Net	Pin	SOC
	GPIO_92	M61	AVS_I2S3_WS_SYNC
		L63	AVS_I2S3_SDO
		L62	AVS_I2S3_SDI
		M62	AVS_I2S3_BCLK
38	AVS_I2S2_WS_SYNC	M57	AVS_I2S2_WS_SYNC
38	AVS_I2S2_SDO / GPIO_88	M58	AVS_I2S2_SDO
38	AVS_I2S2_SDI	K59	AVS_I2S2_SDI
38	AVS_I2S2_MCLK	K58	AVS_I2S2_MCLK/HDA_RST_N
38	AVS_I2S2_BCLK	H59	AVS_I2S2_BCLK
	GPIO_78	J62	AVS_I2S1_WS_SYNC
		K62	AVS_I2S1_SDO
		K61	AVS_I2S1_SDI
		G62	AVS_I2S1_MCLK
		H63	AVS_I2S1_BCLK

R832 0-04

Please ensure that this strap is pulled LOW when
RSM_RST_N de-asserts for normal platform operation.

Middle block (GPIO)

SOC label	Pin	Net	Resistor	Dest
GPIO_26/SATA_LED_N	C31			
GPIO_25	C27	CPU_prog_JTAG_TDO		33,38
GPIO_24	B25	CPU_prog_JTAG_TMS		33,38
GPIO_23/SATA_GP1	A26	CPU_prog_JTAG_TCK		38
GPIO_22/SATA_GP0	C26	CPU_prog_JTAG_TDI		38
GPIO_21		enableJTAG	R812 0-04	38
GPIO_20	B27	disableCEC		33

SOC label	Pin	Net	Resistor	Dest
GPIO_219	L30			
GPIO_218	M30	GPIO_218	R736 0-04	EMMC_RST_N 34
GPIO_217	M29	GPIO_217	R737 0-04	nSTATUS 38
GPIO_216	P30	GPIO_216	R738 0-04	FPGA_RST 38
				FPGA_OE 38
GPIO_27	C29	GPIO_27	R739 0-04	FPGA_fw_reload 38
GPIO_19	C33	GPIO_19	R740 0-04	CONFIG_SEL 38
GPIO_18	J39	GPIO_18	R88 X/0-04	BT_HOST_WAKE 38
GPIO_17	C35	GPIO_17	R741 0-04	CONF_DONE 38
GPIO_16	C36	GPIO_16	R86 0-04	PM_PWRBTN#_GPIO16 13

SOC label	Pin	Net
GPIO_15	F39	GPIO_PME#
GPIO_14	C30	WAKE_RI#_R
GPIO_13	E39	APL_DIO_7 TP46
GPIO_12	A30	APL_DIO_6 TP47
GPIO_11		APL_DIO_5 TP48
GPIO_10	L39	APL_DIO_4 TP50
GPIO_9	A30	APL_DIO_3 TP51
GPIO_8	B29	APL_DIO_2
GPIO_7	H39	APL_DIO_1 TP52
GPIO_6	B31	APL_DIO_0 TP53
GPIO_5	A34	APL_Panel ID_3 TP54
GPIO_4	B39	APL_Panel ID_2 TP55
GPIO_3	E39	APL_Panel ID_1 TP56
GPIO_2	C39	APL_Panel ID_0 TP57
GPIO_1	B33	BOARD_ID_BIT1
GPIO_0	A38	BOARD_ID_BIT0

APL_DIO_4 — R750 X/0-04 — BT_HOST_WAKE

SOC label	Pin	Net	Dest
GPIO_30	C37	ISH_GPIO_12	38
GPIO_29	H35	ISH_GPIO_11	38
GPIO_28	B37	ISH_GPIO_10	38
ISH_GPIO_9	AK57	ISH_GPIO_9	38
ISH_GPIO_8	AM52	ISH_GPIO_8	38
ISH_GPIO_7	AM55	ISH_GPIO_7	38
ISH_GPIO_6	AM57	ISH_GPIO_6	38
ISH_GPIO_5	AM49	ISH_GPIO_5	38
ISH_GPIO_4	AM51	ISH_GPIO_4	38
ISH_GPIO_3/HDA_SDO	AM54	ISH_GPIO_3	38
ISH_GPIO_2/HDA_SDI	AK51	HDA_SDIN0_SOC	R95 0-04 ISH_GPIO_2 38
ISH_GPIO_1/HDA_WS_SYNC	AK58	HDA_SYNC_SOC	R96 0-04 ISH_GPIO_1 38
ISH_GPIO_0/HDA_BCLK	AM48		ISH_GPIO_0 38

SOC label	Pin	Net	Dest
GPIO_33	F34	PMIC_IRQ_N	38,42
GPIO_32	F35	ISH_GPIO_14	38
GPIO_31	H34	ISH_GPIO_13	38
GPIO_RCOMP	E34	GPIO_RCOMP	R103 200-1-04

Board ID (top right) — REV:A0.3

BOARD_ID_BIT1 — R726 10K-04 / R727 X/4.7K-04 — +V1.8A
BOARD_ID_BIT0 — R728 X/10K-04 / R729 4.7K-04 — +V1.8A

BOARD ID, CHANGE BOM EVERY STAGE

I2C pull-ups (+V1.8A)

Net	R	Value
I2C_SCL0	R123	1K-04
I2C_SDA0	R124	1K-04
I2C_SCL1	R125	1K-04
I2C_SDA1	R127	1K-04
I2C_SCL2	R469	1K-04
I2C_SDA2	R470	1K-04
I2C_SCL3	R467	1K-04
I2C_SDA3	R468	1K-04
I2C_SCL4	R757	1K-04
I2C_SDA4	R758	1K-04
I2C_SCL5	R117	1K-04
I2C_SDA5	R118	1K-04
I2C_SCL6	R115	1K-04
I2C_SDA6	R116	1K-04
I2C_SCL7	R300	1K-04
I2C_SDA7	R301	1K-04

HDA_SDIN0_SOC — R126 X/249_1%/R0402 — ISH_GPIO_1
R129 X/510_1%/R0402

WAKE_RI#_R — R111 10K-04 — +V1.8A
GPIO_PME# — R112 10K-04

U6 — 24LC64-I/SN (EEPROM)

+V3.3A
R97 X/4.7K-04
R98 X/4.7K-04
R99 X/4.7K-04
R100 4.7K-04 → 1 A0
R101 4.7K-04 → 2 A1
R102 4.7K-04 → 3 A2
4 GND
5 SDA → SMB_DAT_3V3A
6 SCL → SMB_CLK_3V3A
7 WP
8 VCC → +V3.3A
R104 220-1-04
C7 0.1uF/16VX/04

SMB_ALERT# — R119 2.2K-04 — +V3.3A
SMB_CLK_A — R120 2.2K-04
SMB_DATA_A — R121 2.2K-04

SMB_CLK_A — R84 0-04 — SMB_CLK_3V3A → SMB_CLK_3V3A 22,23
SMB_DATA_A — R85 0-04 — SMB_DAT_3V3A → SMB_DAT_3V3A 22,23

Strap resistors (lower left) — REV:A0.3

PWM1 — R128 10K-04
PWM0 — R130 10K-04
AVS_DMIC_CLK_AB2 — R94 10K-04

PWM2 — R105 X/10K-04 / R108 10K-04 — +V1.8A
GPIO_92 — R113 X/10K-04 / R114 10K-04 — +V1.8A
GPIO_78 — R106 X/10K-04 / R109 1K-04 — +V1.8A
GPIO_88 — R107 X/10K-04 / R110 4.7K-04 — +V1.8A

Strap tables

VCC_1P24V_1P35V_A Volt Selection
PWM2	
0	1.24V (default)
1	1.35

SMBus No Re-Boot
GPIO_92	
0	Disable (default)
1	Enable

SMBus 1.8V/3.3V mode Select
GPIO_78	
0	3.3V
1	1.8V (default)

PMU 1.8V/3.3V Mode Select
GPIO_88	
0	3.3V
1	1.8V (default)

SOC_CLK_PCU_RTC

U1H — APL_SOC / APLI_SOC_DDR3L

Blocks: ICLK, PMC, RTC, SVID, THERMAL, ITP/JTAG, PMU

Oscillator / Clocks
- C8 10pF/50V/04
- C10 10pF/50V/04
- Y1 19.200MHz 20PF 20ppm 4P
- R131 200K-1-04
- XTAL19.2_IN
- XTAL19.2_OUT
- OSCIN — R27
- OSCOUT — P29
- C9 18pF/50V/04
- C11 18pF/50V/04
- Y2 32.768KHz 12.5pF +-20PPM 2P
- R132 10M/R0402
- RTC_X1 / RTC_X2 — AC59 / AC58

OSC_CLK_OUT
- 20 OSC_CLK_OUT_3 — OSC_CLK_OUT_4 — AF62
- 20 OSC_CLK_OUT_2 — OSC_CLK_OUT_3 — AE60
- 38 OSC_CLK_OUT_1 — OSC_CLK_OUT_2 — AG63
- 38 OSC_CLK_OUT_0 — OSC_CLK_OUT_1 — AF61
- OSC_CLK_OUT_0 — AG62

PMC GPIO
- GPIO_224 — J45 — DDR_CH
- GPIO_213 — M47 — mSATA_PCIe_SEL_N
- GPIO_223 — F48
- GPIO_222 — J48
- PMIC_I2C_SDA — F47 — PMIC_I2C_SDA 42
- PMIC_I2C_SCL — H45 — PMIC_I2C_SCL 42
- GPIO_214 — L47 — DDR_ID0
- GPIO_215 — P47 — DDR_ID1
- PMC_SPI_TXD — H50
- PMC_SPI_RXD — J50
- PMC_SPI_FS2 — M48
- PMC_SPI_FS1 — P48
- PMC_SPI_FS0 — L48 — EDP_HPD_CONN_N 21
- PMC_SPI_CLK — C52

RTC
- RTC_TEST# — AH49 — RTC_TEST
- RTC_RST# — AC55 — RTC_RST
- PM_RSMRST# — AC57 — RSM_RST
- VCC_RTC_EXTPAD — AG51
- C12 0.1uF/16VX/04

SVID
- SVID0_CLK — C17 — VR_SVID_CLK
- SVID0_DATA — C18 — VR_SVID_DATA
- SVID0_ALERT_B — B17 — VR_SVID_ALERT#

PMU
- 22 PMU_M2_SUSCLK — PMU_M2_SUSCLK — R138 33/R0402 — PMU_SUSCLK — AE62
- 43 SUS_STAT# — SUSPWRDNACK — AG58 — SUS_STAT
- TP38 — SUSPWRDNACK — AC63
- 35,42 PCH_PWROK — SOC_PWROK — AG49
- 42 PM_SLP_S4#_3P3 — PM_SLP_S4#_3P3 — R140 0-04 — PMU_SLP_S4# — AK54
- 42,43 PM_SLP_S3#_3P3 — R141 0-04 — PMU_SLP_S3# — AC62
- 25,26,27,33,36,42 PM_SLP_S0#_3P3 — R142 0-04 — PMU_SLP_S0# — AD61
- PLT_RST#_3P3 — R145 0-04 — PM_PWRBTN# — AK55 — PMU_PWRBTN
- PMU_WAKE_N — PM_SYSRST# — AD62 — PMU_RSTBTN
- PM_PLTRST# — AG57 — PMU_PLTRST
- AG55 — EMMC_PWR_EN
- PM_BATLOW# — AH51 — PMU_BATLOW
- AC_PRESENT — AK49 — PMU_AC_PRESENT
- INTRUDER — AC54 — EMMC_RCOMP
- PMU_RCOMP — AG59
- R156 200-1-04

THERMAL
- PROCHOT — E47 — PROCHOT#
- THERMTRIP — J47 — THERMTRIP#
- RSVD_AG54 — AG54
- RSVD_AG52 — AG52
- RSVD_J43 — J43
- RSVD_H43 — H43

ITP/JTAG
- JTAG_TCK — B23 — R144 X/51.1-1-04
- JTAG_TRST — C24 — R146 X/51.1-1-04
- JTAG_TMS — C23 — R148 X/51.1-1-04
- JTAG_TDI — C22 — R150 X/51.1-1-04
- JTAG_TDO — A22 — R151 X/100-04
- JTAG_PREQ — C20 — R152 X/100-04
- JTAG_PRDY — C21 — R153 X/100-04
- JTAG_PMODE — B19
- JTAGX — B21

Battery / RTC power
- CN1 2P 712-71-02TW01
- D1 BAT54CW
- R161 1K-04
- R160 20K-04 — RTC_RST#
- C13 1uF/16V/04
- C14 1uF/16V/04
- R165 20K-04 — RTC_TEST#
- C15 1uF/16V/04
- M1 Battery BP-CR2032-M150-00 REV:A0.3

Right side power / MOSFETs
- +V3.3A
- AC_PRESENT — R133 10K-04 — PM_BATLOW# — R134 10K-04
- PMU_WAKE_N — R135 1K-04
- INTRUDER — R136 100K-04 — +V3.3A_RTC
- PM_PLTRST# — R139 X/10K-04
- PMIC_I2C_SDA — R147 X/1K-04
- PMIC_I2C_SCL — R149 X/1K-04
- VR_SVID_CLK — R154 X/84.5-1-06 +V1.05S
- VR_SVID_DATA — R155 X/169-1-06
- R157 X/68/R0402 +V1.05S
- VR_SVID_ALERT# — R158 X/220-1-04

- R701 10K-04 — PM_SYSRST#
- R702 10K-04 — Q41A EM6K1GT2R — Q41B EM6K1GT2R
- R178 10K-04 — CN3 2*1P
- R162 10K-04 — R163 10K-04 — PMIC_THERMTRIP# 42 — Q4A/Q4B EM6K1GT2R
- R796 10K-04 — mSATA_PCIe_SEL 23 — Q6B EM6K1GT2R
- mSATA_PCIe_SEL_N
- THERMTRIP#
- R171 10K-04 — PROCHOT# — Q6A EM6K1GT2R — 42 PROCHOT
- BUF_PLT_RST#
- R164 10K-04 — PM_PWRBTN#_GPIO16 12 — Q5A/Q5B EM6K1GT2R
- R166 10K-04
- R167 10K-04
- SW1 3P 12VDC — R1690-04 — PM_PWRBTN# — CN2 2*1P

U9 / U65 gates
- U9 SN74LVC1G08DCKR
- PLT_RST#_3P3 — A/B/GND/VCC/Y — BUF_PLT_RST# 22,23,30,31,34
- C107 0.1uF/16V/04 — R195 100K-04
- U65 SN74LVC1G08DCKR — 42 PMIC_RSMRST#_3P3 — PM_RSMRST#
- C535 X/0.1uF/16VX/04 — C536 0.1uF/16VX/04 — R180 100K-04

DDR configuration table (REV:A0.2)

DDR_CH	Channel
0	1
1	2

DDR_ID1	DDR_ID0	Memory
0	0	2GB
0	1	4GB
1	0	8GB

- DDR_CH — R790 2.2K-04 — R791 X/2.2K-04 +V1.8A
- DDR_ID0 — R792 2.2K-04 — R793 X/2.2K-04 +V1.8A
- DDR_ID1 — R794 X/2.2K-04 — R795 2.2K-04 +V1.8A

+VCGI_SVID

+VNN_SVID

+VNN_SVID

U1K
APL_SOC

C28 1uF/16V/04	C31 1uF/16V/04	C23 1uF/16V/04	C24 1uF/16V/04
C25 1uF/16V/04	C33 1uF/16V/04	C26 1uF/16V/04	C27 1uF/16V/04
C38 1uF/16V/04	C39 1uF/16V/04	C40 1uF/16V/04	C41 1uF/16V/04
C46 22uF/6.3V/06	C47 22uF/6.3V/06	C48 22uF/6.3V/06	C49 22uF/6.3V/06
C56 22uF/6.3V/06	C57 22uF/6.3V/06	C58 22uF/6.3V/06	C59 22uF/6.3V/06
C60 47uF_6.3V/C0805	C61 47uF_6.3V/C0805	C62 47uF_6.3V/C0805	
C68 0.1uF/16VX/04	C69 0.1uF/16VX/04		

AA36 VCC_VCGI_AA36
AA37 VCC_VCGI_AA37
AA39 VCC_VCGI_AA39
AC36 VCC_VCGI_AC36
AC37 VCC_VCGI_AC37
AE36 VCC_VCGI_AE36
AE37 VCC_VCG_AE37
AG36 VCC_VCGI_AG36
E43 VCC_VCGI_E43
E45 VCC_VCGI_E45
E48 VCC_VCGI_E48
E50 VCC_VCGI_E50
R45 VCC_VCGI_R45
R47 VCC_VCGI_R47
U36 VCC_VCGI_U36
U37 VCC_VCGI_U37
U39 VCC_VCGI_U39
U41 VCC_VCGI_U41
U42 VCC_VCGI_U42
U44 VCC_VCGI_U44
U46 VCC_VCGI_U46
U47 VCC_VCGI_U47
U48 VCC_VCGI_U48
V36 VCC_VCGI_V36
V37 VCC_VCGI_V37
V39 VCC_VCGI_V39
V41 VCC_VCGI_V41
Y36 VCC_VCGI_Y36
Y37 VCC_VCGI_Y37
Y39 VCC_VCGI_Y39
Y41 VCC_VCGI_Y41
AA28 VCC_VCGI_AA28
AA30 VCC_VCGI_AA30
AA32 VCC_VCGI_AA32
AC28 VCC_VCGI_AC28
AC30 VCC_VCGI_AC30
AC32 VCC_VCGI_AC32
AE28 VCC_VCGI_AE28
AE30 VCC_VCGI_AE30
AE32 VCC_VCGI_AE32
AG28 VCC_VCGI_AG28
AG30 VCC_VCGI_AG30
AG32 VCC_VCGI_AG32
AJ28 VCC_VCGI_AJ28
AJ30 VCC_VCGI_AJ30
AJ32 VCC_VCGI_AJ32
AK28 VCC_VCGI_AK28
AK30 VCC_VCGI_AK30
AK32 VCC_VCGI_AK32
AK34 VCC_VCGI_AK34
AM30 VCC_VCGI_AM30
E29 VCC_VCGI_E29
E35 VCC_VCGI_E35
E37 VCC_VCGI_E37
F29 VCC_VCGI_F29
U28 VCC_VCGI_U28
U30 VCC_VCGI_U30
U32 VCC_VCGI_U32
V28 VCC_VCGI_V28
V30 VCC_VCGI_V30
V32 VCC_VCGI_V32
Y28 VCC_VCGI_Y28
Y30 VCC_VCGI_Y30
Y32 VCC_VCGI_Y32

POWER 1

APLI_SOC_DDR3L

RSVD3 AJ44 — R182 X/0-04

C19 22uF/6.3V/06	C20 22uF/6.3V/06	C21 22uF/6.3V/06	C22 22uF/6.3V/06
C29 1uF/16V/04	C30 1uF/16V/04	C32 1uF/16V/04	
C34 0.1uF/16VX/04	C35 0.1uF/16VX/04	C36 0.1uF/16VX/04	C37 0.1uF/16VX/04

VNN_SVID_AJ37 AJ37
VNN_SVID_AJ39 AJ39
VNN_SVID_AJ41 AJ41
VNN_SVID_AJ42 AJ42
VNN_SVID_AJ46 AJ46
VNN_SVID_AK37 AK37
VNN_SVID_AK39 AK39
VNN_SVID_AK41 AK41
VNN_SVID_AK42 AK42
VNN_SVID_AK44 AK44
VNN_SVID_AK46 AK46
VNN_SVID_AM44 AM44

VNN_SENSE AG48 — SOC_VNN_SENSE 41

VCCIOA CONNECTION=
LPDDR4 : VDDQ
DDR3L : VNN_SVID

REV:A0.2 VCCIOA

REV:A0.2

+VDDQ +VNN_SVID
R766 0.01-1-06 R767 X/0.01-1-06

VCCIOA_AM23 AM23
VCCIOA_AM25 AM25
VCCIOA_AM41 AM41
VCCIOA_AM42 AM42

C42 1uF/16V/04	C43 1uF/16V/04	C44 22uF/6.3V/06	C45 22uF/6.3V/06

+VCCRAM_1P05 R183 0.01-1-06 +V1.05S

VCCRAM_1P05_AA25 AA25
VCCRAM_1P05_AC25 AC25
VCCRAM_1P05_AE25 AE25
VCCRAM_1P05_U23 U23
VCCRAM_1P05_V22 V22
VCCRAM_1P05_V23 V23
VCCRAM_1P05_Y23 Y23
VCCRAM_1P05_Y25 Y25
VCCRAM_1P05_U25 U25
VCCRAM_1P05_U20 U20
VCCRAM_1P05_U22 U22

C50 1uF/16V/04	C51 1uF/16V/04	C52 1uF/16V/04	C53 1uF/16V/04	C54 22uF/6.3V/06	C55 22uF/6.3V/06

2x 0402 1uF BSC, 2x 0402 1uF EDC, 2x 0603 22uF
Layout Note: Place CAPS PLACE CAPS NEAR SOC PIN AE25, AC25, AA25, Y25, V25, U25, Y23, V23, U23, V22, U22, U20

VCCRAM_1P05_IO_AA22 AA22
VCCRAM_1P05_IO_AC23 AC23
VCCRAM_1P05_IO_V18 V18
VCCRAM_1P05_IO_Y18 Y18
VCCRAM_1P05_IO_Y20 Y20
VCCRAM_1P05_IO2 AA23

+VCCRAM_1P05_IO R184 0.01-1-06 +V1.05S

C63 1uF/16V/04	C64 1uF/16V/04	C65 1uF/16V/04	C66 1uF/16V/04	C67 22uF/6.3V/06

2x 0402 1uF BSC, 2x 0402 1uF EDC, 1x 0603 22uF
Layout Note: Place CAPS near SOC PIN AC23, AA23, AA22, Y20, Y18, V18

VCC_1P05_INT1 P16
VCC_1P05_INT3 T15
VCC_1P05_INT2 T13

+VCCRAM_1P05_FUSE
+VCCRAM_1P05_FHV1
+VCCRAM_1P05_FHV0

NCTF16 R25 — TP18

VCC_VCGI_SENSE R43
VCC_VCGI_SENSE_P R41

SOC_VCC_VSSSENSE 41
SOC_VCC_SENSE 41

+VCCRAM_1P05_FUSE R185 0-04 +V1.05S
+VCCRAM_1P05_FHV1 R186 0-04
+VCCRAM_1P05_FHV0 R187 0-04

<Core Design>

Title: SOC_POWER I
Size: Custom
Document Number: UP-APL01
Rev: A0.3
Date: Wednesday, January 04, 2017

+V1.24A   R188 0.01-1-06   +VDD2_1P24_USB2   +V1.24A

1x 0402 1uF BSC
Layout Note: Place CAPS near SOC PIN AG20
C70 1uF/16V/04

+V1.24A   R189 0.01-1-06   +VDD2_1P24_MPHY

C71 1uF/16V/04   C72 1uF/16V/04   C73 22uF/6.3V/06

+VDDQ

C74 1uF/16V/04   C75 1uF/16V/04   C76 1uF/16V/04   C77 22uF/6.3V/06

1x 0402 1uF BSC, 1x 0402 1uF EDC
Layout Note: Place CAPS near SOC PIN AK22, AJ20, AJ22

Layout Note: Place CAPS near SOC PIN

2x 0402 1uF BSC, 1x 0402 1uF EDC, 1x 0603 22uF
Layout Note: Place CAPS near SOC PIN AE18, AE20, AE22, AG22

C78 22uF/6.3V/06   C79 22uF/6.3V/06   C80 22uF/6.3V/06   C81 22uF/6.3V/06

+V1.24A   R190 0.01-1-06   +VDD2_1P24_GLML2

U1L   APL_SOC

AJ20   VDD2_1P24_AUD_ISH_PLL_AJ20
AJ22   VDD2_1P24_AUD_ISH_PLL_AJ22

VDDQ_AN18   AN18
VDDQ_AN20   AN20
VDDQ_AN22   AN22
VDDQ_AN23   AN23
VDDQ_AN41   AN41
VDDQ_AN42   AN42
VDDQ_AN44   AN44
VDDQ_AN46   AN46
VDDQ_AR17   AR17
VDDQ_AR47   AR47
VDDQ_AT13   AT13
VDDQ_AT17   AT17
VDDQ_AT47   AT47
VDDQ_AT51   AT51
VDDQ_AV14   AV14
VDDQ_AV50   AV50

C82 22uF/6.3V/06   C83 22uF/6.3V/06   C84 22uF/6.3V/06   C85 22uF/6.3V/06

C86 1uF/16V/04   C87 1uF/16V/04   C88 1uF/16V/04   C89 1uF/16V/04   C90 22uF/6.3V/06

AG20   VDD2_1P24_USB2

AE18   VDD2_1P24_MPHY_AE18
AE20   VDD2_1P24_MPHY_AE20
AE22   VDD2_1P24_MPHY_AE22
AG22   VDD2_1P24_MPHY_AG22

AM20   VDD2_1P24_GLM_AM20
AM28   VDD2_1P24_GLM_AM28
AM37   VDD2_1P24_GLM_AM37
AK20   VDD2_1P24_GLM_AK20

POWER 2

3x 0402 1uF BSC, 1x 0402 1uF EDC, 1x 0603 22uF
Layout Note: Place CAPS near SOC PIN AK20, AM37, AM20. 1*1uF for AM28

+V1.24A   R191 0.01-1-06   +VDD2_1P24_DSI

AA18   VDD2_1P24_DSI_CSI_AA18
AA20   VDD2_1P24_DSI_CSI_AA20

RSVD_AM32   AM32   TP19

+V3.3A   1x 0402 1uF BSC, 1x 0402 1uF EDC
Layout Note: Place CAPS near SOC PIN AC41, AA42, Y44, V46, V44

C92 1uF/16V/04   C93 1uF/16V/04   C94 22uF/6.3V/06   C95 X/22uF_6.3V/C0603

+V1.24A   R192   X/0-04

AK22   VDD2_1P24_AUD_ISH_PLL_AK22
AC20   RSVD_AC20

C91 1uF/16V/04   C96 1uF/16V/04   C97 1uF/16V/04   C98 22uF/6.3V/06

1x 0402 1uF BSC, 1x 0402 1uF EDC, 1x 0603 22uF
Layout Note: Place CAPS near SOC PIN AA18, AA20

VCC_3P3V_A_AC41   AC41
VCC_3P3V_A_AA42   AA42
VCC_3P3V_A_Y44   Y44
VCC_3P3V_A_V44   V44
VCC_3P3V_A_V46   V46
VCC_3P3V_A_AJ25   AJ25
VCC_3P3V_A_AK25   AK25

Shared 1x 0603 22uF
Layout Note: Place CAPS near SOC PIN

AA46   VCC_1P8V_A_AA46
AC46   VCC_1P8V_A_AC46
AE44   VCC_1P8V_A_AE44
AE42   VCC_1P8V_A_AE42
AC44   VCC_1P8V_A_AC44
AE46   VCC_1P8V_A_AE46
AG25   VCC_1P8V_A_AG25

+V3.3A

+V1.8A

+V3.3A_RTC

1x 0402 1uF BSC, 1x 0402 1uF EDC
Layout Note: Place CAPS near SOC PIN AJ25, AK25

2x 0402 1uF BSC
Layout Note: Place CAPS near SOC PIN
AA46, AC46, AE46, AE44, AC44, AE42

AC42   VCC_1P8V_A_AC42

VCCRTC_3P3V   AA44

C99 1uF/16V/04

C100 1uF/16V/04   C101 1uF/16V/04   C102 1uF/16V/04

1x 0402 1uF BSC
CAP near AG25

APLI_SOC_DDR3L

C103 22uF/6.3V/06

1x 0603 22uF
Layout Note: Place CAPS near SOC PIN

2x 0402 1uF EDC, 1x 0603 22uF
Layout Note: Place CAPS near SOC PIN

C104 1uF/16V/04   C105 1uF/16V/04   C106 22uF/6.3V/06

<Core Design>

REV:A0.2

U10

MT53B256M32D1NP-062WT

7 DDR0_DQ_A[31:0]

Net	Pin
DDR0_DQ_A0	B2 DQ0_A
DDR0_DQ_A7	C2 DQ1_A
DDR0_DQ_A5	E2 DQ2_A
DDR0_DQ_A6	F2 DQ3_A
DDR0_DQ_A2	F4 DQ4_A
DDR0_DQ_A3	E4 DQ5_A
DDR0_DQ_A4	C4 DQ6_A
DDR0_DQ_A1	B4 DQ7_A
DDR0_DQ_A8	B11 DQ8_A
DDR0_DQ_A13	C11 DQ9_A
DDR0_DQ_A12	E11 DQ10_A
DDR0_DQ_A11	F11 DQ11_A
DDR0_DQ_A15	F9 DQ12_A
DDR0_DQ_A10	E9 DQ13_A
DDR0_DQ_A14	C9 DQ14_A
DDR0_DQ_A9	B9 DQ15_A
DDR0_DQ_A23	AA2 DQ0_B
DDR0_DQ_A17	Y2 DQ1_B
DDR0_DQ_A19	V2 DQ2_B
DDR0_DQ_A18	U2 DQ3_B
DDR0_DQ_A20	U4 DQ4_B
DDR0_DQ_A21	V4 DQ5_B
DDR0_DQ_A22	Y4 DQ6_B
DDR0_DQ_A16	AA4 DQ7_B
DDR0_DQ_A28	AA11 DQ8_B
DDR0_DQ_A29	Y11 DQ9_B
DDR0_DQ_A25	V11 DQ10_B
DDR0_DQ_A31	U11 DQ11_B
DDR0_DQ_A24	U9 DQ12_B
DDR0_DQ_A26	V9 DQ13_B
DDR0_DQ_A30	Y9 DQ14_B
DDR0_DQ_A27	AA9 DQ15_B

Net	Pin
7 DDR0_DQS_T_A0	DDR0_DQS_T_A0 D3 DQS0_t_A
7 DDR0_DQS_C_A0	DDR0_DQS_C_A0 E3 DQS0_c_A
7 DDR0_DQS_T_A1	DDR0_DQS_T_A1 D10 DQS1_t_A
7 DDR0_DQS_C_A1	DDR0_DQS_C_A1 E10 DQS1_c_A
7 DDR0_DQS_T_A2	DDR0_DQS_T_A2 W3 DQS0_t_B
7 DDR0_DQS_C_A2	DDR0_DQS_C_A2 V3 DQS0_c_B
7 DDR0_DQS_T_A3	DDR0_DQS_T_A3 W10 DQS1_t_B
7 DDR0_DQS_C_A3	DDR0_DQS_C_A3 V10 DQS1_c_B

7 DDR_RESET_N — DDR_RESET_N T11 RESET_n

Pin	Signal	Net
H2	CA0_A	DDR0_CA_A_0 → DDR0_CA_A_0 7
J2	CA1_A	DDR0_CA_A_1 → DDR0_CA_A_1 7
H9	CA2_A	DDR0_CA_A_2 → DDR0_CA_A_2 7
H10	CA3_A	DDR0_CA_A_3 → DDR0_CA_A_3 7
H11	CA4_A	DDR0_CA_A_4 → DDR0_CA_A_4 7
J11	CA5_A	DDR0_CA_A_5 → DDR0_CA_A_5 7
R2	CA0_B	DDR0_CA_A_0
P2	CA1_B	DDR0_CA_A_1
R9	CA2_B	DDR0_CA_A_2
R10	CA3_B	DDR0_CA_A_3
R11	CA4_B	DDR0_CA_A_4
P11	CA5_B	DDR0_CA_A_5
J8	CK_t_A	DDR0_CK1_T_A → DDR0_CK1_T_A 7
J9	CK_c_A	DDR0_CK1_C_A → DDR0_CK1_C_A 7
P8	CK_t_B	DDR0_CK1_T_A
P9	CK_c_B	DDR0_CK1_C_A
C3	DMI0_A	
C10	DMI1_A	
Y3	DMI0_B	
Y10	DMI1_B	
H4	CS0_A	DDR0_CS0_A → DDR0_CS0_A 7
H3	CS1_A	DDR0_CS1_A → DDR0_CS1_A 7
K5	CS2_A	
R4	CS0_B	DDR0_CS0_A
R3	CS1_B	DDR0_CS1_A
N5	CS2_B	
J4	CKE0_A	DDR0_CKE0_A → DDR0_CKE0_A 7
J5	CKE1_A	DDR0_CKE1_A → DDR0_CKE1_A 7
K8	CKE2_A	
P4	CKE0_B	DDR0_CKE0_A
P5	CKE1_B	DDR0_CKE1_A
N8	CKE2_B	
A5	ZQ0	R205 240-1-04 +VDDQ
A8	ZQ1	R206 240-1-04 +VDDQ
G11	ZQ2	
G2	ODT_CA_A	+VDDQ
T2	ODT_CA_B	+VDDQ

DNU1 A1
DNU2 A2
DNU3 A11
DNU4 A12
DNU5 B1
DNU6 B12
DNU7 AA1
DNU8 AA12
DNU9 AB1
DNU10 AB2
DNU11 AB11
DNU12 AB12

+VDDQ   +VDDQ   +V1.8A

Ref	Value
C110	0.1uF/16VX/04
C111	4.7uF/6.3V/04
C112	4.7uF/6.3V/04
C113	10uF/10V-06
C114	22uF/6.3V/06
C115	22uF/6.3V/06
C122	0.1uF/16VX/04
C123	4.7uF/6.3V/04
C124	10uF/10V-06
C125	22uF/6.3V/06

Title	**LPDDR4 (1/4)**
Size: Custom	Document Number: UP-APL01
Rev: A0.3	
Date: Wednesday, January 04, 2017	Sheet: 16 of 45

U11
MT53B256M32D1NP-062WT

DDR0_DQ_B[31:0]

DDR0_DQ_B1 B2 DQ0_A
DDR0_DQ_B5 C2 DQ1_A
DDR0_DQ_B7 E2 DQ2_A
DDR0_DQ_B2 F2 DQ3_A
DDR0_DQ_B3 F4 DQ4_A
DDR0_DQ_B6 E4 DQ5_A
DDR0_DQ_B0 C4 DQ6_A
DDR0_DQ_B4 B4 DQ7_A
DDR0_DQ_B10 B11 DQ8_A
DDR0_DQ_B15 C11 DQ9_A
DDR0_DQ_B9 E11 DQ10_A
DDR0_DQ_B11 F11 DQ11_A
DDR0_DQ_B12 F9 DQ12_A
DDR0_DQ_B8 E9 DQ13_A
DDR0_DQ_B14 C9 DQ14_A
DDR0_DQ_B13 B9 DQ15_A
DDR0_DQ_B16 AA2 DQ0_B
DDR0_DQ_B23 Y2 DQ1_B
DDR0_DQ_B21 V2 DQ2_B
DDR0_DQ_B22 U2 DQ3_B
DDR0_DQ_B20 U4 DQ4_B
DDR0_DQ_B18 V4 DQ5_B
DDR0_DQ_B19 Y4 DQ6_B
DDR0_DQ_B17 AA4 DQ7_B
DDR0_DQ_B31 AA11 DQ8_B
DDR0_DQ_B26 Y11 DQ9_B
DDR0_DQ_B25 V11 DQ10_B
DDR0_DQ_B27 U11 DQ11_B
DDR0_DQ_B24 U9 DQ12_B
DDR0_DQ_B28 V9 DQ13_B
DDR0_DQ_B30 Y9 DQ14_B
DDR0_DQ_B29 AA9 DQ15_B

DDR0_DQS_T_B0 D3 DQS0_t_A
DDR0_DQS_C_B0 E3 DQS0_c_A
DDR0_DQS_T_B1 D10 DQS1_t_A
DDR0_DQS_C_B1 E10 DQS1_c_A
DDR0_DQS_T_B2 W3 DQS0_t_B
DDR0_DQS_C_B2 V3 DQS0_c_B
DDR0_DQS_T_B3 W10 DQS1_t_B
DDR0_DQS_C_B3 V10 DQS1_c_B

DDR_RESET_N T11 RESET_n

CA0_A H2 DDR0_CA_B_0 → DDR0_CA_B_0 7
CA1_A J2 DDR0_CA_B_1 → DDR0_CA_B_1 7
CA2_A H9 DDR0_CA_B_2 → DDR0_CA_B_2 7
CA3_A H10 DDR0_CA_B_3 → DDR0_CA_B_3 7
CA4_A H11 DDR0_CA_B_4 → DDR0_CA_B_4 7
CA5_A J11 DDR0_CA_B_5 → DDR0_CA_B_5 7
CA0_B R2 DDR0_CA_B_0
CA1_B P2 DDR0_CA_B_1
CA2_B R9 DDR0_CA_B_2
CA3_B R10 DDR0_CA_B_3
CA4_B R11 DDR0_CA_B_4
CA5_B P11 DDR0_CA_B_5

CK_t_A J8 DDR0_CK0_T_B → DDR0_CK0_T_B 7
CK_c_A J9 DDR0_CK0_C_B → DDR0_CK0_C_B 7
CK_t_B P8 DDR0_CK0_T_B
CK_c_B P9 DDR0_CK0_C_B

DMI0_A C3
DMI1_A C10
DMI0_B Y3
DMI1_B Y10

CS0_A H4 DDR0_CS0_B → DDR0_CS0_B 7
CS1_A H3 DDR0_CS1_B → DDR0_CS1_B 7
CS2_A K5
CS0_B R4 DDR0_CS0_B
CS1_B R3 DDR0_CS1_B
CS2_B N5

CKE0_A J4 DDR0_CKE0_B → DDR0_CKE0_B 7
CKE1_A J5 DDR0_CKE1_B → DDR0_CKE1_B 7
CKE2_A K8
CKE0_B P4 DDR0_CKE0_B
CKE1_B P5 DDR0_CKE1_B
CKE2_B N8

ZQ0 A5 R230 240-1-04 +VDDQ
ZQ1 A8 R231 240-1-04 +VDDQ
ZQ2 G11

ODT_CA_A G2 +VDDQ
ODT_CA_B T2 +VDDQ

DNU1 A1
DNU2 A2
DNU3 A11
DNU4 A12
DNU5 B1
DNU6 B12
DNU7 AA1
DNU8 AA12
DNU9 AB1
DNU10 AB2
DNU11 AB11
DNU12 AB12

REV:A0.2

+VDDQ   +VDDQ   +V1.8A

+VDDQ   +V1.8A

C116 0.1uF/16VX/04
C117 4.7uF/6.3V/04
C118 4.7uF/6.3V/04
C119 10uF/10V-06
C120 22uF/6.3V/06
C121 22uF/6.3V/06
C600 X/22uF/6.3V/06
REV:A0.3
C126 0.1uF/16VX/04
C127 4.7uF/6.3V/04
C128 10uF/10V-06
C129 22uF/6.3V/06

REV:A0.2

U71

Left side signals (DQ):

Signal	Pin	Net
DDR1_DQ_A0	B2	DQ0_A
DDR1_DQ_A7	C2	DQ1_A
DDR1_DQ_A5	E2	DQ2_A
DDR1_DQ_A4	F2	DQ3_A
DDR1_DQ_A2	F4	DQ4_A
DDR1_DQ_A1	E4	DQ5_A
DDR1_DQ_A6	C4	DQ6_A
DDR1_DQ_A3	B4	DQ7_A
DDR1_DQ_A10	B11	DQ8_A
DDR1_DQ_A11	C11	DQ9_A
DDR1_DQ_A9	E11	DQ10_A
DDR1_DQ_A8	F11	DQ11_A
DDR1_DQ_A14	F9	DQ12_A
DDR1_DQ_A15	E9	DQ13_A
DDR1_DQ_A13	C9	DQ14_A
DDR1_DQ_A15	B9	DQ15_A
DDR1_DQ_A23	AA2	DQ0_B
DDR1_DQ_A21	Y2	DQ1_B
DDR1_DQ_A16	V2	DQ2_B
DDR1_DQ_A19	U2	DQ3_B
DDR1_DQ_A18	U4	DQ4_B
DDR1_DQ_A22	V4	DQ5_B
DDR1_DQ_A17	Y4	DQ6_B
DDR1_DQ_A20	AA4	DQ7_B
DDR1_DQ_A29	AA11	DQ8_B
DDR1_DQ_A24	Y11	DQ9_B
DDR1_DQ_A31	V11	DQ10_B
DDR1_DQ_A27	U11	DQ11_B
DDR1_DQ_A30	U9	DQ12_B
DDR1_DQ_A26	V9	DQ13_B
DDR1_DQ_A28	Y9	DQ14_B
DDR1_DQ_A25	AA9	DQ15_B

7 DDR1_DQ_A[31:0]

DQS signals:

Signal	Pin	Net
7 DDR1_DQS_T_A0	D3	DQS0_t_A
7 DDR1_DQS_C_A0	E3	DQS0_c_A
7 DDR1_DQS_T_A1	D10	DQS1_t_A
7 DDR1_DQS_C_A1	E10	DQS1_c_A
7 DDR1_DQS_T_A2	W3	DQS0_t_B
7 DDR1_DQS_C_A2	V3	DQS0_c_B
7 DDR1_DQS_T_A3	W10	DQS1_t_B
7 DDR1_DQS_C_A3	V10	DQS1_c_B

7 DDR_RESET_N   DDR_RESET_N   T11   RESET_n

Right side signals (CA):

Pin	Net	Signal	Sheet
H2	CA0_A	DDR1_CA_A_0	DDR1_CA_A_0 7
J2	CA1_A	DDR1_CA_A_1	DDR1_CA_A_1 7
H9	CA2_A	DDR1_CA_A_2	DDR1_CA_A_2 7
H10	CA3_A	DDR1_CA_A_3	DDR1_CA_A_3 7
H11	CA4_A	DDR1_CA_A_4	DDR1_CA_A_4 7
J11	CA5_A	DDR1_CA_A_5	DDR1_CA_A_5 7
R2	CA0_B	DDR1_CA_A_0	
P2	CA1_B	DDR1_CA_A_1	
R9	CA2_B	DDR1_CA_A_2	
R10	CA3_B	DDR1_CA_A_3	
R11	CA4_B	DDR1_CA_A_4	
P11	CA5_B	DDR1_CA_A_5	

Pin	Net	Signal	Sheet
J8	CK_t_A	DDR1_CK1_T_A	DDR1_CK1_T_A 7
J9	CK_c_A	DDR1_CK1_C_A	DDR1_CK1_C_A 7
P8	CK_t_B	DDR1_CK1_T_A	
P9	CK_c_B	DDR1_CK1_C_A	

Pin	Net
C3	DMI0_A
C10	DMI1_A
Y3	DMI0_B
Y10	DMI1_B

Pin	Net	Signal	Sheet
H4	CS0_A	DDR1_CS0_A	DDR1_CS0_A 7
H3	CS1_A	DDR1_CS1_A	DDR1_CS1_A 7
K5	CS2_A		
R4	CS0_B	DDR1_CS0_A	
R3	CS1_B	DDR1_CS1_A	
N5	CS2_B		

Pin	Net	Signal	Sheet
J4	CKE0_A	DDR1_CKE0_A	DDR1_CKE0_A 7
J5	CKE1_A	DDR1_CKE1_A	DDR1_CKE1_A 7
K8	CKE2_A		
P4	CKE0_B	DDR1_CKE0_A	
P5	CKE1_B	DDR1_CKE1_A	
N8	CKE2_B		

Pin	Net
A5	ZQ0
A8	ZQ1
G11	ZQ2

R777 240-1-04 +VDDQ
R778 240-1-04 +VDDQ

Pin	Net
G2	ODT_CA_A +VDDQ
T2	ODT_CA_B +VDDQ

DNU pins: A1, A2, A11, A12, B1, B12, AA1, AA12, AB1, AB2, AB11, AB12
(DNU1–DNU12)

MT53B256M32D1NP-062WT

Power pins:
VDD2: A4, A9, F5, F8, H1, H5, H8, H12, K3, K7, K9, K10, K12, N1, N3, N10, N12, R1, R5, R8, R12, U5, U8, AB4, AB9 — +VDDQ

VDDQ: B3, B5, B8, B10, D1, D5, D8, D12, F3, F10, U3, U10, W1, W5, W8, W12, AA3, AA5, AA8, AA10 — +VDDQ

VDD1: F1, F12, G4, G9, T4, T9, U1, U12 — +V1.8A

Bottom capacitor bank (+VDDQ):
C566 0.1uF/16VX/04 · C567 4.7uF/6.3V/04 · C568 4.7uF/6.3V/04 · C569 10uF/10V-06 · C570 22uF/6.3V/06 · C571 22uF/6.3V/06

Bottom capacitor bank (+V1.8A):
C572 0.1uF/16VX/04 · C573 4.7uF/6.3V/04 · C574 10uF/10V-06 · C575 22uF/6.3V/06

REV:A0.2

U72

MT53B256M32D1NP-062WT

DDR1_DQ_B[31:0]

Signal	Pin		Pin	Signal
DDR1_DQ_B6	B2	DQ0_A		
DDR1_DQ_B2	C2	DQ1_A		
DDR1_DQ_B4	E2	DQ2_A		
DDR1_DQ_B5	F2	DQ3_A		
DDR1_DQ_B0	F4	DQ4_A		
DDR1_DQ_B7	E4	DQ5_A		
DDR1_DQ_B3	C4	DQ6_A		
DDR1_DQ_B1	B4	DQ7_A		
DDR1_DQ_B9	B11	DQ8_A		
DDR1_DQ_B15	C11	DQ9_A		
DDR1_DQ_B10	E11	DQ10_A		
DDR1_DQ_B12	F11	DQ11_A		
DDR1_DQ_B8	F9	DQ12_A		
DDR1_DQ_B6	E9	DQ13_A		
DDR1_DQ_B11	C9	DQ14_A		
DDR1_DQ_B13	B9	DQ15_A		
DDR1_DQ_B19	AA2	DQ0_B		
DDR1_DQ_B16	Y2	DQ1_B		
DDR1_DQ_B21	V2	DQ2_B		
DDR1_DQ_B17	U2	DQ3_B		
DDR1_DQ_B23	U4	DQ4_B		
DDR1_DQ_B18	V4	DQ5_B		
DDR1_DQ_B20	Y4	DQ6_B		
DDR1_DQ_B22	AA4	DQ7_B		
DDR1_DQ_B24	AA11	DQ8_B		
DDR1_DQ_B25	Y11	DQ9_B		
DDR1_DQ_B27	V11	DQ10_B		
DDR1_DQ_B31	U11	DQ11_B		
DDR1_DQ_B26	U9	DQ12_B		
DDR1_DQ_B28	V9	DQ13_B		
DDR1_DQ_B29	Y9	DQ14_B		
DDR1_DQ_B30	AA9	DQ15_B		

DDR1_DQS_T_B0 D3 DQS0_t_A
DDR1_DQS_C_B0 E3 DQS0_c_A
DDR1_DQS_T_B1 D10 DQS1_t_A
DDR1_DQS_C_B1 E10 DQS1_c_A
DDR1_DQS_T_B2 W3 DQS0_t_B
DDR1_DQS_C_B2 V3 DQS0_c_B
DDR1_DQS_T_B3 W10 DQS1_t_B
DDR1_DQS_C_B3 V10 DQS1_c_B

DDR_RESET_N T11 RESET_n

CA0_A H2 DDR1_CA_B_0 → DDR1_CA_B_0 7
CA1_A J2 DDR1_CA_B_1 → DDR1_CA_B_1 7
CA2_A H9 DDR1_CA_B_2 → DDR1_CA_B_2 7
CA3_A H10 DDR1_CA_B_3 → DDR1_CA_B_3 7
CA4_A H11 DDR1_CA_B_4 → DDR1_CA_B_4 7
CA5_A J11 DDR1_CA_B_5 → DDR1_CA_B_5 7
CA0_B R2 DDR1_CA_B_0
CA1_B P2 DDR1_CA_B_1
CA2_B R9 DDR1_CA_B_2
CA3_B R10 DDR1_CA_B_3
CA4_B R11 DDR1_CA_B_4
CA5_B P11 DDR1_CA_B_5

CK_t_A J8 DDR1_CK0_T_B → DDR1_CK0_T_B 7
CK_c_A J9 DDR1_CK0_C_B → DDR1_CK0_C_B 7
CK_t_B P8 DDR1_CK0_T_B
CK_c_B P9 DDR1_CK0_C_B

DMI0_A C3
DMI1_A C10
DMI0_B Y3
DMI1_B Y10

CS0_A H4 DDR1_CS0_B → DDR1_CS0_B 7
CS1_A H3 DDR1_CS1_B → DDR1_CS1_B 7
CS2_A K5
CS0_B R4 DDR1_CS0_B
CS1_B R3 DDR1_CS1_B
CS2_B N5

CKE0_A J4 DDR1_CKE0_B → DDR1_CKE0_B 7
CKE1_A J5 DDR1_CKE1_B → DDR1_CKE1_B 7
CKE2_A K8
CKE0_B P4 DDR1_CKE0_B
CKE1_B P5 DDR1_CKE1_B
CKE2_B N8

ZQ0 A5 R779 240-1-04 +VDDQ
ZQ1 A8 R780 240-1-04 +VDDQ
ZQ2 G11

ODT_CA_A G2 +VDDQ
ODT_CA_B T2 +VDDQ

DNU1 A1
DNU2 A2
DNU3 A11
DNU4 A12
DNU5 B1
DNU6 B12
DNU7 AA1
DNU8 AA12
DNU9 AB1
DNU10 AB2
DNU11 AB11
DNU12 AB12

+VDDQ +VDDQ +V1.8A

+VDDQ
| C576 0.1uF/16VX/04 | C577 4.7uF/6.3V/04 | C578 4.7uF/6.3V/04 | C579 10uF/10V-06 | C580 22uF/6.3V/06 | C581 22uF/6.3V/06 |

+V1.8A
| C582 0.1uF/16VX/04 | C583 4.7uF/6.3V/04 | C584 10uF/10V-06 | C585 22uF/6.3V/06 |

MIPI CSI CONNECTOR

CN4 — 31P AYF333135

CAM1_RST_N	R609 X/1K-04	+V1.8A GP_CAMERASB11 RESET# DOUBLE CHECK
	0-04 R281	GP_CAMERASB11
I2C_SCL4	0-04 R283	
	0-04 R282	I2C_SDA4
OSC_CLK_OUT_2	0-04 R285	
MCSI_RX_DATAN_0	MCSI_RX_DATAP_0	MCSI_RX_DATAP_0
MCSI_RX_DATAP_1	MCSI_RX_DATAN_1	MCSI_RX_DATAN_1
MCSI_RX_CLKN_0	MCSI_RX_CLKP_0	MCSI_RX_CLKP_0
MCSI_RX_DATAP_2	MCSI_RX_DATAN_2	MCSI_RX_DATAN_2
MCSI_RX_DATAN_3	MCSI_RX_DATAP_3	MCSI_RX_DATAP_3

+V1P8_CAM
C149 0.1uF/16VX/04
+V2P8_CAM
C152 0.1uF/16VX/04
C151 0.1uF/16VX/04
+V2P8_CAM
+V1P2_CAM
C153 0.1uF/16VX/04
+AVDD_CAM
C148 0.1uF/16VX/04
GND_CAM

+AVDD_CAM   +V2P8_CAM
FB27 FB-120-0.3A-04
FB28 FB-120-0.3A-04
GND_CAM

MIPI CSI CONNECTOR

CN5 — 21P FH35C-21S-0.3SHW(50)

+V1P2_CAM
C155 0.1uF/16VX/04

MCSI_DP_1	MCSI_DN_1	
MCSI_CLKN_0	MCSI_CLKP_0	
MCSI_DP_0	MCSI_DN_0	
I2C_SDA4 0-04 R293	0-04 R724	+V1P8_CAM
FLASH_RESET_N	0-04 R294	I2C_SCL4
	CAM2_RST_N	OSC_CLK_OUT_3

C156 0.1uF/16VX/04
GND_CAM
+V2P8_CAM
C158 0.1uF/16VX/04
GND_CAM

I2C_SCL4 I2C_SCL4
I2C_SDA4 I2C_SDA4

+V1.8A
R610 X/1K-04
GP_CAMERASB10
0-04 R611 FLASH_RESET_N

GP_CAMERASB10
RESET# DOUBLE CHECK

+V1.8A
R612 X/1K-04
GP_CAMERASB11
RESET# DOUBLE CHECK
CAM2_RST_N R296 0-04 GP_CAMERASB11
GP_CAMERASB11

+V2.8S for CAMERA

0.3A
+V2P8_CAM

+V3.3S   +V3.3A
Ven>1.6V
R600 4.7K-04
U67 APL5325BI-TRG
1 EN   NC/SS/FB 5
2 GND
3 VIN   VOUT 4
C503 10uF/6.3V/04
R598 249K
C539 10uF/6.3V/04
C540 0.1uF/16VX/04
R599 97.6K

+V1.8S for CAMERA

0.1A
+V1P8_CAM

+V2P8_CAM   +V3.3A
R715 10K-04
Ven>1.6V
U59 APL5325BI-TRG
1 EN   NC/SS/FB 5
2 GND
3 VIN   VOUT 4
C547 10uF/6.3V/04
R601 127K-1-04
C544 10uF/6.3V/04
C545 0.1uF/16VX/04
R602 100K-1-04

+V1.2S for CAMERA

0.2A
+V1P2_CAM

+V1P8_CAM
R718 10K-04
+V3.3A
U60 APL5325BI-TRG
1 EN   NC/SS/FB 5
2 GND
3 VIN   VOUT 4
C554 10uF/6.3V/04
R711 51K-1-04
C550 10uF/6.3V/04
C551 0.1uF/16VX/04
R712 100K-1-04

eDP CONNECTOR

CN6

41P FH35C-41S-0.3SHW(50)

REV:A0.2

+V1.8A	R297 10K-04
R629 0-04	
Q15 BSS138	R299 100K-04

EDP_HPD_CONN_N

EDP_HPD_CONN

REV:A0.2

8 EDP_TXP_0 — C159 0.1uF/6.3V/02 — EDP_TXP_C_0
8 EDP_TXN_0 — C160 0.1uF/6.3V/02 — EDP_TXN_C_0
8 EDP_TXP_1 — C161 0.1uF/6.3V/02 — EDP_TXP_C_1
8 EDP_TXN_1 — C162 0.1uF/6.3V/02 — EDP_TXN_C_1
8 EDP_TXP_2 — C163 0.1uF/6.3V/02 — EDP_TXP_C_2
8 EDP_TXN_2 — C164 0.1uF/6.3V/02 — EDP_TXN_C_2
8 EDP_TXP_3 — C165 0.1uF/6.3V/02 — EDP_TXP_C_3
8 EDP_TXN_3 — C166 0.1uF/6.3V/02 — EDP_TXN_C_3
8 EDP_AUXP — C167 0.1uF/6.3V/02 — EDP_C_AUXP
8 EDP_AUXN — C168 0.1uF/6.3V/02 — EDP_C_AUXN

EDP_HPD_CONN
DDI0_BKLT_CTRL
DDI0_VDD_EN
DDI0_BKLT_EN
I2C_3V3_SCL7
I2C_3V3_SDA7

+V3.3A FB7 FB-80-3A-06
C169 1uF/16V/04 16V 0402

PAD1
PAD2

REV:A0.2

+V3.3A R703 10K-04 — DDI0_BKLT_CTRL
R704 10K-04
Q42A EM6K1GT2R
Q42B EM6K1GT2R

8 DDI0_BKLTCTL — DDI0_BKLTCTL

+V3.3A R732 10K-04 — DDI0_BKLT_EN
R734 10K-04
Q48A EM6K1GT2R
Q48B EM6K1GT2R

8 DDI0_BKLTEN — DDI0_BKLTEN

REV:A0.2 R298 100K-04

+V3.3S R733 10K-04 — DDI0_VDD_EN
R735 10K-04
Q49A EM6K1GT2R
Q49B EM6K1GT2R

8 DDI0_VDDEN — DDI0_VDDEN

REV:A0.2 R771 100K-04

REV:A0.2

+V1.8A C170 0.1uF/16VX/04

+V3.3A R774 200K-1-04

REV:A0.2

+V3.3A R303 10K-04
R304 10K-04

REV:A0.2

U16
1 GND EN 8
2 VREF1 VREF2 7
3 SCL1 SCL2 6
4 SDA1 SDA2 5
PCA9306DCUR

12 I2C_SCL7
12 I2C_SDA7

I2C_3V3_SCL7
I2C_3V3_SDA7

C171 0.1uF/16VX/04

Title	eDP
Size	B
Document Number	UP-APL01
Rev:	A0.3
Date:	Wednesday, January 04, 2017
Sheet:	21 of 45

AAEON
an ASUS assoc. co.

M.2.2230/WiFi+BT/KeyID E
Intel AC8260 or AC3165

+V3.3A
FB8
FB-80-3A-06
+3.3VAUX_WIFI

+V3.3S
FB9
X/FB-80-3A-06

+3.3VAUX_WIFI

H1
(TF)BOSS.M3*5.0mm.Sn.EMISTOP.F55M30-500740P1D4M

C172 0.1uF/16VX/04
C173 0.1uF/16VX/04

CN7

M.2 KEY-E

+3.3VAUX_WIFI

R309
R310 10K-04 / X/10K-04 WAKE_M2_N / PCIE_M2_CLKREQ#

Pin	Signal		Signal	Pin
75	GND_75		+3.3V_74	74
73	RESERVED/REFCLKN1		+3.3V_72	72
71	RESERVED/REFCLKP1			70
69	GND_69		UIM_PWR_SRC/GPIO1/PEWAKE1#	68
67	RESERVED/PERN1		UIM_PWR_SNK/CLKREQ1#	66
65	RESERVED/PERP1		UIM_SWP/PERST1#	64
63	GND_63		RESVERED_64	62
61	RESERVED/PETN1		ALERT#	60
59	RESERVED/PETP1		I2C_CLK	58
57	GND_57		I2C_DATA	56
55	PEWAKE0#		W_DISABLE1#	54
53	CLKREQ0#		W_DISABLE2#	52
51	GND_51		PERST0#	50
49	REFCLKN0		SUSCLK(32kHz)	48
47	REFCLKP0		COEX1	46
45	GND_45		COEX2	44
43	PERN0		COEX3	42
41	PERP0		VENDOR DEFINED_42	40
39	GND_39		VENDOR DEFINED_40	38
37	PETN0		VENDOR DEFINED_38	36
35	PETP0		UART_RTS	34
33	GND_33		UART_CTS	32
			UART_TXD	

KEY-E

Pin	Signal		Signal	Pin
23	SDIO_RESET#		UART_RXD	22
21	SDIO_WAKE#		UART_WAKE#	20
19	SDIO_DATA3		GND_18	18
17	SDIO_DATA2		LED2#	16
15	SDIO_DATA1		PCM_OUT/I2S_SD_OUT	14
13	SDIO_DATA0		PCM_IN/ I2S_SD_IN	12
11	SDIO_CMD		PCM_SYNC/I2S_WS	10
9	SDIO_CLK		PCM_CLK/I2S_SCK	8
5	GND_7		LED1#	6
3	USB_D-		+3.3V_4	4
1	USB_D+		+3.3V_2	2
	GND_1			

PAD1 PAD2
H1 H2
75P AS0BC21-S67BE-LH
76 77 H1 H2

+3.3VAUX_WIFI

WAKE_M2_N_3V3   R314 0-04   WAKE_M2_N / PCIE_M2_CLKREQ#

9   WAKE_M2_N_3V3

9   CLK_PCIE_M2_N   CLK_PCIE_M2_N
9   CLK_PCIE_M2_P   CLK_PCIE_M2_P

9   PCIE_RXN3   PCIE_RXN3
9   PCIE_RXP3   PCIE_RXP3

9   PCIE_TXN3   PCIE_TXN3   C174 0.1uF/6.3V/02   PCIE_C_TXN3
9   PCIE_TXP3   PCIE_TXP3   C175 0.1uF/6.3V/02   PCIE_C_TXP3

R311 X/0-04   SMB_ALERT#   12
R312 X/0-04   SMB_CLK_3V3A   12,23
R313 X/0-04   SMB_DAT_3V3A   12,23

WIFI_EN
BT_EN
BUF_PLT_RST#   BUF_PLT_RST#   13,23,30,31,34
PMU_M2_SUSCLK   PMU_M2_SUSCLK   13

M2_UART0_RTS
M2_UART0_CTS
M2_UART0_TXD

+3.3VAUX_WIFI

M2_UART0_RXD

+3.3VAUX_WIFI

WIFI_EN R316 10K-04
BT_EN   R317 10K-04

9   USB2_DN4   USB2_DN4   CH2   BT_DM
9   USB2_DP4   USB2_DP4   3 2   BT_DP
                          4 1
90ohm.0.1A.3.5mohm.1.25*1.0mm

+3.3VAUX_WIFI

C176 0.1uF/16VX/04

REV:A0.2

+V1.8S   +V1.8S   +V3.3A

C559 0.1uF/16VX/04   C560 0.1uF/16VX/04

U69

1	VCCA	OE	VCCB	11
11 LPSS_UART0_TXD	LPSS_UART0_TXD 2	A1	B1 10	UART0_TXD_3V3
11 LPSS_UART0_RXD	LPSS_UART0_RXD 3	A2	B2 9	UART0_RXD_3V3
11 LPSS_UART0_RTS	LPSS_UART0_RTS 4	A3	B3 8	UART0_RTS_3V3
11 LPSS_UART0_CTS	LPSS_UART0_CTS 5	A4	B4 7	UART0_CTS_3V3
		GND 6		

NTS0104GU12

UART0_TXD_3V3   R730 0-02   UART0_TXD
                R759 X/0-02   M2_UART0_TXD   UART0_TXD   28

UART0_RXD_3V3   R731 0-02   UART0_RXD
                R760 X/0-02   M2_UART0_RXD   UART0_RXD   28

UART0_RTS_3V3   R761 X/0-02   M2_UART0_RTS

UART0_CTS_3V3   R762 X/0-02   M2_UART0_CTS

mini PCIE

mini_XSD	mSATA_PCIe_SEL	Function	Power +3.3V_MC
High	X(Don't care)	An, Bn, Cn are Hi-Z	N/A
Low	Low	PCIe (An=Bn)	+3.3V_ALW
Low	High	mSATA (An=Cn)	+3.3V

Size B	Document Number UP-APL01	Rev: A0.3
Date: Wednesday, January 04, 2017		Sheet: 23 of 45

AAEON®
an ASUS assoc. co.

SATA 3.0 PORT0

CN9
7P 007-01-00757

9	SATA_TXP0	C195 0.01uF/10V/02 SATA_C_TXP0
9	SATA_TXN0	C196 0.01uF/10V/02 SATA_C_TXN0
9	SATA_RXN0	C197 0.01uF/10V/02 SATA_C_RXN0
9	SATA_RXP0	C199 0.01uF/10V/02 SATA_C_RXP0

1 GND1
2 A+
3 A-
4 GND2
5 B-   H1
6 B+   H2
7 GND3

8
9

REV:A0.2

+V5S

C198
22uF/10V/08
10V
0805
±20%.X5R

CN10
1
2

2P 721-81-02TW00

USB 3.0 VCC

+V5P0_USB_OTG

C205
22uF/10V/08
10V
0805
±20%.X5R

C206
0.1uF/16VX/04
16V
0402

D6
0402ESDA-MLP
30V

+V5A

U18
1 VOUT   VIN 5
2 GND
3 FLAG   EN 4
RT9742CGJ5

C208
0.1uF/16VX/04

C207
1uF/16V/04

13,26,27,33,36,42   PM_SLP_S0#_3P3

R763   0-04

REV:A0.2

+V5P0_USB_OTG

CN13
USB2_C_DN0   1 VBUS   PAD1 11
USB2_C_DP0   2 D-   PAD2 12
USB_OTG_R_ID 3 D+   PAD3 13
              4 ID   PAD4 14
              5 GND
                         H1
                         H2
USB3_RXN_CON_P0 6 Micb_SSTX-
USB3_RXP_CON_P0 7 Micb_SSTX+
                 8 GND_DRAIN
USB3_TXN_CON_P0 9 Micb_SSRX-
USB3_TXP_CON_P0 10 Micb_SSRX+
10P 209E-BE01

REV:A0.2

CH4
9 USB2_DN0   USB2_DN0 3   2 USB2_C_DN0
9 USB2_DP0   USB2_DP0 4   1 USB2_C_DP0
90ohm(100MHz)

REV:A0.3

R816   0-04

CH5
9 USB3_RXP_P0   4   1 USB3_RXP_CON_P0
9 USB3_RXN_P0   3   2 USB3_RXN_CON_P0
90ohm.0.1A.3.5mohm.1.25*1.0mm

R817   0-04

U19
USB3_RXN_CON_P0 1 Line-1   NC1 10 USB3_RXN_CON_P0
USB3_RXP_CON_P0 2 Line-2   NC2 9   USB3_RXP_CON_P0
                 3
USB3_TXN_CON_P0 4 GND   GND1 8
USB3_TXP_CON_P0 5 Line-3   NC3 7   USB3_TXN_CON_P0
                   Line-4   NC4 6   USB3_TXP_CON_P0
AZ1045-04F

R818   0-04

CH6
9 USB3_TXP_P0 C209 0.1uF/6.3V/02 USB3_TXP_C_P0 4   1 USB3_TXP_CON_P0
9 USB3_TXN_P0 C210 0.1uF/6.3V/02 USB3_TXN_C_P0 3   2 USB3_TXN_CON_P0
90ohm.0.1A.3.5mohm.1.25*1.0mm

R819   0-04

U20
USB_OTG_R_ID 1 Line-1   NC1 10 USB_OTG_R_ID
              2 Line-2   NC2 9
              3
USB2_C_DP0   4 GND   GND1 8
USB2_C_DN0   5 Line-3   NC3 7   USB2_C_DP0
                Line-4   NC4 6   USB2_C_DN0
AZ1045-04F

REV:A0.2

+V1.8A

R336
10K-04

9 USB_OTG_R_ID   USB_OTG_R_ID

R337
X/0-04

REV:A0.2

R338 0-04

PM_SLP_S0#_3P3

REV:A0.2

PM_SLP_S0#_3P3   13,25,27,33,36,42

+V5P0_USB_0

C211
22uF/10V/08

C212
0.1uF/16VX/04

D8
0402ESDA-MLP
30V

REV:A0.2   REV:A0.2   REV:A0.2

+V5A

U21
5 VIN   VOUT 1
          GND 2
4 EN   FLAG 3
RT9742CGJ5

REV:A0.2

C213
1uF/16V/04

9 USB2_DN1
9 USB2_DP1

CH7
4   1 USB2_C_DN1
3   2 USB2_C_DP1
90ohm(100MHz)

9 USB2_DN2
9 USB2_DP2

CH8
4   1 USB2_C_DN2
3   2 USB2_C_DP2
90ohm(100MHz)

REV:A0.3

R820   X/0-04

CH9
90ohm.0.1A.3.5mohm.1.25*1.0mm
4   1 USB3_RXP_CON_P1
3   2 USB3_RXN_CON_P1

9 USB3_RXP_P1
9 USB3_RXN_P1

R821   X/0-04

R822   X/0-04

CH10
90ohm.0.1A.3.5mohm.1.25*1.0mm
C214 0.1uF/6.3V/02 USB3_TXP_C_P1 4 1 USB3_TXP_CON_P1
C215 0.1uF/6.3V/02 USB3_TXN_C_P1 3 2 USB3_TXN_CON_P1

9 USB3_TXP_P1
9 USB3_TXN_P1

R823   X/0-04

R824   X/0-04

CH11
90ohm.0.1A.3.5mohm.1.25*1.0mm
4   1 USB3_RXP_CON_P2
3   2 USB3_RXN_CON_P2

9 USB3_RXP_P2
9 USB3_RXN_P2

R825   X/0-04

R826   X/0-04

CH12
90ohm.0.1A.3.5mohm.1.25*1.0mm
C216 0.1uF/6.3V/02 USB3_TXP_C_P2 4 1 USB3_TXP_CON_P2
C217 0.1uF/6.3V/02 USB3_TXN_C_P2 3 2 USB3_TXN_CON_P2

9 USB3_TXP_P2
9 USB3_TXN_P2

R827   X/0-04

+V5P0_USB_0   +V5P0_USB_0

CN14
18P UDNFA199N-AY-00-A

USB2_C_DN1   2 VBUS1   VBUS2 10
USB2_C_DP1   3 D1-   D2- 11   USB2_C_DN2
              4 D1+   D2+ 12   USB2_C_DP2
                 GND1   GND2 13

USB3_RXN_CON_P1 5 SSRX1-   SSRX2- 14 USB3_RXN_CON_P2
USB3_RXP_CON_P1 6 SSRX1+   SSRX2+ 15 USB3_RXP_CON_P2
                 7 GND_DRAIN1 GND_DRAIN2 16
USB3_TXN_CON_P1 8 SSTX1-   SSTX2- 17 USB3_TXN_CON_P2
USB3_TXP_CON_P1 9 SSTX1+   SSTX2+ 18 USB3_TXP_CON_P2

H1 H2 H3 H4

U22
USB3_RXN_CON_P2 1 Line-1   NC1 10
USB3_RXP_CON_P2 2 Line-2   NC2   9
                 3 GND   GND1   8
USB3_RXN_CON_P1 4 Line-3   NC3   7
USB3_RXP_CON_P1 5 Line-4   NC4   6
AZ1045-04F

U23
USB2_C_DP2 1 Line-1   NC1 10
USB2_C_DN2 2 Line-2   NC2   9
            3 GND   GND1   8
USB2_C_DP1 4 Line-3   NC3   7
USB2_C_DN1 5 Line-4   NC4   6
AZ1045-04F

U24
USB3_TXN_CON_P2 1 Line-1   NC1 10
USB3_TXP_CON_P2 2 Line-2   NC2   9
                 3 GND   GND1   8
USB3_TXN_CON_P1 4 Line-3   NC3   7
USB3_TXP_CON_P1 5 Line-4   NC4   6
AZ1045-04F

Title
USB3.0_TYPE-A (1/2)

Size B
Document Number UP-APL01
Rev: A0.3

Date: Wednesday, January 04, 2017

Sheet: 26 of 45

REV:A0.2

R343   0-04   PM_SLP_S0#_3P3   PM_SLP_S0#_3P3   13,25,26,33,36,42

REV:A0.2

+V5P0_USB_1

+V5A

U25
5   VIN   VOUT   1
          GND   2
4   EN   FLAG   3
RT9742CGJ5

REV:A0.2   REV:A0.2   REV:A0.2

C218
22uF/10V/08
C219
0.1uF/16VX/04

D9
0402ESDA-MLP
30V

C220
1uF/16V/04

REV:A0.3

CN15
+V5P0_USB_1

H2
SHIELD_2

USB2_C_DN3   U1   VBUS
USB2_C_DP3   U2   D-
             U3   D+
             U4   GND

USB3_RXN_CON_P3   U5   SSRX-
USB3_RXP_CON_P3   U6   SSRX+
                  U7   GND_DRAIN
USB3_TXN_CON_P3   U8   SSTX-
USB3_TXP_CON_P3   U9   SSTX+

SHIELD_1
H1
1654-USB-9P-5405X0101101

9   USB2_DN3   CH13
9   USB2_DP3
                4   1   USB2_C_DN3
                3   2   USB2_C_DP3
              90ohm(100MHz)

REV:A0.3

R828   X/0-04
CH15
90ohm,0.1A,3.5mohm,1.25*1.0mm
9   USB3_RXP_P3   4   1   USB3_RXP_CON_P3
9   USB3_RXN_P3   3   2   USB3_RXN_CON_P3

R829   X/0-04

R830   X/0-04
CH16
90ohm,0.1A,3.5mohm,1.25*1.0mm
          C221   0.1uF/6.3V/02   USB3_TXP_C_P3   4   1   USB3_TXP_CON_P3
9   USB3_TXP_P3
9   USB3_TXN_P3   C222   0.1uF/6.3V/02   USB3_TXN_C_P3   3   2   USB3_TXN_CON_P3

R831   X/0-04

U26
USB3_RXP_CON_P3   1   Line-1   NC1   10
USB3_RXN_CON_P3   2   Line-2   NC2   9
                  3   8
                  4   GND   GND1   7
                  5   Line-3   NC3   6
                      Line-4   NC4
AZ1045-04F

U27
USB2_C_DP3   1   Line-1   NC1   10
USB2_C_DN3   2   Line-2   NC2   9
             3   8
USB3_TXN_CON_P3   4   GND   GND1   7
USB3_TXP_CON_P3   5   Line-3   NC3   6
                      Line-4   NC4
AZ1045-04F

Title
USB3.0_TYPE-A (2/2)

Size   Document Number   Rev:
B   UP-APL01   A0.3

Date: Wednesday, January 04, 2017   Sheet: 27 of 45

AAEON®
an ASUS assoc. co.

+V5S

+V5A_USB_PANEL

F1
8V;2A
LP-ISML200

C225
0.1uF/16VX/04
16V
0402

C226
22uF/10V/08

C227
0.1uF/16VX/04

REV:A0.2

U29
USB2_DN6	1	Line-1	NC1	10	USB2_DN6
USB2_DP6	2	Line-2	NC2	9	USB2_DP6
	3	GND	GND1	8	
USB2_DN7	4	Line-3	NC3	7	USB2_DN7
USB2_DP7	5	Line-4	NC4	6	USB2_DP7

AZ1045-04F

9 USB2_DP6
9 USB2_DN6

USB2_DP6
USB2_DN6

9 USB2_DP7
9 USB2_DN7

USB2_DP7
USB2_DN7

+V5A_USB_PANEL

CN16

USB2_DN6
USB2_DP6

USB2_DN7
USB2_DP7

22 UART0_RXD
22 UART0_TXD

UART0_RXD
UART0_TXD

1		2
3		4
5		6
7		8
9		11
10		12

10P 710-74-10TWR6

+V5A_USB_PANEL

1

D10
0402ESDA-MLP
30V

2

+V5A

FAN_PWR

APM2301CAC-TRG   Q18

2 (S)
1 (G)
3 (D)

R374
100K-04

C

R376
100K-04

12 PWM2   PWM2

R377
4.7K-04

B

Q19
MMBT3904LT1G

E

FAN_PWR

CN17
2P 712-73-02TWE0

3 1
4 2

C260
0.1uF/16VX/04

C261
1uF/16V/04

Title
FAN

Size
A

Document Number
UP-APL01

Rev:
A0.3

Date: *Wednesday, January 04, 2017*

Sheet: **29** of **45**

U33

LAN1_VDD33 R378 X/10K-04
9 CLK_PCIE_LAN1_P   CLK_PCIE_LAN1_P   15   REFCLK_P
9 CLK_PCIE_LAN1_N   CLK_PCIE_LAN1_N   16   REFCLK_N
                                        12   CLKREQB

9 PCIE_TXP1   C264   0.1uF/6.3V/02   PCIE_C_TXP1   13   HSIP
9 PCIE_TXN1   C265   0.1uF/6.3V/02   PCIE_C_TXN1   14   HSIN

9 PCIE_RXP1   C262   0.1uF/6.3V/02   PCIE_C_RXP1   17   HSOP
9 PCIE_RXN1   C263   0.1uF/6.3V/02   PCIE_C_RXN1   18   HSON

LAN1_VDD33
R381   10K-04
9 WAKE_LAN1_N_3V3   R382   0-04   WAKE_LAN1_N   21   LANWAKEB

BUF_PLT_RST#   19   PERSTB
13,22,23,31,34 BUF_PLT_RST#

LAN1_ISOLATE#   20   ISOLATEB

R385   2.49K   31   RSET
0402   1%

+L1_VDDREG
C269   C270
4.7uF/6.3V/04 0.1uF/16VX/04
6.3V
0402

LAN1_VDD33
R387   0-06   23   VDDREG
0603   5%
                11   AVDD33_1
                32   AVDD33_2
C271   C272
10uF/6.3V/04   0.22uF/10V/04

REGOUT   24
LAN1_VDD10
C275   C276
4.7uF/6.3V/04 0.1uF/16VX/04
6.3V
0402

AVDD10_1   3
AVDD10_2   8
AVDD10_3   30
DVDD10   22
LAN1_VDD10
C279   C280   C281   C284
0.1uF/16VX/04 0.22uF/10V/04 0.22uF/10V/04 1uF/16V/04

GND1   33

RTL8111G-CG

10 MDIN3   LAN1_MDI3-
9   MDIP3   LAN1_MDI3+
7   MDIN2   LAN1_MDI2-
8   MDIP2   LAN1_MDI2+
5   MDIN1   LAN1_MDI1-
4   MDIP1   LAN1_MDI1+
2   MDIN0   LAN1_MDI0-
1   MDIP0   LAN1_MDI0+

28 CKXTAL1   LAN1_XTL25P
29 CKXTAL2   LAN1_XTL25N
R380   1M-1-04
Y8
25MHz 4P
C267   C268
33pF/50V/04   33pF/50V/04
50V   50V
0402   0402

27 LED0   LAN1_LED0   R383   150-1-04   LAN1_LINK100#
26 LED1/GPO LAN1_LED1   R384   150-1-04   LAN1_LINK1000#
25 LED2   LAN1_ACTLEDN
LAN1_VDD33   R386   330   LAN1_ACTLEDP
             0402   5%

CN18A
LAN1_ACTLEDP   L2A   LED1(Y+)A
LAN1_ACTLEDN   L1A   LED1(Y-)A
LAN1_MDI0+   R1A   D1+A
LAN1_MDI0-   R2A   D1-A
LAN1_MDI1+   R3A   D2+A
LAN1_MDI1-   R4A   D2-A
LAN1_MDI2+   R5A   D3+A
LAN1_MDI2-   R6A   D3-A
LAN1_MDI3+   R7A   D4+A
LAN1_MDI3-   R8A   D4-A
               R9A   VCCA
               R10A GND1A

REV:A0.2
LAN1_LINK100#   L4A   LED2(G+,O-)A
LAN1_LINK1000#   L3A   LED2(G-,O+)A
28P RM3-169A9V1Q 90D(F)
C266   0.1uF/25V/04

G1 G2 G3
CGND1 CGND2 CGND3
H1

+V3.3A
FB15   FB-80-3A-06
3.5A   0603
C277   4.7uF/6.3V/04
LAN1_VDD33
C278   0.1uF/16VX/04
6.3V   0402

REV:A0.2
+V3.3S   LAN1_VDD33
R388   R389
1K-1-04   X/1K-1-04
1%   1%
0402   0402
LAN1_ISOLATE#
R390   15K-1-04

Title: RTL8111G-CG_LAN1
Size: B
Document Number: UP-APL01
Rev: A0.3
Date: Wednesday, January 04, 2017
Sheet: 30 of 45

U34
RTL8111G-CG

CLKREQB 12
REFCLK_P 15
REFCLK_N 16
HSIP 13
HSIN 14
HSOP 17
HSON 18
LANWAKEB 21
PERSTB 19
ISOLATEB 20
RSET 31
VDDREG 23
AVDD33_1 11
AVDD33_2 32
REGOUT 24
AVDD10_1 3
AVDD10_2 8
AVDD10_3 30
DVDD10 22
GND1 33

MDIN3 10
MDIP3 9
MDIN2 7
MDIP2 6
MDIN1 5
MDIP1 4
MDIN0 2
MDIP0 1
CKXTAL1 28
CKXTAL2 29
LED0 27
LED1/GPO 26
LED2 25

LAN2_MDI3- 10
LAN2_MDI3+ 9
LAN2_MDI2- 7
LAN2_MDI2+ 6
LAN2_MDI1- 5
LAN2_MDI1+ 4
LAN2_MDI0- 2
LAN2_MDI0+ 1

LAN2_XTL25P 28
LAN2_XTL25N 29

LAN2_LED0 27
LAN2_LED1 26

LAN2_VDD33 R392 X/10K-04
9 CLK_PCIE_LAN2_P CLK_PCIE_LAN2_P
9 CLK_PCIE_LAN2_N CLK_PCIE_LAN2_N

9 PCIE_TXP2 PCIE_TXP2 C285 0.1uF/6.3V/02 PCIE_C_TXP2
9 PCIE_TXN2 PCIE_TXN2 C286 0.1uF/6.3V/02 PCIE_C_TXN2

9 PCIE_RXP2 PCIE_RXP2 C287 0.1uF/6.3V/02 PCIE_C_RXP2
9 PCIE_RXN2 PCIE_RXN2 C288 0.1uF/6.3V/02 PCIE_C_RXN2

LAN2_VDD33
R394 10K-04
9 WAKE_LAN2_N_3V3 R395 0-04 WAKE_LAN2_N

13,22,23,30,34 BUF_PLT_RST# BUF_PLT_RST#

LAN2_ISOLATE#

R398 2.49K 0402 1%

R393 1M-1-04
Y9
25MHz 4P
C290 33pF/50V/04 50V 0402
C291 33pF/50V/04 50V 0402

LAN2_ACTLEDP L2B
LAN2_ACTLEDN L1B
LAN2_MDI0+ R1B
LAN2_MDI0- R2B
LAN2_MDI1+ R3B
LAN2_MDI1- R4B
LAN2_MDI2+ R5B
LAN2_MDI2- R6B
LAN2_MDI3+ R7B
LAN2_MDI3- R8B
R9B
R10B
LAN2_LINK100# L4B
LAN2_LINK1000# L3B

CN18B
LED1(Y+)B
LED1(Y-)B
D1+B
D1-B
D2+B
D2-B
D3+B
D3-B
D4+B
D4-B
VCCB
GNDB
LED2(G+,O-)B
LED2(G-,O+)B
28P RM3-169A9V1Q 90D(F)

REV:A0.2

C289 0.1uF/25V/04

G4 CGND4
G5 CGND5
G6 CGND6
H2

R396 150-1-04 LAN2_LINK100#
R397 150-1-04 LAN2_LINK1000#
LAN2_ACTLEDN
LAN2_VDD33 R399 330 0402 5% LAN2_ACTLEDP

+L2_VDDREG
C292 4.7uF/6.3V/04 6.3V 0402
C293 4.7uF/16VX/04

LAN2_VDD33
R400 0-06 0603 5%
C294 10uF/6.3V/04
C295 0.22uF/10V/04

LAN2_VDD10
C298 4.7uF/6.3V/04 6.3V 0402
C299 4.7uF/16VX/04

LAN2_VDD10
C302 0.1uF/16VX/04
C303 0.22uF/10V/04
C304 0.22uF/10V/04
C307 1uF/16V/04
Close to Pin22

20160711 Changed
+V3.3A
FB16 FB-80-3A-06
3.5A 0603
LAN2_VDD33
C300 4.7uF/6.3V/04 6.3V 0402
C301 0.1uF/16VX/04

REV:A0.2
+V3.3S LAN2_VDD33
R401 1K-1-04 1% 0402
R402 X/1K-1-04 1% 0402
LAN2_ISOLATE#
R403 15K-1-04

HDMI CHOKE SECTION

REV:A0.3

REV:A0.3

REV:A0.3

REV:A0.3

REV:A0.2

REV:A0.2

Title	HDMI_port0	
Size C	Document Number UP-APL01	Rev. A0.3
Date: Wednesday, January 04, 2017		Sheet 32 of 45

HDMI CHOKE SECTION

DDI1_TXN_0
DDI1_TXP_0

8 DDI1_TXN_0
8 DDI1_TXP_0

C319 0.1uF/6.3V/02
C320 0.1uF/6.3V/02

DDI1_TXN_C_0
DDI1_TXP_C_0

CH27
3 2
4 1
90ohm(100MHz)

DDI1_TXN_HDMI_0
DDI1_TXP_HDMI_0

DDI1_TXN_HDMI_0 32
DDI1_TXP_HDMI_0 32

8 DDI1_TXN_1
8 DDI1_TXP_1

C321 0.1uF/6.3V/02
C322 0.1uF/6.3V/02

DDI1_TXN_C_1
DDI1_TXP_C_1

CH28
4 1
3 2
90ohm(100MHz)

DDI1_TXN_HDMI_1
DDI1_TXP_HDMI_1

DDI1_TXN_HDMI_1 32
DDI1_TXP_HDMI_1 32

8 DDI1_TXN_2
8 DDI1_TXP_2

C323 0.1uF/6.3V/02
C324 0.1uF/6.3V/02

DDI1_TXN_C_2
DDI1_TXP_C_2

CH29
3 2
4 1
90ohm(100MHz)

DDI1_TXN_HDMI_2
DDI1_TXP_HDMI_2

DDI1_TXN_HDMI_2 32
DDI1_TXP_HDMI_2 32

8 DDI1_TXN_3
8 DDI1_TXP_3

C325 0.1uF/6.3V/02
C326 0.1uF/6.3V/02

DDI1_TXN_C_3
DDI1_TXP_C_3

CH30
4 1
3 2
90ohm(100MHz)

DDI1_CLK_HDMI_DN
DDI1_CLK_HDMI_DP

DDI1_CLK_HDMI_DN 32
DDI1_CLK_HDMI_DP 32

DDI1_TXN_C_0
DDI1_TXP_C_0
R674 470-1-04 0402
R675 470-1-04 0402

DDI1_TXN_C_1
DDI1_TXP_C_1
R676 470-1-04 0402
R678 470-1-04 0402

13,25,26,27,36,42 PM_SLP_S0#_3P3

PM_SLP_S0#_3P3

R677 0-04

Q37 BSS138
G
D
S

DDI1_TXN_C_2
DDI1_TXP_C_2
R679 470-1-04 0402
R680 470-1-04 0402

DDI1_TXN_C_3
DDI1_TXP_C_3
R681 470-1-04 0402
R682 470-1-04 0402

REV:A0.3

+V3.3S

BAT54HT1G
D21
1
2

R686 27K-1-04

HDMI1_CEC_D

HDMI1_CEC_D 32

REV:A0.3

12,38 CPU_prog_JTAG_TDO   CPU_prog_JTAG_TDO   R689 0-04

12,38 CPU_prog_JTAG_TMS   CPU_prog_JTAG_TMS   R692 0-04

Q38A EM6K1GT2R
6
2
1

R694 10K-04   +V1.8A

Q38B EM6K1GT2R
3
5
4

REV:A0.3

Q52 BSS138
D
G
S

disableCEC 12

REV:A0.3

+V1.8A

C327 0.1uF/16VX/04

+5V_HDMI_1

R776 200K-1-04   REV:A0.2

+5V_HDMI_1

R412 2.2K-04

+5V_HDMI_1

R413 2.2K-04

U40
1 GND   EN 8
2   7
3 VREF1 VREF2 6
SCL1   SCL2
4 SDA1   SDA2 5
PCA9306DCUR

8 DDI1_DDCCLK
8 DDI1_DDCDATA

C328 0.1uF/16VX/04

DDI1_5V_DDCCLK 32
DDI1_5V_DDCDATA 32

AAEON®
an ASUS assoc. co.

Title
HDMI_port1

Size B

Document Number
UP-APL01

Rev:
A0.3

Date: Wednesday, January 04, 2017

Sheet: 33 of 45

EMMC

U41

Signal	Pin		Pin	Signal
EMMC_CLK (11)	M6	CLK	E6 F5 J10 K9	VCC_E6 VCC_F5 VCC_J10 VCC_K9
EMMC_CMD (11)	M5	CMD	C6 M4 N4 P3 P5	VCCQ_C6 VCCQ_M4 VCCQ_N4 VCCQ_P3 VCCQ_P5
EMMC_D0 (11)	A3	DAT0		
EMMC_D1 (11)	A4	DAT1		
EMMC_D2 (11)	A5	DAT2	E7 G5 H10 K8	VSS_E7 VSS_G5 VSS_H10 VSS_K8
EMMC_D3 (11)	B2	DAT3		
EMMC_D4 (11)	B3	DAT4	C4 N2 N5 P4 P6	VSSQ_C4 VSSQ_N2 VSSQ_N5 VSSQ_P4 VSSQ_P6
EMMC_D5 (11)	B4	DAT5		
EMMC_D6 (11)	B5	DAT6	J5 A6	VSS_J5 VSS_A6
EMMC_D7 (11)	B6	DAT7		

+V3P3A_EMMC

+V1P8A_EMMC

EMMC_RST_N (12) — R721 X/0-02 — EMMC_RST_R_N — K5 RST_N

EMMC_VDDI — C2 VDDI

C329 2.2uF/10V/04 <Rating> 0402

H5 DS

R428 X/10-04 — EMMC_DATA_STORBE

EMMC_RCLK (11)

REV:A0.2

R772 X/100K-04

REV:A0.2

+V1P8A_EMMC

R773 10K-04 5% 0402

EMMC_CMD

+V1P8A_EMMC

R429 10K-04 5% 0402

EMMC_RST_R_N

+V3.3A

R430 10K-04

Q20A EM6K1GT2R

R630 0-02

Q20B EM6K1GT2R

BUF_PLT_RST# (13,22,23,30,31)

14-E_F_P-EMMC32GM525A51-0

+V3.3A

FB29 FB-120-0.3A-04

50mA

+V3P3A_EMMC

C330 10uF/6.3V/04 6.3V 0402

C331 0.1uF/16VX/04

C332 0.1uF/16VX/04

+V1.8A

FB30 FB-120-0.3A-04

200mA

+V1P8A_EMMC

C333 10uF/6.3V/04 6.3V 0402

C334 0.1uF/16VX/04

C335 0.1uF/16VX/04

SPI NOR FLASH SOCKET

+VCC_SPI

11,38 SPI_CLK — SPI_CLK — R751 — 22-02 — SPI_BIOS_CLK
11,38 SPI_MOSI — SPI_MOSI — R752 — 22-02 — SPI_BIOS_MOSI
11,38 SPI_MISO — SPI_MISO — R753 — 22-02 — SPI_BIOS_MISO
11,38 SPI_CS0# — SPI_CS0# — R754 — 22-02 — SPI_BIOS_CS0#

C338
X/0.01uF/25V/04

R436 3.3K 5% 0402
R437 3.3K 5% 0402

SPI_SOCK_HOLD_N
SPI_CS0#

SPI_SOCK_HOLD_N 38

PROGRAMMER SECTION

+V5A

+VCC_SPI

R742 10K-04

Q50 2N7002WT1G
G D S

+V1.8A

+V5A

R720 10K-04

Q46B EM6K1GT2R

13,42 PCH_PWROK

+VCC_SPI

R719 10K-04

SPI_SOCK_WP_N

Q46A EM6K1GT2R

REV:A0.3

+VCC_SPI

C339
0.1uF/16VX/04
16V
0402

U43
SPI_BIOS_CS0#	1	CS#	VCC	8	+VCC_SPI side
SPI_BIOS_MISO	2	DO(IO1)	HOLD#(IO3)	7	SPI_SOCK_HOLD_N
SPI_SOCK_WP_N	3	WP#(IO2)	CLK	6	SPI_BIOS_CLK
	4	GND	DI(IO0)	5	SPI_BIOS_MOSI

W25Q128FWSIQ

analog

+V3.3A
C341 10uF/10V C340 0.1uF/16VX/04
<Rating> 16V
0603 0402
D14
SFI0402-050E560NP-LE

CN20
20*2P

+V5A
REV:A0.3
C342 10uF/10V C343 0.1uF/16VX/04
<Rating> 16V
0603 0402
D15 0402ESDA-MLP 30V

HAT_I2C1_SDA 1
HAT_I2C1_SCL 3 4
HAT_ANALOG_IN1 5 6
38 HAT_ANALOG_IN1 7 8 HAT_UART1_TXD HAT_UART1_TXD 38
38 HAT_ANALOG_IN2 9 HAT_ANALOG_IN2 10 HAT_UART1_RXD HAT_UART1_RXD 38
38 HAT_ANALOG_IN3 11 HAT_ANALOG_IN3 12 HAT_I2S6_BCLK HAT_I2S6_BCLK 38
38 HAT_ANALOG_IN4 13 HAT_ANALOG_IN4 14
15 16 HAT_SPI_1_FS1 HAT_SPI_1_FS1 38
HAT_SPI_0_TXD 17 18 HAT_SPI_1_RXD HAT_SPI_1_RXD 38
38 HAT_SPI_0_TXD 19 HAT_SPI_0_RXD 20
38 HAT_SPI_0_RXD 21 22 HAT_SPI_1_TXD HAT_SPI_1_TXD 38
38 HAT_SPI_0_CLK 23 HAT_SPI_0_CLK 24 HAT_SPI_0_FS0 HAT_SPI_0_FS0 38
25 HAT_I2C0_SDA 26 HAT_SPI_0_FS1 HAT_SPI_0_FS1 38
27 HAT_I2C0_SCL 28
38 HAT_GPIO4 29 HAT_GPIO4 30 HAT_PWM0
38 HAT_SPI_1_CLK 31 HAT_SPI_1_CLK 32 HAT_PWM0 38
38 HAT_PWM1 33 HAT_PWM1 34 HAT_UART1_CTS
38 HAT_I2S6_WS_SYNC 35 HAT_I2S6_WS_SYNC 36 HAT_UART1_CTS 38
38 HAT_SPI_1_FS0 37 HAT_SPI_1_FS0 38 HAT_I2S6_SDI HAT_I2S6_SDI 38
39 40 HAT_I2S6_SDO HAT_I2S6_SDO 38

+V3.3A
38 HAT_I2C0_SCL HAT_I2C0_SCL R440 2.2K-02
38 HAT_I2C0_SDA HAT_I2C0_SDA R441 2.2K-02
38 HAT_I2C1_SCL HAT_I2C1_SCL R442 2.2K-02
38 HAT_I2C1_SDA HAT_I2C1_SDA R443 2.2K-02

REV:A0.2
+V1.8S
+V1.8A +V1.8S +V3.3A
R454 X/10K-04
R456 X/10K-04
R457 X/10K-04
R458 X/10K-04
C346 0.1uF/16VX/04 C347 0.1uF/16VX/04

11,37 SIO_SPI_1_TXD
11,37 SIO_SPI_1_RXD
11,37 SIO_SPI_1_FS1
11,37 SIO_SPI_1_CLK
REV:A0.3

U46
1 VCCA OE VCCB 11
2 A1 B1 10
3 A2 B2 9
4 A3 B3 8
5 A4 B4 7
GND
6
NTS0104GU12

SIO_SPI_1_3V3_TXD
SIO_SPI_1_3V3_RXD
SIO_SPI_1_3V3_FS1
SIO_SPI_1_3V3_CLK
REV:A0.3

REV:A0.3
U45
SIO_SPI_1_3V3_TXD 8 DIN DOUT 9 SIO_SPI_1_3V3_RXD

analog
HAT_ANALOG_IN1 R451 0-04 HAT_ANALOG_R_IN1 7 IN1
HAT_ANALOG_IN2 R452 0-04 HAT_ANALOG_R_IN2 6 IN2
HAT_ANALOG_IN3 R453 0-04 HAT_ANALOG_R_IN3 5 IN3
HAT_ANALOG_IN4 R455 0-04 HAT_ANALOG_R_IN4 4 IN4

+V3.3A
FB20 FB-80-3A-06
C351 0.1uF/16VX/04
SIO_SPI_1_3V3_CLK 10 SCLK VA 2
SIO_SPI_1_3V3_FS1 1 CS# GND 3
C352 1uF/16V/04
REV:A0.3
ADC124S101CIMMX/NOPB

REV:A0.2
+V1.8S
13,25,26,27,33,42 PM_SLP_S0#_3P3
R768 0-04
Ven>1.6V
R769 127K-1-04 C564 1uF/16V/04
+V3.3A
U70
1 EN NC/SS/FB 5
2 GND
3 VIN VOUT 4
APL5325BI-TRG
C565 1uF/16V/04
R770 100K-1-04

HAT_ANALOG_R_IN1 C348 X/0.01uF/25VX-04
HAT_ANALOG_R_IN2 C349 X/0.01uF/25VX-04
HAT_ANALOG_R_IN3 C350 X/0.01uF/25VX-04
HAT_ANALOG_R_IN4 C353 X/0.01uF/25VX-04

Title: HAT
Size: B
Document Number: UP-APL01
Rev: A0.3
Date: Wednesday, January 04, 2017
Sheet: 36 of 45

CN21

60P AXK6S60547YG

Left	Pin	Pin	Right
38 GPIO/EXHAT_LVDS0n	1	2	GPIO/EXHAT_LVDS1n 38
38 GPIO/EXHAT_LVDS0p	3	4	GPIO/EXHAT_LVDS1p 38
	5	6	
38 GPIO/EXHAT_LVDS2n	7	8	GPIO/EXHAT_LVDS3n 38
38 GPIO/EXHAT_LVDS2p	9	10	GPIO/EXHAT_LVDS3p 38
	11	12	
38 GPIO/EXHAT_LVDS4n	13	14	GPIO/EXHAT_LVDS5n 38
38 GPIO/EXHAT_LVDS4p	15	16	GPIO/EXHAT_LVDS5p 38
	17	18	
38 GPIO/EXHAT_LVDS6n	19	20	GPIO/EXHAT_LVDS7n 38
38 GPIO/EXHAT_LVDS6p	21	22	GPIO/EXHAT_LVDS7p 38
	23	24	
38 GPIO/EXHAT_PLL1_INn	25	26	GPIO/EXHAT_PLL1_OUTn 38
38 GPIO/EXHAT_PLL1_INp	27	28	GPIO/EXHAT_PLL1_OUTp 38
	29	30	
11 SDCARD_CD_N	31	32	SDCARD_CLK 11
11 SDCARD_LVL_WP	33	34	
	35	36	
11,36 SIO_SPI_1_TXD	37	38	SDCARD_D0 11
11,36 SIO_SPI_1_RXD	39	40	SDCARD_D1 11
11 SIO_SPI_1_FS0	41	42	SDCARD_D2 11
11,36 SIO_SPI_1_FS1	43	44	SDCARD_D3 11
11,36 SIO_SPI_1_CLK	45	46	SDCARD_CMD
	47	48	SDCARD_CMD 11
12 I2C_SCL3	49	50	AVS_DMIC_CLK_A1 12
12 I2C_SDA3	51	52	AVS_DMIC_CLK_B1 12
	53	54	AVS_DMIC_CLK_AB2 12
12 I2C_SCL2	55	56	
12 I2C_SDA2	57	58	AVS_DMIC_DATA_1 12
	59	60	AVS_DMIC_DATA_2 12

REV:A0.3

REV:A0.3

CPLD

1.8V Level

U52B — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 2 of 11
DATE : JUN_2015
10M04SCU169C8G

ISH_GPIO_0, ISH_GPIO_1, ISH_GPIO_3, ISH_GPIO_5, ISH_GPIO_7, ISH_GPIO_6, ISH_GPIO_4
IO_1A_D1/DIFFIO_RX_L1N, IO_1A_C1/DIFFIO_RX_L2N, IO_1A_C2/DIFFIO_RX_L2P, IO_1A_B1/DIFFIO_RX_L1P, IO_1A_B2/DIFFIO_RX_L3P, IO_1A_E4/DIFFIO_RX_L4N, IO_1A_E1/DIFFIO_RX_L4P

AVS_I2S2_MCLK, ISH_GPIO_8, ISH_GPIO_9, ISH_GPIO_10
IO_1B_F4/DIFFIO_RX_L10N, IO_1B_G4/DIFFIO_RX_L10P, IO_1B_H2/DIFFIO_RX_L12N, IO_1B_H3/DIFFIO_RX_L12P

REV:A0.3 1.8V Level
SIO_SPI_2_CLK, SIO_SPI_2_RXD, AVS_I2S2_WS_SYNC, PWM0, SIO_SPI_2_SDO, SIO_SPI_0_CLK, SIO_SPI_0_TXD, SIO_SPI_2_SDI, AVS_I2S2_SDI, AVS_I2S2_BCLK, SIO_SPI_2_TXD, PWM1, PWM3, SIO_SPI_0_FS0

U52F — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 6 of 11
DATE : JUN_2015
10M04SCU169C8G

IO_6_F12/DIFFIO_RX_R14P, IO_6_F11/DIFFIO_RX_R14N, IO_6_C13, IO_6_F8/DIFFIO_RX_R17P, IO_6_B12/DIFFIO_RX_R18P, IO_6_E9/DIFFIO_RX_R17N, IO_6_C12/DIFFIO_RX_R18N, IO_6_C12/DIFFIO_RX_R19P, IO_6_B13/DIFFIO_RX_R20P, IO_6_C11/DIFFIO_RX_R19N, IO_6_A12/DIFFIO_RX_R20N, IO_6_A12/DIFFIO_RX_R21P, IO_6_A13/DIFFIO_RX_R21N, IO_6_D12/DIFFIO_RX_R23P, IO_6_D11/DIFFIO_RX_R23N

I2C_SCL6, I2C_SDA0, I2C_SDA6, I2C_SCL1, I2C_SCL5, I2C_SDA1, I2C_SDA5, BT_HOST_WAKE, I2C_SCL0, LPSS_UART1_CTS, SDIO_D3, LPSS_UART1_RTS, SDIO_PWR#, SDIO_D0, SDIO_D1, LPSS_UART1_TXD, ISH_GPIO_15, SDIO_CLK

U52G — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 7 of 11
DATE : JUN_2015
10M04SCU169C8G

1.8V Level

IO_8_C10/DIFFIO_RX_T1P, IO_8_A8/DIFFIO_RX_T2P, IO_8_C9/DIFFIO_RX_T1N, IO_8_A9/DIFFIO_RX_T2N, IO_8_B10/DIFFIO_RX_T3P, IO_8_A10/DIFFIO_RX_T4P, IO_8_A11/DIFFIO_RX_T4N, IO_8_E8/DIFFIO_RX_T5N, IO_8_A7/DIFFIO_RX_T6P, IO_8_A6/DIFFIO_RX_T6N, IO_8_B6/DIFFIO_RX_T7P, IO_8_B5/DIFFIO_RX_T7N, IO_8_A3/DIFFIO_RX_T8N, IO_8_B3/DIFFIO_RX_T9P, IO_8_B3/DIFFIO_RX_T10P, IO_8_B4/DIFFIO_RX_T10N, IO_8_A5, IO_8_A2/DIFFIO_RX_T13P, IO_8_B2/DIFFIO_RX_T13N

PMIC_IRQ_N R628 X/0-04 ISH_GPIO_15

REV:A0.3

+V1.8A +V3.3A +V1.8A +V3.3A
C597 0.1uF/16VX/04   R808 X/200K-1-04   C595 0.1uF/16VX/04   R806 X/200K-1-04
R809 200K-1-04 I2C_VLS_OE0   R807 200K-1-04 I2C_VLS_OE1
U76 PCA9306DCUR   U75 PCA9306DCUR
GND EN, VREF1 VREF2, SCL1 SCL2, SDA1 SDA2
I2C_SCL0, I2C_SDA0, HAT_I2C0_SCL, HAT_I2C0_SDA
I2C_SCL1, I2C_SDA1, HAT_I2C1_SCL, HAT_I2C1_SDA
C598 0.1uF/16VX/04   C596 0.1uF/16VX/04

reserve for ADC input   REV:A0.3

HAT_ANALOG_IN1 R472 0-04 HAT_R_GPIO1
HAT_ANALOG_IN2 R473 0-04 HAT_UART1_R_RTS
HAT_ANALOG_IN3 R474 0-04 HAT_R_GPIO2
HAT_ANALOG_IN4 R475 0-04 HAT_R_GPIO3

CPU_prog_JTAG_TCK C368 10pF/50V/04
CPU_prog_JTAG_TDO C369 10pF/50V/04
CPU_prog_JTAG_TMS C370 10pF/50V/04
CPU_prog_JTAG_TDI C371 10pF/50V/04

3.3V Level

U52E — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 5 of 11
DATE : JUN_2015
10M04SCU169C8G

HAT_I2S6_BCLK, HAT_I2S6_WS_SYNC, HAT_I2C1_SDA, HAT_I2C1_SDA, HAT_PWM1, HAT_I2S6_SDI, HAT_UART1_CTS, HAT_I2S6_SDO, HAT_I2C1_SCL, HAT_UART1_RXD, HAT_UART1_TXD, HAT_SPI_0_CLK, HAT_SPI_0_FS1, HAT_SPI_0_RXD, HAT_SPI_0_TXD
IO_5_K10/DIFFIO_RX_R1P, IO_5_K11/DIFFIO_RX_R2P, IO_5_J10/DIFFIO_RX_R1N, IO_5_L12/DIFFIO_RX_R2N, IO_5_L13, IO_5_J12/DIFFIO_RX_R3N, IO_5_J9/DIFFIO_RX_R4P, IO_5_J13/DIFFIO_RX_R5P, IO_5_H10/DIFFIO_RX_R4N, IO_5_H13/DIFFIO_RX_R5N, IO_5_H9/DIFFIO_RX_R6P, IO_5_G13/DIFFIO_RX_R7P, IO_5_H8/DIFFIO_RX_R6N, IO_5_G12/DIFFIO_RX_R7N

U52D — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 4 of 11
DATE : JUN_2015
10M04SCU169C8G

GPIO/EXHAT_LVDS4n, GPIO/EXHAT_LVDS5n, GPIO/EXHAT_LVDS5p, GPIO/EXHAT_LVDS6n, GPIO/EXHAT_LVDS6p, GPIO/EXHAT_LVDS0n, GPIO/EXHAT_LVDS0p, GPIO/EXHAT_LVDS7n, GPIO/EXHAT_LVDS7p, GPIO/EXHAT_LVDS1n, LPC_R_AD3, GPIO/EXHAT_LVDS1p, LPC_R_AD2, GPIO/EXHAT_LVDS2n, GPIO/EXHAT_LVDS2p, INT_SERIRQ_R, LPC_R_CLKOUT0, LPC_R_AD0, LPC_CLKRU_N, GPIO/EXHAT_LVDS3n, GPIO/EXHAT_LVDS3p, LPC_R_AD1, LPC_FRAME_R

IO_3_L5/DIFFIO_TX_RX_B1N, IO_3_M4/DIFFIO_TX_RX_B2N, IO_3_L4/DIFFIO_TX_RX_B1P, IO_3_M5/DIFFIO_TX_RX_B2P, IO_3_K5/DIFFIO_TX_RX_B3N, IO_3_N4/DIFFIO_RX_B4N, IO_3_J5/DIFFIO_TX_RX_B3P, IO_3_N5/DIFFIO_RX_B4P, IO_3_N6/DIFFIO_TX_RX_B5P, IO_3_M7/DIFFIO_RX_B6N, IO_3_N8/DIFFIO_RX_B6P, IO_3_J6/DIFFIO_TX_RX_B7N, IO_3_M8/DIFFIO_RX_B8N, IO_3_K6/DIFFIO_RX_B7P, IO_3_M9/DIFFIO_RX_B8P, IO_3_N12, IO_3_M13/DIFFIO_TX_RX_B10N, IO_3_M10/DIFFIO_TX_RX_B11N, IO_3_L11/DIFFIO_TX_RX_B12N, IO_3_M12/DIFFIO_TX_RX_B10P, IO_3_N9/DIFFIO_RX_B11P, IO_3_L11/DIFFIO_TX_RX_B12P, IO_3_J8/DIFFIO_TX_RX_B14N, IO_3_K8/DIFFIO_RX_B14P, IO_3_M10/DIFFIO_TX_RX_B16N, IO_3_L10/DIFFIO_TX_RX_B16P

I2C_VLS_OE0, I2C_VLS_OE1, HAT_R_GPIO3, HAT_R_GPIO1, HAT_R_GPIO2

U52I — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 9 of 11
DATE : JUN_2015
10M04SCU169C8G

enableJTAG, CPU_prog_JTAG_TMS, CPU_prog_JTAG_TCK, CPU_prog_JTAG_TDI, CPU_prog_JTAG_TDO, FPGA_RST, FPGA_OE, CONFIG_SEL, FPGA_fw_reload, nSTATUS, CONF_DONE
IO_1B_E5/JTAGEN, IO_1B_G1/TMS/DIFFIO_RX_L7N, IO_1B_G2/TCK/DIFFIO_RX_L7P, IO_1B_F5/TDI/DIFFIO_RX_L8N, IO_1B_F6/TDO/DIFFIO_RX_L8P, IO_8_B9/DEV_CLRN/DIFFIO_RX_T3N, IO_8_D8/DEV_OE/DIFFIO_RX_T5P, IO_8_D7/CONFIG_SEL, INPUT_ONLY_8_E7/NCONFIG, IO_8_D6/CRC_ERROR/DIFFIO_RX_T9N, IO_8_C4/NSTATUS/DIFFIO_RX_T11P, IO_8_C5/CONF_DONE/DIFFIO_RX_T11N

SDIO_CMD

U52C — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 3 of 11
DATE : JUN_2015
10M04SCU169C8G

GPIO/EXHAT_PLL1_OUTn, GPIO/EXHAT_PLL1_OUTp, HAT_I2C0_SCL, HAT_I2C0_SDA, HAT_SPI_1_CLK, HAT_PWM0, LED3_3V3, HAT_SPI_1_RXD, HAT_SPI_1_TXD
IO_2_M3/PLL_L_CLKOUTN/DIFFIO_RX_L19N, IO_2_L3/PLL_L_CLKOUTP/DIFFIO_RX_L19P, IO_2_J1/DIFFIO_RX_L15N, IO_2_K1/DIFFIO_RX_L15P, IO_2_M1/DIFFIO_RX_L17N, IO_2_M2/DIFFIO_RX_L17P, IO_2_L2, IO_2_K1/DIFFIO_RX_L20N, IO_2_K2/DIFFIO_RX_L20P

U52J — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 10 of 11
DATE : JUN_2015
10M04SCU169C8G
NC_D2, NC_D3, NC_E2

U52H — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 8 of 11
DATE : JUN_2015
10M04SCU169C8G

GPIO/EXHAT_PLL1_INn, GPIO/EXHAT_PLL1_INp, HAT_SPI_1_FS0, HAT_SPI_1_FS0, ISH_GPIO_14, ISH_GPIO_13, OSC_CLK_OUT_1, OSC_CLK_OUT_0, SIO_SPI_2_FS1, SIO_SPI_2_FS0, ISH_GPIO_11, LED2_3V3, HAT_GPIO4, HAT_UART1_R_RTS, SIO_SPI_0_FS1, ISH_GPIO_12
IO_2_G5/CLK0N/DIFFIO_RX_L14N, IO_2_H6/CLK0P/DIFFIO_RX_L14P, IO_2_H5/CLK1N/DIFFIO_RX_L16N, IO_2_H4/CLK1P/DIFFIO_RX_L16P, IO_2_N2/DPCLK0/DIFFIO_RX_L18N, IO_2_N3/DPCLK1/DIFFIO_RX_L18P, IO_6_G9/CLK2P/DIFFIO_RX_R10P, IO_6_G10/CLK2N/DIFFIO_RX_R10N, IO_6_F13/CLK3P/DIFFIO_RX_R12P, IO_6_E13/CLK3N/DIFFIO_RX_R12N, IO_6_F9/DPCLK3/DIFFIO_RX_R16P, IO_6_F10/DPCLK2/DIFFIO_RX_R16N, IO_1B_H1/VREFB1N0, IO_2_L1/VREFB2N0, IO_3_N11/VREFB3N0, IO_5_K13/VREFB5N0, IO_6_D13/VREFB6N0, IO_6_B7/VREFB8N0

U52A — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 1 of 11
DATE : JUN_2015
10M04SCU169C8G

VCCIO1_F2, VCCIO1_G3, VCCIO2_K3, VCCIO2_J3, VCCIO3_L8, VCCIO3_L7, VCCIO3_L6, VCCIO4_J11, VCCIO5_H11, VCCIO5_G11, VCCIO6_F11, VCCIO6_C8, VCCIO7_C8, VCCIO8_C6, VCCIO8_C6, VCCA1_K4, VCCA2_D10, VCCA3_D4, VCCA4_K9, VCC_ONE_H7, VCC_ONE_G8, VCC_ONE_G6, VCC_ONE_F7

REV:A0.3
+V1.8_CPLD, +V3.3_CPLD
R811 X/0-04, R810 0-04, +VLDOA1_2.5V
+V3.3A R787 0-06, +V1.8A R788 0-06

U52K — MAX10 10M02SC U169
VERSION : 1.1
PAGE : 11 of 11
DATE : JUN_2015
10M04SCU169C8G
GND_N13, GND_N1, GND_M6, GND_L9, GND_H12, GND_J4, GND_G7, GND_F3, GND_E11, GND_D5, GND_C3, GND_B8, GND_A13, GND_A1

CONF_DONE CONF_DONE R476 10K-04 +V1.8_CPLD
CONFIG_SEL CONFIG_SEL R477 R478 X/10K-04
FPGA_fw_reload FPGA_fw_reload R479 10K-04
FPGA_OE FPGA_OE R480 R481 X/10K-04
FPGA_RST FPGA_RST R482 R483 X/10K-04
BT_HOST_WAKE R484 R485 X/10K-04
nSTATUS nSTATUS R486 10K-04
CPU_prog_JTAG_TCK R487 1K-04
CPU_prog_JTAG_TDI R488 10K-04
CPU_prog_JTAG_TMS R489 10K-04
enableJTAG enableJTAG R490 10K-04

REV:A0.3

LED section

LED0_3V3 R492 2.2K-04 5% 0402 LED1 1.6*0.8*0.4mm Blue
LED1_3V3 R493 2.2K-04 5% 0402 LED2 1.6*0.8*0.45mm Yellow
LED2_3V3 R494 2.2K-04 5% 0402 LED3 1.6*0.8*0.4mm Green
LED3_3V3 R495 2.2K-04 5% 0402 LED4 1.6*0.8*0.4mm Red

+V3.3_CPLD REV:A0.2
C373 1uF/16V/04, C374 1uF/16V/04, C375 1uF/16V/04, C376 1uF/16V/04
+V1.8_CPLD REV:A0.2
C377 1uF/16V/04, C378 1uF/16V/04, C379 1uF/16V/04, C380 1uF/16V/04
+V3.3_CPLD REV:A0.2
C381 0.1uF/16VX/04, C382 0.1uF/16VX/04, C383 0.1uF/16VX/04, C384 0.1uF/16VX/04
+V1.8_CPLD REV:A0.2
C385 0.1uF/16VX/04, C386 0.1uF/16VX/04, C387 0.1uF/16VX/04, C388 0.1uF/16VX/04

+VCC_SPI C372 0.1uF/16VX/04
CN22 6*2P 27-4121-206-1G-R
CPU_prog_JTAG_TCK, CPU_prog_JTAG_TDO, CPU_prog_JTAG_TMS, SPI_CLK, CPU_prog_JTAG_TDI, SPI_MOSI
SPI_CS0#, SPI_MISO, SPI_SOCK_HOLD_N
SPI_CS0#, SPI_MISO, SPI_SOCK_HOLD_N

Title block

Title: CPLD
Size: C
Document Number: UP-APL01
Rev: A0.3
Date: Wednesday, January 04, 2017
Sheet: 38 of 45
AAEON — an ASUS ASSOC. CO.

DC INPUT

+VIN_EXT

CN23
1
3
2

3P 416AEWTJ02004PA 90D(M)

trace width: 400 mil

+VIN_EXT

trace width: 400 mil

5V

+V5A

Q39
1   8
2   7
3   6
4   5

FDS6681Z

REV:A0.3

trace width: 400 mil

DC_ENABLE_N

+VIN_EXT

R697
1K-04

R698   10K-04   1

Q40
MMBTA92LT1G

R696
100K-04

D22
MMSZ5232B

REV:A0.3

R699
1M-1-04

C392
22uF/10V/08

C393
0.1uF/16VX/04

R765
180K-1-04   REV:A0.2

+V5A

Irms=2.9A

4A

U55

9 IN1
14 IN2

BST 8

C417
22uF/10V/08

C418
22uF/10V/08

C419
0.1uF/16VX/04

C416
0.1uF/16VX/04

R508
910K

R509
4.7-06

REV:A0.3

GND

C420
0.1uF/16VX/04
16V

L16   1.5uH.DCR=20mohm.Irms=6Amp

C423
0.1uF/16VX/04

+V3.3A

V3P3_VR_FREQ 2 FREQ

3VSB_GND

C421 1uF/16V/04

V3P3_VR_VCC 7 VCC

MP8762GLE-Z

SW2 16
SW1 15

V3P3_VR_SW

0402 16V

C425
220pF/25V/04

C426
22uF/10V/08

C422
22uF/10V/08

REV:A0.3

R512
100K-1-04

R511   287K-1-04

C424
0.1uF/16VX/04

42   VREG3.3_PG   R515   0-04

VREG5_PG

6 PG
1 EN

R513
100-1-04

R514
130K

REV:A0.2

R789
287K-1-04

FB 3   V3P3_VR_FB

F=500KHz
Vout=0.611(1+R1/R2)

R517
20K-1-04

SS AGND   PGND1 PGND2 PGND3 PGND4

3VSB_GND

1.5V<EN<6V

+V5A

4 5   10 11 12 13

R700
10K-04

C427
0.22uF/16V/06
16V

VREG5_PG

C561
0.1uF/16VX/04
16V

R518   0-04

3VSB_GND

Title
3.3V

Size A

Document Number
UP-APL01

Rev:
A0.3

Date: *Wednesday, January 04, 2017*

Sheet: **40** of **45**

REV:A0.2

+V5A

FDMC4435BZ

+V5S

C562

0.1uF/16VX/04

R590
10K-04

R591

10K-04

Q27

1
2
3
4

5

C500
22uF/25VX/12

Q28
2N7002WT1G

13,42 PM_SLP_S3#_3P3 PM_SLP_S3#_3P3 G

D

S

+V3.3A

FDMC4435BZ

+V3.3S

+V3.3S

R798
2.2K-04

C563

0.1uF/16VX/04

R594
10K-04

R595

10K-04

Q29

1
2
3
4

5

C501
22uF/6.3V/06

LED5
1.6*0.8*0.4mm Blue

Q30
2N7002WT1G

PM_SLP_S3#_3P3 G

D

S

REV:A0.3

Q51
2N7002WT1G

R815
X/0-04

13 SUS_STAT# G

D

S

Title

System Power

Size
A

Document Number
UP-APL01

Rev:
A0.3

Date: *Wednesday, January 04, 2017*

Sheet: **43** of **45**

AAEON®
an ASUS assoc. co.

SCREW HOLE

Buttom View

MH1	MH2	MH3	MH4	MH5
MH197D107	MH197D107	MH197D107	MH197D107	MH197D107

MH5

MOUNT HOLE

MH1   MH2

REAR CAM BOSS

MH3   MH4

PCB1

PCB

1907UPAP01

FRONT CAM BOSS

Title
Mechanical C omponent

Size
A

Document Number
UP-APL01

Rev:
A0.3

Date: *Wednesday, January 04, 2017*

Sheet: **44** of **45**

HISTORY

DATE	Revision	Description	DATE	Revision	Description
2016.10.19	A02	1. Add LPDDR4 x2 on page 7,18,19. 2. Remove R47 and R46,R75,R78,R67,R728 mount on page 11,12. 3. R178 Change to 10K on page 13. 4. VCCIOA Change to +VDDQ on page 14. 5. Remove VDDQ resistor on page 16,17. 6. Add HPD pull high resistor on page 21,32. 7. Add DDI0_BKLTEN and DDI0_VDDEN pull down resistor on page 21. 8. Add U16, U37 and U40 enable pin of pull high resistor on page 21,32. 9. Change I2C_3V3_SCL7 of pull high resistor connect to +V3.3A on page 21. 10. CN6 power Change to +V3.3A on page 21. 11. U69 and U46 power Change to +V1.8S on page 22,36. 12. Add LPC resistor on page 23. 13. CN15 change to SMD package on page 27. 14. Add EMMC_ CMO pull high resistor on page 34. 15. Add R765 for over voltage protection on page 39. 16. R35,R36,R38,R40 change to 4,7K on page 9. 17. Add DDR ID strap pin on page 12. 18. Add SATA and PCIE control function pin on page 12,23. 19. Add +V1,5S for mini card on page 23. 20. SATA power change to +V5S on page 24. 21. Swap USB3.0 signals on CN13 on page 25. 22. C211,C218,C226 change to 22uF on page 26,27,28. 23. Modify LAN LED signal on page 30,31. 24. LAN ISOLATEB power change to +V3.3S on page 30,31. 25. Remove SATA signal in CN21 on page 37. 26. Add CPLD 1.8V and 3.3V bypass resistor on page 38. 27. Add pull down resistor for VREG3.3_PG on page 40. 28. Change Q22 high side power to +V5A on page 41. 29. Modify +V5S and +V3.3S power switch circuit on page 43.	2016.12.23	A03	1. Remove HDMI0 and add DP port on page 8,32. 2. Add LPSS_UART1_TXD H/W strap pin of pull down resistor on page 11. 3. Add enableJTAG control by SOC on page 12. 4. Add power LED control by SUS_STAT# on page 13,43. 5. Add Mini SATA & Mini PCIE of select pin on page 13,23. 6. Add USB3.0 bypass resistor on page 25,26. 7. Change CN15 to DIP package on page 27. 8. Add U45 CS control pin by ISH_GPIO_2 on page 36. 9. Remove GPIO/EXHAT_LVDS8n/p on page 37. 10. Add I2C0 and I2C1of level shift IC on page 38. 11. Add +VLDOA1_2.5V for CPLD on page 38,42. 12. Change Q39 to FDS6681Z on page 39. 13. Change D22 to MMSZ5232B on page 39. 14. Change L16 package on page 40. 15. Change Q23 to FDMS3664S on page 41. 16. Change Q25 to FDMC4435BZ on page 42. 17. Remove UART2 and add SIO_SPI1,PMW3,DMIC,I2S6 CPLD JTAG on page 11,12,37,38. 18. Change R519,R527,R547 value for OCP on page 41.