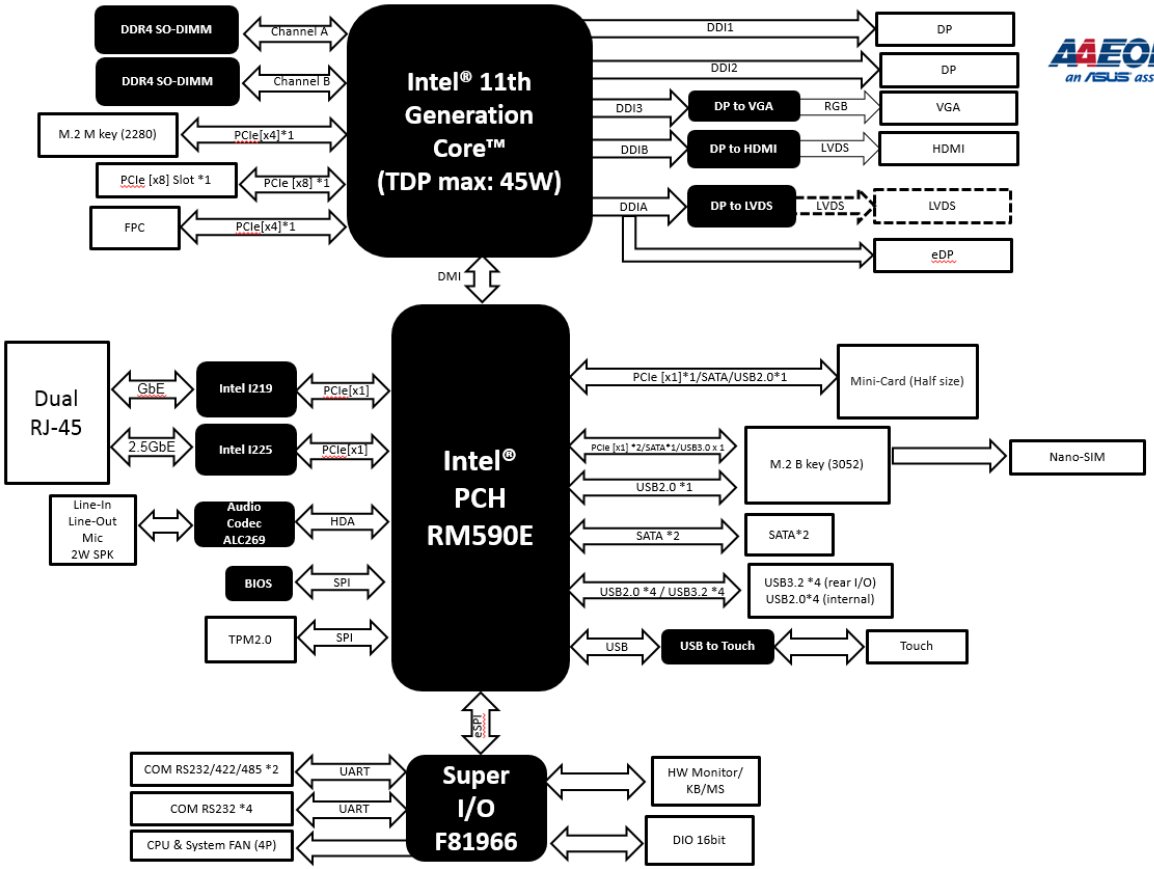
AAEON® an ASUS assoc. co.

Project Name : EPIC-TGH7
Project Number:
Version: A0.1_0_0



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<Variant Name>

AAEON® An ASUS Company

AAEON Technology INC.

Title: Cover Sheet

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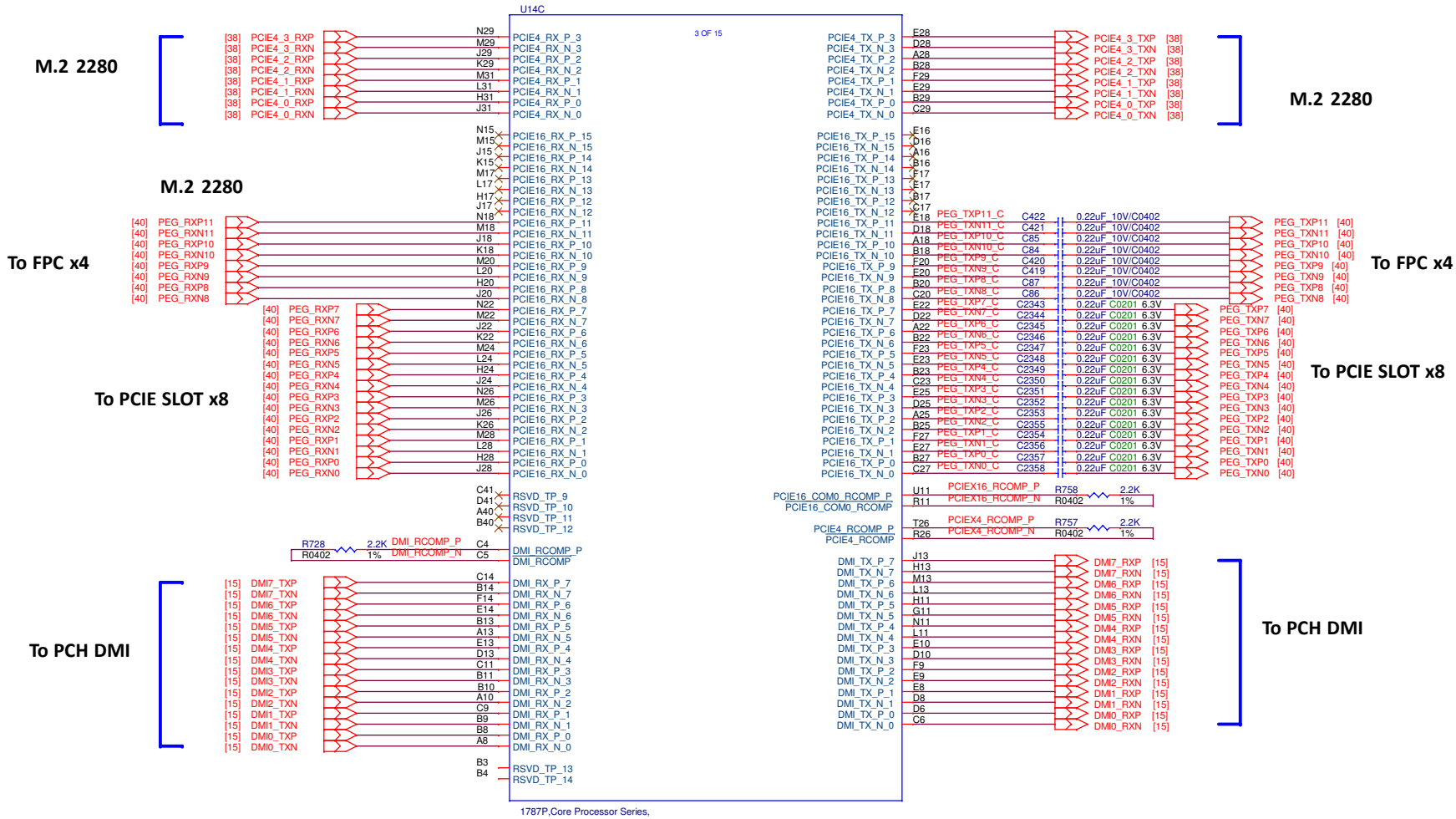
PROCESSOR_DMI/PEG



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AAEON Technology INC.

Title	PROCESSOR_DMI/PEG	
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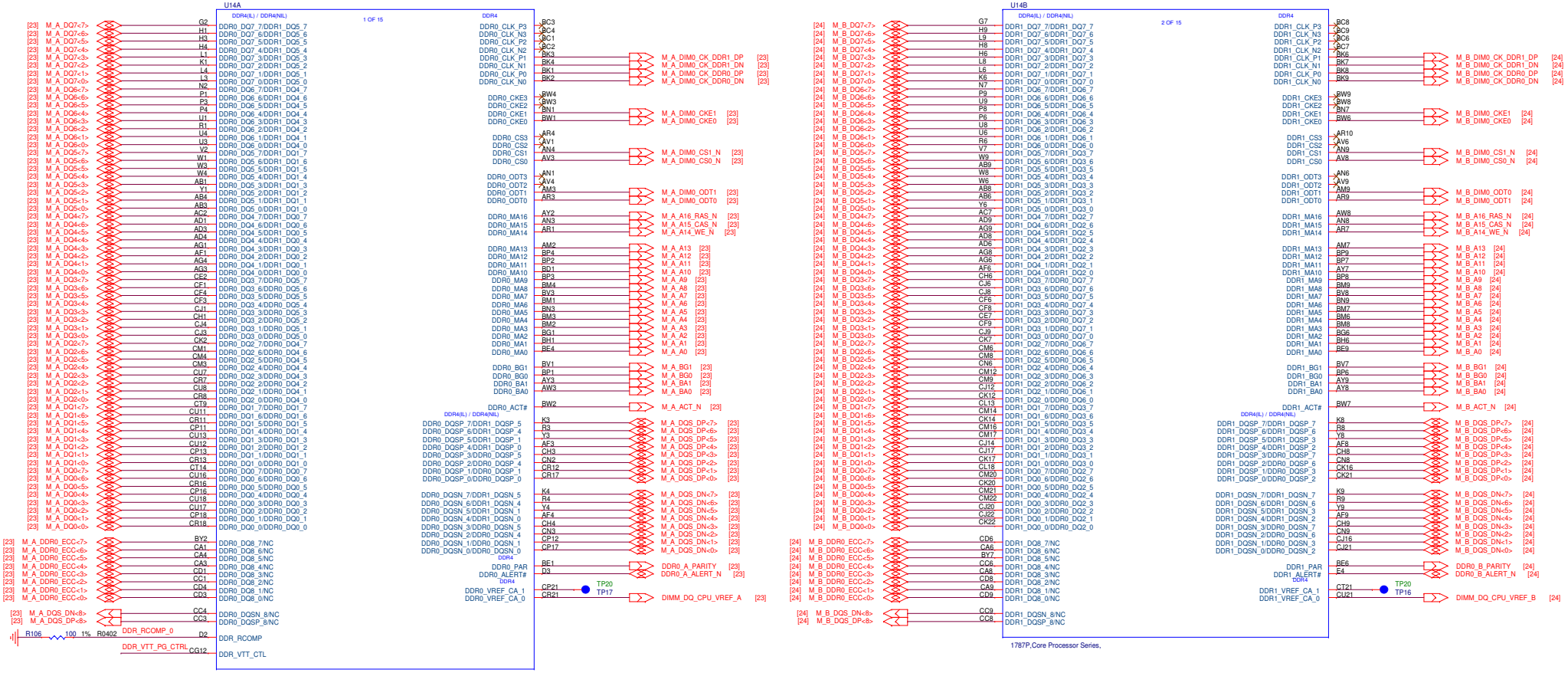
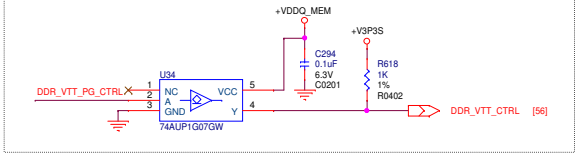
PROCESSOR_DDR4



DDR4 VR Enable Level Shif t er



<Variant Name>

AAEON Technology INC.

Title: PROCESSOR_DDR4

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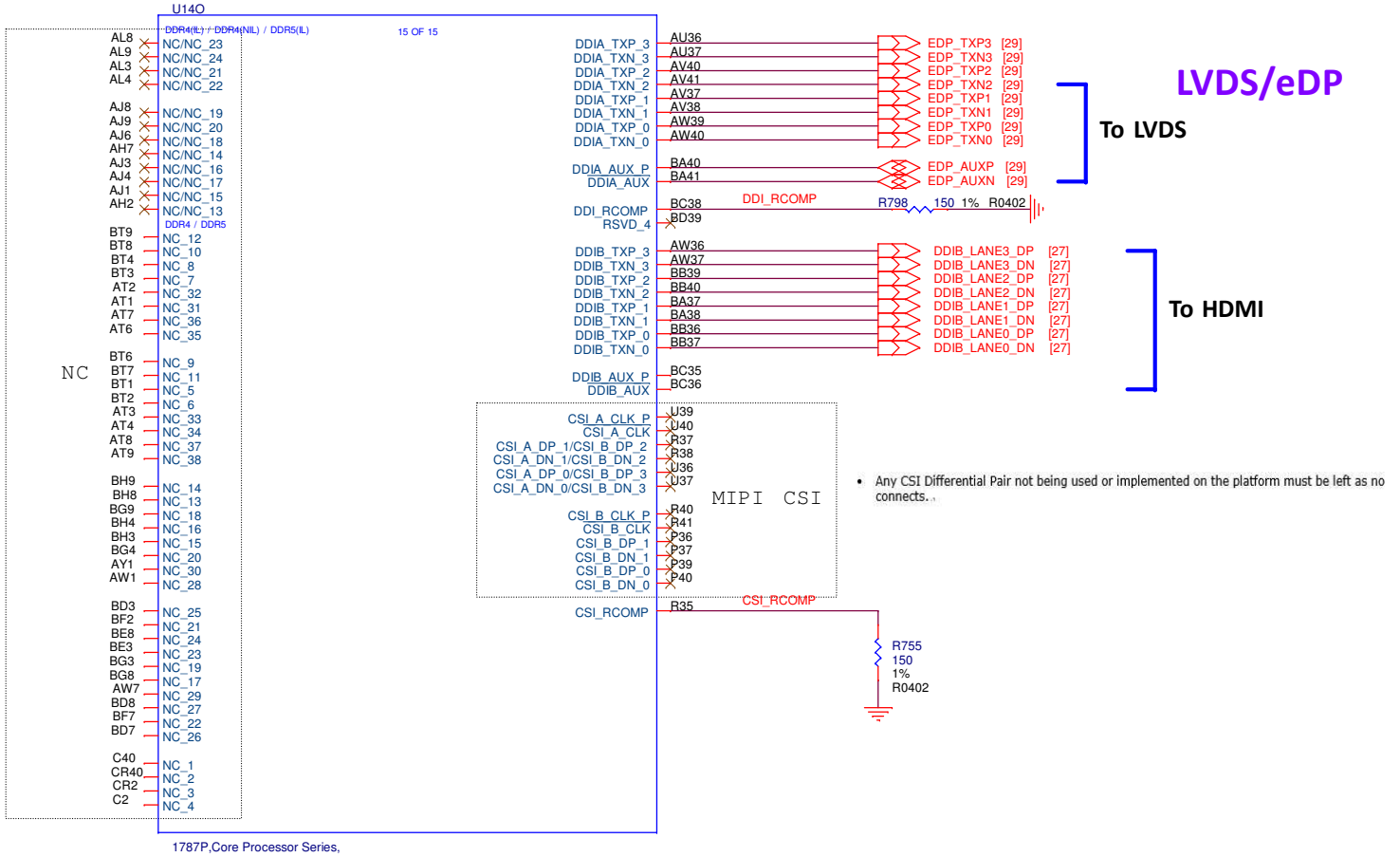
PROCESSOR_DDI/eDP



- Any CSI Differential Pair not being used or implemented on the platform must be left as no connects.

<Variant Name>

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	Title: PROCESSOR_DDI1/eDP	
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PROCESSOR_DDI2

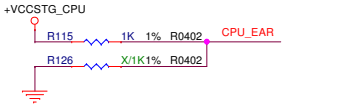
TCP Port Signal Mapping For DisplayPort*

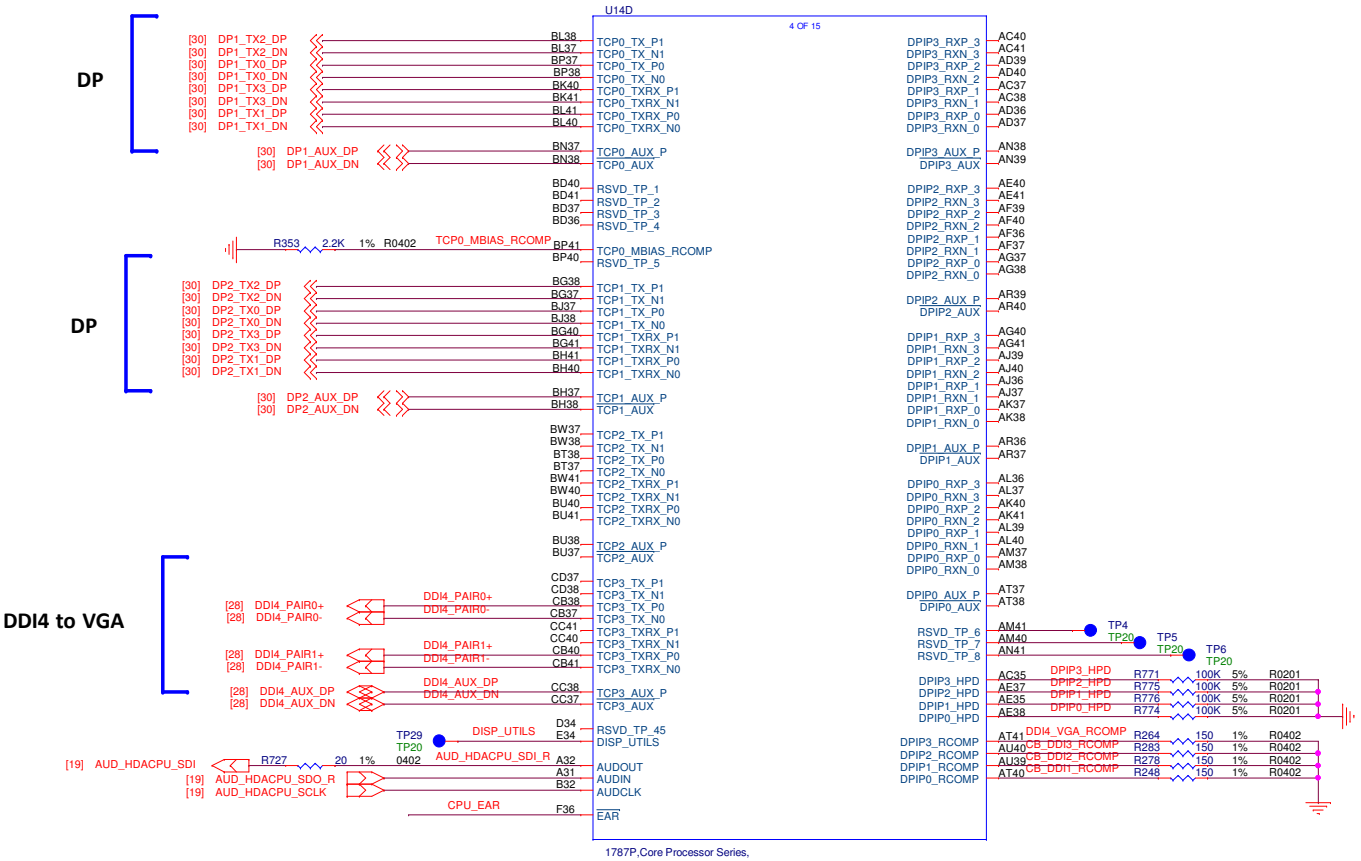
Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3
Note: Apply to TCP ports only.		

DDI Ports Availability

SKU	H Processor Line
DDI A	eDP*
DDI B	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*
TCP1	DP*/HDMI*
TCP2	DP*/HDMI*
TCP3	DP*/HDMI*
DPIP 0	DP*
DPIP 1	DP*
DPIP 2	DP*
DPIP 3	DP*

CPU_EAR	Stall CPU reset sequence until de-asserted:
1 (*)	Normal Operation; No stall.
0	Stall





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AAEON Technology INC.	
Title	PROCESSOR_DDI2
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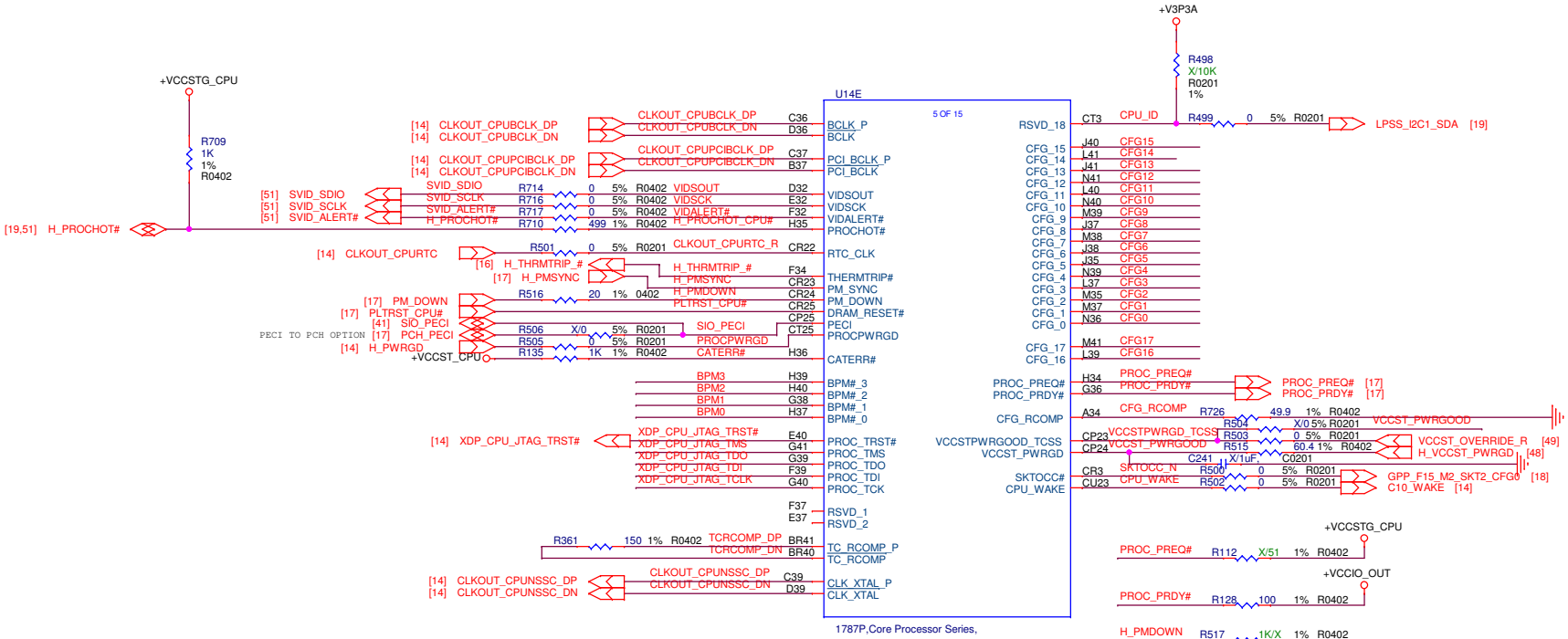
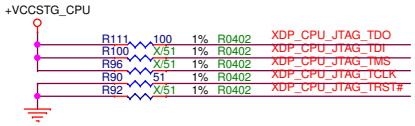
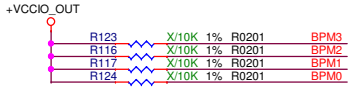
PROCESSOR_CLK/CFG/RSVD



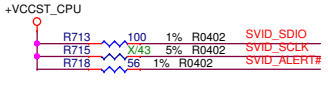
XDP



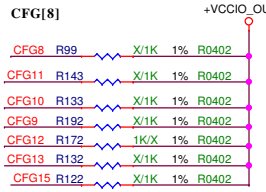
BPM



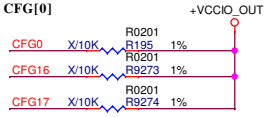
SVID



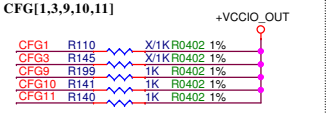
CFG[8]



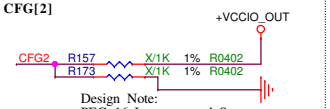
CFG[0]



CFG[1,3,9,10,11]



CFG[2]

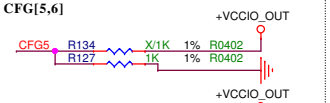


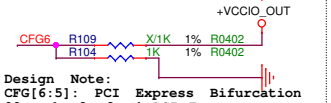
Design Note:
PEGx16 Lane reversal Strap

CFG[4]

Design Note:
CFG[4]:eDP enable strap
0=Enable
1=Disable

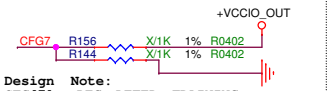
CFG[5,6]





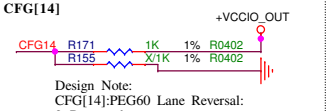
Design Note:
CFG[6:5]: PCI Express Bifurcation
00 = 1 x8, 2 x4 PCI Express
01 = reserved
10 = 2 x8 PCI Express
11 = 1 x16 PCI Express

CFG[7]



Design Note:
CFG[7]: PEG DEFER TRAINING
1(*)=PEG Train immediately following RESET# de assertion
0=PEG Wait for BIOS for training

CFG[14]



Design Note:
CFG[14]:PEG60 Lane Reversal:
0=Reserved
1=Normal(*)

<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.	
	Title: PROCESSOR_CLK/CFG/RSVD	
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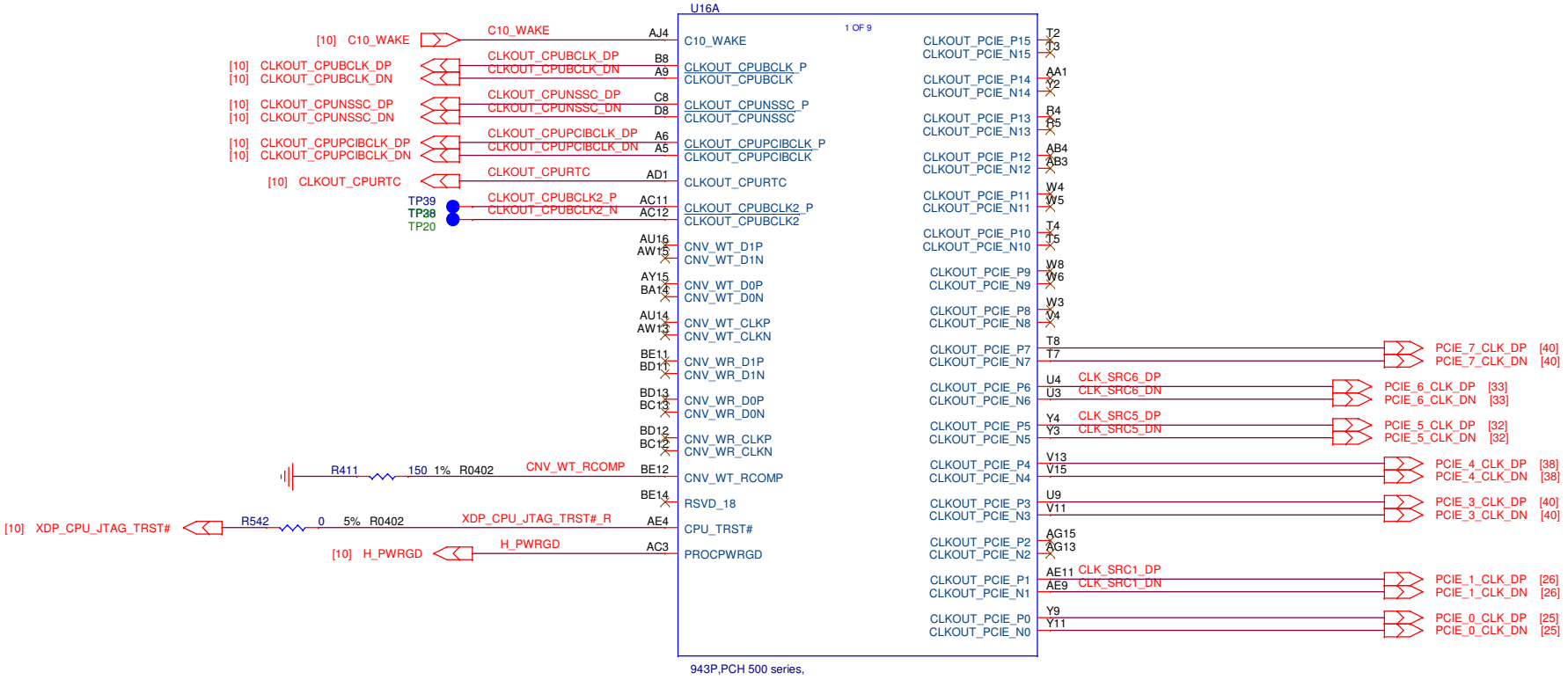
PCH_CLK



Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support
			• CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

<Variant Name>

AAEON® An ASUS Company	AAEON Technology INC.	
	Title: PCH_CLK	
	Size	Document Number: EPIC-TGH7 — Rev: A0.1_0_0
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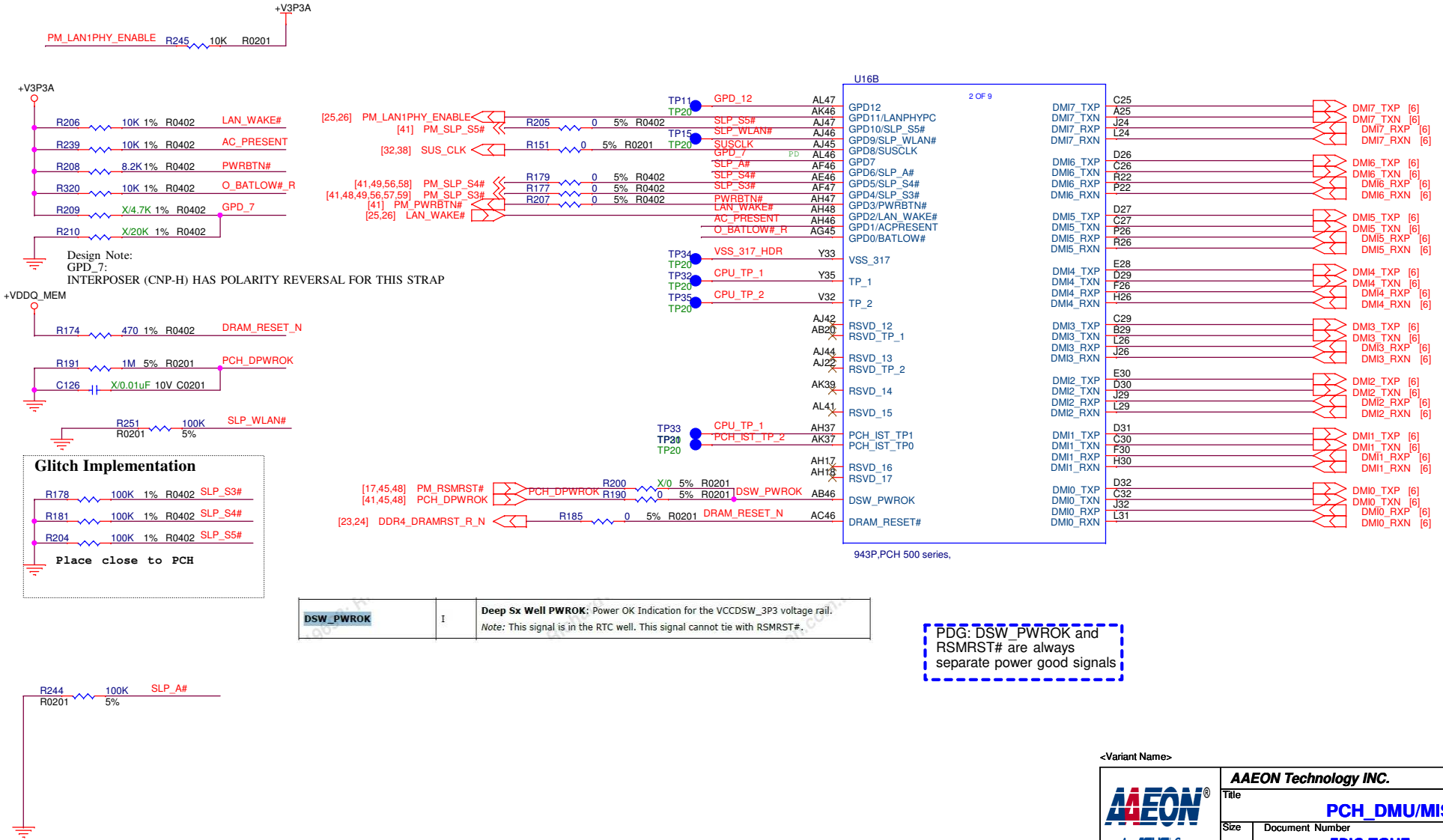
PCH 3_DMI/MISC



DSW_PWROK	I	**Deep Sx Well PWROK**: Power OK Indication for the VCCDSW_3P3 voltage rail. *Note:* This signal is in the RTC well. This signal cannot tie with RSMRST#.

PDG: DSW_PWROK and RSMRST# are always separate power good signals

<Variant Name>

AAEON Technology INC.

Title	PCH_DMU/MISC	
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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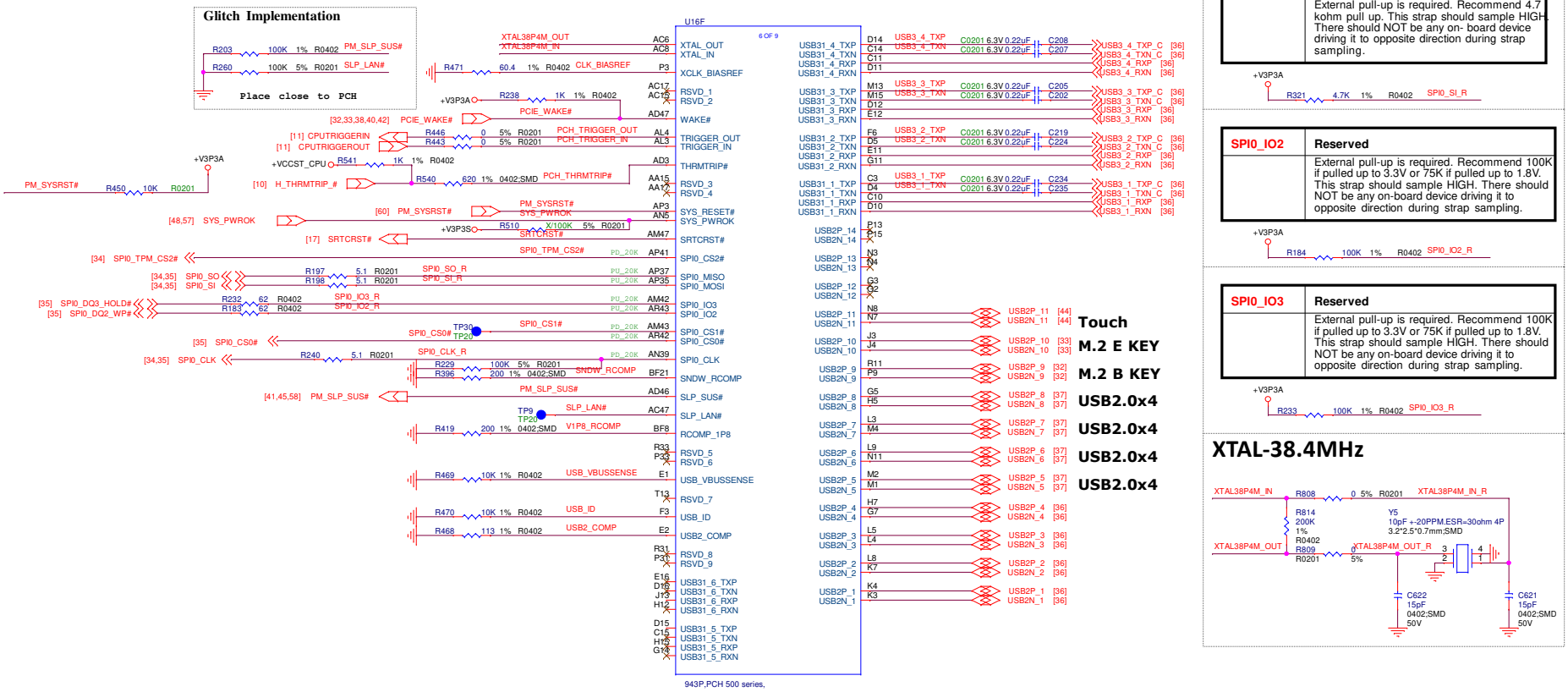
PCH 4_USB3/USB2/SPI



SPI0_MOSI	Reserved
	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on- board device driving it to opposite direction during strap sampling.

SPI0_IO2	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

XTAL-38.4MHz

<Variant Name>

AAEON Technology INC.

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Title	PCH_USB3/USB2/SPI	
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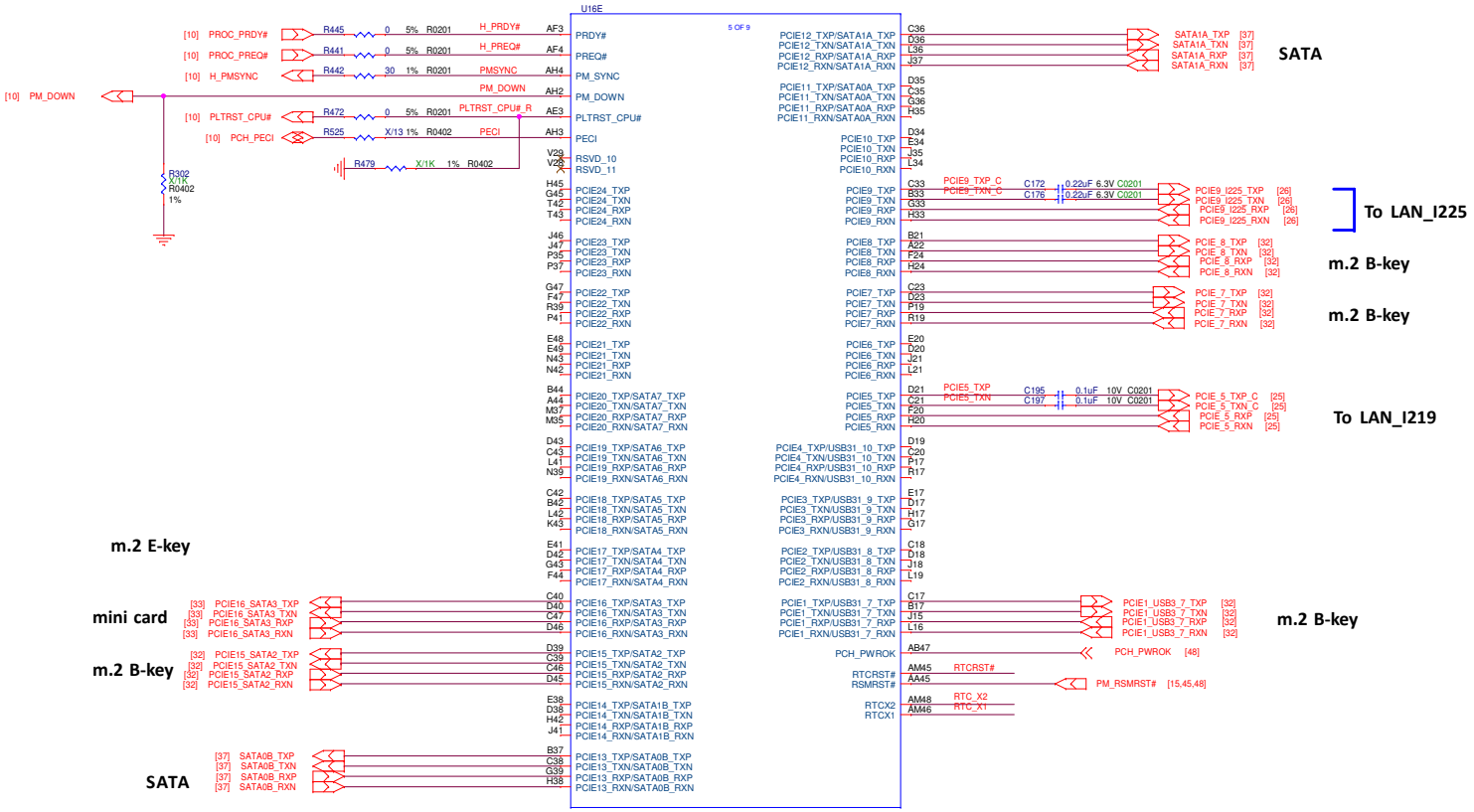
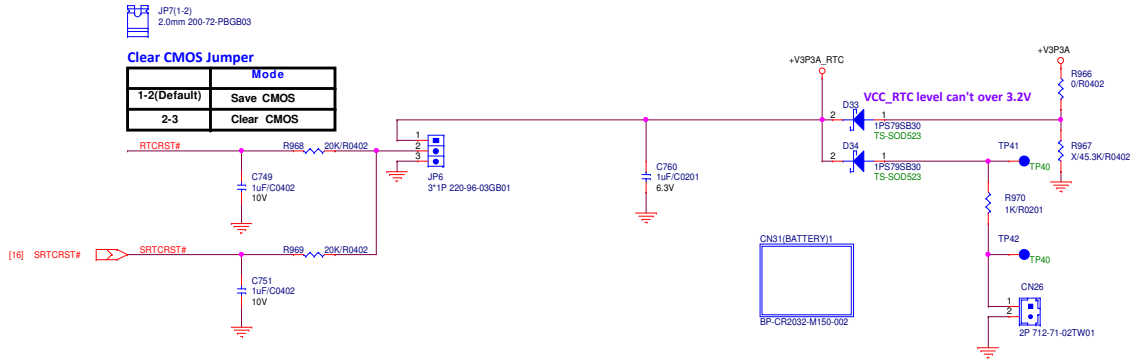
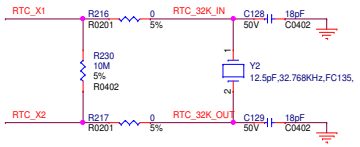
PCH 4_PCIE/SATA/RTC







<Variant Name>

AAEON Technology INC.		
Title: PCH_PCIE/SATA/RTC		
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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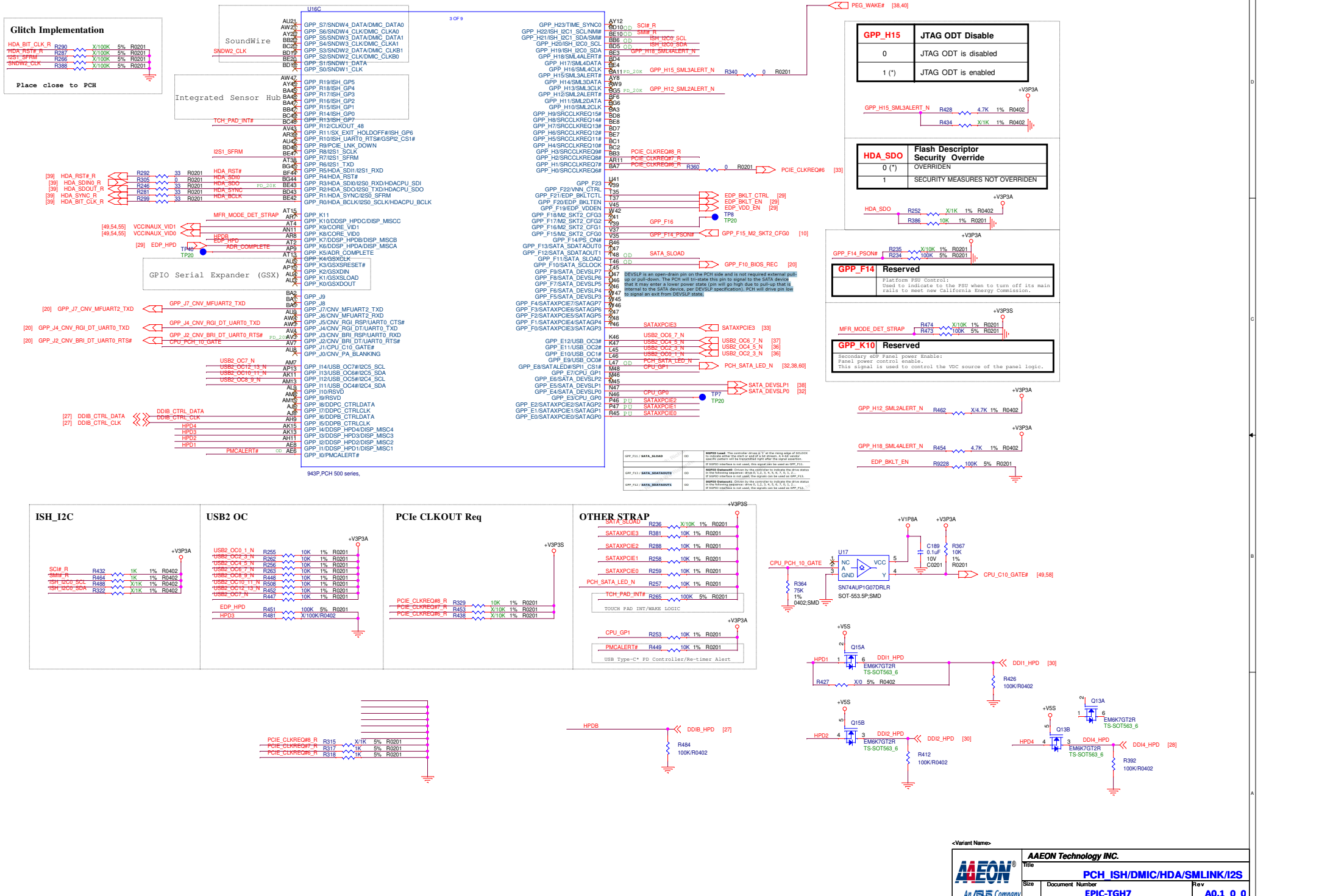
PCH 5_ISH/DMIC/HDA/SMLINK/I2S



PCH 6_UART/GPIO/eSPI/JTAG/SMB

SMBALERT#	TLS confidentiality
0	TLS CONFIDENTIALITY DISABLE
1 (*)	TLS CONFIDENTIALITY ENABLE

SML0ALERT#	ESPI
0 (*)	Enable eSPI
1	Disable eSPI

SML1ALERT#	CPUNSSC CLOCK FREQ
0 (*)	38.4MHZ CLOCK FROM DIRECT CRYSTAL
1	19.2MHZ CLOCK FROM DIVIDER

Design Note:
When used as PCHHOT# and strap low, a 150 kohm pull-up is needed to ensure it does not override the internal pull-down strap sampling.

GSPI1_MOSI	BOOT BIOS STRAP
0 (*)	SPI SELECTED
1	eSPI SELECTED FOR SYSTEM FLASH

GSPI0_MOSI	No Reboot
0 (*)	REBOOT ENABLED
1	NO REBOOT

SPKR	Top Swap Override
0 (*)	Disabled
1	Enable

Glitch Implementation

U16D — 4 OF 9 — 943P,PCH 500 series,

Touch Host Controller (THC)

SMBus Level Shift

DBG_PMODE	Reserved
	This strap should sample high. There should NOT be any on- board device driving it to opposite direction during strap sampling.

VRALERT#	Reserved
	VR Alert: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.

Place close to PCH

<Variant Name>

AAEON Technology INC.

Title: PCH_UART/GPIO/eSPI/JTAG/SMB

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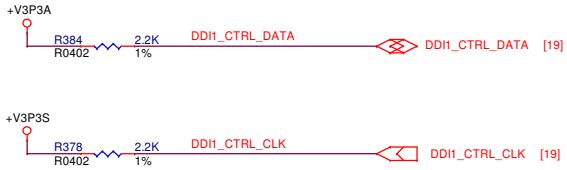
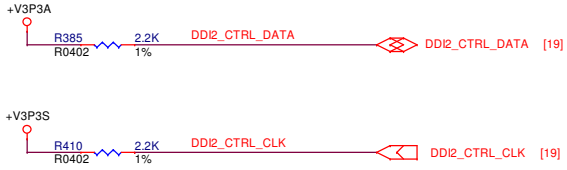
PCH 7_OTHER STRAP

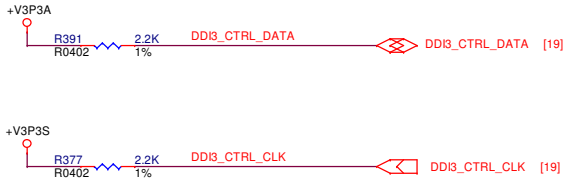
TBT_LSX0	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



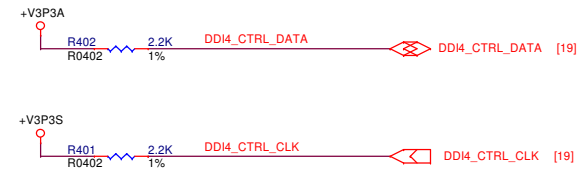
TBT_LSX1	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



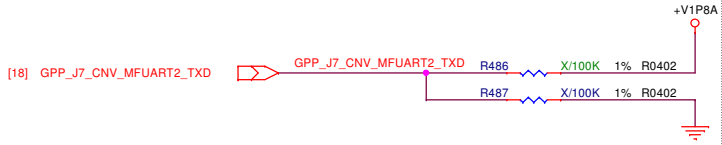
TBT_LSX2	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



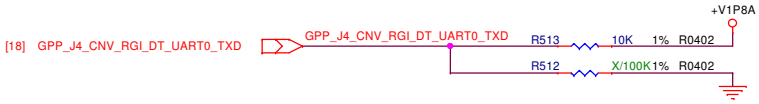
TBT_LSX3	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1(*)	3.3V



GPP_J7	Reserved
	For CNVi and discrete connectivity : Optional WLAN/Bluetooth* WWAN co-existence signal (Output)



GPP_J4	CNVI STRAP
0	CNVI ENABLE
1 (*)	CNVI DISABLE



GPP_J2	XTAL SELECT
0 (*)	38.4/19.2MHZ
1	24MHZ

GPP_F10	Reserved
	SGPIO Reference Clock: The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. The SClock frequency supported is 32 kHz. If SGPIO interface is not used, this signal can be used as GPP_F10.

<Variant Name>

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Title: OTHER STRAP

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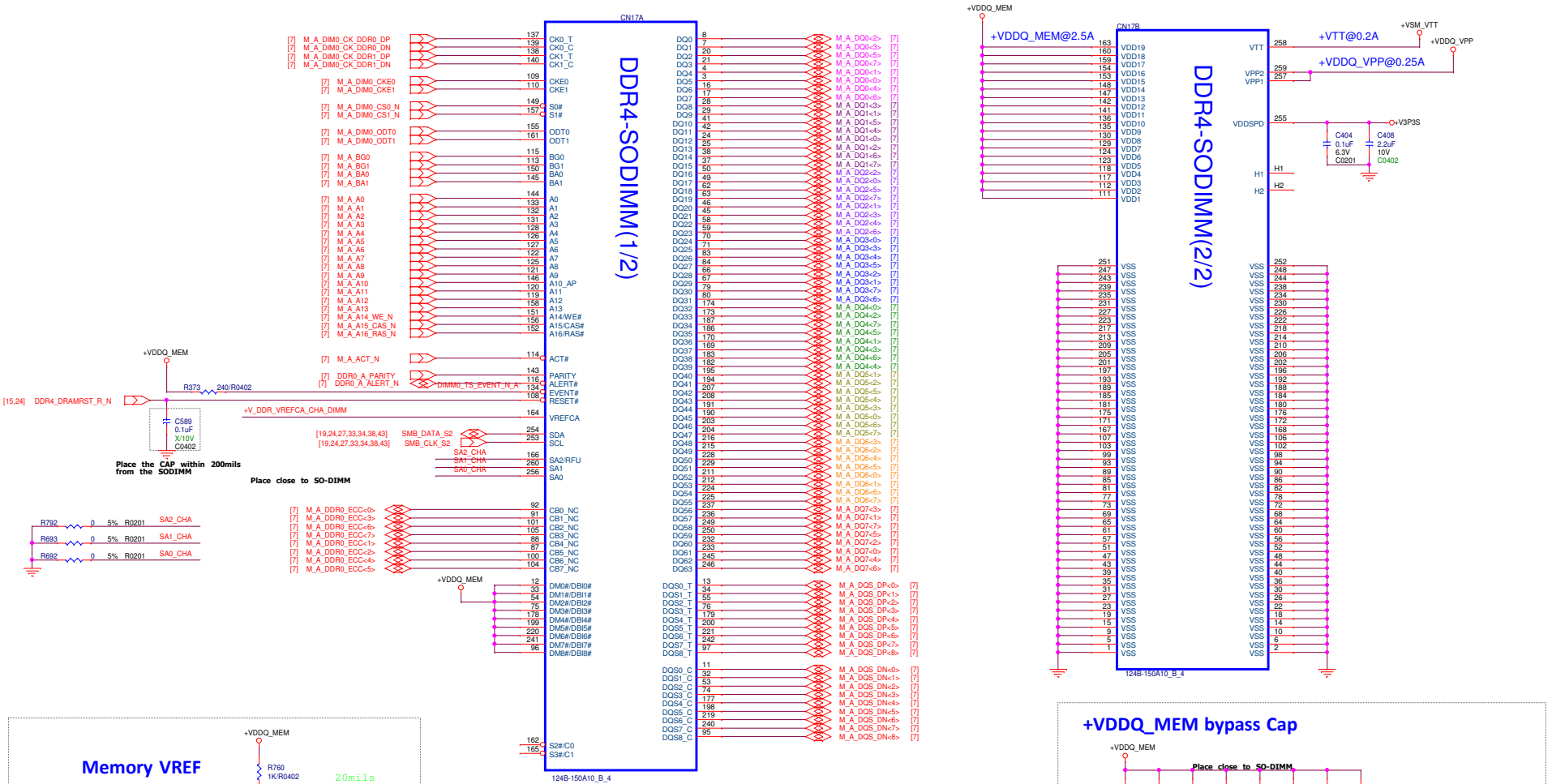
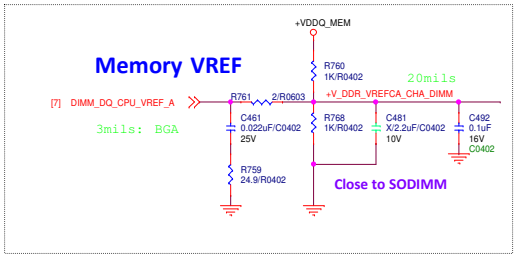
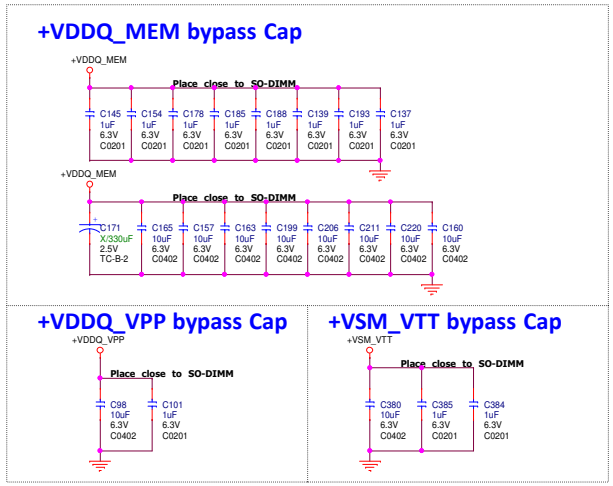
DDR4-SODIMM_A







<Variant Name>

AAEON Technology INC.

Title	DDR4-SODIMM_A	
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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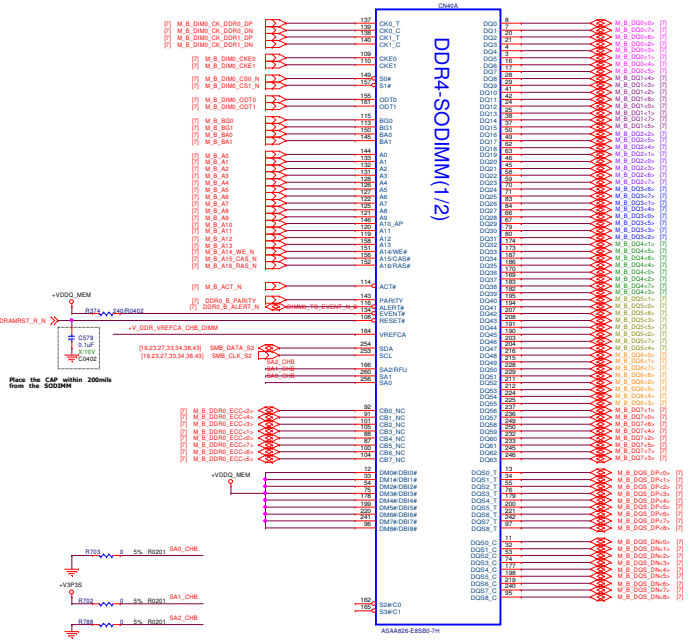
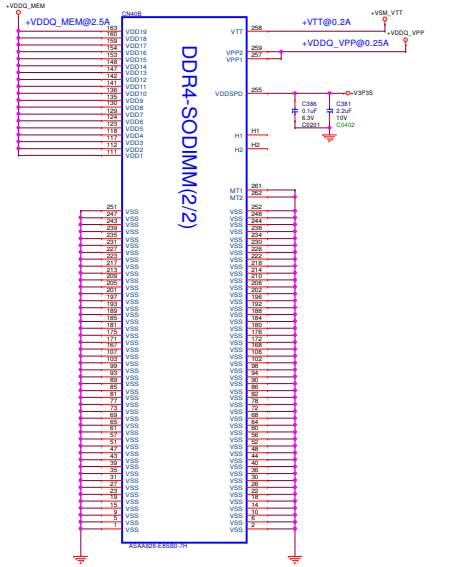
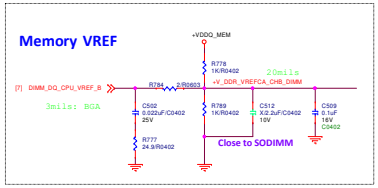
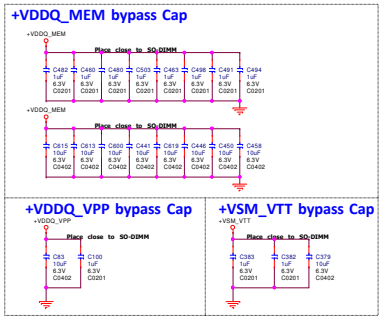
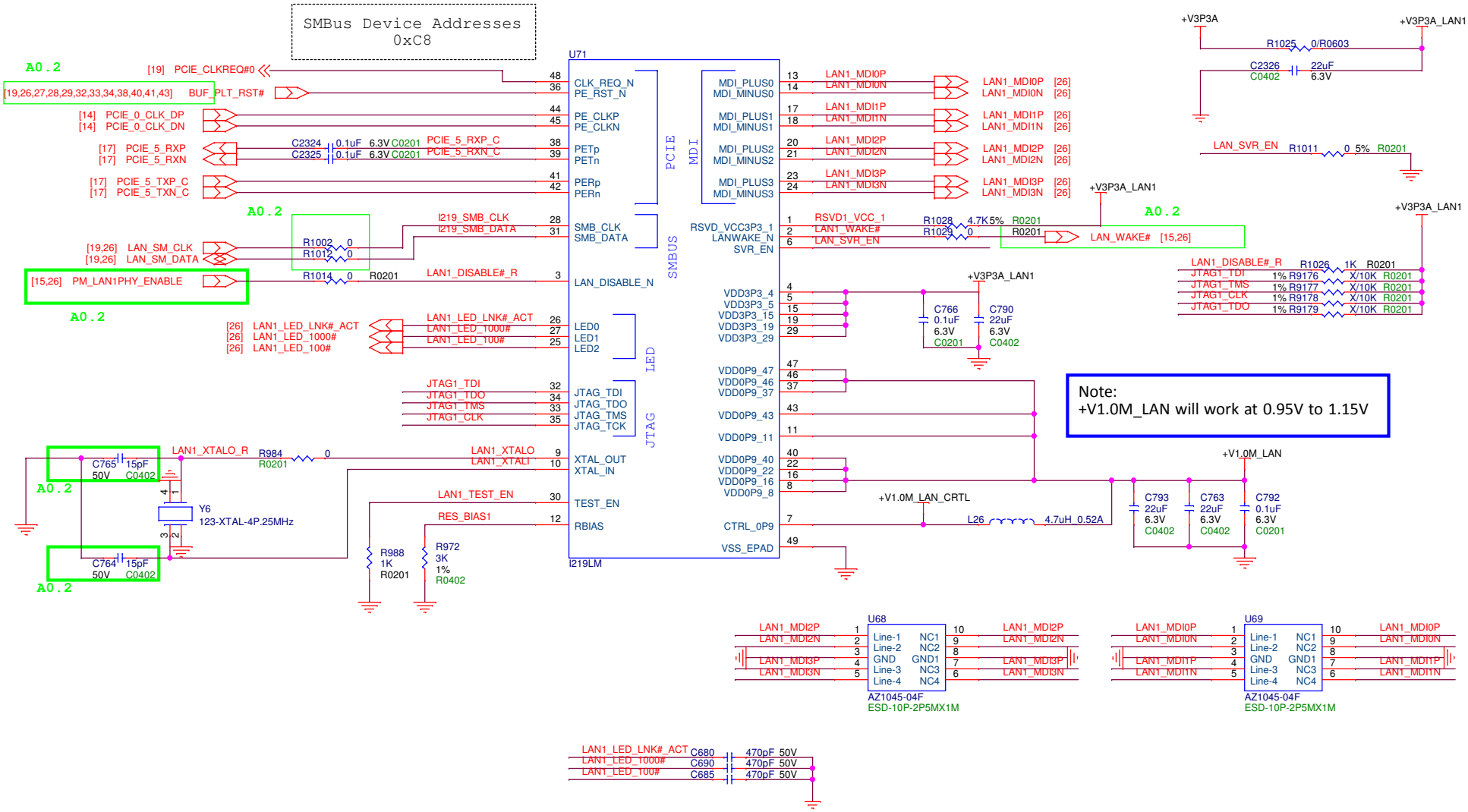
DDR4-SODIMM_B











<Variant Name>

AAEON Technology INC.

Title: LAN1_INTEL i219LM

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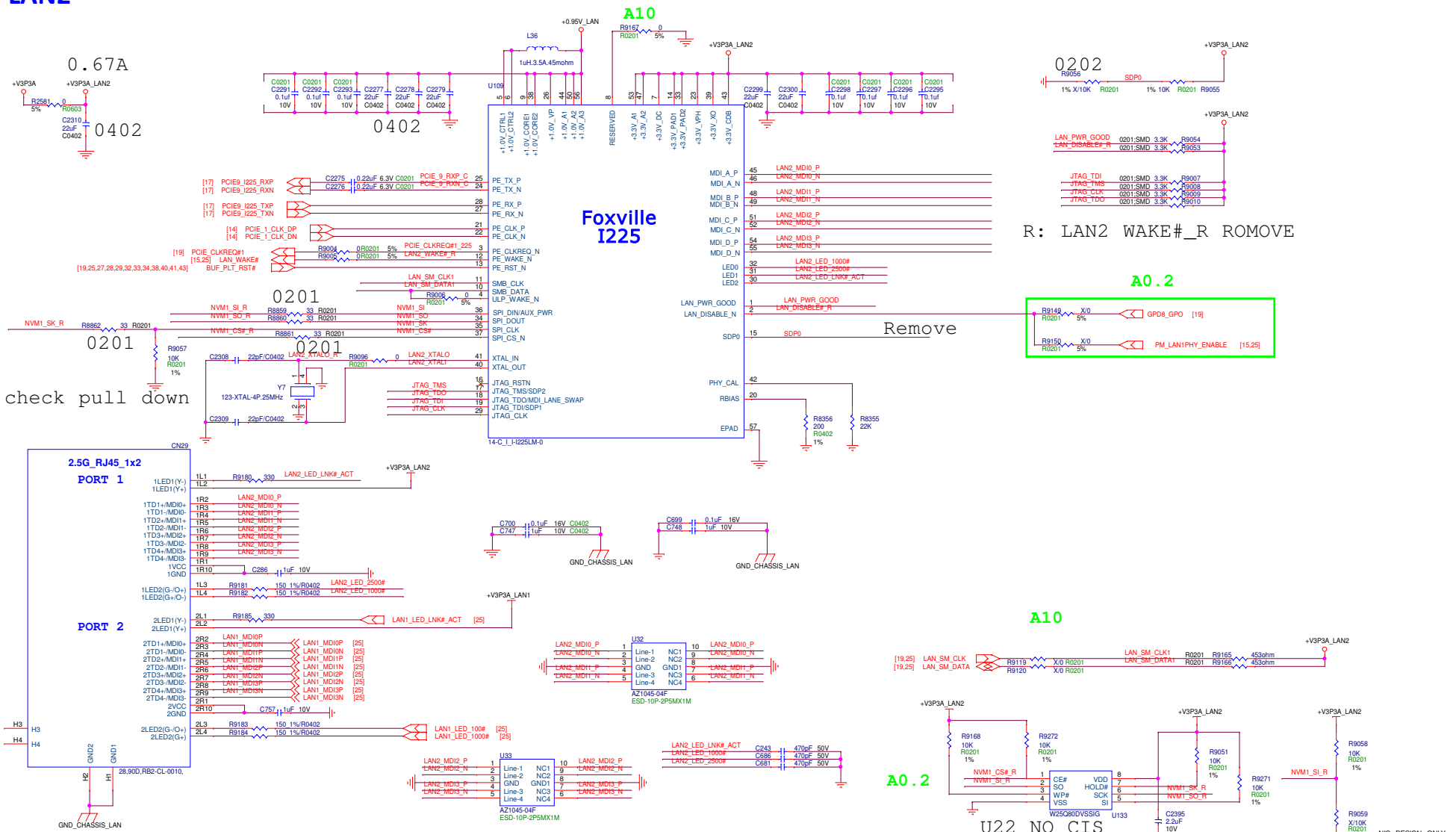
LAN2



<Variant Name>

AAEON Technology INC.

Title	LAN2_INTEL i225LM	
Size	Document Number	Rev
	EPIC-TGH7	A0.1_0_0
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DDIB to HDMI1

DDI1 to HDMI1 Mapping table

DDI1 Pairs	HDMI1 Signals
DDI1_LANE0_DP	HDMI1_D2_DP
DDI1_LANE0_DN	HDMI1_D2_DN
DDI1_LANE1_DP	HDMI1_D1_DP
DDI1_LANE1_DN	HDMI1_D1_DN
DDI1_LANE2_DP	HDMI1_D0_DP
DDI1_LANE2_DN	HDMI1_D0_DN
DDI1_LANE3_DP	HDMI1_CLK_DP
DDI1_LANE3_DN	HDMI1_CLK_DN
DDI1_CTRL_CLK	HDMI1_SCL
DDI1_CTRL_DATA	HDMI1_SDA
DDI1_AUX_DN	
DDI1_AUX_DP	
DDI1_HPD	HDMI1_HPD

<Variant Name>

AAEON Technology INC.

Title	HDMI	
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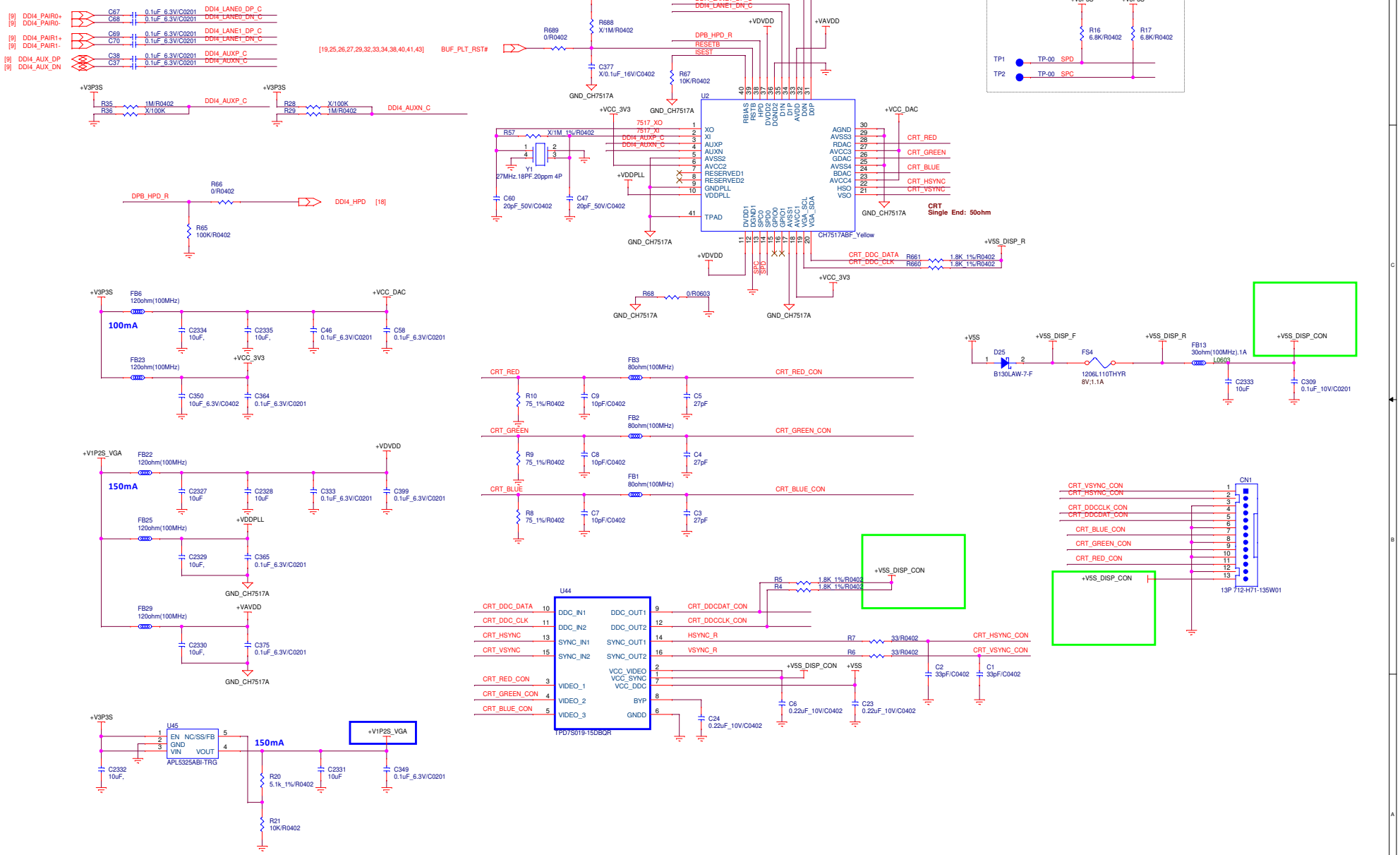
CRT

DDI Interface
Differential Pair: 85ohm



<Variant Name>

AAEON Technology INC.		
Title: DP to VGA		
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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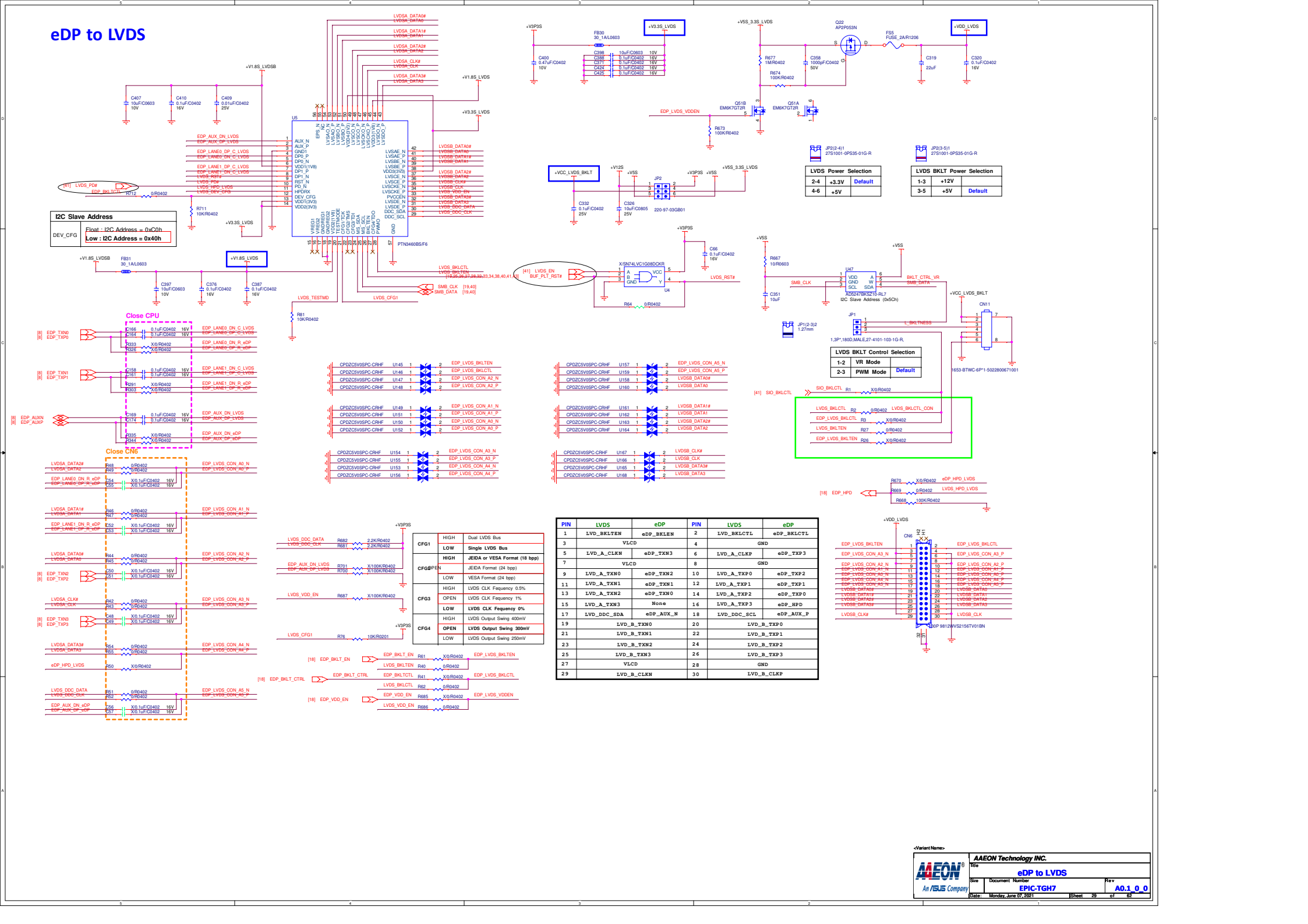
eDP to LVDS


I2C Slave Address
DEV_CFG
Float : I2C Address = 0xC0h
Low : I2C Address = 0x40h
LVDS Power Selection
2-4 +3.3V Default
4-6 +5V
LVDS BKLT Power Selection
1-3 +12V
3-5 +5V Default
LVDS BKLT Control Selection
1-2 VR Mode
2-3 PWM Mode Default
Close CPU
Close CN6
PTN3460BS/F6
AD5247BKSZ10-RL7
I2C Slave Address (0x5Ch)
CFG1 HIGH Dual LVDS Bus
LOW Single LVDS Bus
CFG2 HIGH JEIDA or VESA Format (18 bpp)
OPEN JEIDA Format (24 bppp)
LOW VESA Format (24 bppp)
CFG3 HIGH LVDS CLK Fequency 0.5%
OPEN LVDS CLK Fequency 1%
LOW LVDS CLK Fequency 0%
CFG4 HIGH LVDS Output Swing 400mV
OPEN LVDS Output Swing 300mV
LOW LVDS Output Swing 250mV
PIN LVDS eDP PIN LVDS eDP
1 LVD_BKLTEN eDP_BKLEN 2 LVD_BKLCTL eDP_BKLCTL
3 VLCD 4 GND
5 LVD_A_CLKN eDP_TXN3 6 LVD_A_CLKP eDP_TXP3
7 VLCD 8 GND
9 LVD_A_TXN0 eDP_TXN2 10 LVD_A_TXP0 eDP_TXP2
11 LVD_A_TXN1 eDP_TXN1 12 LVD_A_TXP1 eDP_TXP1
13 LVD_A_TXN2 eDP_TXN0 14 LVD_A_TXP2 eDP_TXP0
15 LVD_A_TXN3 None 16 LVD_A_TXP3 eDP_HPD
17 LVD_DDC_SDA eDP_AUX_N 18 LVD_DDC_SCL eDP_AUX_P
19 LVD_B_TXN0 20 LVD_B_TXP0
21 LVD_B_TXN1 22 LVD_B_TXP1
23 LVD_B_TXN2 24 LVD_B_TXP2
25 LVD_B_TXN3 26 LVD_B_TXP3
27 VLCD 28 GND
29 LVD_B_CLKN 30 LVD_B_CLKP
AAEON Technology INC.
Title eDP to LVDS
Size Document Number EPIC-TGH7 Rev A0.1_0_0
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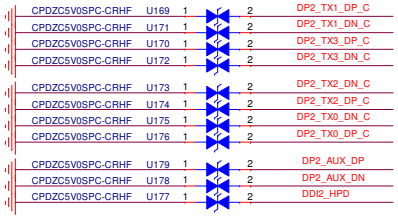
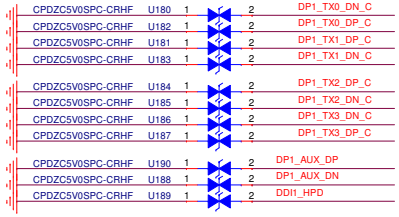
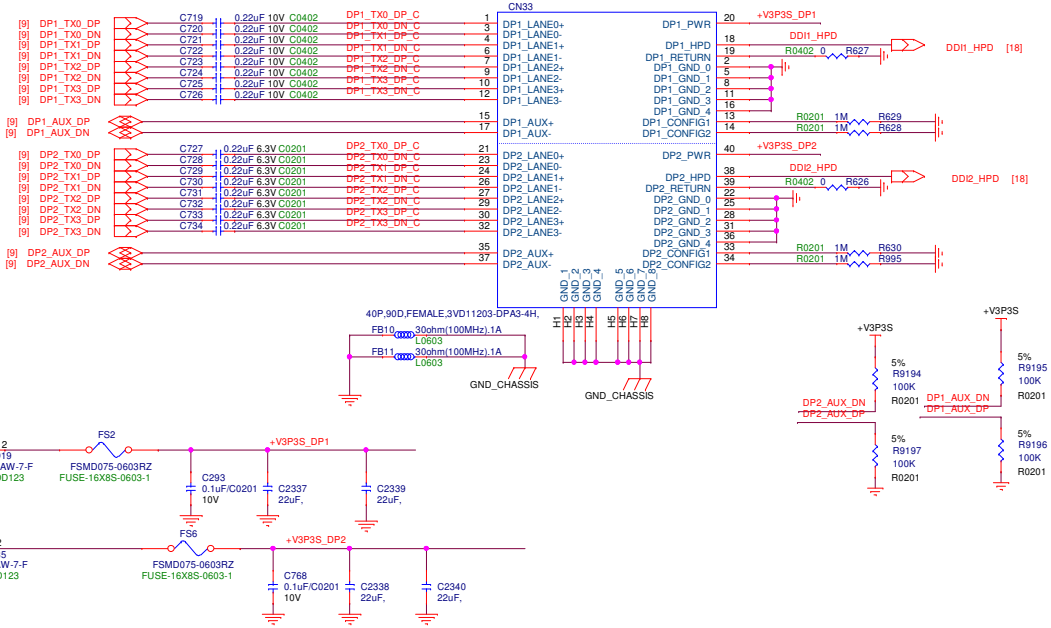
Display Port 1







<Variant Name>

AAEON® An ASUS Company

AAEON Technology INC.

Title: **Display port**

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REMOVE

<Variant Name>

AAEON Technology INC.

Title	M.2 M-KEY	
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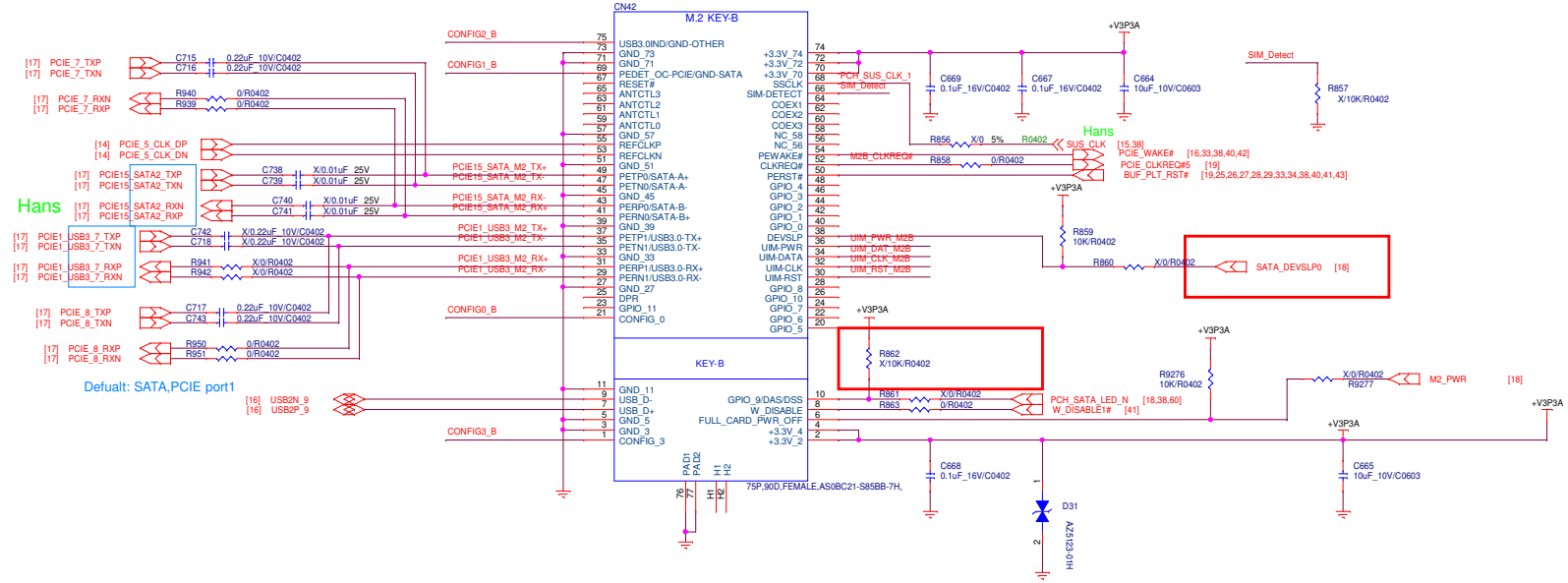
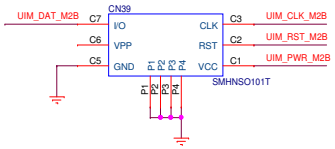
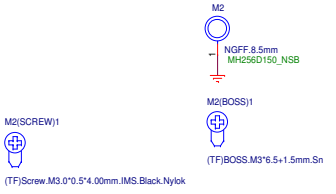
M.2 Key B(3052 need colay 3042)



CONFIG 0	1	2	3	Type	Port Config
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIE	N/A
0	0	1	0	WWAN - PCIe	0
0	1	1	0	WWAN - PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3





<Variant Name>

AAEON Technology INC.

Title	M.2 B-KEY
Size	
Document Number	EPIC-TGH7
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Date:	Monday, June 07, 2021
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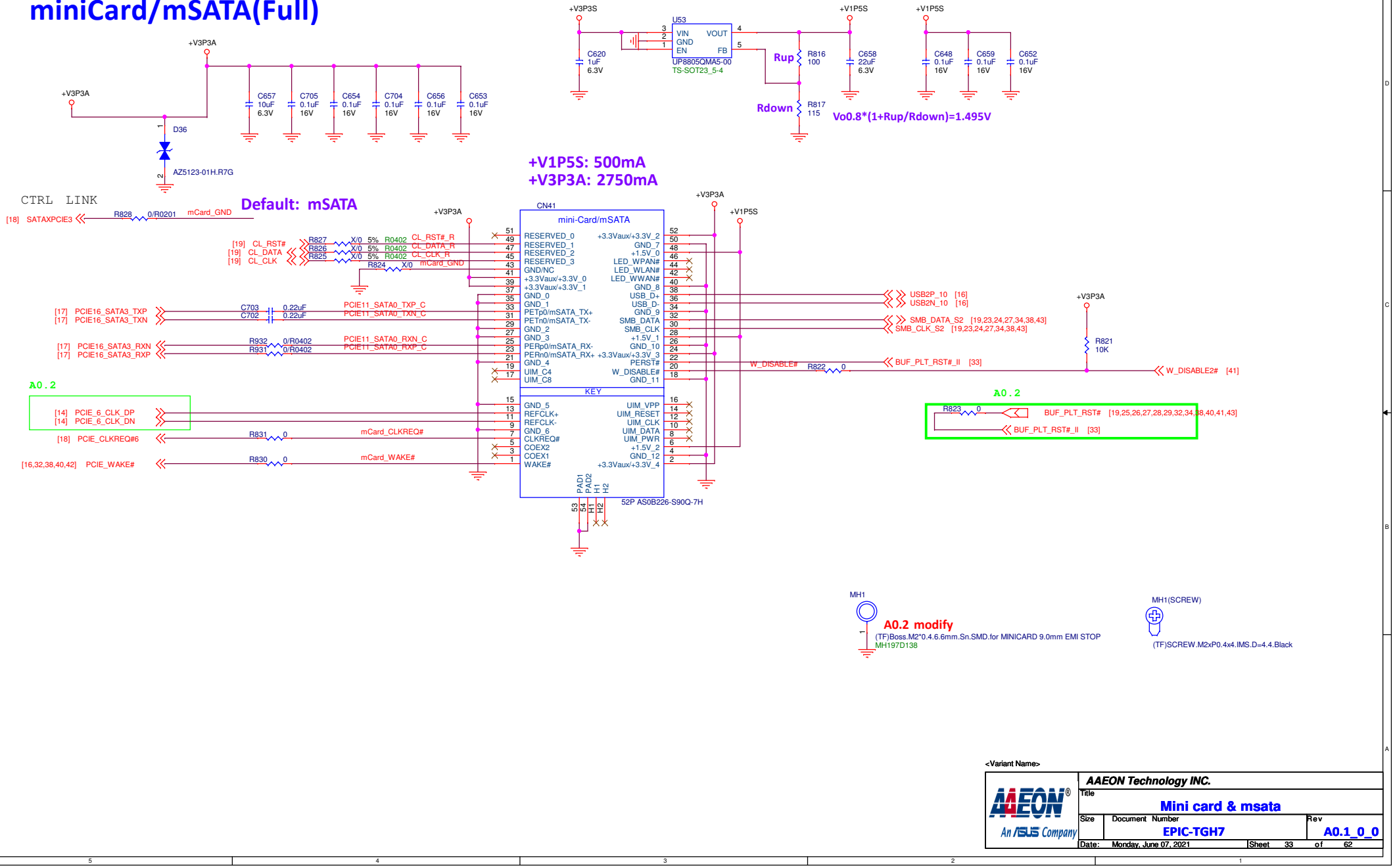
miniCard/mSATA(Full)



<Variant Name>

AAEON Technology INC.

Title: Mini card & msata

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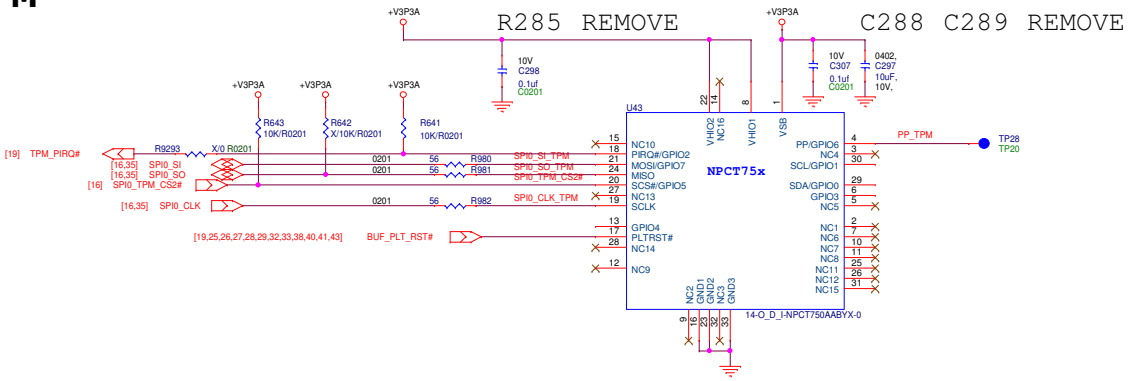
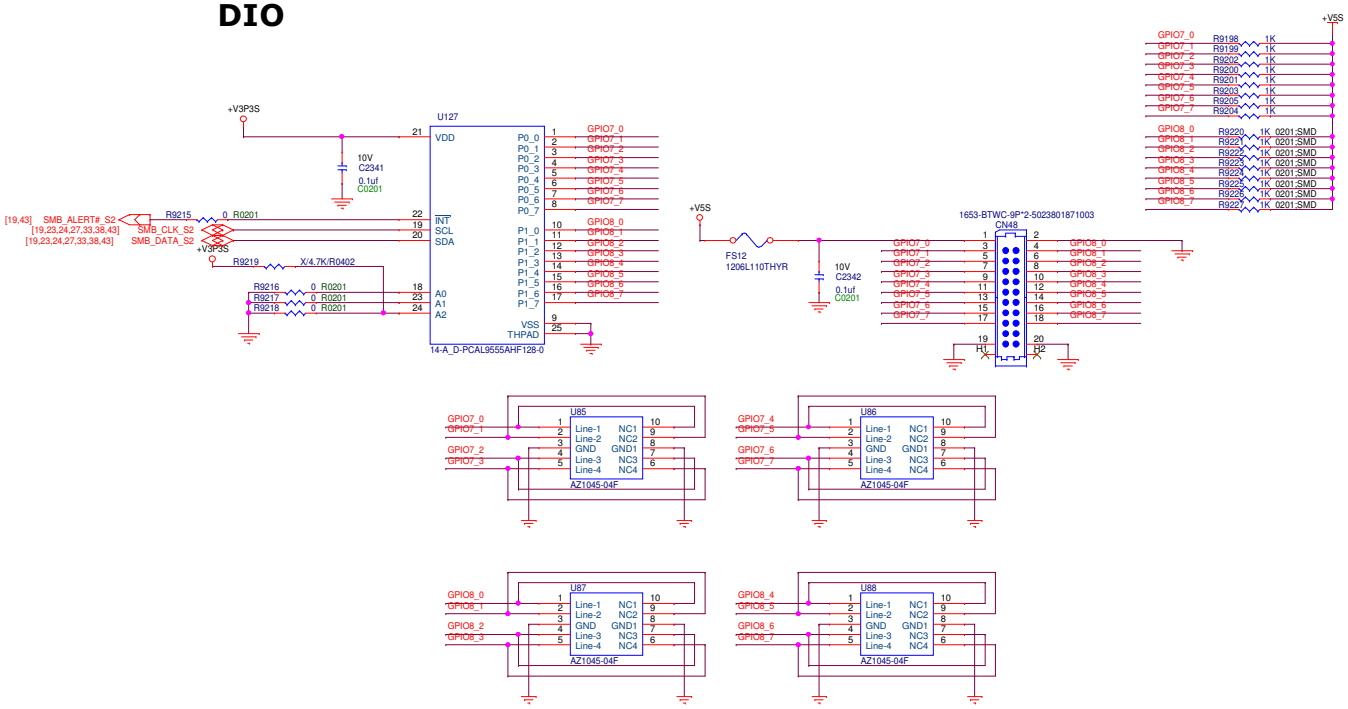
TPM



DIO



<Variant Name>

AAEON Technology INC.

Title	TPM	
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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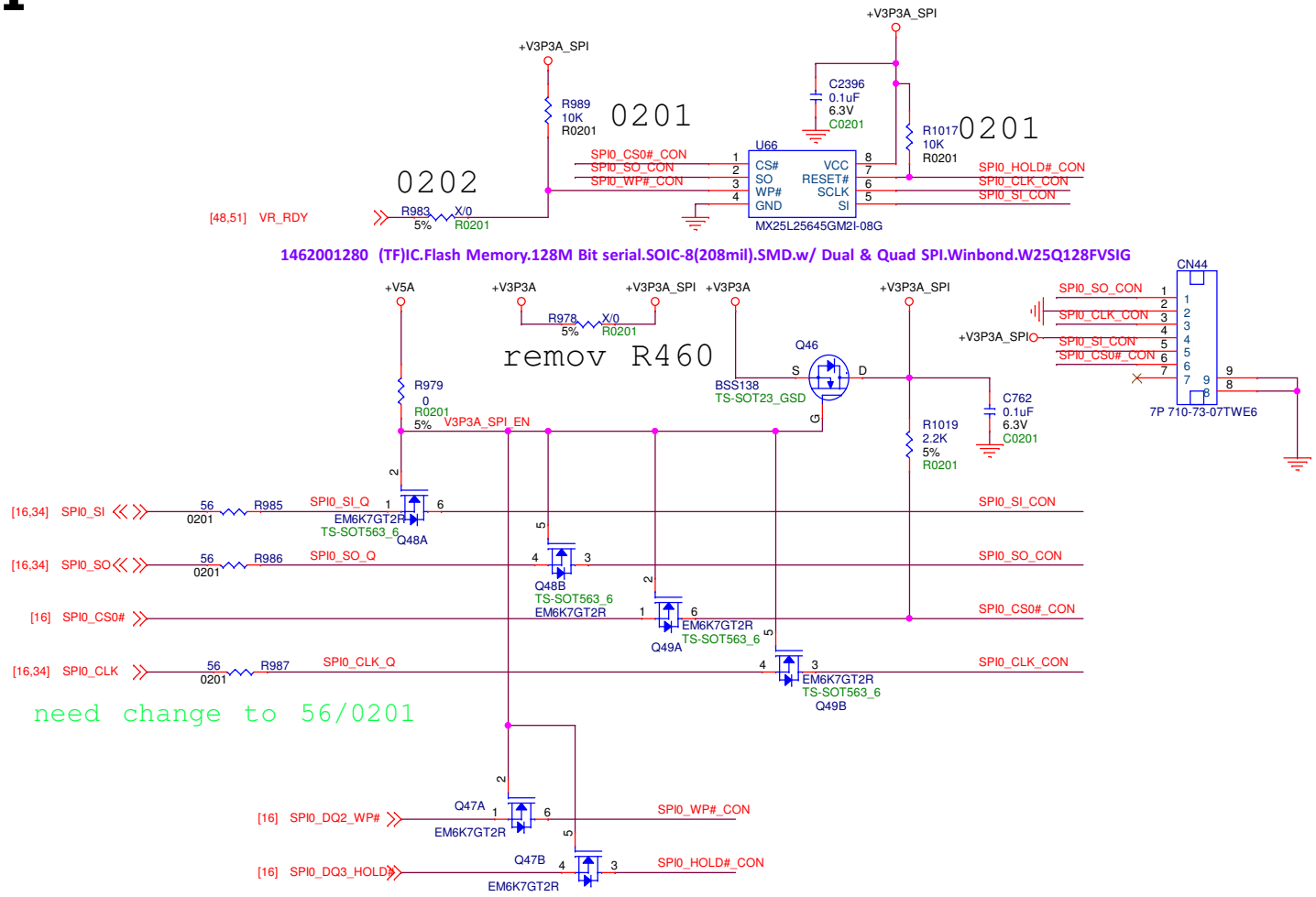
SPI



<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.	
	Title: FAN/BIOS/LPC	
	Size	Document Number: EPIC-TGH7 — Rev: A0.1_0_0
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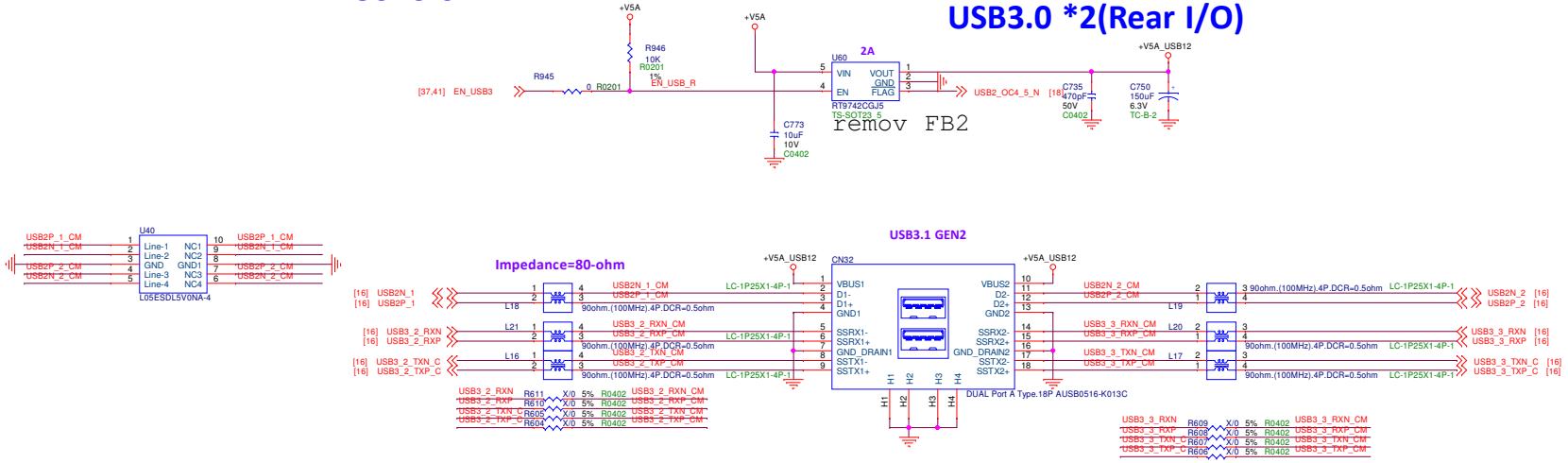
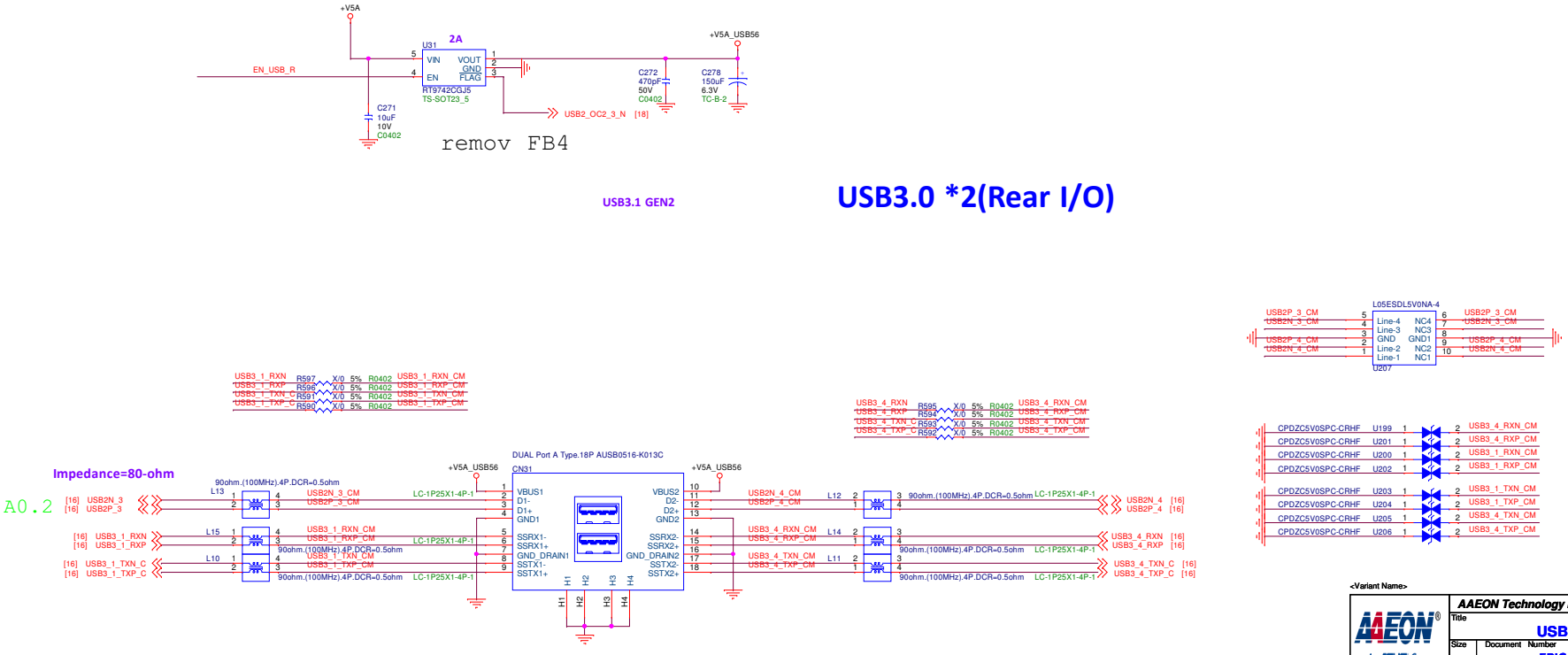
USB3.0

USB3.0 *2(Rear I/O)



USB3.0

USB3.0 *2(Rear I/O)



<Variant Name>

AAEON Technology INC.

Title	USB3.2 X 2	
Size	Document Number: EPIC-TGH7	Rev: A0.1_0_0
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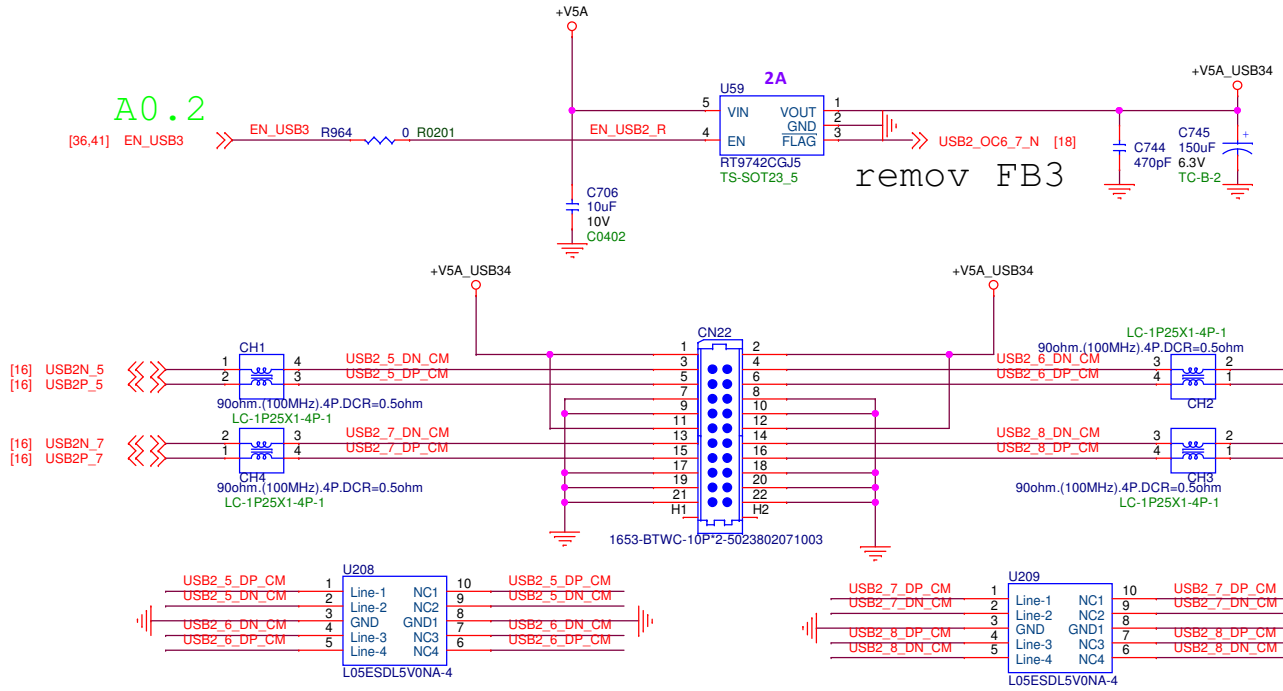

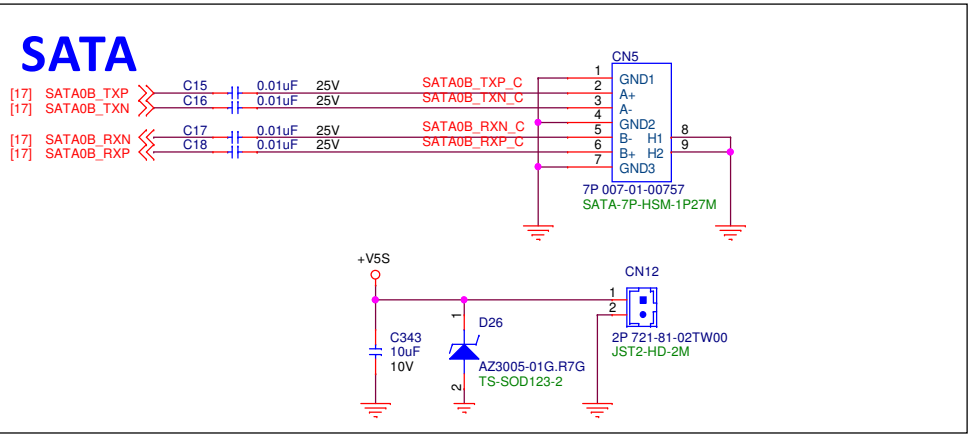

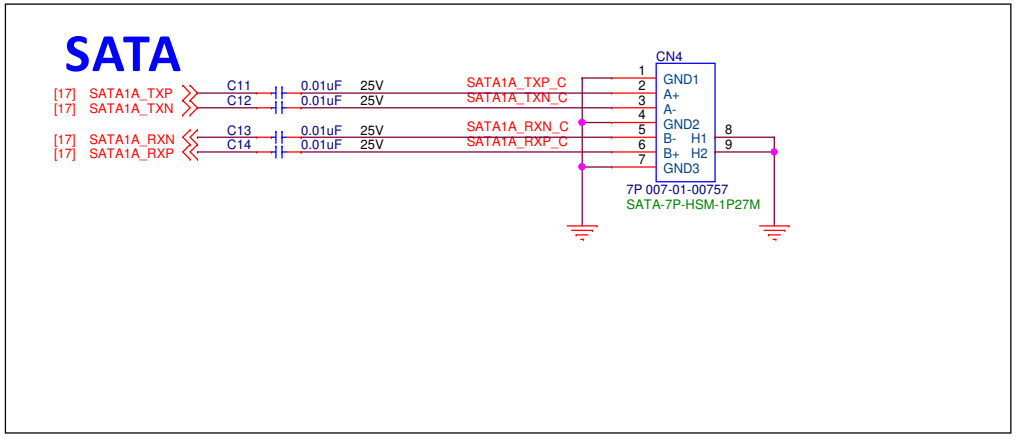

<Variant Name>

AAEON Technology INC.

Title: USB2.0 X 4/SATA X 2

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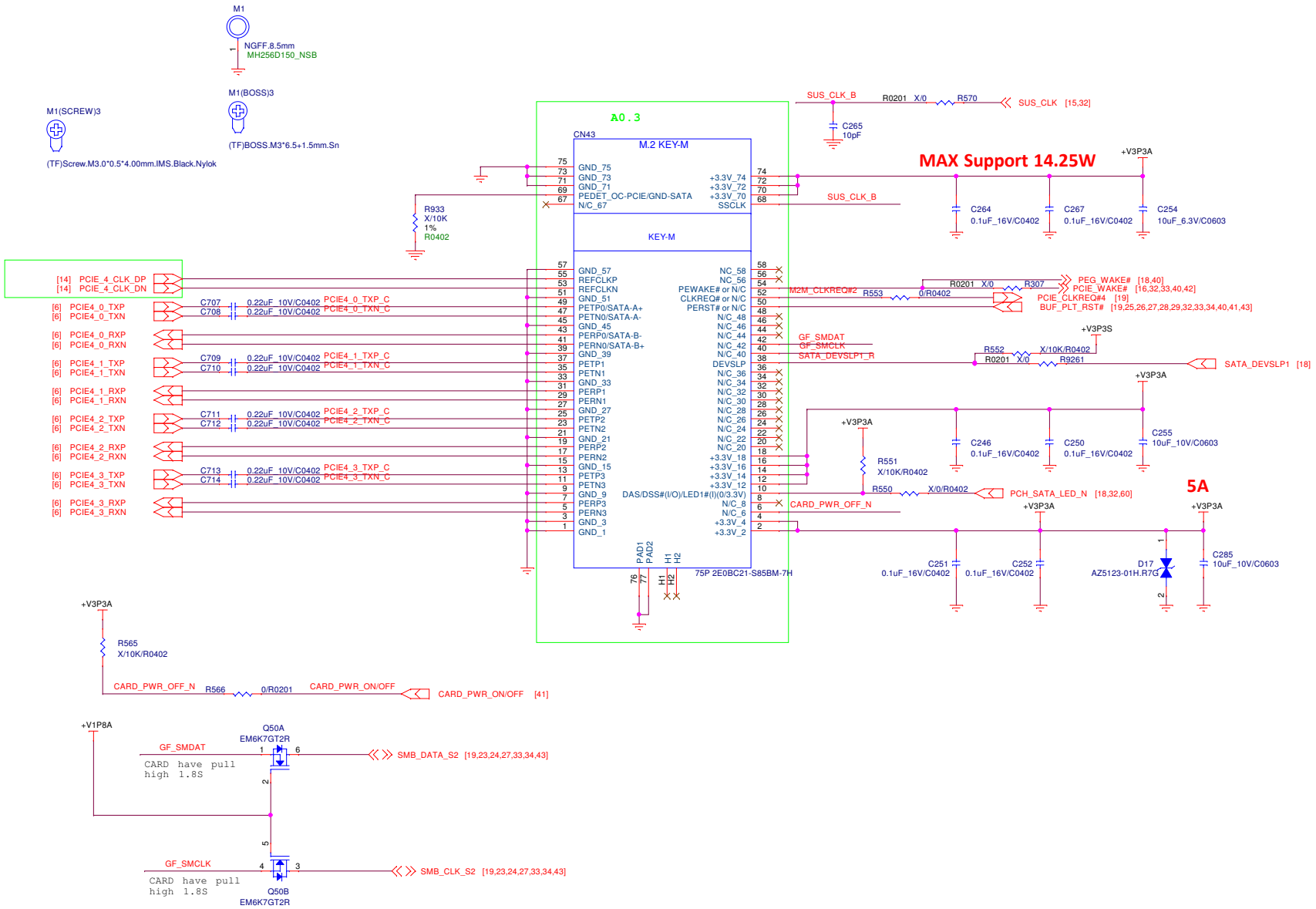
miniCard/mSATA(Full)



<Variant Name>

AAEON Technology INC.			
Title: M.2 M key2			
Size	Document Number: EPIC-TGH7		Rev: A0.1_0_0
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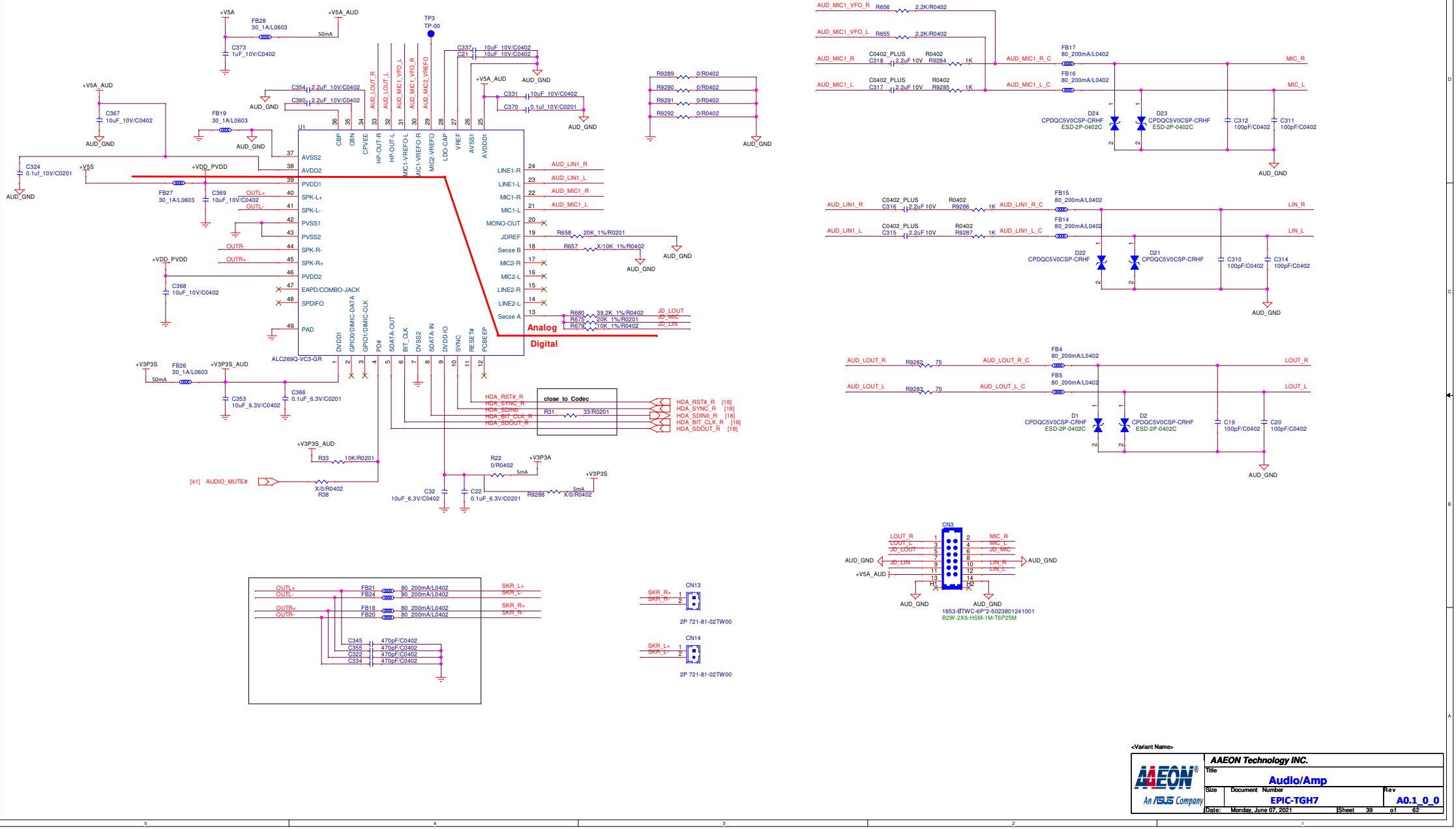

<variant_name>

AAEON Technology INC.

Title: Audio/Amp

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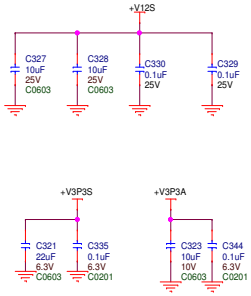
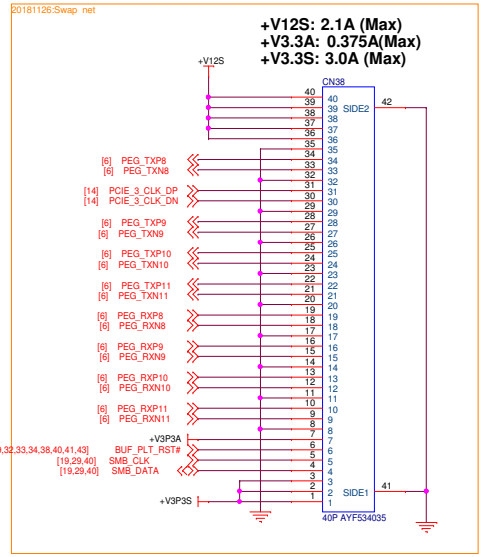
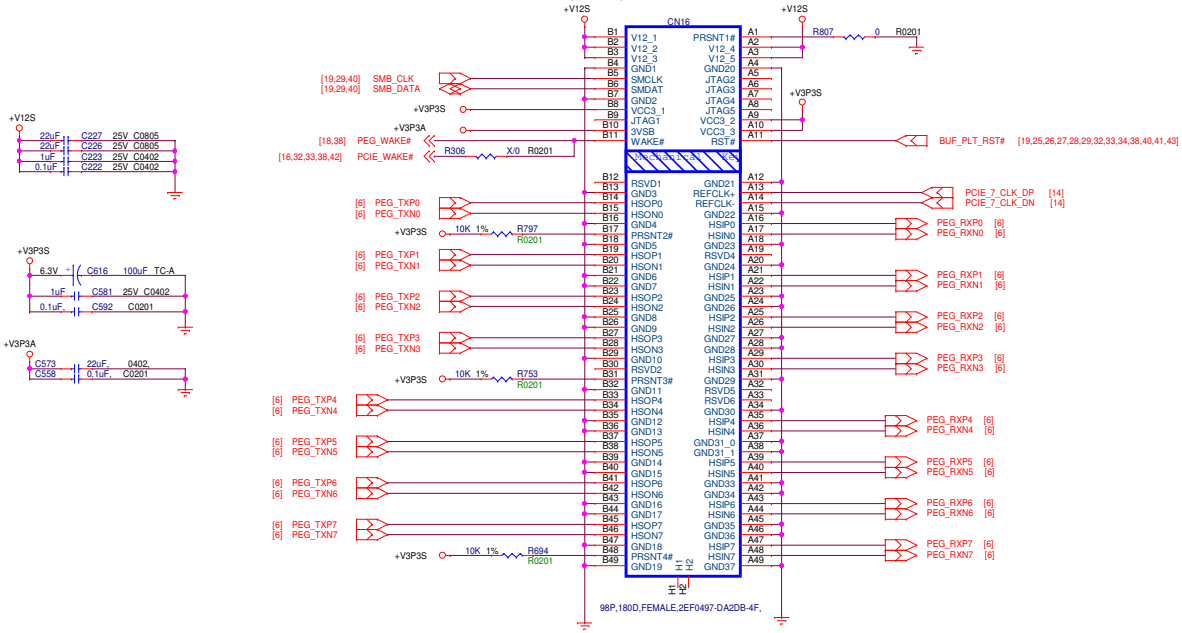




To FPC x4

+V12S: 2.1A (Max)
+V3P3A: 0.375A(Max)
+V3P3S: 3A (Max)



<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.		
	Title: PCIE X8		
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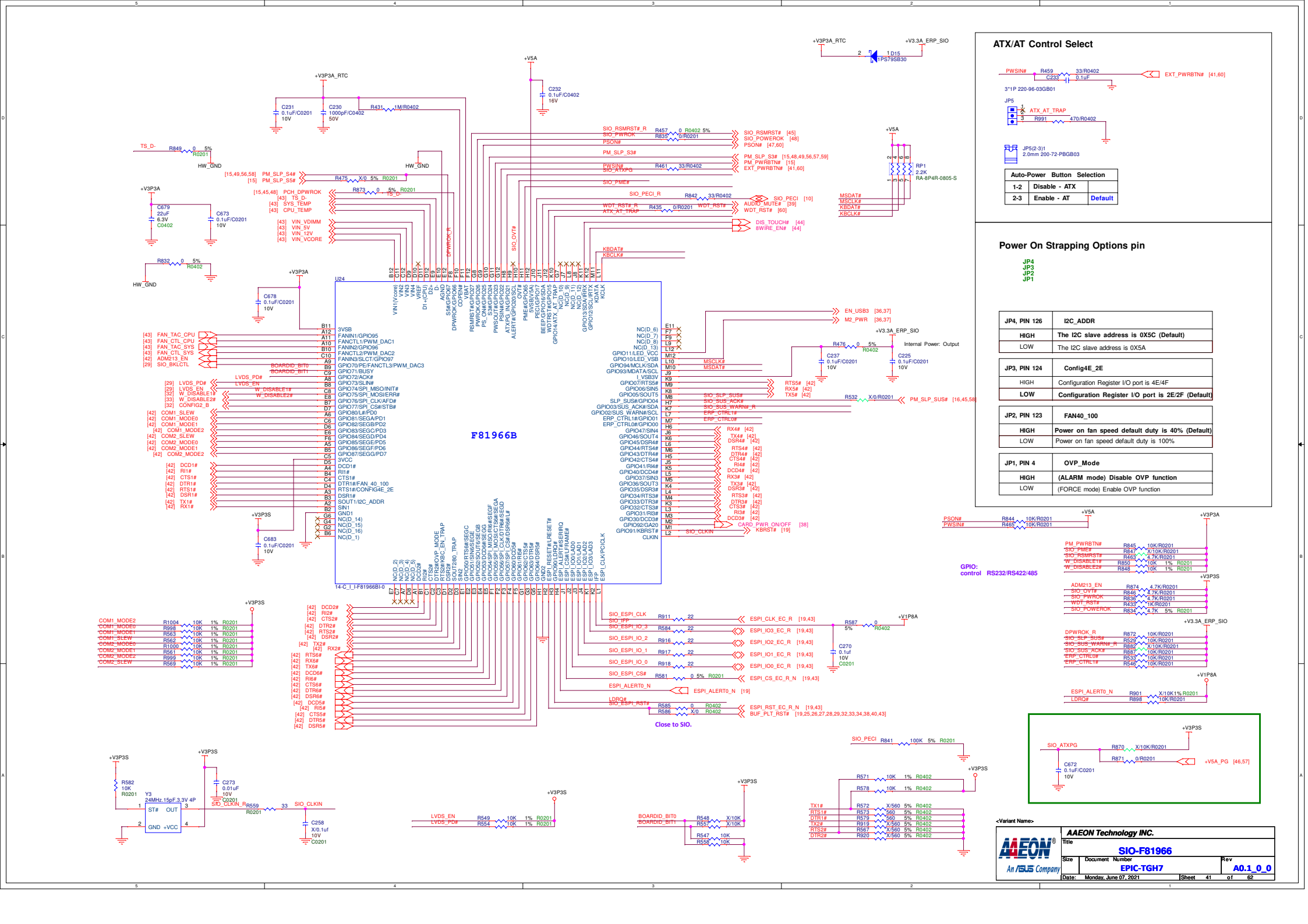
F81966B
14-C_I_I-F81966BI-0
U24
ATX/AT Control Select
PWSIN#
EXT_PWRBTN# [41,60]
JP5
ATX_AT_TRAP
JP5(2-3)1
2.0mm 200-72-PBGB03
Auto-Power Button Selection
1-2 Disable - ATX
2-3 Enable - AT Default
Power On Strapping Options pin
JP4
JP3
JP2
JP1
JP4, PIN 126 I2C_ADDR
HIGH The I2C slave address is 0X5C (Default)
LOW The I2C slave address is 0X5A
JP3, PIN 124 Config4E_2E
HIGH Configuration Register I/O port is 4E/4F
LOW Configuration Register I/O port is 2E/2F (Default)
JP2, PIN 123 FAN40_100
HIGH Power on fan speed default duty is 40% (Default)
LOW Power on fan speed default duty is 100%
JP1, PIN 4 OVP_Mode
HIGH (ALARM mode) Disable OVP function
LOW (FORCE mode) Enable OVP function
GPIO: control RS232/RS422/485
Close to SIO.
AAEON Technology INC.
SIO-F81966
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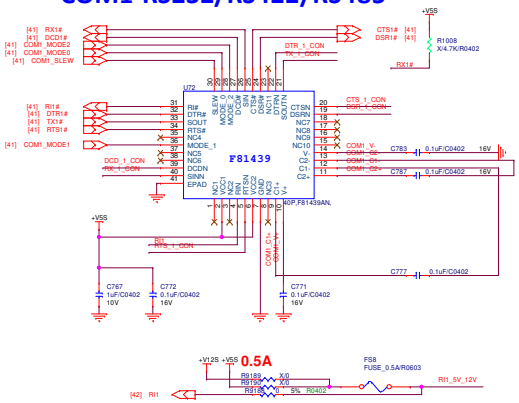
COM1

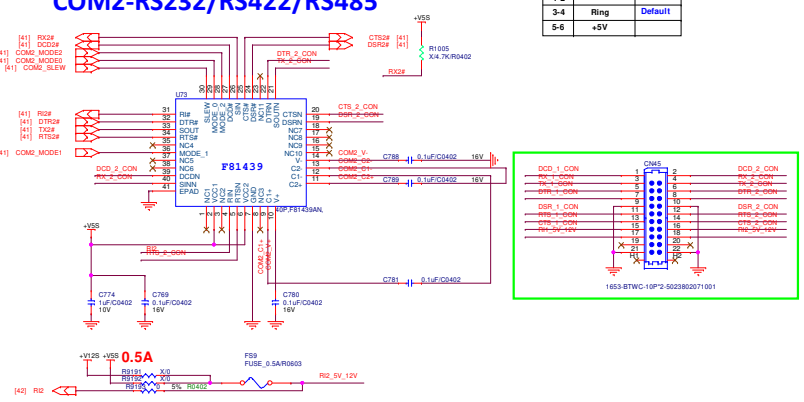
COM1-RS232/RS422/RS485



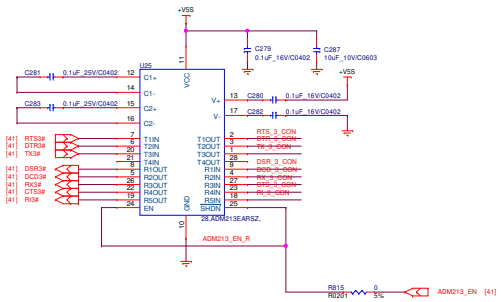
COM2

COM2-RS232/RS422/RS485

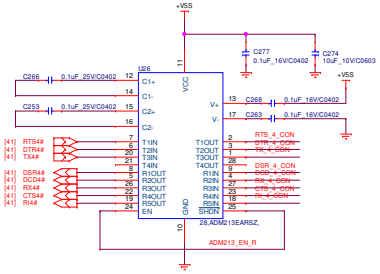
COM2 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	



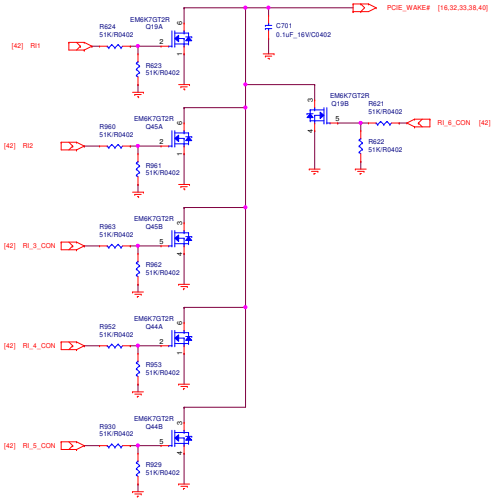
COM3



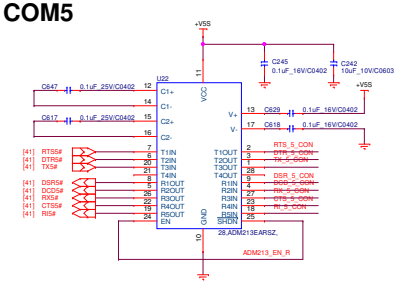
COM4



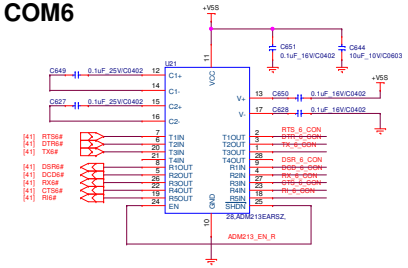
Wake On Modem

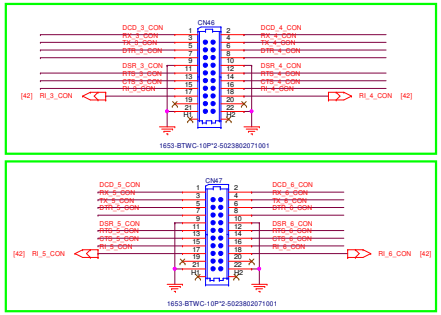


COM5



COM6





<Variant Name>

AAEON Technology INC.

COM X6

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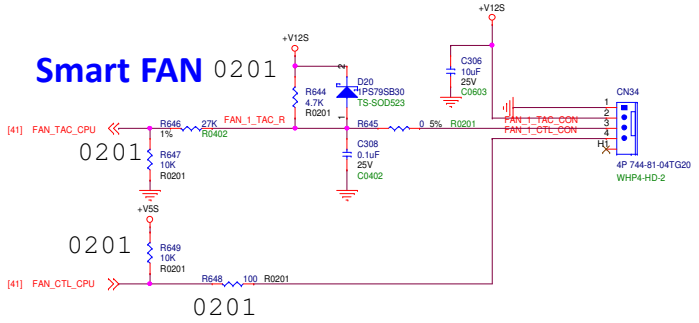
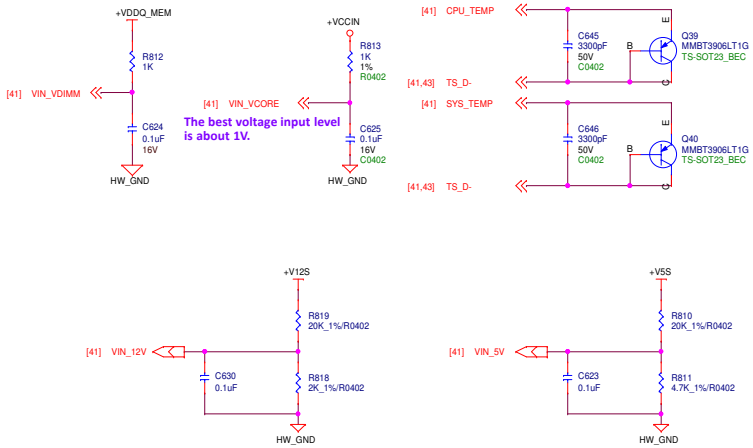
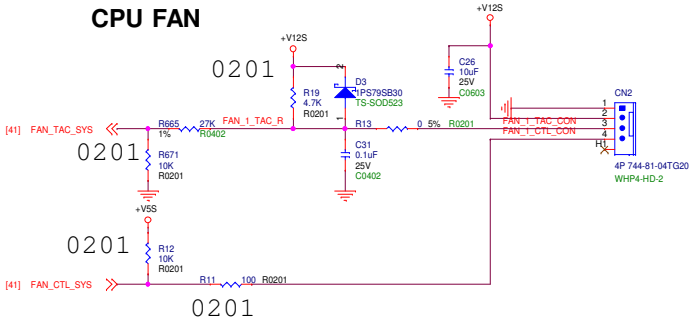
Smart FAN 0201



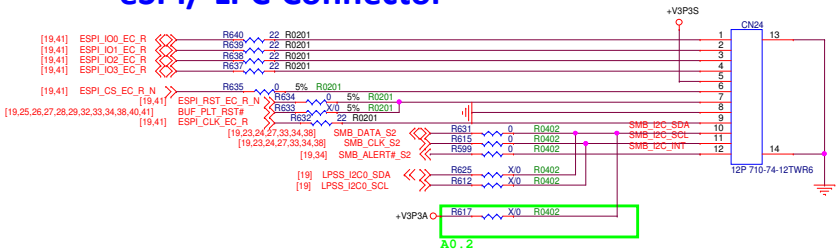
Voltage Monitor(Vcore, Vmem)



CPU FAN



eSPI/ LPC Connector



<Variant Name>

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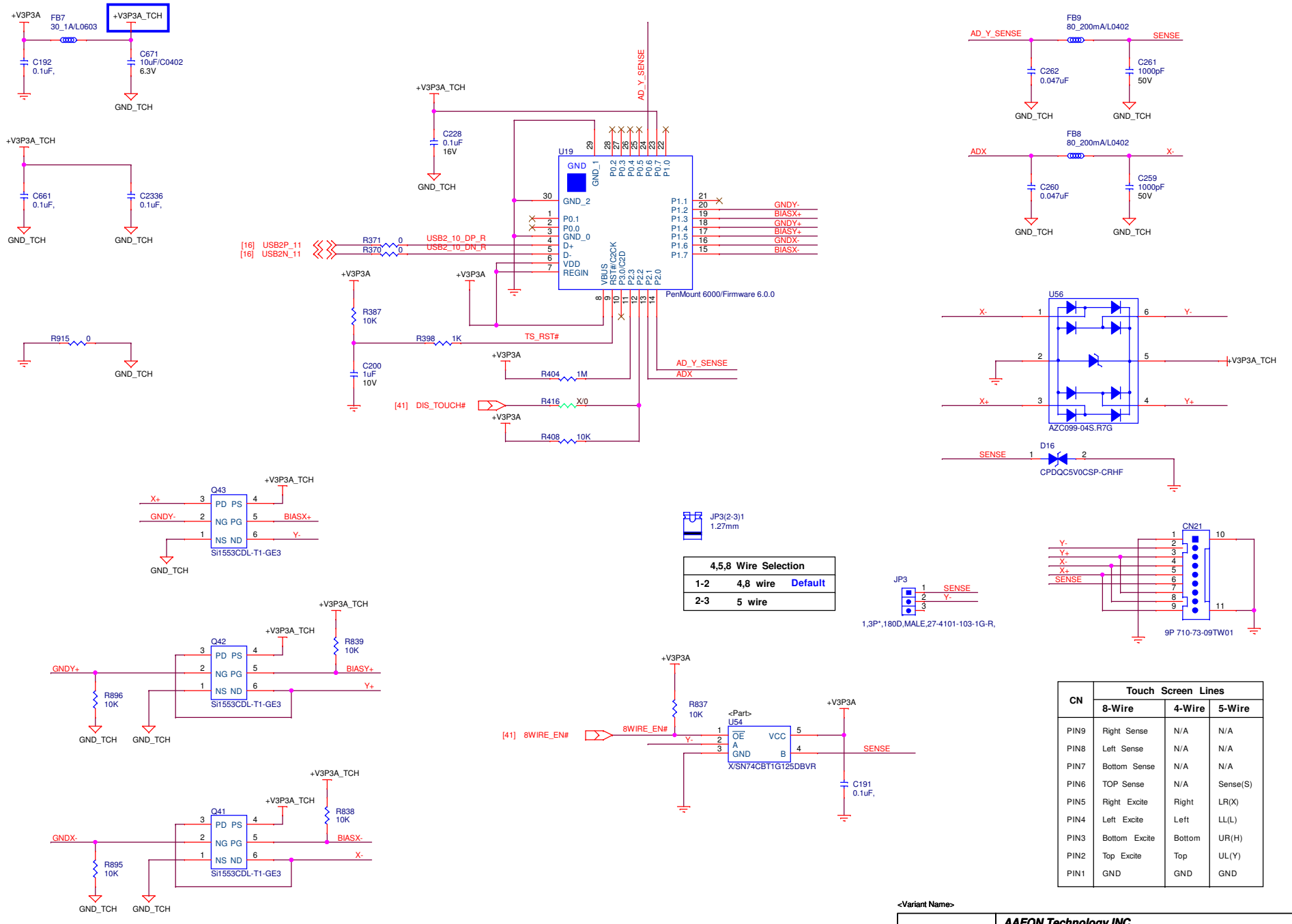

CN	Touch Screen Lines		
	8-Wire	4-Wire	5-Wire
PIN9	Right Sense	N/A	N/A
PIN8	Left Sense	N/A	N/A
PIN7	Bottom Sense	N/A	N/A
PIN6	TOP Sense	N/A	Sense(S)
PIN5	Right Excite	Right	LR(X)
PIN4	Left Excite	Left	LL(L)
PIN3	Bottom Excite	Bottom	UR(H)
PIN2	Top Excite	Top	UL(Y)
PIN1	GND	GND	GND

<Variant Name>

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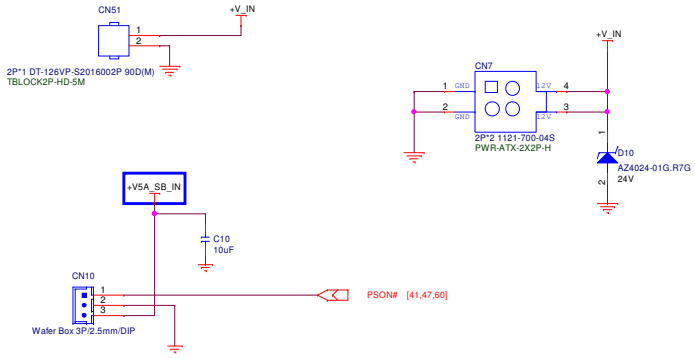
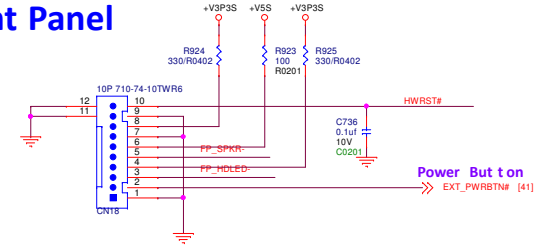
Power Input

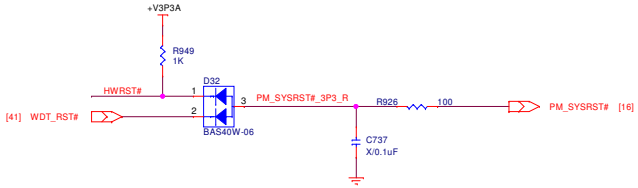
+9V~+36V



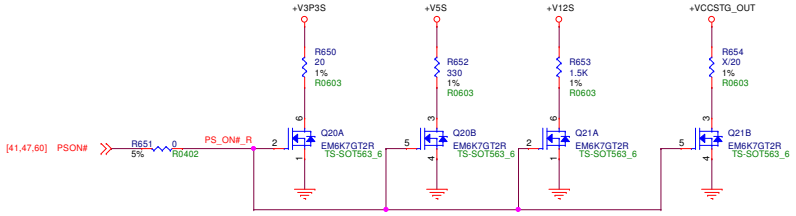
Front Panel



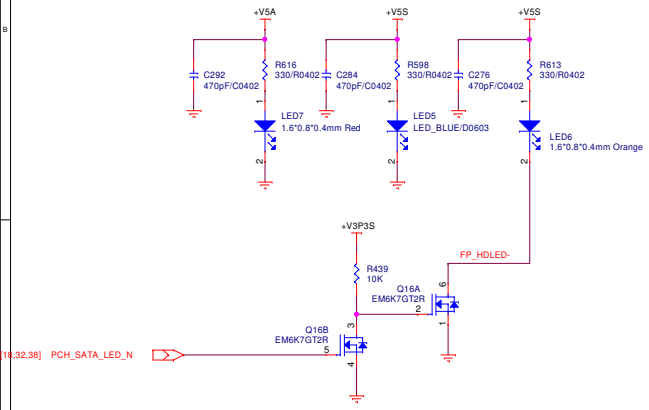
Reset Circuit



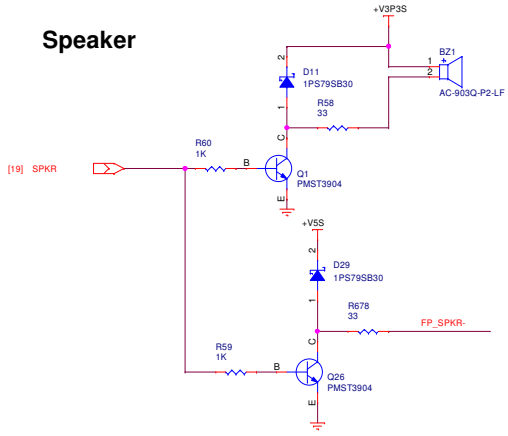
Discharge Circuit



LED



Speaker



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