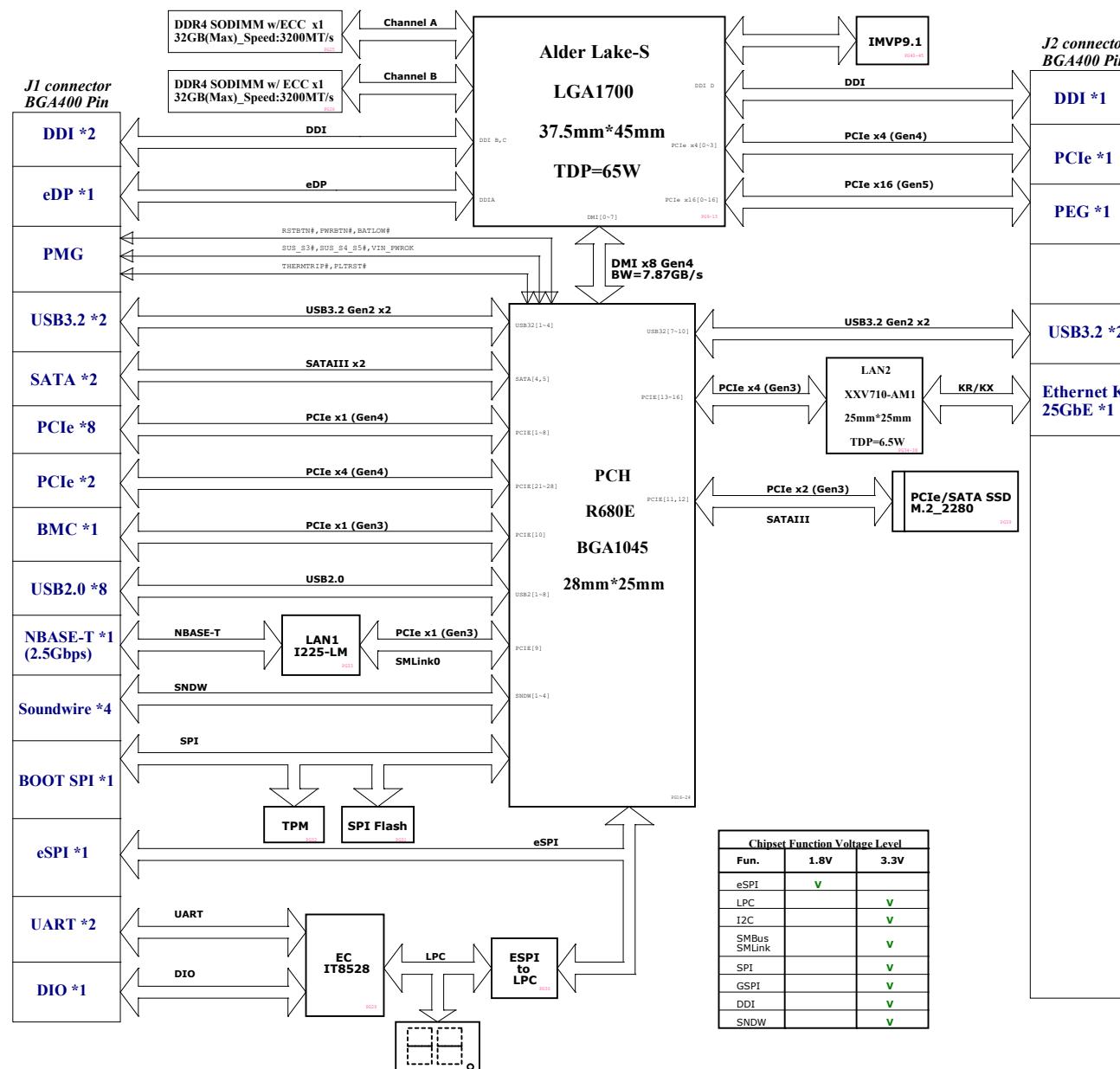
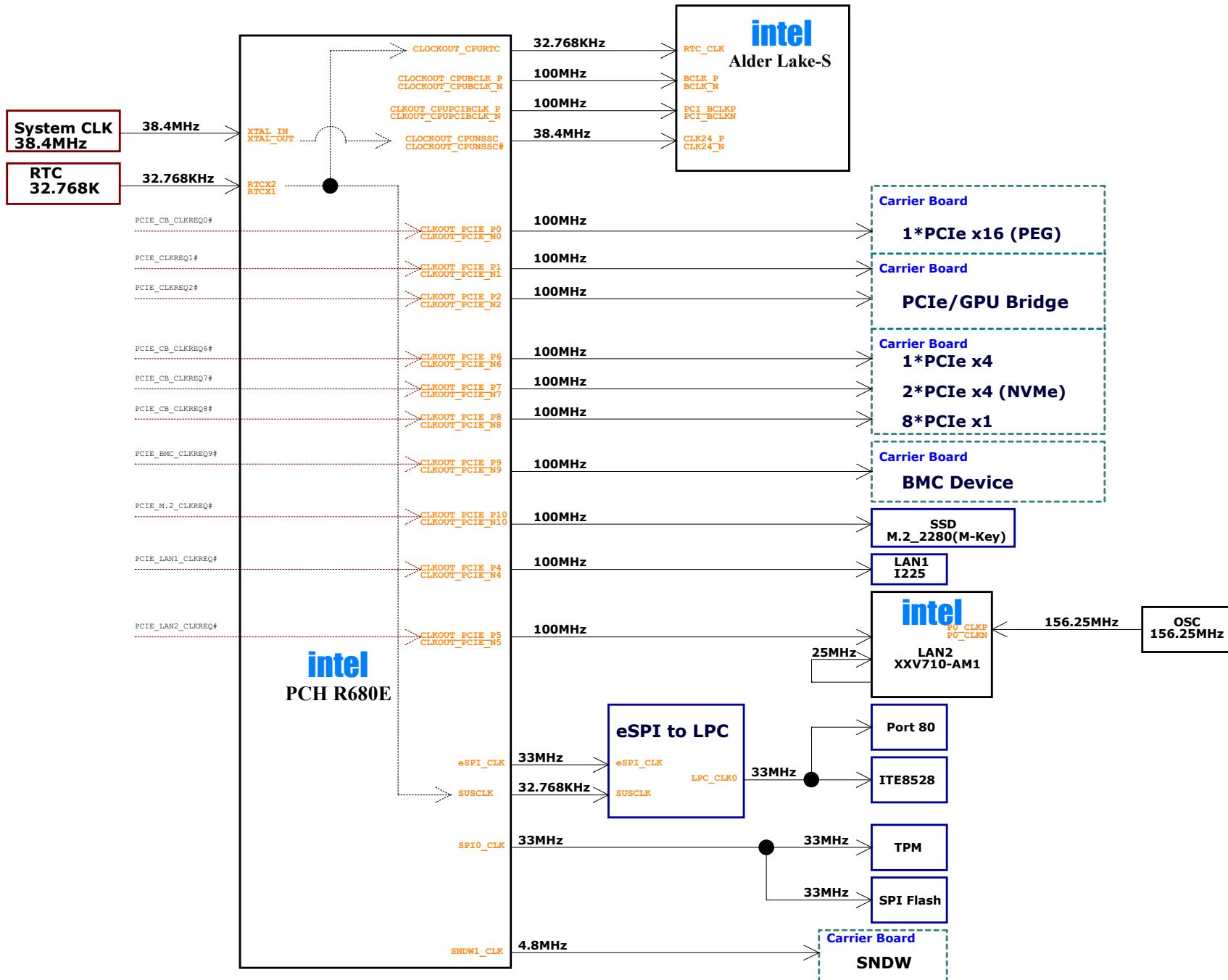


Project Name : HPC-ADSC
Project Code: E210809
Version: A0.2_0_0
Board Size:160mm*120mm



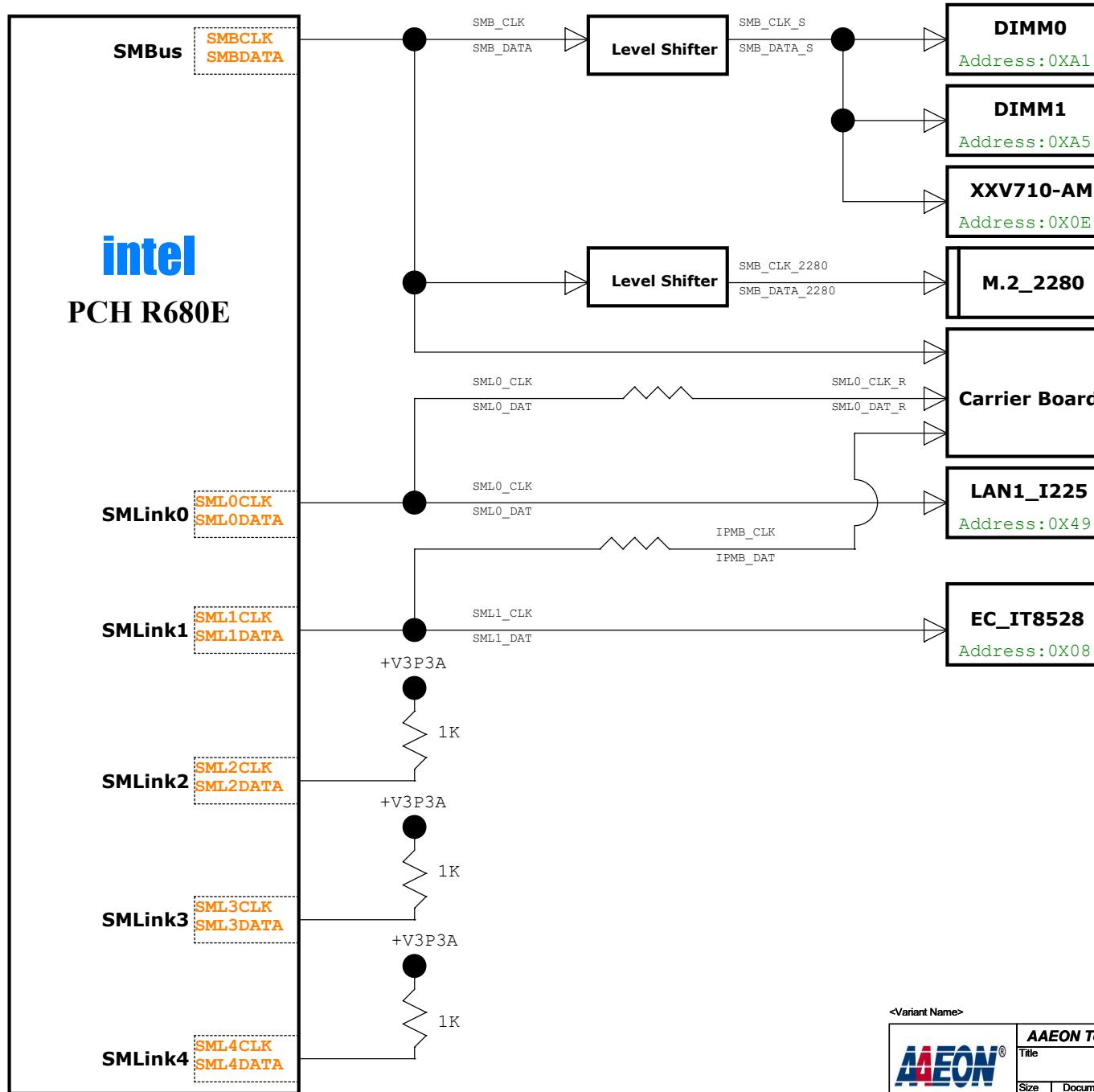
PAGE	TITLE
01	COVER SHEET
02	SYSTEM SETTING
03	CLK TREE
04	SMBus TREE
05	PCIe DELIVERY TREE
06	POWER DELIVERY TREE
07	POWER SEQUENCE_1
08	POWER SEQUENCE_2
09	PROCESSOR 1_DMI/PEG
10	PROCESSOR 2_DDI/EDP
11	PROCESSOR 3_DDR4
12	PROCESSOR 4_CLK/CFG/RSVD
13	PROCESSOR 5_POWER1
14	PROCESSOR 6_POWER2
15	PROCESSOR 7_VSS
16	PCH1_CLK
17	PCH2_DMI
18	PCH3_PCIE/SATA
19	PCH4_USB3.2/USB2
20	PCH5_I2C/SMLINK/UART/SMB
21	PCH6_CNNI/GSPI/SNDW/HDA
22	PCH7_SPI/JTAG/MISC/ESPI
23	PCH8_POWER
24	PCH9_VSS
25	DDR4_SODIMMA(Vertical)
26	DDR4_SODIMMB(Vertical)
27	COM-HPC_Row AB/CD
28	COM-HPC_Row EF/GH
29	EC_IT8528
30	eSPI to LPC
31	BIOS_SPI/eSPI SW
32	TPM2.0
33	LAN1_I225
34	XXV710_PCIE/JTAG/SDP/NCSI/SMB
35	XXV710_POWER
36	XXV710_GND
37	XXV710_I/O_CLK
38	XXV710_VR
39	M.2_2280_M-KEY
40	PWR_IMVP9.1
41	PWR_+VCCCORE_Phase1/2
42	PWR_+VCCCORE_Phase3/4
43	PWR_+VCCCORE_Phase5/6
44	PWR_+VCCGT
45	PWR_+VCCIN_AUX
46	PWR_+VDDQ/+VTT/+VPP
47	PWR_+VSA_DUAL
48	PWR_+V5IN/+V3P3A
49	PWR_+V1P8A_PROC/+V1P8A
50	PWR_+V1P05A_PROC/+V1P05A
51	PWR_+V0P82A
52	PWR_+VIN
53	SYSTEM POWER
54	BOOT SEQUENCE
55	RESET# LOGIC
56	DISCHARGE/LEDs/Port 80/Other BOM
57	Reference Doc
58	Revision History

CLK TREE



<Variant Name>		AAEON Technology INC.	
		CLK TREE	
Size	Document Number	Rev	A0.2.0.0
HPC-ADSC		Date: Wednesday, April 20, 2022	Sheet 3 of 58

SMBus TREE



<Variant Name>



AAEON Technology INC.

Title

SMBus TREE

Size

Document Number

Rev

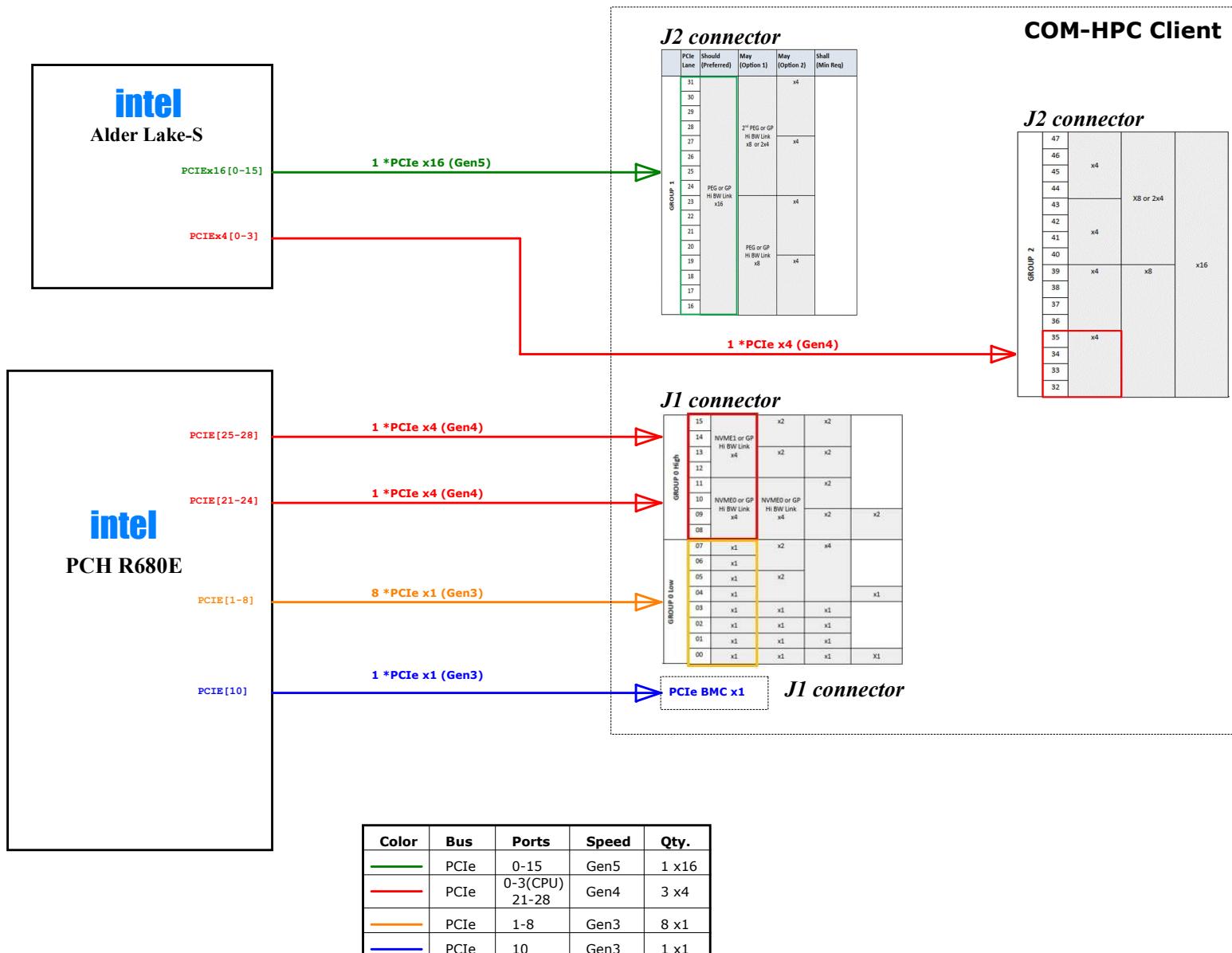
HPC-ADSC

A0.2_0_0

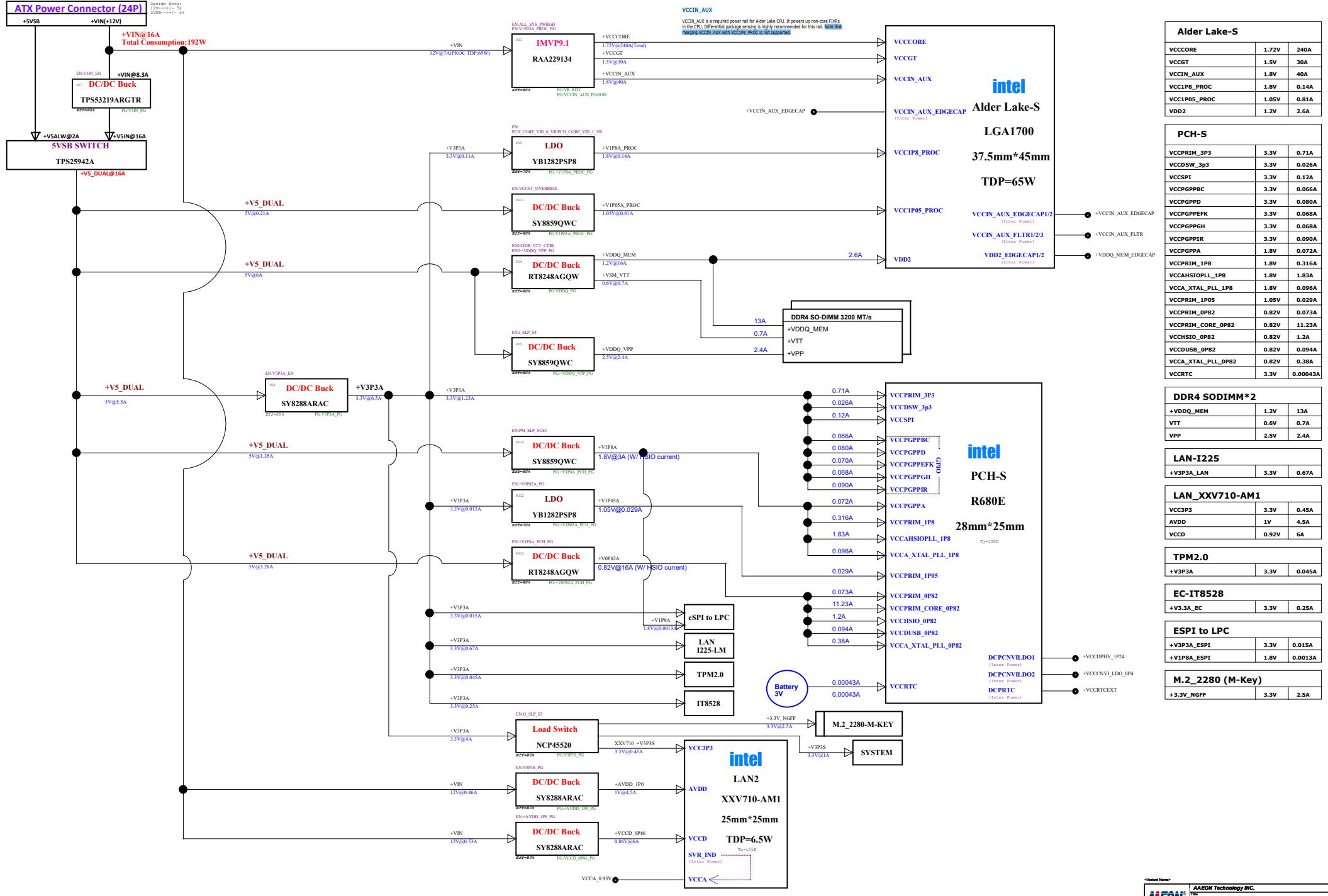
Date: Wednesday, April 20, 2022

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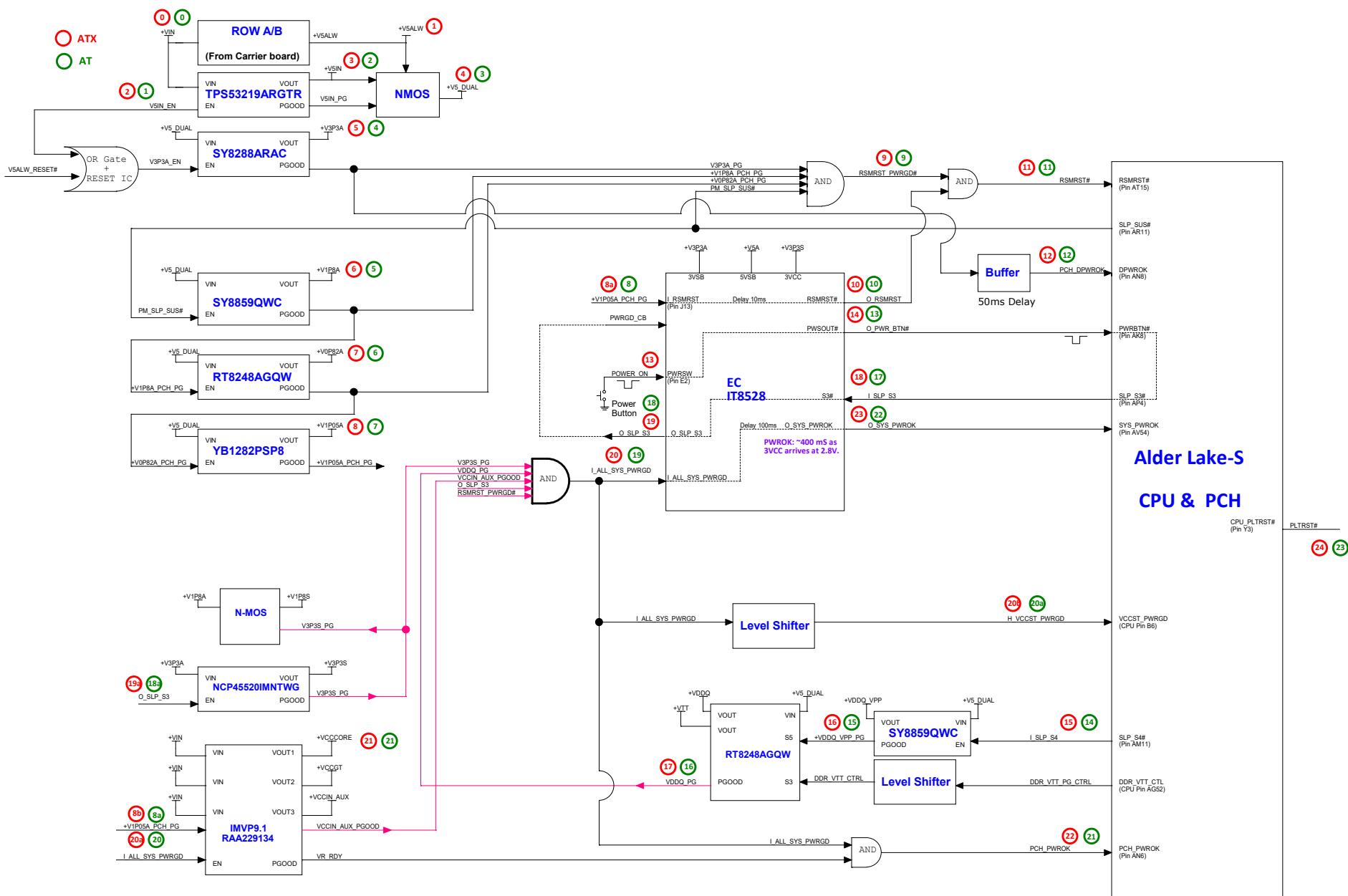
PCIe DELIVERY TREE



POWER DELIVERY TREE

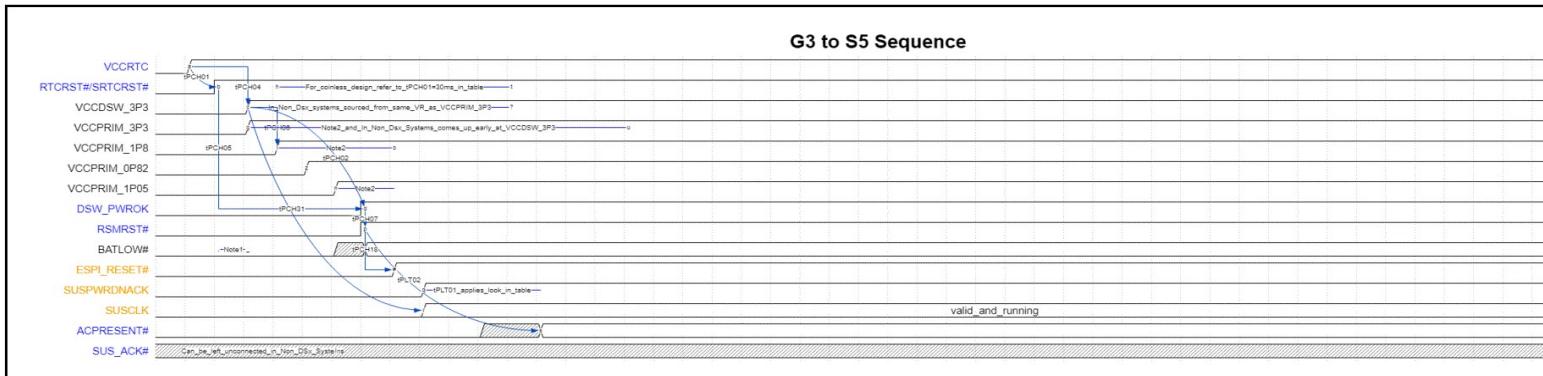


POWER SEQUENCE_1



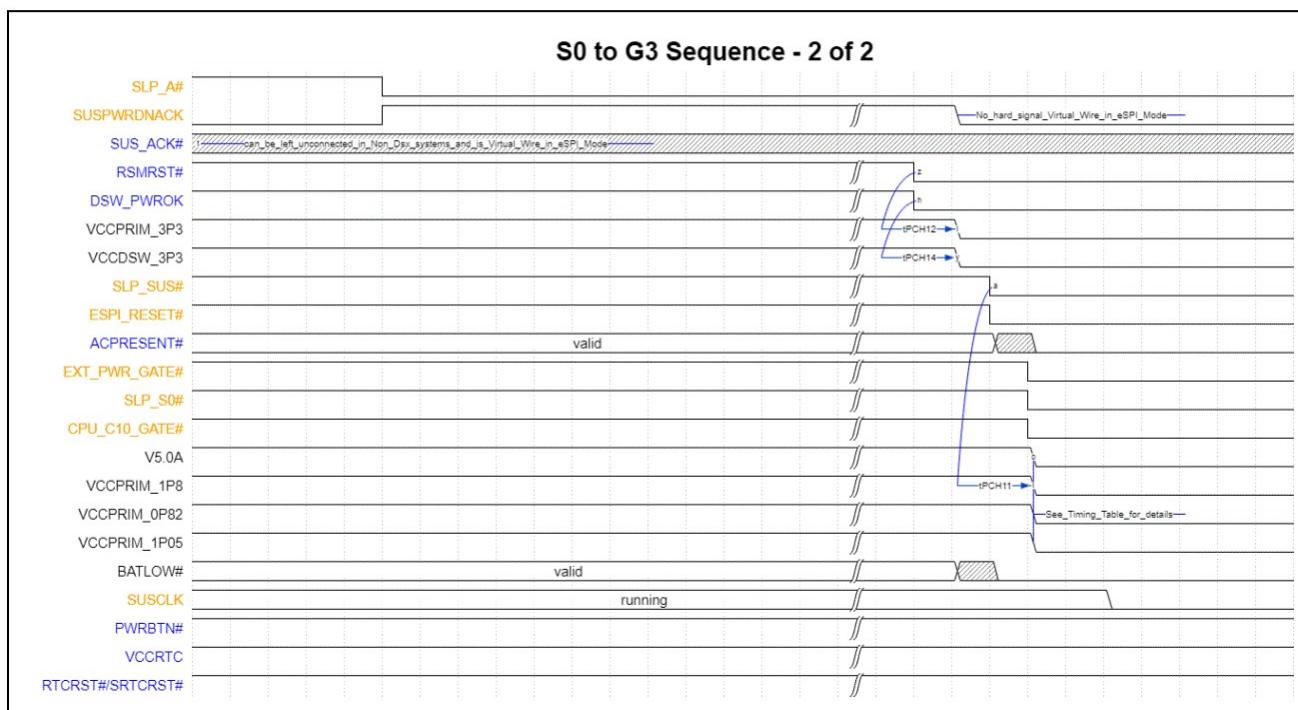
Variant Name		AAEON Technology INC.	
POWER SEQUENCE_1		Title	
Size	Document Number	Rev	Rev
HPC-ADSC			A0.2.0.0
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Timing Diagram for G3 to S5 [Non-Deep Sx Platform]



Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]

For S0 to G3 Sequence 1 of 2 Refer to DSx Sequence



PROCESSOR 1_DMI/PEG

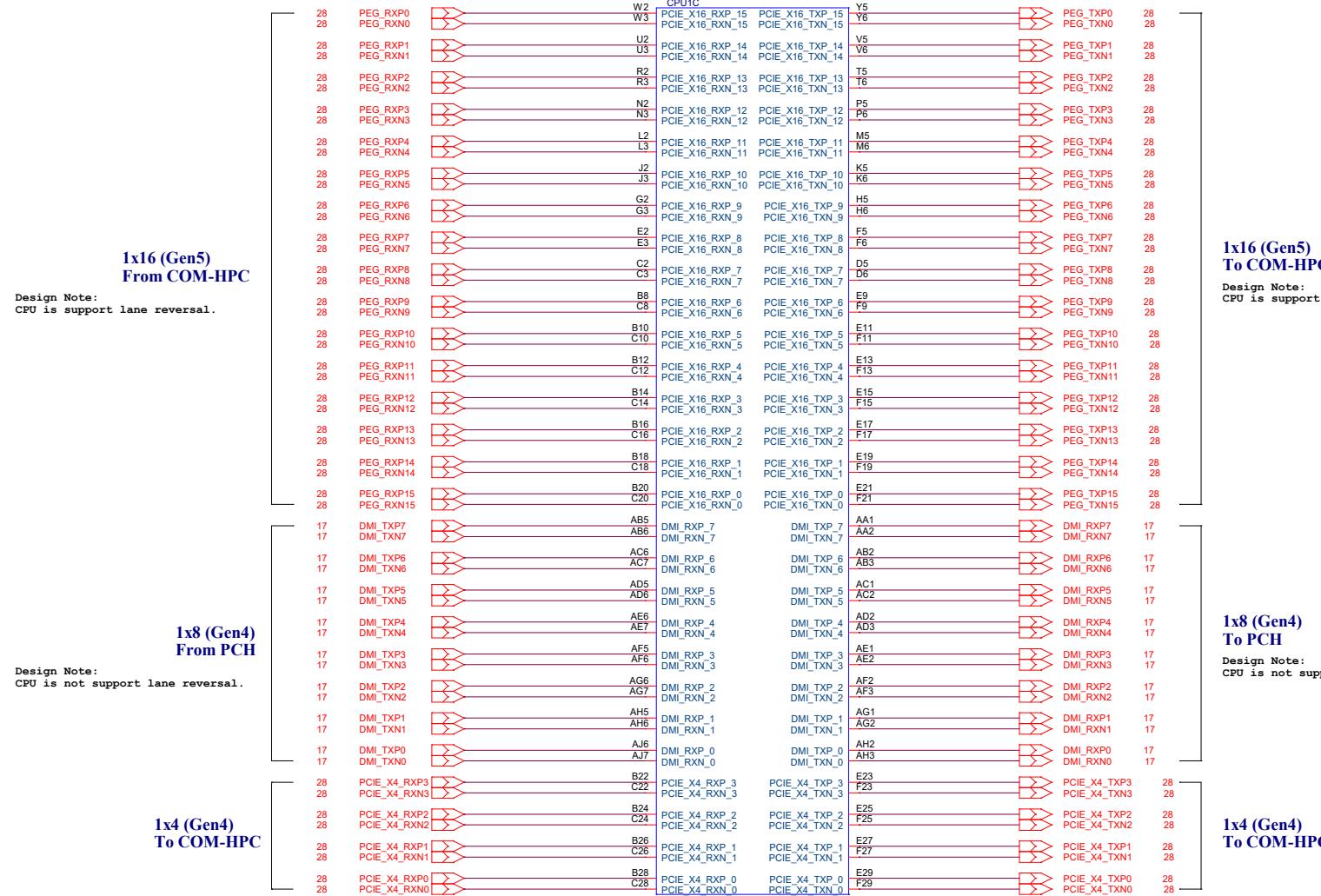


Table 50. PCI Express® 16 - Lane Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width		CFG Signals			Lanes															
	0:1:0	0:1:1	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe controller																					
1x16	x16	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Processor to PCH DMI Lane Connections

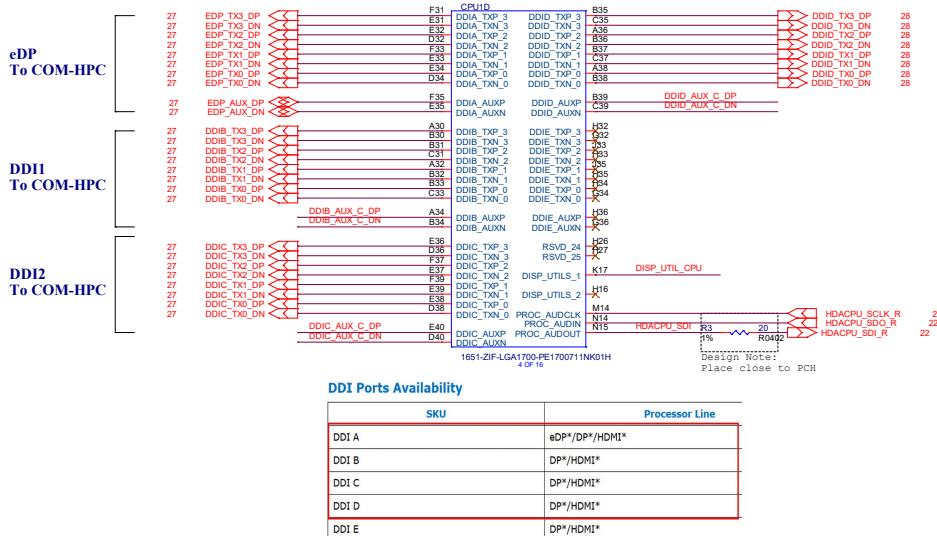
Link Width	Component	Lane Reversal	DMI Package Pin Lane Connections							
			0	1	2	3	4	5	6	7
x8	Processor	No	0	1	2	3	4	5	6	7
x8	PCH	No	0	1	2	3	4	5	6	7
x8	Processor	No	0	1	2	3	4	5	6	7
x8	PCH	Yes	7	6	5	4	3	2	1	0

Notes: • NC = No Connect
• PCH DMI Controller supports x8 static end-to-end Lane Reversal on its Lanes [7:0]
• Processor DMI Controller does not supports static end-to-end Lane Reversal on its Logical Lanes

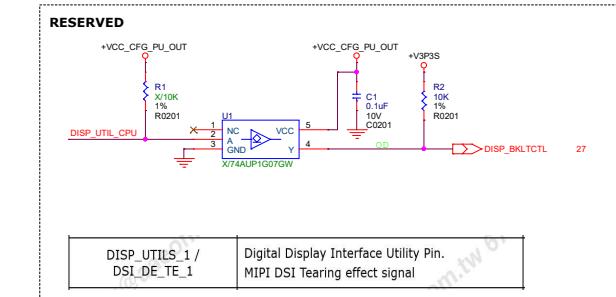
<Variant Name>

AEON An ASUS Company	AAEON Technology INC.	
	Title	
	PROCESSOR 1_DMI/PEG	
Size	Document Number	Rev
	HPC-ADSC	A0.2_0_0
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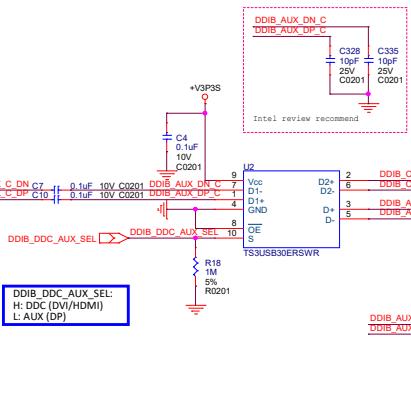
PROCESSOR 2_DDI/EDP



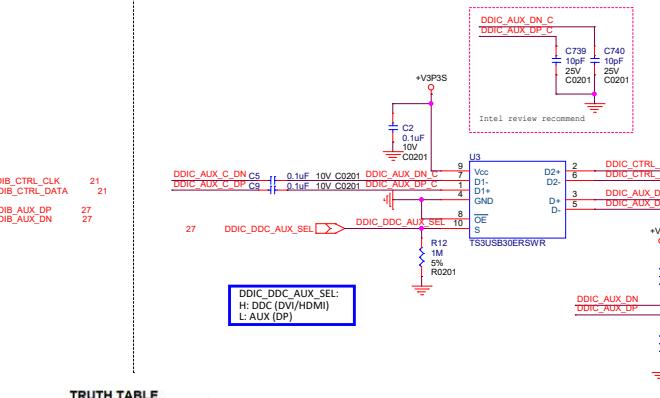
DDI3
To COM-HPC



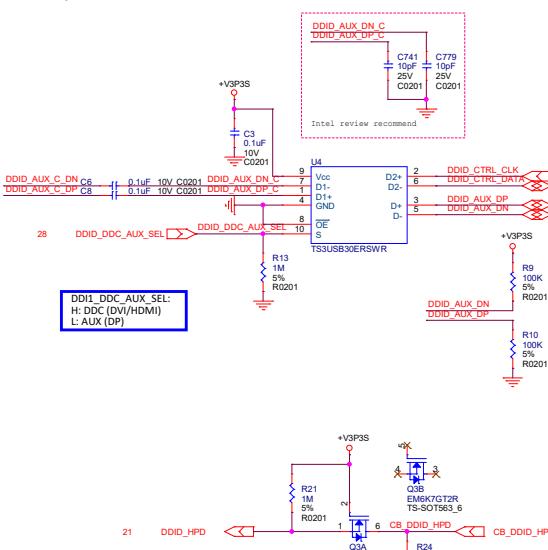
DDI1 / AUX Switch



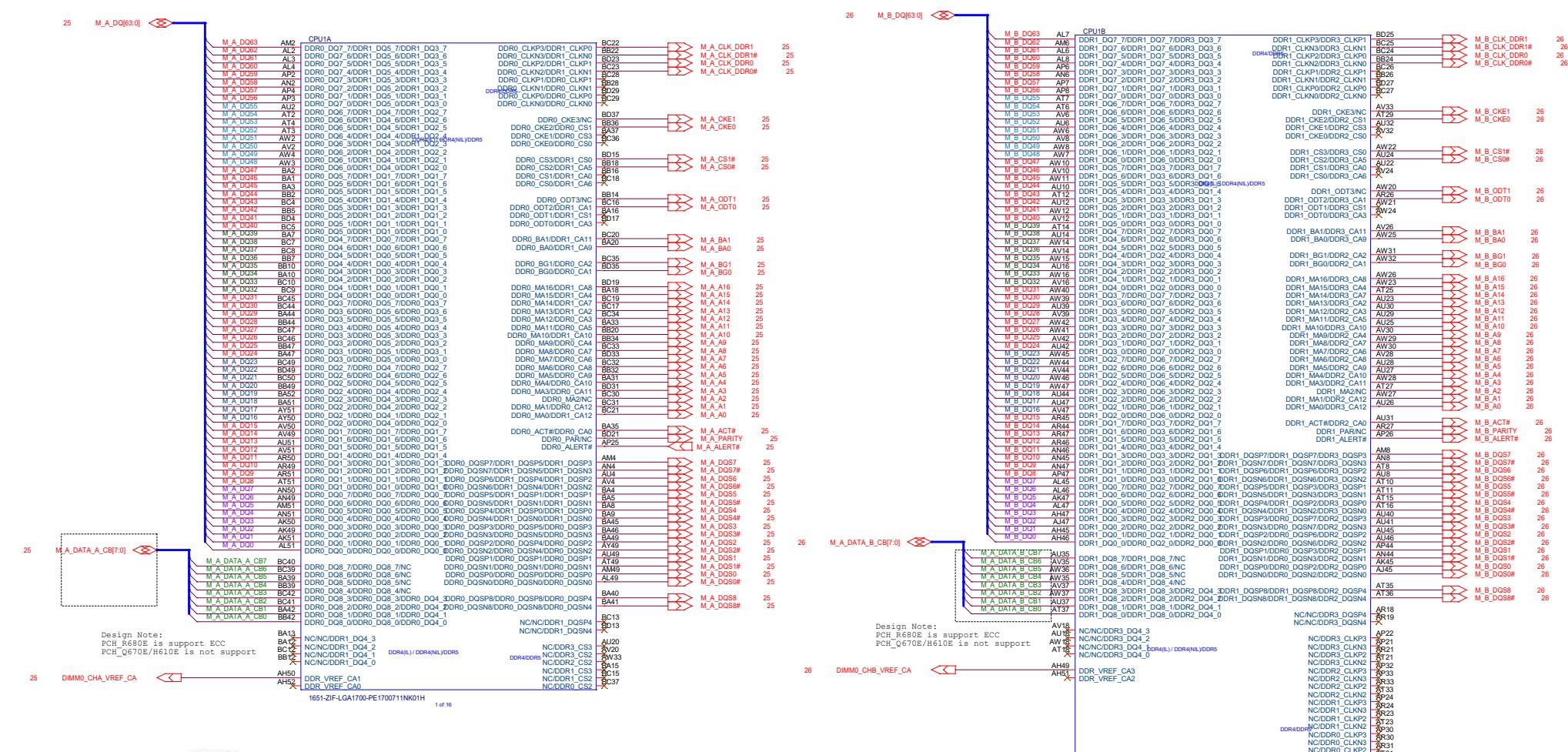
DDI2 / AUX Switch



DDI3 / AUX Switch



PROCESSOR 3_DDR4



NOTE

For DDR4 1DPC SODIMM configuration please follow the RVP design, where:

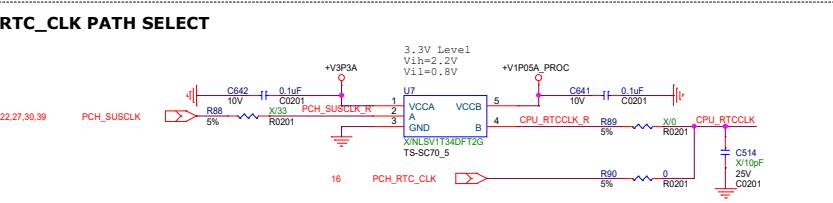
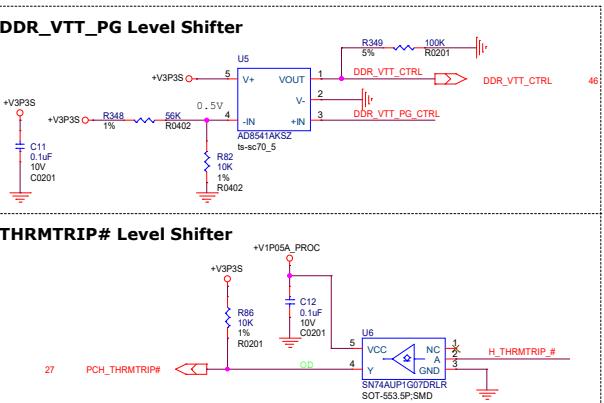
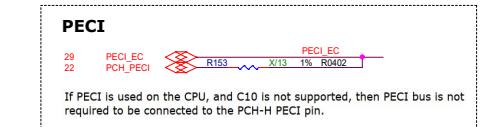
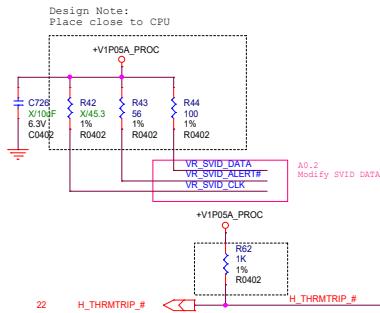
- CHA DIMM used rank 2/3 signals, and thus used Vref1
- ChB DIMM used rank 2/3 signals, and thus used Vref3

DDR Byte Swapping

- DDR4 - Byte swapping is allowed within each x64 channel.
- ECC bits swap is allowed within DDR4 ECC[7..0].

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AEON Technology INC.		PROCESSOR 3_DDR4	
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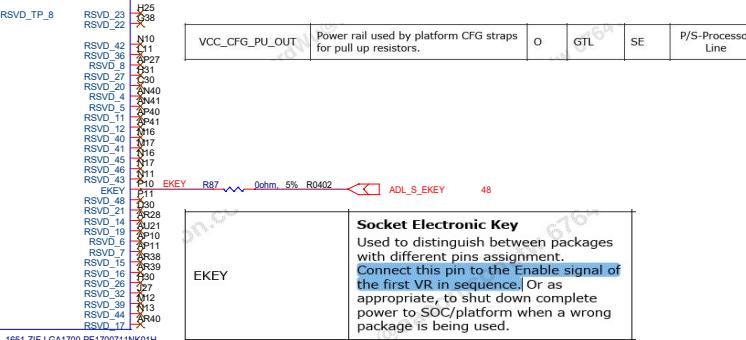
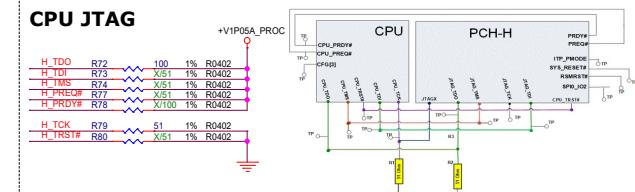
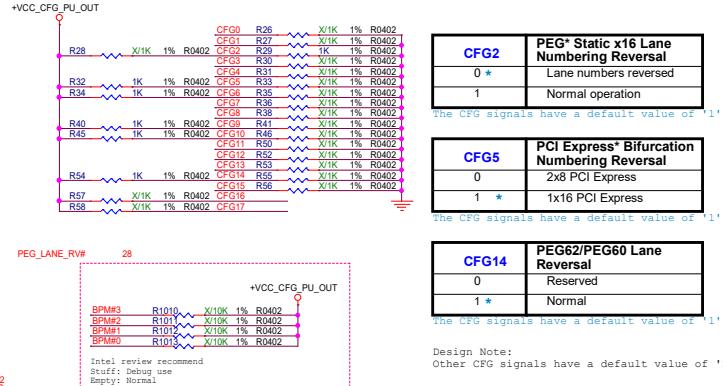
PROCESSOR 4_CLK/CFG/RSVD



Ground and Reserved Signals

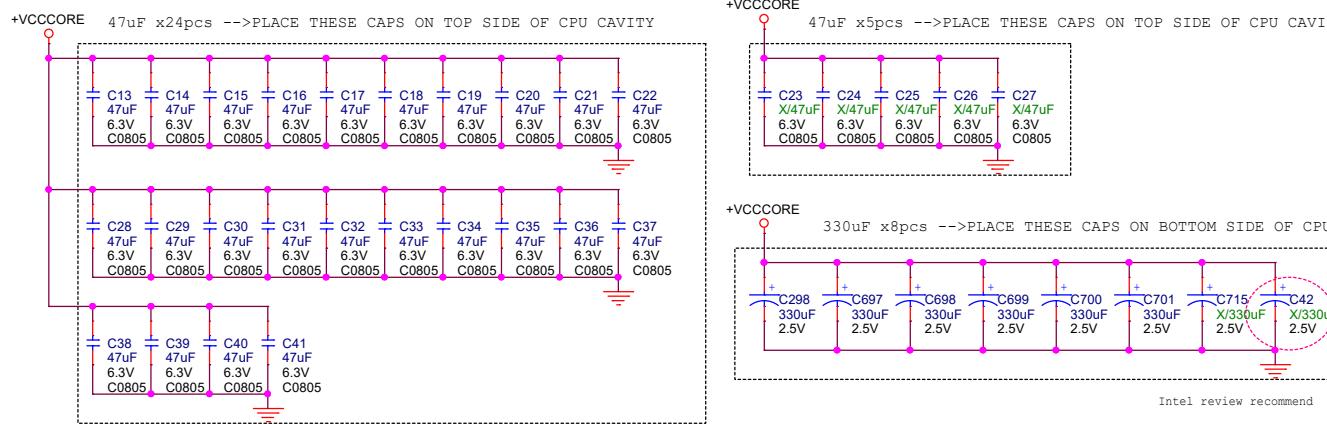
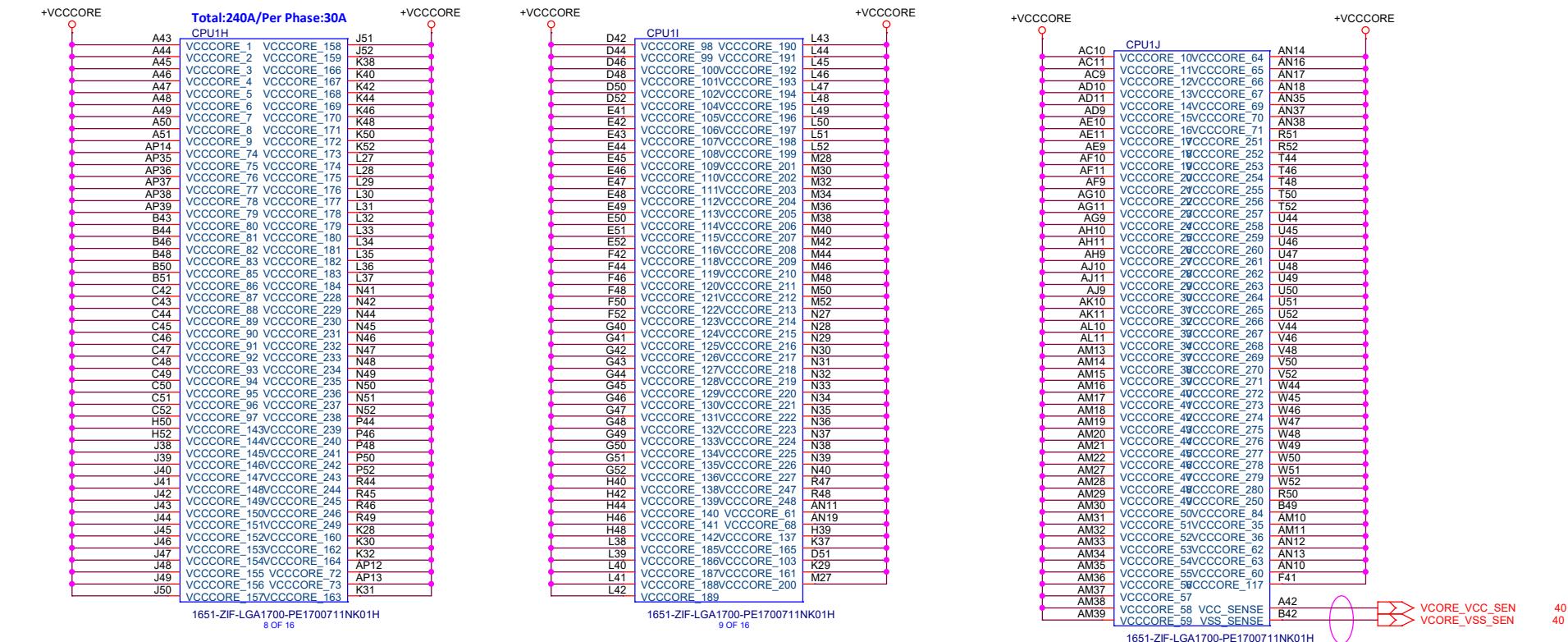
The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- _NCTF – these signals are non-critical to function and should not be connected.



<Variant Name>	
AEON®	AEON Technology INC.
Document Number	Title
HPC-ADSC	PROCESSOR 4_CLK/CFG/RSVD
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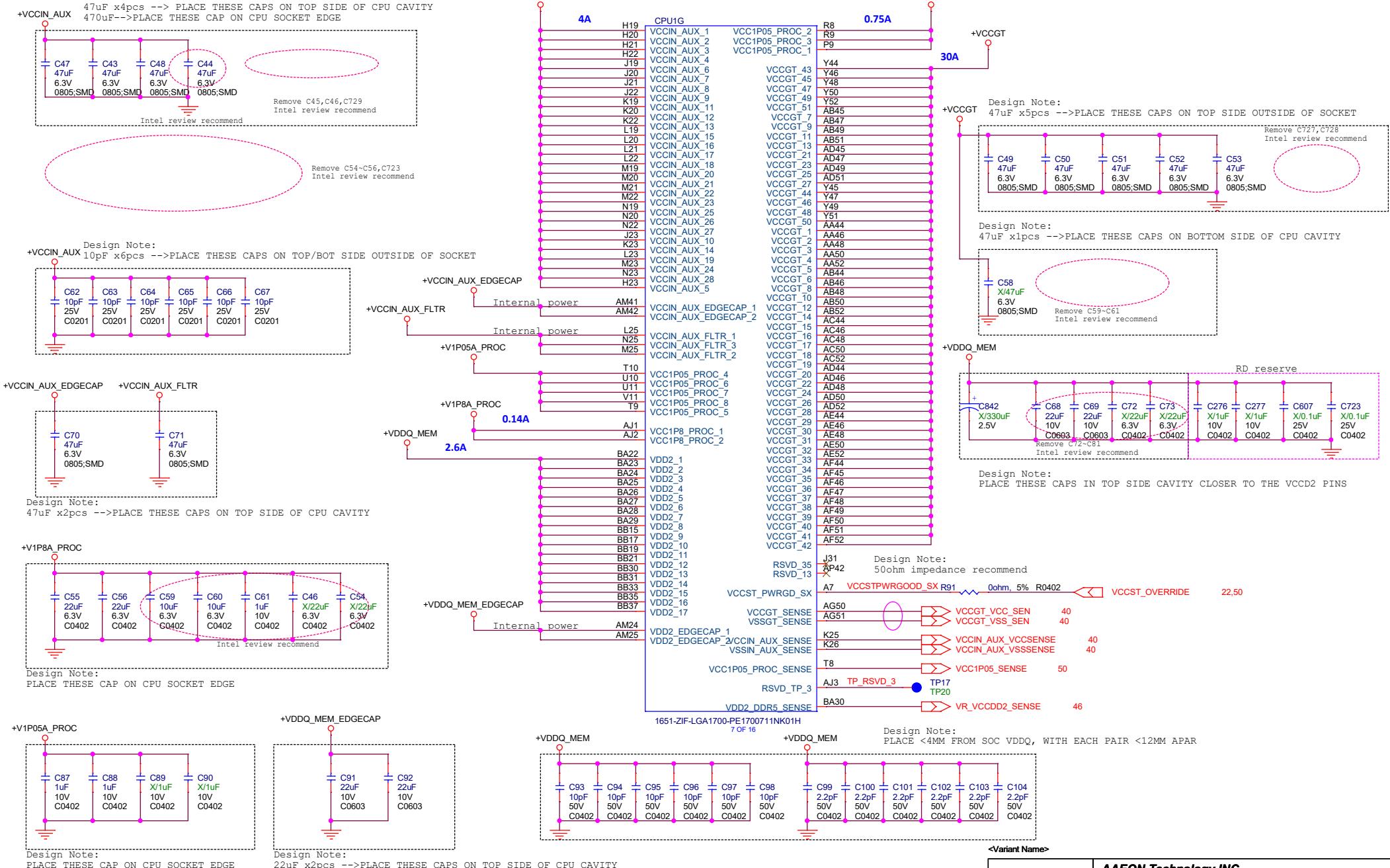
PROCESSOR 5_POWR1



PROCESSOR 5_POWR1

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PROCESSOR 6_POWR2



AAEON Technology INC.

Title

PROCESSOR 6_POWR2

Size Document Number

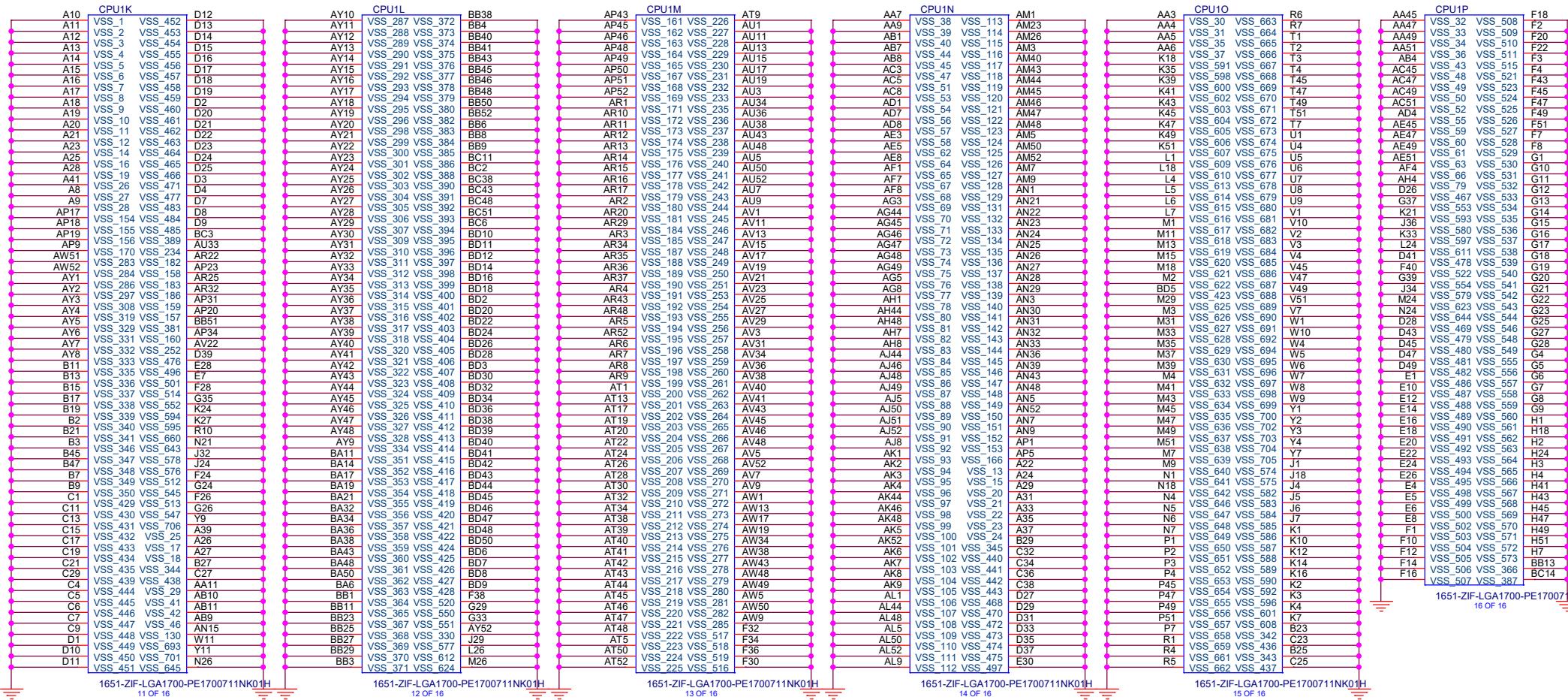
HPC-ADSC

Rev A0.2_0_0

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PROCESSOR 7-VSS



<Variant Name>



AAEON Technology INC.

Title: PROCESSOR 7_VSS

Size Document Number Rev

HPC-ADSC

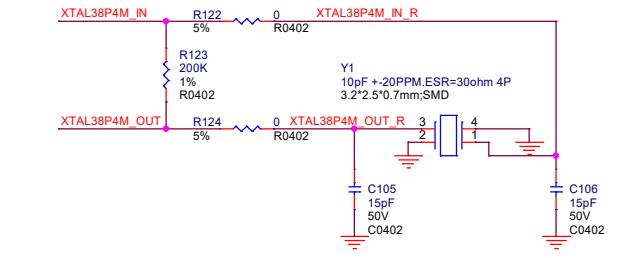
A0.2_0_0

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PCH1_CLK



XTAL-38.4MHz



Signal Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[17:0] CLKOUT_PCIE_N[17:0]	O	Yes	PCI Express® Clock Output: Serial Reference 100 MHz PCIe® specification compliant differential output clocks to PCIe® devices <ul style="list-style-type: none"> CLKOUT_PCIE_P/N[3:0] can be used for PCIe Gen5 support. CLKOUT_PCIE_P/N[17:4] can be used for PCIe Gen4 support.

<Variant Name>



AAON Technology INC.

Title

PCH1_CLK

Size Document Number

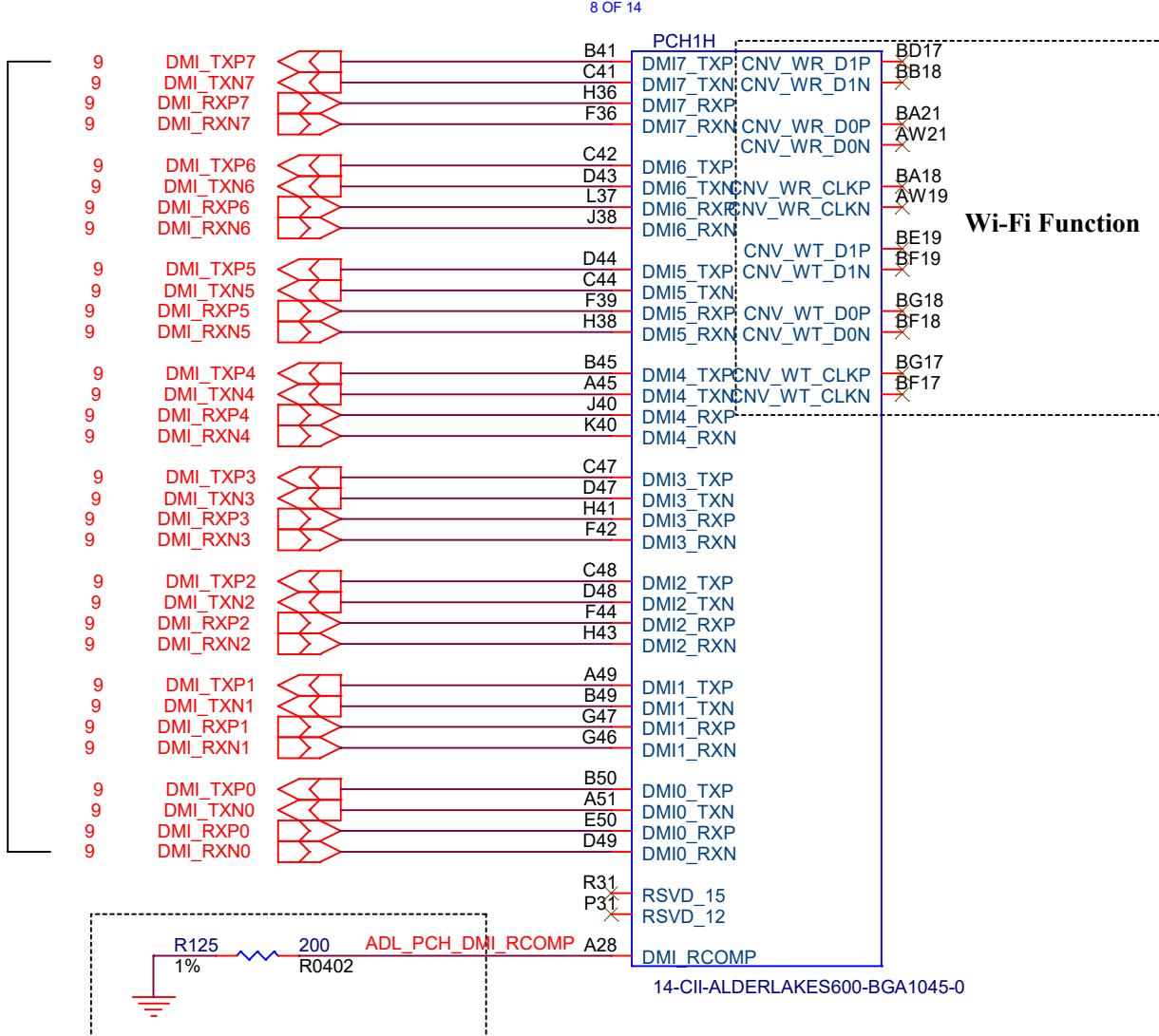
HPC-ADSC

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PCH2_DMI

1x8 (Gen4)
From CPU



<Variant Name>

AAEON Technology INC.

Title

PCH2_DMI

Size Document Number

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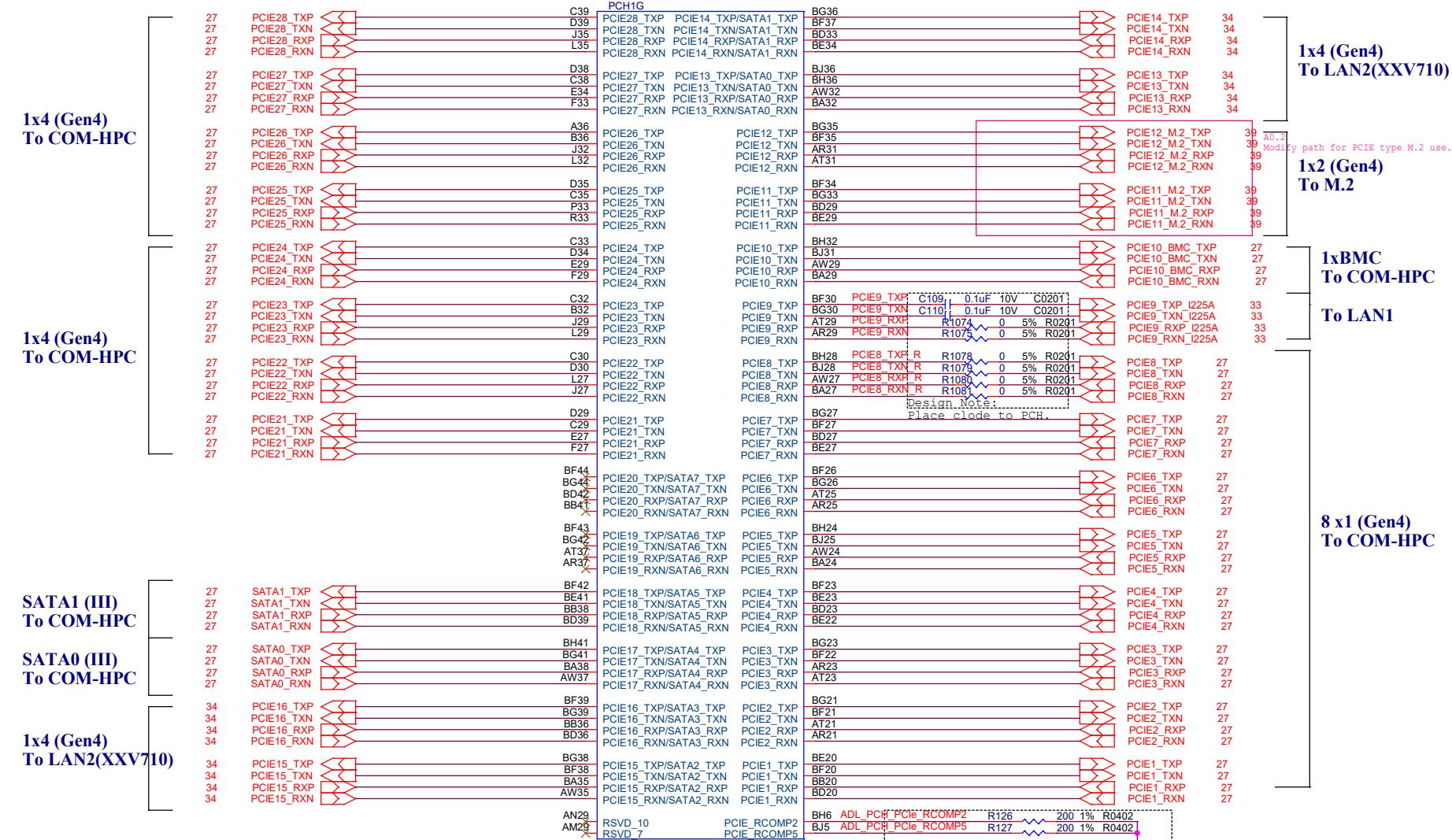
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PCH3_PCIE/SATA



PCIE8_TXP_R	C712	X0.1uF	10V C0201	PCIE9_TXP_I225A
PCIE8_TXN_R	C722	X0.1uF	10V C0201	PCIE9_TXN_I225A
PCIE8_RXP_R	R65	X0 5%	R0201	PCIE9_RXP_I225A
PCIE8_RXN_R	R386	X0 5%	R0201	PCIE9_RXN_I225A

Design Note:
Place clode to PCH.

<Variant Name>



AAEON Technology INC.

Title

PCH3_PCIE/SATA

Size

Document Number

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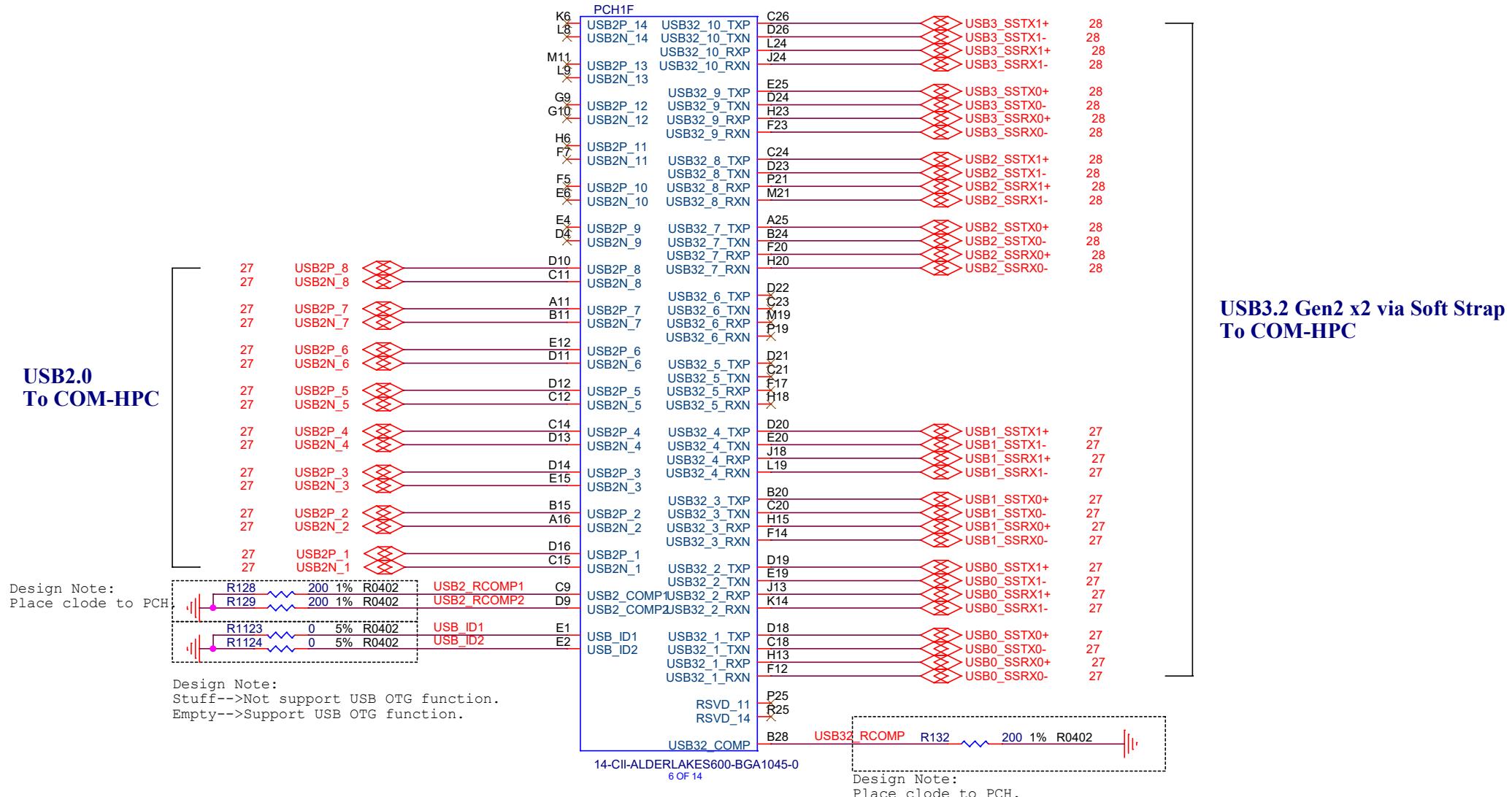
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PCH4_USB3.2/USB2



4. Up to eight USB 3.2 Gen 2x2 Lanes

- A maximum of four USB 3.2 Gen 2x2 Ports can be enabled
- USB 3.2 Gen 2x2 = 20 GT/s

<Variant Name>



AAEON Technology INC.

Title

PCH4_USB3.2/USB2

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PCH5_I2C/SMLINK/UART/SMB

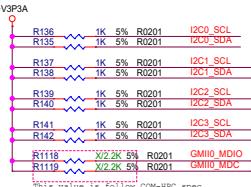
SCI / SMI# and NMI

SCI capability is available on all GPIOs, while SMI and NMI capability is available on only select GPIOs.

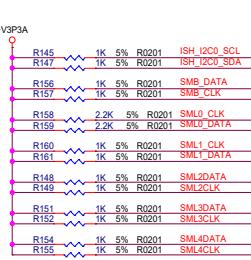
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:

- GPP_B14, GPP_B20, GPP_B23
- GPP_D[3:22]
- GPP_D[0:1], GPP_E[16:13]

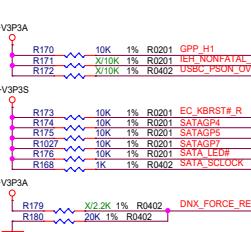
I2C Pull-Up



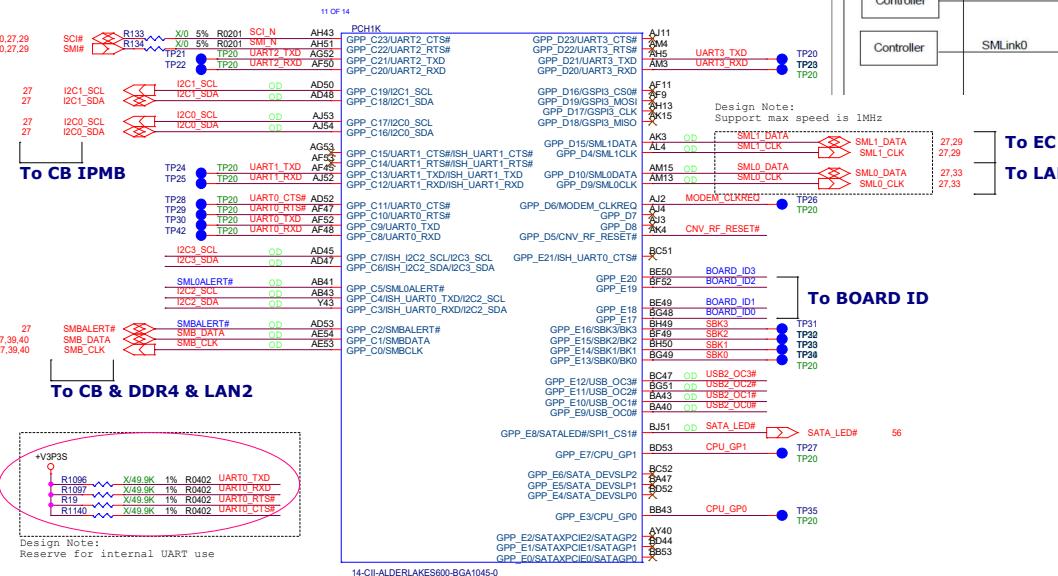
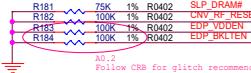
SMLink Pull-Up



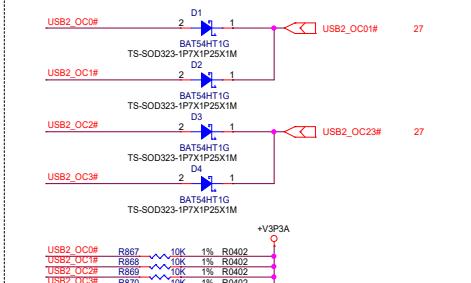
Others PU/PD



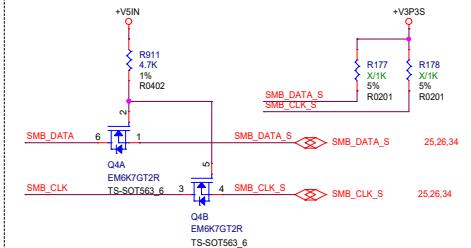
Glitch Issue PD



USB2.0 OC#



SMBus Level Shifter To DDR4



GPP_C2_SMBALERT#	TLS confidentiality
0	Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 *	Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

* Default, Internal Pull-Down 20K

GPP_C5_SML4ALERT#	ESPI DISABLE
0 *	Enabled (Default)
1	Disabled

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts

GPP_H2_SML4ALERT#	ESPI Flash Sharing Mode
0 *	Master Attached Flash Sharing (MAFS)
1	Slave Attached Flash Sharing (SAFS)

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts

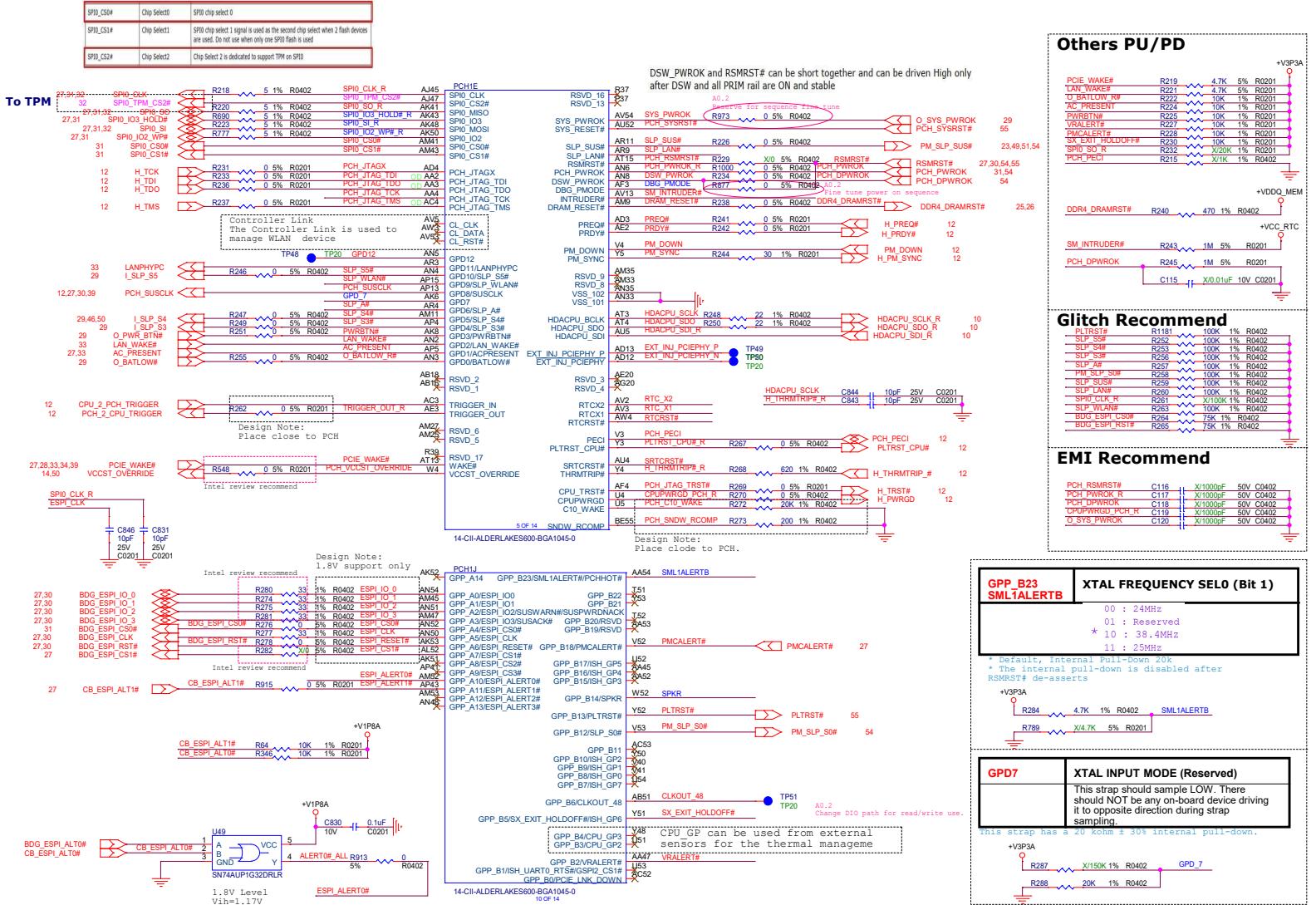
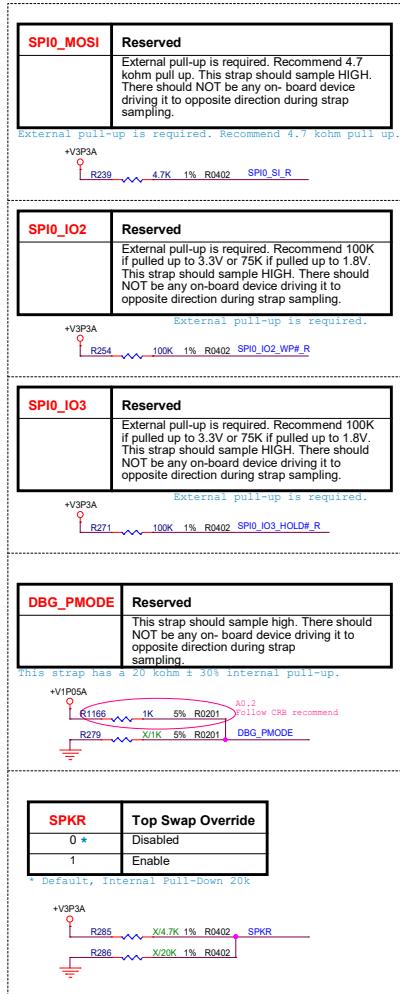
GPP_H15_SML4ALERT#	JTAG ODT Disable
0	JTAG ODT is disabled
1 *	JTAG ODT is enabled

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts

GPP_H18_SML4ALERT#	VCCSPI voltage configuration
0 *	VCCSPI at 3.3 V
1	VCCSPI at 1.8 V

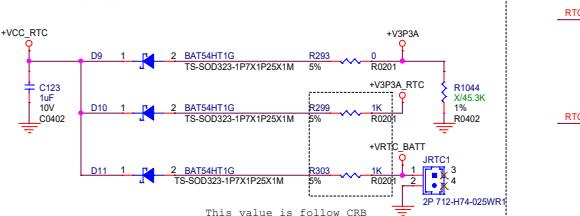
* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts

PCH7_SPI/JTAG/MISC/ESPI

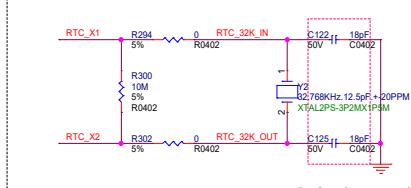


RTC Battery

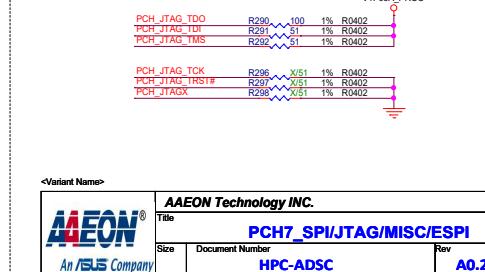
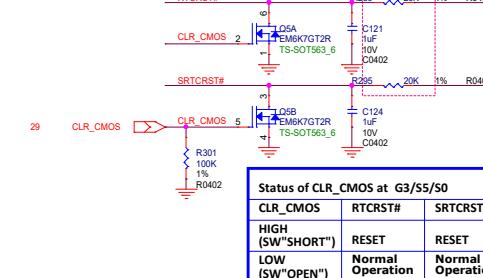
In this platform, whether VCCRTC is sourced from Vbatb in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.465V.



XTAL-32.768KHz



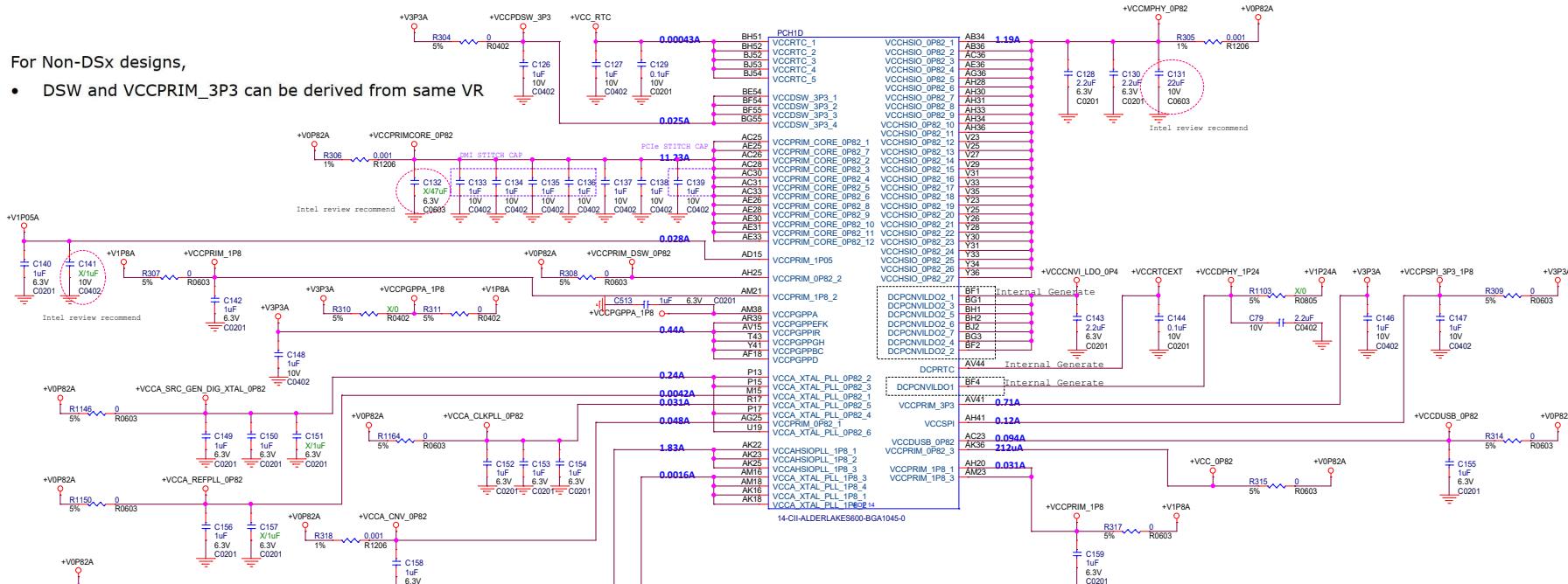
RTCRST#



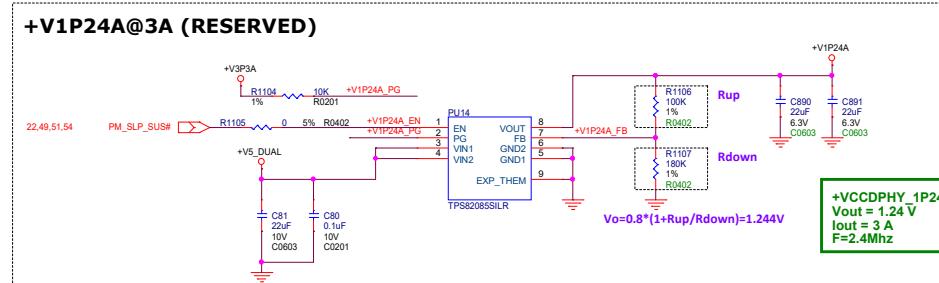
PCH8_POWER

For Non-DSx designs,

- DSW and VCCPRIM_3P3 can be derived from same VR

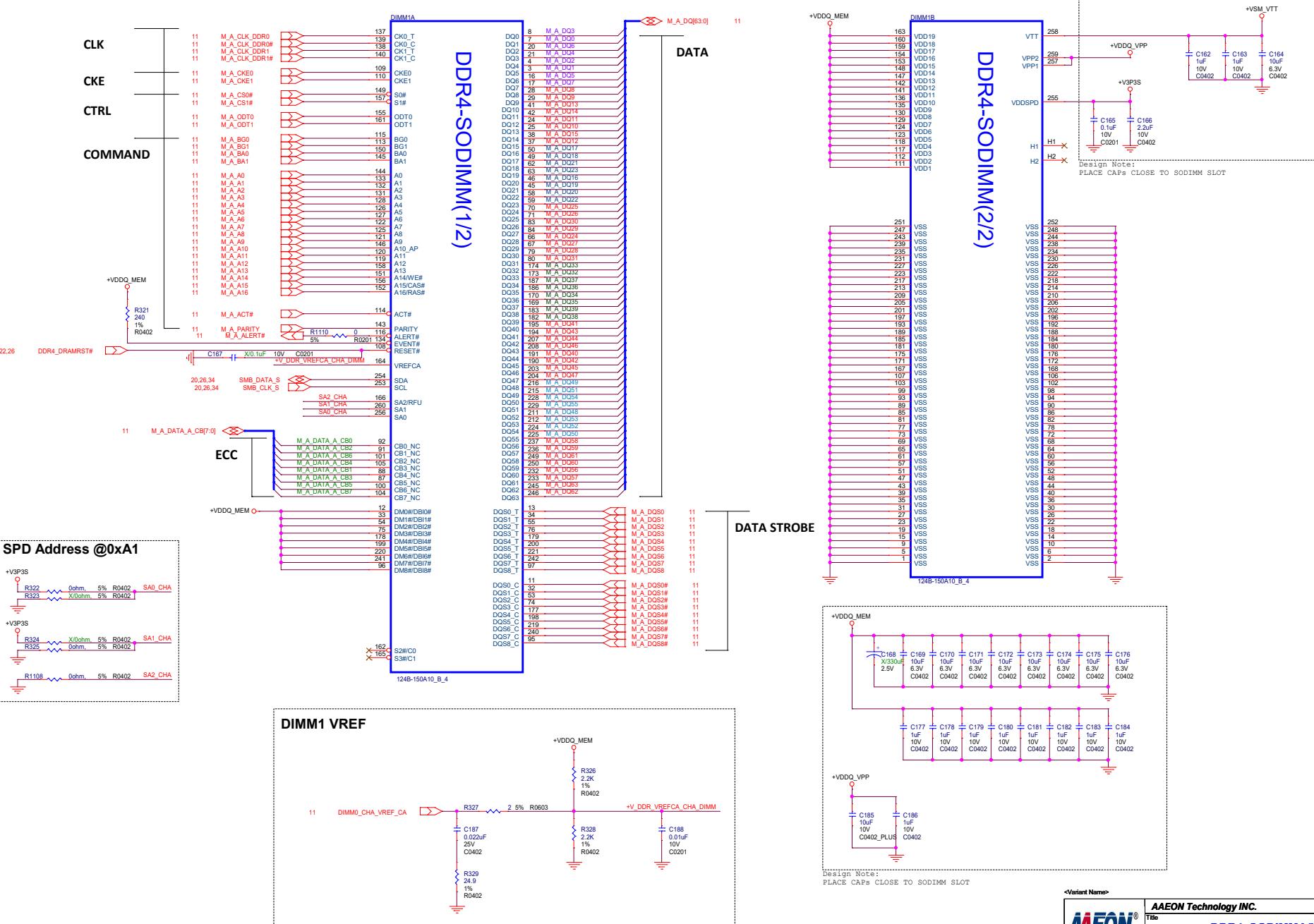


DCPCNVIDO1	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose. Refer to "Platform Design Guidelines" document.
DCPCNVIDO2	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose. Refer to "Platform Design Guidelines" document.

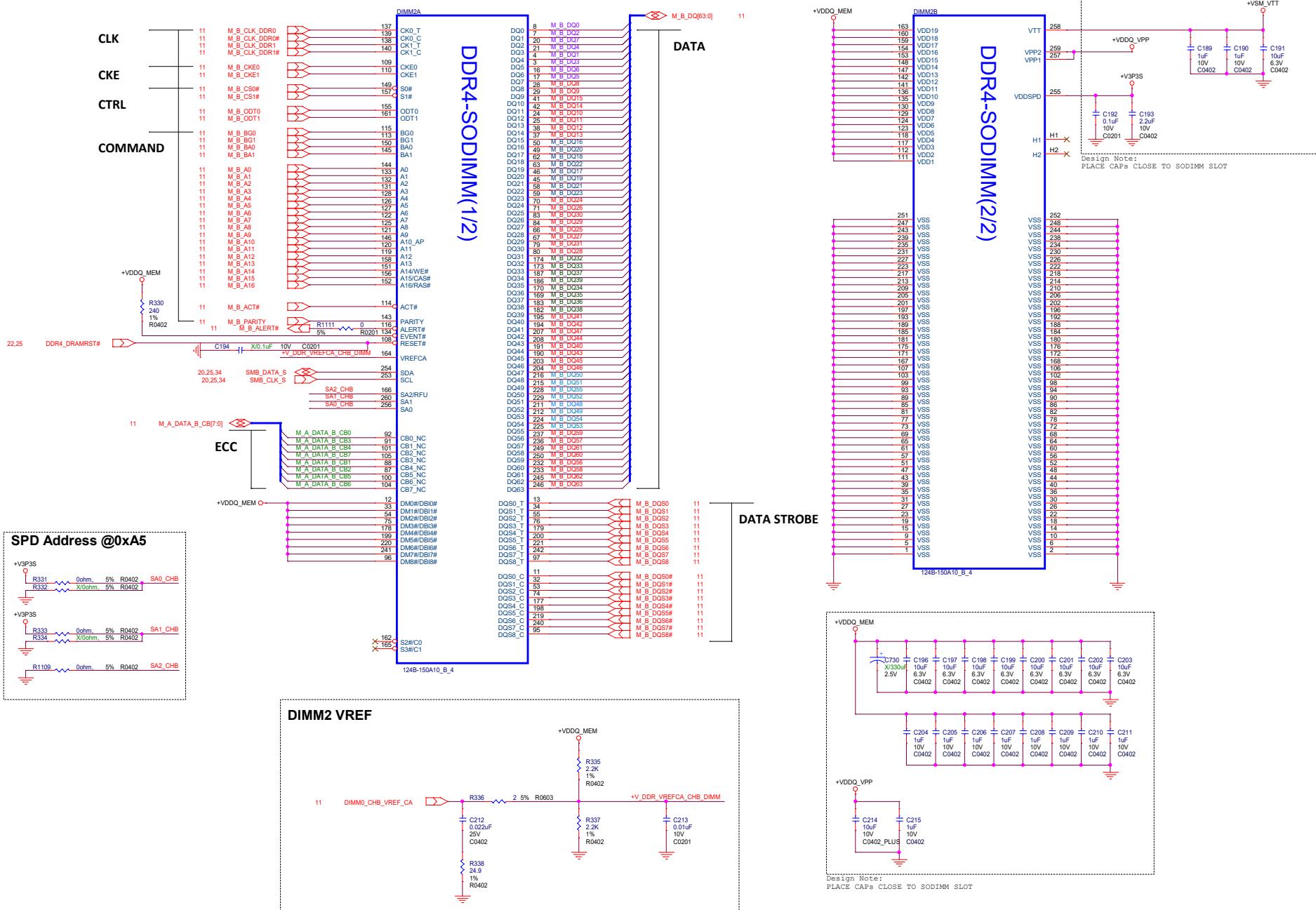


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HPC-ADSC		A0.2.0.0	
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DDR4_SODIMMA(Vertical)

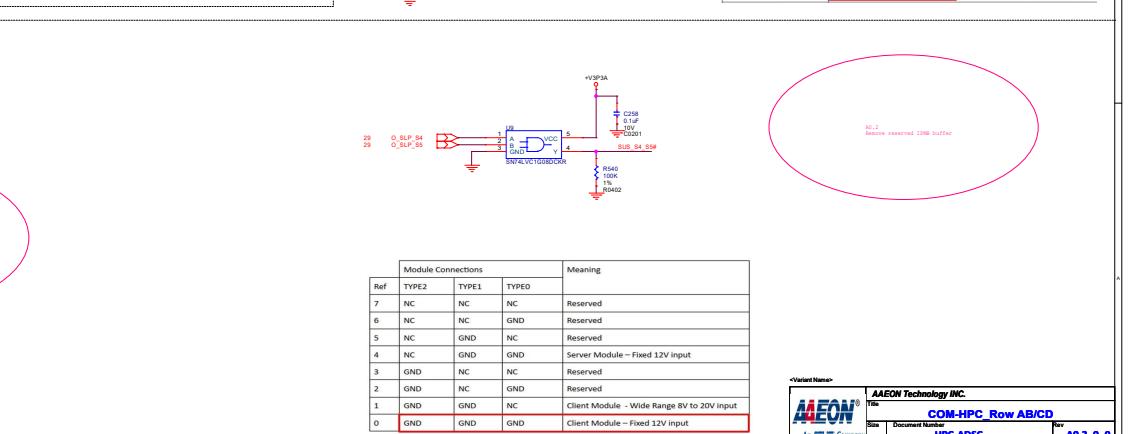
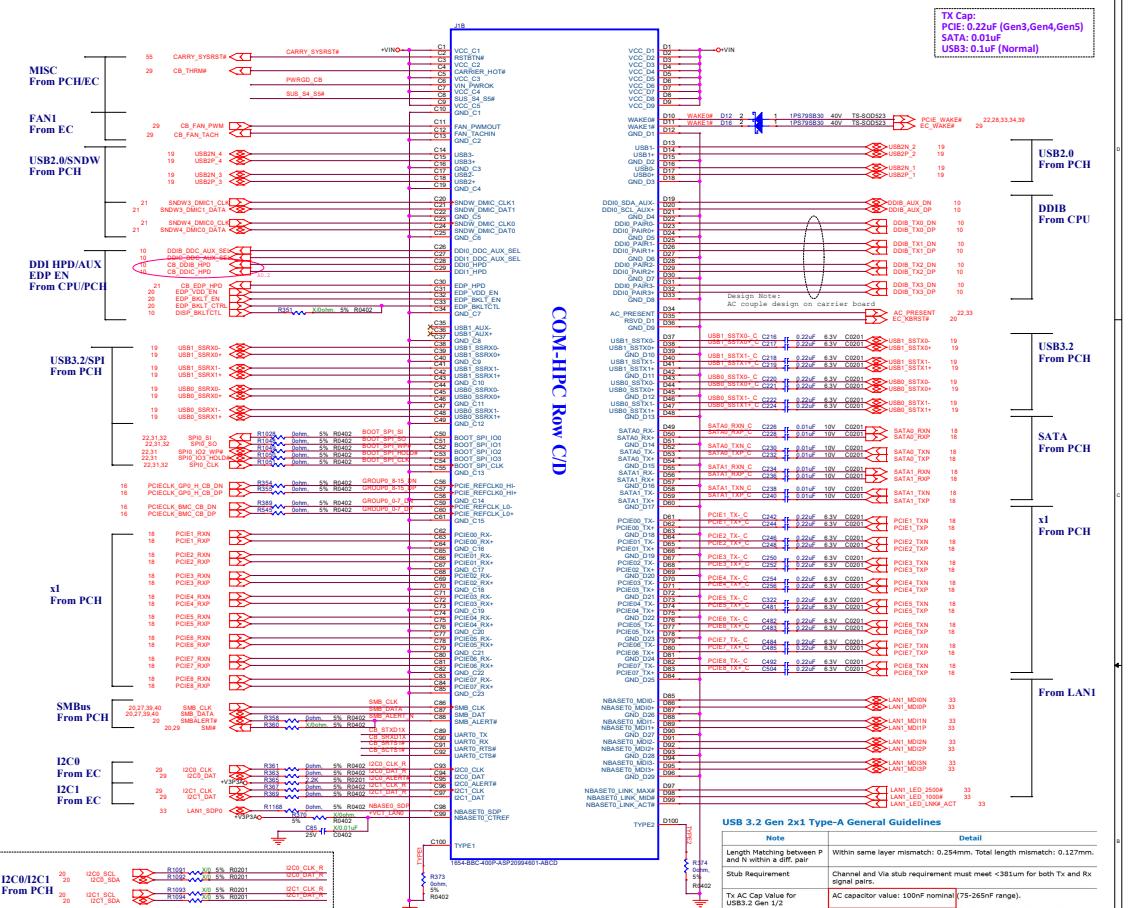
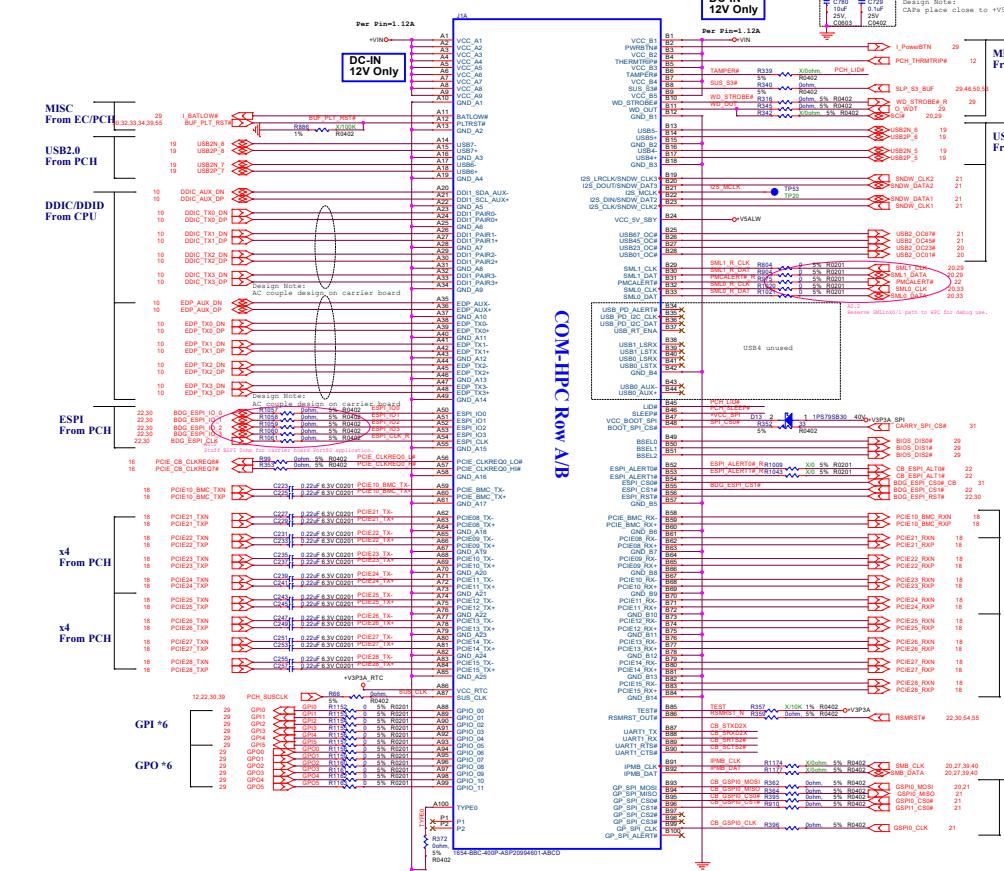


DDR4_SODIMMB(Vertical)



Variant Name		
AAEON Technology INC.		
Title DDR4_SODIMMB(Vertical)		
Size	Document Number	Rev
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COM-HPC_Row AB/CD



AAEON Technology INC.
Title: COM-HPC Row AB/CD
In ASUS Company
Document ID: HPC-ADSC
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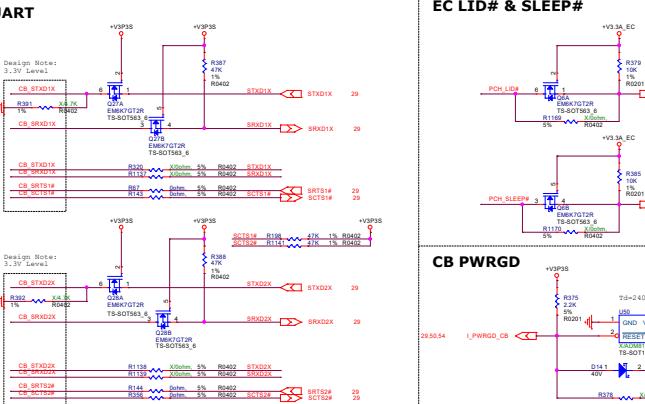
<Variant Name>

COM-HPC Row AB/CD

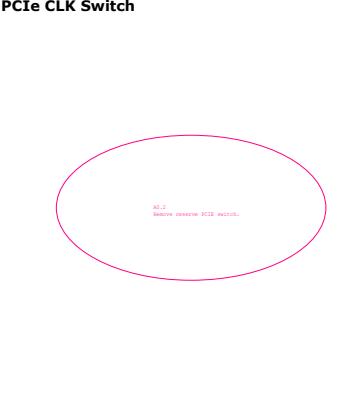
HPC-ADSC

AD 2.0

UART



PCIe CLK Switch



Ref	TYPE2	TYPE1	Meaning
7	NC	NC	Reserved
6	NC	NC	GND
5	NC	GND	NC
4	NC	GND	Server Module - Fixed 12V Input
3	GND	NC	NC
2	GND	NC	GND
1	GND	GND	Client Module - Wide Range 8V to 20V Input
0	GND	GND	Client Module - Fixed 12V Input

<Variant Name>

AAEON Technology INC.

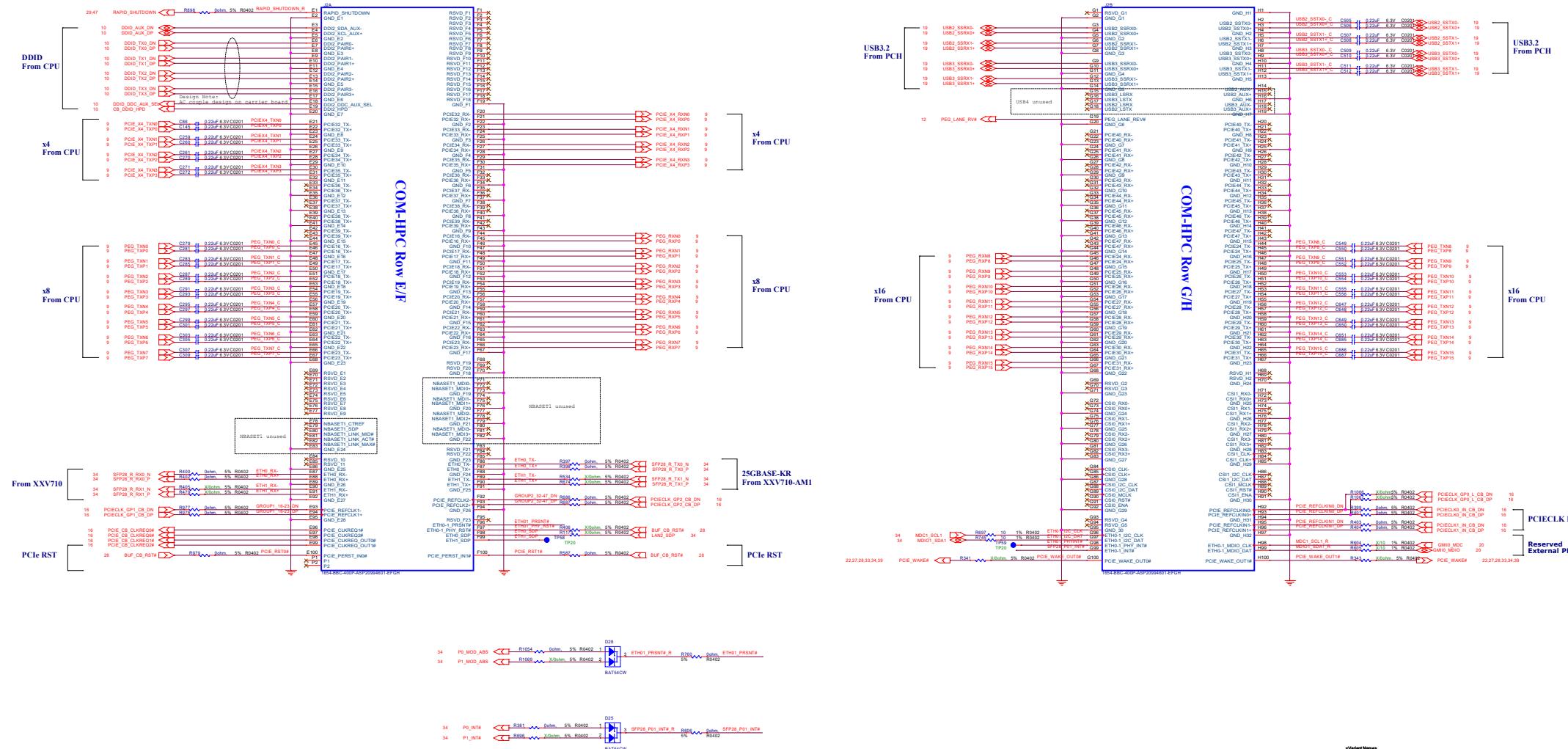
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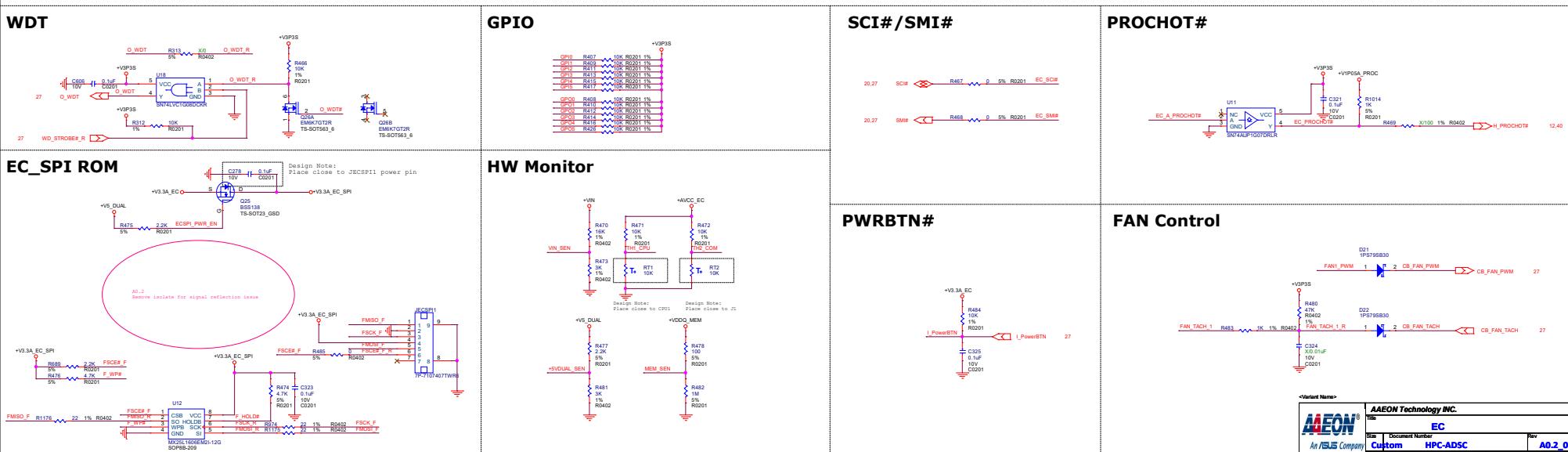
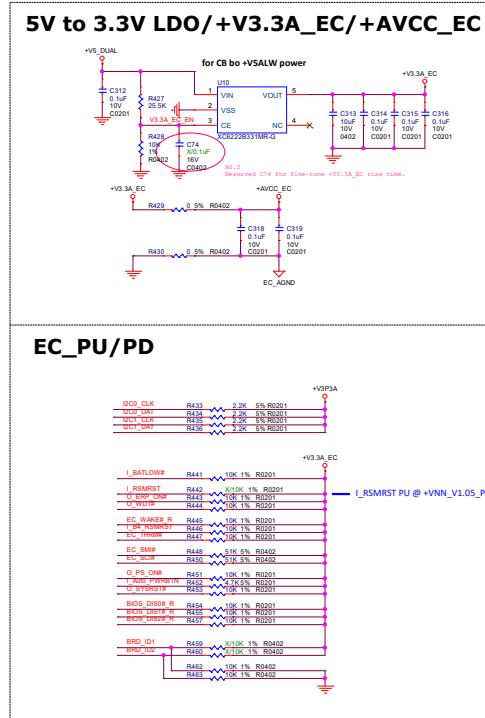
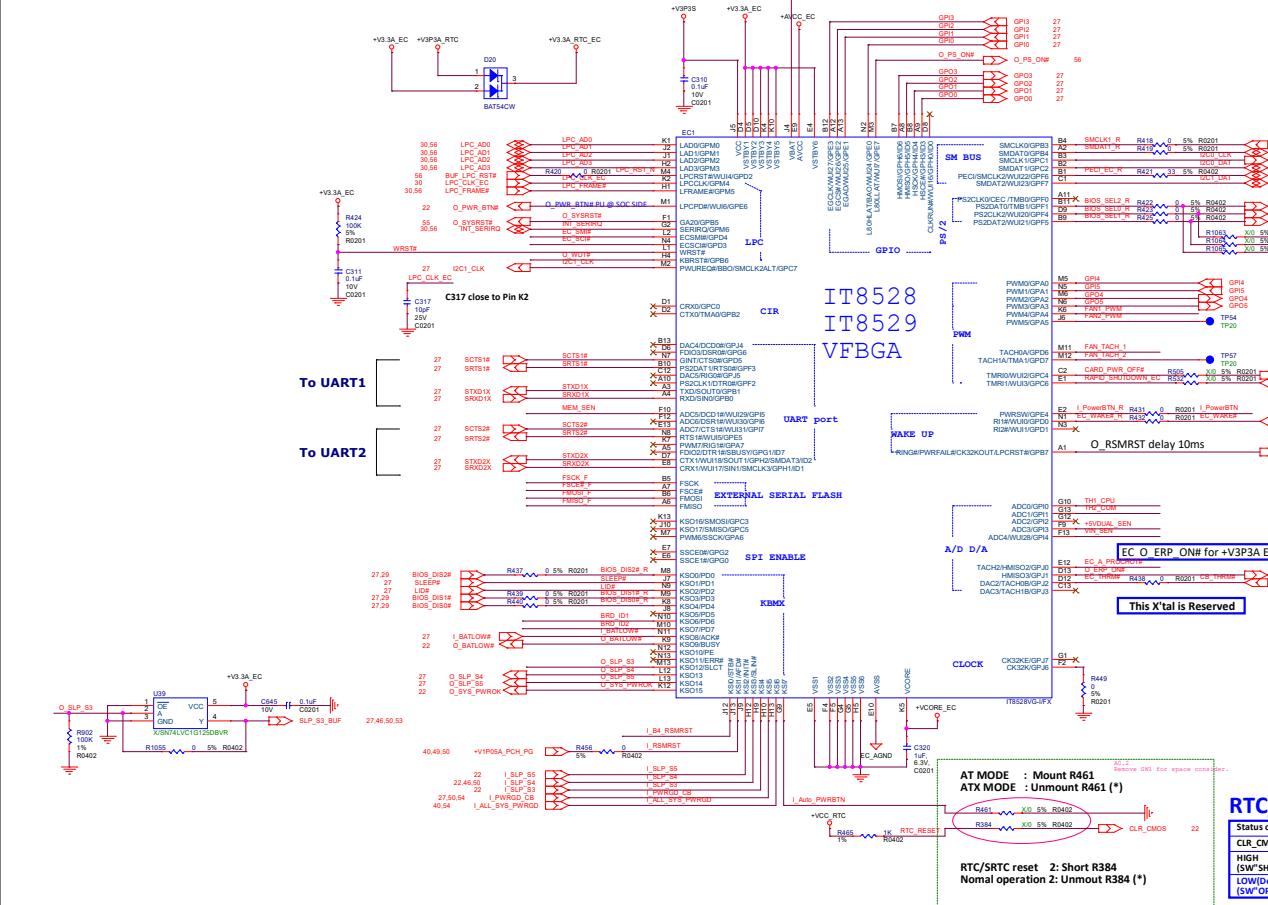
In ASUS Company

Document ID: HPC-ADSC

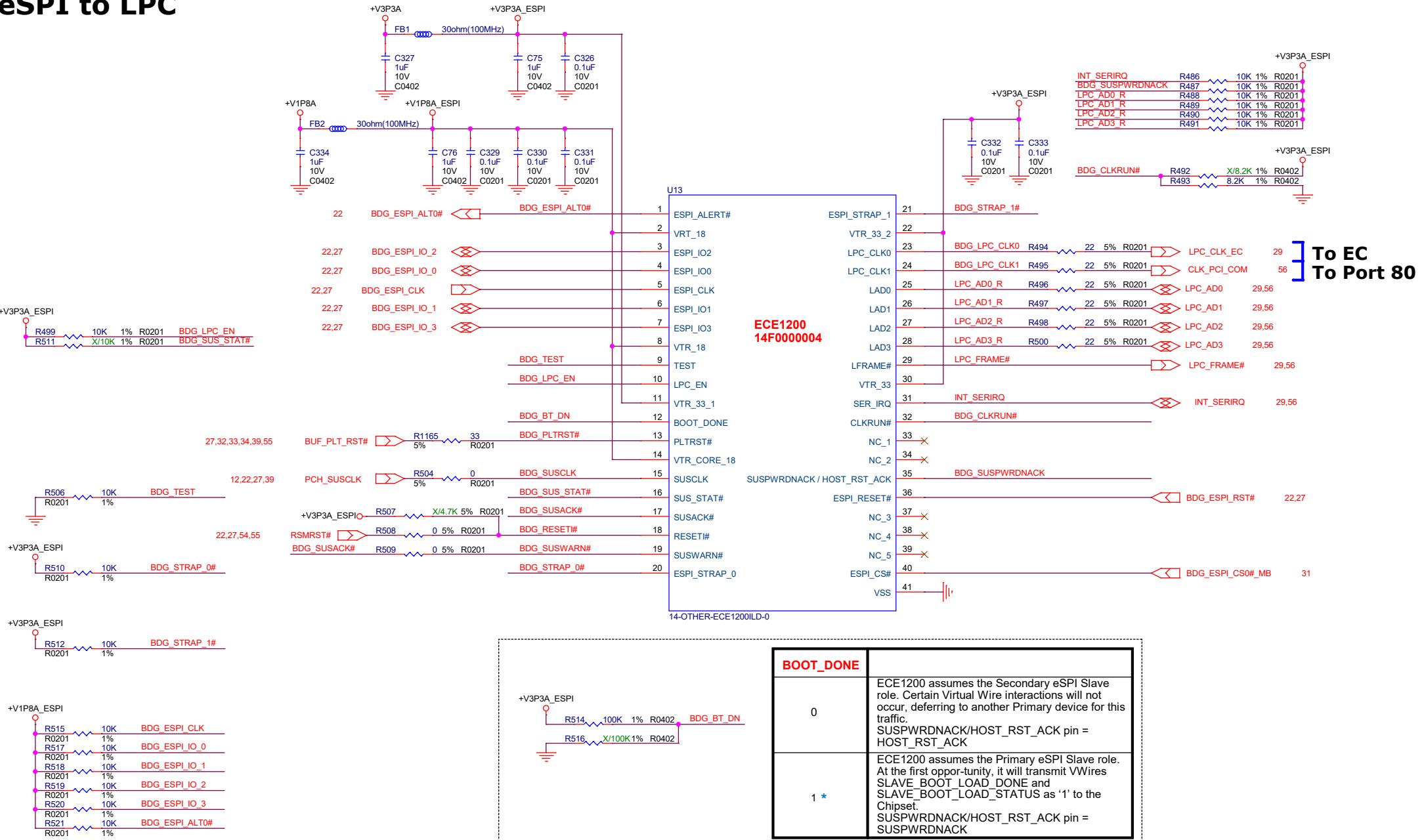
Page: 27 of 36

COM-HPC_Row EF/GH

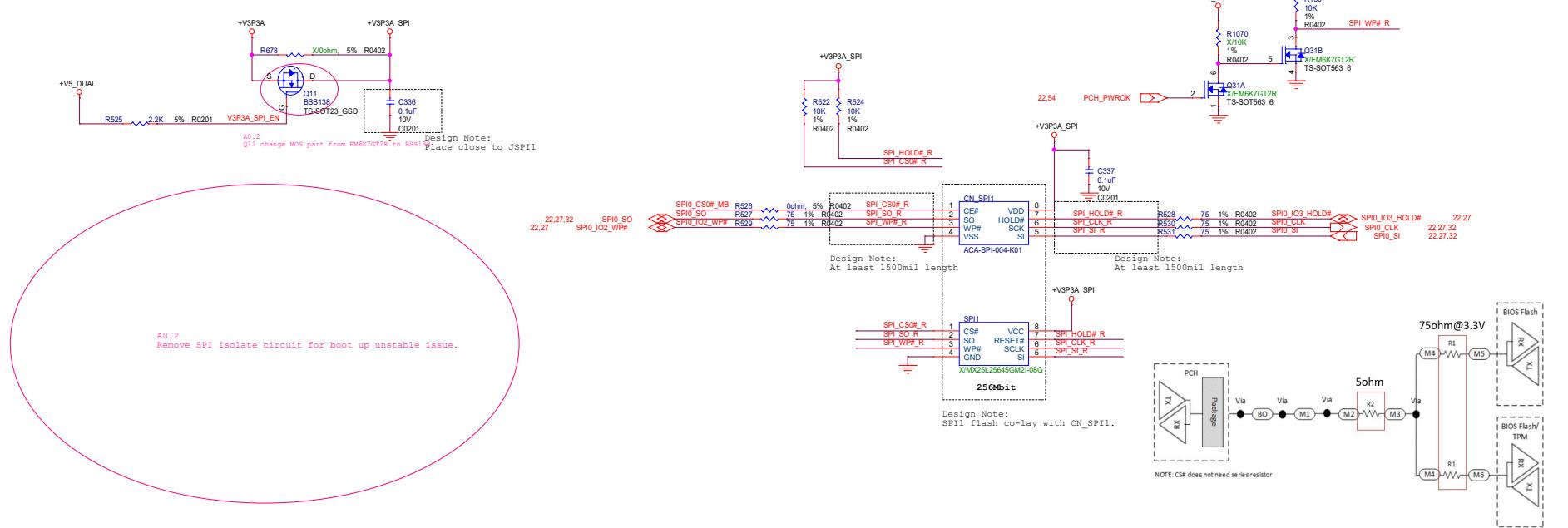




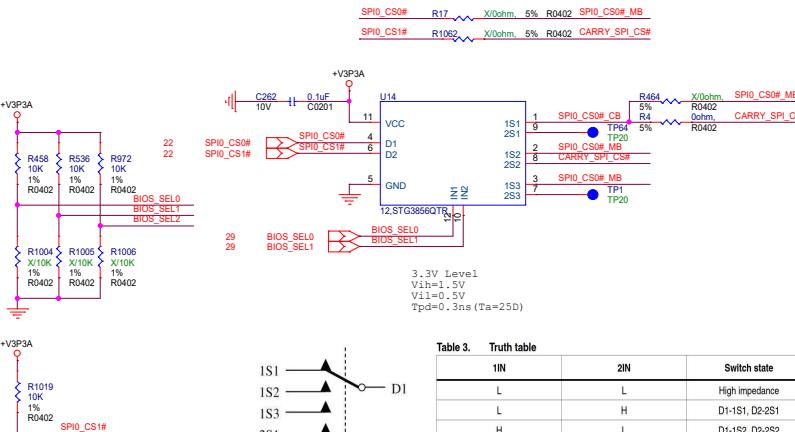
eSPI to LPC



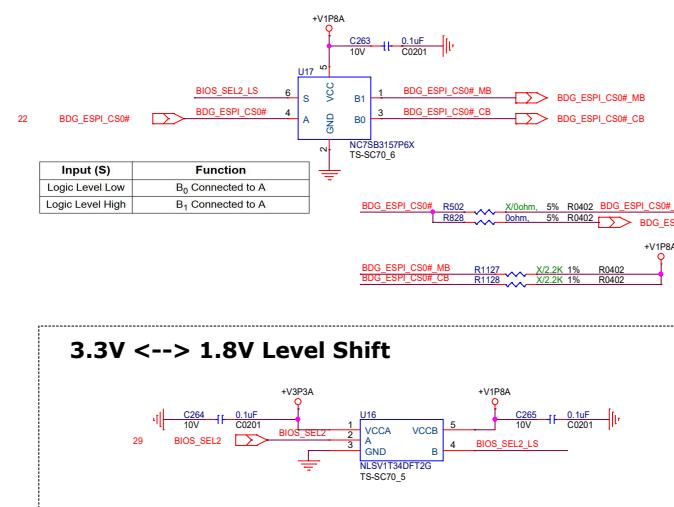
SPI Flash



SPI Switch



eSPI Switch



3.3V <--> 1.8V Level Shift

BSEL2	BSEL1	BSEL0	eSPI_CS0#	eSPI_CS1#	SPI_CS0#	SPI_CS1#	Carrier_SPI_CS#	Carrier_eSPI_CS#	BIOS_ENTRY	Note
1	1	1	Module	N/A	Module	OFF	OFF	SPI	ME on SPI0	
1	1	0	Module	N/A	Carrier	SPI0	OFF	SPI	ME on SPI0	
1	0	1	Module	Carrier	Module	OFF	eSPI_CS0#	SPI	ME on SPI1	
0	1	1	Carrier	N/A	Module	OFF	eSPI_CS0#	ESPI	ME only on Carrier EEPROM	
0	1	0	Carrier	N/A	Carrier	OFF	eSPI_CS0#	ESPI	ME only on Carrier EEPROM	
0	0	1	Carrier	N/A	Module	OFF	eSPI_CS0#	ESPI	ME only on Module EEPROM	
0	0	0	-	-	-	-	-	-	Reserve for future use	



AAEON Technology INC.

Title BIOS-SPI/GSPI

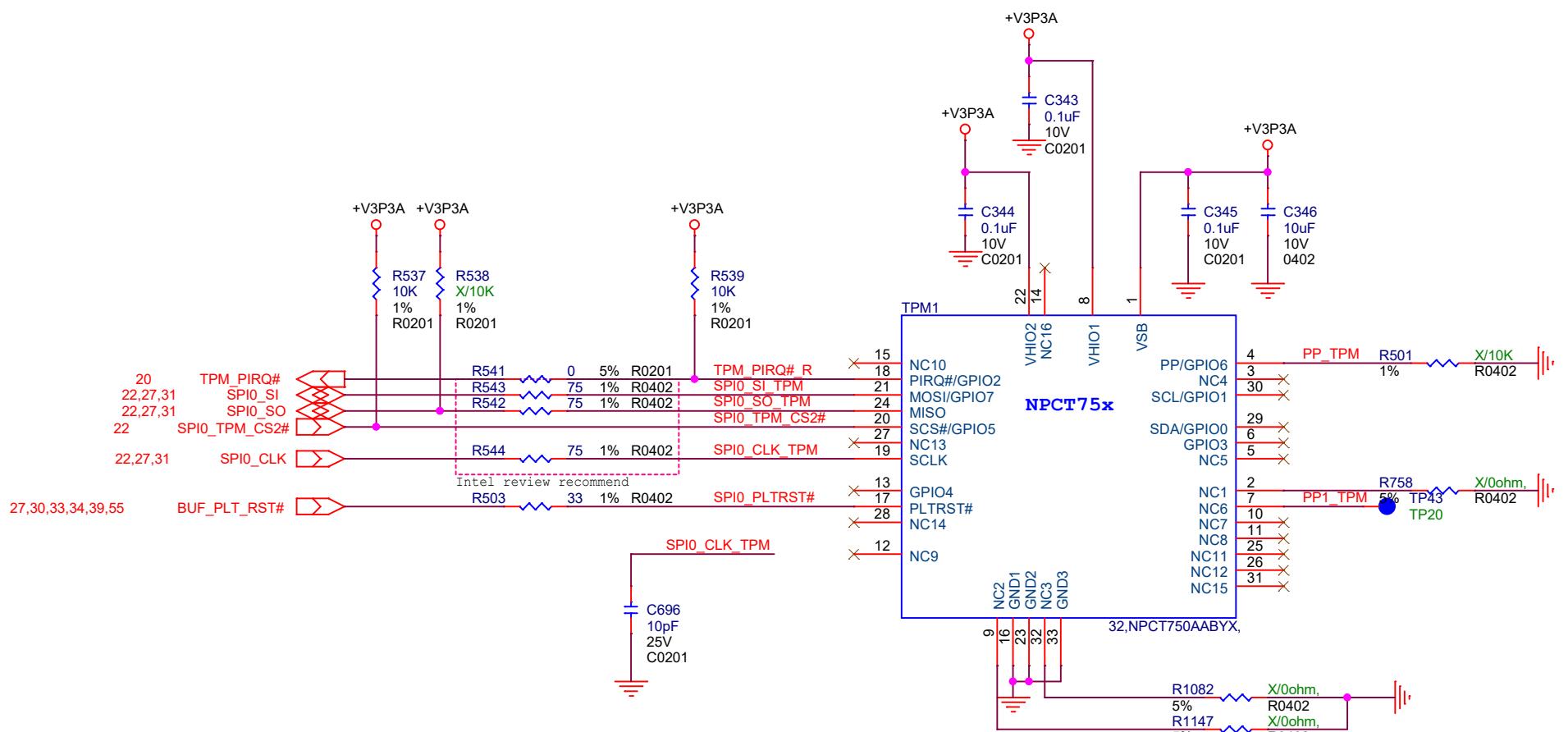
Size Document Number HPC-ADSC

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Date Wednesday, April 20, 2022

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TPM2.0

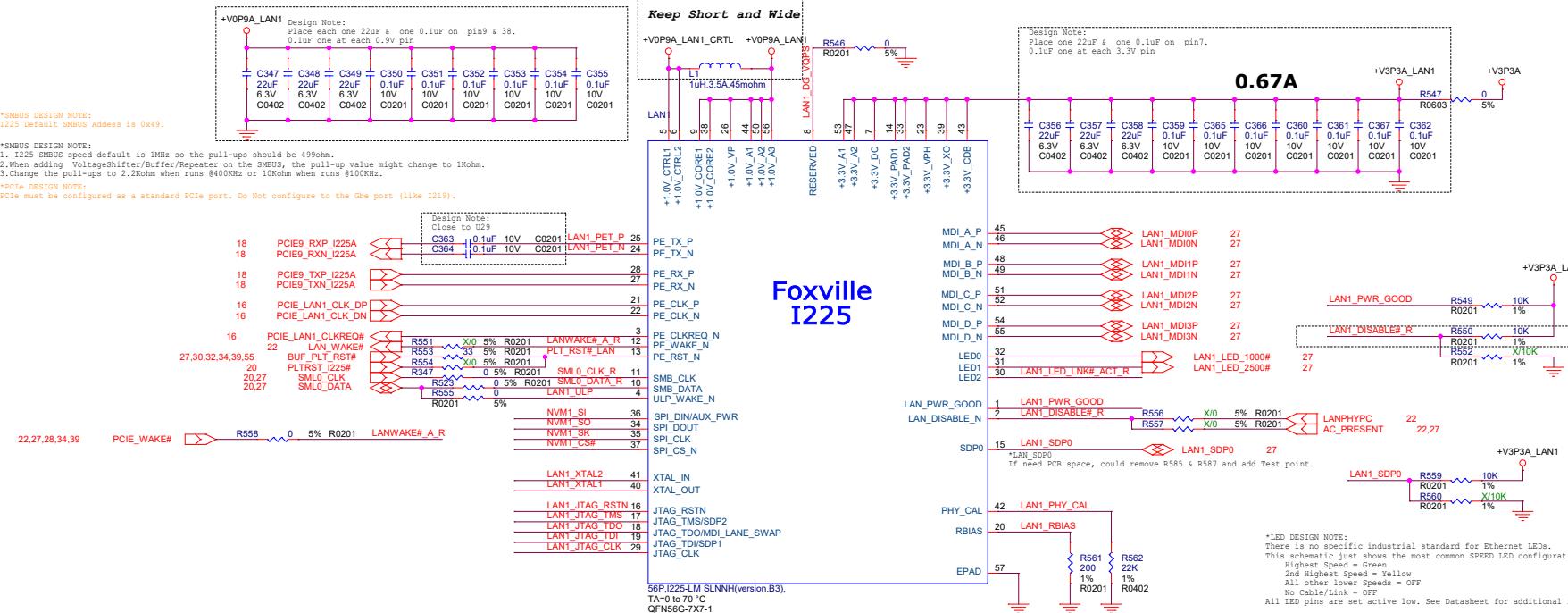


The PP signal indicates the owner's physical presence. The PP is enabled by default and has an internal pull-down¹. When the PP signal is not used, it should be left unconnected.

Design Note:
STUFF:R758,R1082,R1147-->For Infineon SLB9670

<Variant Name>			
AAEON Technology INC.			
Title			
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	HPC-ADSC		
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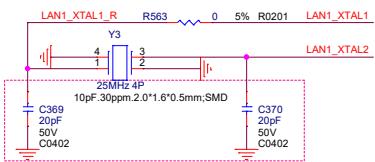
LAN1_I225



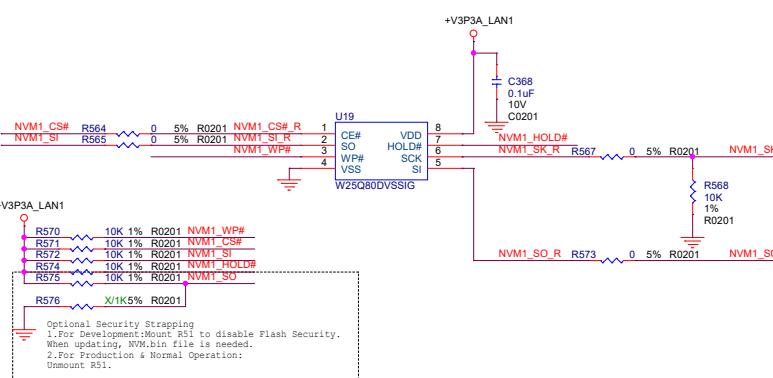
Connecting SMBus Interface

The I225 SMB_DATA and SMB_CLK signals must be connected to the PCH SMLINK0 for supporting vPro. These pins require pull-up resistors to the 3.3V supply rail.

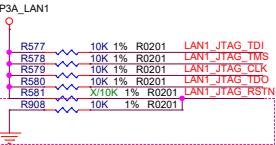
XTAL-25MHz



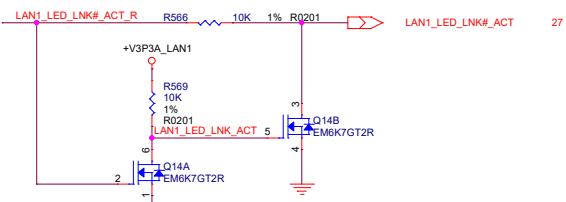
EEPROM



JTAG-STRAP



Leakage Reserve



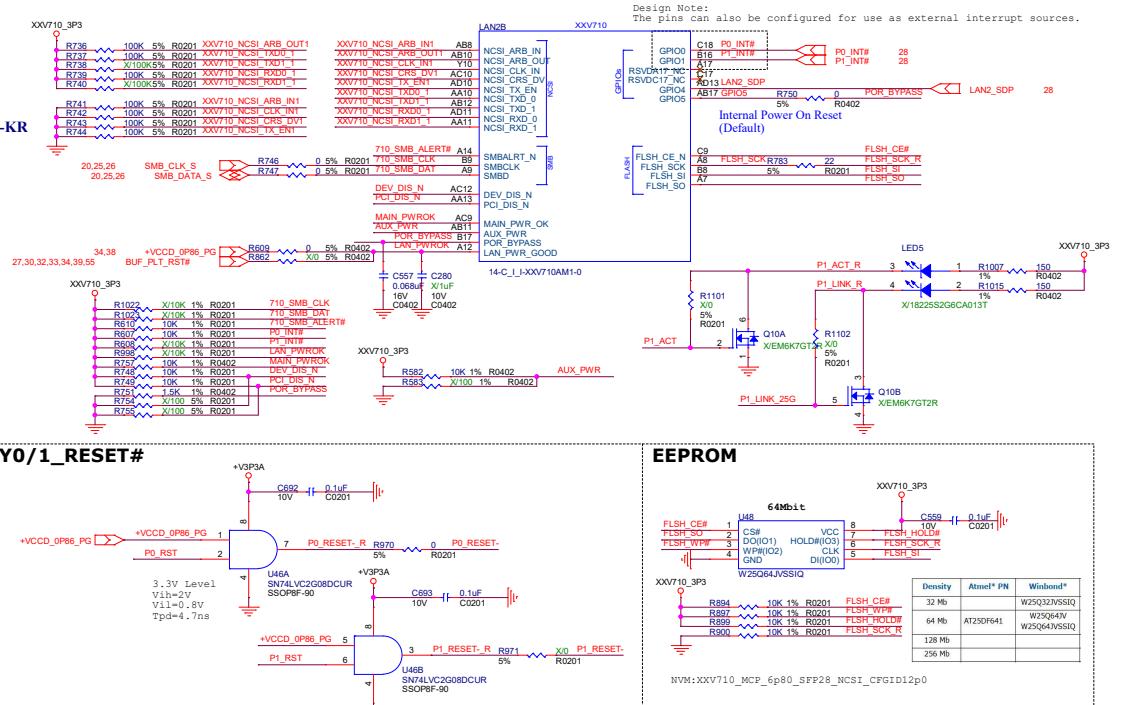
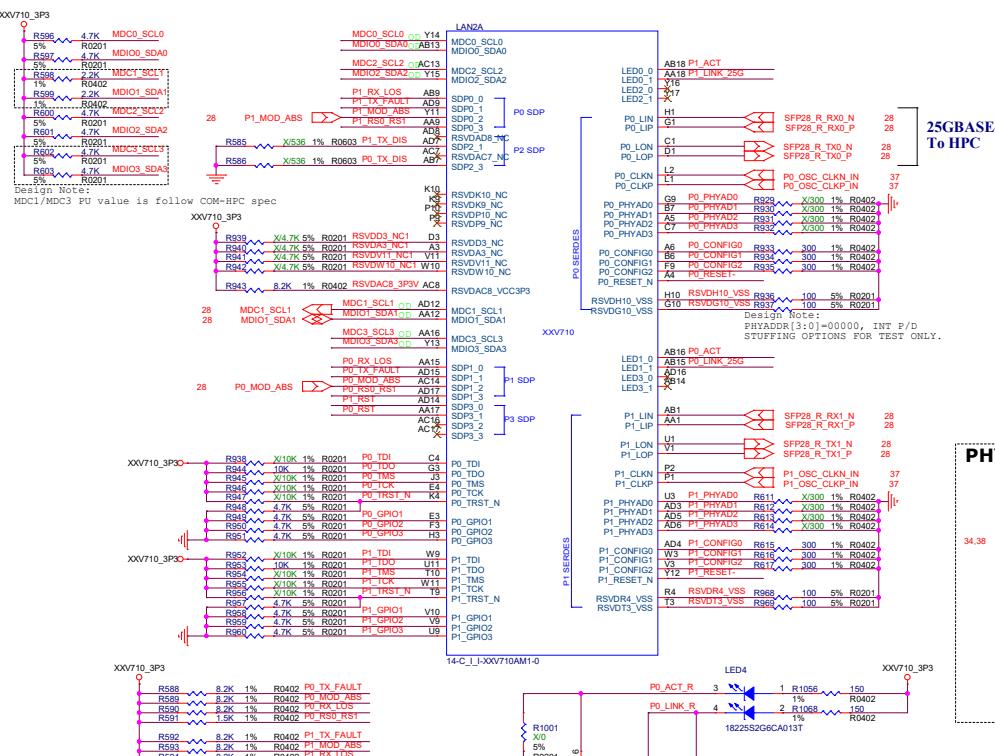
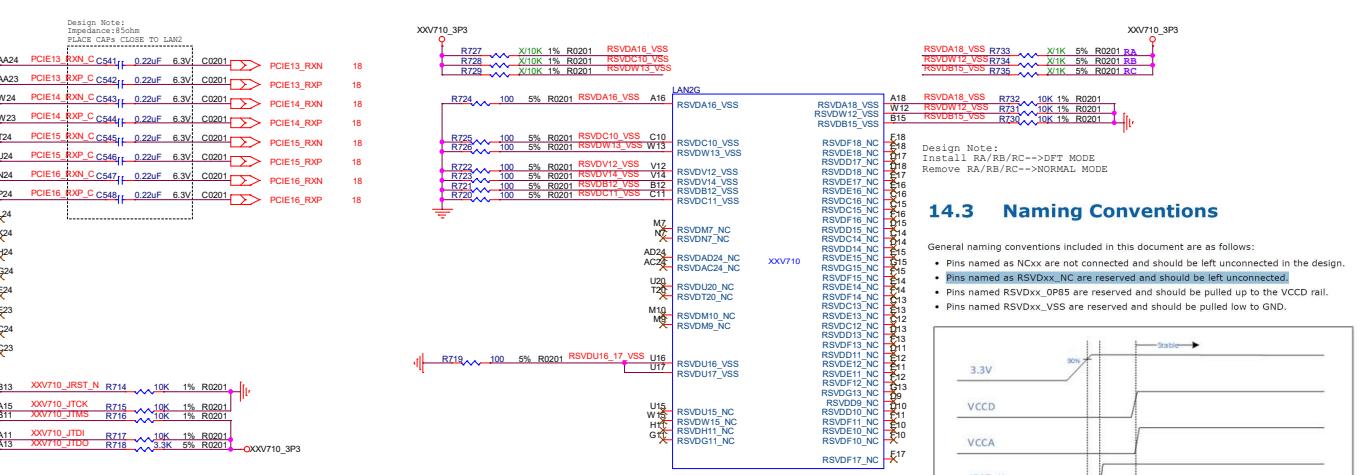
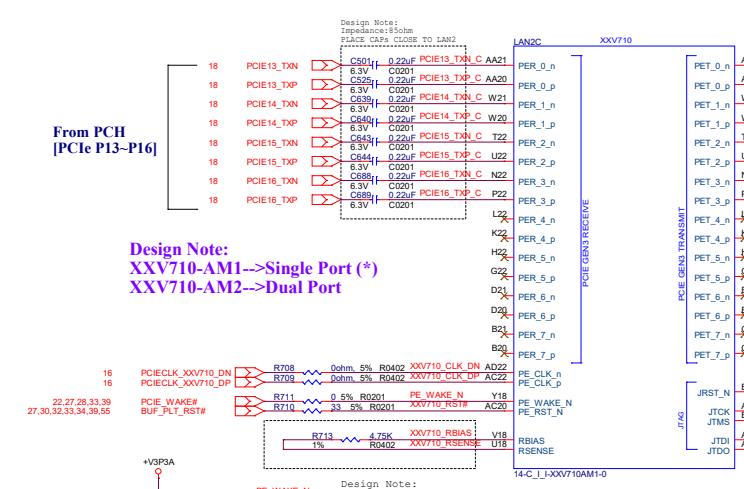
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AEON Technology INC.		
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Size	Document Number	Rev
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Date: Wednesday, April 20, 2022	Sheet 33 of 38	1

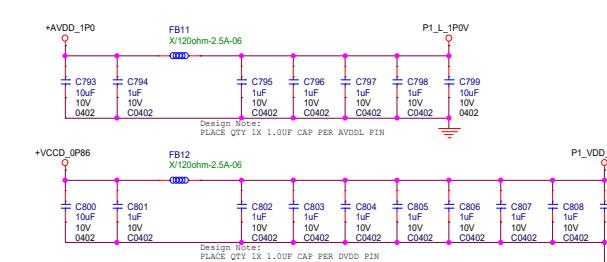
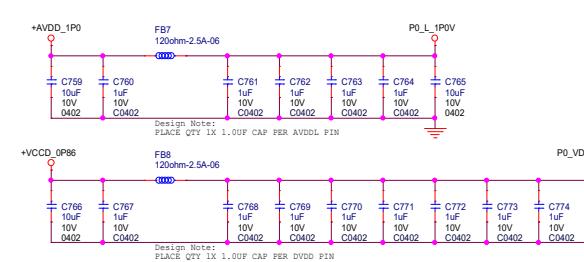
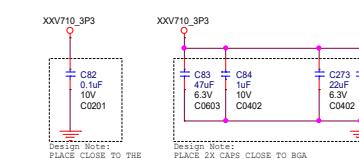
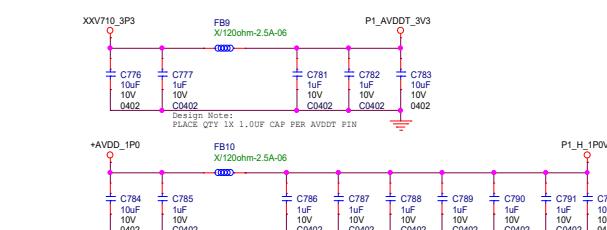
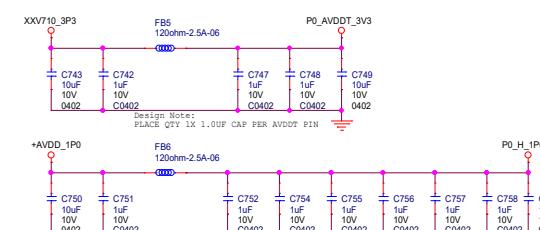
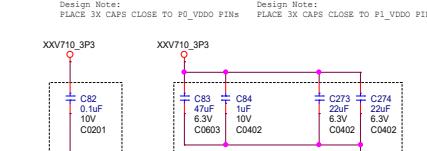
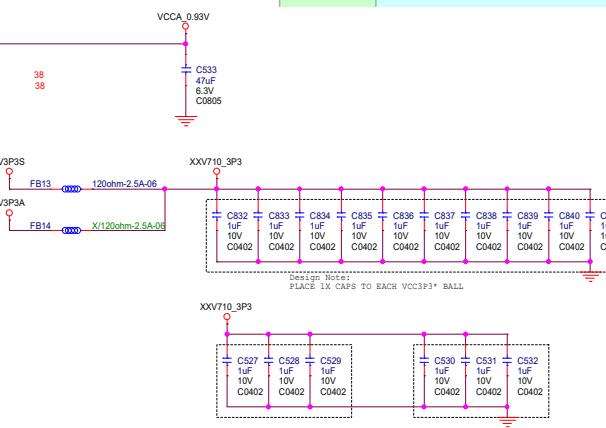
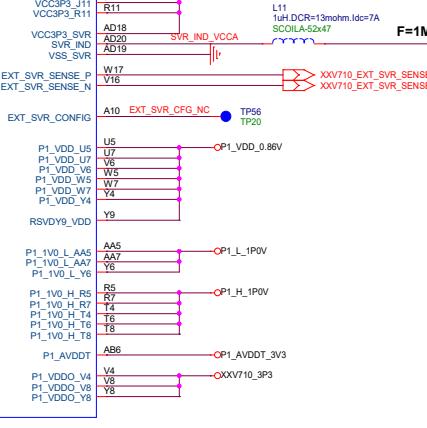
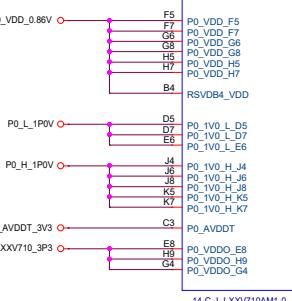
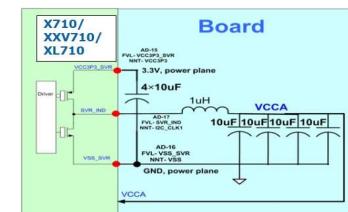
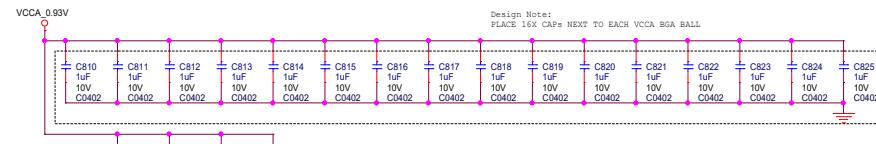
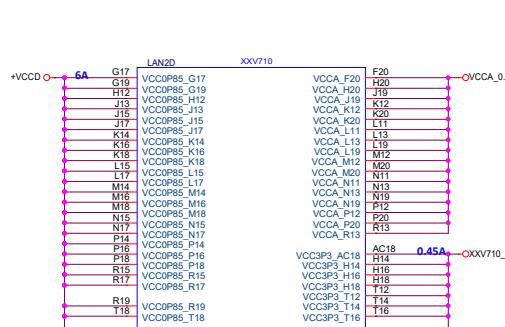
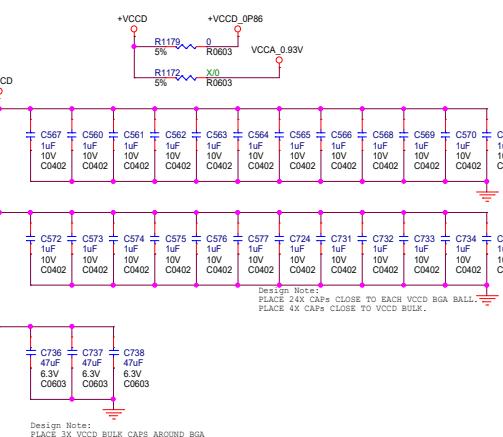
XXV710_PCIE/JTAG/SDP/NCSI/SMB

From PCH
[PCIe P13-P16]



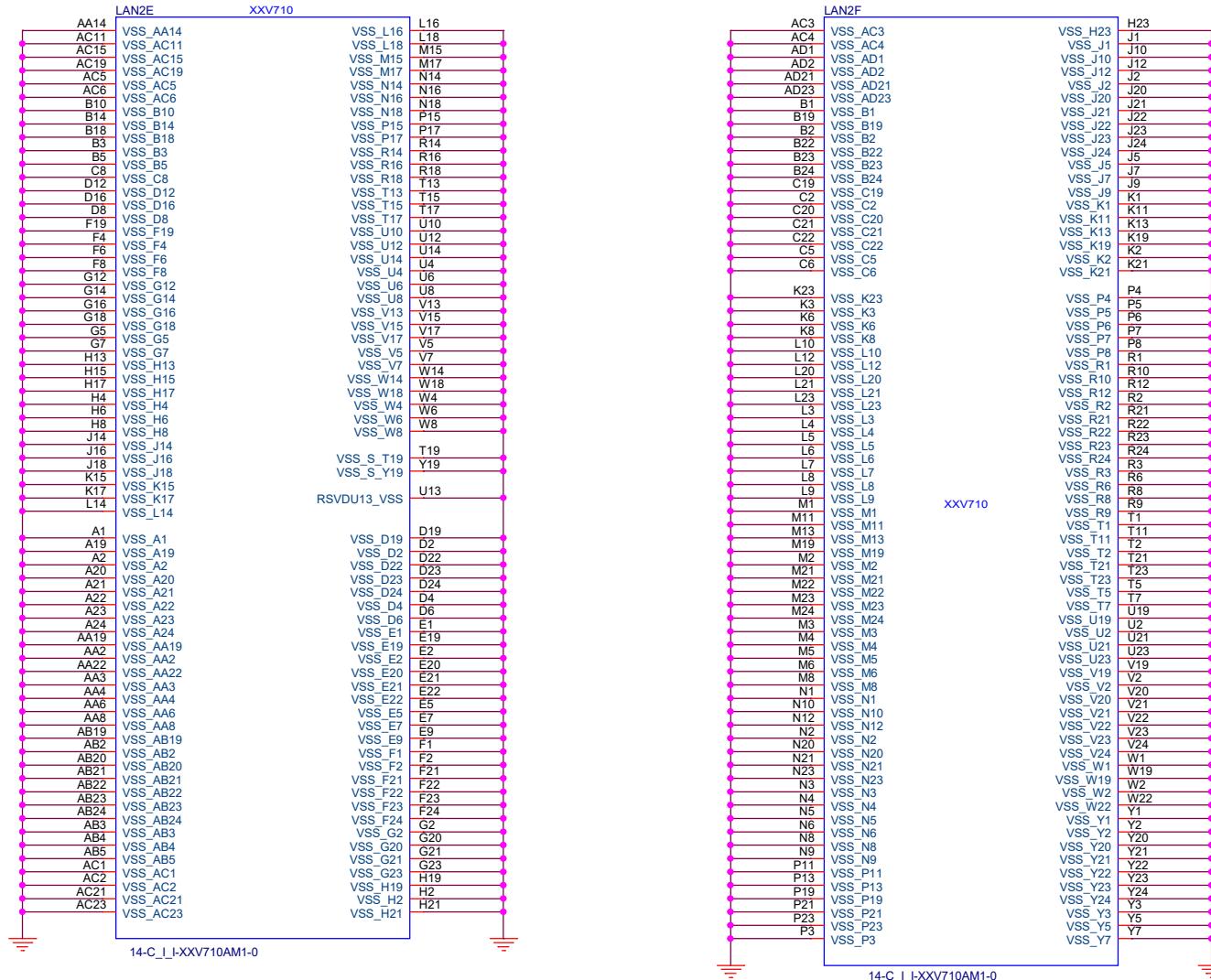
Status	LED Color
Act/Link	Green
25GbE	Orange

XXV710_POWER



Variant Name:			
AAEON Technology INC.			
Title: XXV710_POWER			
Size	Document Number	Rev	
C	HPC-ADSC	A0.2.0_0	
Date: Wednesday, April 20, 2022			

XXV710_GND



<Variant Name>



AAEON Technology INC.

Title

XXV710_GND

Size

Document Number

HPC-ADSC

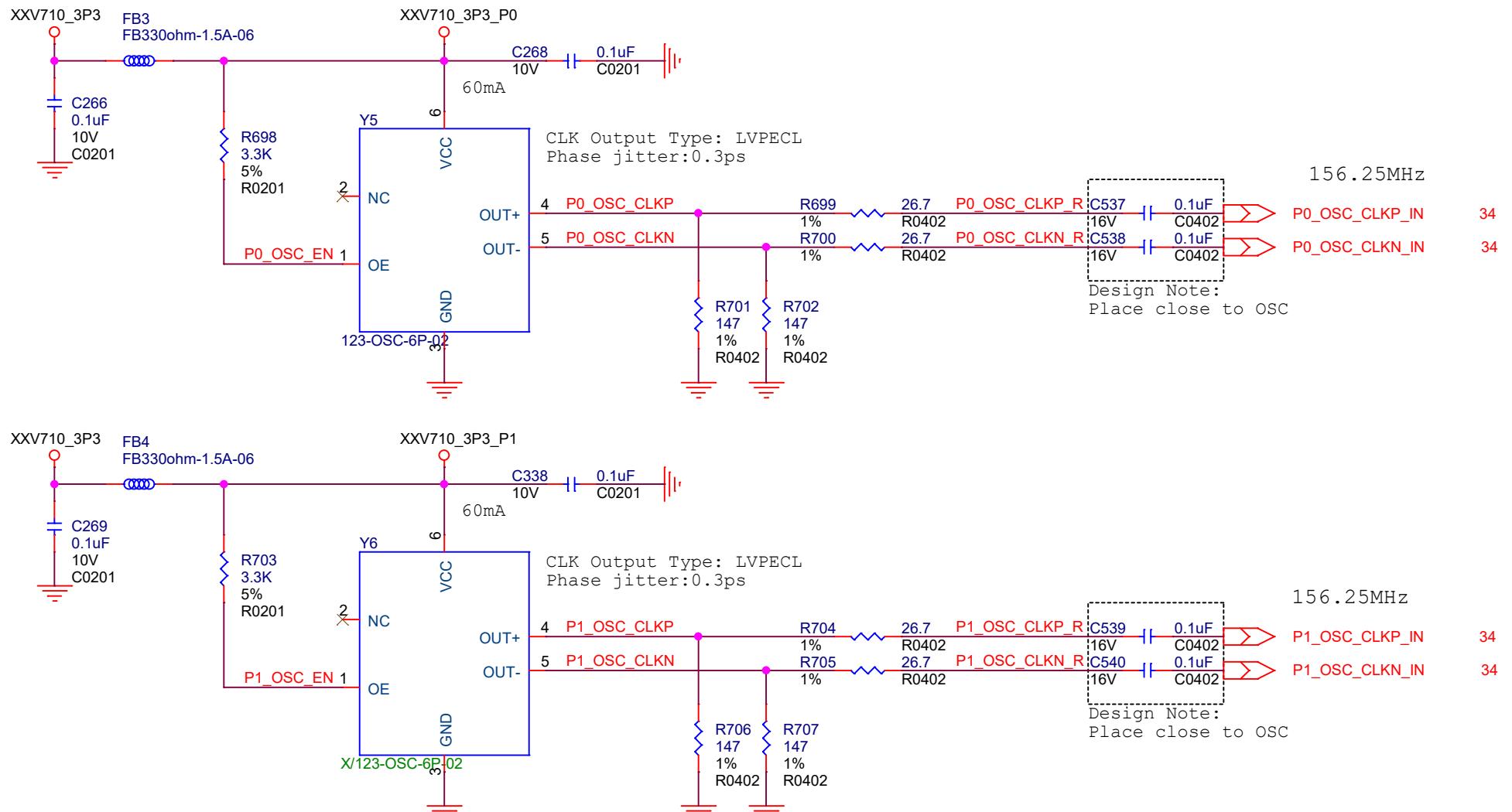
Rev

A0.2_0_0

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XXV710_I/O CLK



<Variant Name>



AAEON Technology INC.

Title

XXV710_I/O CLK

Size

Document Number

Rev

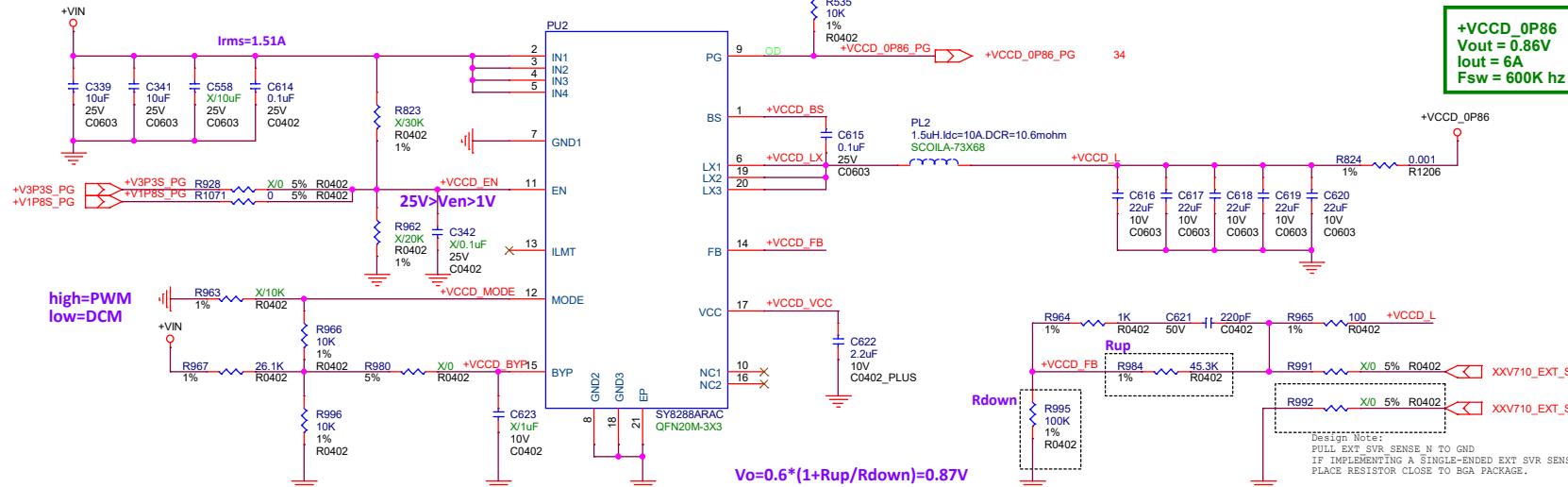
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A0.2_0_0

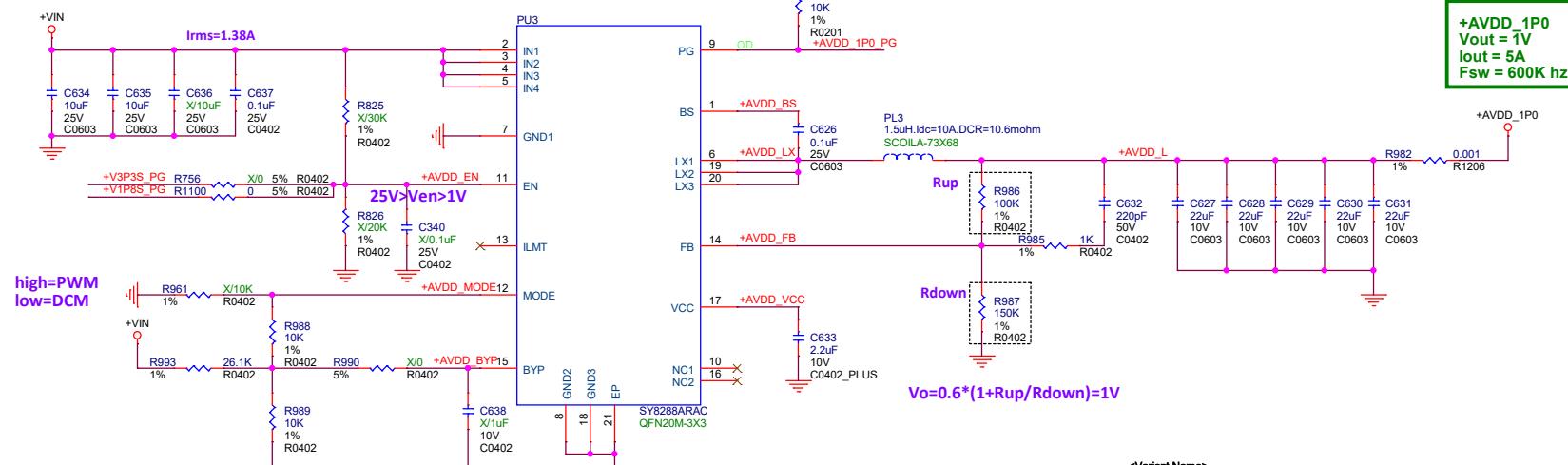
Date: Wednesday, April 20, 2022

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+VCCD_0P86@6A



+AVDD_1P0@5A



<Variant Name>

AAEON Technology INC.

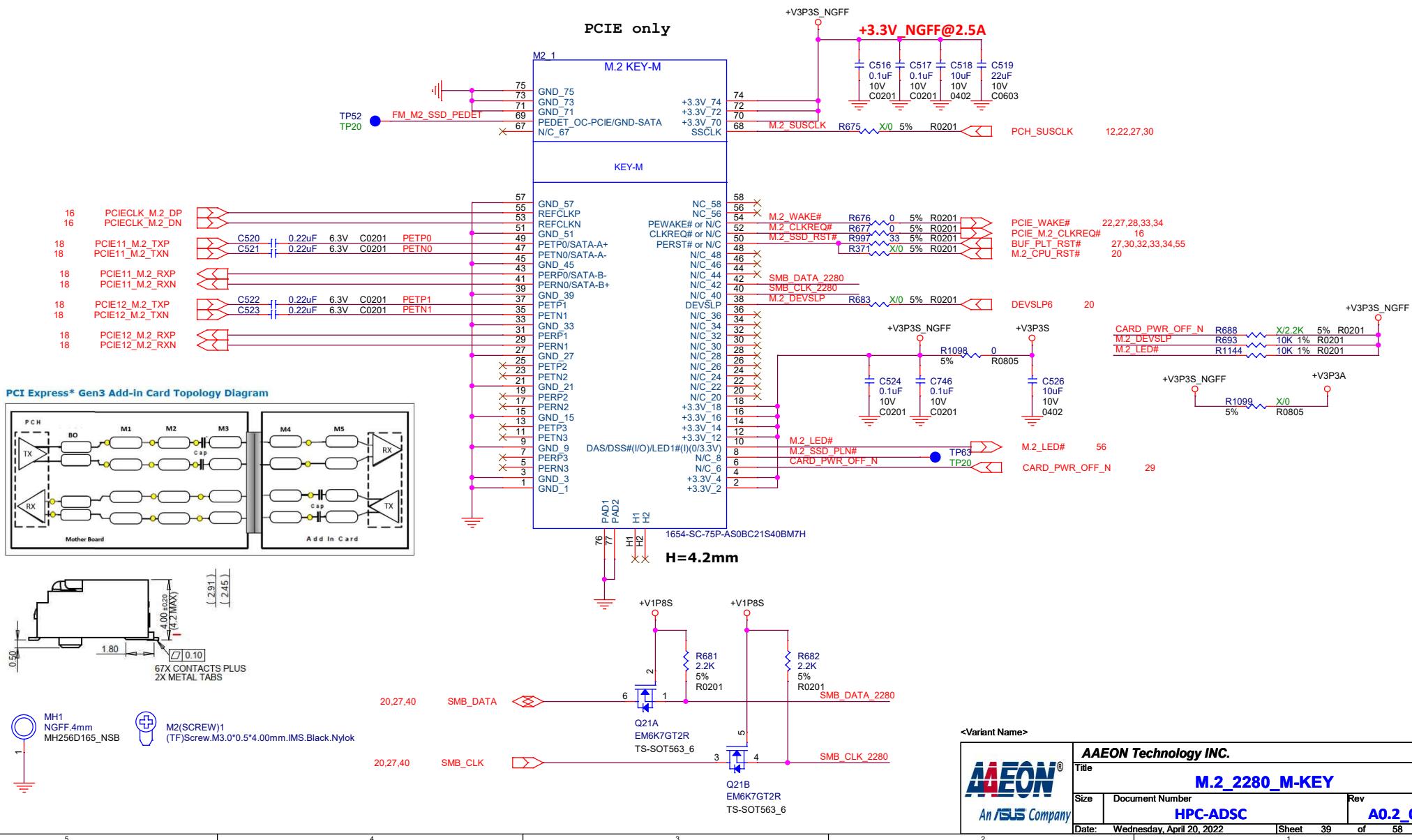
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Size Document Number Rev

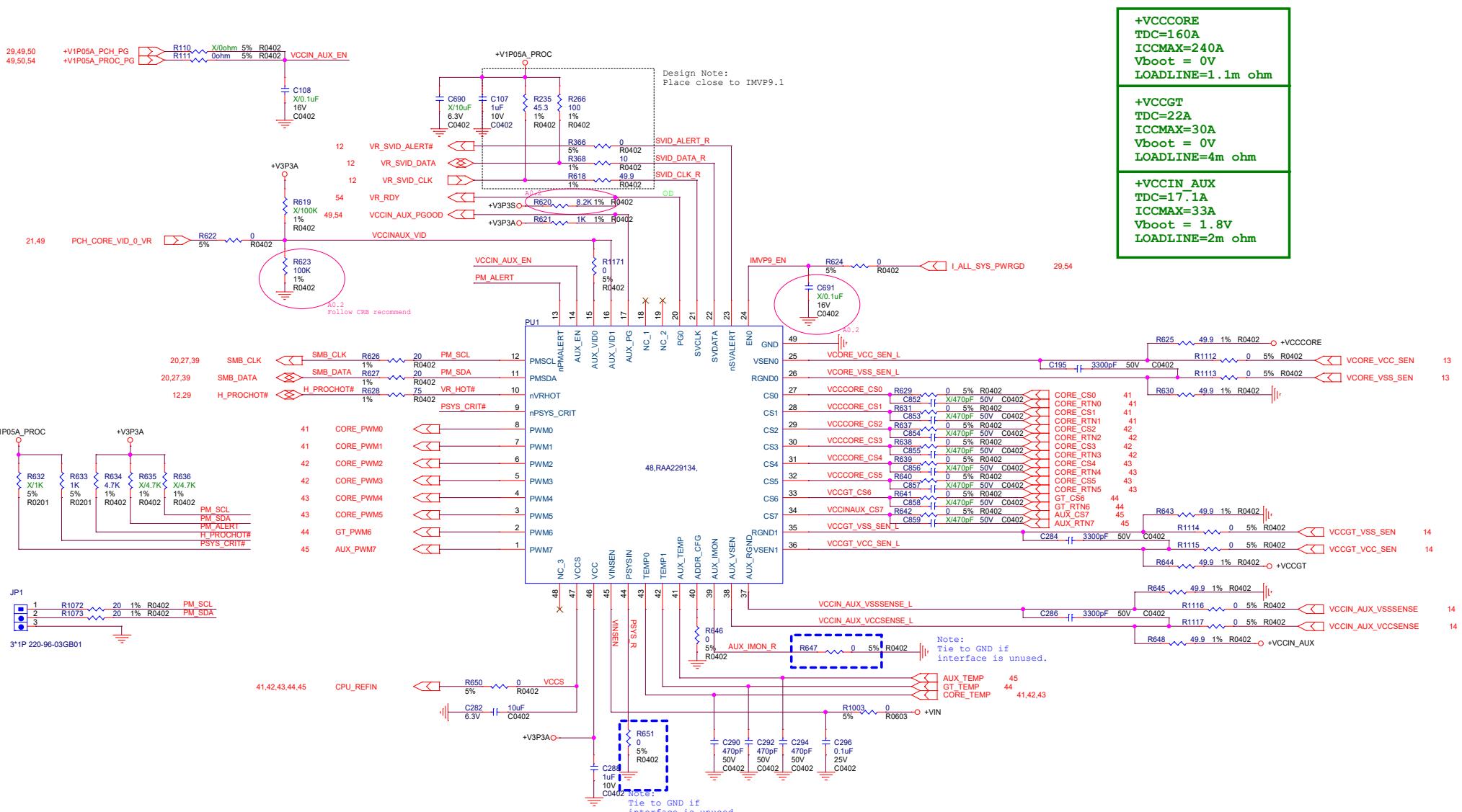
Custom HPC-ADSC A0.2_0_0

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M.2_2280_M-KEY

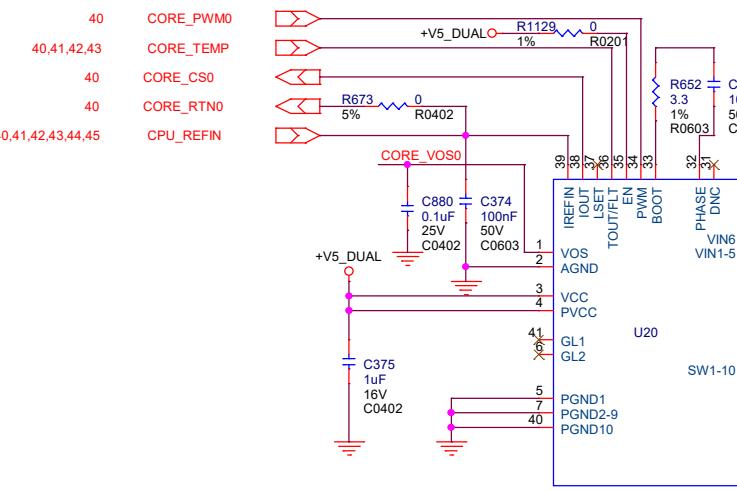


PMR_IMVP9.1@Total_240A

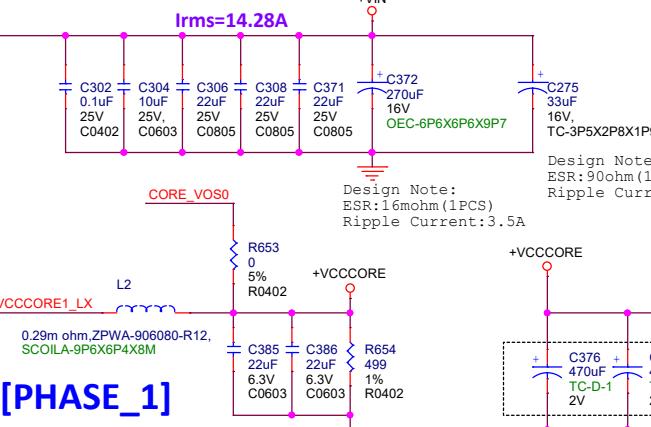


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		PWR_IMVP9 Controller	
Size	Document Number	Rev	
Custom		A0.2_0.0	
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PWR_+VCCCORE_Phase1/2

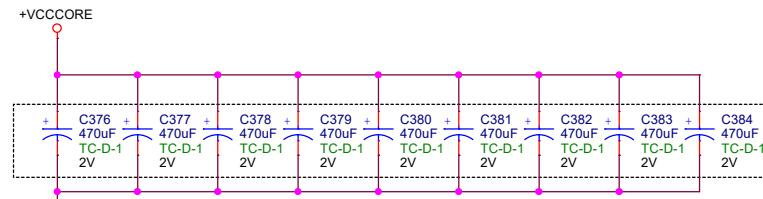


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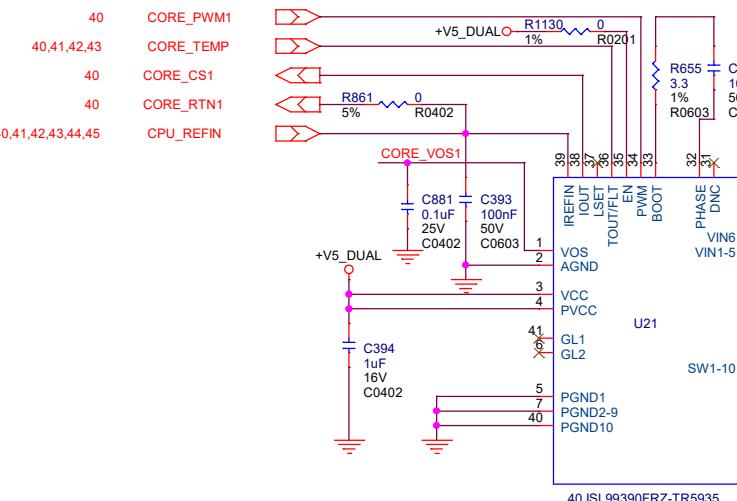


+VCCCORE
TDC=160A
ICCMAX=240A
LOADLINE=1.1m ohm
DCR=0.17mohm
OCP=130%~170%

Design Note:
ESR:16mohm(1PCS)
Ripple Current:3.5A



9 PCS 470uF OSCON OR SP



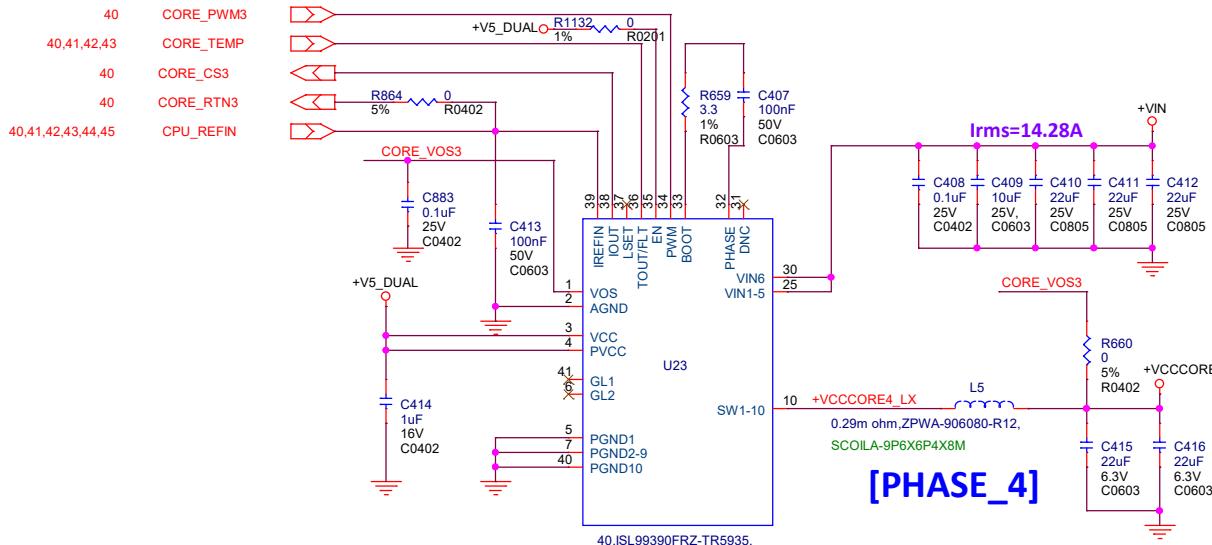
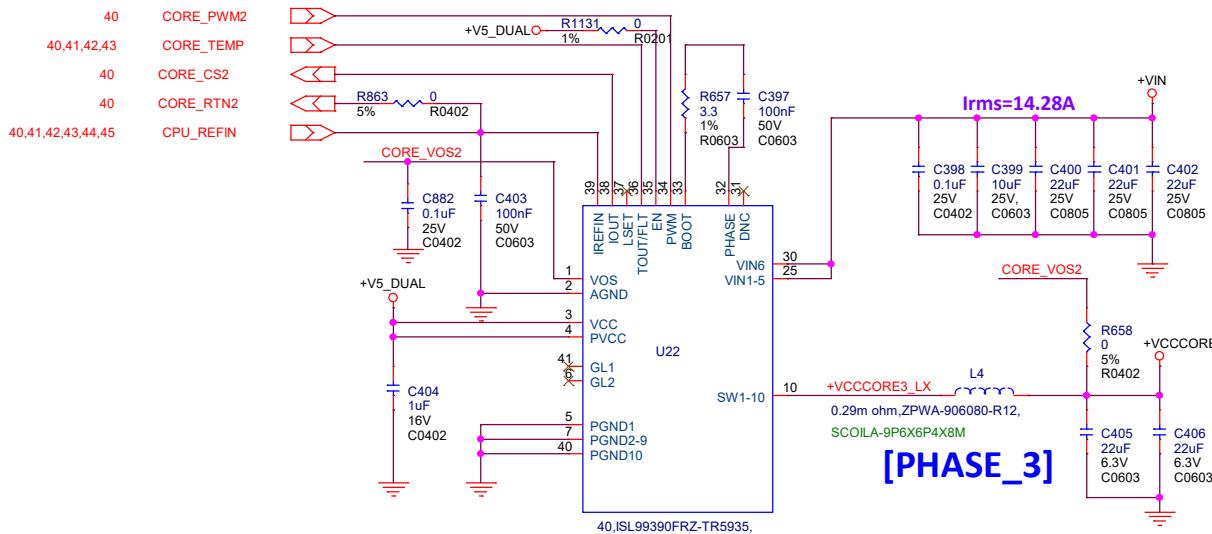
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Title	PWR_+VCCCORE
Size	Document Number
Custom	HPC-ADSC
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PWR_+VCCCORE_Phase3/4



<Variant Name>



AAEON Technology INC.

Title

PWR_+VCCCORE_Phase3/4

Size

Custom

Document Number

HPC-ADSC

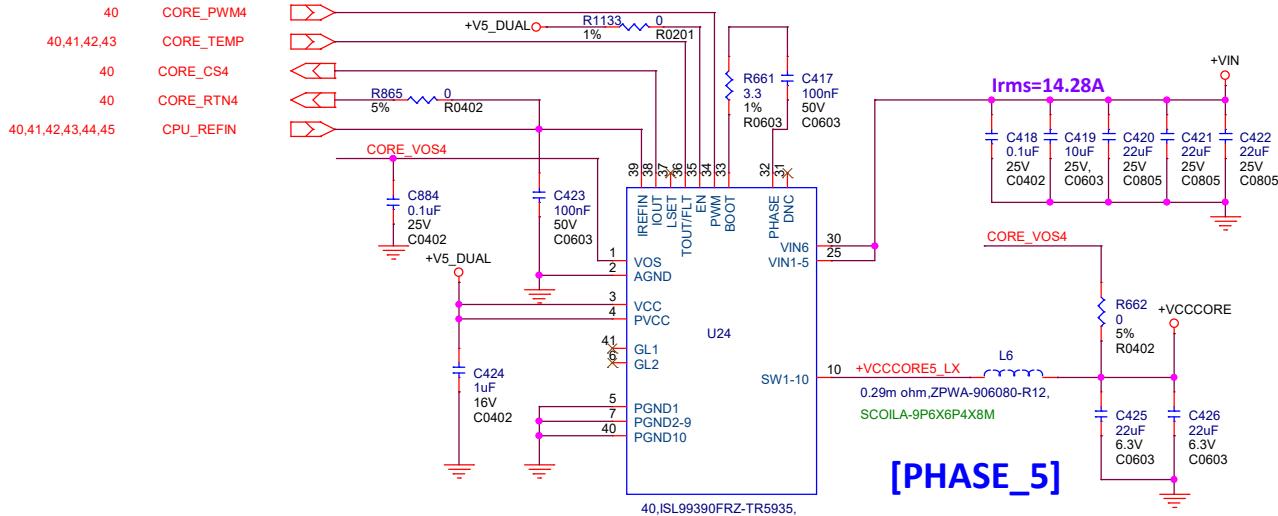
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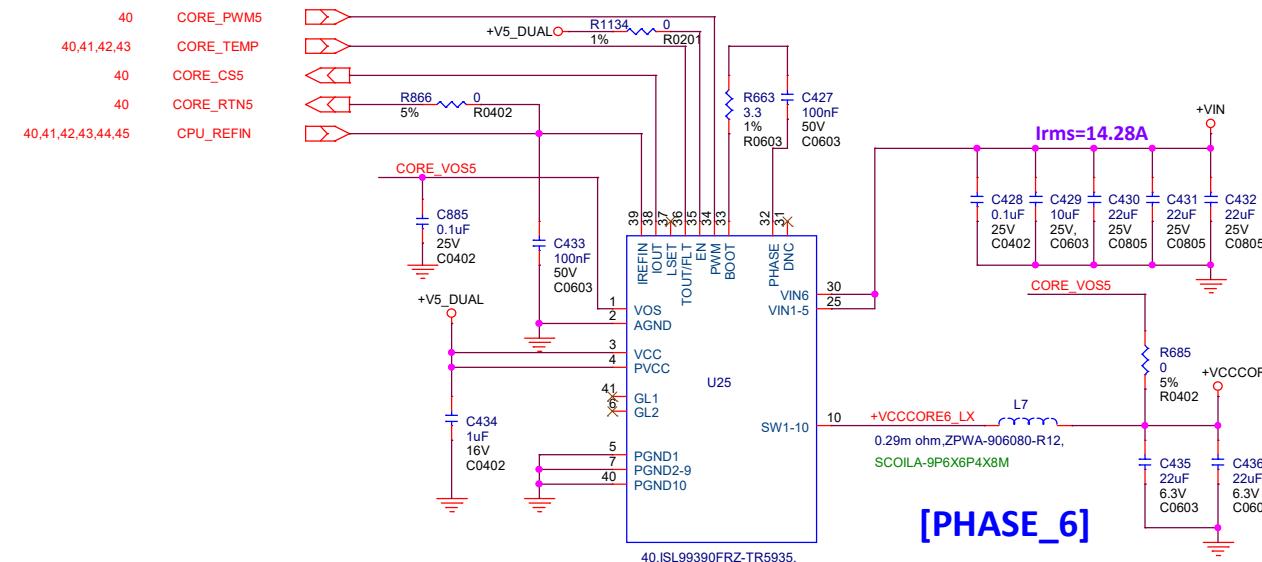
Date: Wednesday, April 20, 2022

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PWR_+VCCCORE_Phase5/6

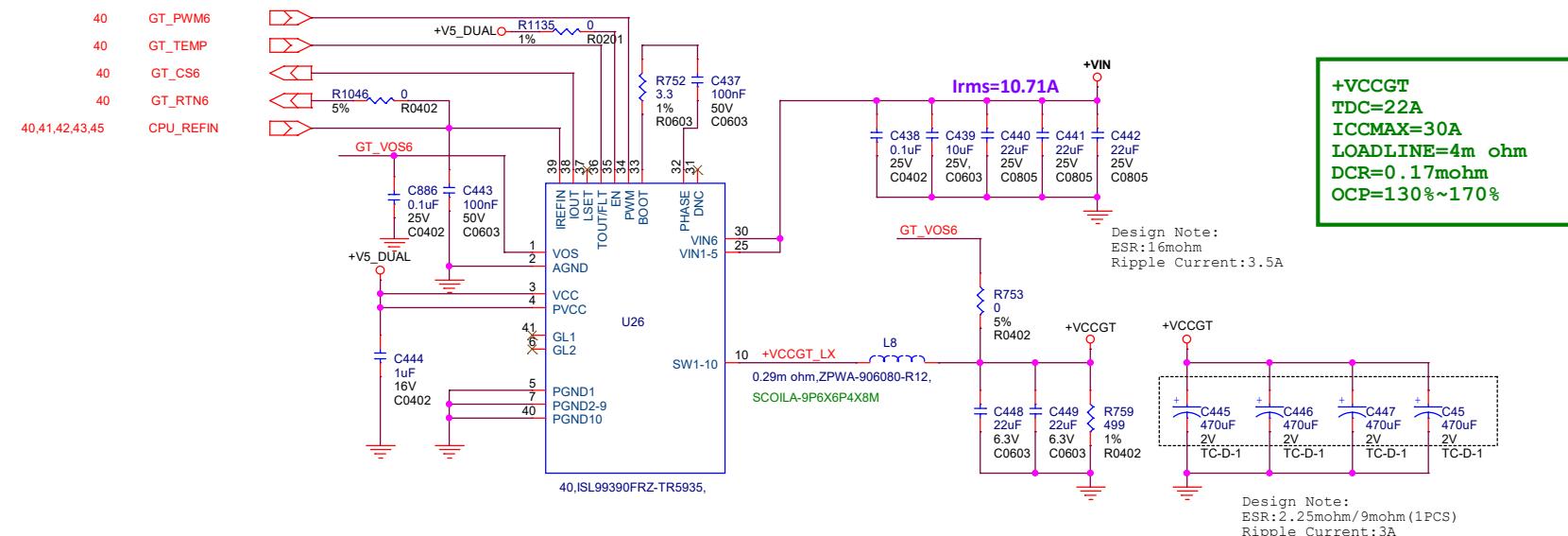


+VCCCORE
TDC=160A
ICCMAX=240A
LOADLINE=1.1m ohm
DCR=0.17mohm
OCP=130%~170%



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AAEON Technology INC.			
Title PWR_+VCCCORE_Phase5/6			
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Custom	HPC-ADSC	A0.2_0_0	
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PWR_+VCCGT@30A



4 PCS 470uF OSCON OR SP

<Variant Name>



AAEON Technology INC.

Title

PWR_+VCCGT

Size

Document Number

Rev

B

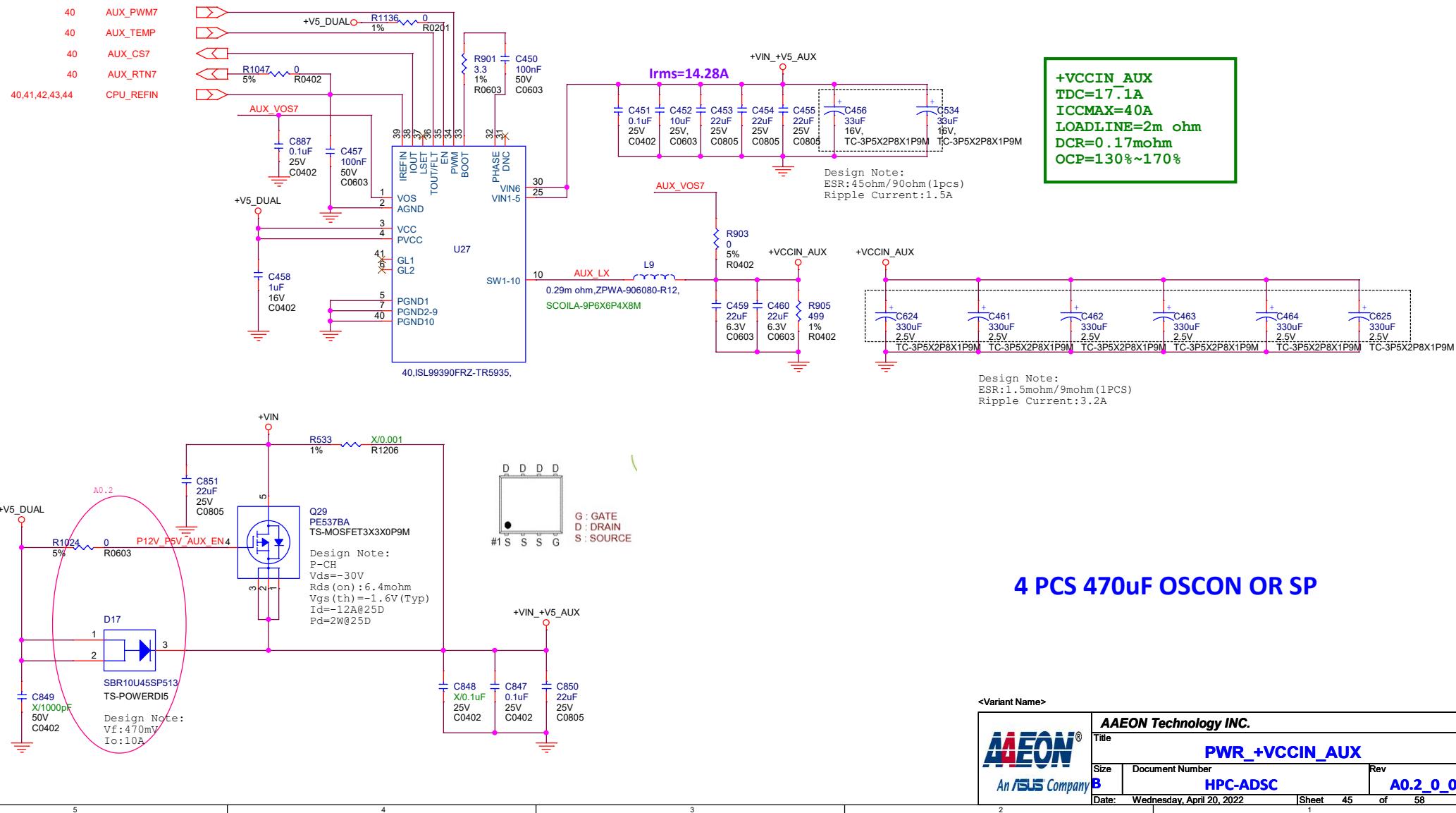
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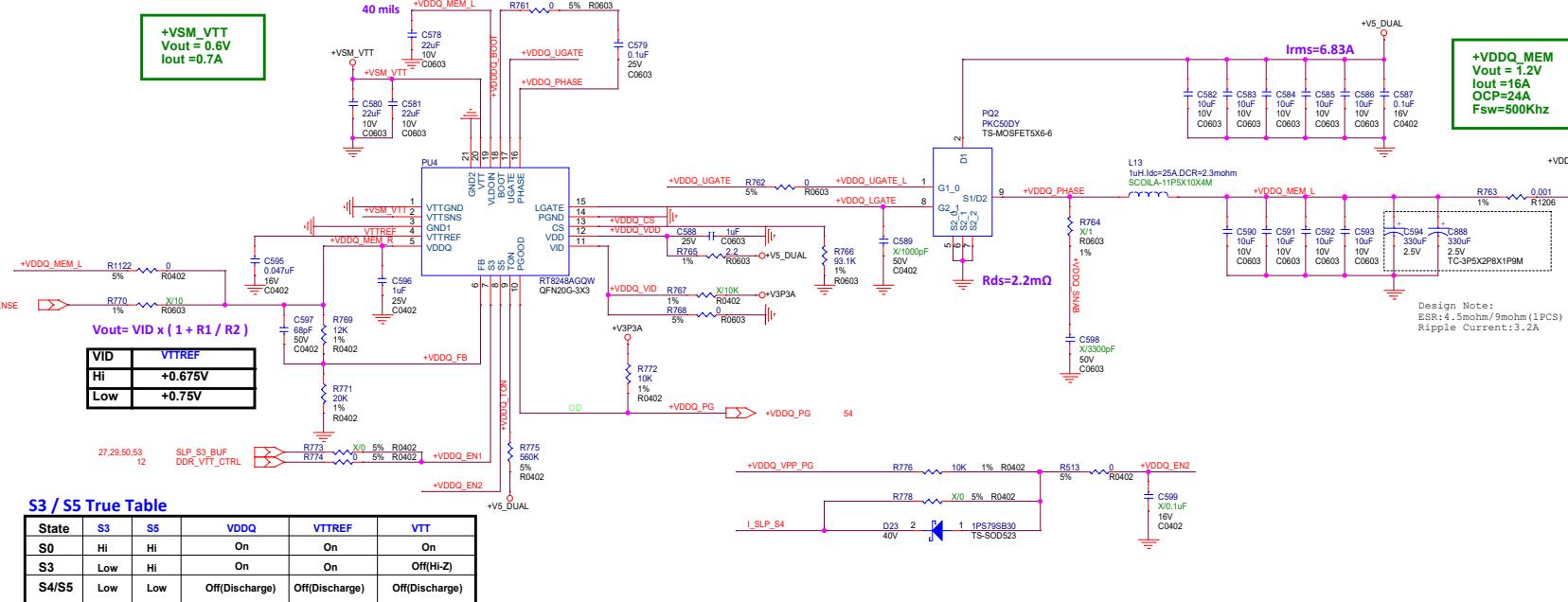
Date: Wednesday, April 20, 2022

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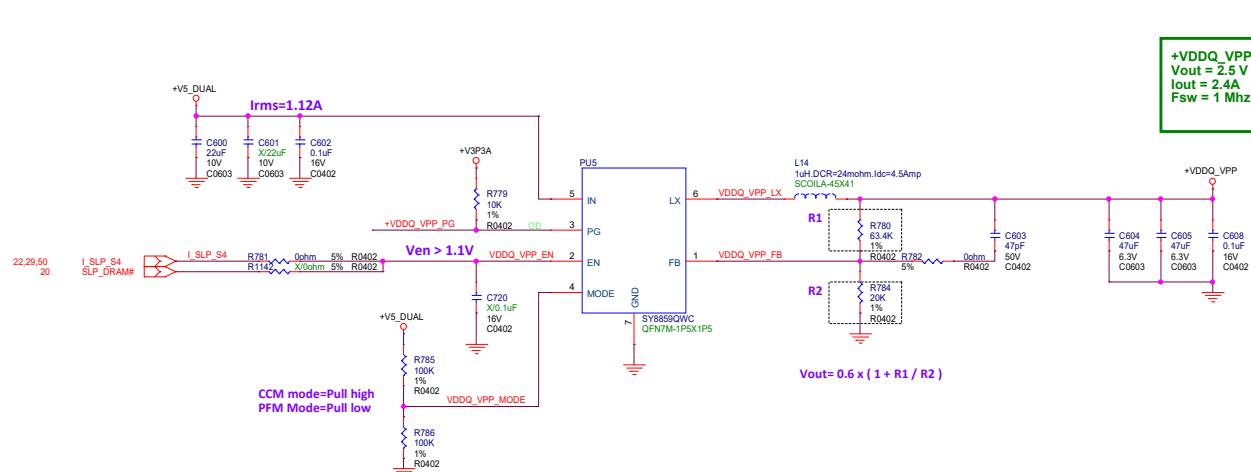
PMR_+VCCIN_AUX@40A



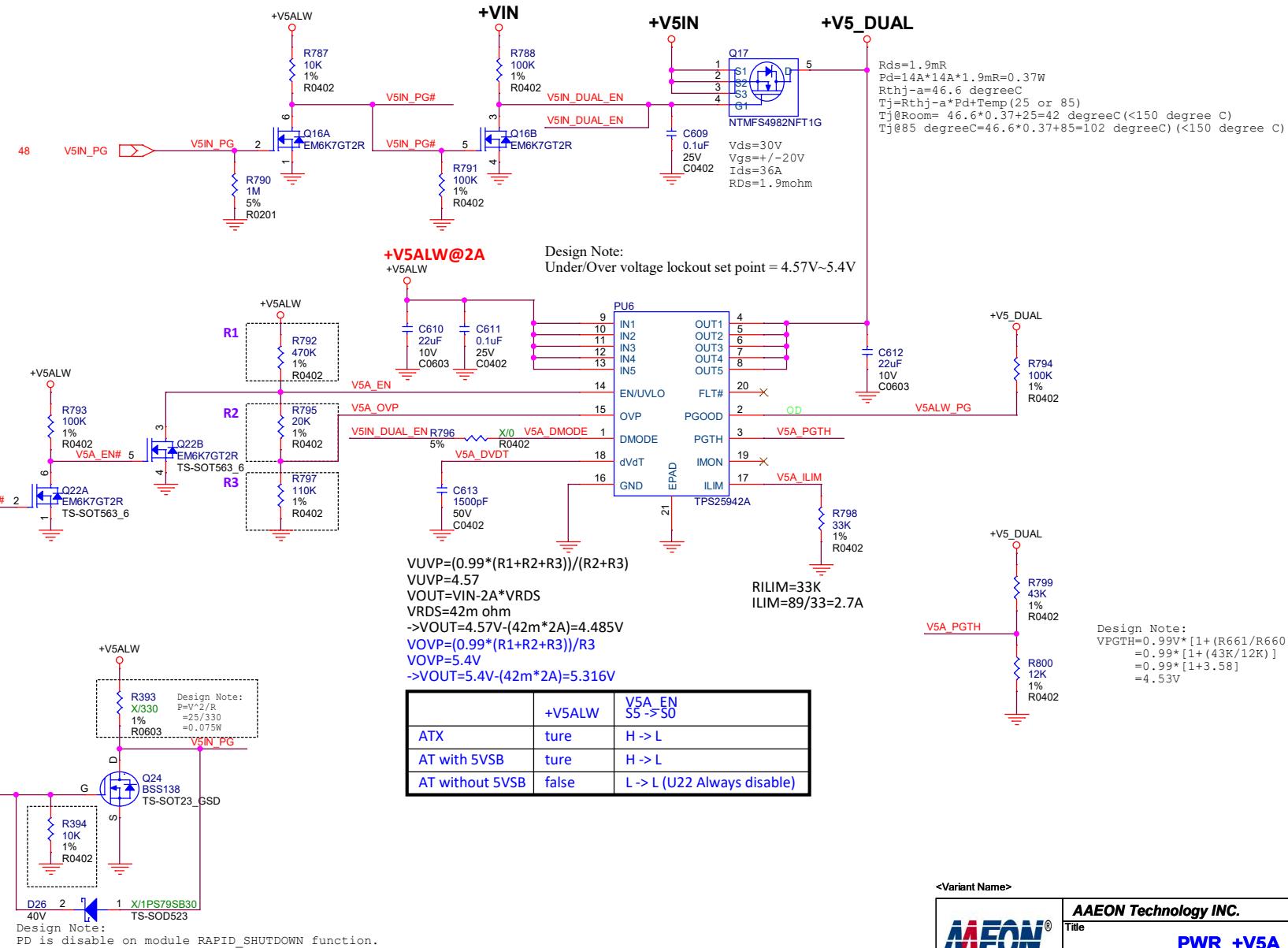
PWR_+VDDQ@16A/+VTT@0.7A



PWR_+VPP/2.4A

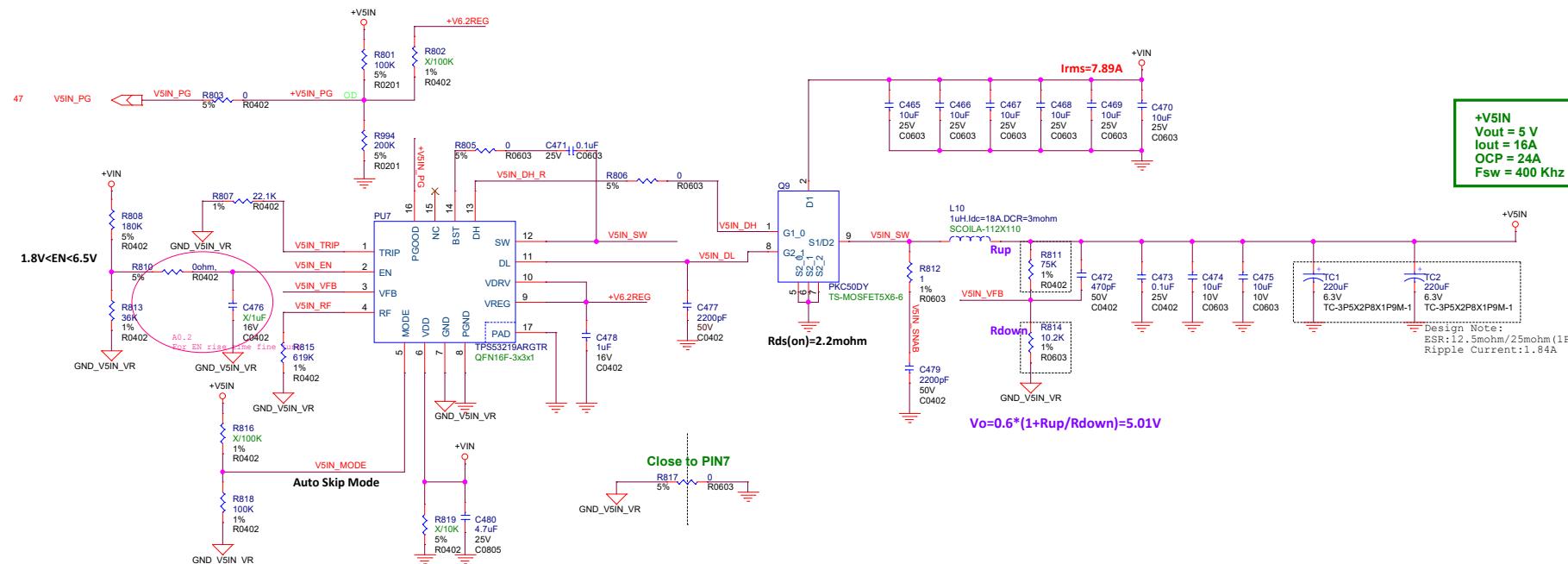


PWR_+V5A_DUAL@13A

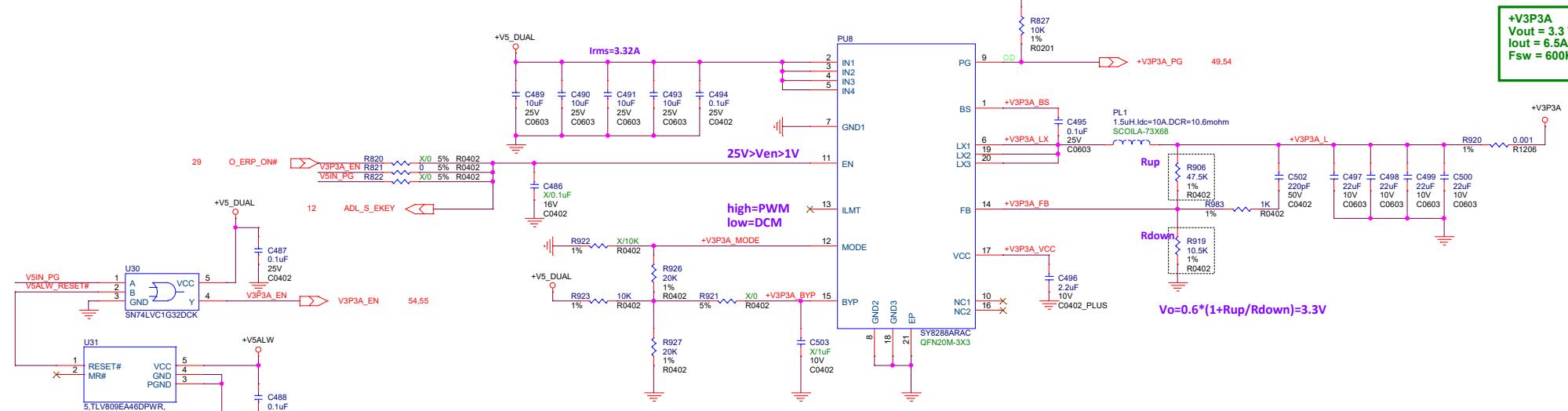


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AAEON Technology INC.			
Title			
AAEON	PWR_+V5A_DUAL		
An ASUS Company			
Size B	Document Number HPC-ADSC	Rev A0.2_0_0	
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+V5IN@16A



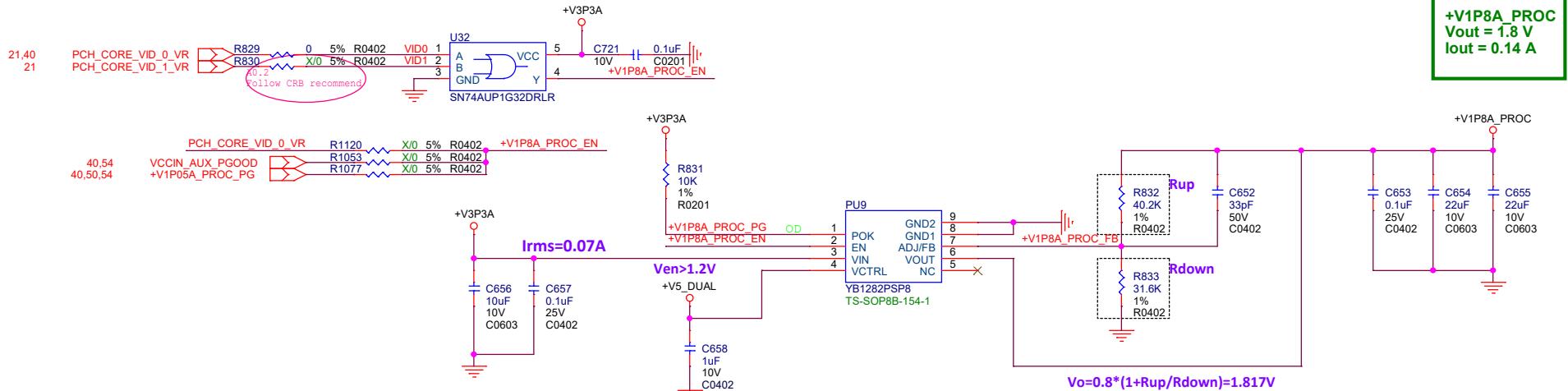
+V3P3A@6.5A



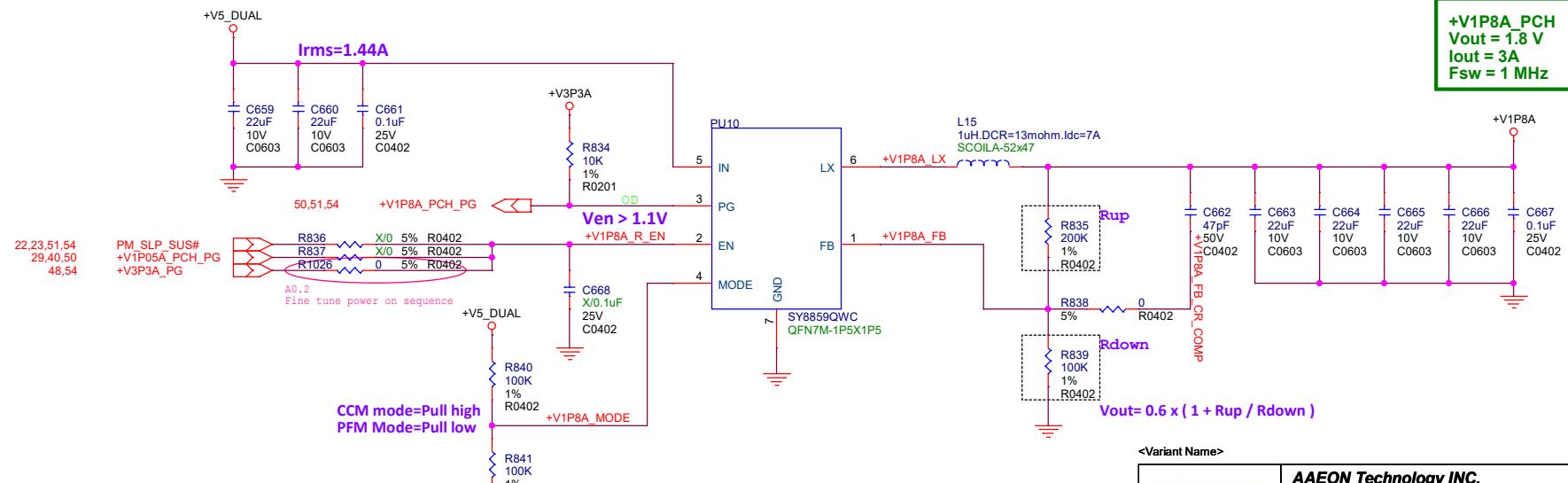
Design Note:
Fastly discharge RSMRST# power off sequence

<Variant Name>		AAEON Technology INC.	
		Title	
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Size	Document Number	CUSTOM	Rev
		HPC-ADSC	A0.2_00
Date:	Wednesday, April 20, 2022		
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+V1P8A_PROC@0.14A



+V1P8A@3A



<Variant Name>

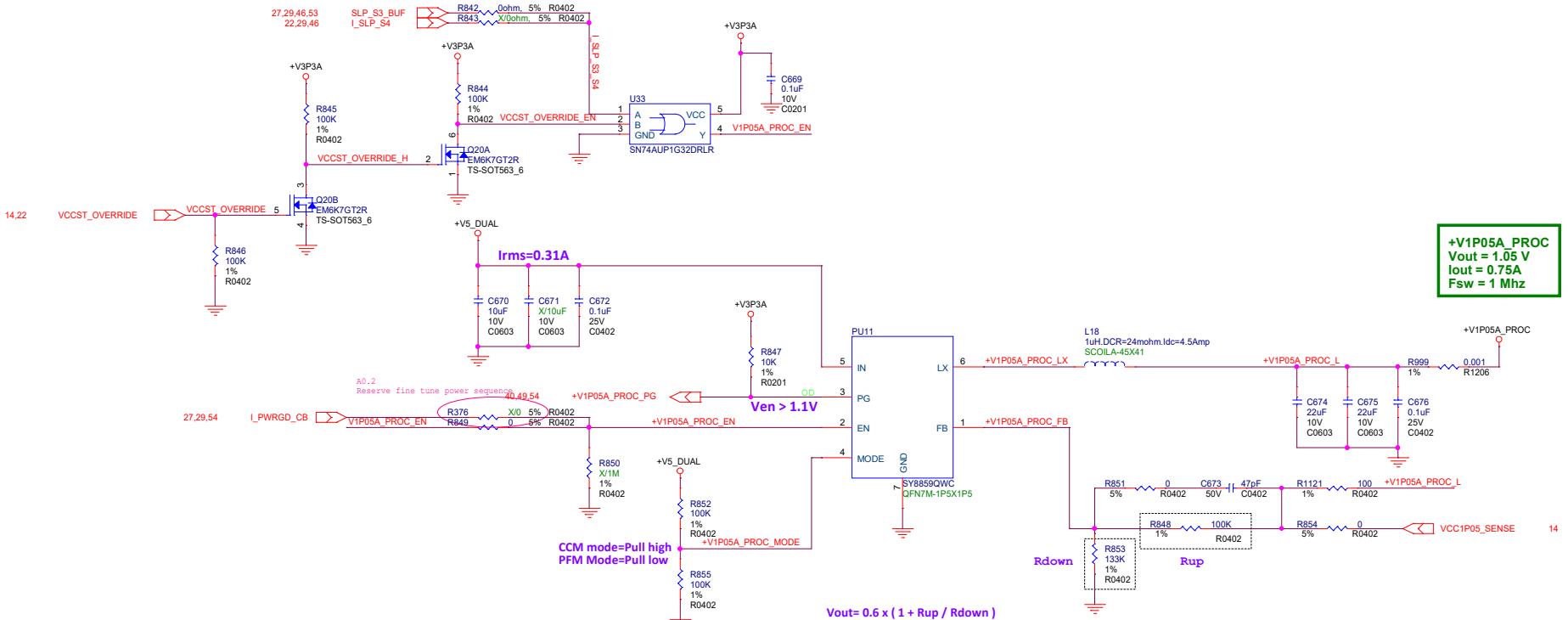


AAEON Technology INC.
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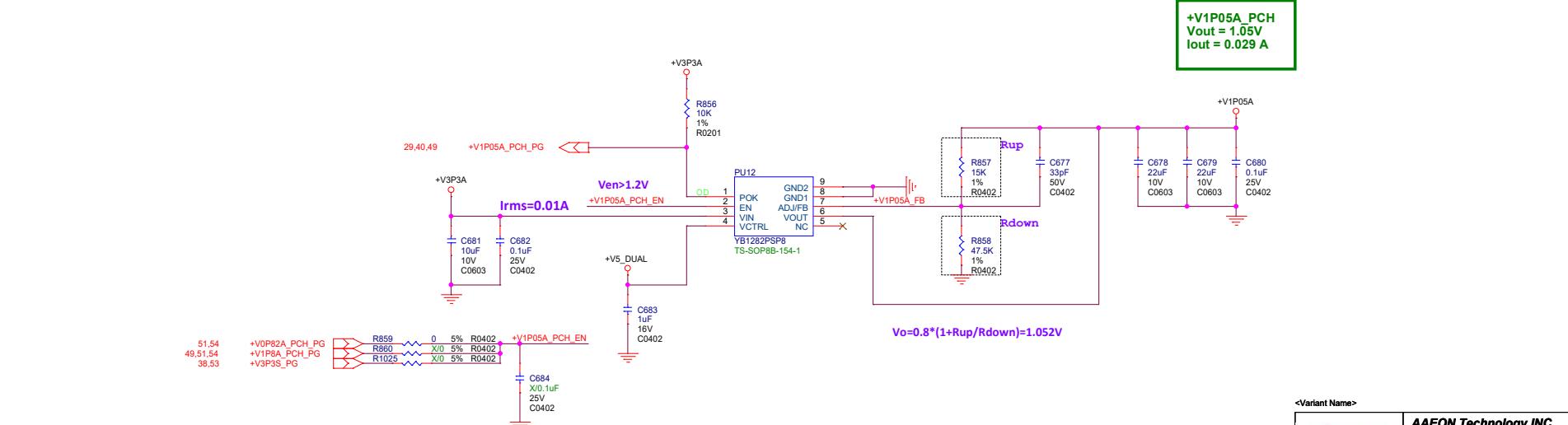
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+V1P05A_PROC@0.75A



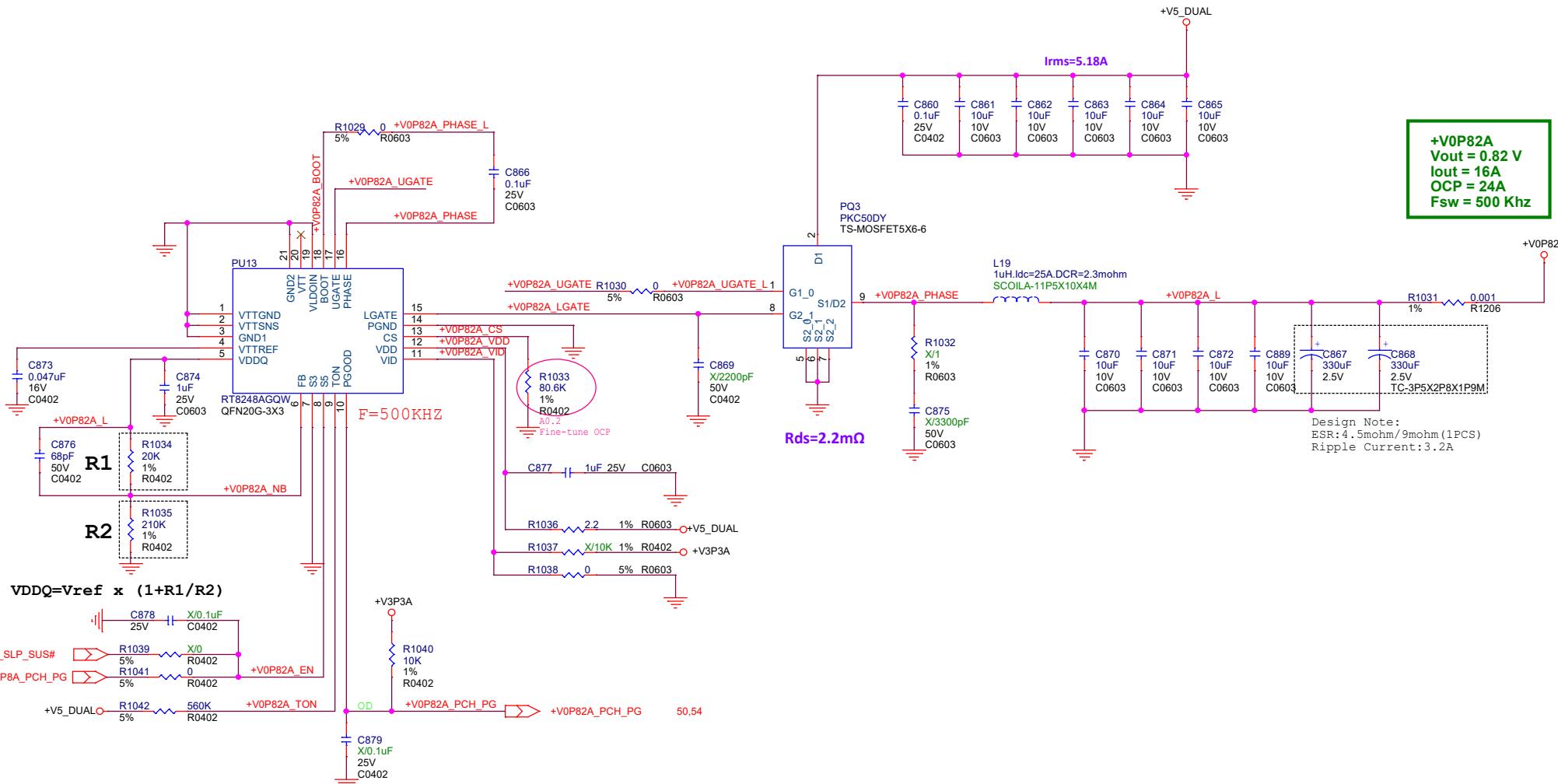
+V1P05A@0.029A



AAEON Technology INC.

<Variant Name>		
Title		
+V1P05A_PROC/+V1P05A	Document Number	Rev
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+VOP82A@16A



VOUT Select Table

VID	Reference Voltage
HI	+0.675V
Low	+0.75V

<Variant Name>



AAEON Technology INC.

Title

+VOP82A

Size

B

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PWR_+VIN@16A

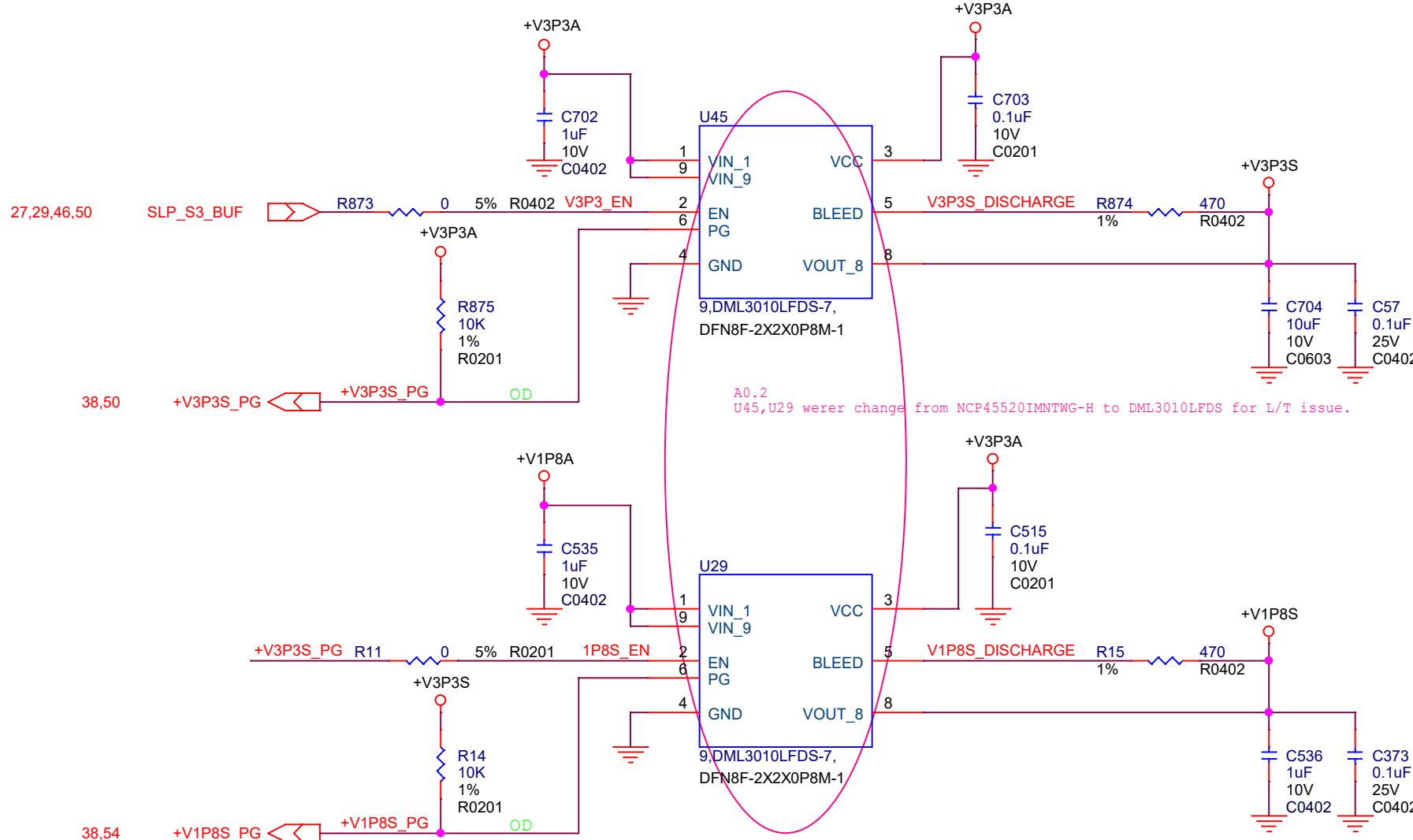
A0.2
Remove +VIN soft-start circuit.



AAEON[®]
An ASUS Company

<Variant Name>		AAEON Technology INC.	
		Title	
		PWR_+VIN	
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A	HPC-ADSC		A0.2_0_0
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SYSTEM POWER



R _{ON} TYP	V _{CC}	V _{IN}	I _{MAX_DC} *
9.5 mΩ	3.3 V	1.8 V	10.5 A
10.1 mΩ	3.3 V	5.0 V	
12.8 mΩ	3.3 V	12 V	

*I_{MAX_DC} is defined as the maximum steady state current the load switch can pass at room ambient temperature without entering thermal lockout.

<Variant Name>



AAEON Technology INC.

Title

SYSTEM POWER

Size Document Number

HPC-ADSC

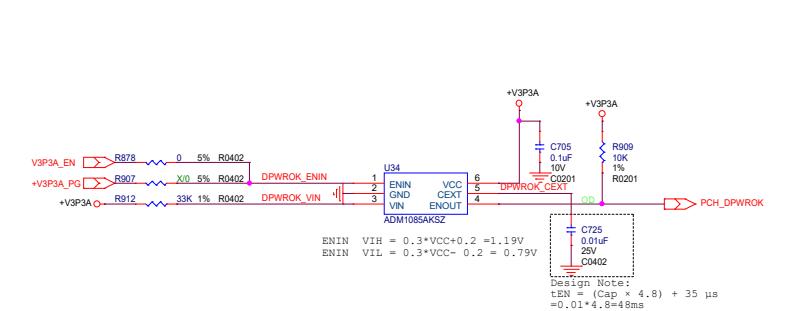
Rev **A0.2_0_0**

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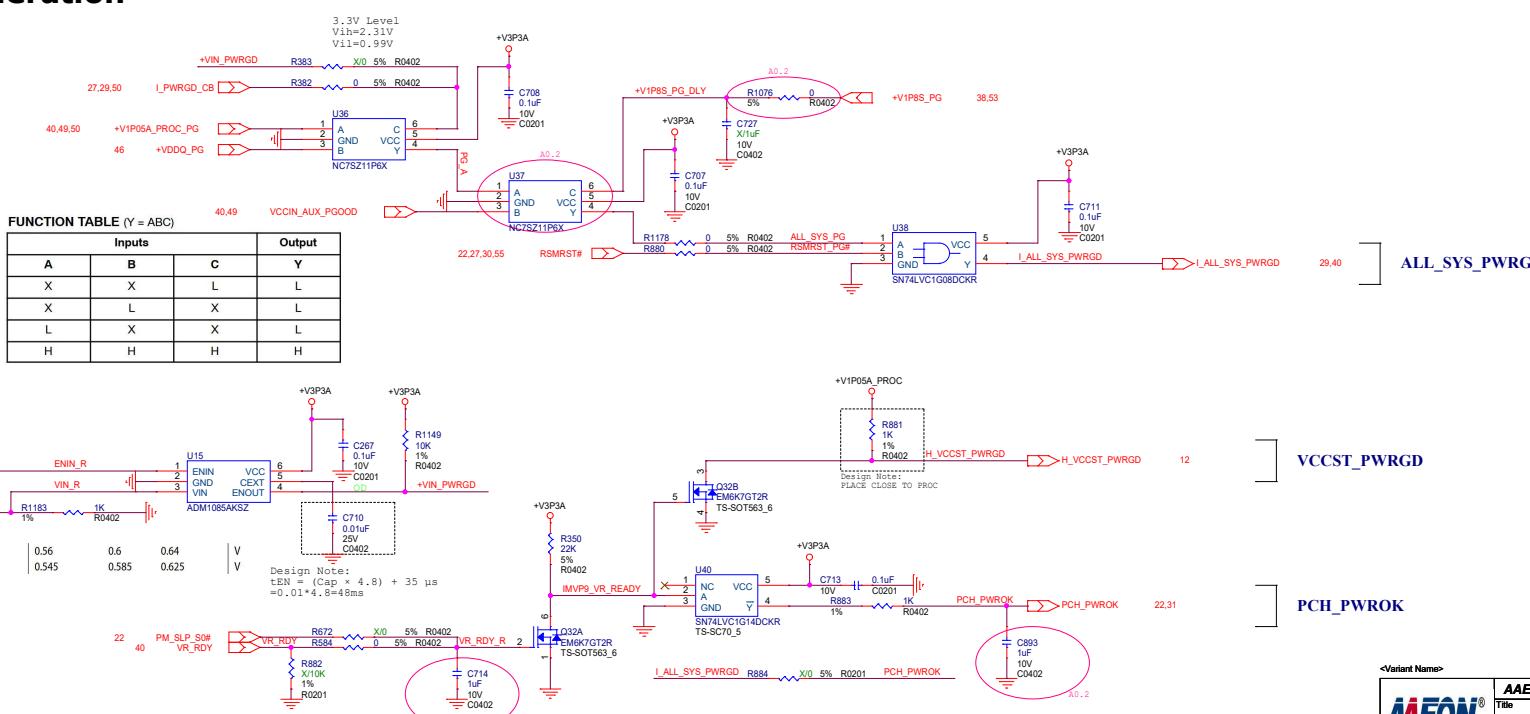
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DSW_PWROK Generation

RSMRST#_PWRGD Generation

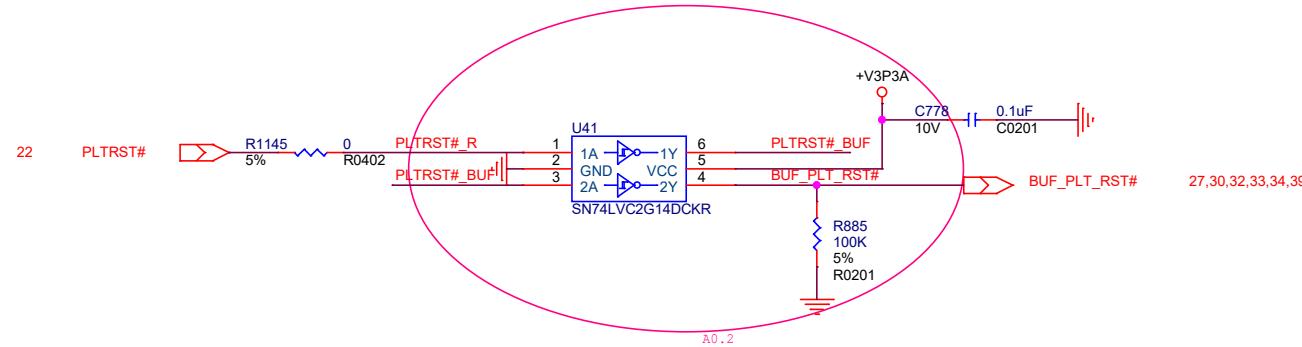


PWROK Generation



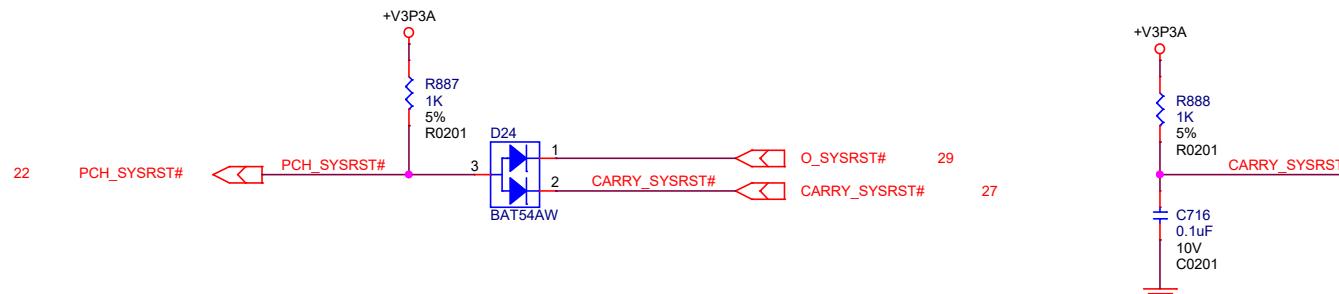
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BOOT SEQUENCE		Title	
Size	Document Number	Rev	
C	HPC-ADSC	A0.2.0.0	
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PLTRST#

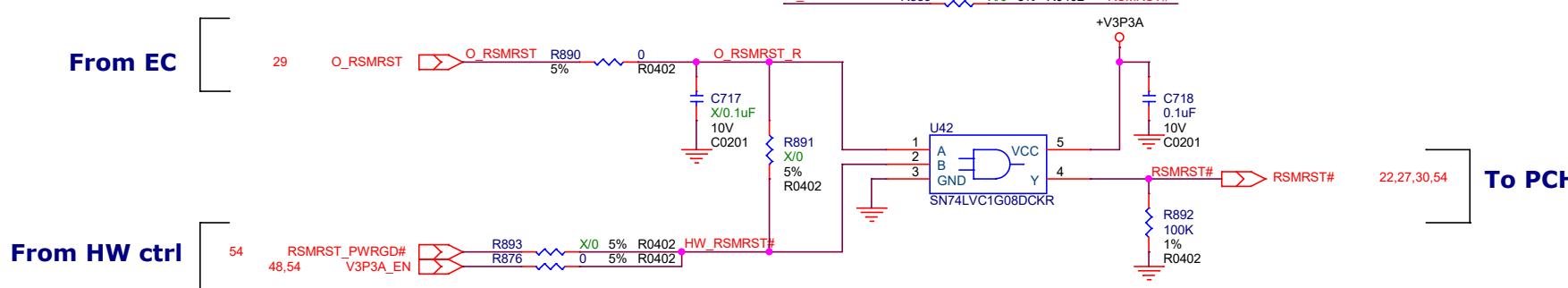


Carrier Board
LPC
LAN1/LAN2
M.2
EC
TPM
Port 80

SYSRST#

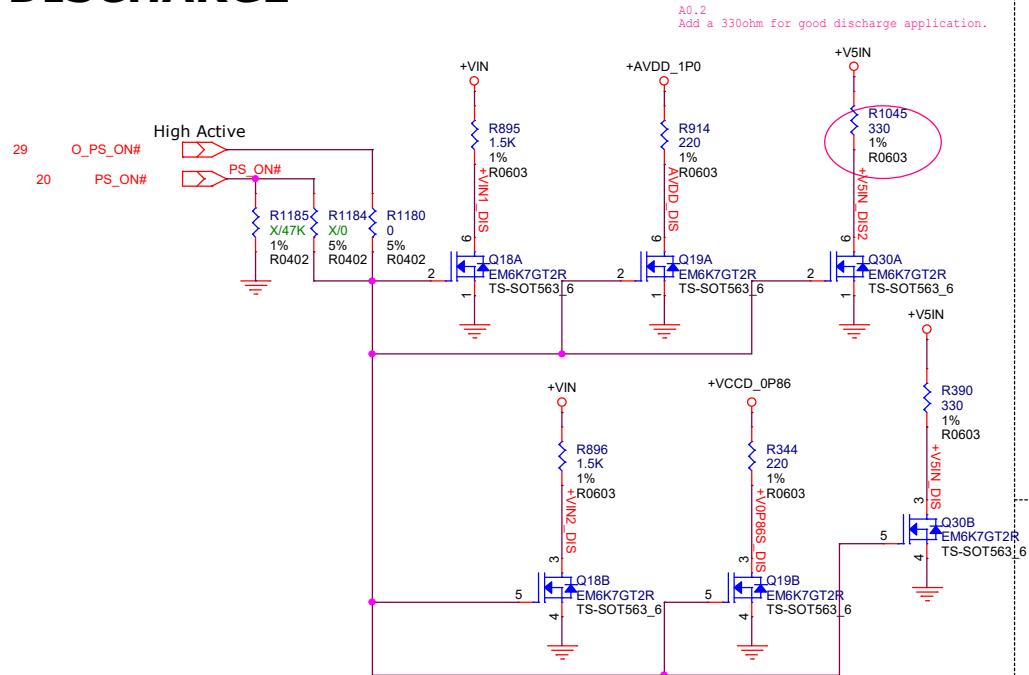


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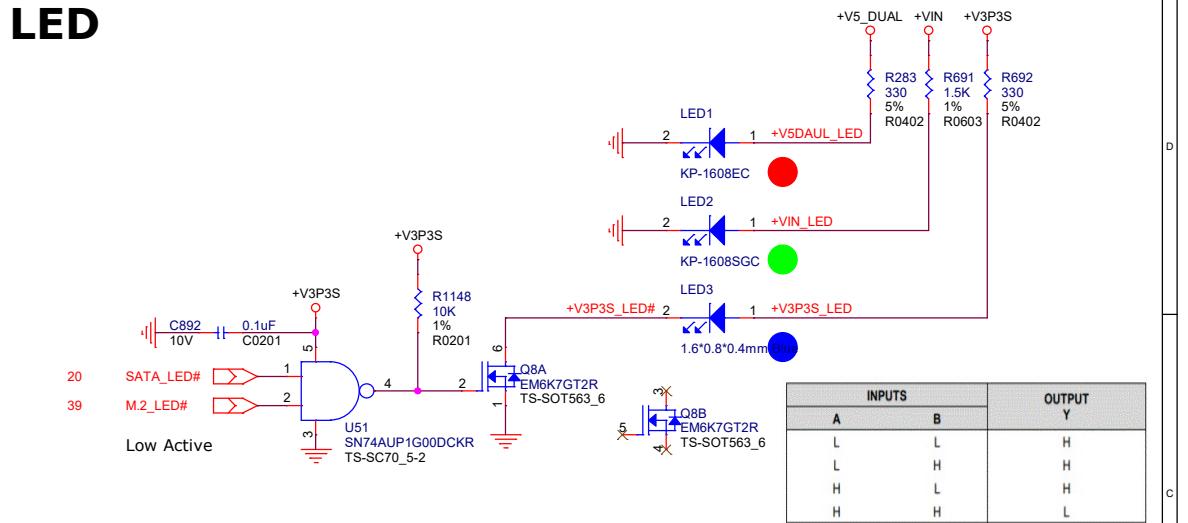


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AAEON Technology INC.	Title	
Aeon An ASUS Company	RESET# LOGIC	
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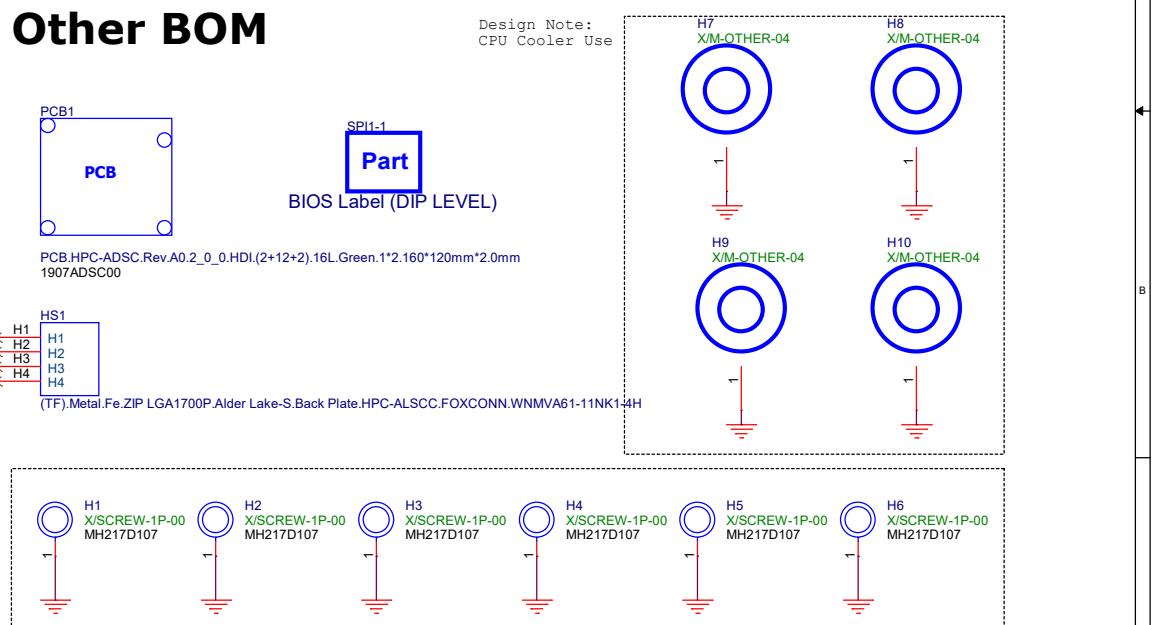
DISCHARGE



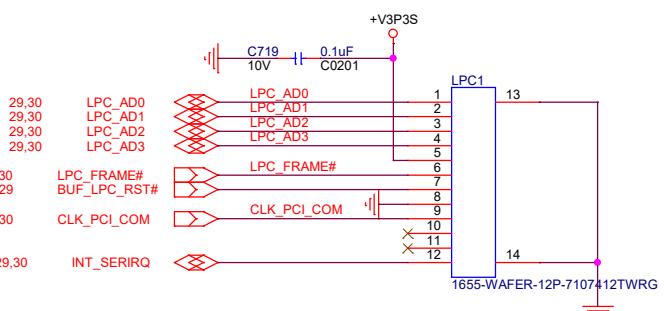
LED



Other BOM



Port 80



Reference DoC

Intel No	Description
627373	IOTG_Alder_Lake_S_Platform_Gold_Deck_Rev 1.1
619501	adl-processor-eds-vol1-rev0p8
619502	ADL_S_Processor_EDS_Vol2a_Rev0p8
619362	adl-s-pch-eds-vol1-rev1p2
621483	ADL_PCH_S_EDS_Vol2_Rev1p0
626732	adl_s_pch_electric_therml_spec_rev1p2
619508	ADL_S_PDG_Rev1.2
626774	ADL_MOW_WW12_2021
626775	ADL_MOW_Archive_WW12_2021
633589	ADL_S_with_ADL_S_PCH_DDR4_SODIMM_1DPC_RVP_SCH_Rev_1p0
619508	ADL_S_SchChk_Rev1.2
332464	710_Series_Datasheet_v_3_9
569998	xxv710-fv1-25-reference-schematics-v1-4
	PICMG_COM_HPC_100-obvmf2
	PICMG_COMHPC_CDG_R1_0

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HPC-ADSCC Revision History

HPC-ALSCC A0.1_0_0 PCB: 1907ALSC00 BOM: Date: 2021/05/19

First Initial.

HPC-ADSC A0.2_0_0 PCB: 1907ADSC00 BOM: Date: 2022/04/06

Schematics Modified	Layout change (need/ok)	BOM change (need/ok)	Description	Page
OK	need	X	01. Modify SVID DATA,CLK,Alert# path for boot up abnormal issue.	12
OK	need	need	02. Add R380_10K resistor for PCIE x1 clock request use.	16
X	X	need	03. Empty UART PU resistors for leakage current issue.	20
OK	need	need	04. Add R573 Ohm resistor for fine-tune power sequence.	22
OK	need	need	05. Fix DDI0 and DDI1 hot plug design issue.	27
OK	need	need	06. Reserve SMLink patch for debug requirement.	27
OK	need	need	07. Reserve C74_0.1uF for fine-tune +V3P3A_EC rise time.	29
OK	need	need	08. Remove isolate circuit for signal reflection issue.	29
OK	need	need	09. Remove SW1 switch for space consider.	29
OK	need	need	10. Remove SPI isolate circuit for boot up unstable issue.	31
OK	need	need	11. Q11 change MOS part from EM6K7GT2R to BSS138 for measure easy requirement.	31
OK	need	need	12. Modify path for PCIE type M.2 use.	39
OK	need	need	13. Stuff R623_100K for follow Intel CRB recommend.	40
OK	need	need	14. R620 change from 1K to 8.2K for fine-tune power sequence fail issue.	40
OK	need	need	15. Stuff R1024_Ohm and D17 for meet follow power on sequence recommend.	45
OK	need	need	16. C476 change from 1000pF to 1uF for fine-tune +V5IN rise time.	48
OK	need	need	17. Remove R830 for follow Intel CRB recommend.	49
OK	need	need	18. Stuff R1026 for support non-deep issue.	49
OK	need	need	19. Reserve R376_Ohm for fine-tune power on sequence.	50
OK	need	need	20. Remove +VIN soft-start circuit for current path margin issue.	52
OK	need	need	21. U45,U29 werer change from NCP45520IMNTWG-H to DML3010LFDS for L/T issue.	53
OK	need	need	22. Stuff C174_1uF and add C893_1uF for power off sequence fail issue.	54
OK	need	need	23. Add R1076_Ohm/R1167_10K for easy fine-tune power sequence application.	54
OK	need	need	24. Change DIO patch from EC to PCH for read slow issue.	20,22
OK	need	need	25. Stuff ESPI Oohm for carrier board Port80 application.	27
OK	need	need	26. U41 was changed from SN74LVC126APWR to SN74LVC2G14DCKR for L/T issue.	55
OK	X	X	27. Add a 330ohm for +V5IN good discharge.	56
OK	need	need	28. Add a R1166_1K for follow CRB recommend.	22

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