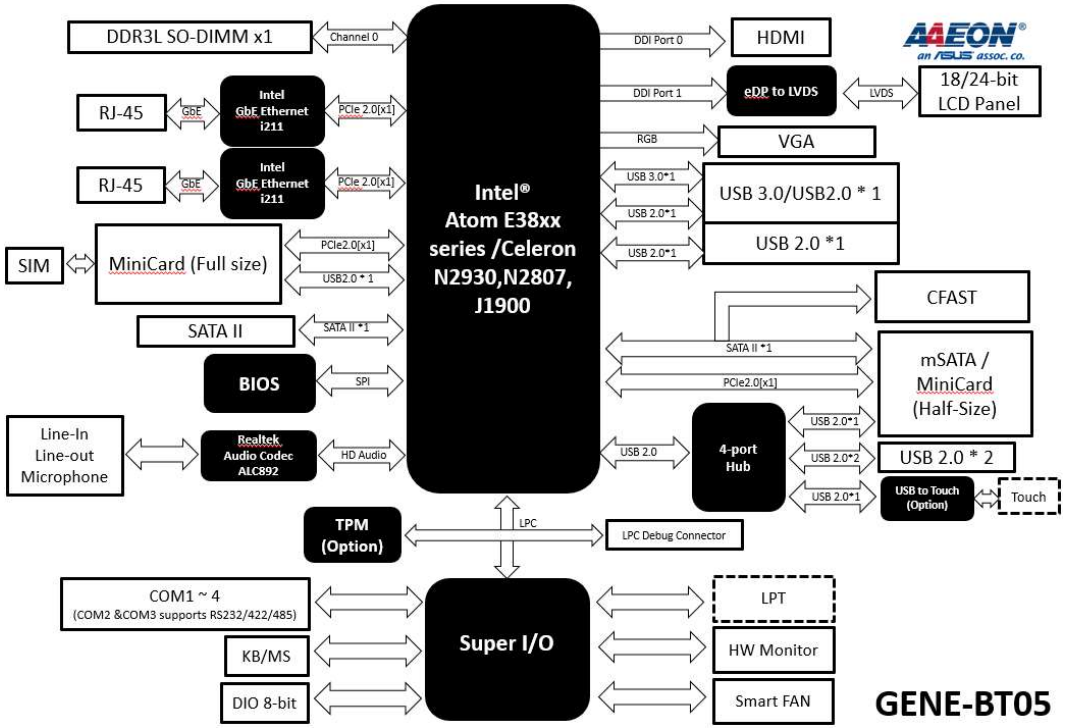
GENE-BT05 Rev.A1.2_0_0

Sub Compact Board

Intel Bay Trail-D / Bay Trail-M / Bay Trail-I Platform Cross Compatibility



-----Bit 4,3,2,1,0-----
Advanced Version: 00000
Standard Version: 00001

****
1.CFast and mSATA CO-LAY
2.mSATA and Mini Card CO-LAY
(BOM Change)
****

Project Number : E130607
Production Line : Sub.ESB.AASM

Title: Cover Sheet			
Size: Custom	Document Number: GENE-BT05		Rev: A1.2_0_0
Date: Monday, March 15, 2021		Sheet: 1 of 43	

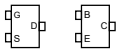
SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_S0_SC[00]	1.8V Core	20k,L	SATA_GP[0]
GPIO_S0_SC[01]	1.8V Core	20k,L	SATA_GP[1]
GPIO_S0_SC[07]	1.8V Core	20k,H	SD3_WP
GPIO_S0_SC[55]	1.8V Core	20k,L	
GPIO_S0_SC[56]	1.8V Core		--
GPIO_S0_SC[57]	1.8V Core	20k,H	
GPIO_S0_SC[58]	1.8V Core	20k,L	
GPIO_S0_SC[59]	1.8V Core	20k,L	LVDS_RBIT0
GPIO_S0_SC[60]	1.8V Core	20k,L	LVDS_RBIT1
GPIO_S0_SC[61]	1.8V Core	20k,H	LVDS_RBIT2
GPIO_S0_SC[92]	1.8V Core	20k,H	LVDS_RBIT3
GPIO_S0_SC[93]	1.8V Core	20k,H	LVDS_RBIT4
GPIO_S0_SC[94]	1.8V Core	20k,L	TOUCH_INT_1P8
GPIO_S0_SC[95]	1.8V Core	20k,L	TOUCH_RST#_1P8
GPIO_S5[00]	1.8V Suspend	20k,H	WAKE_RI#
GPIO_S5[01]	1.8V Suspend	20k,H	GPIO_PME#
GPIO_S5[02]	1.8V Suspend	20k,H	
GPIO_S5[03]	1.8V Suspend	20k,H	
GPIO_S5[04]	1.8V Suspend	20k,L	
GPIO_S5[05]	1.8V Suspend	20k,L	
GPIO_S5[06]	1.8V Suspend	20k,L	
GPIO_S5[07]	1.8V Suspend	20k,L	
GPIO_S5[08]	1.8V Suspend	20k,L	
GPIO_S5[09]	1.8V Suspend	20k,L	
GPIO_S5[10]	1.8V Suspend	20k,H	
GPIO_S5[17]	1.8V Suspend	20k,H	
GPIO_S5[22]	1.8V Suspend	20k,L	V3.3A_TCHC_EN
GPIO_S5[23]	1.8V Suspend	20k,L	
GPIO_S5[24]	1.8V Suspend	20k,L	
GPIO_S5[25]	1.8V Suspend	20k,L	
GPIO_S5[26]	1.8V Suspend	20k,L	
GPIO_S5[27]	1.8V Suspend	20k,H	
GPIO_S5[28]	1.8V Suspend	20k,H	
GPIO_S5[29]	1.8V Suspend	20k,H	
GPIO_S5[30]	1.8V Suspend	20k,H	

SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD_Backlight_Contoller	5Ch
CMOS_Backup_EEPROM	AEh
GPIO_IC	6Eh
PTN3460_Slave	C0h

PCB Footprints



PCB STACK :

Impedence 55ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : Signal
- Layer 5 : POWER
- Layer 6 : Signal
- Layer 7 : GND
- Layer 8 : Solder

F81866D GPIO Pins :

Name	Tolerance	Power Well	Default	Function	
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#	
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#	
GPIO02	5V	I_VSB3V	Native	PM_SUS_WARN#	
GPIO03	5V	I_VSB3V	Native	PM_SUS_ACK#	
GPIO04	5V	I_VSB3V	Native	PM_SLP_SUS#	
GPIO05	5V	I_VSB3V	Native	LAN1_DISABLE#	
GPIO06	5V	I_VSB3V	Native	LAN2_DISABLE#	
GPIO07	5V	I_VSB3V	Native	W_DISABLE0#	
GPIO10	5V	I_VSB3V	Native	W_DISABLE1#	
GPIO11	5V	I_VSB3V	Native	EN_USB	
GPIO12	5V	I_VSB3V	Native	DIS_TOUCH#	
GPIO13	5V	I_VSB3V	Native		-
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP	
GPIO15	5V	I_VSB3V	Native	WDT_RST#	
GPIO16	5V	I_VSB3V	Native		-
GPIO17	5V	I_VSB3V	Native	SIO_PECI	
GPIO20	5V	I_VSB3V	Native		-
GPIO21	5V	I_VSB3V	Native		
GPIO22	5V	I_VSB3V	Native	EXT_PWRBTN#	
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#	
GPIO24	5V	I_VSB3V	Native	PM_SLP_S3#	
GPIO25	5V	I_VSB3V	Native	PSON#	
GPIO26	5V	VBAT	Native	PWOK	
GPIO27	5V	VBAT	Native	SIO_RSMRST#	
GPIO30	5V	3VCC	Native	DCD3#	
GPIO31	5V	3VCC	Native	RI3#	
GPIO32	5V	3VCC	Native	CTS3#	
GPIO33	5V	3VCC	Native	DTR3#	
GPIO34	5V	3VCC	Native	RTS3#	
GPIO35	5V	3VCC	Native	DSR3#	
GPIO36	5V	3VCC	Native	TX3#	
GPIO37	5V	3VCC	Native	RX3#	
GPIO40	5V	3VCC	Native	DCD4#	
GPIO41	5V	3VCC	Native	RI4#	
GPIO42	5V	3VCC	Native	CTS4#	
GPIO43	5V	3VCC	Native	DTR4#	
GPIO44	5V	3VCC	Native	RTS4#	
GPIO45	5V	3VCC	Native	DSR4#	
GPIO46	5V	3VCC	Native	TX4#	
GPIO47	5V	3VCC	Native	RX4#	
GPIO50	5V	3VCC	Native	DIO_0	
GPIO51	5V	3VCC	Native	DIO_1	
GPIO52	5V	3VCC	Native	DIO_2	
GPIO53	5V	3VCC	Native	DIO_3	
GPIO54	5V	3VCC	Native	DIO_4	
GPIO55	5V	3VCC	Native	DIO_5	
GPIO56	5V	3VCC	Native	DIO_6	
GPIO57	5V	3VCC	Native	DIO_7	
GPIO60	5V	3VCC	Native		
GPIO61	5V	3VCC	Native		
GPIO62	5V	3VCC	Native		
GPIO63	5V	3VCC	Native		
GPIO64	5V	3VCC	Native		
GPIO65	5V	I_VSB3V	Native	LPC_PME#	
GPIO66	5V	VBAT	Native	DPWROK	
GPIO67	5V	I_VSB3V	Native	PM_SLP_S5#	
GPIO70	5V	3VCC	Native	PE	
GPIO71	5V	3VCC	Native	BUSY	
GPIO72	5V	3VCC	Native	ACK#	
GPIO73	5V	3VCC	Native	SLIN#	
GPIO74	5V	3VCC	Native	PINIT#	
GPIO75	5V	3VCC	Native	ERR#	
GPIO76	5V	3VCC	Native	AFD#	
GPIO77	5V	3VCC	Native	STB#	
GPIO80	5V	3VCC	Native	PD0	
GPIO81	5V	3VCC	Native	PD1	
GPIO82	5V	3VCC	Native	PD2	
GPIO83	5V	3VCC	Native	PD3	
GPIO84	5V	3VCC	Native	PD4	
GPIO85	5V	3VCC	Native	PD5	
GPIO86	5V	3VCC	Native	PD6	
GPIO87	5V	3VCC	Native	PD7	

F75111RG GPIO Pins :

Name	Tolerance	Power Well	Default	Function	
GPIO10	5V	VSB3V	Native	BOARDID_BIT0	
GPIO11	5V	VSB3V	Native	ADM213_EN	1
GPIO12	5V	VSB3V	Native	SEL_COM2_MD0	0
GPIO13	5V	VSB3V	Native		
GPIO14	5V	VSB3V	Native	BOARDID_BIT1	
GPIO15	5V	VSB3V	Native	BOARDID_BIT2	
GPIO16	5V	VSB3V	Native	BOARDID_BIT3	
GPIO17	5V	VSB3V	Native	BOARDID_BIT4	
GPIO20	5V	VSB3V	Native	SEL_COM2_MD1	
GPIO21	5V	VSB3V	Native	SEL_COM2_MD2	
GPIO22	5V	VSB3V	Native	COM2_SLEW	
GPIO23	5V	VSB3V	Native	SEL_COM3_MD1	
GPIO24	5V	VSB3V	Native	SEL_COM3_MD2	
GPIO25	5V	VSB3V	Native	COM3_SLEW	
GPIO26	5V	VSB3V	Native	SEL_COM3_MD0	
GPIO27	5V	VSB3V	Native		
GPIO30	5V	VSB3V	GPIO	LVDS_EN	
GPIO31	5V	VSB3V	GPIO	LVDS_CFG1	1
GPIO32	5V	VSB3V	GPIO	LVDS_CFG2	0
GPIO33	5V	VSB3V	GPIO	LVDS_PD#	

AAEON an ASUS assoc. co.

Title: **System Settings**

Size	Document Number	Rev:
Custom	GENE-BT05	A1.2_0_0

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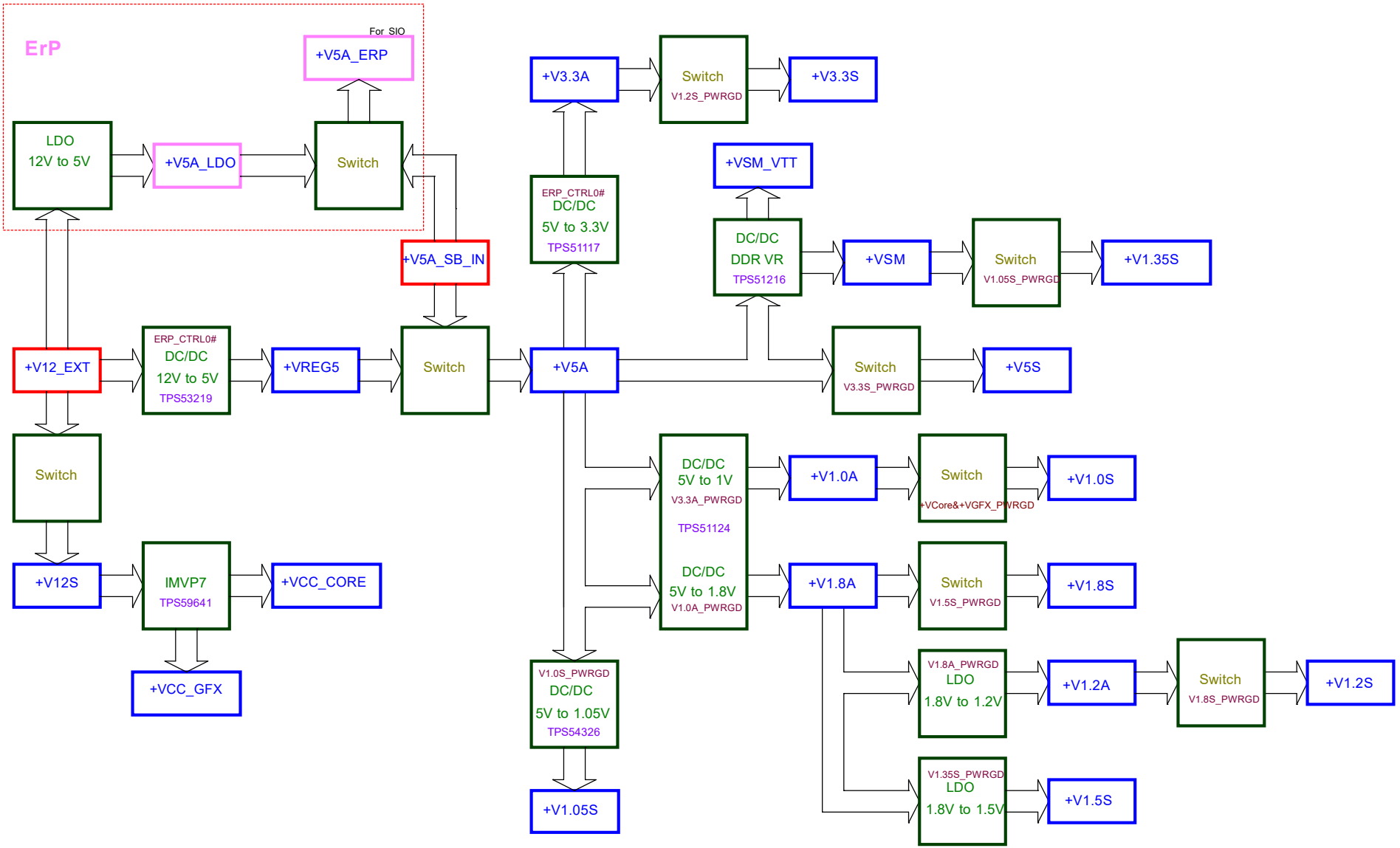

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Size: Custom	Document Number: **GENE-BT05**	Rev: **A1.2_0_0**
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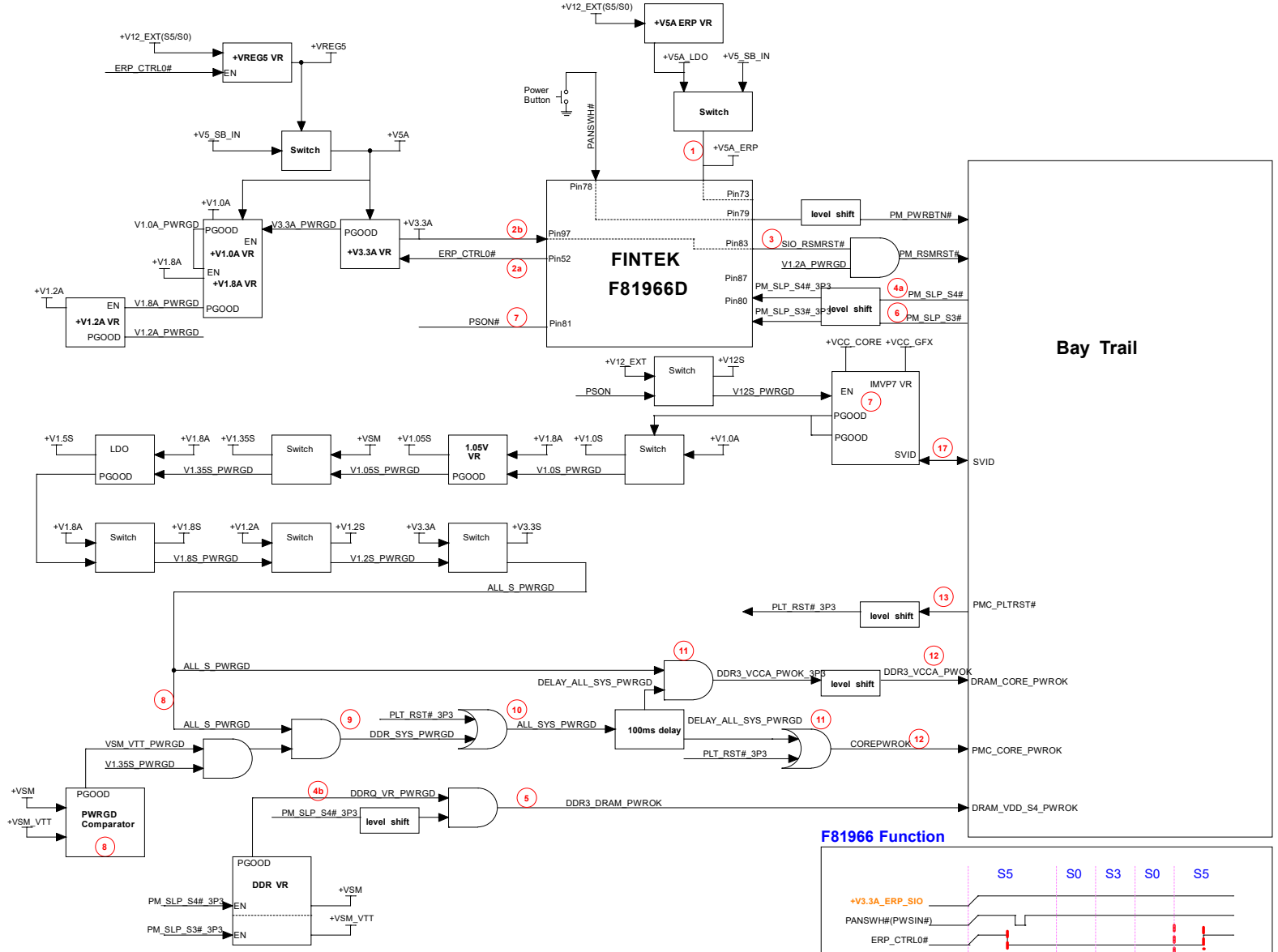
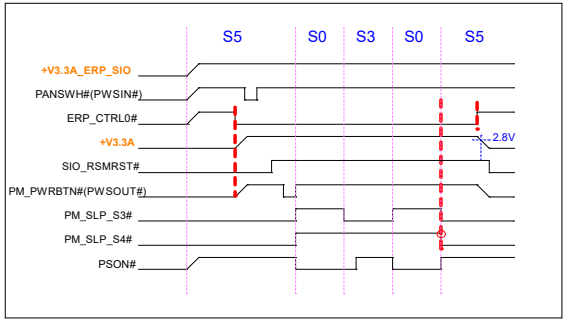
ERP Mode



F81966 Function



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Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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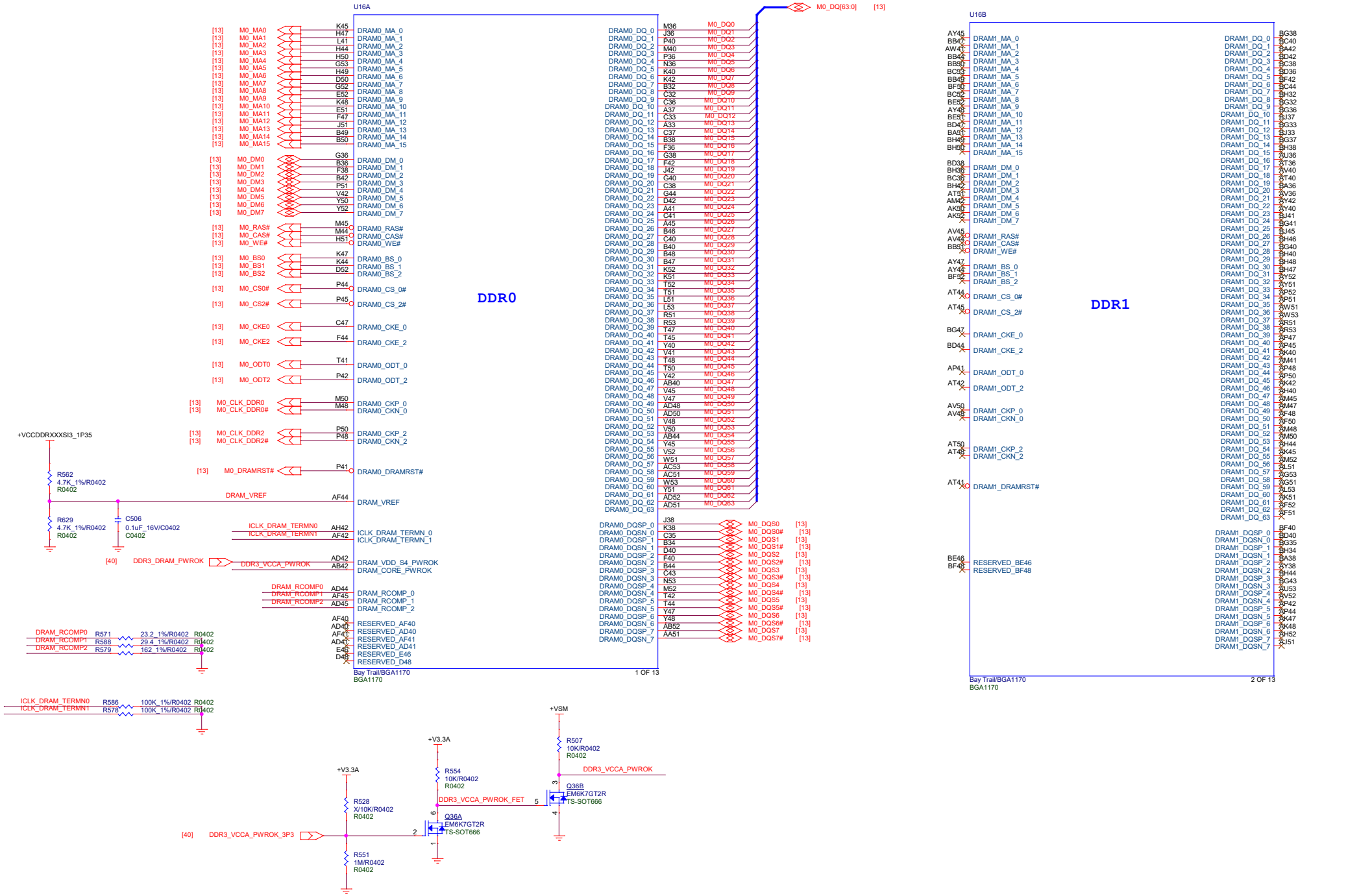

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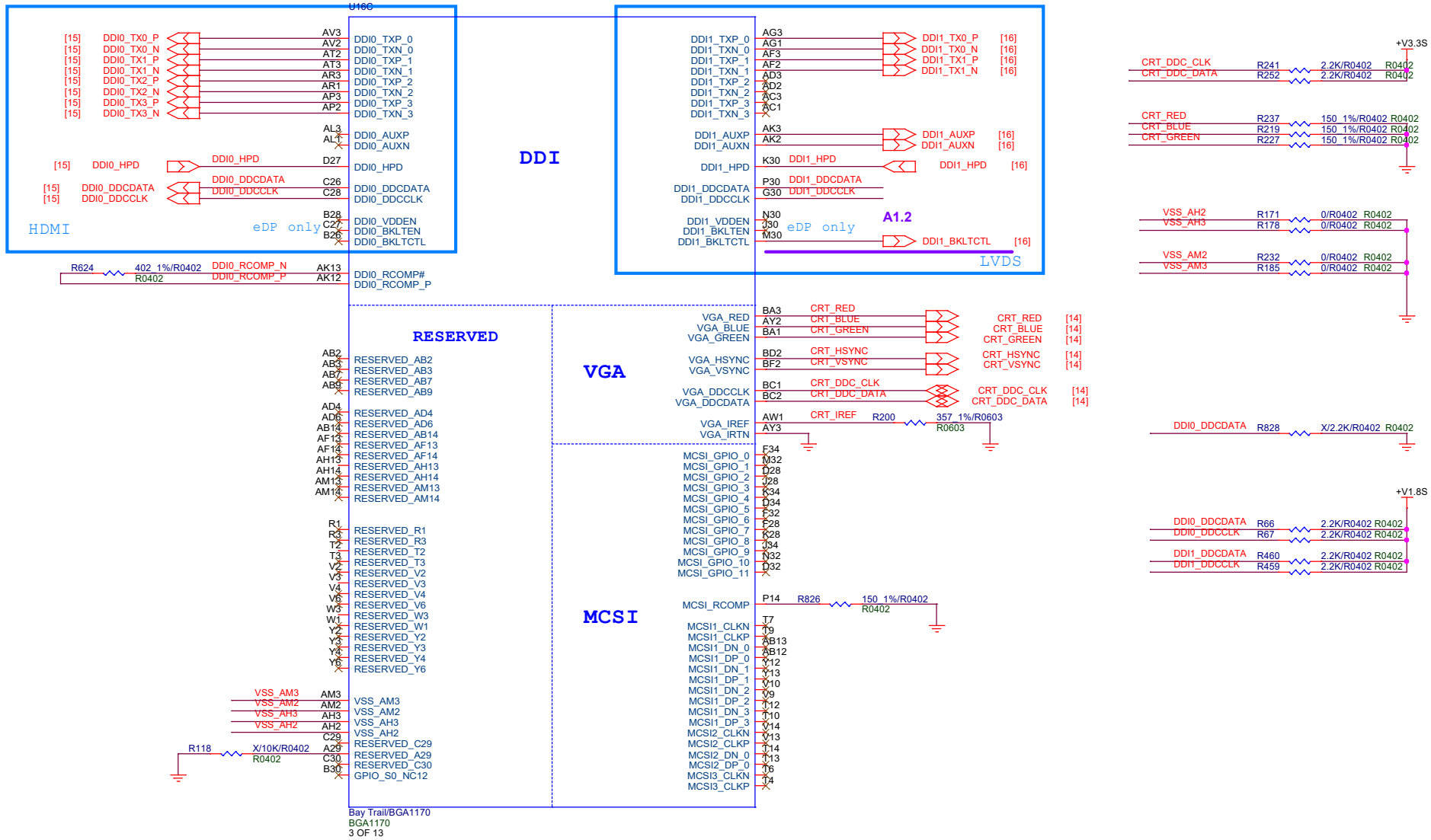

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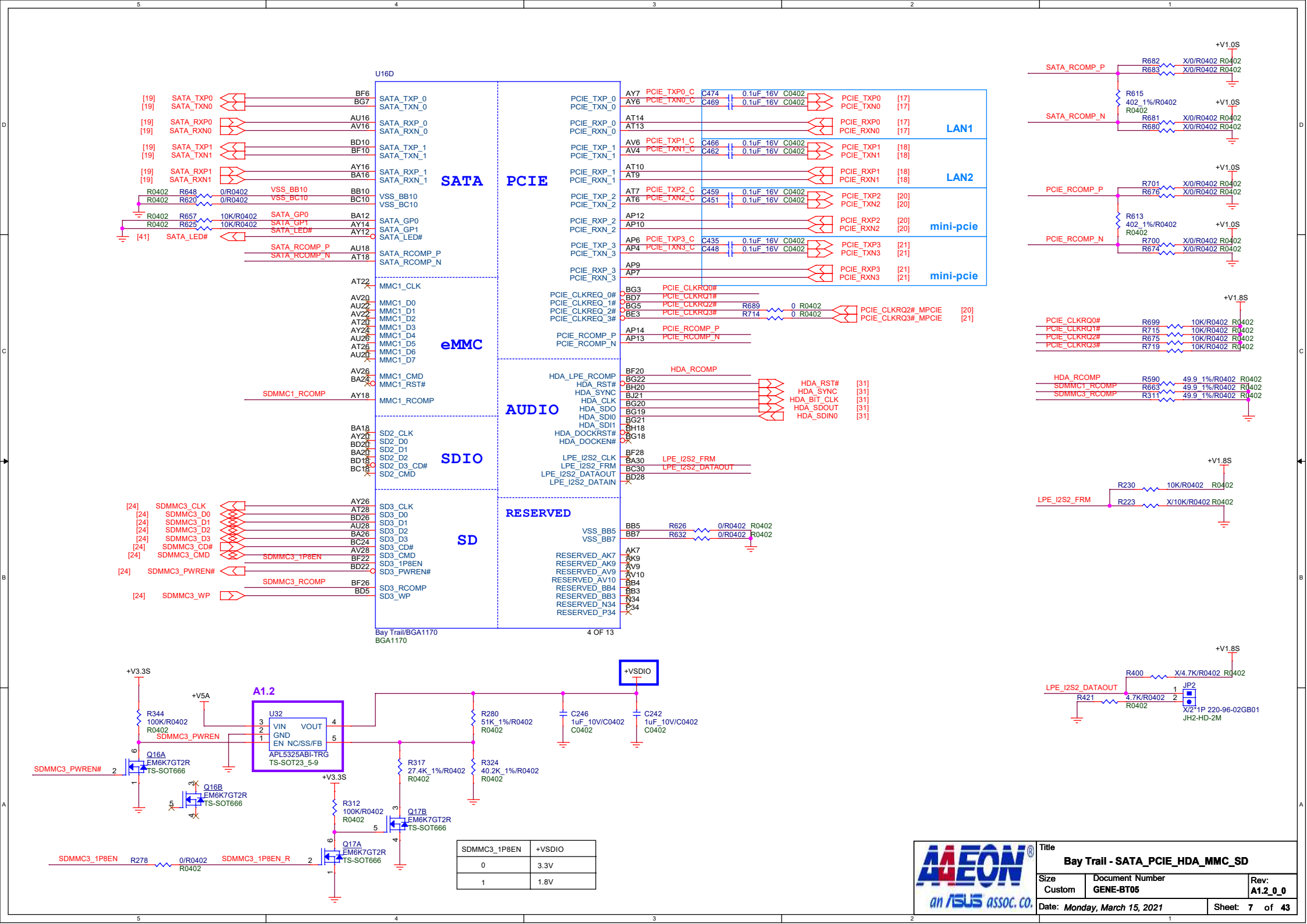

SDMMC3_1P8EN	+VSDIO
0	3.3V
1	1.8V

Title	Bay Trail - SATA_PCIE_HDA_MMC_SD		
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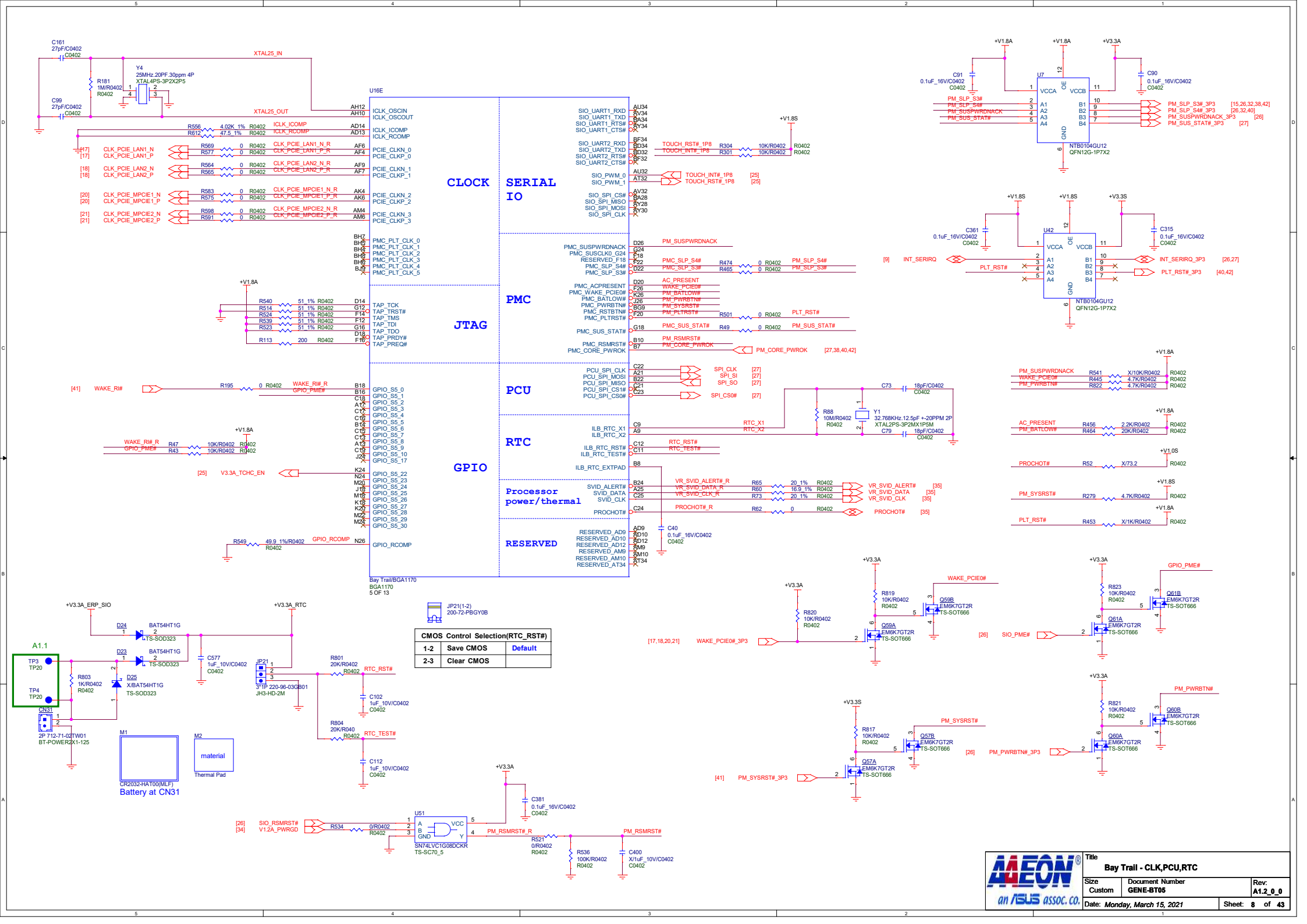
U16E
CLOCK
SERIAL IO
PMC
JTAG
PCU
RTC
GPIO
Processor power/thermal
RESERVED
Bay Trail/BGA1170
BGA1170
5 OF 13
XTAL25_IN
XTAL25_OUT
Y4
25MHz,20PF,30ppm 4P
XTAL4PS-3P2X2P5
C161
27pF/C0402
C99
27pF/C0402
R181
1M/R0402
ICLK_ICOMP
ICLK_RCOMP
CLK_PCIE_LAN1_N_R
CLK_PCIE_LAN1_P_R
CLK_PCIE_LAN2_N_R
CLK_PCIE_LAN2_P_R
CLK_PCIE_MPCIE1_N_R
CLK_PCIE_MPCIE1_P_R
CLK_PCIE_MPCIE2_N_R
CLK_PCIE_MPCIE2_P_R
PMC_PLT_CLK_0
PMC_PLT_CLK_1
PMC_PLT_CLK_2
PMC_PLT_CLK_3
PMC_PLT_CLK_4
PMC_PLT_CLK_5
TAP_TCK
TAP_TRST#
TAP_TMS
TAP_TDI
TAP_TDO
TAP_PRDY#
TAP_PREQ#
WAKE_RI#_R
GPIO_PME#
GPIO_RCOMP
SIO_UART1_RXD
SIO_UART1_TXD
SIO_UART1_RTS#
SIO_UART1_CTS#
SIO_UART2_RXD
SIO_UART2_TXD
SIO_UART2_RTS#
SIO_UART2_CTS#
SIO_PWM_0
SIO_PWM_1
SIO_SPI_CS#
SIO_SPI_MISO
SIO_SPI_MOSI
SIO_SPI_CLK
TOUCH_RST#_1P8
TOUCH_INT#_1P8
PMC_SUSPWRDNACK
PMC_SUSCLK0_G24
PMC_SLP_S4#
PMC_SLP_S3#
PMC_ACPRESENT
PMC_WAKE_PCIE0#
PMC_BATLOW#
PMC_PWRBTN#
PMC_RSTBTN#
PMC_PLTRST#
PMC_SUS_STAT#
PMC_RSMRST#
PMC_CORE_PWROK
PCU_SPI_CLK
PCU_SPI_MOSI
PCU_SPI_MISO
PCU_SPI_CS1#
PCU_SPI_CS0#
ILB_RTC_X1
ILB_RTC_X2
ILB_RTC_RST#
ILB_RTC_TEST#
ILB_RTC_EXTPAD
SVID_ALERT#
SVID_DATA
SVID_CLK
PROCHOT#
RESERVED_AD9
RESERVED_AD10
RESERVED_AD12
RESERVED_AM9
RESERVED_AM10
RESERVED_AT34
JP21(1-2)
200-72-PBGY0B
CMOS Control Selection(RTC_RST#)
1-2 Save CMOS Default
2-3 Clear CMOS
A1.1
CN31
2P 712-71-02TW01
BT-POWER2X1-125
M1
CR2032-HAT00(MLF)
Battery at CN31
M2
material
Thermal Pad
U51
SN74LVC1G08DCKR
TS-SC70_5
U7
NTB0104GU12
QFN12G-1P7X2
U42
NTB0104GU12
QFN12G-1P7X2
Y1
32.768KHz,12.5pF +-20PPM 2P
XTAL2PS-3P2MX1P5M
Q59A EM6K7GT2R TS-SOT666
Q59B EM6K7GT2R TS-SOT666
Q61A EM6K7GT2R TS-SOT666
Q61B EM6K7GT2R TS-SOT666
Q57A EM6K7GT2R TS-SOT666
Q57B EM6K7GT2R TS-SOT666
Q60A EM6K7GT2R TS-SOT666
Q60B EM6K7GT2R TS-SOT666
Title
Bay Trail - CLK,PCU,RTC
Size Custom
Document Number GENE-BT05
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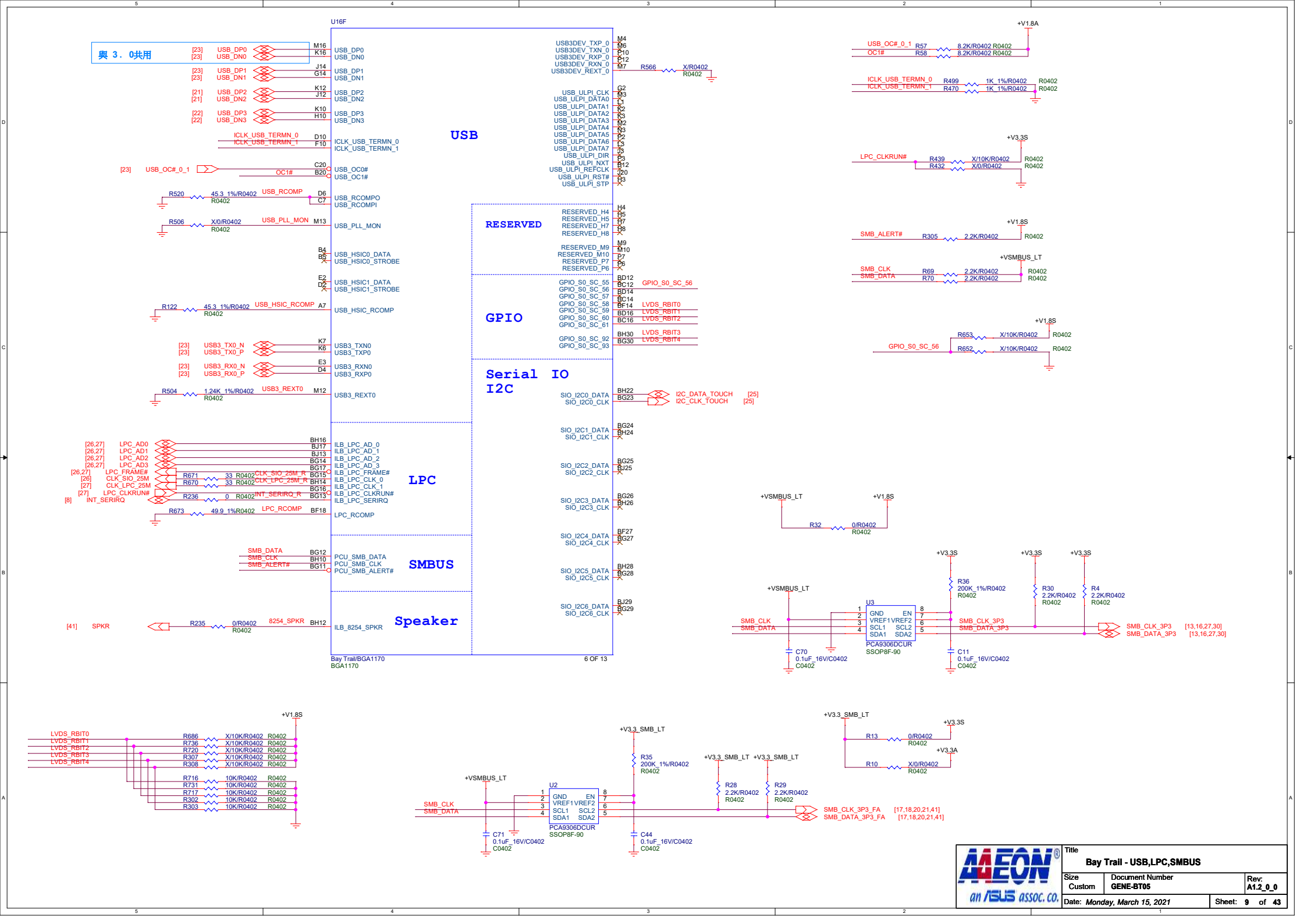
奥 3．0共用
U16F
USB
RESERVED
GPIO
Serial IO
I2C
LPC
SMBUS
Speaker
Bay Trail/BGA1170
BGA1170
6 OF 13
PCA9306DCUR
SSOP8F-90
Bay Trail - USB,LPC,SMBUS
AAEON
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Size
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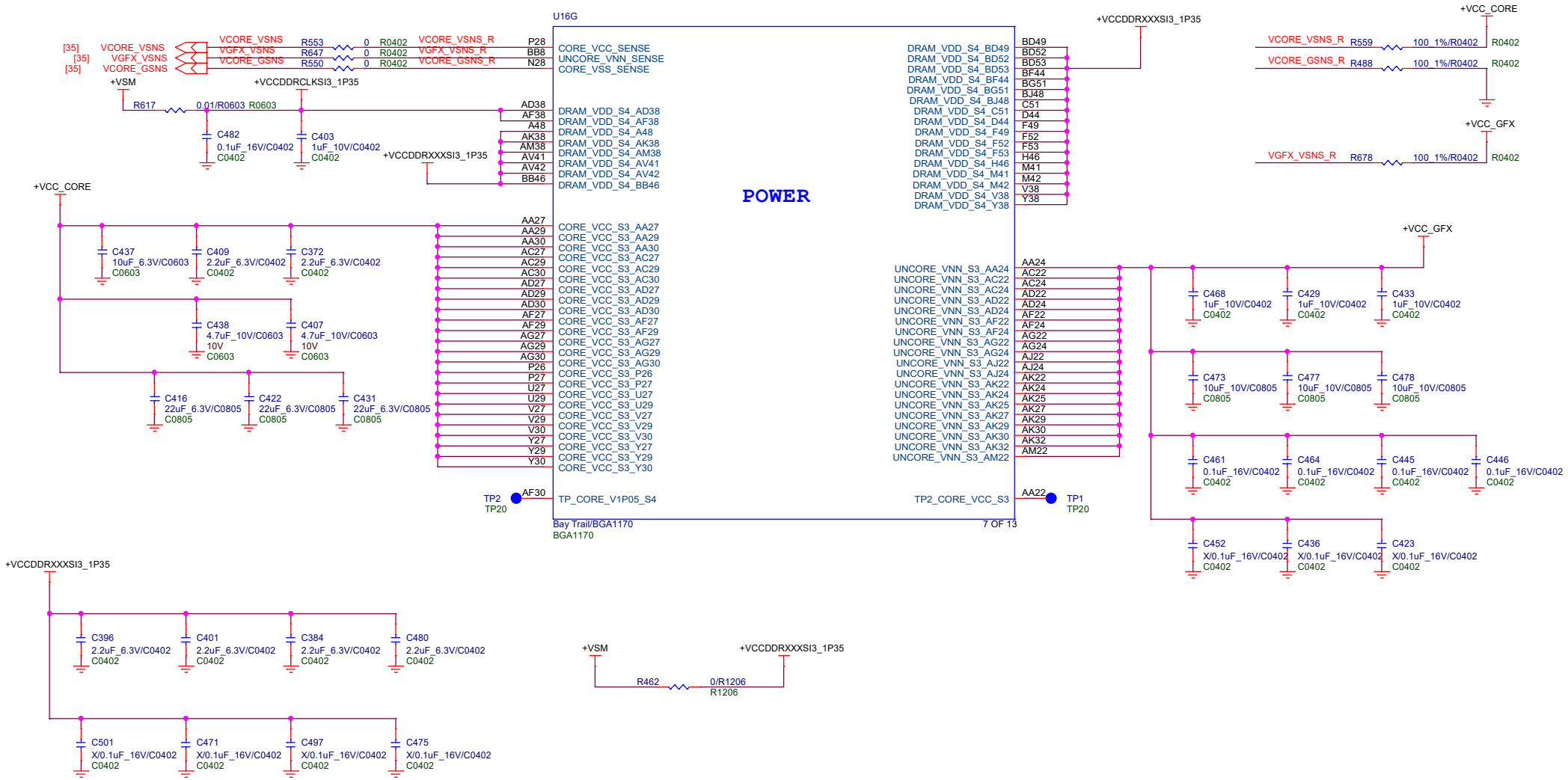

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Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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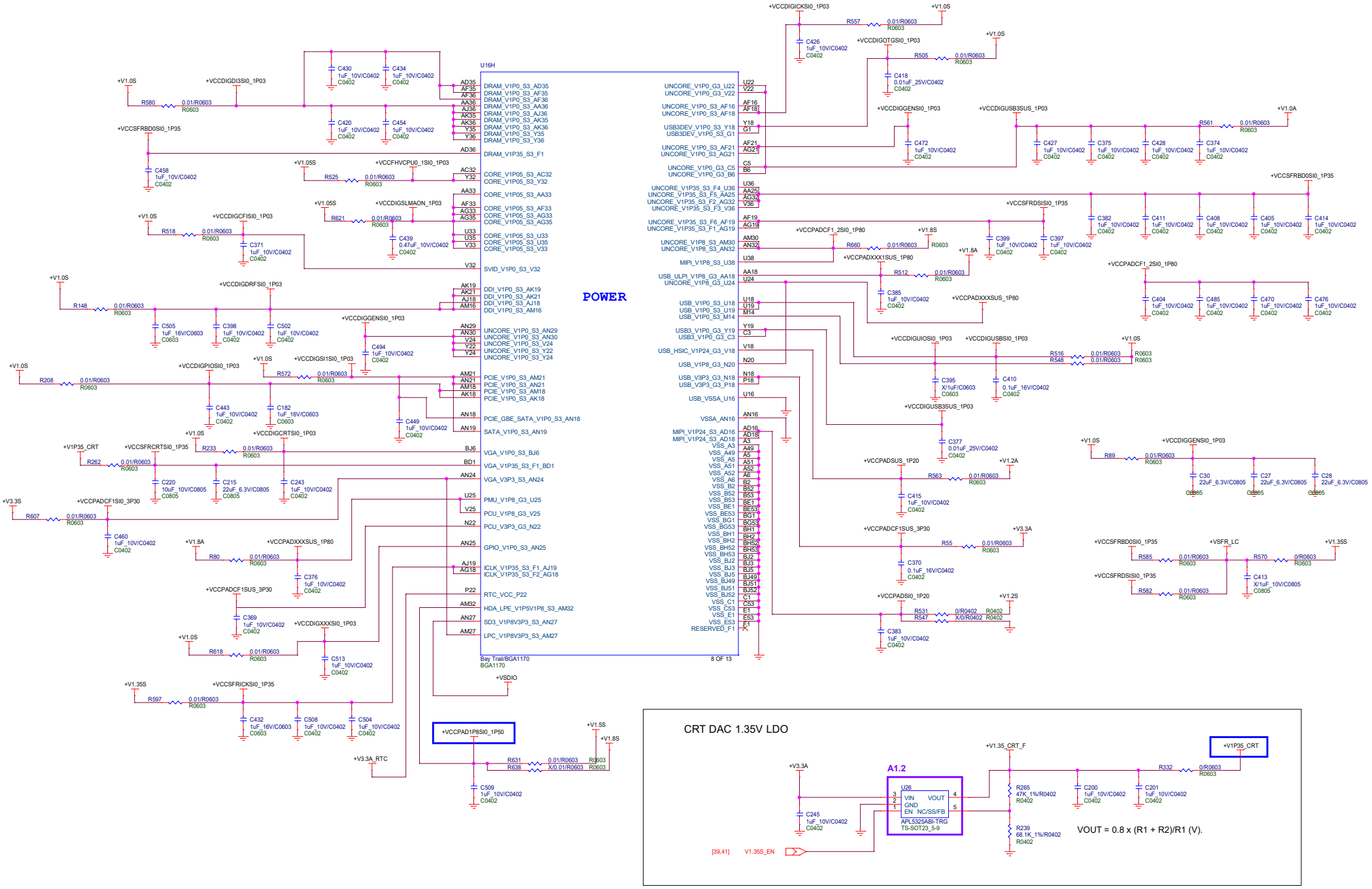

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Size: Custom	Document Number: GENE-BT05		Rev: A1.2_0_0
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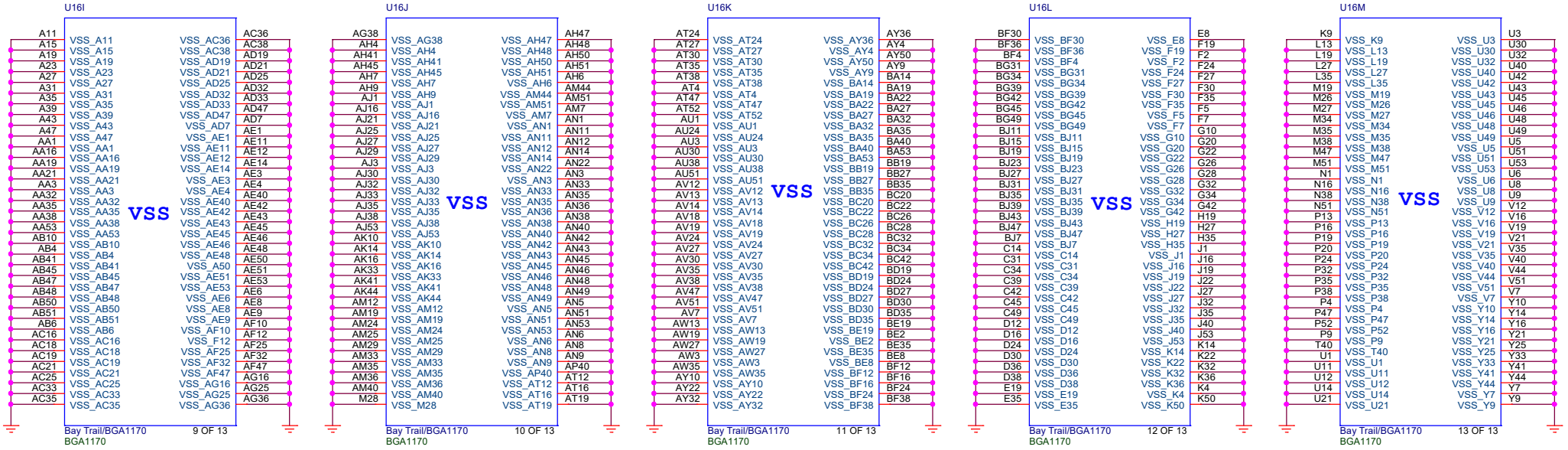

Title	Bay Trail - GND
Size	Custom
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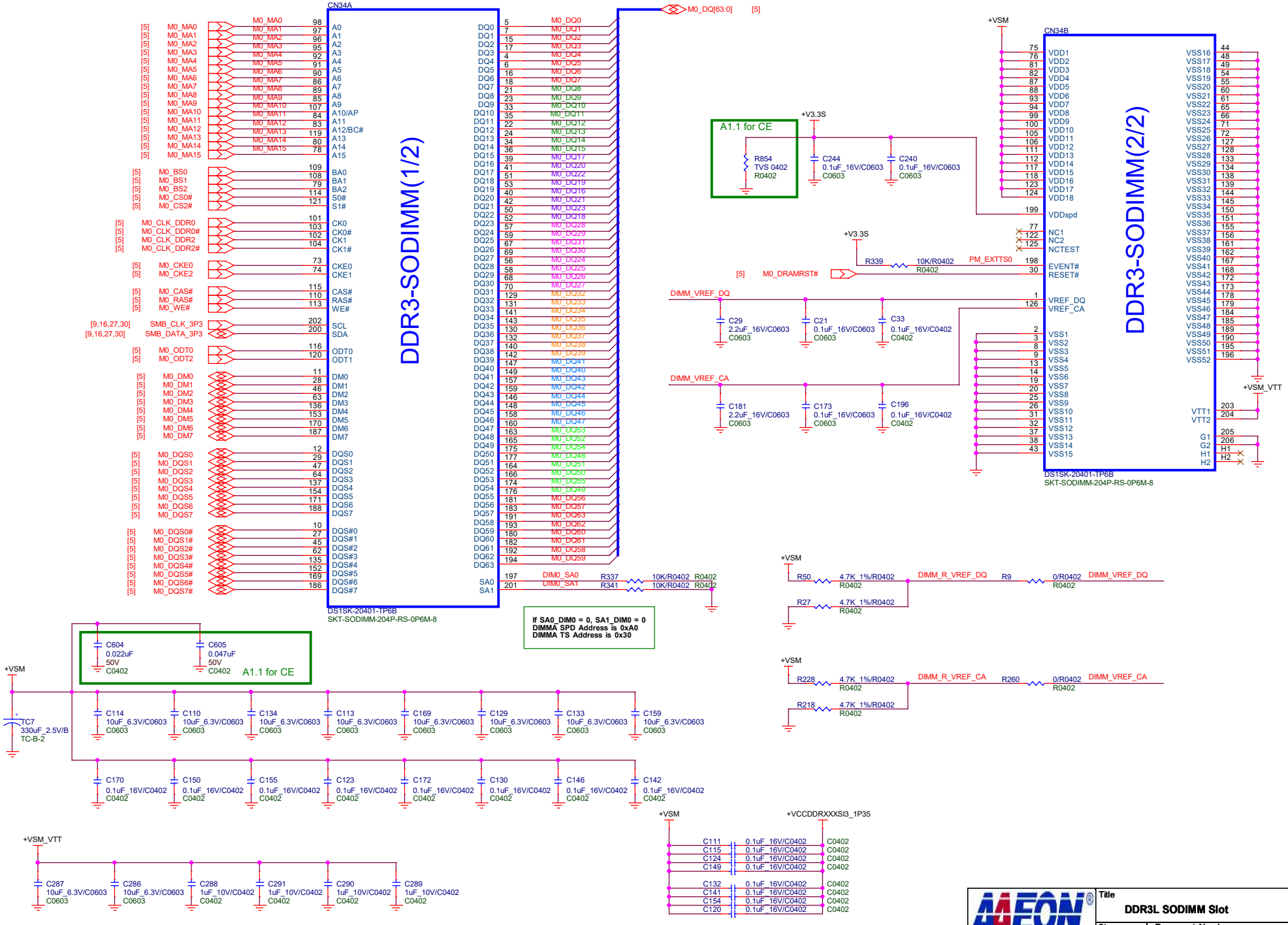
SODIMM#0



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Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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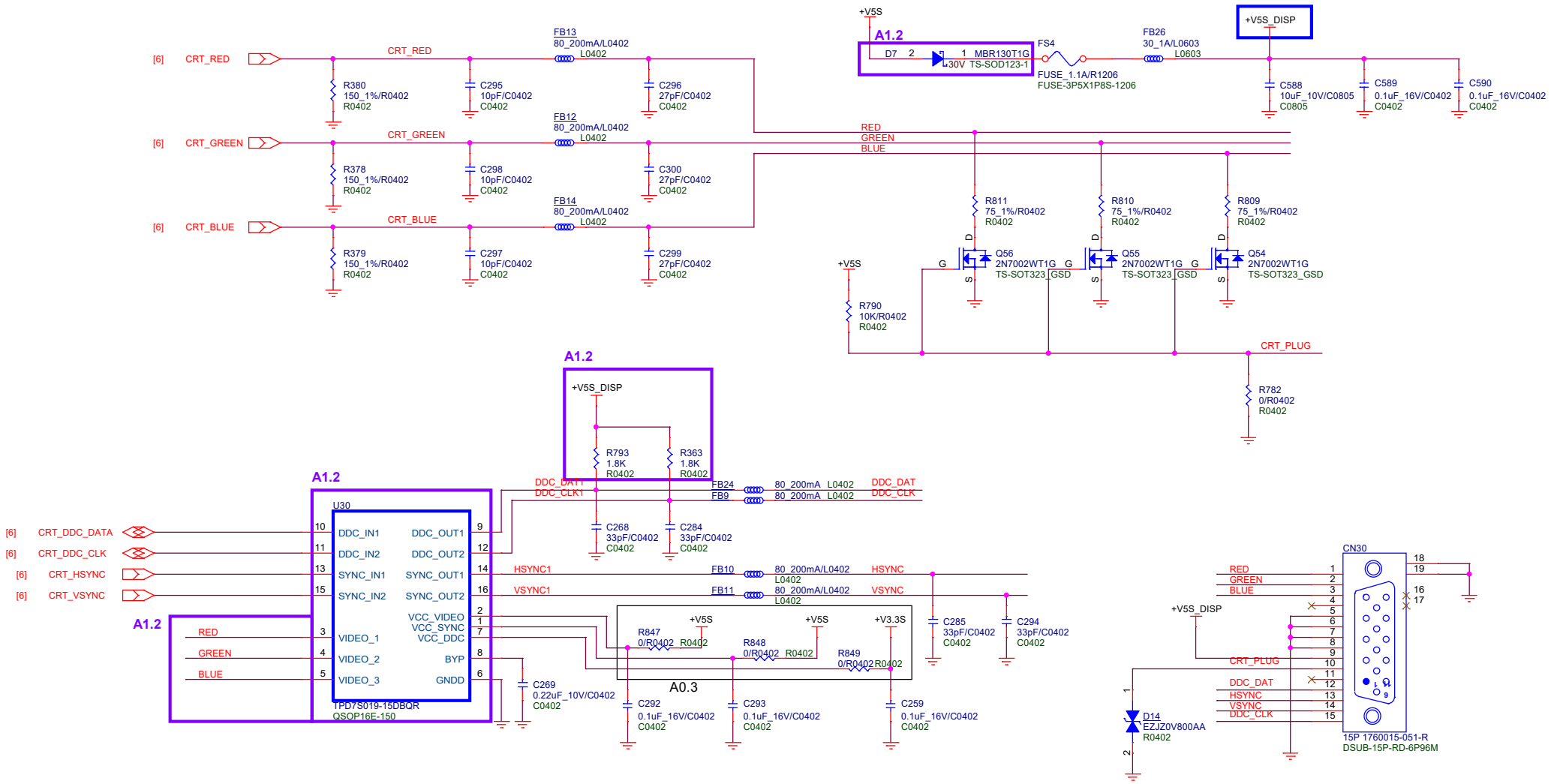
CRT



AAEON an ASUS assoc. co.	Title: CRT	
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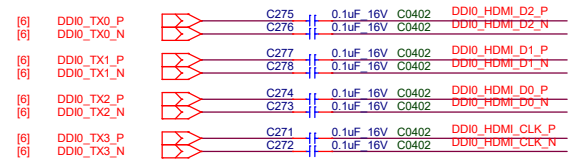
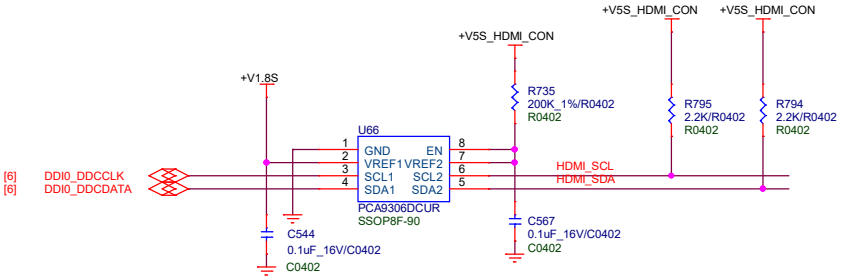
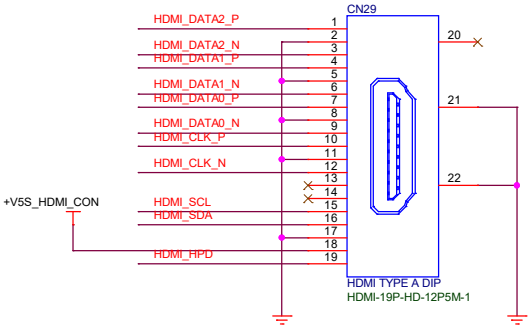
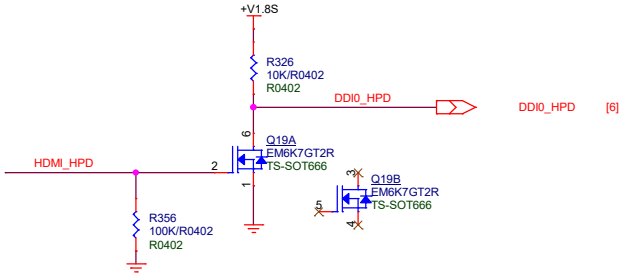
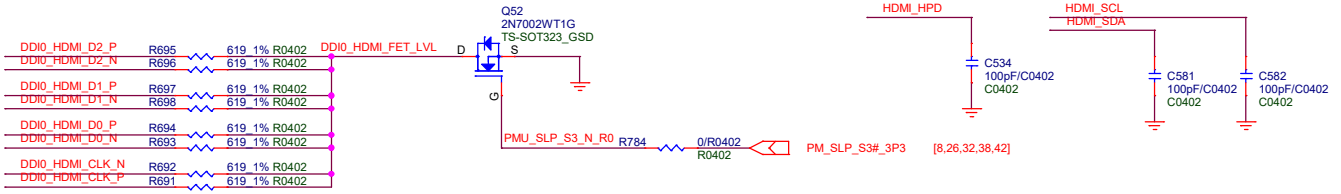
HDMI

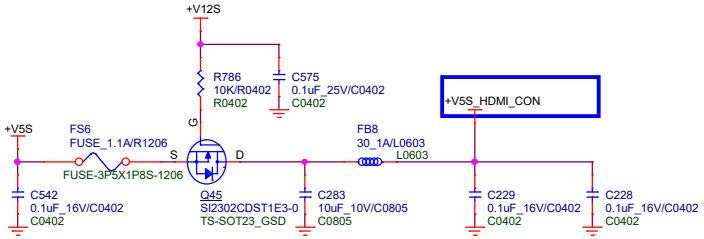


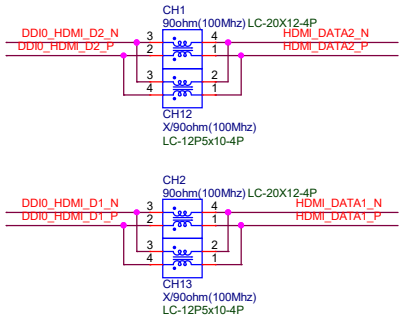


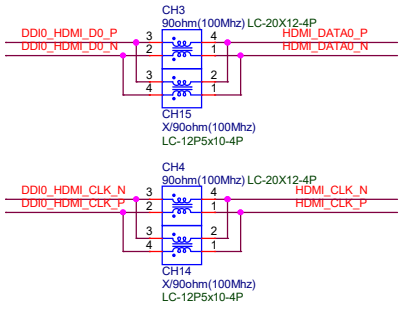


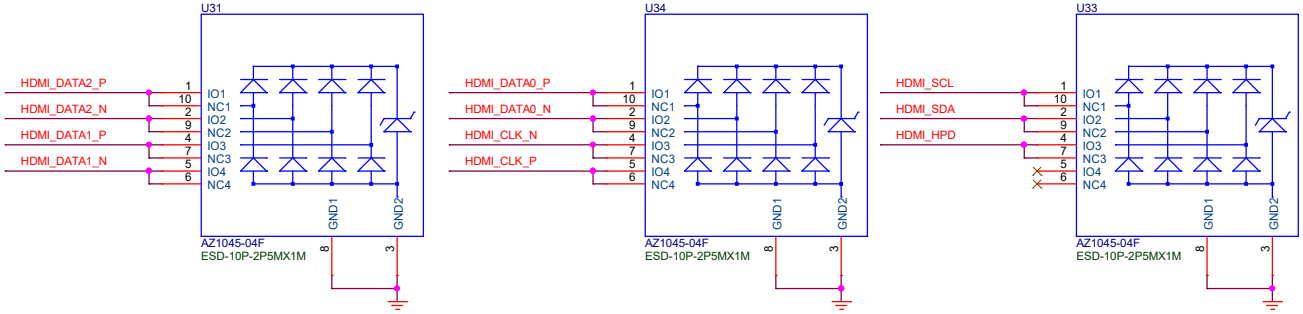






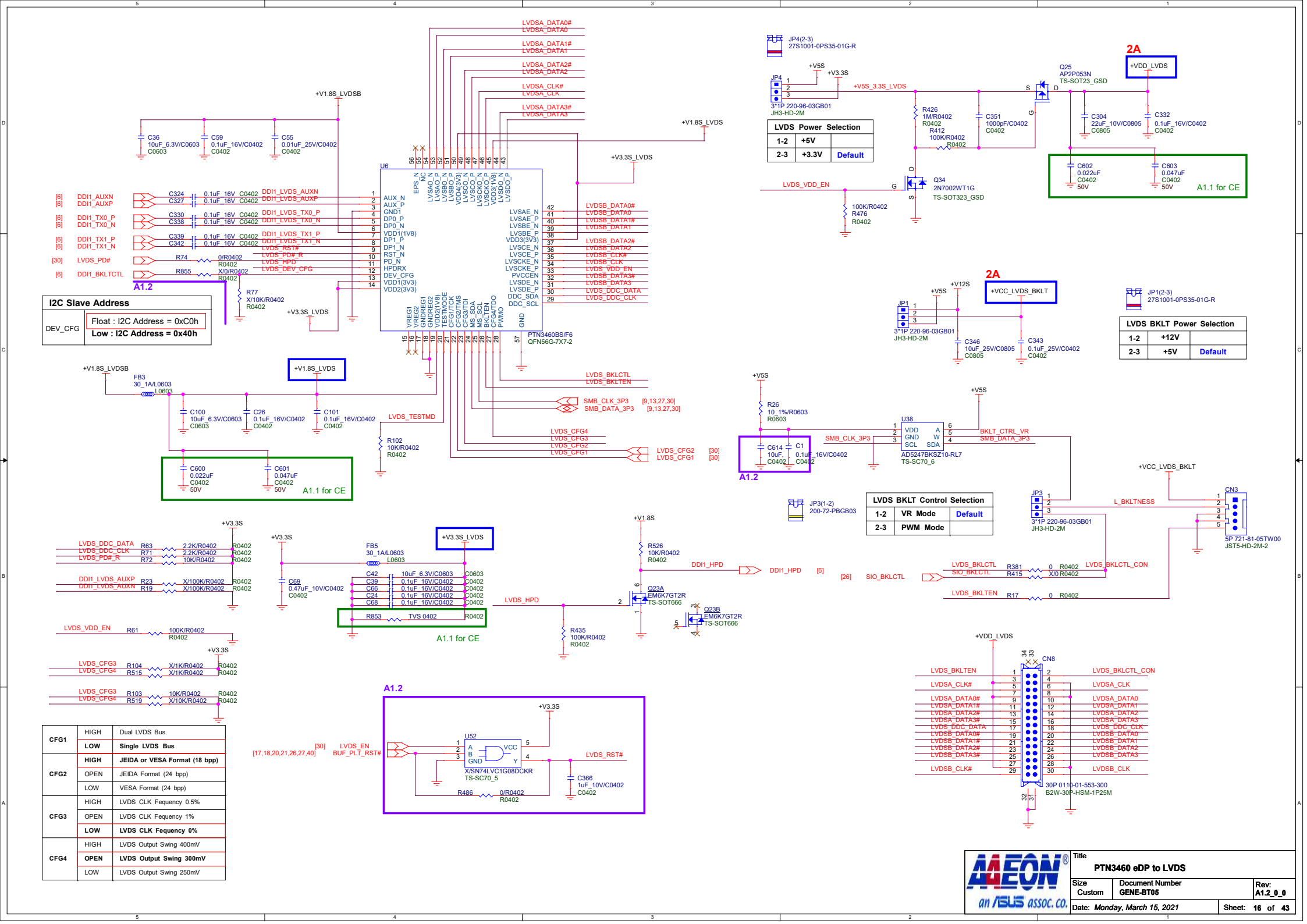






AAEON an ASUS assoc. co.

Title: HDMI		
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021		Sheet: 15 of 43


U6
PTN3460BS/F6
QFN56G-7X7-2
+V1.8S_LVDSB
+V1.8S_LVDS
+V3.3S_LVDS
LVDSA_DATA0#
LVDSA_DATA0
LVDSA_DATA1#
LVDSA_DATA1
LVDSA_DATA2#
LVDSA_DATA2
LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA3#
LVDSA_DATA3
LVDSB_DATA0#
LVDSB_DATA0
LVDSB_DATA1#
LVDSB_DATA1
LVDSB_DATA2#
LVDSB_DATA2
LVDSB_CLK#
LVDSB_CLK
LVDSB_DATA3#
LVDSB_DATA3
LVDS_DDC_DATA
LVDS_DDC_CLK
LVDS_VDD_EN
LVDS_BKLCTL
LVDS_BKLTEN
LVDS_TESTMD
LVDS_CFG4
LVDS_CFG3
LVDS_CFG2
LVDS_CFG1
LVDS_HPD
LVDS_RST#
LVDS_EN
DDI1_AUXN
DDI1_AUXP
DDI1_TX0_P
DDI1_TX0_N
DDI1_TX1_P
DDI1_TX1_N
DDI1_BKLTCTL
LVDS_PD#
DDI1_HPD
SIO_BKLCTL
SMB_CLK_3P3
SMB_DATA_3P3
I2C Slave Address
DEV_CFG
Float : I2C Address = 0xC0h
Low : I2C Address = 0x40h
A1.2
A1.1 for CE
2A
+VDD_LVDS
+VCC_LVDS_BKLT
LVDS Power Selection
1-2 +5V
2-3 +3.3V Default
LVDS BKLT Power Selection
1-2 +12V
2-3 +5V Default
LVDS BKLT Control Selection
1-2 VR Mode Default
2-3 PWM Mode
CFG1 HIGH Dual LVDS Bus
LOW Single LVDS Bus
CFG2 HIGH JEIDA or VESA Format (18 bpp)
OPEN JEIDA Format (24 bpp)
LOW VESA Format (24 bpp)
CFG3 HIGH LVDS CLK Fequency 0.5%
OPEN LVDS CLK Fequency 1%
LOW LVDS CLK Fequency 0%
CFG4 HIGH LVDS Output Swing 400mV
OPEN LVDS Output Swing 300mV
LOW LVDS Output Swing 250mV
Title
PTN3460 eDP to LVDS
Size Custom
Document Number GENE-BT05
Rev: A1.2_0_0
Date: Monday, March 15, 2021
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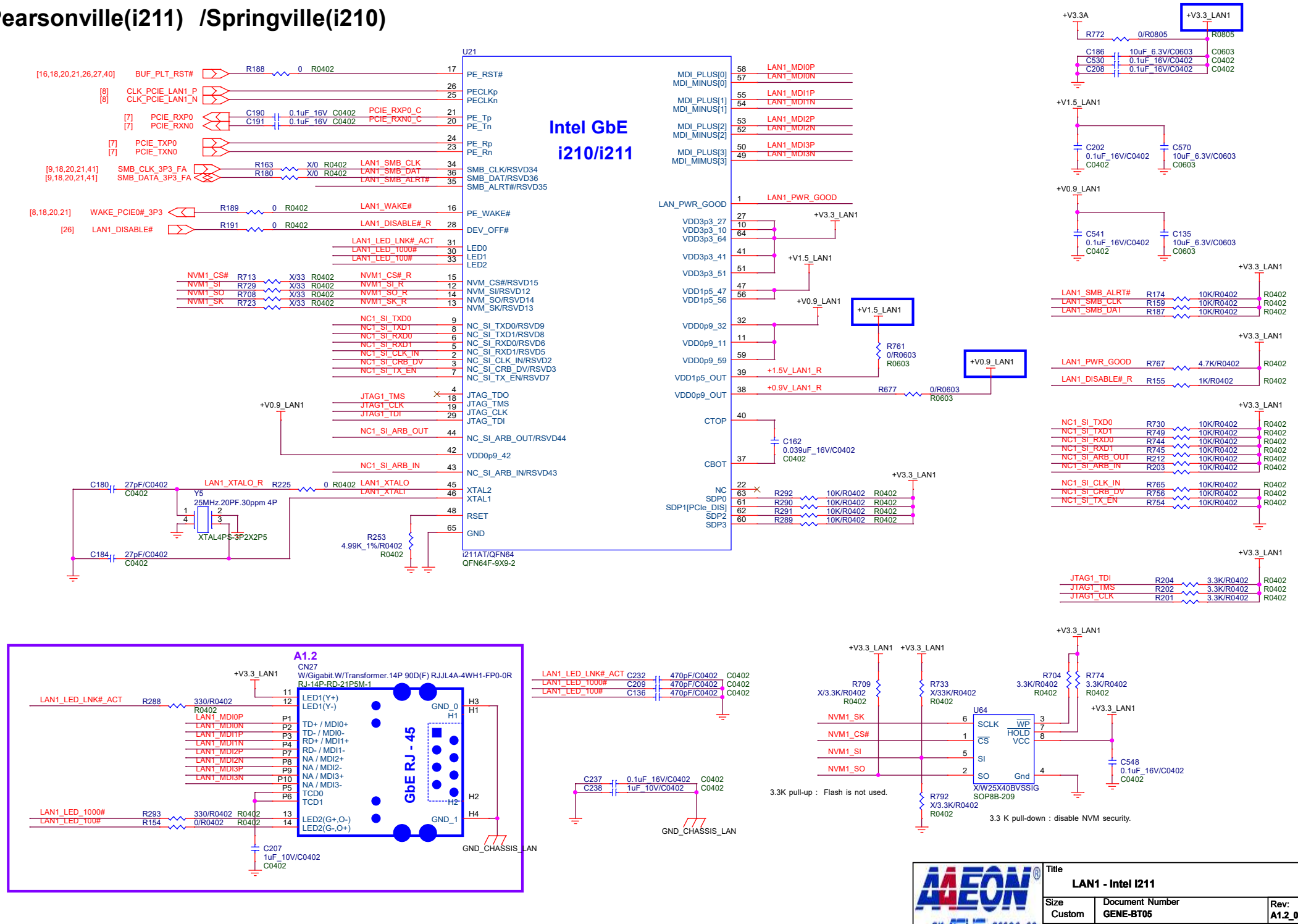
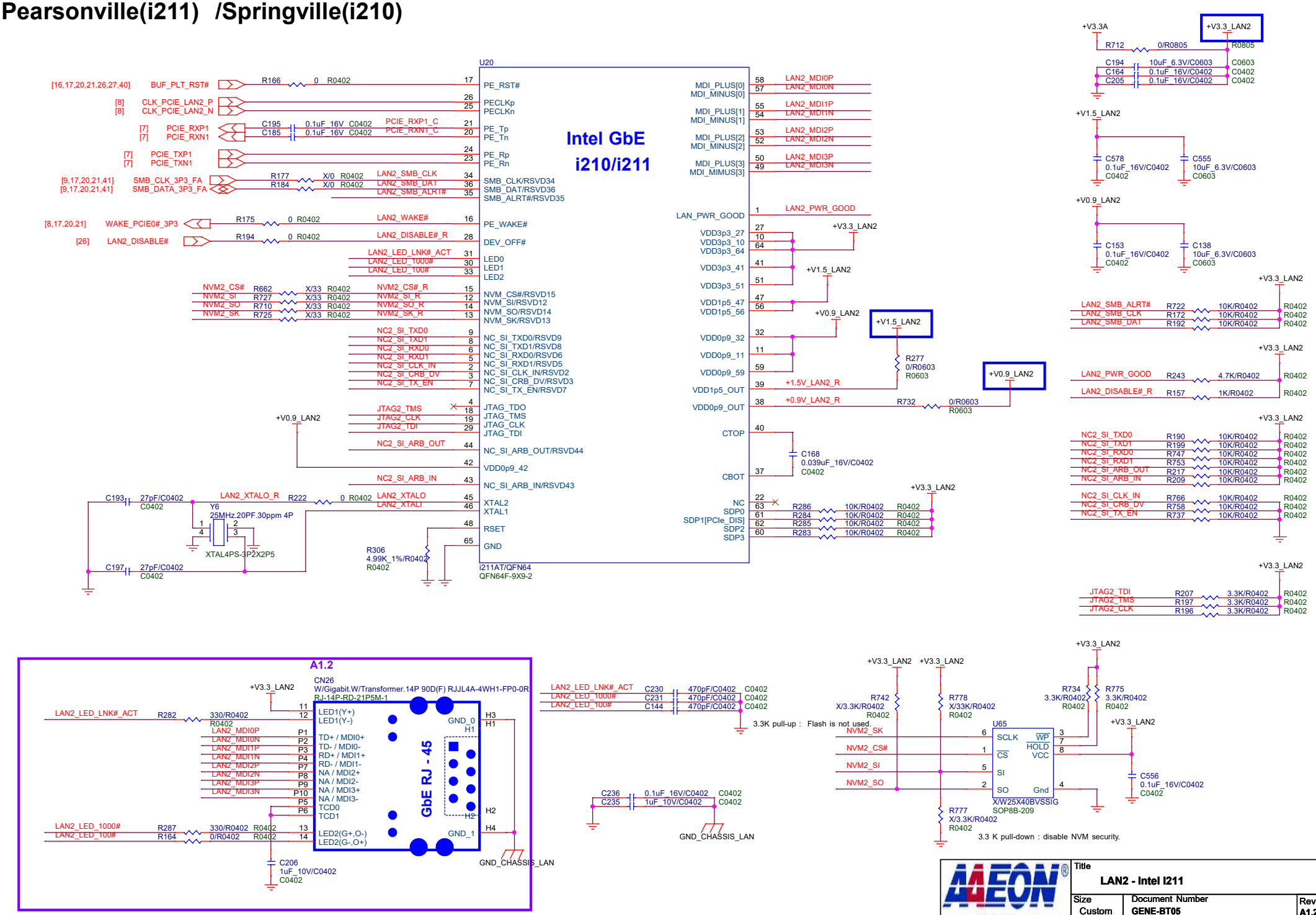
Pearsonville(i211) /Springville(i210)



AAEON an ASUS assoc. co.	Title: LAN1 - Intel I211	
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021	Sheet: 17 of 43	

Pearsonville(i211) /Springville(i210)



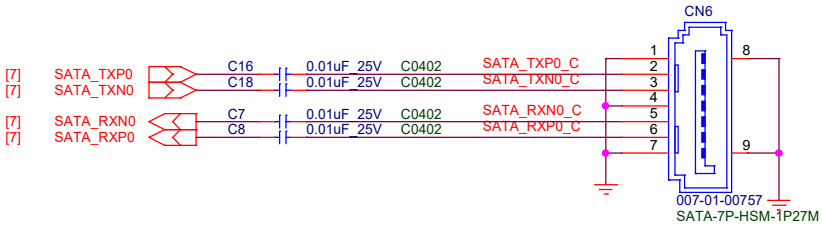
AAEON an ASUS assoc. co.

Title: LAN2 - Intel I211

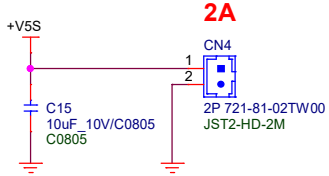
Size	Document Number	Rev:
Custom	GENE-BT05	A1.2_0_0

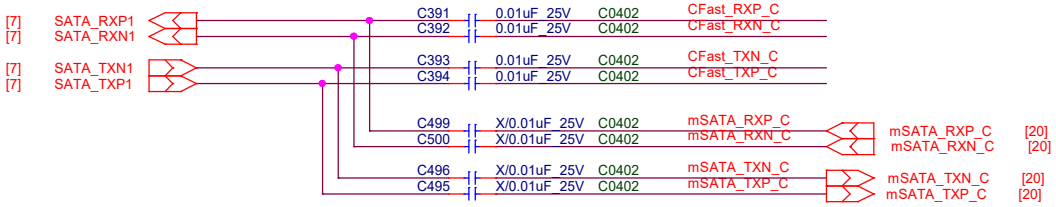
Date: Monday, March 15, 2021 Sheet: 18 of 43

SATA 2.0

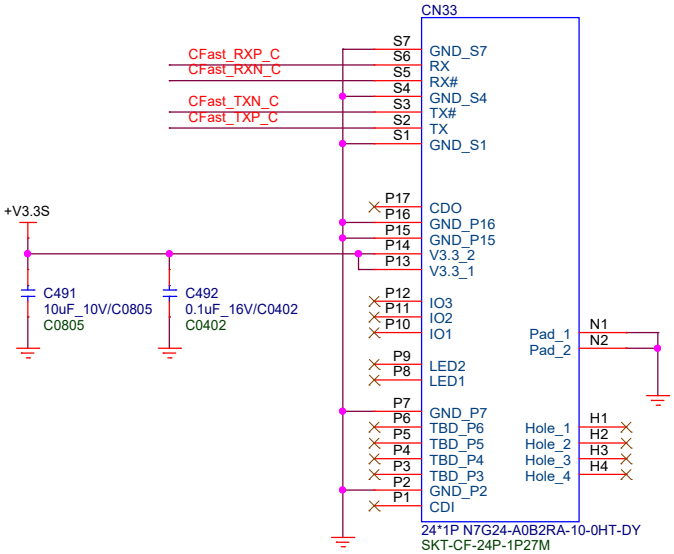


2A

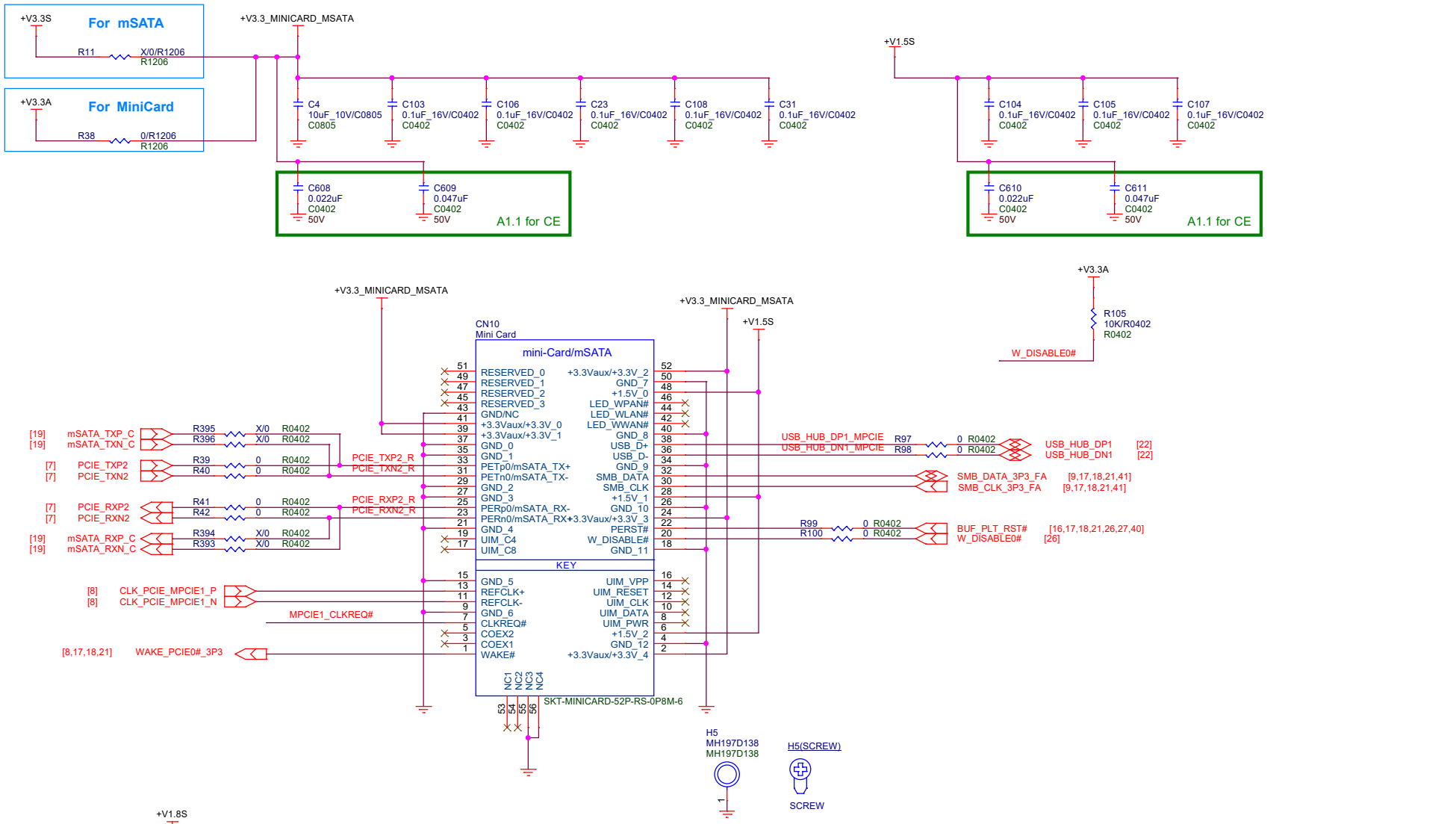




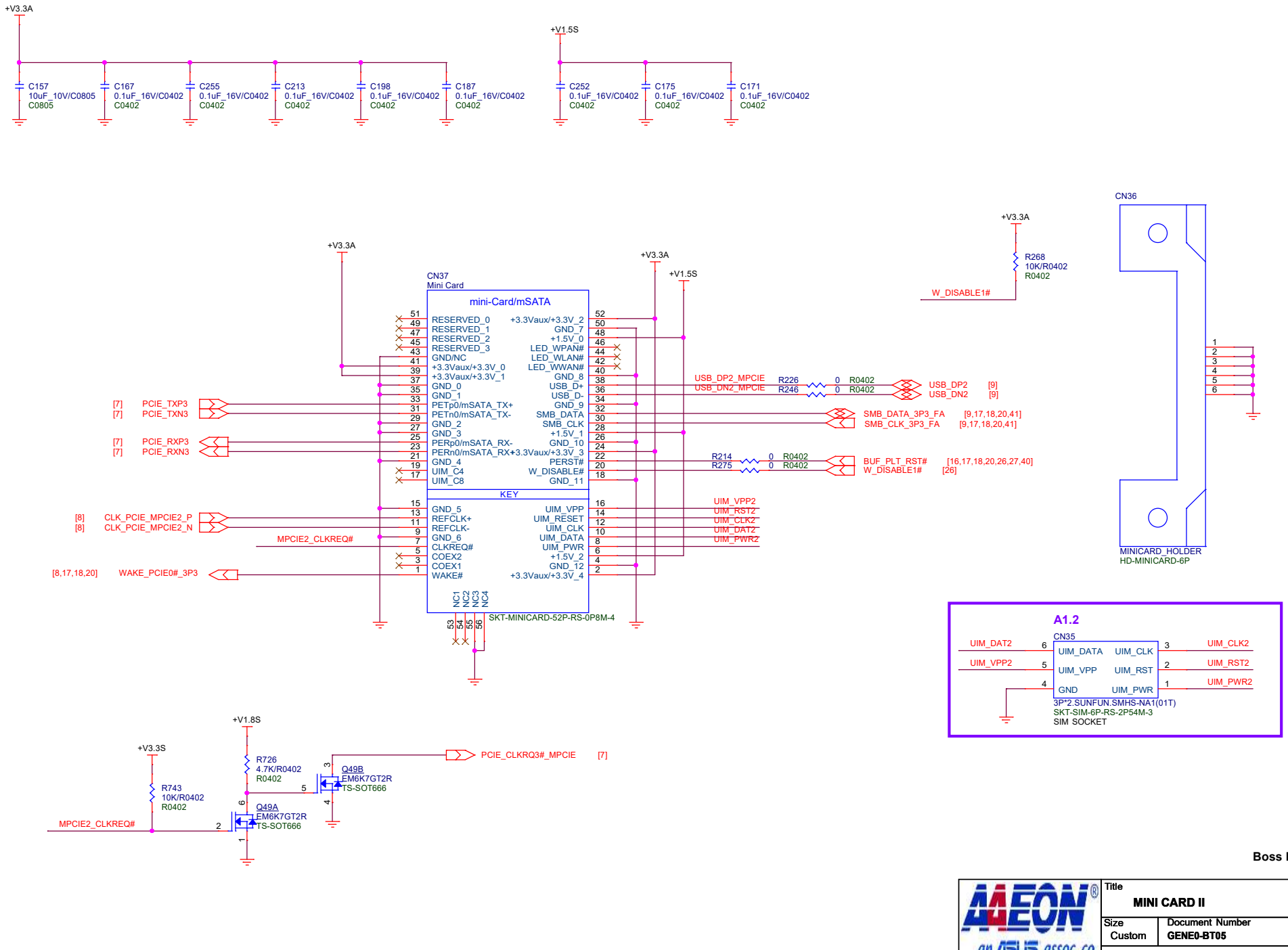
CFast



AAEON an ASUS assoc. co.	Title: SATA,CFAST	
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: *Monday, March 15, 2021*	Sheet: 19 of 43	



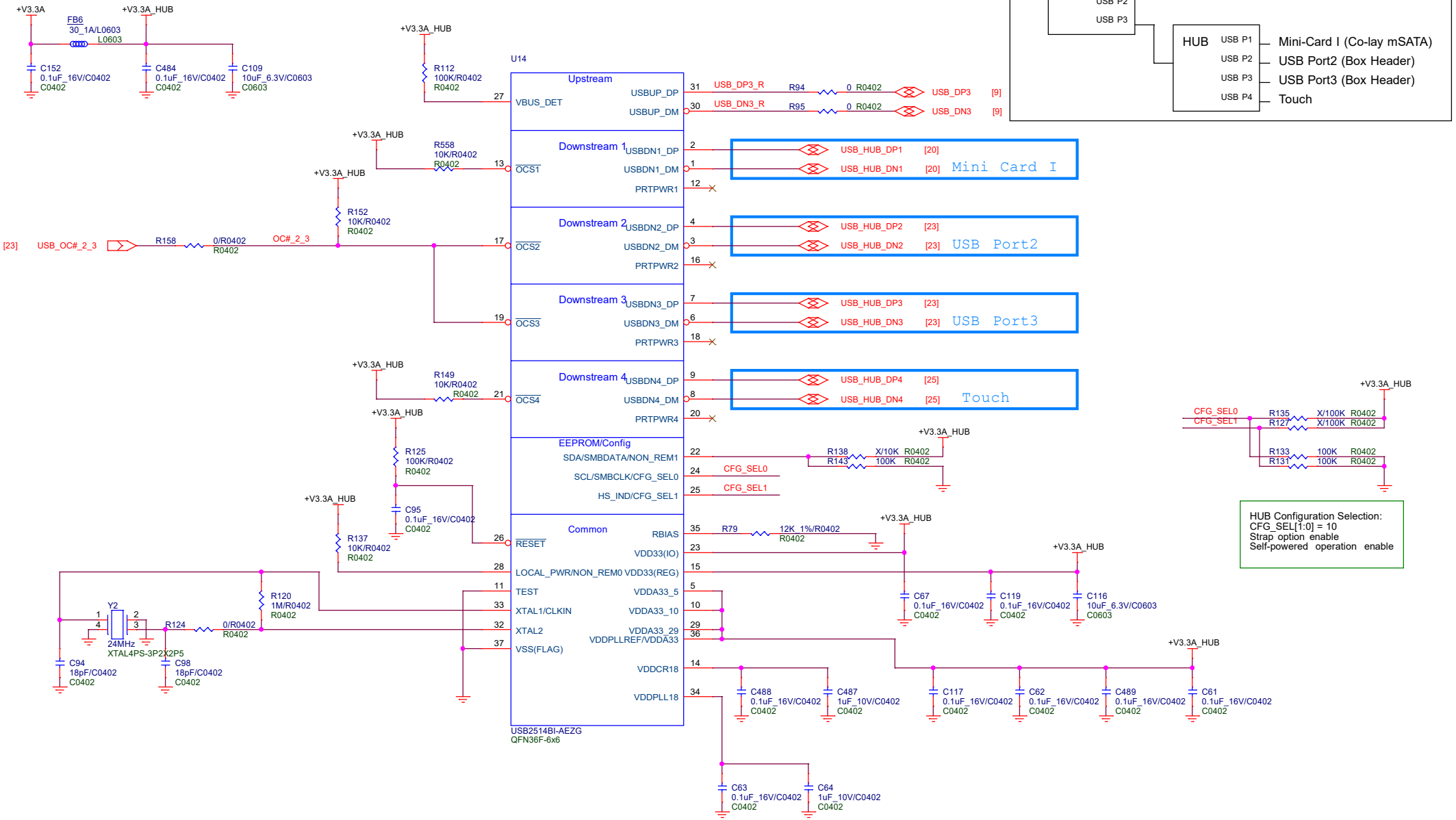
AAEON an ASUS assoc. co.	Title: mSATA, MINI CARD	
Size: Custom	Document Number: GENE0-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021	Sheet: 20 of 43	



Boss Hole: MH197D138

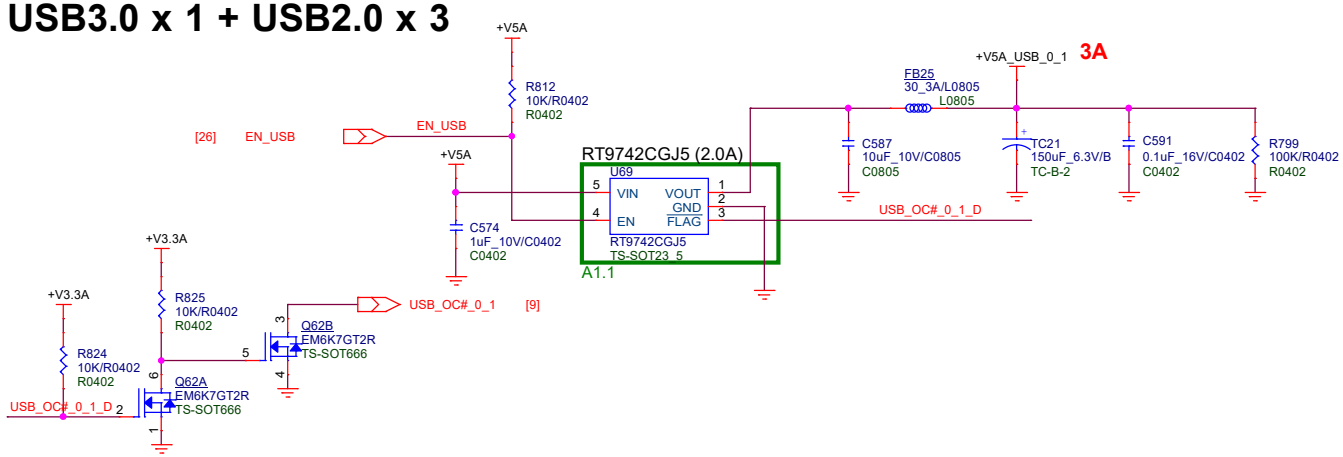
AAEON an ASUS assoc. co.	Title: MINI CARD II	
	Size: Custom	Document Number: GENE0-BT05
	Date: Monday, March 15, 2021	Sheet: 21 of 43
		Rev: A1.2_0_0

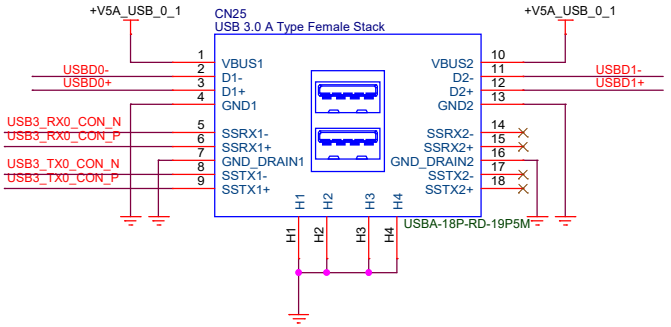
USB HUB

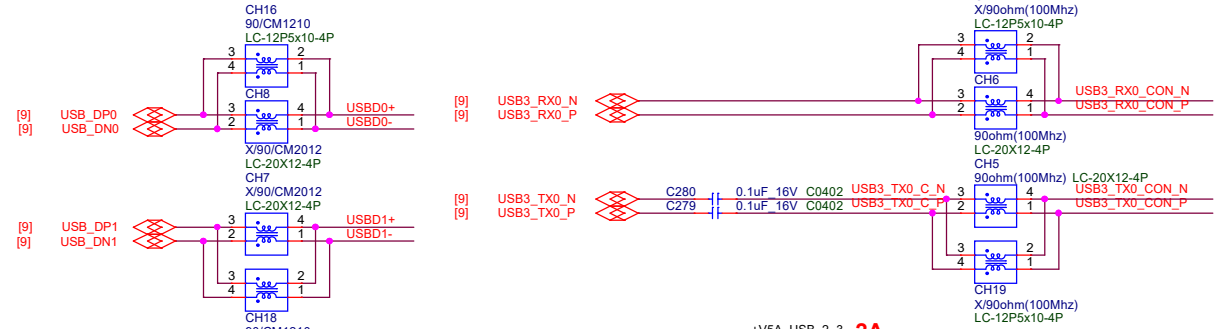


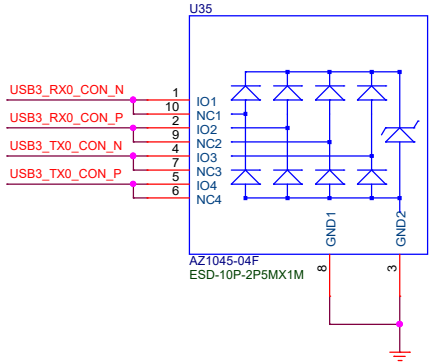
AAEON an ASUS assoc. co.	Title: USB HUB	
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021	Sheet: 22 of 43	

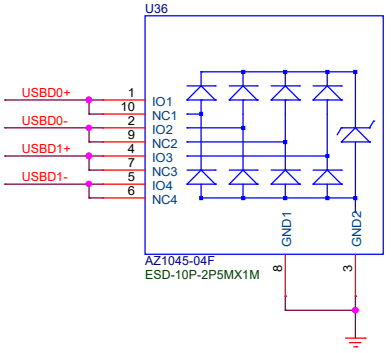
USB3.0 x 1 + USB2.0 x 3

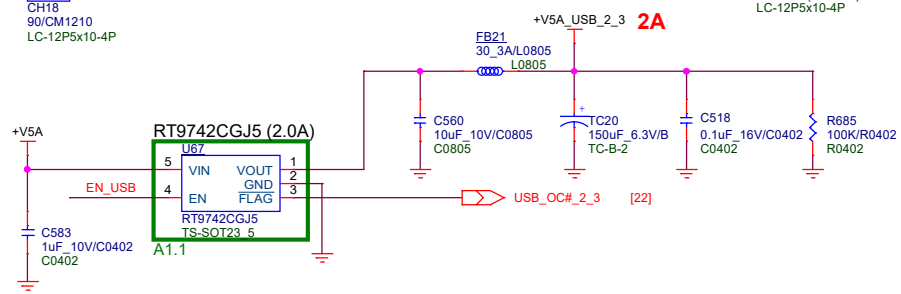


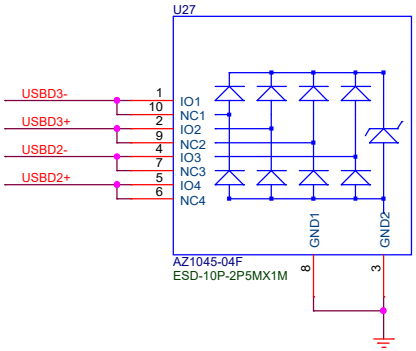


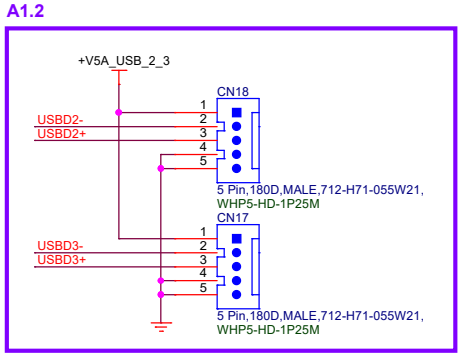


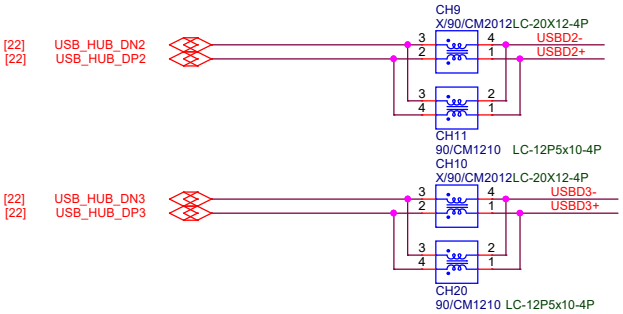










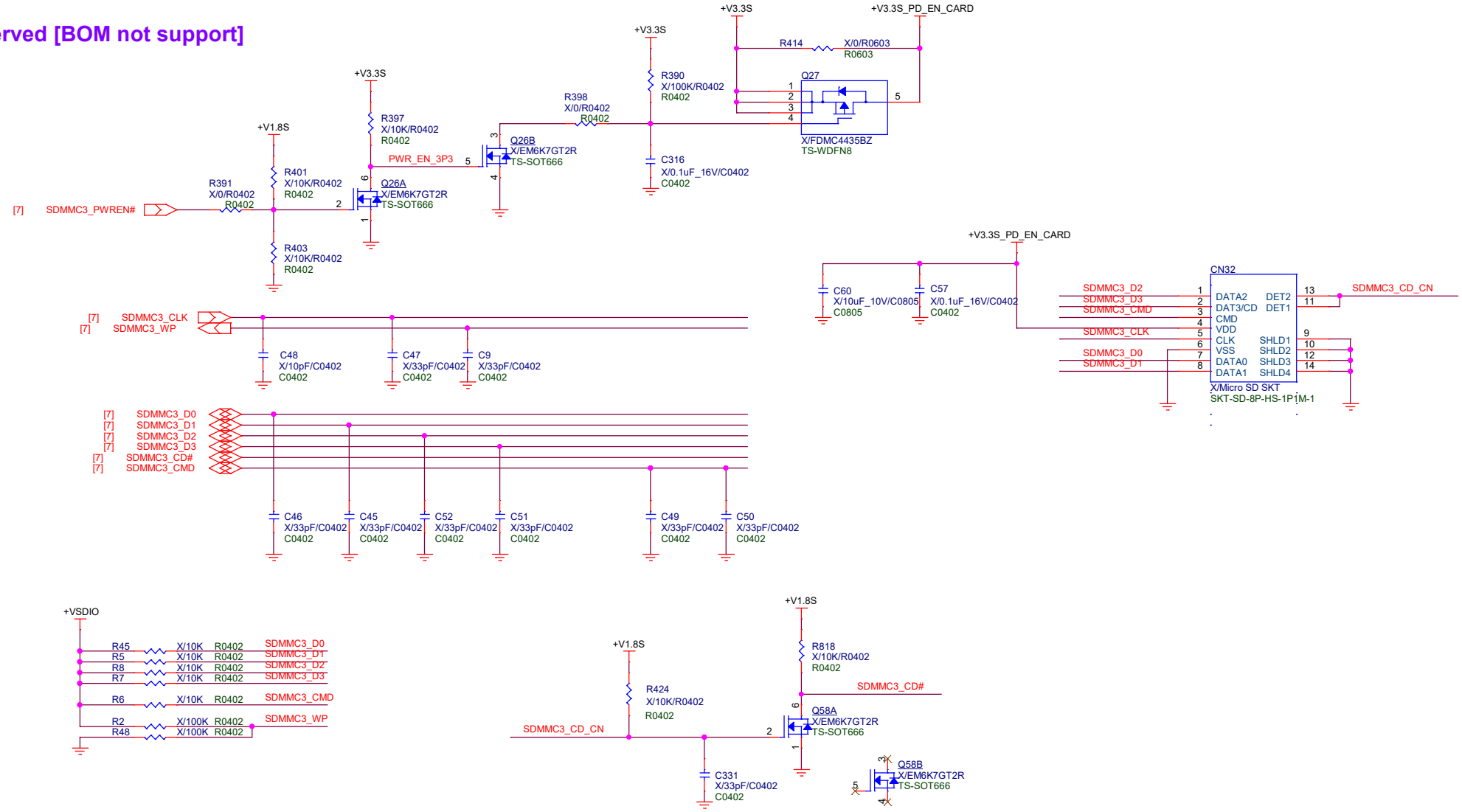


AAEON an ASUS assoc. co.

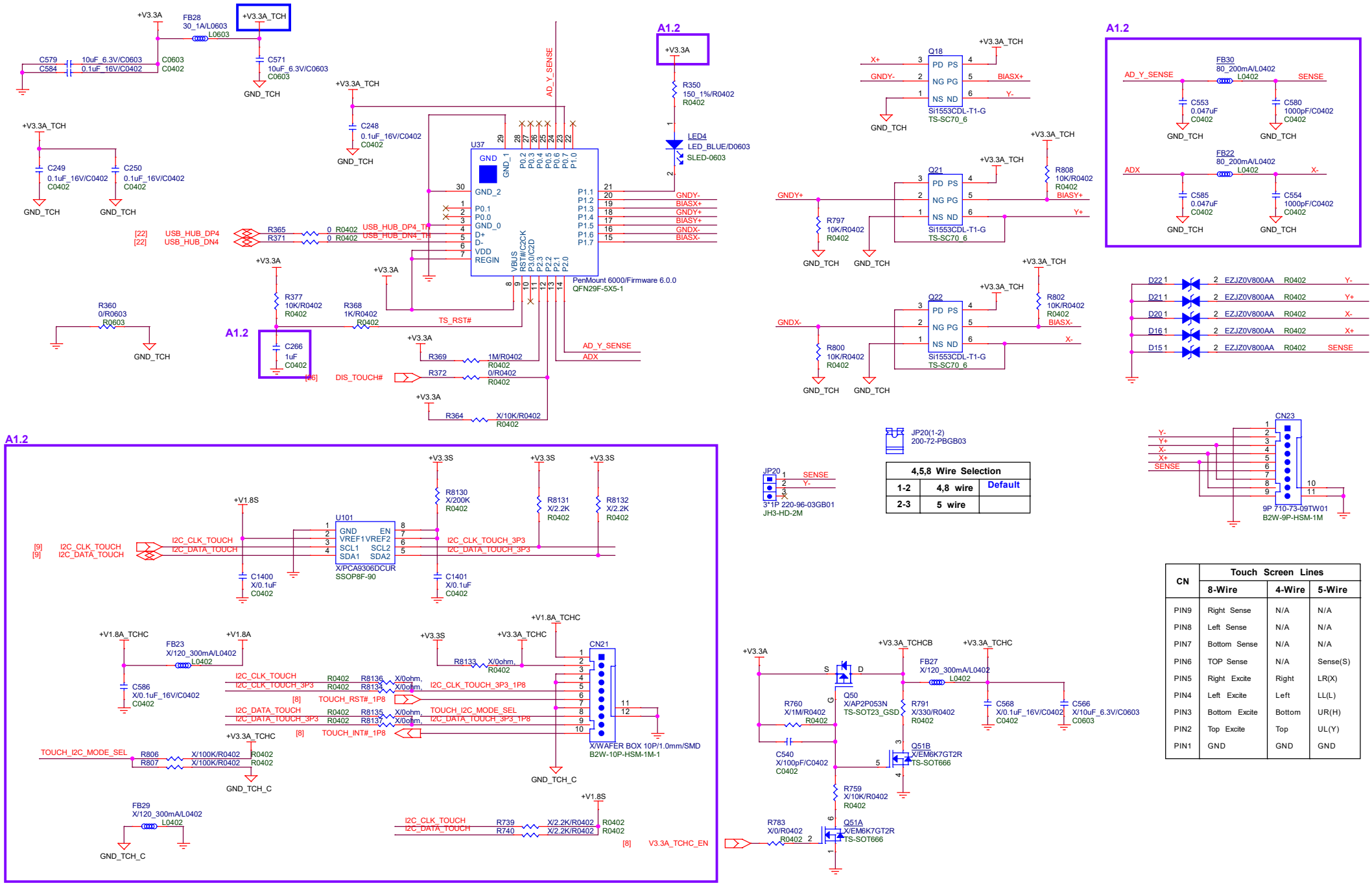
Title: USB PORT		
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021		Sheet: 23 of 43

SD

Reserved [BOM not support]



Title: SD		
Size: B	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021	Sheet: 24 of 43	



CN	Touch Screen Lines		
	8-Wire	4-Wire	5-Wire
PIN9	Right Sense	N/A	N/A
PIN8	Left Sense	N/A	N/A
PIN7	Bottom Sense	N/A	N/A
PIN6	TOP Sense	N/A	Sense(S)
PIN5	Right Excite	Right	LR(X)
PIN4	Left Excite	Left	LL(L)
PIN3	Bottom Excite	Bottom	UR(H)
PIN2	Top Excite	Top	UL(Y)
PIN1	GND	GND	GND

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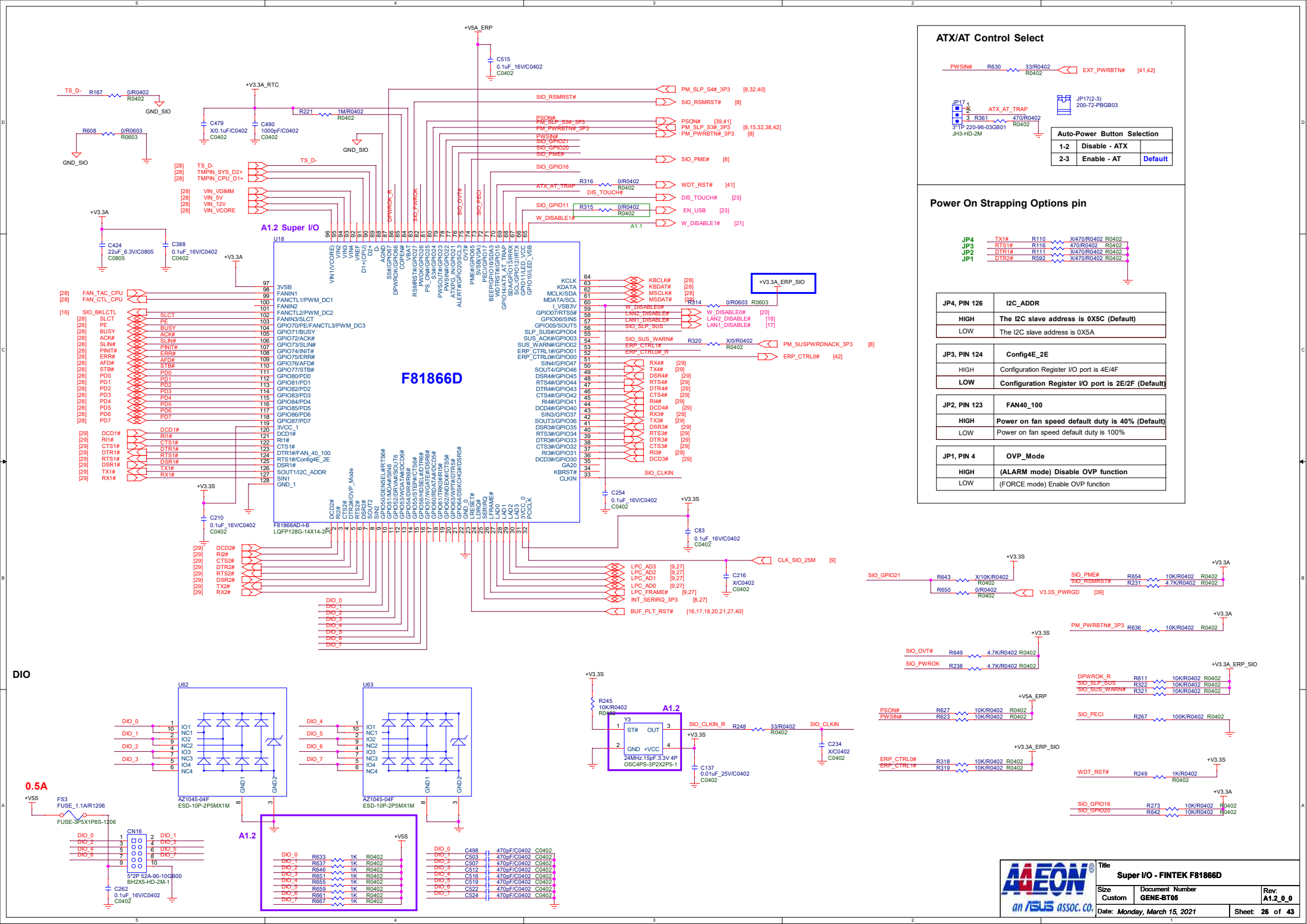
Title: TOUCH PANEL		
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021		Sheet: 25 of 43


F81866D
A1.2 Super I/O
U18
F81866AD-I-B
LQFP128G-14X14-2P0
ATX/AT Control Select
PWSIN# R630 33/R0402 R0402 EXT_PWRBTN# [41,42]
JP17 ATX_AT_TRAP 470/R0402 R0402
3*1P 220-96-03GB01 JH3-HD-2M
JP17(2-3) 200-72-PBGB03
Auto-Power Button Selection
1-2 Disable - ATX
2-3 Enable - AT Default
Power On Strapping Options pin
JP4 TX1# R110 X/470/R0402 R0402
JP3 RTS1# R116 470/R0402 R0402
JP2 DTR1# R111 X/470/R0402 R0402
JP1 DTR2# R592 X/470/R0402 R0402
JP4, PIN 126 I2C_ADDR
HIGH The I2C slave address is 0X5C (Default)
LOW The I2C slave address is 0X5A
JP3, PIN 124 Config4E_2E
HIGH Configuration Register I/O port is 4E/4F
LOW Configuration Register I/O port is 2E/2F (Default)
JP2, PIN 123 FAN40_100
HIGH Power on fan speed default duty is 40% (Default)
LOW Power on fan speed default duty is 100%
JP1, PIN 4 OVP_Mode
HIGH (ALARM mode) Disable OVP function
LOW (FORCE mode) Enable OVP function
DIO
0.5A
U62
U63
AZ1045-04F
ESD-10P-2P5MX1M
A1.2
Y3
24MHz,15pF,3.3V,4P
OSC4PS-3P2X2P5-1
CN16
5*2P 52A-90-10GB00
BH2X5-HD-2M-1
Title
Super I/O - FINTEK F81866D
Size Custom
Document Number GENE-BT05
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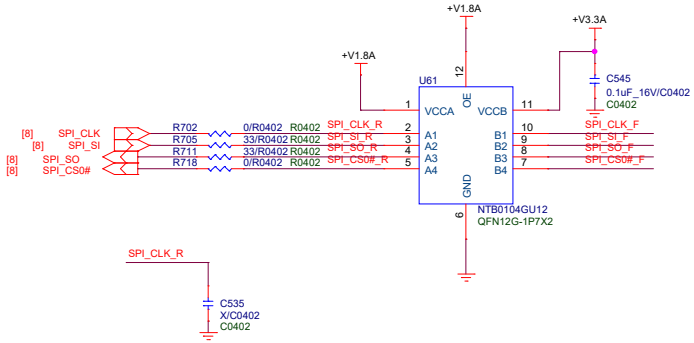
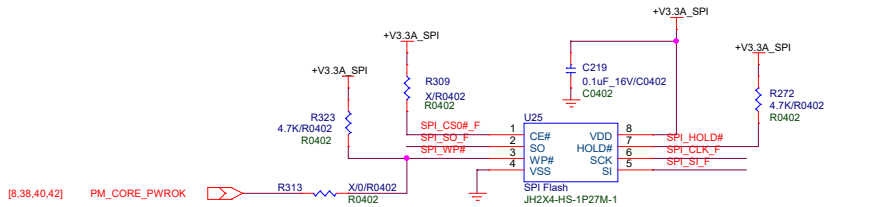
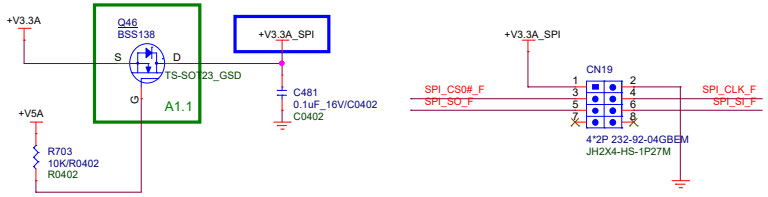
SPI BIOS

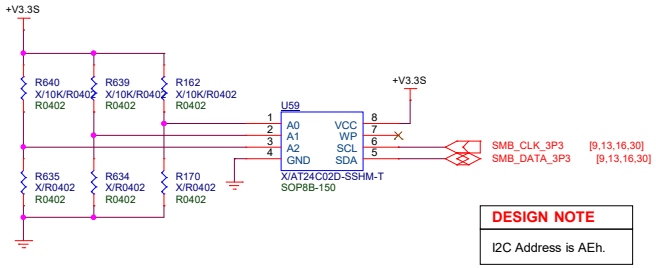




8 pin :
1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0
14S6206404 (AOH)(TF)IC.64 Mbit SPI Flash.SOIC-8P.208mil.SMD.Winbond.W25Q64JVSSIQ



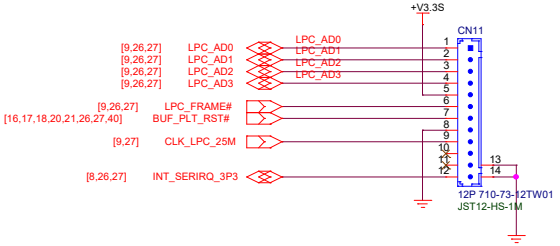
CMOS Backup



DESIGN NOTE

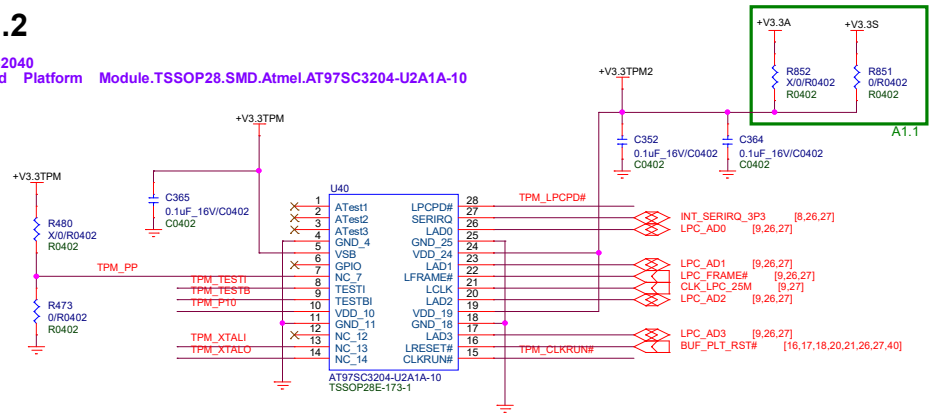
I2C Address is AEh.

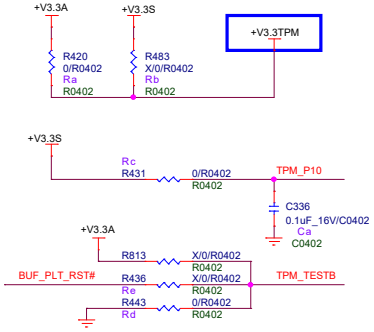
LPC Connector

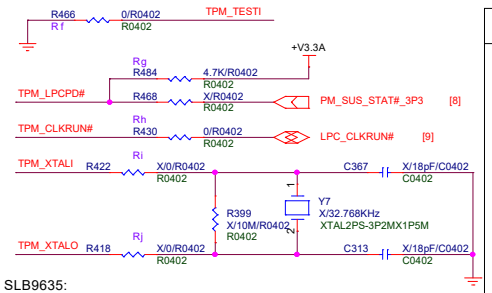


TPM 1.2

BOM: 1440032040
(TF)IC.Trusted Platform Module.TSSOP28.SMD.Atmel.AT97SC3204-U2A1A-10







DESIGN NOTE

TESTB = High, Addr = 4EH / 4FH

SLB9635:
Ra=1; Rb=0; Rc=0; Rd=1; Re=0; Rf=1;
Rg=1; Rh=1; Ri=1; Rj=1; Ca=0

SLB9665:
Ra=0; Rb=1; Rc=1; Rd=0; Re=1; Rf=0;
Rg=0; Rh=0; Ri=0 ; Rj=0; Ca=1

AT24C256C
Ra=1; Rb=0; Rc=1; Rd=1; Re=0; Rf=1;
Rg=1; Rh=1; Ri=0; Rj=0; Ca=1

PIN		AT24C256C	
1	15	ATest	LPCPD#
2	16	ATest	SERIRQ
3	17	ATest	LAD0
4	18	GND	GND
5	19	VSB	VDD
6	20	GPIO	LAD1
7	21	NC	LFRAME#
8	22	TESTI	LCLK
9	23	TESTB	LAD2
10	24	VDD	VDD
11	25	GND	GND
12	26	NC	LAD3
13	27	NC	LRESET#
14	28	NC	CLKRUN#

PIN				SLB9665	
1	15	NC	LPCPD#	NC	NC
2	16	GPIO2	SERIRQ	NC	SERIRQ
3	17	NC	LAD0	NC	LAD0
4	18	GND	GND	GND	GND
5	19	VSB	VDD	VDD	VDD
6	20	GPIO	LAD1	GPIO	LAD1
7	21	PP	LFRAME#	PP	LFRAME#
8	22	TESTI	LCLK	NC	LCLK
9	23	TESTB	LAD2	LRESET#	LAD2
10	24	NC	VDD	VDD	VDD
11	25	GND	GND	GND	GND
12	26	NC	LAD3	NC	LAD3
13	27	XTALI/32KIN	LRESET#	NC	LRESET#
14	28	XTALO	CLKRUN#	NC	NC

AAEON an ASUS assoc. co.

Title: **SPI BIOS,TPM,CMOS BACKUP**

Size	Document Number	Rev:
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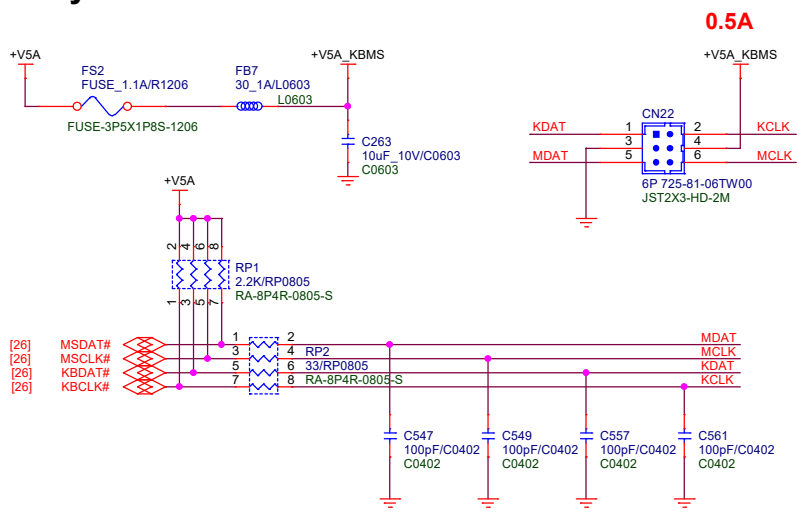
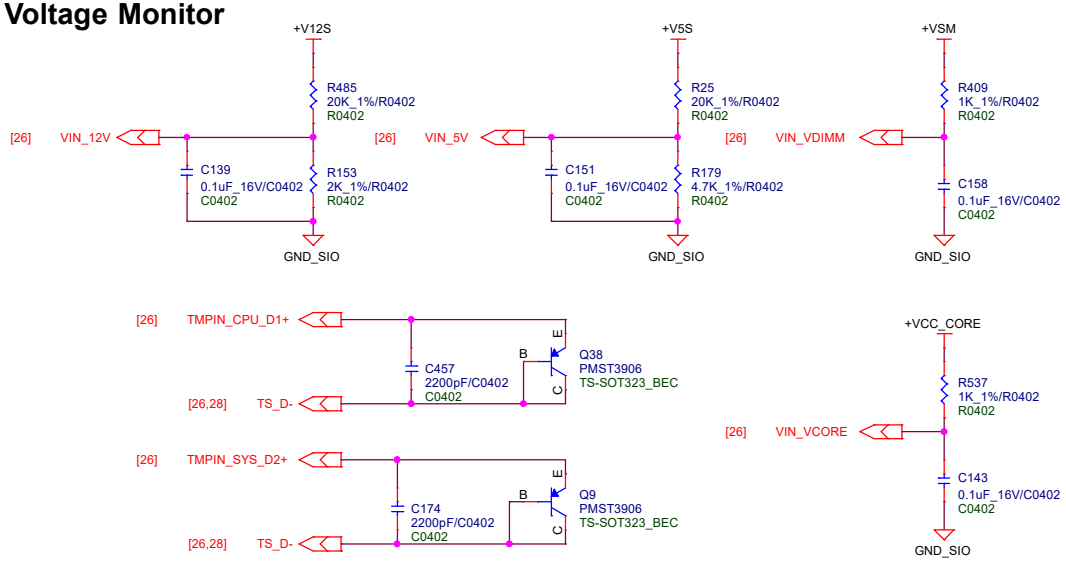
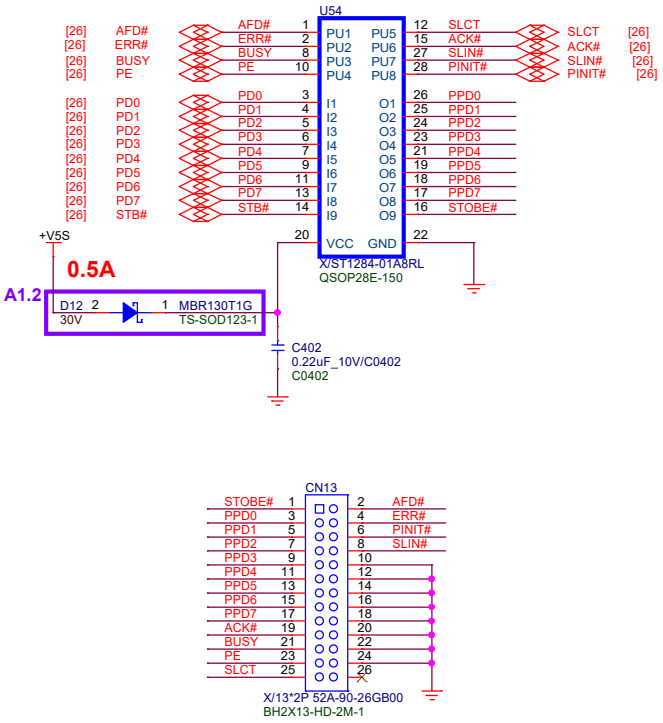
PS/2 Keyboard/Mouse



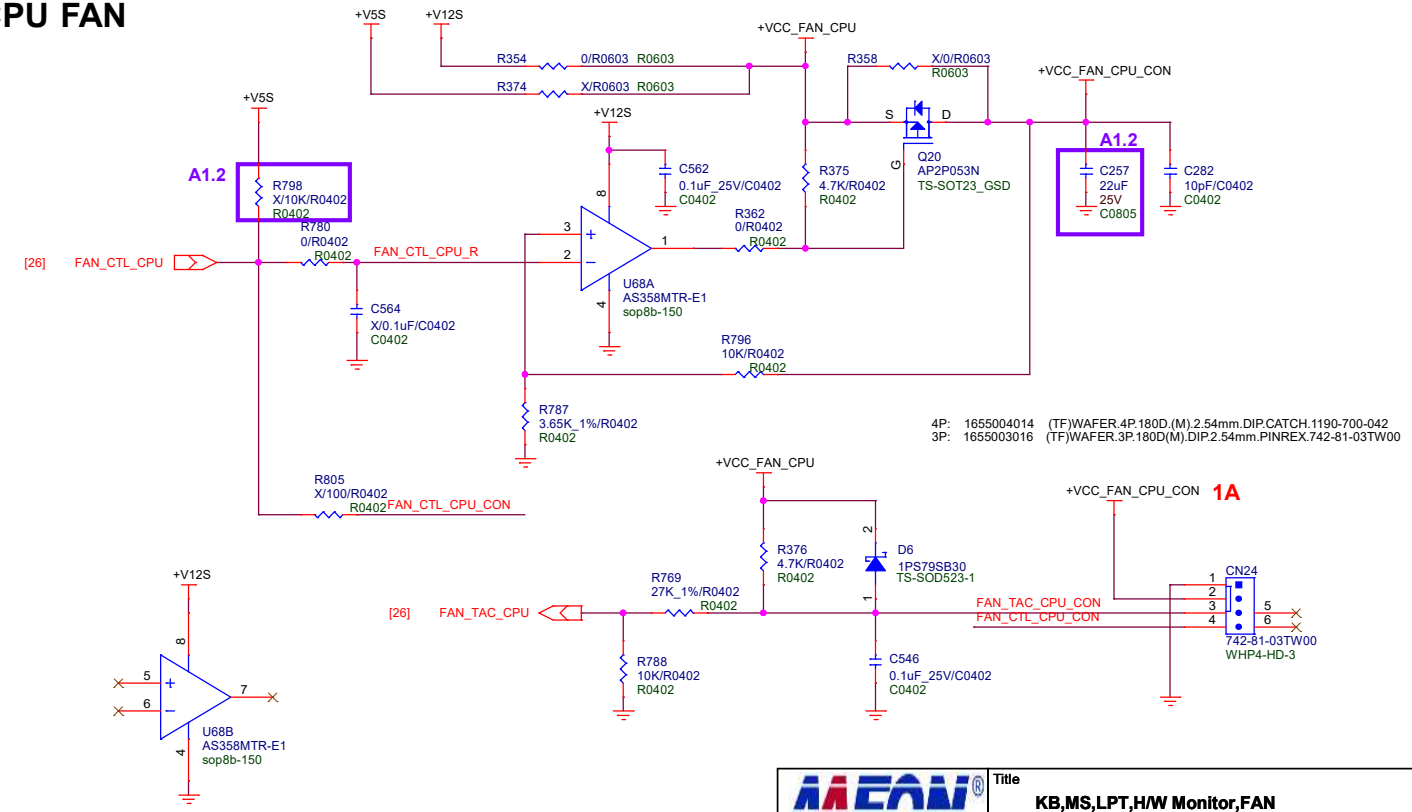
Voltage Monitor



LPT



CPU FAN

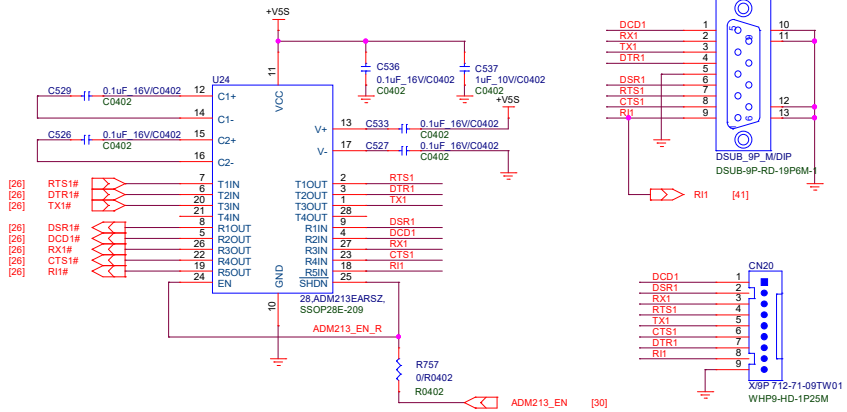


Title: KB,MS,LPT,H/W Monitor,FAN		
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021		Sheet: 28 of 43

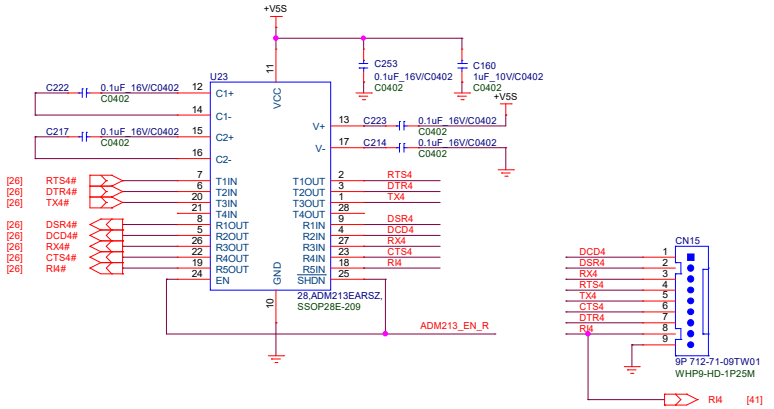
AAEON an ASUS assoc. co.

A1.2

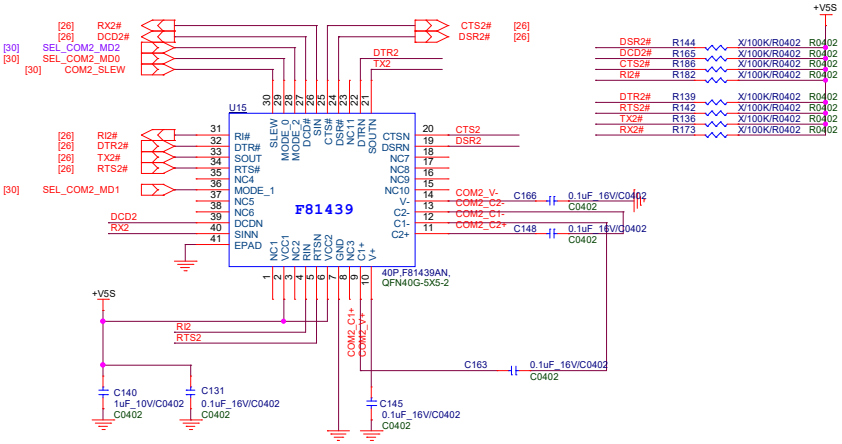
COM1



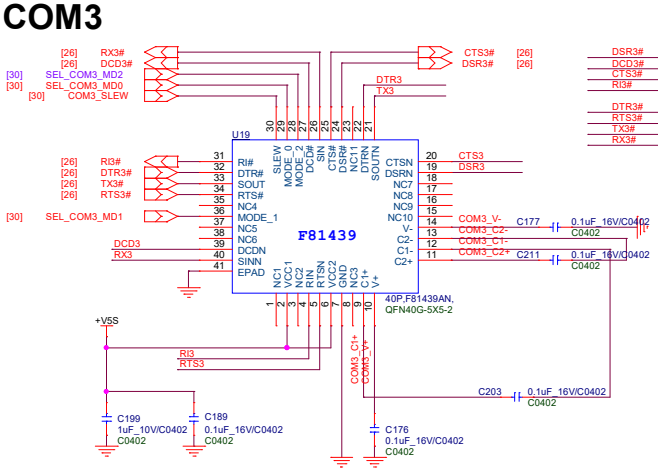
COM4

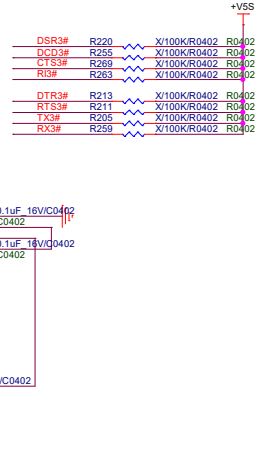


COM2



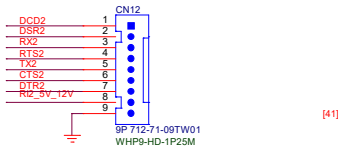
COM3

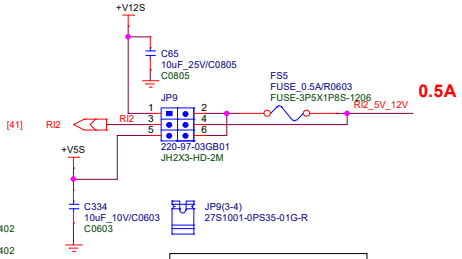




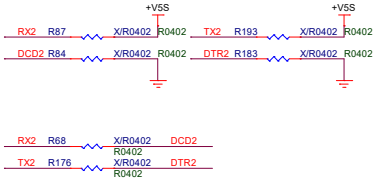
Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

Pin Mapping			
	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

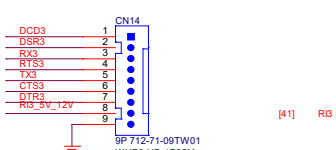


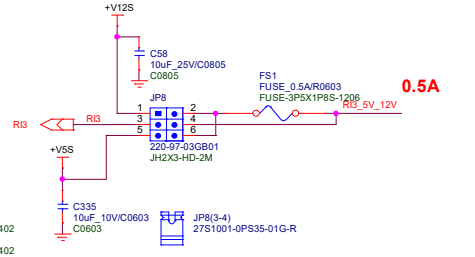


Reserved for FAIL-SAVE.

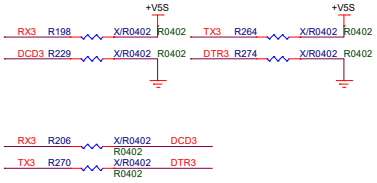


COM2 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	





Reserved for FAIL-SAVE.



COM3 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

AAEON an ASUS assoc. co.

Title: COM1,COM2,COM3,COM4

Size: Custom | Document Number: GENE-BT05 | Rev: A1.2_0_0

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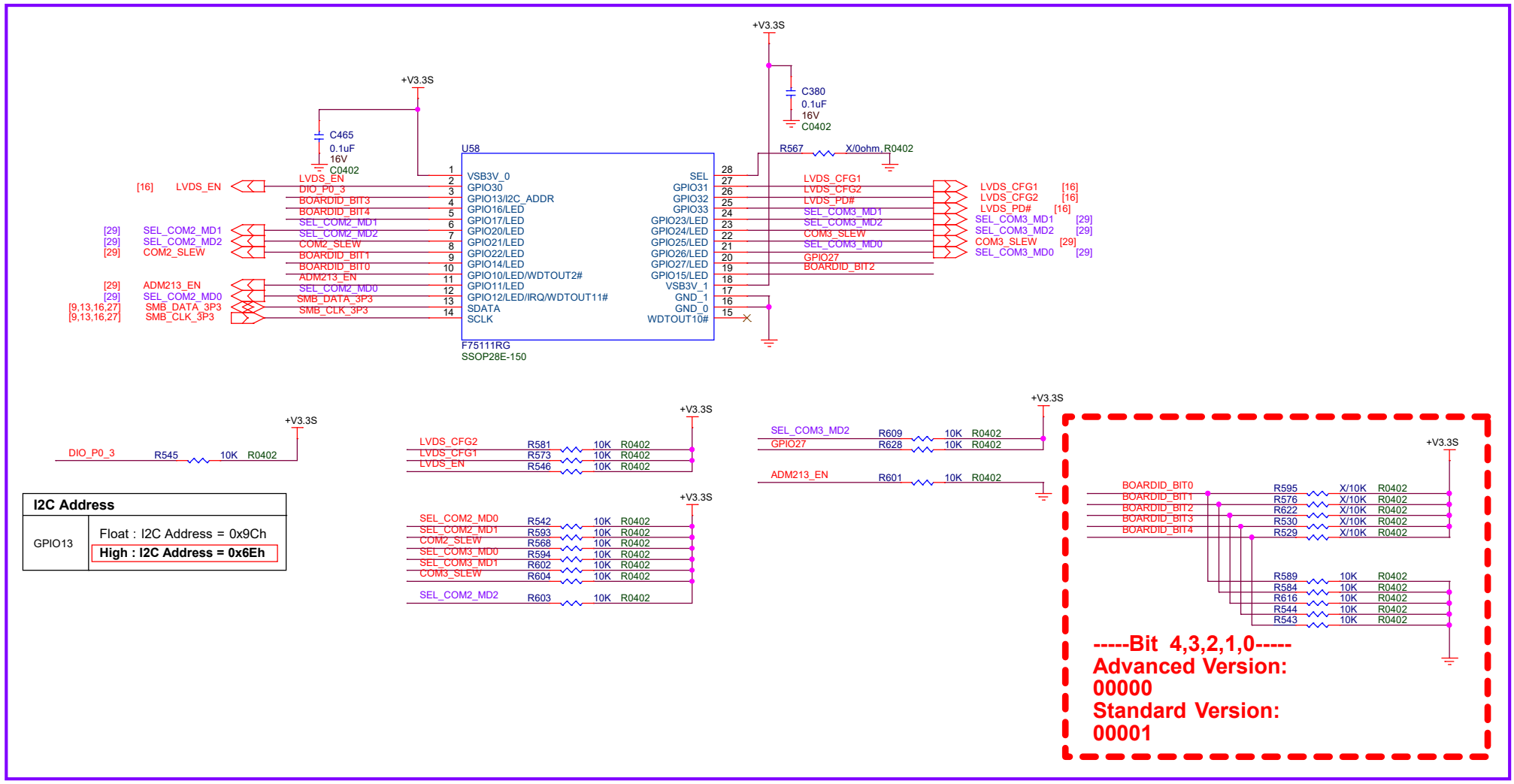
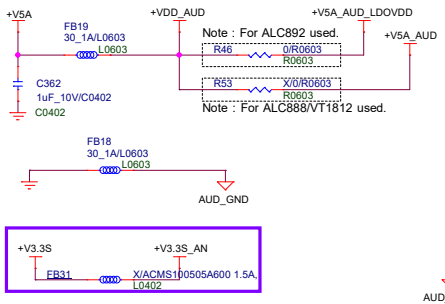
GPIO - F75111RG

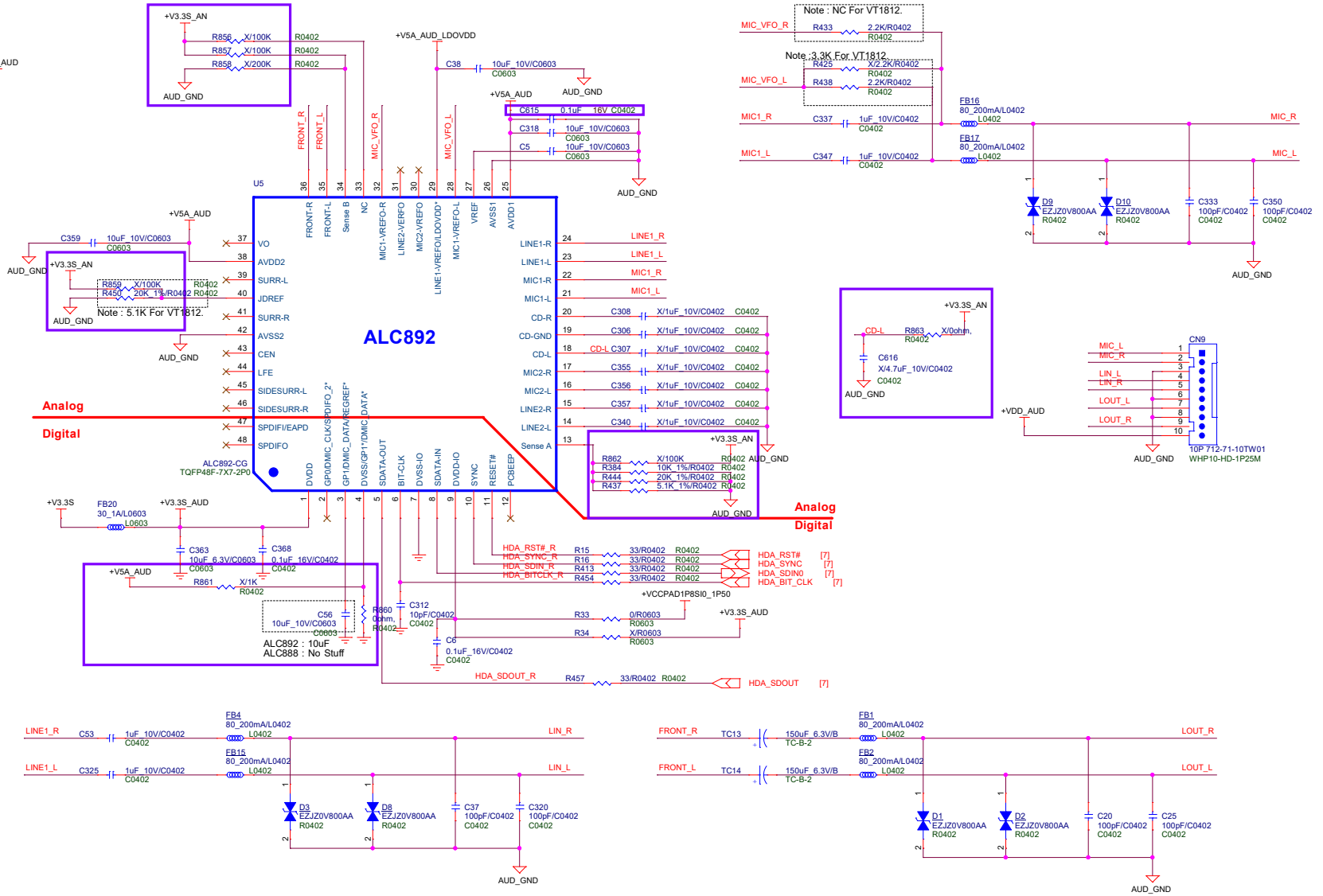


AAEON an ASUS assoc. co.	Title: GPIO F75111	
Size: B	Document Number: GENE-BT05	Rev: A1.2_0_0
Date: Monday, March 15, 2021	Sheet: 30 of 43	

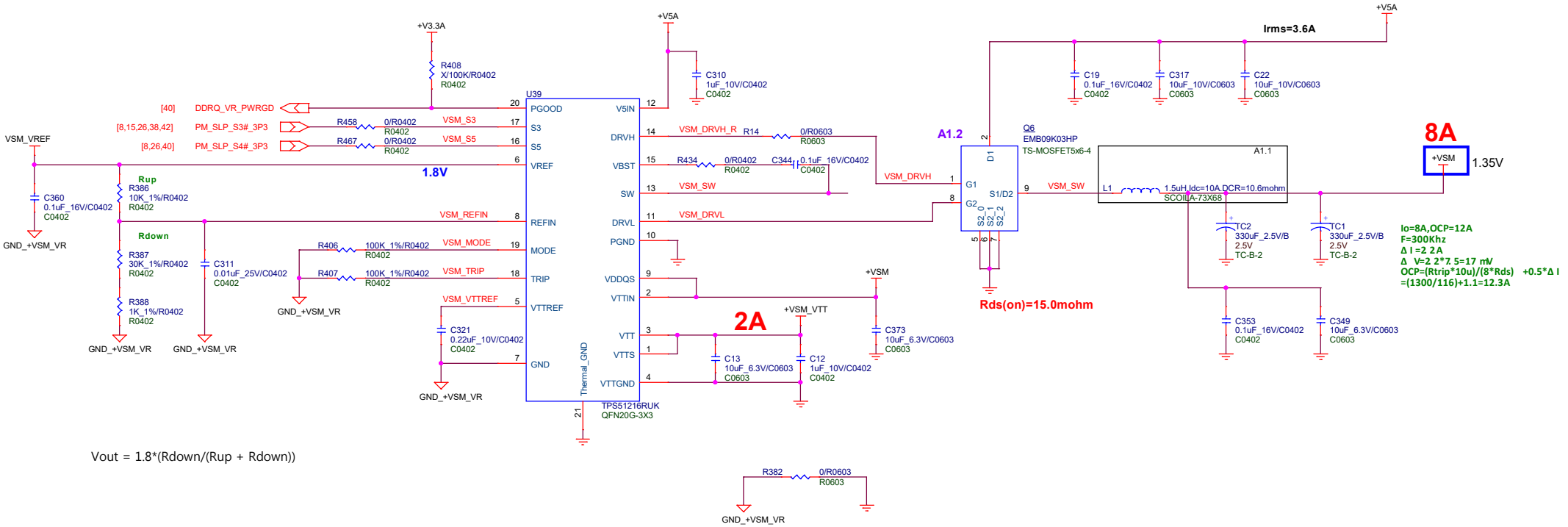
A1.2



	ALC888S/ALC892	ALC897
C308	X	4.7uF
C306	X	0
R862	X	100K
C318	10uF	4.7uF
C5	10uF	2.2uF
R861	X	1K(-VA1)/X(-VA2)
C56	10uF	4.7uF
R856	X	100K
R857	X	100K
R858	X	200K
R450	20K	200K
R859	X	100K
C307	X	0.1uF
C616	X	4.7uF
R863	X	0
R437	5.1K	200K
R444	20K	X
R384	10K	X
C359	10uF	X
FB31	X	Bead



DDR3L Power



Vout = 1.8*(Rdown/(Rup + Rdown))

MODE Selection

Resistance(K ohm)	SW Frequency(kHz)	Discharge Mode
200	400	Tracking
100	300	Tracking
68	300	Non-tracking
47	400	Non-tracking

S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF
S4/S5	LO	LO	OFF	OFF	OFF	OFF

Title: Power VR - +VSM		
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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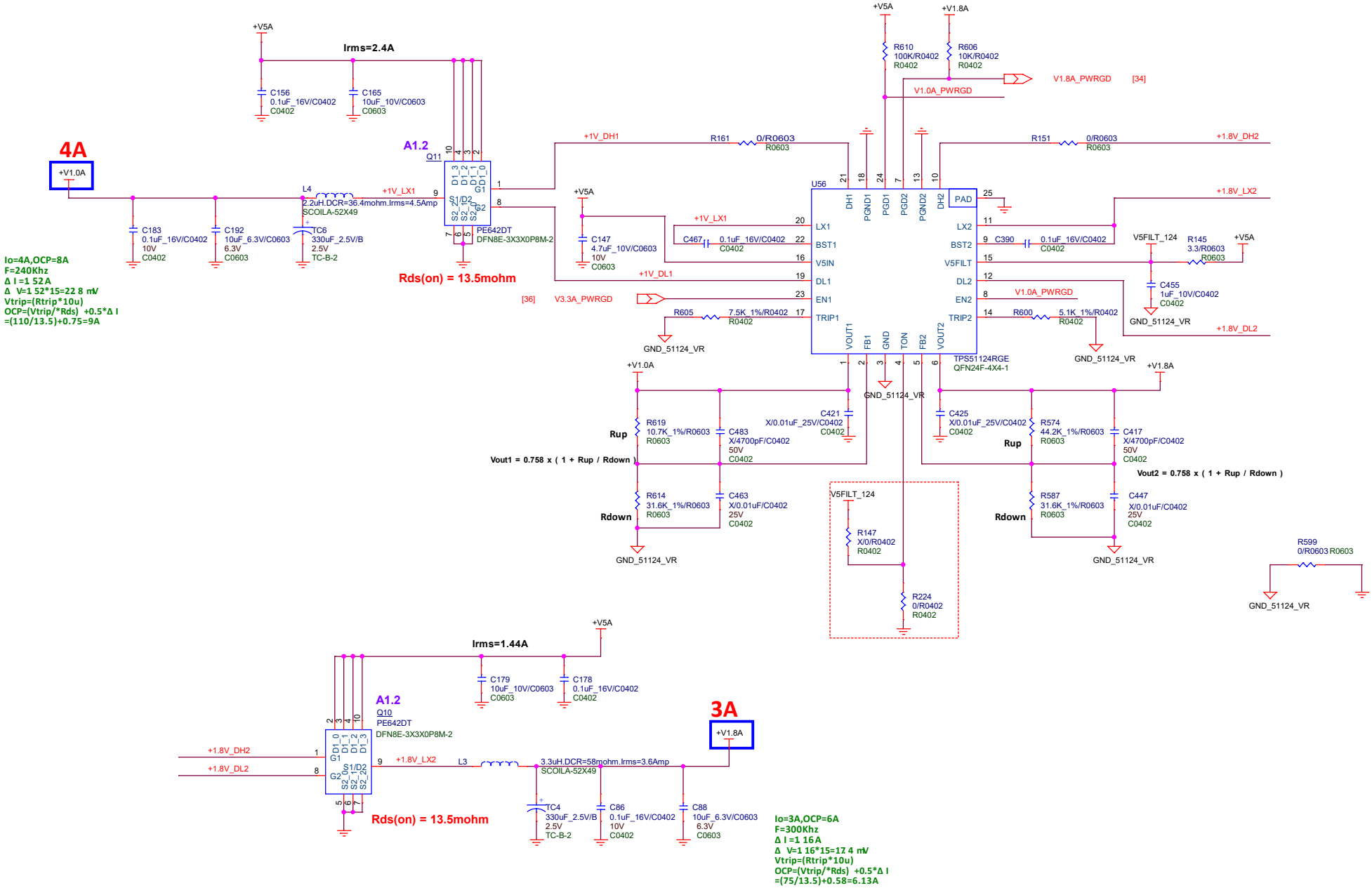
+V1.0A, +V1.8A



AAEON an ASUS assoc. co.	Title: POWER VR_+V1.0A_+V1.8A	
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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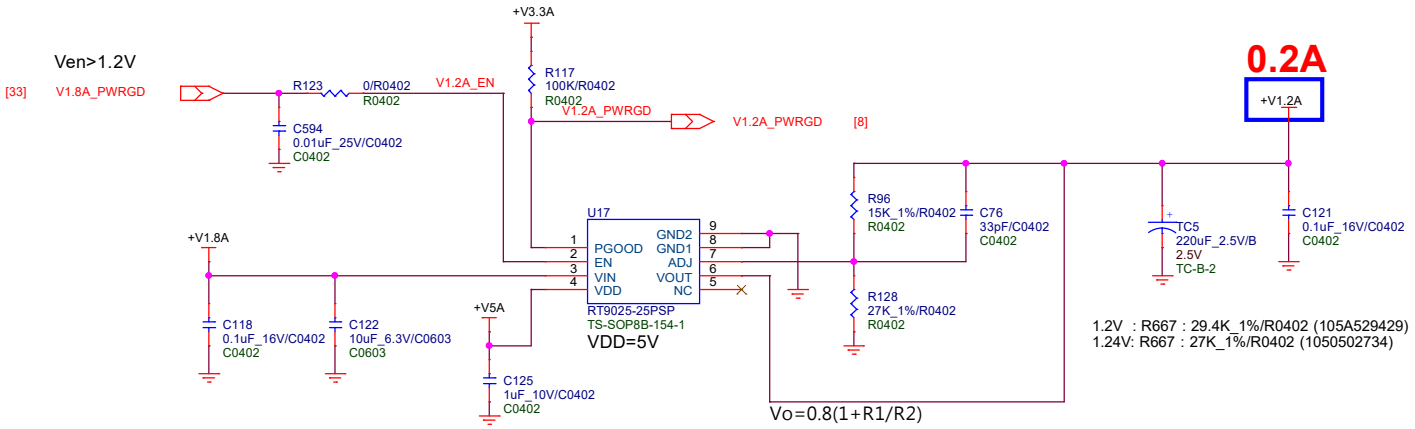
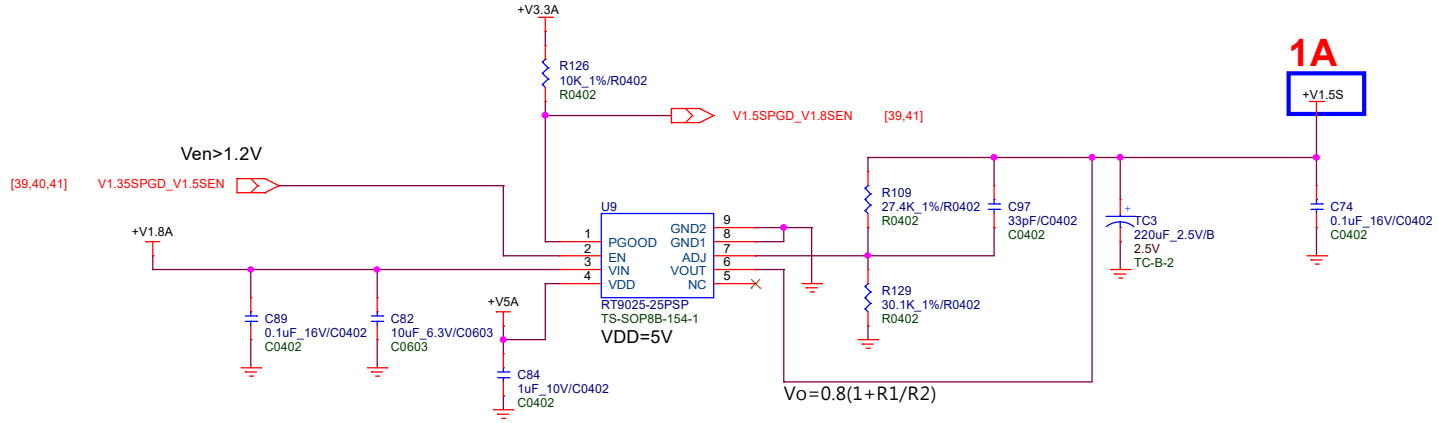
+V1.2A



+V1.5S



AAEON an ASUS assoc. co.

Title: Power VR : +V1.2A, +V1.5S		
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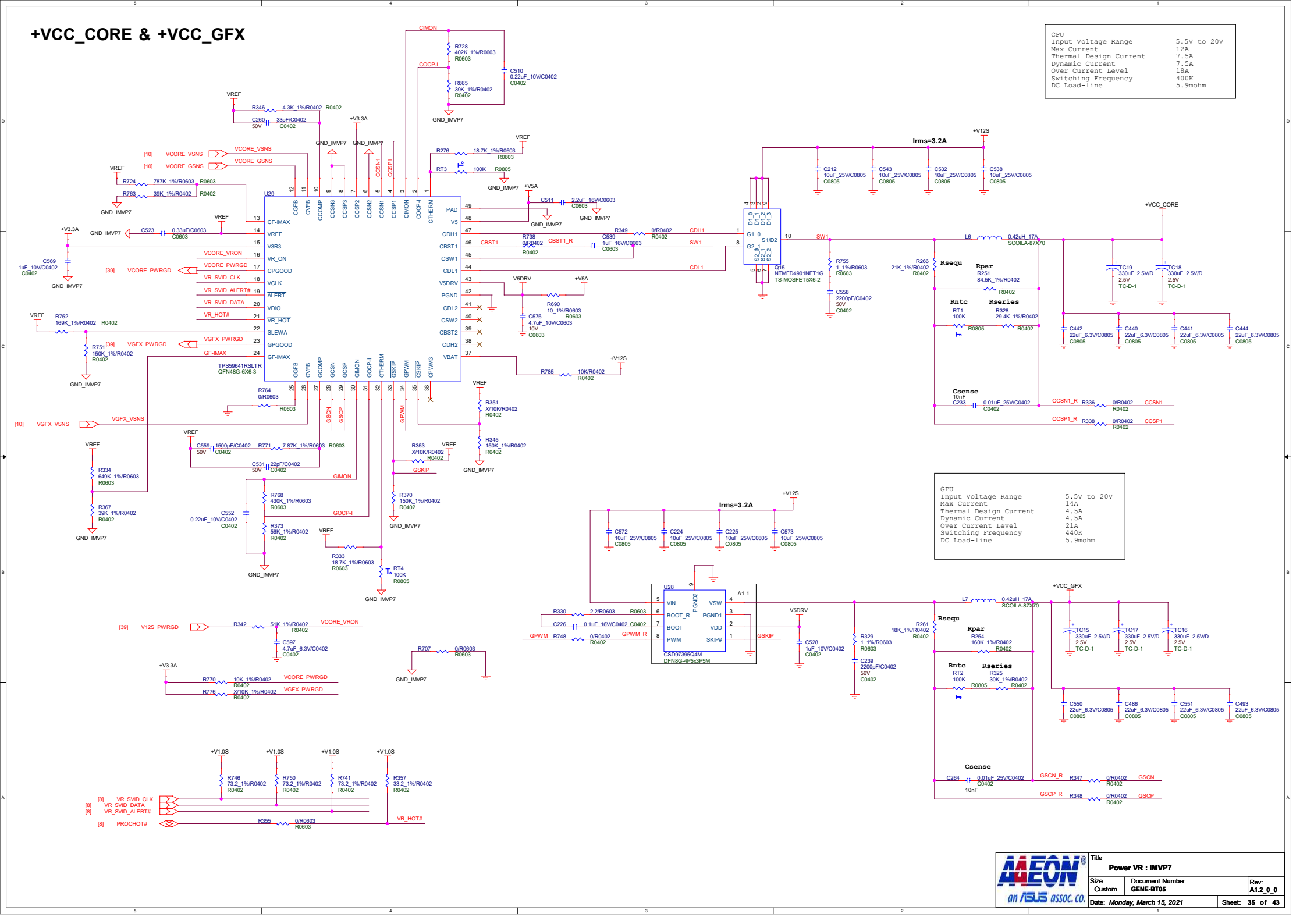
+VCC_CORE & +VCC_GFX

CPU	
Input Voltage Range	5.5V to 20V
Max Current	12A
Thermal Design Current	7.5A
Dynamic Current	7.5A
Over Current Level	18A
Switching Frequency	400K
DC Load-line	5.9mohm

GPU	
Input Voltage Range	5.5V to 20V
Max Current	14A
Thermal Design Current	4.5A
Dynamic Current	4.5A
Over Current Level	21A
Switching Frequency	440K
DC Load-line	5.9mohm



Title	Power VR : IMVP7		
Size: Custom	Document Number: GENE-BT05		Rev: A1.2_0_0
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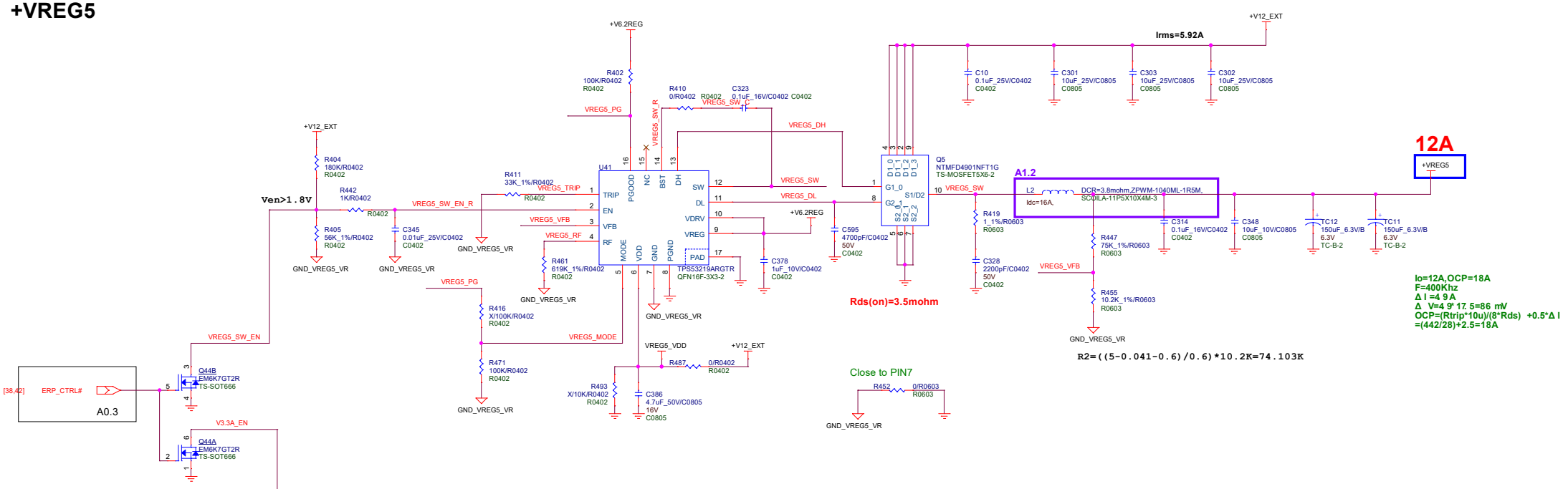
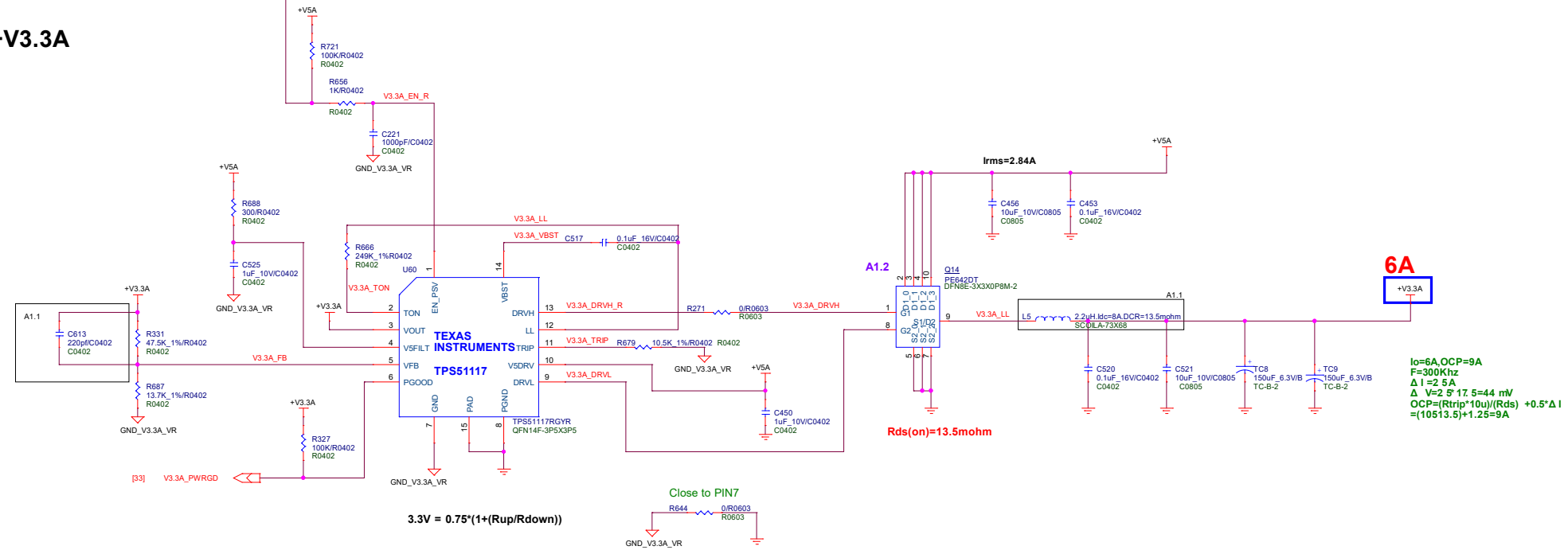
+VREG5



+V3.3A



Title: POWER VR: +VREG5, +V3.3A			
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0	
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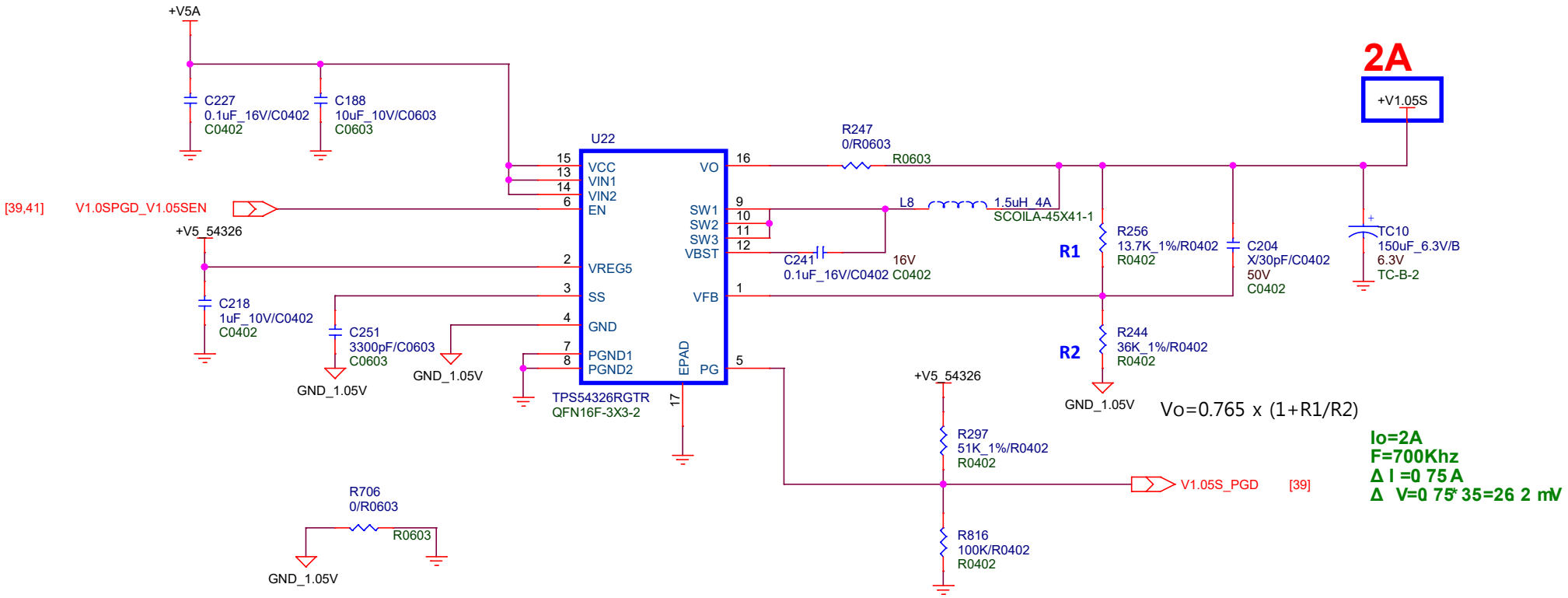
+V1.05S



AAEON an ASUS assoc. co.	Title: POWER VR_+V1.05S	
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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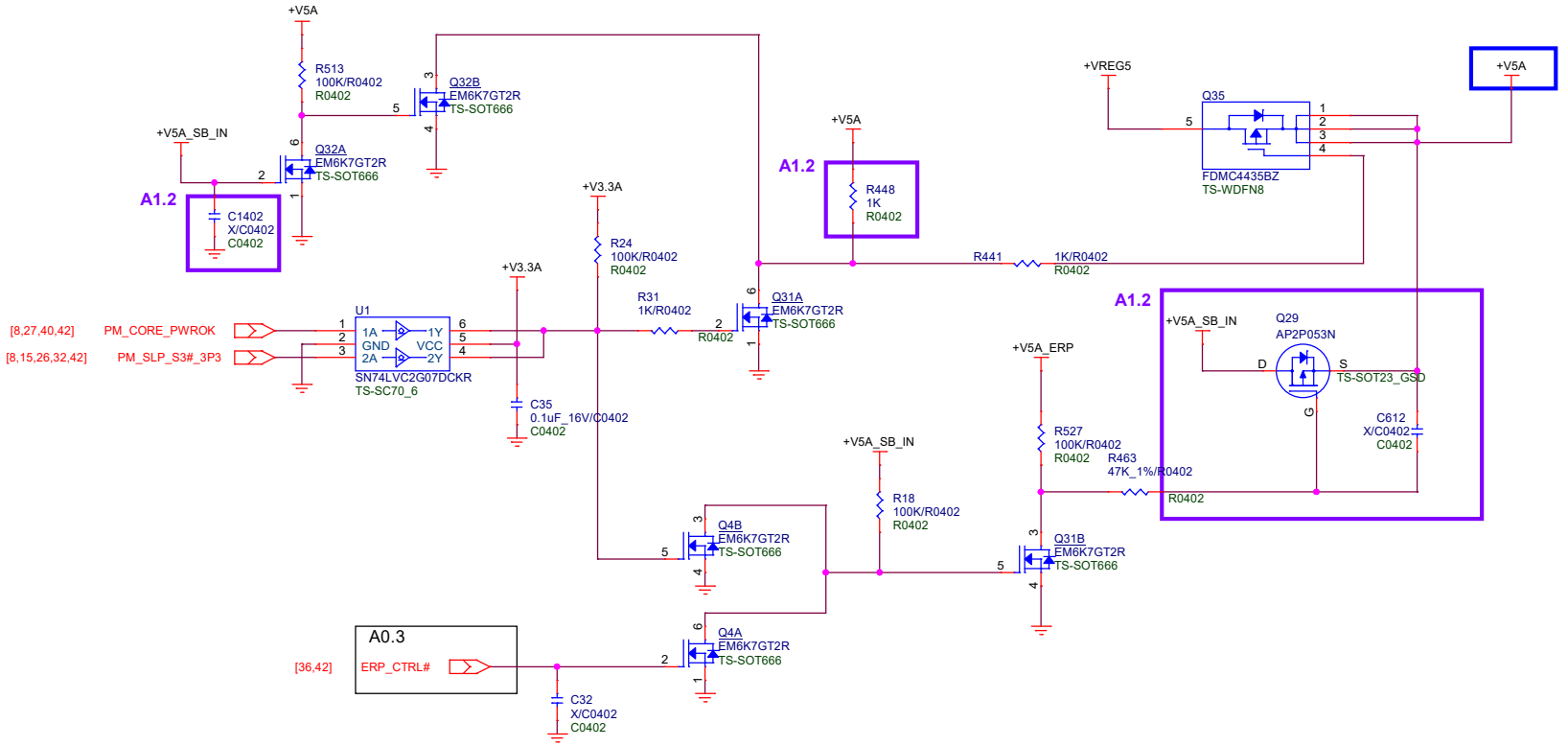
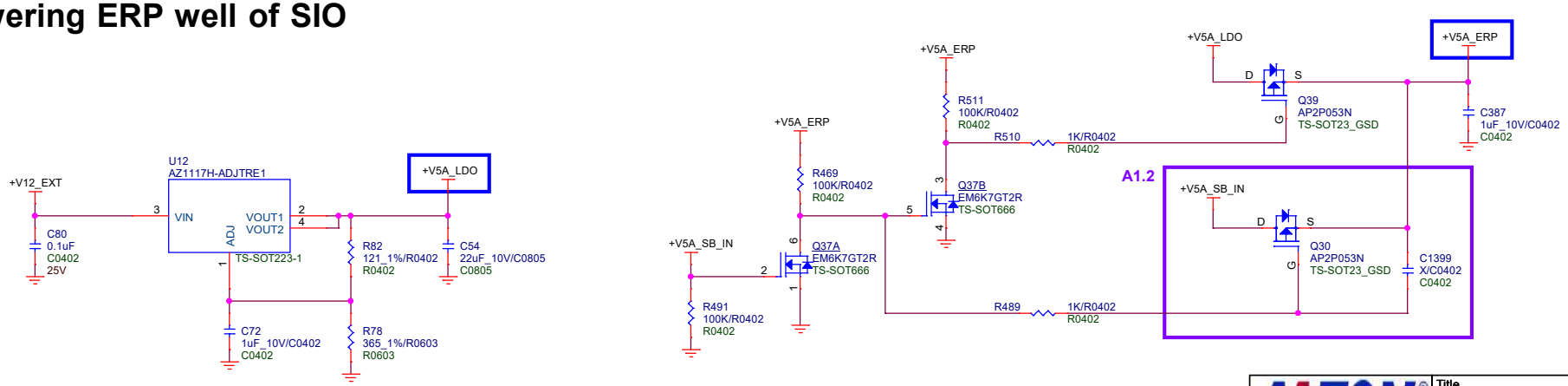
5VDAUL Switch Circuit



Powering ERP well of SIO



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Title: Standby Power		
Size: Custom	Document Number: GENE-BT05	Rev: A1.2_0_0
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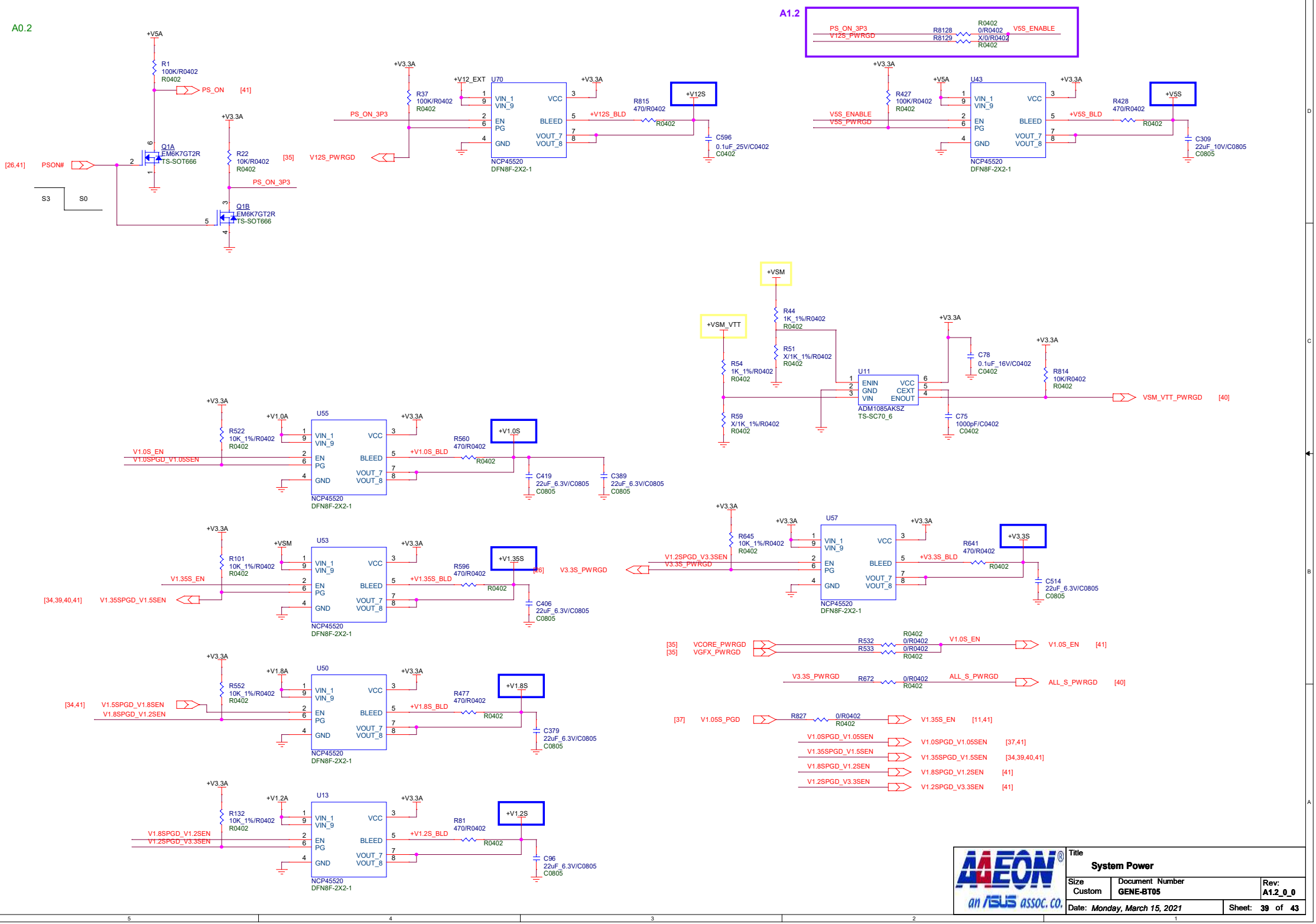
A0.2
A1.2
PS_ON_3P3
V12S_PWRGD
R8128
R8129
R0402
0/R0402
X/0/R0402
V5S_ENABLE
+V5A
R1
100K/R0402
PS_ON
[41]
[26,41]
PSON#
Q1A
EM6K7GT2R
TS-SOT666
Q1B
R22
10K/R0402
[35]
S3
S0
+V3.3A
+V12_EXT
U70
R37
100K/R0402
VIN_1
VIN_9
EN
PG
GND
VCC
BLEED
VOUT_7
VOUT_8
+V12S_BLD
R815
470/R0402
+V12S
C596
0.1uF_25V/C0402
C0402
NCP45520
DFN8F-2X2-1
U43
R427
V5S_PWRGD
+V5S_BLD
R428
470/R0402
+V5S
C309
22uF_10V/C0805
C0805
+VSM
+VSM_VTT
R44
1K_1%/R0402
R51
X/1K_1%/R0402
R54
R59
U11
ENIN
GND
VIN
VCC
CEXT
ENOUT
ADM1085AKSZ
TS-SC70_6
C78
0.1uF_16V/C0402
R814
10K/R0402
VSM_VTT_PWRGD
[40]
C75
1000pF/C0402
U55
R522
V1.0S_EN
V1.0SPGD_V1.05SEN
+V1.0A
+V1.0S_BLD
R560
470/R0402
+V1.0S
C419
22uF_6.3V/C0805
C389
22uF_6.3V/C0805
U53
R101
+VSM
V1.35S_EN
[34,39,40,41]
V1.35SPGD_V1.5SEN
+V1.35S_BLD
R596
470/R0402
+V1.35S
[26]
V3.3S_PWRGD
C406
22uF_6.3V/C0805
U57
R645
V1.2SPGD_V3.3SEN
V3.3S_PWRGD
+V3.3S_BLD
R641
470/R0402
+V3.3S
C514
22uF_6.3V/C0805
[35]
VCORE_PWRGD
VGFX_PWRGD
R532
R533
V1.0S_EN
[41]
R672
ALL_S_PWRGD
[40]
[37]
V1.05S_PGD
R827
V1.35S_EN
[11,41]
V1.0SPGD_V1.05SEN
[37,41]
V1.35SPGD_V1.5SEN
[34,39,40,41]
V1.8SPGD_V1.2SEN
[41]
V1.2SPGD_V3.3SEN
U50
R552
[34,41]
V1.5SPGD_V1.8SEN
V1.8SPGD_V1.2SEN
+V1.8A
+V1.8S_BLD
R477
470/R0402
+V1.8S
C379
22uF_6.3V/C0805
U13
R132
V1.8SPGD_V1.2SEN
V1.2SPGD_V3.3SEN
+V1.2A
+V1.2S_BLD
R81
470/R0402
+V1.2S
C96
22uF_6.3V/C0805
Title
System Power
Size
Custom
Document Number
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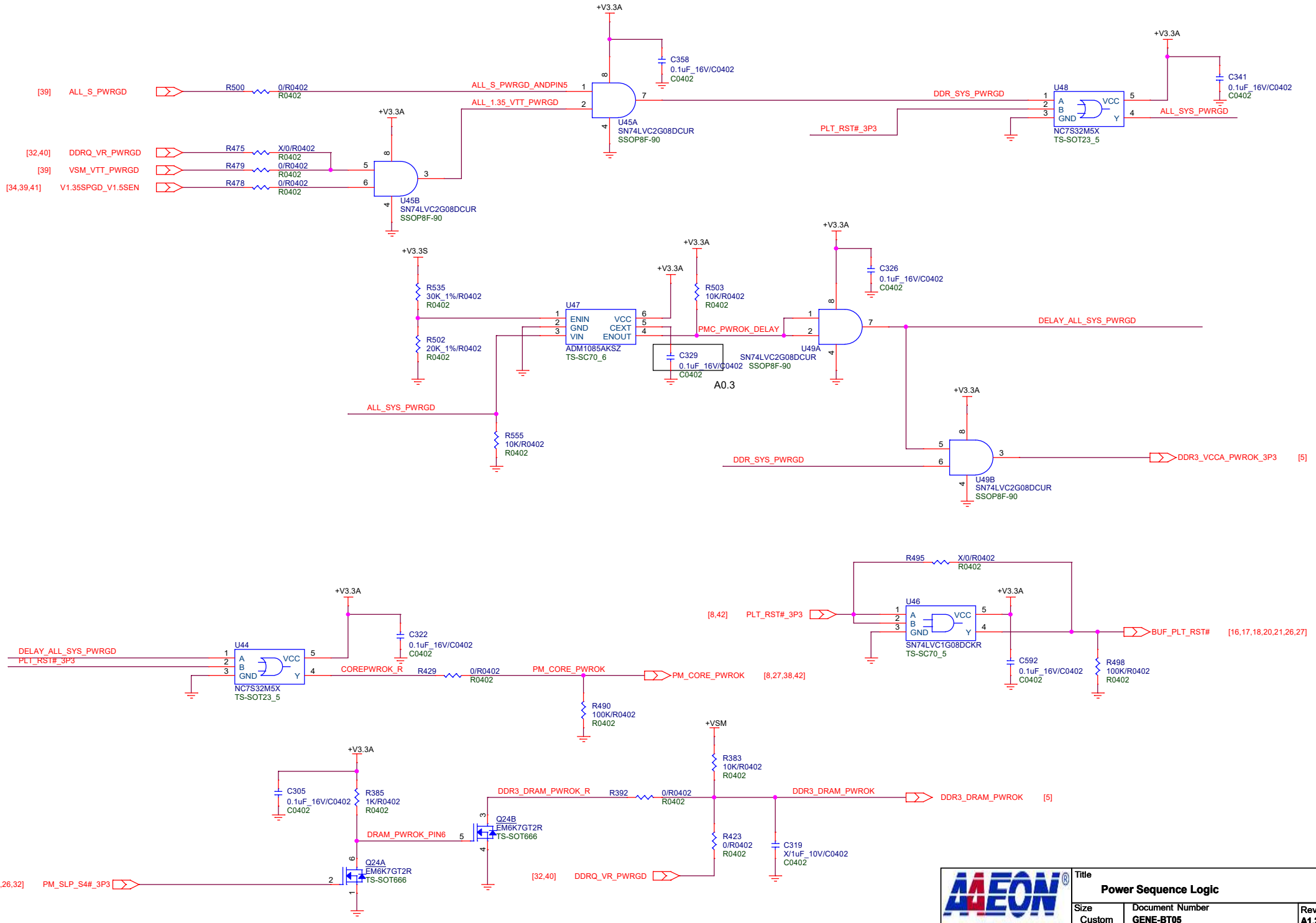
43



AAEON an ASUS assoc. co.

Title: **Power Sequence Logic**		
Size: Custom	Document Number: **GENE-BT05**	Rev: **A1.2_0_0**
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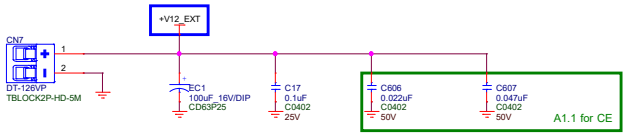
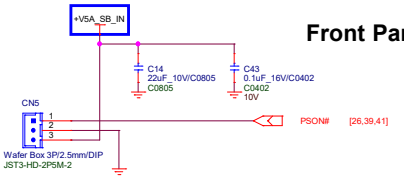
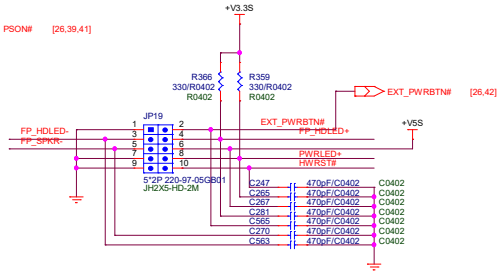
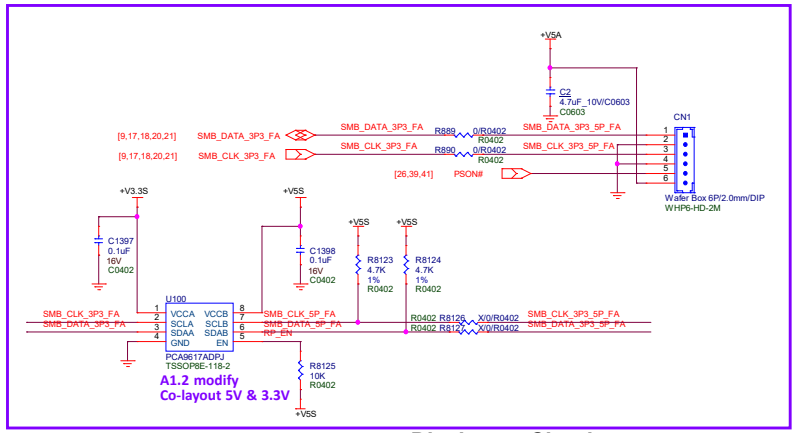
Power Input



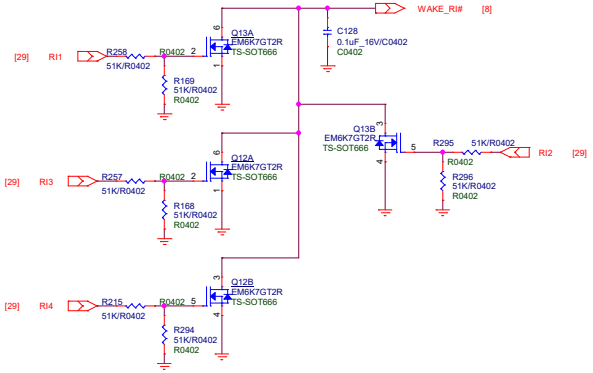
Front Panel



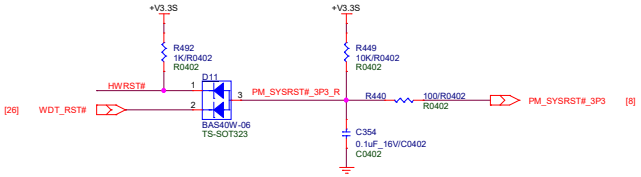




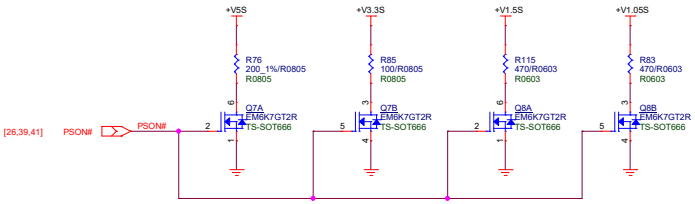
Wake On Modem



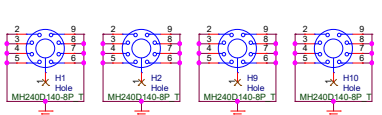
Reset Circuit



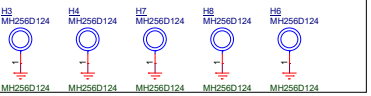
Discharge Circuit



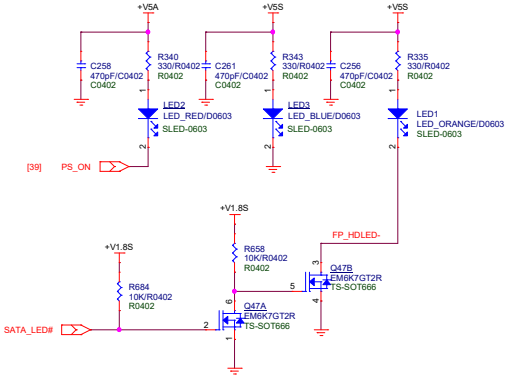
Mounting Holes

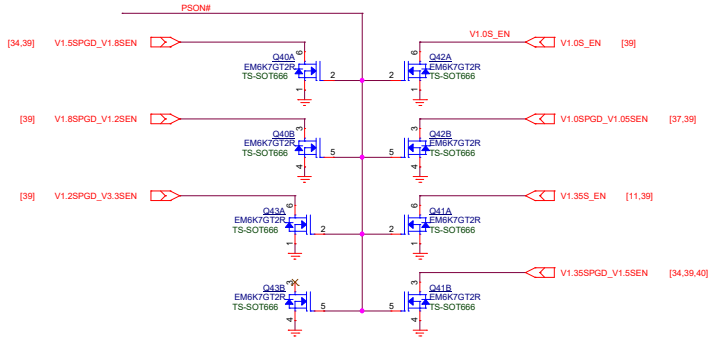


Heat Sink

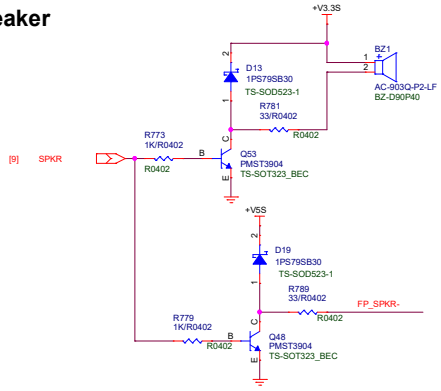


LED





Speaker



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Title: Power Input,Misc		
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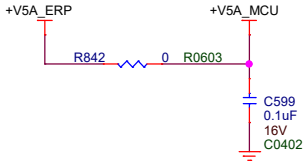
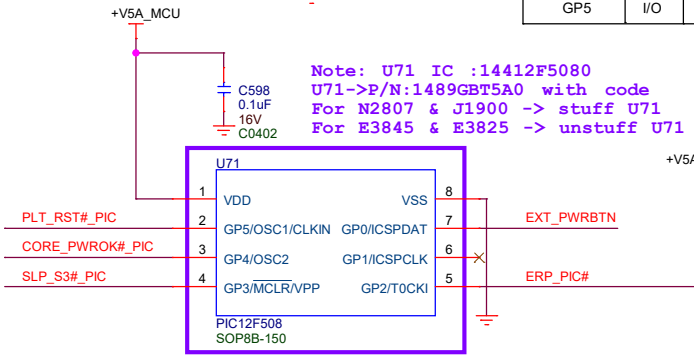
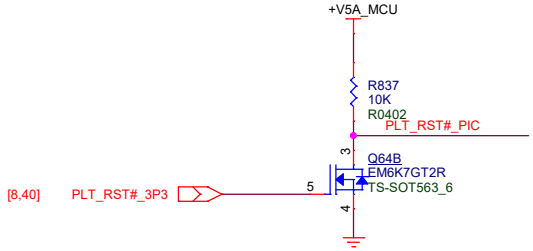
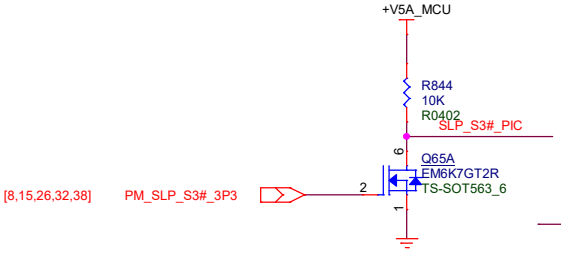
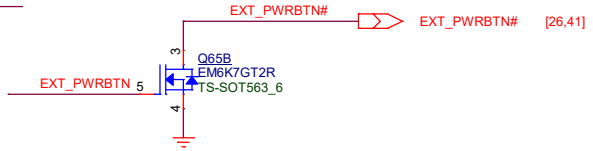
MCU Name	Type	Setting	Signal Name
GP0	I/O	Output	EXT_PWRBTN
GP1	I/O	-	-
GP2	I/O	Output	ERP_PIC#
GP3	I	input	SLP_S3#_PIC
GP4	I/O	Input	CORE_PWROK#_PIC
GP5	I/O	Input	PLT_RST#_PIC

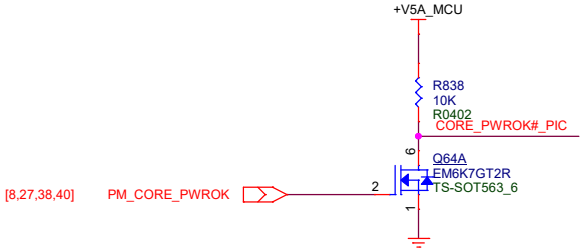


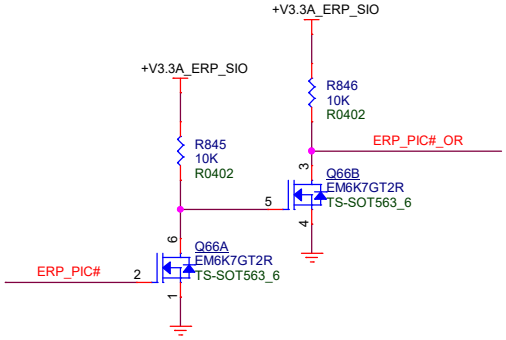


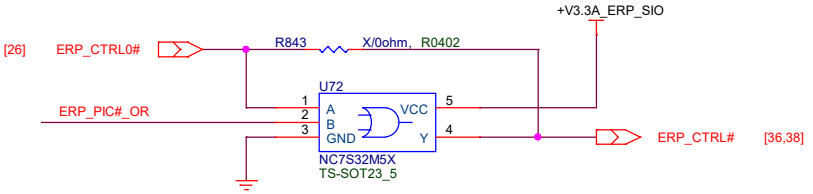












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HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2013/05/17	A0.1	First Release		Lena	Benson
2	2013/06/10	A0.1	Remove DVI circuit.	P15	Lena	Benson
3	2013/06/19	A0.1	1.Remove eDP circuit. 2.Remove eDP page (P17)	P16 P17	Lena	Benson
			DDI1_VDDEN/DDI1_BKLTEN/DDI1_BKLTCTL DDI1_TXP_2/DDI1_TXN_2/DDI1_TXP_3/DDI1_TXN_3 Unconnected.	P6		
			Remove eDP_LVDS_SEL GPIO	P30		
4	2013/09/30	A0.2	1.R407 change to 100K from 130K for OCP adjust. 2.R411 change to 33K from 44.2K for OCP adjust. 3.Q5 G2 add a cap. C378 (4700pf) 4. Remove V5S_EN discharge.	P32 P36 P36 P41	Lena	Benson
5	2014/03/25	A0.3	1.C329 change to 0.1uF from 0.022uF. 2.Add PIC circuit for intel Bay trail M/D PLTRST# issue(#4600919). 3.Remove USB Device. 4.Remove R20,R21,C34,U4 5.Add R847.R848	P40 P42 P9, P24 P41 P14	Lena	Chienkow
6	2014/06/09	A1.0	1.SIO.GPIO21 connect to V3.3S_PWRGD. 2.Change power source of PIC12F508.	P26 P42	Lena	Chienkow
7	2018/03/	A1.1	1.Change RT9715AGBR to RT9742CGJ5. 2.Add co-layout for U40.19,U40.24 and changed Q46 to BSS138. 3.L1:121110156M=>121110156P, L5:121110226V=>121110226X. 4.Reserve C600~C603 and R853 for Product Certification. 5.Reserve C604,C605 and R854 for Product Certification. 6.Reserve C606,C607 for Product Certification. 7.Reserve C608~C611 for Product Certification. 8.Add C612 for soft-start of Q28. 9.Add C613 for power optimization.	P23 P27 P32,P34 P16 P13 P41 P20 P38 P36	Lena	Edwin
8	2020/03/15	A1.2	1. Change CN17 & CN18 from 1655905038 to 1655X00013 2. Change U26 & U32 from 1430053250 to 1430053251 3. Change U30 from 14S2200900 to 14307S0190 4. Change U18 from 14S4186600 to 1440818660 5. Modified LVDS Circuits, add BKLTCTL and C614 6. Change U23,U24 from 1440002130 to 14S4021301 7. Change C553 & C585 from 1000pF to 0.047uF and C266 from 0.1uF to 1uF, Touch_LED to 3.3V 8. Change U15,U19 from 14S4814380 to 144X000041 and Modified F75111RG's control signals 9. Co-layout ALC892 & ALC897 circuits. 10. Add level shift 5V for SMBUS [co-layout] 11. Change CN26&CN27 from 165251420B to 1652814205 12. Change L2 from 121110156Z to 1211X00035 13. ChangeY3 from 12330024A1 to 12330024A4 14. Change D12 from 1301053040 to 1301013040 15. Change Q10,Q11,Q14 from 1315720010 to 1315642DT0 16. Change Q6 from 1315762010 to 1315EMB090 17. Change CN35 from 1654903901 to 1654903902 18. Delete Q28, Change Q29 to 1315000530 19. Reserved V5S_ENABLE contorl signal 20, Change R793 & R363 from 2.2K to 1.8K and Modified the RED,GREEN,Blue Signals. 21. Stuff R486 and unstuff U52 22. DIO's pull-high resistors ->1K 23. Jumper from black 165330010E to yellow 165330010G 24. remove Q33 25. add U101 for I2C level shift circuits at CN21 26. Stuff C257 22uF & R448->1K 27. Unstuff R798		Ricky	Edwin

AAEON an ASUS assoc. co.

Title: **Revision History**

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