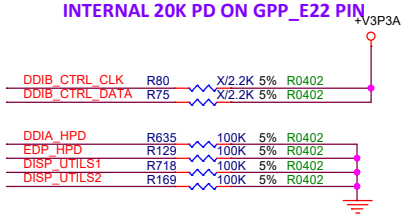
SoC DDI

Design note:
INTERNAL 20K PD ON GPP_E22 PIN



TCP Port Signal Mapping For DisplayPort*

Description	Signal Mapping	
	TCP	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3

Note: Apply to TCP ports only.

DDIA to LVDS

TCP2 GPIO

DDIB to eDP

TCP0 to DP++

TCP1 to HDMI2.1

TCP2 to Type-C

U26A — BMAP_REV = ?

[21] DDIA_LANE1_DP	W3	DDIA_TXP_3
[21] DDIA_LANE1_DN	AA3	DDIA_TXN_3
[21] DDIA_LANE0_DP	AA1	DDIA_TXP_2
[21] DDIA_LANE0_DN	AB1	DDIA_TXN_2
	AB3	DDIA_TXP_1
	AD3	DDIA_TXN_1
	AF1	DDIA_TXP_0
	AD1	DDIA_TXN_0
[21] DDIA_AUX_DP	AF3	DDIA_AUXP
[21] DDIA_AUX_DN	AG3	DDIA_AUXN
[25] DDIA_CTRL_CLK	ER23	GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
[25] DDIA_CTRL_DATA	ET23	GPP_E23/DDPA_CTRLDATA
[21] DDIA_HPD	EV25	GPP_E14/DDSP_HPDA/DISP_MISC_A
[22] DDIB_LANE3_DP	AP6	DDIB_TXP_3
[22] DDIB_LANE3_DN	AP8	DDIB_TXN_3
[22] DDIB_LANE2_DP	AM6	DDIB_TXP_2
[22] DDIB_LANE2_DN	AM8	DDIB_TXN_2
[22] DDIB_LANE1_DP	AK6	DDIB_TXP_1
[22] DDIB_LANE1_DN	AK8	DDIB_TXN_1
[22] DDIB_LANE0_DP	AH6	DDIB_TXP_0
[22] DDIB_LANE0_DN	AH8	DDIB_TXN_0
[22] DDIB_AUX_DP	AE6	DDIB_AUXP
[22] DDIB_AUX_DN	AE8	DDIB_AUXN
DDIB_CTRL_CLK	EK46	GPP_H15/DDPB_CTRLCLK/PCIE_LINK_DOWN
DDIB_CTRL_DATA	EL46	GPP_H17/DDPB_CTRLDATA
[22] EDP_HPD	EB47	GPP_A18/DDSP_HPDB/DISP_MISCB
EDP_BKLT_EN	DV54	GPP_A21/DDPC_CTRLCLK
EDP_BKLTCTL	DV52	GPP_A22/DDPC_CTRLDATA
DDP1_CTRLCLK	ER26	GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD/BSSB_LS0_RX
DDP1_CTRLDATA	ET26	GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD/BSSB_LS0_TX
	EL26	GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD/BSSB_LS1_RX
GPPC_E21	EN26	GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD/BSSB_LS1_TX
	FC37	GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/BSSB_LS2_RX/GSPI2_CS0#
GPPC_D10	EV37	GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/BSSB_LS2_TX/GSPI2_CLK
	EY37	GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/BSSB_LS3_RX/GSPI2_MISO
GPPC_D12	FA37	GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/BSSB_LS3_TX/GSPI2_MOSI
[22] EDP_VDD_EN	DY54	GPP_A17/DISP_MISCC
EDP_VDD_EN	EB49	GPP_A19/DDSP_HPD1/DISP_MISC1
[23] DP_HPD1	EB51	GPP_A20/DDSP_HPD2/DISP_MISC2
[24] HDMI_HPD2		
[25] DDSP_HPD3	DY47	GPP_A14/USB_OC1#/DDSP_HPD3/DISP_MISC3
[25] DDSP_HPD4	DY49	GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4
[21] EDP1_VDD_EN	ET21	VDDEN
[21] EDP1_BKLT_EN	EN21	EDP_BKLTEN
[21] LVDS_BKLTCTL	EL21	EDP_BKLTCTL

TCP0_TXRX_P1	BE8	TCP0_TX3_DP [23]
TCP0_TXRX_N1	BE6	TCP0_TX3_DN [23]
TCP0_TXRX_P0	BG8	TCP0_TX1_DP [23]
TCP0_TXRX_N0	BG6	TCP0_TX1_DN [23]
TCP0_TX_P1	AY3	TCP0_TX2_DP [23]
TCP0_TX_N1	BB3	TCP0_TX2_DN [23]
TCP0_TX_P0	BD3	TCP0_TX0_DP [23]
TCP0_TX_N0	BE3	TCP0_TX0_DN [23]
TCP0_AUX_P	BB1	TCP0_AUX_DP [23]
TCP0_AUX	BD1	TCP0_AUX_DN [23]
TCP1_TXRX_P1	AV8	TCP1_TX3_DP [24]
TCP1_TXRX_N1	AV6	TCP1_TX3_DN [24]
TCP1_TXRX_P0	AY8	TCP1_TX1_DP [24]
TCP1_TXRX_N0	AY6	TCP1_TX1_DN [24]
TCP1_TX_P1	AP3	TCP1_TX2_DP [24]
TCP1_TX_N1	AR3	TCP1_TX2_DN [24]
TCP1_TX_P0	AU3	TCP1_TX0_DP [24]
TCP1_TX_N0	AW3	TCP1_TX0_DN [24]
TCP1_AUX_P	AR1	TCP1_AUX_DP [24]
TCP1_AUX	AU1	TCP1_AUX_DN [24]
TCP2_TXRX_P1	BN8	TCP2_TXRX1_DP [26]
TCP2_TXRX_N1	BN6	TCP2_TXRX1_DN [26]
TCP2_TXRX_P0	BL8	TCP2_TXRX0_DP [26]
TCP2_TXRX_N0	BL6	TCP2_TXRX0_DN [26]
TCP2_TX_P1	BK3	TCP2_TX1_DP [26]
TCP2_TX_N1	BM3	TCP2_TX1_DN [26]
TCP2_TX_P0	BG3	TCP2_TX0_DP [26]
TCP2_TX_N0	BH3	TCP2_TX0_DN [26]
TCP2_AUX_P	BH1	TCP2_AUX_DP [25]
TCP2_AUX	BK1	TCP2_AUX_DN [25]
TCP3_TXRX_P1	BW8	
TCP3_TXRX_N1	BW6	
TCP3_TXRX_P0	BU8	
TCP3_TXRX_N0	BU6	
TCP3_TX_P1	BU3	
TCP3_TX_N1	BV3	
TCP3_TX_P0	BN3	
TCP3_TX_N0	BR3	
TCP3_AUX_P	BR1	
TCP3_AUX	BU1	
VSS_589	AL3	
TCP_RCOMP	AM1	TCRCOMP R712 2.2K 1% R0402
DISP_UTILS_2	AF32	DISP_UTILS2
DDIA_RCOMP	AJ1	DDIA_RCOMP R710 150 1% R0402
DDIB_RCOMP	AL1	DDIB_RCOMP R711 150 1% R0402
DISP_UTILS_1	DJ1	DISP_UTILS1

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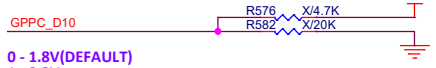
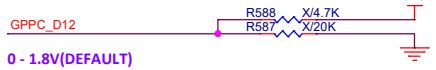
STRAP: TBT LSX #2 PINS VCCIO CONFIGURATION



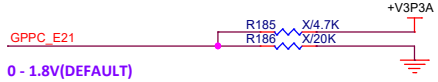
0 - 1.8V(DEFAULT)
1 - 3.3V
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

STRAP: TBT LSX #3 PINS VCCIO CONFIGURATION



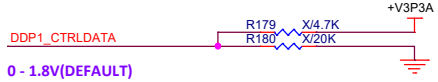
0 - 1.8V(DEFAULT)
1 - 3.3V
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

STRAP: TBT LSX #1 PINS VCCIO CONFIGURATION

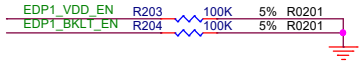


0 - 1.8V(DEFAULT)
1 - 3.3V
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

STRAP: TBT LSX #0 PINS VCCIO CONFIGURATION



0 - 1.8V(DEFAULT)
1 - 3.3V
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB



Function	Port	DDI Signal Name	eDP* Signal Name
BKLT Enable		EDP_BKLTEN - DDIA DDPC_CTRLCL - DDIB	eDPA_BKLT_EN eDPB_BKLT_EN
BKLT Control		EDP_BKLTCTL - DDIA DDPC_CTRLDATA - DDIB	eDPA_BRIGHTNESS eDPB_BRIGHTNESS
HPD		DDSP_HPDA - DDIA DDSP_HPDB - DDIB	eDPA_HPD eDPB_HPD
VDD Enable		EDP_VDDEN - DDIA DISP_MISC_C - DDIB	eDPA_VDDEN eDPB_VDDEN

<Variant Name>

AAEON Technology INC.

Title: SoC DDI

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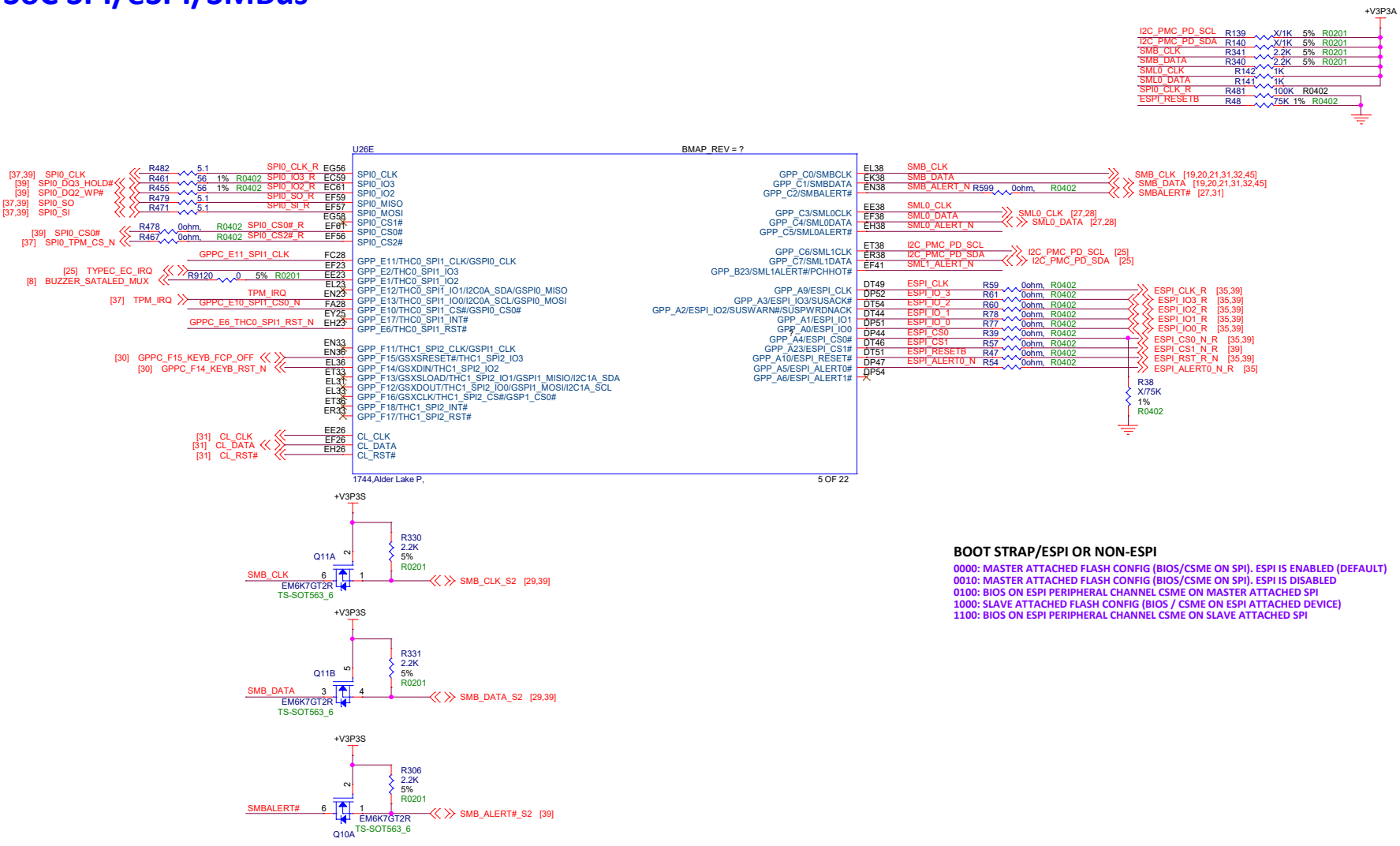
SoC SPI/eSPI/SMBus



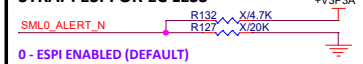
BOOT STRAP/ESPI OR NON-ESPI

0000: MASTER ATTACHED FLASH CONFIG (BIOS/CSME ON SPI). ESPI IS ENABLED (DEFAULT)
0010: MASTER ATTACHED FLASH CONFIG (BIOS/CSME ON SPI). ESPI IS DISABLED
0100: BIOS ON ESPI PERIPHERAL CHANNEL CSME ON MASTER ATTACHED SPI
1000: SLAVE ATTACHED FLASH CONFIG (BIOS / CSME ON ESPI ATTACHED DEVICE)
1100: BIOS ON ESPI PERIPHERAL CHANNEL CSME ON SLAVE ATTACHED SPI

STRAP: TLS CONFIDENTIALITY

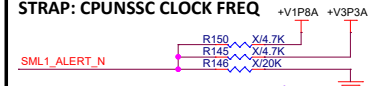
0 - TLS CONFIDENTIALITY ENABLE (DEFAULT)
1 - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

STRAP: ESPI OR EC LESS



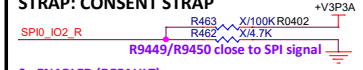
0 - ESPI ENABLED (DEFAULT)
1 - ESPI IS DISABLED
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

STRAP: CPUNSSC CLOCK FREQ



0 - 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1 - 19.2MHZ FROM DIVIDER
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

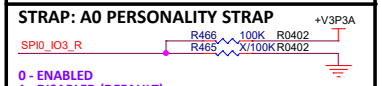
STRAP: CONSENT STRAP



R9449/R9450 close to SPI signal

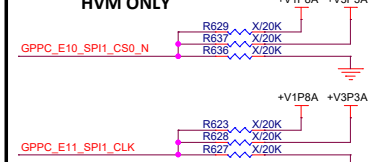
0 - ENABLED (DEFAULT)
1 - DISABLED
NO Internal PU/PD
SAMPLING - RSMRSTB
STUFF Rup WHEN VALIDATING 100MHZ FLASH

STRAP: A0 PERSONALITY STRAP



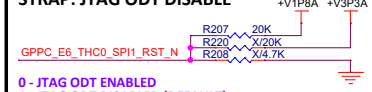
0 - ENABLED
1 - DISABLED (DEFAULT)
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

STRAP: XTAL INPUT FREQUENCY [1:0] HVM ONLY



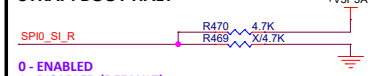
00 - 24MHZ(DEFAULT)
01 - 38.4MHZ
10 - 250MHZ
11 - 100MHZ
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

STRAP: JTAG ODT DISABLE



0 - JTAG ODT ENABLED
1 - JTAG ODT DISABLED (DEFAULT)
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

STRAP: BOOT HALT



0 - ENABLED
1 - DISABLED (DEFAULT)
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

<Variant Name>

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AAEON Technology INC.

Title: SoC SPI/eSPI/SMBus

Size	Document Number	Rev
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SoC HDA/I2C

+V3P3S

I2C1_SDA R128 2.2K 5% R0201
I2C1_SCL R136 2.2K 5% R0201
I2C0_SDA R125 1K 1% R0402
I2C0_SCL R120 1K 1% R0402
UART0_TXD R86 49.9K 1% R0402

+V3P3A

LAN2_DISABLE# R53 10K 1% R0201

STRAP: FLASH DESCRIPTOR SECURITY OVERRIDE

+V3P3A

HDA_SDO_R R533 X/2.2K 5% R0201
R534 X/10K

0 - SECURITY MEASURES NOT OVERRIDEN(DEFAULT)
1 - OVERRIDEN
WEAK INTERNAL PD 20K
SAMPLING - PCH_PWROK

?
?

U26G BMAP_REV = ?

EY34 GPP_D19/I2S_MCLK1_OUT
[31] M.2_BT_PCMCLK EV53 GPP_S0/SNDW0_CLK/I2S1_SCLK
[31] M.2_BT_PCMFRM EY53 GPP_S1/SNDW0_DATA/I2S1_SFRM
[31] M.2_BT_PCMOUT FA50 GPP_S2/SNDW1_CLK/DMIC_CKL_A0/I2S1_TXD
[31] M.2_BT_PCMIN FC50 GPP_S3/SNDW1_DATA/DMIC_DATA0/I2S1_RXD
EV50 GPP_S4/SNDW2_CLK/DMIC_CLK_B0
EY50 GPP_S5/SNDW2_DATA/DMIC_CLK_B1
EW48 GPP_S6/SNDW3_CLK/DMIC_CLK_A1
EY48 GPP_S7/SNDW3_DATA/DMIC_DATA1

GPP_R0/HDA_BCLK/I2S0_SCLK/DMIC_CLK_B0/HDAPROC_BCLK ER56 HDA_BCLK_R R527 33 HDA_BIT_CLK [38]
GPP_R1/HDA_SYNC/I2S0_SFRM/DMIC_CLK_B1 EP60 HDA_SYNC_R R521 33 HDA_SYNC [38]
GPP_R2/HDA_SDO/I2S0_TXD/HDAPROC_SDO ER57 HDA_SDO_R R528 33 HDA_SDOUT [38]
GPP_R3/HDA_SDI0/I2S0_RXD/HDAPROC_SDI ER59 HDA_SDIN0_R HDA_SDIN0_R [38]
GPP_R4/HDA_RST#/I2S2_SCLK/DMIC_CLK_A0 ER53 HDA_RST#_R R105 33 HDA_RST# [38]
GPP_R5/HDA_SDI1/I2S2_SFRM/DMIC_DATA0 ET53
GPP_R6/I2S2_TXD/DMIC_CLK_A1 EB44
GPP_R7/I2S2_RXD/DMIC_DATA1 EB46
DV51
GPP_A11 DV47 GPP_A13_PMC_I2C_SCL GPP_A13_PMC_I2C_SCL [31]
GPP_A13
SNDW_RCOMP_1 FA53 R559 200
SNDW_RCOMP_2 FC53 1% R0402

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?

U26F BMAP_REV = ?

TP35 TP20 UART0_TXD EN48 GPP_H11/UART0_TXD/M2_SKT2_CFG1
EN46 GPP_H10/UART0_RXD/M2_SKT2_CFG0
EL41 GPP_H13/I2C7_SCL/UART0_CTS#/M2_SKT2_CFG3/ISH_GP7B/DEVSLP1B
[29,30] SATA_DEVSLP0 EK41 GPP_H12/I2C7_SDA/UART0_RTS#/M2_SKT2_CFG2/ISH_GP6B/DEVSLP0B
EW30 GPP_D18/UART1_TXD/ISH_UART1_TXD
EV34 GPP_D17/UART1_RXD/ISH_UART1_RXD
[39] I2C0_SCL I2C0_SCL EH46 GPP_H5/I2C0_SCL
[39] I2C0_SDA I2C0_SDA EF46 GPP_H4/I2C0_SDA
[25] I2C1_SCL I2C1_SCL EH43 GPP_H7/I2C1_SCL
[25] I2C1_SDA I2C1_SDA EF43 GPP_H6/I2C1_SDA
TP112 TP20 I2C2_SCL DT57 GPP_B6/ISH_I2C0_SCL/I2C2_SCL
TP114 TP20 I2C2_SDA DT56 GPP_B5/ISH_I2C0_SDA/I2C2_SDA
[24] I2C3_SCL I2C3_SCL DR56 GPP_B8/ISH_I2C1_SCL/I2C3_SCL
[24] I2C3_SDA I2C3_SDA DR58 GPP_B7/ISH_I2C1_SDA/I2C3_SDA
[30,31] CNV_MFUART2_TXD EN43 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
[30,31] CNV_MFUART2_RXD EL43 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD
[28] LAN2_DISABLE# LAN2_DISABLE# DN60 GPP_B17/I2C5_SCL/ISH_I2C2_SCL
TP123 TP20 GPP_B16 DN57 GPP_B16/I2C5_SDA/ISH_I2C2_SDA

GPP_D14/ISH_UART0_TXD/I2C4B_SCL EY28 KEYE_WAKE_N [31]
GPP_D13/ISH_UART0_RXD/I2C4B_SDA EV28 KEYB_WAKE_N [30]
GPP_D16/ISH_UART0_CTS#/I2C7B_SCL EY36 KEYB_DISABLE [30]
GPP_D15/ISH_UART0_RTS#/I2C7B_SDA EW36
GPP_D3/ISH_GP3/BK3/SBK3 FA34
GPP_D2/ISH_GP2/BK2/SBK2 EY30 GPP_D2_LAN_WAKE_N [28]
GPP_D1/ISH_GP1/BK1/SBK1 EY31
GPP_D0/ISH_GP0/BK0/SBK0 EV31
GPPC_RCOMP DR61 R519 200
1% R0402

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16.2.6 SCI / SMI# and NMI

SCI capability is available on all GPIOs, while SMI and NMI capability is available on only select GPIOs.

Below are the PCH GPIOs that can be routed to generate SMI or NMI:

- GPP_B14 and GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0] ; GPP_E[16:13]
- GPP_F12

<Variant Name>

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Title: SoC HDA/I2C

Size: Custom | Document Number: GENE-ALP6/EGENEALP6A01A0.1_0_0 | Rev:

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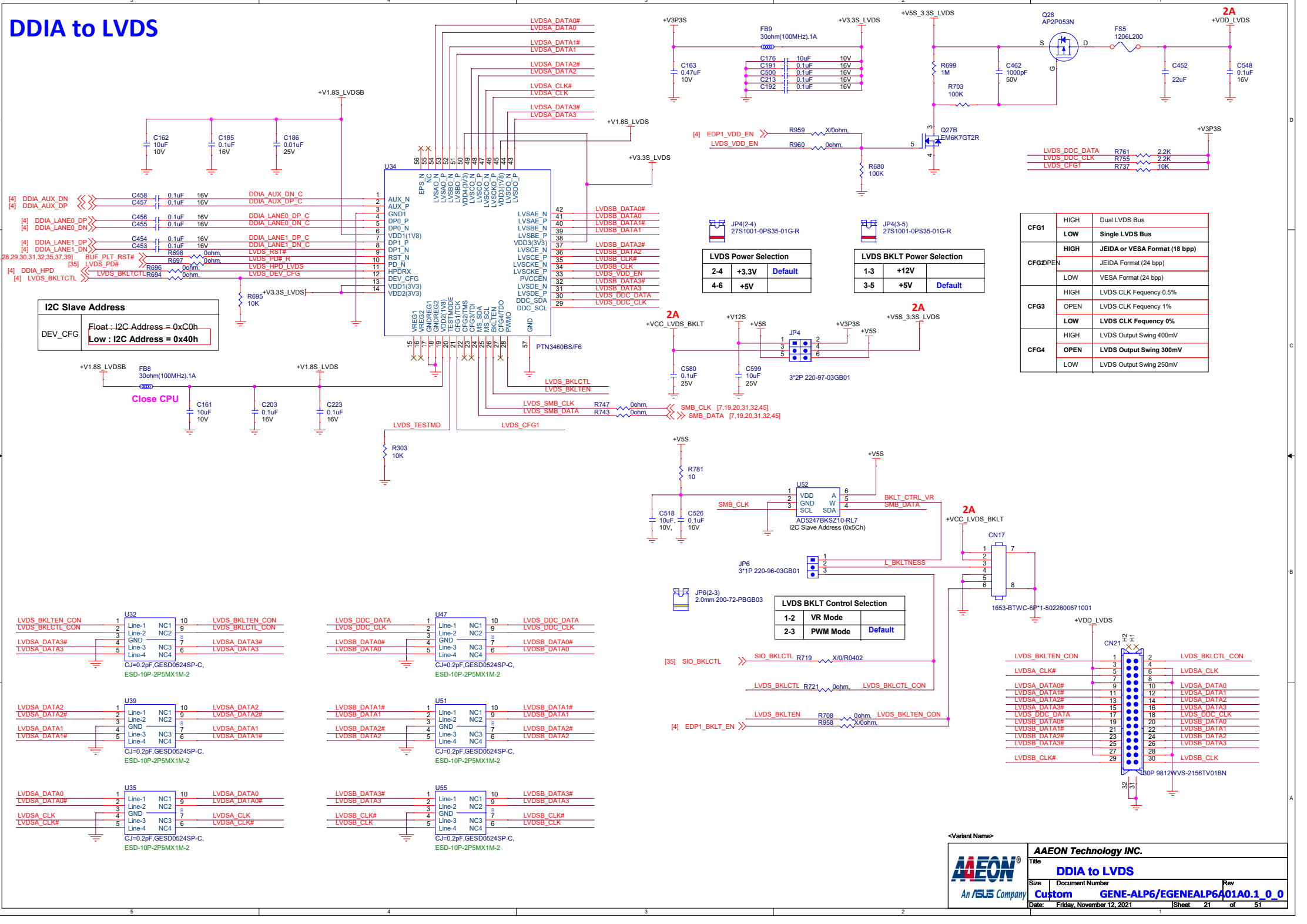
DDIA to LVDS



<Variant Name>

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Title			
DDIA to LVDS			
Size	Document Number		Rev
Custom	GENE-ALP6/EGENEALP6A01A0.1_0_0		
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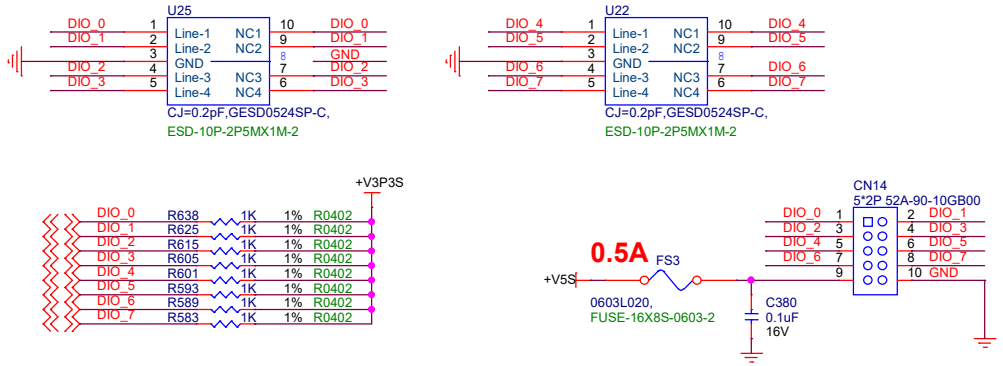
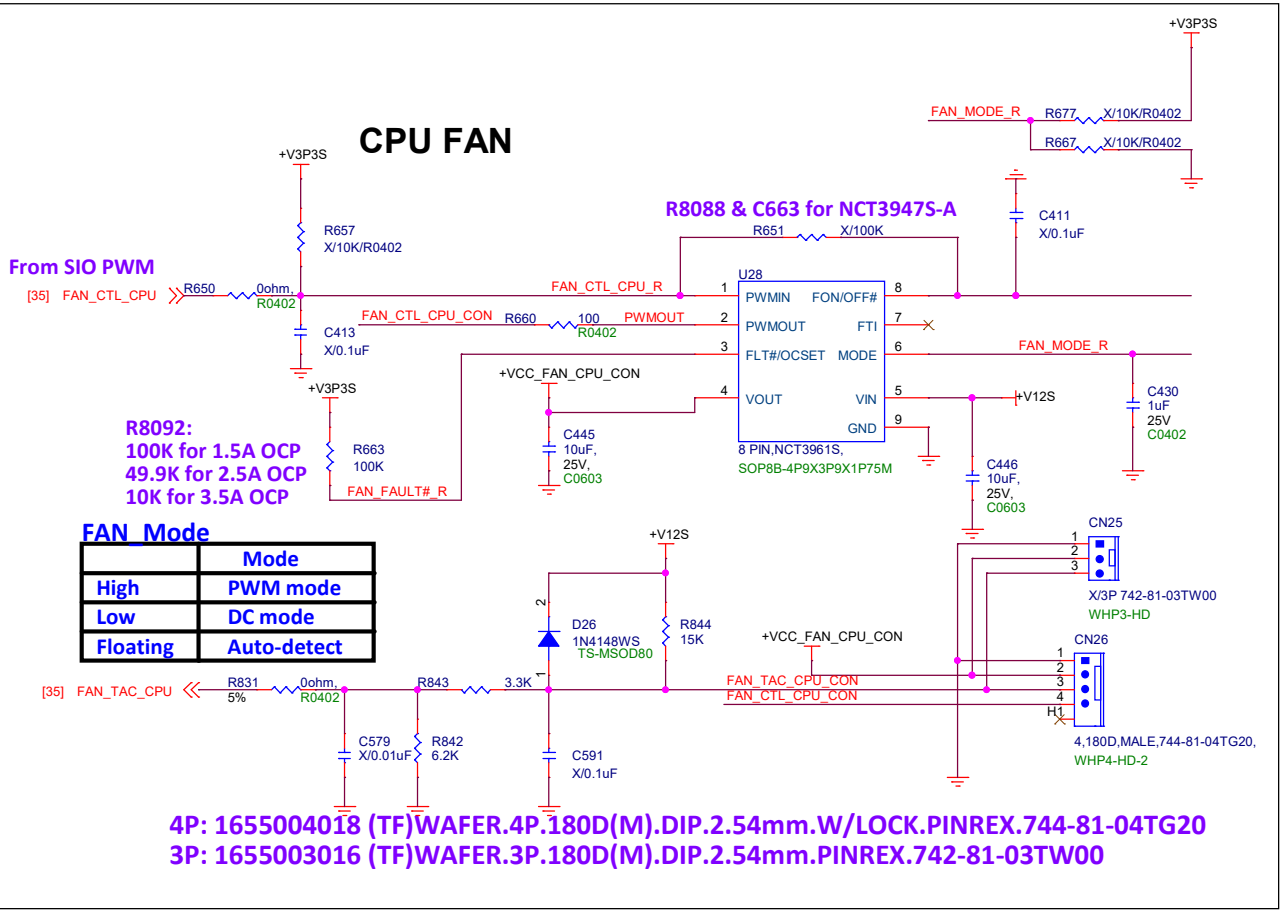
DIO

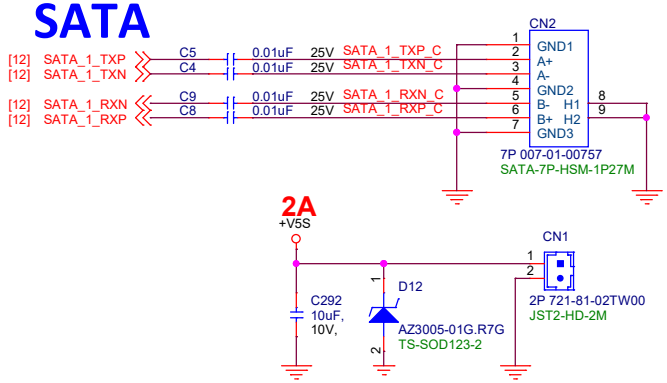


CPU FAN



4P: 1655004018 (TF)WAFER.4P.180D(M).DIP.2.54mm.W/LOCK.PINREX.744-81-04TG20
3P: 1655003016 (TF)WAFER.3P.180D(M).DIP.2.54mm.PINREX.742-81-03TW00

SATA



<Variant Name>

AAEON Technology INC.	
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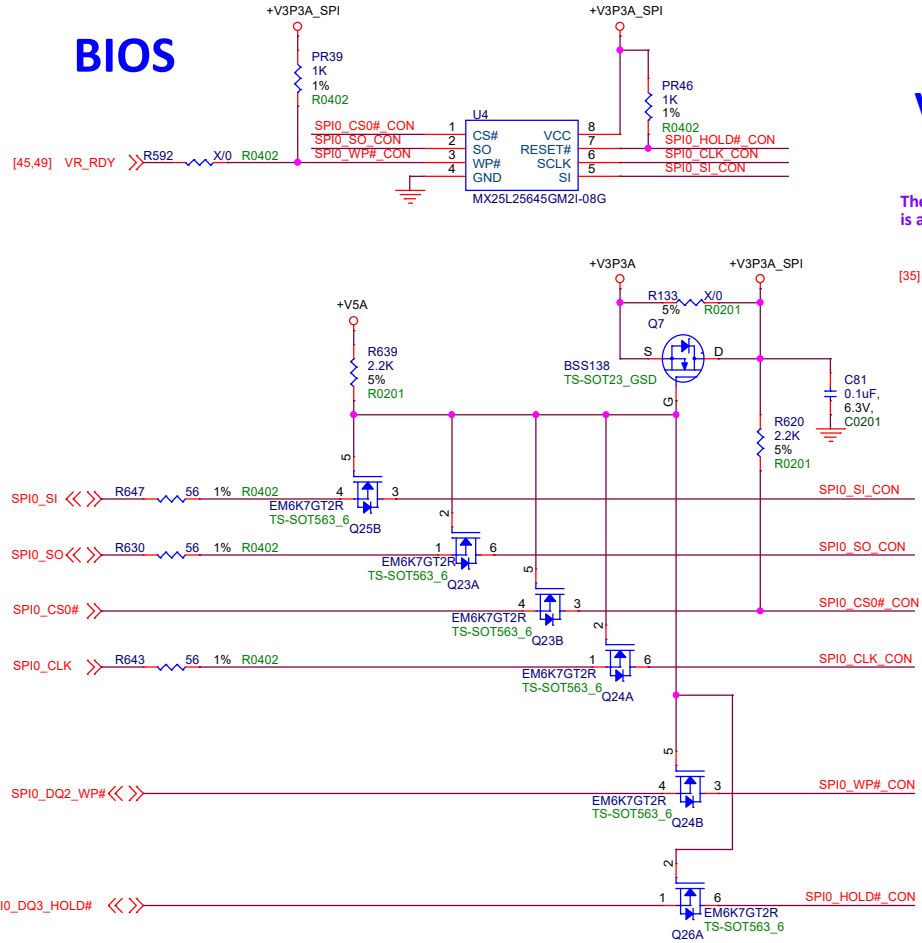
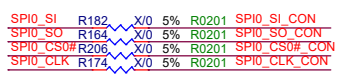
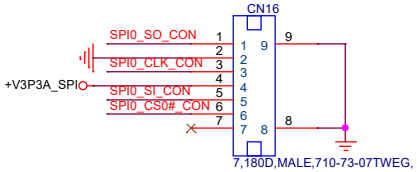
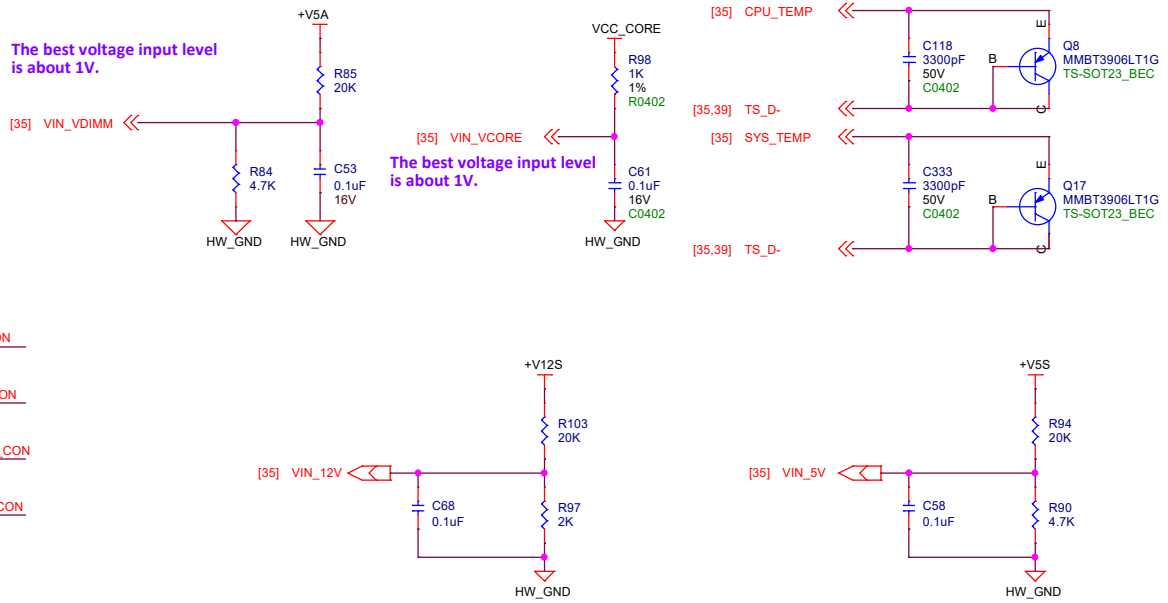
BIOS



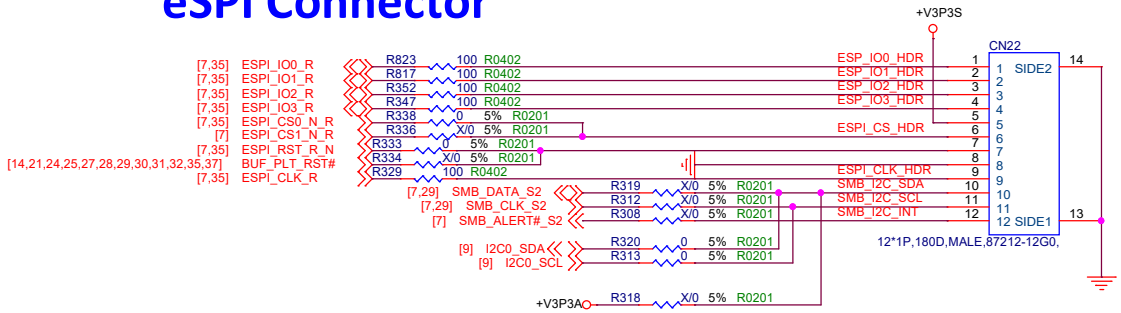




Voltage Monitor(Vcore, Vmem) Temperature Monitor(CPU, SYS)



eSPI Connector



<Variant Name>

AAEON Technology INC.

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Power Input

+9V~+36V

+VIN_EXT

1161627100 (TF)PS-CON.270uF.16V.20%.8*11.5mm.DIP.Pinlength=3.5mm.NIPPON CHEMI-CON.PSC16VB270MH11
1182610190 (TF)OS-CON.100uF.25V.20%.8*11.5mm.DIP.ESR=0.025.Matsuki.MP25RS100MD11
1183610191 (TF)OS-CON.100uF.35V.20%.(8*8mm).DIP.25mohm.3000mA.FPCAP.FP-035RE101M-L8CG

CN4
2PIN_90D,DT-126VP-S2016002P,

Co-layout with CN3

+VIN_EXT

CN3
X/2P*2 1121-700-04S
PWR-ATX-2X2P-H

D2
AZ4036-01G.R7G
TS-SOD123-2

+V5A_SB_IN

C32
10uF

CN8
3P 753-71-03TW01

PSON# [35,40,50]

Front Panel

+V3P3S

R44
243

R448
330

EXT_PWRBTN# [35]

CN9
5*2P 50238-01041-001

FP_HDLED-
FP_BUZZER-
EXT_PWRBTN#
FP_HDLED+
PWRLED+
HWRST#

+V5S

C331 470pF 50V
C325 470pF 50V
C330 470pF 50V
C329 470pF 50V
C328 470pF
C321 470pF
C324 470pF

Wake On Modem

PCIE_WAKE# [14,27,29,30,31]

[36] RI1
R659 51K
Q26B EM6K7GT2R
R653 51K
C311 0.1uF 16V

[36] RI2
R434 51K
Q16A EM6K7GT2R
R432 51K

[36] RI3
R430 51K
Q15A EM6K7GT2R
R426 51K

[36] RI4
R435 51K
Q16B EM6K7GT2R
R431 51K

Reset Circuit

+V3P3A

R480
1K

HWRST#

D15
BAS40W-06

[35] WDT_RST#

PM_SYSRST#_3P3_R

R499 100

PM_SYSRST# [14]

C343
X/0.1uF

Discharge Circuit

+V3P3S +V5S +V12S

R421
20
1%
R0603

R415
330
1%
R0603

R407
1.5K
1%
R0603

[35,40,50] PSON#

R425
5%
0ohm
R0402

PS_ON#_R

Q15B EM6K7GT2R

Q14A EM6K7GT2R

Q14B EM6K7GT2R
TS-SOT563_6

Mounting Holes

H2 Hole
MH240D140-6P-Petals

H7 Hole
MH240D140-6P-Petals

H1 Hole
MH240D140-6P-Petals

H6 Hole
MH240D140-6P-Petals

H3
MH256D126
MH256D126

H5
MH256D126
MH256D126

H4
MH256D126
MH256D126

M3
material
PCB

M4
material
SMT

M7
material
(TF)BIOS Label.AMI.AMI-AptioTM DT(C)2006

LED

+V5A +V5S +V5S

C288
470pF

R389
330

LED5
1.6*0.8*0.4mm Red

C636
470pF

R934
330

LED1
1.6*0.8*0.4mm Blue

C635
470pF

R933
330

LED2
90D,19-217-S2C-FM2P1VY-3T,

+V3P3S

R41
10K

FP_HDLED-

Q2B EM6K7GT2R

Q3A EM6K7GT2R

[6,29,30] PCH_SATA_LED_N

Speaker

+V5S

D7
1PS79SB30
TS-SOD523

R10
33

FP_BUZZER-

[8] BUZZER

R29
X/1K

Q1
PMST3904

R980
1K

[35] BEEP

<Variant Name>

AAEON Technology INC.

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