NCT6791D

Nuvoton LPC I/O

(For ASUS Only)

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1. GENERAL DESCRIPTION

The NCT6791D is a member of Nuvoton's Super I/O product line. The NCT6791D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6791D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6791D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6791D provides two high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6791D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6791D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6791D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6791D supports the Intel® PECI (Platform Environment Control Interface) and AMD® SB-TSI interface. The NCT6791D supports AMD® CPU power on sequence, and it also supports Intel® Deep Sleep Well glue logic to help customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6791D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. It also supports two-color LED control to indicate system power states. The NCT6791D supports Consumer IR function for remote control purpose. It also supports Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6791D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Specification 1.1
Support AMD power on sequence
Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Single 24-MHz or 48-MHz clock input
Support selective pins of 5 V tolerance

UART

Two high-speed, 16550-compatible UART with 16-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

Compatible with IBM® parallel port
Support PS/2-compatible bi-directional parallel port
Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
Enhanced printer port back-drive current protection

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset
12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system

Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode

Support Current Mode (dual current source) temperature sensing method

Fourteen voltage inputs (CPUVCORE, VCOREREFIN, VIN0~7, 3VCC, AVCC, 3VSB and VBAT)

Five fan-speed monitoring inputs

Five fan-speed controls

Dual mode for fan control (PWM and DC) for SYSFANOUT

Built-in case-open and CPU socket occupied detection circuit

Programmable hysteresis and setting points for all monitored items

Issue SMI#, OVT# (Over-temperature) to activate system protection

Nuvoton Health Manager support

Provide I^2C master / slave interface to read / write registers

CIR and IR (Infrared)

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR, including CIRTX, CIRRX, CIRRXWB

General Purpose I/O Ports

GPIO0 ~ GPIO8 programmable general purpose I/O ports

Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions

Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys

Mouse Wake-Up by programmable buttons

OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification

Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement
Fading LED driver control for power status and diagnostic indications

Intel Deep Sleep Well (DSW) Glue Logic

Support Deep Sleep Well (DSW) Glue Logic

AMD® CPU Power on Sequence

Support AMD® CPU power on sequence

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

- 3.3 voltage

Package

128-pin LQFP
Green

3. BLOCK DIAGRAM

Figure 3-1 NCT6791D Block Diagram

4. PIN LAYOUT

Figure 4-1 NCT6791D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 24.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{tsp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5} - 5V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tcup5} - 5V TTL-level, input buffer with controllable pull-up
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
15	IOCLK	I	IN_{tp5}	VCC	System clock input, either 24MHz or 48MHz. The actual frequency must be specified by 24M_48M_SEL strapping.
65	PME#	O	OD_{12}	VSB	Generated PME event.
17	PCICLK	I	IN_{tp5}	VCC	PCI-clock 33-MHz input.
18	LDRQ#	O	O_{12}	VCC	Encoded DMA Request signal.
19	SERIRQ	I/O	IN_{tp3} O_{12} OD_{12}	VCC	Serialized IRQ input / output.
20-23	LAD[3:0]	I/O	IN_{tp3} OD_{12}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
25	LFRAME#	I	IN_{tp3}	VCC	Indicates the start of a new cycle or the termination of a broken cycle.
26	LRESET#	I	IN_{tsp3}	VCC	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 Multi-Mode Parallel Port

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
38	SLCT	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
39	PE	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
40	BUSY	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
41	ACK#	I	IN_{tsp5}	VSB	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
53	ERR#	I	IN_{tsp5}	VSB	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
51	SLIN#	O	O_{12}	VSB	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
52	INIT#	O	O_{12}	VSB	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
54	AFD#	O	O_{12}	VSB	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
55	STB#	O	O_{12}	VSB	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
50	PD0	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
49	PD1	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
48	PD2	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
47	PD3	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
45	PD4	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
44	PD5	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
43	PD6	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
42	PD7	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.3 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
35	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
34	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
33	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
32	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
31	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
30	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
29	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
14	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
13	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
12	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
11	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
10	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
9	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
8	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

5.4 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
27	GA20M	O	O_{12} OD_{12}	VCC	Gate A20 output. This pin is high after system reset. (KBC P21)
28	KBRST#	O	O_{12} OD_{12}	VCC	Keyboard reset. This pin is high after system reset. (KBC P20)
58	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock. Pull up is recommended if useless.
59	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data. Pull up is recommended if useless.
56	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock. Pull up is recommended if useless.
57	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data. Pull up is recommended if useless.

5.5 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
95	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length
6	CIRTX0	O	O_{12}	VCC	CIR transmission output
96	CIRTX1	O	O_{12}	VSB	CIR transmission output
38	CIRRXWB0	I	IN_{tsp5}	VSB	CIR input for wide band.
98	CIRRXWB1	I	IN_{tsp5}	VSB	CIR input for wide band.

5.6 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
102	SKTOCC#	I	IN_{tsp5}	VRTC	CPU socket occupied detection
100	CASEOPEN0#	I	IN_{tsp5}	VRTC	CASE OPEN 0 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
72	CASEOPEN1#	I	IN_{tsp5}	VRTC	CASE OPEN 1 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
103	VCOREREFIN	I	AIN	VSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
116	VIN7	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
115	VIN6	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
114	VIN5	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
111	VIN4	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
107	VIN3	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
106	VIN2	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
105	VIN1	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
104	VIN0	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
109	CPUVCORE	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
110	VREF	O	AOUT	AVCC	Reference Voltage (around 2.048 V).
116	AUXTIN3	I	AIN	AVCC	The input of temperature sensor 6.
115	AUXTIN2	I	AIN	AVCC	The input of temperature sensor 5. It is used for AUX2 temperature sensing.
114	AUXTIN1	I	AIN	AVCC	The input of temperature sensor 4. It is used for AUX1 temperature sensing.
111	AUXTIN0	I	AIN	AVCC	The input of temperature sensor 3. It is used for AUX0 temperature sensing.
112	CPUTIN	I	AIN	AVCC	The input of temperature sensor 2. It is used for CPU temperature sensing.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
113	SYSTIN	I	AIN	AVCC	The input of temperature sensor 1. It is used for system temperature sensing.
128	OVT#	O	OD_{12}	VCC	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#	O	OD_{12}	VCC	System Management Interrupt channel output.
83	OVT#	O	OD_{12}	VCC	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#	O	OD_{12}	VCC	System Management Interrupt channel output.
3	AUXFANIN0	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
4	AUXFANIN1	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
5	AUXFANIN2	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
5	AUXFANIN3	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
121	AUXFANOUT0	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
122	AUXFANOUT1	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
123	AUXFANOUT2	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
90	AUXFANOUT3	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
124	CPUFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
125	CPUFANOUT	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
126	SYSFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
127	SYSFANOUT	O	O_{12} OD_{12} AOUT	VCC	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.
51	BEEP	O	OD_{12}	VSB	Beep function for hardware monitor.

5.7 Intel® PECI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
120	PECI	I/O	I/O_{V3}	Vtt	INTEL® CPU PECI interface. Connect to CPU.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
119	Vtt	I	Power	Vtt	INTEL® CPU Vtt Power.

5.8 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
61	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
60	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
101	RSMRST#	O	OD_8	VRTC	Resume reset signal output.
73	DPWROK#	O	OD_8	VRTC	V3A signal output
64	SLP_S3#	I	IN_{tp5}	VSB	SLP_S3# input.
84	SLP_S5#	I	IN_{tp5}	VSB	SLP_S5# input.
80	ATXPGD	I	IN_{tcup5}	VSB	ATX power good signal.
63	PSON#	O	OD_{12}	VSB	Power supply on-off output.
82	PWROK	O	O_8 OD_8	VRTC	3VCC PWROK signal.
81	PWROK	O	O_8 OD_8	VRTC	3VCC PWROK signal.
70	PWROK	O	OD_8	VRTC	3VCC PWROK signal.
89	PWROK	O	OD_{12}	VSB	3VCC PWROK signal.
88	PWROK#	O	OD_{12}	VSB	3VCC PWROK# signal.
81	AMD_PWROK	O	OD_8	VRTC	3VCC AMD PWROK signal.
83	RESETCONI#	I	IN_{tp5}	VSB	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
37	RESETCONO#	O	OD_{12}	VSB	RESETCONO# output.
70	3VSBSW	O	OD_{12}	VRTC	Switch 3VSB power to memory when in S3 state.
71	3VSBSW#	O	OD_{24}	VSB	Switch 3VSB power to memory when in S3 state.
89	3VSBSW#	O	OD_{12}	VSB	Switch 3VSB power to memory when in S3 state.
79	RSTOUT0#	O	OD_{24}	VSB	PCI Reset Buffer 0. (from pin26)
78	RSTOUT1#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 1. (from pin26) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit6.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
77	RSTOUT2#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 2. (from pin26) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit7.
91	RSTOUT4#	O	O_{12}	VSB	PCI Reset Buffer 4. (from pin26) This pin is push-pull output.
93	RSTOUT3#	O	O_{12}	VSB	PCI Reset Buffer 3. (from pin26) This pin is push-pull output.

5.9 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
70	DEEP_S5_0	O	OD_{12}	VRTC	This pin is to control system power for entering “more power saving mode”.
72	DEEP_S5_1	O	OD_{8}	VRTC	This pin is to control system power for entering “more power saving mode”.

5.10 Port 80 Message Display & LED Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
42	DGH_0#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
41	DGL_0#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
54	DGH_1#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
53	DGL_1#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
50 49 48 47 45 44 43	LED_A LED_B LED_C LED_D LED_E LED_F LED_G	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
39	YLW_LED	O	OD_{12}	VSB	Yellow LED output control. This pin could indicate the power status.
40	GRN_LED	O	OD_{12}	VSB	Green LED output control. This pin could indicate the power status.

5.11 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
75	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
76	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
52	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
51	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
75	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
76	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
52	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
51	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.

5.12 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46, 85	3VSB	I			+3.3 V stand-by power supply for the digital circuits.
99	VBAT	I			+3 V on-board battery for the digital circuits.
1,24	VCC	I			+3.3 V power supply for driving 3 V on host interface.
108	AVCC	I			Analog +3.3 V power input. Internally supply power to all analog circuits.
117	CPUD- / AGND	I			Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
16, 94	VSS	I			Ground.
119	VTT	I			INTEL® CPU Vtt power.

5.13 AMD Power-On Sequence

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
109	CPUVCORE	I	AIN	AVCC	Power sequence group B signal
106	VLDT	I	AIN	AVCC	Power sequence group C signal
107	VDIMM	I	AIN	AVCC	Memory power enable
87	VCORE_EN	O	OD_{12}	VSB	CPU Vcore power enable
86	VLDT_EN	O	OD_{12}	VSB	Hyper transport I/O power enable
81	AMD_PWROK	O	OD_{12}	VSB	AMD power on sequence ok signal
63	AMD_PSON#	O	OD_{12}	VSB	Power supply on/off output to enable ATX

5.14 AMD SB-TSI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
118	TSIC	O	OD_{12}	VCC	AMD SB-TSI clock output.
120	TSID	I/O	IN_{tsp3} OD_{12}	VCC	AMD SB-TSI data input / output.

5.15 Dual Voltage Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
74	BKFD_CUT	O	OD_{12}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S3 sleep state.
71	LATCH_BKFD_CUT#	O	O_{24}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.
70	LATCH_BKFD_CUT	O	O_{12}	VRTC	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

5.16 DSW

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
89	SLP_SUS#	I	IN_{tp5}	VSB	This pin connects to SLP_SUS# in CPT PCH
90	SUS_WARN_5VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits
91	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
92	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
93	SUSWARN#	I	IN_{tp5}	VSB	This pin connects to SUSWARN# in CPT PCH
88	SLP_SUS_FET	O	OD_{12}	VSB	This pin connects to VSB power switch
97	PCHVSB	I	AIN	VSB	PCHVSB function

5.17 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
11	IRRX0	I	IN_{tp5}	VSB	IR Receiver input.
12	IRTX0	O	O_{12}	VSB	IR Transmitter output.
95	IRRX1	I	IN_{tsp5}	VSB	IR Receiver input.
96	IRTX1	O	O_{12}	VSB	IR Transmitter output.

5.18 General Purpose I/O Port

5.18.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
121	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 0.
122	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 1.
123	GP02	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 2.
2	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 3.
3	GP04	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 4.
4	GP05	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 5.
5	GP06	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 6.
6	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 7.

5.18.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
13	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
12	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.
11	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
10	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
9	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.
8	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
7	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.18.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
59	GP20	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 0.
58	GP21	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 1.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
57	GP22	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 2.
56	GP23	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 3.
95	GP24	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 4.
96	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 5.
118	GP26	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 6.
98	GP27	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 7.

5.18.4 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
83	GP30	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 0.
76	GP31	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 1.
75	GP32	I/O	IN_{tsp5} O_{12} OD_{12}	VRTC	General-purpose I/O port 3 bit 2.
71	GP33	I/O	IN_{tp5} O_{24} OD_{24}	VRTC	General-purpose I/O port 3 bit 3.
55	GP34	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 4.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
54	GP35	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 5.
53	GP36	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 6.

5.18.5 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	GP40	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 0.
52	GP41	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 1.
51	GP42	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 2.
41	GP43	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 4 bit 3.
40	GP44	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 4.
39	GP45	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 5.
38	GP46	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 6.
37	GP47	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 7.

5.18.6 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
93	GP50	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 0.
92	GP51	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 1.
91	GP52	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 2.
90	GP53	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 3.
89	GP54	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 4.
88	GP55	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 5.
87	GP56	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 6.
86	GP57	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 7.

5.18.7 GPIO-6 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
50	GP60	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 0.
49	GP61	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 1.
48	GP62	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 2.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
47	GP63	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 3.
45	GP64	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 4.
44	GP65	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 5.
43	GP66	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 6.
42	GP67	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 6 bit 7.

5.18.8 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
69	GP70	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 0.
68	GP71	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 1.
67	GP72	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 2.
66	GP73	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 3.
79	GP74	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 7 bit 4.
78	GP75	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 7 bit 5.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
77	GP76	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 7 bit 6.

5.18.9 GPIO-8 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
29	GP80	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 0.
30	GP81	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 1.
31	GP82	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 2.
32	GP83	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 3.
33	GP84	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 4.
34	GP85	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 5.
35	GP86	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 6.
36	GP87	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 7.

5.19 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	2E_4E_SEL	I	IN_{tdp5}	VSB	SIO I/O address selection. (Strapped by LRESET#) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
32	24M_48M_SEL	I	IN_{tdp5}	VSB	Input clock rate selection (Strapped by **VCC**: internal Power OK signal without any delay.) Strapped to high: The clock input on pin 15 is 48MHz. Strapped to low: The clock input on pin 15 is 24MHz.
34	PO80_EN	I	IN_{tdp5}	VSB	Port80 / GPIO function selection. (Strapped by LRESET#) Strapped to high: Port80 function. Strapped to low: non-PRT function
9	UARTP80_EN	I	IN_{tdp5}	VSB	Pin34 function selection. (Strapped by LRESET#) See configuration register
10	UARTCP80_EN	I	IN_{tdp5}	VSB	Pin55 function selection. (Strapped by LRESET#) See configuration register
12	TEST1_MODE_EN	I	IN_{tp5}	VSB	Test1 mode function selection. (Strapped by **VSB** power: internal RSMRST# signal]) Recommand pull-down
62	EN_AS	I	IN_{tdp5}	VSB	Enable ASUS specific function. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high: Enable ASUS function Strapped to low: Disable ASUS function
68	TEST_MODE0_EN	I	IN_{tp5}	VSB	Test0 mode function selection. (Strapped by **VSB** power: internal RSMRST# signal]) Recommand pull-down
69	DSW_EN	I	IN_{tp5}	VSB	DSW position selection. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high: DSW function Strapped to low: GPIO function

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
96	AMDPWR_EN	I	IN_{tdp5}	VSB	Enable AMD power sequence function. (Strapped by **VSB** power: internal RSMRST# signal.) Strapped to high: Enable AMD power sequence Strapped to low: Disable AMD power sequence

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.20 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	31	3VSB	Pull-down	47.4K	1
24M_48M_SEL	32	3VSB	Pull-down	47.4K	1
PO80_EN	34	3VSB	Pull-down	47.4K	1
UARTP80_EN	9	3VSB	Pull-down	47.4K	1
UARTCP80_EN	10	3VSB	Pull-down	47.4K	1
TEST1_MODE_EN	12	3VSB	Pull-down	47.4K	1
TEST_MODE0_EN	68	3VSB	Pull-down	47.4K	1
EN_AS	62	3VSB	Pull-down	47.4K	2
AMDPWR_EN	96	3VSB	Pull-down	47.4K	2
Advanced Configuration & Power Interface					
PSIN#	61	3VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

5.21 Strapping multi function pin control

PO80_EN	**Pin38** function selection (See CR27) **Pin39 ~ 40** function selection (See CR1B) **Pin41 ~ 50** function selection (See CR27)

<table>
<tr><td></td><td>

Pin51 function selection (See CR1B)
Pin52 function selection (See CR1A)
Pin53 function selection

PO80_EN	Pin53
0	GP36
1	DGL_1#

Pin54 function selection

PO80_EN	Pin54
0	GP35
1	DGH_1#

</td></tr>
<tr><td>UARTP80_EN</td><td>**Pin34** function selection (See CR2A)</td></tr>
<tr><td>UARTCP80_EN</td><td>

Pin55 function selection

UARTCP80_EN	Pin55
0	GP34
1	SOUTC_P80

</td></tr>
<tr><td>EN_AS</td><td>

Pin66 function selection

EN_AS	Pin66
0	GP73
1	BCLKIN1

Pin67 function selection

EN_AS	Pin67
0	GP72
1	BCLKIN0

Pin68 function selection

EN_AS	Pin68
0	GP71
1	BCLKOUT1

Pin69 function selection

EN_AS	Pin69
0	GP70
1	BCLKOUT0

</td></tr>
<tr><td>DSW_EN</td><td>

Pin90 function selection

DSW_EN	Pin90
0	GP53
1	SUSWARN_5VDUAL

Pin92 function selection

DSW_EN	Pin92
0	GP51
1	5VDUAL

</td></tr>
</table>

<table>
<tr><td>AMDPWR_EN</td><td>

Pin63 function Selection

AMDPWR_EN	Pin63
0	PSON#
1	AMD_PSON#

Pin81 function Selection

AMDPWR_EN	Pin81
0	PWROK
1	AMD_PWROK

Pin86 function Selection

AMDPWR_EN	Pin86
0	GP57
1	VLDT_EN

Pin87 function Selection

AMDPWR_EN	Pin87
0	GP56
1	VCORE_EN

</td></tr>
</table>

6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	84	SLP_S5# input.
RESETCONI#	83	RESETCON# input signal. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
RESETCONO#	37	RESETCON# output signal.
PWROK	82	This pin generates the PWROK signals while 3VCC is present.
DPWROK	73	This pin generates the DPWROK signals while 3VSB is present.
ATXPGD	80	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.
RSMRST#	101	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT6791D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Figure 6-1 RSMRST# and DPWROK#

Figure 6-2 PWROK

Figure 6-3 RESETCONI# and PWROK

Figure 6-4 RSTOUTX# and LRESET#

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tp	Valid 3VSB to DPWROK# inactive	100	150	mS

TIMING	PARAMETER	MIN	MAX	UNIT
tg	3VSB Glitch allowance		1	uS
td	Falling 3VSB supply Delay		5	uS
t2	Valid 3VCC to PWROK active	300	500	mS
t3	RESETCONI# de-bounce	15	20	mS
t4	RESETCONO# and PWROK active	See LDB CRFA		
t5	RESETCONO# active to PWROK active	1	2	uS
t6	RESETCONO# inactive to RESETCONI# detect	3	4	S
t7	LRESET# active to RSTOUTx# active	0	80	nS
t8	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	-	3.033	Volt
V2	3VSB Ineffective Voltage	2.882	-	Volt
V3	3VCC Valid Voltage	-	2.83	Volt
V4	3VCC Ineffective Voltage	2.68	-	Volt
Vg	3VSB drops by Power noise	2	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

6.2 GPIOE#

NCT6791D supports GPIOE# functions, please refer the timing diagram below:

Figure 6-5 GPIOE#

6.3 BKFD_CUT & LATCH_BKFD_CUT

NCT6791D supports BKFD_CUT & LATCH_BKFD_CUT functions, please refer the timing diagram below:

Figure 6-6 BKFD_CUT and LATCH_BKFD_CUT

BKFD_CUT (Backfeed_Cut) – When high, switches dual rails to standby power.

LATCH_BKFD_CUT (Latched_Backfeed_Cut) – When high, switches dual rails to standby power.

6.4 3VSBSW#

Figure 6-7 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t9	SLP_S3# active to 3VSBSW# active	0	10	mS
t10	3VCC active to 3VSBSW# inactive	120	190	mS
t11	SLP_S3# inactive to PSON# active	0	80	nS
t12	SLP_S3# active to PSON# inactive	15	45	mS
t13	SLP_S3# minimal Low Time	40	-	mS

6.5 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

Figure 6-8 PSON# Block Diagram

6.6 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

Figure 6-9 PWROK Block Diagram

6.7 Front Panel LEDs

NCT6791D supports two LED control pins – GRN_LED and YLW_LED.

For dual-color LED application:

(1)GRN_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the green LED and the anode of the yellow LED.

(2)YLW_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the yellow LED and the anode of the green LED.

Figure 6-10 Illustration of Dual Color LED application

GRN_LED and YLW_LED pins are designed to show currently power states. There are Manual Mode and Automatic Mode:

6.7.1 Automatic Mode

Power state is S0 or S1: GRN_LED will be asserted by default.

Power state is S3: YLW_LED will be asserted by default.

Power state is S4 or S5: Both GRN_LED and YLW_LED will be de-asserted by default.

AUTO_EN	GRN_LED_RST (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
1	X	S0,S1	1	1	GRN_BLK_FREQ	HIGH-Z
1	X	S3	0	1	HIGH-Z	YLW_BLK_FREQ
1	X	S4,S5	X	0	HIGH-Z	HIGH-Z

6.7.2 Manual Mode

AUTO_EN	GRN_LED_RST# (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
0	0	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	0	S3	0	1	HIGH-Z	HIGH-Z
0	0	S4,S5	X	0	HIGH-Z	HIGH-Z
0	1	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S3	0	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S4,S5	X	0	GRN_BLK_FREQ	YLW_BLK_FREQ

Register Neme	Register Location
AUTO_EN	Logic Device B, CRF7h, bit7
GRN_BLK_FREQ	Logic Device B, CRF7h, bit3~0
YLW_BLK_FREQ	Logic Device B, CRF8h, bit3~0
GRN_LED_RST#	Logic Device B, CRF7h, bit6
YLW_LED_RST#	Logic Device B, CRF8h, bit6

6.7.3 S0~S5 LED Blink Block Diagram

6.7.4 LED Pole (LED_POL)

Set to 0b, GRN_LED output is active low, as the following Figure(a)

Set to 1b, GRN_LED output is active high, as the following Figure(b)

Figure 6-11 Illustration of LED polarity

6.7.5 Deeper Sleeping State Detect Function

These two LED pins could also be used to indicate if the system is in Deeper Sleeping State. For more detail, please refer to the section of Advanced Sleep State Control Function.

Enable_DEEP_S5	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S5	DeepS5_GRN_BLK_FREQ	DeepS5_YLW_BLK_FREQ
1	1	DEEP_S5	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior

Enable_DEEP_S3	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S3	DeepS3_GRN_BLK_FREQ	DeepS3_YLW_BLK_FREQ
1	1	DEEP_S3	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior

S0 ~ S5
Block
HIGH-Z
0.0625Hz
0.125Hz
0.25Hz
0.5Hz
1Hz
2Hz
0
Fading LED
0000
0001
0010
0011
0100
0101
0110
0111
1xxx
User define for Deep S5#
Q
LED_FREQ
[3:0]
(For Deep S5#)
HIGH-Z
0.0625Hz
0.125Hz
0.25Hz
0.5Hz
1Hz
2Hz
0
Fading LED
0000
0001
0010
0011
0100
0101
0110
0111
1xxx
User define for Deep S3#
Q
LED_FREQ
[3:0]
(For Deep S3#)
00
01
10
11
{Deep S5#, Deep S3#}
LED_POL
LED

6.8 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device 16 CRE0h ~ CRE3h.

Figure 6-12 ASSC Application Diagram

6.8.1 When ASSC is disabled

When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

6.8.2 When ASSC is enabled (Enter into Deeper Sleeping State)

When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS3 or DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the "Deeper Sleeping State (DSS)" where system's VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

6.8.3 When ASSC is enabled (Exit Deeper Sleeping State)

When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time

(wakeup delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

6.8.4 SLP_S5#_LATCH Control Function

SLP_S5#_LATCH control signal is similar to SLPS5# signal. When System is at S0 ~ S5 state, SLP_S5#_LATCH follows the SLPS5# signal. When system is at DeepS5 State, SLP_S5#_LATCH will keep low state till system returns to S0 state. When system is at DeepS3 State, SLP_S5#_LATCH will keep high till system returns to S0 state. Please see the following timing diagram:

6.9 Intel DSW Function

6.9.1 Enter DSW State timing diagram

6.9.2 Exit DSW State timing diagram

6.9.3 Application Circuit

The NCT6776 can not only provide SIO Deep S5/S3 function, but Intel DSW function. The application circuit should follow the guide below:

6.10 AMD Power-On Sequence

The NCT6791D supports new AMD power on sequence bace on ACPI power on sequence，therefore，user can choose which architecture by set the strapping pin98。If pin98 is 0, only ACPI power on sequence is set，otherwise, AMD power on sequence is combined with ACPI, user can set CR2F[5] to get the same condition. To make sure CR2B[4]:GP34_SEL and CR2B[0]:GP30_SEL are “0” before running the sequence, because they are ATXPGD and SLP_S5# pin select.

When S0->S3 or S0->S5, we support two kinds of power off sequence. One is non_level detect: it means VCORE_EN will pull low as long as about 10~15ms after VLDT_EN pull low and PSON will pull high as long as about 10~15ms after VCORE_EN pull low. Two, level detect, means VCORE_EN will pull low depend on delay time and pre-power group VLDT_IN, and PSON will pull high depend on pre-power group (VDIMM_IN, ATXPGD), too. User can set CR27[1] to choose two condition and its default is “0” (level detect).

Timing Parameters

Parameter	Description	Min.	Typ.	Max.	Unit
T1	Period of VDIMM rises to 0.7V to VCORE_EN assertion	10		15	ms
T2	Period of CPUVCORE rises to 0.7V to VLDT_EN assertion	10		15	ms
T3	Period of VLDT_IN rises to 0.7V to AMD_PWROK assertion	10		15	ms
T4	Period of SLP_S3# deassertion to AMD_PWROK deassertion	10		50	ms
T5	Period of CPUPWRGD deassertion to VLDT_EN deassertion	10		15	ms
T6	Period of VLDT_EN deassertion to VCORE_EN deassertion	10		15	ms
T7	Period of VCORE_EN deassertion to PSON# deassertion	10		15	ms

VDDA: 2.5V (not controlled by SIO)
VDIMM: DDR 1.8V, DDR3 1.5V (not controlled by SIO)
VLDT: 1.2V
VCORE: 0.8V ~ 1.55V

To support AMD power on sequence，we add some Pinout as VLDT_EN ，VCORE_EN，VLDT，VDIMM。The sequence is follow the figure above。CPU and NB must conform to the SPEC or else the SIO will suspend at the sequence。

7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT6791D uses a special protocol to access configuration registers to set up different types of configurations. The NCT6791D has a total of 16 Logical Devices (from Logical Device 1 to Logical Device 16 with the exception of Logical Device 0, 4, C, 10, 11, 12, 13 & 15 for backward compatibility) corresponding to fourteen individual functions: Parallel Port (Logical Device 1), UART A (Logical Device 2), UART B & IR (Logical Device 3), Keyboard Controller (Logical Device 5), CIR (Logical Device 6), GPIO6, 7 & 8 (Logical Device 7), WDT1 & GPIO0 & 1 (Logical Device 8), GPIO1, 2, 3, 4, 5, 6, 7 & 8 (Logical Device 9), ACPI (Logical Device A), Hardware Monitor & Front Panel LED (Logical Device B), BCLK (Logical Device D), CIRWAKEUP (Logical Device E), GPIO (Logical Device F), PORT80 UART (Logical Device 14), and Deep Sleep (Logical Device 16).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT6791D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

Figure 7-1 Structure of the Configuration Register

Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	Reserved	
1	Parallel Port	100h ~ FF8h
2	UART A	100h ~ FF8h
3	UART B & IR	100h ~ FF8h
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	CIR	100h ~ FF8h
7	GPIO 6, 7 & 8	Reserved
8	WDT1 ,GPIO 0 & 1	Reserved
9	GPIO 1, 2, 3, 4, 5, 6, 7 & 8	Reserved
A	ACPI	Reserved
B	Hardware Monitor & Front Panel LED	100h ~ FFEh
C	Reserved	
D	BCLK	Reserved
E	CIRWAKEUP	100h ~ FF8h
F	GPIO	Reserved
10	Reserved	
11	Reserved	
12	Reserved	
13	Reserved	
14	PORT80 UART	Reserved
15	Reserved	
16	Deep Sleep	Reserved

7.1 Configuration Sequence

Figure 7-2 Configuration Register

To program the NCT6791D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV     DX, 2EH
MOV     AL, 87H
OUT     DX, AL
OUT     DX, AL
;-----------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-----------------------------------------------------------------------------
MOV     DX, 2EH
MOV     AL, 07H
OUT     DX, AL          ; point to Logical Device Number Reg.
MOV     DX, 2FH
MOV     AL, 01H
OUT     DX, AL          ; select Logical Device 1
;
MOV     DX, 2EH
MOV     AL, F0H
OUT     DX, AL          ; select CRF0
MOV     DX, 2FH
MOV     AL, 3CH
OUT     DX, AL          ; update CRF0 with value 3CH
;----------------------------------------------
; Exit the Extended Function Mode
;----------------------------------------------
MOV     DX, 2EH
MOV     AL, AAH
OUT     DX, AL
```

8. HARDWARE MONITOR

8.1 General Description

The NCT6791F monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT6791F can simultaneously monitor all of the following inputs:

- Nine analog voltage inputs (five internal voltages CPUVCORE, VBAT, 3VSB, 3VCC and AVCC; four external voltage inputs)
- Five fan tachometer inputs
- Three remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- Two case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT6791F can generate the following outputs:

- Three PWM (pulse width modulation) and one DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT6791F provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS.

The rest of this section introduces the various features of the NCT6791F hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT6791F provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The

standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

Figure 8-1 LPC Bus’ Reads from / Write to Internal Registers

8.4 I²C interface

The I²C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the NCT6791F hardware monitor and control fan speeds. The address of the I²C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

Figure 8-3 Serial Bus Read from Internal Address Register

8.5 Analog Inputs

The nine analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 4 general-purpose inputs connected to external device pins (VIN0 – VIN3) and five internal signals connected to the power supplies (CPUVCORE, AVCC, VBAT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

Figure 8-4 Analog Inputs and Application Circuit of the NCT6791F

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.5.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVCC, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.5.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.5.2.1. Voltage Reading

NCT6791F has 15 voltage reading:

	CPUVCORE	**VIN0**	**AVCC**	**3VCC**	**VIN1**
Voltage reading	Bank4, Index80	Bank4, Index84	Bank4, Index82	Bank4, Index83	Bank4, Index81
	VIN2	**VIN3**	**3VSB**	**VBAT**	**VTT**
Voltage reading	Bank4, Index8C	Bank4, Index8D	Bank4, Index87	Bank4, Index88	Bank4, Index89
	VIN4	**VIN5**	**VIN6**	**VIN7**	**VCOREREFIN**
Voltage reading	Bank4, Index86	Bank4, Index8A	Bank4, Index8B	Bank4, Index8E	Bank4, Index85

Note: Bank0 CRBD bit 7:6 are lowest bit1:0 for ADC. These two bits accrancy is not guarantee.

8.5.3 Temperature Data Format

The data format for sensors SYSTIN, CPUTIN, AUXTIN0, AUXTIN1, AUXTIN2 and AUXTIN3 is 9-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1Ceh
-55°C	1100,1001	C9h	1,1001,0010	192h

8.5.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF (pin 110). The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 0, index 59h, 5Dh, and 5Eh.

Figure 8-5 Monitoring Temperature from Thermistor

8.5.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND (pin 117), and the D+ pin is connected to the temperature sensor pin in the NCT6791F. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh, and 5Eh.

Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.5.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The NCT6791F can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- (pin 117) and the pin D+ is connected to temperature sensor pin in the NCT6791F. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

8.5.3.4. Temperature Reading

NCT6791F has 6 temperature reading can monitor different temperature sources (ex. SYSTIN, CPUTIN, AUXTIN, PECI…etc).

	SMIOVT1	SMIOVT2
Temperature source select	Bank6,index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default:CPUTIN
Temperature reading	Bank0, index27	Bank1, index50 & index51 bit7

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

8.6 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT6791F supports. The NCT6791F contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-8 PECI Temperature shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

Figure 8-8 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

The device also provides an offset register to 'shift' the negative PECI readings to positive values. The offset registers are called "Tbase", which are located at Bank7 Index 09h for Agent0 and Bank7 Index 0Ah for Agent1. All default values of these Tbase registers are 8'h00. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

The Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets, shows the temperature and fan-speed relationship after Tbase offset is applied (based on Figure 8-8 PECI Temperature). This view is from the perspective of the NCT6791F fan control circuit.

Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets

Assuming Tbase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT6791F, BIOS/software can include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the "100% fan duty-cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

8.7 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.7.1 Fan Speed Reading

The fan speed reading at:

	FAN COUNT READING		FAN RPM READING	
	13-bit		16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	Bank4, indexB0	Bank4, indexB1	Bank4, indexC0	Bank4, indexC1
CPUFANIN	Bank4, indexB2	Bank4, indexB3	Bank4, indexC2	Bank4, indexC3
AUXFANIN0	Bank4, indexB4	Bank4, indexB5	Bank4, indexC4	Bank4, indexC5
AUXFANIN1	Bank4, indexB6	Bank4, indexB7	Bank4, indexC6	Bank4, indexC7
AUXFANIN2	Bank4, indexB8	Bank4, indexB9	Bank4, indexC8	Bank4, indexC9

8.7.2 Fan Speed Calculation by Fan Count Reading

In 13-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.7.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.7.4 Fan Speed Control

The NCT6791F has five output pins for fan control, Only SYSFANOUT offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 index 04h, bits 0 for SYSFANOUT.

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Output Type Select	Bank0, index04 bit0 **0: PWM output** **1: DC output (default)**	**Only PWM output**	**Only PWM output**
Output Type Select (in PWM output)	CR24 bit4 0: open-drain (default) 1: push-pull	CR24 bit3 0: open-drain (default) 1: push-pull	CR24 bit5 0: open-drain (default) 1: push-pull
PWM Output	Bank0,	Bank0,	Bank0,

Freqency		Index00	Index02	Index10
Fan Control Mode Select		Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	**PWM output (Duty)**	Bank1, index09 bit[7:0]	Bank2, index09 bit[7:0]	Bank3, index09 bit[7:0]
	DC output (Voltage)	Bank1, index09 bit[7:2]		
Current Output Value (read only)		Bank0, index01	Bank0, index03	Bank0, index11

		AUXFANOUT1	**AUXFANOUT2**	
Output Type Select		**Only PWM output**	**Only PWM output**	
Output Type Select (in PWM output)		CR24 bit6 0: open-drain (default) 1: push-pull	CR24 bit7 0: open-drain (default) 1: push-pull	
PWM Output Freqency		Bank0, Index12	Bank0, Index14	
Fan Control Mode Select		Bank8, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank9, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	
Output Value (write)	**PWM output (Duty)**	Bank8, index09 bit[7:0]	Bank9, index09 bit[7:0]	
	DC output (Voltage)			
Current Output Value (read only)		Bank0, Index13	Bank0, Index15	

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 09h for SYSFANOUT, Bank2 Index 09h for CPUFANOUT, Bank3 Index 09h for AUXFANOUT0, Bank8 Index 09h for AUXFANOUT1 and Bank9 Index 09h for AUXFANOUT2. The duty cycle can be calculated using the following equation:

$$\text{Duty cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

The default duty cycle is 7Fh, or 50% for SYSFANOUT and CPUFANOUT, duty cycle is FFh, or 100% for AUXFANOUT0, AUXFANOUT1 and AUXFANOUT2.

Note.The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B.

The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, Index 10, Index 12 and Index 14h.

For DC, the NCT6791F has a six bit digital-to-analog converter (DAC) that produces 0 to 2.048 Volts DC. The analog output is programmed at Bank1 Index 09h bit[7:2] for SYSFANOUT. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = Vref \times \frac{\text{Programmed 6-bit Register Value}}{64}$$

The default value is 111111YY, or nearly 2.048 V, and Y is a reserved bit.

8.7.5 SMART FAN™ Control

The NCT6791F supports various different fan control features:

- SMART FAN™ I (Thermal Cruise & Speed Cruise)
- SMART FAN™ IV
- SMART FAN™ IV Close-Loop Fan Control RPM mode

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Mode Select	Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV

	AUXFANOUT1	AUXFANOUT2	
Fan Control Mode Select	Bank8, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank9, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	

8.7.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Temperature Source Select	Bank1, index00 bit[4:0] Default: SYSTIN	Bank2, index00 bit[4:0] Default: CPUTIN	Bank3, index00 bit[4:0] Default: AUXTIN0
Fan Control Temperature Reading	Bank0, index73 & Bank0, index74 bit7	Bank0, index75 & Bank0, index76 bit7	Bank0, index77 & Bank0, index78 bit7

	AUXFANOUT1	AUXFANOUT2	

Fan Control Temperature Source Select	Bank8, index00 bit[4:0] Default: AUXTIN1	Bank9, index00 bit[4:0] Default: AUXTIN2	
Fan Control Temperature Reading	Bank0, index79 & Bank0, index7A bit7	Bank0, index7B & Bank0, index7C bit7	

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

Figure 8-10 SMART FAN^{TM} Function Block Diagram

8.8 SMART FAN^{TM} I

8.8.1 Thermal Cruise Mode

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified “stop value”.

This “stop value” is enabled by the Bank1, Index00h, Bit7 for SYSFANOUT; Bank2, Index00h, Bit7 for CPUFANOUT ; Bank3, Index00h, Bit7 for AUXFANOUT0; Bank8, Index00h, Bit7 for AUXFANOUT1 and Bank9, Index00h, Bit7 for AUXFANOUT2.
The “stop value” itself is separately specified in Bank1 Index05h, Bank2 Index05h, Bank3 Index05h, Bank8 Index05h and Bank9 Index05h.

The “stop time” means fan remains at the stop value for the period of time also separately defined in Bank1 Index07h, Bank2 Index07h, Bank3 Index07h, Bank8 Index07h and Bank9 Index07h.

Note. The function only support for Thermal Cruise Mode.

Figure 8-11 Thermal Cruise™ Mode Parameters Figure

In general, Thermal Cruise mode means

- If the current temperature is higher than the high end, increase the fan speed.
- If the current temperature is lower than the low end, decrease the fan speed.
- Otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

Figure 8-12 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

Figure 8-13 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.8.2 Speed Cruise Mode

Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

Figure 8-14 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-2 Relative Registers – at Thermal CruiseTM Mode

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP- UP TIME	STEP-DOWN TIME
SYSFANOUT	Bank 1, index 01h bit[7:0]	Bank 1, index 02h Bit[2:0]	Bank 1, index 06h	Bank 1, index 05h	Bank 1, Index 00h, bit7	Bank 1, index 07h	Bank 1, index 03h	Bank 1, index 04h
CPUFANOUT	Bank 2, index 01h bit[7:0]	Bank 2, index 02h Bit[2:0]	Bank 2, index 06h	Bank 2, index 05h	Bank 2, Index 00h, bit7	Bank 2, index 07h	Bank 2, index 03h	Bank 2, index 04h
AUXFANOUT0	Bank 3, index 01h bit[7:0]	Bank 3, index 02h Bit[2:0]	Bank 3, index 06h	Bank 3, index 05h	Bank 3, Index 00h, bit7	Bank 3, index 07h	Bank 3, index 03h	Bank 3, index 04h
AUXFANOUT1	Bank 8, index 01h bit[7:0]	Bank 8, index 02h Bit[2:0]	Bank 8, index 06h	Bank 8, index 05h	Bank 8, Index 00h, bit7	Bank 8, index 07h	Bank 8, index 03h	Bank 8, index 04h
AUXFANOUT2	Bank 9, index 01h bit[7:0]	Bank 9, index 02h Bit[2:0]	Bank 9, index 06h	Bank 9, index 05h	Bank 9, Index 00h, bit7	Bank 9, index 07h	Bank 9, index 03h	Bank 9, index 04h

THERMAL CRUISE MODE	CRITICAL TEMPERATURE	ENABLE THERMAL CRUISE MODE
SYSFANOUT	Bank 1, index 35h	Bank 1, Index 02h, bit[7:4] = 01h
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 02h, bit[7:4] = 01h
AUXFANOUT0	Bank 3, Index 35h	Bank 3, Index 02h, bit[7:4] = 01h
AUXFANOUT1	Bank 8, Index 35h	Bank 8, Index 02h, bit[7:4] = 01h
AUXFANOUT2	Bank 9, Index 35h	Bank 9, Index 02h, bit[7:4] = 01h

Table 8-3 Relative Registers – at Speed CruiseTM Mode

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP- UP TIME	STEP-DOWN TIME	ENABLE SPEED CRUISE MODE

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP- UP TIME	STEP-DOWN TIME	ENABLE SPEED CRUISE MODE
SYSFANOUT	Bank 1, Index 01h	Bank 1, Index 0C bit[3:0]	Bank 1, Index 02 bit[2:0]	Bank 1, Index 0C bit[6:4]	Bank 1, Index 03h	Bank 1, Index 04h	Bank 1, Index 02h bit[7:4] = 02h
CPUFANOUT	Bank 2, Index 01h	Bank 2, Index 0C bit[3:0]	Bank 2, Index 02 bit[2:0]	Bank 2, Index 0C bit[6:4]	Bank 2, Index 03h	Bank 2, Index 04h	Bank 2, Index 02h bit[7:4] = 02h
AUXFANOUT0	Bank 3, Index 01h	Bank 3, Index 0C bit[3:0]	Bank 3, Index 02 bit[2:0]	Bank 3, Index 0C bit[6:4]	Bank 3, Index 03h	Bank 3, Index 04h	Bank 3, Index 02h bit[7:4] = 02h
AUXFANOUT1	Bank 8, Index 01h	Bank 8, Index 0C bit[3:0]	Bank 8, Index 02 bit[2:0]	Bank 8, Index 0C bit[6:4]	Bank 8, Index 03h	Bank 8, Index 04h	Bank 8, Index 02h bit[7:4] = 02h
AUXFANOUT2	Bank 9, Index 01h	Bank 9, Index 0C bit[3:0]	Bank 9, Index 02 bit[2:0]	Bank 9, Index 0C bit[6:4]	Bank 9, Index 03h	Bank 9, Index 04h	Bank 9, Index 02h bit[7:4] = 02h

8.9 SMART FAN^{TM} IV & Close Loop Fan Control Mode

SMART FAN^{TM} IV and Close Loop Fan Control Mode offer 3 slopes to control the fan speed.

Set **Critical Temperature, Bank1 Index 35$_{HEX}$, Bank2 Index 35$_{HEX}$, Bank3 Index 35$_{HEX}$, Bank8 Index 35$_{HEX}$, Bank9 Index 35$_{HEX}$.**

- Set the **Relative Register-at SMART FAN^{TM} IV Control Mode Table**
  If fan control mode is set as Close Loop Fan Control, the unit step is 50RPM. So the maximum controllable RPM is 50*255=12,750RPM.
- Set Tolerance **of Target Temperature, Bank1 Index 02$_{HEX}$ bit[2:0] . Bank2 Index 02$_{HEX}$ bit[2:0]. Bank3 Index 02$_{HEX}$ bit[2:0], Bank8 Index 02$_{HEX}$ bit[2:0]., Bank9 Index 02$_{HEX}$ bit[2:0].**

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X2 = \frac{(FanDuty3/RPM3)-(FanDuty2/RPM2)}{(T3-T2)}$$

Fan Output:

$$Target\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2)+(Tx-T2)\cdot X2$$

Figure 8-15 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-4 Relative Register-at SMART FAN™ IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 21h	Bank 1, Index 22h	Bank 1, Index 23h	Bank 1, Index 24h
CPUFANOUT	Bank 2, Index 21h	Bank 2, Index 22h	Bank 2, Index 23h	Bank 2, Index 24h
AUXFANOUT0	Bank 3, Index 21h	Bank 3, Index 22h	Bank 3, Index 23h	Bank 3, Index 24h
AUXFANOUT1	Bank 8, Index 21h	Bank 8, Index 22h	Bank 8, Index 23h	Bank 8, Index 24h
AUXFANOUT2	Bank 9, Index 21h	Bank 9, Index 22h	Bank 9, Index 23h	Bank 9, Index 24h
DESCRIPTION	**FD1/PWM1**	**FD2/PWM2**	**FD3/PWM3**	**FD4/PWM4**
SYSFANOUT	Bank 1, Index 27h	Bank 1, Index 28h	Bank 1, Index 29h	Bank 1, Index 2Ah
CPUFANOUT	Bank 2, Index 27h	Bank 2, Index 28h	Bank 2, Index 29h	Bank 2, Index 2Ah
AUXFANOUT0	Bank 3, Index 27h	Bank 3, Index 28h	Bank 3, Index 29h	Bank 3, Index 2Ah
AUXFANOUT1	Bank 8, Index 27h	Bank 8, Index 28h	Bank 8, Index 29h	Bank 8, Index 2Ah
AUXFANOUT2	Bank 9, Index 27h	Bank 9, Index 28h	Bank 9, Index 29h	Bank 9, Index 2Ah

DESCRIPTION	STEP- UP TIME	STEP-DOWN TIME	Enable SMART FAN IV	ENABLE FANOUT STEP	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, index 03h	Bank 1, index 04h	Bank 1, Index 02h bit[7:4] = 04h	Bank 1, Index 20h, Bit0	Bank 1, Index 36h, Bit0	Bank 1, index 37h
CPUFANOUT	Bank 2, index 03h	Bank 2, index 04h	Bank 2, Index 02h bit[7:4] = 04h	Bank 2, Index 20h, Bit0	Bank 2, Index 36h, Bit0	Bank 2, index 37h
AUXFANOUT0	Bank 3, index 03h	Bank 3, index 04h	Bank 3, Index 02h bit[7:4] = 04h	Bank 3, Index 20h, Bit0	Bank 3, Index 36h, Bit0	Bank 3, index 37h
AUXFANOUT1	Bank 8, Index 03h	Bank 9, Index 04h	Bank 8, Index 02h bit[7:4] = 04h	Bank 8, Index 20h, Bit0	Bank 8, Index 36h, Bit0	Bank 8, index 37h
AUXFANOUT2	Bank 9, Index 03h	Bank 9, Index 04h	Bank 9, Index 02h bit[7:4] = 04h	Bank 9, Index 20h, Bit0	Bank 9, Index 36h, Bit0	Bank 9, index 37h

DESCRIPTION	CRITICAL TEMPERATURE	CRITICAL TOLERANCE	TEMPERATURE TOLERANCE	ENABLE RPM MODE	RPM TOLERANCE	ENABLE RPM HIGH MODE
SYSFANOUT	Bank 1, Index 35h	Bank 1, Index 38h, bit[2:0]	Bank 1, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit0	Bank 6, index 01h	Bank 6, Index 06h, Bit0
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 38h, bit[2:0]	Bank 2, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit1	Bank 6, index 02h	Bank 6, Index 06h, Bit1
AUXFANOUT0	Bank 3, Index 35h	Bank 3, Index 38h, bit[2:0]	Bank 3, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit2	Bank 6, index 03h	Bank 6, Index 06h, Bit2
AUXFANOUT1	Bank 8, Index 35h	Bank 8, Index 38h, bit[2:0]	Bank 8, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit3	Bank 6, index 04h	Bank 6, Index 06h, Bit3
AUXFANOUT2	Bank 9, Index 35h	Bank 9, Index 38h, bit[2:0]	Bank 9, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit4	Bank 6, index 05h	Bank 6, Index 06h, Bit4

Figure 8-16 Fan Control Duty Mode Programming Flow

Figure 8-17 Close-Loop Fan Control RPM mode Programming Flow

8.9.1 Step Up Time / Step Down Time

SMART FAN^{TM} IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat.

8.9.2 Fan Output Step

The “Fanout Step” itself is separately specified in Bank1 Index20h bit0 for SYSFANOUT, Bank2 Index20h bit0 for CPUFANOUT, Bank3 Index20h bit0 for AUXFANOUT0, Bank8 Index20h bit0 for AUXFANOUT1 and Bank9 Index20h bit0 for AUXFANOUT2.

This example for Fanout Step exposition:

Figure 8-18 CPUFAN SMART FAN^{TM} IV Table Parameters Figure

Figure 8-19 Fanout Step Relation of CPUFANOUT

8.9.3 Revolution Pulse Selection

The NCT6791F supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution.The others could be set by HM register at Bank6, Index44, Bit1-0 for SYSFANIN; Index45, Bit1-0 for CPUFANIN; Index46, Bit1-0 for AUXFANIN0; Index47, Bit1-0 for AUXFANIN1 and Index48, Bit1-0 for AUXFANIN2. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for “Pulse Selections Bits”:

00: 4 pulses per revolution
01: 1 pulse per revolution
10: 2 pulses per revolution (default)
11: 3 pulses per revolution

8.9.4 Weight Value Control

The NCT6791F supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of SMART FAN^{TM} I or IV and output to the fan. Take CPUFANOUT for example, if SMART FAN^{TM} IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN^{TM} IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

Figure 8-20 SYS TEMP and Weight Value Relations shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN

temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

Nots：This relative register should not be zero and not support negative temperature.

Figure 8-20 SYS TEMP and Weight Value Relations

Table 8-5 Relative Register-at Weight Value Control

DESCRIPTION	ENABLE WEIGHT MODE	WEIGHT TEMPERATURE SOURCE SELECT
SYSFANOUT	Bank 1, Index 39h, bit7	Bank 1, Index 39h, bit[4:0]
CPUFANOUT	Bank 2, Index 39h, bit7	Bank 2, Index 39h, bit[4:0]
AUXFANOUT0	Bank 3, Index 39h, bit7	Bank 3, Index 39h, bit[4:0]
AUXFANOUT1	Bank 8, Index 39h, bit7	Bank 8, Index 39h, bit[4:0]
AUXFANOUT2	Bank 9, Index 39h, bit7	Bank 9, Index 39h, bit[4:0]

DESCRIPTION	TEMP BASE	DUTY BASE	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP
SYSFANOUT	Bank 1, Index 3Dh	Bank 1, Index 3Eh	Bank 1, Index 3Ah	Bank 1, Index 3Bh	Bank 1, Index 3Ch

DESCRIPTION	TEMP BASE	DUTY BASE	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP
CPUFANOUT	Bank 2, Index 3Dh	Bank 2, Index 3Eh	Bank 2, Index 3Ah	Bank 2, Index 3Bh	Bank 2, Index 3Ch
AUXFANOUT0	Bank 3, Index 3Dh	Bank 3, Index 3Eh	Bank 3, Index 3Ah	Bank 3, Index 3Bh	Bank 3, Index 3Ch
AUXFANOUT1	Bank 8, Index 3Dh	Bank 8, Index 3Eh	Bank 8, Index 3Ah	Bank 8, Index 3Bh	Bank 8, Index 3Ch
AUXFANOUT2	Bank 9, Index 3Dh	Bank 9, Index 3Eh	Bank 9, Index 3Ah	Bank 9, Index 3Bh	Bank 9, Index 3Ch

Figure 8-21 Fan Control Weighting Duty Mode Programming Flow

8.10 Alert and Interrupt

NCT6791F supports 6 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	SMIOVT2
Temperature source select	Bank6, index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default: CPUTIN
Temperature reading (2's complement)	Bank0, index27	Bank1, index50 & index51 bit7
Temperature High Limit	Bank0, index39	Bank1, index55 & index56 bit7
Temperature Low Limit	Bank0, index3A	Bank1, index53 & index54 bit7

SMIOVT Relative Temperature Registers

8.10.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin.128) is a multi-function pin. It can be in HM_SMI# mode or in OVT# mode by setting Configuration Register CR24h, bit 2. In HM_SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.10.2 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.

*Interrupt Reset when Interrupt Status Registers are read

Figure 8-22 SMI Mode of Voltage and Fan Inputs

8.10.3 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.10.4 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN / AUXTIN.

8.10.4.1. Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)

The SMI# pin has four interrupt modes with Temperature Sensor 1.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index 40h, bit 4 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

Figure 8-23 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C. This mode is enabled by setting Bank0 Index 40h, bit 4 to 0.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.

*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-24 SMI Mode of SYSTIN I

(3) Two-Times Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to zero. This mode is enabled by setting Bank0 Index 40h, bit 4 to 0.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Figure 3- **One-Time Interrupt Mode**

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to one. This mode is enabled by setting Bank0 Index 40h, bit 4 to 0.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.

*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-25 SMI Mode of SYSTIN II

8.10.4.2. SMI# Interrupt of Temperature Sensor 2 (Default: CPUTIN) and Temperature Sensor 3 (Default: AUXTIN) and Temperature Sensor 4 (Default: SYSTIN) and Temperature Sensor 5 (Default: SYSTIN) and Temperature Sensor 6 (Default: SYSTIN).

The SMI# pin has 3 interrupt modes with Temperature Sensor 2~6.

(1) Shut-down Interrupt Mode

This mode is enabled by Bank0 Index 40h, bit5 to one for Temperature Sensor 2; Bank0 Index 40h, bit6 to one for Temperature Sensor 3; Bank6 Index 74h, bit1 to one for Temperature Sensor 4; Bank6 Index 79h, bit1 to one for Temperature Sensor 5 and Bank6 Index 7Eh, bit1 to one for Temperature Sensor 6.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

Figure 8-26 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.

*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode

Two-Times Interrupt Mode

Figure 8-27 SMI Mode of CPUTIN

(3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Table 8-6 Relative Register of SMI functions

	SHUTDOWN MODE	**COMPARATOR MODE**	**TWO-TIME INTERRUPT MODE**	**ONE-TIME INTERRUPT MODE**
SMIOVT1	Bank0,Index40_Bit4 (EN_WS=1) Bank0,Index43 _Bit4(TIN=0) Bank0,Index46 _Bit3 (Shut = 0)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index3A (Thyst = 8'h7F)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index4C_Bit5 (EN_T1_One = 0)	Bank0,Index43_ Bit4 Bank0,Index4C_ Bit5
SMIOVT2	Bank0,Index40_Bit5 (EN_WS=1) Bank0,Index43_ Bit5(TIN=0) Bank0,Index46_ Bit 4 (Shut = 0)	Bank0,Index43_Bit5 (TIN=0) Bank0,Index4C_ Bit6 (T2T3_INT=1)	Bank0,Index43_ Bit5(TIN=0) Bank0,Index4C_ Bit6 (T2T3_INT=0)	

Table 8-7 Relative Register of OVT functions

SMIOVT1	SMIOVT2
Bank0,Index18_Bit6=0 (Enable OVT output) **Bank0,Index18_Bit4** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank0, Index18_Bit0** **0:** Start to monitor the source of SMIOVT1 temperature. **1:** Stop monitoring the source of SMIOVT1 temperature.	**Bank1, Index52_Bit0** **0:** Start to monitor the source of SMIOVT2 temperature. **1:** Stop monitoring the source of SMIOVT2 temperature. **Bank 0, Inedex4C_Bit 3** **0:** Disable SMIOVT2 temperature sensor over temperature output **1:** Enable SMIOVT2 temperature sensor over temperature output **Bank 1, Index52_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 1, Index52_Bit 3~4** Number of faults to detect before setting OVT# output.

8.10.5 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[24h], bit 2 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and OVT pin could be enabled to OVT output by Bank0 Index 18h, bit 6 for Temperature Sensor 1(default: SYSTIN); Bank1 Index 52h, bit 1 for Temperature Sensor 2(default: CPUTIN); Bank2 Index 52h, bit1 for Temperature Sensor 3(default: AUXTIN); Bank6 Index 28h, bit1 for Temperature Sensor 4(default: SYSTIN); Bank6 Index 29h, bit1 for Temperature Sensor 5(default: SYSTIN)and Bank6 Index 2Ah, bit1 for Temperature Sensor 6(default: SYSTIN).

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.

Figure 8-28 OVT# Modes of Temperature Inputs

If Bank0 Index 18h, bit 4, is set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index 18h, bit 4, is set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.10.6 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possible tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either Pin 99 (VBAT) or Pin 85 (3VSB). 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN0# or CASEOPEN1# must be pulled high by an externally pulled-up 2MΩ resistor that is connected to VBAT (pin 99). When the case is opened, CASEOPEN0# or CASEOPEN1# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The CASEOPEN0# status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to “1” first and then to “0”. The CASEOPEN1# status will not be cleared unless CR[46h], bit 6, or CR[Eeh] bit 0 at Logical Device A is set to “1” first and then to “0”.

Figure 8-29 Caseopen Mechanism

8.11 Power Measurement

Figure 8-30 Power measurement architecture

This function will detect the voltage from current measurement IC on board and calculate the current and power. Fig 8.28 is the architecture. Vin3 ($Vin3 = Power_V \times \frac{R1}{R1+R2}$) and Vin1 ($Vin1 = Is \times Rs \times Gm \times RL2$) could

	HM Register	Note
Is	Bank4 Index 60h & Index 61h	Calculate by IO
POWER	Bank4 Index 62h & Index 63h	Calculate by IO
VIN	Bank4 Index 64h	Given by user
Rre	Bank4 Index 65h	Given by user Rreg=Rs*RL2*Gm
Reg_Ration_K	Bank4 Index 66h	Given by user Reg_Ration_K = (R1+R2)/(R1)
Power_Volt_En	Bank4 Index 66h	Given by user
POWER_V	Bank4 Index 67h	Calculate by IO or given by user depend on Power_Volt_En
Vin1	Bank0 Index 24h	Measure by IO

not over 2.048. We suggest the ratio $\frac{R1}{R1+R2} = \frac{1}{15}$.

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at Bank0, index 04Eh.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6-0	**READ/WRITE.**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved (Power On default 0)	Address Pointer (Power On default 00h)						
	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 SYSFANOUT PWM Output Frequency Configuration Register – Index 00h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is progarmmed for PWM output (i.e., Bank0, Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	**PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.4 SYSFANOUT Output Value Select Register – Index 01h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.						Reserved	
This register could be programmed by Bank1, Index 09									

9.5 CPUFANOUT PWM Output Frequency Configuration Register – Index 02h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.** This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	**PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency. If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.6 CPUFANOUT Output Value Select Register – Index 03h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	CPUFANOUT PWM Duty. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.							
This register could be programmed by Bank2, Index 09									

9.7 SYSFANOUT Configuration Register I – Index 04h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED							SYSFANOUT_SEL
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-1	Reserved.
0	**SYSFANOUT Output Mode Selection.**

BIT	DESCRIPTION
	0: SYSFANOUT pin produces a PWM duty cycle output. 1: SYSFANOUT pin produces DC output. **(Default)**

9.8 Reserved Register – Index 05h ~ 0Fh (Bank 0)

9.9 AUXFANOUT0 PWM Output Frequency Configuration Register – Index 10h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT0 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL3. AUXFANOUT0 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE3. AUXFANOUT0 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.10 AUXFANOUT0 Output Value Select Register – Index 11h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value							
DEFAULT	FFh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT0 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by Bank3, Index 09									

9.11 AUXFANOUT1 PWM Output Frequency Configuration Register – Index 12h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL4	PWM_SCALE4						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT1 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL4. AUXFANOUT1 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE4. AUXFANOUT1 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.12 AUXFANOUT1 Output Value Select Register – Index 13h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value							
DEFAULT	FFh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT1 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by Bank8, Index 09									

9.13 AUXFANOUT2 PWM Output Frequency Configuration Register – Index 14h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL5	PWM_SCALE5						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT2 is programmed for PWM output.

BIT	DESCRIPTION

BIT	DESCRIPTION
7	**PWM_CLK_SEL5. AUXFANOUT2 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE5. AUXFANOUT2 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.14 AUXFANOUT2 Output Value Select Register – Index 15h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	FFh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT2 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh							

		creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.
This register could be programmed by Bank9, Index 09		

9.15 Reserved Register – Index 16-17h (Bank 0)

9.16 OVT# Configuration Register – Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	RESERVED	DIS_OVT1	RESERVED	OVT1_Mode	RESERVED			STOP
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**DIS_OVT1.** 0: Enable SMIOVT1 OVT# output. (Default) 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output.
5	**Reserved.**
4	**OVT1_Mode. SMIOVT1 Mode Select.** 0 : Compare Mode. (Default) 1 : Interrupt Mode.
3-1	**Reserved.**
0	**STOP.** **0: Monitor SMIOVT1 temperature source.** **1: Stop monitoring SMIOVT1 temperature source.**

9.17 Reserved Registers – Index 19h ~ 1Fh (Bank 0)

9.18 Value RAM — Index 27h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
27h	SMIOVT1 temperature source reading.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN1 High Limit
2Eh	VIN1 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN0 High Limit

ADDRESS A6-A0	DESCRIPTION
34h	VIN0 Low Limit
35h	VCOREREFIN High Limit
36h	VCOREREFIN Low Limit
37h	VIN4 High Limit
38h	VIN4 Low Limit
39h	SMIOVT1 temperature sensor High Limit
3Ah	SMIOVT1 temperature sensor Hysteresis Limit

9.19 Configuration Register – Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	RESERVED	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	**RESERVED**
5	**Output type of SMIOVT2:** 1: SMI# output type of SMIOVT Source2 temperature (Default: CPUTIN) is Shut-down Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit6.
4	**Output type of SMIOVT1** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit5.
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved.**
1	**SMI# Enable.** A one enables the SMI# Interrupt output. 1: Enable SMI# function (Deafult) 0: Disable SMI# function
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the “INT_Clear” bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.20 Interrupt Status Register 1 – Index 41h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	CPUFANIN	SYSFANIN	SOURCE2 _ SMI	SOURCE1 _ SMI	3VCC	AVCC	VIN1	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN.** A one indicates the fan count limit of CPUFANIN has been exceeded.
6	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
5	**SMIOVT2.** A one indicates the high limit of SMIOVT2 temperature has been exceeded. (CPUTIN is default temperature)
4	**SMIOVT1.** A one indicates the high limit of SMIOVT1 temperature has been exceeded. (SYSTIN is default temperature)
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVCC (Pin 106).** A one indicates the high or low limit of AVCC has been exceeded.
1	**VIN1.** A one indicates the high or low limit of VIN1 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

9.21 Interrupt Status Register 2 – Index 42h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.	CASEOPEN1	RESERVED	CASEOPEN0	AUXFANIN0	VCOREREFIN	VIN4	VIN0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**CASEOPEN1.** A one indicates the case has been opened.
5	**RESERVED**
4	**CASEOPEN0.** A one indicates the case has been opened.
3	**AUXFANIN0.** A one indicates the fan count limit of AUXFANIN0 has been exceeded.
2	**VCOREREFIN.** A one indicates the high or low limit of VCOREREFIN has been exceeded.
1	**VIN4.** A one indicates the high or low limit of VIN4 has been exceeded.
0	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.

9.22 SMI# Mask Register 1 – Index 43h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	VIN1	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**CPUFANIN.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**SYSFANIN.**	
5	**SMIOVT2.**	
4	**SMIOVT1.**	
3	**3VCC.**	
2	**AVCC (Pin 106).**	
1	**VIN1.**	
0	**CPUVCORE.**	

9.23 SMI# Mask Register 2 – Index 44h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	RESERVED	CASEOPEN0	AUXFANIN0	VIN4	VCOREREFIN	VIN0
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**TAR2.**	A one disables the corresponding interrupt status bit for the interrupt. (See Interrupt Status Register 2 – Index 42h (*Bank 0*))
6	**TAR1.**	
5	**RESERVED**	
4	**CASEOPEN0.**	
3	**AUXFANIN0.**	
2	**VIN4.**	
1	**VCOREREFIN.**	
0	**VIN0.**	

9.24 Interrupt Status Register 4 – Index 45h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		AUX FANOUT0	CPU FANOUT	SYS FANOUT	RESERVED	Shut_ SOURCE2_SMI	Shut_ SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED**
6	**RESERVED**
5	**AUXFANOUT0.** “1” indicates that AUXFANOUT0 works for three minutes at the full fan speed.

BIT	DESCRIPTION
4	**CPUFANOUT.** “1” indicates that CPUFANOUT works for three minutes at the full fan speed.
3	**SYSFANOUT.** “1” indicates that SYSFANOUT works for three minutes at the full fan speed.
2	**RESERVED**
1	**Shut_SOURCE2_SMI.** “1” indicates the high limit of SMIOVT _SOURCE2 temperature of SMI# Shut-down mode has been exceeded. (CPUTIN is default temperature)
0	**Shut_SOURCE1_SMI.** “1” indicates the high limit of SMIOVT _SOURCE1 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)

9.25 SMI# Mask Register 3 – Index 46h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR0	CASEOPEN CLEAR1	RESERVED	Shut_CPU	Shut_SYS	AUXFANIN2	AUXFANIN1	CASEOPEN1
DEFAULT	0	0	0	1	1	1	1	0

BIT	DESCRIPTION	
7	**CASEOPEN0 Clear Control.** Writing 1 to this bit will clear CASEOPEN status. This bit will be cleared itself. The function is the same as LDA, CR[E6h], bit 5.	
6	**CASEOPEN1 Clear Control.** Writing 1 to this bit will clear CASEOPEN status. This bit will be cleared itself. The function is the same as LDA, CR[E6h], bit 5.**.**	
5	**RESERVED**	“1” disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
4	**Shut_SOURCE2_SMI**	
3	**Shut_SOURCE1_SMI**	
2	**AUXFANIN2**	“1” disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt.
1	**AUXFANIN1**	“1” disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt
0	**CASEOPEN1**	“1” disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt.

9.26 Reserved Register – Index 47h (Bank 0)

9.27 Serial Bus Address Register – Index 48h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SERIAL BUS ADDRESS						

DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**Reserved (Read Only).**
6-0	**Serial Bus Address <7:1>**

9.28 Reserved Register – Index 49h ~ 4Bh (Bank 0)

9.29 SMI/OVT Control Register1 – Index 4Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**T2ToT6_INT MODE**	**EN_T1 _ONE**	**RESERVED**	**DIS_ OVT2**	**OVTPOL**	**RESERVED**	
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**T2ToT6_INTMode.** 1: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Comparator Interrupt mode. 0: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Two-Times Interrupt mode. (Default)
5	**EN_T1_ONE.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default)
4	**RESERVED**
3	**DIS_OVT2.** 1: Disable SMIOVT Source2 temperature sensor (Default: CPUTIN) over-temperature (OVT) output. 0: Enable SMIOVT Source2 temperature OVT output through pin OVT#. (Default)
2	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low (Default).
1-0	**Reserved.**

9.30 FAN IN/OUT Control Register – Index 4Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**FANOPV4**	**FANINC4**	**FANOPV3**	**FANINC3**	**FANOPV2**	**FANINC2**	**FANOPV1**	**FANINC1**

DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION
7	**FANOPV4. AUXFANIN1 output value**, only if bit 2 is set to zero. 1: Pin 124 (CPUFANIN) generates a logic-high signal. 0: Pin 124 generates a logic-low signal. (Default)
6	**FANINC4. AUXFANIN1 Input Control.** 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.
5	**FANOPV3. AUXFANIN0 output value**, only if bit 2 is set to zero. 1: Pin 124 (CPUFANIN) generates a logic-high signal. 0: Pin 124 generates a logic-low signal. (Default)
4	**FANINC3. AUXFANIN0 Input Control.** 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.
3	**FANOPV2. CPUFANIN output value**, only if bit 2 is set to zero. 1: Pin 124 (CPUFANIN) generates a logic-high signal. 0: Pin 124 generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN Input Control.** 1: Pin 124 (CPUFANIN) acts as a fan tachometer input. (Default) 0: Pin 124 acts as a fan control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: Pin 126 (SYSFANIN) generates a logic-high signal. 0: Pin 126 generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.

9.31 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**HBACS**	**Reserved.**			**BANK SEL3**	**BANK SEL2**	**BANK SEL1**	**BANK SEL0**
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**HBACS. HBACS – High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.
6	**Reserved.**
5	**Reserved.**
4	**Reserved.**

BIT	DESCRIPTION	
3	**BANKSEL3.**	Bank Select for Bank0 to Bank7. The Three -bit binary value corresponds to the bank number. For example, "0010" selects bank2.
2	**BANKSEL2.**	
1	**BANKSEL1.**	
0	**BANKSEL0.**	

9.32 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.33 FAN IN/OUT Control Register – Index 50h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						FANOPV5	FANINC5
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7~2	**Reserved**
1	**FANOPV5. AUXFANIN2 output value**, only if bit 0 is set to zero. 1: Pin 126 (SYSFANIN) generates a logic-high signal. 0: Pin 126 generates a logic-low signal. (Default)
0	**FANINC5. SYSFANIN2 Input Control.** 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.

9.34 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only

Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.35 Reserved Register – Index 51h ~ 57h (Bank 0)

9.36 Chip ID – Index 58h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.37 Reserved Register – Index 59h ~ 5Ch (Bank 0)

9.38 VBAT Monitor Control Register – Index 5Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	DIODES6	DIODES5	DIODES4	DIODES3	DIODES2	DIODES1	EN_ VBAT _MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**DIODES 6. Sensor type selection for AUXTIN3.** 1: Diode sensor. 0: Thermistor sensor. (default)

BIT	DESCRIPTION
5	**DIODES 5. Sensor type selection for AUXTIN2.** 1: Diode sensor. 0: Thermistor sensor. (default)
4	**DIODES 4. Sensor type selection for AUXTIN1.** 1: Diode sensor. 0: Thermistor sensor. (default)
3	**DIODES 3. Sensor type selection for AUXTIN0.** 1: Diode sensor. 0: Thermistor sensor. (default)
2	**DIODES 2. Sensor type selection for CPUTIN.** 1: Diode sensor. (default) 0: Thermistor sensor.
1	**DIODES 1. Sensor type selection for SYSTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.39 Current Mode Enable Register – Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	EN_ AUXTIN3 CURRENT MODE	EN_ AUXTIN2 CURRENT MODE	EN_ AUXTIN1 CURRENT MODE	EN_ AUXTIN0 CURRENT MODE	EN_ CPUTIN CURRENT MODE	EN_ SYSTIN CURRENT MODE	Reserved
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Enable AUXTIN3 Current Mode**. With AUXTIN3 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN3 by Current Mode. 0: Temperature sensing of AUXTIN3 depends on the setting of Index 5Dh. **(Default)**
5	**Enable AUXTIN2 Current Mode**. With AUXTIN2 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN2 by Current Mode. 0: Temperature sensing of AUXTIN2 depends on the setting of Index 5Dh. **(Default)**
4	**Enable AUXTIN1 Current Mode**. With AUXTIN1 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN1 by Current Mode. 0: Temperature sensing of AUXTIN1 depends on the setting of Index 5Dh. **(Default)**
3	**Enable AUXTIN0 Current Mode**. With AUXTIN0 is selected to Diode sensor (Bank0, Index

BIT	DESCRIPTION
	5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN0 by Current Mode. 0: Temperature sensing of AUXTIN0 depends on the setting of Index 5Dh. **(Default)**
2	**Enable CPUTIN Current Mode.** With CPUTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 2 = 1). 1: Temperature sensing of CPUTIN by Current mode. **(Default)** 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	**Enable SYSTIN Current Mode.** With SYSTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 1 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. **(Default)**
0	**Reserved.**

9.40 Reserved Register – Index 5F (Bank 0)

9.41 PORT 80 DATA INPUT Register – Index 60 (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	P80_IN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PORT 80 DATA INPUT**

9.42 Reserved Register – Index 61F ~ 72F (Bank 0)

9.43 MONITOR TEMPERATURE 1 Register (Integer Value)- Index 73h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 1 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 1 [8:1]** SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])

9.44 MONITOR TEMPERATURE 1 Register (Fractional Value)- Index 74h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 1 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**MONITOR TEMPERATURE 1 [0]** SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])
6-0	**Reserved**

9.45 MONITOR TEMPERATURE 2 Register (Integer Value)- Index 75h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 2 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 2 [8:1]** CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])

9.46 MONITOR TEMPERATURE 2 Register (Fractional Value)- Index 76h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 2 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**MONITOR TEMPERATURE 2 [0]** CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])
6-0	**Reserved**

9.47 MONITOR TEMPERATURE 3 Register (Integer Value)- Index 77h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 3 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 3 [8:1]** AUXFANOUT0 fan control temperature reading. (Source is selected by Bank3, Index00 bit[4:0])

9.48 MONITOR TEMPERATURE 3 Register (Fractional Value)- Index 78h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 3 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 3 [0]** AUXFANOUT0 fan control temperature reading. (Source is selected by Bank3, Index00 bit[4:0])
6-0	**Reserved.**

9.49 MONITOR TEMPERATURE 4 Register (Integer Value)- Index 79h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 4 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 4 [8:1]** AUXFANOUT1 fan control temperature reading. (Source is selected by Bank8, Index00 bit[4:0])

9.50 MONITOR TEMPERATURE 4 Register (Fractional Value)- Index 7Ah (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	MONITOR TEMPERATURE 4 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 4 [0]** AUXFANOUT1 fan control temperature reading. (Source is selected by Bank8, Index00 bit[4:0])
6-0	**Reserved.**

9.51 MONITOR TEMPERATURE 5 Register (Integer Value)- Index 7Bh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 5 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 5 [8:1]** AUXFANOUT2 fan control temperature reading. (Source is selected by Bank9, Index00 bit[4:0])

9.52 MONITOR TEMPERATURE 5 Register (Fractional Value)- Index 7Ch (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 5 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 5 [0]** AUXFANOUT2 fan control temperature reading. (Source is selected by Bank9, Index00 bit[4:0])
6-0	**Reserved.**

9.53 Reserved Register – Index 7Dh~ADh (Bank 0)

9.54 PECI Temperature Reading Enable for SMIOVT and SMART FAN Control Register – Index AEh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_PECI1	EN_PECI0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved.**
1	**Enable PECI Agent1**
0	**Enable PECI Agent0**

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.55 BEEP Control Register 1 – Index B2h (Bank0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En3VSB_BP	EnVIN4_BP	EnVCOREREFIN_BP	EnVIN0_BP	En3VCC_BP	EnAVCC_BP	EnVIN1_BP	EnCPUVCORE_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En3VSB_BP** **1 : Enable 3VSB Beep function** **0 : Disable 3VSB Beep fuction**
6	**EnVIN4_BP** **1 : Enable VIN4 Beep function** **0 : Disable VIN4 Beep fuction**
5	**EnVCOREREFIN_BP** **1 : Enable VCOREREFIN Beep function** **0 : Disable VCOREREFIN Beep fuction**
4	**EnVIN0_BP** **1 : Enable VIN0 Beep function** **0 : Disable VIN0 Beep fuction**
3	**En3VCC_BP** **1 : Enable 3VCC Beep function** **0 : Disable 3VCC Beep fuction**
2	**EnAVCC_BP** **1 : Enable AVCC Beep function** **0 : Disable AVCC Beep fuction**
1	**EnVIN1_BP** **1 : Enable VIN1 Beep function** **0 : Disable VIN1 Beep fuction**
0	**EnCPUVCORE_BP**

BIT	DESCRIPTION
	1 : Enable CPUVCORE Beep function **0 : Disable CPUVCORE Beep fuction**

9.56 BEEP Control Register 2 – Index B3h (Bank0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	User Mode	EnVIN7_ BP	EnVIN3_ BP	EnVIN2_ BP	EnVIN6_ BP	EnVIN5_ BP	EnVTT_ BP	EnVBAT_ BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**User control for Beep alarm** **1 : Enable** **0 : Disable**
6	**EnVIN7_BP** **1 : Enable VIN7 Beep function** **0 : Disable VIN7 Beep fuction**
5	**EnVIN3_BP** **1 : Enable VIN3 Beep function** **0 : Disable VIN3 Beep fuction**
4	**EnVIN2_BP** **1 : Enable VIN2 Beep function** **0 : Disable VIN2 Beep fuction**
3	**EnVIN6_BP** **1 : Enable VIN6 Beep function** **0 : Disable VIN6 Beep fuction**
2	**EnVIN5_BP** **1 : Enable VIN5 Beep function** **0 : Disable VIN5 Beep fuction**
1	**EnVTT_BP** **1 : Enable VTT Beep function** **0 : Disable VTT Beep fuction**
0	**EnVBAT_BP** **1 : Enable VBAT Beep function** **0 : Disable VBAT Beep fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.57 BEEP Control Register 3 – Index B4h (Bank0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	EnT2 _BP	EnT1 _BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved**
0	**EnT2_BP** **1 : Enable SMIOVT2 Beep function** **0 : Disable SMIOVT2 Beep fuction**
0	**EnT1_BP** **1 : Enable SMIOVT1 Beep function** **0 : Disable SMIOVT1 Beep fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.58 BEEP Control Register 4 – Index B5h (Bank0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En Caseopen1_BP	En Caseopen0_BP	En AUXFANIN2 _BP	En AUXFANIN1 _BP	En AUXFANIN0 _BP	En CPUFANIN _BP	En SYSFANIN _BP	En_Beep
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En Caseopen1_BP** **1 : Enable Caseopen1 Beep function** **0 : Disable Caseopen1 Beep fuction**
6	**En Caseopen0_BP** **1 : Enable Caseopen0_bp Beep function** **0 : Disable Caseopen0_bp Beep fuction**
5	**En AUXFANIN2_BP** **1 : Enable AUXFANIN2 Beep function** **0 : Disable AUXFANIN2 Beep fuction**
4	**En AUXFANIN1_BP** **1 : Enable AUXFANIN1 Beep function** **0 : Disable AUXFANIN1 Beep fuction**
3	**En AUXFANIN0_BP** **1 : Enable AUXFANIN0 Beep function** **0 : Disable AUXFANIN0 Beep fuction**
2	**En CPUFANIN _BP** **1 : Enable CPUFANIN Beep function** **0 : Disable CPUFANIN Beep fuction**
1	**En SYSFANIN _BP** **1 : Enable SYSFANIN Beep function**

BIT	DESCRIPTION
	0 : Disable SYSFANIN Beep fuction
0	**Enable Beep Function:** **1 : Enable Beep Function** **0 : Disable Beep Fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.59 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		SYSFAN SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to SYSFANOUT Stop Value (Bank1, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**SYSFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source.

BIT	DESCRIPTION
	1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.60 SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 01h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN Target Temperature / SYSFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	SYSFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.61 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 02h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE				Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**SYSFANOUT Mode Select.** 0000: SYSFANOUT is in Manual Mode. **(Default)** 0001: SYSFANOUT is in Thermal Cruise Mode. 0010: SYSFANOUT is in Speed Cruise Mode. 0100: SYSFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.62 SYSFANOUT Step Up Time Register – Index 03h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

(1) For PWM output:
The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:
The units are intervals of 0.4 second. The default time is 4 seconds.

9.63 SYSFANOUT Step Down Time Register – Index 04h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(1) For PWM output:
The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:
The units are intervals of 0.4 second. The default time is 4 seconds.

9.64 SYSFANOUT Stop Value Register – Index 05h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.65 SYSFANOUT Start-up Value Register – Index 06h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	SYSFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.66 SYSFANOUT Stop Time Register – Index 07h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes SYSFANOUT value to fall from the stop value to zero.

(1) For PWM output:
The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:
The units are intervals of 0.4 second. The default time is 4 seconds.

9.67 Reserved Register – Index 08h (Bank 1)

9.68 SYSFANOUT Output Value Select Register – Index 09h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E0h] is the Default Speed Configuration Register of SYSFANOUT.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.						Reserved	

9.69 Reserved Register – Index 0Ah~0Bh (Bank 1)

9.70 SYSFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	SYSFANIN TOL_H			SYSFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	SYSFANIN Tolerance_H [5:3]
3-0	SYSFANIN Target Speed_H [11:8]

9.71 Reserved Register – Index 0Dh~1Fh (Bank 1)

9.72 SMART FAN IV SYSFANOUT STEP Register – Index 20h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_SYSFANOUT_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_SYSFANOUT_STEP** 0: Disable SMART FAN IV has Stepping SYSFANOUT. (default) 1: Enable SMART FAN IV has Stepping SYSFANOUT.

9.73 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.74 SYSFAN (SMART FAN^{TM} IV) Temperature 2 Register(T2) – Index 22h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN^{TM} IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN^{TM} IV) Temperature 2 Register (T2).

9.75 SYSFAN (SMART FAN^{TM} IV) Temperature 3 Register(T3) – Index 23h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN^{TM} IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN^{TM} IV) Temperature 3 Register (T3).

9.76 SYSFAN (SMART FAN^{TM} IV) Temperature 4 Register(T4) – Index 24h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN^{TM} IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN^{TM} IV) Temperature 4 Register (T4).

9.77 Reserved Register – Index 25h~26h (Bank 1)

9.78 SYSFAN (SMART FAN^{TM} IV) DC/PWM 1 Register – Index 27h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN^{TM} IV) DC/PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 1 Register.

9.79 SYSFAN (SMART FAN™ IV) DC/PWM 2 Register – Index 28h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 2 Register.

9.80 SYSFAN (SMART FAN™ IV) DC/PWM 3 Register – Index 29h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 3 Register.

9.81 SYSFAN (SMART FAN™ IV) DC/PWM 4 Register – Index 2Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 4 Register.

9.82 Reserved Register – Index 2Bh~30h (Bank 1)

9.83 SYSFAN 3-Wire Enable Register – Index 31h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	Reserved	EN_SYS_3WFAN
DEFAULT	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_SYS_3WFAN (SYSFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.84 Reserved Register – Index 32h~34h(Bank 1)

9.85 SYSFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Critical Temperature Register.

9.86 SYSFAN Enable Critical Duty – Index 36h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_SYS_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_SYS_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for SYSFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for SYSFANOUT.

9.87 SYSFAN Critical Duty Register – Index 37h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Critical Duty							

DEFAULT	CC

BIT	DESCRIPTION
7-0	SYSFAN Critical Duty.

9.88 SYSFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	SYSFANOUT Critical Temperature Tolerance

9.89 Weight value Configuration Register – Index 39h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_SYSFAN_WEIGHT	Reserved		SYS_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_SYSFAN_WEIGHT.** 0: Disable Weight Value Control for SYSFAN. 1: Enable Weight Value Control for SYSFAN.
6-5	**Reserved**
4-0	**SYSFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source.

BIT	DESCRIPTION
	0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.90 SYSFANOUT Temperature Step Register – Index 3Ah (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step (SYS_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Step**

9.91 SYSFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step Tolerance (SYS_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Step Tolerance**

9.92 SYSFANOUT Weight Step Register – Index 3Ch (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Weight Step (SYS_WEIGHT_STEP)							

DEFAULT	0

BIT	DESCRIPTION
7-0	**SYSFANOUT Weight Step**

9.93 SYSFANOUT Temperature Base Register – Index 3Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**SYSFANOUT Temperature Base (SYS_TEMP_BASE)**							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Base**

9.94 SYSFANOUT Temperature Fan Duty Base Register – index 3Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**SYSFANOUT Temperature Base (SYS_FC_BASE)**							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Start point of Fan Duty increasing**

9.95 SYSFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**						**EN_SYS_PECIERR_DUTY**	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_SYS_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_SYSOUT** Value for SYSFANOUT. 10,11: Keep Full Speed

9.96 Reserved Register – Index 40h (Bank 1)

9.97 SYSFANOUT Pre-Configured Register For PECI Error – Index 41h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured register for PECI error (PECI_ERR_SYSOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SYSFANOUT pre-configured register for PECI error.**

9.98 Reserved Register – Index 42h ~ 4Fh (Bank 1)

9.99 SMIOVT2 Temperature Source (High Byte) Register – Index 50h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.100 SMIOVT2 Temperature Source (Low Byte) Register – Index 51h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	**Temperature <0> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.101 SMIOVT2 Temperature Source Configuration Register – Index 52h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved.** This bit should be set to zero.
1	**OVTMOD. SMIOVT2 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT2 temperature source. 1: Stop monitoring SMIOVT2 temperature source.

9.102 SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.103 SMIOVT2 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.104 SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.105 SMIOVT2 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.106 Reserved Register – Index 57h ~ FFh (Bank 1)

9.107 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		CPUFAN SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to CPUFANOUT Stop Value (Bank2, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**CPUFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source.

BIT	DESCRIPTION
	0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.108 CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 01h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	CPUFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.109 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 02h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE				Reserved	Tolerance of		

						CPUFAN Target Temperature or CPUFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-4	**CPUFANOUT Mode Select.** 0000: CPUFANOUT is in Manual Mode. (Default) 0001: CPUFANOUT is in Thermal Cruise Mode. 0010: CPUFANOUT is in Speed Cruise Mode. 0100: CPUFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.110 CPUFANOUT Step Up Time Register – Index 03h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.111 CPUFANOUT Step Down Time Register – Index 04h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.112 CPUFANOUT Stop Value Register – Index 05h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							

DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.113 CPUFANOUT Start-up Value Register – Index 06h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFANOUT Start-Up Value**							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.114 CPUFANOUT Stop Time Register – Index 07h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFANOUT Value Stop Time**							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes CPUFANOUT value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.115 Reserved Register – Index 08h (Bank 2)

9.116 CPUFANOUT Output Value Select Register – Index 09h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFANOUT Value**							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E1h] is the Default Speed Configuration Register of CPUFANOUT.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output Only	**DESCRIPTION**	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.117 Reserved Register – Index 0Ah~0Bh (Bank 2)

9.118 CPUFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CPUFANIN TOL_H			CPUFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	CPUFANIN Tolerance_H [5:3]
3-0	CPUFANIN Target Speed_H [11:8]

9.119 Reserved Register – Index 0Dh~1Fh (Bank 2)

9.120 SMART FAN IV CPUFANOUT STEP Register – Index 20h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPUFANOUT_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_CPUFANOUT_STEP** 0: Disable SMART FAN IV has Stepping CPUFANOUT. (default) 1: Enable SMART FAN IV has Stepping CPUFANOUT.

9.121 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 1							

DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.122 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFAN (SMART FAN™ IV) Temperature 2**							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.123 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFAN (SMART FAN™ IV) Temperature 3**							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.124 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFAN (SMART FAN™ IV) Temperature 4**							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.125 Reserved Register – Index 25h~26h (Bank 2)

9.126 CPUFAN (SMART FAN™ IV) PWM1 Register – Index 27h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM1 Register.

9.127 CPUFAN (SMART FAN™ IV) PWM2 Register – Index 28h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM2 Register.

9.128 CPUFAN (SMART FAN™ IV) PWM3 Register – Index 29h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM3 Register.

9.129 CPUFAN (SMART FAN™ IV) PWM4 Register – Index 2Ah (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM4 Register.

9.130 Reserved Register – Index 2Bh~30h (Bank 2)

9.131 CPUFAN 3-Wire FAN Enable Register – Index 31h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_CPU_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_CPU_3WFAN (CPUFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.132 Reserved Register – Index 32h ~ 34h(Bank 2)

9.133 CPUFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Critical Temperature Register.

9.134 CPUFAN Enable Critical Duty – Index 36h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPU_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_CPU_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for CPUFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for CPUFANOUT.

9.135 CPUFAN Critical Duty Register – Index 37h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	CPUFAN Critical Duty.

9.136 CPUFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**CPUFANOUT Critical Temperature Tolerance**

9.137 Weight value Configuration Register – Index 39h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_ WEIGHT	Reserved		CPU_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_CPUFAN_WEIGHT.** 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-5	**Reserved**
4-0	**CPUFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source.

BIT	DESCRIPTION
	0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.138 CPUFANOUT Temperature Step Register – Index 3Ah (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step**

9.139 CPUFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step Tolerance**

9.140 CPUFANOUT Weight Step Register – Index 3Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Weight Step (CPU_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Weight Step**

9.141 CPUFANOUT Temperature Base Register – Index 3Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Base**

9.142 CPUFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Start point of Fan Duty increasing**

9.143 CPUFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_CPU_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION

7-2	**Reserved**
1-0	**EN_CPU_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_CPUOUT** Value for CPUFANOUT. 10,11: Keep Full Speed

9.144 Reserved Register – Index 40h (Bank 2)

9.145 CPUFANOUT Pre-Configured Register For PECI Error – Index 41h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured register for PECI error (PECI_ERR_CPUOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**CPUFANOUT pre-configured register for PECI error.**

9.146 Reserved Register – Index 42h ~ FFh (Bank 1)

9.147 AUXFAN0 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN0 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT0 Stop Value (Bank3, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN0 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source.

BIT	DESCRIPTION
	0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.148 AUXFAN0 Target Temperature Register / AUXFANIN0 Target Speed_L Register – Index 01h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXTIN0 Target Temperature / AUXFANIN0 Target Speed_L**							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN0 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN0 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.149 AUXFAN0 MODE Register / AUXFAN0 TOLERRANCE Register – Index 02h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFAN0 MODE**				**Reseved**	**Tolerance of AUXFAN0 Target Temperature or**		

						AUXFANIN0 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT0 Mode Select.** 0000: **AUXFANOUT0** is in Manual Mode. **(Default)** 0001: **AUXFANOUT0** is in Thermal Cruise Mode. 0010: **AUXFANOUT0** is as Speed Cruise Mode. 0100: **AUXFANOUT0** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN0 Target Temperature or AUXFANIN0 Target Speed_L.

9.150 AUXFANOUT0 Step Up Time Register – Index 03h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Value Step Up Time**							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.151 AUXFANOUT0 Step Down Time Register – Index 04h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Value Step Down Time**							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.152 AUXFANOUT0 Stop Value Register – Index 05h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Stop Value**							

DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT0 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.153 AUXFANOUT0 Start-up Value Register – Index 06h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Start-Up Value**							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT0 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.154 AUXFANOUT0 Stop Time Register – Index 07h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Value Stop Time**							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT0 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.155 Reserved Register – Index 08h (Bank 3)

9.156 AUXFANOUT0 Output Value Select Register – Index 09h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Value**							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E2h] is the Default Speed Configuration Register of AUXFANOUT0.

FUNCTION MODE		**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

PWM Output	**DESCRIPTION**	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.

9.157 AUXFANIN0 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN0 TOL_H			AUXFANIN0 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN0 Tolerance_H [5:3]
3-0	AUXFANIN0 Target Speed_H [11:8]

9.158 Reserved Register – Index 0Dh (Bank 3)

9.159 SMART FAN IV AUXFANOUT0 STEP Register – Index 20h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUXFANOUT0_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUXFANOUT0_STEP** 0: Disable SMART FAN IV has Stepping AUXFANOUT0. (default) 1: Enable SMART FAN IV has Stepping AUXFANOUT0.

9.160 AUXFAN0 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 1 Register (T1).

9.161 AUXFAN0 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 2 Register (T2).

9.162 AUXFAN0 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 3 Register (T3).

9.163 AUXFAN0 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 4 Register (T4).

9.164 Reserved Register – Index 25h~26h (Bank 3)

9.165 AUXFAN0 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 1 Register.

9.166 AUXFAN0 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 2 Register.

9.167 AUXFAN0 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 3 Register.

9.168 AUXFAN0 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 4 Register.

9.169 Reserved Register – Index Index 2Bh~30h (Bank 3)

9.170 AUXFAN0 3-Wire Enable Register – Index 31h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	Reserved		EN_AUX0_3WFAN
DEFAULT	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX0_3WFAN (AUXFAN0 type setting)** 0: 4-wire fan 1: 3-wire fan

9.171 Reserved Register – Index 32h~34h(Bank 3)

9.172 AUXFAN0 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Critical Temperature Register

9.173 AUXFAN0 Enable Critical Duty – Index 36h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX0_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX0_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for AUXFANOUT0. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT0.

9.174 AUXFAN0 Critical Duty Register – Index 37h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Critical Duty							

DEFAULT	CC

BIT	DESCRIPTION
7-0	AUXFAN0 Critical Duty.

9.175 AUXFANOUT0 Critical Temperature Tolerance Register – Index 38h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT0 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT0 Critical Temperature Tolerance**

9.176 Weight value Configuration Register – Index 39h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_AUXFAN0_WEIGHT	Reserved		AUX0_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_AUXFAN0_WEIGHT.** 0: Disable Weight Value Control for AUXFAN0. 1: Enable Weight Value Control for AUXFAN0.
6-5	**Reserved**
4-0	**AUXFAN0 Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source.

BIT	DESCRIPTION
	0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.177 AUXFANOUT0 Temperature Step Register – Index 3Ah (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Temperature Step (AUX0_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT0 Temperature Step**

9.178 AUXFANOUT0 Temperature Step Tolerance Register – Index 3Bh (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Temperature Step Tolerance (AUX0_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT0 Temperature Step Tolerance**

9.179 AUXFANOUT0 Weight Step Register – Index 3Ch (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Weight Step (AUX0_WEIGHT_STEP)							

DEFAULT	0

BIT	DESCRIPTION
7-0	**AUXFANOUT0 Weight Step**

9.180 AUXFANOUT0 Temperature Base Register – Index 3Dh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Temperature Base (AUX0_TEMP_BASE)**							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT0 Temperature Base**

9.181 AUXFANOUT0 Temperature Fan Duty Base Register – Index 3Eh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Temperature Base (AUX0_FC_BASE)**							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT0 Start point of Fan Duty increasing**

9.182 AUXFAN0 PECIERR DUTY Enable Register – Index 3Fh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**						**EN_AUX0_PECIERR_DUTY**	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_AUX0_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT0** Value for AUXFANOUT0. 10,11: Keep Full Speed

9.183 Reserved Register – Index 40h (Bank 3)

9.184 AUXFANOUT0 Pre-Configured Register For PECI Error – Index 41h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 pre-configured register for PECI error (PECI_ERR_AUXOUT0)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT0 pre-configured register for PECI error.**

9.185 Reserved Register – Index 42h ~ FFh (Bank 3)

9.186 PCH_CHIP_CPU_MAX_TEMP Register – Index 00h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_CPU_MAX_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_CPU_MAX_TEMP:** The maximum temperature in absolute degree C, of the CPU and MCH.

9.187 PCH_CHIP_TEMP Register – Index 01h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_TEMP** The IBX_CHIP temperature in degree C.

9.188 PCH_CPU_TEMP_H Register – Index 02h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CPU_TEMP_H** The CPU temperature in degree C. (Integer Part)

9.189 PCH_CPU_TEMP_L Register – Index 03h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_L						Reserved	Reading _Flag
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**PCH_CPU_TEMP_L** The CPU temperature in degree C. (Fractional Part)
1	**Reserved**
0	**Reading_Flag:** If there is an error when the IBX read the data from the CPU, then Bit0 is set to '1'.

9.190 PCH_MCH_TEMP Register – Index 04h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_MCH_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_MCH_TEMP** The MCH temperature in degree C.

9.191 PCH_DIM0_TEMP Register – Index 05h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM0_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM0_TEMP** The DIM0 temperature in degree C.

9.192 PCH_DIM1_TEMP Register – Index 06h (Bank 4)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM1_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM1_TEMP** The DIM1 temperature in degree C.

9.193 PCH_DIM2_TEMP Register – Index 07h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM2_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM2_TEMP** The DIM2 temperature in degree C.

9.194 PCH_DIM3_TEMP Register – Index 08h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM3_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM3_TEMP** The DIM3 temperature in degree C.

9.195 PCH_TSI0_TEMP_H Register – Index 09h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI0_TEMP_H** The TSI High-Byte temperature in degree C.

9.196 PCH_TSI0_TEMP_L Register – Index 0Ah (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI0_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.197 PCH_TSI1_TEMP_H Register – Index 0Bh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI1_TEMP_H** The TSI High-Byte temperature in degree C.

9.198 PCH_TSI1_TEMP_L Register – Index 0Ch (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI1_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.199 PCH_TSI2_TEMP_H Register – Index 0Dh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI2_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**PCH_TSI2_TEMP_H** The TSI High-Byte temperature in degree C.

9.200 PCH_TSI2_TEMP_L Register – Index 0Eh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI2_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI2_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.201 PCH_TSI3_TEMP_H Register – Index 0Fh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI3_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI3_TEMP_H** The TSI High-Byte temperature in degree C.

9.202 PCH_TSI3_TEMP_L Register – Index 10h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI3_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI3_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.203 PCH_TSI4_TEMP_H Register – Index 11h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PCH_TSI4_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI4_TEMP_H** The TSI High-Byte temperature in degree C.

9.204 PCH_TSI4_TEMP_L Register – Index 12h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI4_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI4_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.205 PCH_TSI5_TEMP_H Register – Index 13h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI5_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI5_TEMP_H** The TSI High-Byte temperature in degree C.

9.206 PCH_TSI5_TEMP_L Register – Index 14h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI5_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI5_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.207 PCH_TSI6_TEMP_H Register – Index 15h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI6_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI6_TEMP_H** The TSI High-Byte temperature in degree C.

9.208 PCH_TSI6_TEMP_L Register – Index 16h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI6_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI6_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.209 PCH_TSI7_TEMP_H Register – Index 17h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI7_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI7_TEMP_H** The TSI High-Byte temperature in degree C.

9.210 PCH_TSI7_TEMP_L Register – Index 18h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI7_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI7_TEMP_L** The TSI Low-Byte temperature in degree C.

BIT	DESCRIPTION
4-0	**Reserved**

9.211 ByteTemp_H Register – Index 19h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_H** The TSI Byte format High-Byte temperature in degree C.

9.212 ByteTemp_L Register – Index 1Ah (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_L** The TSI Byte format Low-Byte temperature in degree C.

9.213 Reserved Register – Index 1Bh ~ 22h (Bank 4)

9.214 VIN1 High Limit Compared Voltage Register – Index 23h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 High Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**VIN1 High Limit Compared Voltage.** Default: 0x96h (1.2V)

9.215 VIN1 Low Limit Compared Voltage Register – Index 24h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	VIN1 Low Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	**VIN1 Low Limit Compared Voltage.** Default: 0x64h (0.8V)

9.216 VIN0 High Limit Compared Voltage Register – Index 25h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 High Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**VIN0 High Limit Compared Voltage.** Default: 0x96h (1.2V)

9.217 VIN0 Low Limit Compared Voltage Register – Index 26h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 Low Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	**VIN0 Low Limit Compared Voltage.** Default: 0x64h (0.8V)

9.218 AVCC High Limit Compared Voltage Register – Index 27h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVCC High Limit Compared Voltage (AVCC _LimtH)							
DEFAULT	1	1	1	0	0	0	0	1

BIT	DESCRIPTION
7-0	**AVCC High Limit Compared Voltage.** Default: 0xE1h (1.8V *2)

9.219 AVCC Low Limit Compared Voltage Register – Index 28h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVCC Low Limit Compared Voltage (AVCC_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**AVCC Low Limit Compared Voltage (AVCC_LimtH).** Default: 0x96h (1.2V *2)

9.220 Reserved Register – Index 29h ~ 41h (Bank 4)

9.221 Voltage Comparation Interrupt Status Register - Index 42h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AVCC_Warn	VIN0_Warn	VIN1_Warn
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved.**
2	**AVCC_Warn.** A one indicates the limit of AVCC voltage has been exceeded.
1	**VIN0_Warn.** A one indicates the limit of VIN0 voltage has been exceeded.
0	**VIN1_Warn** A one indicates the limit of VIN1 voltage has been exceeded.

9.222 Reserved Register – Index 43h ~ 49h (Bank 4)

9.223 AUXTIN1 Temperature Sensor Offset Register – Index 4Ah (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN1 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.224 AUXTIN2 Temperature Sensor Offset Register – Index 4Bh (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN2 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.225 AUXTIN3 Temperature Sensor Offset Register – Index 4Ch (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN3 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.226 Reserved Register – Index 4Eh ~ 4Fh (Bank 4)

9.227 Interrupt Status Register 3 – Index 50h (Bank 4)

Attribute: Read Clear
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2	AUXFANOUT1	AUXFANIN2	AUXFANIN1	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFANOUT2.** “1” indicates that AUXFANOUT2 works for three minutes at the full fan speed.
6	**AUXFANOUT1.** “1” indicates that AUXFANOUT1 works for three minutes at the full fan speed.
5	**AUXFANIN2. A one indicates the fan count limit of AUXFANIN2 has been exceeded.**
4	**AUXFANIN1. A one indicates the fan count limit of AUXFANIN1 has been exceeded.**
2-3	**Reserved.**
1	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.
0	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.

9.228 SMI# Mask Register 4 – Index 51h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	TAR5	TAR4	TAR3	RESERVED		SMSKVBAT	SMSKVSB
DEFAULT	0	1	1	1	0	0	1	1

BIT	DESCRIPTION
7	**Reserved.**
6	**TAR5.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
5	**TAR4.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
4	**TAR3.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 45h (Bank 0))
3-2	**Reserved.**
1	**SMSKVBAT.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
0	**SMSKVSB.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))

9.229 Reserved Register – Index 52h ~ 53h (Bank 4)

9.230 SYSTIN Temperature Sensor Offset Register – Index 54h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.231 CPUTIN Temperature Sensor Offset Register – Index 55h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the

BIT	DESCRIPTION
	monitored value so that the read value is the sum of the monitored value and this offset value.

9.232 AUXTIN0 Temperature Sensor Offset Register – Index 56h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN0 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.233 Reserved Register – Index 57h-58h (Bank 4)

9.234 Real Time Hardware Status Register I – Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN _STS	SYSFANIN _STS	CPUTIN _STS	SYSTIN _STS	3VCC _STS	AVCC _STS	VIN1 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN_STS. CPUFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**SYSFANIN_STS. SYSFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
5	**CPUTIN_STS. CPUTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	**SYSTIN_STS. SYSTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	**3VCC_STS. 3VCC Voltage Status.** 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	**AVCC_STS. AVCC Voltage Status.** 1: AVCC voltage is over or under the allowed range.

BIT	DESCRIPTION
	0: AVCC voltage is in the allowed range.
1	**VIN1_STS. VIN1 Voltage Status.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.
0	**CPUVCORE_STS. CPUVCORE Voltage Status.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

9.235 Real Time Hardware Status Register II – Index 5Ah (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2 _STS	TAR1 _STS	AUXTIN _STS	CASEOPEN0 _STS	AUXFANIN0 _STS	AUXFANIN1 _STS	CASEOPEN1 _STS	VIN0 _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN Warning Status.** 1: Selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN^{TM} IV. 0: Selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN^{TM} IV. 0: SYSTIN temperature has not reached the warning range.
5	**AUXTIN_STS. AUXTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	**CASEOPEN0_STS. CaseOpen Status.** 1: Caseopen is detected and latched. 0: Caseopen is not latched.
3	**AUXFANIN0_STS. AUXFANIN0 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
2	**AUXFANIN1_STS. AUXFANIN1 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	**CASEOPEN1_STS. CaseOpen Status.** 1: Caseopen is detected and latched. 0: Caseopen is not latched.
0	**VIN0_STS. VIN0 Voltage Status.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.

9.236 Real Time Hardware Status Register III – Index 5Bh (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 _STS	TAR5 _STS	VCOREREFIN _STS	VIN4 _STS	TAR4 _STS	TAR3 _STS	VBAT _STS	VSB _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFANIN1_STS. AUXFANIN2 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**TAR5_STS. Smart Fan of AUXFANIN2 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
5	**VCOREREFIN_STS. VCOREREFIN Voltage Status.** 1: VCOREREFIN Voltage is over or under the allowed range. 0: VCOREREFIN Voltage is in the allowed range.
4	**VIN4_STS. VIN4 Voltage Status.** 1: VIN4 voltage is over or under the allowed range. 0: VIN4 voltage is in the allowed range.
3	**TAR4_STS. Smart Fan of AUXFANIN1 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
2	**TAR3_STS. Smart Fan of AUXFANIN0 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
1	**VBAT_STS. VBAT Voltage Status.** 1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	**VSB_STS. 3VSB Voltage Status.** 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.237 Reserved Register – Index 5Ch ~ 5Fh (Bank 4)

9.238 Is<8:1> Current Register – Index 60h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Is<8:1>							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Is<8:1>.** Current measure by current measure IC (1LSB=31.25mA)

9.239 Is<0> Current Register – Index 61h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**							**Is<0>**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**Is<0>.** Current measure by current measure IC (1LSB=31.25mA)

9.240 POWER <9:2> Register – Index 62h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**POWER <9:2>**							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER <9:2>.** Power calculate by IO (1LSB=0.25W)

9.241 POWER<1:0> Register – Index 63h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**						**POWER<1:0>**	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
1:0	**POWER<1:0>.** Power calculate by IO (1LSB=0.25W)

9.242 VIN Register – Index 64h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN.** Power voltage given by customer. (1LSB=128mV)

9.243 Rreg Setting Register – Index 65h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Rreg							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Rreg.** Equivalent electric impedance in order to calculate Is. (1LSB=1m ohm)

9.244 Reg_Ratio_K and POWER_Voltage Enable Register – Index 66h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reg_Ration_K				Reserved			Power_ Volt_En
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**Reg_Ration_K:** The ration in order to make power voltage input to IO is below 2.048. Reg_Ration_K=(R1+R2)/(R1)
3-1	**Reserved**
0	**Power_Volt_En** 0:Power voltage is monitored by IO 1:Power voltage is given by customer

9.245 POWER_V Register – Index 67h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	POWER_V							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER_V:** Power voltage (1LSB=128mV)

9.246 Reserved Register – Index 68h ~ 7Fh (Bank 4)

9.247 Value RAM — Index 80h ~ 96h (Bank 4)

ADDRESS A6-A0	DESCRIPTION
80h	CPUVCORE reading
81h	VIN1 reading
82h	AVCC reading
83h	3VCC reading
84h	VIN0 reading
85h	VCOREREFIN reading
86h	VIN4 reading
87h	3VSB reading
88h	VBAT reading
89h	VTT reading
8Ah	VIN5 reading
8Bh	VIN6 reading
8Ch	VIN2 reading
8Dh	VIN3 reading
8Eh	VIN7 reading
8Fh	Reserved
90h	SYSTIN temperature reading
91h	CPUTIN temperature reading
92h	AUXTIN0 temperature reading
93h	AUXTIN1 temperature reading
94h	AUXTIN2 temperature reading
95h	AUXTIN3 temperature reading

9.248 (SYSFANIN) FANIN1 COUNT High-byte Register – Index B0h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT1 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION

7-0	**FANCNT1_H:** 13-bit SYSFANIN Fan Count, High Byte

9.249 (SYSFANIN) FANIN1 COUNT Low-byte Register – Index B1h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT1 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT1_L:** 13-bit SYSFANIN Fan Count, Low Byte

9.250 (CPUFANIN) FANIN2 COUNT High-byte Register – Index B2h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT2 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT2_H:** 13-bit CPUFANIN Fan Count, High Byte

9.251 (CPUFANIN) FANIN2 COUNT Low-byte Register – Index B3h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT2 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT2_L:** 13-bit CPUFANIN Fan Count, Low Byte

9.252 (AUXFANIN0) FANIN3 COUNT High-byte Register – Index B4h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT3 [12:5]							

DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT3_H:** 13-bit AUXFANIN0 Fan Count, High Byte

9.253 (AUXFANIN0) FANIN3 COUNT Low-byte Register – Index B5h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**RESERVED**			**FANCNT3 [4:0]**				
DEFAULT	0			**1F**				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT3_L:** 13-bit AUXFANIN0 Fan Count, Low Byte

9.254 (AUXFANIN1) FANIN4 COUNT High-byte Register – Index B6h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**FANCNT4 [12:5]**							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT4_H:** 13-bit AUXFANIN0 Fan Count, High Byte

9.255 (AUXFANIN1) FANIN4 COUNT Low-byte Register – Index B7h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**RESERVED**			**FANCNT4 [4:0]**				
DEFAULT	0			**1F**				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT4_L:** 13-bit AUXFANIN0 Fan Count, Low Byte

9.256 (AUXFANIN2) FANIN5 COUNT High-byte Register – Index B8h (Bank 4)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT5 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT5_H:** 13-bit AUXFANIN2 Fan Count, High Byte

9.257 (AUXFANIN2) FANIN5 COUNT Low-byte Register – Index B9h (Bank 4)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT5 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT5_L:** 13-bit AUXFANIN2 Fan Count, Low Byte

9.258 Reserved Register – Index BAh ~ BFh (Bank 4)

9.259 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index C0h (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED HIGH-BYTE VALUE.**

9.260 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index C1h (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED LOW-BYTE VALUE.**

9.261 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) – Index C2h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN SPEED HIGH-BYTE VALUE.**

9.262 CPUFANIN SPEED LOW-BYTE VALUE (RPM) – Index C3h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN SPEED LOW-BYTE VALUE.**

9.263 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) – Index C4h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED HIGH-BYTE VALUE.**

9.264 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) – Index C5h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED LOW-BYTE VALUE.**

9.265 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) – Index C6h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIIN1 SPEED HIGH-BYTE VALUE.**

9.266 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) – Index C7h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN1 SPEED LOW-BYTE VALUE.**

9.267 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) – Index C8h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIIN2 SPEED HIGH-BYTE VALUE.**

9.268 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) – Index C9h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED LOW-BYTE VALUE							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN2 SPEED LOW-BYTE VALUE.**

9.269 Reserved Register – Index 00h ~ 53h (Bank 5)

9.270 Value RAM 2 — Index 50h-5Fh (Bank 5)

ADDRESS A6-A0	DESCRIPTION
54h	**3VSB High Limit**
55h	**3VSB Low Limit**
56h	**VBAT High Limit**
57h	**VBAT Low Limit**
58h	**VTT High Limit**
59h	**VTT Low Limit**
5Ah	**VIN5 High Limit**
5Bh	**VIN5 Low Limit**
5Ch	**VIN6 High Limit**
5Dh	**VIN6 Low Limit**
5Eh	**VIN2 High Limit**
5Fh	**VIN2 Low Limit**
60h	**VIN3 High Limit**
61h	**VIN3 Low Limit**
62h	**VIN7 High Limit**
63h	**VIN7 Low Limit**

9.271 SMI# Mask Register 1 – Index 66h (Bank 5)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**VIN7**	**VIN3**	**VIN2**	**VIN6**	**VIN5**	**VTT**
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**Reserved**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**Reserved**	
5	**VIN7**	
4	**VIN3**	
3	**VIN2**	

BIT	DESCRIPTION	
2	VIN6	
1	VIN5	
0	VTT	

9.272 Interrupt Status Register – Index 67h (Bank 5)

Attribute: Read Clear
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	VIN7	VIN3	VIN2	VIN6	VIN5	VTT
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Reserved.**
5	**VIN7.** A one indicates the high or low limit of VIN7 has been exceeded.
4	**VIN3.** A one indicates the high or low limit of VIN3 has been exceeded.
3	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded.
2	**VIN6.** A one indicates the high or low limit of VIN6 has been exceeded.
1	**VIN5.** A one indicates the high or low limit of VIN5 has been exceeded.
0	**VTT.** A one indicates the high or low limit of VTT has been exceeded.

9.273 Real Time Hardware Status Register – Index 68h (Bank 5)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	VIN7 _STS	VIN3 _STS	VIN2 _STS	VIN6 _STS	VIN5 _STS	VTT _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	**VIN7_STS. VIN7 Voltage Status.** 1: VIN7 voltage is over or under the allowed range. 0: VIN7 voltage is in the allowed range.
4	**VIN3_STS. VIN3 Voltage Status.** 1: VIN3 voltage is over or under the allowed range. 0: VIN3 voltage is in the allowed range.
3	**VIN2_STS. VIN2 Voltage Status.** 1: VIN2 voltage is over or under the allowed range.

BIT	DESCRIPTION
	0: VIN2 voltage is in the allowed range.
2	**VIN6_STS. VIN6 Voltage Status.** 1: VIN6 voltage is over or under the allowed range. 0: VIN6 voltage is in the allowed range.
1	**VIN5_STS. VIN5 Voltage Status.** 1: VIN5 voltage is over or under the allowed range. 0: VIN5 voltage is in the allowed range.
0	**VTT_STS. VTT Voltage Status.** 1: VTT voltage is over or under the allowed range. 0: VTT voltage is in the allowed range.

9.274 Reserved Register – Index 69h ~ FFh (Bank 5)

9.275 Close-Loop Fan Control RPM mode Register – Index 00 (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			En_AUX2_RPM	En_AUX1_RPM	En_AUX0_RPM	En_CPU_RPM	En_SYS_RPM
DEFAULT	0			0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED**
4	**En_AUX2_RPM** 0: Disable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode.
3	**En_AUX1_RPM** 0: Disable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode.
2	**En_AUX0_RPM** 0: Disable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode.
1	**En_CPU_RPM** 0: Disable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode.
0	**En_SYS_RPM** 0: Disable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN^{TM} IV Close Loop Fan Control RPM Mode.

9.276 SYSFAN RPM Mode Tolerance Register – Index 01 (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ SYS_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit0）, unit is 100 RPM.

9.277 CPUFAN RPM Mode Tolerance Register – Index 02 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ CPU_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit1）, unit is 100 RPM.

9.278 AUXFAN0 RPM Mode Tolerance Register – Index 03 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX0_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit2）, unit is 100 RPM.

9.279 AUXFAN1 RPM Mode Tolerance Register – Index 04 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX1_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit3）, unit is 100 RPM.

9.280 AUXFAN2 RPM Mode Tolerance Register – Index 05 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX2_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit4）, unit is 100 RPM.

9.281 Enable RPM High Mode Register – Index 00 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			En_AUX2_RPM_HIGH	En_AUX1_RPM_HIGH	En_AUX0_RPM_HIGH	En_CPU_RPM_HIGH	En_SYS_RPM_HIGH
DEFAULT	0			0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED**
4	**En_AUX2_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
3	**En_AUX1_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
2	**En_AUX0_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan,

	0: Disable 1: Enable
1	**En_CPU_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
0	**En_SYS_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable

9.282 SMIOVT1 Temperature Source Select Register – Index 21 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC1				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT1 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source.

	1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.283 SMIOVT2 Temperature Source Select Register – Index 22 (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC2				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT2 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.284 Reserved Register – Index 23~39h (Bank 6)

9.285 (SYSFANIN) Fan Count Limit High-byte Register – Index 3Ah (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN1_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, High Byte

9.286 (SYSFANIN) Fan Count Limit Low-byte Register – Index 3Bh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN1_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, Low Byte

9.287 (CPUFANIN) Fan Count Limit High-byte Register – Index 3Ch (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN2_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, High Byte

9.288 (CPUFANIN) Fan Count Limit Low-byte Register – Index 3Dh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN2_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, Low Byte

9.289 (AUXFANIN0) Fan Count Limit High-byte Register – Index 3Eh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN3_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, High Byte

9.290 (AUXFANIN0) Fan Count Limit Low-byte Register – Index 3Fh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN3_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, Low Byte

9.291 (AUXFANIN1) Fan Count Limit High-byte Register – Index 40h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN4_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, High Byte

9.292 (AUXFANIN1) Fan Count Limit Low-byte Register – Index 41h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	RESERVED	FANIN4_HL [4:0]
DEFAULT	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, Low Byte

9.293 (AUXFANIN2) Fan Count Limit High-byte Register – Index 42h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN5_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, High Byte

9.294 (AUXFANIN2) Fan Count Limit Low-byte Register – Index 43h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN5_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, Low Byte

9.295 SYSFANIN Revolution Pulses Selection Register – Index 44h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan1_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**SYSFANIN Revolution Pulses Selection** = 00, four pulses per revolution.

	= 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.296 CPUFANIN Revolution Pulses Selection Register – Index 45h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan2_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**CPUFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.297 AUXFANIN0 Revolution Pulses Selection Register – Index 46h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan3_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN0 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.298 AUXFANIN1 Revolution Pulses Selection Register – Index 47h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan4_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN1 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.299 AUXFANIN2 Revolution Pulses Selection Register – Index 48h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan5_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN2 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.300 Reserved Register – Index 49~FFh (Bank 6)

9.301 PECI Function Control Registers – Index 01 ~ 04h (Bank 7)

9.302 PECI Enable Function Register – Index 01h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI_En	Reserved				Is_PECI30	Manual_En	Routine_En
DEFAULT	0	0	0	1	0	1	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECI Function. (**PECI_En**)
6 ~ 3	R / W	Reserved
2	R / W	Enable PECI 3.0 Command function (**Is_PECI30**)
1	R / W	Enable PECI 3.0 Manual Function (**Manual_En**) (**One-shot clear**)
0	R / W	Enable PECI 3.0 Routine Function (**Routine_En**)

9.303 PECI Timing Config Register – Index 02h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TN_Extend		Adj[2:0]			PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserve
5	R / W	**TN_Extend[1:0]** Adjust Transaction Rate. 00_{BIN} = 1.5 MHz (Default) 01_{BIN} = 750 KHz 10_{BIN} = 375 KHz 11_{BIN} = 187.5 KHz
4	R / W	
3	R / W	**Adj[2:0]** Compensate the effect of rising time on physical bus Default Value = 001
2	R / W	
1	R / W	
0	R / W	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

9.304 PECI Agent Config Register – Index 03h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		En_Agt[1:0]		Reserved		Domain1_Agt1	Domain1_Agt0
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserved
5	R / W	**En_Agt[1:0] Enable Agent** 00 = Disable Agent. 01= Enable Agent0. 10 = Reserved. 11 = Enable Agent0 and Agent1.
4	R / W	
3 ~ 2	R / W	Reserved

BIT	READ / WRITE	DESCRIPTION
1	R / W	Enable domain 1 for Agent1 0 = Agent1 without domain1 1 = Agent1 with domain 1
0	R / W	Enable domain 1 for Agent0 0 = Agent0 without domain 1 1 = Agent0 with domain 1

9.305 PECI Temperature Config Register – Index 04h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Virtual_En	Reserved		Clamp	Reserved	RtDmn_Agt[1:0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Virtual Temp Function Enable.(**Virtual_En)** When enable this function, the temperature raw data can use LPC to write raw data to CR 17_{HEX} ~ CR $1E_{HEX}$
6 ~ 5	R / W	Reserved
4	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(**Clamp**)
3	R / W	Reserved
2	R / W	**RtDmn_Agt[1:0]** Agent 1 – Agent 0 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
1	R / W	
0	R / W	Return High Temperature of doamin0 or domain1.(**RtHigher**) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04_{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.306 PECI Command Write Date Registers – Index 05 ~ 1Eh (Bank 7)

9.307 PECI Command Address Register – Index 05h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Address							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.308 PECI Command Write Length Register – Index 06h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Write Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.309 PECI Command Read Length Register – Index 07h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Read Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.310 PECI Command Code Register – Index 08h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Code							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.311 PECI Command Tbase0 Register – Index 09h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 0						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.312 PECI Command Tbase1 Register – Index 0Ah (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 1						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.313 PECI Command Write Data 1 Register – Index 0Bh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.314 PECI Command Write Data 2 Register – Index 0Ch (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.315 PECI Command Write Data 3 Register – Index 0Dh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.316 PECI Command Write Data 4 Register – Index 0Eh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.317 PECI Command Write Data 5 Register – Index 0Fh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.318 PECI Command Write Data 6 Register – Index 10h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.319 PECI Command Write Data 7 Register – Index 11h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.320 PECI Command Write Data 8 Register – Index 12h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.321 PECI Command Write Data 9 Register – Index 13h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.322 PECI Command Write Data 10 Register – Index 14h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.323 PECI Command Write Data 11 Register – Index 15h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.324 PECI Command Write Data 12 Register – Index 16h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.325 PECI Agent Relative Temperature Register (ARTR) – Index 17h-1Eh (Bank 7)

These registers return the **"raw data"** retrieved from PECI GetTemp() command. These data could be the error codes (range: 8000H~81FFH) or relative temperatures to process the defined Tbase. The error code will only be update in **ARTR**; while "Temperature Reading Register", Bank7 Index 20h and 21h, will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is $8001_{HEX,}$ in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read / Write(When Virtual_En enable)

ADDRESS 17-1E	DESCRIPTION

ADDRESS 17-1E	DESCRIPTION
17h[15:8],18h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
19h[15:8],1Ah[7:0]	Domain1 Relative Temperature Agent0 [15:0]
1Bh[15:8],1Ch[7:0]	Domain0 Relative Temperature Agent1 [15:0]
1Dh[15:8],1Eh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECI Temperature format

Error Code	Description	Host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127℃ back to the temperature readouts.
8004_{HEX}	Reserved.	No further operation.

$81FF_{HEX}$		

9.326 PECI Command Read Date Registers – Index 1F ~ 32h (Bank 7)

9.327 PECI Alive Agent Register – Index 1Fh (Bank 7)

Attribute: Read only
Size: 8 bits
Record which agentis able to respond to Ping().**Default value is 00_{HEX}.**
1: agent is able to respond to Ping() command. Agent alive
0: agent isn't able to respond to Ping() command. Agent is not alive

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Alive Agent	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~2	Reserve
1	1: agent1 is able to respond to Ping() command. Agent alive 0: agent1 isn't able to respond to Ping() command. Agent is not alive
0	1: agent0 is able to respond to Ping() command. Agent alive 0: agent0 isn't able to respond to Ping() command. Agent is not alive

9.328 PECI Temperature Reading Register (Integer) – Index 20h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Temperature Reading---Integer [9:2]							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7~0	**Temperature value [9] (Sign bit)** **Temperature value [8:2] (Integer bits)** Temperature value [1:0] (Fraction bits)

Note. Temperature reading register is count from raw data and Tbase, for example:

Raw data	+	*Tbase*	=	*Temp Reading*
Bank7, Index [17][18]	**+**	**Bank7, Index [09]**	**=**	**Bank7, Index [20][21]**

9.329 PECI Temperature Reading Register (Fraction) – Index 21h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Temperature Vaule[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Temperature value [9] (Sign bit) Temperature value [8:2] (Integer bits) **Temperature value [1:0] (Fraction bits)**

9.330 PECI Command TN Count Value Register – Index 22h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Timing Negotiation count Value[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.331 PECI Command TN Count Value Register – Index 23h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				PECI Timing Negotiation count Value[11:8]			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.332 PECI Command Warning Flag Register – Index 24h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						Alert Value[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
1~0	**Agent Alert Bit** (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions. **Default value is 00_{HEX}.**

9.333 PECI Command FCS Data Register – Index 25h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserve		Wraning	CC_Fail	ZeroWFCS	AbortWFCS	BadRFCS	BadWFCS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
5~0	Retrieve PECI related data from client and host. **Default value is 00_{HEX}.**

9.334 PECI Command WFCS Data Register – Index 26h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI WFCS related data from client. **Default value is 00_{HEX}.**

9.335 PECI RFCS Data Register – Index 27h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PECI RFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. **Default value is 00_{HEX}.**

9.336 PECI AWFCS Data Register – Index 28h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI AWFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PCI related data from client. **Default value is 00_{HEX}.**

9.337 PECI CRC OUT WFCS Data Register – Index 29h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI CRC OUT WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. **Default value is 00_{HEX}.**

9.338 PECI Command Read Data 1 Register – Index 2Ah (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.339 PECI Command Read Data 2 Register – Index 2Bh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.340 PECI Command Read Data 3 Register – Index 2Ch (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.341 PECI Command Read Data 4 Register – Index 2Dh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.342 PECI Command Read Data 5 Register – Index 2Eh (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.343 PECI Command Read Data 6 Register – Index 2Fh (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.344 PECI Command Read Data 7 Register – Index 30h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.345 PECI Command Read Data 8 Register – Index 31h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.346 PECI Command Read Data 9 Register – Index 32h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

PECI Manual Command Address Table

Command Bank 7	Address CR 05_{HEX}	WriteLength CR 06_{HEX}	Read Length CR 07_{HEX}	Command Code CR 08_{HEX}
Ping	Addr	00	00	
GetDIB		01	08	F7
GetTemp		01	02	01
PCIRd30		06	02 / 03 / 05	61
PCIWr30		08 / 09 / 0B	01	65
PCIRdLocal30		05	02 / 03 / 05	E1
PCIWrLocal30		07 / 08 / 0A	01	E5
PKGRd30		05	02 / 03 / 05	A1
PKGWr30		07 / 08 / 0A	01	A5
IAMSRRd30		05	02 / 03 / 05 / 09	B1
IAMSRWr30		07 / 08 / 0A / 0E	01	B5

PECI Manual Command Read Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30	GetDIB	GetTemp
Command Code	61	65	E1	E5	A1	A5	B1	B5	F7	01
RdData 1 CR $2A_{HEX}$	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	X	X
RdData 2 CR $2B_{HEX}$	X	X	X	X	X	X	Data LSB_1	X	Device Info	X
RdData 3	X	X	X	X	X	X	Data	X	Revision	X

CR 2C$_{HEX}$							LSB_2		Number	
RdData 4 CR 2D$_{HEX}$	X	X	X	X	X	X	Data LSB_3	X	Reserved 1	X
RdData 5 CR 2E$_{HEX}$	X	X	x	X	X	X	Data LSB_4	X	Reserved 2	X
RdData 6 CR 2F$_{HEX}$	Data LSB_1	X	Data LSB_1	X	Data LSB_1	X	Data LSB_5	X	Reserved 3	X
RdData 7 CR 30$_{HEX}$	Data LSB_2	X	Data LSB_2	X	Data LSB_2	X	Data LSB_6	X	Reserved 4	X
RdData 8 CR 31$_{HEX}$	Data LSB_3	X	Data LSB_3	X	Data LSB_3	X	Data LSB_7	X	Reserved 5	Temp_LB
RdData 9 CR 32$_{HEX}$	Data MSB	x	Data MSB	X	Data MSB	X	Data MSB	X	Reserved 6	Temp_HB

PECI Manual Command Write Data Table

Command	**PCI Rd30**	**PCI Wr30**	**PCIRd Local30**	**PCIWr Local30**	**PKG Rd30**	**PKG Wr30**	**IAMSR Rd30**	**IAMSR Wr30**
Command Code	**61**	**65**	**E1**	**E5**	**A1**	**A5**	**B1**	**B5**
WrData 1 CR 0B$_{HEX}$	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID
WrData 2 CR 0C$_{HEX}$	Addr LSB_1	Addr LSB_1	Addr LSB_1	Addr LSB_1	Index	Index	Process or ID	Process or ID
WrData 3	Addr	Addr	Addr	Addr	Param	Param	Addr	Addr

CR 0D$_{HEX}$	LSB_2	LSB_2	LSB_2	LSB_2	LSB	LSB	LSB	LSB
WrData 4 CR 0E$_{HEX}$	Addr LSB_3	Addr LSB_3	Addr MSB	Addr MSB	Param MSB	Param MSB	Addr MSB	Addr MSB
WrData 5 CR 0F$_{HEX}$	Addr MSB	Addr MSB	X	Data LSB_1	X	Data LSB_1	X	Data LSB_1
WrData 6 CR 10$_{HEX}$	X	Data LSB_1	X	Data LSB_2	X	Data LSB_2	X	Data LSB_2
WrData 7 CR 11$_{HEX}$	X	Data LSB_2	X	Data LSB_3	X	Data LSB_3	X	Data LSB_3
WrData 8 CR 12$_{HEX}$	X	Data LSB_3	X	Data MSB	X	Data MSB	X	Data LSB_4
WrData 9 CR 13$_{HEX}$	X	Data MSB	X	X	X	X	X	Data LSB_5
WrData10 CR 14$_{HEX}$	X	X	X	X	X	X	X	Data LSB_6
WrData11 CR 15$_{HEX}$	X	X	X	X	X	X	X	Data LSB_7
WrData12 CR 16$_{HEX}$	X	X	X	X	X	X	X	Data MSB

9.347 AUXFAN1 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN1 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT1 Stop Value (Bank8, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN1 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN1 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN1 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN1 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN1 monitoring source.

BIT	DESCRIPTION
	0 0 1 0 1: Select **AUXTIN2** as AUXFAN1 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN1 monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN1 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as AUXFAN1 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as AUXFAN1 monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as AUXFAN1 monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as AUXFAN1 monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as AUXFAN1 monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as AUXFAN1 monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN1 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN1 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN1 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN1 monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as AUXFAN1 monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as AUXFAN1 monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as AUXFAN1 monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as AUXFAN1 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as AUXFAN1 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.348 AUXFAN1 Target Temperature Register / AUXFANIN1 Target Speed_L Register – Index 01h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN1 Target Temperature / AUXFANIN1 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN1 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN1 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.349 AUXFAN1 MODE Register / AUXFAN1 TOLERRANCE Register – Index 02h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 MODE				Reseved	Tolerance of		

						AUXFAN1 Target Temperature or AUXFANIN1 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT1 Mode Select.** 0000: **AUXFANOUT1** is in Manual Mode. **(Default)** 0001: **AUXFANOUT1** is in Thermal Cruise Mode. 0010: **AUXFANOUT1** is as Speed Cruise Mode. 0100: **AUXFANOUT1** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN1 Target Temperature or AUXFANIN1 Target Speed_L.

9.350 AUXFANOUT1 Step Up Time Register – Index 03h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Value Step Up Time**							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT1 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.351 AUXFANOUT1 Step Down Time Register – Index 04h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Value Step Down Time**							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT1 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.352 AUXFANOUT1 Stop Value Register – Index 05h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Stop Value**							

DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT1 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.353 AUXFANOUT1 Start-up Value Register – Index 06h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Start-Up Value**							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT1 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.354 AUXFANOUT1 Stop Time Register – Index 07h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Value Stop Time**							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT1 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.355 Reserved Register – Index 08h (Bank 8)

9.356 AUXFANOUT1 Output Value Select Register – Index 09h (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Value**							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E3h] is the Default Speed Configuration Register of AUXFANOUT1.

FUNCTION MODE		**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

PWM Output	**DESCRIPTION**	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.

9.357 AUXFANIN1 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN1 TOL_H			AUXFANIN1 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN1 Tolerance_H [5:3]
3-0	AUXFANIN1 Target Speed_H [11:8]

9.358 Reserved Register – Index 0Dh (Bank 8)

9.359 SMART FAN IV AUXFANOUT1 STEP Register – Index 20h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUXFANOUT1_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUXFANOUT1_STEP** 0: Disable SMART FAN IV has Stepping AUXFANOUT1. (default) 1: Enable SMART FAN IV has Stepping AUXFANOUT1.

9.360 AUXFAN1 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 1 Register (T1).

9.361 AUXFAN1 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 2 Register (T2).

9.362 AUXFAN1 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 3 Register (T3).

9.363 AUXFAN1 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 4 Register (T4).

9.364 Reserved Register – Index 25h~26h (Bank 8)

9.365 AUXFAN1 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 1 Register.

9.366 AUXFAN1 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 2 Register.

9.367 AUXFAN1 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 3 Register.

9.368 AUXFAN1 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 4 Register.

9.369 Reserved Register – Index Index 2Bh~30h (Bank 8)

9.370 AUXFAN1 3-Wire Enable Register – Index 31h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	Reserved		EN_AUX1_3WFAN
DEFAULT	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX1_3WFAN (AUXFAN1 type setting)** 0: 4-wire fan 1: 3-wire fan

9.371 Reserved Register – Index 32h~34h(Bank 8)

9.372 AUXFAN1 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Critical Temperature Register

9.373 AUXFAN1 Enable Critical Duty – Index 36h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX1_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX1_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for AUXFANOUT1. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT1.

9.374 AUXFAN1 Critical Duty Register – Index 37h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Critical Duty							

DEFAULT	CC

BIT	DESCRIPTION
7-0	AUXFAN1 Critical Duty.

9.375 AUXFANOUT1 Critical Temperature Tolerance Register – Index 38h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT1 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT1 Critical Temperature Tolerance**

9.376 Weight value Configuration Register – Index 39h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_AUXFAN1_WEIGHT	Reserved		AUX1_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_AUXFAN1_WEIGHT.** 0: Disable Weight Value Control for AUXFAN1. 1: Enable Weight Value Control for AUXFAN1.
6-5	**Reserved**
4-0	**AUXFAN1 Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN1 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN1 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN1 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN1 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN1 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN1 monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN1 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as AUXFAN1 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as AUXFAN1 monitoring source.

BIT	DESCRIPTION
	0 1 1 0 0: Select **SMBUSMASTER 4** as AUXFAN1 monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as AUXFAN1 monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as AUXFAN1 monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as AUXFAN1 monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN1 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN1 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN1 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN1 monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as AUXFAN1 monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as AUXFAN1 monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as AUXFAN1 monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as AUXFAN1 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as AUXFAN1 monitoring source.

9.377 AUXFANOUT1 Temperature Step Register – Index 3Ah (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Temperature Step (AUX1_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT1 Temperature Step**

9.378 AUXFANOUT1 Temperature Step Tolerance Register – Index 3Bh (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Temperature Step Tolerance (AUX1_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT1 Temperature Step Tolerance**

9.379 AUXFANOUT1 Weight Step Register – Index 3Ch (Bank 8)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Weight Step (AUX1_WEIGHT_STEP)							

DEFAULT	0

BIT	DESCRIPTION
7-0	**AUXFANOUT1 Weight Step**

9.380 AUXFANOUT1 Temperature Base Register – Index 3Dh (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Temperature Base (AUX1_TEMP_BASE)**							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT1 Temperature Base**

9.381 AUXFANOUT1 Temperature Fan Duty Base Register – Index 3Eh (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT1 Temperature Base (AUX1_FC_BASE)**							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT1 Start point of Fan Duty increasing**

9.382 AUXFAN1 PECIERR DUTY Enable Register – Index 3Fh (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**						**EN_AUX1_PECIERR_DUTY**	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_AUX1_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT1** Value for AUXFANOUT1. 10,11: Keep Full Speed

9.383 Reserved Register – Index 40h (Bank 8)

9.384 AUXFANOUT1 Pre-Configured Register For PECI Error – Index 41h (Bank 8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 pre-configured register for PECI error (PECI_ERR_AUXOUT1)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT1 pre-configured register for PECI error.**

9.385 Reserved Register – Index 42h ~ FFh (Bank 8)

9.386 AUXFAN2 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN2 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT2 Stop Value (Bank9, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN2 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN2 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN2 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN2 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN2 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN2 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN2 monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN2 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as AUXFAN2 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as AUXFAN2 monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as AUXFAN2 monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as AUXFAN2 monitoring source.

BIT	DESCRIPTION
	0 1 1 1 0: Select **SMBUSMASTER 6** as AUXFAN2 monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as AUXFAN2 monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN2 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN2 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN2 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN2 monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as AUXFAN2 monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as AUXFAN2 monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as AUXFAN2 monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as AUXFAN2 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as AUXFAN2 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.387 AUXFAN2 Target Temperature Register / AUXFANIN2 Target Speed_L Register – Index 01h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXTIN2 Target Temperature / AUXFANIN2 Target Speed_L**							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN2 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN2 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.388 AUXFAN2 MODE Register / AUXFAN2 TOLERRANCE Register – Index 02h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFAN2 MODE**				**Reseved**	**Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L**		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

7-4	**AUXFANOUT2 Mode Select.** 0000: **AUXFANOUT2** is in Manual Mode. **(Default)** 0001: **AUXFANOUT2** is in Thermal Cruise Mode. 0010: **AUXFANOUT2** is as Speed Cruise Mode. 0100: **AUXFANOUT2** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L.

9.389 AUXFANOUT2 Step Up Time Register – Index 03h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.390 AUXFANOUT2 Step Down Time Register – Index 04h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.391 AUXFANOUT2 Stop Value Register – Index 05h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT2 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.392 AUXFANOUT2 Start-up Value Register – Index 06h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT2 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.393 AUXFANOUT2 Stop Time Register – Index 07h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT2 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.394 Reserved Register – Index 08h (Bank 9)

9.395 AUXFANOUT2 Output Value Select Register – Index 09h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E4h] is the Default Speed Configuration Register of AUXFANOUT2.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.396 AUXFANIN2 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN2 TOL_H			AUXFANIN2 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN2 Tolerance_H [5:3]
3-0	AUXFANIN2 Target Speed_H [11:8]

9.397 Reserved Register – Index 0Dh (Bank 9)

9.398 SMART FAN IV AUXFANOUT2 STEP Register – Index 20h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUXFANOUT2_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUXFANOUT2_STEP** 0: Disable SMART FAN IV has Stepping AUXFANOUT2. (default) 1: Enable SMART FAN IV has Stepping AUXFANOUT2.

9.399 AUXFAN2 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 1 Register (T1).

9.400 AUXFAN2 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN^{TM} IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN^{TM} IV) Temperature 2 Register (T2).

9.401 AUXFAN2 (SMART FAN^{TM} IV) Temperature 3 Register(T3) – Index 23h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2(SMART FAN^{TM} IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN^{TM} IV) Temperature 3 Register (T3).

9.402 AUXFAN2 (SMART FAN^{TM} IV) Temperature 4 Register(T4) – Index 24h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN^{TM} IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN^{TM} IV) Temperature 4 Register (T4).

9.403 Reserved Register – Index 25h~26h (Bank 9)

9.404 AUXFAN2 (SMART FAN^{TM} IV) PWM 1 Register – Index 27h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN^{TM} IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN^{TM} IV) PWM 1 Register.

9.405 AUXFAN2 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 2 Register.

9.406 AUXFAN2 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 3 Register.

9.407 AUXFAN2 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 4 Register.

9.408 Reserved Register – Index Index 2Bh~30h (Bank 9)

9.409 AUXFAN2 3-Wire Enable Register – Index 31h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX2_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX2_3WFAN (AUXFAN2 type setting)** 0: 4-wire fan 1: 3-wire fan

9.410 Reserved Register – Index 32h~34h(Bank 9)

9.411 AUXFAN2 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Critical Temperature Register

9.412 AUXFAN2 Enable Critical Duty – Index 36h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX2_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX2_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for AUXFANOUT2. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT2.

9.413 AUXFAN2 Critical Duty Register – Index 37h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN2 Critical Duty.

9.414 AUXFANOUT2 Critical Temperature Tolerance Register – Index 38h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT2 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT2 Critical Temperature Tolerance**

9.415 Weight value Configuration Register – Index 39h (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_AUXFAN2_WEIGHT	Reserved		AUX2_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_AUXFAN2_WEIGHT.** 0: Disable Weight Value Control for AUXFAN2. 1: Enable Weight Value Control for AUXFAN2.
6-5	**Reserved**
4-0	**AUXFAN2 Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN2 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN2 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN2 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN2 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN2 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN2 monitoring source. 0 0 1 1 1: Reserved. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN2 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as AUXFAN2 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as AUXFAN2 monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as AUXFAN2 monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as AUXFAN2 monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as AUXFAN2 monitoring source.

BIT	DESCRIPTION
	0 1 1 1 1: Select **SMBUSMASTER 7** as AUXFAN2 monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN2 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN2 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN2 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN2 monitoring source. 1 0 1 1 0: Select **PCH_DIM0_TEMP** as AUXFAN2 monitoring source. 1 0 1 1 1: Select **PCH_DIM1_TEMP** as AUXFAN2 monitoring source. 1 1 0 0 0: Select **PCH_DIM2_TEMP** as AUXFAN2 monitoring source. 1 1 0 0 1: Select **PCH_DIM3_TEMP** as AUXFAN2 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP** as AUXFAN2 monitoring source.

9.416 AUXFANOUT2 Temperature Step Register – Index 3Ah (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Temperature Step (AUX2_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT2 Temperature Step**

9.417 AUXFANOUT2 Temperature Step Tolerance Register – Index 3Bh (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Temperature Step Tolerance (AUX2_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT2 Temperature Step Tolerance**

9.418 AUXFANOUT2 Weight Step Register – Index 3Ch (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Weight Step (AUX2_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT2 Weight Step**

9.419 AUXFANOUT2 Temperature Base Register – Index 3Dh (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Temperature Base (AUX2_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT2 Temperature Base**

9.420 AUXFANOUT2 Temperature Fan Duty Base Register – Index 3Eh (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Temperature Base (AUX2_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT2 Start point of Fan Duty increasing**

9.421 AUXFAN2 PECIERR DUTY Enable Register – Index 3Fh (Bank 9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX2_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_AUX2_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT2** Value for AUXFANOUT2. 10,11: Keep Full Speed

9.422 Reserved Register – Index 40h (Bank 9)

9.423 AUXFANOUT2 Pre-Configured Register For PECI Error – Index 41h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 pre-configured register for PECI error (PECI_ERR_AUXOUT2)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT2 pre-configured register for PECI error.**

9.424 Reserved Register – Index 42h ~ FFh (Bank 9)

10. UART PORT

10.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 10-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

10.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

10.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

10.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

10.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

10.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.
5-4	**RESERVED.**
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table

	below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

10.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	**RESERVED.**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.

BIT	DESCRIPTION
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

10.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

10.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

10.10 UART RS485 Auto Flow Control

NCT6791D supports RS485 auto flow control function for UARTA and UARTB. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA and UARTB when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA adn UARTB.

The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1~2 x Bit-time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA and UARTB.

	UARTA	**UARTB**
RTS485_enable	Logic Device 2, CRF2_Bit7	Logic Device 3, CRF2_Bit7
RTS485_inv_sel	Logic Device 2, CRF2_Bit6	Logic Device 3, CRF2_Bit6

11. PARALLEL PORT

11.1 Printer Interface Logic

The NCT6791D parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The NCT6791D supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 11-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF NCT6791D	PIN ATTRIBUTE	SPP	EPP	ECP
1	55	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	421-45, 47-50	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	41	I	nACK	Intr	nACK, PeriphClk[2]
11	40	I	BUSY	nWait	BUSY, PeriphAck[2]
12	39	I	PE	PE	Peerror, nAckReverse[2]
13	38	I	SLCT	Select	SLCT, Xflag[2]
14	54	O	Nafd	nDStrb	nAFD, HostAck[2]
15	53	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	52	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	51	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:
n<name > : Active Low
1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF NCT6791D	PIN ATTRIBUTE	SPP
1	55	O	nSTB
2	50	I/O	PD0
3	49	I/O	PD1
4	48	I/O	PD2
5	47	I/O	PD3
6	45	I/O	PD4
7	44	I/O	PD5
8	43	I/O	PD6
9	42	I/O	PD7
10	41	I	nACK
11	40	I	BUSY
12	39	I	PE
13	38	I	SLCT
14	54	O	nAFD
15	53	I	nERR
16	52	O	nINIT
17	51	O	nSLIN

11.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 11-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 11-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

11.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

11.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	**RESERVED.**
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means hat no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

11.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED.** These two bits are always read as logical 1 and can be written.
5	**DIR (Direction Control Bit).** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

11.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

11.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

11.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
Nwrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
Nwait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

11.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

11.2.8 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

11.2.9 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

11.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the NCT6791D parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The NCT6791D ECP supports the following modes.

Table 11-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

11.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 11-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 11-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	Perror	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

11.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0

NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

11.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	Perror	Select	nFault	1	1	1

BIT	DESCRIPTION
7	**nBusy.** This bit reflects the complement of the Busy input.
6	**nAck.** This bit reflects the nAck input.
5	**Perror.** This bit reflects the Perror input.
4	**Select.** This bit reflects the Select input.
3	**nFault.** This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

11.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**Reserved.** These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**nInit.** This bit is output to the INIT# output.

BIT	DESCRIPTION
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

11.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

11.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

11.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

11.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

11.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION	
7	**Compress.** This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.	
6	**intrValue.** Returns the value on the ISA IRQ line to determine possible conflicts.	
5	**IRQx2.**	Reflects the IRQ resource assigned for ECP port. **cnfgB[5:3]** — **IRQ resource** 000 — Reflects other IRQ resources selected by PnP register (default)

BIT	DESCRIPTION		
4	**IRQx1.**	001	IRQ7
		010	IRQ9
		011	IRQ10
		100	IRQ11
		101	IRQ14
3	**IRQx0.**	110	IRQ15
		111	IRQ5
2-0	**Reserved.** These three bits are logical 1 during a read and can be written.		

11.3.10ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION	
7-5	**Mode.** Read/Write. These bits select the mode.	
	000	Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
	001	PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
	010	Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
	011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
	100	EPP Mode. EPP mode is activated if the EPP mode is selected.
	101	Reserved.
	110	Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.
	111	Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.
4	**nErrIntrEn.** Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.	
3	**dmaEn.** Read/Write.	

BIT	DESCRIPTION
	0: Disable DMA unconditionally. 1: Enable DMA.
2	**serviceIntr.** Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be rest to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

11.3.11ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
Nstrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
Perror (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.

NAME	TYPE	DESCRIPTION
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

11.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

I Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

11.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

11.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

11.3.12.3. Data Compression

The NCT6791D hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

11.3.13FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

11.3.14DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or Cfifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

11.3.15Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

12. KEYBOARD CONTROLLER

The NCT6791D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

Figure 12-1 Keyboard and Mouse Interface

12.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

12.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

12.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 12-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

12.4 Commands

Table 12-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>Aah</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>Abh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>Adh</td><td>Disable Keyboard Interface</td></tr>
</table>

COMMAND	FUNCTION
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

12.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

12.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: KBC clock input is 12 MHz. 1 1: Reserved
6	**KCLKS0.**	
5-3	**RESERVED.**	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a “D1” command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an “FE” command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

12.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RES. (0)**
5	**RES. (1)**
4-3	**RES. (0)**
2	**RES. (1)**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

13. CONSUMER INFRARED REMOTE (CIR)

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of H Level and L Level. The results are saved/stored in 32*8 RX FIFO. The max widths of H Level and L Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

As for the transmission, the user has to set up the Carrier frequency and the transmission mode first and then writes the widths of H Level and L Level via TX FIFO. The hardware will add Carrier to H Level according to the transmission mode.

13.1 CIR Register Table

Table 13-1 CIR Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	R	WIREN	TXEN	RXEN	WRXINV	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+2	IREN	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+3	RXFCONT	RXFIFO Count							
base+4	CP	MODE	Reserved						Carrier Prescalar
base+5	CC	Carrier Period							
base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	TXFIFOCLR	R	Tx Trigger Level		RXFIFOCLR	R	Rx Trigger Level	
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
base+A	SRXFIFO	Sample RX FIFO							
base+B	TXFCONT	TX FIFO Count							
base+C	STXFIFO	Sample TX FIFO							
base+D	FCCH	Frame Carrier Count High Byte							
base+E	FCCL	Frame Carrier Count Low Byte							
base+F	IRFSM	R	Decoder FSM			R	Encoder FSM		

13.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Received**	**WIREN**	**TXEN**	**RXEN**	**WRXINV**	**RXINV**	**Sample Period Select**	
DEFAULT	0	0	0	0	0	1	0	0

BIT	**DESCRIPTION**
7	**Received**.
6	**Wide-band IR Enable**

5	**TX Enable** 1: Transmission Enable. After confirming that FIFO is not empty, the transmission starts (the hardware will wait until TX FIFO data are written). If TX Enable is set to 0 during the transmission, the transmission stops when the transmission of FIFO data is completed. 0: Transmission Disable.
4	**RX Enable**
3	**Wide-band IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1~0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

13.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
Name	**RDR**	**RTR**	**PE**	**RFO**	**TE**	**TTR**	**TFU**	**GH**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**TX FIFO Empty** (Writing 1 will clear the bit).
2	**TX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
1	**TX FIFO Underrun** (Writing 1 will clear the bit).
0	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

13.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**TX FIFO Empty**
2	**TX FIFO Trigger Level Reach**
1	**TX FIFO Underrun**
0	**Min Length Detected**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

13.1.4 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	**RX FIFO Count**

13.1.5 IR TX Carrier Prescalar Configuration Register (CP) – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Mode	Reserved						CP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Mode** 0 : DC Mode 1 : Pulse Mode
6~1	**Reserved**.
0	**Carrier Prescalar** (CP). This bit is set for the Prescalar value of the IR TX carrier

	frequency.

13.1.6 IR TX Carrier Period Configuration Register (CC) – Base Address + 5

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Period (CC)							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is set for IR TX carrier period. The actual carrier period will be: Period = 2 * (2 ^ (CP*2)) * (CC+1) / (System Clock), where the frequency = 1 / period, and System Clock = 24MHz. Setting CP and CC to 0 will cause stop the device to from use using anyno carrier at all (that is, no light modulation, just constant on and off periods). The period count value CC can be any number from 0 to 255.

13.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the high byte of the limited count in the IR RX mode.

13.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

13.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TXFIFOCLR	Reserved	TX Trigger Level		RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TX FIFO Cleared**.
6	**Reserved**.
5~4	**TX Trigger Level** **Bits** **5 4** 0 0: 31 0 1: 24 1 0: 16 1 1: 8
3	**RX FIFO Cleared**.
2	**Reserved**.
1~0	**RX Trigger Level** **Bits** **1 0** 0 0: 1 0 1: 8 1 0: 16 1 1: 24

13.1.10IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**IR Pending** 1: No Interrupt 0: Interrupt issue
6	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
5	**RX FIFO Trigger Level Active**.
4	**RX FIFO Empty Flag**.
3	**RX FIFO Full Flag**.
2	**TX FIFO Trigger Level Active**.

BIT	DESCRIPTION
1	**TX FIFO Empty Flag**.
0	**TX FIFO Full Flag**.

13.1.11IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6~0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

13.1.12TX FIFO Count– Base Address + 5

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TX FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	**TX FIFO Count**

13.1.13IR Sample TX FIFO Register – Base Address + C

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample TX FIFO						

BIT	DESCRIPTION

7	**Voltage Level** 0: Low, 1: High
6~0	**TX data length** (Unit : Sample Period)

13.1.14IR Carrier Count High Byte Register – Base Address + D

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count High Byte							

BIT	DESCRIPTION
7~0	**Carrier Count High Byte**. This byte records the total amount of the total rising edges until time-out event appears.

13.1.15IR Carrier Count Low Byte Register – Base Address + E

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count Low Byte							

BIT	DESCRIPTION
7~0	**Carrier Count Low Byte**. This byte records the total amount of the the rising edges until time-out event appears.

After a time-out of reception on the learning receiver, this response is sent to tell the host the carrier frequency of the previous sample. The Carrier Count High Byte (ch) and Carrier Count Low Byte (cl) specify the cycle counts of cycles of the carrier. Carrier counts can also be thought ofregarded as the number of leading edges in the previous sample.

This is used toe calculation of the calculate carrier frequency is as followsfollowed:

$lastCarrierCount_{(decimal)}$ = ch*256+cl;

Thus,

Carrier frequency = (lastCarrierCount) / (irPacketOnDuration);

The **irPacketOnDuration** value is the total amount of time that the envelope of the signal was is high. The IR receiver should keep track of the time that of the high envelope is high and return it using this response.

This response is unsolicited. It is returned by the receiver when IR arrives but is never explicitly requested.

13.1.16IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved	Encoder FSM		

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Decoder over status**
5	**Decoder continuing status**
4	**Decoder wait H status** 1: idle, 0: RX busy
3	**Reserved**.
2	**Encoder Idle Status**. 1: idle, 0: TX busy
1	**Encoder Read Status**
0	**Encoder Level Output Status**

13.1.17IR Minimum Length Register – Base Address + F

Attribute: Write Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Min Length Register**							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	**Min Length Register**. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

14. CONSUMER INFRARED REMOTE (CIR) WAKE-UP

One of the features of the NCT6791D is system boot-up by a remote controller. The hardware will store a specifically appointed key command from the IR remote controller in the FIFO of 67Byte.

The same key is required to re-boot the system after the computer shut-down. Such way can be applied to any remote controllers. Learning is necessary only at the first time.

14.1 CIR WAKE-UP Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	DEC_RST	Mode[1]	Mode[0]	RXEN	IgnoreEN	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	GH	R	R	IR Pending
base+2	IREN	RDR	RTR	PE	RFO	GH	R		
Base+3		FIFO_COMPARE_DEEP							
base+4		FIFO_COMPARE_TOLERANCE							
base+5		FIFO_Count							
Base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	SRXFSTS	GS	FTA	Empty	Full	R			
base+A		Sample RX FIFO							
base+B		WR_FIFO_DATA							
Base+C		Read FIFO Only							
Base+D		Read FIFO Only Index							
Base+E		FIFO_Ignore							
Base+F	IRFSM	R	Decoder FSM			R			Wakeup Event

14.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**DEC_RST**	**Mode[1]**	**Mode[0]**	**RXEN**	**Received**	**RXINV**	**Sample Period Select**	
DEFAULT	0	0	1	0	0	1	1	0

BIT	**DESCRIPTION**
7	**Reset CIR DECODER** (Write 1 to clear)
6	**Mode[1]** : 0: FIFO can't be written 1: FIFO can be written
5	**Mode[0]** 0: Learning Mode

BIT	DESCRIPTION
	1: Wake up Mode (Before enter in Power S3 state, this bit should be set) This bit reset by VCC.
4	**RX Enable**
3	**Ignore Bit Enable**
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1~0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

14.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Received		IR_Pending
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.
2~1	**Reserved**.
0	**IR Pending** 1: No Interrupt 0: Interrupt issue

14.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**Min Length Detected**
2~0	**Reserved**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

14.1.4 IR TX Configuration Register – Base Address + 3

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Deep							
DEFAULT	0	1	0	0	0	0	1	1

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	When in S3 state, how many bytes need to compare. Default is 67 bytes.

14.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	**FIFO Data Tolerance between Learning mode and Wakeup mode**. (Every byte) FIFO Date Tolerance = (Learning mode data) – (Wakeup mode data)

14.1.6 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	RX FIFO Count

14.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the high byte of the limited count in the IR RX mode.

14.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

14.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~4	**Reserved**
3	**RX FIFO Cleared.**
2	**Reserved.**
1~0	**RX Trigger Level** **Bits** **1 0** 0 0: 67

	0 1: 66 1 0: 65 1 1: 64

14.1.10IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GS	FTA	Empty	Full	Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
6	**RX FIFO Trigger Level Active.**
5	**RX FIFO Empty Flag**.
4	**RX FIFO Full Flag**.
3~0	**Reserved**

14.1.11IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

14.1.12Write FIFO – Base Address + B

Attribute: Write Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Write Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period)

Note. Before writing FIFO Data, mode[1] register should be set.

14.1.13Read FIFO Only – Base Address + C

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	RX data length (Unit : Sample Period)

Note. Only Read FIFO Data.

14.1.14Read FIFO Index – Base Address + D

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Index							

BIT	DESCRIPTION
7~0	Indicate that FIFO Index when only read FIFO data(Base Address + C)

Note. Only Read FIFO Data.

14.1.15Reserved – Base Address + E

14.1.16 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			Wake up event
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6~4	CIR State Machine
3~1	Reserved
0	**Wake up event:** 0: CIR wake up event has not been triggered. 1: CIR wake up event has been triggered. (Wake up event clear: Write 11b to “Logic Decice A, CRE8h, bit7~6” then 00b.)

14.1.17IR Minimum Length Register – Base Address + F

Attribute: Write Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Min Length Register. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

15. POWER MANAGEMENT EVENT

The PME# (pin 65) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the NCT6791D are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the NCT6791D won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events [Note.1].

1) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

[Note.1] PME wake-up events that the NCT6791D supports include:

- Mouse event*
- Keyboard event*
- GP41, GP46, GP31, GP32 events *
- CIR*
- Printer IRQ event
- UART A IRQ event
- UART B IRQ event
- IR IRQ event
- Hardware Monitor IRQ event
- WDT1 event
- RIA (UARTA Ring Indicator) event
- RIB (UARTB Ring Indicator) event

[Note.2] All the above support both S0 and S1 states. Events with the "*" mark also support S3 ~ S5 states.

15.1 Power Control Logic

This chapter describes how the NCT6791D implements its ACPI function via these power control pins: PSIN# (Pin 61), PSOUT# (Pin 60), SLP_S3# (Pin 64) and PSON# (Pin 63). The following figure illustrates the relationships.

Figure 15-1 Power Control Mechanism

15.1.1 PSON# Logic

15.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 15-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

Figure 15-2 Power Sequence from S5 to S0, then Back to S5

15.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT6791D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 15-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The NCT6791D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

Figure 15-3 The previous state is “on”

3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

Figure 15-4 The previous state is “off”.

3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6791D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

15.2 Wake Up the System by Keyboard and Mouse

The NCT6791D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT6791D works.

15.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to “1”.

There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to “1” (Default).
2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to “0”.

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of “0” is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index(CRE1)→	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data(CRE2)→	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00

First-pressed key “0”

Second-pressed key “1”

Third-pressed key “2”

15.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to “1”.

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 15-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

15.3 Resume Reset Logic

The RSMRST# (Pin 101) signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT6791D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 15-5 and Table 15-3.

Figure 15-5 Mechanism of Resume Reset Logic

Table 15-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.033	V
V2	3VSB Ineffective Voltage	2.882	-	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

16. SERIALIZED IRQ

The NCT6791D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

16.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT6791D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT6791D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

Figure 16-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT6791D because IRQ1 of the NCT6791D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

16.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT6791D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT6791D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT6791D device drives the SERIRQ high. During the Turn-around phase, the NCT6791D device leaves the SERIRQ tri-stated. The NCT6791D starts to drive the SERIRQ line from the beginning of “IRQ0 FRAME” based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 16-1.

Table 16-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	IR
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

16.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

Figure 16-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

17. WATCHDOG TIMER

The Watchdog Timer of the NCT6791D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7 provides an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0, GPIO2, GPIO4, GPIO6, bit[0],[4], GPIO3, bit[3], and GPIO7, bit[0] will trigger a low pluse apporx 100mS or low level by Logical Device 8 CR[F5h], bit[0]. In other words, when the value is counted down to zero, the timer stops, and the NCT6791D sets the WDT1 status bit in Logical Device 8, CR[F7h], bit[4]. Writing a zero will clear the status bit. it. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

18. GENERAL PURPOSE I/O

18.1 GPIO ARCHITECTURE

The NCT6791D provides 67 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inver-se). Port value is read/write through data register.

In addition, only **GP41, GP46, GP31 and GP32** are designed to be able to assert **PSOUT# or PME#** signal to wake up the system if any of them has any transitions. There are about 16ms debounced circuit inside these 4 GPIOs and it can be disabled by programming respective bit (LD9, CR[Feh] bit 4~7). The following table gives more detailed register map on GP41, GP46, GP31 and GP32.

Table 18-1 Relative Control Registers of GPIO 41, 46, 31 and 32 that Support Wake-Up Function

	EVENTROUTE I (PSOUT#) **0 : DISABLE** **1 : ENABLE**	**EVENTROUTE II (PME#)** **0 : DISABLE** **1 : ENABLE**	**EVENT DEBOUNCED** **0 : ENABLE** **1 : DISABLE**
GPIO41 (PIN52)	LDA, CR[FEh] bit7	LDA, CR[FEh] bit3	LD9, CR[FEh] bit4
GPIO46 (PIN38)	LDA, CR[FEh] bit6	LDA, CR[FEh] bit2	LD9, CR[FEh] bit5
GPIO31 (PIN76)	LDA, CR[FEh] bit5	LDA, CR[FEh] bit1	LD9, CR[FEh] bit6
GPIO32 (PIN75)	LDA, CR[FEh] bit4	LDA, CR[FEh] bit0	LD9, CR[FEh] bit7

Table 18-2 GPIO Group Programming Table

Equips maximum 67-pin GPIOs.					
GPIO0 Group Enable: Logic Device 8, CR30[1] Data: Logic Device 8, E0~E3 Multi-function: WDTO, SMI, BEEP, MLED (Logic Device 8, CRE4[0~7]) Reset: Logic Device A, CRE9[0] OD/PP: Logic Device F, CRE9					
Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP00	121	AUXFANOUT0	Output	3VCC	CR1C[0]=1
GP01	122	AUXFANOUT1	Output	3VCC	CR1C[1]=1

GP02	123	AUXFANOUT2	Output	3VCC	CR1C[2]=1
GP03	2	OVT#	Output (OD)	3VCC	CR1C[4:3]=00
GP04	3	AUXFANIN0	Input	3VCC	CR1C[5]=1
GP05	4	AUXFANIN1	Input	3VCC	CR1C[6]=1
GP06	5	AUXFANIN2	Input	3VCC	CR1C[7]=1
GP07	6	GP07	Input	3VCC	

GPIO1 Group

Enable: Logic Device 9, CR30[1]
Data: Logic Device 8, F0~F3
Multi-function: GRN, YLW (Logic Device 8, CRF4[0~7])
Reset: Logic Device A, CRE9[1]
OD/PP: Logic Device F, CRE0

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP10	14	GP10	Input	3VSB	
GP11	13	GP11	Input	3VSB	
GP12	12	GP12	Input	3VSB	
GP13	11	GP13	Input	3VSB	
GP14	10	GP14	Input	3VSB	
GP15	9	GP15	Input	3VSB	
GP16	8	GP16	Input	3VSB	
GP17	7	GP17	Input	3VSB	

GPIO2 Group

Enable: Logic Device 9, CR30[2]
Data: Logic Device 9, E0~E3
Multi-function: WDTO, SMI, BEEP, GRN, OVT (Logic Device 9, CRE9[0~7])
Reset: Logic Device A, CRE9[2]
OD/PP: Logic Device F, CRE1

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP20	59	KDAT	Bi-direction	3VSB	CR2A[0]=1
GP21	58	KCLK	Bi-direction	3VSB	
GP22	57	MDAT	Bi-direction	3VSB	CR2A[1]=1
GP23	56	MCLK	Bi-direction	3VSB	
GP24	95	CIRRX	Input	3VSB	CR27[3]=0, CR1B[4]=0
GP25	96	GP25	Input	3VSB	
GP26	118	TSIC	Input	3VSB	CR2C[0]=0
GP27	98	GP27	Input	3VSB	

GPIO3 Group

Enable: Logic Device 9, CR30[3]
Data: Logic Device 9, E4~E7
Multi-function: SMI, BEEP, GRN, WDTO (Logic Device 9, CREA[0~7])
Reset: Logic Device A, CRE9[3]
OD/PP: Logic Device F, CRE2

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP30	83	RESETCONI#		Input		3VSB	CR1A[7:6]= 01
GP31	76	SDA		Output		3VSB	CR1B[0]=0, CR1A[5]=1
GP32	75	SCL		Input		3VSB	CR1B[0]=0, CR1A[4]=1
GP33	71	VSBSW_L		Output		3VSB	CR2C[6:5]=01
GP34	55	{ SOUTC_P80_EN }		{ SOUTC_P80_EN }		3VSB	Strapping by LPT_EN or CR2F[1]
		0	GP34	0	Input		
		1	SOUTC_P80	1	Output		
GP35	54	{PO80_EN }		{ PO80_EN }		3VSB	
		0	GP35	0	Input		
		1	DGH_1	1	Output		
GP36	53	{ PO80_EN }		{ PO80_EN }		3VSB	
		0	GP36	0	Input		
		1	DGL_1	1	Input		

GPIO4 Group
Enable: Logic Device 9, CR30[4]
Data: Logic Device 9, F0~F2, E8
Multi-function: WDTO, SMI, BEEP, YLW (Logic Device 9, CREE[0~7])
Reset: Logic Device A, CRE9[4]
OD/PP: Logic Device F, CRE3

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP40	62	GP40		Input		3VSB	
GP41	52	{ LPT_EN }		{ LPT_EN }		3VSB	CR1A[3:2]=10, LPT_EN=0
		0	MSCL	0	Input		
		1	INIT#	1	Otput		
GP42	51	{ LPT_EN }		{ LPT_EN }		3VSB	CR1B[2:1]=11, LPT_EN=0
		0	MSDA	0	Input		
		1	SLIN#	1	Output		
GP43	41	{ PO80_EN }		{ PO80_EN }		3VSB	CR27[4]=1, LPT_EN=0
		0	DGL_0#	0	Output		
		1	ACK#	1	Input		
GP44	40	{ LPT_EN }		{ LPT_EN }		3VSB	CR1B[6]=0, LPT_EN=0
		0	GRN_LED	0	Output		
		1	BUSY	1	Input		
GP45	39	{ LPT_EN }		{ LPT_EN }		3VSB	
		0	YLW_LED	0	Output		
		1	PE	1	Input		
GP46	38	{ LPT_EN }		{ LPT_EN }		3VSB	CR27[5]=0, LPT_EN=0
		0	GP46	0	Input		
		1	SLCT	1	Input		

GP47	37	RESETCONO#	output(OD)	3VSB	CR1B[7]=1

GPIO5 Group
Enable: Logic Device 9, CR30[5]
Data: Logic Device 9, F4~F7
Multi-function: GRN, YLW, SLPS5_Lch (Logic Device 8, CREB[0~7])
Reset: Logic Device A, CRE9[5]
OD/PP: Logic Device F, CRE4

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP50	93	{ DSW_EN }		{ DSW_EN }		3VSB	Strapping by DSW_EN or CR2F[3]
		0	GP50	0	Input		
		1	SUSWARN#	1	Input		
GP51	92	{ DSW_EN }		{ DSW_EN }		3VSB	
		0	GP51	0	Input		
		1	5VDUAL	1	Input		
GP52	91	{ DSW_EN }		{ DSW_EN }		3VSB	
		0	GP52	0	Inputi		
		1	SUSACK#	1	Output(OD)		
GP53	90	{ DSW_EN }		{ DSW_EN }		3VSB	
		0	GP53	0	Input		
		1	SUSWARN _5VDUAL	1	Output (OD)		
GP54	89	{ DSW_EN }		{ DSW_EN }		3VSB	
		0	GP54	0	Input		
		1	SLP_SUS#	1	Input		
GP55	88	{ DSW_EN }		{ DSW_EN }		3VSB	
		0	GP55	0	Input		
		1	SLP_SUS_FET	1	Output		
GP56	87	{ AMDPWR_EN }		{ AMDPWR_EN }		3VSB	Strapping by AMDPWR_EN or CR2F[5]
		0	GP56	0	Input		
		1	VCORE_EN	1	Output (OD)		
GP57	86	{ AMDPWR_EN }		{ AMDPWR_EN }		3VSB	
		0	GP57	0	Input		
		1	VLDT_EN	1	Output (OD)		

GPIO6 Group
Enable: Logic Device 9, CR30[6]
Data: Logic Device 7, F4~F7
Multi-function: MLED, BEEP, SMI, WDTO (Logic Device 8, CRF8[0~7])
Reset: Logic Device A, CRE5[3]
OD/PP: Logic Device F, CRE5

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO

GP60	50	PO80_EN = 0 LED_A~LED_G, DGH_0#	PO80_EN = 0 Output	3VSB	CR27[4]=1, LPT_EN=0
GP61	49			3VSB	
GP62	48			3VSB	
GP63	47	LPT_EN = 1 PD0 ~ PD7	LPT_EN = 1 Bi-direction	3VSB	
GP64	45			3VSB	
GP65	44			3VSB	
GP66	43			3VSB	
GP67	42			3VSB	

GPIO7 Group
Enable: Logic Device 9, CR30[7]
Data: Logic Device 7, E0~E3
Multi-function: GRN, BEEP, SMI, WDTO (Logic Device 7, CREC[0~3])
Reset: Logic Device A, CRE5[4]
OD/PP: Logic Device F, CRE6

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP70	69	{ EN_AS }		{ EN_AS }		3VSB	Strapping by EN_AS or CR2F[2]
		0	GP70	0	Input		
		1	BCLKOUT0	1	Output		
GP71	68	{ EN_AS }		{ EN_AS }		3VSB	
		0	GP71	0	Input		
		1	BCLKOUT1	1	Output		
GP72	67	{ EN_AS }		{ EN_AS }		3VSB	
		0	GP72	0	Input		
		1	BCLKIN0	1	Input		
GP73	66	{ EN_AS }		{ EN_AS }		3VSB	
		0	GP73	0	Input		
		1	BCLKIN1	1	Input		
GP74	79	RSTOUT0#		Output		3VSB	CR2B[5]=1
GP75	78	RSTOUT1#		Output		3VSB	CR2B[6]=1
GP76	77	RSTOUT2#		Output		3VSB	CR2B[7]=1

GPIO8 Group
Enable: Logic Device 9, CR30[0]
Data: Logic Device 7, E4~E7
Multi-function: YLW, BEEP, SMI, WDTO (Logic Device 7, CRED[0~6])
Reset: Logic Device A, CRE5[5]
OD/PP: Logic Device F, CRE7

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP80	29	GP80	Input	3VSB	
GP81	30	GP81	Input	3VSB	
GP82	31	GP82	Input	3VSB	
GP83	32	GP83	Input	3VSB	

GP84	33	GP84		Input		3VSB	
GP85	34	{ UARTP80_EN }		{ UARTP80_EN }		3VSB	
		0	GP85	0	Input		
		1	SOUTA_P80	1	Output		
GP86	35	GP86		Input		3VSB	
GP87	36	GP87		Input		3VSB	

18.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 18-2. Base address plus 0 to 4 are GPIO registers, base address plus 5 and 6 are watchdog registers.Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#7 for GPIO0 ~ GPIO7 respectively). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time.

Table 18-3 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved				INDEX			
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							
Base + 5	Wdtmod	Watchdog Timer I (WDT1) and KBC P20 Control Mode Register							
Base + 6	Wdttim	Watchdog Timer I (WDT1) Control Register							

19. SMBUS MASTER INTERFACE

19.1 General Description

The SMBus interface module is two wire serial interface compatible to the SMBus physical layer. It is also compatible with Intel's SMBus and Philips' I^2C bus.

The rest of this section introduces the various features of the SMBus master capability. These features are divided into the following sections:

- SMBus and I^2C compliant
- AMD-TSI
- PCH
- SMBus master

19.2 Introduction to the SMBus Master

19.2.1 Data Transfer Format

Every byte transferred on the bus consists of 8 bits. After the start condition, the master places the 7-bit address to the slave device it wants to address on the bus. The address followed an eight bit indicating the direction of the data transfer (R/W#); a zero indicates a transmission for data while a one indicates a request for data. Each byte is transferred with the most significant bit first, and after each byte, an acknowledge signal must follow. A data transfer is always terminated by stop condition generated by master.

Figure 19-1 Data Transfer Format

19.2.2 Arbitration

Arbitration takes place on the SMBDAT data line while the SMBCLK line is high. Two devices may generate a start condition at the same time and enter the arbitration procedure. Arbitration continues until one master generates a HIGH level on the SMBDAT line while another competing master generates a LOW level on the SMBDAT line while SMBCLK is high. The master device which generated the HIGH level on SMBDAT loses arbitration. If a device loses arbitration during the first byte following a start condition i.e. while transmitting a slave address it becomes a slave receiver and monitors the address for a potential match. Arbitration may also be lost in the master receive mode during the acknowledge cycle.

Figure 19-2 SMBus Arbitration

19.2.3 Clock Synchronization

Clock synchronization is performed while the arbitration procedure described above is in effect. Clock Synchronization takes place between two competing devices by utilizing the wired-AND nature of the SMBCLK line. The SMBCLK line will go low as soon as the master with the shortest high time pulls SMBCLK low. SMBCLK will remain low until the device with the longest SMBCLK low time relinquishes the SMBCLK line. Therefore the SMBCLK high time is determined by device with the shortest high time while the SMBCLK low time is determined by the device with the longest low time.

Figure 19-3 Clock synchronization

19.3 SB-TSI

The combined-format repeated start sequence is not supported in standard-mode and fast-mode.

- Only 7-bit SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only by written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

19.3.1 SB-TSI Address

The SMBus address is really 7 bits. The SB-TSI address is normally 98h or 4Ch. The address could vary with address select bits.

Table 19-1 SB-TSI Address Encoding

Address Select Bits	SB-TSI Address
000b	98h
001b	9Ah
010b	9Ch
011b	9Eh
100b	90h
101b	92h
110b	94h
111b	96h

19.4 PCH

The PCH provide system thermal data to EC. The EC can manage the fans and other cooling elements based on this data. A subset of the thermal collection is that the PCH and be programmed to alert the EC when a device has gone outside of its temperature limits.

19.4.1 Command Summary

Table 19-2 PCH Command Summary

Trans-action	Slave Addr.	Data Byte 0 =Command	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write STS Preferences	I2C	0x41	0x6	STS [47:40]	STS [39:32]	STS [31:24]	STS [23:16]	STS [15:8]	STS [7:0]
Write CPU Temp Limits	I2C	0x42	0x6	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [15:8]		
Write MCH	I2C	0x43	0x2	Lower	Upper	na	na		

Temp Limits				Limit [7:0]	Limit [7:0]				
Write IBX Temp Limits	I2C	0x44	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write DIMM Temp Limits	I2C	0x45	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write MPC CPU Power Clamp	I2C	0x50	0x2	Lower Limit [7:0]	Power Clamp [7:0]				
Block Read	Block Read Address	0x40	Block Read Address	Byte Count	Data 0	Data N	PEC (optional)		

19.5 SMBus Master

19.5.1 Block Diagram

Figure 19-4 SMBus Master Block Diagram

.

19.5.2 Programming Flow

Figure 19-5 Programming Flow

19.5.3 TSI Routine

Figure 19-6 TSI Routine

19.5.4 PCH Routine

Figure 19-7 PCH Routine

19.5.5 BYTE Ruttine

Figure 19-8 PCH Routine

19.5.6 Manual Mode interface

The SMBus host supports Block/Word/Byte Write and Block/Word/Byte read with PEC. The SMBus host can use the interface to access the smbus slave. The timing diagrams below illustrate how to use the smbus interface to write the data or read the data to the smbus slave.

Figure 19-9 Manual Mode Programming Flow

19.6 Register Type Abbreviations

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register.
- W = Write.
- RO = Read-only.

To program the SMBus master configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

19.6.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x26 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

19.6.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

19.7 SMBus Master Register Set

19.7.1 SMBus Register Map

SMBus Master base address in register Logic Device B CR62h(MSB), CR63h(LSB).

Table 19-3 SMBus Master Bank 0 Registers

Offset	Type	Name	Section
0	R/W	**SMBus Data**	19.7.2
1	R/W	**SMBus Write Data Size**	19.7.3
2	R/W	**SMBus Command**	19.7.4
3	R/W	**SMBus Index**	19.7.5
4	R/W	**SMBus Control**	19.7.6
5	R/W	**SMBus Address**	19.7.7
6	R/W	**SMBCLK Frequency**	19.7.8
7	RO	**Reserved**	--
8	R/W	**PCH Address**	19.7.9
9	R/W	**Error status**	19.7.10
A	R/W	**Reserved**	--
B	R/W	**PCH Command**	19.7.11
D	R/W	**TSI Agent Enable**	19.7.12
E	R/W	**SMBus Control 3 Register**	19.7.13
F	R/W	**SMBus Control 3 Register**	19.7.14
10	R/W	**BYTE_ADDR**	19.7.15
11	R/W	**BYTE Index High Byte**	19.7.16
12	R/W	**BYTE Index Low Byte**	19.7.17
13	R/W	**Reserved**	
14	R/W	**Reserved**	

19.7.2 SMBus Data (SMDATA) – Bank 0

This 32 bits register is the data in and out register of SMBus data register. Before writing to SMDATA register, this register contains the input data, after writing to SMDATA register, this register contains the output data.

Offset: 0h

Type: R/W

Byte	3	2	1	0
Name	**SMFIFO3**	**SMFIFO2**	**SMFIFO1**	**SMFIFO0**
Default	00h	00h	00h	00h

Byte	Description
3	**SMFIFO3 (SMBus FIFO 3).** This byte represents the high byte of the 32 bits SMBus data.
2	**SMFIFO2 (SMBus FIFO 2).** This byte represents the second byte of the 32 bits SMBus data.
1	**SMFIFO1 (SMBus FIFO 1).** This byte represents the first byte of the 32 bits SMBus data.
0	**SMFIFO0 (SMBus FIFO 0).** This byte represents the low byte of the 32 bits SMBus data.

19.7.3 SMBus Write Data Size (SMWRSIZE) – Bank 0

Offset: 1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**SMWRSIZE**				
Default	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4-0	**SMWRSIZE (SMBus Write Byte Counter).** This field sets the write byte counter, the max counter size is 32 bytes, and the minimal size is 1 bytes.

19.7.4 SMBus Command (SMCMD) – Bank 0

Offset: 2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
NAME	REV				SMBus CMD			
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**

3-0	**SMBCMD (SMBus Command).** This field sets SMBus Command: 0000 : Read Byte (Default) 0001 : Read Word 0010 : Read Block 0011 : Block Write and Read Process Call 0100 : Process Call 1000 : Write Byte 1001 : Write Word 1010 : Write Block

19.7.5 SMBus INDEX (SMIDX) – Bank 0

Offset: 3h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMCMD**							
Default	0	0	0	0	0	0	0	0

Bit	Description
7-0	**SMIDX (SMBus INDEX).** This field represents the index data of the SMBus.

19.7.6 SMBus Control (SMCTL) – Bank 0

Offset: 4h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**MMODE_S**	**S_RST**	**CRC8_EN**	**REFLASH_CLK**			**BYTE_EN**	**PCH_EN**
Default	0	0	0	0	0	0	0	0

Bit	Description
7	**MMODE_S (Manual Mode Set).** 0 : Disable. 1 : Enable.
6	**S_RST (Soft Reset SMBus).** 0 : Disable. 1 : Enable.
5	**CRC8_EN (CRC8 Enable).** 0 : CRC8 function is disable. 1 : CRC8 function is enable.

4-2	**REFRASH_CLK (Refrash Clock Select).** 000, 100 – 128ms 001, 101 – 256ms 010, 110 – 512ms 011, 111 – 64ms (1KHz)
1	**BYTE_EN (BYTE Enable).** 0 : BYTE function is disable. 1 : BYTE function is enable.
0	**PCH_EN (PCH Enable).** 0 : PCH function is disable. 1 : PCH function is enable.

19.7.7 SMBus Address (SMADDR) – Bank 0

Offset: 5h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMADDR**							**REV**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-1	**SMADDR (SMBus Address).** AMD-TSI only supports 7-bit SMBus address.
0	**Reserved:** 0 : Write. If the protocol is write, the WR_SIZE can't be zero. (Default)

19.7.8 SCL FREQ (SCLFREQ) – Bank 0

Offset: 6h

Type: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved:				**SCLFREQ**			
Default	0	0	0	0	0	1	1	1

Bit	Description
7-4	Reserved

3-0	**SCLFQ (SMBCLK Frequency).** This field defines the SMBCLK period (low time and high time). The clock low time and high time ate defined as follows: 0000 : 365KHz 0001 : 261KHz 0010 : 200KHz 0011 : 162KHz 0100 : 136KHz 0101 : 117KHz 0110 : 103KHz 0111 : 92KHz (Default) 1000 : 83KHz 1001 : 76KHz 1010 : 71KHz 1011 : 65KHz 1100 : 61KHz 1101 : 57KHz 1110 : 53KHz 1111 : 47KHz

19.7.9 PCH Address (PCHADDR) – Bank 0

Offset: 8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHADDR**							**REV**
Default	1	0	0	1	0	1	0	0

Bit	Description
7-1	**PCHADDR (PCH Address).** PCH supports 8-bit SMBus address. The default address is 94h. The last bit is read or write bit. It needs to set to “0”.

19.7.10SMBus Error Status (Error_status) – Bank 0

Offset: 9h

Type: RO/W1C

Bit	7	6	5	4	3	2	1	0
Name	**REV**		**ADNACK**	**Timeout**	**Reserved**	**BER**	**NACK**	**Reserved**
Default	1	0	0	1	0	1	0	0

Bit	Description
7-6	**Reserved.**
5	**ADDR Non ACK.** This bit reflects SMBus occurred ADDRESS NON ACK in Manual mode..
4	**Timeout.** This bit reflects when SMBus occurs timeout.

3	**Reserved.**
2	**BER (Bus Error).** This bit reflects when a start or stop condition is detected during data transfer, or when an arbitration problem is detected.
1	**NACK (Negative acknowledge).** This bit is set by hardware when a transmission is not acknowledged on the ninth clock. While NACK is set SCL will be drive low and subsequent bus transactions are stalled until NACK is cleared.
0	**Reserved.**

19.7.11PCH Command (PCHCMD) – Bank 0

Offset: Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHCMD**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**PCHCMD (PCH Command).** This field represents the command data of the PCH. The default command is block read (40h).

19.7.12TSI Agent Enable Register (TSI_AGENT) – Bank

Offset: Dh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0
Default	0	0	0	0	0	0	0	0

Bit	Description
7	**TSI AGENT7 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
6	**TSI AGENT6 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
5	**TSI AGENT5 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
4	**TSI AGENT4 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable

3	**TSI AGENT3 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
2	**TSI AGENT2 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
1	**TSI AGENT1 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
0	**TSI AGENT0 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable

19.7.13SMBus Control 3 Register (SMCTL3) – Bank 0

Offset: Eh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**CRC_CHK**	**M_MODE**	**F_FULL**	**F_EMPT**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**CRC_CHK (CRC Check).** 0 : incorrect 1 : correct
2	**M_MODE (Manual Mode).** 0 : Non-active 1 : Active
1	**F_FULL (fifo_full). :** This bit reflects SMBus data fifo is full. 0 : Non-full 1 : Full
0	**F_EMPT (fifo empty). :** This bit reflects the SMBus data fifo is empty. 0 : Non-empty 1 : Empty

19.7.14SMBus Control 2 Register (SMCTL2) – Bank 0

Offset: Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**INT_LCH_E**	**Reserved**		**BYTE_SEL**	**BANKSEL**	
Default	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**INT_LCH_E (Interrupt Latch Enable). :** This bit will latch the I2CSTA register. 0 : Disable. 1 : Enable.
2	**BYTE_SEL :**This field represents byte polling 8-bit/16bit select bits. 0: BYTE_TEMP is 16 bit data 1: BYTE_TEMP is 8 bit data
1-0	**BANKSEL (Bank Select).** 00 – Bank 0. 01 – Bank 1. 10 – Bank 2.

19.7.15BYTE ADDRESS (BYTE ADDR) – Bank 0

Offset: 10h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**BYTE ADDRESS (BYTE ADDR).** This field represents the address data of the BYTE.

19.7.16BYTE INDEX_H (BYTE_IDX_H) – Bank 0

Offset: 11h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_H**							
Default	0	0	0	0	0	0	0	1

Bit	Description
7-0	**BYTE_IDX_H (High BYTE INDEX).** This field represents the high byte index of the Byte polling. The default command is byte read (01h).

19.7.17BYTE INDEX_L (BYTE_IDX_L) – Bank 0

Offset: 12h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_L**							
Default	0	0	0	1	0	0	0	0

Bit	Description
7-0	**BYTE_IDX_L (LOW BYTE INDEX).** This field represents the low byte index of the Byte polling. The default command is byte read (10h).

The EC may read thermal information from IBX using the SMBus block read command. The IBX doesn't support byte-read or word-read SMBus commands. The read use a different address that the writes. The address must be different so that the IBX knows which target Is intended, either the I2C target or the block read buffer.

The IBX and EC are set up by BIOS with the length of the read that is supported by the platform. The EC must always do reads of the lengths set up by BIOS. There is no way to change the length of the read after BIOS has set things up.

An EC that only wants the single highest temperature among MCH, and CPU could read one byte. A 2 byte read would provide both IBX and CPU/MCH package temperature. An EC that wanted each components temperature would do a 4 byte read. An EC that also wanted DIMM information would read 9 bytes. If an EC wanted to read the HOST STS status, it must read 19 bytes. An EC can also read the energy data provided by the CPU by reading 12 bytes.

20. OVP & UVP DETECT

20.1 ASUS OVP & UVP Detect

Figure 20-1 OVP & UVP Detect (ANTISURGE_EN = 1)

20.2 ASUSTEK OVP & UVP Detect

Figure 20-2 OVP & UVP Detect when SLP_S3# = 1 (ANTISURGE_EN = 0)

Figure 20-3 OVP & UVP Detect when SLP_S3# = 1 (ANTISURGE_EN = 0)

Table 20-1 Timing Parameters of OVP/UVP

TIMING	PARAMETER
T1	3VCC to OVP/UVP Detect Start (See LDA CRF1 Bit6-5)
T2	PSON# inactive to SLP_S3# Detect (See LDA CRF1 Bit4-3)

21. PORT80 TO UART

The NCT6106D provides UART interface to transfer PORT80 information to other peripheral devices. Default baud rate is 115200Hz for universal UART protocol and it could be change by LD14 CRE2 and LD14 CRE3. When BIOS program PORT80 LED, in proportion to UART baud rate, it changes very frequently. Thus, some information might be lose. But we make sure the last one would be send.

Figure 21-1 PORT80 to UART Block Diagram

After enter OS, we support other root to control PORT80 LED by write LDF CRF2 and LDF CRF1 to change other path. The UART could be control by other root, too. It is set by LD14 CRE4.

22. BCLK

BCLK can decode 2bit BCLK input (BCLKIN0~1) from PCH to BCLK output (BCLKOUT0~1) to CPU. We support 4 mode (Bypass, offset, manual, compare). We can use EN_AS strapping pin to enable BCLK function, or set blobal register CR2Fh[2] to enable.

Figure 22-1 BCLK architecture

In bypass mode, we don't interfere input but bypass. In offset mode, BCLK output in BCLK input add offset register. In manual mode, we send output depend on manual data but don't consider input. In compare mode, we compare input data add offset register and manual register, the bigger one is the output.

23. CONFIGURATION REGISTER

23.1 Chip (Global) Control Register

Default Value of Global Control Register:

Register	Default	Register	Default	Register	Default
CR 07h	00h	CR 20h	C5h (ID_H)	CR 2Bh	00h
CR 10h	FFh	CR 21h	62h (ID_L)	CR 2Ch	01h
CR 11h	FFh	CR 22h	FFh	CR 2Fh	0ss0ssssb
CR 13h	00h	CR 24h	04h		
CR 14h	00h	CR 25h	00h		
CR 1Ah	30h	CR 26h	0s000000b		
CR 1Bh	70h	CR 27h	00h		
CR 1Ch	10h	CR 28h	00h		
CR 1Dh	00h	CR 2Ah	C0h		

Note. The value of “s” means hardware strapping result: strapping high will report 1; strapping low will report 0.
In addition, BIOS can write the value of strapping result after hardware strapping.

Note. The CR21h is low-byte of the Chip-ID; the “X” means IC version. EX. 61=A version, 62=B version, 63=C version.

Reserved Registers of Global Control Register:

Register	Default	Register	Default
CR 02h	00h	CR 1Eh	FFh
CR 12h	FFh	CR 1Fh	FFh
CR 15h	FFh	CR 23h	00h
CR 16h	FFh	CR 29h	FFh
CR 17h	FFh	CR 2Dh	FFh
CR 18h	FFh	CR 2Eh	00h
CR 19h	FFh		

Note. All reserved registers must keep default value.

Note. Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 07h. Logical Device Selection

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	PRT IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	CIRWAKUP IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	WDTO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5-2	Reserved.	

BIT	READ / WRITE	DESCRIPTION
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah. Multi Function Selection
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 30h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin83 function selection
<table>
<tr><td>CR1A [Bit7-6]</td><td>Pin83</td></tr>
<tr><td>00</td><td>RESETCONI#</td></tr>
<tr><td>01</td><td>GP30</td></tr>
<tr><td>10</td><td>OVT#</td></tr>
<tr><td>11</td><td>SMI#</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin76 function selection
<table>
<tr><td>CR1B [Bit0]</td><td>CR1A [Bit5]</td><td>Pin76</td></tr>
<tr><td>1</td><td>x</td><td>MSDA</td></tr>
<tr><td>0</td><td>0</td><td>SDA</td></tr>
<tr><td>0</td><td>1</td><td>GP31</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><td>CR1B [Bit0]</td><td>CR1A [Bit4]</td><td>Pin75</td></tr>
<tr><td>1</td><td>x</td><td>MSCL</td></tr>
<tr><td>0</td><td>0</td><td>SCL</td></tr>
<tr><td>0</td><td>1</td><td>GP32</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin52 function selection
<table>
<tr><td>LPT_EN</td><td>CR1A [Bit3-2]</td><td>Pin52</td></tr>
<tr><td>1</td><td>xx</td><td>INIT#</td></tr>
<tr><td>0</td><td>00</td><td>MSCL</td></tr>
<tr><td>0</td><td>01</td><td>SCL</td></tr>
<tr><td>0</td><td>10</td><td>GP41</td></tr>
<tr><td>0</td><td>11</td><td>MSCL</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin74 function selection
<table>
<tr><td>CR1A [Bit1]</td><td>Pin74</td></tr>
<tr><td>0</td><td>BKFD_CUT</td></tr>
<tr><td>1</td><td>GPIOE#</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin27(GA20M) and Pin28(KBRST#) output type selection
0: push pull
1: OD</td></tr>
</table>

CR 1Bh. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 70h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin37 function selection
<table>
<tr><td>CR1B [Bit7]</td><td>Pin37</td></tr>
<tr><td>0</td><td>RESETCONO#</td></tr>
<tr><td>1</td><td>GP47</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin39 function selection
<table>
<tr><td>LPT_EN</td><td>CR1B [Bit6]</td><td>Pin39</td></tr>
<tr><td>1</td><td>x</td><td>PE</td></tr>
<tr><td>0</td><td>0</td><td>GP45</td></tr>
<tr><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
Pin40 function selection
<table>
<tr><td>LPT_EN</td><td>CR1B [Bit6]</td><td>Pin40</td></tr>
<tr><td>1</td><td>x</td><td>BUSY</td></tr>
<tr><td>0</td><td>0</td><td>GP44</td></tr>
<tr><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table></td></tr>
<tr><td>5</td><td colspan="2">Reserved.</td></tr>
<tr><td>4</td><td>R / W</td><td>Pin95 function selection
<table>
<tr><td>CR1B [Bit4]</td><td>CR27 [Bit3]</td><td>Pin95</td></tr>
<tr><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>GP24</td></tr>
<tr><td>0</td><td>1</td><td>IRRX1</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin62 function selection
<table>
<tr><td>CR1B [Bit3]</td><td>Pin62</td></tr>
<tr><td>1</td><td>GP40</td></tr>
</table></td></tr>
<tr><td>2-1</td><td>R / W</td><td>Pin51 function selection
<table>
<tr><td>LPT_EN</td><td>CR1B [Bit2-1]</td><td>Pin51</td></tr>
<tr><td>1</td><td>x</td><td>SLIN#</td></tr>
<tr><td>0</td><td>00</td><td>MSDA</td></tr>
<tr><td>0</td><td>01</td><td>SDA</td></tr>
<tr><td>0</td><td>10</td><td>BEEP</td></tr>
<tr><td>0</td><td>11</td><td>GP42</td></tr>
</table></td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
0	R / W	**Pin75** function selection CR1B [Bit0] / CR1A [Bit4] / Pin75 1 / x / MSCL 0 / 0 / SCL 0 / 1 / GP32 **Pin76** function selection CR1B [Bit0] / CR1A [Bit5] / Pin76 1 / x / MSDA 0 / 0 / SDA 0 / 1 / GP31

CR 1Ch. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: PWROK

Default : 10h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Pin5** function selection CR1C [Bit7] / Pin5 0 / AUXFANIN2 1 / GP06
6	R / W	**Pin4** function selection CR1C [Bit6] / Pin4 0 / AUXFANIN1 1 / GP05
5	R / W	**Pin3** function selection CR1C [Bit5] / Pin3 0 / AUXFANIN0 1 / GP04
4-3	R / W	**Pin2** function selection CR1C [Bit4-3] / Pin2 00 / GP03 01 / SMI# 10 / OVT# 11 / Tri-state

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>R / W</td><td>Pin123 function selection
<table>
<tr><td>CR1C [Bit2]</td><td>Pin123</td></tr>
<tr><td>0</td><td>AUXFANOUT2</td></tr>
<tr><td>1</td><td>GP02</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin122 function selection
<table>
<tr><td>CR1C [Bit1]</td><td>Pin122</td></tr>
<tr><td>0</td><td>AUXFANOUT1</td></tr>
<tr><td>1</td><td>GP01</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin121 function selection
<table>
<tr><td>CR1C [Bit0]</td><td>Pin121</td></tr>
<tr><td>0</td><td>AUXFANOUT0</td></tr>
<tr><td>1</td><td>GP00</td></tr>
</table></td></tr>
</table>

CR 1Dh. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: PWROK(Bit7-5, 0), RSMRST#(Bit4-3), RSMRST#&BCLKIN(Bit2-1)

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>0: GPIOE# is inactive. 1: GPIOE# is active.</td></tr>
<tr><td>6</td><td>R / W</td><td>Issue GPIOE# to RESETCONO#.
0: Disable
1: Enable</td></tr>
<tr><td>5</td><td>R / W</td><td>Issue GPIOE# to PWROK.
0: Disable
1: Enable</td></tr>
<tr><td>4</td><td>R / W</td><td>0: Disable ANTISURGE event route to KBRST#
1: Enable ANTISURGE event route to KBRST#</td></tr>
<tr><td>3-1</td><td>R / W</td><td>Pin89 function selection
<table>
<tr><td>DSW_EN</td><td>CR1D [Bit3]</td><td>CR1D [Bit2-1]</td><td>Pin89</td></tr>
<tr><td>1</td><td>x</td><td>xx</td><td>SLP_SUS#</td></tr>
<tr><td>0</td><td>0</td><td>xx</td><td>GP54</td></tr>
<tr><td>0</td><td>1</td><td>00</td><td>Tri-state</td></tr>
<tr><td>0</td><td>1</td><td>01</td><td>3VSBSW#</td></tr>
<tr><td>0</td><td>1</td><td>10</td><td>PWROK</td></tr>
<tr><td>0</td><td>1</td><td>11</td><td>Tri-state</td></tr>
</table></td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
0	R / W	**Pin6** function selection CR1D [Bit0] — Pin6 0 — GP07 1 — CIRTX0

CR 20h. Chip ID (High Byte)
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : C5h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = C5h (high byte).

CR 21h. Chip ID (Low Byte)
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 61h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 62h (low byte)

CR 22h. Device Power Down
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2-0	Reserved.	

CR 24h. Global Option
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	Select output type of AUXFANOUT2 =0 AUXFANOUT2 is Open-drain. =1 AUXFANOUT2 is Push-pull.
6	R / W	Select output type of AUXFANOUT1 =0 AUXFANOUT1 is Open-drain. =1 AUXFANOUT1 is Push-pull.
5	R / W	Select output type of AUXFANOUT0 =0 AUXFANOUT0 is Open-drain. =1 AUXFANOUT0 is Push-pull.
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. =1 SYSFANOUT is Push-pull.
3	R / W	Select output type of CPUFANOUT =0 CPUFANOUT is Open-drain. =1 CPUFANOUT is Push-pull.
2	R / W	**Pin128** function selection CR24 [Bit2] / Pin128 0 / OVT# 1 / SMI#
1	Reserved.	
0	R / W	PNPCVS => = 0 The compatible PNP address-select registers have default values. = 1 The compatible PNP address-select registers have no default values.

CR 25h. Interface Tri-state Enable
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	UARTBTRI
2	R / W	UARTATRI
1	R / W	PRTTRI
0	Reserved.	

CR 26h. Global Option s: value by strapping
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : 0s000000b

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin 31).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4-3	Reserved.	
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. Global Option

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	**Pin38** function selection

LPT_EN	CR27 [Bit5]	Pin38
1	x	SLCT
0	0	GP46
0	1	CIRRXWB

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin41 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin41</td></tr>
<tr><td>1</td><td>x</td><td>ACK#</td></tr>
<tr><td>0</td><td>0</td><td>DGL#</td></tr>
<tr><td>0</td><td>1</td><td>GP43</td></tr>
</table>
Pin42 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin42</td></tr>
<tr><td>1</td><td>x</td><td>PD7</td></tr>
<tr><td>0</td><td>0</td><td>DGH#</td></tr>
<tr><td>0</td><td>1</td><td>GP67</td></tr>
</table>
Pin43 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin43</td></tr>
<tr><td>1</td><td>x</td><td>PD6</td></tr>
<tr><td>0</td><td>0</td><td>LED_G</td></tr>
<tr><td>0</td><td>1</td><td>GP66</td></tr>
</table>
Pin44 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin44</td></tr>
<tr><td>1</td><td>x</td><td>PD5</td></tr>
<tr><td>0</td><td>0</td><td>LED_F</td></tr>
<tr><td>0</td><td>1</td><td>GP65</td></tr>
</table>
Pin45 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin45</td></tr>
<tr><td>1</td><td>x</td><td>PD4</td></tr>
<tr><td>0</td><td>0</td><td>LED_E</td></tr>
<tr><td>0</td><td>1</td><td>GP64</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin47 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin47</td></tr>
<tr><td>1</td><td>x</td><td>PD3</td></tr>
<tr><td>0</td><td>0</td><td>LED_D</td></tr>
<tr><td>0</td><td>1</td><td>GP63</td></tr>
</table>
Pin48 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin48</td></tr>
<tr><td>1</td><td>x</td><td>PD2</td></tr>
<tr><td>0</td><td>0</td><td>LED_C</td></tr>
<tr><td>0</td><td>1</td><td>GP62</td></tr>
</table>
Pin49 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin49</td></tr>
<tr><td>1</td><td>x</td><td>PD1</td></tr>
<tr><td>0</td><td>0</td><td>LED_B</td></tr>
<tr><td>0</td><td>1</td><td>GP61</td></tr>
</table>
Pin50 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin50</td></tr>
<tr><td>1</td><td>x</td><td>PD0</td></tr>
<tr><td>0</td><td>0</td><td>LED_A</td></tr>
<tr><td>0</td><td>1</td><td>GP60</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>R / W</td><td>
Pin95 function selection
<table>
<tr><td>CR1B [Bit4]</td><td>CR27 [Bit3]</td><td>Pin95</td></tr>
<tr><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>GP24</td></tr>
<tr><td>0</td><td>1</td><td>IRRX1</td></tr>
</table>
Pin96 function selection
<table>
<tr><td>CR2A [Bit3]</td><td>CR27 [Bit3]</td><td>Pin96</td></tr>
<tr><td>1</td><td>x</td><td>CIRTX1</td></tr>
<tr><td>0</td><td>0</td><td>GP25</td></tr>
<tr><td>0</td><td>1</td><td>IRTX1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>R / W</td><td>Pin11 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin11</td></tr>
<tr><td>1</td><td>x</td><td>IRRX0</td></tr>
<tr><td>0</td><td>0</td><td>SINB</td></tr>
<tr><td>0</td><td>1</td><td>GP13</td></tr>
</table>
Pin12 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin12</td></tr>
<tr><td>1</td><td>x</td><td>IRTX0</td></tr>
<tr><td>0</td><td>0</td><td>SOUTB</td></tr>
<tr><td>0</td><td>1</td><td>GP12</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>LV_DETECT_L
0: AMD power sequence detect level and time delay
1: AMD power sequence non detect level but time delay</td></tr>
<tr><td>0</td><td colspan="2">Reserved.</td></tr>
</table>

CR 28h. Global Option

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	PRTMODS2 ~ 0 => **Bits** **2 1 0** = 0 x x Parallel Port Mode. = 1 x x Reserved.

CR 2Ah. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, GP2X_MRST(Bit0)
Default : C0h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin29 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin29</td></tr>
<tr><td>0</td><td>CTSA#</td></tr>
<tr><td>1</td><td>GP80</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>
Pin30 function selection
<table><tr><td>CR2A [Bit7]</td><td>Pin30</td></tr><tr><td>0</td><td>DSRA#</td></tr><tr><td>1</td><td>GP81</td></tr></table>
Pin31 function selection
<table><tr><td>CR2A [Bit7]</td><td>Pin31</td></tr><tr><td>0</td><td>RTSA#</td></tr><tr><td>1</td><td>GP82</td></tr></table>
Pin32 function selection
<table><tr><td>CR2A [Bit7]</td><td>Pin32</td></tr><tr><td>0</td><td>DTRA#</td></tr><tr><td>1</td><td>GP83</td></tr></table>
Pin33 function selection
<table><tr><td>CR2A [Bit7]</td><td>Pin33</td></tr><tr><td>0</td><td>SINA</td></tr><tr><td>1</td><td>GP84</td></tr></table>
Pin34 function selection
<table><tr><td>UARTP80_EN</td><td>CR2A [Bit7]</td><td>Pin34</td></tr><tr><td>1</td><td>x</td><td>SOUTA_P80</td></tr><tr><td>0</td><td>0</td><td>SOUTA</td></tr><tr><td>0</td><td>1</td><td>GP85</td></tr></table>
Pin35 function selection
<table><tr><td>CR2A [Bit7]</td><td>Pin35</td></tr><tr><td>0</td><td>DCDA#</td></tr><tr><td>1</td><td>GP86</td></tr></table>
Pin36 function selection
<table><tr><td>CR2A [Bit7]</td><td>Pin36</td></tr><tr><td>0</td><td>RIA#</td></tr><tr><td>1</td><td>GP87</td></tr></table>
</td></tr>
<tr><td>6</td><td>R / W</td><td>
Pin7 function selection
<table><tr><td>CR2A [Bit6]</td><td>Pin7</td></tr><tr><td>0</td><td>CTSB#</td></tr><tr><td>1</td><td>GP17</td></tr></table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R/W</td><td>
Pin8 function selection
<table><tr><td>CR2A [Bit6]</td><td>Pin8</td></tr><tr><td>0</td><td>DSRB#</td></tr><tr><td>1</td><td>GP16</td></tr></table>
Pin9 function selection
<table><tr><td>CR2A [Bit6]</td><td>Pin9</td></tr><tr><td>0</td><td>RTSB#</td></tr><tr><td>1</td><td>GP15</td></tr></table>
Pin10 function selection
<table><tr><td>CR2A [Bit6]</td><td>Pin10</td></tr><tr><td>0</td><td>DTRB#</td></tr><tr><td>1</td><td>GP14</td></tr></table>
Pin11 function selection
<table><tr><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin11</td></tr><tr><td>1</td><td>x</td><td>IRRX0</td></tr><tr><td>0</td><td>0</td><td>SINB</td></tr><tr><td>0</td><td>1</td><td>GP13</td></tr></table>
Pin12 function selection
<table><tr><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin12</td></tr><tr><td>1</td><td>x</td><td>IRTX0</td></tr><tr><td>0</td><td>0</td><td>SOUTB</td></tr><tr><td>0</td><td>1</td><td>GP12</td></tr></table>
Pin13 function selection
<table><tr><td>CR2A [Bit6]</td><td>Pin13</td></tr><tr><td>0</td><td>DCDB#</td></tr><tr><td>1</td><td>GP11</td></tr></table>
Pin14 function selection
<table><tr><td>CR2A [Bit6]</td><td>Pin14</td></tr><tr><td>0</td><td>RIB#</td></tr><tr><td>1</td><td>GP10</td></tr></table>
</td></tr>
<tr><td>5-4</td><td colspan="2">Reserved.</td></tr>
<tr><td>3</td><td>R/W</td><td>
Pin96 function selection
<table><tr><td>CR2A [Bit3]</td><td>CR27 [Bit3]</td><td>Pin96</td></tr><tr><td>1</td><td>x</td><td>CIRTX1</td></tr><tr><td>0</td><td>0</td><td>GP25</td></tr><tr><td>0</td><td>1</td><td>IRTX1</td></tr></table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>R/W</td><td>Enable Over Temperature shutdown Protection (OVT#)
= 0 The thermal shutdown function is disabled. (Default)
= 1 Enable thermal shutdown function.
(If set this bit to 1, the relative registers of OVT# event are:
Bank0, CR18 ,Bit6 → SMIOVT1 OVT# (Default SYSTIN)
Bank0, CR4C ,Bit4 → SMIOVT3 OVT# (Default AUXTIN)
Bank0, CR4C ,Bit3 → SMIOVT2 OVT# (Default CPUTIN)
If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately.)</td></tr>
<tr><td>1</td><td>R / W</td><td>Pin56 function selection
<table>
<tr><td>CR2A [Bit1]</td><td>Pin56</td></tr>
<tr><td>0</td><td>MCLK</td></tr>
<tr><td>1</td><td>GP23</td></tr>
</table>
Pin57 function selection
<table>
<tr><td>CR2A [Bit1]</td><td>Pin57</td></tr>
<tr><td>0</td><td>MDAT</td></tr>
<tr><td>1</td><td>GP22</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin58 function selection
<table>
<tr><td>CR2A [Bit0]</td><td>Pin58</td></tr>
<tr><td>0</td><td>KCLK</td></tr>
<tr><td>1</td><td>GP21</td></tr>
</table>
Pin59 function selection
<table>
<tr><td>CR2A [Bit0]</td><td>Pin59</td></tr>
<tr><td>0</td><td>KDAT</td></tr>
<tr><td>1</td><td>GP20</td></tr>
</table></td></tr>
</table>

CR 2Bh. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin77 function selection
<table>
<tr><td>CR2B [Bit7]</td><td>Pin77</td></tr>
<tr><td>0</td><td>RSTOUT2#</td></tr>
<tr><td>1</td><td>GP76</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin78 function selection
<table>
<tr><td>CR2B [Bit6]</td><td>Pin78</td></tr>
<tr><td>0</td><td>RSTOUT1#</td></tr>
<tr><td>1</td><td>GP75</td></tr>
</table></td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
5	R / W	**Pin79** function selection CR2B [Bit5] – Pin79 0 – RSTOUT0# 1 – GP74
4-0	Reserved.	

CR 2Ch. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6-5	R / W	**Pin71** function selection CR2C [Bit6-5] – Pin71 00 – 3VSBSW# 01 – GP33 10 – LATCH_BKFD_CUT# 11 – 3VSBSW#
4-3	R / W	**Pin98** function selection CR2C [Bit4-3] – Pin98 00 – GP27 01 – MLED 10 – CIRRXWB1 11 – Tri-state
2-1	Reserved.	
0	R / W	**Pin118** function selection CR2C [Bit0] – Pin118 0 – GP26 1 – TSIC **Pin120** function selection CR2C [Bit0] – Pin120 0 – PECI 1 – TSID

CR 2Fh. Strapping Function Result

Location: Address 2Fh

Attribute: Read/Write

Power Well: VSB
Reset by: RSMRST#(Bit5-2), PWROK(Bit0), LRESET#(Bit6, 1)
Default : by 0ss0_ssss
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	UARTP80_EN Strapping result reading
5	R / W	AMDPWR_EN Strapping result reading
4	Reserved.	
3	R / W	DSW_EN Strapping result reading
2	R / W	EN_AS Strapping result reading
1	R / W	LPT_EN Strapping result reading
0	R / W	24M_48M_SEL Strapping result reading

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

4) VSB Strapping result can be programming by LPC, and reset by RSMRST#
5) VCC Strapping result can be programming by LPC, and reset by PWROK
6) LRESET Strapping (2E_4E_SEL) : No change

23.2 Logical Device 1 (Parallel Port)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, 78h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 07h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for PRT.

CR 74h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 3Fh

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6-3	R / W	ECP FIFO Threshold.
2-0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). **Bits** **2 1 0** 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved. 1 1 1: ECP and EPP – 1.7 mode.

23.3 Logical Device 2 (UART A)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.

BIT	READ / WRITE	DESCRIPTION
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 0 0: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTA_RS485_enable** 0: Disable RS485 auto flow control function for UARTA 1: Enable RS485 auto flow control function for UARTA
6	R / W	**UARTA_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSA# pin for RS485 auto flow control. 1: Invert the behavior of RTSA# pin for RS485 auto flow control.
5-0	Reserved.	

23.4 Logical Device 3 (UART B, IR)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for IR.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.

BIT	READ / WRITE	DESCRIPTION
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: IR clock source is 2 MHz (24 MHz / 12). 0 0: IR clock source is 24 MHz (24 MHz / 1). 0 0: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: reserved. 1: Through IRRX / IRTX.
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTB_RS485_enable** 0: Disable RS485 auto flow control function for UARTB 1: Enable RS485 auto flow control function for UARTB
6	R / W	**UARTB_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSB# pin for RS485 auto flow control. 1: Invert the behavior of RTSB# pin for RS485 auto flow control.
5-0	Reserved.	

23.5 Logical Device 5 (Keyboard Controller)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET#

Default : 83h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: 12MHz 1 1: Reserved
5-3	Reserved.	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

23.6 Logical Device 6 (CIR)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 08h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R/W	CIR wide band filter select 0: Low-pass filter 1: Band-pass filter

BIT	READ / WRITE	DESCRIPTION
2-1	R/W	Timeout margin selection of CIR wide band band-pass filter 00: 200% recording carrier period 01: 100% recording carrier period 10: 50% recording carrier period 11: 25% recording carrier period
0	R/W	Carrier recording mode CIR wide band band-pass filter 0: Second carrier 1: Every carrier

CR F1h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 09h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Highest input period of CIR wide band band-pass filter (unit : us)

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 32h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Lowest input period of CIR wide band band-pass filter (unit : us)

CR F3h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Recording carrier period of CIR wide band band-pass filter (unit : us)

23.7 Logical Device 7 (GPIO6, GPIO7, GPIO8)

CR E0h. GPIO7 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 0Fh

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.

CR E1h. GPIO7 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO7 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO7 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	Read Only Read-Clear	GPIO7 Event Status Bit 7-0 corresponds to GP77-GP70, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO8 I/O Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 I/O register 0: The respective GPIO8 PIN is programmed as an output port 1: The respective GPIO8 PIN is programmed as an input port.

CR E5h. GPIO8 Data Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO8 Inversion Registe

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO8 Status Register

Location: Address E7h
Attribute: Read Only
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO8 Event Status Bit 7-0 corresponds to GP87-GP80, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR ECh. GPIO7 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	0: GPIO73 1: GPIO73 → WDTO (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO72 1: GPIO72 → SMI (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO71 1: GPIO71 → BEEP (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO70 1: GPIO70 → GRN (Please also set this GPIO to “output” type.)

CR EDh. GPIO8 Multi-function Select Register

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO87 1: GPIO87 → YLW
6	R / W	0: GPIO86 1: GPIO86 → BEEP
5	R / W	0: GPIO85 1: GPIO85 → SMI
4	R / W	0: GPIO84 1: GPIO84 → WDTO
3	R / W	0: GPIO83 1: GPIO83 → YLW
2	R / W	0: GPIO82 1: GPIO82 → BEEP
1	R / W	0: GPIO81 1: GPIO81 → SMI
0	R / W	0: GPIO80 1: GPIO80 → WDTO

CR F4h. GPIO6 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F5h. GPIO6 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. GPIO6 Inversion Register

Attribute: Read/Write
Power Well: VSB

Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. GPIO6 Status Register
Attribute: Read Only
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F8h. GPIO6 Multi-function Select Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO67 1: GPIO67 → MLED (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO66 1: GPIO66 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO65 1: GPIO65 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO64 1: GPIO64 → WDTO (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO63 1: GPIO63 → MLED (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO62 1: GPIO62 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO61 1: GPIO61 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO60 1: GPIO60 → WDTO (Please also set this GPIO to “output” type.)

23.8 Logical Device 8 (WDT1, GPIO0, GPIO1)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
2	Reserved.	
1	R / W	0: GPIO0 is inactive. 1: GPIO0 is active.
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

Note. The active and inactive register for GPIO1 is located in logic device 9, CR30, bit1.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR E0h. GPIO0 I/O Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Attribute: Read Only
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP05-GP00, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO0 Multi-function Select Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO07 1: GPIO07 → MLED (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO06 1: GPIO06 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO05 1: GPIO05 → SMI (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
4	R / W	0: GPIO04 1: GPIO04 → WDTO (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO03 1: GPIO03 → MLED (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO02 1: GPIO02 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO01 1: GPIO01 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO00 1: GPIO00 → WDTO (Please also set this GPIO to “output” type.)

CR F0h. GPIO1 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

CR F1h. GPIO1 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. GPIO1 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. GPIO1 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F4h. GPIO1 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO16 1: GPIO16 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO15 1: GPIO15 → YLW (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO14 1: GPIO14 → GRN (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO13 1: GPIO13 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO12 1: GPIO12 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO11 1: GPIO11 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO10 1: GPIO10 → GRN (Please also set this GPIO to “output” type.)

CR F5h. Watchdog Timer I(WDT1) and KBC P20 Control Mode Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Watchdog Timer I count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the Watchdog Timer I output low pulse to the KBRST# pin (PIN28) 0: Disable. 1: Enable.
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F6h. Watchdog Timer I(WDT1) Counter Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF5, bit[3], by analogy.

CR F7h. Watchdog Timer I(WDT1) Control & Status Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by mouse interrupt. 1: Watchdog Timer I is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by keyboard interrupt. 1: Watchdog Timer I is reset by keyboard interrupt.
5	Write “1” Only	Trigger Watchdog Timer I event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer I status bit 0: Watchdog Timer I is running. 1: Watchdog Timer I issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer I

23.9 Logical Device 9 (GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7	R / W	0: GPIO7 is inactive.	1: GPIO7 is active
6	R / W	0: GPIO6 is inactive.	1: GPIO6 is active
5	R / W	0: GPIO5 is inactive.	1: GPIO5 is active.
4	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
3	R / W	0: GPIO3 is inactive.	1: GPIO3 is active
2	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.
1	R / W	0: GPIO1 is inactive.	1: GPIO1 is active.
0	R / W	0: GPIO8 is inactive.	1: GPIO8 is active.

CR E0h. GPIO2 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.

CR E1h. GPIO2 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E2h. GPIO2 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. GPIO2 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO3 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR E5h. GPIO3 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E6h. GPIO3 Inversion Register

Attribute: Read/Write

Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E7h. GPIO3 Status Register
Attribute: Read Only
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

CR E9h. GPIO2 Multi-function Select Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → GRN (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO26 1: GPIO26 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO25 1: GPIO25 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO24 1: GPIO24 → OVT (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO23 1: GPIO23 → GRN (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO22 1: GPIO22 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO21 1: GPIO21 → SMI (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO20 1: GPIO20 → WDTO (Please also set this GPIO to “output” type.)

CR EAh. GPIO3 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: GPIO36 1: GPIO36 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO35 1: GPIO35 → BEEP (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO34 1: GPIO34 → SMI (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO33 1: GPIO33 → WDTO (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO32 1: GPIO32 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO31 1: GPIO31 → BEEP (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO30 1: GPIO30 → SMI (Please also set this GPIO to “output” type.)

CR EBh. GPIO5 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO56 1: GPIO56 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO55 1: GPIO55 → SLPS5_Lch (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO54 1: GPIO54 → GRN (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO53 1: GPIO53 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO52 1: GPIO52 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO51 1: GPIO51 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO50 1: GPIO50 → GRN (Please also set this GPIO to “output” type.)

CR F0h. GPIO4 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F1h. GPIO4 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F2h. GPIO4 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E8h. GPIO4 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR EEh. GPIO4 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO46 1: GPIO46 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO45 1: GPIO45 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO44 1: GPIO44 → WDTO (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO43 1: GPIO43 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO42 1: GPIO42 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO41 1: GPIO41 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO40 1: GPIO40 → WDTO (Please also set this GPIO to “output” type.)

CR F4h. GPIO5 I/O Register

Attribute: Read/Write

Power Well: VSB
Reset by: GP5X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

CR F5h. GPIO5 Data Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F6h. GPIO5 Inversion Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F7h. GPIO5 Status Register
Attribute: Read Only
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR FEh. Input Detected Type Register
Attribute: Read/Write

Power Well: VSB
Reset by: GP3X_MRST(Bit7-6), GP4X_MRST(Bit5-4)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable GP32 input de-bouncer 1: Disable GP32 input de-bouncer
6	R / W	0: Enable GP31 input de-bouncer 1: Disable GP31 input de-bouncer
5	R / W	0: Enable GP46 input de-bouncer 1: Disable GP46 input de-bouncer
4	R / W	0: Enable GP41 input de-bouncer 1: Disable GP41 input de-bouncer
3-0	Reserved	

23.10 Logical Device A (ACPI)

CR E0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Enable CIR wake-up
0: Disable CIR wake-up function via PSOUT#.
1: Enable CIR wake-up function via PSOUT#.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
<tr><td>0</td><td>R / W</td><td>KBXKEY =>
0: Only the pre-determined key combination in sequence can wake up the system.
1: Any character received from the keyboard can wake up the system.</td></tr>
</table>

CR E1h. KBC Wake-Up Index Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Attribute: Read Only
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset, PWROK(Bit4), LRESET#(Bit3-2)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	Power-loss control [Note] (These two bits will determine the system turn on or off after AC resume, from G3 to S5 state.) **Bits** **6 5** 0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before the power loss. Pease check the definition of the pre-state is "ON" or "OFF" in chapter 26.2.) 1 1: User defined mode for power loss last-state. (The last-state flag is located on "CRE6h, bit4.")
4	R / W	3VSBSW# enable bit 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for wake-up events set in CRE0. This bit is cleared when any wake-up event is captured. (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1-0	Reserved.	

Note. Whether "Always turn on", "Pre-state" or "User defined mode", the PSON#'s active condition for system to turn-on is S3# goes high. For south-bridge which S3# default is low while AC resume, please refer "CRE7h, bit4" to achieve the power-loss control application.

CR E5h. GPIOs Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	GP8X_MRST 0: GP8X reset by RSMRST#. (Default) 1: GP8X reset by SLPS5.

BIT	READ / WRITE	DESCRIPTION
4	R / W	GP7X_MRST 0: GP7X reset by RSMRST#. (Default) 1: GP7X reset by SLPS5.
3	R / W	GP6X_MRST 0: GP6X reset by RSMRST#. (Default) 1: GP6X reset by SLPS5.
2	R / W	RESETCONO# signal to control PWROK 0: Disable (Default) 1: Enable
1	R / W	Route to PWROK source selection. 0: PSON#. 1: SLP_S3#. (Default)
0	R / W	ATXPGD signal to control PWROK 0: Enable. (Default) 1: Disable.

CR E6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7, Bit5, Bit3-1), Battery reset(Bit6, Bit4), PWROK(Bit0)

Default : 1Ch

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Read Only	SKTOCC Status. This bit is ‘1’ when pin 102 SKTOCC# = 1.
5	R / W	CASEOPEN0 Clear Control. Write 1 to this bit to clear CASEOPEN0 status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF. (Default)

BIT	READ / WRITE	DESCRIPTION
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS (Default) 1 1 1: 420 ~ 560mS
0	R / W	PWROK_TRIG => 0: PWROK work normally. (Default) 1: Write 1 will let PWROK keep low or from high to low immediately.

CR E7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7-5, Bit3-2), Battery reset(Bit4, Bit1-0)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (For southbridge which S3# default is low when AC resume, like VIA, AMD…etc.) 0: Disable. (Default) 1: Enable.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Select WDT1 reset source 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2	Reserved.	
1	R / W	SKTOCC Clear Control. Write 1 to this bit to clear SKTOCC status. This bit will clear the status itself.
0	R / W	Hardware Monitor RESET source select 0: PWROK. (Default) 1: LRESET#.

CR E9h. GPIOs Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	GP5X_MRST 0: GP5X reset by RSMRST#. 1: GP5X reset by SLPS5.
4	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLPS5.
3	R / W	GP3X_MRST 0: GP3X reset by RSMRST#. 1: GP3X reset by SLPS5.
2	R / W	GP2X_MRST 0: GP2X reset by RSMRST#. 1: GP2X reset by SLPS5.
1	R / W	GP1X_MRST 0: GP1X reset by RSMRST#. 1: GP1X reset by SLPS5.
0	R / W	GP0X_MRST 0: GP0X reset by LRESET#. 1: GP0X reset by PWROK.

CR EEh.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	CASEOPEN polarity 0: None inverse CASEOPEN0/1 INPUT 1: Inverse CASEOPEN0/1 INPUT
0	R / W	CASEOPEN1 Clear Control. Write 1 to this bit to clear CASEOPEN1 status. This bit will clear the status itself.

CR F0h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	**Pin70** function selection LDA CRF0 [Bit7-5] / Pin70 000 / DEEP_S5_0 001 / 3VSBSW 010 / LATCH_BKFD_CUT 011 / ATXPGDO 1xx / PWROK
4	R / W	**Pin72** function selection LDA CRF0 [Bit4] / Pin72 0 / CASEOPEN1# 1 / DEEP_S5_1
3-0	Reserved.	

CR F1h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 48h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ASUSTEK OVP/UVP Enable
6-5	R / W	TIME_ANTIPWRD 00: 3us ~ 4us 01: 1.5s ~ 2s 10: 93.75ms ~ 125ms (Default) 11: 187.5ms ~ 250ms

BIT	READ / WRITE	DESCRIPTION
4-3	R / W	TIME_ANTIDETS3 00: 0.5s ~ 0.625s 01: 1s ~ 1.25s(Default) 10: 2s ~ 2.5s 11: 4s ~ 5s
2-1	Reserved.	
0	R / W	ASUSTEK OVP/UVP Status

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 5Ch

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#. (Default)
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#. (Default)
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#. (Default)
1	Reserved.	
0	R / W	EN_PME 0 : Disable PME. (Default) 1 : Enable PME.

CR F3h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W-Clear	PME status of the Mouse event. Write 1 to clear this status.

BIT	READ / WRITE	DESCRIPTION
4	R / W-Clear	PME status of the KBC event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	Reserved.	
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDT1 event. Write 1 to clear this status.
1	R / W-Clear	PME status of the RIA event. Write 1 to clear this status.
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F6h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#(Bit7), RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.
6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse event. 1: Enable PME interrupt of the Mouse event.
4	R / W	0: Disable PME interrupt of the KBC event. 1: Enable PME interrupt of the KBC event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.

BIT	READ / WRITE	DESCRIPTION
2	Reserved.	
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : C0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RSTOUT2# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
6	R / W	RSTOUT1# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
5	R / W	PSIN_S3_BLK EN It will filter PSIN 1sec after S3# active 0: Disable 1: Enable
4	R / W	0: Disable PME interrupt of the CIRWAKEUP IRQ event. 1: Enable PME interrupt of the CIRWAKEUP IRQ event.
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDT1 event. 1: Enable PME interrupt of the WDT1 event.
1	R / W	0: Disable PME interrupt of the RIA event. 1: Enable PME interrupt of the RIA event.
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

CR FBh. GPIO41, GPIO46, GPIO31 and GPIO32 Event Route Selection Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	DESCRIPTION
7-0	Reserved

CR FEh. GPIO41, GPIO46, GPIO31 and GPIO32 Event Route Selection Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable GP41 event route to PSOUT#. 1: Enable GP41 event route to PSOUT#.
6	R / W	0: Disable GP46 event route to PSOUT#. 1: Enable GP46 event route to PSOUT#.
5	R / W	0: Disable GP31 event route to PSOUT#. 1: Enable GP31 event route to PSOUT#.
4	R / W	0: Disable GP32 event route to PSOUT#. 1: Enable GP32 event route to PSOUT#.
3	R / W	0: Disable GP41 event route to PME#. 1: Enable GP41 event route to PME#.
2	R / W	0: Disable GP46 event route to PME#. 1: Enable GP46 event route to PME#.
1	R / W	0: Disable GP31 event route to PME#. 1: Enable GP31 event route to PME#.
0	R / W	0: Disable GP32 event route to PME#. 1: Enable GP32 event route to PME#.

23.11 Logical Device B (Hardware Monitor, Front Panel LED)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: Hardware Monitor & SB-TSI device is inactive. 1: Hardware Monitor & SB-TSI device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the SB-TSI base address <100h : FFEh> along a two-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E2h. AUXFAN0 Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN0 Duty Cycle Register

CR E3h. ANTISURGE Voltage Channel Confiugration Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : A8h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	AVCC high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%
5-4	R / W	VIN0 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%
3-2	R / W	VIN1 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%

BIT	READ / WRITE	DESCRIPTION
1	R / W	ANTISURGE Voltage Channel selection 0: VIN0 and VIN1 1: VIN2 and VIN3
0	Reserved.	

CR E4h. Configuration Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit7, Bit4-0), WDT&PWROK(Bit6), AMD_PWROK(Bit5)

Default : FFh

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>CR2A Bit1-0 reset source selection
0: WDT & PWROK
1: RSMRST#</td></tr>
<tr><td>6</td><td>R / W</td><td>RESETCONI# and PSIN# input block
0: Enable
1: Disable</td></tr>
<tr><td>5</td><td>R / W</td><td>AMD Power Sequence VCORE detect selection
0: Disable
1: Enable</td></tr>
<tr><td>4</td><td colspan="2">Reserved.</td></tr>
<tr><td>3</td><td>R / W</td><td>Pin88 function selection
<table>
<tr><th>DSW_EN</th><th>LDB CRE4 [Bit3]</th><th>EN_AS</th><th>Pin88</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>SLP_SUS_FET</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>GP55</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>PWROK#</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin93 function selection
<table>
<tr><th>DSW_EN</th><th>LDB CRE4 [Bit2]</th><th>Pin93</th></tr>
<tr><td>1</td><td>x</td><td>SUSWARN#</td></tr>
<tr><td>0</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>1</td><td>RSTOUT3#</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin91 function selection
<table>
<tr><th>DSW_EN</th><th>LDB CRE4 [Bit1]</th><th>Pin91</th></tr>
<tr><td>1</td><td>x</td><td>SUSACK#</td></tr>
<tr><td>0</td><td>0</td><td>GP52</td></tr>
<tr><td>0</td><td>1</td><td>RSTOUT4#</td></tr>
</table></td></tr>
<tr><td>0</td><td colspan="2">Reserved.</td></tr>
</table>

CR F0h. FANIN De-bouncer Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	1: Enable AUXFANIN2 input de-bouncer. 0: Disable AUXFANIN2 input de-bouncer.
4	R / W	1: Enable AUXFANIN1 input de-bouncer. 0: Disable AUXFANIN1 input de-bouncer.
3	R / W	1: Enable AUXFANIN0 input de-bouncer. 0: Disable AUXFANIN0 input de-bouncer.
2	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
1	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
0	Reserved.	

CR F1h. SMI IRQ Register
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	SMI IRQ Enable
6-0	Reserved.	

CR F2h. Deep S3 Sleeping State Front panel Green & Yellow LED control register
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	**Deep S3**_YLW_BLK_FREQ bits (This function affects by LDB CRF9 Bit 7) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. 1XXX: Fading LED.

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	**Deep S3**_GRN_BLK_FREQ bits (This function affects by LDB CRF9 Bit 6) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. 1XXX: Fading LED.

CR F5h. SMBus de-bouncer Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#, PWROK(Bit7-5)

Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	MLED Frequency 000: always high 001: always low 010: 4 Hz 011: 2 Hz 100: 1 Hz 101: 1/2 Hz 110: 1/4 Hz 111: 1/8 Hz
4	R / W	1: Enable ANTI-SURGE filter 0: Disable ANTI-SURGE filter
3-2	Reserved.	
1	R / W	1: Enable SCL input de-bouncer 160ns. 0: Disable SCL input de-bouncer.
0	R / W	1: Enable SDA input de-bouncer 160ns. 0: Disable SDA input de-bouncer.

CR F6h. Deep S5 Front Panel Green & Yellow LED control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	**Deep S5**_YLW_BLK_FREQ bits (This function affects by LDB CRF9 Bit 5) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. 1XXX: Fading LED.
3-0	R / W	**Deep S5**_GRN_BLK_FREQ bits (This function affects by LDB CRF9 Bit 4) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. 1XXX: Fading LED.

CR F7h. Front Panel Green LED (GRN_LED) control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 87h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**AUTO_EN** (Powered by VSB, RSMRST# reset , default = 1) 0: GRN_LED and YLW_LED are controlled by GRN_ LED_ RST, GRN_BLK_FREQ and YLW_LED_RST, YLW_BLK_FREQ bits. 1: GRN_LED and YLW_LED are controlled by “SLP_S5#” and “SLP_S3#”.
6	R / W	**GRN_LED_RST#** (Default= 0) 0: GRN_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: GRN_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	GRN_LED_POL 0: GRN_LED output is active low. (Default) 1: GRN_LED output is active high.
4	Reserved.	

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	**GRN_BLK_FREQ** bits (The reset depends on bit6, GRN_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. (Default) 1XXX: Fading LED.

CR F8h. Front Panel Yellow LED (YLW_LED) control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 47h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	**YLW_LED_RST#** (Default =1) 0: YLW_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: YLW_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	YLW_LED_POL 0: YLW_LED output is active low. (Default) 1: YLW_LED output is active high.
4	Reserved.	
3-0	R / W	**YLW_BLK_FREQ** bits (The reset depends on bit6,YLW_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. (Default) 1XXX: Fading LED.

CR F9h. Deep Sleep LED Eanble register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	Deep S3_YLW_BLK_FREQ : 0: Depend on setting of CRF2h, bit7~4. 1: Always output high.
6	R / W	Deep S3_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3~0. 1: Always output high.
5	R / W	Deep S5_YLW_BLK_FREQ : 0: Depend on setting of CRF6h, bit7~4. 1: Always output high.
4	R / W	Deep S5_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3~0. 1: Always output high.
3-0	Reserved.	

CR FAh.RESETCONO# and PWROK active Pulse width selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-2	R / W	RESETCONO# and PWROK active Pulse width selection 00:50ms ~ 60ms 01:100ms ~ 130ms 10:200ms ~ 260ms 11:200ms ~ 260ms
1-0	Reserved.	

CR FBh.GPIOE# status

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIOE# status. Write 1 to clear this status.
6-0	Reserved.	

23.12 Logical Device D (BCLK)

CR E0h. BCLK Configure Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	Read/Write	Description
7-6	R / W	BCLK Mode Select 00: Bypass Mode 01: Offset Mode 10: Manual Mode 11: Compare Mode
5-4	R / W	BCLK Manual Data
3-2	R / W	BCLK Offset Data (2's complement)
1-0	Reserved.	

CR E1h. BCLK I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : xx00_0000b

BIT	READ / WRITE	DESCRIPTION
7-6	Read Only	BCLK input Data
5-4	Reserved.	
3-2	Read Only	BCLK output Data
1-0	Reserved.	

CR F0h. Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	RO	Mask WDT1 to affect PWROK 0: Mask enable. (WDT1 not affect PWROK) 1: Mask disable. (WDT1 default affect PWROK)
6-0	Reserved.	

23.13 Logical Device E (CIR WAKE-UP)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Wake-up is inactive. 1: CIR Wake-up Interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Wake-up Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR Wake-up.

23.14 Logical Device F (GPIO Push-pull or Open-drain selection)

CR E0h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP1 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E1h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP2 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E2h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GP3 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E3h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP4 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E4h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP5 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E5h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP6 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E6h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 0Fh

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	GP7 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E7h.
Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP8 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E9h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR F0h. I2C Control & Address Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 9Dh

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable I2C_Slave
6-0	R / W	I2C Address

CR F1h. I2C to 80PORT Control Register
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	80PORT Display 0: Enable 1: Disable
0	R / W	LPC or I2C to 80PORT switch

CR F2h. I2C to 80PORT Data Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

23.15 Logical Device 14 (PORT80 UART)

CR E0h. PORT80 UART Control Register

Location: Address E0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved.	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length selecion) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved.	

CR E1h. PORT80 UART Status Register

Location: Address E1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Location: Address E2h
Attribute: Read/Write
Power Well: VCC

Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte
Location: Address E3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer
Location: Address E4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

23.16 Logical Device 16 (Deep Sleep)

CR 30h. Deep Sleep configuration register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 20h

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_SLPSUS_PULLUP (test mode) 0: Enable pin 89 (SLP_SUS#) internal pull-up. 1: Disable pin 89 (SLP_SUS#) internal pull-up.
6	R / W	RSMRST# Detect Source Select for Deep Sleep Mode. 0: RSMRST# detected source from PSOUT# voltage (Pin60). 1: RSMRST# detected source from PCHVSB voltage (Pin97). **Note**. Set to 0, if Deep S5 is enabled. Set to 1, if DSW is enabled.
5	R / W	Deep_s3_opt 0: When enter Deep S3 state, the SUS_WARN_5VDUAL will keep low. 1: When enter Deep S3 state, the SUS_WARN_5VDUAL will follow DSW sequence.
4	R / W	dsw_wake_opt (test mode) 0: The PSOUT# will assert until SLPS3# high when deep s5 wakeup event happened. 1: The PSOUT# will assert until RSMRST_L high and SLP_SUS_L high when deep s5 wakeup event happened. **PS. This bit only active when PCH_DSW_EN & (Deep S5 Enable | Deep S3 Enable)**
3	R / W	PCH DSW Enable 0: If PCH disable DSW function. 1: if PCH enable DSW function. (SLP_SUS# affects RSMRST#)
2	R / W	Reserved.
1	R / W	Deep S3 Enable 0: If SLP_S3# state will not enter Deep S3 state. 1: If SLP_S3# state will enter Deep S3 state.
0	R / W	Deep S5 Enable 0: Disable Deep S5 function when into S5 state (SLP_S5#). 1: Enable Deep S5 function when into S5 state (SLP_S5#).

CR E0h. Deep Sleep wake up PSOUT# delay time

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **20h** (Default: 512ms)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : **04h** (Default: 128 ms)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Deep Sleep Delay Time Control

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 05h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6-0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

24. SPECIFICATIONS

24.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

24.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	μA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	IVCC			25	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
Vtt Quiescent Current	IVTT			1	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V VTT = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
AIN – Analog input						
AOUT – Analog output						
IN_{tp3} – 3.3V TTL-level input pin						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{gp5} – 5V GTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OD8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
O12 – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD12 – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O24 – Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD24 – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
O48 – Output pin with 48mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -48 mA
OD48 – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	$0.275*V_{tt}$		$0.5*V_{tt}$	V	
Input High Voltage	V_{IH}	$0.55*V_{tt}$		$0.725*V_{tt}$	V	
Output Low Voltage	V_{OL}			$0.25*V_{tt}$	V	
Output High Voltage	V_{OH}	$0.75*V_{tt}$			V	
Hysterisis	V_{Hys}	$0.1*V_{tt}$			V	
O12cu – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD12cu – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

25. AC CHARACTERISTICS

25.1 Power On / Off Timing

	T1	T2	T3	T4
IDEAL TIMING	48ms~66ms	Over 64ms at least	< 10ns	15ms~32ms

25.2 AC Power Failure Resume Timing

(1) Logical Device A, CR [E4h] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)

(2) Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.
(“ON” means the system is always turned on after AC power loss recovered.)

**** What's the definition of former state at AC power failure?**

1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V

2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6791D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

25.3 CPUVCORE & VCOREREFIN Timing

When CPUVCORE (Tolerance +/- 100mv) is ovet than VCOREREFIN last for 10u second, PSON# will be immediate locked in the high state when EN_AS=1. This situation can only reset by RSMRST#.

25.4 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%

PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

25.5 PECI Timing

SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	

t_{H1}	0.6	3/4	0.8	× t_{BIT}
t_{H0}	0.2	1/4	0.4	× t_{BIT}

25.6 SMBus Timing

25.7 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	T_{SINT}		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	T_{RINT}		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	T_{IRS}		1/16	8/16	Baud Rate
Delay from to Reset interrupt	T_{HR}			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	T_{SI}		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	T_{STI}			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	T_{IR}		8	250	nS
Delay from $\overline{IOR}$ to Output	T_{MWO}		6	200	nS
Set Interrupt Delay from Modem Input	T_{SIM}		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	T_{RIM}		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

UART Transmitter Timing

25.8 Modem Control Timing

Modem Control Timing

25.9 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS

$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

25.9.1 Parallel Port Timing

Parallel Port Timing

25.9.2 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

25.9.3 EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)

25.9.4 EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)

25.9.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid	t22	0		nS
$\overline{WRITE}$ to Command Asserted	t16	5	35	nS

25.9.6 EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)

25.9.7 EPP Data or Address Write Cycle (EPP Version 1.7)

EPP Data or Address Write Cycle (EPP Version 1.7)

25.9.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

25.9.9 Parallel FIFO Timing

Parallel FIFO Timing

25.9.10ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

25.9.11ECP Parallel Port Forward Timing

ECP Parallel Port Forward Timing

25.9.12ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

25.9.13ECP Parallel Port Reverse Timing

ECP Parallel Port Reverse Timing

25.9.14KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–16 Mhz)	63	167	nS

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

25.9.15Writing Cycle Timing

Write Cycle Timing

25.9.16Read Cycle Timing

Read Cycle

25.9.17Send Data to K/B

Send Data to K/B

25.9.18Receive Data from K/B

Receive Data from K/B

25.9.19Input Clock

Input Clock

25.9.20Send Data to Mouse

Send Data to Mouse

25.9.21Receive Data from Mouse

Receive Data from Mouse

25.10 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns

Note: Refer to Microprocessor Interface Timing for Read Timing.

25.10.1 GPIO Write Timing

GPIO Write Timing diagram

26. TOP MARKING SPECIFICATIONS

1st line: Nuvoton logo
2nd line: part number NCT6791D
3rd line: wafer production series lot number 28201234
4th line: tracking code 123G9AFA

123: packages made in 2011, week 23
G: assembly house ID; G means GR, A means ASE, etc.
9: code version; 9 means code 009
A: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use.

27. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6791D	128Pin LQFP (Green package)	Commercial, 0°C to +70°C

28. PACKAGE SPECIFICATION

COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-pin LQFP (14mm x 14mm x 1.4mm)

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.3	06/27/2011	N.A.	Draft datasheet to define features and pin configuration
0.5	10/13/2011	N.A.	Update the datasheet “For ASUS Only” to version 0.5
0.6	11/9/2011	N.A	Correct information

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