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1.CFast and mSATA CO-LAY  
2.mSATA and Mini Card CO-LAY  
(BOM Change)

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Project Number : E130607  
Production Line : Sub.ESB.AASM

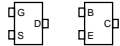
SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_S0_SC[00]	1.8V Core	20k,L	SATA_GP[0]
GPIO_S0_SC[01]	1.8V Core	20k,L	SATA_GP[1]
GPIO_S0_SC[07]	1.8V Core	20k,H	SD3_WP
GPIO_S0_SC[55]	1.8V Core	20k,L	
GPIO_S0_SC[56]	1.8V Core		--
GPIO_S0_SC[57]	1.8V Core	20k,H	
GPIO_S0_SC[58]	1.8V Core	20k,L	
GPIO_S0_SC[59]	1.8V Core	20k,L	LVDS_RBIT0
GPIO_S0_SC[60]	1.8V Core	20k,L	LVDS_RBIT1
GPIO_S0_SC[61]	1.8V Core	20k,H	LVDS_RBIT2
GPIO_S0_SC[92]	1.8V Core	20k,H	LVDS_RBIT3
GPIO_S0_SC[93]	1.8V Core	20k,H	LVDS_RBIT4
GPIO_S0_SC[94]	1.8V Core	20k,L	TOUCH_INT_1P8
GPIO_S0_SC[95]	1.8V Core	20k,L	TOUCH_RST#_1P8
GPIO_S5[00]	1.8V Suspend	20k,H	WAKE_RI#
GPIO_S5[01]	1.8V Suspend	20k,H	GPIO_PME#
GPIO_S5[02]	1.8V Suspend	20k,H	
GPIO_S5[03]	1.8V Suspend	20k,H	
GPIO_S5[04]	1.8V Suspend	20k,L	
GPIO_S5[05]	1.8V Suspend	20k,L	
GPIO_S5[06]	1.8V Suspend	20k,L	
GPIO_S5[07]	1.8V Suspend	20k,L	
GPIO_S5[08]	1.8V Suspend	20k,L	
GPIO_S5[09]	1.8V Suspend	20k,L	
GPIO_S5[10]	1.8V Suspend	20k,H	
GPIO_S5[17]	1.8V Suspend	20k,H	
GPIO_S5[22]	1.8V Suspend	20k,L	V3.3A_TCHC_EN
GPIO_S5[23]	1.8V Suspend	20k,L	
GPIO_S5[24]	1.8V Suspend	20k,L	
GPIO_S5[25]	1.8V Suspend	20k,L	
GPIO_S5[26]	1.8V Suspend	20k,L	
GPIO_S5[27]	1.8V Suspend	20k,H	
GPIO_S5[28]	1.8V Suspend	20k,H	
GPIO_S5[29]	1.8V Suspend	20k,H	
GPIO_S5[30]	1.8V Suspend	20k,H	

SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
CMOS Backup EEPROM	AEh
GPIO IC	6Eh
PTN3460 Slave	C0h

PCB Footprints



PCB STACK :

Impedence 55ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : Signal
- Layer 5 : POWER
- Layer 6 : Signal
- Layer 7 : GND
- Layer 8 : Solder

F81866D GPIO Pins :

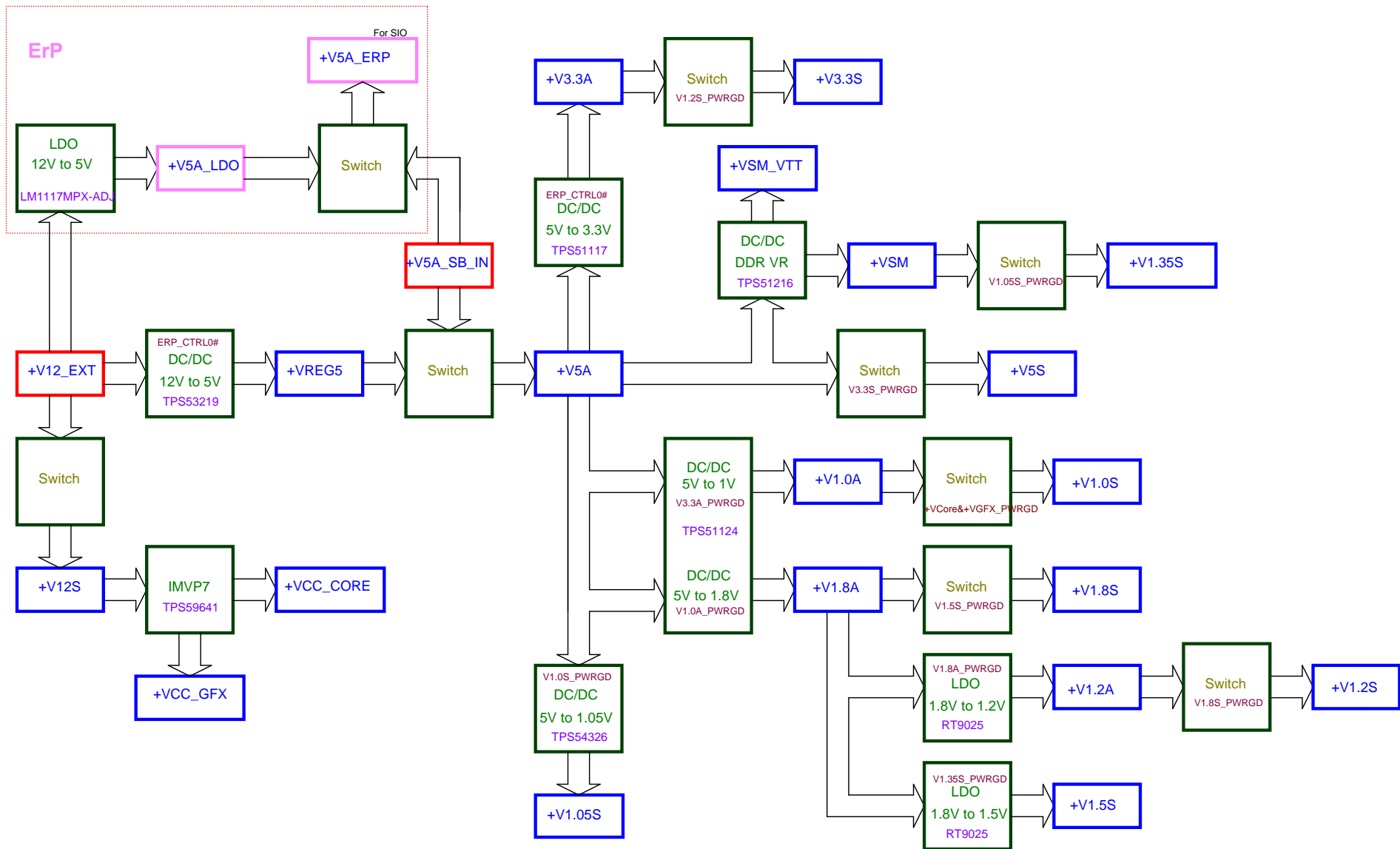
Name	Tolerance	Power Well	Default	Function
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#
GPIO02	5V	I_VSB3V	Native	PM_SUS_WARN#
GPIO03	5V	I_VSB3V	Native	PM_SUS_ACK#
GPIO04	5V	I_VSB3V	Native	PM_SLP_SUS#
GPIO05	5V	I_VSB3V	Native	LAN1_DISABLE#
GPIO06	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO07	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO10	5V	I_VSB3V	Native	W_DISABLE1#
GPIO11	5V	I_VSB3V	Native	EN_USB
GPIO12	5V	I_VSB3V	Native	DIS_TOUCH#
GPIO13	5V	I_VSB3V	Native	
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP
GPIO15	5V	I_VSB3V	Native	WDT_RST#
GPIO16	5V	I_VSB3V	Native	
GPIO17	5V	I_VSB3V	Native	SIO_PECI
GPIO20	5V	I_VSB3V	Native	
GPIO21	5V	I_VSB3V	Native	
GPIO22	5V	I_VSB3V	Native	EXT_PWRBTN#
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#
GPIO24	5V	I_VSB3V	Native	PM_SLP_S3#
GPIO25	5V	I_VSB3V	Native	PSON#
GPIO26	5V	VBAT	Native	PWOK
GPIO27	5V	VBAT	Native	SIO_RSMRST#
GPIO30	5V	3VCC	Native	DCD3#
GPIO31	5V	3VCC	Native	RI3#
GPIO32	5V	3VCC	Native	CTS3#
GPIO33	5V	3VCC	Native	DTR3#
GPIO34	5V	3VCC	Native	RTS3#
GPIO35	5V	3VCC	Native	DSR3#
GPIO36	5V	3VCC	Native	TX3#
GPIO37	5V	3VCC	Native	RX3#
GPIO40	5V	3VCC	Native	DCD4#
GPIO41	5V	3VCC	Native	RI4#
GPIO42	5V	3VCC	Native	CTS4#
GPIO43	5V	3VCC	Native	DTR4#
GPIO44	5V	3VCC	Native	RTS4#
GPIO45	5V	3VCC	Native	DSR4#
GPIO46	5V	3VCC	Native	TX4#
GPIO47	5V	3VCC	Native	RX4#
GPIO50	5V	3VCC	Native	DIO_0
GPIO51	5V	3VCC	Native	DIO_1
GPIO52	5V	3VCC	Native	DIO_2
GPIO53	5V	3VCC	Native	DIO_3
GPIO54	5V	3VCC	Native	DIO_4
GPIO55	5V	3VCC	Native	DIO_5
GPIO56	5V	3VCC	Native	DIO_6
GPIO57	5V	3VCC	Native	DIO_7
GPIO60	5V	3VCC	Native	
GPIO61	5V	3VCC	Native	
GPIO62	5V	3VCC	Native	
GPIO63	5V	3VCC	Native	
GPIO64	5V	3VCC	Native	
GPIO65	5V	I_VSB3V	Native	LPC_PME#
GPIO66	5V	VBAT	Native	DPWROK
GPIO67	5V	I_VSB3V	Native	PM_SLP_S5#
GPIO70	5V	3VCC	Native	PE
GPIO71	5V	3VCC	Native	BUSY
GPIO72	5V	3VCC	Native	ACK#
GPIO73	5V	3VCC	Native	SLIN#
GPIO74	5V	3VCC	Native	PINIT#
GPIO75	5V	3VCC	Native	ERR#
GPIO76	5V	3VCC	Native	AFD#
GPIO77	5V	3VCC	Native	STB#
GPIO80	5V	3VCC	Native	PD0
GPIO81	5V	3VCC	Native	PD1
GPIO82	5V	3VCC	Native	PD2
GPIO83	5V	3VCC	Native	PD3
GPIO84	5V	3VCC	Native	PD4
GPIO85	5V	3VCC	Native	PD5
GPIO86	5V	3VCC	Native	PD6
GPIO87	5V	3VCC	Native	PD7

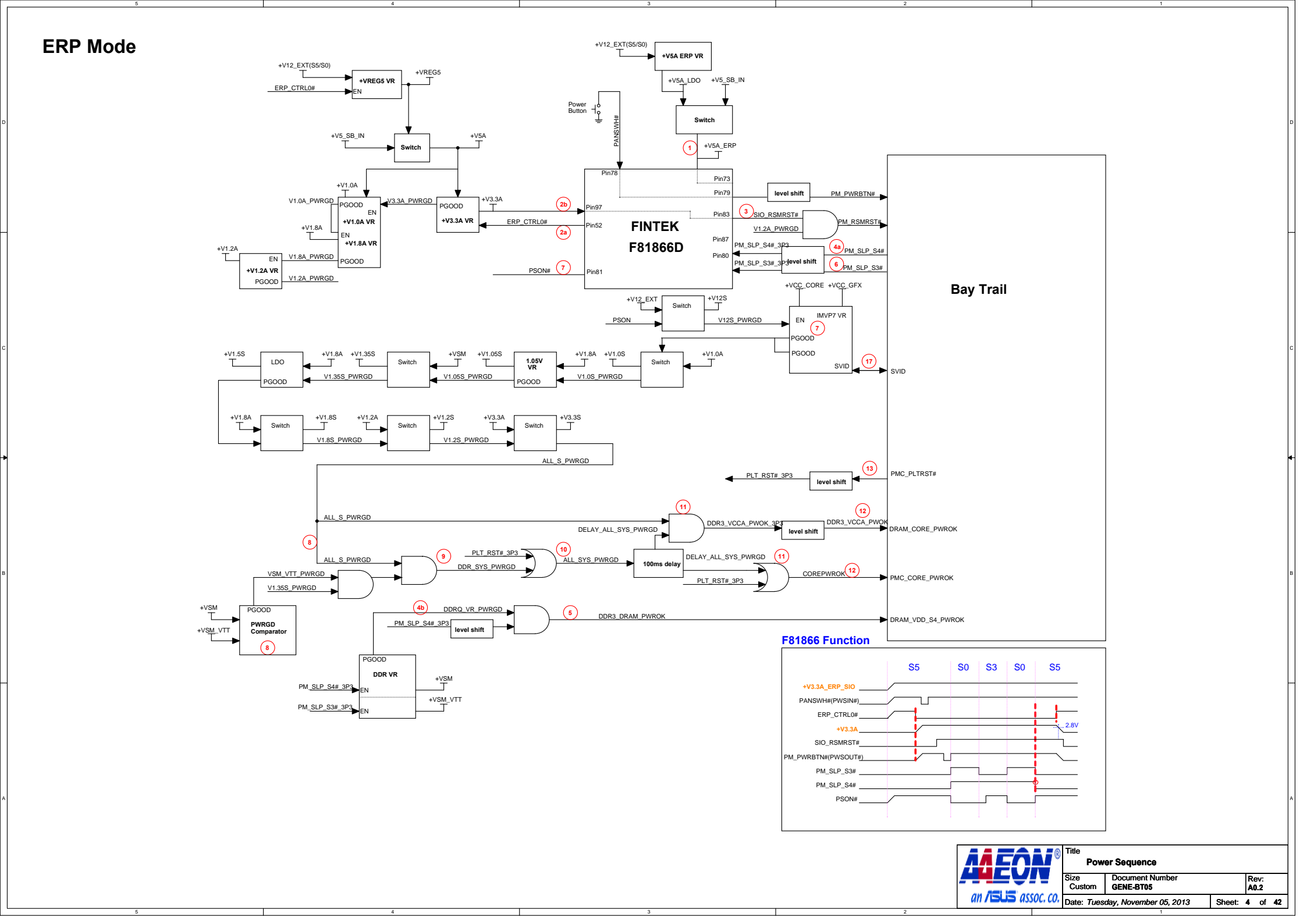
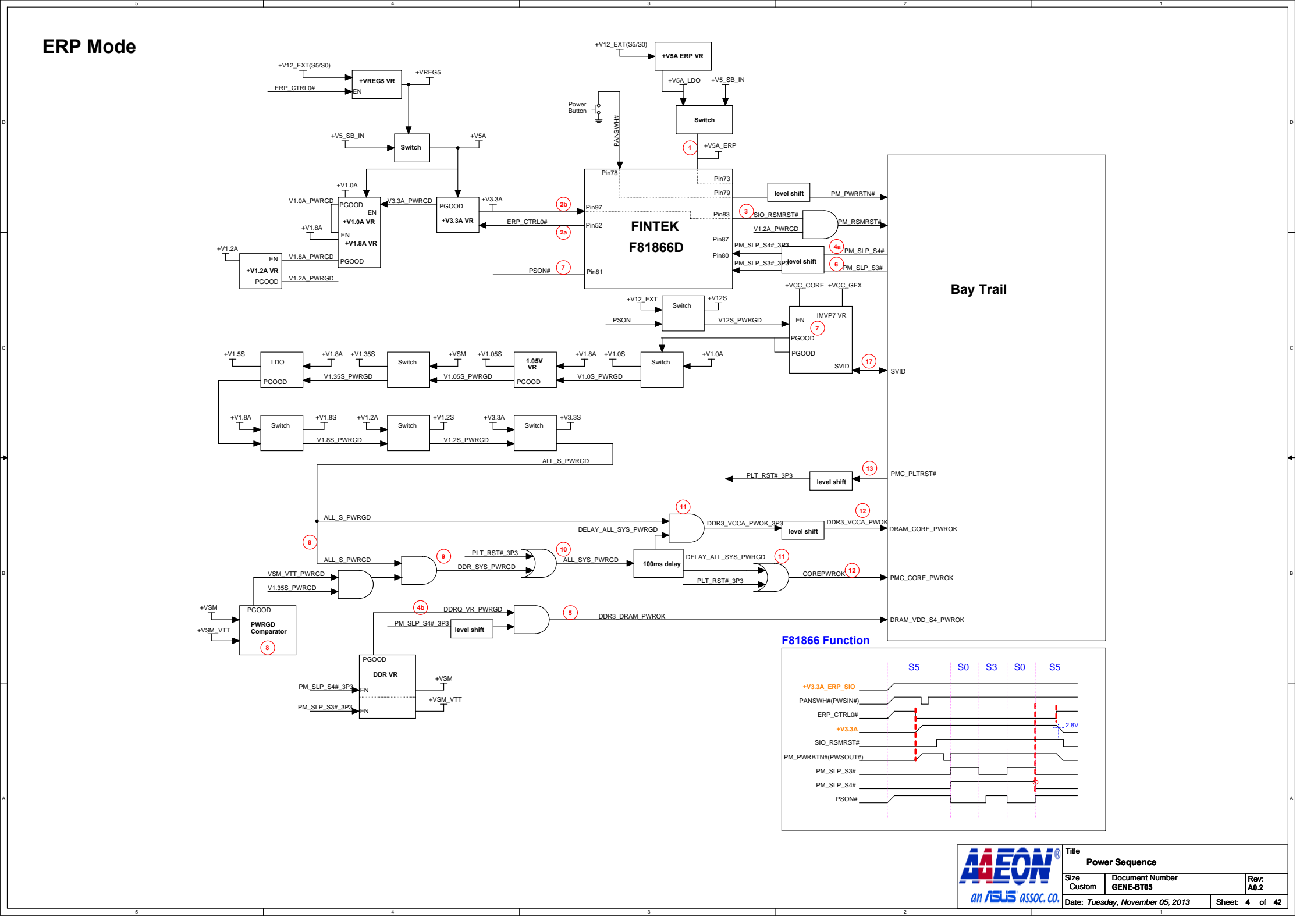
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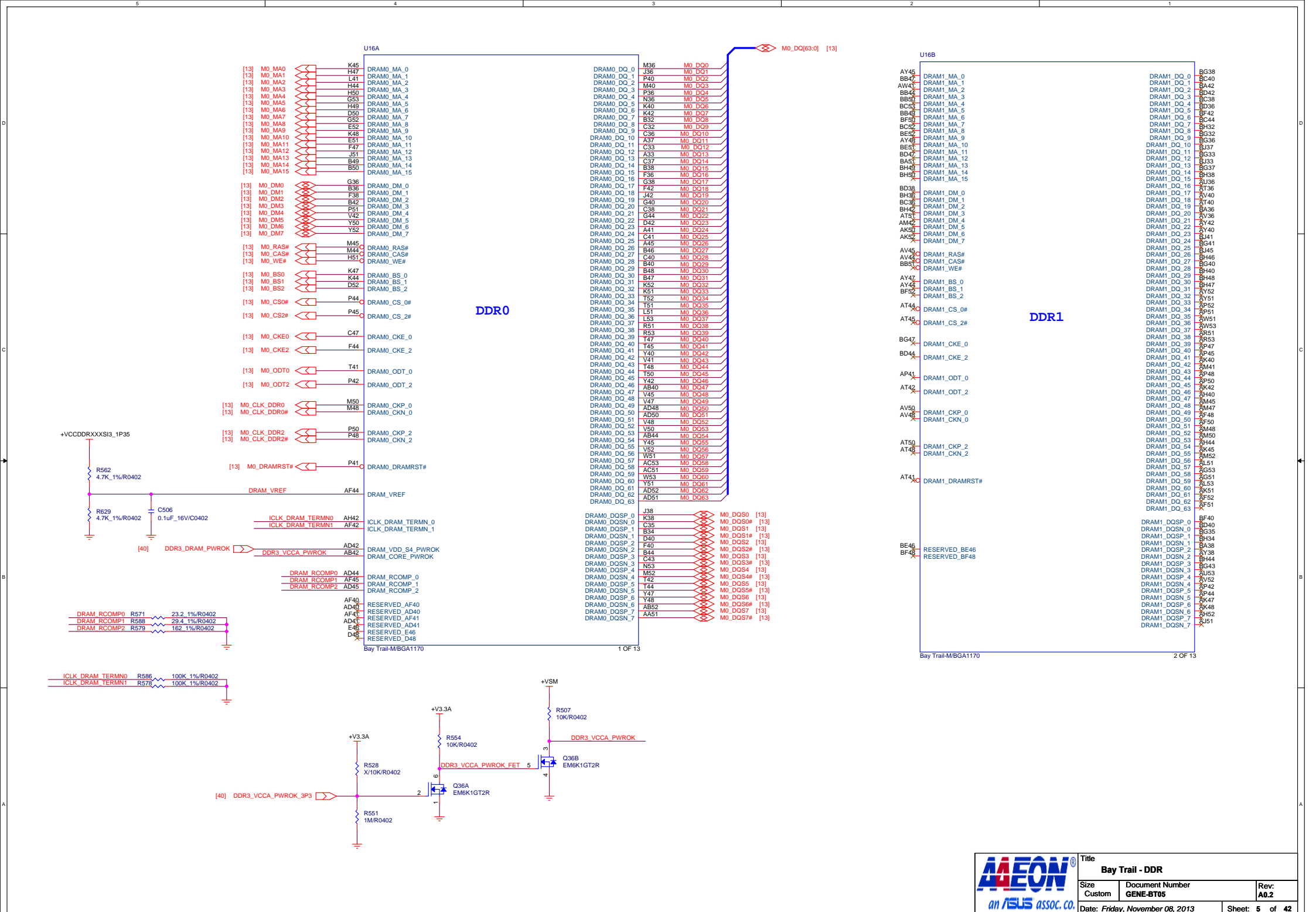
Name	Tolerance	Power Well	Default	Function
GPIO10	5V	VSB3V	Native	BOARDID_BIT0
GPIO11	5V	VSB3V	Native	ADM213_EN
GPIO12	5V	VSB3V	Native	81438_SD
GPIO13	5V	VSB3V	Native	
GPIO14	5V	VSB3V	Native	BOARDID_BIT1
GPIO15	5V	VSB3V	Native	BOARDID_BIT2
GPIO16	5V	VSB3V	Native	BOARDID_BIT3
GPIO17	5V	VSB3V	Native	BOARDID_BIT4
GPIO20	5V	VSB3V	Native	SEL_COM2_MD0
GPIO21	5V	VSB3V	Native	SEL_COM2_MD1
GPIO22	5V	VSB3V	Native	COM2_SLEW
GPIO23	5V	VSB3V	Native	SEL_COM3_MD0
GPIO24	5V	VSB3V	Native	SEL_COM3_MD1
GPIO25	5V	VSB3V	Native	COM3_SLEW
GPIO26	5V	VSB3V	Native	
GPIO27	5V	VSB3V	Native	
GPIO30	5V	VSB3V	GPIO	LVDS_EN
GPIO31	5V	VSB3V	GPIO	LVDS_CFG1
GPIO32	5V	VSB3V	GPIO	LVDS_CFG2
GPIO33	5V	VSB3V	GPIO	LVDS_Pd#

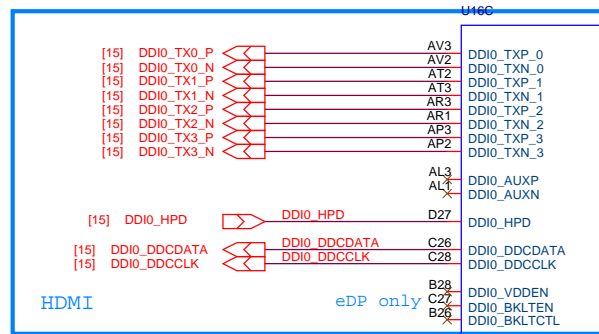


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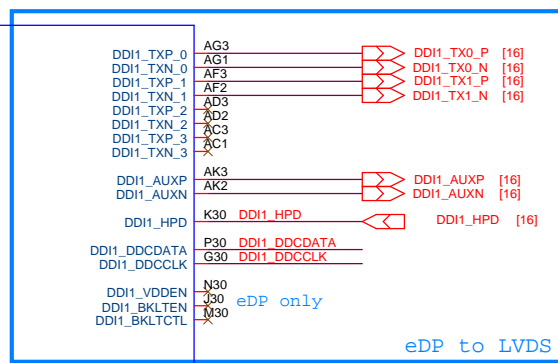


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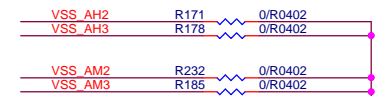
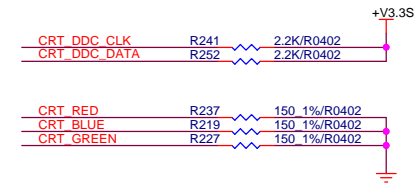




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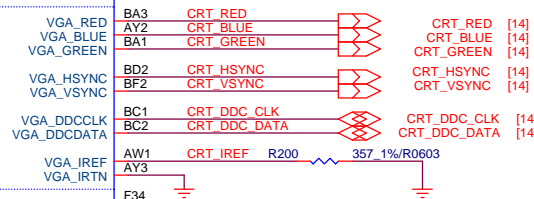


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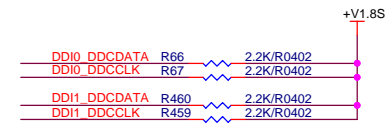
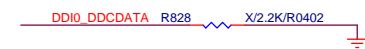
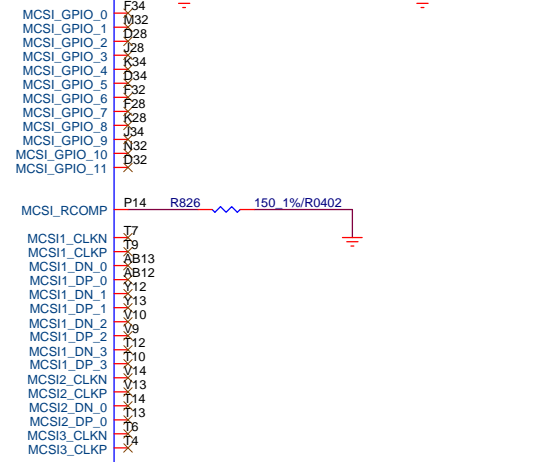


## RESERVED

## VGA



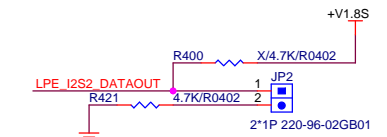
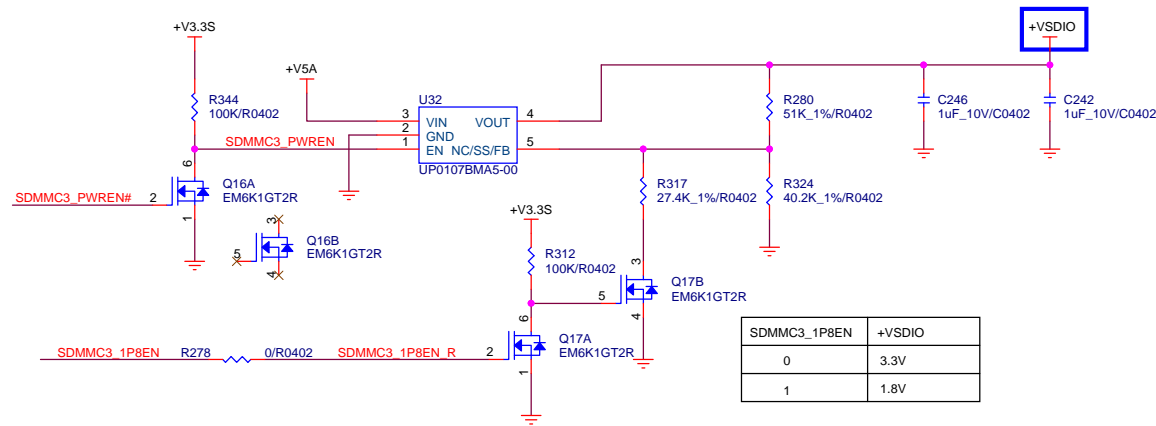
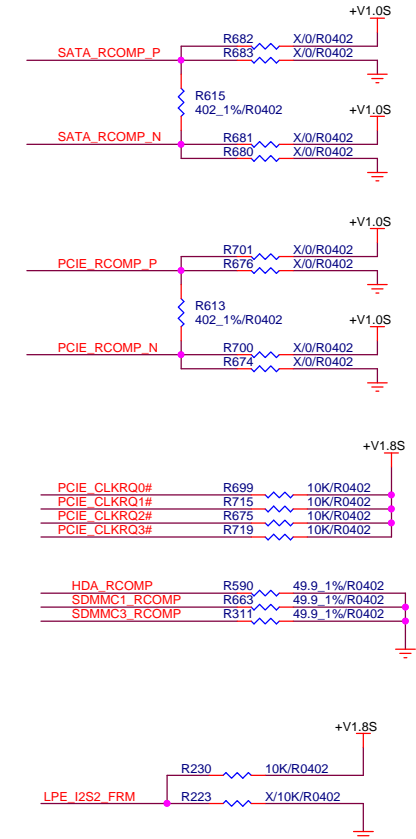
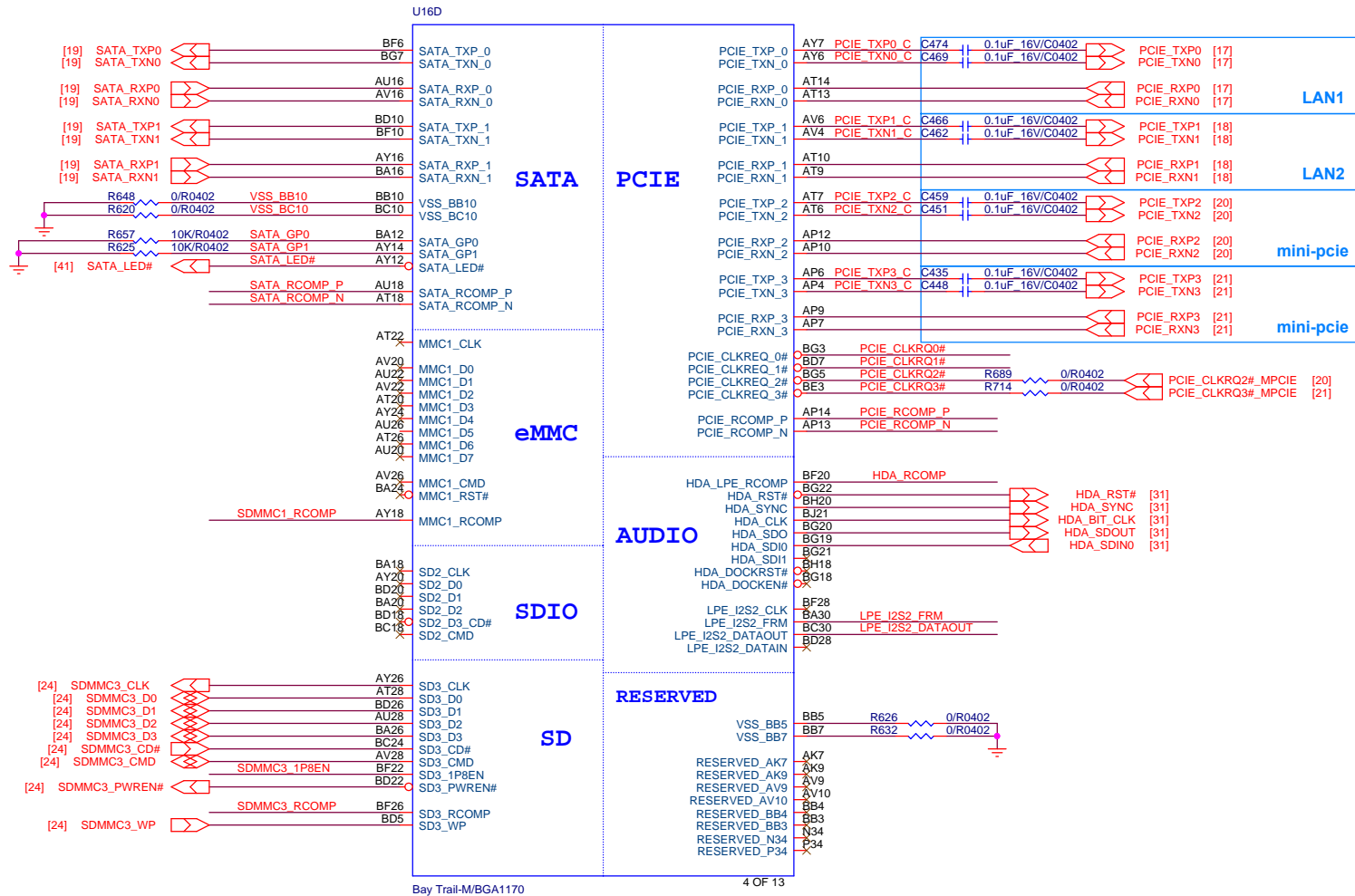
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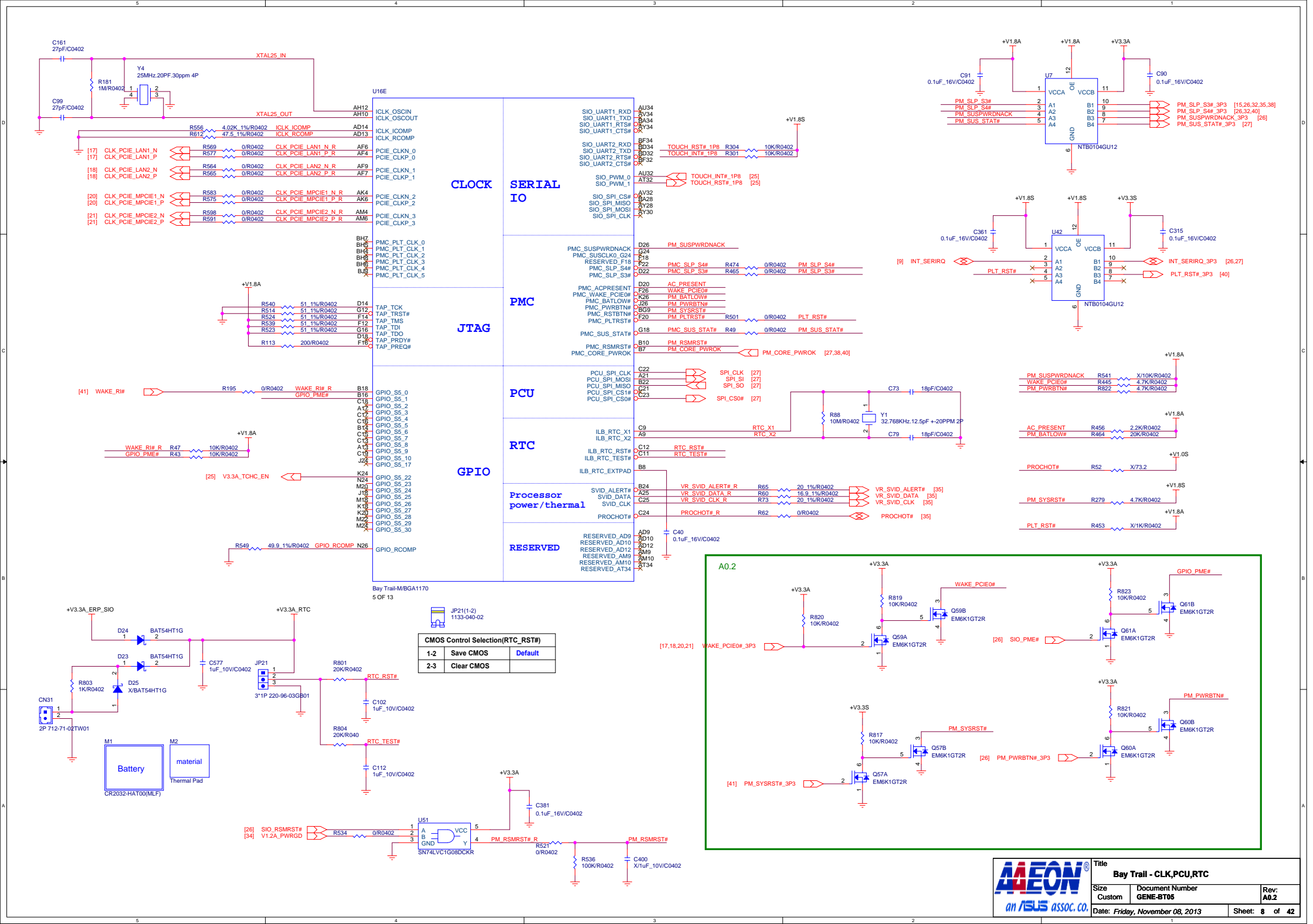


Bay Trail-M/BGA1170  
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Title <b>Bay Trail - CRT_DDI</b>		
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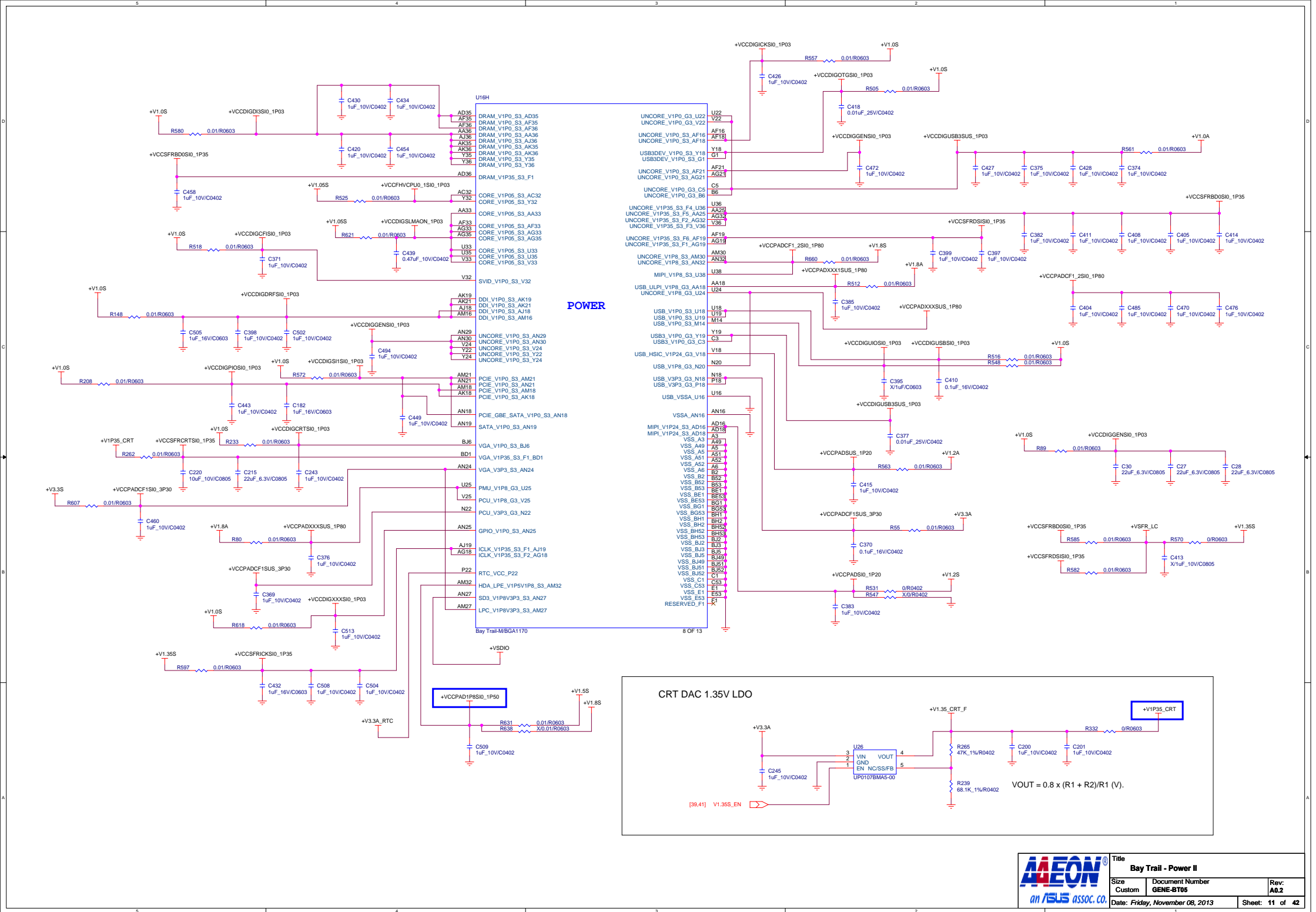


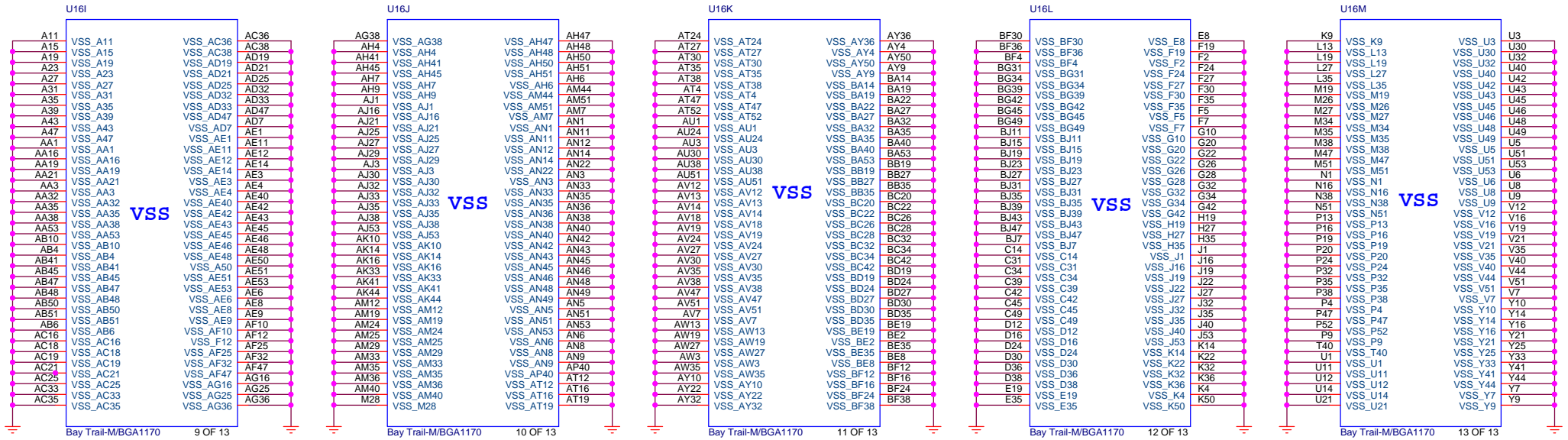




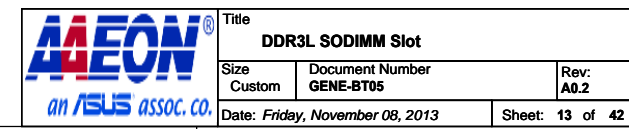




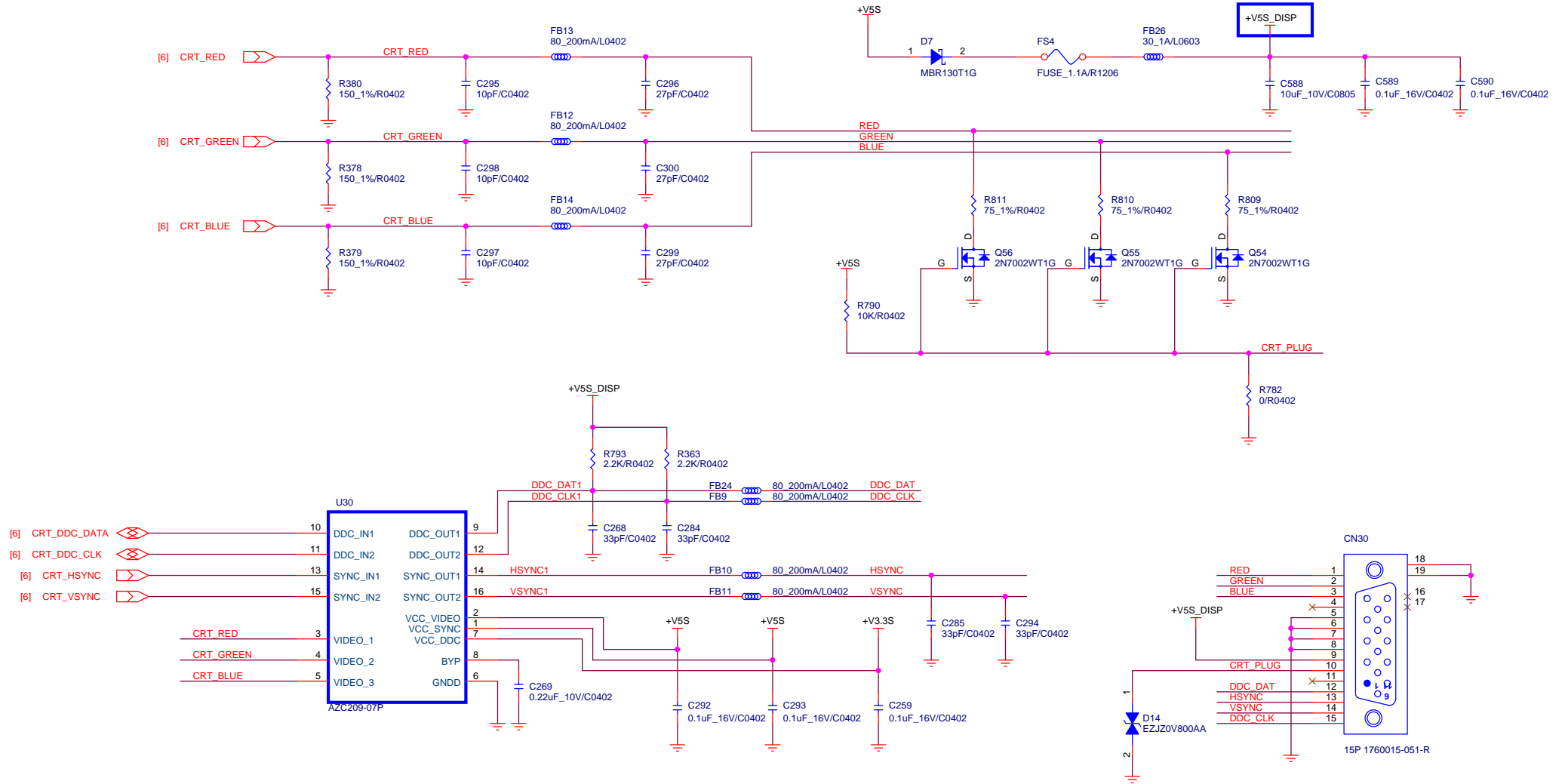




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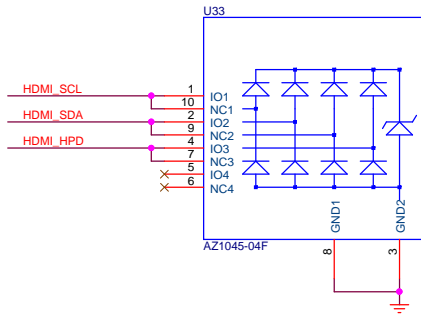
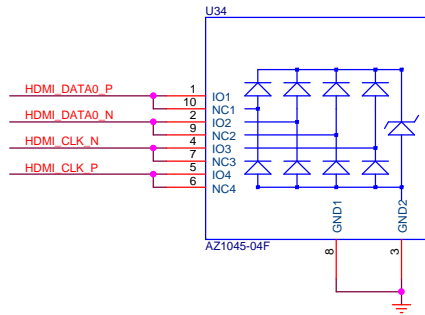
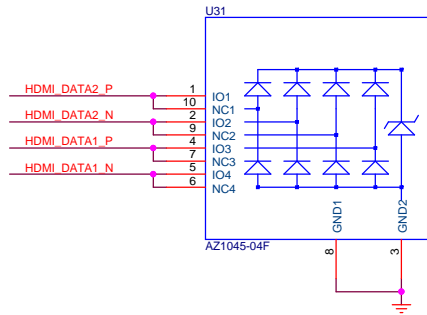
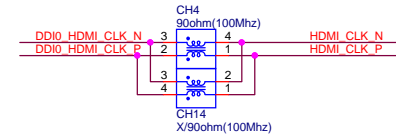
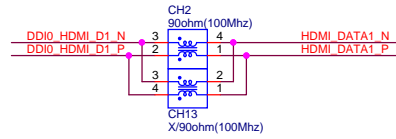
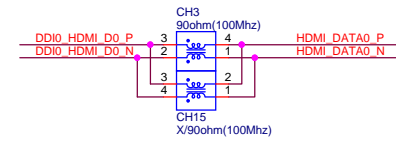
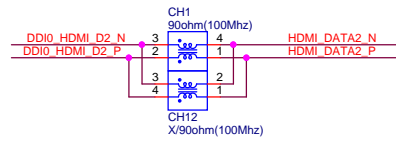
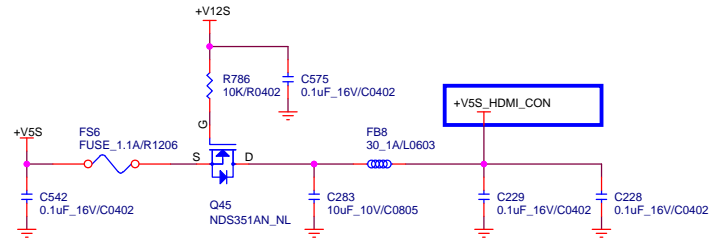
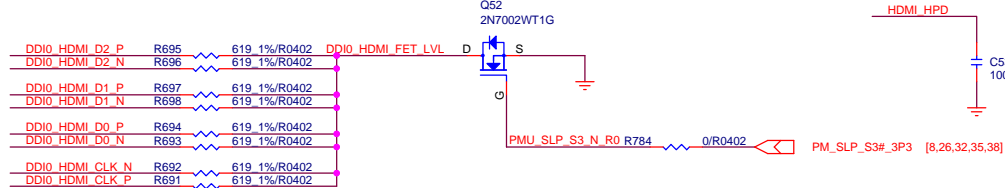
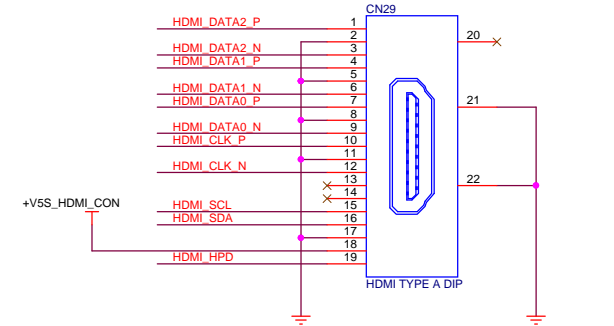
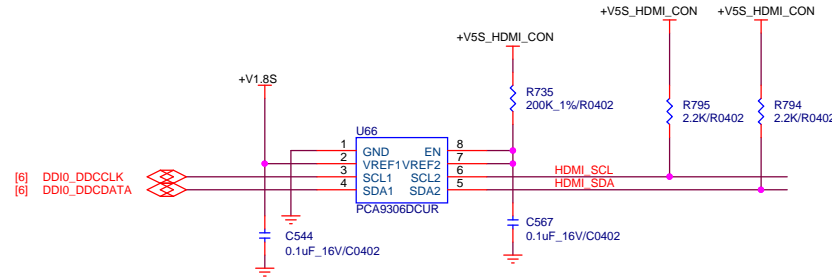
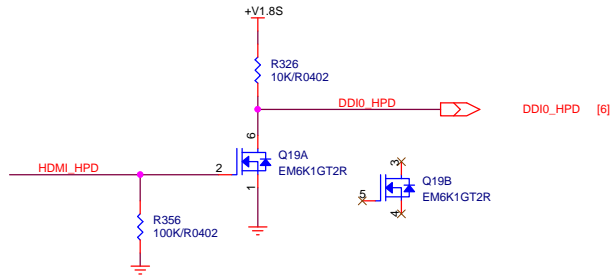


# CRT



# HDMI

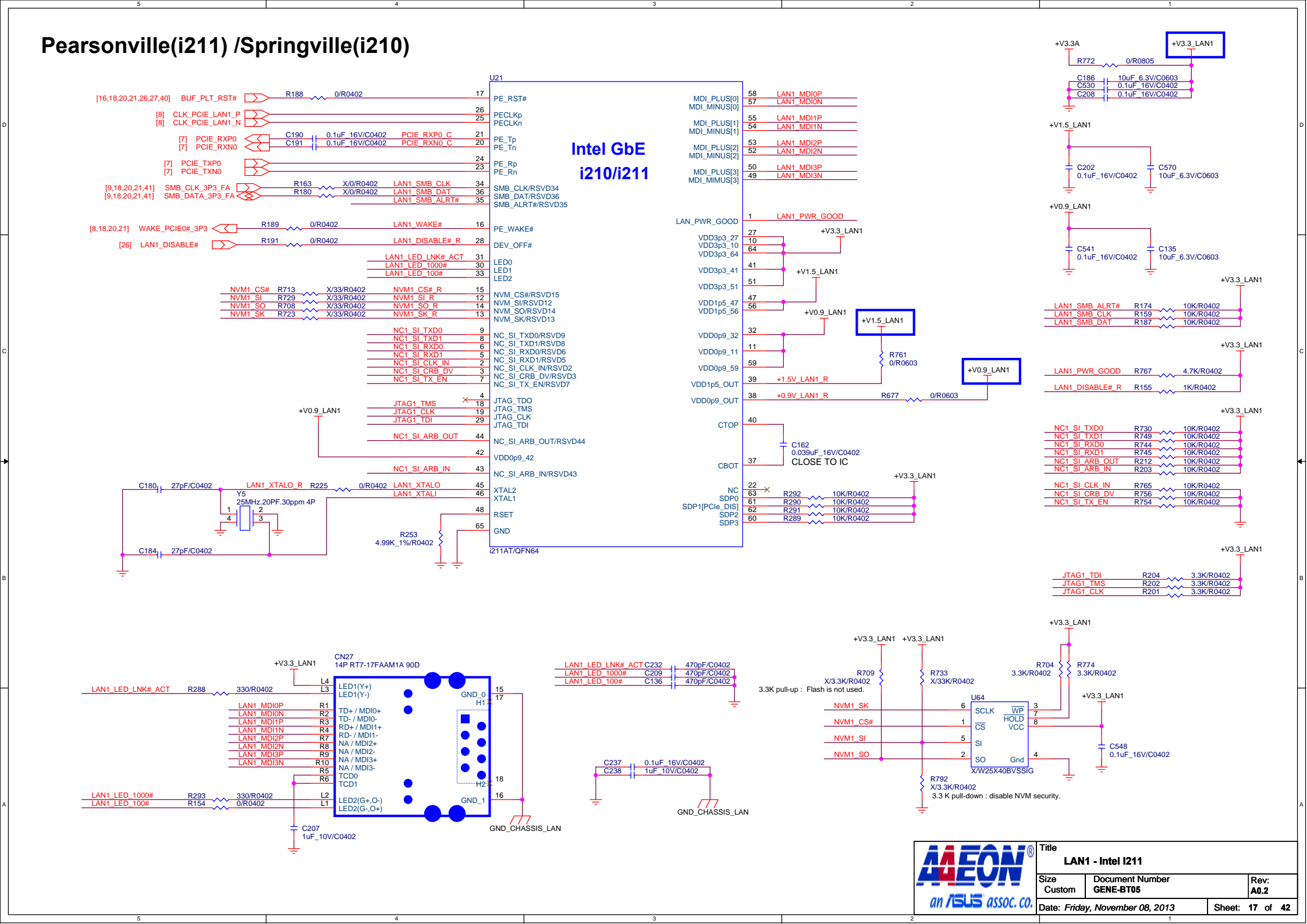
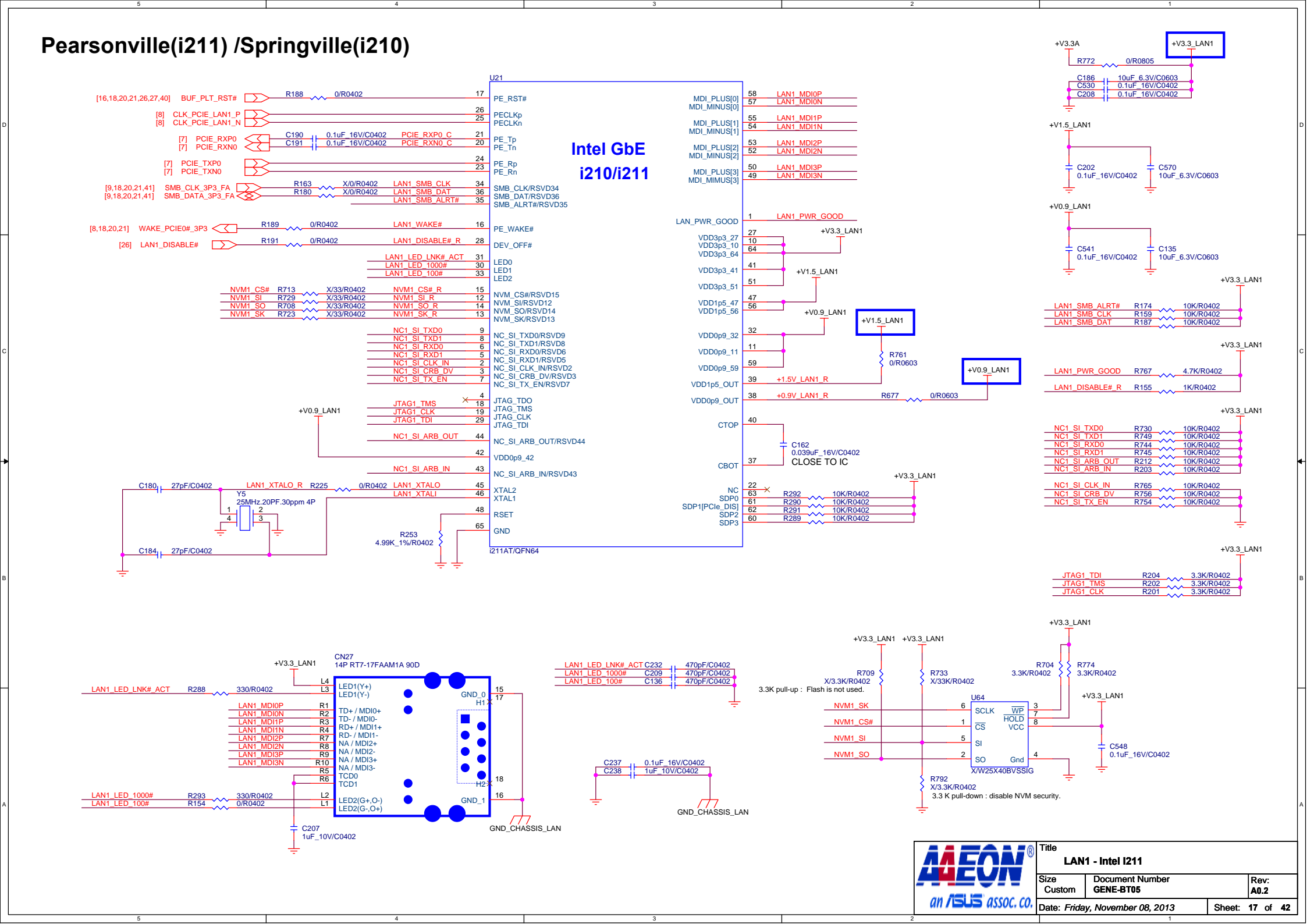
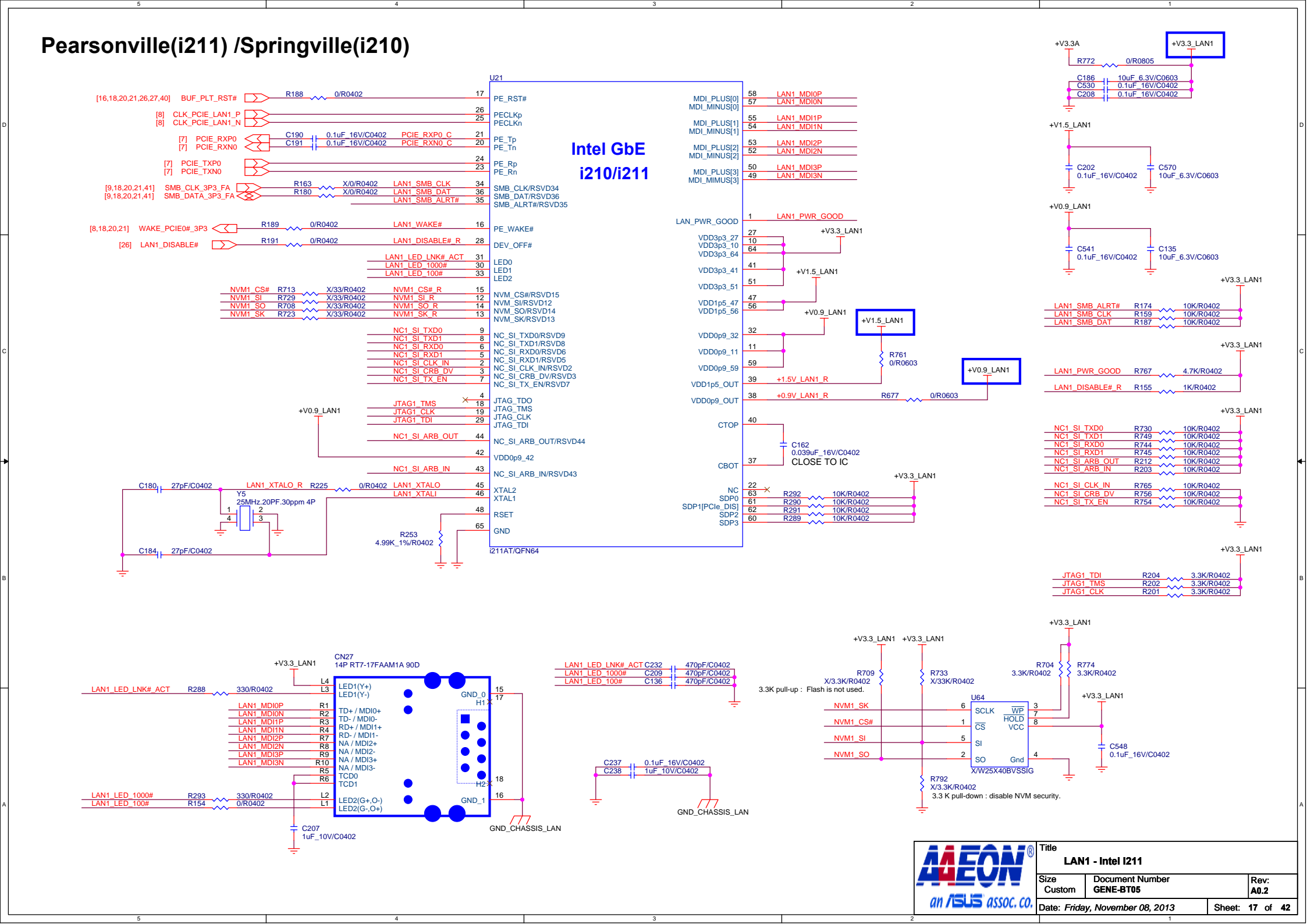
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[6] DDIO_TX1_P	C277	0.1uF 16V/C0402	DDIO_HDMI_D1_P
[6] DDIO_TX1_N	C278	0.1uF 16V/C0402	DDIO_HDMI_D1_N
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[6] DDIO_TX3_P	C271	0.1uF 16V/C0402	DDIO_HDMI_CLK_P
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Title <b>HDMI</b>		
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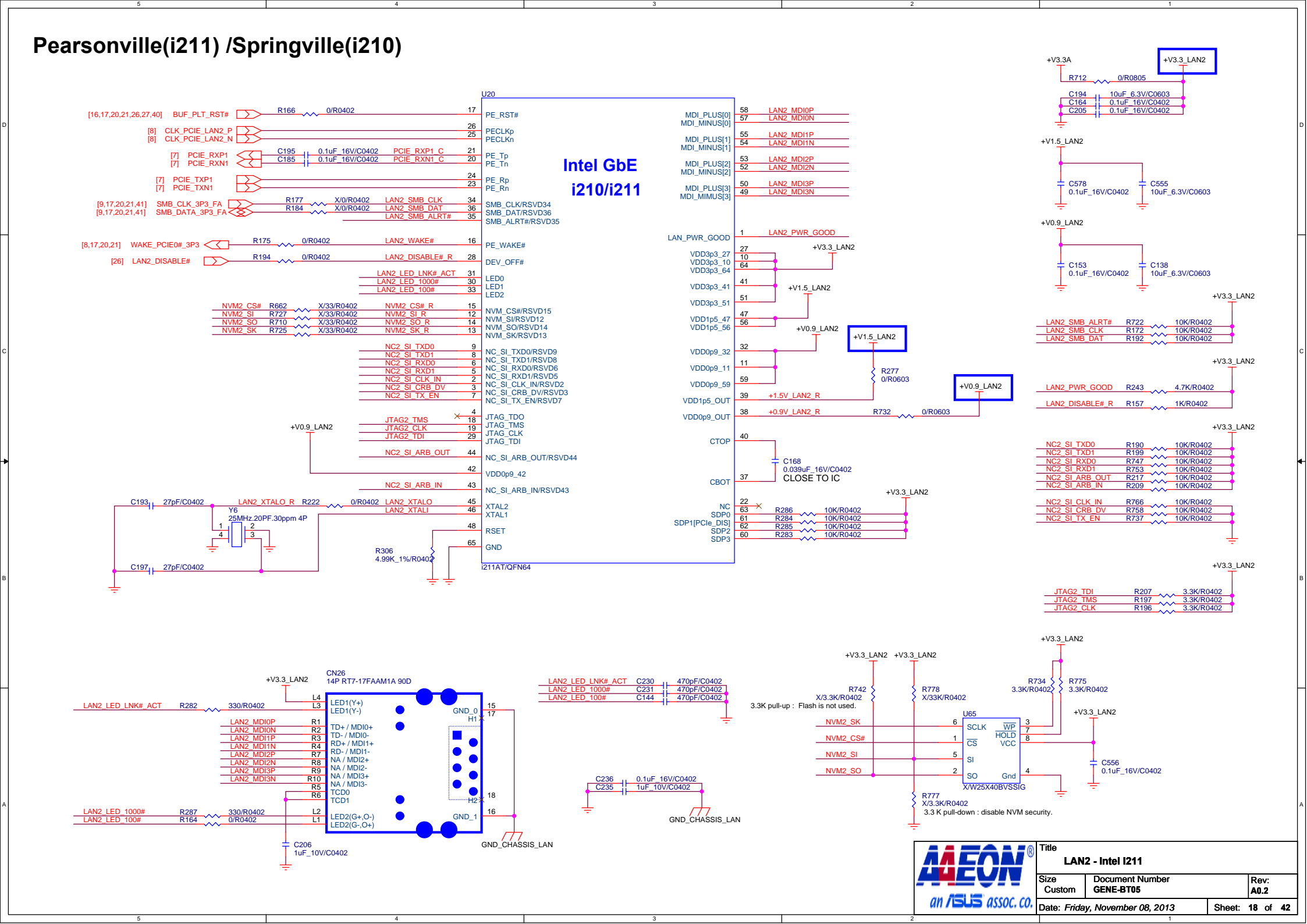
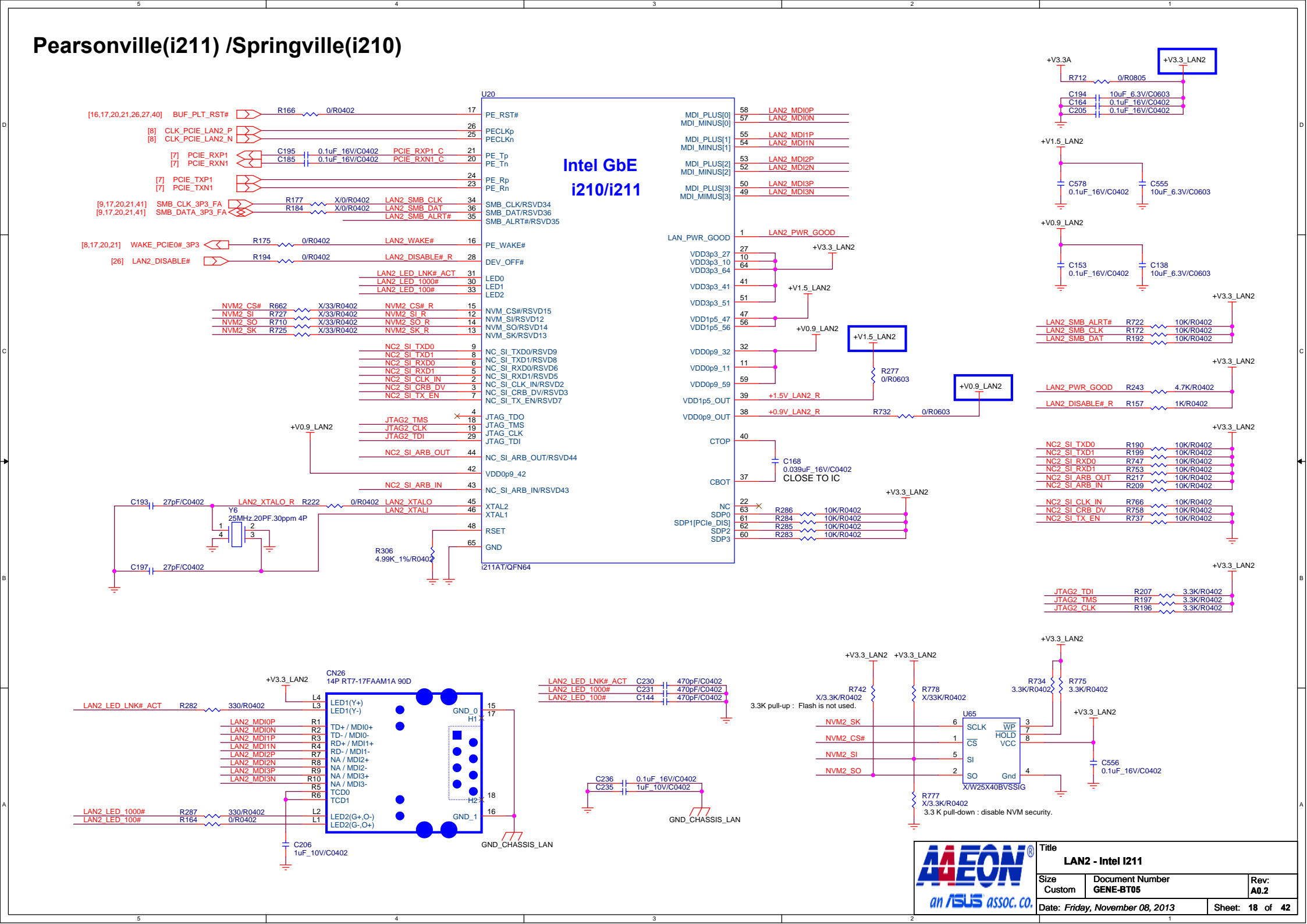
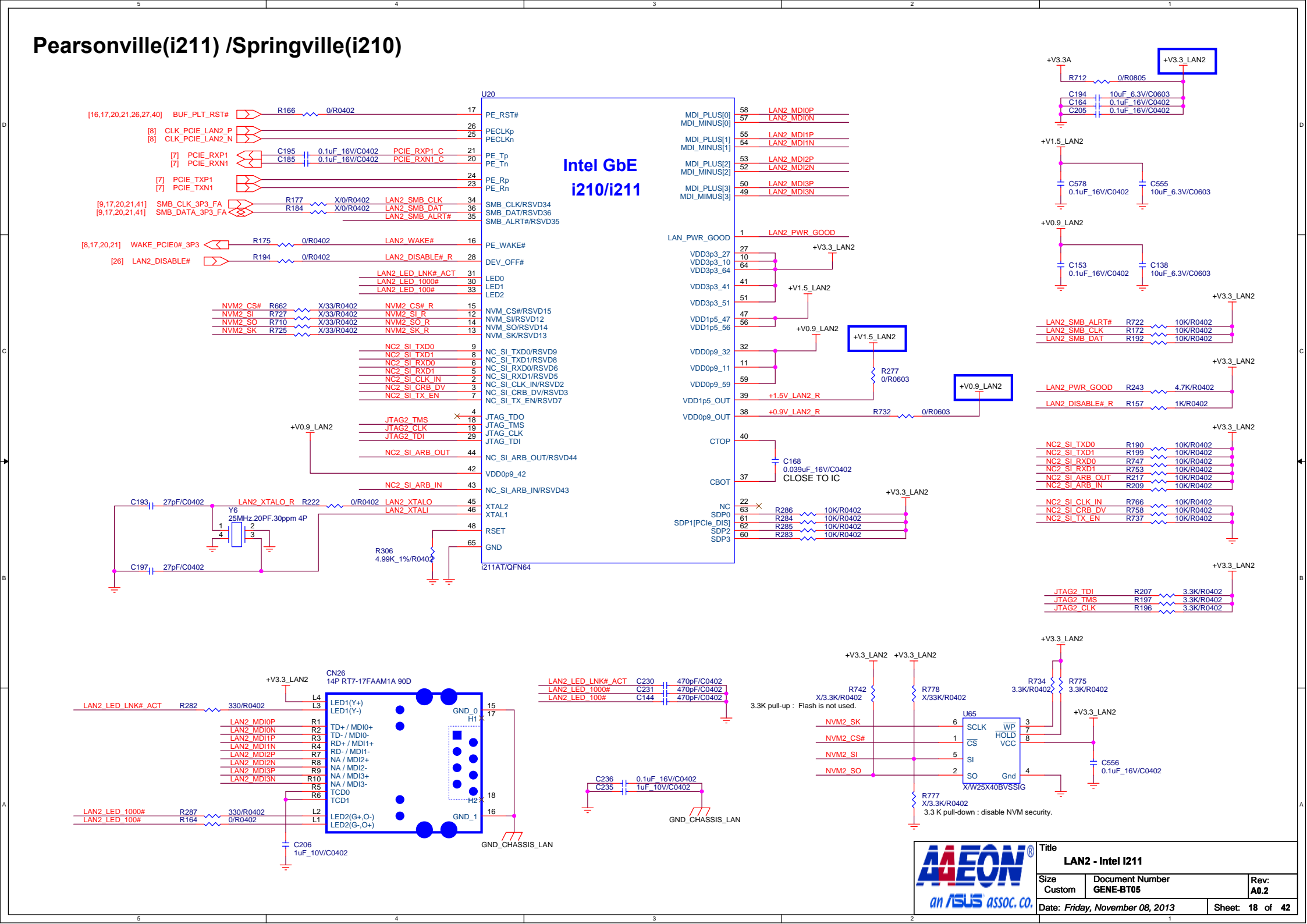
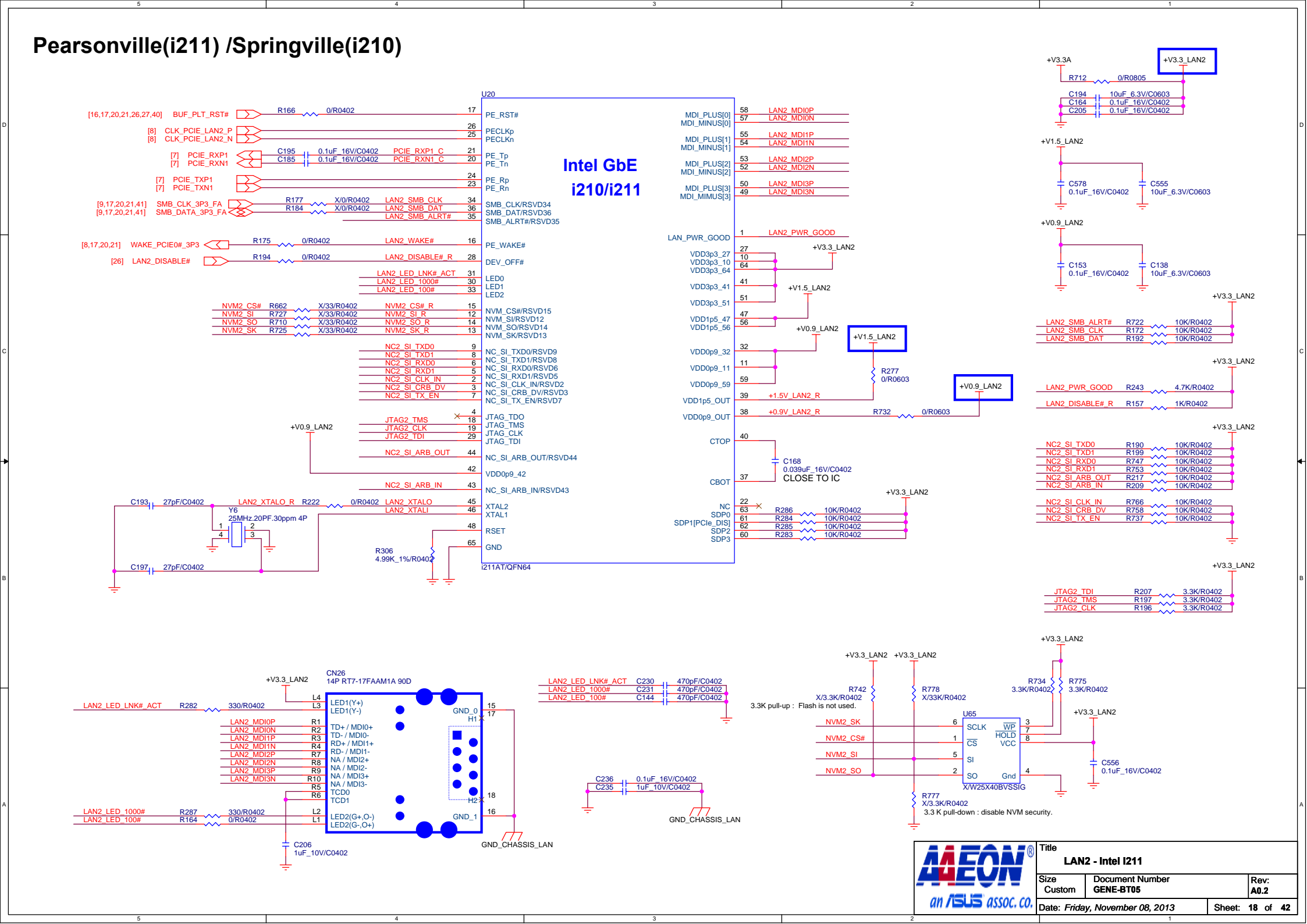
**Pearsonville(i211) /Springville(i210)**

**Intel GbE i210/i211**

**LAN2 - Intel I211**

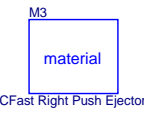
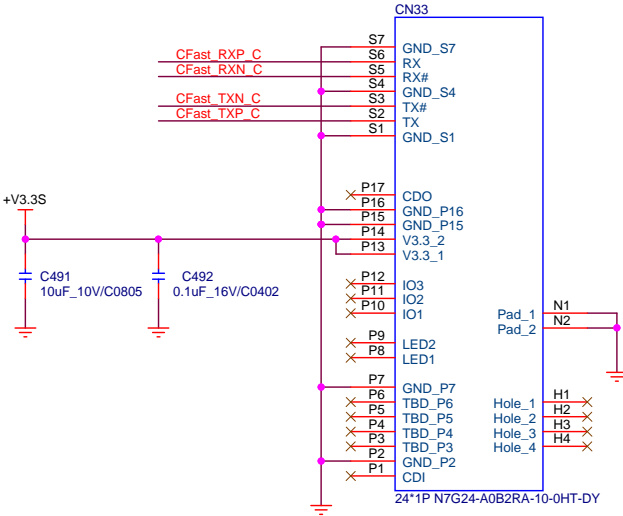
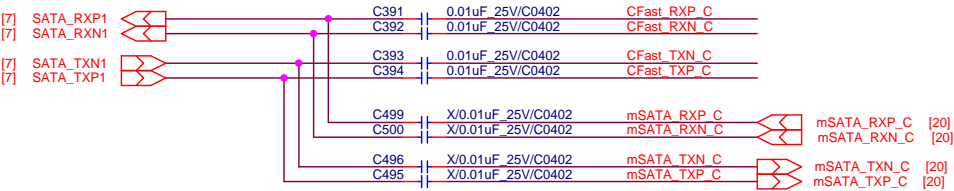
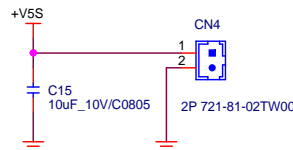
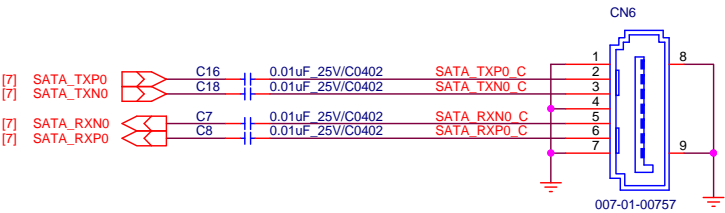
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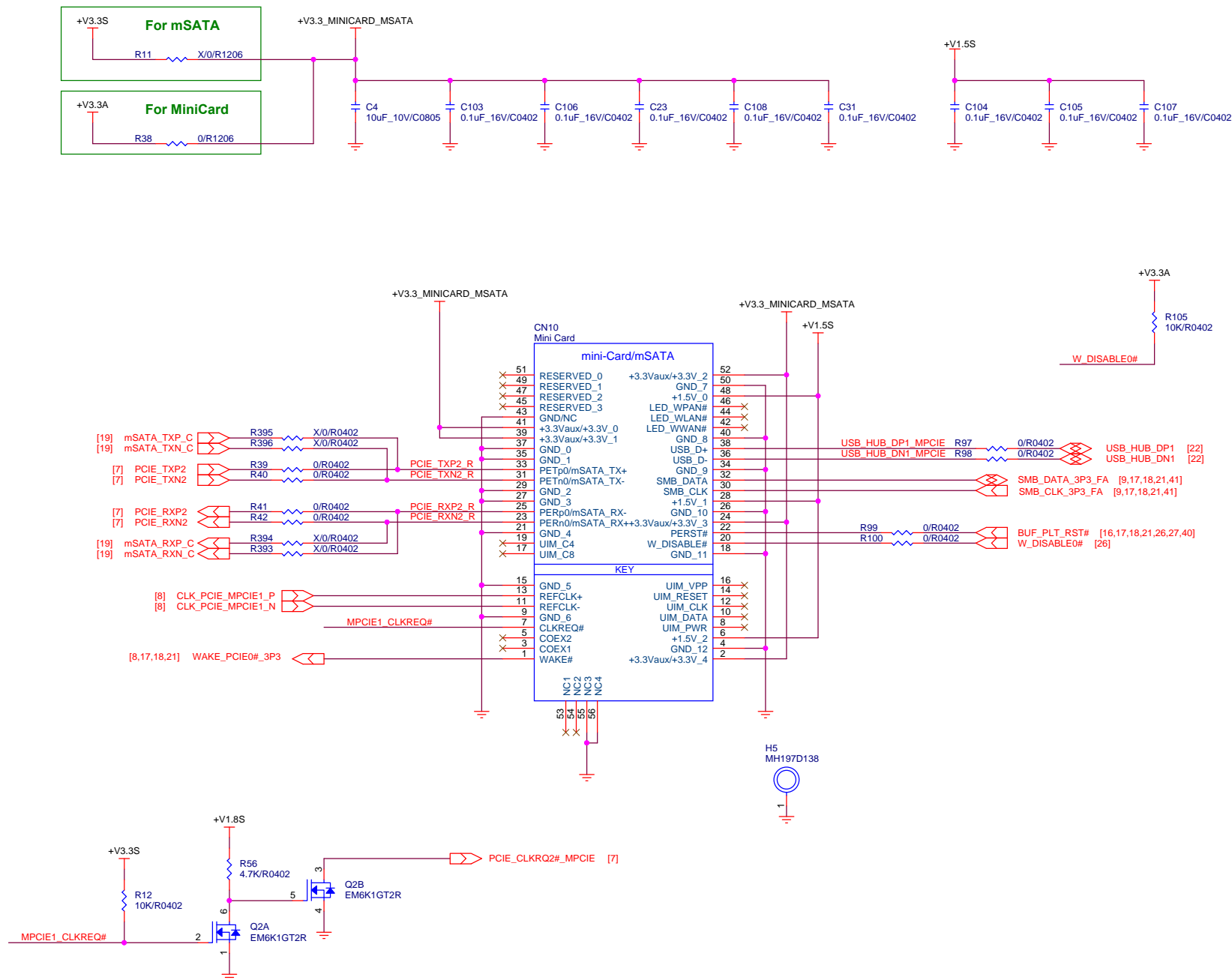


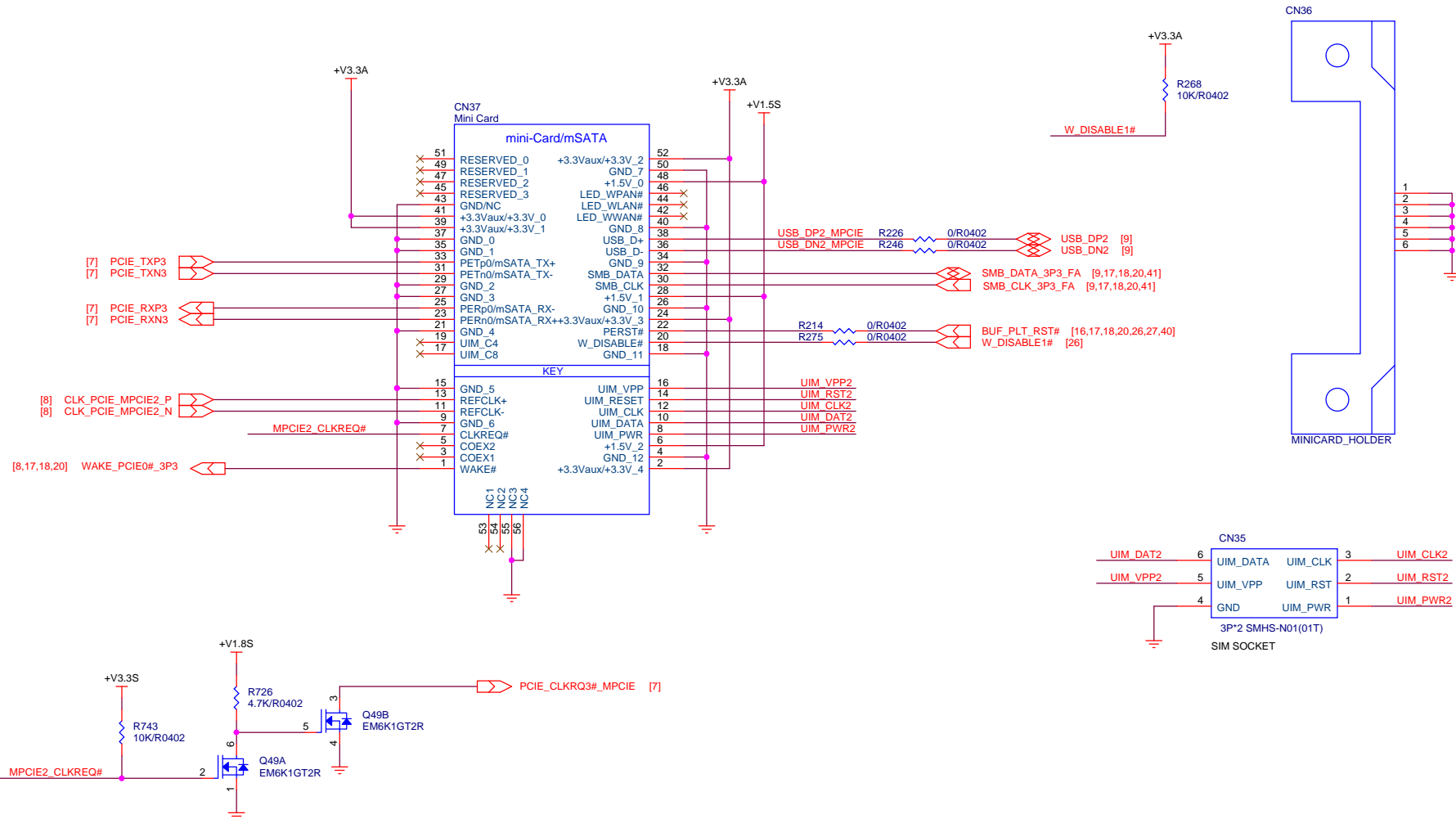
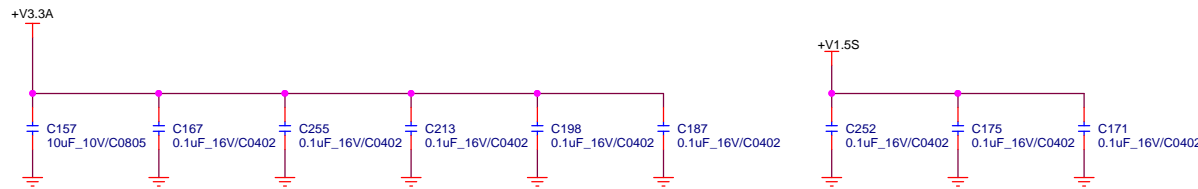
SATA 2.0

CFast




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Size Custom	Document Number <b>GENE-BT05</b>	Rev: <b>A0.2</b>
Date: Friday, November 08, 2013		Sheet: 19 of 42

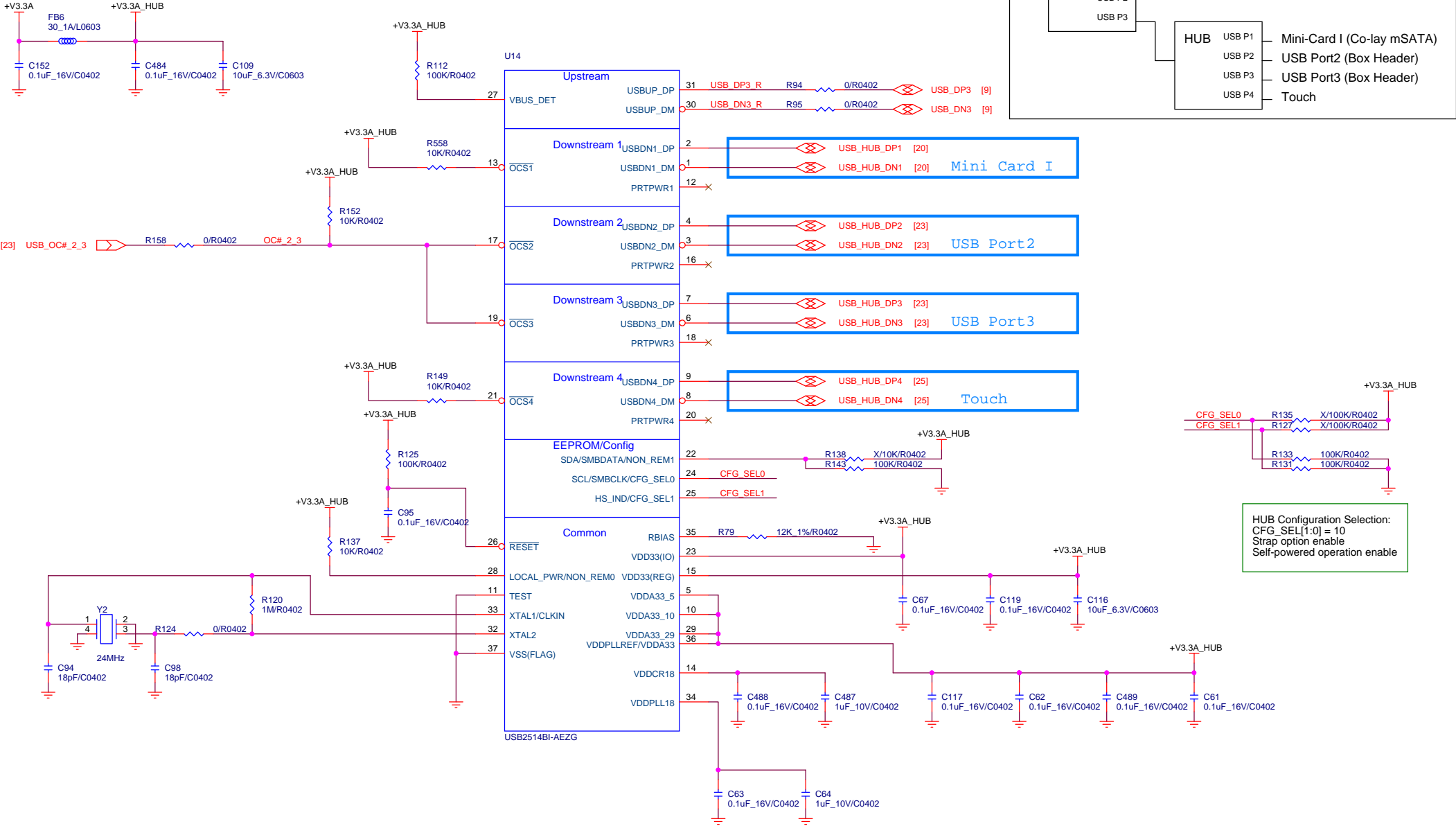




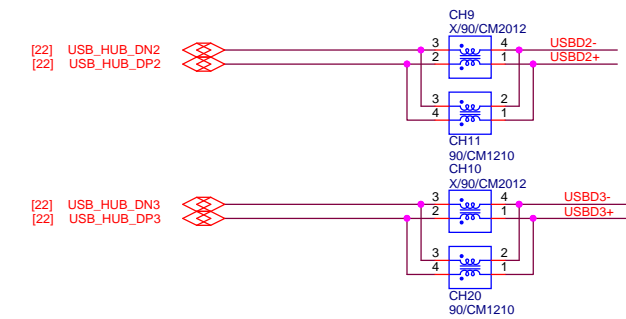
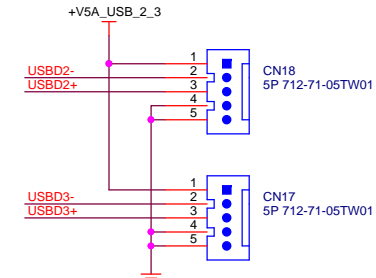
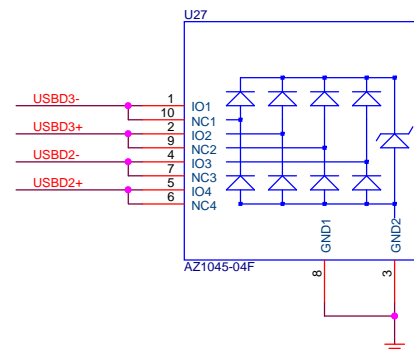
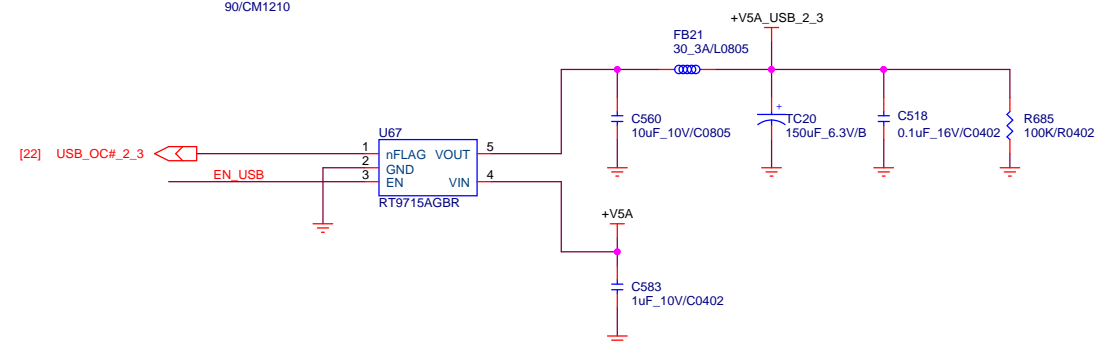
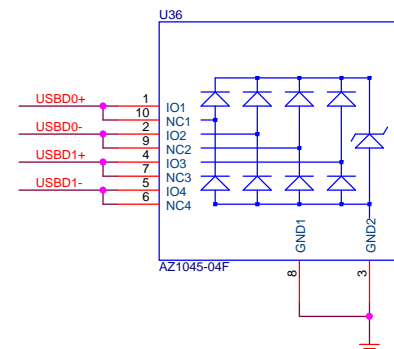
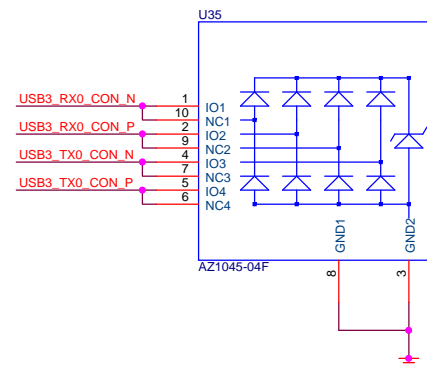
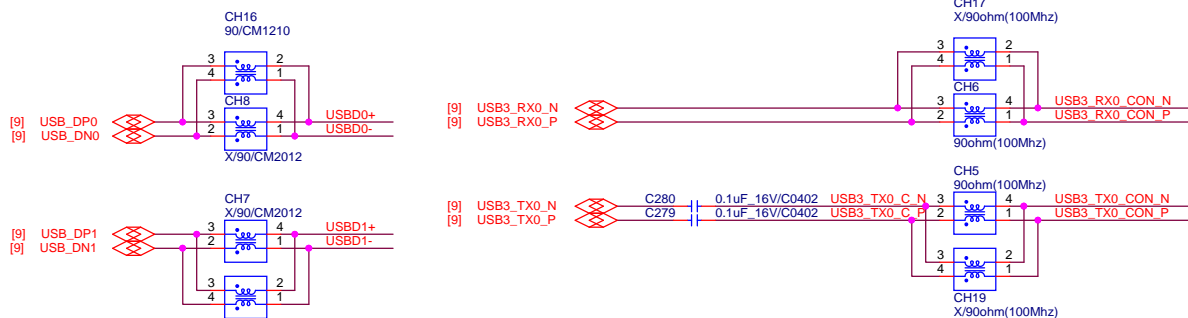
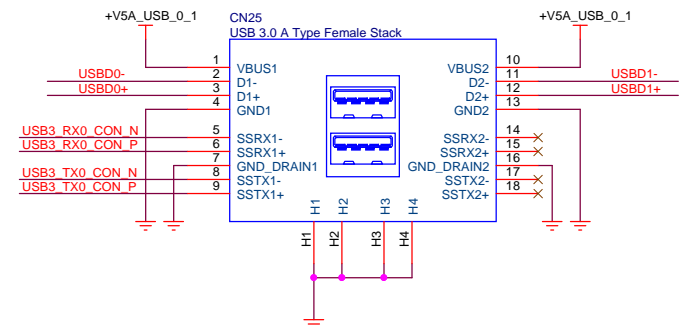
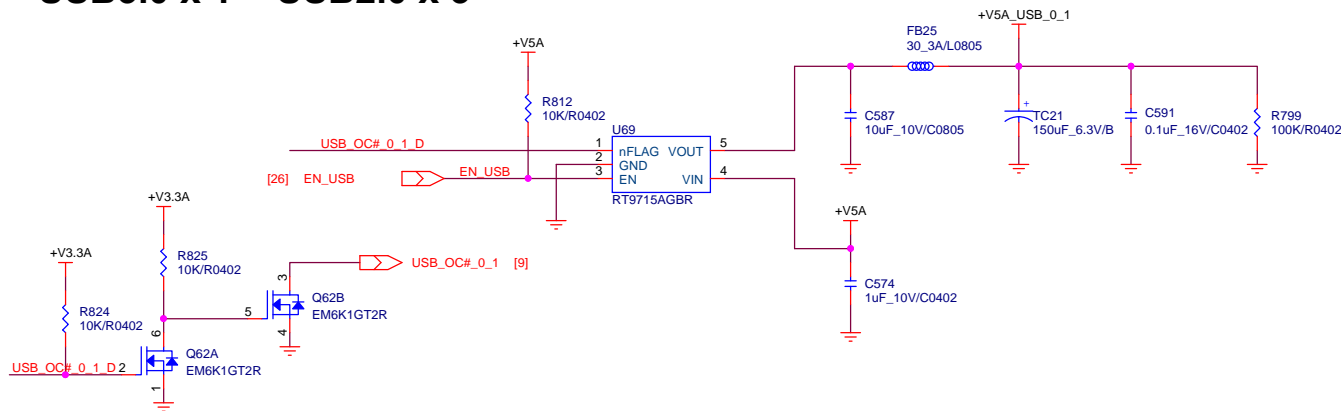
Boss Hole: MH197D138

 <i>an ASUS assoc. co.</i>	Title <b>MINI CARD II</b>		
	Size Custom	Document Number <b>GENE0-BT05</b>	Rev: <b>A0.2</b>
	Date: Friday, November 08, 2013		Sheet: 21 of 42

USB HUB



# USB3.0 x 1 + USB2.0 x 3



Title <b>USB PORT</b>		
Size Custom	Document Number <b>GENE-BT05</b>	Rev: <b>A0.2</b>
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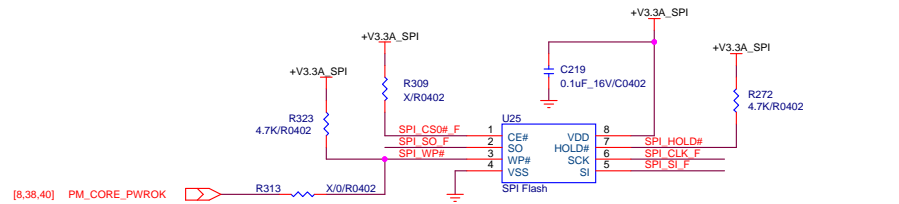
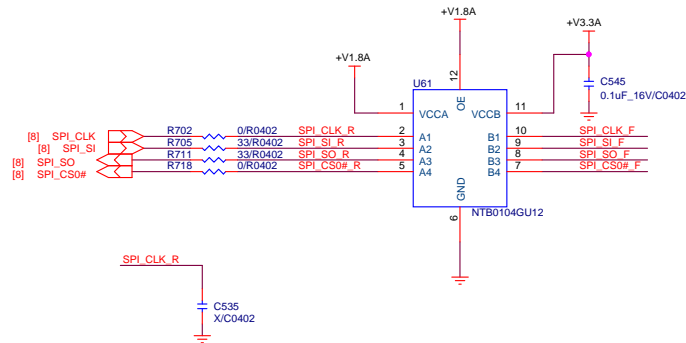




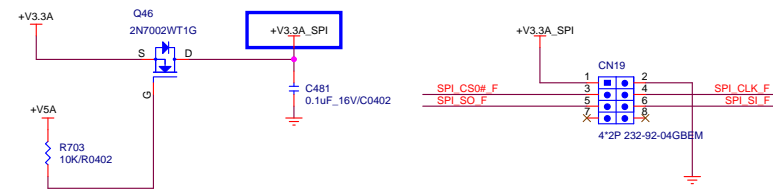




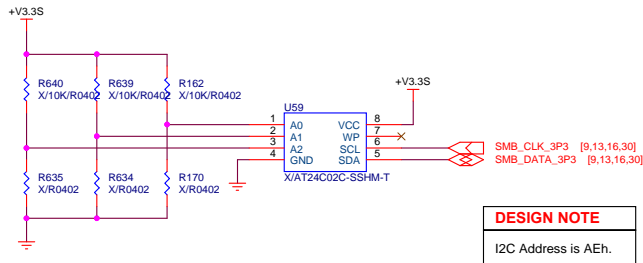
## SPI BIOS



8 pin : 1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0  
14S6206403 (TF)IC.64 Mbit SPI Flash.SOIC-8P 208mil.SMD.Winbond.W25Q64FVSSIG

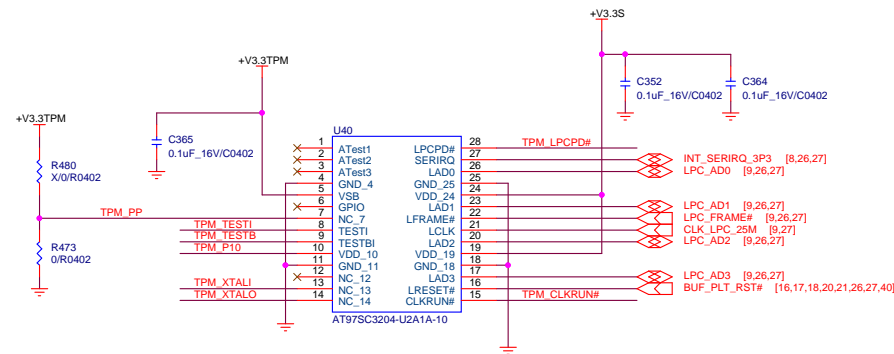


## CMOS Backup



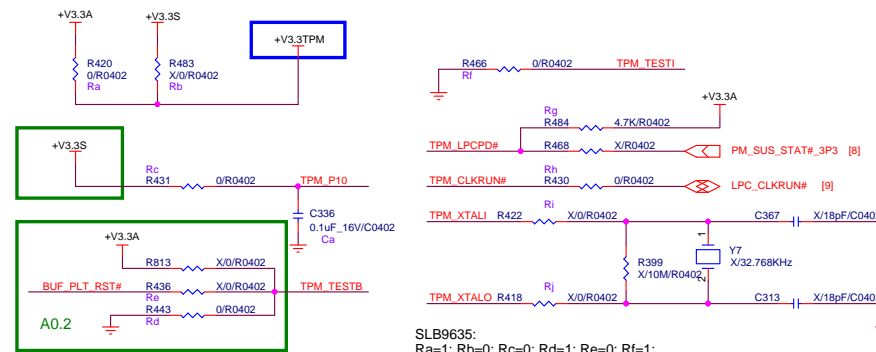
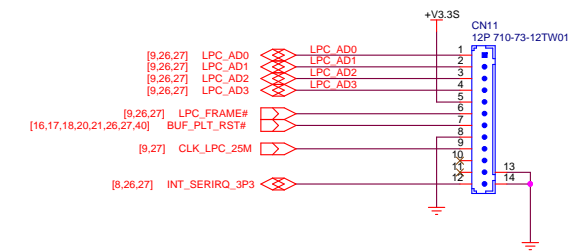
**DESIGN NOTE**  
I2C Address is AEh.

## TPM



PIN		AT24C256C	
1	15	ATest	LPCPD#
2	16	ATest	SERIRQ
3	17	ATest	LAD0
4	18	GND	GND
5	19	VSB	VDD
6	20	GPIO	LAD1
7	21	NC	LFRAME#
8	22	TESTI	LCLK
9	23	TESTB	LAD2
10	24	VDD	VDD
11	25	GND	GND
12	26	NC	LAD3
13	27	NC	LRESET#
14	28	NC	CLKRUN#

## LPC Connector



**DESIGN NOTE**  
TESTB = High, Addr = 4EH / 4FH

SLB9635:  
Ra=1; Rb=0; Rc=0; Rd=1; Re=0; Rf=1;  
Rg=1; Rh=1; Ri=1; Rj=1; Ca=0

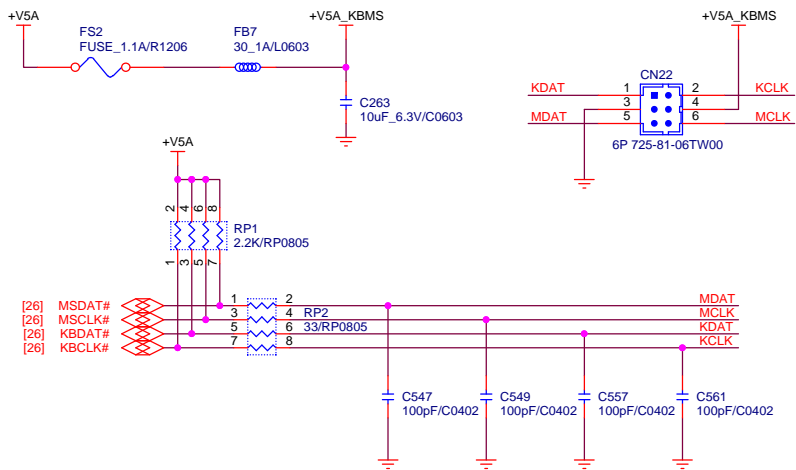
SLB9665:  
Ra=0; Rb=1; Rc=1; Rd=0; Re=1; Rf=0;  
Rg=0; Rh=0; Ri=0; Rj=0; Ca=1

AT24C256C  
Ra=1; Rb=0; Rc=1; Rd=1; Re=0; Rf=1;  
Rg=1; Rh=1; Ri=0; Rj=0; Ca=1

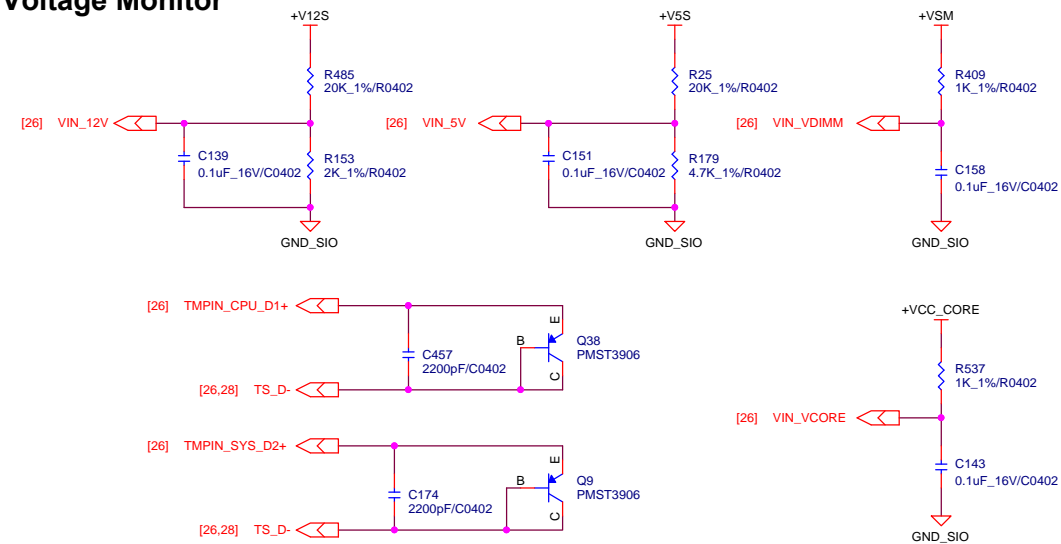
PIN		SLB9665			
1	15	NC	LPCPD#	NC	NC
2	16	GPIO2	SERIRQ	NC	SERIRQ
3	17	NC	LAD0	NC	LAD0
4	18	GND	GND	GND	GND
5	19	VSB	VDD	VDD	VDD
6	20	GPIO	LAD1	GPIO	LAD1
7	21	PP	LFRAME#	PP	LFRAME#
8	22	TESTI	LCLK	NC	LCLK
9	23	TESTB	LAD2	LRESET#	LAD2
10	24	NC	VDD	VDD	VDD
11	25	GND	GND	GND	GND
12	26	NC	LAD3	NC	LAD3
13	27	XTALI/32KIN	LRESET#	NC	LRESET#
14	28	XTALO	CLKRUN#	NC	NC



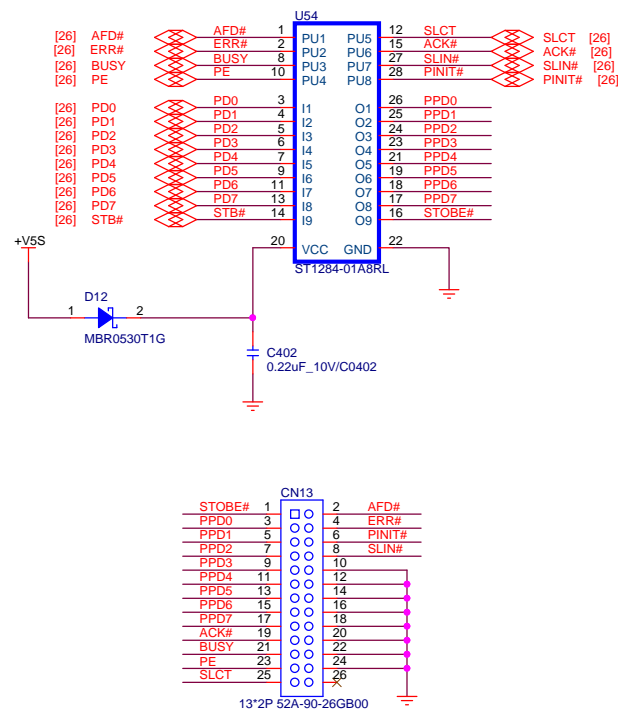
PS/2 Keyboard/Mouse



Voltage Monitor



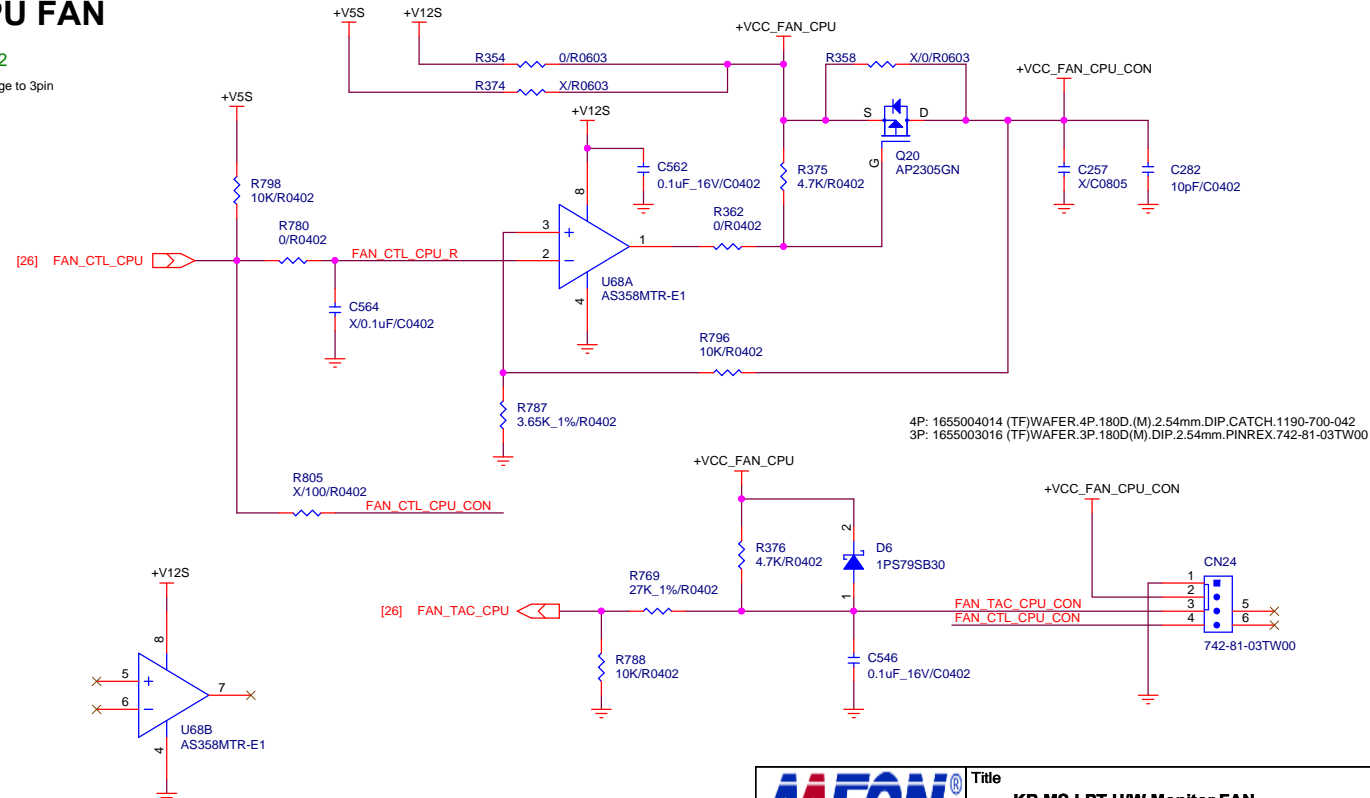
LPT



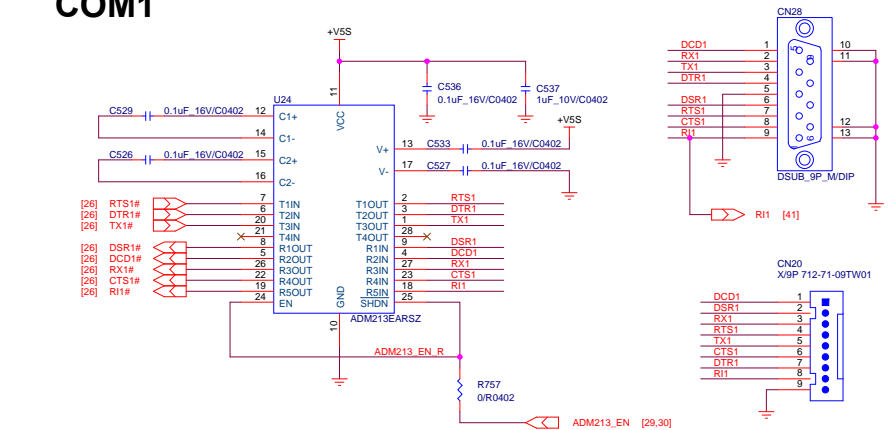
CPU FAN

A0.2

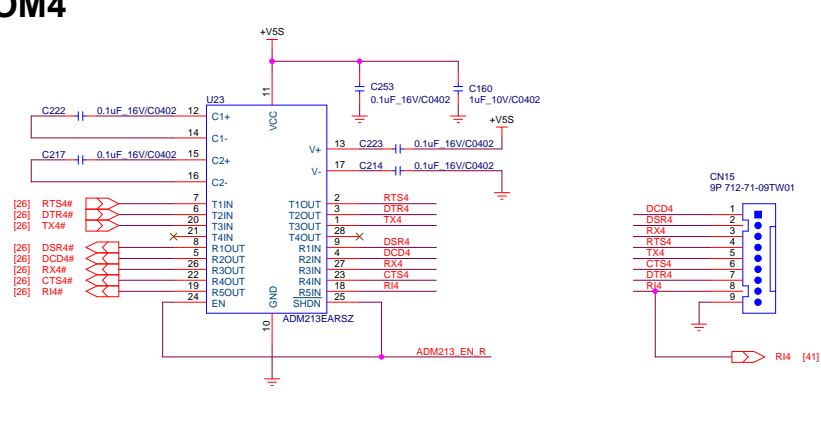
change to 3pin



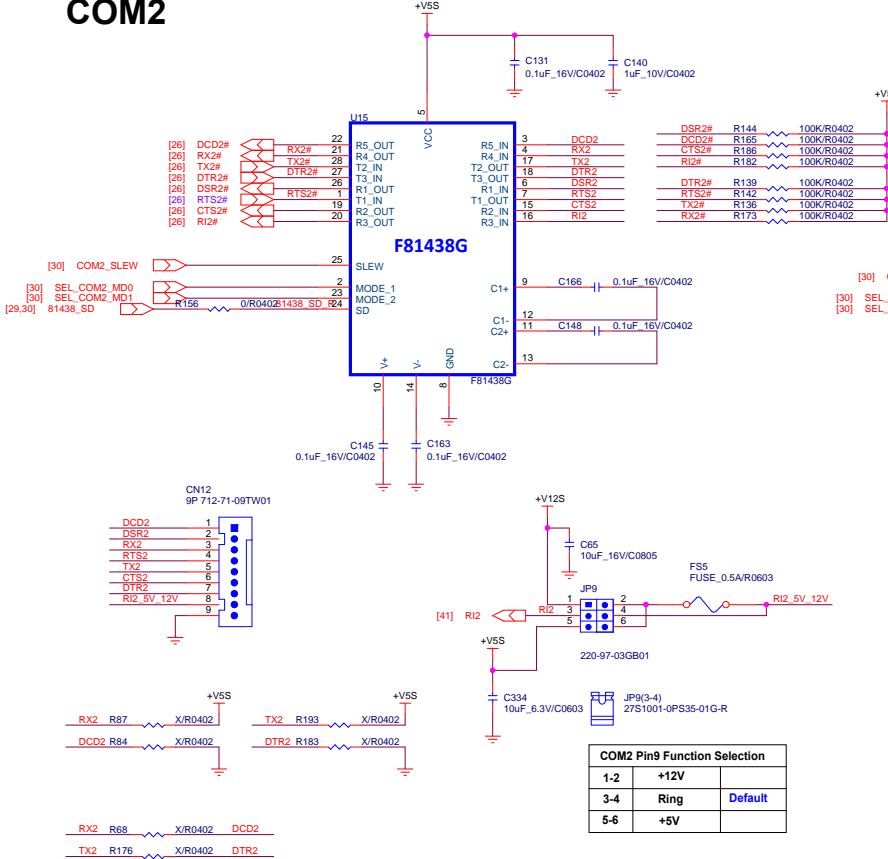
COM1



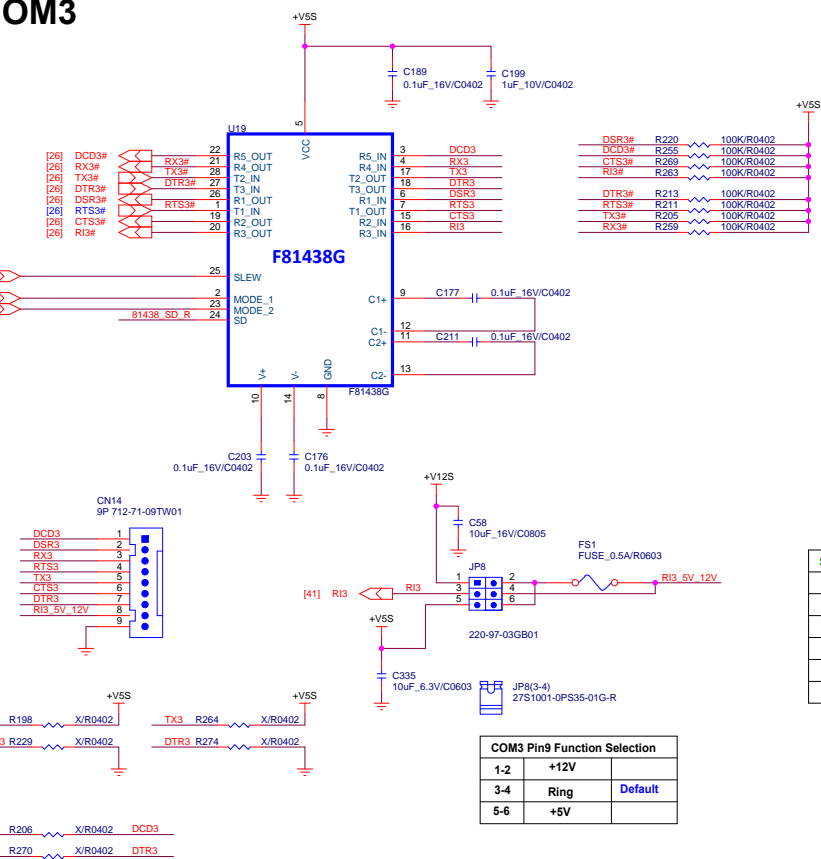
COM4



COM2



COM3



Maximum Slew rate control			
SLEW	RS-232	RS-485/RS-422	
0	1Mbps	10Mbps	
1	250Kbps	250Kbps	

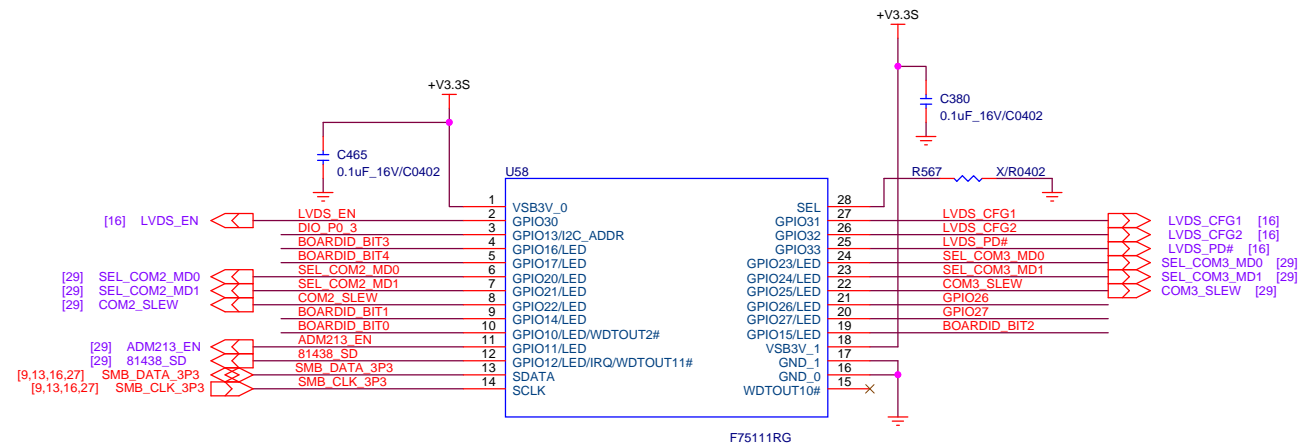
Pin Mapping			
	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

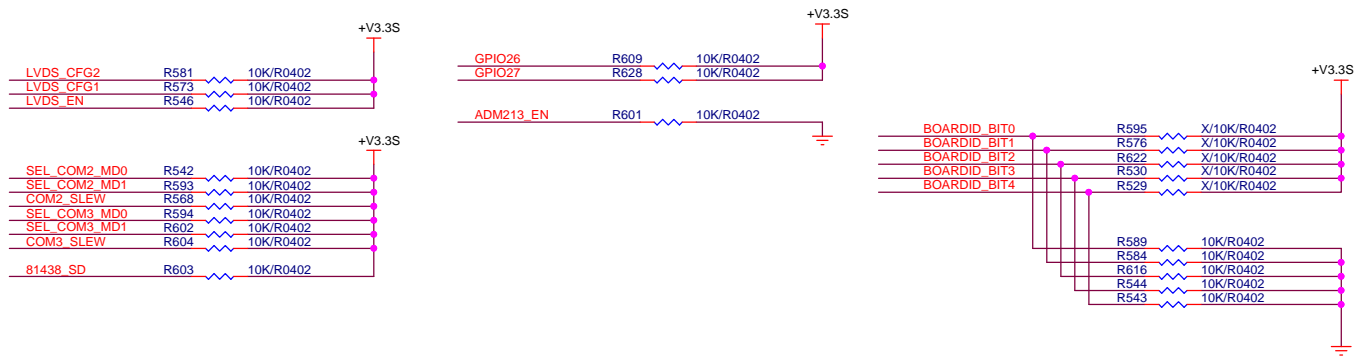
COM2 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

COM3 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

GPIO - F75111RG

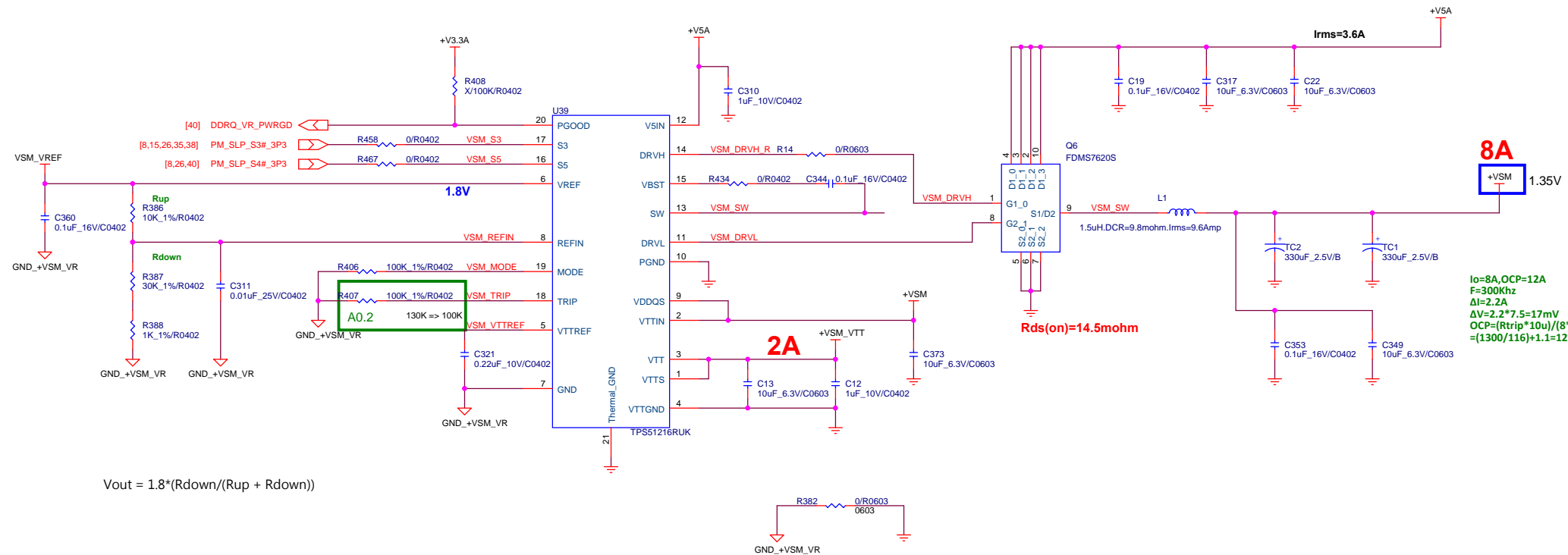


I2C Address	
GPIO13	Float : I2C Address = 0x9Ch
	High : I2C Address = 0x6Eh





DDR3L Power



$V_{out} = 1.8 * (R_{down} / (R_{up} + R_{down}))$

MODE Selection

Resistance(K ohm)	SW Frequency(kHz)	Discharge Mode
200	400	Tracking
100	300	Tracking
68	300	Non-tracking
47	400	Non-tracking

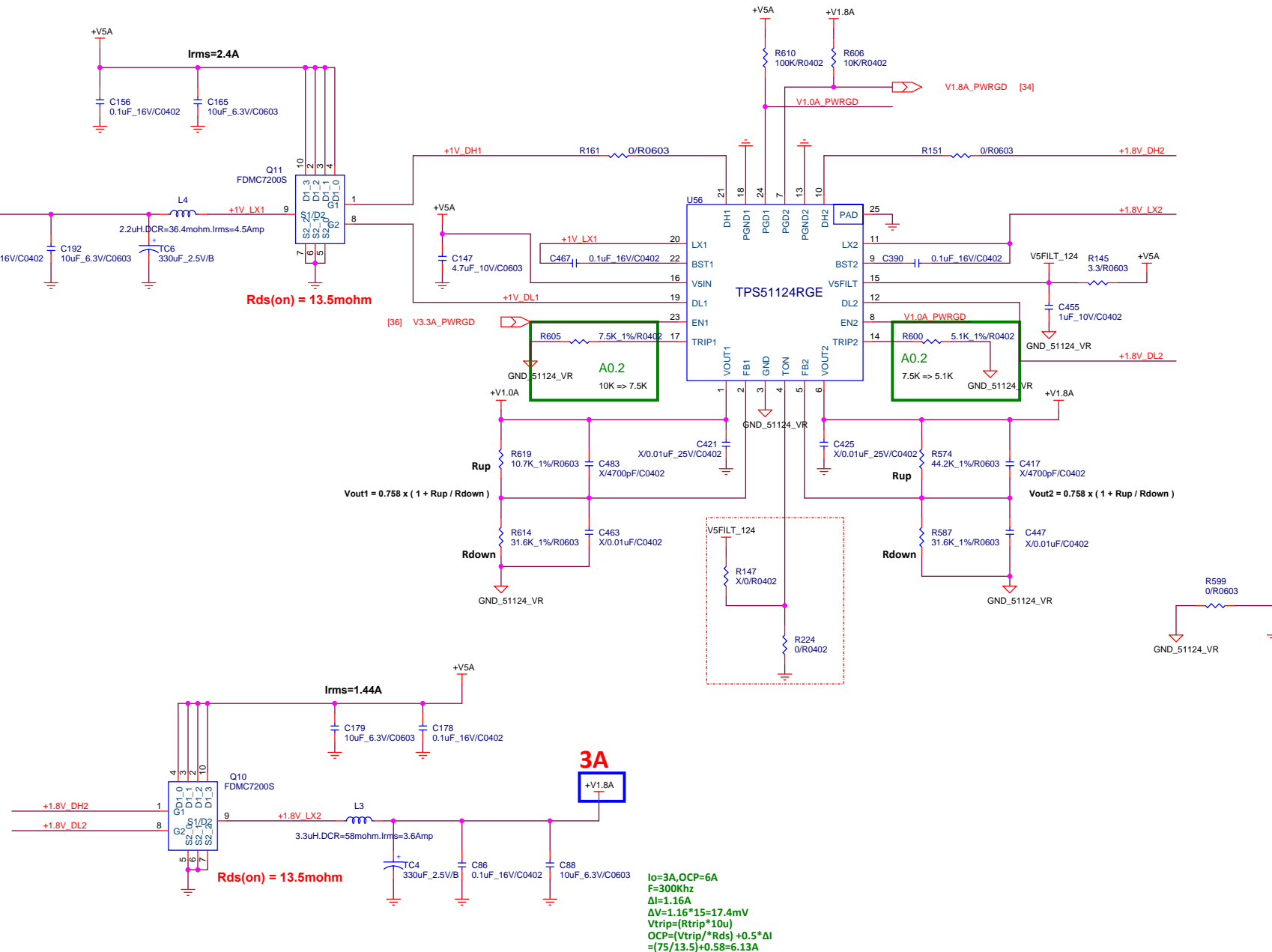
S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF
S4/S5	LO	LO	OFF	OFF	OFF	OFF

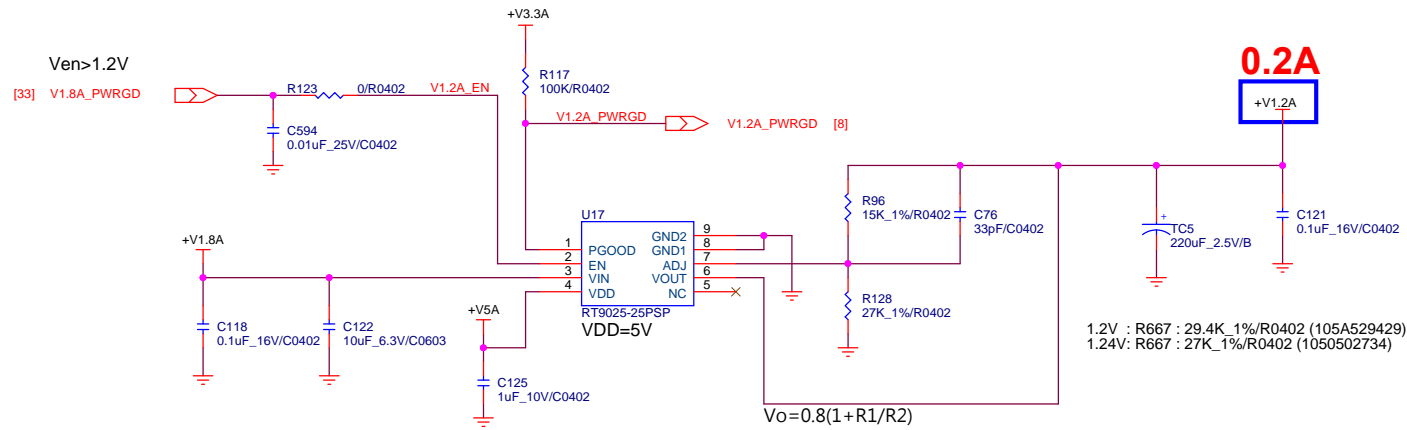


# +V1.0A, +V1.8A

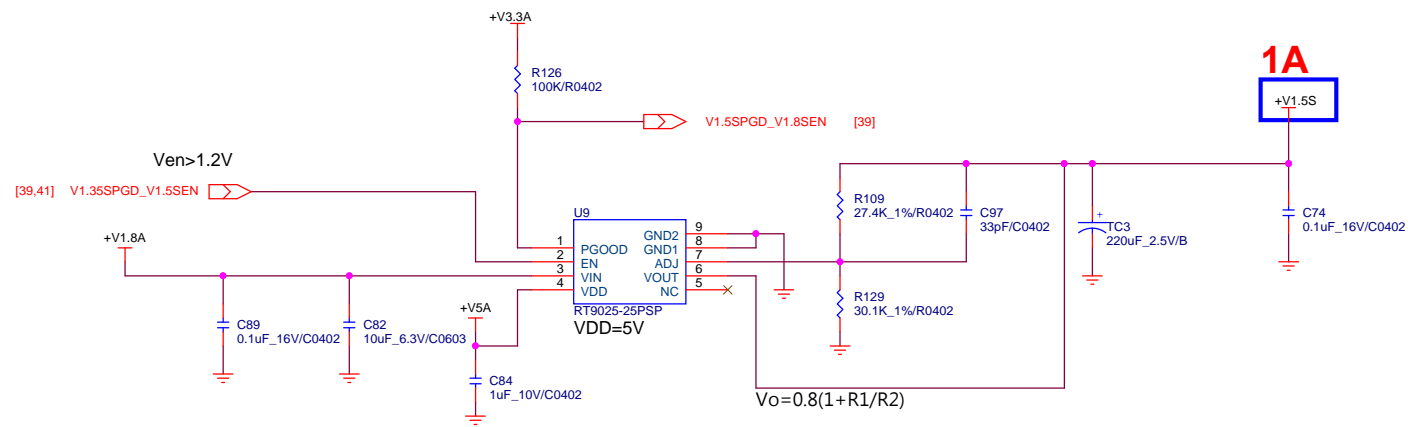
$I_o=4A, OCP=8A$   
 $F=240KHz$   
 $\Delta I=1.52A$   
 $\Delta V=1.52*15=22.8mV$   
 $V_{trip}=(R_{trip}*10u)$   
 $OCP=(V_{trip}/R_{ds})+0.5*\Delta I$   
 $=(110/13.5)+0.75=9A$



+V1.2A

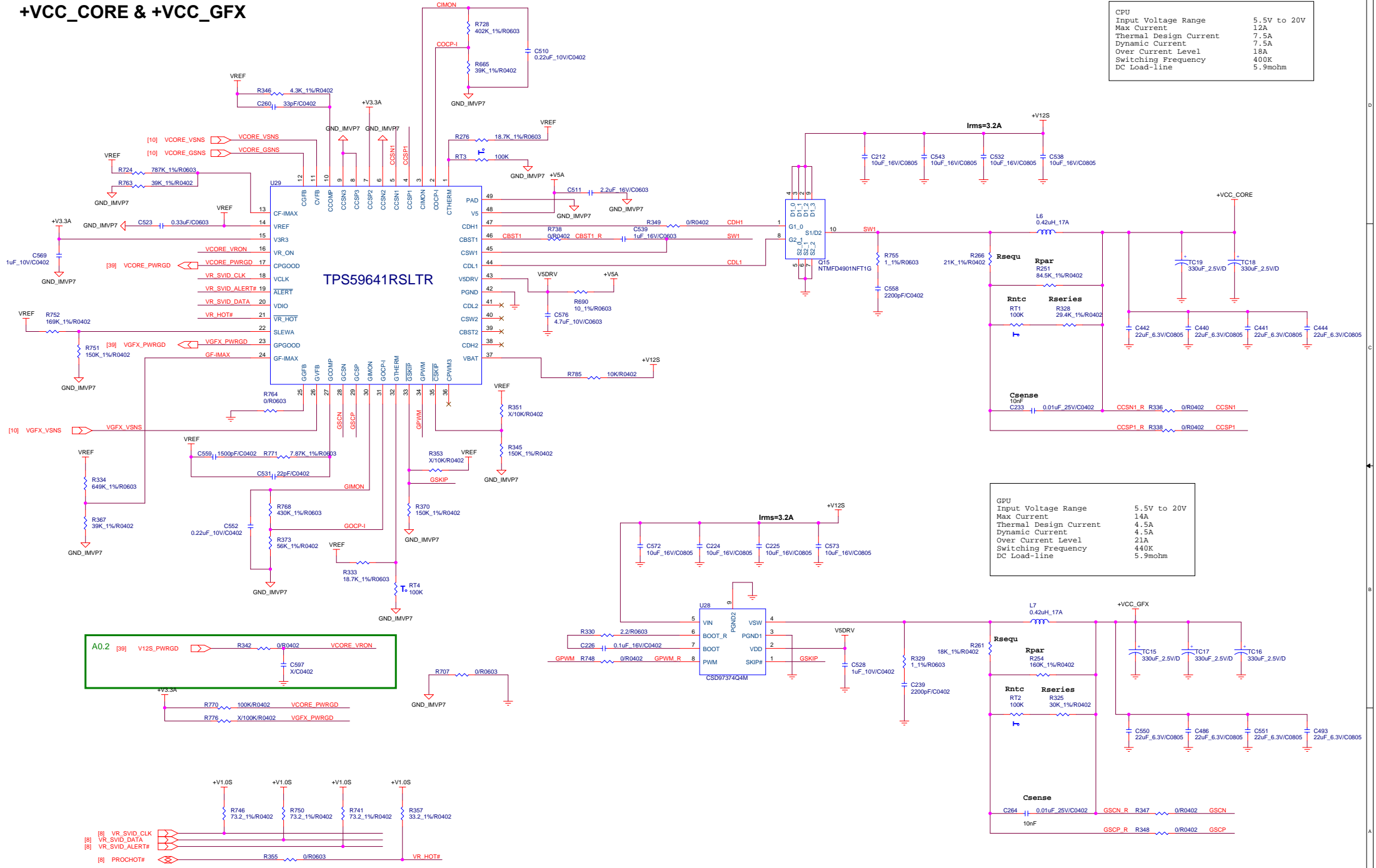


+V1.5S



+VCC\_CORE & +VCC\_GFX

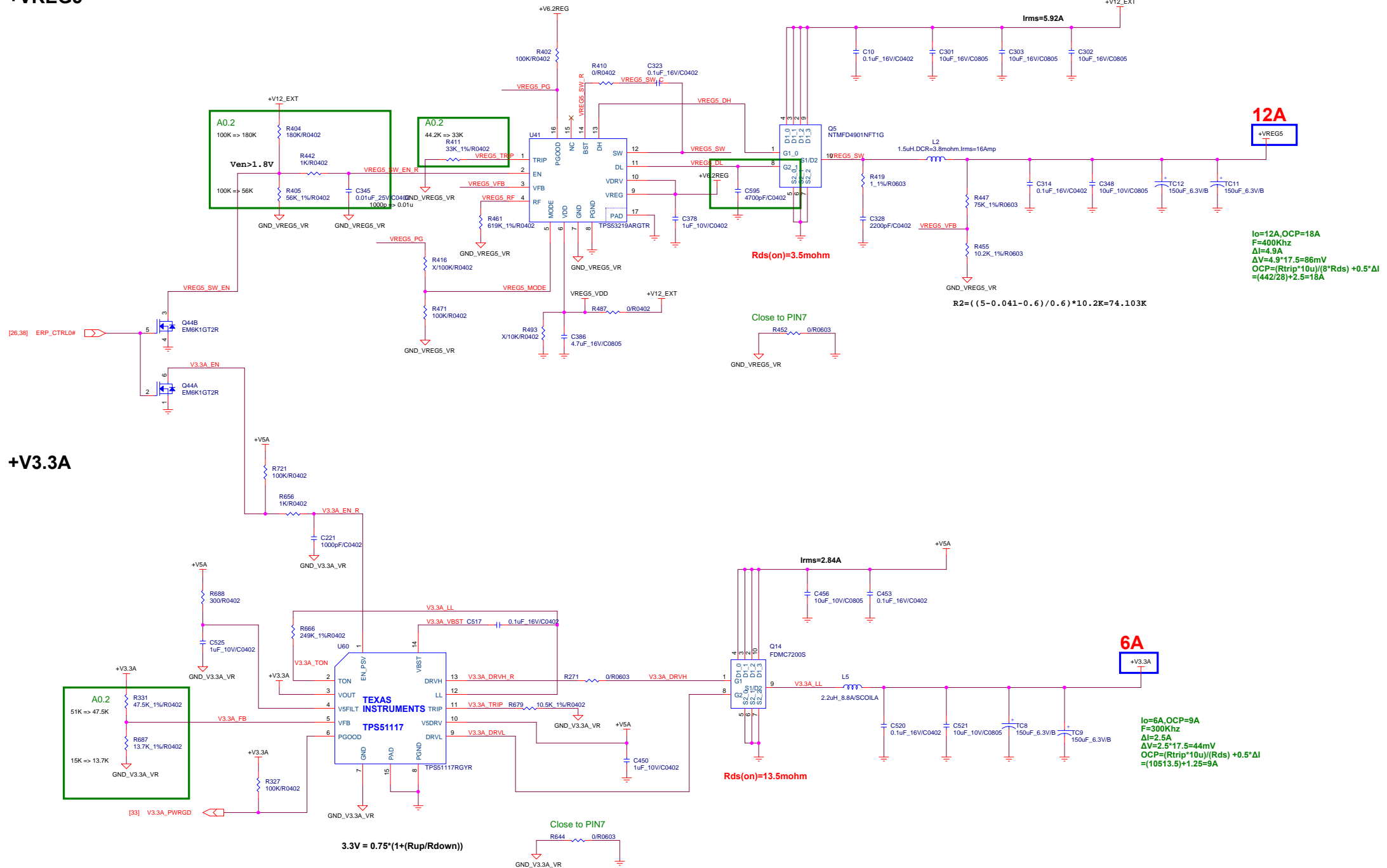
CPU	
Input Voltage Range	5.5V to 20V
Max Current	12A
Thermal Design Current	7.5A
Dynamic Current	7.5A
Over Current Level	18A
Switching Frequency	400K
DC Load-line	5.9mohm



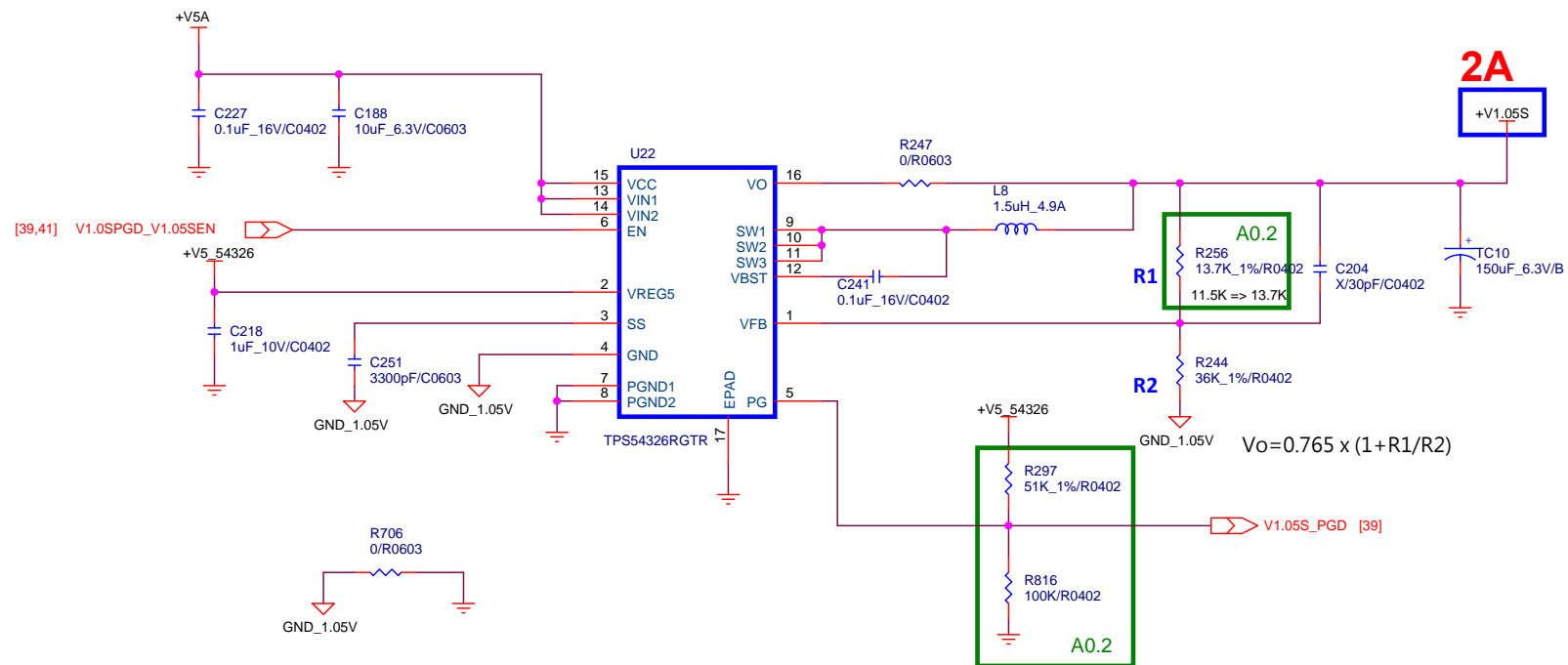
GPU	
Input Voltage Range	5.5V to 20V
Max Current	14A
Thermal Design Current	4.5A
Dynamic Current	4.5A
Over Current Level	21A
Switching Frequency	440K
DC Load-line	5.9mohm



## +VREG5

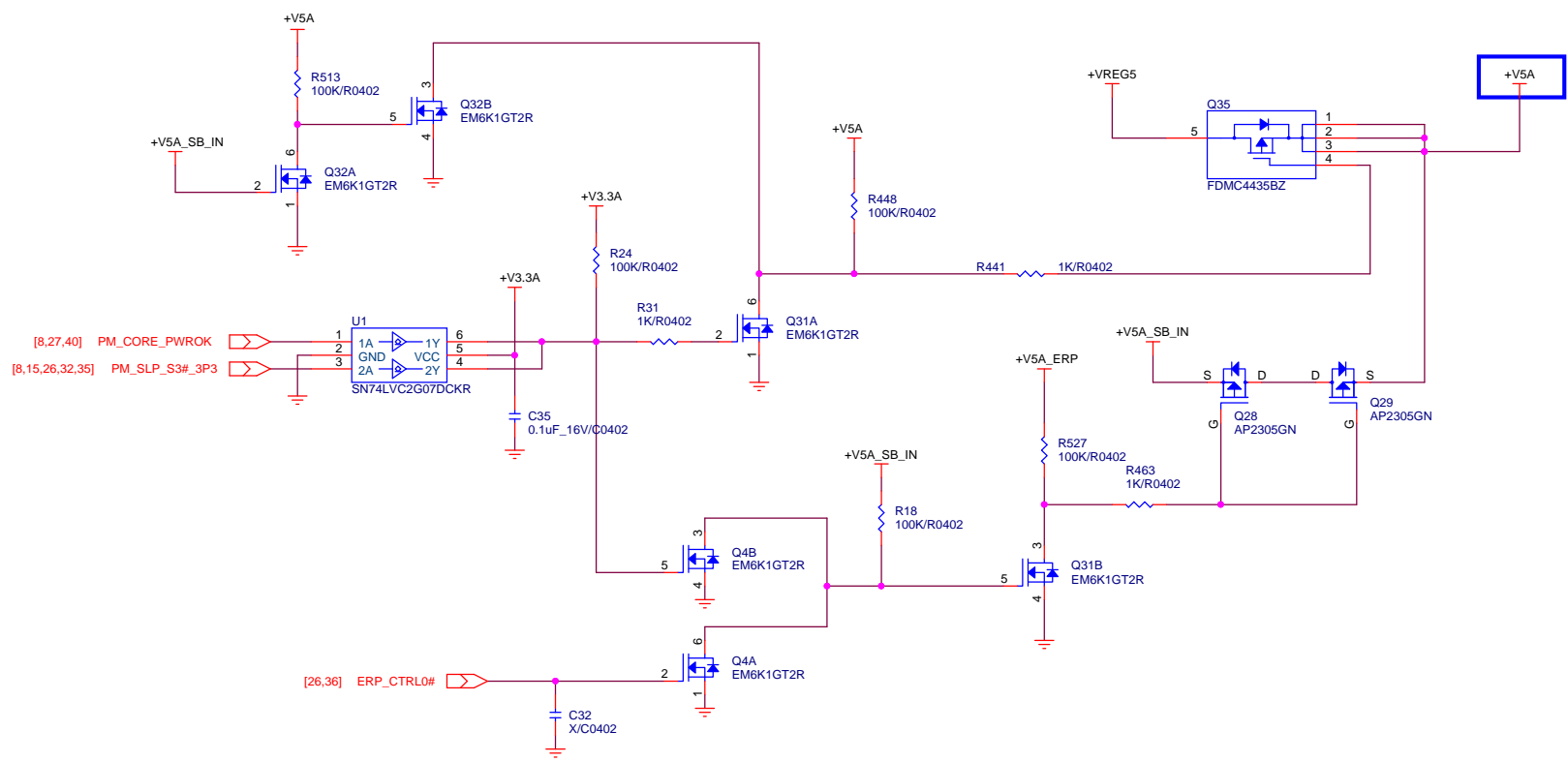


## +V1.05S

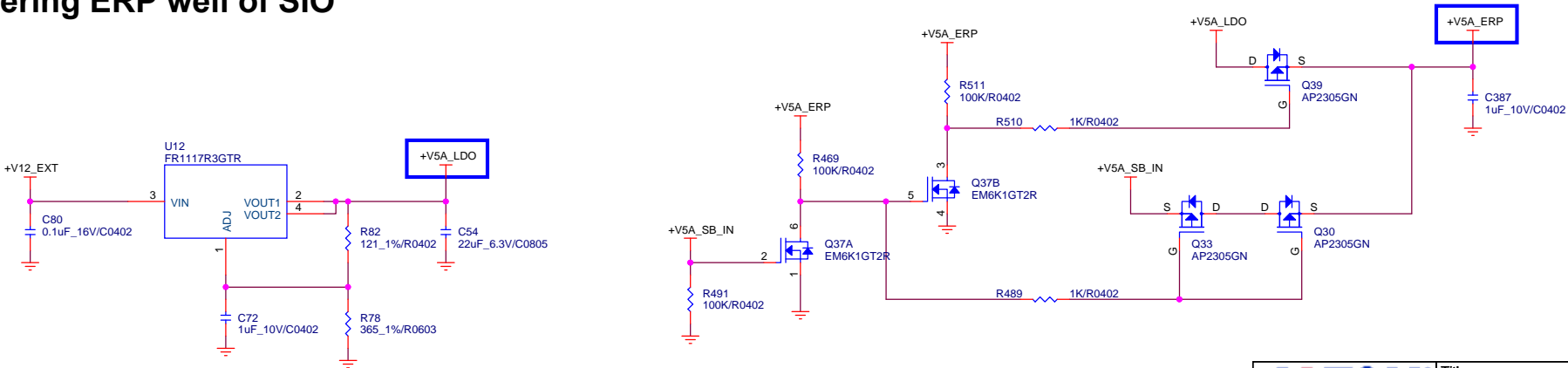


$I_o = 2A$   
 $F = 700KHz$   
 $\Delta I = 0.75A$   
 $\Delta V = 0.75 \times 35 = 26.2mV$

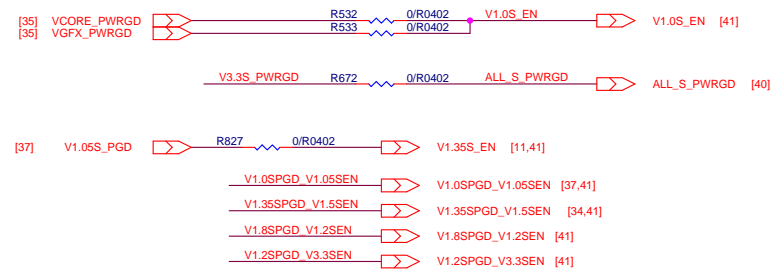
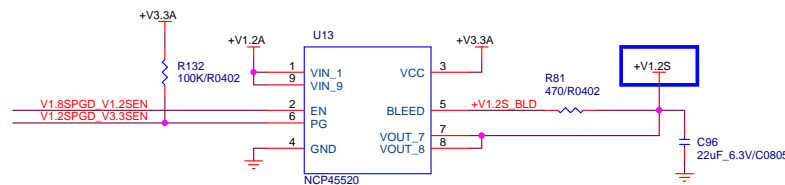
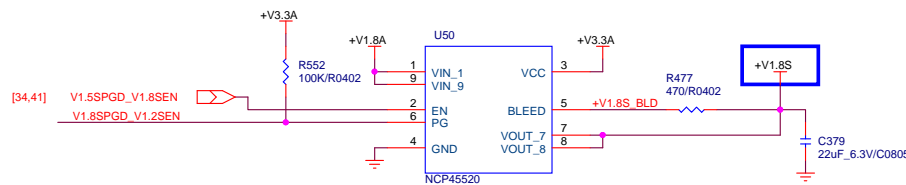
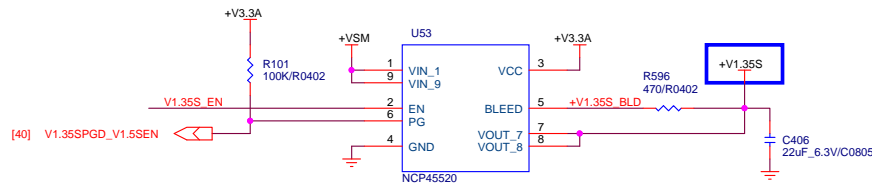
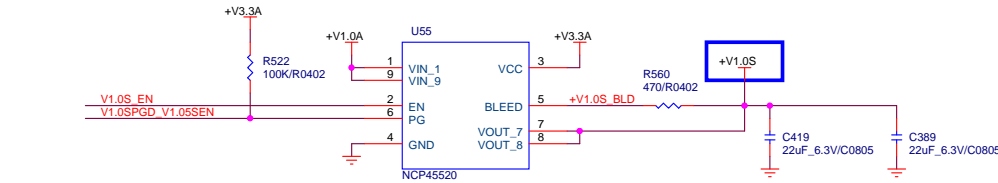
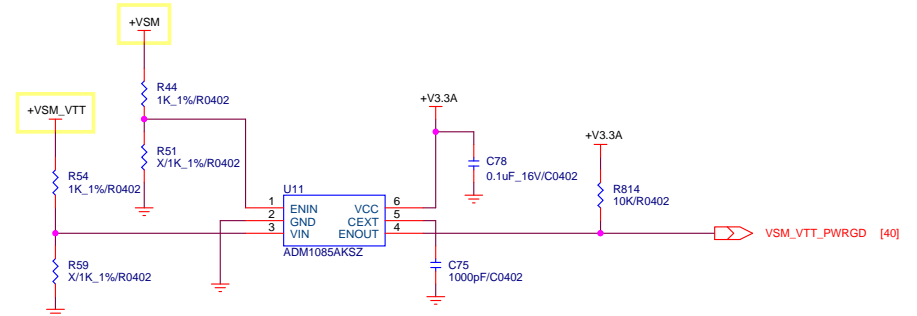
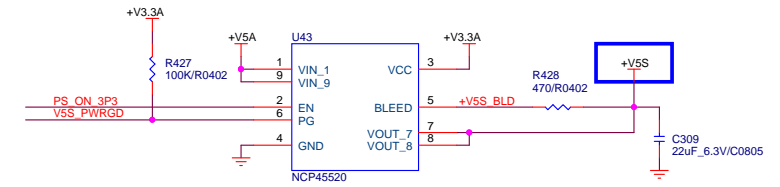
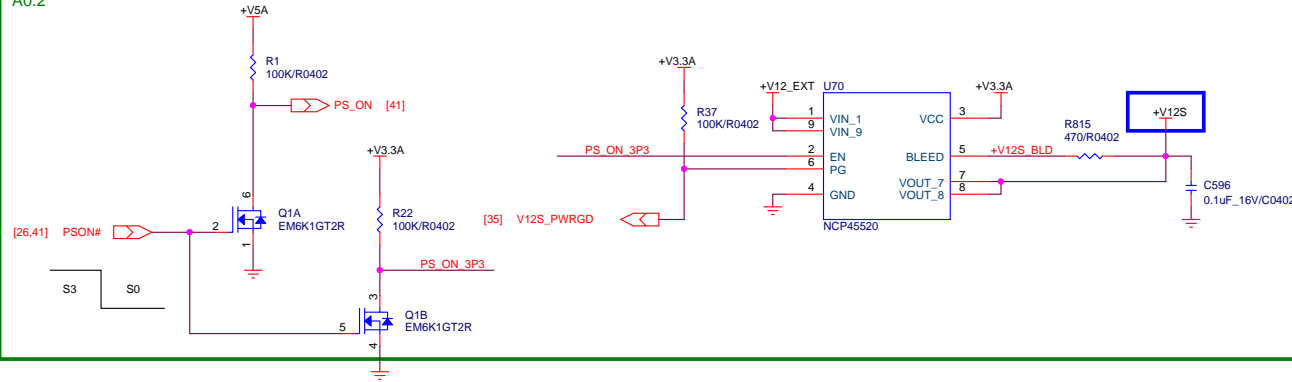
5VDAUL Switch Circuit



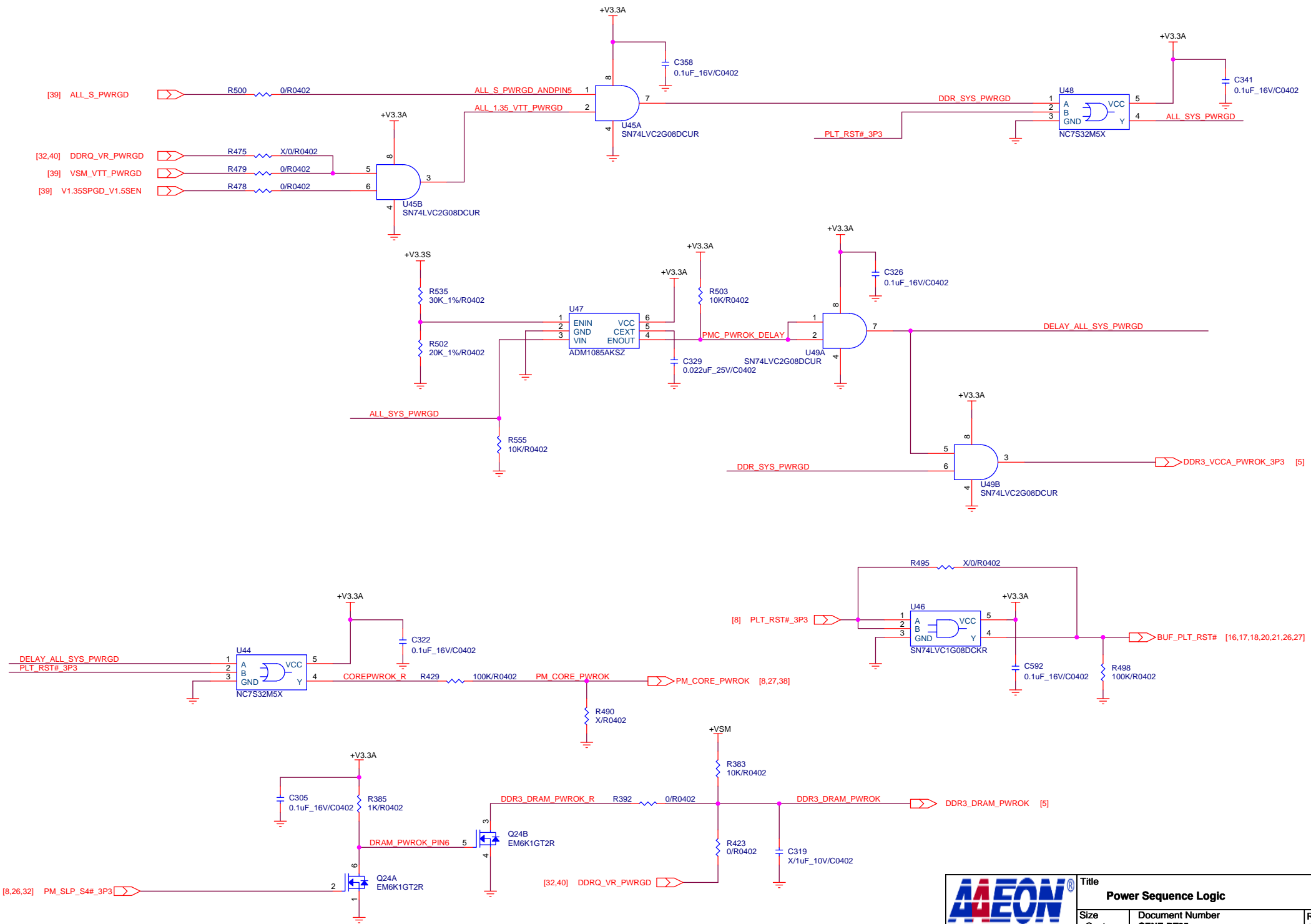
Powering ERP well of SIO



A0.2



Title		
System Power		
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HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2013/05/17	A0.1	First Release		Lena	Benson
2	2013/06/10	A0.1	Remove DVI circuit.	P15	Lena	Benson
3	2013/06/19	A0.1	1.Remove eDP circuit. 2.Remove eDP page (P17)	P16 P17	Lena	Benson
			DDI1_VDDEN/DDI1_BKLTEN/DDI1_BKLTCTL DDI1_TXP_2/DDI1_TXN_2/DDI1_TXP_3/DDI1_TXN_3 Unconnected.	P6		
			Remove eDP_LVDS_SEL GPIO	P30		
3	2013/09/30	A0.2	1.R407 change to 100K from 130K for OCP adjust. 2.R411 change to 33K from 44.2K for OCP adjust. 3.Q5 G2 add a cap. C378 (4700pf) 4. Remove V5S_EN discharge.	P32 P36 P36 P41	Lena	Benson