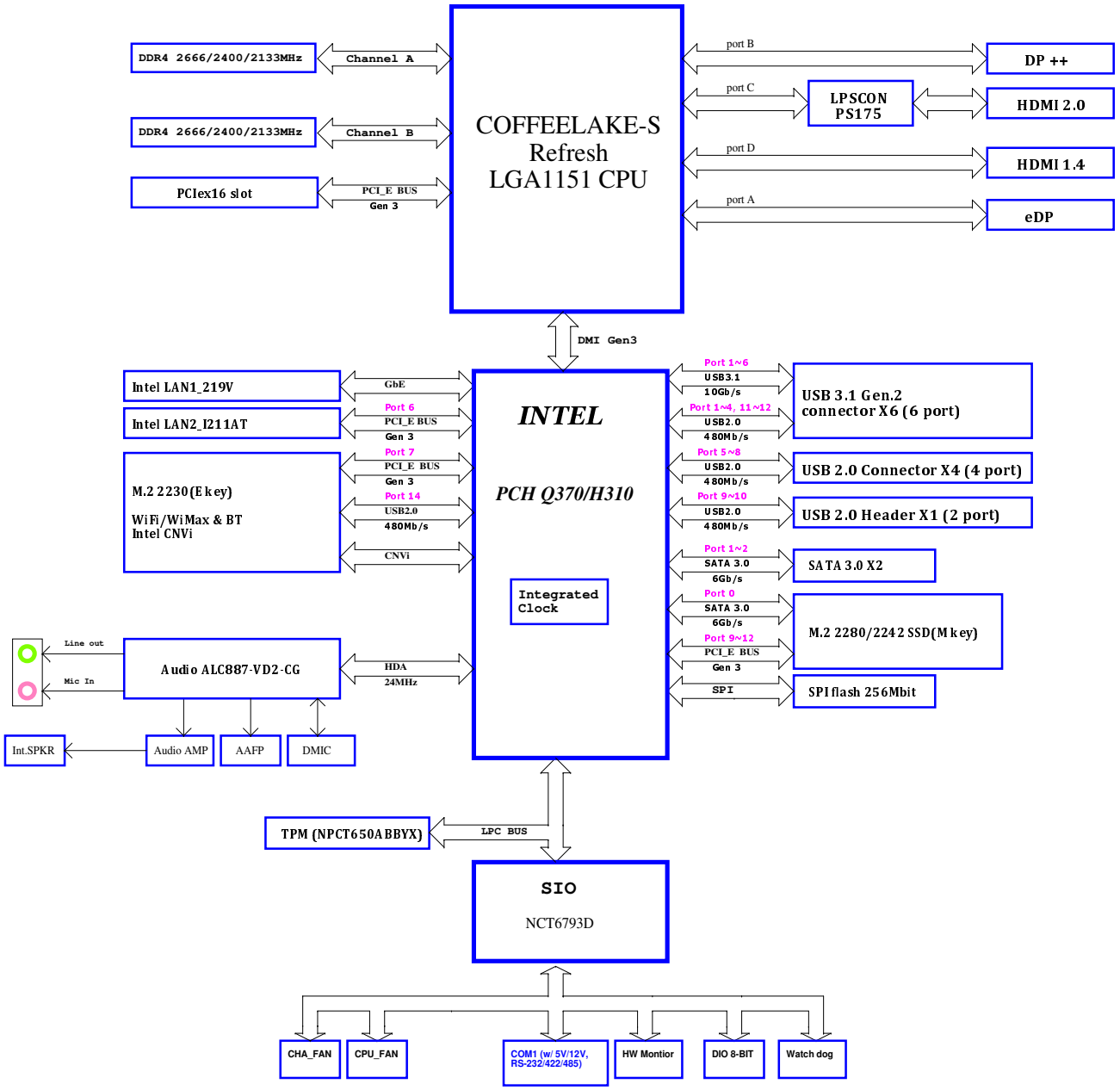
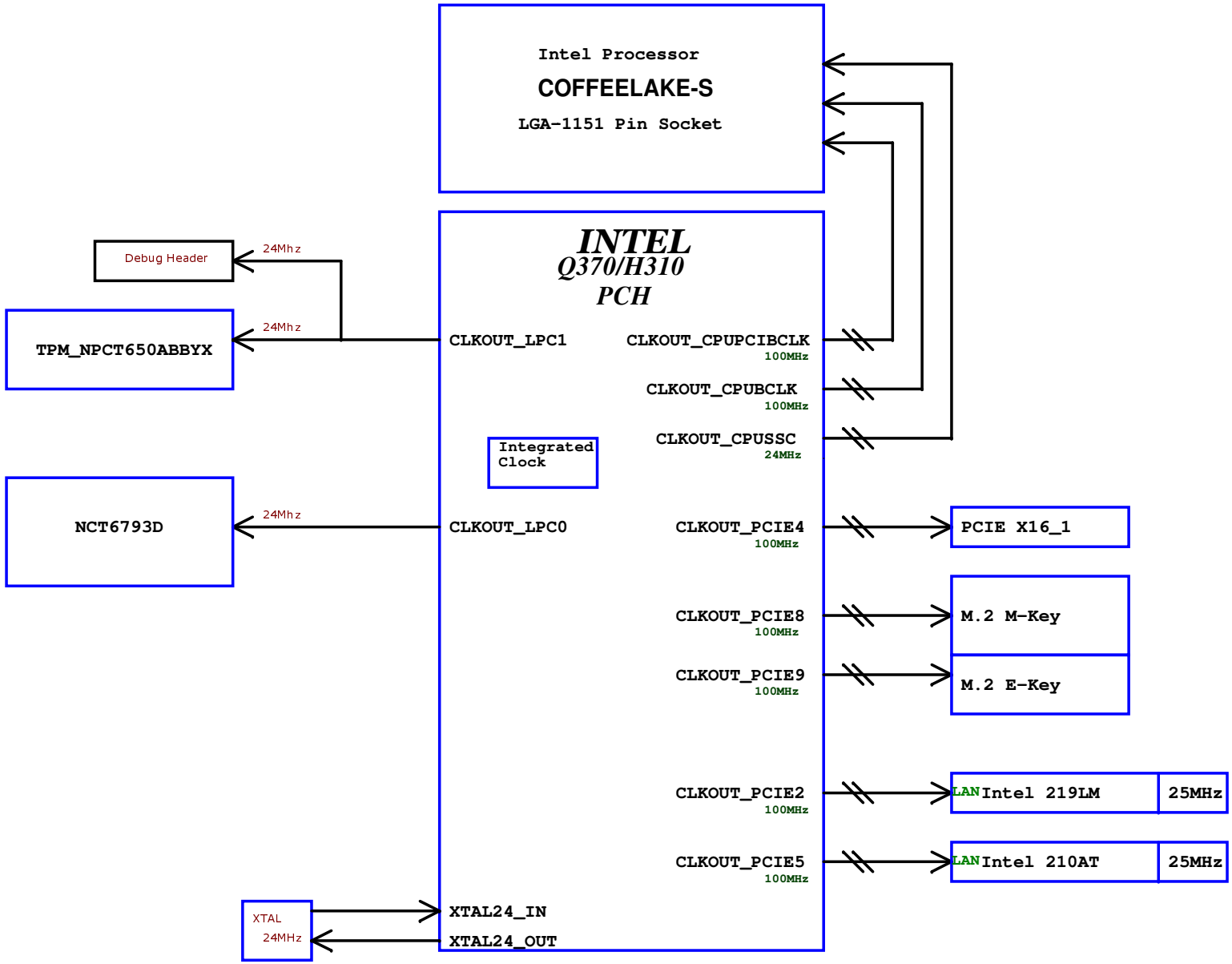
MIX-Q370D2
Block diagram

Rev 1.00



ASUSTeK COMPUTER INC.	Title : Block Diagram
	Engineer: IPC-EE3
Size: A2	Project Name: MIX-Q370D2
Rev: R1.00	
Date: Monday, October 14, 2019	Sheet 1 of 75



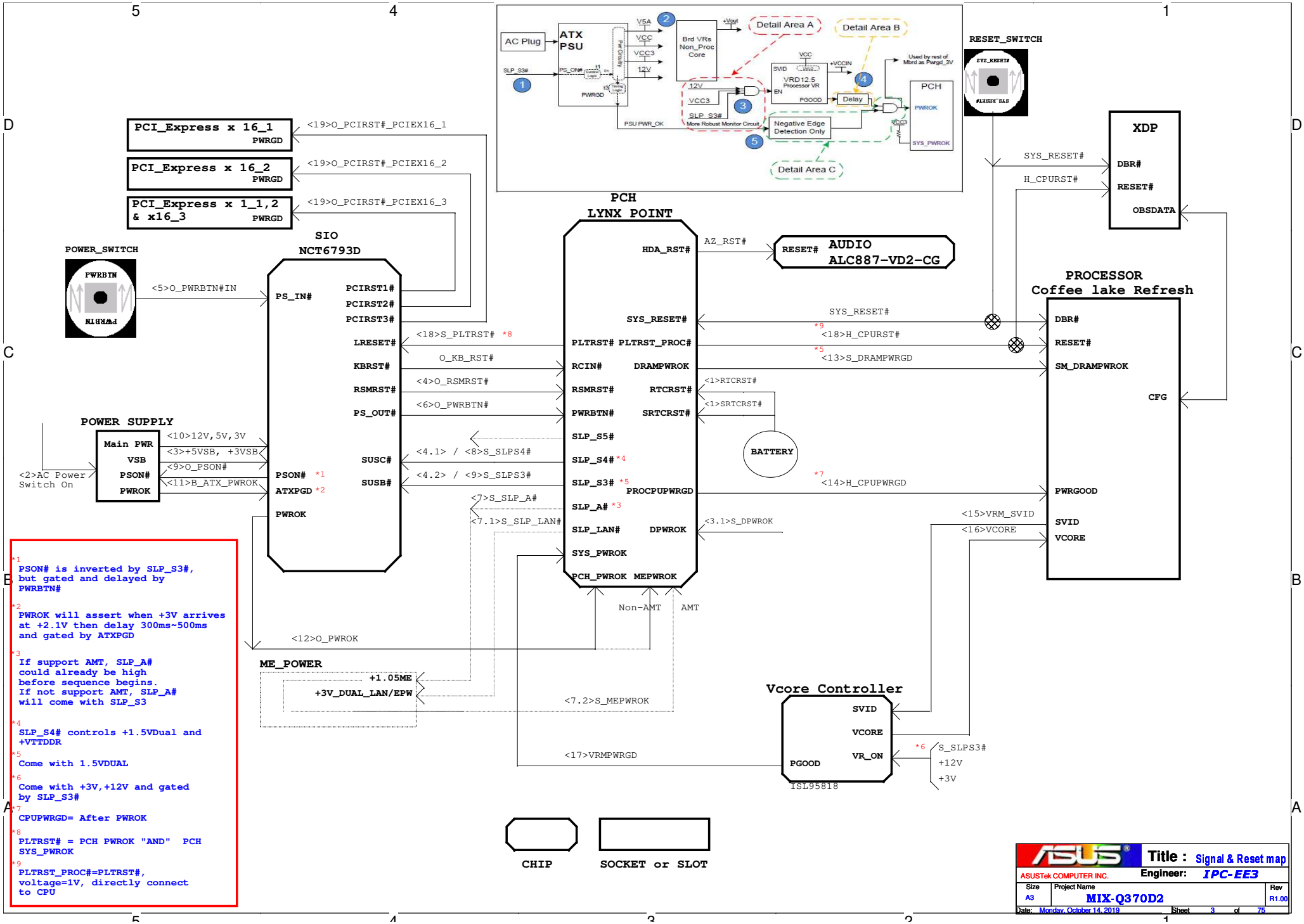
ASUSTek COMPUTER INC.

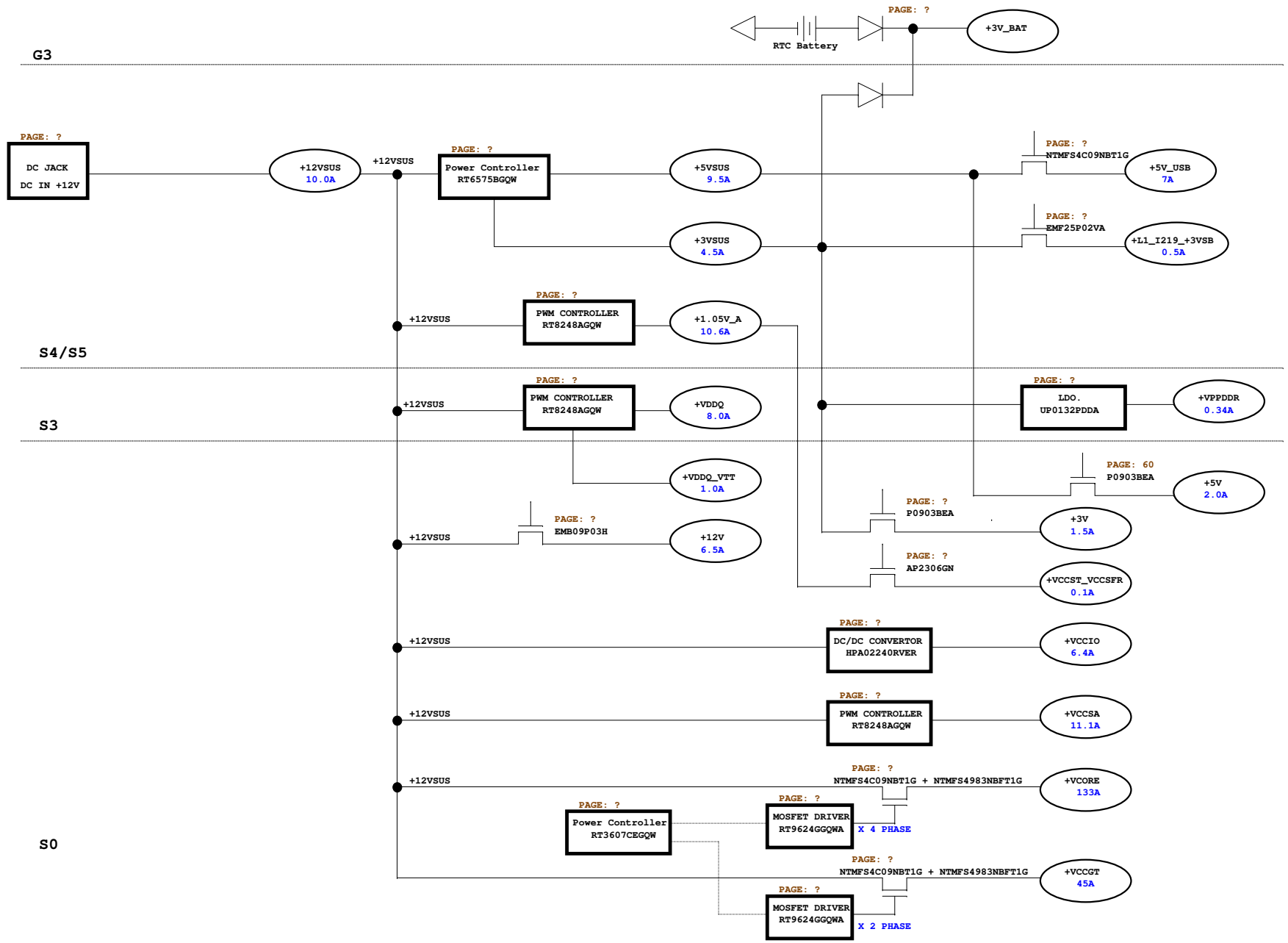
Title : Clock Distribution

Engineer: IPC-EE3

Size	Project Name	Rev
A3	MIX-Q370D2	R1.00

Date: Monday, October 14, 2019 Sheet 2 of 75


AC Plug
ATX PSU
SLP_S3#
PS_ON#
PWRGD
PSU PWR_OK
V5A
VCC
VCC3
12V
Brd VRs Non_Proc Core
+Vout
Detail Area A
Detail Area B
Detail Area C
VRD12.5 Processor VR
SVID
EN
PGOOD
+VCCIN
Delay
Negative Edge Detection Only
More Robust Monitor Circuit
Used by rest of Mbrd as Pwrgd_3V
PCH
PWROK
SYS_PWROK
RESET_SWITCH
SYS_RESET#
PCI_Express x 16_1
PWRGD
<19>O_PCIRST#_PCIEX16_1
PCI_Express x 16_2
PWRGD
<19>O_PCIRST#_PCIEX16_2
PCI_Express x 1_1,2 & x16_3
PWRGD
<19>O_PCIRST#_PCIEX16_3
POWER_SWITCH
PWRBTN
<5>O_PWRBTN#IN
SIO
NCT6793D
PS_IN#
PCIRST1#
PCIRST2#
PCIRST3#
LRESET#
KBRST#
RSMRST#
PS_OUT#
SUSC#
SUSB#
PSON# *1
ATXPGD *2
PWROK
<18>S_PLTRST# *8
O_KB_RST#
<4>O_RSMRST#
<6>O_PWRBTN#
<4.1> / <8>S_SLPS4#
<4.2> / <9>S_SLPS3#
<7>S_SLP_A#
<7.1>S_SLP_LAN#
PCH
LYNX POINT
HDA_RST#
AZ_RST#
RESET#
AUDIO
ALC887-VD2-CG
SYS_RESET#
PLTRST# PLTRST_PROC#
RCIN# DRAMPWROK
RSMRST# RTCRST#
PWRBTN# SRTCRST#
SLP_S5#
SLP_S4# *4
SLP_S3# *5
PROCPUPWRGD
SLP_A# *3
SLP_LAN# DPWROK
SYS_PWROK
PCH_PWROK MEPWROK
<1>RTCRST#
<1>SRTCRST#
BATTERY
<3.1>S_DPWROK
Non-AMT
AMT
XDP
DBR#
RESET#
OBSDATA
H_CPURST#
PROCESSOR
Coffee lake Refresh
SYS_RESET#
*9
<18>H_CPURST#
*5
<13>S_DRAMPWRGD
*7
<14>H_CPUPWRGD
DBR#
RESET#
SM_DRAMPWROK
CFG
PWRGOOD
SVID
VCORE
<15>VRM_SVID
<16>VCORE
POWER SUPPLY
Main PWR
VSB
PSON#
PWROK
<10>12V,5V,3V
<3>+5VSB, +3VSB
<9>O_PSON#
<11>B_ATX_PWROK
<2>AC Power Switch On
<12>O_PWROK
ME_POWER
+1.05ME
+3V_DUAL_LAN/EPW
<7.2>S_MEPWROK
Vcore Controller
SVID
VCORE
VR_ON
PGOOD
ISL95818
<17>VRMPWRGD
*6
S_SLPS3#
+12V
+3V
CHIP
SOCKET or SLOT
*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#
*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD
*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3
*4 SLP_S4# controls +1.5VDual and +VTTDDR
*5 Come with 1.5VDUAL
*6 Come with +3V,+12V and gated by SLP_S3#
*7 CPUPWRGD= After PWROK
*8 PLTRST# = PCH PWROK "AND" PCH SYS_PWROK
*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU
ASUS
Title : Signal & Reset map
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 3 of 75



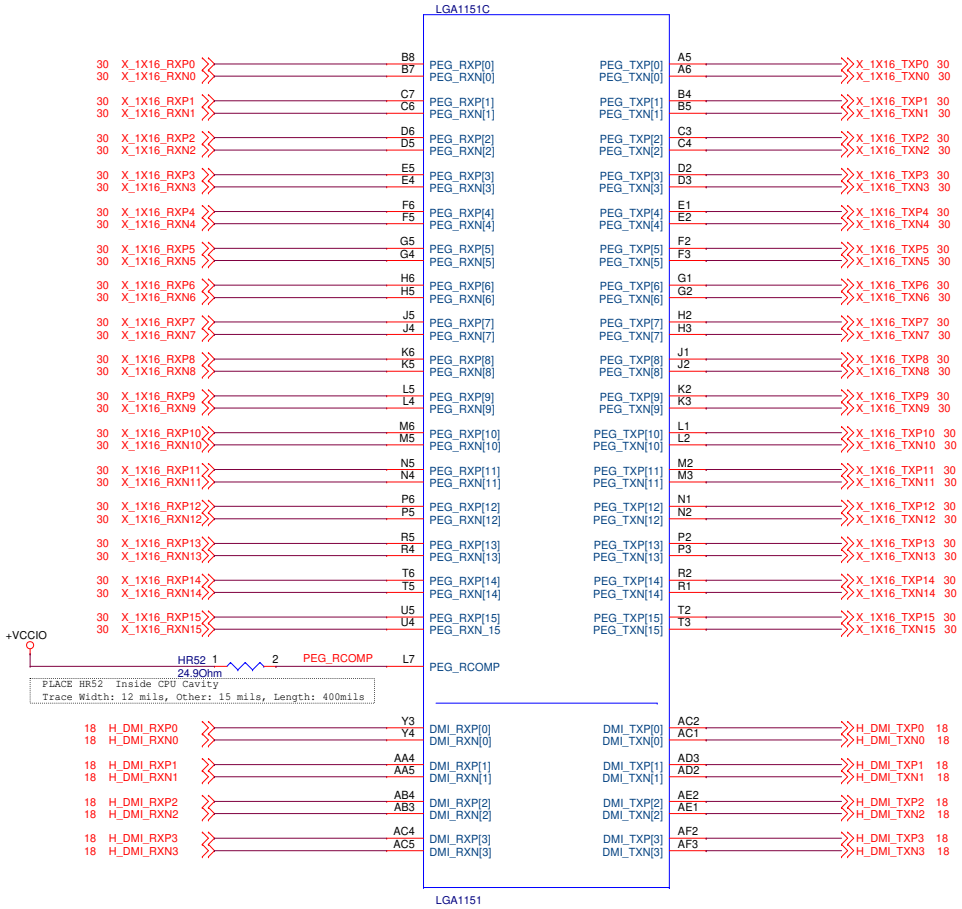
ASUSTeK COMPUTER INC.

Title : Power Flow

Engineer: IPC-EE3

Size	Project Name	Rev
Custom	MIX-Q370D2	R1.00

Date: Monday, October 14, 2019 Sheet 4 of 75



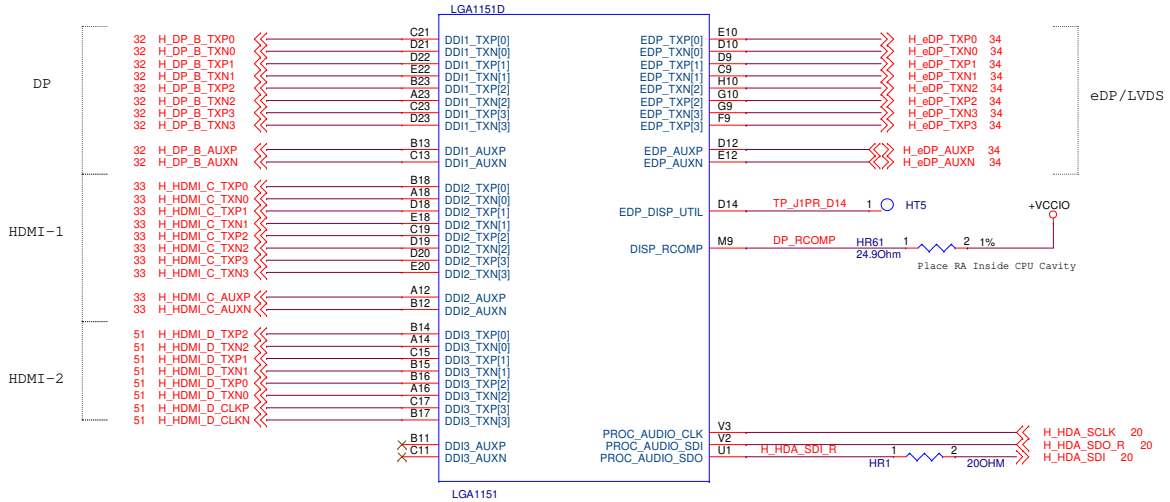
12001-00180200

LGA1151 LGA 1151P SOCKET 15U SMT

1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C

2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUS	Title : LGA1150 (DMI/PEG)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 5 of 75		



12001-00180200

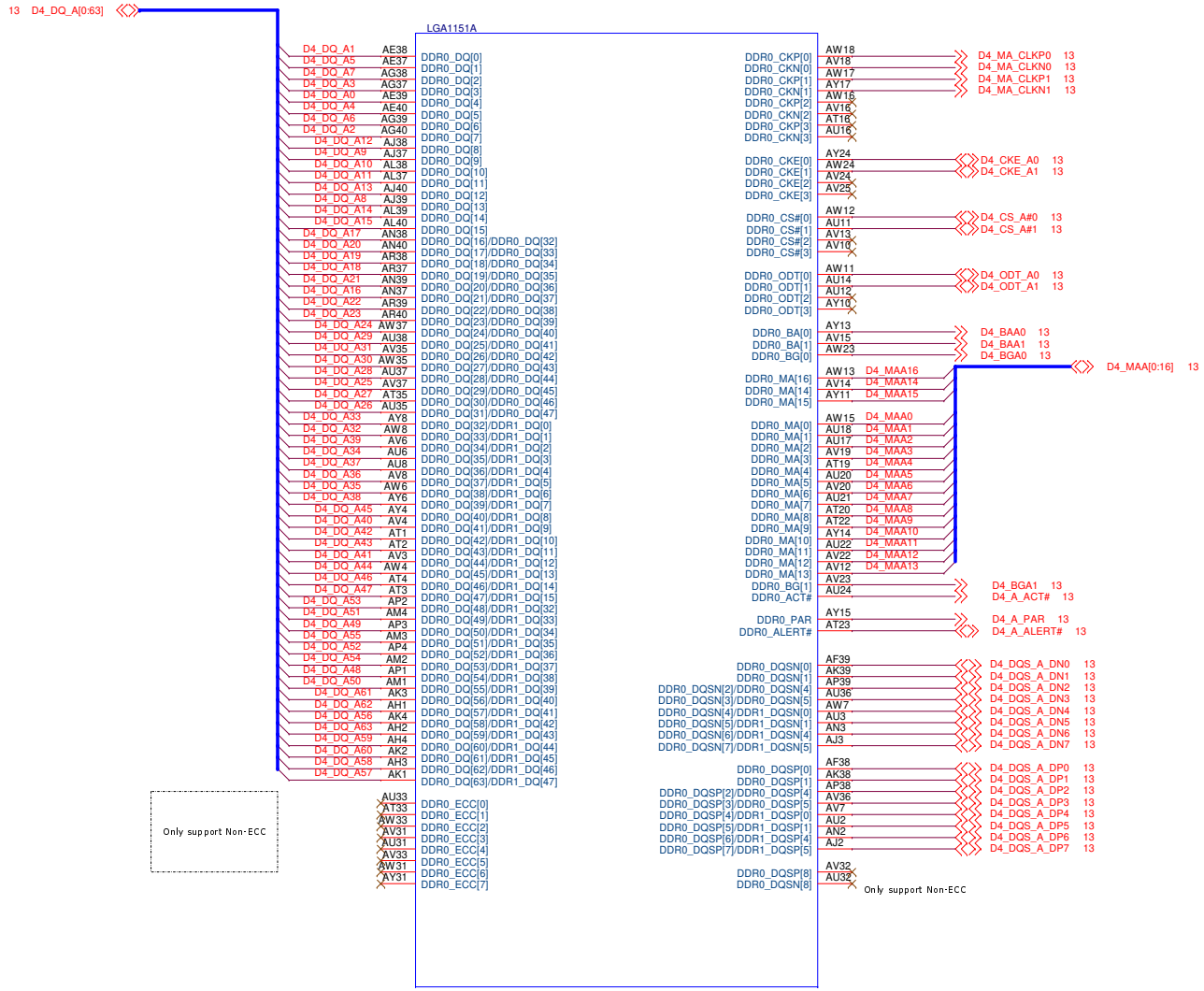
LGA1151 LGA 1151P SOCKET 15U SMT

1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C

2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUS	Title: LGA1150 (FDI/DISPLAY)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 6 of 75		

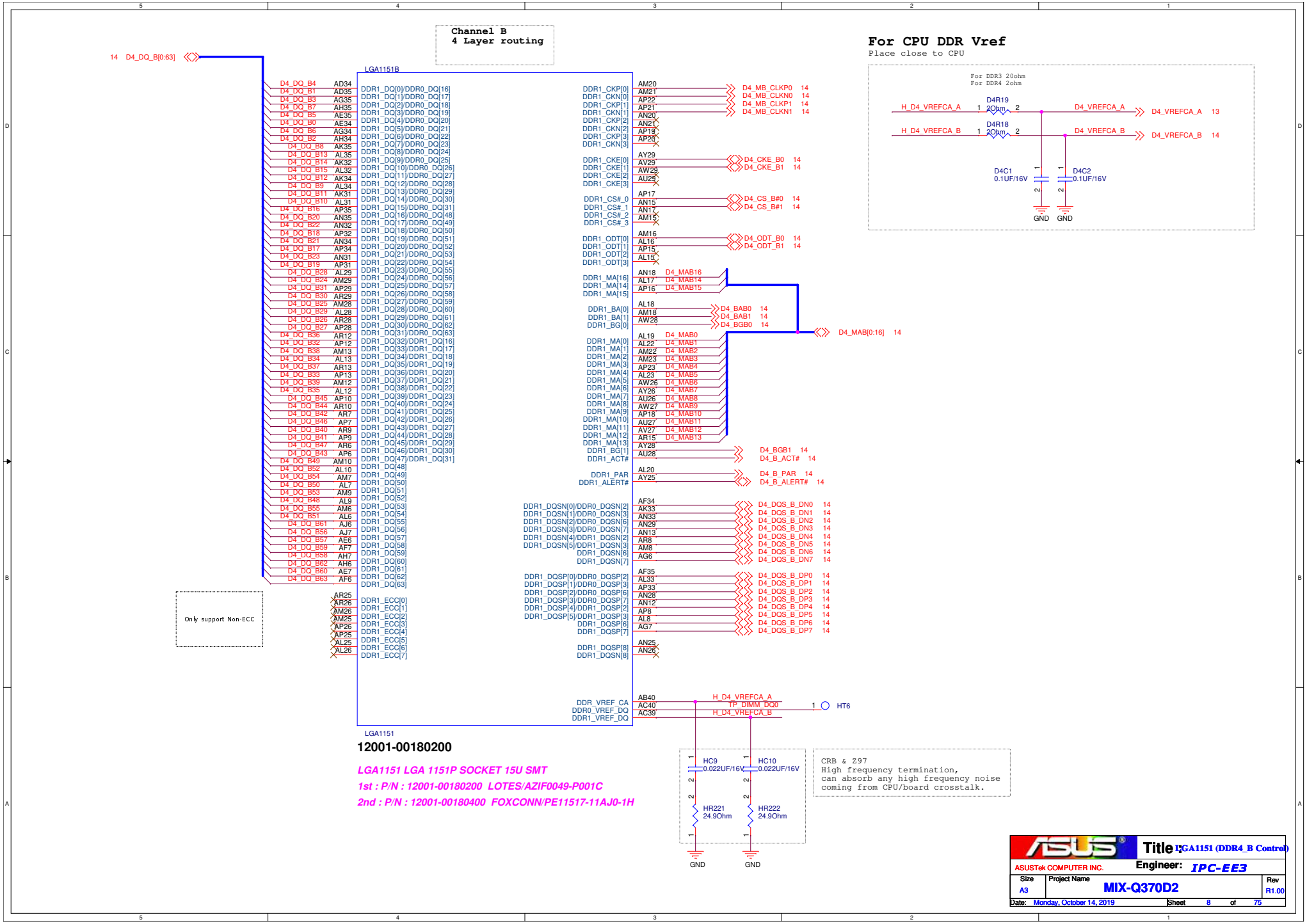
Channel A
4 Layer routing



12001-00180200

LGA1151 LGA 1151P SOCKET 15U SMT
1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C
2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUS	Title: LGA1151 (DDR4_A Control)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A3	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 7 of 75	



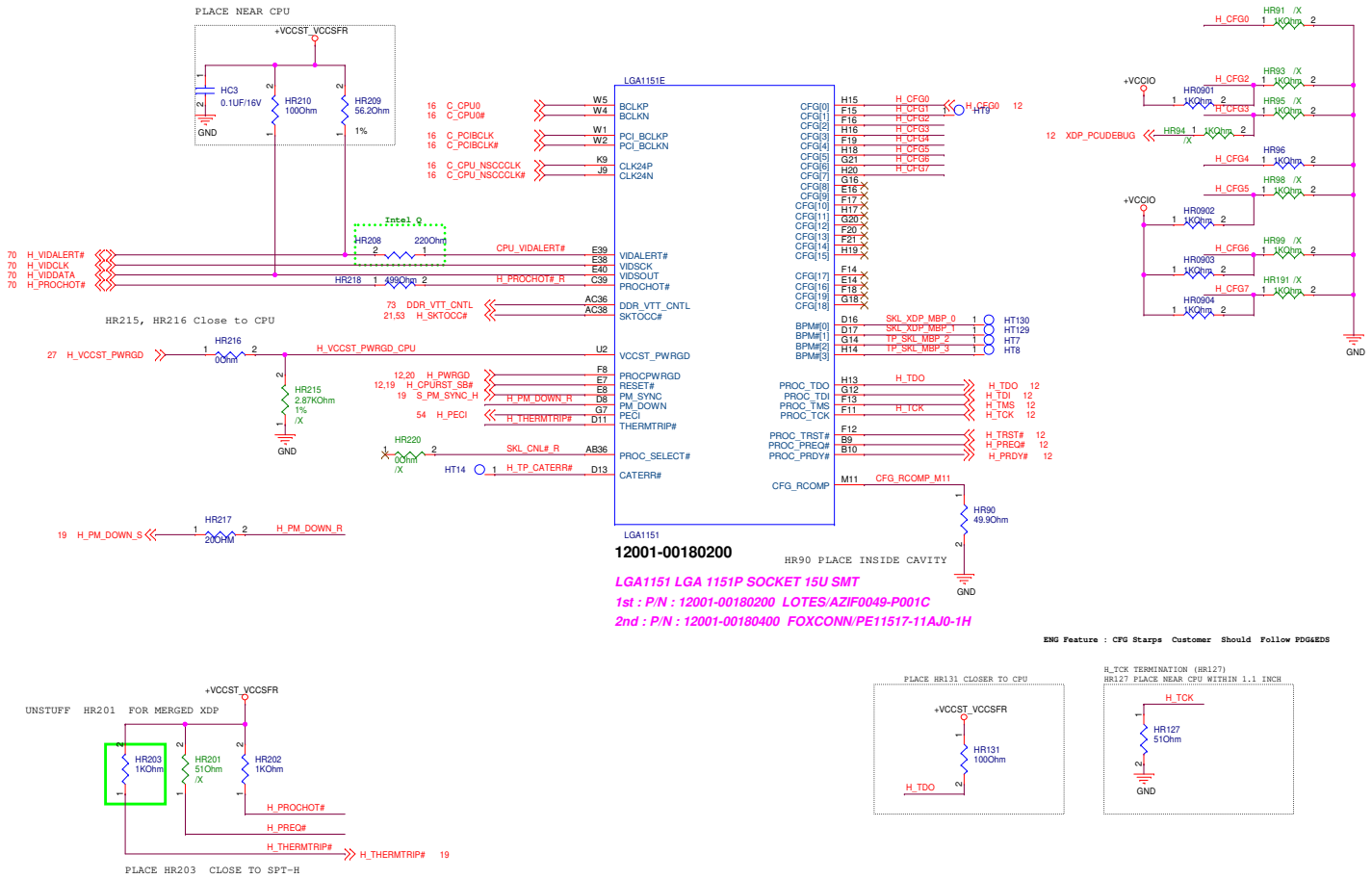
12001-00180200

LGA1151 LGA 1151P SOCKET 15U SMT

1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C

2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUS	Title: LGA1151 (DDR4_B Control)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 8 of 75		



CFG Straps for Processor

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane
Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes
Reserved Configuration Lane

CFG[4] : eDP Enable
- 1 : Disabled
- 0 : Enabled

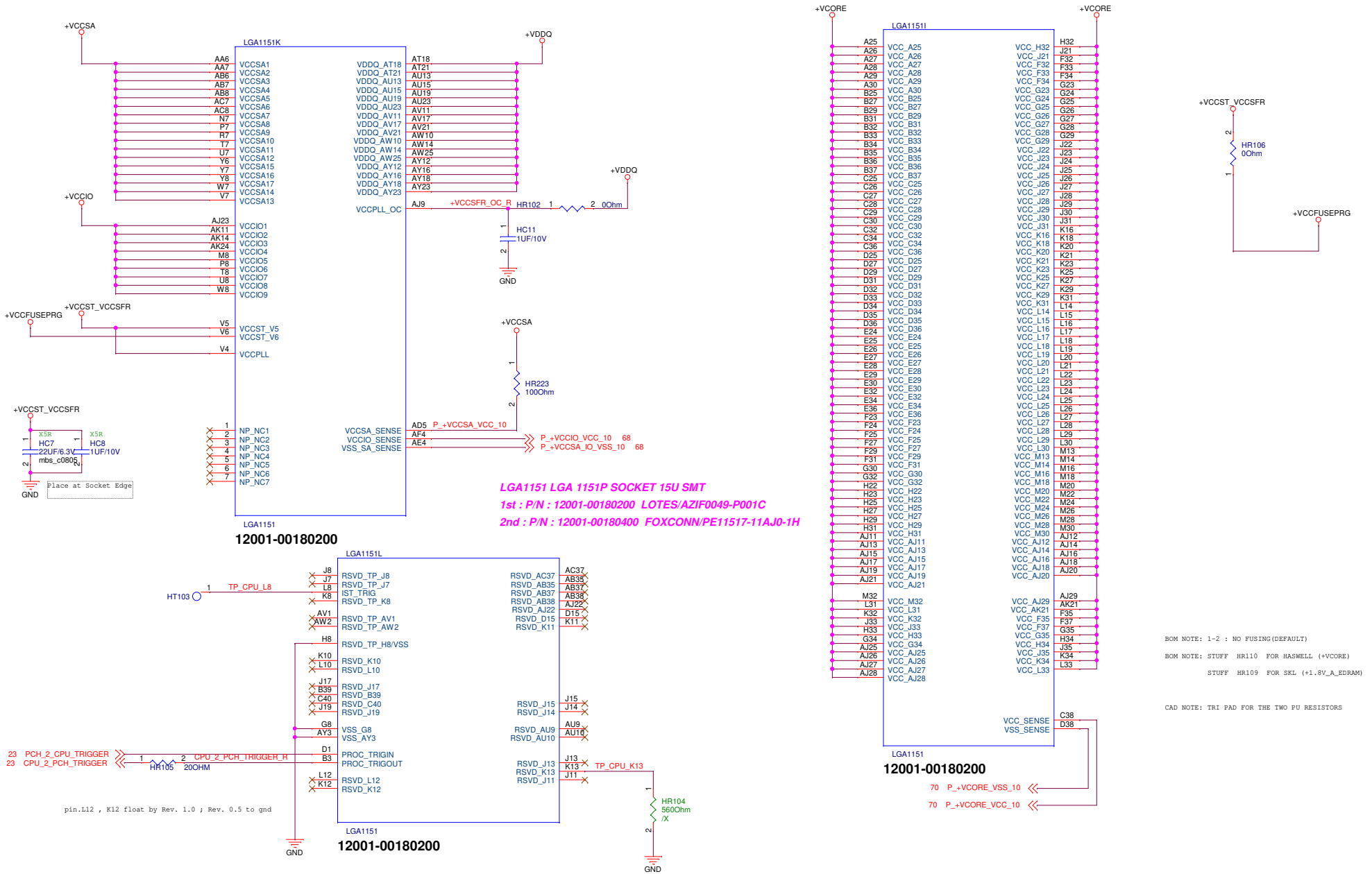
CFG[6:5] : PCI Expres* Bifurcation
- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

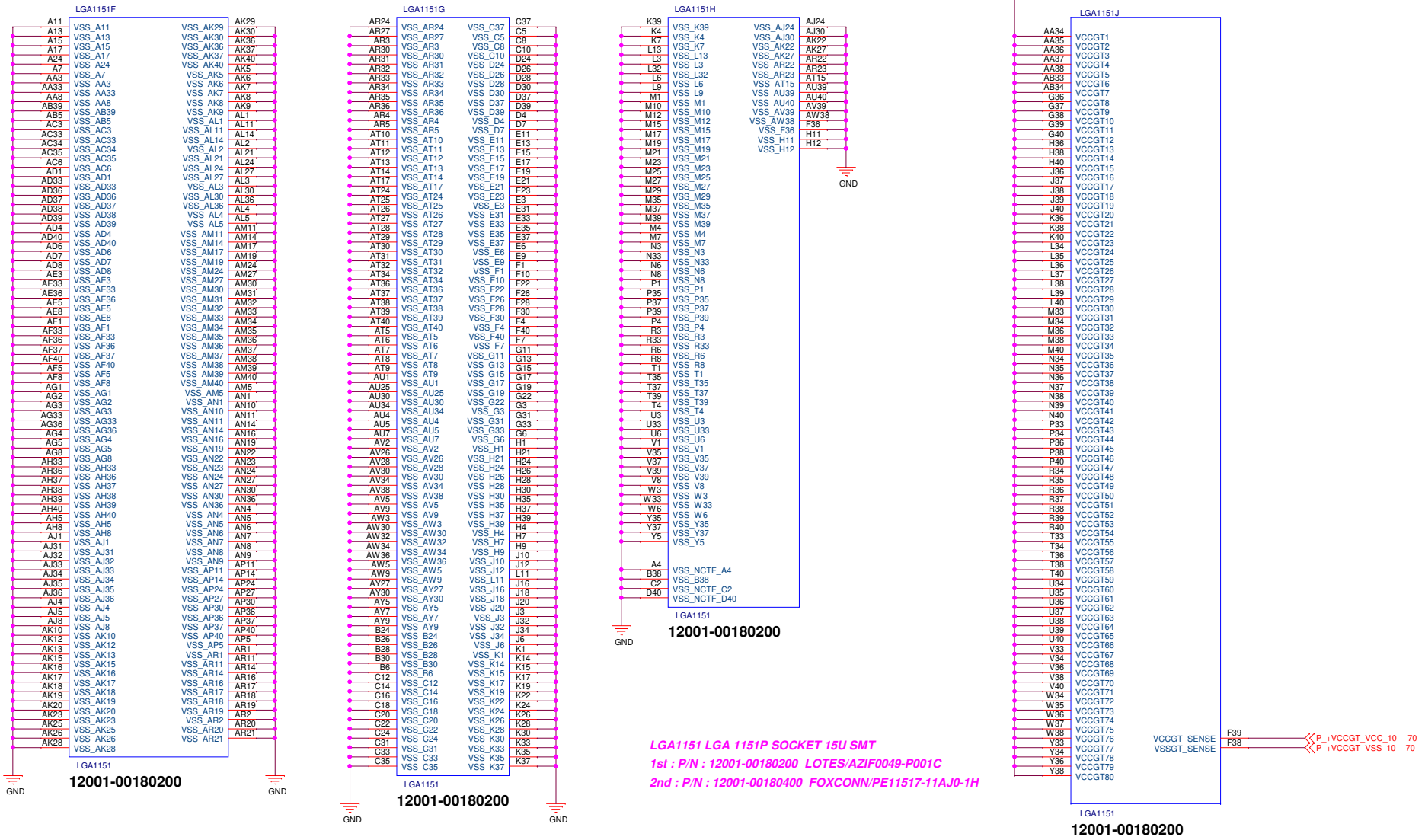
CFG[19:8] : Reserved Configuration Lanes
Reserved Configuration Lanes

Refer : Intel 570805_CFL_EDS_Vol1_Rev1.1, Table 6-7, P.116

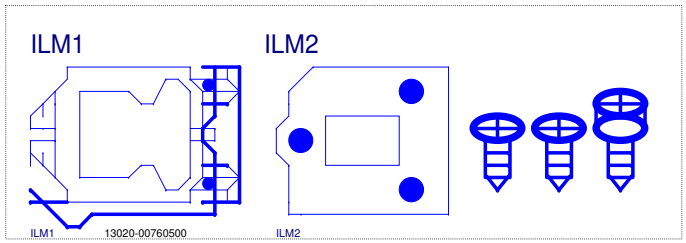
ASUSTek COMPUTER INC.	Title : LGA1151 (Control)	Engineer: IPC-EE3
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 9 of 75	



ASUS	Title : LGA1150 (POWER)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 10 of 75		



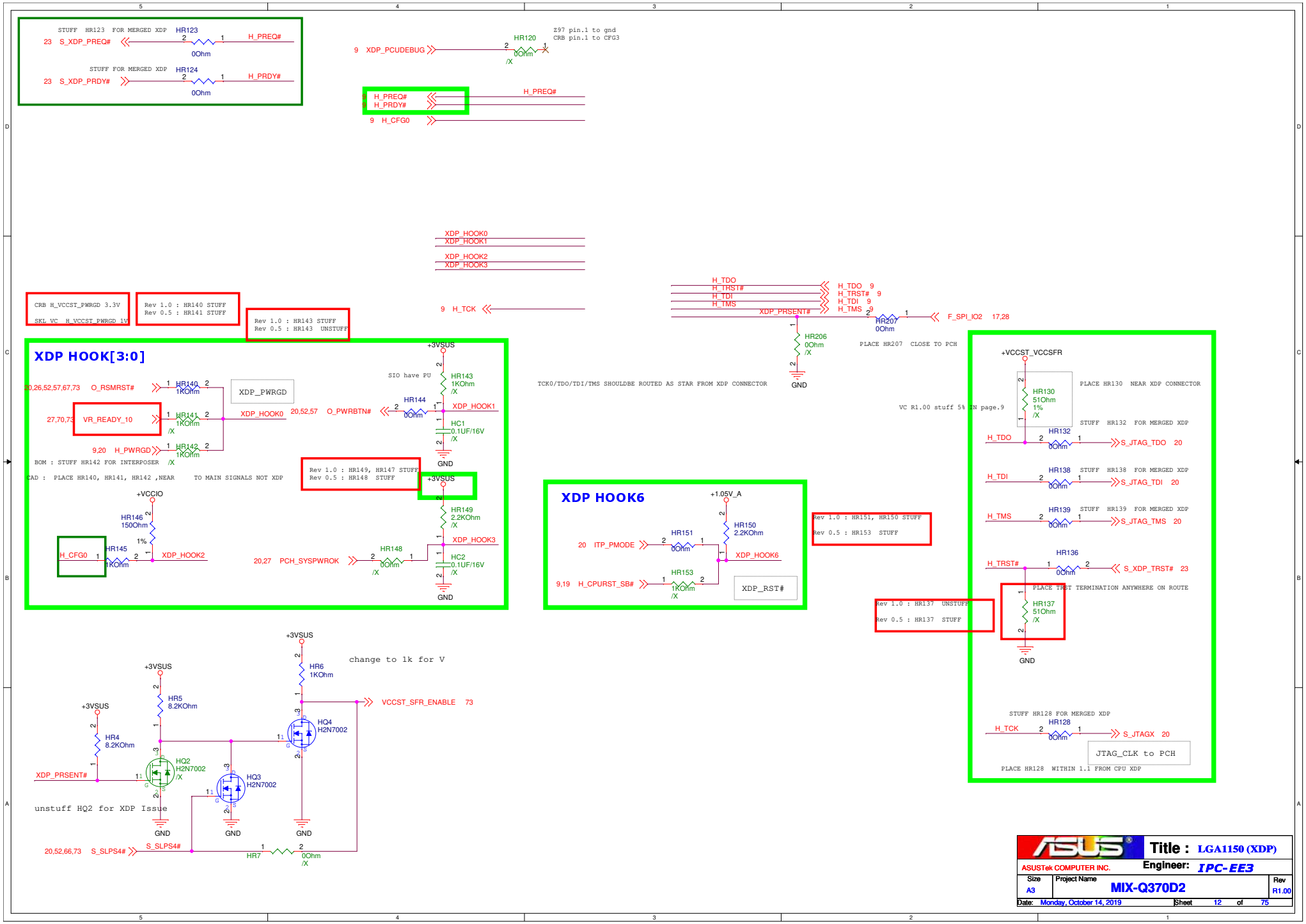
LGA1151 LGA 1151P SOCKET 15U SMT
1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C
2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

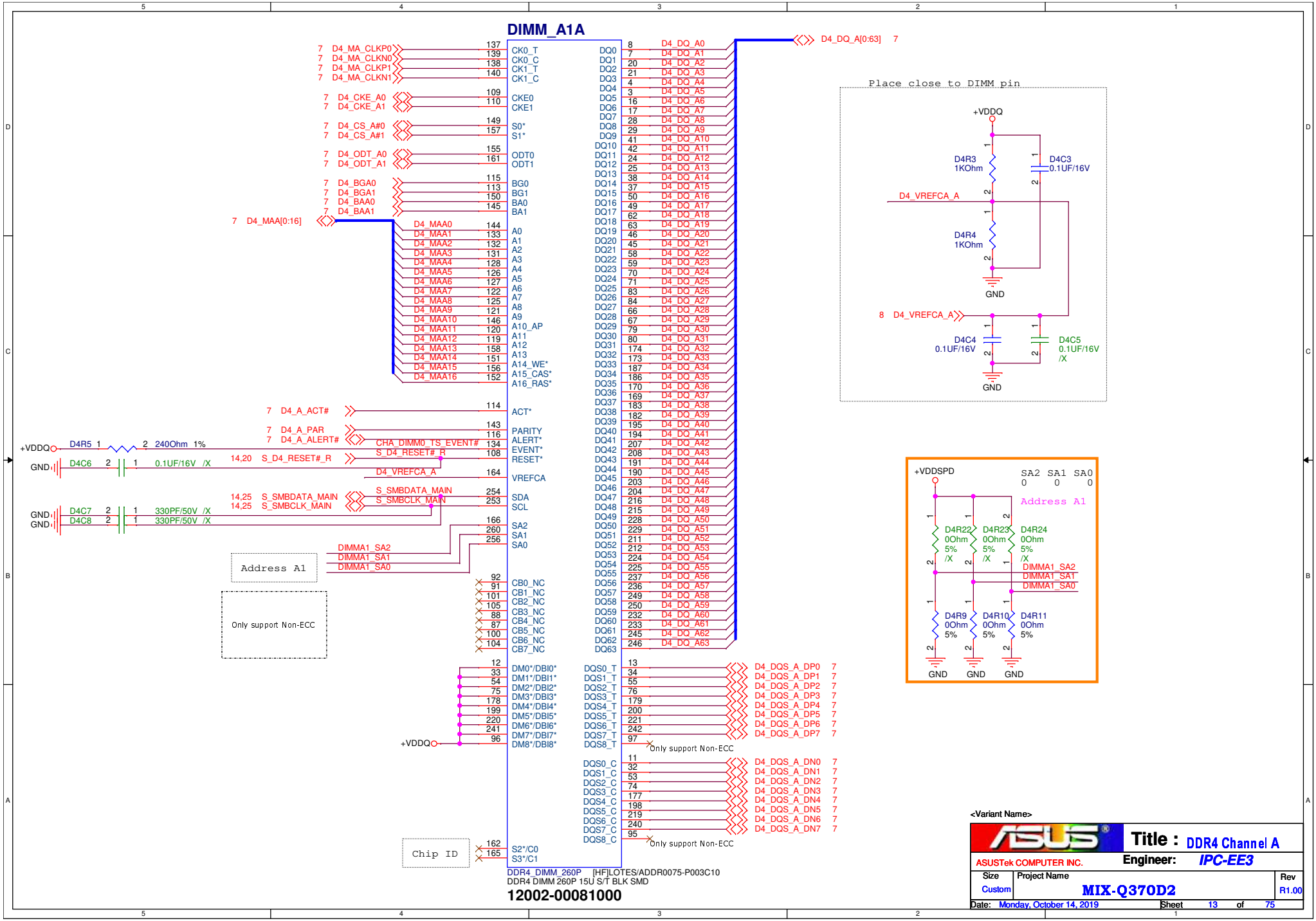


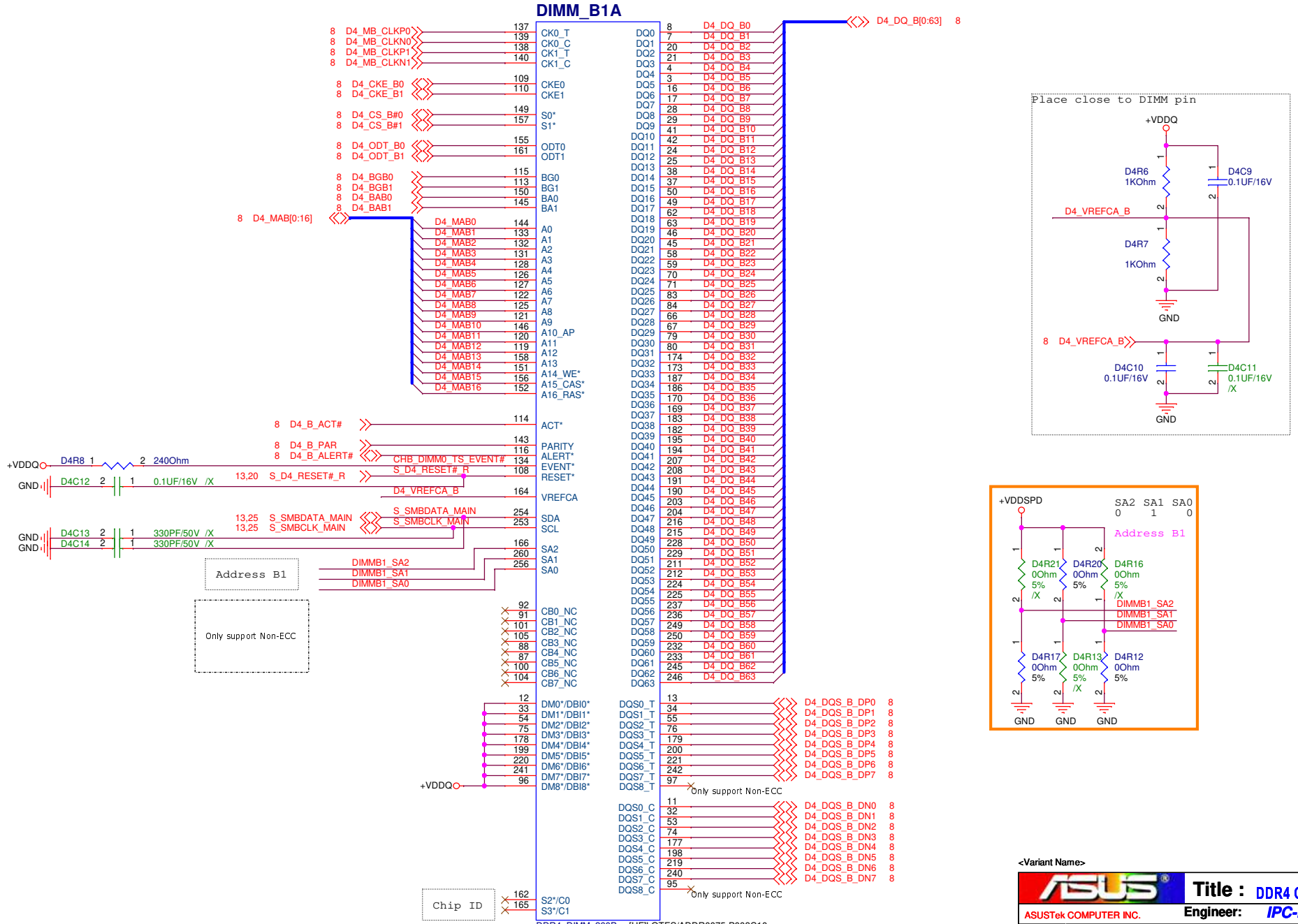
1. ILM + COVER P/N : 13020-00061900
2. BACKPLATE P/N : 13020-00062000 (替代料 13020-00061300)

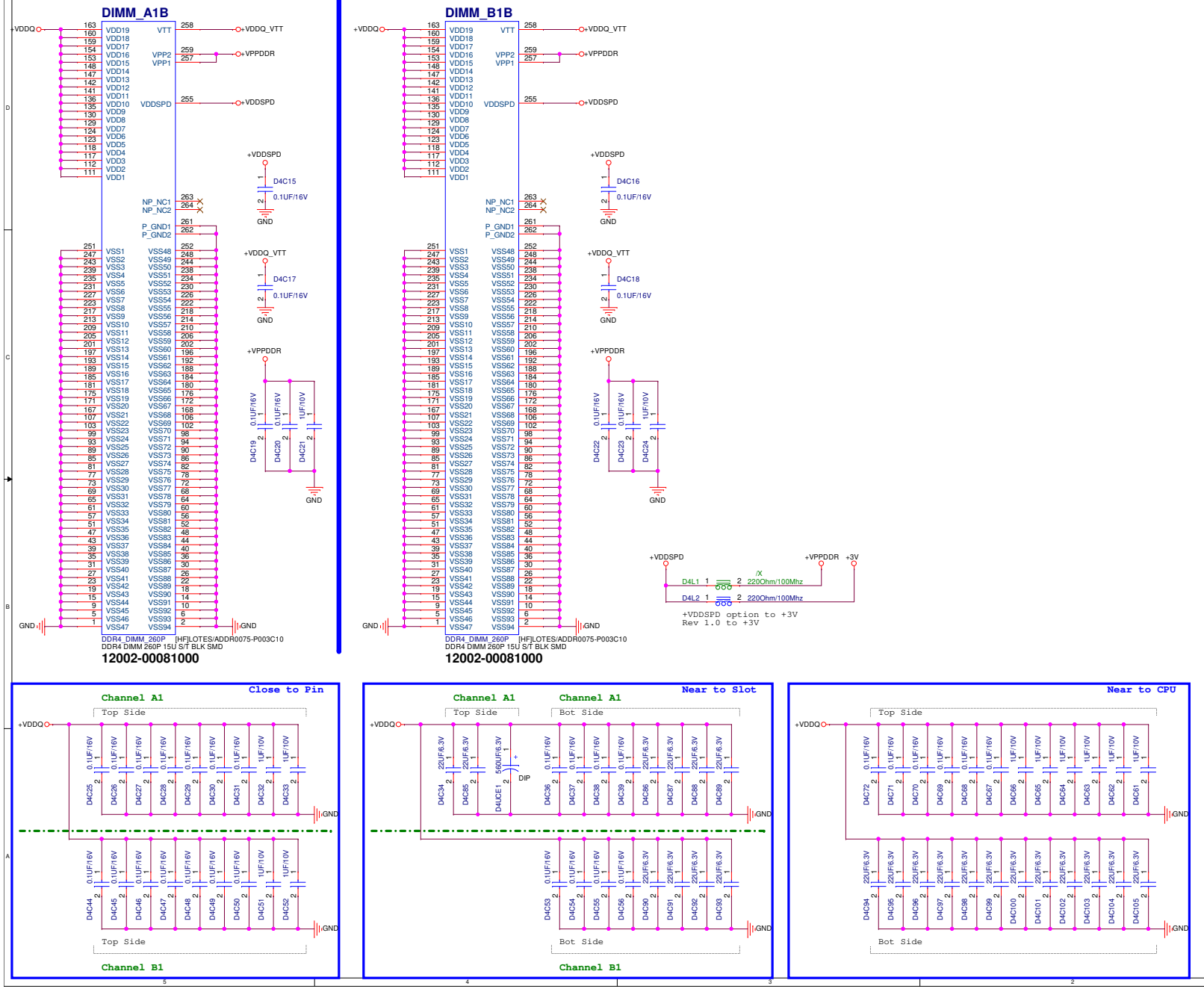
各別加入 BOM 內, Location 皆為 ILM1 , ILM2

ASUS	Title : LGA1151 (GND)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 11 of 75		


STUFF HR123 FOR MERGED XDP
HR123
23 S_XDP_PREQ#
H_PREQ#
0Ohm
STUFF FOR MERGED XDP
HR124
23 S_XDP_PRDY#
H_PRDY#
0Ohm
9 XDP_PCUDEBUG
HR120
0Ohm
/X
Z97 pin.1 to gnd
CRB pin.1 to CFG3
H_PREQ#
H_PRDY#
9 H_CFG0
XDP_HOOK0
XDP_HOOK1
XDP_HOOK2
XDP_HOOK3
9 H_TCK
H_TDO
H_TRST#
H_TDI
H_TMS
XDP_PRSENT#
H_TDO 9
H_TRST# 9
H_TDI 9
H_TMS 9
HR207
0Ohm
F_SPI_IO2 17,28
HR206
0Ohm
/X
GND
PLACE HR207 CLOSE TO PCH
TCK0/TDO/TDI/TMS SHOULDBE ROUTED AS STAR FROM XDP CONNECTOR
CRB H_VCCST_PWRGD 3.3V
SKL VC H_VCCST_PWRGD 1V
Rev 1.0 : HR140 STUFF
Rev 0.5 : HR141 STUFF
Rev 1.0 : HR143 STUFF
Rev 0.5 : HR143 UNSTUFF
XDP HOOK[3:0]
+3VSUS
SIO have PU
HR143
1KOhm
/X
20,26,52,57,67,73 O_RSMRST#
HR140
1KOhm
XDP_PWRGD
HR144
0Ohm
XDP_HOOK1
27,70,73 VR_READY_10
HR141
1KOhm
/X
XDP_HOOK0
20,52,57 O_PWRBTN#
HC1
0.1UF/16V
/X
9,20 H_PWRGD
HR142
1KOhm
/X
GND
BOM : STUFF HR142 FOR INTERPOSER
CAD : PLACE HR140, HR141, HR142 ,NEAR TO MAIN SIGNALS NOT XDP
Rev 1.0 : HR149, HR147 STUFF
Rev 0.5 : HR148 STUFF
+3VSUS
+VCCIO
HR146
150Ohm
1%
HR149
2.2KOhm
/X
H_CFG0
HR145
1KOhm
XDP_HOOK2
20,27 PCH_SYSPWROK
HR148
0Ohm
/X
XDP_HOOK3
HC2
0.1UF/16V
/X
GND
XDP HOOK6
+1.05V_A
HR151
0Ohm
HR150
2.2KOhm
20 ITP_PMODE
XDP_HOOK6
HR153
1KOhm
/X
9,19 H_CPURST_SB#
XDP_RST#
Rev 1.0 : HR151, HR150 STUFF
Rev 0.5 : HR153 STUFF
+VCCST_VCCSFR
HR130
51Ohm
1%
/X
PLACE HR130 NEAR XDP CONNECTOR
VC R1.00 stuff 5% IN page.9
STUFF HR132 FOR MERGED XDP
H_TDO
HR132
0Ohm
S_JTAG_TDO 20
H_TDI
HR138
0Ohm
STUFF HR138 FOR MERGED XDP
S_JTAG_TDI 20
H_TMS
HR139
0Ohm
STUFF HR139 FOR MERGED XDP
S_JTAG_TMS 20
HR136
H_TRST#
0Ohm
S_XDP_TRST# 23
PLACE TRST TERMINATION ANYWHERE ON ROUTE
HR137
51Ohm
/X
Rev 1.0 : HR137 UNSTUFF
Rev 0.5 : HR137 STUFF
GND
STUFF HR128 FOR MERGED XDP
H_TCK
HR128
0Ohm
S_JTAGX 20
JTAG_CLK to PCH
PLACE HR128 WITHIN 1.1 FROM CPU XDP
+3VSUS
HR6
1KOhm
change to 1k for V
VCCST_SFR_ENABLE 73
HR5
8.2KOhm
HQ4
H2N7002
HR4
8.2KOhm
HQ2
H2N7002
/X
XDP_PRSENT#
HQ3
H2N7002
unstuff HQ2 for XDP Issue
GND
GND
GND
20,52,66,73 S_SLPS4#
S_SLPS4#
HR7
0Ohm
/X
ASUS
Title : LGA1150 (XDP)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 12 of 75

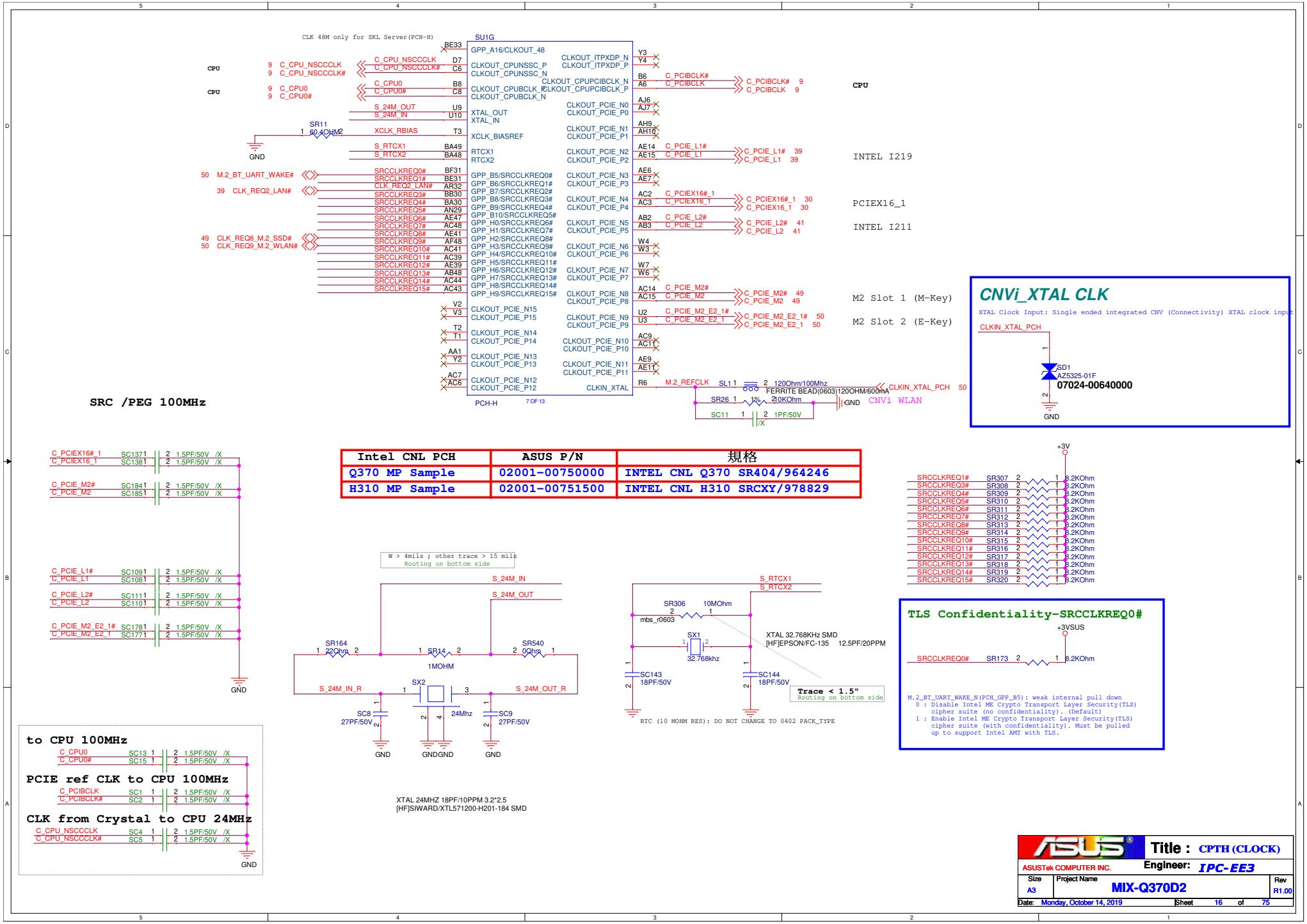

DIMM_A1A
7 D4_MA_CLKP0
7 D4_MA_CLKN0
7 D4_MA_CLKP1
7 D4_MA_CLKN1
7 D4_CKE_A0
7 D4_CKE_A1
7 D4_CS_A#0
7 D4_CS_A#1
7 D4_ODT_A0
7 D4_ODT_A1
7 D4_BGA0
7 D4_BGA1
7 D4_BAA0
7 D4_BAA1
7 D4_MAA[0:16]
7 D4_A_ACT#
7 D4_A_PAR
7 D4_A_ALERT#
CHA_DIMM0_TS_EVENT#
14,20 S_D4_RESET#_R
D4_VREFCA_A
14,25 S_SMBDATA_MAIN
14,25 S_SMBCLK_MAIN
DIMMA1_SA2
DIMMA1_SA1
DIMMA1_SA0
+VDDQ
GND
D4R5 240Ohm 1%
D4C6 0.1UF/16V /X
D4C7 330PF/50V /X
D4C8 330PF/50V /X
Address A1
Only support Non-ECC
Chip ID
CK0_T
CK0_C
CK1_T
CK1_C
CKE0
CKE1
S0*
S1*
ODT0
ODT1
BG0
BG1
BA0
BA1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10_AP
A11
A12
A13
A14_WE*
A15_CAS*
A16_RAS*
ACT*
PARITY
ALERT*
EVENT*
RESET*
VREFCA
SDA
SCL
SA2
SA1
SA0
CB0_NC
CB1_NC
CB2_NC
CB3_NC
CB4_NC
CB5_NC
CB6_NC
CB7_NC
DM0*/DBI0*
DM1*/DBI1*
DM2*/DBI2*
DM3*/DBI3*
DM4*/DBI4*
DM5*/DBI5*
DM6*/DBI6*
DM7*/DBI7*
DM8*/DBI8*
S2*/C0
S3*/C1
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63
D4_DQ_A0
D4_DQ_A1
D4_DQ_A2
D4_DQ_A3
D4_DQ_A4
D4_DQ_A5
D4_DQ_A6
D4_DQ_A7
D4_DQ_A8
D4_DQ_A9
D4_DQ_A10
D4_DQ_A11
D4_DQ_A12
D4_DQ_A13
D4_DQ_A14
D4_DQ_A15
D4_DQ_A16
D4_DQ_A17
D4_DQ_A18
D4_DQ_A19
D4_DQ_A20
D4_DQ_A21
D4_DQ_A22
D4_DQ_A23
D4_DQ_A24
D4_DQ_A25
D4_DQ_A26
D4_DQ_A27
D4_DQ_A28
D4_DQ_A29
D4_DQ_A30
D4_DQ_A31
D4_DQ_A32
D4_DQ_A33
D4_DQ_A34
D4_DQ_A35
D4_DQ_A36
D4_DQ_A37
D4_DQ_A38
D4_DQ_A39
D4_DQ_A40
D4_DQ_A41
D4_DQ_A42
D4_DQ_A43
D4_DQ_A44
D4_DQ_A45
D4_DQ_A46
D4_DQ_A47
D4_DQ_A48
D4_DQ_A49
D4_DQ_A50
D4_DQ_A51
D4_DQ_A52
D4_DQ_A53
D4_DQ_A54
D4_DQ_A55
D4_DQ_A56
D4_DQ_A57
D4_DQ_A58
D4_DQ_A59
D4_DQ_A60
D4_DQ_A61
D4_DQ_A62
D4_DQ_A63
D4_DQ_A[0:63] 7
DQS0_T
DQS1_T
DQS2_T
DQS3_T
DQS4_T
DQS5_T
DQS6_T
DQS7_T
DQS8_T
D4_DQS_A_DP0 7
D4_DQS_A_DP1 7
D4_DQS_A_DP2 7
D4_DQS_A_DP3 7
D4_DQS_A_DP4 7
D4_DQS_A_DP5 7
D4_DQS_A_DP6 7
D4_DQS_A_DP7 7
Only support Non-ECC
DQS0_C
DQS1_C
DQS2_C
DQS3_C
DQS4_C
DQS5_C
DQS6_C
DQS7_C
DQS8_C
D4_DQS_A_DN0 7
D4_DQS_A_DN1 7
D4_DQS_A_DN2 7
D4_DQS_A_DN3 7
D4_DQS_A_DN4 7
D4_DQS_A_DN5 7
D4_DQS_A_DN6 7
D4_DQS_A_DN7 7
Only support Non-ECC
DDR4_DIMM_260P [HF]LOTES/ADDR0075-P003C10
DDR4 DIMM 260P 15U S/T BLK SMD
12002-00081000
Place close to DIMM pin
+VDDQ
D4R3 1KOhm
D4C3 0.1UF/16V
D4_VREFCA_A
D4R4 1KOhm
GND
8 D4_VREFCA_A
D4C4 0.1UF/16V
D4C5 0.1UF/16V /X
+VDDSPD
SA2 SA1 SA0
0 0 0
Address A1
D4R22 0Ohm 5% /X
D4R23 0Ohm 5% /X
D4R24 0Ohm 5% /X
DIMMA1_SA2
DIMMA1_SA1
DIMMA1_SA0
D4R9 0Ohm 5%
D4R10 0Ohm 5%
D4R11 0Ohm 5%
GND GND GND
<Variant Name>
Title : DDR4 Channel A
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 13 of 75


DIMM_B1A
8 D4_MB_CLKP0
8 D4_MB_CLKN0
8 D4_MB_CLKP1
8 D4_MB_CLKN1
8 D4_CKE_B0
8 D4_CKE_B1
8 D4_CS_B#0
8 D4_CS_B#1
8 D4_ODT_B0
8 D4_ODT_B1
8 D4_BGB0
8 D4_BGB1
8 D4_BAB0
8 D4_BAB1
8 D4_MAB[0:16]
8 D4_B_ACT#
8 D4_B_PAR
8 D4_B_ALERT#
+VDDQ
D4R8 240Ohm
GND
D4C12 0.1UF/16V /X
13,20 S_D4_RESET#_R
CHB_DIMM0_TS_EVENT#
S_D4_RESET#_R
D4_VREFCA_B
13,25 S_SMBDATA_MAIN
13,25 S_SMBCLK_MAIN
D4C13 330PF/50V /X
D4C14 330PF/50V /X
Address B1
DIMMB1_SA2
DIMMB1_SA1
DIMMB1_SA0
Only support Non-ECC
CK0_T
CK0_C
CK1_T
CK1_C
CKE0
CKE1
S0*
S1*
ODT0
ODT1
BG0
BG1
BA0
BA1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10_AP
A11
A12
A13
A14_WE*
A15_CAS*
A16_RAS*
ACT*
PARITY
ALERT*
EVENT*
RESET*
VREFCA
SDA
SCL
SA2
SA1
SA0
CB0_NC
CB1_NC
CB2_NC
CB3_NC
CB4_NC
CB5_NC
CB6_NC
CB7_NC
DM0*/DBI0*
DM1*/DBI1*
DM2*/DBI2*
DM3*/DBI3*
DM4*/DBI4*
DM5*/DBI5*
DM6*/DBI6*
DM7*/DBI7*
DM8*/DBI8*
DQS0_T
DQS1_T
DQS2_T
DQS3_T
DQS4_T
DQS5_T
DQS6_T
DQS7_T
DQS8_T
DQS0_C
DQS1_C
DQS2_C
DQS3_C
DQS4_C
DQS5_C
DQS6_C
DQS7_C
DQS8_C
Only support Non-ECC
Chip ID
S2*/C0
S3*/C1
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63
D4_DQ_B[0:63] 8
D4_DQS_B_DP0 8
D4_DQS_B_DP1 8
D4_DQS_B_DP2 8
D4_DQS_B_DP3 8
D4_DQS_B_DP4 8
D4_DQS_B_DP5 8
D4_DQS_B_DP6 8
D4_DQS_B_DP7 8
D4_DQS_B_DN0 8
D4_DQS_B_DN1 8
D4_DQS_B_DN2 8
D4_DQS_B_DN3 8
D4_DQS_B_DN4 8
D4_DQS_B_DN5 8
D4_DQS_B_DN6 8
D4_DQS_B_DN7 8
DDR4_DIMM_260P [HF]LOTES/ADDR0075-P003C10
DDR4 DIMM 260P 15U S/T BLK SMD
12002-00081000
Place close to DIMM pin
+VDDQ
D4R6 1KOhm
D4C9 0.1UF/16V
D4_VREFCA_B
D4R7 1KOhm
GND
8 D4_VREFCA_B
D4C10 0.1UF/16V
D4C11 0.1UF/16V /X
+VDDSPD
SA2 SA1 SA0
0 1 0
Address B1
D4R21 0Ohm 5% /X
D4R20 0Ohm 5%
D4R16 0Ohm 5% /X
DIMMB1_SA2
DIMMB1_SA1
DIMMB1_SA0
D4R17 0Ohm 5%
D4R13 0Ohm 5% /X
D4R12 0Ohm 5%
GND GND GND
<Variant Name>
Title : DDR4 Channel B
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 14 of 75

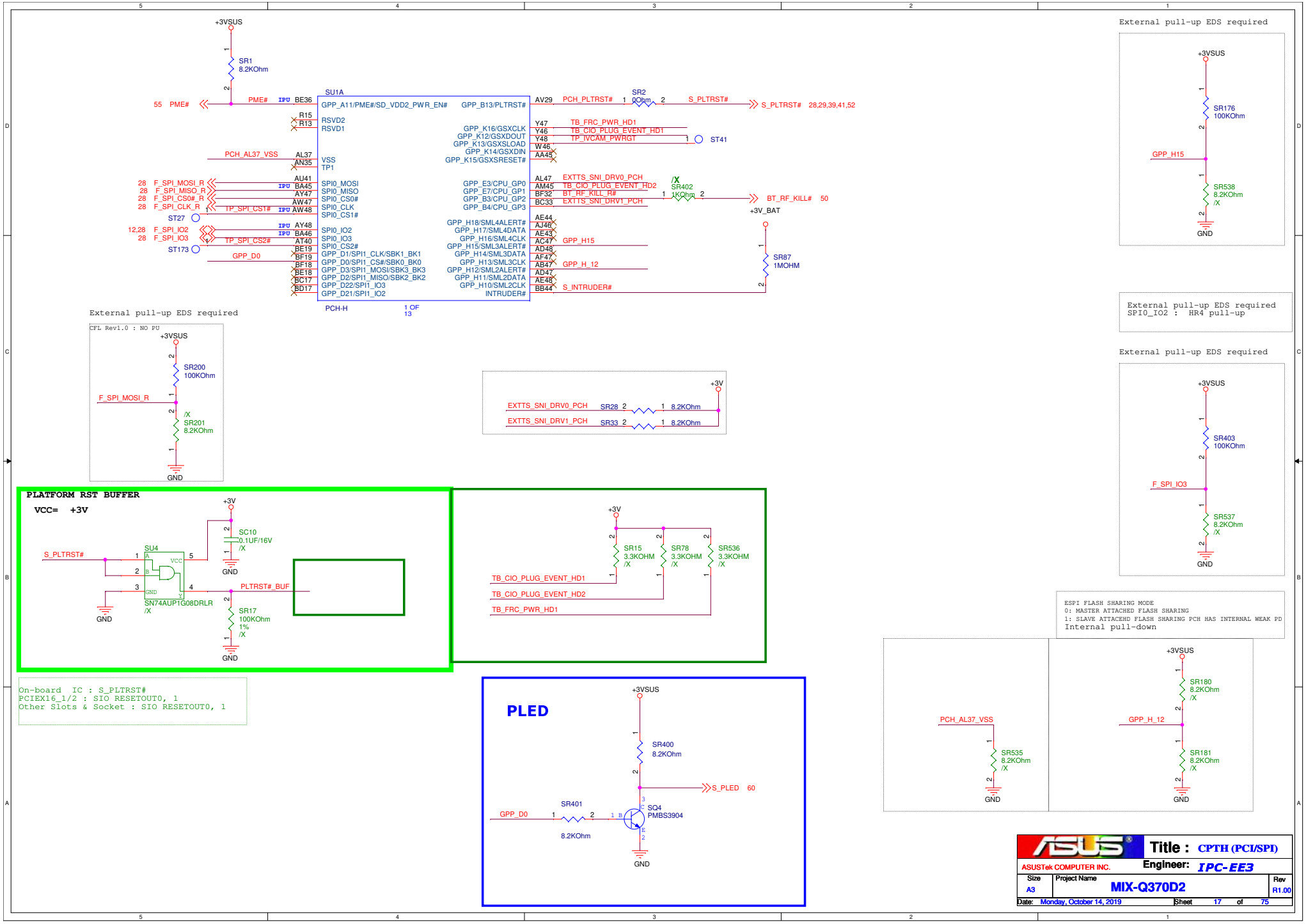


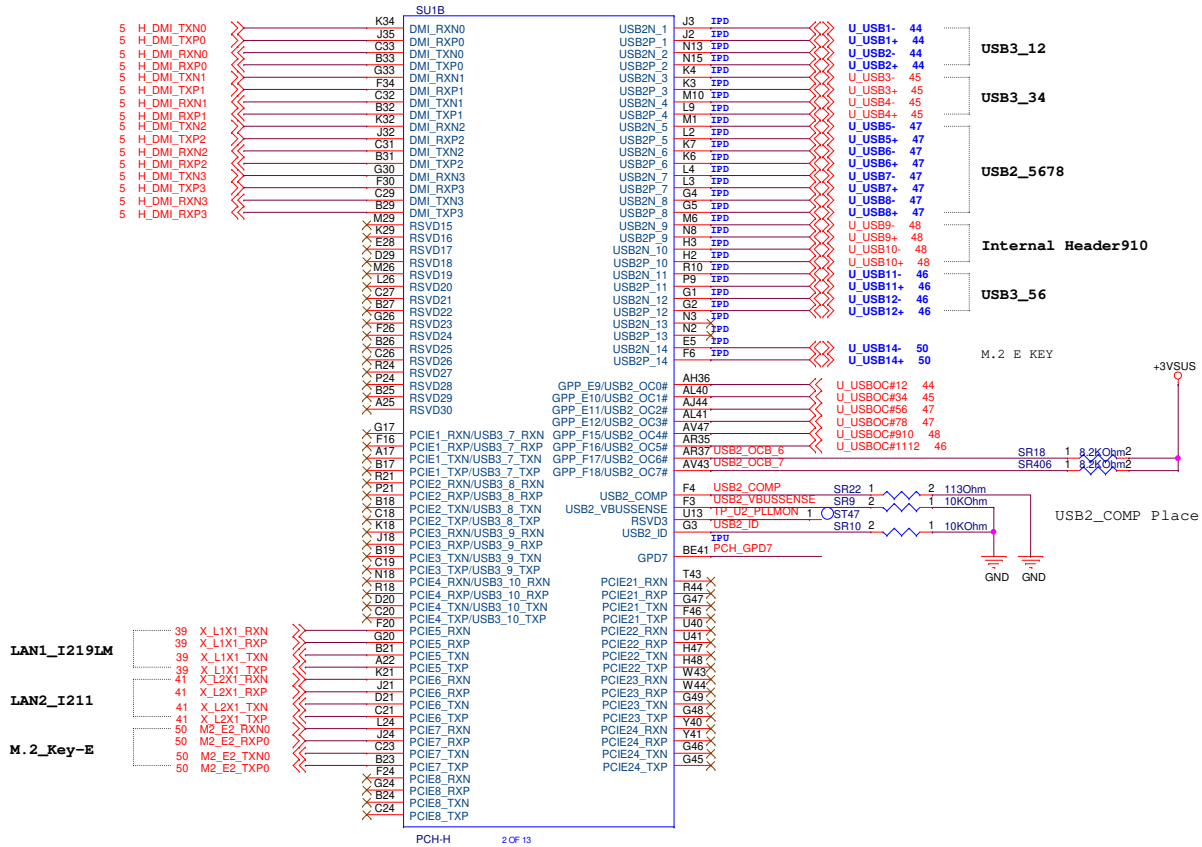
<Variant Name>

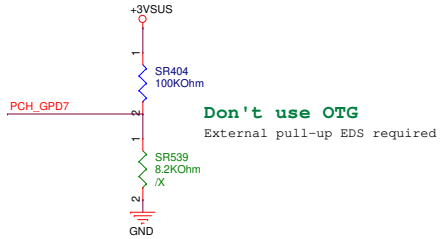
ASUSTek COMPUTER INC.	Title : DDR4 (Power)	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 15 of 75	



Intel CNL PCH	ASUS P/N	規格
Q370 MP Sample	02001-00750000	INTEL CNL Q370 SR404/964246
H310 MP Sample	02001-00751500	INTEL CNL H310 SRCXY/978829


+3VSUS
SR1
8.2KOhm
55 PME#
PME# IPU BE36
SU1A
GPP_A11/PME#/SD_VDD2_PWR_EN#
GPP_B13/PLTRST#
AV29 PCH_PLTRST# SR2 0Ohm S_PLTRST#
S_PLTRST# 28,29,39,41,52
R15
R13
RSVD2
RSVD1
GPP_K16/GSXCLK
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
Y47 TB_FRC_PWR_HD1
Y46 TB_CIO_PLUG_EVENT_HD1
Y48 TP_IVCAM_PWRGT
ST41
W46
AA45
PCH_AL37_VSS AL37
AN35
VSS
TP1
28 F_SPI_MOSI_R AU41
28 F_SPI_MISO_R IPU BA45
28 F_SPI_CS0#_R AY47
28 F_SPI_CLK_R AW47
TP_SPI_CS1# IPU AW48
ST27
12,28 F_SPI_IO2 IPU AY48
28 F_SPI_IO3 IPU BA46
TP_SPI_CS2# AT40
ST173
GPP_D0 BE19
BF19
BF18
BE18
BC17
BD17
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_D1/SPI1_CLK/SBK1_BK1
GPP_D0/SPI1_CS#/SBK0_BK0
GPP_D3/SPI1_MOSI/SBK3_BK3
GPP_D2/SPI1_MISO/SBK2_BK2
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
AL47 EXTTS_SNI_DRV0_PCH
AM45 TB_CIO_PLUG_EVENT_HD2
BF32 BT_RF_KILL_R#
BC33 EXTTS_SNI_DRV1_PCH
/X SR402 1KOhm
BT_RF_KILL# 50
+3V_BAT
AE44
AJ46
AE43
AC47 GPP_H15
AD48
AF47
AB47 GPP_H_12
AD47
AE48
BB44 S_INTRUDER#
SR87 1MOHM
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
PCH-H
1 OF 13
External pull-up EDS required
CFL Rev1.0 : NO PU
+3VSUS
SR200
100KOhm
F_SPI_MOSI_R
/X
SR201
8.2KOhm
GND
+3V
EXTTS_SNI_DRV0_PCH SR28 8.2KOhm
EXTTS_SNI_DRV1_PCH SR33 8.2KOhm
PLATFORM RST BUFFER
VCC= +3V
+3V
SC10
0.1UF/16V
/X
GND
S_PLTRST#
SU4
VCC
GND
SN74AUP1G08DRLR
/X
PLTRST#_BUF
SR17
100KOhm
1%
/X
GND
+3V
SR15
3.3KOHM
/X
SR78
3.3KOHM
/X
SR536
3.3KOHM
/X
TB_CIO_PLUG_EVENT_HD1
TB_CIO_PLUG_EVENT_HD2
TB_FRC_PWR_HD1
On-board IC : S_PLTRST#
PCIEX16_1/2 : SIO RESETOUT0, 1
Other Slots & Socket : SIO RESETOUT0, 1
PLED
+3VSUS
SR400
8.2KOhm
S_PLED 60
SR401
GPP_D0
SQ4
PMBS3904
8.2KOhm
GND
External pull-up EDS required
+3VSUS
SR176
100KOhm
GPP_H15
SR538
8.2KOhm
/X
GND
External pull-up EDS required
SPI0_IO2 : HR4 pull-up
External pull-up EDS required
+3VSUS
SR403
100KOhm
F_SPI_IO3
SR537
8.2KOhm
/X
GND
ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1: SLAVE ATTACHED FLASH SHARING PCH HAS INTERNAL WEAK PD
Internal pull-down
PCH_AL37_VSS
SR535
8.2KOhm
/X
GND
+3VSUS
SR180
8.2KOhm
/X
GPP_H_12
SR181
8.2KOhm
/X
GND
ASUSTek COMPUTER INC.
Title : CPTH (PCI/SPI)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 17 of 75





HSIO	Q370 Device ID: A306		H310 Device ID: A303		IRST for PCIE Storage			MIX-Q370D2 Assign	MIX-H310D2 Assign
0	USB3.1 Gen1/Gen2 #1		USB3.1 Gen1 #1					(port1) LAN+USB31 Gen2-10G#01	(port1) LAN+USB31 Gen1-5G#01
1	USB3.1 Gen1/Gen2 #2		USB3.1 Gen1 #2					(port2) LAN+USB31 Gen2-10G#01	(port2) LAN+USB31 Gen1-5G#01
2	USB3.1 Gen1/Gen2 #3		USB3.1 Gen1 #3					(port3) LAN+USB31 Gen2-10G#02	(port3) LAN+USB31 Gen1-5G#02
3	USB3.1 Gen1/Gen2 #4		USB3.1 Gen1 #4					(port4) LAN+USB31 Gen2-10G#02	(port4) LAN+USB31 Gen1-5G#02
4	USB3.1 Gen1/Gen2 #5		N/A					(port5) USB31 Gen2-10G#01	N/A
5	USB3.1 Gen1/Gen2 #6		N/A					(port6) USB31 Gen2-10G#01	N/A
6	USB3.1 Gen1 #7	PCIE #1	N/A		NO	x4	x2	N/A	N/A
7	USB3.1 Gen1 #8	PCIE #2	N/A					N/A	N/A
8	USB3.1 Gen1 #9	PCIE #3	N/A				x2	N/A	N/A
9	USB3.1 Gen1 #10	PCIE #4	N/A					N/A	N/A
10	PCIE #5	GbE	PCIE Gen2 #1	GbE	NO	x4	x2	LAN1_I219LM	LAN1_I219LM
11	PCIE #6		PCIE Gen2 #2					LAN2_I211	LAN2_I211 (PCIe Gen2)
12	PCIE #7		PCIE Gen2 #3				x2	M.2_Key-E	M.2_Key-E (PCIe Gen2)
13	PCIE #8		PCIE Gen2 #4					N/A	N/A
14	PCIE #9	GbE	GbE		Yes	x4	x2	M.2_Key-M SSD (PCIE*4 / SATA#4) (PCIE*4, Optane)	N/A
15	PCIE #10		N/A						N/A
16	PCIE #11	SATA #0a	PCIE Gen2 #5				x2		N/A
17	PCIE #12	SATA #1a	PCIE Gen2 #6	GbE					M.2_Key-M SSD (PCIE*1 Gen2)
18	PCIE #13	SATA #0b GbE	SATA #0	GbE	NO	x4	x2		SATA6G_0
19	PCIE #14	SATA #1b	SATA #1						N/A
20	PCIE #15	SATA #2	SATA #2				x2		SATA6G_2
21	PCIE #16	SATA #3	SATA #3						N/A
22	PCIE #17	SATA #4	N/A		Yes	x4	x2		N/A
23	PCIE #18	SATA #5	N/A						N/A
24	PCIE #19		N/A				x2		N/A
25	PCIE #20		N/A						N/A
26	PCIE #21		N/A		Yes	x4	x2		N/A
27	PCIE #22		N/A						N/A
28	PCIE #23		N/A				x2		N/A
29	PCIE #24		N/A						N/A

MIX-Q370D2 Port Assignment

Cannon Lake PCH Q370/H310 (MP)

USB Setting

USB 2.0	Function
USB2_01	LAN1+USB31 Gen2-10G#01
USB2_02	LAN1+USB31 Gen2-10G#02
USB2_03	LAN2+USB31 Gen2-10G#03
USB2_04	LAN2+USB31 Gen2-10G#04
USB2_05	USB2.0 Only_#5 Typc A
USB2_06	USB2.0 Only_#6 Typc A
USB2_07	USB2.0 Only_#7 Typc A
USB2_08	USB2.0 Only_#8 Typc A
USB2_09	USB2.0 Internal Header#9
USB2_10	USB2.0 Internal Header#10
USB2_11	USB31 Gen2-10G#11
USB2_12	USB31 Gen2-10G#12
USB2_13	N/A
USB2_14	M.2 E KEY

USB 3.1	Function
USB31_01	LAN1+USB31 Gen2-10G#01
USB31_02	LAN1+USB31 Gen2-10G#02
USB31_03	LAN2+USB31 Gen2-10G#03
USB31_04	LAN2+USB31 Gen2-10G#04
USB31_05	USB31 Gen2-10G#05
USB31_06	USB31 Gen2-10G#06
USB30_07	N/A
USB30_08	N/A
USB30_09	N/A
USB30_10	N/A

PCIE/SATA Function Define

	Function
PCIE-01 (USB3#7)	N/A
PCIE-02 (USB3#8)	N/A
PCIE-03 (USB3#9)	N/A
PCIE-04 (USB3#10)	N/A
PCIE-05	LAN1_I219LM
PCIE-06	LAN2_I211
PCIE-07	M.2_Key-E
PCIE-08	N/A
PCIE-09	M.2_Key-M SSD (PCIEx4/SATA#1) Support Optane
PCIE-10	
PCIE-11 (SATA-0a)	
PCIE-12 (SATA-1a)	

	Function
PCIE-13 (SATA-0b)	SATA6G_0
PCIE-14 (SATA-1b)	N/A
PCIE-15 (SATA-2)	SATA6G_2
PCIE-16 (SATA-3)	N/A
PCIE-17 (SATA-4)	N/A
PCIE-18 (SATA-5)	N/A
PCIE-19 (SATA-6)	N/A
PCIE-20 (SATA-7)	N/A
PCIE-21	N/A
PCIE-22	N/A
PCIE-23	N/A
PCIE-24	N/A

	Function
CLKREQ-0	M.2_BT_UART_WAKE#
CLKREQ-1	
CLKREQ-2	CLK_REQ2_LAN#
CLKREQ-3	
CLKREQ-4	
CLKREQ-5	
CLKREQ-6	
CLKREQ-7	
CLKREQ-8	CLK_REQ8_M.2_SSD#
CLKREQ-9	CLK_REQ9_M.2_WLAN#
CLKREQ-10~15	

ASUS

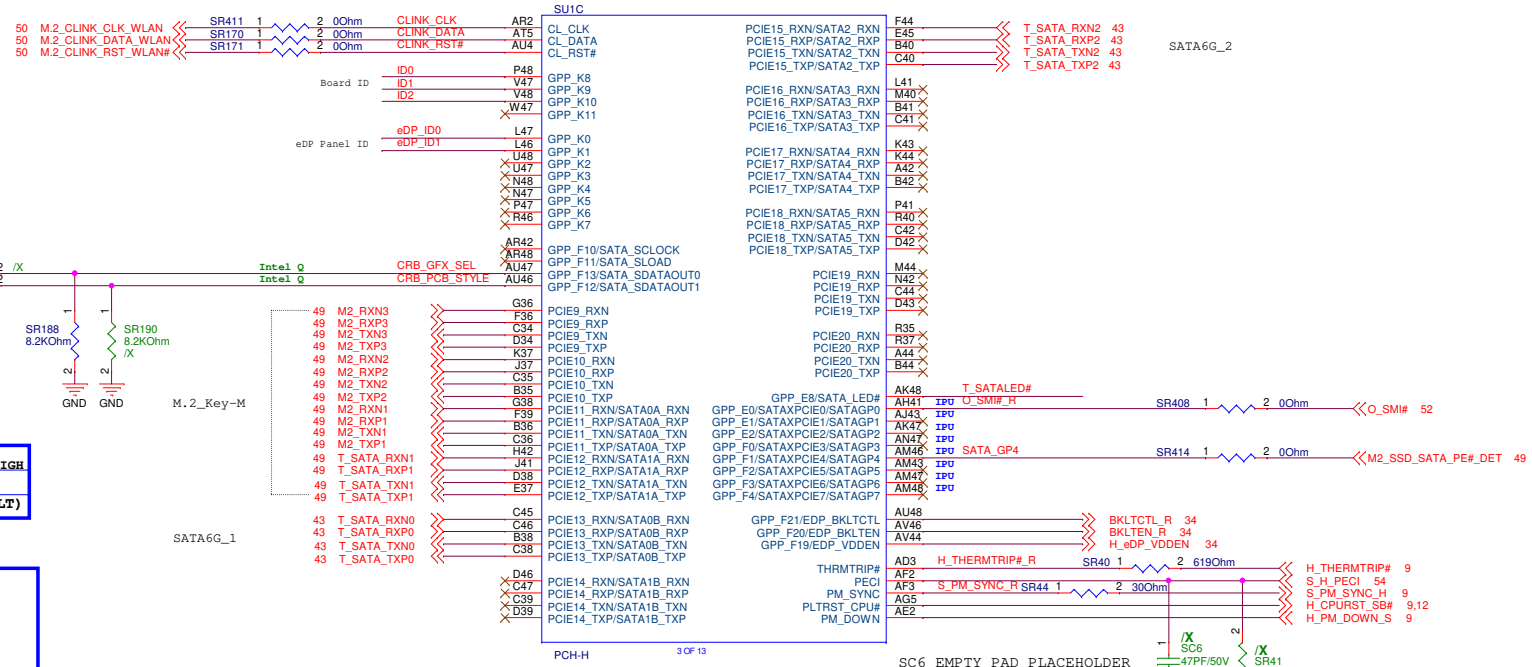
ASUSTek COMPUTER INC.

Title : CPTH (PCIE/DMI/USB)

Engineer: IPC-EE3

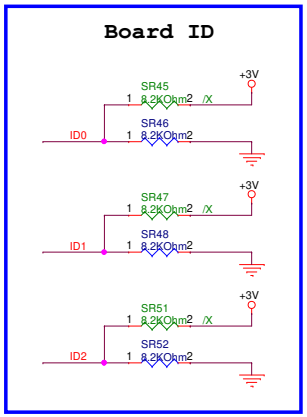
Size	Project Name	Rev
A3	MIX-Q370D2	R1.00

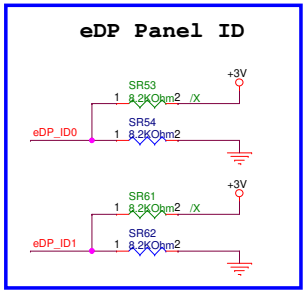
Date: Monday, October 14, 2019 Sheet 18 of 75



CRB_GFX_SEL	
CRB: LOW	
0	NORMAL GFX
1	CUSTOMER GFX

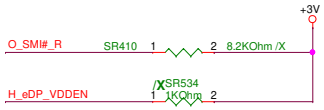
CRB_PCB_STYLE	
CRB: HIGH	
0	SV ADVANCE MENU
1	NORMAL MENU (DEFAULT)

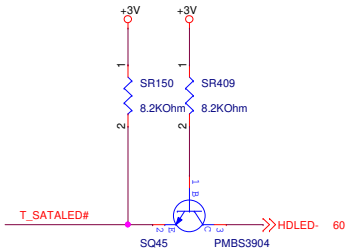




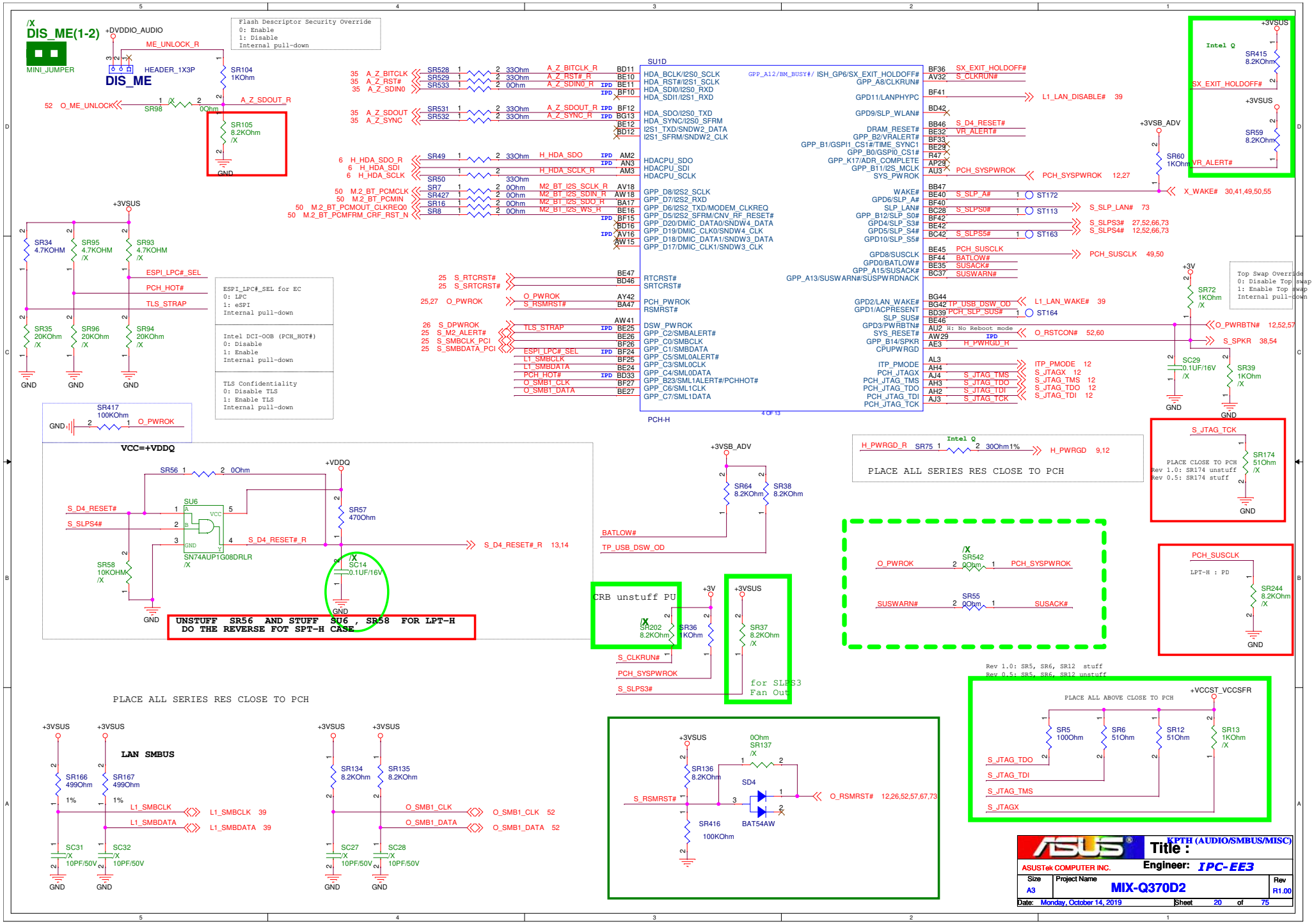
Note:

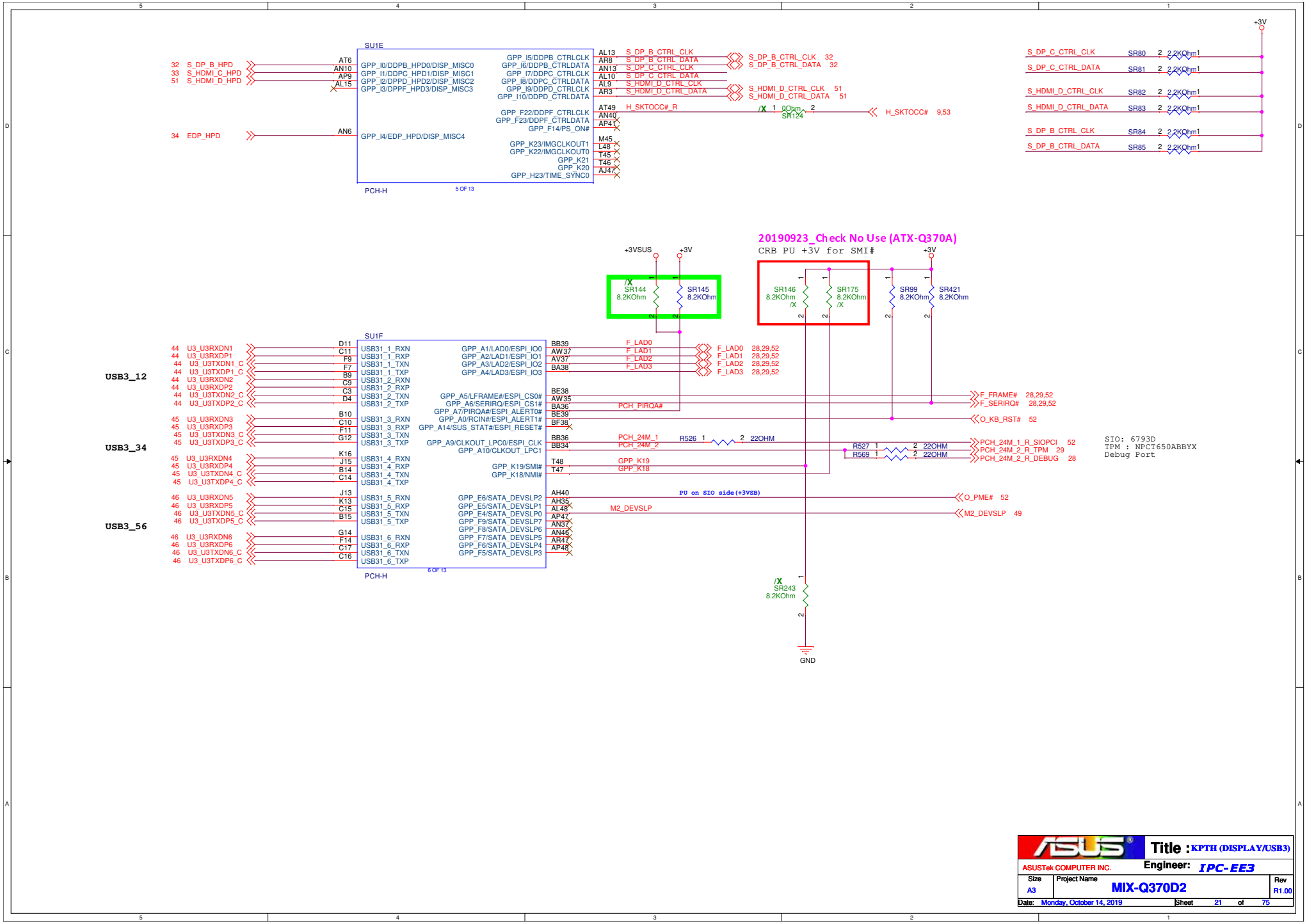
1. SATAGP[2:0]/SATAXPCIE[2:0]/GPP_E[2:0] and SATAGP[7:3]/SATAXPCIE[7:3]/GPP_F[4:0] has two native functions – the first native function (SATAXPCIEx) is selected if the Flex I/O soft strap SATA_PCIE_Select_for_Port_x = 11b. Setting SATA_PCIE_Select_for_Port_x = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe* Port x to be assigned based on the type of card installed and based on the SATAXPCIEx mux selector with the polarity for SATA or PCIe* (When SPSGPx = 0, PCIe* will be selected if the sampled value is "0" and SATA will be selected if the sampled value is "1"; When SPSGPx = 1, SATA will be selected if the sampled value is "0" and PCIe* will be selected if the sampled value is "1"). SATA/PCIe Select GPIO polarity for SATA Port x (SPSGPx) and Soft straps are handled through FITC and described in Skylake PCH SPI Flash Programming Guide (CDI doc #TBD).

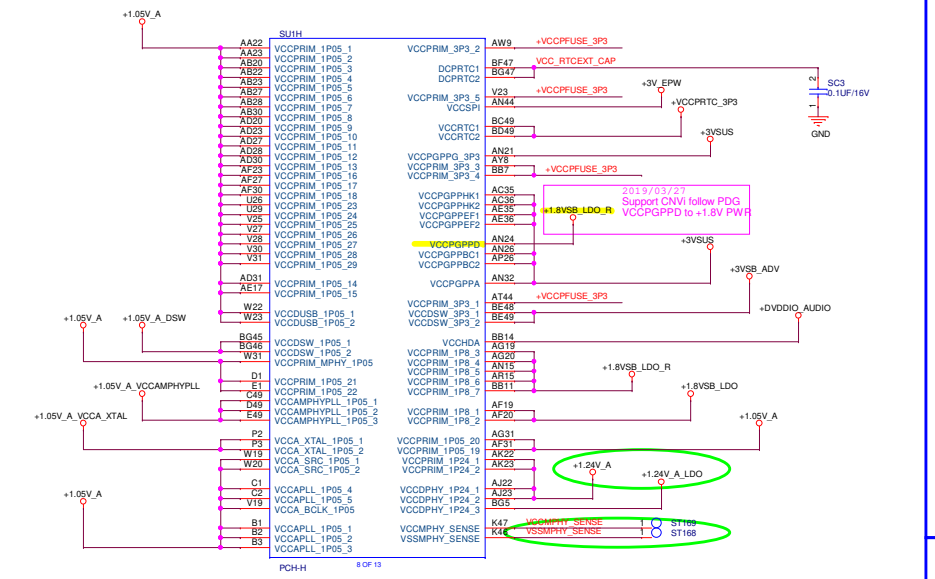




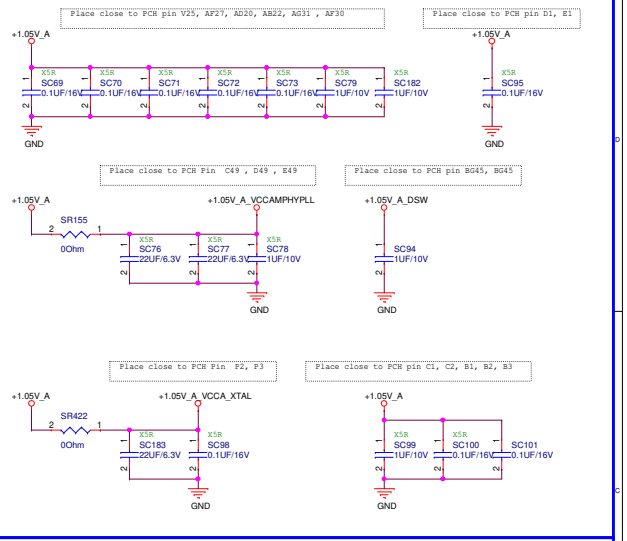
ASUS	Title : KPTH (HOST/FAN/SATA)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.00
Date: Monday, October 14, 2019	Sheet 19 of 75		


/X
DIS_ME(1-2)
MINI_JUMPER
+DVDDIO_AUDIO
ME_UNLOCK_R
HEADER_1X3P
DIS_ME
SR104 1KOhm
52 O_ME_UNLOCK
SR98 0Ohm
A_Z_SDOUT_R
SR105 8.2KOhm /X
GND
Flash Descriptor Security Override
0: Enable
1: Disable
Internal pull-down
SU1D
HDA_BCLK/I2S0_SCLK
HDA_RST#/I2S1_SCLK
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
GPP_D8/I2S2_SCLK
GPP_D7/I2S2_RXD
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
4 OF 13
PCH-H
GPP_A12/BM_BUSY#/ ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_K17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
L1_LAN_DISABLE# 39
PCH_SYSPWROK 12,27
X_WAKE# 30,41,49,50,55
S_SLP_LAN# 73
S_SLPS3# 27,52,66,73
S_SLPS4# 12,52,66,73
PCH_SUSCLK 49,50
L1_LAN_WAKE# 39
O_PWRBTN# 12,52,57
O_RSTCON# 52,60
S_SPKR 38,54
H_PWRGD 9,12
+3VSUS
Intel Q
SR415 8.2KOhm
SX_EXIT_HOLDOFF#
SR59 8.2KOhm
VR_ALERT#
+3VSB_ADV
SR60 1KOhm
+3V
SR72 1KOhm /X
Top Swap Override
0: Disable Top swap
1: Enable Top swap
Internal pull-down
SC29 0.1UF/16V /X
SR39 1KOhm /X
SR34 4.7KOHM
SR95 4.7KOHM /X
SR93 4.7KOHM /X
ESPI_LPC#_SEL
PCH_HOT#
TLS_STRAP
SR35 20KOhm /X
SR96 20KOhm /X
SR94 20KOhm /X
ESPI_LPC#_SEL for EC
0: LPC
1: eSPI
Internal pull-down
Intel DCI-OOB (PCH_HOT#)
0: Disable
1: Enable
Internal pull-down
TLS Confidentiality
0: Disable TLS
1: Enable TLS
Internal pull-down
SR417 100KOhm
O_PWROK
VCC=+VDDQ
SR56 0Ohm
+VDDQ
SR57 470Ohm
SU6
S_D4_RESET#
S_SLPS4#
S_D4_RESET#_R
SN74AUP1G08DRLR /X
SR58 10KOHM /X
SC14 0.1UF/16V
UNSTUFF SR56 AND STUFF SU6 , SR58 FOR LPT-H
DO THE REVERSE FOT SPT-H CASE
PLACE ALL SERIES RES CLOSE TO PCH
SR64 8.2KOhm
SR38 8.2KOhm
BATLOW#
TP_USB_DSW_OD
H_PWRGD_R SR75 30Ohm1%
PLACE ALL SERIES RES CLOSE TO PCH
S_JTAG_TCK
SR174 51Ohm /X
PLACE CLOSE TO PCH
Rev 1.0: SR174 unstuff
Rev 0.5: SR174 stuff
O_PWROK SR542 0Ohm PCH_SYSPWROK
SUSWARN# SR55 0Ohm SUSACK#
PCH_SUSCLK
LPT-H : PD
SR244 8.2KOhm /X
CRB unstuff PU
SR202 8.2KOhm
SR36 1KOhm
S_CLKRUN#
PCH_SYSPWROK
S_SLPS3#
SR37 8.2KOhm /X
for SLPS3 Fan Out
Rev 1.0: SR5, SR6, SR12 stuff
Rev 0.5: SR5, SR6, SR12 unstuff
PLACE ALL ABOVE CLOSE TO PCH
+VCCST_VCCSFR
SR5 100Ohm
SR6 51Ohm
SR12 51Ohm
SR13 1KOhm /X
S_JTAG_TDO
S_JTAG_TDI
S_JTAG_TMS
S_JTAGX
PLACE ALL SERIES RES CLOSE TO PCH
LAN SMBUS
SR166 499Ohm 1%
SR167 499Ohm 1%
L1_SMBCLK L1_SMBCLK 39
L1_SMBDATA L1_SMBDATA 39
SC31 /X 10PF/50V
SC32 /X 10PF/50V
SR134 8.2KOhm
SR135 8.2KOhm
O_SMB1_CLK O_SMB1_CLK 52
O_SMB1_DATA O_SMB1_DATA 52
SC27 /X 10PF/50V
SC28 /X 10PF/50V
SR136 8.2KOhm
0Ohm SR137 /X
SD4
S_RSMRST#
O_RSMRST# 12,26,52,57,67,73
SR416 100KOhm
BAT54AW
ASUS
ASUSTek COMPUTER INC.
Title : KPTH (AUDIO/SMBUS/MISC)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 20 of 75

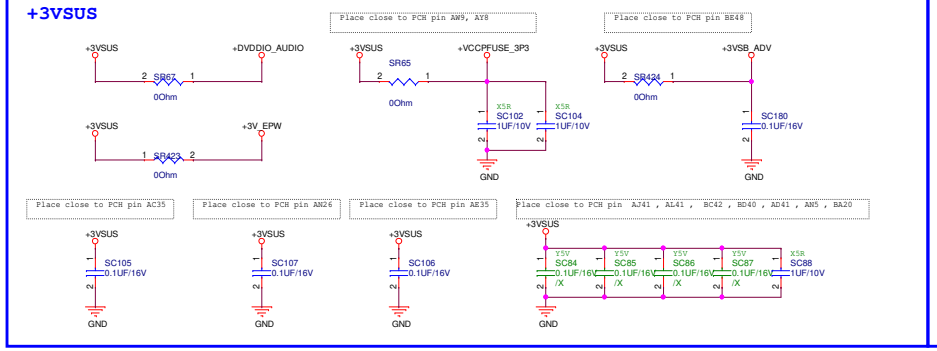

SU1E
PCH-H
5 OF 13
32 S_DP_B_HPD
33 S_HDMI_C_HPD
51 S_HDMI_D_HPD
34 EDP_HPD
AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
AP9 GPP_I2/DPPD_HPD2/DISP_MISC2
AL15 GPP_I3/DPPF_HPD3/DISP_MISC3
AN6 GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F22/DDPF_CTRLCLK
GPP_F23/DDPF_CTRLDATA
GPP_F14/PS_ON#
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0
AL13 S_DP_B_CTRL_CLK
AR8 S_DP_B_CTRL_DATA
AN13 S_DP_C_CTRL_CLK
AL10 S_DP_C_CTRL_DATA
AL9 S_HDMI_D_CTRL_CLK
AR3 S_HDMI_D_CTRL_DATA
AT49 H_SKTOCC#_R
AN40
AP41
M45
L48
T45
T46
AJ47
S_DP_B_CTRL_CLK 32
S_DP_B_CTRL_DATA 32
S_HDMI_D_CTRL_CLK 51
S_HDMI_D_CTRL_DATA 51
/X 1 0Ohm 2 SR124
H_SKTOCC# 9,53
+3V
S_DP_C_CTRL_CLK SR80 2 2.2KOhm1
S_DP_C_CTRL_DATA SR81 2 2.2KOhm1
S_HDMI_D_CTRL_CLK SR82 2 2.2KOhm1
S_HDMI_D_CTRL_DATA SR83 2 2.2KOhm1
S_DP_B_CTRL_CLK SR84 2 2.2KOhm1
S_DP_B_CTRL_DATA SR85 2 2.2KOhm1
20190923_Check No Use (ATX-Q370A)
CRB PU +3V for SMI#
+3VSUS
+3V
/X SR144 8.2KOhm
SR145 8.2KOhm
SR146 8.2KOhm /X
SR175 8.2KOhm /X
SR99 8.2KOhm
SR421 8.2KOhm
SU1F
PCH-H
6 OF 13
USB3_12
USB3_34
USB3_56
44 U3_U3RXDN1
44 U3_U3RXDP1
44 U3_U3TXDN1_C
44 U3_U3TXDP1_C
44 U3_U3RXDN2
44 U3_U3RXDP2
44 U3_U3TXDN2_C
44 U3_U3TXDP2_C
45 U3_U3RXDN3
45 U3_U3RXDP3
45 U3_U3TXDN3_C
45 U3_U3TXDP3_C
45 U3_U3RXDN4
45 U3_U3RXDP4
45 U3_U3TXDN4_C
45 U3_U3TXDP4_C
46 U3_U3RXDN5
46 U3_U3RXDP5
46 U3_U3TXDN5_C
46 U3_U3TXDP5_C
46 U3_U3RXDN6
46 U3_U3RXDP6
46 U3_U3TXDN6_C
46 U3_U3TXDP6_C
D11 USB31_1_RXN
C11 USB31_1_RXP
F9 USB31_1_TXN
F7 USB31_1_TXP
B9 USB31_2_RXN
C9 USB31_2_RXP
C3 USB31_2_TXN
D4 USB31_2_TXP
B10 USB31_3_RXN
C10 USB31_3_RXP
F11 USB31_3_TXN
G12 USB31_3_TXP
K16 USB31_4_RXN
J15 USB31_4_RXP
B14 USB31_4_TXN
C14 USB31_4_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP
C15 USB31_5_TXN
B15 USB31_5_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP
C17 USB31_6_TXN
C16 USB31_6_TXP
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
BB39 F_LAD0
AW37 F_LAD1
AV37 F_LAD2
BA38 F_LAD3
BE38
AW35
BA36 PCH_PIRQA#
BE39
BF38
BB36 PCH_24M_1
BB34 PCH_24M_2
T48 GPP_K19
T47 GPP_K18
AH40
AH35
AL48 M2_DEVSLP
AP47
AN37
AN46
AR47
AP48
F_LAD0 28,29,52
F_LAD1 28,29,52
F_LAD2 28,29,52
F_LAD3 28,29,52
F_FRAME# 28,29,52
F_SERIRQ# 28,29,52
O_KB_RST# 52
R526 1 2 22OHM
R527 1 2 22OHM
R569 1 2 22OHM
PCH_24M_1_R_SIOPCI 52
PCH_24M_2_R_TPM 29
PCH_24M_2_R_DEBUG 28
PU on SIO side(+3VSB)
O_PME# 52
M2_DEVSLP 49
SIO: 6793D
TPM : NPCT650ABBYX
Debug Port
/X SR243 8.2KOhm
GND
ASUSTek COMPUTER INC.
Title : KPTH (DISPLAY/USB3)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 21 of 75



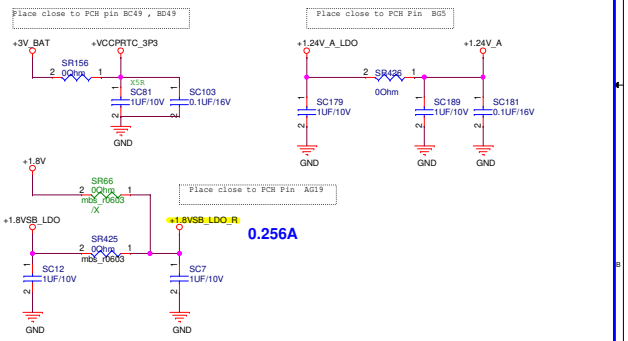
+1.05V_A



+3VSUS



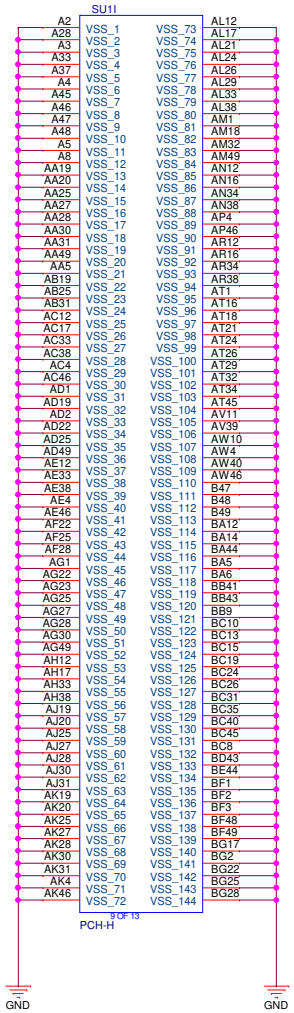
Other Power

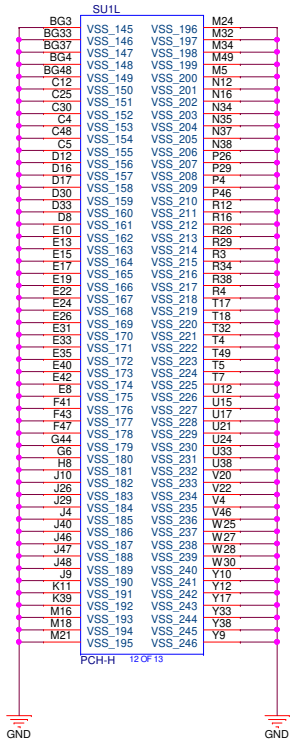


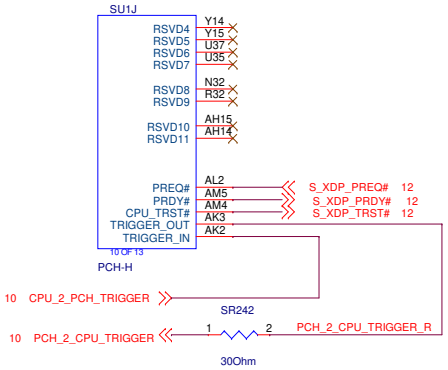
GPIO Voltage Level

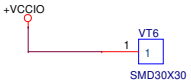
Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+3VSUS
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_D	VCCPGPPD	1.8V or 3.3V	+1.8VSUS
GPP_E	VCCPGPPEF	1.8V or 3.3V	+3VSUS
GPP_F	VCCPGPPEF	1.8V or 3.3V	+3VSUS
GPP_G	VCCPGPPG_3P3 VCCPRIM_1P8	Dynamic voltage to be config SDIO	+3VSUS +1.8VSUS
GPP_H	VCCPGPPHK	1.8V or 3.3V	+3VSUS
GPP_I	VCCPRIM_3P3	3.3V Only	+3VSUS
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8VSUS
GPP_K	VCCPGPPHK	1.8V or 3.3V	+3VSUS
GPD	VCCDSW_3P3	3.3V Only	+3VA_DSW

ASUS	Title : KPTH (POWER)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.00
Date: Monday, October 14, 2019	Sheet 22 of 75		

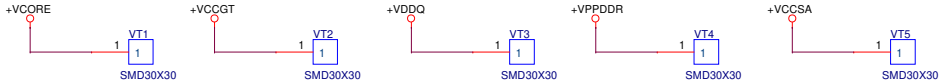




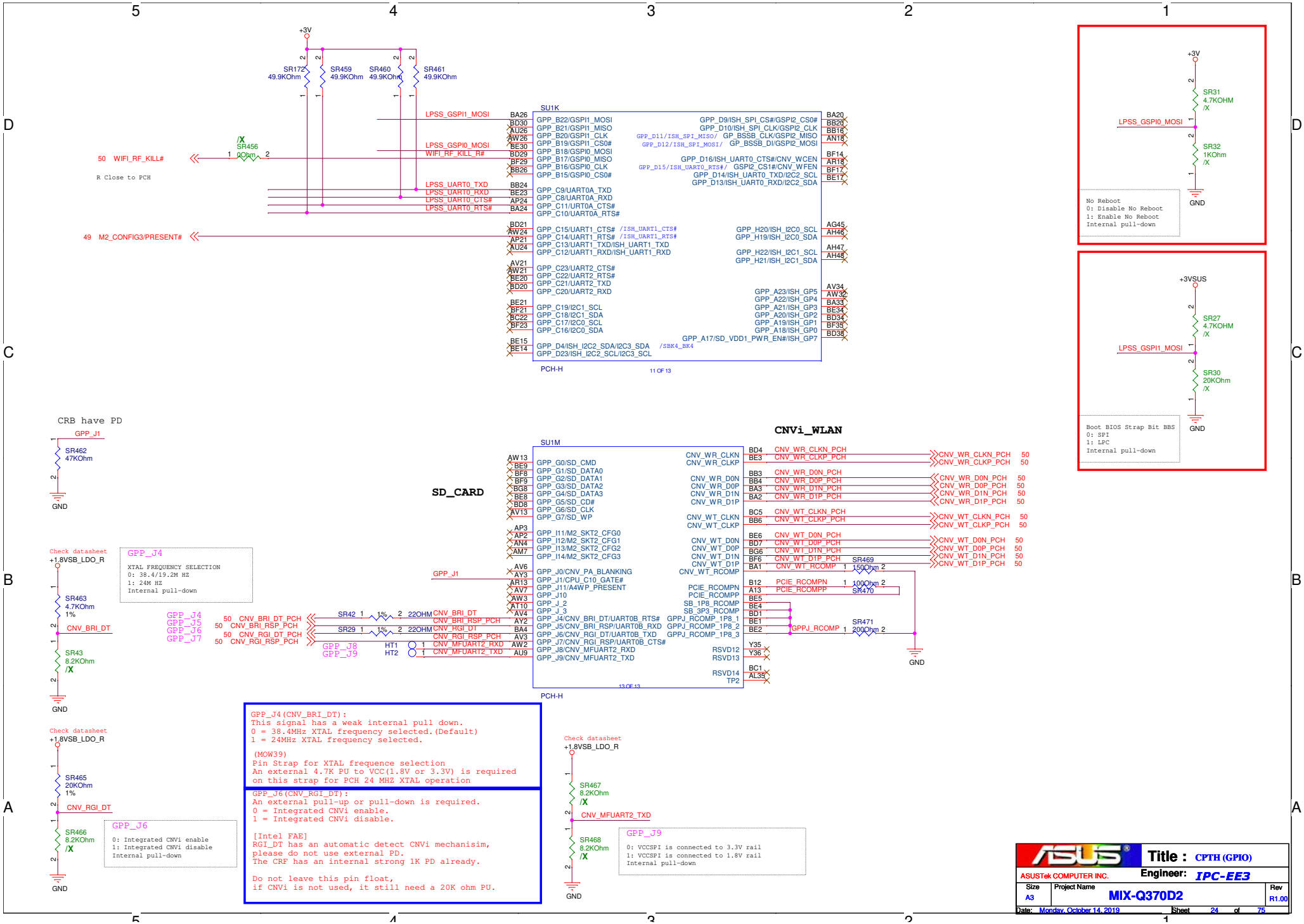


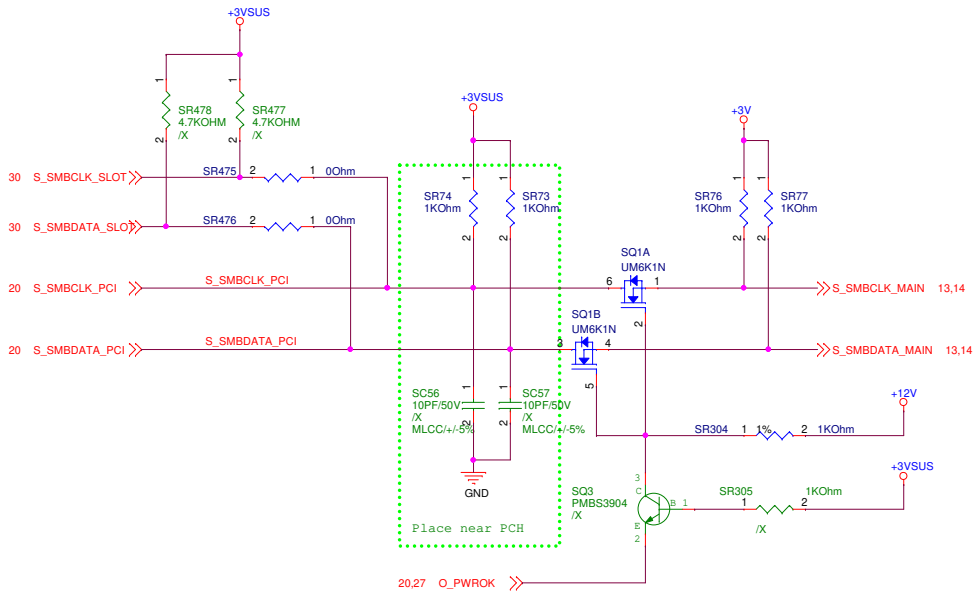


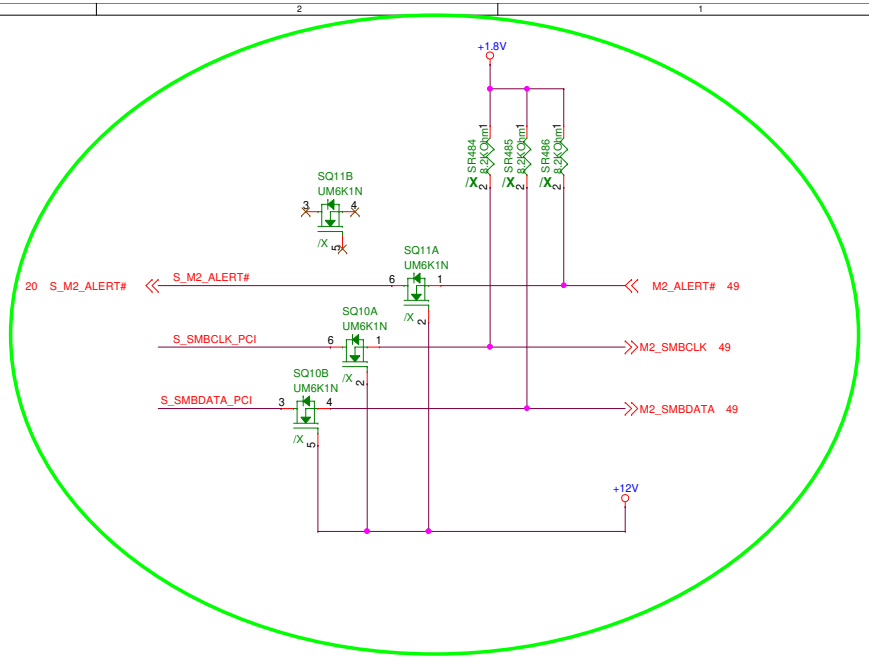
Easy point to measure voltage from top.



ASUS	Title : CPTH (GND)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 23 of 75		


SU1K
PCH-H
11 OF 13
SR172 49.9KOhm
SR459 49.9KOhm
SR460 49.9KOhm
SR461 49.9KOhm
SR456 0Ohm
50 WIFI_RF_KILL#
R Close to PCH
49 M2_CONFIG3/PRESENT#
LPSS_GSPI1_MOSI
LPSS_GSPI0_MOSI
WIFI_RF_KILL_R#
LPSS_UART0_TXD
LPSS_UART0_RXD
LPSS_UART0_CTS#
LPSS_UART0_RTS#
SR31 4.7KOHM /X
SR32 1KOhm /X
No Reboot
0: Disable No Reboot
1: Enable No Reboot
Internal pull-down
SR27 4.7KOHM /X
SR30 20KOhm /X
Boot BIOS Strap Bit BBS
0: SPI
1: LPC
Internal pull-down
CRB have PD
SR462 47KOhm
SR463 4.7KOhm 1%
SR43 8.2KOhm /X
GPP_J4
XTAL FREQUENCY SELECTION
0: 38.4/19.2M HZ
1: 24M HZ
Internal pull-down
SD_CARD
CNVi_WLAN
SU1M
PCH-H
13 OF 13
SR42 22OHM
SR29 22OHM
SR469 150Ohm
SR470
SR471 200Ohm
GPP_J8
GPP_J9
GPP_J6
0: Integrated CNVi enable
1: Integrated CNVi disable
Internal pull-down
SR465 20KOhm 1%
SR466 8.2KOhm /X
SR467 8.2KOhm /X
SR468 8.2KOhm /X
GPP_J9
0: VCCSPI is connected to 3.3V rail
1: VCCSPI is connected to 1.8V rail
Internal pull-down
GPP_J4(CNV_BRI_DT):
This signal has a weak internal pull down.
0 = 38.4MHz XTAL frequency selected.(Default)
1 = 24MHz XTAL frequency selected.
(MOW39)
Pin Strap for XTAL frequence selection
An external 4.7K PU to VCC(1.8V or 3.3V) is required
on this strap for PCH 24 MHZ XTAL operation
GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
[Intel FAE]
RGI_DT has an automatic detect CNVi mechanisim,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.
Title : CPTH (GPIO)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 24 of 75

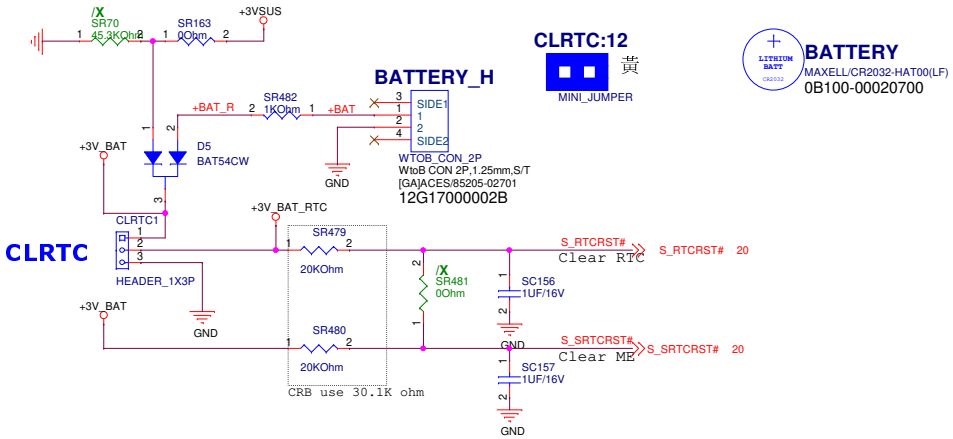


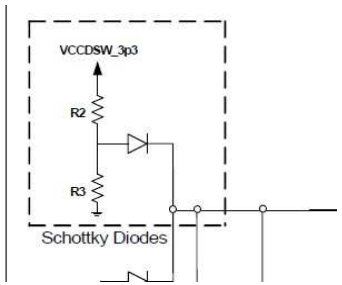


VCCRTC External Circuit

On SKL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

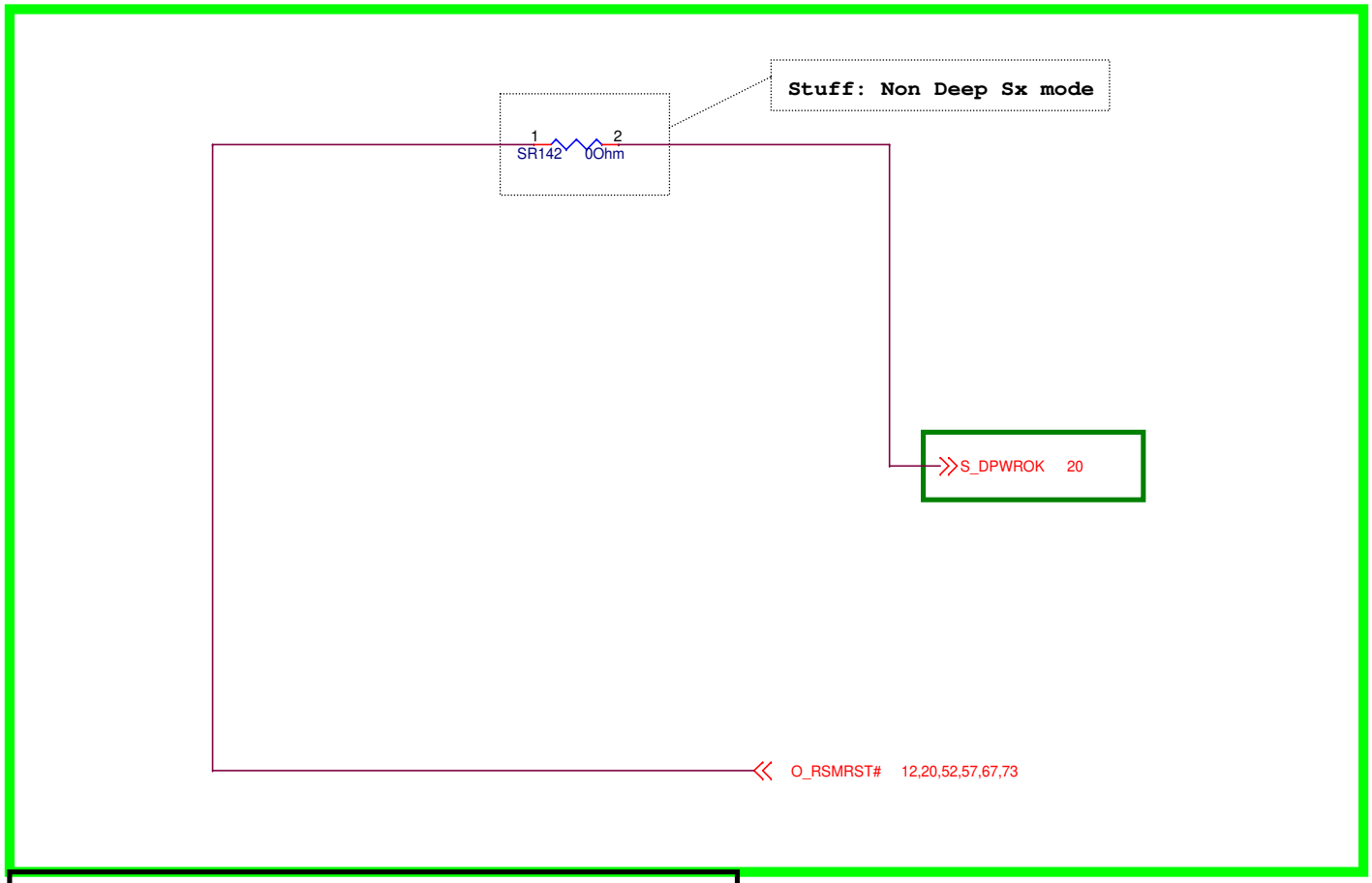
CRB use resistor divider newrok [SR163=0 , SR70=/X]

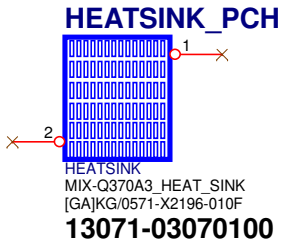




ASUS	Title : CPTH (SMBUS/CLRTC)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 25 of 75		

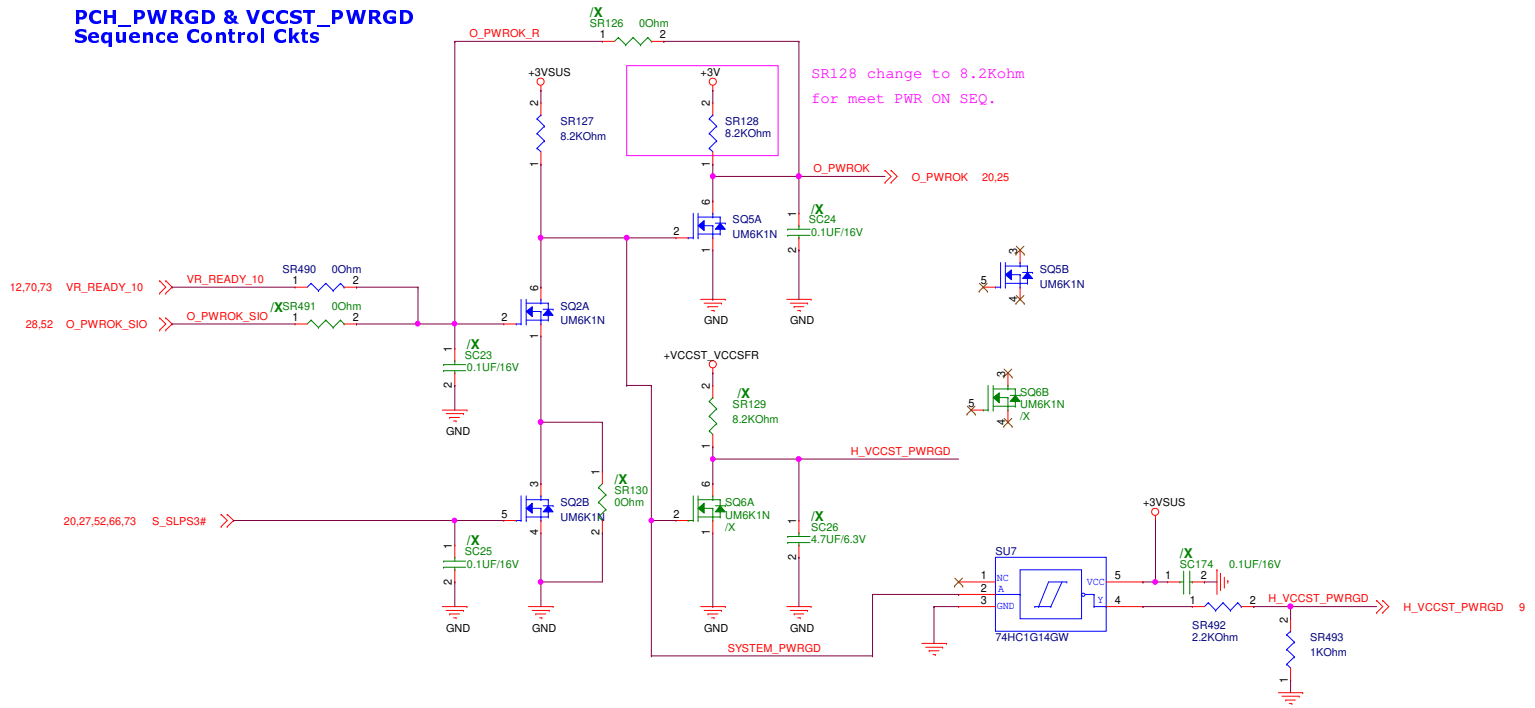
2015/04/15



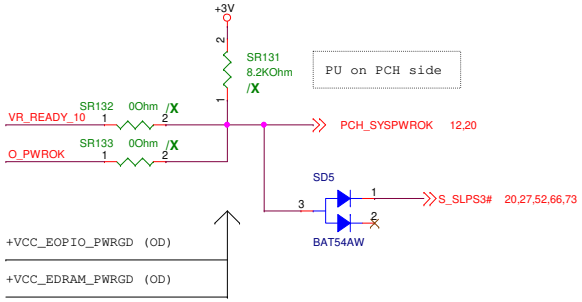


ASUS	Title : CPTH (DSW SEQUENCE)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A4	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 26 of 75		

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

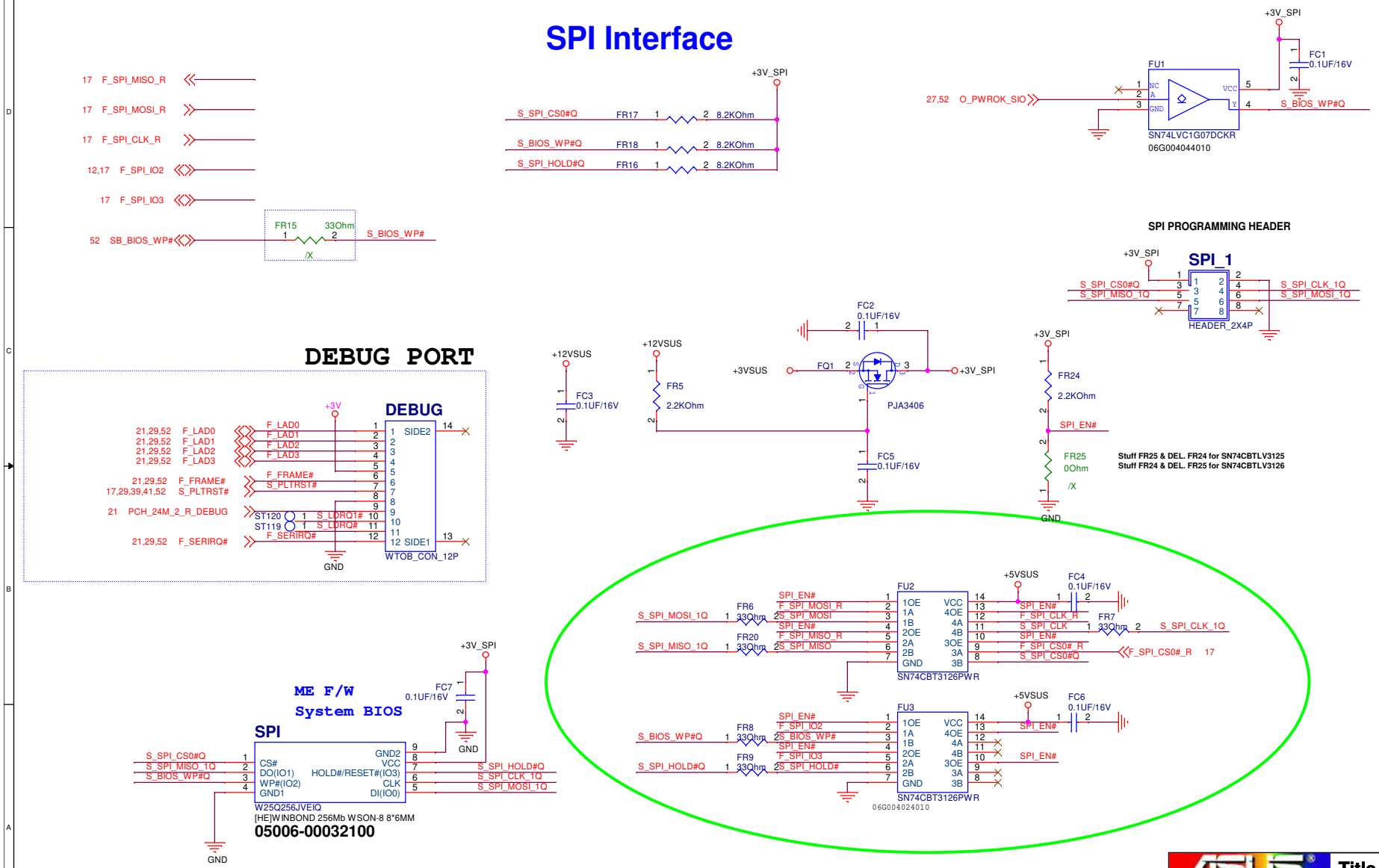
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

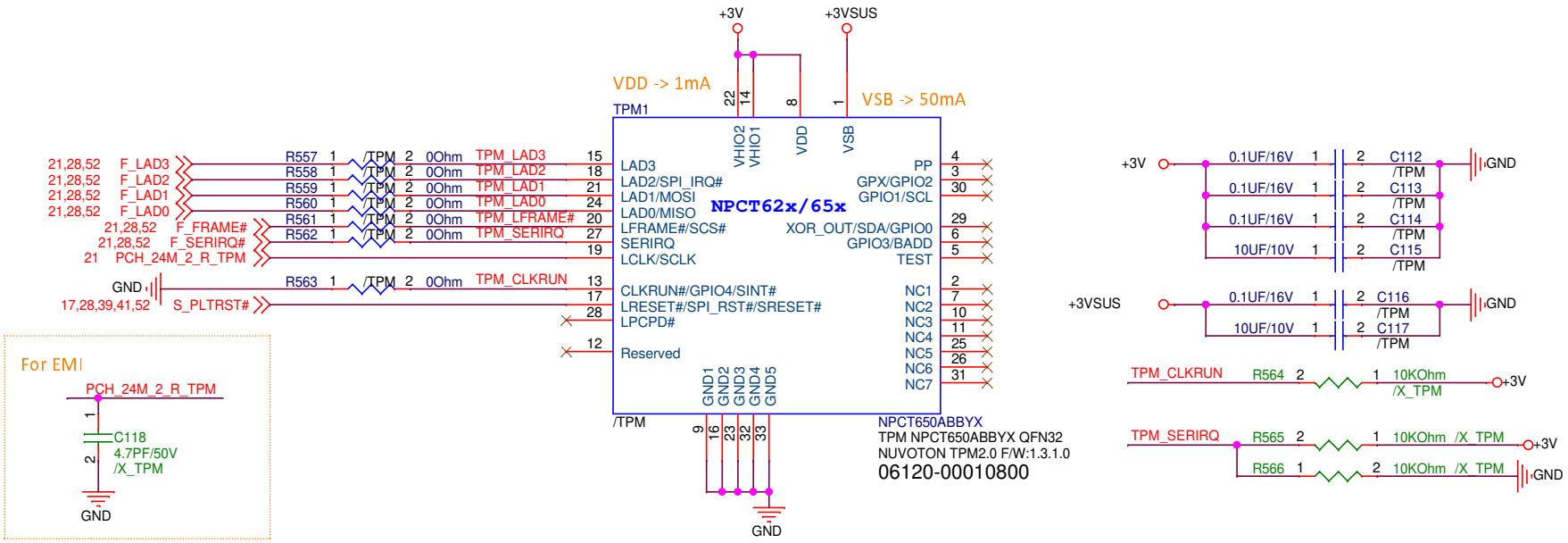
ASUSTek COMPUTER INC.	Title : CPTH (PCH/SYS/PROC_PWROK)	
	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 27 of 75	

SPI Interface

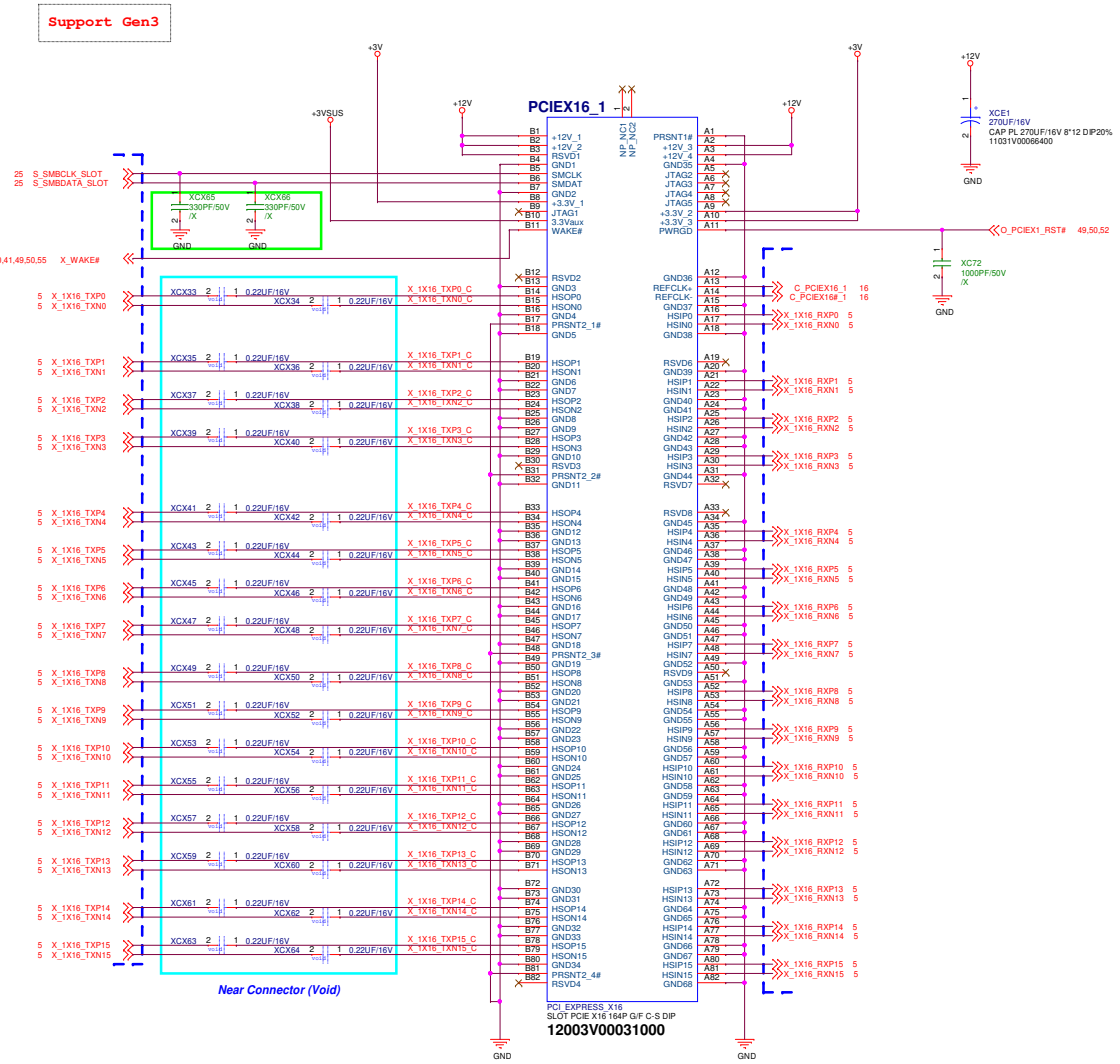


ASUSTek COMPUTER INC.	Title : BIOS/DEBUG
	Engineer: IPC-EE3
Size B	Project Name MIX-Q370D2
Rev R1.00	
Date: Monday, October 14, 2019	Sheet 28 of 75

TPM

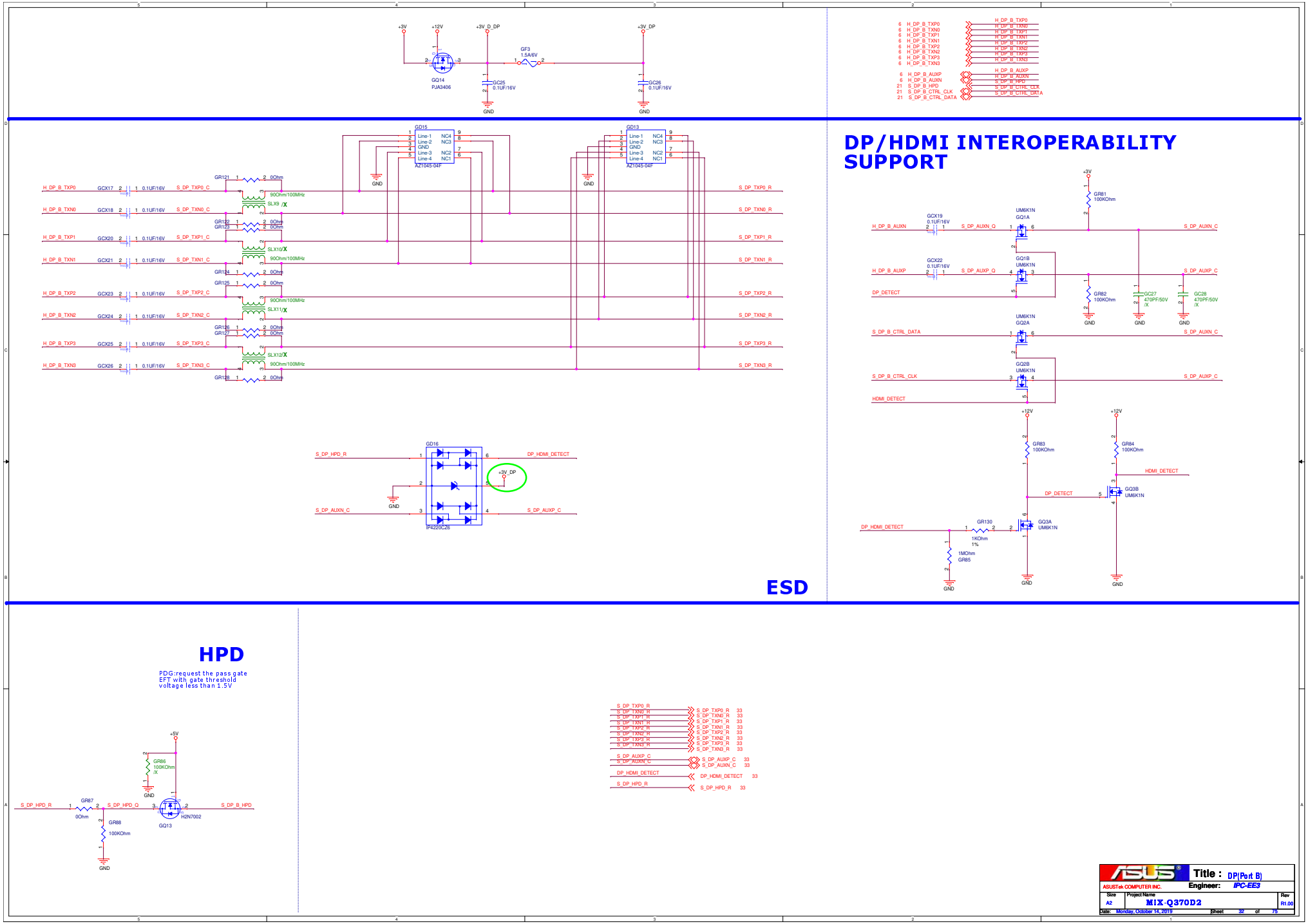


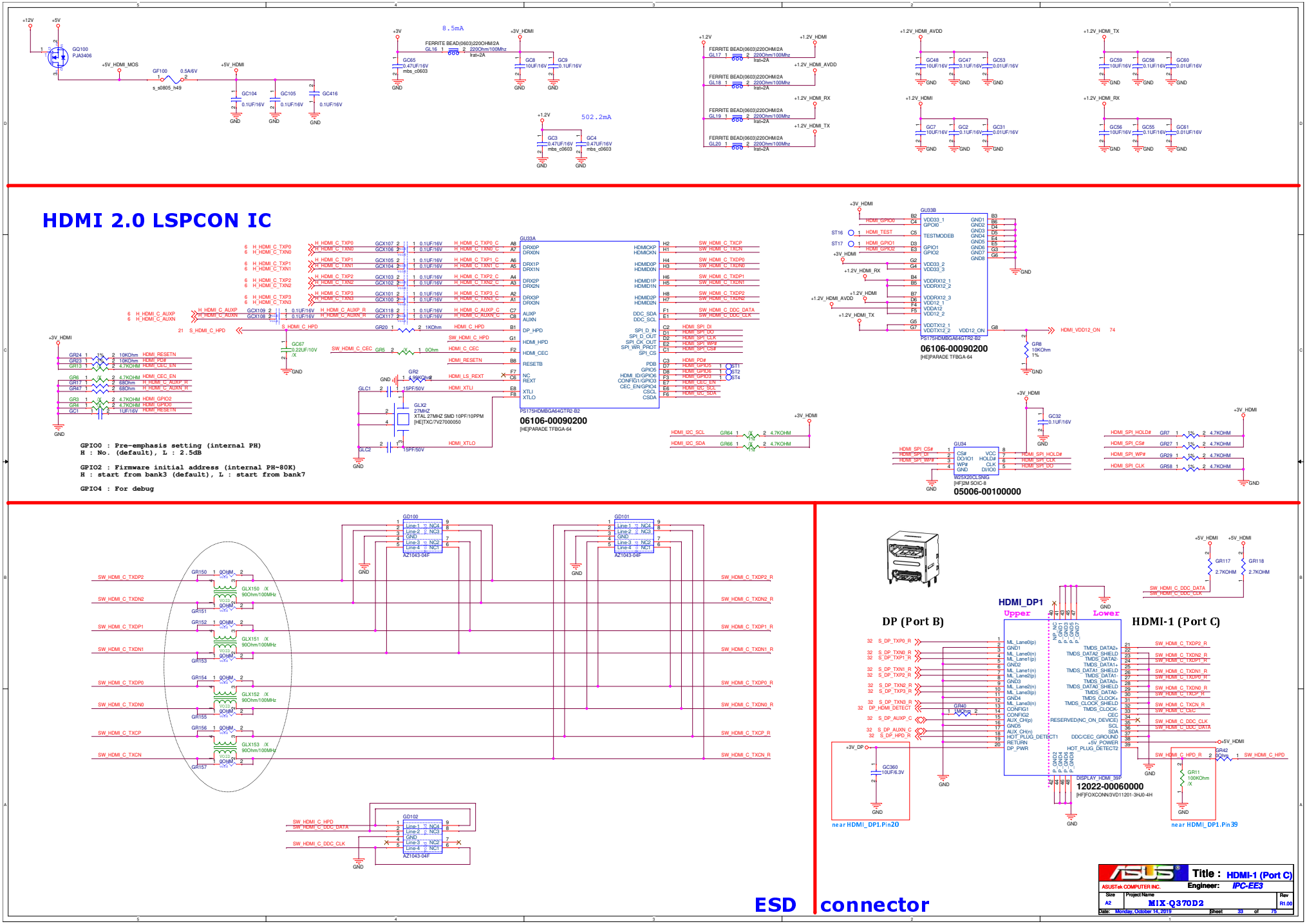
ASUSTek COMPUTER INC.	Title : TPM_NPCT650ABBYX	
	Engineer: IPC-EE3	
Size A4	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 29 of 75	



ASUSTeK COMPUTER INC.	Title : PCIEX16_1		
	Engineer: IPC-EE3		
Size C	Project Name MIX-Q370D2		Rev 1.00
Date: Monday, October 14, 2019	Sheet 30 of 75		

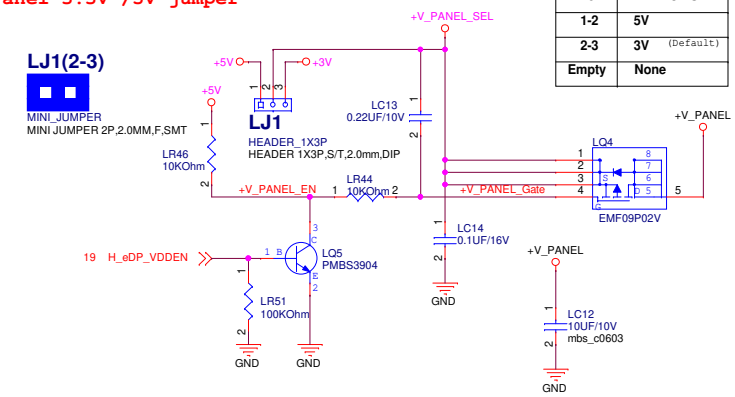
ASUSTek COMPUTER INC.	Title : CH7511 LVDS	
	Engineer: IPC-EE3	
Size: C	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 31 of 75	


+3V
+12V
+3V_D_DP
+3V_DP
GQ14
PJA3406
GF3
1.5A6V
GC25
0.1UF/16V
GC26
0.1UF/16V
GND
H_DP_B_TXP0
H_DP_B_TXN0
H_DP_B_TXP1
H_DP_B_TXN1
H_DP_B_TXP2
H_DP_B_TXN2
H_DP_B_TXP3
H_DP_B_TXN3
H_DP_B_AUXP
H_DP_B_AUXN
S_DP_B_HPD
S_DP_B_CTRL_CLK
S_DP_B_CTRL_DATA
GD15
AZ1045-04F
GD13
AZ1045-04F
Line-1
Line-2
Line-3
Line-4
NC1
NC2
NC3
NC4
H_DP_B_TXP0
H_DP_B_TXN0
H_DP_B_TXP1
H_DP_B_TXN1
H_DP_B_TXP2
H_DP_B_TXN2
H_DP_B_TXP3
H_DP_B_TXN3
GCX17
GCX18
GCX20
GCX21
GCX23
GCX24
GCX25
GCX26
0.1UF/16V
S_DP_TXP0_C
S_DP_TXN0_C
S_DP_TXP1_C
S_DP_TXN1_C
S_DP_TXP2_C
S_DP_TXN2_C
S_DP_TXP3_C
S_DP_TXN3_C
GR121
GR122
GR123
GR124
GR125
GR126
GR127
GR128
0Ohm
90Ohm/100MHz
SLX9
SLX10
SLX11
SLX12
S_DP_TXP0_R
S_DP_TXN0_R
S_DP_TXP1_R
S_DP_TXN1_R
S_DP_TXP2_R
S_DP_TXN2_R
S_DP_TXP3_R
S_DP_TXN3_R
GD16
IP4220CZ6
S_DP_HPD_R
S_DP_AUXN_C
DP_HDMI_DETECT
S_DP_AUXP_C
+3V_DP
ESD
DP/HDMI INTEROPERABILITY SUPPORT
GR81
100KOhm
GCX19
0.1UF/16V
GCX22
0.1UF/16V
S_DP_AUXN_Q
S_DP_AUXP_Q
UM6K1N
GQ1A
GQ1B
GQ2A
GQ2B
GQ3A
GQ3B
GR82
100KOhm
GC27
470PF/50V
GC28
470PF/50V
DP_DETECT
S_DP_B_CTRL_DATA
S_DP_B_CTRL_CLK
HDMI_DETECT
GR83
100KOhm
GR84
100KOhm
GR130
1KOhm
1%
1MOhm
GR85
HPD
PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V
GR86
100KOhm
GR87
0Ohm
GR88
100KOhm
S_DP_HPD_Q
S_DP_B_HPD
GQ13
H2N7002
S_DP_TXP0_R 33
S_DP_TXN0_R 33
S_DP_TXP1_R 33
S_DP_TXN1_R 33
S_DP_TXP2_R 33
S_DP_TXN2_R 33
S_DP_TXP3_R 33
S_DP_TXN3_R 33
S_DP_AUXP_C 33
S_DP_AUXN_C 33
DP_HDMI_DETECT 33
S_DP_HPD_R 33
ASUSTek COMPUTER INC.
Engineer: PC-EE3
Title : DP(Port B)
Size A2
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 32 of 75

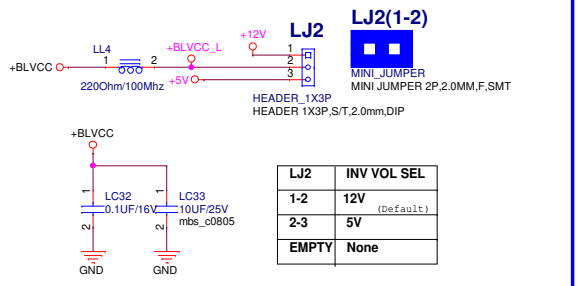

HDMI 2.0 LSPCON IC
GPIO0 : Pre-emphasis setting (internal PH)
H : No. (default), L : 2.5dB
GPIO2 : Firmware initial address (internal PH~80K)
H : start from bank3 (default), L : start from bank7
GPIO4 : For debug
06106-00090200
05006-00100000
12022-00060000
DP (Port B)
HDMI-1 (Port C)
HDMI_DP1
Upper
Lower
ESD connector
Title : HDMI-1 (Port C)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size A2
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 33 of 75

Panel 3.3V /5V jumper

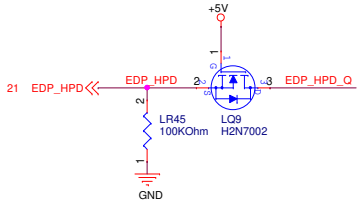
LJ1	PAN VOL SEL
1-2	5V
2-3	3V (Default)
Empty	None

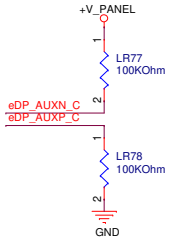


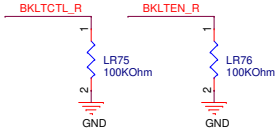
Panel backlight 12V /5V jumper

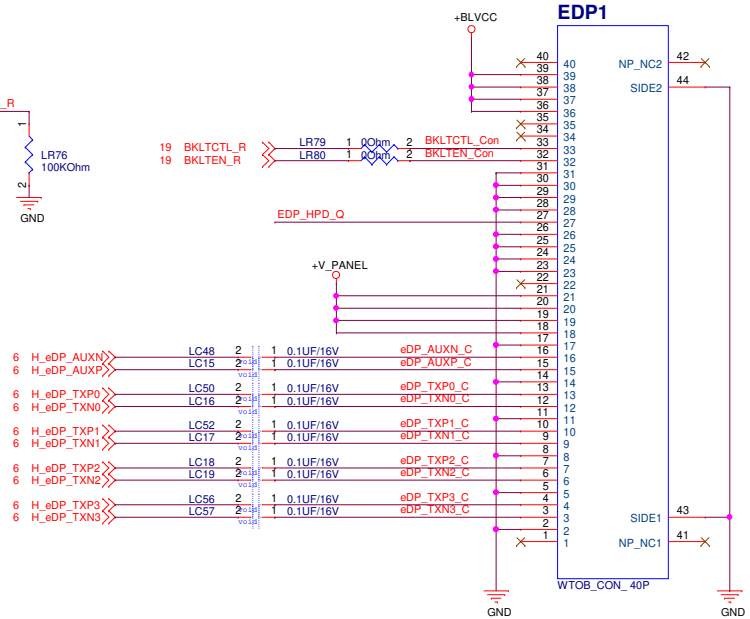


LJ2	INV VOL SEL
1-2	12V (Default)
2-3	5V
EMPTY	None

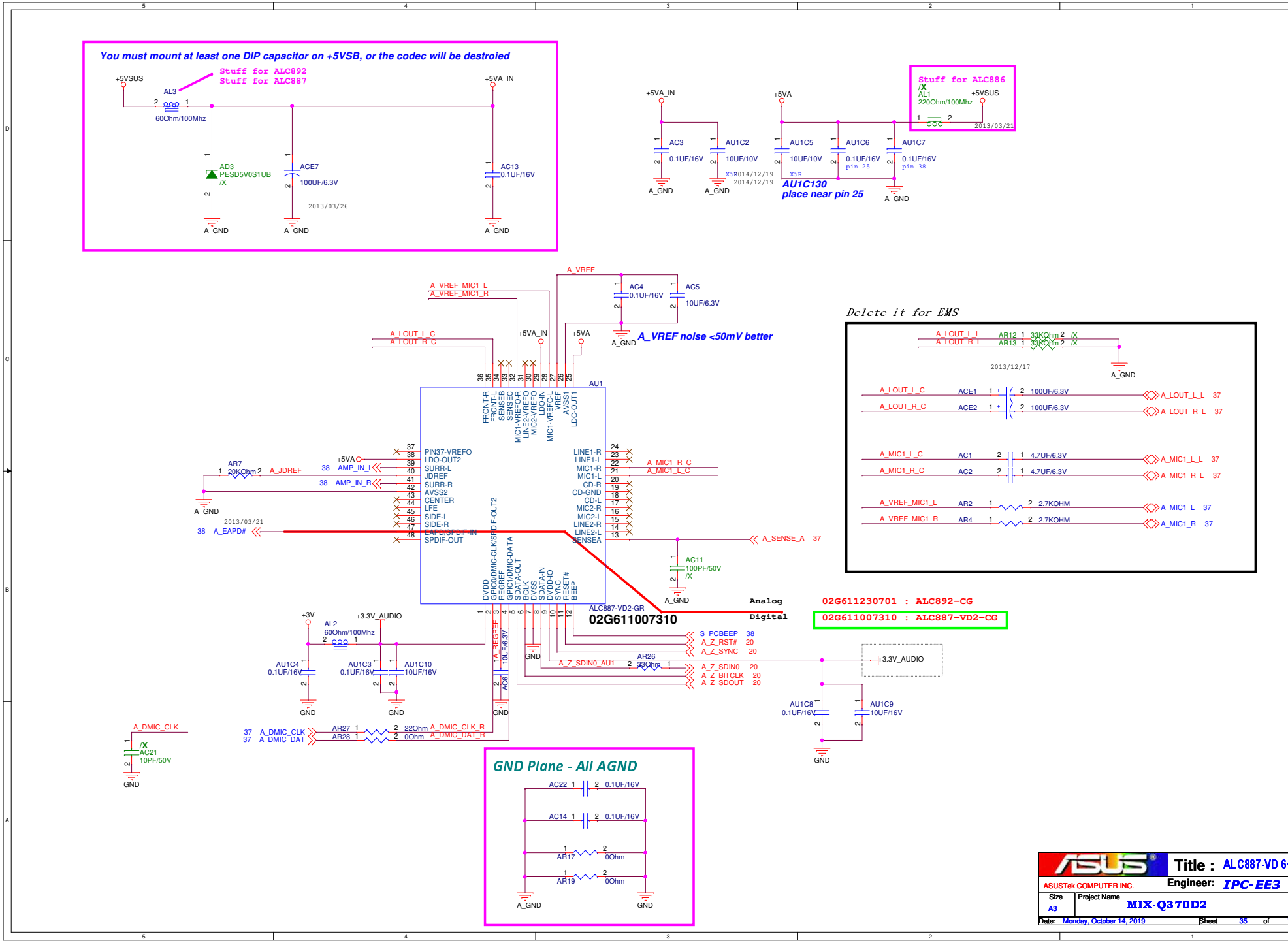






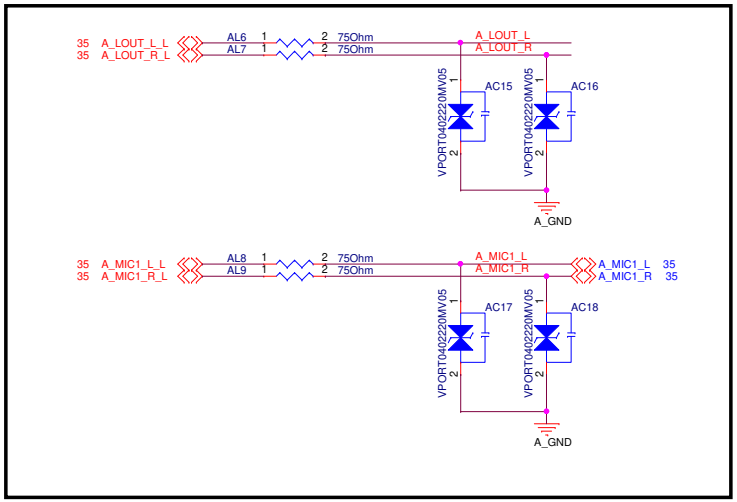


ASUSTek COMPUTER INC.	Title : eDP	
	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 34 of 75	

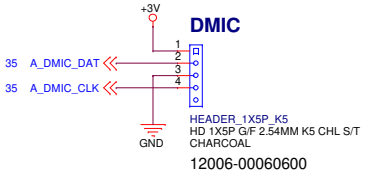

You must mount at least one DIP capacitor on +5VSB, or the codec will be destroied
Stuff for ALC892
Stuff for ALC887
+5VSUS
AL3
60Ohm/100Mhz
AD3
PESD5V0S1UB
/X
ACE7
100UF/6.3V
2013/03/26
+5VA_IN
AC13
0.1UF/16V
A_GND
Stuff for ALC886
/X
AL1
220Ohm/100Mhz
+5VSUS
2013/03/21
+5VA_IN
AC3
0.1UF/16V
AU1C2
10UF/10V
X5R
2014/12/19
+5VA
AU1C5
10UF/10V
AU1C6
0.1UF/16V
pin 25
AU1C7
0.1UF/16V
pin 38
AU1C130
place near pin 25
A_VREF
AC4
0.1UF/16V
AC5
10UF/6.3V
A_VREF noise <50mV better
A_VREF_MIC1_L
A_VREF_MIC1_R
A_LOUT_L_C
A_LOUT_R_C
AU1
ALC887-VD2-GR
02G611007310
PIN37-VREFO
LDO-OUT2
SURR-L
JDREF
SURR-R
AVSS2
CENTER
LFE
SIDE-L
SIDE-R
EAPD/SPDIF-IN
SPDIF-OUT
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
SENSEA
AR7
20KOhm
A_JDREF
AMP_IN_L
AMP_IN_R
A_EAPD#
2013/03/21
A_MIC1_R_C
A_MIC1_L_C
A_SENSE_A
AC11
100PF/50V
/X
Analog
Digital
02G611230701 : ALC892-CG
02G611007310 : ALC887-VD2-CG
+3V
AL2
60Ohm/100Mhz
+3.3V_AUDIO
AU1C4
0.1UF/16V
AU1C3
0.1UF/16V
AU1C10
10UF/16V
AC6
10UF/6.3V
S_PCBEEP
A_Z_RST#
A_Z_SYNC
A_Z_SDIN0_AU1
AR26
33Ohm
A_Z_SDIN0
A_Z_BITCLK
A_Z_SDOUT
AU1C8
0.1UF/16V
AU1C9
10UF/16V
A_DMIC_CLK
/X
AC21
10PF/50V
A_DMIC_CLK
A_DMIC_DAT
AR27
22Ohm
AR28
0Ohm
A_DMIC_CLK_R
A_DMIC_DAT_R
GND
Delete it for EMS
A_LOUT_L_L
A_LOUT_R_L
AR12
AR13
33KOhm
2013/12/17
ACE1
ACE2
100UF/6.3V
AC1
AC2
4.7UF/6.3V
AR2
AR4
2.7KOHM
A_MIC1_L_L
A_MIC1_R_L
A_MIC1_L
A_MIC1_R
GND Plane - All AGND
AC22
AC14
0.1UF/16V
AR17
AR19
0Ohm
ASUS
Title : ALC887-VD 6+2CH
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 35 of 75

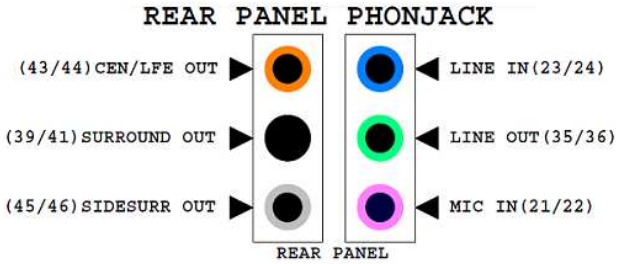
ASUSTek COMPUTER INC.	Title : ALC887-VD 6+2CH	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 36 of 75	

Delete it for EMS



Digital Microphone





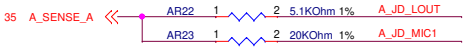
ALC889/ALC892/ALC898 Configuation (7.1 Channel)

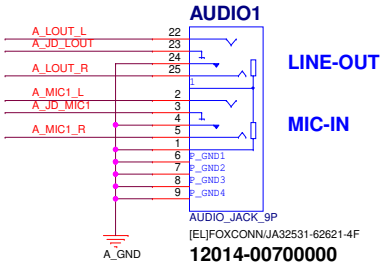
Rear Panel: 6 dedicated audio jacks
Front Panel: 2 re-tasking audio jacks

Pin Assignment	Location	Function
FRONT(pin-35,36)/Port-D	Rear Panel	Front-Out, HP-Out
SURR (pin-39,41)/Port-A	Rear Panel	Surr-Out
CEN/LFE (pin-43,44)/Port-G	Rear Panel	Cen/Lfe-Out
SIDE (pin-45,46)/Port-H	Rear Panel	Side-Surr Out
LINE1 (pin-23,24)/Port-C	Rear Panel	Line-In
MIC1 (pin-21,22)/Port-B	Rear Panel	Mic-In
LINE2 (pin-14,15)/Port-E	Front Panel	HP-Out, Line-In, Mic-In
MIC2 (pin-16,17)/Port-F	Front Panel	Mic-In, HP-Out, Line-In

SPDIF Optical

A-11

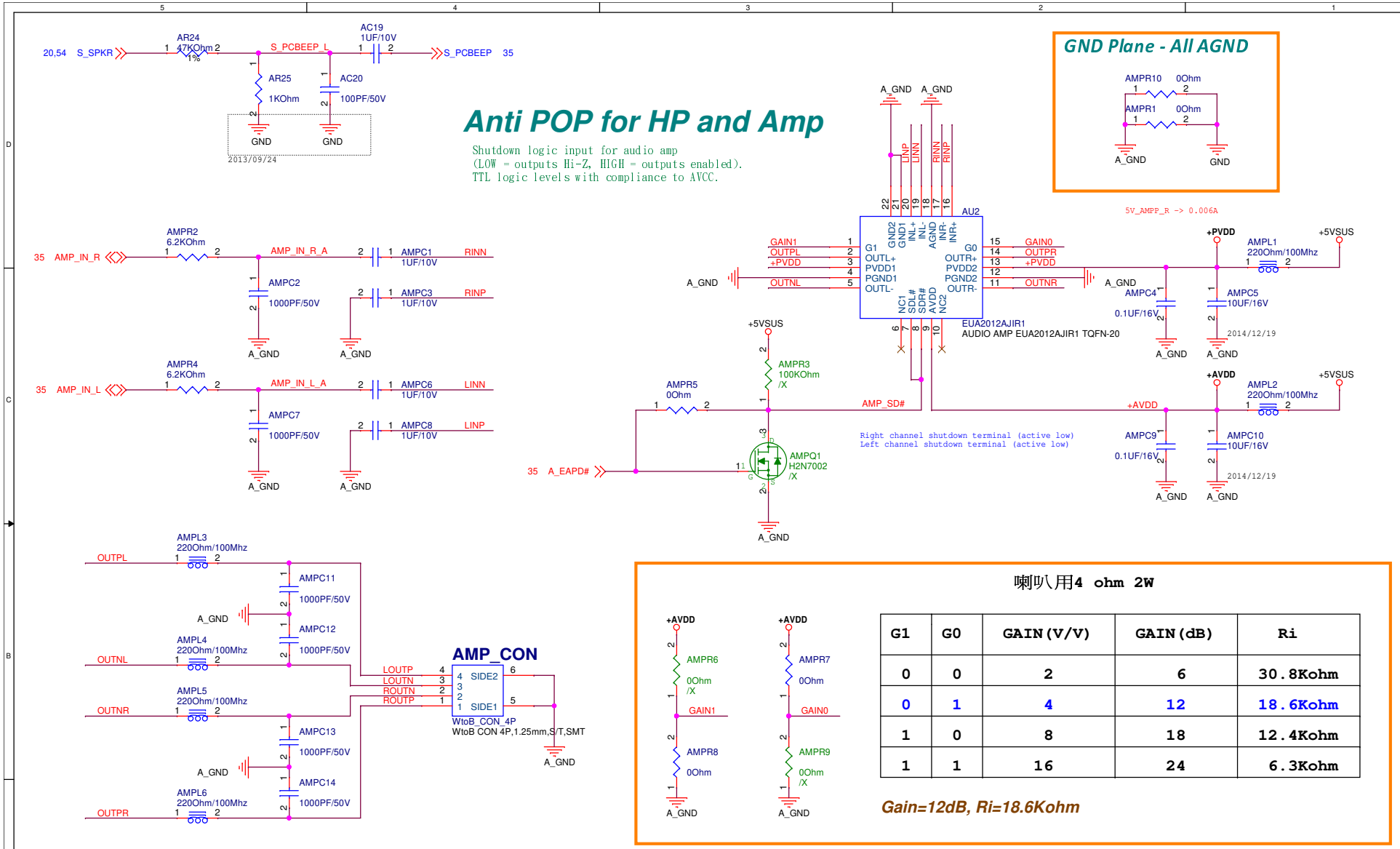




SPDIF Optical (High Rise)

A-12

ASUS	Title : ALC887-VD 6+2CH		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 37 of 75		



喇叭用4 ohm 2W

G1	G0	GAIN(V/V)	GAIN(dB)	Ri
0	0	2	6	30.8Kohm
0	1	4	12	18.6Kohm
1	0	8	18	12.4Kohm
1	1	16	24	6.3Kohm

若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.

R1.00
Ref to page.104 +5VDUAL/5V_DUAL_USBKB*

+L1_I219_+3VSB
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.

1.3

Standard Circuit	
LAN	I218V
REV.	L1_1.3

/X

I218V

PCIE IF
勿接在chipset PCIE port0

16 C_PCIE_L1
16 C_PCIE_L1#
18 X_L1X1_RXP
18 X_L1X1_RXN
18 X_L1X1_TXP
18 X_L1X1_TXN

L1CX1 2 void 1 0.1UF/16V X7R X_L1X1_RXP_C 38 PETp
L1CX2 2 void 1 0.1UF/16V X7R X_L1X1_RXN_C 39 PETn
Close to PHY

SL1CX3 2 1 0.1UF/16V X7R X_L1X1_TXP_C 41 PERp
SL1CX4 2 void 1 0.1UF/16V X7R X_L1X1_TXN_C 42 PERn
Close to Chipset

PE_CLKP 44
PE_CLKN 45

20 L1_SMBCLK
20 L1_SMBDATA

L1C1 2 1 15PF/50V NPO /X
L1C2 2 1 15PF/50V NPO /X
GND
Close to PHY

SMB_CLK 28
SMB_DATA 31

20 L1_LAN_DISABLE#
LAN_DISABLE_N 3

2015/04/16
L1R100 1 2 8.2KOhm
L1R101 1 2 8.2KOhm /X
+L1_I219_+3VSB
GND

L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.

L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

+L1_I219_+3VSB
LT1 1 L1_TP_JDI 32 JTAG_TDI
LT2 1 L1_TP_TDO 34 JTAG_TDO
L1R18 1 8.2KOhm 2 /X L1_TMS 33 JTAG_TMS
L1R19 1 8.2KOhm 2 /X L1_TCK 35 JTAG_TCK

L1R20 1 2.7KOHM 2 L1_TESTEN 30 TEST_EN
CRB 1K
GND

+L1_I219_+3VSB
CRB : L1R3 UNSTUFF FOR LPT-H
L1R9 10KOhm 1 2 L1_CLKREQN 48 CLK_REQ_N
L1R3 0Ohm 2 1
16 CLK_REQ2_LAN#

17,28,29,41,52 S_PLTRST#
PE_RST_N 36
L1C29 2 1 10PF/50V NPO /X
GND

Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0

+L1_I219_0.9V
L1U1C8 0.1UF/16V /X
L1U1C16 0.1UF/16V /X
L1U1C40 0.1UF/16V /X
L1U1C47 0.1UF/16V /X
GND

VDD0P9_46 46
VDD0P9_47 47
VDD0P9_37 37
VDD0P9_43 43
VDD0P9_11 11
VDD0P9_8 8
VDD0P9_40 40
VDD0P9_22 22
VDD0P9_16 16

L1L1 4.7UH 1 2 L1_CTRLP 7 CTRL0P9
L1U1C50 10UF/16V /X
L1U1C49 0.1UF/16V
L1U1C7 22UF/6.3V X5R
GND
L1L1
Idc_min=500 mA
Rdc_max=100 mohm
Placement rule:
1.Place close to L1U1
2.Trace length < 500mil
3.Trace wide > 20mil

L1U1

MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch

MDI_PLUS[0] 13 L1_MDI_0+ 40
MDI_MINUS[0] 14 L1_MDI_0- 40
MDI_PLUS[1] 17 L1_MDI_1+ 40
MDI_MINUS[1] 18 L1_MDI_1- 40
MDI_PLUS[2] 20 L1_MDI_2+ 40
MDI_MINUS[2] 21 L1_MDI_2- 40
MDI_PLUS[3] 23 L1_MDI_3+ 40
MDI_MINUS[3] 24 L1_MDI_3- 40

XTAL_OUT 9 L1_XOUT
XTAL_IN 10 L1_XIN
L1R6 0Ohm 2 1 L1_XOUT_R
L1X1 25Mhz XTAL 25MHZ SMD 10PF/20PPM [GA]EPSON/FA-238
L1C3 10PF/50V NPO
L1C4 10PF/50V NPO
GND

L1X1,L1C7,L1C8
Placement rule:
1.Place close to L1U1
2.Trace length <1inch

+L1_I219_+3VSB
L1R2 300OHM
L1_ACTLEDP 40

LED2 25 L1_LED2 L1R1 1 2 300OHM L1_LINK100# 40
LED1 27 L1_LINK1000# 40
LED0 26 L1_ACTLEDN 40

CRB pull up 4.7Kohm
VDD3P3_IN 5
Close to pin5
L1U1C5 0.1UF/16V
L1U1C48 22UF/6.3V X5R
GND
+L1_I219_+3VSB
L1R21 4.7KOhm 1%
L1R4 4.7KOHM /X
L1R22 4.7KOhm 1%

RSVD1_VCC3P3 1 L1_RSVD
LANWAKE_N 2
SVR_EN_N 6 L1_SVR_EN
L1_LAN_WAKE# 20
L1R26 0Ohm
GND

L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電

L1_LAN_WAKE#
Must be connected to PCH's LANWAKE

+L1_I219_+3VSB
VDD3P3_4 4
VDD3P3_15 15
VDD3P3_19 19
VDD3P3_29 29
L1U1C4 1UF/16V
GND

RBIAS 12 L1_RBIAS
GND_EPAD 49
L1R16 1 3.01KOHM 1% 2
GND

L1R16
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch

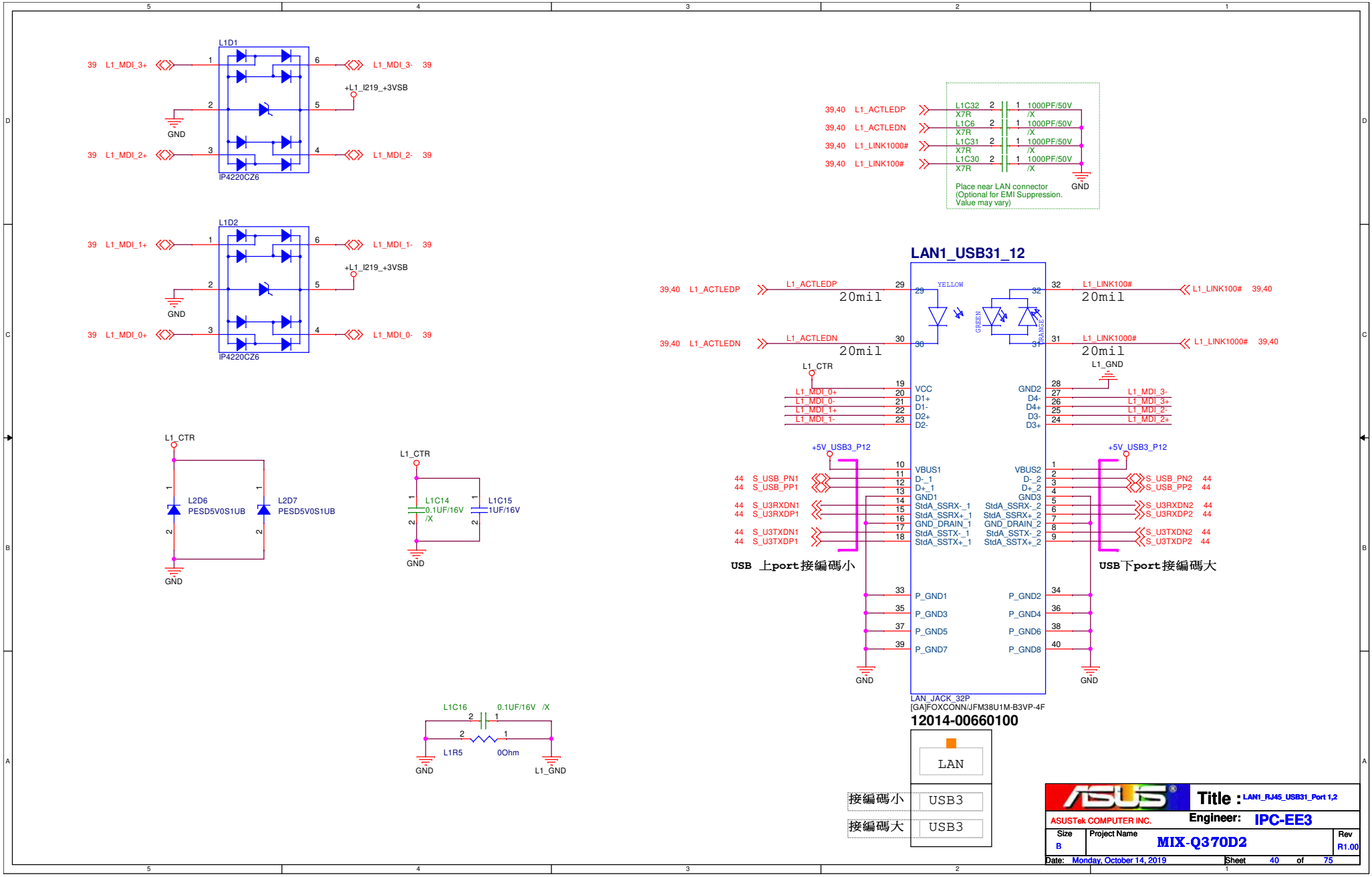
GND1 50
GND2 51
GND3 52
GND4 53
GND

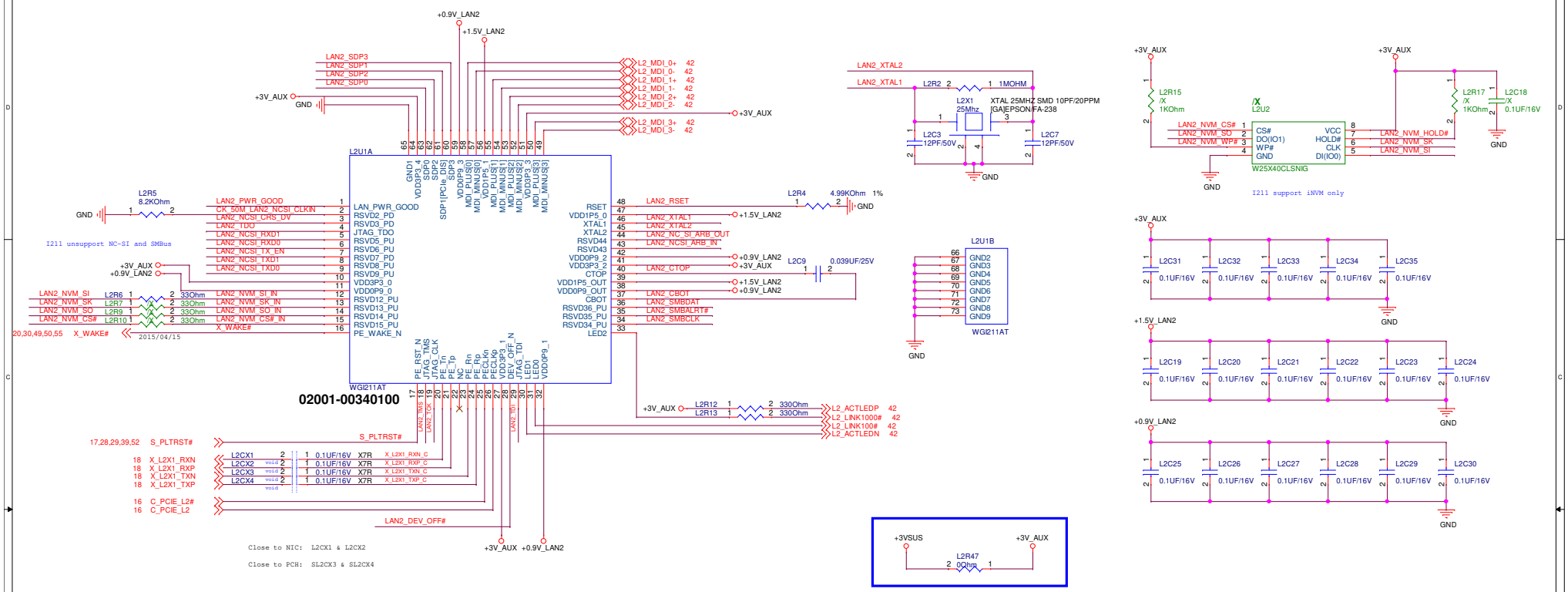
WGI219V
06112-00020000

06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)

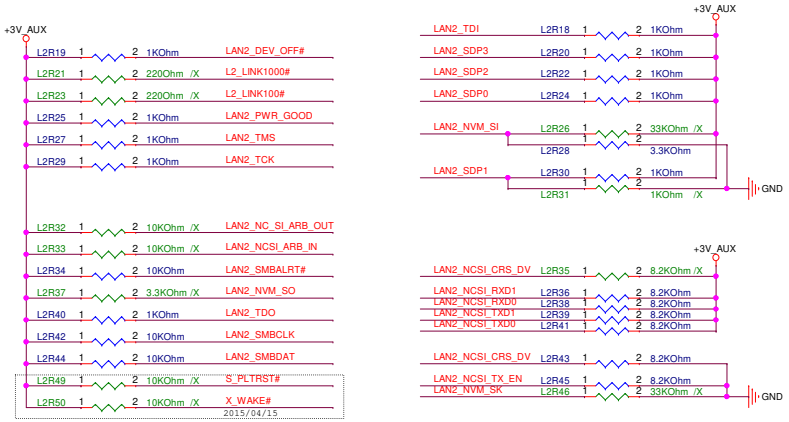
06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)

ASUS
ASUSTek COMPUTER INC.
Title : L1_I219V
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 39 of 75


L1D1
39 L1_MDI_3+
L1_MDI_3- 39
+L1_I219_+3VSB
GND
39 L1_MDI_2+
L1_MDI_2- 39
IP4220CZ6
L1D2
39 L1_MDI_1+
L1_MDI_1- 39
+L1_I219_+3VSB
GND
39 L1_MDI_0+
L1_MDI_0- 39
IP4220CZ6
39,40 L1_ACTLEDP
39,40 L1_ACTLEDN
39,40 L1_LINK1000#
39,40 L1_LINK100#
L1C32 2 1 1000PF/50V X7R /X
L1C6 2 1 1000PF/50V X7R /X
L1C31 2 1 1000PF/50V X7R /X
L1C30 2 1 1000PF/50V X7R /X
Place near LAN connector
(Optional for EMI Suppression.
Value may vary)
GND
LAN1_USB31_12
39,40 L1_ACTLEDP
L1_ACTLEDP 29
20mil
39,40 L1_ACTLEDN
L1_ACTLEDN 30
20mil
YELLOW
GREEN
ORANGE
32 L1_LINK100#
L1_LINK100# 39,40
20mil
31 L1_LINK1000#
L1_LINK1000# 39,40
20mil
L1_CTR
L1_GND
19 VCC
L1_MDI_0+ 20 D1+
L1_MDI_0- 21 D1-
L1_MDI_1+ 22 D2+
L1_MDI_1- 23 D2-
28 GND2
27 D4- L1_MDI_3-
26 D4+ L1_MDI_3+
25 D3- L1_MDI_2-
24 D3+ L1_MDI_2+
+5V_USB3_P12
+5V_USB3_P12
10 VBUS1
44 S_USB_PN1 11 D-_1
44 S_USB_PP1 12 D+_1
13 GND1
44 S_U3RXDN1 14 StdA_SSRX-_1
44 S_U3RXDP1 15 StdA_SSRX+_1
16 GND_DRAIN_1
44 S_U3TXDN1 17 StdA_SSTX-_1
44 S_U3TXDP1 18 StdA_SSTX+_1
1 VBUS2
2 D-_2 S_USB_PN2 44
3 D+_2 S_USB_PP2 44
4 GND3
5 StdA_SSRX-_2
6 StdA_SSRX+_2 S_U3RXDN2 44
7 GND_DRAIN_2 S_U3RXDP2 44
8 StdA_SSTX-_2
9 StdA_SSTX+_2 S_U3TXDN2 44
S_U3TXDP2 44
USB 上port接編碼小
USB下port接編碼大
33 P_GND1
35 P_GND3
37 P_GND5
39 P_GND7
34 P_GND2
36 P_GND4
38 P_GND6
40 P_GND8
GND
GND
LAN_JACK_32P
[GA]FOXCONN/JFM38U1M-B3VP-4F
12014-00660100
LAN
接編碼小 USB3
接編碼大 USB3
L1_CTR
L2D6 PESD5V0S1UB
L2D7 PESD5V0S1UB
GND
L1_CTR
L1C14 0.1UF/16V /X
L1C15 1UF/16V
GND
L1C16 0.1UF/16V /X
L1R5 0Ohm
GND
L1_GND
ASUSTek COMPUTER INC.
Title : LAN1_RJ45_USB31_Port 1,2
Engineer: IPC-EE3
Size B
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 40 of 75



Follow CRB A.B.



Strapping Options

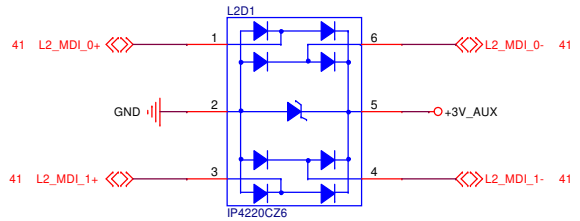
```
DEV_OFF_N
 I210.28 (DEV_OFF_N)
   1: Exit Device off mode (Default)
   0: Enter Device off mode


AUX_PWR
 I210.28 (DEV_OFF_N)
 I210.60 (SDP3)
   11: Enable AUX power mode (Default)


Security_EN
 I210.12 (NVM_SI)
   1: Enable Flash security
   0: Disable Flash security (Default)


PCIE_DIS_N
 I210.61 (SDP1[PCIe_DIS])
   1: Enable PCIe function (Default)
   0: Disable PCIe function
```

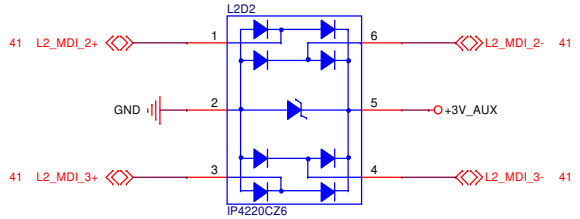
3.4 Voltage Regulator

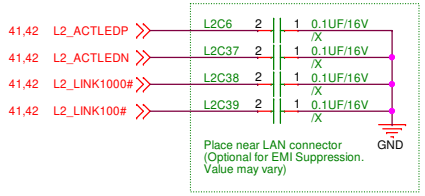
To reduce Bill of Material (BOM) cost, the I211 supports generating the 1.5V and 0.9V power supplies from the 3.3V supply using an on-chip Switching Capacitor Voltage Regulator (SVR) control circuit, which requires only an external capacitor component.

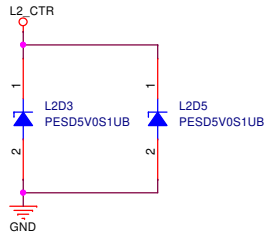
Refer to Section 10.6.4 for more details.

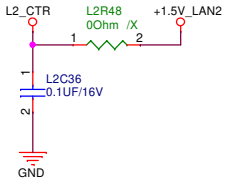
ASUS	Title : LAN2_I210-AT		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.00
Date: Monday, October 14, 2019	Sheet 41 of 75		

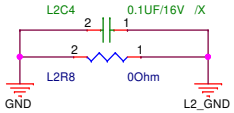


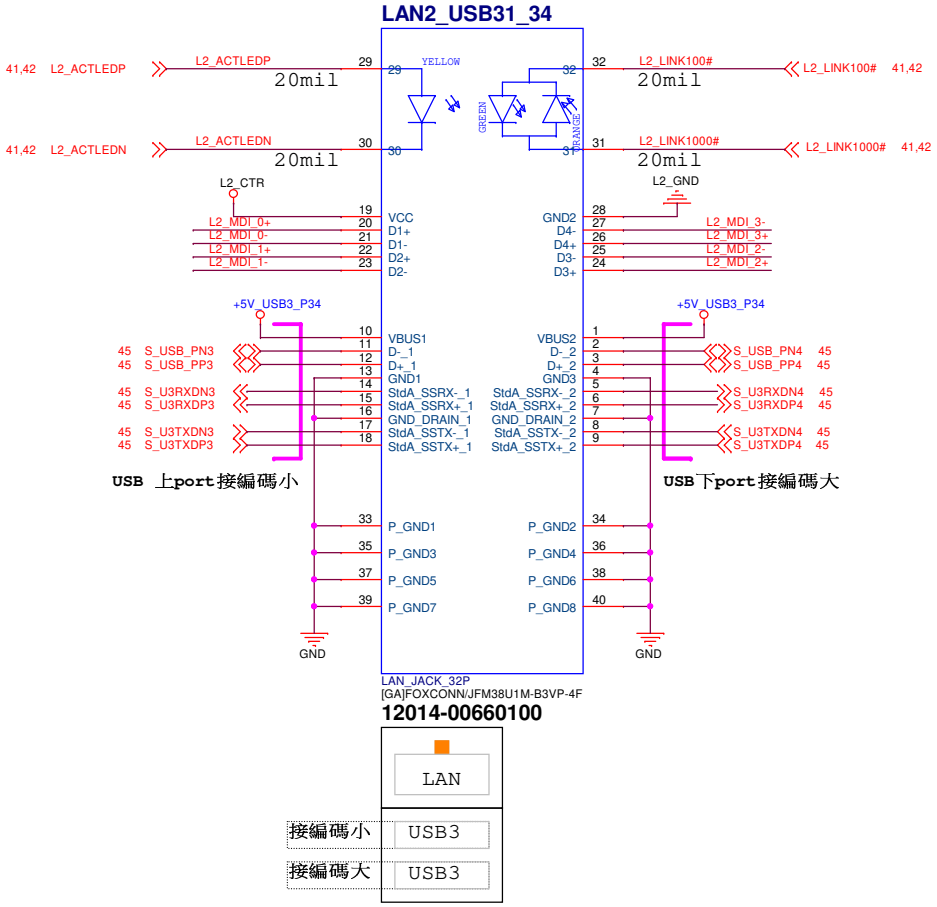




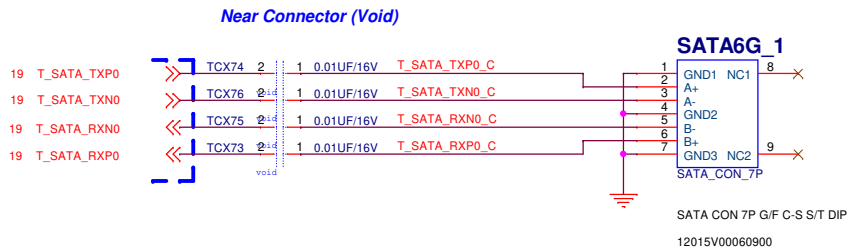


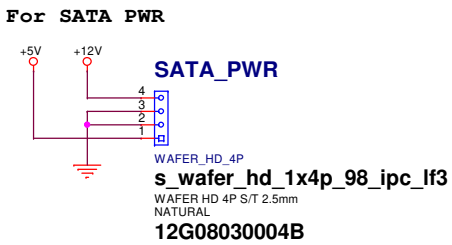


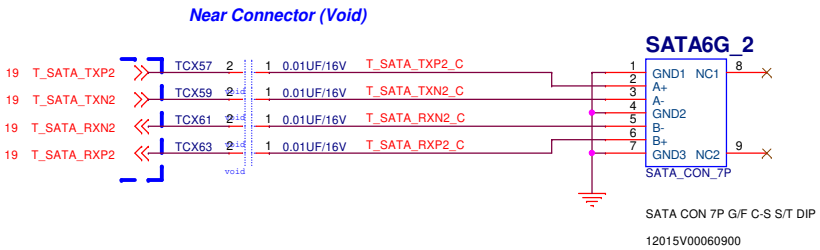




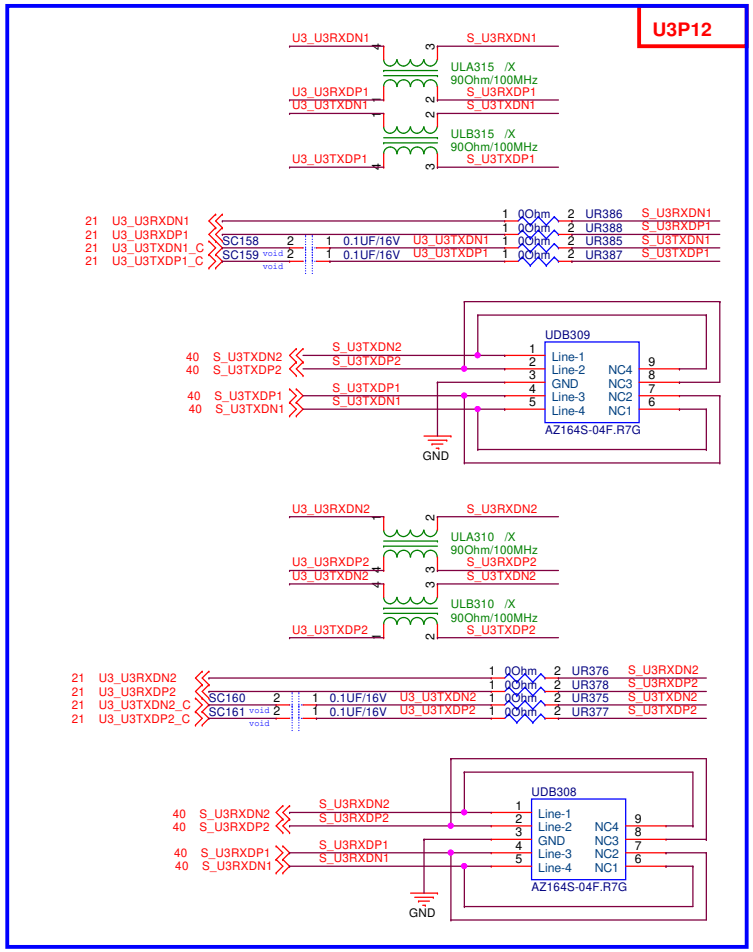
ASUSTek COMPUTER INC.	Title : LAN2_RJ45_USB31_Port 3,4	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 42 of 75	

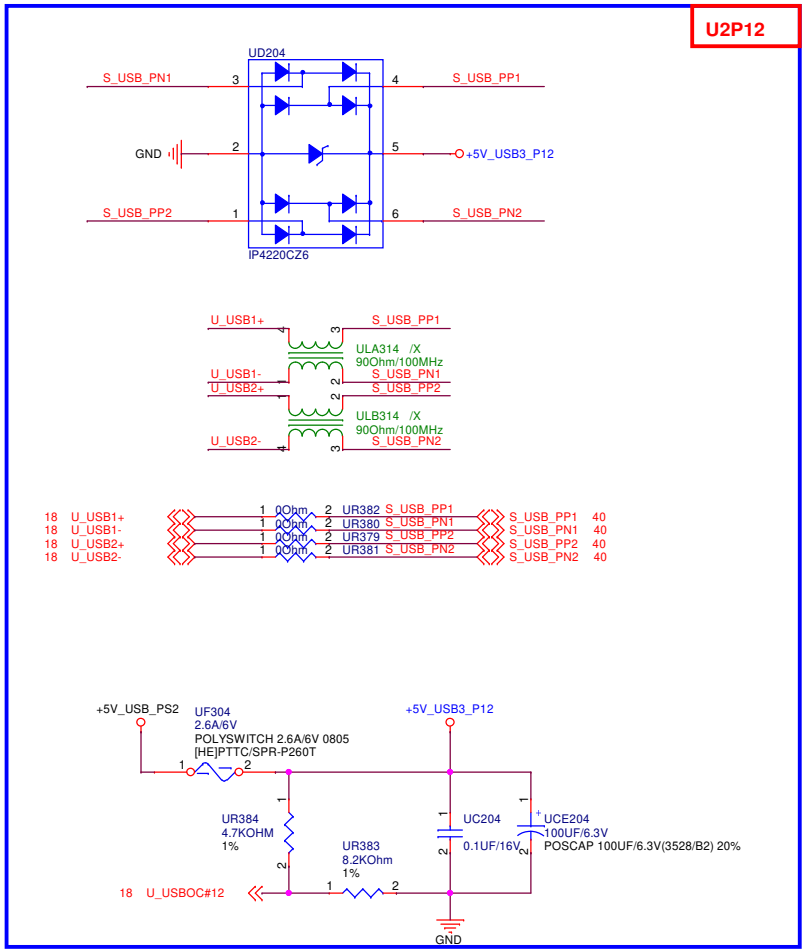


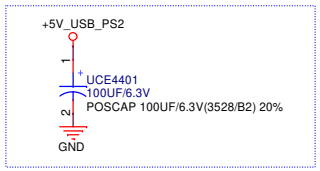




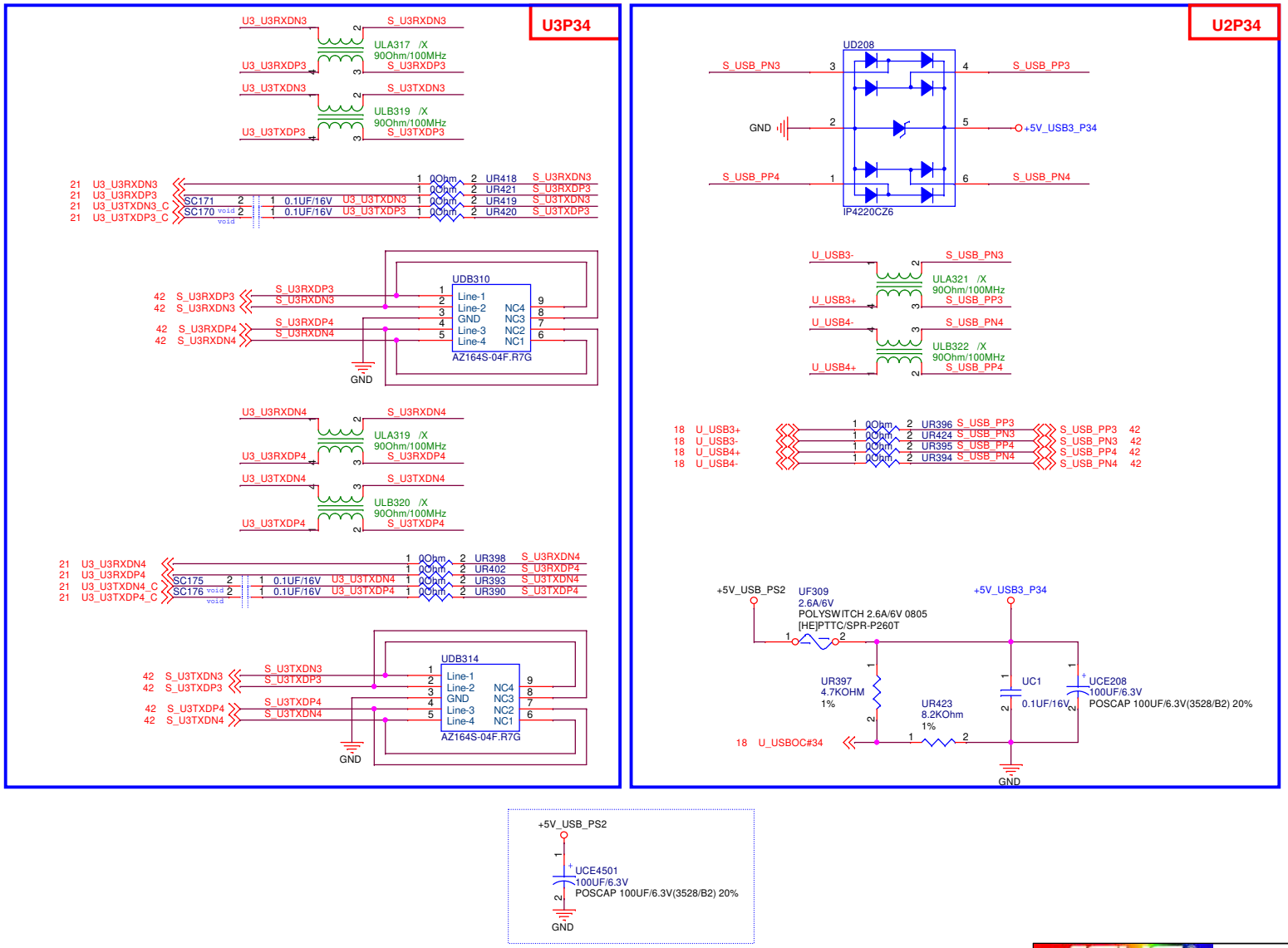
ASUSTek COMPUTER INC.	Title : SATA6G_12345(CHIPSET)	Engineer: IPC-EE3
Size B	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 43 of 75	



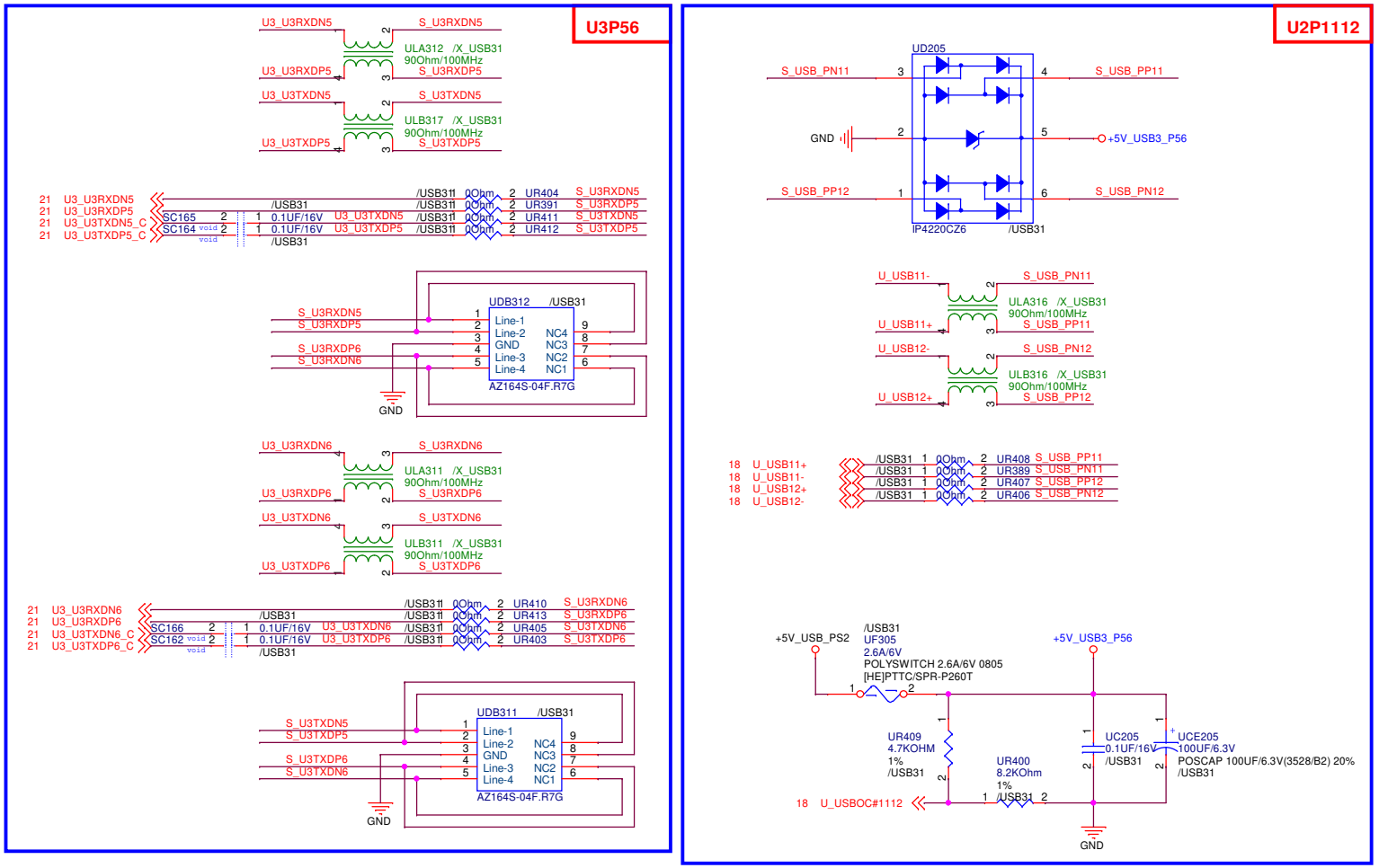




ASUS	Title : USB31 Port 1,2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 44 of 75	



ASUSTek COMPUTER INC.	Title : USB31 Port 3,4	Engineer: IPC-EE3
Size: B	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 45 of 75	



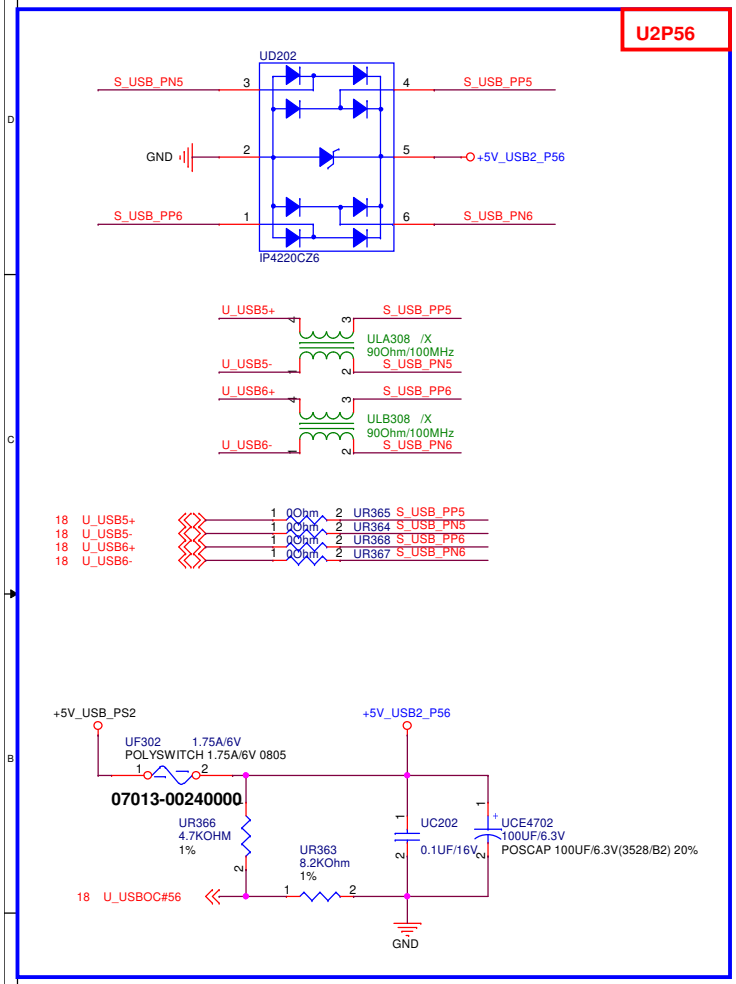
ASUSTek COMPUTER INC.

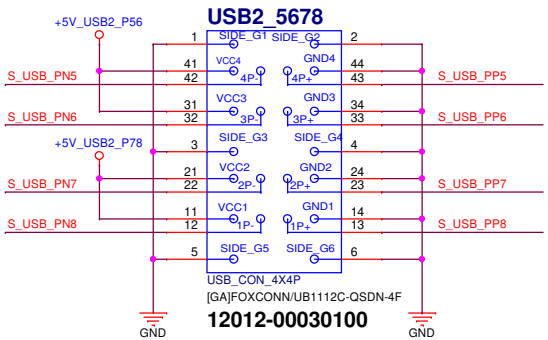
Title : USB31 Port 5,6

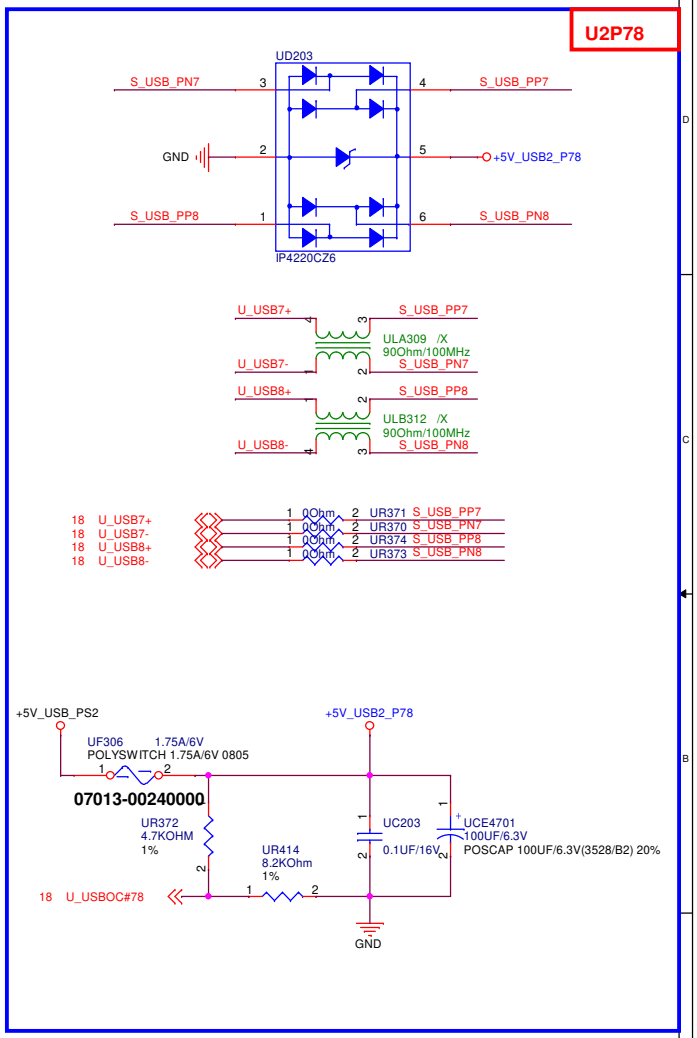
Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.00

Date: Monday, October 14, 2019 Sheet 46 of 75







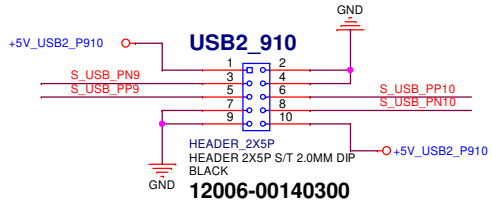
ASUSTek COMPUTER INC.

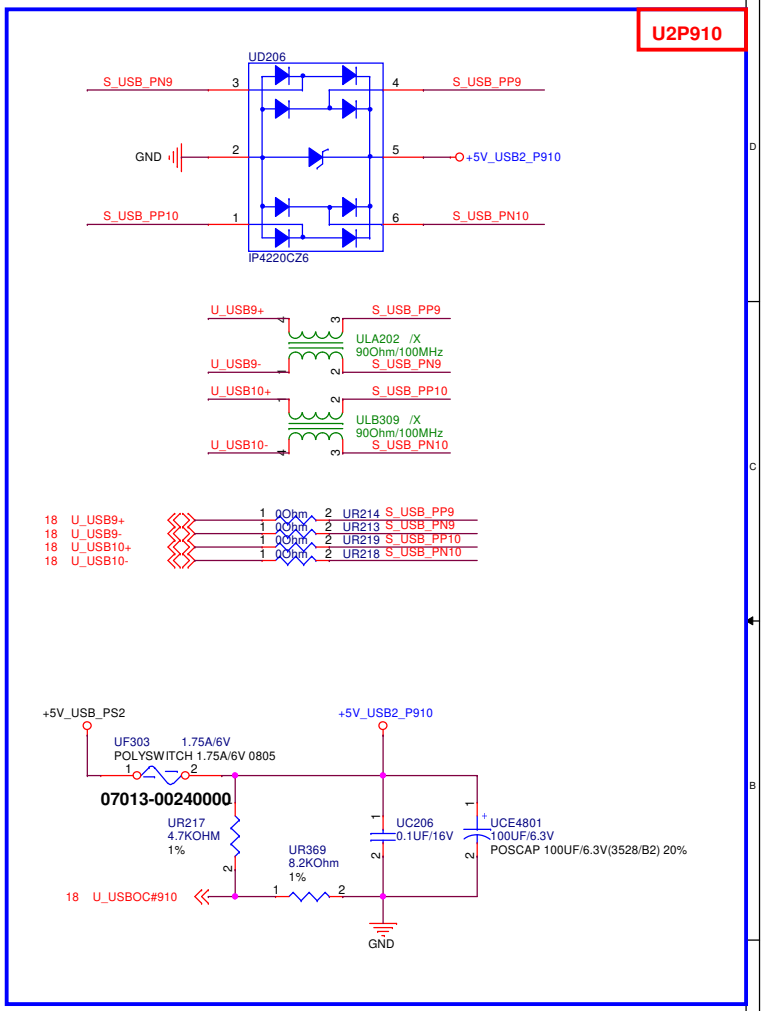
Title : USB2 Port 5,6,7,8

Engineer: IPC-EE3

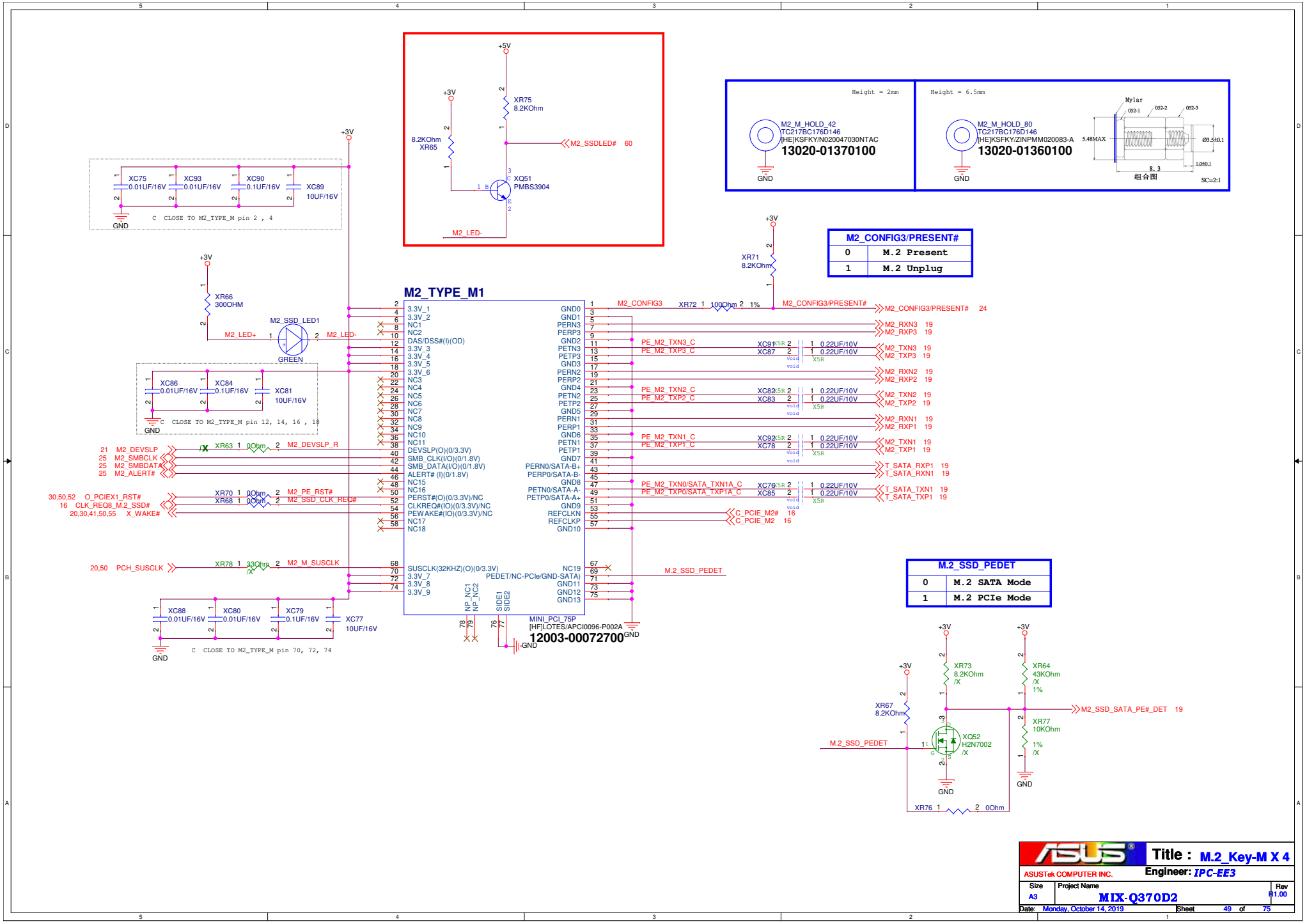
Size	Project Name	Rev
B	MIX-Q370D2	R1.00

Date: Monday, October 14, 2019 Sheet 47 of 75

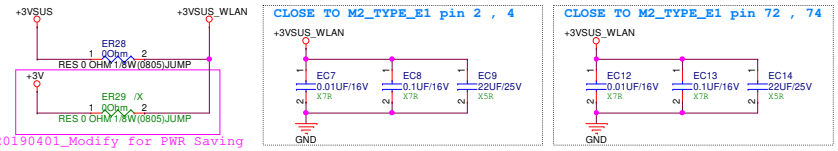




ASUS	Title : USB2 Port 9,10 (Internal)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 48 of 75	

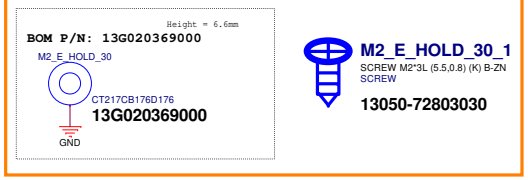

M2_TYPE_M1
MINI_PCI_75P
[HF]LOTES/APCI0096-P002A
12003-00072700
M2_M_HOLD_42
TC217BC176D146
[HE]KSFKY/N020047030NTAC
13020-01370100
Height = 2mm
M2_M_HOLD_80
TC217BC176D146
[HE]KSFKY/ZINPMM020083-A
13020-01360100
Height = 6.5mm
Mylar
5.48MAX
Ø3.5±0.1
1.0±0.1
8.3
组合图
SC=2:1
XR75
8.2KOhm
XR65
8.2KOhm
XQ51
PMBS3904
M2_SSDLED# 60
M2_LED-
XC75
0.01UF/16V
XC93
0.01UF/16V
XC90
0.1UF/16V
XC89
10UF/16V
C CLOSE TO M2_TYPE_M pin 2 , 4
XR66
300OHM
M2_SSD_LED1
GREEN
M2_LED+
XC86
0.01UF/16V
XC84
0.1UF/16V
XC81
10UF/16V
C CLOSE TO M2_TYPE_M pin 12, 14, 16 , 18
XR71
8.2KOhm
M2_CONFIG3
XR72 1 100Ohm 2 1%
M2_CONFIG3/PRESENT#
M2_CONFIG3/PRESENT# 24
M2_RXN3 19
M2_RXP3 19
M2_TXN3 19
M2_TXP3 19
M2_RXN2 19
M2_RXP2 19
M2_TXN2 19
M2_TXP2 19
M2_RXN1 19
M2_RXP1 19
M2_TXN1 19
M2_TXP1 19
T_SATA_RXP1 19
T_SATA_RXN1 19
T_SATA_TXN1 19
T_SATA_TXP1 19
C_PCIE_M2# 16
C_PCIE_M2 16
PE_M2_TXN3_C
PE_M2_TXP3_C
PE_M2_TXN2_C
PE_M2_TXP2_C
PE_M2_TXN1_C
PE_M2_TXP1_C
PE_M2_TXN0/SATA_TXN1A_C
PE_M2_TXP0/SATA_TXP1A_C
XC91 X5R 0.22UF/10V void
XC87 X5R 0.22UF/10V void
XC82 X5R 0.22UF/10V void
XC83 X5R 0.22UF/10V void
XC92 X5R 0.22UF/10V void
XC78 X5R 0.22UF/10V void
XC76 X5R 0.22UF/10V void
XC85 X5R 0.22UF/10V void
21 M2_DEVSLP
25 M2_SMBCLK
25 M2_SMBDATA
25 M2_ALERT#
XR63 1 0Ohm 2 M2_DEVSLP_R
30,50,52 O_PCIEX1_RST#
16 CLK_REQ8_M.2_SSD#
20,30,41,50,55 X_WAKE#
XR70 1 0Ohm 2 M2_PE_RST#
XR68 1 0Ohm 2 M2_SSD_CLK_REQ#
20,50 PCH_SUSCLK
XR78 1 33Ohm 2 M2_M_SUSCLK
M.2_SSD_PEDET
XC88
0.01UF/16V
XC80
0.01UF/16V
XC79
0.1UF/16V
XC77
10UF/16V
C CLOSE TO M2_TYPE_M pin 70, 72, 74
M2_CONFIG3/PRESENT#
0 M.2 Present
1 M.2 Unplug
M.2_SSD_PEDET
0 M.2 SATA Mode
1 M.2 PCIe Mode
XR73
8.2KOhm
/X
XR64
43KOhm
/X
1%
XR67
8.2KOhm
XQ52
H2N7002
/X
XR77
10KOhm
1%
/X
M2_SSD_SATA_PE#_DET 19
XR76 1 2 0Ohm
GND
Title : M.2_Key-M X 4
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 49 of 75

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

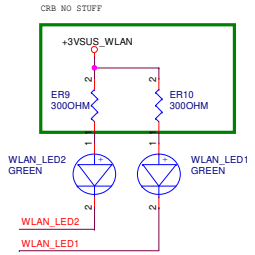


20190401_Modify for PWR Saving

Screw Hole & NUT Hole

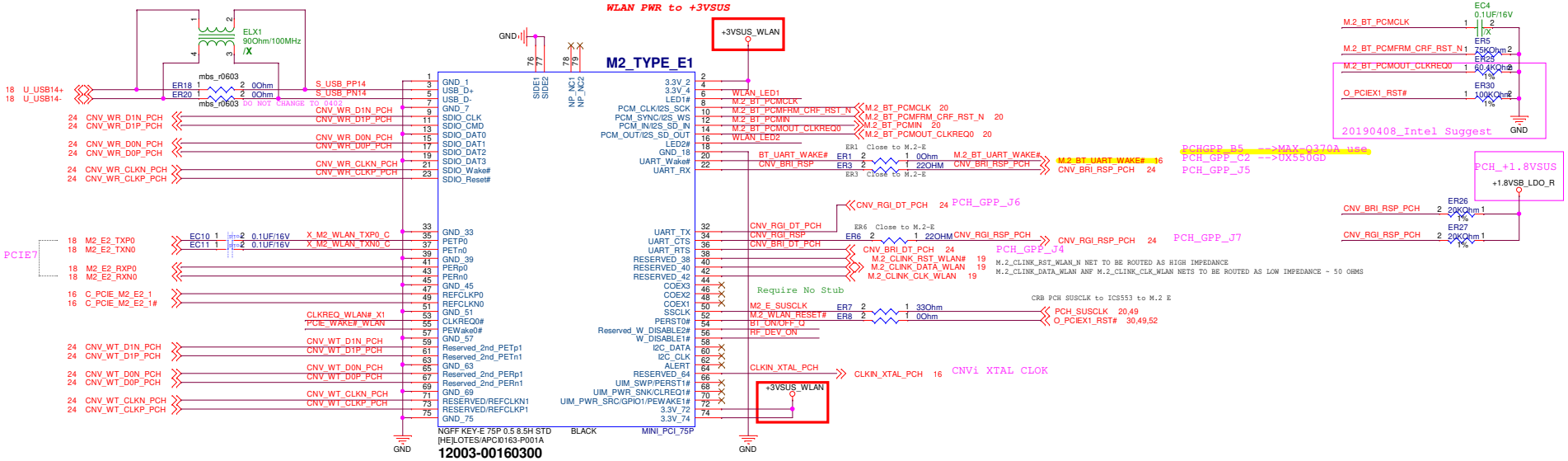


WLAN LED



Support ASUS Open Cloud Computing (AOConnect)

WLAN PWR to +3VSUS



M2_TYPE_E1 NGFF KEY-E 75P 0.5 8.5H STD

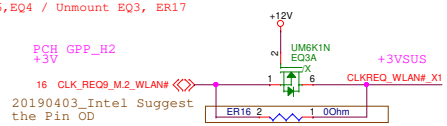
ME-Cost down suggest: P/N : 12003-00160300 LOTES/APCI0163-P001A

20190401_Modify

WLAN CLKREQ#

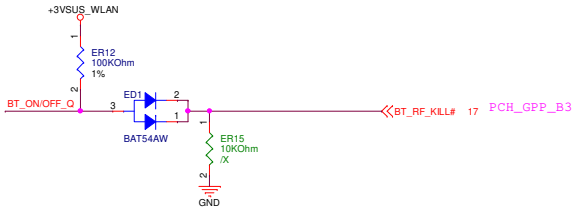
WLAN PWR : +3VSUS (Mount ER28 / Unmount ER29)
Mount EQ3, ER17 / Unmount ER16, EQ4

WLAN PWR : +3V (Mount ER29 / Unmount ER28)
Mount ER16,EQ4 / Unmount EQ3, ER17

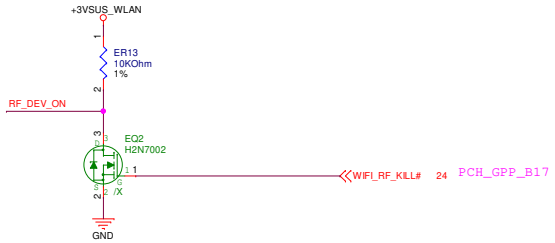


20190401_Modify

BT ON for CNVi Setting



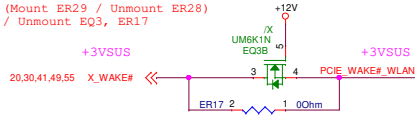
WLAN ON for CNVi Setting



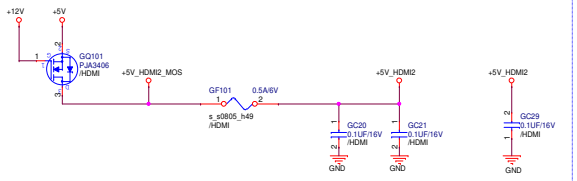
WLAN_Wake# Control

WLAN PWR : +3VSUS (Mount ER28 / Unmount ER29)
Mount EQ3, ER17 / Unmount ER16, EQ4

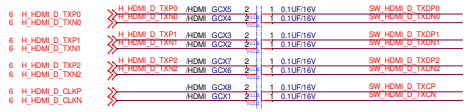
WLAN PWR : +3V (Mount ER29 / Unmount ER28)
Mount ER16,EQ4 / Unmount EQ3, ER17

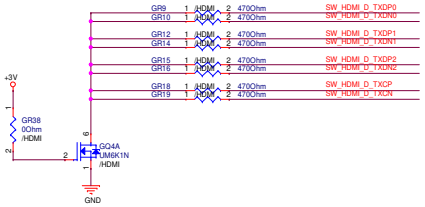


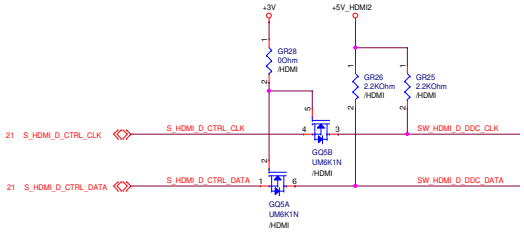
ASUSTek COMPUTER INC.	Title : M.2_Key-E_WLAN_CNVi	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 50 of 75	

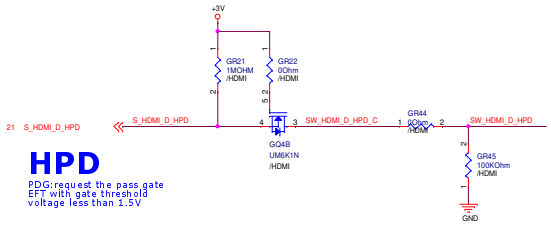


Cost Reduced Level Shifter



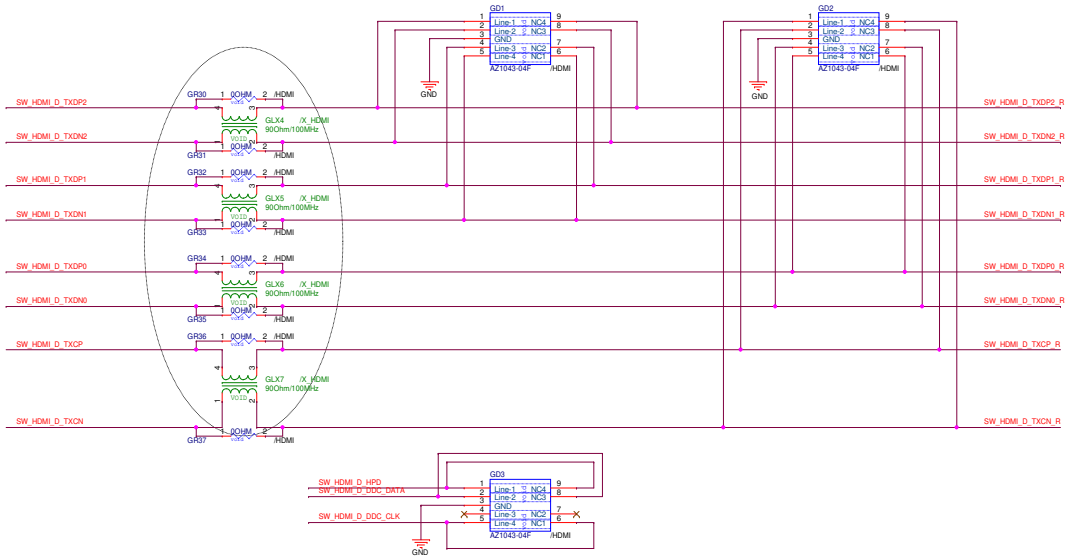






HPD

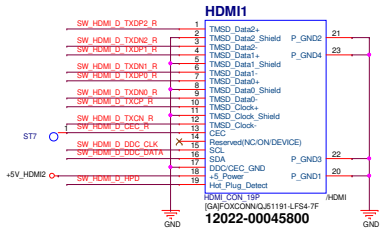
PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V



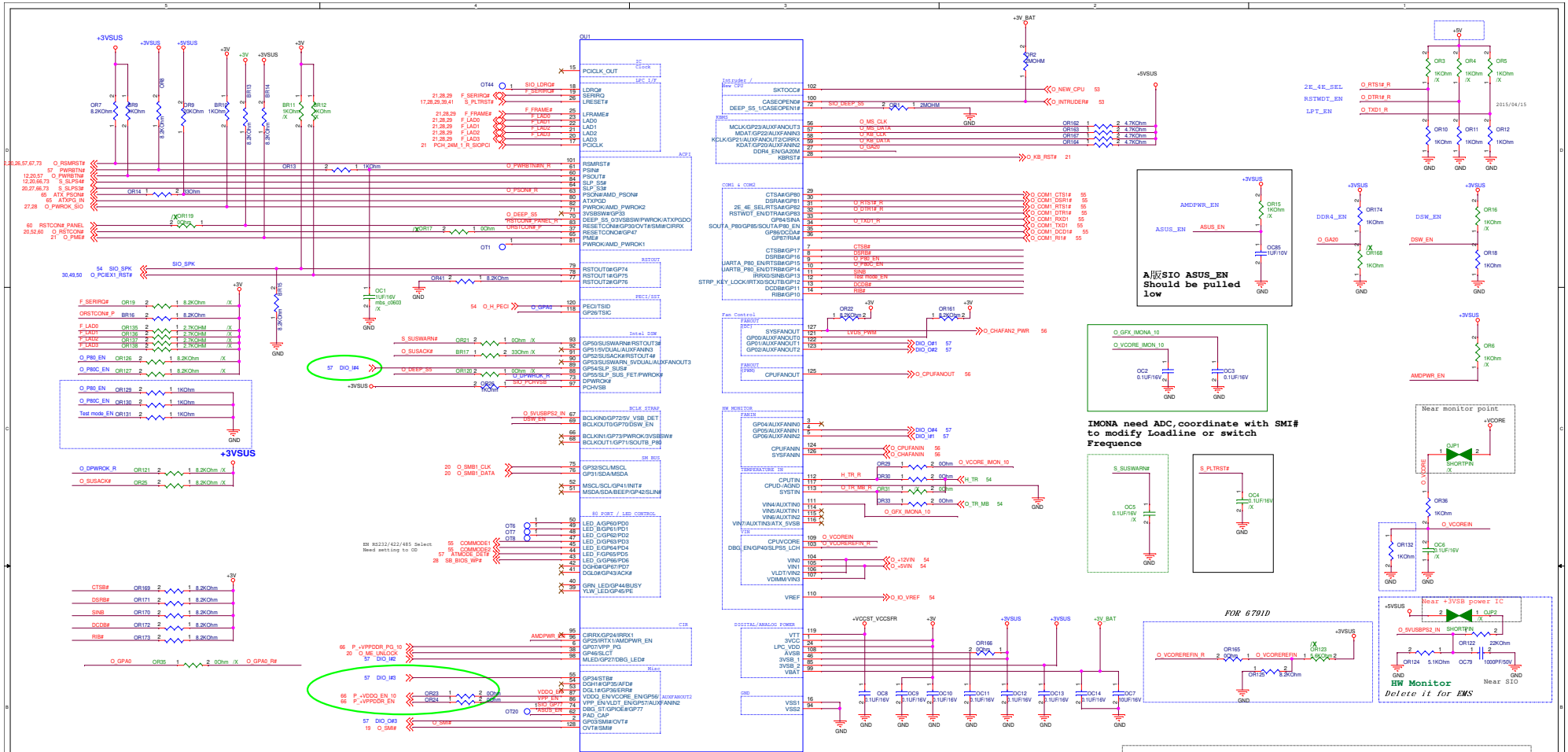
ESD

connector

HDMI-2 (Port D)



ASUS	Title : HDMI-2 (Port D)	
ASUSTeK COMPUTER INC.	Engineer: IPC-EE3	
Size A2	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 51 of 75	

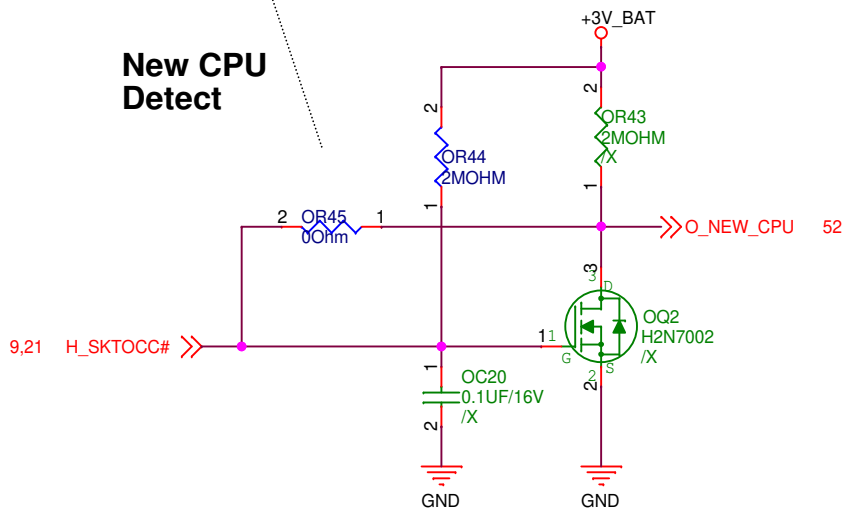


POWER ON STRAPPING PIN NCT6791D

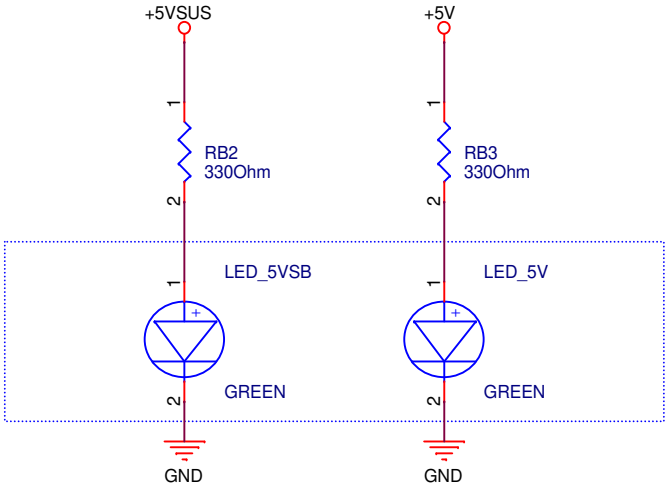
PIN	Name	0	1	Power	Description
31	2E_4E_SEL	2E	4E	VCC	I/O Configuration Address
32	24_48_SEL	24M clock source	48M clock source	VCC	Clock Source Selection
34	LPT_EN	Disable LPT	Enable LPT	VCC	LPT OR OTHERS
62	ASUS_EN	Disable ASUS ASIC	Enable ASUS ASIC	VSB	ASUS GLUE LOGIC
69	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	VSB	DSW OR SVID FUNCTION
71	ANTISURGE_EN	DISABLE ANTISURGE FUNCTION	ENABLE ANTISURGE FUNCTION	VSB	ANTISURGE FUNCTION
96	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	VSB	AMD SEQ OR PVID FUNCTION

ASUSTeK COMPUTER INC.	Title : NCT6793D	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.00
Date: Monday, October 14, 2019	Sheet 52 of 75		

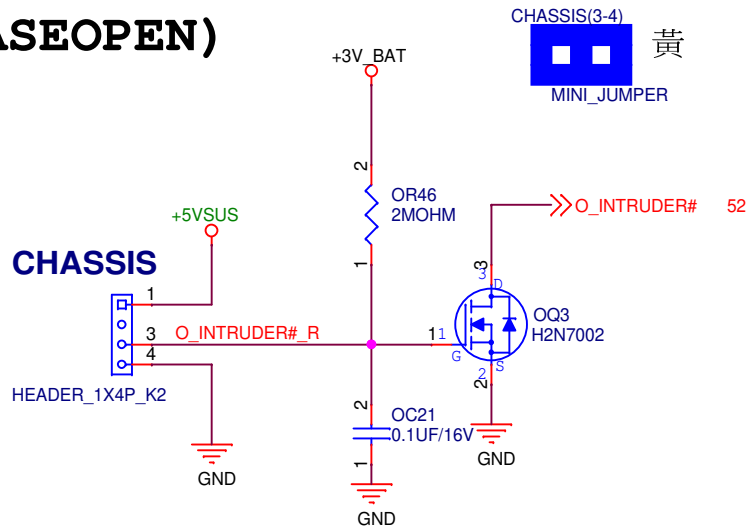
if there is pull-high@CPU side,remove OR31



POWER_PWR

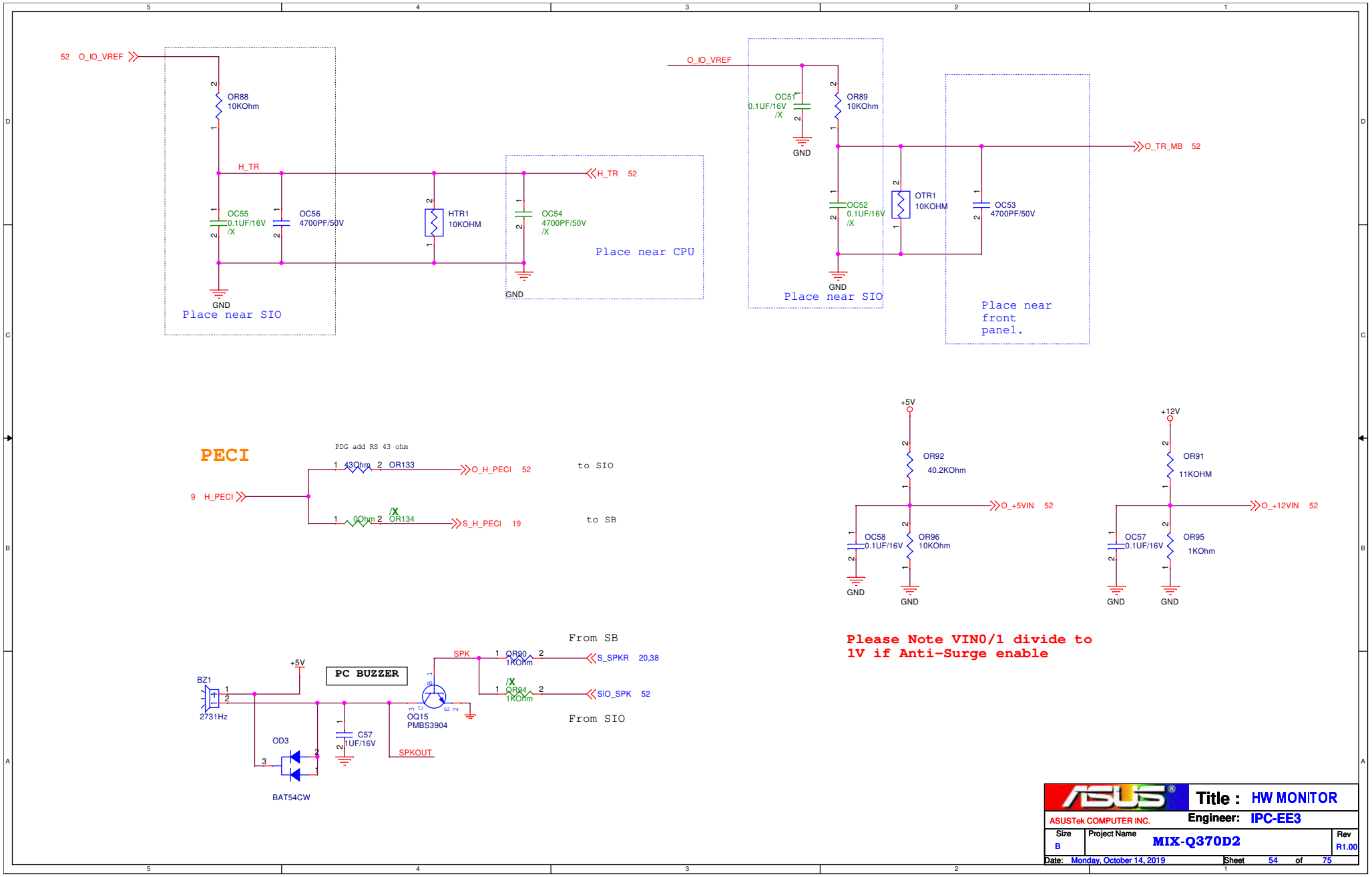


Intrudor (CASEOPEN)

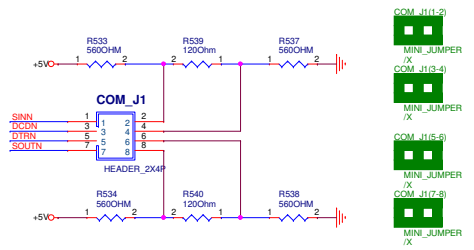


To SIO

ASUSTek COMPUTER INC.	Title : Intrudor(CASEOPEN)		
	Engineer: IPC-EE3		
Size A	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 53 of 75		


52 O_IO_VREF
OR88
10KOhm
H_TR
OC55
0.1UF/16V
/X
OC56
4700PF/50V
HTR1
10KOHM
OC54
4700PF/50V
/X
H_TR 52
GND
Place near SIO
Place near CPU
O_IO_VREF
OC51
0.1UF/16V
/X
OR89
10KOhm
OC52
0.1UF/16V
/X
OTR1
10KOHM
OC53
4700PF/50V
O_TR_MB 52
Place near SIO
Place near front panel.
PECI
PDG add RS 43 ohm
9 H_PECI
43Ohm OR133
O_H_PECI 52
to SIO
0Ohm OR134
/X
S_H_PECI 19
to SB
+5V
OR92
40.2KOhm
O_+5VIN 52
OC58
0.1UF/16V
OR96
10KOhm
+12V
OR91
11KOHM
O_+12VIN 52
OC57
0.1UF/16V
OR95
1KOhm
Please Note VIN0/1 divide to
1V if Anti-Surge enable
From SB
SPK
OR90
1KOhm
S_SPKR 20,38
OR94
1KOhm
SIO_SPK 52
From SIO
BZ1
2731Hz
+5V
PC BUZZER
OD3
BAT54CW
C57
1UF/16V
OQ15
PMBS3904
SPKOUT
Title : HW MONITOR
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size B
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 54 of 75

RS422/RS485 Terminator



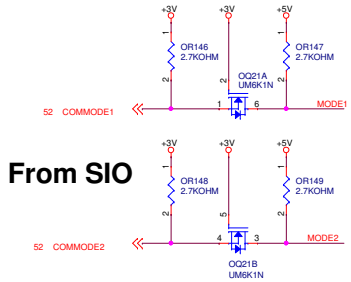
COM_J1 all off -->RS232
COM_J1 all on -->RS485/RS422 with terminator

Mode Selection

SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ. As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.

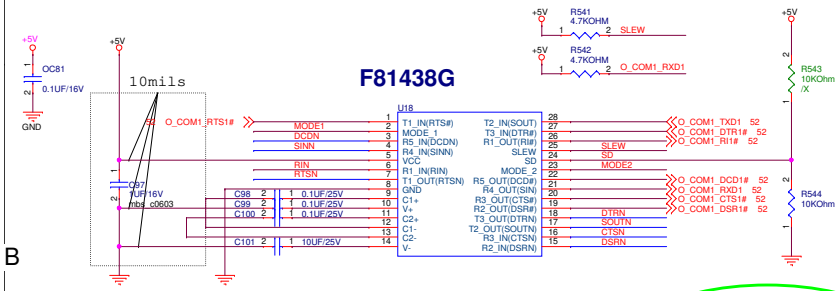


(VDD = +5.0V ± 5%)

Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01.		2	30	mA
Supply Current (RS-485)	No Load, MODE = 10, 11.		2		mA
Supply Current (RS-422)	MODE = 00.		2		mA
Operating Temperature *	Symbol: T	-40		85	◦ C

(VDD = +5.0V ± 5%)

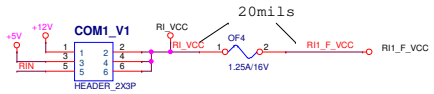
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V_{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	μA	
Driver Input Pull High Current	I_{IT}			±15	μA	

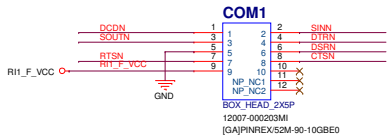


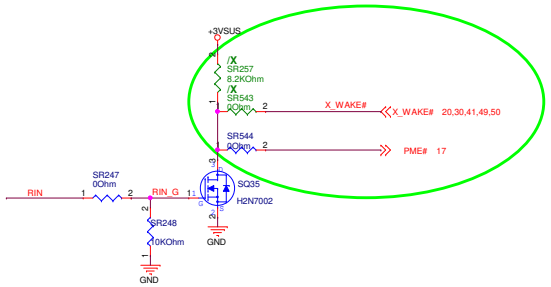
COM1_V1(5-6)	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

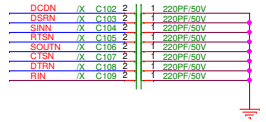
COM1_V1(5-6)

MINI_JUMPER

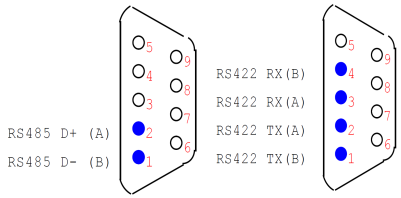






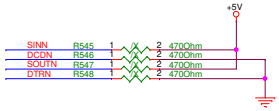


Close to COM port connector



Maximum Slew rate control

SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps



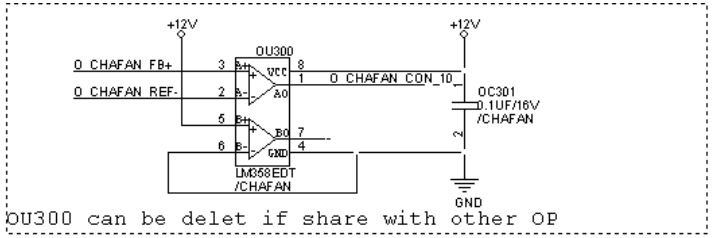
Note:Reserved for FAIL-SAVE

ASUSTek COMPUTER INC.	Title : COM1_RS232/422/485
	Engineer: IPC-EE3
Size: Custom	Project Name: MIX-Q370D2
	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 55 of 75

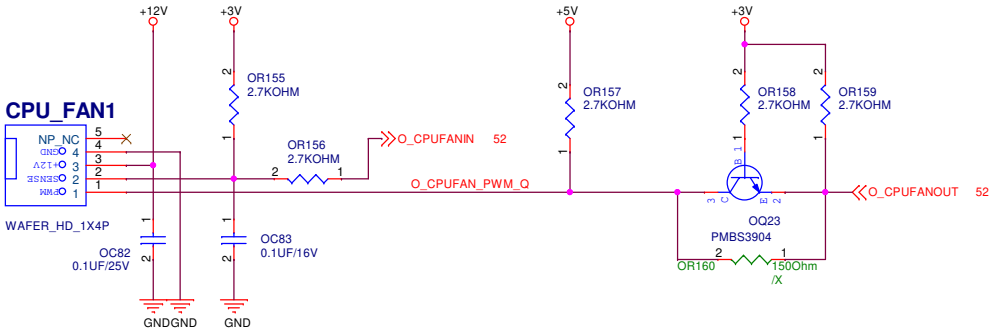
FAN CONTROL

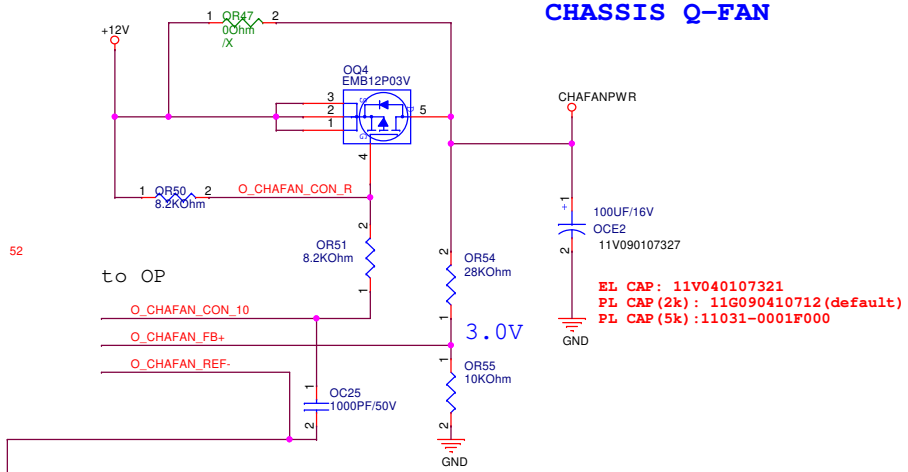
PWM FAN CONTROL(New)

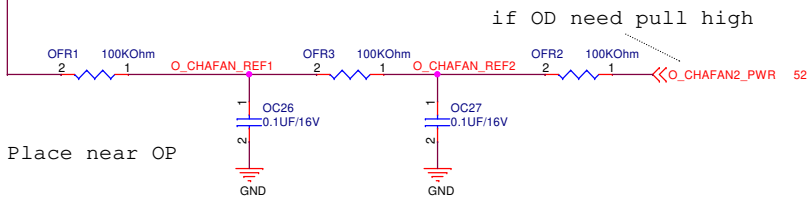
Pin Number	Signal
1	Control
2	Sense
3	+12V
4	GND

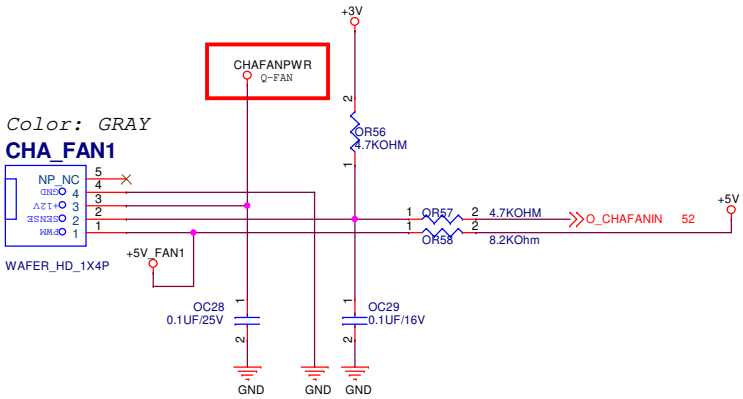


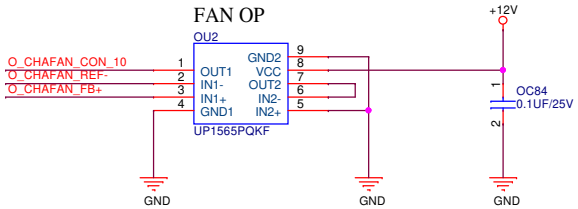
CHASSIS Q-FAN











ASUSTek COMPUTER INC.

Title : CPUFAN_SYSFAN1

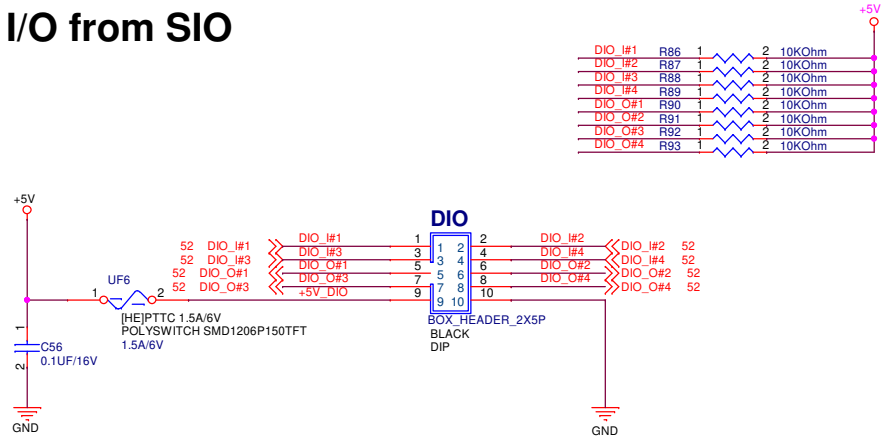
Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.00

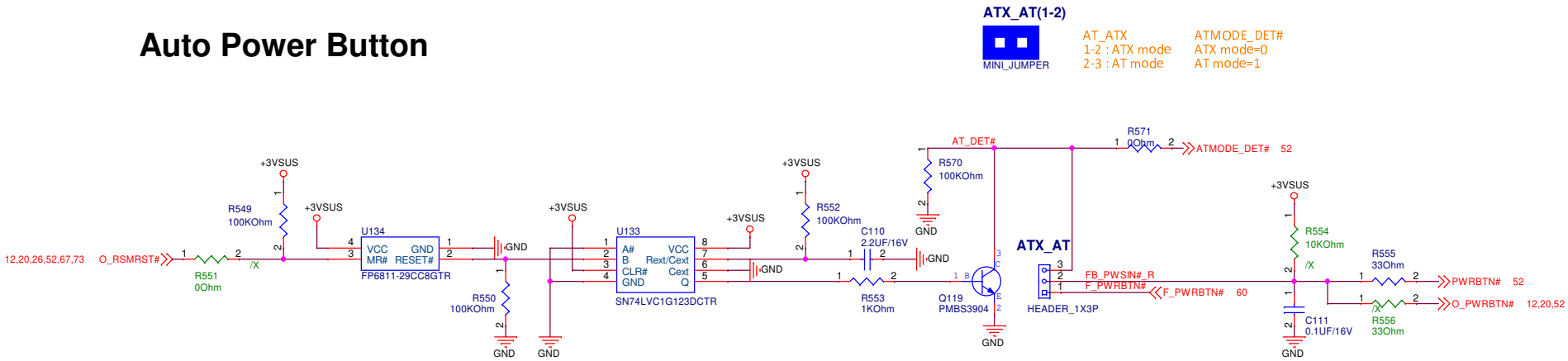
Date: Monday, October 14, 2019 Sheet 56 of 75

COM2

Digitial I/O from SIO



Auto Power Button



ASUSTek COMPUTER INC.

Title : DIO/ATX

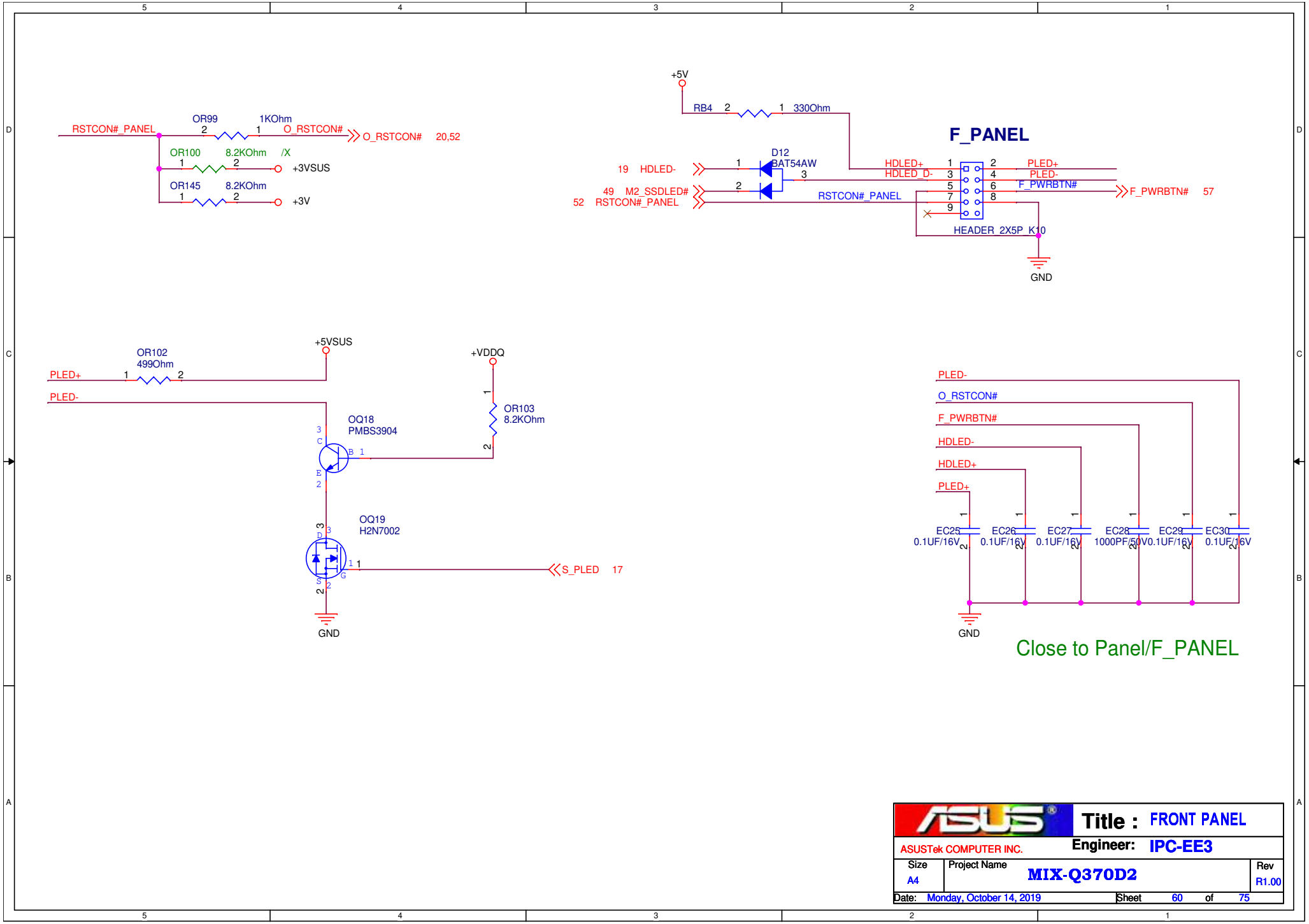
Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.00

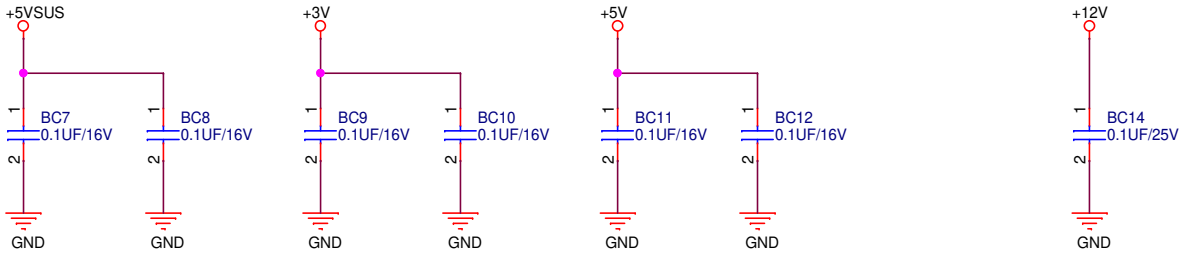
Date: Monday, October 14, 2019 Sheet 57 of 75

ASUSTek COMPUTER INC.	Title : F81216HD-I			
	Engineer: IPC-EE3			
Size B	Project Name MIX-Q370D2			Rev R1.00
Date: Monday, October 14, 2019		Sheet 58 of 75		

Title : XXXXX		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 59 of 75	


RSTCON#_PANEL
OR99
1KOhm
O_RSTCON#
O_RSTCON# 20,52
OR100
8.2KOhm
/X
+3VSUS
OR145
8.2KOhm
+3V
+5V
RB4
330Ohm
F_PANEL
19 HDLED-
D12
BAT54AW
49 M2_SSDLED#
52 RSTCON#_PANEL
HDLED+
HDLED_D-
RSTCON#_PANEL
PLED+
PLED-
F_PWRBTN#
F_PWRBTN# 57
HEADER_2X5P_K10
GND
OR102
499Ohm
+5VSUS
+VDDQ
PLED+
PLED-
OR103
8.2KOhm
OQ18
PMBS3904
OQ19
H2N7002
S_PLED 17
GND
PLED-
O_RSTCON#
F_PWRBTN#
HDLED-
HDLED+
PLED+
EC25
0.1UF/16V
EC26
0.1UF/16V
EC27
0.1UF/16V
EC28
1000PF/50V
EC29
0.1UF/16V
EC30
0.1UF/16V
GND
Close to Panel/F_PANEL
Title : FRONT PANEL
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A4
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 60 of 75

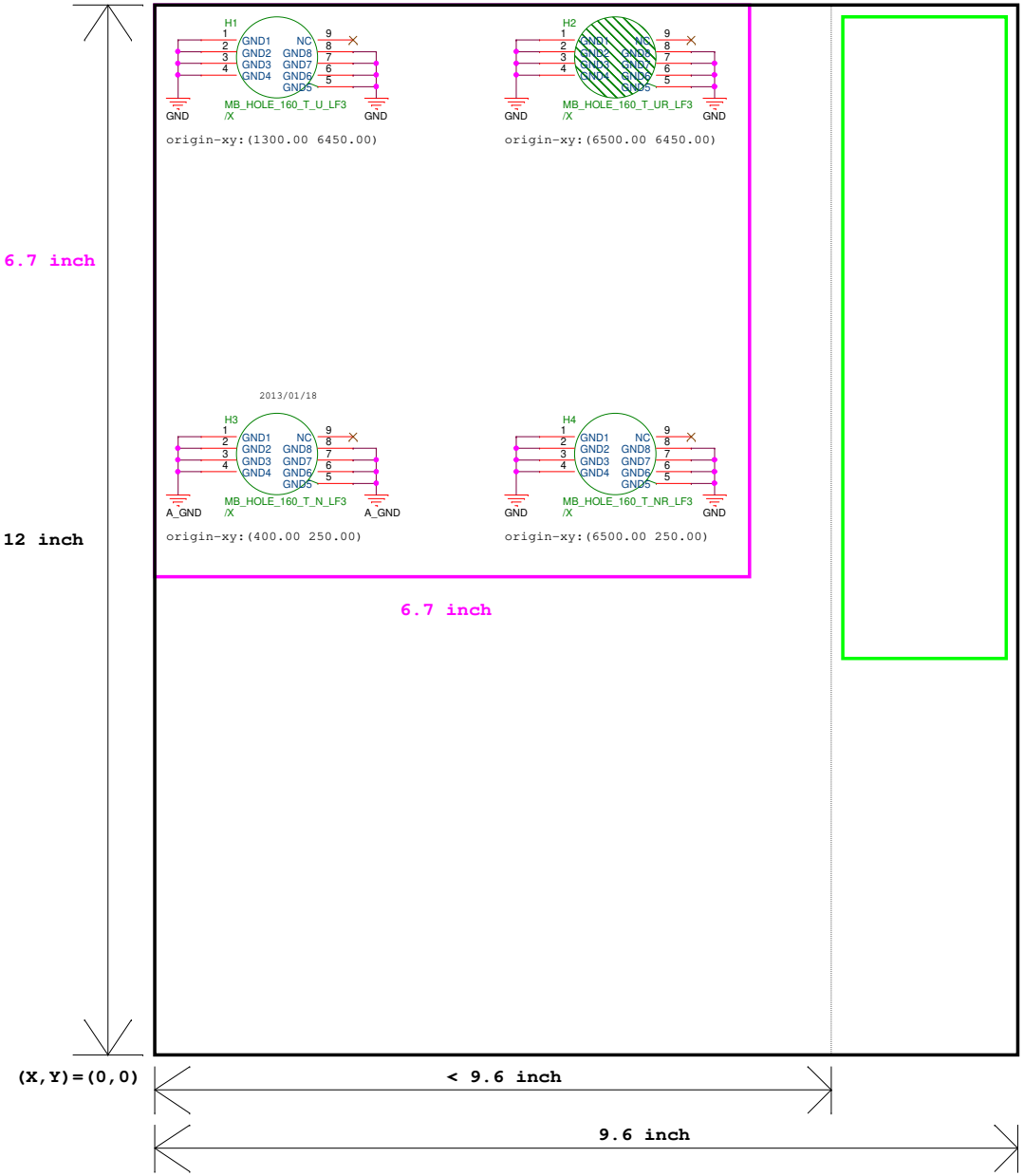
Bypass/EMI Capacitor



ASUS	Title : EMI Cap	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A4	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 61 of 75	

Delete it for EMS

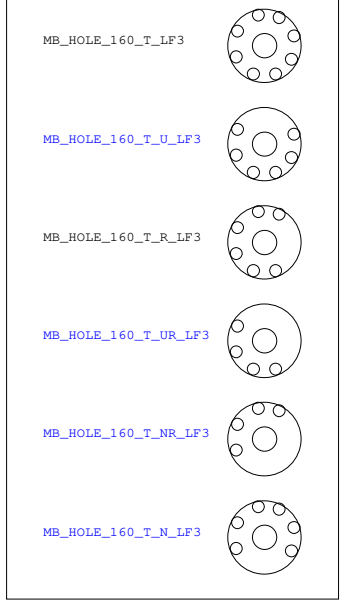
mini-ITX Screw Hole



m-ATX Screw Select

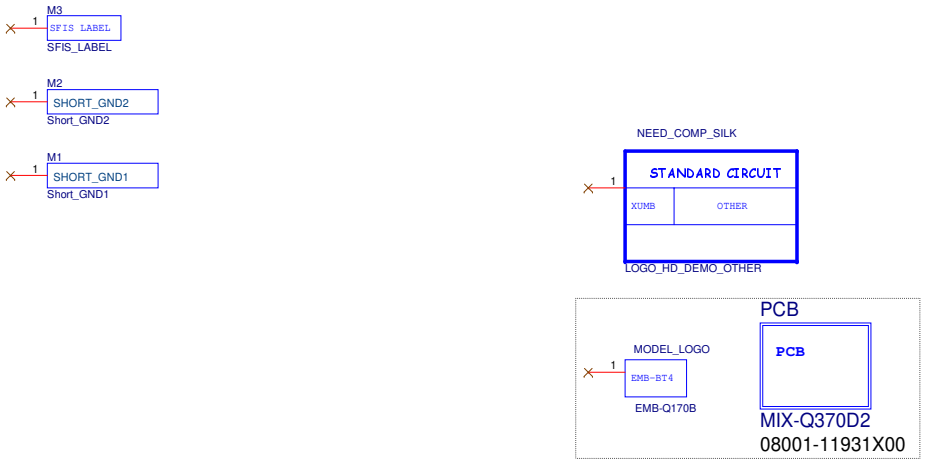
	Standard (9.6 x 9.6)	Scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H20	V	V

MB SCREW FOOTPRINT



ASUS	Title : Screw Hole	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 62 of 75	

Selling Point

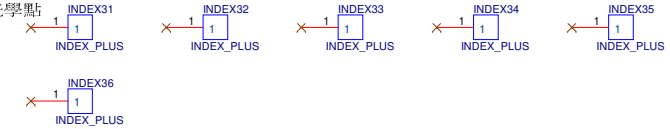


Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

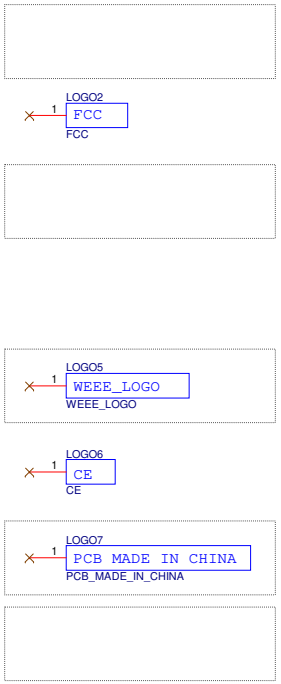
小顆十字光學點



2012/09/11

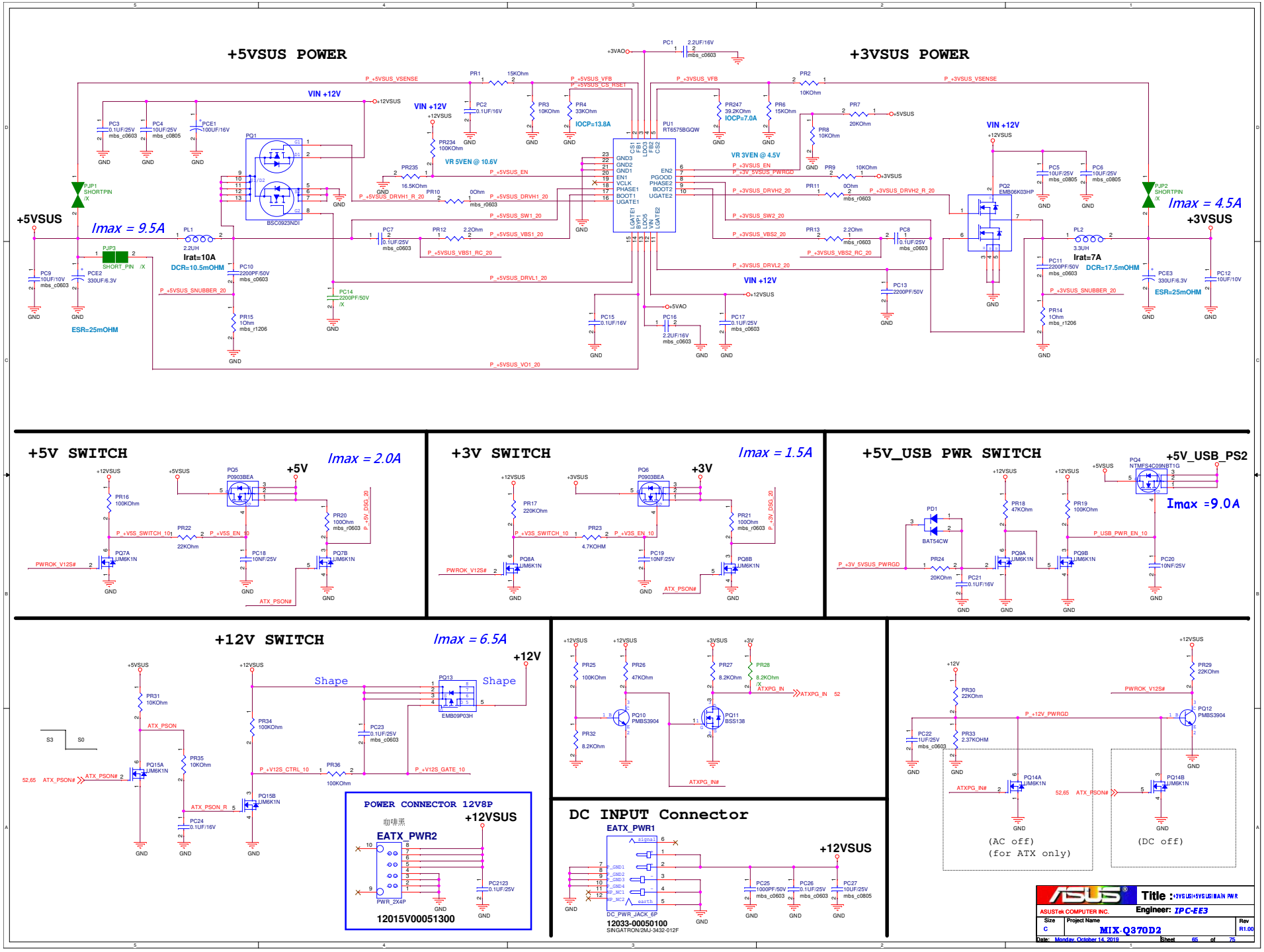
Logo

common Logo for all projects



ASUSTek COMPUTER INC.	Title : Selling Point_Logo	
	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 63 of 75	

ASUSTek COMPUTER INC.	Title : COM3-6		
	Engineer: IPC-EE3		
Size B	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019		Sheet 64 of 75	


+5VSUS POWER
+3VSUS POWER
+5VSUS
Imax = 9.5A
Irat=10A
DCR=10.5mOHM
ESR=25mOHM
+3VSUS
Imax = 4.5A
Irat=7A
DCR=17.5mOHM
ESR=25mOHM
VIN +12V
VR 5VEN @ 10.6V
VR 3VEN @ 4.5V
IOCP=13.8A
IOCP=7.0A
PU1
RT6575BGQW
BSC0923NDI
PQ2
EMB06K03HP
+5V SWITCH
Imax = 2.0A
+5V
PQ5
P0903BEA
PQ7A
UM6K1N
PQ7B
UM6K1N
+3V SWITCH
Imax = 1.5A
+3V
PQ6
P0903BEA
PQ8A
UM6K1N
PQ8B
UM6K1N
+5V_USB PWR SWITCH
+5V_USB_PS2
Imax =9.0A
PQ4
NTMFS4C09NBT1G
PQ9A
UM6K1N
PQ9B
UM6K1N
+12V SWITCH
Imax = 6.5A
+12V
Shape
PQ13
EMB09P03H
PQ15A
UM6K1N
PQ15B
UM6K1N
S3
S0
POWER CONNECTOR 12V8P
咖啡黑
EATX_PWR2
+12VSUS
PWR_2X4P
12015V00051300
PQ10
PMBS3904
PQ11
BSS138
PQ12
PMBS3904
PQ14A
UM6K1N
PQ14B
UM6K1N
(AC off)
(for ATX only)
(DC off)
DC INPUT Connector
EATX_PWR1
DC_PWR_JACK_6P
12033-00050100
SINGATRON/2MJ-3432-012F
+12VSUS
Title : +5VSUS+3VSUS+5VSUS+MAIN PWR
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
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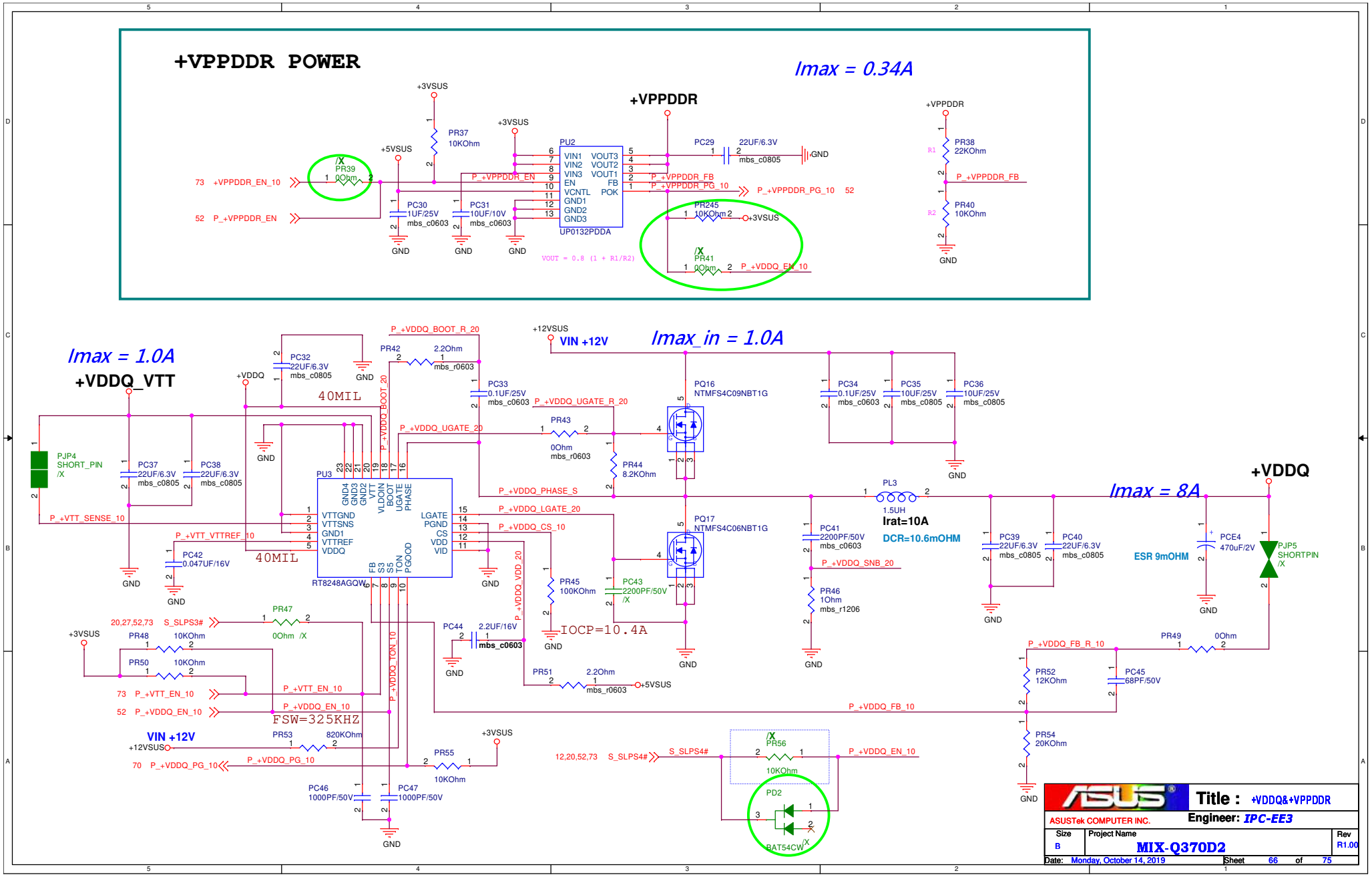
+VPPDDR POWER
Imax = 0.34A
+VPPDDR
+3VSUS
+5VSUS
PR37 10KOhm
PR39 0Ohm /X
73 +VPPDDR_EN_10
52 P_+VPPDDR_EN
PC30 1UF/25V mbs_c0603
PC31 10UF/10V mbs_c0603
PU2
VIN1 VIN2 VIN3 EN VCNTL GND1 GND2 GND3
VOUT3 VOUT2 VOUT1 FB POK
UP0132PDDA
PC29 22UF/6.3V mbs_c0805
P_+VPPDDR_FB
P_+VPPDDR_PG_10
52
PR245 10KOhm
PR41 0Ohm /X
P_+VDDQ_EN_10
VOUT = 0.8 (1 + R1/R2)
PR38 22KOhm
PR40 10KOhm
Imax = 1.0A
+VDDQ_VTT
PC32 22UF/6.3V mbs_c0805
40MIL
PJP4 SHORT_PIN /X
PC37 22UF/6.3V mbs_c0805
PC38 22UF/6.3V mbs_c0805
P_+VTT_SENSE_10
PC42 0.047UF/16V
P_+VTT_VTTREF_10
PU3
RT8248AGQW
VTTGND VTTSNS GND1 VTTREF VDDQ
GND4 GND3 GND2 VTT VLDOIN BOOT UGATE PHASE
LGATE PGND CS VDD VID
FB S3 S5 TON PGOOD
P_+VDDQ_BOOT_R_20
PR42 2.2Ohm mbs_r0603
P_+VDDQ_BOOT_20
P_+VDDQ_UGATE_20
P_+VDDQ_UGATE_R_20
PC33 0.1UF/25V mbs_c0603
PR43 0Ohm mbs_r0603
PR44 8.2KOhm
P_+VDDQ_PHASE_S
P_+VDDQ_LGATE_20
P_+VDDQ_CS_10
P_+VDDQ_VDD_20
PR45 100KOhm
PC43 2200PF/50V /X
IOCP=10.4A
PC44 2.2UF/16V mbs_c0603
PR51 2.2Ohm mbs_r0603
+5VSUS
+12VSUS
VIN +12V
Imax_in = 1.0A
PQ16 NTMFS4C09NBT1G
PQ17 NTMFS4C06NBT1G
PC34 0.1UF/25V mbs_c0603
PC35 10UF/25V mbs_c0805
PC36 10UF/25V mbs_c0805
PL3 1.5UH
Irat=10A
DCR=10.6mOHM
PC41 2200PF/50V mbs_c0603
P_+VDDQ_SNB_20
PR46 1Ohm mbs_r1206
PC39 22UF/6.3V mbs_c0805
PC40 22UF/6.3V mbs_c0805
Imax = 8A
+VDDQ
ESR 9mOHM
PCE4 470uF/2V
PJP5 SHORTPIN /X
PR47 0Ohm /X
20,27,52,73 S_SLPS3#
PR48 10KOhm
PR50 10KOhm
73 P_+VTT_EN_10
52 P_+VDDQ_EN_10
P_+VTT_EN_10
P_+VDDQ_EN_10
P_+VDDQ_TON_10
FSW=325KHZ
PR53 820KOhm
70 P_+VDDQ_PG_10
P_+VDDQ_PG_10
PR55 10KOhm
PC46 1000PF/50V
PC47 1000PF/50V
12,20,52,73 S_SLPS4#
S_SLPS4#
PR56 10KOhm /X
P_+VDDQ_EN_10
PD2 BAT54CW /X
P_+VDDQ_FB_R_10
PR49 0Ohm
PR52 12KOhm
PC45 68PF/50V
P_+VDDQ_FB_10
PR54 20KOhm
GND
ASUSTek COMPUTER INC.
Title : +VDDQ&+VPPDDR
Engineer: IPC-EE3
Size B
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
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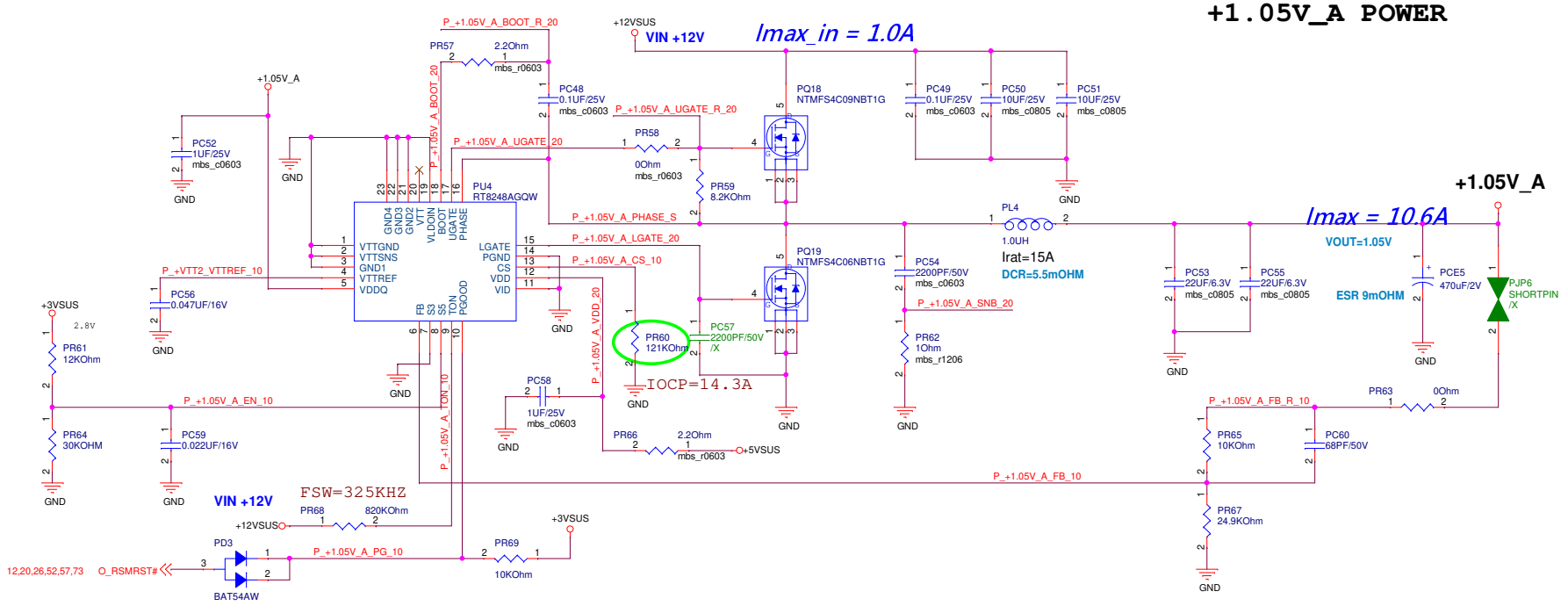
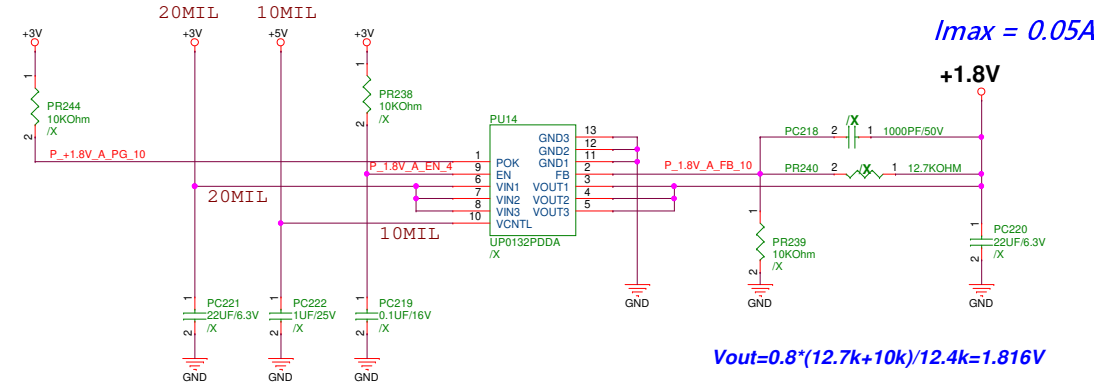
+1.05V_A POWER



+1.8V POWER

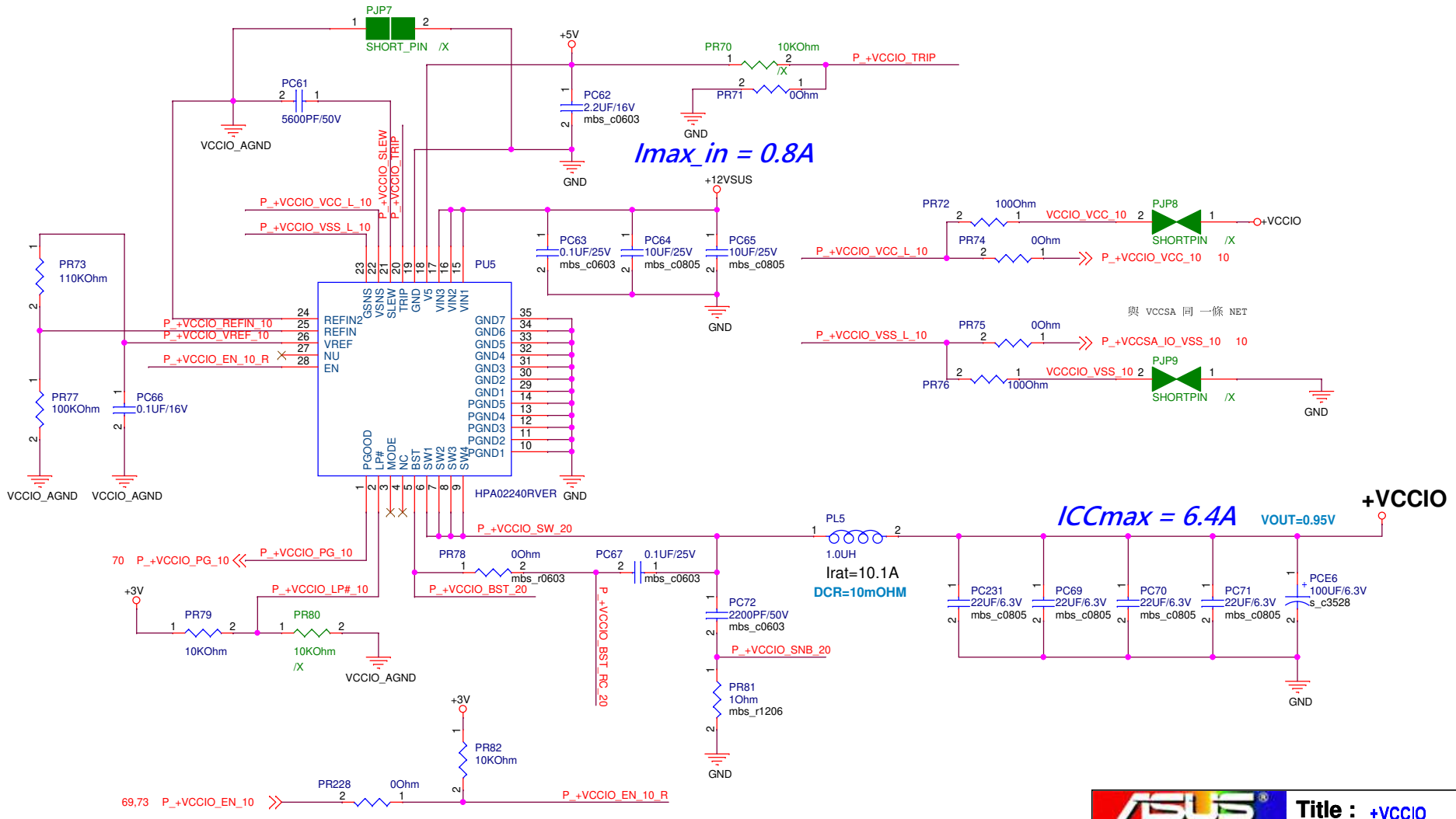
1.8V allowed to ramp first with no limit; only requirement is it must ramp after VccRTC



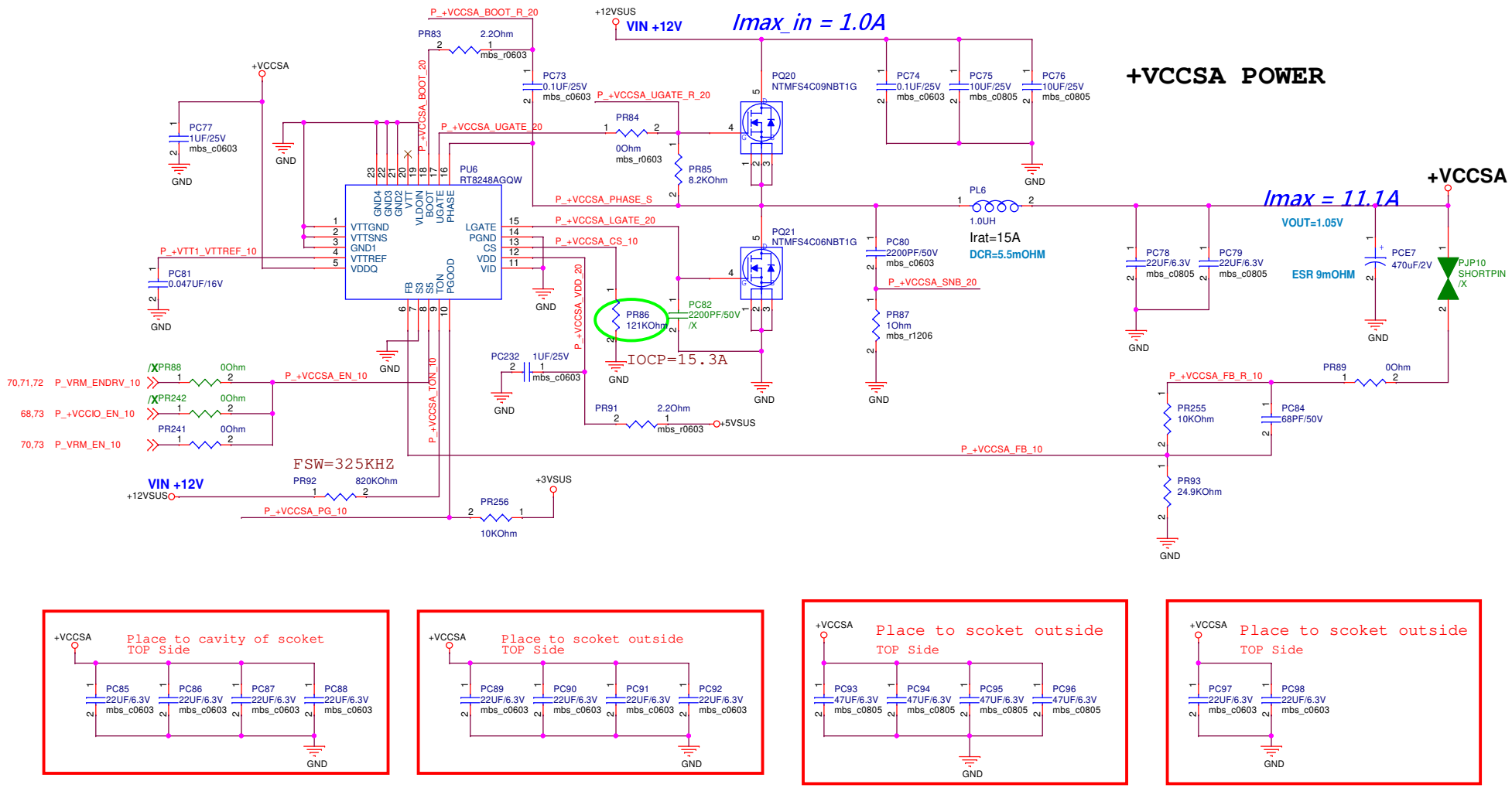
Vout=0.8*(12.7k+10k)/12.4k=1.816V

ASUS	Title : +1.05V_A//+1.8V	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 67 of 75	

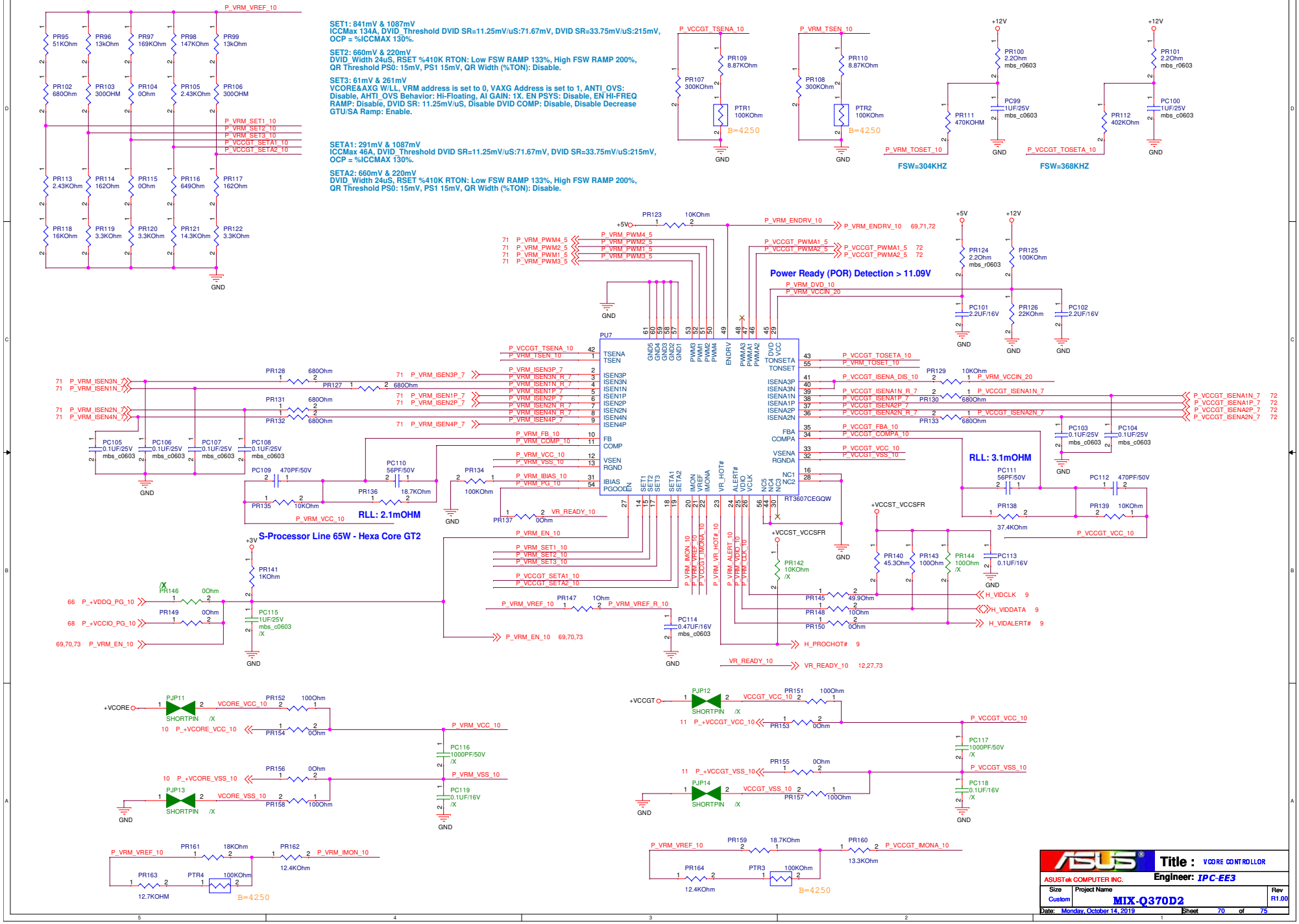
+VCCIO POWER



ASUSTek COMPUTER INC.	Title : +VCCIO	Engineer: IPC-EE3
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.00
Date: Monday, October 14, 2019	Sheet 68 of 75	



ASUS	Title : +VCCSA	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 69 of 75	


SET1: 841mV & 1087mV
ICCMax 134A, DVID_Threshold DVID SR=11.25mV/uS:71.67mV, DVID SR=33.75mV/uS:215mV, OCP = %ICCMAX 130%.
SET2: 660mV & 220mV
DVID_Width 24uS, RSET %410K RTON: Low FSW RAMP 133%, High FSW RAMP 200%, QR Threshold PS0: 15mV, PS1 15mV, QR Width (%TON): Disable.
SET3: 61mV & 261mV
VCORE&AXG W/LL, VRM address is set to 0, VAXG Address is set to 1, ANTI_OVS: Disable, AHTI_OVS Behavior: Hi-Floating, AI GAIN: 1X. EN PSYS: Disable, EN HI-FREQ RAMP: Disable, DVID SR: 11.25mV/uS, Disable DVID COMP: Disable, Disable Decrease GTU/SA Ramp: Enable.
SETA1: 291mV & 1087mV
ICCMax 46A, DVID_Threshold DVID SR=11.25mV/uS:71.67mV, DVID SR=33.75mV/uS:215mV, OCP = %ICCMAX 130%.
SETA2: 660mV & 220mV
DVID_Width 24uS, RSET %410K RTON: Low FSW RAMP 133%, High FSW RAMP 200%, QR Threshold PS0: 15mV, PS1 15mV, QR Width (%TON): Disable.
FSW=304KHZ
FSW=368KHZ
Power Ready (POR) Detection > 11.09V
RLL: 2.1mOHM
RLL: 3.1mOHM
S-Processor Line 65W - Hexa Core GT2
PU7
RT3607CEGQW
Title : VCORE CONTROLLOR
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
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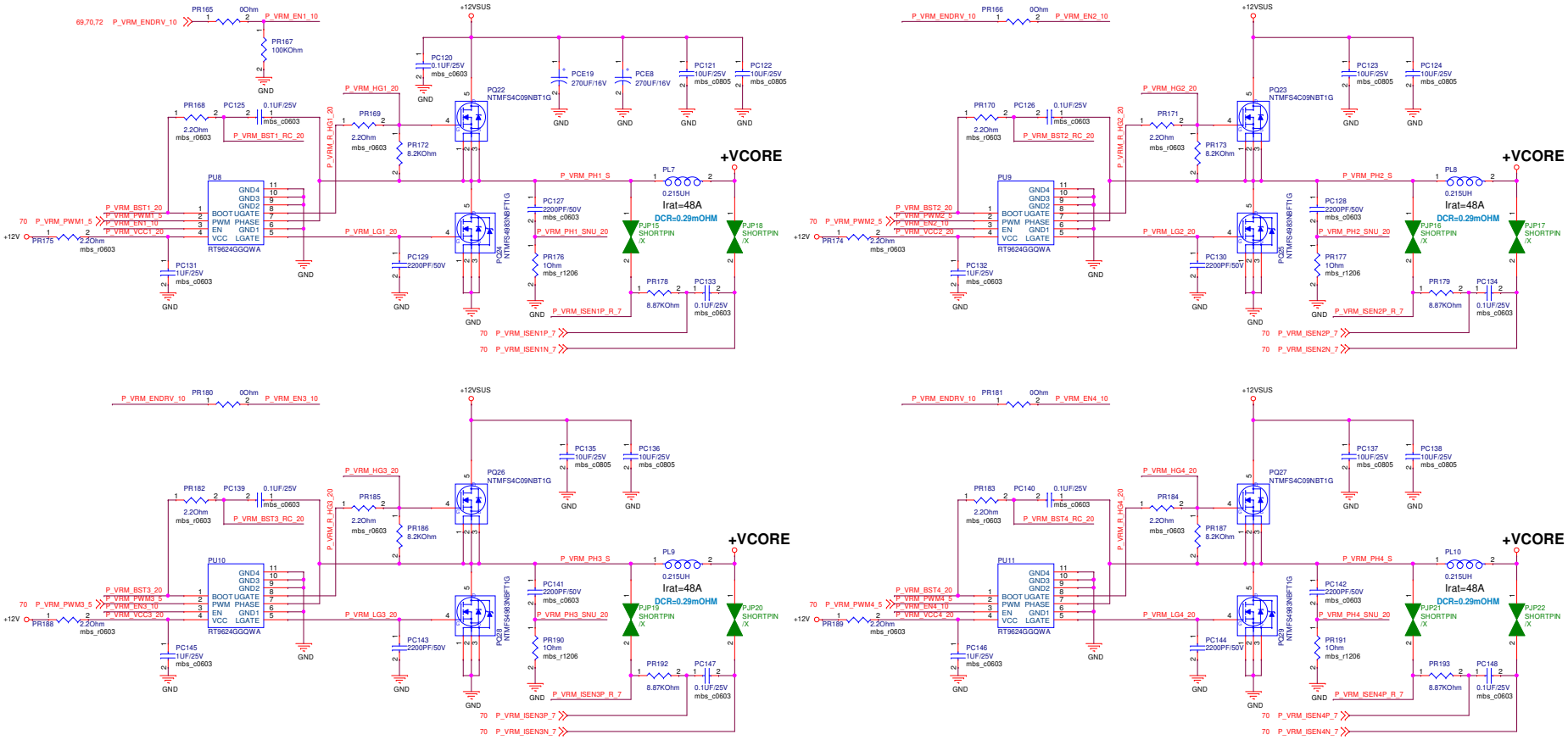
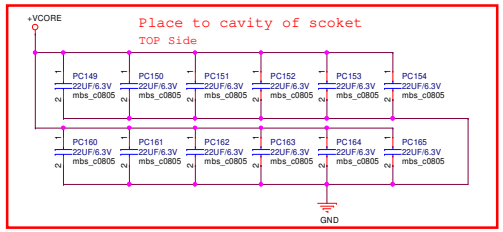
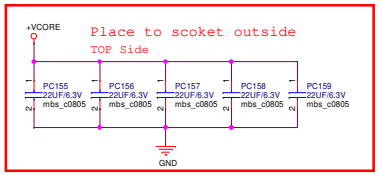
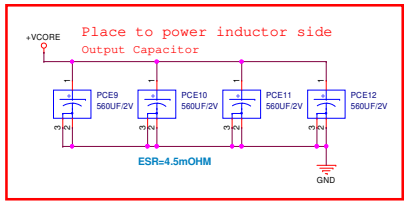
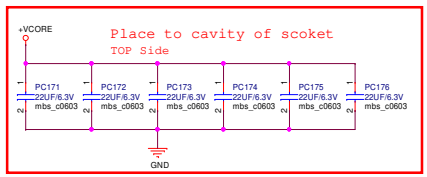
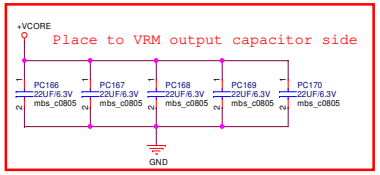




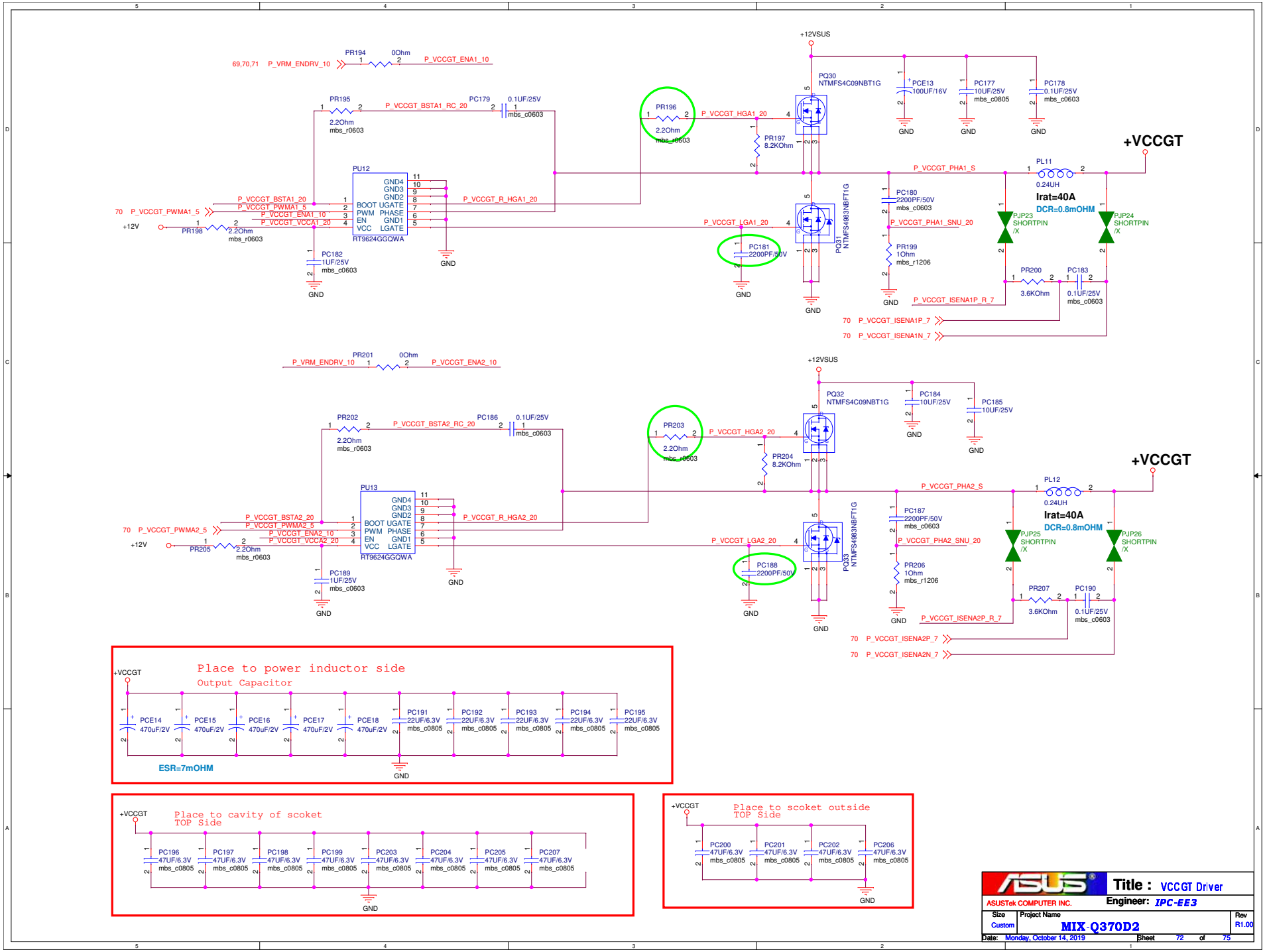








ASUSTeK COMPUTER INC.	Title : VCORE Driver		
	Engineer: IPC-EE3		
Size C	Project Name MIX-Q370D2		Rev R1.00
Date: Monday, October 14, 2019	Sheet 71 of 75		


+12VSUS
PR194 0Ohm
69,70,71 P_VRM_ENDRV_10
P_VCCGT_ENA1_10
PR195 2.2Ohm mbs_r0603
P_VCCGT_BSTA1_RC_20
PC179 0.1UF/25V mbs_c0603
PR196 2.2Ohm mbs_r0603
P_VCCGT_HGA1_20
PQ30 NTMFS4C09NBT1G
PR197 8.2KOhm
PCE13 100UF/16V
PC177 10UF/25V mbs_c0805
PC178 0.1UF/25V mbs_c0603
GND
+VCCGT
PU12
RT9624GGQWA
GND4 GND3 GND2 BOOT UGATE PWM PHASE EN GND1 VCC LGATE
P_VCCGT_BSTA1_20
P_VCCGT_PWMA1_5
P_VCCGT_ENA1_10
P_VCCGT_VCCA1_20
P_VCCGT_R_HGA1_20
70 P_VCCGT_PWMA1_5
+12V
PR198 2.2Ohm mbs_r0603
PC182 1UF/25V mbs_c0603
P_VCCGT_LGA1_20
PC181 2200PF/50V
PQ31 NTMFS4983NBFT1G
P_VCCGT_PHA1_S
PL11 0.24UH
Irat=40A
DCR=0.8mOHM
PC180 2200PF/50V mbs_c0603
P_VCCGT_PHA1_SNU_20
PR199 1Ohm mbs_r1206
PJP23 SHORTPIN /X
PJP24 SHORTPIN /X
PR200 3.6KOhm
PC183 0.1UF/25V mbs_c0603
P_VCCGT_ISENA1P_R_7
70 P_VCCGT_ISENA1P_7
70 P_VCCGT_ISENA1N_7
PR201 0Ohm
P_VRM_ENDRV_10
P_VCCGT_ENA2_10
PR202 2.2Ohm mbs_r0603
P_VCCGT_BSTA2_RC_20
PC186 0.1UF/25V mbs_c0603
PR203 2.2Ohm mbs_r0603
P_VCCGT_HGA2_20
PQ32 NTMFS4C09NBT1G
PR204 8.2KOhm
PC184 10UF/25V
PC185 10UF/25V
PU13
RT9624GGQWA
P_VCCGT_BSTA2_20
P_VCCGT_PWMA2_5
P_VCCGT_ENA2_10
P_VCCGT_VCCA2_20
P_VCCGT_R_HGA2_20
70 P_VCCGT_PWMA2_5
PR205 2.2Ohm mbs_r0603
PC189 1UF/25V mbs_c0603
P_VCCGT_LGA2_20
PC188 2200PF/50V
PQ33 NTMFS4983NBFT1G
P_VCCGT_PHA2_S
PL12 0.24UH
Irat=40A
DCR=0.8mOHM
PC187 2200PF/50V mbs_c0603
P_VCCGT_PHA2_SNU_20
PR206 1Ohm mbs_r1206
PJP25 SHORTPIN /X
PJP26 SHORTPIN /X
PR207 3.6KOhm
PC190 0.1UF/25V mbs_c0603
P_VCCGT_ISENA2P_R_7
70 P_VCCGT_ISENA2P_7
70 P_VCCGT_ISENA2N_7
Place to power inductor side
Output Capacitor
PCE14 470uF/2V
PCE15 470uF/2V
PCE16 470uF/2V
PCE17 470uF/2V
PCE18 470uF/2V
PC191 22UF/6.3V mbs_c0805
PC192 22UF/6.3V mbs_c0805
PC193 22UF/6.3V mbs_c0805
PC194 22UF/6.3V mbs_c0805
PC195 22UF/6.3V mbs_c0805
ESR=7mOHM
Place to cavity of scoket
TOP Side
PC196 47UF/6.3V mbs_c0805
PC197 47UF/6.3V mbs_c0805
PC198 47UF/6.3V mbs_c0805
PC199 47UF/6.3V mbs_c0805
PC203 47UF/6.3V mbs_c0805
PC204 47UF/6.3V mbs_c0805
PC205 47UF/6.3V mbs_c0805
PC207 47UF/6.3V mbs_c0805
Place to scoket outside
TOP Side
PC200 47UF/6.3V mbs_c0805
PC201 47UF/6.3V mbs_c0805
PC202 47UF/6.3V mbs_c0805
PC206 47UF/6.3V mbs_c0805
Title : VCCGT Driver
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
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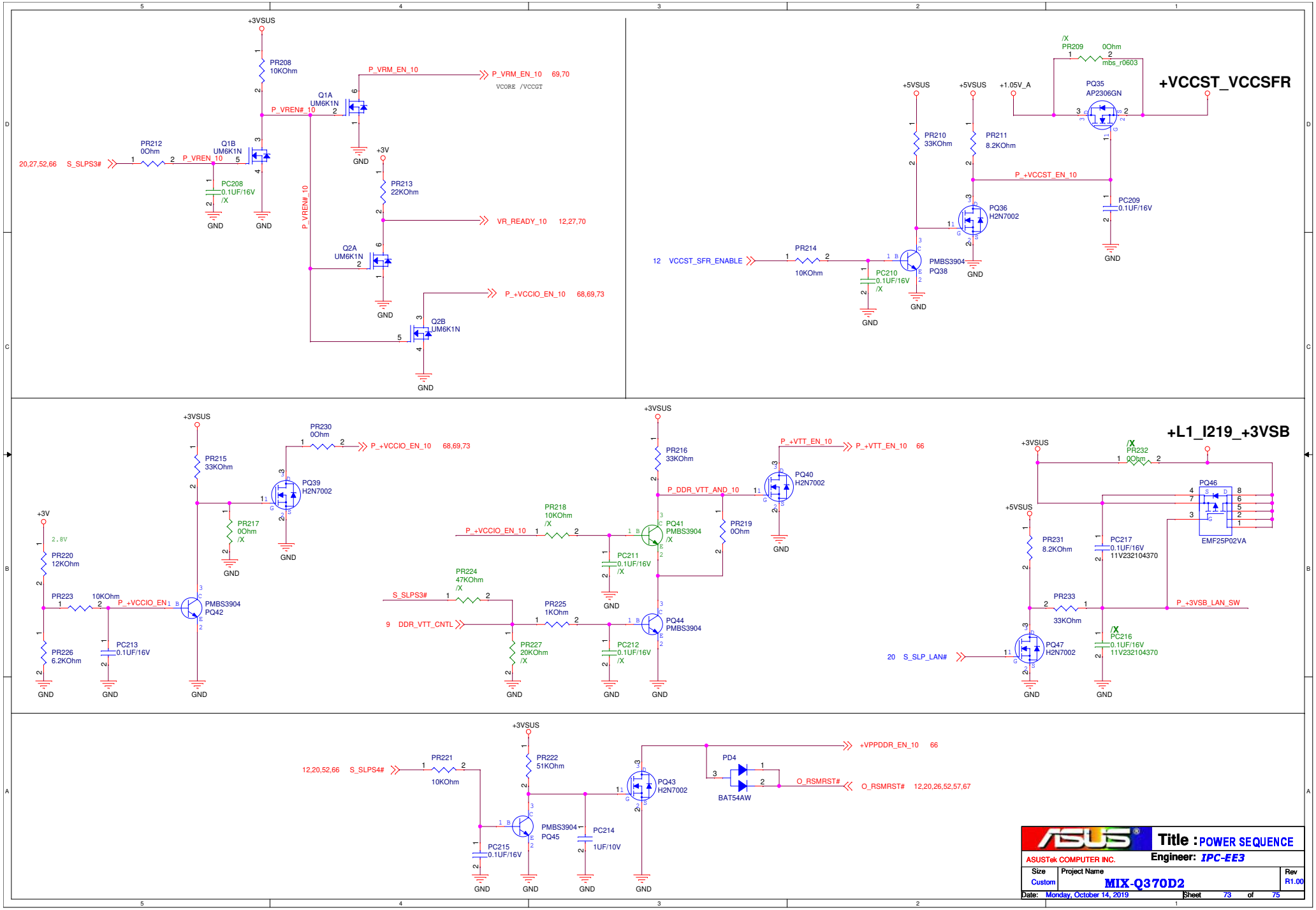
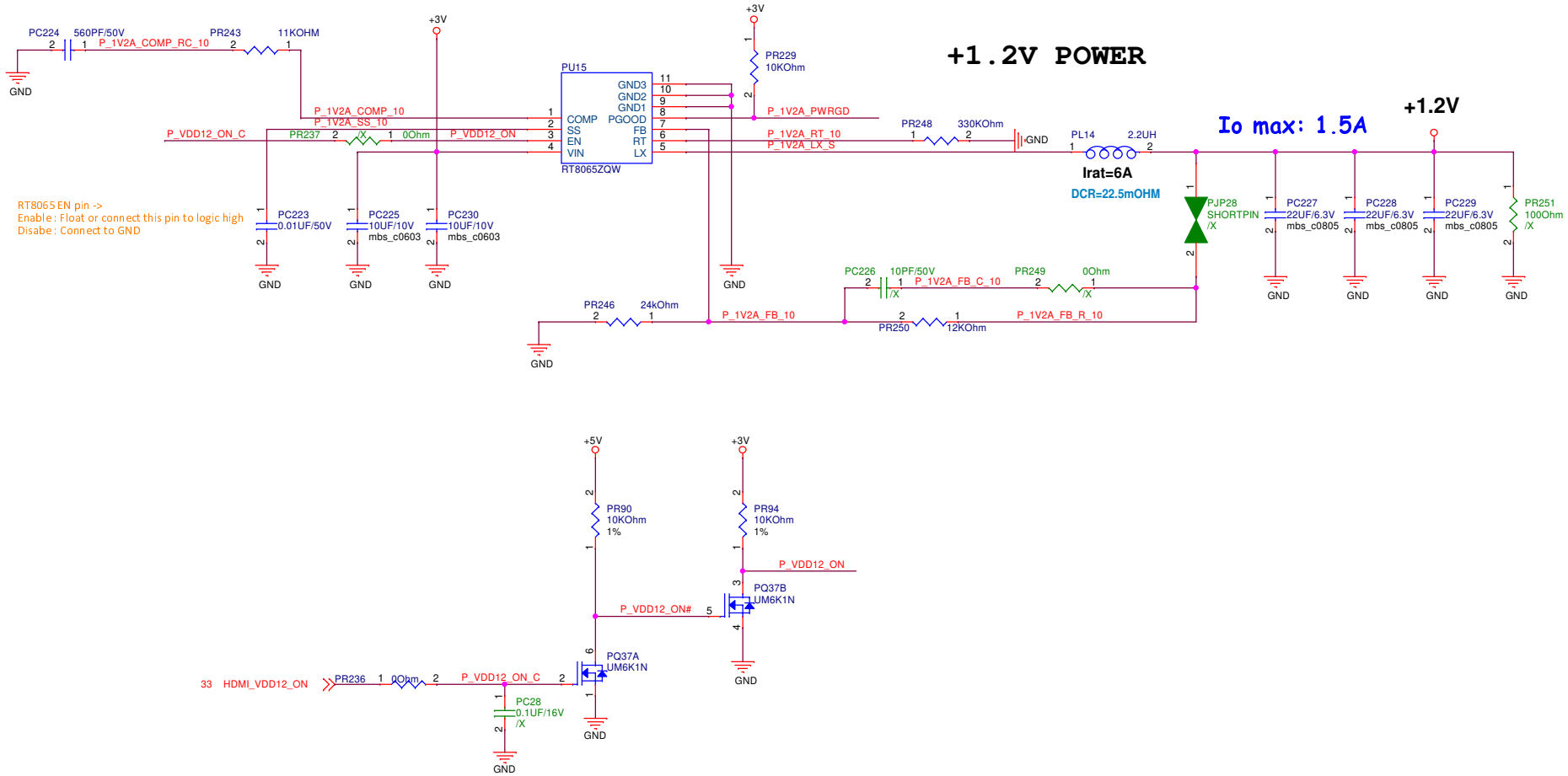

+VCCST_VCCSFR
+L1_I219_+3VSB
+3VSUS
PR208 10KOhm
P_VRM_EN_10
P_VRM_EN_10 69,70
VCORE /VCCGT
Q1A UM6K1N
P_VREN#_10
PR212 0Ohm
Q1B UM6K1N
20,27,52,66 S_SLPS3#
PC208 0.1UF/16V /X
GND
+3V
PR213 22KOhm
VR_READY_10 12,27,70
Q2A UM6K1N
P_+VCCIO_EN_10 68,69,73
Q2B UM6K1N
/X PR209 0Ohm mbs_r0603
+5VSUS
+1.05V_A
PQ35 AP2306GN
PR210 33KOhm
PR211 8.2KOhm
P_+VCCST_EN_10
PQ36 H2N7002
PC209 0.1UF/16V
12 VCCST_SFR_ENABLE
PR214 10KOhm
PMBS3904 PQ38
PC210 0.1UF/16V /X
PR230 0Ohm
PR215 33KOhm
PQ39 H2N7002
PR217 0Ohm /X
2.8V
PR220 12KOhm
PR223 10KOhm
P_+VCCIO_EN1
PMBS3904 PQ42
PR226 6.2KOhm
PC213 0.1UF/16V
PR216 33KOhm
P_+VTT_EN_10
P_+VTT_EN_10 66
P_DDR_VTT_AND_10
PQ40 H2N7002
PR218 10KOhm /X
PQ41 PMBS3904 /X
PR219 0Ohm
PC211 0.1UF/16V /X
PR224 47KOhm /X
S_SLPS3#
PR225 1KOhm
9 DDR_VTT_CNTL
PQ44 PMBS3904
PR227 20KOhm /X
PC212 0.1UF/16V /X
/X PR232 0Ohm
PQ46 EMF25P02VA
PR231 8.2KOhm
PC217 0.1UF/16V 11V232104370
PR233 33KOhm
P_+3VSB_LAN_SW
20 S_SLP_LAN#
PQ47 H2N7002
/X PC216 0.1UF/16V 11V232104370
12,20,52,66 S_SLPS4#
PR221 10KOhm
PR222 51KOhm
PQ43 H2N7002
+VPPDDR_EN_10 66
PD4 BAT54AW
O_RSMRST#
O_RSMRST# 12,20,26,52,57,67
PMBS3904 PQ45
PC214 1UF/10V
PC215 0.1UF/16V
ASUS
Title : POWER SEQUENCE
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.00
Date: Monday, October 14, 2019
Sheet 73 of 75



ASUS	Title : +1.2V	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.00
Date: Monday, October 14, 2019	Sheet 74 of 75	

History 2019/07/29 R1.00

01) change HDMI LSPCON IC to Protocol Converter IC at p.51
(intel only support one LSPCON IC)

History 2019/07/31

01) change PS185 to MB symbol & part at p.51
02) change LSPCON IC to PS175 for RVL at p.33
03) short GPIO5 & TMDS_CFG1 for IC Power saving at p.51
04) reserve 0ohm at HDMI CLKP/N, p.51
05) GR43 change to reserve & reserve PH at GPIO4, p.51
06) add 0.22uF at S_HDMI_D_HPD, p.51
07) change Board ID to PCH GPP_K8~K10 at p.19
08) add eDP/LVDS backlight control select at PCH GPP_K11, p.19
09) unmount PCH I2C port PH resister due to un-used at p.24
10) modfiy Power at p.4, 65, 70~74

History 2019/08/06

01) reserve I2C debug port, unmount GR45 and PH/PD at TMDS_CFG1 at PS185, P.51
02) modify HDMI2_PD# and reserve HDMI2_EQ1 to GND at PS185, P.51
03) add 1kohm at S_HDMI_D_HPD path and reserve 0.22uF at S_HDMI_C_HPD, P.33, 51
04) add ATX_PSON# to USB2_9 at p.48
05) modify SATA Connector No. and add /TPM option at p.29, 43
06) change GR23/GR24 to 10kohm and reserve I2C PH at p.33
07) change Power MOS from AP2306GN to PJA3406 for reliability risk at p.28, 32, 33, 51
08) delete +1.8V at p.25, 67
09) modify +1.2V EN to HDMI_VDD12_ON and change PS175 power bead at p.33, 74
10) Add external +1.2V for separate PS175/PS185 power at p.51

History 2019/08/07

01) Mount SR200 for Intel SPEC at p.17
02) remove PCH I2C PH res. due to unused at p.24
03) remove M2 SMBus 0ohm and change MOS package at p.25, 49
04) change MOS package at p.27, 31, 32, 50, 55
05) modify PS175/PS185 power bead & Cap. at p.33, 51
06) change USB power cap. from DIP to 3528 size at p.44, 45, 46, 47, 48
07) reserve 0ohm at +1.2V enable pin at p.74
08) modify CPU CFG setting and remove un-used PH at p.9

History 2019/08/08

01) remove USB2_9 at p.1, 18, 48
02) remove COM2 at p.1, 52, 55, 57
03) remove LVDS at p.1, 17, 18, 19, 34, 52
04) add +1.8V at p.25, 67
05) remove AAFP at p.1, 35, 36
06) change BIOS ROM & Buzzer to small package at p.28, 54
07) change HDMI2.0 optional to HDMI1.4 with Cost Reduced Level Shifter at p.1, 6, 21, 51

History 2019/09/02

01) correct un-used net to NC at p.33, 51
02) change HR104, HR215, SR96, SR35, SR94, SR30, D5, PD2, UF302, UF303, UF304, UF305, UF306, UF309 for 不建議用料 at p.9, 10, 20, 24, 25, 44-48, 66
03) modify CPU socket P/N at p.5~11
04) modify USB2.0 port for one internal header at p.18, 46, 48

History 2019/09/17

01) change +5VSUS to small package at p.65
02) change DC Jack at p.65

History 2019/09/23

01) change PCIex16 +12V DIP cap. (270UF/16V) to 2*poscap (100UF/16V) at p.30
02) add AAFP at p.1, 35, 36
03) change COM1 to SMT type Con. at p.55
04) modify description at p.1, 2, 3, 16, 18, 22
05) add 1UF/10V at +VCCPLL_OC p.10
06) add DIMM select resistor at p.13, 14
07) add net name "USB2_ID" at p.18
08) delete un-used TP at p.6, 9, 10, 19, 20, 21, 52
09) move SPI resistor after switch at p.28
10) add GND for eDP Con. at p.34
11) modfiy eDP HPD PD 100kohm to PCH side at p.34
12) mount HDMI_2 TMDS PH resistor at p.51
13) reserve +1.8V path for CNVi at p.22
14) change USB2.0 Power fuse to 1.75A at p.47, 48
15) modify i211 LAN ESD Power to +3V_AUX at p.42
16) mount SR145 for intel DG request at p.21
17) unmount SR146/SR175/SR478/SR477 for un-used at p.21, 25
18) reserve EMI solution for eDP signal at p.34
19) change SR128 to 8.2kohm for Power sequence at p.27
20) remove 0ohm at DP power p.32
21) change cap. footprint at p.32, 34
22) L1R21/L1R22 change to 4.7kohm follow i219 CRB at p.39

History 2019/09/24

01) delete AAFP and chang audio IC symbol at p.35, 36
02) change COM port termination jumper pckage at p.55
03) change AR24 to 47kohm at p.38 (follow MAX-Q370B)
04) delete eDP ESD at p.34
05) change audio power +3VSUS to +3V at p.35
06) add two 0.1uf cap. at GND/A_GND p.36, 38
07) reserve 0ohm for XTAL fine tune at p.39
08) change PCIe cap. type at p.39
09) change PCIex16 +12V 2*poscap (100UF/16V) to DIP cap. (270UF/16V) at p.30

History 2019/09/27

01) swap HDMI Port D GD1/GD2 for layout request at p.51
02) un-mount +1.8V and L2R7/L2R9/L2R10 for reserve at p.67
03) modify Audio Power design at p.35, 36
04) add 0ohm for GND/AGND connection at p.38
05) delete GPP_K0~K7 for un-used and reserve eDP panel ID at p.19

History 2019/09/27v2

01) swap DP/HDMI GD13/GD100/GD101 for layout request at p.32, 33

History 2019/10/02

01) swap HDMI/DP/USB Choke, ESD at p.33, 32, 44~47, 51

History 2019/10/03

01) swap USB Choke, ESD at p.44, 46

History 2019/10/14

01) modify USB2_5678 Power net name at p.47