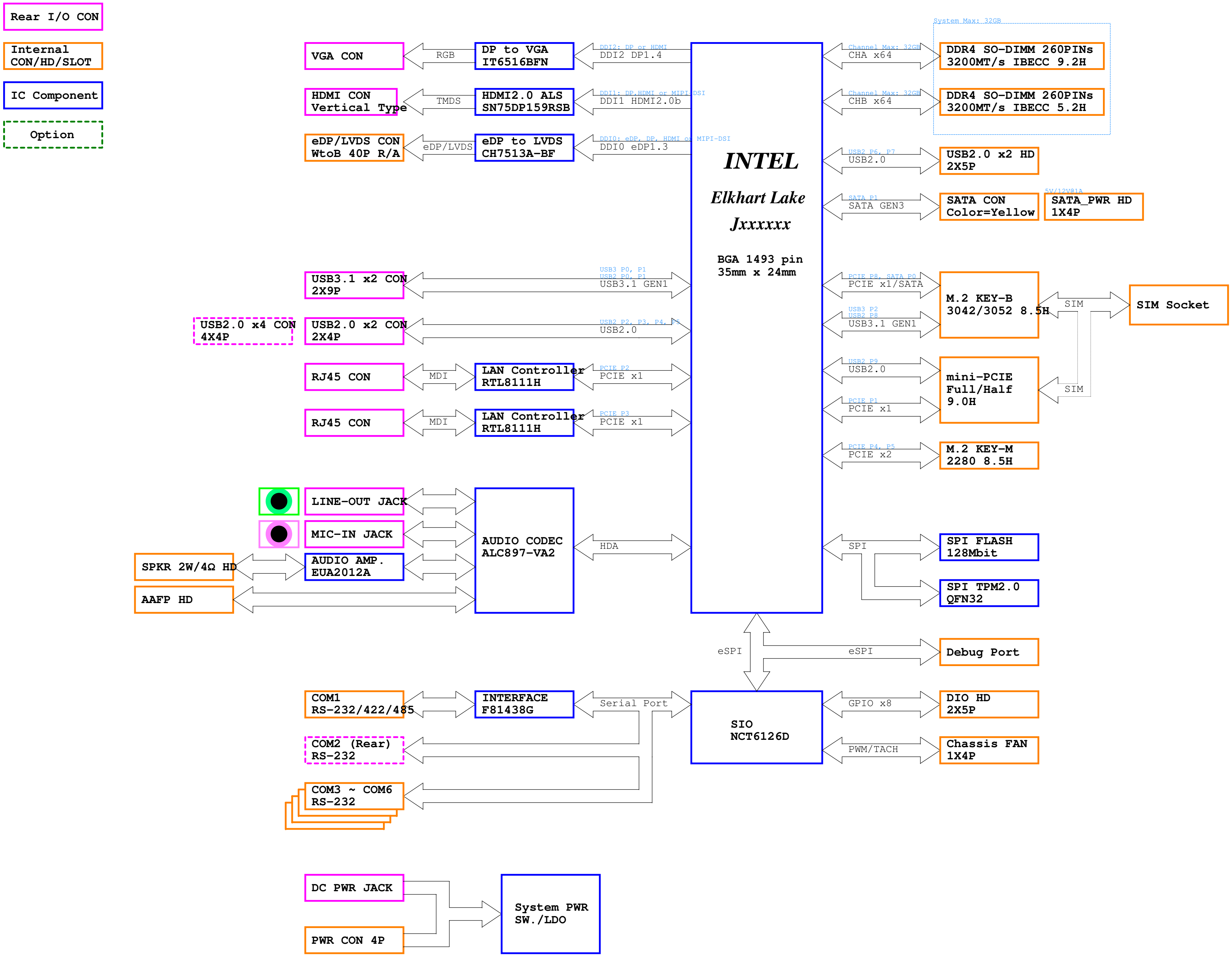
COVER PAGE

Model Name: MIX-EHLD1 R1.01

BLOCK DIAGRAM



ASUSTek COMPUTER INC.

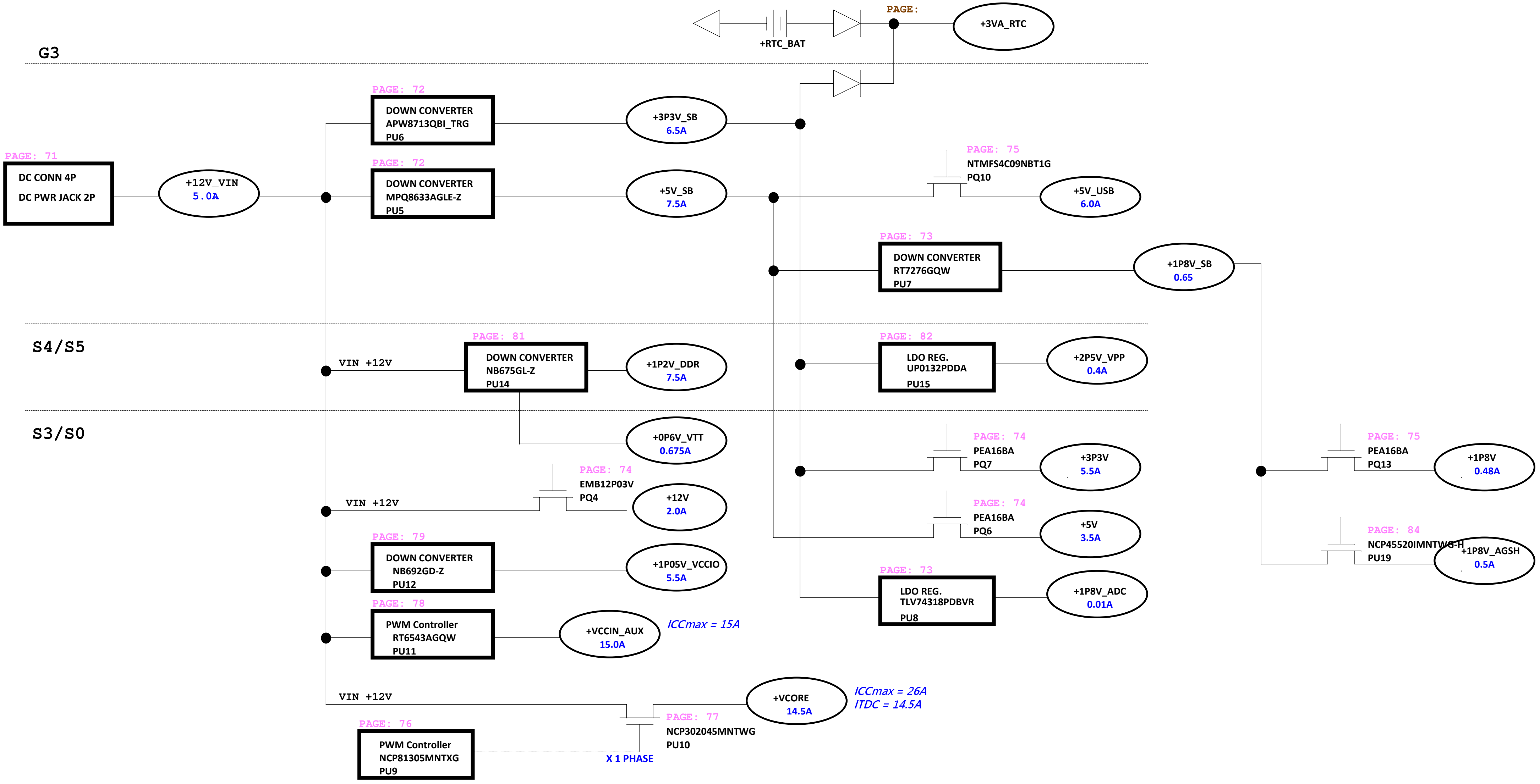
Title : BLOCK DIAGRAM

Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 2 of 90

POWER FLOW



ASUSTek COMPUTER INC.

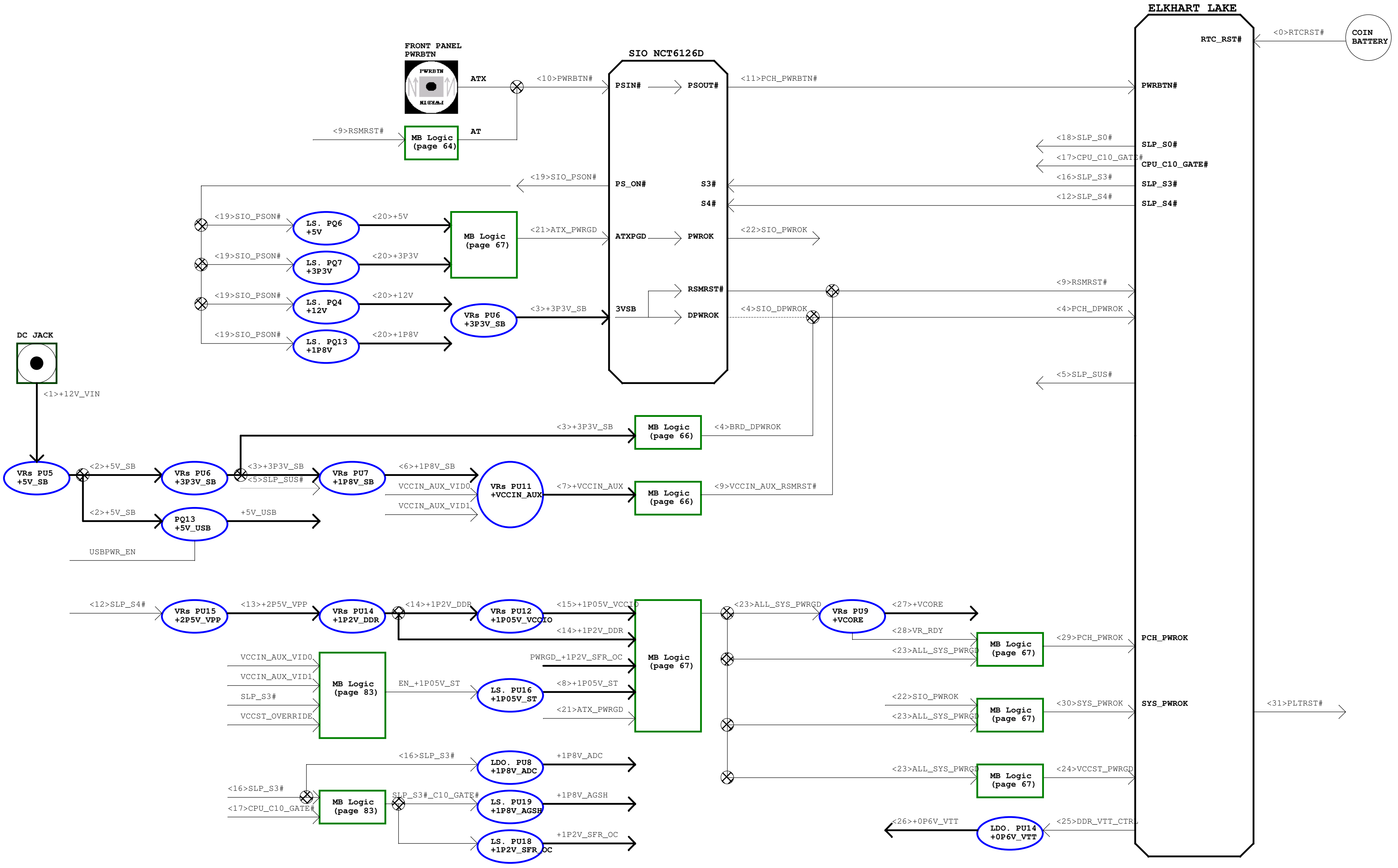
Title : POWER FLOW

Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 3 of 90

POWER SEQUENCE



Title : POWER SEQUENCE

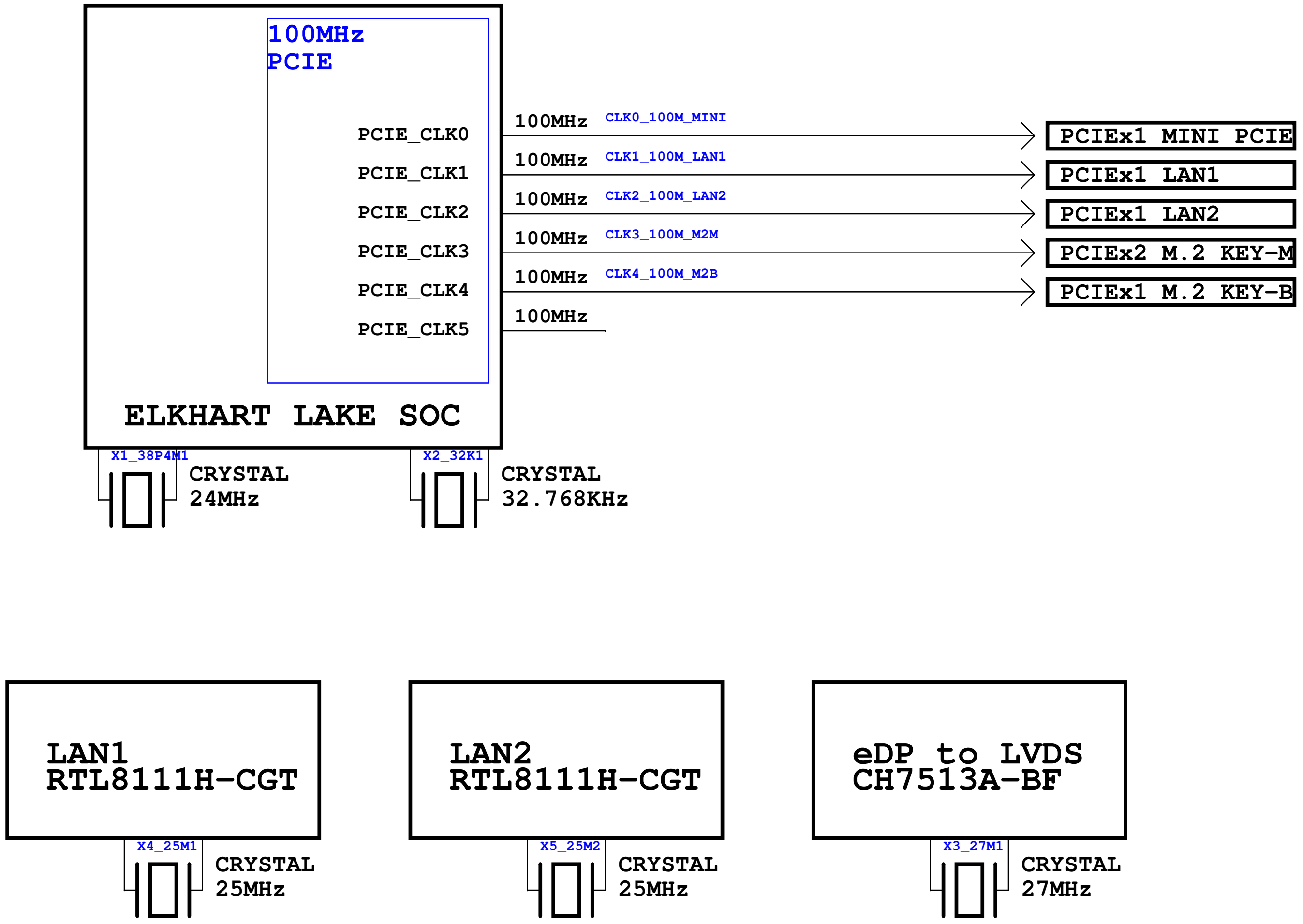
ASUSTek COMPUTER INC.
Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 4 of 90

Title : xxx		
ASUSTek COMPUTER INC.	**Engineer:** Shawn Yu	
Size A2	Project Name **MIX-EHLD1**	Rev R1.01
Date: Thursday, July 15, 2021	Sheet 5 of 90	

CLOCK DISTRIBUTION



ASUSTek COMPUTER INC.

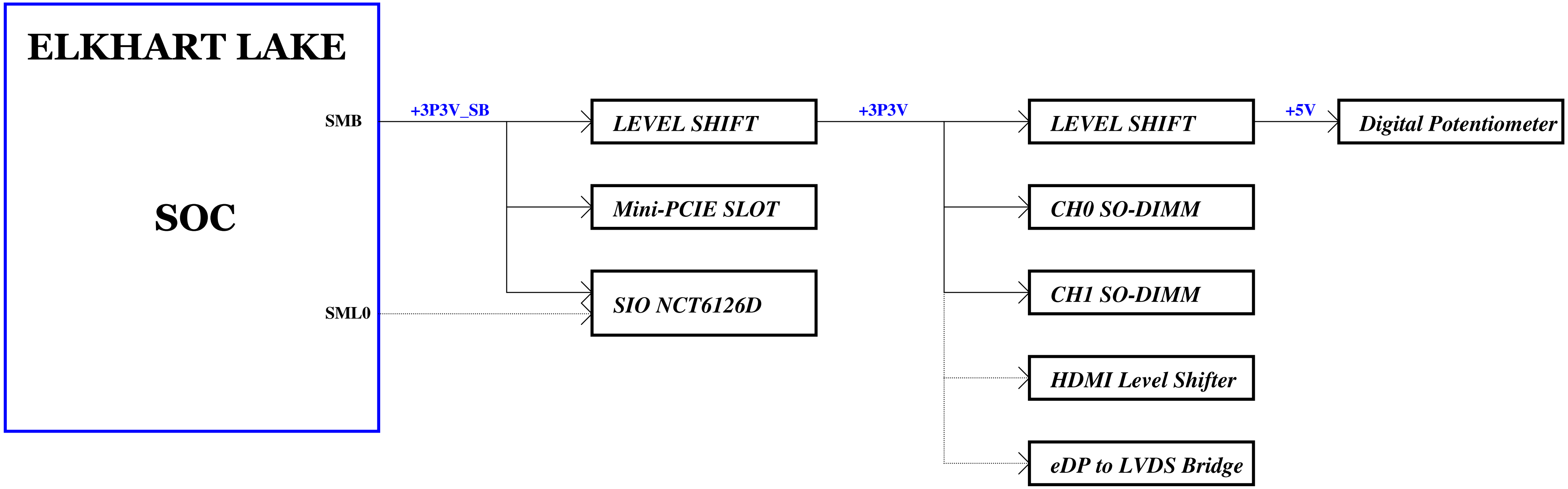
Title : CLOCK DISTRIBUTION

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 6 of 90

SMBUS MAP



ASUSTek COMPUTER INC.

Title : SMBUS MAP

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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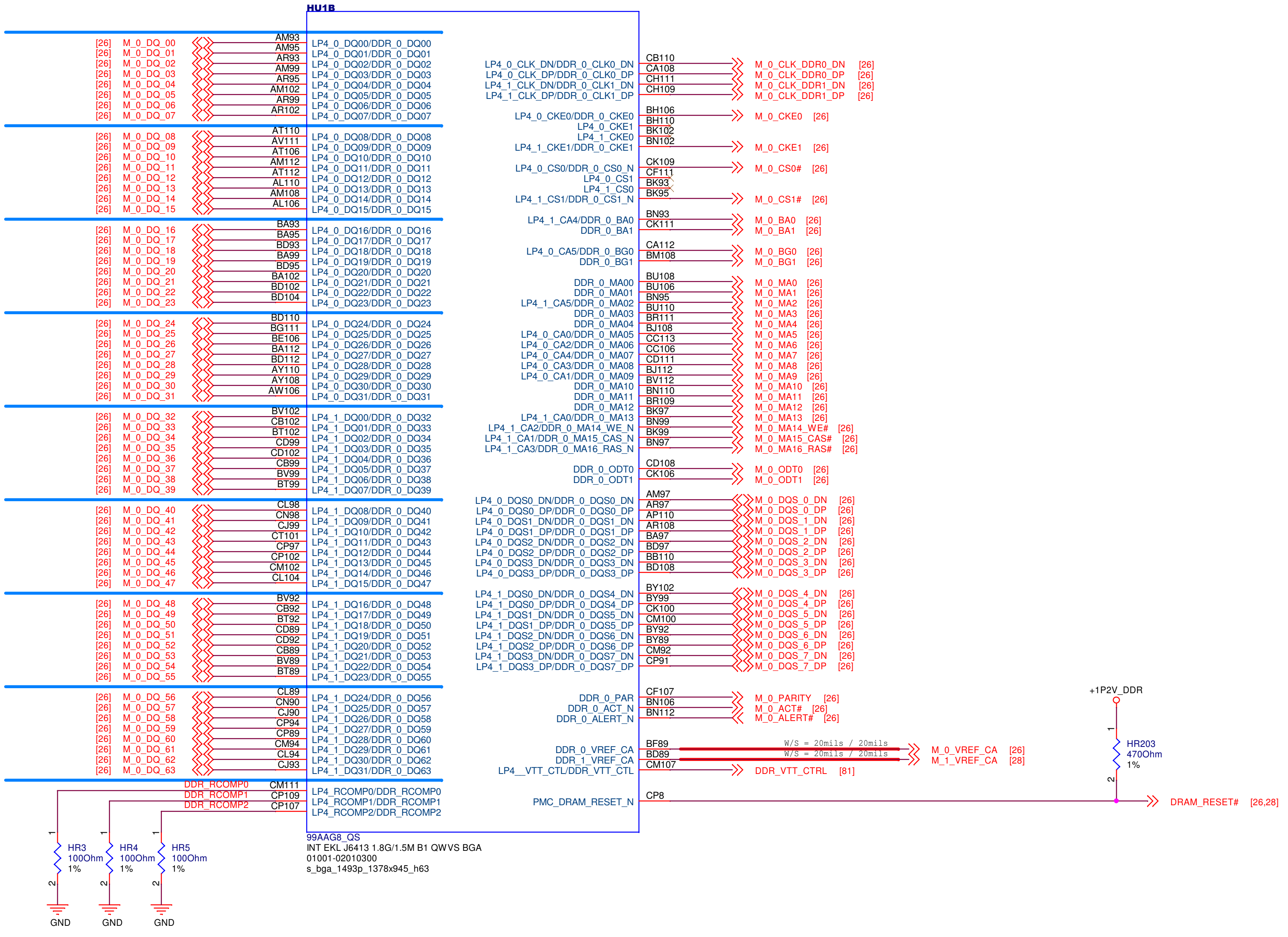
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DDR_RCOMP2 CP107 LP4_RCOMP2/DDR_RCOMP2
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HR4 100Ohm 1%
HR5 100Ohm 1%
1
2
GND
GND
GND
99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
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HR203 470Ohm 1%

ASUSTek COMPUTER INC.

Title : CPU DDR4 CH0

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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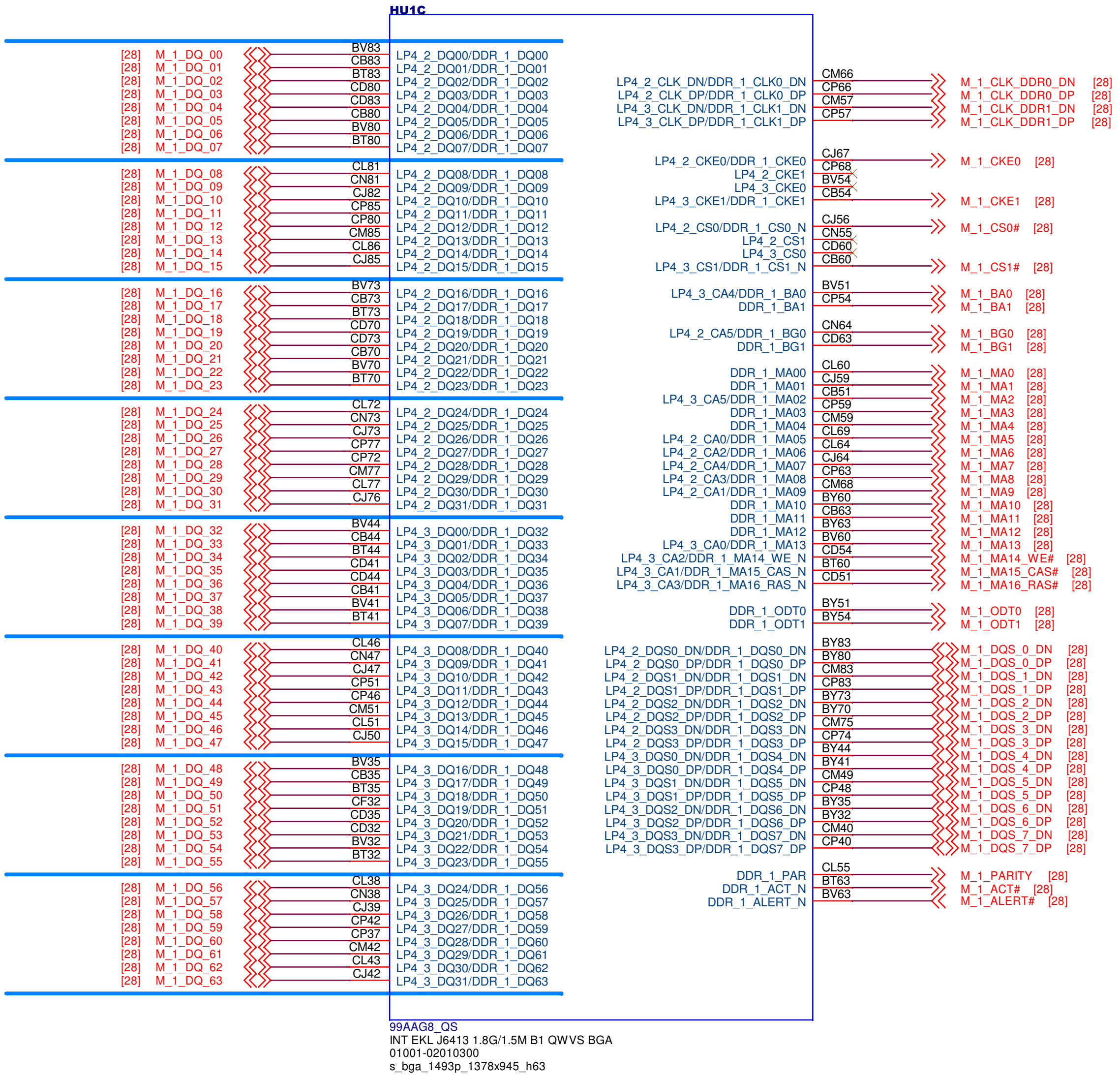
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DDR_1_MA01 CJ59 M_1_MA1 [28]
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DDR_1_MA04 CM59 M_1_MA4 [28]
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DDR_1_MA11 CB63 M_1_MA11 [28]
DDR_1_MA12 BY63 M_1_MA12 [28]
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LP4_3_DQS0_DP/DDR_1_DQS4_DP BY41 M_1_DQS_4_DP [28]
LP4_3_DQS1_DN/DDR_1_DQS5_DN CM49 M_1_DQS_5_DN [28]
LP4_3_DQS1_DP/DDR_1_DQS5_DP CP48 M_1_DQS_5_DP [28]
LP4_3_DQS2_DN/DDR_1_DQS6_DN BY35 M_1_DQS_6_DN [28]
LP4_3_DQS2_DP/DDR_1_DQS6_DP BY32 M_1_DQS_6_DP [28]
LP4_3_DQS3_DN/DDR_1_DQS7_DN CM40 M_1_DQS_7_DN [28]
LP4_3_DQS3_DP/DDR_1_DQS7_DP CP40 M_1_DQS_7_DP [28]
DDR_1_PAR CL55 M_1_PARITY [28]
DDR_1_ACT_N BT63 M_1_ACT# [28]
DDR_1_ALERT_N BV63 M_1_ALERT# [28]
99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
s_bga_1493p_1378x945_h63

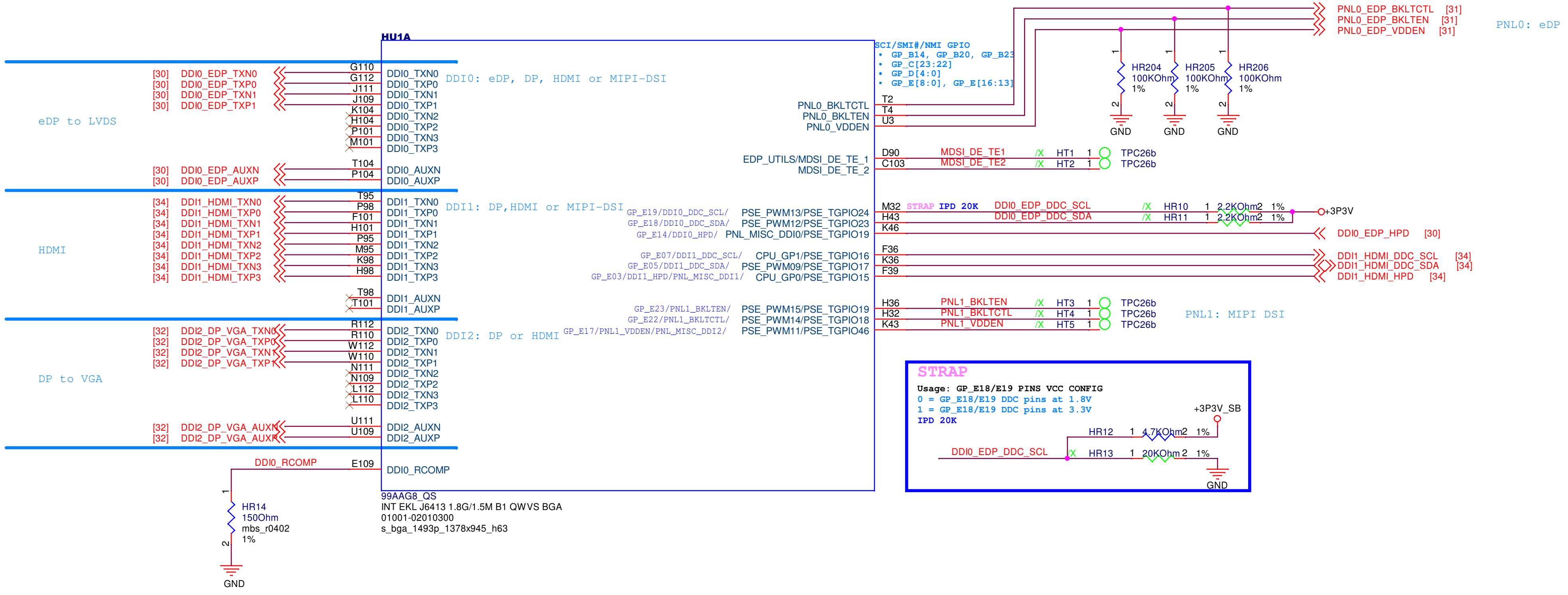
Title : CPU DDR4 CH1

ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 9 of 90



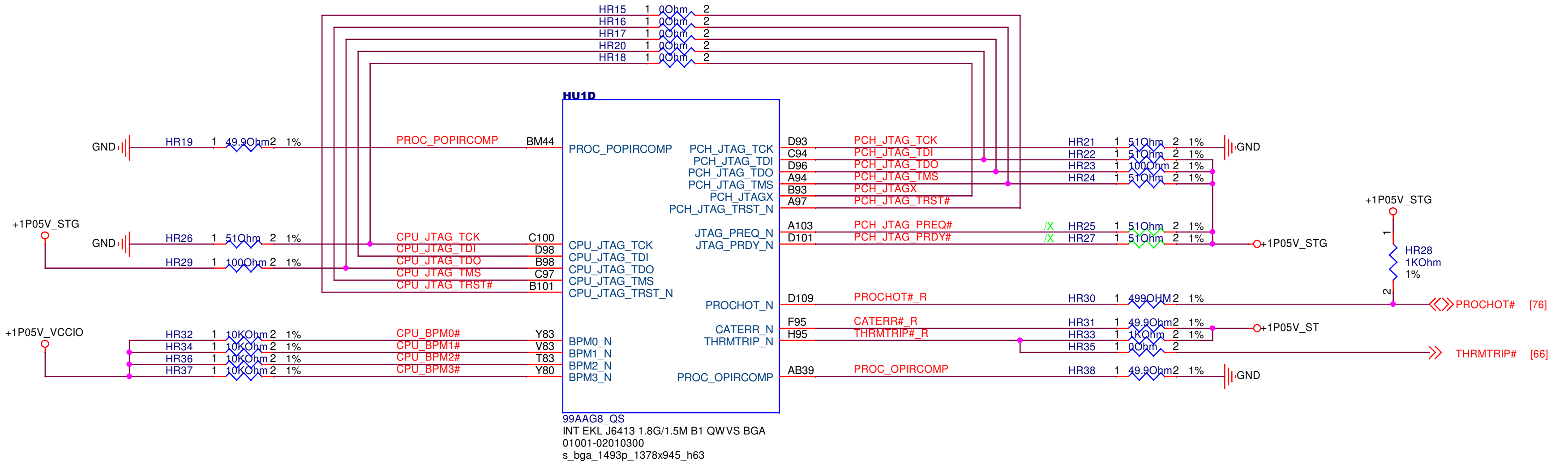
ASUSTek COMPUTER INC.

Title : CPU DDI

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 10 of 90



ASUSTek COMPUTER INC.

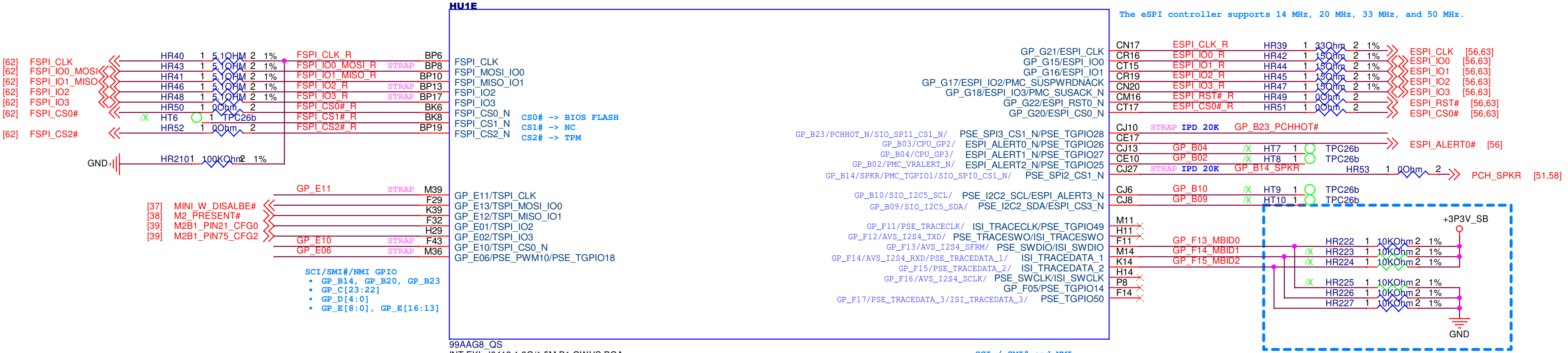
Title : CPU JTAG BPM

Engineer: Shawn Yu

Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

Date: Thursday, July 15, 2021 Sheet 11 of 90

GPIO Disabling and Termination Guidelines
When GPIO interface is not implemented on the platform, the signal pin(s)
may be left unterminated, but should not be configured as GPI's.


HU1E
[62] FSPI_CLK
[62] FSPI_IO0_MOSI
[62] FSPI_IO1_MISO
[62] FSPI_IO2
[62] FSPI_IO3
[62] FSPI_CS0#
[62] FSPI_CS2#
HR40 1 5.1OHM 2 1%
HR43 1 5.1OHM 2 1%
HR41 1 5.1OHM 2 1%
HR46 1 5.1OHM 2 1%
HR48 1 5.1OHM 2 1%
HR50 1 0Ohm 2
/X HT6 1 TPC26b
HR52 1 0Ohm 2
GND
HR2101 100KOhm 2 1%
FSPI_CLK_R
FSPI_IO0_MOSI_R STRAP
FSPI_IO1_MISO_R
FSPI_IO2_R STRAP
FSPI_IO3_R STRAP
FSPI_CS0#_R
FSPI_CS1#_R
FSPI_CS2#_R
BP6
BP8
BP10
BP13
BP17
BK6
BK8
BP19
FSPI_CLK
FSPI_MOSI_IO0
FSPI_MISO_IO1
FSPI_IO2
FSPI_IO3
FSPI_CS0_N
FSPI_CS1_N
FSPI_CS2_N
GP_E11 STRAP M39
[37] MINI_W_DISALBE# F29
[38] M2_PRESENT# K39
[39] M2B1_PIN21_CFG0 F32
[39] M2B1_PIN75_CFG2 H29
GP_E10 STRAP F43
GP_E06 STRAP M36
GP_E11/TSPI_CLK
GP_E13/TSPI_MOSI_IO0
GP_E12/TSPI_MISO_IO1
GP_E01/TSPI_IO2
GP_E02/TSPI_IO3
GP_E10/TSPI_CS0_N
GP_E06/PSE_PWM10/PSE_TGPIO18
GP_G21/ESPI_CLK
GP_G15/ESPI_IO0
GP_G16/ESPI_IO1
GP_G17/ESPI_IO2/PMC_SUSPWRDNACK
GP_G18/ESPI_IO3/PMC_SUSACK_N
GP_G22/ESPI_RST0_N
GP_G20/ESPI_CS0_N
GP_B23/PCHHOT_N/SIO_SPI1_CS1_N/ PSE_SPI3_CS1_N/PSE_TGPIO28
GP_B03/CPU_GP2/ ESPI_ALERT0_N/PSE_TGPIO26
GP_B04/CPU_GP3/ ESPI_ALERT1_N/PSE_TGPIO27
GP_B02/PMC_VRALERT_N/ ESPI_ALERT2_N/PSE_TGPIO25
GP_B14/SPKR/PMC_TGPIO1/SIO_SPI0_CS1_N/ PSE_SPI2_CS1_N
GP_B10/SIO_I2C5_SCL/ PSE_I2C2_SCL/ESPI_ALERT3_N
GP_B09/SIO_I2C5_SDA/ PSE_I2C2_SDA/ESPI_CS3_N
GP_F11/PSE_TRACECLK/ ISI_TRACECLK/PSE_TGPIO49
GP_F12/AVS_I2S4_TXD/ PSE_TRACESWO/ISI_TRACESWO
GP_F13/AVS_I2S4_SFRM/ PSE_SWDIO/ISI_SWDIO
GP_F14/AVS_I2S4_RXD/PSE_TRACEDATA_1/ ISI_TRACEDATA_1
GP_F15/PSE_TRACEDATA_2/ ISI_TRACEDATA_2
GP_F16/AVS_I2S4_SCLK/ PSE_SWCLK/ISI_SWCLK
GP_F05/PSE_TGPIO14
GP_F17/PSE_TRACEDATA_3/ISI_TRACEDATA_3/ PSE_TGPIO50
CN17 ESPI_CLK_R HR39 1 33Ohm 2 1% ESPI_CLK [56,63]
CR16 ESPI_IO0_R HR42 1 15Ohm 2 1% ESPI_IO0 [56,63]
CT15 ESPI_IO1_R HR44 1 15Ohm 2 1% ESPI_IO1 [56,63]
CR19 ESPI_IO2_R HR45 1 15Ohm 2 1% ESPI_IO2 [56,63]
CN20 ESPI_IO3_R HR47 1 15Ohm 2 1% ESPI_IO3 [56,63]
CM16 ESPI_RST#_R HR49 1 0Ohm 2 ESPI_RST# [56,63]
CT17 ESPI_CS0#_R HR51 1 0Ohm 2 ESPI_CS0# [56,63]
CJ10 STRAP IPD 20K GP_B23_PCHHOT#
CE17 ESPI_ALERT0# [56]
CJ13 GP_B04 /X HT7 1 TPC26b
CE10 GP_B02 /X HT8 1 TPC26b
CJ27 STRAP IPD 20K GP_B14_SPKR HR53 1 0Ohm 2 PCH_SPKR [51,58]
CJ6 GP_B10 /X HT9 1 TPC26b
CJ8 GP_B09 /X HT10 1 TPC26b
M11
H11
F11 GP_F13_MBID0
M14 GP_F14_MBID1
K14 GP_F15_MBID2
H14
P8
F14
+3P3V_SB
HR222 1 10KOhm 2 1%
/X HR223 1 10KOhm 2 1%
/X HR224 1 10KOhm 2 1%
/X HR225 1 10KOhm 2 1%
HR226 1 10KOhm 2 1%
HR227 1 10KOhm 2 1%
GND

The eSPI controller supports 14 MHz, 20 MHz, 33 MHz, and 50 MHz.

CS0# -> BIOS FLASH
CS1# -> NC
CS2# -> TPM

SCI/SMI#/NMI GPIO
- GP_B14, GP_B20, GP_B23
- GP_C[23:22]
- GP_D[4:0]
- GP_E[8:0], GP_E[16:13]

99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
s_bga_1493p_1378x945_h63

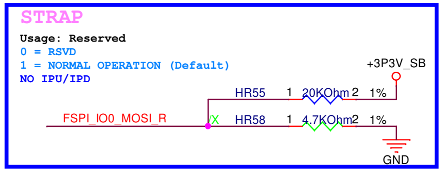
SCI / SMI# and NMI
- GP_B14, GP_B20, GP_B23
- GP_C[23:22]
- GP_D[4:0]
- GP_E[8:0], GP_E[16:13]

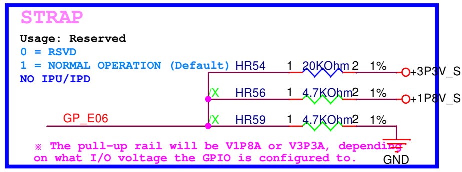
M/B ID

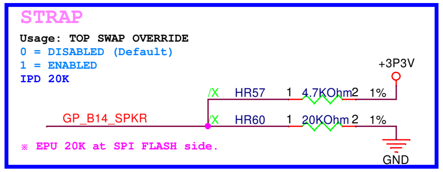
MBID2	MBID1	MBID0	Rev.
0	0	0	R1.00
0	0	1	R1.01
0	1	0	
0	1	1	

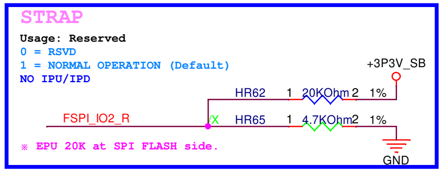
GSPI/TSPI Disable Guidelines:
SIO_SPI[2:0]
PSE_SPI[3:0]
TSPI

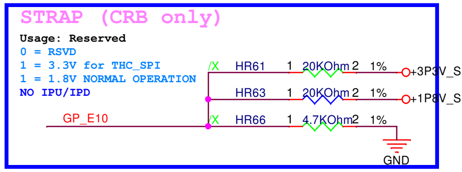
GSPI/TSPI signals are multiplexed with GPIOs and default to GPIO functionality.
If GSPI/TSPI interface is not used, the signals can be used as GPIOs instead.
If the GPIO functionality is also not used, the signals can be left as no-connect.

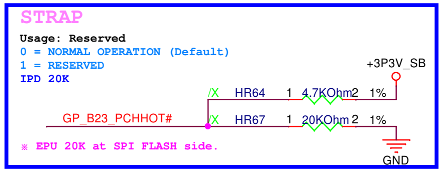

STRAP
Usage: Reserved
0 = RSVD
1 = NORMAL OPERATION (Default)
NO IPU/IPD

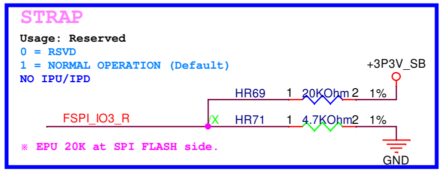

STRAP
Usage: Reserved
0 = RSVD
1 = NORMAL OPERATION (Default)
NO IPU/IPD
※ The pull-up rail will be V1P8A or V3P3A, depending on what I/O voltage the GPIO is configured to.

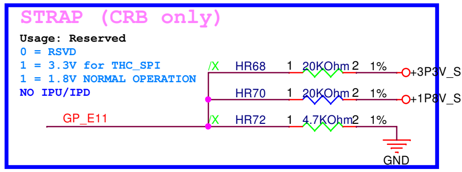

STRAP
Usage: TOP SWAP OVERRIDE
0 = DISABLED (Default)
1 = ENABLED
IPD 20K
※ EPU 20K at SPI FLASH side.


STRAP
Usage: Reserved
0 = RSVD
1 = NORMAL OPERATION (Default)
NO IPU/IPD
※ EPU 20K at SPI FLASH side.


STRAP (CRB only)
Usage: Reserved
0 = RSVD
1 = 3.3V for THC_SPI
1 = 1.8V NORMAL OPERATION
NO IPU/IPD


STRAP
Usage: Reserved
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K
※ EPU 20K at SPI FLASH side.


STRAP
Usage: Reserved
0 = RSVD
1 = NORMAL OPERATION (Default)
NO IPU/IPD
※ EPU 20K at SPI FLASH side.


STRAP (CRB only)
Usage: Reserved
0 = RSVD
1 = 3.3V for THC_SPI
1 = 1.8V NORMAL OPERATION
NO IPU/IPD

ASUSTek COMPUTER INC.
Title : CPU ESPI/FSPI
Engineer: Shawn Yu

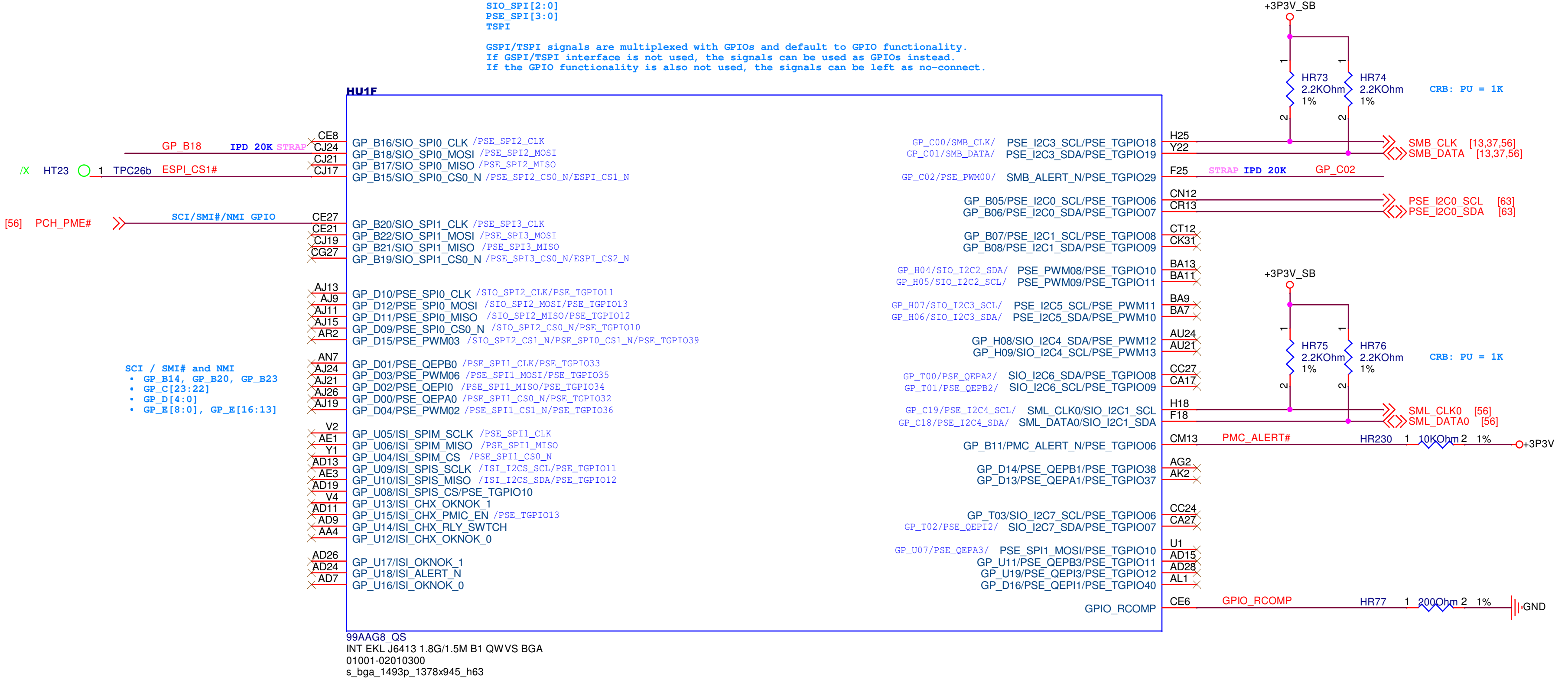
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Friday, July 16, 2021 Sheet 12 of 90

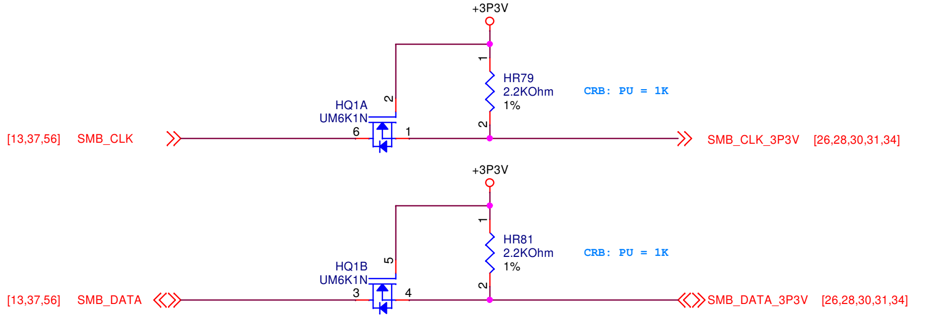
GPIO Disabling and Termination Guidelines
When GPIO interface is not implemented on the platform, the signal pin(s) may be left unterminated, but should not be configured as GPI's.

GSPI/TSPI Disable Guidelines:
SIO_SPI[2:0]
PSE_SPI[3:0]
TSPI

GSPI/TSPI signals are multiplexed with GPIOs and default to GPIO functionality.
If GSPI/TSPI interface is not used, the signals can be used as GPIOs instead.
If the GPIO functionality is also not used, the signals can be left as no-connect.

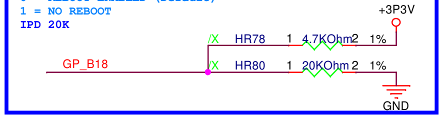

HU1F
GP_B18
IPD 20K STRAP
/X HT23 1 TPC26b ESPI_CS1#
[56] PCH_PME#
SCI/SMI#/NMI GPIO
CE8 GP_B16/SIO_SPI0_CLK /PSE_SPI2_CLK
CJ24 GP_B18/SIO_SPI0_MOSI /PSE_SPI2_MOSI
CJ21 GP_B17/SIO_SPI0_MISO /PSE_SPI2_MISO
CJ17 GP_B15/SIO_SPI0_CS0_N /PSE_SPI2_CS0_N/ESPI_CS1_N
CE27 GP_B20/SIO_SPI1_CLK /PSE_SPI3_CLK
CE21 GP_B22/SIO_SPI1_MOSI /PSE_SPI3_MOSI
CJ19 GP_B21/SIO_SPI1_MISO /PSE_SPI3_MISO
CG27 GP_B19/SIO_SPI1_CS0_N /PSE_SPI3_CS0_N/ESPI_CS2_N
AJ13 GP_D10/PSE_SPI0_CLK /SIO_SPI2_CLK/PSE_TGPIO11
AJ9 GP_D12/PSE_SPI0_MOSI /SIO_SPI2_MOSI/PSE_TGPIO13
AJ11 GP_D11/PSE_SPI0_MISO /SIO_SPI2_MISO/PSE_TGPIO12
AJ15 GP_D09/PSE_SPI0_CS0_N /SIO_SPI2_CS0_N/PSE_TGPIO10
AR2 GP_D15/PSE_PWM03 /SIO_SPI2_CS1_N/PSE_SPI0_CS1_N/PSE_TGPIO39
AN7 GP_D01/PSE_QEPB0 /PSE_SPI1_CLK/PSE_TGPIO33
AJ24 GP_D03/PSE_PWM06 /PSE_SPI1_MOSI/PSE_TGPIO35
AJ21 GP_D02/PSE_QEPI0 /PSE_SPI1_MISO/PSE_TGPIO34
AJ26 GP_D00/PSE_QEPA0 /PSE_SPI1_CS0_N/PSE_TGPIO32
AJ19 GP_D04/PSE_PWM02 /PSE_SPI1_CS1_N/PSE_TGPIO36
V2 GP_U05/ISI_SPIM_SCLK /PSE_SPI1_CLK
AE1 GP_U06/ISI_SPIM_MISO /PSE_SPI1_MISO
Y1 GP_U04/ISI_SPIM_CS /PSE_SPI1_CS0_N
AD13 GP_U09/ISI_SPIS_SCLK /ISI_I2CS_SCL/PSE_TGPIO11
AE3 GP_U10/ISI_SPIS_MISO /ISI_I2CS_SDA/PSE_TGPIO12
AD19 GP_U08/ISI_SPIS_CS/PSE_TGPIO10
V4 GP_U13/ISI_CHX_OKNOK_1
AD11 GP_U15/ISI_CHX_PMIC_EN /PSE_TGPIO13
AD9 GP_U14/ISI_CHX_RLY_SWTCH
AA4 GP_U12/ISI_CHX_OKNOK_0
AD26 GP_U17/ISI_OKNOK_1
AD24 GP_U18/ISI_ALERT_N
AD7 GP_U16/ISI_OKNOK_0
GP_C00/SMB_CLK/ PSE_I2C3_SCL/PSE_TGPIO18 H25
GP_C01/SMB_DATA/ PSE_I2C3_SDA/PSE_TGPIO19 Y22
GP_C02/PSE_PWM00/ SMB_ALERT_N/PSE_TGPIO29 F25
GP_B05/PSE_I2C0_SCL/PSE_TGPIO06 CN12
GP_B06/PSE_I2C0_SDA/PSE_TGPIO07 CR13
GP_B07/PSE_I2C1_SCL/PSE_TGPIO08 CT12
GP_B08/PSE_I2C1_SDA/PSE_TGPIO09 CK31
GP_H04/SIO_I2C2_SDA/ PSE_PWM08/PSE_TGPIO10 BA13
GP_H05/SIO_I2C2_SCL/ PSE_PWM09/PSE_TGPIO11 BA11
GP_H07/SIO_I2C3_SCL/ PSE_I2C5_SCL/PSE_PWM11 BA9
GP_H06/SIO_I2C3_SDA/ PSE_I2C5_SDA/PSE_PWM10 BA7
GP_H08/SIO_I2C4_SDA/PSE_PWM12 AU24
GP_H09/SIO_I2C4_SCL/PSE_PWM13 AU21
GP_T00/PSE_QEPA2/ SIO_I2C6_SDA/PSE_TGPIO08 CC27
GP_T01/PSE_QEPB2/ SIO_I2C6_SCL/PSE_TGPIO09 CA17
GP_C19/PSE_I2C4_SCL/ SML_CLK0/SIO_I2C1_SCL H18
GP_C18/PSE_I2C4_SDA/ SML_DATA0/SIO_I2C1_SDA F18
GP_B11/PMC_ALERT_N/PSE_TGPIO06 CM13
GP_D14/PSE_QEPB1/PSE_TGPIO38 AG2
GP_D13/PSE_QEPA1/PSE_TGPIO37 AK2
GP_T03/SIO_I2C7_SCL/PSE_TGPIO06 CC24
GP_T02/PSE_QEPI2/ SIO_I2C7_SDA/PSE_TGPIO07 CA27
GP_U07/PSE_QEPA3/ PSE_SPI1_MOSI/PSE_TGPIO10 U1
GP_U11/PSE_QEPB3/PSE_TGPIO11 AD15
GP_U19/PSE_QEPI3/PSE_TGPIO12 AD28
GP_D16/PSE_QEPI1/PSE_TGPIO40 AL1
GPIO_RCOMP CE6
+3P3V_SB
HR73 2.2KOhm 1%
HR74 2.2KOhm 1%
CRB: PU = 1K
SMB_CLK [13,37,56]
SMB_DATA [13,37,56]
STRAP IPD 20K GP_C02
PSE_I2C0_SCL [63]
PSE_I2C0_SDA [63]
+3P3V_SB
HR75 2.2KOhm 1%
HR76 2.2KOhm 1%
CRB: PU = 1K
SML_CLK0 [56]
SML_DATA0 [56]
PMC_ALERT# HR230 1 10KOhm 2 1% +3P3V
GPIO_RCOMP HR77 1 200Ohm 2 1% GND
99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
s_bga_1493p_1378x945_h63

SCI / SMI# and NMI
- GP_B14, GP_B20, GP_B23
- GP_C[23:22]
- GP_D[4:0]
- GP_E[8:0], GP_E[16:13]



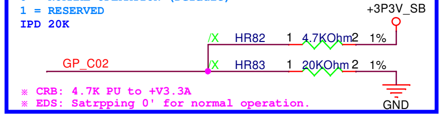
STRAP

Usage: NO REBOOT
0 = REBOOT ENABLED (Default)
1 = NO REBOOT
IPD 20K



STRAP

Usage: Reserved
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K



※ CRB: 4.7K PU to +V3.3A
※ EDS: Satrpping 0' for normal operation.

ASUSTek COMPUTER INC.
Title : CPU SPI
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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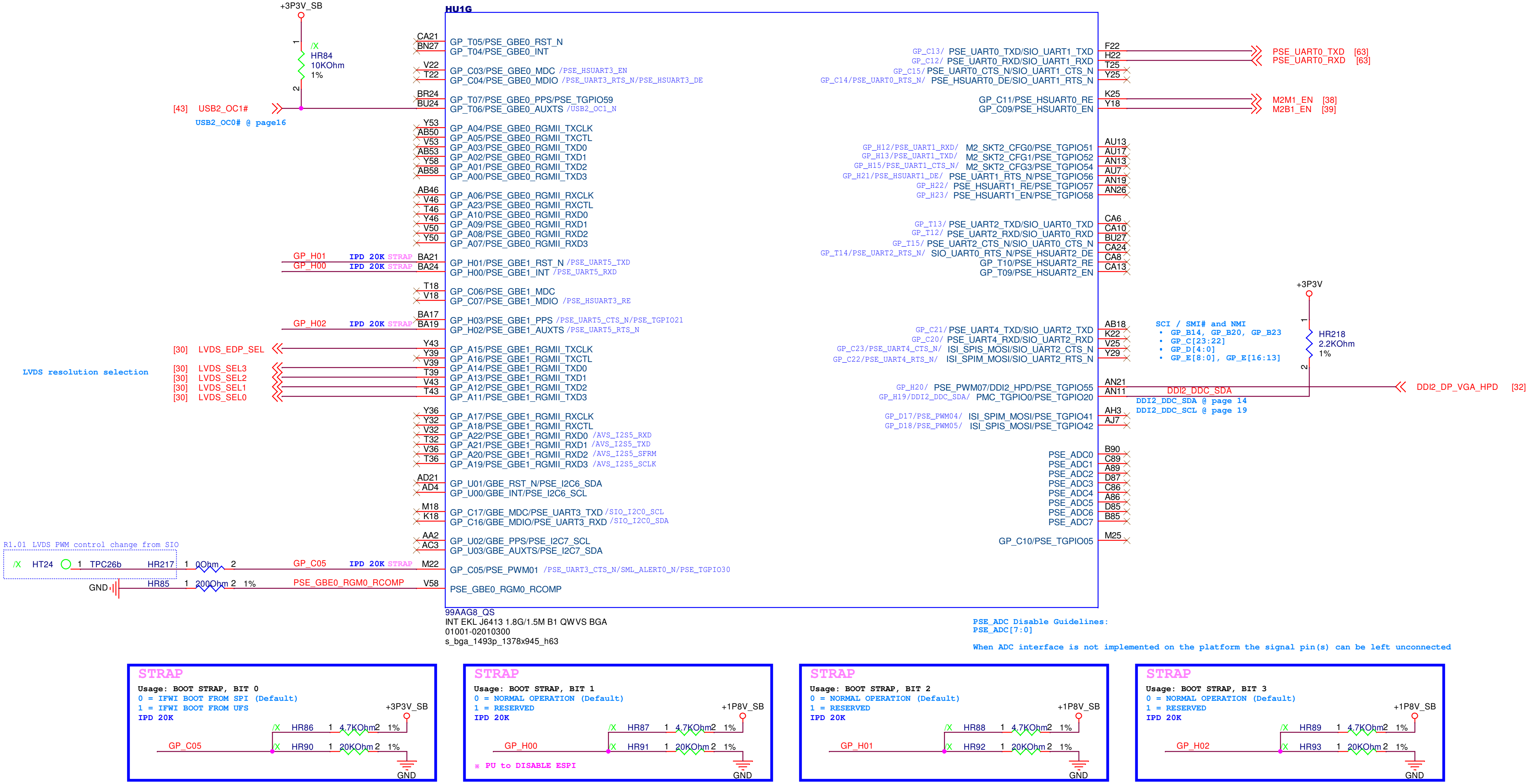
HU1G
+3P3V_SB
HR84 10KOhm 1%
[43] USB2_OC1#
USB2_OC0# @ page16
CA21 GP_T05/PSE_GBE0_RST_N
BN27 GP_T04/PSE_GBE0_INT
V22 GP_C03/PSE_GBE0_MDC /PSE_HSUART3_EN
T22 GP_C04/PSE_GBE0_MDIO /PSE_UART3_RTS_N/PSE_HSUART3_DE
BR24 GP_T07/PSE_GBE0_PPS/PSE_TGPIO59
BU24 GP_T06/PSE_GBE0_AUXTS /USB2_OC1_N
Y53 GP_A04/PSE_GBE0_RGMII_TXCLK
AB50 GP_A05/PSE_GBE0_RGMII_TXCTL
V53 GP_A03/PSE_GBE0_RGMII_TXD0
AB53 GP_A02/PSE_GBE0_RGMII_TXD1
Y58 GP_A01/PSE_GBE0_RGMII_TXD2
AB58 GP_A00/PSE_GBE0_RGMII_TXD3
AB46 GP_A06/PSE_GBE0_RGMII_RXCLK
V46 GP_A23/PSE_GBE0_RGMII_RXCTL
T46 GP_A10/PSE_GBE0_RGMII_RXD0
Y46 GP_A09/PSE_GBE0_RGMII_RXD1
V50 GP_A08/PSE_GBE0_RGMII_RXD2
Y50 GP_A07/PSE_GBE0_RGMII_RXD3
GP_H01 IPD 20K STRAP BA21 GP_H01/PSE_GBE1_RST_N /PSE_UART5_TXD
GP_H00 IPD 20K STRAP BA24 GP_H00/PSE_GBE1_INT /PSE_UART5_RXD
T18 GP_C06/PSE_GBE1_MDC
V18 GP_C07/PSE_GBE1_MDIO /PSE_HSUART3_RE
BA17 GP_H03/PSE_GBE1_PPS /PSE_UART5_CTS_N/PSE_TGPIO21
GP_H02 IPD 20K STRAP BA19 GP_H02/PSE_GBE1_AUXTS /PSE_UART5_RTS_N
[30] LVDS_EDP_SEL
LVDS resolution selection
[30] LVDS_SEL3
[30] LVDS_SEL2
[30] LVDS_SEL1
[30] LVDS_SEL0
Y43 GP_A15/PSE_GBE1_RGMII_TXCLK
Y39 GP_A16/PSE_GBE1_RGMII_TXCTL
V39 GP_A14/PSE_GBE1_RGMII_TXD0
T39 GP_A13/PSE_GBE1_RGMII_TXD1
V43 GP_A12/PSE_GBE1_RGMII_TXD2
T43 GP_A11/PSE_GBE1_RGMII_TXD3
Y36 GP_A17/PSE_GBE1_RGMII_RXCLK
Y32 GP_A18/PSE_GBE1_RGMII_RXCTL
V32 GP_A22/PSE_GBE1_RGMII_RXD0 /AVS_I2S5_RXD
T32 GP_A21/PSE_GBE1_RGMII_RXD1 /AVS_I2S5_TXD
V36 GP_A20/PSE_GBE1_RGMII_RXD2 /AVS_I2S5_SFRM
T36 GP_A19/PSE_GBE1_RGMII_RXD3 /AVS_I2S5_SCLK
AD21 GP_U01/GBE_RST_N/PSE_I2C6_SDA
AD4 GP_U00/GBE_INT/PSE_I2C6_SCL
M18 GP_C17/GBE_MDC/PSE_UART3_TXD /SIO_I2C0_SCL
K18 GP_C16/GBE_MDIO/PSE_UART3_RXD /SIO_I2C0_SDA
AA2 GP_U02/GBE_PPS/PSE_I2C7_SCL
AC3 GP_U03/GBE_AUXTS/PSE_I2C7_SDA
R1.01 LVDS PWM control change from SIO
/X HT24 1 TPC26b
HR217 1 0Ohm 2 GP_C05 IPD 20K STRAP M22 GP_C05/PSE_PWM01 /PSE_UART3_CTS_N/SML_ALERT0_N/PSE_TGPIO30
GND HR85 1 200Ohm 2 1% PSE_GBE0_RGM0_RCOMP V58 PSE_GBE0_RGM0_RCOMP
99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
s_bga_1493p_1378x945_h63
GP_C13/ PSE_UART0_TXD/SIO_UART1_TXD F22
GP_C12/ PSE_UART0_RXD/SIO_UART1_RXD H22
GP_C15/ PSE_UART0_CTS_N/SIO_UART1_CTS_N T25
GP_C14/PSE_UART0_RTS_N/ PSE_HSUART0_DE/SIO_UART1_RTS_N Y25
PSE_UART0_TXD [63]
PSE_UART0_RXD [63]
GP_C11/PSE_HSUART0_RE K25
GP_C09/PSE_HSUART0_EN Y18
M2M1_EN [38]
M2B1_EN [39]
GP_H12/PSE_UART1_RXD/ M2_SKT2_CFG0/PSE_TGPIO51 AU13
GP_H13/PSE_UART1_TXD/ M2_SKT2_CFG1/PSE_TGPIO52 AU17
GP_H15/PSE_UART1_CTS_N/ M2_SKT2_CFG3/PSE_TGPIO54 AN13
GP_H21/PSE_HSUART1_DE/ PSE_UART1_RTS_N/PSE_TGPIO56 AU7
GP_H22/ PSE_HSUART1_RE/PSE_TGPIO57 AN19
GP_H23/ PSE_HSUART1_EN/PSE_TGPIO58 AN26
GP_T13/ PSE_UART2_TXD/SIO_UART0_TXD CA6
GP_T12/ PSE_UART2_RXD/SIO_UART0_RXD CA10
GP_T15/ PSE_UART2_CTS_N/SIO_UART0_CTS_N BU27
GP_T14/PSE_UART2_RTS_N/ SIO_UART0_RTS_N/PSE_HSUART2_DE CA24
GP_T10/PSE_HSUART2_RE CA8
GP_T09/PSE_HSUART2_EN CA13
+3P3V
HR218 2.2KOhm 1%
SCI / SMI# and NMI
• GP_B14, GP_B20, GP_B23
• GP_C[23:22]
• GP_D[4:0]
• GP_E[8:0], GP_E[16:13]
GP_C21/ PSE_UART4_TXD/SIO_UART2_TXD AB18
GP_C20/ PSE_UART4_RXD/SIO_UART2_RXD K22
GP_C23/PSE_UART4_CTS_N/ ISI_SPIS_MOSI/SIO_UART2_CTS_N V25
GP_C22/PSE_UART4_RTS_N/ ISI_SPIM_MOSI/SIO_UART2_RTS_N Y29
GP_H20/ PSE_PWM07/DDI2_HPD/PSE_TGPIO55 AN21
GP_H19/DDI2_DDC_SDA/ PMC_TGPIO0/PSE_TGPIO20 AN11
DDI2_DDC_SDA
DDI2_DP_VGA_HPD [32]
DDI2_DDC_SDA @ page 14
DDI2_DDC_SCL @ page 19
GP_D17/PSE_PWM04/ ISI_SPIM_MOSI/PSE_TGPIO41 AH3
GP_D18/PSE_PWM05/ ISI_SPIS_MOSI/PSE_TGPIO42 AJ7
PSE_ADC0 B90
PSE_ADC1 C89
PSE_ADC2 A89
PSE_ADC3 D87
PSE_ADC4 C86
PSE_ADC5 A86
PSE_ADC6 D85
PSE_ADC7 B85
GP_C10/PSE_TGPIO05 M25
STRAP
Usage: BOOT STRAP, BIT 0
0 = IFWI BOOT FROM SPI (Default)
1 = IFWI BOOT FROM UFS
IPD 20K
+3P3V_SB
/X HR86 1 4.7KOhm 2 1%
GP_C05
/X HR90 1 20KOhm 2 1%
GND
STRAP
Usage: BOOT STRAP, BIT 1
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K
+1P8V_SB
/X HR87 1 4.7KOhm 2 1%
GP_H00
/X HR91 1 20KOhm 2 1%
※ PU to DISABLE ESPI
GND
STRAP
Usage: BOOT STRAP, BIT 2
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K
+1P8V_SB
/X HR88 1 4.7KOhm 2 1%
GP_H01
/X HR92 1 20KOhm 2 1%
GND
STRAP
Usage: BOOT STRAP, BIT 3
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K
+1P8V_SB
/X HR89 1 4.7KOhm 2 1%
GP_H02
/X HR93 1 20KOhm 2 1%
GND

PSE_ADC Disable Guidelines:
PSE_ADC[7:0]

When ADC interface is not implemented on the platform the signal pin(s) can be left unconnected

GP_C05	GP_H00	GP_H01	GP_H02	Boot Strap Configuration
0	0	0	0	IFWI boot from SPI (eSPI enabled)
0	1	0	0	IFWI boot from SPI (eSPI disabled)

ASUSTek COMPUTER INC.
Title : CPU PSE GBE RGMI
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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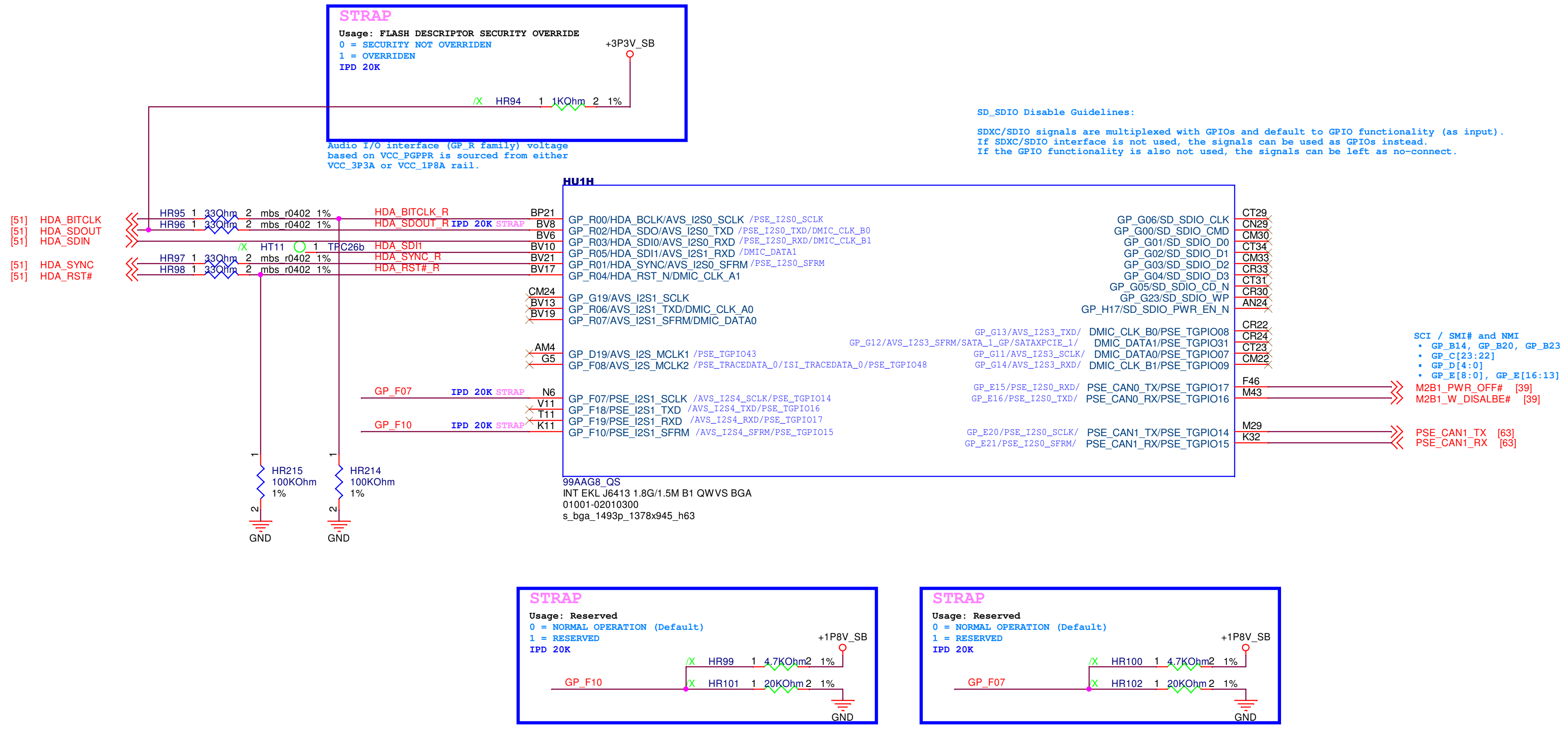


STRAP

Usage: FLASH DESCRIPTOR SECURITY OVERRIDE
0 = SECURITY NOT OVERRIDEN
1 = OVERRIDEN
IPD 20K

Audio I/O interface (GP_R family) voltage based on VCC_PGPPR is sourced from either VCC_3P3A or VCC_1P8A rail.

SD_SDIO Disable Guidelines:

SDXC/SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input).
If SDXC/SDIO interface is not used, the signals can be used as GPIOs instead.
If the GPIO functionality is also not used, the signals can be left as no-connect.

SCI / SMI# and NMI
- GP_B14, GP_B20, GP_B23
- GP_C[23:22]
- GP_D[4:0]
- GP_E[8:0], GP_E[16:13]

STRAP

Usage: Reserved
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K

STRAP

Usage: Reserved
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K

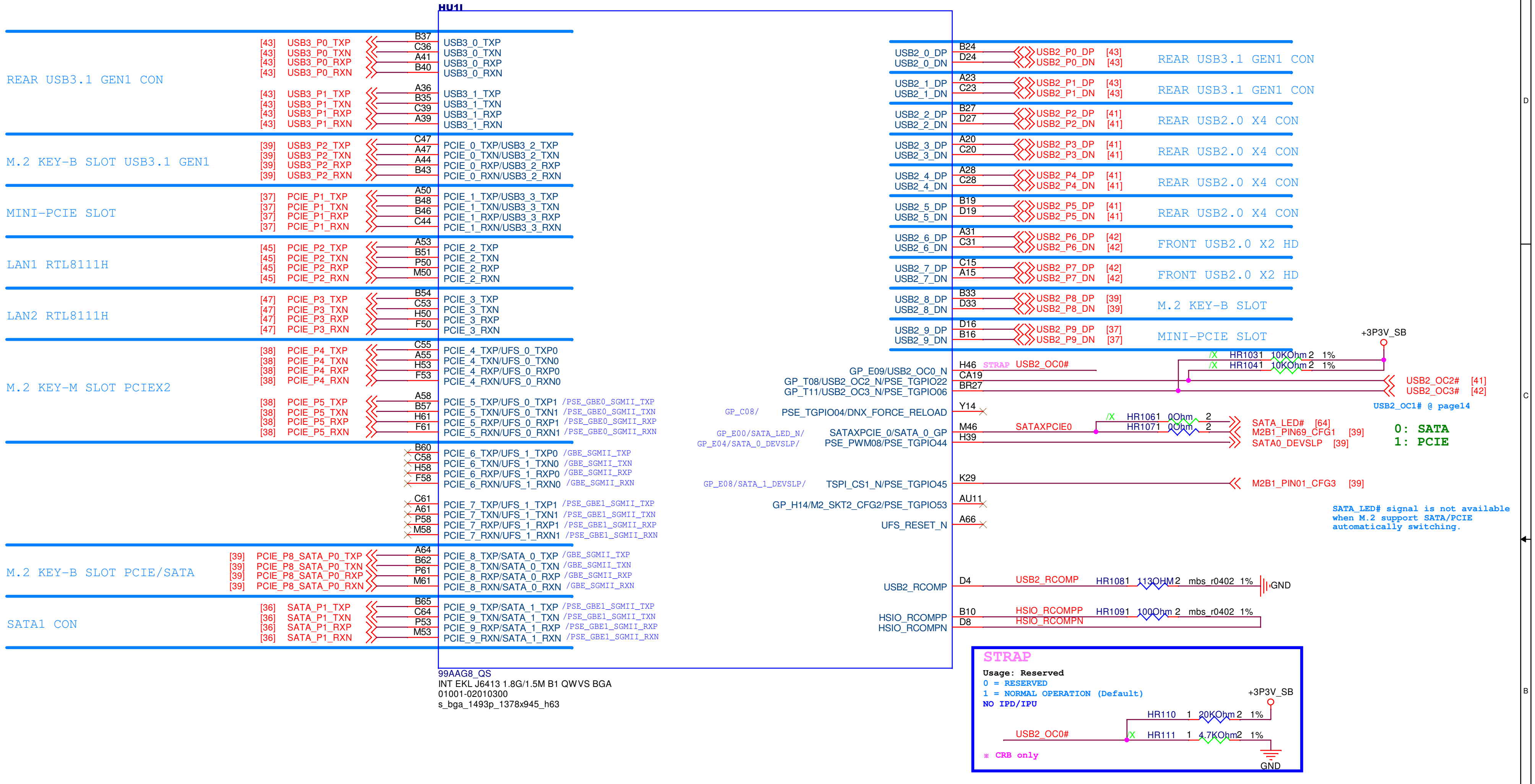
+3P3V_SB
/X HR94 1 1KOhm 2 1%
[51] HDA_BITCLK
[51] HDA_SDOUT
[51] HDA_SDIN
[51] HDA_SYNC
[51] HDA_RST#
HR95 1 33Ohm 2 mbs_r0402 1%
HR96 1 33Ohm 2 mbs_r0402 1%
/X HT11 1 TPC26b
HR97 1 33Ohm 2 mbs_r0402 1%
HR98 1 33Ohm 2 mbs_r0402 1%
HDA_BITCLK_R
HDA_SDOUT_R IPD 20K STRAP
HDA_SDI1
HDA_SYNC_R
HDA_RST#_R
GP_F07 IPD 20K STRAP
GP_F10 IPD 20K STRAP
HR215 100KOhm 1%
HR214 100KOhm 1%
1
2
GND
GND
HU1H
BP21 GP_R00/HDA_BCLK/AVS_I2S0_SCLK /PSE_I2S0_SCLK
BV8 GP_R02/HDA_SDO/AVS_I2S0_TXD /PSE_I2S0_TXD/DMIC_CLK_B0
BV6 GP_R03/HDA_SDI0/AVS_I2S0_RXD /PSE_I2S0_RXD/DMIC_CLK_B1
BV10 GP_R05/HDA_SDI1/AVS_I2S1_RXD /DMIC_DATA1
BV21 GP_R01/HDA_SYNC/AVS_I2S0_SFRM /PSE_I2S0_SFRM
BV17 GP_R04/HDA_RST_N/DMIC_CLK_A1
CM24 GP_G19/AVS_I2S1_SCLK
BV13 GP_R06/AVS_I2S1_TXD/DMIC_CLK_A0
BV19 GP_R07/AVS_I2S1_SFRM/DMIC_DATA0
AM4 GP_D19/AVS_I2S_MCLK1 /PSE_TGPIO43
G5 GP_F08/AVS_I2S_MCLK2 /PSE_TRACEDATA_0/ISI_TRACEDATA_0/PSE_TGPIO48
N6 GP_F07/PSE_I2S1_SCLK /AVS_I2S4_SCLK/PSE_TGPIO14
V11 GP_F18/PSE_I2S1_TXD /AVS_I2S4_TXD/PSE_TGPIO16
T11 GP_F19/PSE_I2S1_RXD /AVS_I2S4_RXD/PSE_TGPIO17
K11 GP_F10/PSE_I2S1_SFRM /AVS_I2S4_SFRM/PSE_TGPIO15
GP_G06/SD_SDIO_CLK CT29
GP_G00/SD_SDIO_CMD CN29
GP_G01/SD_SDIO_D0 CM30
GP_G02/SD_SDIO_D1 CT34
GP_G03/SD_SDIO_D2 CM33
GP_G04/SD_SDIO_D3 CR33
GP_G05/SD_SDIO_CD_N CT31
GP_G23/SD_SDIO_WP CR30
GP_H17/SD_SDIO_PWR_EN_N AN24
GP_G13/AVS_I2S3_TXD/ DMIC_CLK_B0/PSE_TGPIO08 CR22
GP_G12/AVS_I2S3_SFRM/SATA_1_GP/SATAXPCIE_1/ DMIC_DATA1/PSE_TGPIO31 CR24
GP_G11/AVS_I2S3_SCLK/ DMIC_DATA0/PSE_TGPIO07 CT23
GP_G14/AVS_I2S3_RXD/ DMIC_CLK_B1/PSE_TGPIO09 CM22
GP_E15/PSE_I2S0_RXD/ PSE_CAN0_TX/PSE_TGPIO17 F46
GP_E16/PSE_I2S0_TXD/ PSE_CAN0_RX/PSE_TGPIO16 M43
GP_E20/PSE_I2S0_SCLK/ PSE_CAN1_TX/PSE_TGPIO14 M29
GP_E21/PSE_I2S0_SFRM/ PSE_CAN1_RX/PSE_TGPIO15 K32
M2B1_PWR_OFF# [39]
M2B1_W_DISALBE# [39]
PSE_CAN1_TX [63]
PSE_CAN1_RX [63]
99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
s_bga_1493p_1378x945_h63
+1P8V_SB
/X HR99 1 4.7KOhm2 1%
GP_F10
/X HR101 1 20KOhm 2 1%
GND
+1P8V_SB
/X HR100 1 4.7KOhm2 1%
GP_F07
/X HR102 1 20KOhm 2 1%
GND
5
4
3
2
1
D
C
B
A

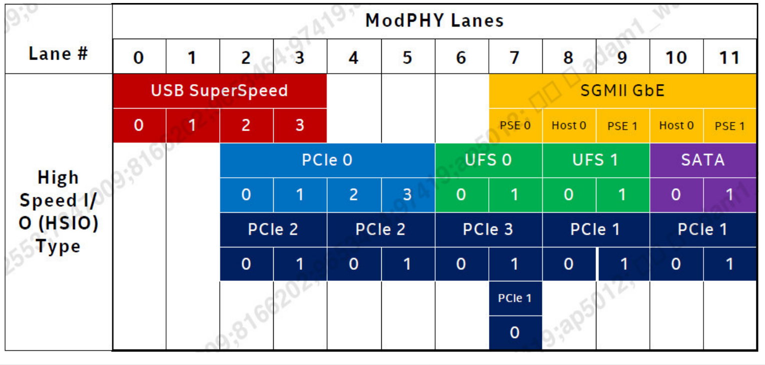
ASUSTek COMPUTER INC.

Title : CPU HDA/I2S/SD_SDIO
Engineer: Shawn Yu

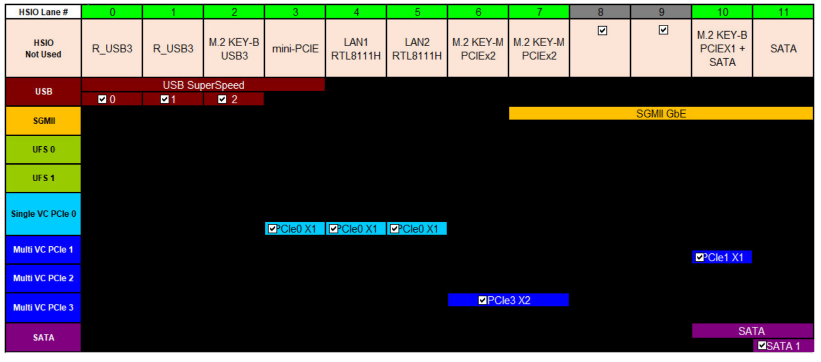
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 15 of 90


HU1I
REAR USB3.1 GEN1 CON
[43] USB3_P0_TXP B37 USB3_0_TXP
[43] USB3_P0_TXN C36 USB3_0_TXN
[43] USB3_P0_RXP A41 USB3_0_RXP
[43] USB3_P0_RXN B40 USB3_0_RXN
[43] USB3_P1_TXP A36 USB3_1_TXP
[43] USB3_P1_TXN B35 USB3_1_TXN
[43] USB3_P1_RXP C39 USB3_1_RXP
[43] USB3_P1_RXN A39 USB3_1_RXN
M.2 KEY-B SLOT USB3.1 GEN1
[39] USB3_P2_TXP C47 PCIE_0_TXP/USB3_2_TXP
[39] USB3_P2_TXN A47 PCIE_0_TXN/USB3_2_TXN
[39] USB3_P2_RXP A44 PCIE_0_RXP/USB3_2_RXP
[39] USB3_P2_RXN B43 PCIE_0_RXN/USB3_2_RXN
MINI-PCIE SLOT
[37] PCIE_P1_TXP A50 PCIE_1_TXP/USB3_3_TXP
[37] PCIE_P1_TXN B48 PCIE_1_TXN/USB3_3_TXN
[37] PCIE_P1_RXP B46 PCIE_1_RXP/USB3_3_RXP
[37] PCIE_P1_RXN C44 PCIE_1_RXN/USB3_3_RXN
LAN1 RTL8111H
[45] PCIE_P2_TXP A53 PCIE_2_TXP
[45] PCIE_P2_TXN B51 PCIE_2_TXN
[45] PCIE_P2_RXP P50 PCIE_2_RXP
[45] PCIE_P2_RXN M50 PCIE_2_RXN
LAN2 RTL8111H
[47] PCIE_P3_TXP B54 PCIE_3_TXP
[47] PCIE_P3_TXN C53 PCIE_3_TXN
[47] PCIE_P3_RXP H50 PCIE_3_RXP
[47] PCIE_P3_RXN F50 PCIE_3_RXN
M.2 KEY-M SLOT PCIEX2
[38] PCIE_P4_TXP C55 PCIE_4_TXP/UFS_0_TXP0
[38] PCIE_P4_TXN A55 PCIE_4_TXN/UFS_0_TXN0
[38] PCIE_P4_RXP H53 PCIE_4_RXP/UFS_0_RXP0
[38] PCIE_P4_RXN F53 PCIE_4_RXN/UFS_0_RXN0
[38] PCIE_P5_TXP A58 PCIE_5_TXP/UFS_0_TXP1 /PSE_GBE0_SGMII_TXP
[38] PCIE_P5_TXN B57 PCIE_5_TXN/UFS_0_TXN1 /PSE_GBE0_SGMII_TXN
[38] PCIE_P5_RXP H61 PCIE_5_RXP/UFS_0_RXP1 /PSE_GBE0_SGMII_RXP
[38] PCIE_P5_RXN F61 PCIE_5_RXN/UFS_0_RXN1 /PSE_GBE0_SGMII_RXN
B60 PCIE_6_TXP/UFS_1_TXP0 /GBE_SGMII_TXP
C58 PCIE_6_TXN/UFS_1_TXN0 /GBE_SGMII_TXN
H58 PCIE_6_RXP/UFS_1_RXP0 /GBE_SGMII_RXP
F58 PCIE_6_RXN/UFS_1_RXN0 /GBE_SGMII_RXN
C61 PCIE_7_TXP/UFS_1_TXP1 /PSE_GBE1_SGMII_TXP
A61 PCIE_7_TXN/UFS_1_TXN1 /PSE_GBE1_SGMII_TXN
P58 PCIE_7_RXP/UFS_1_RXP1 /PSE_GBE1_SGMII_RXP
M58 PCIE_7_RXN/UFS_1_RXN1 /PSE_GBE1_SGMII_RXN
M.2 KEY-B SLOT PCIE/SATA
[39] PCIE_P8_SATA_P0_TXP A64 PCIE_8_TXP/SATA_0_TXP /GBE_SGMII_TXP
[39] PCIE_P8_SATA_P0_TXN B62 PCIE_8_TXN/SATA_0_TXN /GBE_SGMII_TXN
[39] PCIE_P8_SATA_P0_RXP P61 PCIE_8_RXP/SATA_0_RXP /GBE_SGMII_RXP
[39] PCIE_P8_SATA_P0_RXN M61 PCIE_8_RXN/SATA_0_RXN /GBE_SGMII_RXN
SATA1 CON
[36] SATA_P1_TXP B65 PCIE_9_TXP/SATA_1_TXP /PSE_GBE1_SGMII_TXP
[36] SATA_P1_TXN C64 PCIE_9_TXN/SATA_1_TXN /PSE_GBE1_SGMII_TXN
[36] SATA_P1_RXP P53 PCIE_9_RXP/SATA_1_RXP /PSE_GBE1_SGMII_RXP
[36] SATA_P1_RXN M53 PCIE_9_RXN/SATA_1_RXN /PSE_GBE1_SGMII_RXN
USB2_0_DP B24 USB2_P0_DP [43]
USB2_0_DN D24 USB2_P0_DN [43] REAR USB3.1 GEN1 CON
USB2_1_DP A23 USB2_P1_DP [43]
USB2_1_DN C23 USB2_P1_DN [43] REAR USB3.1 GEN1 CON
USB2_2_DP B27 USB2_P2_DP [41]
USB2_2_DN D27 USB2_P2_DN [41] REAR USB2.0 X4 CON
USB2_3_DP A20 USB2_P3_DP [41]
USB2_3_DN C20 USB2_P3_DN [41] REAR USB2.0 X4 CON
USB2_4_DP A28 USB2_P4_DP [41]
USB2_4_DN C28 USB2_P4_DN [41] REAR USB2.0 X4 CON
USB2_5_DP B19 USB2_P5_DP [41]
USB2_5_DN D19 USB2_P5_DN [41] REAR USB2.0 X4 CON
USB2_6_DP A31 USB2_P6_DP [42]
USB2_6_DN C31 USB2_P6_DN [42] FRONT USB2.0 X2 HD
USB2_7_DP C15 USB2_P7_DP [42]
USB2_7_DN A15 USB2_P7_DN [42] FRONT USB2.0 X2 HD
USB2_8_DP B33 USB2_P8_DP [39]
USB2_8_DN D33 USB2_P8_DN [39] M.2 KEY-B SLOT
USB2_9_DP D16 USB2_P9_DP [37]
USB2_9_DN B16 USB2_P9_DN [37] MINI-PCIE SLOT
+3P3V_SB
/X HR1031 10KOhm 2 1%
/X HR1041 10KOhm 2 1%
GP_E09/USB2_OC0_N H46 STRAP USB2_OC0#
GP_T08/USB2_OC2_N/PSE_TGPIO22 CA19 USB2_OC2# [41]
GP_T11/USB2_OC3_N/PSE_TGPIO06 BR27 USB2_OC3# [42]
USB2_OC1# @ page14
GP_C08/ PSE_TGPIO04/DNX_FORCE_RELOAD Y14
/X HR1061 0Ohm 2
HR1071 0Ohm 2
GP_E00/SATA_LED_N/ SATAXPCIE_0/SATA_0_GP M46 SATAXPCIE0 SATA_LED# [64] M2B1_PIN69_CFG1 [39]
GP_E04/SATA_0_DEVSLP/ PSE_PWM08/PSE_TGPIO44 H39 SATA0_DEVSLP [39]
0: SATA
1: PCIE
GP_E08/SATA_1_DEVSLP/ TSPI_CS1_N/PSE_TGPIO45 K29 M2B1_PIN01_CFG3 [39]
GP_H14/M2_SKT2_CFG2/PSE_TGPIO53 AU11
UFS_RESET_N A66
SATA_LED# signal is not available when M.2 support SATA/PCIE automatically switching.
USB2_RCOMP D4 USB2_RCOMP HR1081 113OHM 2 mbs_r0402 1% GND
HSIO_RCOMPP B10 HSIO_RCOMPP HR1091 100Ohm 2 mbs_r0402 1%
HSIO_RCOMPN D8 HSIO_RCOMPN
99AAG8_QS
INT EKL J6413 1.8G/1.5M B1 QWVS BGA
01001-02010300
s_bga_1493p_1378x945_h63
STRAP
Usage: Reserved
0 = RESERVED
1 = NORMAL OPERATION (Default)
NO IPD/IPU
+3P3V_SB
HR110 1 20KOhm 2 1%
USB2_OC0# /X HR111 1 4.7KOhm 2 1%
GND
※ CRB only



	ModPHY Lanes											
Lane #	0	1	2	3	4	5	6	7	8	9	10	11
High Speed I/O (HSIO) Type	USB SuperSpeed							SGMII GbE				
	0	1	2	3				PSE 0	Host 0	PSE 1	Host 0	PSE 1
			PCIe 0				UFS 0		UFS 1		SATA	
			0	1	2	3	0	1	0	1	0	1
			PCIe 2		PCIe 2		PCIe 3		PCIe 1		PCIe 1	
			0	1	0	1	0	1	0	1	0	1
								PCIe 1				
								0				



HSIO Lane #	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Not Used	R_USB3	R_USB3	M.2 KEY-B USB3	mini-PCIE	LAN1 RTL8111H	LAN2 RTL8111H	M.2 KEY-M PCIEx2	M.2 KEY-M PCIEx2	☑	☑	M.2 KEY-B PCIEX1 + SATA	SATA
USB	USB SuperSpeed ☑ 0	☑ 1	☑ 2									
SGMII								SGMII GbE				
UFS 0												
UFS 1												
Single VC PCIe 0				☑PCIe0 X1	☑PCIe0 X1	☑PCIe0 X1						
Multi VC PCIe 1											☑PCIe1 X1	
Multi VC PCIe 2												
Multi VC PCIe 3							☑PCIe3 X2					
SATA											SATA	☑SATA 1

ASUSTek COMPUTER INC.

Title : CPU HSIO USB2.0

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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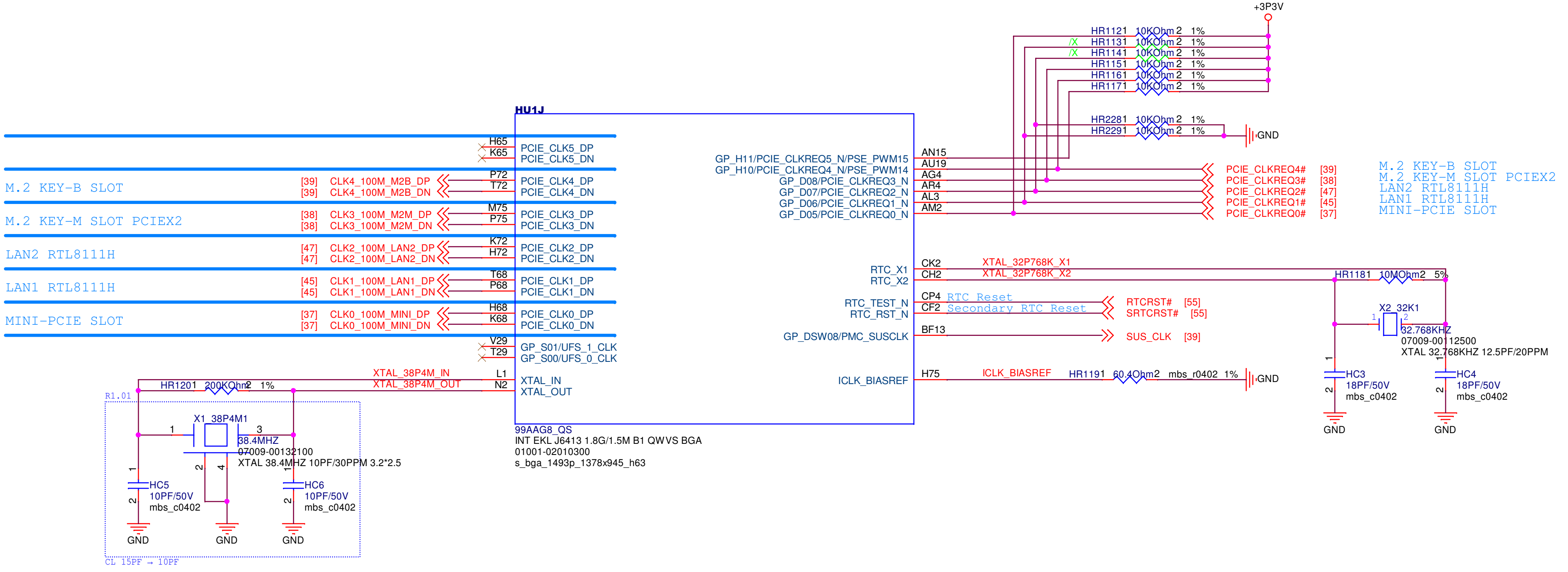


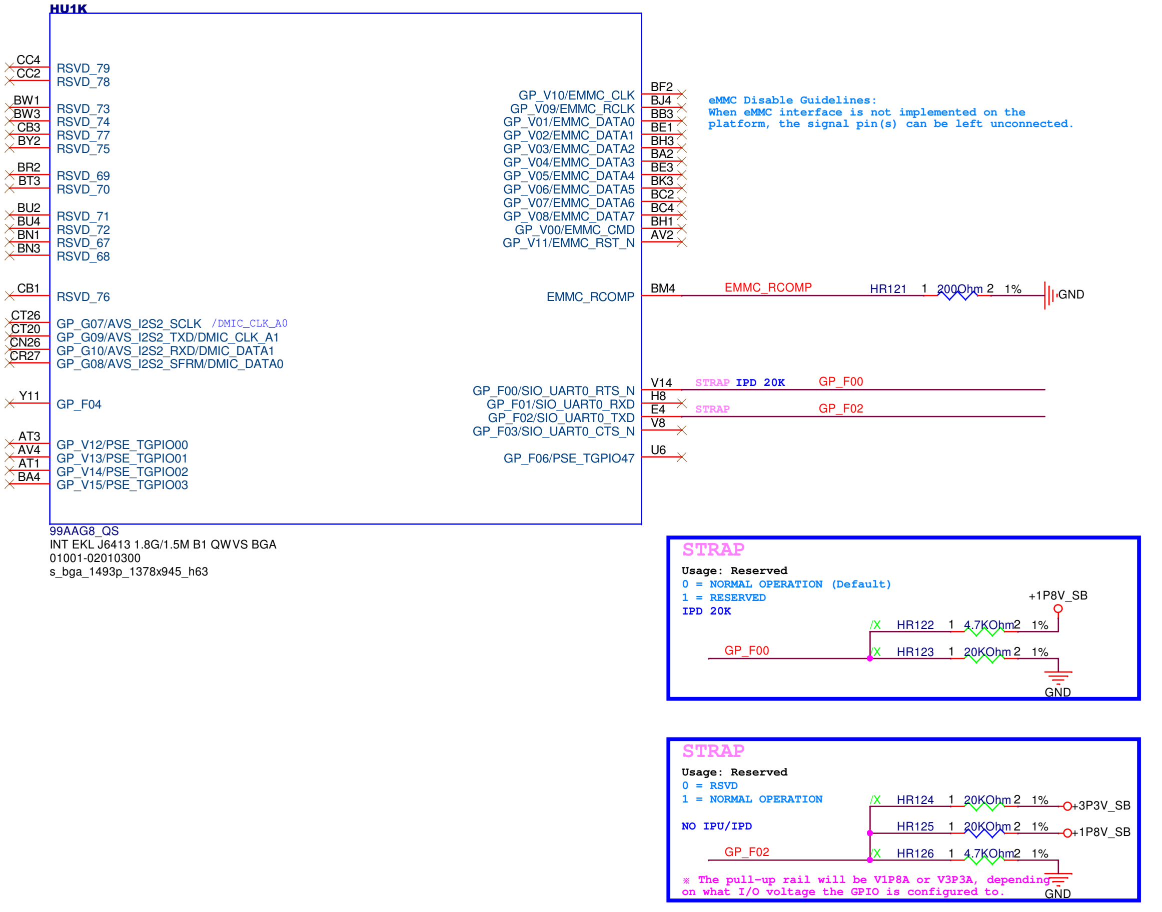
ASUSTek COMPUTER INC.

Title : CPU CLK RTC

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 17 of 90



eMMC Disable Guidelines:
When eMMC interface is not implemented on the platform, the signal pin(s) can be left unconnected.

STRAP

Usage: Reserved
0 = NORMAL OPERATION (Default)
1 = RESERVED
IPD 20K

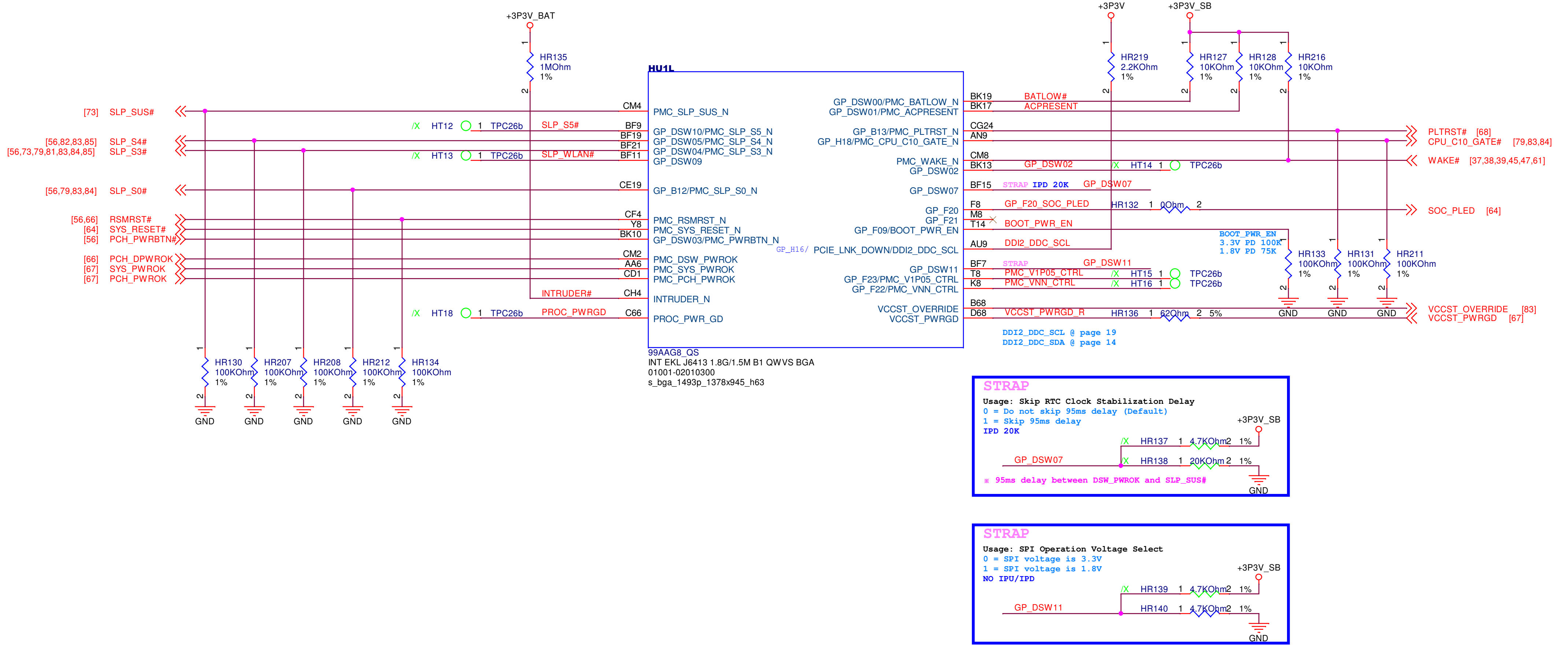
STRAP

Usage: Reserved
0 = RSVD
1 = NORMAL OPERATION

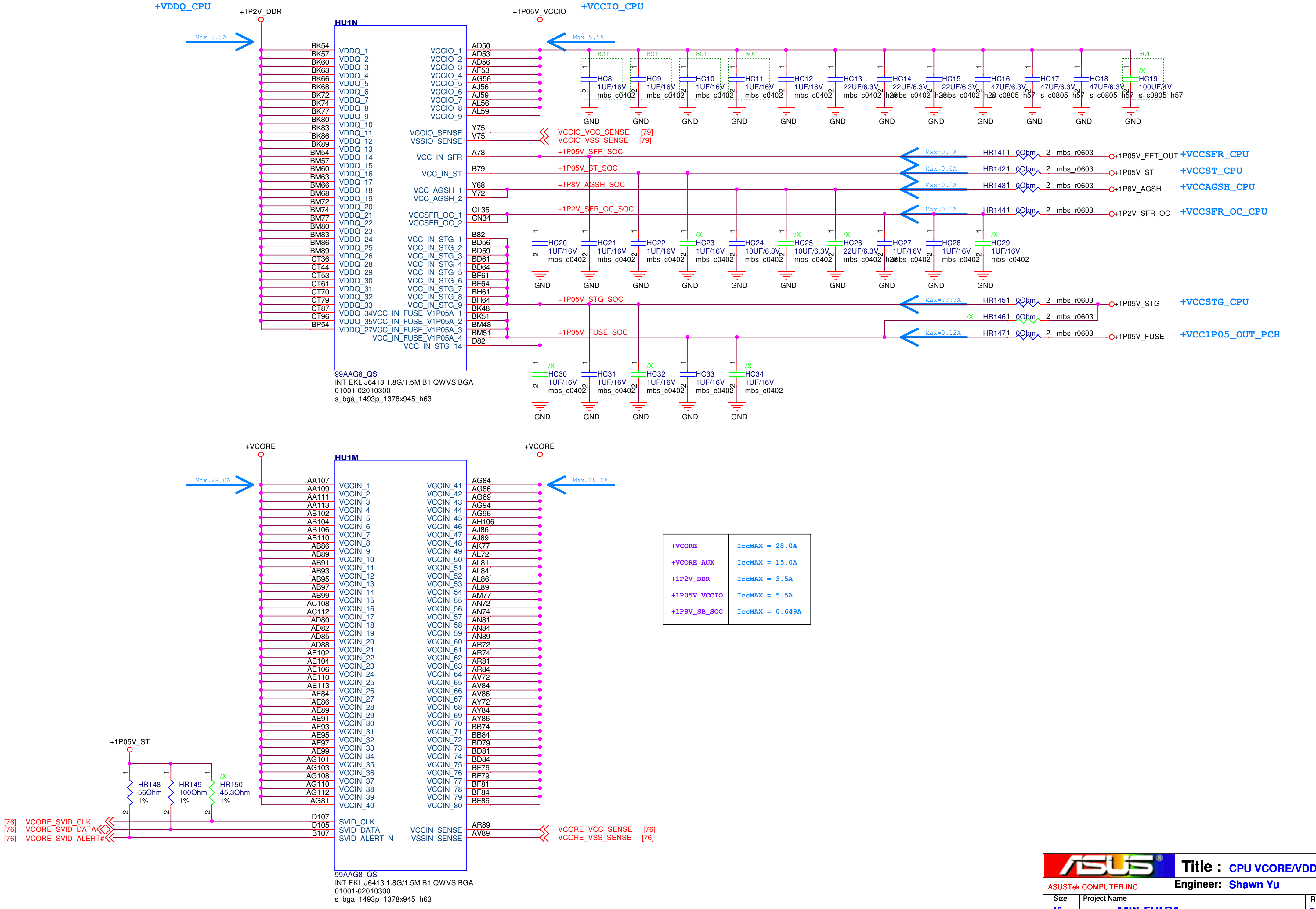
NO IPU/IPD

※ The pull-up rail will be V1P8A or V3P3A, depending on what I/O voltage the GPIO is configured to.

	Title : **CPU EMMC**		
ASUSTek COMPUTER INC.	**Engineer:** **Shawn Yu**		
Size A3	Project Name **MIX-EHLD1**		Rev R1.01
Date: Thursday, July 15, 2021		Sheet 18 of 90	



ASUSTek COMPUTER INC.	Title : CPU MISC Engineer: Shawn Yu	
Size A3	Project Name MIX-EHLD1	Rev R1.01
Date: Thursday, July 15, 2021	Sheet 19 of 90	
]



+VCORE	IccMAX = 28.0A
+VCORE_AUX	IccMAX = 15.0A
+1P2V_DDR	IccMAX = 3.5A
+1P05V_VCCIO	IccMAX = 5.5A
+1P8V_SB_SOC	IccMAX = 0.649A

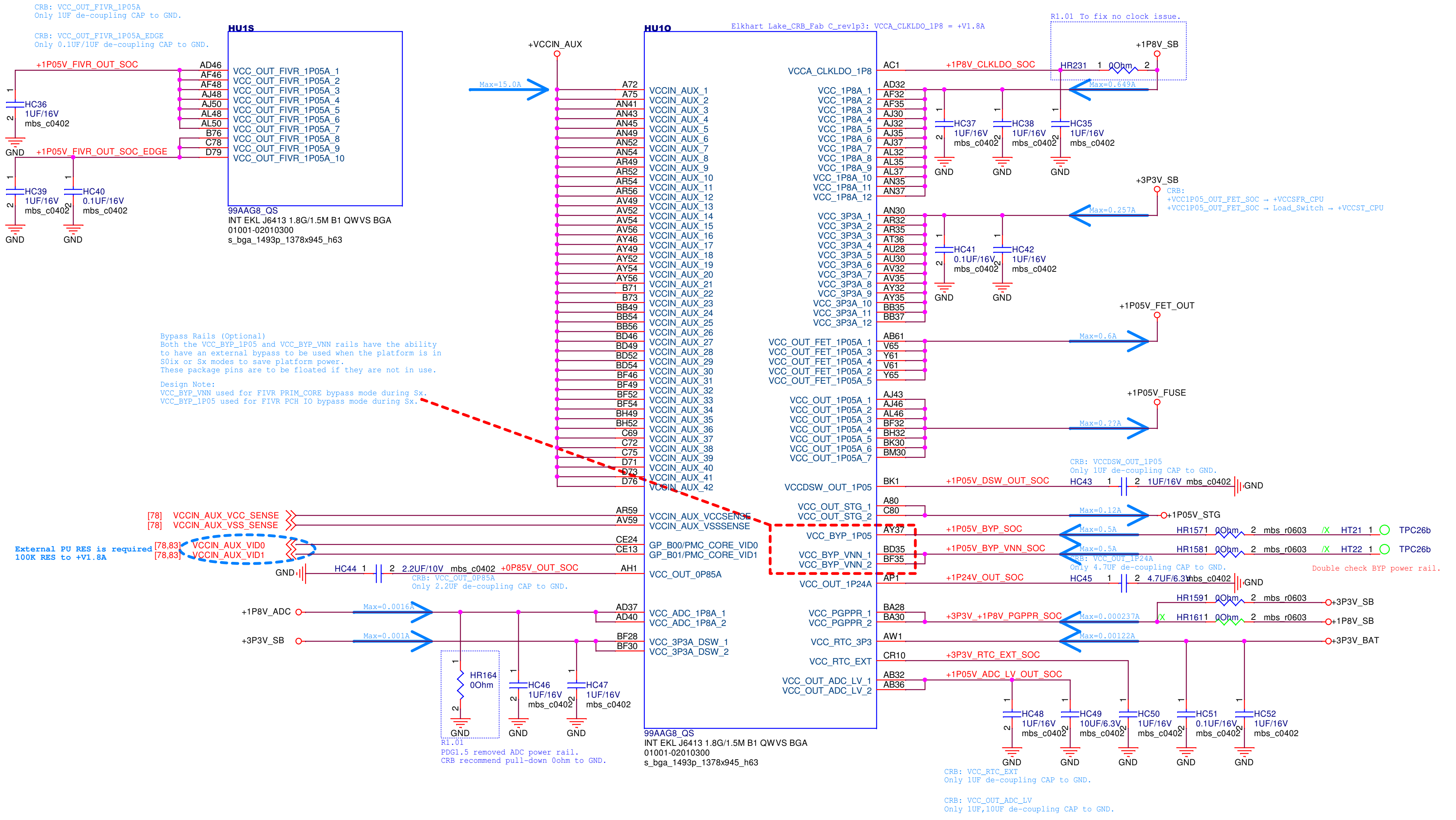
ASUSTek COMPUTER INC.

Title : CPU VCORE/VDDQ/VCCI

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 20 of 90



CRB: VCC_OUT_FIVR_1P05A
Only 1UF de-coupling CAP to GND.

CRB: VCC_OUT_FIVR_1P05A_EDGE
Only 0.1UF/1UF de-coupling CAP to GND.

Elkhart Lake_CRB_Fab C_rev1p3: VCCA_CLKLDO_1P8 = +V1.8A

R1.01 To fix no clock issue.

CRB:
+VCC1P05_OUT_FET_SOC → +VCCSFR_CPU
+VCC1P05_OUT_FET_SOC → Load_Switch → +VCCST_CPU

Bypass Rails (Optional)
Both the VCC_BYP_1P05 and VCC_BYP_VNN rails have the ability to have an external bypass to be used when the platform is in S0ix or Sx modes to save platform power.
These package pins are to be floated if they are not in use.

Design Note:
VCC_BYP_VNN used for FIVR PRIM_CORE bypass mode during Sx.
VCC_BYP_1P05 used for FIVR PCH IO bypass mode during Sx.

CRB: VCCDSW_OUT_1P05
Only 1UF de-coupling CAP to GND.

External PU RES is required
100K RES to +V1.8A

CRB: VCC_OUT_0P85A
Only 2.2UF de-coupling CAP to GND.

CRB: VCC_OUT_1P24A
Only 4.7UF de-coupling CAP to GND.

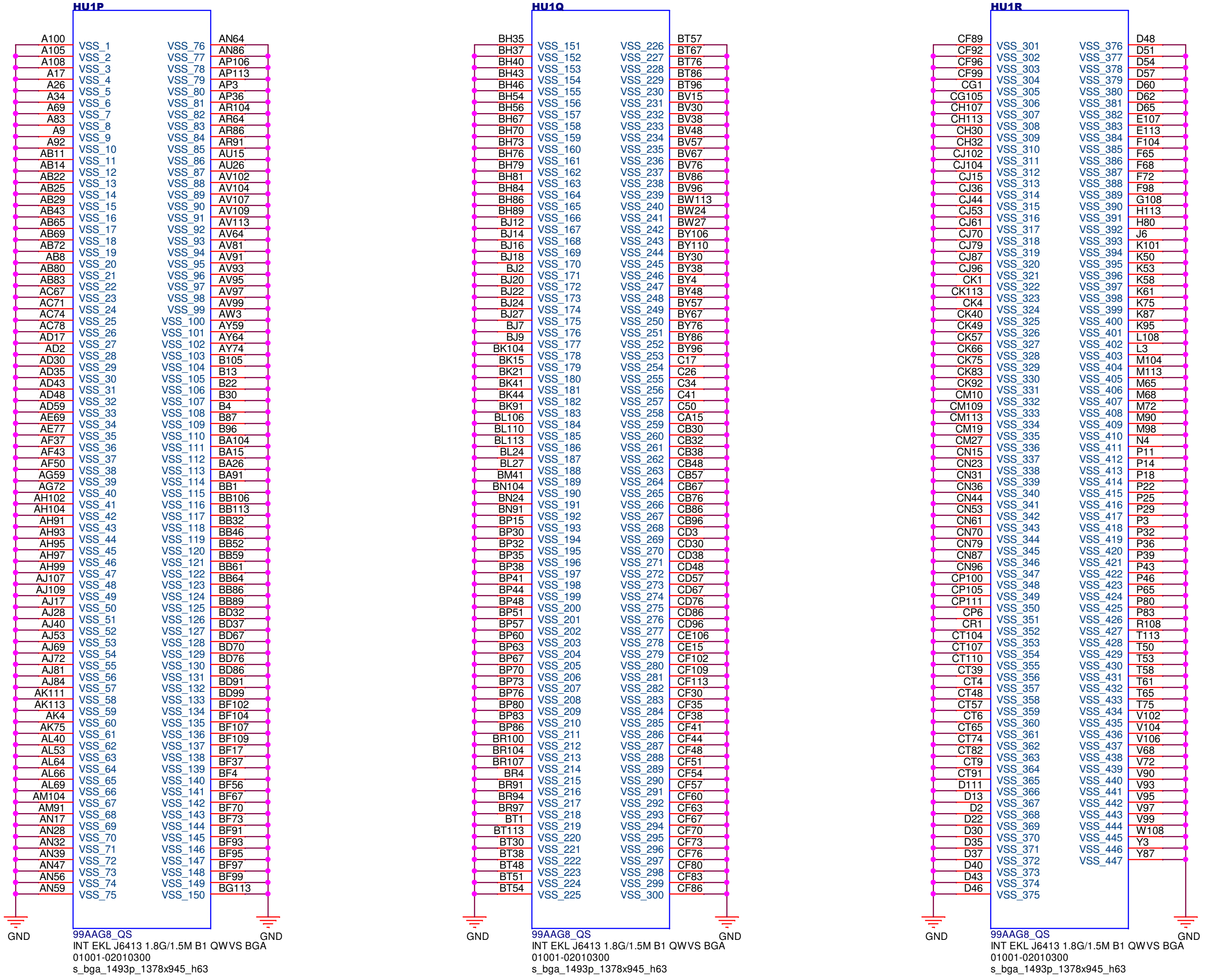
Double check BYP power rail.

R1.01
PDG1.5 removed ADC power rail.
CRB recommend pull-down 0ohm to GND.

CRB: VCC_RTC_EXT
Only 1UF de-coupling CAP to GND.

CRB: VCC_OUT_ADC_LV
Only 1UF,10UF de-coupling CAP to GND.

ASUS	Title : CPU VCORE_AUX/1P8V/	
ASUSTek COMPUTER INC.	Engineer: Shawn Yu	
Size A3	Project Name MIX-EHLD1	Rev R1.01
Date: Thursday, July 15, 2021	Sheet 21 of 90	



Title : CPU VSS

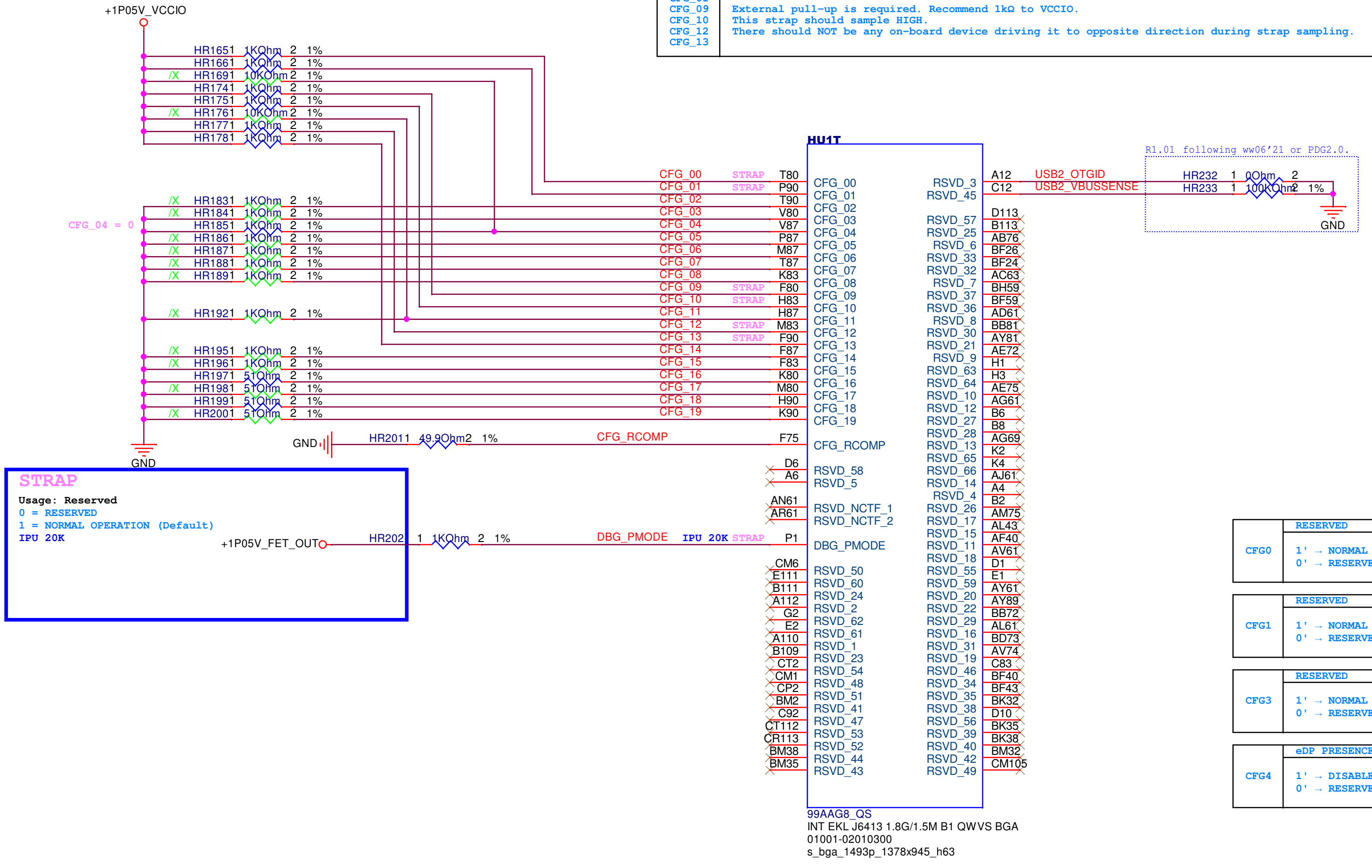
ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

Date: Thursday, July 15, 2021 Sheet 22 of 90

CFG_00 CFG_01 CFG_09 CFG_10 CFG_12 CFG_13	#601458 EDS External pull-up is required. Recommend 1kΩ to VCCIO. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



STRAP

Usage: Reserved
0 = RESERVED
1 = NORMAL OPERATION (Default)
IPU 20K

CFG0	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG1	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG3	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG4	eDP PRESENCE STRAP 1' → DISABLED (DEFAULT) 0' → RESERVED

CFG9	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG10	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG11	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG12	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

CFG13	RESERVED 1' → NORMAL (DEFAULT) 0' → RESERVED

ASUSTek COMPUTER INC.
Title : CPU CFG/RSVD
Engineer: Shawn Yu
Size A3
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
Sheet 23 of 90

D

C

B

A

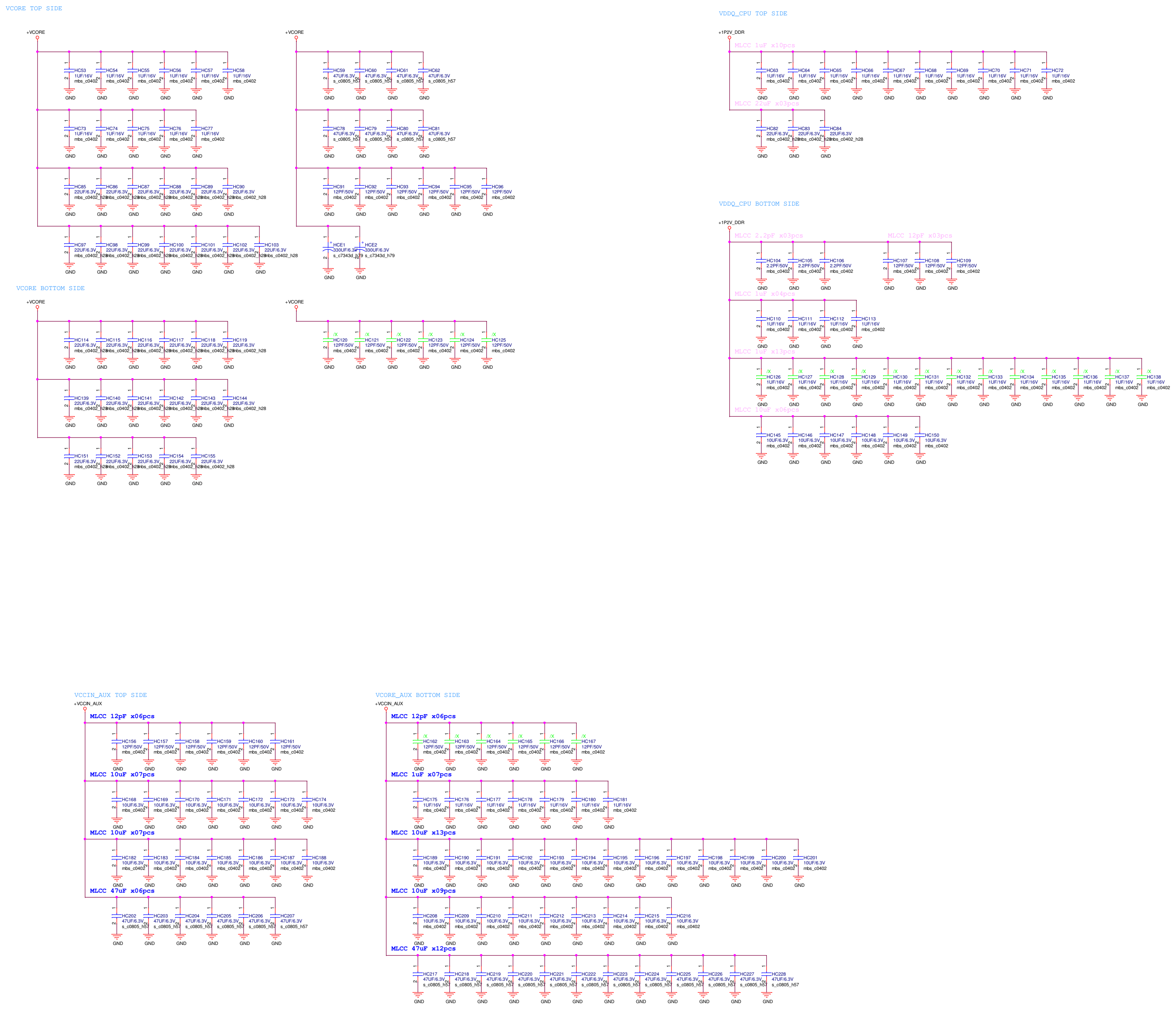
Title : xxx

ASUSTek COMPUTER INC.

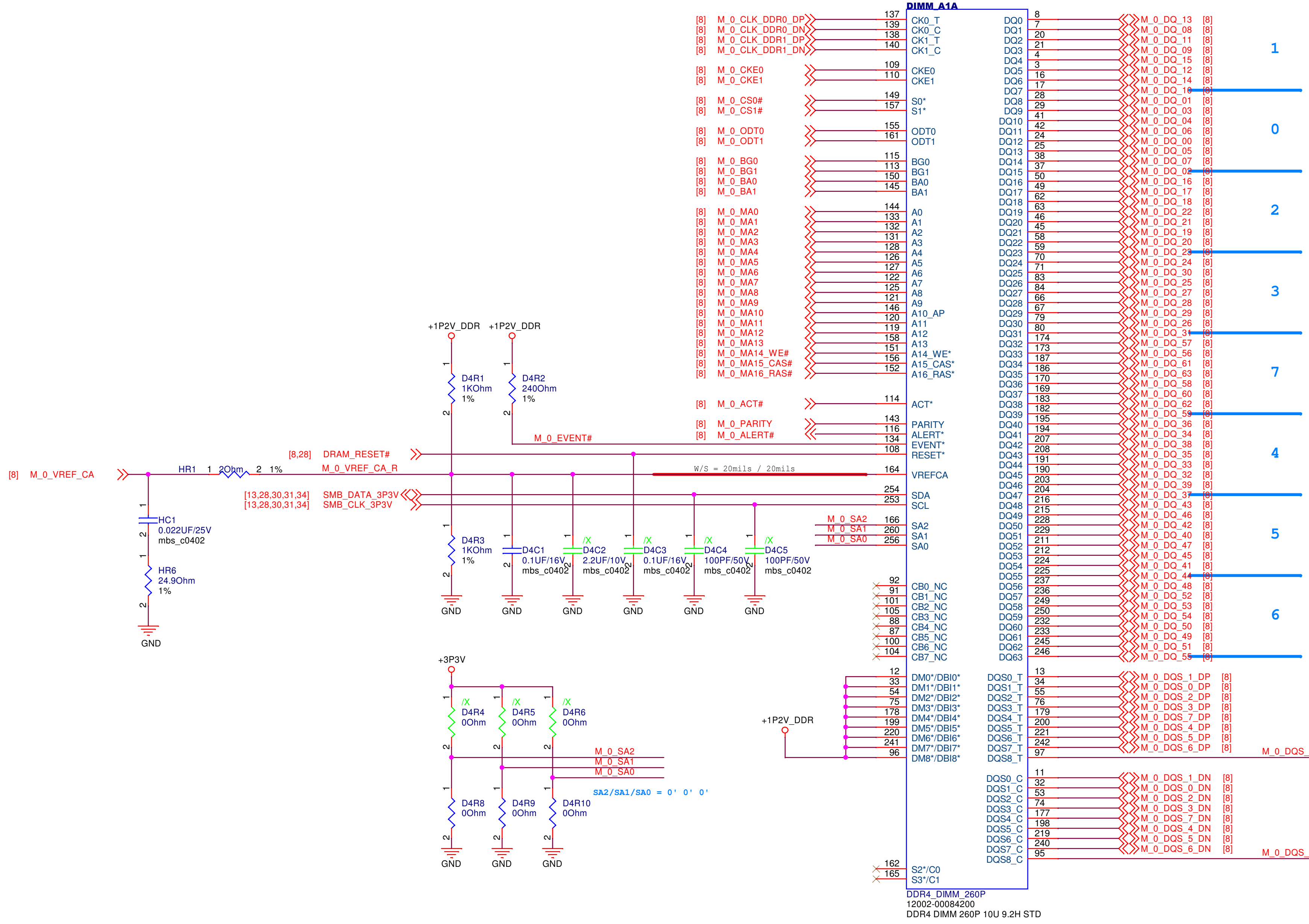
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 24 of 90


VCORE TOP SIDE
+VCORE
HC53 1UF/16V mbs_c0402
HC54 1UF/16V mbs_c0402
HC55 1UF/16V mbs_c0402
HC56 1UF/16V mbs_c0402
HC57 1UF/16V mbs_c0402
HC58 1UF/16V mbs_c0402
HC73 1UF/16V mbs_c0402
HC74 1UF/16V mbs_c0402
HC75 1UF/16V mbs_c0402
HC76 1UF/16V mbs_c0402
HC77 1UF/16V mbs_c0402
HC85 22UF/6.3V mbs_c0402_h28
HC86 22UF/6.3V mbs_c0402_h28
HC87 22UF/6.3V mbs_c0402_h28
HC88 22UF/6.3V mbs_c0402_h28
HC89 22UF/6.3V mbs_c0402_h28
HC90 22UF/6.3V mbs_c0402_h28
HC97 22UF/6.3V mbs_c0402_h28
HC98 22UF/6.3V mbs_c0402_h28
HC99 22UF/6.3V mbs_c0402_h28
HC100 22UF/6.3V mbs_c0402_h28
HC101 22UF/6.3V mbs_c0402_h28
HC102 22UF/6.3V mbs_c0402_h28
HC103 22UF/6.3V mbs_c0402_h28
+VCORE
HC59 47UF/6.3V s_c0805_h57
HC60 47UF/6.3V s_c0805_h57
HC61 47UF/6.3V s_c0805_h57
HC62 47UF/6.3V s_c0805_h57
HC78 47UF/6.3V s_c0805_h57
HC79 47UF/6.3V s_c0805_h57
HC80 47UF/6.3V s_c0805_h57
HC81 47UF/6.3V s_c0805_h57
HC91 12PF/50V mbs_c0402
HC92 12PF/50V mbs_c0402
HC93 12PF/50V mbs_c0402
HC94 12PF/50V mbs_c0402
HC95 12PF/50V mbs_c0402
HC96 12PF/50V mbs_c0402
HCE1 330UF/6.3V s_c7343d_h79
HCE2 330UF/6.3V s_c7343d_h79
VCORE BOTTOM SIDE
+VCORE
HC114 22UF/6.3V mbs_c0402_h28
HC115 22UF/6.3V mbs_c0402_h28
HC116 22UF/6.3V mbs_c0402_h28
HC117 22UF/6.3V mbs_c0402_h28
HC118 22UF/6.3V mbs_c0402_h28
HC119 22UF/6.3V mbs_c0402_h28
HC139 22UF/6.3V mbs_c0402_h28
HC140 22UF/6.3V mbs_c0402_h28
HC141 22UF/6.3V mbs_c0402_h28
HC142 22UF/6.3V mbs_c0402_h28
HC143 22UF/6.3V mbs_c0402_h28
HC144 22UF/6.3V mbs_c0402_h28
HC151 22UF/6.3V mbs_c0402_h28
HC152 22UF/6.3V mbs_c0402_h28
HC153 22UF/6.3V mbs_c0402_h28
HC154 22UF/6.3V mbs_c0402_h28
HC155 22UF/6.3V mbs_c0402_h28
+VCORE
/X HC120 12PF/50V mbs_c0402
/X HC121 12PF/50V mbs_c0402
/X HC122 12PF/50V mbs_c0402
/X HC123 12PF/50V mbs_c0402
/X HC124 12PF/50V mbs_c0402
/X HC125 12PF/50V mbs_c0402
VDDQ_CPU TOP SIDE
+1P2V_DDR
MLCC 1uF x10pcs
HC63 1UF/16V mbs_c0402
HC64 1UF/16V mbs_c0402
HC65 1UF/16V mbs_c0402
HC66 1UF/16V mbs_c0402
HC67 1UF/16V mbs_c0402
HC68 1UF/16V mbs_c0402
HC69 1UF/16V mbs_c0402
HC70 1UF/16V mbs_c0402
HC71 1UF/16V mbs_c0402
HC72 1UF/16V mbs_c0402
MLCC 22uF x03pcs
HC82 22UF/6.3V mbs_c0402_h28
HC83 22UF/6.3V mbs_c0402_h28
HC84 22UF/6.3V mbs_c0402_h28
VDDQ_CPU BOTTOM SIDE
+1P2V_DDR
MLCC 2.2pF x03pcs
HC104 2.2PF/50V mbs_c0402
HC105 2.2PF/50V mbs_c0402
HC106 2.2PF/50V mbs_c0402
MLCC 12pF x03pcs
HC107 12PF/50V mbs_c0402
HC108 12PF/50V mbs_c0402
HC109 12PF/50V mbs_c0402
MLCC 1uF x04pcs
HC110 1UF/16V mbs_c0402
HC111 1UF/16V mbs_c0402
HC112 1UF/16V mbs_c0402
HC113 1UF/16V mbs_c0402
MLCC 1uF x13pcs
/X HC126 1UF/16V mbs_c0402
/X HC127 1UF/16V mbs_c0402
/X HC128 1UF/16V mbs_c0402
/X HC129 1UF/16V mbs_c0402
/X HC130 1UF/16V mbs_c0402
/X HC131 1UF/16V mbs_c0402
/X HC132 1UF/16V mbs_c0402
/X HC133 1UF/16V mbs_c0402
/X HC134 1UF/16V mbs_c0402
/X HC135 1UF/16V mbs_c0402
/X HC136 1UF/16V mbs_c0402
/X HC137 1UF/16V mbs_c0402
/X HC138 1UF/16V mbs_c0402
MLCC 10uF x06pcs
HC145 10UF/6.3V mbs_c0402
HC146 10UF/6.3V mbs_c0402
HC147 10UF/6.3V mbs_c0402
HC148 10UF/6.3V mbs_c0402
HC149 10UF/6.3V mbs_c0402
HC150 10UF/6.3V mbs_c0402
VCCIN_AUX TOP SIDE
+VCCIN_AUX
MLCC 12pF x06pcs
HC156 12PF/50V mbs_c0402
HC157 12PF/50V mbs_c0402
HC158 12PF/50V mbs_c0402
HC159 12PF/50V mbs_c0402
HC160 12PF/50V mbs_c0402
HC161 12PF/50V mbs_c0402
MLCC 10uF x07pcs
HC168 10UF/6.3V mbs_c0402
HC169 10UF/6.3V mbs_c0402
HC170 10UF/6.3V mbs_c0402
HC171 10UF/6.3V mbs_c0402
HC172 10UF/6.3V mbs_c0402
HC173 10UF/6.3V mbs_c0402
HC174 10UF/6.3V mbs_c0402
MLCC 10uF x07pcs
HC182 10UF/6.3V mbs_c0402
HC183 10UF/6.3V mbs_c0402
HC184 10UF/6.3V mbs_c0402
HC185 10UF/6.3V mbs_c0402
HC186 10UF/6.3V mbs_c0402
HC187 10UF/6.3V mbs_c0402
HC188 10UF/6.3V mbs_c0402
MLCC 47uF x06pcs
HC202 47UF/6.3V s_c0805_h57
HC203 47UF/6.3V s_c0805_h57
HC204 47UF/6.3V s_c0805_h57
HC205 47UF/6.3V s_c0805_h57
HC206 47UF/6.3V s_c0805_h57
HC207 47UF/6.3V s_c0805_h57
VCORE_AUX BOTTOM SIDE
+VCCIN_AUX
MLCC 12pF x06pcs
/X HC162 12PF/50V mbs_c0402
/X HC163 12PF/50V mbs_c0402
/X HC164 12PF/50V mbs_c0402
/X HC165 12PF/50V mbs_c0402
/X HC166 12PF/50V mbs_c0402
/X HC167 12PF/50V mbs_c0402
MLCC 1uF x07pcs
HC175 1UF/16V mbs_c0402
HC176 1UF/16V mbs_c0402
HC177 1UF/16V mbs_c0402
HC178 1UF/16V mbs_c0402
HC179 1UF/16V mbs_c0402
HC180 1UF/16V mbs_c0402
HC181 1UF/16V mbs_c0402
MLCC 10uF x13pcs
HC189 10UF/6.3V mbs_c0402
HC190 10UF/6.3V mbs_c0402
HC191 10UF/6.3V mbs_c0402
HC192 10UF/6.3V mbs_c0402
HC193 10UF/6.3V mbs_c0402
HC194 10UF/6.3V mbs_c0402
HC195 10UF/6.3V mbs_c0402
HC196 10UF/6.3V mbs_c0402
HC197 10UF/6.3V mbs_c0402
HC198 10UF/6.3V mbs_c0402
HC199 10UF/6.3V mbs_c0402
HC200 10UF/6.3V mbs_c0402
HC201 10UF/6.3V mbs_c0402
MLCC 10uF x09pcs
HC208 10UF/6.3V mbs_c0402
HC209 10UF/6.3V mbs_c0402
HC210 10UF/6.3V mbs_c0402
HC211 10UF/6.3V mbs_c0402
HC212 10UF/6.3V mbs_c0402
HC213 10UF/6.3V mbs_c0402
HC214 10UF/6.3V mbs_c0402
HC215 10UF/6.3V mbs_c0402
HC216 10UF/6.3V mbs_c0402
MLCC 47uF x12pcs
HC217 47UF/6.3V s_c0805_h57
HC218 47UF/6.3V s_c0805_h57
HC219 47UF/6.3V s_c0805_h57
HC220 47UF/6.3V s_c0805_h57
HC221 47UF/6.3V s_c0805_h57
HC222 47UF/6.3V s_c0805_h57
HC223 47UF/6.3V s_c0805_h57
HC224 47UF/6.3V s_c0805_h57
HC225 47UF/6.3V s_c0805_h57
HC226 47UF/6.3V s_c0805_h57
HC227 47UF/6.3V s_c0805_h57
HC228 47UF/6.3V s_c0805_h57
GND

ASUSTek COMPUTER INC.	**Title :** CPU CAPS **Engineer:** Shawn Yu	
Size A1	Project Name MIX-EHLD1	Rev R1.01
Date: Thursday, July 15, 2021	Sheet 25 of 90	



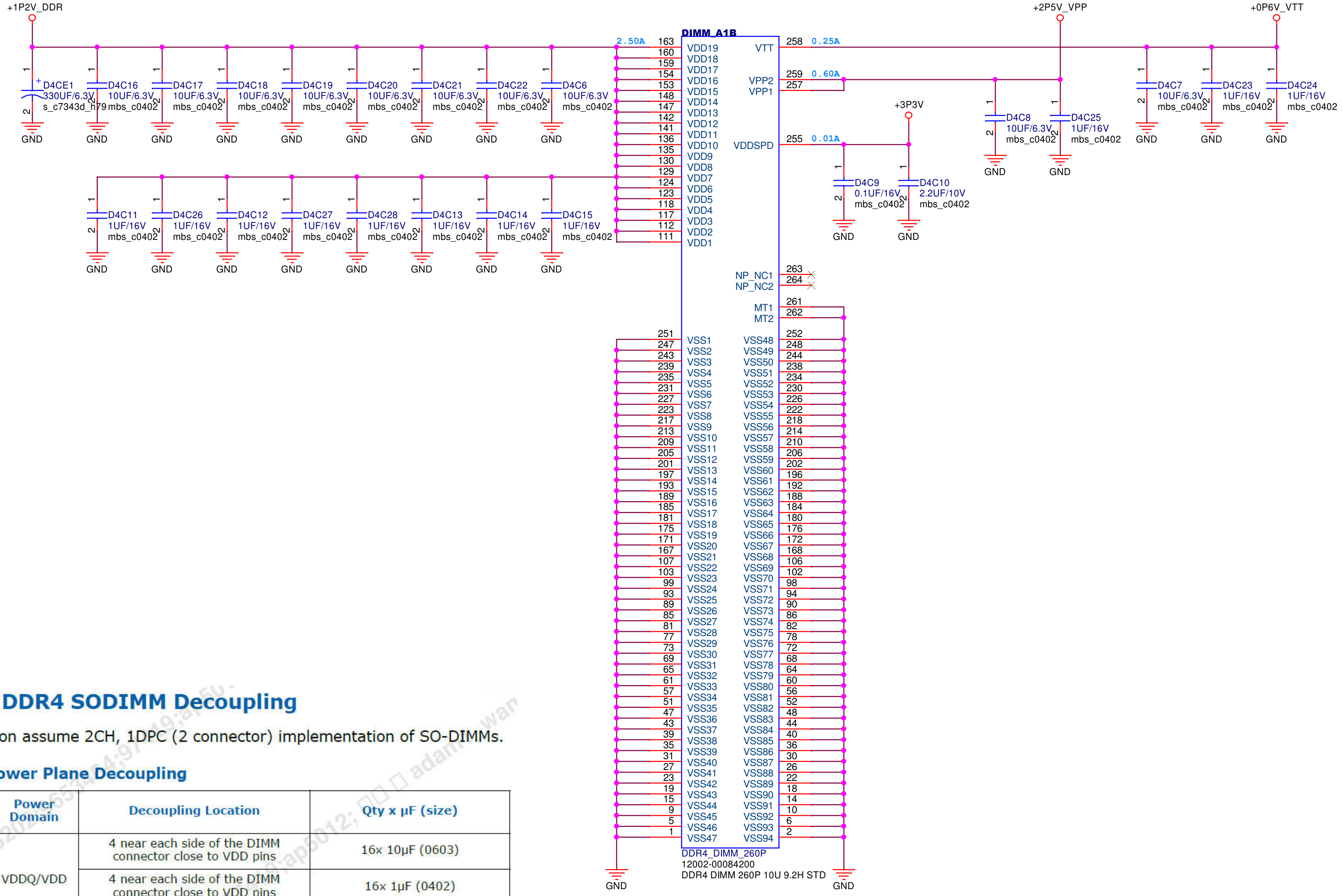
ASUSTek COMPUTER INC.

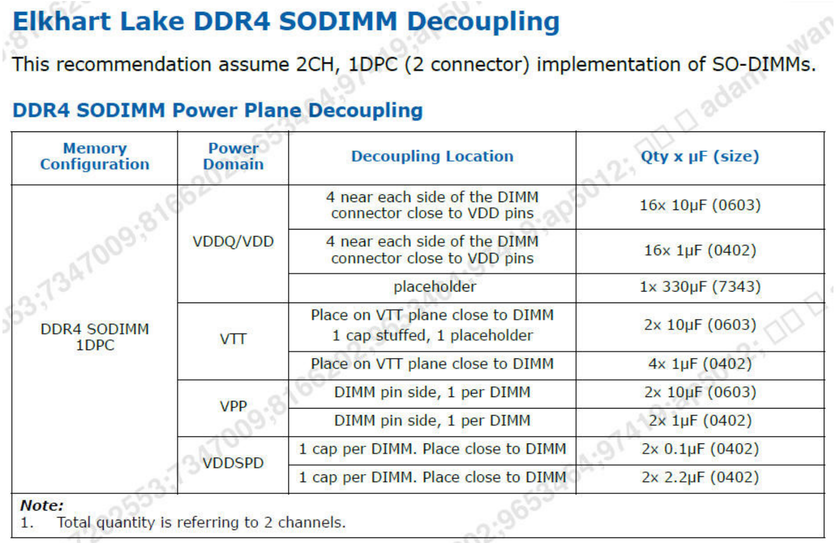
Title : **DDR4 SODIMM CH0 9.2H**

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 26 of 90





Elkhart Lake DDR4 SODIMM Decoupling

This recommendation assume 2CH, 1DPC (2 connector) implementation of SO-DIMMs.

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	1 cap per DIMM. Place close to DIMM	2x 0.1µF (0402)
		1 cap per DIMM. Place close to DIMM	2x 2.2µF (0402)

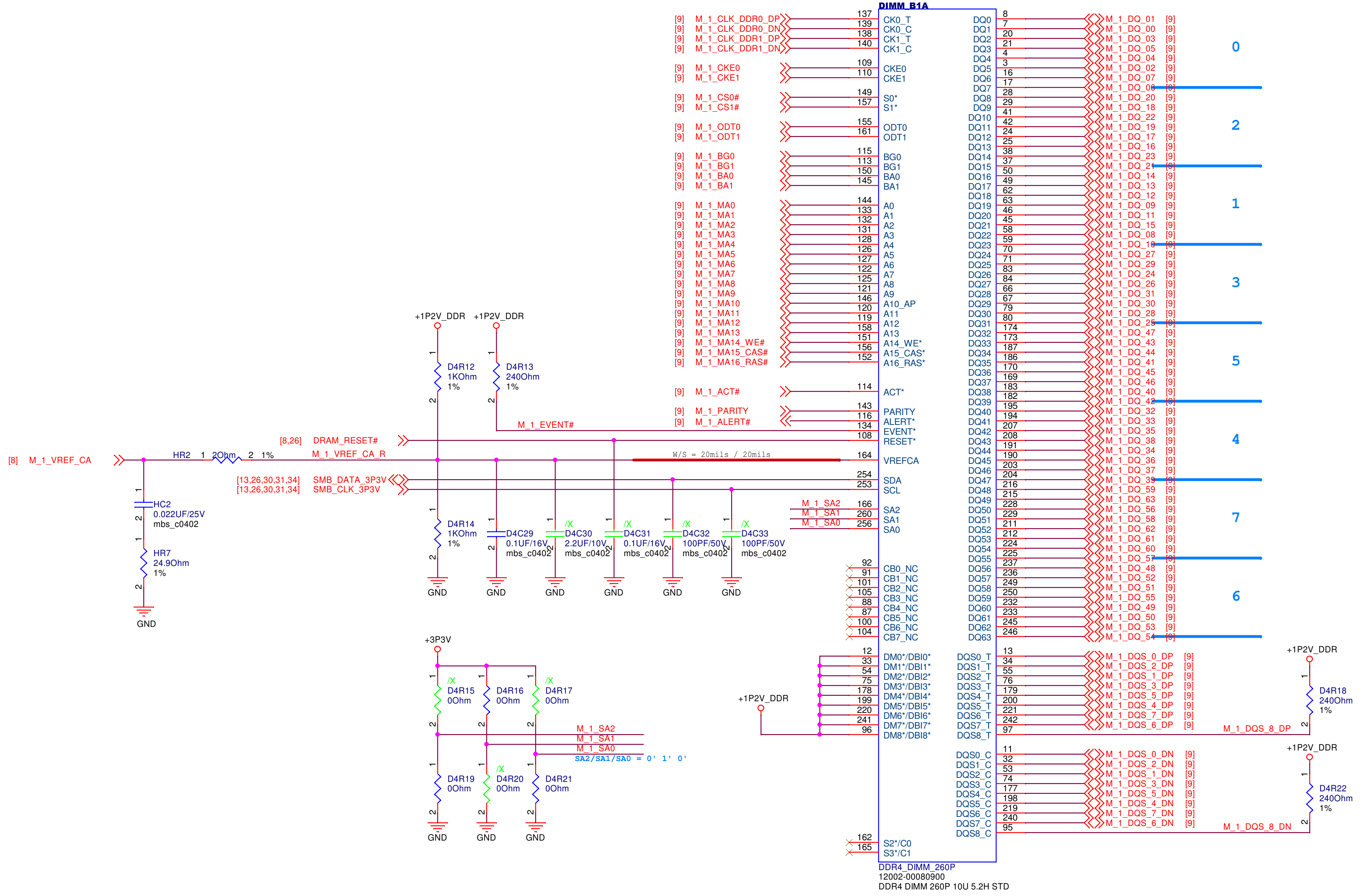
Note:
1. Total quantity is referring to 2 channels.

ASUSTek COMPUTER INC.

Title : DDR4 SODIMM CH0 PWF

Engineer: Shawn Yu

Size: A3
Project Name: MIX-EHLD1
Rev: R1.01
Date: Thursday, July 15, 2021



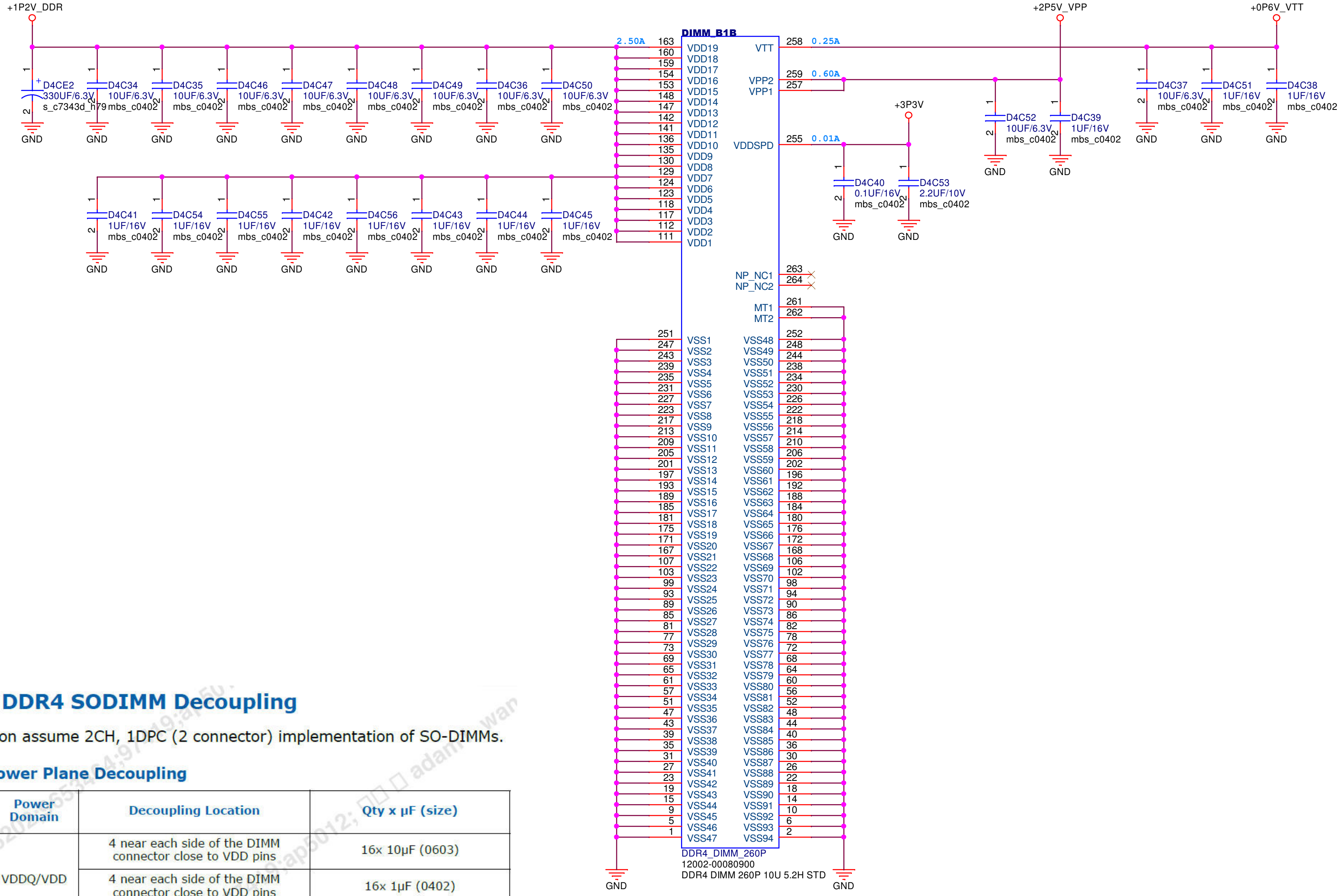
ASUSTek COMPUTER INC.

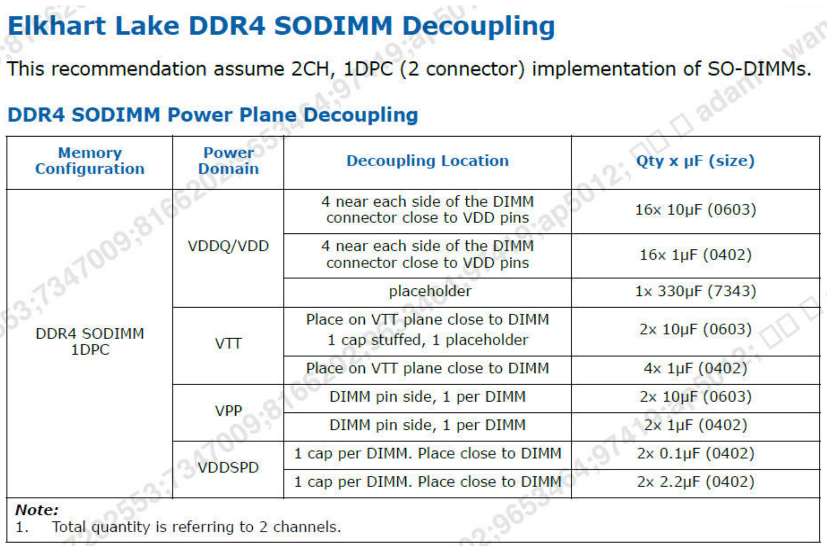
Title : DDR4 SODIMM CH1 5.2H

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 28 of 90





Elkhart Lake DDR4 SODIMM Decoupling

This recommendation assume 2CH, 1DPC (2 connector) implementation of SO-DIMMs.

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	1 cap per DIMM. Place close to DIMM	2x 0.1µF (0402)
		1 cap per DIMM. Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

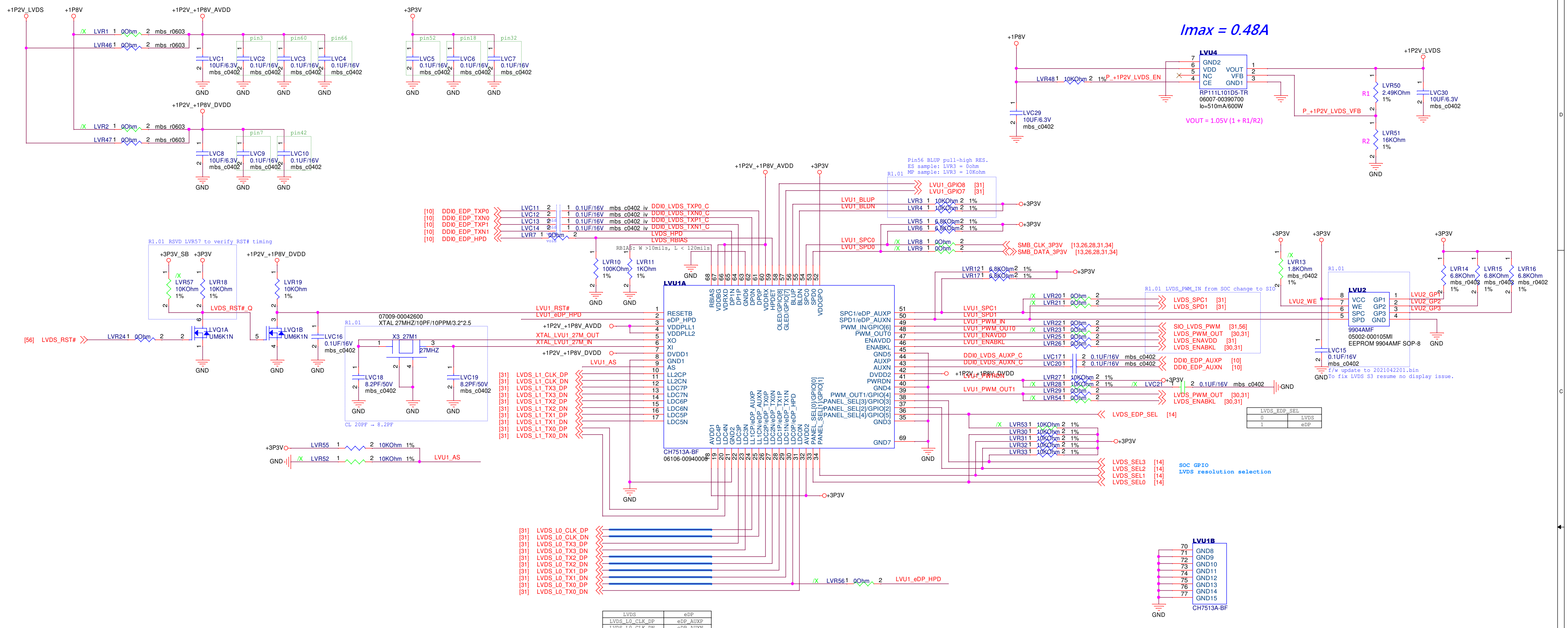
ASUSTek COMPUTER INC.

Title : DDR4 SODIMM CH1 PWR

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 29 of 90



LVDS	eDP
LVDS_L0_CLK_DP	eDP_AUXP
LVDS_L0_CLK_DN	eDP_AUXN
LVDS_L0_TX2_DP	eDP_TX0P
LVDS_L0_TX2_DN	eDP_TX0N
LVDS_L0_TX1_DP	eDP_TX1P
LVDS_L0_TX1_DN	eDP_TX1N
LVDS_L0_TX0_DP	eDP_HPD

LVDS_EDP_SEL	
0	LVDS
1	eDP

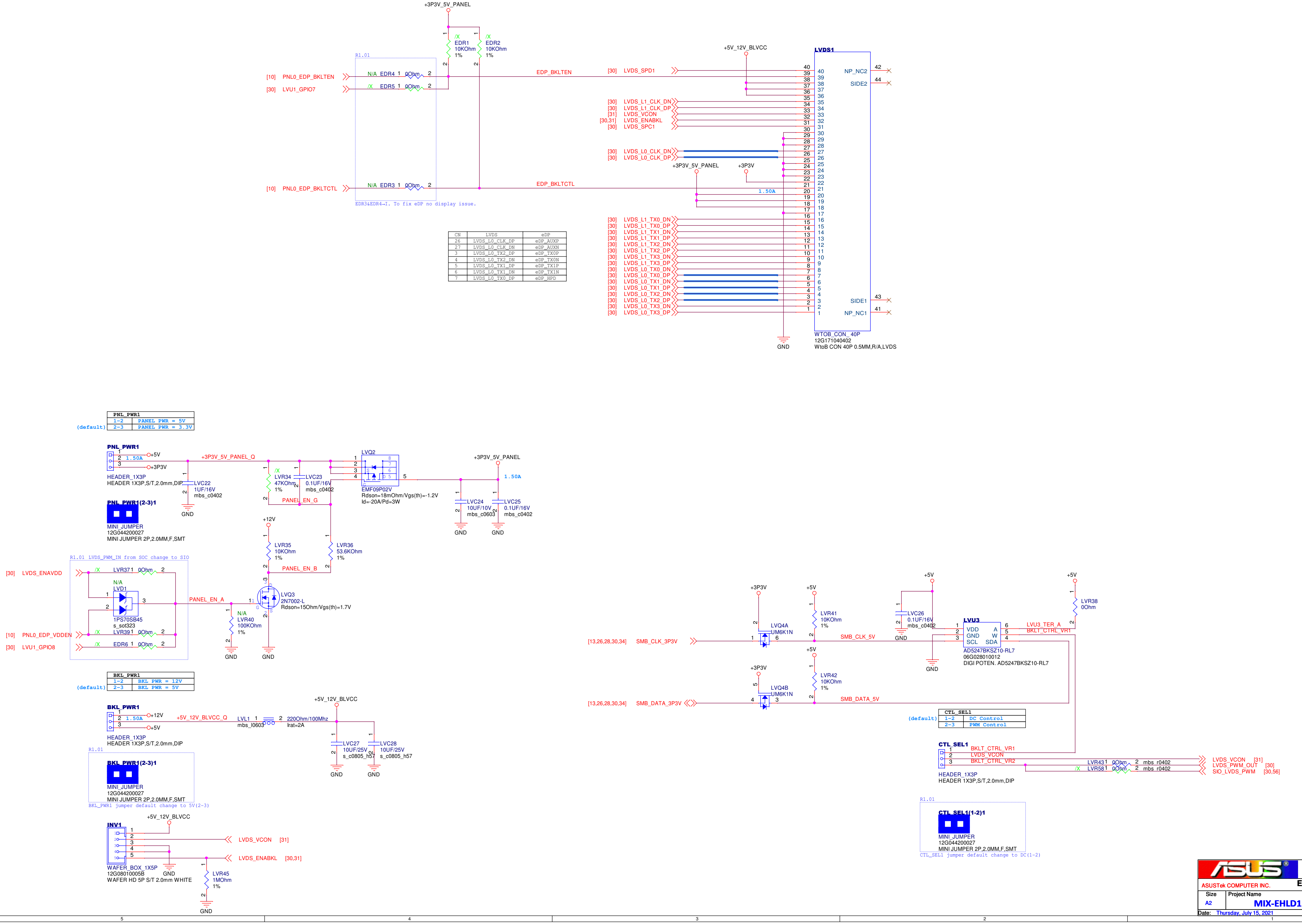
ASUSTek COMPUTER INC.

Title : DDI0 eDP to LVDS CH7513B-BF

Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 30 of 90



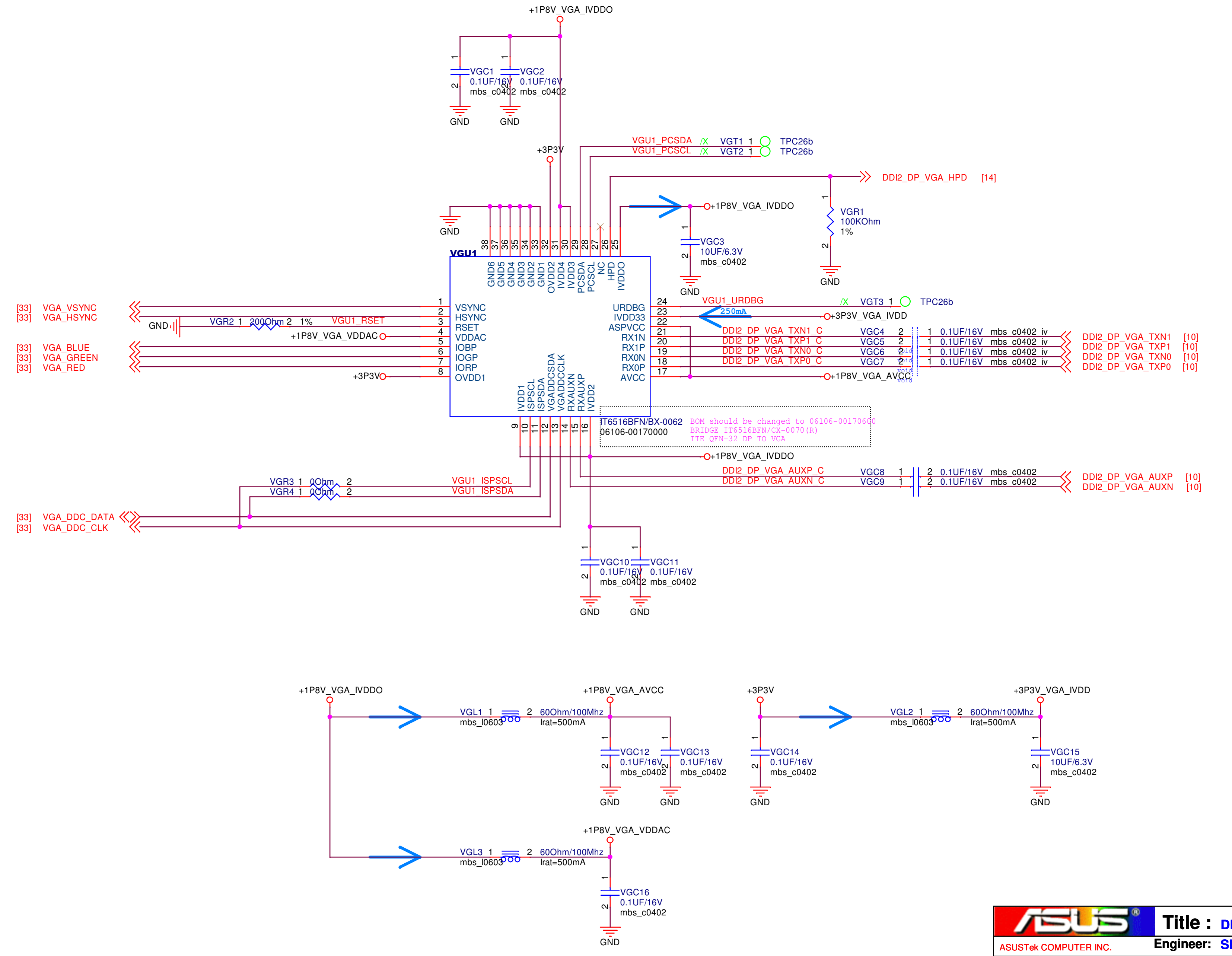
CN	LVDS	eDP
26	LVDS_L0_CLK_DP	eDP_AUXP
27	LVDS_L0_CLK_DN	eDP_AUXN
3	LVDS_L0_TX2_DP	eDP_TX0P
4	LVDS_L0_TX2_DN	eDP_TX0N
5	LVDS_L0_TX1_DP	eDP_TX1P
6	LVDS_L0_TX1_DN	eDP_TX1N
7	LVDS_L0_TX0_DP	eDP_HPD

	PNL_PWR1	
	1-2	PANEL PWR = 5V
(default)	2-3	PANEL PWR = 3.3V

	BKL_PWR1	
	1-2	BKL PWR = 12V
(default)	2-3	BKL PWR = 5V

	CTL_SEL1	
(default)	1-2	DC Control
	2-3	PWM Control

Title : DDI0 eDP/LVDS CON
ASUSTek COMPUTER INC.
Engineer: Shawn Yu
Size A2
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
Sheet 31 of 90



BOM should be changed to 06106-00170600
BRIDGE IT6516BFN/CX-0070(R)
ITE QFN-32 DP TO VGA

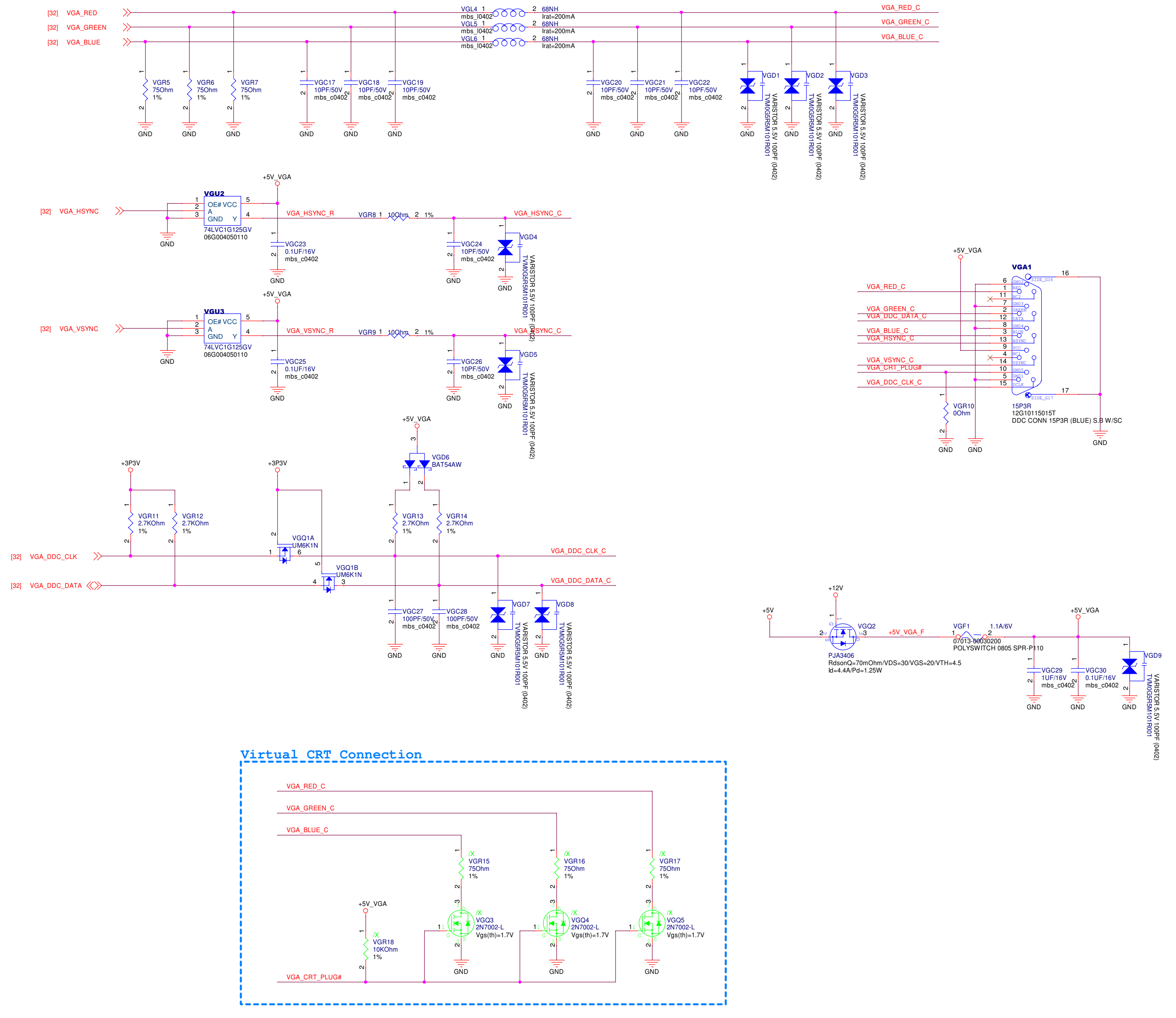
Title : DDI2 DP to VGA IT6516B

ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 32 of 90


[32] VGA_RED
[32] VGA_GREEN
[32] VGA_BLUE
VGL4 68NH mbs_l0402 Irat=200mA
VGL5 68NH mbs_l0402 Irat=200mA
VGL6 68NH mbs_l0402 Irat=200mA
VGA_RED_C
VGA_GREEN_C
VGA_BLUE_C
VGR5 75Ohm 1%
VGR6 75Ohm 1%
VGR7 75Ohm 1%
VGC17 10PF/50V mbs_c0402
VGC18 10PF/50V mbs_c0402
VGC19 10PF/50V mbs_c0402
VGC20 10PF/50V mbs_c0402
VGC21 10PF/50V mbs_c0402
VGC22 10PF/50V mbs_c0402
VGD1 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
VGD2 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
VGD3 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
GND
+5V_VGA
VGU2 74LVC1G125GV 06G004050110
OE# VCC A GND Y
[32] VGA_HSYNC
VGA_HSYNC_R
VGR8 10Ohm 1%
VGA_HSYNC_C
VGC23 0.1UF/16V mbs_c0402
VGC24 10PF/50V mbs_c0402
VGD4 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
VGU3 74LVC1G125GV 06G004050110
[32] VGA_VSYNC
VGA_VSYNC_R
VGR9 10Ohm 1%
VGA_VSYNC_C
VGC25 0.1UF/16V mbs_c0402
VGC26 10PF/50V mbs_c0402
VGD5 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
VGD6 BAT54AW
+3P3V
VGR11 2.7KOhm 1%
VGR12 2.7KOhm 1%
VGR13 2.7KOhm 1%
VGR14 2.7KOhm 1%
VGQ1A UM6K1N
VGQ1B UM6K1N
[32] VGA_DDC_CLK
[32] VGA_DDC_DATA
VGA_DDC_CLK_C
VGA_DDC_DATA_C
VGC27 100PF/50V mbs_c0402
VGC28 100PF/50V mbs_c0402
VGD7 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
VGD8 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
VGA1
15P3R 12G10115015T DDC CONN 15P3R (BLUE) S.B W/SC
VGA_RED_C
VGA_GREEN_C
VGA_DDC_DATA_C
VGA_BLUE_C
VGA_HSYNC_C
VGA_VSYNC_C
VGA_CRT_PLUG#
VGA_DDC_CLK_C
VGR10 0Ohm
+12V
+5V
VGQ2 PJA3406 RdsonQ=70mOhm/VDS=30/VGS=20/VTH=4.5 Id=4.4A/Pd=1.25W
+5V_VGA_F
VGF1 1.1A/6V 07013-00030200 POLYSWITCH 0805 SPR-P110
VGC29 1UF/16V mbs_c0402
VGC30 0.1UF/16V mbs_c0402
VGD9 VARISTOR 5.5V 100PF (0402) TVM0G5R5M101R001
Virtual CRT Connection
VGA_RED_C
VGA_GREEN_C
VGA_BLUE_C
VGR15 75Ohm 1%
VGR16 75Ohm 1%
VGR17 75Ohm 1%
VGQ3 2N7002-L Vgs(th)=1.7V
VGQ4 2N7002-L Vgs(th)=1.7V
VGQ5 2N7002-L Vgs(th)=1.7V
VGR18 10KOhm 1%
VGA_CRT_PLUG#

ASUSTek COMPUTER INC.

Title : DDI2 VGA CON

Engineer: Shawn Yu

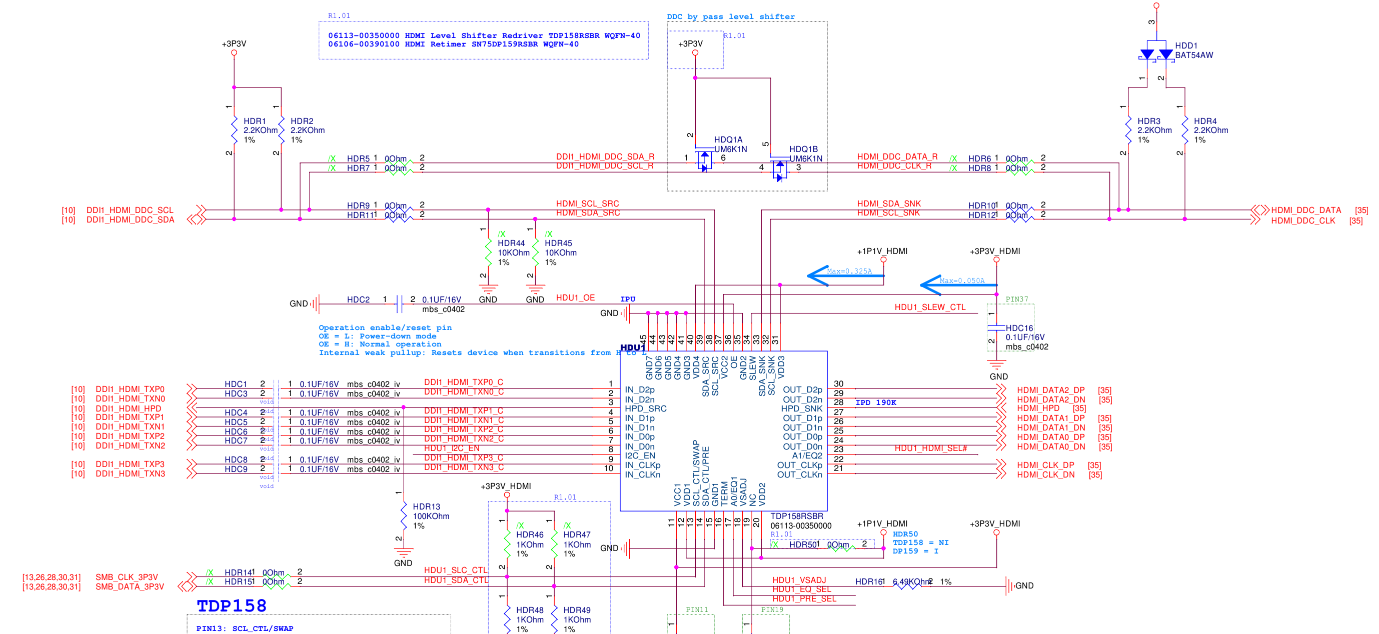
Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 33 of 90

HDMI Level Shifter Redriver TDP158 Co-Lay HDMI Retimer SN75DP159RSBR

R1.01

06113-00350000 HDMI Level Shifter Redriver TDP158RSBR WQFN-40
06106-00390100 HDMI Retimer SN75DP159RSBR WQFN-40

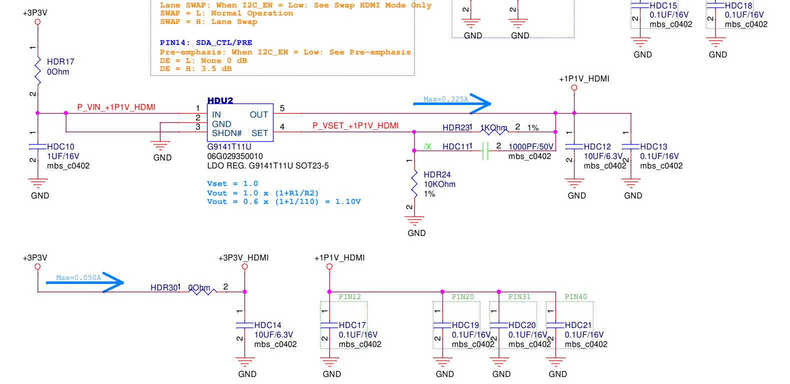


Operation enable/reset pin
OE = L: Power-down mode
OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

TDP158

PIN13: SCL_CTL/SWAP
Lane SWAP: When I2C_EN = Low: See Swap HDMI Mode Only
SWAP = L: Normal Operation
SWAP = H: Lane Swap

PIN14: SDA_CTL/PRE
Pre-emphasis: When I2C_EN = Low: See Pre-emphasis
DE = L: None 0 dB
DE = H: 3.5 dB


+3P3V
HDR17 0Ohm
P_VIN_+1P1V_HDMI
HDC10 1UF/16V mbs_c0402
HDU2
IN OUT
GND
SHDN# SET
G9141T11U
06G029350010
LDO REG. G9141T11U SOT23-5
Max=0.325A
+1P1V_HDMI
P_VSET_+1P1V_HDMI
HDR23 1KOhm 1%
HDC11 1000PF/50V mbs_c0402
HDR24 10KOhm 1%
HDC12 10UF/6.3V mbs_c0402
HDC13 0.1UF/16V mbs_c0402
+3P3V
Max=0.050A
HDR30 0Ohm
+3P3V_HDMI
HDC14 10UF/6.3V mbs_c0402
PIN12
HDC17 0.1UF/16V mbs_c0402
PIN20
HDC19 0.1UF/16V mbs_c0402
PIN31
HDC20 0.1UF/16V mbs_c0402
PIN40
HDC21 0.1UF/16V mbs_c0402
GND

Vset = 1.0
Vout = 1.0 x (1+R1/R2)
Vout = 0.6 x (1+1/110) = 1.10V

R1.01 **TDP158**	R1.01 **SN75DP159RSBR**
PIN08: I2C_EN I2C_EN = High; Puts Device into I2C Control Mode I2C_EN = Low; Puts Device into Pin Strap Mode /X HDR18 1KOhm 1% +3P3V_HDMI HDU1_I2C_EN HDR25 1KOhm 1% GND	**PIN08: I2C_EN/PIN** I2C_EN/PIN = High; puts device into I2C control mode I2C_EN/PIN = Low; puts device into pin strap mode ← default ※ PU or PD RES = 64.9Kohm for DP159

PIN17: A0/EQ1
I2C_EN = High, Address Bit 1 for I2C Programming
I2C_EN = Low, EQ1 Pin Setting,
Works in conjunction with A1/EQ2; See Main Link Inputs for settings.
For pin control,
Low = 1 kΩ pulldown resistor to GND,
High = 1 kΩpullup resistor to VCC,
NC = Floating.
/X HDR21 1KOhm 1% +3P3V_HDMI
HDU1_EQ_SEL
/X HDR28 1KOhm 1% GND
	PIN17: EQ_SEL/A0
	Input Receive Equalization pin strap when I2C_EN/PIN = Low
	EQ_SEL = L: Fixed EQ at 7.5 dB
	EQ_SEL = No Connect: Adaptive EQ ← default
	EQ_SEL = H: Fixed at 14 dB
	※ PU or PD RES = 64.9Kohm for DP159

PIN23: A1/EQ2 I2C_EN = High, Address Bit 2 for I2C Programming I2C_EN = Low, EQ2 Pin Setting, Works in conjunction with A0/EQ1; See Main Link Inputs for settings. For pin control, Low = 1 kΩ pulldown resistor to GND, High = 1 kΩpullup resistor to VCC, NC = Floating. /X HDR22 1KOhm 1% +3P3V_HDMI HDU1_HDMI_SEL# HDR29 1KOhm 1% GND	**PIN23: HDMI_SEL#/A1** HDMI_SEL when I2C_EN/PIN = Low HDMI_SEL = High: Device configured for DVI HDMI_SEL = Low: Device configured for HDMI ← default (Adaptor ID block is readable through I2C[4] or I2C-over-AUX.) ※ PU or PD RES = 64.9Kohm for DP159

PIN34: SLEW
Clock Slew Rate Control: See Slew Rate Control
SLEW = L: Slowest ~ 203 ps
SLEW = NC (Default): Mid-range 1 ~ 180 ps
SLEW = H: Fastest ~ 122 ps
For pin control,
L = 1 kΩ pulldown resistor to GND,
H = 1 kΩ pullup resistor to VCC,
NC = Floating.
/X HDR19 1KOhm 1% +3P3V_HDMI
HDU1_SLEW_CTL
/X HDR26 1KOhm 1% GND
	PIN34: SLEW_CTL
	Slew rate control when I2C_EN/PIN = Low.
	SLEW_CTL = H, fastest data rate
	SLEW_CTL = L, 5 ps slow
	SLEW_CTL = No Connect, 10 ps slow ← default
	※ PU or PD RES = 64.9Kohm for DP159

PIN16: TERM
Source Termination Cotnrol: See Transmitter Impedance Control
TERM = H, 75 Ω ~ 150 Ω
TERM = L, Transmit Termination impedance in 150 Ω ~ 300 Ω
TERM = NC, No transmit Termination
Note: When TMDS_CLOCK_RATIO_STATUS bit = 1 the TDP158 sets source termination to 75 Ω ~ 150 Ω Automatically
For pin control,
L = 1 kΩ pulldown resistor to GND,
H = 1 kΩ pullup resistor to VCC,
NC = Floating.
/X HDR20 1KOhm 1% +3P3V_HDMI
HDU1_PRE_SEL
/X HDR27 1KOhm 1% GND
	PIN16: PRE_SEL
	De-emphasis pin strap when I2C_EN/PIN = Low.
	PRE_SEL = L: - 2 dB de-emphasis
	PRE_SEL = No Connect: 0 dB ← default
	PRE_SEL = H: Reserved
	※ PU or PD RES = 64.9Kohm for DP159

ASUSTek COMPUTER INC.
Title : DDI1 HDMI ALS SN75DP159
Engineer: Shawn Yu
Size A2
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
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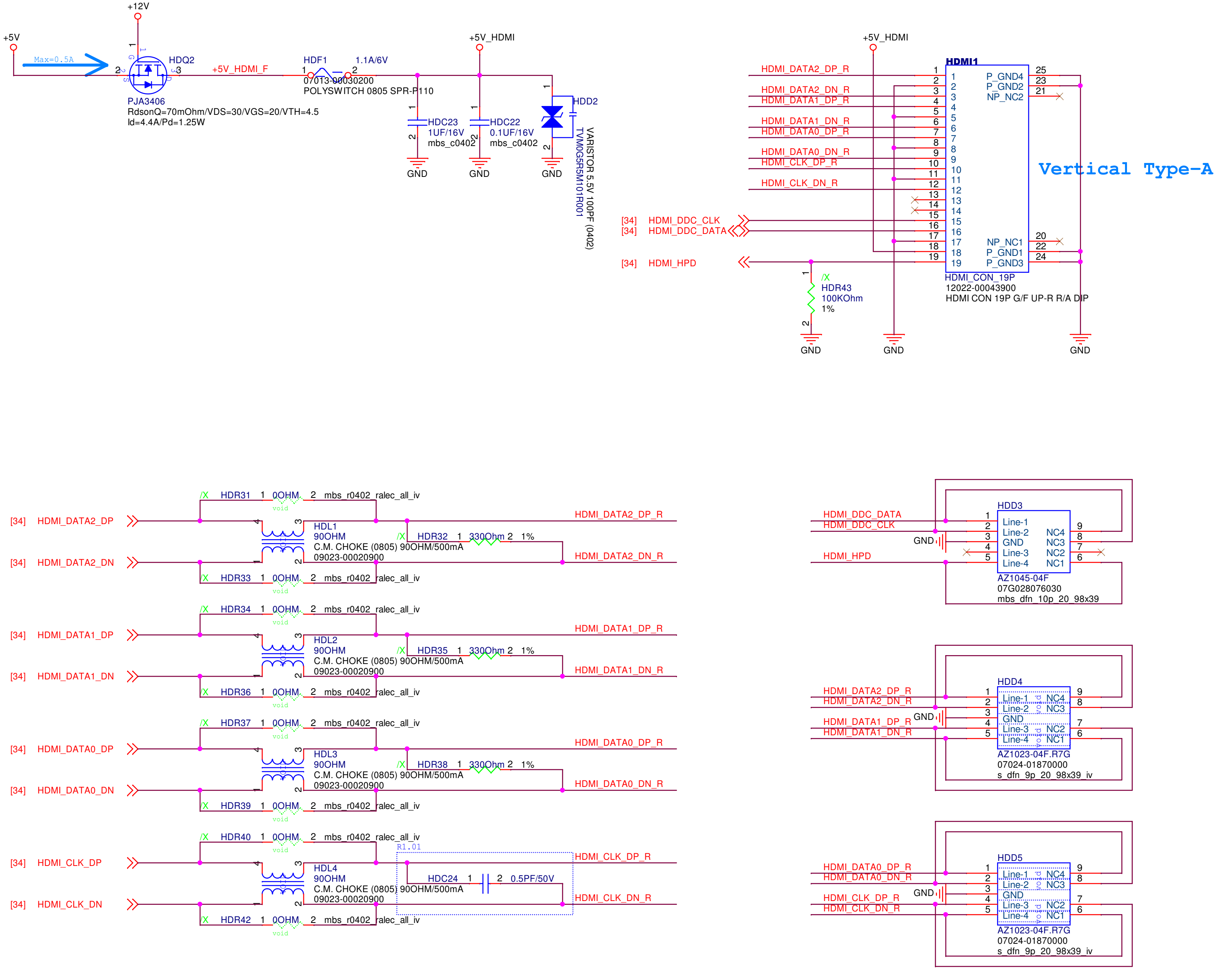

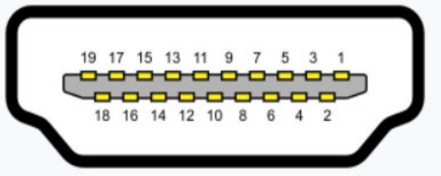

HDMI type A receptacle

Pin 1	TMDS Data2+
Pin 2	TMDS Data2 Shield
Pin 3	TMDS Data2−
Pin 4	TMDS Data1+
Pin 5	TMDS Data1 Shield
Pin 6	TMDS Data1−
Pin 7	TMDS Data0+
Pin 8	TMDS Data0 Shield
Pin 9	TMDS Data0−
Pin 10	TMDS Clock+
Pin 11	TMDS Clock Shield
Pin 12	TMDS Clock−
Pin 13	CEC
Pin 14	Reserved (HDMI 1.0–1.3a) Utility/HEAC+ (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)
Pin 15	SCL (I²C serial clock for DDC)
Pin 16	SDA (I²C serial data for DDC)
Pin 17	Ground (for DDC, CEC, ARC, and HEC)
Pin 18	+5 V (min. 0.055 A)[3]
Pin 19	Hot Plug Detect (all versions) HEAC− (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)

ASUSTek COMPUTER INC.

Title : DDI1 HDMI CON

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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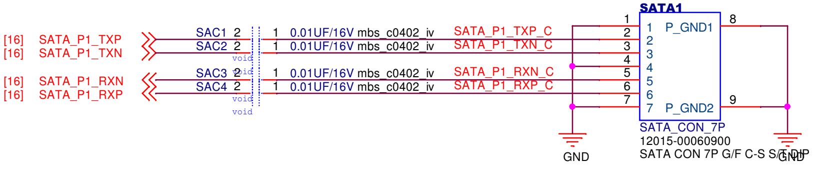
SATA CON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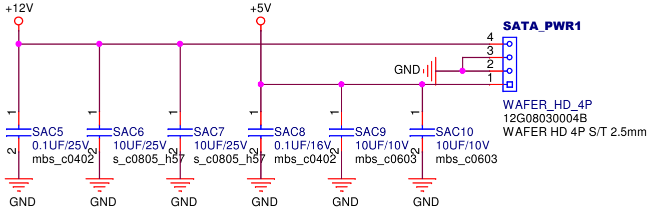
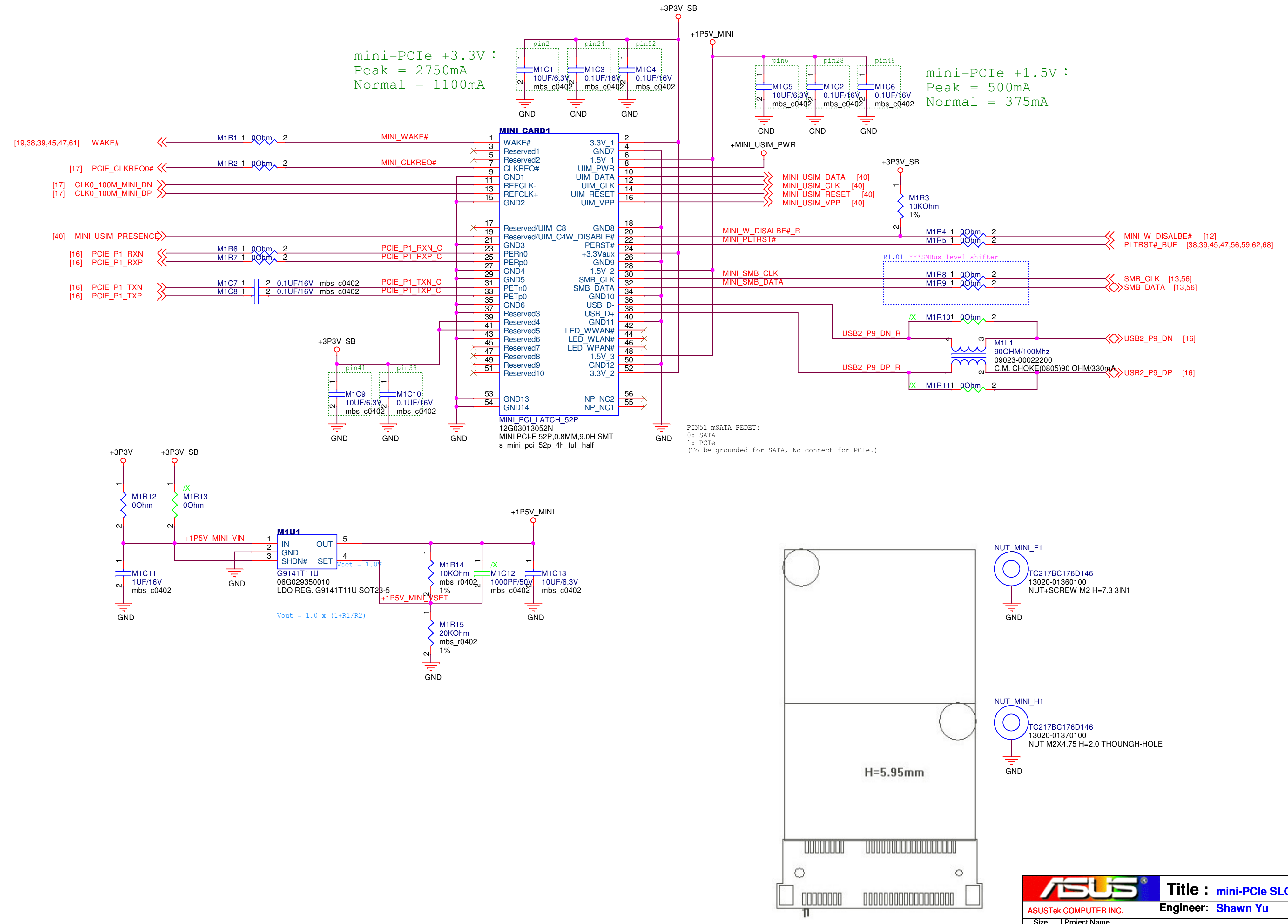

5V / 12V @1.5A

Title : SATA CON
ASUSTek COMPUTER INC.
Engineer: Shawn Yu
Size A3
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
Sheet 36 of 90



ASUSTek COMPUTER INC.

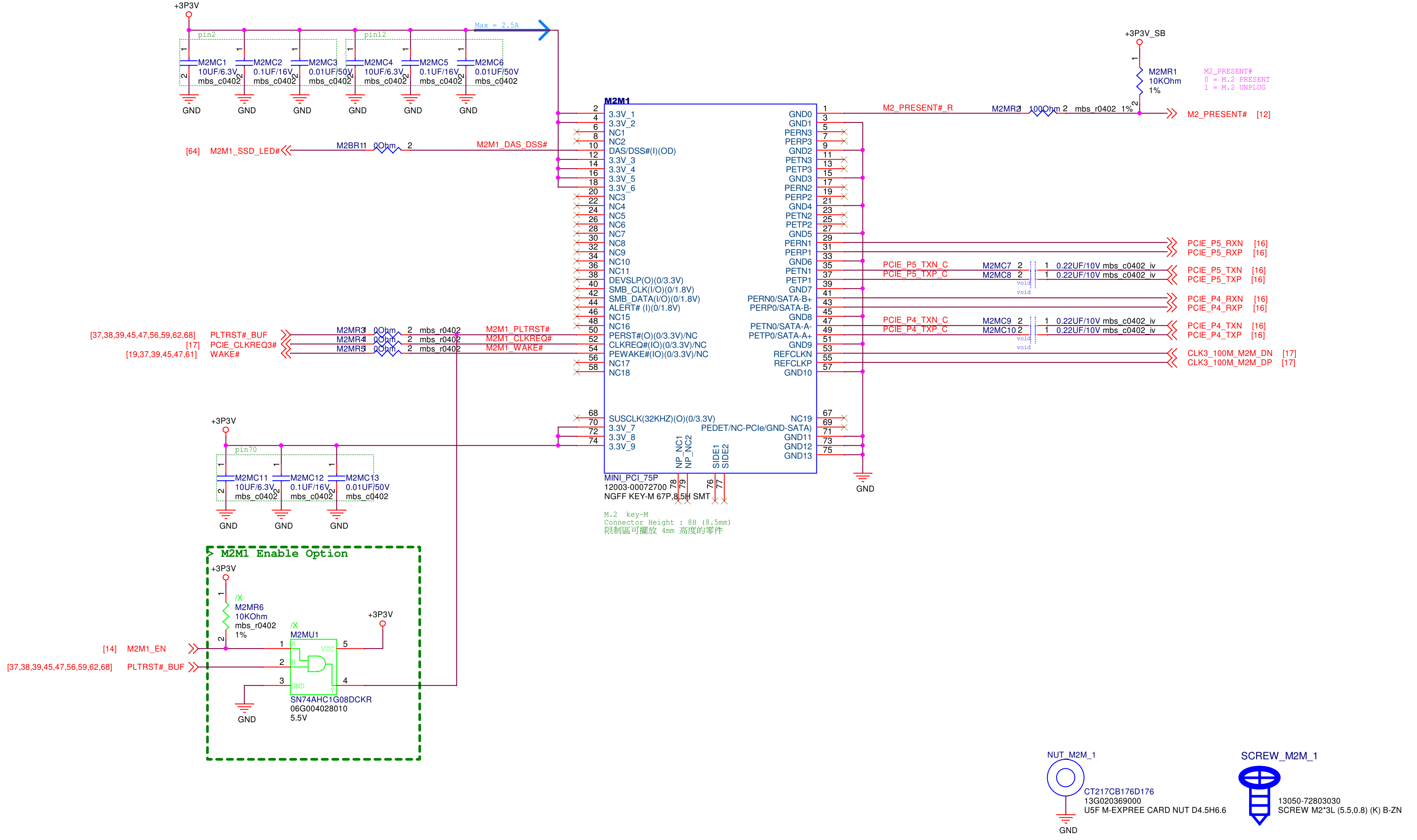
Title : mini-PCIe SLOT

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 37 of 90

M.2 KEY-M 2280 (PCIE x2 NVME)



ASUSTek COMPUTER INC.

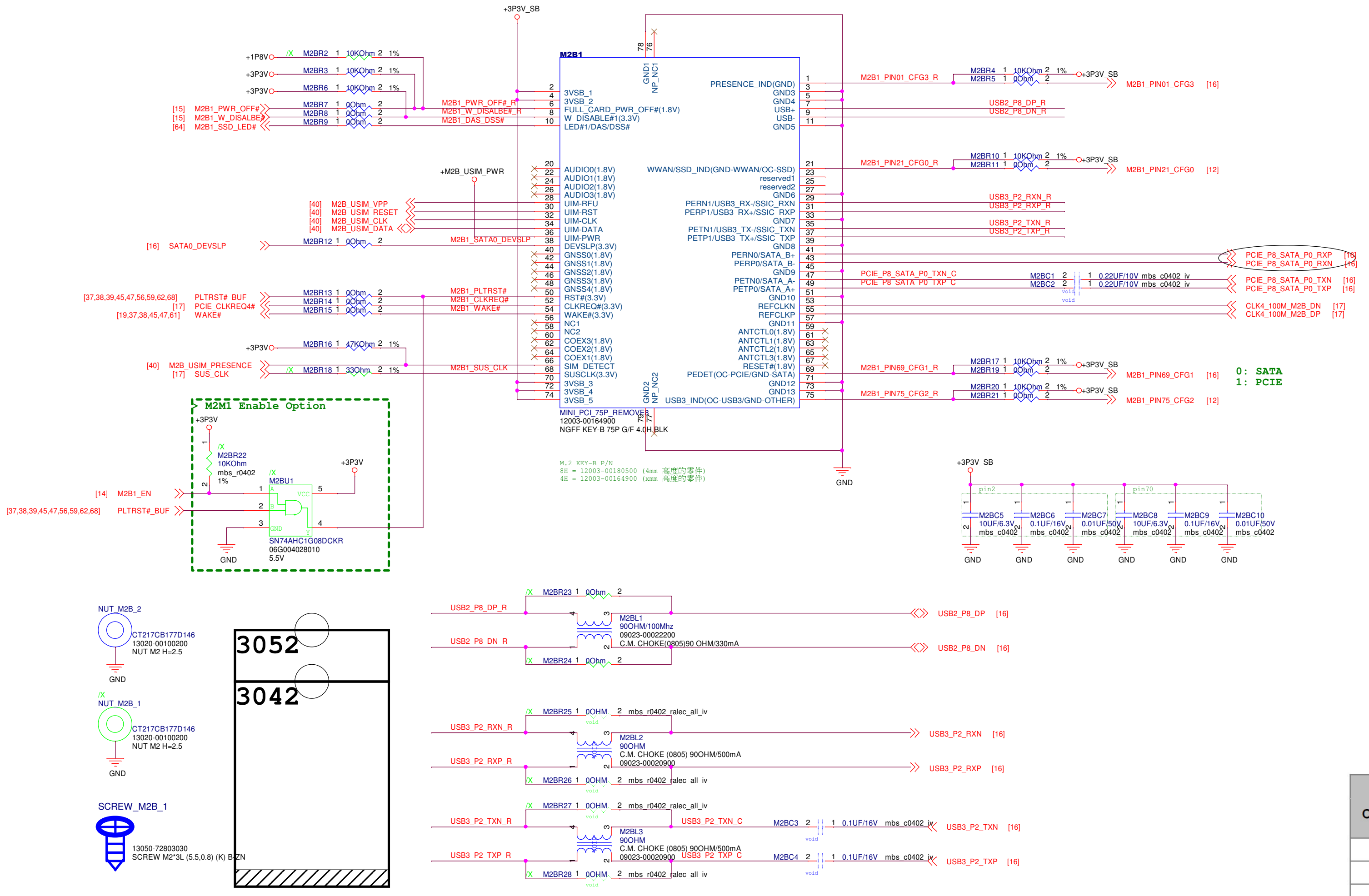
Title : **M.2 KEY-M 2280**

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

Date: Thursday, July 15, 2021 Sheet 38 of 90

M.2 KEY-B 3042/3052



Socket 2 Module Configuration Table

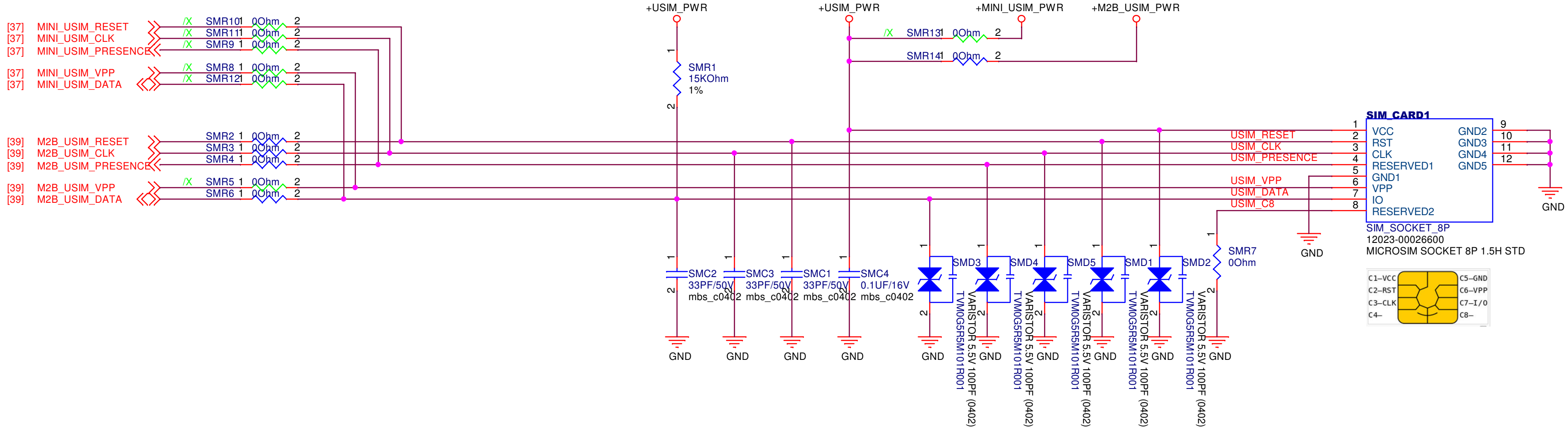
Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
1	0	1	1	RFU	N/A
1	1	1	1	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
[2] Applicable to WWAN only

Title : M.2 KEY-B 3042/3052
ASUSTek COMPUTER INC.
Engineer: Shawn Yu
Size A2
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
Sheet 39 of 90

MICRO SIM SOCKET

USIM support mini-PCIE & M.2 KEY-B solt by BOM option.
Default = M.2 KEY-B



ASUSTek COMPUTER INC.

Title : SIM CARD SLOT

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021
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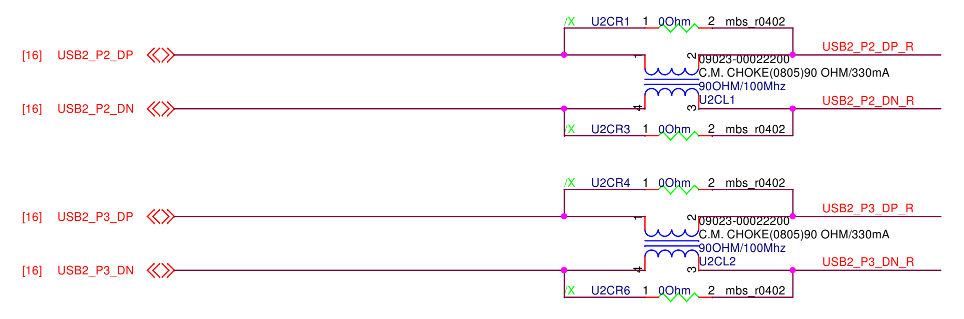
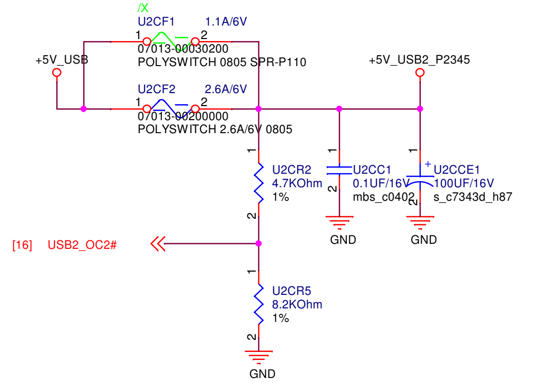
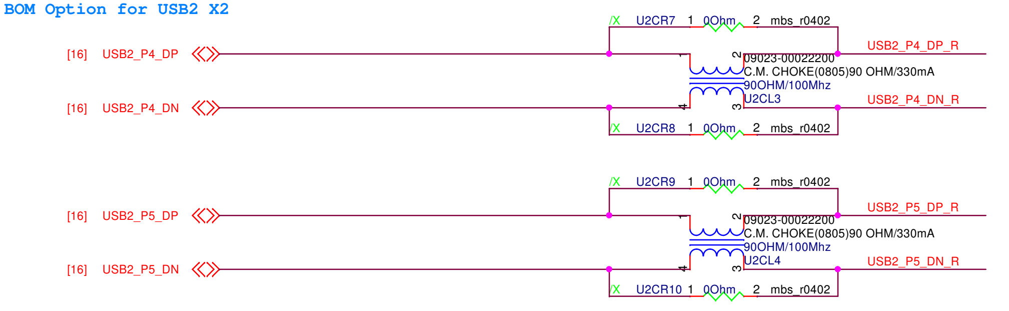
USB2.0 REAR CON

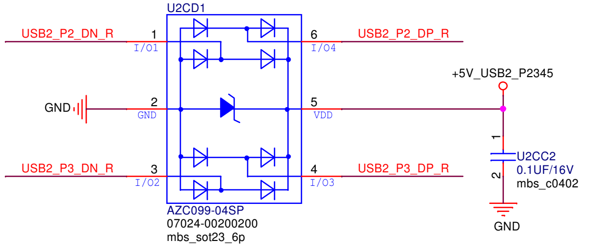




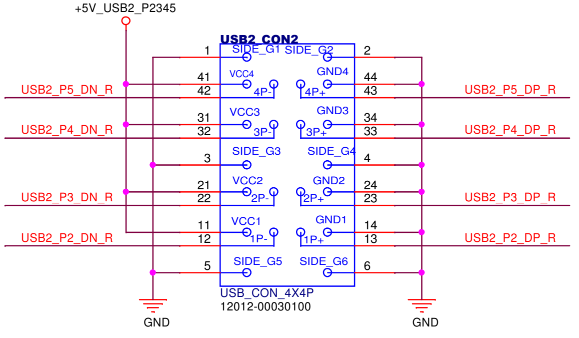
BOM Option for USB2 X2



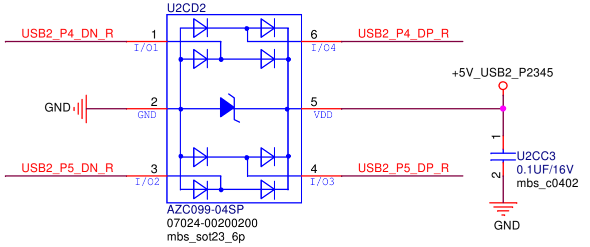
BOM Option for USB2 X2



BOM Option for USB2 X4


+5V_USB2_P2345
USB2_CON2
SIDE_G1 1
SIDE_G2 2
USB2_P5_DN_R 41 VCC4 42 4P-
GND4 44 4P+ 43 USB2_P5_DP_R
USB2_P4_DN_R 31 VCC3 32 3P-
GND3 34 3P+ 33 USB2_P4_DP_R
SIDE_G3 3
SIDE_G4 4
USB2_P3_DN_R 21 VCC2 22 2P-
GND2 24 2P+ 23 USB2_P3_DP_R
USB2_P2_DN_R 11 VCC1 12 1P-
GND1 14 1P+ 13 USB2_P2_DP_R
SIDE_G5 5
SIDE_G6 6
USB_CON_4X4P
12012-00030100
GND
GND

BOM Option for USB2 X2



Title : USB2.0 REAR CON
ASUSTek COMPUTER INC.
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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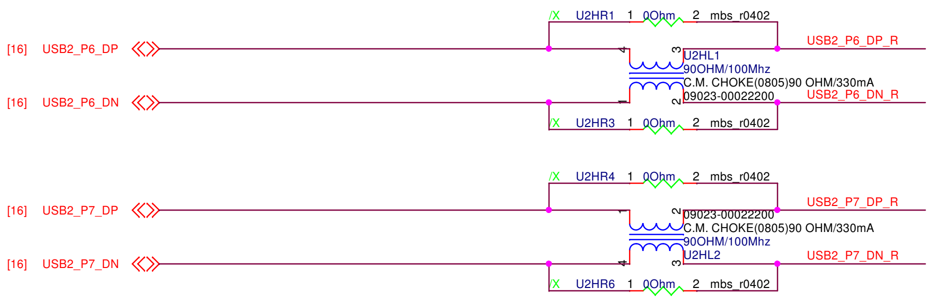
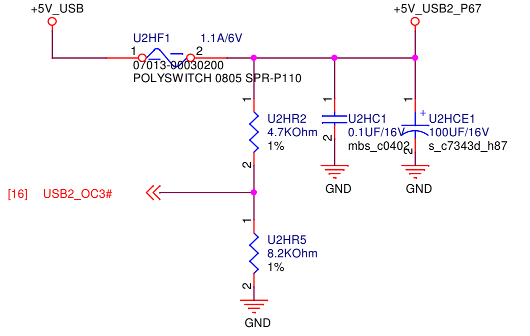
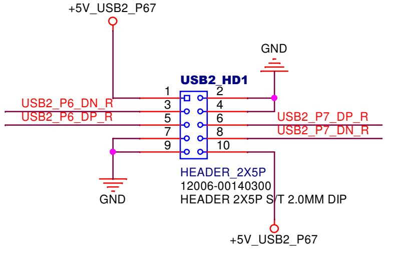
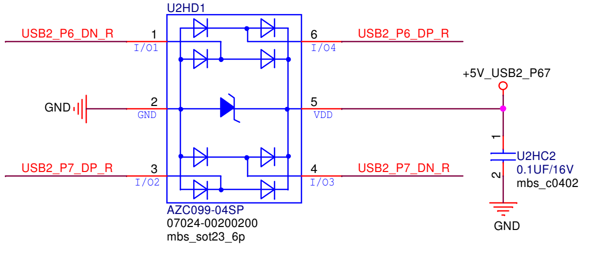
USB2.0 FRONT HD









Title : USB2.0 FRONT HD

ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size A3

Project Name **MIX-EHLD1**

Rev R1.01

Date: Thursday, July 15, 2021

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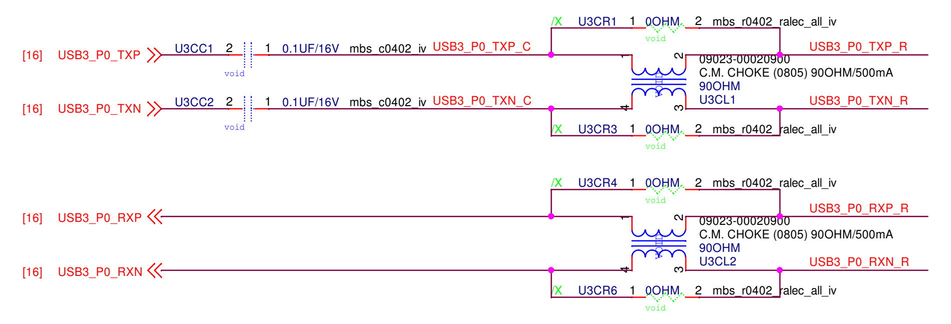
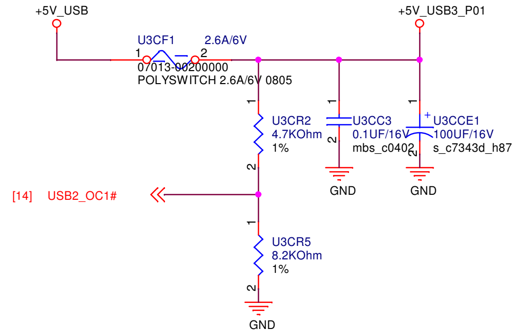
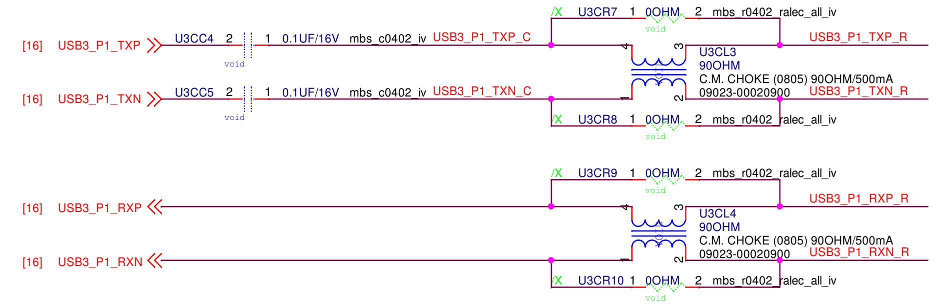
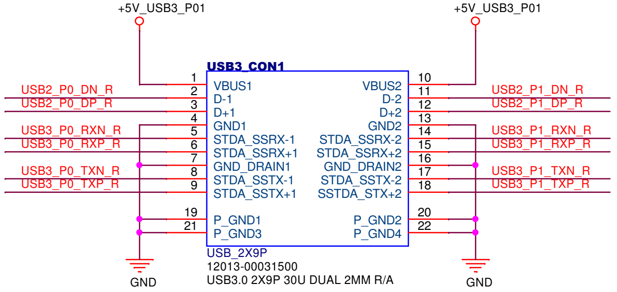
USB3.1 GEN1 REAR CON


[16] USB3_P0_TXP
U3CC1 2 1 0.1UF/16V mbs_c0402_iv
void
USB3_P0_TXP_C
/X U3CR1 1 0OHM 2 mbs_r0402_ralec_all_iv
void
USB3_P0_TXP_R
09023-00020900
C.M. CHOKE (0805) 90OHM/500mA
90OHM
U3CL1
[16] USB3_P0_TXN
U3CC2 2 1 0.1UF/16V mbs_c0402_iv
void
USB3_P0_TXN_C
USB3_P0_TXN_R
/X U3CR3 1 0OHM 2 mbs_r0402_ralec_all_iv
void
/X U3CR4 1 0OHM 2 mbs_r0402_ralec_all_iv
void
[16] USB3_P0_RXP
USB3_P0_RXP_R
09023-00020900
C.M. CHOKE (0805) 90OHM/500mA
90OHM
U3CL2
[16] USB3_P0_RXN
USB3_P0_RXN_R
/X U3CR6 1 0OHM 2 mbs_r0402_ralec_all_iv
void

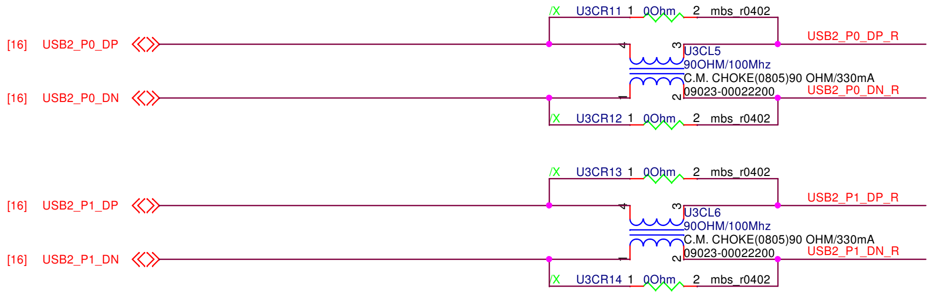


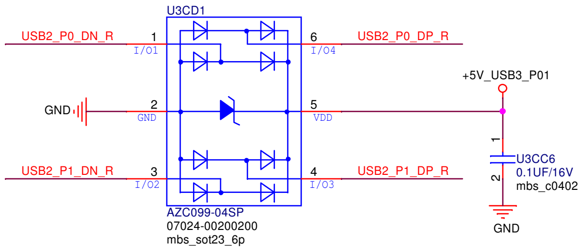

/X U3CR7 1 0OHM 2 mbs_r0402_ralec_all_iv
void
[16] USB3_P1_TXP
U3CC4 2 1 0.1UF/16V mbs_c0402_iv
void
USB3_P1_TXP_C
USB3_P1_TXP_R
U3CL3
90OHM
C.M. CHOKE (0805) 90OHM/500mA
09023-00020900
[16] USB3_P1_TXN
U3CC5 2 1 0.1UF/16V mbs_c0402_iv
void
USB3_P1_TXN_C
USB3_P1_TXN_R
/X U3CR8 1 0OHM 2 mbs_r0402_ralec_all_iv
void
/X U3CR9 1 0OHM 2 mbs_r0402_ralec_all_iv
void
[16] USB3_P1_RXP
USB3_P1_RXP_R
U3CL4
90OHM
C.M. CHOKE (0805) 90OHM/500mA
09023-00020900
[16] USB3_P1_RXN
USB3_P1_RXN_R
/X U3CR10 1 0OHM 2 mbs_r0402_ralec_all_iv
void

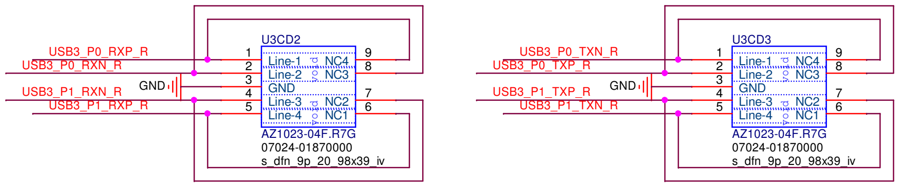


> Meet USB3.2 GEN2 connector

> Color: light blue







Title : USB3.1 GEN1 REAR CON

ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 43 of 90

USB3.2 GEN1 FRONT HD

D

C

B

A

Title : xxx

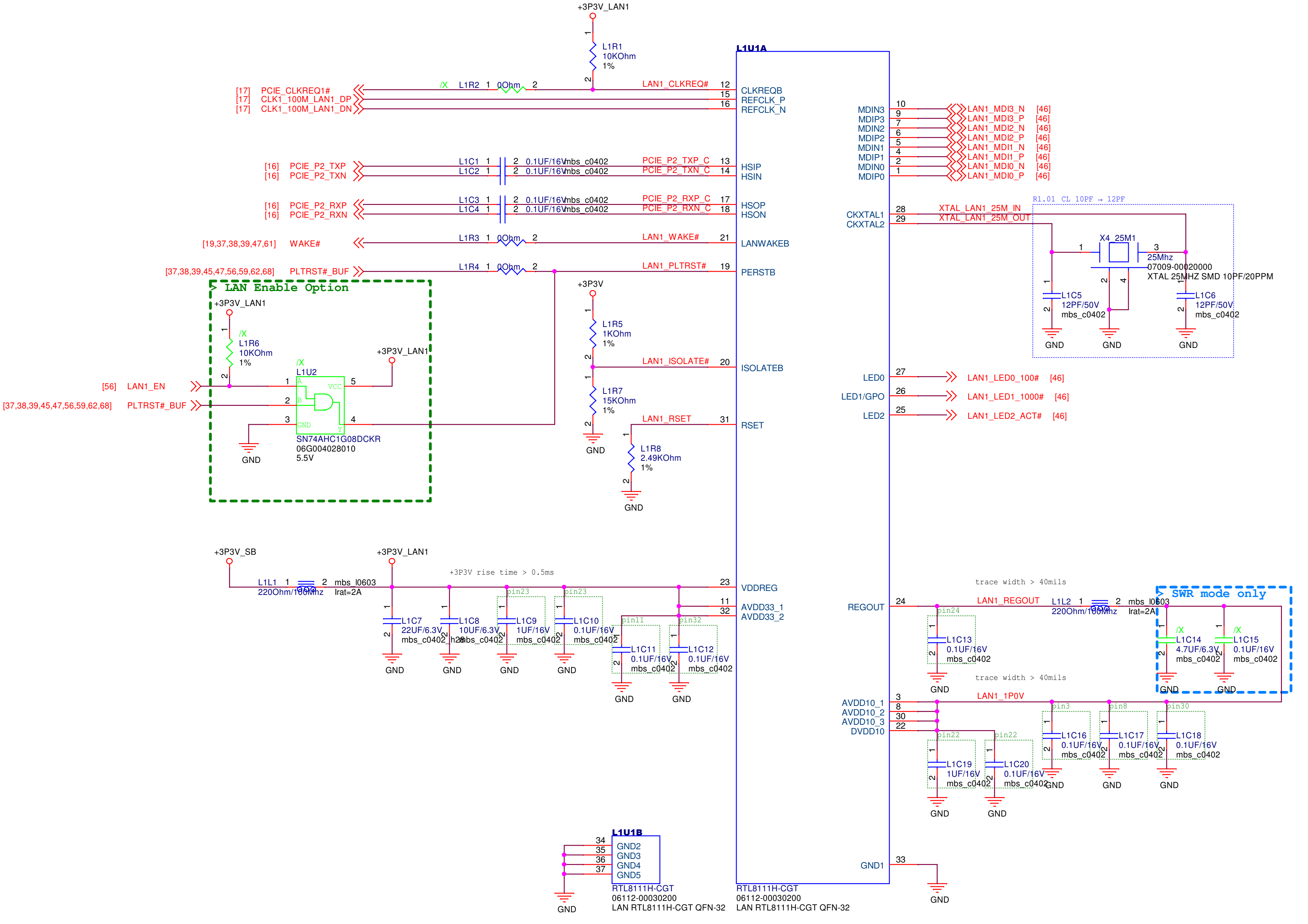
ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 44 of 90

LAN1 RTL8111H



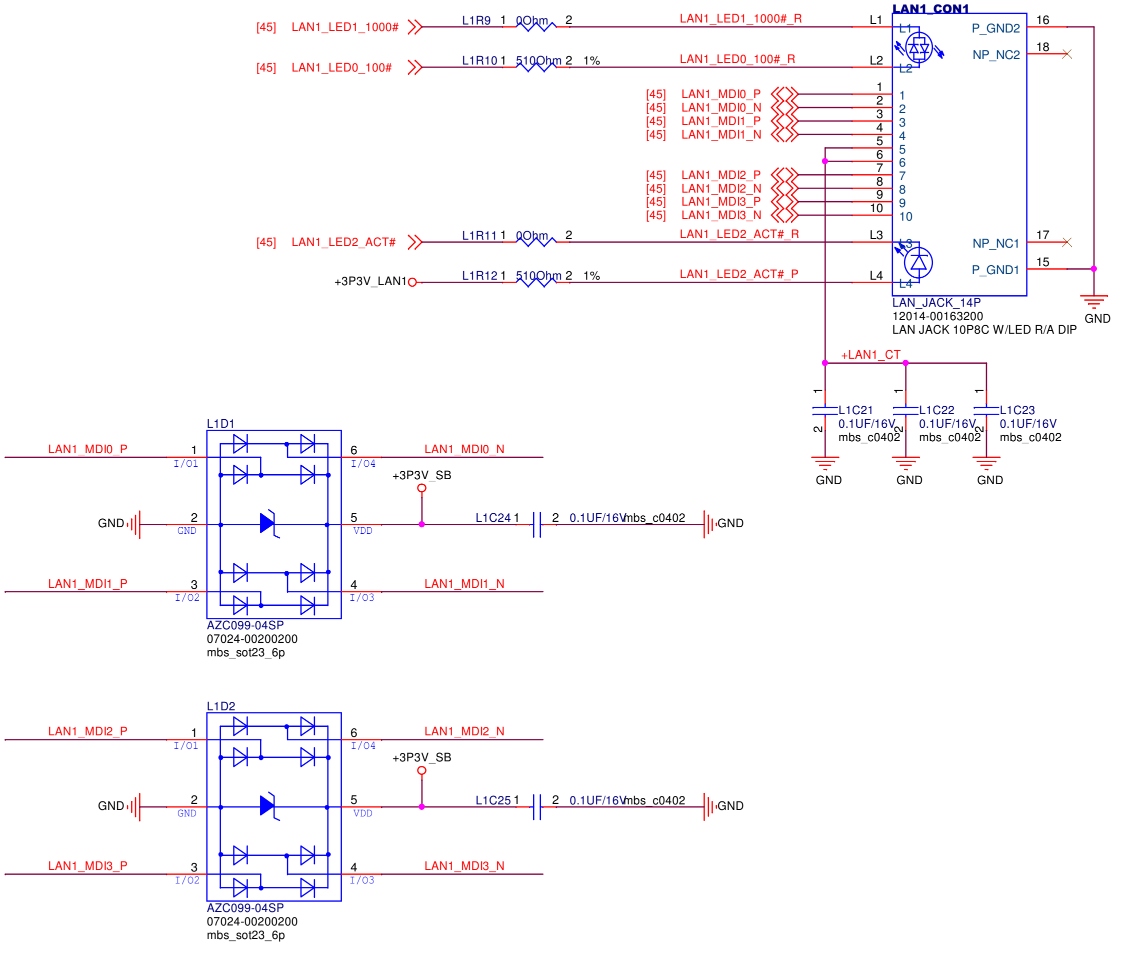
ASUSTek COMPUTER INC.

Title : LAN1 RTL8111H

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 45 of 90



ASUSTek COMPUTER INC.

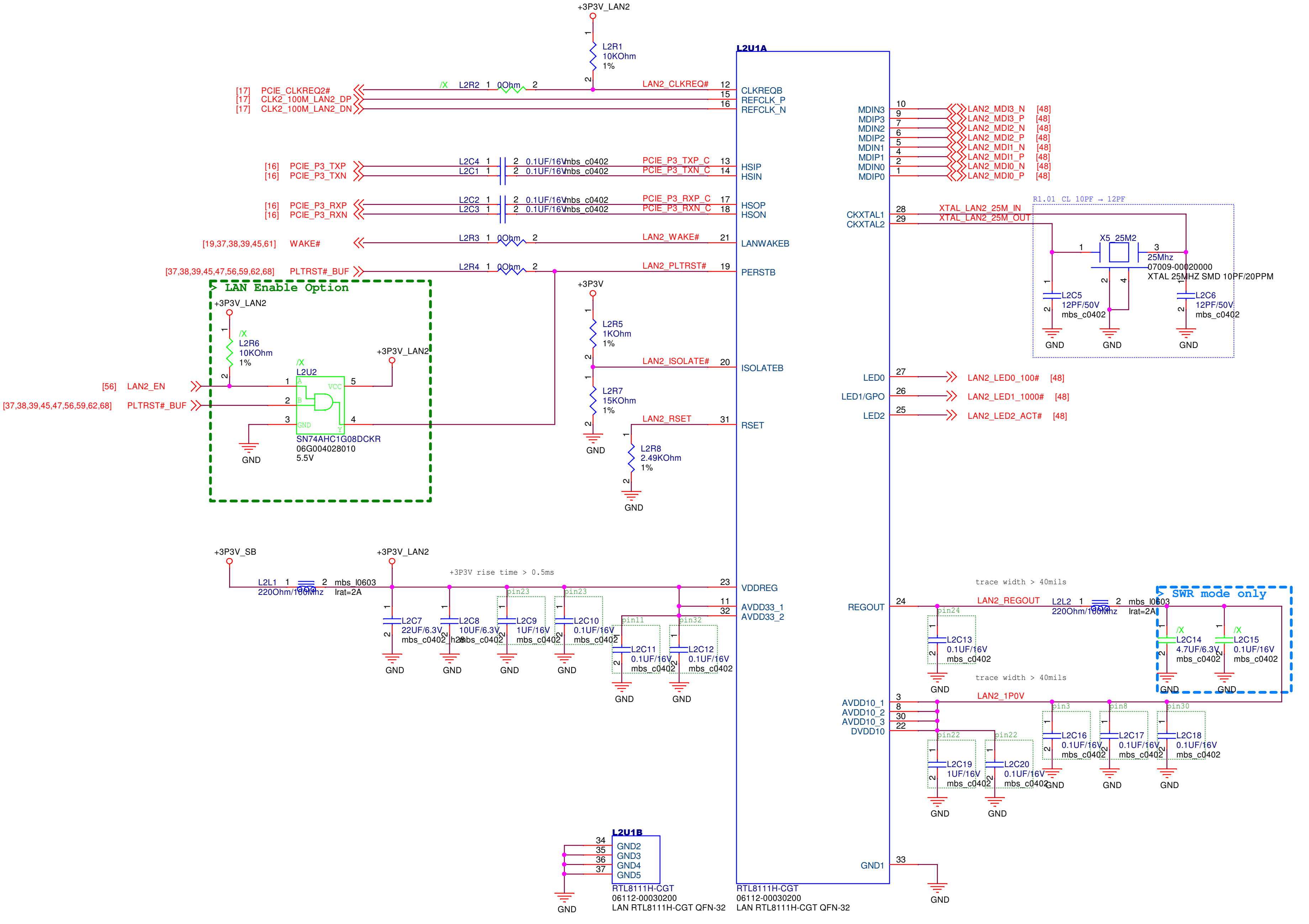
Title : **LAN1 RJ45 CON**

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

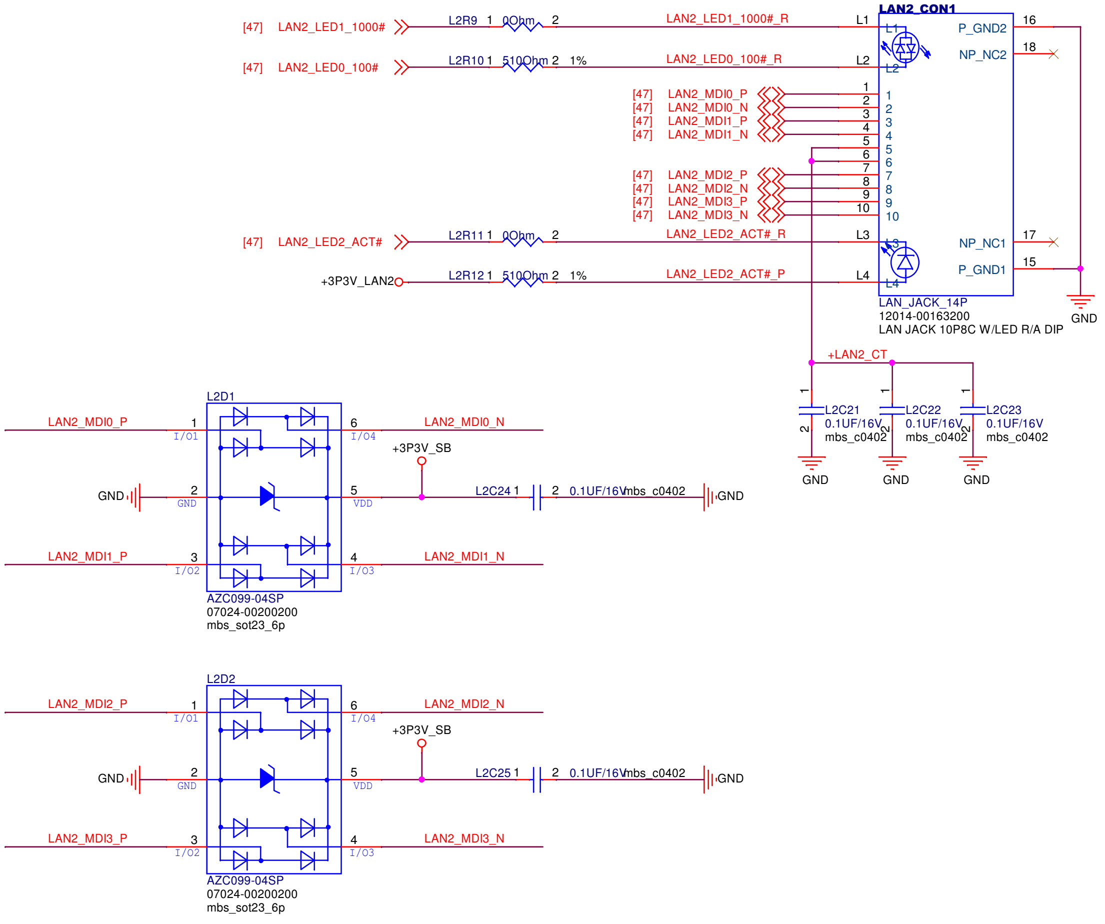
Date: Thursday, July 15, 2021 Sheet 46 of 90

LAN2 RTL8111H



ASUSTek COMPUTER INC.

Title :	LAN2 RTL8111H	
Engineer:	Shawn Yu	
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01
Date: Thursday, July 15, 2021	Sheet 47 of 90	



ASUSTek COMPUTER INC.

Title : **LAN2 RJ45 CON**

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

Date: Thursday, July 15, 2021 Sheet 48 of 90

LAN3

	Title : xxx		
ASUSTek COMPUTER INC.	Engineer: Shawn Yu		
Size A3	Project Name MIX-EHLD1		Rev R1.01
Date: Thursday, July 15, 2021		Sheet 49 of 90	

LAN3

ASUSTek COMPUTER INC.

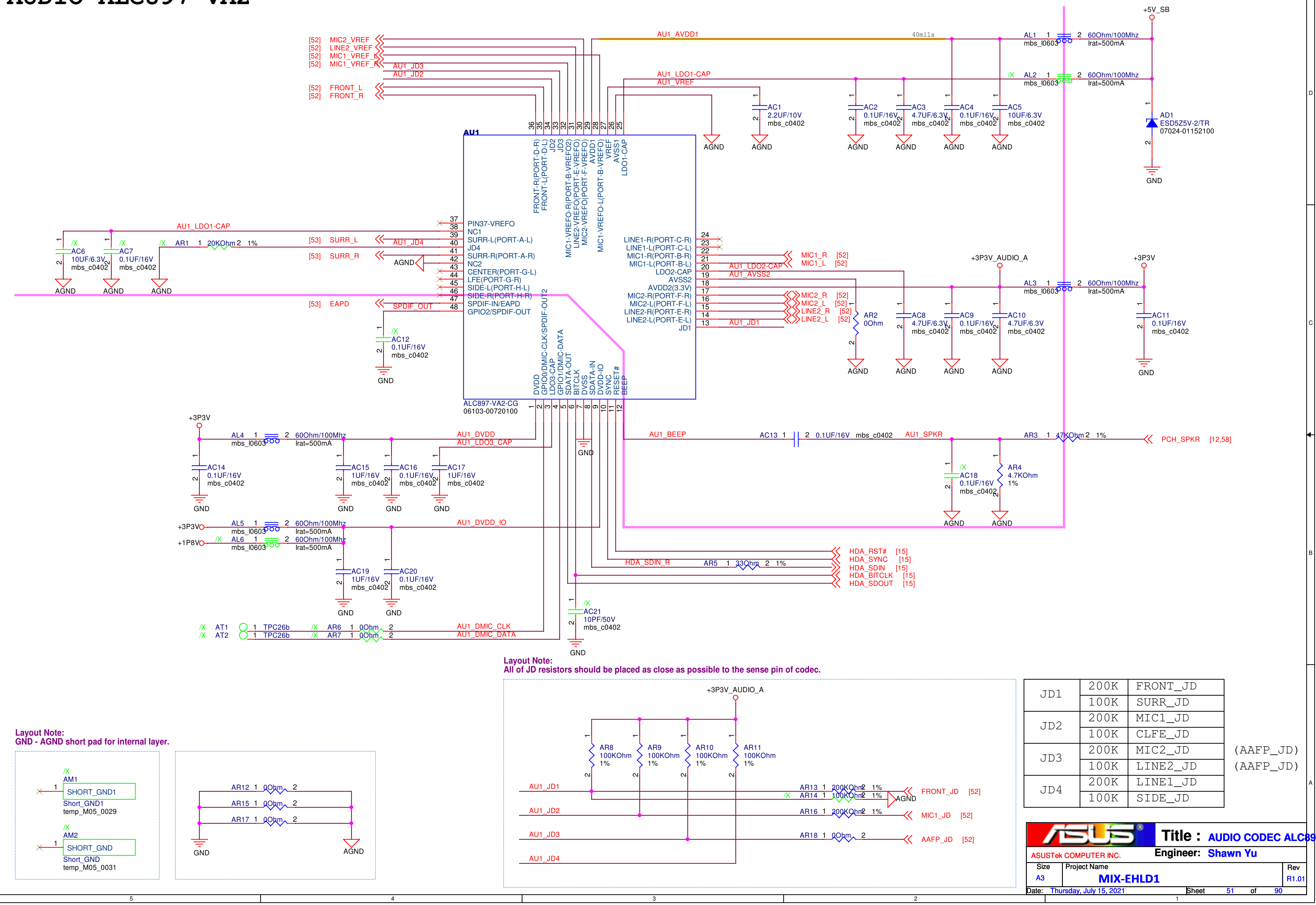
Title : xxx

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021

AUDIO ALC897-VA2



Layout Note:
All of JD resistors should be placed as close as possible to the sense pin of codec.

Layout Note:
GND - AGND short pad for internal layer.

JD1	200K	FRONT_JD	
	100K	SURR_JD	
JD2	200K	MIC1_JD	
	100K	CLFE_JD	
JD3	200K	MIC2_JD	(AAFP_JD)
	100K	LINE2_JD	(AAFP_JD)
JD4	200K	LINE1_JD	
	100K	SIDE_JD	

ASUSTek COMPUTER INC.

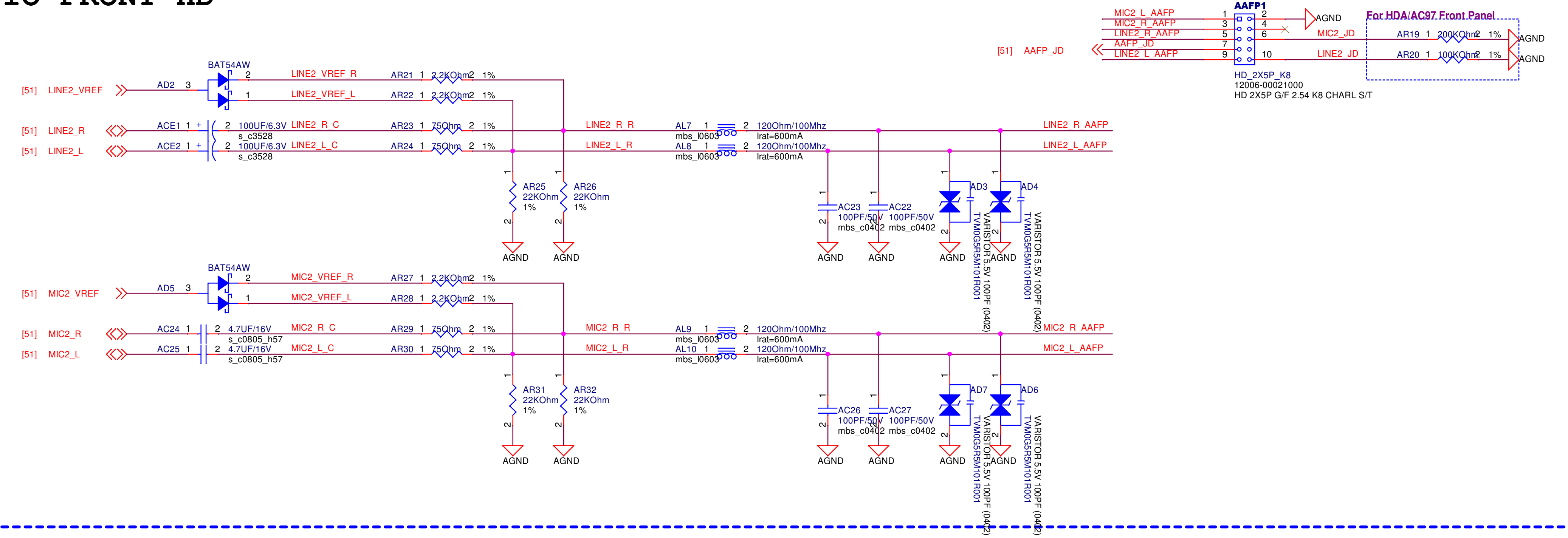
Title : AUDIO CODEC ALC897

Engineer: Shawn Yu

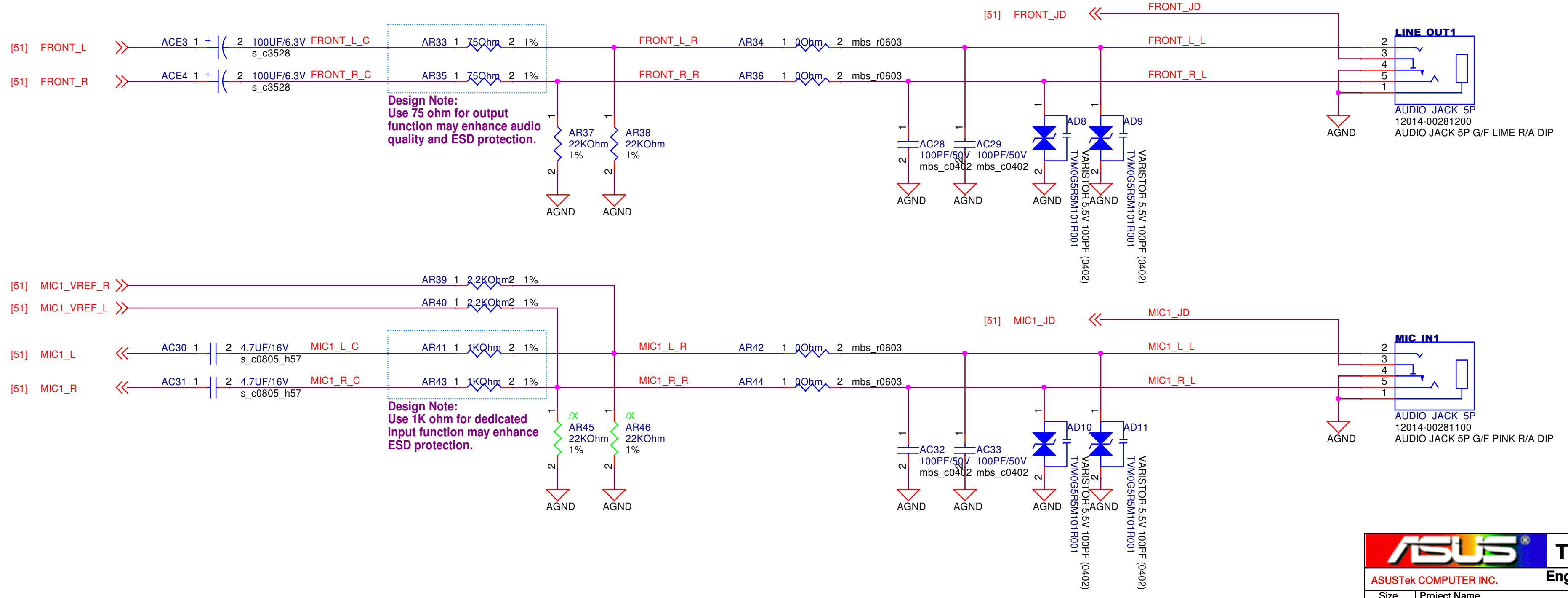
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 51 of 90

AUDIO FRONT HD



AUDIO REAR PHONE JACK



Design Note:
Use 75 ohm for output function may enhance audio quality and ESD protection.

Design Note:
Use 1K ohm for dedicated input function may enhance ESD protection.

ASUSTek COMPUTER INC.
Title : AUDIO PHONE JACK
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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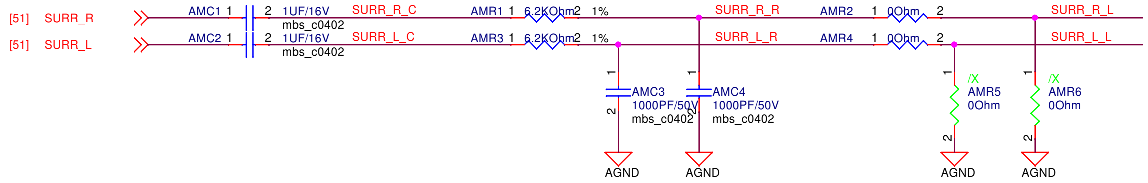
AUDIO AMP EUA2075



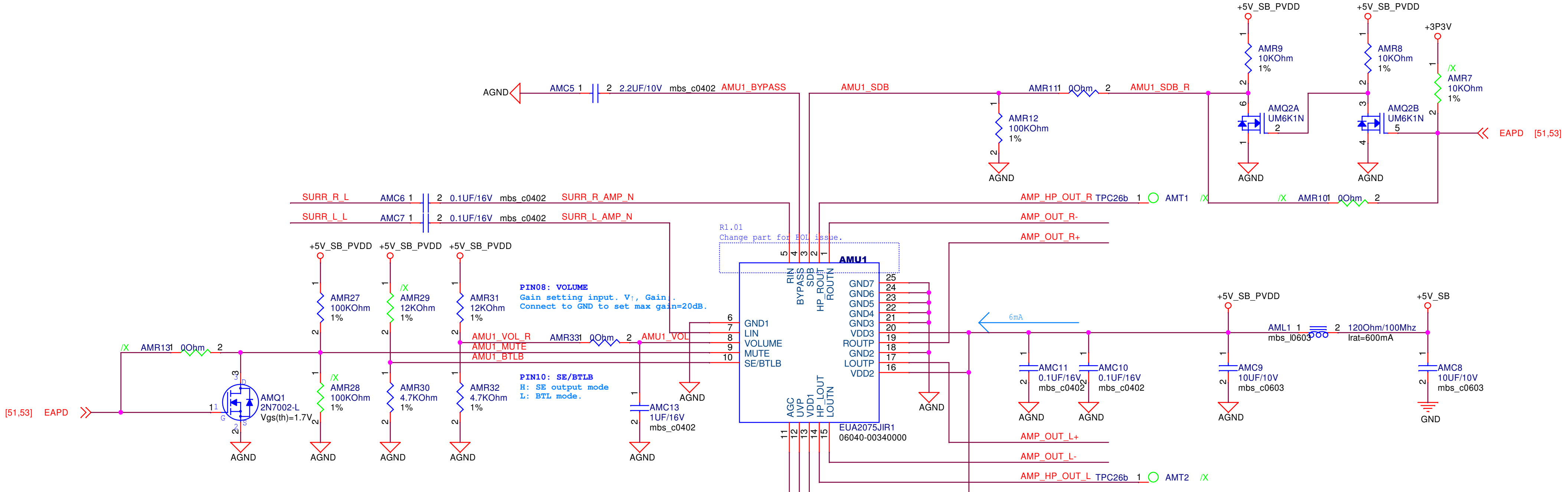
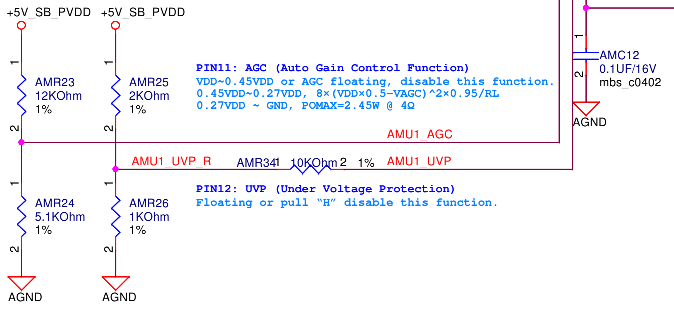
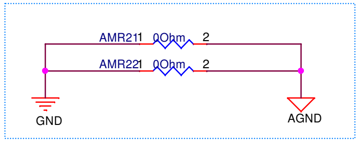


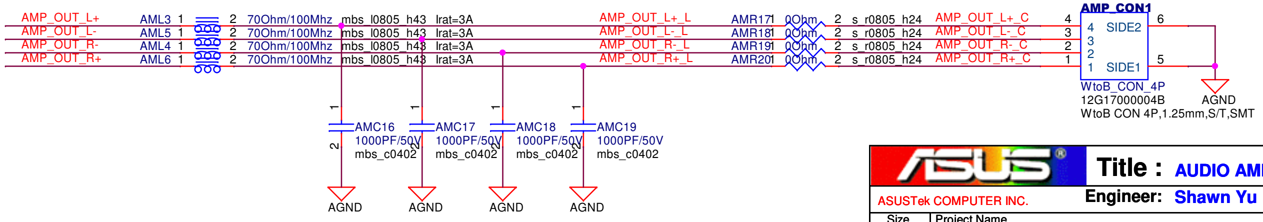
Table 2. AGC Function

AGC Voltage	Output Power
VDD ~ 0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$8\times(VDD\times0.5-VAGC)^2\times0.95/R_L$
0.27VDD ~ GND	$P_{OMAX}=2.45W$ @ 4Ω $P_{OMAX}=1.225W$ @ 8Ω


+5V_SB_PVDD
AMR23 12KOhm 1%
AMR25 2KOhm 1%
AMR24 5.1KOhm 1%
AMR26 1KOhm 1%
PIN11: AGC (Auto Gain Control Function)
VDD~0.45VDD or AGC floating, disable this function.
0.45VDD~0.27VDD, 8×(VDD×0.5-VAGC)^2×0.95/RL
0.27VDD ~ GND, POMAX=2.45W @ 4Ω
AMU1_AGC
AMU1_UVP_R
AMR34 1 10KOhm 2 1%
AMU1_UVP
PIN12: UVP (Under Voltage Protection)
Floating or pull "H" disable this function.
AMC12 0.1UF/16V mbs_c0402
AGND



Speaker 2W/4Ω


AMP_OUT_L+
AMP_OUT_L-
AMP_OUT_R-
AMP_OUT_R+
AML3 1 2 70Ohm/100Mhz mbs_l0805_h43 Irat=3A
AML5 1 2 70Ohm/100Mhz mbs_l0805_h43 Irat=3A
AML4 1 2 70Ohm/100Mhz mbs_l0805_h43 Irat=3A
AML6 1 2 70Ohm/100Mhz mbs_l0805_h43 Irat=3A
AMP_OUT_L+_L
AMP_OUT_L-_L
AMP_OUT_R-_L
AMP_OUT_R+_L
AMR17 1 0Ohm 2 s_r0805_h24
AMR18 1 0Ohm 2 s_r0805_h24
AMR19 1 0Ohm 2 s_r0805_h24
AMR20 1 0Ohm 2 s_r0805_h24
AMP_OUT_L+_C
AMP_OUT_L-_C
AMP_OUT_R-_C
AMP_OUT_R+_C
AMP_CON1
SIDE2
SIDE1
WtoB_CON_4P
12G17000004B
WtoB CON 4P,1.25mm,S/T,SMT
AMC16 1000PF/50V mbs_c0402
AMC17 1000PF/50V mbs_c0402
AMC18 1000PF/50V mbs_c0402
AMC19 1000PF/50V mbs_c0402
AGND

With the condition: R3 >> R1//R2

$V_{UVP}=[1.2-(5.7\mu A\times R3)]\times(R1+R2)/R2$

Hysteresis=$(4.6\mu A\times R3)\times(R1+R2)/R2$

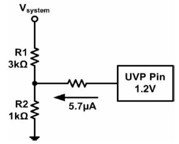


Figure 30. Under Voltage Protection

ASUSTek COMPUTER INC.
Title : AUDIO AMP. EUA2012A
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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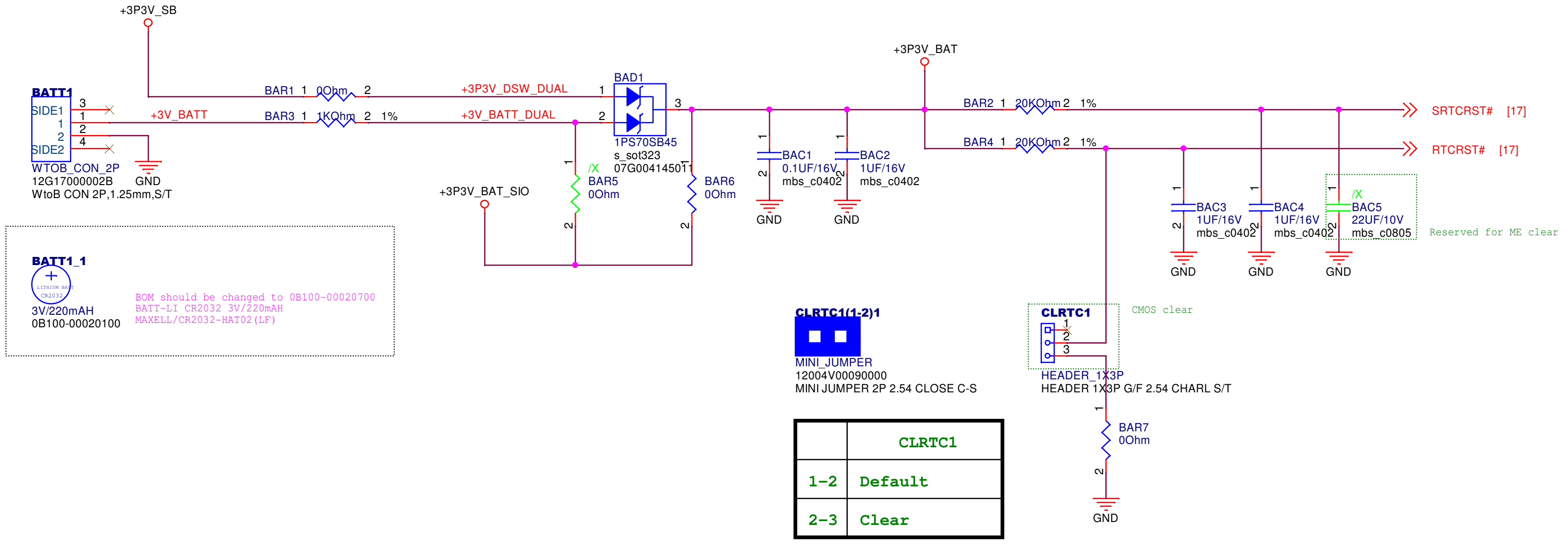

	CLRTC1
1-2	Default
2-3	Clear

ASUSTek COMPUTER INC.

Title : RTC

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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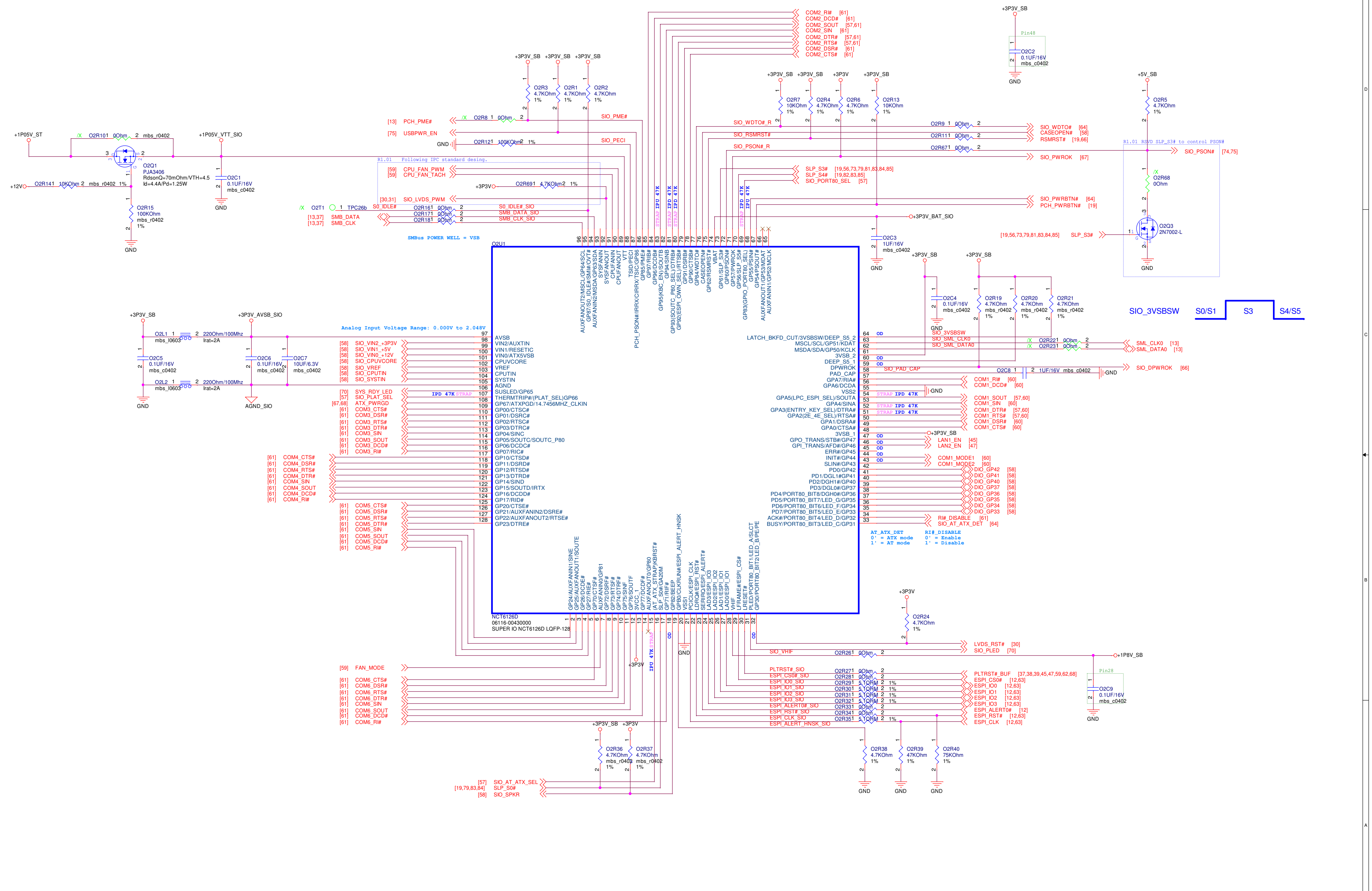


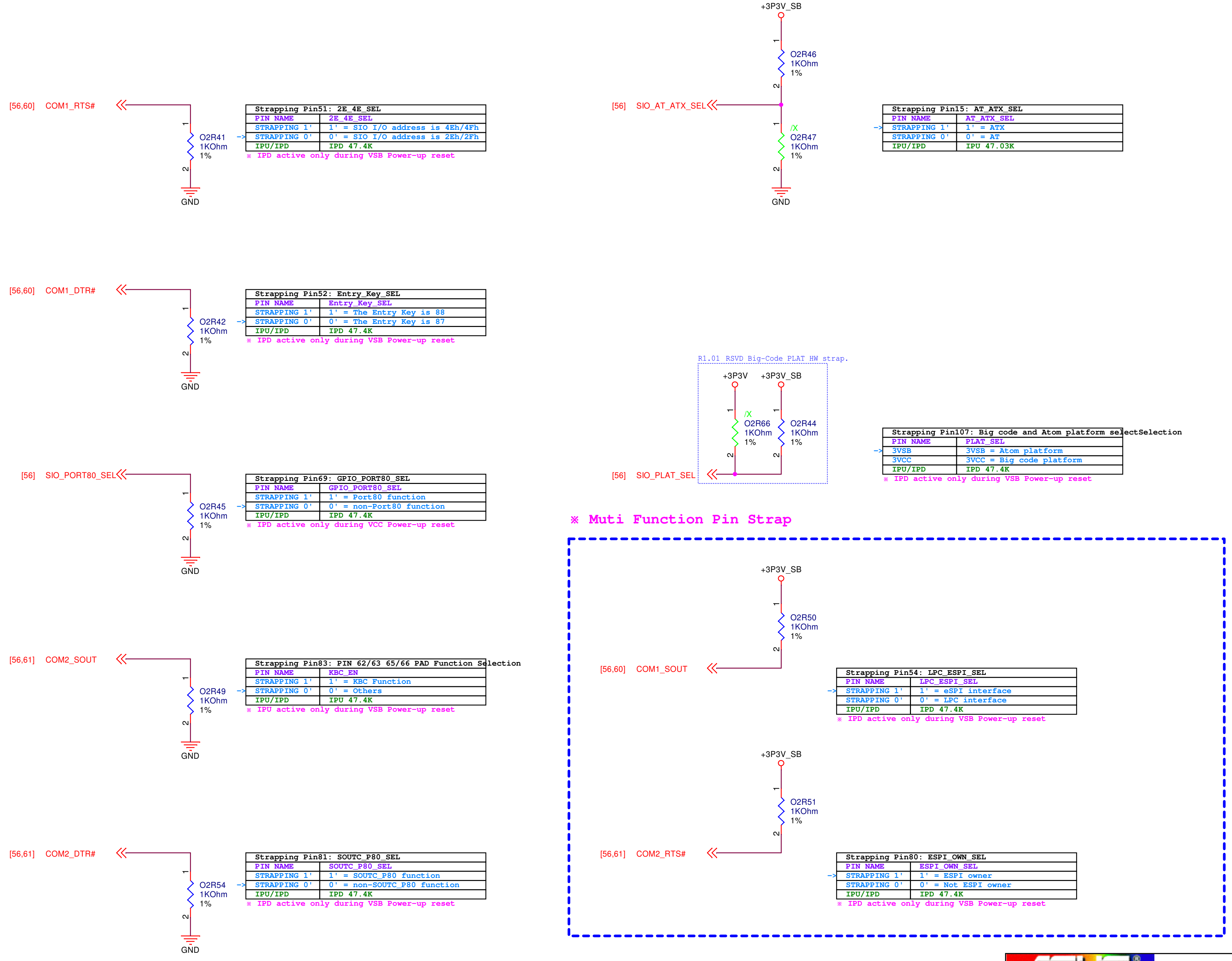
ASUSTek COMPUTER INC.

Title : SIO NCT6126D

Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 56 of 90



Strapping Pin51: 2E_4E_SEL

PIN NAME	2E_4E_SEL
STRAPPING 1'	1' = SIO I/O address is 4Eh/4Fh
STRAPPING 0'	0' = SIO I/O address is 2Eh/2Fh
IPU/IPD	IPD 47.4K

※ IPD active only during VSB Power-up reset

Strapping Pin15: AT_ATX_SEL

PIN NAME	AT_ATX_SEL
STRAPPING 1'	1' = ATX
STRAPPING 0'	0' = AT
IPU/IPD	IPU 47.03K

Strapping Pin52: Entry_Key_SEL

PIN NAME	Entry_Key_SEL
STRAPPING 1'	1' = The Entry Key is 88
STRAPPING 0'	0' = The Entry Key is 87
IPU/IPD	IPD 47.4K

※ IPD active only during VSB Power-up reset

Strapping Pin107: Big code and Atom platform selectSelection

PIN NAME	PLAT_SEL
3VSB	3VSB = Atom platform
3VCC	3VCC = Big code platform
IPU/IPD	IPD 47.4K

※ IPD active only during VSB Power-up reset

Strapping Pin69: GPIO_PORT80_SEL

PIN NAME	GPIO_PORT80_SEL
STRAPPING 1'	1' = Port80 function
STRAPPING 0'	0' = non-Port80 function
IPU/IPD	IPD 47.4K

※ IPD active only during VCC Power-up reset

※ Muti Function Pin Strap

Strapping Pin83: PIN 62/63 65/66 PAD Function Selection

PIN NAME	KBC_EN
STRAPPING 1'	1' = KBC Function
STRAPPING 0'	0' = Others
IPU/IPD	IPU 47.4K

※ IPU active only during VSB Power-up reset

Strapping Pin54: LPC_ESPI_SEL

PIN NAME	LPC_ESPI_SEL
STRAPPING 1'	1' = eSPI interface
STRAPPING 0'	0' = LPC interface
IPU/IPD	IPD 47.4K

※ IPD active only during VSB Power-up reset

Strapping Pin81: SOUTC_P80_SEL

PIN NAME	SOUTC_P80_SEL
STRAPPING 1'	1' = SOUTC_P80 function
STRAPPING 0'	0' = non-SOUTC_P80 function
IPU/IPD	IPD 47.4K

※ IPD active only during VSB Power-up reset

Strapping Pin80: ESPI_OWN_SEL

PIN NAME	ESPI_OWN_SEL
STRAPPING 1'	1' = ESPI owner
STRAPPING 0'	0' = Not ESPI owner
IPU/IPD	IPD 47.4K

※ IPD active only during VSB Power-up reset

ASUSTek COMPUTER INC.
Title : SIO PIN STRAP
Engineer: Shawn Yu
Size A3
Project Name MIX-EHLD1
Rev R1.01
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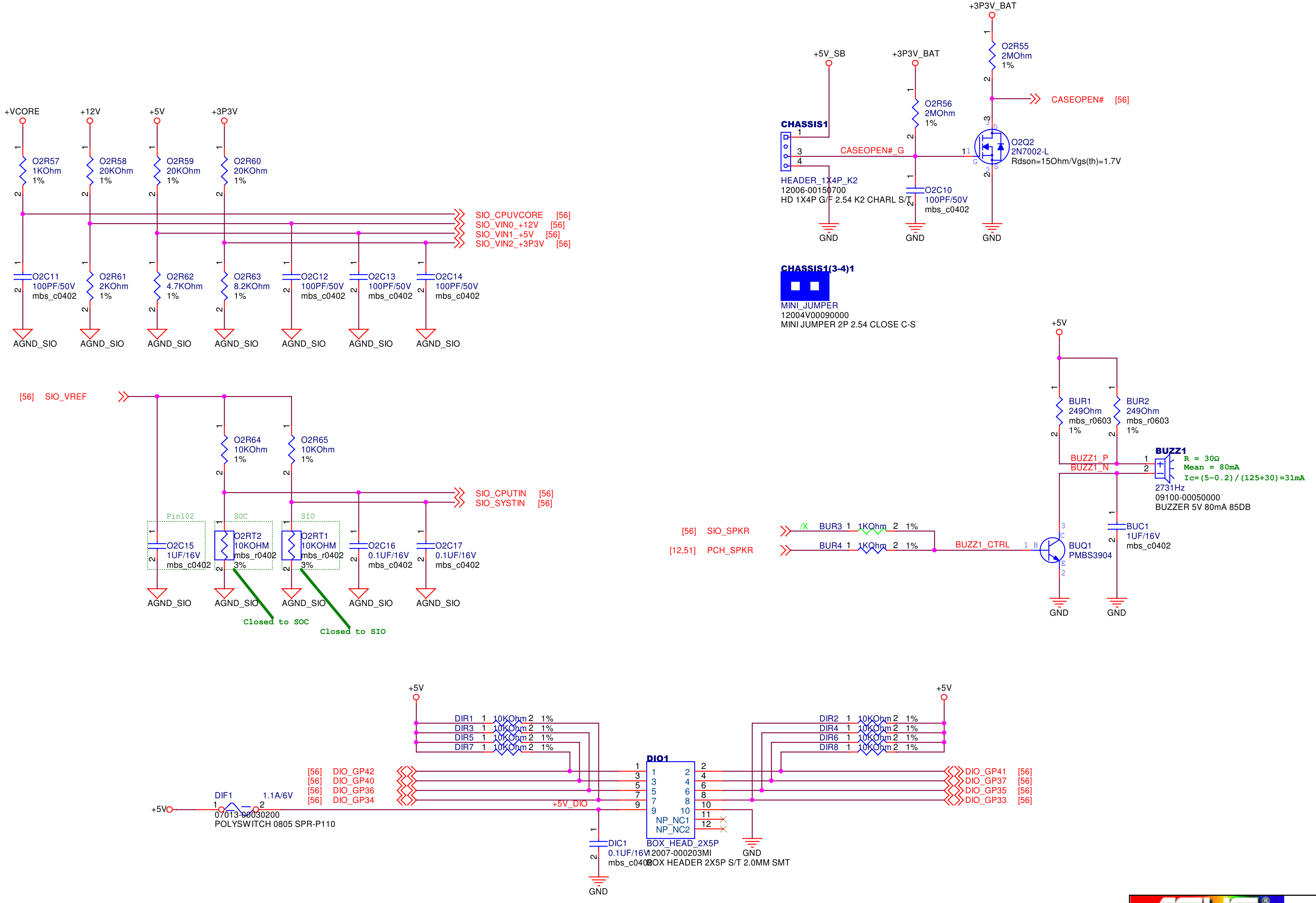

ASUSTek COMPUTER INC.

Title : **HW MONITOR**

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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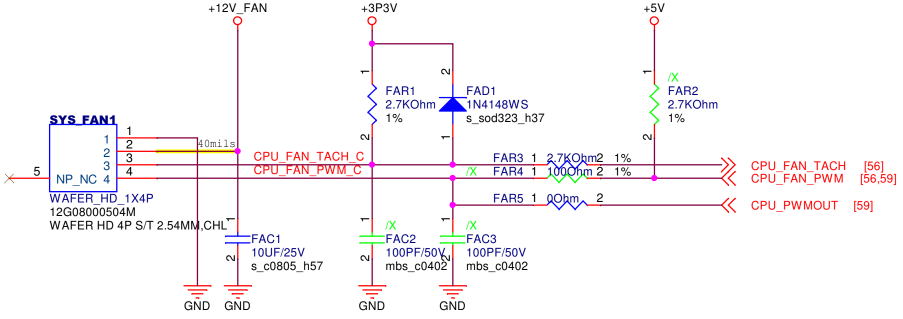
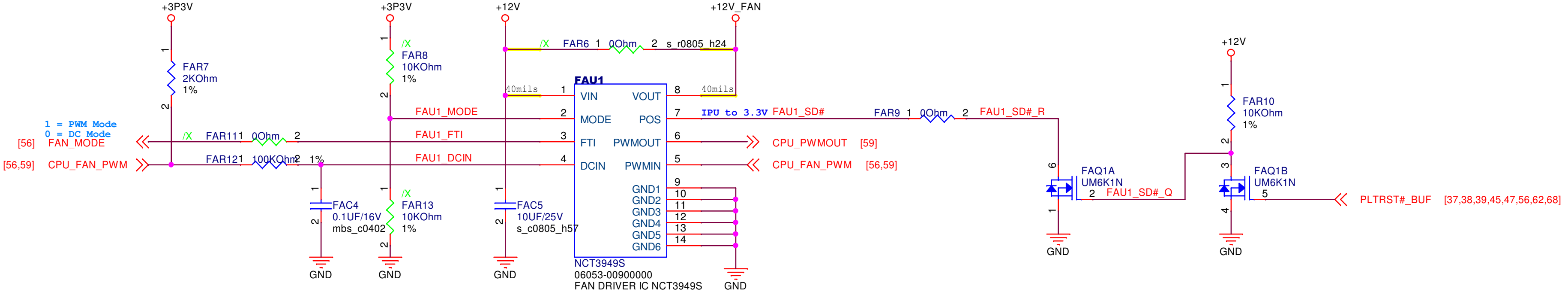
SYS_FAN HD (PWM MODE ONLY)

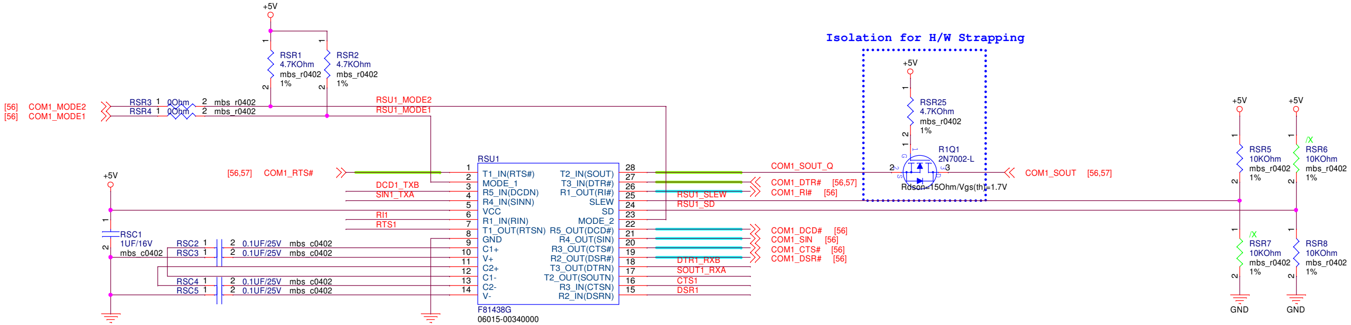


FAN DRIVER for SUPPORT DC/PWM MODE



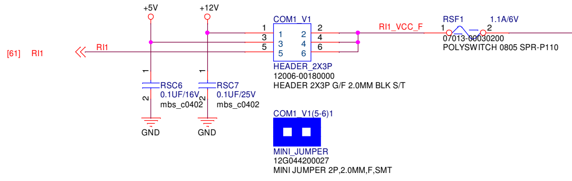
NCT3949S MODE setting	
NC (Floating)	Auto-detection Mode
Pull-up 3.3V	PWM Mode
Pull-down GND	DC Mode
IPU/IPD	Internal pull-up to 1.65V (typ.)

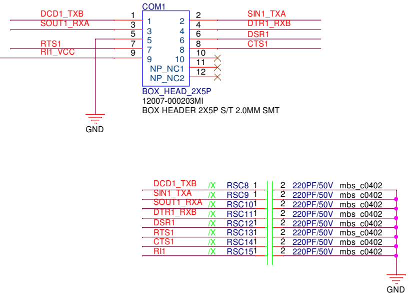
ASUSTek COMPUTER INC.	Title : **FAN HD**		
	Engineer: **Shawn Yu**		
Size A3	Project Name **MIX-EHLD1**		Rev R1.01
Date: Thursday, July 15, 2021	Sheet 59	of 90	



Slew rate control pin. Internal pull high≒ 625KΩ.
1: RS-232 to 1Mbps or RS-485/RS-422 to 10Mbps.
0: 250kbps for RS-232 &, RS-485/RS-422.

COM1_V1	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)




DCD1_TXB
SOUT1_RXA
RTS1
RI1_VCC
COM1
SIN1_TXA
DTR1_RXB
DSR1
CTS1
NP_NC1
NP_NC2
BOX_HEAD_2X5P
12007-000203MI
BOX HEADER 2X5P S/T 2.0MM SMT
GND
RSC8 220PF/50V mbs_c0402
RSC9 220PF/50V mbs_c0402
RSC10 220PF/50V mbs_c0402
RSC11 220PF/50V mbs_c0402
RSC12 220PF/50V mbs_c0402
RSC13 220PF/50V mbs_c0402
RSC14 220PF/50V mbs_c0402
RSC15 220PF/50V mbs_c0402

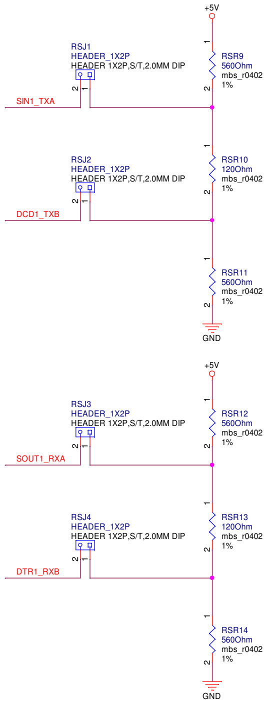
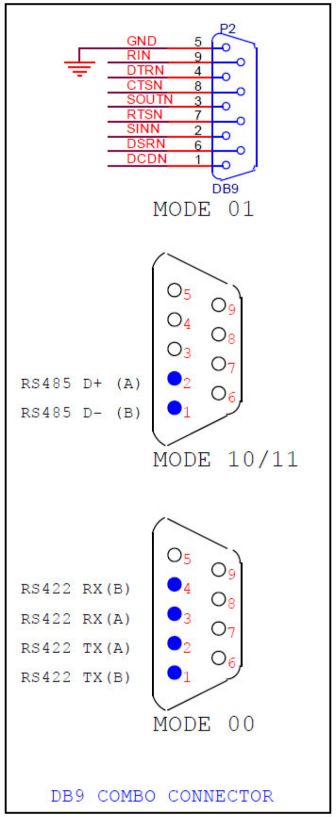

+5V
RSJ1 HEADER_1X2P HEADER 1X2P,S/T,2.0MM DIP
RSR9 560Ohm mbs_r0402 1%
SIN1_TXA
RSJ2 HEADER_1X2P HEADER 1X2P,S/T,2.0MM DIP
RSR10 120Ohm mbs_r0402 1%
DCD1_TXB
RSR11 560Ohm mbs_r0402 1%
GND
RSJ3 HEADER_1X2P HEADER 1X2P,S/T,2.0MM DIP
RSR12 560Ohm mbs_r0402 1%
SOUT1_RXA
RSJ4 HEADER_1X2P HEADER 1X2P,S/T,2.0MM DIP
RSR13 120Ohm mbs_r0402 1%
DTR1_RXB
RSR14 560Ohm mbs_r0402 1%

TABLE 1: Mode Select Configuration

Pin 2 Mode_1	Pin 23 Mode_2	Pin 24 SD	Mode	Status
0	1	X	Pure RS-232	3T/ 5R RS-232.
1	0	X	RS-485 DE#/RE Half Duplex	1T/1R RS-485
1	1	X	RS-485 DE/RE# Half Duplex	1T/1R RS-485
0	0	X	Pure RS-422 Full Duplex	1T/1R RS422 mode
X	X	1	Shutdown Mode	



Title : COM1 RS232/422/485
ASUSTek COMPUTER INC.
Engineer: Shawn Yu
Size A2
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
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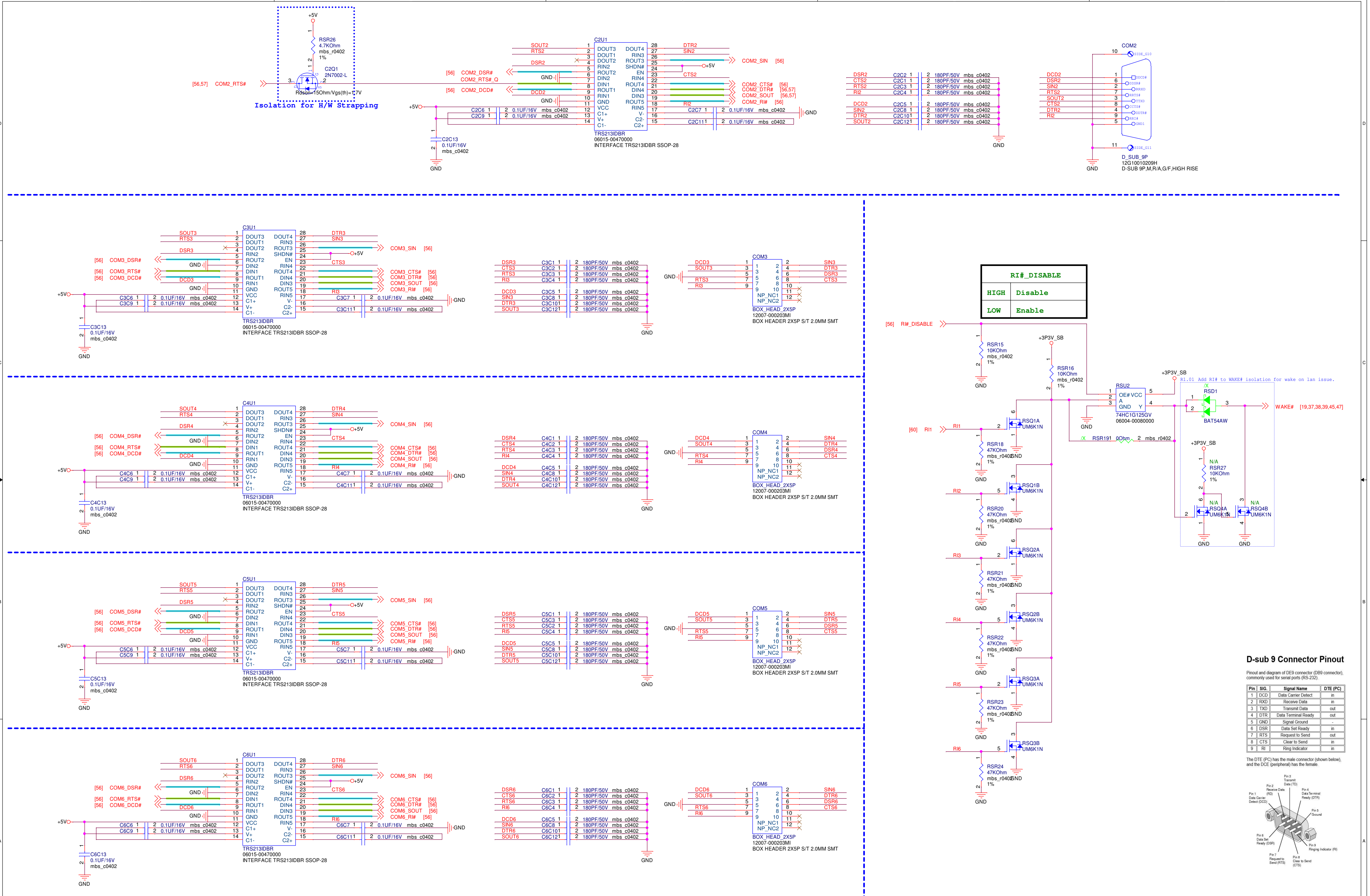


+5V
RSR26
4.7KOhm
mbs_r0402
1%
C2Q1
2N7002-L
Rdson=15Ohm/Vgs(th)=1.7V
[56,57] COM2_RTS#
Isolation for H/W Strapping
C2U1
TRS213IDBR
06015-00470000
INTERFACE TRS213IDBR SSOP-28
DOUT3 DOUT1 DOUT2 RIN2 ROUT2 DIN2 DIN1 ROUT1 RIN1 GND VCC C1+ V+ C1-
DOUT4 RIN3 ROUT3 SHDN# EN RIN4 ROUT4 DIN4 DIN3 ROUT5 RIN5 V- C2- C2+
SOUT2 RTS2 DSR2 DCD2 DTR2 SIN2 CTS2 RI2
[56] COM2_DSR#
COM2_RTS#_Q
[56] COM2_DCD#
COM2_SIN [56]
COM2_CTS# [56]
COM2_DTR# [56,57]
COM2_SOUT [56,57]
COM2_RI# [56]
C2C6 C2C9 0.1UF/16V mbs_c0402
C2C7 C2C11 0.1UF/16V mbs_c0402
C2C13 0.1UF/16V mbs_c0402
C2C2 C2C1 C2C3 C2C4 C2C5 C2C8 C2C10 C2C12 180PF/50V mbs_c0402
COM2
D_SUB_9P
12G10010209H
D-SUB 9P,M,R/A,G/F,HIGH RISE
C3U1 C4U1 C5U1 C6U1
TRS213IDBR
06015-00470000
INTERFACE TRS213IDBR SSOP-28
[56] COM3_DSR# [56] COM3_RTS# [56] COM3_DCD#
COM3_SIN [56] COM3_CTS# [56] COM3_DTR# [56] COM3_SOUT [56] COM3_RI# [56]
[56] COM4_DSR# [56] COM4_RTS# [56] COM4_DCD#
COM4_SIN [56] COM4_CTS# [56] COM4_DTR# [56] COM4_SOUT [56] COM4_RI# [56]
[56] COM5_DSR# [56] COM5_RTS# [56] COM5_DCD#
COM5_SIN [56] COM5_CTS# [56] COM5_DTR# [56] COM5_SOUT [56] COM5_RI# [56]
[56] COM6_DSR# [56] COM6_RTS# [56] COM6_DCD#
COM6_SIN [56] COM6_CTS# [56] COM6_DTR# [56] COM6_SOUT [56] COM6_RI# [56]
COM3 COM4 COM5 COM6
BOX_HEAD_2X5P
12007-000203MI
BOX HEADER 2X5P S/T 2.0MM SMT
NP_NC1 NP_NC2
[56] RI#_DISABLE
RSR15 10KOhm mbs_r0402 1%
+3P3V_SB
RSR16 10KOhm mbs_r0402 1%
RSU2
74HC1G125GV
06004-00080000
OE# VCC A GND Y
R1.01 Add RI# to WAKE# isolation for wake on lan issue.
RSD1
BAT54AW
WAKE# [19,37,38,39,45,47]
RSR191 0Ohm mbs_r0402
RSR27 10KOhm 1%
RSQ4A RSQ4B UM6K1N N/A
[60] RI1
RSQ1A RSQ1B RSQ2A RSQ2B RSQ3A RSQ3B UM6K1N
RSR18 RSR20 RSR21 RSR22 RSR23 RSR24 47KOhm mbs_r0402 1%
RI1 RI2 RI3 RI4 RI5 RI6
GND
Pin 1 Data Carrier Detect (DCD)
Pin 2 Receive Data (RD)
Pin 3 Transmit Data (TD)
Pin 4 Data Terminal Ready (DTR)
Pin 5 Ground
Pin 6 Data Set Ready (DSR)
Pin 7 Request to Send (RTS)
Pin 8 Clear to Send (CTS)
Pin 9 Ringing Indicator (RI)

RI#_DISABLE	
HIGH	Disable
LOW	Enable

D-sub 9 Connector Pinout

Pinout and diagram of DE9 connector (DB9 connector), commonly used for serial ports (RS-232).

Pin	SIG.	Signal Name	DTE (PC)
1	DCD	Data Carrier Detect	in
2	RXD	Receive Data	in
3	TXD	Transmit Data	out
4	DTR	Data Terminal Ready	out
5	GND	Signal Ground	-
6	DSR	Data Set Ready	in
7	RTS	Request to Send	out
8	CTS	Clear to Send	in
9	RI	Ring Indicator	in

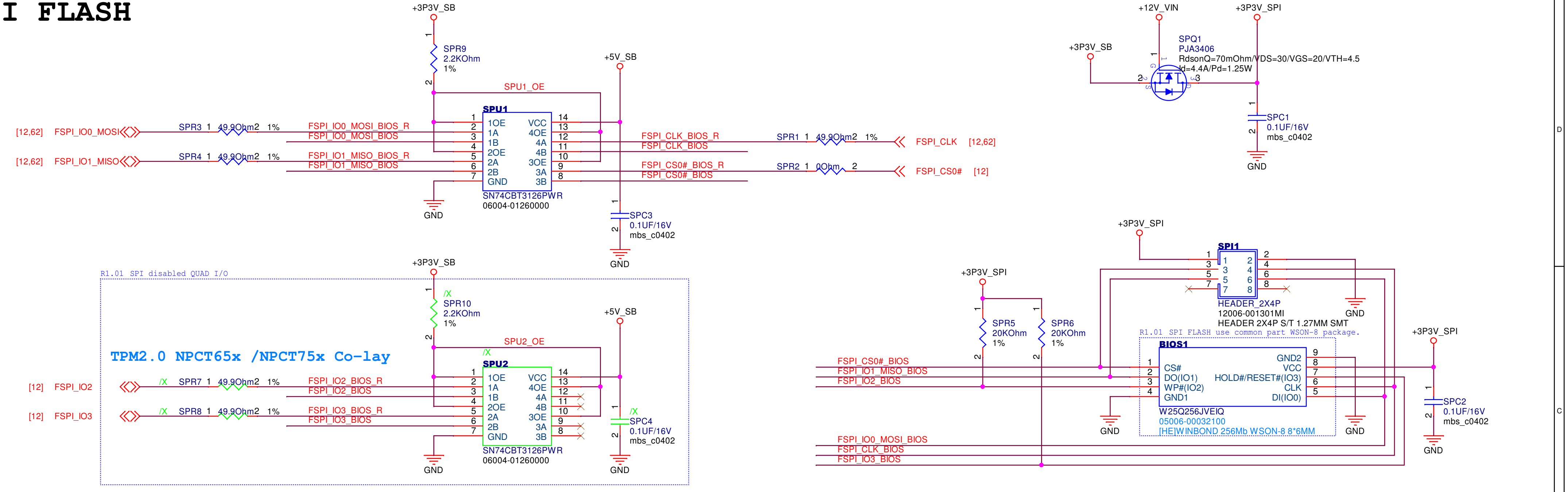
The DTE (PC) has the male connector (shown below), and the DCE (peripheral) has the female.

ASUSTek COMPUTER INC.
Title : COM2/3/4/5/6
Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021
Sheet 61 of 90

SPI FLASH

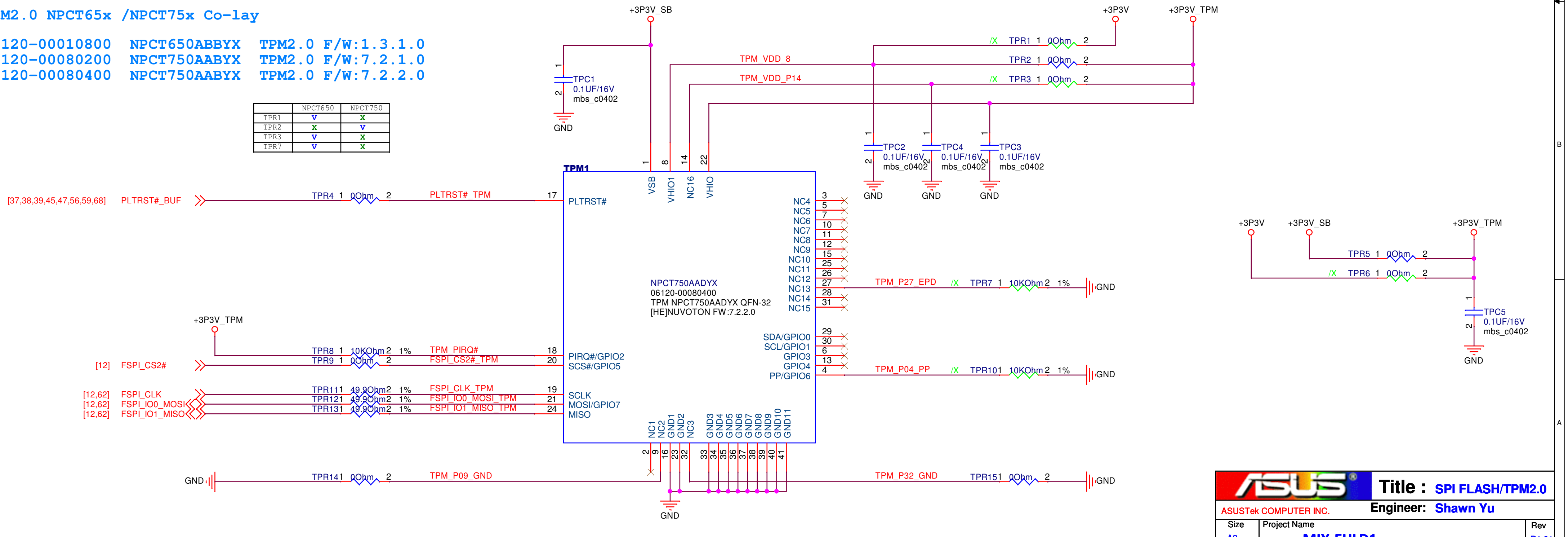


SPI TPM2.0

TPM2.0 NPCT65x /NPCT75x Co-lay

06120-00010800 NPCT650ABBYX TPM2.0 F/W:1.3.1.0
06120-00080200 NPCT750AABYX TPM2.0 F/W:7.2.1.0
06120-00080400 NPCT750AABYX TPM2.0 F/W:7.2.2.0

	NPCT650	NPCT750
TPR1	V	X
TPR2	X	V
TPR3	V	X
TPR7	V	X



ASUSTek COMPUTER INC.

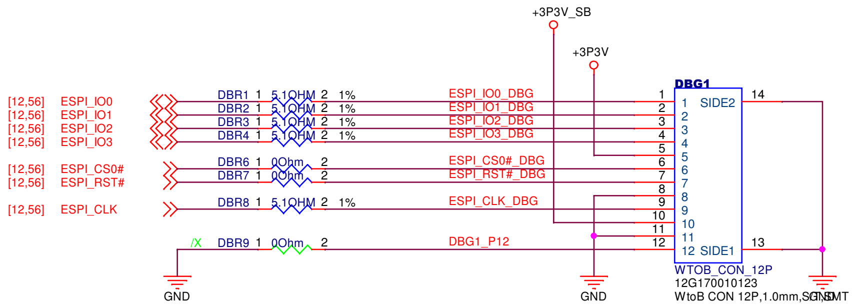
Title : SPI FLASH/TPM2.0

Engineer: Shawn Yu

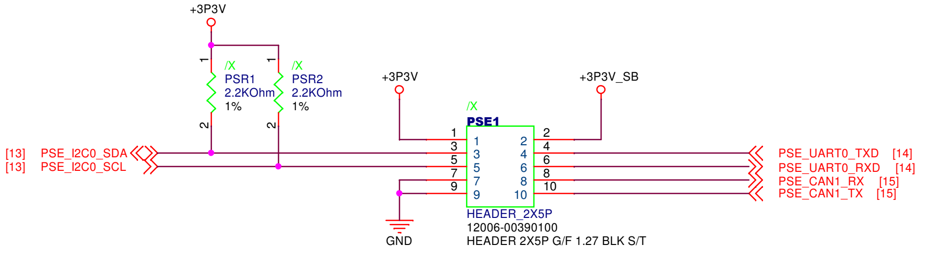
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 62 of 90

eSPI DEBUG PORT



PSE DEBUG HEADER



ASUSTek COMPUTER INC.

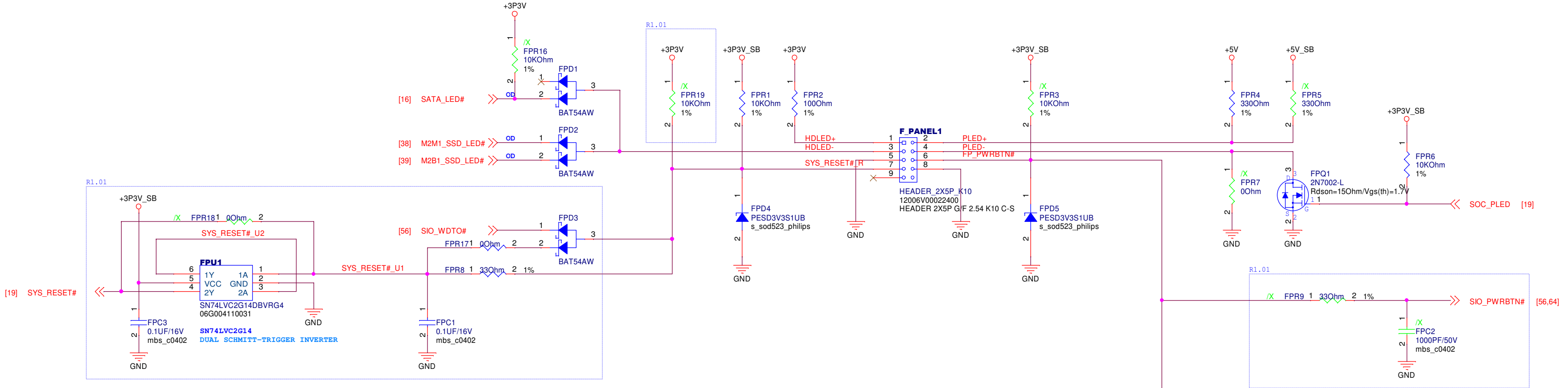
Title : **DEBUG PORT**

Engineer: **Shawn Yu**

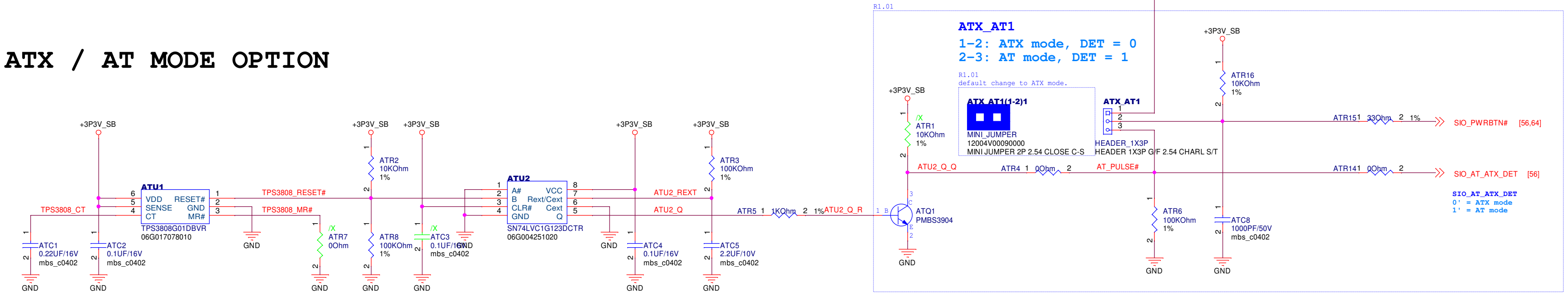
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 63 of 90

FRONT PANEL HD



ATX / AT MODE OPTION



ASUSTek COMPUTER INC.

Title : FRONT PANEL AT/ATX MODE

Engineer: Shawn Yu

Size	Project Name	Rev
A2	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 64 of 90

Title : xxx

ASUSTek COMPUTER INC.

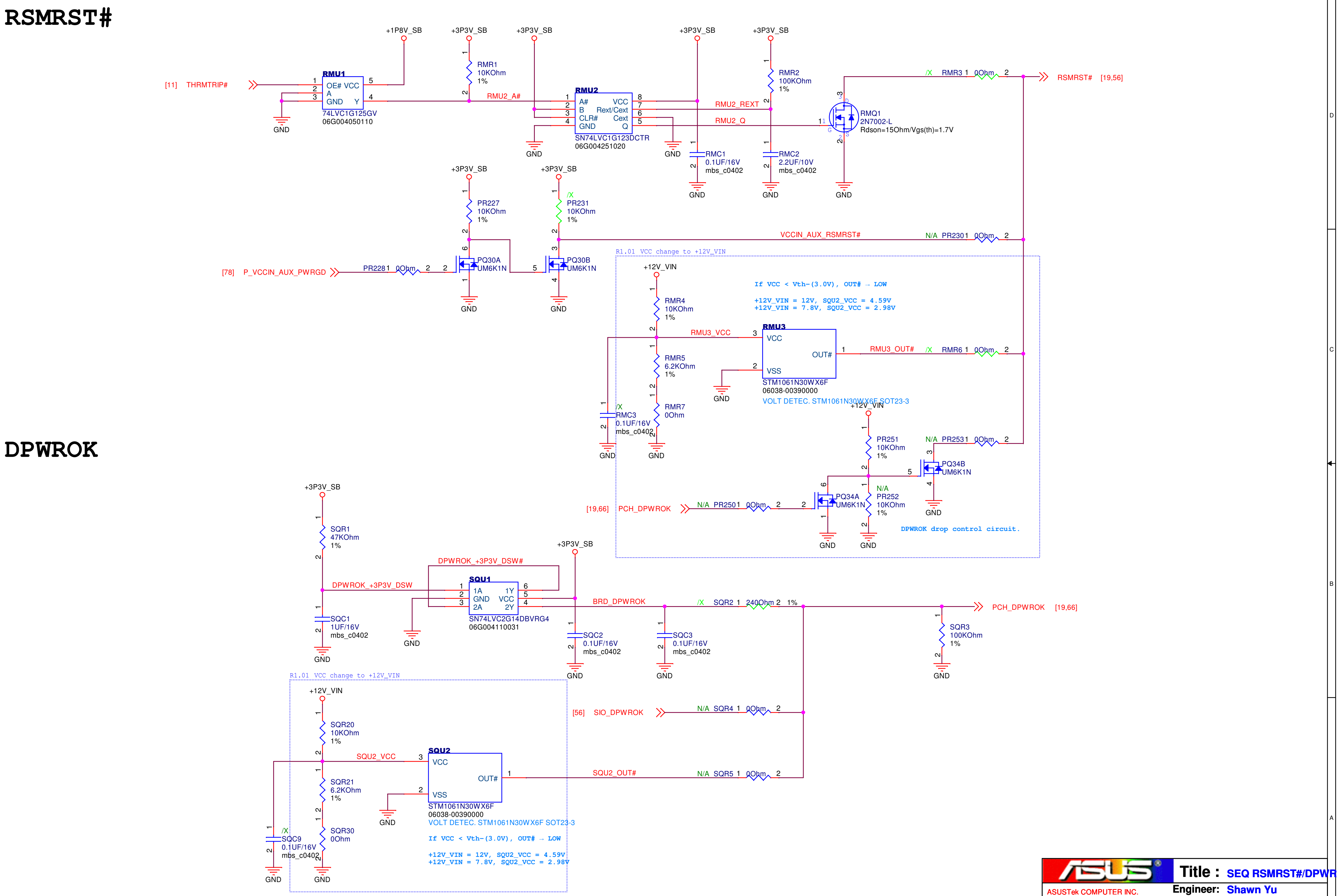
Engineer: Shawn Yu

Size
A3

Project Name
MIX-EHLD1

Rev
R1.01

Date: Thursday, July 15, 2021



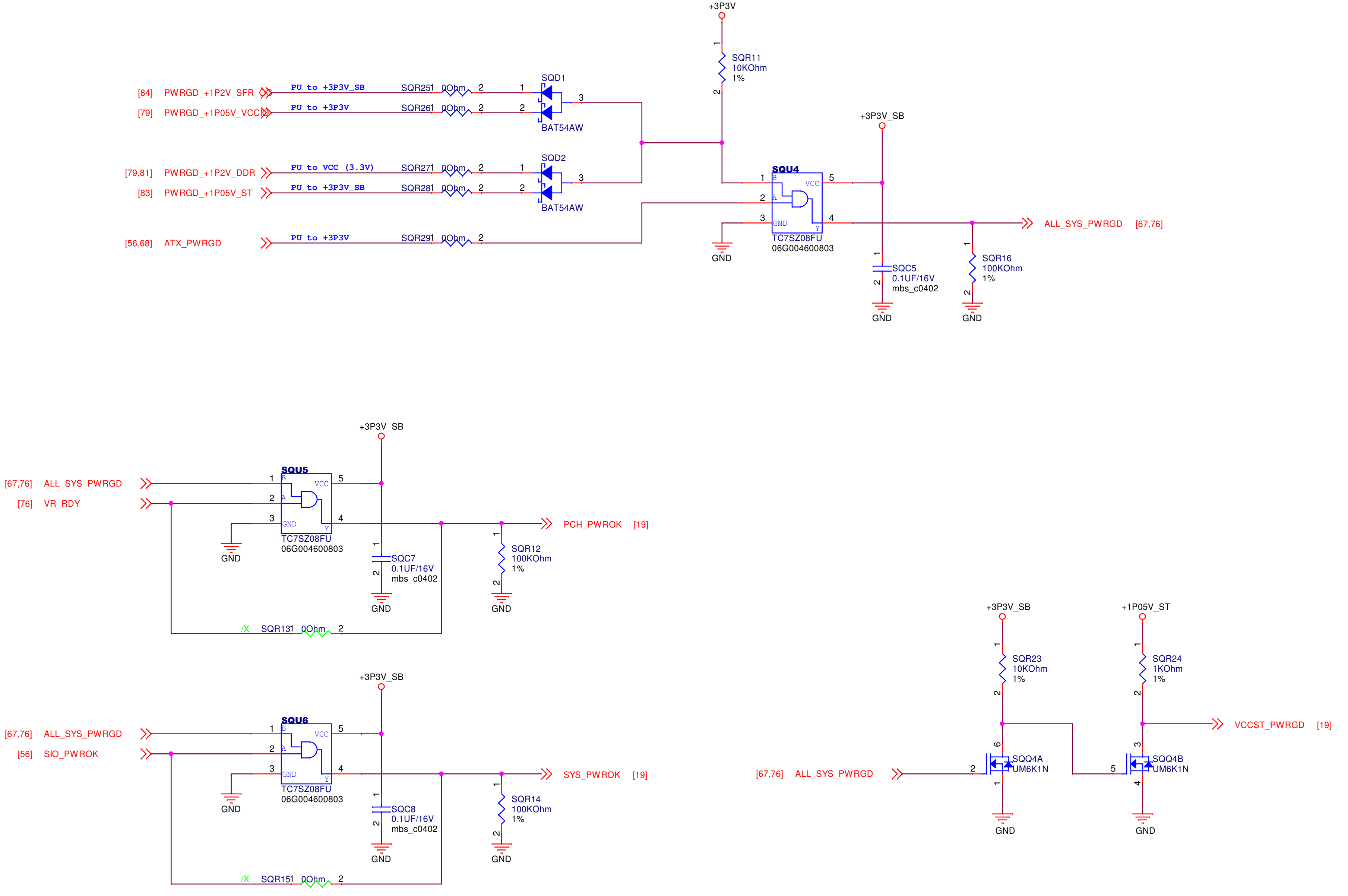
ASUSTek COMPUTER INC.

Title : SEQ RSMRST#/DPWROK

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 66 of 90



Title : SEQ PWRGD

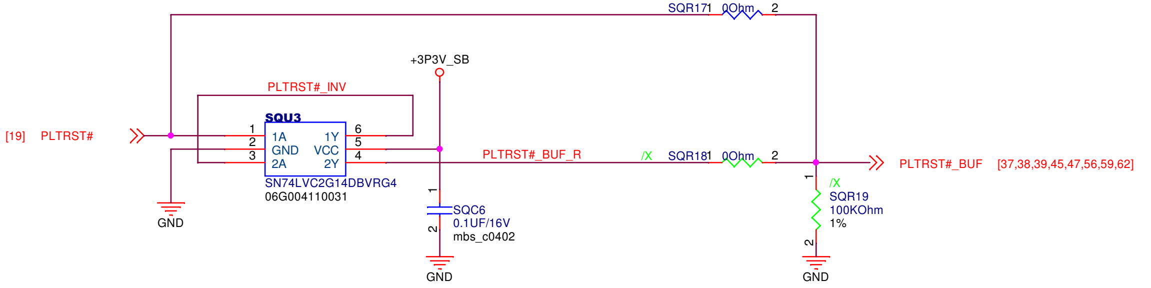
ASUSTek COMPUTER INC.

Engineer: Shawn Yu

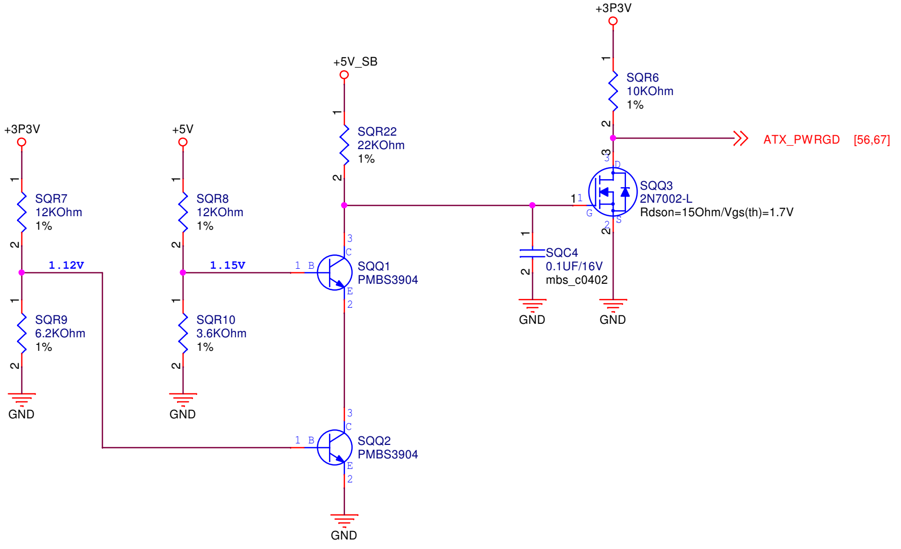
Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

Date: Thursday, July 15, 2021 Sheet 67 of 90

PLTRST#



ATX PWRGD



Title : xxx

ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021

ASUSTek COMPUTER INC.

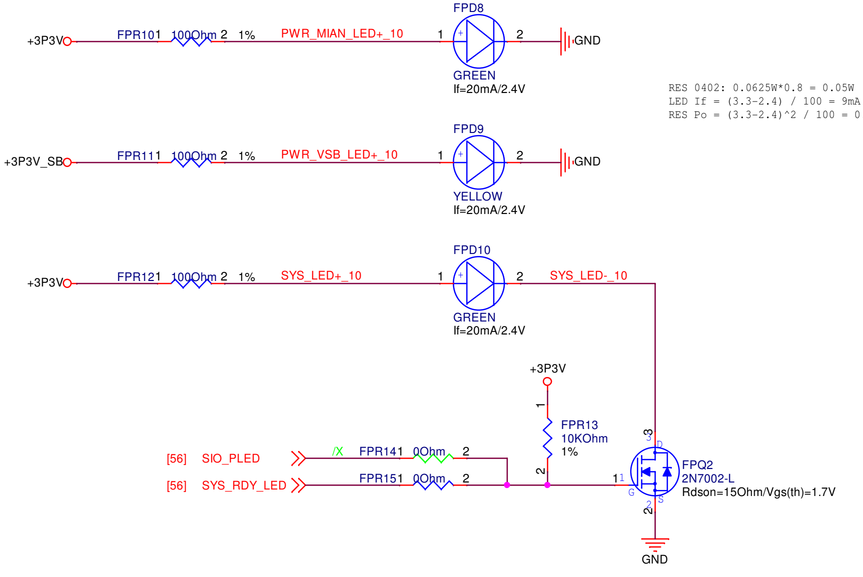
Title : xxx

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021

Standby PWR LED: +3P3V_SB
Main PWR LED: +3P3V



RES 0402: 0.0625W*0.8 = 0.05W (normal stress)
LED If = (3.3-2.4) / 100 = 9mA
RES Po = (3.3-2.4)^2 / 100 = 0.008W (<0.05W stress)

ASUSTek COMPUTER INC.
Title : STATUS LED
Engineer: Shawn Yu
Size: A3
Project Name: **MIX-EHLD1**
Rev: R1.01
Date: Thursday, July 15, 2021
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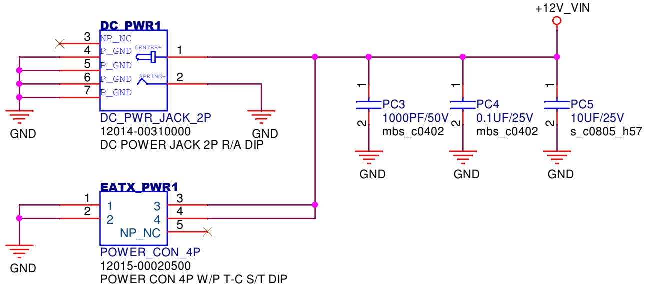
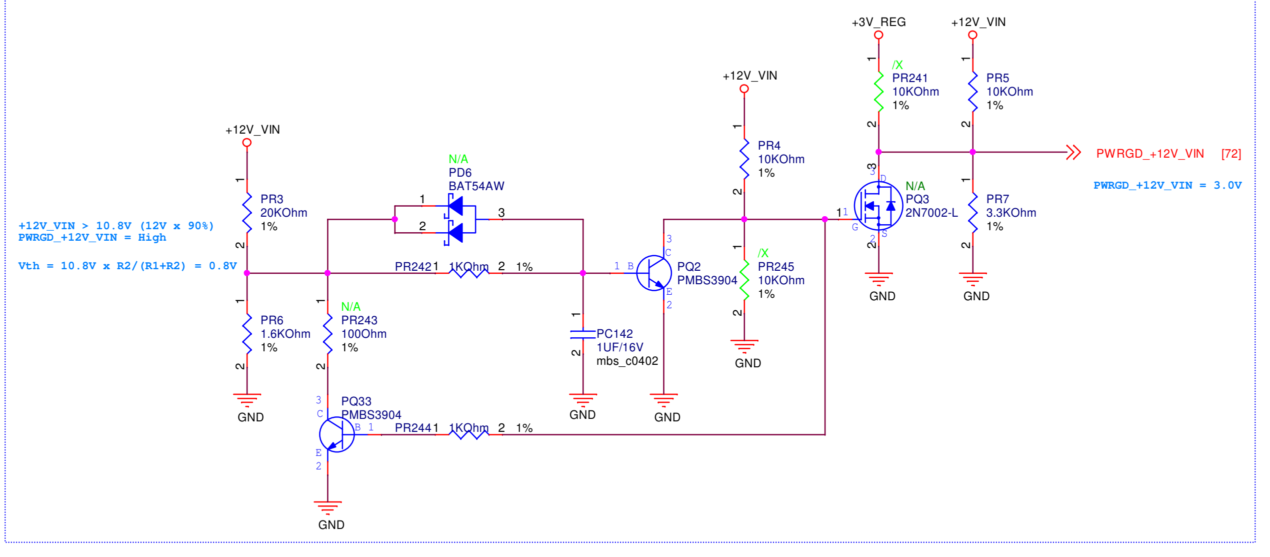
DC PWR INPUT



PWRGD +12V_VIN

R1.01 Change +12V_VIN PWRGD solution for AC off ring issue.(Optional)



ASUSTek COMPUTER INC.

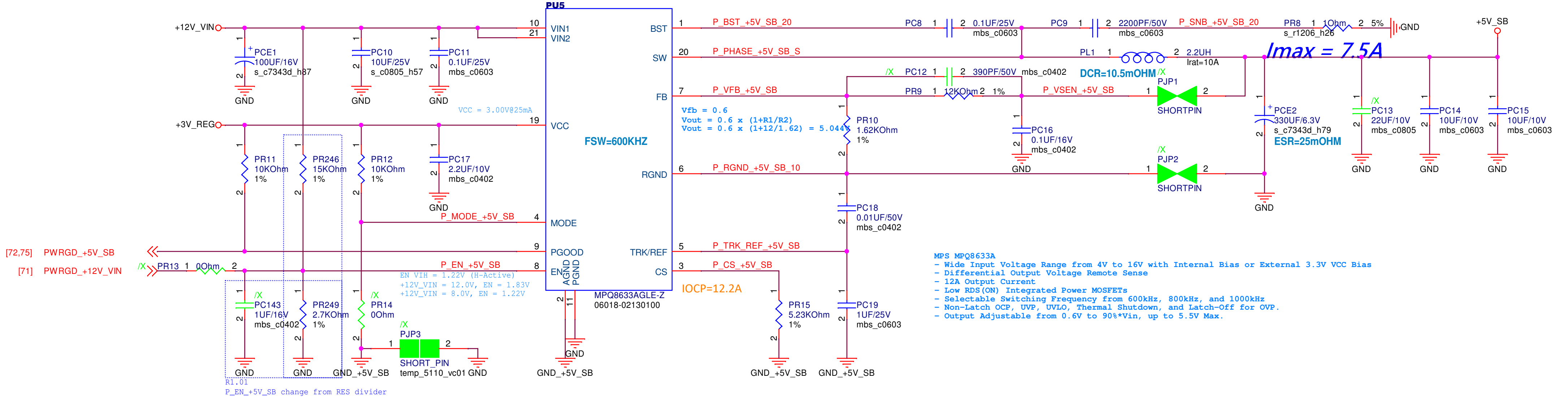
Title : PWR +12V_DCIN

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

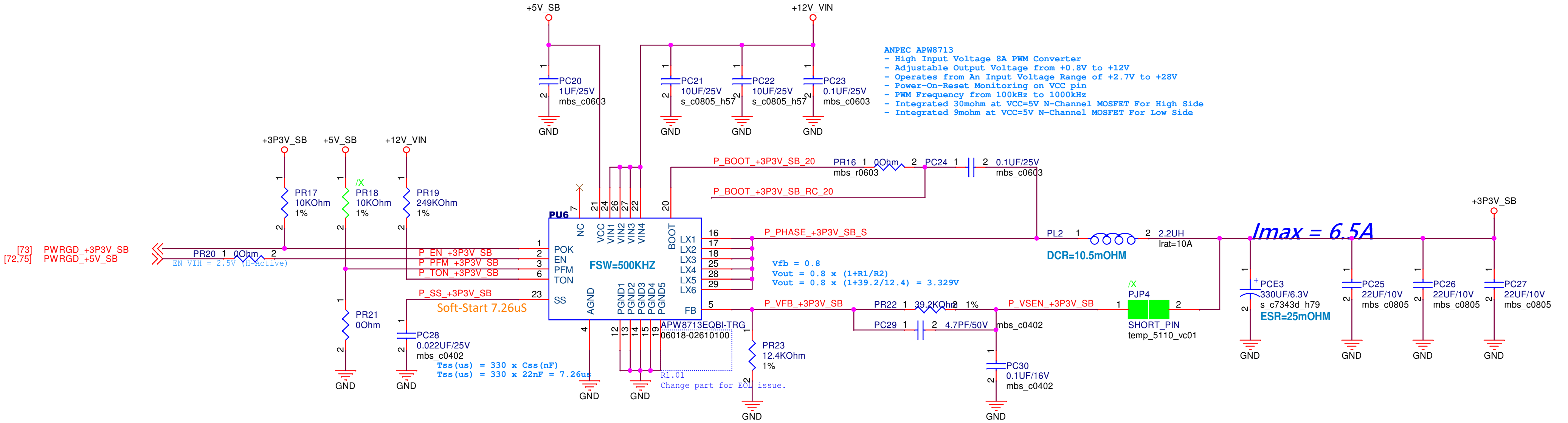
Date: Friday, July 16, 2021 Sheet 71 of 90

PWR +5V_SB



MPS MPQ8633A
- Wide Input Voltage Range from 4V to 16V with Internal Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- 12A Output Current
- Low RDS(ON) Integrated Power MOSFETs
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, UVLO, Thermal Shutdown, and Latch-Off for OVP.
- Output Adjustable from 0.6V to 90%*Vin, up to 5.5V Max.

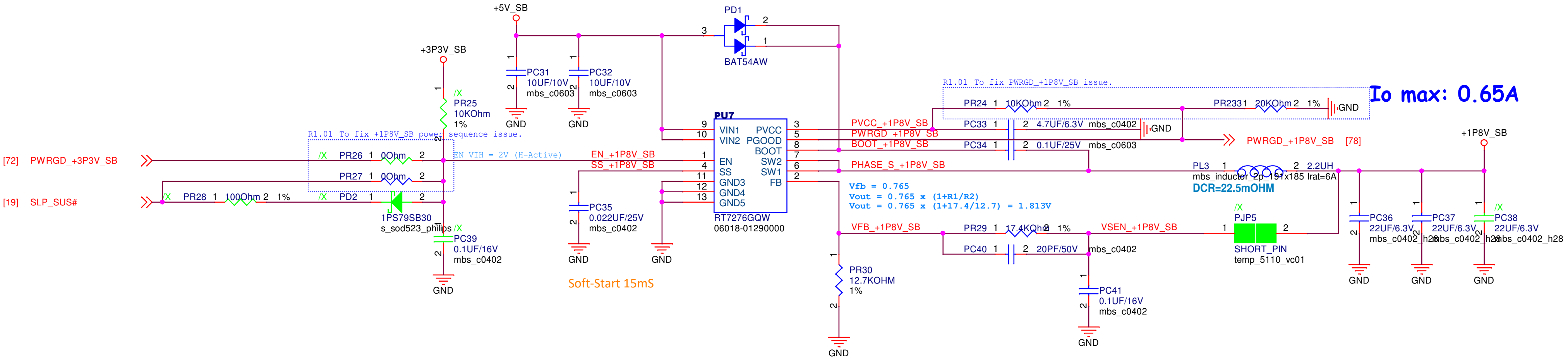
PWR +3P3V_SB



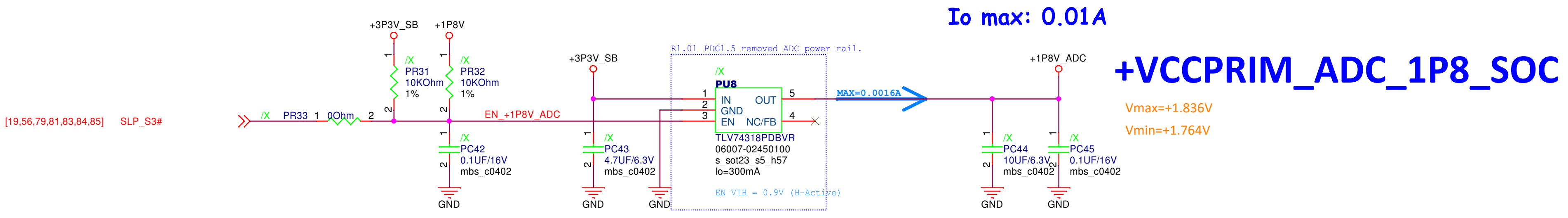
ANPEC APW8713
- High Input Voltage 8A PWM Converter
- Adjustable Output Voltage from +0.8V to +12V
- Operates from An Input Voltage Range of +2.7V to +28V
- Power-On-Reset Monitoring on VCC pin
- PWM Frequency from 100kHz to 1000kHz
- Integrated 30mohm at VCC=5V N-Channel MOSFET For High Side
- Integrated 9mohm at VCC=5V N-Channel MOSFET For Low Side

ASUSTek COMPUTER INC.	Title : PWR +5V_SB/+3P3V_SB		
	Engineer: Shawn Yu		
Size A3	Project Name MIX-EHLD1		Rev R1.01
Date: Friday, July 16, 2021	Sheet 72	of 90	

PWR +1P8V_SB



PWR +1P8V_ADC



ASUSTek COMPUTER INC.

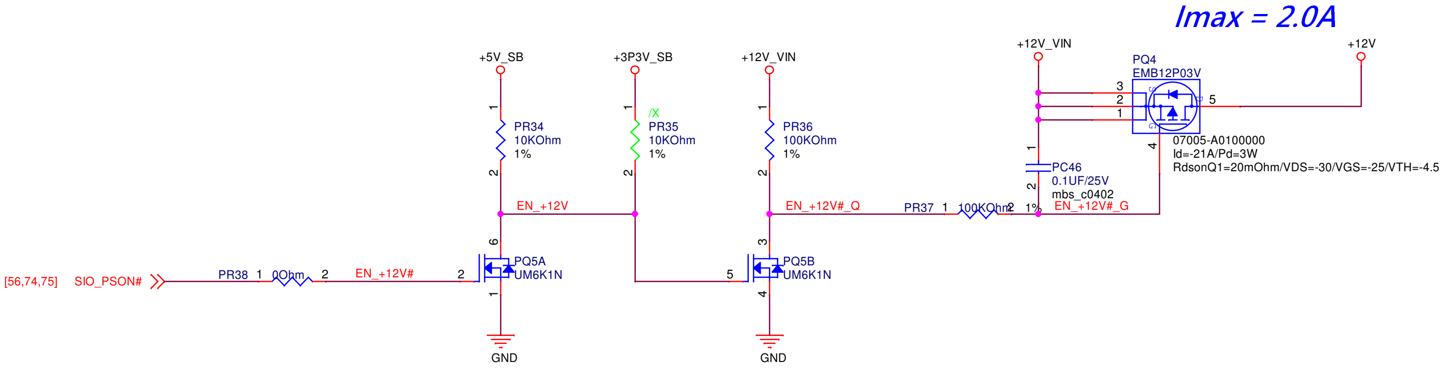
Title : PWR +1P8V_SB/+1P8V_

Engineer: Shawn Yu

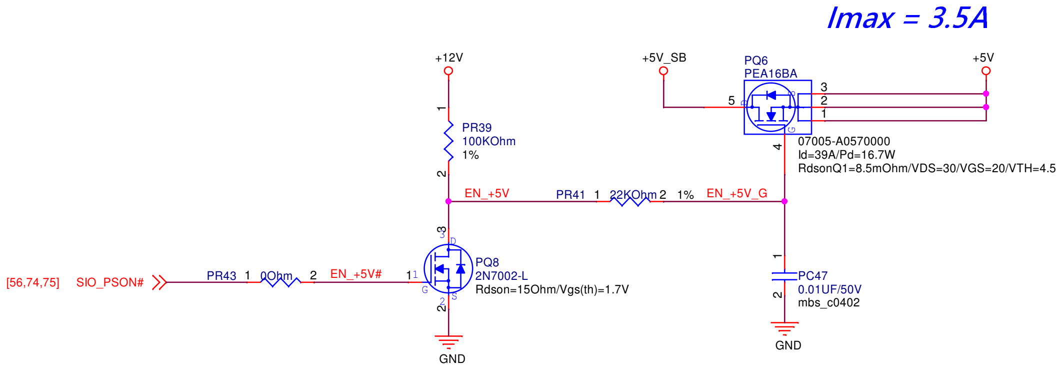
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 73 of 90

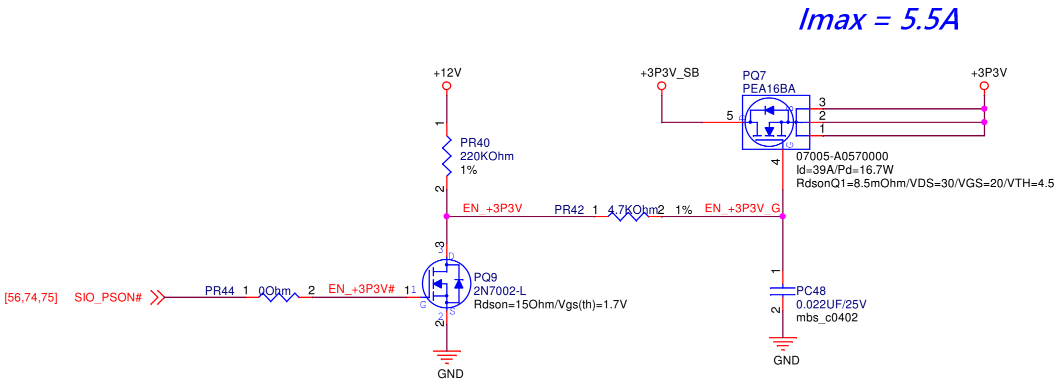
PWR +12V



PWR +5V



PWR +3P3V



Title : PWR +12V/+5V/+3P3V

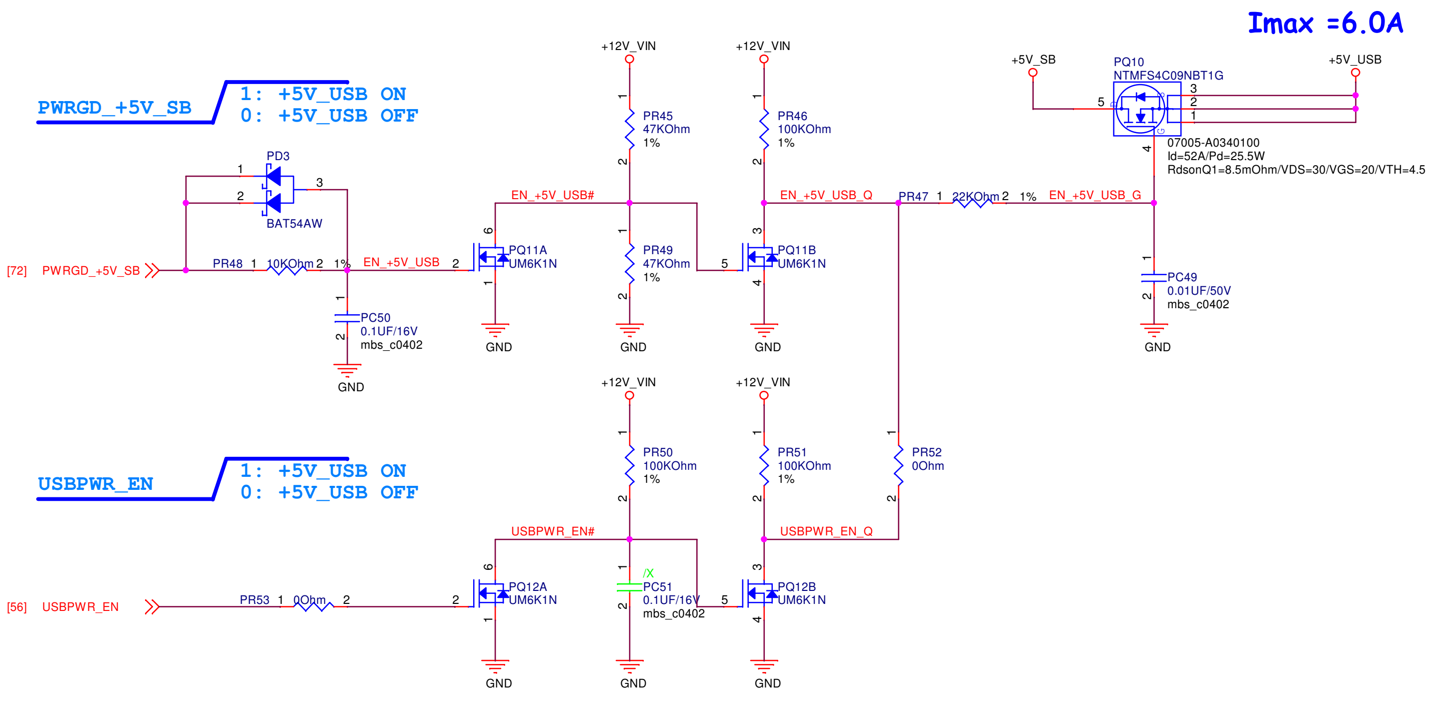
ASUSTek COMPUTER INC.

Engineer: Shawn Yu

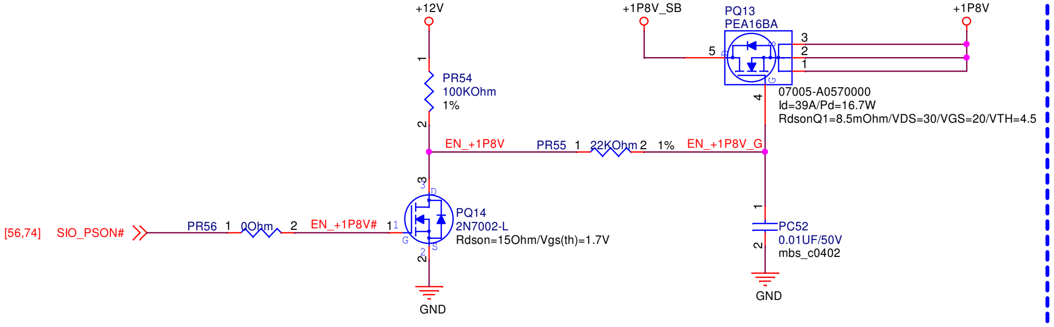
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 74 of 90

PWR +5V_USB



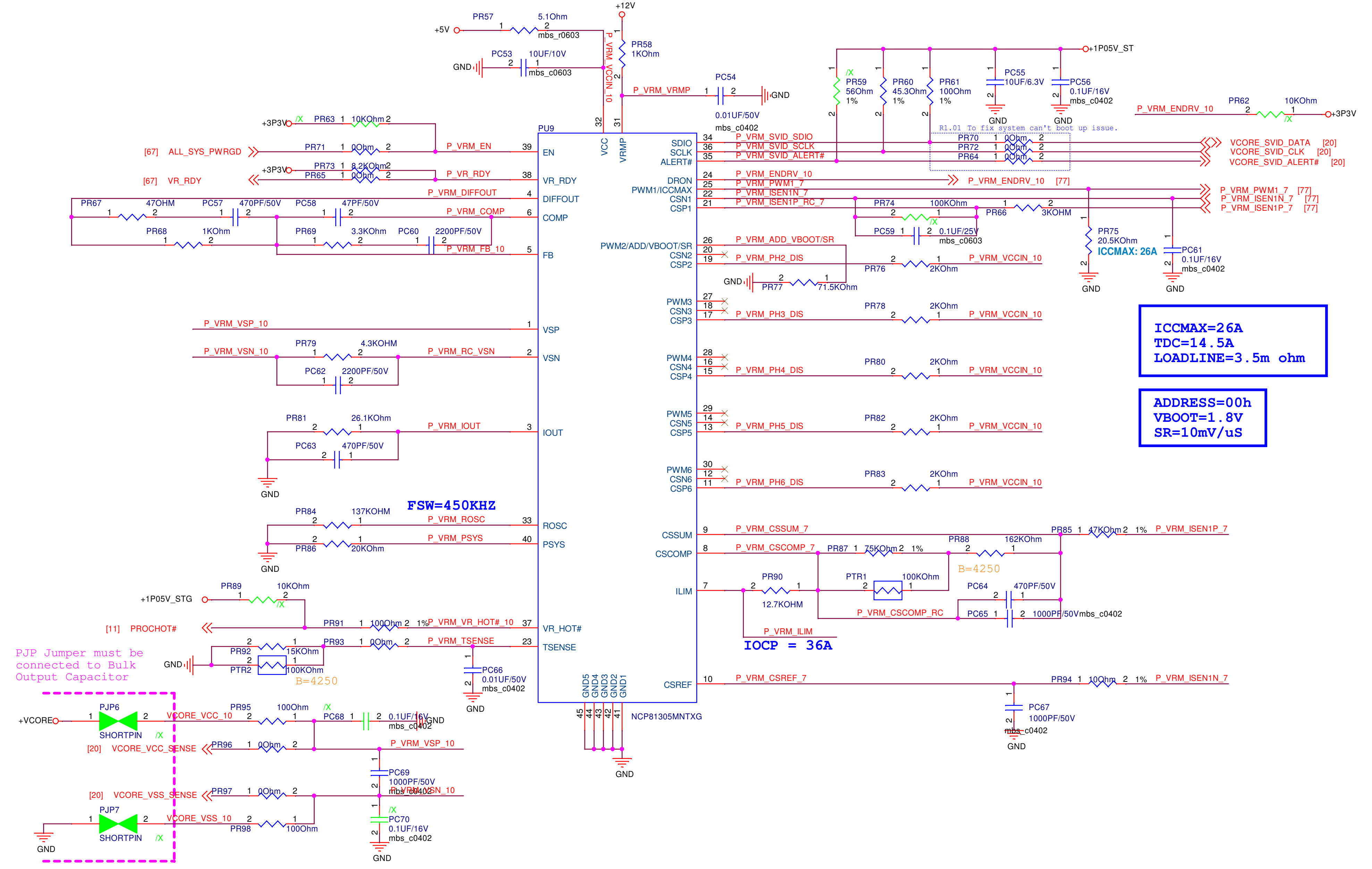
PWR +1P8V



N/A

ASUSTek COMPUTER INC.	Title : **PWR +1P8V/+5V_USB**	
	Engineer: **Shawn Yu**	
Size A3	Project Name **MIX-EHLD1**	Rev R1.01
Date: Thursday, July 15, 2021	Sheet 75 of 90	

PWR +VCORE



ICCMAX=26A
TDC=14.5A
LOADLINE=3.5m ohm

ADDRESS=00h
VBOOT=1.8V
SR=10mV/uS

ASUSTek COMPUTER INC.

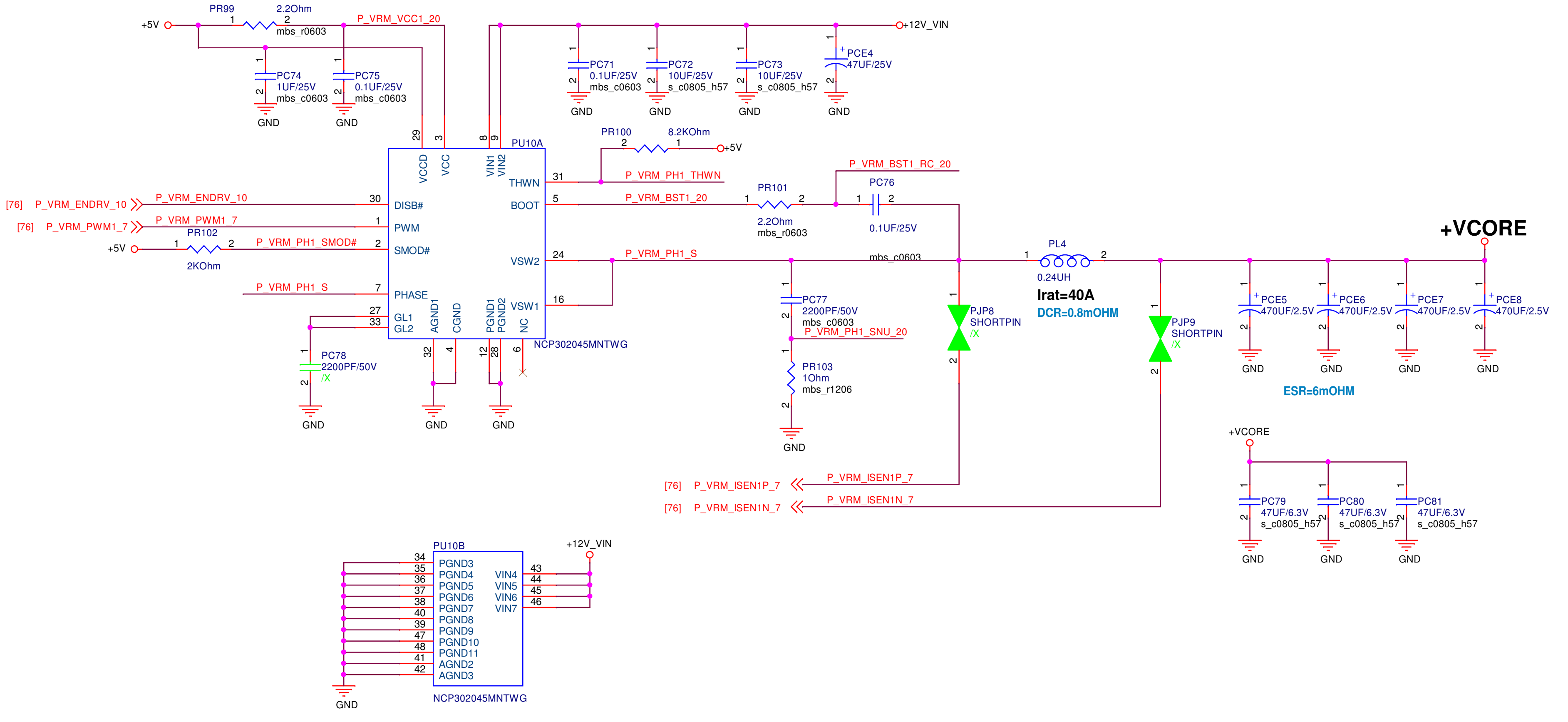
Title : PWR +VCORE CONTROL

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 76 of 90

PWR +VCORE



Title : **PWR +VCORE**

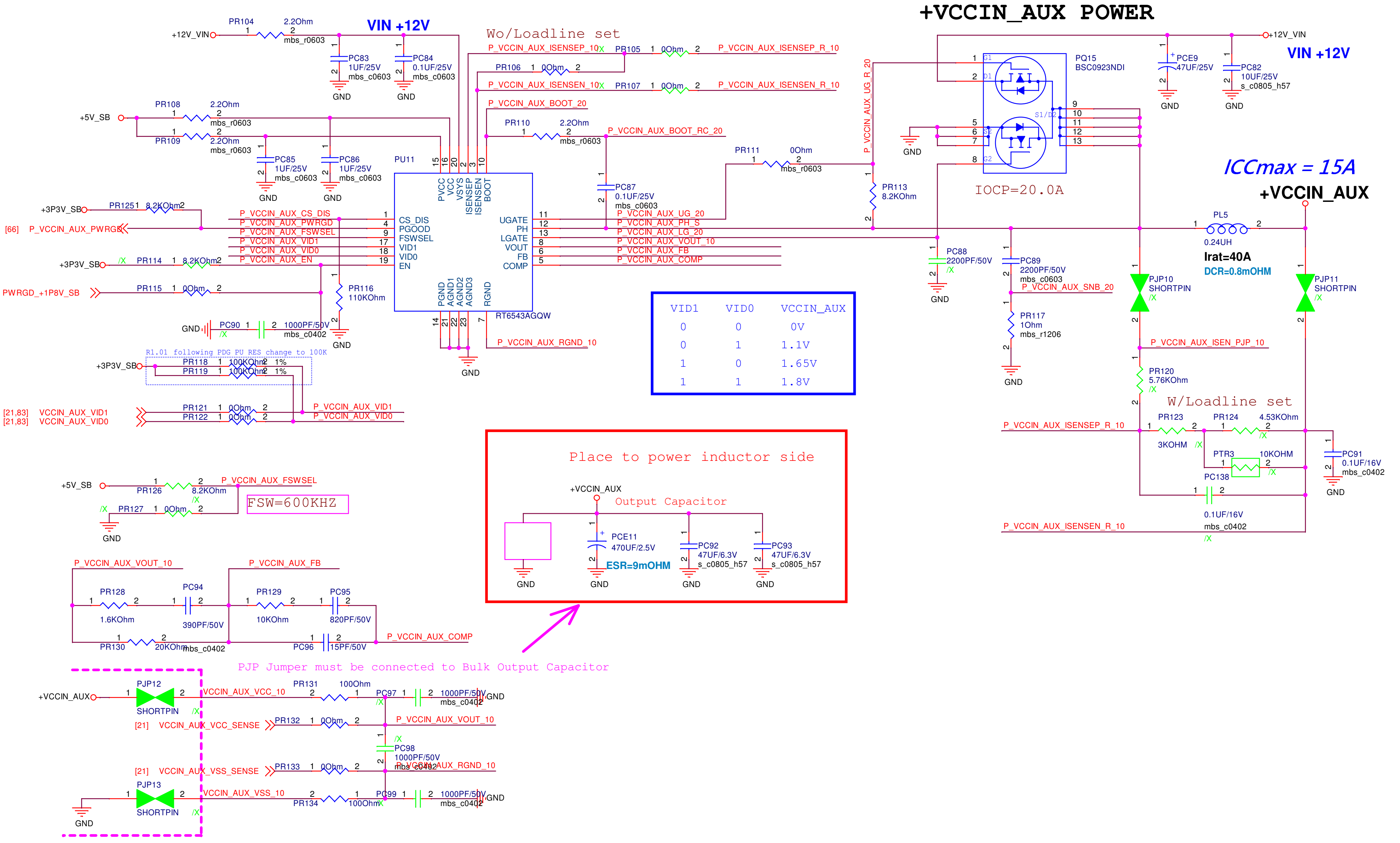
ASUSTek COMPUTER INC.

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 77 of 90

PWR +VCCIN_AUX



VID1	VID0	VCCIN_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

ASUSTek COMPUTER INC.

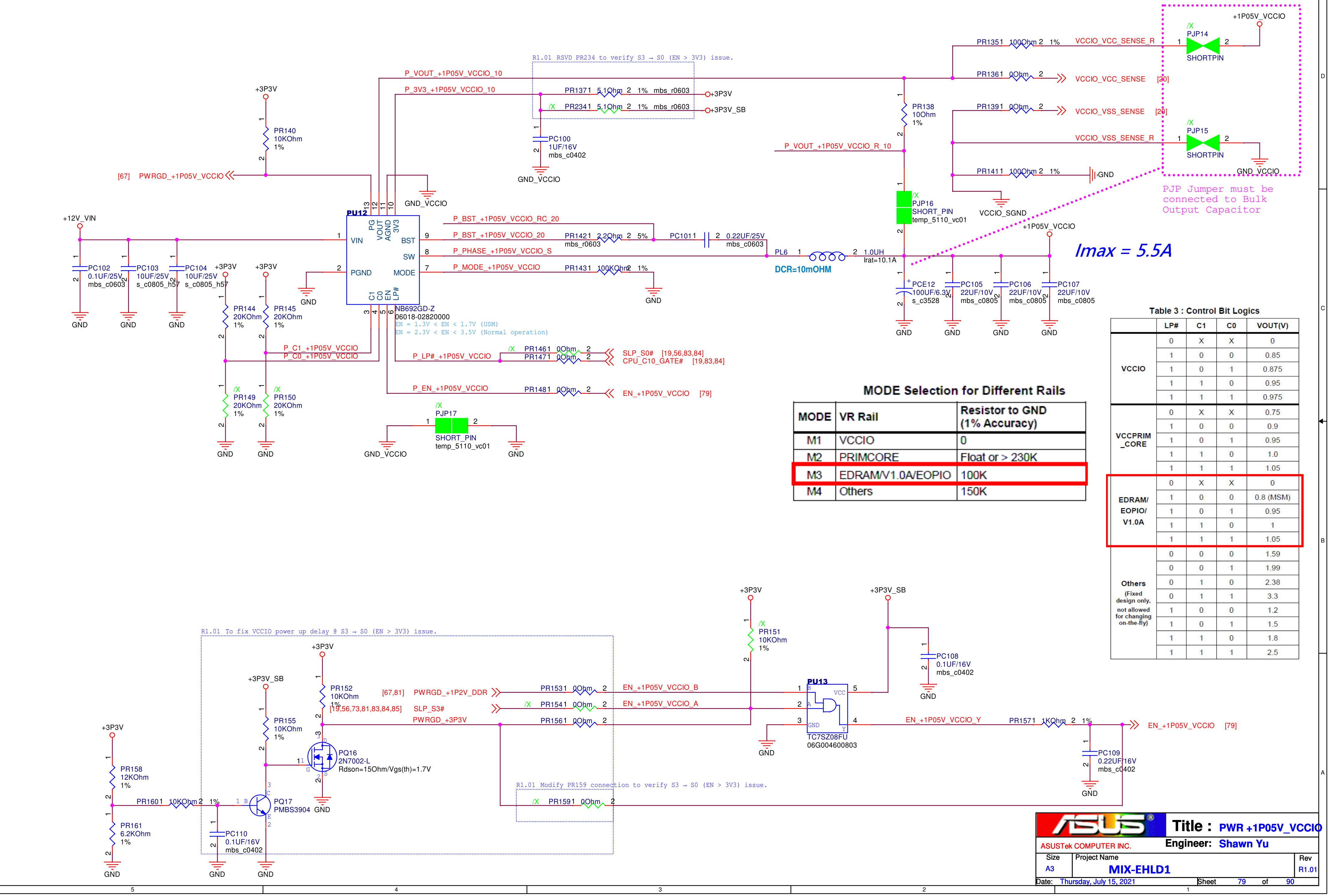
Title : PWR +VCCIN_AUX

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 78 of 90

PWR +1P05V_VCCIO



MODE Selection for Different Rails

MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

Table 3 : Control Bit Logics

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.75
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1.0
	1	1	1	1.05
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

ASUSTek COMPUTER INC.
Title : PWR +1P05V_VCCIO
Engineer: Shawn Yu
Size A3
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
Sheet 79 of 90

N/A

N/A

Title : PWR +1P05V_BYP

ASUSTek COMPUTER INC.

Engineer: Shawn Yu

Size	Project Name	Rev
A3	**MIX-EHLD1**	R1.01

Date: Thursday, July 15, 2021 Sheet 80 of 90

PWR +1P2V_DDR

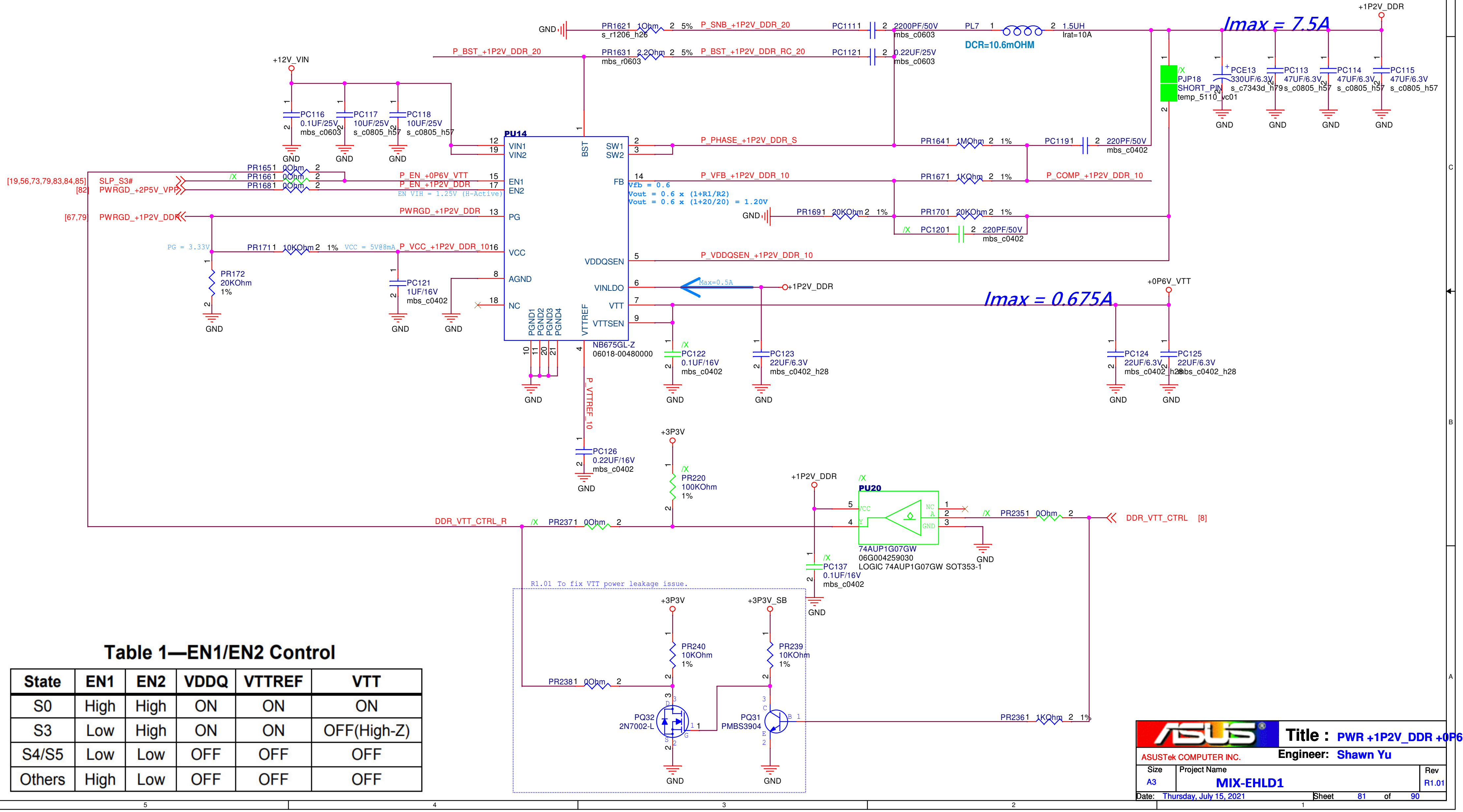


Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

ASUSTek COMPUTER INC.

Title : PWR +1P2V_DDR +0P6V

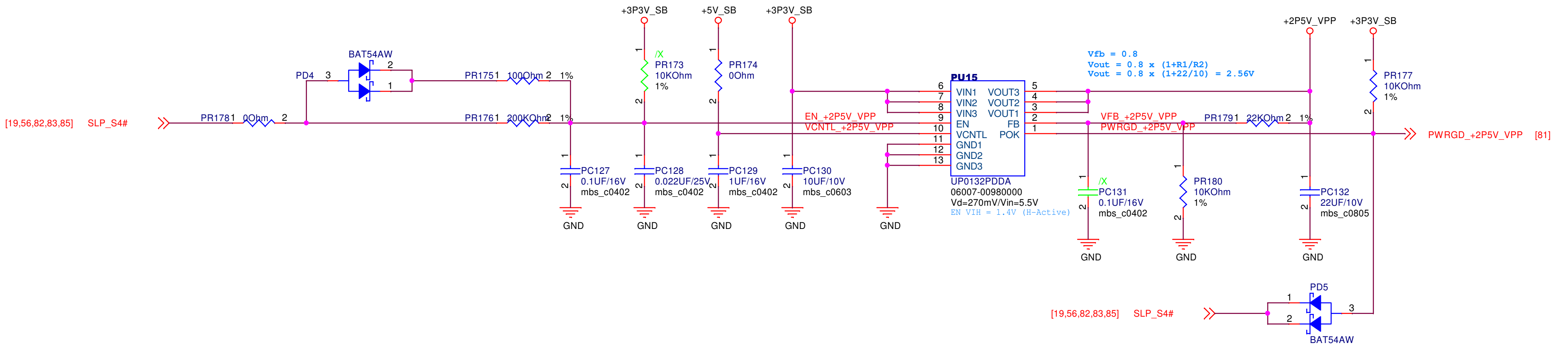
Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 81 of 90

PWR +2P5V_VPP

Imax = 0.4A



N/A

Title : **PWR +2P5V_VPP**

ASUSTek COMPUTER INC.

Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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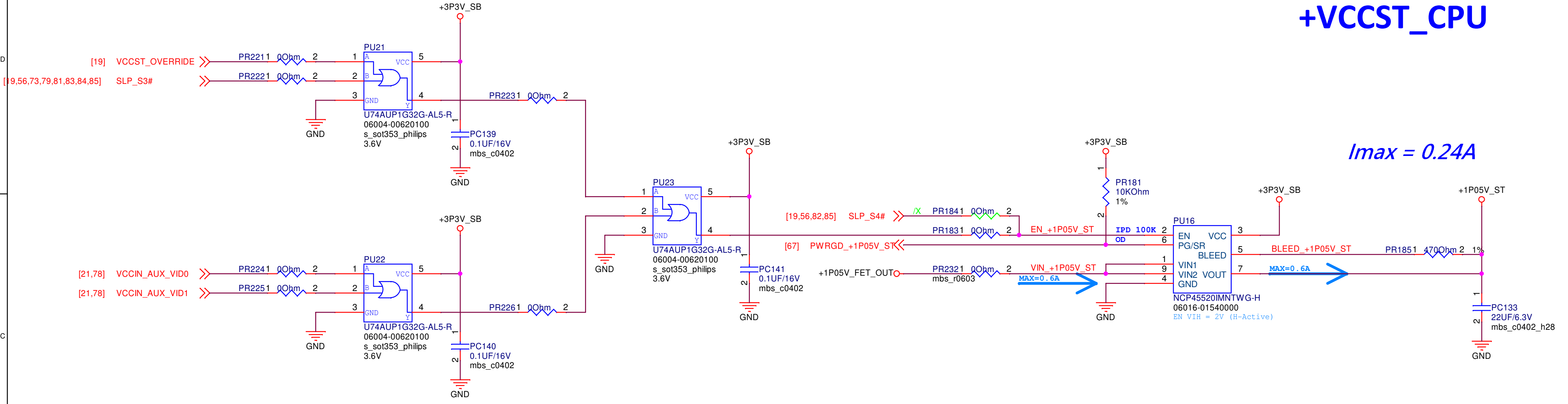
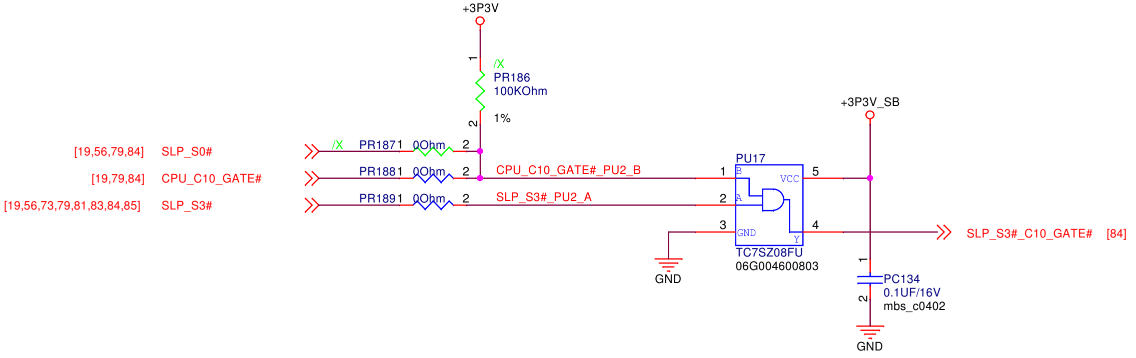
PWR +1P05V_ST



+VCCST_CPU

Imax = 0.24A

SEQ SLP_S3#_C10_GATE#



ASUSTek COMPUTER INC.

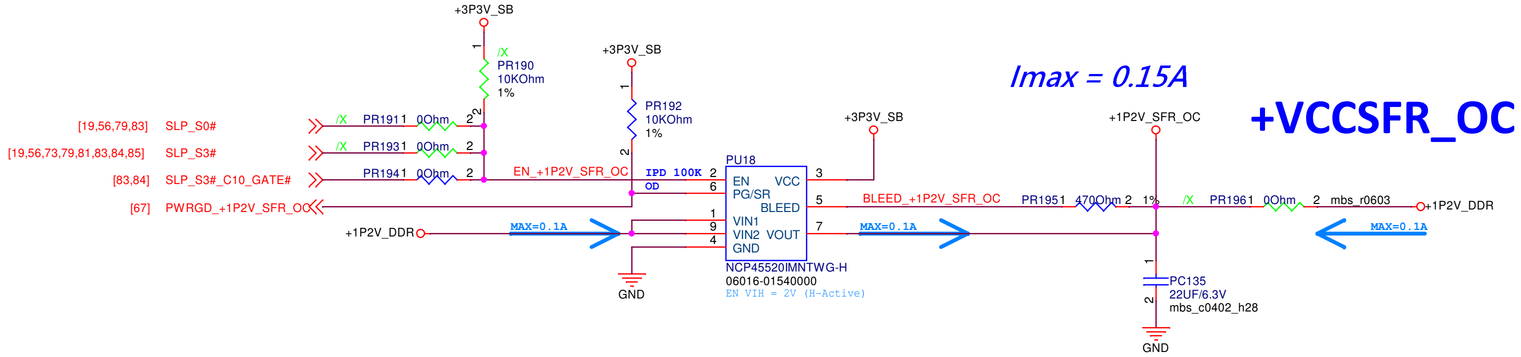
Title : PWR +VCCST

Engineer: Shawn Yu

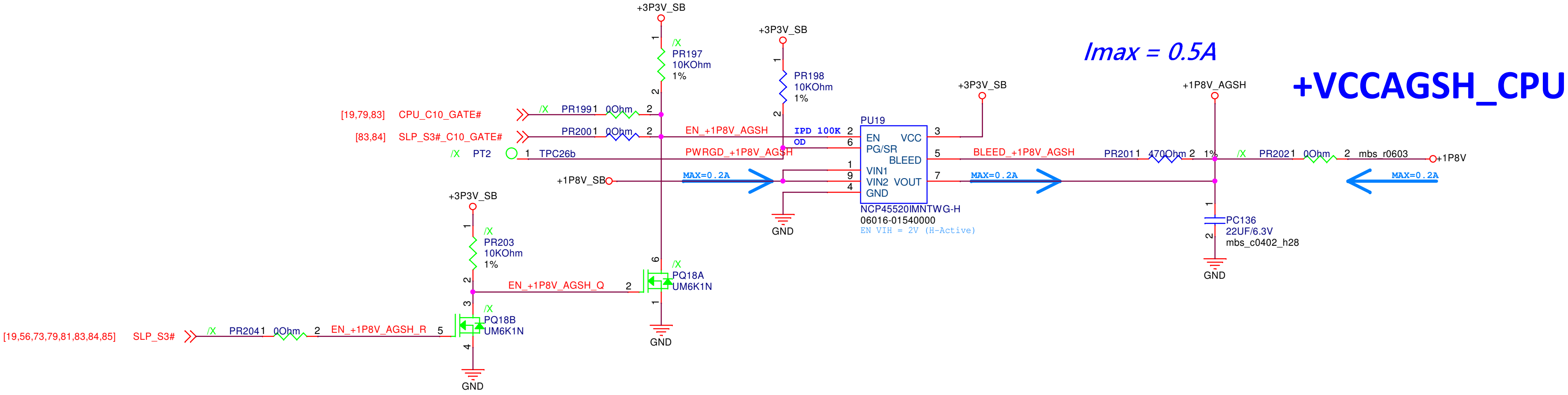
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 83 of 90

PWR +1P2V_SFR_OC



PWR +1P8V_AGSH



ASUSTek COMPUTER INC.

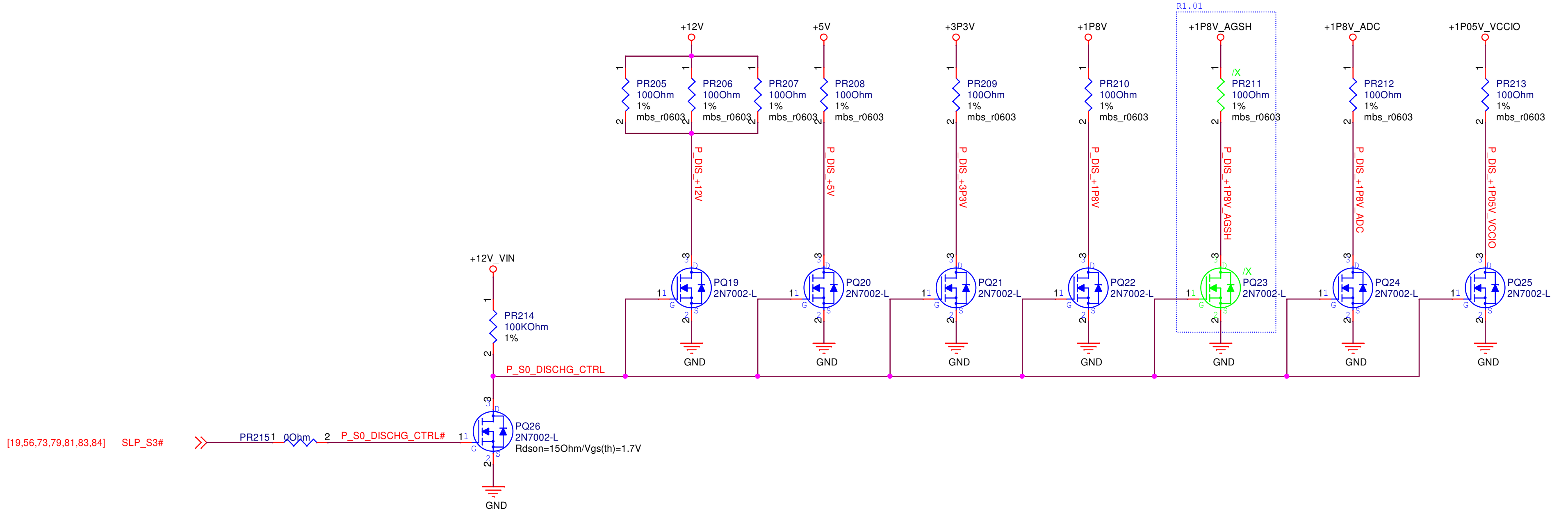
Title : PWR +VCCSFR_OC/+VC

Engineer: Shawn Yu

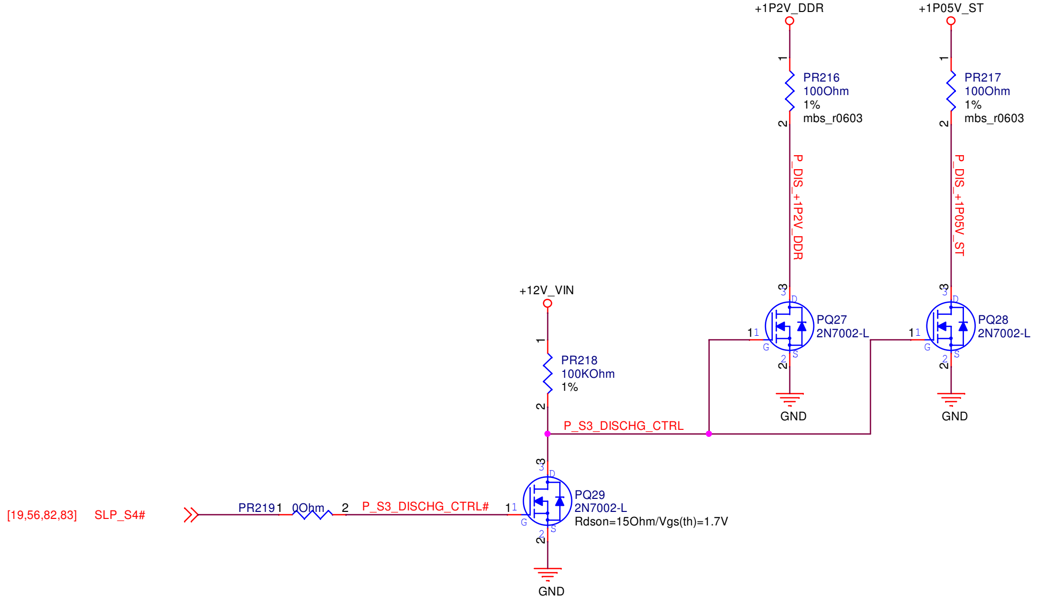
Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 84 of 90

PWR S0 POWER DISCHARGE



PWR S3 POWER DISCHARGE



ASUSTek COMPUTER INC.

Title : PWR DISCHARGE

Engineer: Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

Date: Thursday, July 15, 2021 Sheet 85 of 90

N/A

N/A

N/A

	Title : xxx
ASUSTek COMPUTER INC.	**Engineer:** Shawn Yu

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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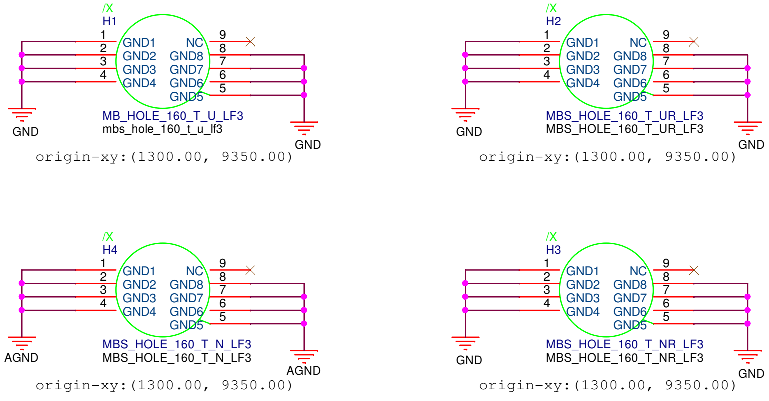
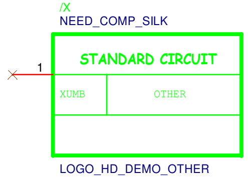
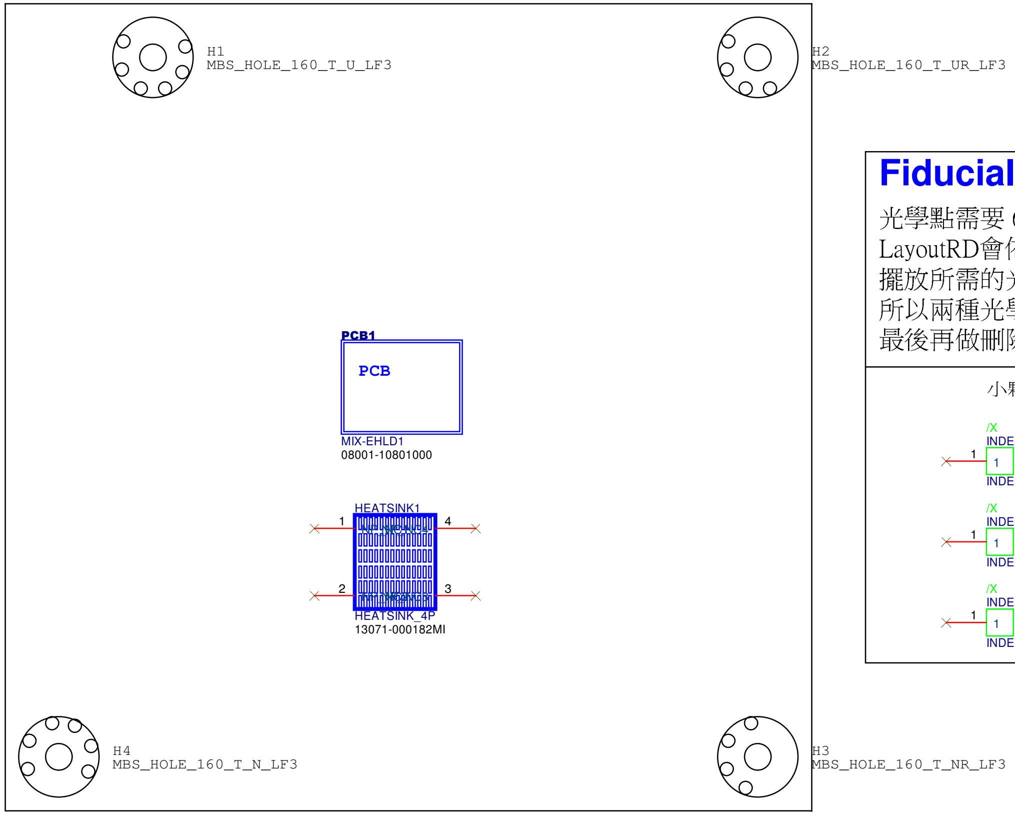
PCB & SCREW_HOLE & LOGO



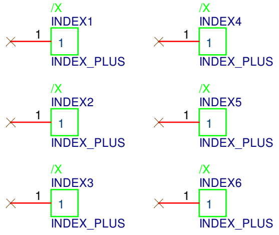




Fiducial Mask (光學點)

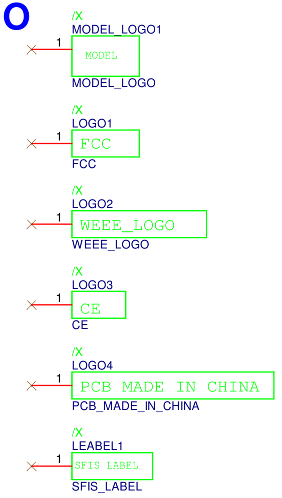
光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

小顆十字光學點



MODEL_LOGO: MIX-EHLD1

LOGO



ASUSTek COMPUTER INC.
Title : PCB&SCREW HOLE&LO
Engineer: Shawn Yu
Size A3
Project Name MIX-EHLD1
Rev R1.01
Date: Thursday, July 15, 2021
Sheet 89 of 90

Revision History

R1.00 (First Release)

R1.01 Change List, Date: 2021/07/15

01. Page21: Add HR231, +1P8V_CLKLDO_SOC connected to +1P8V_SB. To fix no clock issue.
02. Page73: PR26→NI, PR27→I, +1P8V_SB enable signal change to SLP_SUS#. To fix +1P8V_SB power sequence issue.
03. Page73: Add PR233, PWRGD_+1P8V_SB pull-high change to PVCC. To fix PWRGD_+1P8V_SB issue.
04. Page76: PR64 from 220ohm change to 0ohm. To fix SVID_ALERT# signal level lead to the system can't boot issue.
05. Page56: Add O2R67, O2R68, O2Q3, RSVD SLP_S3# to control PSON#.
06. Page57: RSVD O2R66 pull-high to +3P3V for Big-Code PLAT HW strap.
07. Page57: AT_ATX_SEL strap default change to ATX mode.
08. Page64: ATX_AT1 jumper default change to ATX mode.
09. Page79: PR154→NI, PR156→I, PC110→I. To fix VCCIO power up delay @ S3 → S0 (EN > 3V3) issue.
10. Page79: RSVD PR234 connected to +3P3V_SB & modify PR159 connection to verify S3 → S0 (EN > 3V3) issue.
11. Page30: f/w update to 2021042201.bin. To fix LVDS S3 resume no display issue.
12. Page30: LVR3 = 0ohm for ES sample, LVR3 = 10K for MP sample.
13. Page30: RSVD LVR57 pull-high to +3P3V_SB to verify RST# timing
14. Page31: eDP/LVDS jumper change to BKL_PWR1=5V(2-3), PNL_PWR1=3.3V(2-3), CTL_SEL1=DC(1-2).
15. Page81: The DDR_VTT_CTRL level shifter solution change to BJT+NMOS to fix VTT power lekage issue.
16. Page17: X1_38P4M1 CL 15PF → 10PF
17. Page30: X3_27M1 CL 20PF → 8.2PF
18. Page45: X4_25M1 CL 10PF → 12PF
19. Page47: X5_25M2 CL 10PF → 12PF
20. Page23: Add HR232 0ohm & HR233 100Kohm, to follow the ww06’21 update and PDG2.0 recommended.
21. Page73: Removed +1P8V_ADC power, following PDG2.0
22. Page21: HR164 change to 0ohm, default = I, following CRB Fab.C
23. Page61: Add RI# to WAKE# isolation for wake on lan issue.
24. Page78: VCCIN_AUX_VID0/1 pull-high PR118, PR119 from 8.2K change to 100K, following PDG2.0.
25. Page34: HDMI level shifter solution change to TDP158 co-lay SN75DP159.
26. Page35: HDMI CLK add HDC24 0.5PF/50V for EMI.
27. Page53: Audio AMP. solution form EUA2012AJIR1 change to EUA2075JIR1
28. Page64: Add SYS_RESET# debounce circuit for reset glitch lead to system hang issue.
29. Page64: AT/ATX circuit follow IPC standard design.
30. Page14: Del LVDS PWM signal
31. Page56: FAN control signal from SYSFAN change to CPUFAN
32. Page56: LVDS_PWM control signal from SOC change to SIO SYSFAN_OUT
33. Page85: +1P8V_AGSH discharge PR211, PQ23 change to NI
34. Page62: SPI disabled Quad I/O, SPU2, SPR7, SPR8, SPR10, SPC4 change to NI.
35. Page62: SPI FLASH use common part WSON-8 package.
36. Page71: Change +12V_VIN PWRGD solution for AC off ring issue.(Optional)
37. Page72: Add RES divider for P_EN_+5V_SB
38. Page66: DPWROK SQU2 VCC change to +12V_VIN for power loss sequence tPCH14
39. Page66: RSMRST# RMU3 VCC change to +12V_VIN for power loss sequence tPCH12, and add DPWROK drop control circuit.
40. Page72: PU6 part change to 06018-02610100
41. Page31: Add LVD1 for LVDS/eDP VDDEN isolation
42. Page12: M/B ID change to 0 0 1 (R1.01)

ASUSTek COMPUTER INC.
Title : **REVISION HISTORY**
Engineer: **Shawn Yu**

Size	Project Name	Rev
A3	MIX-EHLD1	R1.01

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