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Logical Device A3h: AAEON HAT Controller

Function and Device 00h: HAT Feature Version Information

OPRn	R/W	Description
00h	R	Reserve
01h	R	AAEON HAT Major Version
02h	R	AAEON HAT Minor Version

Option Register 01h: AAEON HAT Major Version

Bit	R/W	Default	Description
7-0	R	-	

Option Register 02h: AAEON HAT Minor Version

Bit	R/W	Default	Description
7-0	R	-	

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Function and Device 01h: Flexible GPIO Use Select Configuration

OPRn	R/W	Description
00h	R/W	Reserve
04-01h	R/W	Flexible GPIO Use Select Register

Option Register 04-01h: Flexible GPIO Use Select Register

Bit	R/W	Default	Description
27-0	R/W	-	GPIO_USE_SEL[27:0] — R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO.
31-28	R/W	-	Reserve

Function and Device 02h: Flexible GPIO Input/Output Select Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R	Flexible GPIO Input/Output Select Register

Option Register 04-01h: Flexible GPIO Input/Output Select Register

Bit	R/W	Default	Description
27-0	R/W	-	GP_IO_SEL[27:0] — R/W. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.
31-28	R/W	-	Reserve

Function and Device 03h: Flexible GPIO Level for Input or Output Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R/W	GPIO Level for Input or Output Register

Option Register 04-01h: Flexible GPIO Input/Output Select Register

Bit	R/W	Default	Description
27-0	R/W	-	GP_LVL[27:0]— R/W: If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode.
31-28	R/W	-	Reserve