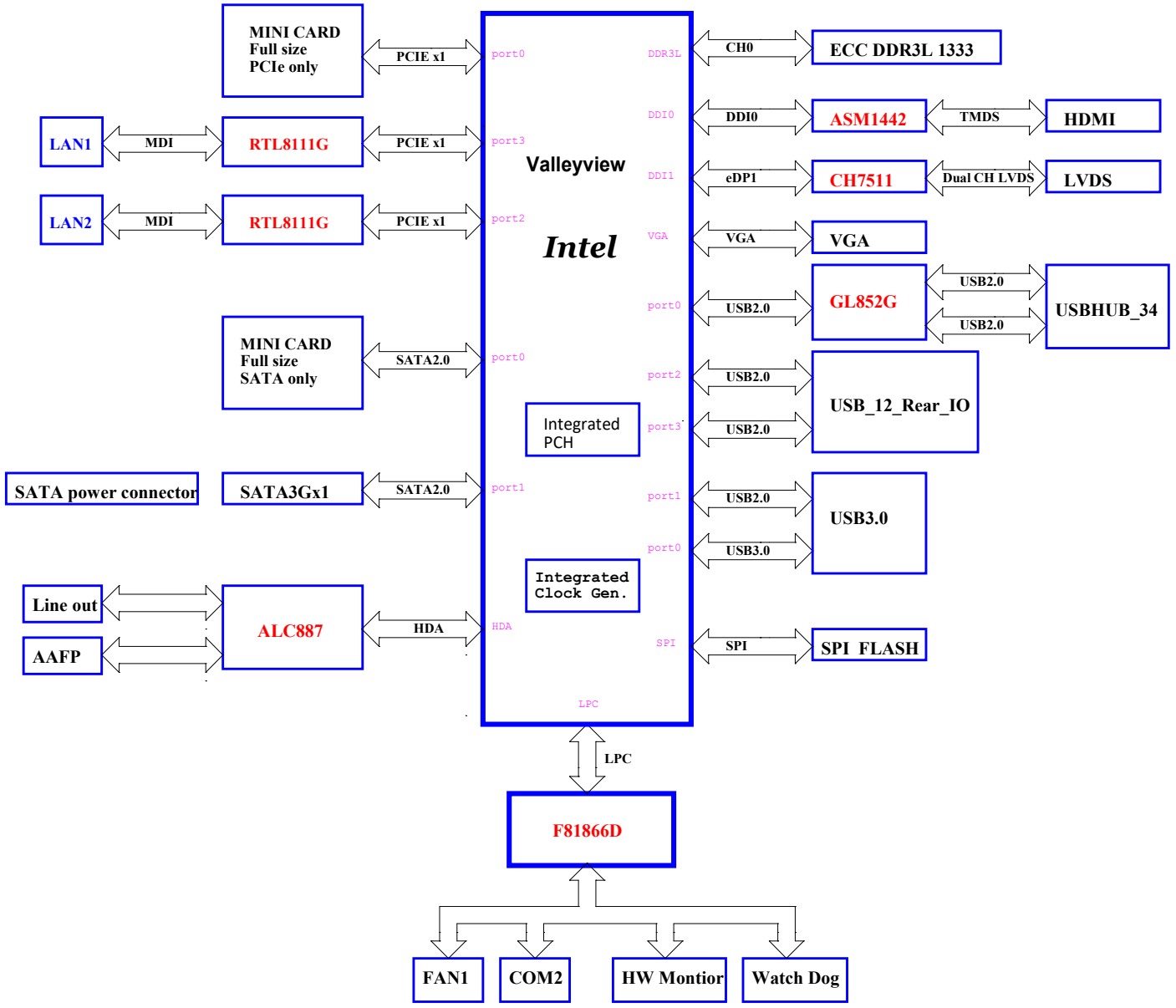
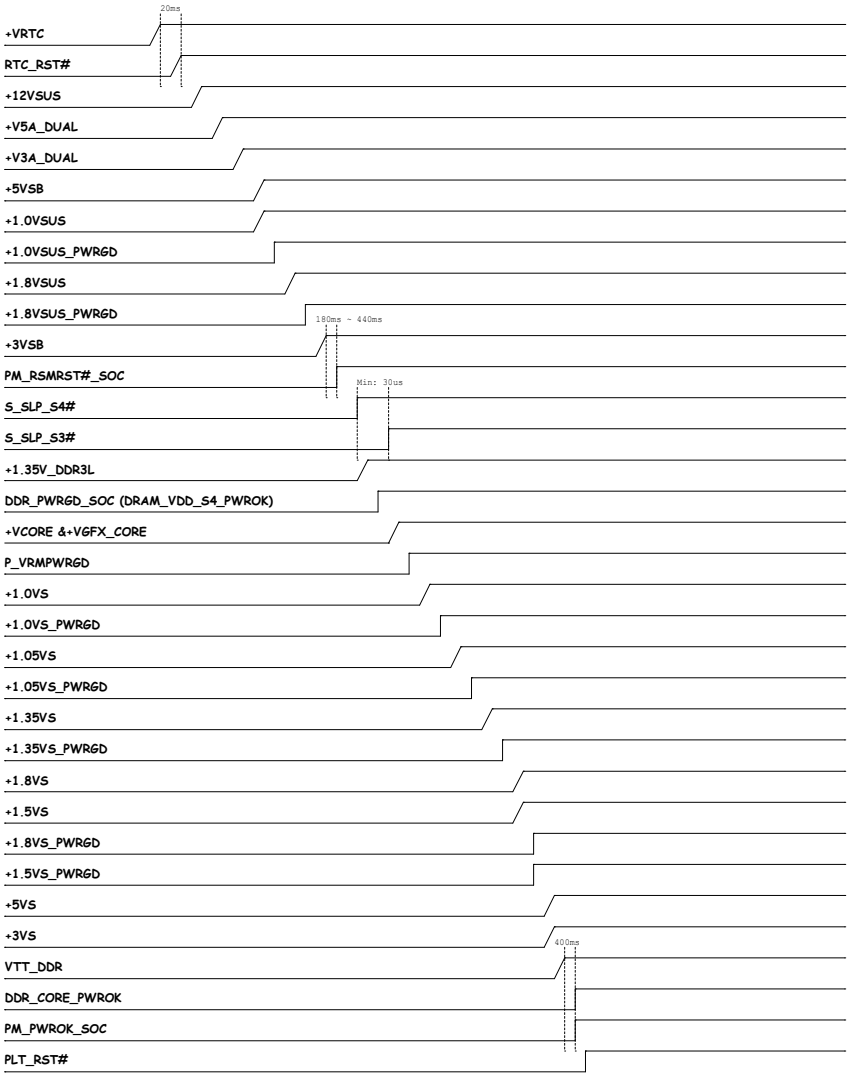
EMB-BT7-B10 Block Diagram

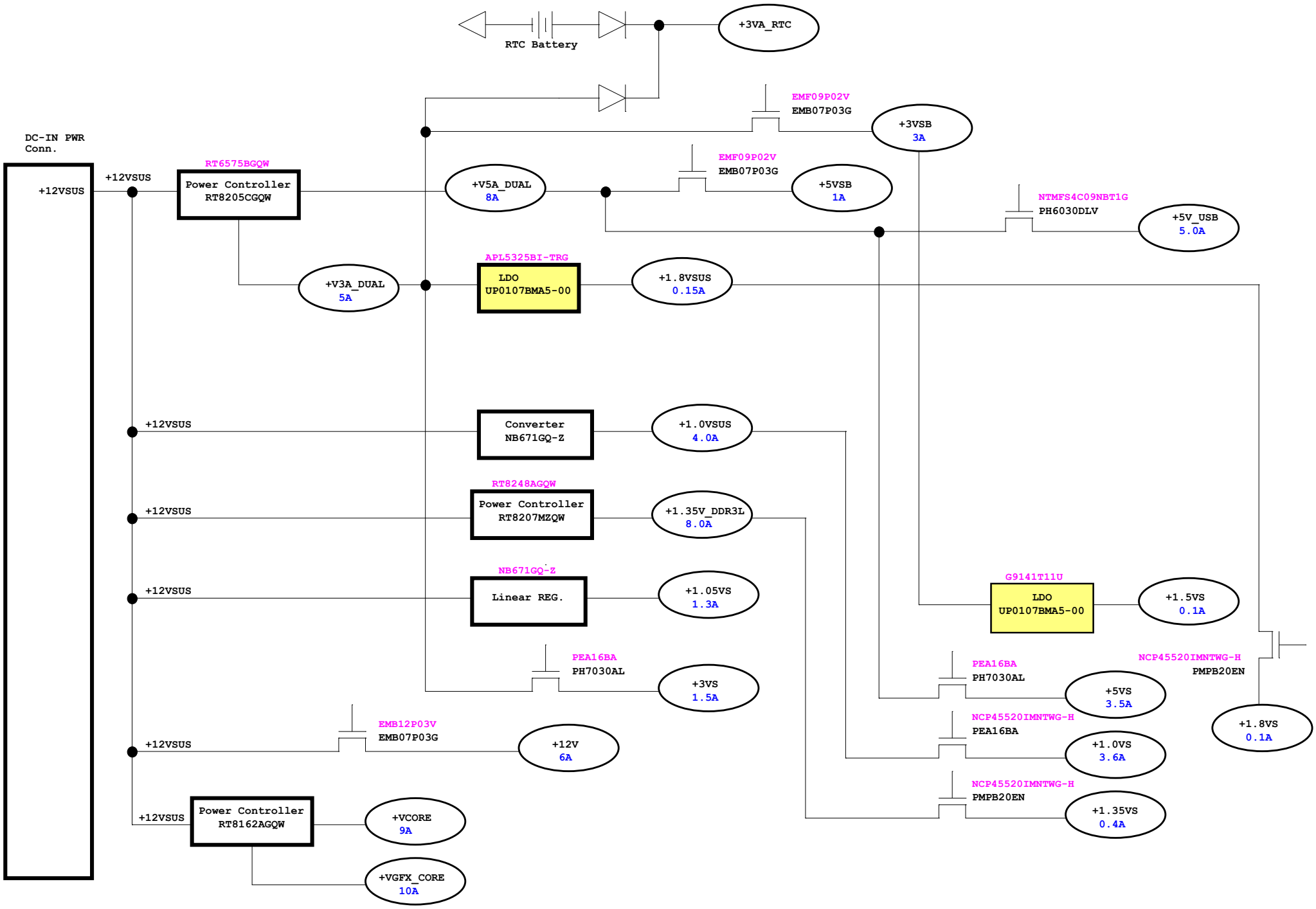


ASUSTeK COMPUTER INC.		Title : BLOCK DIAGRAM	
		Engineer:	
Size: C	Project Name: EMB-BT7		Rev: R2.00
Date: Friday, October 04, 2019	Sheet 1 of 60		

Power Up Sequence



ASUSTEK COMPUTER INC	Title : POWER SEQUENCE		
	Engineer:		
Size: C	Project Name: EMB-BT7		Rev: R2.00
Date: Friday, October 04, 2019	Sheet 2 of 60		



EMB-BT7

ASUSTEK COMPUTER INC

Title : POWER FLOW

Engineer:

Size	Project Name	Rev
C	EMB-BT7	R2.00

Date: Friday, October 04, 2019 Sheet 3 of 60

Title :	EMPTY
ASUSTEK COMPUTER INC	Engineer:
Size: Custom	Project Name: EMB-BT7
Rev: R2.00	
Date: Friday, October 04, 2019	Sheet 4 of 60

Title :	EMPTY
ASUSTEK COMPUTER INC	Engineer:
Size: Custom	Project Name: EMB-BT7
Rev: R2.00	
Date: Friday, October 04, 2019	Sheet 5 of 60

SOC (Bay Trail) GPIO Setting

	SOC_GPIO	Use As	Signal Name	Int & Ext Pull-up/down	Power
	GPIO_S0_SC[00]	Native	NC	INT PD	+1.8VS
	GPIO_S0_SC[01]	Native	NC	INT PD	+1.8VS
	GPIO_S0_SC[02]	Native	SATA_LED#	EXT PU	+1.8VS
	GPIO_S0_SC[03]	Native	CLKREQ_WLAN#	INT PU & EXT PU	+1.8VS
	GPIO_S0_SC[04]	Native	CLKREQ1# (NC)	INT PU & EXT PU	+1.8VS
	GPIO_S0_SC[05]	Native	CLKREQ2# (NC)	INT PU & EXT PU	+1.8VS
	GPIO_S0_SC[06]	Native	CLKREQ_GLAN#	INT PU & EXT PU	+1.8VS
	GPIO_S0_SC[07]				
	GPIO_S0_SC[08]	Native	ACZ_RST#	INT PD	+1.5VS
	GPIO_S0_SC[09]	Native	ACZ_SYNC	INT PD	+1.5VS
	GPIO_S0_SC[10]	Native	ACZ_BCLK	INT PD	+1.5VS
	GPIO_S0_SC[11]	Native	ACZ_SDOUT	INT PD	+1.5VS
	GPIO_S0_SC[12]	Native	ACZ_SDIN0_AUD	INT PD	+1.5VS
	GPIO_S0_SC[13]	Native	NC	INT PD	+1.5VS
	GPIO_S0_SC[14]	Native	NC	INT PD	+1.5VS
	GPIO_S0_SC[15]	Native	NC	INT PD	+1.5VS
*	GPIO_S0_SC[16]	Native	NC	INT PD	+1.8VS
*	GPIO_S0_SC[24:17]	Native	NC	INT PU	+1.8VS
	GPIO_S0_SC[25]	Native	NC	INT PU	+1.8VS
	GPIO_S0_SC[26]	Native	NC	INT PU	+1.8VS
*	GPIO_S0_SC[27]	Native	NC	INT PD	+1.8VS
	GPIO_S0_SC[31:28]	Native	NC	INT PU	+1.8VS
	GPIO_S0_SC[32]	Native	NC	INT PU	+1.8VS
*	GPIO_S0_SC[33]	Native	SD3_CLK	INT PD & EXT PU	+1.8VS/+3VS
	GPIO_S0_SC[37:34]	Native	SD3_D[3:0]	INT PU & EXT PU	+1.8VS/+3VS
	GPIO_S0_SC[38]	Native	SD3_CD#	INT PU & EXT PU	+1.8VS
	GPIO_S0_SC[39]	Native	SD3_CMD	INT PU & EXT PU	+1.8VS/+3VS
	GPIO_S0_SC[40]	Native	SD3_1P8_EN	INT PD	+1.8VS
	GPIO_S0_SC[41]	Native	SD3_PWR_EN#	INT PU & EXT PU	+1.8VS
	GPIO_S0_SC[45:42]	Native	LPC_AD[3:0]	INT PU	+3VS
	GPIO_S0_SC[46]	Native	LPC_FRAME#	INT PU	+3VS
	GPIO_S0_SC[47]	Native	L_CLKOUT0	INT PD	+3VS
	GPIO_S0_SC[48]	Native	L_CLKOUT1	INT PD	+3VS
	GPIO_S0_SC[49]	Native	PM_CLKRUN#_R	INT PU & EXT PU	+3VS
	GPIO_S0_SC[50]	Native	INT_SERIRQ_SOC_R	INT PU	+1.8VS
	GPIO_S0_SC[51]	Native	SMB_DATA_SOC	INT PU & EXT PU(NC)	+1.8VS
	GPIO_S0_SC[52]	Native	SMB_CLK_SOC	INT PU & EXT PU(NC)	+1.8VS
	GPIO_S0_SC[53]	Native	SMB_ALERT#_SOC	INT PU & EXT PU	+1.8VS
*	GPIO_S0_SC[54]	GPI	EC_SMB_INT2#		
	GPIO_S0_SC[55]	GPO	WWAN_ON#		+1.8VS
	GPIO_S0_SC[56]	GPI	STRAP_A16_SWAP	EXT PU	+1.8VS
	GPIO_S0_SC[57]	GPO	UART_TXD_DBG		+1.8VS
	GPIO_S0_SC[58]	GPI	MEMID0		+1.8VS
	GPIO_S0_SC[59]	GPI	MEMID1		+1.8VS
	GPIO_S0_SC[60]	GPI	MEMID2		+1.8VS
	GPIO_S0_SC[61]	GPI	UART_RXD_DBG		+1.8VS
	GPIO_S0_SC[62]	Native	NC		+1.8VS
	GPIO_S0_SC[63]	GPI	I2S_2_FRM	EXT PU	+1.8VS
	GPIO_S0_SC[64]	Native	NC		+1.8VS
	GPIO_S0_SC[65]	GPI	I2S_2_TXD	EXT PU	+1.8VS
	GPIO_S0_SC[66]	GPI	PCB_ID0	EXT PD	+1.8VS
	GPIO_S0_SC[67]	GPI	PCB_ID1	EXT PD	+1.8VS
	GPIO_S0_SC[68]	Native	NC		+1.8VS
	GPIO_S0_SC[69]	Native	NC		+1.8VS
	GPIO_S0_SC[77:70]	Native	NC	INT PU	+1.8VS
	GPIO_S0_SC[83:78]	Native	NC	INT PU	+1.8VS
*	GPIO_S0_SC[84]	Native	EC_SMB_DAT2		+1.8VS
*	GPIO_S0_SC[85]	Native	EC_SMB_CLK2		+1.8VS
*	GPIO_S0_SC[86]	Native	EC_SMB_DAT3		+1.8VS
*	GPIO_S0_SC[87]	Native	EC_SMB_CLK3		+1.8VS
	GPIO_S0_SC[88]	GPO	WLAN_LED	INT PU	+1.8VS
	GPIO_S0_SC[89]	GPO	BT_LED	INT PU	+1.8VS
	GPIO_S0_SC[90]	Native	NC	INT PU	+1.8VS
	GPIO_S0_SC[91]	GPIO	SD3_WP	INT PU & EXT PU(NC)	+1.8VS
	GPIO_S0_SC[92]	GPO	WLAN_ON#		+1.8VS
	GPIO_S0_SC[93]	GPO	BT_ON#		+1.8VS
	GPIO_S0_SC[94]	Native	NC		+1.8VS
	GPIO_S0_SC[95]	Native	NC		+1.8VS
	GPIO_S0_SC[:10196]	Native	NC		+1.8VS

SOC (Bay Trail) GPIO Setting

	SOC_GPIO	Use As	Signal Name	Int & Ext Pull-up/down	Power
	GPIO_S5[0]	GPI	EC_WAKE_SCI_SOC		+1.8VSUS
	GPIO_S5[3:1]	Native	NC	INT PU	+1.8VS
	GPIO_S5[4]	Native	NC		+1.8VS
	GPIO_S5[6:5]	Native	NC		+1.8VS
	GPIO_S5[7]	GPI	EXT_SMI#_SOC		+1.8VSUS
	GPIO_S5[8]	Native	NC		+1.8VS
	GPIO_S5[9]	Native	NFC_RST#_R		+1.8VS
	GPIO_S5[10]	Native	NFC_INT_R		+1.8VS
	GPIO_S5[11]	Native	ME_SUSPWRDNACK		+1.8VS
	GPIO_S5[12]	Native	NC		+1.8VS
	GPIO_S5[13]	Native	SLP_S0IX#_18		+1.8VSUS
	GPIO_S5[14]	Native	SLP_LAN#	EXT PU(NC)	+1.8VS
	GPIO_S5[15]	Native	PCIE_WAKE#	INT PU & EXT PU	+1.8VSUS
	GPIO_S5[16]	Native	PM_PWRBTN#_18	INT PU	+1.8VSUS
	GPIO_S5[17]	Native	NC		+1.8VS
	GPIO_S5[18]	Native	NC		+1.8VS
	GPIO_S5[19]	Native	USB_OC_0#	INT PU & EXT PU	+1.8VSUS
	GPIO_S5[20]	Native	USB_OC_0#	INT PU & EXT PU	+1.8VSUS
*	GPIO_S5[21]	GPI	SPI_SO_SPI	INT PU	+1.8VS
*	GPIO_S5[30:22]	GPIO	XDP_GPIO_DFX[8:0]		+1.8VS
*	GPIO_S5[31]	GPI	EC_SMB_INT3#		+1.8VSUS
	GPIO_S5[43:32]	Native	NC		+1.8VS
*					

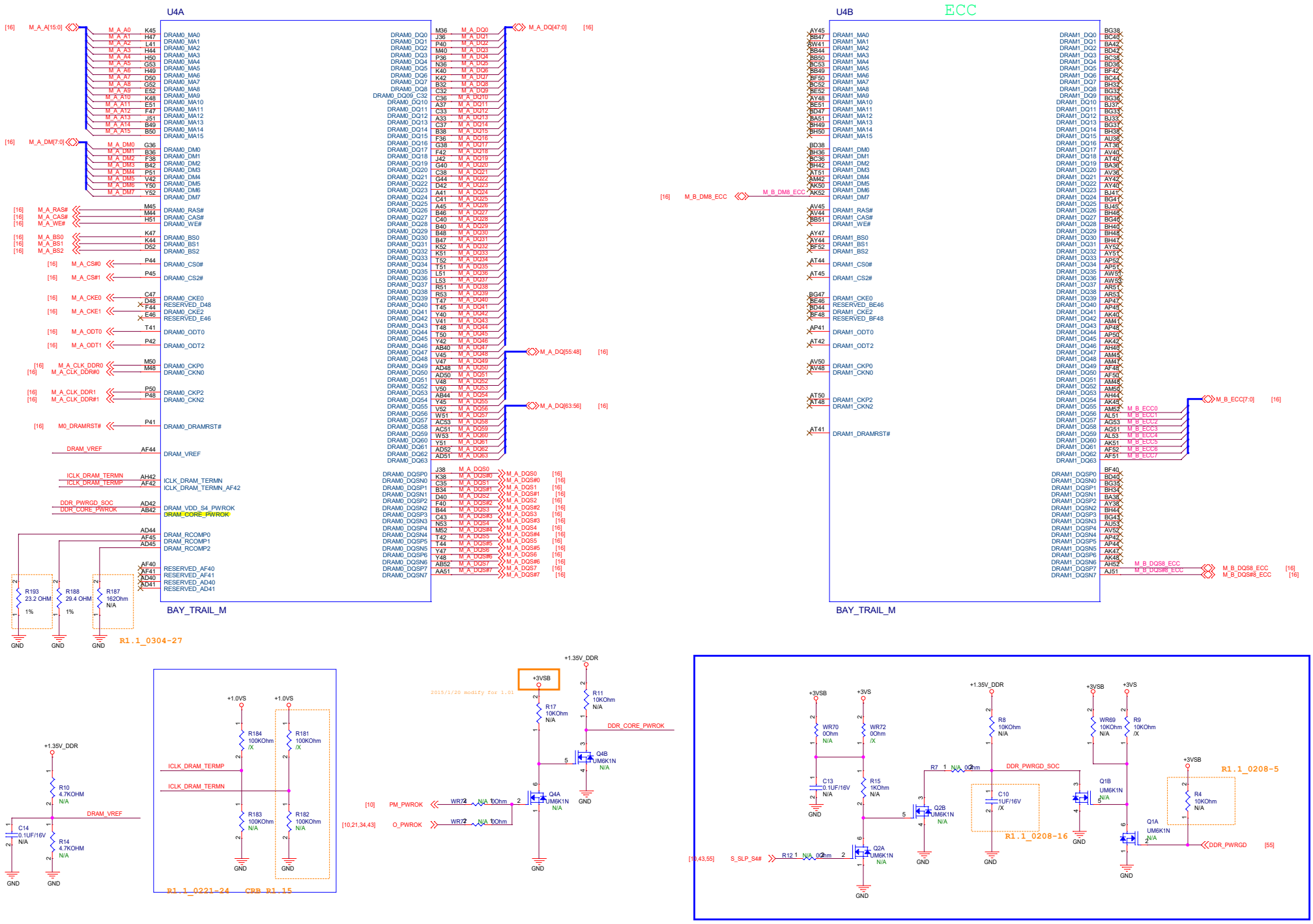
ASUSTeK COMPUTER INC.

Title : SYSTEM SETTING

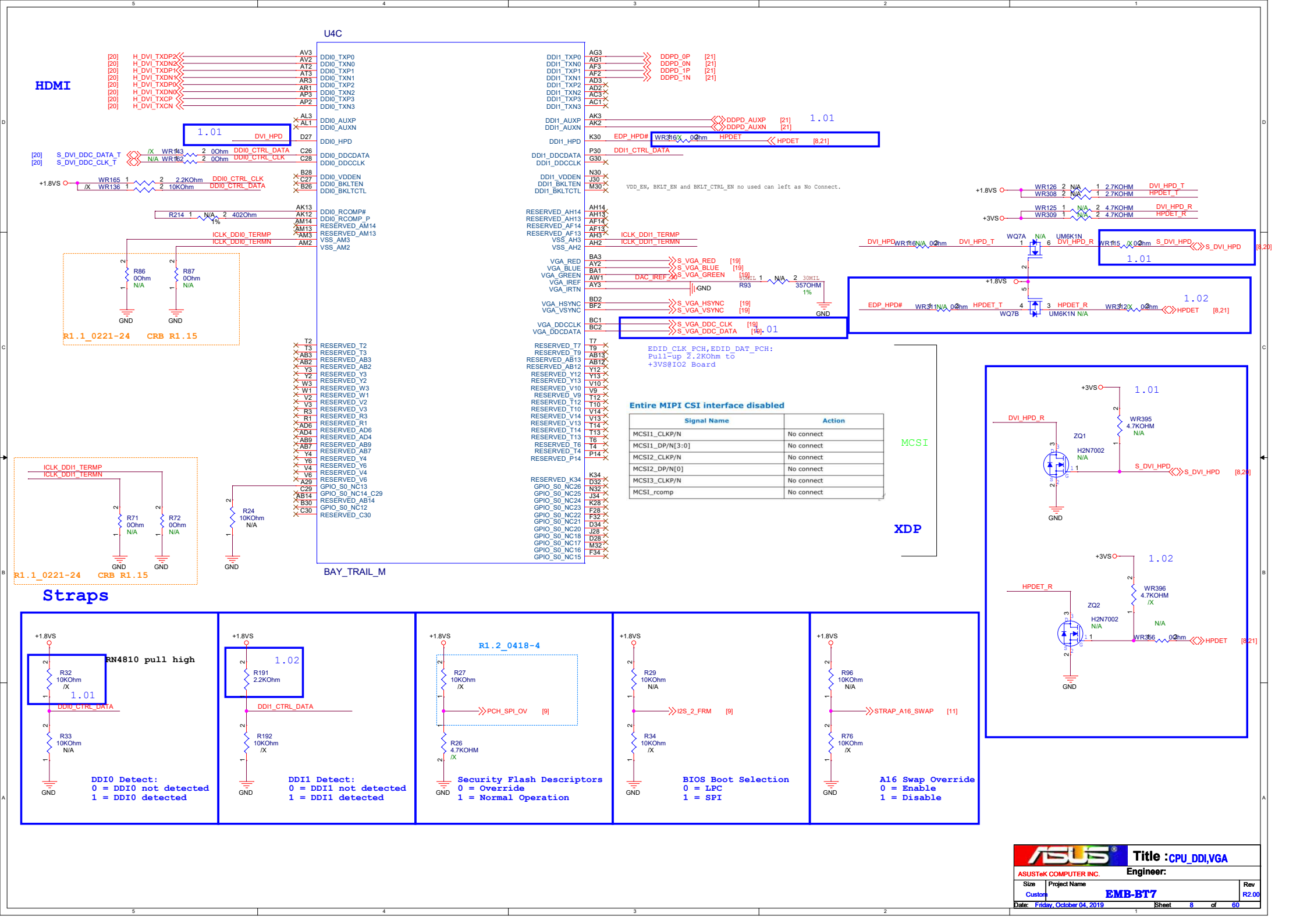
Engineer:

Size	Project Name	Rev
C	EMB-BT7	R2.00

Date: Friday, October 04, 2019 Sheet 6 of 60



ASUSTeK COMPUTER INC.	Title : CPU_DDR3		
	Engineer:		
Size: C	Project Name: EMB-BT7		Rev: R2.00
Date: Friday, October 04, 2019	Sheet 7 of 60		


HDMI
U4C
BAY_TRAIL_M
DDI0_TXP0
DDI0_TXN0
DDI0_TXP1
DDI0_TXN1
DDI0_TXP2
DDI0_TXN2
DDI0_TXP3
DDI0_TXN3
DDI0_AUXP
DDI0_AUXN
DDI0_HPD
DDI0_DDCDATA
DDI0_DDCCLK
DDI0_VDDEN
DDI0_BKLTEN
DDI0_BKLTCTL
DDI0_RCOMP#
DDI0_RCOMP_P
RESERVED_AM14
RESERVED_AM13
VSS_AM3
VSS_AM2
DDI1_TXP0
DDI1_TXN0
DDI1_TXP1
DDI1_TXN1
DDI1_TXP2
DDI1_TXN2
DDI1_TXP3
DDI1_TXN3
DDI1_AUXP
DDI1_AUXN
DDI1_HPD
DDI1_DDCDATA
DDI1_DDCCLK
DDI1_VDDEN
DDI1_BKLTEN
DDI1_BKLTCTL
VDD_EN, BKLT_EN and BKLT_CTRL_EN no used can left as No Connect.
RESERVED_AH14
RESERVED_AH13
RESERVED_AF14
RESERVED_AF13
RESERVED_AF13
VSS_AH3
VSS_AH2
VGA_RED
VGA_BLUE
VGA_GREEN
VGA_IREF
VGA_IRTN
VGA_HSYNC
VGA_VSYNC
VGA_DDCCLK
VGA_DDCDATA
RESERVED_T2
RESERVED_T3
RESERVED_AB3
RESERVED_AB2
RESERVED_Y3
RESERVED_Y2
RESERVED_W3
RESERVED_W1
RESERVED_V2
RESERVED_V3
RESERVED_R3
RESERVED_R1
RESERVED_AD6
RESERVED_AD4
RESERVED_AB9
RESERVED_AB7
RESERVED_Y4
RESERVED_Y6
RESERVED_V4
RESERVED_V6
GPIO_S0_NC13
GPIO_S0_NC14_C29
RESERVED_AB14
GPIO_S0_NC12
RESERVED_C30
RESERVED_T7
RESERVED_T9
RESERVED_AB13
RESERVED_AB12
RESERVED_Y12
RESERVED_Y13
RESERVED_V10
RESERVED_V9
RESERVED_T12
RESERVED_T10
RESERVED_V14
RESERVED_V13
RESERVED_T14
RESERVED_T13
RESERVED_T6
RESERVED_T4
RESERVED_P14
RESERVED_K34
GPIO_S0_NC26
GPIO_S0_NC25
GPIO_S0_NC24
GPIO_S0_NC23
GPIO_S0_NC22
GPIO_S0_NC21
GPIO_S0_NC20
GPIO_S0_NC18
GPIO_S0_NC17
GPIO_S0_NC16
GPIO_S0_NC15
EDID_CLK_PCH,EDID_DAT_PCH:
Pull-up 2.2KOhm to
+3VS@IO2 Board
Entire MIPI CSI interface disabled
Signal Name
Action
MCSI1_CLKP/N
No connect
MCSI1_DP/N[3:0]
No connect
MCSI2_CLKP/N
No connect
MCSI2_DP/N[0]
No connect
MCSI3_CLKP/N
No connect
MCSI_rcomp
No connect
MCSI
XDP
R1.1_0221-24 CRB R1.15
Straps
RN4810 pull high
DDI0 Detect:
0 = DDI0 not detected
1 = DDI0 detected
DDI1 Detect:
0 = DDI1 not detected
1 = DDI1 detected
R1.2_0418-4
Security Flash Descriptors
0 = Override
1 = Normal Operation
BIOS Boot Selection
0 = LPC
1 = SPI
A16 Swap Override
0 = Enable
1 = Disable
Title :CPU_DDI,VGA
ASUSTeK COMPUTER INC.
Engineer:
Size
Project Name
EMB-BT7
Rev
R2.00
Date: Friday, October 04, 2019
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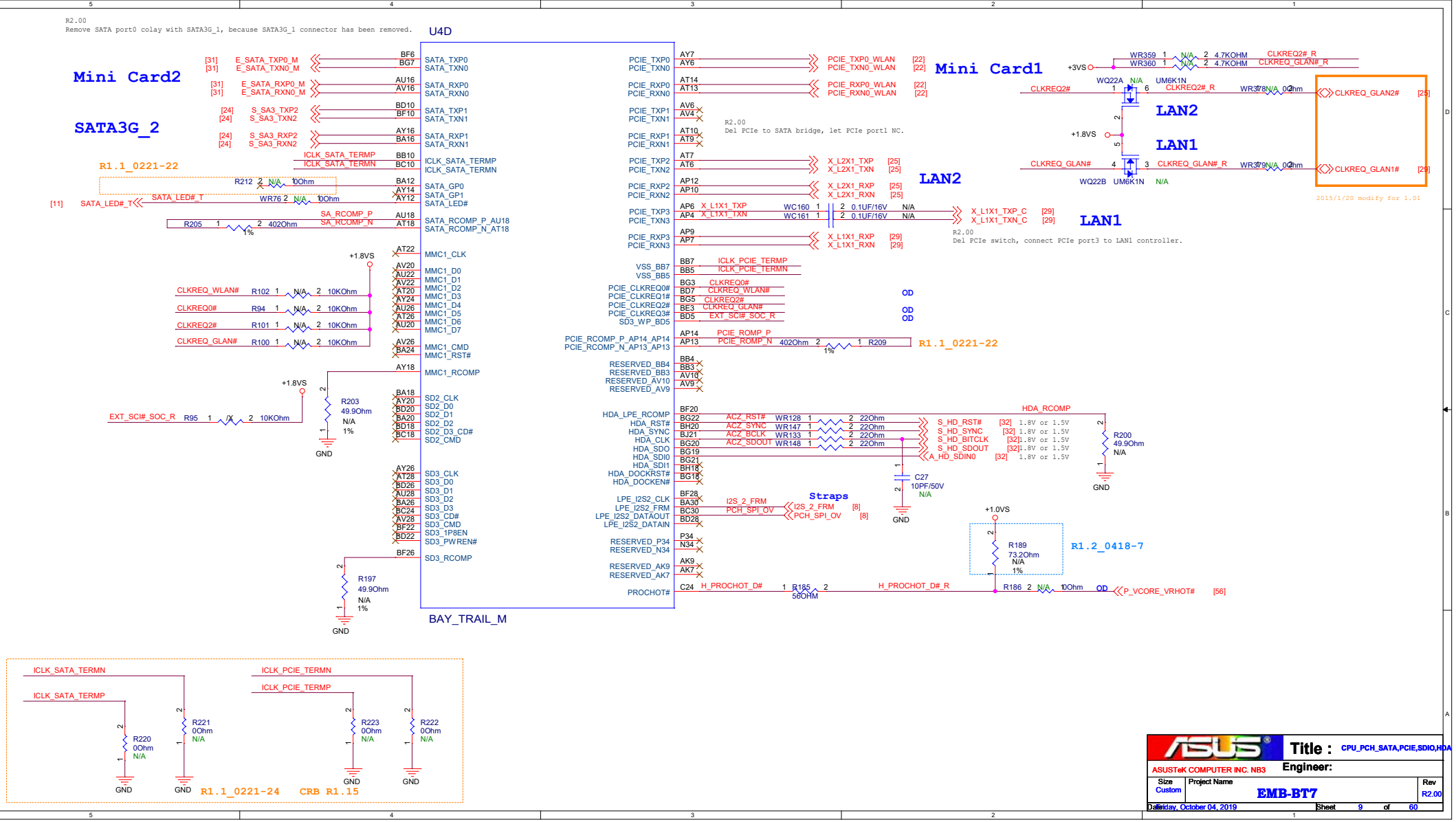
R2.00
Remove SATA port0 colay with SATA3G_1, because SATA3G_1 connector has been removed.
U4D
Mini Card2
SATA3G_2
R1.1_0221-22
SATA_LED#_T
SATA_LED#
SA_RCOMP_P
SA_RCOMP_N
R205 1 2 402Ohm 1%
+1.8VS
CLKREQ_WLAN# R102 10KOhm
CLKREQ0# R94 10KOhm
CLKREQ2# R101 10KOhm
CLKREQ_GLAN# R100 10KOhm
EXT_SCI#_SOC_R R95 10KOhm
R203 49.9Ohm N/A 1%
R197 49.9Ohm N/A 1%
GND
SATA_TXP0
SATA_TXN0
SATA_RXP0
SATA_RXN0
SATA_TXP1
SATA_TXN1
SATA_RXP1
SATA_RXN1
ICLK_SATA_TERMP
ICLK_SATA_TERMN
SATA_GP0
SATA_GP1
SATA_LED#
SATA_RCOMP_P_AU18
SATA_RCOMP_N_AT18
MMC1_CLK
MMC1_D0
MMC1_D1
MMC1_D2
MMC1_D3
MMC1_D4
MMC1_D5
MMC1_D6
MMC1_D7
MMC1_CMD
MMC1_RST#
MMC1_RCOMP
SD2_CLK
SD2_D0
SD2_D1
SD2_D2
SD2_D3_CD#
SD2_CMD
SD3_CLK
SD3_D0
SD3_D1
SD3_D2
SD3_D3
SD3_CD#
SD3_CMD
SD3_1P8EN
SD3_PWREN#
SD3_RCOMP
BAY_TRAIL_M
PCIE_TXP0
PCIE_TXN0
PCIE_RXP0
PCIE_RXN0
PCIE_TXP1
PCIE_TXN1
PCIE_RXP1
PCIE_RXN1
PCIE_TXP2
PCIE_TXN2
PCIE_RXP2
PCIE_RXN2
PCIE_TXP3
PCIE_TXN3
PCIE_RXP3
PCIE_RXN3
VSS_BB7
VSS_BB5
PCIE_CLKREQ0#
PCIE_CLKREQ1#
PCIE_CLKREQ2#
PCIE_CLKREQ3#
SD3_WP_BD5
PCIE_RCOMP_P_AP14_AP14
PCIE_RCOMP_N_AP13_AP13
RESERVED_BB4
RESERVED_BB3
RESERVED_AV10
RESERVED_AV9
HDA_LPE_RCOMP
HDA_RST#
HDA_SYNC
HDA_CLK
HDA_SDO
HDA_SDI0
HDA_SDI1
HDA_DOCKRST#
HDA_DOCKEN#
LPE_I2S2_CLK
LPE_I2S2_FRM
LPE_I2S2_DATAOUT
LPE_I2S2_DATAIN
RESERVED_P34
RESERVED_N34
RESERVED_AK9
RESERVED_AK7
PROCHOT#
PCIE_TXP0_WLAN [22]
PCIE_TXN0_WLAN [22]
PCIE_RXP0_WLAN [22]
PCIE_RXN0_WLAN [22]
R2.00
Del PCIe to SATA bridge, let PCIe port1 NC.
X_L2X1_TXP [25]
X_L2X1_TXN [25]
X_L2X1_RXP [25]
X_L2X1_RXN [25]
LAN2
X_L1X1_TXP
X_L1X1_TXN
WC160 0.1UF/16V
WC161 0.1UF/16V
X_L1X1_TXP_C [29]
X_L1X1_TXN_C [29]
LAN1
X_L1X1_RXP [29]
X_L1X1_RXN [29]
R2.00
Del PCIe switch, connect PCIe port3 to LAN1 controller.
ICLK_PCIE_TERMP
ICLK_PCIE_TERMN
CLKREQ0#
CLKREQ_WLAN#
CLKREQ2#
CLKREQ_GLAN#
EXT_SCI#_SOC_R
OD
PCIE_RCOMP_P
PCIE_RCOMP_N
402Ohm 1% R209
R1.1_0221-22
HDA_RCOMP
ACZ_RST# WR128 22Ohm
ACZ_SYNC WR147 22Ohm
ACZ_BCLK WR133 22Ohm
ACZ_SDOUT WR148 22Ohm
S_HD_RST# [32] 1.8V or 1.5V
S_HD_SYNC [32] 1.8V or 1.5V
S_HD_BITCLK [32] 1.8V or 1.5V
S_HD_SDOUT [32] 1.8V or 1.5V
A_HD_SDIN0 [32] 1.8V or 1.5V
R200 49.9Ohm N/A
C27 10PF/50V N/A
Straps
I2S_2_FRM
PCH_SPI_OV
I2S_2_FRM [8]
PCH_SPI_OV [8]
+1.0VS
R189 73.2Ohm N/A 1%
R1.2_0418-7
C24 H_PROCHOT_D#
R185 56OHM
H_PROCHOT_D#_R
R186 10Ohm OD
P_VCORE_VRHOT# [56]
Mini Card1
+3VS
WR359 4.7KOHM CLKREQ2#_R
WR360 4.7KOHM CLKREQ_GLAN#_R
WQ22A UM6K1N
WQ22B UM6K1N
LAN2
LAN1
CLKREQ_GLAN2# [25]
CLKREQ_GLAN1# [29]
2015/1/20 modify for 1.01
ICLK_SATA_TERMN
ICLK_SATA_TERMP
ICLK_PCIE_TERMN
ICLK_PCIE_TERMP
R220 0Ohm N/A
R221 0Ohm N/A
R223 0Ohm N/A
R222 0Ohm N/A
R1.1_0221-24
CRB R1.15
Title : CPU_PCH_SATA,PCIE,SDIO,HDA
ASUSTeK COMPUTER INC. NB3
Engineer:
Size Custom
Project Name EMB-BT7
Rev R2.00
Date: Friday, October 04, 2019
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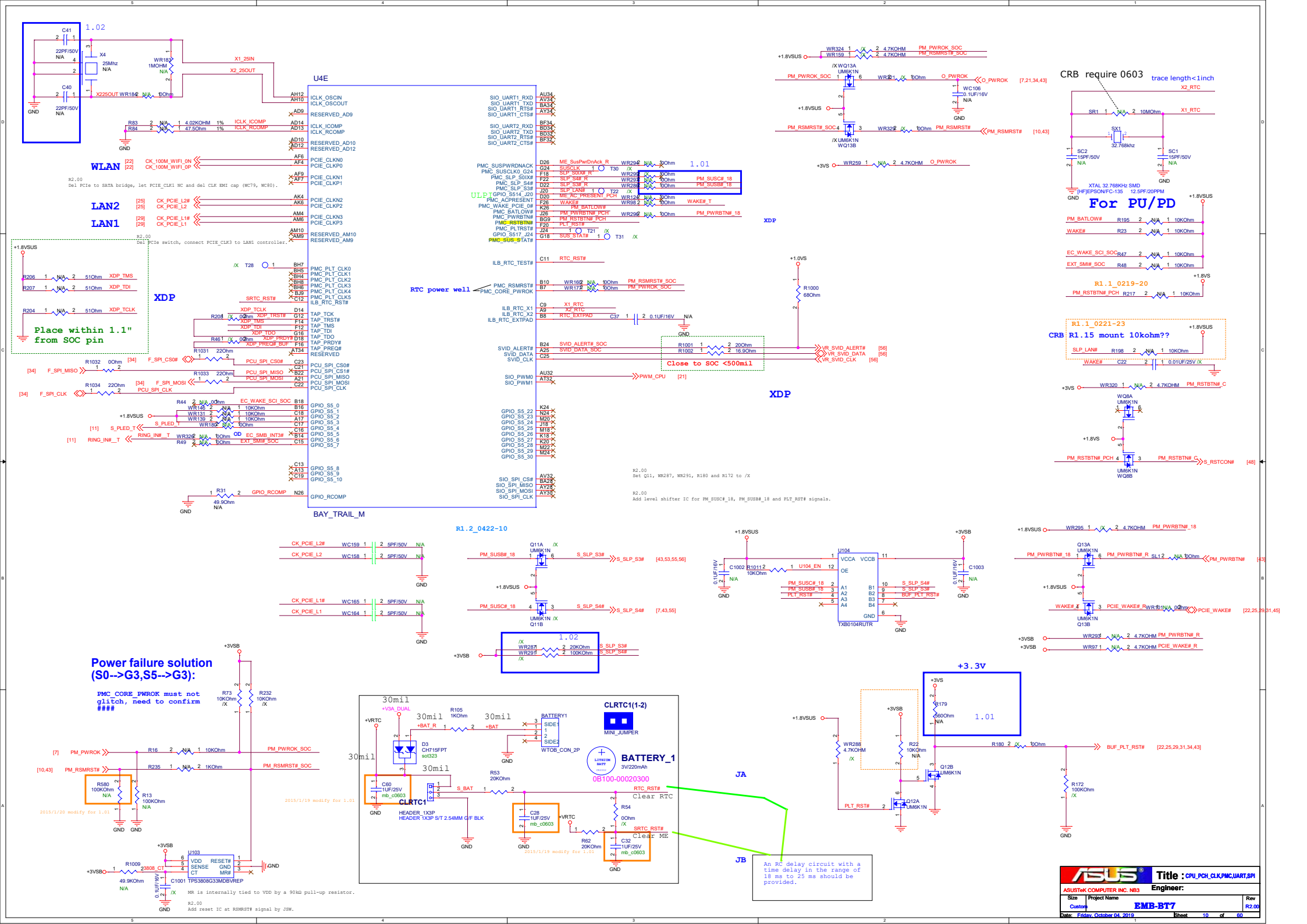
U4E
BAY_TRAIL_M
WLAN
LAN2
LAN1
XDP
RTC power well
ULPT
Place within 1.1" from SOC pin
Close to SOC <500mil
For PU/PD
CRB require 0603
trace length<1inch
CRB R1.15 mount 10kohm??
R1.2_0422-10
Power failure solution (S0-->G3,S5-->G3):
PMC_CORE_PWROK must not glitch, need to confirm ####
CLRTC1(1-2)
BATTERY_1
0B100-00020300
Clear RTC
Clear ME
+3.3V
JA
JB
An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided.
Title : CPU_PCH_CLK,PMC,UART,SPI
ASUSTeK COMPUTER INC. NB3
Engineer:
EMB-BT7
Friday, October 04, 2019

U4F

BAY_TRAIL_M

ULPI for BAYTRIAL_I

If the USB ULPI interface is unused, the pins may be left unconnected.
Refer to PDG Rev3.0

USB_4
USB3_1
USB_23
USB_23

USB3.0 for BAYTRIAL_I

USB3.0

R2.00
USB port0 connect to USB_4 connector, because USB_Hub IC has been removed.

R2.00
USB port2 connect to USB_23 connector, because MINI CARD2 don't need USB interface by JSW confirmed.

R2.00
USB port3 connect to USB_23 connector, because USB_Hub IC has been removed.

USB port 2 / USB port3
USB port 1 / USB3.0

R2.00
Remove HSIC interface, because USB_Hub IC has been removed.

No connect. Tri-State will occur.
The RCOMP should always pull down to GND with 45.3 ohm ±1%.
USB_HSIC_V1P24_G3(VCCPADSUS_1P20) can be connected to V1P0A when the USB_HSIC disabled/not used.

R2.00
Remove ENRS232_T, ENRS422_T and ENRS485__T, because COM1 has been removed.

R2.00
Remove TPM funcion, del PM_CLKRUN# connect to TPM

R2.00
Remove R55 and connect LPC_CLK1 to DEBUG1, because clock buffer has been removed.

R2.00
Connect LPC_CLK0 to SIO, because clock buffer has been removed.

Straps

R1.1_0221-24 CRB R1.15

1.01

TO DIMM, ClickPad

TO XDP

PCB ID

R1.1_0208-19
R1.2_0422-9

+1.8VS or +1.8VSUS??

no need VSS sense?

U4G

10MIL
10MIL
10MIL

[56] CPU_VCC_SENSE
[56] GFX_VCC_SENSE
[56] CPU_VSS_SENSE
[56] GFX_VSS_SENSE

CPU_VCC_SENSE
GFX_VCC_SENSE
CPU_VSS_SENSE

WR290 1 2 0Ohm

+1.35V_DDRCLK

+1.35V_DDR

+VCORE

+VGFX_CORE

AD24 power or GND?

P28	CORE_VCC_SENSE_P28	
BB8	UNCORE_VNN_SENSE	
N28	CORE_VSS_SENSE_N28	
AD38	DRAM_VDD_S4_AD38	
AF38	DRAM_VDD_S4_AF38	
A48	DRAM_VDD_S4	
AK38	DRAM_VDD_S4_AK38	
AM38	DRAM_VDD_S4_AM38	
AV41	DRAM_VDD_S4_AV41	
AV42	DRAM_VDD_S4_AV42	
BB46	DRAM_VDD_S4_BB46	
AA27	CORE_VCC_S0IX_AA27	
AA29	CORE_VCC_S0IX_AA29	
AA30	CORE_VCC_S0IX_AA30	
AC27	CORE_VCC_S0IX_AC27	
AC29	CORE_VCC_S0IX_AC29	
AC30	CORE_VCC_S0IX_AC30	
AD27	CORE_VCC_S0IX_AD27	
AD29	CORE_VCC_S0IX_AD29	
AD30	CORE_VCC_S0IX_AD30	
AF27	CORE_VCC_S0IX_AF27	
AF29	CORE_VCC_S0IX_AF29	
AG27	CORE_VCC_S0IX_AG27	
AG29	CORE_VCC_S0IX_AG29	
AG30	CORE_VCC_S0IX_AG30	
P26	CORE_VCC_S0IX_P26	
P27	CORE_VCC_S0IX_P27	
U27	CORE_VCC_S0IX_U27	
U29	CORE_VCC_S0IX_U29	
V27	CORE_VCC_S0IX_V27	
V29	CORE_VCC_S0IX_V29	
V30	CORE_VCC_S0IX_V30	
Y27	CORE_VCC_S0IX_Y27	
Y29	CORE_VCC_S0IX_Y29	
Y30	CORE_VCC_S0IX_Y30	
AF30	TP_CORE_V1P05_S4	

	DRAM_VDD_S4_BD49	BD49
	DRAM_VDD_S4_BD52	BD52
	DRAM_VDD_S4_BD53	BD53
	DRAM_VDD_S4_BF44	BF44
	DRAM_VDD_S4_BG51	BG51
	DRAM_VDD_S4_BJ48	BJ48
	DRAM_VDD_S4_C51	C51
	DRAM_VDD_S4_D44	D44
	DRAM_VDD_S4_F49	F49
	DRAM_VDD_S4_F52	F52
	DRAM_VDD_S4_F53	F53
	DRAM_VDD_S4_H46	H46
	DRAM_VDD_S4_M41	M41
	DRAM_VDD_S4_M42	M42
	DRAM_VDD_S4_V38	V38
	DRAM_VDD_S4_Y38	Y38
	UNCORE_VNN_S3_AA24	AA24
	UNCORE_VNN_S3_AC22	AC22
	UNCORE_VNN_S3_AC24	AC24
	UNCORE_VNN_S3_AD22	AD22
	UNCORE_VNN_S3_AD24	AD24
	UNCORE_VNN_S3_AF22	AF22
	UNCORE_VNN_S3_AF24	AF24
	UNCORE_VNN_S3_AG22	AG22
	UNCORE_VNN_S3_AG24	AG24
	UNCORE_VNN_S3_AJ22	AJ22
	UNCORE_VNN_S3_AJ24	AJ24
	UNCORE_VNN_S3_AK22	AK22
	UNCORE_VNN_S3_AK24	AK24
	UNCORE_VNN_S3_AK25	AK25
	UNCORE_VNN_S3_AK27	AK27
	UNCORE_VNN_S3_AK29	AK29
	UNCORE_VNN_S3_AK30	AK30
	UNCORE_VNN_S3_AK32	AK32
	UNCORE_VNN_S3_AM22	AM22
AA22	TP2_CORE_VCC_S0IX	

BAY_TRAIL_M
N/A

HEATSINK1
HEATSINK_4P

+1.35V_DDR3L
+1.35V_DDRCLK
WL17 2 1 600Ohm/100Mhz N/A
C141 1UF/10V N/A
C140 0.1UF/16V N/A
+1.35V_DDR
C130 22UF/6.3V
C129 1UF/10V N/A

Close to DIMM ?

+VCORE
C6 22UF/6.3V
C9 22UF/6.3V
C153 22UF/6.3V
C148 22UF/6.3V
C154 22UF/6.3V
C1 1UF/10V N/A
C155 1UF/10V N/A

+VGFX_CORE
C150 22UF/6.3V
C156 22UF/6.3V
C12 10UF/10V c0603 N/A
C17 1UF/10V N/A
C157 1UF/10V N/A

2015/1/19 modify for 1.01

+VCORE
C1019 1UF/10V N/A
+VCORE
C1020 1UF/10V N/A
+VGFX_CORE
C1022 1UF/10V N/A
+VGFX_CORE
C1023 1UF/10V N/A

ASUSTeK COMPUTER INC.

Title : CPU_PWR

Engineer:

Size	Project Name	Rev
B	EMB-BT7	R2.00

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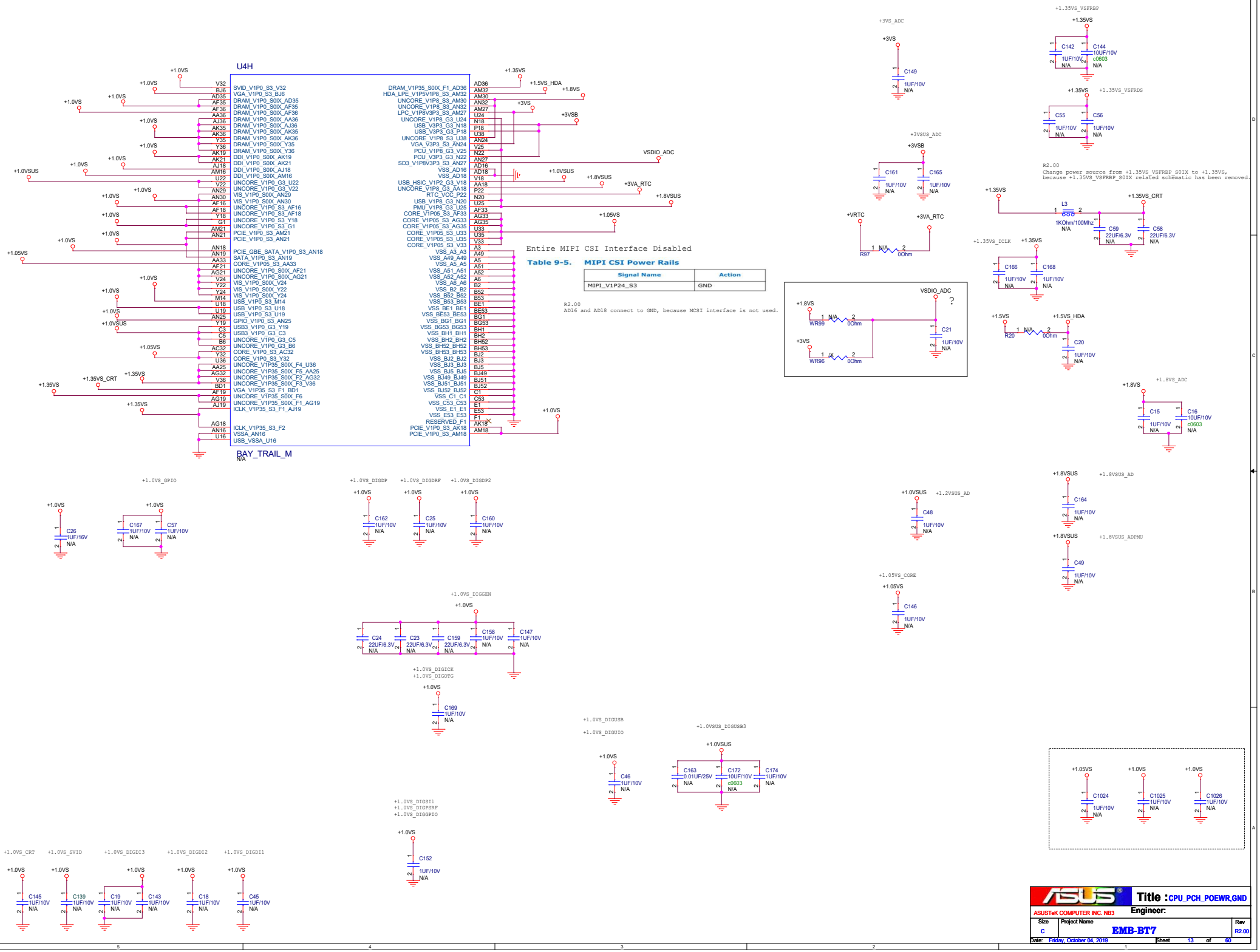
U4H
BAY_TRAIL_M
N/A
Entire MIPI CSI Interface Disabled
Table 9-5. MIPI CSI Power Rails
Signal Name
Action
MIPI_V1P24_S3
GND
R2.00
AD16 and AD18 connect to GND, because MCSI interface is not used.
R2.00
Change power source from +1.35VS_VSFRBP_S0IX to +1.35VS, because +1.35VS_VSFRBP_S0IX related schematic has been removed.
Title : CPU_PCH_POEWR,GND
ASUSTeK COMPUTER INC. NB3
Engineer:
Size C
Project Name EMB-BT7
Rev R2.00
Date: Friday, October 04, 2019
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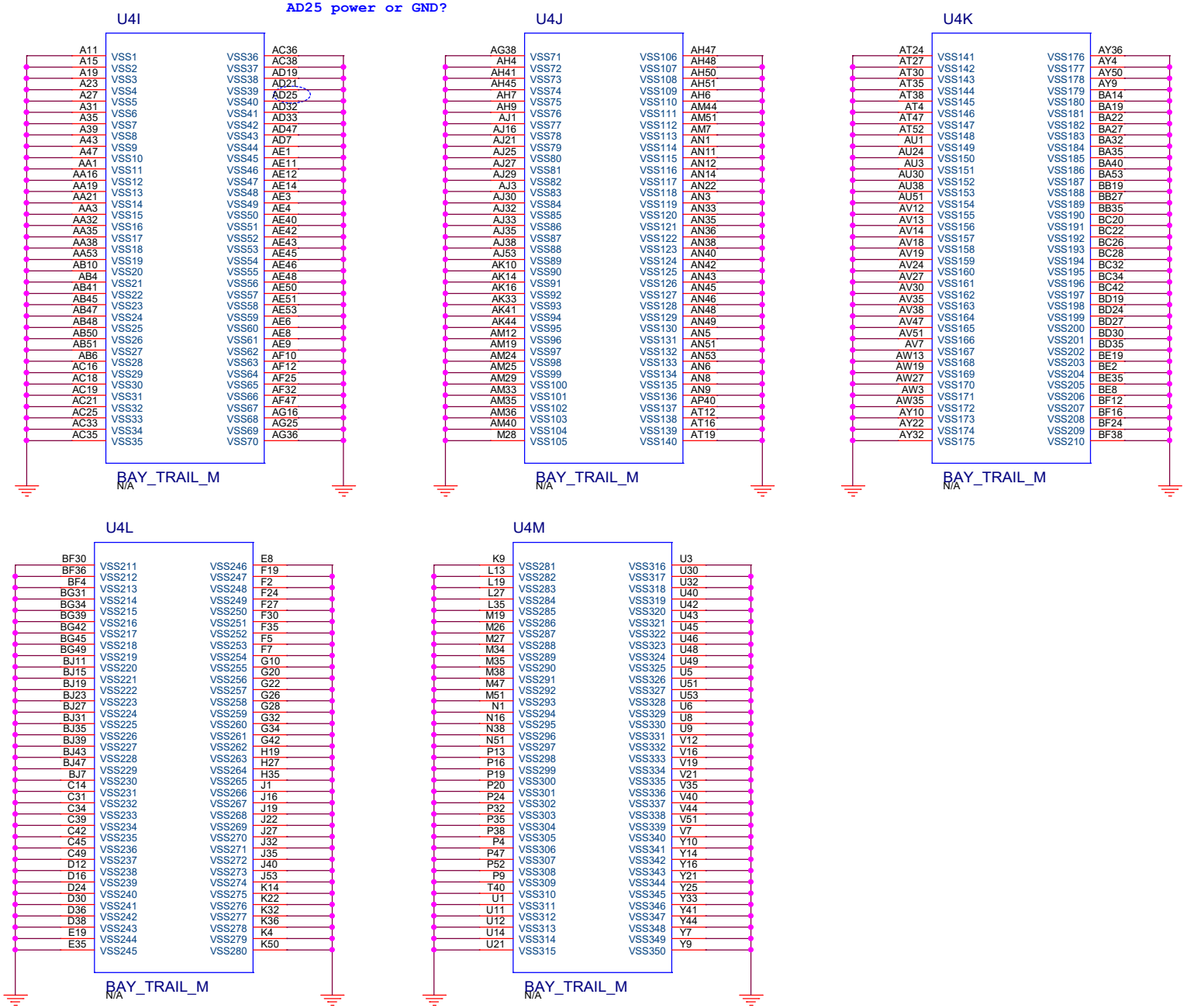
AD25 power or GND?



ASUSTeK COMPUTER INC. NB3

Title : CPU_PCH_POEWR,GND

Engineer:

Size	Project Name	Rev
B	EMB-BT7	R2.00

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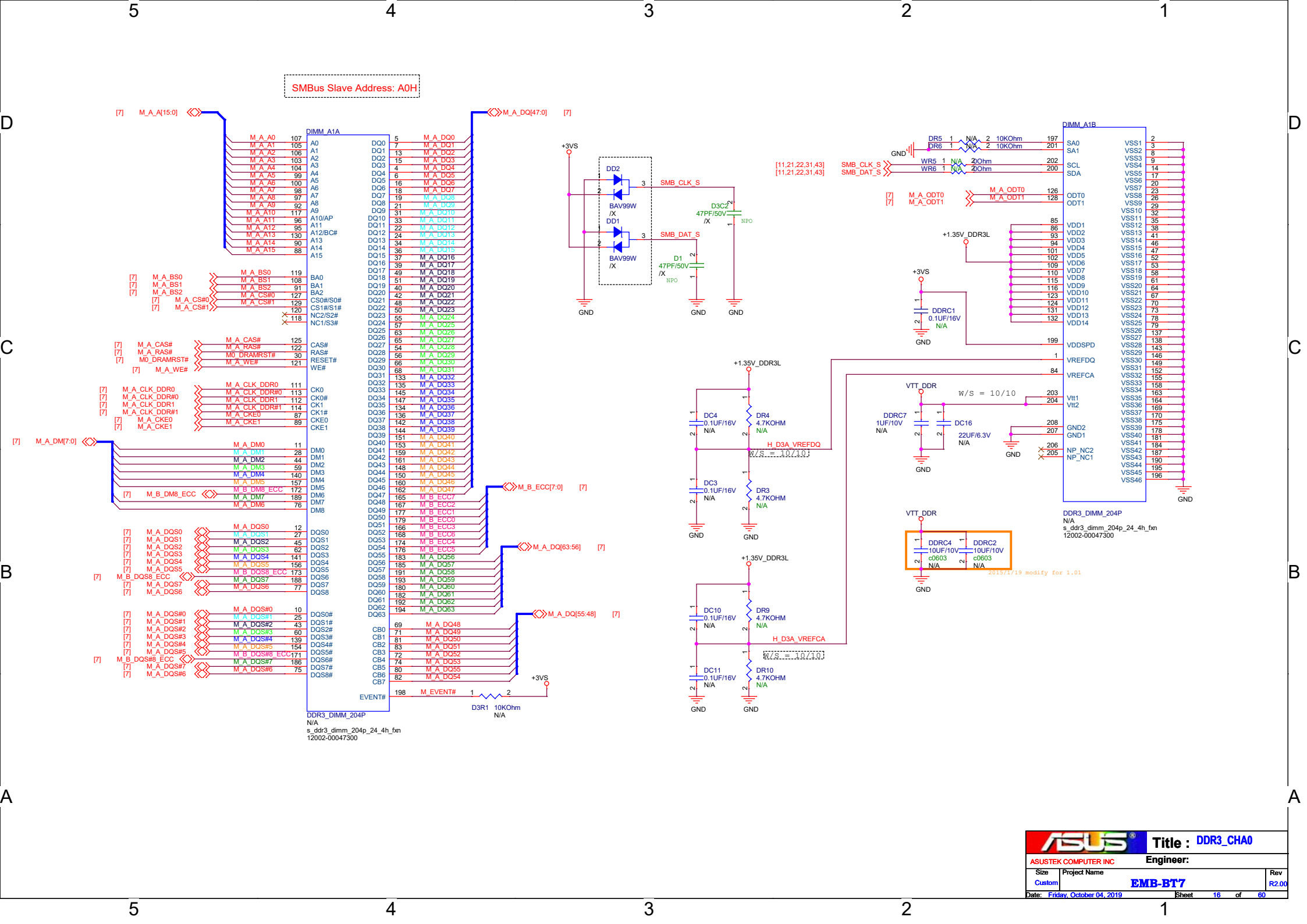
Title :	EMPTY
ASUSTeK COMPUTER INC. NB3	Engineer:
Size: Custom	Project Name: EMB-BT7
Rev: R2.00	
Date: Friday, October 04, 2019	Sheet 15 of 60


SMBus Slave Address: A0H
DIMM_A1A
DDR3_DIMM_204P
N/A
s_ddr3_dimm_204p_24_4h_fxn
12002-00047300
DIMM_A1B
DDR3_DIMM_204P
N/A
s_ddr3_dimm_204p_24_4h_fxn
12002-00047300
M_A_A[15:0]
M_A_DQ[47:0]
M_A_DM[7:0]
M_B_ECC[7:0]
M_A_DQ[63:56]
M_A_DQ[55:48]
M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
M_B_DQS8_ECC
M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7
M_B_DQS#8_ECC
M_A_BS0
M_A_BS1
M_A_BS2
M_A_CS#0
M_A_CS#1
M_A_CAS#
M_A_RAS#
M0_DRAMRST#
M_A_WE#
M_A_CLK_DDR0
M_A_CLK_DDR#0
M_A_CLK_DDR1
M_A_CLK_DDR#1
M_A_CKE0
M_A_CKE1
M_A_ODT0
M_A_ODT1
M_EVENT#
D3R1 10KOhm N/A
SMB_CLK_S
SMB_DAT_S
[11,21,22,31,43]
DD2
DD1
BAV99W /X
D3C2 47PF/50V /X NPO
D1 47PF/50V /X NPO
+3VS
GND
+1.35V_DDR3L
DDRC1 0.1UF/16V N/A
VTT_DDR
W/S = 10/10
DDRC7 1UF/10V N/A
DC16 22UF/6.3V N/A
DDRC4 10UF/10V c0603 N/A
DDRC2 10UF/10V c0603 N/A
2015/1/19 modify for 1.01
DC4 0.1UF/16V N/A
DR4 4.7KOHM N/A
DC3 0.1UF/16V N/A
DR3 4.7KOHM N/A
H_D3A_VREFDQ
DC10 0.1UF/16V N/A
DR9 4.7KOHM N/A
DC11 0.1UF/16V N/A
DR10 4.7KOHM N/A
H_D3A_VREFCA
DR5 N/A 10KOhm
DR6 N/A 10KOhm
WR5 N/A 20hm
WR6 N/A 20hm
Title : DDR3_CHA0
ASUSTEK COMPUTER INC
Engineer:
Size Custom
Project Name EMB-BT7
Rev R2.00
Date: Friday, October 04, 2019
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5 4 3 2 1

D C B A

ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
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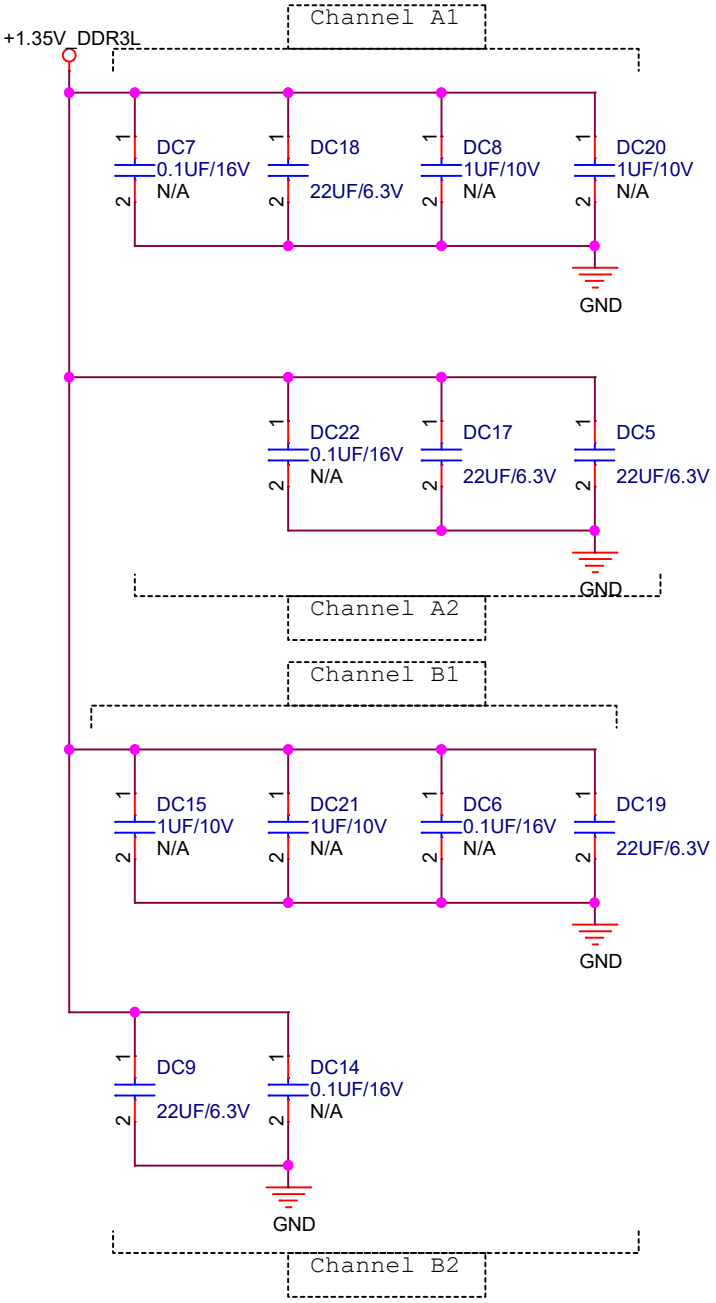
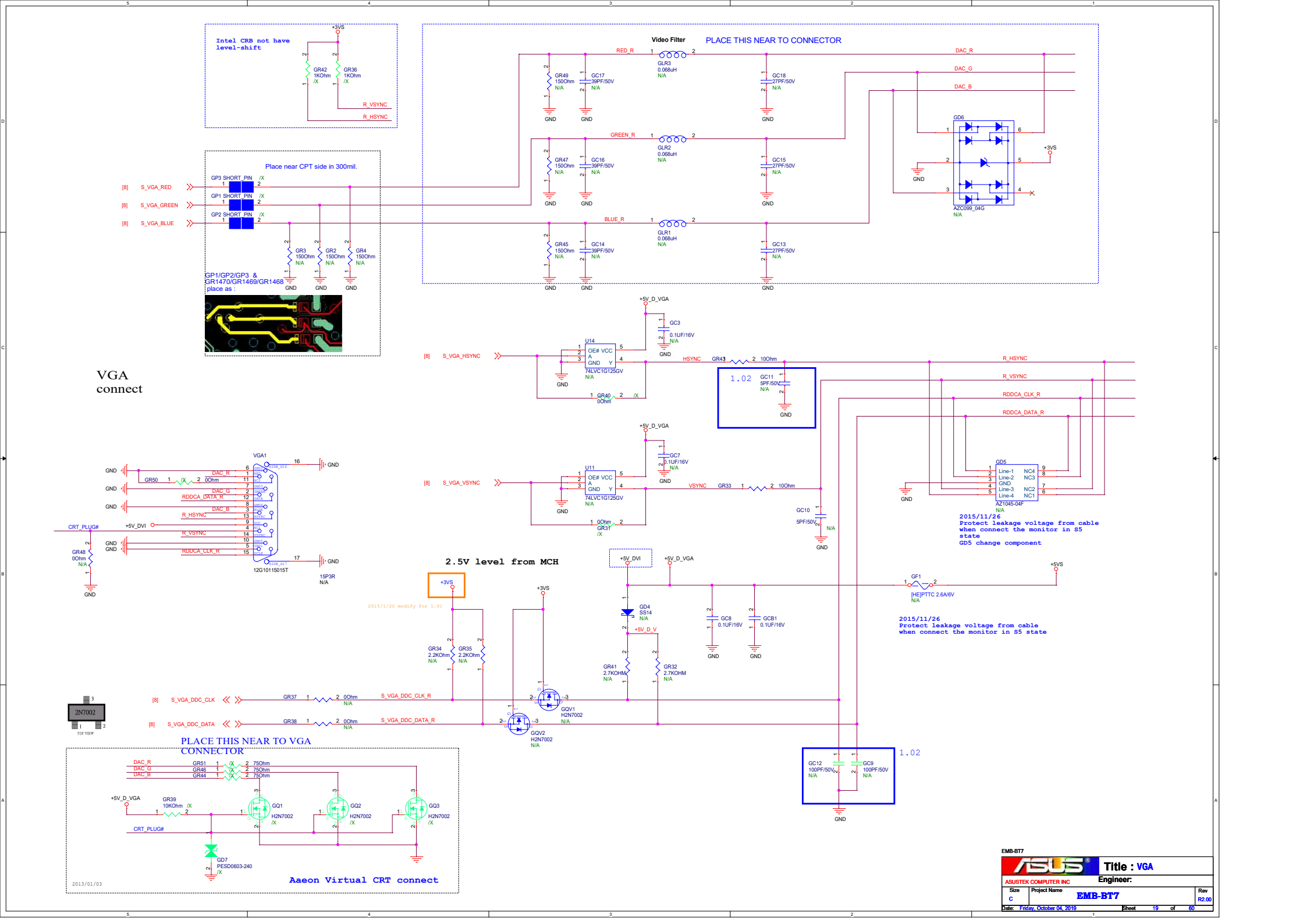
0.3B Beta



ASUSTEK COMPUTER INC	Title : DDR3_POWER	
	Engineer:	
Size: A	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 18 of 60	

VGA connect



EMB-BT7

ASUSTEK COMPUTER INC

Title : VGA

Engineer:

Size	Project Name	Rev
C	EMB-BT7	R2.00

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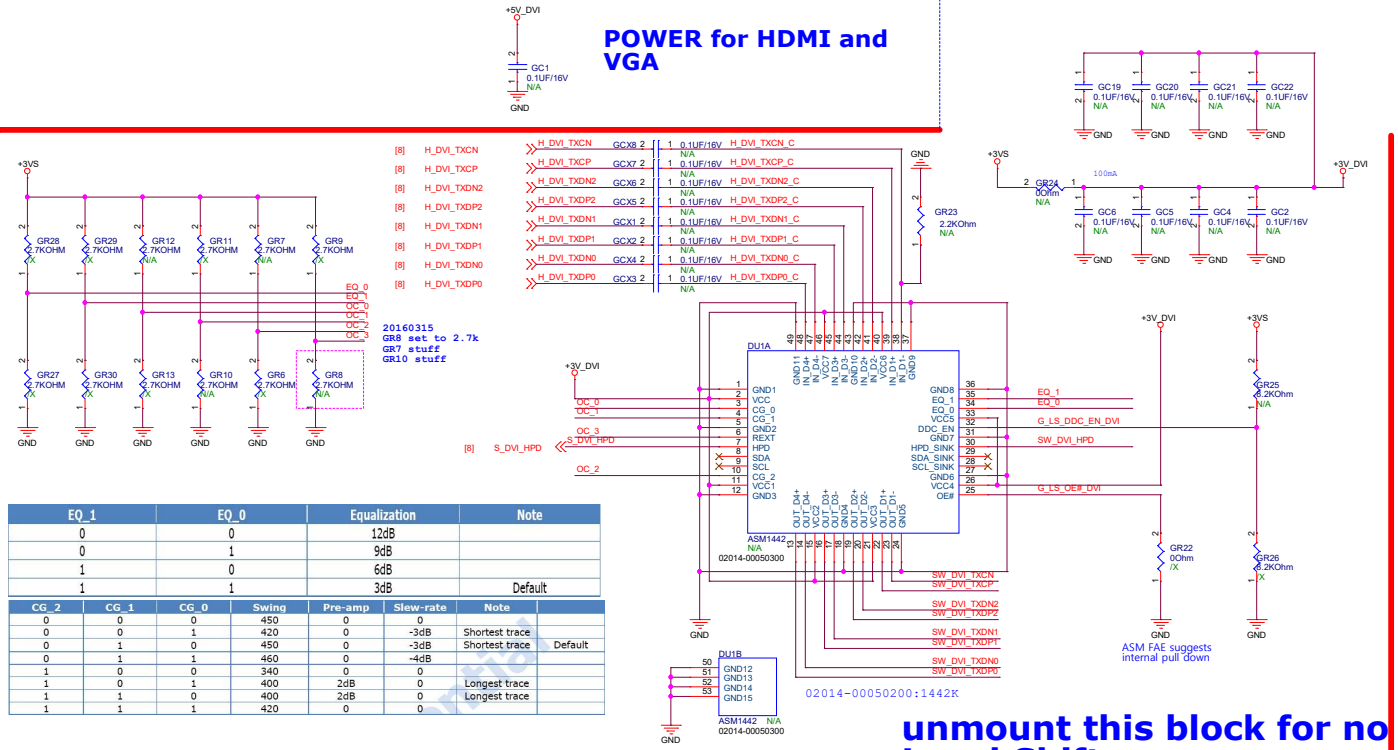
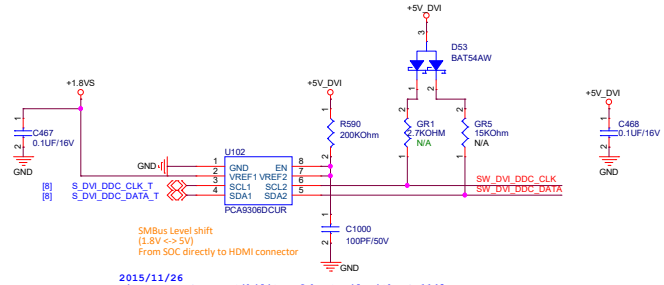
POWER for HDMI and VGA

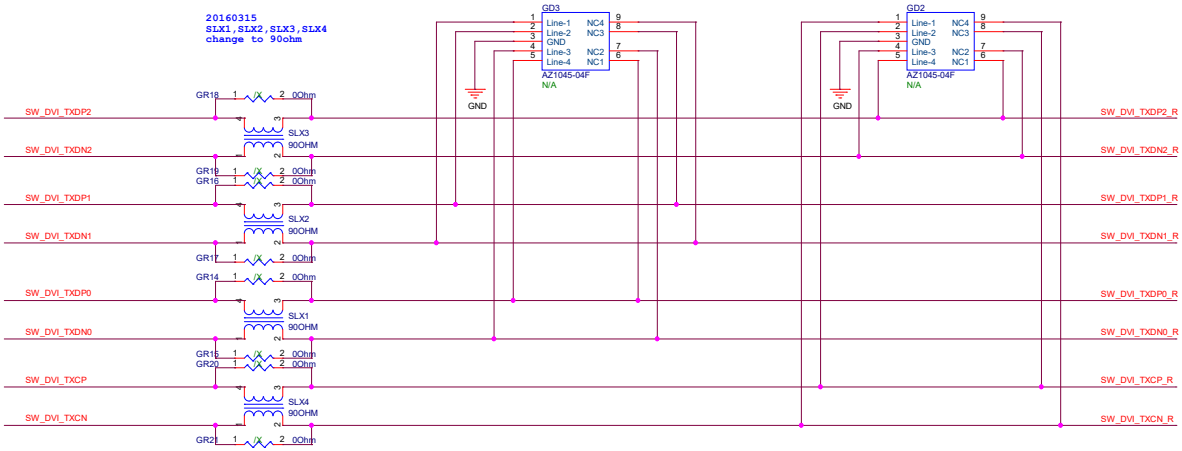


EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

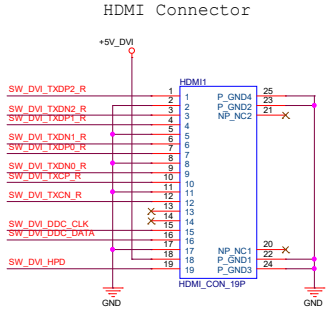
CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	0	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		



unmount this block for no Level Shifter



ESD



ASUSTEK COMPUTER INC

Title : HDMI(port A)

Engineer:

Size	Project Name	Rev
A2	EMB-BT7	R2.00

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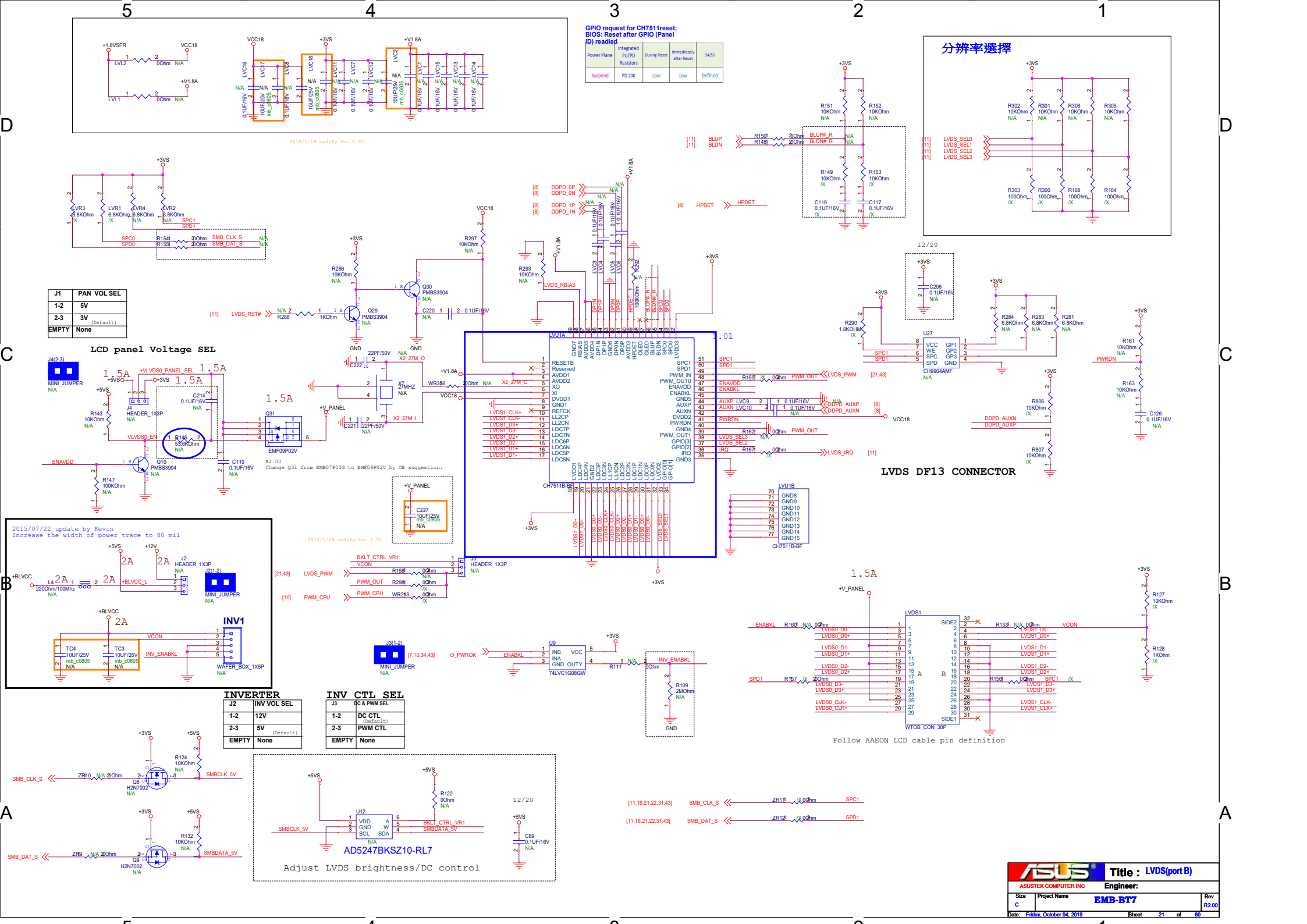
GPIO request for CH7511reset;
BIOS: Reset after GPIO (Panel ID) readied
Power Plane | Integrated PU/PD Resistors | During Reset | Immediately after Reset | S4/S5
Suspend | PD 20K | Low | Low | Defined
分辨率選擇
LCD panel Voltage SEL
J1 | PAN VOL SEL
1-2 | 5V
2-3 | 3V (Default)
EMPTY | None
LVDS DF13 CONNECTOR
INVERTER
J2 | INV VOL SEL
1-2 | 12V
2-3 | 5V (Default)
EMPTY | None
INV CTL SEL
J3 | DC & PWM SEL
1-2 | DC CTL (Default)
2-3 | PWM CTL
EMPTY | None
2015/07/22 update by Kevin
Increase the width of power trace to 80 mil
2015/1/19 modify for 1.01
R2.00
Change Q31 from EMB07P03G to EMF09P02V by CE suggestion.
Follow AAEON LCD cable pin definition
Adjust LVDS brightness/DC control
AD5247BKSZ10-RL7
Title : LVDS(port B)
ASUSTEK COMPUTER INC
Engineer:
Size C
Project Name EMB-BT7
Rev R2.00
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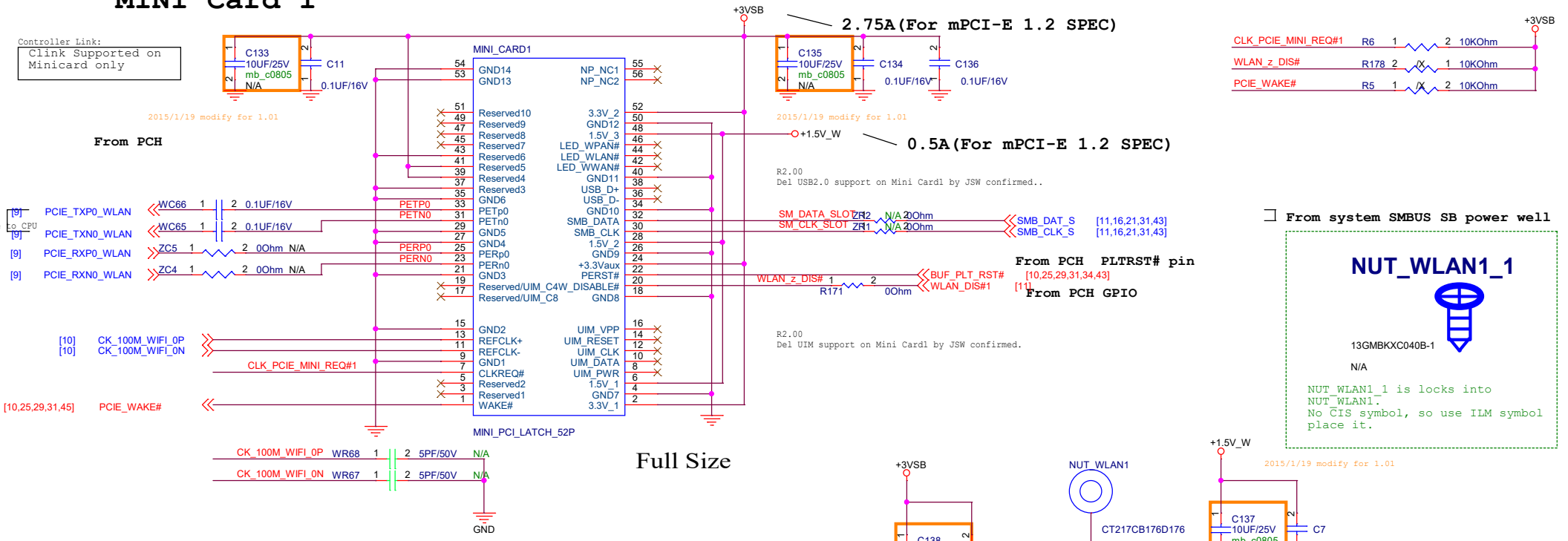
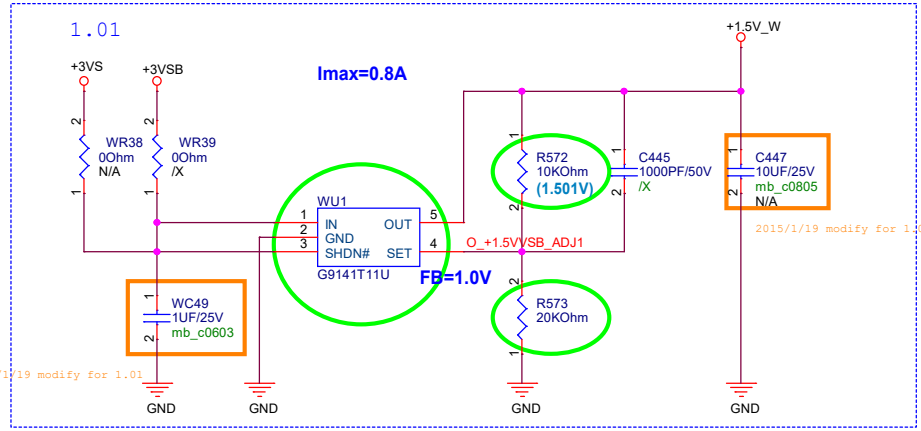
MINI Card 1



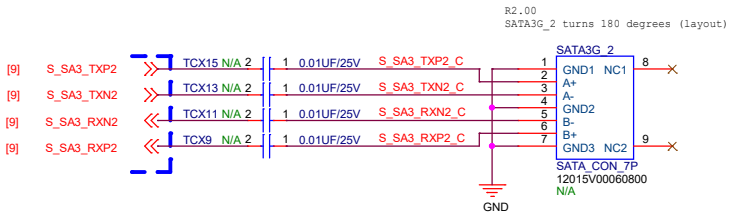
Full Size

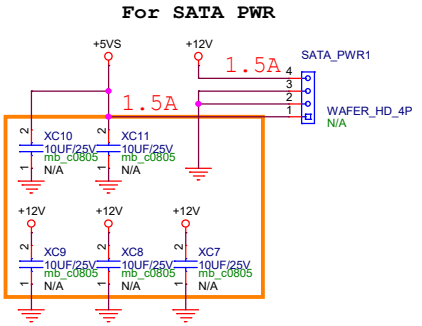


ASUSTEK COMPUTER INC	Title : Mini_Card1_PCIE		
	Engineer:		
Size: B	Project Name: EMB-BT7	Rev: R2.00	
Date: Friday, October 04, 2019	Sheet 22 of 60		

R2.00
Remove PCIe to SATA bridge
by JSW confirmed.

ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 23 of 60	





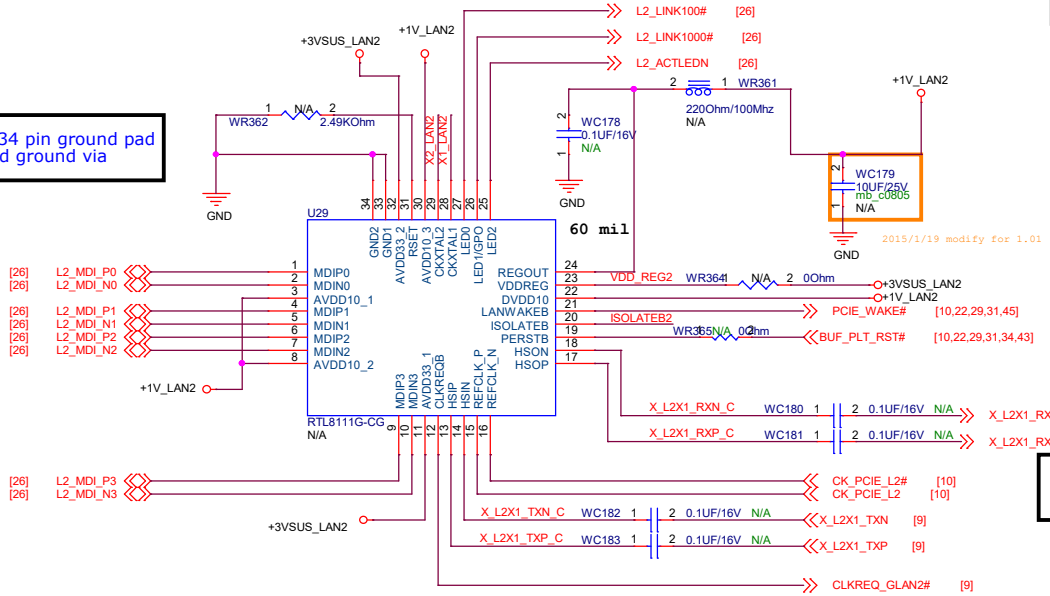
R2.00

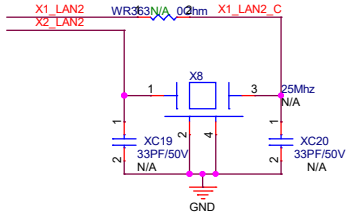
Del SATA3G_1, SATA6G_1, SATA6G_2 and 1.25V LDO of ASM1061.

ASUSTEK COMPUTER INC	Title : SATA Connector	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 24 of 60	

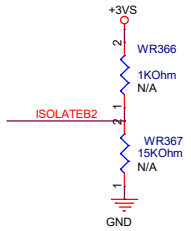
The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad need ground via



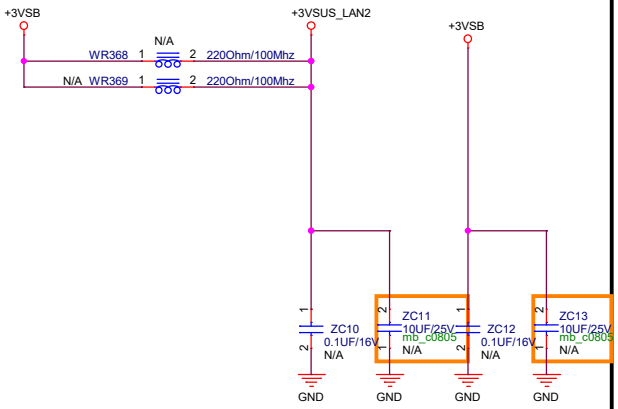


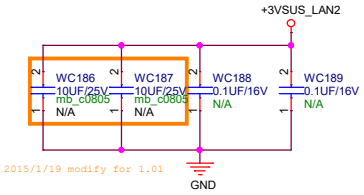
PCIE Tx,Rx方向是以南橋為觀點
chip pin Tx,Rx是以chip為觀點

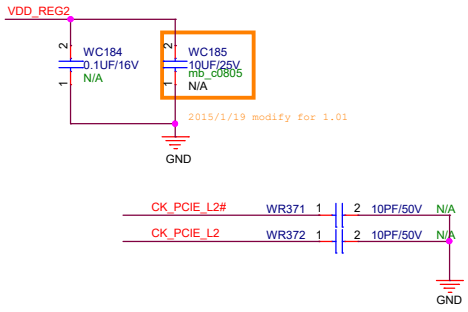


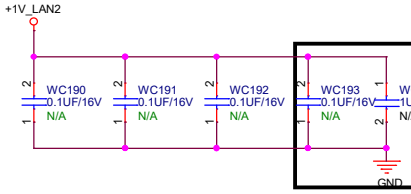
CLKREQ_GLAN#, PCIE_WAKE# should be PU on the host side

Realtek suggests 3V_LAN raise time >1ms



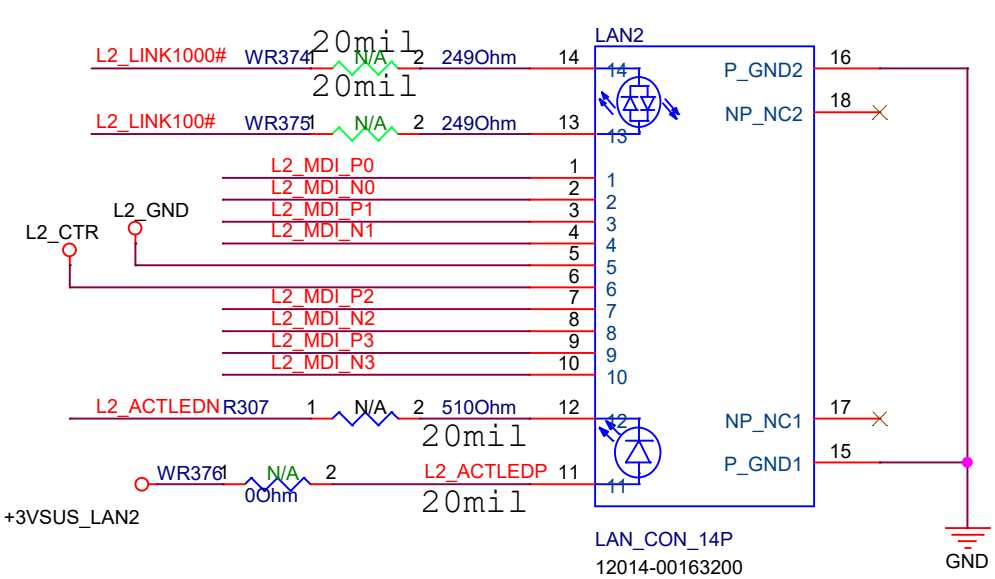


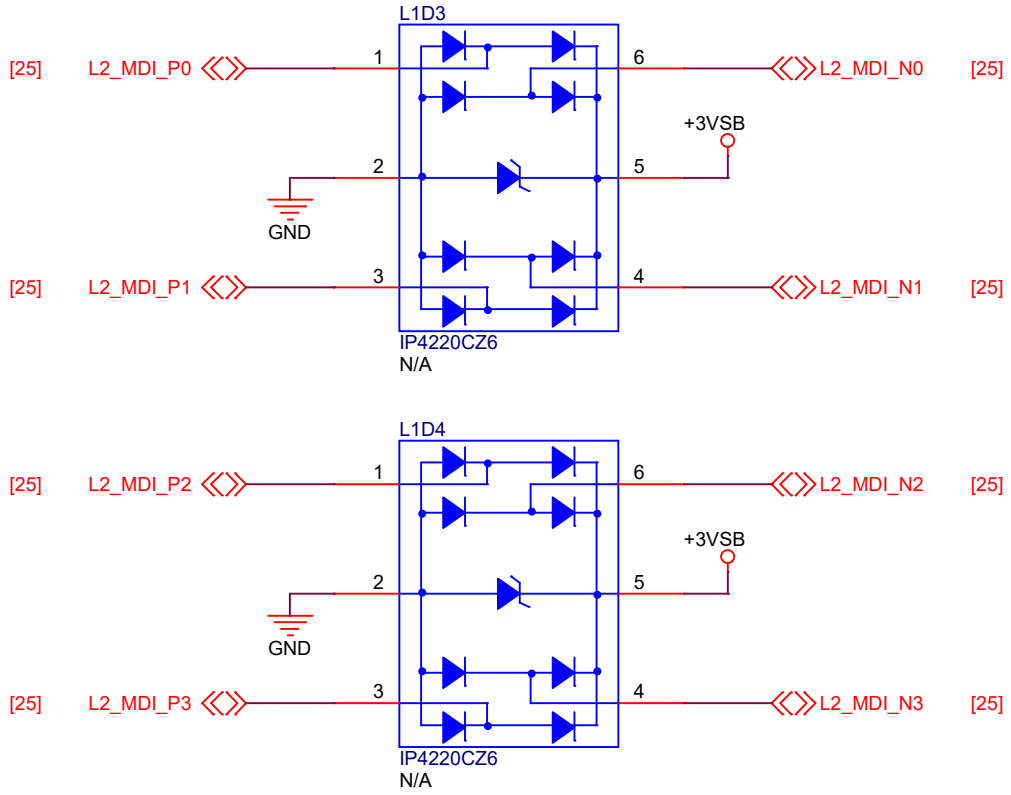


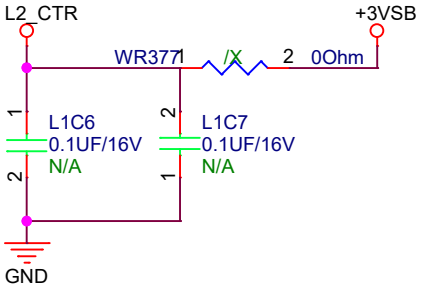


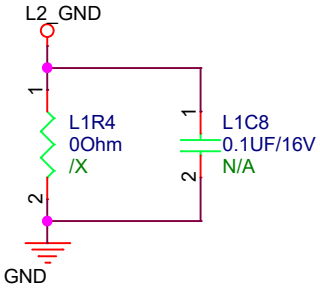
Each Cap close to each pin of IC of pin22

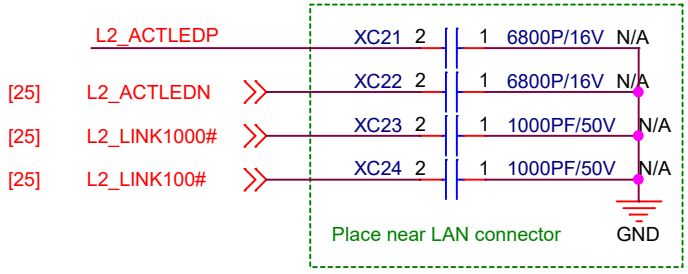
ASUSTEK COMPUTER INC	Title : LAN2_RTL8111G	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 25 of 60	











ASUSTEK COMPUTER INC	Title : LAN2_RJ45	
	Engineer:	
Size: A	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 26 of 60	

R2.00

Remove PCIe switch.

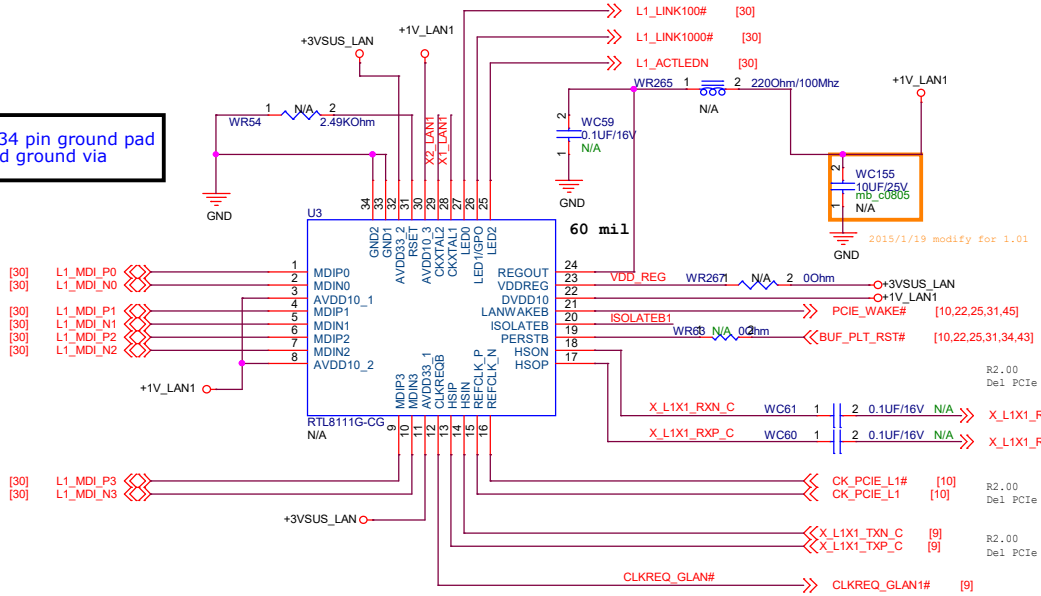
ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 27 of 60	

R2.00
Remove PCIex1 Connector.

ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 28 of 60	

The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

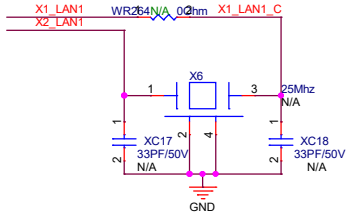
33/34 pin ground pad need ground via

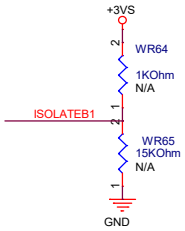


R2.00
Del PCIe switch, connect PCIe port3 to LAN1 controller

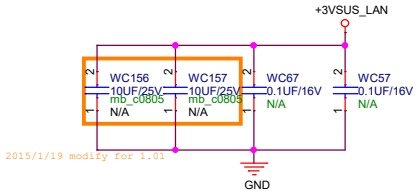
R2.00
Del PCIe switch, connect PCIE_CLK3 to LAN1 controller

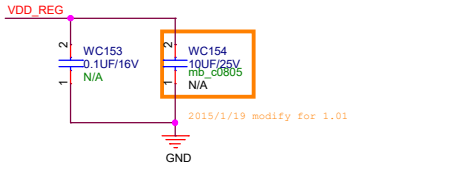
R2.00
Del PCIe switch, connect PCIe port3 to LAN1 controller

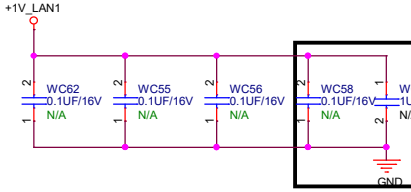




CLKREQ_GLAN#, PCIE_WAKE# should be PU on the host side

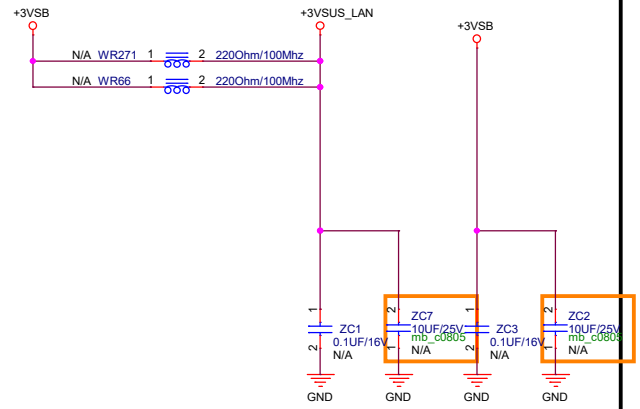






Each Cap close to each pin of IC of pin22

Realtek suggests 3V_LAN raise time >1ms



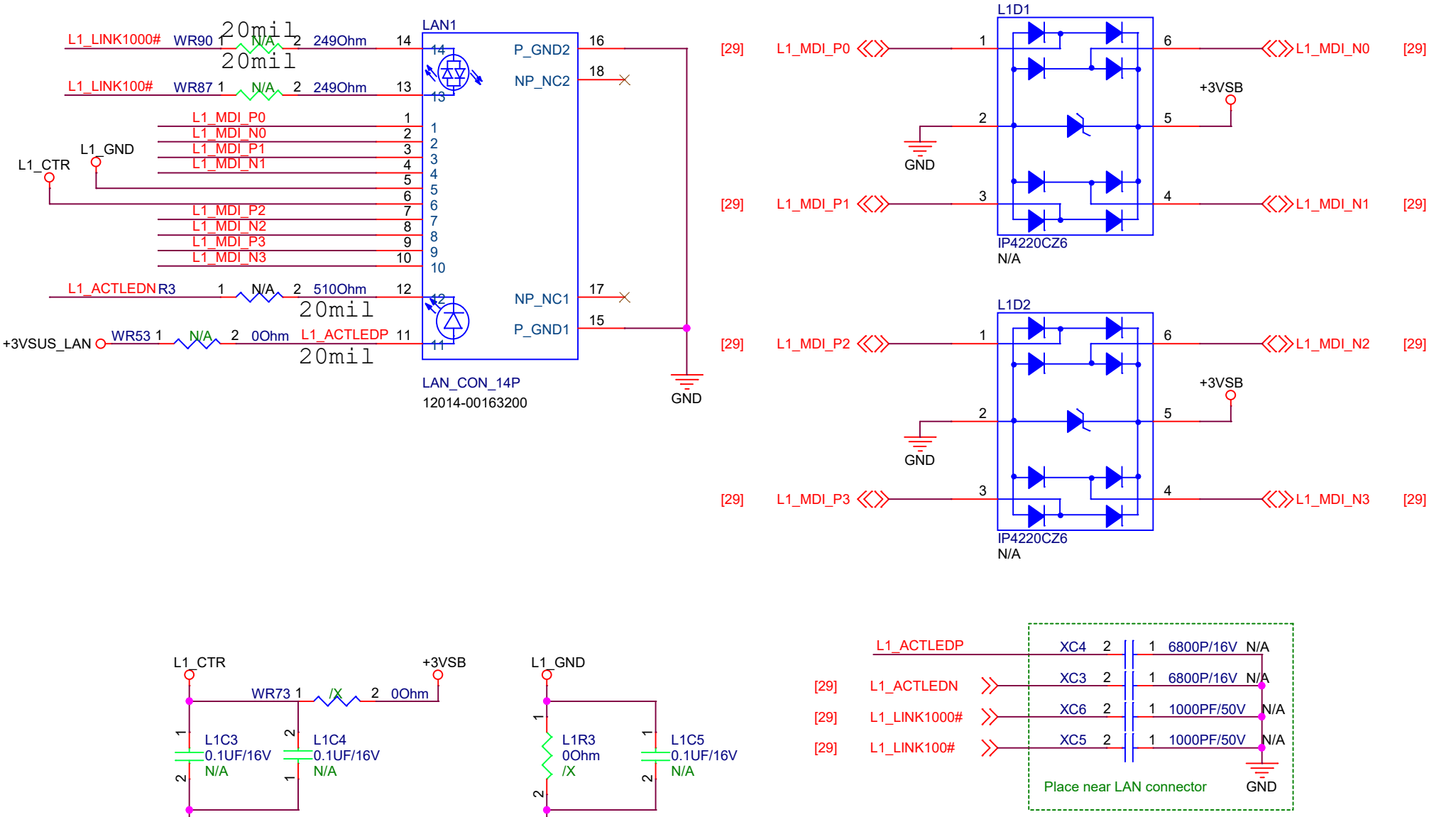
ASUSTEK COMPUTER INC

Title : LAN1_RTL8111G

Engineer:

Size	Project Name	Rev
Custom	EMB-BT7	R2.00

Date: Friday, October 04, 2019 Sheet 29 of 60



ASUSTEK COMPUTER INC	Title : LAN1_RJ45	
	Engineer:	
Size: A	Project Name: EMB-BT7	Rev: R2.00
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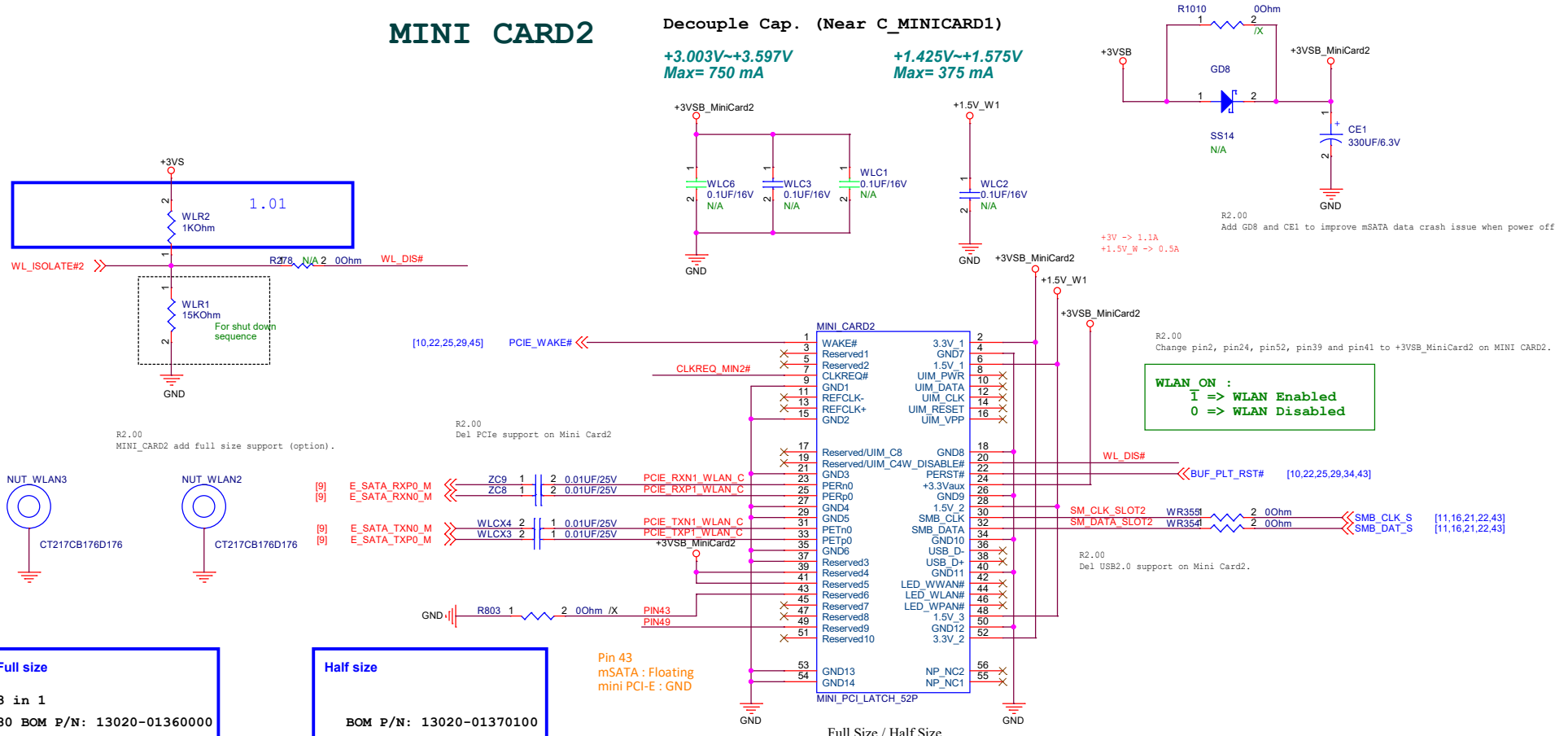
MINI CARD2

Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

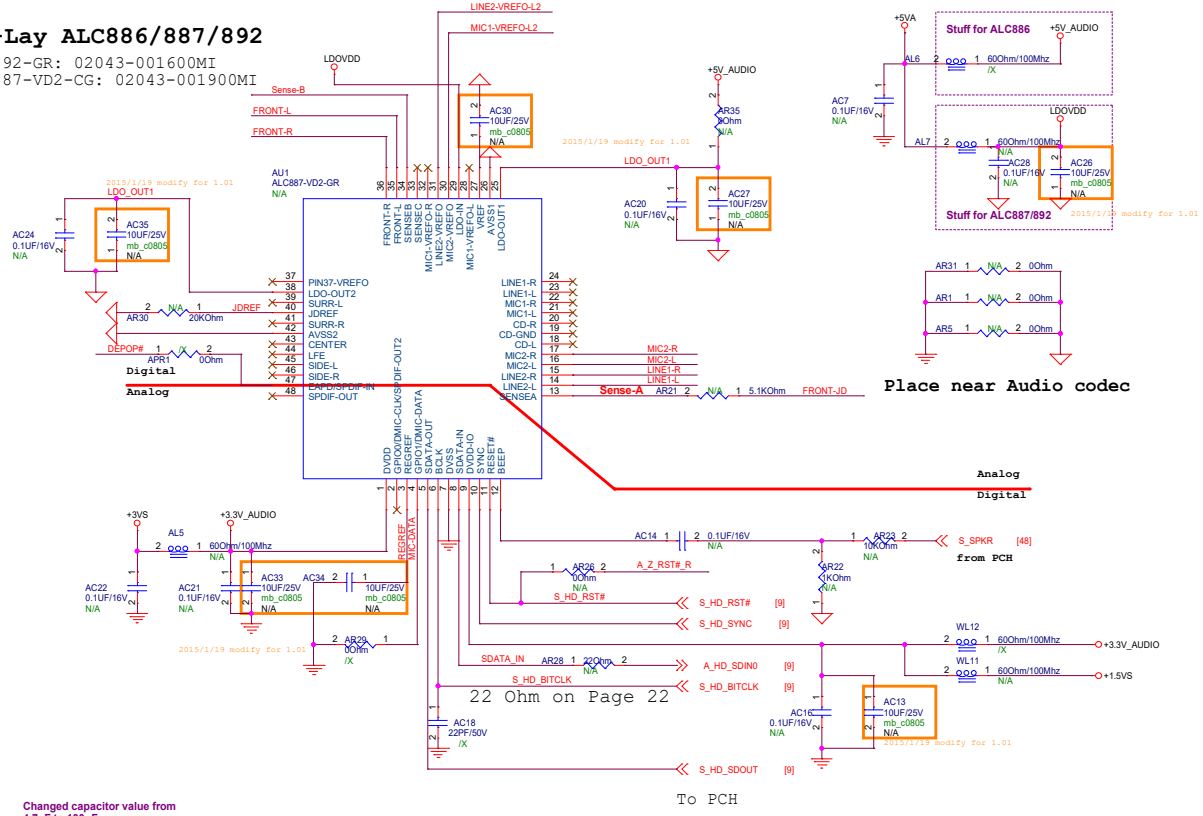
+1.425V~+1.575V
Max= 375 mA



ASUSTeK COMPUTER INC	Title : Mini_Card2_mSATA	
	Engineer:	
Size: A3	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 31 of 60	

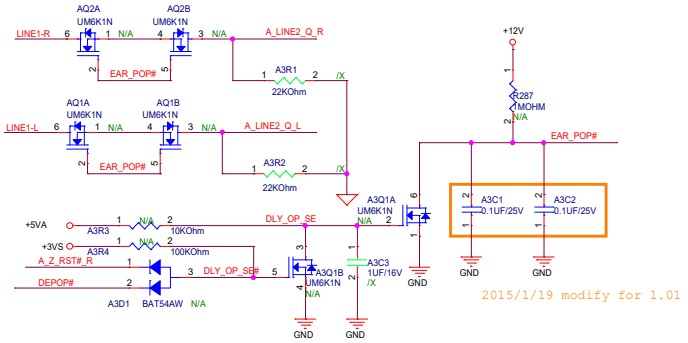
Co-Lay ALC886/887/892

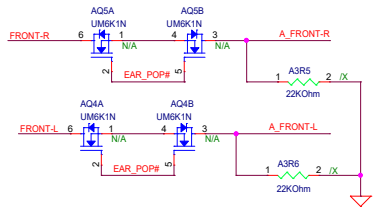
ALC892-GR: 02043-001600MI
ALC887-VD2-CG: 02043-001900MI

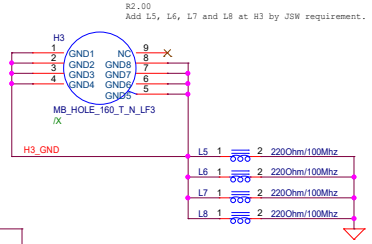


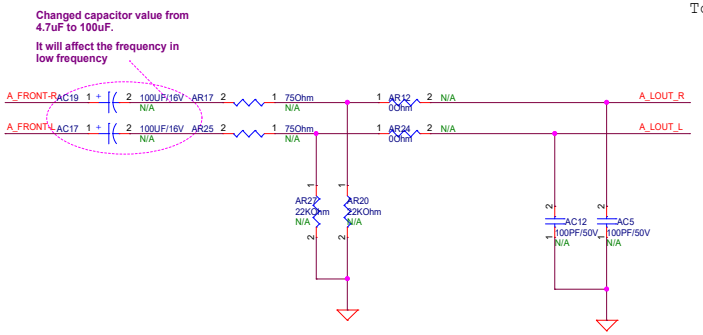
Place near Audio codec

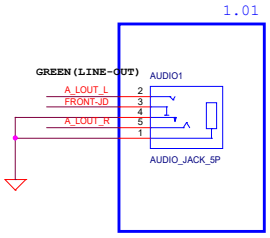
Anti POP for HEADPHONE

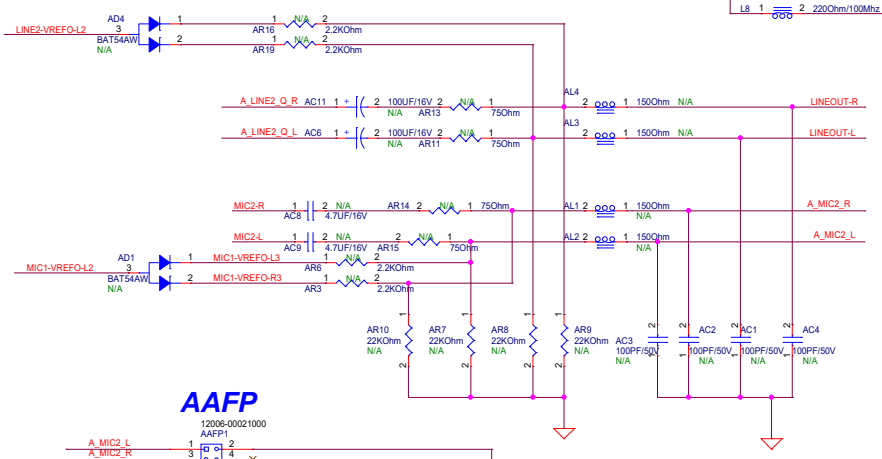


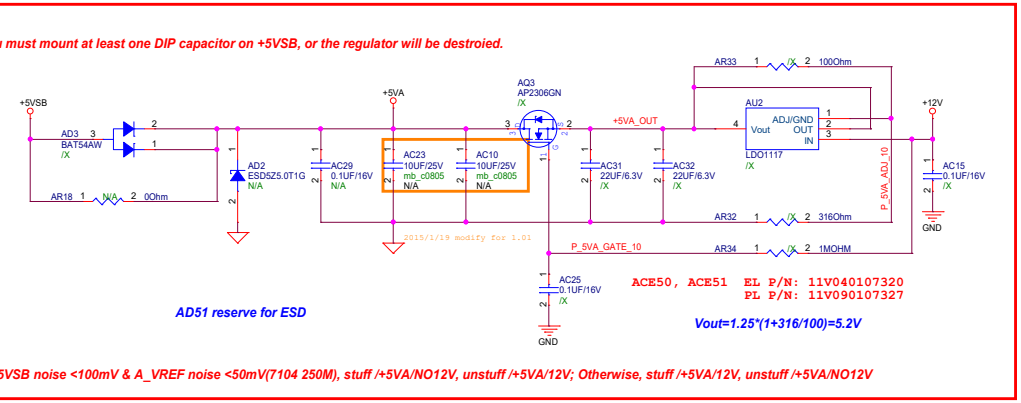




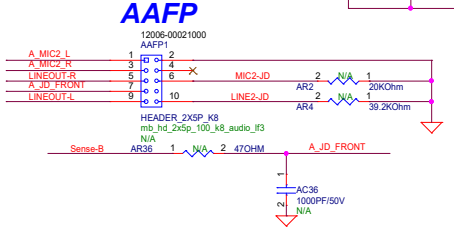








AAFP



ASUSTEK COMPUTER INC	Title : ALC887		
	Engineer:		
Size: C	Project Name: EMB-BT7		Rev: R2.00
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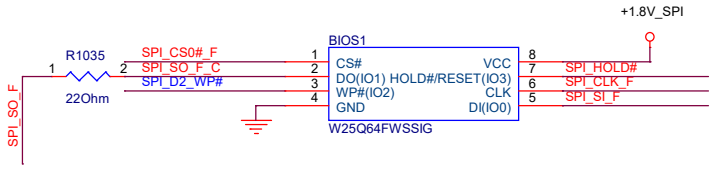
R2.00
Remove DIO function

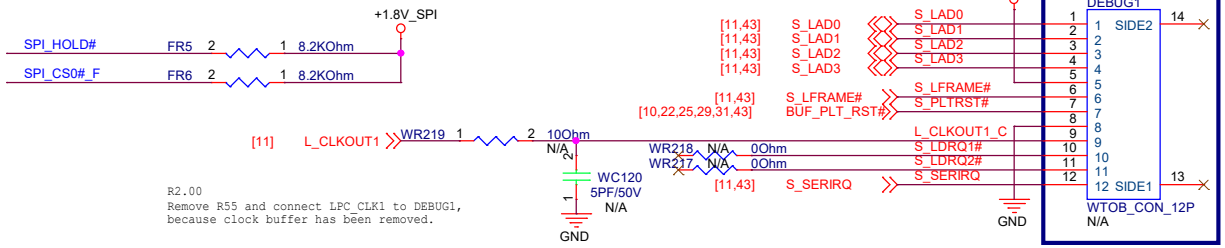
ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 33 of 60	

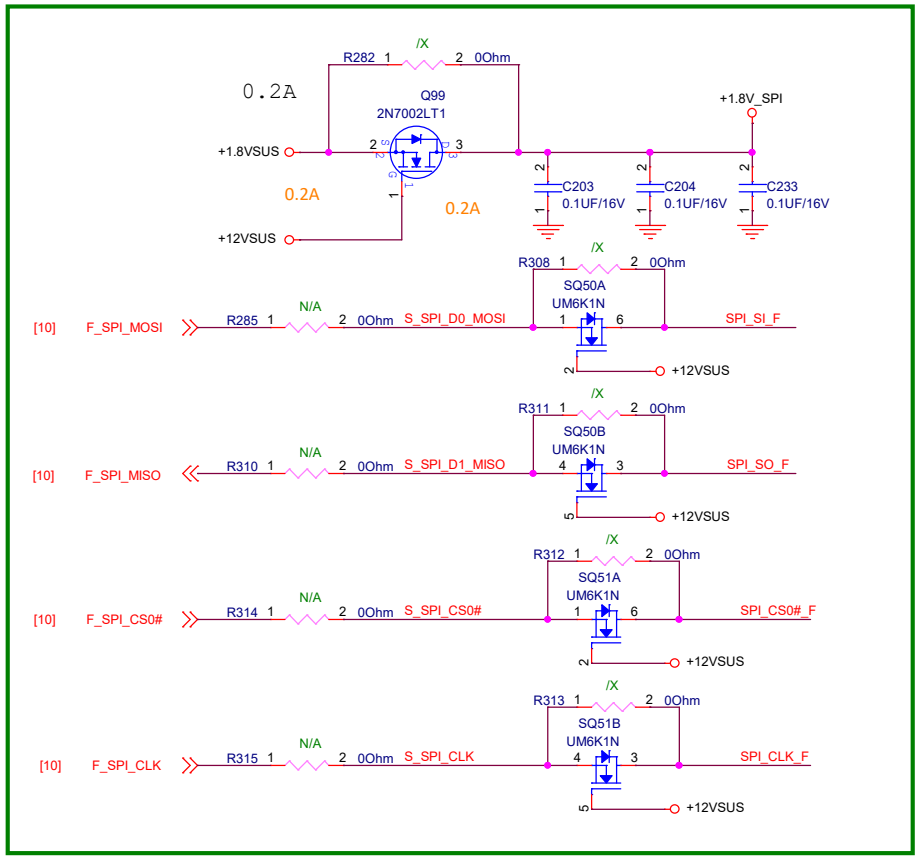
BIOS

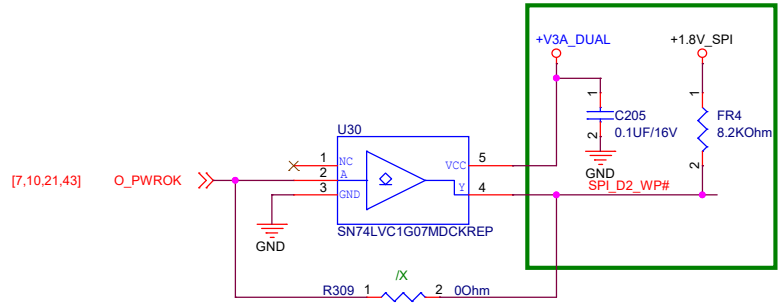


DEBUG PORT

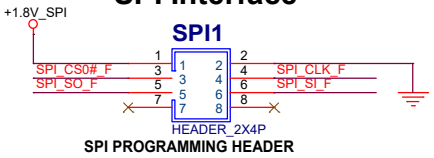
1.01







SPI Interface



SPI PROGRAMMING HEADER

EMB-BT7

ASUSTek Computer Inc.

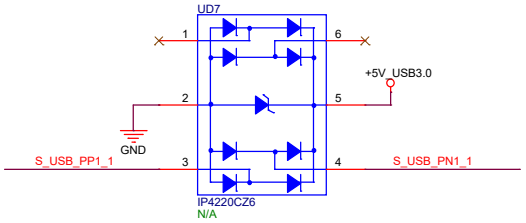
Title : SINGLE BIOS_SPI-1

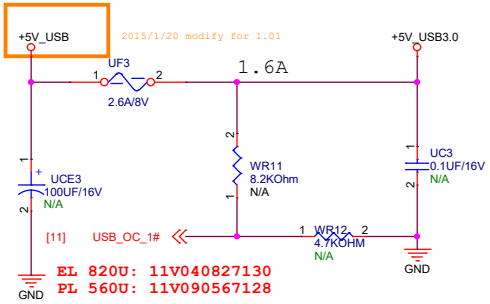
Engineer:

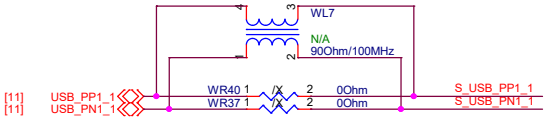
Size	Project Name	Rev
B	EMB-BT7	R2.00

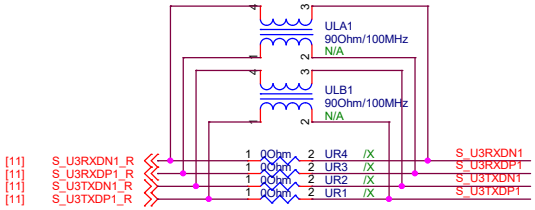
Date: Friday, October 04, 2019 Sheet 34 of 60

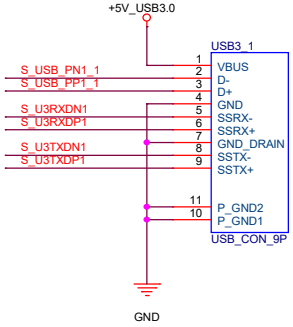
R2.00
Add UD7 for USB2.0 ESD protection.

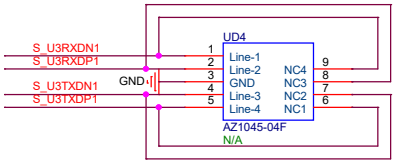






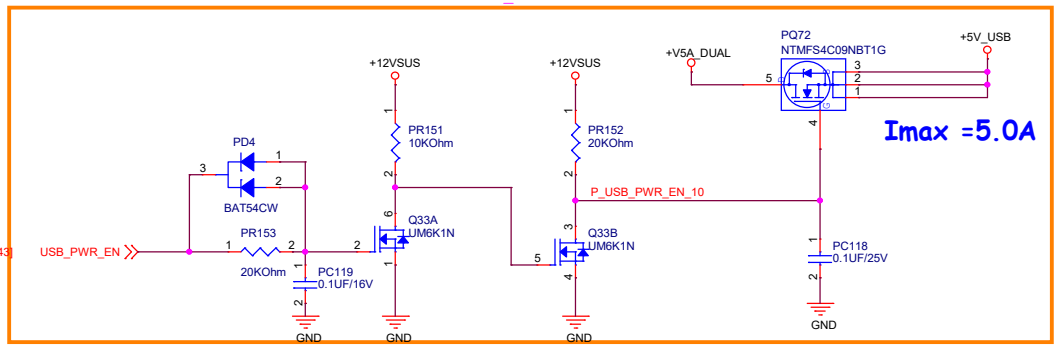






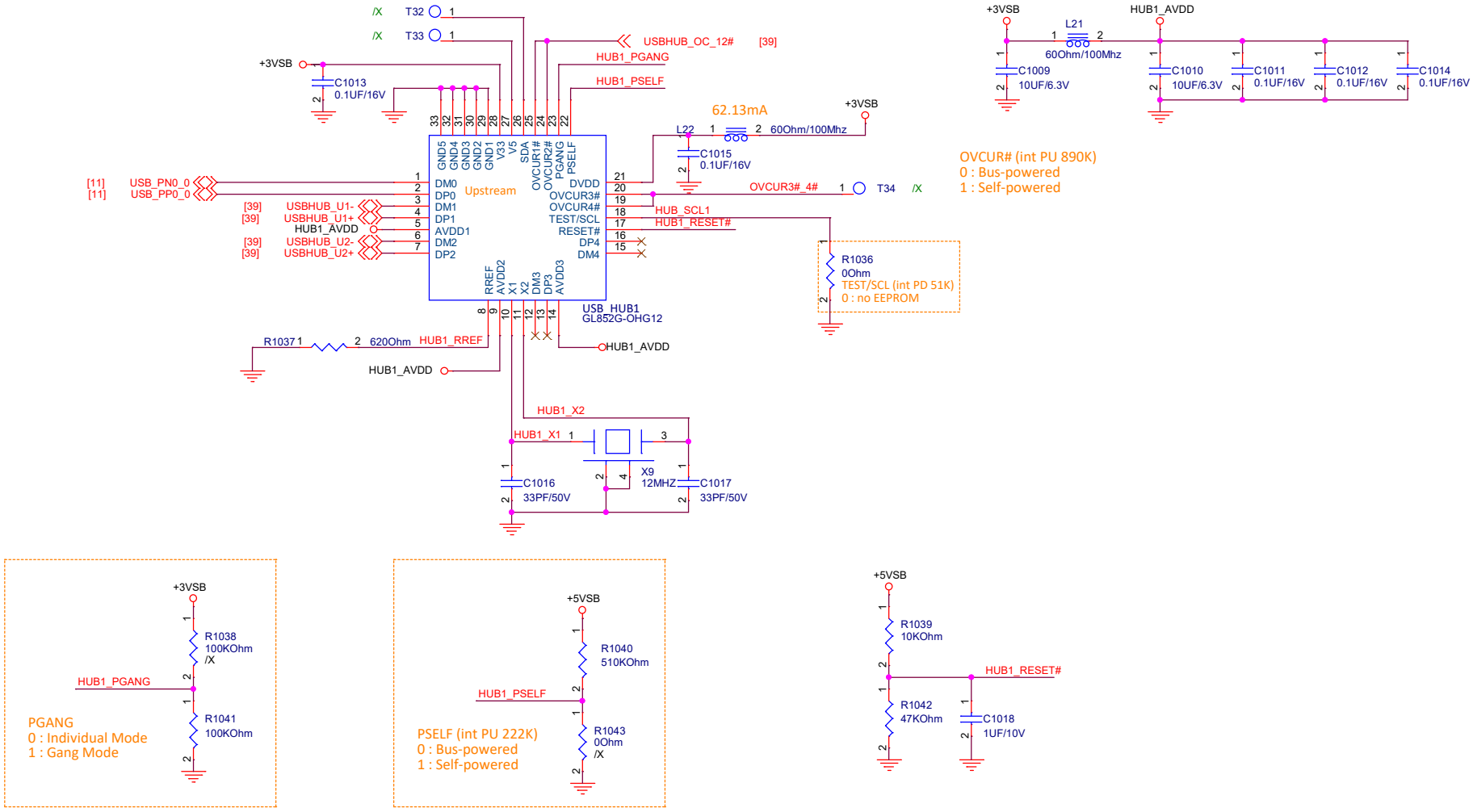
EMB-BT7 add power source
+5V_USB for USB Power.

R2.00
Change PQ72 from PH6030DLV to NTMFS4C09NBT1G by CE suggestion.



2015/1/20 modify for 1.01

ASUSTek Computer Inc.	Title : USB3.0 Connector	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 35 of 60	



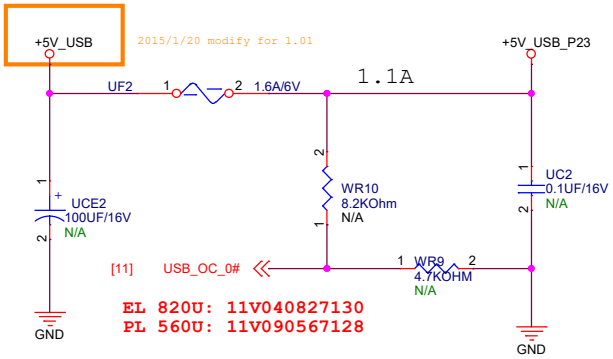
ASUSTeK COMPUTER INC.	Title : USB Hub	
	Engineer:	
Size: B	Project Name: EMB-BT1	Rev: R3.00
Date: Friday, October 04, 2019	Sheet 36 of 60	

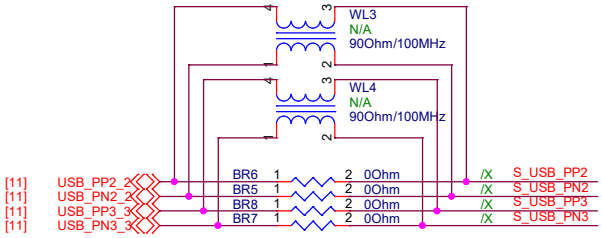
R2.00

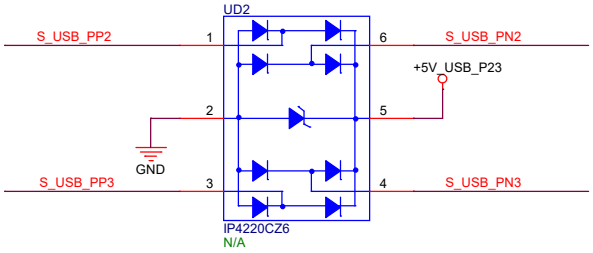
Remove USB2.0 Hub.

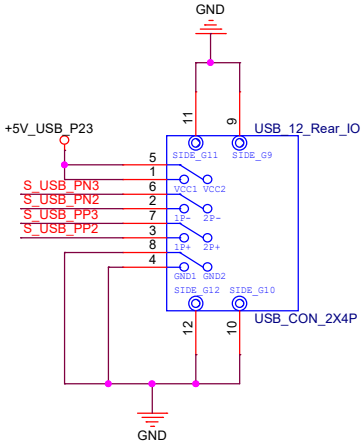
ASUSTeK COMPUTER INC.	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 37 of 60	

Circuit in this page is also including in Back I/O demo circuit



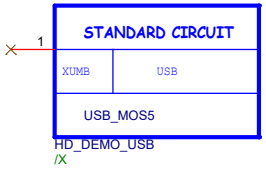






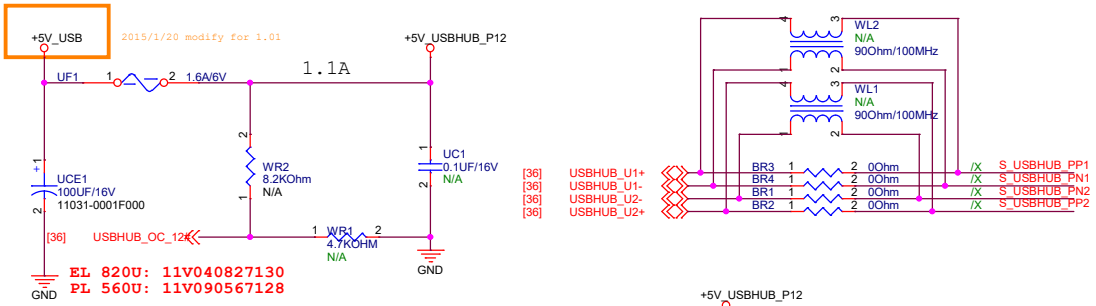
R2.00
USB port2 connect to USB_23 connector,
because MINI CARD2 don't need USB interface by JSW confirmed.

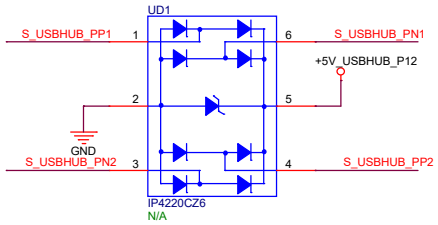
R2.00
USB port3 connect to USB_23 connector,
because USB_Hub IC has been removed.

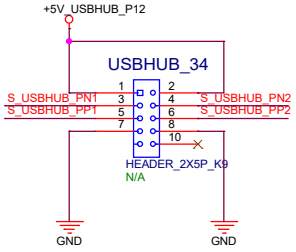


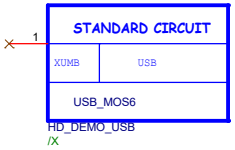
ASUSTeK COMPUTER INC.	Title : USB_23	
	Engineer:	
Size: B	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 38 of 60	

Circuit in this page is also including in Back I/O demo circuit









ASUSTeK COMPUTER INC.	Title : USBHUB_34	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 39 of 60	

R2.00
Remove USB_HUB56 Header

ASUSTeK COMPUTER INC.	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 40 of 60	

R2.00

Remove USB_HUB7 Header.

ASUSTeK COMPUTER INC.	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 41 of 60	

R2.00
Remove TPM function.

ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
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Resume Reset# function, It is power good signal of 3VSB, which is delayed 66ms as 3VSB arrives at 2.8V.

PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed via register (100ms ~ 400ms).

FAN Control

1.02

+5VSB Switch

+3VSB Switch

EMB-BT7 add USB Power Enable

EMB-BT7 add ATX Power Good In circuit for SIO suggestion.

EUP

DSW

POWER TRIP

RSMRST# POWER Down

(PLACE THE CAPCITOR CLOSE TO IC)

20 MIL

Close to SIO

R2.00
Change PQ26 and PQ33 from EMB07P03G to EMF09P02V by CE suggestion.

2015/06/17
Solve +5VSB two steps wave form
OC8 change to 1uF

2015/1/20 modify for 1.01

2015/1/19 modify for 1.01

2015/11/30
WQ18 BJT --> NMOS

R2.00
Connect LPC_CLK0 to SIO, because clock buffer has been removed.

R2.00
Remove COM1, COM3-COM6, LPT and KBMS functions.

R2.00
Del FINAL_POWGD,because related schematic has been removed.

R2.00
Change +1.2VSUS to +1.8VSUS, because +1.2VSUS related design has been removed.

20150730
Update by Kevin
R579 change to 75k ohm
To solve AC power loss issue

Title :	SIO F81866
Engineer:	
ASUSTEK COMPUTER INC	
Size: Custom	Project Name: EMB-BT7
Rev:	R2.00
Date: Friday, October 04, 2019	Sheet 43 of 60

R2.00

Remove COM1 and LPT conne

ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
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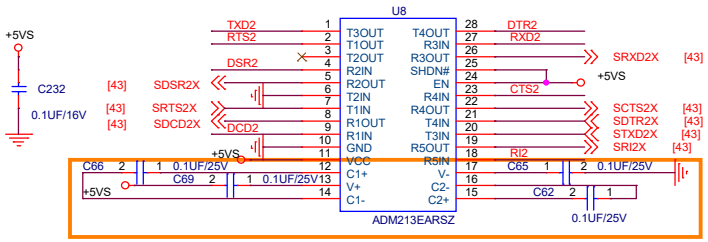
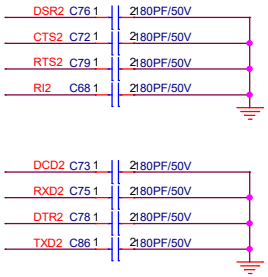
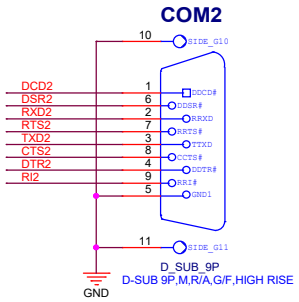
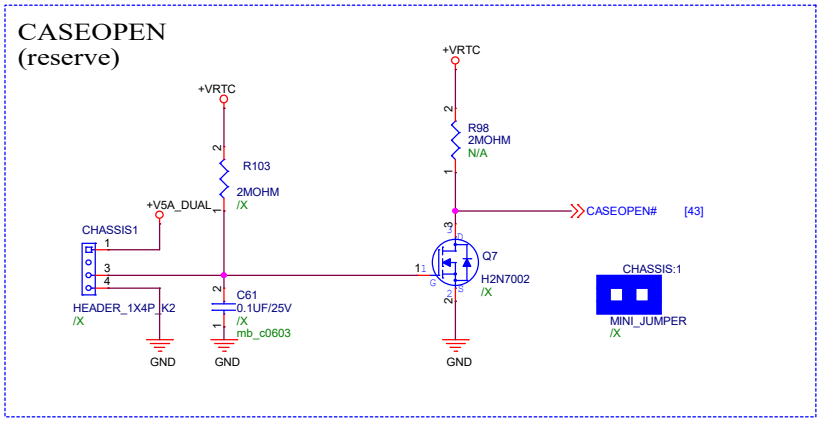
COM2



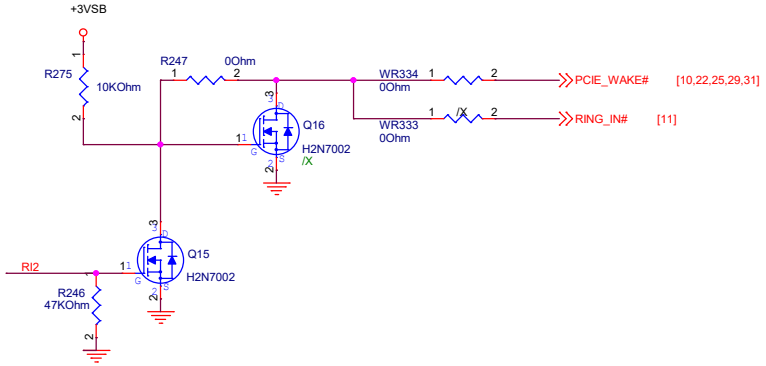
2015/1/19 modify for 1.01







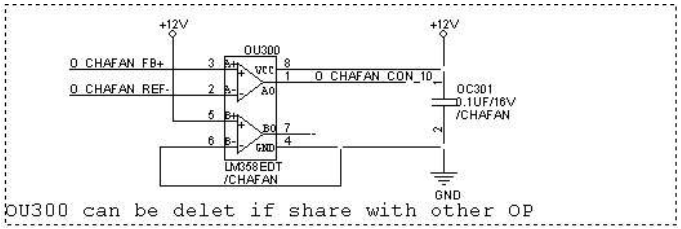
WAKE ON MODEM



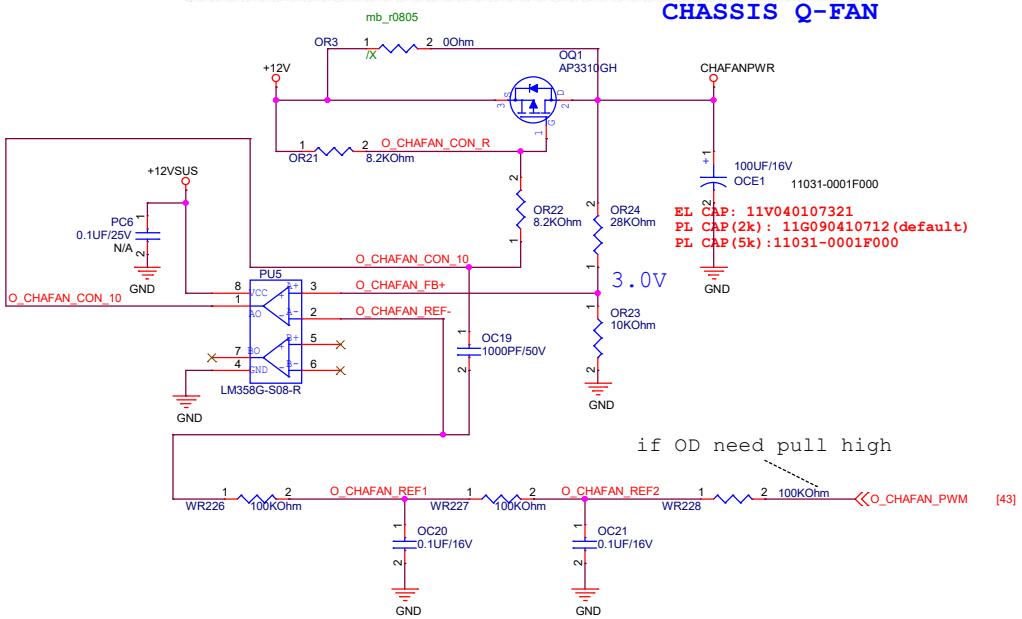
R2.00

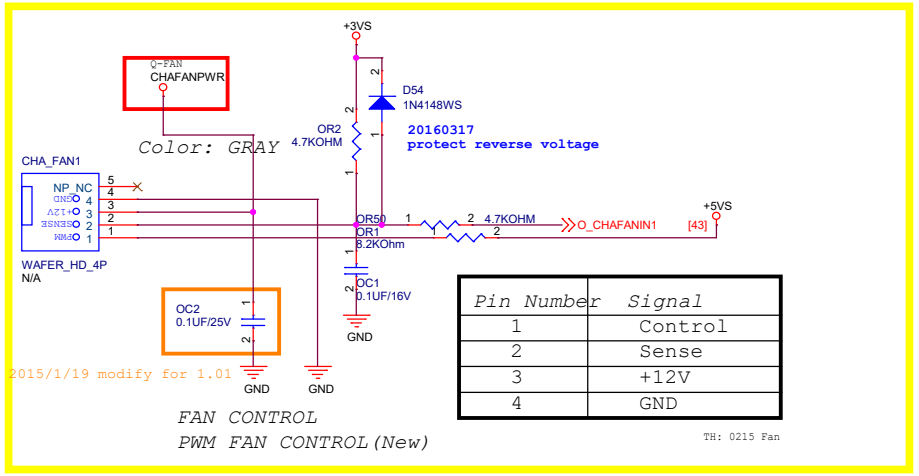
Remove COM3~COM6 connectors.

ASUSTEK COMPUTER INC	Title : COM2	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 45 of 60	

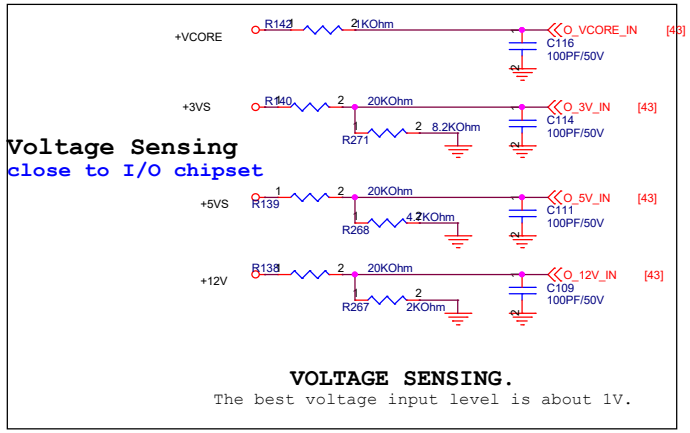


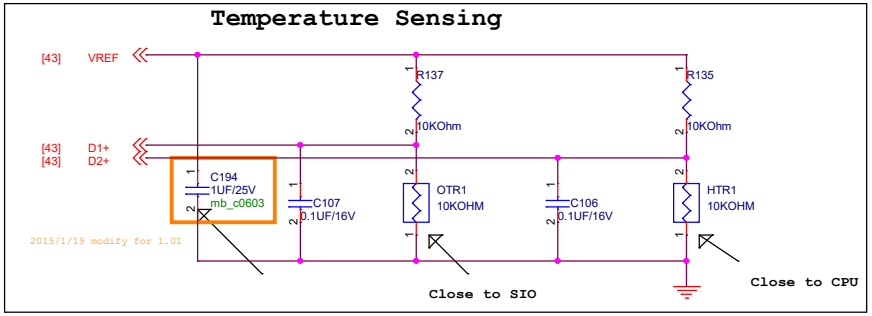
CHASSIS Q-FAN





Pin Number	Signal
1	Control
2	Sense
3	+12V
4	GND





ASUSTEK COMPUTER INC

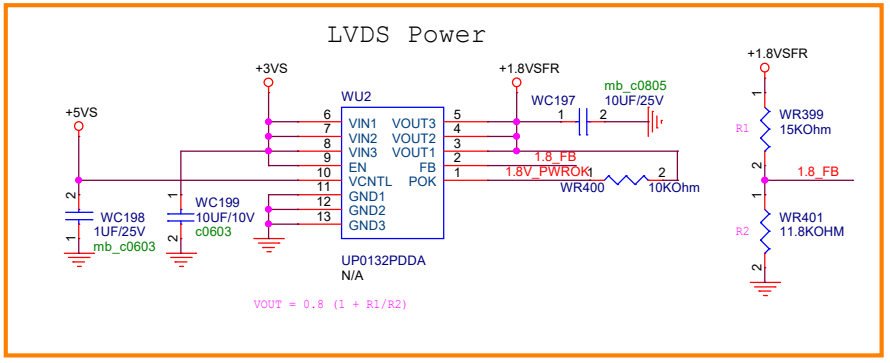
Title : CHA_FAN1& HW Monitor

Engineer:

Size	Project Name	Rev
Custom	EMB-BT7	R2.00

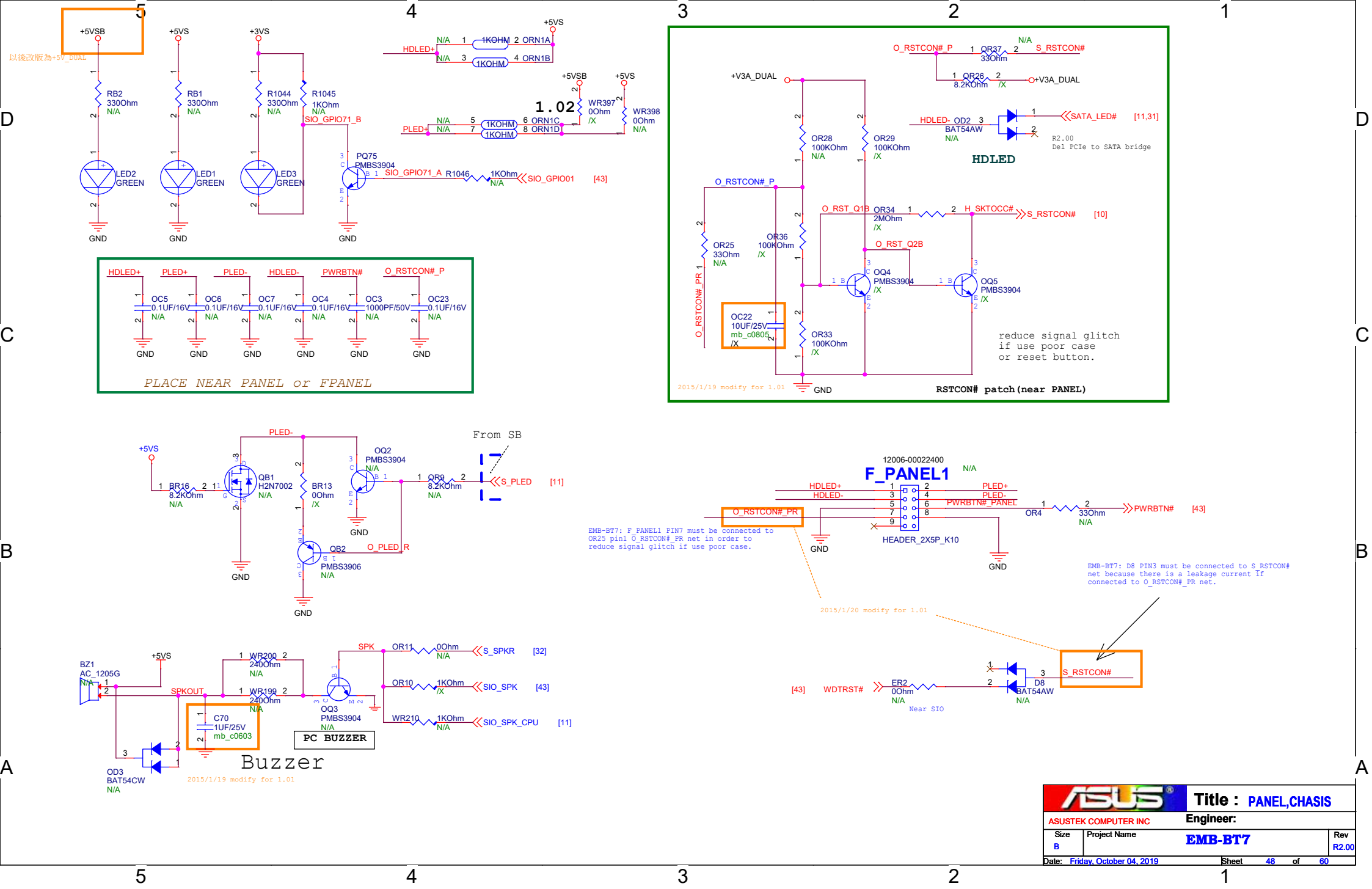
Date: Friday, October 04, 2019 Sheet 46 of 60

R2.00
Remove KBMS connector.



2015/1/20 modify for 1.01

ASUSTEK COMPUTER INC	Title : LVDS power		
	Engineer:		
Size: B	Project Name: EMB-BT7		Rev: R2.00
Date: Friday, October 04, 2019	Sheet 47 of 60		



Title :	PANEL,CHASIS
ASUSTEK COMPUTER INC	Engineer:
Size: B	Project Name: EMB-BT7
Rev: R2.00	
Date: Friday, October 04, 2019	Sheet 48 of 60

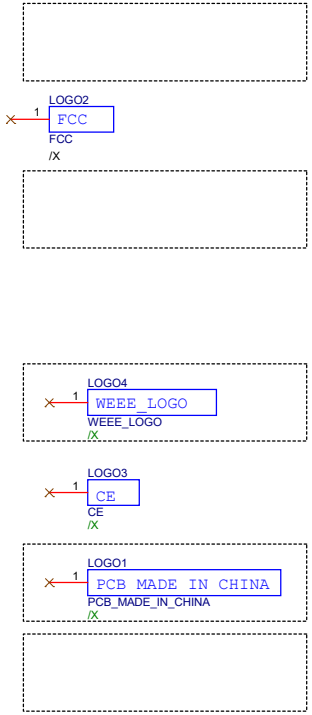
R2.00
Remove LPC Clock buffer.

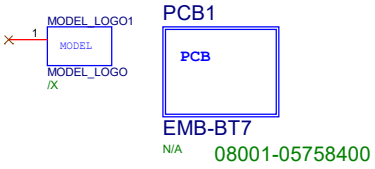
ASUSTEK COMPUTER INC	Title : EMPTY	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 49 of 60	

EMI

Logo

common Logo for all projects



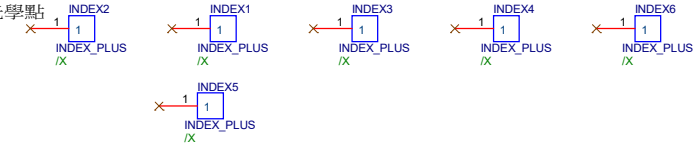


Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

小顆十字光學點



ASUSTEK COMPUTER INC	Title : Selling Point_Logo	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 50 of 60	

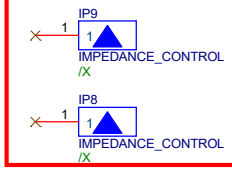
Delete it for EMS

You can only choose 6 pcs point for your project!Please choose them by your need!

Intel Platform(非G41)

Priority1,must choose if MB have these functions

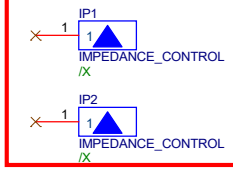
1 LAN



2 PCIE GEN2/3

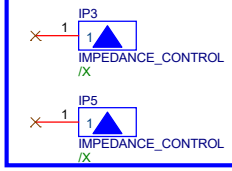
3 DDR3 DATA&CTRL

4 USB2.0

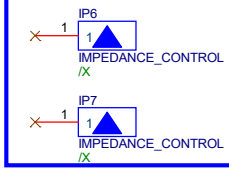


Priority2,can choose if MB have these functions(By project)

1 DP/DVI/HDMI



2 USB3.0



Priority3,can choose if MB have these functions(By project)

1 2

	W/P/S	single end impedance
DDR3 CLK	8/5/20	62ohm+/-15%
DMI	4/5/12	85ohm+/-15%
USB3	5/7/20	85ohm+/-15%
DP/DVI/HDMI	4/6/20	90ohm+/-15%
USB2.0	4.5/7.5/12	90ohm+/-15%
DDR3 DATA& CTRL	6.5mil	40ohm+/-15%
PCIE GEN2/3	5/5/16	80ohm+/-15%
LAN	4/8	100 ohm +/-15%

*** You can only choose 1 function to place point per block.

ASUSTEK COMPUTER INC	Title : PCB Impedance Point	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
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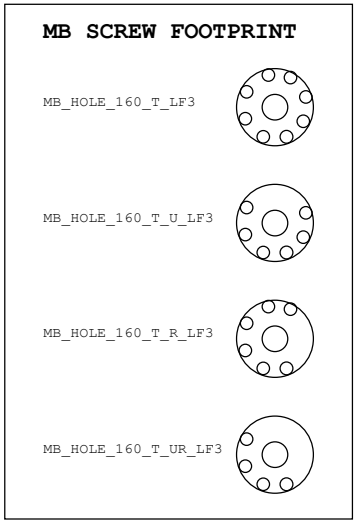
m-ATX Screw Hole

Delete it for EMS

R2.00
Add L9, L10, L12 and L14 at H4 by JSW requirement.

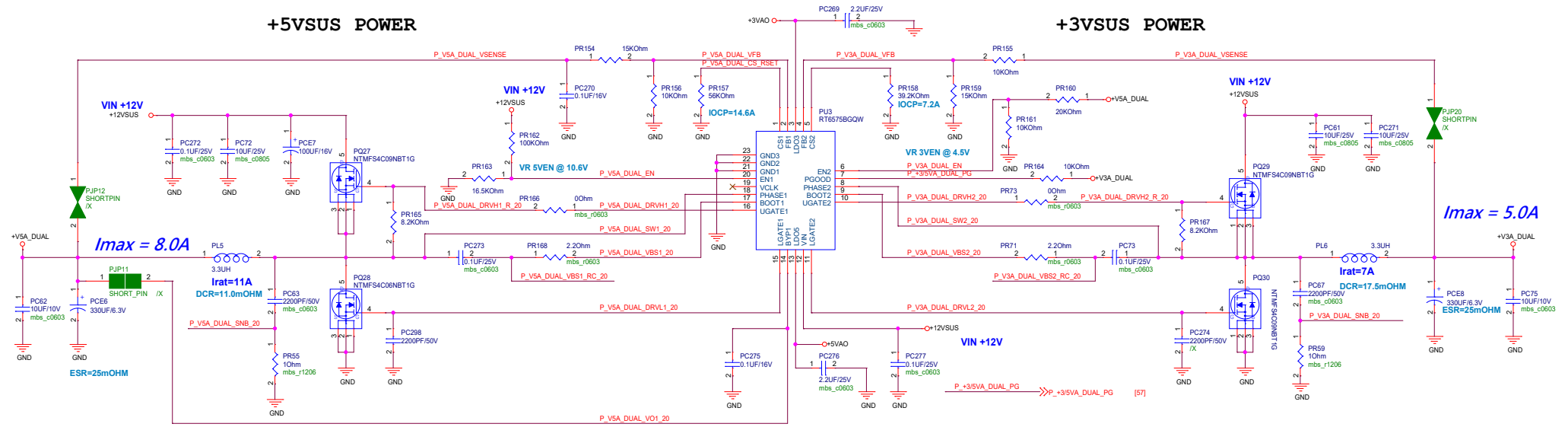
MB SCREW FOOTPRINT



m-ATX Screw Select

	Standard (9.6 x 9.6)	Scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H20	V	V

ASUSTEK COMPUTER INC	Title : m-ATX Screw Hole	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 52 of 60	



Title	5V/3.3V_DUAL&SYSTEM PWR
Engineer:	
ASUSTEK COMPUTER INC	
Size	C
Project Name	EMB-BT7
Rev	R2.00
Date:	Friday, October 04, 2019
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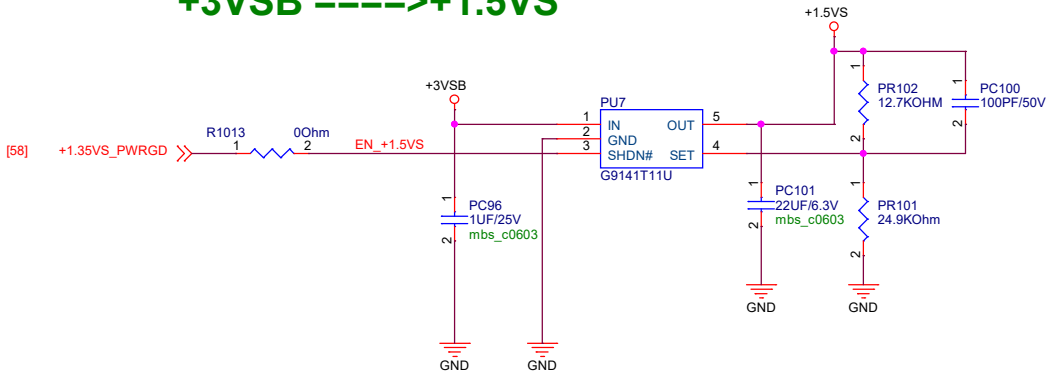
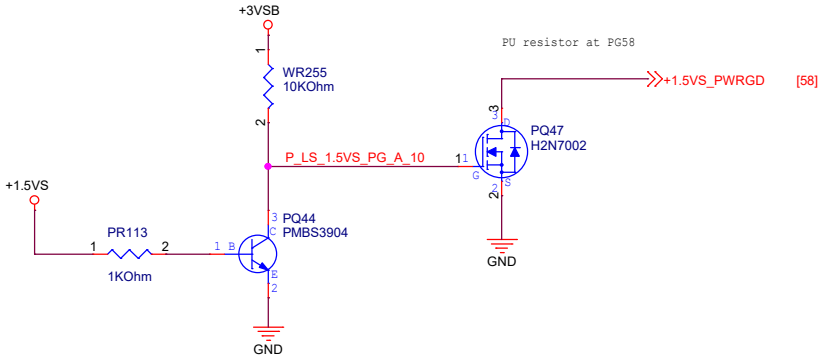
Io:0.403A

+3VSB ====>+1.5VS

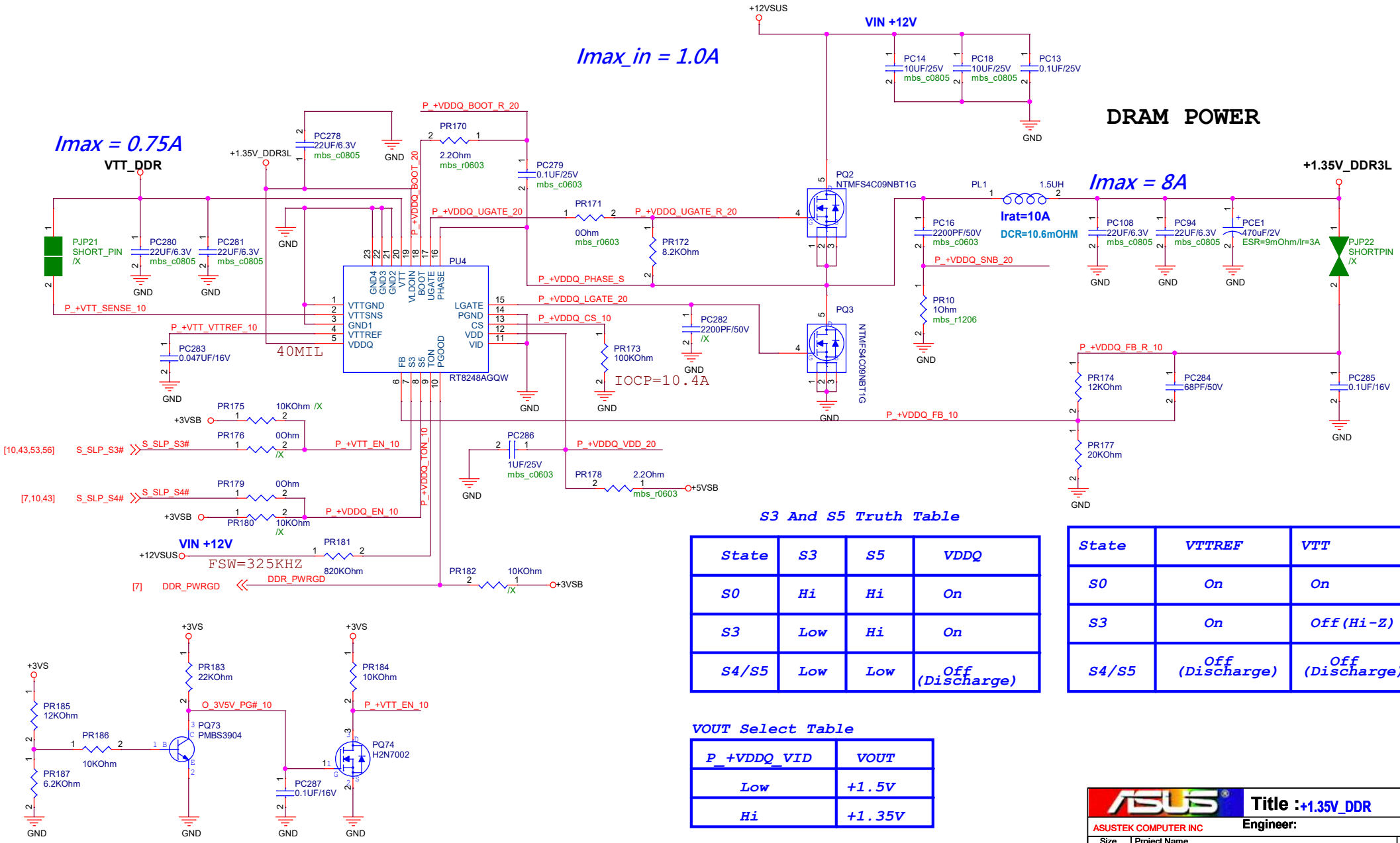


When HDA_LPE_V1P5V1P8_S3 is powered by a V1P5S rail, the V1P5S rail sequencing should meet the same sequencing requirements as the V1P8S rail.



ASUSTEK COMPUTER INC	Title : +1.5VS		
	Engineer:		
Size: B	Project Name: EMB-BT7		Rev: R2.00
Date: Friday, October 04, 2019	Sheet 54 of 60		

DRAM POWER



S3 And S5 Truth Table

State	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Low	Hi	On
S4/S5	Low	Low	Off (Discharge)

State	VTTREF	VTT
S0	On	On
S3	On	Off(Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)

VOUT Select Table

P_+VDDQ_VID	VOUT
Low	+1.5V
Hi	+1.35V

ASUSTEK COMPUTER INC

Title :+1.35V_DDR

Engineer:

Size	Project Name	Rev
B	EMB-BT7	R2.00

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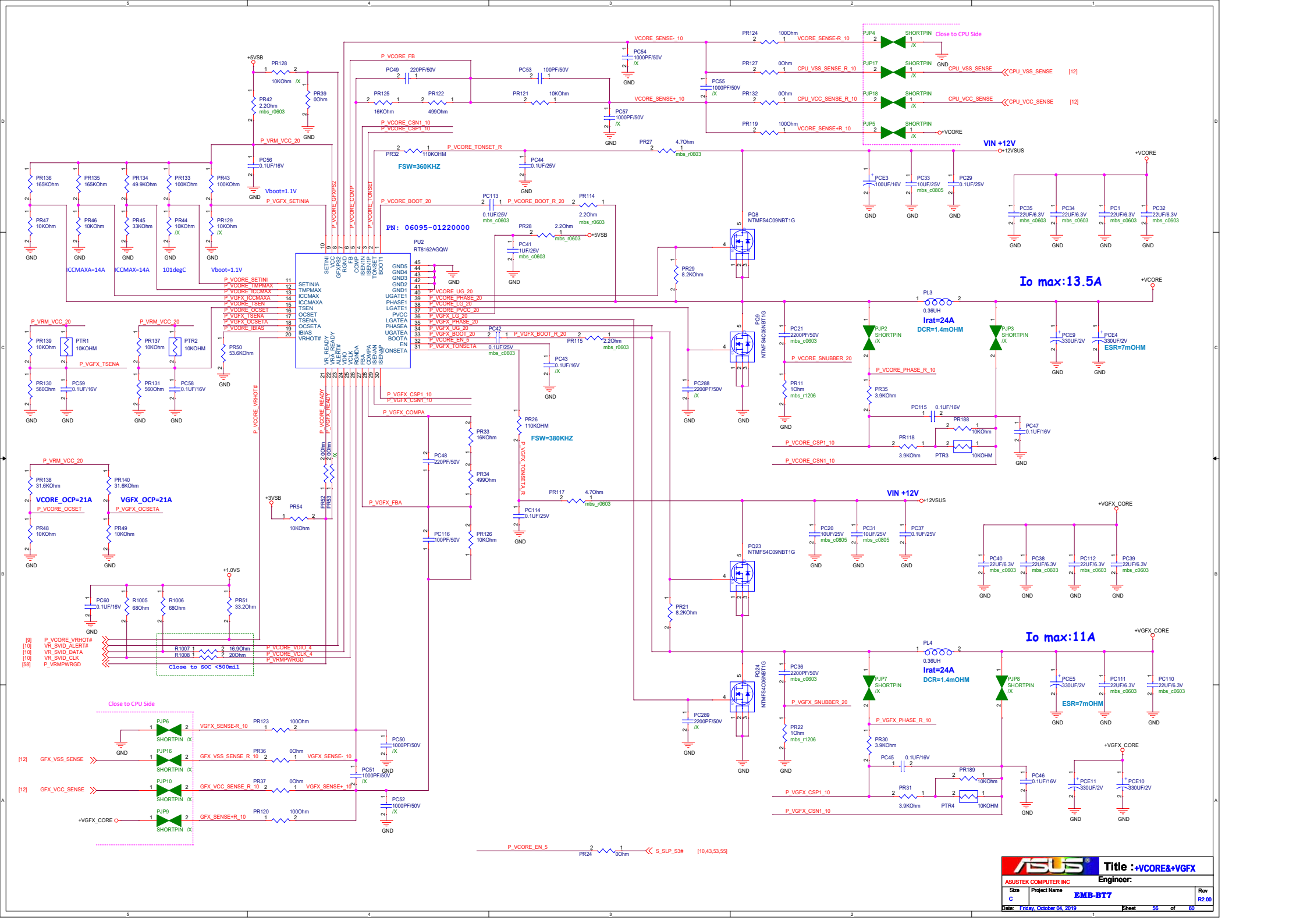
PU2
RT8162AGQW
PN: 06095-01220000
FSW=360KHZ
FSW=380KHZ
Vboot=1.1V
Vboot=1.1V
ICCMAXA=14A
ICCMAX=14A
101degC
VIN +12V
Io max:13.5A
Irat=24A
DCR=1.4mOHM
ESR=7mOHM
Io max:11A
Irat=24A
DCR=1.4mOHM
ESR=7mOHM
VCORE_OCP=21A
VGFX_OCP=21A
Close to CPU Side
Close to SOC <500mil
Title :+VCORE&+VGFX
ASUSTEK COMPUTER INC
Engineer:
Project Name
EMB-BT7
Rev
R2.00
Size
C
Date: Friday, October 04, 2019
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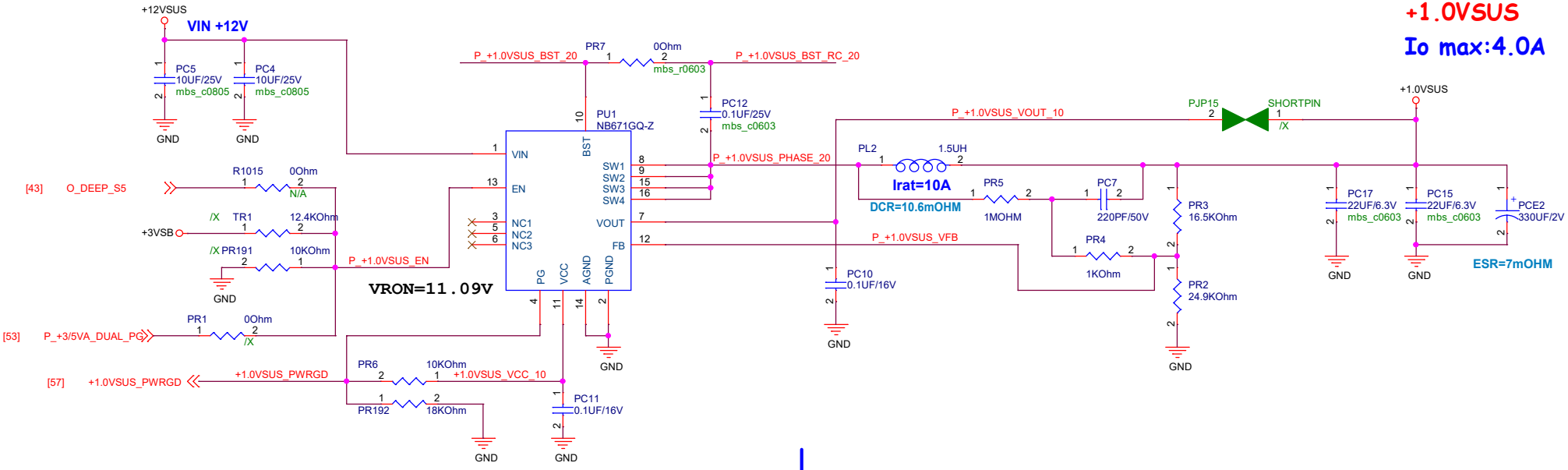
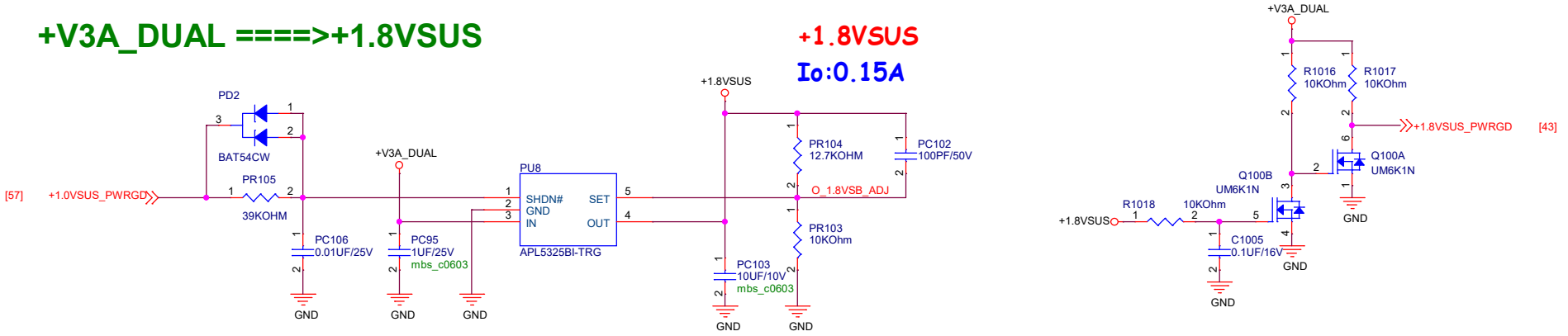
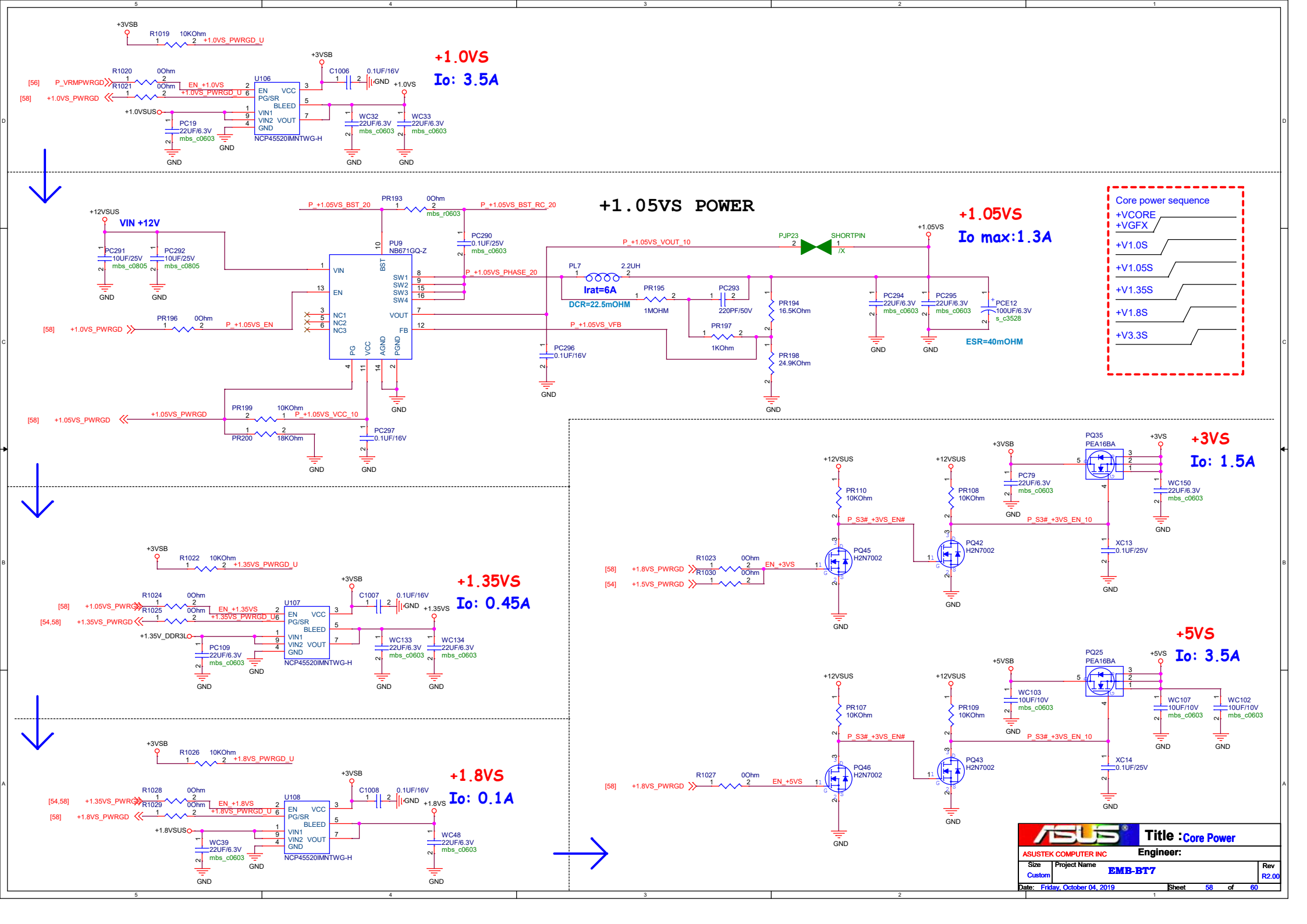




ASUSTEK COMPUTER INC	Title : +1.0VSUS/+1.8VSUS	
	Engineer:	
Size: B	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 57 of 60	


+1.0VS
Io: 3.5A
+1.05VS POWER
+1.05VS
Io max:1.3A
VIN +12V
Irat=6A
DCR=22.5mOHM
ESR=40mOHM
Core power sequence
+VCORE
+VGFX
+V1.0S
+V1.05S
+V1.35S
+V1.8S
+V3.3S
+3VS
Io: 1.5A
+1.35VS
Io: 0.45A
+5VS
Io: 3.5A
+1.8VS
Io: 0.1A
Title : Core Power
ASUSTEK COMPUTER INC
Engineer:
Size
Custom
Project Name
EMB-BT7
Rev
R2.00
Date: Friday, October 04, 2019
Sheet 58 of 60

EMB-BT7 schematic change list for R1.01A

2015/07/28

1. Solve PLX8605 reset issue
   delete WR405 WC200 WQ23 WR403 WR402 WR404 WR350 WQ20 WR339 WQ19 WR338 WR341
   add C449 U33 R586 R585 U34 R589 C450 D9 R588
   R238 change to 0 ohm
2. Solve compatibility of PCIE card
   add C500 C501
3. For spec.
   WR216 set to NC

EMB-BT7 schematic change list for R1.10

2015/11/30

1. Add level shift of HDMI DDC singal

EMB-BT7 schematic change list for R1.11

2016/03/22

1. Modify SPI BIOS level shift circuit

EMB-BT7 schematic change list for R1.12 (Customer's request)

1. SATA singal connect to MINI_CARD2 from MINI_CARD1
2. memory slot change to low profire

EMB-BT7 schematic change list for R1.12A

2017/09/06

1. Modify SVID circuit

ASUSTEK COMPUTER INC	Title : History1	
	Engineer:	
Size: Custom	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 59 of 60	

R2.00
PG09: Remove SATA port0 colay with SATA3G_1, because SATA3G_1 connector has been removed.
PG09: Del PCIe to SATA bridge, let PCIe port1 NC.
PG09/PG29: Del PCIe switch, connect PCIe port3 to LAN1 controller.
PG10: Del PCIe to SATA bridge, let PCIE_CLK1 NC and del CLK EMI cap (WC79, WC80).
PG10/PG29: Del PCIe switch, connect PCIE_CLK3 to LAN1 controller.
PG10: Add reset IC at RSMRST# signal by JSW.
PG10: Set Q11, WR287, WR291, R180 and R172 to /X.
PG10: Add level shifter IC for PM_SUSC#_18, PM_SUSB#_18 and PLT_RST# signals.
PG11/PG39: USB port0 connect to USB_4 connector, because USB_Hub IC has been removed.
PG11/PG38: USB port2 connect to USB_23 connector, because MINI CARD2 don't need USB interface by JSW confirmed.
PG11/PG38: USB port3 connect to USB_23 connector, because USB_Hub IC has been removed.
PG11: Remove HSIC interface, because USB_Hub IC has been removed.
PG11: Remove ENRS232_T, ENRS422_T and ENRS485__T, because COM1 has been removed.
PG11/PG34: Remove R55 and connect LPC_CLK1 to DEBUG1, because clock buffer has been removed.
PG11/PG43: Connect LPC_CLK0 to SIO, because clock buffer has been removed.

PG13: AD16 and AD18 connect to GND, because MCSI interface is not used.
PG21: Change Q31 from EMB07P03G to EMF09P02V by CE suggestion.
PG22: Del USB2.0 support on Mini Card1 by JSW confirmed.
PG22: Del UIM support on Mini Card1 by JSW confirmed.
PG23: Remove PCIe to SATA bridge by JSW confirmed.
PG24: Del SATA3G_1, SATA6G_1, SATA6G_2 and 1.25V LDO of ASM1061.
PG27: Remove PCIe switch.
PG28: Remove PCIex1 Connector.
PG31: Add GD8 and CE1 to improve mSATA data crash issue when power off.
PG31: Change pin2, pin24, pin52, pin39 and pin41 to +3VSB_MiniCard2 on MINI CARD2.
PG31: Del USB2.0 support on Mini Card2.
PG31: Del PCIe support on Mini Card2.
PG31: MINI_CARD2 add full size support (option).
PG32: Add L5, L6, L7 and L8 at H3 by JSW requirement.
PG33: Remove DIO function.
PG35: Add UD7 for USB2.0 ESD protection.
PG35: Change PQ72 from PH6030DLV to NTMFS4C09NBT1G by CE suggestion.
PG36: Remove USB2.0 Hub.
PG37: Remove USB2.0 Hub.
PG40: Remove USB_HUB56 Header.
PG41: Remove USB_HUB7 Header.
PG42: Remove TPM function.
PG43: Remove COM1, COM3~COM6, LPT and KBMS functions.
PG44: Remove COM1 and LPT connector.
PG45: Remove COM3~COM6 connectors.
PG47: Remove KBMS connector.
PG49: Del CLK2 connect to TPM, because TPM IC has been removed.
PG52: Add L11, L13, L15 and L16 at H1 by JSW requirement.
PG52: Add L17, L18, L19 and L20 at H2 by JSW requirement.
PG52: Add L9, L10, L12 and L14 at H4 by JSW requirement.

PG43: Change +1.2VSUS to +1.8VSUS, because +1.2VSUS related design has been removed.

ASUSTEK COMPUTER INC	Title : History2	
	Engineer:	
Size: A3	Project Name: EMB-BT7	Rev: R2.00
Date: Friday, October 04, 2019	Sheet 60 of 60	