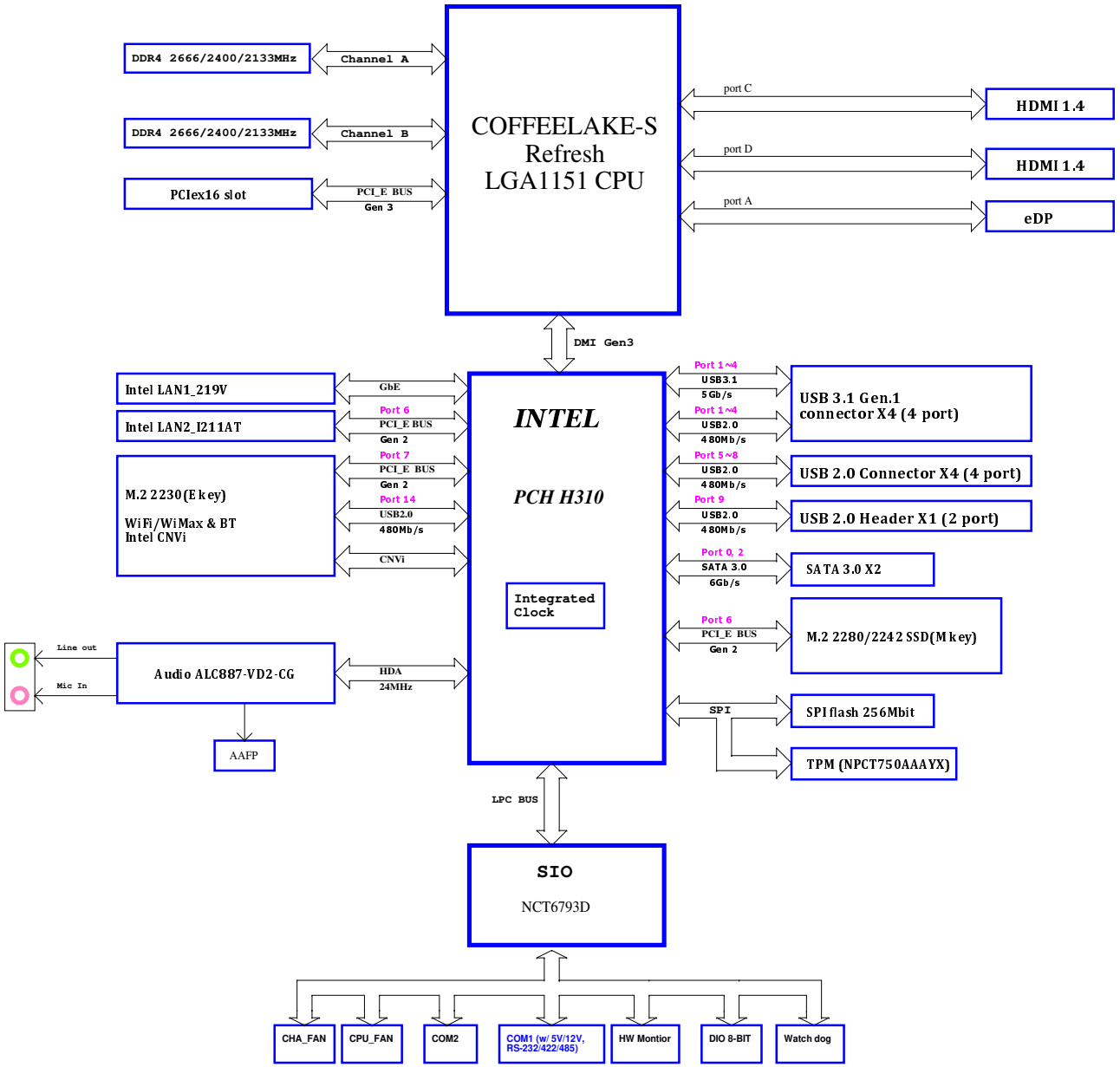
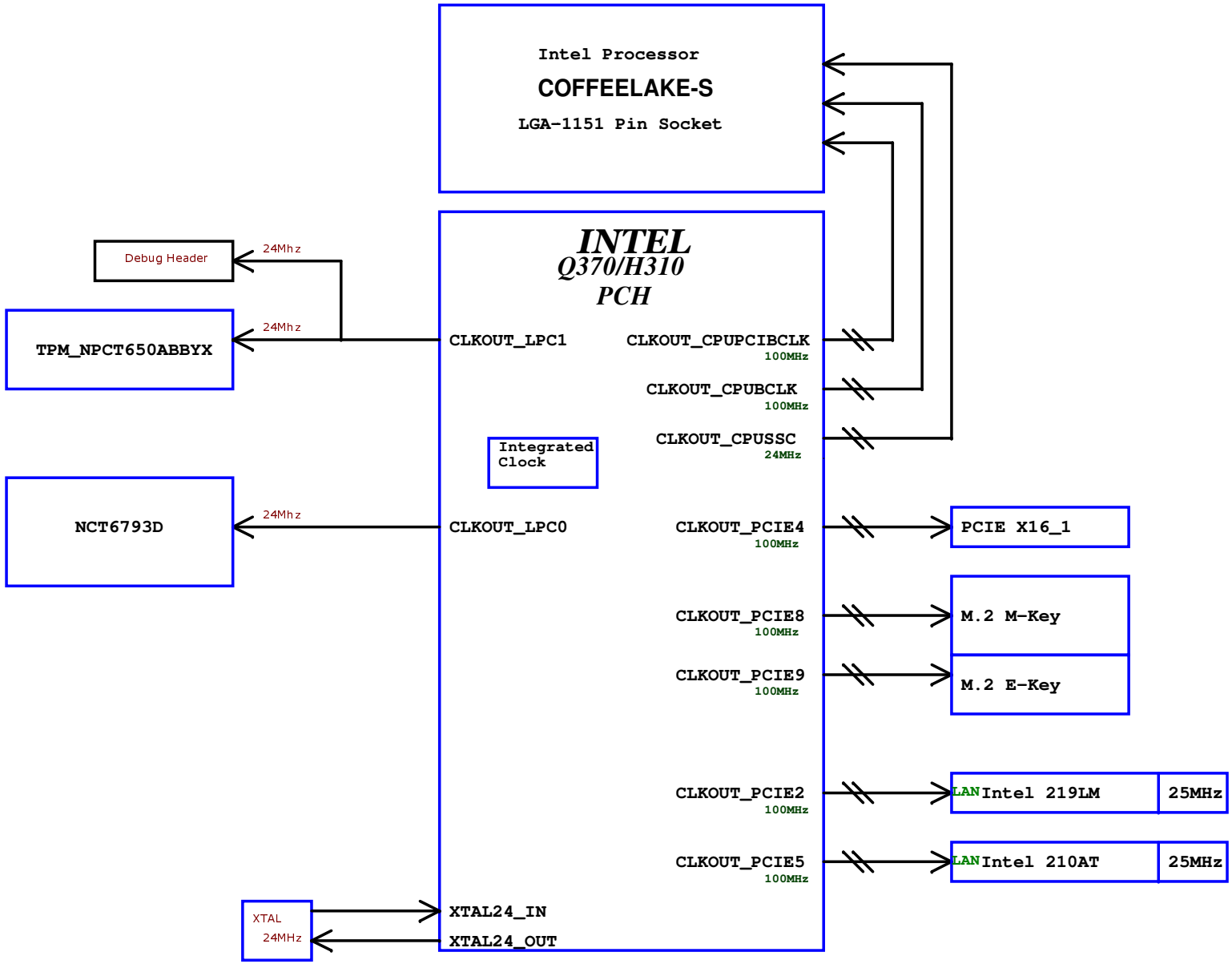
MIX-H310D2
Block diagram Rev 1.01



ASUSTeK COMPUTER INC.	Title : Block Diagram		
	Engineer: IPC-EE3		
Size A2	Project Name MIX-Q370D2		Rev 01.01
Date: Monday, February 17, 2020	Sheet 1 of 75		



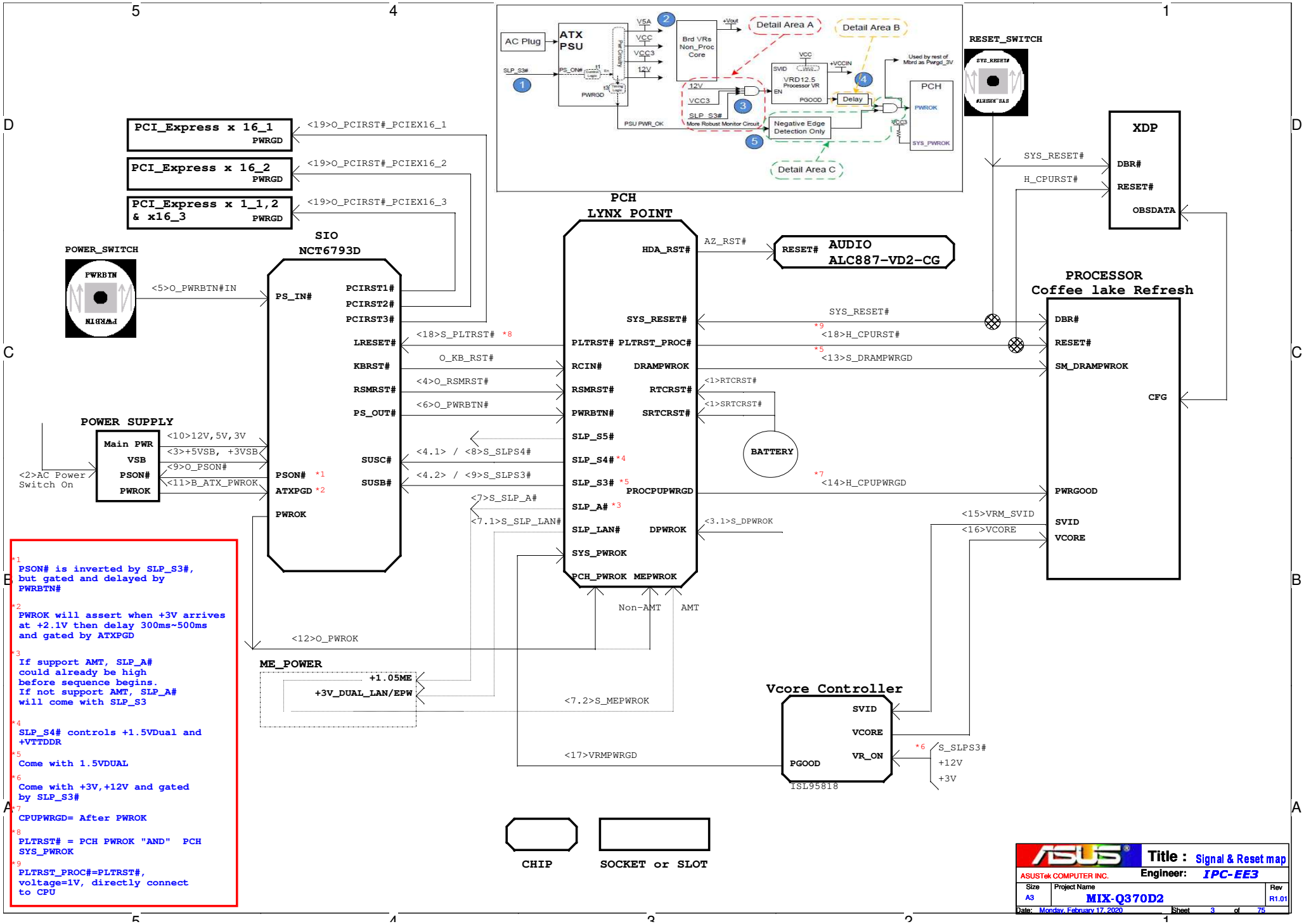
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: IPC-EE3

Size	Project Name	Rev
A3	MIX-Q370D2	R1.01

Date: Monday, February 17, 2020 Sheet 2 of 75



*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

*5 Come with 1.5VDUAL

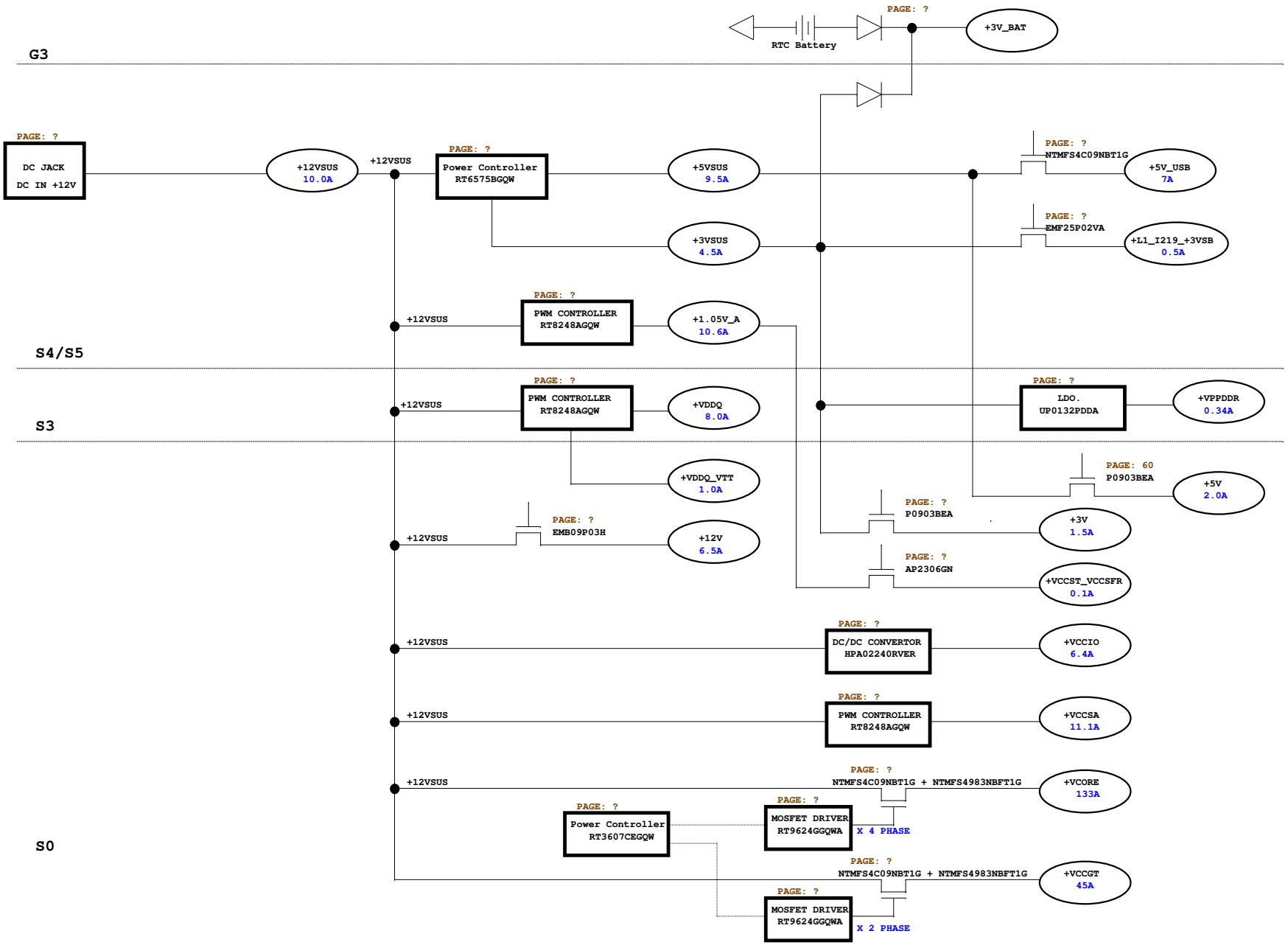
*6 Come with +3V,+12V and gated by SLP_S3#

*7 CPUPWRGD= After PWROK

*8 PLTRST# = PCH PWROK "AND" PCH SYS_PWROK

*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

ASUSTek COMPUTER INC.	Title : Signal & Reset map	
	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 3 of 75	



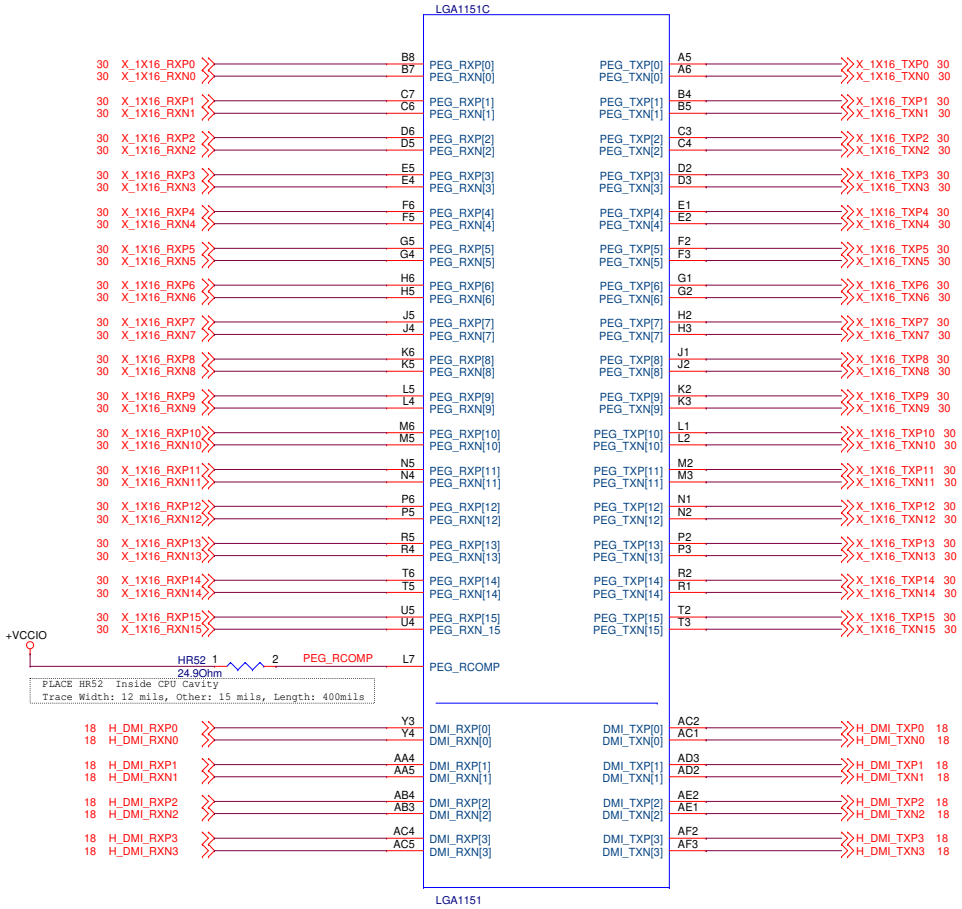
ASUSTeK COMPUTER INC.

Title : Power Flow

Engineer: IPC-EE3

Size	Project Name	Rev
Custom	MIX-Q370D2	R1.01

Date: Monday, February 17, 2020 Sheet 4 of 75



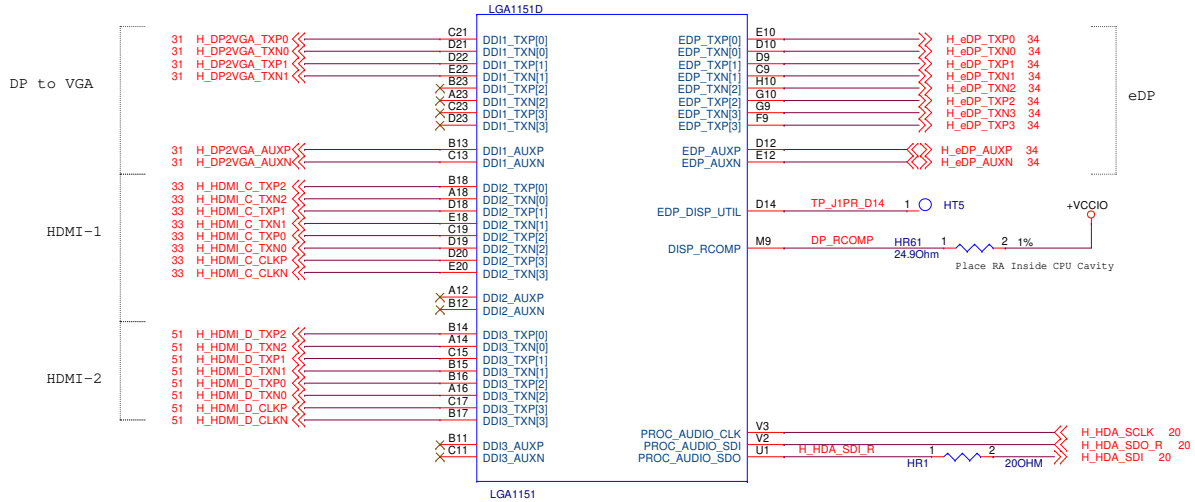
12001-00180200

LGA1151 LGA 1151P SOCKET 15U SMT

1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C

2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUS	Title : LGA1150 (DMI/PEG)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 5 of 75		



12001-00180200

LGA1151 LGA 1151P SOCKET 15U SMT

1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C

2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUSTek COMPUTER INC.	Title : LGA1150 (FDI/DISPLAY)	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 6 of 75		

Channel A
4 Layer routing

13 D4_DQ_A[0:63]

LGA1151A

D4_DQ_A1	AE38	DDR0_DQ[0]
D4_DQ_A5	AE37	DDR0_DQ[1]
D4_DQ_A7	AG38	DDR0_DQ[2]
D4_DQ_A3	AG37	DDR0_DQ[3]
D4_DQ_A0	AE39	DDR0_DQ[4]
D4_DQ_A4	AE40	DDR0_DQ[5]
D4_DQ_A6	AG39	DDR0_DQ[6]
D4_DQ_A2	AG40	DDR0_DQ[7]
D4_DQ_A12	AJ38	DDR0_DQ[8]
D4_DQ_A9	AJ37	DDR0_DQ[9]
D4_DQ_A10	AL38	DDR0_DQ[10]
D4_DQ_A11	AL37	DDR0_DQ[11]
D4_DQ_A13	AJ40	DDR0_DQ[12]
D4_DQ_A8	AJ39	DDR0_DQ[13]
D4_DQ_A14	AL39	DDR0_DQ[14]
D4_DQ_A15	AL40	DDR0_DQ[15]
D4_DQ_A17	AN38	DDR0_DQ[16]/DDR0_DQ[32]
D4_DQ_A20	AN40	DDR0_DQ[17]/DDR0_DQ[33]
D4_DQ_A19	AR38	DDR0_DQ[18]/DDR0_DQ[34]
D4_DQ_A18	AR37	DDR0_DQ[19]/DDR0_DQ[35]
D4_DQ_A21	AN39	DDR0_DQ[20]/DDR0_DQ[36]
D4_DQ_A16	AN37	DDR0_DQ[21]/DDR0_DQ[37]
D4_DQ_A22	AR39	DDR0_DQ[22]/DDR0_DQ[38]
D4_DQ_A23	AR40	DDR0_DQ[23]/DDR0_DQ[39]
D4_DQ_A24	AW37	DDR0_DQ[24]/DDR0_DQ[40]
D4_DQ_A29	AU38	DDR0_DQ[25]/DDR0_DQ[41]
D4_DQ_A31	AV35	DDR0_DQ[26]/DDR0_DQ[42]
D4_DQ_A30	AW35	DDR0_DQ[27]/DDR0_DQ[43]
D4_DQ_A28	AU37	DDR0_DQ[28]/DDR0_DQ[44]
D4_DQ_A25	AV37	DDR0_DQ[29]/DDR0_DQ[45]
D4_DQ_A27	AT35	DDR0_DQ[30]/DDR0_DQ[46]
D4_DQ_A26	AU35	DDR0_DQ[31]/DDR0_DQ[47]
D4_DQ_A33	AY8	DDR0_DQ[32]/DDR1_DQ[0]
D4_DQ_A32	AW8	DDR0_DQ[33]/DDR1_DQ[1]
D4_DQ_A39	AV6	DDR0_DQ[34]/DDR1_DQ[2]
D4_DQ_A34	AU6	DDR0_DQ[35]/DDR1_DQ[3]
D4_DQ_A37	AU8	DDR0_DQ[36]/DDR1_DQ[4]
D4_DQ_A36	AV8	DDR0_DQ[37]/DDR1_DQ[5]
D4_DQ_A35	AW6	DDR0_DQ[38]/DDR1_DQ[6]
D4_DQ_A38	AY6	DDR0_DQ[39]/DDR1_DQ[7]
D4_DQ_A45	AY4	DDR0_DQ[40]/DDR1_DQ[8]
D4_DQ_A40	AV4	DDR0_DQ[41]/DDR1_DQ[9]
D4_DQ_A42	AT1	DDR0_DQ[42]/DDR1_DQ[10]
D4_DQ_A43	AT2	DDR0_DQ[43]/DDR1_DQ[11]
D4_DQ_A41	AV3	DDR0_DQ[44]/DDR1_DQ[12]
D4_DQ_A44	AW4	DDR0_DQ[45]/DDR1_DQ[13]
D4_DQ_A46	AT4	DDR0_DQ[46]/DDR1_DQ[14]
D4_DQ_A47	AT3	DDR0_DQ[47]/DDR1_DQ[15]
D4_DQ_A53	AP2	DDR0_DQ[48]/DDR1_DQ[32]
D4_DQ_A51	AM4	DDR0_DQ[49]/DDR1_DQ[33]
D4_DQ_A49	AP3	DDR0_DQ[50]/DDR1_DQ[34]
D4_DQ_A55	AM3	DDR0_DQ[51]/DDR1_DQ[35]
D4_DQ_A52	AP4	DDR0_DQ[52]/DDR1_DQ[36]
D4_DQ_A54	AM2	DDR0_DQ[53]/DDR1_DQ[37]
D4_DQ_A48	AP1	DDR0_DQ[54]/DDR1_DQ[38]
D4_DQ_A50	AM1	DDR0_DQ[55]/DDR1_DQ[39]
D4_DQ_A61	AK3	DDR0_DQ[56]/DDR1_DQ[40]
D4_DQ_A62	AH1	DDR0_DQ[57]/DDR1_DQ[41]
D4_DQ_A56	AK4	DDR0_DQ[58]/DDR1_DQ[42]
D4_DQ_A63	AH2	DDR0_DQ[59]/DDR1_DQ[43]
D4_DQ_A59	AH4	DDR0_DQ[60]/DDR1_DQ[44]
D4_DQ_A60	AK2	DDR0_DQ[61]/DDR1_DQ[45]
D4_DQ_A58	AH3	DDR0_DQ[62]/DDR1_DQ[46]
D4_DQ_A57	AK1	DDR0_DQ[63]/DDR1_DQ[47]

Only support Non-ECC

AU33		DDR0_ECC[0]
AT33		DDR0_ECC[1]
AW33		DDR0_ECC[2]
AV31		DDR0_ECC[3]
AU31		DDR0_ECC[4]
AV33		DDR0_ECC[5]
AW31		DDR0_ECC[6]
AY31		DDR0_ECC[7]

DDR0_CKP[0]	AW18		D4_MA_CLKP0 13
DDR0_CKN[0]	AV18		D4_MA_CLKN0 13
DDR0_CKP[1]	AW17		D4_MA_CLKP1 13
DDR0_CKN[1]	AY17		D4_MA_CLKN1 13
DDR0_CKP[2]	AW16		
DDR0_CKN[2]	AV16		
DDR0_CKP[3]	AT16		
DDR0_CKN[3]	AU16		
DDR0_CKE[0]	AY24		D4_CKE_A0 13
DDR0_CKE[1]	AW24		D4_CKE_A1 13
DDR0_CKE[2]	AV24		
DDR0_CKE[3]	AV25		
DDR0_CS#[0]	AW12		D4_CS_A#0 13
DDR0_CS#[1]	AU11		D4_CS_A#1 13
DDR0_CS#[2]	AV13		
DDR0_CS#[3]	AV10		
DDR0_ODT[0]	AW11		D4_ODT_A0 13
DDR0_ODT[1]	AU14		D4_ODT_A1 13
DDR0_ODT[2]	AU12		
DDR0_ODT[3]	AY10		
DDR0_BA[0]	AY13		D4_BAA0 13
DDR0_BA[1]	AV15		D4_BAA1 13
DDR0_BG[0]	AW23		D4_BGA0 13
DDR0_MA[16]	AW13	D4_MAA16	D4_MAA[0:16] 13
DDR0_MA[14]	AV14	D4_MAA14	
DDR0_MA[15]	AY11	D4_MAA15	
DDR0_MA[0]	AW15	D4_MAA0	
DDR0_MA[1]	AU18	D4_MAA1	
DDR0_MA[2]	AU17	D4_MAA2	
DDR0_MA[3]	AV19	D4_MAA3	
DDR0_MA[4]	AT19	D4_MAA4	
DDR0_MA[5]	AU20	D4_MAA5	
DDR0_MA[6]	AV20	D4_MAA6	
DDR0_MA[7]	AU21	D4_MAA7	
DDR0_MA[8]	AT20	D4_MAA8	
DDR0_MA[9]	AT22	D4_MAA9	
DDR0_MA[10]	AY14	D4_MAA10	
DDR0_MA[11]	AU22	D4_MAA11	
DDR0_MA[12]	AV22	D4_MAA12	
DDR0_MA[13]	AV12	D4_MAA13	
DDR0_BG[1]	AV23		D4_BGA1 13
DDR0_ACT#	AU24		D4_A_ACT# 13
DDR0_PAR	AY15		D4_A_PAR 13
DDR0_ALERT#	AT23		D4_A_ALERT# 13
DDR0_DQSN[0]	AF39		D4_DQS_A_DN0 13
DDR0_DQSN[1]	AK39		D4_DQS_A_DN1 13
DDR0_DQSN[2]/DDR0_DQSN[4]	AP39		D4_DQS_A_DN2 13
DDR0_DQSN[3]/DDR0_DQSN[5]	AU36		D4_DQS_A_DN3 13
DDR0_DQSN[4]/DDR1_DQSN[0]	AW7		D4_DQS_A_DN4 13
DDR0_DQSN[5]/DDR1_DQSN[1]	AU3		D4_DQS_A_DN5 13
DDR0_DQSN[6]/DDR1_DQSN[4]	AN3		D4_DQS_A_DN6 13
DDR0_DQSN[7]/DDR1_DQSN[5]	AJ3		D4_DQS_A_DN7 13
DDR0_DQSP[0]	AF38		D4_DQS_A_DP0 13
DDR0_DQSP[1]	AK38		D4_DQS_A_DP1 13
DDR0_DQSP[2]/DDR0_DQSP[4]	AP38		D4_DQS_A_DP2 13
DDR0_DQSP[3]/DDR0_DQSP[5]	AV36		D4_DQS_A_DP3 13
DDR0_DQSP[4]/DDR1_DQSP[0]	AV7		D4_DQS_A_DP4 13
DDR0_DQSP[5]/DDR1_DQSP[1]	AU2		D4_DQS_A_DP5 13
DDR0_DQSP[6]/DDR1_DQSP[4]	AN2		D4_DQS_A_DP6 13
DDR0_DQSP[7]/DDR1_DQSP[5]	AJ2		D4_DQS_A_DP7 13
DDR0_DQSP[8]	AV32		
DDR0_DQSN[8]	AU32		

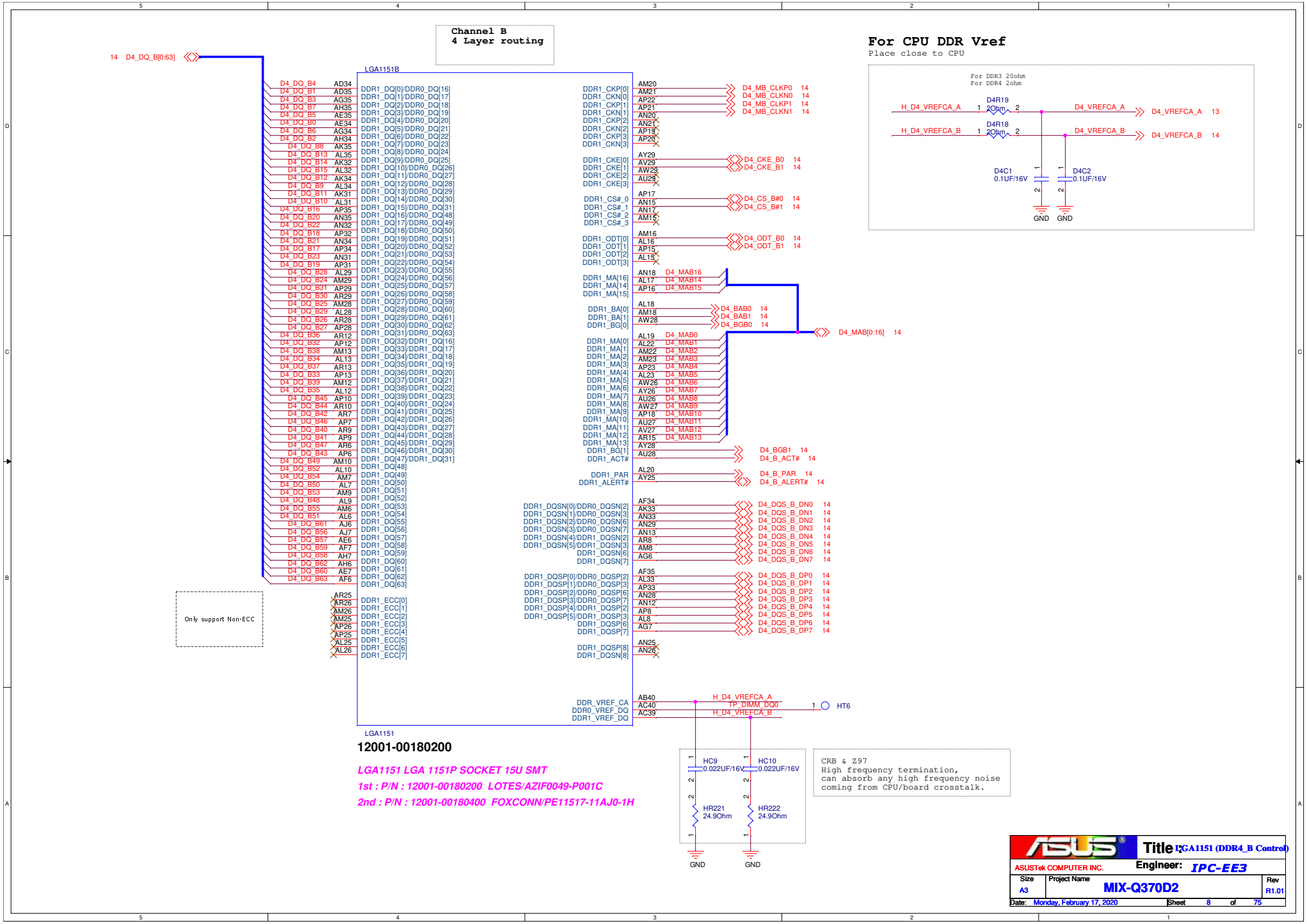
Only support Non-ECC

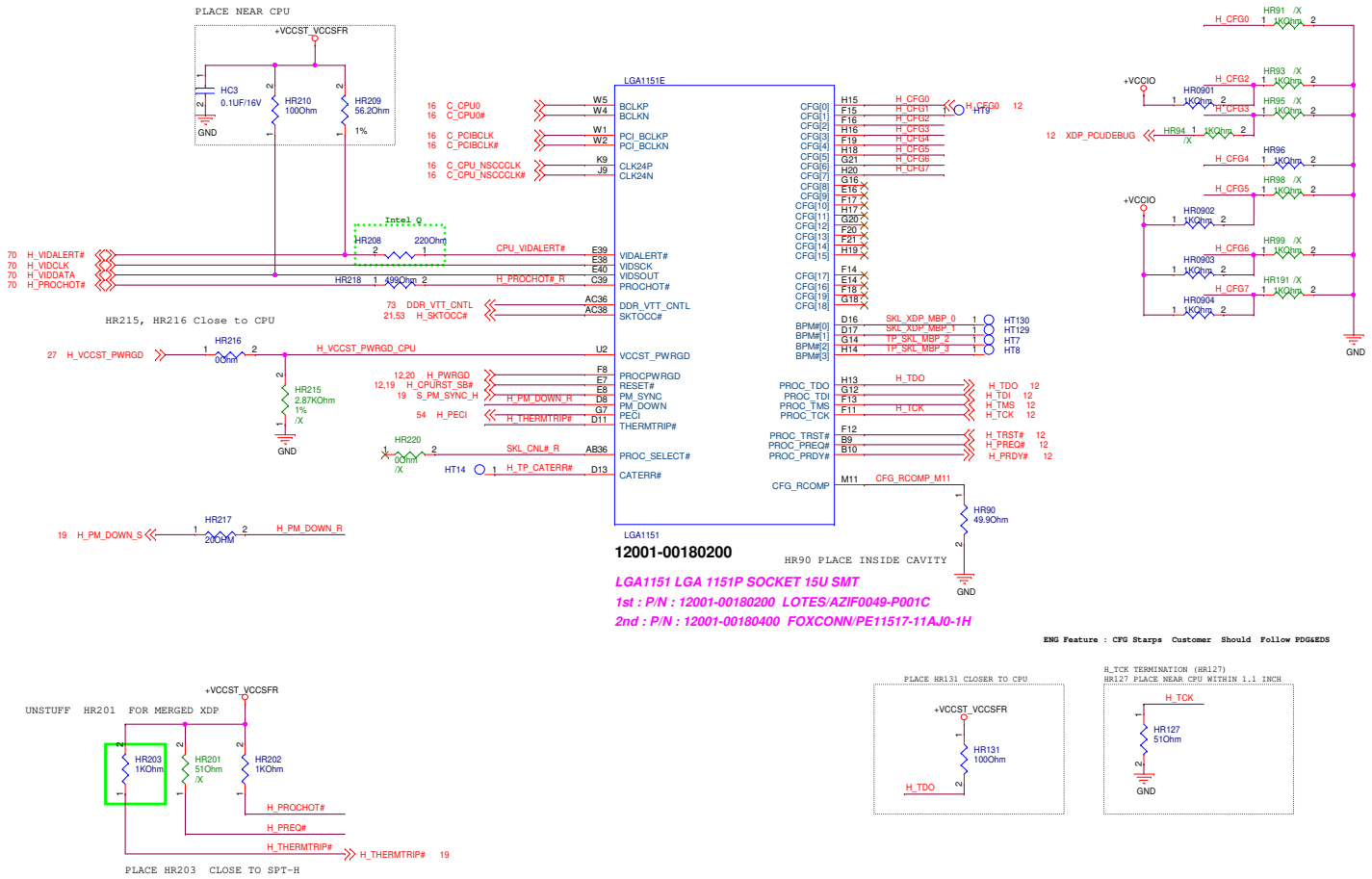
LGA1151

12001-00180200

LGA1151 LGA 1151P SOCKET 15U SMT
1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C
2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

ASUSTek COMPUTER INC.	Title: LGA1151 (DDR4_A Control)	Engineer: IPC-EE3
Size: A3	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 7 of 75	


Channel B
4 Layer routing
For CPU DDR Vref
Place close to CPU
For DDR3 20ohm
For DDR4 2ohm
D4R19 20hm
D4R18 20hm
H_D4_VREFCA_A
H_D4_VREFCA_B
D4_VREFCA_A
D4_VREFCA_B
D4C1 0.1UF/16V
D4C2 0.1UF/16V
GND
14 D4_DQ_B[0:63]
LGA1151B
LGA1151
Only support Non-ECC
D4_MAB[0:16] 14
HT6
TP_DIMM_DQ0
HC9 0.022UF/16V
HC10 0.022UF/16V
HR221 24.9Ohm
HR222 24.9Ohm
CRB & Z97
High frequency termination,
can absorb any high frequency noise
coming from CPU/board crosstalk.
12001-00180200
LGA1151 LGA 1151P SOCKET 15U SMT
1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C
2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H
ASUS
ASUSTek COMPUTER INC.
Title: LGA1151 (DDR4_B Control)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 8 of 75



CFG Straps for Processor

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane
Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes
Reserved Configuration Lane

CFG[4] : eDP Enable
- 1 : Disabled
- 0 : Enabled

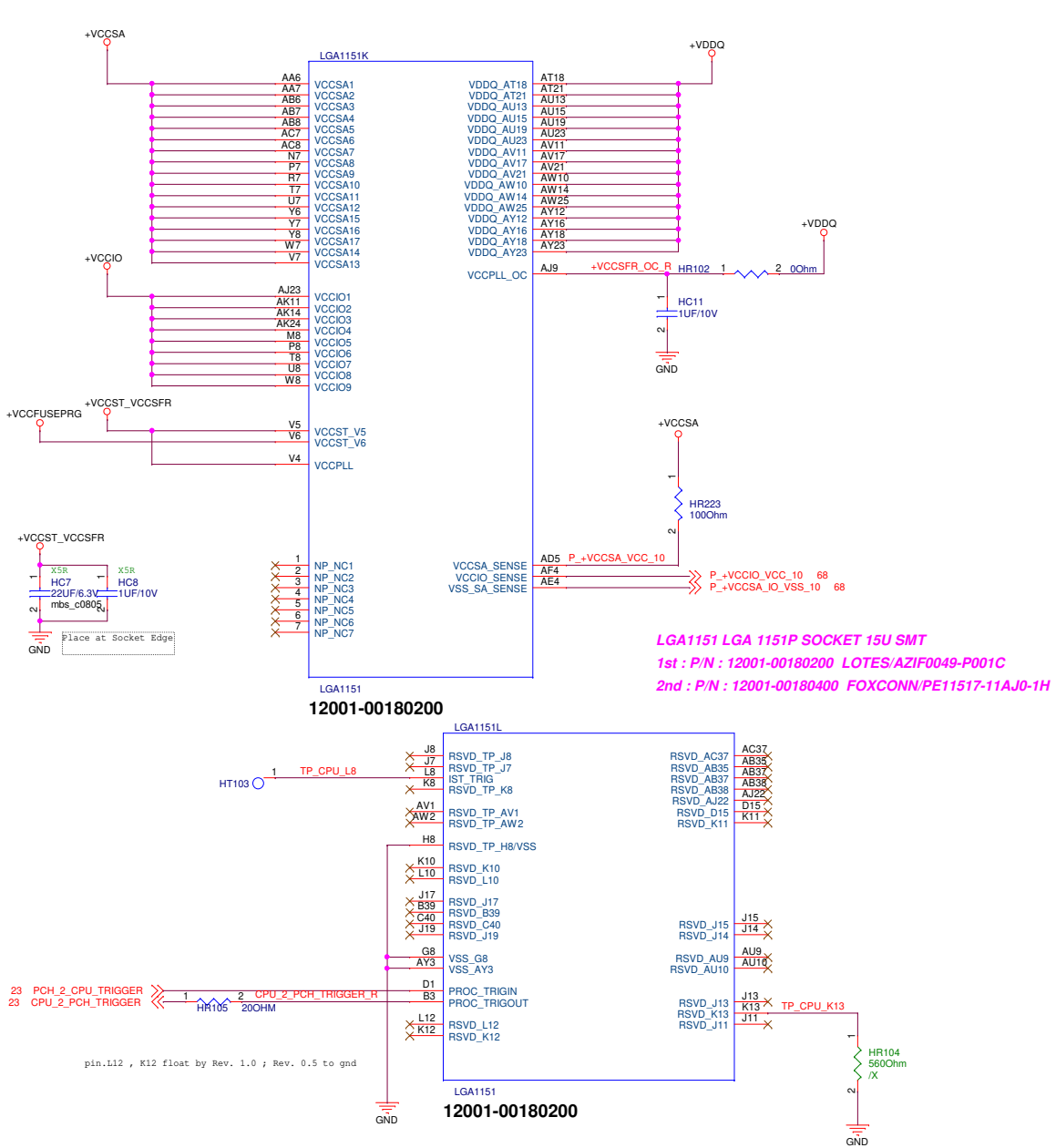
CFG[6:5] : PCI Expres* Bifurcation
- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes
Reserved Configuration Lanes

Refer : Intel 570805_CFL_EDS_Vol1_Rev1.1, Table 6-7, P.116

ASUSTek COMPUTER INC.	Title : LGA1151 (Control)	Engineer: IPC-EE3
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 9 of 75	

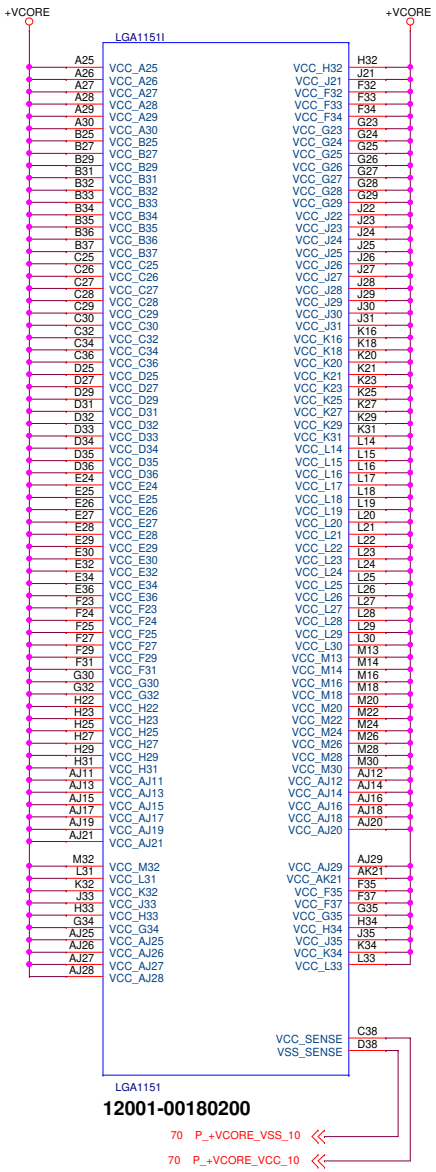


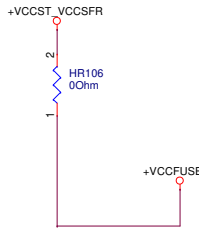
LGA1151 LGA 1151P SOCKET 15U SMT

1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C

2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

pin.L12 , K12 float by Rev. 1.0 ; Rev. 0.5 to gnd





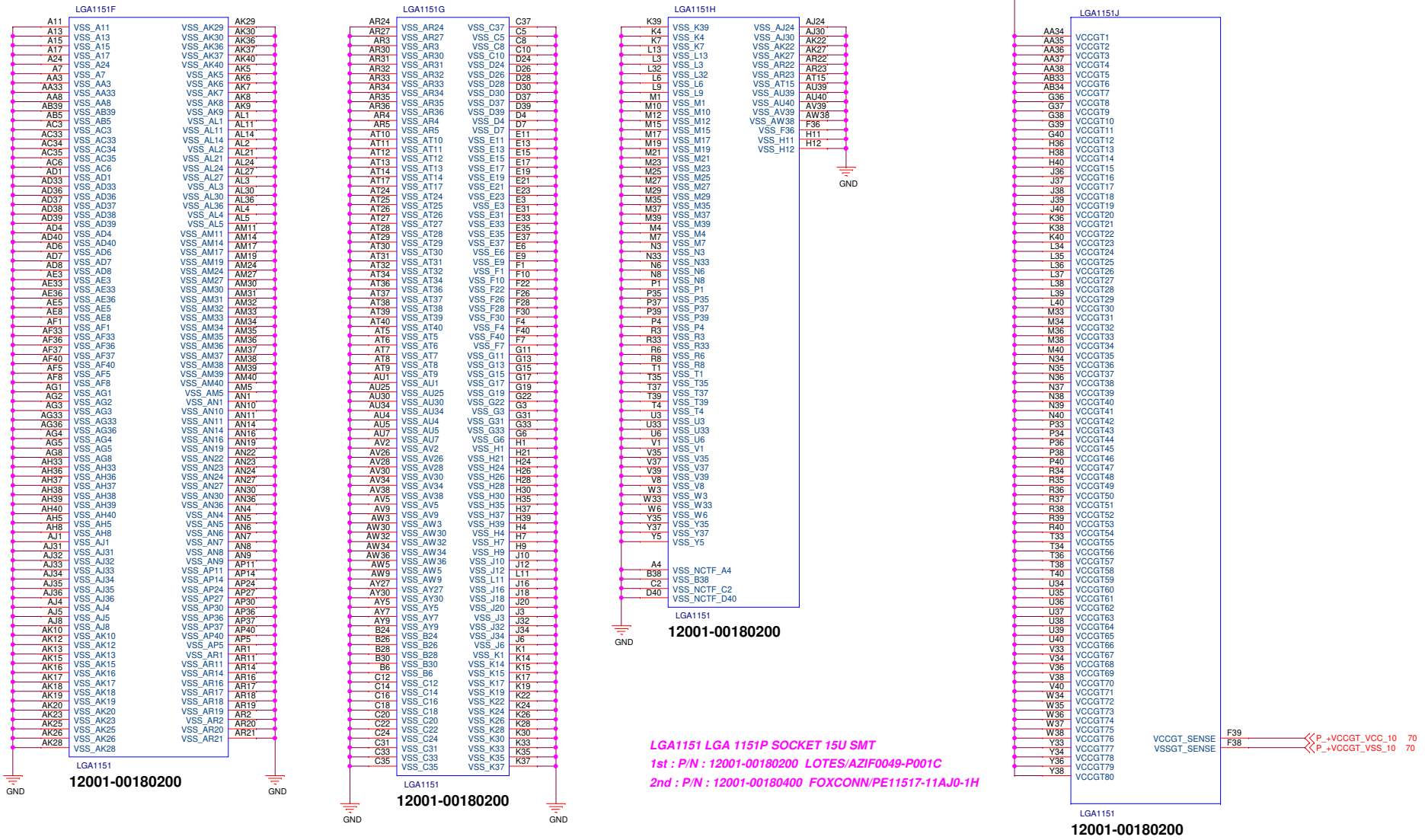
BOM NOTE: 1-2 : NO FUSING(DEFAULT)

BOM NOTE: STUFF HR110 FOR HASWELL (+VCORE)

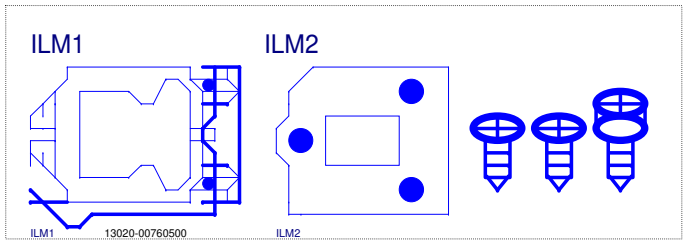
STUFF HR109 FOR SKL (+1.8V_A_EDRAM)

CAD NOTE: TRI PAD FOR THE TWO PU RESISTORS

ASUS	Title : LGA1150 (POWER)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 10 of 75		



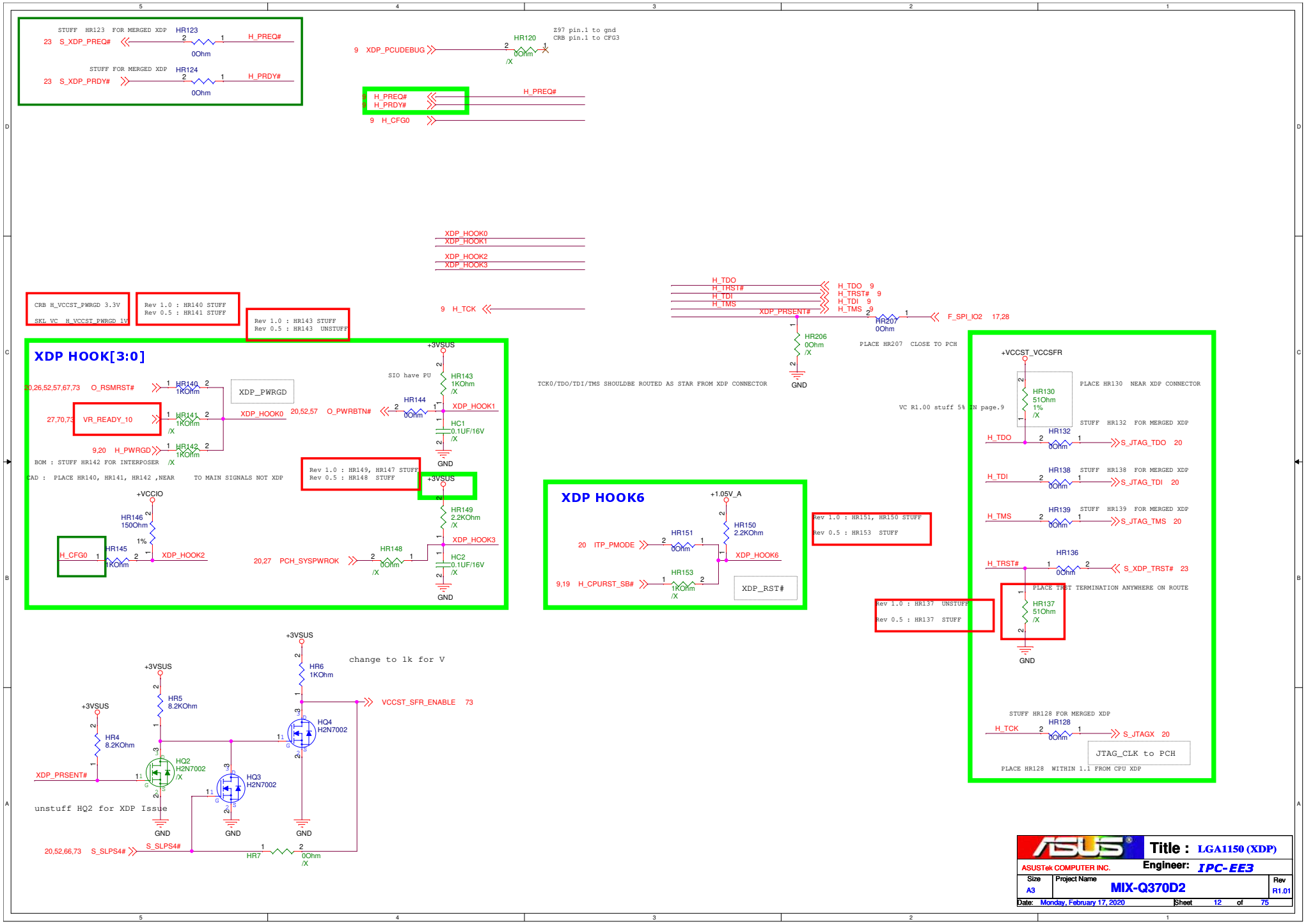
LGA1151 LGA 1151P SOCKET 15U SMT
1st : P/N : 12001-00180200 LOTES/AZIF0049-P001C
2nd : P/N : 12001-00180400 FOXCONN/PE11517-11AJ0-1H

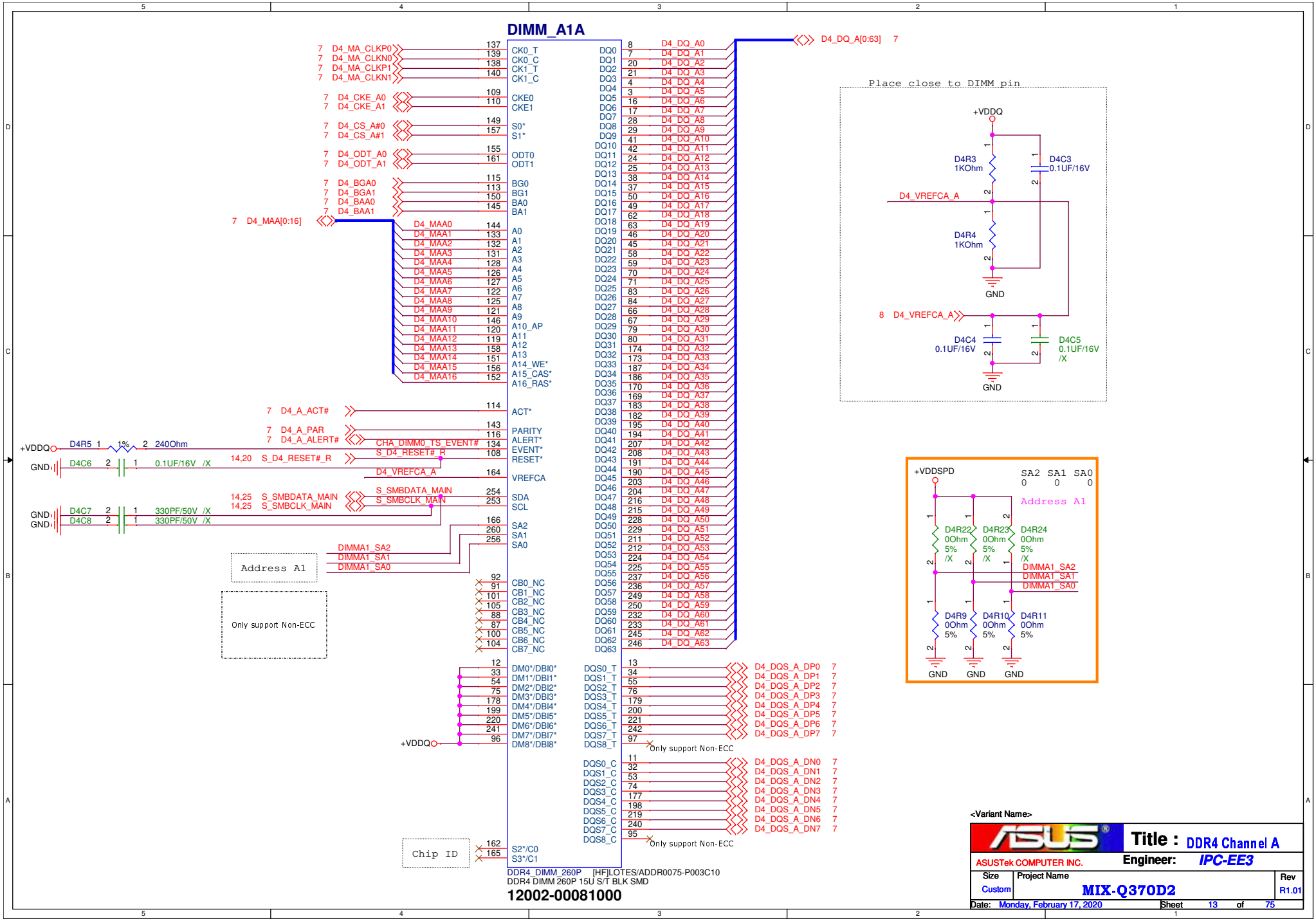


1. ILM + COVER P/N : 13020-00061900
2. BACKPLATE P/N : 13020-00062000 (替代料 13020-00061300)

各別加入 BOM 內, Location 皆為 ILM1 , ILM2

ASUS	Title : LGA1151 (GND)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 11 of 75		


STUFF HR123 FOR MERGED XDP
HR123
23 S_XDP_PREQ#
H_PREQ#
0Ohm
STUFF FOR MERGED XDP
HR124
23 S_XDP_PRDY#
H_PRDY#
0Ohm
9 XDP_PCUDEBUG
HR120
0Ohm
/X
Z97 pin.1 to gnd
CRB pin.1 to CFG3
H_PREQ#
H_PRDY#
9 H_CFG0
XDP_HOOK0
XDP_HOOK1
XDP_HOOK2
XDP_HOOK3
9 H_TCK
H_TDO
H_TRST#
H_TDI
H_TMS
XDP_PRSENT#
H_TDO 9
H_TRST# 9
H_TDI 9
H_TMS 9
HR207
0Ohm
F_SPI_IO2 17,28
HR206
0Ohm
/X
GND
PLACE HR207 CLOSE TO PCH
TCK0/TDO/TDI/TMS SHOULDBE ROUTED AS STAR FROM XDP CONNECTOR
CRB H_VCCST_PWRGD 3.3V
SKL VC H_VCCST_PWRGD 1V
Rev 1.0 : HR140 STUFF
Rev 0.5 : HR141 STUFF
Rev 1.0 : HR143 STUFF
Rev 0.5 : HR143 UNSTUFF
XDP HOOK[3:0]
+3VSUS
SIO have PU
HR143
1KOhm
/X
20,26,52,57,67,73 O_RSMRST#
HR140
1KOhm
XDP_PWRGD
HR144
0Ohm
XDP_HOOK1
27,70,73 VR_READY_10
HR141
1KOhm
/X
XDP_HOOK0
20,52,57 O_PWRBTN#
HC1
0.1UF/16V
/X
9,20 H_PWRGD
HR142
1KOhm
/X
GND
BOM : STUFF HR142 FOR INTERPOSER
CAD : PLACE HR140, HR141, HR142 ,NEAR TO MAIN SIGNALS NOT XDP
Rev 1.0 : HR149, HR147 STUFF
Rev 0.5 : HR148 STUFF
+3VSUS
+VCCIO
HR146
150Ohm
1%
HR149
2.2KOhm
/X
H_CFG0
HR145
1KOhm
XDP_HOOK2
20,27 PCH_SYSPWROK
HR148
0Ohm
/X
XDP_HOOK3
HC2
0.1UF/16V
/X
GND
XDP HOOK6
+1.05V_A
HR151
0Ohm
HR150
2.2KOhm
20 ITP_PMODE
XDP_HOOK6
HR153
1KOhm
/X
9,19 H_CPURST_SB#
XDP_RST#
Rev 1.0 : HR151, HR150 STUFF
Rev 0.5 : HR153 STUFF
+VCCST_VCCSFR
HR130
51Ohm
1%
/X
PLACE HR130 NEAR XDP CONNECTOR
VC R1.00 stuff 5% IN page.9
STUFF HR132 FOR MERGED XDP
H_TDO
HR132
0Ohm
S_JTAG_TDO 20
H_TDI
HR138
0Ohm
STUFF HR138 FOR MERGED XDP
S_JTAG_TDI 20
H_TMS
HR139
0Ohm
STUFF HR139 FOR MERGED XDP
S_JTAG_TMS 20
HR136
H_TRST#
0Ohm
S_XDP_TRST# 23
PLACE TRST TERMINATION ANYWHERE ON ROUTE
HR137
51Ohm
/X
GND
Rev 1.0 : HR137 UNSTUFF
Rev 0.5 : HR137 STUFF
STUFF HR128 FOR MERGED XDP
H_TCK
HR128
0Ohm
S_JTAGX 20
JTAG_CLK to PCH
PLACE HR128 WITHIN 1.1 FROM CPU XDP
+3VSUS
HR6
1KOhm
change to 1k for V
VCCST_SFR_ENABLE 73
+3VSUS
HR5
8.2KOhm
HQ4
H2N7002
+3VSUS
HR4
8.2KOhm
HQ2
H2N7002
/X
XDP_PRSENT#
HQ3
H2N7002
unstuff HQ2 for XDP Issue
GND
GND
GND
20,52,66,73 S_SLPS4#
S_SLPS4#
HR7
0Ohm
/X
ASUS
Title : LGA1150 (XDP)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 12 of 75


DIMM_A1A
7 D4_MA_CLKP0
7 D4_MA_CLKN0
7 D4_MA_CLKP1
7 D4_MA_CLKN1
7 D4_CKE_A0
7 D4_CKE_A1
7 D4_CS_A#0
7 D4_CS_A#1
7 D4_ODT_A0
7 D4_ODT_A1
7 D4_BGA0
7 D4_BGA1
7 D4_BAA0
7 D4_BAA1
7 D4_MAA[0:16]
7 D4_A_ACT#
7 D4_A_PAR
7 D4_A_ALERT#
CHA_DIMM0_TS_EVENT#
14,20 S_D4_RESET#_R
D4_VREFCA_A
14,25 S_SMBDATA_MAIN
14,25 S_SMBCLK_MAIN
DIMMA1_SA2
DIMMA1_SA1
DIMMA1_SA0
+VDDQ
GND
D4R5 1% 240Ohm
D4C6 0.1UF/16V /X
D4C7 330PF/50V /X
D4C8 330PF/50V /X
Address A1
Only support Non-ECC
Chip ID
CK0_T
CK0_C
CK1_T
CK1_C
CKE0
CKE1
S0*
S1*
ODT0
ODT1
BG0
BG1
BA0
BA1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10_AP
A11
A12
A13
A14_WE*
A15_CAS*
A16_RAS*
ACT*
PARITY
ALERT*
EVENT*
RESET*
VREFCA
SDA
SCL
SA2
SA1
SA0
CB0_NC
CB1_NC
CB2_NC
CB3_NC
CB4_NC
CB5_NC
CB6_NC
CB7_NC
DM0*/DBI0*
DM1*/DBI1*
DM2*/DBI2*
DM3*/DBI3*
DM4*/DBI4*
DM5*/DBI5*
DM6*/DBI6*
DM7*/DBI7*
DM8*/DBI8*
DQS0_T
DQS1_T
DQS2_T
DQS3_T
DQS4_T
DQS5_T
DQS6_T
DQS7_T
DQS8_T
DQS0_C
DQS1_C
DQS2_C
DQS3_C
DQS4_C
DQS5_C
DQS6_C
DQS7_C
DQS8_C
S2*/C0
S3*/C1
D4_DQ_A[0:63] 7
D4_DQS_A_DP0 7
D4_DQS_A_DP1 7
D4_DQS_A_DP2 7
D4_DQS_A_DP3 7
D4_DQS_A_DP4 7
D4_DQS_A_DP5 7
D4_DQS_A_DP6 7
D4_DQS_A_DP7 7
D4_DQS_A_DN0 7
D4_DQS_A_DN1 7
D4_DQS_A_DN2 7
D4_DQS_A_DN3 7
D4_DQS_A_DN4 7
D4_DQS_A_DN5 7
D4_DQS_A_DN6 7
D4_DQS_A_DN7 7
DDR4_DIMM_260P [HF]LOTES/ADDR0075-P003C10
DDR4 DIMM 260P 15U S/T BLK SMD
12002-00081000
Place close to DIMM pin
+VDDQ
D4R3 1KOhm
D4C3 0.1UF/16V
D4_VREFCA_A
D4R4 1KOhm
GND
8 D4_VREFCA_A
D4C4 0.1UF/16V
D4C5 0.1UF/16V /X
+VDDSPD
SA2 SA1 SA0
0 0 0
Address A1
D4R22 0Ohm 5% /X
D4R23 0Ohm 5% /X
D4R24 0Ohm 5% /X
DIMMA1_SA2
DIMMA1_SA1
DIMMA1_SA0
D4R9 0Ohm 5%
D4R10 0Ohm 5%
D4R11 0Ohm 5%
GND GND GND
<Variant Name>
Title : DDR4 Channel A
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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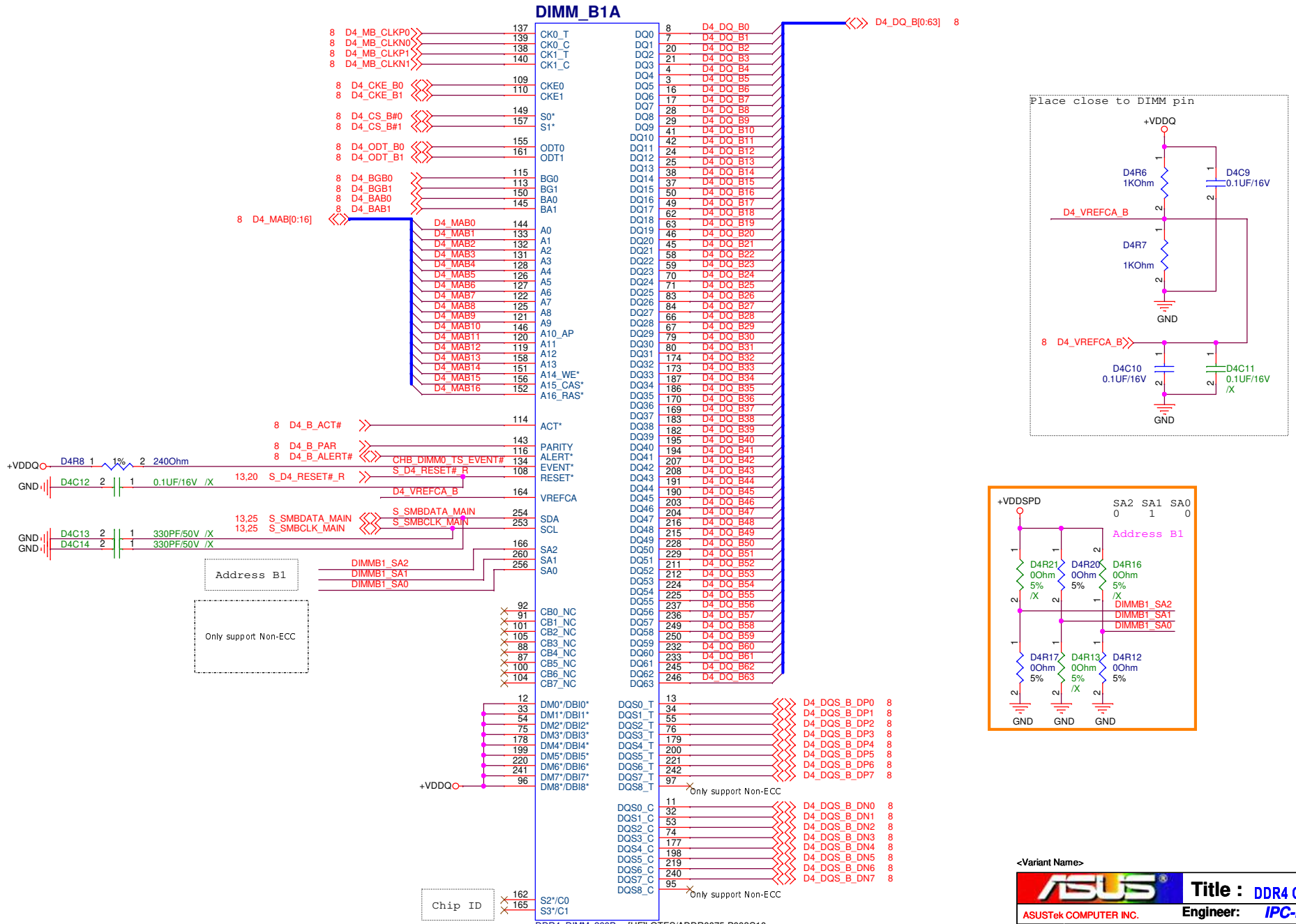
DIMM_B1A
8 D4_MB_CLKP0
8 D4_MB_CLKN0
8 D4_MB_CLKP1
8 D4_MB_CLKN1
8 D4_CKE_B0
8 D4_CKE_B1
8 D4_CS_B#0
8 D4_CS_B#1
8 D4_ODT_B0
8 D4_ODT_B1
8 D4_BGB0
8 D4_BGB1
8 D4_BAB0
8 D4_BAB1
8 D4_MAB[0:16]
8 D4_B_ACT#
8 D4_B_PAR
8 D4_B_ALERT#
+VDDQ
D4R8 1 1% 2 240Ohm
GND
D4C12 2 1 0.1UF/16V /X
13,20 S_D4_RESET#_R
CHB_DIMM0_TS_EVENT#
S_D4_RESET#_R
D4_VREFCA_B
S_SMBDATA_MAIN
S_SMBCLK_MAIN
13,25 S_SMBDATA_MAIN
13,25 S_SMBCLK_MAIN
GND
D4C13 2 1 330PF/50V /X
GND
D4C14 2 1 330PF/50V /X
Address B1
DIMMB1_SA2
DIMMB1_SA1
DIMMB1_SA0
Only support Non-ECC
+VDDQ
Chip ID
CK0_T
CK0_C
CK1_T
CK1_C
CKE0
CKE1
S0*
S1*
ODT0
ODT1
BG0
BG1
BA0
BA1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10_AP
A11
A12
A13
A14_WE*
A15_CAS*
A16_RAS*
ACT*
PARITY
ALERT*
EVENT*
RESET*
VREFCA
SDA
SCL
SA2
SA1
SA0
CB0_NC
CB1_NC
CB2_NC
CB3_NC
CB4_NC
CB5_NC
CB6_NC
CB7_NC
DM0*/DBI0*
DM1*/DBI1*
DM2*/DBI2*
DM3*/DBI3*
DM4*/DBI4*
DM5*/DBI5*
DM6*/DBI6*
DM7*/DBI7*
DM8*/DBI8*
S2*/C0
S3*/C1
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63
D4_DQ_B[0:63] 8
D4_DQS_B_DP0 8
D4_DQS_B_DP1 8
D4_DQS_B_DP2 8
D4_DQS_B_DP3 8
D4_DQS_B_DP4 8
D4_DQS_B_DP5 8
D4_DQS_B_DP6 8
D4_DQS_B_DP7 8
Only support Non-ECC
D4_DQS_B_DN0 8
D4_DQS_B_DN1 8
D4_DQS_B_DN2 8
D4_DQS_B_DN3 8
D4_DQS_B_DN4 8
D4_DQS_B_DN5 8
D4_DQS_B_DN6 8
D4_DQS_B_DN7 8
Only support Non-ECC
DDR4_DIMM_260P [HF]LOTES/ADDR0075-P003C10
DDR4 DIMM 260P 15U S/T BLK SMD
12002-00081000
Place close to DIMM pin
+VDDQ
D4R6 1KOhm
D4C9 0.1UF/16V
D4_VREFCA_B
D4R7 1KOhm
GND
8 D4_VREFCA_B
D4C10 0.1UF/16V
D4C11 0.1UF/16V /X
GND
+VDDSPD
SA2 SA1 SA0
0 1 0
Address B1
D4R21 0Ohm 5% /X
D4R20 0Ohm 5%
D4R16 0Ohm 5% /X
DIMMB1_SA2
DIMMB1_SA1
DIMMB1_SA0
D4R17 0Ohm 5%
D4R13 0Ohm 5% /X
D4R12 0Ohm 5%
GND GND GND
<Variant Name>
Title : DDR4 Channel B
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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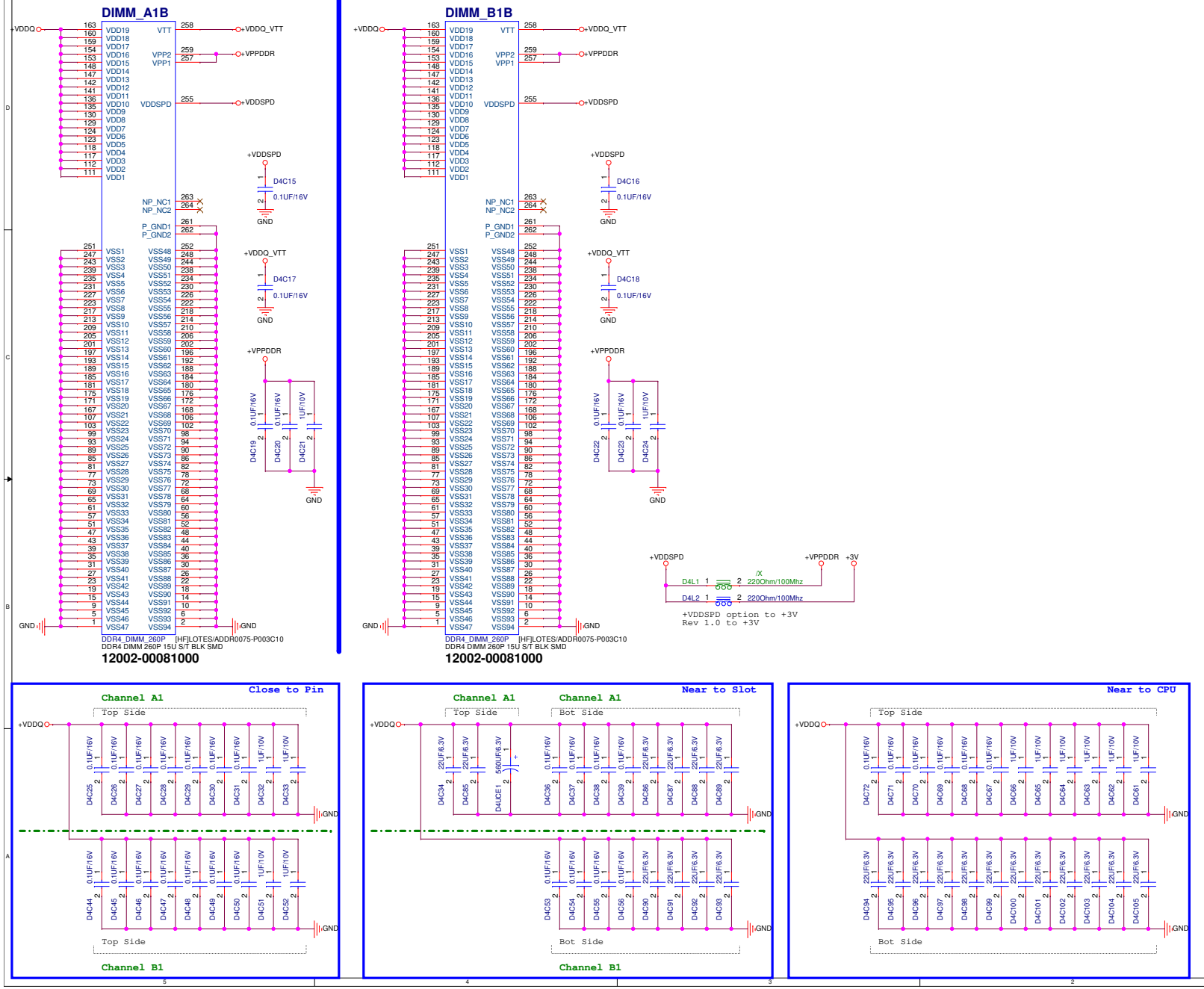


<Variant Name>

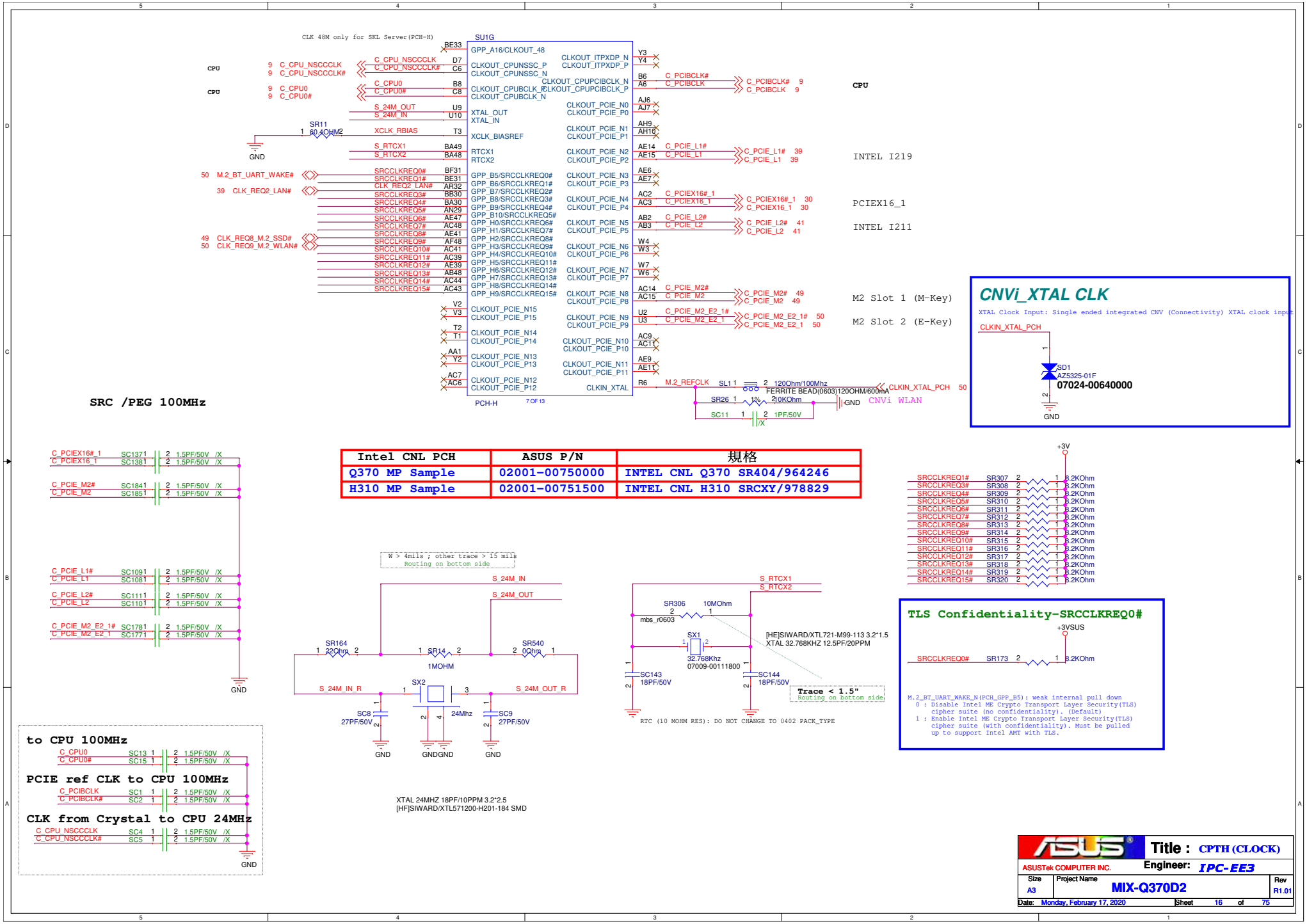
ASUSTek COMPUTER INC.

Title : DDR4 (Power)

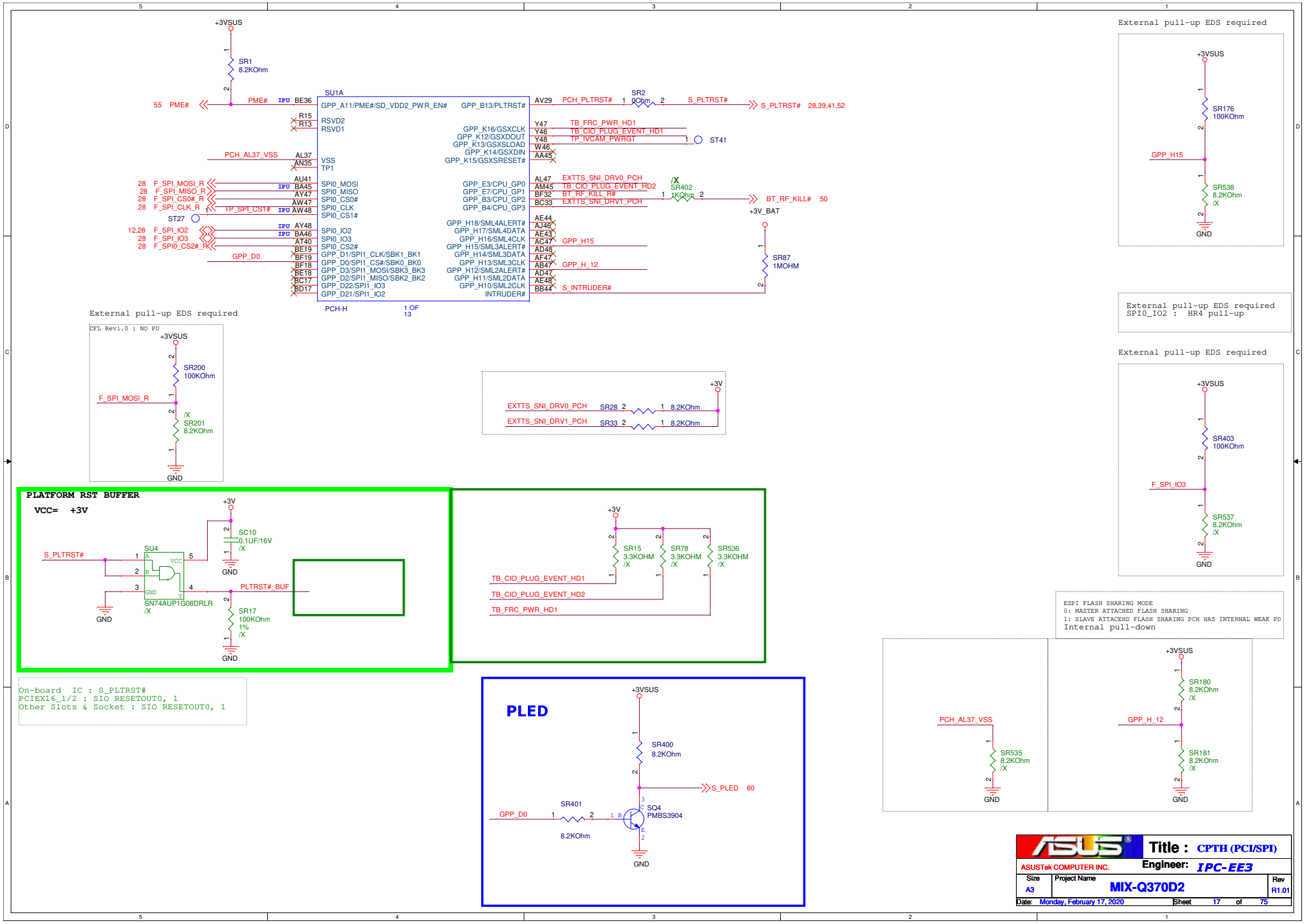
Engineer: IPC-EE3

Size	Project Name	Rev
Custom	MIX-Q370D2	R1.01

Date: Monday, February 17, 2020 Sheet 15 of 75



Intel CNL PCH	ASUS P/N	規格
Q370 MP Sample	02001-00750000	INTEL CNL Q370 SR404/964246
H310 MP Sample	02001-00751500	INTEL CNL H310 SRCXY/978829


+3VSUS
SR1
8.2KOhm
55 PME#
PME# IPU BE36
SU1A
GPP_A11/PME#/SD_VDD2_PWR_EN#
GPP_B13/PLTRST#
AV29 PCH_PLTRST# SR2 0Ohm S_PLTRST#
S_PLTRST# 28,39,41,52
R15
R13
RSVD2
RSVD1
GPP_K16/GSXCLK
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
Y47 TB_FRC_PWR_HD1
Y46 TB_CIO_PLUG_EVENT_HD1
Y48 TP_IVCAM_PWRGT
ST41
W46
AA45
PCH_AL37_VSS AL37
AN35
VSS
TP1
28 F_SPI_MOSI_R AU41 SPI0_MOSI
28 F_SPI_MISO_R IPU BA45 SPI0_MISO
28 F_SPI_CS0#_R AY47 SPI0_CS0#
28 F_SPI_CLK_R AW47 SPI0_CLK
TP_SPI_CST# IPU AW48 SPI0_CS1#
ST27
12,28 F_SPI_IO2 IPU AY48 SPI0_IO2
28 F_SPI_IO3 IPU BA46 SPI0_IO3
28 F_SPI0_CS2#_R AT40 SPI0_CS2#
GPP_D0 BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2
PCH-H
1 OF 13
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
AL47 EXTTS_SNI_DRV0_PCH
AM45 TB_CIO_PLUG_EVENT_HD2
BF32 BT_RF_KILL_R#
BC33 EXTTS_SNI_DRV1_PCH
/X SR402 1KOhm
BT_RF_KILL# 50
+3V_BAT
AE44
AJ46
AE43
AC47 GPP_H15
AD48
AF47
AB47 GPP_H_12
AD47
AE48
BB44 S_INTRUDER#
SR87 1MOHM
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
External pull-up EDS required
+3VSUS
SR176 100KOhm
GPP_H15
SR538 8.2KOhm /X
GND
External pull-up EDS required
SPI0_IO2 : HR4 pull-up
External pull-up EDS required
CFL Rev1.0 : NO PU
+3VSUS
SR200 100KOhm
F_SPI_MOSI_R
/X SR201 8.2KOhm
GND
+3V
EXTTS_SNI_DRV0_PCH SR28 8.2KOhm
EXTTS_SNI_DRV1_PCH SR33 8.2KOhm
External pull-up EDS required
+3VSUS
SR403 100KOhm
F_SPI_IO3
SR537 8.2KOhm /X
GND
PLATFORM RST BUFFER
VCC= +3V
+3V
SC10 0.1UF/16V /X
S_PLTRST#
SU4
SN74AUP1G08DRLR /X
PLTRST#_BUF
SR17 100KOhm 1% /X
GND
+3V
SR15 3.3KOHM /X
SR78 3.3KOHM /X
SR536 3.3KOHM /X
TB_CIO_PLUG_EVENT_HD1
TB_CIO_PLUG_EVENT_HD2
TB_FRC_PWR_HD1
ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1: SLAVE ATTACHED FLASH SHARING PCH HAS INTERNAL WEAK PD
Internal pull-down
On-board IC : S_PLTRST#
PCIEX16_1/2 : SIO RESETOUT0, 1
Other Slots & Socket : SIO RESETOUT0, 1
PLED
+3VSUS
SR400 8.2KOhm
S_PLED 60
SR401 8.2KOhm
GPP_D0
SQ4 PMBS3904
GND
PCH_AL37_VSS
SR535 8.2KOhm /X
GND
+3VSUS
SR180 8.2KOhm /X
GPP_H_12
SR181 8.2KOhm /X
GND
ASUSTek COMPUTER INC.
Title : CPTH (PCI/SPI)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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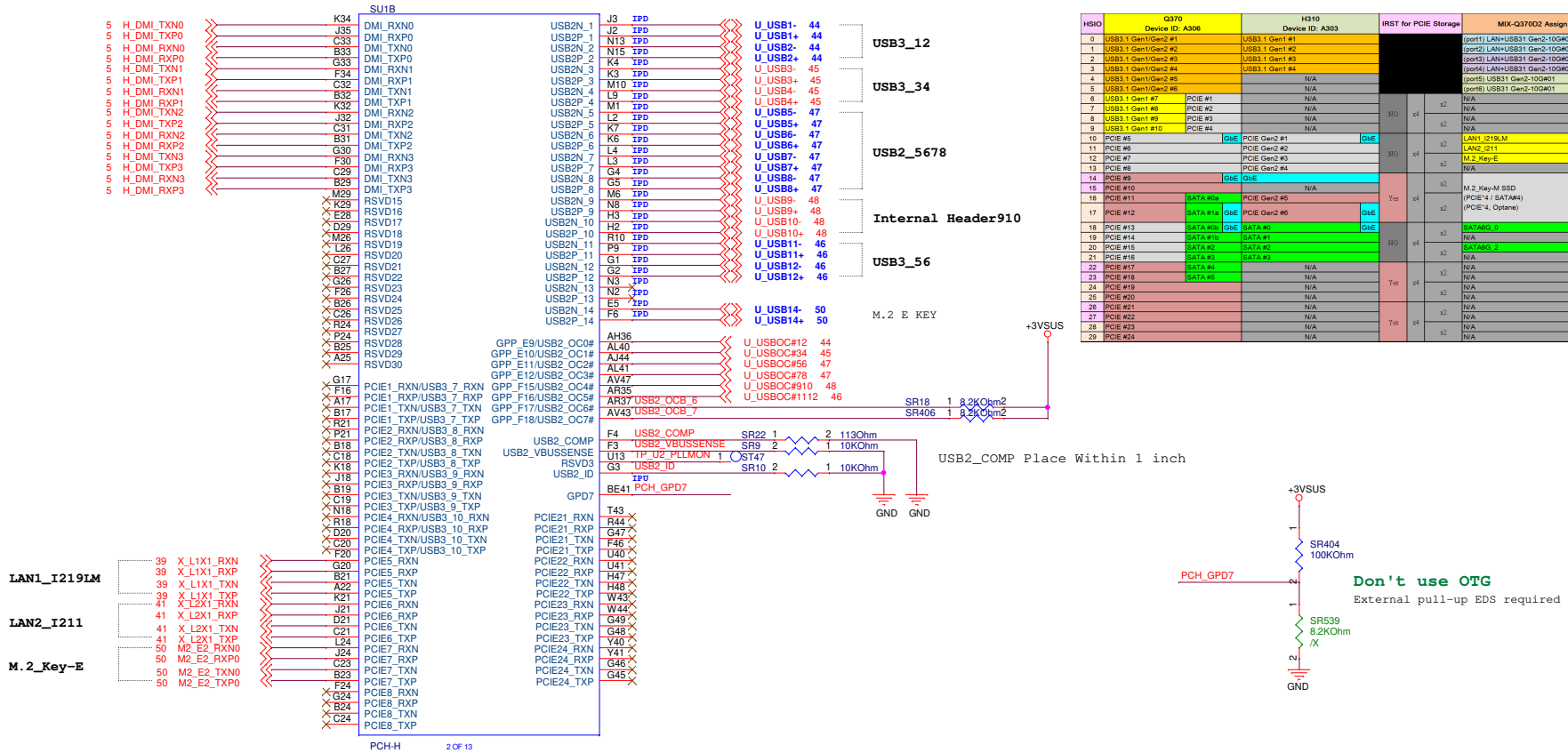


HSIO	Q370 Device ID: A306		H310 Device ID: A303		IRST for PCIE Storage			MIX-Q370D2 Assign	MIX-H310D2 Assign
0	USB3.1 Gen1/Gen2 #1		USB3.1 Gen1 #1					(port1) LAN+USB31 Gen2-10G#01	(port1) LAN+USB31 Gen1-5G#01
1	USB3.1 Gen1/Gen2 #2		USB3.1 Gen1 #2					(port2) LAN+USB31 Gen2-10G#01	(port2) LAN+USB31 Gen1-5G#01
2	USB3.1 Gen1/Gen2 #3		USB3.1 Gen1 #3					(port3) LAN+USB31 Gen2-10G#02	(port3) LAN+USB31 Gen1-5G#02
3	USB3.1 Gen1/Gen2 #4		USB3.1 Gen1 #4					(port4) LAN+USB31 Gen2-10G#02	(port4) LAN+USB31 Gen1-5G#02
4	USB3.1 Gen1/Gen2 #5		N/A					(port5) USB31 Gen2-10G#01	N/A
5	USB3.1 Gen1/Gen2 #6		N/A					(port6) USB31 Gen2-10G#01	N/A
6	USB3.1 Gen1 #7	PCIE #1	N/A		NO	x4	x2	N/A	N/A
7	USB3.1 Gen1 #8	PCIE #2	N/A					N/A	N/A
8	USB3.1 Gen1 #9	PCIE #3	N/A				x2	N/A	N/A
9	USB3.1 Gen1 #10	PCIE #4	N/A					N/A	N/A
10	PCIE #5	GbE	PCIE Gen2 #1	GbE	NO	x4	x2	LAN1_I219LM	LAN1_I219LM
11	PCIE #6		PCIE Gen2 #2					LAN2_I211	LAN2_I211 (PCIe Gen2)
12	PCIE #7		PCIE Gen2 #3				x2	M.2_Key-E	M.2_Key-E (PCIe Gen2)
13	PCIE #8		PCIE Gen2 #4					N/A	N/A
14	PCIE #9	GbE	GbE		Yes	x4	x2	M.2_Key-M SSD (PCIE*4 / SATA#4) (PCIE*4, Optane)	N/A
15	PCIE #10		N/A						N/A
16	PCIE #11	SATA #0a	PCIE Gen2 #5				x2		N/A
17	PCIE #12	SATA #1a	PCIE Gen2 #6	GbE					M.2_Key-M SSD (PCIE*1 Gen2)
18	PCIE #13	SATA #0b GbE	SATA #0	GbE	NO	x4	x2		SATA6G_0
19	PCIE #14	SATA #1b	SATA #1						N/A
20	PCIE #15	SATA #2	SATA #2				x2		SATA6G_2
21	PCIE #16	SATA #3	SATA #3						N/A
22	PCIE #17	SATA #4	N/A		Yes	x4	x2		N/A
23	PCIE #18	SATA #5	N/A						N/A
24	PCIE #19		N/A				x2		N/A
25	PCIE #20		N/A						N/A
26	PCIE #21		N/A		Yes	x4	x2		N/A
27	PCIE #22		N/A						N/A
28	PCIE #23		N/A				x2		N/A
29	PCIE #24		N/A						N/A

MIX-Q370D2 Port Assignment

Cannon Lake PCH Q370/H310 (MP)

USB Setting

USB 2.0	Function
USB2_01	LAN1+USB31 Gen2-10G#01
USB2_02	LAN1+USB31 Gen2-10G#02
USB2_03	LAN2+USB31 Gen2-10G#03
USB2_04	LAN2+USB31 Gen2-10G#04
USB2_05	USB2.0 Only_#5 Typc A
USB2_06	USB2.0 Only_#6 Typc A
USB2_07	USB2.0 Only_#7 Typc A
USB2_08	USB2.0 Only_#8 Typc A
USB2_09	USB2.0 Internal Header#9
USB2_10	USB2.0 Internal Header#10
USB2_11	USB31 Gen2-10G#11
USB2_12	USB31 Gen2-10G#12
USB2_13	N/A
USB2_14	M.2 E KEY

USB 3.1	Function
USB31_01	LAN1+USB31 Gen2-10G#01
USB31_02	LAN1+USB31 Gen2-10G#02
USB31_03	LAN2+USB31 Gen2-10G#03
USB31_04	LAN2+USB31 Gen2-10G#04
USB31_05	USB31 Gen2-10G#05
USB31_06	USB31 Gen2-10G#06
USB30_07	N/A
USB30_08	N/A
USB30_09	N/A
USB30_10	N/A

PCIE/SATA Function Define

	Function
PCIE-01 (USB3#7)	N/A
PCIE-02 (USB3#8)	N/A
PCIE-03 (USB3#9)	N/A
PCIE-04 (USB3#10)	N/A
PCIE-05	LAN1_I219LM
PCIE-06	LAN2_I211
PCIE-07	M.2_Key-E
PCIE-08	N/A
PCIE-09	M.2_Key-M SSD (PCIEx4/SATA#1) Support Optane
PCIE-10	
PCIE-11 (SATA-0a)	
PCIE-12 (SATA-1a)	

	Function
PCIE-13 (SATA-0b)	SATA6G_0
PCIE-14 (SATA-1b)	N/A
PCIE-15 (SATA-2)	SATA6G_2
PCIE-16 (SATA-3)	N/A
PCIE-17 (SATA-4)	N/A
PCIE-18 (SATA-5)	N/A
PCIE-19 (SATA-6)	N/A
PCIE-20 (SATA-7)	N/A
PCIE-21	N/A
PCIE-22	N/A
PCIE-23	N/A
PCIE-24	N/A

	Function
CLKREQ-0	M.2_BT_UART_WAKE#
CLKREQ-1	
CLKREQ-2	CLK_REQ2_LAN#
CLKREQ-3	
CLKREQ-4	
CLKREQ-5	
CLKREQ-6	
CLKREQ-7	
CLKREQ-8	CLK_REQ8_M.2_SSD#
CLKREQ-9	CLK_REQ9_M.2_WLAN#
CLKREQ-10~15	

ASUS

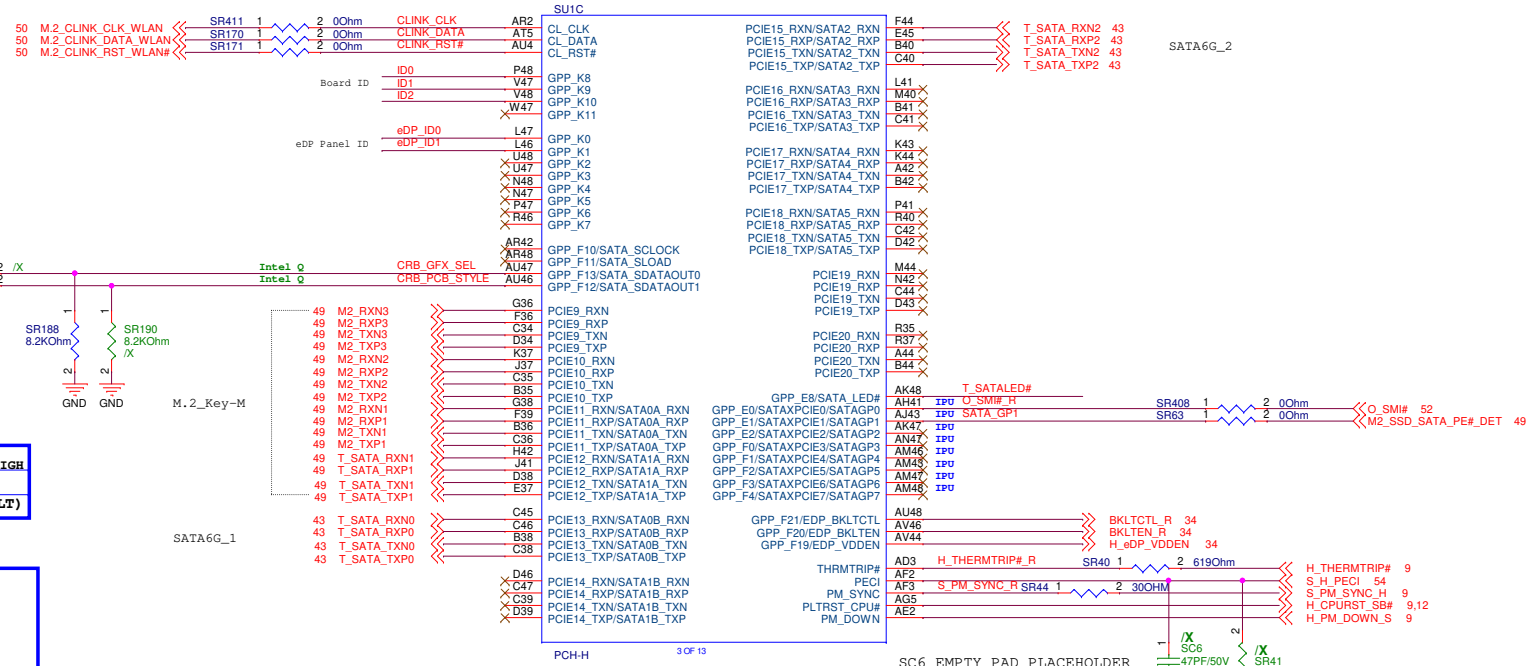
ASUSTek COMPUTER INC.

Title : CPTH (PCIE/DMI/USB)

Engineer: IPC-EE3

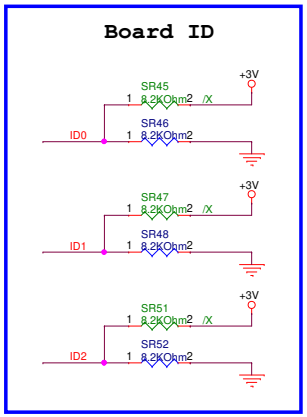
Size	Project Name	Rev
A3	MIX-Q370D2	R1.01

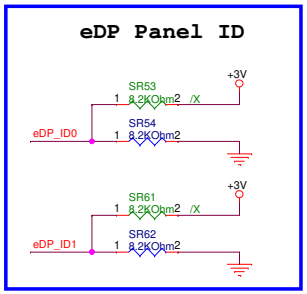
Date: Monday, February 17, 2020 Sheet 18 of 75



CRB_GFX_SEL	CRB: LOW
0	NORMAL GFX
1	CUSTOMER GFX

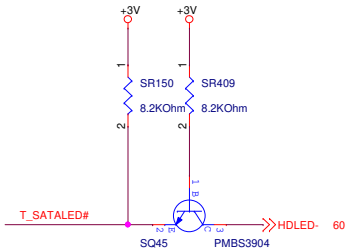
CRB_PCB_STYLE	CRB: HIGH
0	SV ADVANCE MENU
1	NORMAL MENU (DEFAULT)

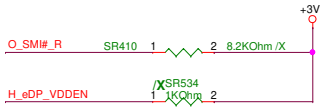




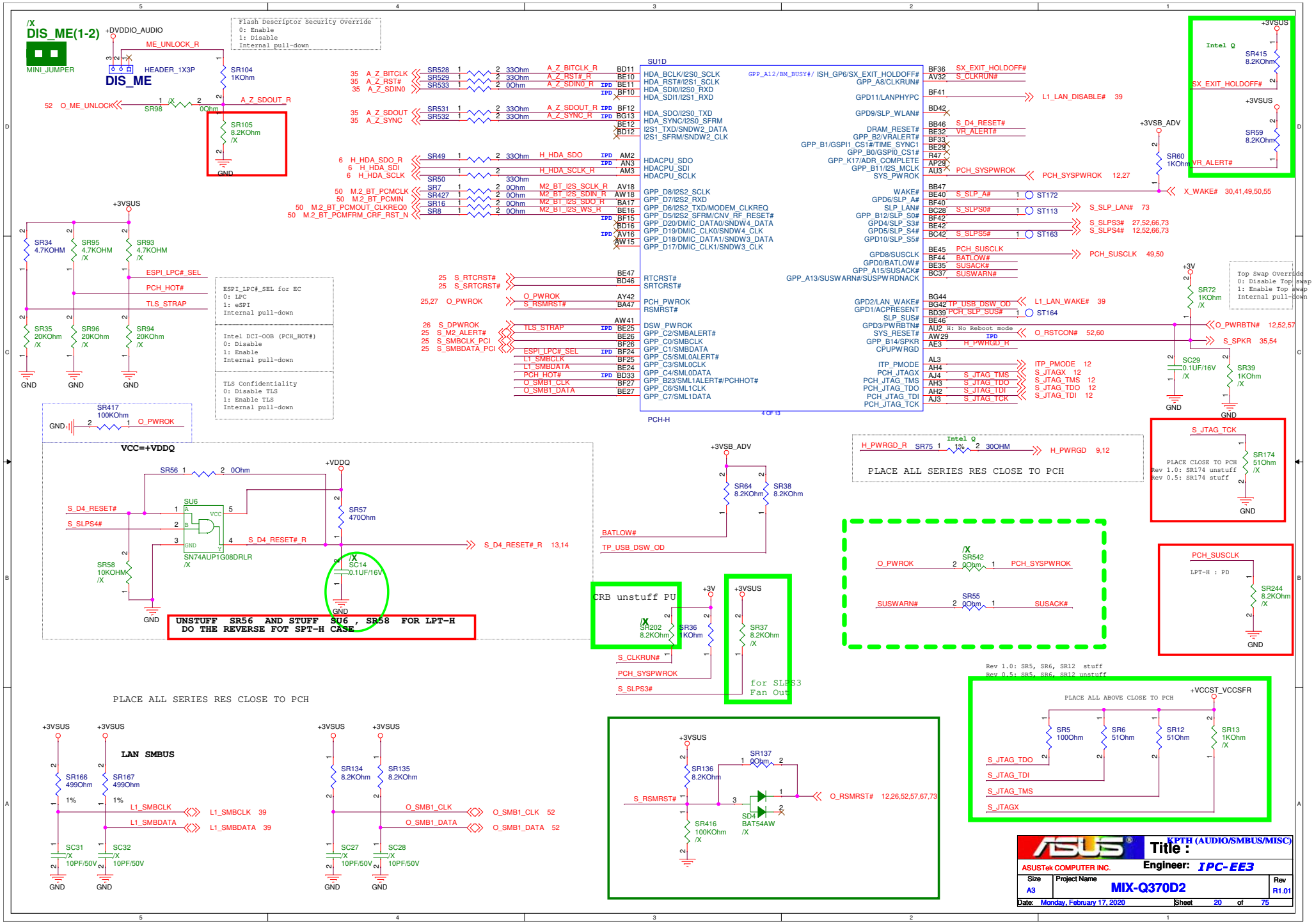
Note:

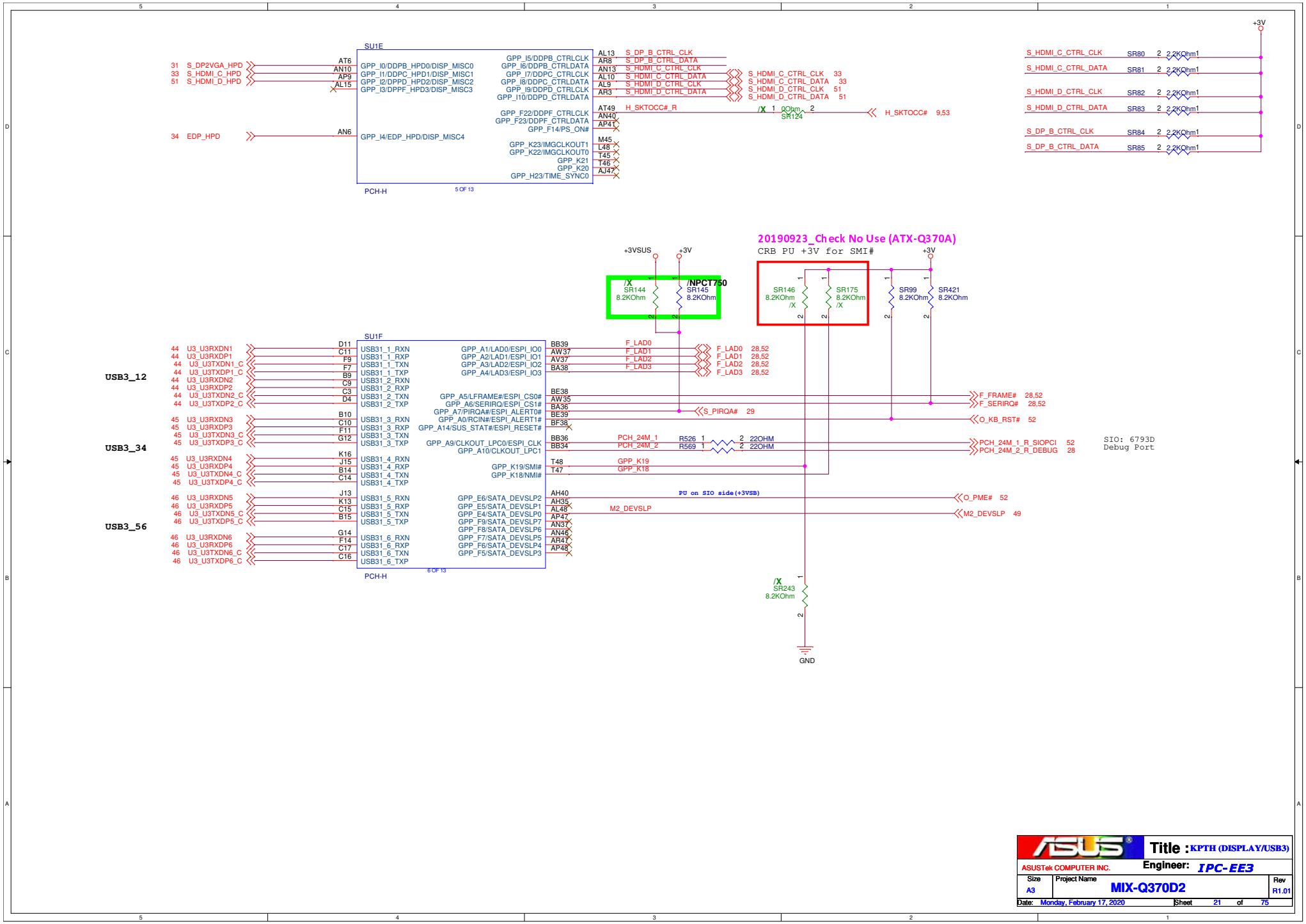
1. SATAGP[2:0]/SATAXPCIE[2:0]/GPP_E[2:0] and SATAGP[7:3]/SATAXPCIE[7:3]/GPP_F[4:0] has two native functions – the first native function (SATAXPCIEx) is selected if the Flex I/O soft strap SATA_PCIE_Select_for_Port_x = 11b. Setting SATA_PCIE_Select_for_Port_x = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe* Port x to be assigned based on the type of card installed and based on the SATAXPCIEx mux selector with the polarity for SATA or PCIe* (When SPSGPx = 0, PCIe* will be selected if the sampled value is "0" and SATA will be selected if the sampled value is "1"; When SPSGPx = 1, SATA will be selected if the sampled value is "0" and PCIe* will be selected if the sampled value is "1"). SATA/PCIe Select GPIO polarity for SATA Port x (SPSGPx) and Soft straps are handled through FITC and described in Skylake PCH SPI Flash Programming Guide (CDI doc #TBD).

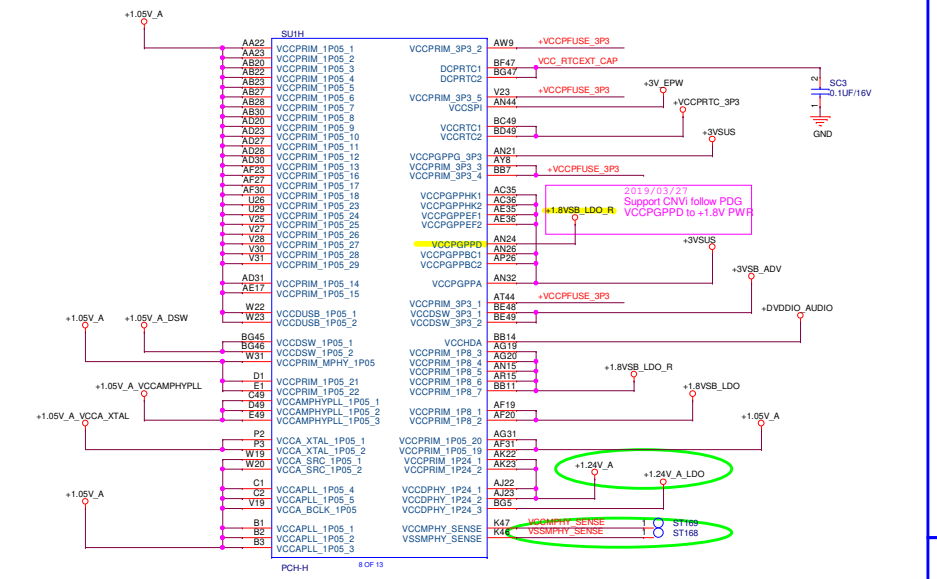


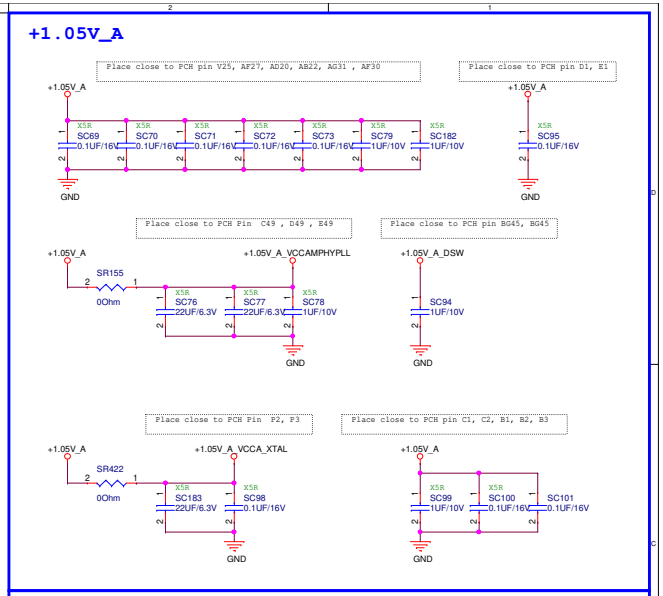


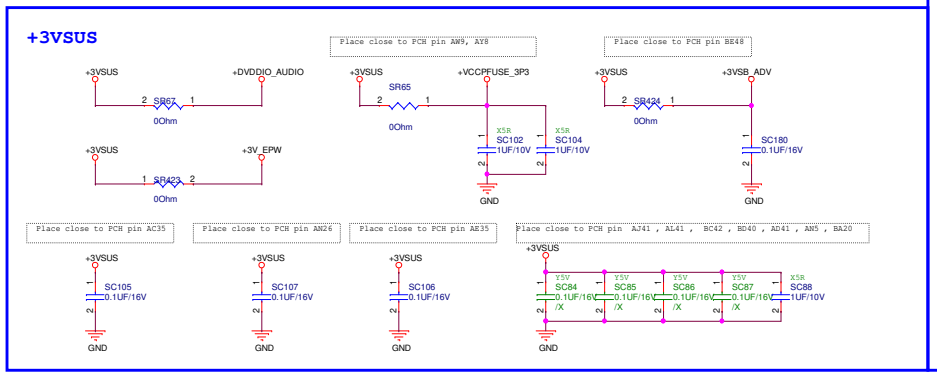
ASUSTek COMPUTER INC.	Title : KPTH (HOST/FAN/SATA)	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 19 of 75	

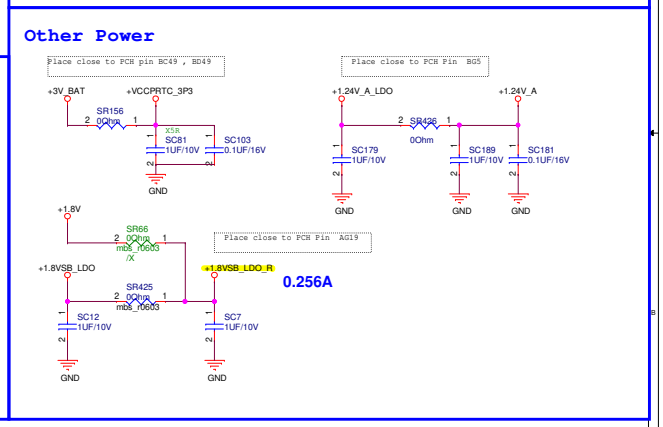

/X
DIS_ME(1-2)
MINI_JUMPER
+DVDDIO_AUDIO
ME_UNLOCK_R
HEADER_1X3P
DIS_ME
SR104 1KOhm
52 O_ME_UNLOCK
SR98 0Ohm
A_Z_SDOUT_R
SR105 8.2KOhm /X
GND
Flash Descriptor Security Override
0: Enable
1: Disable
Internal pull-down
SU1D
PCH-H
4 OF 13
35 A_Z_BITCLK SR528 33Ohm A_Z_BITCLK_R BD11 HDA_BCLK/I2S0_SCLK
35 A_Z_RST# SR529 33Ohm A_Z_RST#_R BE10 HDA_RST#/I2S1_SCLK
35 A_Z_SDIN0 SR533 0Ohm A_Z_SDIN0_R BE11 HDA_SDI0/I2S0_RXD
BF10 HDA_SDI1/I2S1_RXD
35 A_Z_SDOUT SR531 33Ohm A_Z_SDOUT_R BF12 HDA_SDO/I2S0_TXD
35 A_Z_SYNC SR532 33Ohm A_Z_SYNC_R BG13 HDA_SYNC/I2S0_SFRM
BE12 I2S1_TXD/SNDW2_DATA
BD12 I2S1_SFRM/SNDW2_CLK
6 H_HDA_SDO_R SR49 33Ohm H_HDA_SDO AM2 HDACPU_SDO
6 H_HDA_SDI AN3 HDACPU_SDI
6 H_HDA_SCLK SR50 33Ohm H_HDA_SCLK_R AM3 HDACPU_SCLK
50 M.2_BT_PCMCLK SR7 0Ohm M2_BT_I2S_SCLK_R AV18 GPP_D8/I2S2_SCLK
50 M.2_BT_PCMIN SR427 0Ohm M2_BT_I2S_SDIN_R AW18 GPP_D7/I2S2_RXD
50 M.2_BT_PCMOUT_CLKREQ0 SR16 0Ohm M2_BT_I2S_SDO_R BA17 GPP_D6/I2S2_TXD/MODEM_CLKREQ
50 M.2_BT_PCMFRM_CRF_RST_N SR8 0Ohm M2_BT_I2S_WS_R BE16 GPP_D5/I2S2_SFRM/CNV_RF_RESET#
BF15 GPP_D20/DMIC_DATA0/SNDW4_DATA
BD16 GPP_D19/DMIC_CLK0/SNDW4_CLK
AV16 GPP_D18/DMIC_DATA1/SNDW3_DATA
AW15 GPP_D17/DMIC_CLK1/SNDW3_CLK
25 S_RTCRST# BE47 RTCRST#
25 S_SRTCRST# BD46 SRTCRST#
25,27 O_PWROK AY42 PCH_PWROK
S_RSMRST# BA47 RSMRST#
AW41 DSW_PWROK
26 S_DPWROK TLS_STRAP BE25 GPP_C2/SMBALERT#
25 S_M2_ALERT# BE26 GPP_C0/SMBCLK
25 S_SMBCLK_PCI BF26 GPP_C1/SMBDATA
25 S_SMBDATA_PCI ESPI_LPC#_SEL BF24 GPP_C5/SML0ALERT#
L1_SMBCLK BF25 GPP_C3/SML0CLK
L1_SMBDATA BE24 GPP_C4/SML0DATA
PCH_HOT# BD33 GPP_B23/SML1ALERT#/PCHHOT#
O_SMB1_CLK BF27 GPP_C6/SML1CLK
O_SMB1_DATA BE27 GPP_C7/SML1DATA
GPP_A12/BM_BUSY#/ ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
BF36 SX_EXIT_HOLDOFF#
AV32 S_CLKRUN#
GPD11/LANPHYPC BF41 L1_LAN_DISABLE# 39
GPD9/SLP_WLAN# BD42
DRAM_RESET# BB46 S_D4_RESET#
GPP_B2/VRALERT# BE32 VR_ALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1 BF33
GPP_B0/GSPI0_CS1# BE29
GPP_K17/ADR_COMPLETE R47
GPP_B11/I2S_MCLK AP29
SYS_PWROK AU3 PCH_SYSPWROK PCH_SYSPWROK 12,27
WAKE# BB47 X_WAKE# 30,41,49,50,55
GPD6/SLP_A# BE40 S_SLP_A# ST172
SLP_LAN# BF40
GPP_B12/SLP_S0# BC28 S_SLPS0# ST113 S_SLP_LAN# 73
GPD4/SLP_S3# BF42 S_SLPS3# 27,52,66,73
GPD5/SLP_S4# BE42 S_SLPS4# 12,52,66,73
GPD10/SLP_S5# BC42 S_SLPS5# ST163
GPD8/SUSCLK BE45 PCH_SUSCLK PCH_SUSCLK 49,50
GPD0/BATLOW# BF44 BATLOW#
GPP_A15/SUSACK# BE35 SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK BC37 SUSWARN#
GPD2/LAN_WAKE# BG44
GPD1/ACPRESENT BG42 TP_USB_DSW_OD L1_LAN_WAKE# 39
SLP_SUS# BD39 PCH_SLP_SUS# ST164
GPD3/PWRBTN# BE46
SYS_RESET# AU2 H: No Reboot mode O_PWRBTN# 12,52,57
GPP_B14/SPKR AW29 IPD O_RSTCON# 52,60
CPUPWRGD AE3 H_PWRGD_H S_SPKR 35,54
ITP_PMODE AL3 ITP_PMODE 12
PCH_JTAGX AH4 S_JTAGX 12
PCH_JTAG_TMS AJ4 S_JTAG_TMS 12
PCH_JTAG_TDO AH3 S_JTAG_TDO 12
PCH_JTAG_TDI AH2 S_JTAG_TDI 12
PCH_JTAG_TCK AJ3 S_JTAG_TCK
+3VSUS
Intel Q
SR415 8.2KOhm
SX_EXIT_HOLDOFF#
+3VSUS
SR59 8.2KOhm
VR_ALERT#
+3VSB_ADV
SR60 1KOhm
+3V
SR72 1KOhm /X
Top Swap Override
0: Disable Top swap
1: Enable Top swap
Internal pull-down
SC29 0.1UF/16V /X
SR39 1KOhm /X
GND
+3VSUS
SR34 4.7KOHM
SR95 4.7KOHM /X
SR93 4.7KOHM /X
ESPI_LPC#_SEL
PCH_HOT#
TLS_STRAP
SR35 20KOhm /X
SR96 20KOhm /X
SR94 20KOhm /X
GND
ESPI_LPC#_SEL for EC
0: LPC
1: eSPI
Internal pull-down
Intel DCI-OOB (PCH_HOT#)
0: Disable
1: Enable
Internal pull-down
TLS Confidentiality
0: Disable TLS
1: Enable TLS
Internal pull-down
SR417 100KOhm
GND
O_PWROK
VCC=+VDDQ
SR56 0Ohm
+VDDQ
SU6
S_D4_RESET#
S_SLPS4#
SN74AUP1G08DRLR /X
SR57 470Ohm
S_D4_RESET#_R
S_D4_RESET#_R 13,14
SR58 10KOHM /X
/X SC14 0.1UF/16V
GND
UNSTUFF SR56 AND STUFF SU6 , SR58 FOR LPT-H
DO THE REVERSE FOT SPT-H CASE
+3VSB_ADV
SR64 8.2KOhm
SR38 8.2KOhm
BATLOW#
TP_USB_DSW_OD
H_PWRGD_R SR75 1% 30OHM H_PWRGD 9,12
Intel Q
PLACE ALL SERIES RES CLOSE TO PCH
S_JTAG_TCK
SR174 51Ohm /X
PLACE CLOSE TO PCH
Rev 1.0: SR174 unstuff
Rev 0.5: SR174 stuff
GND
/X SR542 0Ohm
O_PWROK PCH_SYSPWROK
SR55 0Ohm
SUSWARN# SUSACK#
PCH_SUSCLK
LPT-H : PD
SR244 8.2KOhm /X
GND
CRB unstuff PU
/X SR202 8.2KOhm
SR36 1KOhm
+3V
+3VSUS
SR37 8.2KOhm /X
S_CLKRUN#
PCH_SYSPWROK
S_SLPS3#
for SLPS3 Fan Out
Rev 1.0: SR5, SR6, SR12 stuff
Rev 0.5: SR5, SR6, SR12 unstuff
PLACE ALL ABOVE CLOSE TO PCH
+VCCST_VCCSFR
SR5 100Ohm
SR6 51Ohm
SR12 51Ohm
SR13 1KOhm /X
S_JTAG_TDO
S_JTAG_TDI
S_JTAG_TMS
S_JTAGX
PLACE ALL SERIES RES CLOSE TO PCH
LAN SMBUS
+3VSUS
SR166 499Ohm 1%
SR167 499Ohm 1%
L1_SMBCLK L1_SMBCLK 39
L1_SMBDATA L1_SMBDATA 39
SC31 /X 10PF/50V
SC32 /X 10PF/50V
GND
SR134 8.2KOhm
SR135 8.2KOhm
O_SMB1_CLK O_SMB1_CLK 52
O_SMB1_DATA O_SMB1_DATA 52
SC27 /X 10PF/50V
SC28 /X 10PF/50V
+3VSUS
SR136 8.2KOhm
SR137 0Ohm
S_RSMRST#
O_RSMRST# 12,26,52,57,67,73
SR416 100KOhm /X
SD4 BAT54AW /X
ASUS
ASUSTek COMPUTER INC.
Title : KPTH (AUDIO/SMBUS/MISC)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 20 of 75


SU1E
PCH-H
5 OF 13
31 S_DP2VGA_HPD
33 S_HDMI_C_HPD
51 S_HDMI_D_HPD
34 EDP_HPD
AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
AP9 GPP_I2/DPPF_HPD2/DISP_MISC2
AL15 GPP_I3/DPPF_HPD3/DISP_MISC3
AN6 GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F22/DDPF_CTRLCLK
GPP_F23/DDPF_CTRLDATA
GPP_F14/PS_ON#
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0
AL13 S_DP_B_CTRL_CLK
AR8 S_DP_B_CTRL_DATA
AN13 S_HDMI_C_CTRL_CLK
AL10 S_HDMI_C_CTRL_DATA
AL9 S_HDMI_D_CTRL_CLK
AR3 S_HDMI_D_CTRL_DATA
AT49 H_SKTOCC#_R
AN40
AP41
M45
L48
T45
T46
AJ47
S_HDMI_C_CTRL_CLK 33
S_HDMI_C_CTRL_DATA 33
S_HDMI_D_CTRL_CLK 51
S_HDMI_D_CTRL_DATA 51
/X 1 0Ohm 2 SR124
H_SKTOCC# 9,53
+3V
S_HDMI_C_CTRL_CLK SR80 2 2.2KOhm 1
S_HDMI_C_CTRL_DATA SR81 2 2.2KOhm 1
S_HDMI_D_CTRL_CLK SR82 2 2.2KOhm 1
S_HDMI_D_CTRL_DATA SR83 2 2.2KOhm 1
S_DP_B_CTRL_CLK SR84 2 2.2KOhm 1
S_DP_B_CTRL_DATA SR85 2 2.2KOhm 1
20190923_Check No Use (ATX-Q370A)
CRB PU +3V for SMI#
+3VSUS
+3V
/X SR144 8.2KOhm
/NPCT750 SR145 8.2KOhm
SR146 8.2KOhm /X
SR175 8.2KOhm /X
SR99 8.2KOhm
SR421 8.2KOhm
SU1F
PCH-H
6 OF 13
USB3_12
USB3_34
USB3_56
44 U3_U3RXDN1 D11 USB31_1_RXN
44 U3_U3RXDP1 C11 USB31_1_RXP
44 U3_U3TXDN1_C F9 USB31_1_TXN
44 U3_U3TXDP1_C F7 USB31_1_TXP
44 U3_U3RXDN2 B9 USB31_2_RXN
44 U3_U3RXDP2 C9 USB31_2_RXP
44 U3_U3TXDN2_C C3 USB31_2_TXN
44 U3_U3TXDP2_C D4 USB31_2_TXP
45 U3_U3RXDN3 B10 USB31_3_RXN
45 U3_U3RXDP3 C10 USB31_3_RXP
45 U3_U3TXDN3_C F11 USB31_3_TXN
45 U3_U3TXDP3_C G12 USB31_3_TXP
45 U3_U3RXDN4 K16 USB31_4_RXN
45 U3_U3RXDP4 J15 USB31_4_RXP
45 U3_U3TXDN4_C B14 USB31_4_TXN
45 U3_U3TXDP4_C C14 USB31_4_TXP
46 U3_U3RXDN5 J13 USB31_5_RXN
46 U3_U3RXDP5 K13 USB31_5_RXP
46 U3_U3TXDN5_C C15 USB31_5_TXN
46 U3_U3TXDP5_C B15 USB31_5_TXP
46 U3_U3RXDN6 G14 USB31_6_RXN
46 U3_U3RXDP6 F14 USB31_6_RXP
46 U3_U3TXDN6_C C17 USB31_6_TXN
46 U3_U3TXDP6_C C16 USB31_6_TXP
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
BB39 F_LAD0
AW37 F_LAD1
AV37 F_LAD2
BA38 F_LAD3
F_LAD0 28,52
F_LAD1 28,52
F_LAD2 28,52
F_LAD3 28,52
BE38 F_FRAME# 28,52
AW35 F_SERIRQ# 28,52
BA36 S_PIRQA# 29
BE39 O_KB_RST# 52
BF38
BB36 PCH_24M_1 R526 1 2 22OHM PCH_24M_1_R_SIOPCI 52
BB34 PCH_24M_2 R569 1 2 22OHM PCH_24M_2_R_DEBUG 28
SIO: 6793D
Debug Port
T48 GPP_K19
T47 GPP_K18
AH40 PU on SIO side(+3VSB) O_PME# 52
AH35
AL48 M2_DEVSLP M2_DEVSLP 49
AP47
AN37
AN46
AR47
AP48
/X SR243 8.2KOhm
GND
ASUSTek COMPUTER INC.
Title : KPTH (DISPLAY/USB3)
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 21 of 75





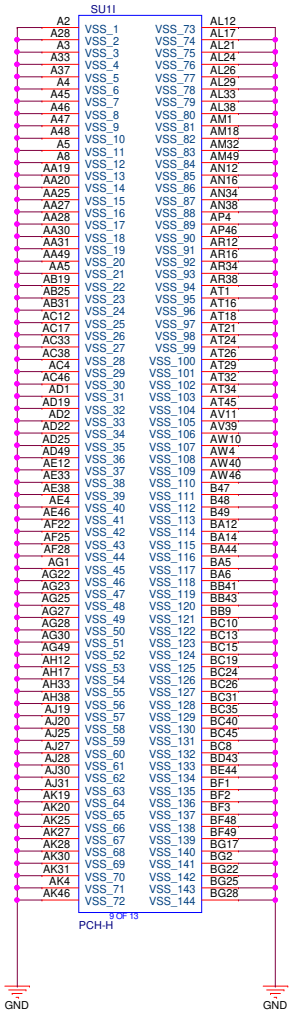


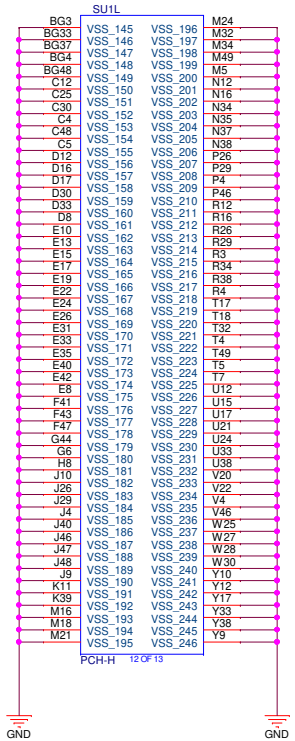


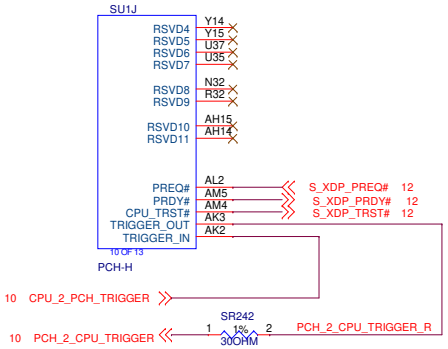
GPIO Voltage Level

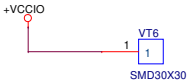
Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+3VSUS
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_D	VCCPGPPD	1.8V or 3.3V	+1.8VSUS
GPP_E	VCCPGPPEF	1.8V or 3.3V	+3VSUS
GPP_F	VCCPGPPEF	1.8V or 3.3V	+3VSUS
GPP_G	VCCPGPPG_3P3 VCCPRIM_1P8	Dynamic voltage to be config SDIO	+3VSUS +1.8VSUS
GPP_H	VCCPGPPHK	1.8V or 3.3V	+3VSUS
GPP_I	VCCPRIM_3P3	3.3V Only	+3VSUS
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8VSUS
GPP_K	VCCPGPPHK	1.8V or 3.3V	+3VSUS
GPD	VCCDSW_3P3	3.3V Only	+3VA_DSW

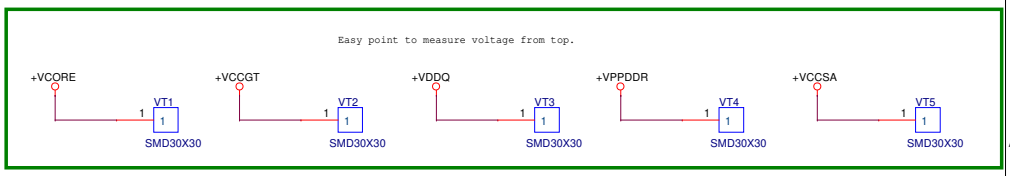
ASUSTek COMPUTER INC.	Title : KPTH (POWER)	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.01
Date: Monday, February 17, 2020	Sheet 22 of 75		



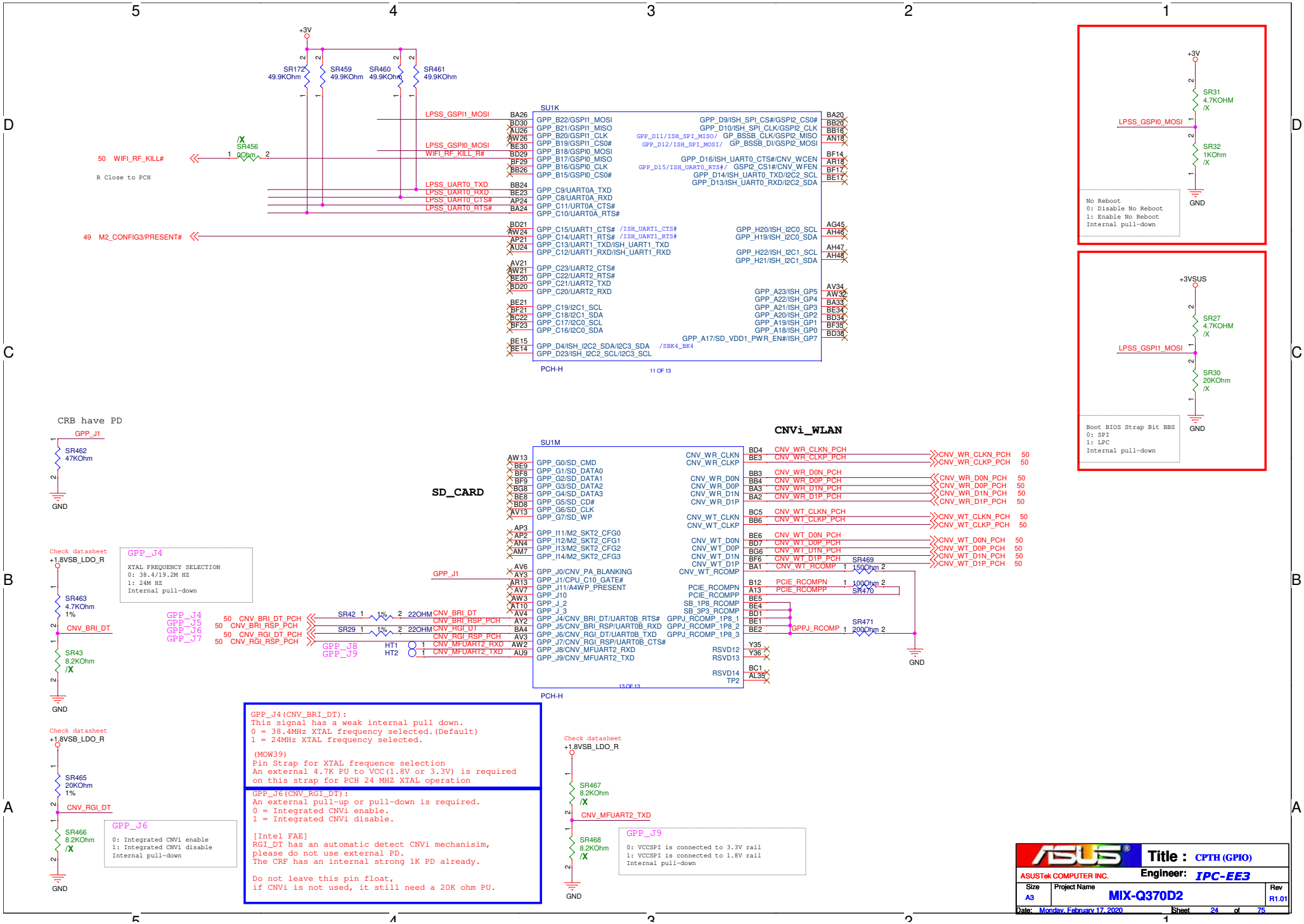


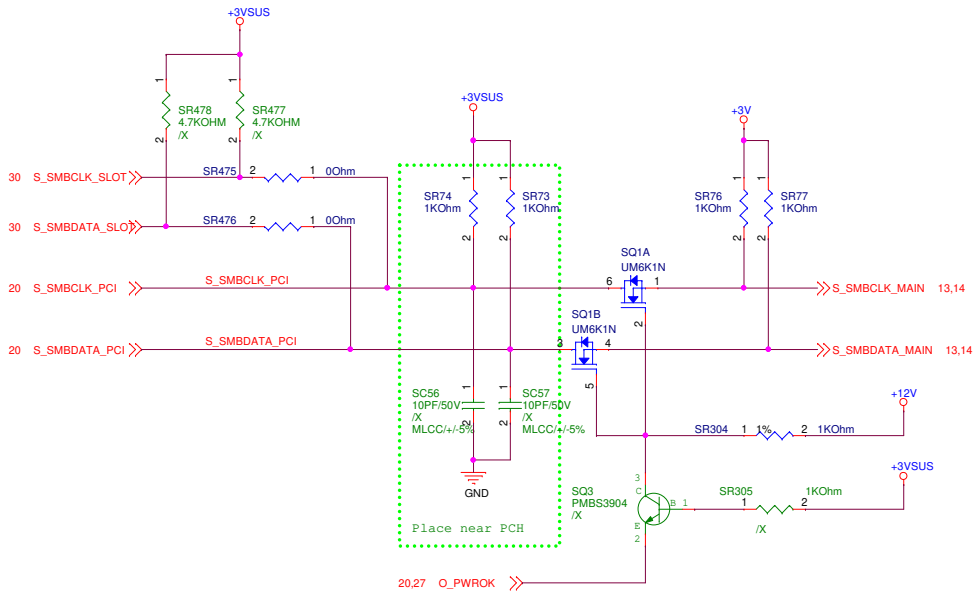


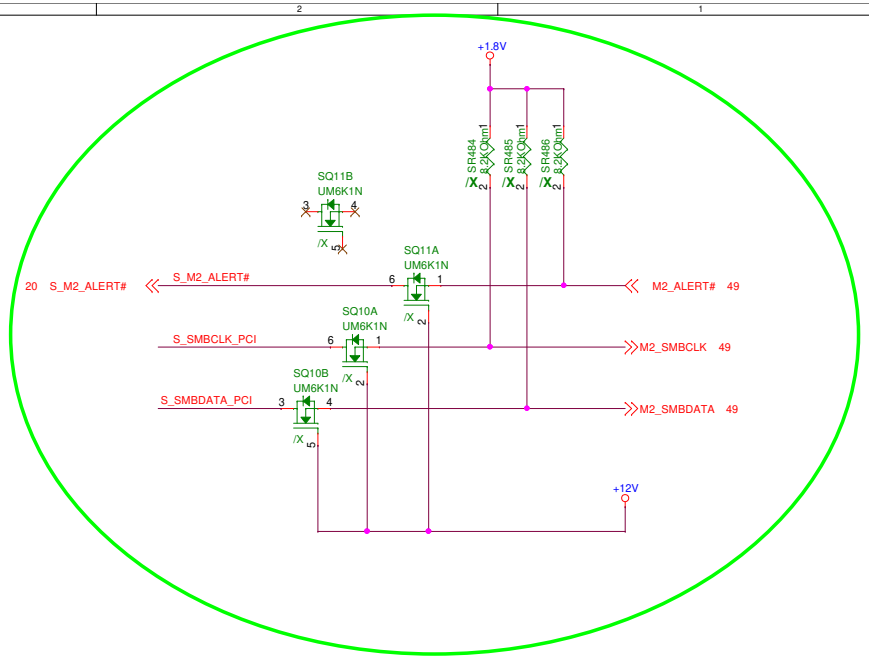




ASUS	Title : CPTH (GND)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 23 of 75		


SU1K
PCH-H
11 OF 13
SR172 49.9KOhm
SR459 49.9KOhm
SR460 49.9KOhm
SR461 49.9KOhm
SR456 0Ohm
50 WIFI_RF_KILL#
R Close to PCH
49 M2_CONFIG3/PRESENT#
LPSS_GSPI1_MOSI
LPSS_GSPI0_MOSI
WIFI_RF_KILL_R#
LPSS_UART0_TXD
LPSS_UART0_RXD
LPSS_UART0_CTS#
LPSS_UART0_RTS#
SR31 4.7KOHM /X
SR32 1KOhm /X
No Reboot
0: Disable No Reboot
1: Enable No Reboot
Internal pull-down
SR27 4.7KOHM /X
SR30 20KOhm /X
Boot BIOS Strap Bit BBS
0: SPI
1: LPC
Internal pull-down
CRB have PD
SR462 47KOhm
SR463 4.7KOhm 1%
SR43 8.2KOhm /X
GPP_J4
XTAL FREQUENCY SELECTION
0: 38.4/19.2M HZ
1: 24M HZ
Internal pull-down
SD_CARD
SU1M
PCH-H
13 OF 13
CNVi_WLAN
SR469 150Ohm
SR470
SR471 200Ohm
SR42 22OHM
SR29 22OHM
GPP_J8
GPP_J9
GPP_J6
0: Integrated CNVi enable
1: Integrated CNVi disable
Internal pull-down
SR465 20KOhm 1%
SR466 8.2KOhm /X
GPP_J4(CNV_BRI_DT):
This signal has a weak internal pull down.
0 = 38.4MHz XTAL frequency selected.(Default)
1 = 24MHz XTAL frequency selected.
(MOW39)
Pin Strap for XTAL frequence selection
An external 4.7K PU to VCC(1.8V or 3.3V) is required
on this strap for PCH 24 MHZ XTAL operation
GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
[Intel FAE]
RGI_DT has an automatic detect CNVi mechanisim,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.
SR467 8.2KOhm /X
SR468 8.2KOhm /X
GPP_J9
0: VCCSPI is connected to 3.3V rail
1: VCCSPI is connected to 1.8V rail
Internal pull-down
Title : CPTH (GPIO)
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 24 of 75

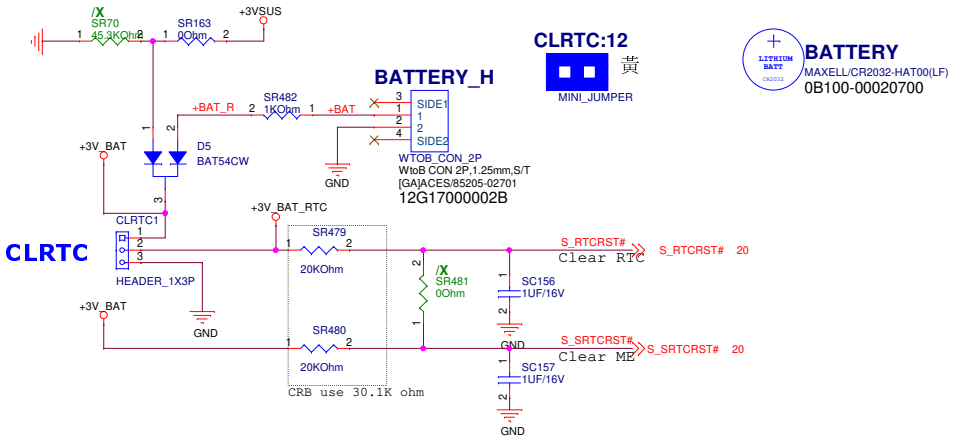


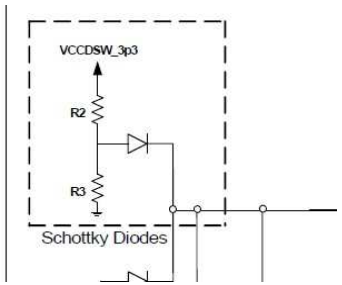


VCCRTC External Circuit

On SKL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

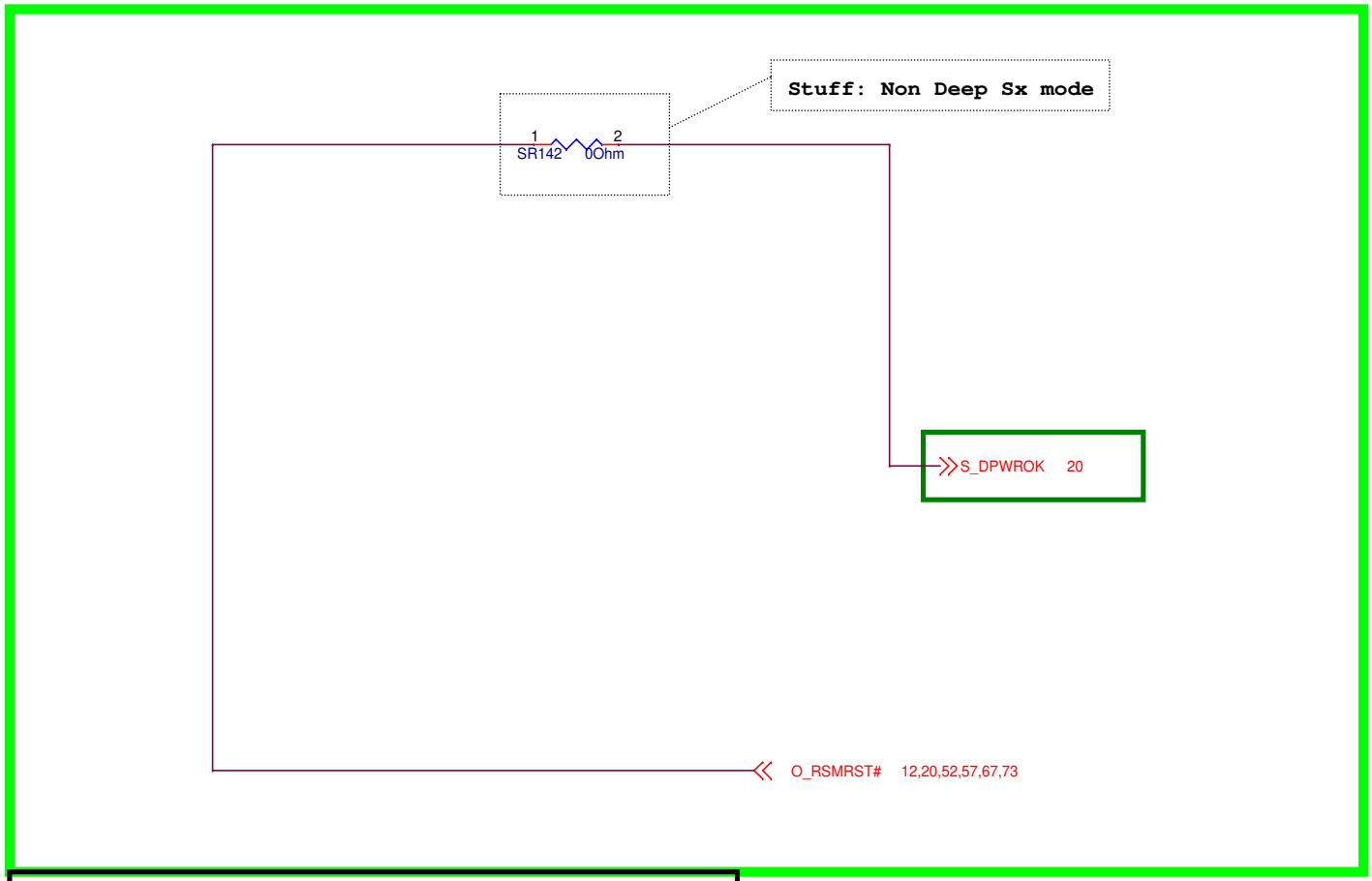
CRB use resistor divider newrok [SR163=0 , SR70=/X]

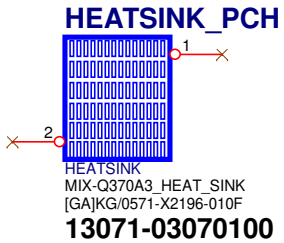




ASUS	Title : CPTH (SMBUS/CLRTC)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 25 of 75		

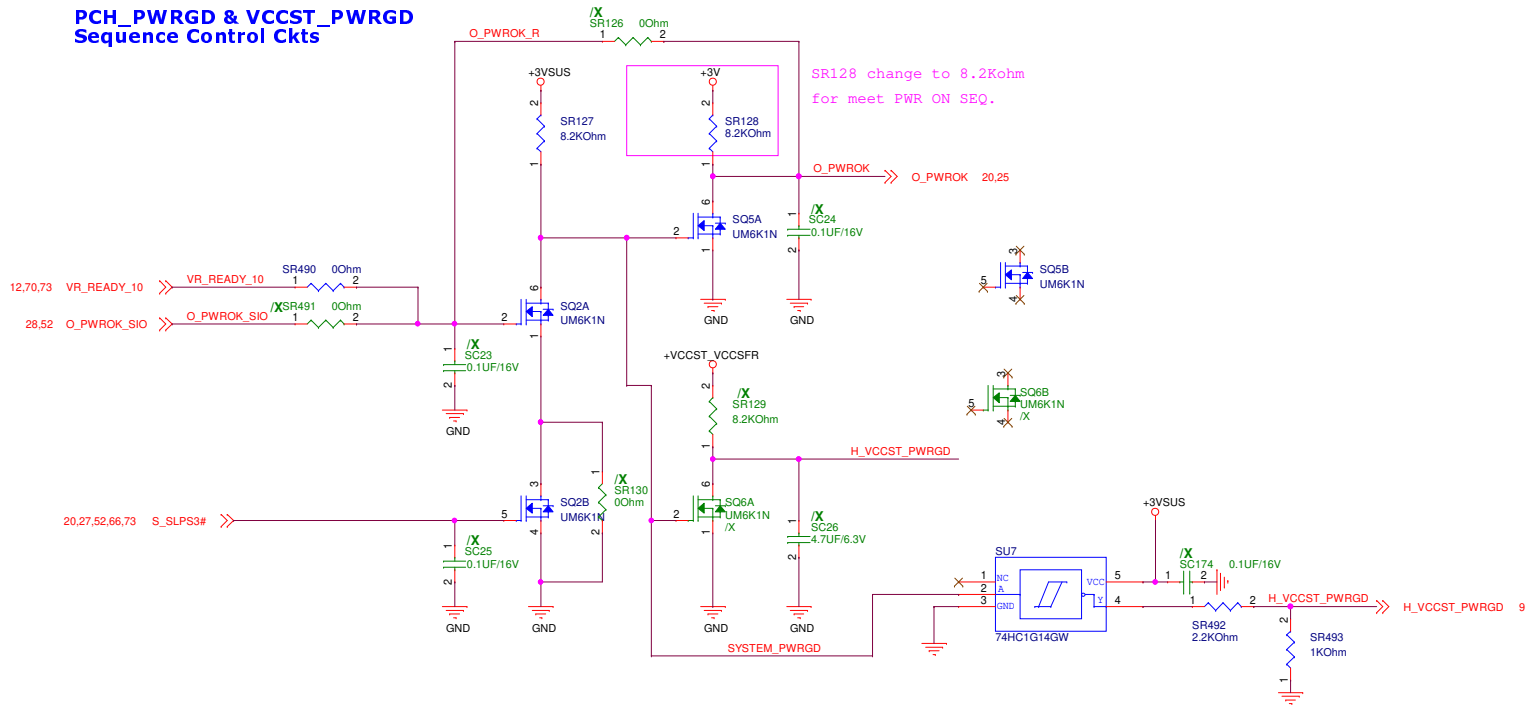
2015/04/15



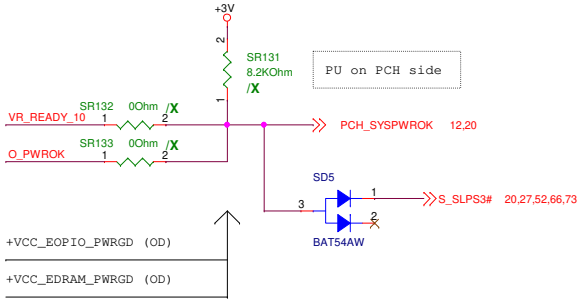


ASUS	Title : CPTH (DSW SEQUENCE)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A4	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 26 of 75		

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

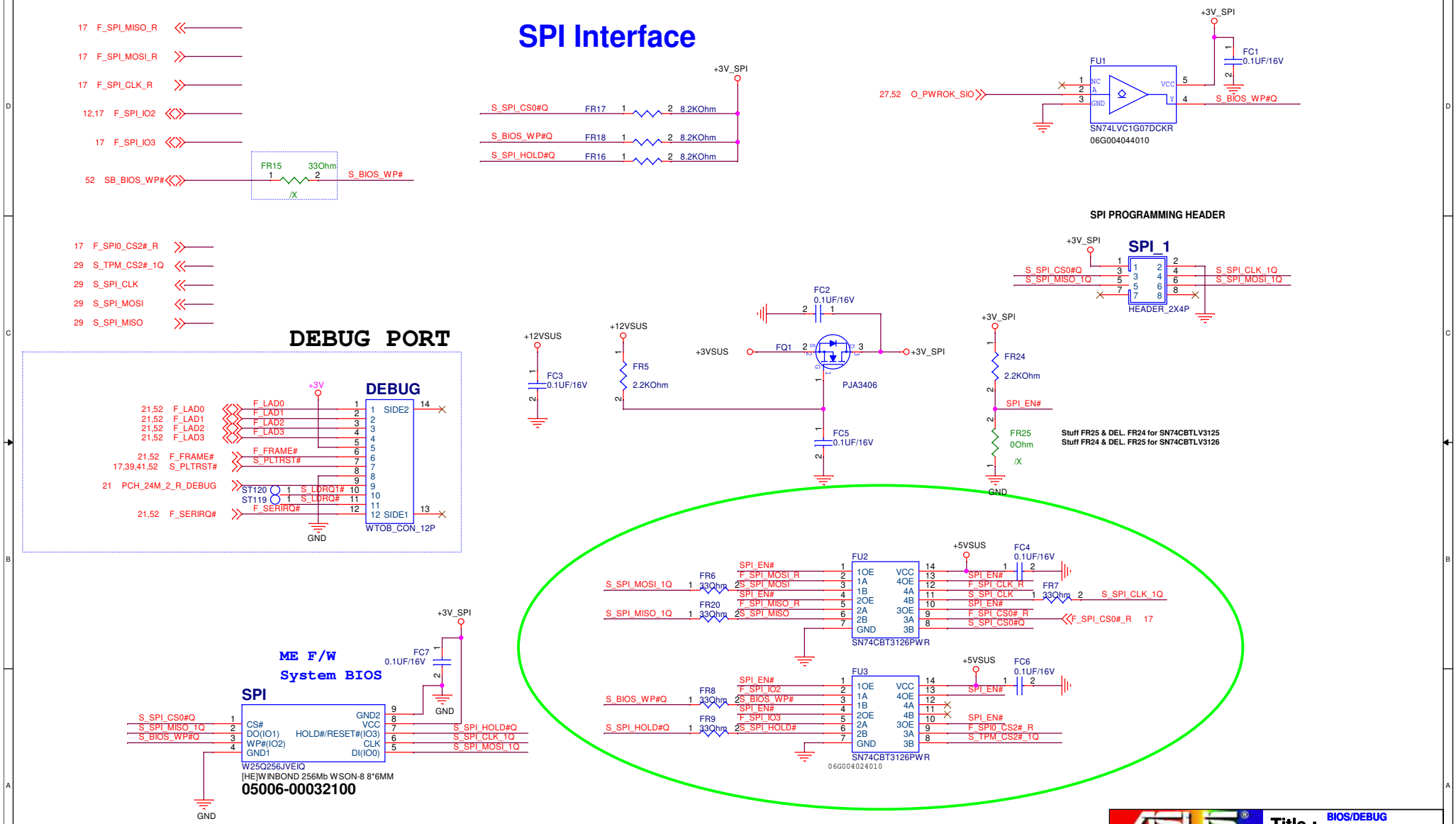
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

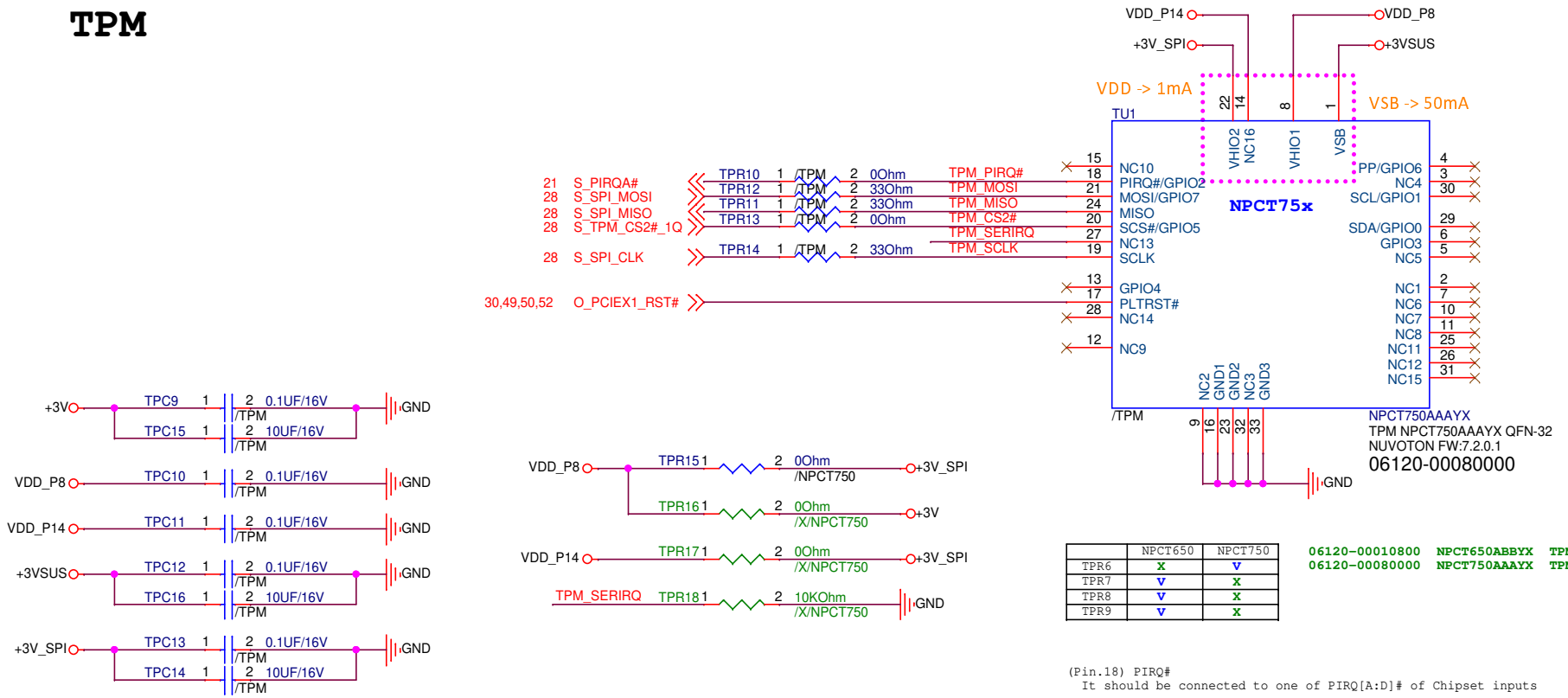
ASUS	Title : CPTH (PCH/SYS/PROC_PWROK)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 27 of 75	

SPI Interface



ASUSTek COMPUTER INC.	Title : BIOS/DEBUG		
	Engineer: IPC-EE3		
Size B	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 28 of 75		

TPM



	NPCT650	NPCT750
TPR6	X	V
TPR7	V	X
TPR8	V	X
TPR9	V	X

06120-00010800 NPCT650ABBYX TPM2.0 F/W:1.3.1.0
06120-00080000 NPCT750AAAYX TPM2.0 F/W:7.2.0.1

(Pin.18) PIRQ#
It should be connected to one of PIRQ[A:D]# of Chipset inputs

(Pin.27) SERIRQ
for LPC interface use only

(Pin.17) SPI_RST#
PCI system reset used for LPC/SPI bus (Hardware reset)

(Pin.4) PP (Physical Presense Input)
By default the PP functionality is disabled.

GPIO[0:6] and PP are optional.
Leave them open if not used.

GPIO[0] contact to SLP_S0# for Connected Standby, if supported.

Windows10 Hardware Compatibility Specifications for RS3
Mandatory: The TPM must support driven communication.
Mandatory: The TPM interrupt pin must be connected to an interrupt controller.

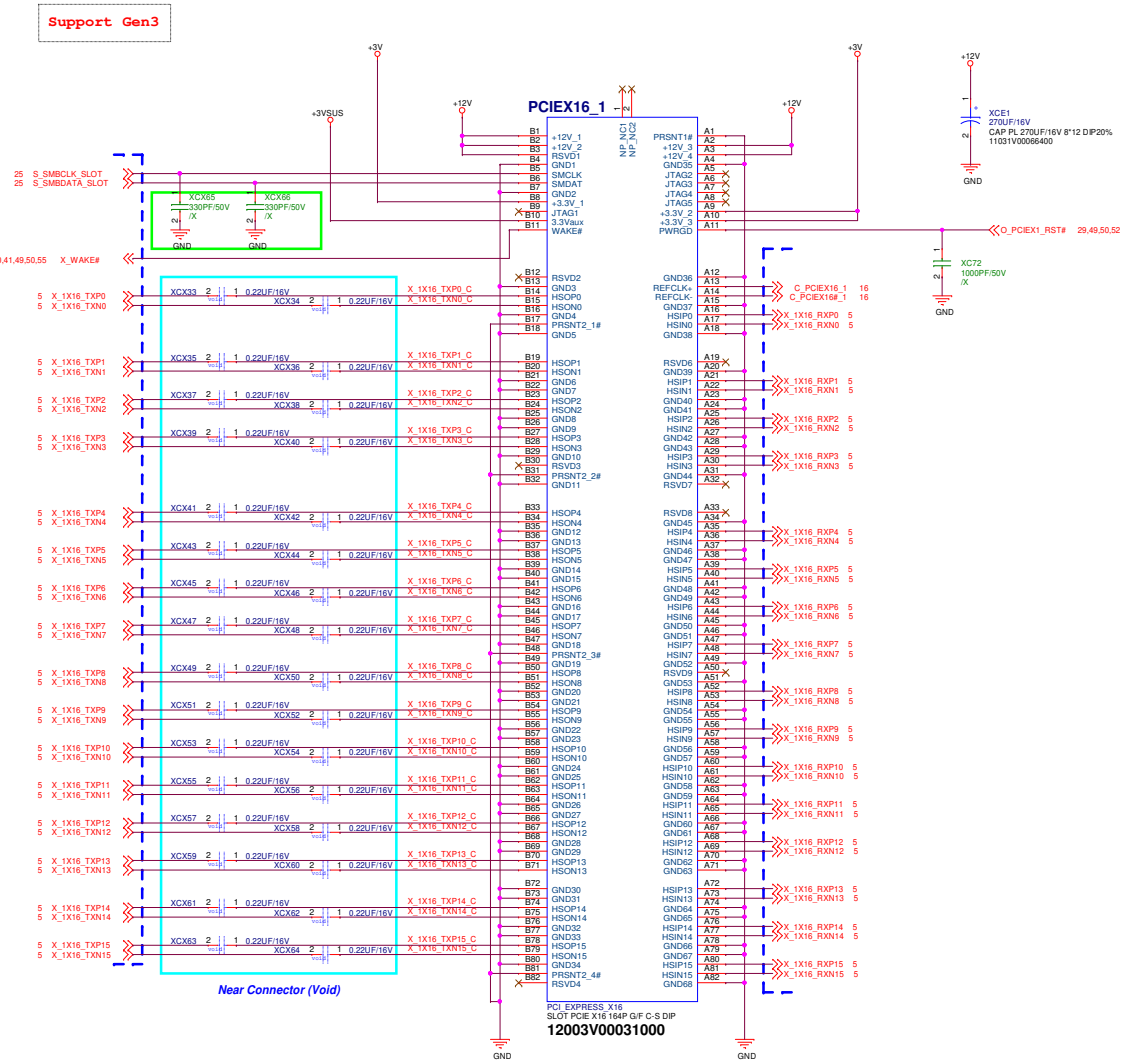
Note:
TPM.VDD change to +1.8V or +3.3V
TPM.VHIO change to +1.8V_SPI or +3V_SPI (same as chipset LPC/SPI interface)

If MP schedule after 2018/02/28,
Recommend change TPM solution to NPCT750 for Win10 RS3 WHQL

Co-Layout NPCT650 and NPCT750 (+3.3V SPI only)

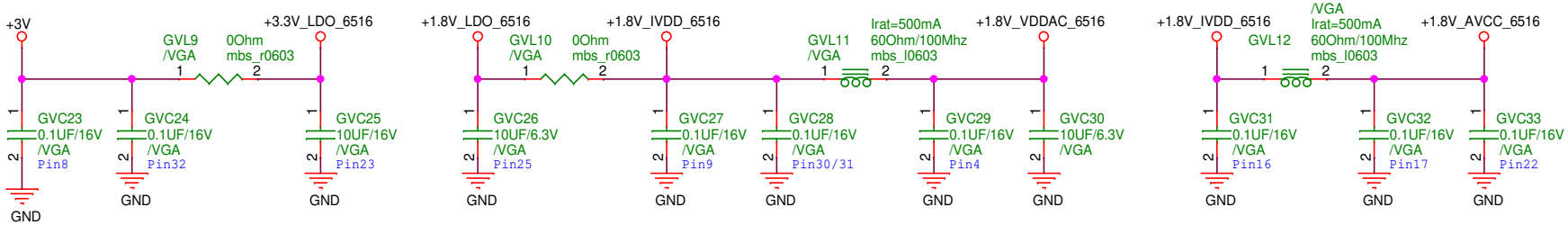
Based on Microsoft request,
nuvoTon will update NPCT750 F/W during 2018 Q2

ASUS	Title : TPM_NPCT750AAAYX		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A4	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 29 of 75		



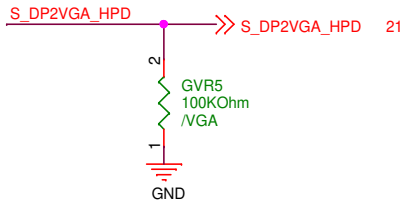
ASUSTeK COMPUTER INC.	Title : PCIEX16_1		
	Engineer: IPC-EE3		
Size C	Project Name MIX-Q370D2		Rev 1.01
Date: Monday, February 17, 2020	Sheet 30 of 75		

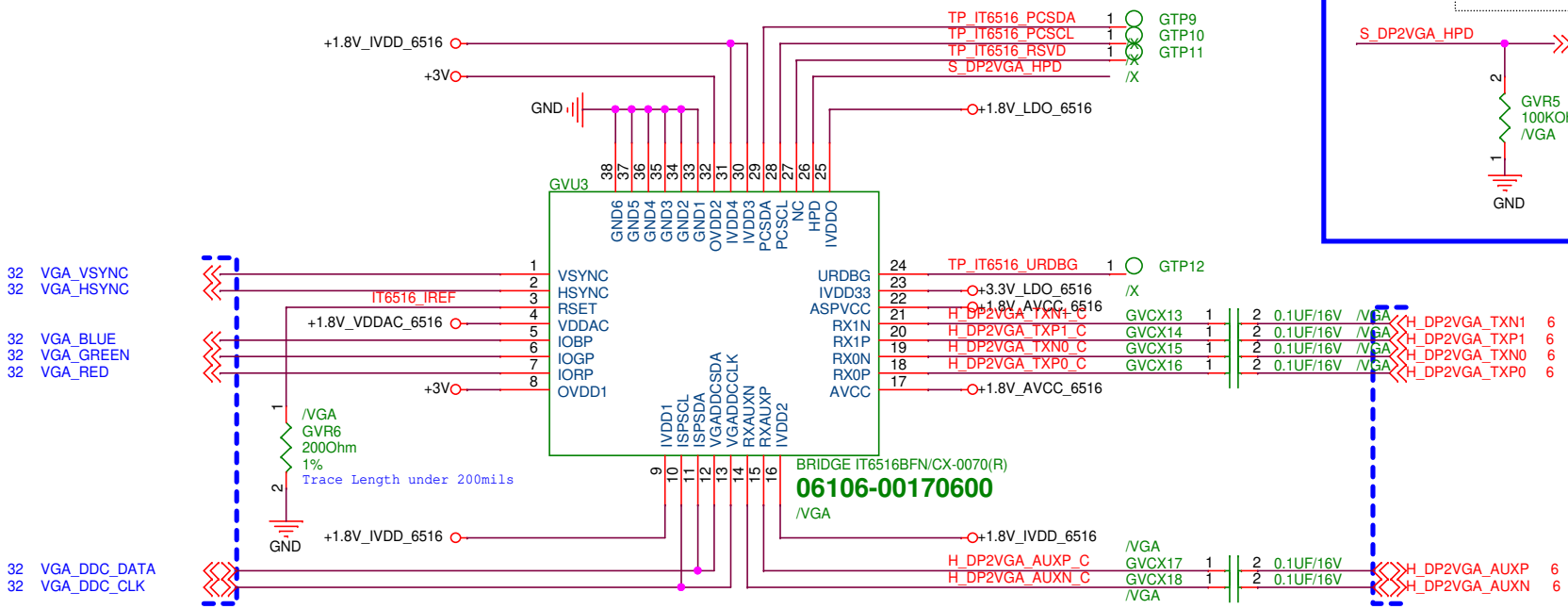
IT6516B Power Caps and Beads



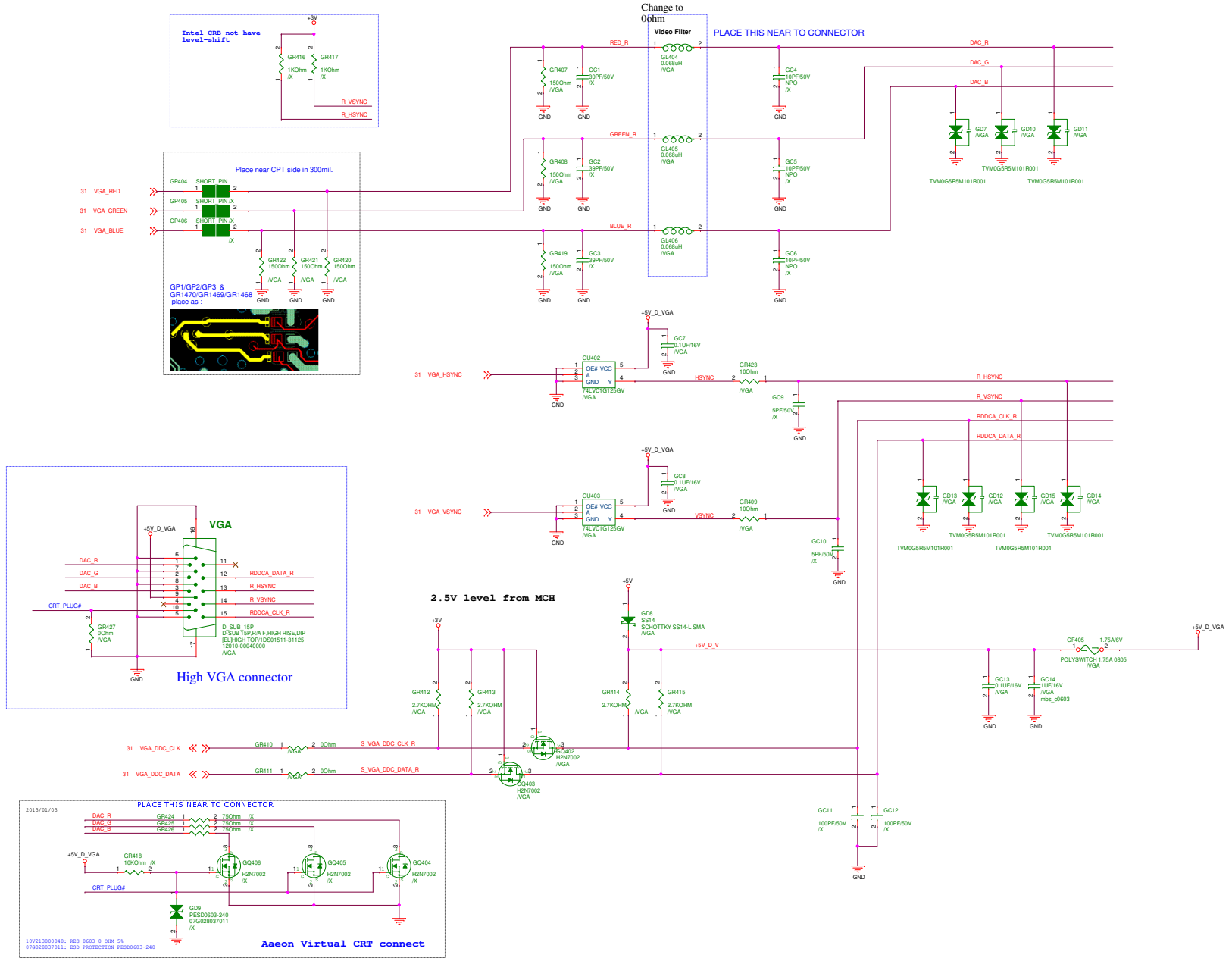
Hot-Plug Detect

Voltage Level +3.3V

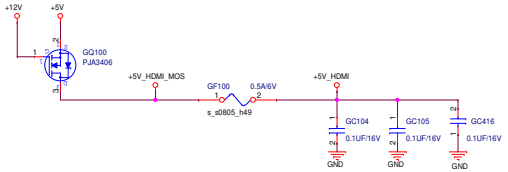




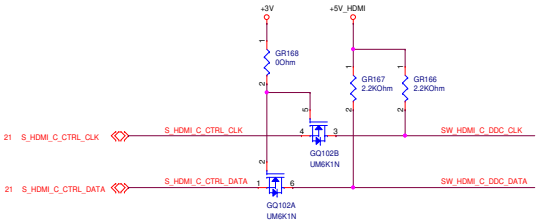
ASUS	Title : DP to VGA_IT6516B (Port B)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A4	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 31 of 75	

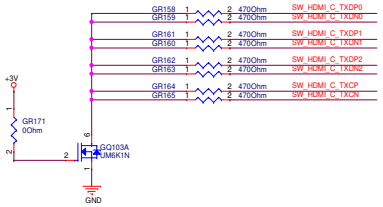


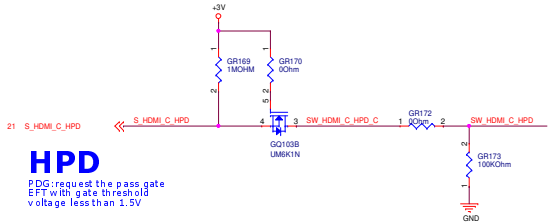
ASUSTeK COMPUTER INC.	Title : VGA	
	Engineer: IPC-EE3	
Size: A2	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 32 of 75	



Cost Reduced Level Shifter

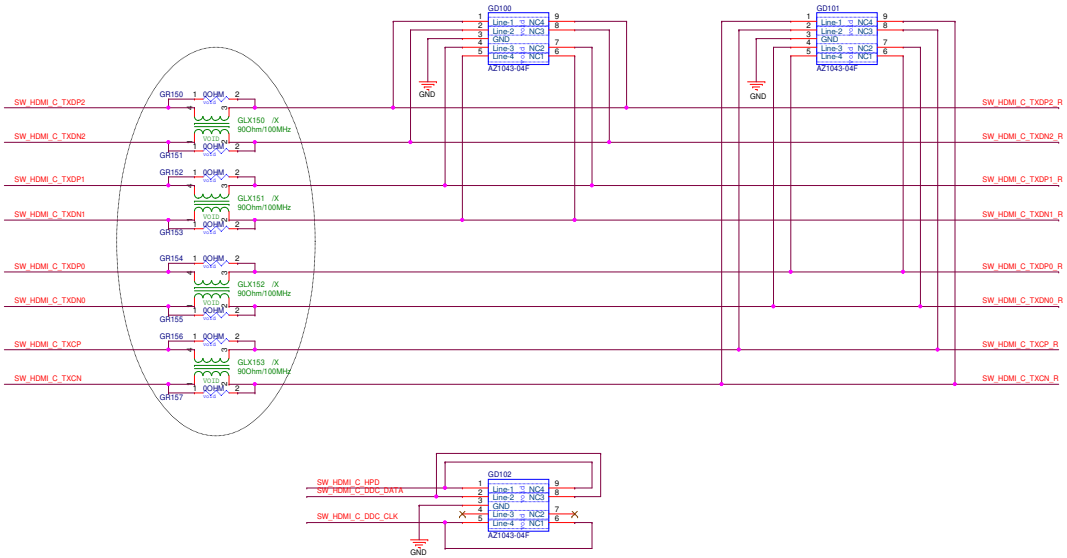


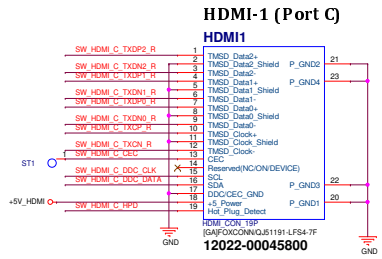




HPD

PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V



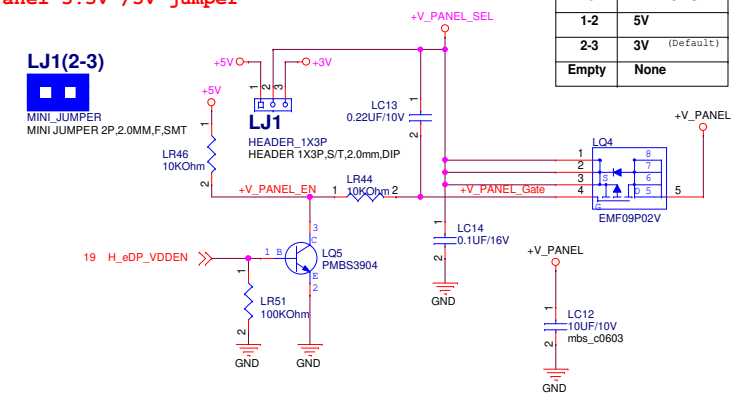


ESD connector

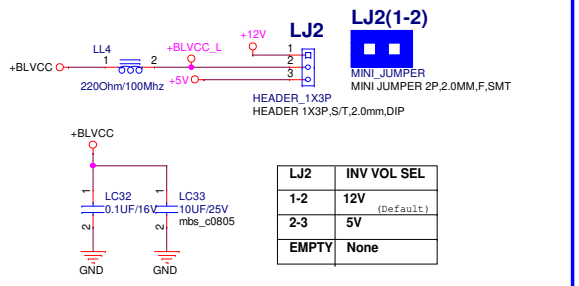
ASUSTek COMPUTER INC.	Title : HDMI-1 (Port C)	Engineer: IPC-EE3	
Size: A2	Project Name: MIX-Q370D2		Rev: R1.01
Date: Monday, February 17, 2020	Sheet 33 of 75		

Panel 3.3V /5V jumper

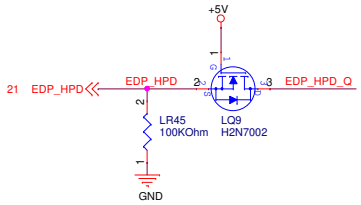
LJ1	PAN VOL SEL
1-2	5V
2-3	3V (Default)
Empty	None

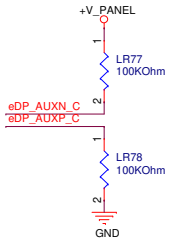


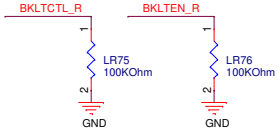
Panel backlight 12V /5V jumper

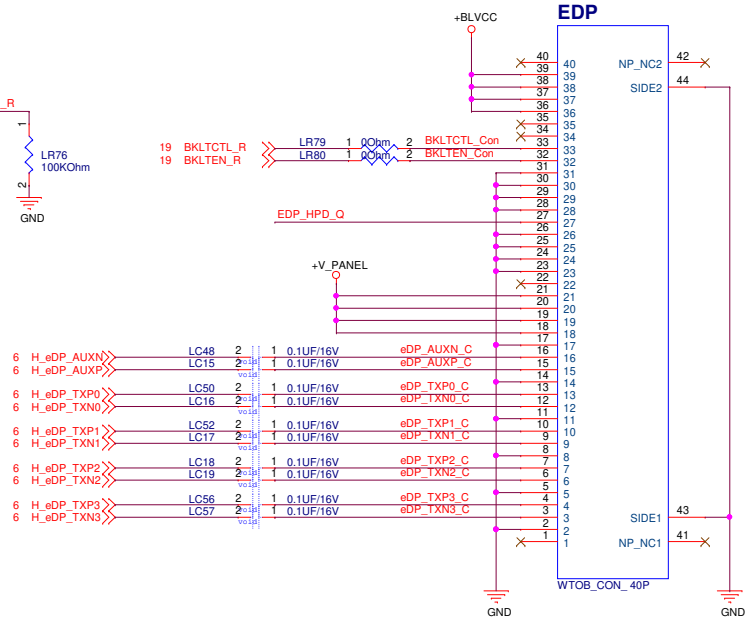


LJ2	INV VOL SEL
1-2	12V (Default)
2-3	5V
EMPTY	None

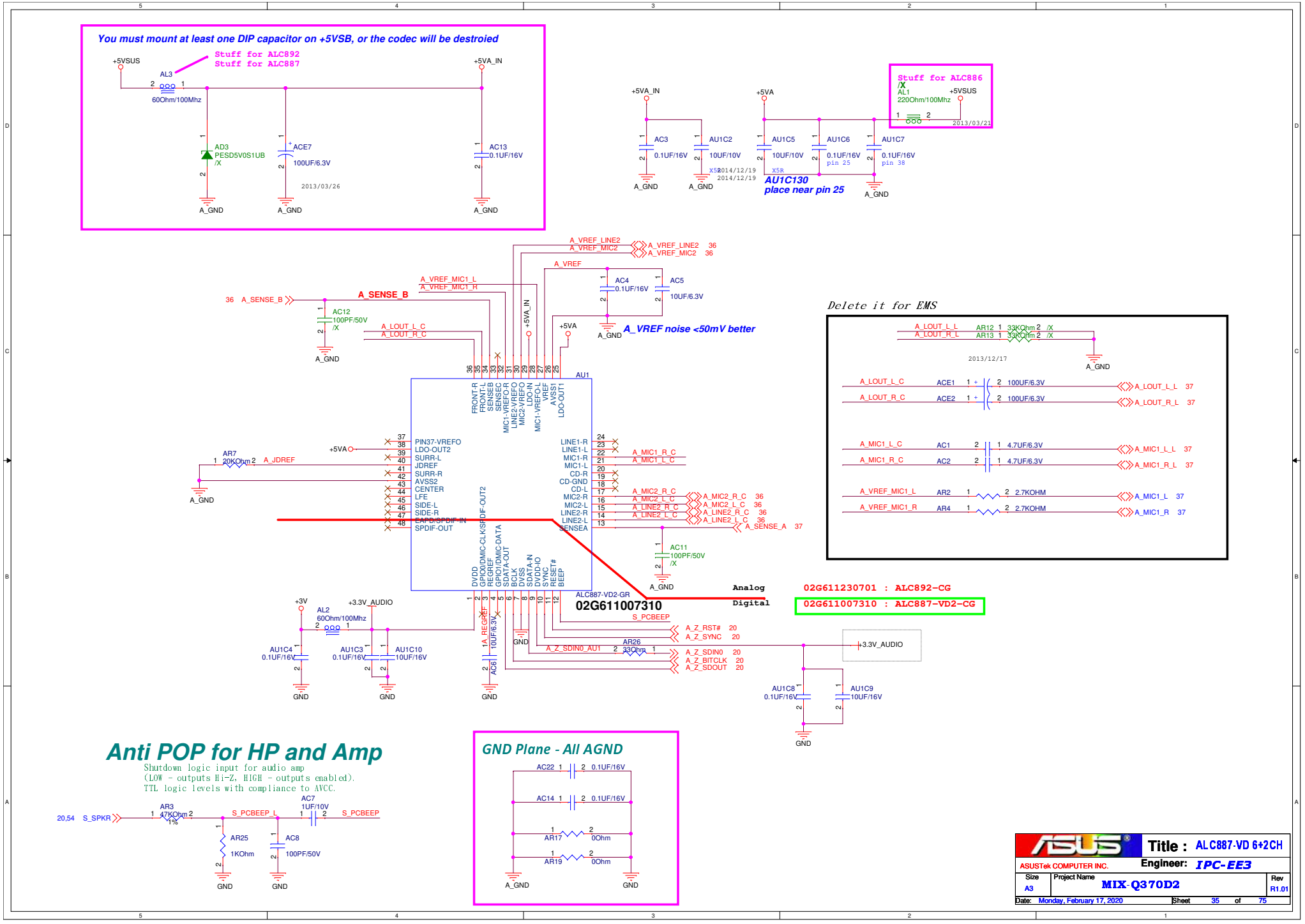


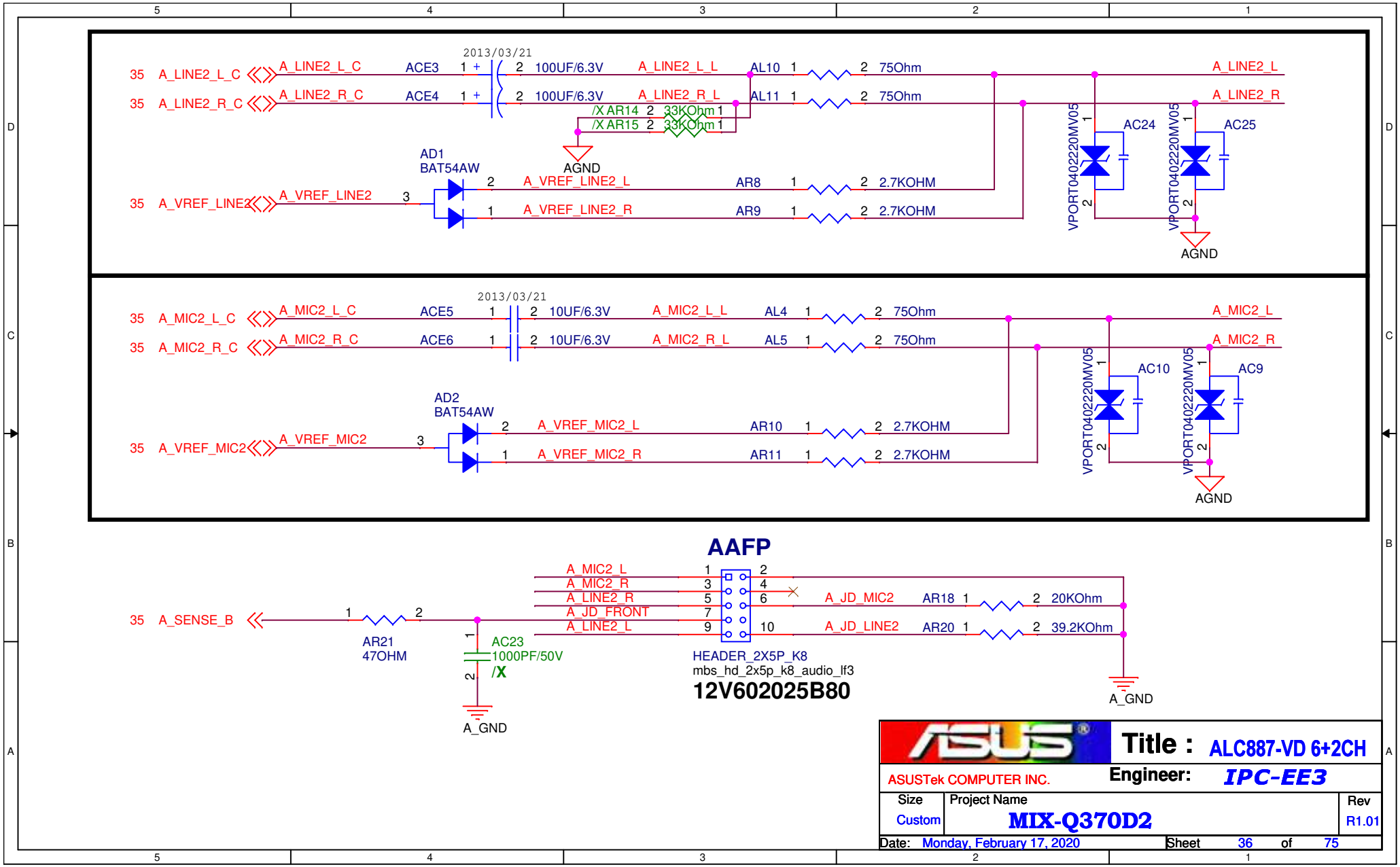






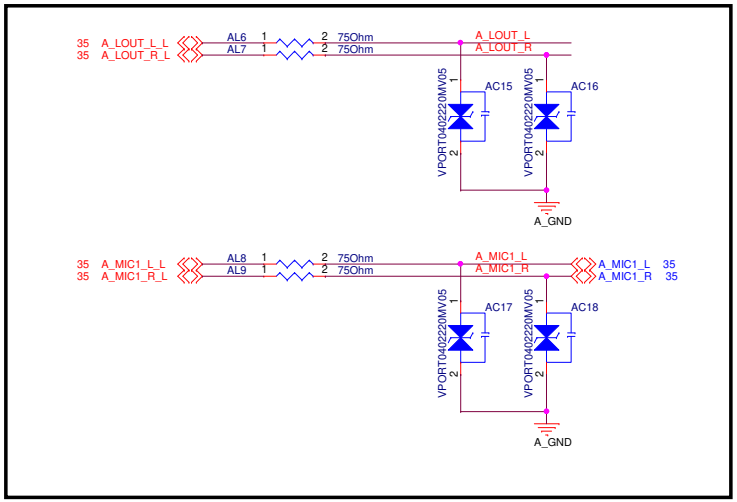
ASUSTek COMPUTER INC.	Title : eDP	
	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 34 of 75	


You must mount at least one DIP capacitor on +5VSB, or the codec will be destroied
Stuff for ALC892
Stuff for ALC887
+5VSUS
AL3
60Ohm/100Mhz
AD3
PESD5V0S1UB
/X
ACE7
100UF/6.3V
2013/03/26
+5VA_IN
AC13
0.1UF/16V
A_GND
Stuff for ALC886
/X
AL1
220Ohm/100Mhz
+5VSUS
2013/03/21
+5VA_IN
AC3
0.1UF/16V
AU1C2
10UF/10V
X5R
2014/12/19
+5VA
AU1C5
10UF/10V
AU1C6
0.1UF/16V
pin 25
AU1C7
0.1UF/16V
pin 38
AU1C130
place near pin 25
A_VREF_LINE2
A_VREF_MIC2
A_VREF
A_VREF_MIC1_L
A_VREF_MIC1_R
A_SENSE_B
AC12
100PF/50V
/X
A_LOUT_L_C
A_LOUT_R_C
AC4
0.1UF/16V
AC5
10UF/6.3V
A_VREF noise <50mV better
AU1
FRONT-R
FRONT-L
SENSEB
SENSEC
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
LDO-IN
MIC1-VREFO-L
VREF
AVSS1
LDO-OUT1
PIN37-VREFO
LDO-OUT2
SURR-L
JDREF
SURR-R
AVSS2
CENTER
LFE
SIDE-L
SIDE-R
EAPD/SPDIF-IN
SPDIF-OUT
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
SENSEA
DVDD
GPIO0/DMIC-CLK
REGREF
GPIO1/DMIC-DATA
SDATA-OUT
BCLK
DVSS
SDATA-IN
DVDD-IO
SYNC
RESET#
BEEP
AR7
20KOhm
A_JDREF
A_MIC1_R_C
A_MIC1_L_C
A_MIC2_R_C
A_MIC2_L_C
A_LINE2_R_C
A_LINE2_L_C
A_SENSE_A
AC11
100PF/50V
/X
ALC887-VD2-GR
02G611007310
Analog
Digital
02G611230701 : ALC892-CG
02G611007310 : ALC887-VD2-CG
S_PCBEEP
A_Z_RST#
A_Z_SYNC
A_Z_SDIN0_AU1
AR26
33Ohm
A_Z_SDIN0
A_Z_BITCLK
A_Z_SDOUT
+3V
AL2
60Ohm/100Mhz
+3.3V_AUDIO
AU1C4
0.1UF/16V
AU1C3
0.1UF/16V
AU1C10
10UF/16V
1A_REGREF
10UF/6.3V
AC6
AU1C8
0.1UF/16V
AU1C9
10UF/16V
GND
Delete it for EMS
A_LOUT_L_L
A_LOUT_R_L
AR12
AR13
33KOhm
2013/12/17
ACE1
ACE2
100UF/6.3V
AC1
AC2
4.7UF/6.3V
AR2
AR4
2.7KOHM
A_MIC1_L
A_MIC1_R
Anti POP for HP and Amp
Shutdown logic input for audio amp
(LOW - outputs Hi-Z, HIGH - outputs enabled).
TTL logic levels with compliance to AVCC.
S_SPKR
AR3
47KOhm
1%
S_PCBEEP_L
AC7
1UF/10V
S_PCBEEP
AR25
1KOhm
AC8
100PF/50V
GND Plane - All AGND
AC22
0.1UF/16V
AC14
AR17
0Ohm
AR19
0Ohm
A_GND
GND
Title : ALC887-VD 6+2CH
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A3
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 35 of 75



ASUS	Title : ALC887-VD 6+2CH		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.01
Date: Monday, February 17, 2020	Sheet 36 of 75		

Delete it for EMS

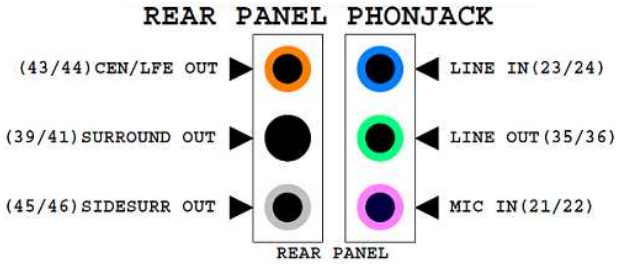


SPDIF Optical

A-11

SPDIF Optical (High Rise)

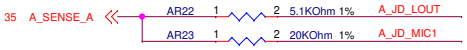
A-12

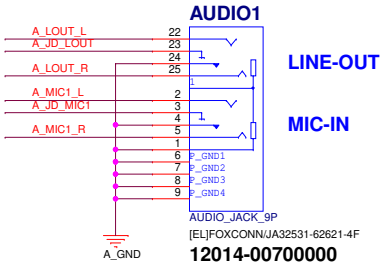


ALC889/ALC892/ALC898 Configuation (7.1 Channel)

Rear Panel: 6 dedicated audio jacks
Front Panel: 2 re-tasking audio jacks

Pin Assignment	Location	Function
FRONT(pin-35,36)/Port-D	Rear Panel	Front-Out, HP-Out
SURR (pin-39,41)/Port-A	Rear Panel	Surr-Out
CEN/LFE (pin-43,44)/Port-G	Rear Panel	Cen/Lfe-Out
SIDE (pin-45,46)/Port-H	Rear Panel	Side-Surr Out
LINE1 (pin-23,24)/Port-C	Rear Panel	Line-In
MIC1 (pin-21,22)/Port-B	Rear Panel	Mic-In
LINE2 (pin-14,15)/Port-E	Front Panel	HP-Out, Line-In, Mic-In
MIC2 (pin-16,17)/Port-F	Front Panel	Mic-In, HP-Out, Line-In





ASUSTek COMPUTER INC.	Title : ALC887-VD 6+2CH	
	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 37 of 75	

ASUS	Title : EUA2012AJIR1		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.01
Date: Monday, February 17, 2020	Sheet 38 of 75		

若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.

R1.00
Ref to page.104 +5VDUAL/5V_DUAL_USBKB*

+L1_I219_+3VSB
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.

1.3

Standard Circuit	
LAN	I218V
REV.	L1_1.3

/X

I218V

PCIE IF
勿接在chipset PCIE port0

16 C_PCIE_L1
16 C_PCIE_L1#
18 X_L1X1_RXP
18 X_L1X1_RXN
18 X_L1X1_TXP
18 X_L1X1_TXN

L1CX1 2 — 1 0.1UF/16V X7R — X_L1X1_RXP_C 38
L1CX2 void 2 — 1 0.1UF/16V X7R — X_L1X1_RXN_C 39
Close to PHY
SL1CX3 2 — 1 0.1UF/16V X7R — X_L1X1_TXP_C 41
SL1CX4 void 2 — 1 0.1UF/16V X7R — X_L1X1_TXN_C 42
Close to Chipset

L1U1

PE_CLKP 44
PE_CLKN 45
PETp 38
PETn 39
PERp 41
PERn 42

20 L1_SMBCLK
20 L1_SMBDATA

L1C1 2 — 1 15PF/50V NPO /X
L1C2 2 — 1 15PF/50V NPO /X
Close to PHY
GND

SMB_CLK 28
SMB_DATA 31

20 L1_LAN_DISABLE#
LAN_DISABLE_N 3

2015/04/16
L1R100 1 — 2 8.2KOhm
L1R101 1 — 2 8.2KOhm /X
+L1_I219_+3VSB
GND

L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.

L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

+L1_I219_+3VSB
LT1 — L1_TP_JDI 32
LT2 — L1_TP_TDO 34
L1_TMS 33
L1_TCK 35
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
L1R18 1 — 8.2KOhm 2 /X
L1R19 1 — 8.2KOhm 2 /X

L1R20 1 — 2.7KOHM 2 — L1_TESTEN 30
TEST_EN
CRB 1K
GND

+L1_I219_+3VSB
CRB : L1R3 UNSTUFF FOR LPT-H
L1R9 10KOhm 1 — 2 — L1_CLKREQN 48
CLK_REQ_N
L1R3 0Ohm 2 — 1
16 CLK_REQ2_LAN#

17,28,41,52 S_PLTRST# — PE_RST_N 36
L1C29 2 — 1 10PF/50V NPO /X
GND

Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0

+L1_I219_0.9V
L1U1C8 0.1UF/16V /X
L1U1C16 0.1UF/16V /X
L1U1C40 0.1UF/16V /X
L1U1C47 0.1UF/16V /X
GND

VDD0P9_46 46
VDD0P9_47 47
VDD0P9_37 37
VDD0P9_43 43
VDD0P9_11 11
VDD0P9_8 8
VDD0P9_40 40
VDD0P9_22 22
VDD0P9_16 16

L1L1 4.7UH 1 — 2 — L1_CTRLP 7
CTRL0P9
L1U1C50 10UF/16V /X
L1U1C49 0.1UF/16V
L1U1C7 22UF/6.3V X5R
GND
L1L1
Idc_min=500 mA
Rdc_max=100 mohm
Placement rule:
1.Place close to L1U1
2.Trace length < 500mil
3.Trace wide > 20mil

GND1 50
GND2 51
GND3 52
GND4 53
WGI219V
06112-00020000
GND

MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch

MDI_PLUS[0] 13 — L1_MDI_0+ 40
MDI_MINUS[0] 14 — L1_MDI_0- 40
MDI_PLUS[1] 17 — L1_MDI_1+ 40
MDI_MINUS[1] 18 — L1_MDI_1- 40
MDI_PLUS[2] 20 — L1_MDI_2+ 40
MDI_MINUS[2] 21 — L1_MDI_2- 40
MDI_PLUS[3] 23 — L1_MDI_3+ 40
MDI_MINUS[3] 24 — L1_MDI_3- 40

XTAL_OUT 9 — L1_XOUT
XTAL_IN 10 — L1_XIN
L1R6 0Ohm 2 — 1 — L1_XOUT_R
L1X1 25MHZ [HF]TROQ/RL25000866 SMD 07009-00024400
L1C3 10PF/50V NPO
L1C4 10PF/50V NPO
GND

L1X1,L1C7,L1C8
Placement rule:
1.Place close to L1U1
2.Trace length <1inch

+L1_I219_+3VSB
L1R2 300OHM
L1_ACTLEDP 40

LED2 25 — L1_LED2
LED1 27
LED0 26
L1R1 1 — 2 300OHM
L1_LINK100# 40
L1_LINK1000# 40
L1_ACTLEDN 40

CRB pull up 4.7Kohm
VDD3P3_IN 5
Close to pin5
L1U1C5 0.1UF/16V
L1U1C48 22UF/6.3V X5R
GND
+L1_I219_+3VSB
L1R21 4.7KOhm 1%
L1R4 4.7KOHM /X
L1R22 4.7KOhm 1%

RSVD1_VCC3P3 1 — L1_RSVD
LANWAKE_N 2
SVR_EN_N 6 — L1_SVR_EN
L1_LAN_WAKE# 20
L1R26 0Ohm
GND

L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電

L1_LAN_WAKE#
Must be connected to PCH's LANWAKE

+L1_I219_+3VSB
VDD3P3_4 4
VDD3P3_15 15
VDD3P3_19 19
VDD3P3_29 29
L1U1C4 1UF/16V
GND

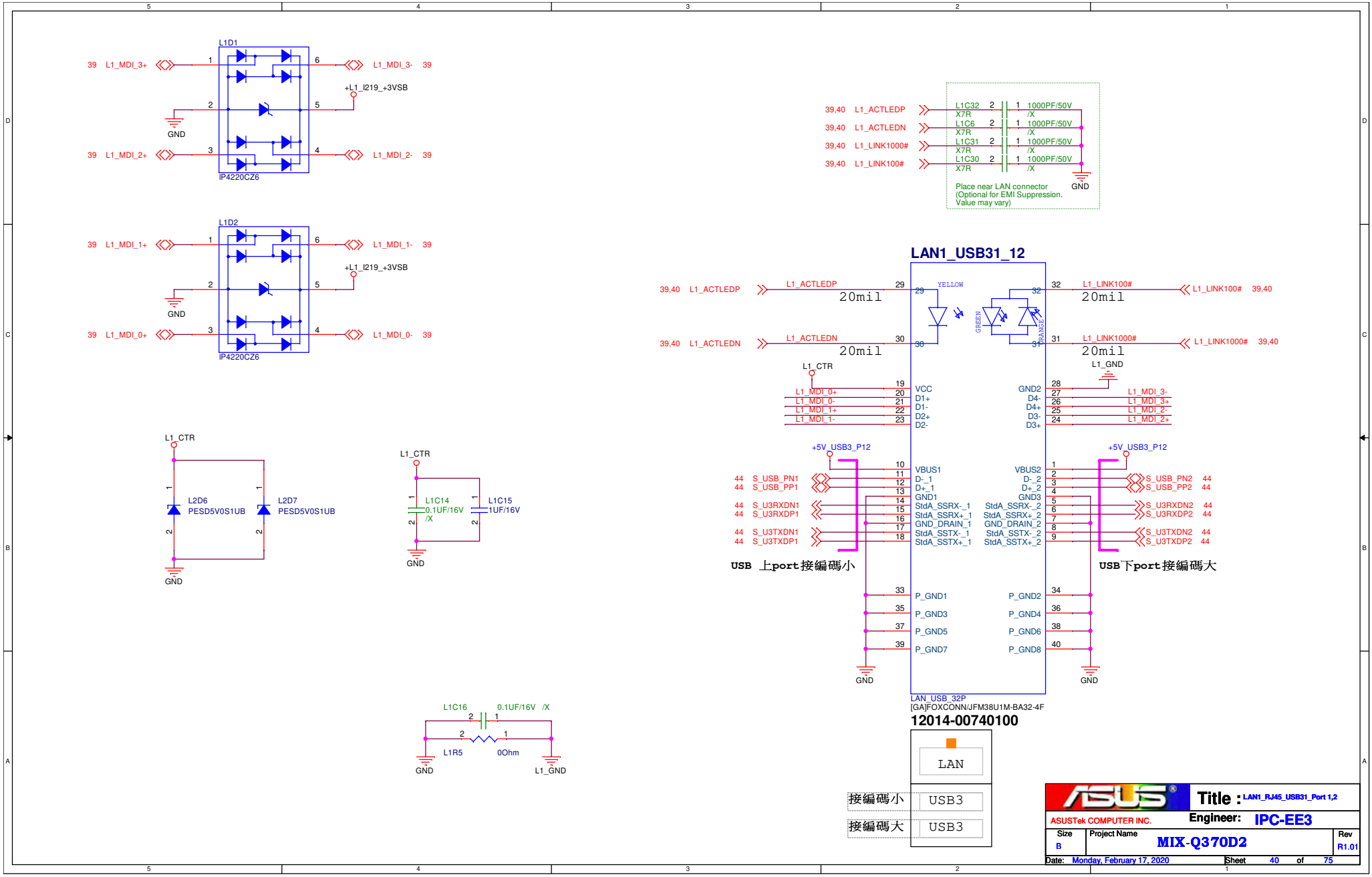
RBIAS 12 — L1_RBIAS
GND_EPAD 49
L1R16 1 — 2 3.01KOHM 1%
GND

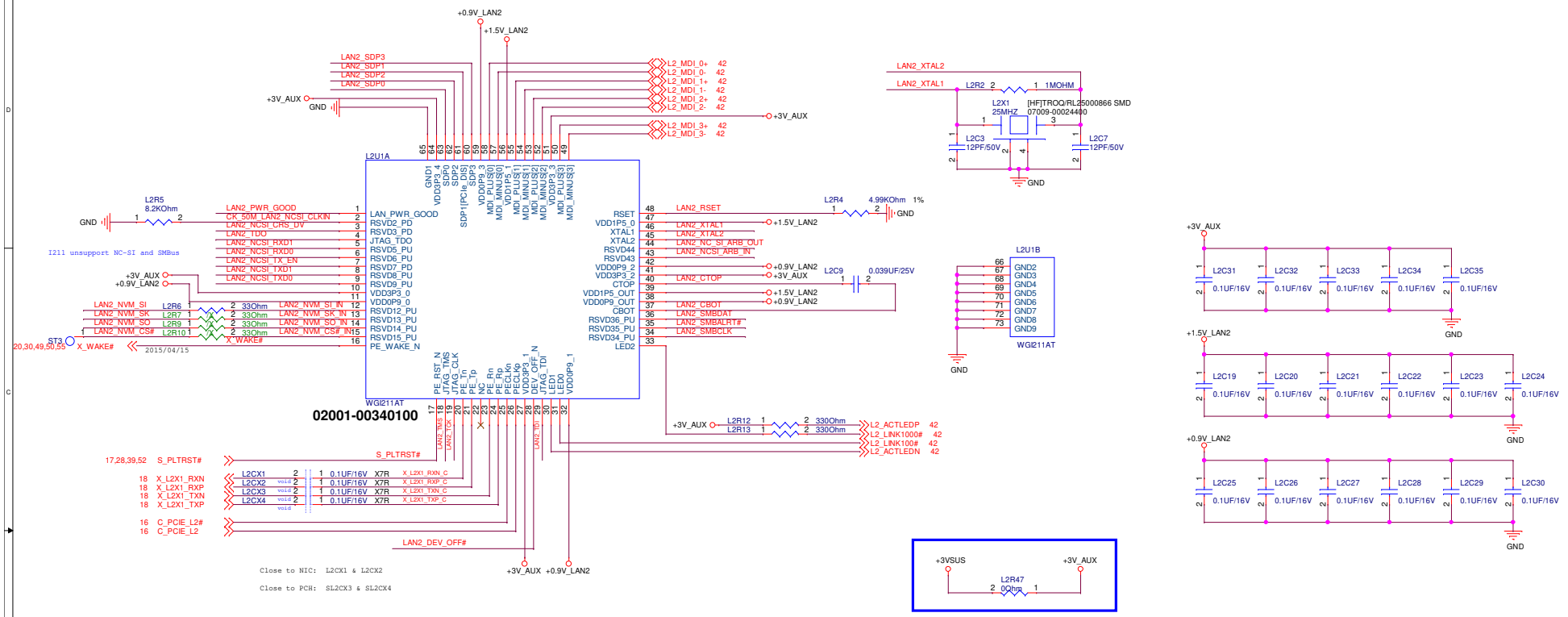
L1R16
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch

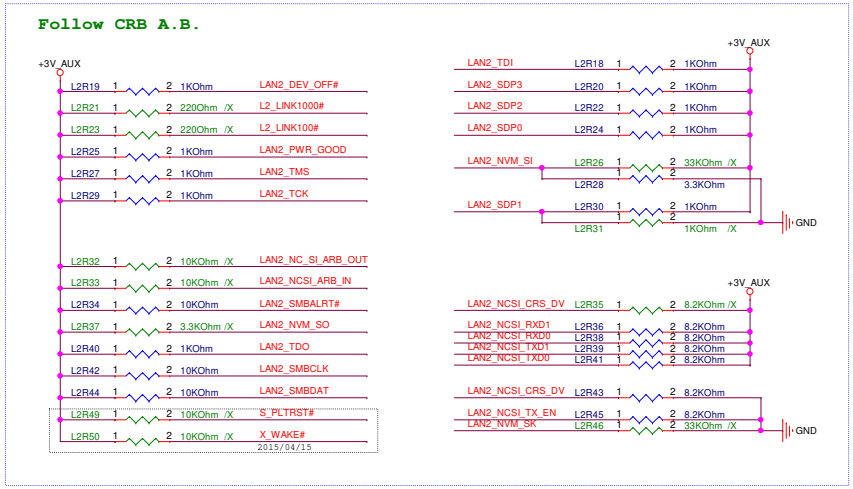
06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)

06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)

ASUS	Title : L1_I219V		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 39 of 75		


L1D1
39 L1_MDI_3+
L1_MDI_3- 39
+L1_I219_+3VSB
GND
39 L1_MDI_2+
L1_MDI_2- 39
IP4220CZ6
L1D2
39 L1_MDI_1+
L1_MDI_1- 39
+L1_I219_+3VSB
GND
39 L1_MDI_0+
L1_MDI_0- 39
IP4220CZ6
39,40 L1_ACTLEDP
39,40 L1_ACTLEDN
39,40 L1_LINK1000#
39,40 L1_LINK100#
L1C32 X7R 1000PF/50V /X
L1C6 X7R 1000PF/50V /X
L1C31 X7R 1000PF/50V /X
L1C30 X7R 1000PF/50V /X
Place near LAN connector
(Optional for EMI Suppression.
Value may vary)
GND
LAN1_USB31_12
L1_ACTLEDP 20mil
L1_ACTLEDN 20mil
L1_LINK100# 20mil
L1_LINK1000# 20mil
YELLOW
GREEN
ORANGE
L1_CTR
L1_GND
VCC
D1+
D1-
D2+
D2-
GND2
D4-
D4+
D3-
D3+
L1_MDI_0+
L1_MDI_0-
L1_MDI_1+
L1_MDI_1-
L1_MDI_3-
L1_MDI_3+
L1_MDI_2-
L1_MDI_2+
+5V_USB3_P12
VBUS1
D-_1
D+_1
GND1
StdA_SSRX-_1
StdA_SSRX+_1
GND_DRAIN_1
StdA_SSTX-_1
StdA_SSTX+_1
VBUS2
D-_2
D+_2
GND3
StdA_SSRX-_2
StdA_SSRX+_2
GND_DRAIN_2
StdA_SSTX-_2
StdA_SSTX+_2
S_USB_PN1
S_USB_PP1
S_U3RXDN1
S_U3RXDP1
S_U3TXDN1
S_U3TXDP1
S_USB_PN2
S_USB_PP2
S_U3RXDN2
S_U3RXDP2
S_U3TXDN2
S_U3TXDP2
USB 上port接編碼小
USB下port接編碼大
P_GND1
P_GND3
P_GND5
P_GND7
P_GND2
P_GND4
P_GND6
P_GND8
GND
LAN_USB_32P
[GA]FOXCONN/JFM38U1M-BA32-4F
12014-00740100
L2D6 PESD5V0S1UB
L2D7 PESD5V0S1UB
L1C14 0.1UF/16V /X
L1C15 1UF/16V
L1C16 0.1UF/16V /X
L1R5 0Ohm
L1_GND
LAN
接編碼小 USB3
接編碼大 USB3
ASUS
Title : LAN1_RJ45_USB31_Port 1,2
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size B
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 40 of 75





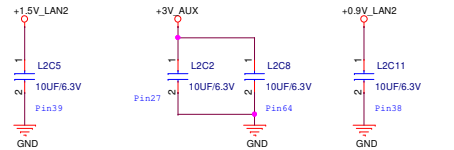
Strapping Options

```
DEV_OFF_N
 I210.28 (DEV_OFF_N)
   1: Exit Device off mode (Default)
   0: Enter Device off mode

AUX_PWR
 I210.28 (DEV_OFF_N)
 I210.60 (SDP3)
   11: Enable AUX power mode (Default)

Security_EN
 I210.12 (NVM_SI)
   1: Enable Flash security
   0: Disable Flash security (Default)

PCIE_DIS_N
 I210.61 (SDP1[PCIe_DIS])
   1: Enable PCIe function (Default)
   0: Disable PCIe function
```

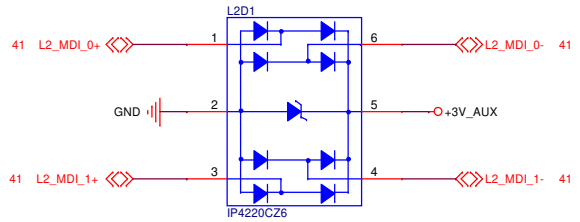


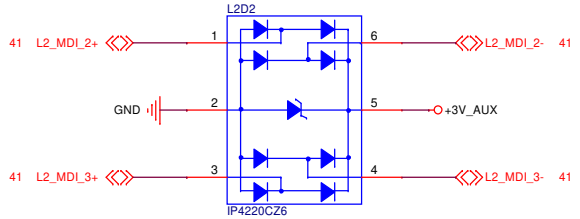
3.4 Voltage Regulator

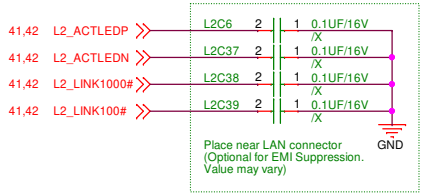
To reduce Bill of Material (BOM) cost, the I211 supports generating the 1.5V and 0.9V power supplies from the 3.3V supply using an on-chip Switching Capacitor Voltage Regulator (SVR) control circuit, which requires only an external capacitor component.

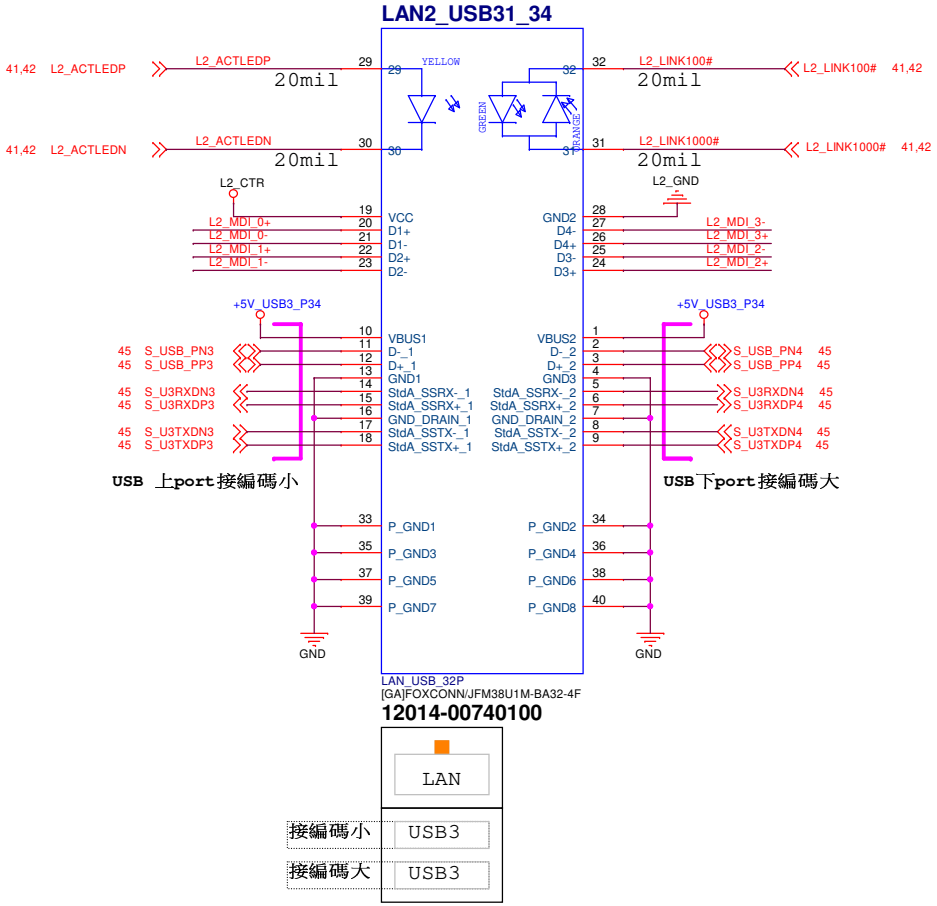
Refer to Section 10.6.4 for more details.

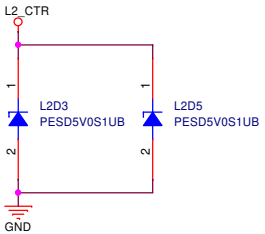
ASUS	Title : LAN2_I210-AT		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.01
Date: Monday, February 17, 2020	Sheet 41 of 75		

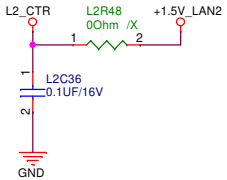


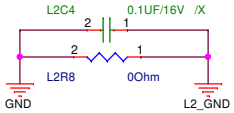




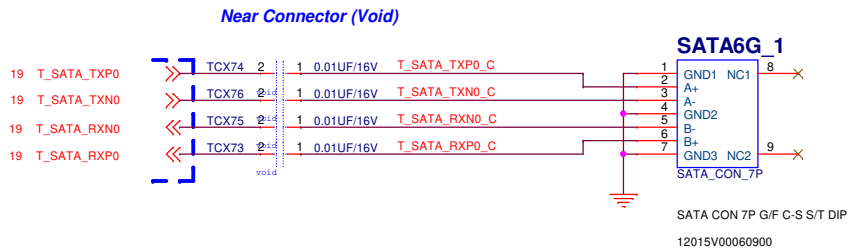


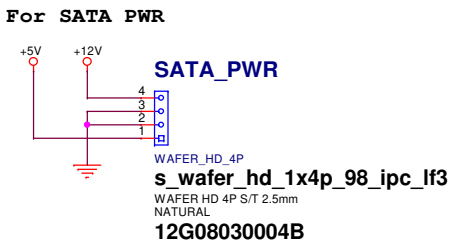


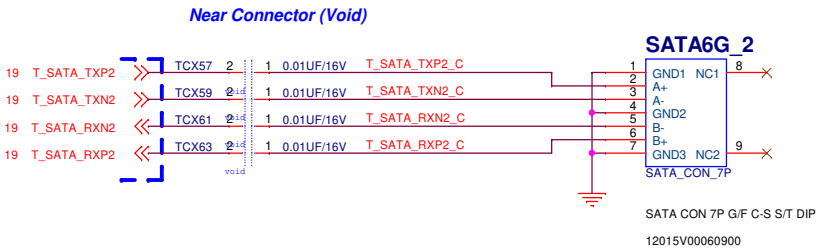




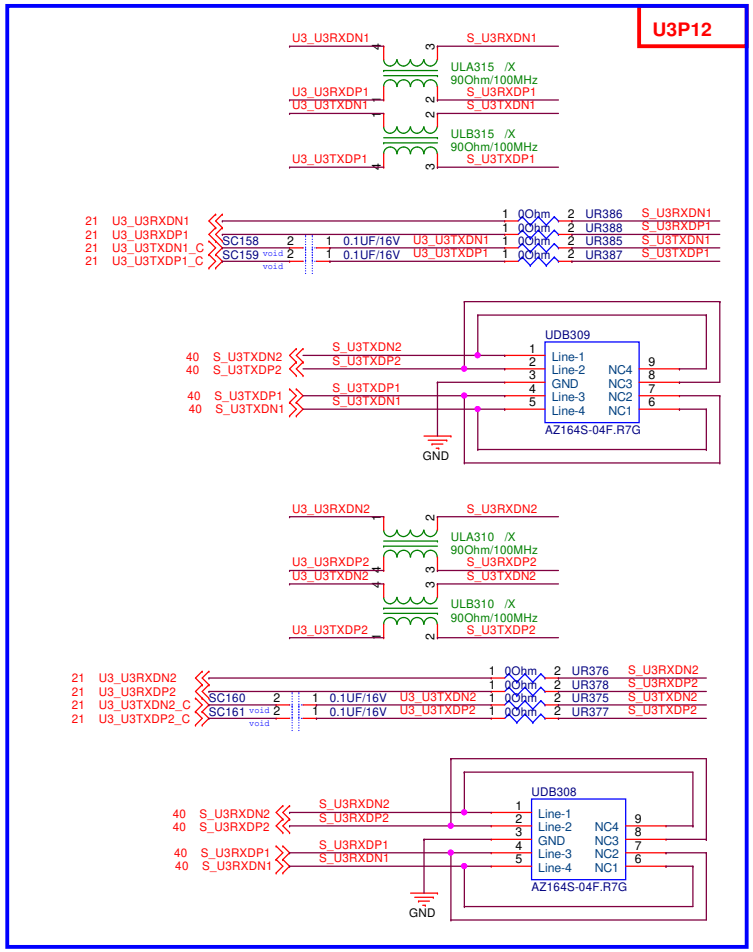
ASUS	Title : LAN2_RJ45_USB31_Port 3,4	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 42 of 75	

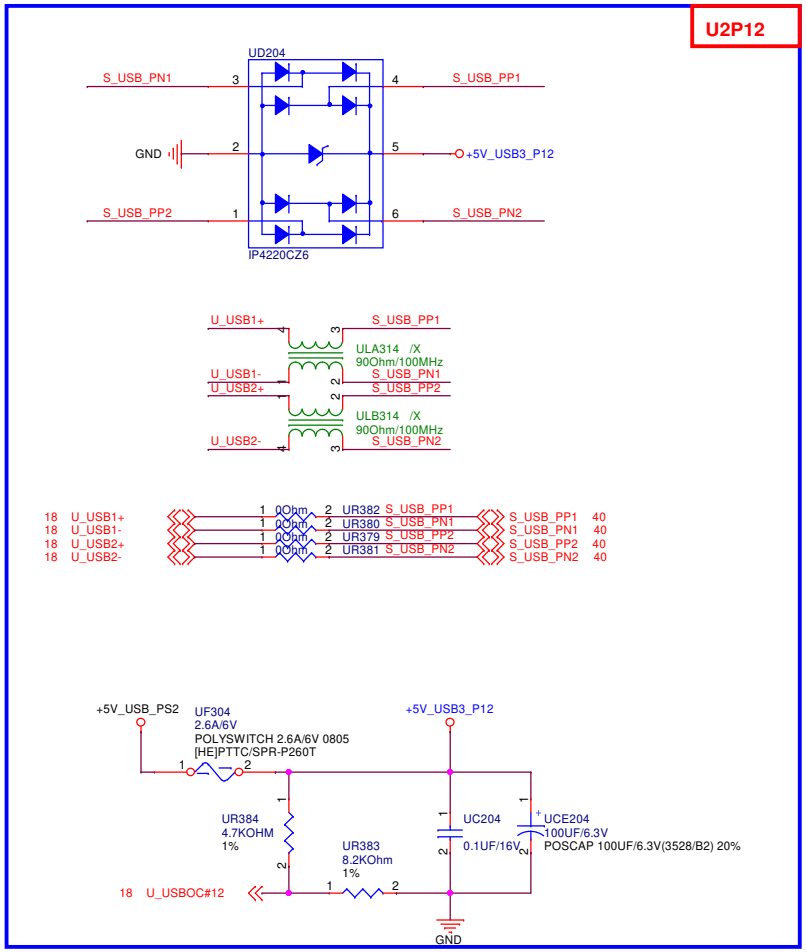


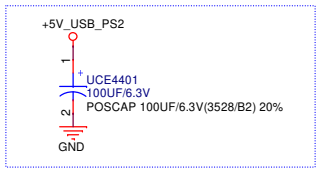




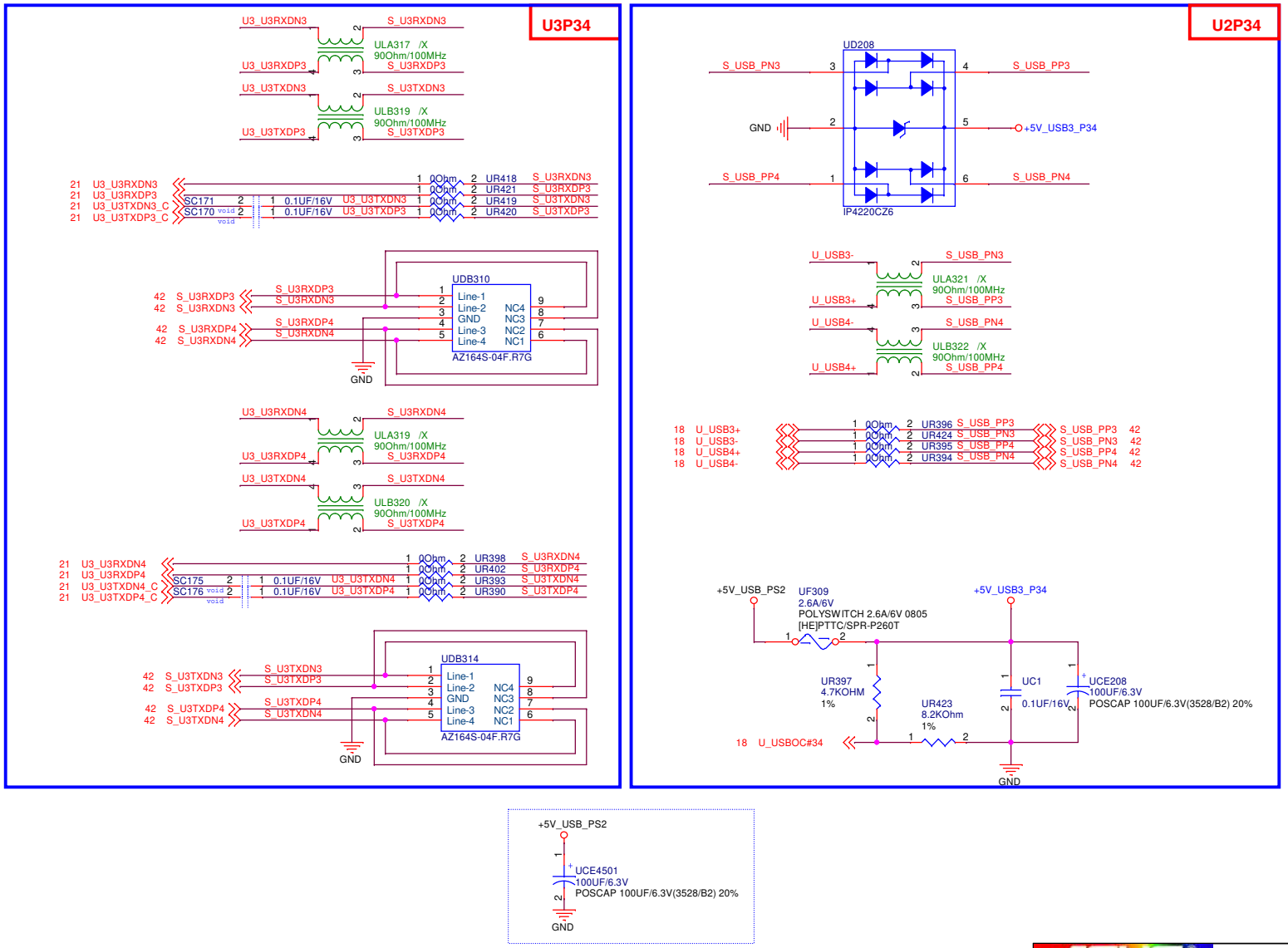
ASUSTek COMPUTER INC.	Title : SATA6G_12345(CHIPSET)	Engineer: IPC-EE3
Size B	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 43 of 75	



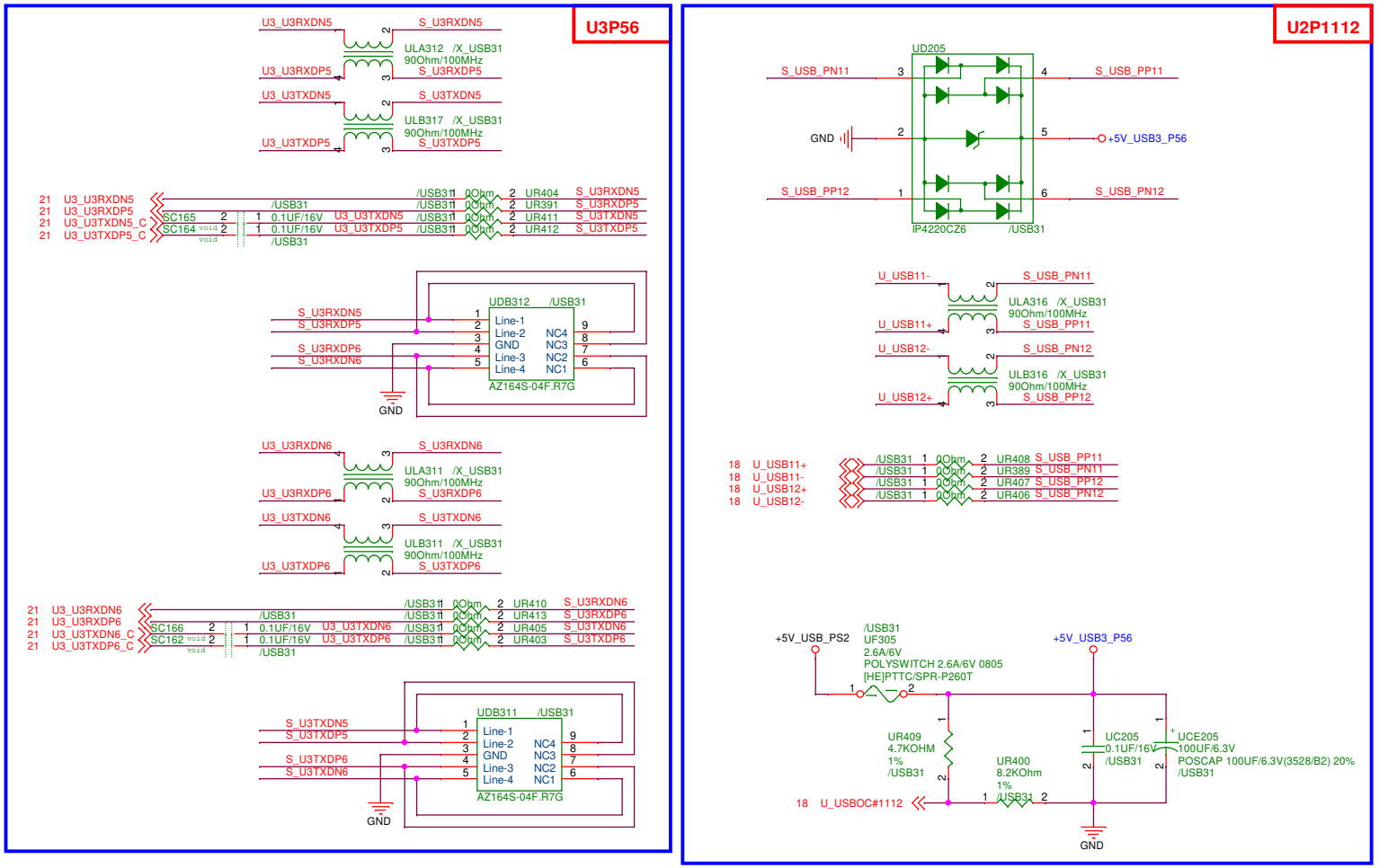




ASUS	Title : USB31 Port 1,2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 44 of 75	



ASUSTek COMPUTER INC.	Title : USB31 Port 3,4	Engineer: IPC-EE3
Size: B	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 45 of 75	



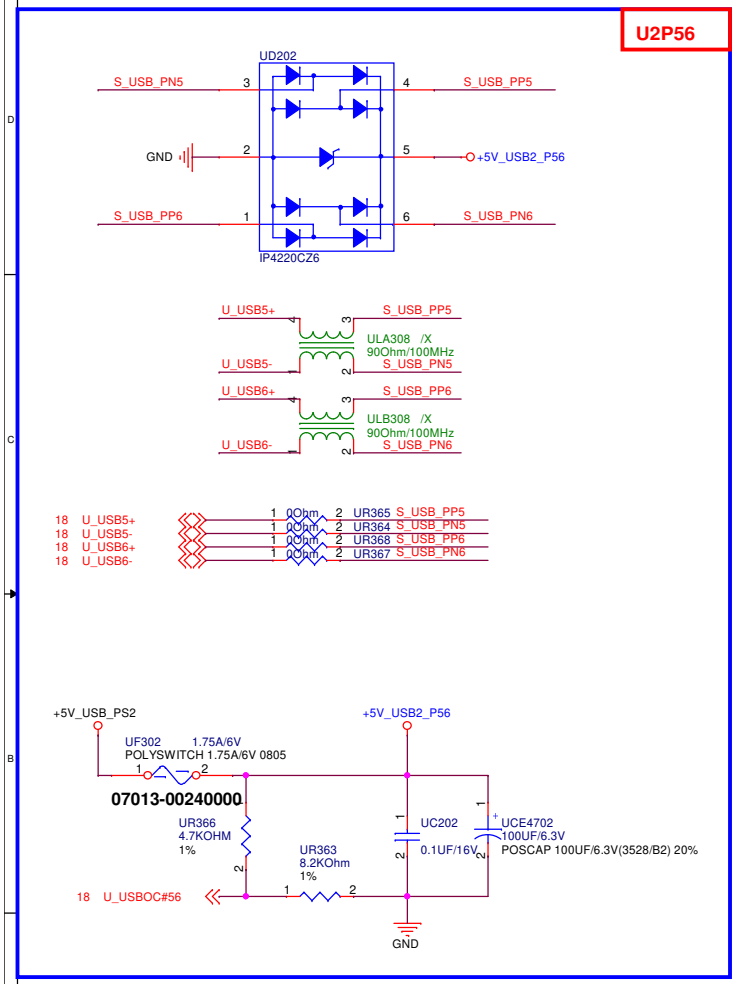
ASUSTek COMPUTER INC.

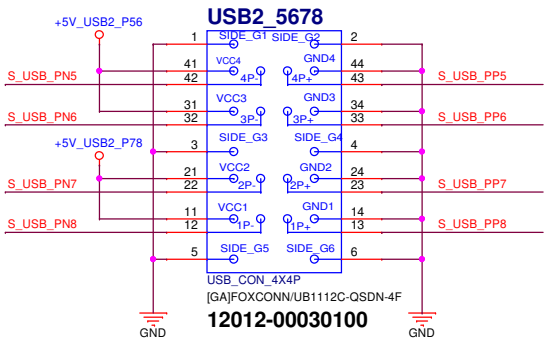
Title : USB31 Port 5,6

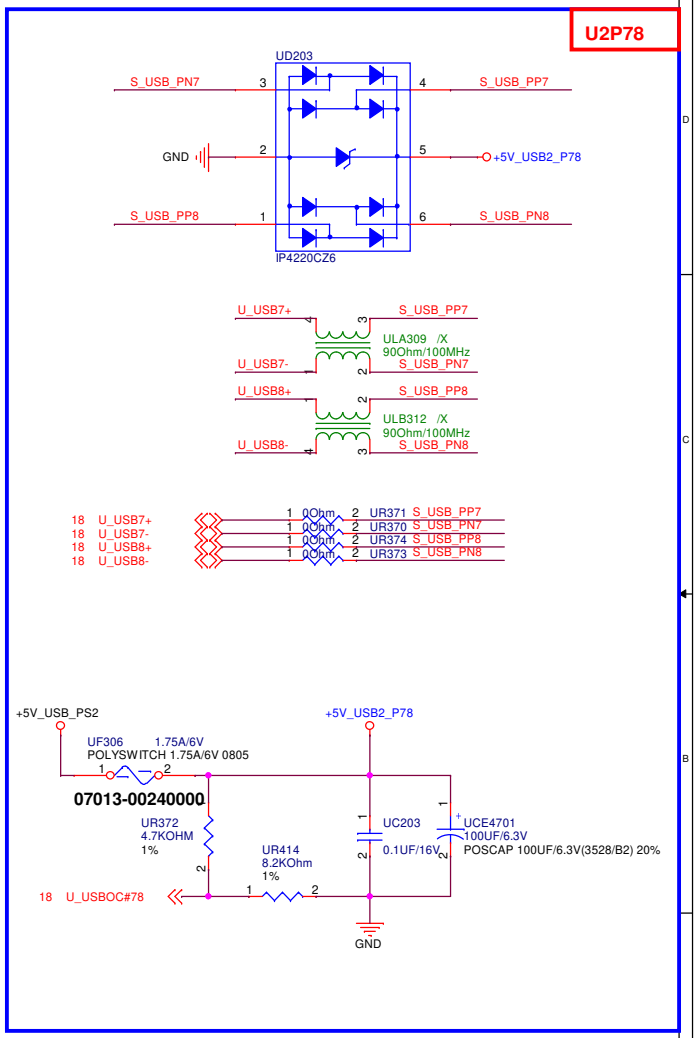
Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.01

Date: Monday, February 17, 2020 Sheet 46 of 75







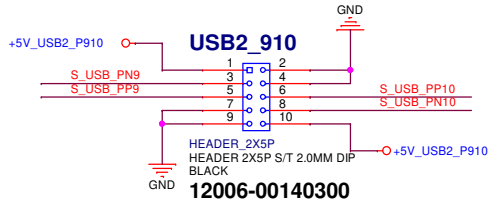
ASUSTek COMPUTER INC.

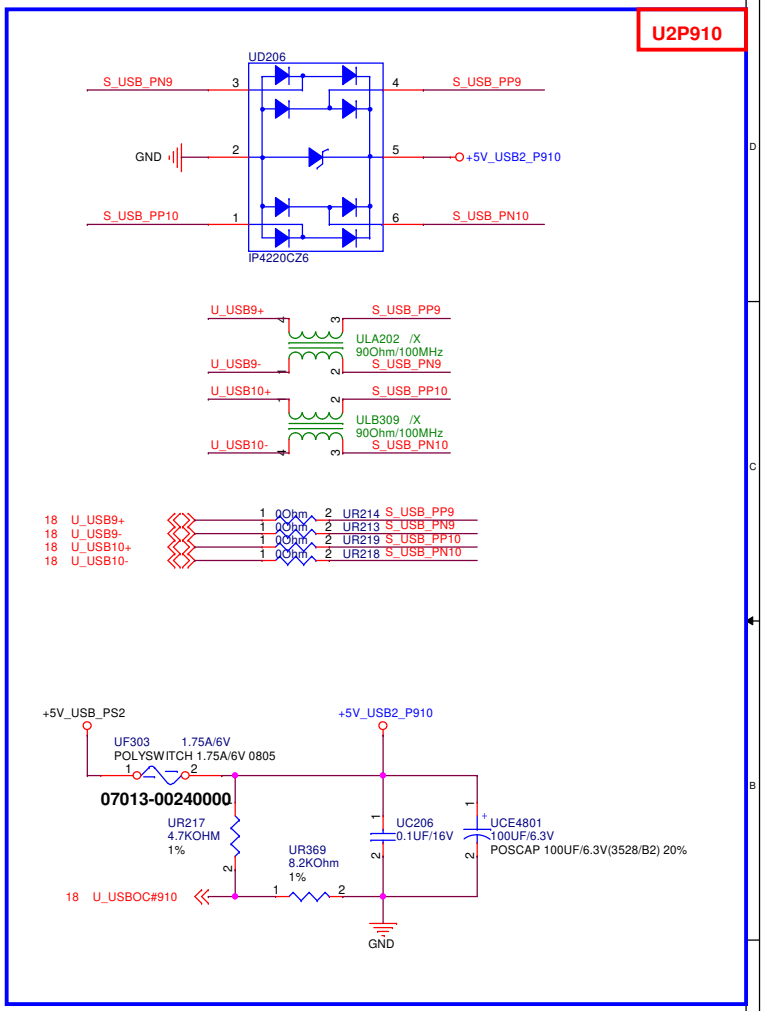
Title : USB2 Port 5,6,7,8

Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.01

Date: Monday, February 17, 2020 Sheet 47 of 75





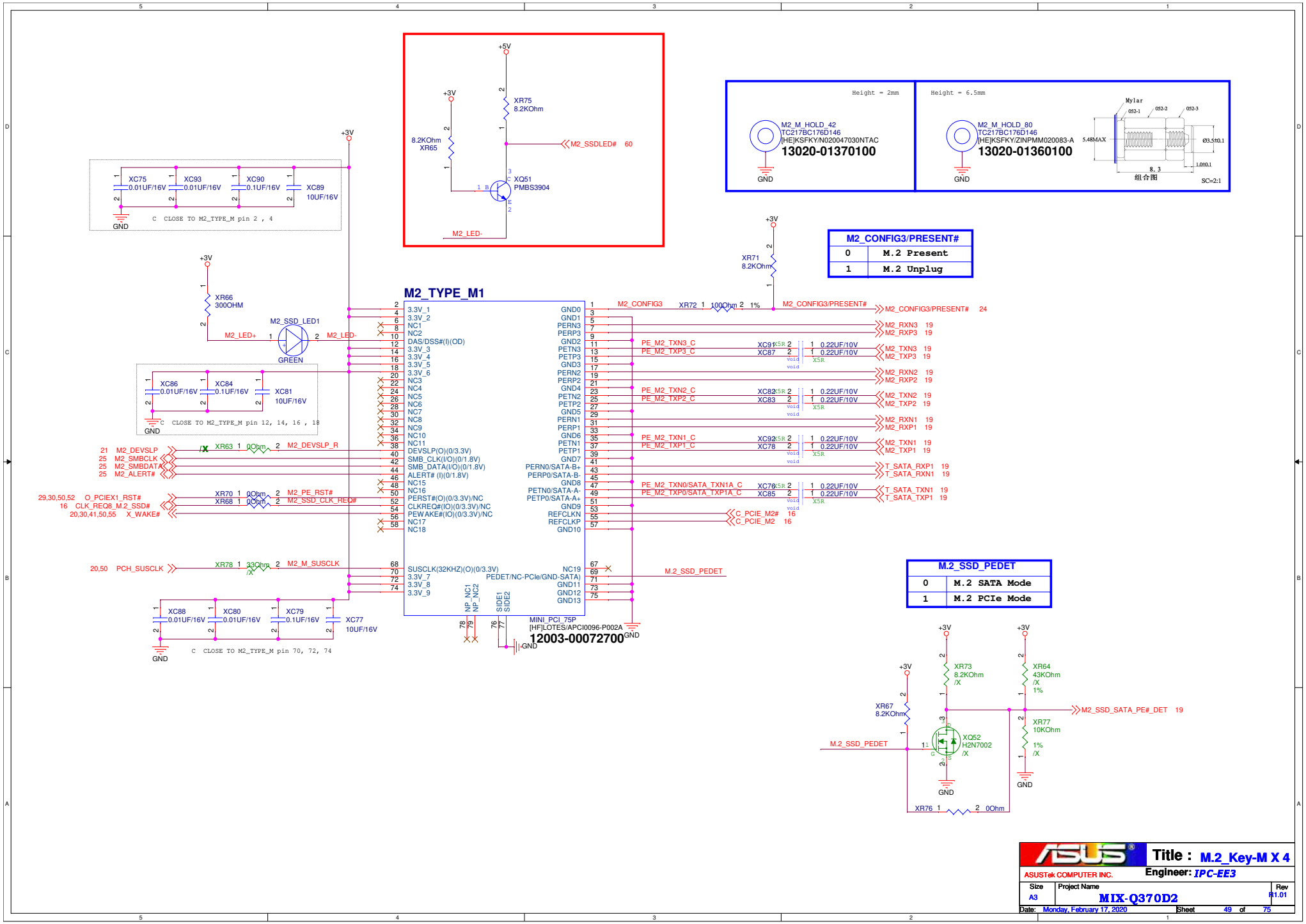
ASUSTek COMPUTER INC.

Title : USB2 Port 9,10 (Internal)

Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.01

Date: Monday, February 17, 2020 Sheet 48 of 75



M2_CONFIG3/PRESENT#	
0	M.2 Present
1	M.2 Unplug

M.2_SSD_PEDET	
0	M.2 SATA Mode
1	M.2 PCIe Mode

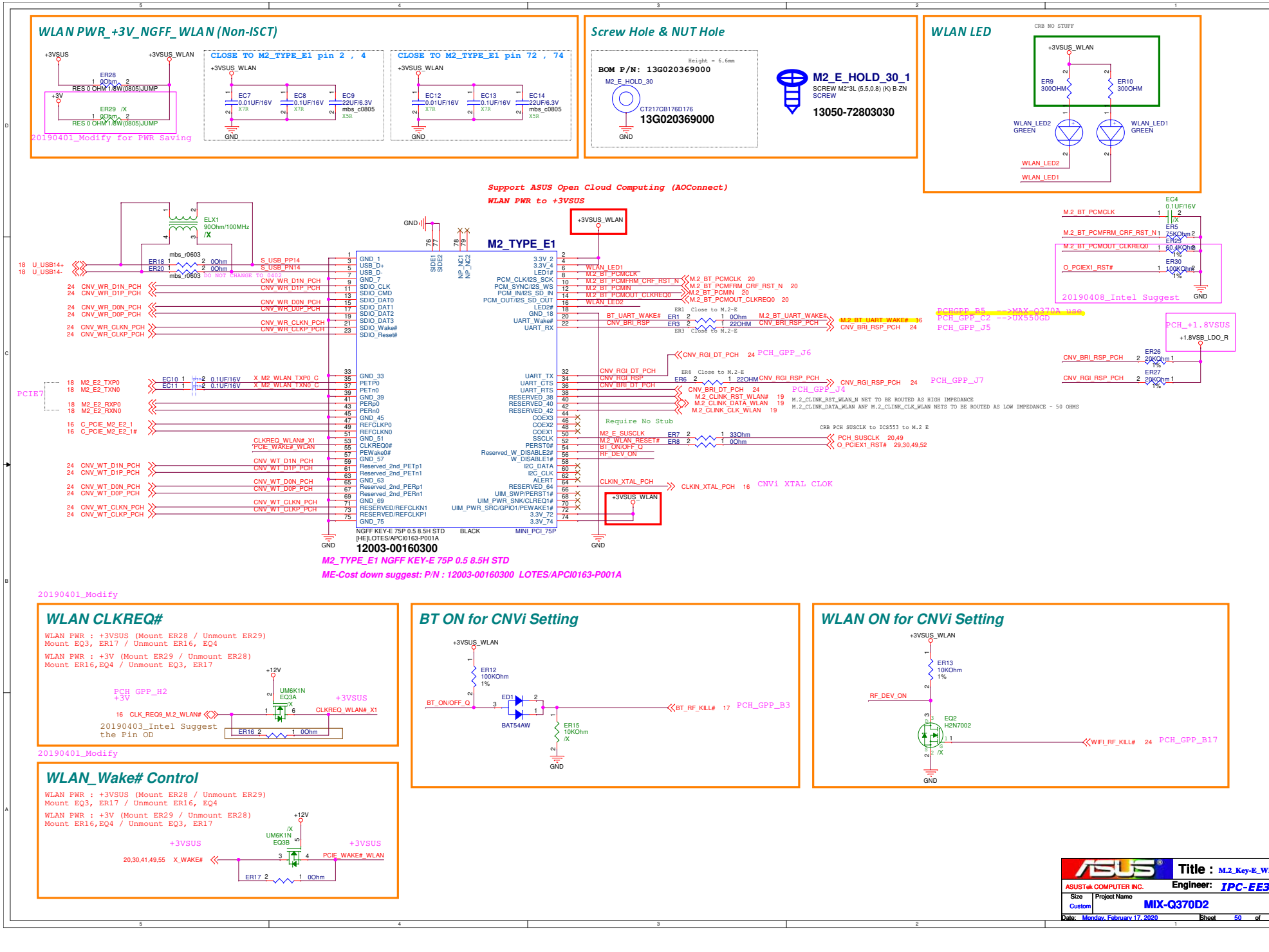
ASUSTek COMPUTER INC.

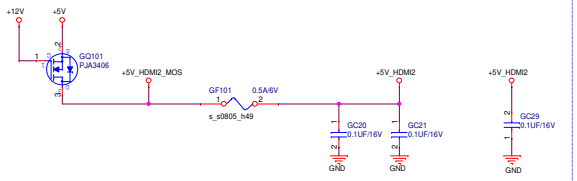
Title : M.2_Key-M X 4

Engineer: IPC-EE3

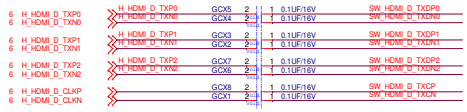
Size	Project Name	Rev
A3	MIX-Q370D2	R1.01

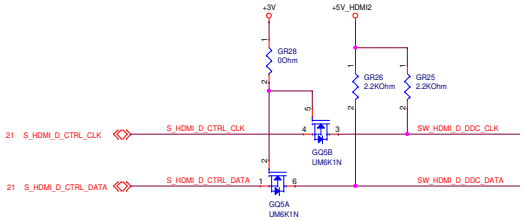
Date: Monday, February 17, 2020 Sheet 49 of 75

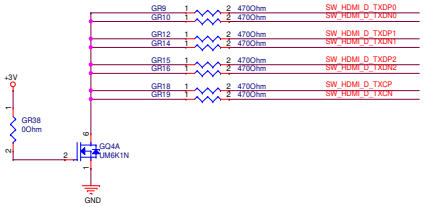

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)
+3VSUS
+3VSUS_WLAN
ER28 0Ohm
RES 0 OHM 1/8W(0805)JUMP
+3V
ER29 /X 0Ohm
RES 0 OHM 1/8W(0805)JUMP
20190401_Modify for PWR Saving
CLOSE TO M2_TYPE_E1 pin 2 , 4
EC7 0.01UF/16V X7R
EC8 0.1UF/16V X7R
EC9 22UF/6.3V mbs_c0805 X5R
GND
CLOSE TO M2_TYPE_E1 pin 72 , 74
EC12 0.01UF/16V X7R
EC13 0.1UF/16V X7R
EC14 22UF/6.3V mbs_c0805 X5R
Screw Hole & NUT Hole
Height = 6.6mm
BOM P/N: 13G020369000
M2_E_HOLD_30
CT2170B176D176
13G020369000
M2_E_HOLD_30_1
SCREW M2*3L (5.5,0.8) (K) B-ZN SCREW
13050-72803030
WLAN LED
CRB NO STUFF
+3VSUS_WLAN
ER9 300OHM
ER10 300OHM
WLAN_LED2 GREEN
WLAN_LED1 GREEN
WLAN_LED2
WLAN_LED1
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS
ELX1 90Ohm/100MHz /X
mbs_r0603
ER18 0Ohm
ER20 0Ohm
DO NOT CHANGE TO 0402
18 U_USB14+
18 U_USB14-
S_USB_PP14
S_USB_PN14
M2_TYPE_E1
GND_1
SIDE1 SIDE2
NP_NC1 NP_NC2
GND_1
USB_D+
USB_D-
GND_7
SDIO_CLK
SDIO_CMD
SDIO_DAT0
SDIO_DAT1
SDIO_DAT2
SDIO_DAT3
SDIO_Wake#
SDIO_Reset#
CNV_WR_D1N_PCH
CNV_WR_D1P_PCH
CNV_WR_D0N_PCH
CNV_WR_D0P_PCH
CNV_WR_CLKN_PCH
CNV_WR_CLKP_PCH
3.3V_2
3.3V_4
LED1#
PCM_CLK/I2S_SCK
PCM_SYNC/I2S_WS
PCM_IN/I2S_SD_IN
PCM_OUT/I2S_SD_OUT
LED2#
GND_18
UART_Wake#
UART_RX
WLAN_LED1
M2_BT_PCMCLK
M2_BT_PCMFRM_CRF_RST_N
M2_BT_PCMIN
M2_BT_PCMOUT_CLKREQ0
WLAN_LED2
M2_BT_PCMCLK 20
M2_BT_PCMFRM_CRF_RST_N 20
M2_BT_PCMIN 20
M2_BT_PCMOUT_CLKREQ0 20
BT_UART_WAKE#
CNV_BRI_RSP
ER1 Close to M.2-E
ER3 Close to M.2-E
0Ohm
22OHM
M2_BT_UART_WAKE#
CNV_BRI_RSP_PCH
M2_BT_UART_WAKE# 16
CNV_BRI_RSP_PCH 24
PCHGPP_B5 -->MAX_Q370A use
PCH_GPP_C2 -->UX550GD
PCH_GPP_J5
EC4 0.1UF/16V /X
M.2_BT_PCMCLK
M.2_BT_PCMFRM_CRF_RST_N
M.2_BT_PCMOUT_CLKREQ0
O_PCIEX1_RST#
ER5 75KOhm 1%
ER28 60.4KOhm 1%
ER30 100KOhm 1%
20190408_Intel Suggest
PCH_+1.8VSUS
+1.8VSB_LDO_R
CNV_BRI_RSP_PCH
CNV_RGI_RSP_PCH
ER26 20KOhm 1%
ER27 20KOhm 1%
CNV_RGI_DT_PCH 24 PCH_GPP_J6
CNV_RGI_RSP_PCH 24 PCH_GPP_J7
CNV_BRI_DT_PCH 24 PCH_GPP_J4
M.2_CLINK_RST_WLAN_N NET TO BE ROUTED AS HIGH IMPEDANCE
M.2_CLINK_DATA_WLAN ANF M.2_CLINK_CLK_WLAN NETS TO BE ROUTED AS LOW IMPEDANCE ~ 50 OHMS
PCIE7
18 M2_E2_TXP0
18 M2_E2_TXN0
18 M2_E2_RXP0
18 M2_E2_RXN0
16 C_PCIE_M2_E2_1
16 C_PCIE_M2_E2_1#
EC10 0.1UF/16V
EC11 0.1UF/16V
X_M2_WLAN_TXP0_C
X_M2_WLAN_TXN0_C
GND_33
PETP0
PETn0
GND_39
PERp0
PERn0
GND_45
REFCLKP0
REFCLKN0
GND_51
CLKREQ0#
PEWake0#
GND_57
Reserved_2nd_PETp1
Reserved_2nd_PETn1
GND_63
Reserved_2nd_PERp1
Reserved_2nd_PERn1
GND_69
RESERVED/REFCLKN1
RESERVED/REFCLKP1
GND_75
CLKREQ_WLAN#_X1
PCIE_WAKE#_WLAN
CNV_WT_D1N_PCH
CNV_WT_D1P_PCH
CNV_WT_D0N_PCH
CNV_WT_D0P_PCH
CNV_WT_CLKN_PCH
CNV_WT_CLKP_PCH
UART_TX
UART_CTS
UART_RTS
RESERVED_38
RESERVED_40
RESERVED_42
COEX3
COEX2
COEX1
SSCLK
PERST0#
Reserved_W_DISABLE2#
W_DISABLE1#
I2C_DATA
I2C_CLK
ALERT
RESERVED_64
UIM_SWP/PERST1#
UIM_PWR_SNK/CLREQ1#
UIM_PWR_SRC/GPIO1/PEWAKE1#
3.3V_72
3.3V_74
CNV_RGI_DT_PCH
CNV_RGI_RSP
CNV_BRI_DT_PCH
ER6 Close to M.2-E
22OHM
CNV_RGI_RSP_PCH
CNV_BRI_DT_PCH 24
M.2_CLINK_RST_WLAN# 19
M.2_CLINK_DATA_WLAN 19
M.2_CLINK_CLK_WLAN 19
Require No Stub
M2_E_SUSCLK
M2_WLAN_RESET#
BT_ON/OFF_Q
RF_DEV_ON
ER7 33Ohm
ER8 0Ohm
CRB PCH SUSCLK to ICS553 to M.2 E
PCH_SUSCLK 20,49
O_PCIEX1_RST# 29,30,49,52
CLKIN_XTAL_PCH
CLKIN_XTAL_PCH 16
CNVi XTAL CLOK
+3VSUS_WLAN
NGFF KEY-E 75P 0.5 8.5H STD
[HE]LOTES/APCI0163-P001A
BLACK
MINI_PCI_75P
12003-00160300
M2_TYPE_E1 NGFF KEY-E 75P 0.5 8.5H STD
ME-Cost down suggest: P/N : 12003-00160300 LOTES/APCI0163-P001A
20190401_Modify
WLAN CLKREQ#
WLAN PWR : +3VSUS (Mount ER28 / Unmount ER29)
Mount EQ3, ER17 / Unmount ER16, EQ4
WLAN PWR : +3V (Mount ER29 / Unmount ER28)
Mount ER16,EQ4 / Unmount EQ3, ER17
+12V
PCH GPP_H2 +3V
UM6K1N EQ3A /X
+3VSUS
16 CLK_REQ9_M2_WLAN#
CLKREQ_WLAN#_X1
20190403_Intel Suggest the Pin OD
ER16 0Ohm
20190401_Modify
BT ON for CNVi Setting
+3VSUS_WLAN
ER12 100KOhm 1%
BT_ON/OFF_Q
ED1 BAT54AW
ER15 10KOhm /X
BT_RF_KILL# 17 PCH_GPP_B3
WLAN ON for CNVi Setting
+3VSUS_WLAN
ER13 10KOhm 1%
RF_DEV_ON
EQ2 H2N7002 /X
WIFI_RF_KILL# 24 PCH_GPP_B17
WLAN_Wake# Control
WLAN PWR : +3VSUS (Mount ER28 / Unmount ER29)
Mount EQ3, ER17 / Unmount ER16, EQ4
WLAN PWR : +3V (Mount ER29 / Unmount ER28)
Mount ER16,EQ4 / Unmount EQ3, ER17
+12V
/X UM6K1N EQ3B
+3VSUS
+3VSUS
20,30,41,49,55 X_WAKE#
PCIE_WAKE#_WLAN
ER17 0Ohm
ASUSTek COMPUTER INC.
Title : M.2_Key-E_WLAN_CNVi
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
Sheet 50 of 75

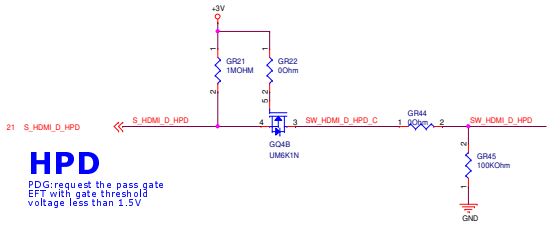


Cost Reduced Level Shifter



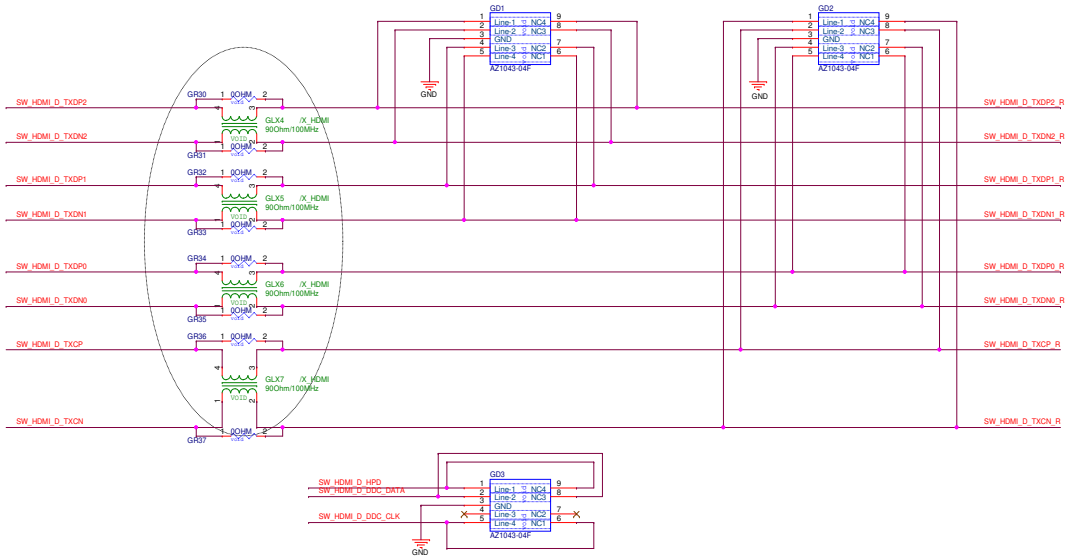




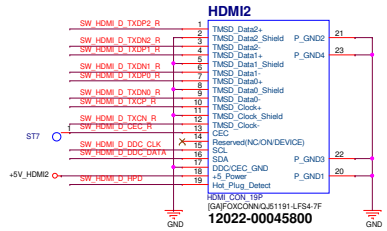


HPD

PDG:request the pass gate
EFT with gate threshold
voltage less than 1.5V

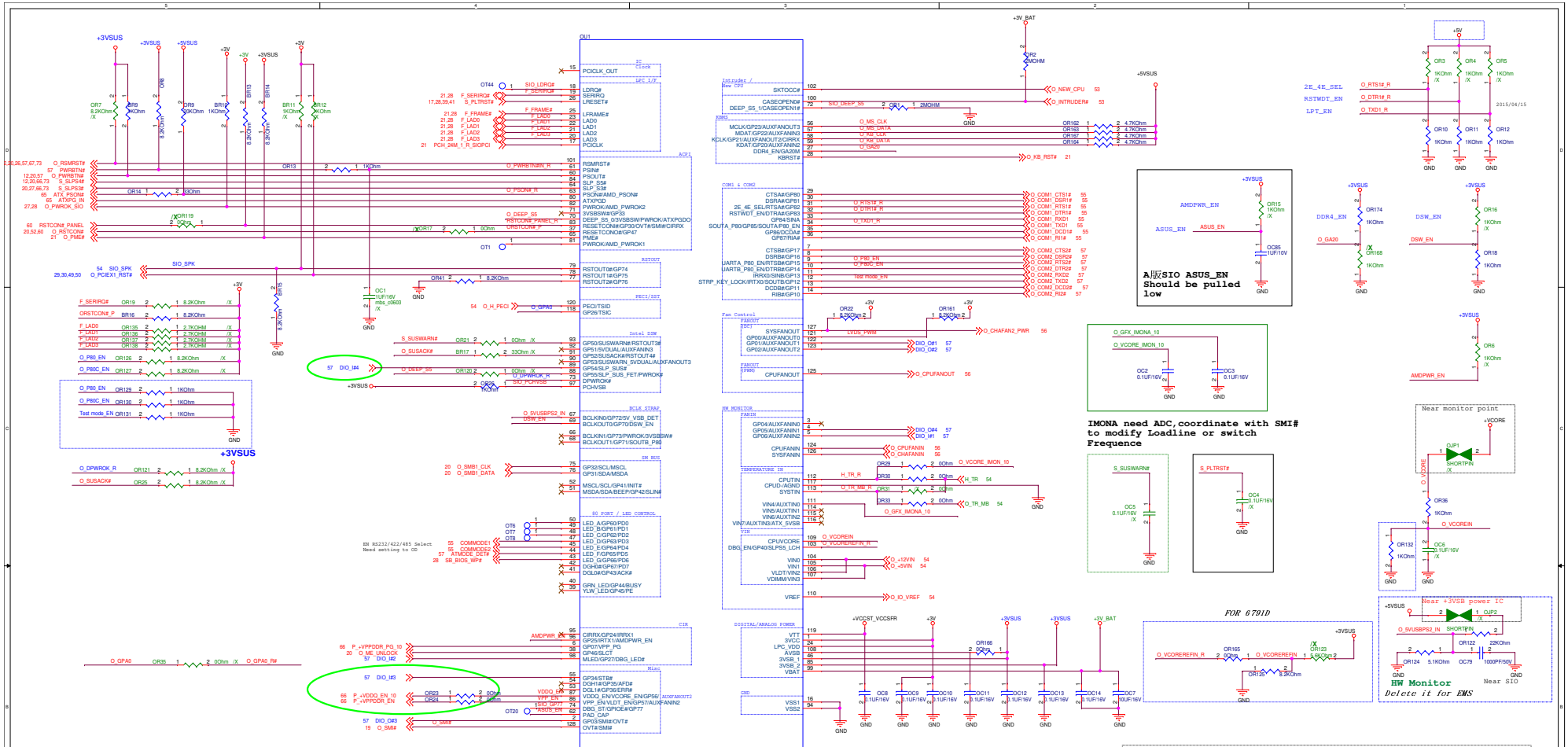


HDMI-2 (Port D)



ESD connector

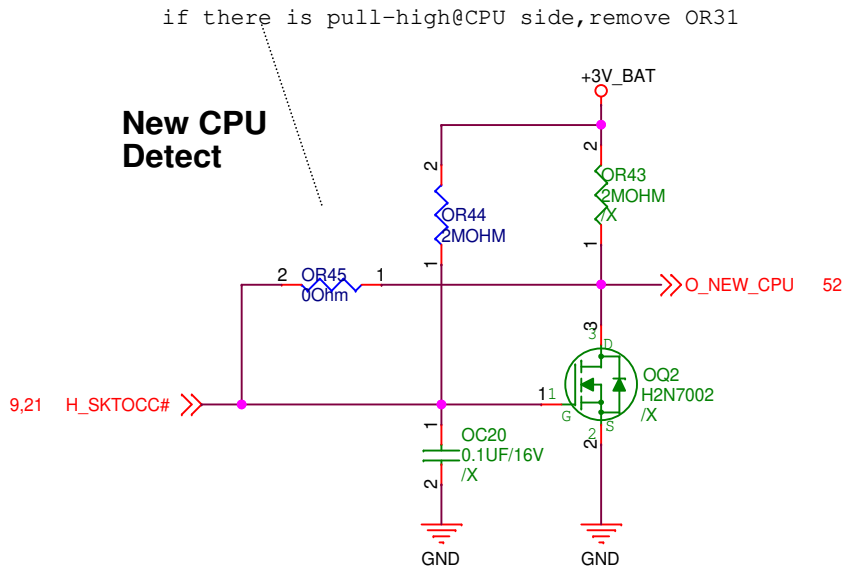
ASUSTeK COMPUTER INC.	Title : HDMI-2 (Port D)	Engineer: IPC-EE3
Size A2	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 51 of 75	

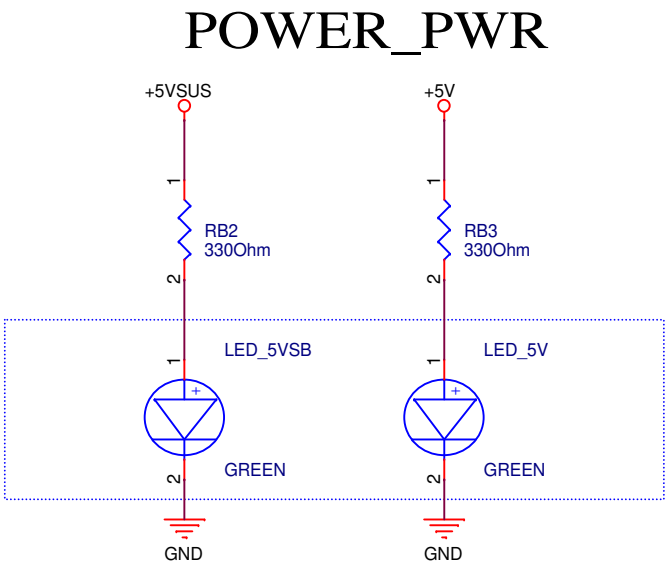


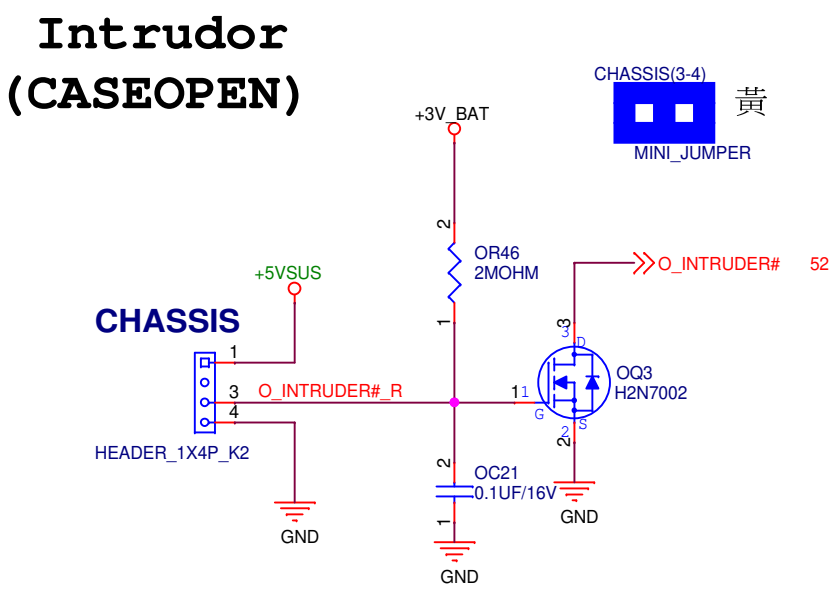
POWER ON STRAPPING PIN NCT6791D

PIN	Name	0	1	Power	Description
31	2E_4E_SEL	2E	4E	VCC	I/O Configuration Address
32	24_48_SEL	24M clock source	48M clock source	VCC	Clock Source Selection
34	LPT_EN	Disable LPT	Enable LPT	VCC	LPT OR OTHERS
62	ASUS_EN	Disable ASUS ASIC	Enable ASUS ASIC	VSB	ASUS GLUE LOGIC
69	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	VSB	DSW OR SVID FUNCTION
71	ANTISURGE_EN	DISABLE ANTISURGE FUNCTION	ENABLE ANTISURGE FUNCTION	VSB	ANTISURGE FUNCTION
96	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	VSB	AMD SEQ OR PVID FUNCTION

ASUSTeK COMPUTER INC.	Title : NCT6793D	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2		Rev: R1.01
Date: Monday, February 17, 2020	Sheet 52 of 75		

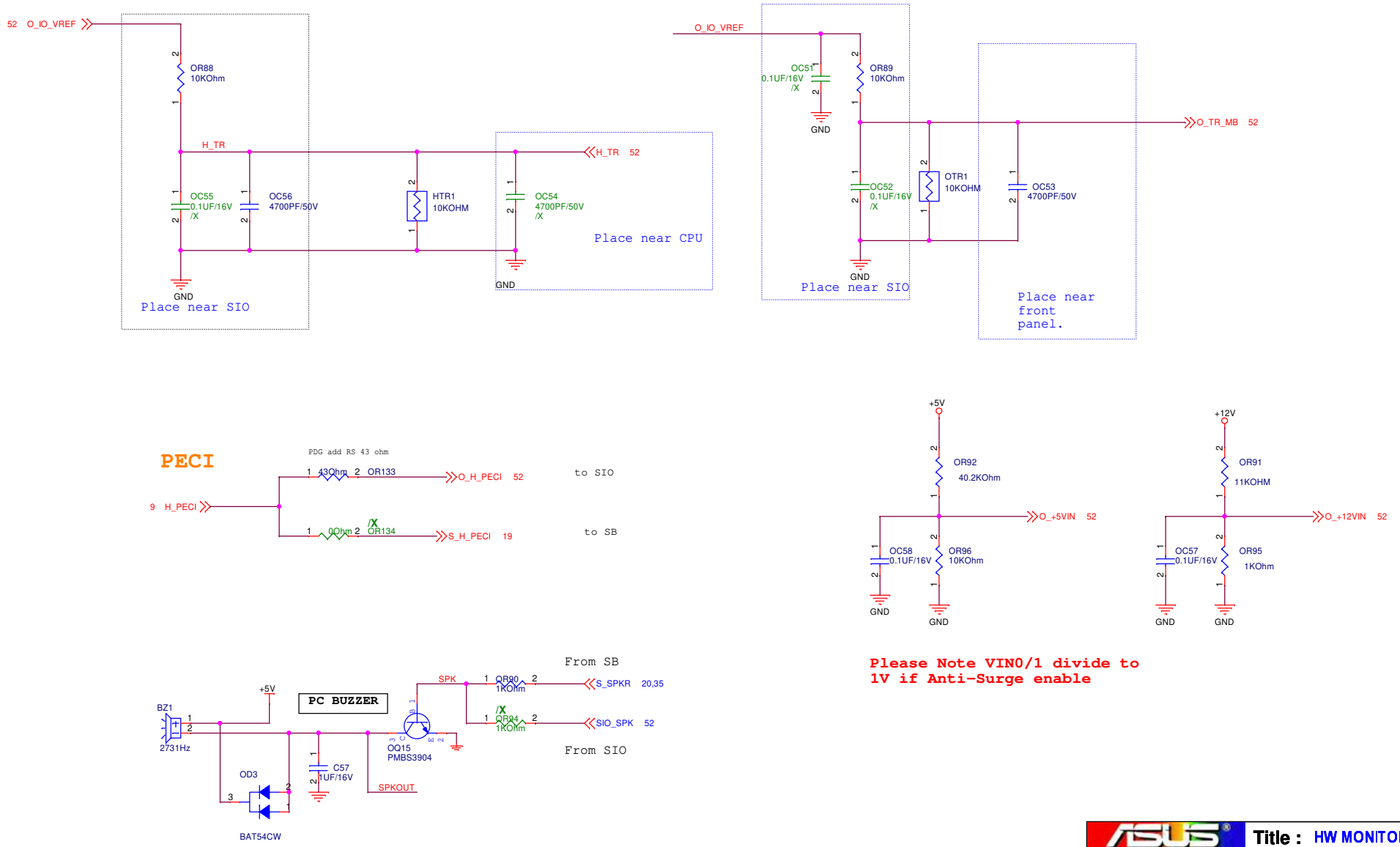






To SIO

ASUSTek COMPUTER INC.	Title : Intrudor(CASEOPEN)		
	Engineer: IPC-EE3		
Size A	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 53 of 75		



ASUS	Title : HW MONITOR	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 54 of 75	

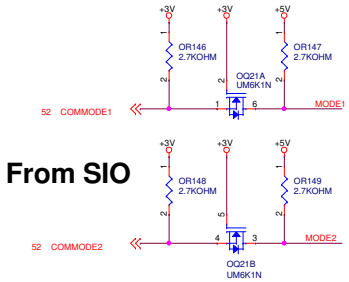
RS422/RS485 Terminator

COM_J1 all off -->RS232
COM_J1 all on -->RS485/RS422 with terminator

Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ.
As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.

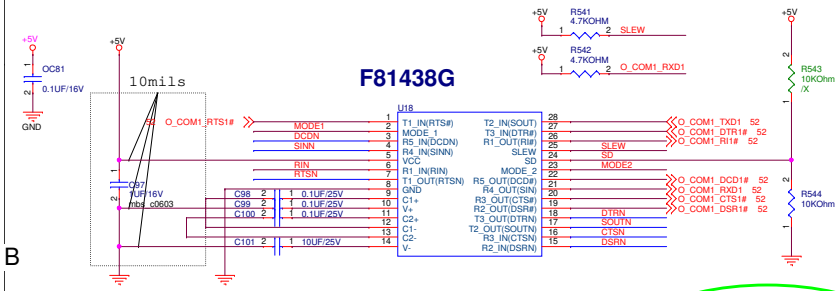


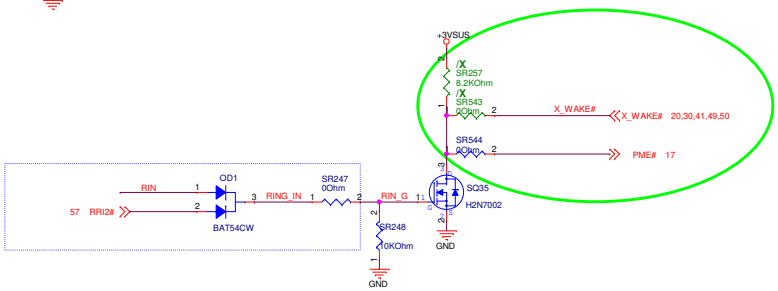
(VDD = +5.0V ± 5%)

Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01.		2	30	mA
Supply Current (RS-485)	No Load, MODE = 10, 11.		2		mA
Supply Current (RS-422)	MODE = 00.		2		mA
Operating Temperature *	Symbol: T	-40		85	◦ C

(VDD = +5.0V ± 5%)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V_{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	μA	
Driver Input Pull High Current	I_{IT}			±15	μA	

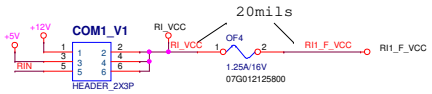


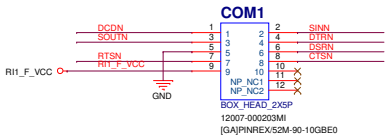


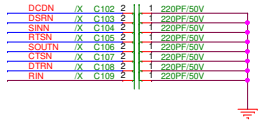
COM1_V1(5-6)	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

COM1_V1(5-6)

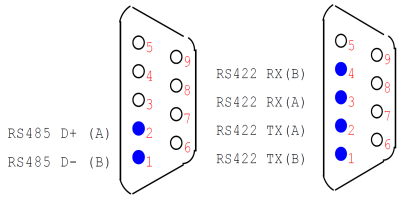
MINI_JUMPER



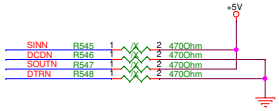




Close to COM port connector



Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps



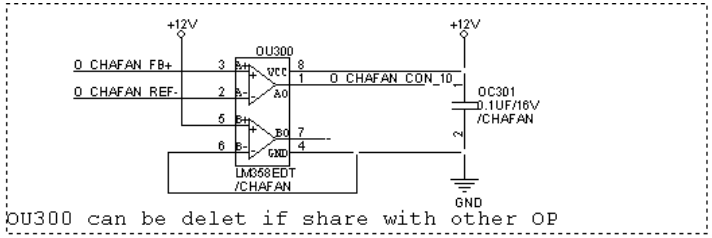
Note:Reserved for FAIL-SAVE

ASUSTek COMPUTER INC.	Title : COM1_RS232/422/485
	Engineer: IPC-EE3
Size: Custom	Project Name: MIX-Q370D2
	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 55 of 75

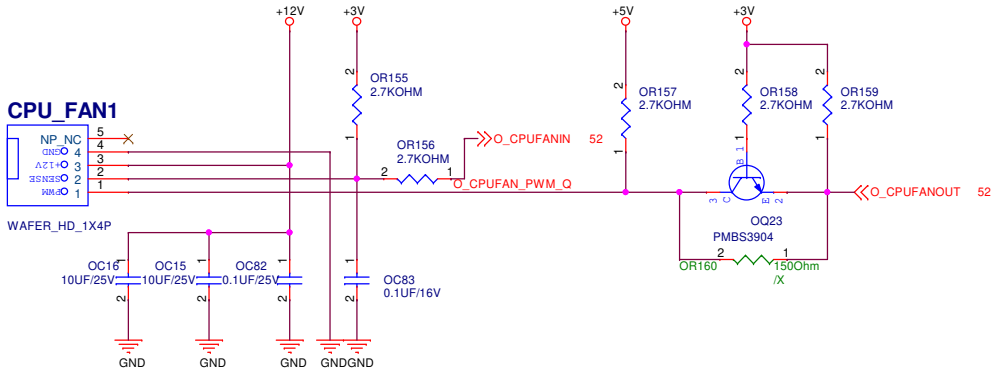
FAN CONTROL

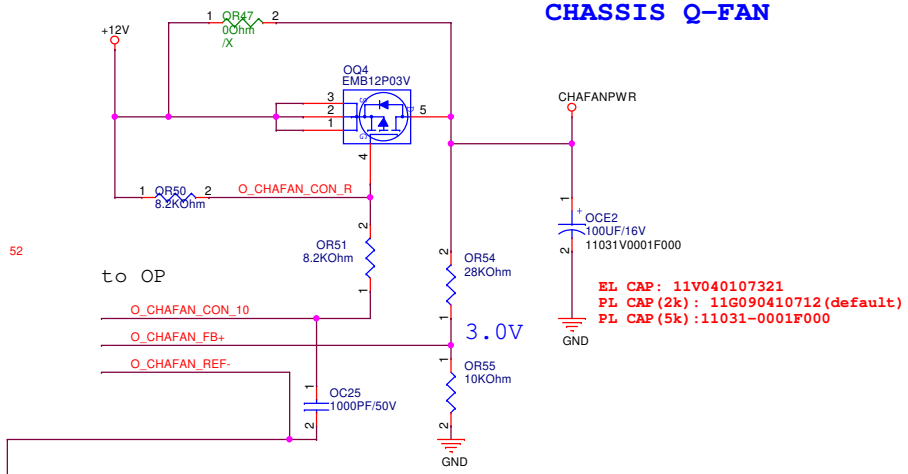
PWM FAN CONTROL(New)

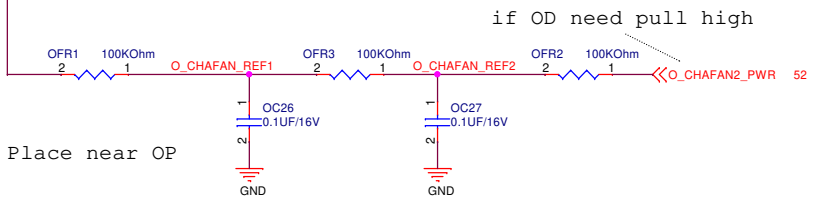
Pin Number	Signal
1	Control
2	Sense
3	+12V
4	GND

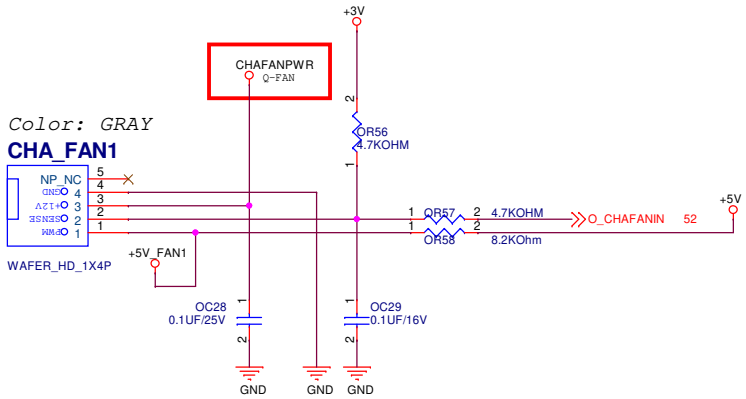


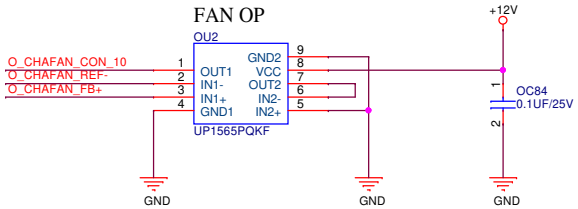
CHASSIS Q-FAN











ASUS

ASUSTek COMPUTER INC.

Title : CPUFAN_SYSFAN1

Engineer: IPC-EE3

Size	Project Name	Rev
B	MIX-Q370D2	R1.01

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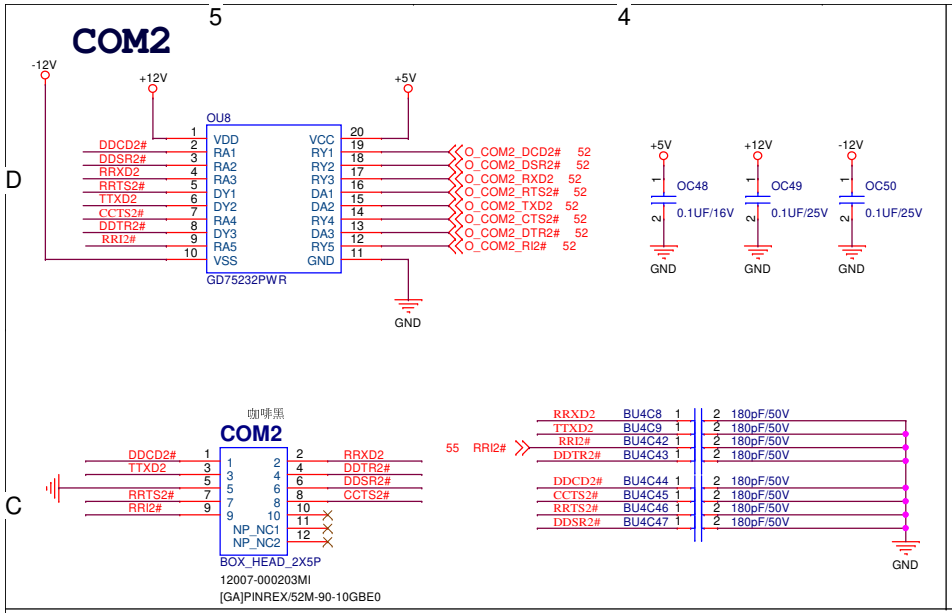
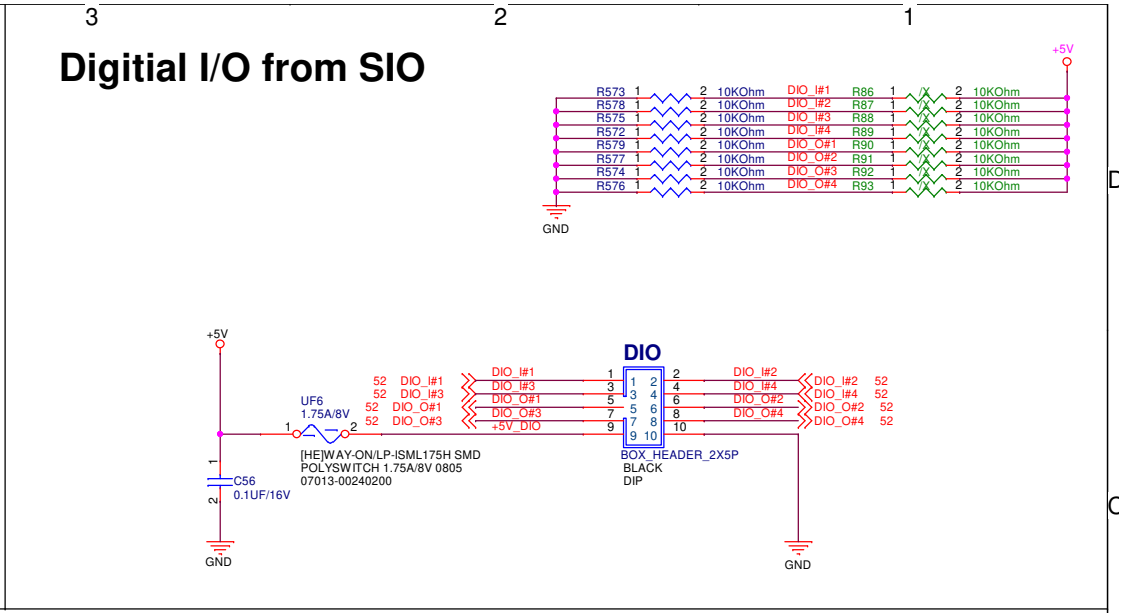
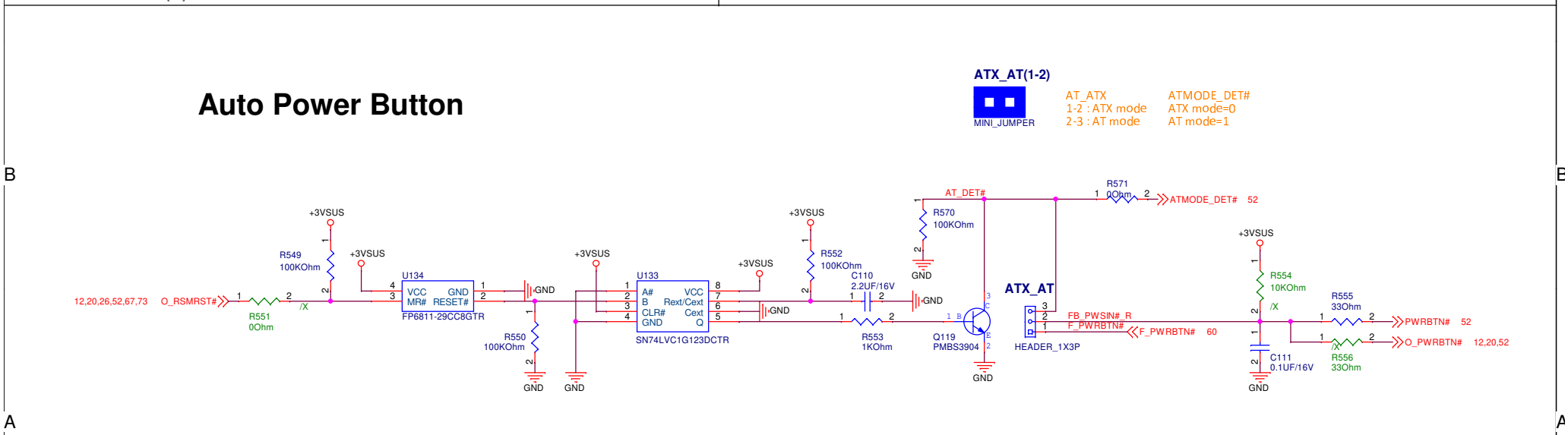


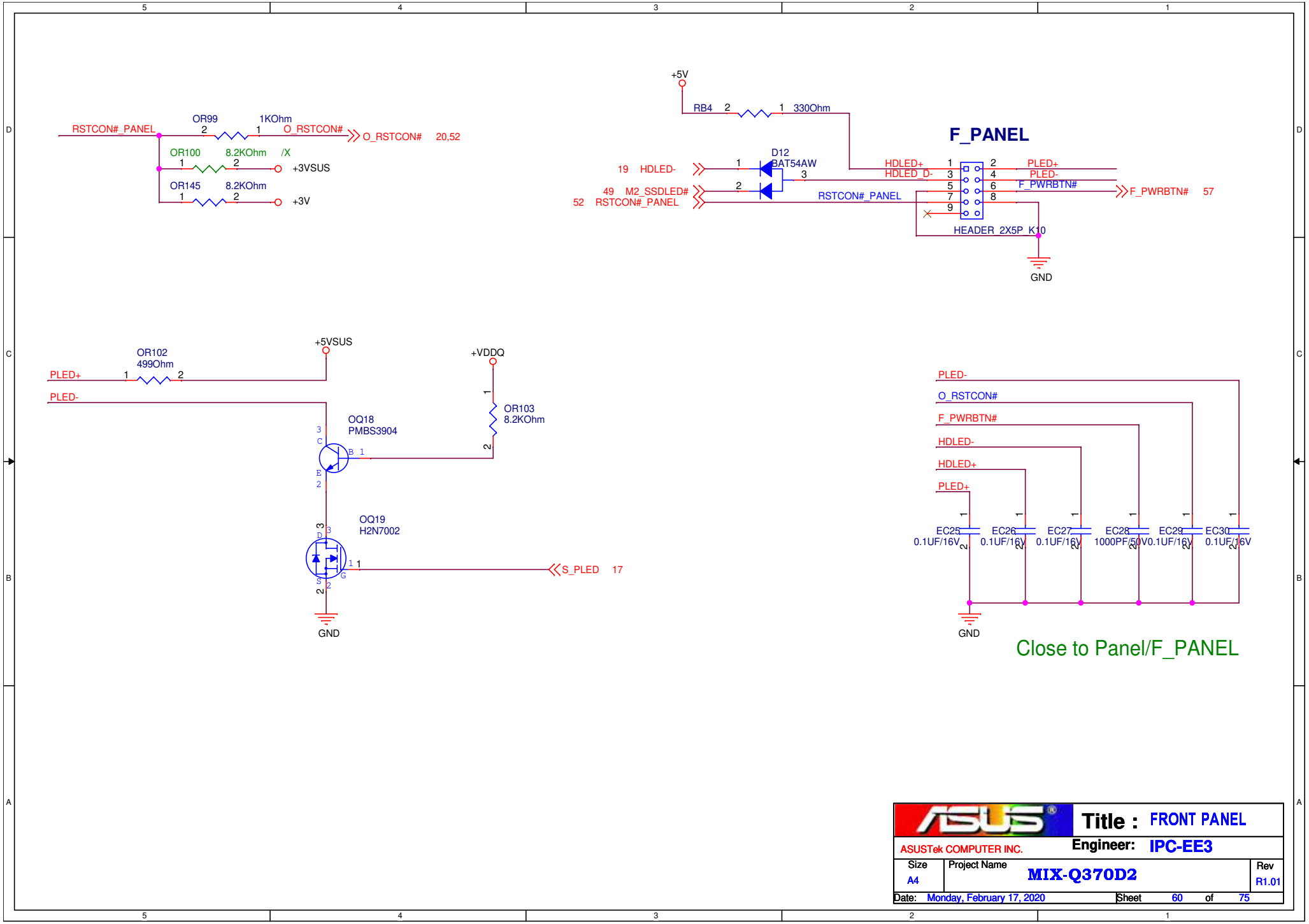




ASUS	Title : COM2/DIO/ATX		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size B	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 57 of 75		

ASUSTek COMPUTER INC.	Title : F81216HD-I			
	Engineer: IPC-EE3			
Size B	Project Name MIX-Q370D2			Rev R1.01
Date: Monday, February 17, 2020		Sheet 58 of 75		

Title : XXXXX		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 59 of 75	


RSTCON#_PANEL
OR99
1KOhm
O_RSTCON#
O_RSTCON# 20,52
OR100
8.2KOhm
/X
+3VSUS
OR145
8.2KOhm
+3V
+5V
RB4
330Ohm
F_PANEL
19 HDLED-
D12
BAT54AW
49 M2_SSDLED#
52 RSTCON#_PANEL
HDLED+
HDLED_D-
RSTCON#_PANEL
PLED+
PLED-
F_PWRBTN#
F_PWRBTN# 57
HEADER_2X5P_K10
GND
+5VSUS
OR102
499Ohm
PLED+
PLED-
+VDDQ
OR103
8.2KOhm
OQ18
PMBS3904
OQ19
H2N7002
S_PLED 17
GND
PLED-
O_RSTCON#
F_PWRBTN#
HDLED-
HDLED+
PLED+
EC25
0.1UF/16V
EC26
0.1UF/16V
EC27
0.1UF/16V
EC28
1000PF/50V
EC29
0.1UF/16V
EC30
0.1UF/16V
GND
Close to Panel/F_PANEL
Title : FRONT PANEL
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size A4
Project Name MIX-Q370D2
Rev R1.01
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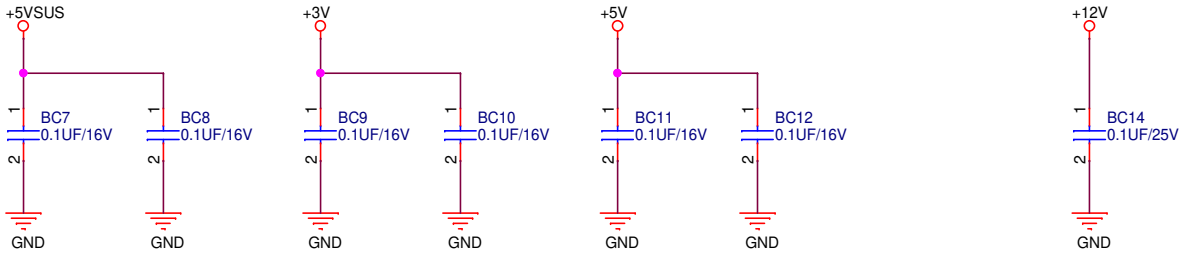
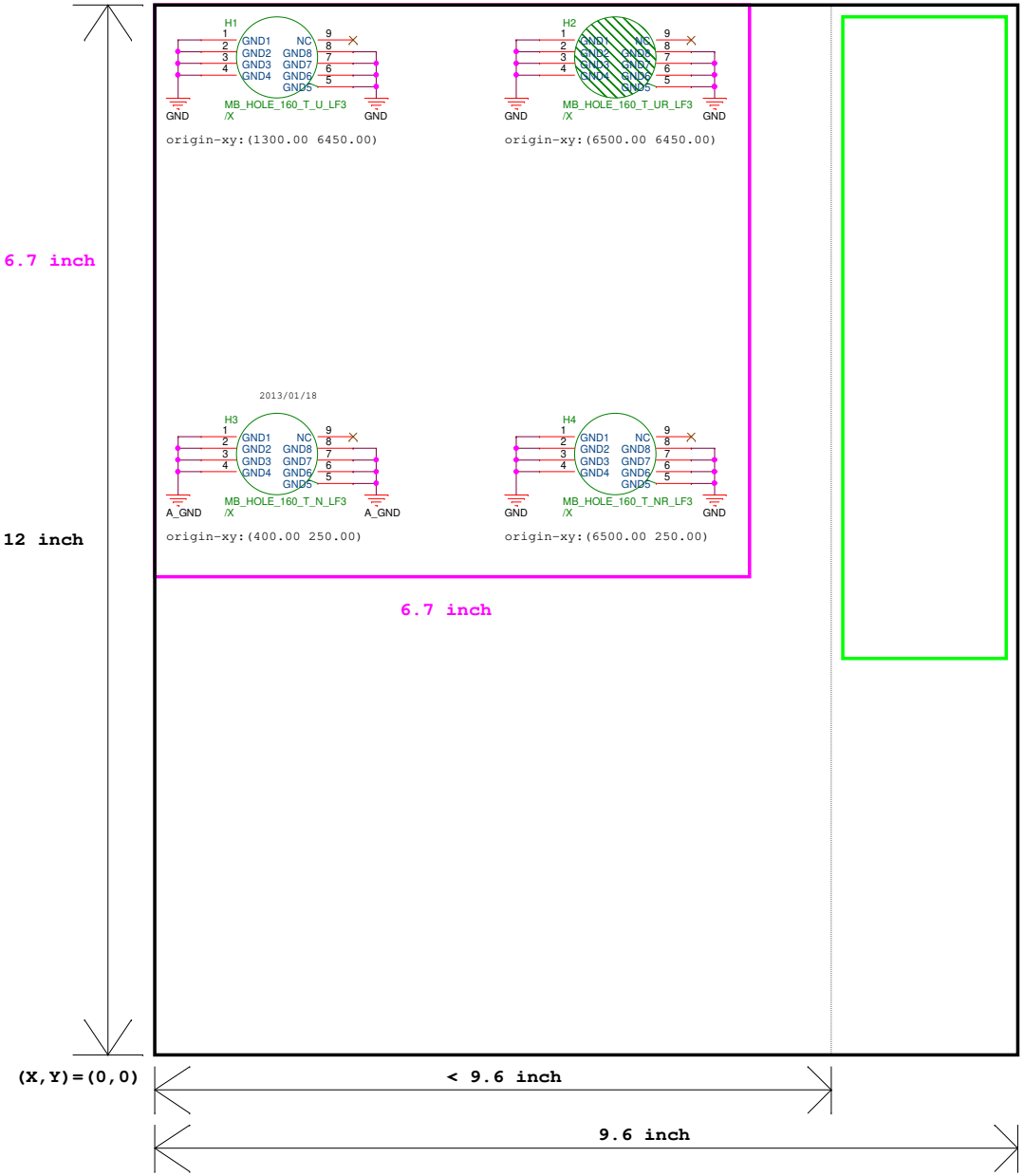
Bypass/EMI Capacitor



ASUS	Title : EMI Cap	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A4	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 61 of 75	

Delete it for EMS

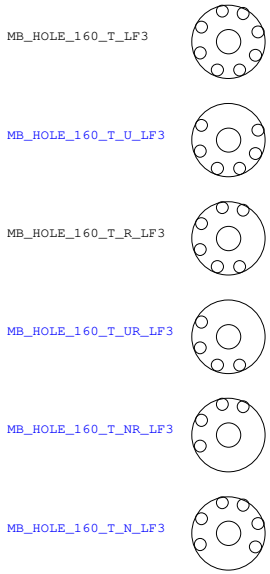
mini-ITX Screw Hole



m-ATX Screw Select

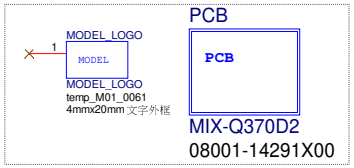
	Standard (9.6 x 9.6)	Scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H20	V	V

MB SCREW FOOTPRINT



ASUS	Title : Screw Hole	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 62 of 75	

Selling Point



MIX-Q370D2 R1.01 PCB-08 :

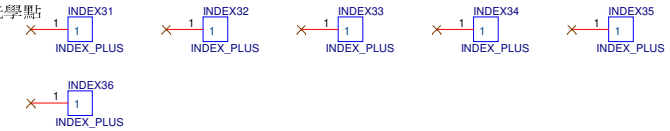
R1.01 PCB_DF : 08001-14291100

Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

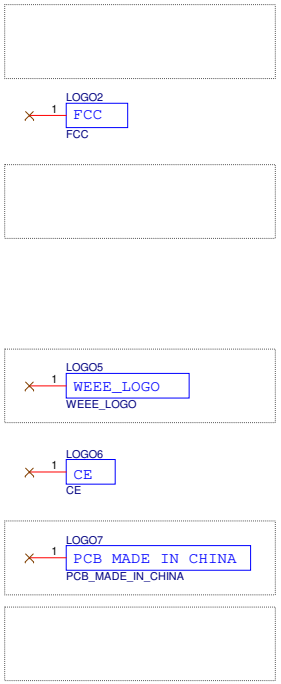
小顆十字光學點



2012/09/11

Logo

common Logo for all projects



ASUS	Title : Selling Point_Logo		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size A3	Project Name MIX-Q370D2		Rev R1.01
Date: Monday, February 17, 2020	Sheet 63 of 75		

ASUSTek COMPUTER INC.	Title : COM3-6	
	Engineer: IPC-EE3	
Size: B	Project Name: MIX-Q370D2	Rev: R1.01
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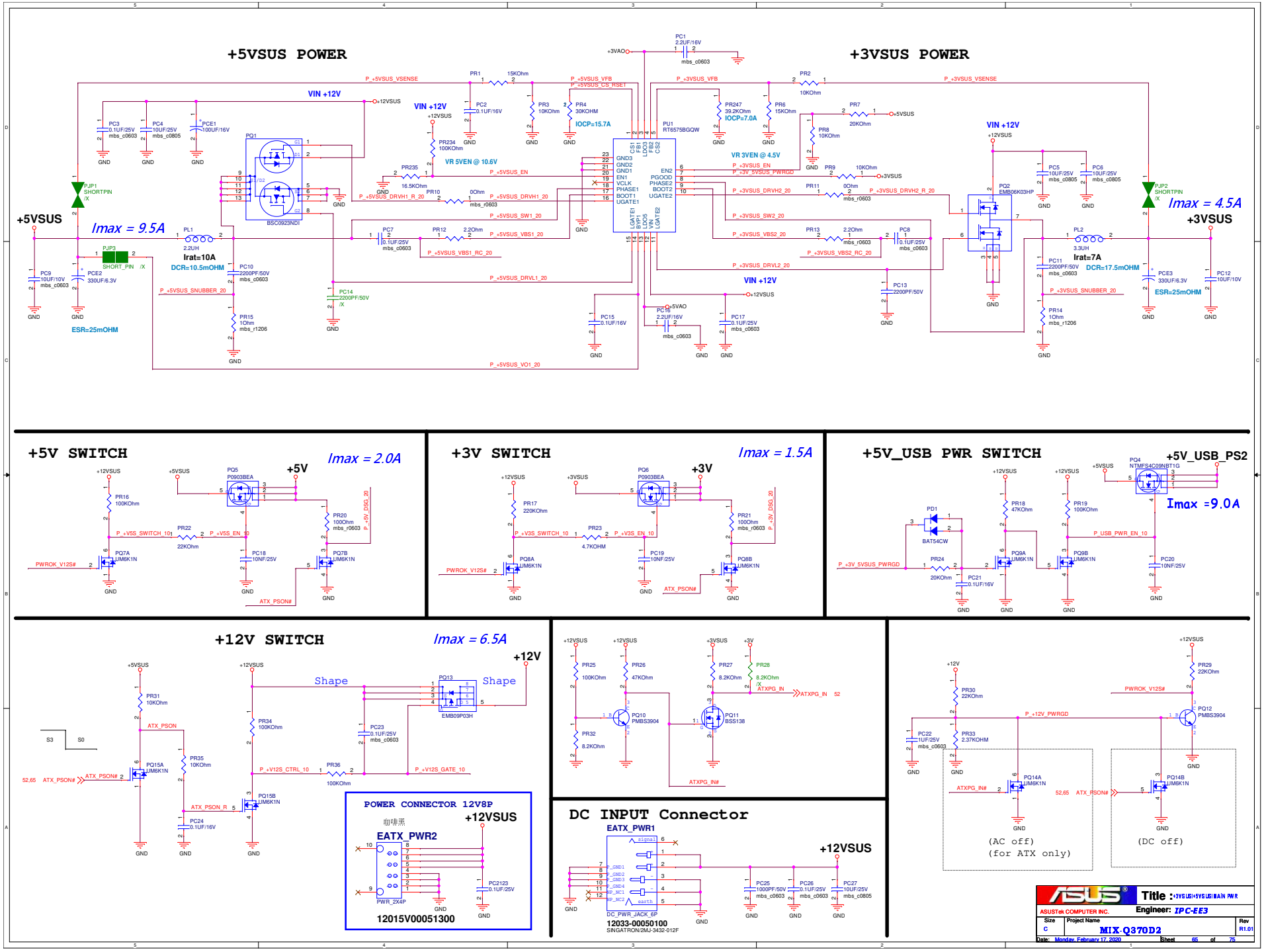
+5VSUS POWER
+3VSUS POWER
+5VSUS
Imax = 9.5A
Irat=10A
DCR=10.5mOHM
ESR=25mOHM
+3VSUS
Imax = 4.5A
Irat=7A
DCR=17.5mOHM
ESR=25mOHM
VIN +12V
VR 5VEN @ 10.6V
VR 3VEN @ 4.5V
IOCP=15.7A
IOCP=7.0A
PU1 RT6575BGQW
BSC0923NDI
PQ2 EMB06K03HP
+5V SWITCH
Imax = 2.0A
+5V
+3V SWITCH
Imax = 1.5A
+3V
+5V_USB PWR SWITCH
+5V_USB_PS2
Imax =9.0A
+12V SWITCH
Imax = 6.5A
+12V
Shape
EMB09P03H
POWER CONNECTOR 12V8P
+12VSUS
EATX_PWR2
12015V00051300
DC INPUT Connector
EATX_PWR1
+12VSUS
DC_PWR_JACK_6P
12033-00050100
SINGATRON/2MJ-3432-012F
(AC off)
(for ATX only)
(DC off)
Title : +3VSUS+5VSUS+MAIN PWR
ASUSTeK COMPUTER INC.
Engineer: IPC-EE3
Size C
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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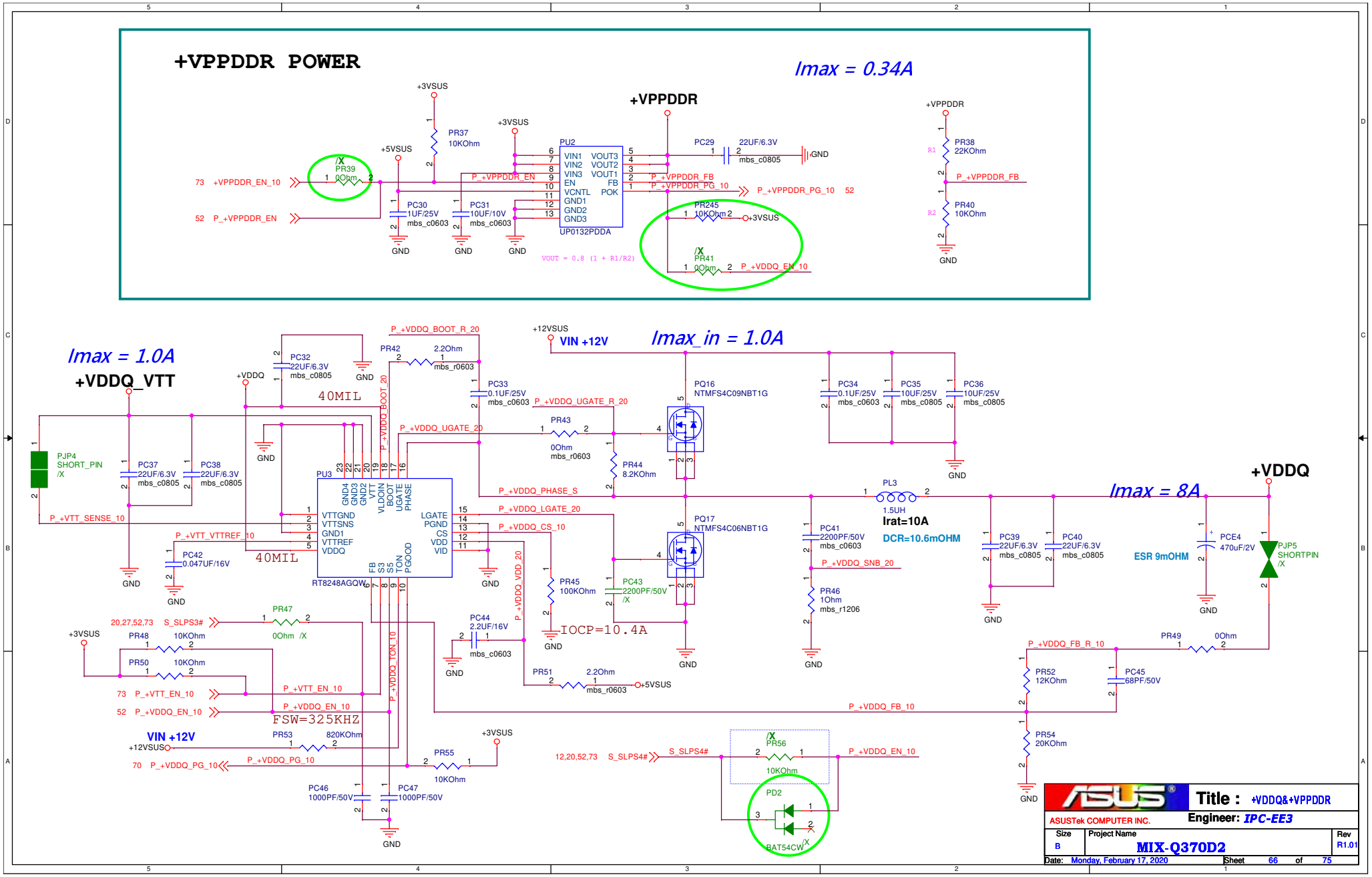
+VPPDDR POWER
Imax = 0.34A
+VPPDDR
+3VSUS
+5VSUS
PR37 10KOhm
/X PR39 0Ohm
73 +VPPDDR_EN_10
52 P_+VPPDDR_EN
PU2
VIN1 VOUT3
VIN2 VOUT2
VIN3 VOUT1
EN FB
VCNTL POK
GND1
GND2
GND3
UP0132PDDA
PC30 1UF/25V mbs_c0603
PC31 10UF/10V mbs_c0603
PC29 22UF/6.3V mbs_c0805
P_+VPPDDR_FB
P_+VPPDDR_PG_10
52
PR245 10KOhm
/X PR41 0Ohm
P_+VDDQ_EN_10
VOUT = 0.8 (1 + R1/R2)
PR38 22KOhm
PR40 10KOhm
Imax = 1.0A
+VDDQ_VTT
PC32 22UF/6.3V mbs_c0805
40MIL
PJP4 SHORT_PIN /X
PC37 22UF/6.3V mbs_c0805
PC38 22UF/6.3V mbs_c0805
P_+VTT_SENSE_10
P_+VTT_VTTREF_10
PC42 0.047UF/16V
PU3
RT8248AGQW
VTTGND
VTTSNS
GND1
VTTREF
VDDQ
LGATE
PGND
CS
VDD
VID
P_+VDDQ_BOOT_R_20
PR42 2.2Ohm mbs_r0603
PC33 0.1UF/25V mbs_c0603
P_+VDDQ_UGATE_R_20
P_+VDDQ_UGATE_20
PR43 0Ohm mbs_r0603
PR44 8.2KOhm
P_+VDDQ_PHASE_S
P_+VDDQ_LGATE_20
P_+VDDQ_CS_10
PR45 100KOhm
PC43 2200PF/50V /X
IOCP=10.4A
PC44 2.2UF/16V mbs_c0603
PR51 2.2Ohm mbs_r0603
+5VSUS
PR47 0Ohm /X
20,27,52,73 S_SLPS3#
PR48 10KOhm
PR50 10KOhm
73 P_+VTT_EN_10
52 P_+VDDQ_EN_10
P_+VTT_EN_10
P_+VDDQ_EN_10
FSW=325KHZ
VIN +12V
+12VSUS
PR53 820KOhm
70 P_+VDDQ_PG_10
P_+VDDQ_PG_10
PR55 10KOhm
PC46 1000PF/50V
PC47 1000PF/50V
Imax_in = 1.0A
PQ16 NTMFS4C09NBT1G
PQ17 NTMFS4C06NBT1G
PC34 0.1UF/25V mbs_c0603
PC35 10UF/25V mbs_c0805
PC36 10UF/25V mbs_c0805
PL3 1.5UH
Irat=10A
DCR=10.6mOHM
PC41 2200PF/50V mbs_c0603
P_+VDDQ_SNB_20
PR46 1Ohm mbs_r1206
PC39 22UF/6.3V mbs_c0805
PC40 22UF/6.3V mbs_c0805
Imax = 8A
+VDDQ
ESR 9mOHM
PCE4 470uF/2V
PJP5 SHORTPIN /X
PR49 0Ohm
P_+VDDQ_FB_R_10
PR52 12KOhm
PC45 68PF/50V
P_+VDDQ_FB_10
PR54 20KOhm
12,20,52,73 S_SLPS4#
S_SLPS4#
/X PR56 10KOhm
P_+VDDQ_EN_10
PD2 BAT54CW /X
GND
ASUSTek COMPUTER INC.
Title : +VDDQ&+VPPDDR
Engineer: IPC-EE3
Size B
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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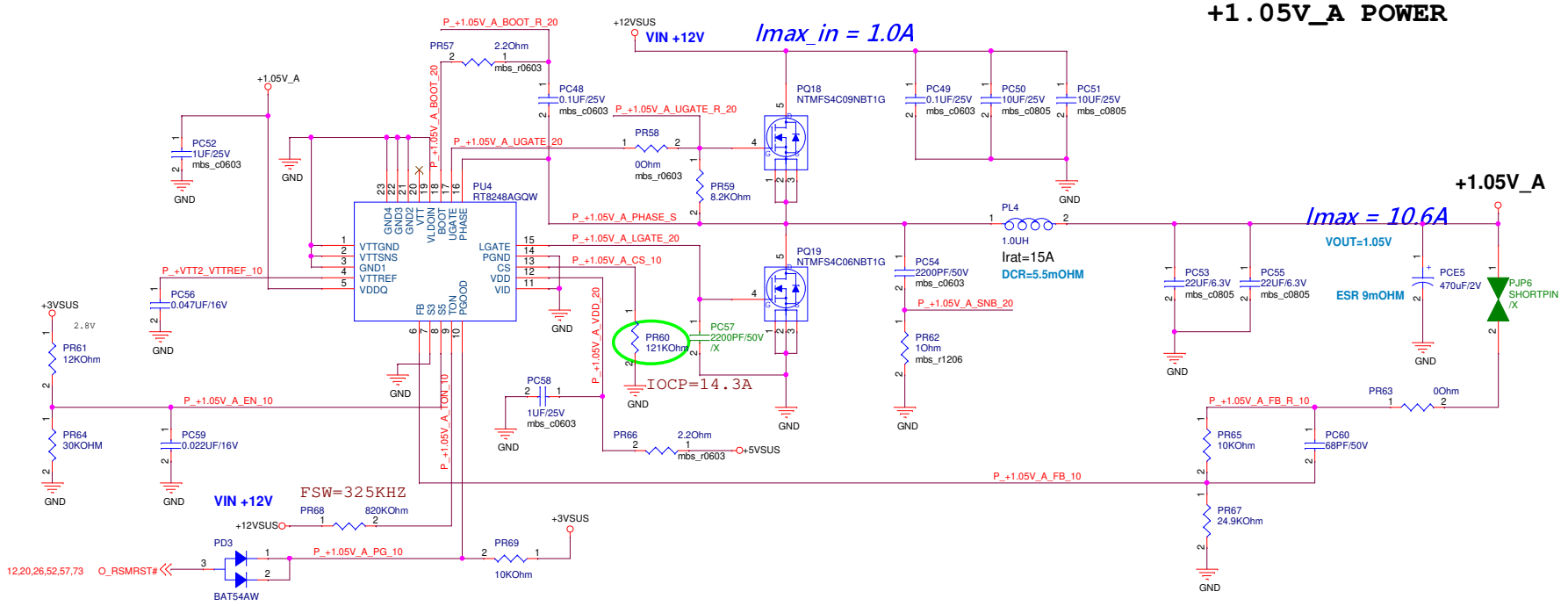
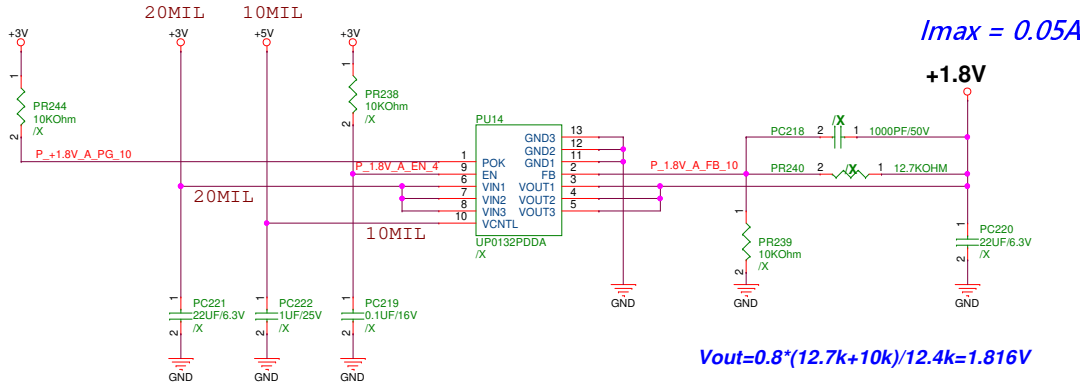
+1.05V_A POWER



+1.8V POWER

1.8V allowed to ramp first with no limit; only requirement is it must ramp after VccRTC



ASUS	Title : +1.05V_A//+1.8V	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size A3	Project Name MIX-Q370D2	Rev R1.01
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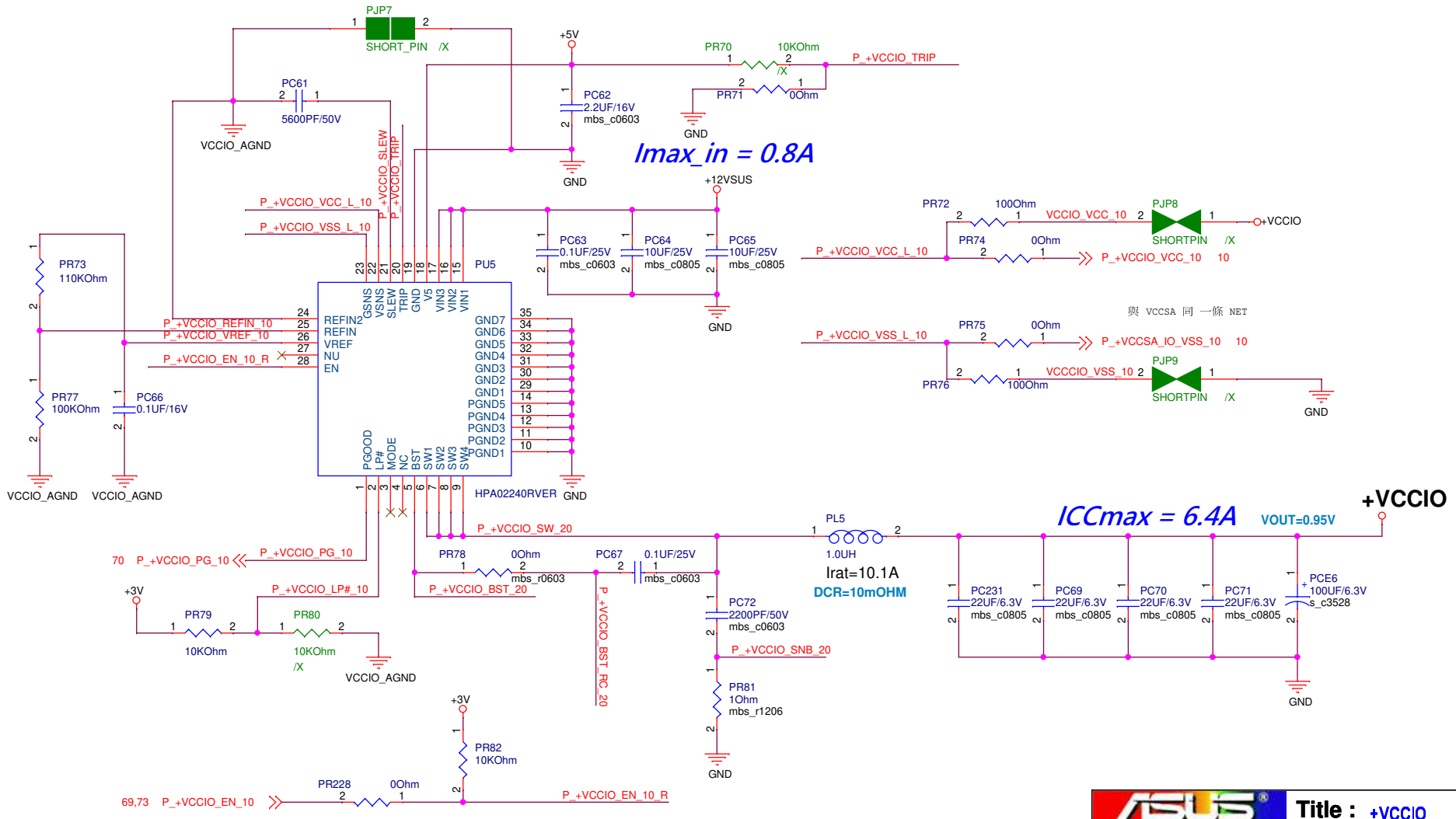
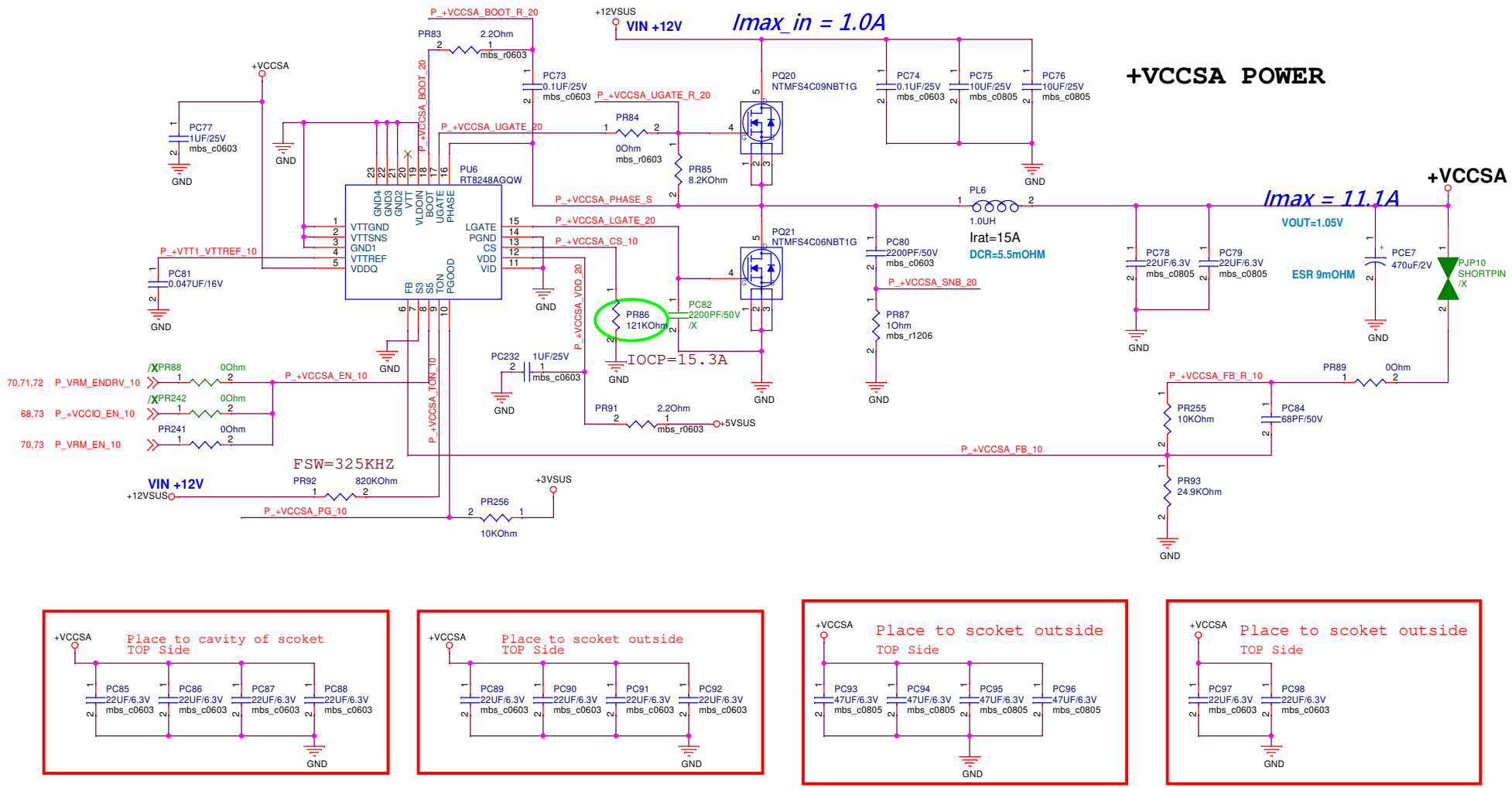
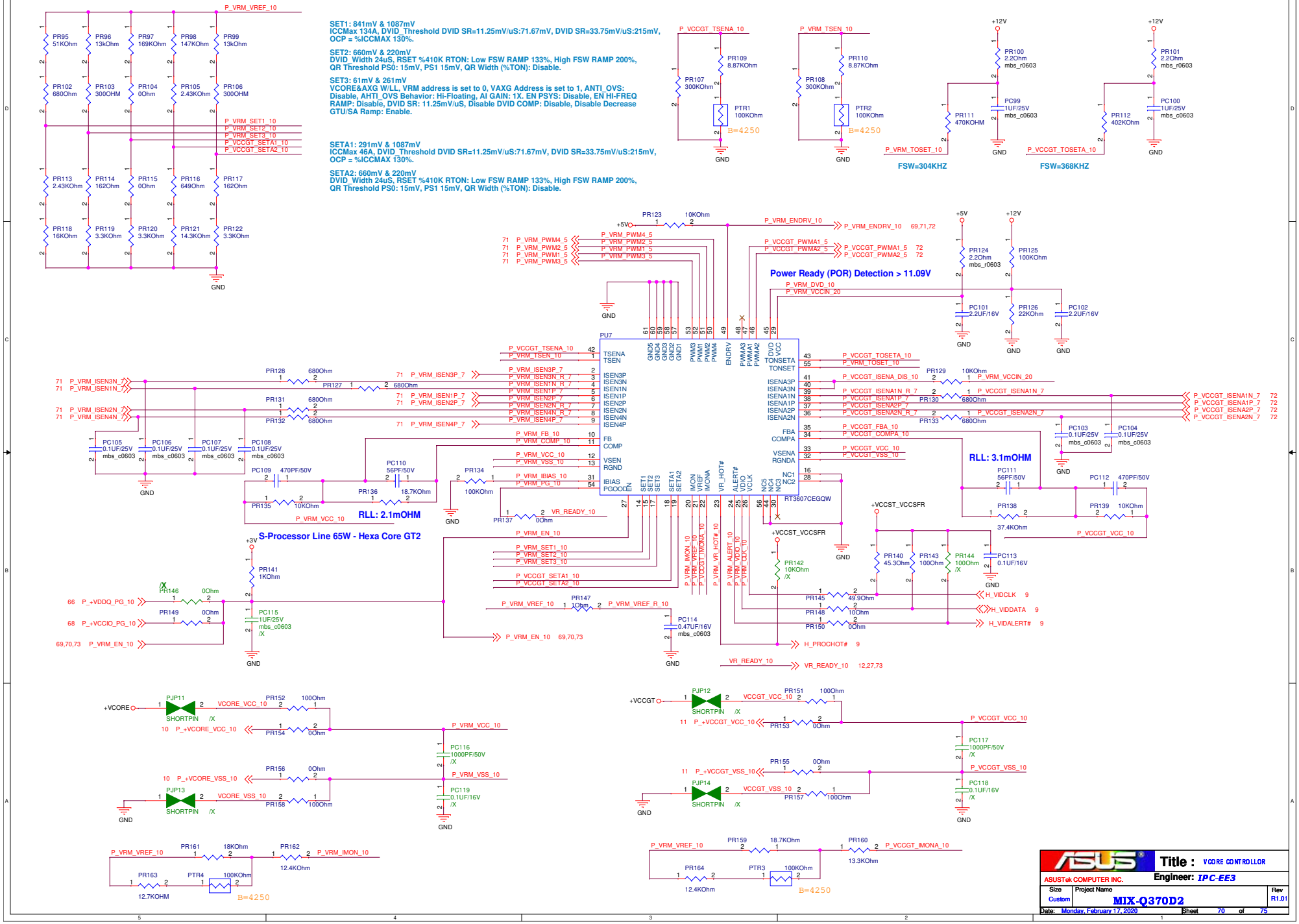
+VCCIO POWER



ASUSTek COMPUTER INC.	Title : +VCCIO	
	Engineer: IPC-EE3	
Size: Custom	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 68 of 75	



ASUS	Title : +VCCSA	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: B	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 69 of 75	


SET1: 841mV & 1087mV
ICCMax 134A, DVID_Threshold DVID SR=11.25mV/uS:71.67mV, DVID SR=33.75mV/uS:215mV, OCP = %ICCMAX 130%.
SET2: 660mV & 220mV
DVID_Width 24uS, RSET %410K RTON: Low FSW RAMP 133%, High FSW RAMP 200%, QR Threshold PS0: 15mV, PS1 15mV, QR Width (%TON): Disable.
SET3: 61mV & 261mV
VCORE&AXG W/LL, VRM address is set to 0, VAXG Address is set to 1, ANTI_OVS: Disable, AHTI_OVS Behavior: Hi-Floating, AI GAIN: 1X. EN PSYS: Disable, EN HI-FREQ RAMP: Disable, DVID SR: 11.25mV/uS, Disable DVID COMP: Disable, Disable Decrease GTU/SA Ramp: Enable.
SETA1: 291mV & 1087mV
ICCMax 46A, DVID_Threshold DVID SR=11.25mV/uS:71.67mV, DVID SR=33.75mV/uS:215mV, OCP = %ICCMAX 130%.
SETA2: 660mV & 220mV
DVID_Width 24uS, RSET %410K RTON: Low FSW RAMP 133%, High FSW RAMP 200%, QR Threshold PS0: 15mV, PS1 15mV, QR Width (%TON): Disable.
FSW=304KHZ
FSW=368KHZ
Power Ready (POR) Detection > 11.09V
RLL: 3.1mOHM
RLL: 2.1mOHM
S-Processor Line 65W - Hexa Core GT2
RT3607CEGQW
Title : VCORE CONTROLLOR
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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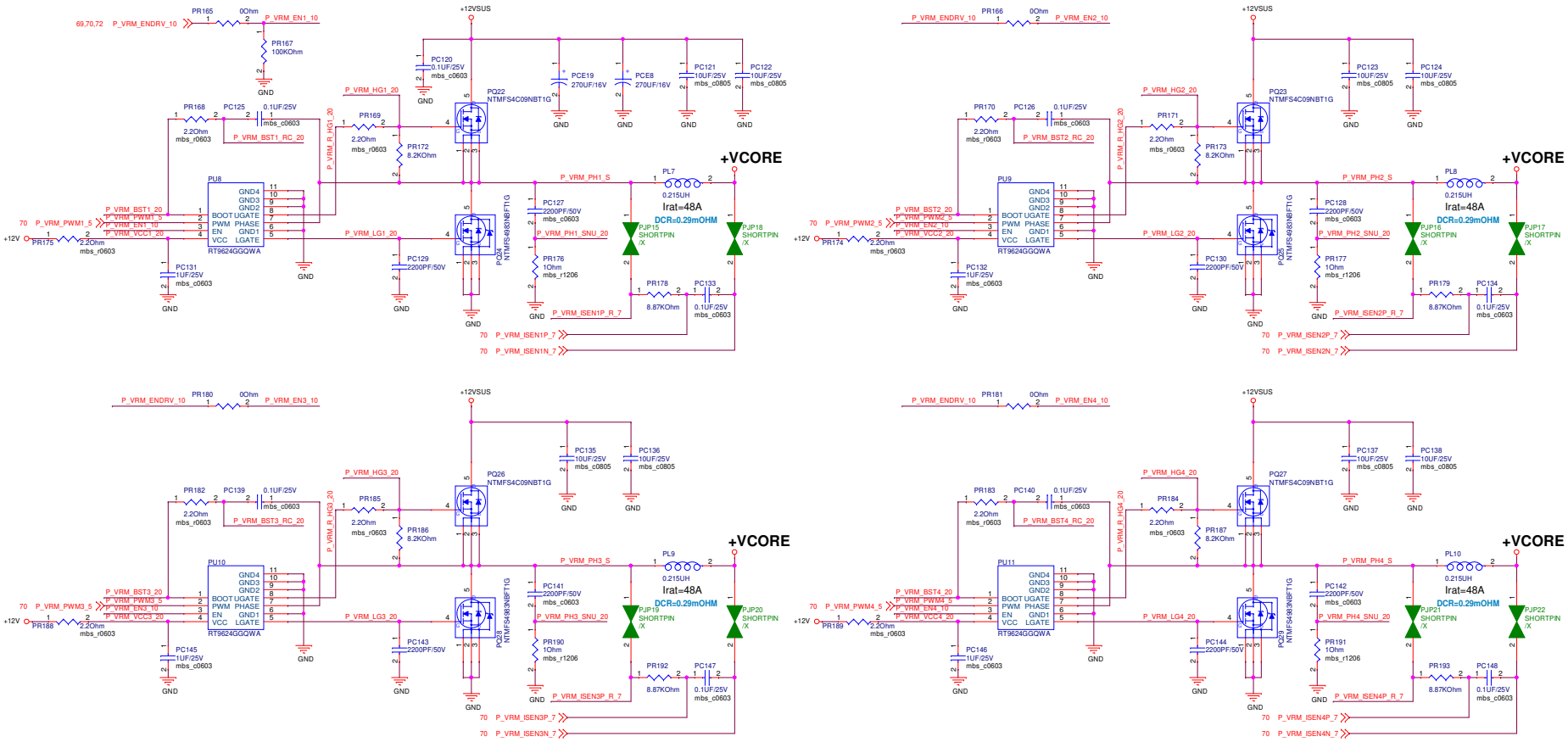
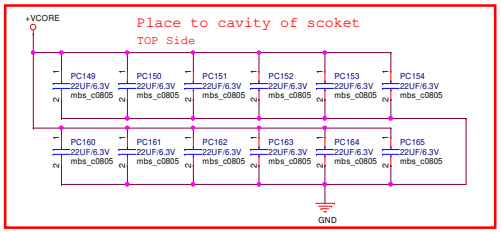
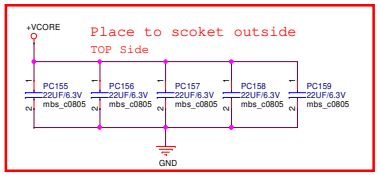
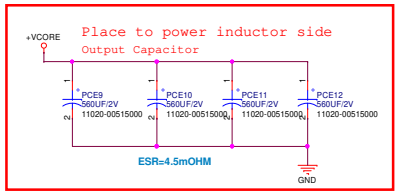
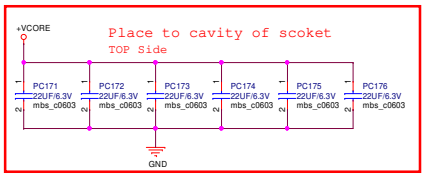
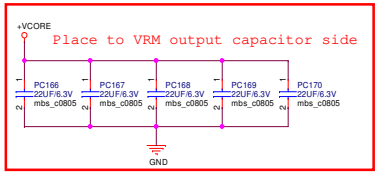




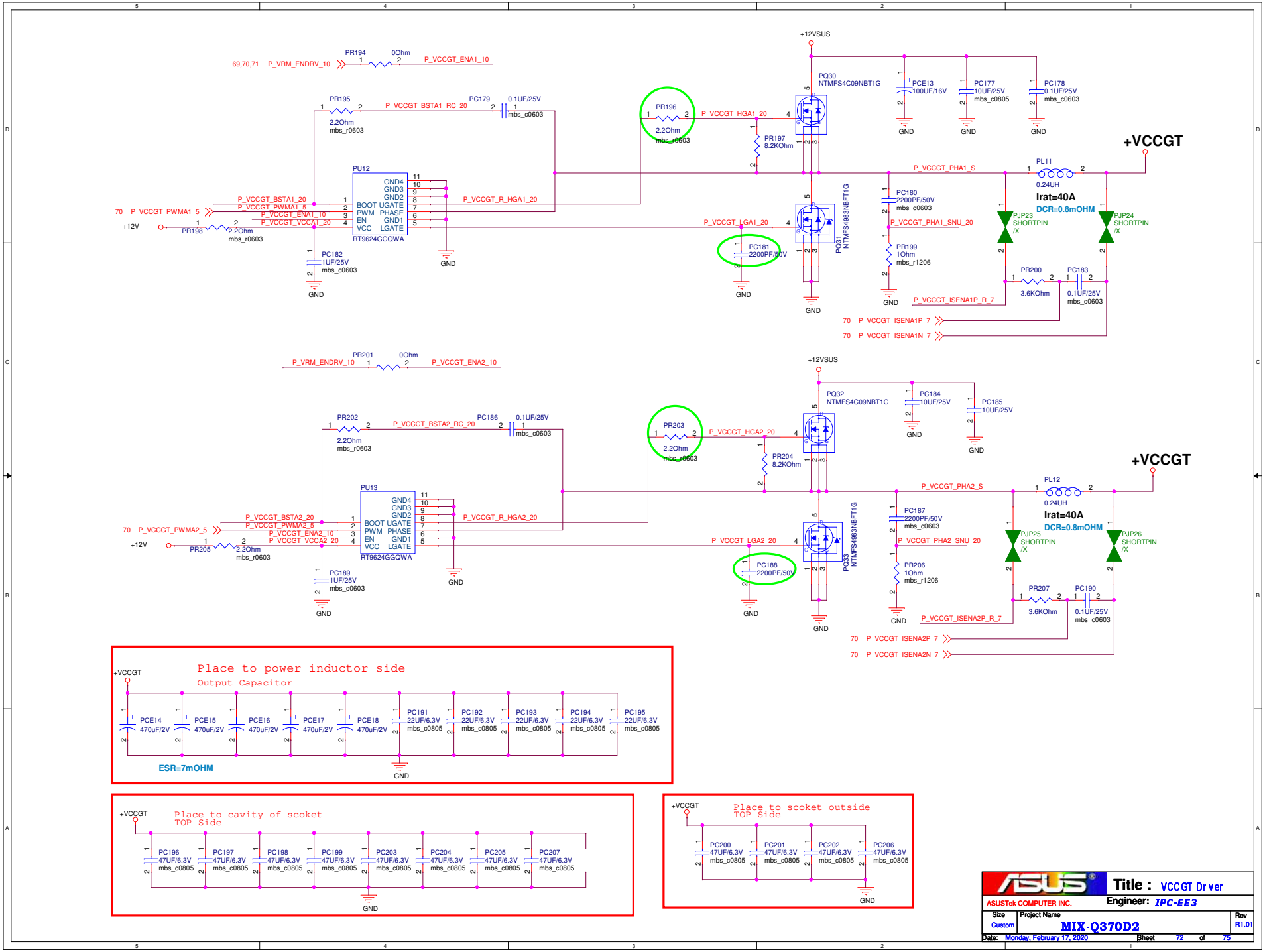








ASUSTek COMPUTER INC.	Title : VCORE Driver	
	Engineer: IPC-EE3	
Size: C	Project Name: MIX-Q370D2	Rev: R1.01
Date: Monday, February 17, 2020	Sheet 71 of 75	


+12VSUS
PR194 0Ohm
69,70,71 P_VRM_ENDRV_10
P_VCCGT_ENA1_10
PR195 2.2Ohm mbs_r0603
P_VCCGT_BSTA1_RC_20
PC179 0.1UF/25V mbs_c0603
PR196 2.2Ohm mbs_r0603
P_VCCGT_HGA1_20
PQ30 NTMFS4C09NBT1G
PR197 8.2KOhm
PCE13 100UF/16V
PC177 10UF/25V mbs_c0805
PC178 0.1UF/25V mbs_c0603
GND
+VCCGT
PU12
RT9624GGQWA
GND4 GND3 GND2 BOOT UGATE PWM PHASE EN GND1 VCC LGATE
P_VCCGT_BSTA1_20
P_VCCGT_PWMA1_5
P_VCCGT_ENA1_10
P_VCCGT_VCCA1_20
P_VCCGT_R_HGA1_20
70 P_VCCGT_PWMA1_5
+12V
PR198 2.2Ohm mbs_r0603
PC182 1UF/25V mbs_c0603
P_VCCGT_LGA1_20
PC181 2200PF/50V
PQ31 NTMFS4983NBFT1G
P_VCCGT_PHA1_S
PL11 0.24UH
Irat=40A
DCR=0.8mOHM
PC180 2200PF/50V mbs_c0603
P_VCCGT_PHA1_SNU_20
PR199 1Ohm mbs_r1206
PJP23 SHORTPIN /X
PJP24 SHORTPIN /X
PR200 3.6KOhm
PC183 0.1UF/25V mbs_c0603
P_VCCGT_ISENA1P_R_7
70 P_VCCGT_ISENA1P_7
70 P_VCCGT_ISENA1N_7
PR201 0Ohm
P_VRM_ENDRV_10
P_VCCGT_ENA2_10
PR202 2.2Ohm mbs_r0603
P_VCCGT_BSTA2_RC_20
PC186 0.1UF/25V mbs_c0603
PR203 2.2Ohm mbs_r0603
P_VCCGT_HGA2_20
PQ32 NTMFS4C09NBT1G
PR204 8.2KOhm
PC184 10UF/25V
PC185 10UF/25V
PU13
RT9624GGQWA
P_VCCGT_BSTA2_20
P_VCCGT_PWMA2_5
P_VCCGT_ENA2_10
P_VCCGT_VCCA2_20
P_VCCGT_R_HGA2_20
70 P_VCCGT_PWMA2_5
PR205 2.2Ohm mbs_r0603
PC189 1UF/25V mbs_c0603
P_VCCGT_LGA2_20
PC188 2200PF/50V
PQ33 NTMFS4983NBFT1G
P_VCCGT_PHA2_S
PL12 0.24UH
Irat=40A
DCR=0.8mOHM
PC187 2200PF/50V mbs_c0603
P_VCCGT_PHA2_SNU_20
PR206 1Ohm mbs_r1206
PJP25 SHORTPIN /X
PJP26 SHORTPIN /X
PR207 3.6KOhm
PC190 0.1UF/25V mbs_c0603
P_VCCGT_ISENA2P_R_7
70 P_VCCGT_ISENA2P_7
70 P_VCCGT_ISENA2N_7
Place to power inductor side
Output Capacitor
PCE14 470uF/2V
PCE15 470uF/2V
PCE16 470uF/2V
PCE17 470uF/2V
PCE18 470uF/2V
PC191 22UF/6.3V mbs_c0805
PC192 22UF/6.3V mbs_c0805
PC193 22UF/6.3V mbs_c0805
PC194 22UF/6.3V mbs_c0805
PC195 22UF/6.3V mbs_c0805
ESR=7mOHM
Place to cavity of scoket
TOP Side
PC196 47UF/6.3V mbs_c0805
PC197 47UF/6.3V mbs_c0805
PC198 47UF/6.3V mbs_c0805
PC199 47UF/6.3V mbs_c0805
PC203 47UF/6.3V mbs_c0805
PC204 47UF/6.3V mbs_c0805
PC205 47UF/6.3V mbs_c0805
PC207 47UF/6.3V mbs_c0805
Place to scoket outside
TOP Side
PC200 47UF/6.3V mbs_c0805
PC201 47UF/6.3V mbs_c0805
PC202 47UF/6.3V mbs_c0805
PC206 47UF/6.3V mbs_c0805
Title : VCCGT Driver
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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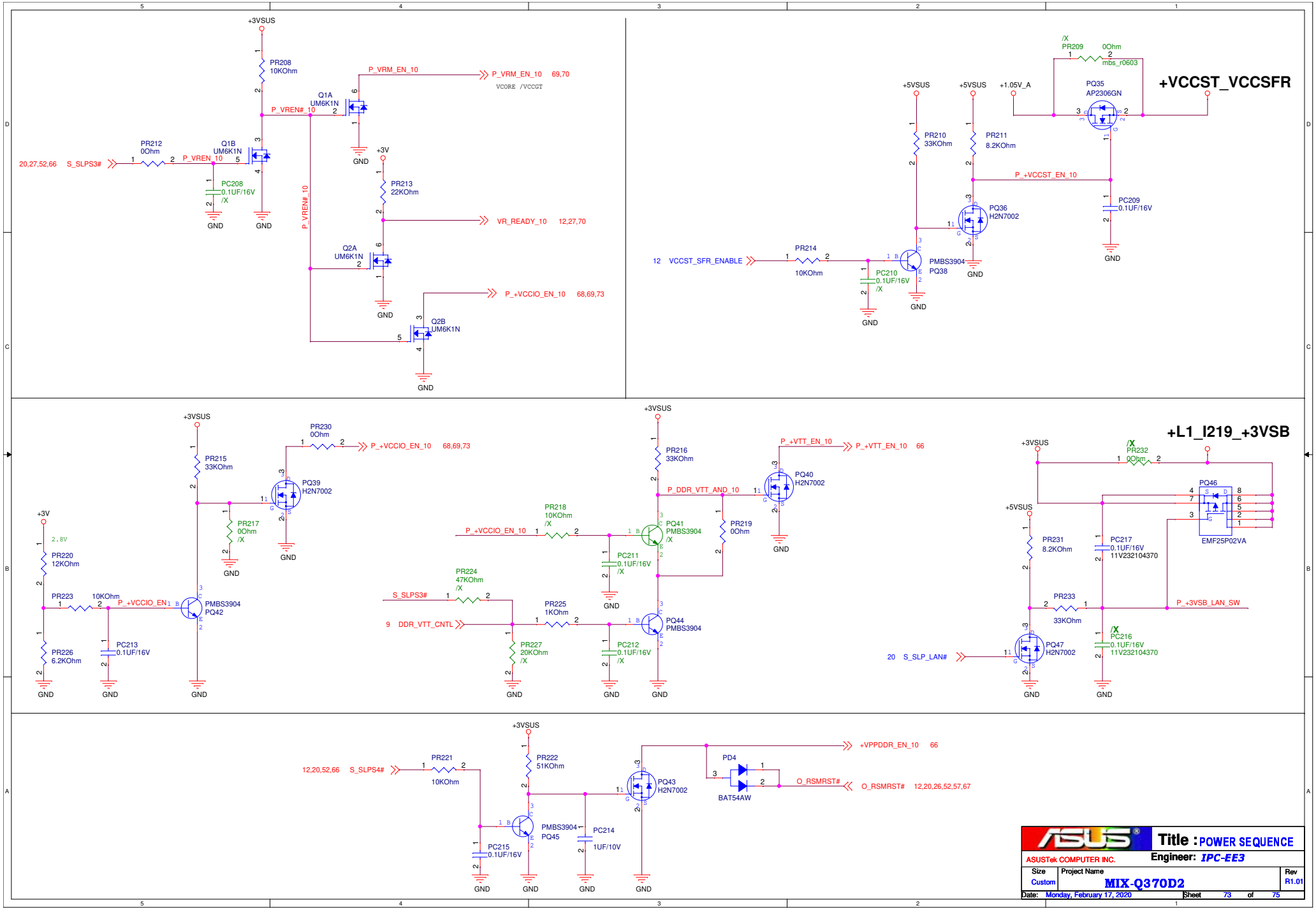
+VCCST_VCCSFR
+L1_I219_+3VSB
+3VSUS
PR208 10KOhm
P_VRM_EN_10
P_VRM_EN_10 69,70
VCORE /VCCGT
Q1A UM6K1N
P_VREN#_10
PR212 0Ohm
Q1B UM6K1N
20,27,52,66 S_SLPS3#
PC208 0.1UF/16V /X
GND
+3V
PR213 22KOhm
VR_READY_10 12,27,70
Q2A UM6K1N
P_+VCCIO_EN_10 68,69,73
Q2B UM6K1N
/X PR209 0Ohm mbs_r0603
+5VSUS
+1.05V_A
PQ35 AP2306GN
PR210 33KOhm
PR211 8.2KOhm
P_+VCCST_EN_10
PQ36 H2N7002
PC209 0.1UF/16V
12 VCCST_SFR_ENABLE
PR214 10KOhm
PC210 0.1UF/16V /X
PMBS3904 PQ38
PR230 0Ohm
PR215 33KOhm
PQ39 H2N7002
PR217 0Ohm /X
2.8V
PR220 12KOhm
PR223 10KOhm
P_+VCCIO_EN1
PMBS3904 PQ42
PR226 6.2KOhm
PC213 0.1UF/16V
PR216 33KOhm
P_+VTT_EN_10
P_+VTT_EN_10 66
P_DDR_VTT_AND_10
PQ40 H2N7002
PR218 10KOhm /X
PQ41 PMBS3904 /X
PR219 0Ohm
PC211 0.1UF/16V /X
PR224 47KOhm /X
S_SLPS3#
PR225 1KOhm
9 DDR_VTT_CNTL
PQ44 PMBS3904
PR227 20KOhm /X
PC212 0.1UF/16V /X
/X PR232 0Ohm
PQ46 EMF25P02VA
PR231 8.2KOhm
PC217 0.1UF/16V 11V232104370
PR233 33KOhm
P_+3VSB_LAN_SW
20 S_SLP_LAN#
PQ47 H2N7002
/X PC216 0.1UF/16V 11V232104370
12,20,52,66 S_SLPS4#
PR221 10KOhm
PR222 51KOhm
PQ43 H2N7002
+VPPDDR_EN_10 66
PD4 BAT54AW
O_RSMRST#
O_RSMRST# 12,20,26,52,57,67
PMBS3904 PQ45
PC214 1UF/10V
PC215 0.1UF/16V
Title : POWER SEQUENCE
ASUSTek COMPUTER INC.
Engineer: IPC-EE3
Size Custom
Project Name MIX-Q370D2
Rev R1.01
Date: Monday, February 17, 2020
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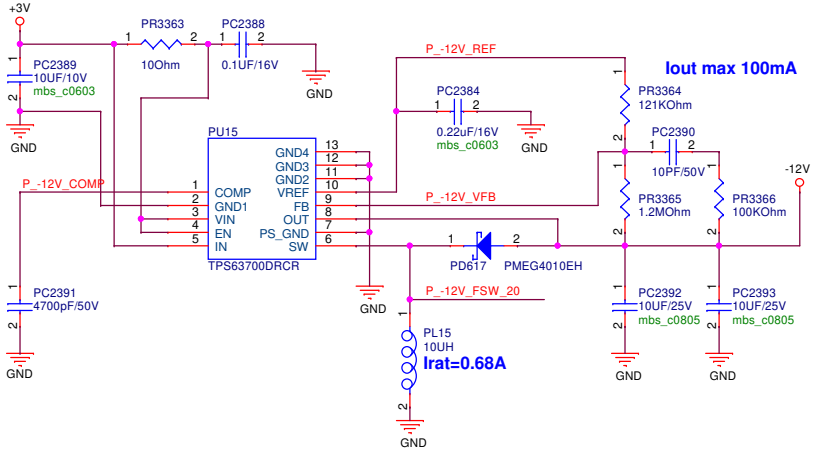
-12V POWER



ASUS	Title : -12V	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q370D2	Rev R1.01
Date: Monday, February 17, 2020	Sheet 74 of 75	

History 2019/12/10 R1.01

01) modify PCIe/SATA Auto-detec GPIO to SATAGP1 at p.19
02) mount GR4 for HDMI 2.0 SI tuning at p.33
03) change PN for BOM at p.55, 71 (11020-00515000 need change footprint)
04) remove AMP/Speaker/DMIC and i211 ex-ROM at p.35, 37, 38, 41
05) add reserve PD resister at DIO p.57
06) add AAFP p.35, 36
07) change L1L1 package for damage risk p.39
08) change TPM module to SPI interface NPCT750AAAYX at p.17, 21, 28, 29
09) modify Block diagram at p.1
10) modify PR4 to 30kohm for +5VSUS OCP tuning at p.65

History 2019/12/12

01) change DIO default PD at p.57
02) change L1L1 package for common pool use at p.39
03) change 11020-00515000 footprint at p.71
04) change HDMI2.0 to HDMI1.4 at p.6, 21, 33, 74
05) change DP to VGA at p.6, 21, 31, 32
06) add COM2 and delete COM_J1 at p.52, 55, 57

History 2019/12/17

01) change COM2 to SMT packge at p.57
02) unmount SD4/SR416/OR7, mount SR137 for power sequence tPCH07 at p.20, 52

History 2019/12/19

01) modfiy SX1, L1X1, L2X1, OCE2, D4UCE1, UF6 for BOM at p.15, 16, 39, 41, 56, 57
02) modfiy PCB P/N at p.63
03) change L1L1 package for damage risk p.39
04) change LAN+USB30 Connector to LAN+USB31 at p.40, 42

History 2019/12/26

01) modfiy D4UCE1 footprint at p.15
02) modfiy USB31_56 P/N at p.46

History 2019/12/27

01) add -12V for COM2_RS232 at p.74