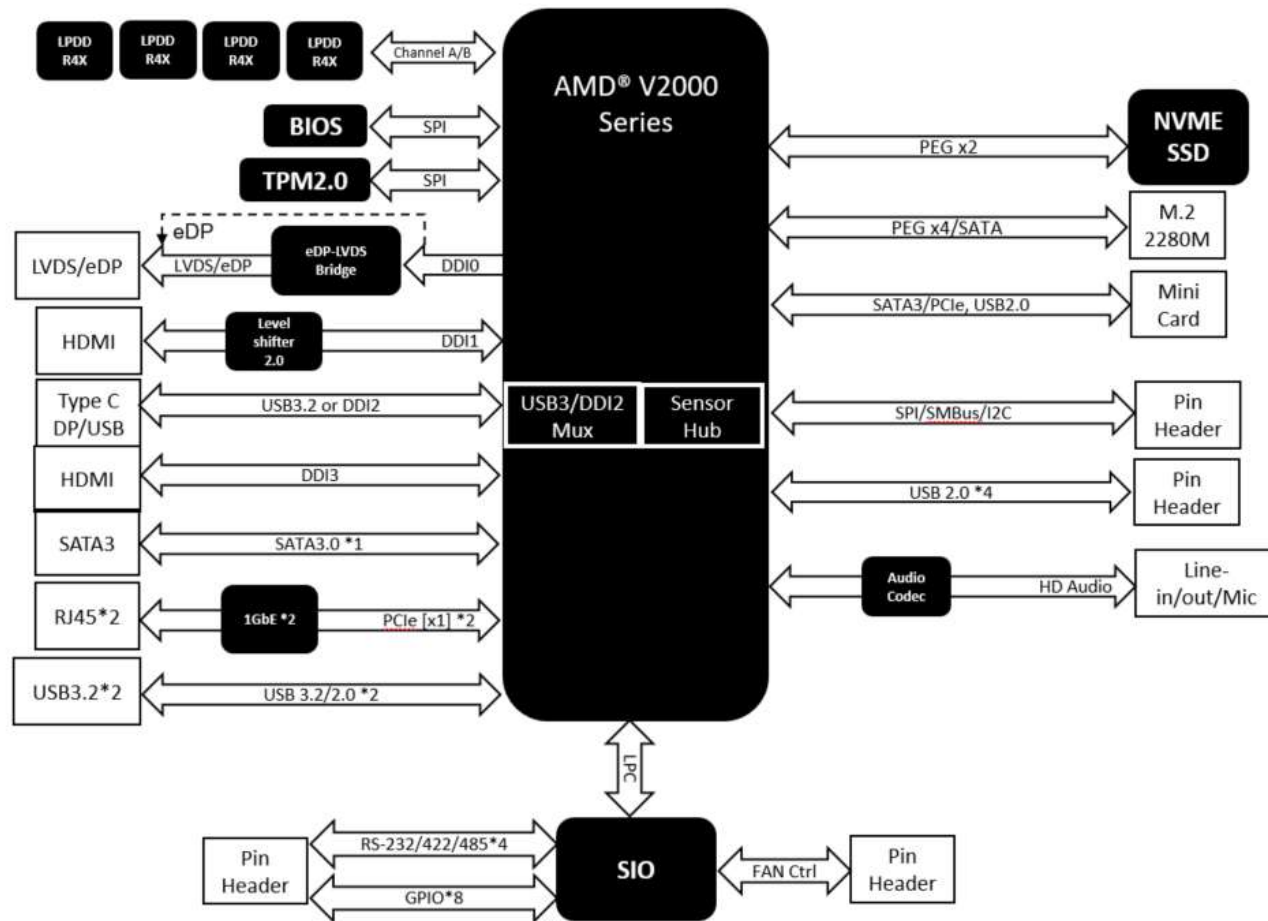


PICO-V2K4 Block



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44	PWR08_+V1P8S/ +VDDPS
45	Sequence
46	History

SOC AGPIO Pins :

Name	Power Well	Default	GPIO Function
AGPIO0	VDD 33 S5		PM PWRBTN#
AGPIO1	VDD 33 S5		PM SYSRST#
AGPIO2	VDD 33 S5		PCIE_WAKE#
AGPIO3			SMB_ALERT#
AGPIO4			APU AGPIO4(TP)
AGPIO5			SSD SATA DeVSLP
AGPIO6			I2C SOC_IRQ
AGPIO7			
AGPIO8			SIO_OVT#
AGPIO9			I2C_SDA_EC
AGPIO10	VDD 33 S5		SDA3_GPIO
AGPIO11	VDD 33 S5		M2MDET
AGPIO12	VDD 33 S5		
AGPIO16			USB_TYPEC_OC
AGPIO17			USB_OCF_1
AGPIO18			USB_OCF_2
AGPIO19	VDD 33 S5		I2C3_SCL
AGPIO20	VDD 33 S5		I2C3_SDA
AGPIO21			
AGPIO22			SIO_PME#
AGPIO23			AC_PRES
AGPIO24			USB_OCF_3
AGPIO29	VDD 18		TPM_SPI_CS#
AGPIO30	VDD 18 S5		ESPI_SPI_CS#
AGPIO31			
AGPIO32			LPC_RST#_R
AGPIO40			I2C_SCL_EC
AGPIO68			
AGPIO69			I2C_IRQ_EC
AGPIO84			
AGPIO85			
AGPIO86			SPI_CLK2_R
AGPIO87			LPC_SERIRQ
AGPIO88			TPM_PIRQ
AGPIO89			
AGPIO90			
AGPIO91			SPKR
AGPIO92	VDD 33		CLKREQ0#_SSD
AGPIO115	VDD 33		CLKREQ0#_LAN1
AGPIO116	VDD 33		CLKREQ2#_LAN2
AGPIO129	VDD 33/VDD 18		KBRST#
AGPIO130			SATA_ACT#
AGPIO144			
AGPIO256			
AGPIO257			
AGPIO258			
AGPIO259			
AGPIO260			
AGPIO261			
AGPIO262			
AGPIO263			
AGPIO264			
AGPIO265			
AGPIO269			
AGPIO270			

SOC EGPIO Pins :

Name	Power Well	Default	GPIO Function
EGPIO26			APU_PCIE_RST#
EGPIO27			PCIE_RST1#
EGPIO42			
EGPIO67			SPI_ROM_REQ#
EGPIO70			
EGPIO74			LPCCCLK0
EGPIO75			LPCCCLK1
EGPIO76			
EGPIO104			LAD0_ESPI1_DATA0
EGPIO105			LAD1_ESPI1_DATA1
EGPIO106			LAD2_ESPI1_DATA2
EGPIO107			LAD3_ESPI1_DATA3
EGPIO108	VDD 33		LPC_DRQ#
EGPIO109			LPC_FRAME#
EGPIO113	VDD 33		SMB_CLK
EGPIO114	VDD 33		SMB_DATA
EGPIO120	VDD 33		
EGPIO121	VDD 33		
EGPIO131	VDD 33		CLKREQ3#_MINI
EGPIO132	VDD 33		CLKREQ4#_M2M
EGPIO140			
EGPIO141			
EGPIO142			
EGPIO143			
EGPIO145	VDD 18 S5		I2C0_SCL
EGPIO146	VDD 18 S5		I2C0_SDA
EGPIO147	VDD 18 S5		I2C1_SCL
EGPIO148	VDD 18 S5		I2C1_SDA
EGPIO266			
EGPIO267			
EGPIO268			
EGPIO271			

Advanced GPIO - can be used for interrupt, wake, or GPIO.

Enhanced GPIO - can be used only for GPIO.

F81966D GPIO Pins :

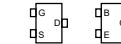
Name	Tolerance	Power Well	Default	Function
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#
GPIO02	5V	I_VSB3V	Native	SIO_SUS_WARN#_R
GPIO03	5V	I_VSB3V	Native	SIO_SUS_ACK#_R
GPIO04	5V	I_VSB3V	Native	SIO_SUS_SUS#
GPIO05	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO06	5V	I_VSB3V	Native	LAN1_DISABLE#
GPIO07	5V	I_VSB3V	Native	BID0
GPIO10	5V	I_VSB3V	Native	AUDIO_MUTE#
GPIO11	5V	I_VSB3V	Native	EN_USB
GPIO12	5V	I_VSB3V	Native	I2C_SCL_SIO
GPIO13	5V	I_VSB3V	Native	I2C_SDA_SIO
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP
GPIO15	5V	I_VSB3V	Native	WDT_RST#
GPIO16	5V	I_VSB3V	Native	USB_PD_EEPROM_CTRL
GPIO17	5V	I_VSB3V	Native	PECI
GPIO20	5V	I_VSB3V	Native	ALERT#
GPIO21	5V	I_VSB3V	Native	SIO_ATXPG
GPIO22	5V	I_VSB3V	Native	PWSIN#
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#
GPIO24	5V	I_VSB3V	Native	PM_SLP_S3#
GPIO25	5V	I_VSB3V	Native	PS_CMD
GPIO26	5V	VBAT	Native	PCH_PWROK
GPIO27	5V	VBAT	Native	SIO_RSMRST#
GPIO30	5V	3VCC	Native	DCD3#
GPIO31	5V	3VCC	Native	RI3#
GPIO32	5V	3VCC	Native	CTS3#
GPIO33	5V	3VCC	Native	CTS4#
GPIO34	5V	3VCC	Native	RTS3#
GPIO35	5V	3VCC	Native	DSR3#
GPIO36	5V	3VCC	Native	TX3#
GPIO37	5V	3VCC	Native	RX3#
GPIO40	5V	3VCC	Native	DCD4#
GPIO41	5V	3VCC	Native	TX4#
GPIO42	5V	3VCC	Native	CTS4#
GPIO43	5V	3VCC	Native	DTR4#
GPIO44	5V	3VCC	Native	RTS4#
GPIO45	5V	3VCC	Native	DSR4#
GPIO46	5V	3VCC	Native	TX4#
GPIO47	5V	3VCC	Native	RX4#
GPIO50	5V	3VCC	Native	COM1_SLEW
GPIO51	5V	3VCC	Native	COM1_MODE0
GPIO52	5V	3VCC	Native	COM1_MODE1
GPIO53	5V	3VCC	Native	COM1_MODE2
GPIO54	5V	3VCC	Native	COM2_SLEW
GPIO55	5V	3VCC	Native	COM2_MODE0
GPIO56	5V	3VCC	Native	COM2_MODE1
GPIO57	5V	3VCC	Native	COM2_MODE2
GPIO60	5V	3VCC	Native	COM3_SLEW
GPIO61	5V	3VCC	Native	COM3_MODE0
GPIO62	5V	3VCC	Native	COM3_MODE1
GPIO63	5V	3VCC	Native	COM3_MODE2
GPIO64	5V	3VCC	Native	COM3_MODE3
GPIO65	5V	I_VSB3V	Native	I2C_SIO_IRQ
GPIO66	5V	VBAT	Native	DPWROK
GPIO67	5V	I_VSB3V	Native	PM_SLP_S5#
GPIO70	5V	3VCC	Native	LVDS_EN
GPIO71	5V	3VCC	Native	W_DISABLE0#
GPIO72	5V	3VCC	Native	CARD_PWR_OFF
GPIO73	5V	3VCC	Native	LVD1_PD#
GPIO74	5V	3VCC	Native	COM4_SLEW
GPIO75	5V	3VCC	Native	COM4_MODE0
GPIO76	5V	3VCC	Native	COM4_MODE1
GPIO77	5V	3VCC	Native	COM4_MODE2
GPIO80	5V	3VCC	Native	DIO_0
GPIO81	5V	3VCC	Native	DIO_1
GPIO82	5V	3VCC	Native	DIO_2
GPIO83	5V	3VCC	Native	DIO_3
GPIO84	5V	3VCC	Native	DIO_4
GPIO85	5V	3VCC	Native	DIO_5
GPIO86	5V	3VCC	Native	DIO_6
GPIO87	5V	3VCC	Native	DIO_7
GPIO90	5V	IFP	Native	LPC_DRQ#
GPIO91	5V	I_VSB3V	Native	KBRST#
GPIO92	5V	I_VSB3V	Native	BID1
GPIO93	5V	I_VSB3V	Native	MSDAT#
GPIO94	5V	I_VSB3V	Native	MSCLK#
GPIO95	5V	3VCC	Native	FAN_1_TAC
GPIO96	5V	3VCC	Native	SIO_BKCTL
GPIO97	5V	3VCC	Native	SIO_SSD_PWREN

Note:
REV means reserved

SMBus/I2C Addresses :

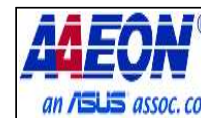
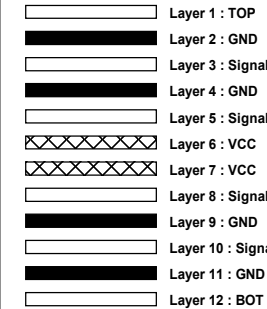
Device	Address
PTN3460	0x40h
GPIO IC (SIO 81966)	6Eh

PCB Footprints



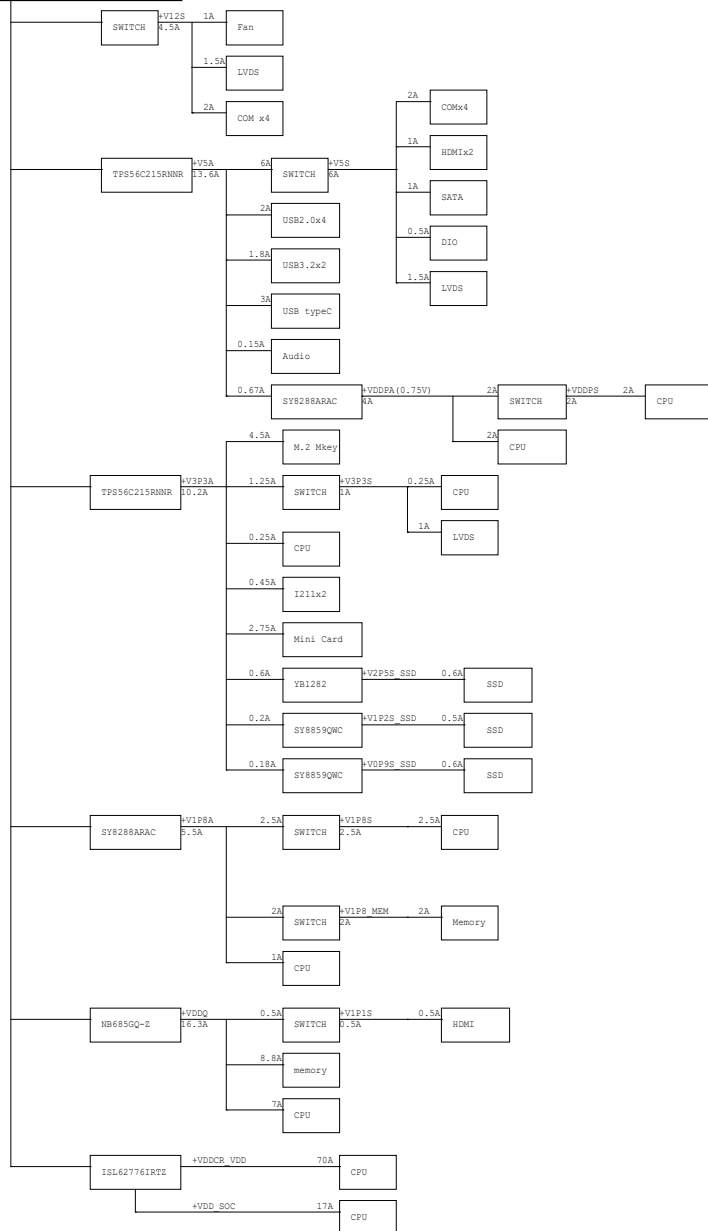
PCB STACK :

Impedance 50ohm +/-10%.

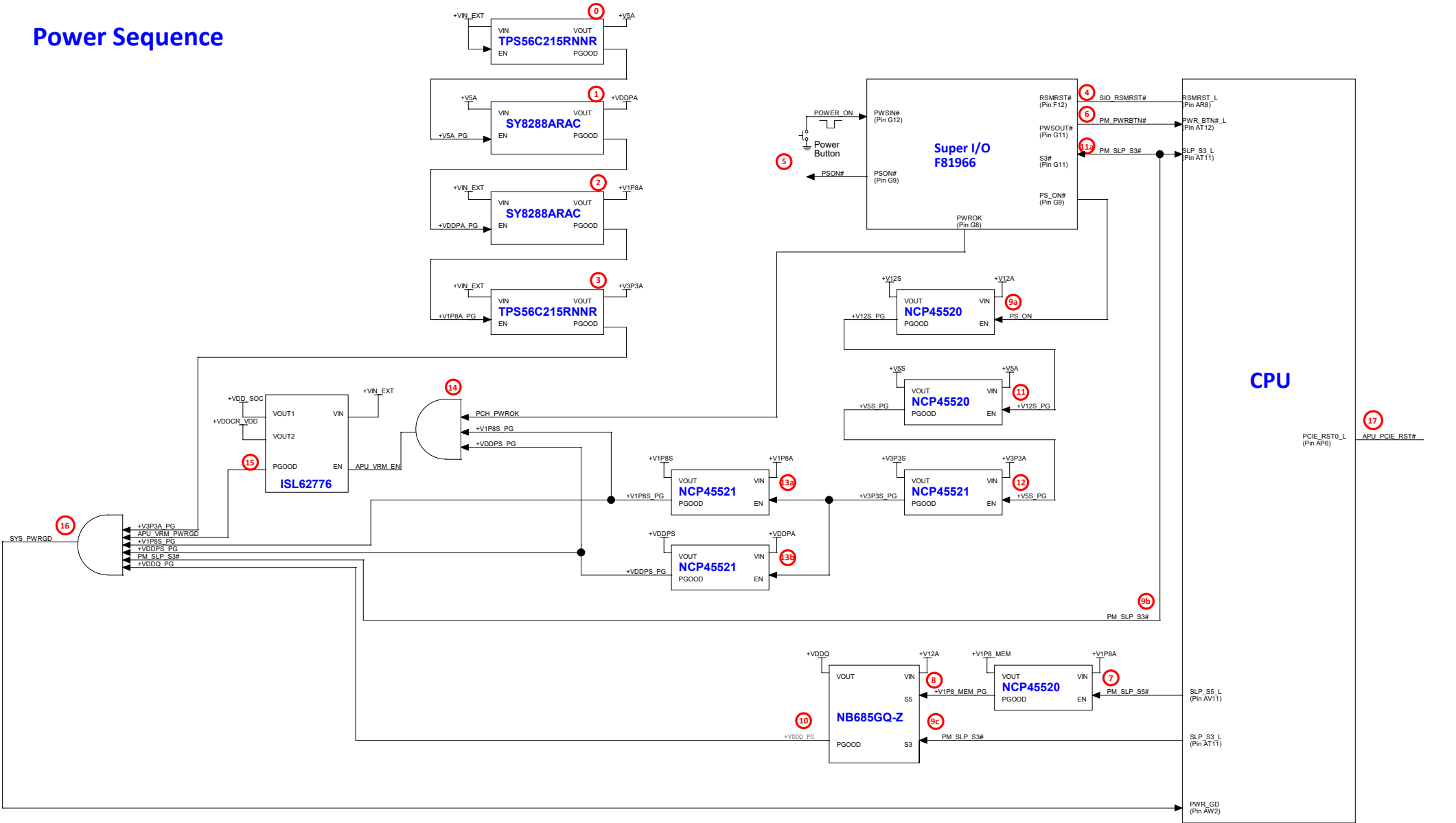


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Size Custom	Document Number PICO-V2K4	Rev: A0.1_0_0
Date: Monday, May 03, 2021		Sheet: 2 of 46

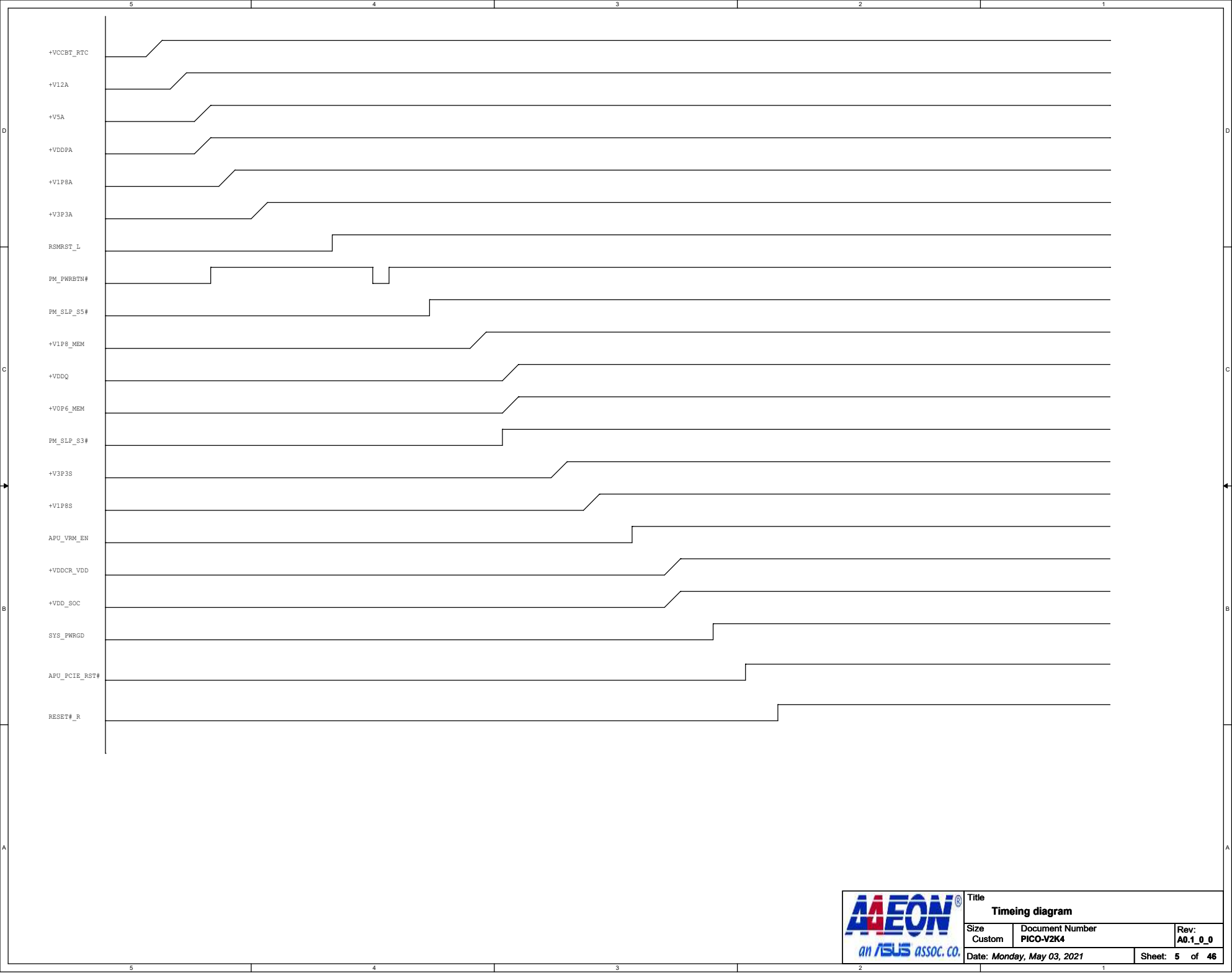
POWER CONNECTOR
+VIN_EXT(+V12A)



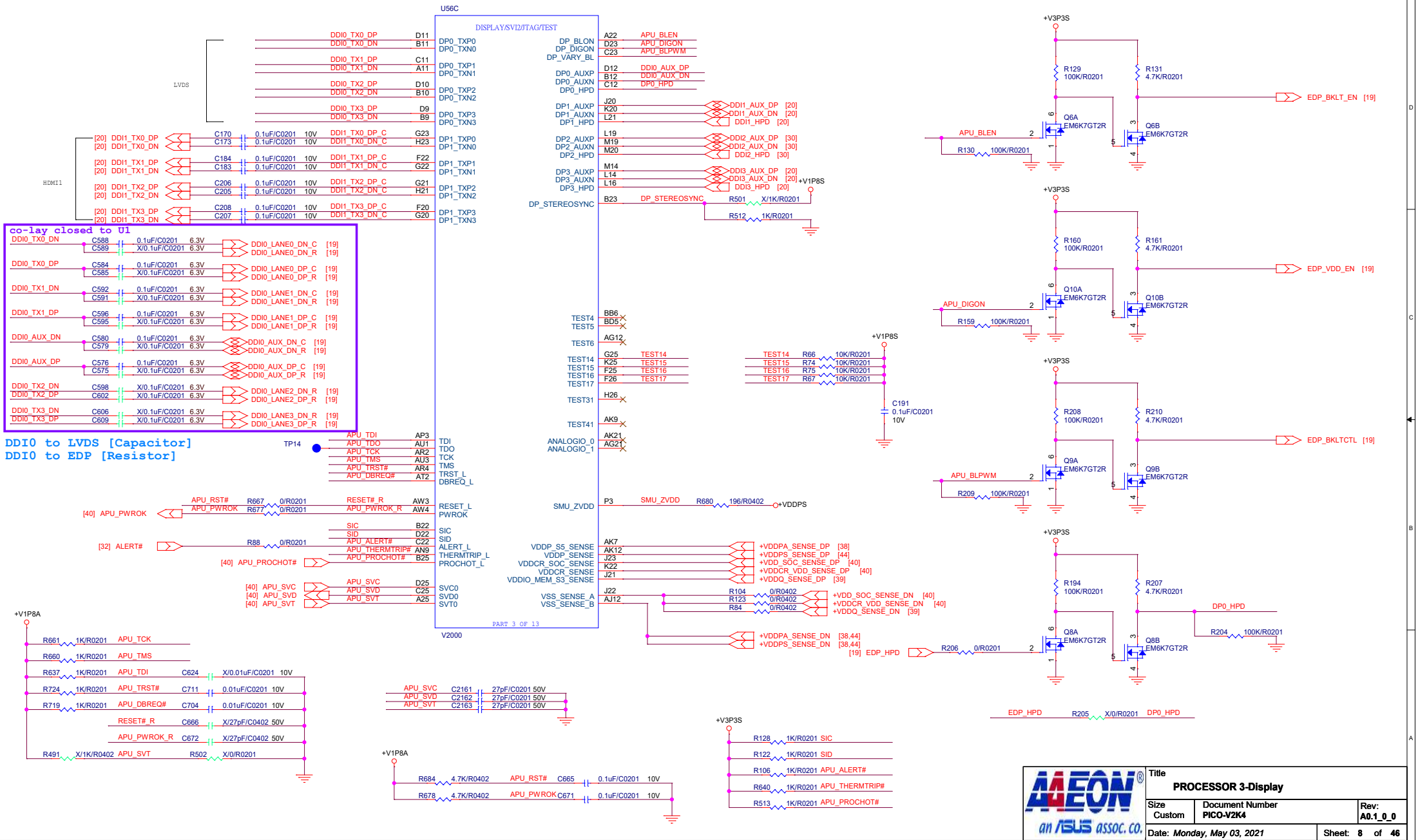
Power Sequence

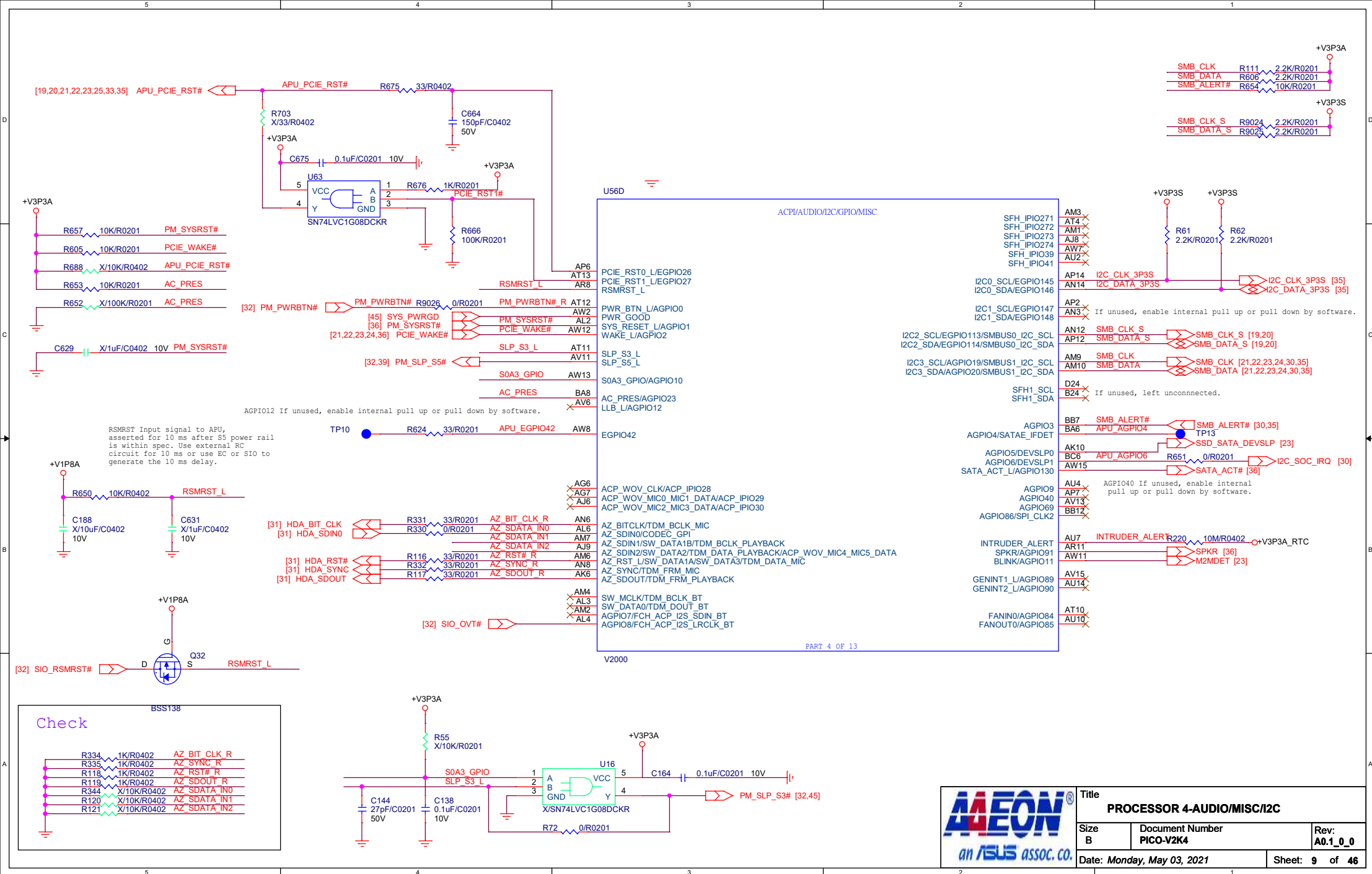


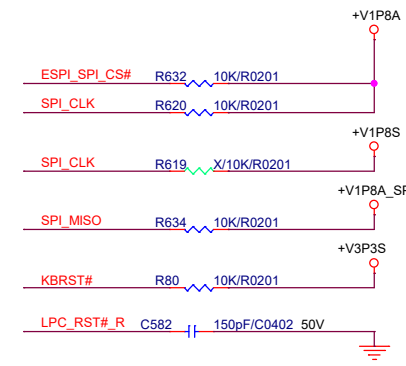
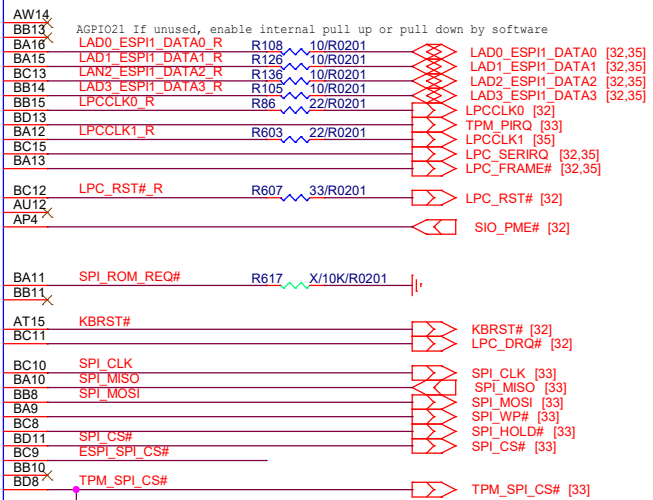
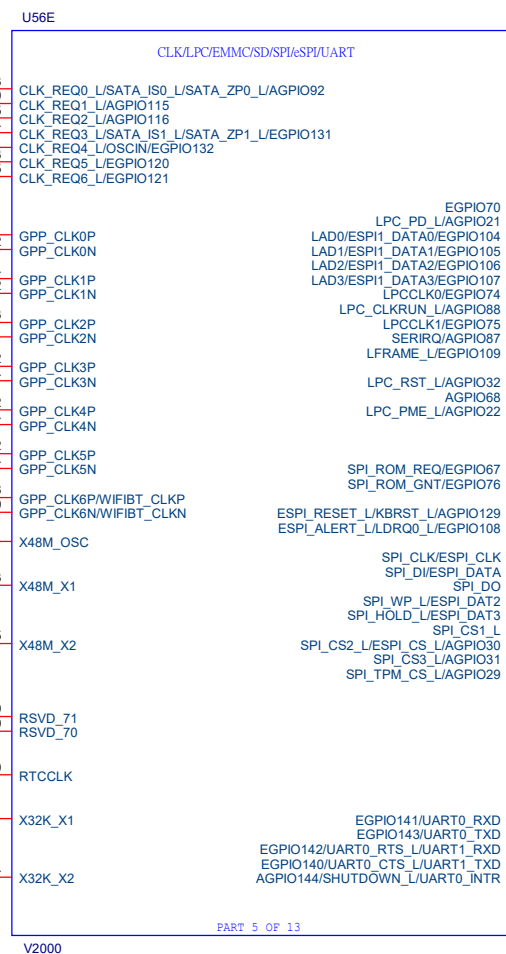
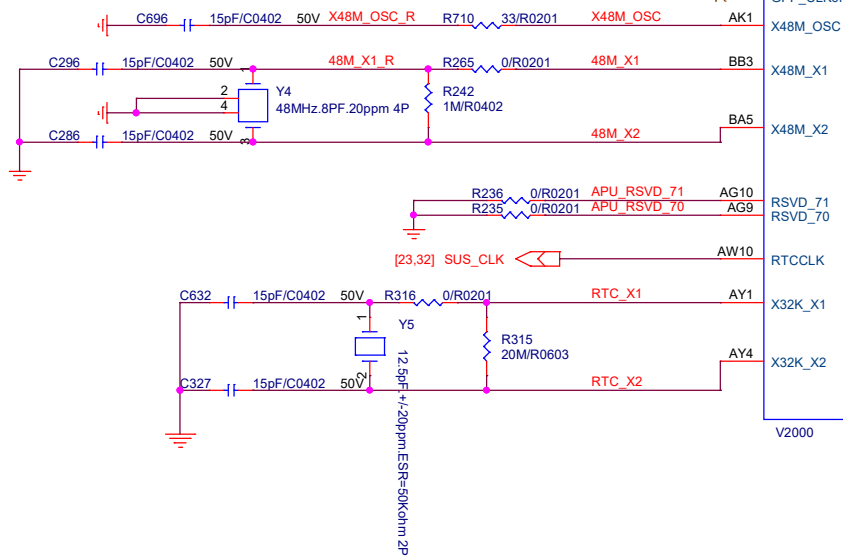
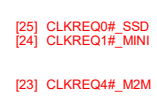
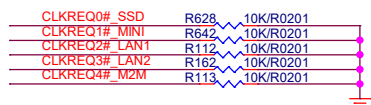
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Size Custom	Document Number PICO-V2K4	Rev. A0.1_0_0
Date: Monday, May 03, 2021		Sheet: 4 of 46

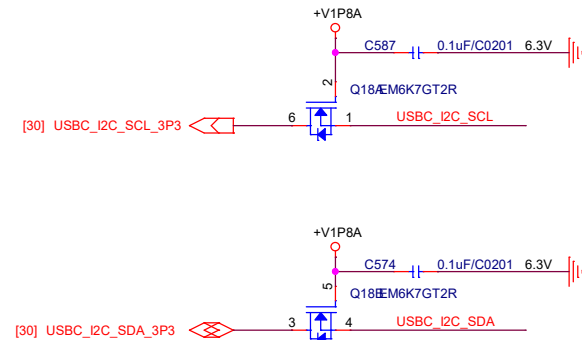
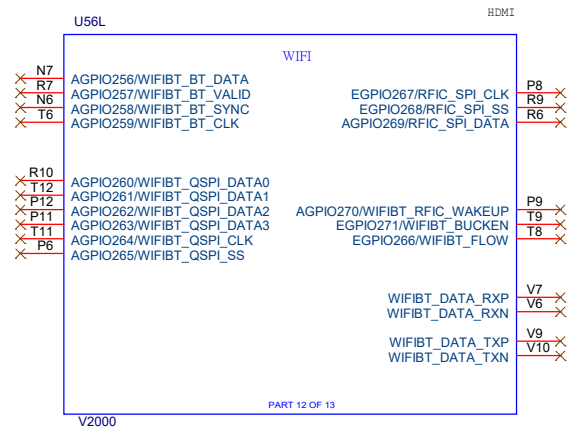
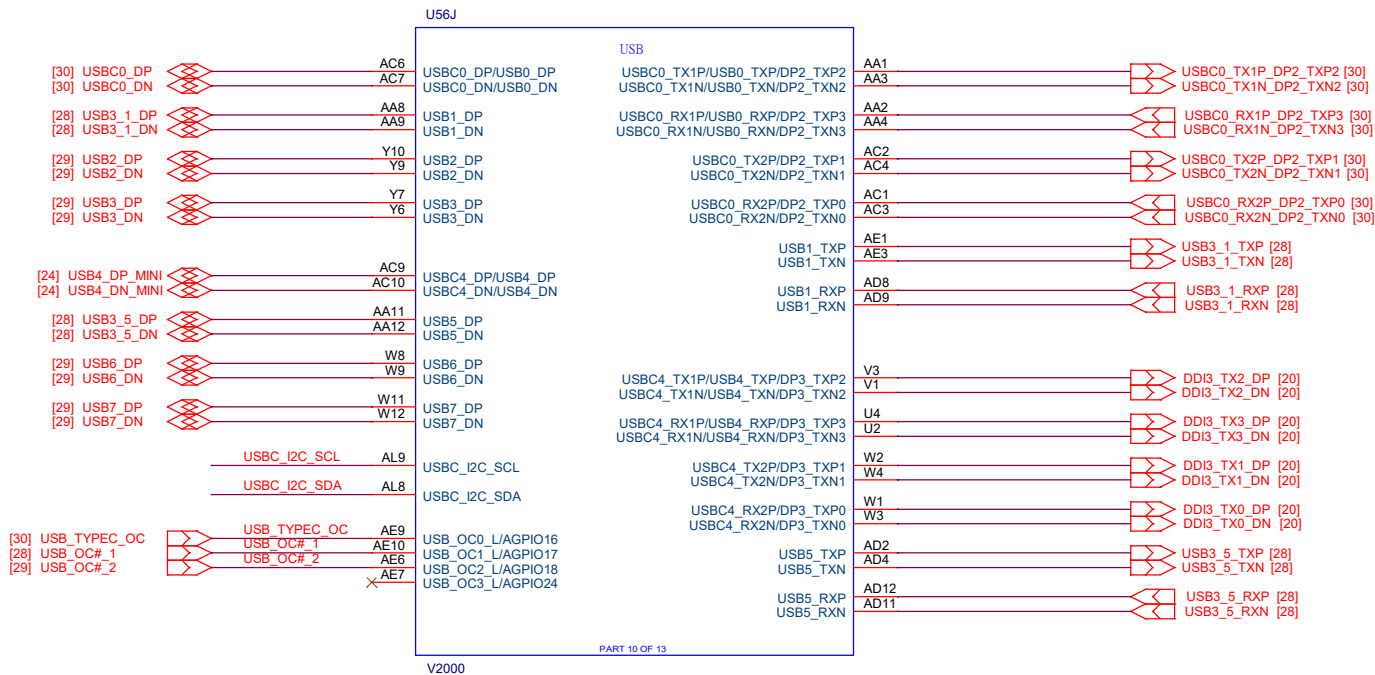
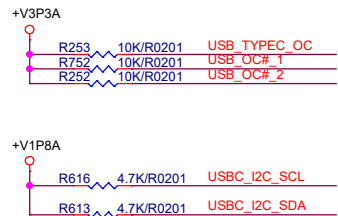


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Size Custom	Document Number PICO-V2K4	Rev: A0.1_0_0
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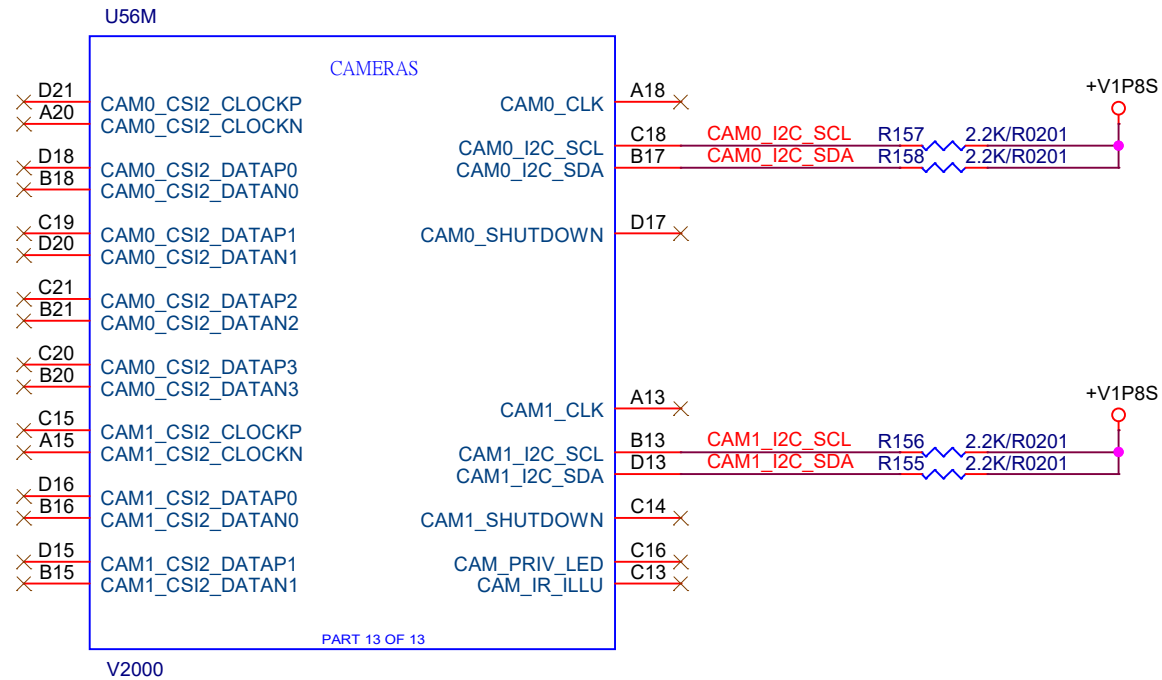




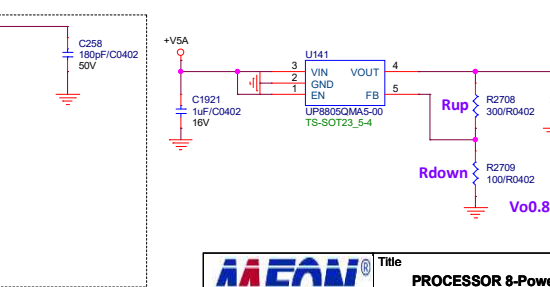
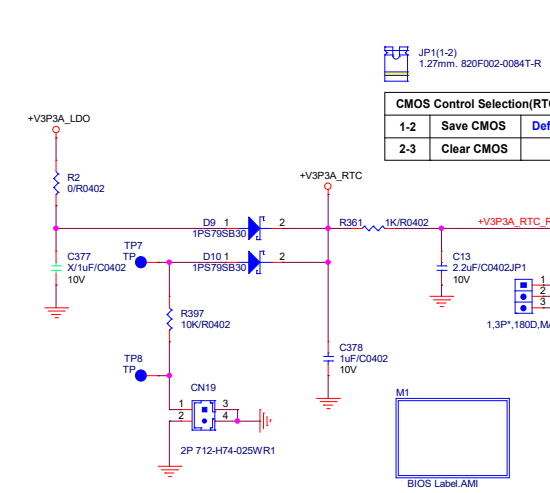
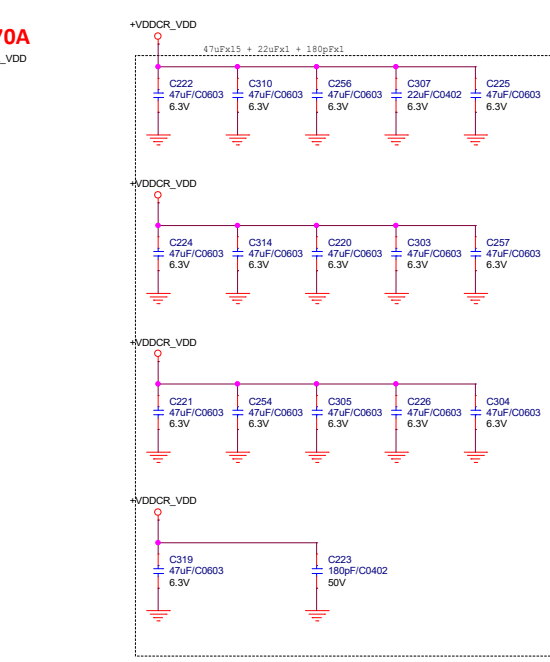
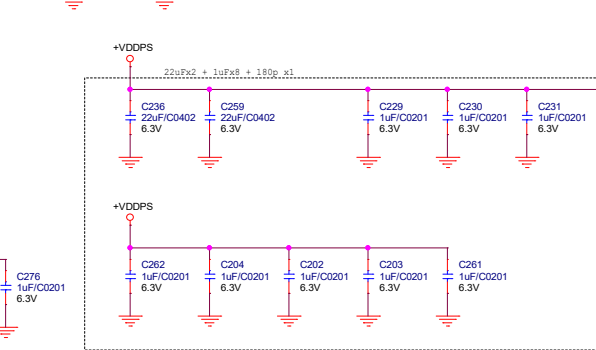
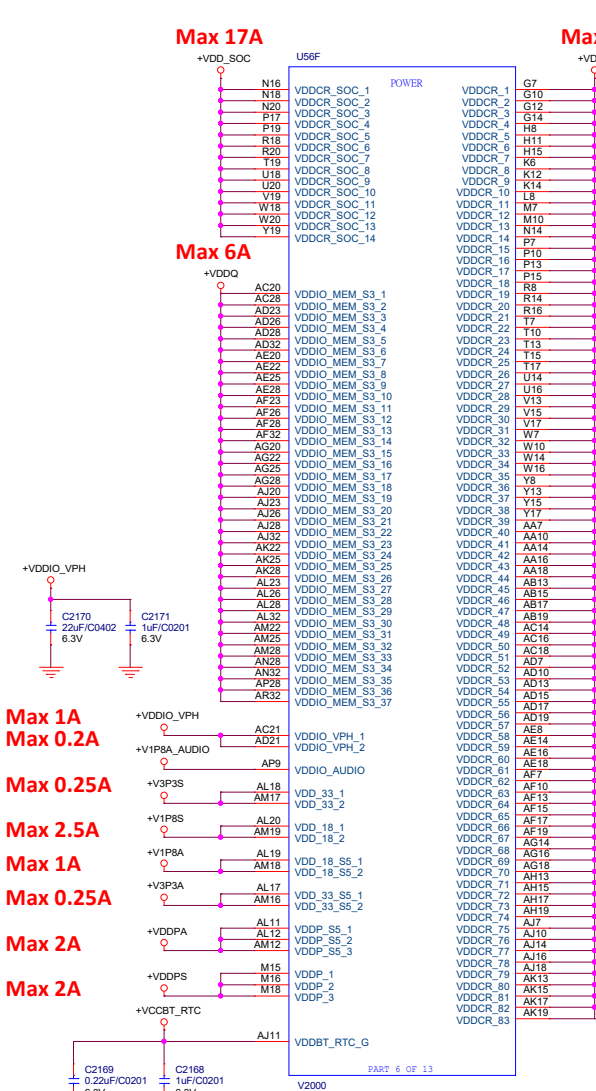
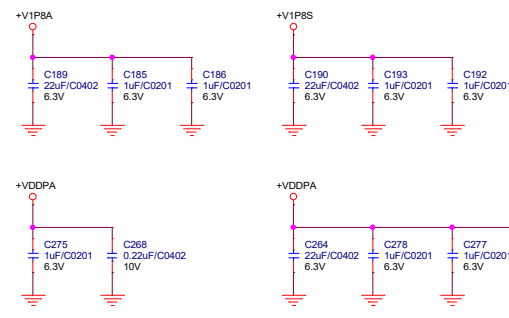
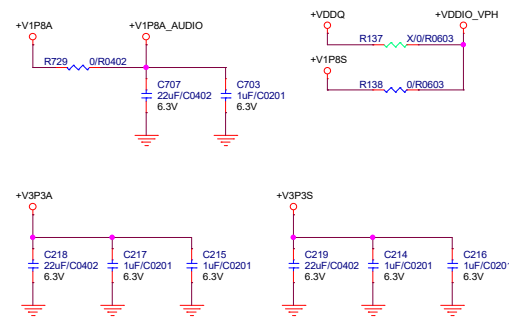
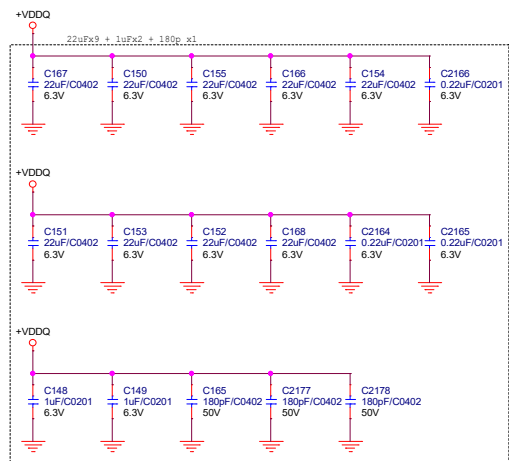
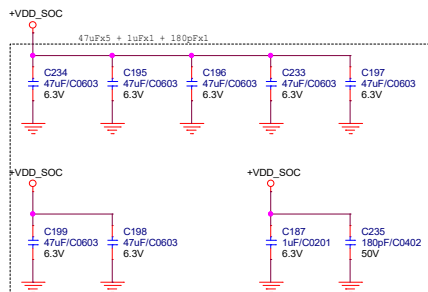




Title		
PROCESSOR 6-USB/WIFI		
Size	Document Number	Rev:
B	PICO-V2K4	A0.1_0_0
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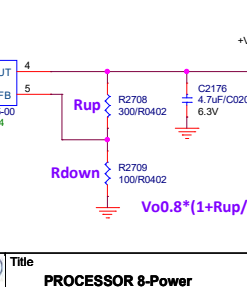
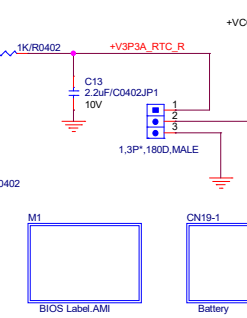


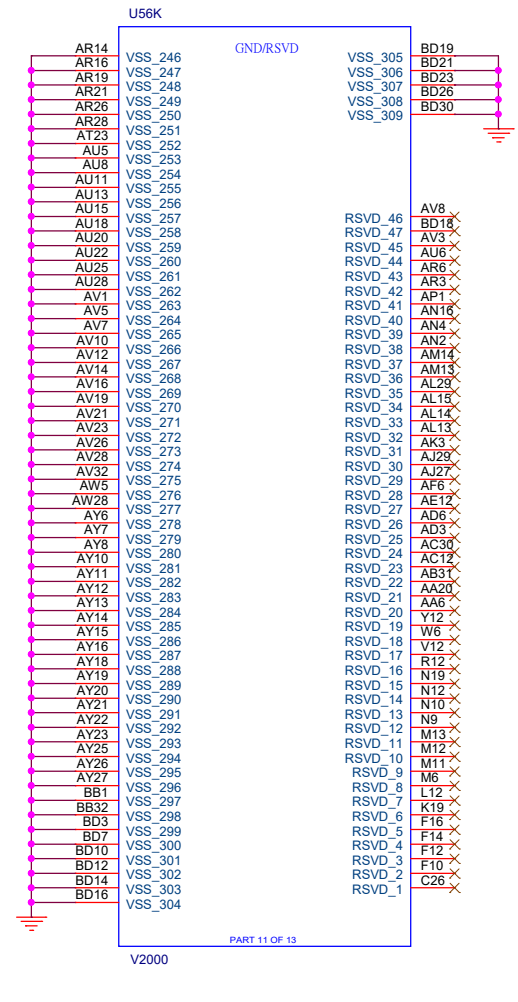
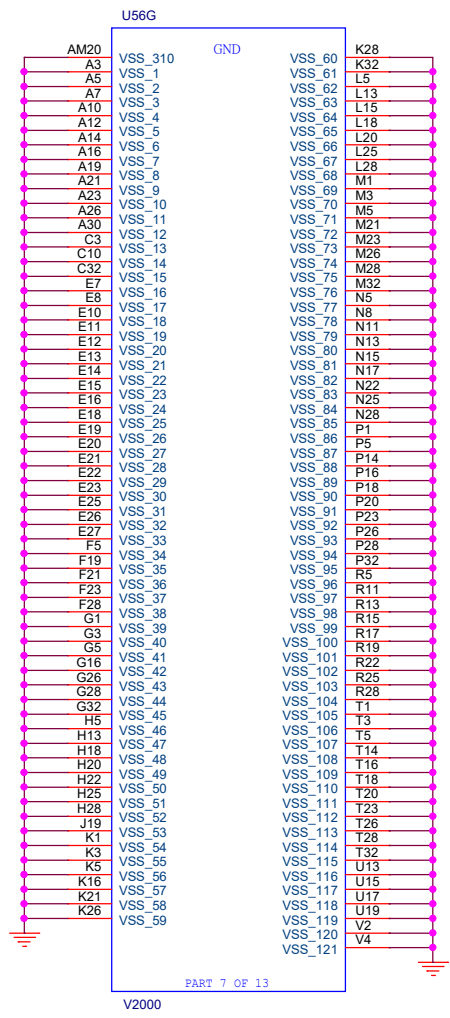
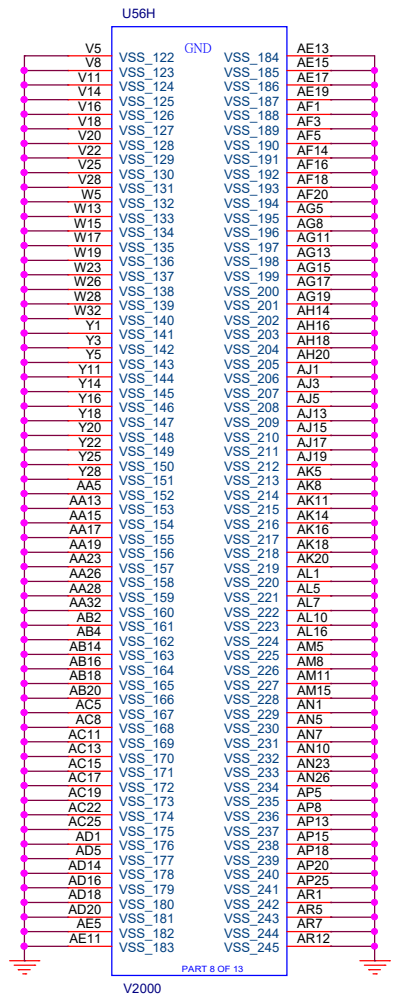
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Size A	Document Number PICO-V2K4	Rev: A0.1_0_0
Date: <i>Monday, May 03, 2021</i>		Sheet: 12 of 46



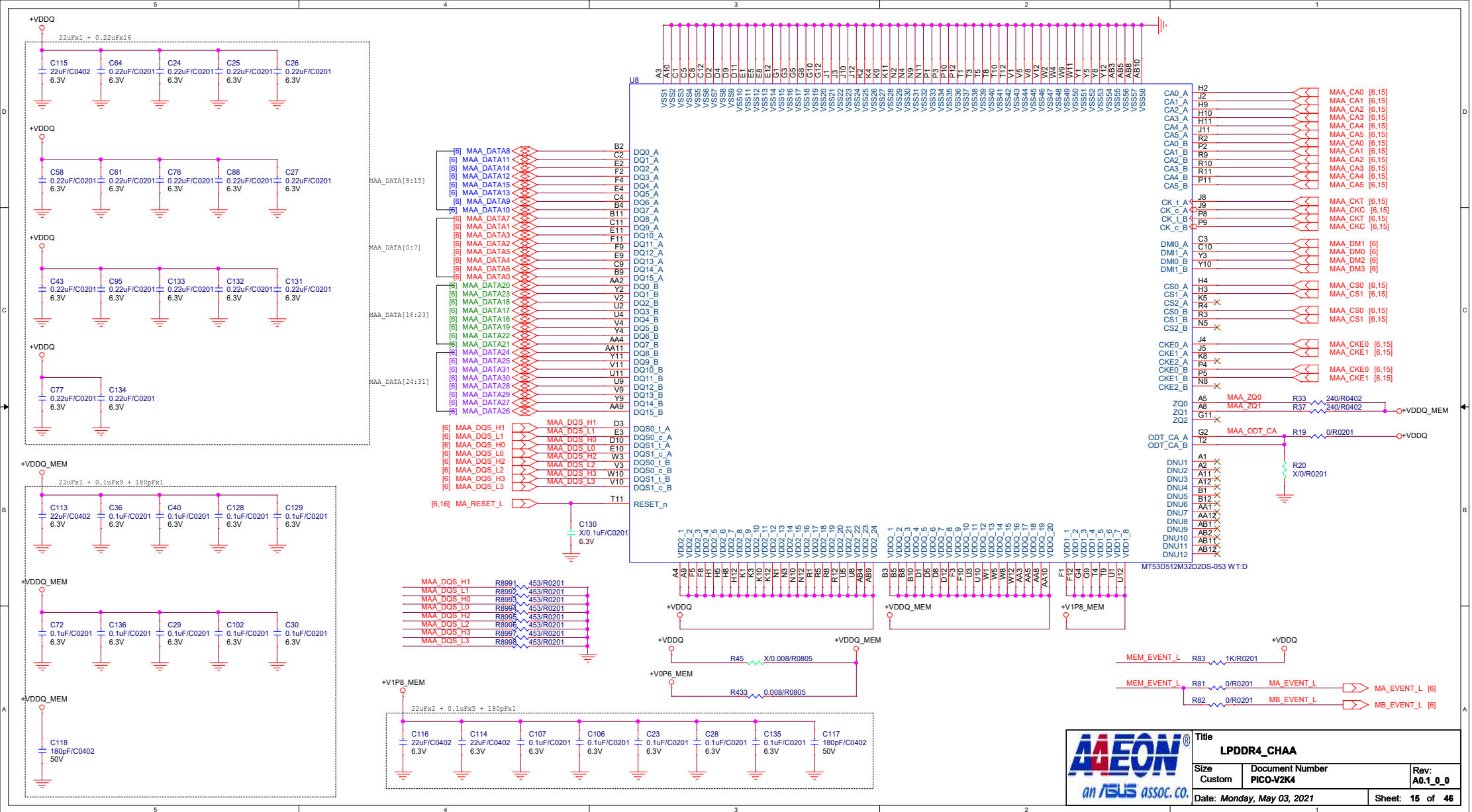
JP1(1-2)
1.27mm, 820F002-0084T-R


CMOS Control Selection(RTC_RST#)		
1-2	Save CMOS	Default
2-3	Clear CMOS	





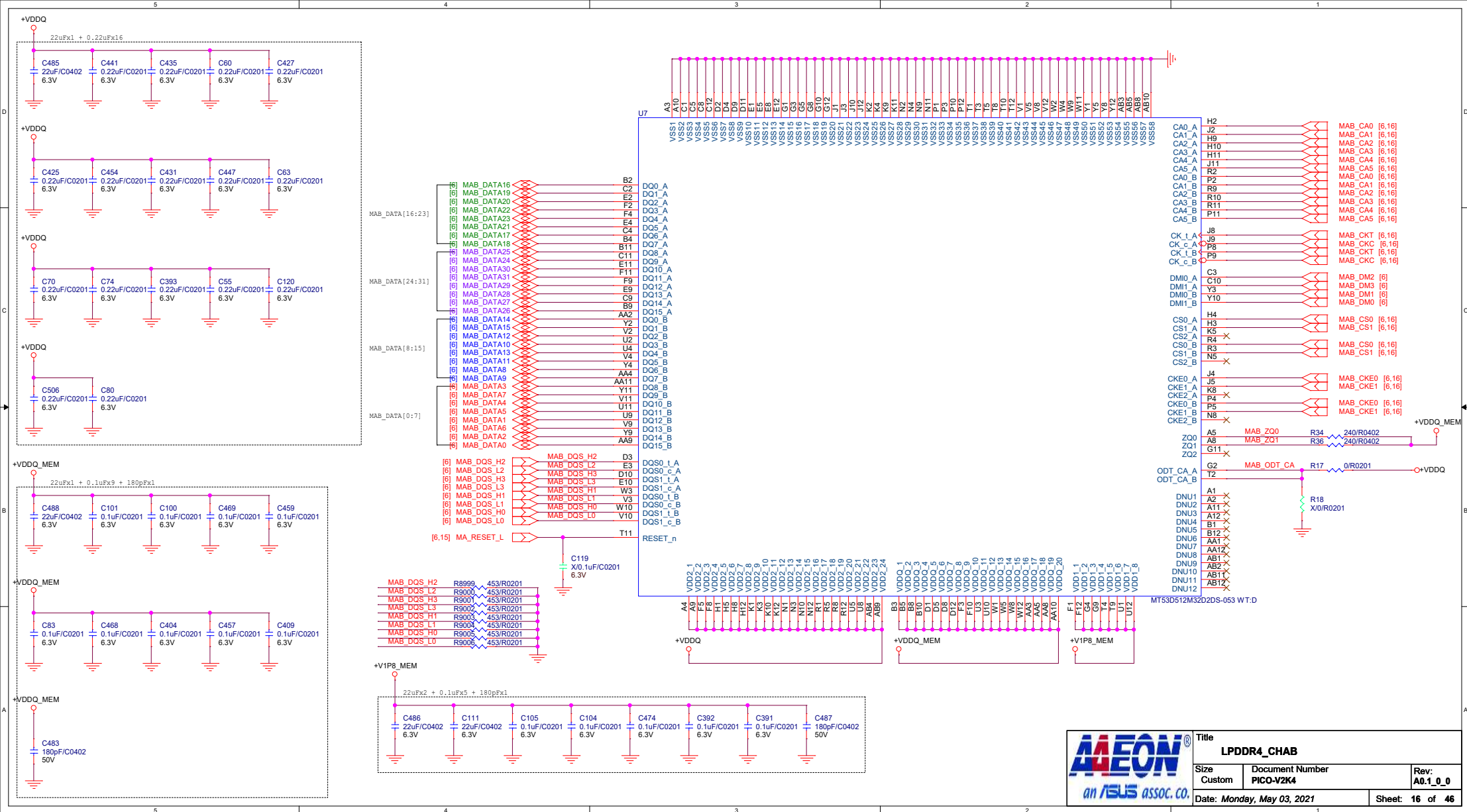
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Size B	Document Number PICO-V2K4	Rev: A0.1_0_0
Date: Monday, May 03, 2021		Sheet: 14 of 46

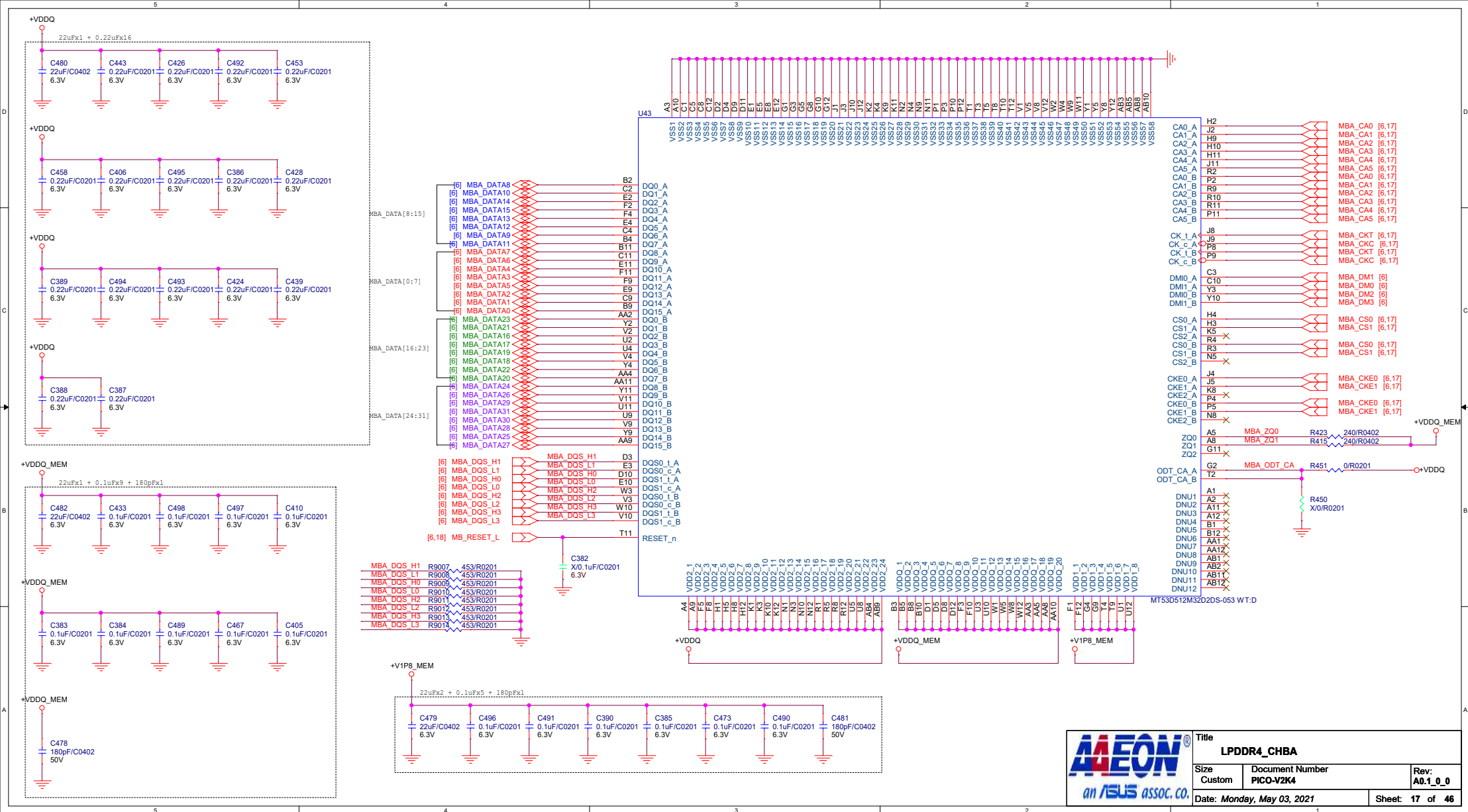


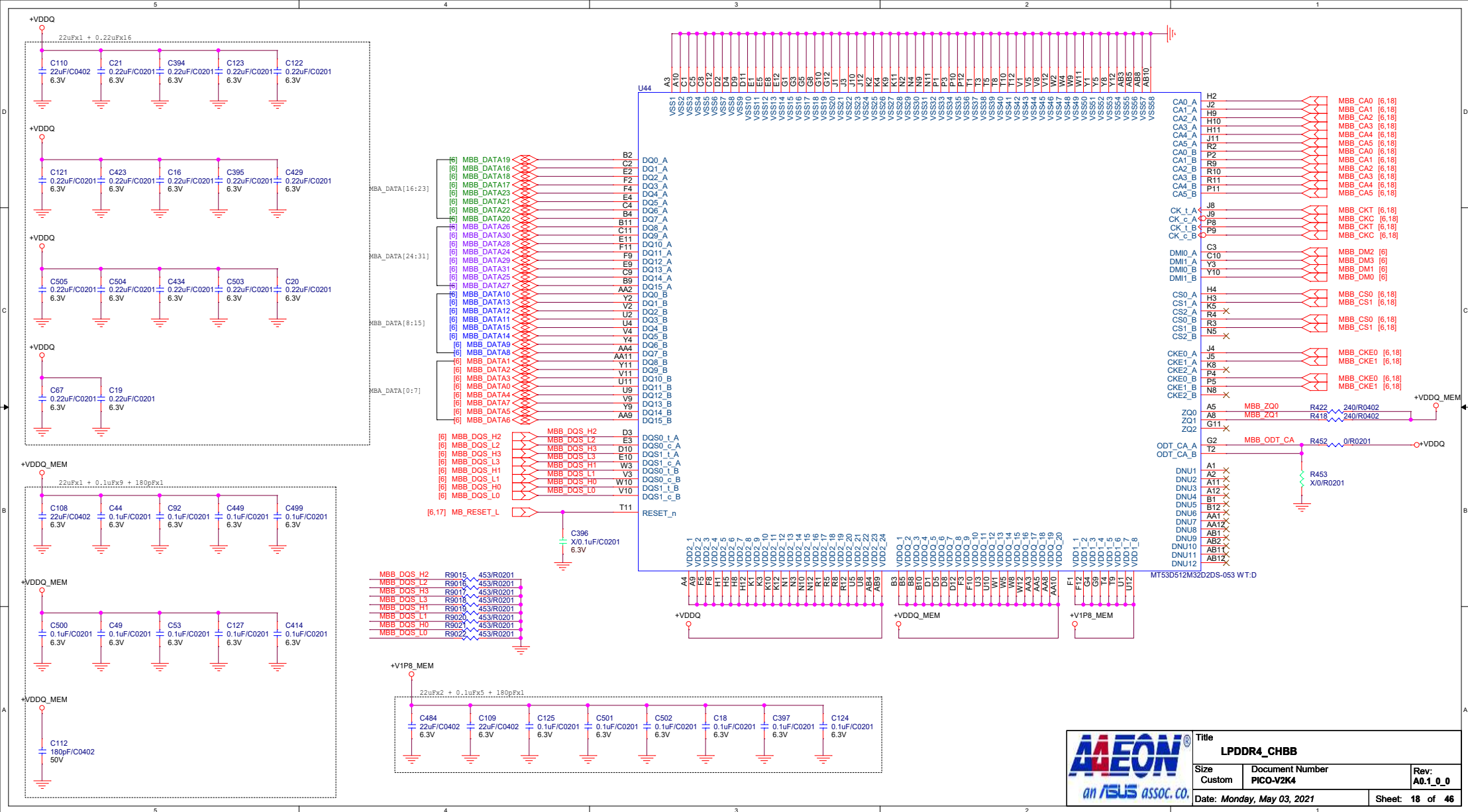


an ASUS assoc. co.

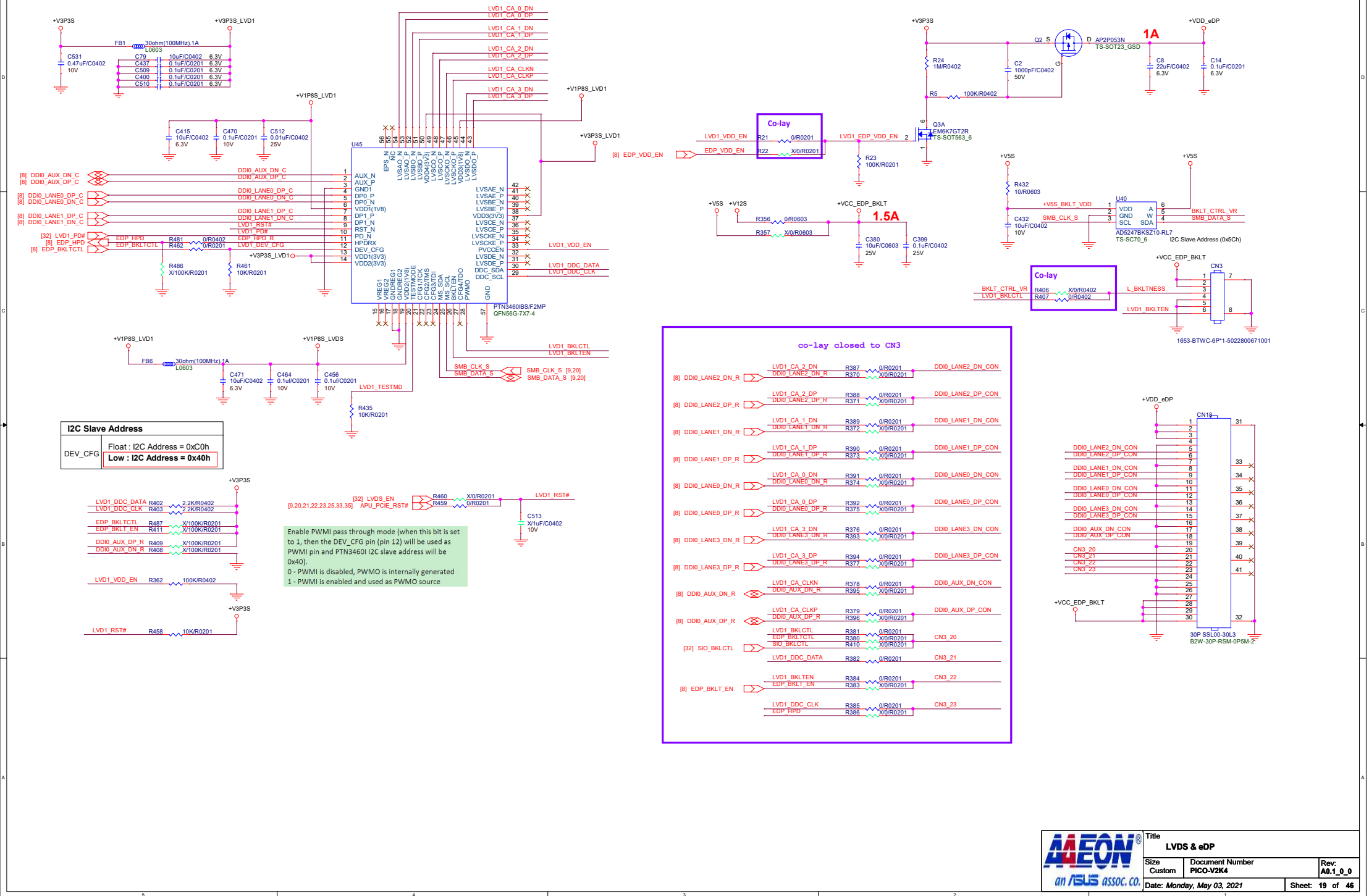
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Size Custom	Document Number PICO-V2K4	Rev: A0.1_0_0
Date: Monday, May 03, 2021		Sheet: 15 of 46



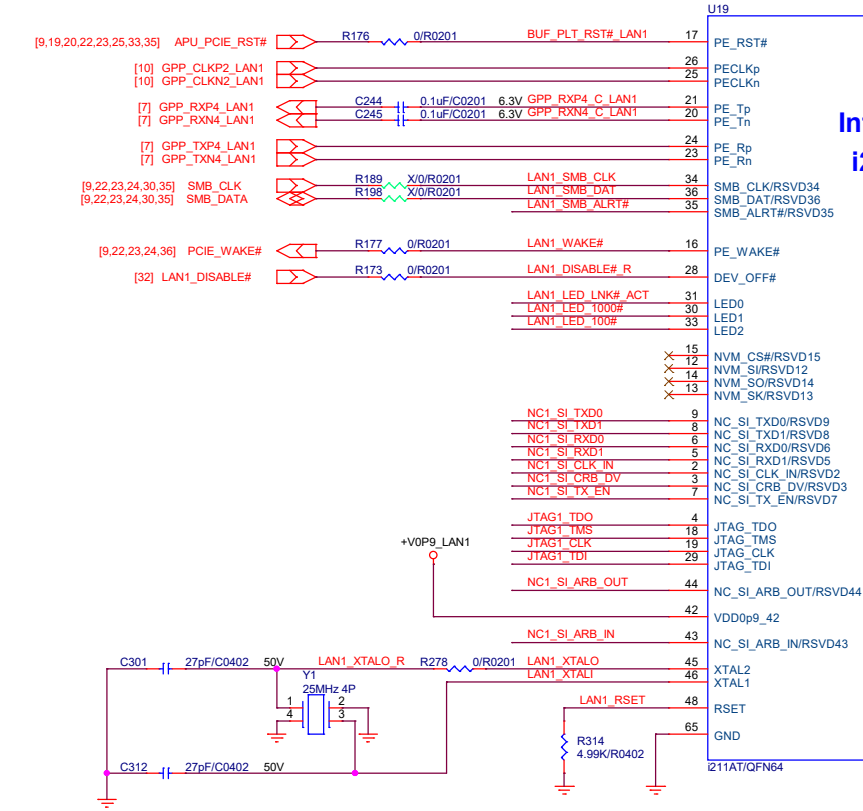




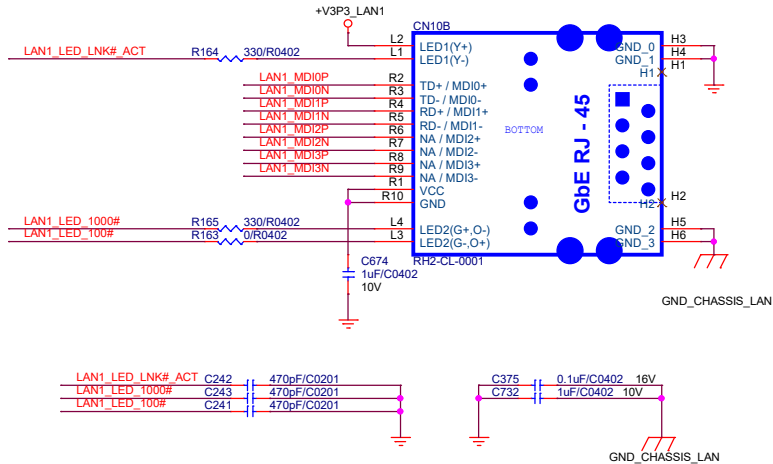
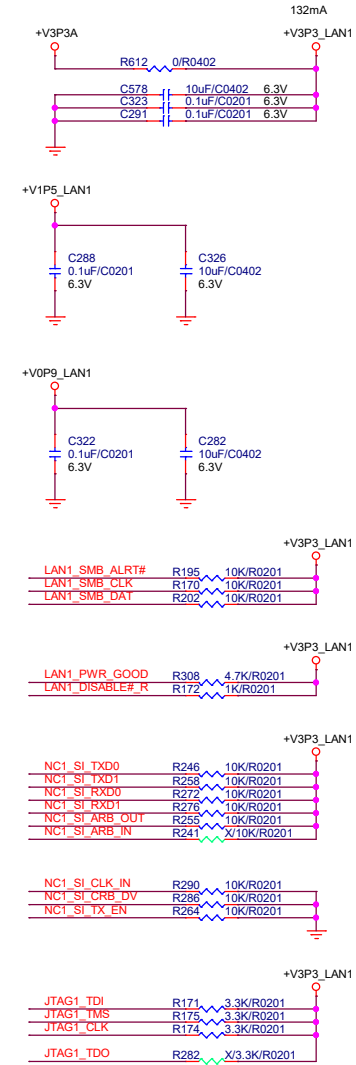
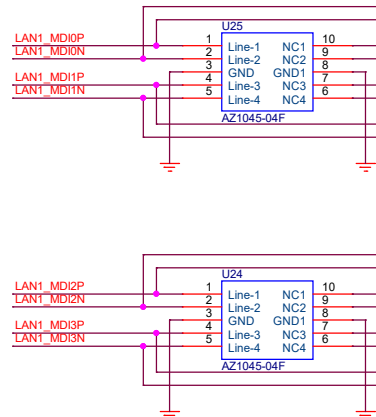
eDP/LVDS



Pearsonville(i211) /Springville(i210)



Intel GbE
i210/i211

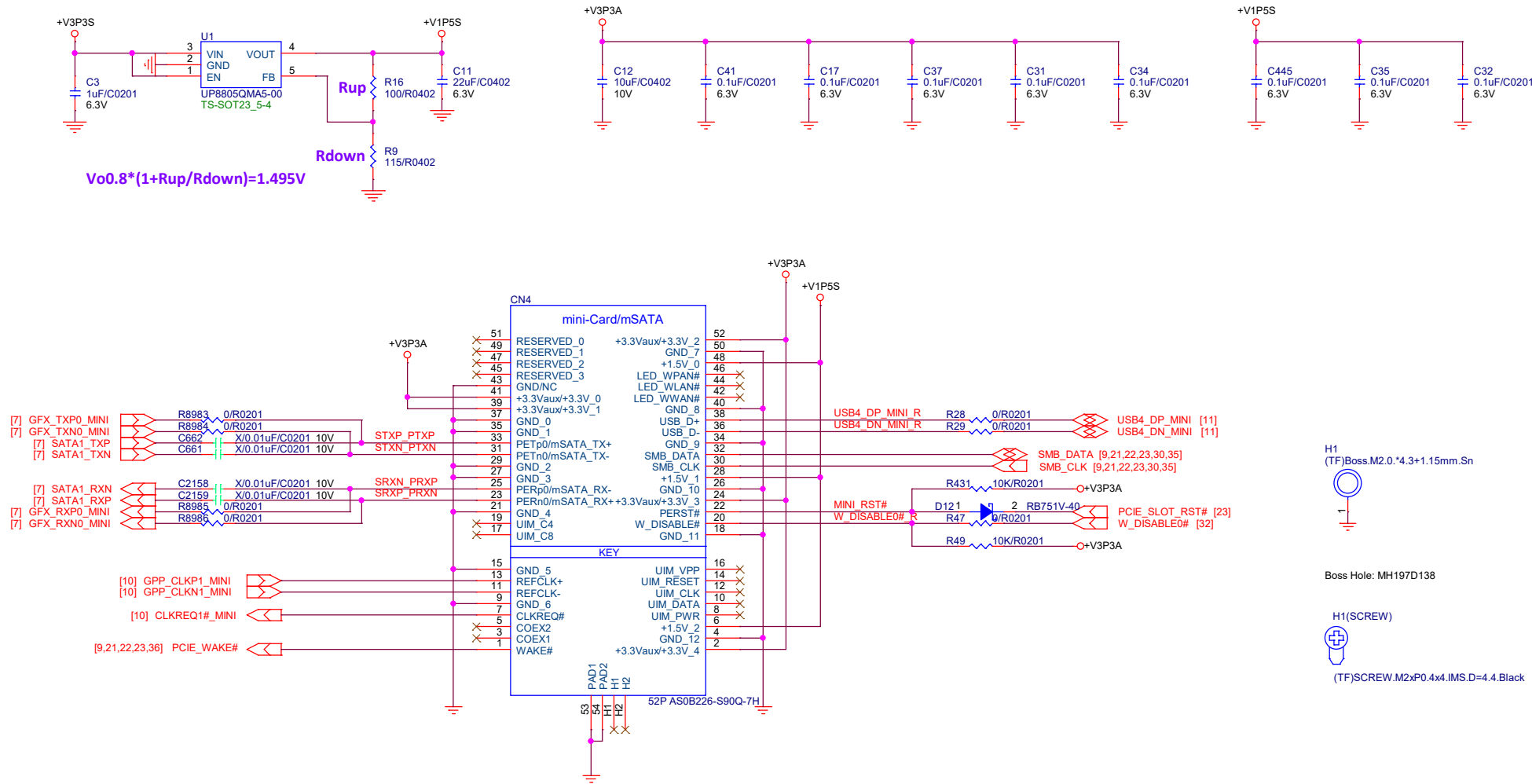


Title		LAN1_INTEL I211	
Size	Custom	Document Number	PICO-V2K4
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M.2 Key M



Title M2_Key M		
Size Custom	Document Number PICO-V2K4	Rev: A0.1_0_0
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H1
(TF)Boss.M2.0.*4.3+1.15mm.Sn

Boss Hole: MH197D138

H1(SCREW)

(TF)SCREW.M2xP0.4x4.1MS.D=4.4.Black



Title MINI_CARD		
Size B	Document Number PICO-V2K4	Rev: A0.1_0_0
Date: Monday, May 03, 2021		Sheet: 24 of 46

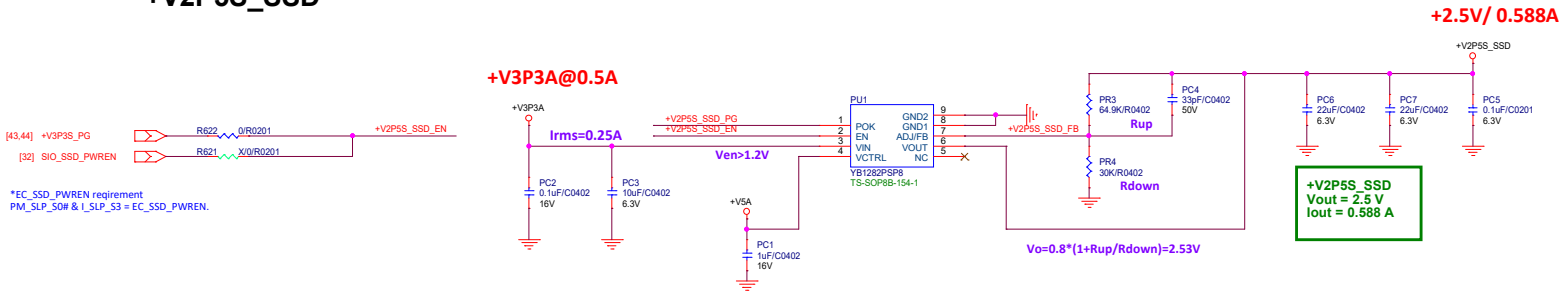
+V2P5S_SSD



PCIe SSD 3* PWR supply

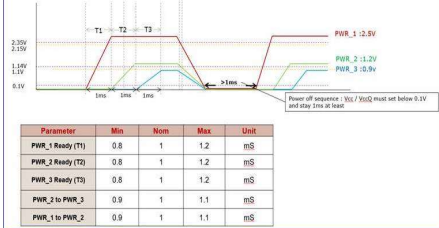
20200929 Run out of PCB space for DDR4 Memory down
Change design from DDR4 to LPDDR4x
Modify +V2P5S_SSD/+V1P2S_SSD for PU25/PU26

+V2P5S_SSD

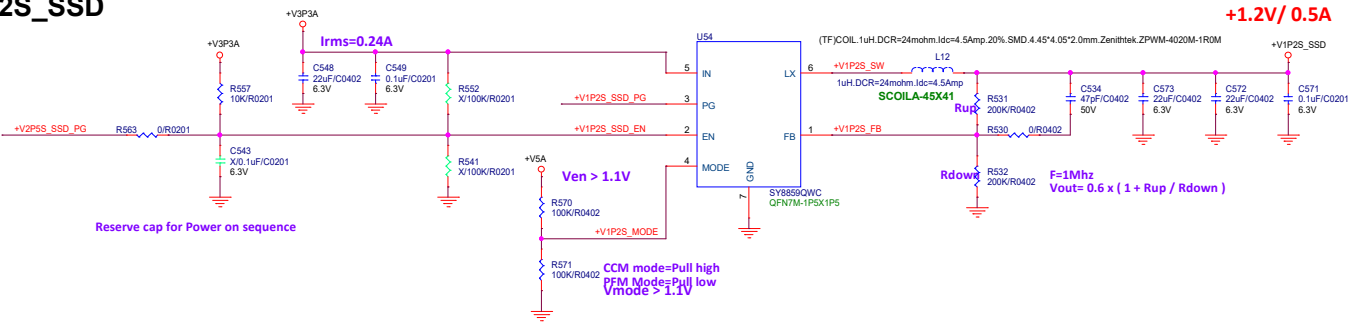


1. Power domain:

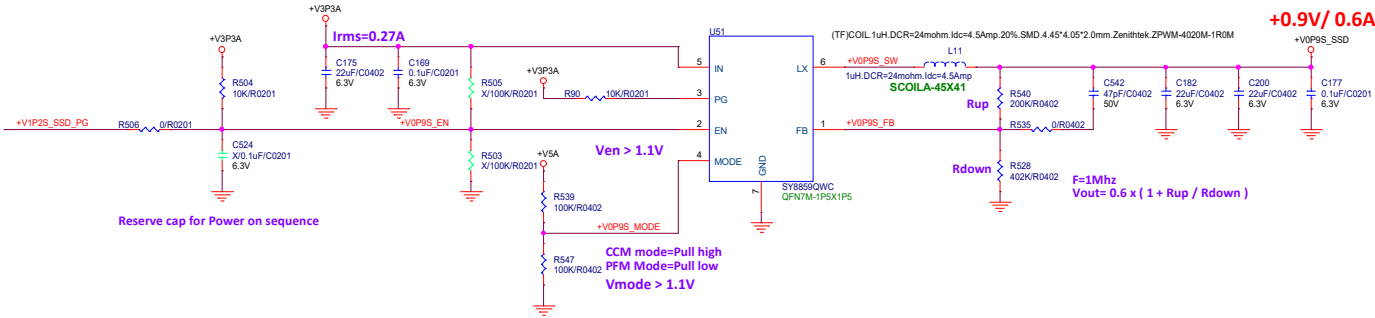
1.4 Power on sequence timing parameter



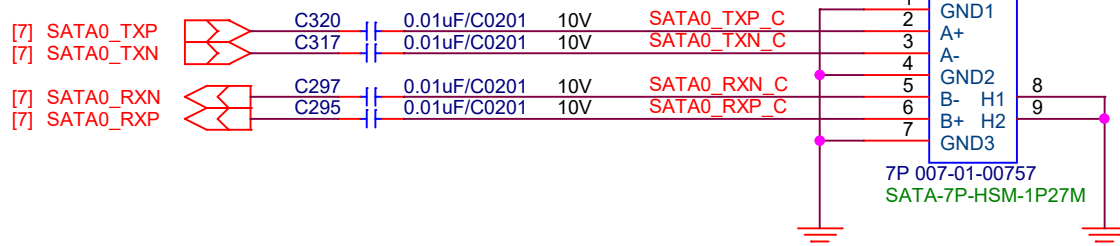
+V1P2S_SSD



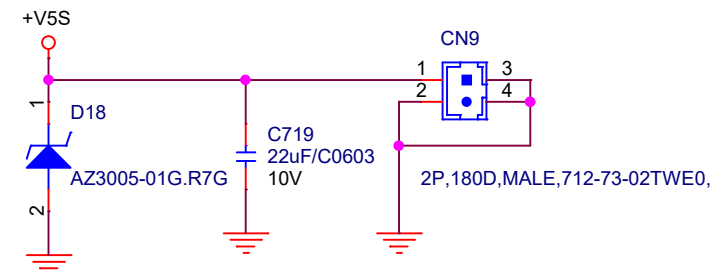
+V0P9S_SSD



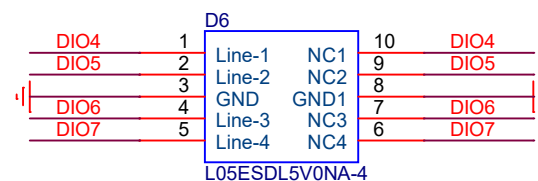
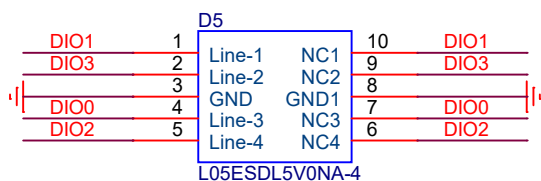
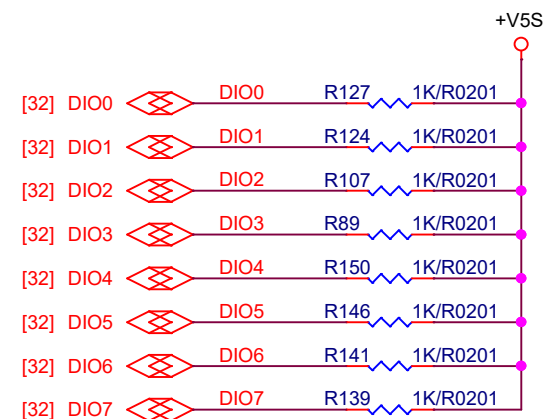
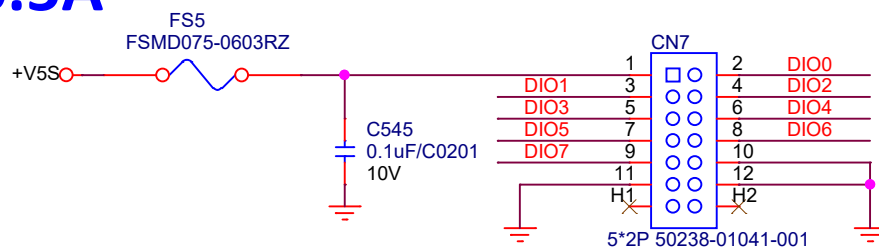
SATA



1A

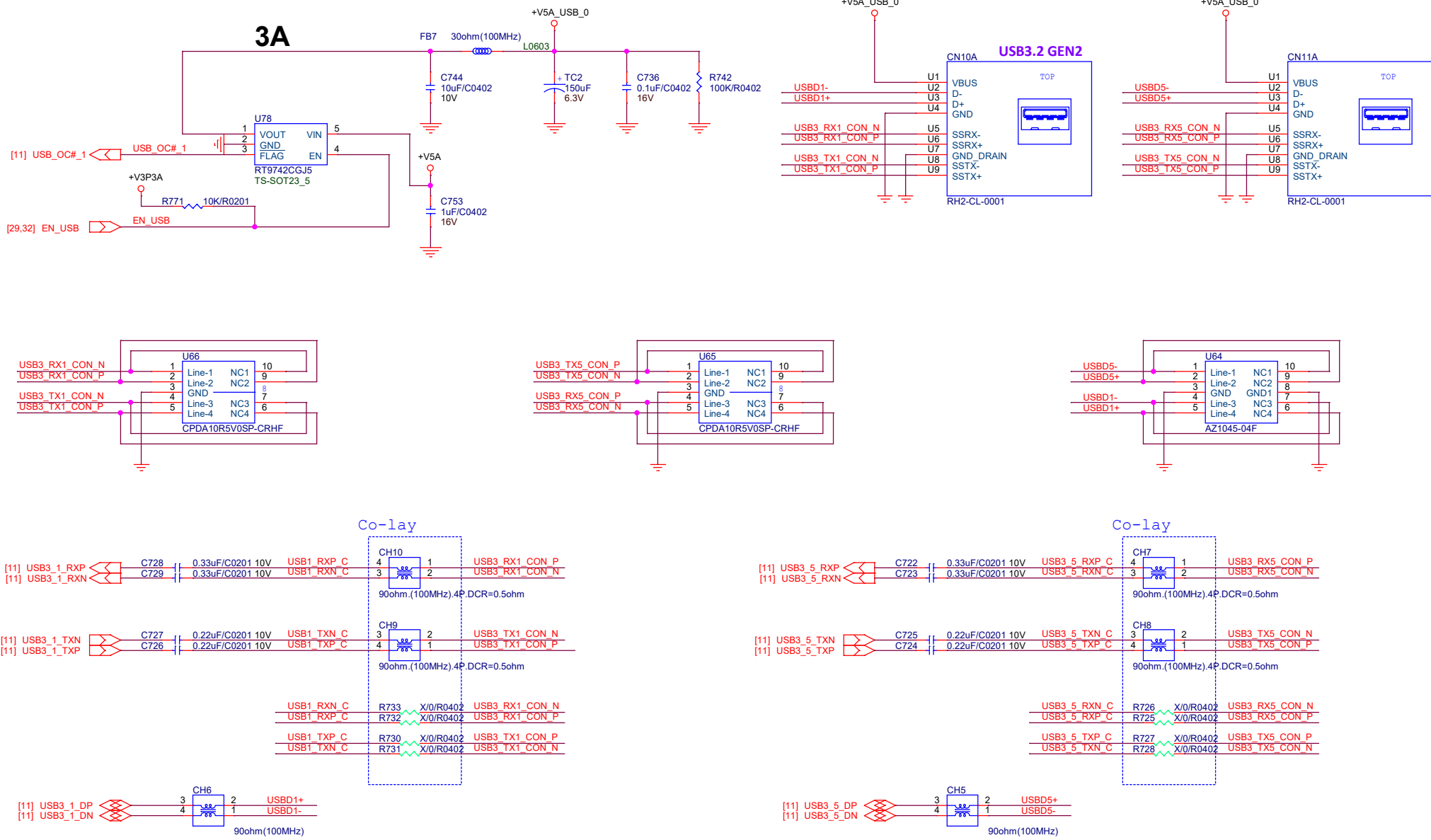


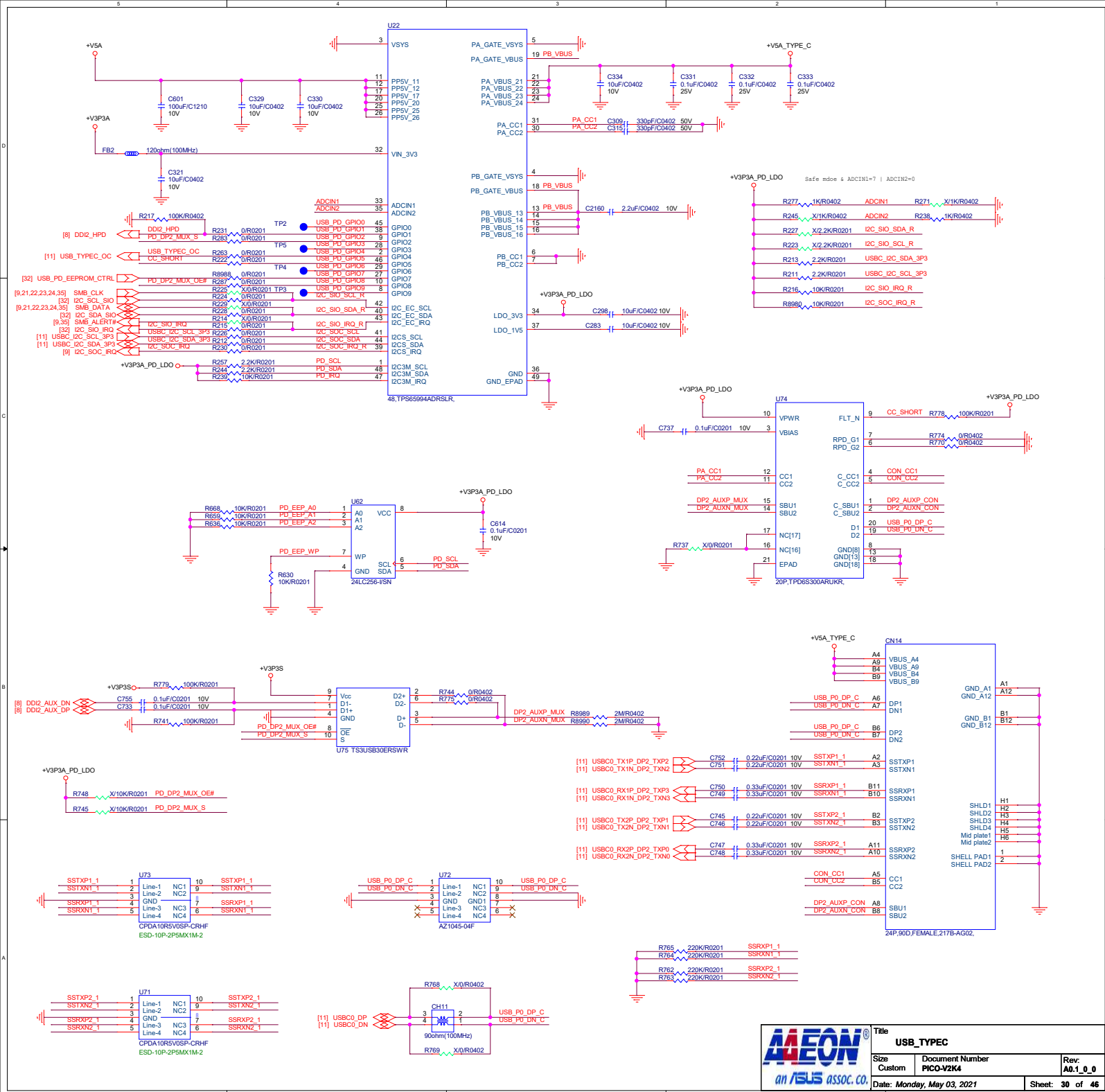
0.5A



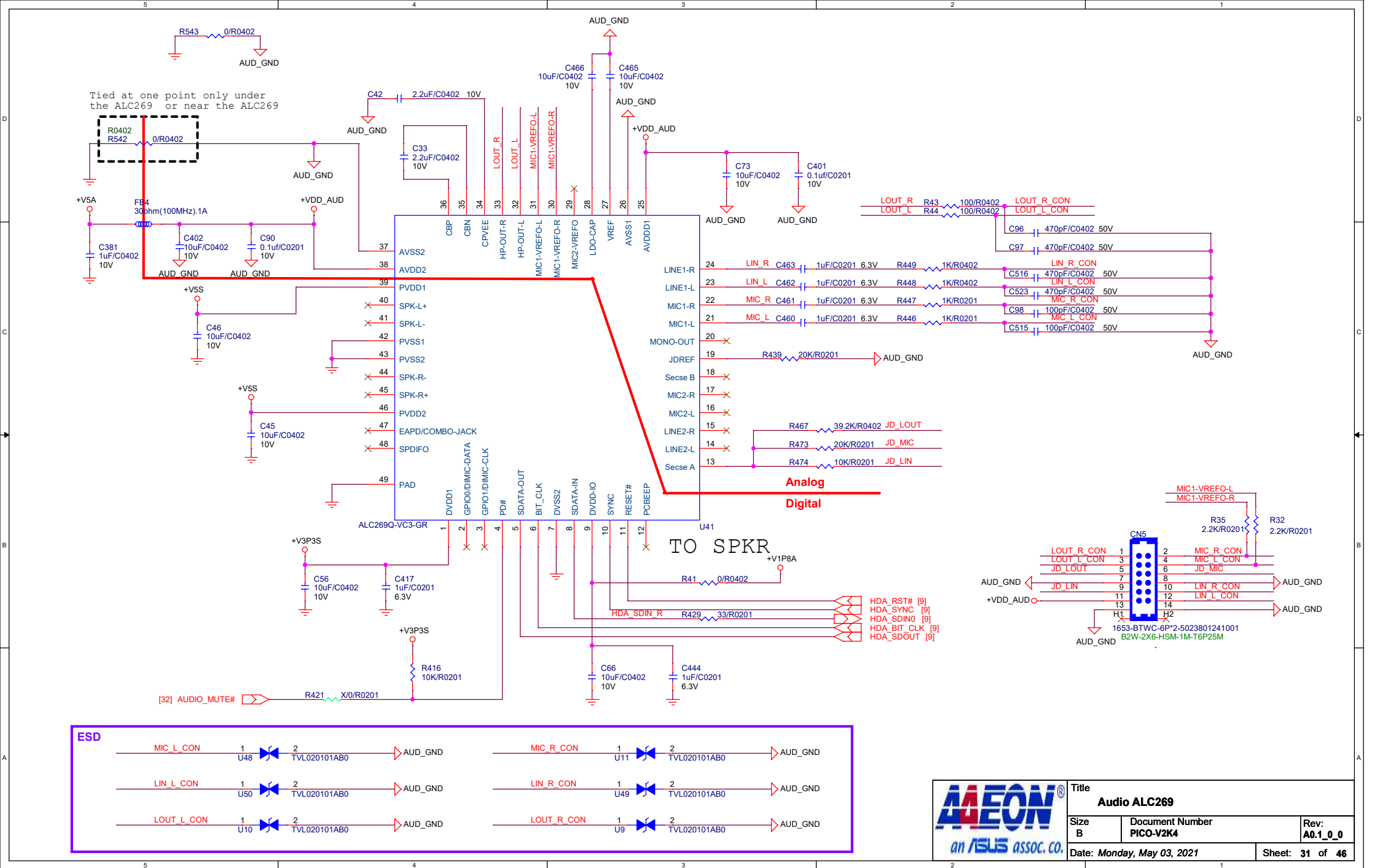
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Size A	Document Number PICO-V2K4	Rev: A0.1_0_0
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USB3.2 Gen2 x 2

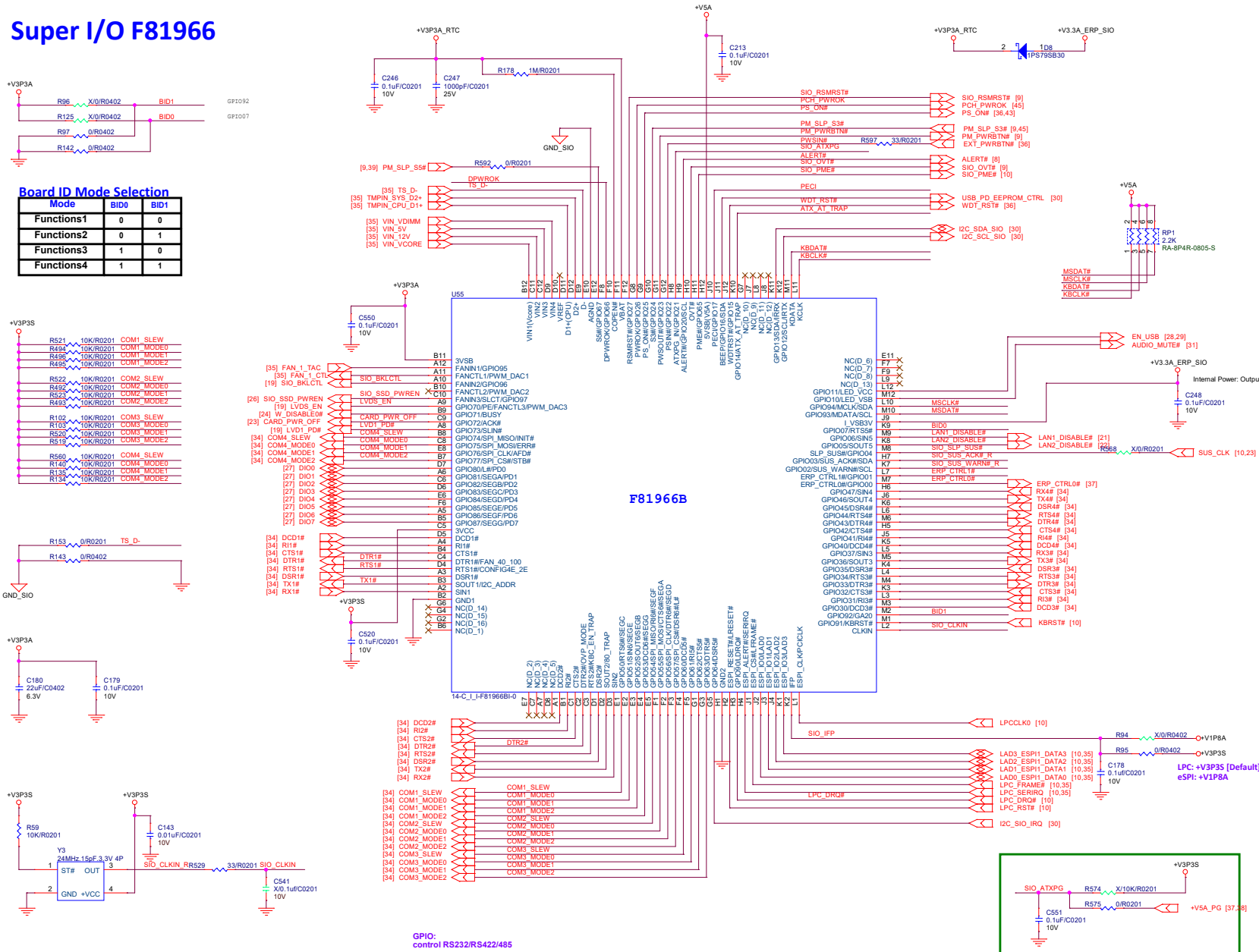




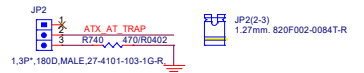
Title		
USB_TYPEC		
Size	Document Number	Rev.
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Super I/O F81966

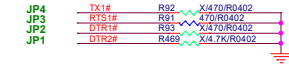


ATX/AT Control Select

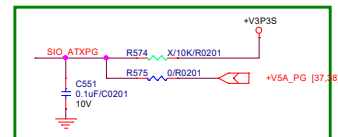
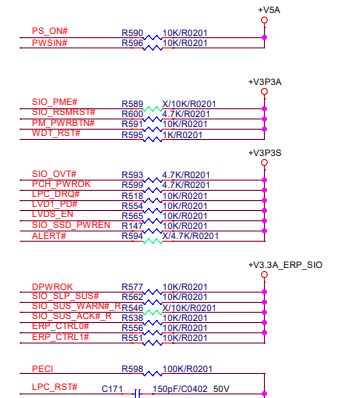


PIN69	ATX_AT_TRAP	
HIGH	ATX mode (internal pull high 47Kohm)	
LOW	AT mode	Default

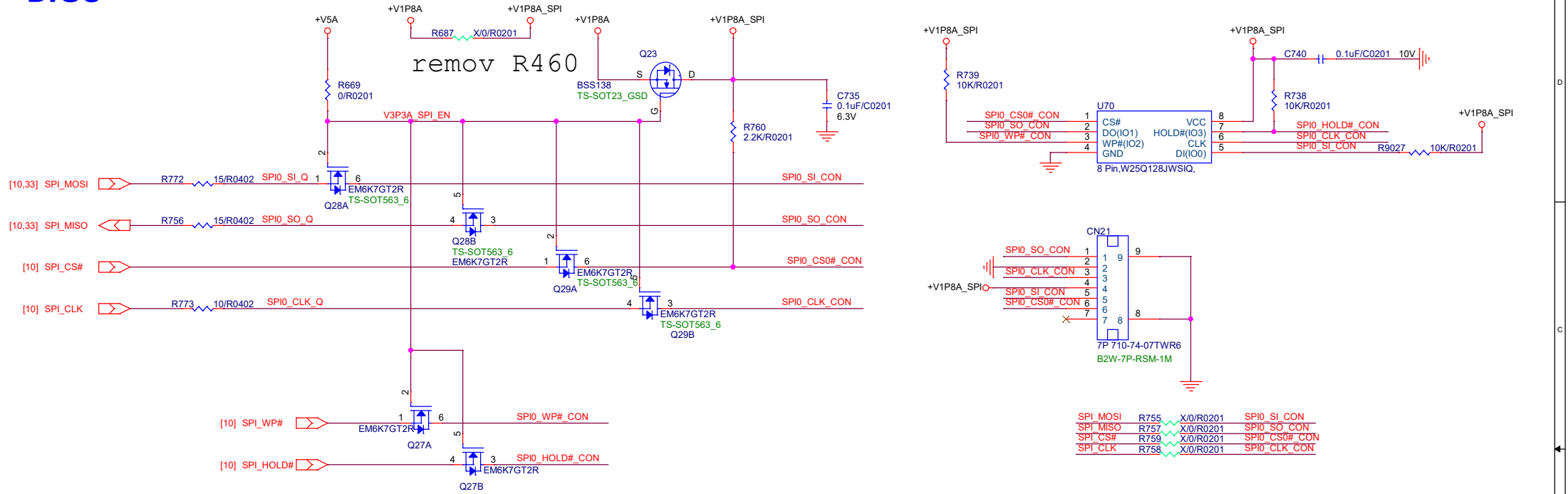
Power On Strapping Options pin



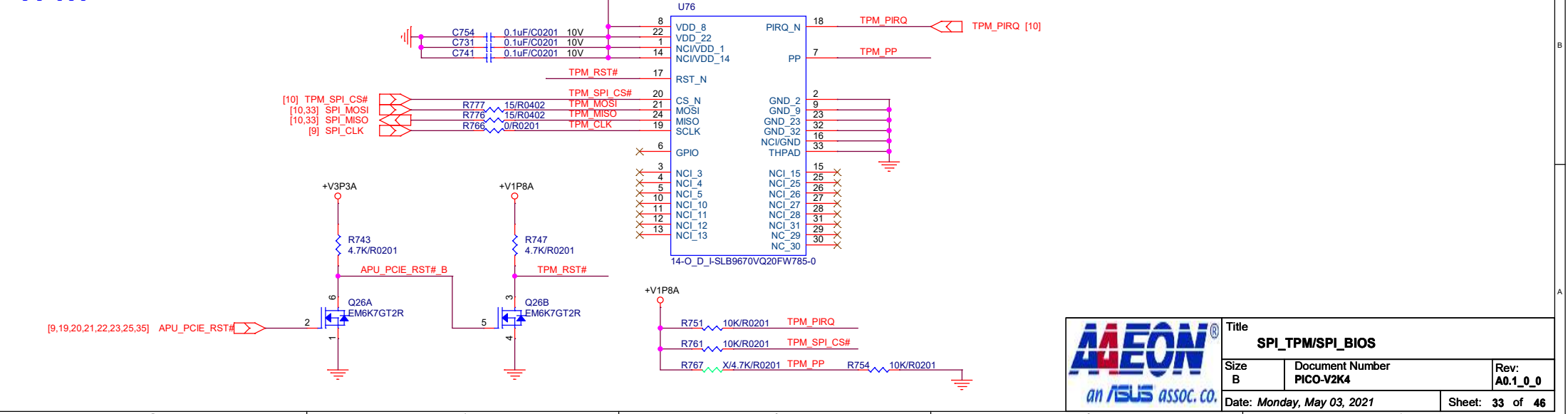
JP4, B3	I2C_ADDR
HIGH	The I2C slave address is 7h2E. (Default)
LOW	The I2C slave address is 7h2D.
JP3, D4	Config4E_2E
HIGH	Configuration Register I/O port is 4E/4F.
LOW	Configuration Register I/O port is 2E/2F(Default).
JP2, C4	FAN40_100
HIGH	Power on fan speed default duty is 40% (Default)
LOW	Power on fan speed default duty is 100%
JP1, C2	OVP_Mode
HIGH	(ALARM mode) Disable OVP function
LOW	(FORCE mode) Enable OVP function




BIOS



TPM

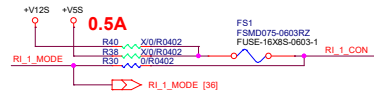
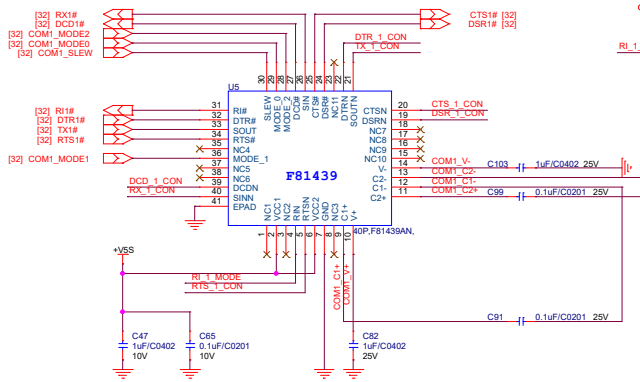




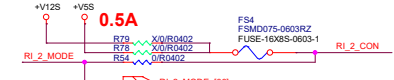
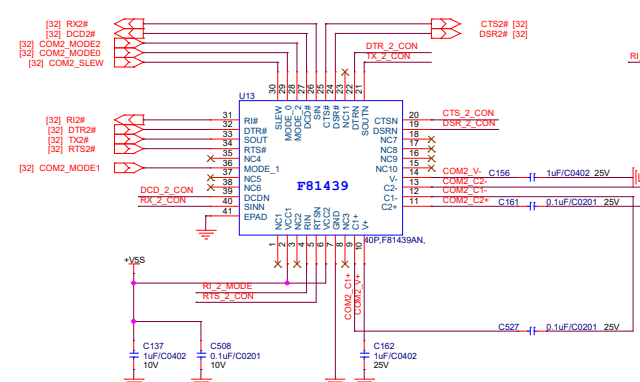
an /EUS/ assoc. co.

Title SPI_TPM/SPI_BIOS		
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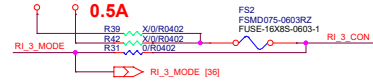
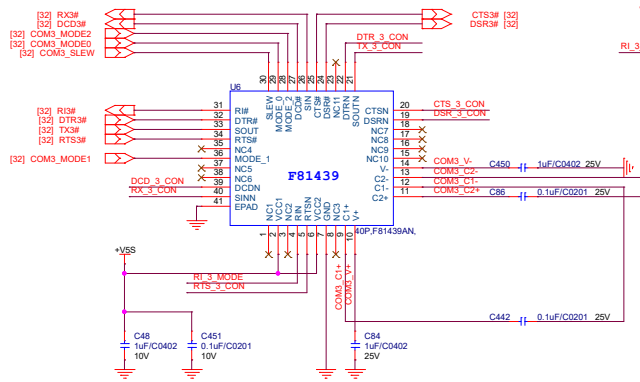
COM1-RS232/RS422/RS485



COM2-RS232/RS422/RS485



COM3-RS232/RS422/RS485



COM4-RS232/RS422/RS485

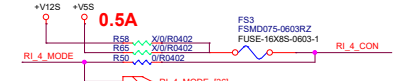
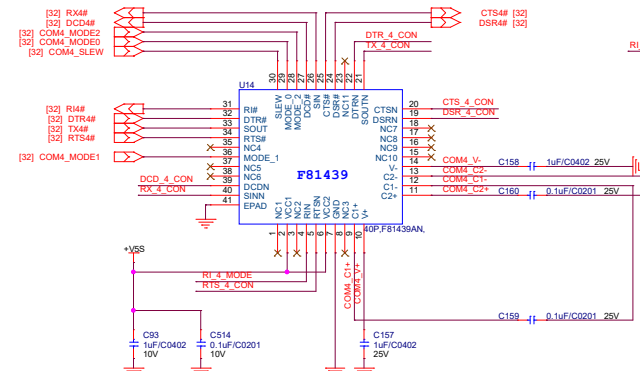
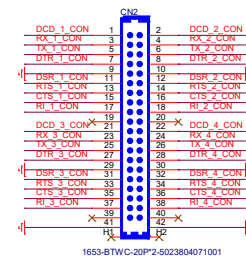


TABLE 1: Mode Select Configuration for F81439

Pin 29 MODE_0	Pin 36 MODE_1	Pin 28 MODE_2	Mode	Status
0	0	0	RS-422 Full Duplex	1T/1R RS-422
0	0	1	Pure RS-232	3T/5R RS-232
0	1	0	RS-485 Half Duplex	1T/1R RS-485, TX ENABLE Low Active
0	1	1	RS-485 Half Duplex	1T/1R RS-485, TX ENABLE High Active
1	0	0	RS-422 Full Duplex	1T/1R RS-422 with termination resistor
1	0	1	Pure RS-232	1T/1R RS-232 co-exists with RS485 application without the need for the bus switch IC (for special usage).
1	1	0	RS-485 Half Duplex	1T/1R RS-485 with termination resistor TX ENABLE Low Active
1	1	1	Low Power Shutdown	All I/O pins are High Impedance



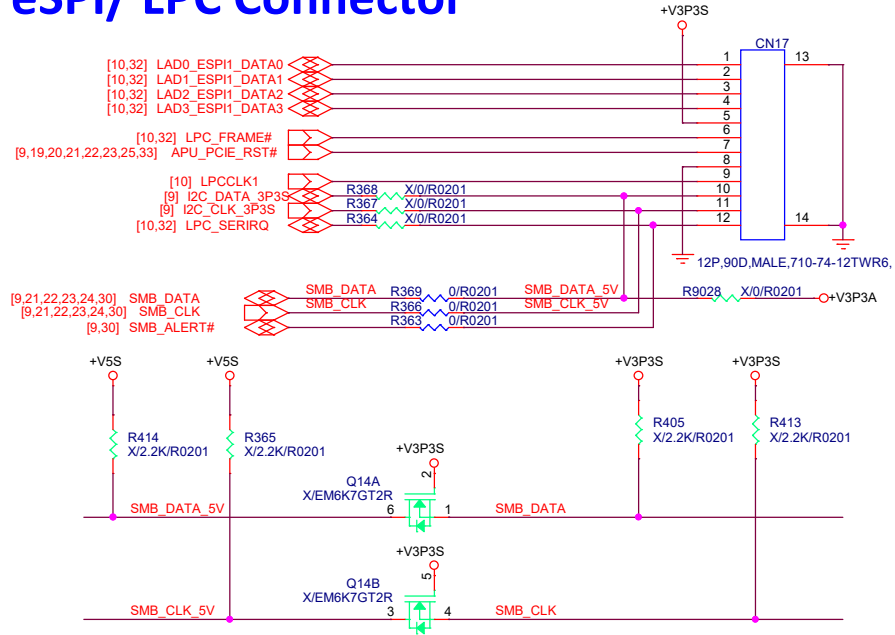
Pin Mapping	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

Maximum Slew rate control			
SLEW	RS-232	RS-485/RS-422	
0	1Mbps	10Mbps	
1	250Kbps	250Kbps	

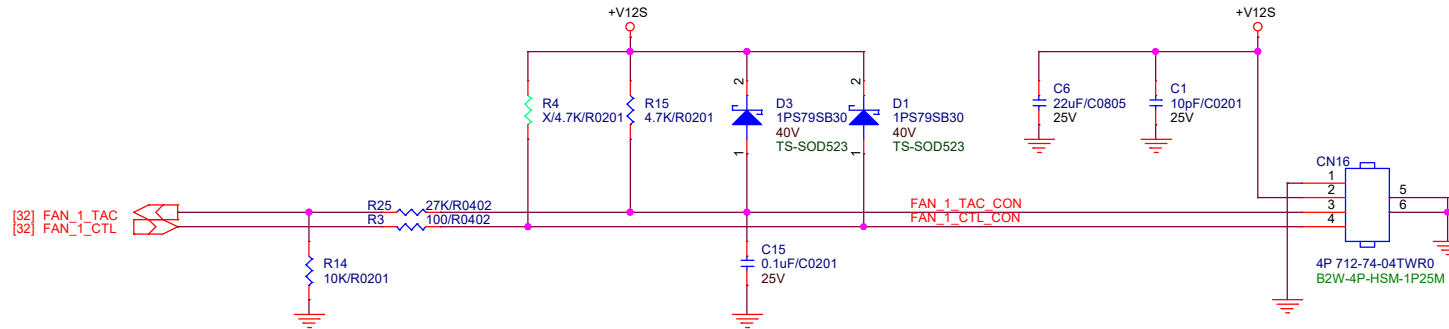


Title COM_PORT		
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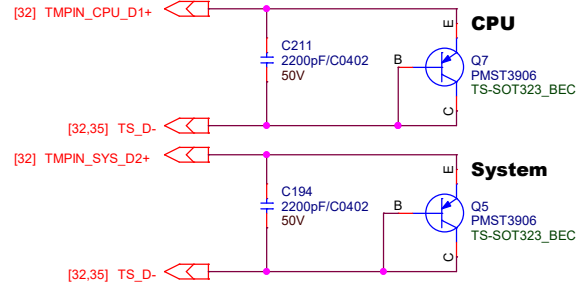
eSPI/ LPC Connector



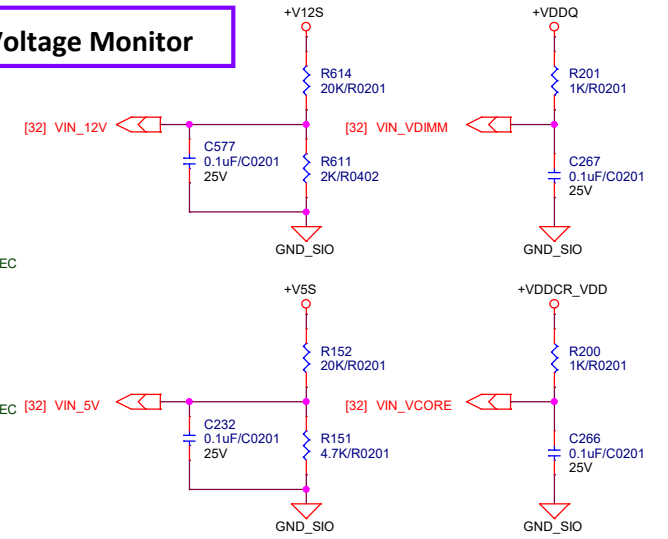
CPU FAN



Temperature Monitor

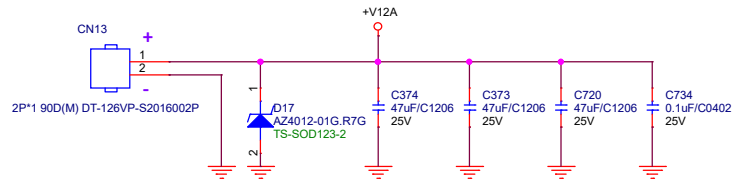


Voltage Monitor

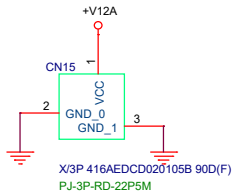


Title FAN/ LPC/ HW Monitor		
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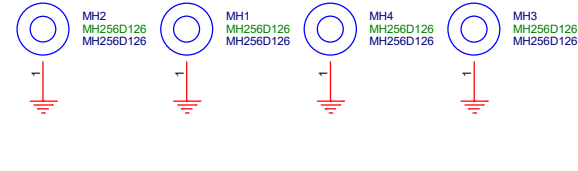
Power Input



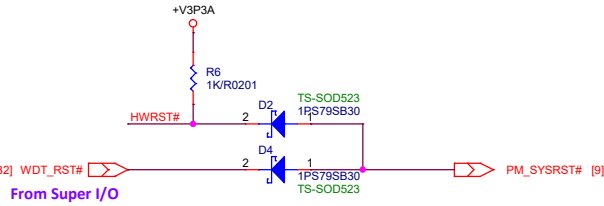
DC Jack



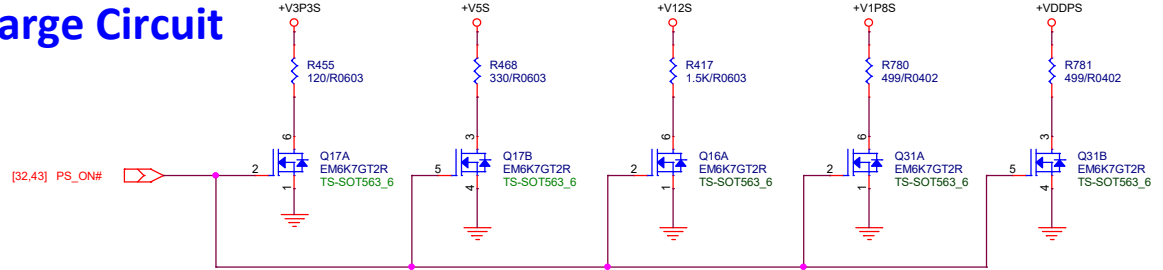
Mounting Holes / Non-PTH



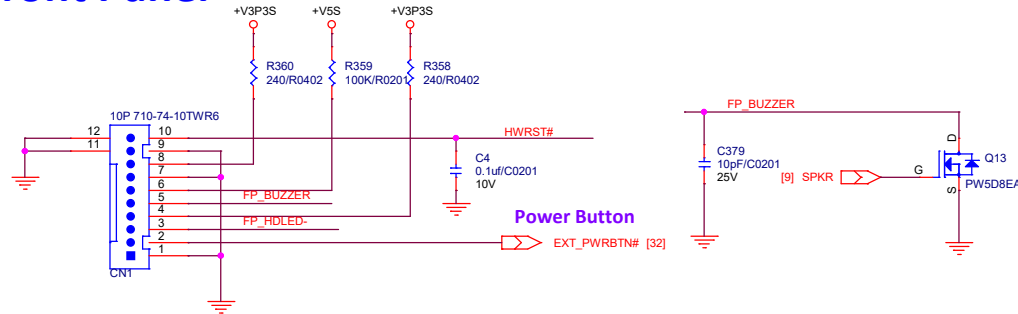
System Reset



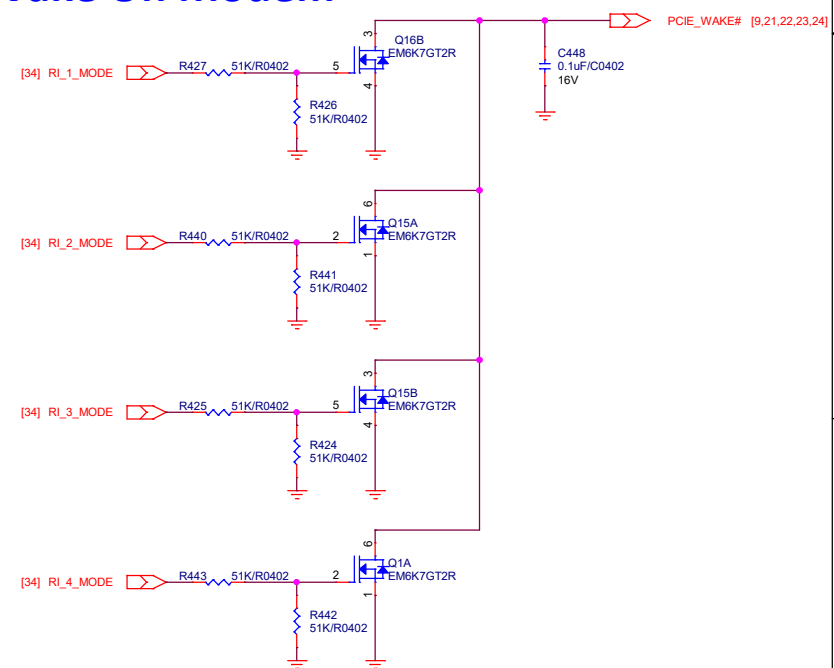
Discharge Circuit



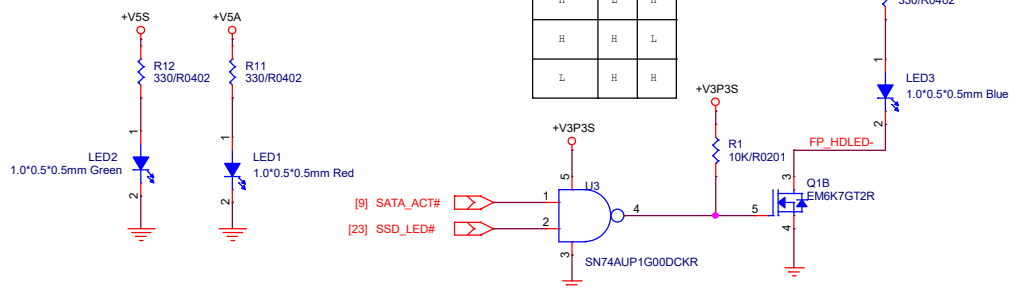
Front Panel



Wake On Modem

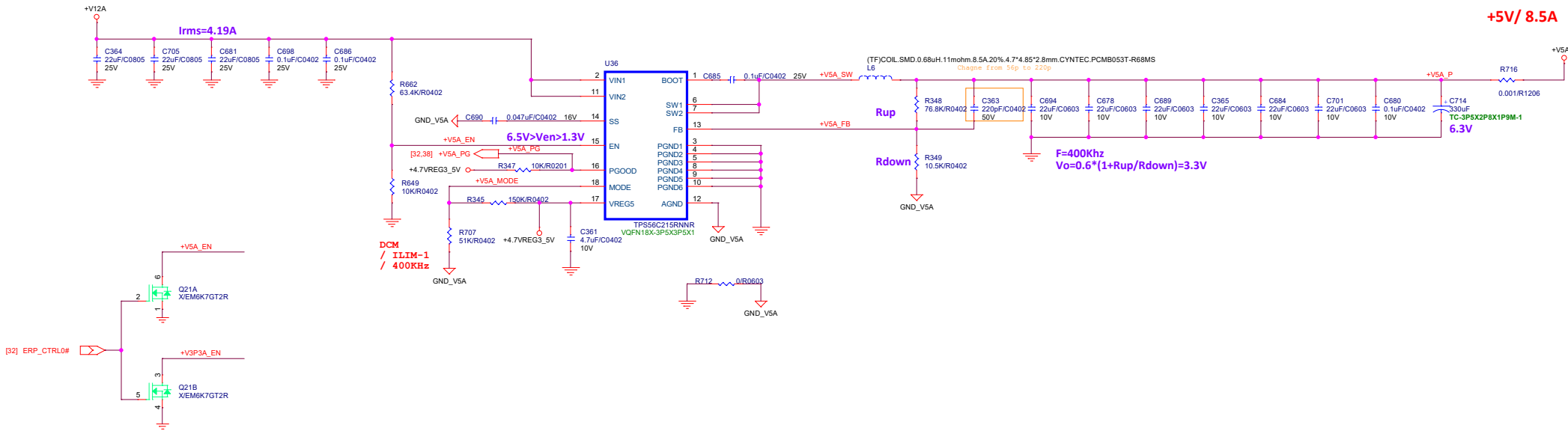


LED

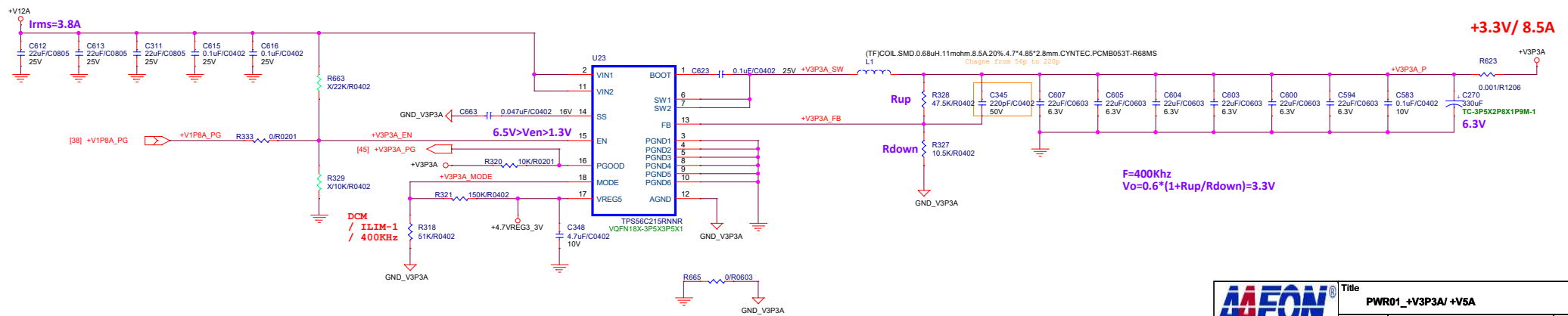



Title		
Power IN/ Front Panel/ MISC		
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+V5A

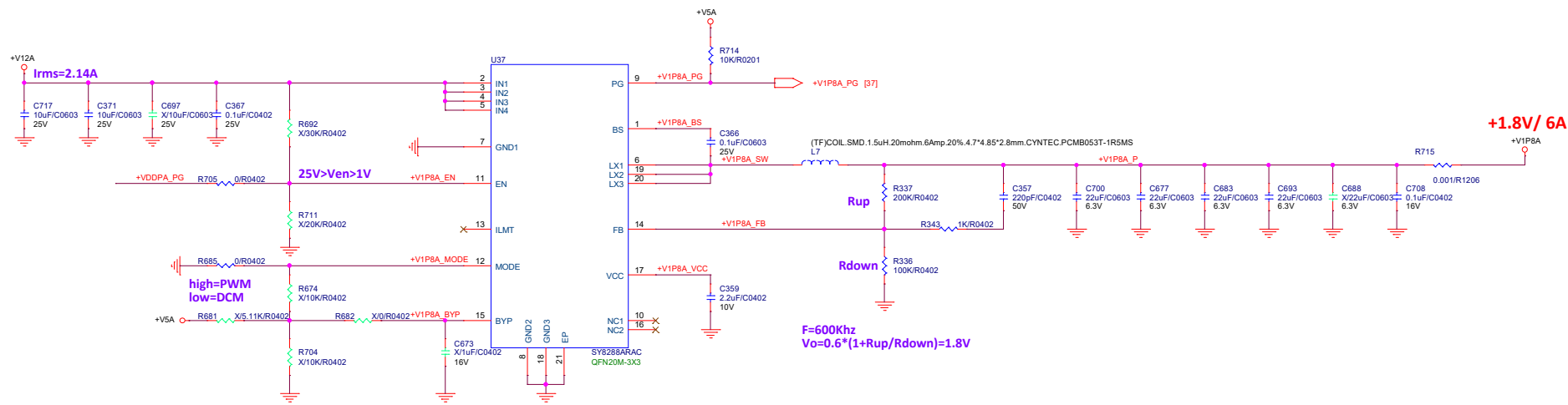


+V3P3A

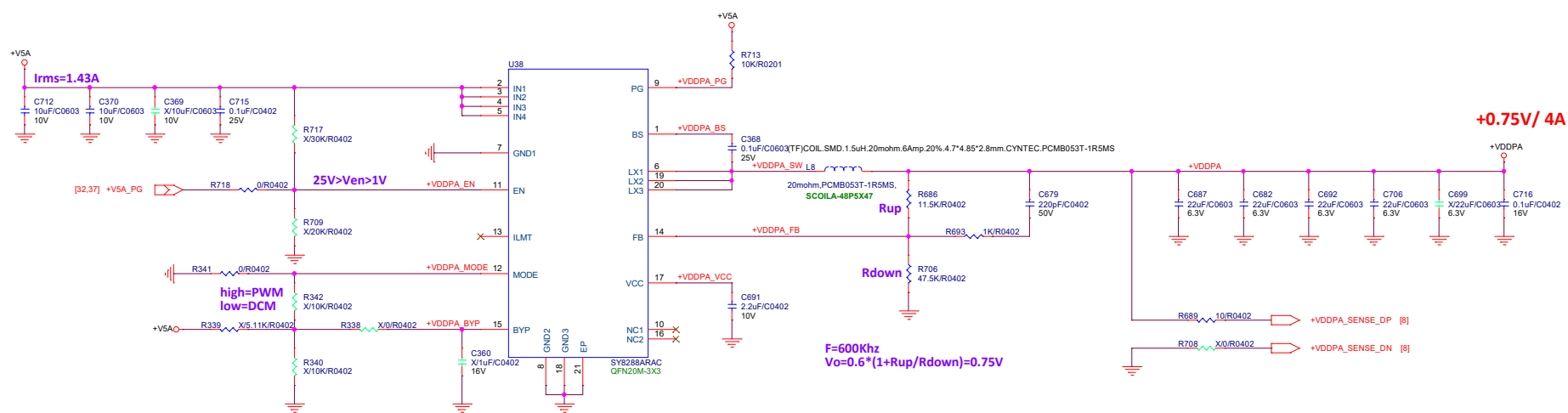


	Title PWR01_V3P3A/ +V5A		
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+V1P8A

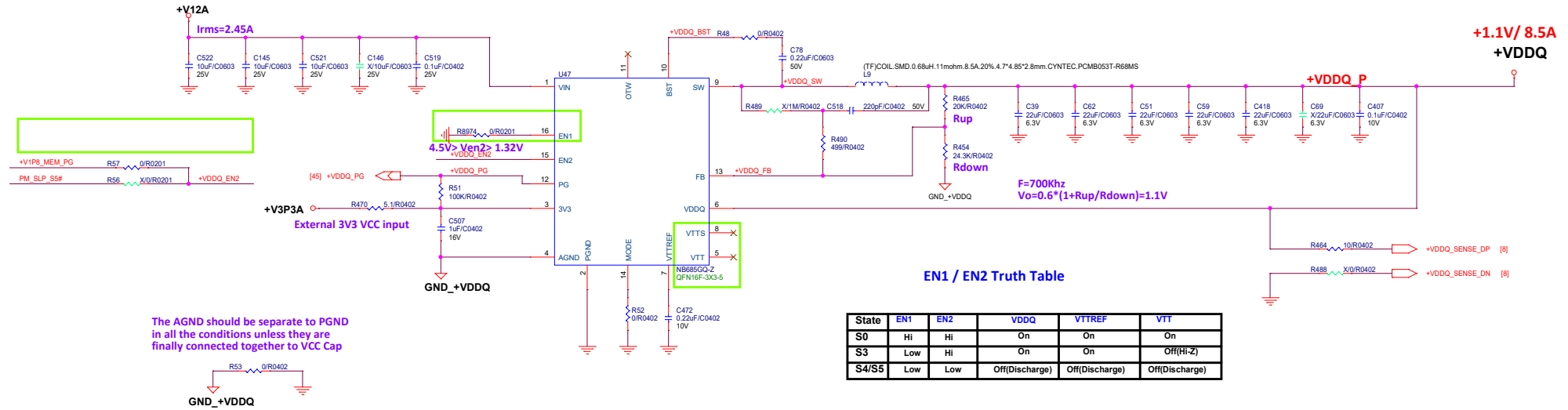


+VDDPA

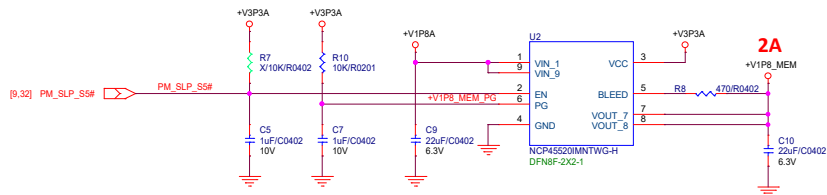


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PWR02_+V1P8A/ +VDDPA(0.75V)		
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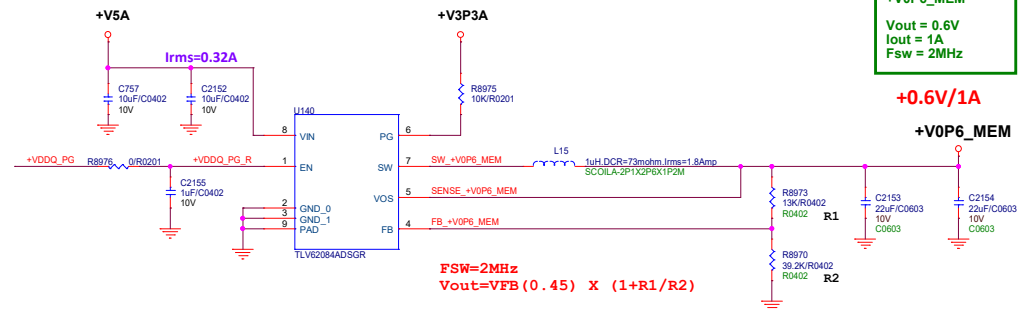
+VDDQ

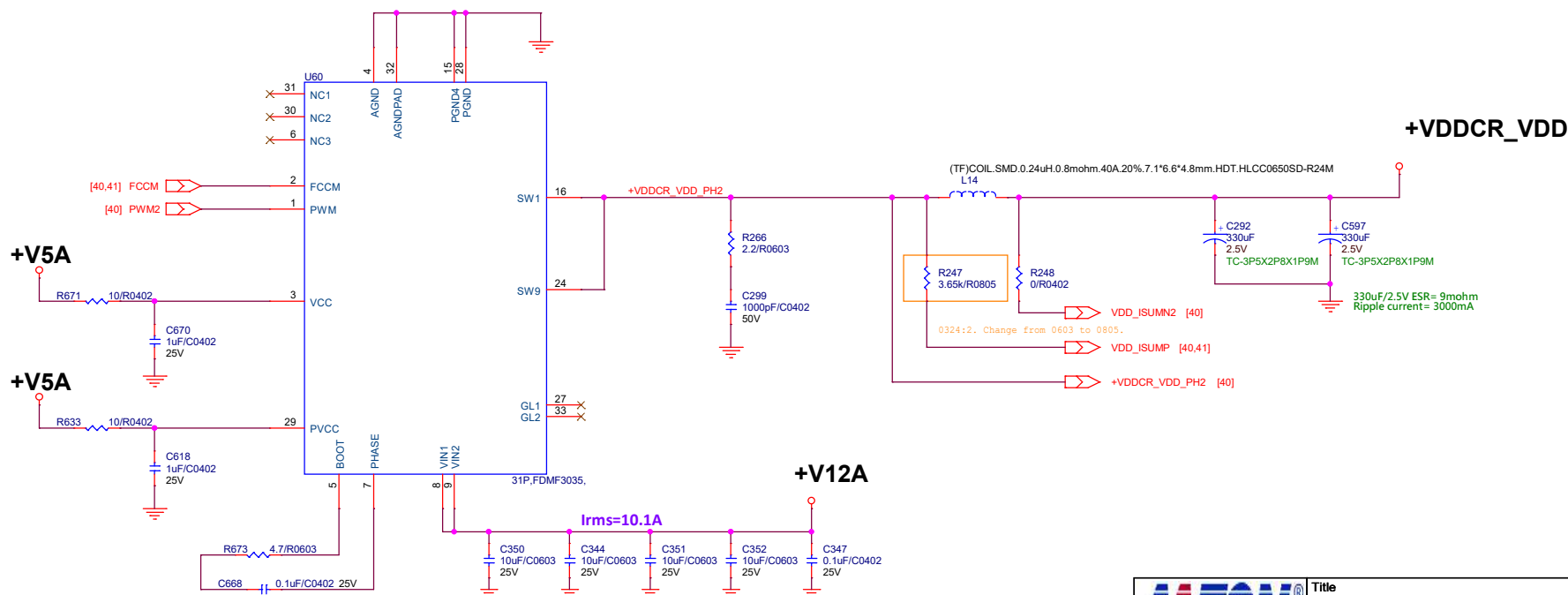
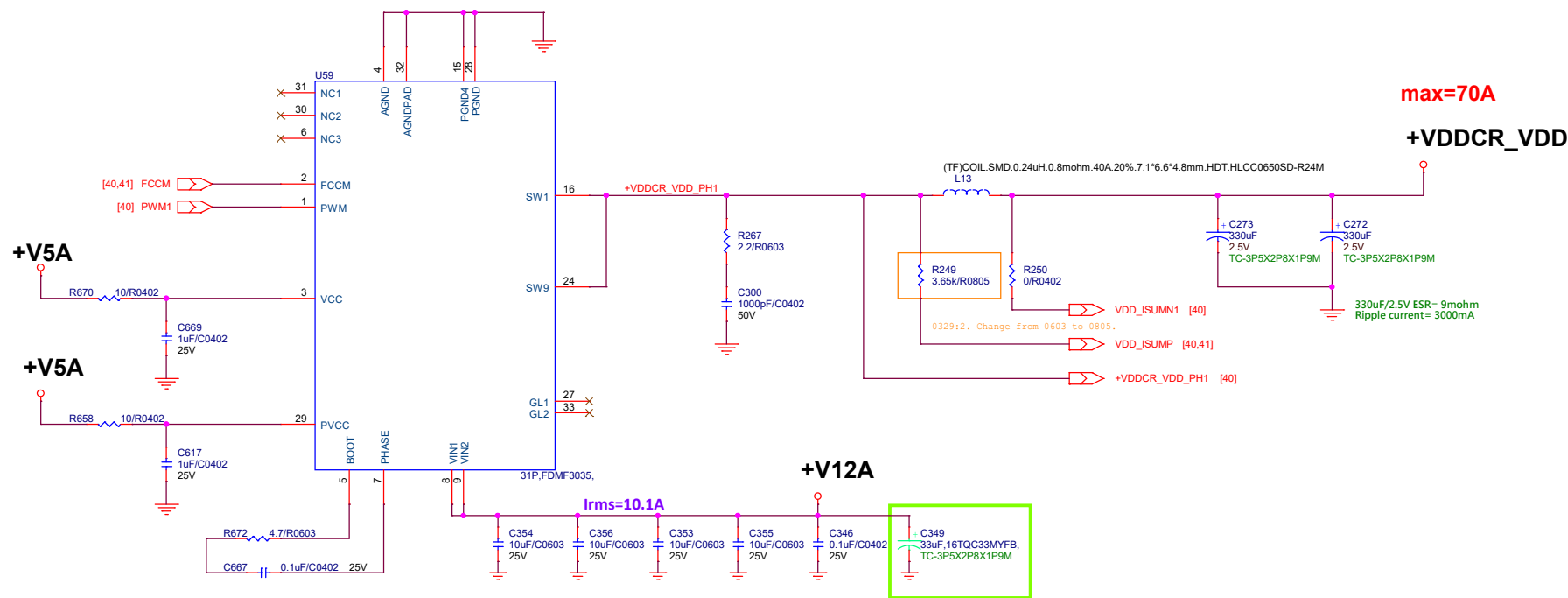


+VDDQ_VPP

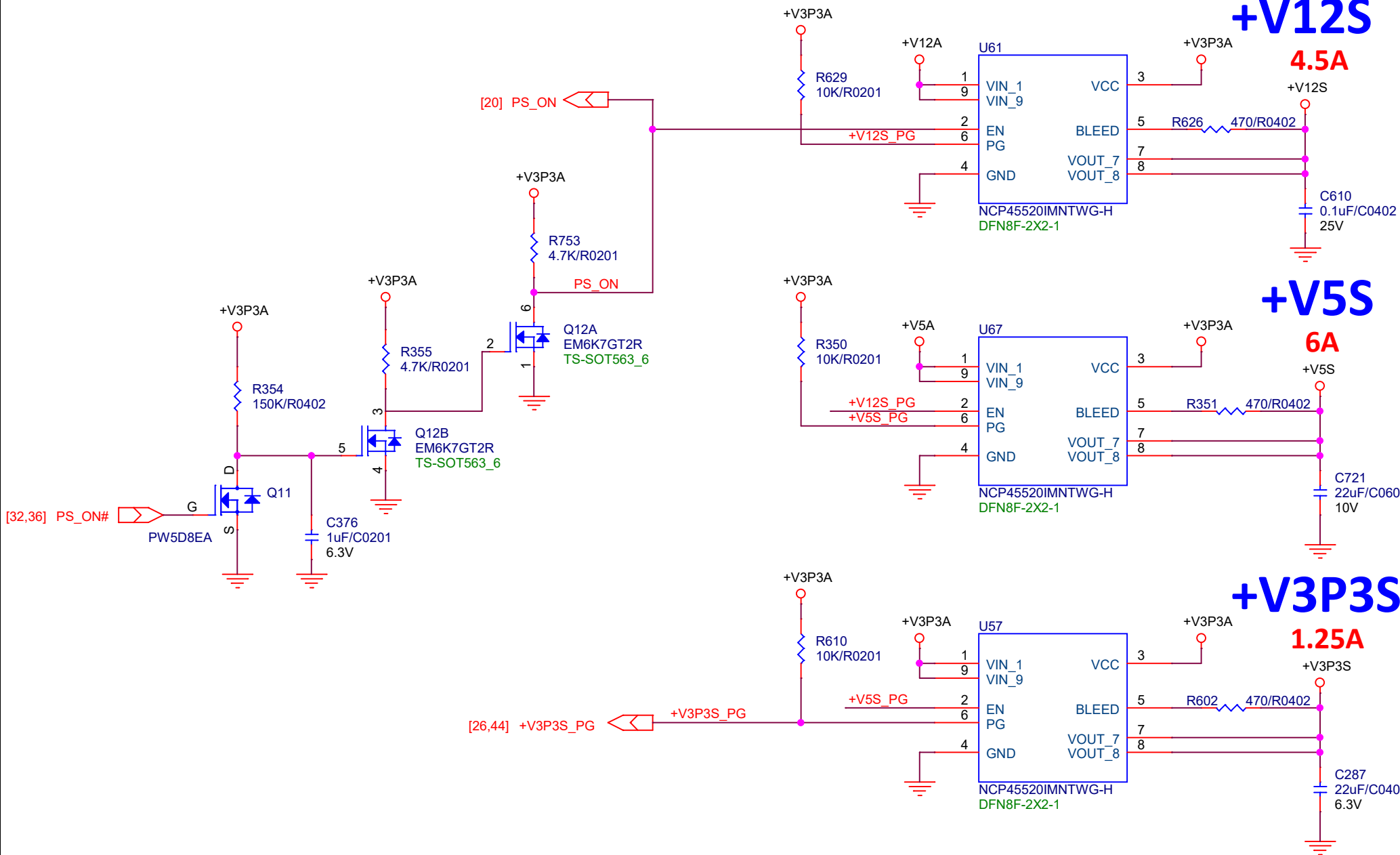


+VOP6_MEM

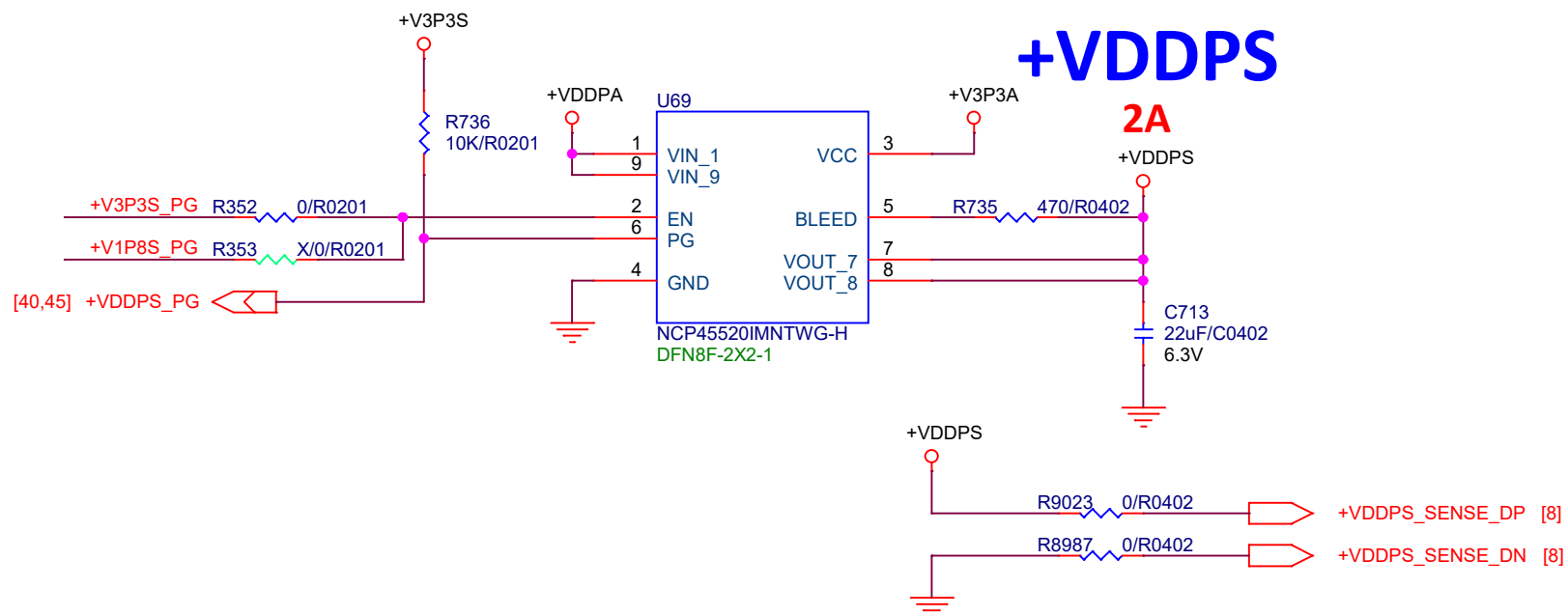
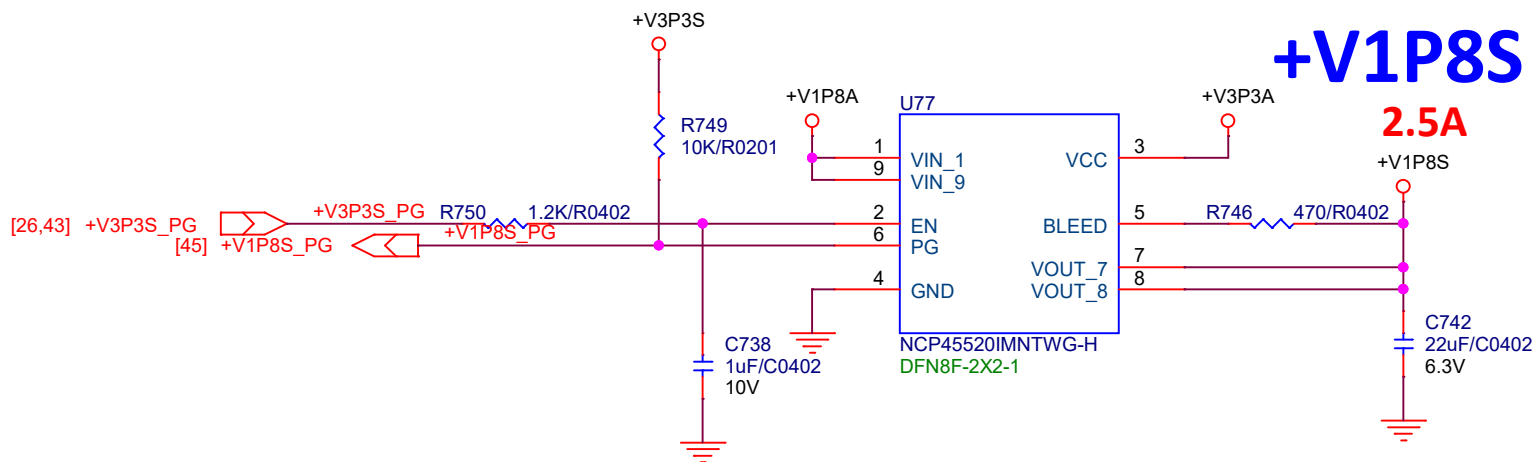


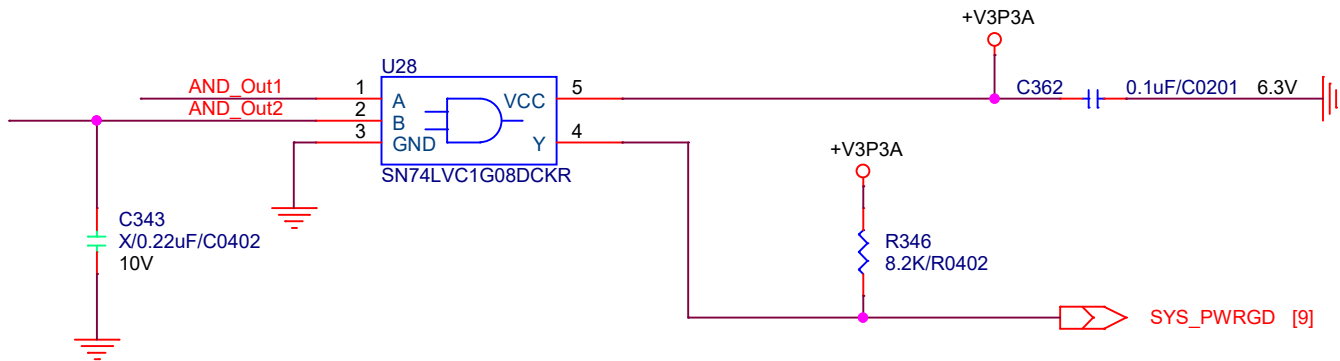
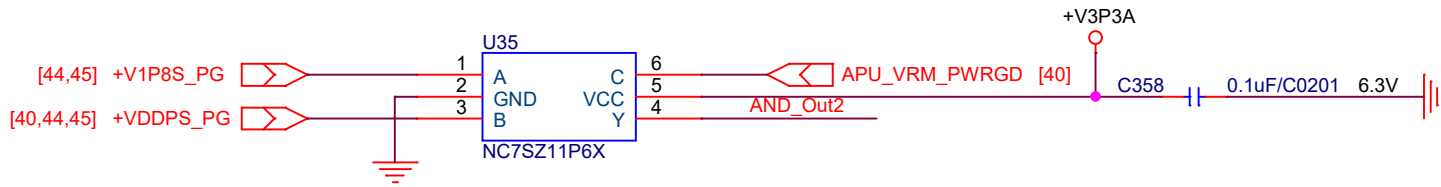
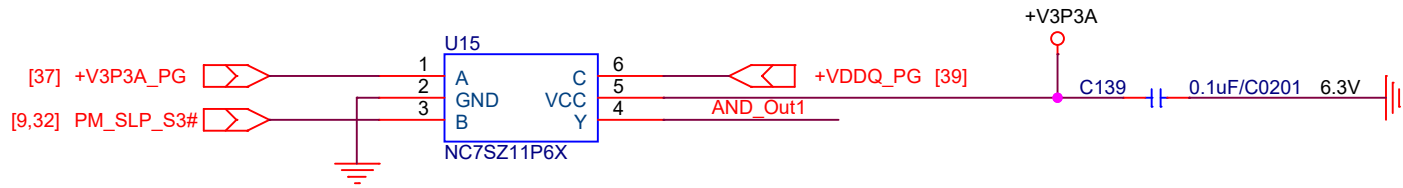
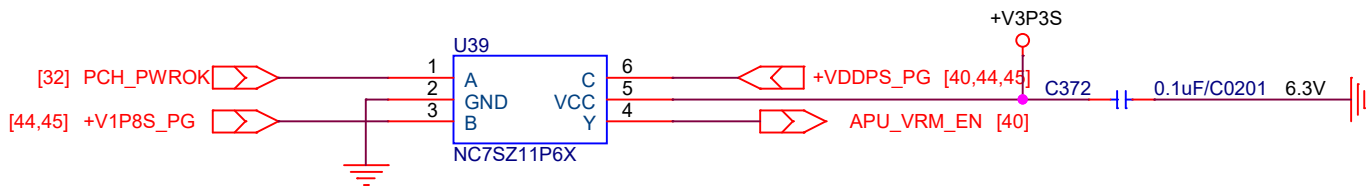


Title PWR05_+VDDCR_VDD_2phase		
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Title Sequence		
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