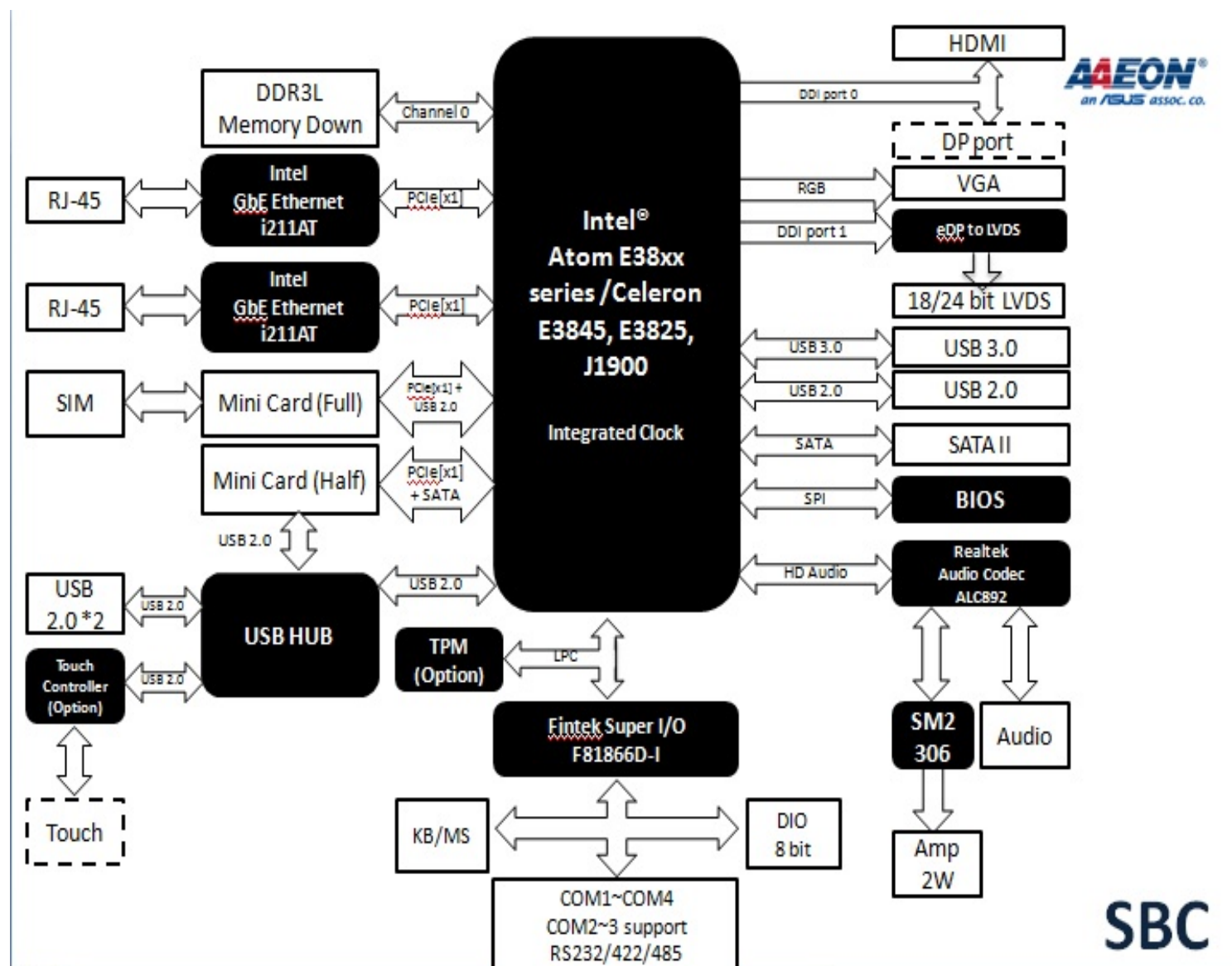


# GENE-BT06 Rev.A1.1\_0\_0

## Intel Bay Trail-M / D / I Platform Cross Compatibility



Page	Index
1	Cover Sheet
2	System Settings
3	Power Tree
4	Power Sequence
5	SoC DDR Memory
6	SoC Display
7	SoC SATA,PCIE,HDA,eMMC,SD
8	SOC CLK,PCU,RTC
9	SOC USB,LPC,SMBUS
10	SOC POWER I
11	SOC POWER II
12	SOC GND
13	Level Shift
14	DDR3L Memory on board
15	VGA
16	HDMI / DP port
17	LVDS
18	LAN1_INTEL i211
19	LAN2_INTEL i211
20	Super I/O F81866
21	SATA
22	mini-Card I / mSATA
23	mini-Card II
24	USB HUB
25	USB 3.0/2.0 PORT
26	Power input / MISC
27	PIC12F508
28	HD AUDIO ALC892
29	Touch Panel
30	SPI BIOS / TPM /LPC /COMS
31	KB /MS /HW Monitor
32	COM1~COM4
33	POWER VR_+V12A
34	POWER VR_PMIC
35	POWER VR_LDO
36	POWER VR_+VREG5, +V3.3A
37	POWER SEQUENCE LOGIC
38	Standby Power
39	Backup
40	Revision History

Project Number : EXXXXXX

Production Line : Sub.ESB.XXXX

<b>AAEON</b> an ASUS ASSOC. CO.		Title Cover Sheet	
Size C	Document Number GENE-BT06 / EGENEBT06A11	Rev. A1.1	Date: Monday, May 11, 2015
		Sheet: 1	of 41

SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_S0_SC[00]	1.8V Core	GPI	SATA_GP[0]
GPIO_S0_SC[01]	1.8V Core	GPI	SATA_GP[1]
GPIO_S0_SC[07]	1.8V Core	GPI	SD3_WP
GPIO_S0_SC[55]	1.8V Core		
GPIO_S0_SC[56]	1.8V Core		
GPIO_S0_SC[57]	1.8V Core		
GPIO_S0_SC[58]	1.8V Core		
GPIO_S0_SC[59]	1.8V Core		LVDS_RB[10]
GPIO_S0_SC[60]	1.8V Core		LVDS_RB[11]
GPIO_S0_SC[61]	1.8V Core		LVDS_RB[12]
GPIO_S0_SC[92]	1.8V Core		LVDS_RB[13]
GPIO_S0_SC[93]	1.8V Core		LVDS_RB[14]
GPIO_S0_SC[94]	1.8V Core		
GPIO_S0_SC[95]	1.8V Core		
GPIO_S5[00]	1.8V Suspend		WAKE_R[#]
GPIO_S5[01]	1.8V Suspend		GPIO_PME#
GPIO_S5[02]	1.8V Suspend		
GPIO_S5[03]	1.8V Suspend		
GPIO_S5[04]	1.8V Suspend		
GPIO_S5[05]	1.8V Suspend		
GPIO_S5[06]	1.8V Suspend		
GPIO_S5[07]	1.8V Suspend		
GPIO_S5[08]	1.8V Suspend		
GPIO_S5[09]	1.8V Suspend		
GPIO_S5[10]	1.8V Suspend		
GPIO_S5[17]	1.8V Suspend		
GPIO_S5[22]	1.8V Suspend		
GPIO_S5[23]	1.8V Suspend		
GPIO_S5[24]	1.8V Suspend		
GPIO_S5[25]	1.8V Suspend		
GPIO_S5[26]	1.8V Suspend		
GPIO_S5[27]	1.8V Suspend		
GPIO_S5[28]	1.8V Suspend		
GPIO_S5[29]	1.8V Suspend		
GPIO_S5[30]	1.8V Suspend		

F81866D GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#
GPIO02	5V	I_VSB3V	Native	PM_SUS_WARN#
GPIO03	5V	I_VSB3V	Native	PM_SUS_ACK#
GPIO04	5V	I_VSB3V	Native	PM_SLP_SUS#
GPIO05	5V	I_VSB3V	Native	LAN1_DISABLE#
GPIO06	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO07	5V	I_VSB3V	Native	W_DISABLE0#
GPIO10	5V	I_VSB3V	Native	W_DISABLE1#
GPIO11	5V	I_VSB3V	Native	
GPIO12	5V	I_VSB3V	Native	DIS_TOUCH#
GPIO13	5V	I_VSB3V	Native	
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP
GPIO15	5V	I_VSB3V	Native	WDT_RST#
GPIO16	5V	I_VSB3V	Native	
GPIO17	5V	I_VSB3V	Native	SIO_PECI
GPIO20	5V	I_VSB3V	Native	
GPIO21	5V	I_VSB3V	Native	
GPIO22	5V	I_VSB3V	Native	EXT_PWRBTN#
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#
GPIO24	5V	I_VSB3V	Native	PM_SLP_S#
GPIO25	5V	I_VSB3V	Native	PSON#
GPIO26	5V	VBAT	Native	PWOK
GPIO27	5V	VBAT	Native	SIO_RSMRST#
GPIO30	5V	3VCC	Native	DCD3#
GPIO31	5V	3VCC	Native	R13#
GPIO32	5V	3VCC	Native	CTS3#
GPIO33	5V	3VCC	Native	DTR3#
GPIO34	5V	3VCC	Native	RTS3#
GPIO35	5V	3VCC	Native	DSR3#
GPIO36	5V	3VCC	Native	TX3#
GPIO37	5V	3VCC	Native	RX3#
GPIO40	5V	3VCC	Native	DCD4#
GPIO41	5V	3VCC	Native	R14#
GPIO42	5V	3VCC	Native	CTS4#
GPIO43	5V	3VCC	Native	DTR4#
GPIO44	5V	3VCC	Native	RTS4#
GPIO45	5V	3VCC	Native	DSR4#
GPIO46	5V	3VCC	Native	TX4#
GPIO47	5V	3VCC	Native	RX4#
GPIO50	5V	3VCC	Native	DIO_0
GPIO51	5V	3VCC	Native	DIO_1
GPIO52	5V	3VCC	Native	DIO_2
GPIO53	5V	3VCC	Native	DIO_3
GPIO54	5V	3VCC	Native	DIO_4
GPIO55	5V	3VCC	Native	DIO_5
GPIO56	5V	3VCC	Native	DIO_6
GPIO57	5V	3VCC	Native	DIO_7
GPIO60	5V	3VCC	Native	
GPIO61	5V	3VCC	Native	
GPIO62	5V	3VCC	Native	
GPIO63	5V	3VCC	Native	
GPIO64	5V	3VCC	Native	
GPIO65	5V	I_VSB3V	Native	LPC_PME#
GPIO66	5V	VBAT	Native	DPWOK
GPIO67	5V	I_VSB3V	Native	PM_SLP_S#
GPIO70	5V	3VCC	Native	LVDS_EN
GPIO71	5V	3VCC	Native	LVDS_CFG1
GPIO72	5V	3VCC	Native	LVDS_CFG2
GPIO73	5V	3VCC	Native	LVDS_PD#
GPIO74	5V	3VCC	Native	BOARDID_BIT0
GPIO75	5V	3VCC	Native	BOARDID_BIT1
GPIO76	5V	3VCC	Native	BOARDID_BIT2
GPIO77	5V	3VCC	Native	BOARDID_BIT3
GPIO80	5V	3VCC	Native	SEL_COM2_MD0
GPIO81	5V	3VCC	Native	SEL_COM2_MD1
GPIO82	5V	3VCC	Native	COM2_SLEW
GPIO83	5V	3VCC	Native	SEL_COM3_MD0
GPIO84	5V	3VCC	Native	SEL_COM3_MD1
GPIO85	5V	3VCC	Native	COM3_SLEW
GPIO86	5V	3VCC	Native	ADM213_EN
GPIO87	5V	3VCC	Native	81438_SD

PCB Footprints

G

D

B

C

E

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
PTN3460 Slave	C0h

PCB STACK :  
Impedence 50ohm +/-15%.

Layer 1 : Component

Layer 2 : GND

Layer 3 : Signal

Layer 4 : GND

Layer 5 : Signal

Layer 6 : VCC

Layer 7 : Signal

Layer 4 : Signal

Layer 9 : GND

Layer 10 : Solder

A4EON

an ASUS assoc. co.

Title

System Settings

Size

B

Document Number

GENE-BT06 / EGENEBT06A11

Rev:

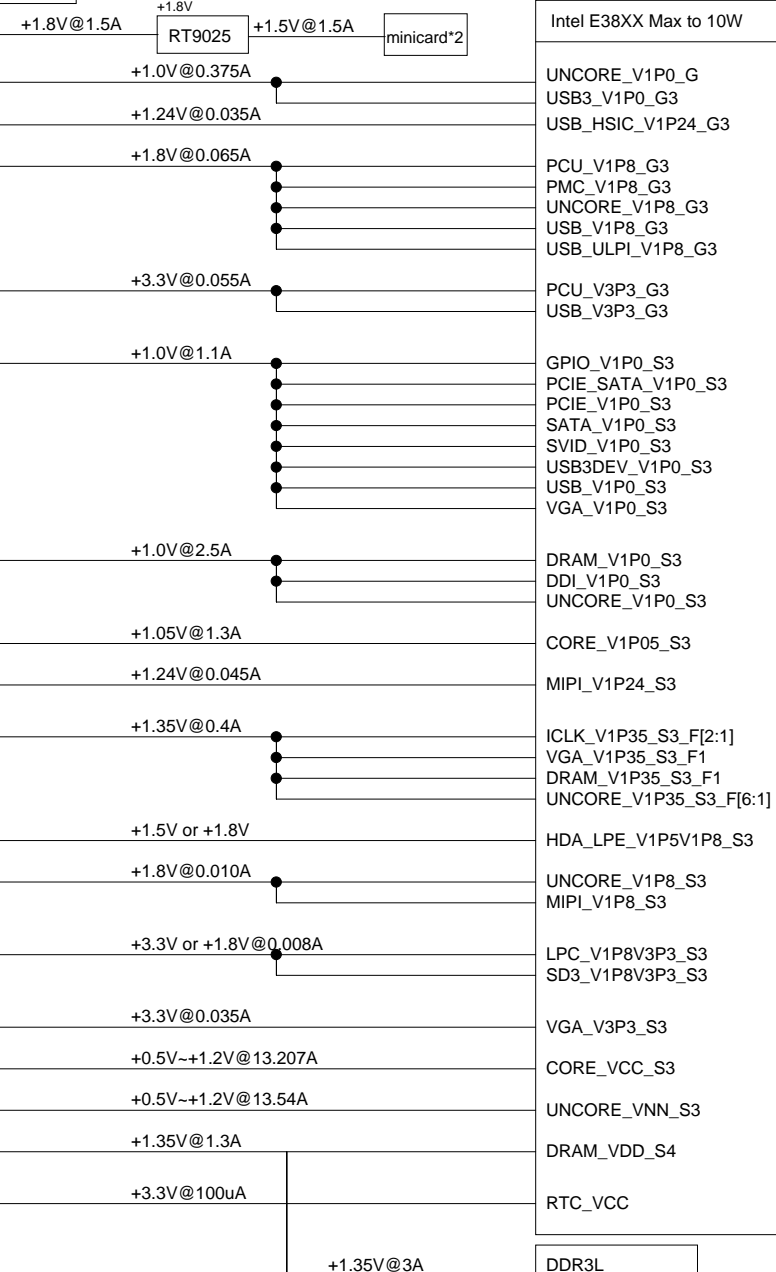
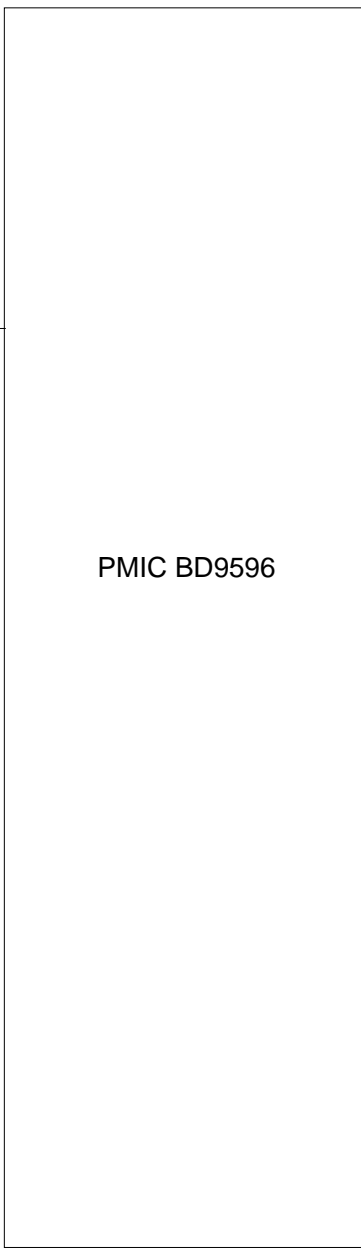
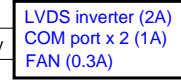
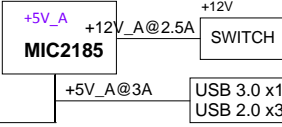
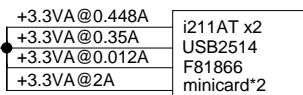
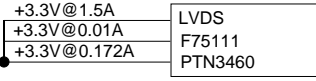
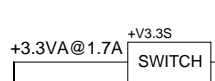
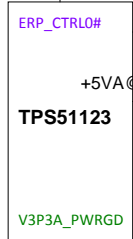
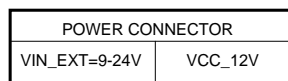
A1.1

Date:

Monday, May 11, 2015

Sheet:

2 of 41



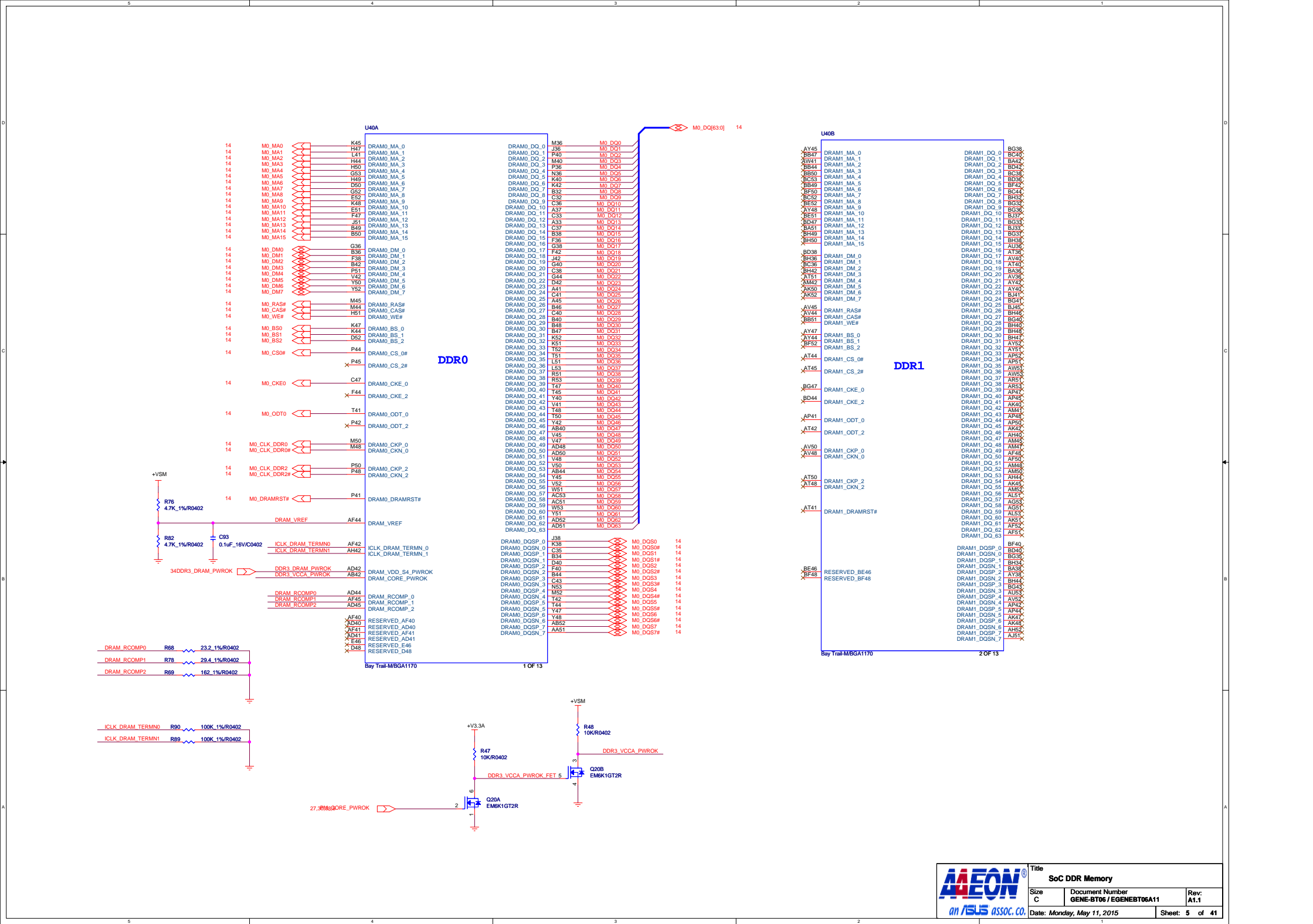
Platform Rail	Voltage Tolerances	Max Icc Premium
V1P0A - UNCORE_V1P0_G3 - USB3_V1P0_G3	1.0 V DC: ±2% AC: ±3%	375 mA
V1P24A - USB_HSIC_V1P24_G3 (Can connect to V1P0A when USB HSIC isn't used)	1.24 V DC: ±2% AC: ±2%	35 mA
V1P8A - PCU_V1P8_G3 - PMC_V1P8_G3 - UNCORE_V1P8_G3 - USB_V1P8_G3 - USB_ULPI_V1P8_G3	1.8 V DC: ±3% AC: ±2%	65 mA
V3P3A - PCU_V3P3_G3 - USB_V3P3_G3	3.3 V DC: ±2% AC: ±3%	55 mA
V1P0S - GPIO_V1P0_S3 - PCIE_SATA_V1P0_S3 - PCIE_V1P0_S3 - SATA_V1P0_S3 - SVID_V1P0_S3 - USB3DEV_V1P0_S3 - USB_V1P0_S3 - VGA_V1P0_S3	1.0 V DC: ±2% AC: ±3%	1.1 A

Platform Rail	Voltage Tolerances	Max Icc Premium
V1P0S - DRAM_V1P0_S3 - DDI_V1P0_S3 - UNCORE_V1P0_S3	1.0 V DC: ±2% AC: ±3%	2.5 A
V1P05S - CORE_V1P05_S3	1.05 V DC: ±2% AC: ±3%	1.3 A
V1P24S - MIPI_V1P24_S3 (can be grounded if MIPI CSI not used)	1.24 V DC: ±2% AC: ±3%	45 mA
V1P35S (VSFR) - ICLK_V1P35_S3_F[2:1] - VGA_V1P35_S3_F1 - DRAM_V1P35_S3_F1 - UNCORE_V1P35_S3_F[6:1]	1.35 V DC: ±3% AC: ±2%	400 mA
V1P5V1P8S (VAUD) - HDA_LPE_V1P5V1P8_S3	1.5 V (LV HDA) 1.8 V (LPE)	In V1P8S
V1P8S - UNCORE_V1P8_S3 - MIPI_V1P8_S3	1.8 V DC: ±3% AC: ±2%	10 mA
V1P8V3P3S (VSDIO,VLPC) - LPC_V1P8V3P3_S3 - SD3_V1P8V3P3_S3	1.8 V 3.3 V (V3P3A) DC: ±2% AC: ±3%	8 mA
V3P3S - VGA_V3P3_S3	3.3 V DC: ±2% AC: ±3%	35 mA
VCC - CORE_VCC_S3	See Table 78	11 A
VNN - UNCORE_VNN_S3	See Table 78	14 A
VDD - DRAM_VDD_S4	1.35 V DC: ±2% AC: ±3%	1.3 A
VRTC - RTC_VCC	G3: 2-3 V at battery* Otherwise: V3P3A (pre diode drop)	100 uA (6 uA Avg.) (see note)

+V1.8A -> +V1.0A -> +V1.2A -> +V3.3A

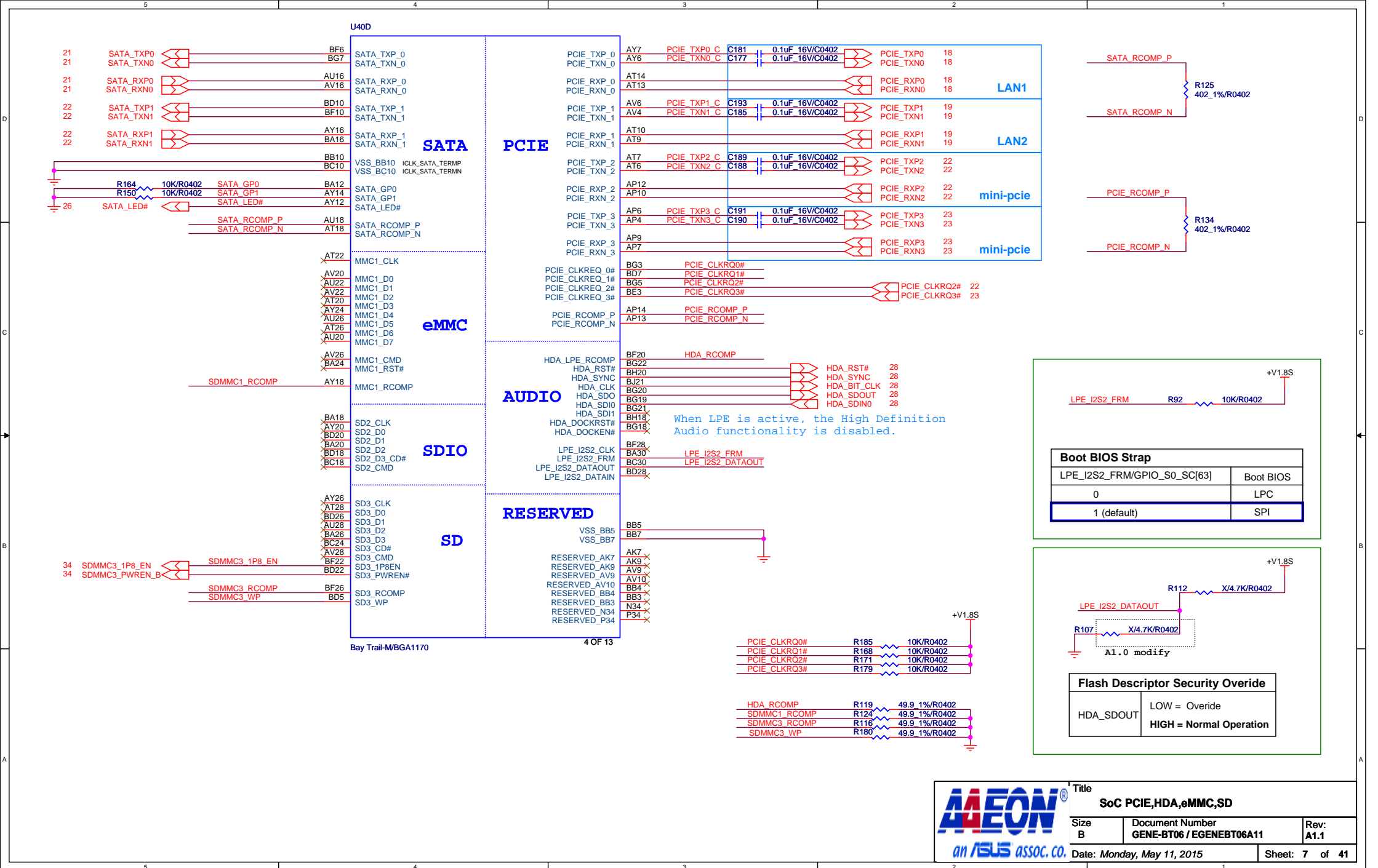
+V1.0S -> +V1.05S -> +V1.8S -> +V1.2S -> +V3.3S -> +VSFR -> +V1.5S

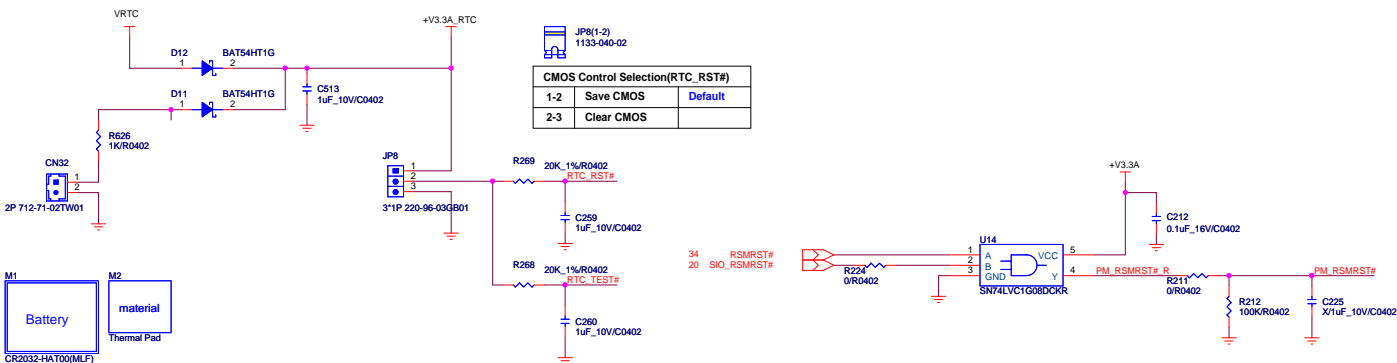




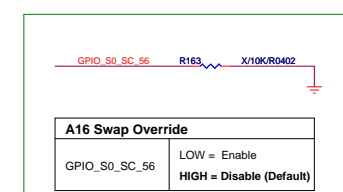
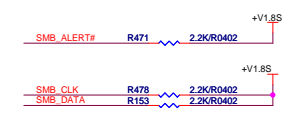
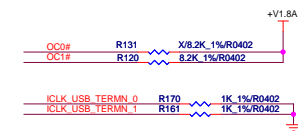
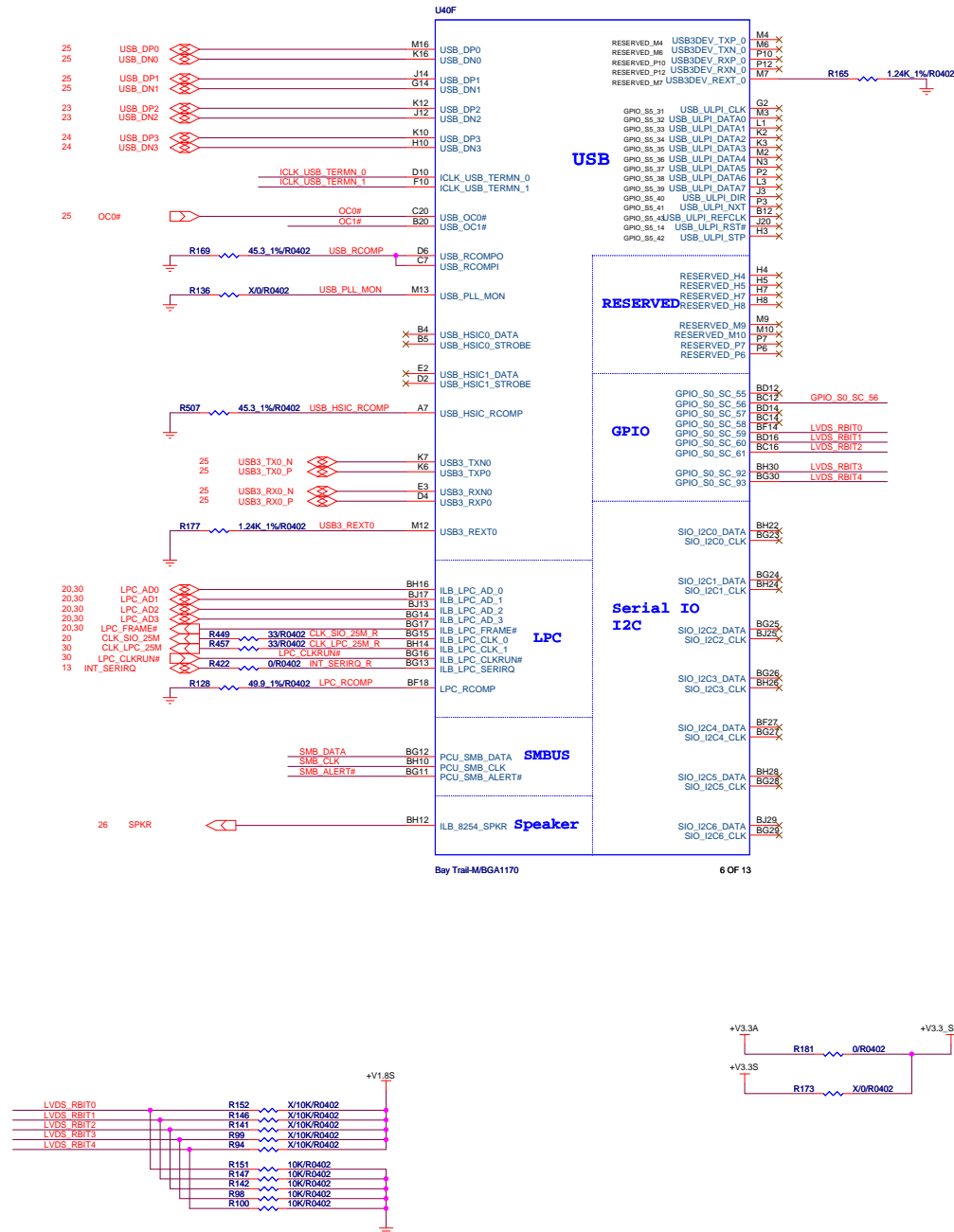




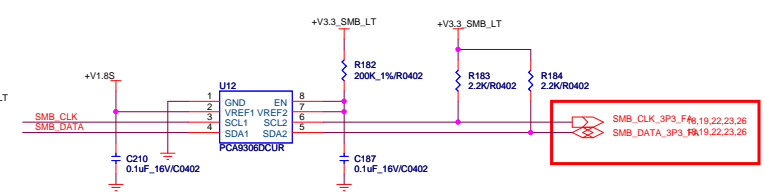
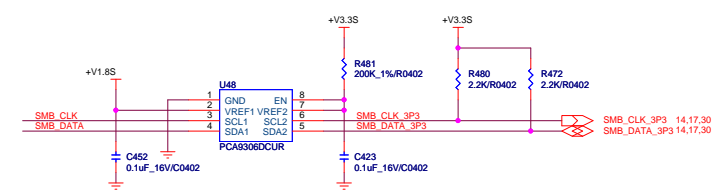




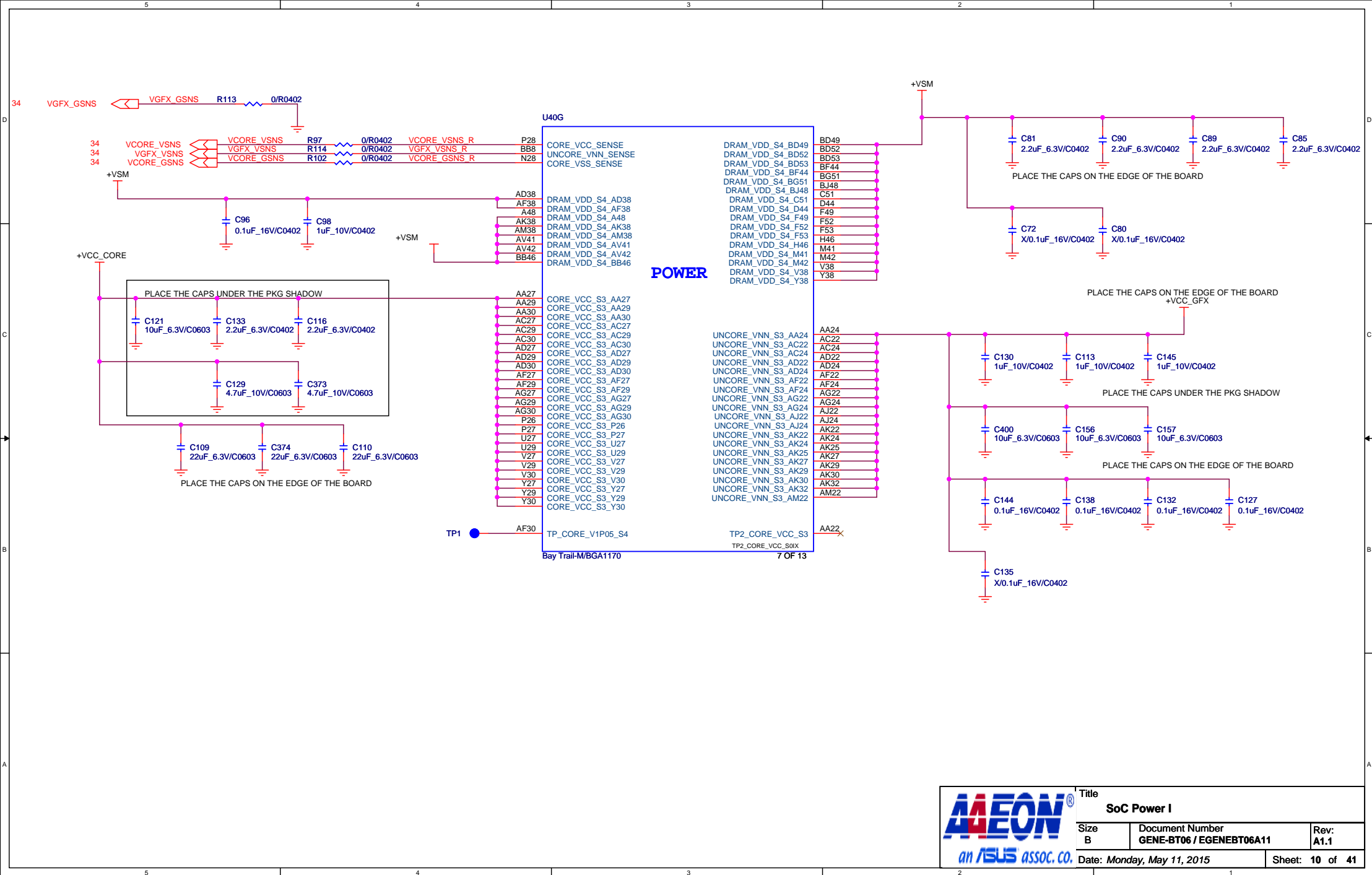




A16 Swap Override	
GPIO_S0_SC_56	LOW = Enable HIGH = Disable (Default)



SMB\_CLK\_3P3 F6,19,22,23,26  
SMB\_DATA\_3P3 F6,19,22,23,26

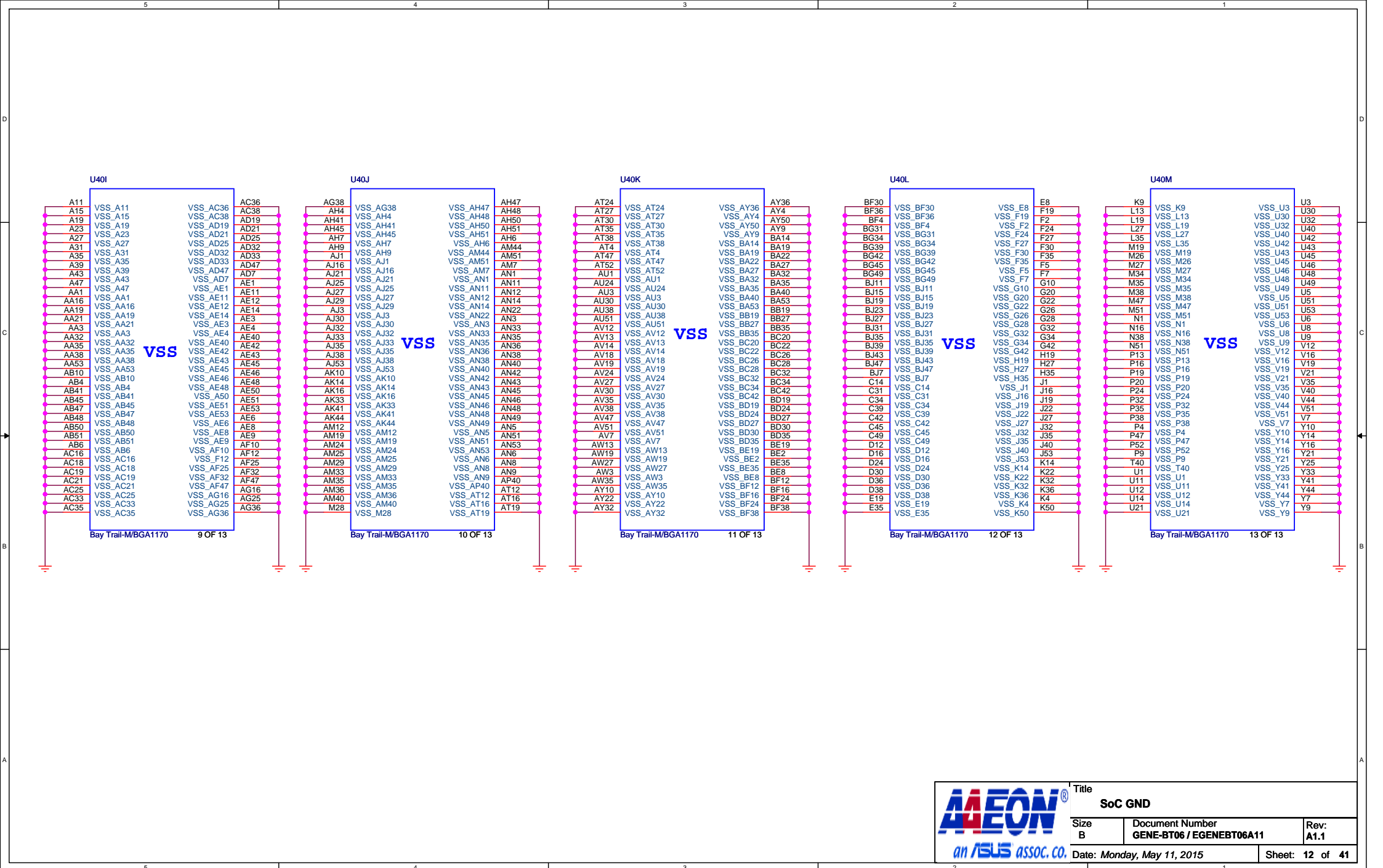


# POWER

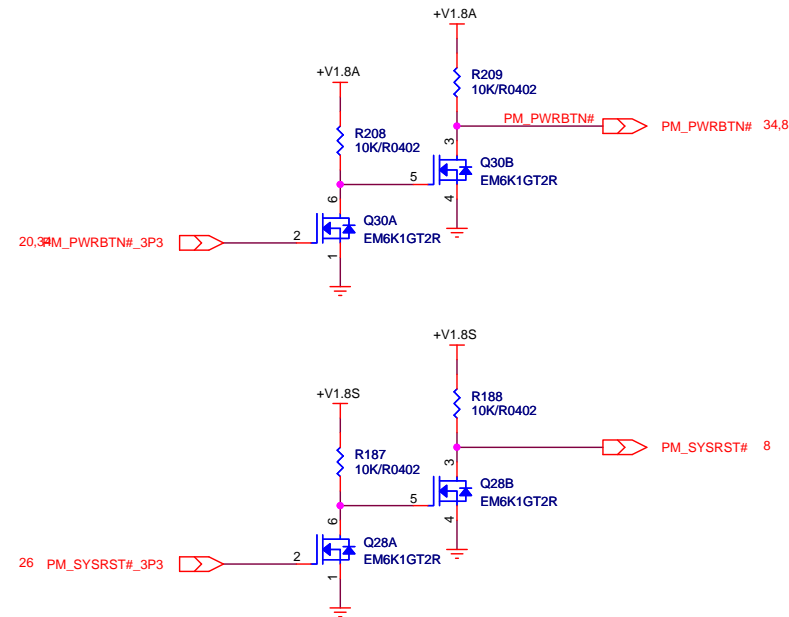
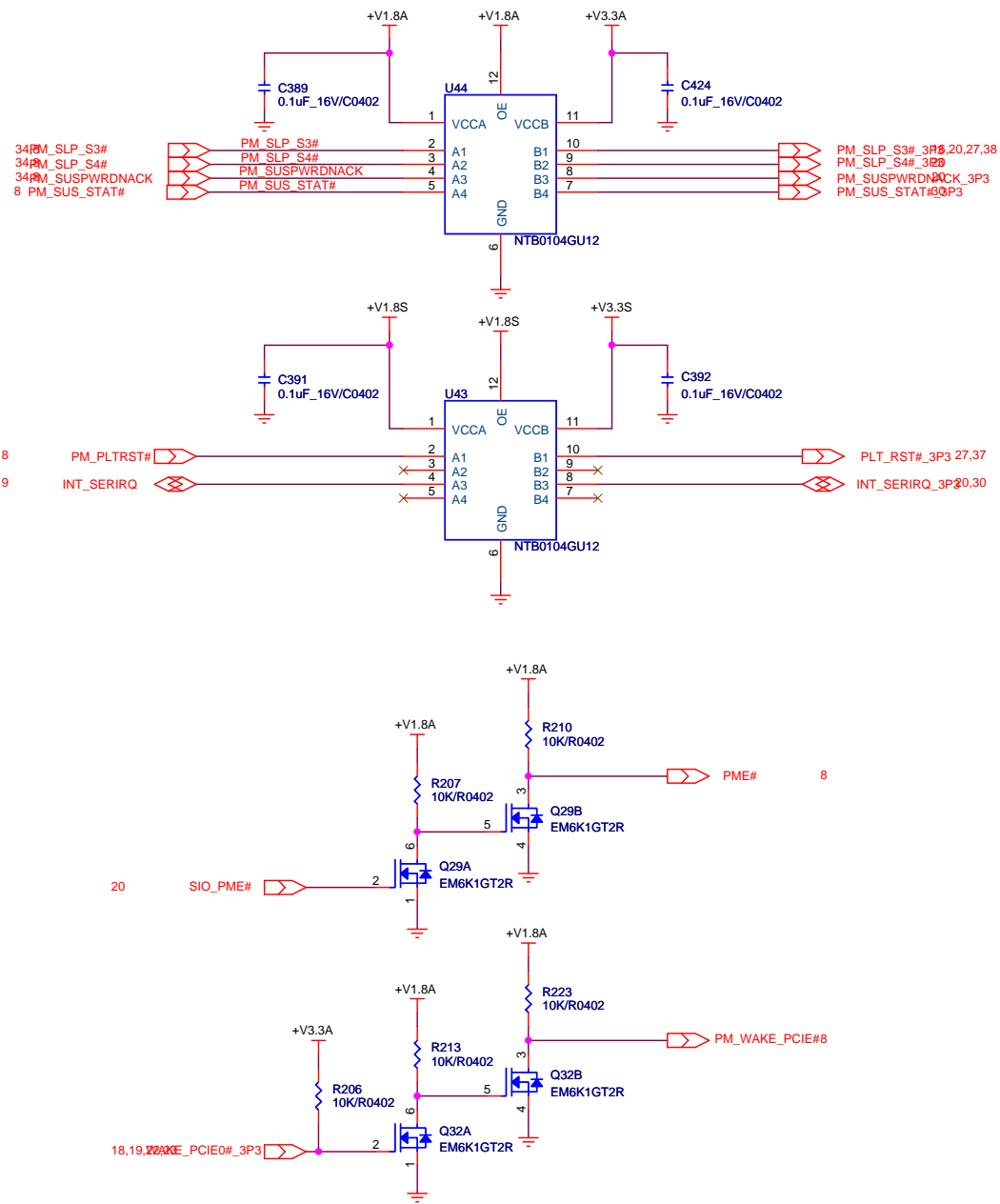
8 OF 13

Bay Trail-MBGA1170

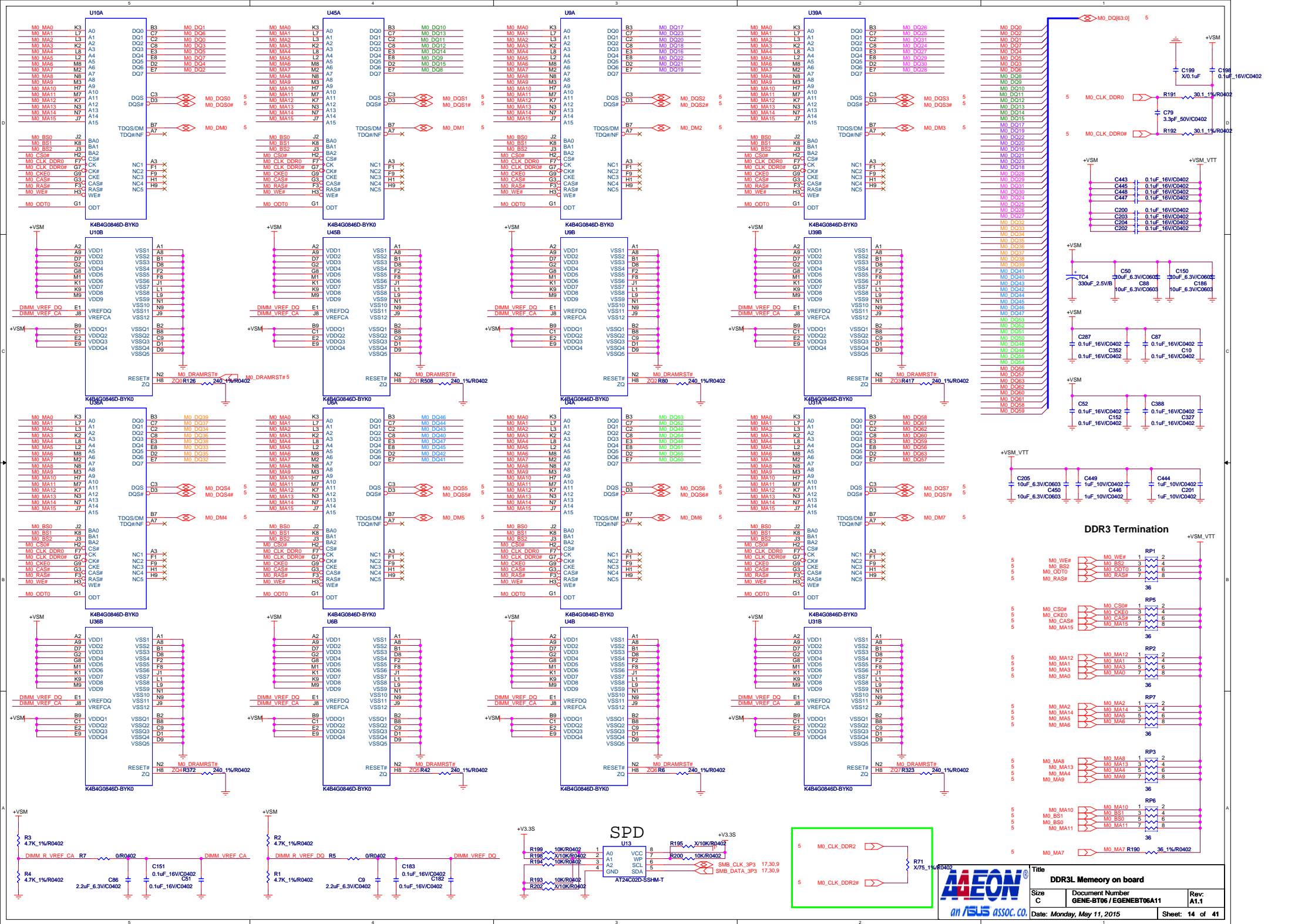
Bay-Trail M/D = connect GND  
Bay-Trail I = connect +V1.2S



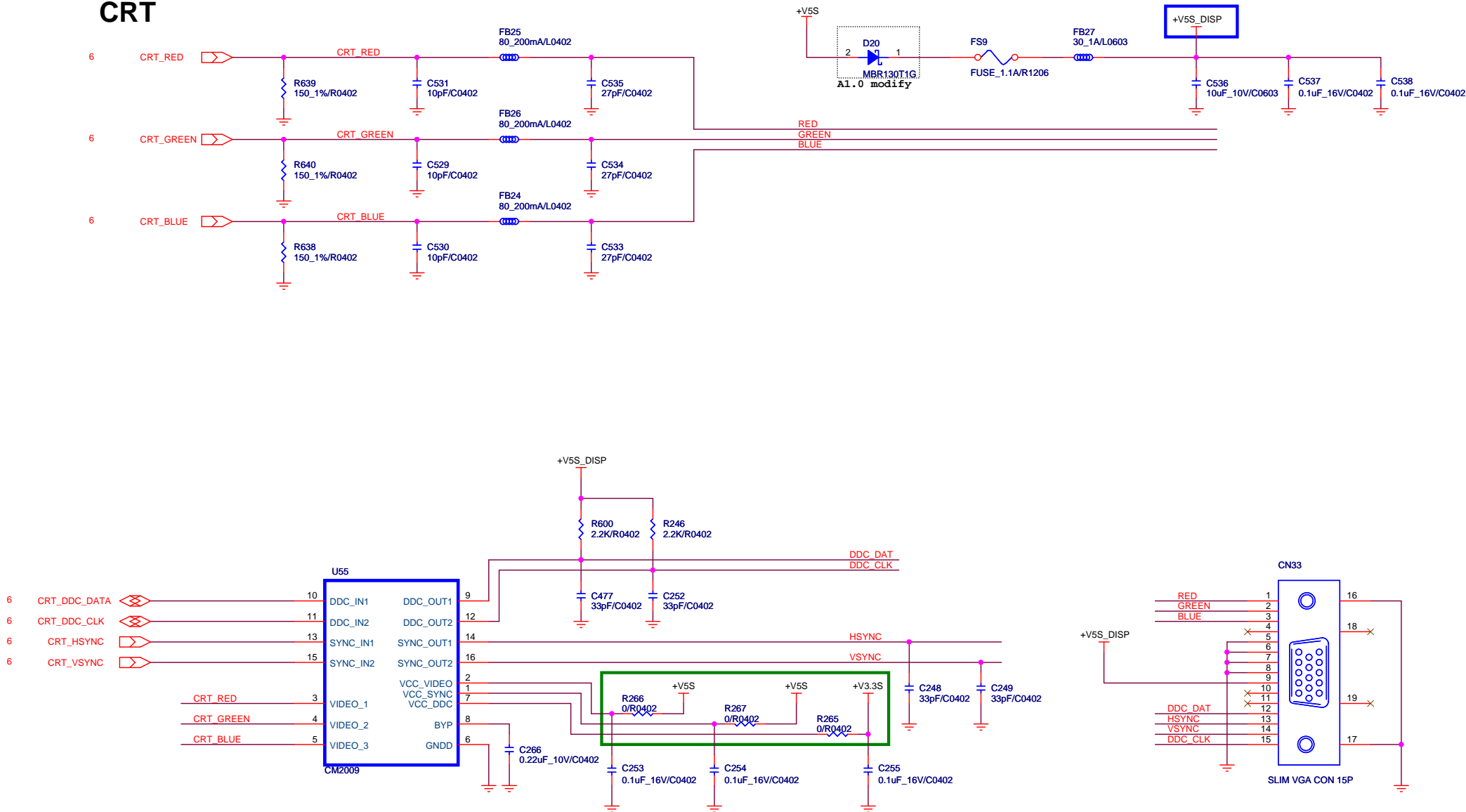
Title <b>SoC GND</b>		
Size <b>B</b>	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <b>Monday, May 11, 2015</b>		Sheet: <b>12 of 41</b>



Title		
Level Shift		
Size B	Document Number GENE-BT06 / EGENEBT06A11	Rev: A1.1
Date: Monday, May 11, 2015		Sheet: 13 of 41



# CRT

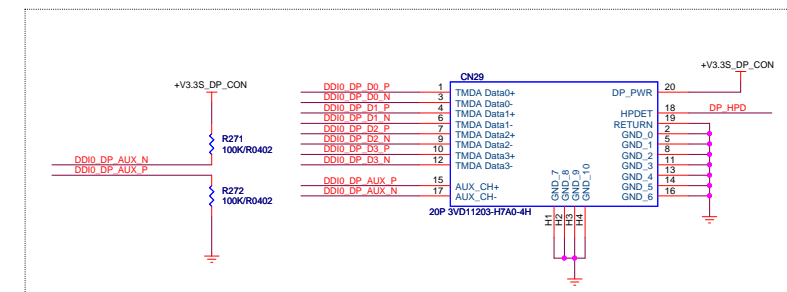
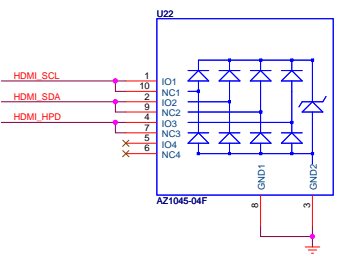
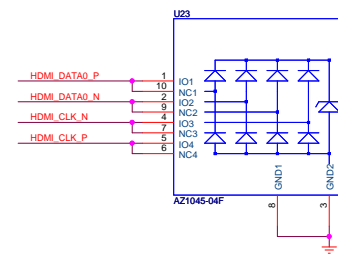
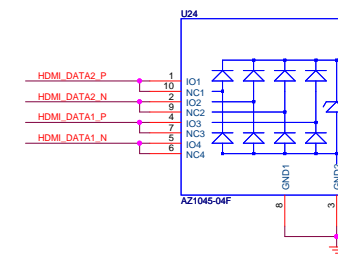
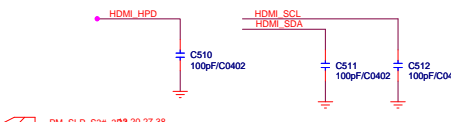
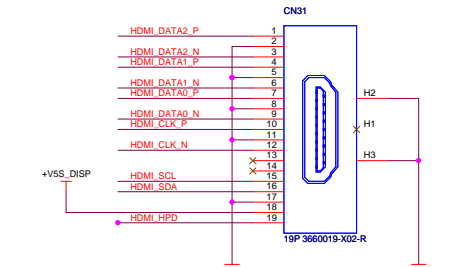
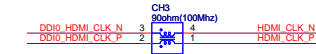
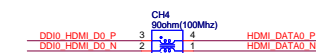
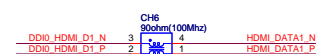
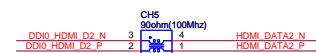
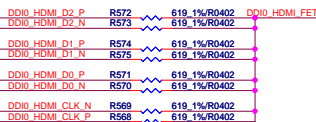
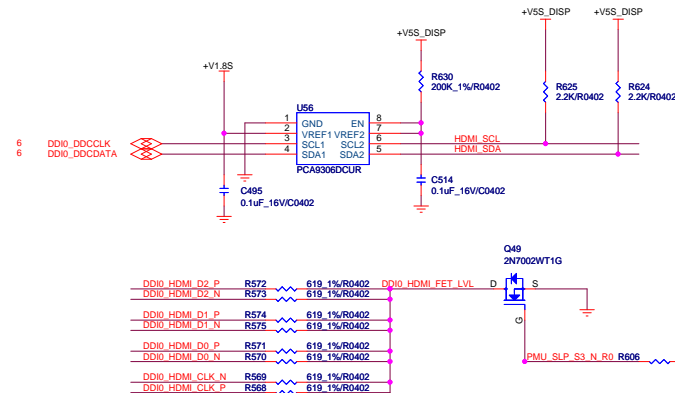
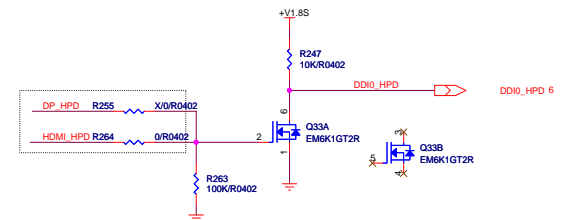


Title <b>VGA</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <b>Monday, May 11, 2015</b>		Sheet: <b>15 of 41</b>



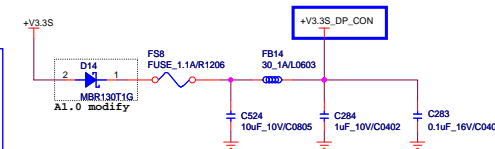
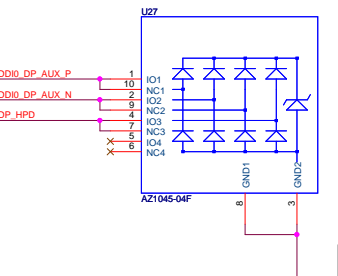
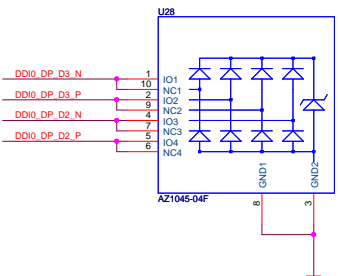
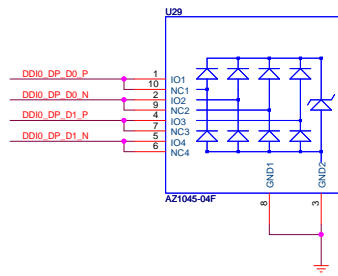
# HDMI

6	DDIO_TX0_P	DDIO_TX0_P	C237	0.1uF_16V/C0402	DDIO_HDMI_D2_P
6	DDIO_TX0_N	DDIO_TX0_N	C238	0.1uF_16V/C0402	DDIO_HDMI_D2_N
6	DDIO_TX1_P	DDIO_TX1_P	C239	0.1uF_16V/C0402	DDIO_HDMI_D1_P
6	DDIO_TX1_N	DDIO_TX1_N	C240	0.1uF_16V/C0402	DDIO_HDMI_D1_N
6	DDIO_TX2_P	DDIO_TX2_P	C236	0.1uF_16V/C0402	DDIO_HDMI_D0_P
6	DDIO_TX2_N	DDIO_TX2_N	C235	0.1uF_16V/C0402	DDIO_HDMI_D0_N
6	DDIO_TX3_P	DDIO_TX3_P	C233	0.1uF_16V/C0402	DDIO_HDMI_CLK_P
6	DDIO_TX3_N	DDIO_TX3_N	C234	0.1uF_16V/C0402	DDIO_HDMI_CLK_N



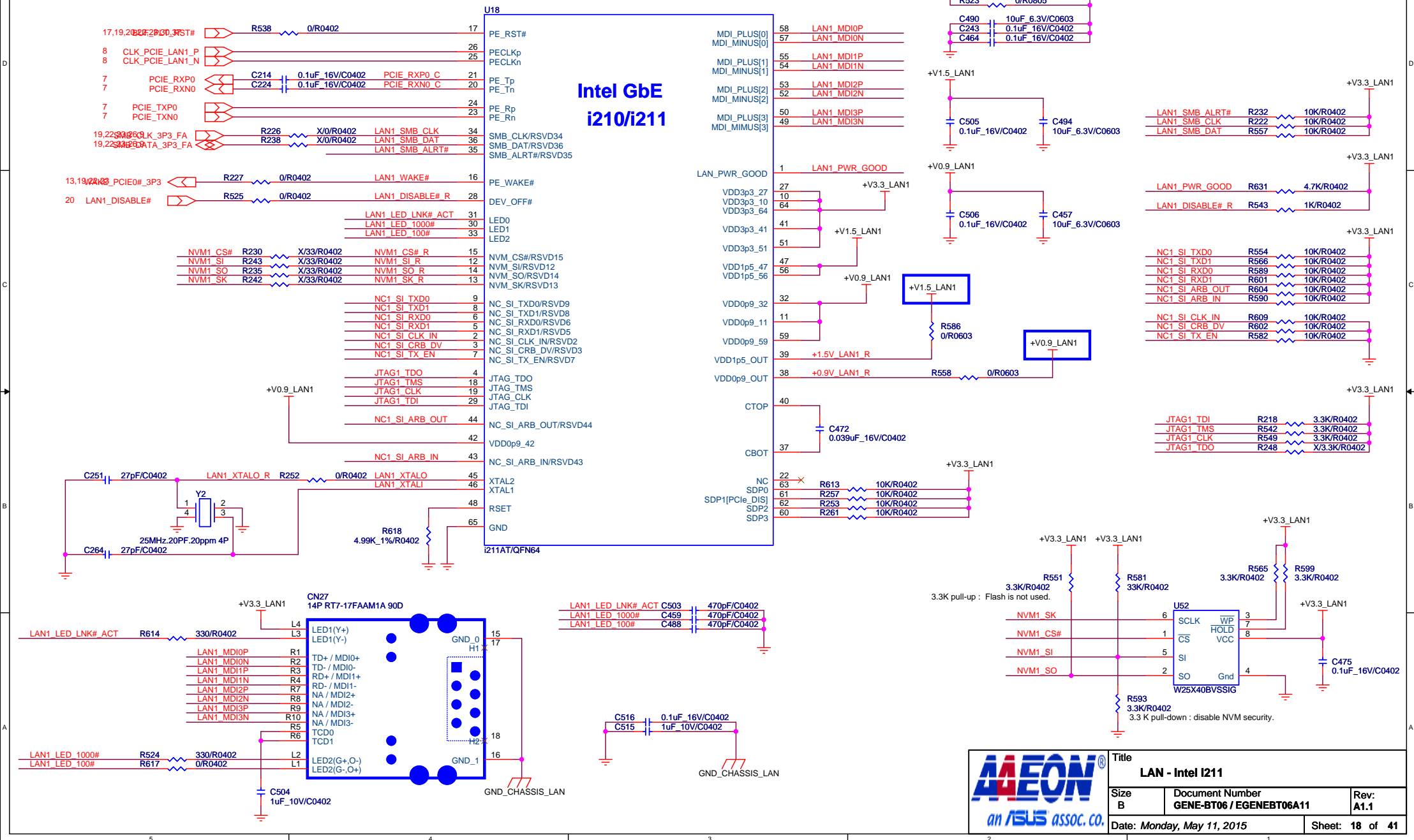
## A1.1 add

DDIO_TX0_P	R654	X0/R0402	DDIO_TX0_P_R	C278	0.1uF_16V/C0402	DDIO_DP_D0_P
DDIO_TX0_N	R655	X0/R0402	DDIO_TX0_N_R	C277	0.1uF_16V/C0402	DDIO_DP_D0_N
DDIO_TX1_P	R656	X0/R0402	DDIO_TX1_P_R	C276	0.1uF_16V/C0402	DDIO_DP_D1_P
DDIO_TX1_N	R657	X0/R0402	DDIO_TX1_N_R	C275	0.1uF_16V/C0402	DDIO_DP_D1_N
DDIO_TX2_P	R658	X0/R0402	DDIO_TX2_P_R	C274	0.1uF_16V/C0402	DDIO_DP_D2_P
DDIO_TX2_N	R659	X0/R0402	DDIO_TX2_N_R	C273	0.1uF_16V/C0402	DDIO_DP_D2_N
DDIO_TX3_P	R660	X0/R0402	DDIO_TX3_P_R	C272	0.1uF_16V/C0402	DDIO_DP_D3_P
DDIO_TX3_N	R661	X0/R0402	DDIO_TX3_N_R	C271	0.1uF_16V/C0402	DDIO_DP_D3_N
DDIO_AUXP			DDIO_AUXP	C520	0.1uF_16V/C0402	DDIO_DP_AUX_P
DDIO_AUXN			DDIO_AUXN	C519	0.1uF_16V/C0402	DDIO_DP_AUX_N



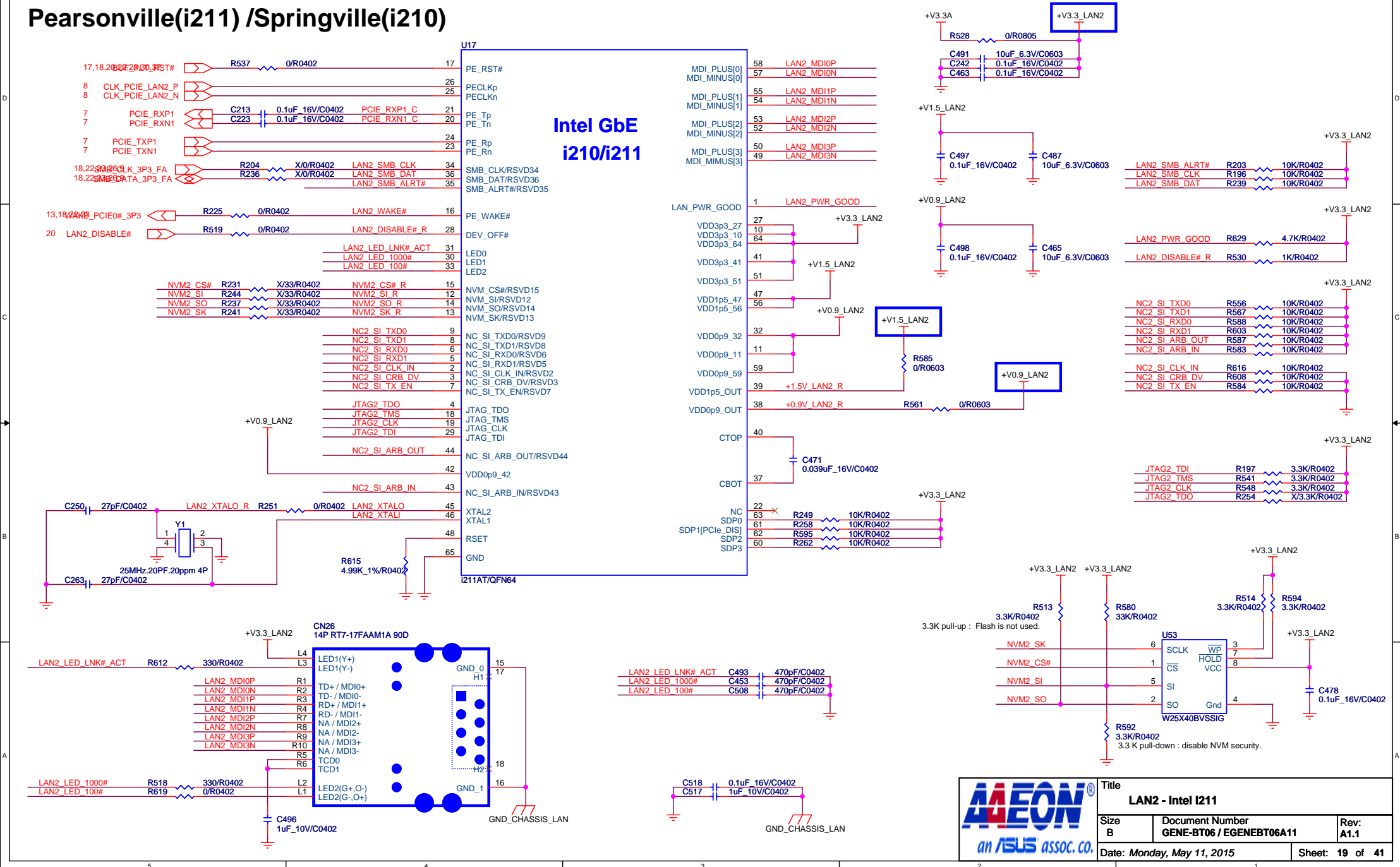


## Pearsonville(i211) /Springville(i210)



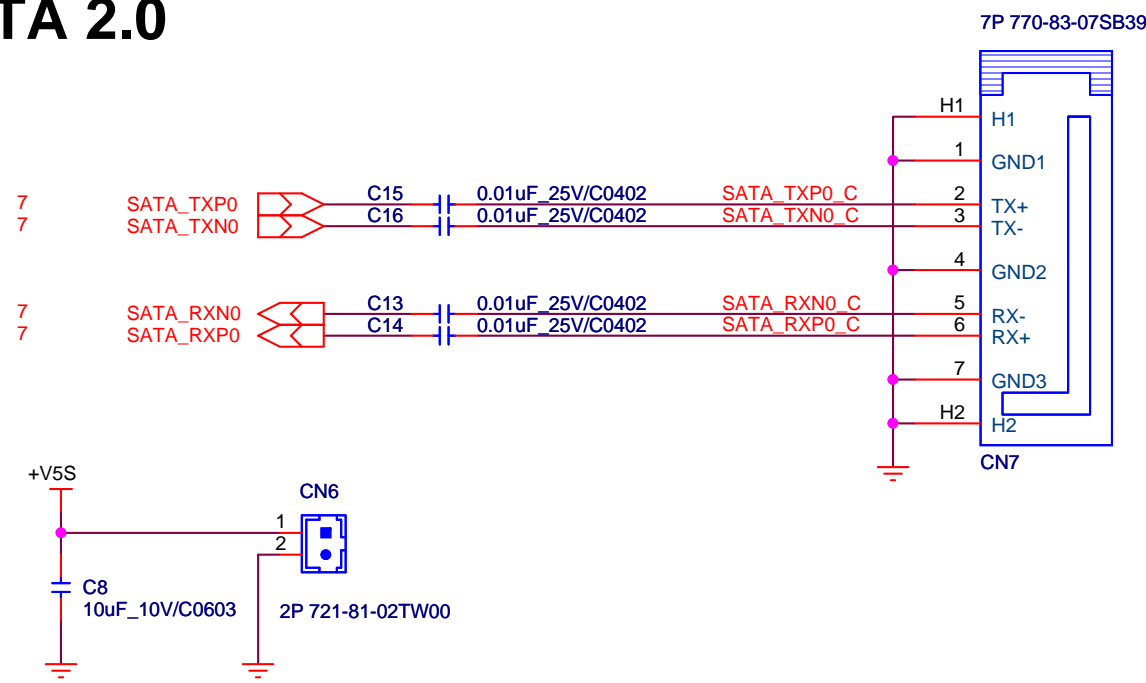
Title		
LAN - Intel I211		
Size B	Document Number GENE-BT06 / EGENEBT06A11	Rev: A1.1
Date: Monday, May 11, 2015		Sheet: 18 of 41

## Pearsonville(i211) /Springville(i210)

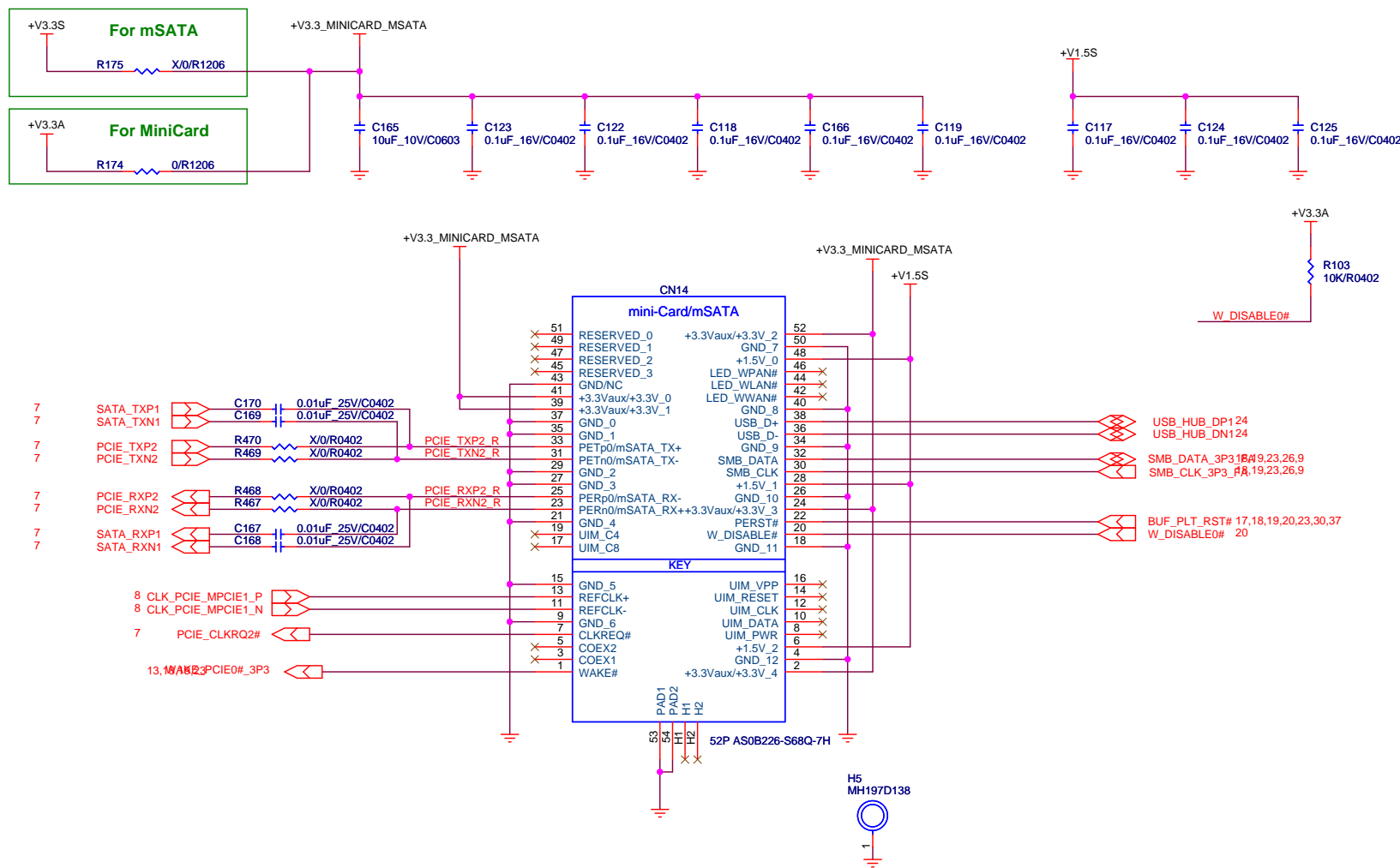




# SATA 2.0

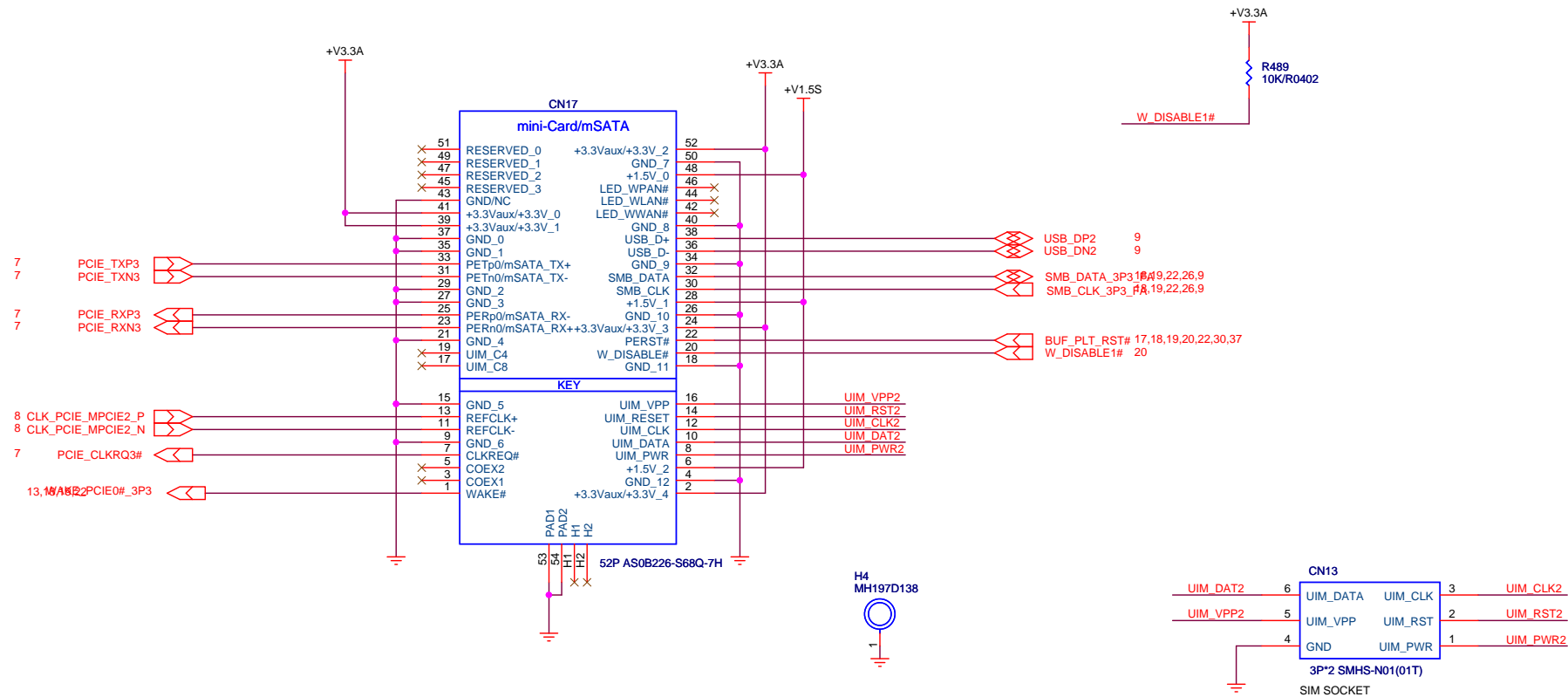
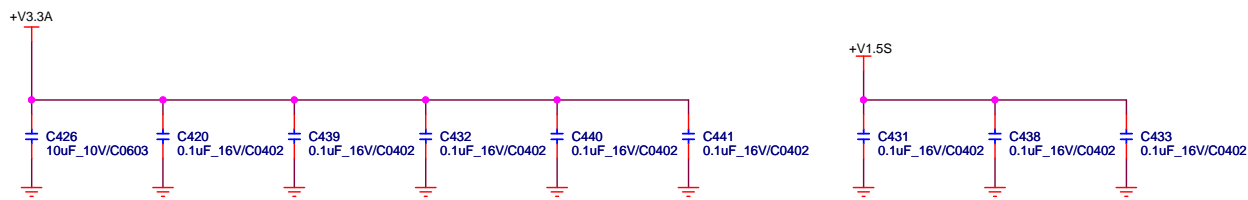


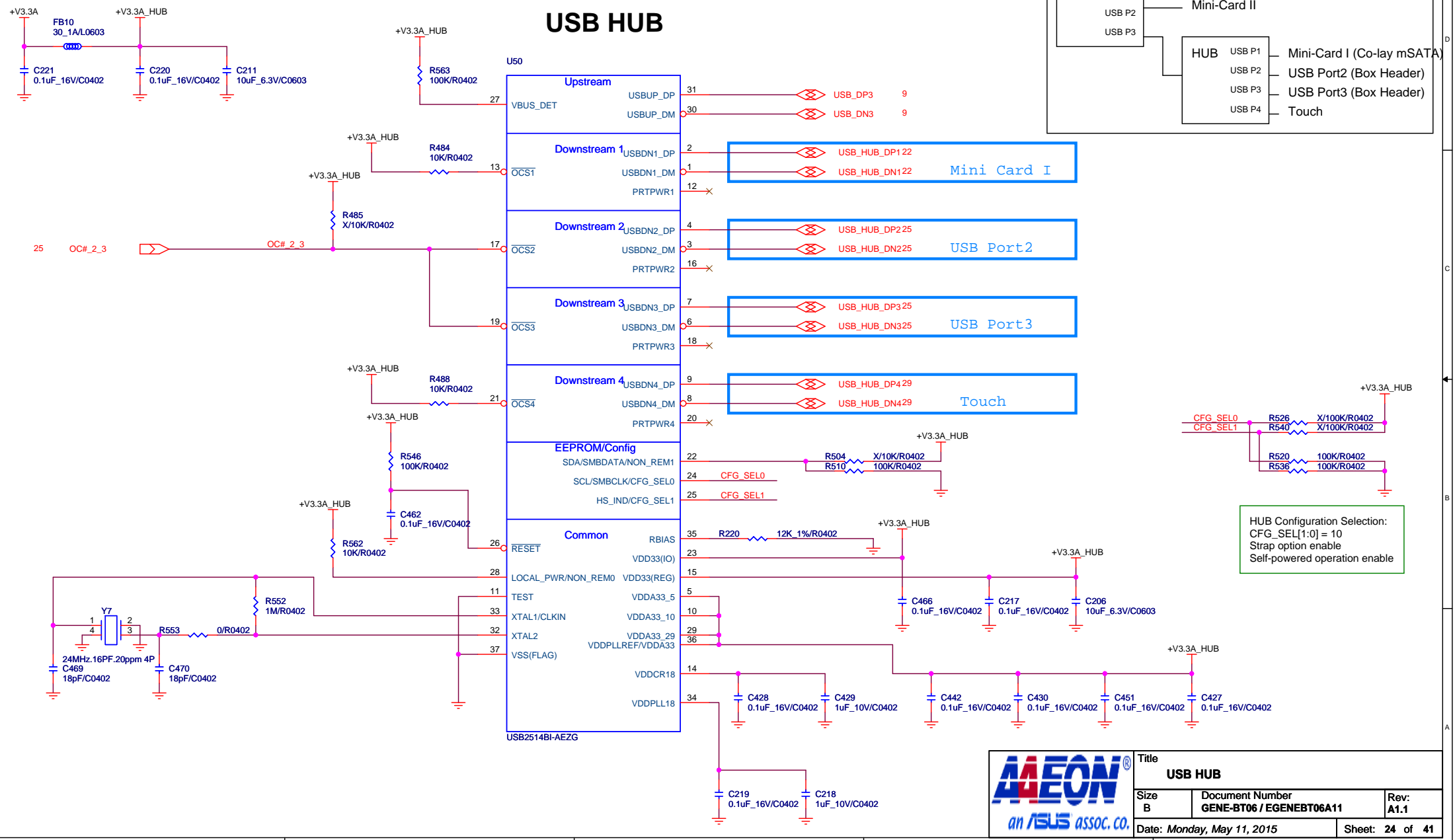
Title SATA		
Size A	Document Number GENE-BT06 / EGENEBT06A11	Rev: A1.1
Date: Monday, May 11, 2015		Sheet: 21 of 41



Title <b>mSATA, MINI CARD</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <b>Monday, May 11, 2015</b>		Sheet: <b>22 of 41</b>








USB MAP			
BT	USB P1	USB 3.0 Port0 (Rear IO)	
	USB P0	USB Port1 (Rear IO)	
	USB P2	Mini-Card II	
	USB P3		
HUB	USB P1	Mini-Card I (Co-lay mSATA)	
	USB P2	USB Port2 (Box Header)	
	USB P3	USB Port3 (Box Header)	
	USB P4	Touch	

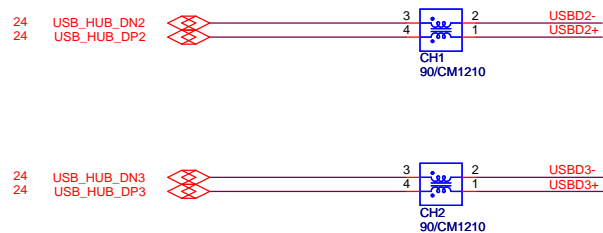
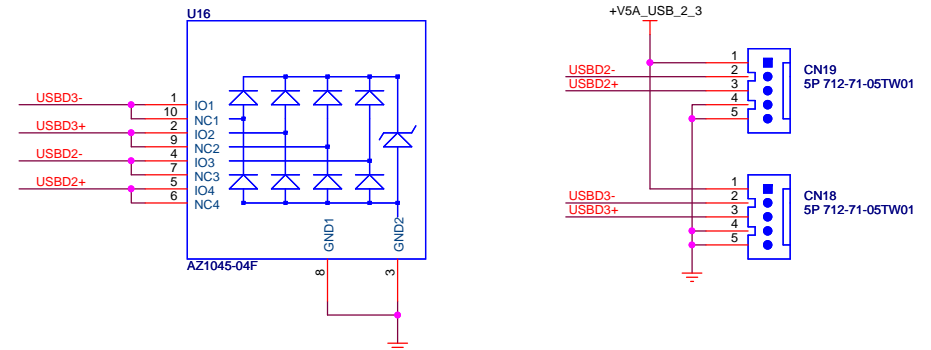
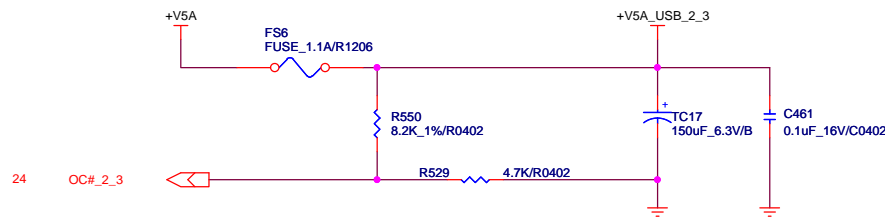
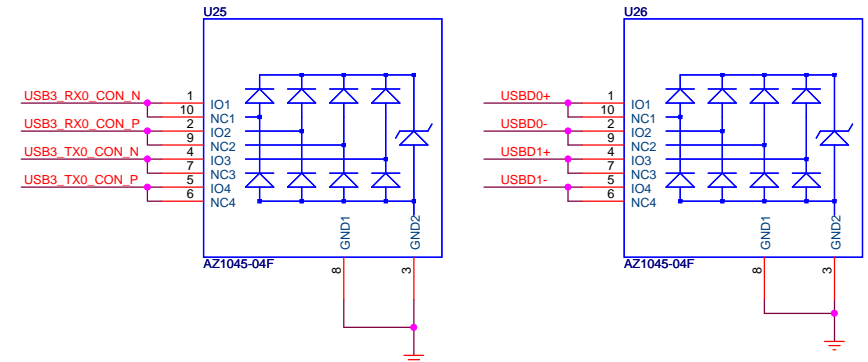
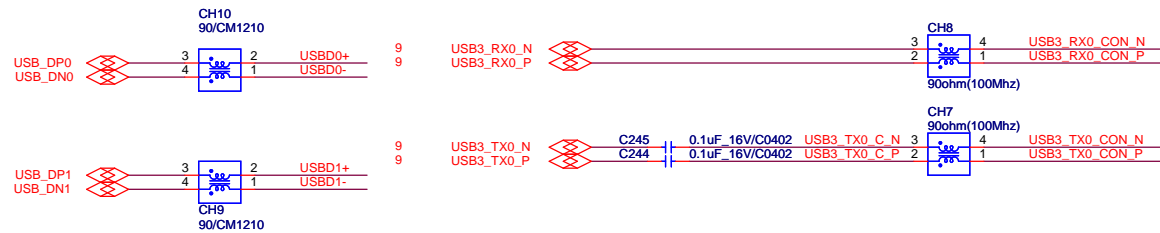
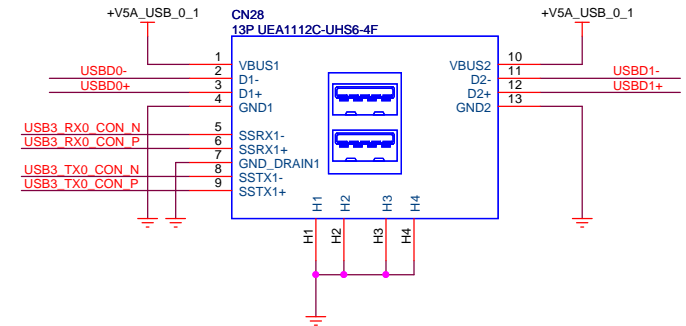
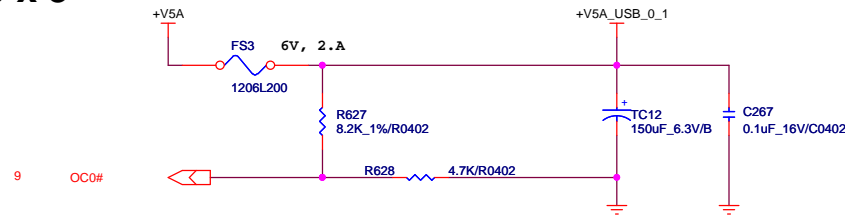
HUB Configuration Selection:  
CFG\_SEL[1:0] = 10  
Strap option enable  
Self-powered operation enable



an ASUS ASSOC. CO.

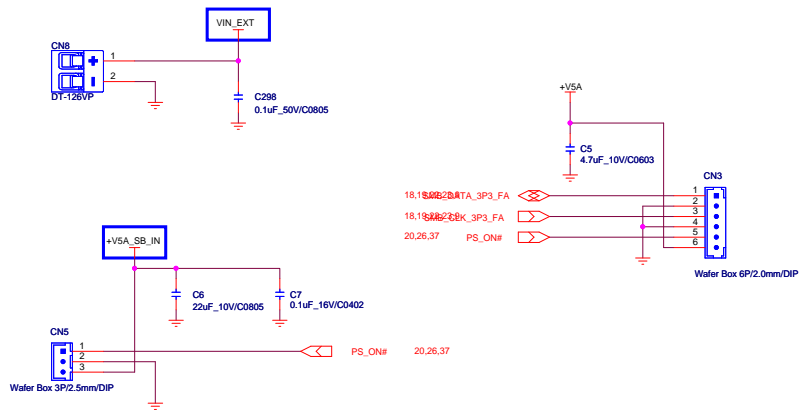
Title <b>USB HUB</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <b>Monday, May 11, 2015</b>		Sheet: <b>24 of 41</b>

# USB3.0 x 1 + USB2.0 x 3

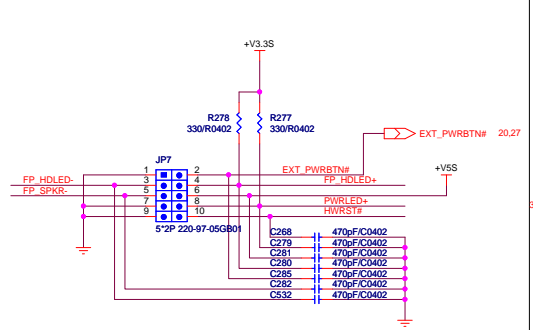


Title		
USB PORT		
Size	Document Number	Rev:
Custom	GENE-BT06 / EGENEBT06A11	A1.1
Date: Monday, May 11, 2015	Sheet: 25 of 41	

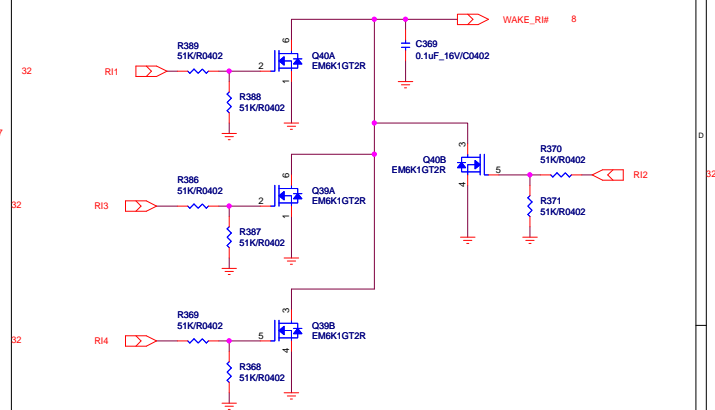
## Power Input



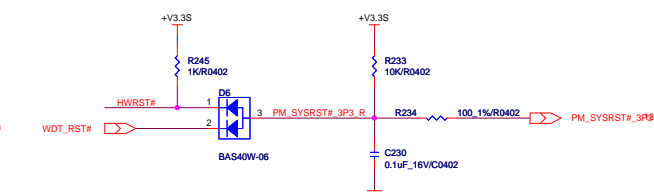
## Front Panel



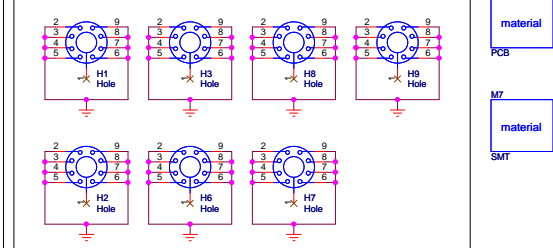
## Wake On Modem



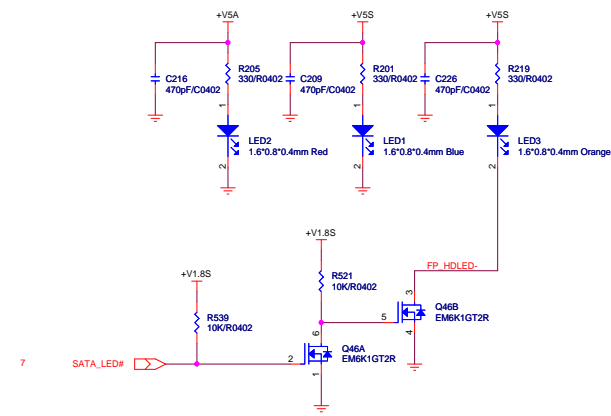
## Reset Circuit



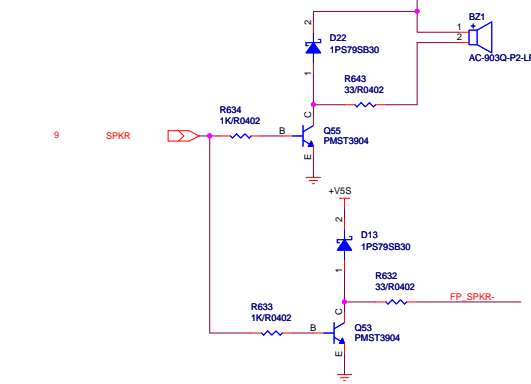
## Mounting Holes



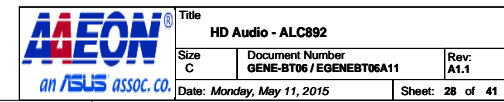
## LED

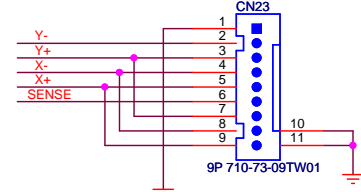
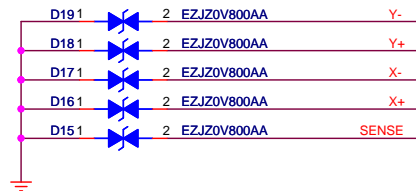
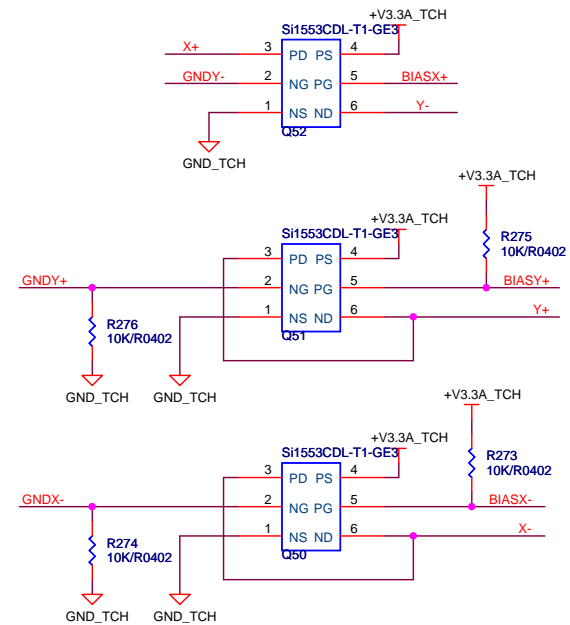
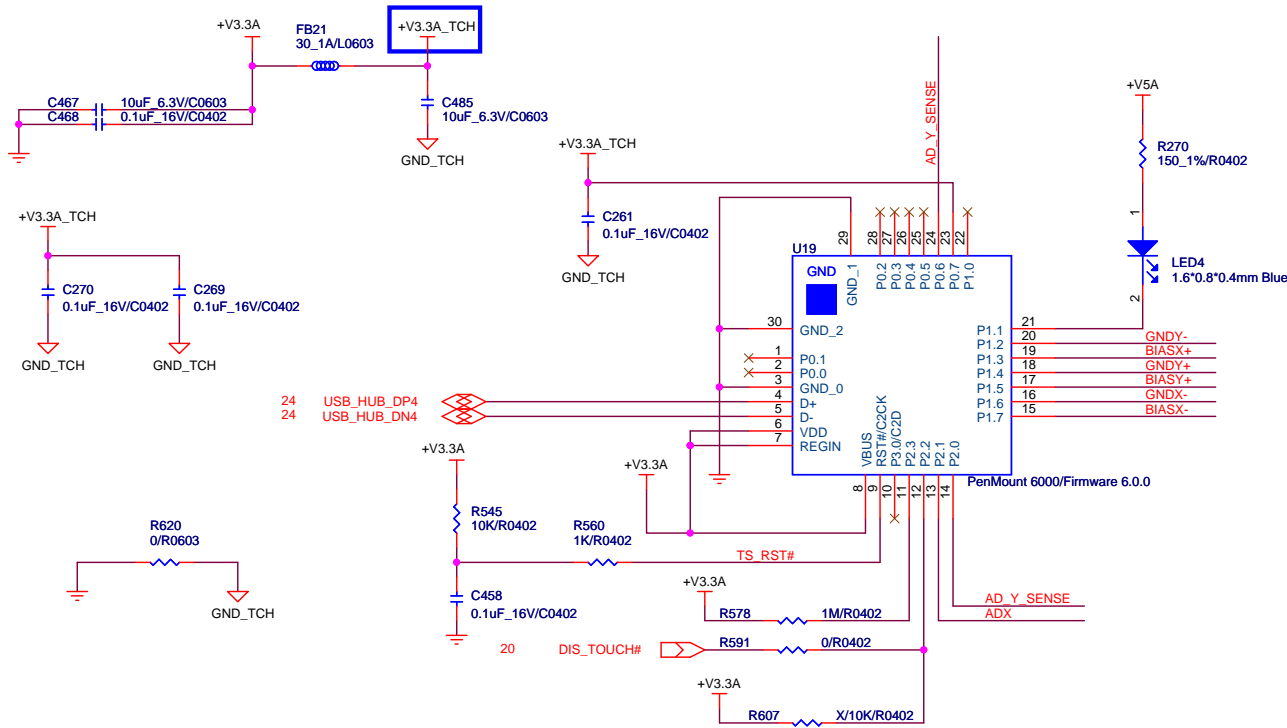


## Speaker

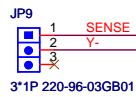






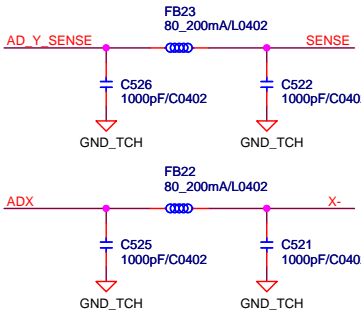


CN	Touch Screen Lines		
	8-Wire	4-Wire	5-Wire
PIN9	Right Sense	N/A	N/A
PIN8	Left Sense	N/A	N/A
PIN7	Bottom Sense	N/A	N/A
PIN6	TOP Sense	N/A	Sense(S)
PIN5	Right Excite	Right	LR(X)
PIN4	Left Excite	Left	LL(L)
PIN3	Bottom Excite	Bottom	UR(H)
PIN2	Top Excite	Top	UL(Y)
PIN1	GND	GND	GND



JP9(1-2)  
200-72-PBGB03

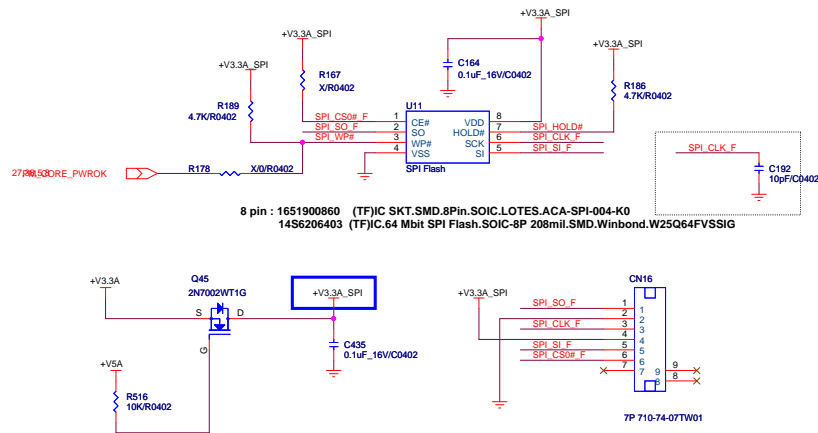
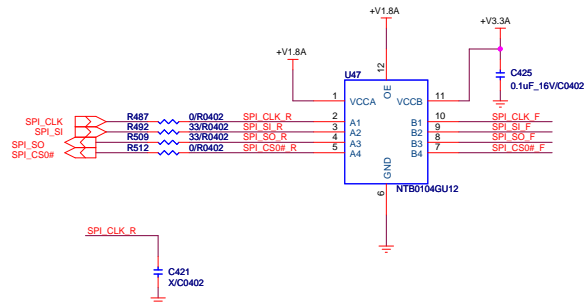
4,5,8 Wire Selection		
1-2	4,8 wire	Default
2-3	5 wire	



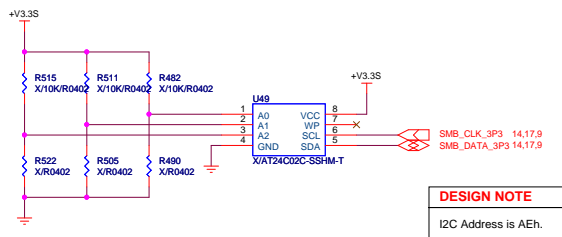
Title <b>Touch Panel</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <b>Monday, May 11, 2015</b>		Sheet: <b>29 of 41</b>



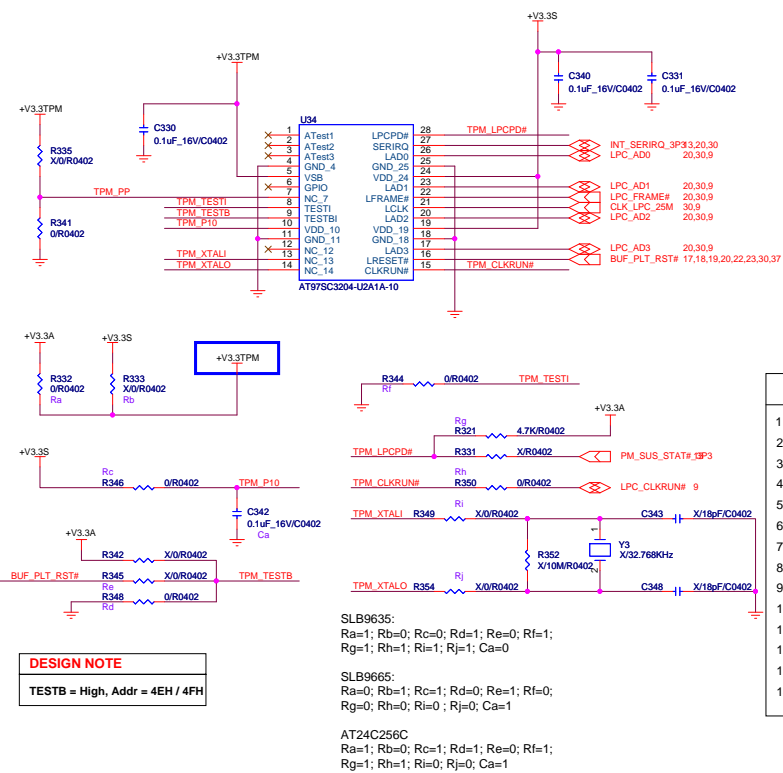
## SPI BIOS



## CMOS Backup

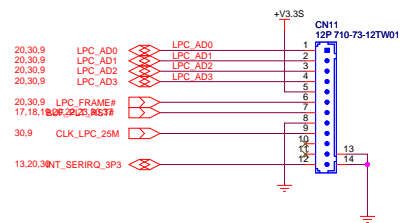


## TPM



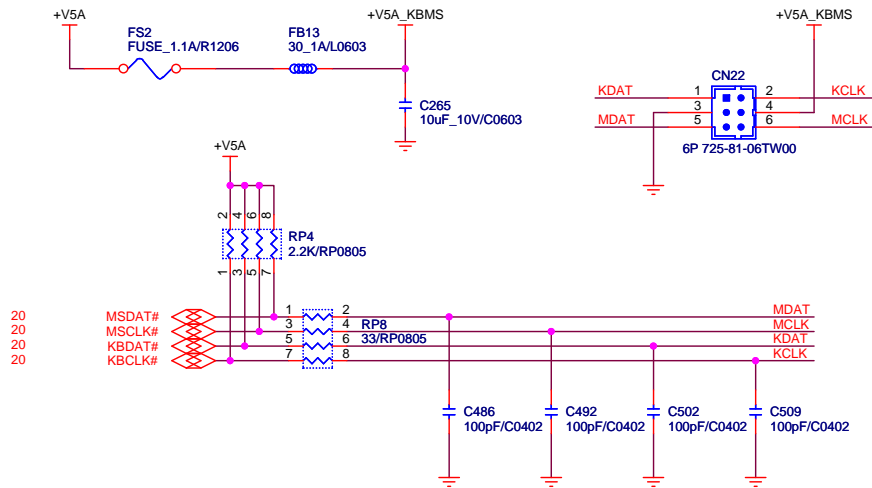
PIN		AT24C256C	
1	15	A <b>Test</b>	LPCPD#
2	16	A <b>Test</b>	SERIRQ
3	17	A <b>Test</b>	LAD0
4	18	GND	GND
5	19	V <b>SB</b>	VDD
6	20	GPIO	LAD1
7	21	NC	LFRAME#
8	22	T <b>ESTI</b>	LCLK
9	23	T <b>ESTB</b>	LAD2
10	24	VDD	VDD
11	25	GND	GND
12	26	NC	LAD3
13	27	NC	LRESET#
14	28	NC	CLKRUN#

## LPC Connector

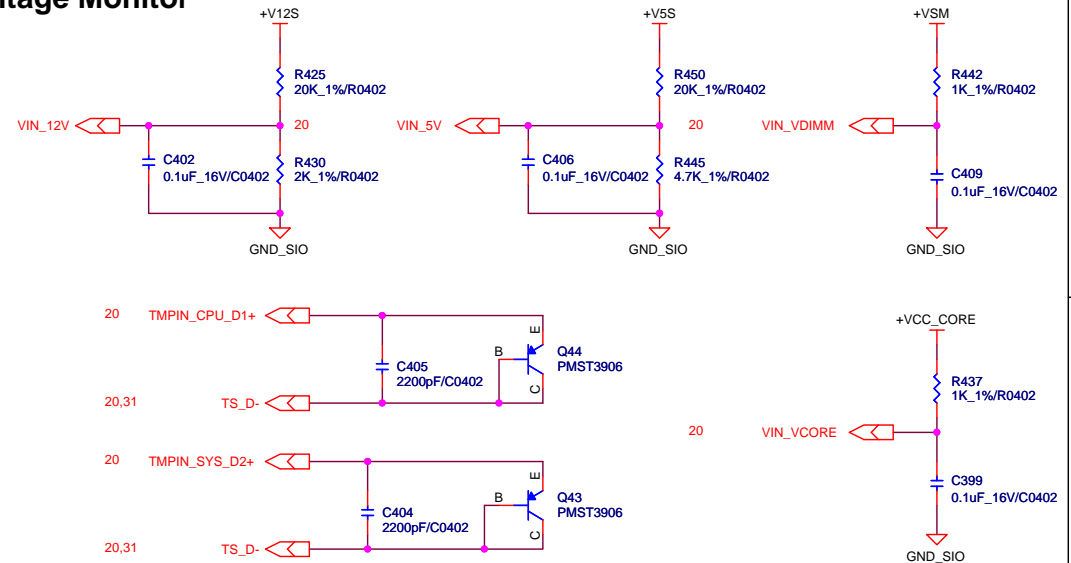


PIN		SLB9665			
1	15	NC	LPCPD#	NC	NC
2	16	GPIO2	SERIRQ	NC	SERIRQ
3	17	NC	LAD0	NC	LAD0
4	18	GND	GND	GND	GND
5	19	VS <sub>B</sub>	VDD	VDD	VDD
6	20	GPIO	LAD1	GPIO	LAD1
7	21	PP	LFRAME#	PP	LFRAME#
8	22	TESTI	LCLK	NC	LCLK
9	23	TESTB	LAD2	LRESET#	LAD2
10	24	NC	VDD	VDD	VDD
11	25	GND	GND	GND	GND
12	26	NC	LAD3	NC	LAD3
13	27	XTALI/32KIN	LRESET#	NC	LRESET#
14	28	XTALO	CLKRUN#	NC	NC

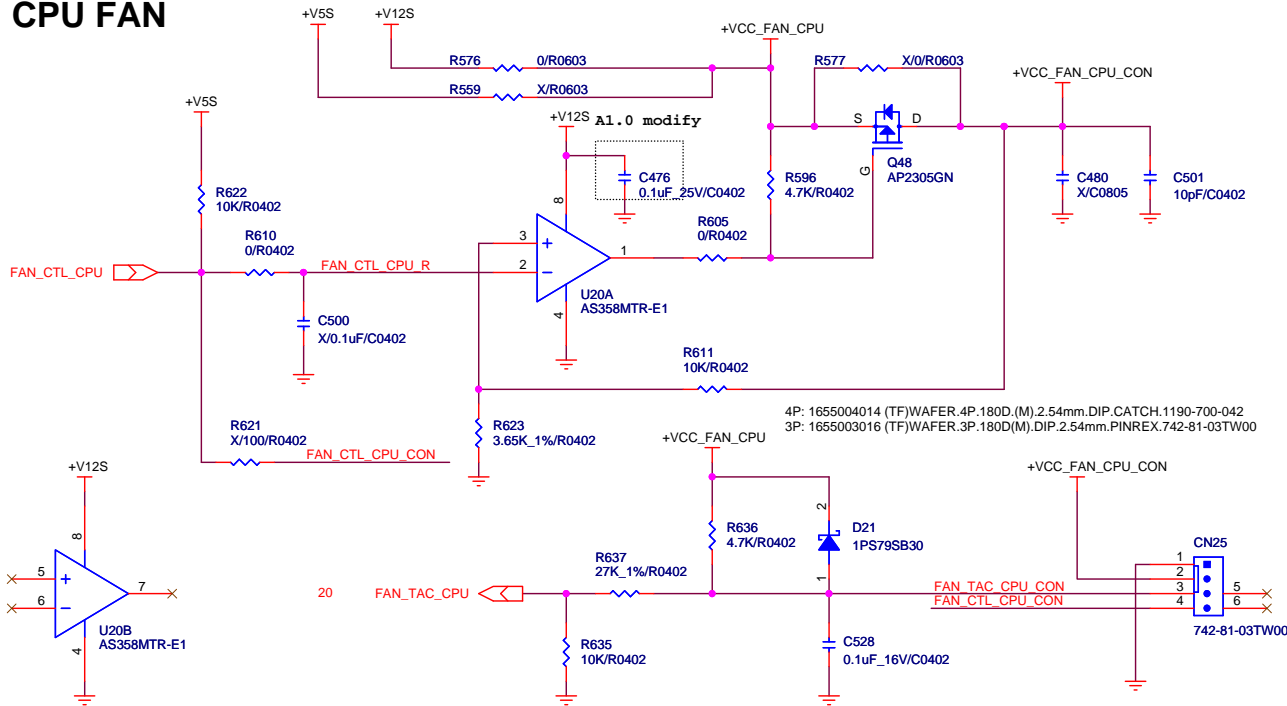
## PS/2 Keyboard/Mouse



## Voltage Monitor

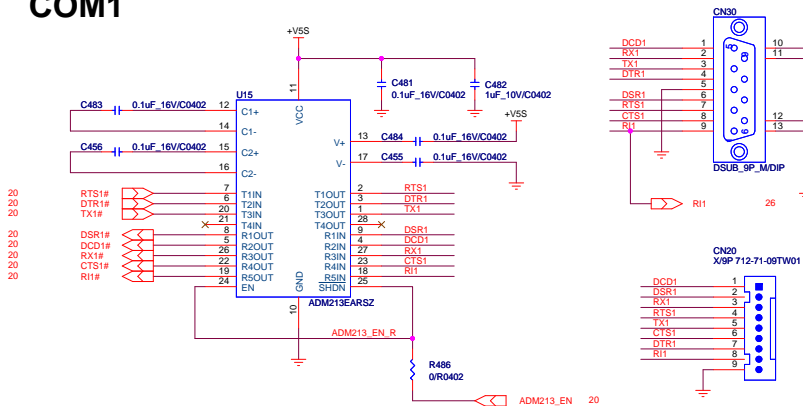


## CPU FAN

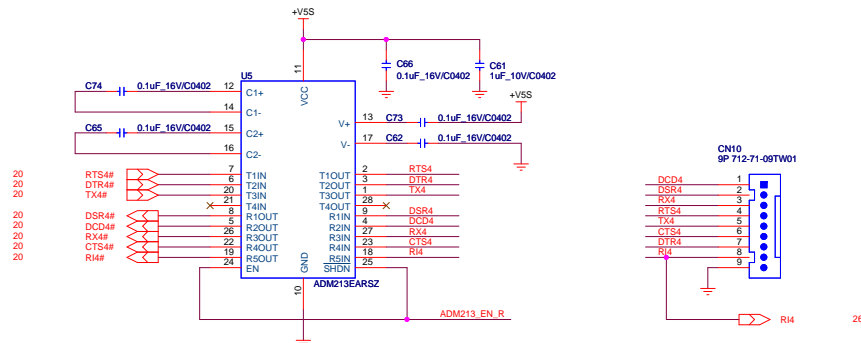


Title <b>KB,MS,H/W Monitor,FAN</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: Monday, May 11, 2015		Sheet: 31 of 41

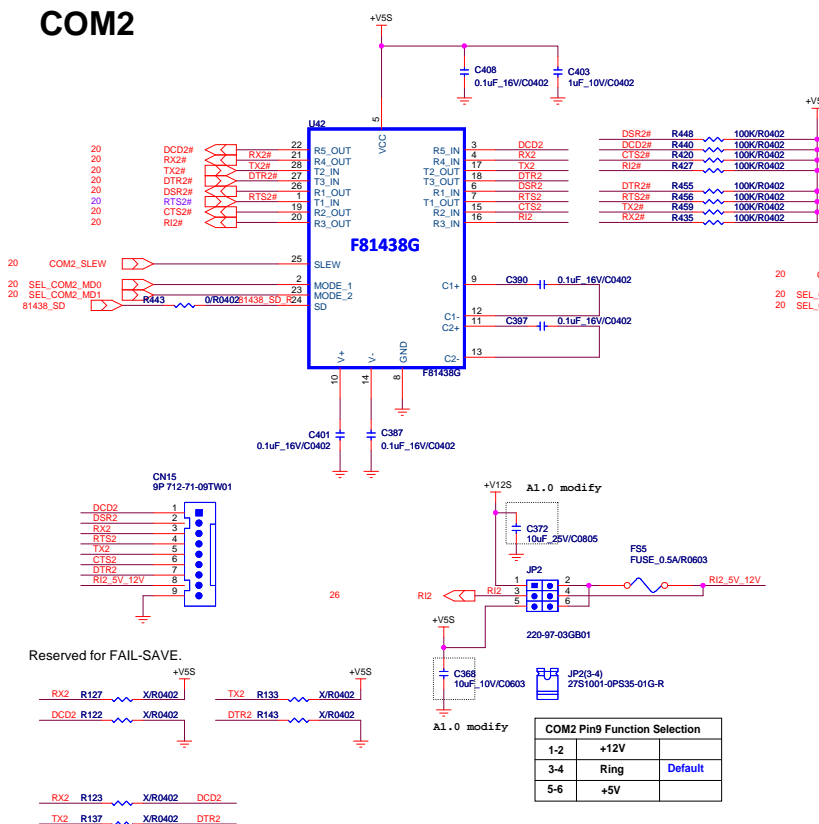
## COM1



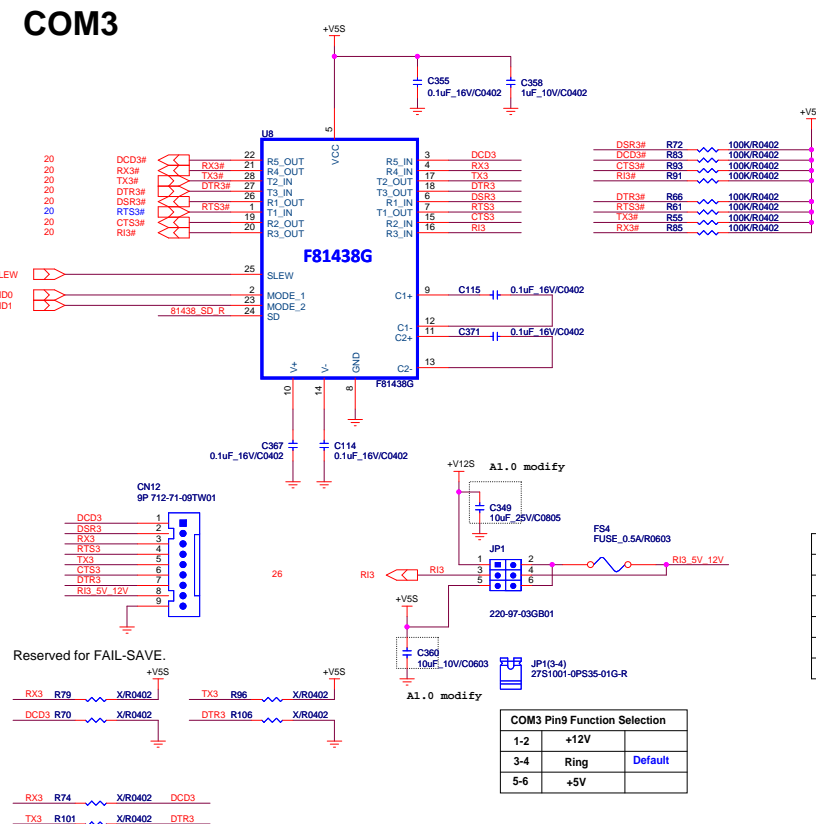
## COM4



## COM2



## COM3



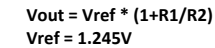
Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

Pin Mapping		
	RS-232	RS-485
R1_IN	DSR	
T1_OUT	RTS	
T2_OUT	TX	RS422_RX+ (A)
T3_OUT	DTR	RS422_RX- (B)
R2_IN	CTS	
R3_IN	RI	
R4_IN	RX	RS485_D+ (A)
R5_IN	DCD	RS485_D- (B)

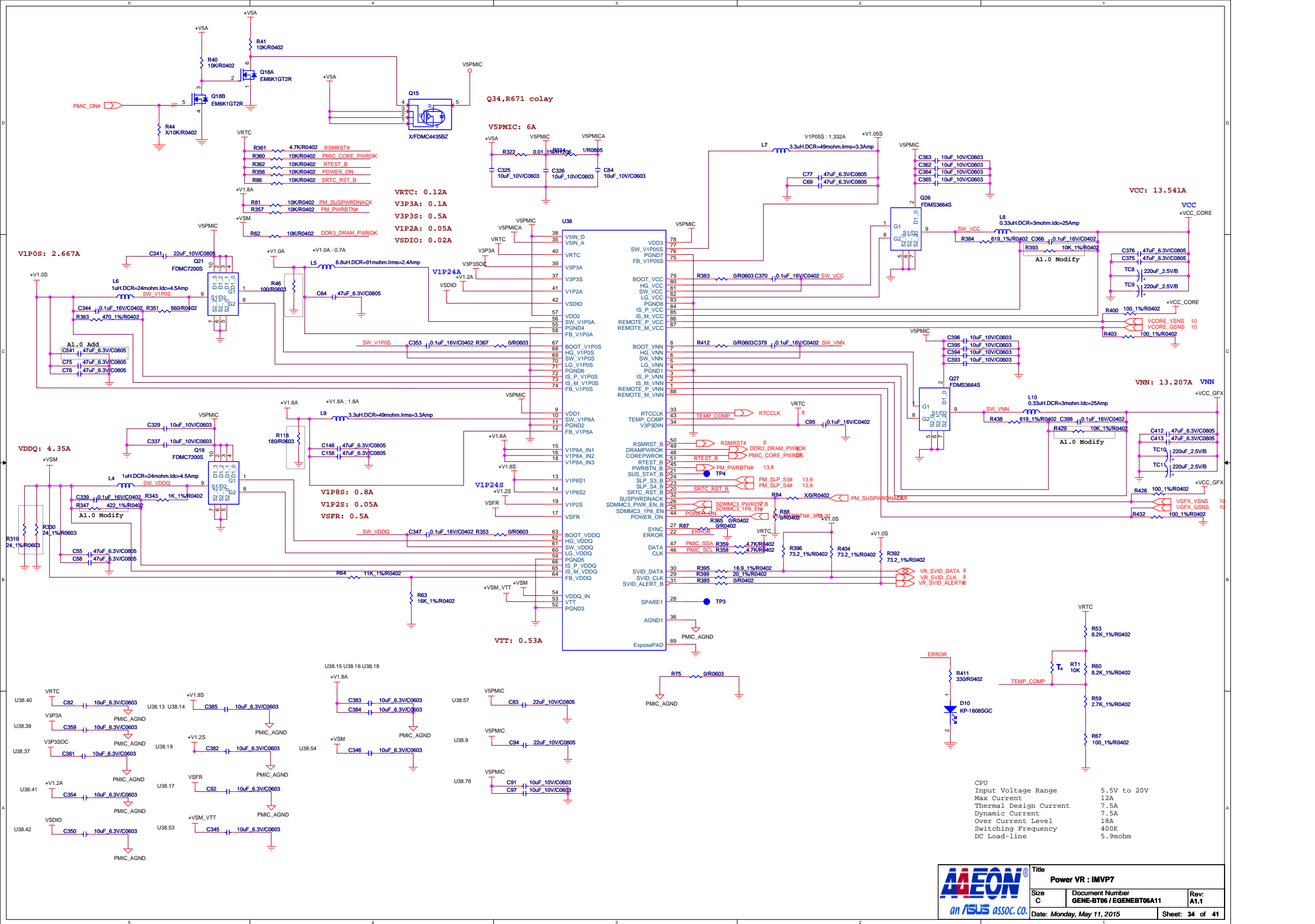
Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

COM3 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

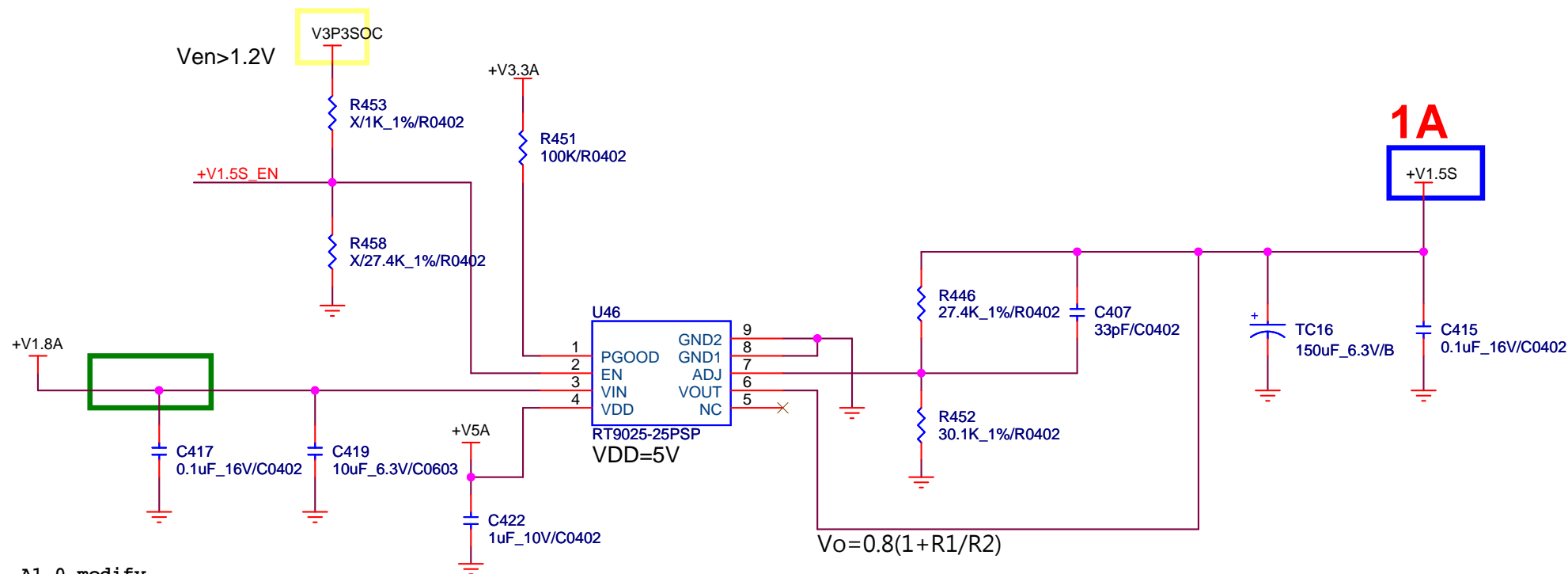
SKIP pin  
VDD = skip mode  
GND = PWM mode



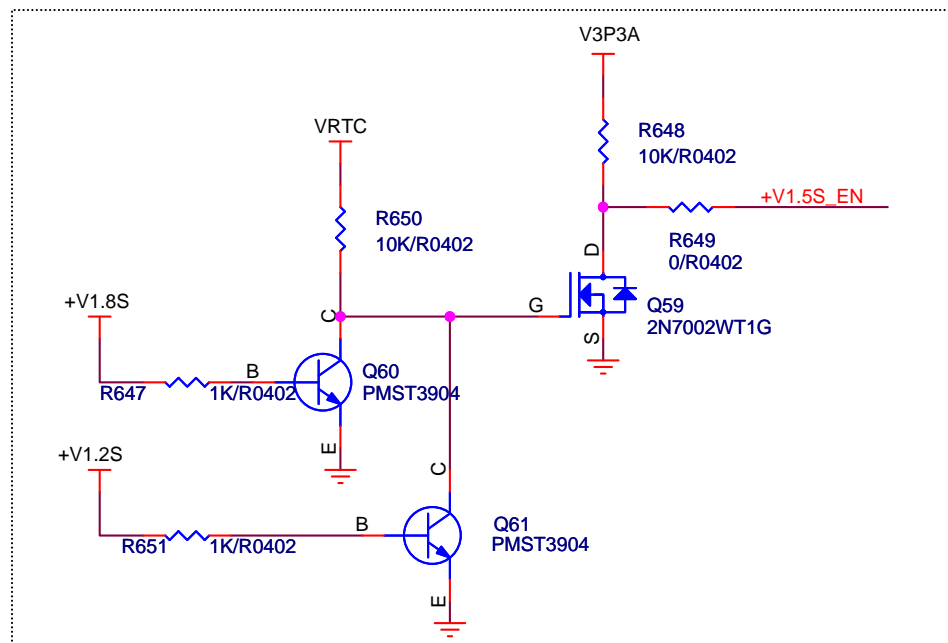
	<b>Title</b> <b>POWER VR : +V12A</b>		
	<b>Size</b> <b>B</b>	<b>Document Number</b> <b>GENE-BT06 / EGENEBT06A11</b>	<b>Rev:</b> <b>A1.1</b>
	<b>Date:</b> <i>Monday, May 11, 2015</i>		<b>Sheet:</b> <b>33</b> of <b>41</b>



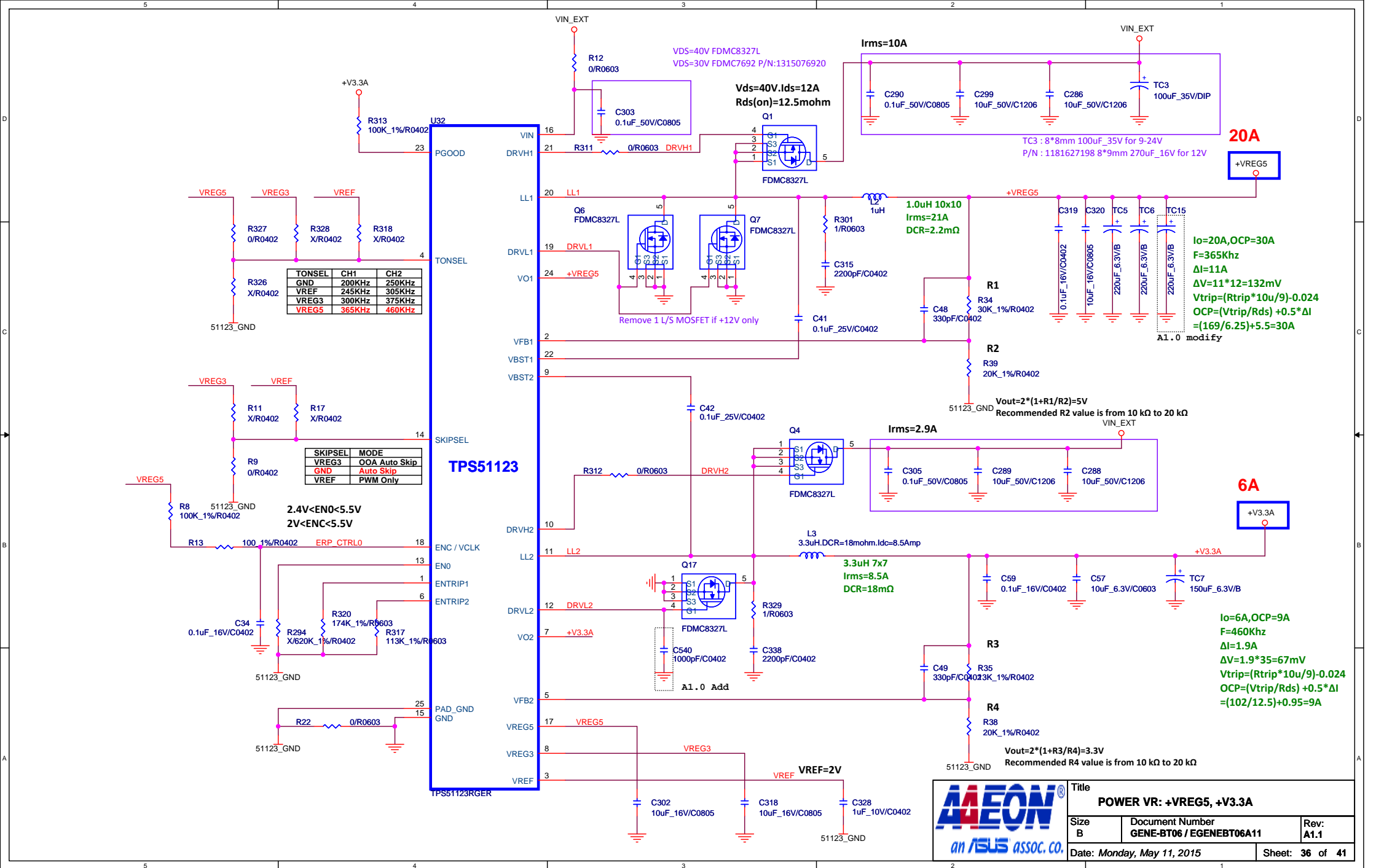
# +V1.5S



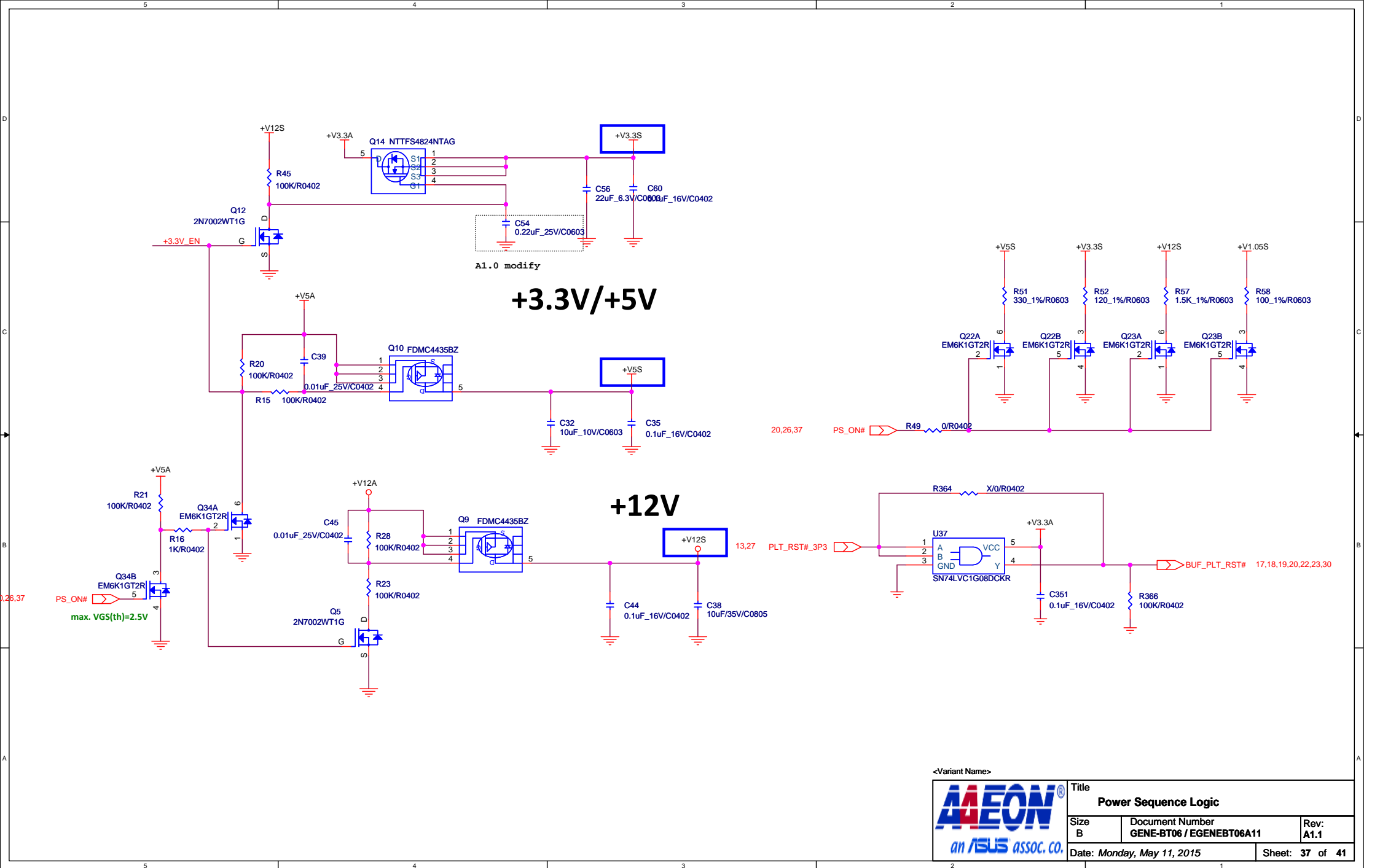
A1.0 modify



Title <b>Power VR : +V1.2A, +V1.5S</b>		
Size A	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <i>Monday, May 11, 2015</i>		Sheet: <b>35</b> of <b>41</b>





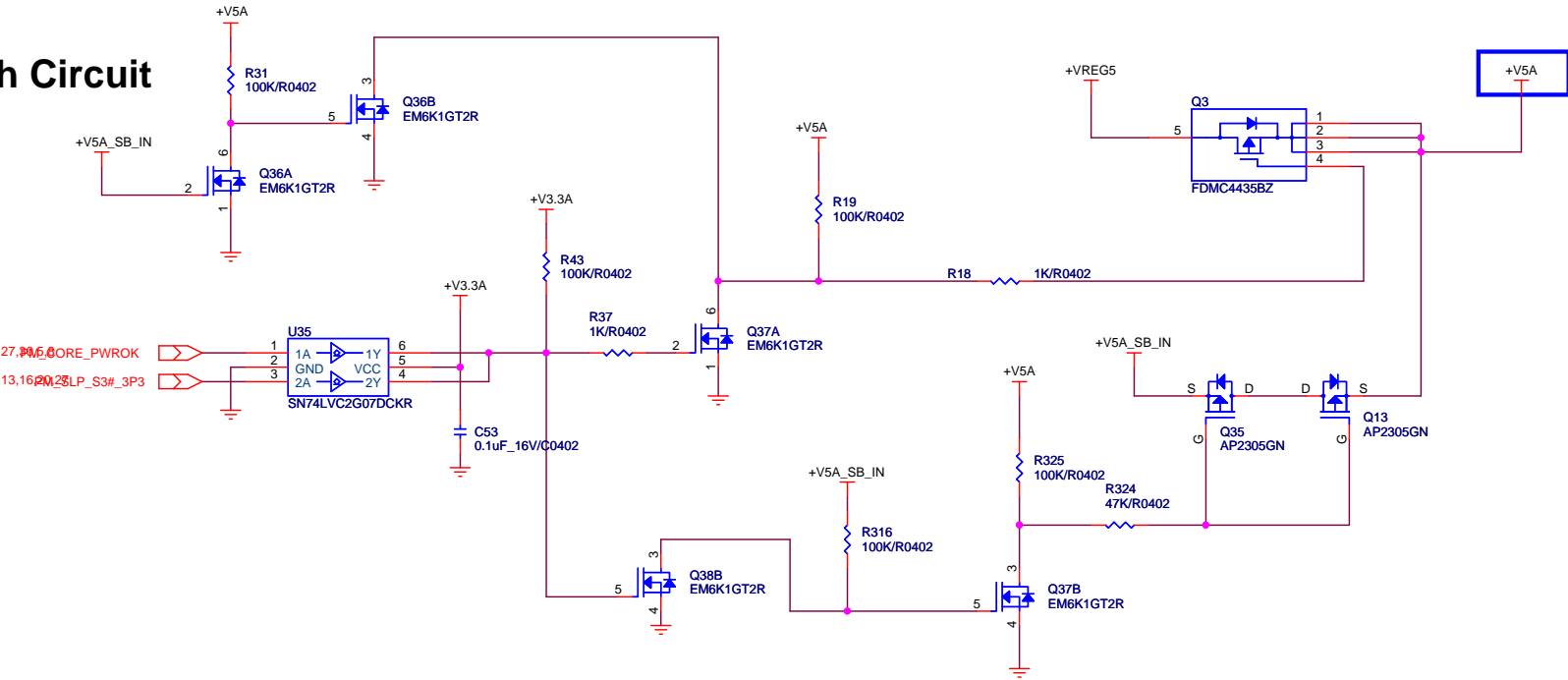


<Variant Name>



Title <b>Power Sequence Logic</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <b>Monday, May 11, 2015</b>		Sheet: <b>37 of 41</b>

# 5VDAUL Switch Circuit



Title <b>Standby Power</b>		
Size B	Document Number <b>GENE-BT06 / EGENEBT06A11</b>	Rev: <b>A1.1</b>
Date: <i>Monday, May 11, 2015</i>		Sheet: <b>38</b> of <b>41</b>


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



Title Backup		
Size B	Document Number GENE-BT06 / EGENEBT06A11	Rev: A1.1
Date: Monday, May 11, 2015		Sheet: 39 of 40

HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2014/X/XX	A0.1	First Release.		Daniel	



an ASUS assoc. co.

Title

Revision History

Size  
B

Document Number  
GENE-BT06 / EGENEBT06A11

Rev:  
A1.1

Date: Monday, May 11, 2015

Sheet: 40 of 40