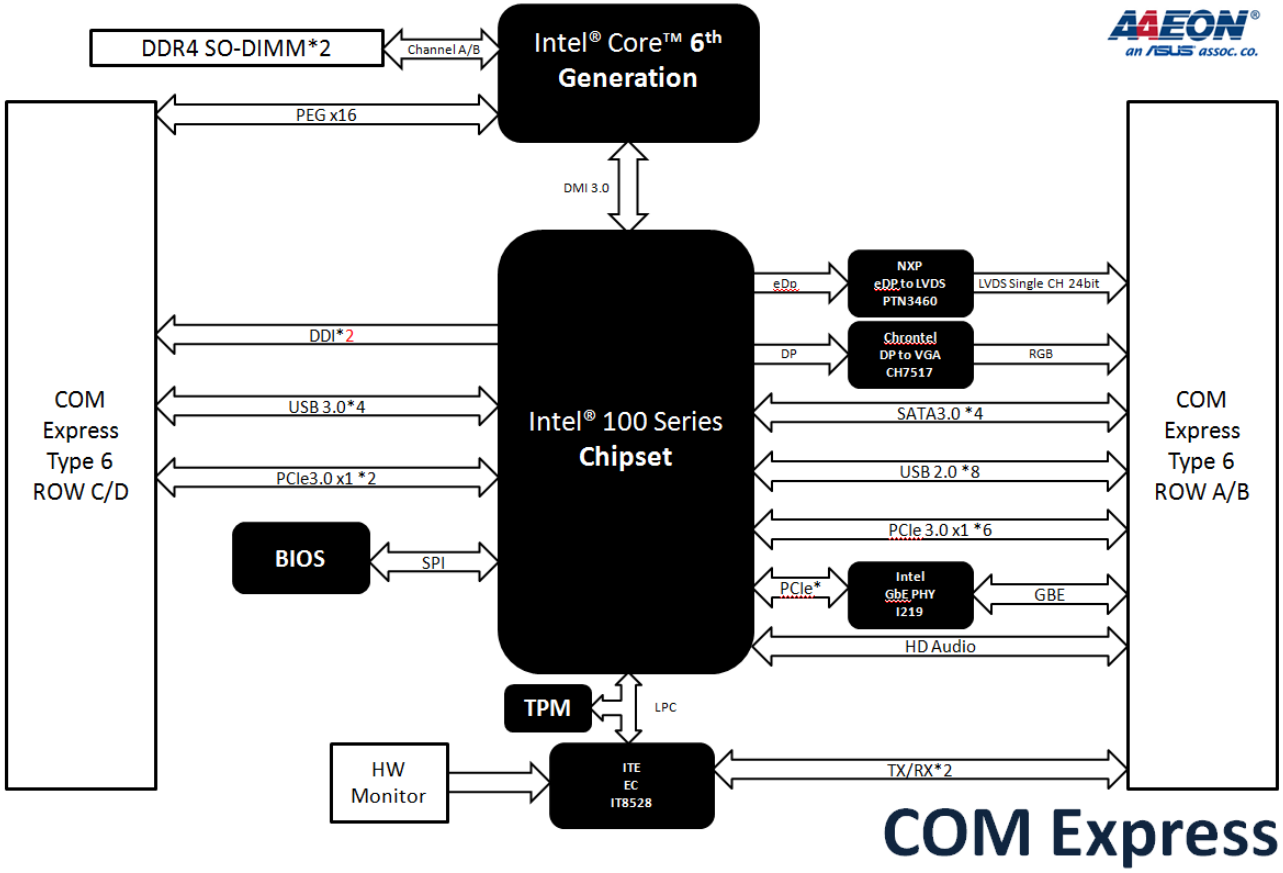
COM-SKH Rev. A0.1 BLOCK DIAGRAM



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AAEON an ASUS assoc. co.

Title: System Setting

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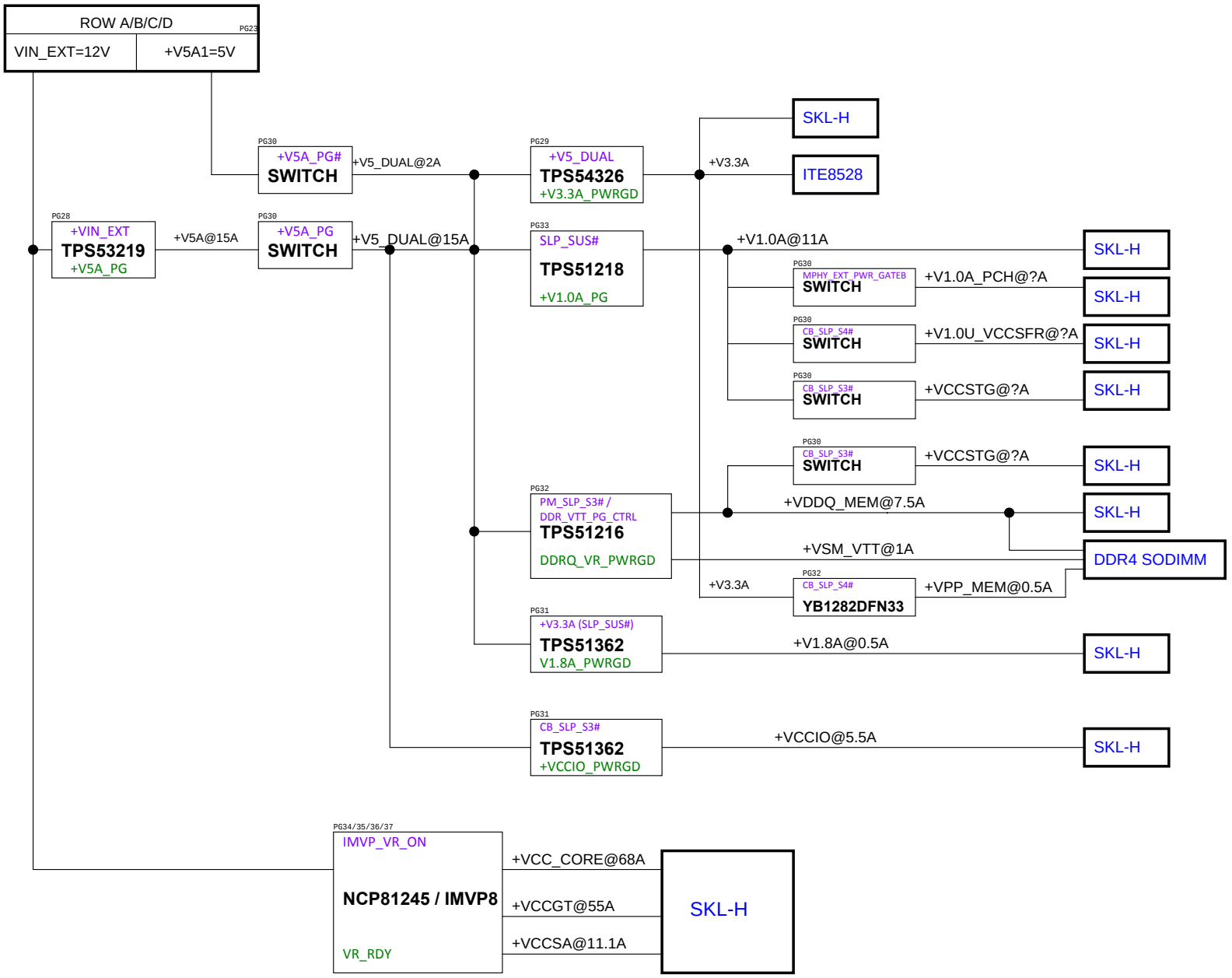

AAEON an ASUS assoc. co.	Title: **POWER MAP**	
Size: A	Document Number: **COM-SKH**	Rev: **A0.1**
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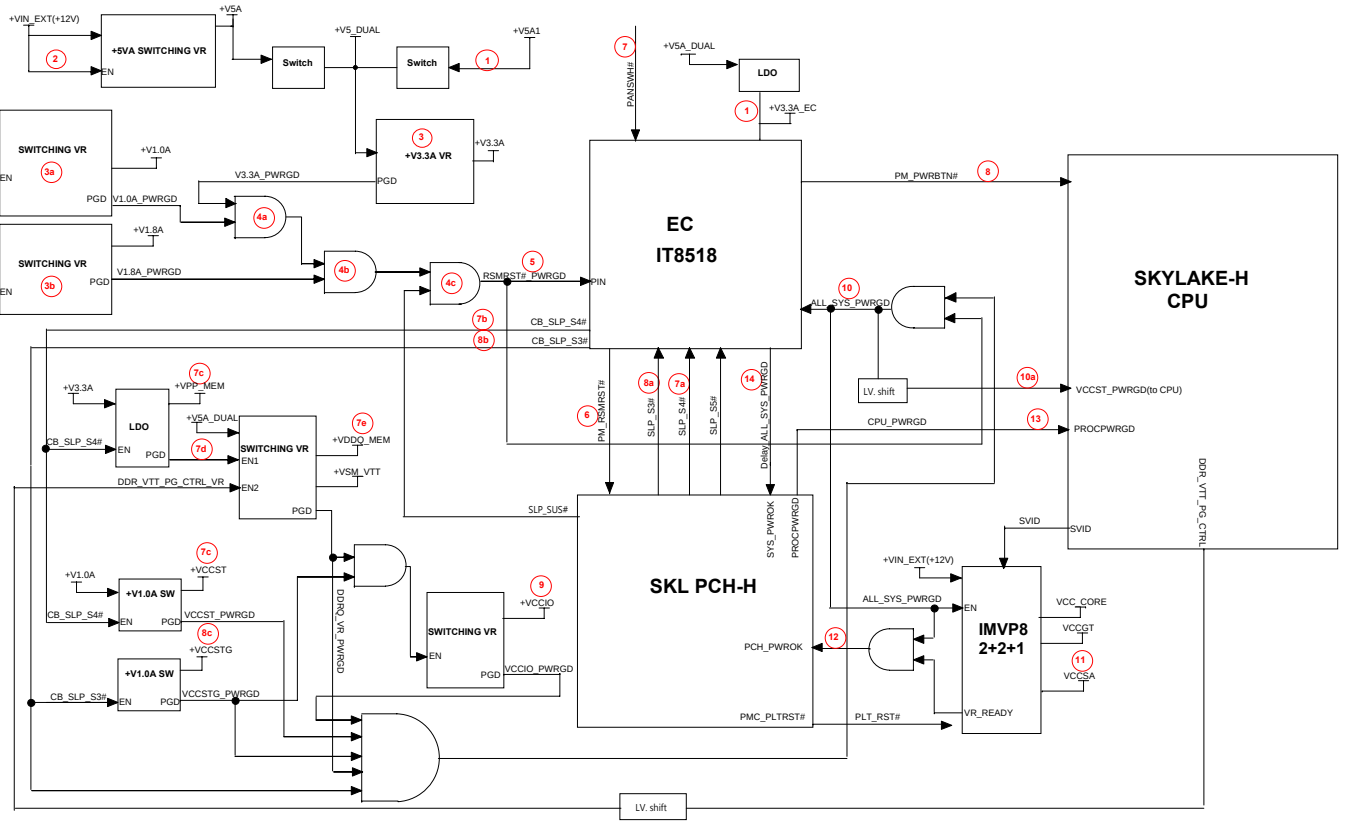

AAEON an ASUS assoc. co.	Title: Power Sequence		
	Size: C	Document Number: COM-SKH	Rev: A0.1
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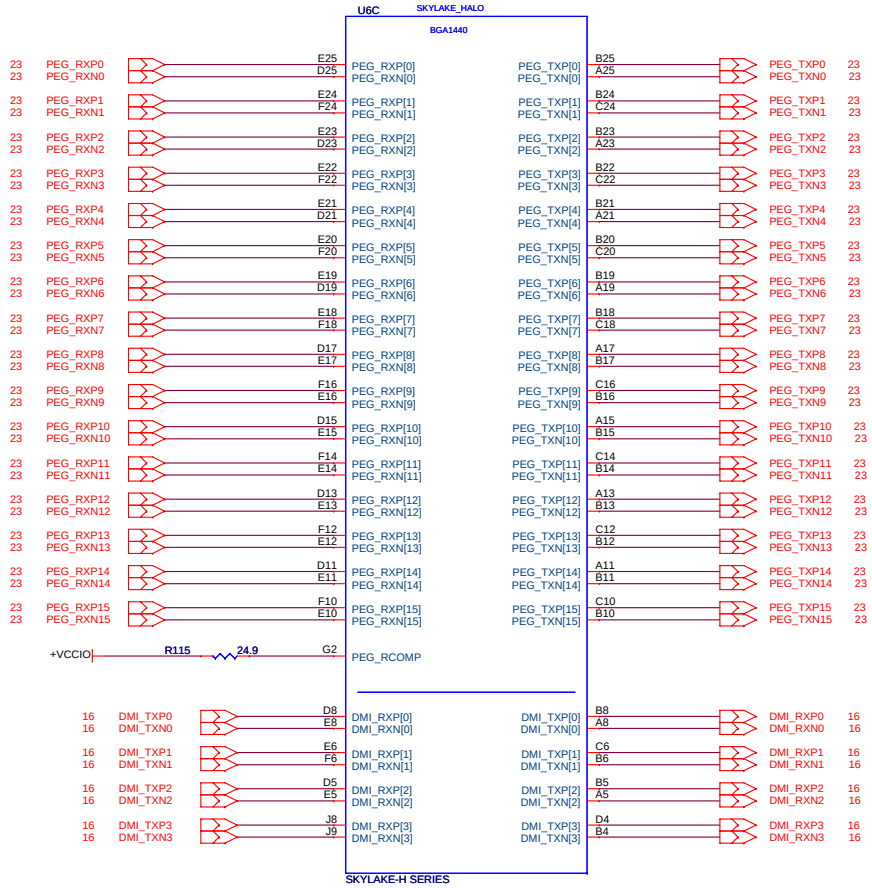
SKYLAKE-H BGA PROCESSOR(DMI/PEG)



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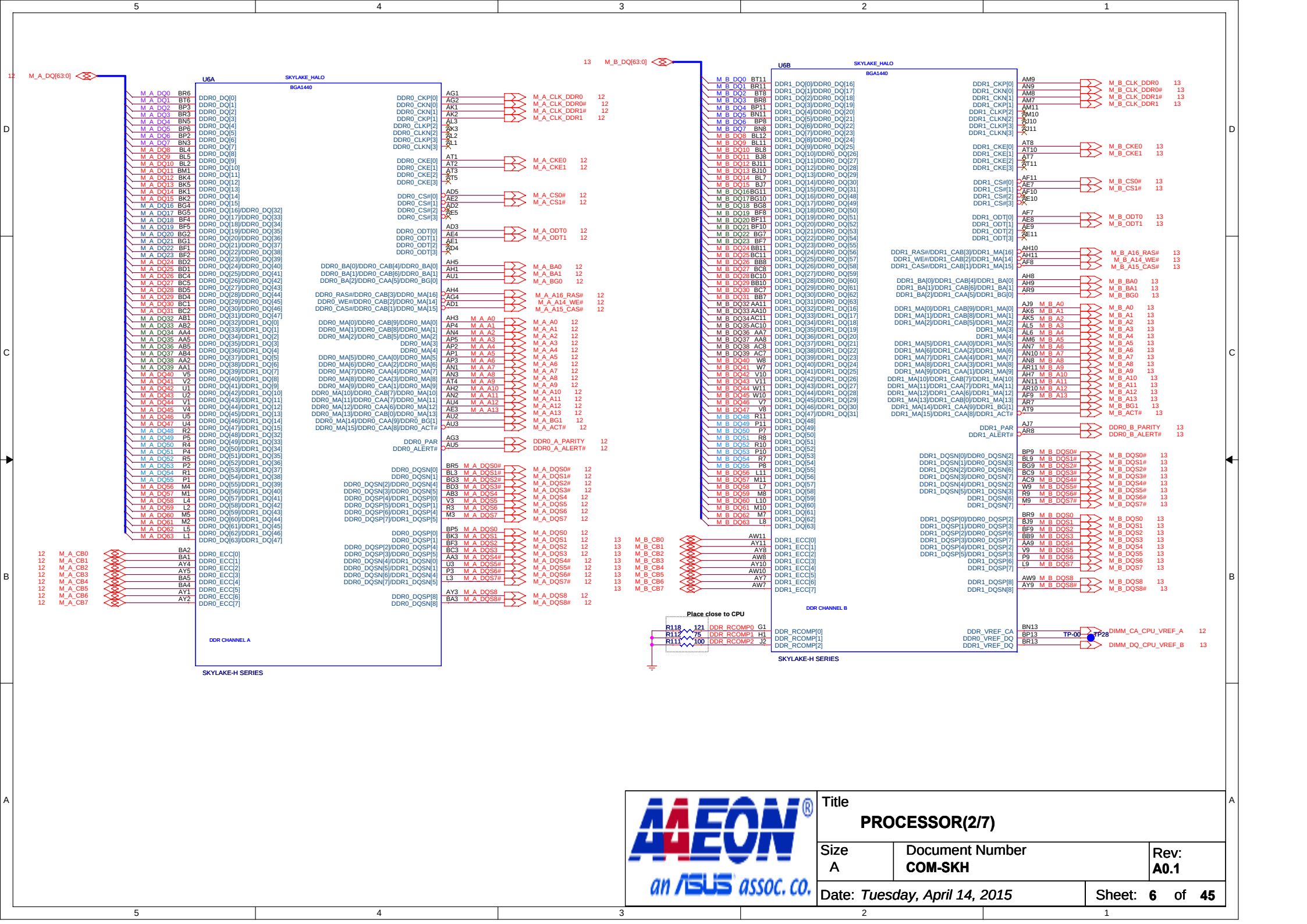

AAEON an ASUS assoc. co.	Title: **PROCESSOR(2/7)**	
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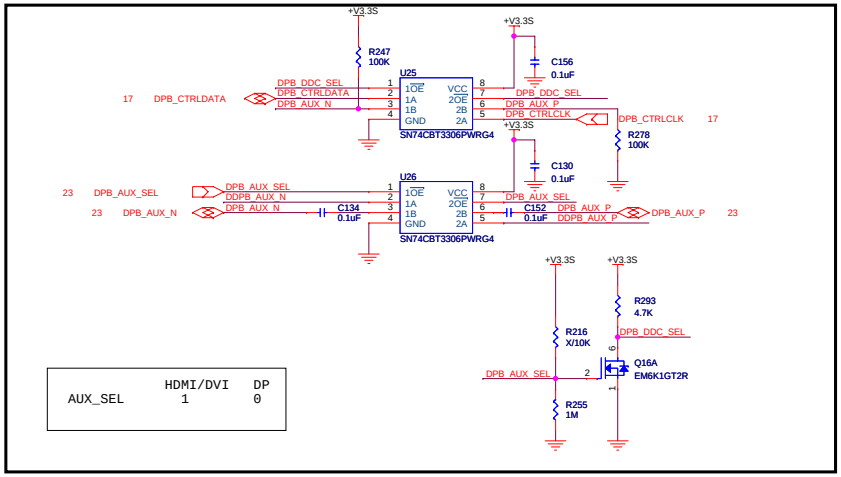
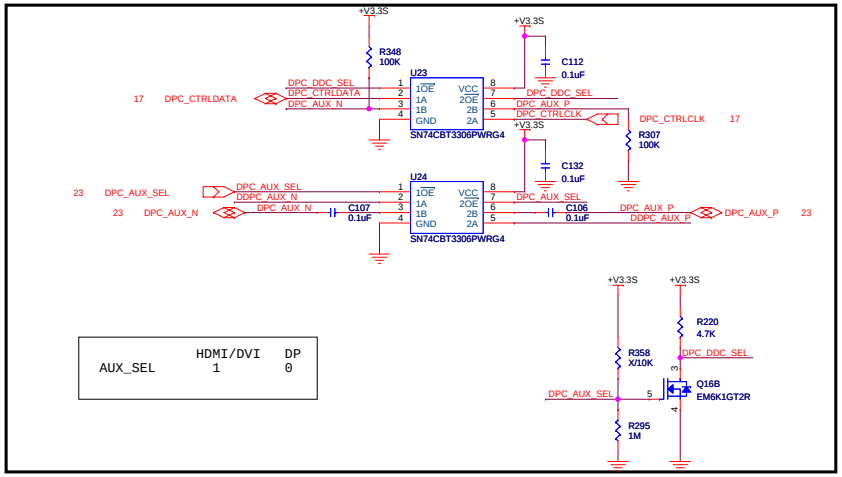
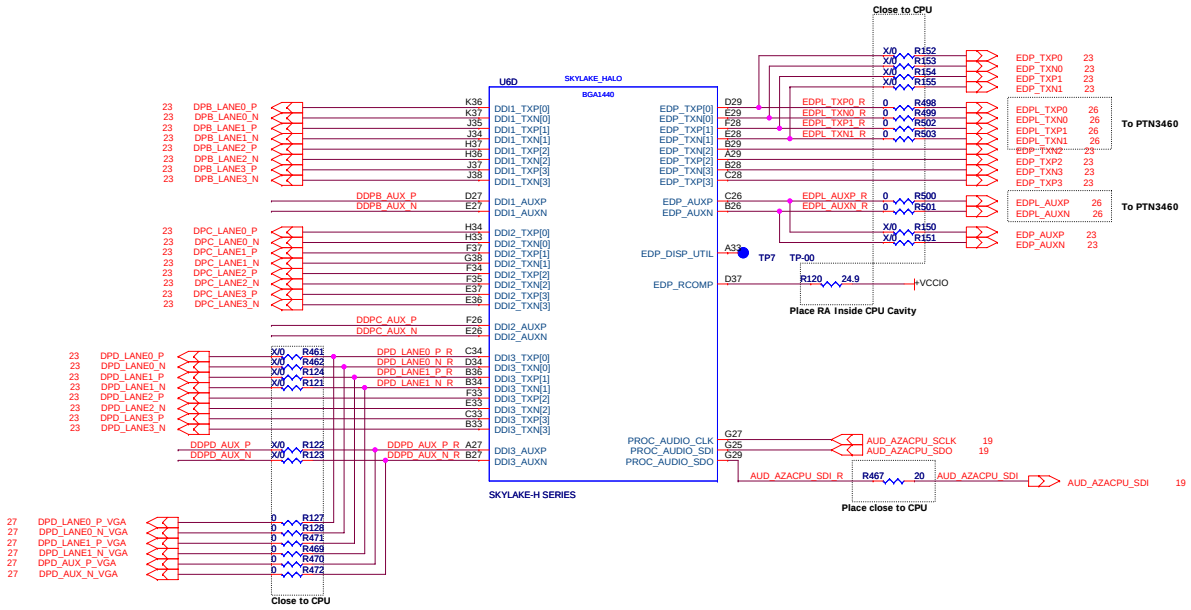
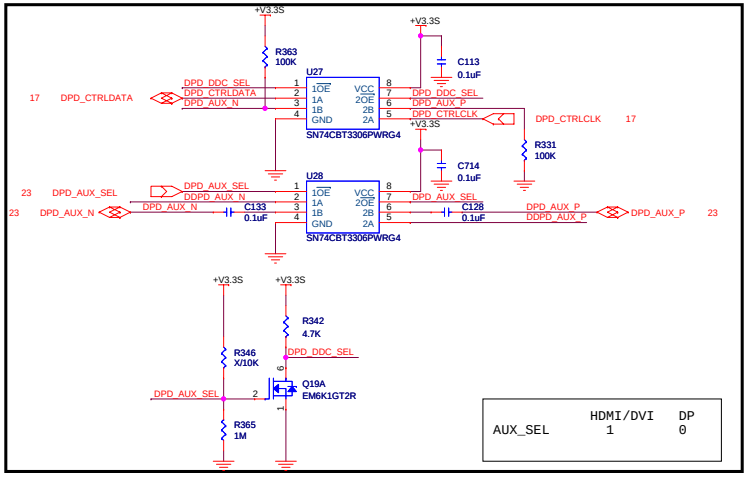

+V3.3S
R247
100K
U25
SN74CBT3306PWRG4
C156
0.1uF
DPB_DDC_SEL
DPB_CTRLDATA
DPB_AUX_N
DPB_AUX_P
DPB_CTRLCLK
17
DPB_CTRLDATA
R278
100K
C130
0.1uF
U26
SN74CBT3306PWRG4
23
DPB_AUX_SEL
DPB_AUX_N
C134
0.1uF
C152
0.1uF
DPB_AUX_P
23
R293
4.7K
R216
X/10K
Q16A
EM6K1GT2R
R255
1M
AUX_SEL
HDMI/DVI
DP
1
0

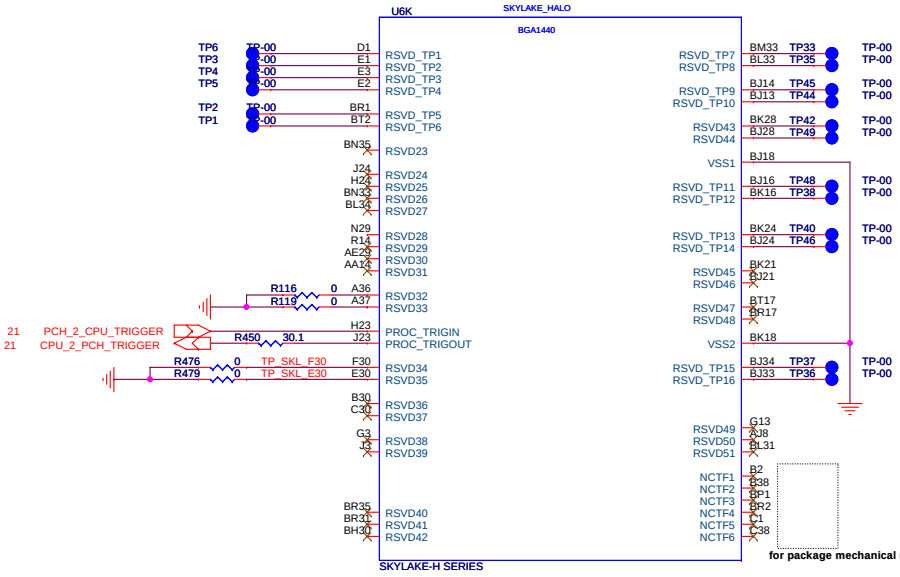

+V3.3S
R348
100K
U23
SN74CBT3306PWRG4
C112
0.1uF
DPC_DDC_SEL
DPC_CTRLDATA
DPC_AUX_N
DPC_AUX_P
DPC_CTRLCLK
17
DPC_CTRLDATA
R307
100K
C132
0.1uF
U24
SN74CBT3306PWRG4
23
DPC_AUX_SEL
DPC_AUX_N
C107
0.1uF
C106
0.1uF
DPC_AUX_P
23
R220
4.7K
R358
X/10K
Q16B
EM6K1GT2R
R295
1M
AUX_SEL
HDMI/DVI
DP
1
0

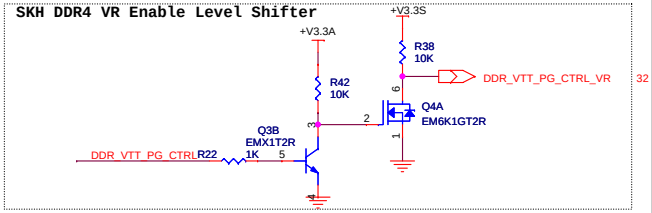

Close to CPU
U6D
SKYLAKE_HALO
BGA1440
SKYLAKE-H SERIES
DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]
DDI1_AUXP
DDI1_AUXN
DDI2_TXP[0]
DDI2_TXN[0]
DDI2_TXP[1]
DDI2_TXN[1]
DDI2_TXP[2]
DDI2_TXN[2]
DDI2_TXP[3]
DDI2_TXN[3]
DDI2_AUXP
DDI2_AUXN
DDI3_TXP[0]
DDI3_TXN[0]
DDI3_TXP[1]
DDI3_TXN[1]
DDI3_TXP[2]
DDI3_TXN[2]
DDI3_TXP[3]
DDI3_TXN[3]
DDI3_AUXP
DDI3_AUXN
EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXP[2]
EDP_TXN[2]
EDP_TXP[3]
EDP_TXN[3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
EDP_RCOMP
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
EDPL_TXP0_R
EDPL_TXN0_R
EDPL_TXP1_R
EDPL_TXN1_R
EDPL_AUXP_R
EDPL_AUXN_R
To PTN3460
TP7
TP-00
R120
24.9
+VCCIO
Place RA Inside CPU Cavity
AUD_AZACPU_SCLK
AUD_AZACPU_SDO
AUD_AZACPU_SDI_R
R467
20
AUD_AZACPU_SDI
Place close to CPU
DPD_LANE0_P_R
DPD_LANE0_N_R
DPD_LANE1_P_R
DPD_LANE1_N_R
DDPD_AUX_P_R
DDPD_AUX_N_R
Close to CPU

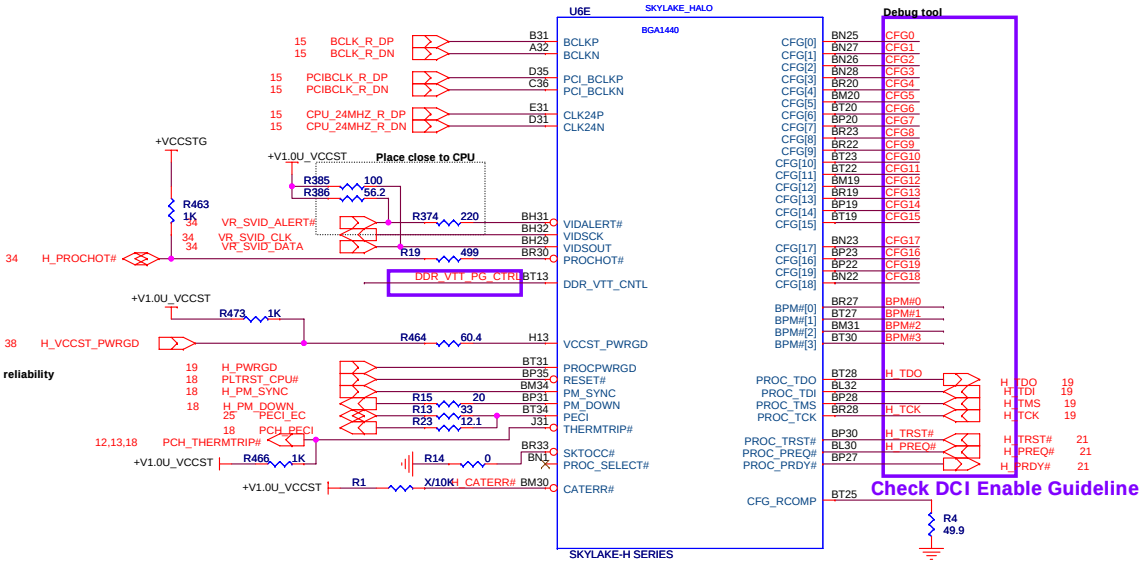

+V3.3S
R363
100K
U27
SN74CBT3306PWRG4
C113
0.1uF
DPD_DDC_SEL
DPD_CTRLDATA
DPD_AUX_N
DPD_AUX_P
DPD_CTRLCLK
17
DPD_CTRLDATA
R331
100K
C714
0.1uF
U28
SN74CBT3306PWRG4
23
DPD_AUX_SEL
DPD_AUX_N
C133
0.1uF
C128
0.1uF
DPD_AUX_P
23
R342
4.7K
R346
X/10K
Q19A
EM6K1GT2R
R365
1M
AUX_SEL
HDMI/DVI
DP
1
0

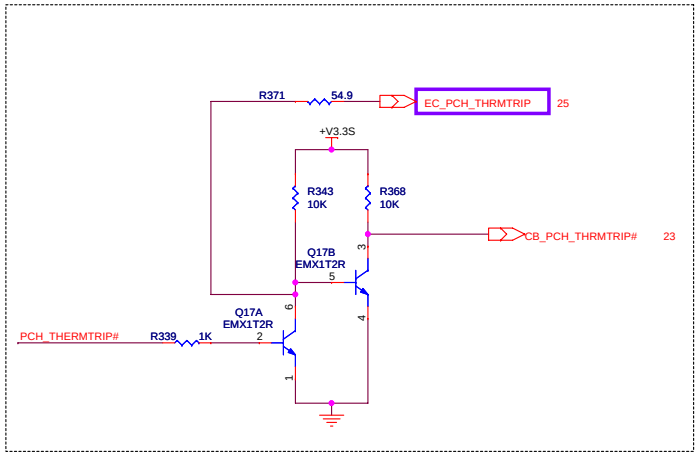
GND, RSVD, and NCTF Signals

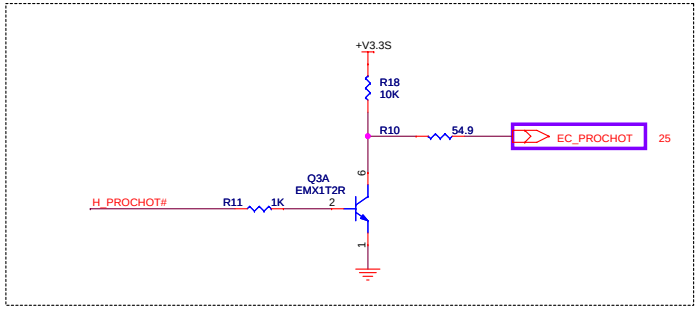
Signal Name	Description
Vss	Processor ground node
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.

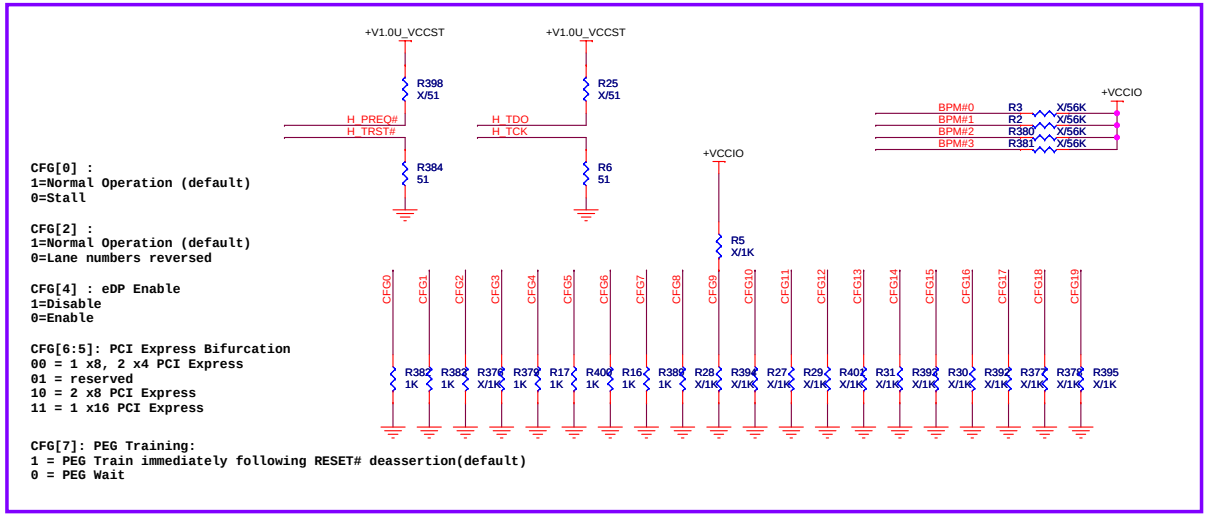












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Title
PROCESSOR(3/7)

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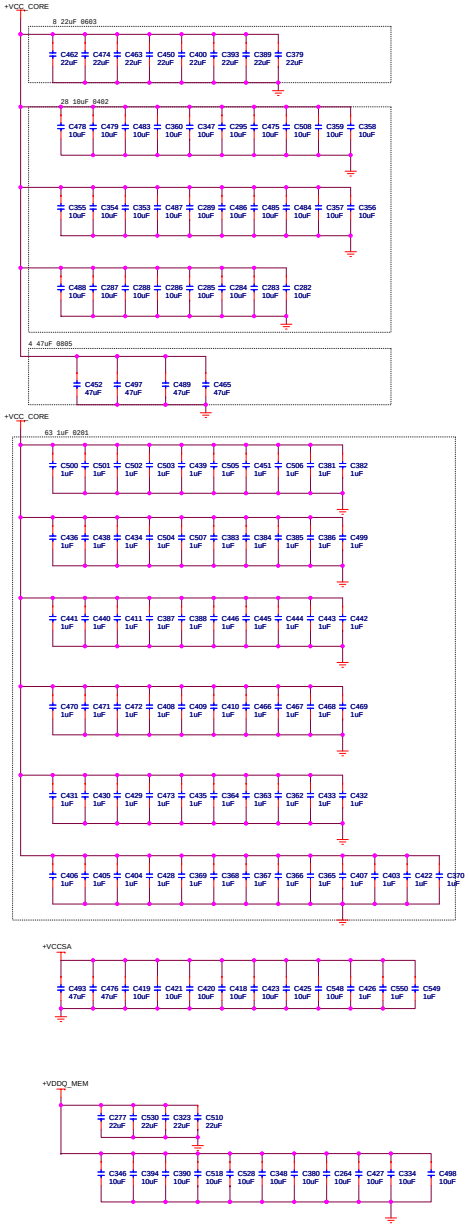
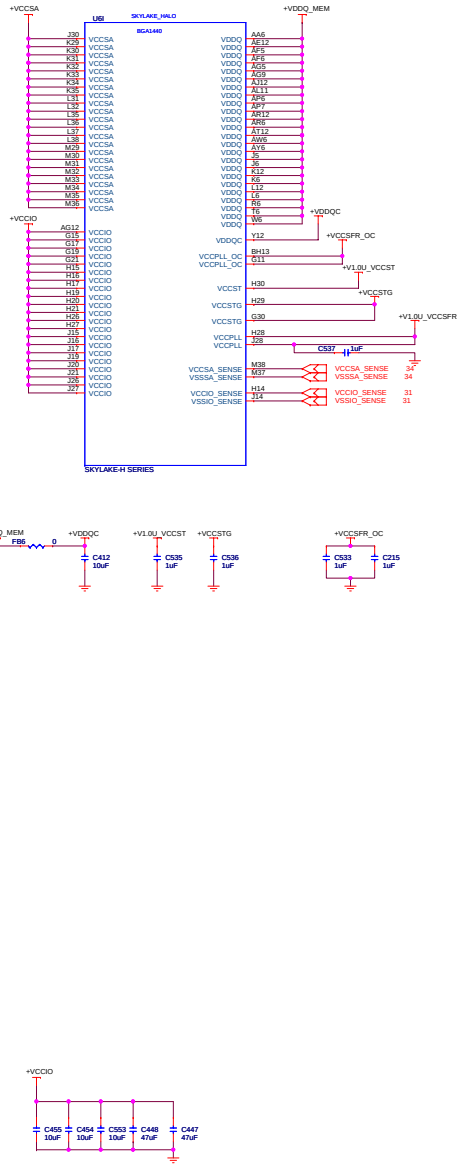
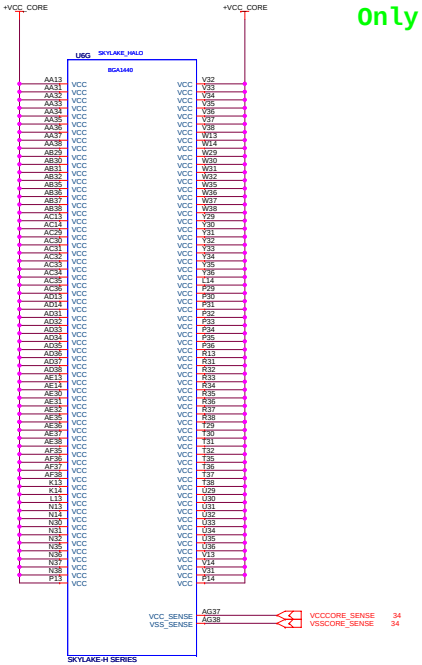
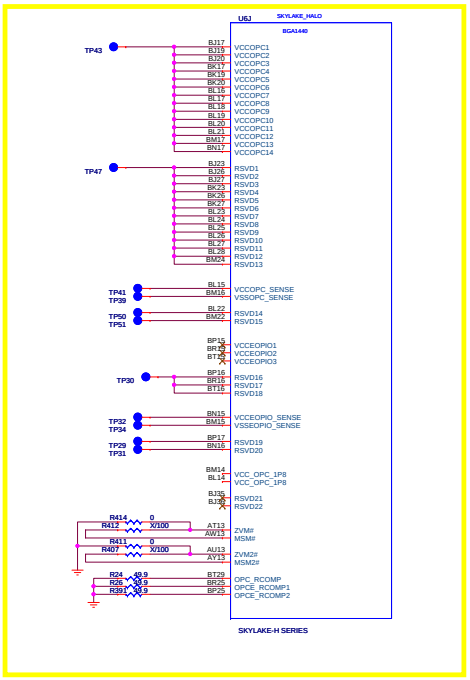






Only Support CPU SKUs without OPC in COM-SKH



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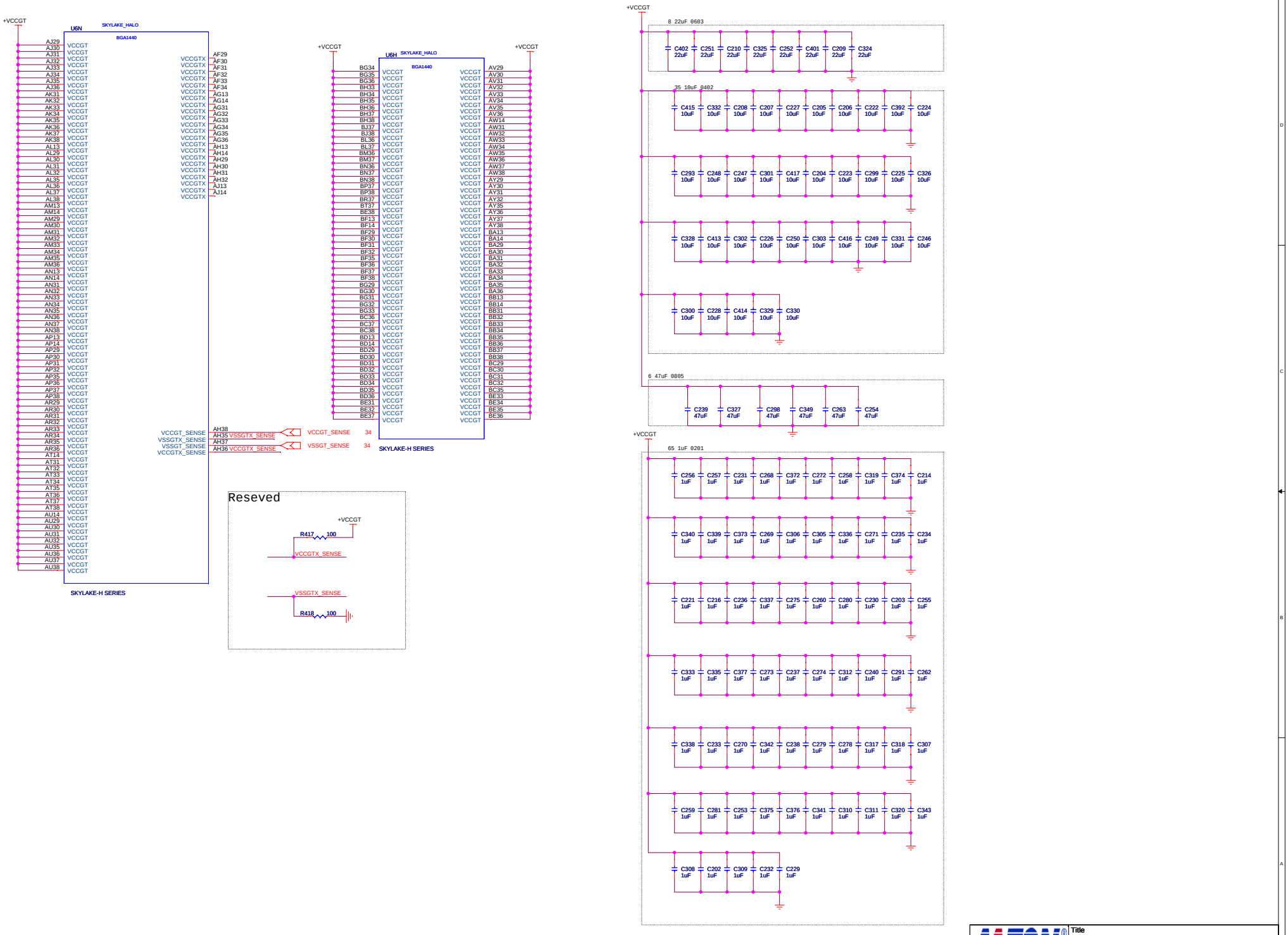

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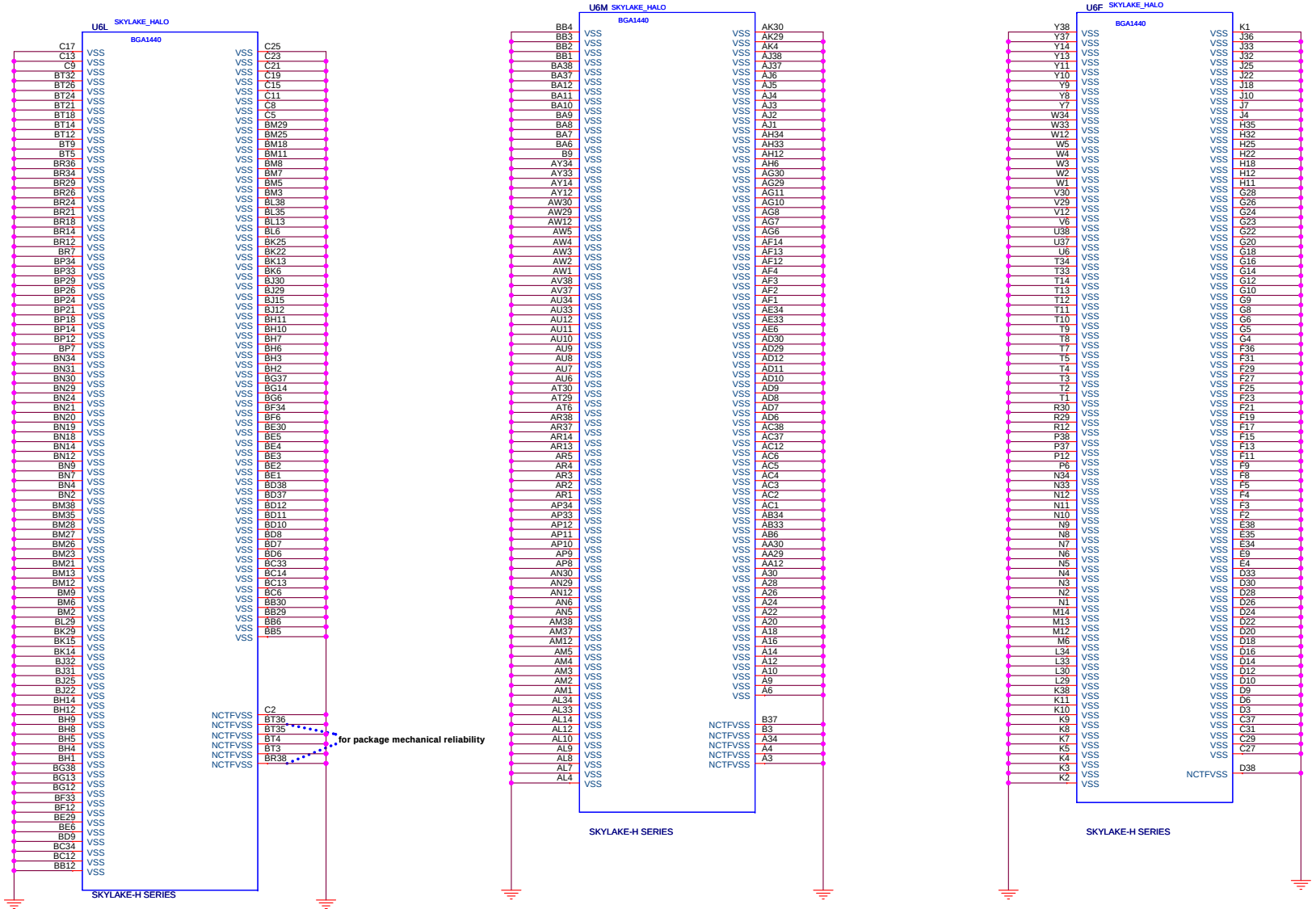

AAEON an ASUS assoc. co.	Title: **PROCESSOR(7/7)**	
Size: A	Document Number: **COM-SKH**	Rev: **A0.1**
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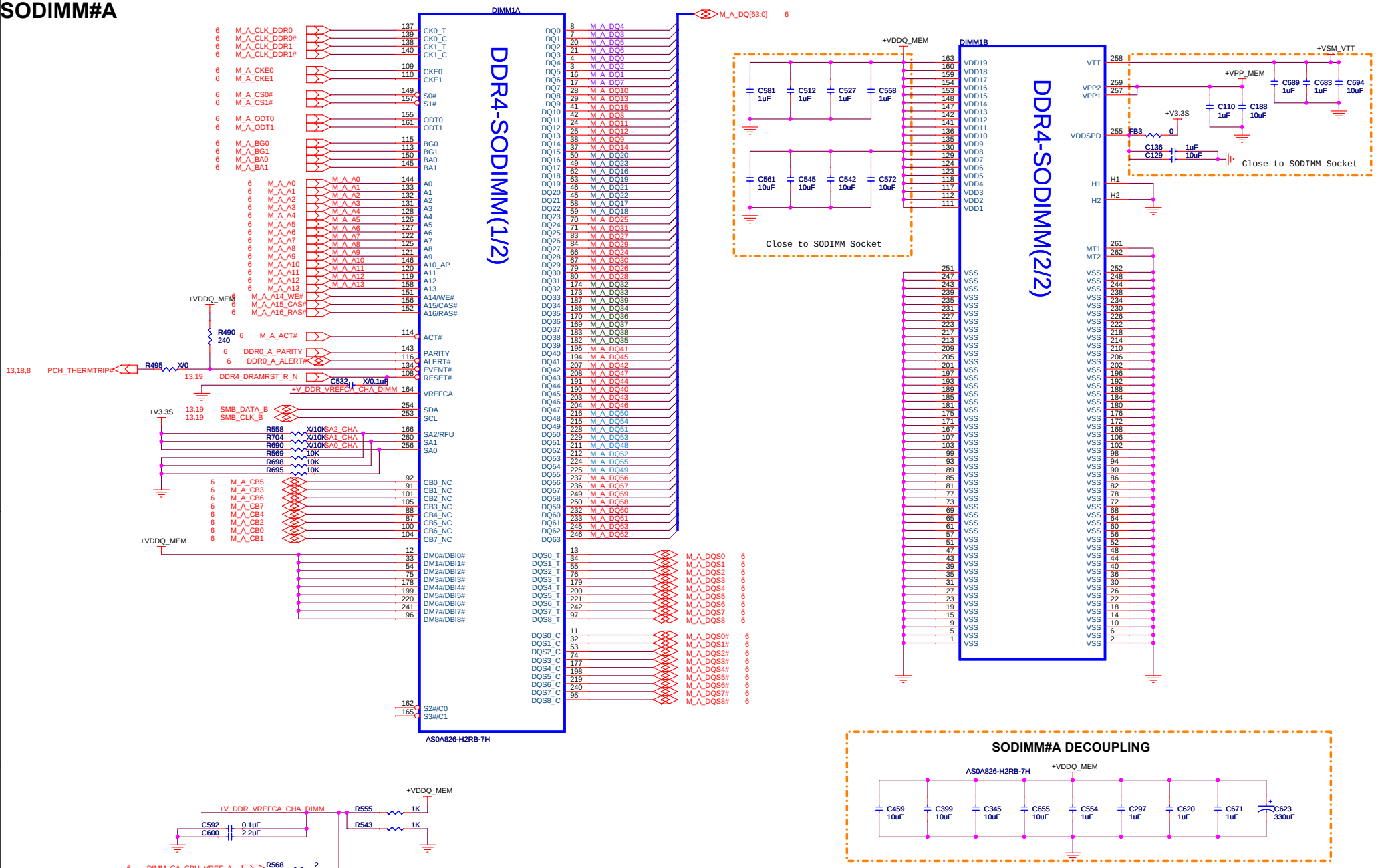
SODIMM#A



SODIMM#A DECOUPLING

AAEON an ASUS assoc. co.	Title: **DDR4 SO-DIMM-A**	
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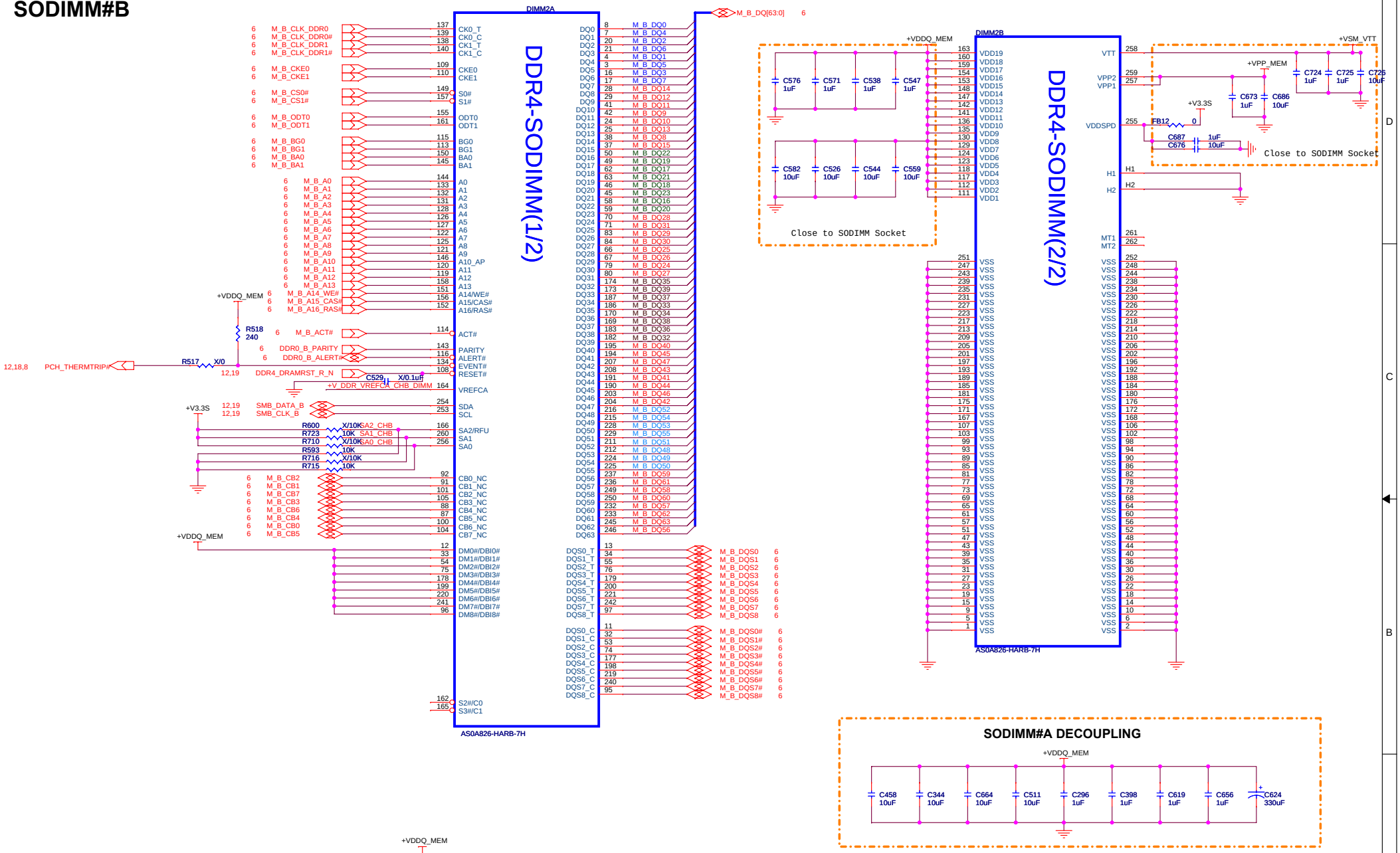
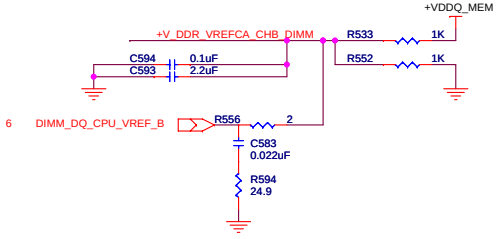
SODIMM#B





Title: **DDR4 SO-DIMM-B**		
Size: A	Document Number: **COM-SKH**	Rev: **A0.1**
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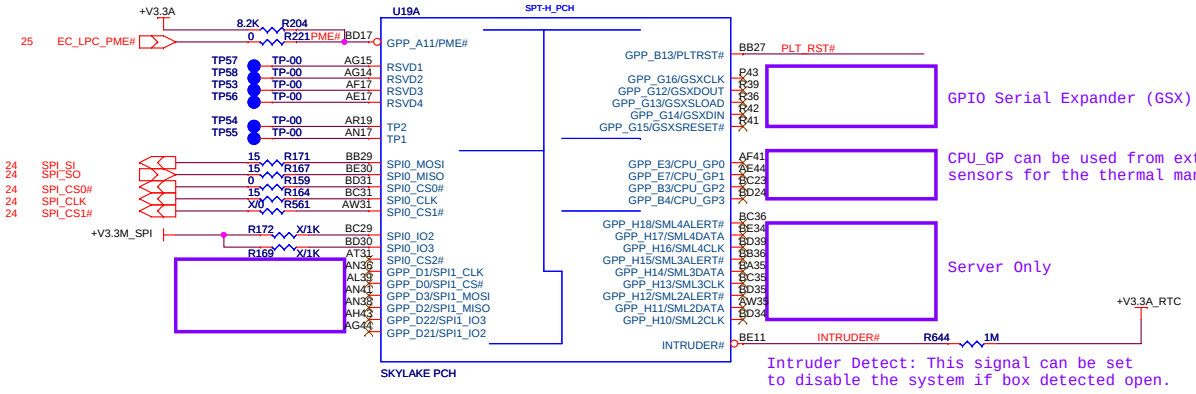

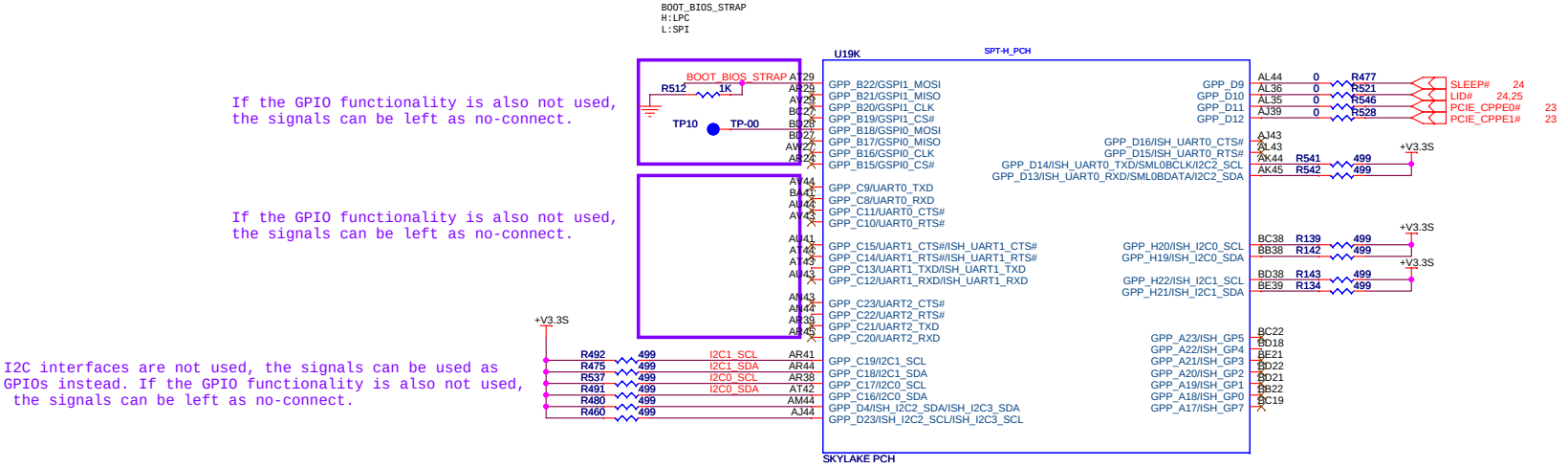

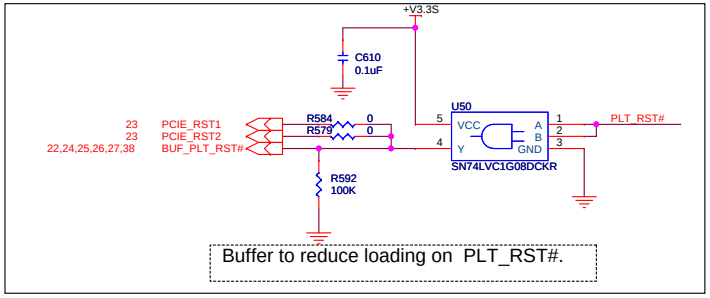

Title: **PCH(1/8)**		
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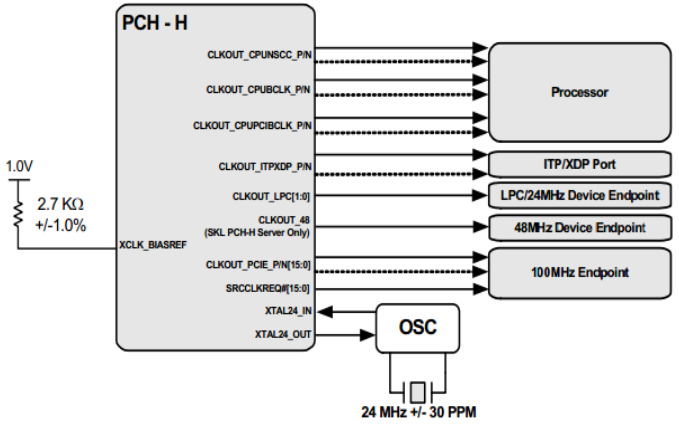

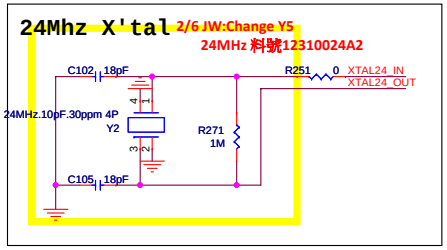

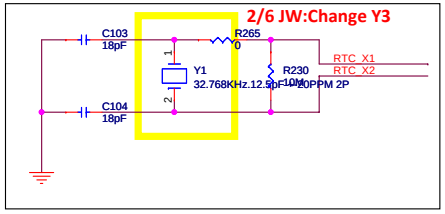

NOTE:

Any differential clock pair not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel ME FW

Any single ended clock signal not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel ME FW.

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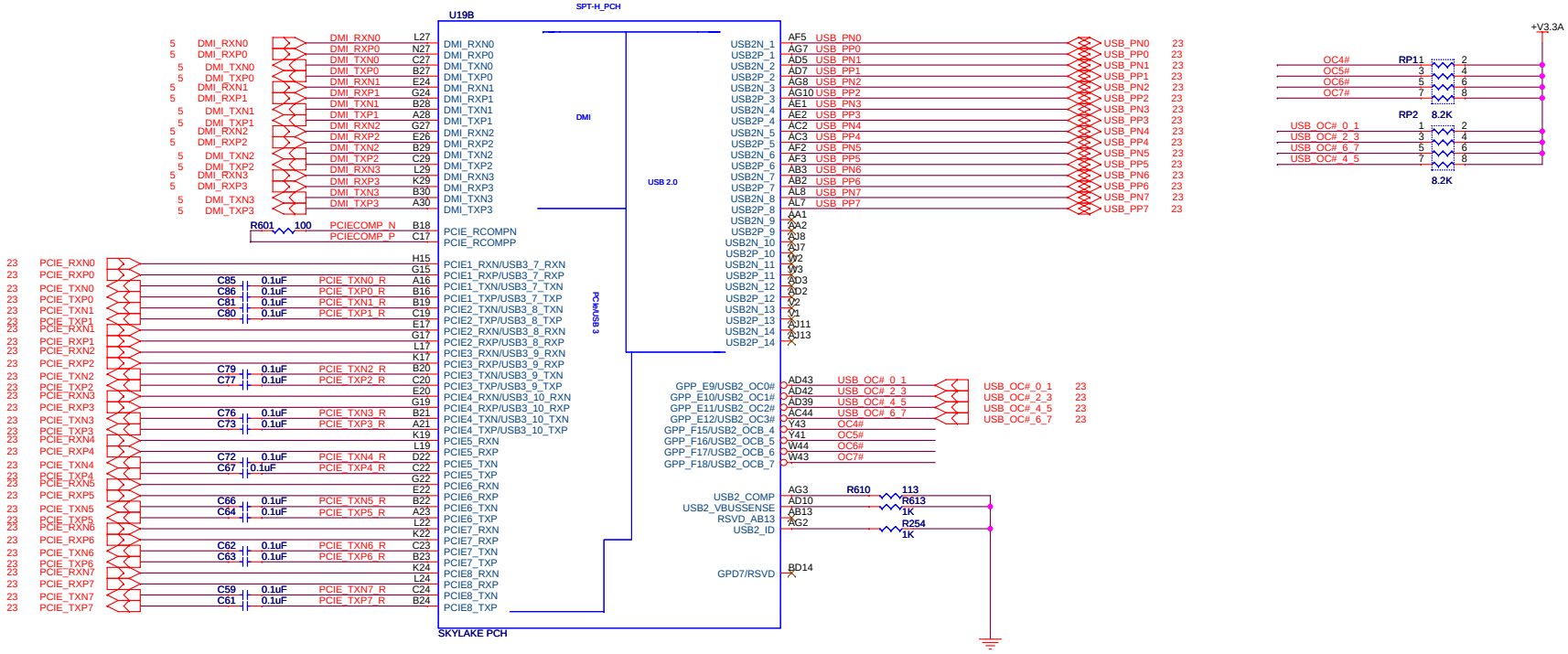

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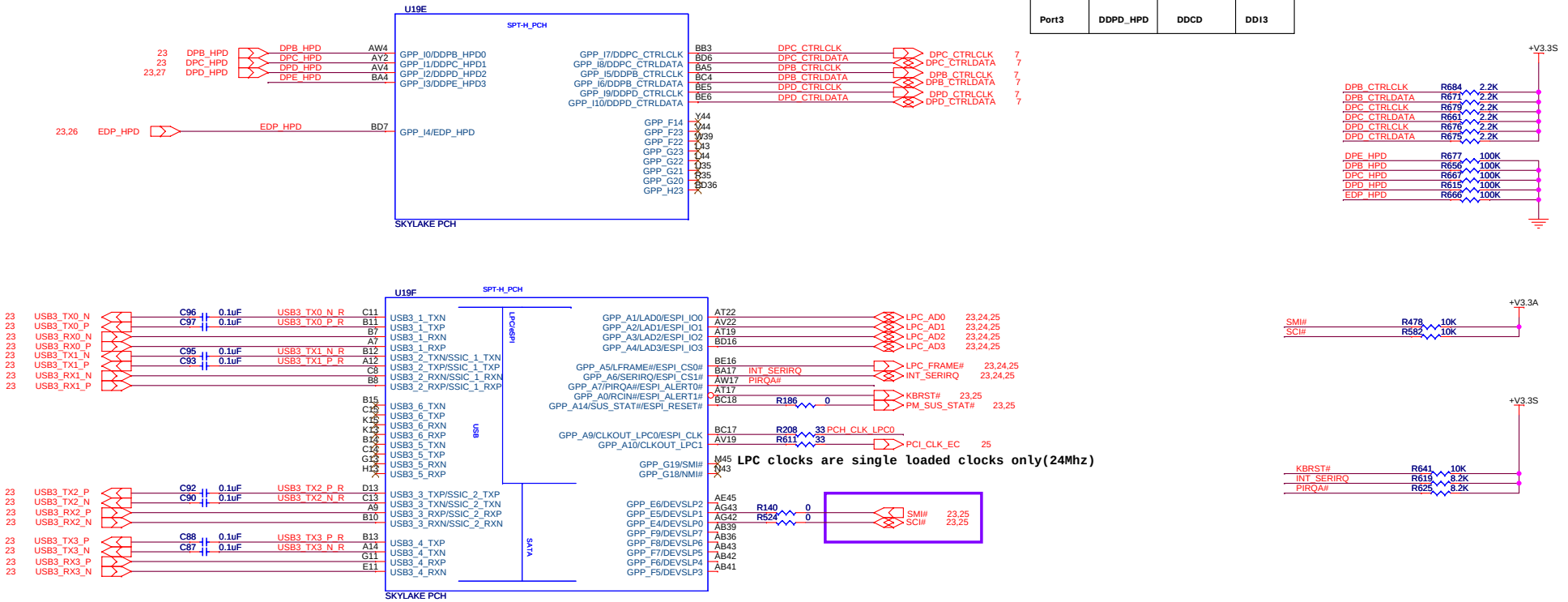
	HPD	DDC	DDI(CPU)
Port1	DDPB_HPD	DDCB	DDI1
Port2	DDPC_HPD	DDCC	DDI2
Port3	DDPD_HPD	DDCD	DDI3



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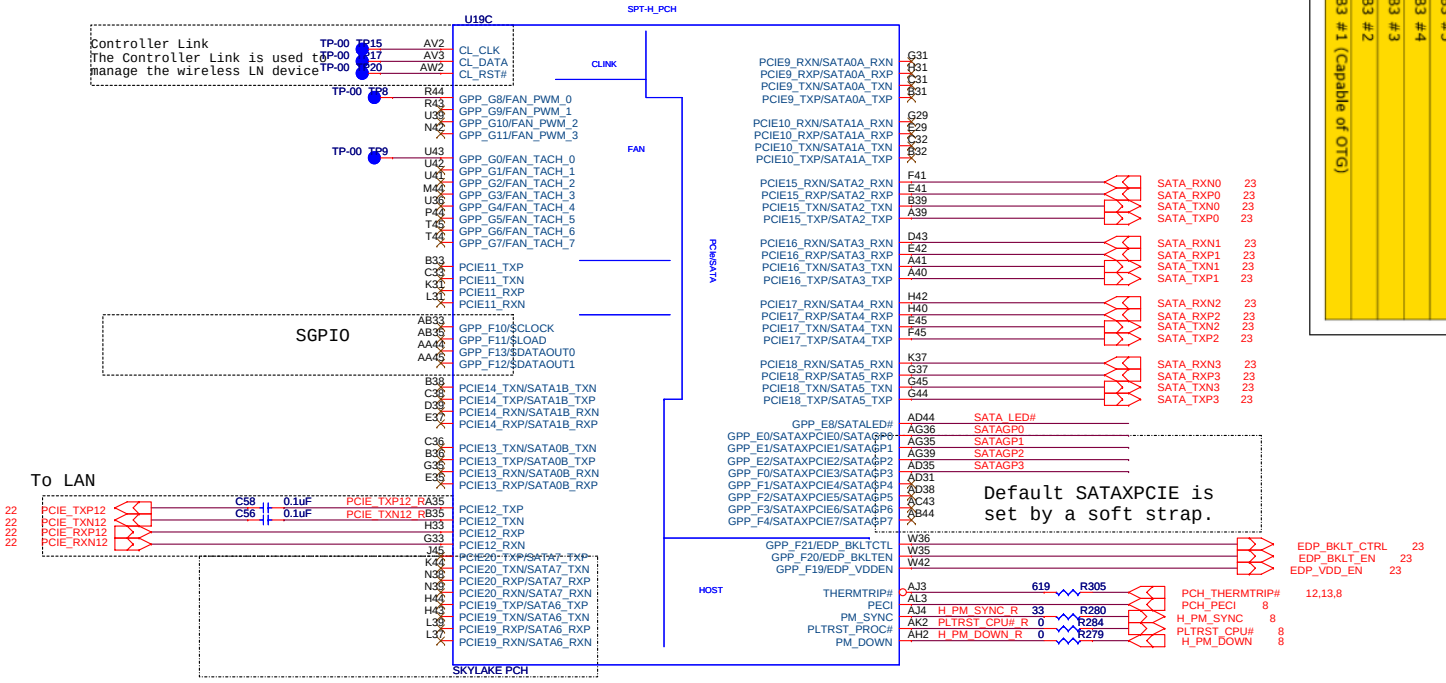
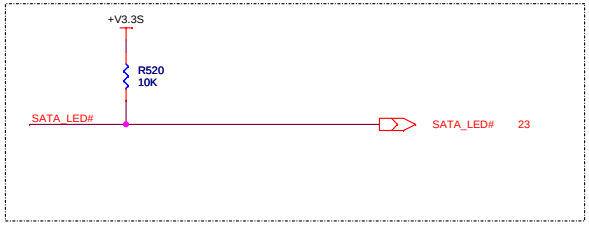
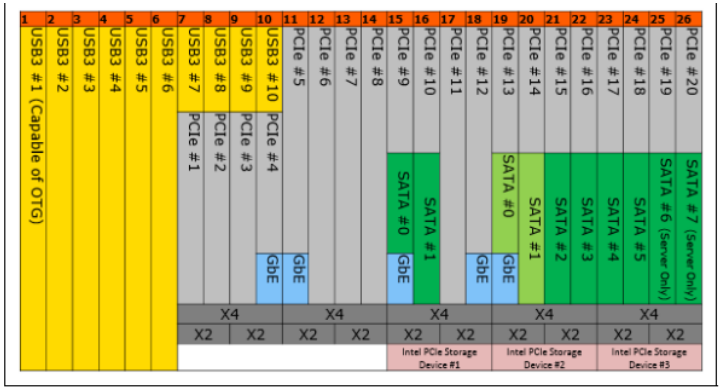
If an AMT capable Intel WLAN device is not implemented, then this signal can be left as NO CONNECT (NC).

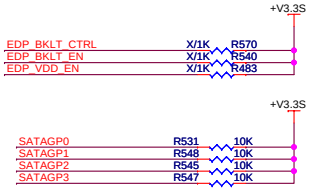


PCIE19/SATA6 AND PCIE20/SATA7 ARE ONLY AVAILABLE ON SERVER SKU



SKL PCH H Flexible I/O





AAEON an ASUS assoc. co.	Title: **PCH(5/8)**		
	Size: A	Document Number: **COM-SKH**	Rev: **A0.1**
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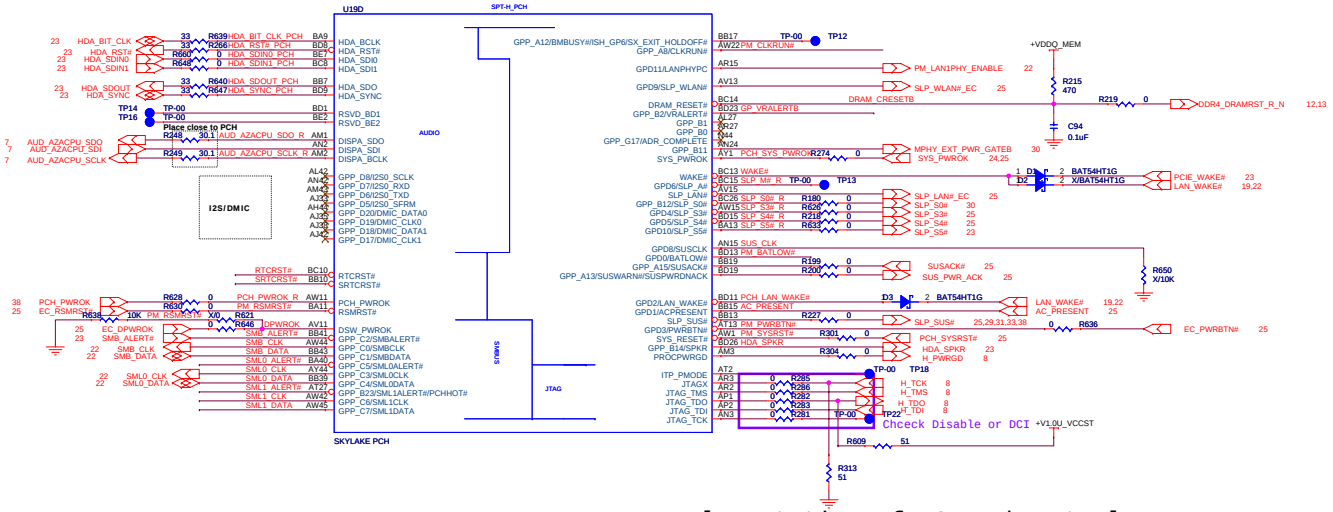
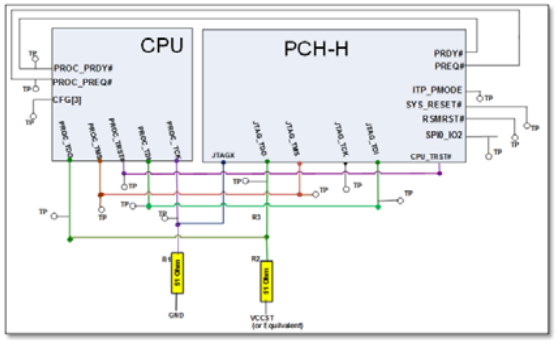
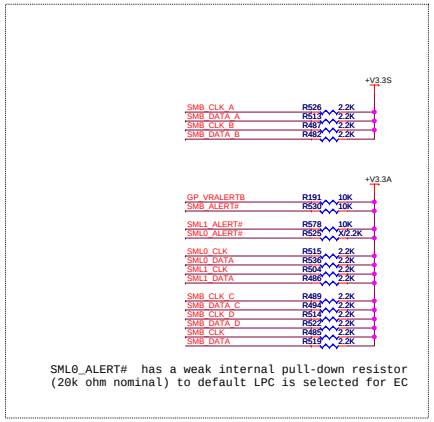
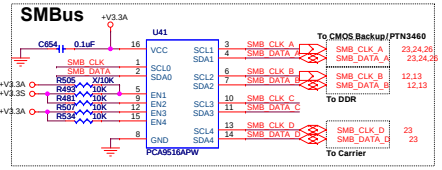
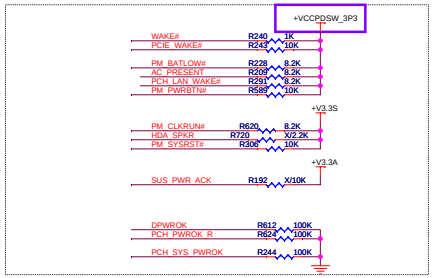


Implementation of DCI Debug tool









AAEON an ASUS assoc. co.	Title: PCH(6/8)		
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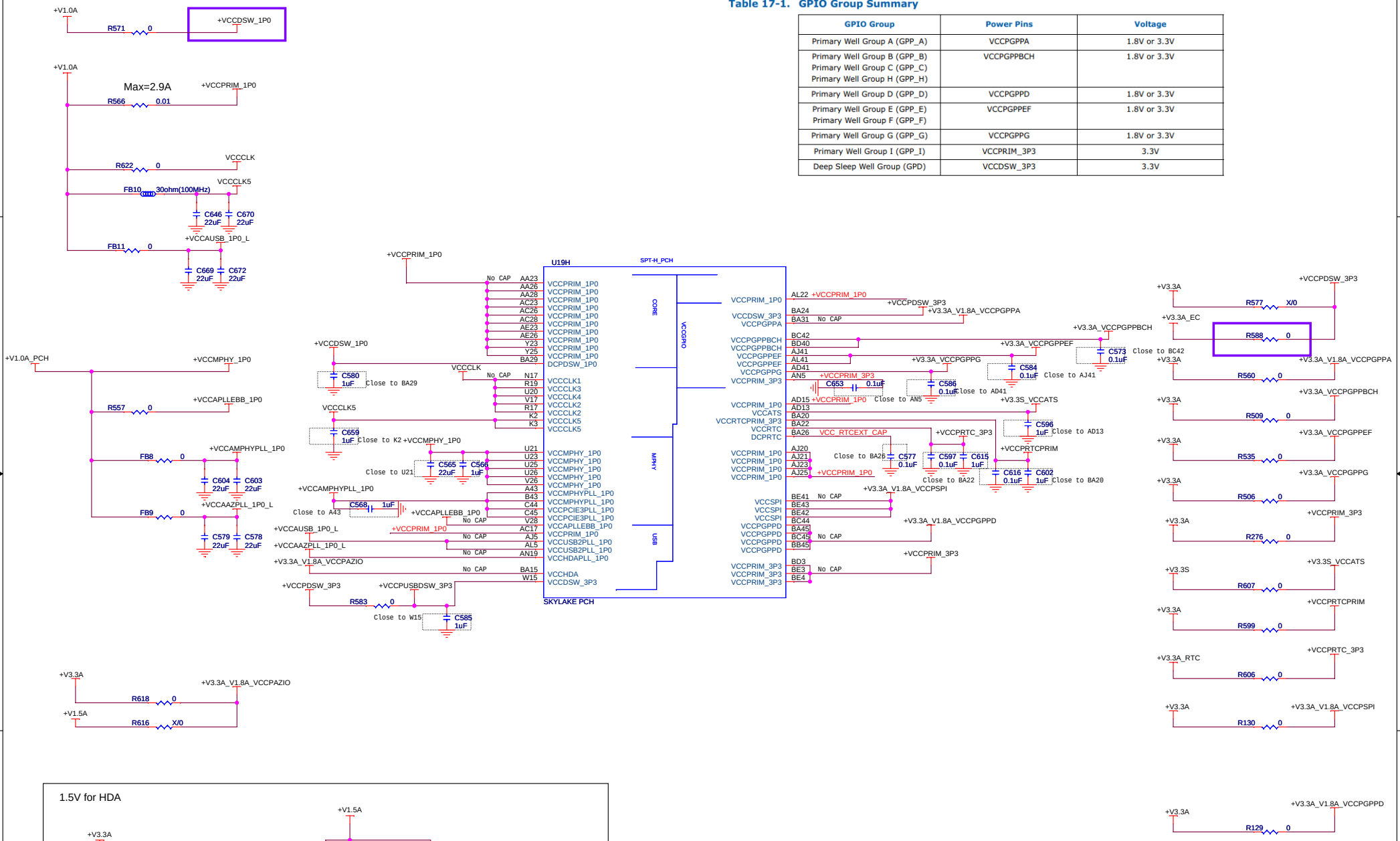
Table 17-1. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C) Primary Well Group H (GPP_H)	VCCPGPPBCH	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V



AAEON an ASUS assoc. co.	Title: **PCH(7/8)**	
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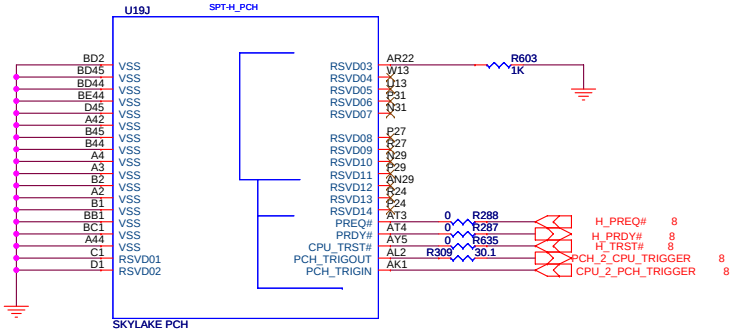

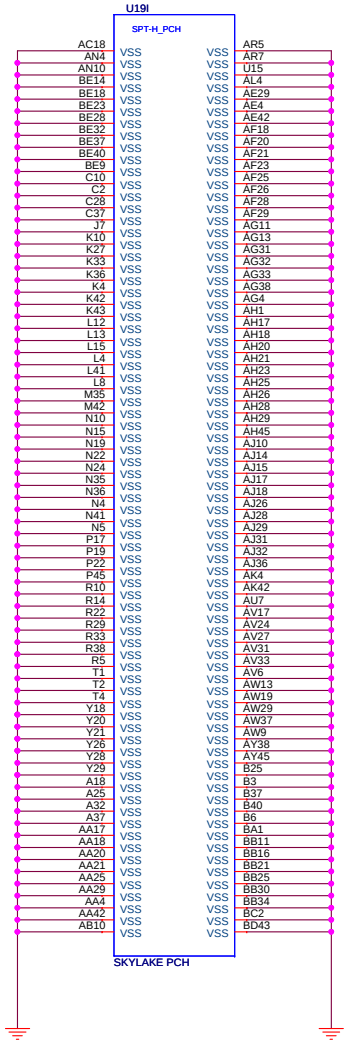

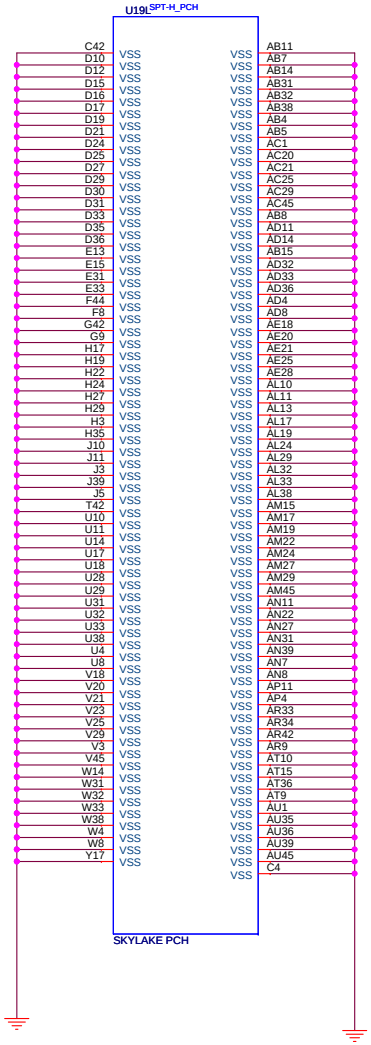

AAEON an ASUS assoc. co.	Title: **PCH(8/8)**	
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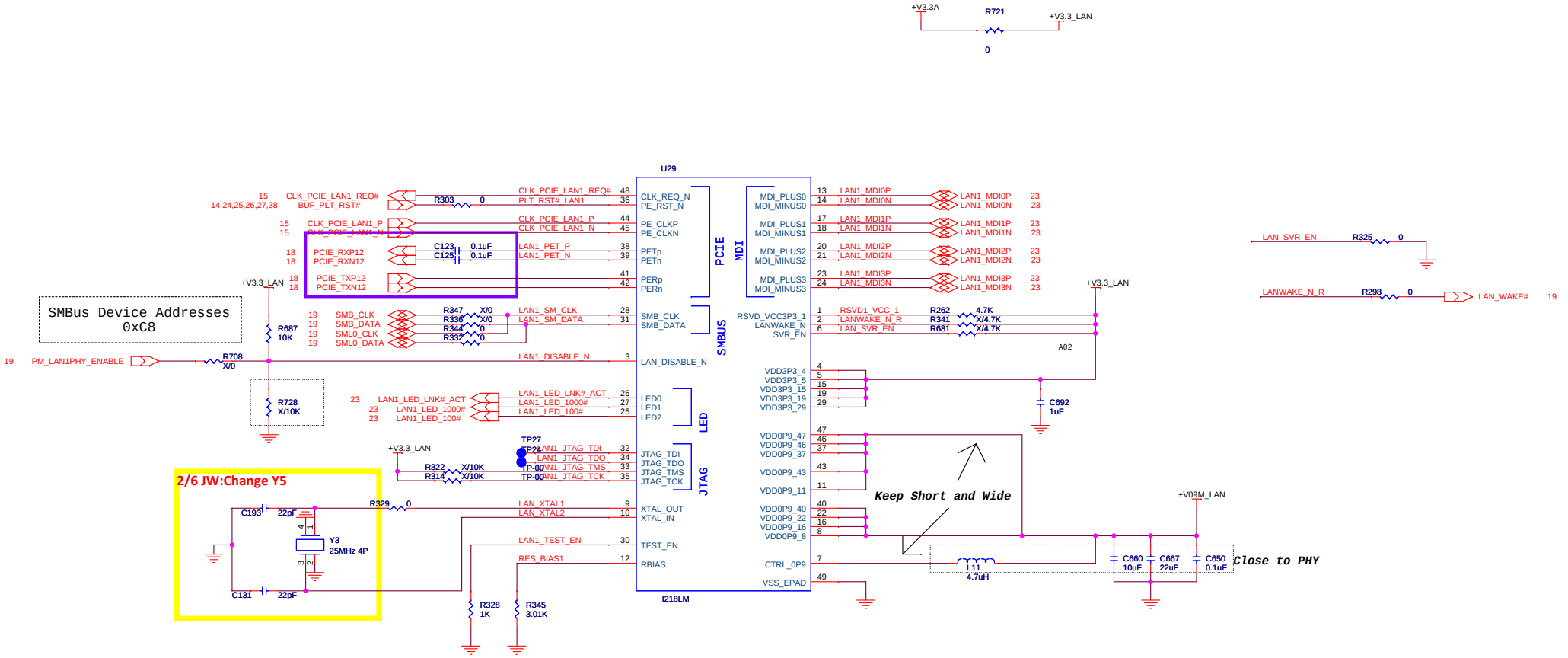
Jacksonville -MOBILE



ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY

SPEED LED
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps

LEDs	Mode	Function
LED0	0100	LINK/ACTIVITY
LED1	0111	LINK 1000
LED2	0110	LINK 100

AAEON an ASUS assoc. co.

Title: **LAN-I219**		
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Wide Voltage Input
+8.5V --- +19V

3/1 R403, R404, R411
change to NA.

Type 6
RowA & DowB
PN = 1654M0000

Wide Voltage Input
+8.5V --- +19V

Type 6
RowC & DowD
PN = 1654M0000

2/6 JW: Del U31, R352, R375

SKH新增

VGA HSYNC VSYNC

Bright Control BOM Control

Title	ROW A/B & C/D	
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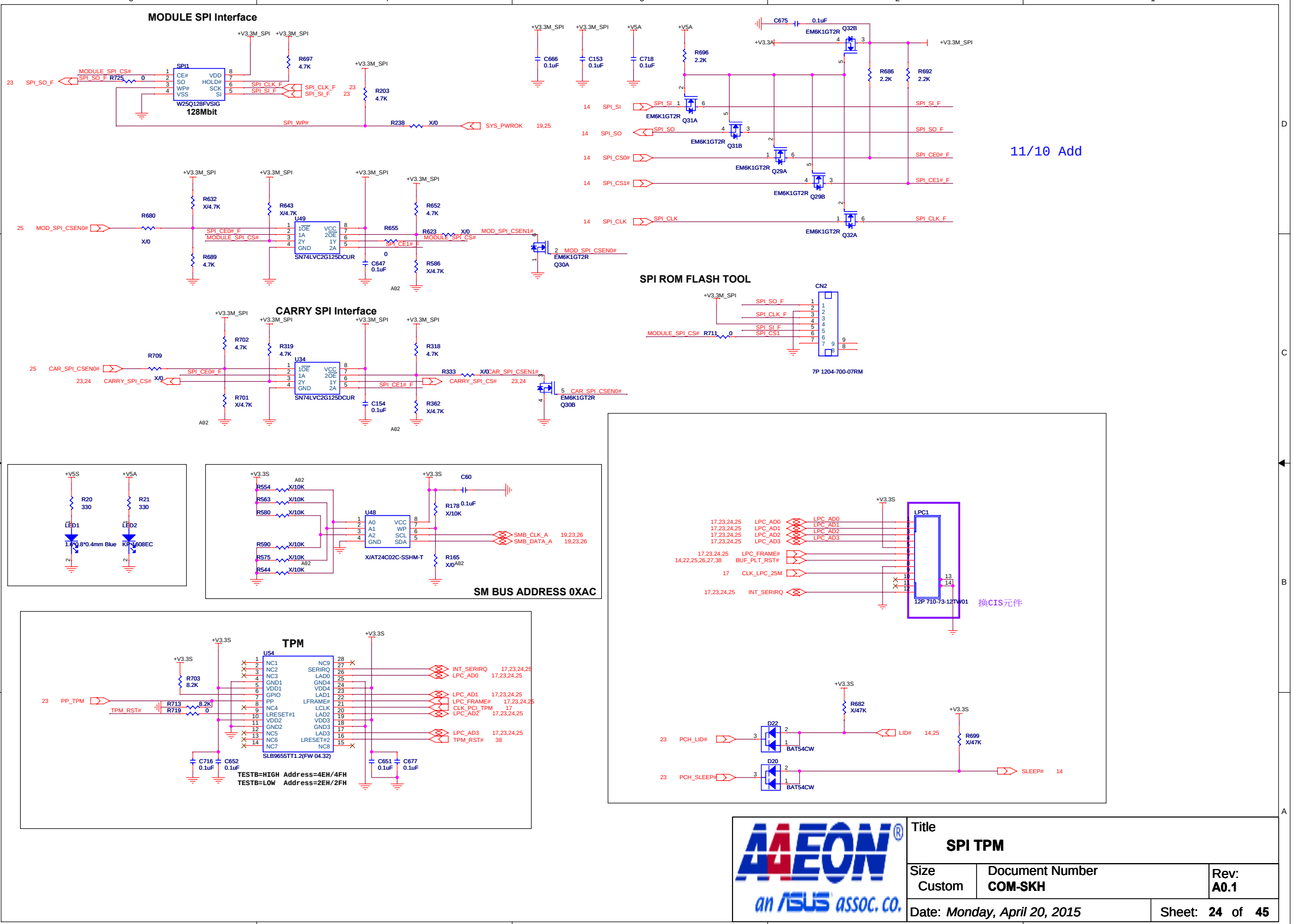
MODULE SPI Interface
SPI1
W25Q128FVSIG
128Mbit
CARRY SPI Interface
U49
U34
SN74LVC2G125DCUR
SPI ROM FLASH TOOL
CN2
7P 1204-700-07RM
11/10 Add
SM BUS ADDRESS 0XAC
U48
X/AT24C02C-SSHM-T
TPM
U54
SLB9655TT1.2(FW 04.32)
TESTB=HIGH Address=4EH/4FH
TESTB=LOW Address=2EH/2FH
LPC1
12P 710-73-12TW01
換CIS元件
D22
D20
BAT54CW
Title
SPI TPM
Size
Custom
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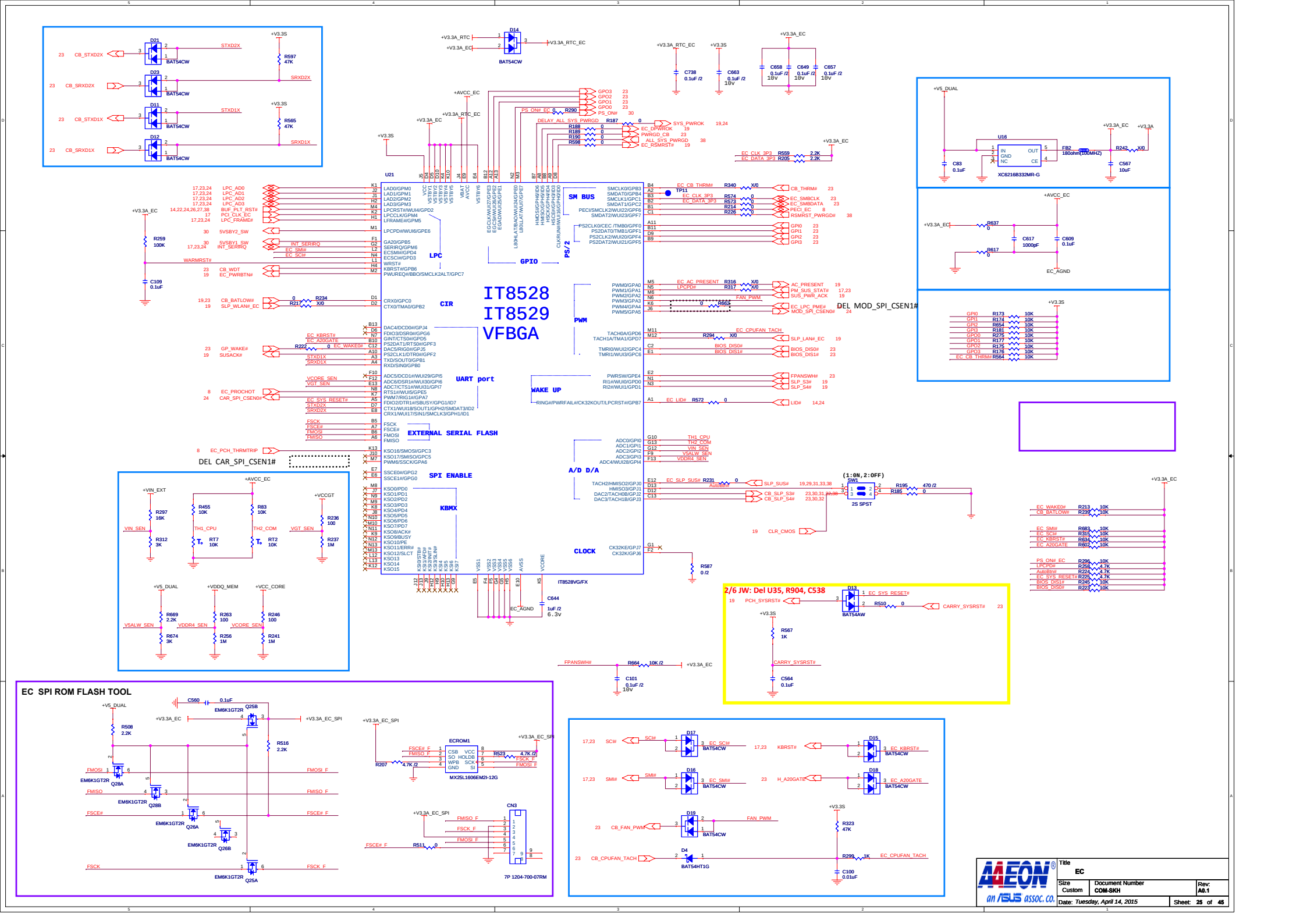
IT8528
IT8529
VFBGA
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
IT8528VG/FX
DEL CAR_SPI_CSEN1#
DEL MOD_SPI_CSEN1#
2/6 JW: Del U35, R904, C538
EC SPI ROM FLASH TOOL
MX25L1606EM2I-12G
7P 1204-700-07RM
XC6216B332MR-G
2S SPST
Title
EC
Size
Custom
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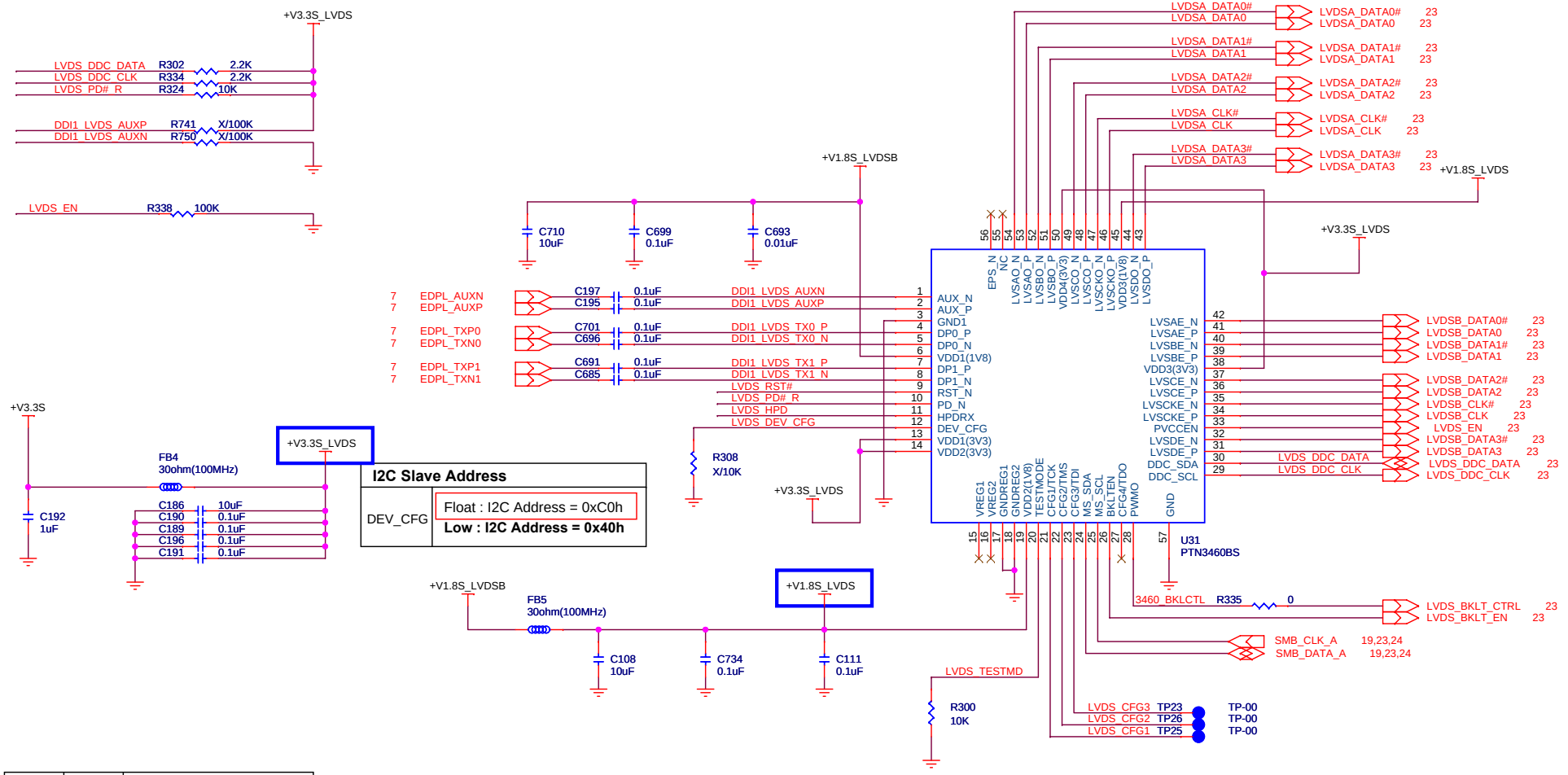
PTN3460



CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

AAEON an ASUS assoc. co.

Title: **DP TO LVDS**

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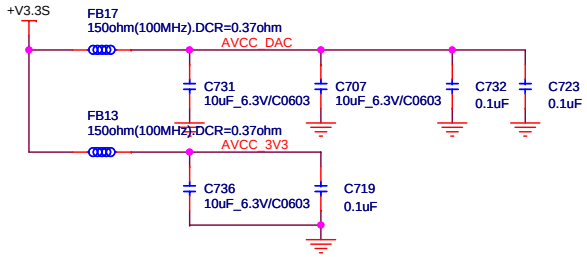
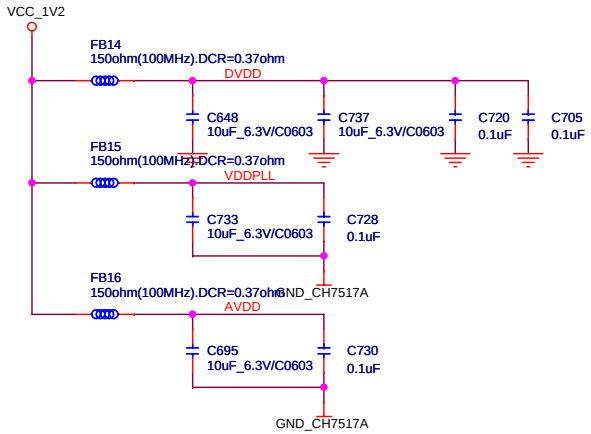
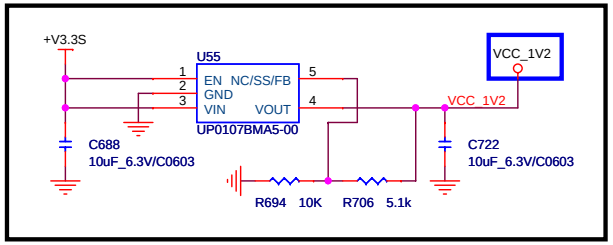
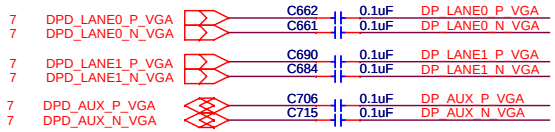
Note:
1. +1.05V power spply tolerance range -5%~+25%
2. +3.3V power spply tolerance range +/-10%





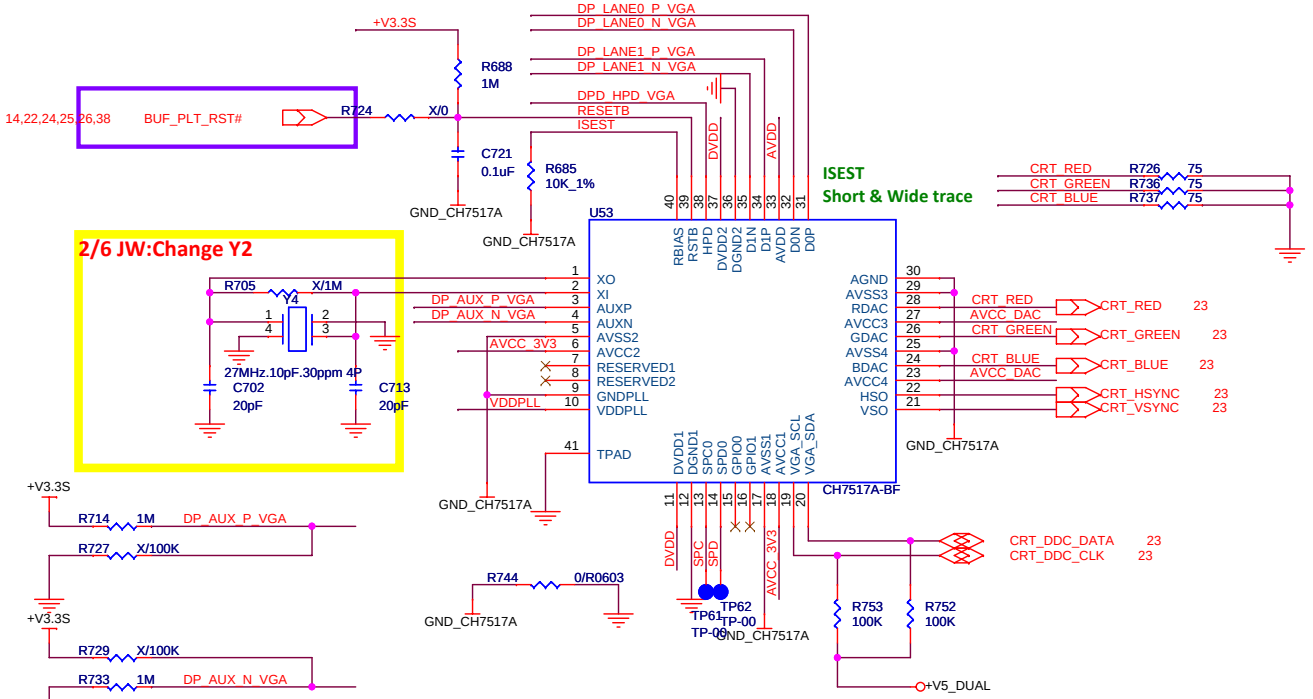
Reserve for Test





Note:
HPD要不要反向,要看DDI來源晶片的設計.

CH7517



AAEON an ASUS assoc. co.	Title: DP to VGA	
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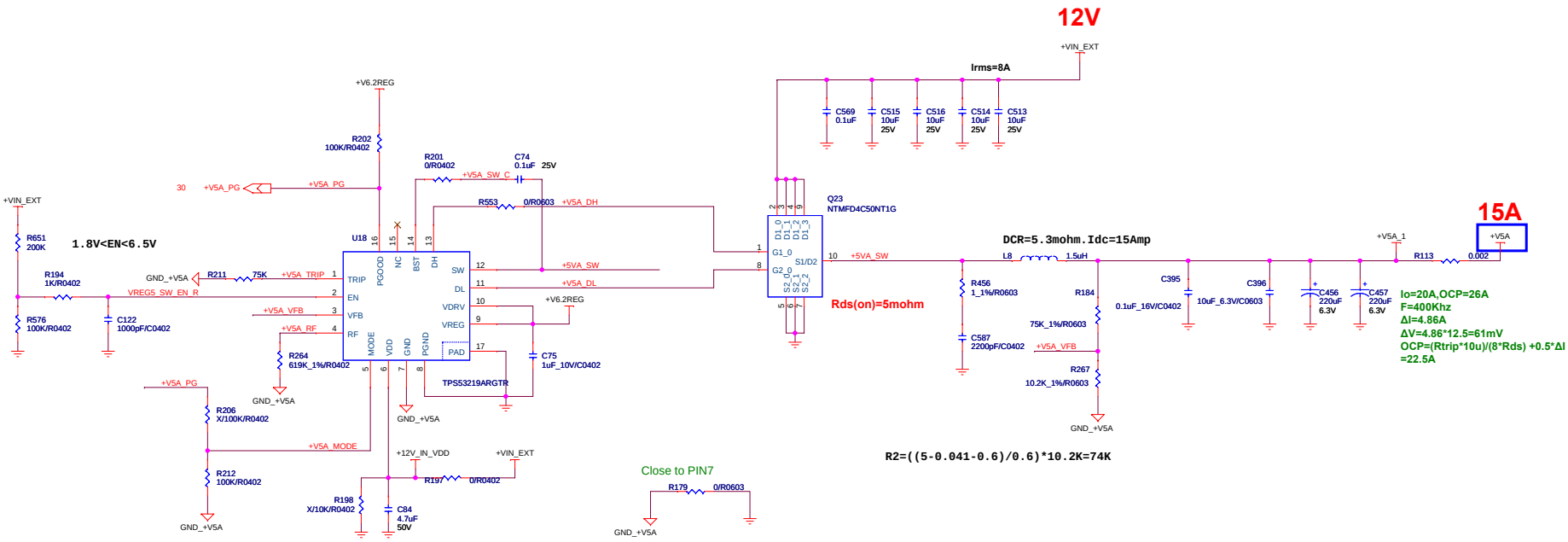

AAEON an ASUS assoc. co.	Title: **PPWER SWITCH +V5A**	
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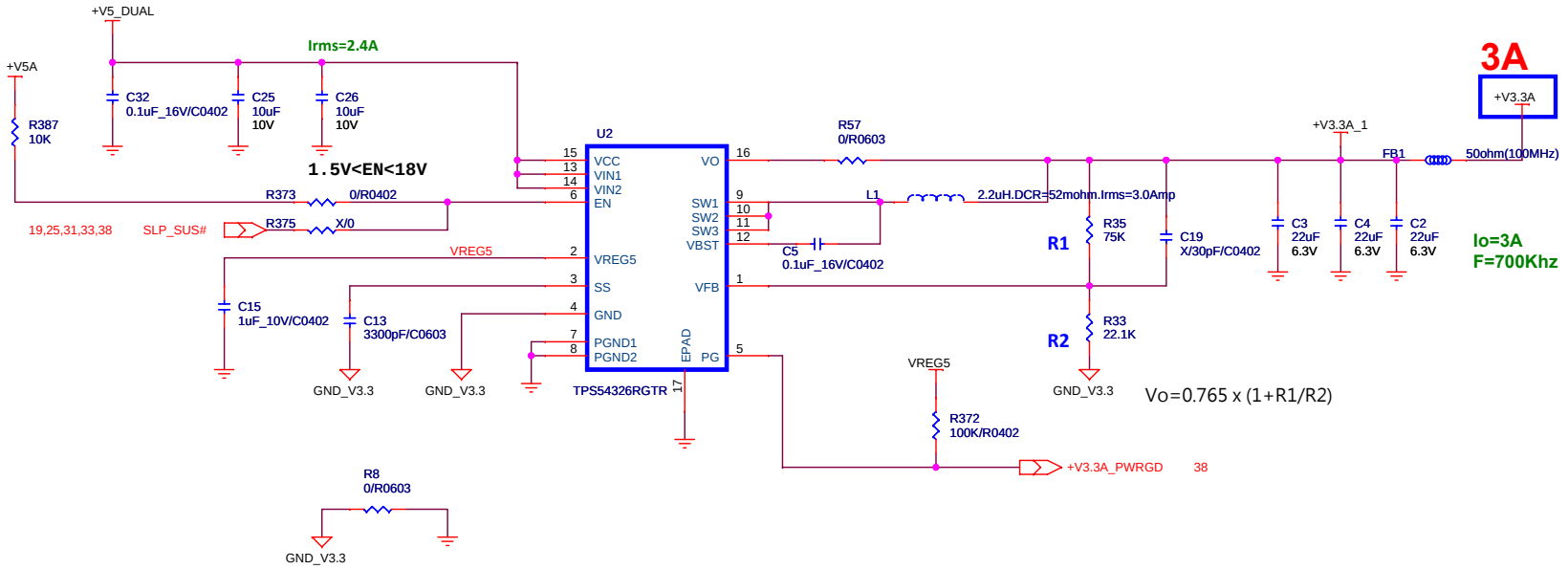
+V3.3A



AAEON an ASUS assoc. co.	Title: PPWER SWITCH +V3A	
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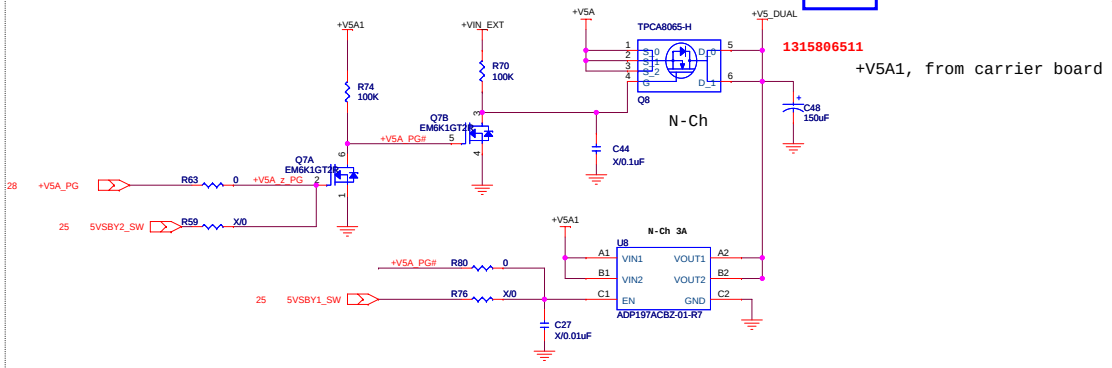
+V5A switch circuit

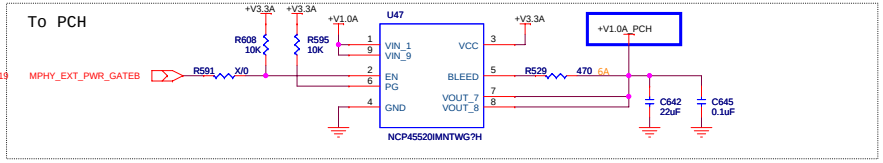
+V5A1, from carrier board
+V5A, from COM Module

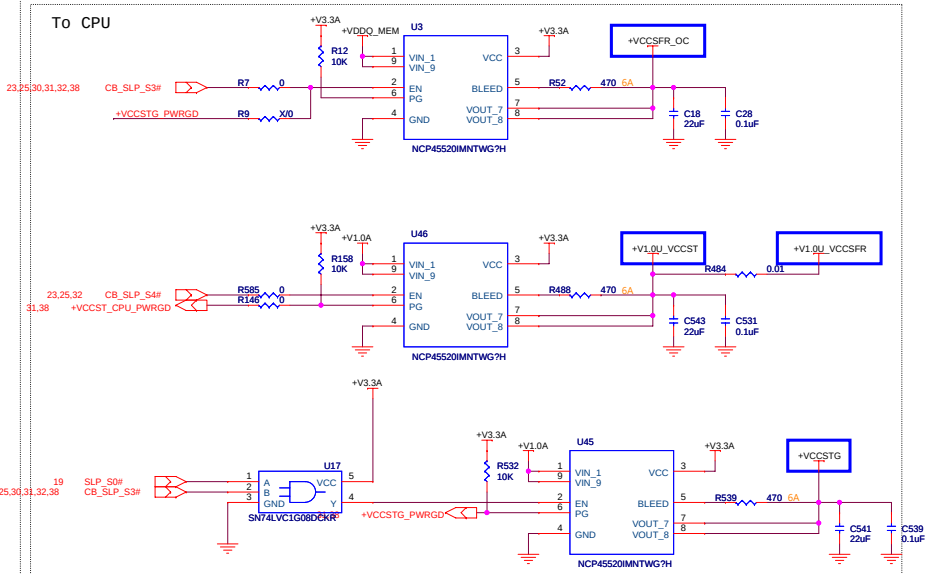
+V5A

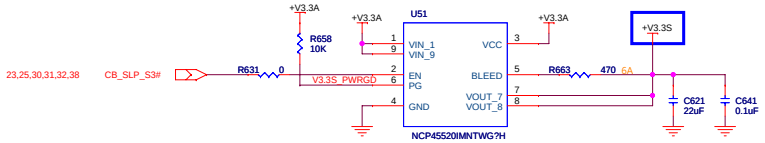
1315806511

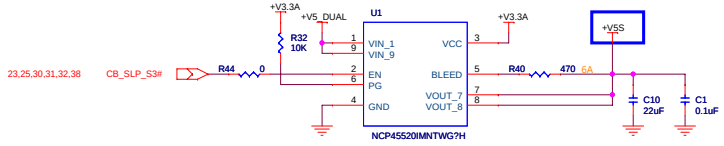
+V5A1, from carrier board

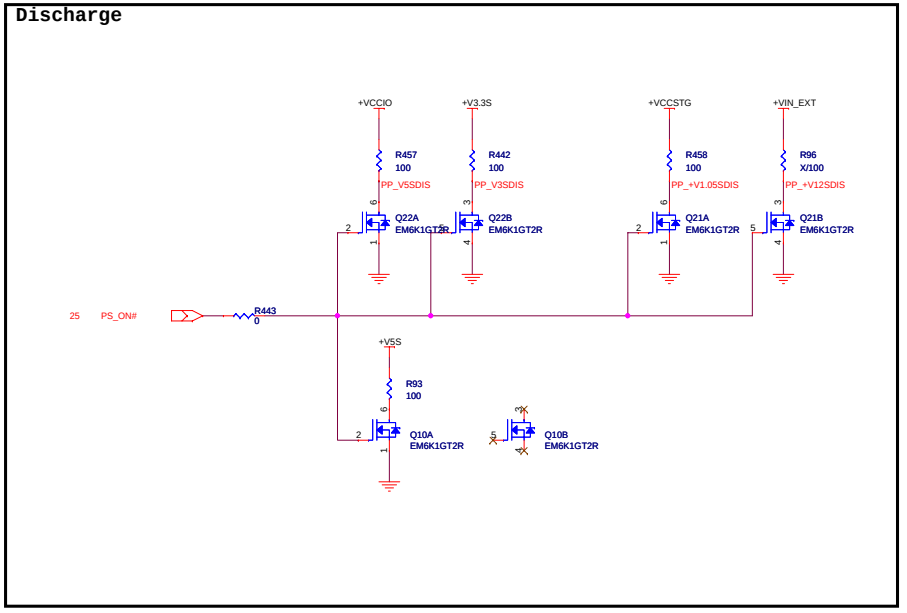












AAEON an ASUS assoc. co.	Title: PPWER SWITCH +V5_3V_1.8V_STG	
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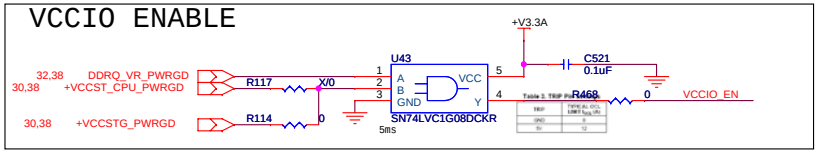
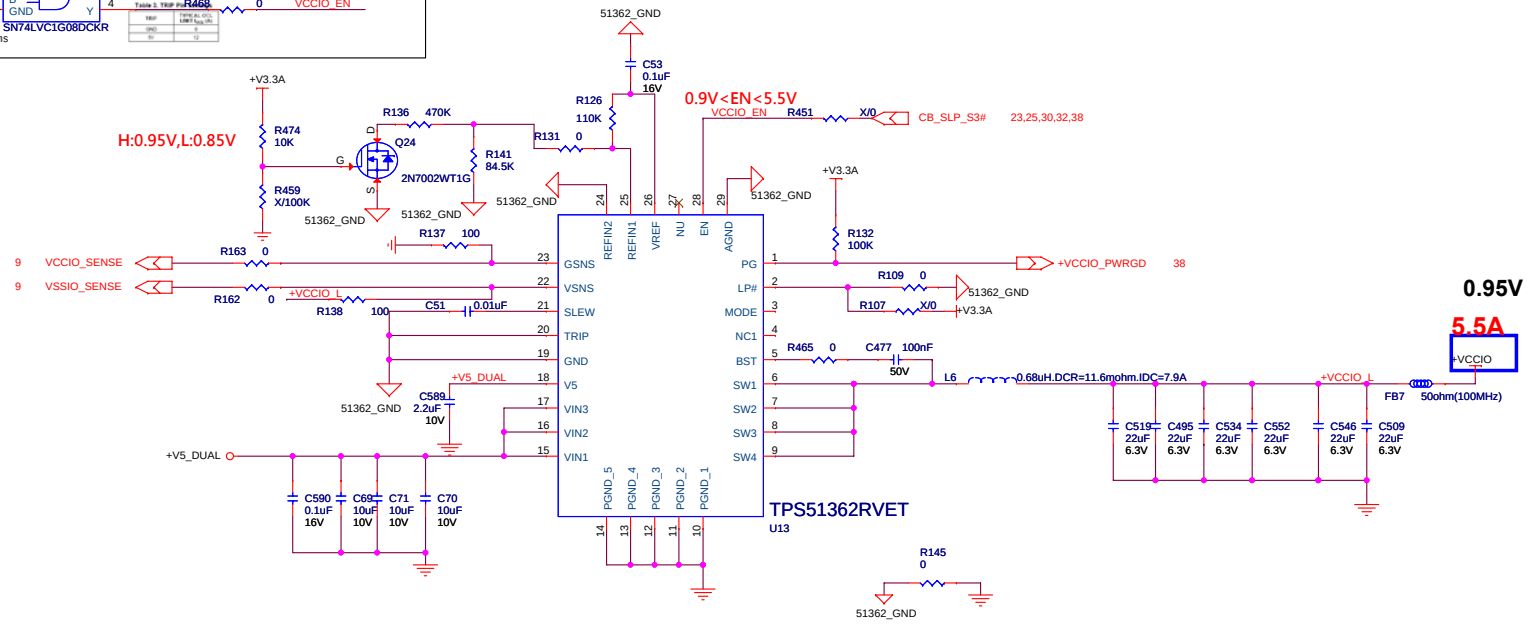
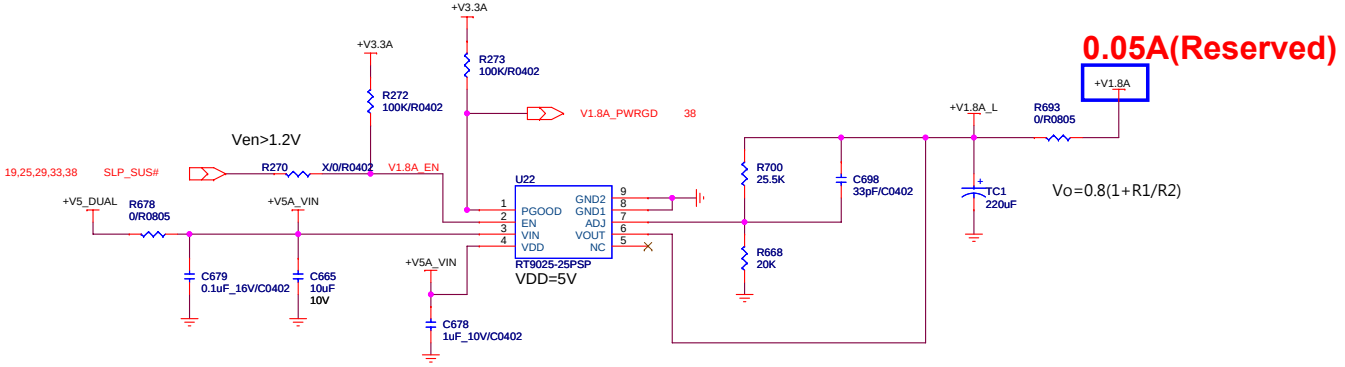
+VCCIO







AAEON an ASUS assoc. co.	Title: **+V1.05/+V1.5S**	
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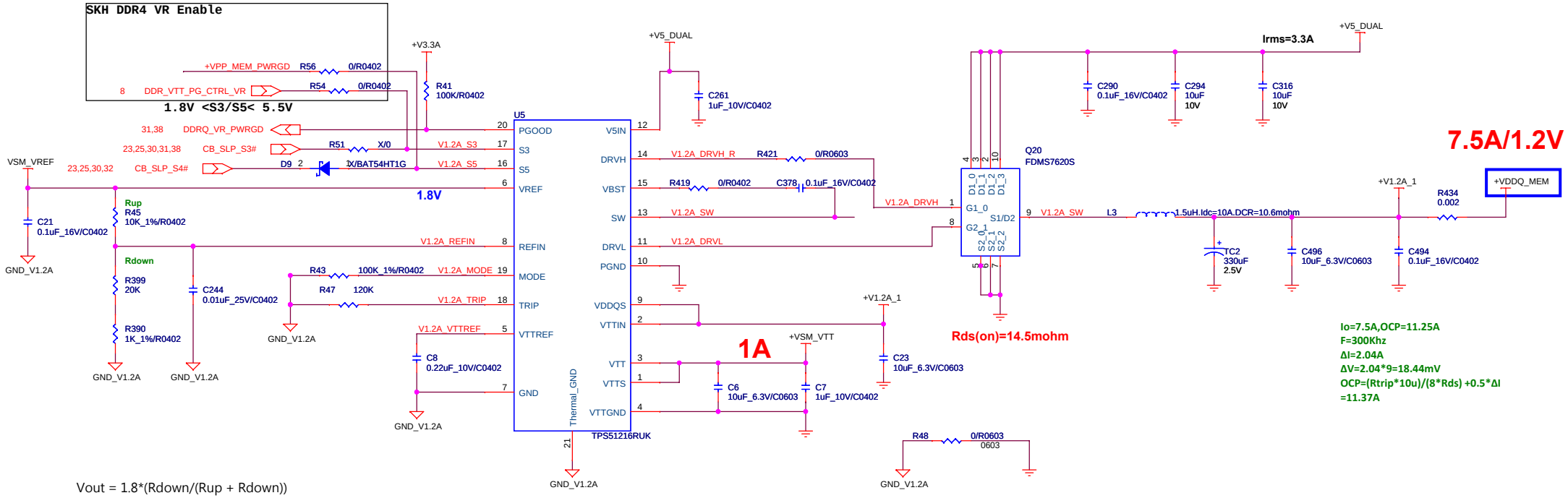


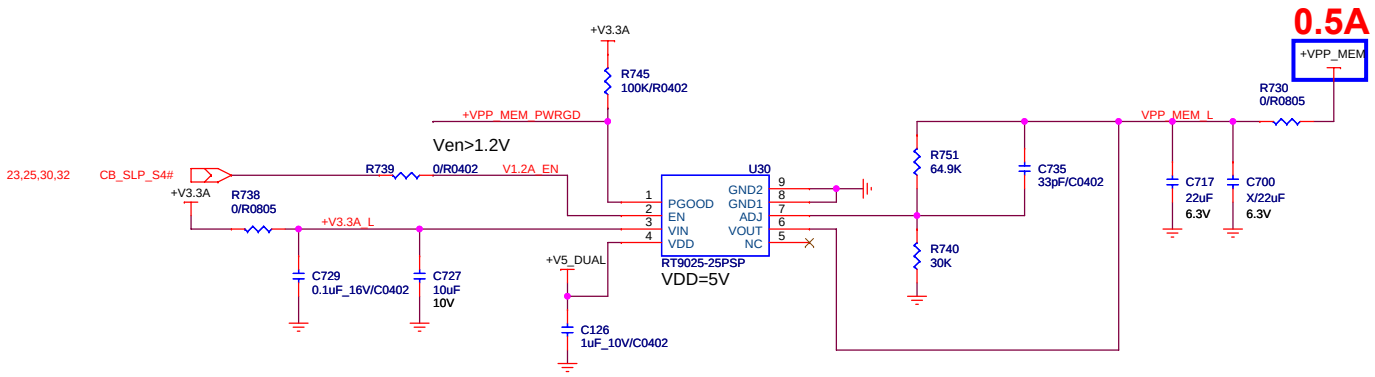
Vout = 1.8*(Rdown/(Rup + Rdown))

MODE Selection

Resistance(K ohm)	SW Frequency(kHz)	Discharge Mode
200	400	Tracking
100	300	Tracking
68	300	Non-tracking
47	400	Non-tracking

S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF
S4/S5	LO	LO	OFF	OFF	OFF	OFF



Vout = 0.8 x (1 + Rup / Rdown)=2.5V

AAEON an ASUS assoc. co.	Title: +VDDQ_MEM/VPP	
	Size: A3	Document Number: COM-SKH — Rev: A0.1
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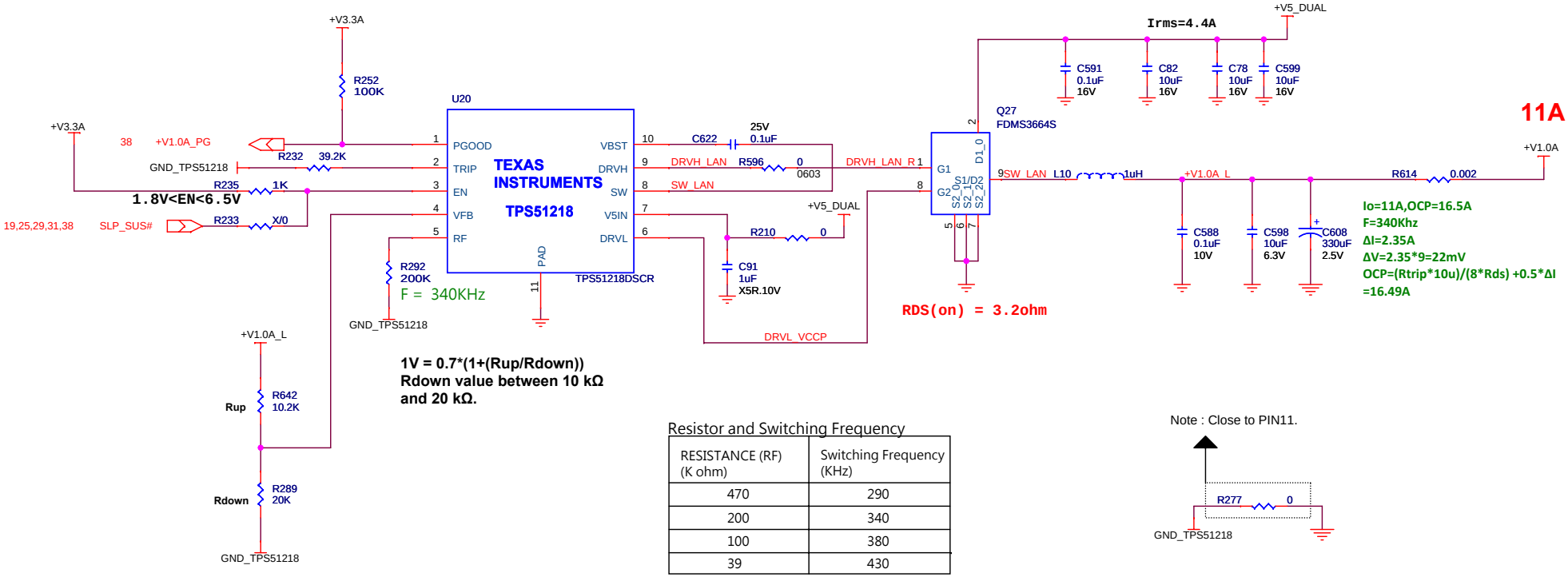

Resistor and Switching Frequency

RESISTANCE (RF) (K ohm)	Switching Frequency (KHz)
470	290
200	340
100	380
39	430

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Size: B	Document Number: COM-SKH	Rev: A0.1
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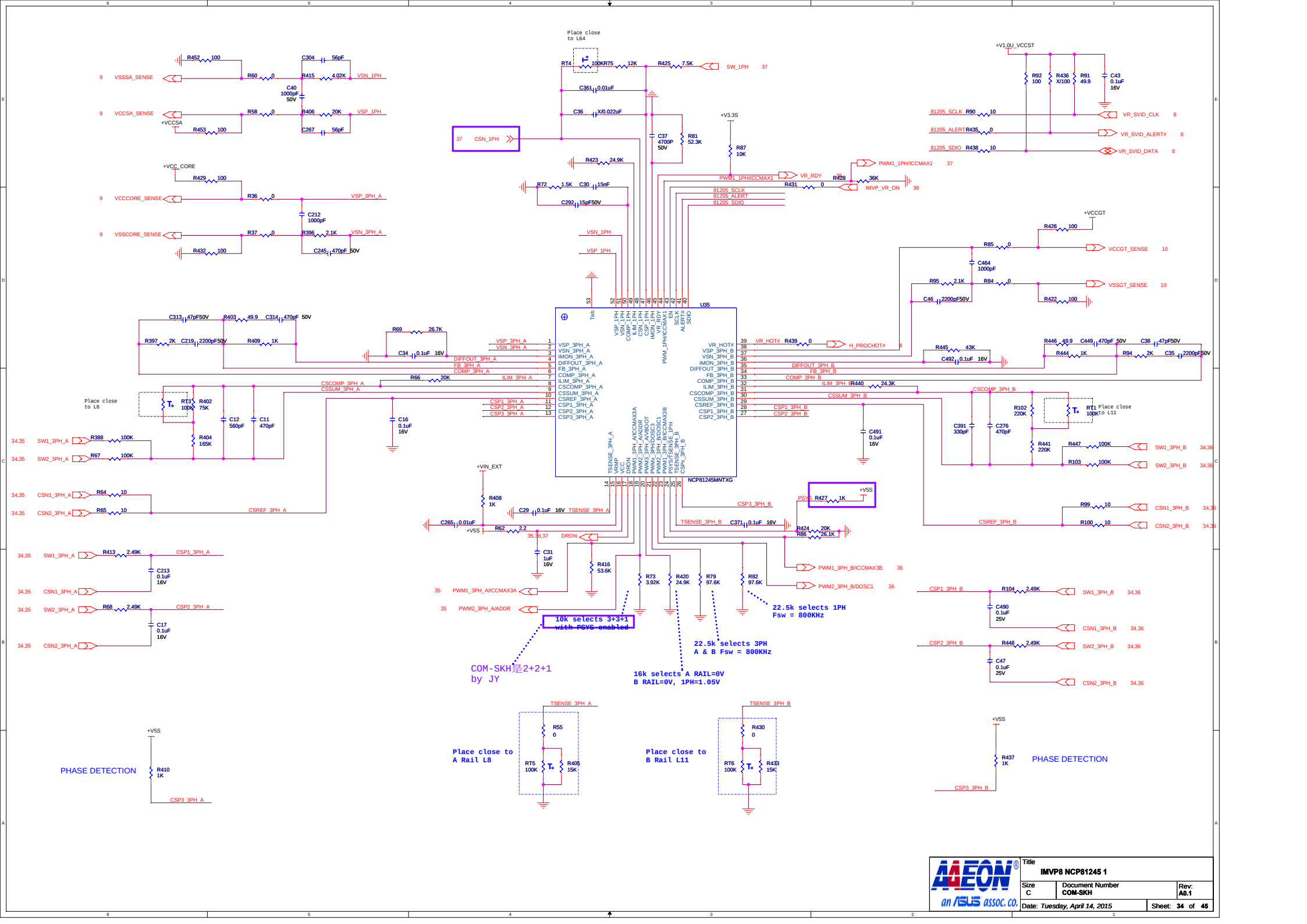

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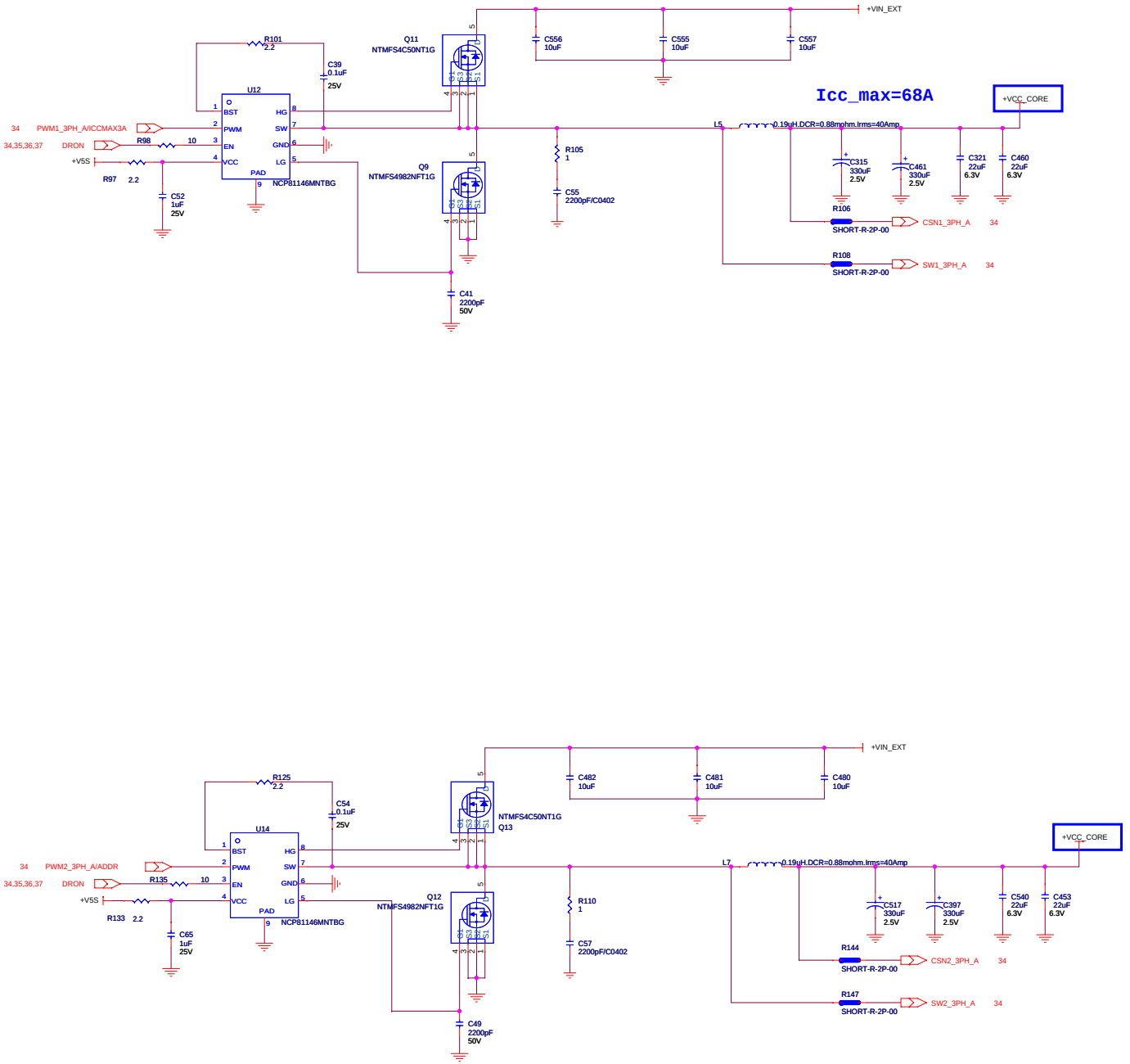

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Title: **33) IMVP8 VCORE**

Size	Document Number	Rev:
C	**COM-SKH**	**A0.1**

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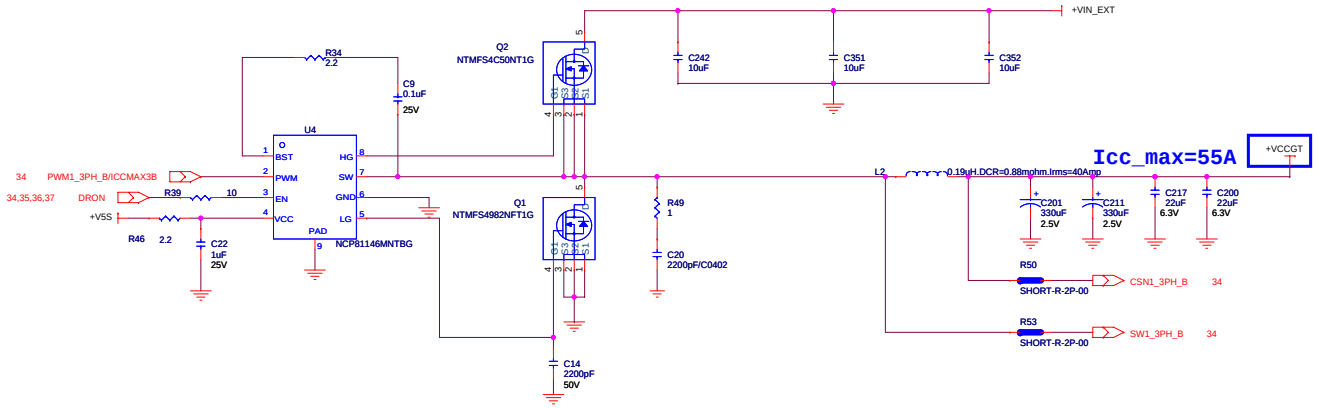

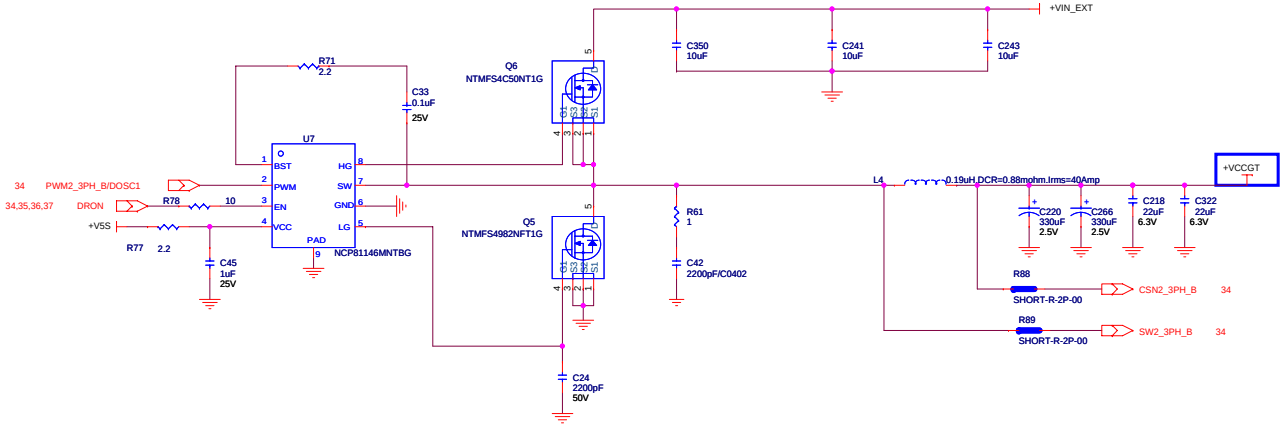

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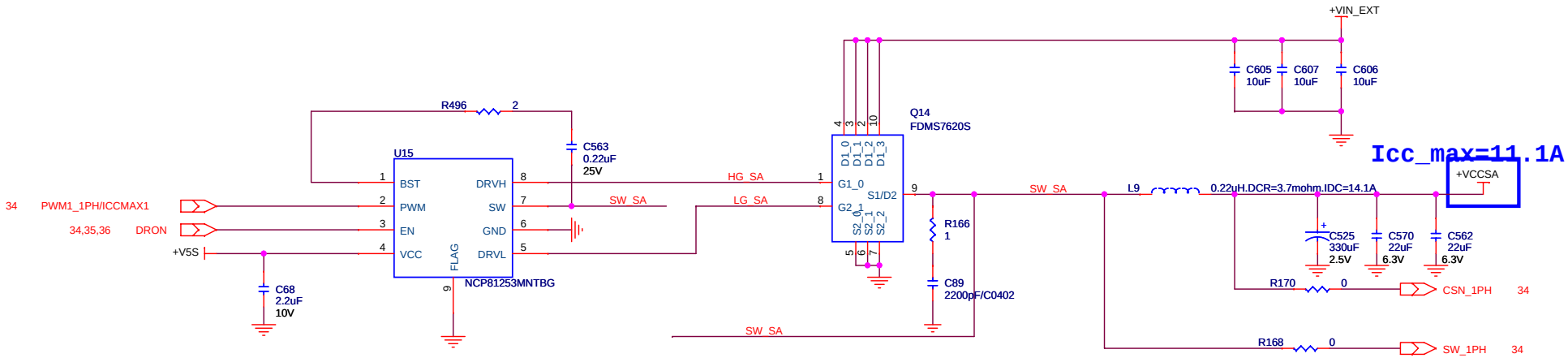
Size: C	Document Number: COM-SKH	Rev: A0.1
Date: Tuesday, April 14, 2015		Sheet: 36 of 45



AAEON an ASUS assoc. co.	Title: IMVP8 VCCSA		
	Size: B	Document Number: COM-SKH	Rev: A0.1
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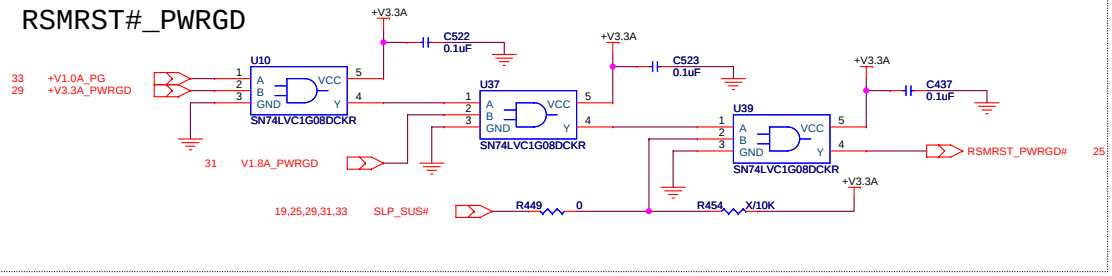
RSMRST#_PWRGD



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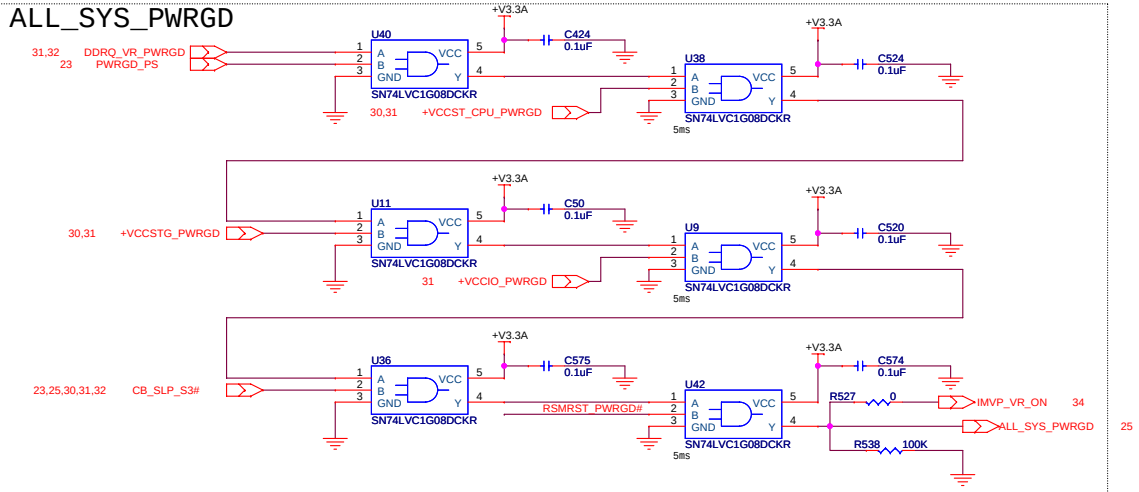
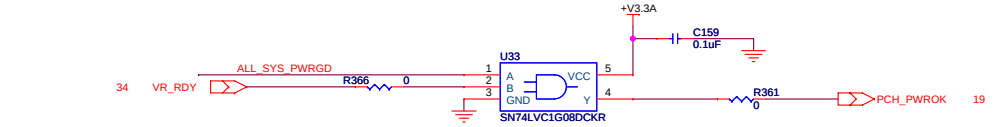
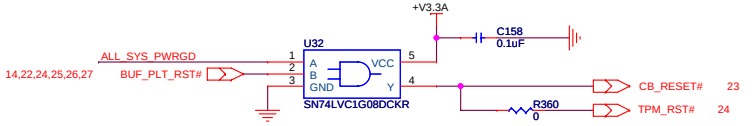
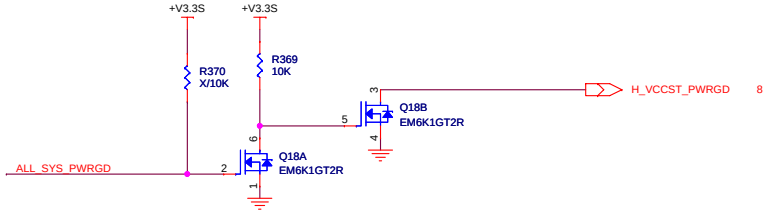
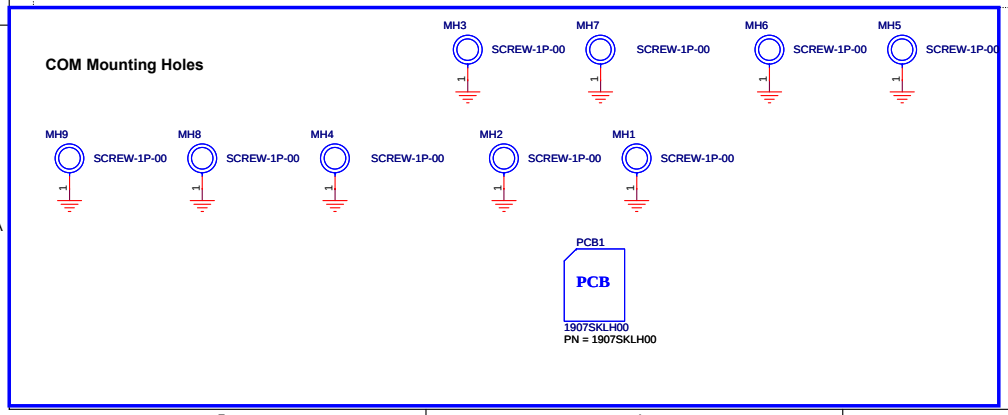


PCH_PWROK









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Title: **Boot Sequence/iAMT Control**

Size	Document Number	Rev:
A	**COM-SKH**	**A0.1**

Date: *Tuesday, April 14, 2015* Sheet: **38** of **45**

HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
	2015/	A0.1	First Release			

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已接接了
但不確定

James Wu
修改

Vic 修改

Jamew Yang
修改

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Size	Document Number	Rev:
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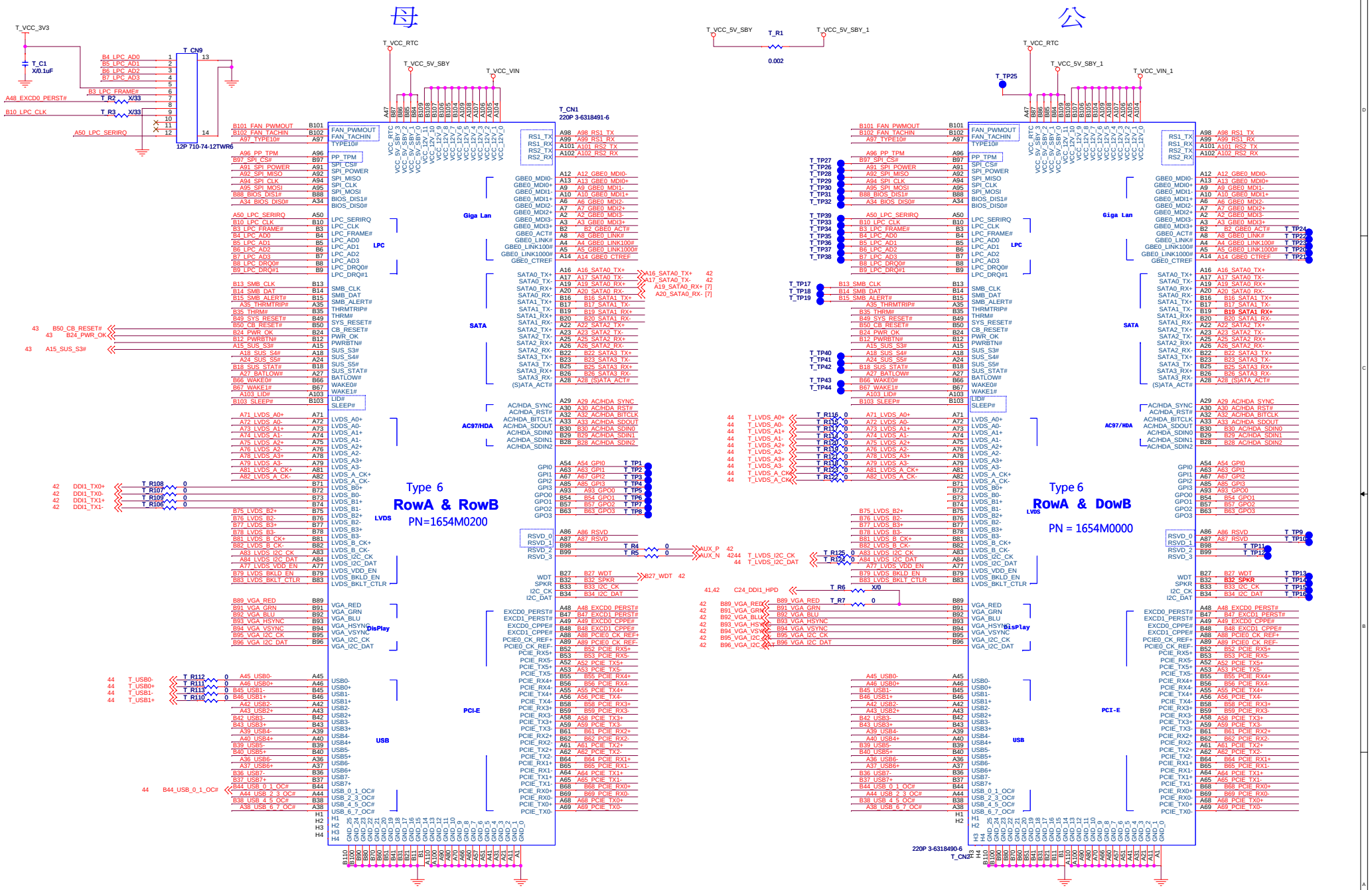
Date: *Tuesday, April 14, 2015*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220P 3-6318491-6
T_CN2
220P 3-6318490-6
Type 6
RowA & RowB
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Type 6
RowA & DowB
PN = 1654M0000
Giga Lan
LPC
SATA
AC97/HDA
LVDS
DisPlay
PCI-E
USB
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T_VCC_RTC
T_VCC_5V_SBY
T_VCC_VIN
T_VCC_5V_SBY_1
T_VCC_VIN_1
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X0.1uF
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X/33
T_R3
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B6_LPC_AD2
B7_LPC_AD3
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A50_LPC_SERIRQ
B3_LPC_FRAME#
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FAN_TACHIN
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SPI_MISO
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BIOS_DIS0#
LPC_SERIRQ
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LPC_FRAME#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ0#
LPC_DRQ#1
SMB_CLK
SMB_DAT
SMB_ALERT#
THRMTRIP#
THRM#
SYS_RESET#
CB_RESET#
PWR_OK
PWRBTN#
SUS_S3#
SUS_S4#
SUS_S5#
SUS_STAT#
BATLOW#
WAKE0#
WAKE1#
LID#
SLEEP#
B50_CB_RESET#
B24_PWR_OK
A15_SUS_S3#
LVDS_A0+
LVDS_A0-
LVDS_A1+
LVDS_A1-
LVDS_A2+
LVDS_A2-
LVDS_A3+
LVDS_A3-
LVDS_A_CK+
LVDS_A_CK-
LVDS_B0+
LVDS_B0-
LVDS_B1+
LVDS_B1-
LVDS_B2+
LVDS_B2-
LVDS_B3+
LVDS_B3-
LVDS_B_CK+
LVDS_B_CK-
LVDS_I2C_CK
LVDS_I2C_DAT
LVDS_VDD_EN
LVDS_BKLD_EN
LVDS_BKLT_CTLR
DDI1_TX0+
DDI1_TX0-
DDI1_TX1+
DDI1_TX1-
VGA_RED
VGA_GRN
VGA_BLU
VGA_HSYNC
VGA_VSYNC
VGA_I2C_CK
VGA_I2C_DAT
USB0-
USB0+
USB1-
USB1+
USB2-
USB2+
USB3-
USB3+
USB4-
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USB5+
USB6-
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USB7-
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USB_2_3_OC#
USB_4_5_OC#
USB_6_7_OC#
B44_USB_0_1_OC#
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GBE0_MDI1-
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GBE0_MDI2-
GBE0_MDI2+
GBE0_MDI3-
GBE0_MDI3+
GBE0_ACT#
GBE0_LINK#
GBE0_LINK100#
GBE0_LINK1000#
GBE0_CTREF
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SATA0_TX-
SATA0_RX+
SATA0_RX-
SATA1_TX+
SATA1_TX-
SATA1_RX+
SATA1_RX-
SATA2_TX+
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SATA3_RX-
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AC/HDA_RST#
AC/HDA_BITCLK
AC/HDA_SDOUT
AC/HDA_SDIN0
AC/HDA_SDIN1
AC/HDA_SDIN2
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GPI1
GPI2
GPI3
GPO0
GPO1
GPO2
GPO3
RSVD_0
RSVD_1
RSVD_2
RSVD_3
WDT
SPKR
I2C_CK
I2C_DAT
RS1_TX
RS1_RX
RS2_TX
RS2_RX
PCIE_RX5+
PCIE_RX5-
PCIE_TX5+
PCIE_TX5-
PCIE_RX4+
PCIE_RX4-
PCIE_TX4+
PCIE_TX4-
PCIE_RX3+
PCIE_RX3-
PCIE_TX3+
PCIE_TX3-
PCIE_RX2+
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PCIE_TX2-
PCIE_RX1+
PCIE_RX1-
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T_R124
A16_SATA0_TX+
A17_SATA0_TX-
A19_SATA0_RX+
A20_SATA0_RX-
B27_WDT
C24_DDI1_HPD
AUX_P
AUX_N
T_LVDS_I2C_CK
T_LVDS_I2C_DAT
T_LVDS_A0+
T_LVDS_A0-
T_LVDS_A1+
T_LVDS_A1-
T_LVDS_A2+
T_LVDS_A2-
T_LVDS_A3+
T_LVDS_A3-
T_LVDS_A_CK+
T_LVDS_A_CK-
B89_VGA_RED
B91_VGA_GRN
B92_VGA_BLU
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B96_VGA_I2C_DAT
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Title
ROWA/B
Size
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Document Number
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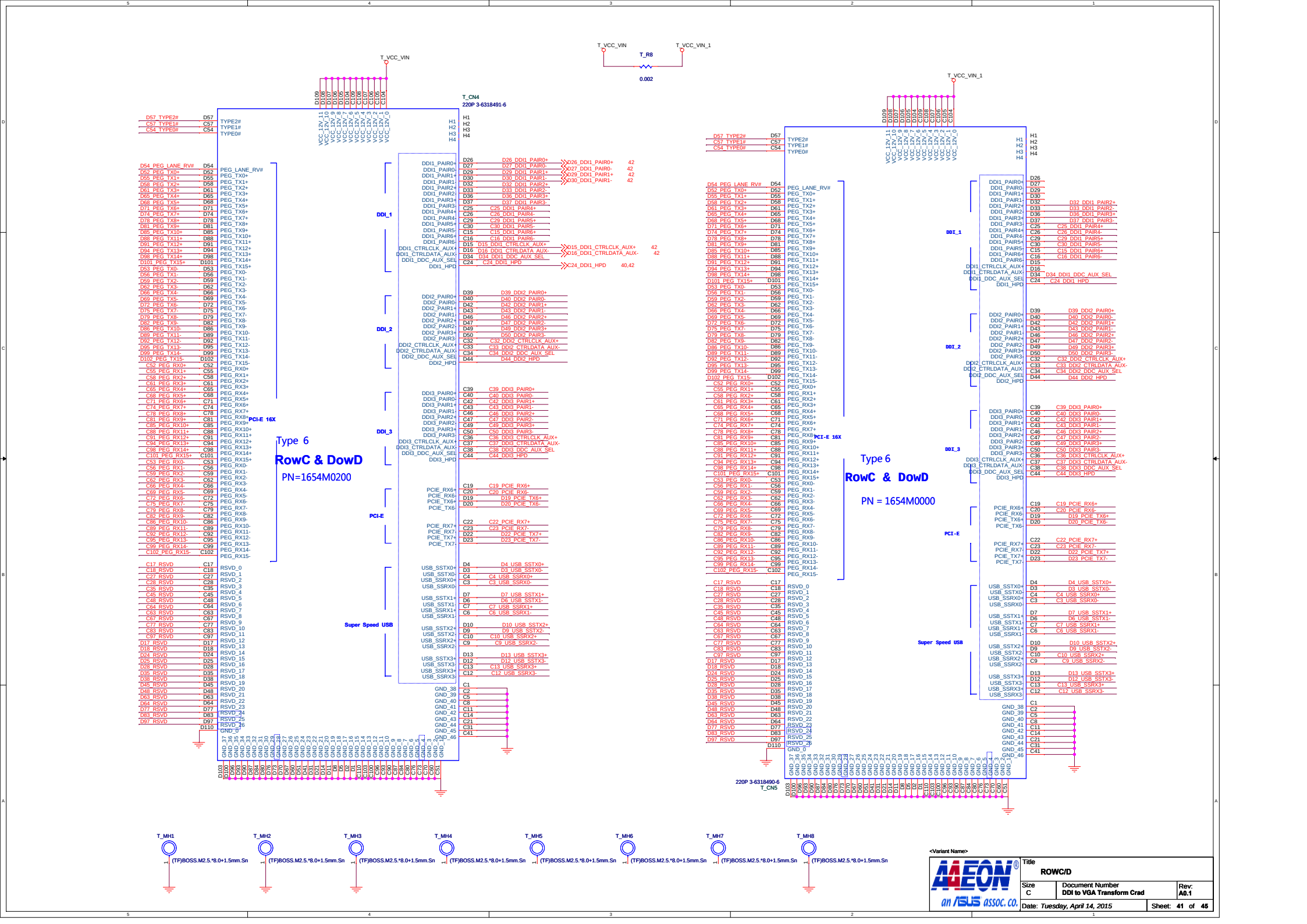
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DDI_2
DDI_3
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T_MH4
T_MH5
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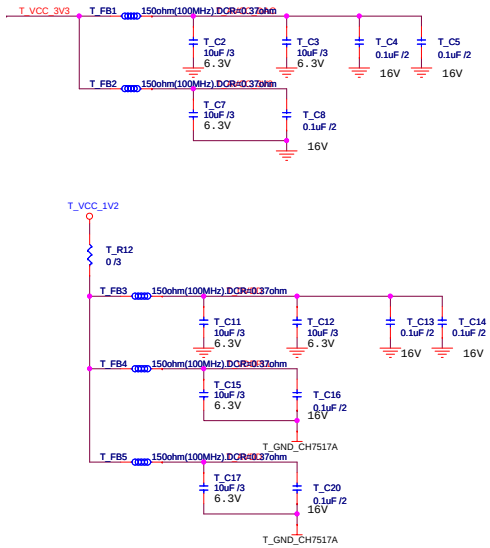
CH7517



Note:
1. +1.05V power spply tolerance range -5%~+25%
2. +3.3V power spply tolerance range +/-10%

Note : CH7517 RESET# PIN Sequence

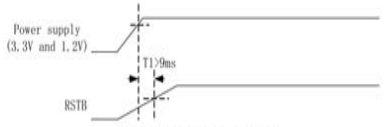


Figure 3: Power on and reset timing of RC

Another method is using an external reset signal. In this case, the power supply should be valid and stable for at least 9ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in **Figure 4.**

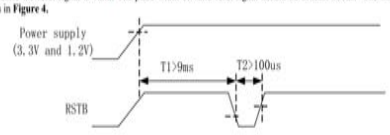
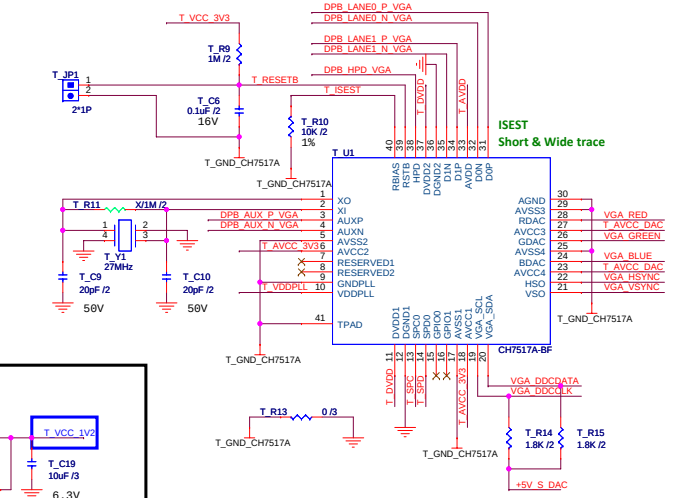
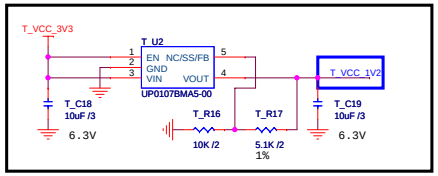


Figure 4: Power on and reset timing of external reset

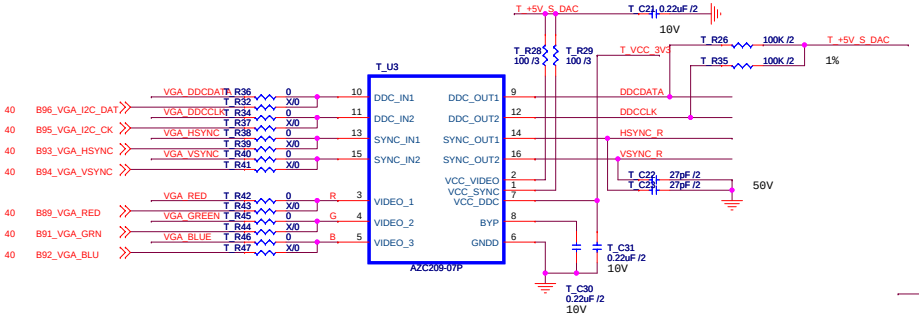
Note: 1. The power supply will be valid when it rises to 90% of standard level.
2. The rising threshold of RSTB is 2.4V.
3. The falling threshold of RSTB is 0.4V.



Reserve for Test

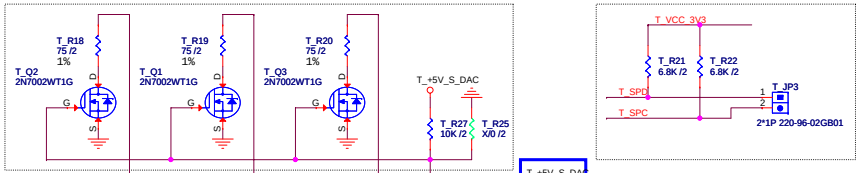


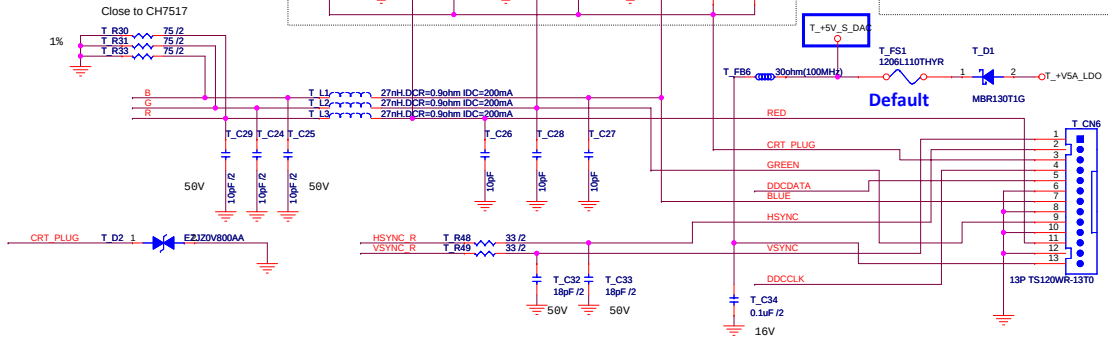
VGA

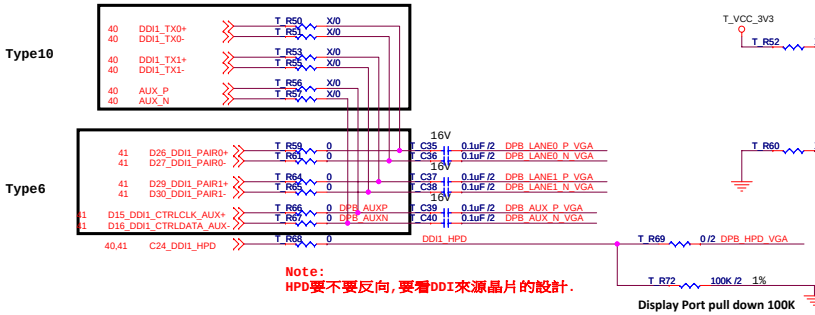


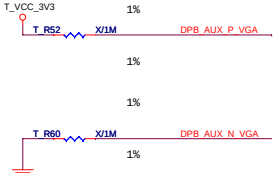
Note : Dammy load for CRT Always-On feature supporting.

Optional for firmware update









Note:
HPD要不要反向,要看DDI來源晶片的設計.

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Title: DDI to VGA		
Size: C	Document Number: DDI to VGA Transform Crad	Rev: A0.1
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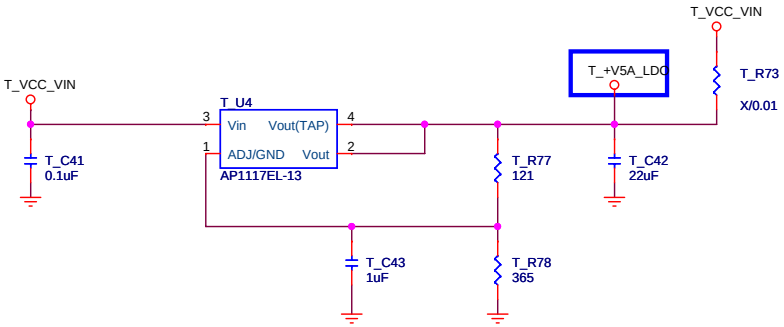

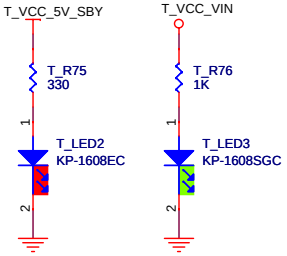

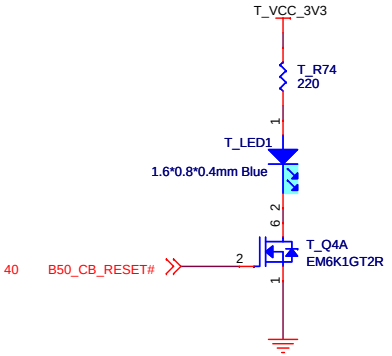

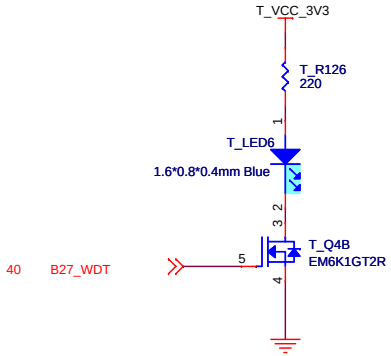

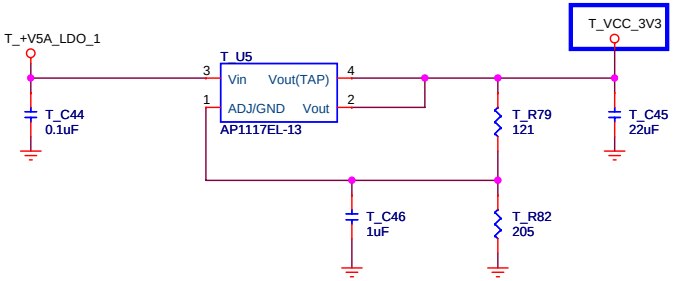

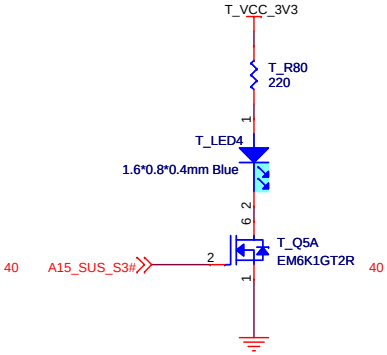

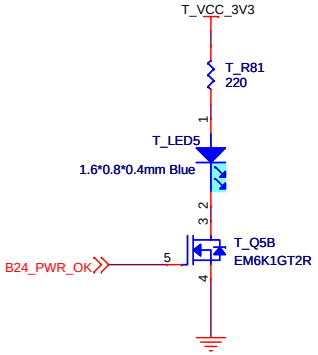

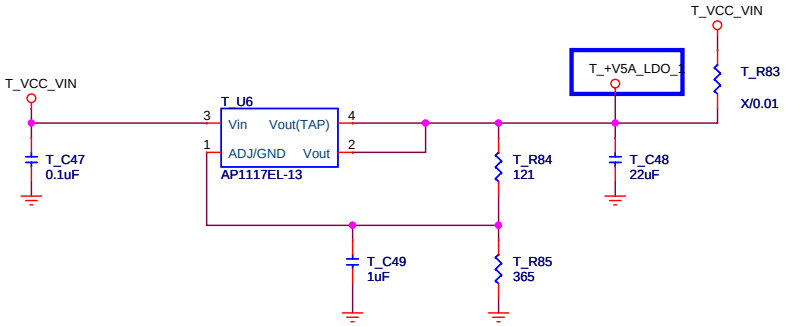

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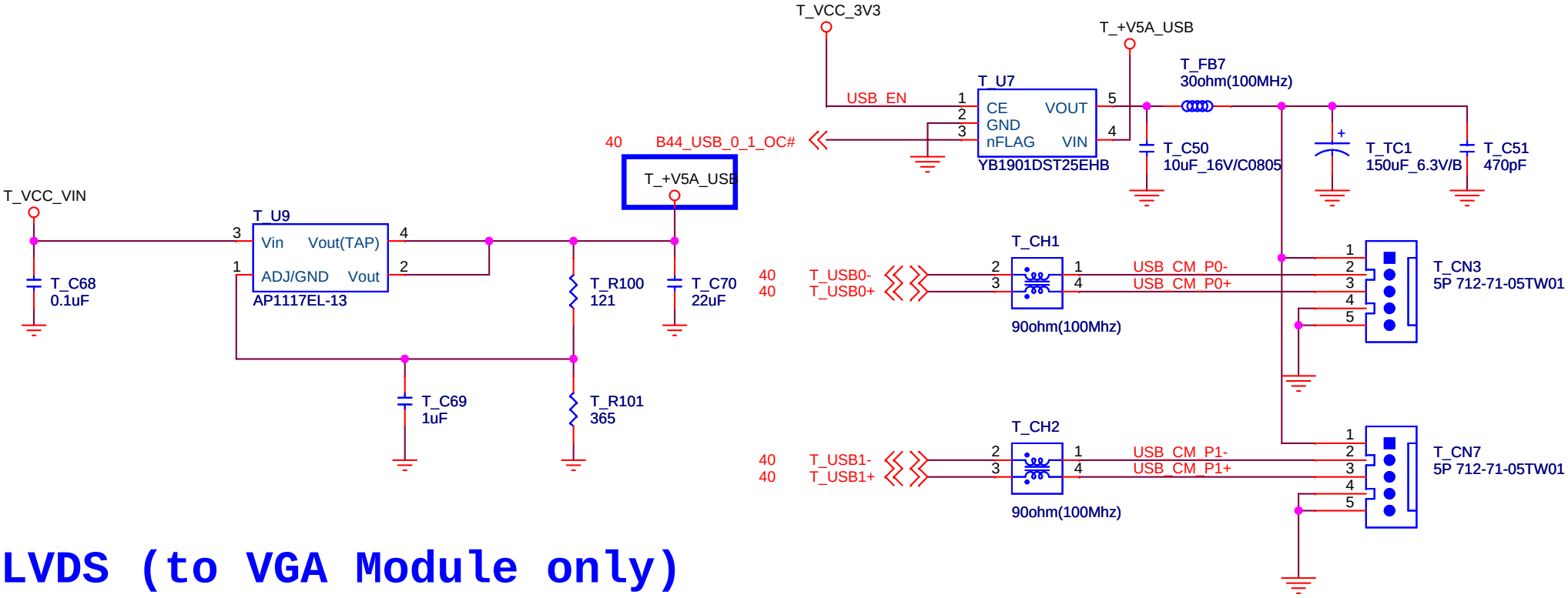
USB (KB/MS Only)



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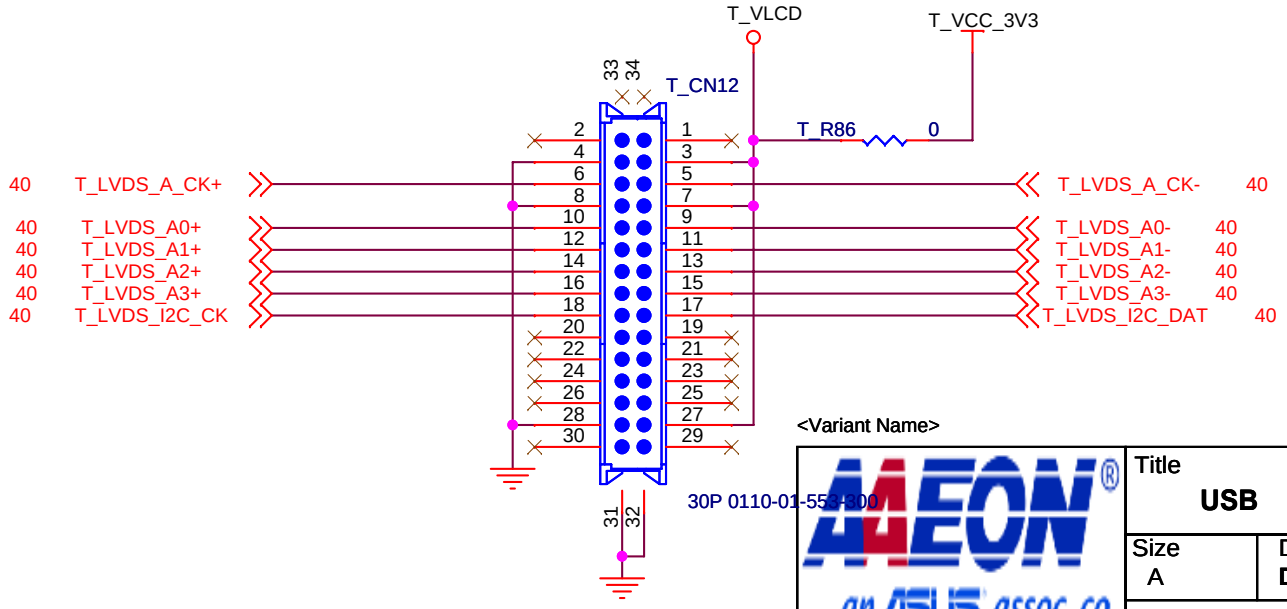

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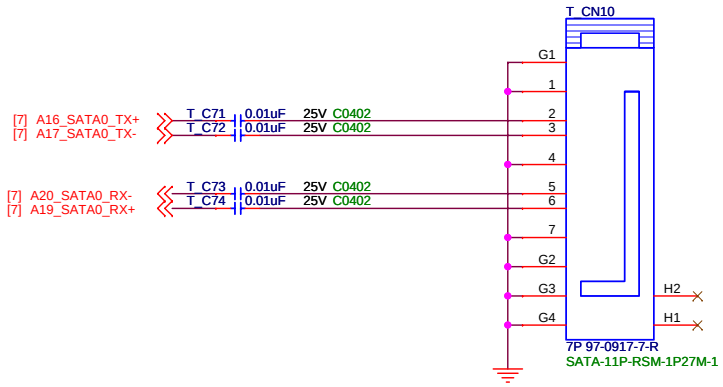

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