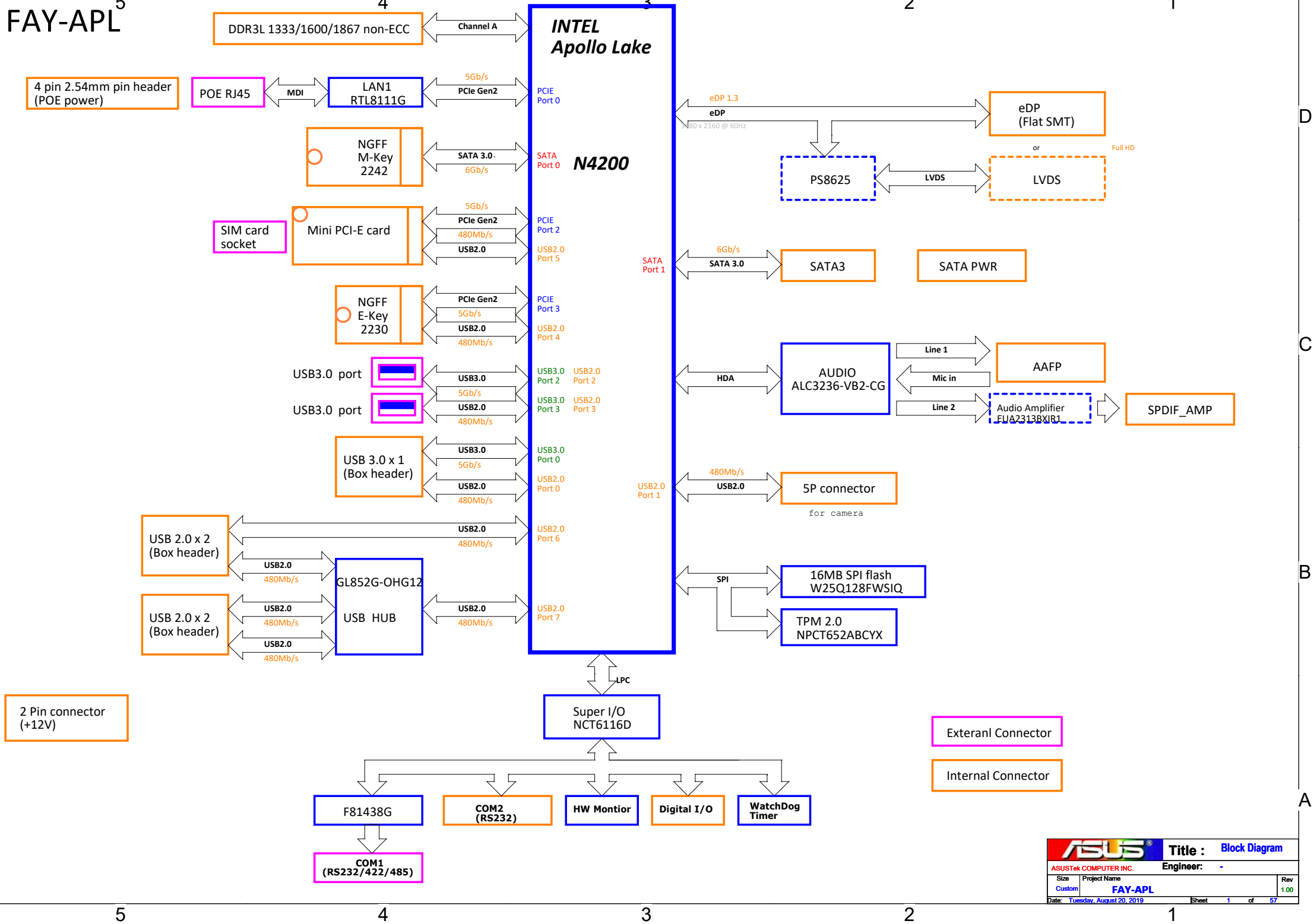
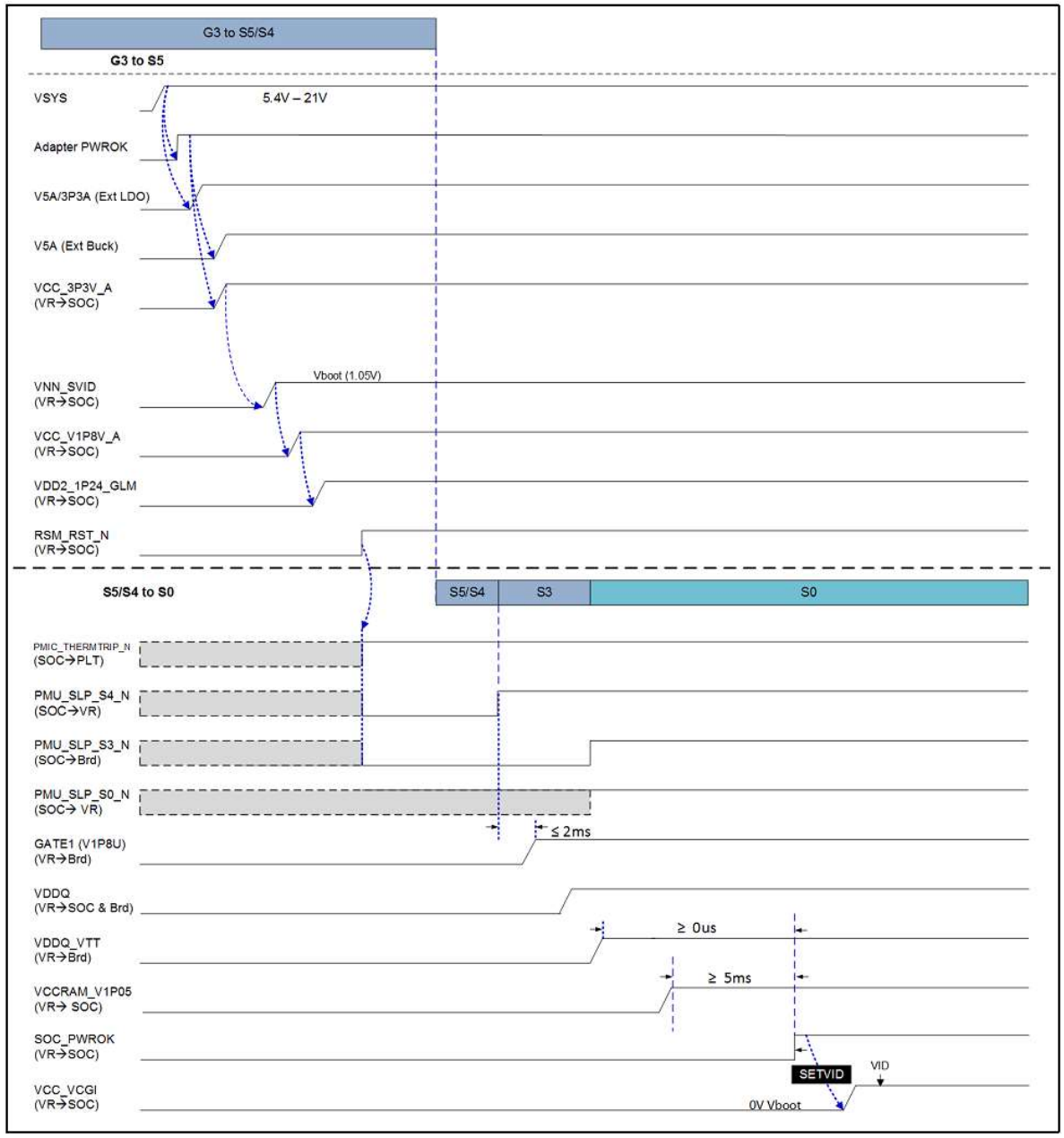
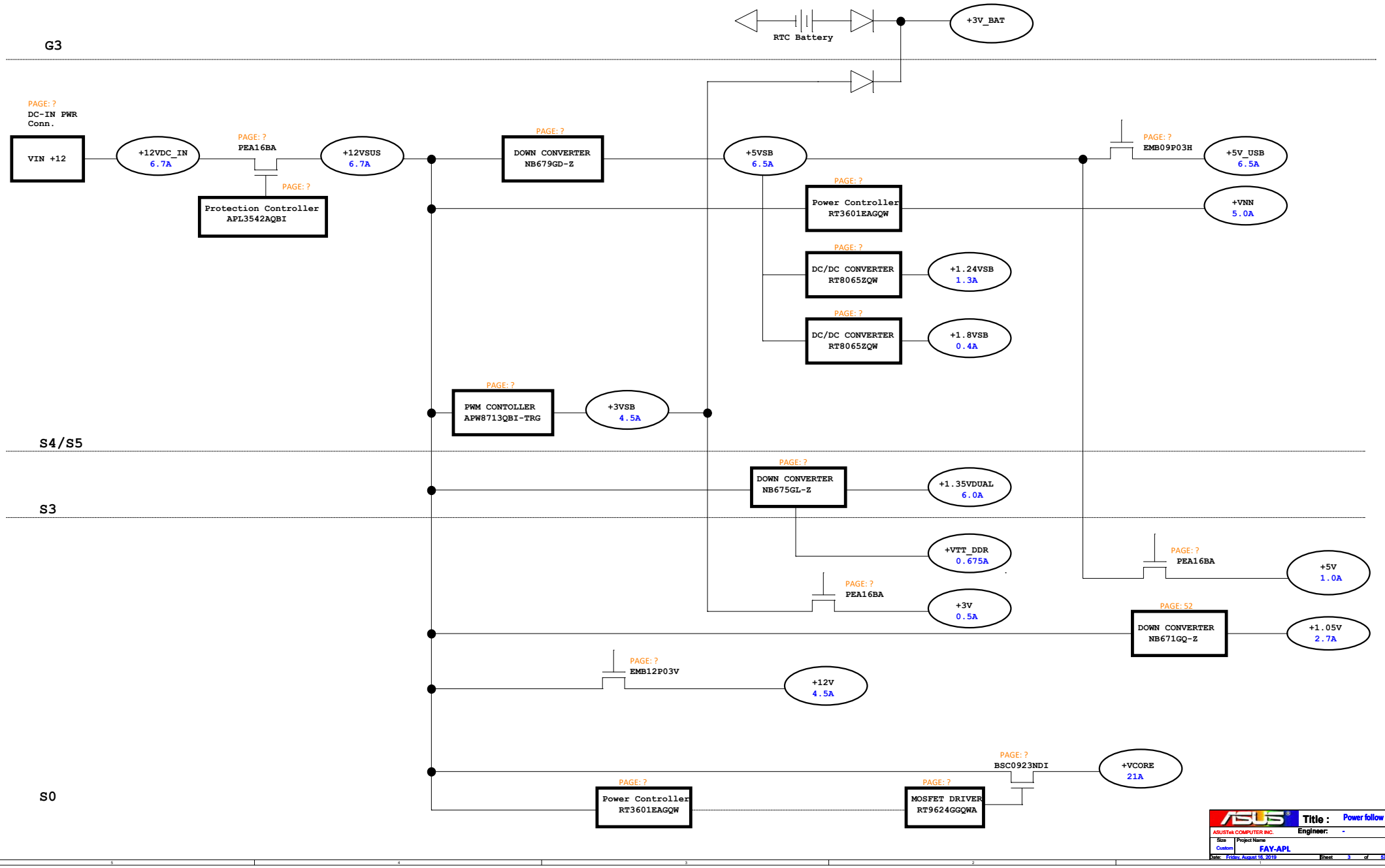
FAY-APL



Title :	Block Diagram
ASUSTek COMPUTER INC.	Engineer: -
Size: Custom	Project Name: FAY-APL
Rev	1.00
Date: Tuesday, August 20, 2019	Sheet 1 of 57



ASUSTek COMPUTER INC.	Title : Power ON seqence	
	Engineer: -	
Size: Custom	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 2 of 57	


G3
RTC Battery
+3V_BAT
PAGE: ?
DC-IN PWR Conn.
VIN +12
+12VDC_IN
6.7A
PAGE: ?
PEA16BA
+12VSUS
6.7A
PAGE: ?
Protection Controller
APL3542AQBI
PAGE: ?
DOWN CONVERTER
NB679GD-Z
+5VSB
6.5A
PAGE: ?
Power Controller
RT3601EAGQW
PAGE: ?
DC/DC CONVERTER
RT8065ZQW
+1.24VSB
1.3A
PAGE: ?
DC/DC CONVERTER
RT8065ZQW
+1.8VSB
0.4A
PAGE: ?
EMB09P03H
+5V_USB
6.5A
+VNN
5.0A
PAGE: ?
PWM CONTOLLER
APW8713QBI-TRG
+3VSB
4.5A
S4/S5
S3
PAGE: ?
DOWN CONVERTER
NB675GL-Z
+1.35VDUAL
6.0A
+VTT_DDR
0.675A
PAGE: ?
PEA16BA
+3V
0.5A
PAGE: ?
PEA16BA
+5V
1.0A
PAGE: 52
DOWN CONVERTER
NB671GQ-Z
+1.05V
2.7A
PAGE: ?
EMB12P03V
+12V
4.5A
S0
PAGE: ?
BSC0923NDI
+VCORE
21A
PAGE: ?
Power Controller
RT3601EAGQW
PAGE: ?
MOSFET DRIVER
RT9624GGQWA
ASUSTeK COMPUTER INC.
Title : Power follow
Engineer: -
Size: Custom
Project Name: FAY-APL
Rev: 1.00
Date: Friday, August 16, 2019
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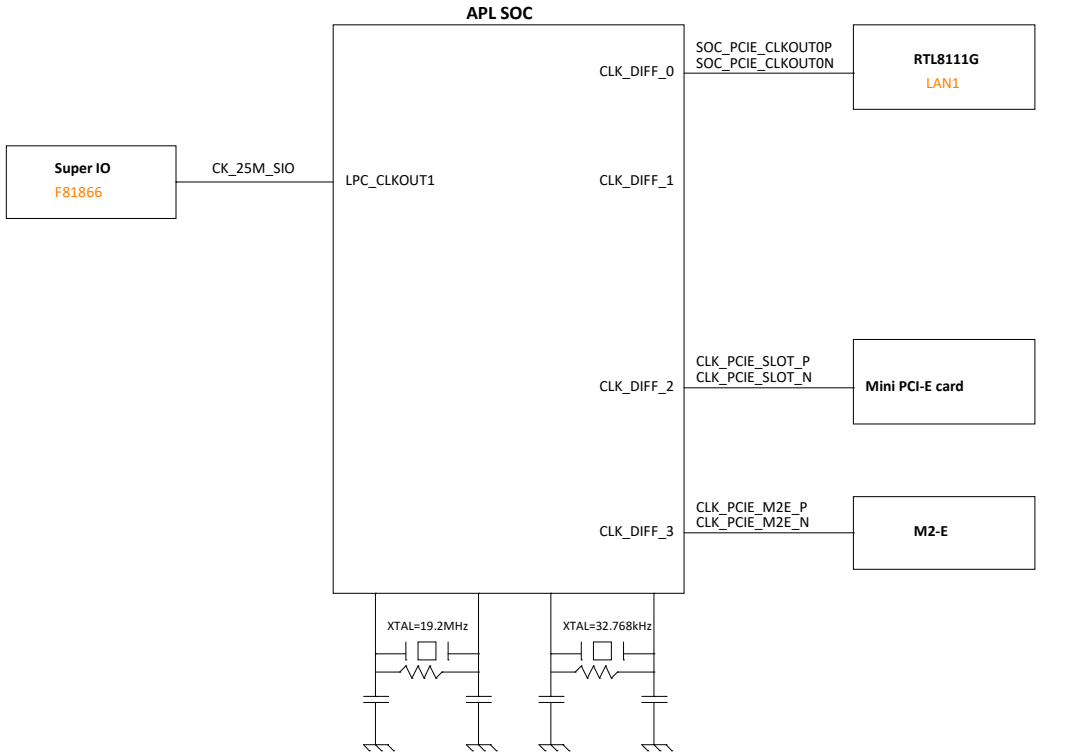

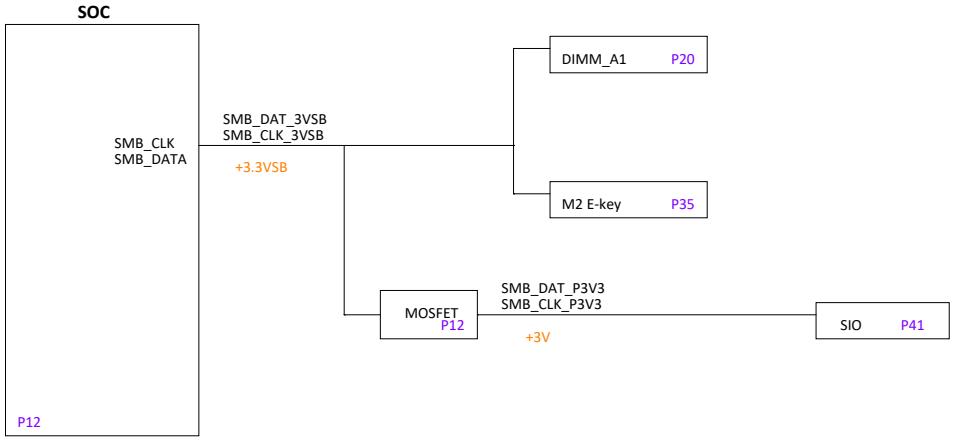

ASUSTek COMPUTER INC.	Title : CLK/I2C map	
	Engineer: -	
Size: Custom	Project Name: FAY-APL	Rev: 1.00
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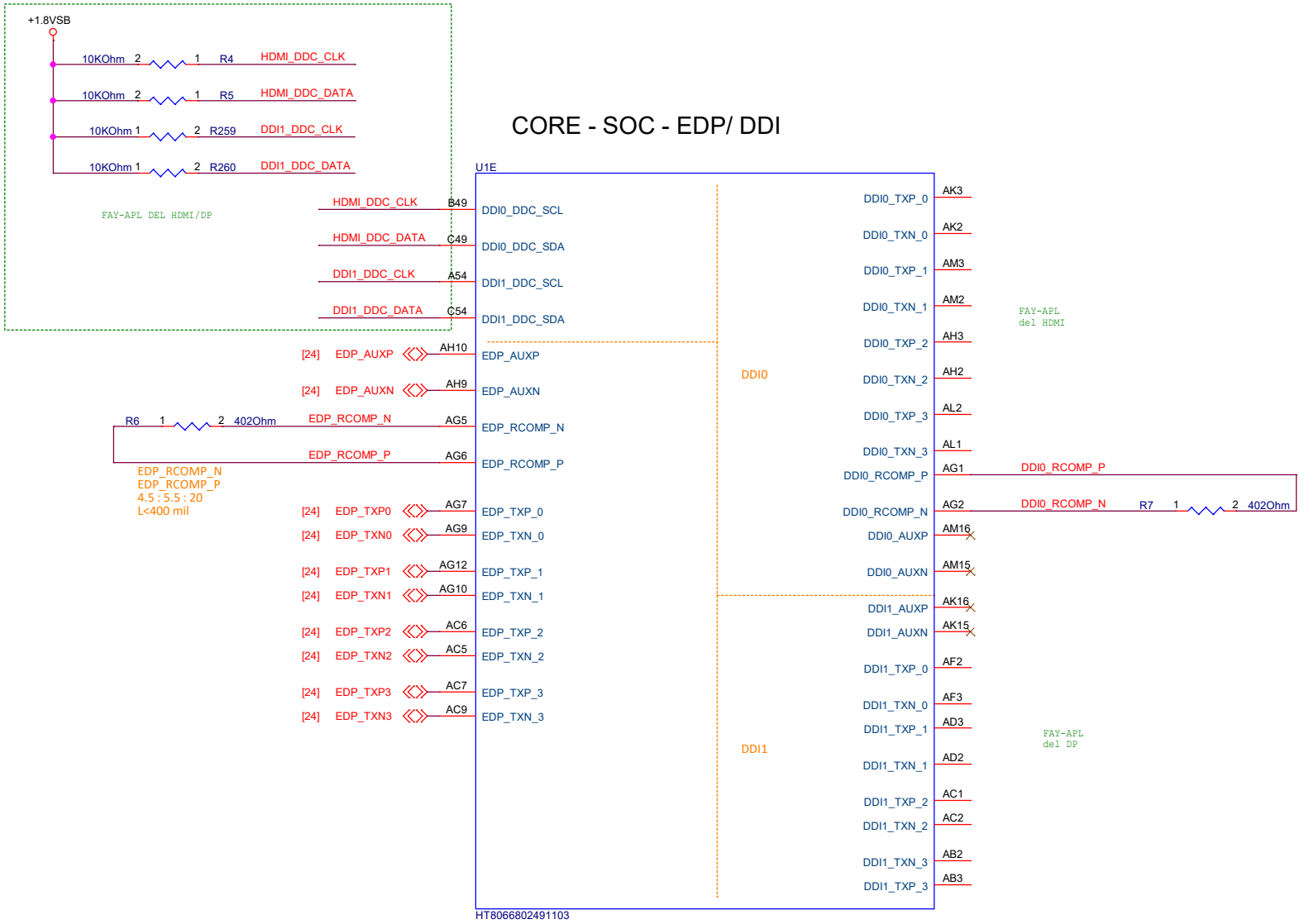
CORE - SOC - EDP/ DDI



ASUSTek COMPUTER INC.	Title : SOC-3(DDI/EDP)	
	Engineer: -	
Size: B	Project Name: FAY-APL	Rev: 1.00
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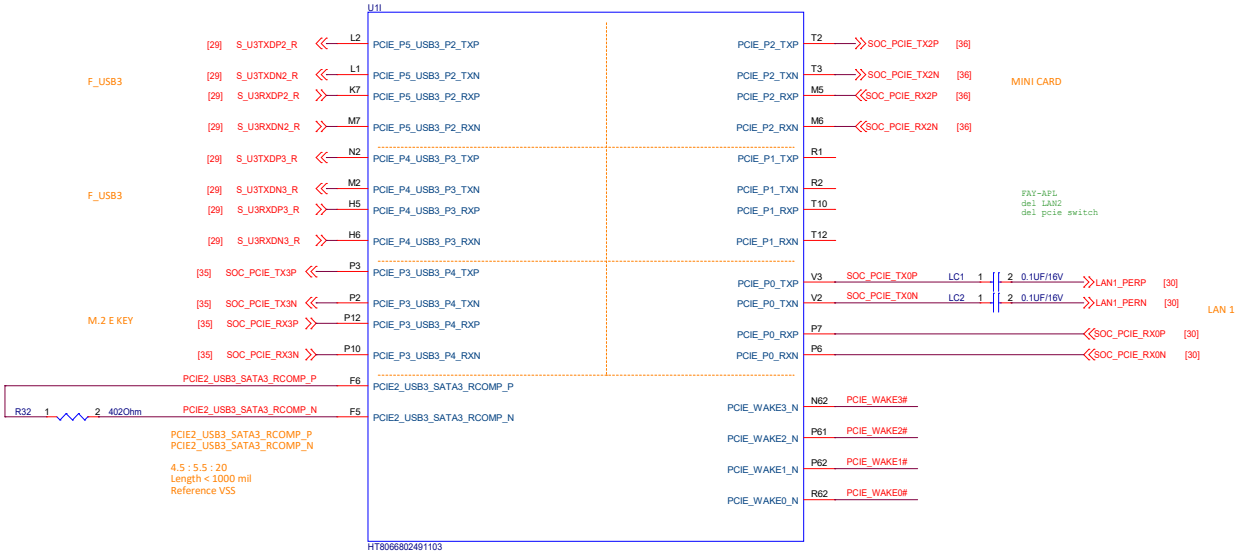
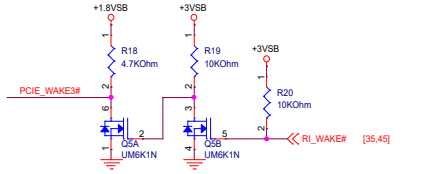
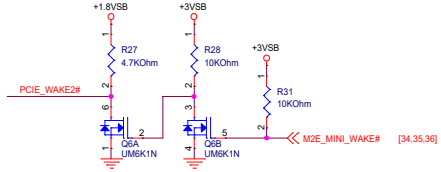
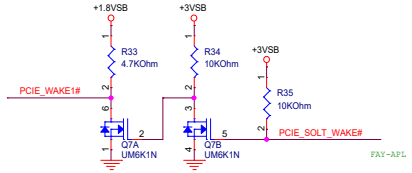
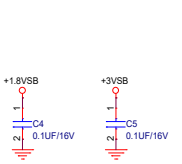
CORE - SOC - PCIE/SATA/USB3

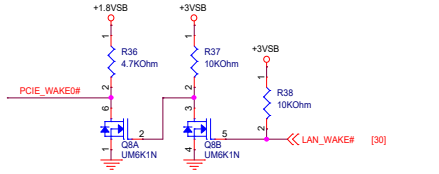




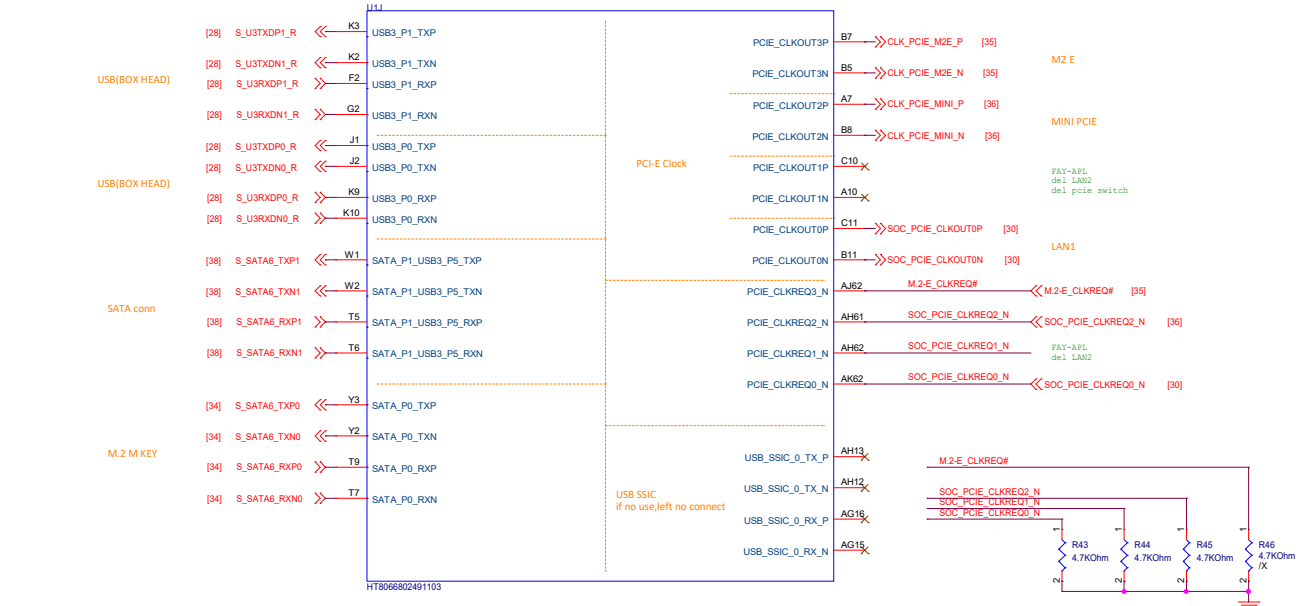








CORE - SOC - SSIC/USB3/SATA



ASUSTek COMPUTER INC.	Title : SOC-6(PCIE/SATA/USB3)	
	Engineer: -	
Size: C	Project Name: FAY-APL	Rev: 1.00
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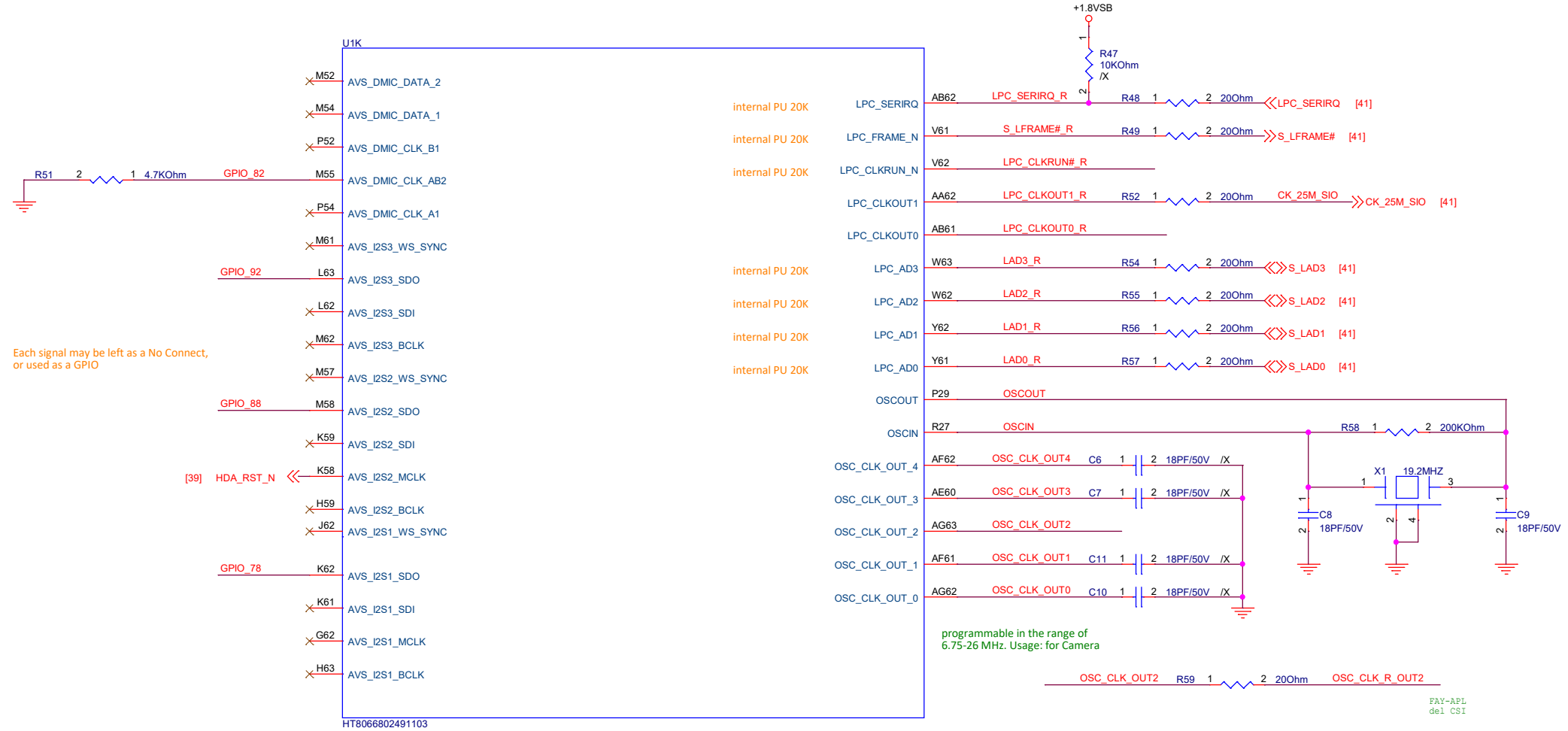
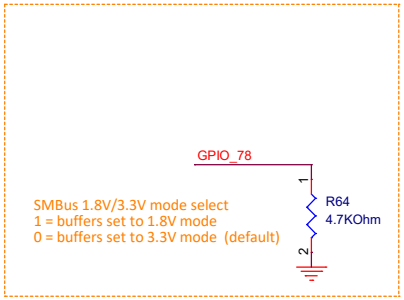
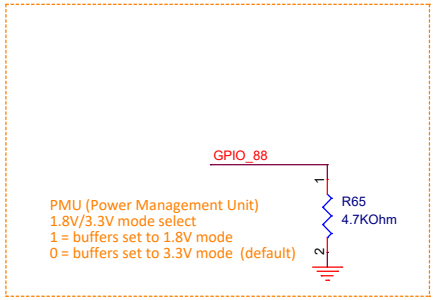
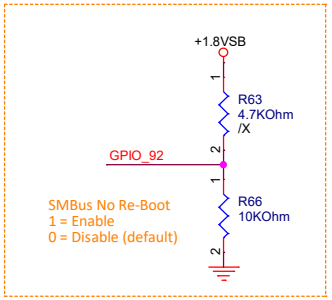
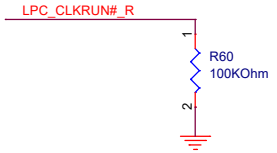
CORE - SOC - I2S/LPC/CLOCKS

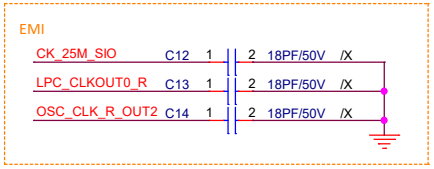












ASUSTek COMPUTER INC.

Title : SOC-7(LPC/CLOCK)

Engineer: -

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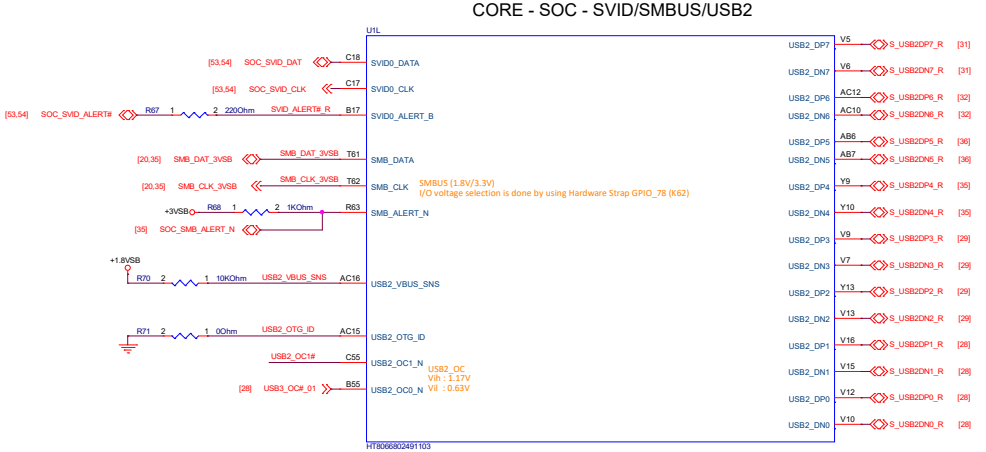
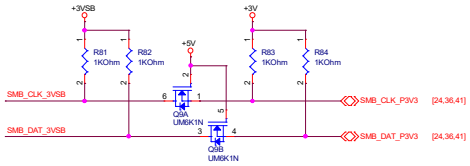
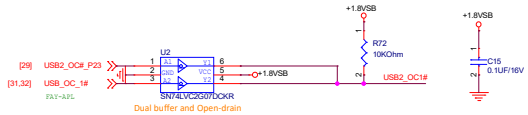
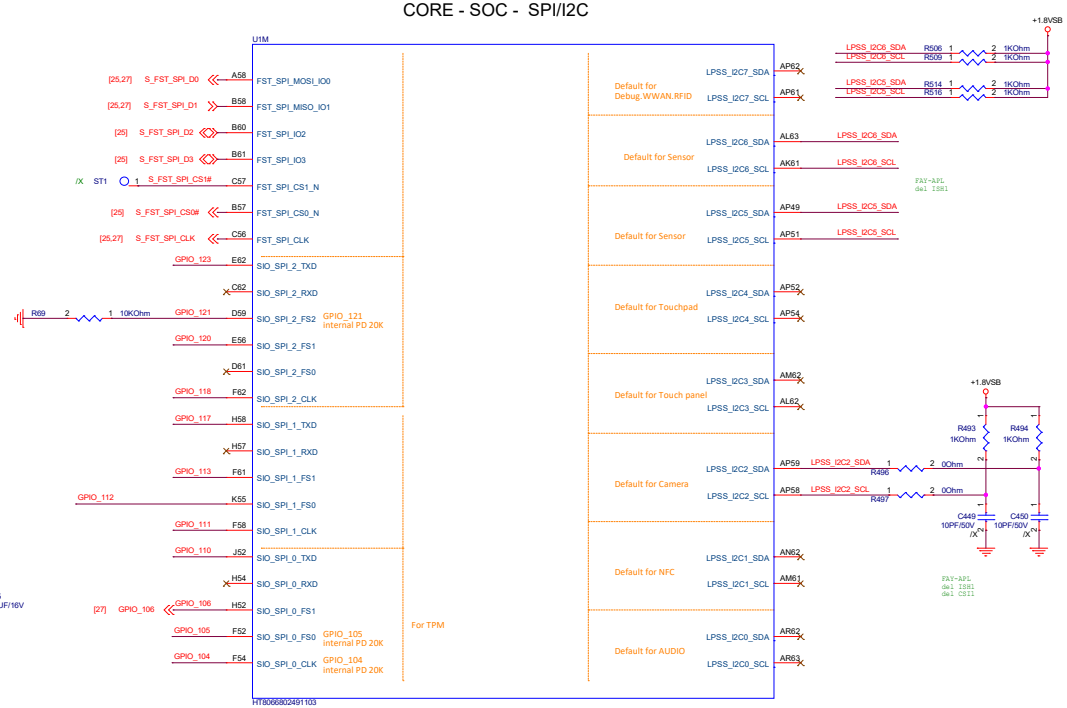
CORE - SOC - SVID/SMBUS/USB2

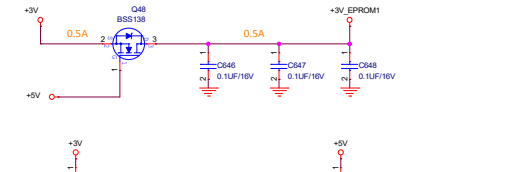


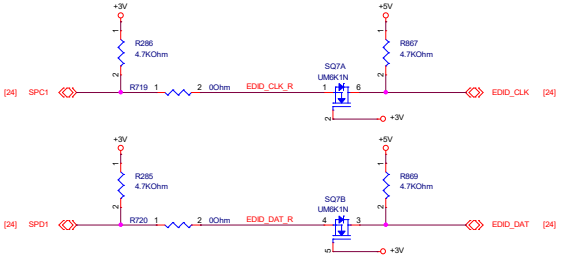


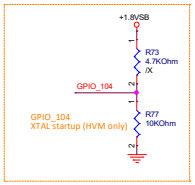


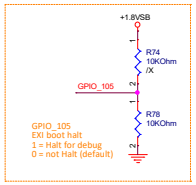
CORE - SOC - SPI/I2C

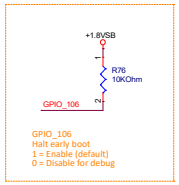


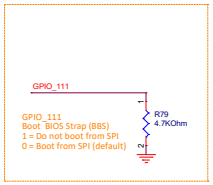


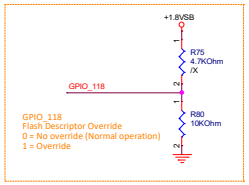


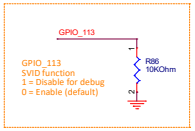


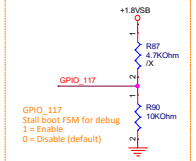


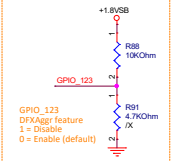


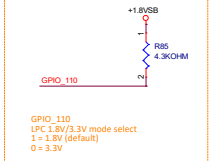


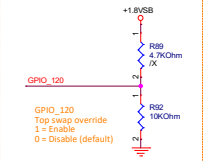


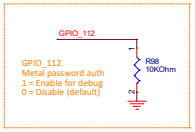












ASUSTek COMPUTER INC.	Title : SOC-8(SVID/SMBUS/USB2/I2C)	
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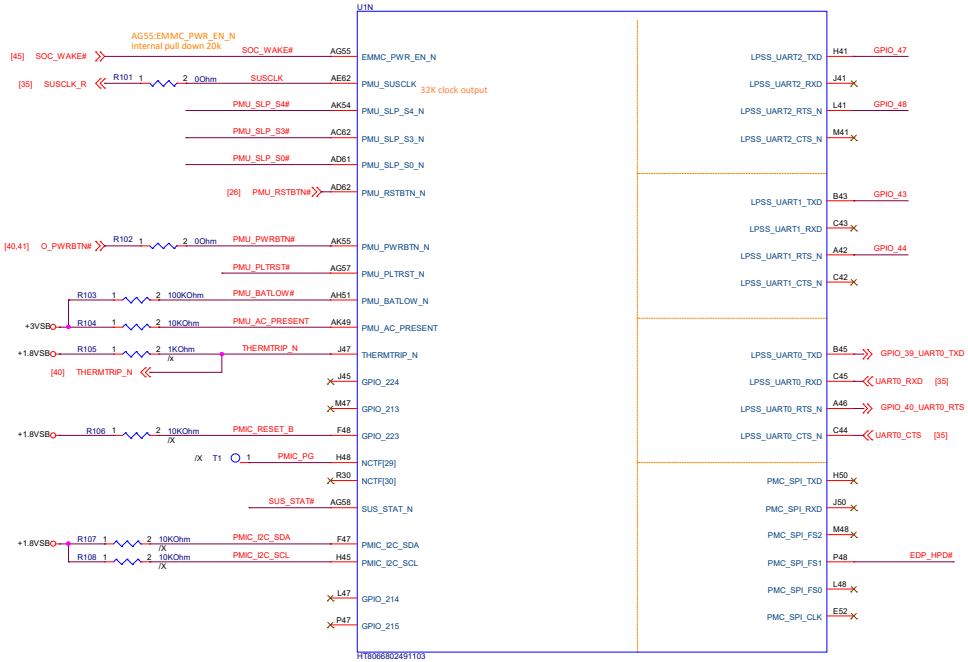
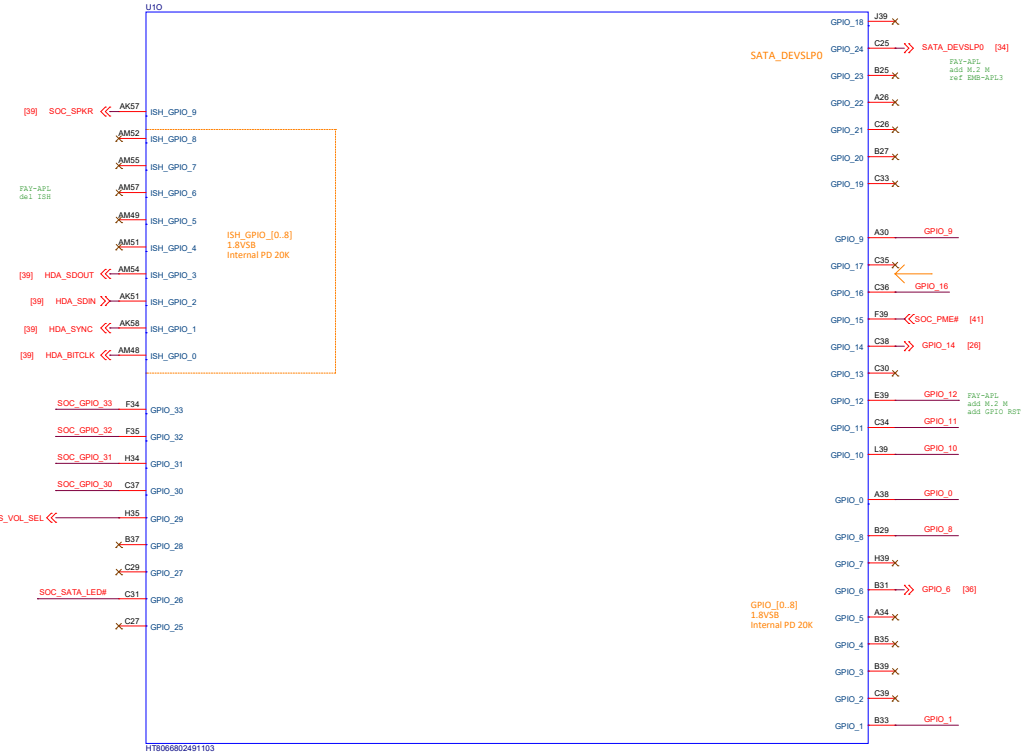
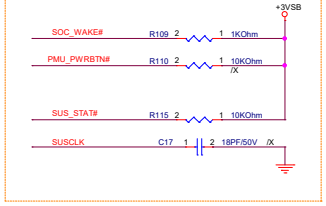
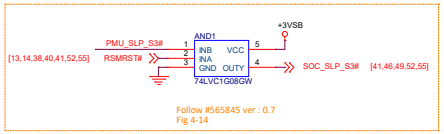
CORE - SOC - PMU/UART

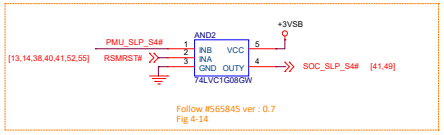


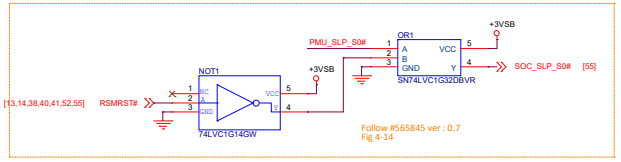
CORE - SOC - GPIO/ISH

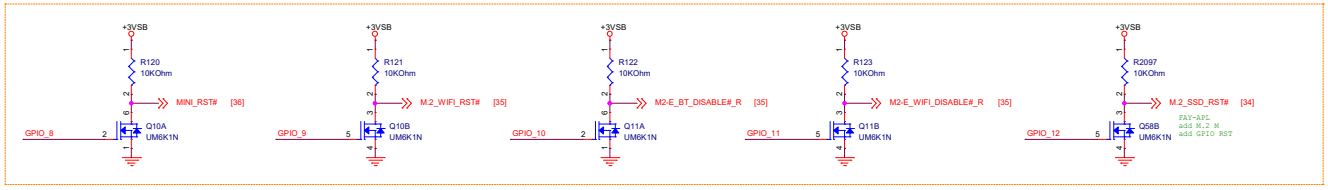


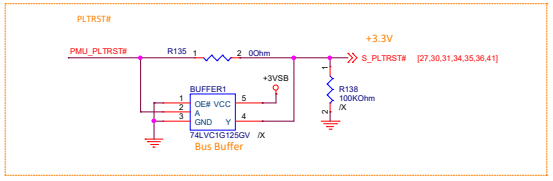


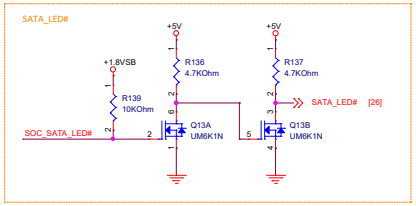


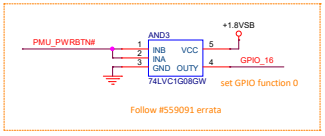


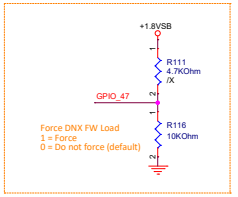


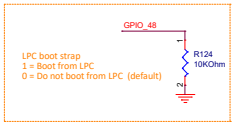


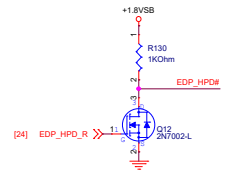


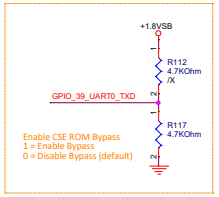


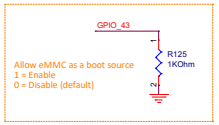


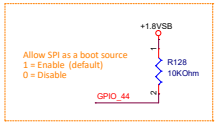


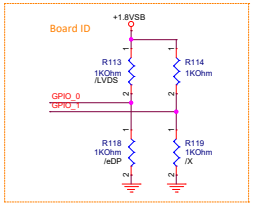


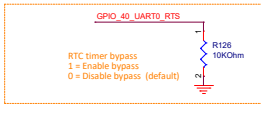


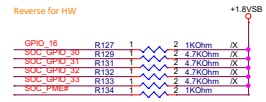












ASUSTeK COMPUTER INC.

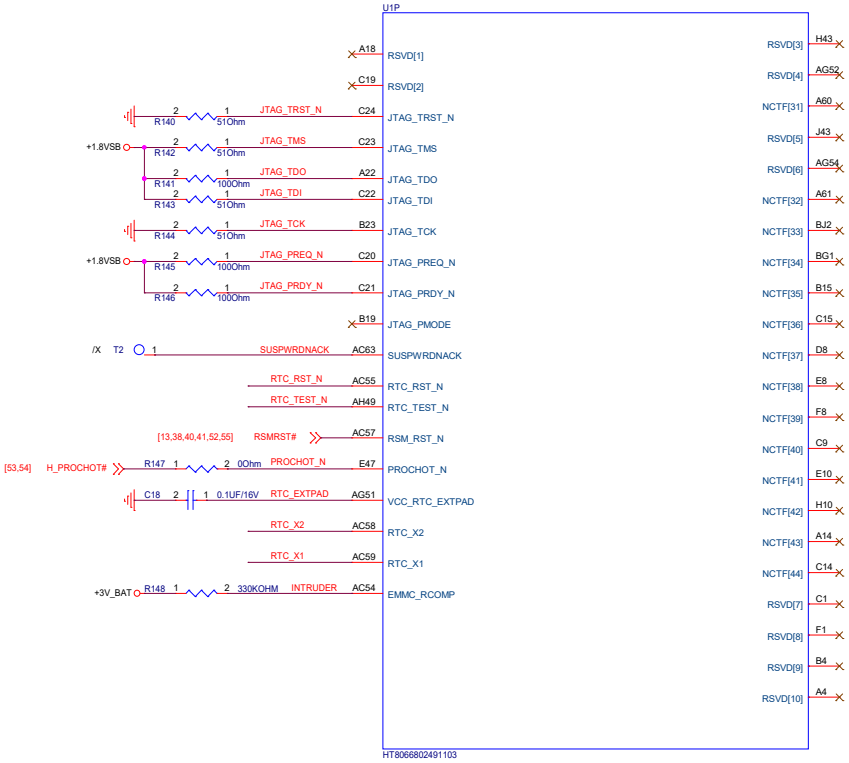
Title : SOC-9(UART/GPIO)

Engineer: -

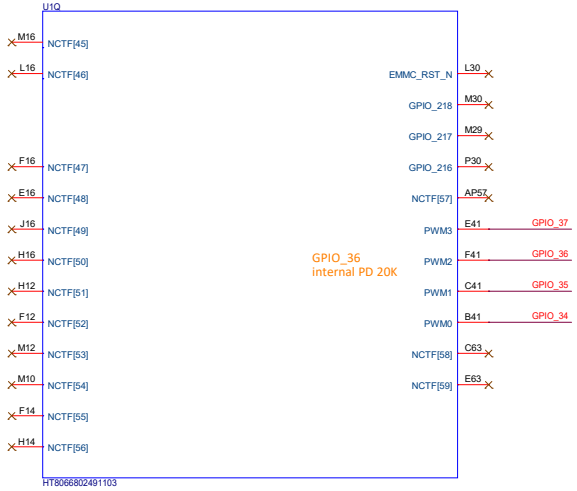
Size	Project Name	Rev
Custom	FAY-APL	1.00

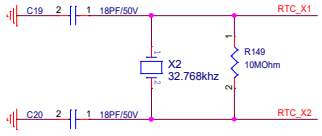
Date: Tuesday, October 15, 2019 Sheet 13 of 57

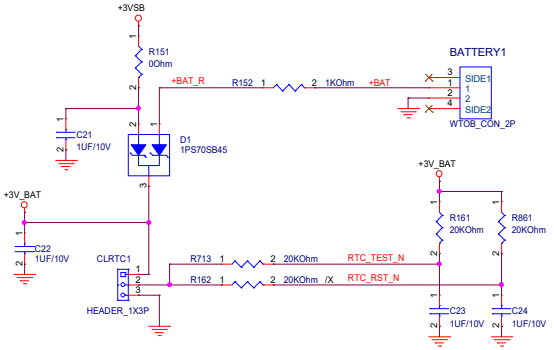
CORE - SOC - JTAG/OBS/THERMAL



CORE - SOC - CNV, PWM







BATTERY1_1

3V/220mAh

0B100-00020700

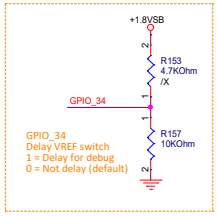
0B001-00010200

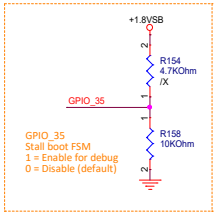
Temp:-30~+80

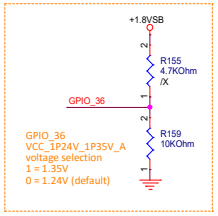
CLRTC1(1-2)1

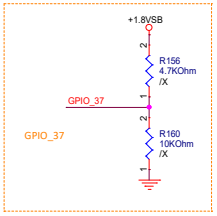
MINI_JUMPER

CLRTC1
1-2 : Normal (Default)
2-3 : Clear CMOS

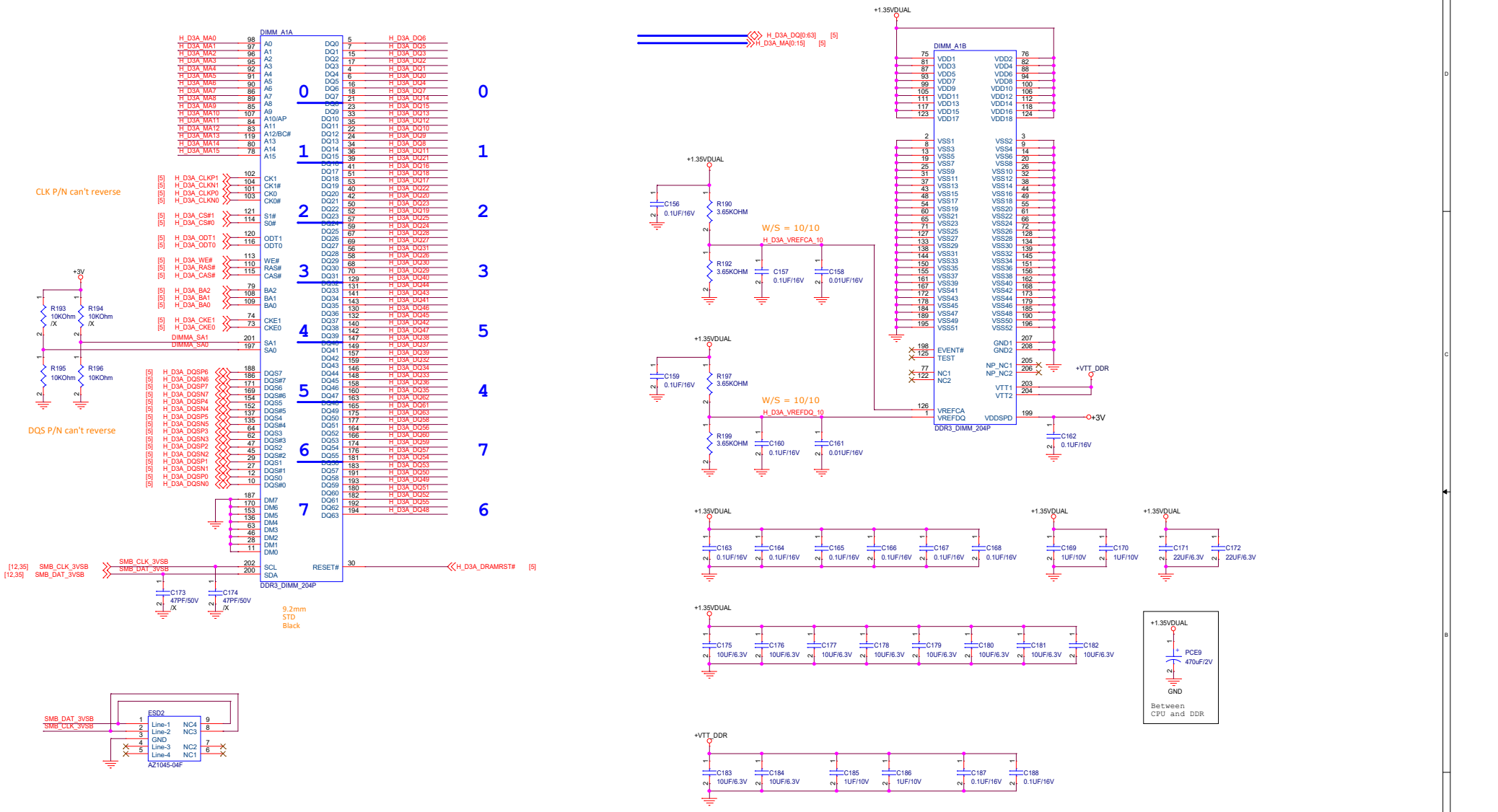




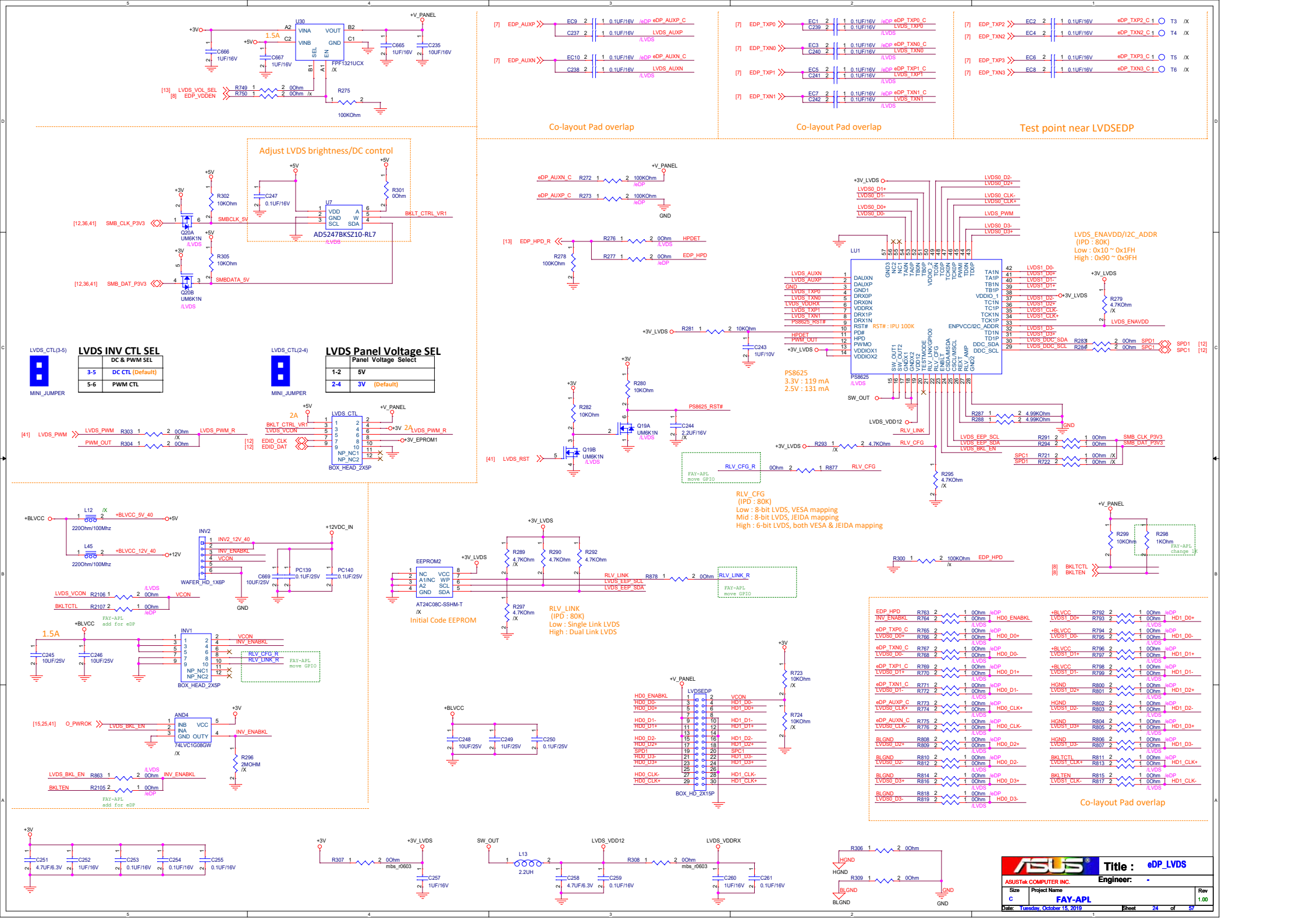




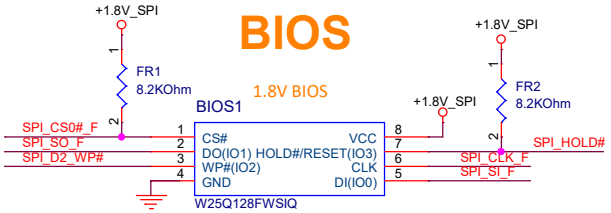
ASUSTek COMPUTER INC.	Title : SOC-10(JTAG)	
	Engineer: -	
Size: C	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 14 of 57	



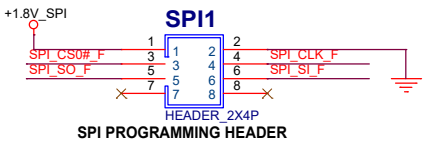
ASUSTek COMPUTER INC.	Title : DDR3L_CHA		
	Engineer: -		
Size: C	Project Name: FAY-APL		Rev: 1.00
Date: Friday, August 16, 2019	Sheet 20 of 57		


Adjust LVDS brightness/DC control
AD5247BKSZ10-RL7
LVDS INV CTL SEL
DC & PWM SEL
3-5 DC CTL (Default)
5-6 PWM CTL
LVDS Panel Voltage SEL
Panel Voltage Select
1-2 5V
2-4 3V (Default)
Co-layout Pad overlap
Co-layout Pad overlap
Test point near LVDSEDP
PS8625
3.3V : 119 mA
2.5V : 131 mA
LVDS_ENAVDD/I2C_ADDR
(IPD : 80K)
Low : 0x10 ~ 0x1FH
High : 0x90 ~ 0x9FH
RLV_CFG
(IPD : 80K)
Low : 8-bit LVDS, VESA mapping
Mid : 8-bit LVDS, JEIDA mapping
High : 6-bit LVDS, both VESA & JEIDA mapping
RLV_LINK
(IPD : 80K)
Low : Single Link LVDS
High : Dual Link LVDS
Initial Code EEPROM
Co-layout Pad overlap
Title : eDP_LVDS
Engineer: -
ASUSTek COMPUTER INC.
Project Name FAY-APL
Rev 1.00
Date: Tuesday, October 15, 2019
Sheet 24 of 57

BIOS

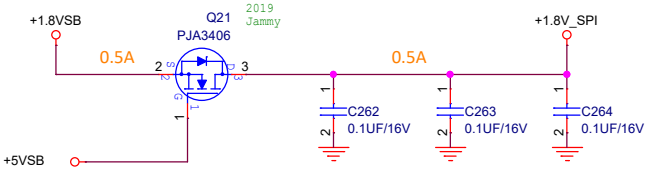


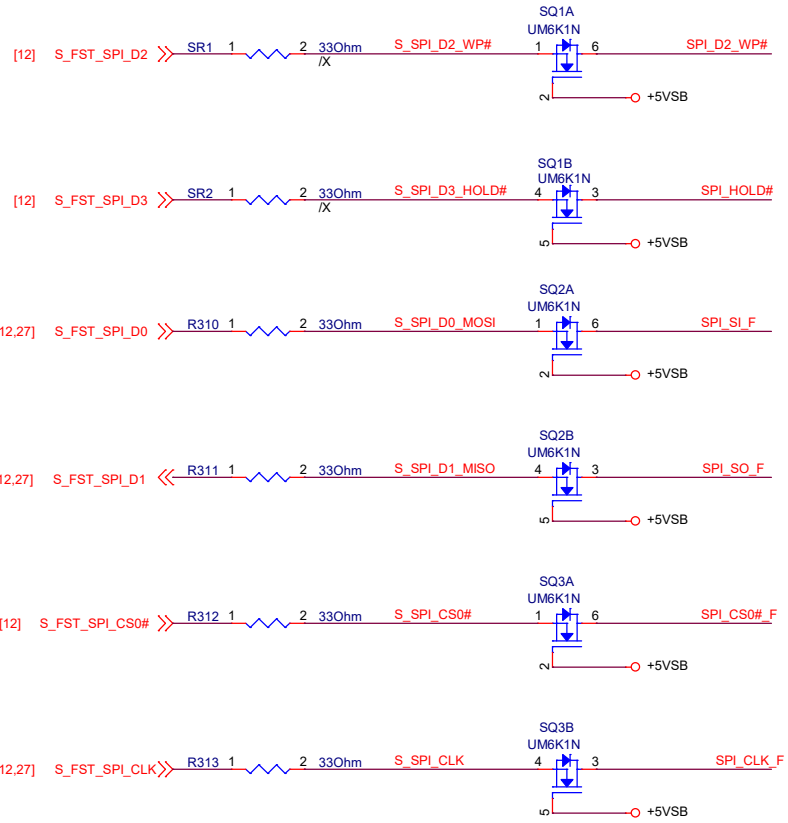
SPI Interface

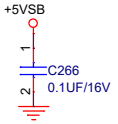


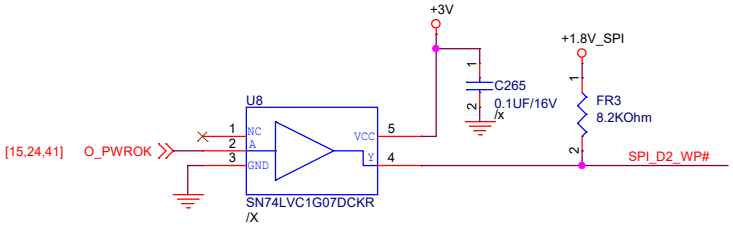
SPI PROGRAMMING HEADER

BIOS
max current : 25mA

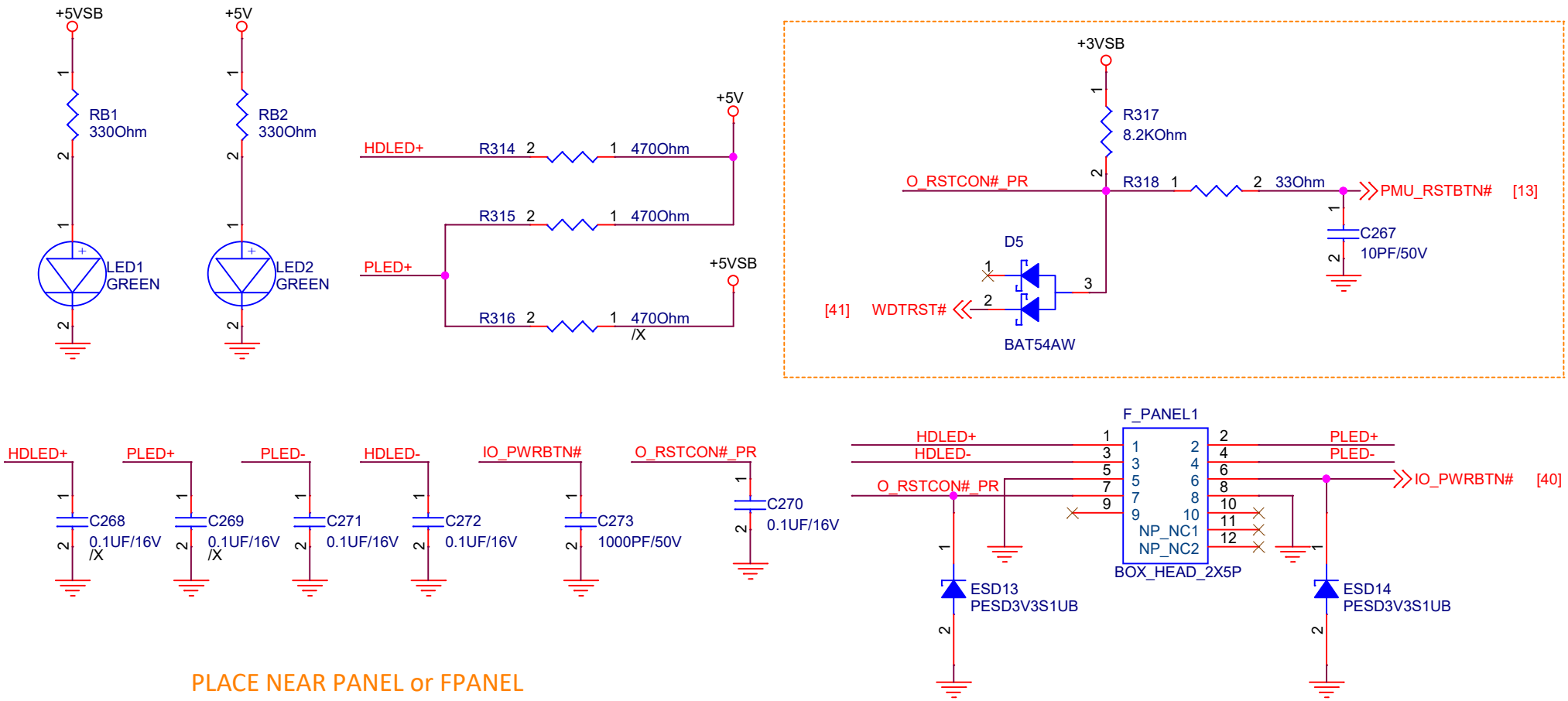




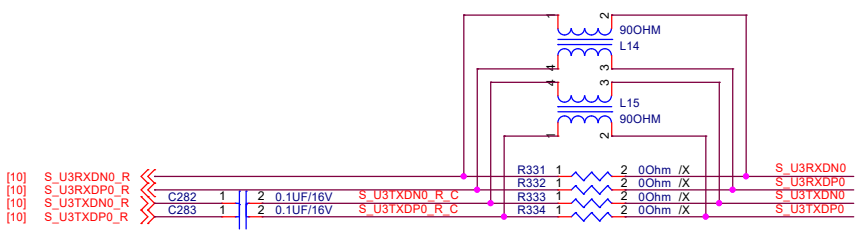


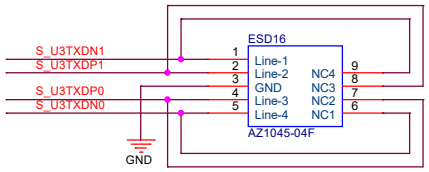


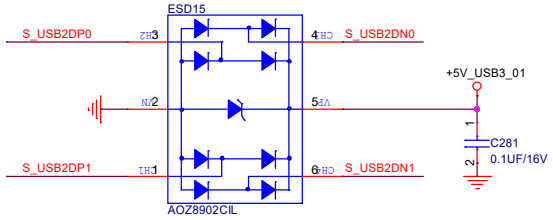
ASUSTek COMPUTER INC.	Title : SPI and BIOS		
	Engineer: -		
Size: B	Project Name: FAY-APL		Rev: 1.00
Date: Thursday, September 12, 2019	Sheet 25 of 57		

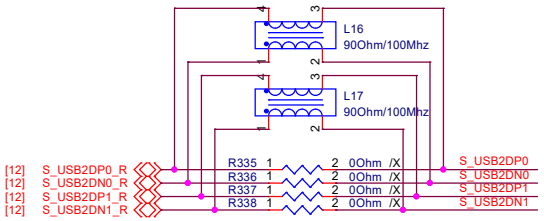


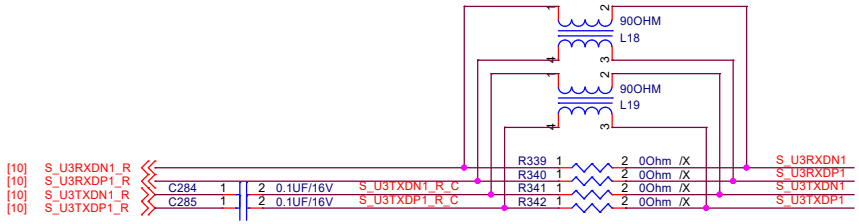
ASUSTek COMPUTER INC.	Title : Front panel	
	Engineer: -	
Size: A	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 26 of 57	

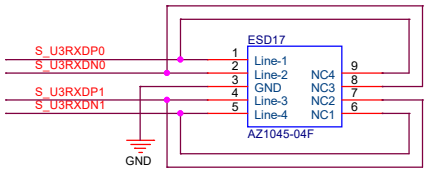


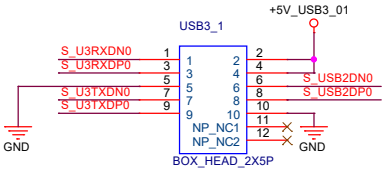


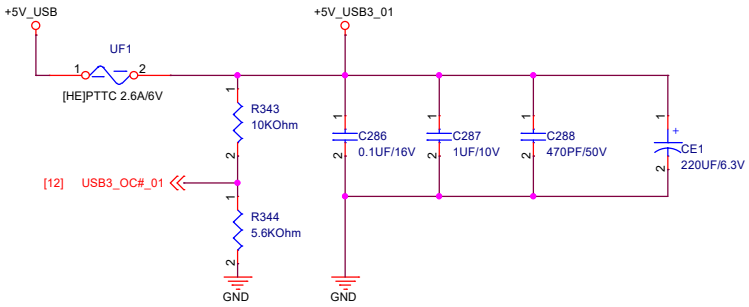


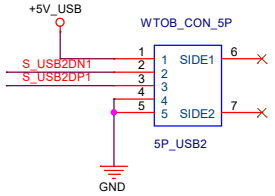






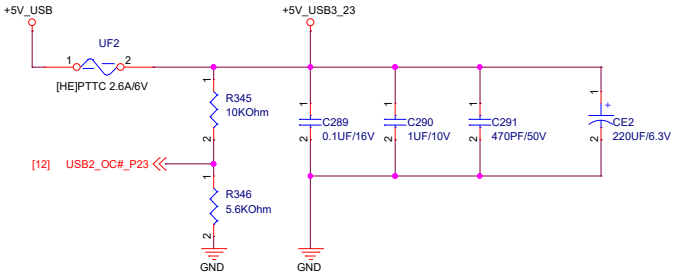


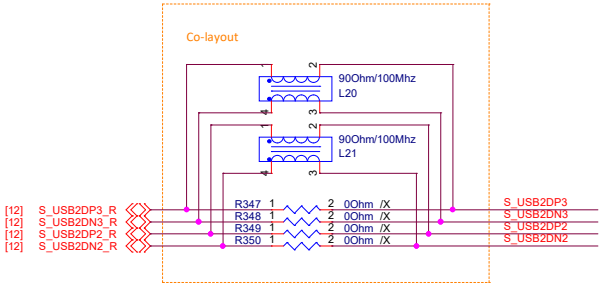


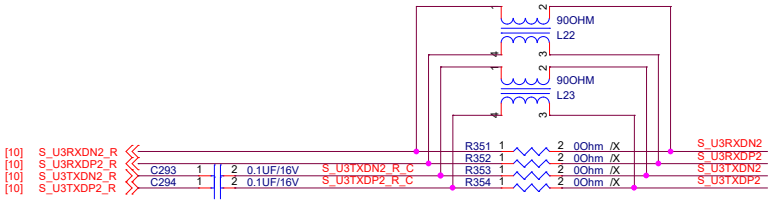


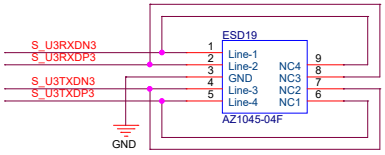
FAY-APL
change USB3 CONN.
add USB2 5P CONN.

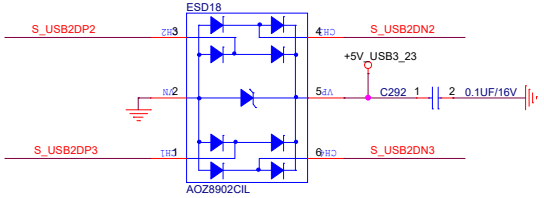
ASUSTek COMPUTER INC.	Title : USB3.0(BOX HEAD)	
	Engineer: -	
Size: A3	Project Name: FAY-APL	Rev: 1.00
Date: Monday, September 02, 2019	Sheet 28 of 57	

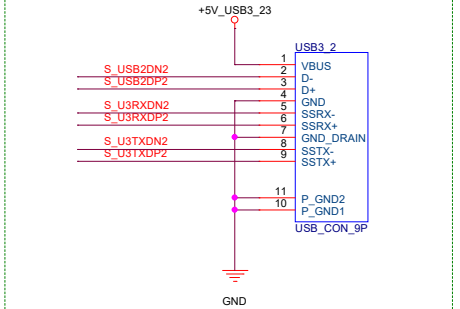


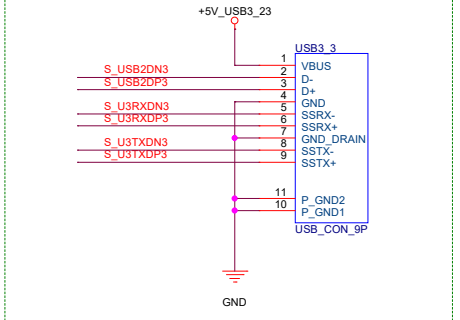




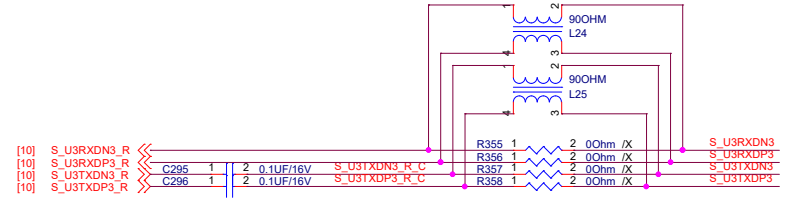


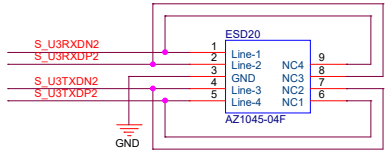






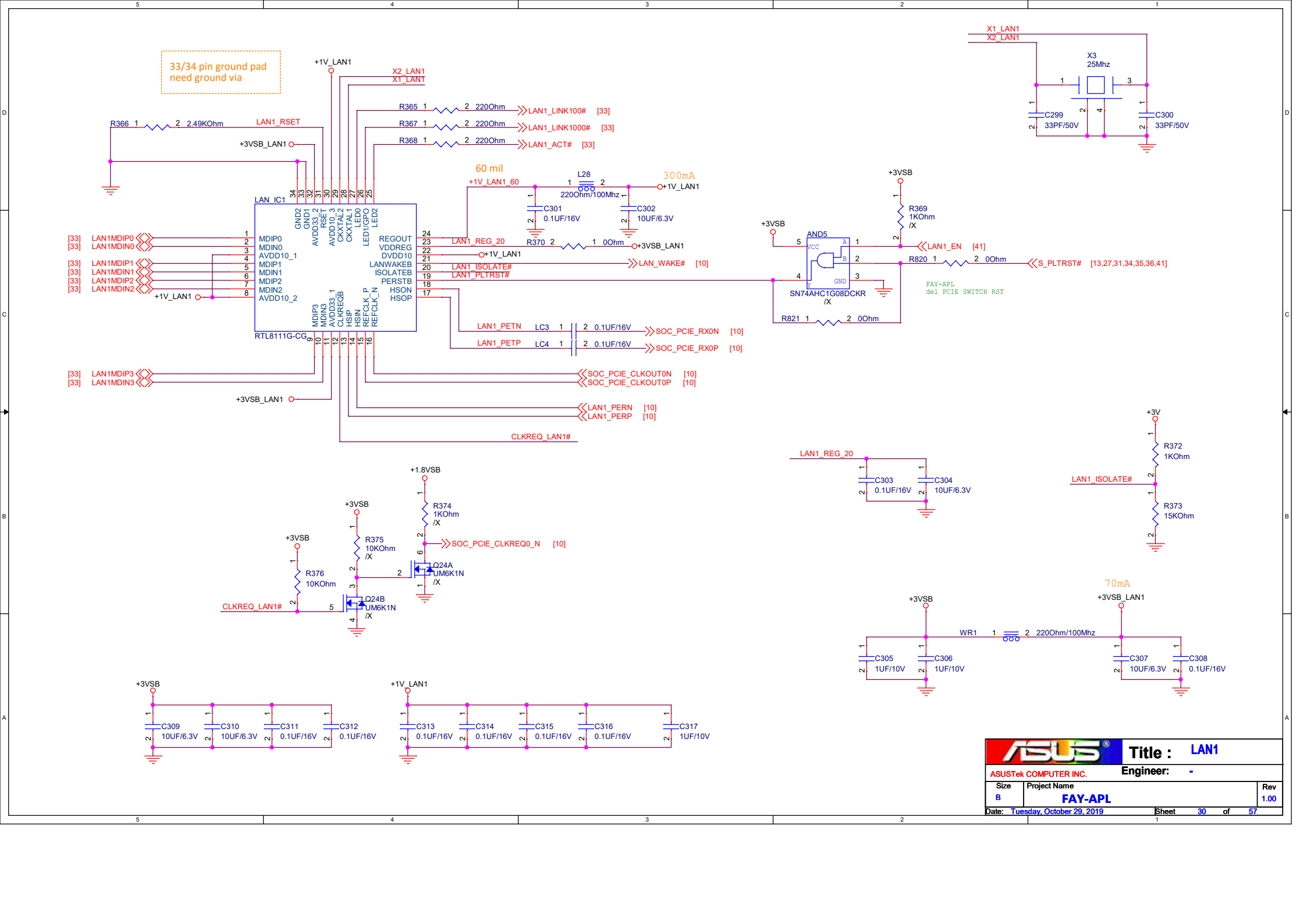
FAY-APL
change USB3 CONN

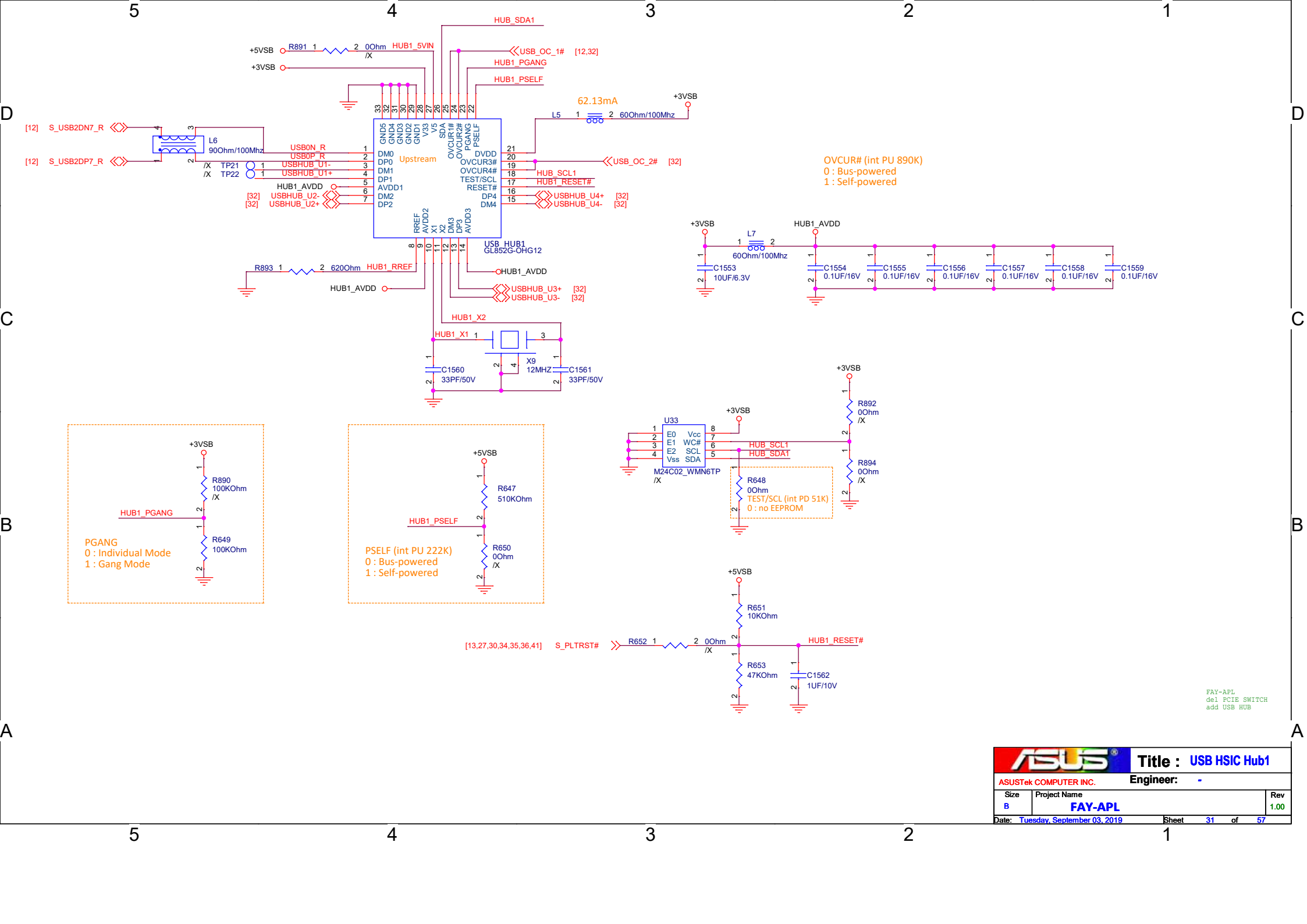


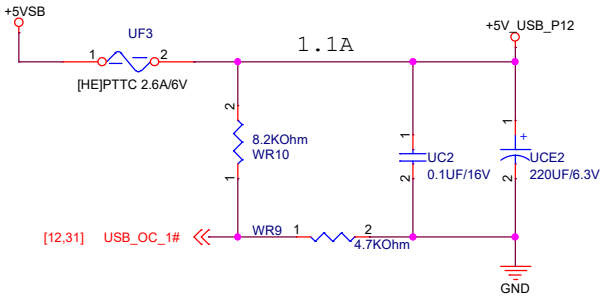


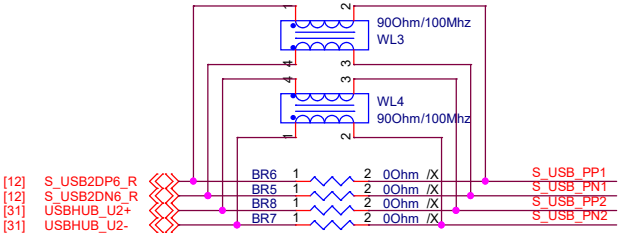
FAY-APL
del USB2 CONN

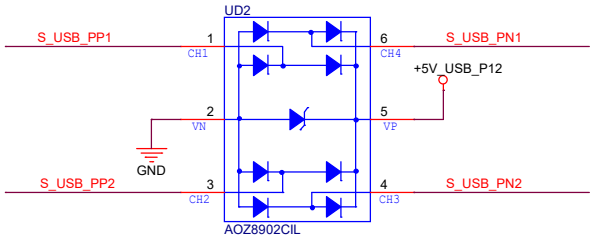
ASUSTek COMPUTER INC.	Title : USB3.0	
	Engineer: -	
Size: Custom	Project Name: FAY-APL	Rev: 1.00
Date: Tuesday, September 10, 2019	Sheet 29 of 57	

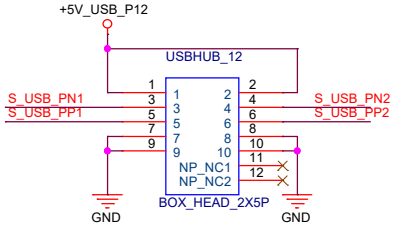

33/34 pin ground pad need ground via
LAN_IC1
RTL8111G-CG
MDIP0
MDIN0
AVDD10_1
MDIP1
MDIN1
MDIP2
MDIN2
AVDD10_2
MDIP3
MDIN3
AVDD33_1
CLKREQB
HSIP
HSIN
REFCLK_P
REFCLK_N
HSON
HSOP
PERSTB
LANWAKEB
ISOLATEB
DVDD10
VDDREG
REGOUT
GND2
GND1
AVDD33_2
RSET
AVDD10_3
CKXTAL2
CKXTAL1
LED0
LED1/GPO
LED2
+1V_LAN1
+3VSB_LAN1
+3VSB
+1.8VSB
X1_LAN1
X2_LAN1
X3
25Mhz
C299
33PF/50V
C300
33PF/50V
R366 2.49KOhm
LAN1_RSET
R365 220Ohm
R367 220Ohm
R368 220Ohm
LAN1_LINK100# [33]
LAN1_LINK1000# [33]
LAN1_ACT# [33]
60 mil
300mA
L28
220Ohm/100Mhz
C301
0.1UF/16V
C302
10UF/6.3V
R370 0Ohm
LAN1_REG_20
LAN_WAKE# [10]
LAN1_ISOLATE#
LAN1_PLTRST#
LAN1_PETN
LAN1_PETP
LC3 0.1UF/16V
LC4 0.1UF/16V
SOC_PCIE_RX0N [10]
SOC_PCIE_RX0P [10]
SOC_PCIE_CLKOUT0N [10]
SOC_PCIE_CLKOUT0P [10]
LAN1_PERN [10]
LAN1_PERP [10]
CLKREQ_LAN1#
[33] LAN1MDIP0
[33] LAN1MDIN0
[33] LAN1MDIP1
[33] LAN1MDIN1
[33] LAN1MDIP2
[33] LAN1MDIN2
[33] LAN1MDIP3
[33] LAN1MDIN3
AND5
SN74AHC1G08DCKR
/X
R369 1KOhm
/X
LAN1_EN [41]
R820 0Ohm
S_PLTRST# [13,27,31,34,35,36,41]
R821 0Ohm
FAY-APL
del PCIE SWITCH RST
R374 1KOhm
/X
R375 10KOhm
/X
R376 10KOhm
Q24A UM6K1N
/X
Q24B UM6K1N
/X
SOC_PCIE_CLKREQ0_N [10]
LAN1_REG_20
C303 0.1UF/16V
C304 10UF/6.3V
+3V
R372 1KOhm
R373 15KOhm
LAN1_ISOLATE#
70mA
WR1 220Ohm/100Mhz
C305 1UF/10V
C306 1UF/10V
C307 10UF/6.3V
C308 0.1UF/16V
C309 10UF/6.3V
C310 10UF/6.3V
C311 0.1UF/16V
C312 0.1UF/16V
C313 0.1UF/16V
C314 0.1UF/16V
C315 0.1UF/16V
C316 0.1UF/16V
C317 1UF/10V
Title : LAN1
ASUSTek COMPUTER INC.
Engineer: -
Size B
Project Name FAY-APL
Rev 1.00
Date: Tuesday, October 29, 2019
Sheet 30 of 57

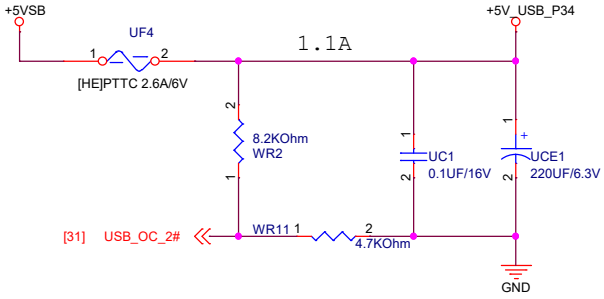

HUB_SDA1
+5VSB
R891 1 2 0Ohm HUB1_5VIN
/X
+3VSB
USB_OC_1# [12,32]
HUB1_PGANG
HUB1_PSELF
62.13mA
+3VSB
L5 1 2 60Ohm/100Mhz
[12] S_USB2DN7_R
[12] S_USB2DP7_R
L6
90Ohm/100Mhz
USB0N_R
USB0P_R
/X TP21
/X TP22
USBHUB_U1-
USBHUB_U1+
HUB1_AVDD
[32] USBHUB_U2-
[32] USBHUB_U2+
Upstream
USB_OC_2# [32]
HUB_SCL1
HUB1_RESET#
USBHUB_U4+ [32]
USBHUB_U4- [32]
USB_HUB1
GL852G-OHG12
R893 1 2 620Ohm HUB1_RREF
HUB1_AVDD
HUB1_AVDD
USBHUB_U3+ [32]
USBHUB_U3- [32]
HUB1_X2
HUB1_X1
X9
12MHZ
C1560
33PF/50V
C1561
33PF/50V
OVCUR# (int PU 890K)
0 : Bus-powered
1 : Self-powered
+3VSB
L7
60Ohm/100Mhz
HUB1_AVDD
C1553
10UF/6.3V
C1554
0.1UF/16V
C1555
0.1UF/16V
C1556
0.1UF/16V
C1557
0.1UF/16V
C1558
0.1UF/16V
C1559
0.1UF/16V
+3VSB
R890
100KOhm
/X
HUB1_PGANG
R649
100KOhm
PGANG
0 : Individual Mode
1 : Gang Mode
+5VSB
R647
510KOhm
HUB1_PSELF
R650
0Ohm
/X
PSELF (int PU 222K)
0 : Bus-powered
1 : Self-powered
U33
E0 Vcc
E1 WC#
E2 SCL
Vss SDA
M24C02_WMN6TP
/X
+3VSB
HUB_SCL1
HUB_SDA1
R648
0Ohm
TEST/SCL (int PD 51K)
0 : no EEPROM
+3VSB
R892
0Ohm
/X
R894
0Ohm
/X
+5VSB
R651
10KOhm
[13,27,30,34,35,36,41] S_PLTRST#
R652 1 2 0Ohm
/X
HUB1_RESET#
R653
47KOhm
C1562
1UF/10V
FAY-APL
del PCIE SWITCH
add USB HUB
Title : USB HSIC Hub1
ASUSTek COMPUTER INC.
Engineer: -
Size B
Project Name FAY-APL
Rev 1.00
Date: Tuesday, September 03, 2019
Sheet 31 of 57

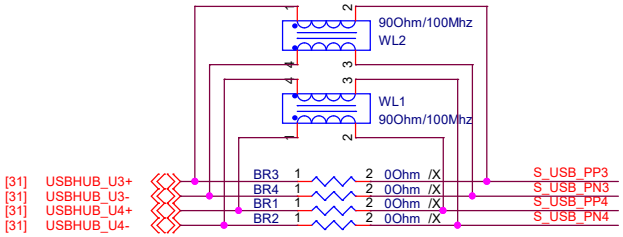


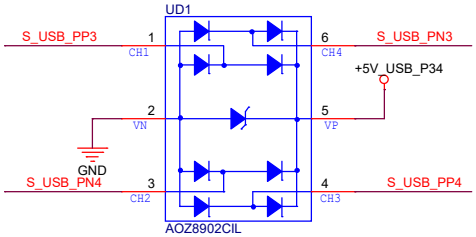


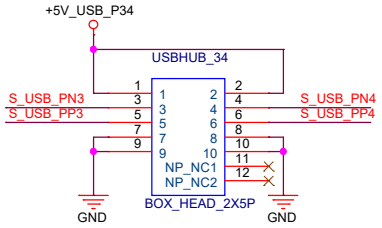






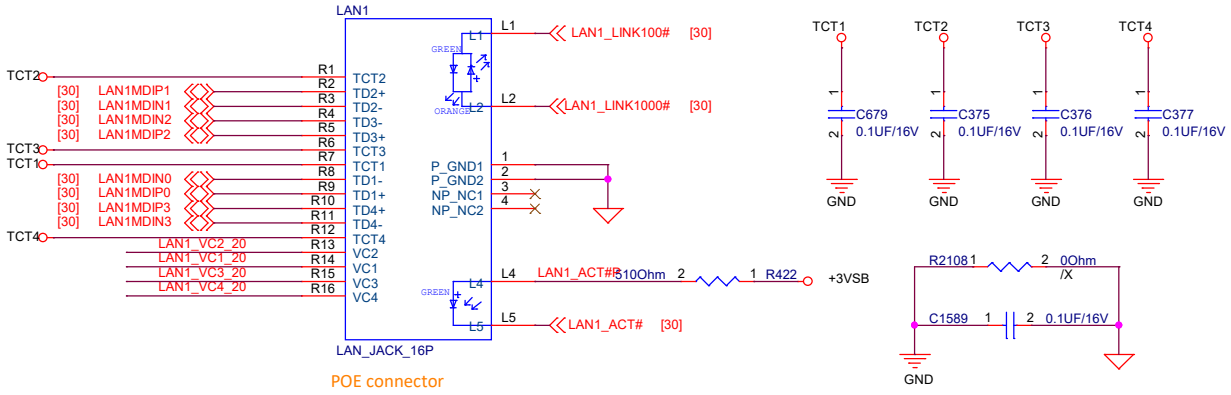


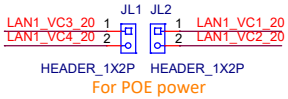




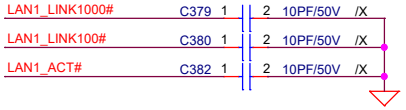
FAY-APL
del LAN2
add USB2 CONN

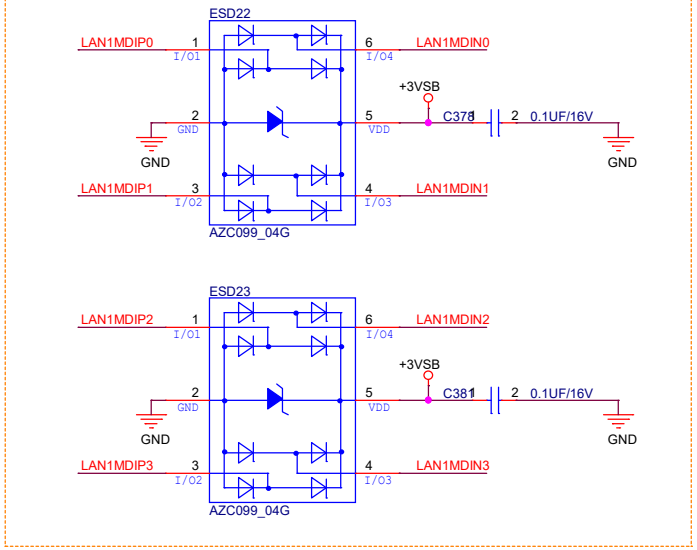
ASUSTek COMPUTER INC.	Title : USB2.0	
	Engineer: -	
Size: B	Project Name: FAY-APL	Rev: 1.00
Date: Monday, September 02, 2019	Sheet 32 of 57	





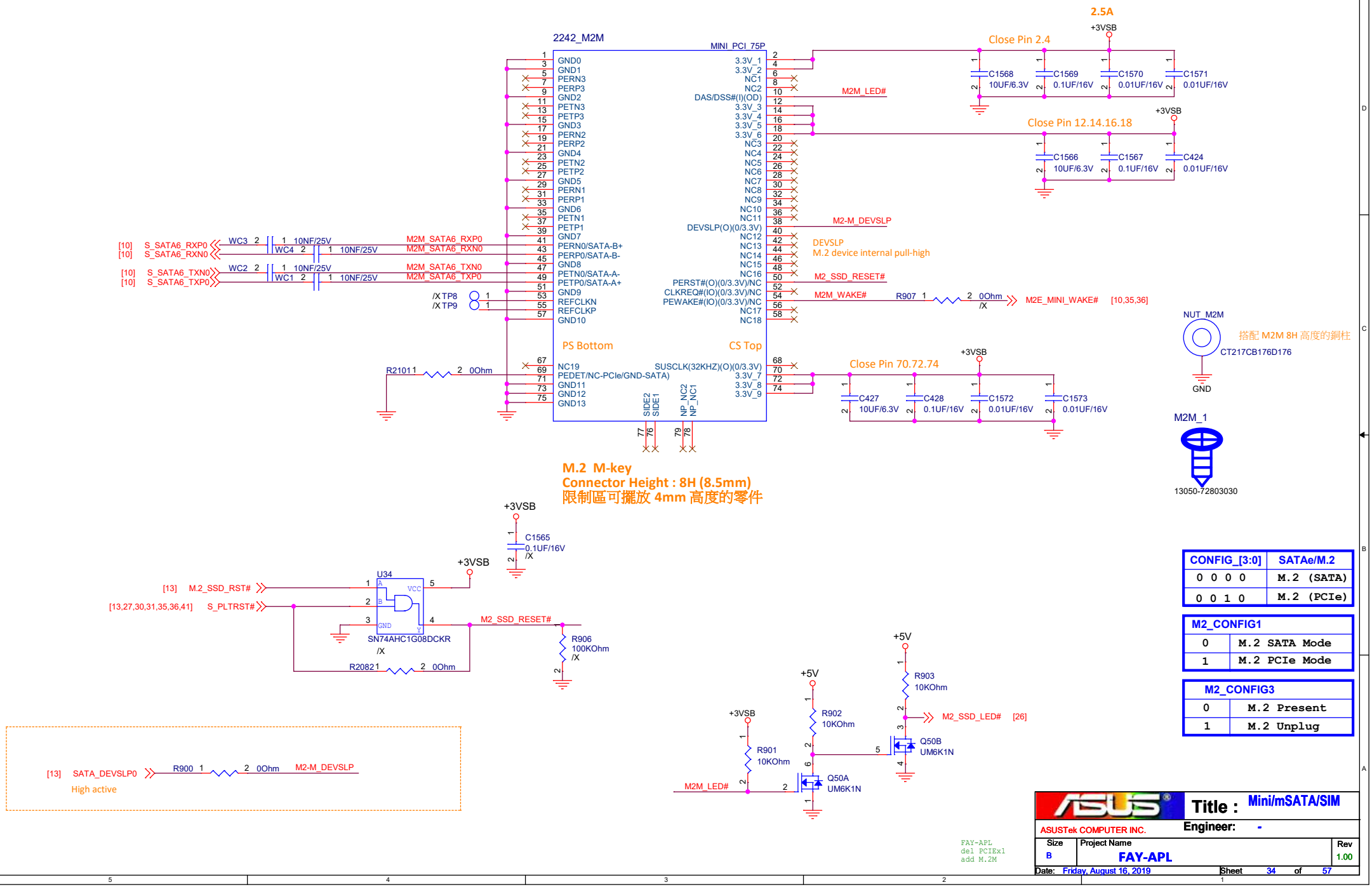
For POE power

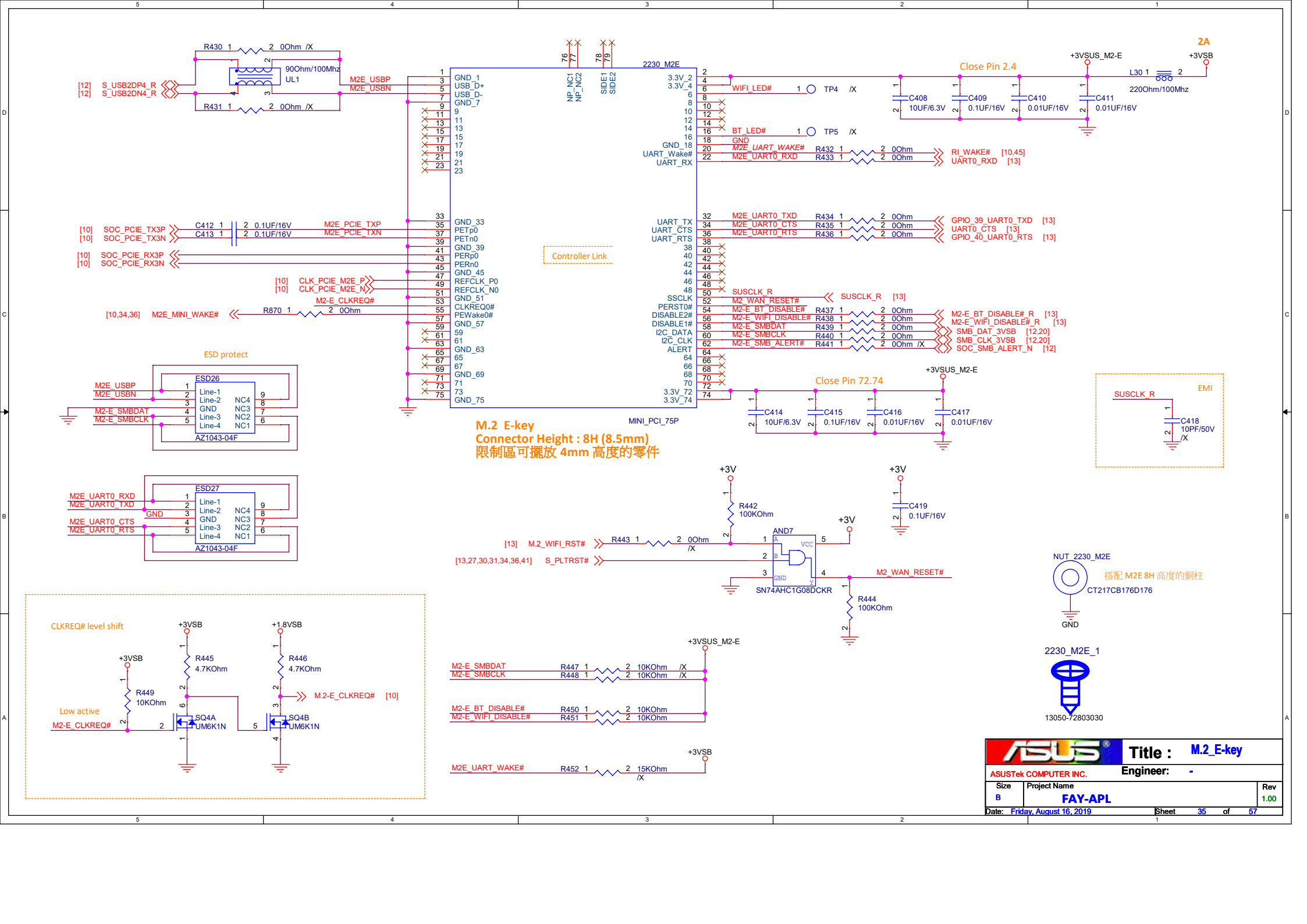




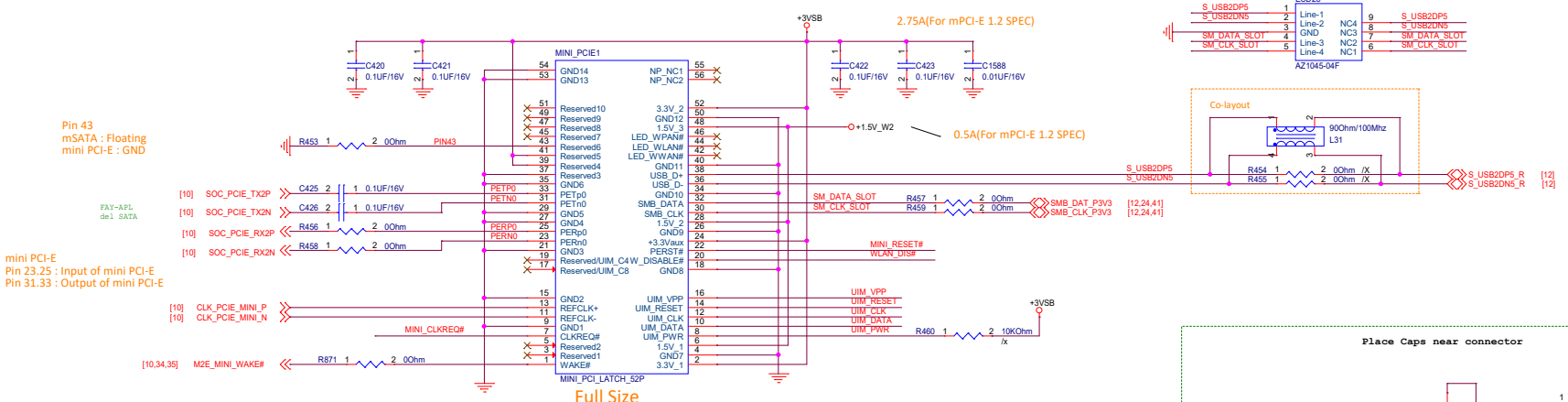
FAY-APL
del LAN2

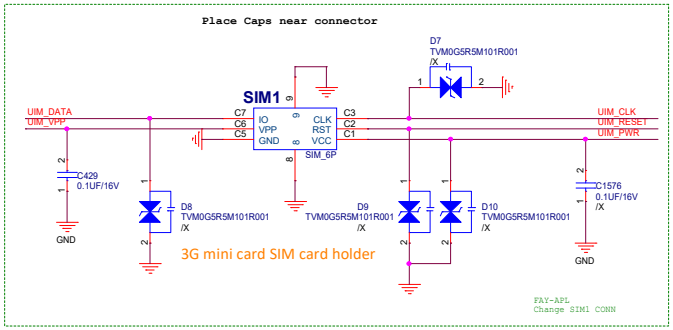
ASUSTek COMPUTER INC.	Title : LAN connector		
	Engineer: -		
Size: B	Project Name: FAY-APL		Rev: 1.00
Date: Monday, September 09, 2019	Sheet 33 of 57		

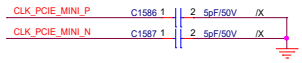

2.5A
2242_M2M
MINI_PCI_75P
GND0
GND1
PERN3
PERP3
GND2
PETN3
PETP3
GND3
PERN2
PERP2
GND4
PETN2
PETP2
GND5
PERN1
PERP1
GND6
PETN1
PETP1
GND7
PERN0/SATA-B+
PERP0/SATA-B-
GND8
PETN0/SATA-A-
PETP0/SATA-A+
GND9
REFCLKN
REFCLKP
GND10
NC19
PEDET/NC-PCIe/GND-SATA)
GND11
GND12
GND13
3.3V_1
3.3V_2
NC1
NC2
DAS/DSS#(I)(OD)
3.3V_3
3.3V_4
3.3V_5
3.3V_6
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
DEVSLP(O)(0/3.3V)
NC12
NC13
NC14
NC15
NC16
PERST#(O)(0/3.3V)/NC
CLKREQ#(IO)(0/3.3V)/NC
PEWAKE#(IO)(0/3.3V)/NC
NC17
NC18
SUSCLK(32KHZ)(O)(0/3.3V)
3.3V_7
3.3V_8
3.3V_9
SIDE2
SIDE1
NP_NC2
NP_NC1
PS Bottom
CS Top
M2M_LED#
M2-M_DEVSLP
DEVSLP
M.2 device internal pull-high
M2_SSD_RESET#
M2M_WAKE#
R907 1 2 0Ohm /X
M2E_MINI_WAKE# [10,35,36]
Close Pin 2.4
+3VSB
C1568 10UF/6.3V
C1569 0.1UF/16V
C1570 0.01UF/16V
C1571 0.01UF/16V
Close Pin 12.14.16.18
C1566 10UF/6.3V
C1567 0.1UF/16V
C424 0.01UF/16V
Close Pin 70.72.74
C427 10UF/6.3V
C428 0.1UF/16V
C1572 0.01UF/16V
C1573 0.01UF/16V
NUT_M2M
CT217CB176D176
GND
搭配 M2M 8H 高度的銅柱
M2M_1
13050-72803030
[10] S_SATA6_RXP0
[10] S_SATA6_RXN0
WC3 2 1 10NF/25V
WC4 2 1 10NF/25V
M2M_SATA6_RXP0
M2M_SATA6_RXN0
[10] S_SATA6_TXN0
[10] S_SATA6_TXP0
WC2 2 1 10NF/25V
WC1 2 1 10NF/25V
M2M_SATA6_TXN0
M2M_SATA6_TXP0
/X TP8
/X TP9
R21011 2 0Ohm
M.2 M-key
Connector Height : 8H (8.5mm)
限制區可擺放 4mm 高度的零件
+3VSB
C1565 0.1UF/16V /X
U34
SN74AHC1G08DCKR
/X
[13] M.2_SSD_RST#
[13,27,30,31,35,36,41] S_PLTRST#
M2_SSD_RESET#
R906 100KOhm /X
R20821 2 0Ohm
+5V
R903 10KOhm
R902 10KOhm
R901 10KOhm
M2_SSD_LED# [26]
Q50B UM6K1N
Q50A UM6K1N
M2M_LED#
[13] SATA_DEVSLP0
R900 1 2 0Ohm M2-M_DEVSLP
High active
CONFIG_[3:0] SATAe/M.2
0 0 0 0 M.2 (SATA)
0 0 1 0 M.2 (PCIe)
M2_CONFIG1
0 M.2 SATA Mode
1 M.2 PCIe Mode
M2_CONFIG3
0 M.2 Present
1 M.2 Unplug
FAY-APL
del PCIEx1
add M.2M
Title : Mini/mSATA/SIM
ASUSTek COMPUTER INC.
Engineer: -
Size B
Project Name FAY-APL
Rev 1.00
Date: Friday, August 16, 2019
Sheet 34 of 57

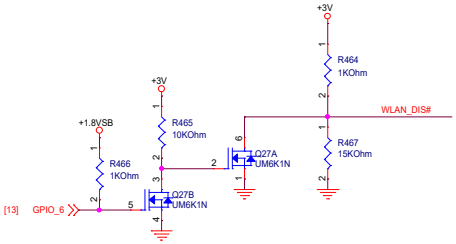

2A
R430 1 2 0Ohm /X
90Ohm/100Mhz
UL1
R431 1 2 0Ohm /X
[12] S_USB2DP4_R
[12] S_USB2DN4_R
M2E_USBP
M2E_USBN
2230_M2E
GND_1
USB_D+
USB_D-
GND_7
NP_NC1
NP_NC2
SIDE1
SIDE2
3.3V_2
3.3V_4
WIFI_LED#
BT_LED#
GND_18
M2E_UART_WAKE#
UART_Wake#
UART_RX
Close Pin 2.4
+3VSUS_M2E
+3VSB
L30 1 2
220Ohm/100Mhz
C408 10UF/6.3V
C409 0.1UF/16V
C410 0.01UF/16V
C411 0.01UF/16V
TP4 /X
TP5 /X
GND
R432 1 2 0Ohm
R433 1 2 0Ohm
RI_WAKE# [10,45]
UART0_RXD [13]
[10] SOC_PCIE_TX3P
[10] SOC_PCIE_TX3N
C412 1 2 0.1UF/16V
C413 1 2 0.1UF/16V
M2E_PCIE_TXP
M2E_PCIE_TXN
[10] SOC_PCIE_RX3P
[10] SOC_PCIE_RX3N
GND_33
PETp0
PETn0
GND_39
PERp0
PERn0
GND_45
REFCLK_P0
REFCLK_N0
GND_51
CLKREQ0#
PEWake0#
GND_57
GND_63
GND_69
GND_75
[10] CLK_PCIE_M2E_P
[10] CLK_PCIE_M2E_N
M2-E_CLKREQ#
[10,34,36] M2E_MINI_WAKE#
R870 1 2 0Ohm
Controller Link
UART_TX
UART_CTS
UART_RTS
SSCLK
PERST0#
DISABLE2#
DISABLE1#
I2C_DATA
I2C_CLK
ALERT
3.3V_72
3.3V_74
M2E_UART0_TXD
M2E_UART0_CTS
M2E_UART0_RTS
R434 1 2 0Ohm
R435 1 2 0Ohm
R436 1 2 0Ohm
GPIO_39_UART0_TXD [13]
UART0_CTS [13]
GPIO_40_UART0_RTS [13]
SUSCLK_R
M2_WAN_RESET#
M2-E_BT_DISABLE#
M2-E_WIFI_DISABLE#
M2-E_SMBDAT
M2-E_SMBCLK
M2-E_SMB_ALERT#
R437 1 2 0Ohm
R438 1 2 0Ohm
R439 1 2 0Ohm
R440 1 2 0Ohm
R441 1 2 0Ohm /X
SUSCLK_R [13]
M2-E_BT_DISABLE#_R [13]
M2-E_WIFI_DISABLE#_R [13]
SMB_DAT_3VSB [12,20]
SMB_CLK_3VSB [12,20]
SOC_SMB_ALERT_N [12]
Close Pin 72.74
C414 10UF/6.3V
C415 0.1UF/16V
C416 0.01UF/16V
C417 0.01UF/16V
MINI_PCI_75P
M.2 E-key
Connector Height : 8H (8.5mm)
限制區可擺放 4mm 高度的零件
EMI
SUSCLK_R
C418 10PF/50V /X
ESD protect
ESD26
M2E_USBP
M2E_USBN
M2-E_SMBDAT
M2-E_SMBCLK
Line-1
Line-2
Line-3
Line-4
GND
NC1
NC2
NC3
NC4
AZ1043-04F
ESD27
M2E_UART0_RXD
M2E_UART0_TXD
M2E_UART0_CTS
M2E_UART0_RTS
GND
AZ1043-04F
+3V
R442 100KOhm
C419 0.1UF/16V
[13] M.2_WIFI_RST#
R443 1 2 0Ohm /X
[13,27,30,31,34,36,41] S_PLTRST#
AND7
SN74AHC1G08DCKR
M2_WAN_RESET#
R444 100KOhm
NUT_2230_M2E
搭配 M2E 8H 高度的銅柱
CT217CB176D176
GND
2230_M2E_1
13050-72803030
CLKREQ# level shift
+3VSB
+1.8VSB
R445 4.7KOhm
R446 4.7KOhm
R449 10KOhm
Low active
M2E-CLKREQ#
SQ4A UM6K1N
SQ4B UM6K1N
M.2-E_CLKREQ# [10]
+3VSUS_M2-E
M2-E_SMBDAT
M2-E_SMBCLK
R447 1 2 10KOhm /X
R448 1 2 10KOhm /X
M2-E_BT_DISABLE#
M2-E_WIFI_DISABLE#
R450 1 2 10KOhm
R451 1 2 10KOhm
M2E_UART_WAKE#
R452 1 2 15KOhm /X
Title : M.2_E-key
ASUSTek COMPUTER INC.
Engineer: -
Size B
Project Name FAY-APL
Rev 1.00
Date: Friday, August 16, 2019
Sheet 35 of 57

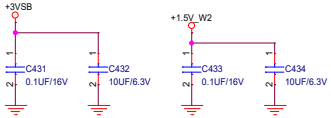
MINI Card (PCIE only)

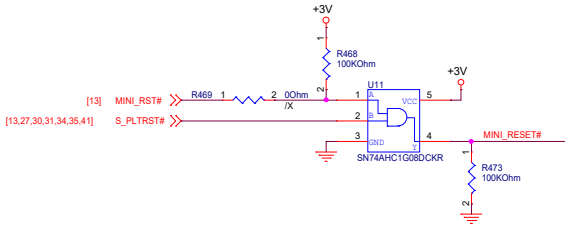


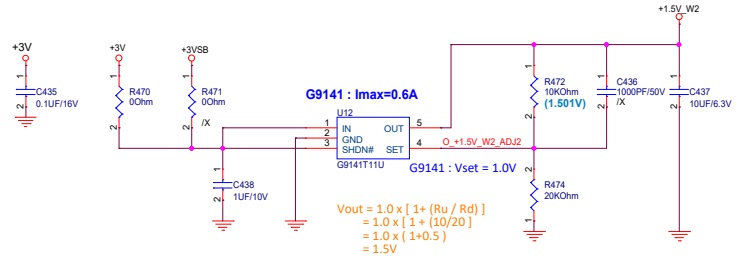


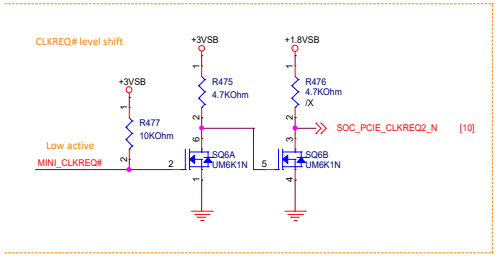


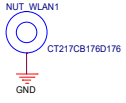












ASUSTek COMPUTER INC.	Title : PCI-E x1 slot		
	Engineer: -		
Size: C	Project Name: FAY-APL		Rev: 1.00
Date: Friday, August 16, 2019	Sheet 36 of 57		

Analog GND form Pin 13 to 33 and Pin 38~40

AU1

GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
SDATA-IN
SDATA-OUT
SYNC
RESETB
BCLK
PCBEEP
SPDIF-OUT/GPIO2
DVDD
DVDD-IO
AVDD1
AVDD2
PVDD1
PVDD2
VREF
LDO1-CAP
LDO2-CAP
MIC-CAP
LDO3-CAP
JDREF
Sense_A
Sense_B
GND1
GND_VIA1
GND_VIA2
GND_VIA3
GND_VIA4
GND_VIA5
GND_VIA6
GND_VIA7
GND_VIA8
AVSS1
AVSS2
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
LINE1-VREFO-L
LINE1-VREFO-R
HPOUT-L(PORT-I-L)
HPOUT-R(PORT-I-R)
MIC2-L(PORT-F-L)/RING2
MIC2-R(PORT-F-R)/SLEEVE
MIC2-VREFO
SPK-OUT-L-
SPK-OUT-L+
SPK-OUT-R-
SPK-OUT-R+
CPVDD
CPVEE
CBN
CBP
PDB
LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
MONO-OUT
NC

ALC3236-VB2-CG

[13] HDA_SDIN — R543 33Ohm — HDA_SDIN_R
[13] HDA_SDOUT — R544 33Ohm — HDA_SDOUT_R
[13] HDA_SYNC — R546 33Ohm — HDA_SYNC_R
[11] HDA_RST_N — R538 33Ohm — HDA_RST_N_R
[13] HDA_BITCLK — R547 33Ohm — HDA_BITCLK_R
C478 15PF/50V /X

[13] SOC_SPKR — R540 1KOhm — PCBEEP_R — C485 0.1UF/16V — PCBEEP
[41] SIO_SPKR — R549 1KOhm /X
R541 2.61KOHM /X
C486 100PF/50V /X
SPDIF_OUT

+3V
+3.3V_AUDIO
L36 120Ohm/100Mhz Irat=600mA
C488 10UF/16V
C489 10UF/16V
C490 0.1UF/16V

DVDD-IO : AUDIO codec interface voltage
DVDD-IO_AUDIO
1.8V for Apollo Lake
+1.8V_AUDIO
set HD interface voltage
L37 120Ohm/100Mhz Irat=600mA
C491 0.1UF/16V

+5VSB
L39 120Ohm/100Mhz Irat=600mA
+AVDD1_AUDIO
C493 10UF/16V
C494 0.1UF/16V

+AVDD2_AUDIO
+1.5V_AUDIO
L41 120Ohm/100Mhz Irat=600mA
C500 10UF/16V
C501 0.1UF/16V

+5VSB
L43 120Ohm
PVDD_AUDIO
C504 10UF/16V
C505 0.1UF/16V
C506 10UF/16V
C507 0.1UF/16V

C509 2.2UF/16V
C510 10UF/16V
R557 100KOhm
C511 10UF/16V
C512 10UF/16V
R560 20KOhm /X

for ALC3236-VB2
+3V
R561 100KOhm SENSE-A
LINEOUT-JD R755 200KOhm
MIC1-JD R756 100KOhm

DC_DET
R759 10KOhm
R760 0Ohm /X
+3.3V_AUDIO

LINE1-L_CR — L34 120Ohm/100Mhz — A_LOUT_L
LINE1-R_CR — L35 120Ohm/100Mhz — A_LOUT_R
C479 100PF/50V
C480 100PF/50V

MIC1-L — C481 4.7UF/16V — MIC1-L_C — R542 1KOhm — MIC1-L_CR — L32 120Ohm/100Mhz — A_MIC1_L
MIC1-R — C482 4.7UF/16V — MIC1-R_C — R536 1KOhm — MIC1-R_CR — L33 120Ohm/100Mhz — A_MIC1_R
MIC1-VREFO-L — R537 4.7KOhm
MIC1-VREFO-R — R545 4.7KOhm
C483 100PF/50V
C484 100PF/50V

AAFP
A_MIC1_L
A_MIC1_R
A_LOUT_R
A_LOUT_L
R757 0Ohm
MIC1-JD — R550 0Ohm /X
LINEOUT-JD — R552 0Ohm /X
NP_NC1
NP_NC2
BOX_HEAD_2X5P

SPK-OUT-L- — INT-SPK-L-_40
SPK-OUT-L+ — INT-SPK-L+_40
SPK-OUT-R- — INT-SPK-R-_40
SPK-OUT-R+ — INT-SPK-R+_40

+3.3V_AUDIO
C496 0.1UF/16V
C497 10UF/16V
C499 2.2UF/16V
CBN — C498 2.2UF/16V
CBP
PDB_AUDIO

[37] A_LOUT_PL_30
[37] A_LOUT_NL_30
[37] A_LOUT_NR_30
[37] A_LOUT_PR_30
SPDIF_AMP
R559 10Ohm
R558 0Ohm — SPDIF_OUT
Option to 470PF
C514 100PF/50V /X
+5V
C513 0.1UF/16V
FAY-APL
add audio AMP
modify pinout for LAYOUT

LINE2-L_10 — C1585 0.22UF/6.3V — AMP_IN_L [37]
LINE2-N_10 — C1584 0.22UF/6.3V — AMP_IN_R [37]
10 mil
add Audio Amplifier
FAY-APL
add audio AMP
R555 0Ohm — +3VSB
for ALC3236-VB2

+3.3V_AUDIO
R753 10KOhm
Q51 2N7002-L
DC_DET
R754 0Ohm /X
Q53 BSS138
HDA_RST_N_R
R554 10KOhm
Q52 2N7002-L
PDB_AUDIO
R556 10KOhm /X
C508 1UF/10V /X

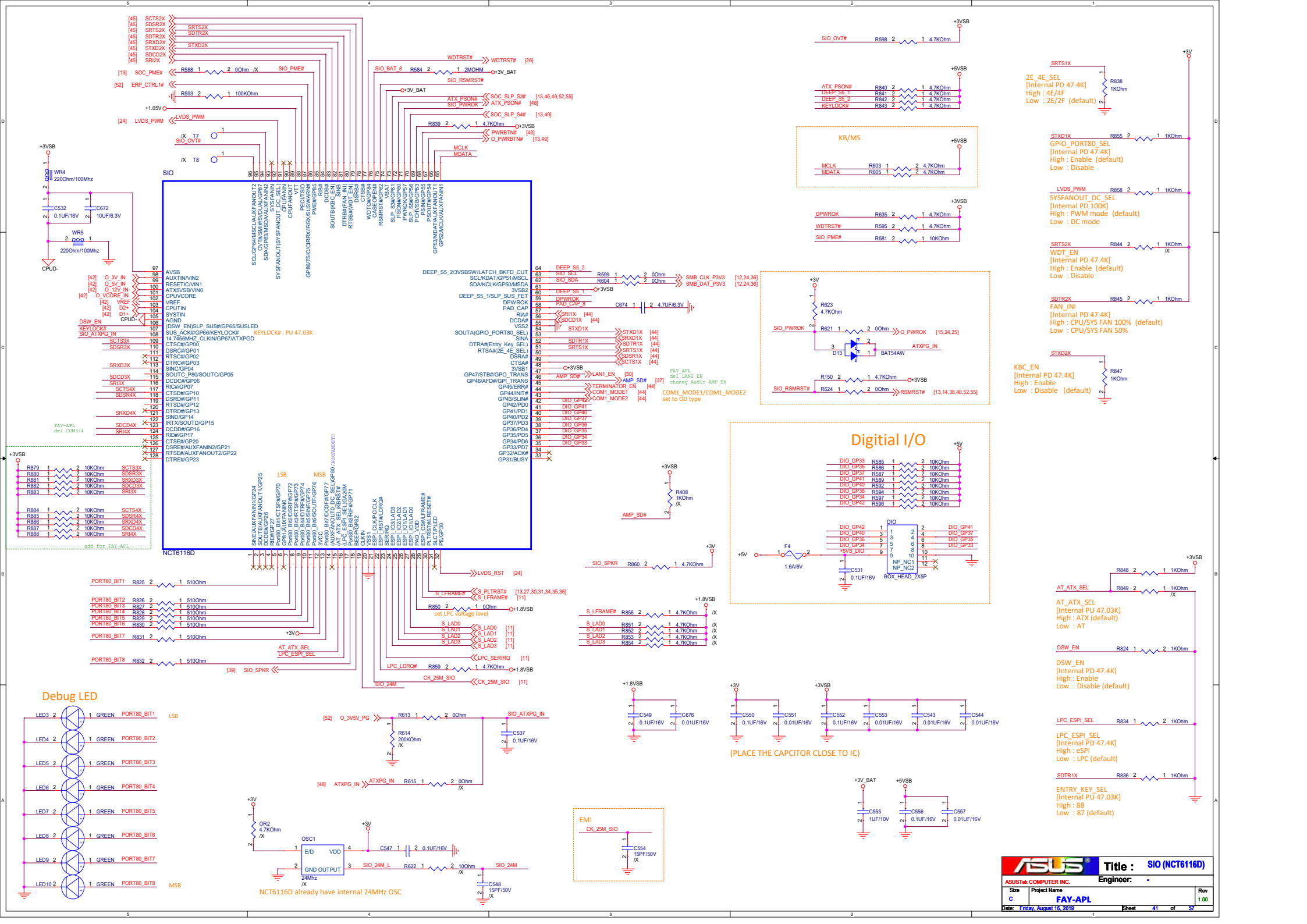
INT-SPK-L+_40 — L38 30Ohm/100Mhz — C492 1000PF/50V — C495 1000PF/50V — LOUTP_40 LOUTN_40 — SPEAK_L HEADER_1X2P /X
INT-SPK-L-_40 — L40 30Ohm/100Mhz
INT-SPK-R-_40 — L42 30Ohm/100Mhz — C502 1000PF/50V — C503 1000PF/50V — ROUTP_40 ROUTN_40 — SPEAK_R HEADER_1X2P /X
INT-SPK-R+_40 — L44 30Ohm/100Mhz
Speaker 4 ohm : 40 mil
Speaker 8 ohm : 20 mil

M3 /X — SHORT_GND1 — Short_GND1
M4 /X — SHORT_GND2 — Short_GND2
R562 0Ohm
R563 0Ohm
R564 0Ohm
R565 0Ohm
AGND

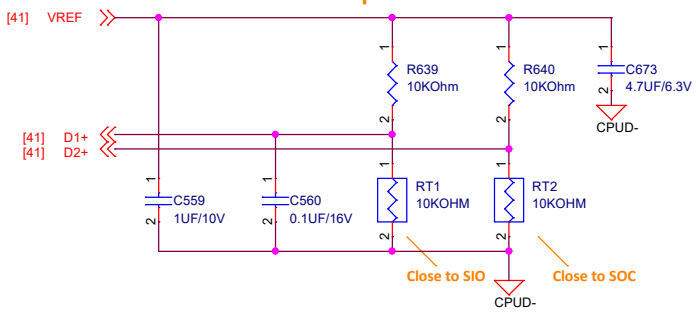
+3V
G9141 : Imax=0.6A
U16 G9141T11U
IN GND SHDN# OUT SET
C519 1UF/10V
G9141 : Vset = 1.0V
Vout = 1.0 x [1+ (Ru / Rd)]
= 1.0 x [1 + (10/20]
= 1.0 x (1+0.5)
= 1.5V
R566 10KOhm
C515 1000PF/50V /X
C516 10UF/6.3V
R568 20KOhm
+1.5V_AUDIO

+3V
G9141 : Imax=0.6A
U17 G9141T11U
IN GND SHDN# OUT SET
C520 1UF/10V
G9141 : Vset = 1.0V
Vout = 1.0 x [1+ (Ru / Rd)]
= 1.0 x (1+0.8)
= 1.8V
R567 16KOhm
C517 1000PF/50V /X
C518 10UF/6.3V
R569 20KOhm
+1.8V_AUDIO

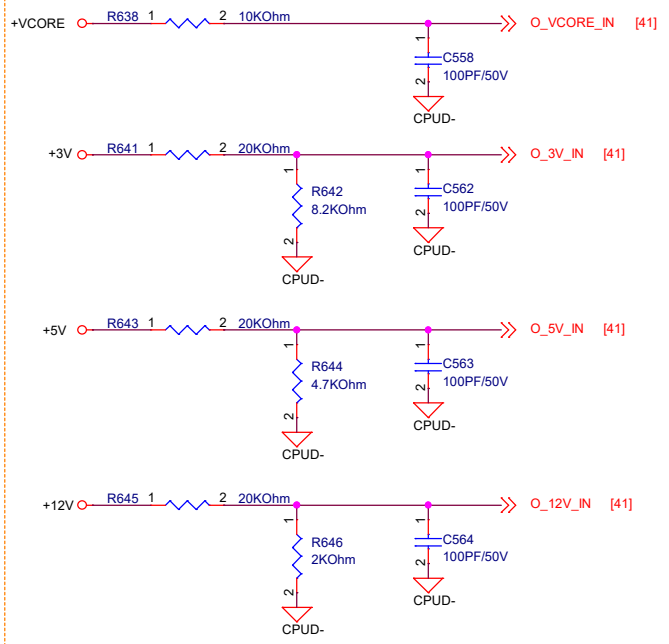
ASUSTek COMPUTER INC.
Title : AUDIO(ALC3236)
Engineer: -
Size: C
Project Name: FAY-APL
Rev: 1.00
Date: Thursday, September 12, 2019
Sheet 39 of 57


SIO
NCT6116D
Debug LED
KB/MS
Digitial I/O
EMI
(PLACE THE CAPCITOR CLOSE TO IC)
NCT6116D already have internal 24MHz OSC
KEYLOCK# : PU 47.03K
FAY_APL del COM3/4
FAY_APL del LAN2 EN chaneg Audio AMP EN
COM1_MODE1/COM1_MODE2 set to OD type
set LPC voltage level
2E_4E_SEL [Internal PD 47.4K] High : 4E/4F Low : 2E/2F (default)
GPIO_PORT80_SEL [Internal PD 47.4K] High : Enable (default) Low : Disable
SYSFANOUT_DC_SEL [Internal PD 100K] High : PWM mode (default) Low : DC mode
WDT_EN [Internal PD 47.4K] High : Enable (default) Low : Disable
FAN_INI [Internal PD 47.4K] High : CPU/SYS FAN 100% (default) Low : CPU/SYS FAN 50%
KBC_EN [Internal PD 47.4K] High : Enable Low : Disable (default)
AT_ATX_SEL [Internal PU 47.03K] High : ATX (default) Low : AT
DSW_EN [Internal PD 47.4K] High : Enable Low : Disable (default)
LPC_ESPI_SEL [Internal PD 47.4K] High : eSPI Low : LPC (default)
ENTRY_KEY_SEL [Internal PU 47.03K] High : 88 Low : 87 (default)
Title : SIO (NCT6116D)
ASUSTek COMPUTER INC.
Engineer: -
Size C
Project Name FAY-APL
Rev 1.00
Date: Friday, August 16, 2019
Sheet 41 of 57

Temp monitor



Voltage monitor



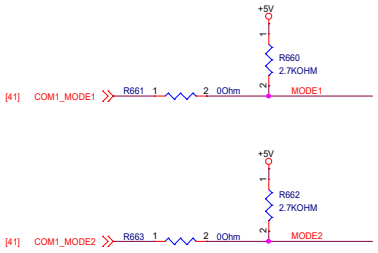
The voltage sense input range is 0 ~ 2.08V

ASUSTek COMPUTER INC.	Title : HW monitor	
	Engineer: -	
Size: B	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 42 of 57	

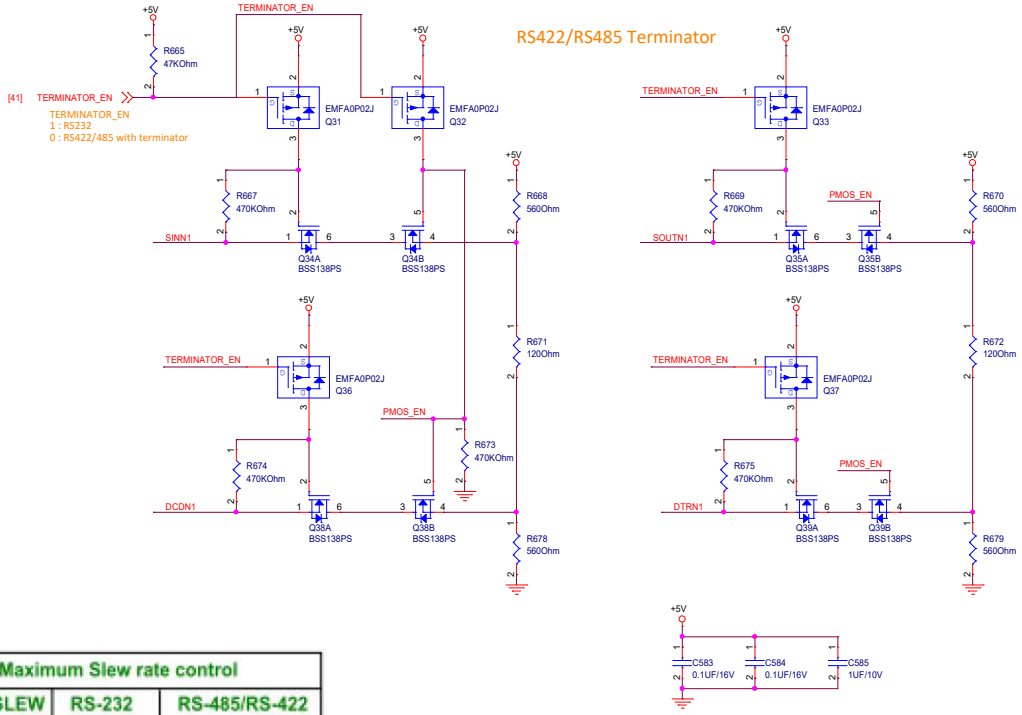
Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

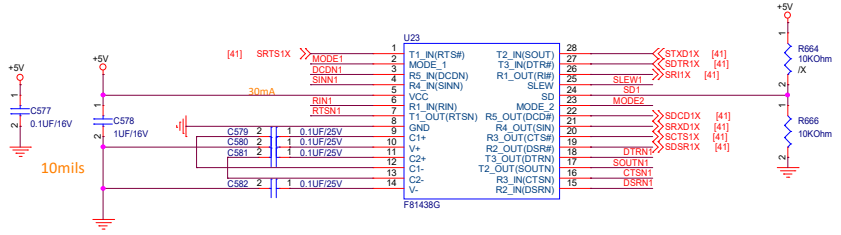
Note:

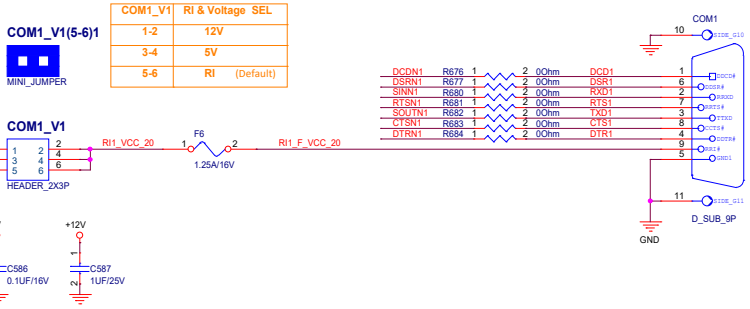
Mode_1 and Mode_2 pin. Internal pull high ≒ 625KΩ. As the current is very small (≒ 15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.



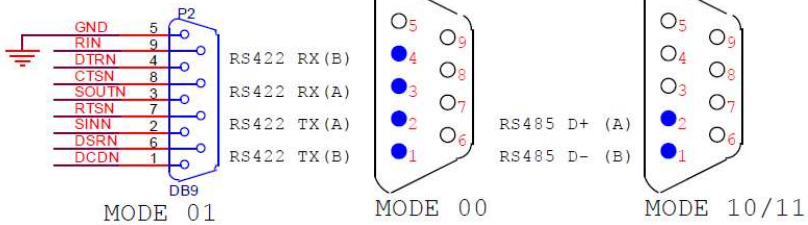
RS422/RS485 Terminator

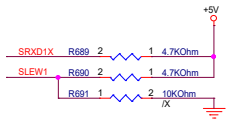


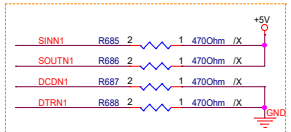


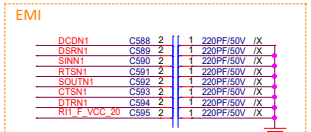


Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps









ASUSTek COMPUTER INC.

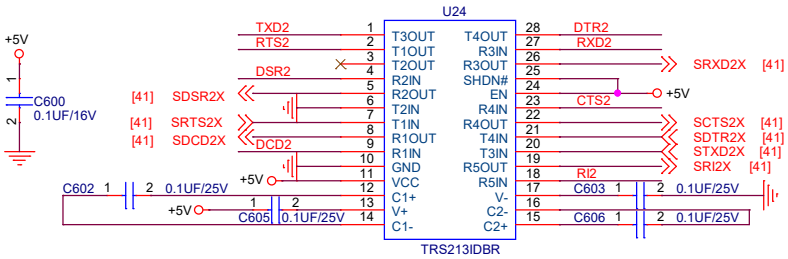
Title : COM1(RS232/422/485)

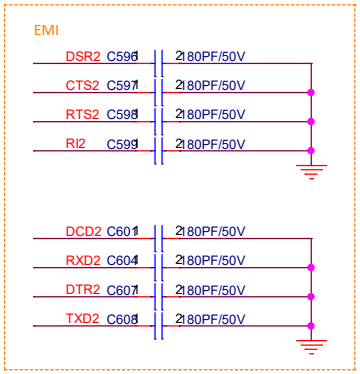
Engineer: -

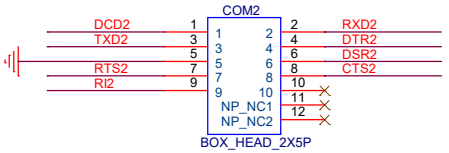
Size	Project Name	Rev
C	FAY-APL	1.00

Date: Friday, August 16, 2019 Sheet 44 of 57

COM2

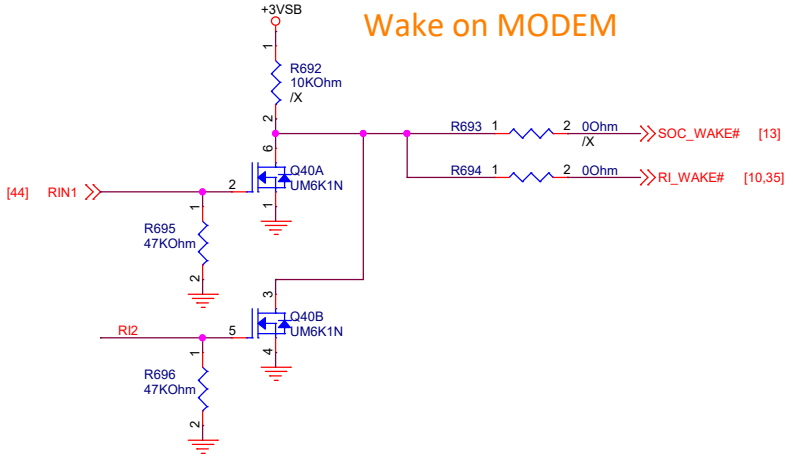






FAY-APL
del COM3/4

Wake on MODEM

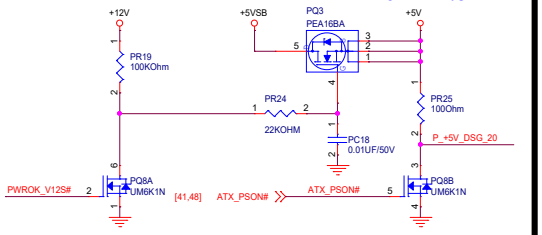


ASUSTek COMPUTER INC.	Title : COM2	
	Engineer: -	
Size: B	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 45 of 57	

FAY-APL
change +5VSUS/+3VSUS solution

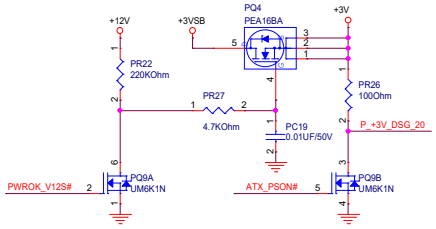
+5V SWITCH

Imax = 1.0A

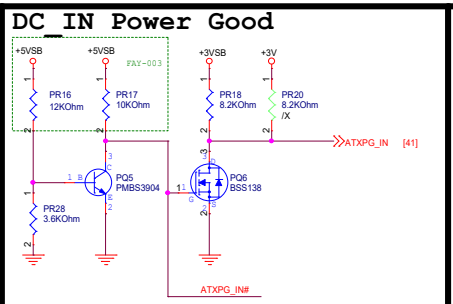


+3V SWITCH

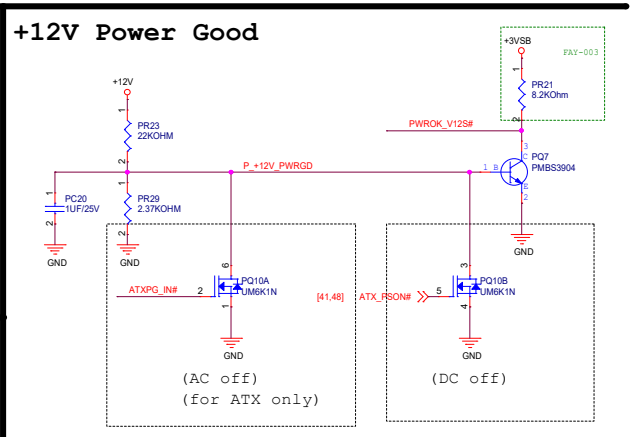
Imax = 0.5A



DC_IN Power Good

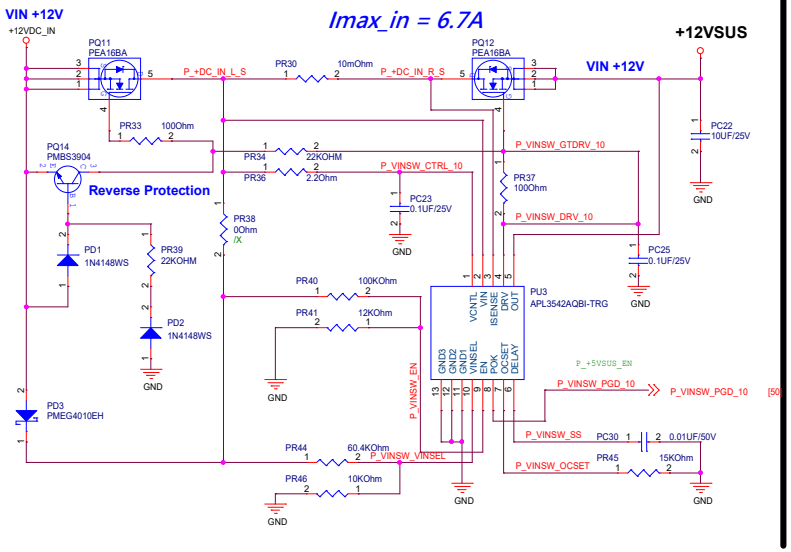


+12V Power Good



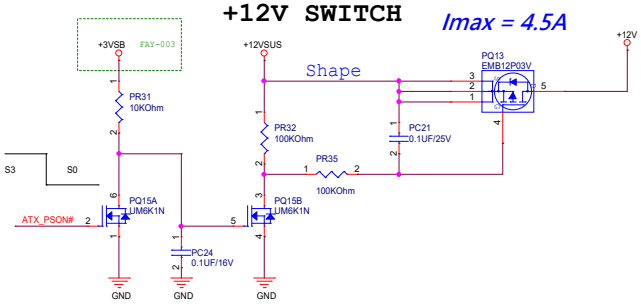
VIN +12V

Imax_in = 6.7A

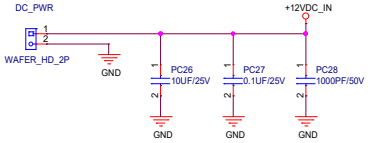


+12V SWITCH

Imax = 4.5A

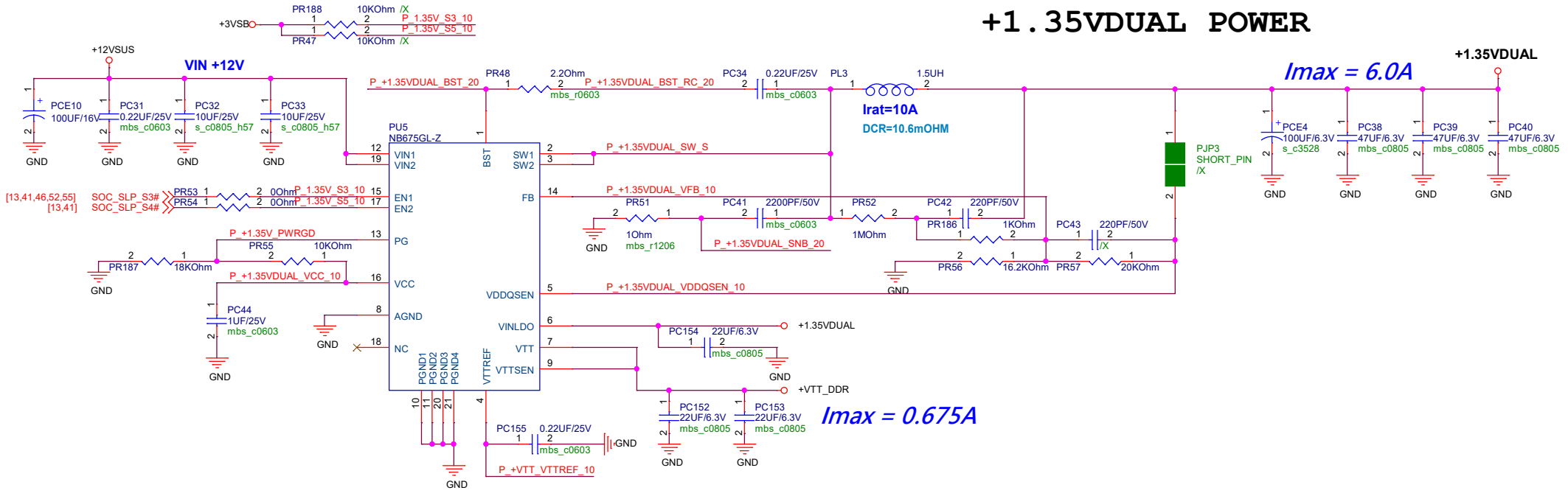


DC INPUT Connector



ASUSTek COMPUTER INC.	Title : +5VSB/+3VSB	
	Engineer: -	
Size: C	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 48 of 57	

+1.35VDUAL POWER



S3 And S5 Truth Table

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off
OTHERS	Hi	Low	Off	Off	Off

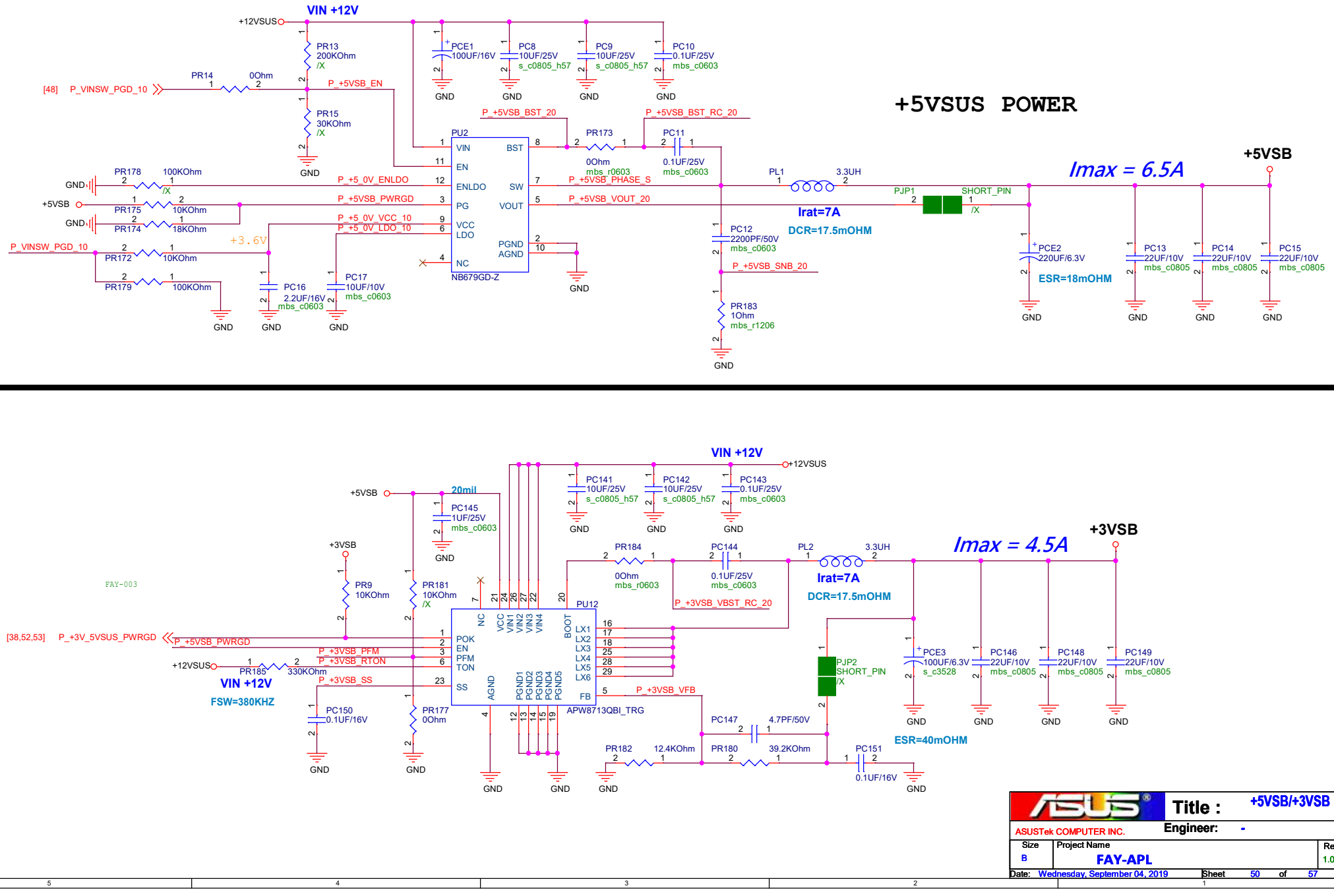
ASUSTeK COMPUTER INC.

Title : +1.35VDUAL

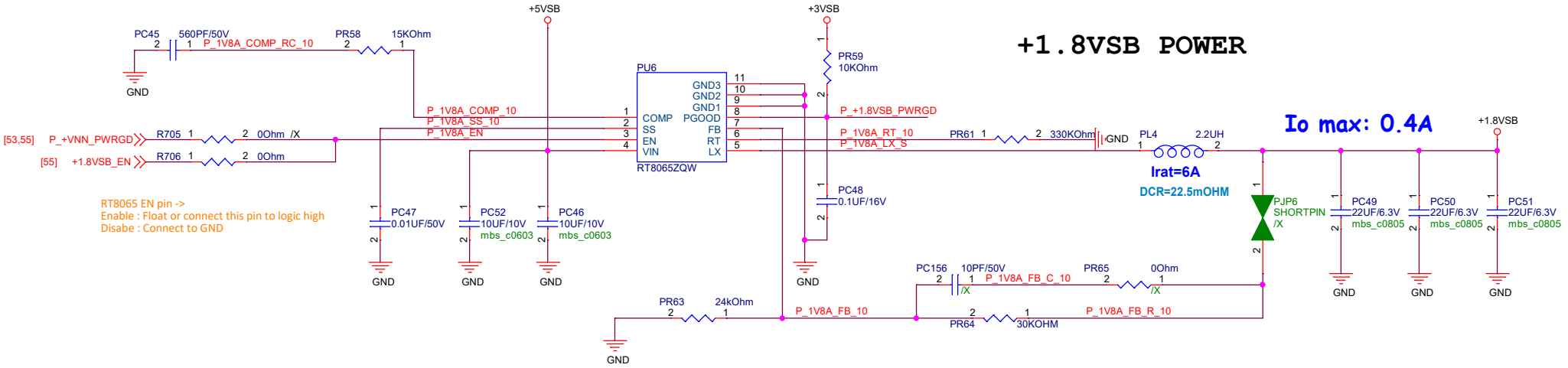
Engineer:

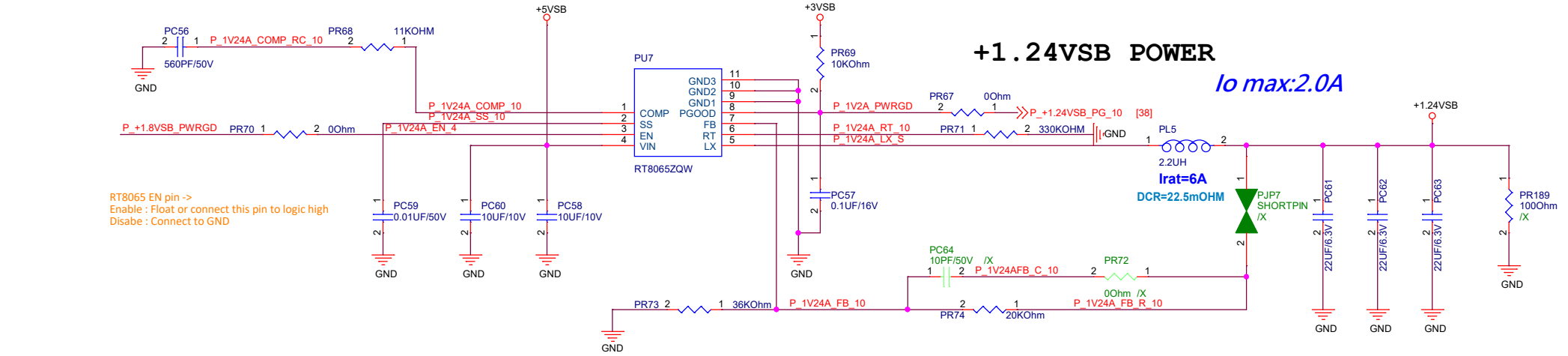
Size	Project Name	Rev
B	FAY-APL	1.00

Date: Tuesday, August 20, 2019 Sheet 49 of 57

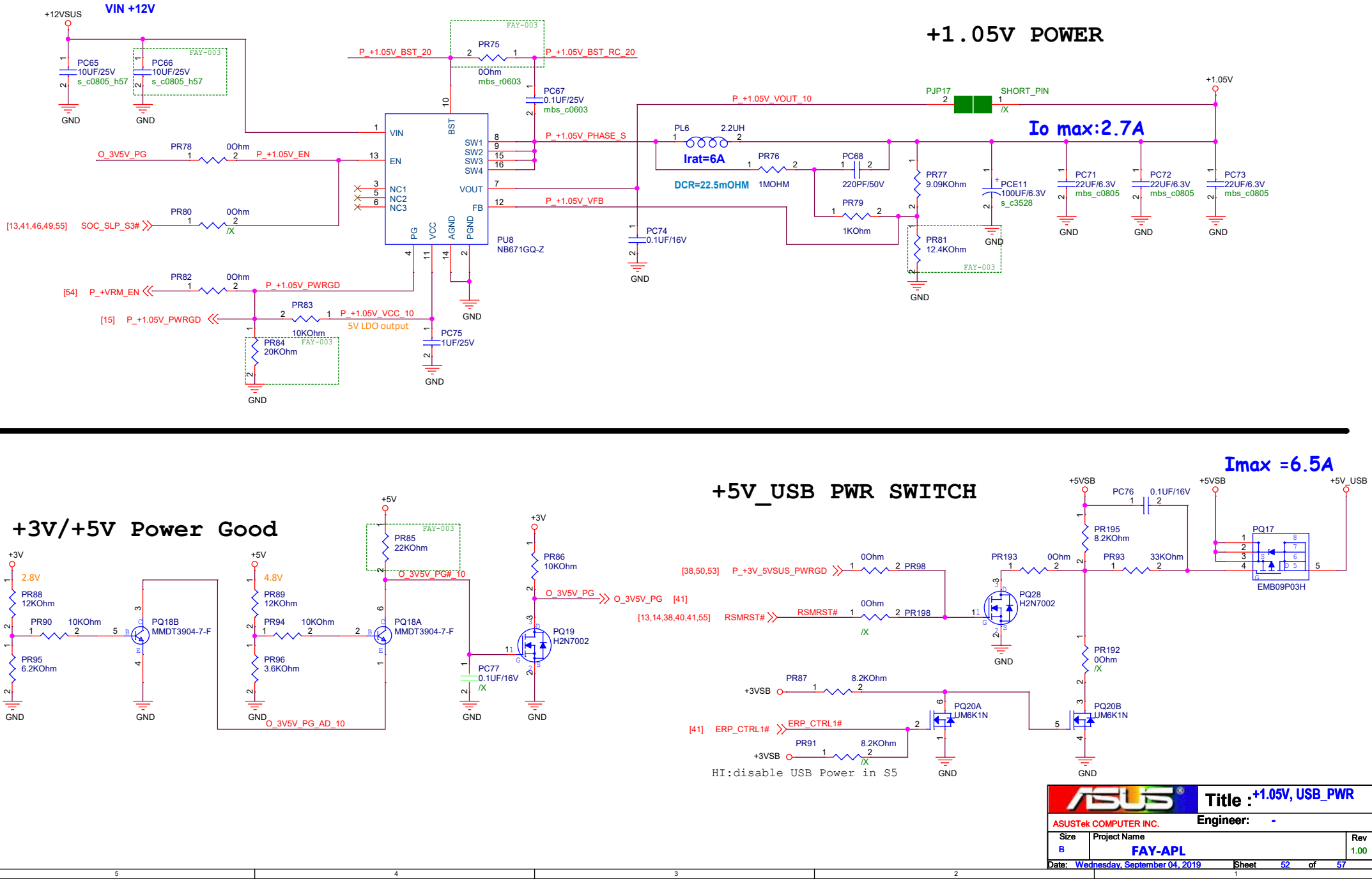


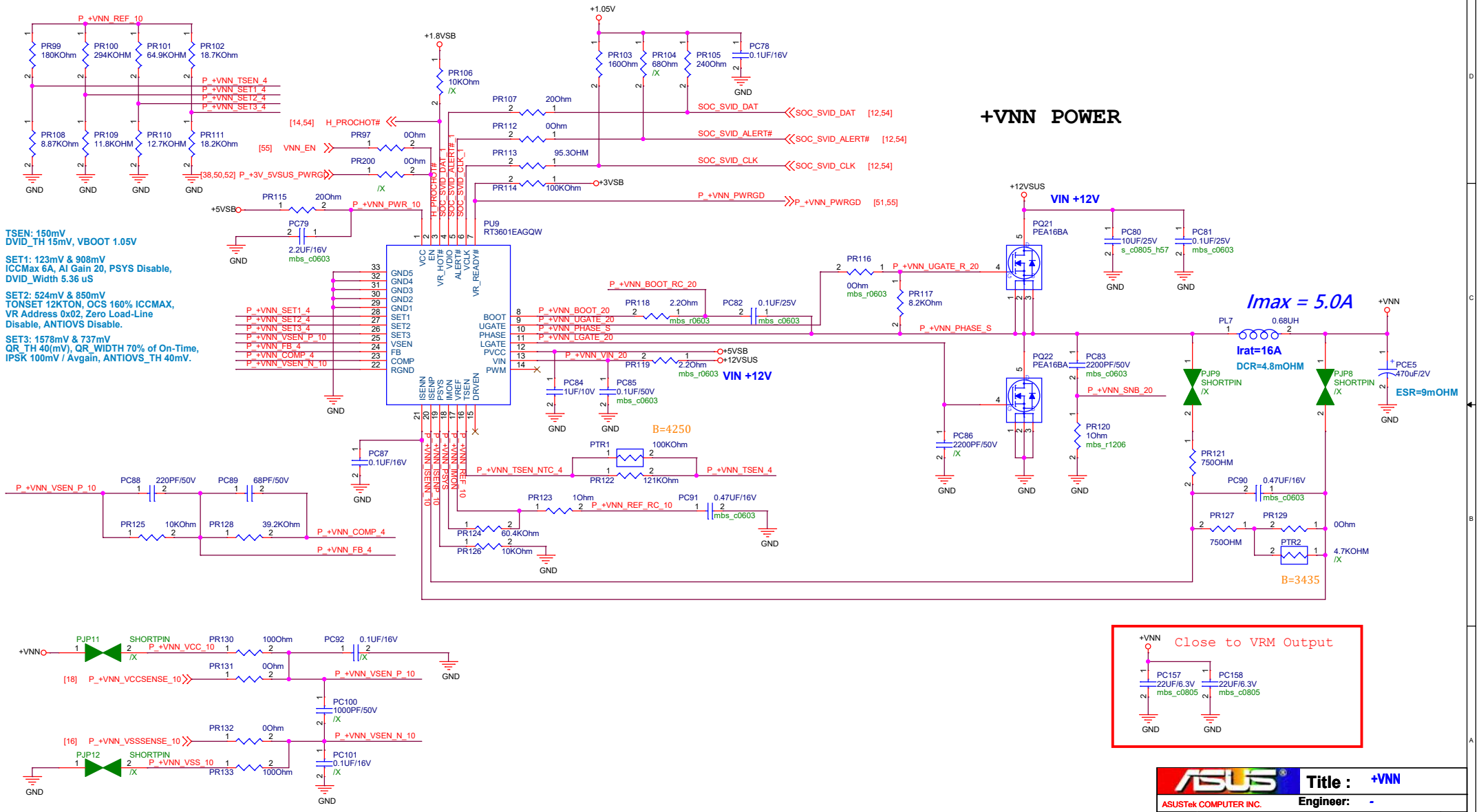
ASUSTek COMPUTER INC.	Title : +5VSB/+3VSB	
	Engineer: -	
Size: B	Project Name: FAY-APL	Rev: 1.00
Date: Wednesday, September 04, 2019	Sheet 50 of 57	





ASUSTek COMPUTER INC.	Title : +1.8VSB & +1.24VSB	
	Engineer: -	
Size: B	Project Name: FAY-APL	Rev: 1.00
Date: Friday, August 16, 2019	Sheet 51 of 57	


+1.05V POWER
VIN +12V
+12VSUS
PC65 10UF/25V s_c0805_h57
PC66 10UF/25V s_c0805_h57
FAY-003
GND
P_+1.05V_BST_20
PR75 0Ohm mbs_r0603
P_+1.05V_BST_RC_20
PC67 0.1UF/25V mbs_c0603
P_+1.05V_VOUT_10
PJP17 SHORT_PIN /X
+1.05V
Io max:2.7A
P_+1.05V_PHASE_S
PL6 2.2UH
Irat=6A
DCR=22.5mOHM
PR76 1MOHM
PC68 220PF/50V
PR77 9.09KOhm
PCE11 100UF/6.3V s_c3528
PC71 22UF/6.3V mbs_c0805
PC72 22UF/6.3V mbs_c0805
PC73 22UF/6.3V mbs_c0805
PR78 0Ohm
O_3V5V_PG
P_+1.05V_EN
PR80 0Ohm /X
[13,41,46,49,55] SOC_SLP_S3#
VIN
EN
BST
SW1
SW2
SW3
SW4
NC1
NC2
NC3
VOUT
FB
PG
VCC
AGND
PGND
PU8 NB671GQ-Z
P_+1.05V_VFB
PC74 0.1UF/16V
PR79 1KOhm
PR81 12.4KOhm
PR82 0Ohm
[54] P_+VRM_EN
P_+1.05V_PWRGD
[15] P_+1.05V_PWRGD
PR83 10KOhm
P_+1.05V_VCC_10
5V LDO output
PR84 20KOhm
PC75 1UF/25V
+3V/+5V Power Good
+3V
+5V
2.8V
4.8V
PR88 12KOhm
PR90 10KOhm
PR95 6.2KOhm
PQ18B MMDT3904-F
PR89 12KOhm
PR94 10KOhm
PR96 3.6KOhm
PQ18A MMDT3904-F
PR85 22KOhm
O_3V5V_PG#_10
O_3V5V_PG_AD_10
PR86 10KOhm
O_3V5V_PG
[41]
PC77 0.1UF/16V /X
PQ19 H2N7002
+5V_USB PWR SWITCH
Imax =6.5A
+5VSB
+5V_USB
[38,50,53] P_+3V_5VSUS_PWRGD
PR98 0Ohm
PR193 0Ohm
PQ28 H2N7002
[13,14,38,40,41,55] RSMRST#
PR198 0Ohm /X
PC76 0.1UF/16V
PR195 8.2KOhm
PR93 33KOhm
PQ17 EMB09P03H
PR192 0Ohm /X
PR87 8.2KOhm
+3VSB
[41] ERP_CTRL1#
PQ20A UM6K1N
PQ20B UM6K1N
PR91 8.2KOhm /X
HI:disable USB Power in S5
Title :+1.05V, USB_PWR
ASUSTek COMPUTER INC.
Engineer: -
Size B
Project Name FAY-APL
Rev 1.00
Date: Wednesday, September 04, 2019
Sheet 52 of 57


+VNN POWER
TSEN: 150mV
DVID_TH 15mV, VBOOT 1.05V
SET1: 123mV & 908mV
ICCMax 6A, AI Gain 20, PSYS Disable,
DVID_Width 5.36 uS
SET2: 524mV & 850mV
TONSET 12KTON, OCS 160% ICCMAX,
VR Address 0x02, Zero Load-Line
Disable, ANTIOVS Disable.
SET3: 1578mV & 737mV
QR_TH 40(mV), QR_WIDTH 70% of On-Time,
IPSK 100mV / Avgain, ANTIOVS_TH 40mV.
VIN +12V
Imax = 5.0A
Irat=16A
DCR=4.8mOHM
ESR=9mOHM
B=4250
B=3435
Close to VRM Output
PU9
RT3601EAGQW
PQ21
PEA16BA
PQ22
PEA16BA
PL7
0.68UH
PJP8
PJP9
PJP11
PJP12
SHORTPIN
PTR1
PTR2
+VNN
Title : +VNN
ASUSTek COMPUTER INC.
Engineer: -
Size Custom
Project Name FAY-APL
Rev 1.00
Date: Tuesday, September 03, 2019
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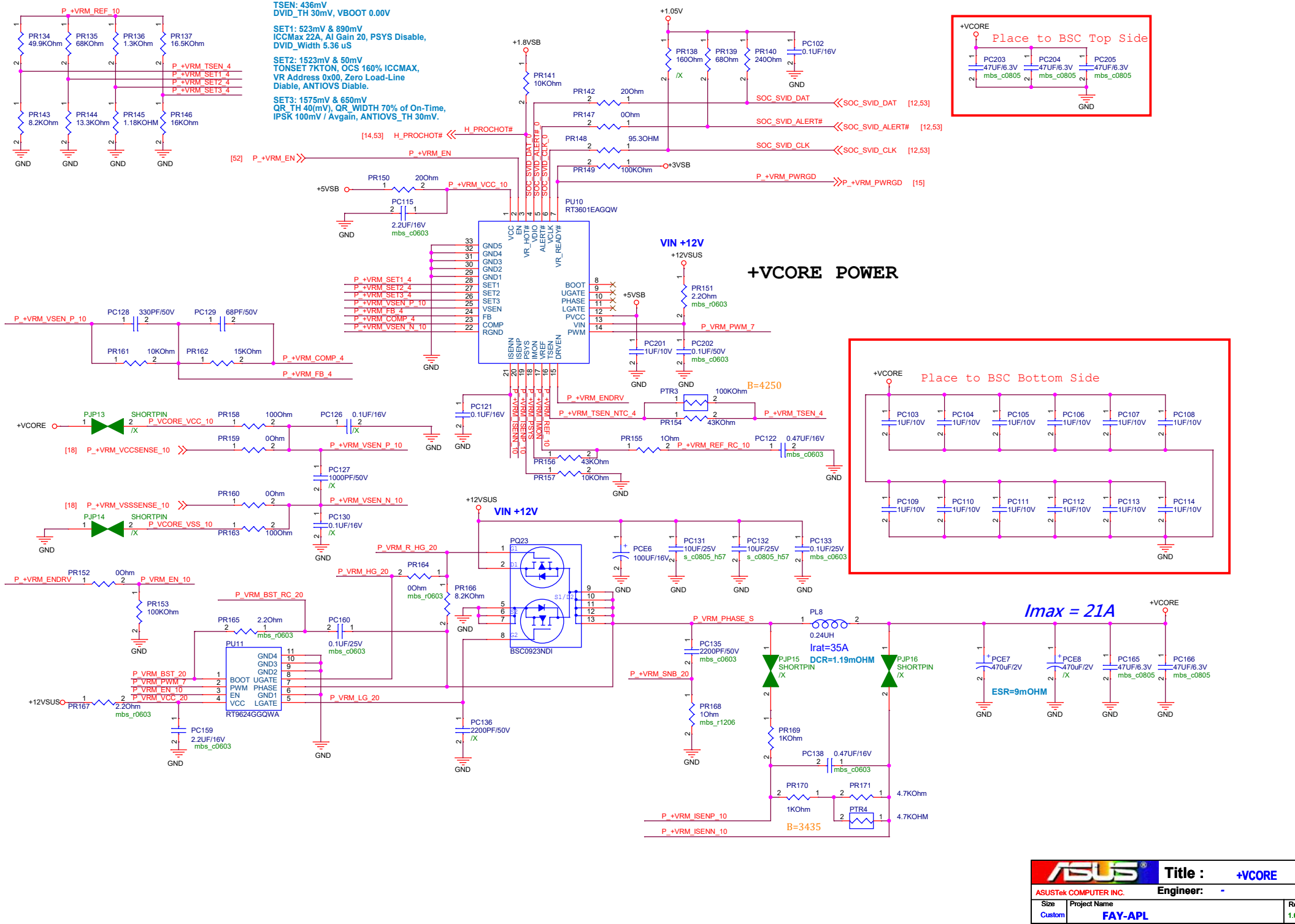
TSEN: 436mV
DVID_TH 30mV, VBOOT 0.00V
SET1: 523mV & 890mV
ICCMax 22A, AI Gain 20, PSYS Disable,
DVID_Width 5.36 uS
SET2: 1523mV & 50mV
TONSET 7KTON, OCS 160% ICCMAX,
VR Address 0x00, Zero Load-Line
Diable, ANTIOVS Diable.
SET3: 1575mV & 650mV
QR_TH 40(mV), QR_WIDTH 70% of On-Time,
IPSK 100mV / Avgain, ANTIOVS_TH 30mV.
+VCORE POWER
VIN +12V
Place to BSC Top Side
Place to BSC Bottom Side
Imax = 21A
ESR=9mOHM
Irat=35A
DCR=1.19mOHM
B=4250
B=3435
RT3601EAGQW
RT9624GGQWA
BSC0923NDI
SOC_SVID_DAT
SOC_SVID_ALERT#
SOC_SVID_CLK
P_+VRM_PWRGD
H_PROCHOT#
P_+VRM_EN
P_+VRM_VCC_10
P_+VRM_PWM_7
P_+VRM_ENDRV
P_+VRM_TSEN_NTC_4
P_+VRM_TSEN_4
P_+VRM_REF_RC_10
P_+VRM_VSEN_P_10
P_+VRM_VSEN_N_10
P_+VRM_COMP_4
P_+VRM_FB_4
P_+VRM_HG_20
P_+VRM_LG_20
P_+VRM_PHASE_S
P_+VRM_SNB_20
P_+VRM_ISENP_10
P_+VRM_ISENN_10
P_+VRM_BST_RC_20
P_+VRM_BST_20
P_+VRM_VSEN_P_10
P_+VRM_VSEN_N_10
P_+VRM_VSENSE_10
P_+VRM_VSSSENSE_10
P_+VRM_VCCSENSE_10
P_VCORE_VCC_10
P_VCORE_VSS_10
P_+VRM_REF_10
P_+VRM_TSEN_4
P_+VRM_SET1_4
P_+VRM_SET2_4
P_+VRM_SET3_4
P_+VRM_VSEN_P_10
P_+VRM_FB_4
P_+VRM_COMP_4
P_+VRM_VSEN_N_10
P_+VRM_ENDRV
P_+VRM_EN_10
P_+VRM_VCC_20
P_+VRM_PWM_7
P_+VRM_EN_10
P_+VRM_HG_20
P_+VRM_LG_20
P_+VRM_BST_20
P_+VRM_BST_RC_20
P_+VRM_PHASE_S
P_+VRM_SNB_20
P_+VRM_ISENP_10
P_+VRM_ISENN_10
P_+VRM_TSEN_NTC_4
P_+VRM_TSEN_4
P_+VRM_REF_RC_10
P_+VRM_PWRGD
H_PROCHOT#
SOC_SVID_DAT
SOC_SVID_ALERT#
SOC_SVID_CLK
+1.05V
+1.8VSB
+5VSB
+3VSB
+12VSUS
+VCORE
GND
PR134 49.9KOhm
PR135 68KOhm
PR136 1.3KOhm
PR137 16.5KOhm
PR143 8.2KOhm
PR144 13.3KOhm
PR145 1.18KOHM
PR146 16KOhm
PR138 160Ohm
PR139 68Ohm
PR140 240Ohm
PC102 0.1UF/16V
PR141 10KOhm
PR142 20Ohm
PR147 0Ohm
PR148 95.3OHM
PR149 100KOhm
PR150 20Ohm
PC115 2.2UF/16V mbs_c0603
PU10
PR151 2.2Ohm mbs_r0603
PC201 1UF/10V
PC202 0.1UF/50V mbs_c0603
PC203 47UF/6.3V mbs_c0805
PC204 47UF/6.3V mbs_c0805
PC205 47UF/6.3V mbs_c0805
PC103 1UF/10V
PC104 1UF/10V
PC105 1UF/10V
PC106 1UF/10V
PC107 1UF/10V
PC108 1UF/10V
PC109 1UF/10V
PC110 1UF/10V
PC111 1UF/10V
PC112 1UF/10V
PC113 1UF/10V
PC114 1UF/10V
PTR3 100KOhm
PR154 43KOhm
PC121 0.1UF/16V
PR155 1Ohm
PC122 0.47UF/16V mbs_c0603
PR156 43KOhm
PR157 10KOhm
PC128 330PF/50V
PC129 68PF/50V
PR161 10KOhm
PR162 15KOhm
PJP13 SHORTPIN /X
PR158 100Ohm
PC126 0.1UF/16V /X
PR159 0Ohm
PC127 1000PF/50V /X
PJP14 SHORTPIN /X
PR160 0Ohm
PR163 100Ohm
PC130 0.1UF/16V /X
PR152 0Ohm
PR153 100KOhm
PR164 0Ohm mbs_r0603
PR165 2.2Ohm mbs_r0603
PC160 0.1UF/25V mbs_c0603
PR166 8.2KOhm
PU11
PR167 2.2Ohm mbs_r0603
PC159 2.2UF/16V mbs_c0603
PQ23
PCE6 100UF/16V
PC131 10UF/25V s_c0805_h57
PC132 10UF/25V s_c0805_h57
PC133 0.1UF/25V mbs_c0603
PC135 2200PF/50V mbs_c0603
PC136 2200PF/50V /X
PL8 0.24UH
PJP15 SHORTPIN /X
PJP16 SHORTPIN /X
PCE7 470uF/2V
PCE8 470uF/2V /X
PC165 47UF/6.3V mbs_c0805
PC166 47UF/6.3V mbs_c0805
PR168 1Ohm mbs_r1206
PR169 1KOhm
PC138 0.47UF/16V mbs_c0603
PR170 1KOhm
PR171 4.7KOhm
PTR4 4.7KOHM
Title : +VCORE
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