Appendix A:

AAECON Embedded Controller

API Protocol

Rev 0.1
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Department: AAEON / DSD

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History

VERSION	DATE	DESCRIPTION	Editor
V0.1	06/23/2012	First draft release.	Elf Lo
V0.4	03/25/2014	Support EC Thermal Alert Function.	Elf Lo
V0.5	04/11/2016	Updating SPEC bases on IT8528 chip. Add ‘Power Manger Feature’ chapter. Add ‘Restore On AC Power Loss function’ definition.	Elf Lo

Index

T.B.D

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1. Introduction

AAEON EC API is used to communicate with OS / DRIVER / SDK to configure EC provides functions by ***I/O Port.*** **Note 1**.

Note 1:

AAEON I/O Port is defined for service the AAEON EC API Protocol, it's using as follow I/O resource.

Mother Board:	Index/Data Port:	284h/285h
Carrier Board:	Index/Data Port:	280h/281h

Sample:

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EC API Registers Map Table:

Index	R/W	Description
10h	R/W	Logic Device Number Register
11h	R/W	Function and Device Register
12h	R/W	Configuration Register
13h	R/W	Option Register 0
14h	R/W	Option Register 1
15h	R/W	Option Register 2
16h	R/W	Option Register 3
17h	R/W	Option Register 4
18h	R/W	Option Register 5
19h	R/W	Option Register 6
1Ah	R/W	Option Register 7
1Bh	R/W	Option Register 8
1Ch	R/W	Option Register 9
1Dh	R/W	Option Register A
1Eh	R/W	Option Register B
1Fh	R/W	Option Register C

LDNR — Logic Device Number Register

Index Address: 10h

Bit	R/W	Description
7:0	R/W	**Logic Device Number** Reference with 'Logic Device and Function Map table' for more detail.

FNDR — Function and Device Register

Index Address: 11h

Bit	R/W	Description
7:0	R/W	**Function and Device** Reference with 'Logic Device and Function Map table' for more detail.

CONFR — Configuration Register

Index Address: 12h

Bit	R/W	Description
7:6	-	**Reserved**
5	R/W	**Data Register Read/Write Setting** 1b: Write 0b: Read
4	R/W	**API Active Setting** 1b: Enable API service. (It will be cleared after service activate)
3	R	**Reserved** **Sub Controller Access error.**
2	R	**API Progress status (It will set to b'1' during API Service enabled)** 1: API Progressing 0: None
1	R	**API Operation Fail Status (Return API operating status after API progress)** 1: API Operation fail. 0: None
0	R	**API Operation Done Status (Return API operating status after API progress)** 1: API Operation Done 0: None

OPRn — Option Register (0Ch-00h)

Index Address: 1Fh-13h

Bit	R/W	Description
7-0	R/W	API Data Buffer.

Logic Device and Function Map Table:

LDNR	FNDR	Description
A1h	-	EC Firmware Information Function
	02h	EC Firmware Information
A2h	-	Dynamic Digital Input/Output Function
	00h	Flexible I/O Direction Configuration
	01h	Flexible I/O Level Configuration
	02h	Flexible I/O Use Select Configuration
	03h	Flexible I/O Interrupt Mode Configuration
A3h	-	HAT
A5h	-	Hardware Monitor Controller
	00h	System Temperature Information
	02-01h	Internal ADC Function
	10h	PWM Controller Function
A6h	-	SMART FAN Function
	00h	FAN1 Configuration
	01h	FAN2 Configuration
A7h		SMBUS/I2C/SPI Host Controller
	00h	AAEON Internal debug use.
	01h	SMBUS Host Controller 1
	02h	SMBUS Host Controller 2
	03h	SMBUS Host Controller 3
	04h	SMBUS Host Controller 4
A7h	10h	SPI Host Controller - reserve
	11h	SPI Host Controller

A8h	-	System Protect Function
	00h	Watchdog Configuration
A9h	-	Power Manager Function
		//Wake Function
AAh	-	Panel Backlight Controller
	00h	Backlight Configuration
	01h	Brightness Curves Setting
ABh		Alert Event Function
	00h	
	01h	
B1h	-	SMART Battery 1 Function
	00h	Battery Information DAT0
	01h	Battery Information DAT1
B2h	-	SMART Battery 2 Function
	00h	Battery Information DAT0
	01h	Battery Information DAT1
C0h~CFh	-	Customer OEM Function Define
C0h	-	Brightness Controller Function
	00	Brightness Configuration

LDNR	FNDR	Description
C0h~CFh	-	Customer OEM Function Define
C0h	-	Brightness Controller Function
	00	Brightness Configuration
C5h	00	S3 Alarm Function.
		Battery Capacity Alarm.
		System wil be woken when battery capacity is under BatAlarm register.

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Logic Device and Function Map Table:

LDNR	FNDR	Description
01h	-	SMRA1 0100h Device Register Access
16h	-	GPIO Device Register Access
18h	--	PWM Device Register Access
19h	-	ADC Device Register Access
1Ah	-	DAC Device Register access

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Logical Device A1h: EC Firmware Information Function

Function and Device 01h: EC Firmware Information

OPRn	R/W	Description
00h	R	Board Information Register.
01h	R	Year Register (High Byte)
02h	R	Year Register (Low Byte)
03h	R	Month Register
04h	R	Date Register
0C-05h	R	EC firmware version Register.

Option Register 00h: EC Board Information Register

Bit	R/W	Default	Description
7-1	-	-	Reserved
0	R	-	EC Board Type 0: Carrier Board or Single Board. 1: Mother Board.

Option Register 01h: Year Register (High Byte)

Bit	R/W	Default	Description
7-0	R	-	Indicate the build date of years (High Byte) ex. Return 20h as year 2012.

Option Register 02h: Year Register (High Byte)

Bit	R/W	Default	Description
7-0	R	-	Indicate the build date of years (Low Byte) ex. Return 12h as year 2012.

Option Register 03h: Month Register

Bit	R/W	Default	Description
7-0	R	-	Indicate the build date of Month. ex. Return 10h as October.

Option Register 04h: Date Register

Bit	R/W	Default	Description
7-0	R	-	**Indicate the build date of date.** ex. Return 21h as twenty-first.

Option Register 0C-05h: EC firmware version Register

Bit	R/W	Default	Description
7-0	R	-	**Indicate EC Firmware Version String in ASCII Code.** ex. CM77BE10 Return 43h of Option Register 05. Return 47h of Option Register 06. ….. Return 31h of Option Register 0B. Return 30h of Option Register 0C.

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Logical Device A2h: Flexible I/O Function

Function and Device 00h: Flexible I/O Direction Configuration

OPRn	R/W	Description
00h	R	Amount of flexible I/O are supported.
08-01h	R/W	Flexible I/O Direction setting… (DIO 63-55) … (DIO 7-0)

Option Register 00h: Digital Input/Output amount

Bit	R/W	Default	Description
7-0	R/W	-	The number of “Digital Input/Output” supports in the project.

Option Register 08h-01h: Digital Input/Output Pin Mode Register

Bit	R/W	Default	Description
7-0	R/W	-	Indicate the flexible I/O Pin Operating mode for (DIO 63-55) … (DIO 7-0). 0: Output 1: Input

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Function and Device 01h: Flexible I/O Status and Level Configuration

OPRn	R/W	Description
00h	R	Flexible I/O amount
08-01h	R/W	Flexible Status and Level Register
0C-09h	-	Reserved

Option Register 00h: Flexible I/O amount

Bit	R/W	Default	Description
7-0	R/W	-	The number of "Digital Input/Output" supports in the project.

Option Register 08-01h: Flexible Status and Level Register

Bit	R/W	Default	Description
7-0	R/W	-	In the output mode, reading returns the last written date for each Individual DIO pin (DIO 63-55) … (DIO 7-0). In the input mode, reading this register returns the pin level status. 0: Pin Level States Low. 1: Pin Level States High.

Function and Device 02h: Flexible I/O Use Select Configuration

OPRn	R/W	Description
00h	R	Amount of Flexible I/O
04-01h	R/W	Flexible I/O Use Select Register

Option Register 00h: Amount of Flexible I/O

Bit	R/W	Default	Description
7-0	R/W	-	The number of "Digital Input/Output" supports in the project.

Option Register 04-01h: Flexible I/O Use Select Register

Bit	R/W	Default	Description
31-0	R/W	-	FlexIO_USE_SEL[31:0] — R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO.

Function and Device 03h: Flexible I/O Interrupt Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R/W	Flexible I/O Interrupt Configuration

Option Register 04-01h: Flexible I/O Interrupt Register

Bit	R/W	Default	Description
31-0	R/W	-	FlexIO_INT [31:0]— R/W: If FlexIO[n] is programmed to be an Input (via the corresponding bit in the FlexIO_IO_SEL register), then the corresponding FlxeIO_INT[n] bit can be programmed to support interrupt function. 1 = Enable, 0 = Disable.

Function and Device 04h: Flexible I/O Interrupt Polarity Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R/W	Flexible I/O Interrupt Configuration

Option Register 04-01h: Flexible I/O Interrupt Polarity Register

Bit	R/W	Default	Description
31-0	R/W	-	FlxeIO_POL [31:0]— R/W: If GPIO[n] is programmed to be an Interrupt function (via the corresponding bit in the FlexIO_INT register), then the interrupt polarity can be programmed by corresponding FlxeIO_POL[n] bit. 1: Reserve (Level High) 0: Level Low.

Function and Device 05h: Flexible I/O Interrupt Mode Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R/W	Flexible I/O Interrupt Mode Configuration

Option Register 04-01h: Flexible I/O Interrupt Mode Register

Bit	R/W	Default	Description
31-0	R/W	-	FlxeIO_INTMOD [31:0]— R/W: If GPIO[n] is programmed to be an Interrupt function (via the corresponding bit in the FlexIO_INT register), then the interrupt mode can be programmed by corresponding FlxeIO_INTMOD [n] bit. 1: Reserve. (Level Mode) 0: Pulse Mode.

Function and Device 06h: Flexible I/O Interrupt Status Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R/W	Flexible I/O Interrupt Status Configuration

Option Register 04-01h: Flexible I/O Interrupt Mode Register

Bit	R/W	Default	Description
31-0	R/W	-	FlxeIO_INTSTS [31:0]— R/W: If GPIO[n] is programmed to be an Interrupt function (via the corresponding bit in the FlexIO_INT register), then the interrupt corresponding FlxeIO_INTMOD [n] bit which use to indicate the interrupt is triggered. 1: Interrupt triggered. (Write clear.) 0: N/A.

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Logical Device A3h: AAEON HAT Controller

Function and Device 00h: HAT Feature Version Information

OPRn	R/W	Description
00h	R	Reserve
01h	R	AAEON HAT Major Version
02h	R	AAEON HAT Minor Version

Option Register 01h: AAEON HAT Major Version

Bit	R/W	Default	Description
7-0	R	-	

Option Register 02h: AAEON HAT Minor Version

Bit	R/W	Default	Description
7-0	R	-	

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Function and Device 01h: HAT GPIO Use Select Configuration

OPRn	R/W	Description
00h	R/W	Reserve
04-01h	R/W	HAT GPIO Use Select Register

Option Register 04-01h: HAT GPIO Use Select Register

Bit	R/W	Default	Description
27-0	R/W	-	GPIO_USE_SEL[27:0] — R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO.
31-28	R/W	-	Reserve

Function and Device 02h: HAT GPIO Input/Output Select Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R	Flexible GPIO Input/Output Select Register

Option Register 04-01h: HAT GPIO Input/Output Select Register

Bit	R/W	Default	Description
27-0	R/W	-	GP_IO_SEL[27:0] — R/W. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.
31-28	R/W	-	Reserve

Function and Device 03h: HAT GPIO Level for Input or Output Configuration

OPRn	R/W	Description
00h	R	Reserve
04-01h	R/W	GPIO Level for Input or Output Register

Option Register 04-01h: Flexible GPIO Input/Output Select Register

Bit	R/W	Default	Description
27-0	R/W	-	GP_LVL[27:0]— R/W: If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode.
31-28	R/W	-	Reserve

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Logical Device A5h: Hardware Monitor Controller

Function and Device 00h: System Temperature Information

OPRn	R/W	Description
00h	R	System Thermal Sensor amount.
0C-01h	R	System (01~0C) Temperature Register.

Option Register 00h: System Thermal Sensor amount

Bit	R/W	Default	Description
7-0	R	-	The number of “System Thermal Sensor” supports in the project.

Option Register 0C-01h: System Temperature Register

Bit	R/W	Default	Description
7-0	R/W	-	The System Temperature Register data format is a binary twos complement signed byte format as follow: Returns 7Dh when system temperature reaches 125℃. Returns 19h when system temperature reaches 25℃. Returns 01h when system temperature reaches 1℃. Returns FFh when system temperature reaches -1℃. Returns E7h when system temperature reaches -25℃. Returns C9h when system temperature reaches -55℃.

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Function and Device 01h: ADC sensor Information

OPRn	R/W	Description
00h	R	System ADC sensor amount
01h-02h	R	ADC0 sensor value,10-bit resolution and 0 to 3V input voltage range.
03h-04h	R	ADC1 sensor value,10-bit resolution and 0 to 3V input voltage range.
05h-06h	R	ADC2 sensor value,10-bit resolution and 0 to 3V input voltage range.
07h-08h	R	ADC3 sensor value,10-bit resolution and 0 to 3V input voltage range.

Option Register 00h: System ADC Sensor amount

Bit	R/W	Default	Description
7-0	R	-	The number of “ADC Sensor” are supported in the project.

Option Register 01-01h: System Temperature Register

Bit	R/W	Default	Description
7-0	R/W	-	The System Temperature Register data format is a binary twos complement signed byte format as follow: Returns 7Dh when system temperature reaches 125℃. Returns 19h when system temperature reaches 25℃. Returns 01h when system temperature reaches 1℃. Returns FFh when system temperature reaches -1℃. Returns E7h when system temperature reaches -25℃. Returns C9h when system temperature reaches -55℃.

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Logical Device A5h: Hardware Monitor Controller

Function and Device 10h: PWM Controller.

OPRn	R/W	Description
00h	R	Amount of PWM controllers are supported.
01h	RW	PWM1,2 Configuration register.
02h	RW	PWM3,4 Configuration register.
03h	RW	PWM5,6 Configuration register.
04h	RW	PWM7,8 Configuration register.
0C-05h	RW	PWM8-1 output value configuration register

Option Register 01h : PWM1,2 Configuration register

Bit	R/W	Default	Description
7	R/W	0	PWM2 output enable. 0: Disable PWM1 output 1: Enable PWM1 output.
6	R/W	0	PWM2 invert output. 0: None. 1: Inversion
5:4	rev	-	Reserved
7	R/W	0	PWM1 output enable. 0: Disable PWM1 output 1: Enable PWM1 output.
6	R/W	0	PWM1 invert output. 0: None. 1: Inversion
1:0	R/W	-	Reserved

Option Register 02h : PWM3,4 Configuration register

Bit	R/W	Default	Description
7	R/W	0	PWM4 output enable. 0: Disable PWM4 output 1: Enable PWM4 output.
6	R/W	0	PWM4 invert output. 0: None. 1: Inversion
5:4	rev	-	Reserved
7	R/W	0	PWM3 output enable. 0: Disable PWM3 output 1: Enable PWM3 output.
6	R/W	0	PWM3 invert output. 0: None. 1: Inversion
1:0	R/W	-	Reserved

Option Register 03h : PWM5,6 Configuration register

Bit	R/W	Default	Description
7	R/W	0	PWM6 output enable. 0: Disable PWM6 output 1: Enable PWM6 output.
6	R/W	0	PWM6 invert output. 0: None. 1: Inversion
5:4	rev	-	Reserved
7	R/W	0	PWM5 output enable. 0: Disable PWM5 output 1: Enable PWM5 output.
6	R/W	0	PWM5 invert output. 0: None. 1: Inversion
1:0	R/W	-	Reserved

Option Register 04h : PWM7,8 Configuration register

Bit	R/W	Default	Description
7	R/W	0	PWM8 output enable. 0: Disable PWM8 output 1: Enable PWM8 output.
6	R/W	0	PWM8 invert output. 0: None. 1: Inversion
5:4	rev	-	Reserved
7	R/W	0	PWM7 output enable. 0: Disable PWM7 output 1: Enable PWM7 output.
6	R/W	0	PWM7 invert output. 0: None. 1: Inversion
1:0	R/W	-	Reserved

Option Register 0C-05h : PWM8-1 output value configuration register

Bit	R/W	Default	Description
7-0	R/W	0	256 step PWM output value. Output duty cycle = value/255 * 100%

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Logical Device A7h: **SMBUS/I2C/SPI Host Controller**

Function and Device 00h:

OPRn	R/W	Description

Option Register 00h:

Bit	R/W	Default	Description

Option Register 0C-01h:

Bit	R/W	Default	Description

Function and Device 01-04h: SMBUS/I2C Host Controller 1, 2, 3, 4

OPRn	R/W	Description
00h	R	Host Controller Status Register
01h	R	Host Control Register
02h	R	Transmit Slave Address Register
03h	R/W	Host Command Register
04h	R/W	Data Low Byte Register
05h	R/W	Data High Byte Register

Option Register 00h: Host Controller Status Register

Bit	R/W	Default	Description
0	R		Host Busy (HOBY)

Option Register 01h: Host Control Register

Bit	R/W	Default	Description
7-3	R/W	0	Reserved
4-2	R/W	0	001: Send Byte / Receive Byte 010: Write Byte / Read Byte 011: Write Word / Read Word
1-0	R/W	0	Reserved

Option Register 02h: Transmit Slave Address Register

Bit	R/W	Default	Description
7-1	R/W	00h	Address of the targeted slave.
0	R/W	0b	Direction of the host transfer. 0: Write 1: Read

Option Register 03h: SMBUS/I2C Host Command Register

Bit	R/W	Default	Description
7-0	R/W	-	These bits are transmitted in the command field of the SMBus protocol.

Option Register 04h: Data Low Byte Register

Bit	R/W	Default	Description
7-0	R/W	00h	The Data Byte Low (first transaction Data Byte) of the SMBus protocol.

Option Register 05h: Data 1 Register

Bit	R/W	Default	Description
7-0	R/W	00h	The Data Byte High of the SMBus protocol.

Function and Device 01-04h: SMBUS/I2C Host Controller 1, 2, 3, 4

OPRn	R/W	Description
00h	R	Host Controller Status Register
01h	R	Host Control Register
02h	R	Transmit Slave Address Register
03h	R/W	Host Command Register
04h	R/W	Data Low Byte Register
05h	R/W	Data High Byte Register

Option Register 00h: Host Controller Status Register

Bit	R/W	Default	Description
0	R		Host Busy (HOBY)

Option Register 01h: Host Control Register

Bit	R/W	Default	Description
7-3	R/W	0	Reserved
4-2	R/W	0	001: Send Byte / Receive Byte 010: Write Byte / Read Byte 011: Write Word / Read Word
1-0	R/W	0	Reserved

Option Register 02h: Transmit Slave Address Register

Bit	R/W	Default	Description
7-1	R/W	00h	Address of the targeted slave.
0	R/W	0b	Direction of the host transfer. 0: Write 1: Read

Option Register 03h: SMBUS/I2C Host Command Register

Bit	R/W	Default	Description
7-0	R/W	-	These bits are transmitted in the command field of the SMBus protocol.

Option Register 04h: Data Low Byte Register

Bit	R/W	Default	Description
7-0	R/W	00h	The Data Byte Low (first transaction Data Byte) of the SMBus protocol.

Option Register 05h: Data 1 Register

Bit	R/W	Default	Description
7-0	R/W	00h	The Data Byte High of the SMBus protocol.

Function and Device 11h: SPI Host Controller

OPRn	R/W	Description
00h	R/W	SPI Status Register (SPICSTS)
01h	R/W	SPI Configuration Register 1 (SPICONF1)
02h	R/W	SPI Configuration Register 2 (SPICONF2)
03h	R/W	SPI Configuration Register 3 (SPICONF3)
04h	R/W	Reserved
05h	R/W	SPI Data Register (SPIDATA)

Option Register 00h: SPI Control/Status Register (SPICSTS)

Bit	R/W	Default	Description
7	R/W	-	Reserved
6	R	-	Device Busy Signal (DEVBUSY) The bit indicates the device busy signal.
5	R/WC	0b	SPI Transmission End (TRANED) Wirte 1 to end the SPI transmission.
4	R/W	0b	Channel 0 Enable (CH0Enable) 0: Disable 1: Enable Channel 0 for SPI communication
3	R/W	0b	Channel 1 Enable (CH0Enable) 0: Disable 1: Enable Channel 0 for SPI communication
2	R	0b	Transfer In Progress (TRANIP) This bit indicates the SPI is in the transmission state. 0: Data transfer is not in progress. 1: Data transfer is in progress.
1	R/WC	0b	Transfer End Flag (TRANENDIF) This bit indicates SPI transmission ends. The bit will be 1 when writing 1 to TRANEND bit. Write 1 to clear this bit and terminate data transmission.
0	R	0b	SPI Busy (SPIBUSY) This bit indicates whether the SPI interface is busy or not. 0: SPI idle 1: SPI busy

Option Register 01h: SPI Configuration Register 1 (SPICONF1)

Bit	R/W	Default	Description
7	R/W	0b-	Chip Select Polarity (CHPOL) If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 0. Otherwise, the bit indicates both the chip select polarity of device 0 and device 1. 0: Active low 1: Active high
6-5	R/W	00b	Bit 6: Clock Polarity (CLPOL) 0: SSCK is low in the idle mode 1: SSCK is high in the idle mode. Bit 5: 0: Latch data on the first SSCK edge. 1: Latch data on the second SSCK edge. 00b: SSCK is low in the idle mode. Data is sampled on the rising edge. 01b: SSCK is low in the idle mode. Data is sampled on the falling edge. 10b: SSCK is high in the idle mode. Data is sampled on the rising edge. 11b: SSCK is high in the idle mode. Data is sampled on the falling edge.
4-2	R/W	000b	SSCK Frequency (SCKFREQ) 000B: 9.2MHz / 2 001B: 9.2MHz / 4 010B: 9.2MHz / 6 011B: 9.2MHz / 8 100B: 9.2MHz / 10 101B: 9.2MHz / 12 110B: 9.2MHz / 14 111B: 9.2MHz / 16
1	R/W	0b	
0	R/W	0b	SPI0 3-Wire Mode Support 0: 4 Wire Mode 1: 3 Wire Mode

Option Register 02h: SPI Configuration Register 2 (SPICONF2)

Bit	R/W	Default	Description
7-6	R/W	0b-	Reserved
5-3	R/W	000b	Data Width (DATAWIDTH) 000b: 8-bit transmission 001b: 1-bit transmission 010b: 2-bit transmission 011b: 3-bit transmission 100b: 4-bit transmission 101b: 5-bit transmission 110b: 6-bit transmission 111b: 7-bit transmission
2	R/W	0b	Channel Read/Write Cycle (CHRW) 0: Write cycle 1: Read cycle
1	R/W	0b	Reserved
0	R/W	0b	SPI1 3-Wire Mode Support 0: 4 Wire Mode 1: 3 Wire Mode

Option Register 03h: SPI Configuration Register 3 (SPICONF3)

Bit	R/W	Default	Description
7-3	R/W	0b-	Reserve
2	R/W	0b	Chip Select Polarity Select (CSPOLSEL) 0: The chip select polarity of SPI 1 and SPI 0 is the same. 1: The chip select polarity of SPI 1 and SPI 0 is different.
1	R/W	0b	Chip Select Polarity (CHPOL1) If CSPOLSEL is set to 1, the bit indicates the chip select polarity of SPI 1. 0: Active low 1: Active high
0	R/W	0b	SPI1 3-Wire Mode Support 0: 4 Wire Mode 1: 3 Wire Mode

Option Register 05h: SPI Data Register (SPIDATA)

Bit	R/W	Default	Description
7-0	R/W	0b-	SPI Data Register

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Logical Device A8h: System Protection

Function and Device 00h: Watchdog Configuration

OPRn	R/W	Description
00h	R/W	Watchdog Timer Configuration Register
01h	R/W	Watchdog Configuration Register.
0C-02h	-	Reserved

Option Register 00h: Watchdog Timer Configuration Register

Bit	R/W	Default	Description
7-0	R/W	00h	**Time of watchdog unit. (1~255)** 0: Stop watchdog counter.

Option Register 01h: Watchdog Configuration Register

Bit	R/W	Default	Description
7:4	R/W	-	Reserved
3:2	R/W	00b	**Pulse Width** 00 = 20ms 01 = 60ms 10 = 100ms 11 = 250ms
1	R/W	0b	**Pulse Type** 0 = High Active 1 = Low Active
0	R/W	0b	**Time Setting** 0 = Second 1 = Minute

Alert Event Function (reserved)	Logical Device	Function & Device
	ABh	00h

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Thermal 1 Alert Event Configuration	Logical Device	Function & Device
	ABh	01h

Option Register 00h: Thermal Alert Event 1 Enable Register

Bit	R/W	Default	Description
7	R/WC	0b	Enable TAE1 temperature 4 status.
6	R/WC	0b	Enable TAE1 temperature 3 status.
5	R/WC	0b	Enable TAE1 temperature 2 status.
4	R/WC	0b	Enable TAE1 temperature 1 status.
3	R/W	0h	Enable TAE1 temperature 4 alert event.
2	R/W	0h	Enable TAE1 temperature 3 alert event.
1	R/W	0h	Enable TAE1 temperature 2 alert event.
0	R/W	0h	Enable TAE1 temperature 1 alert event.

Option Register 01h:

Bit	R/W	Default	Description
7-4	-	0h	Reserved
3-0	R/W	0h	Select alert temperature source.

Option Register 02h:

Bit	R/W	Default	Description
7-4	-	0h	Reserved
3	R/W	0h	Select temperature 4 alert mode. 0: Falling Trigged 1: Rising Trigged
2	R/W	0h	Select temperature 3 alert mode. 0: Falling Trigged 1: Rising Trigged
1	R/W	0h	Select temperature 2 alert mode. 0: Falling Trigged 1: Rising Trigged
0	R/W	0h	Select temperature 1 alert mode. 0: Falling Trigged 1: Rising Trigged

Option Register 03h:

Bit	R/W	Default	Description
7	–	-	Reserved
6-0	R	-	Current alter temperature.

Option Register 04h:

Bit	R/W	Default	Description
7	–	-	Reserved
6-0	R	-	TAE1 temperature 1 limit register

Option Register 05h:

Bit	R/W	Default	Description
7	–	-	Reserved
6-0	R	-	TAE1 temperature 2 limit register

Option Register 06h:

Bit	R/W	Default	Description
7	–	-	Reserved
6-0	R	-	TAE1 temperature 3 limit register

Option Register 07h:

Bit	R/W	Default	Description
7	–	-	Reserved
6-0	R	-	TAE1 temperature 4 limit register

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Logical Device A9h: Power Manager Function

Function and Device 00h: Restore On AC Power Loss

OPRn	R/W	Description
00h	R/W	Restore On AC Power Loss Configuration Register

Option Register 00h: Restore On AC Power Loss Configuration Register

Bit	R/W	Default	Description
7:2	R	-	Reserved
1:0	R/W	0b	Select AC power state when power is re-applied after a power failure. 00: Power Off 01: Power On 10: Last State 11: Bypass

Logical Device : SMART Battery Function B0h

Function and Device 00h: System support Features

OPRn	R/W	Description
00h	-	Reserved.
01h	R/W	AAEON Features.

Option Register 01: AAEON features.

Bit	R/W	Default	Description
7-4	R	-	Reserved
3-0	R/W	0	Amount of batteries which are supported.

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Logical Device : SMART Battery Function (B1h & B2h)

Function and Device 00h: Battery Information DAT0

OPRn	R/W	Description
00h	R	System Information
01h	R	Battery Information
03-02h	R	Battery Design Capacity
05-04h	R	Battery Full Charge Capacity
07-06h	R	Battery Design Voltage

Option Register 00h: System Information

Bit	R/W	Default	Description
7-1			Reserved
0	R		Power Source Device Present 0 – Not present 1 – Present

Option Register 01h: Battery Information

Bit	R/W	Default	Description
7-4	R	-	Reserved
3-1	R	-	Battery State Bit values. Notice that the Charging bit and the Discharging bit are mutually exclusive and must not both is set at the same time. Even in critical state, hardware should report the corresponding charging/discharging state. Bit2 – 1 indicates the battery is in the critical energy state Bit1 – 1 indicates the battery is charging. Bit0 – 1 indicates the battery is discharging.
0	R	-	Battery Device Present 0 – Not present 1 – Present

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Option Register 05-04h: Battery Full Charge Capacity

Returns an unsigned integer value(05h-04h high/low byte), with a range of to 65535, of the predicted pack capacity when it is fully charged. This value is expressed in either charge (mAh) or power (10mWh) depending on setting of [Power Unit] flag.

Name	R/W	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Full Charge Capacity	R	Unsigned integer	2	0	65535	-	mAh or 10 mWh

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Function and Device 01h: Battery Information DAT1

OPRn	R/W	Description
1-0h	R	Battery Design Capacity of Warning
3-2h	R	Battery Design Capacity of Low
5-4h	R	Battery Remaining Capacity
7-6h	R	Battery Voltage

Option Register 05-04h: Battery Remaining Capacity

Returns an unsigned integer value(05h-04h high/low byte), with a range of to 65535, of the predicted charge or energy remaining in the battery. This value is expressed in either charge (mAh) or power (10mWh) depending on setting of [Power Unit] flag.

Name	R/W	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Remaining Capacity	R	Unsigned integer	2	0	65535	-	mAh or 10 mWh

Option Register 07-06h: Battery Voltage

Returns an unsigned integer value(07h-06h high/low byte) of sum of the individual cell voltage measurements in mV with a range of 0 t0 20000 mV.

Name	R/W	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Voltage	R	Unsigned integer	2	0	20000	-	mV

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Logical Device : Customer's Function Define (0xC0)

Function and Device 00h: Backlight and Brightness Function Controller

OPRn	R/W	Description
00h	R	Brightness Configuration
01h	R	

Option Register 00h: Brightness Configuration

Bit	R/W	Default	Description
7	R/W		Backlight Enable
6-0	-	-	Reserve

Option Register 01h: Brightness Setting

Bit	R/W	Default	Description
7-4	-	-	Reserve
3-0	R		Current Brightness Level. (It is on ly support step 8 – 0 in the project.

Function and Device 01h: Brightness Curves Level Setting.

OPRn	R/W	Description
08-00h	R/W	Brightness Level Value 8–0. (The high level value must be higher than the low level.)

Logical Device: Auto Dimming Function Controller (0xC1)

Function and Device 00h: Auto Dimming Configuration

OPRn	R/W	Description
00h	R/W	Auto Dimming Function Configuration Register
03-01h	-	Reserved
05-04h	R	ADC Channel Data0 Register
07-06h	R	ADC Channel Data1 Register

Option Register 00h: Auto Dimming Function Configuration Register

Bit	R/W	Default	Description
7	R/W	1b	Auto Dimming Function Enable 1: Enable 0: Disable
6-0	-	-	Reserve

Option Register 01h:

Bit	R/W	Default	Description
7-0			Auto Dimming Mode. Display current working mode.

//=====================================

Option Register 00h: Mode 1 Dark room

Data 0 : Lower Limit of reference Lumen. 0x30

Data 1 : Upper Limit of reference Lumen. 0x75

//=====================================

Option Register 00h: Mode 2 Indoor

Data 0 : Lower Limit of reference Lumen

Data 1 : Upper Limit of reference Lumen

//=====================================

Option Register 00h: Mode 3 Outdoor

Data 0 : Lower Limit of reference Lumen

Data 1 : Upper Limit of reference Lumen

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Option Register 02h:

Bit	R/W	Default	Description
7-0			

Option Register 03h:

Bit	R/W	Default	Description
7-0			

Option Register 05-04h: ADC Channel 0 Data Registers

Bit	R/W	Default	Description
15-8	R	-	ADC channel 0 upper byte
7-0	R	-	ADC channel 0 lower byte

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Option Register 07-06h: ADC Channel 1 Data Registers

Bit	R/W	Default	Description
15-8	R	-	ADC channel 1 upper byte
7-0	R	-	ADC channel 1 lower byte

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Logical Device : Auto Rotation Function Controller (0xC2)

Function and Device 00h: Auto Rotation Function Controller

OPRn	R/W	Description
00h	R	
01h	R	

Option Register 01h: Auto Dimming Function Configuration

Bit	R/W	Default	Description
7	R/W	10b	Auto Rotation Function Setting 0b: Function Disable 1b: Auto (Tilt Sensor Enable)
6-0	-	-	Reserve

Function and Device 01h: Tilt Sensor Monitor.

OPRn	R/W	Description
01-00h	R	Read return Tilt Sensor X threshold.
03-02h	R	Read return Tilt Sensor Y threshold.
05-04h	R	Read return Tilt Sensor Z threshold.

Logical Device : User Mode Select (0xC6)

Function and Device 00h: User Mode Controller

OPRn	R/W	Description
00h	R	User Mode Configuration.
01h	R	

Option Register 00h: User Mode Configuration.

Bit	R/W	Default	Description
7-1	R/W	-	Reserve
0	-	-	0: Protable 1:Mounted