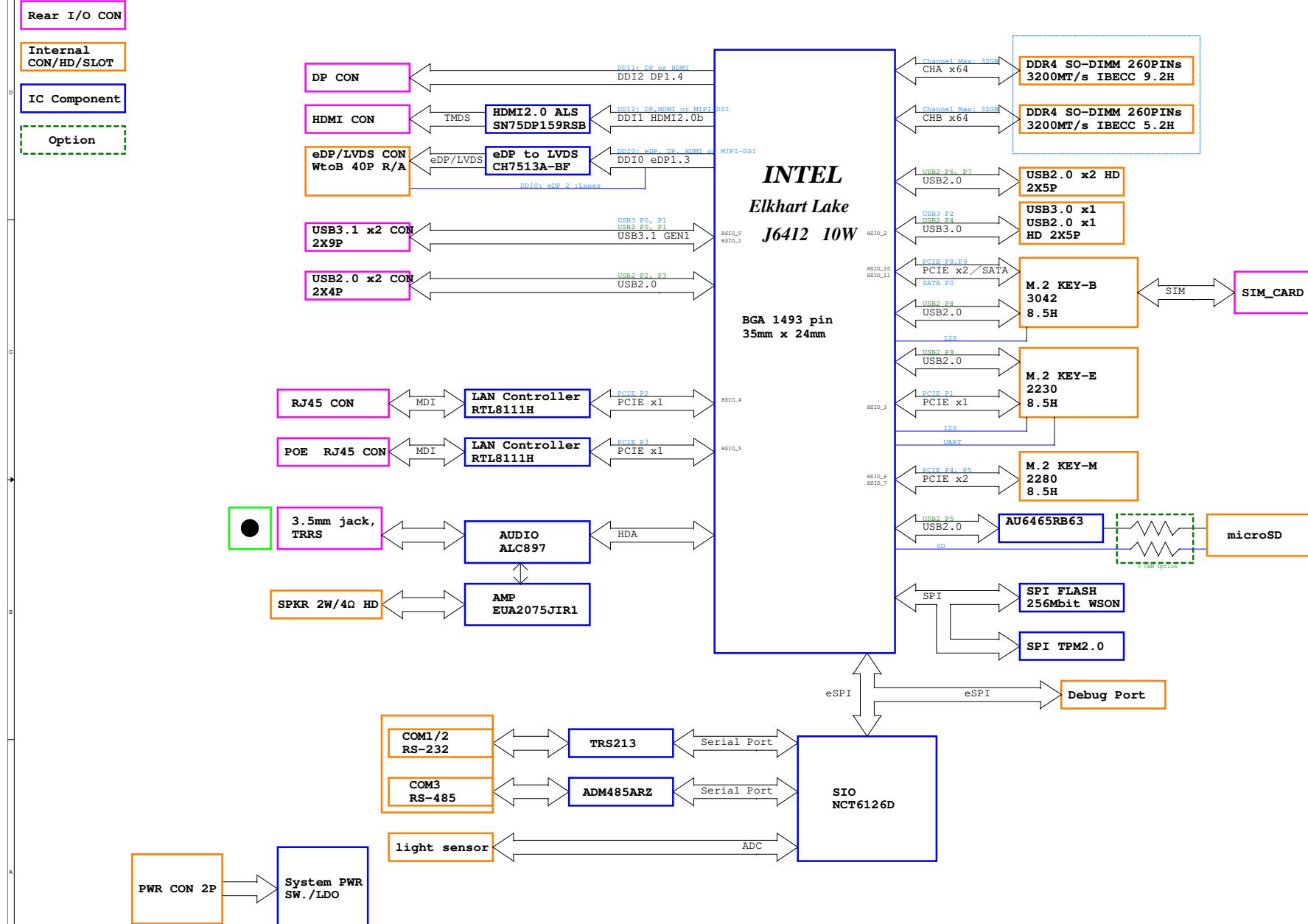


COVER PAGE**Model Name: FAY-EHL R1.00**

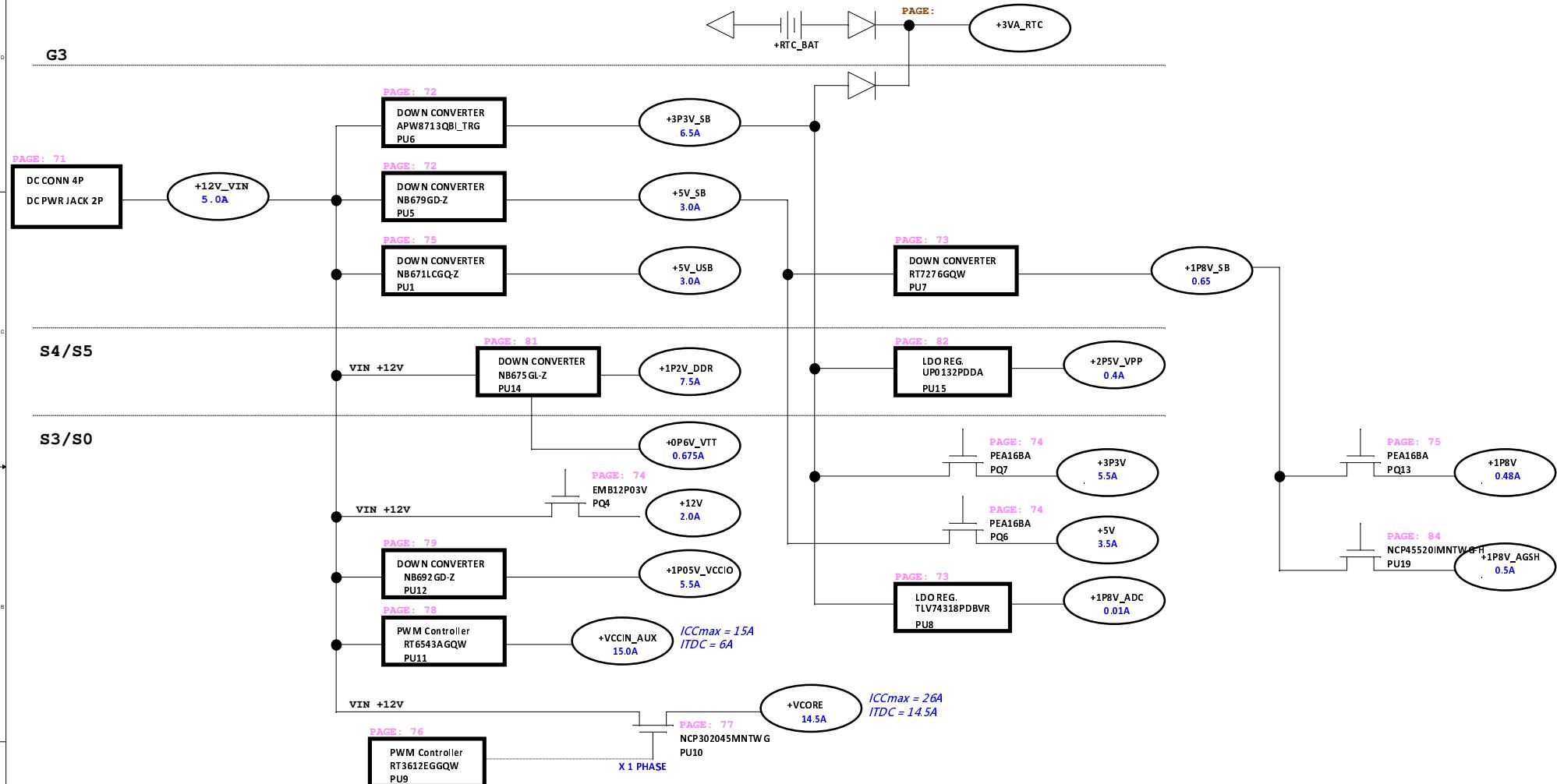
01	COVER PAGE
02	BLOCK DIAGRAM
03	POWER FLOW
04	POWER SEQUENCE
05	XXX
06	CLOCK DISTRIBUTION
07	SMBUS MAP
08	CPU DDR4 CH0
09	CPU DDR4 CH1
10	CPU DDI
11	CPU JTAG BPM
12	CPU ESPI/FSPI
13	CPU SPI
14	CPU PSE GBE RGMII
15	CPU HDA/I2S/SD_SDIO
16	CPU HSIO USB2.0
17	CPU CLK RTC
18	CPU EMMC
19	CPU MISC
20	CPU VCORE/VDDQ/VCCIO
21	CPU VCORE_AUX/1P8V/3P3V
22	CPU VSS
23	CPU CFG/RSVD
24	XXX
25	CPU CAPS
26	DDR4 SODIMM CH0 9.2H
27	DDR4 SODIMM CH0 PWR
28	DDR4 SODIMM CH1 5.2H
29	DDR4 SODIMM CH1 PWR
30	DDIO eDP to LVDS CH7513B-BF
31	DDIO eDP/LVDS CON
32	DDI2 DisplayPort
33	XXX
34	DDI1 HDMI ALS SN75DP158
35	DDI1 HDMI CON
36	XXX
37	M.2 E KEY
38	M.2 KEY-M 2280
39	M.2 KEY-B 3042/3052
40	SIM CARD
41	USB2.0 REAR CON
42	USB2.0 FRONT HD
43	USB3.1 GEN1 REAR CON
44	XXX
45	LAN1 RTL8111H
46	LAN1 RJ45 CON
47	LAN2 RTL8111H
48	LAN2 RJ45 CON
49	XXX
50	Card reader

51	AUDIO CODEC ALC897
52	AUDIO PHONE JACK
53	AUDIO AMP. EUA2075JIR1
54	XXX
55	RTC
56	SIO NCT6126D
57	SIO PIN STRAP
58	HW MONITOR RGB LED
59	XXX
60	CAN RS232/485
61	COM port
62	SPI FLASH
63	DEBUG PORT
64	FRONT PANEL AT/ATX MODE
65	XXX
66	SEQ RSMRST#/DPWROK/PLTRST#
67	SEQ PWRGD
68	SEQ PLTRST
69	XXX
70	STATUS LED
71	PWR +12V_DCIN
72	PWR +5V_SB/+3P3V_SB
73	PWR +1P8V_SB/+1P8V_ADC
74	PWR +12V/+5V/+3P3V
75	PWR +1P8V/+5V_USB
76	PWR +VCORE CONTROLLER
77	PWR +VCORE
78	PWR +VCCIN_AUX
79	PWR +1P05V_VCCIO
80	PWR
81	PWR +1P2V_DDR +0P6V_VTT
82	PWR +2P5V_VPP
83	PWR +VCCST
84	PWR +VCCSFR_OC/+VCCAGSH
85	PWR DISCHARGE
86	XXX
87	XXX
88	XXX
89	PCB&SCREW HOLE&LOGO
90	REVISION HISTORY

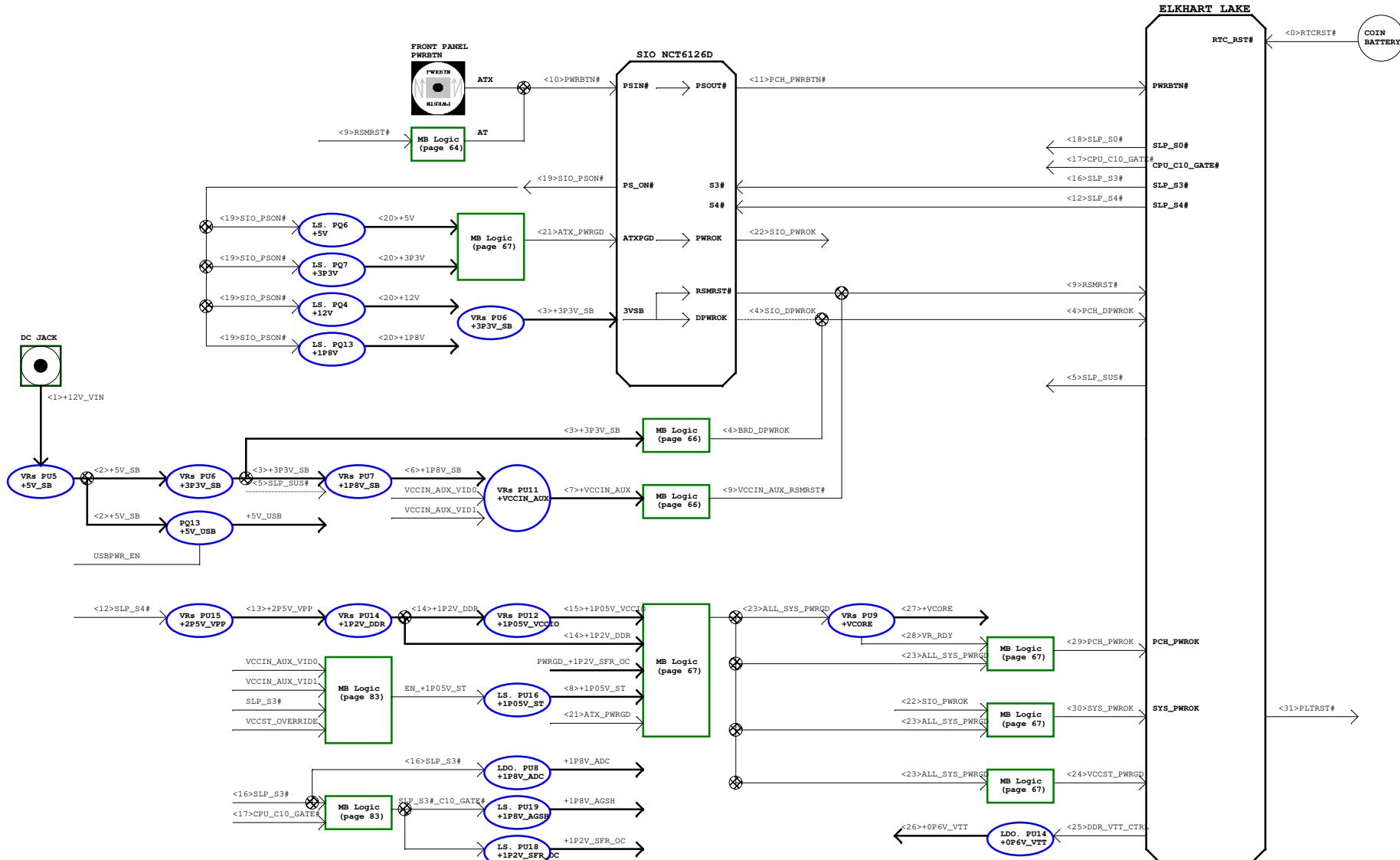
BLOCK DIAGRAM



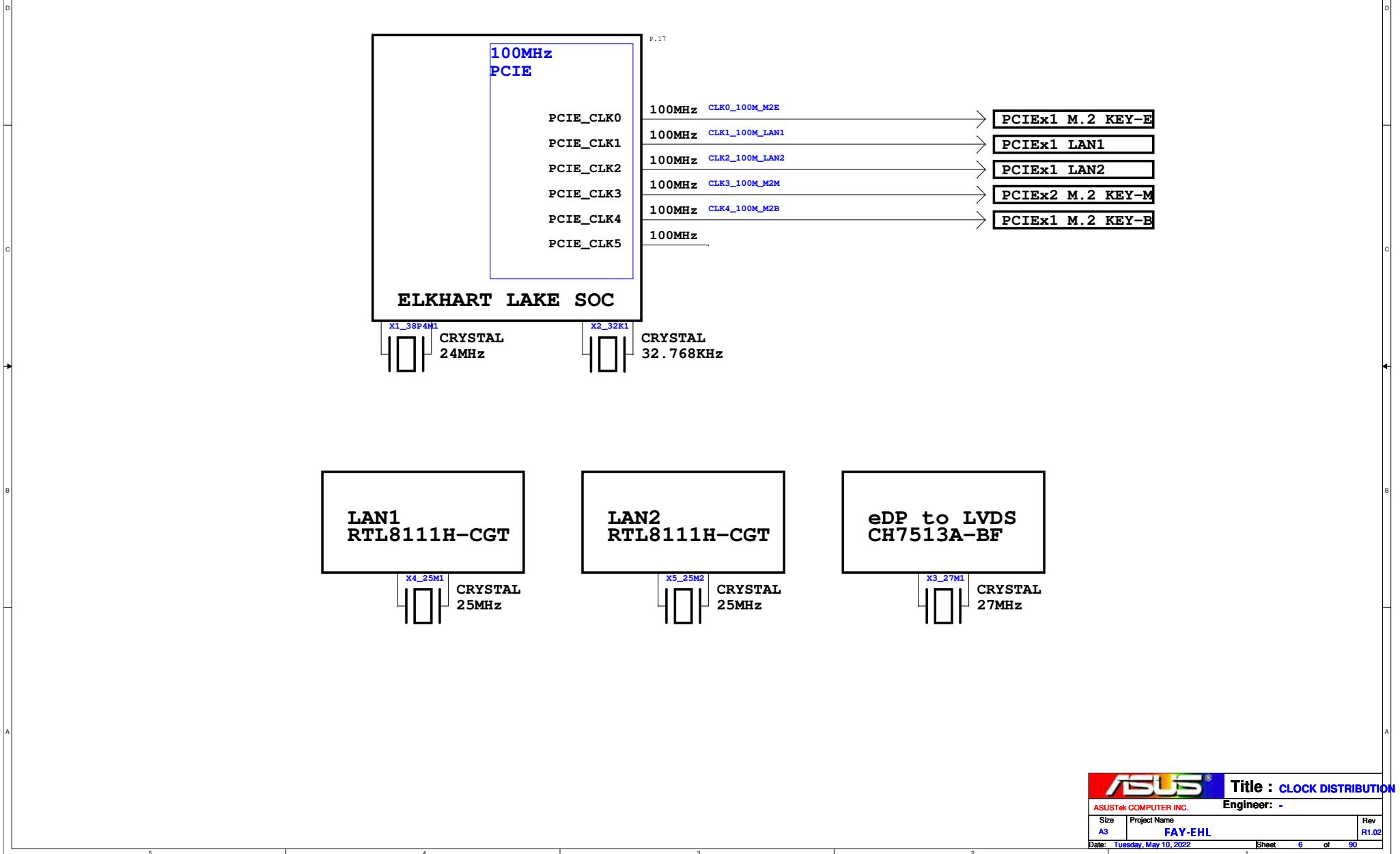
POWER FLOW



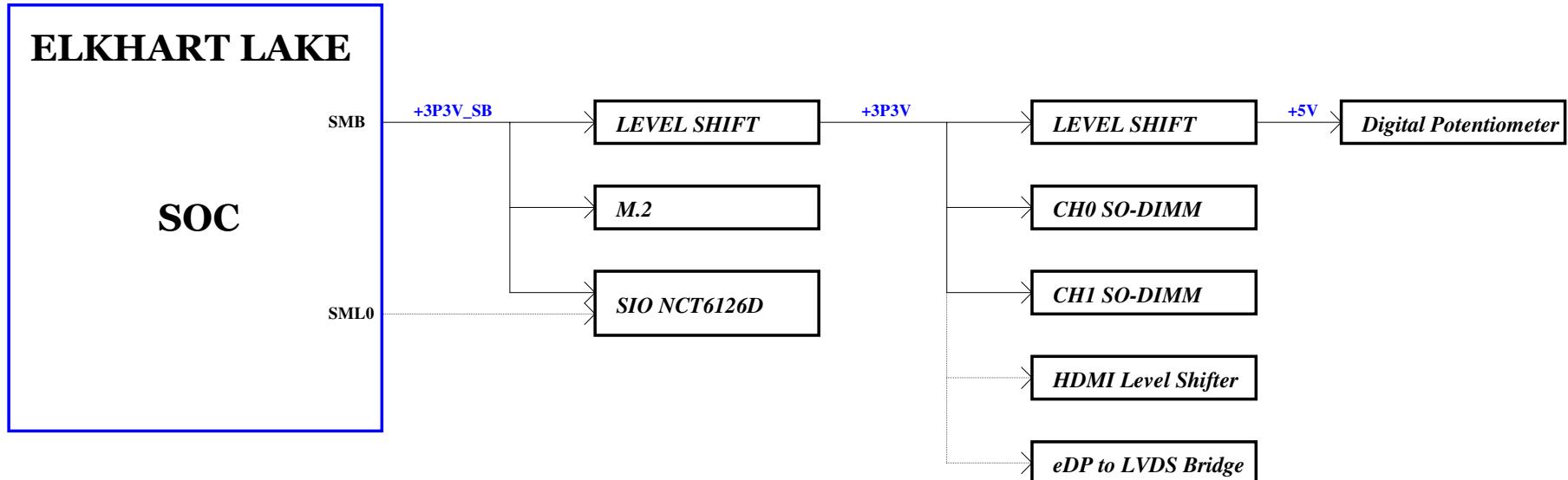
POWER SEQUENCE

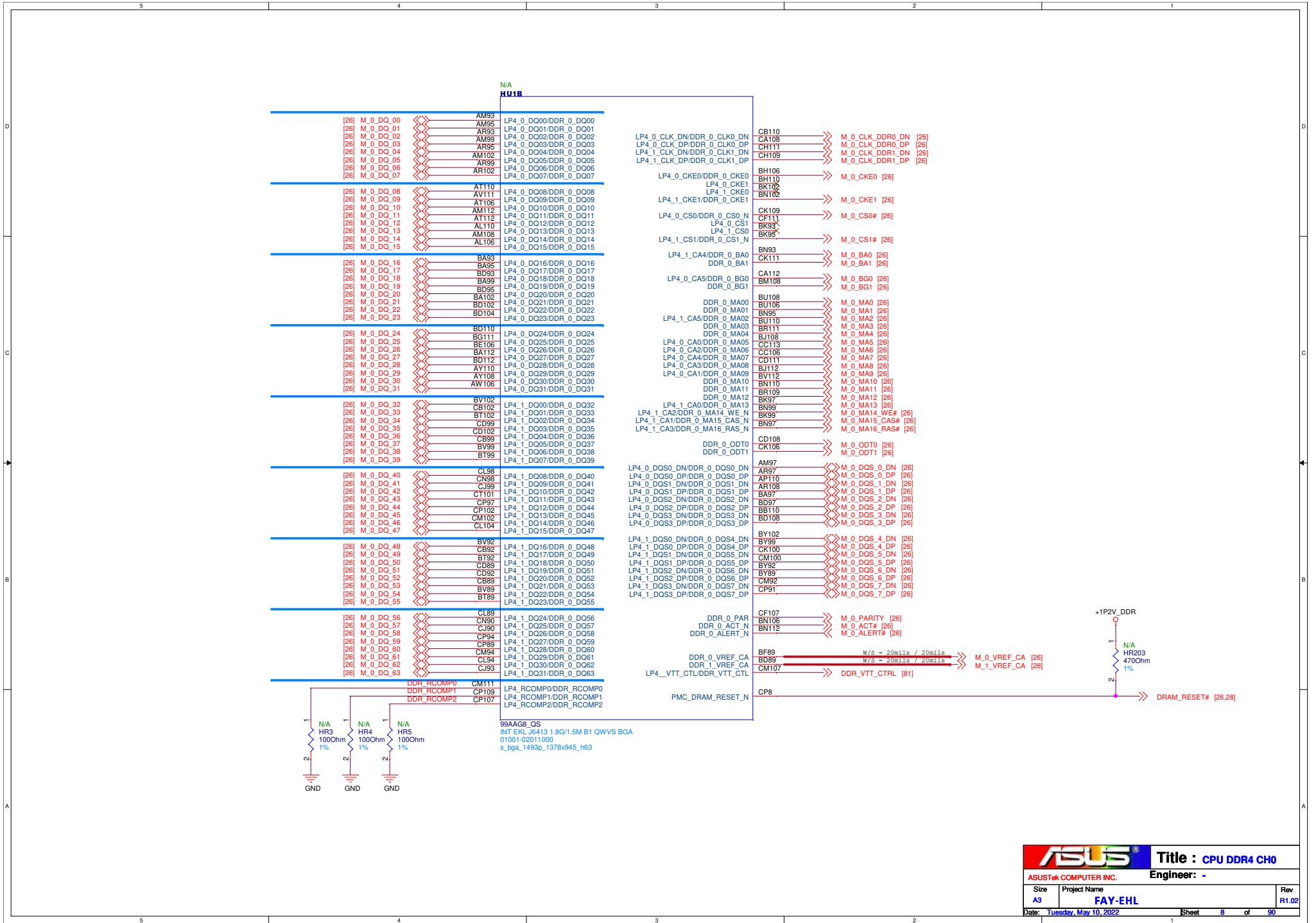


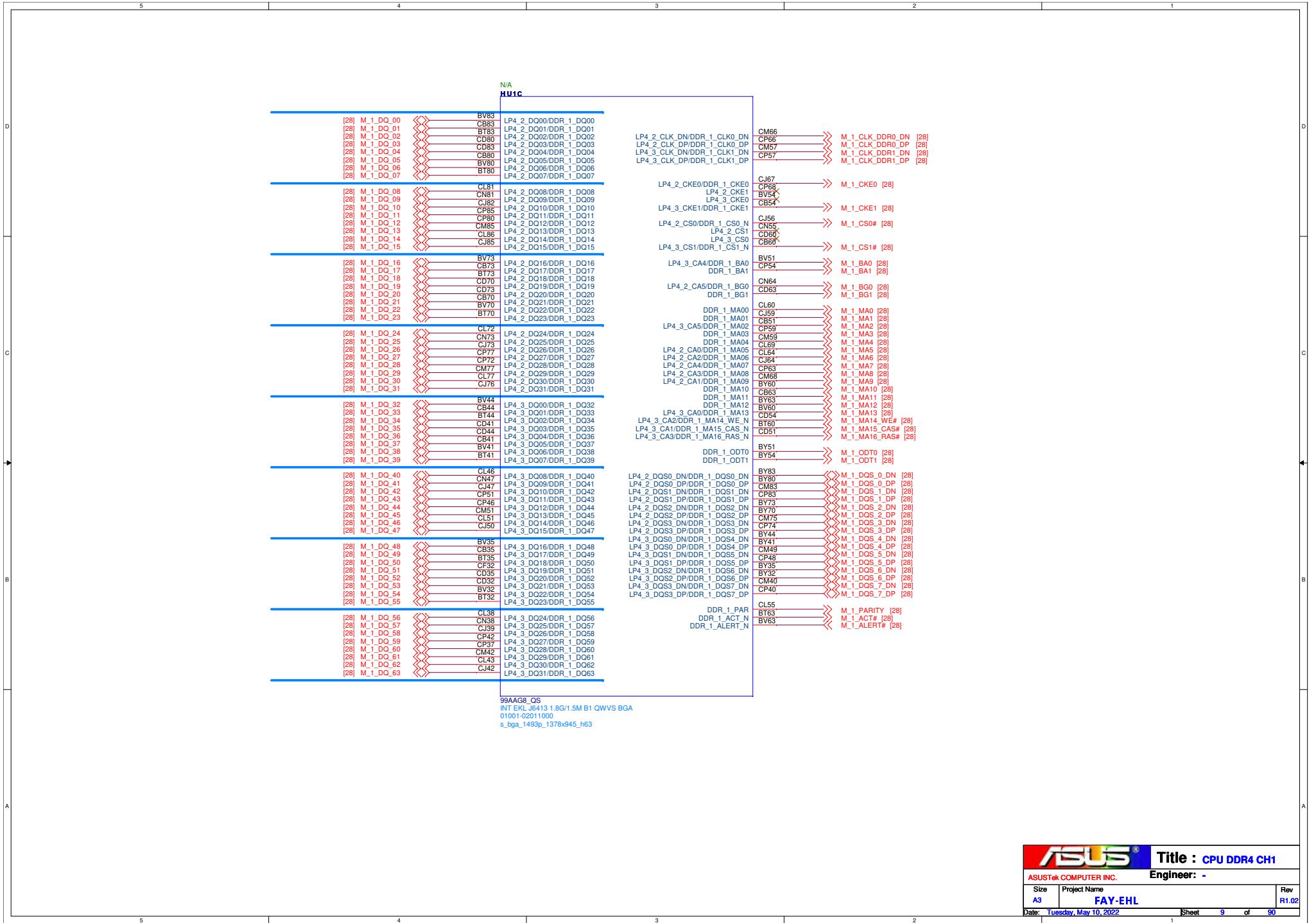
CLOCK DISTRIBUTION

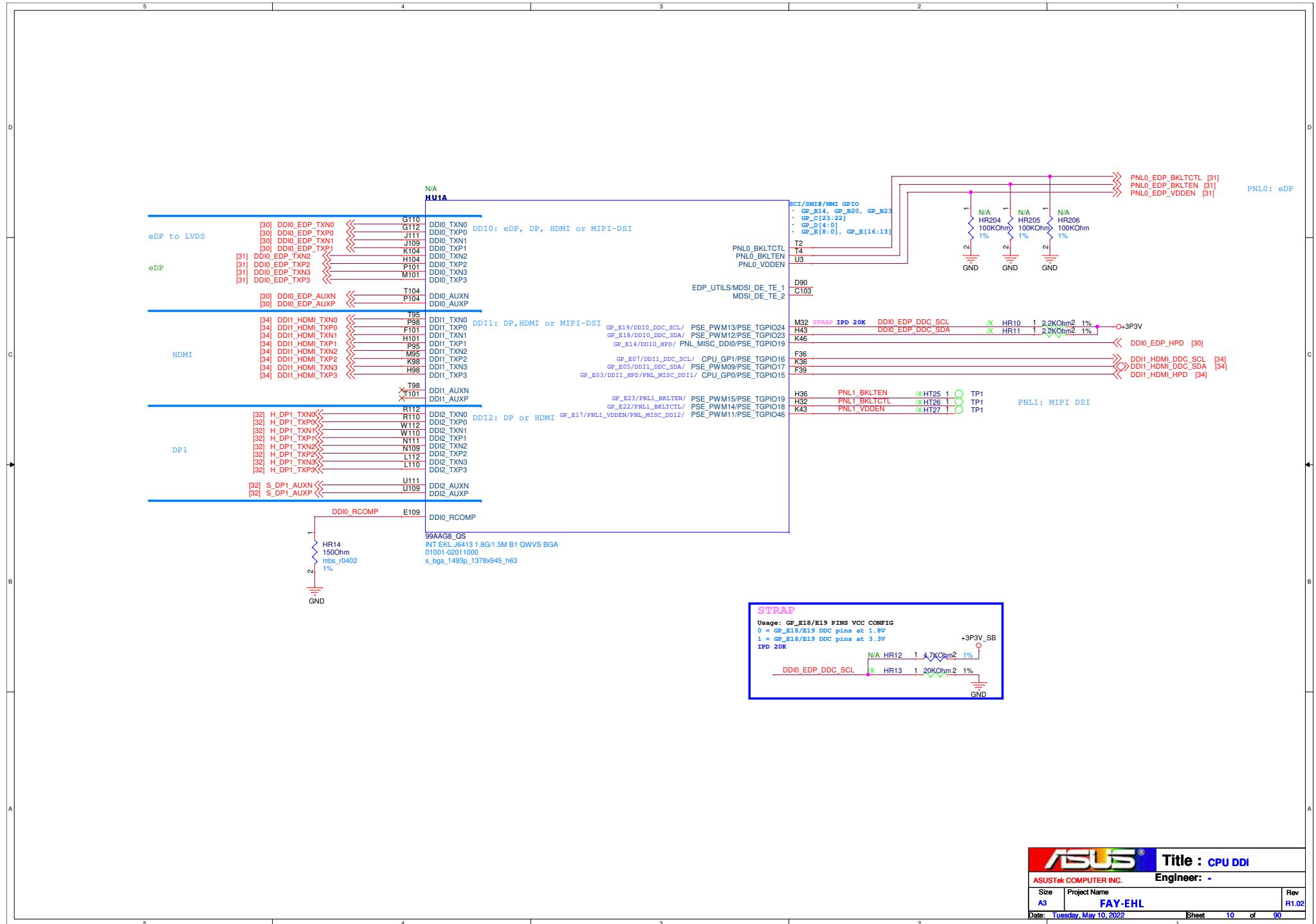


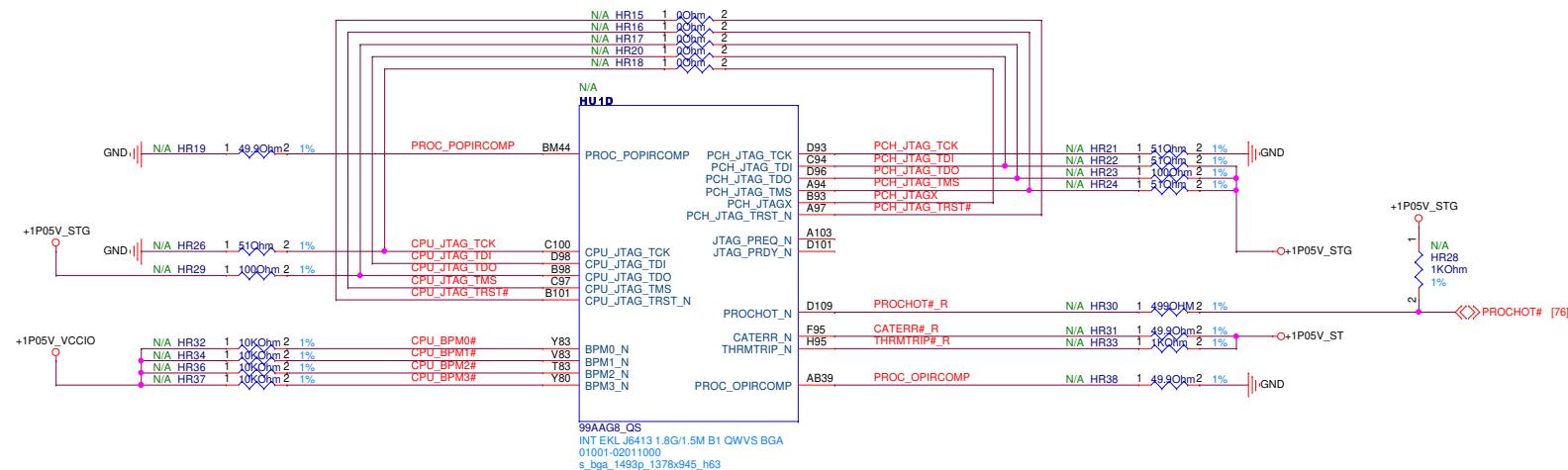
SMBUS MAP

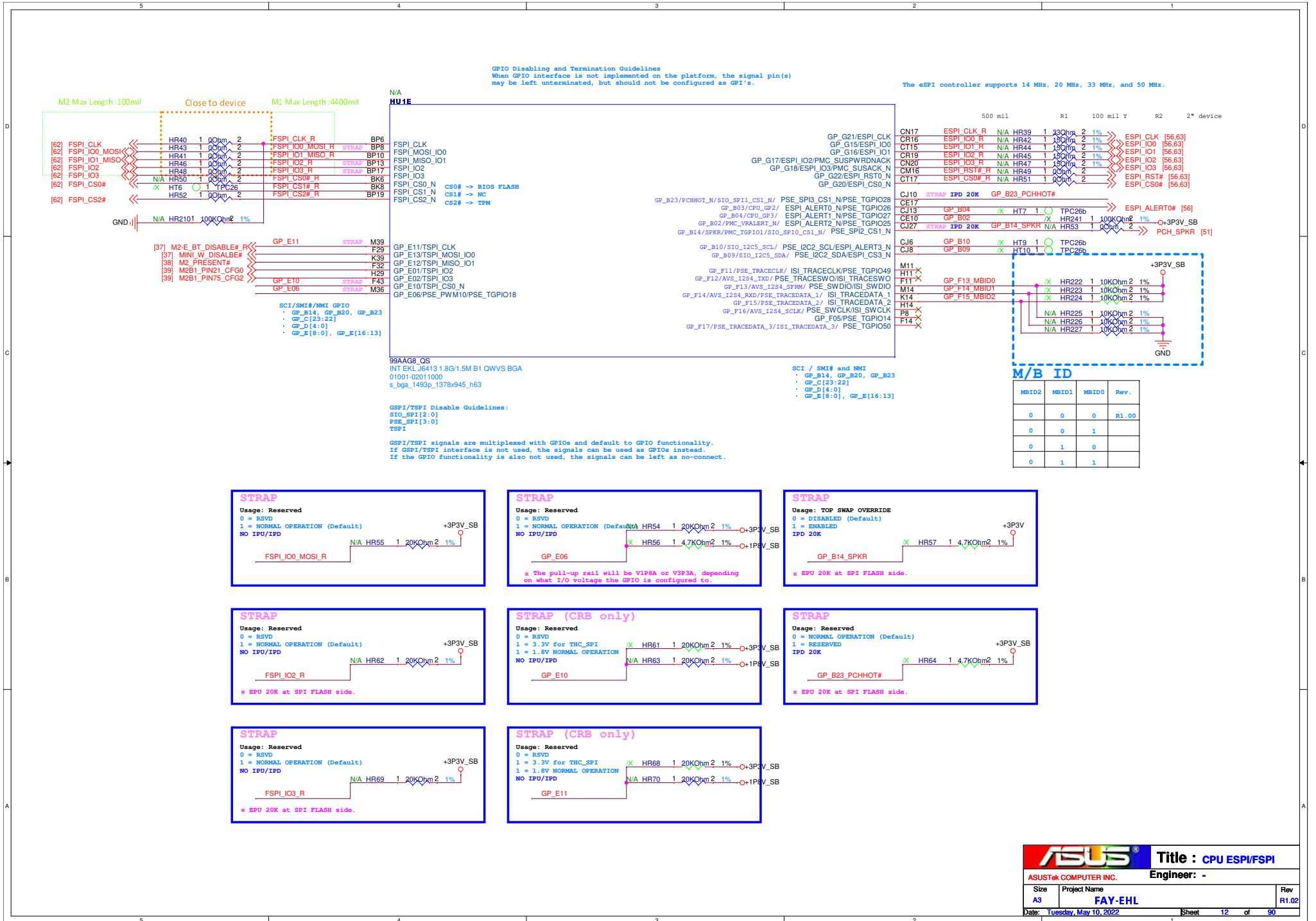


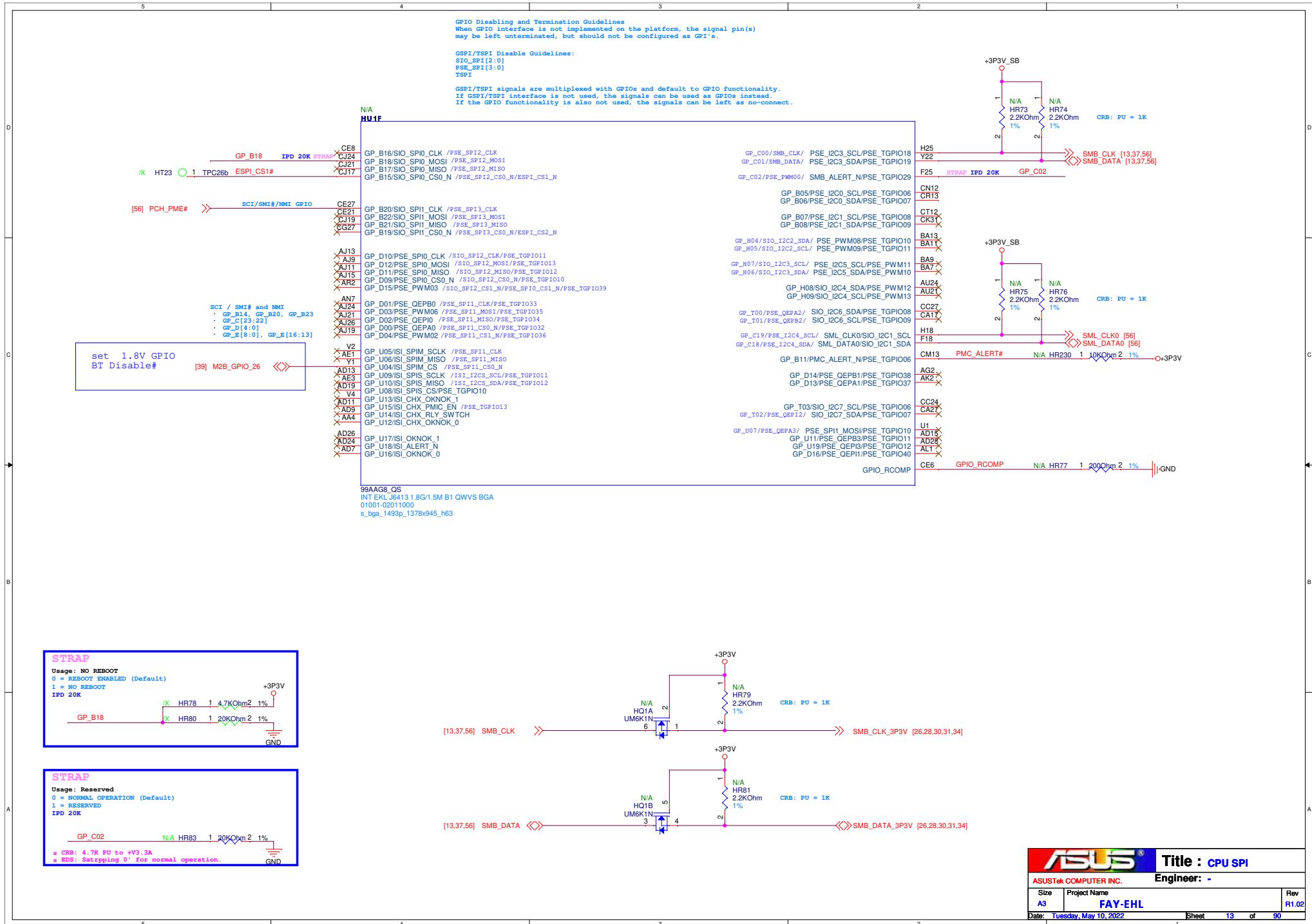


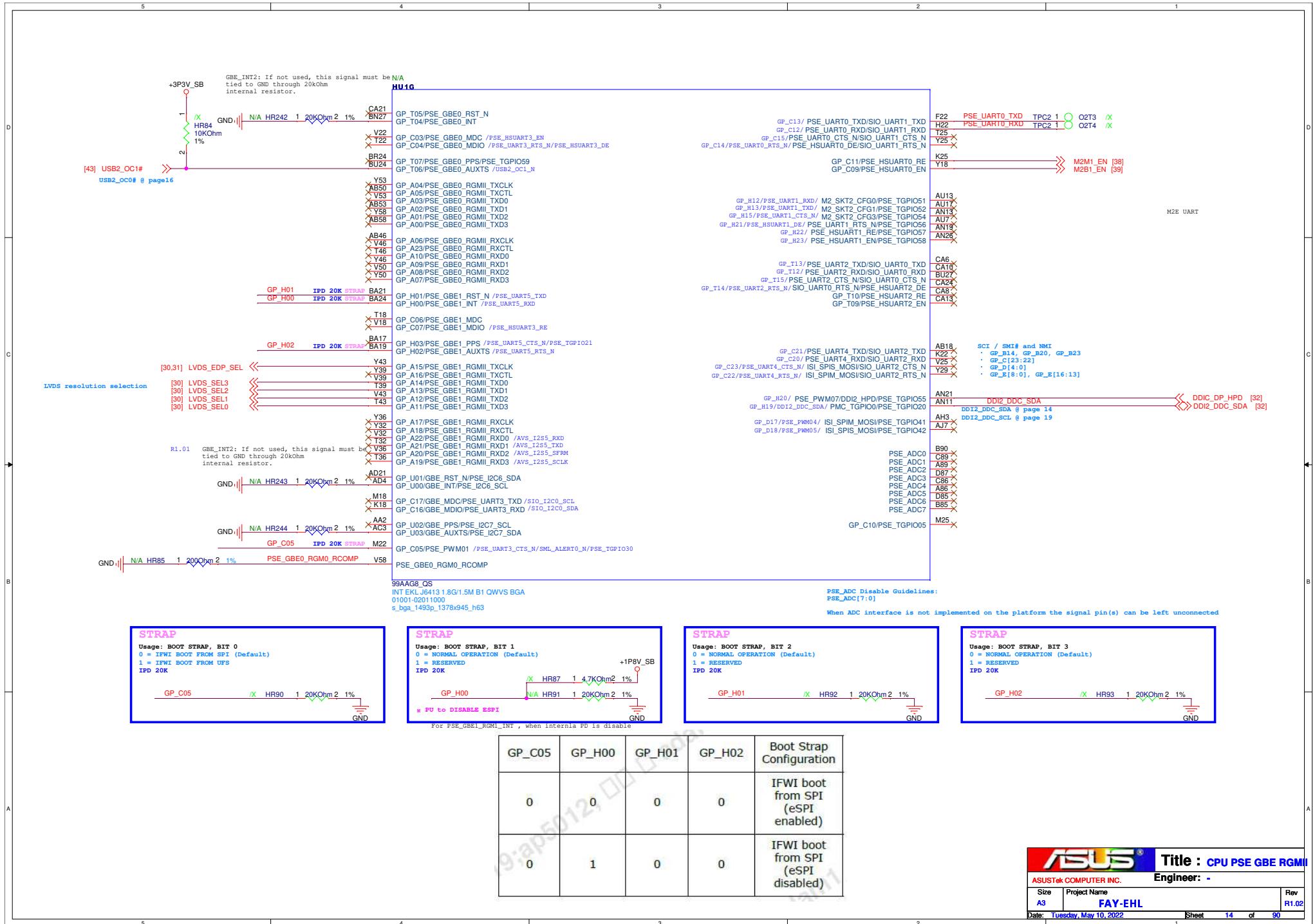


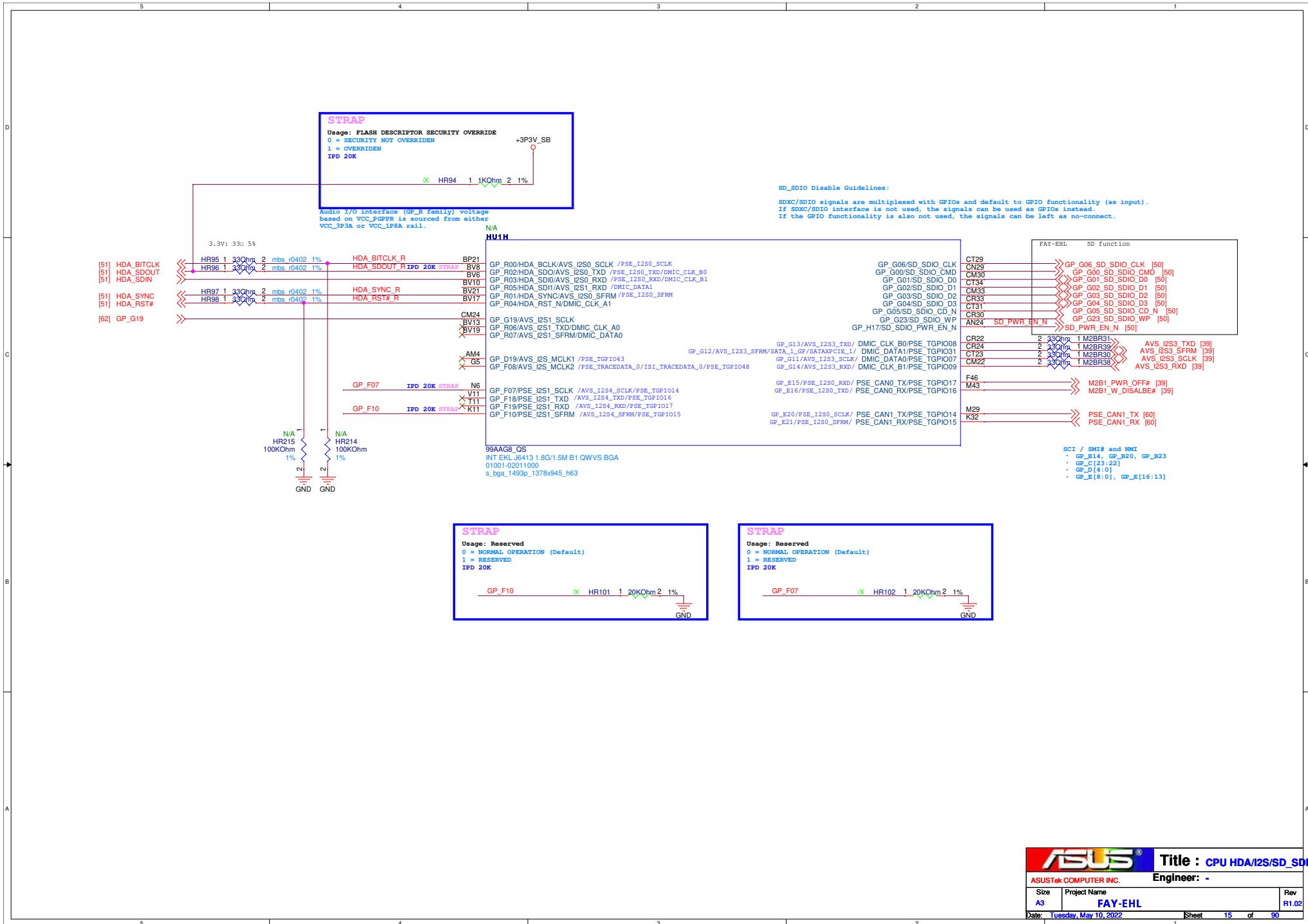


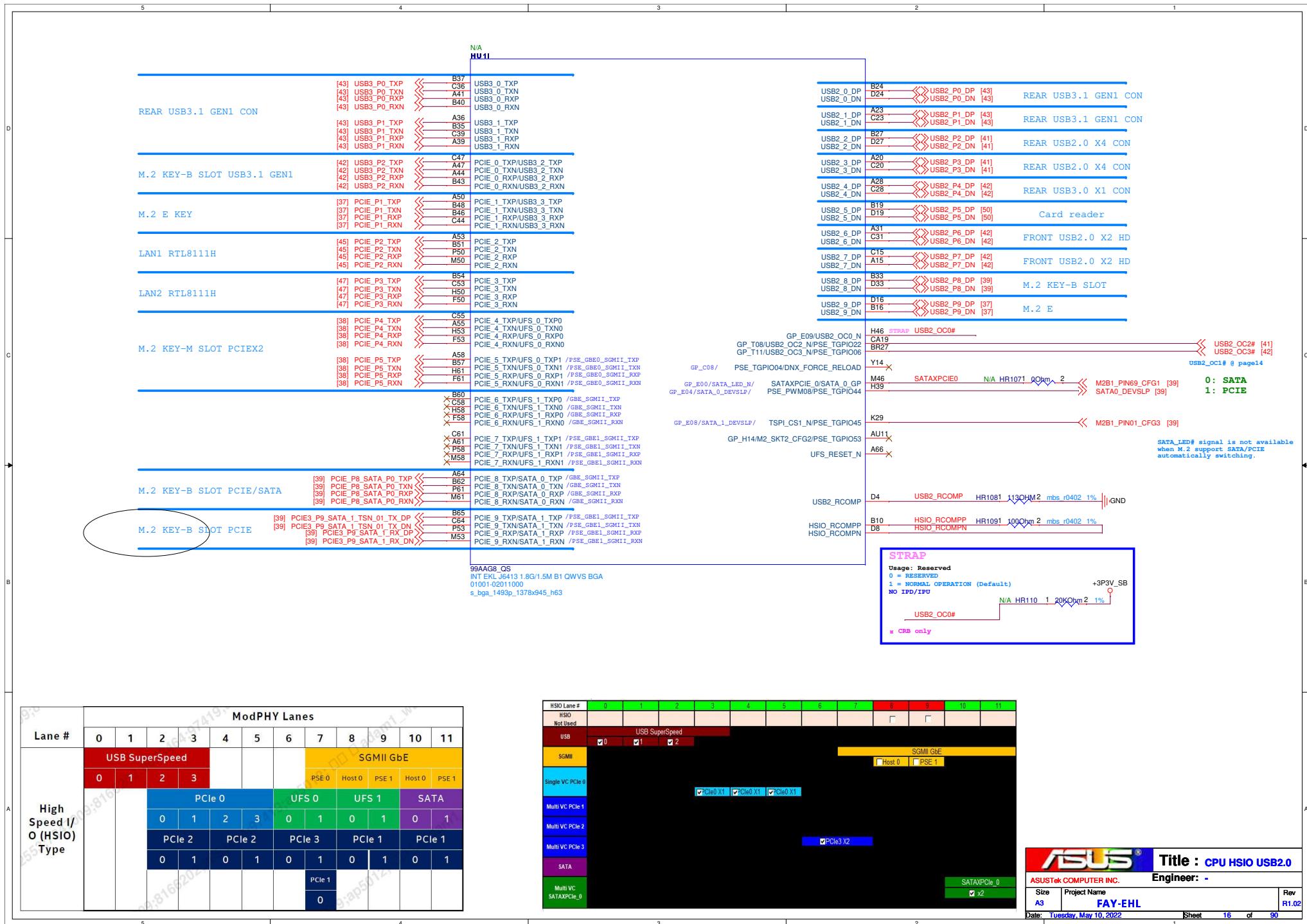


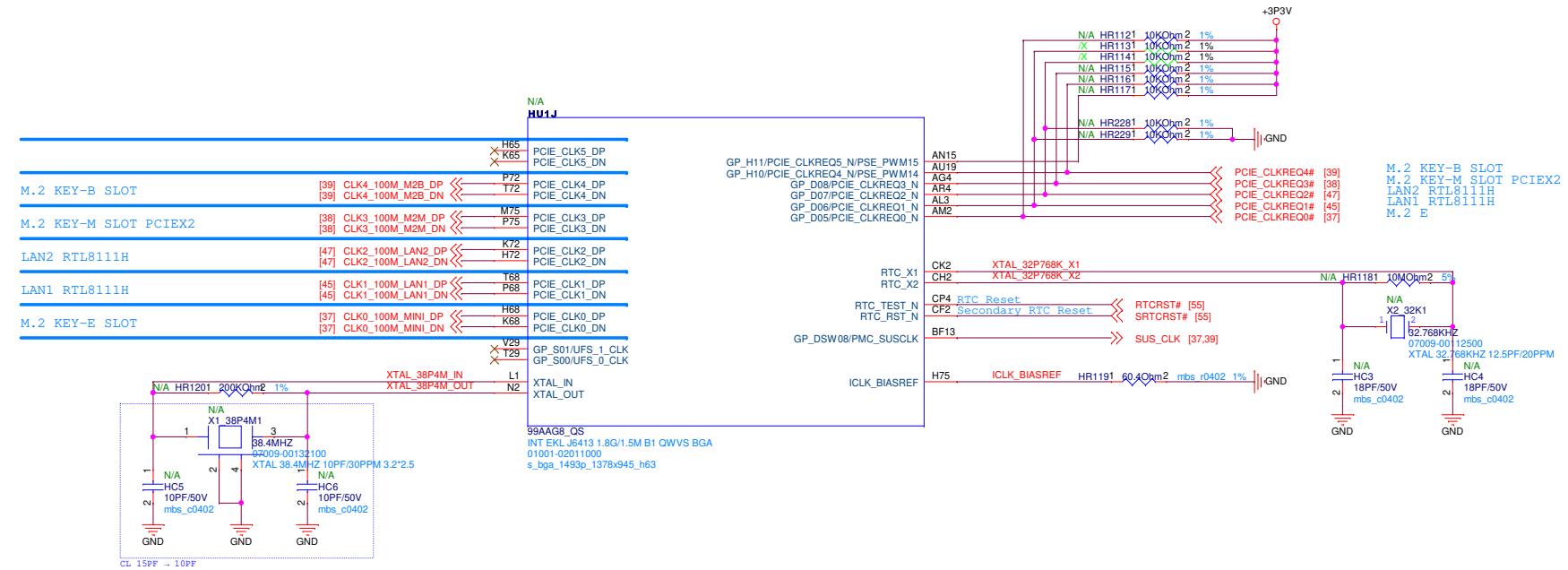


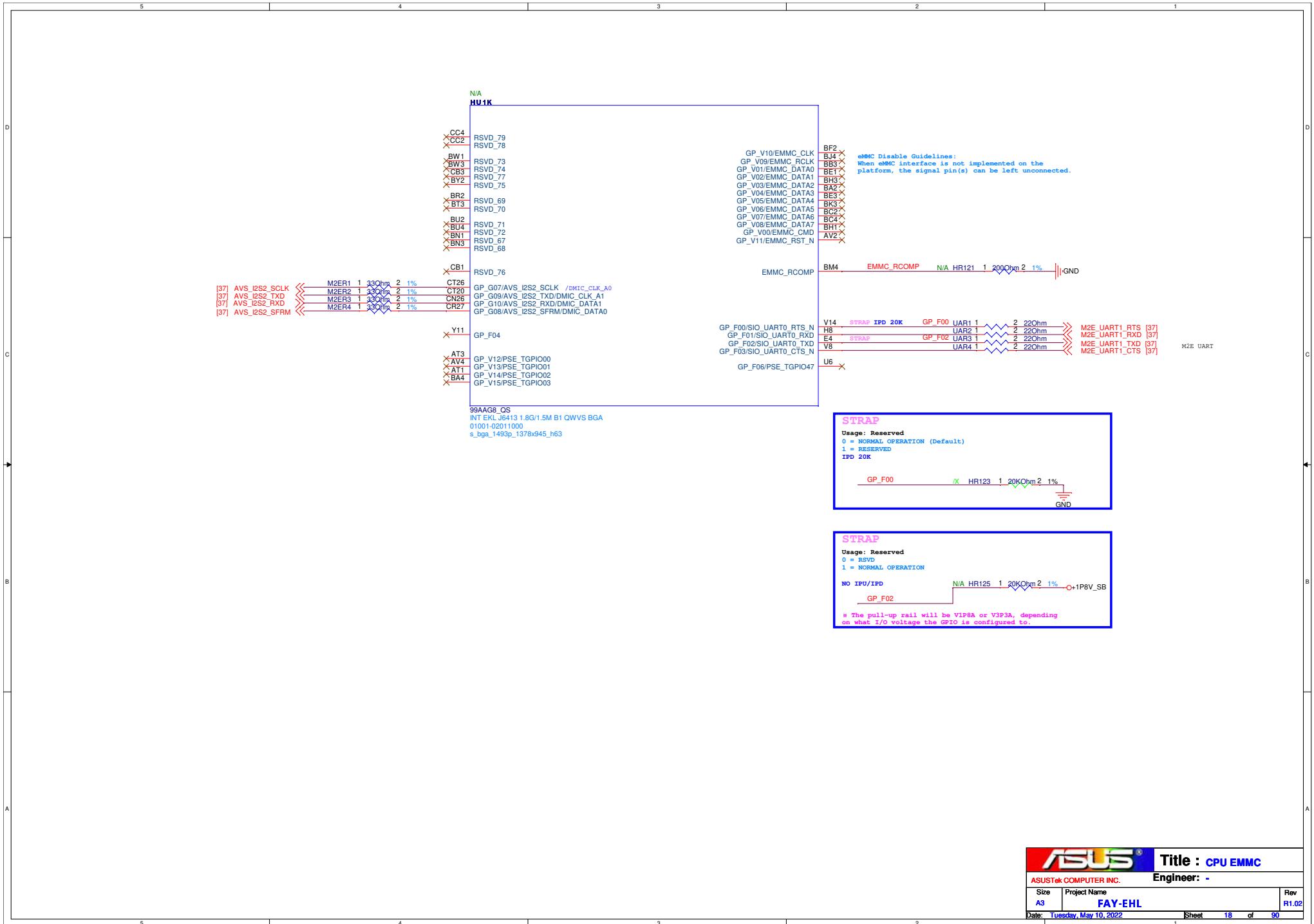


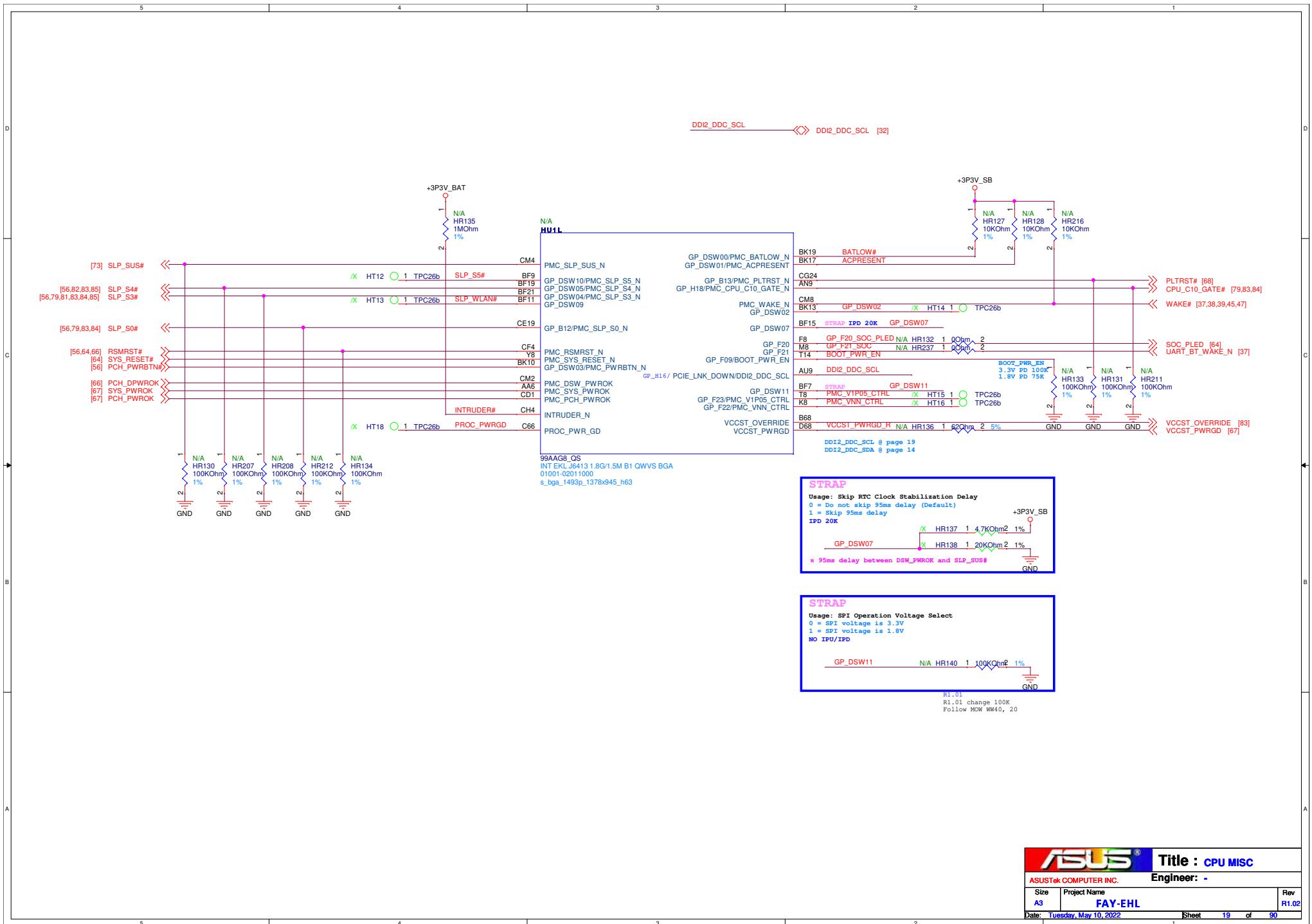


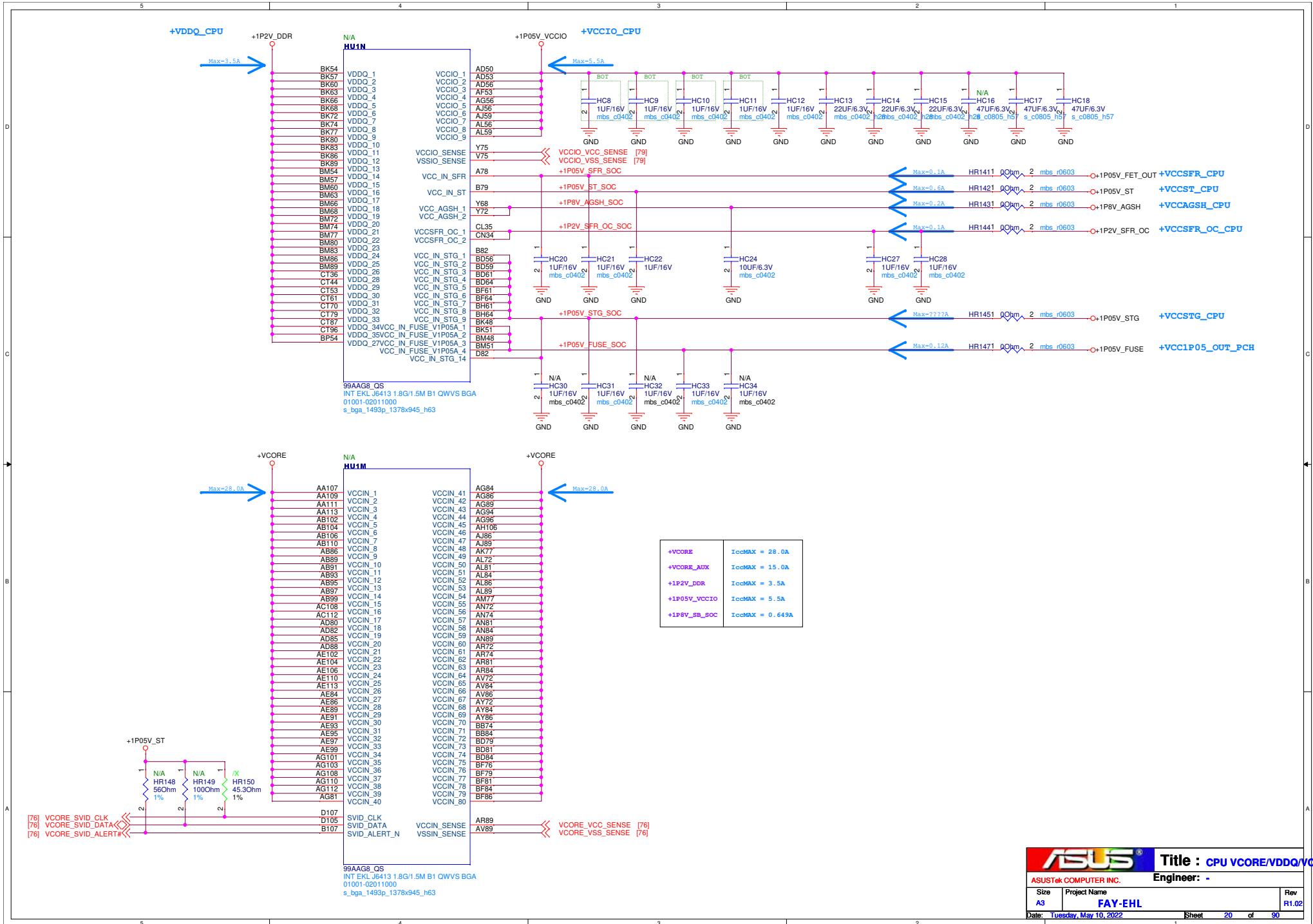


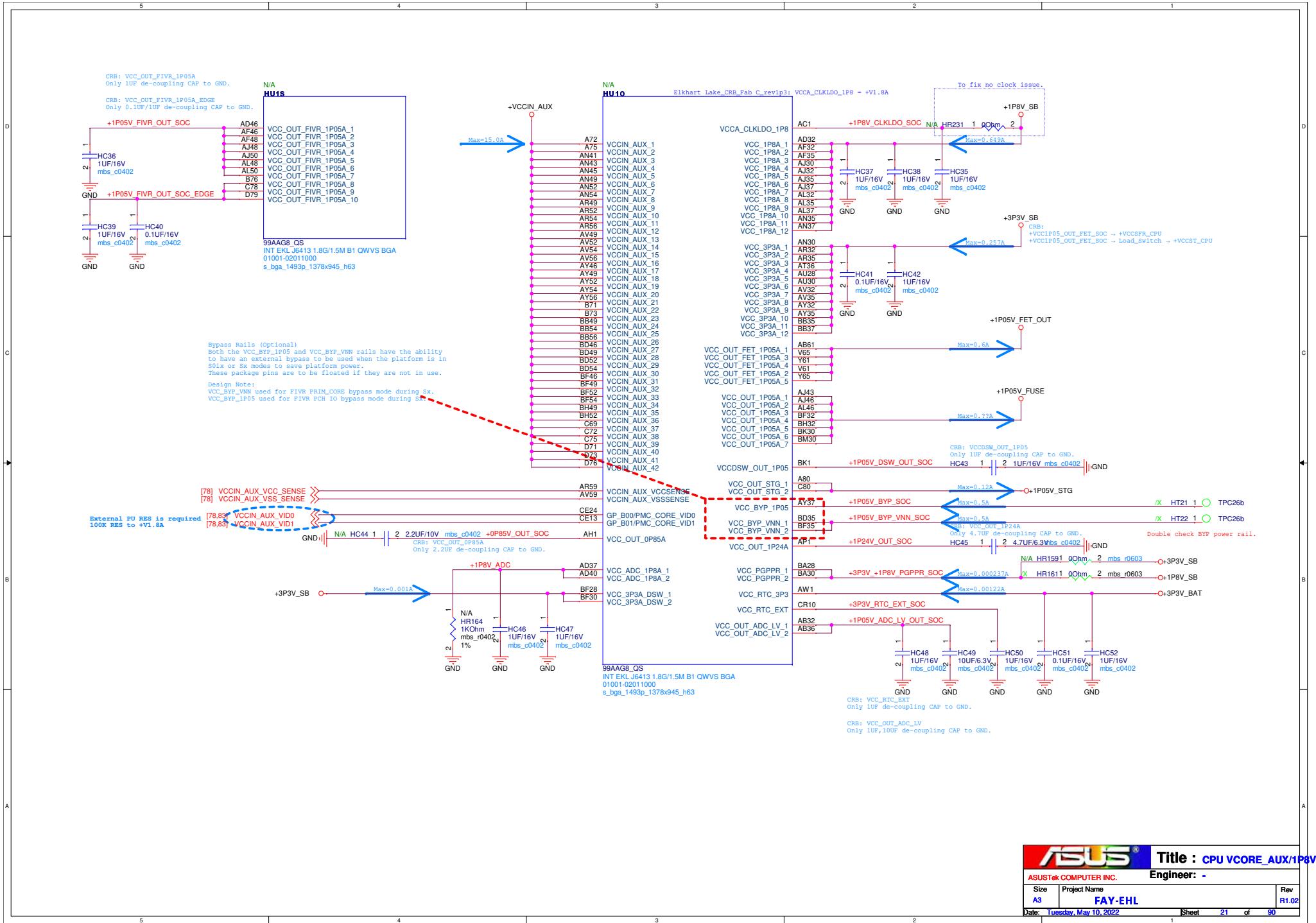


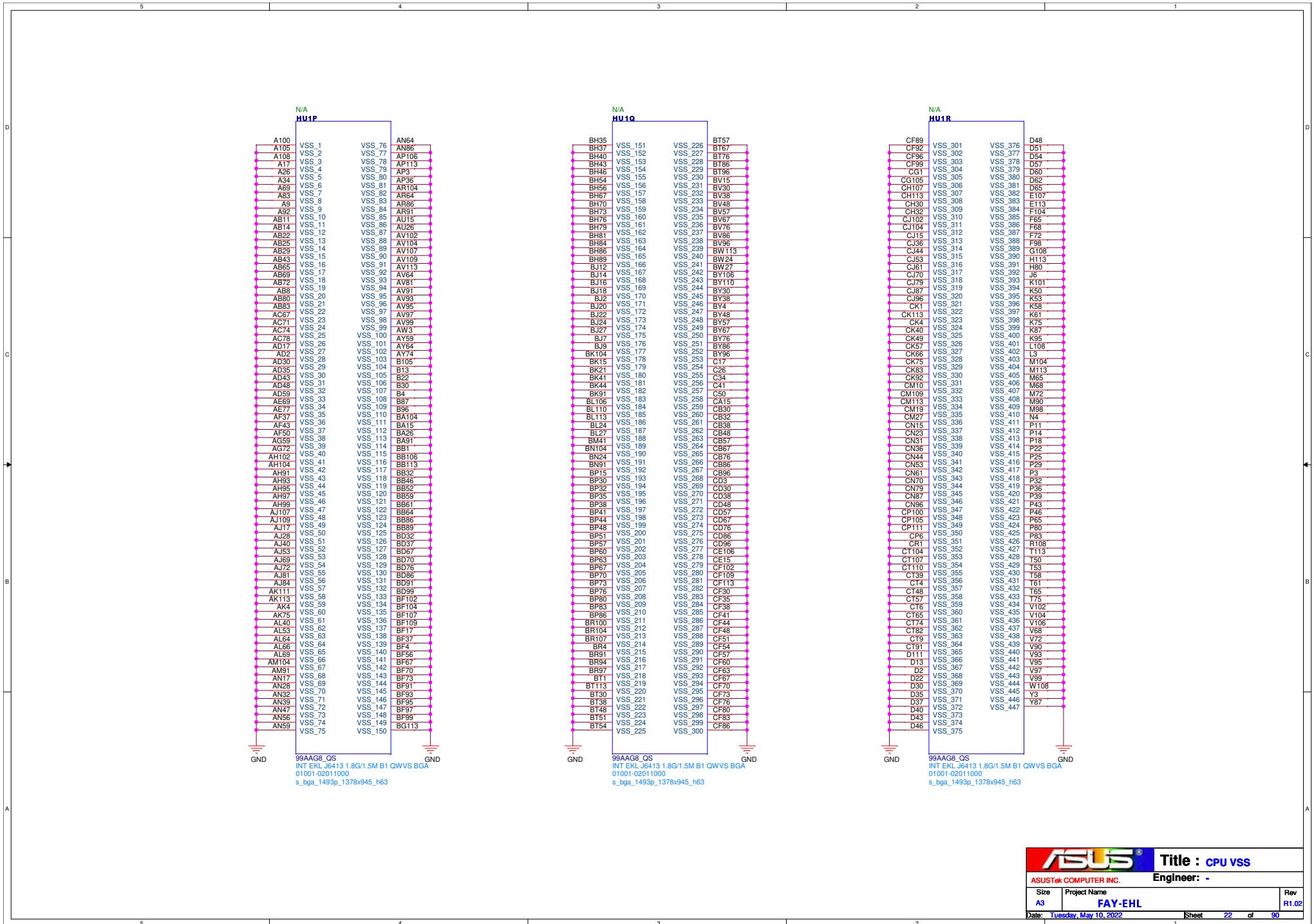


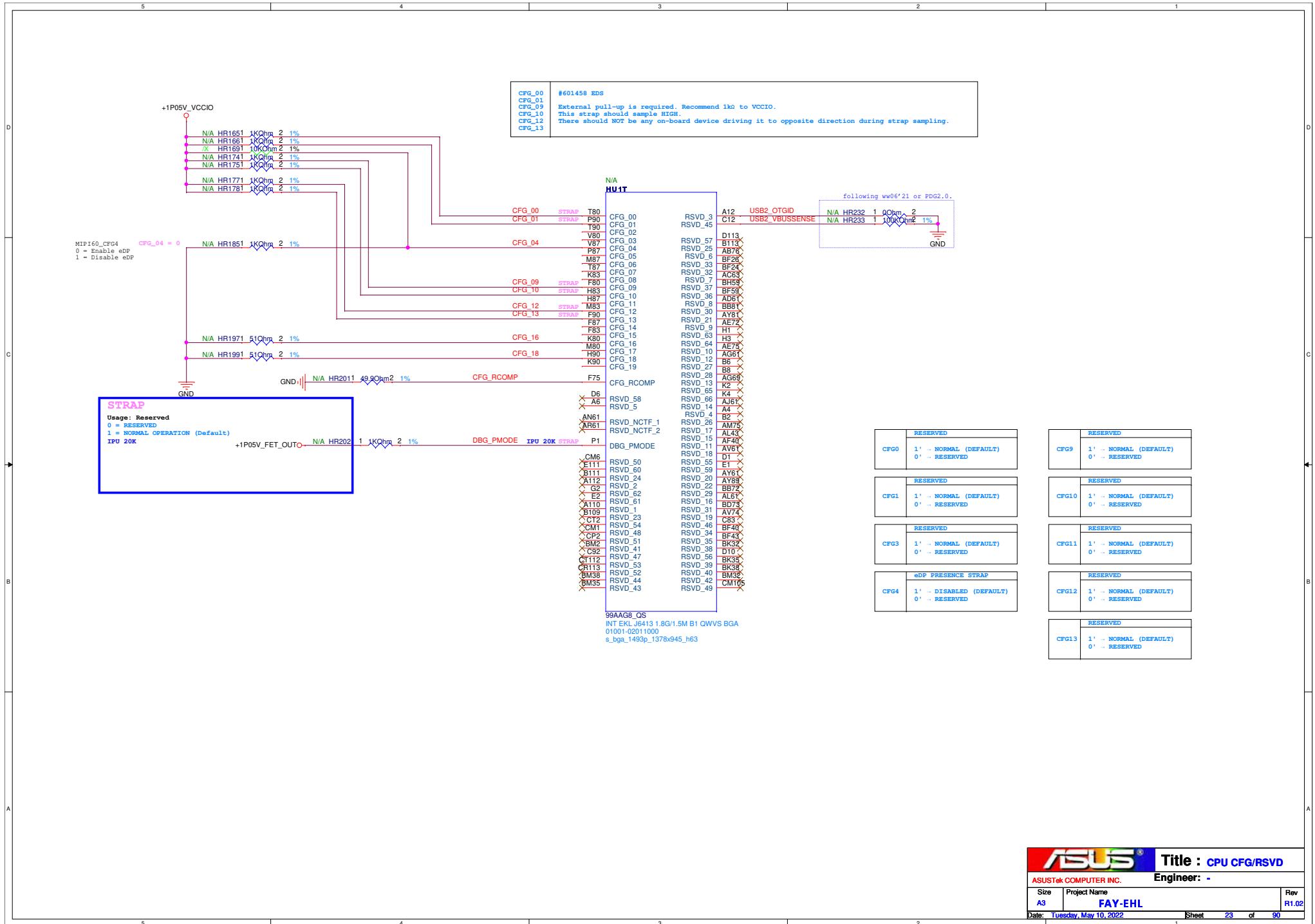


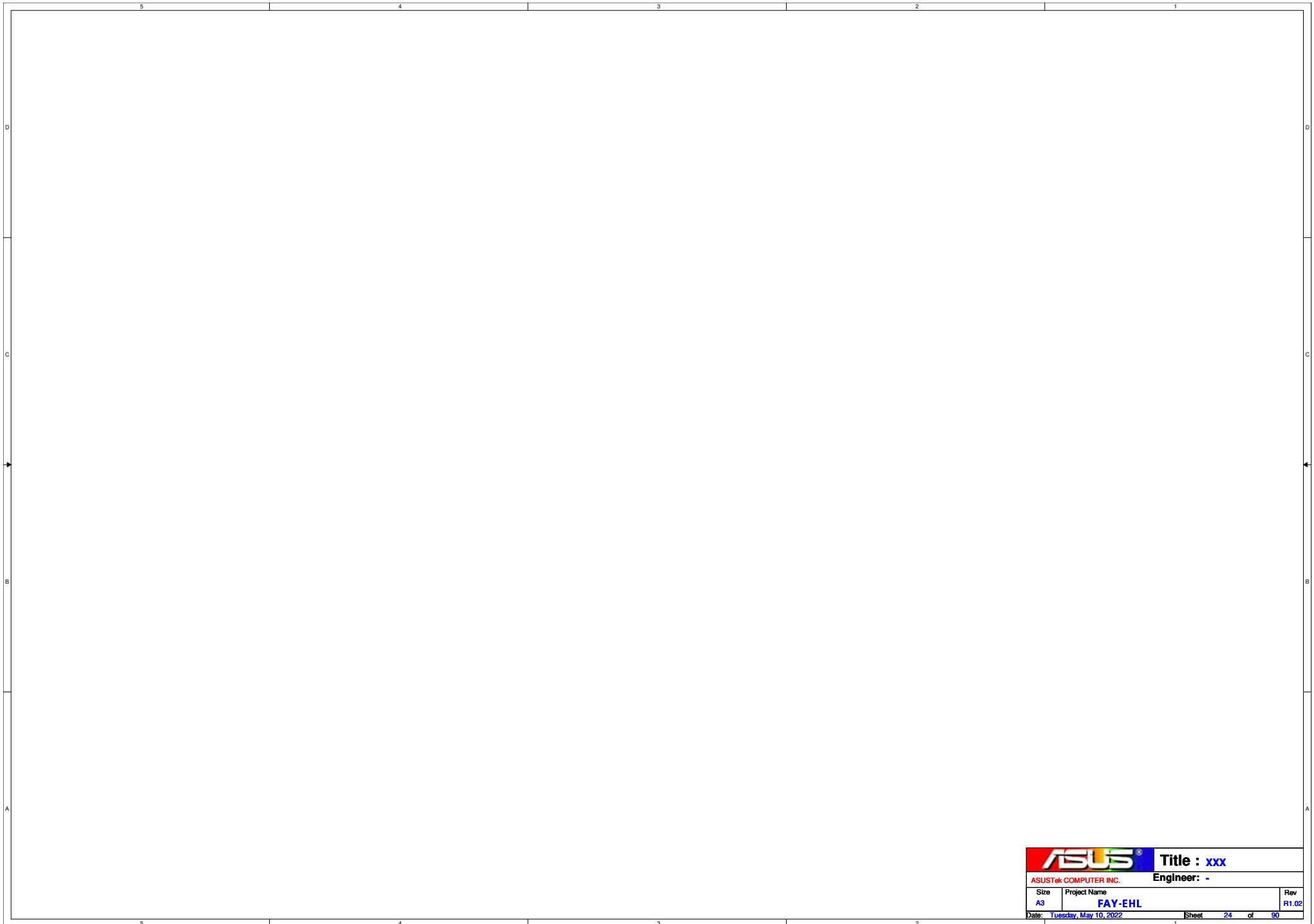


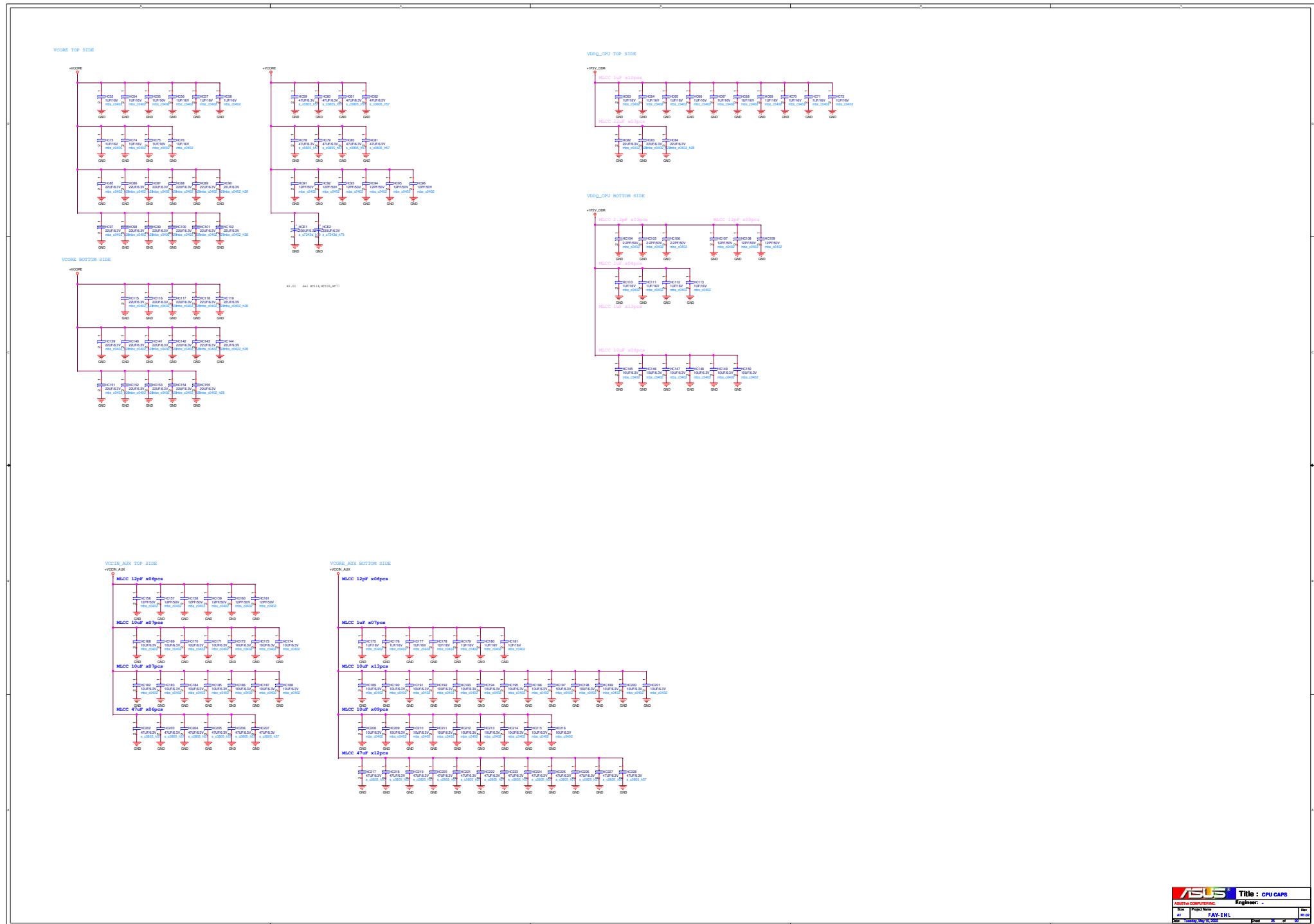


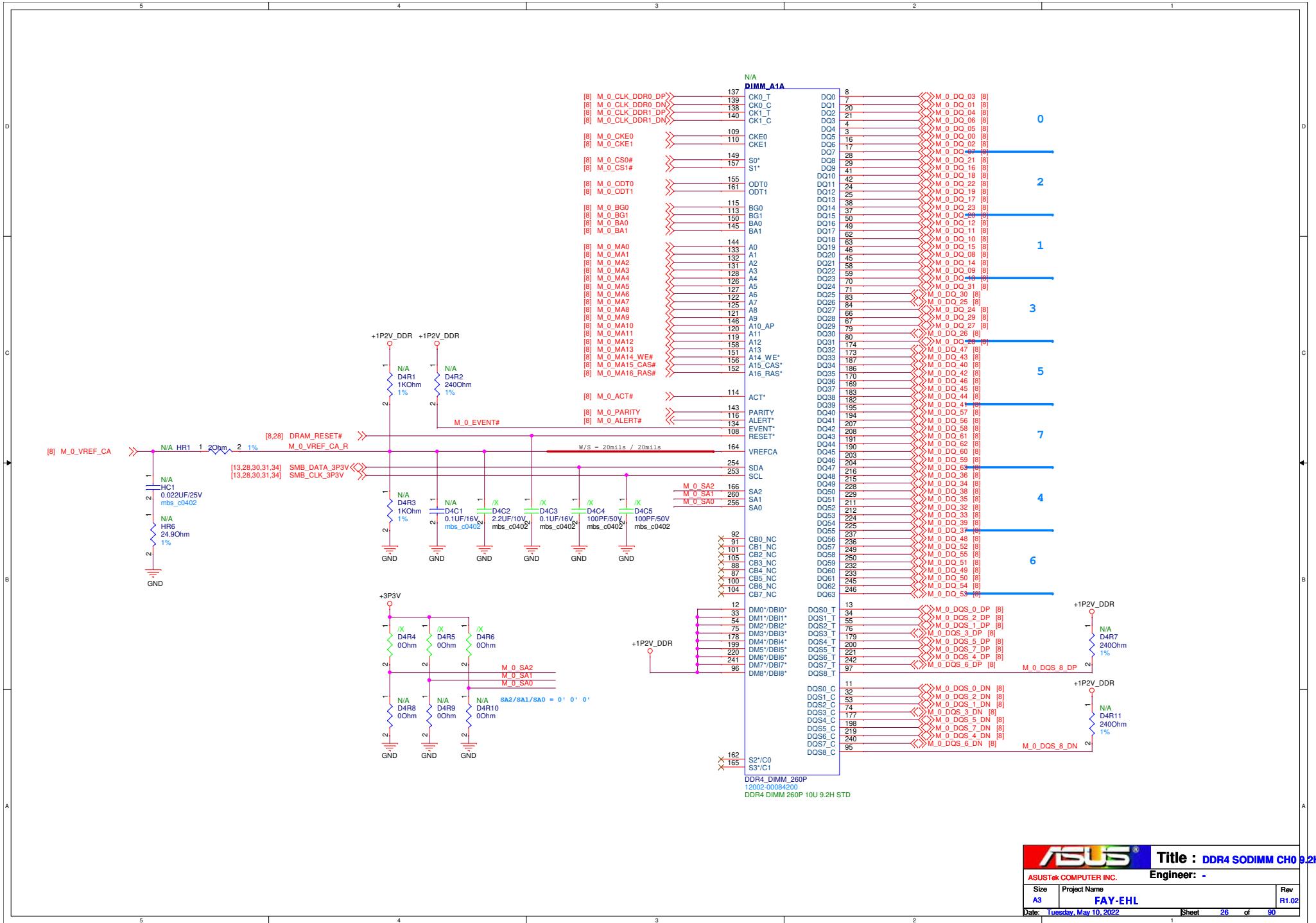


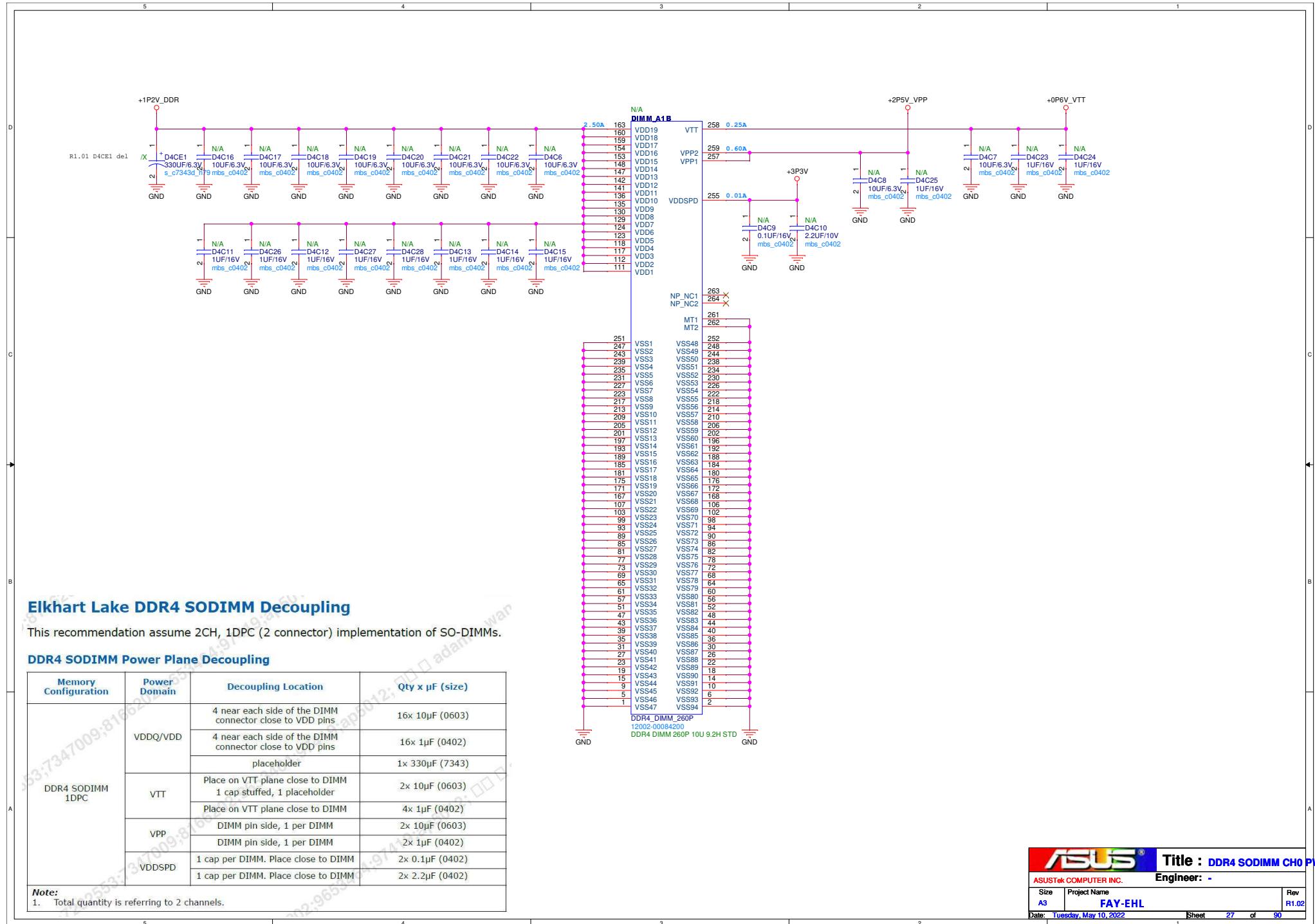


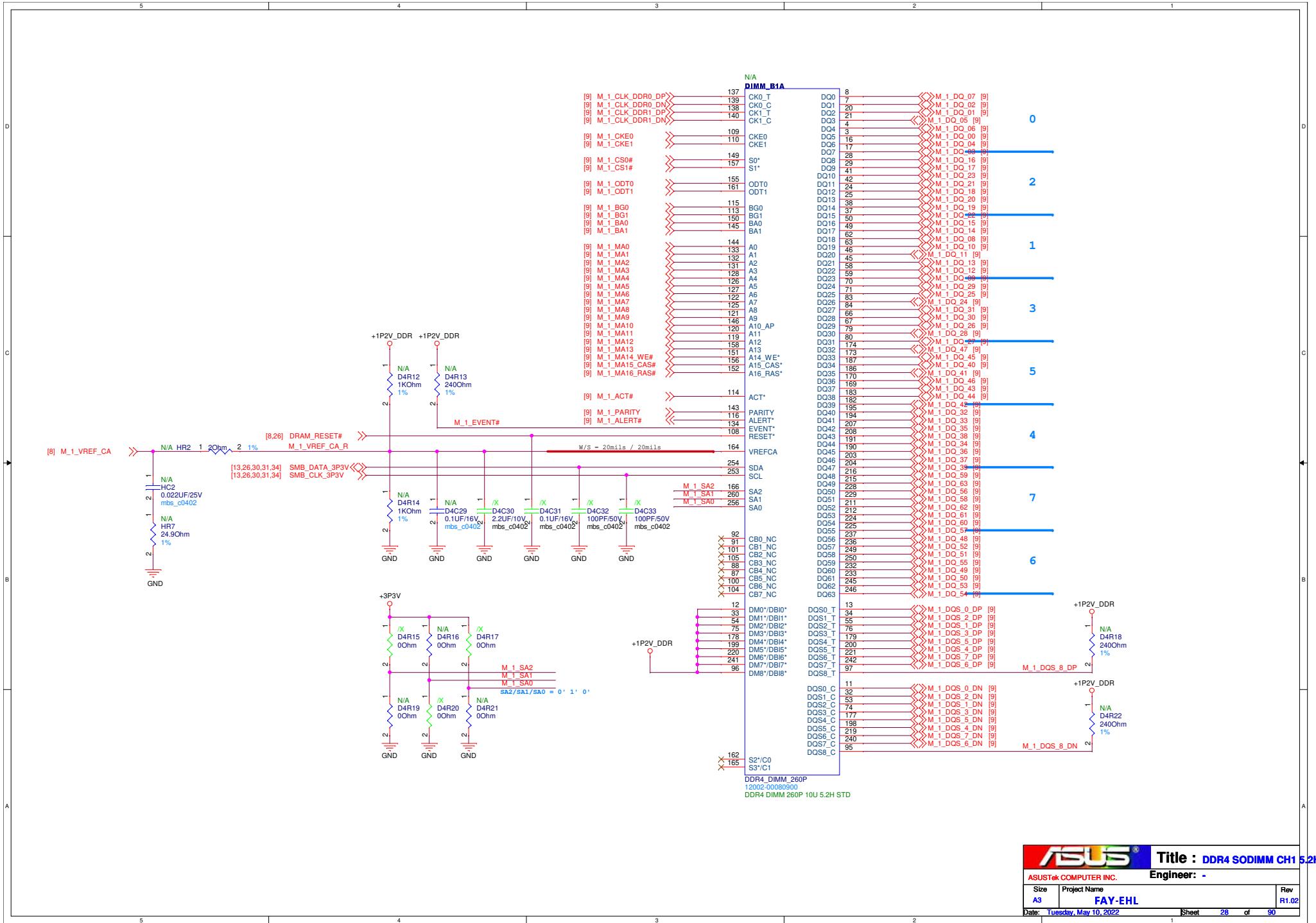


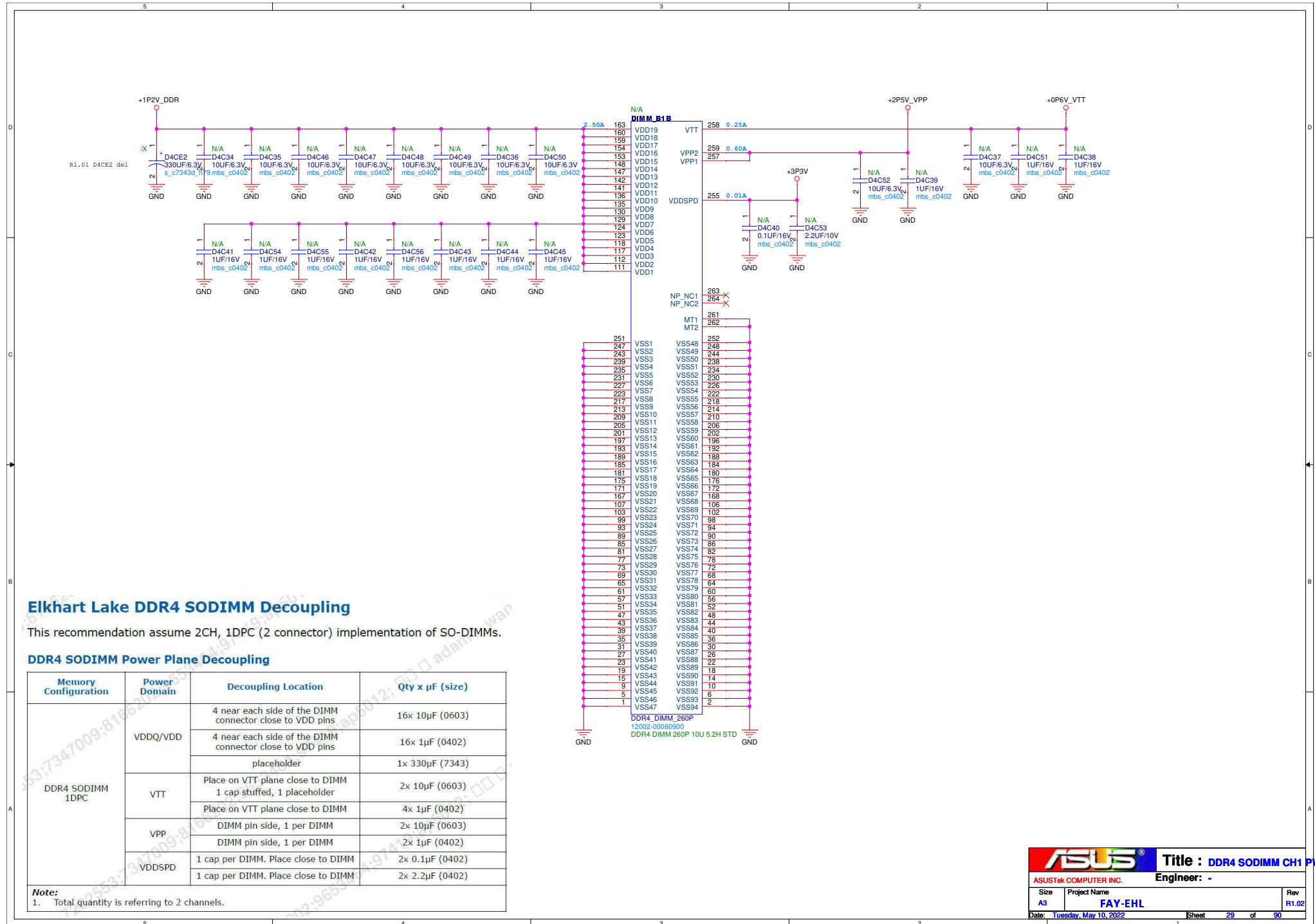


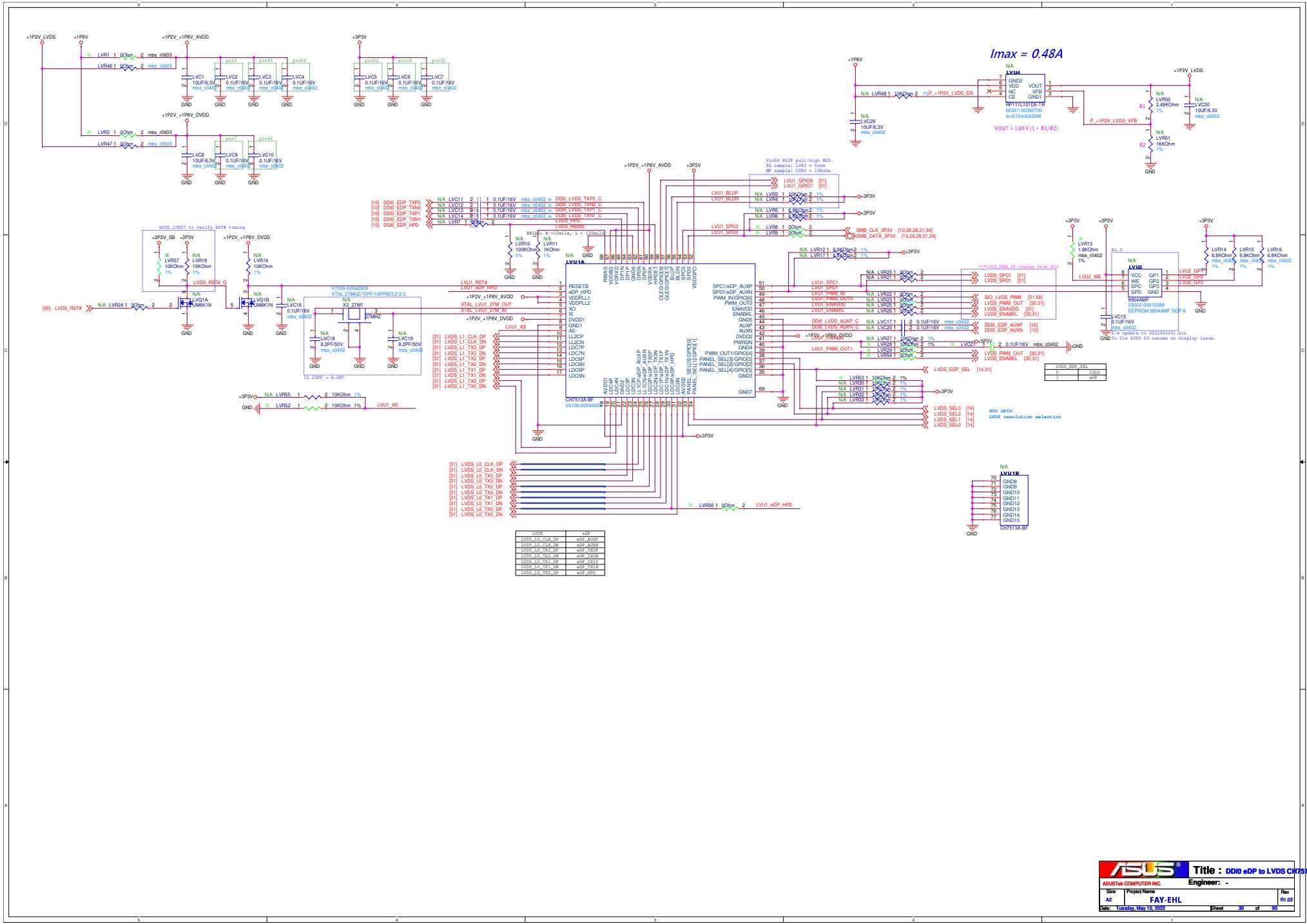


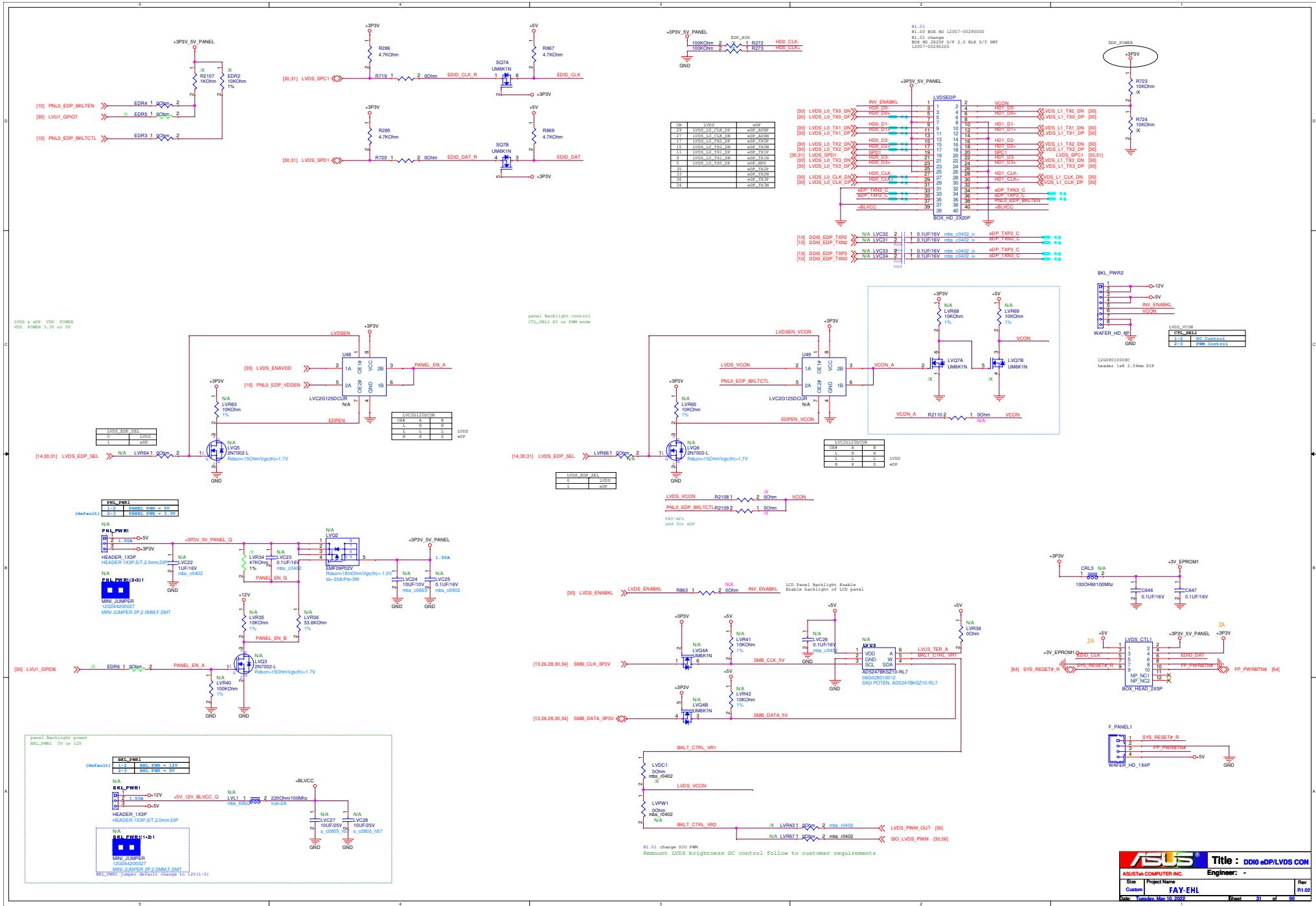


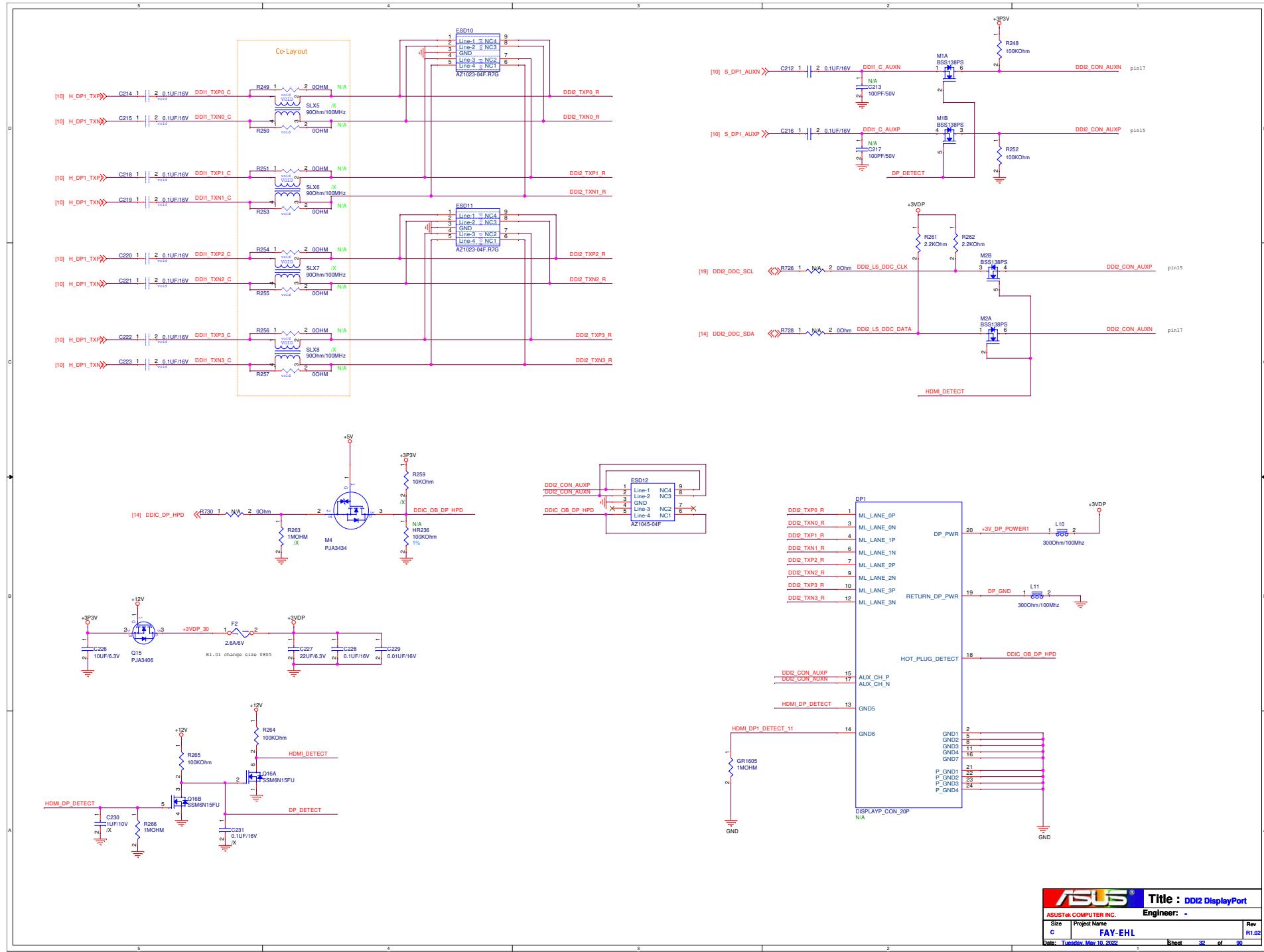




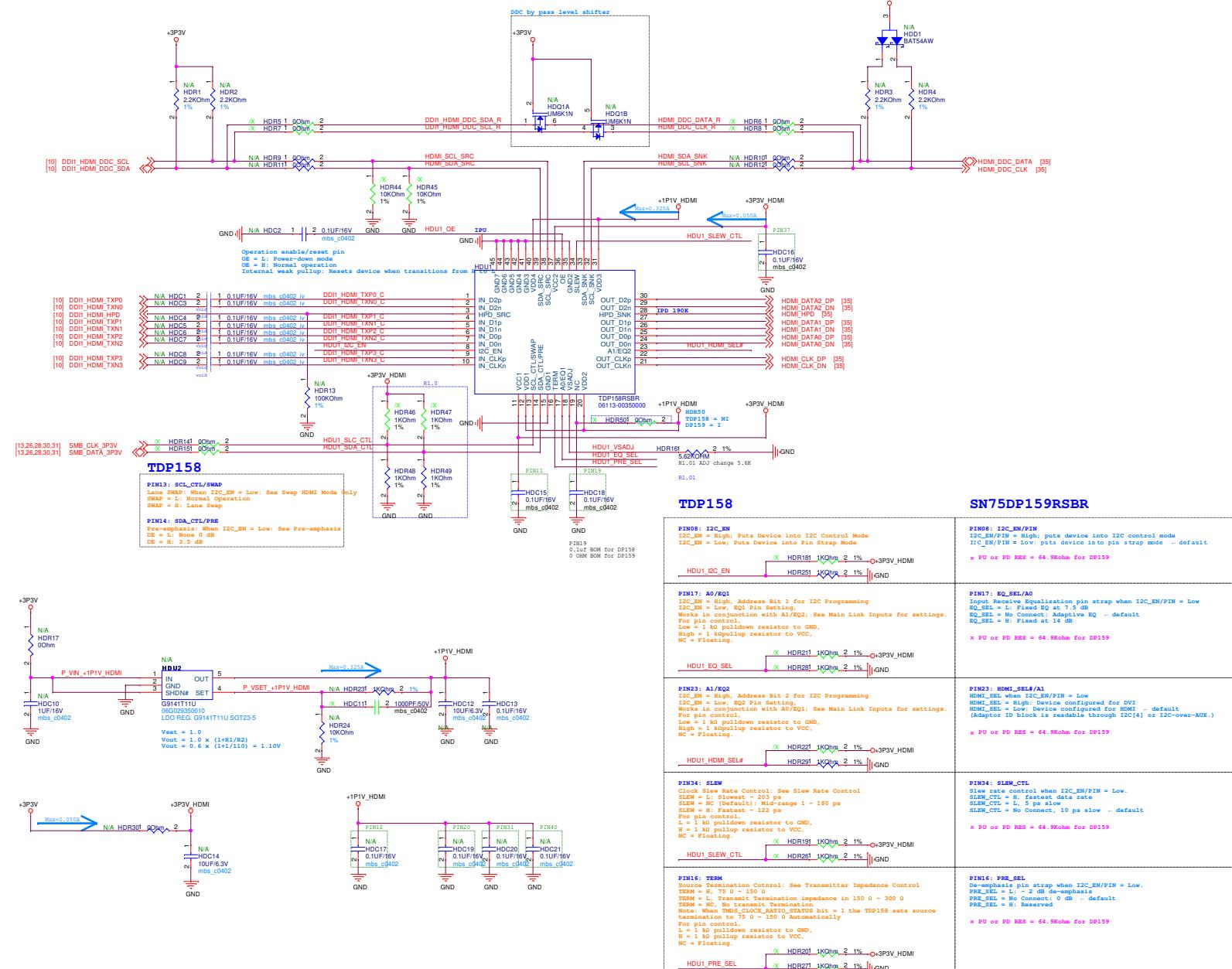








HDMI Level Shifter Redriver TDP158 Co-Lay HDMI Retimer SN75DP159RSBR



Title : DDH1 HDMI Level Shifter Redriver

Engineer: -

ASUSTek COMPUTER INC.

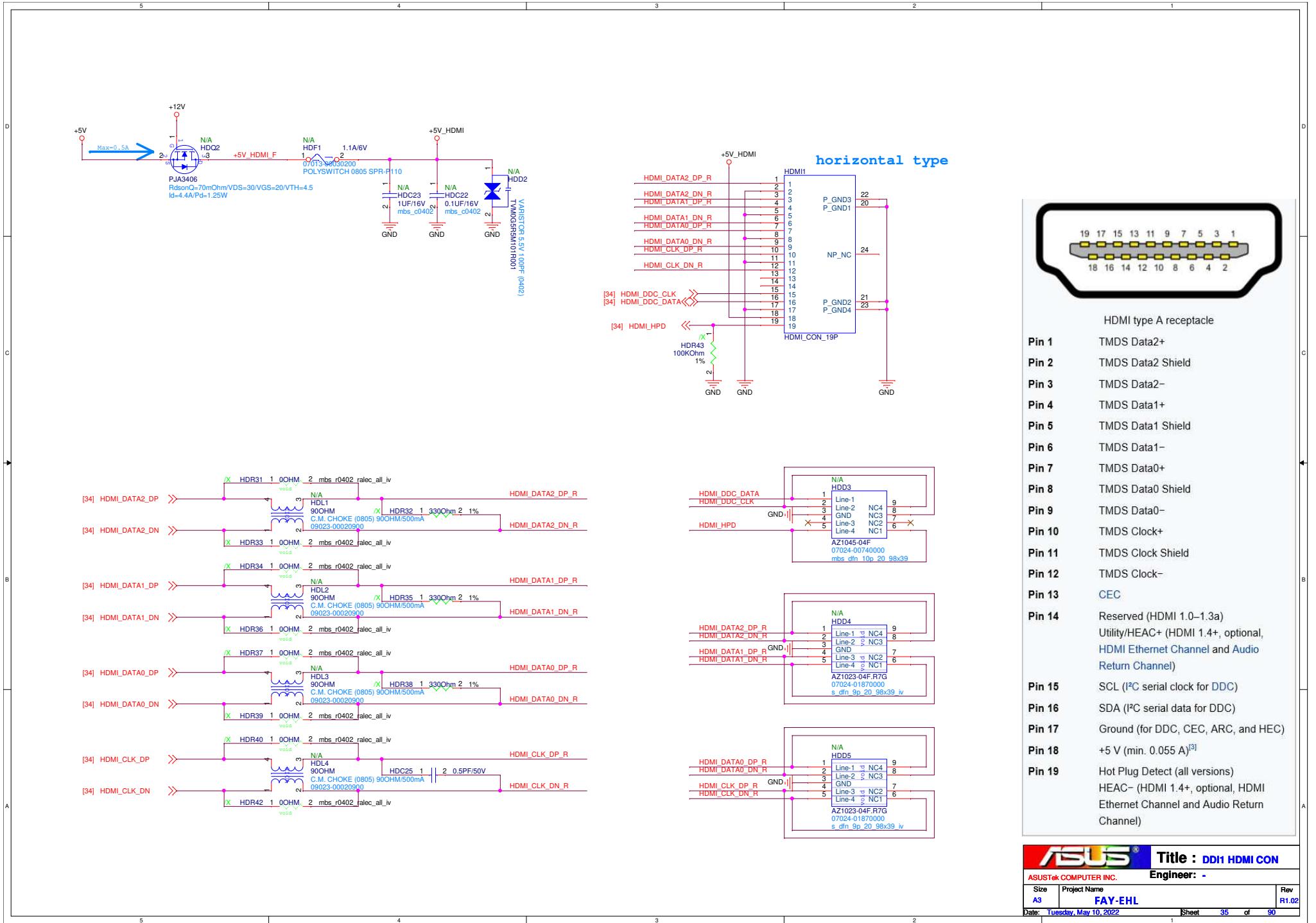
Size Project Name

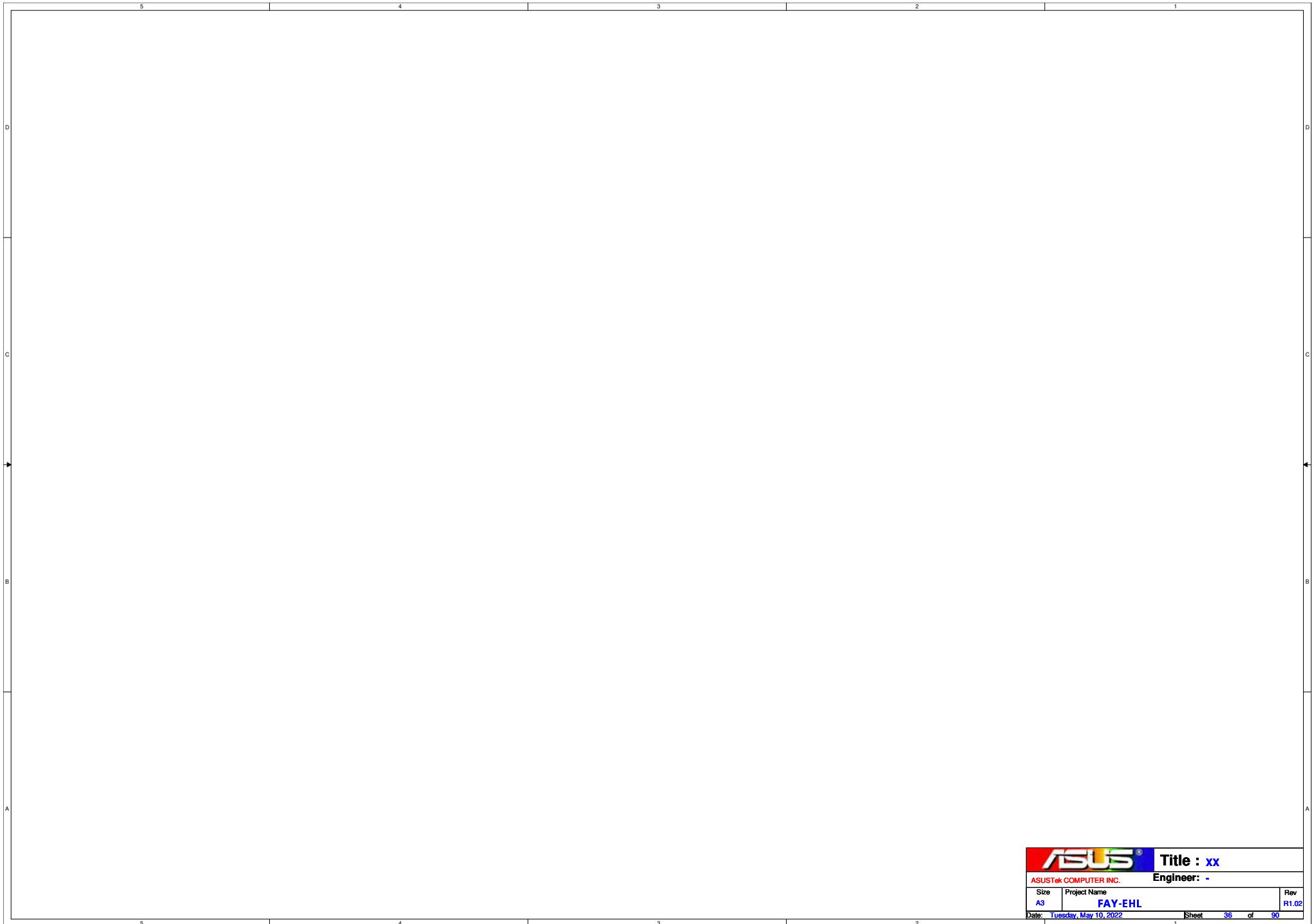
C FAY-EHL

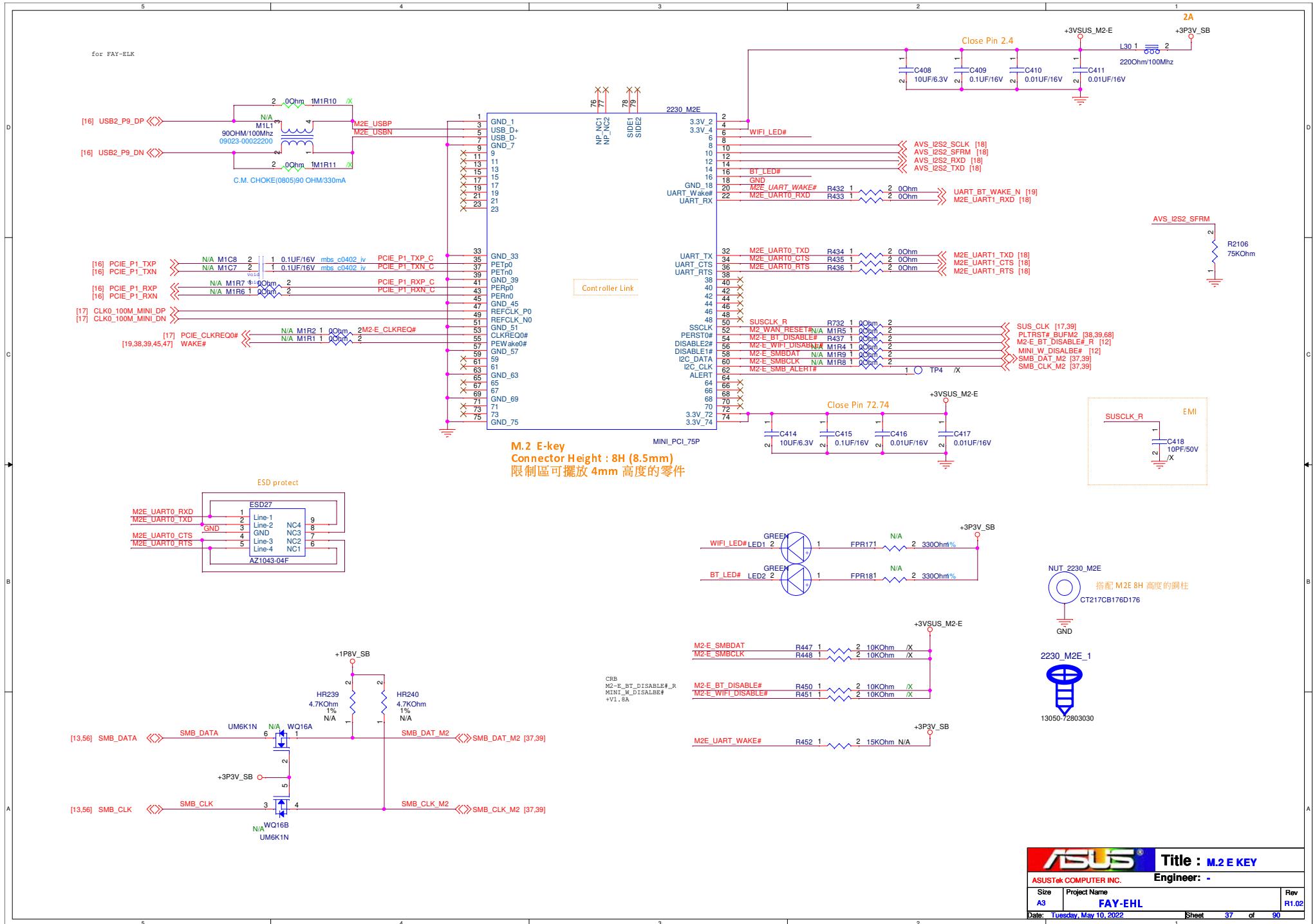
Rev R1.02

Date: Tuesday, May 10, 2022

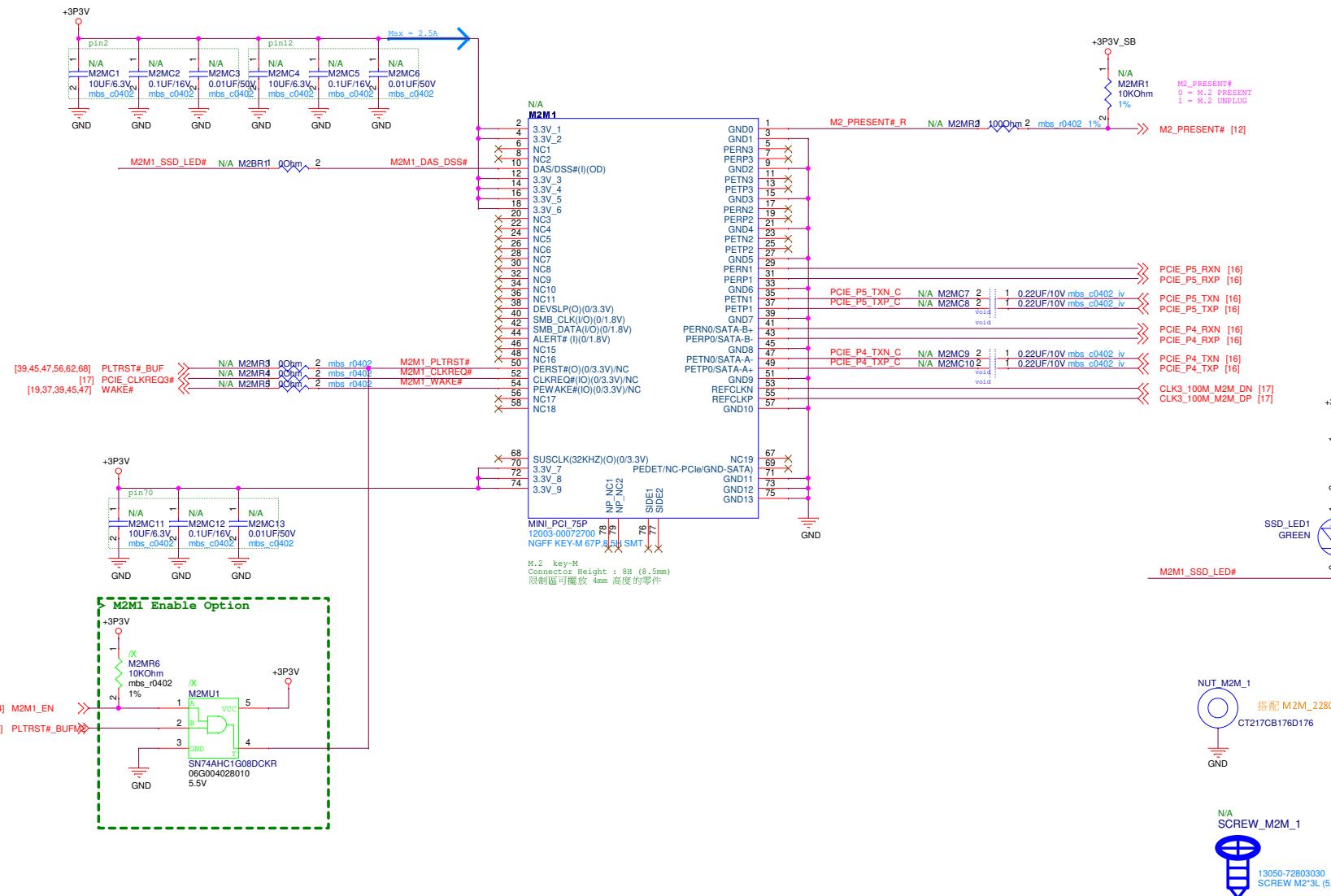
Sheet 34 of 90



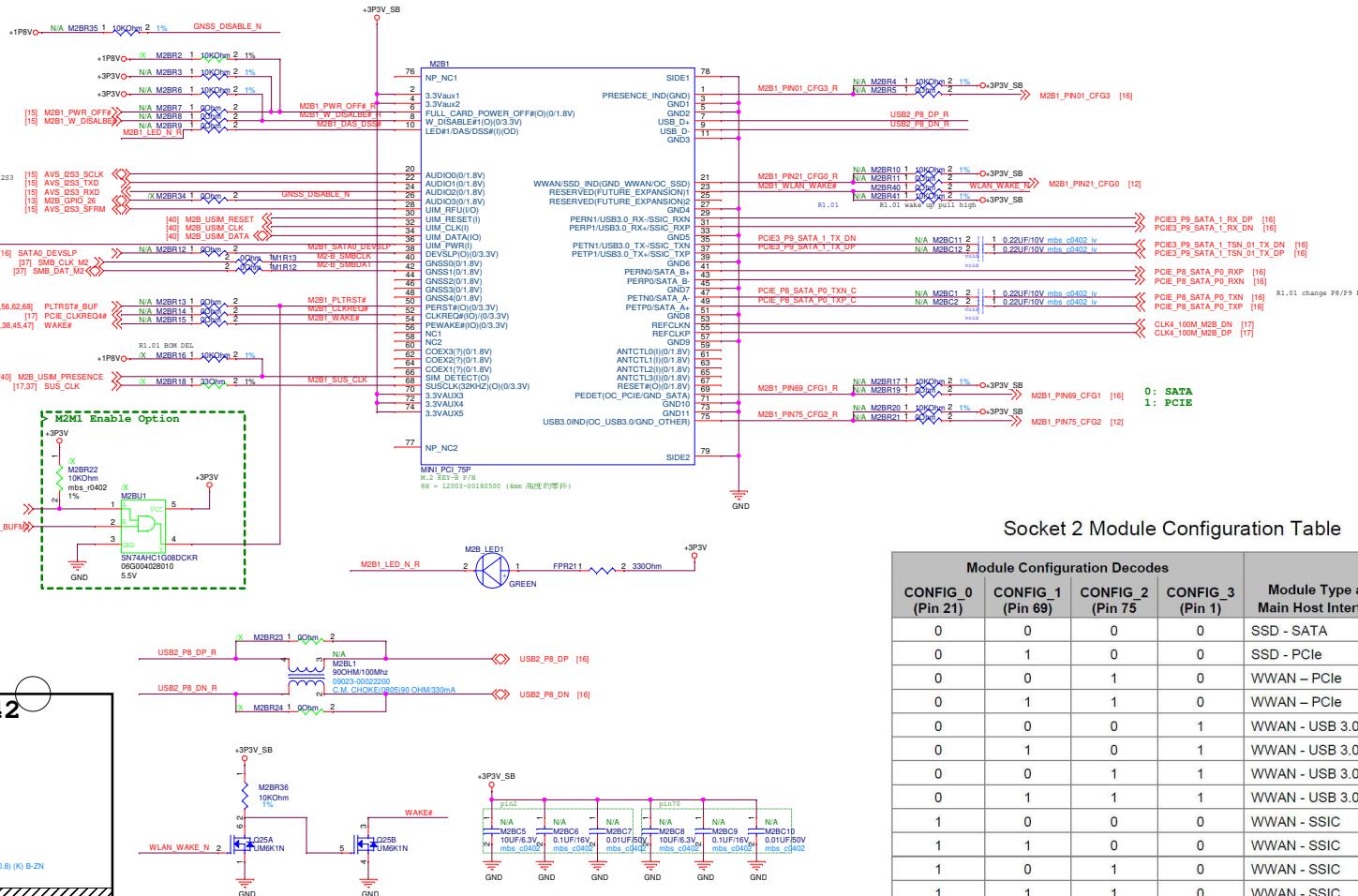




M.2 KEY-M 2280 (PCIE x2 NVME)



M.2 KEY-B 3042/3052



Socket 2 Module Configuration Table

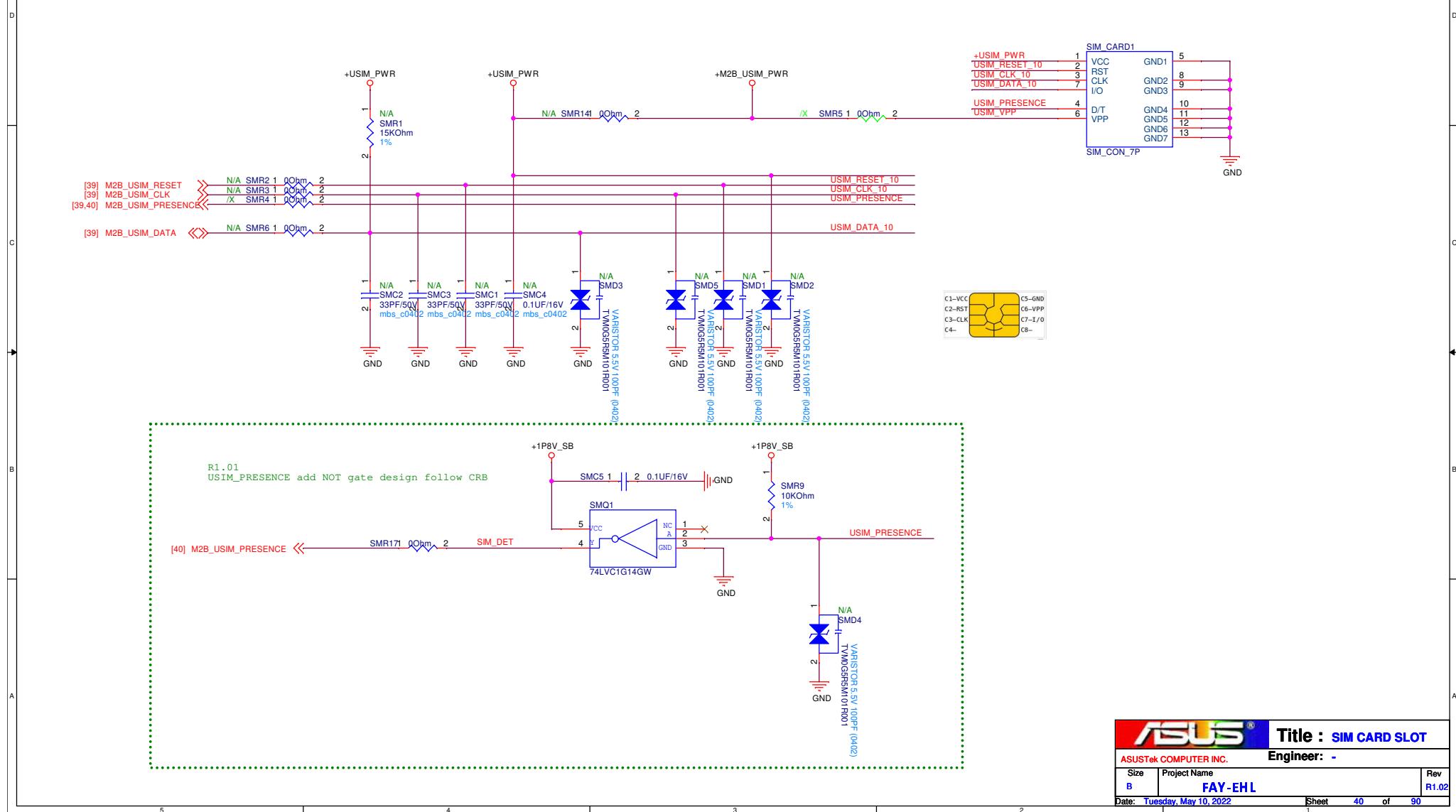
Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN - PCIe	0
0	1	1	0	WWAN - PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
1	0	1	1	RFU	N/A
1	1	1	1	No Module Present	N/A

¹ USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration).

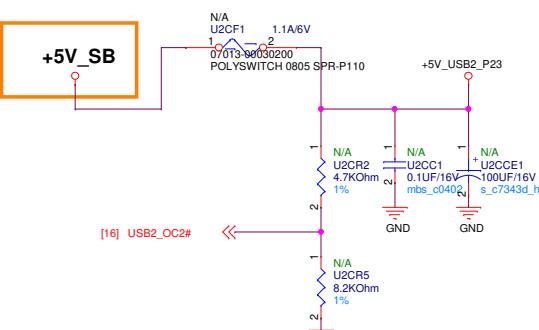
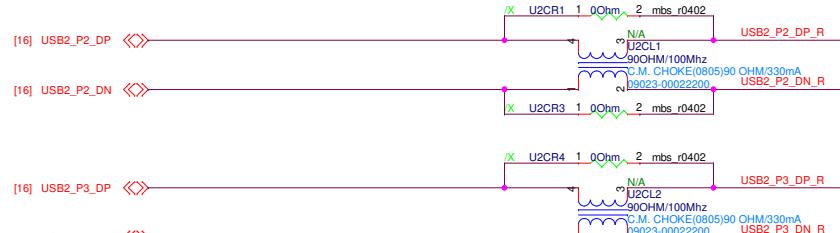
² Applicable to WWAN only

MICRO SIM SOCKET

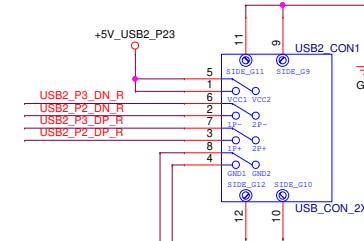
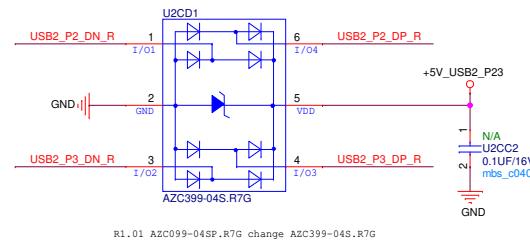
USIM support mini-PCIE & M.2 KEY-B slot by BOM option.
Default = M.2 KEY-B



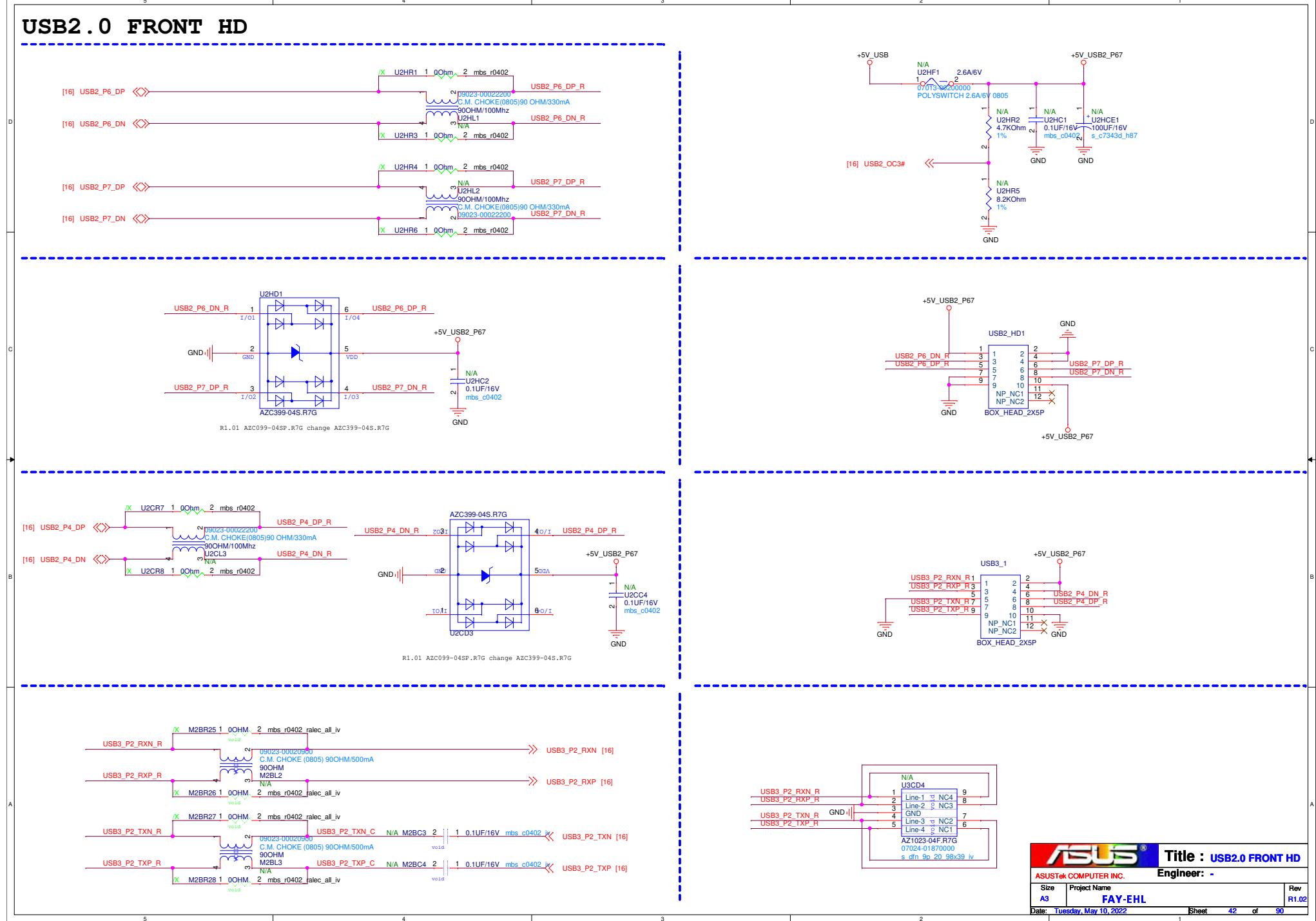
USB2.0 REAR CON



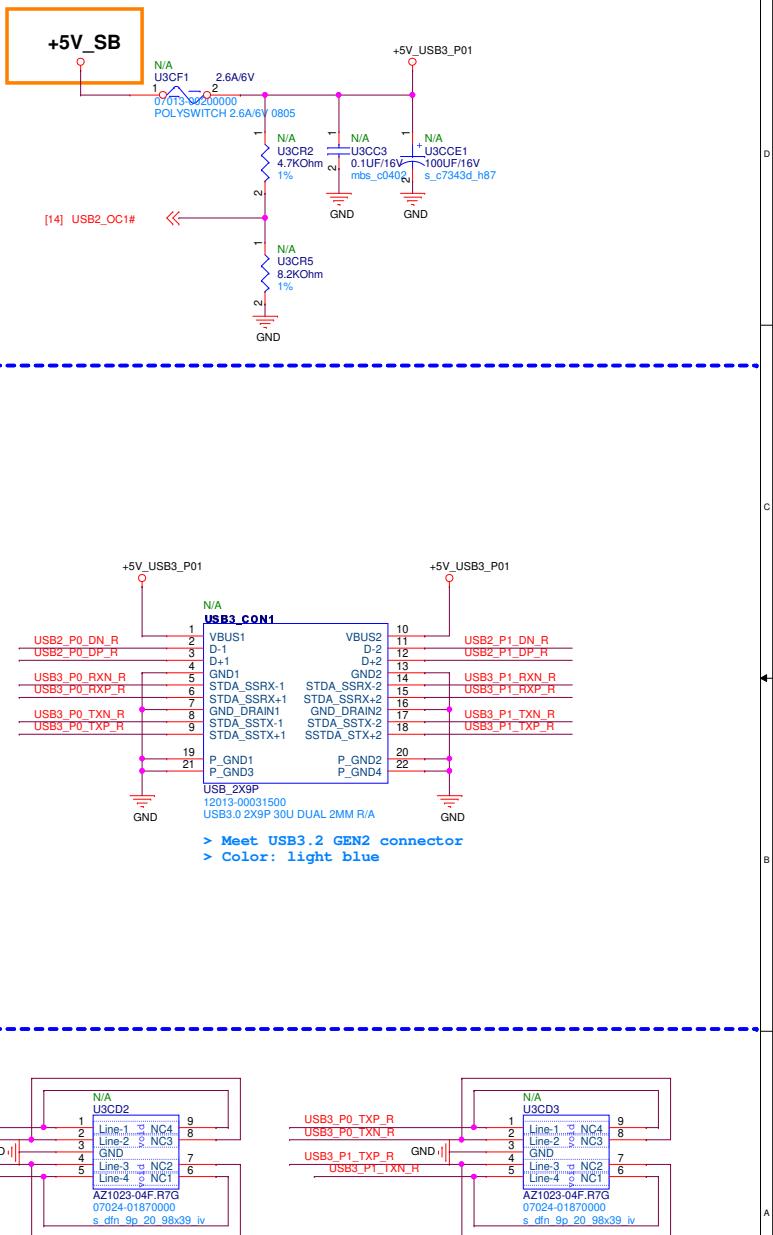
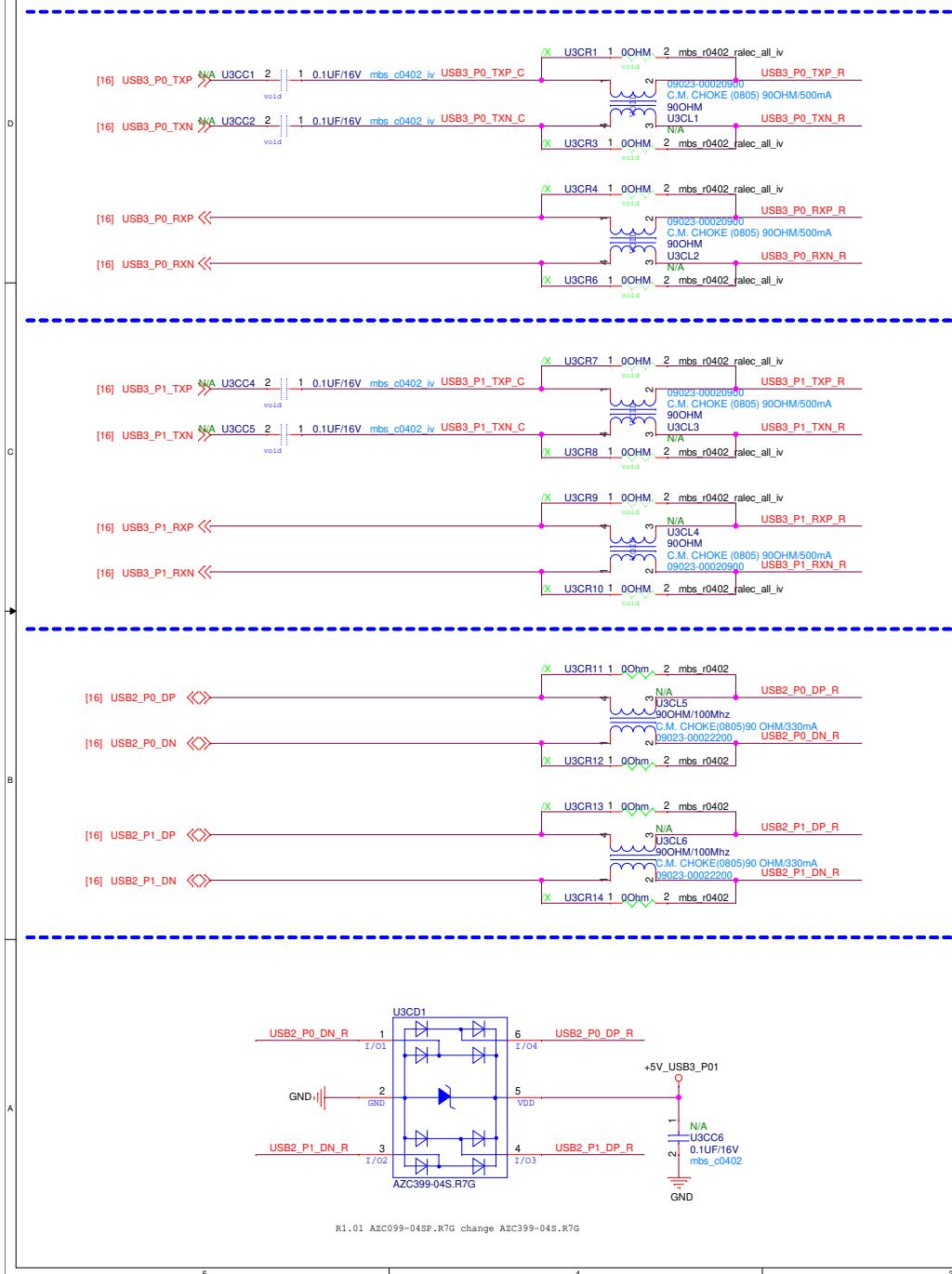
BOM Option for USB2 X2



USB2.0 FRONT HD

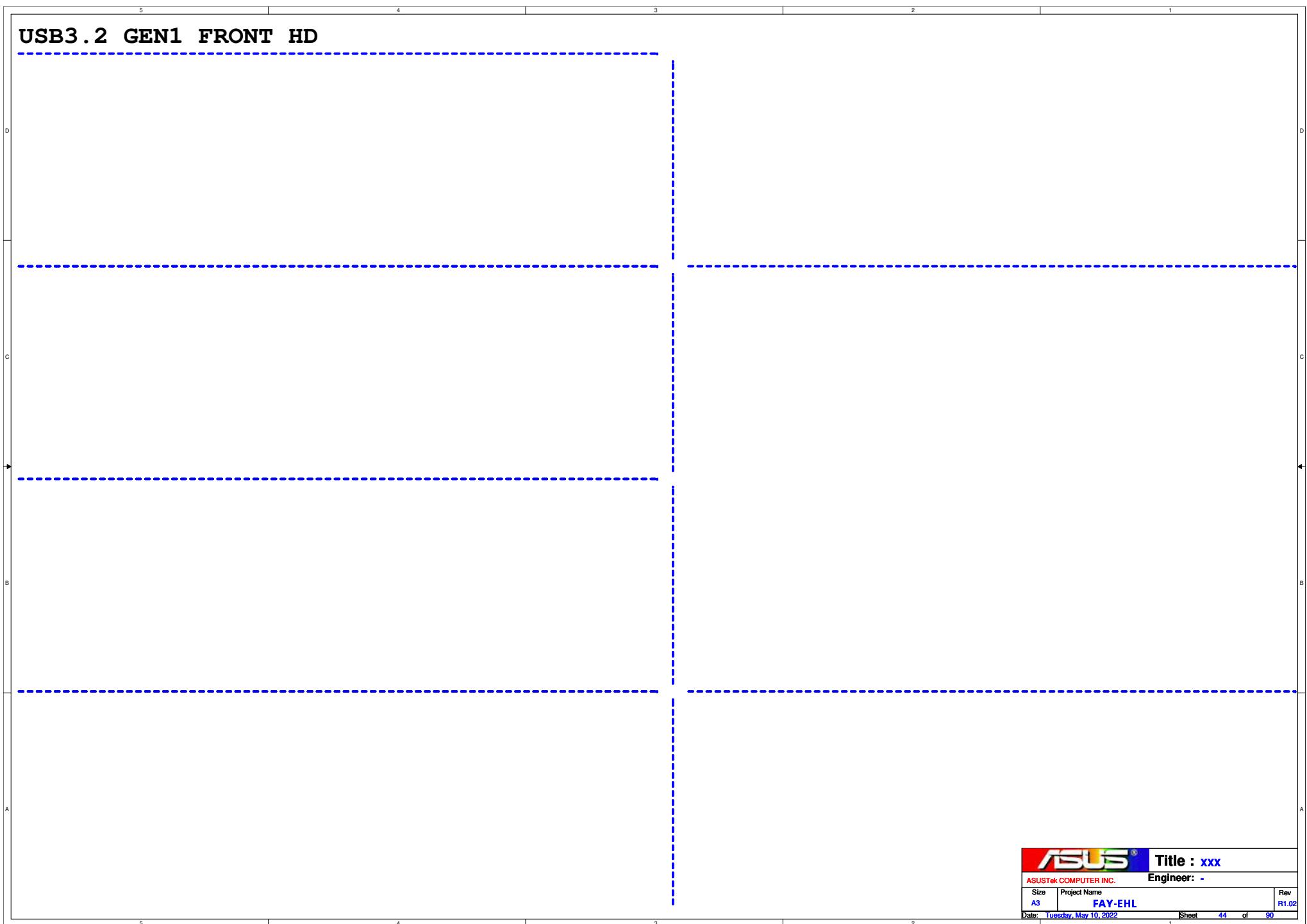


USB3.1 GEN2 REAR CON

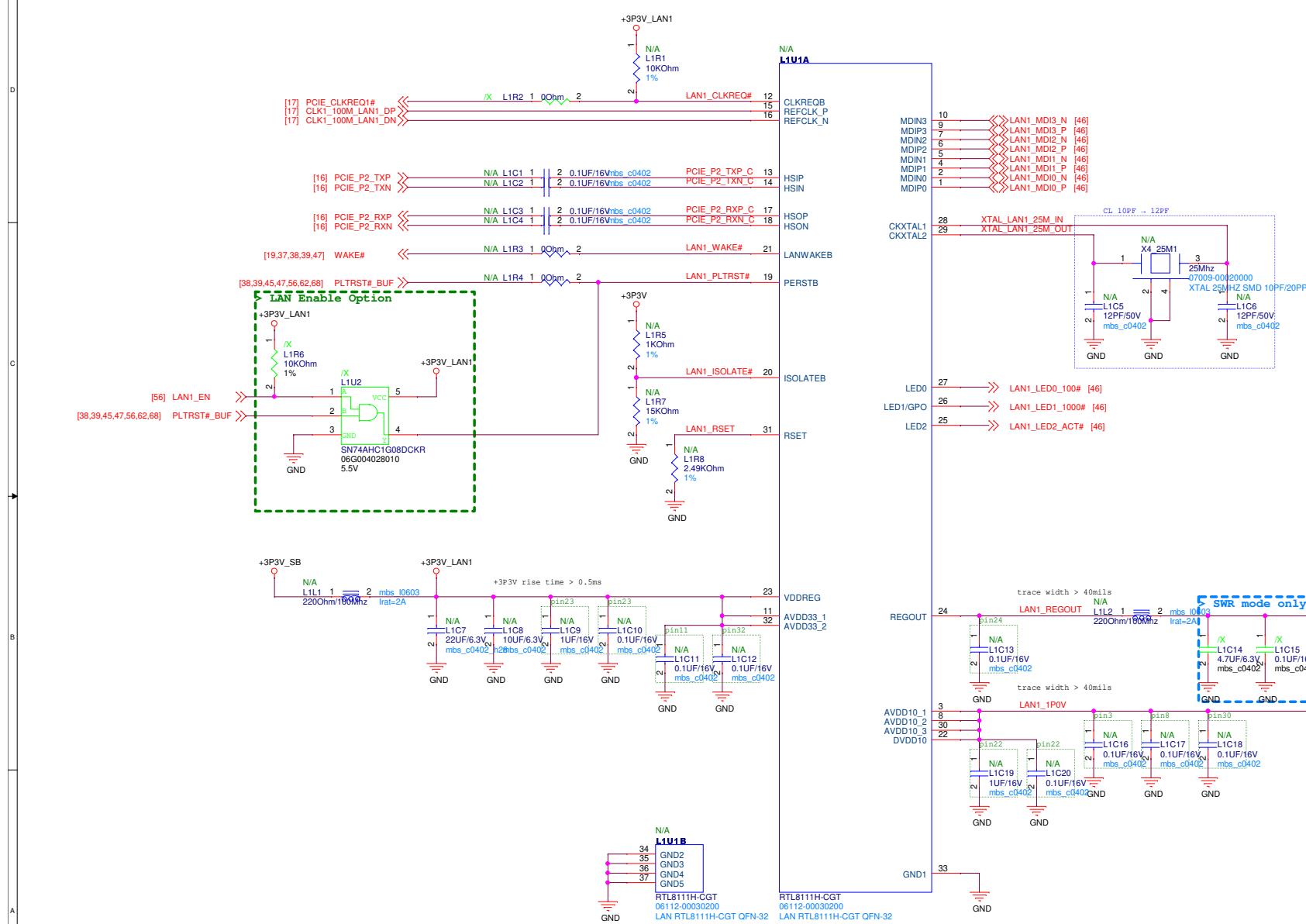


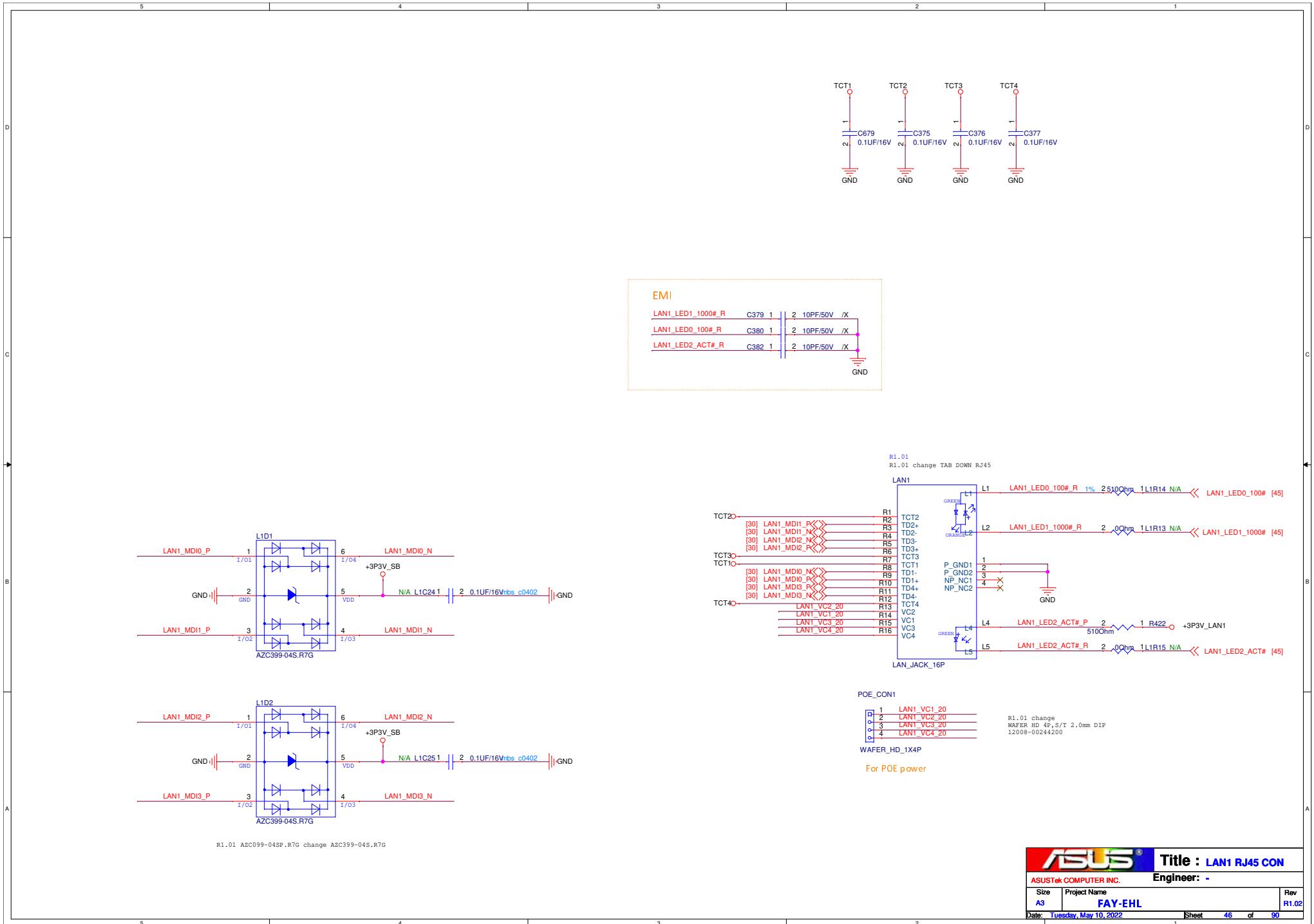
ASUS		Title : USB3.1 GEN1 REAR CON
ASUSTek COMPUTER INC.		
Engineer: -		
Size	Project Name	Rev
A3	FAY-EHL	R1.02
Date: Tuesday, May 10, 2022		Sheet
		43
		of
		90

USB3.2 GEN1 FRONT HD

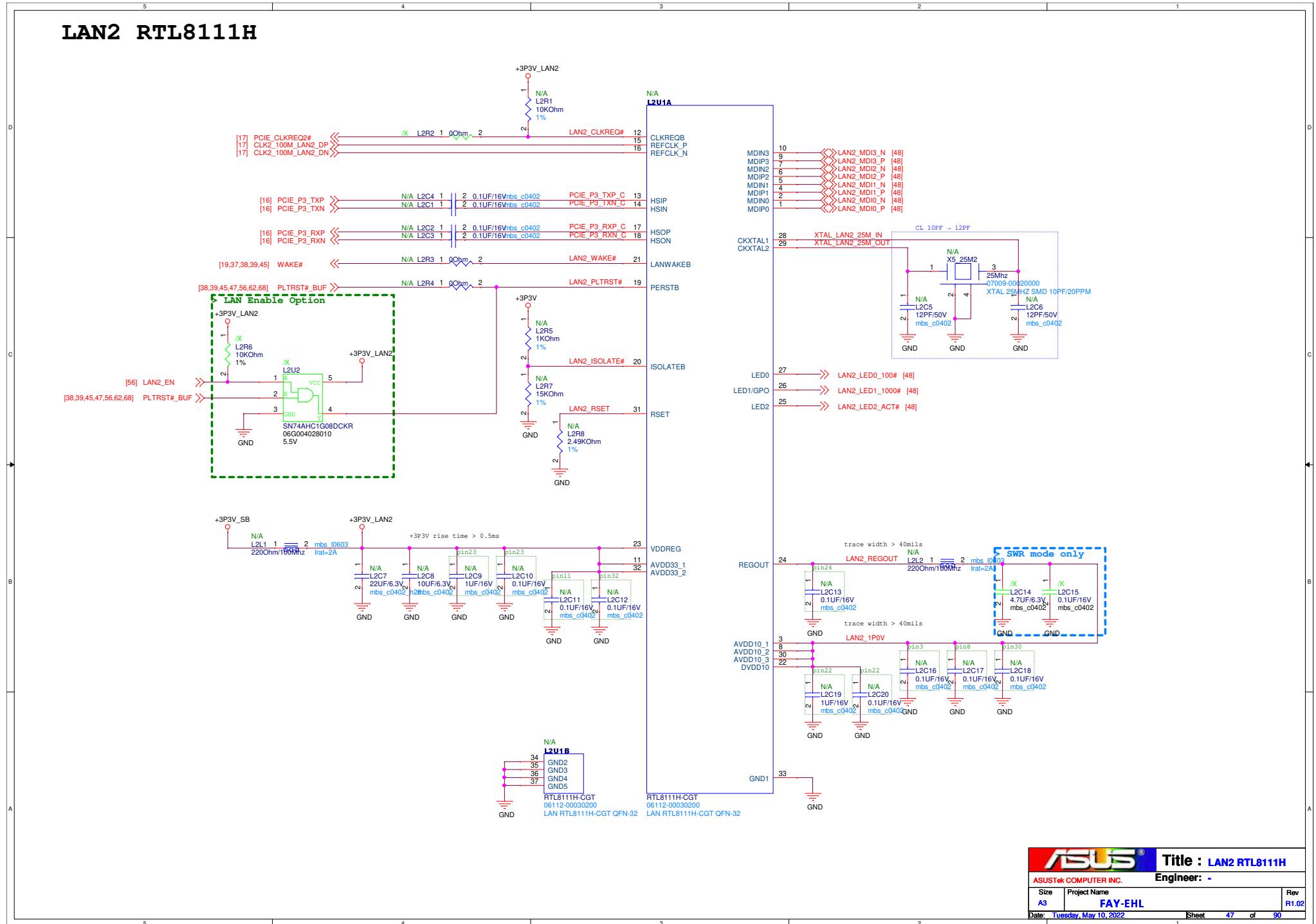


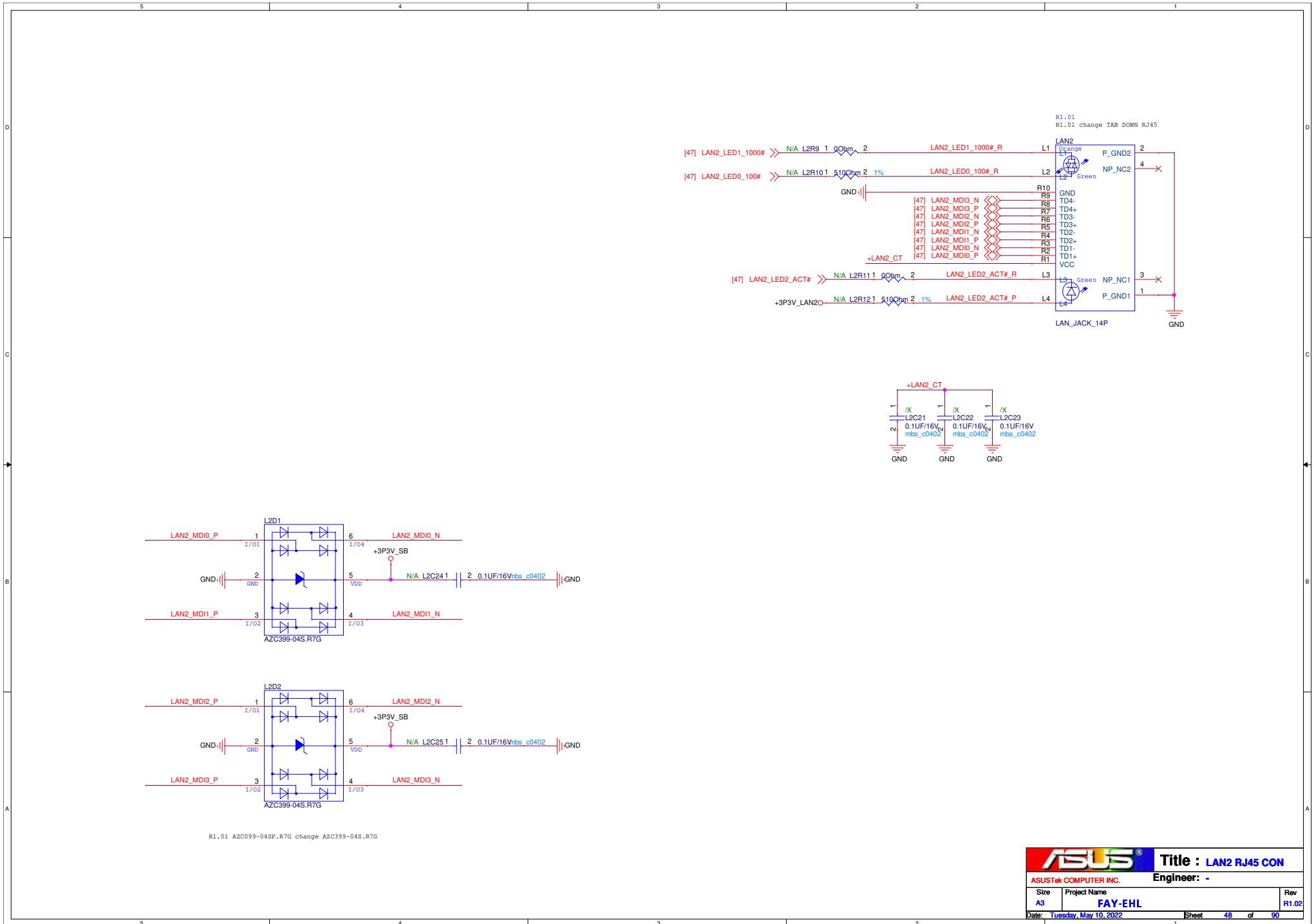
LAN1 RTL8111H





LAN2 RTL8111H





LAN3

D

D

C

C

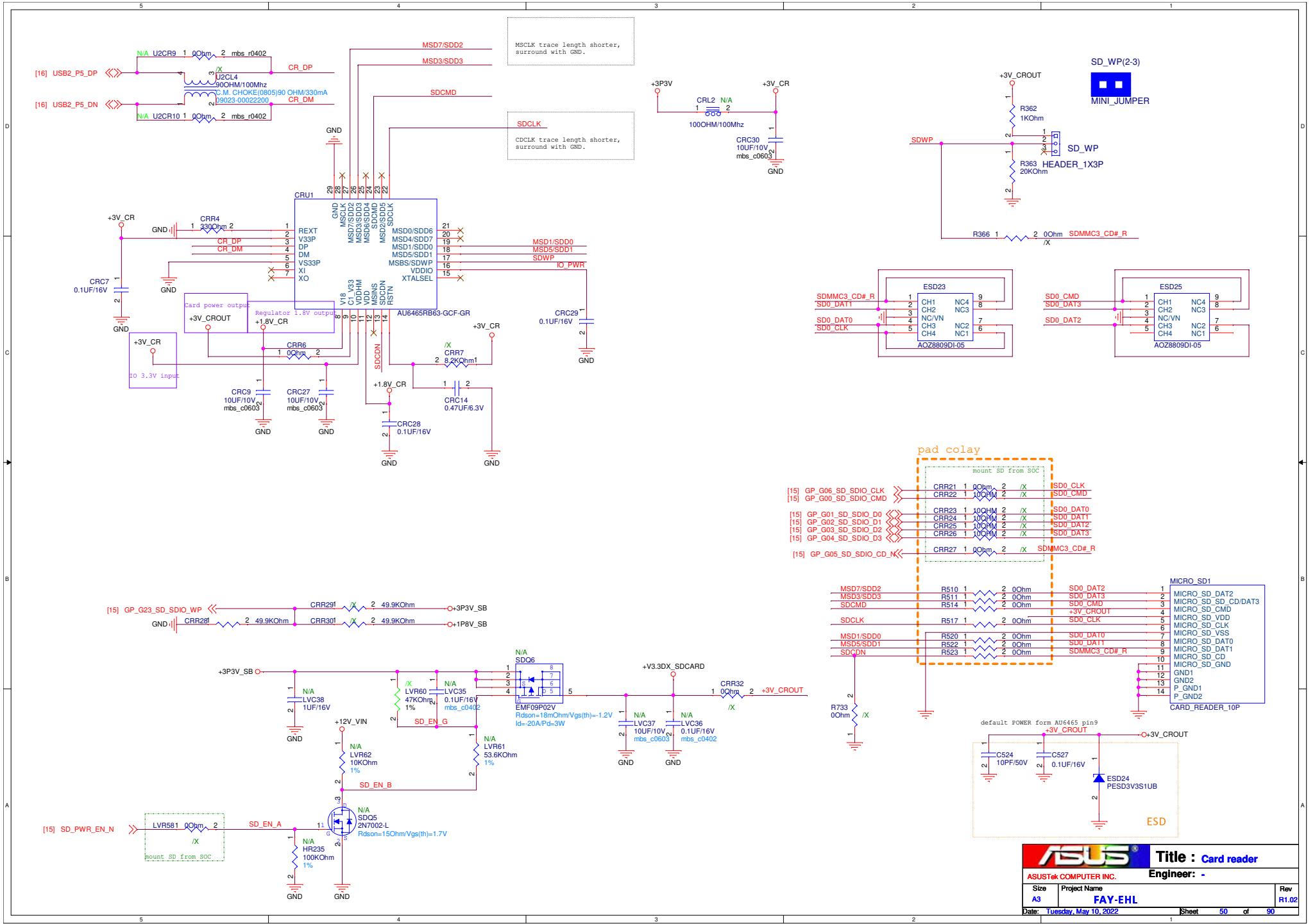
B

B

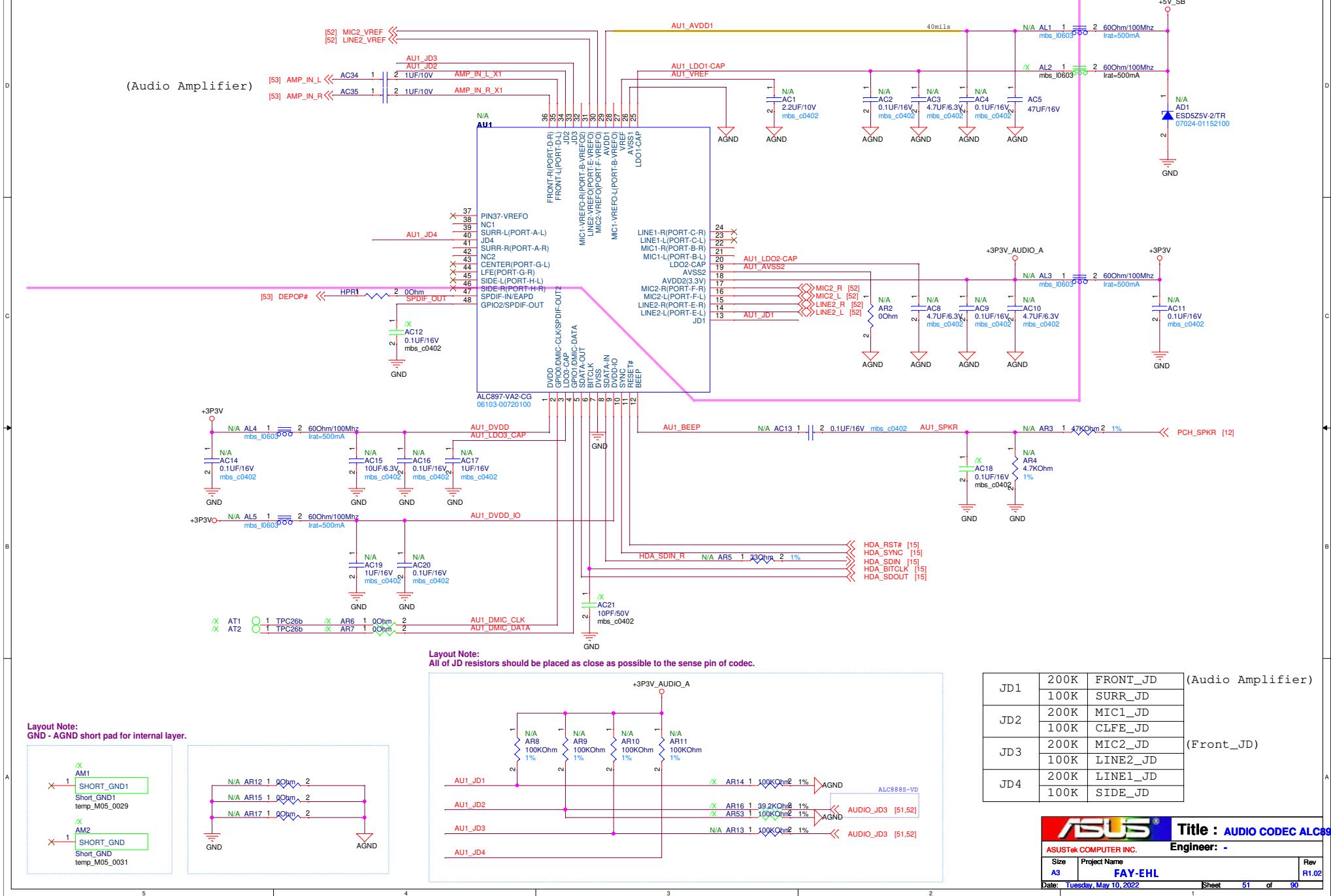
A

A

 Title : xxx	
ASUSTek COMPUTER INC. Engineer: -	
Size	Project Name
A3	FAY-EHL
Rev	R1.02
Date:	Tuesday, May 10, 2022
Sheet	49 of 90

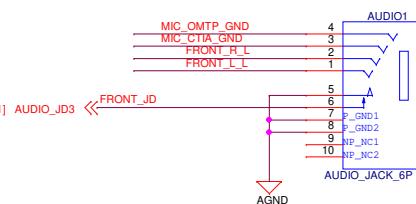
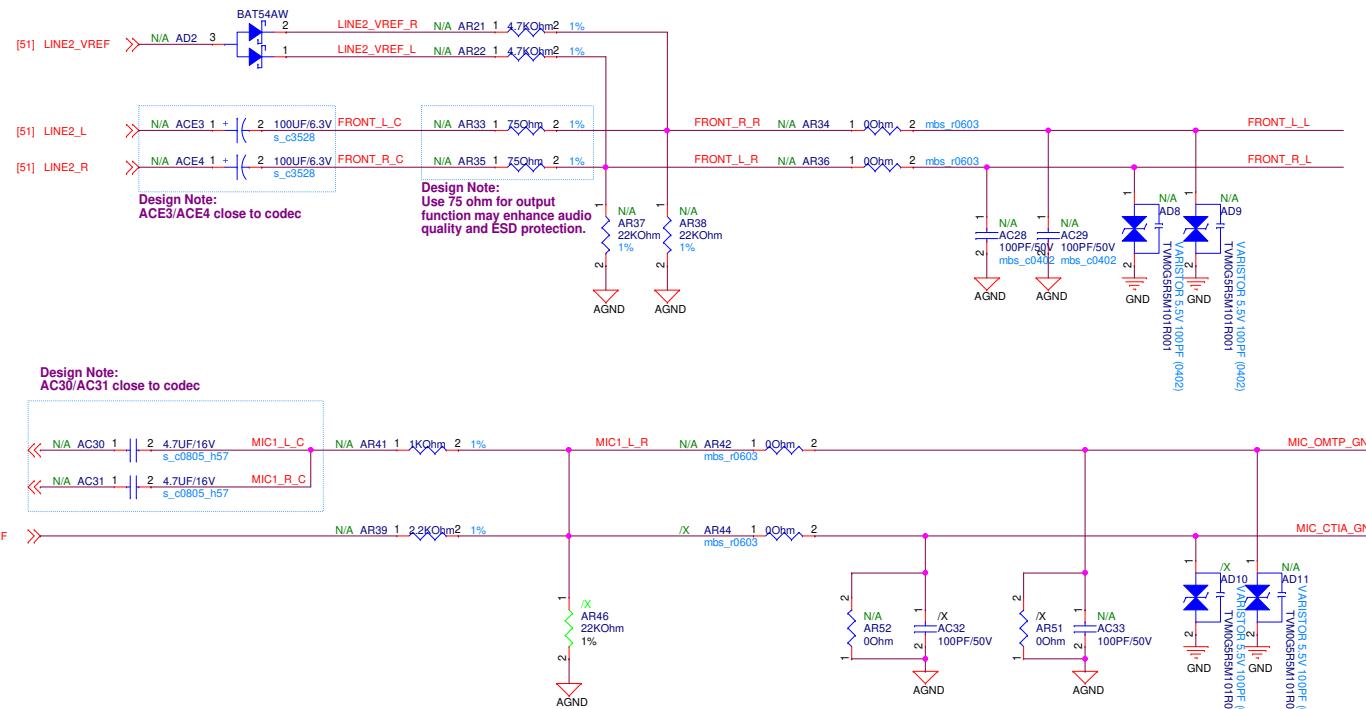


AUDIO ALC897-VA2

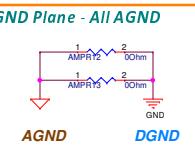
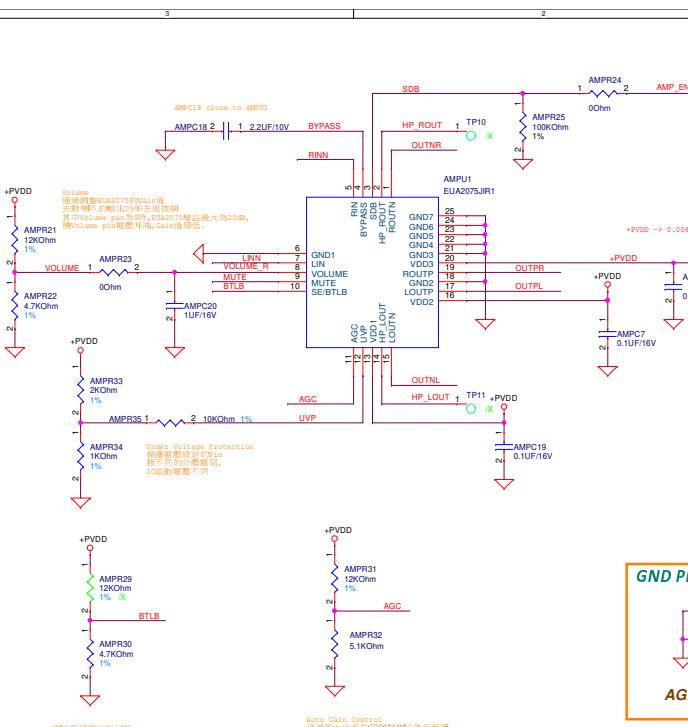
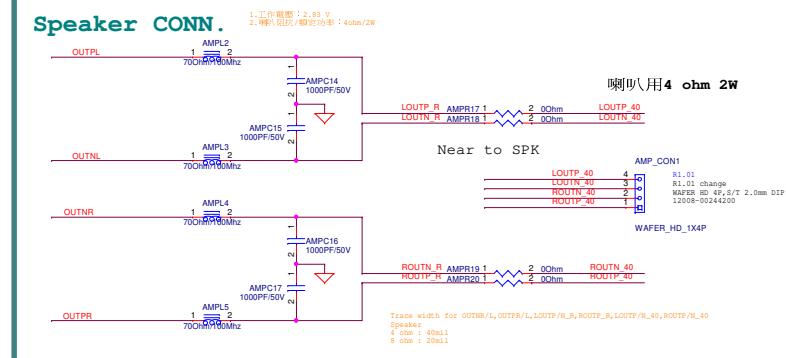
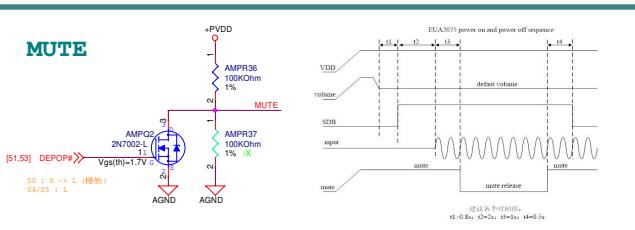
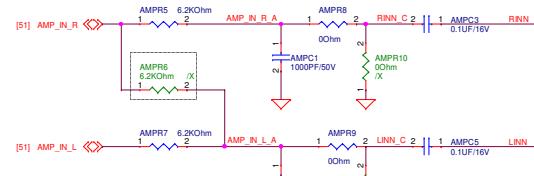
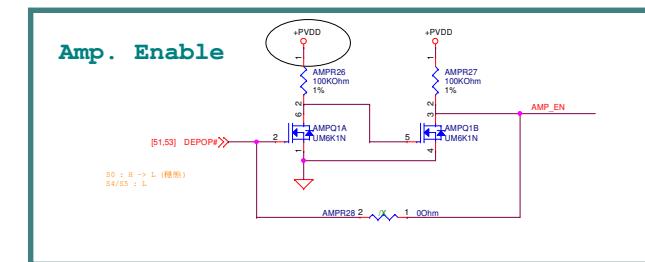


AUDIO FRONT HD

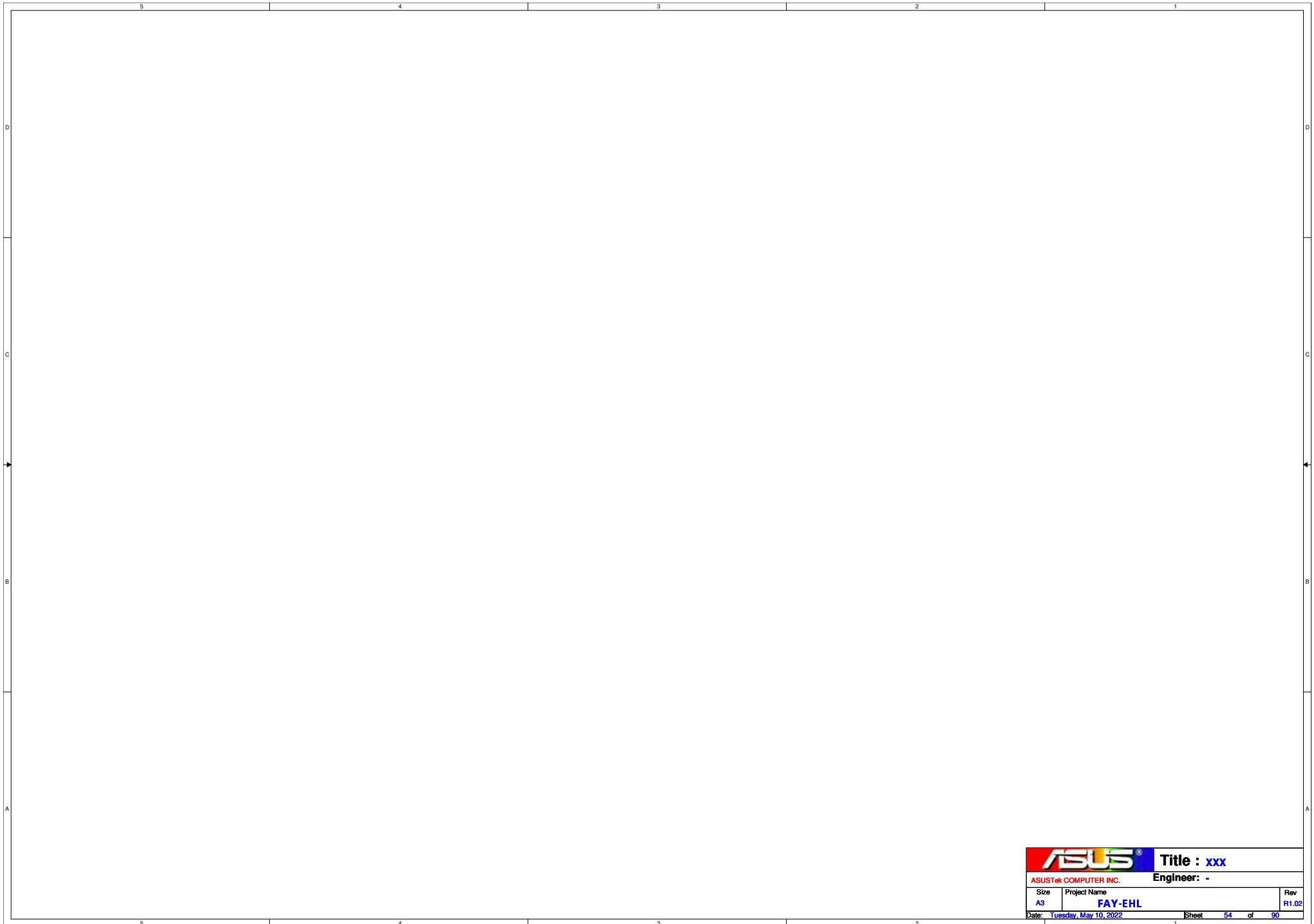
AUDIO REAR PHONE JACK



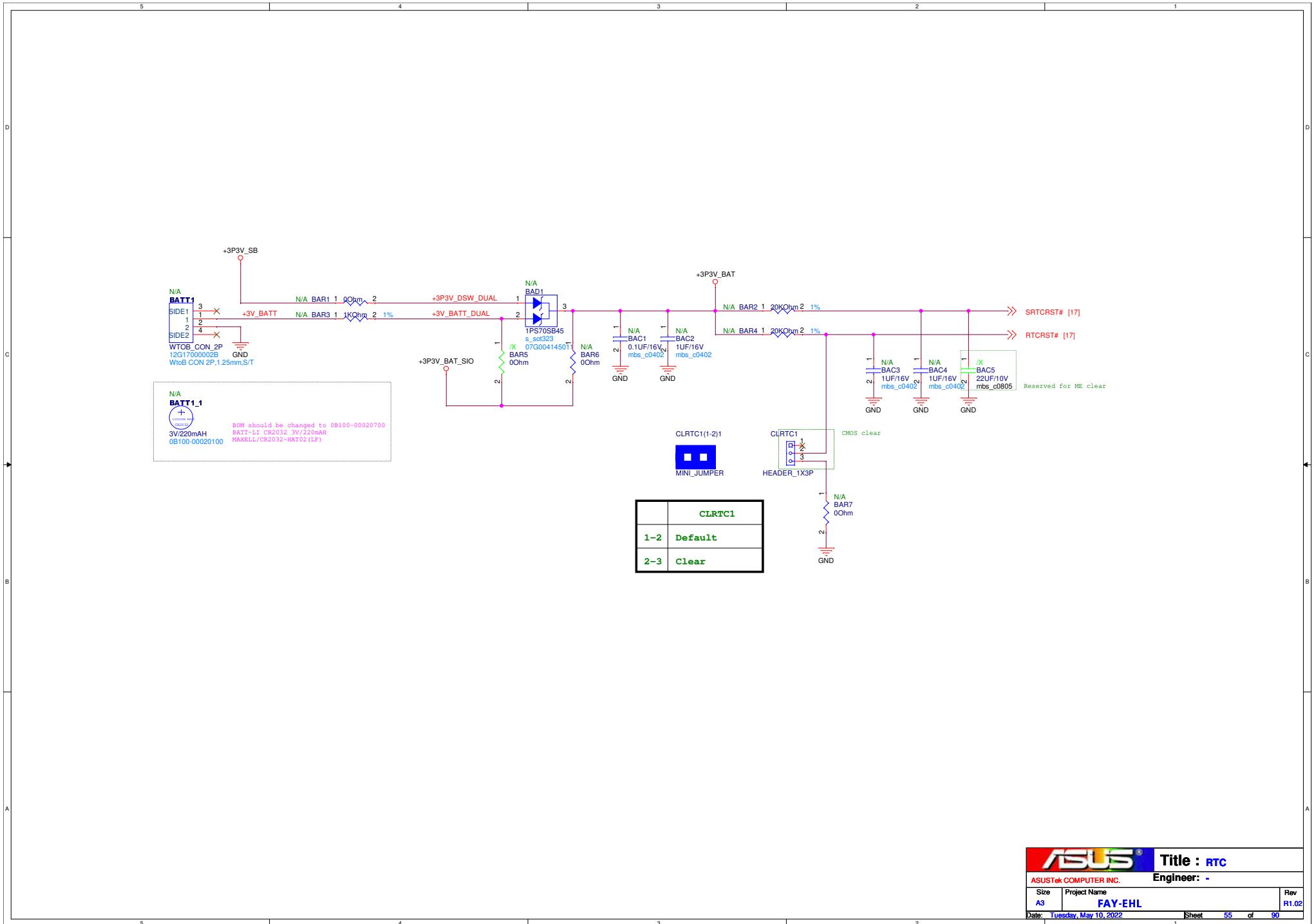
Audio Amp. EUA2075JIR1

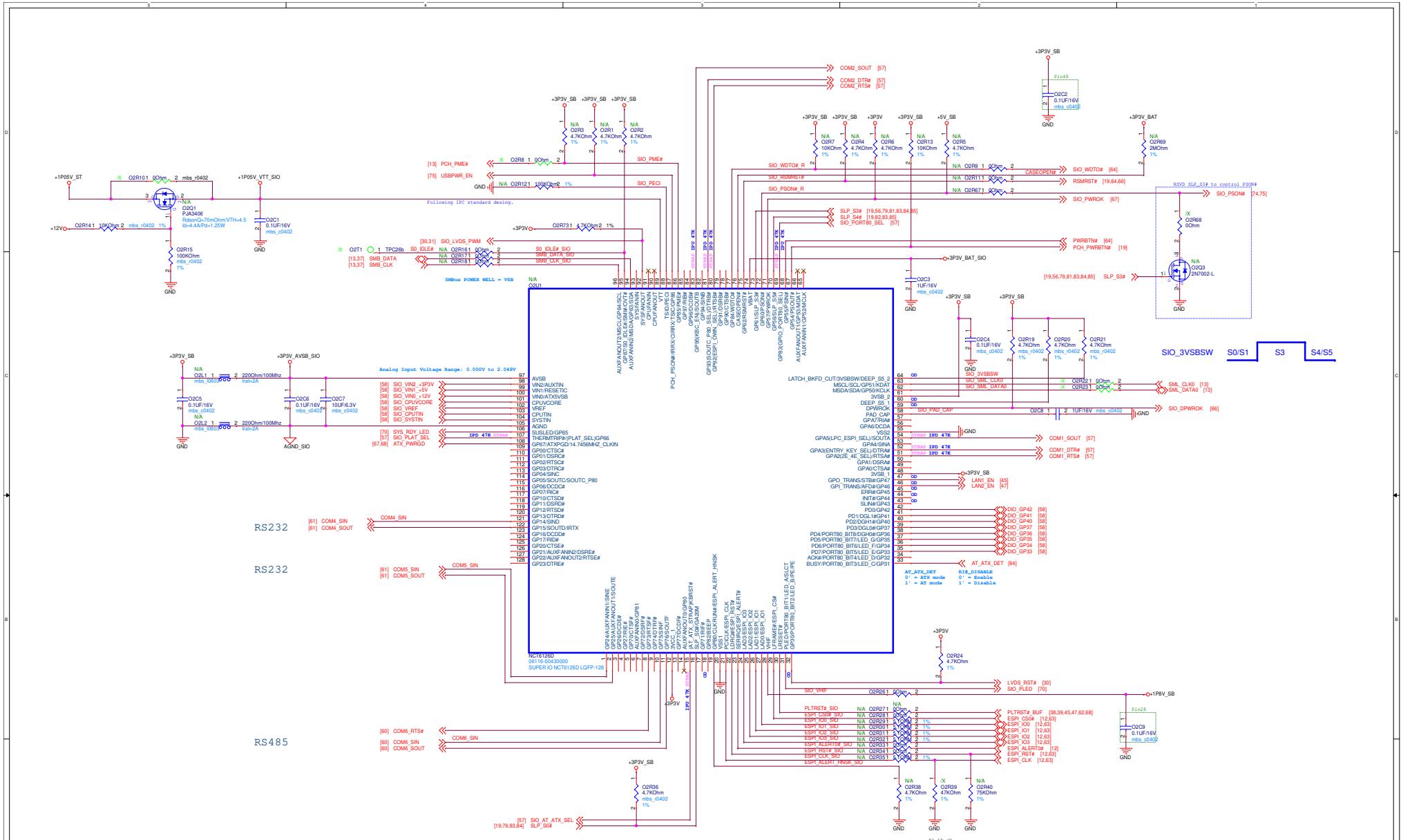


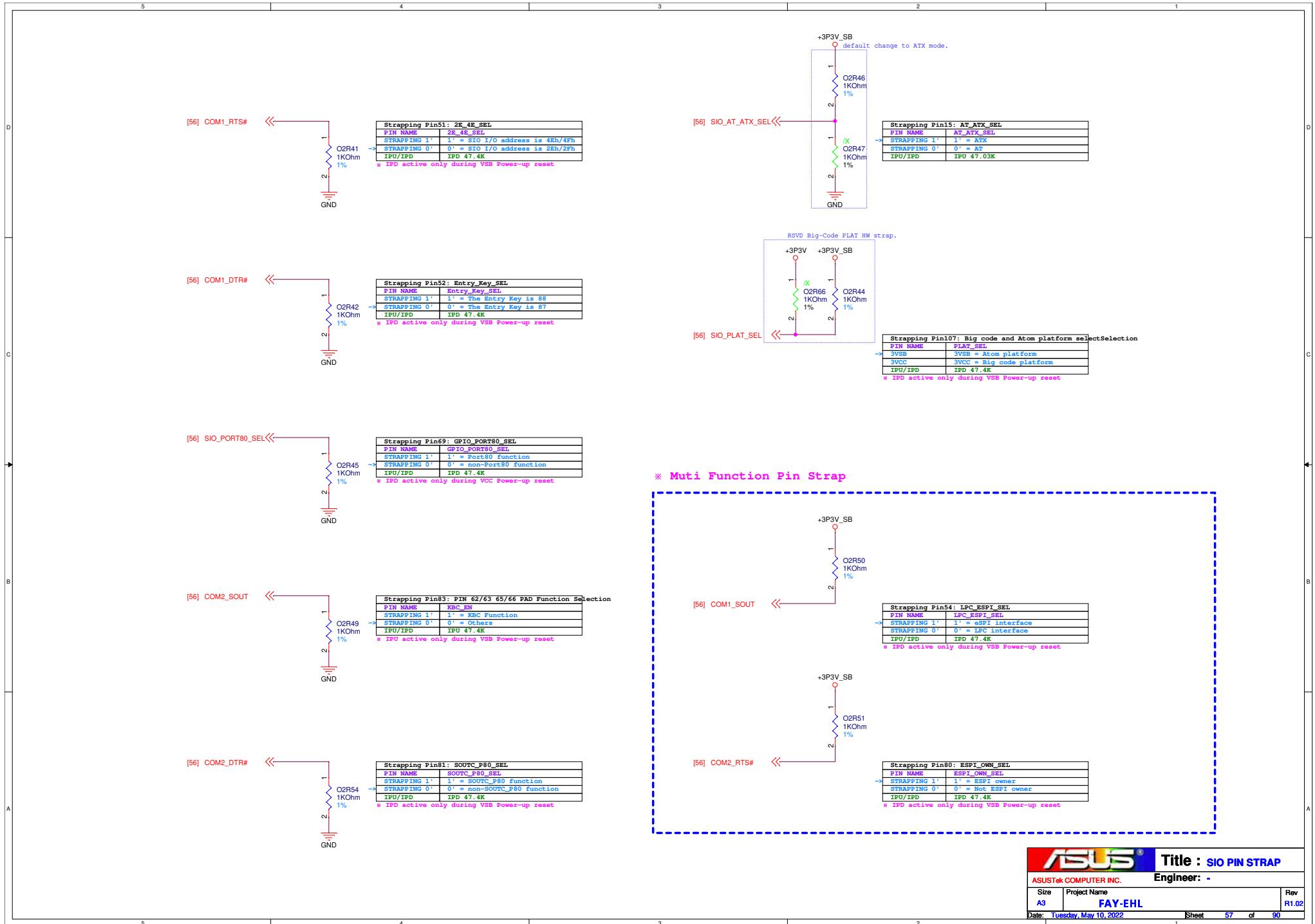
Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)	SE Gain (dB)
1	0.0 - 3.4	2.4 - 0.0	20.0	3.5
2	3.4 - 4.8	3.8 - 2.4	19.6	3.2
3	4.8 - 6.2	5.2 - 3.8	19.2	2.9
4	6.2 - 7.6	6.6 - 5.2	18.8	2.6
5	7.6 - 9.0	8.0 - 6.6	18.4	2.3
6	9.0 - 10.4	9.4 - 8.0	18.0	2.0
7	10.4 - 11.8	10.8 - 9.4	17.6	1.7
8	11.8 - 13.2	12.2 - 10.8	17.2	1.4
9	13.2 - 14.6	13.6 - 12.2	16.8	1.1
10	14.6 - 16.0	15.0 - 13.6	16.4	0.8
11	16.0 - 17.4	16.4 - 15.0	16.0	0.5
12	17.4 - 18.8	17.8 - 16.4	15.6	0.2
13	18.8 - 20.2	19.2 - 17.8	15.2	-0.2
14	20.2 - 21.6	20.6 - 19.2	14.8	-0.5
15	21.6 - 23.0	22.0 - 20.6	14.4	-0.8
16	23.0 - 24.4	23.4 - 22.0	14.0	-1.2
17	24.4 - 25.8	24.8 - 23.4	13.6	-1.5
18	25.8 - 27.2	26.2 - 24.8	13.2	-1.8
19	27.2 - 28.6	27.6 - 26.2	12.8	-2.2
20	28.6 - 30.0	29.0 - 26.6	12.4	-2.5
21	30.0 - 31.4	30.4 - 29.0	12.0	-2.9
22	31.4 - 32.8	31.8 - 30.4	11.6	-3.2
23	32.8 - 34.2	33.2 - 31.8	11.2	-3.6
24	34.2 - 35.6	34.6 - 33.2	10.8	-3.9
25	35.6 - 37.0	36.0 - 34.6	10.4	-4.3
26	37.0 - 38.4	37.4 - 36.0	10.0	-4.6
27	38.4 - 39.8	38.8 - 37.4	9.6	-5.0
28	39.8 - 41.2	40.2 - 38.8	9.2	-5.4
29	41.2 - 42.6	41.6 - 40.2	8.8	-5.7
30	42.6 - 44.0	43.0 - 41.6	8.4	-6.1
31	44.0 - 45.4	44.4 - 43.0	8.0	-6.4
32	45.4 - 46.8	45.8 - 44.4	7.6	-6.8
33	46.8 - 48.2	47.2 - 45.8	7.2	-7.2
34	48.2 - 49.6	48.6 - 47.2	6.8	-7.5



 Title : xxx	
ASUSTek COMPUTER INC. Engineer: -	
Size	Project Name
A3	FAY-EHL
Rev	R1.02
Date:	Tuesday, May 10, 2022
Sheet	54 of 90



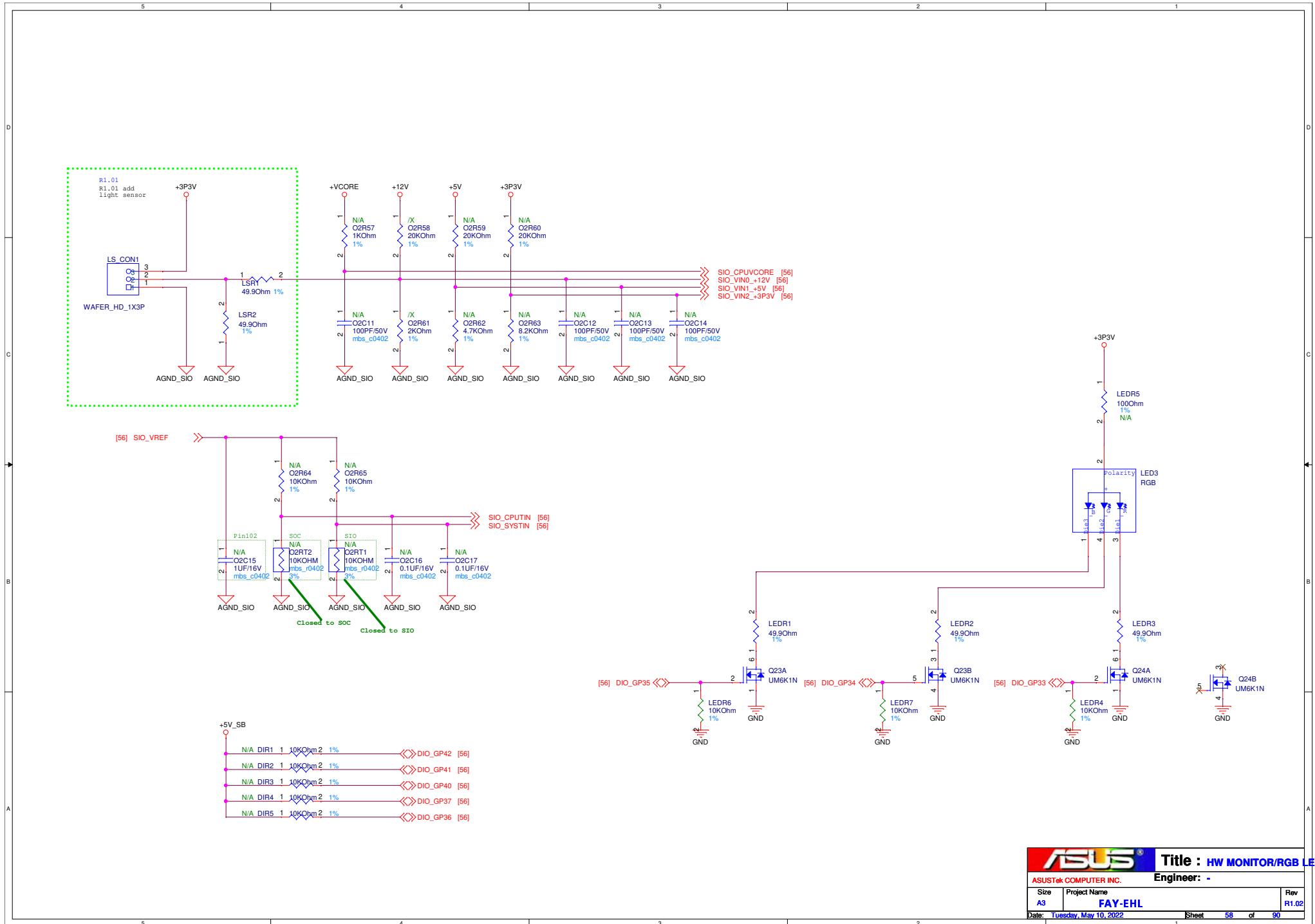




Title : SIO PIN STRAP

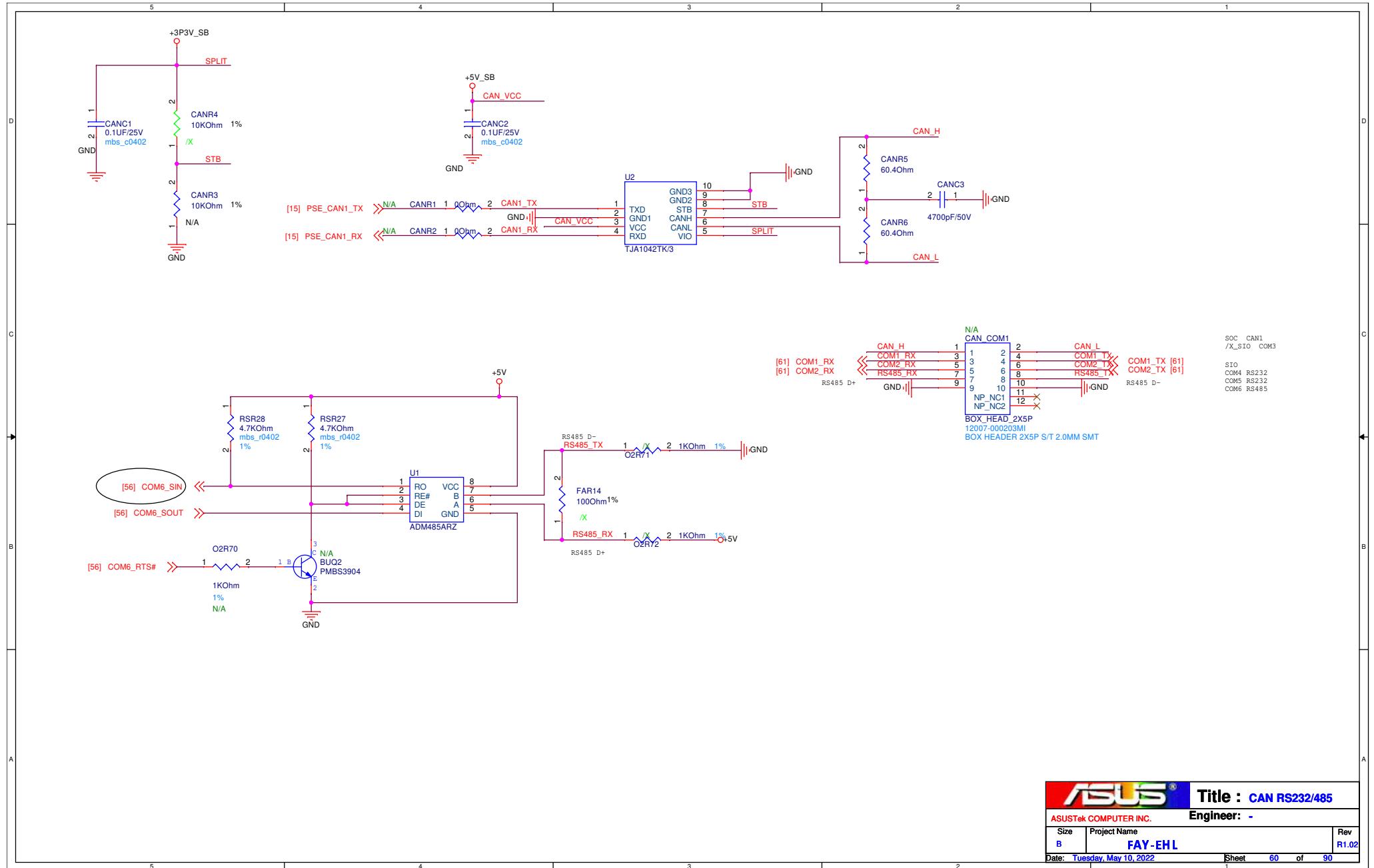
Engineer: -

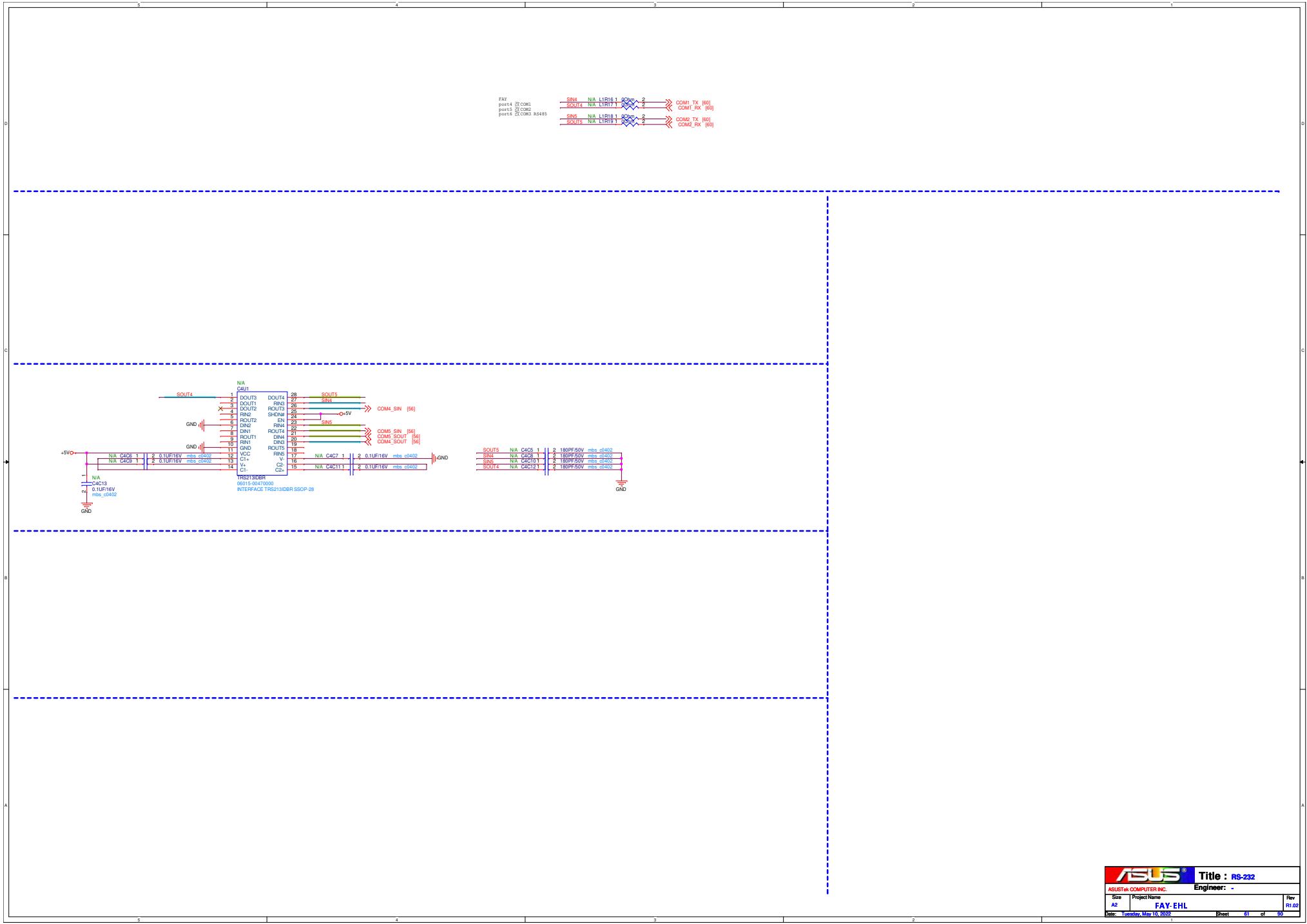
Size	Project Name	Rev
A3	FAY-EHL	R1.02
Date: Tuesday, May 10, 2022	Sheet	57 of 90



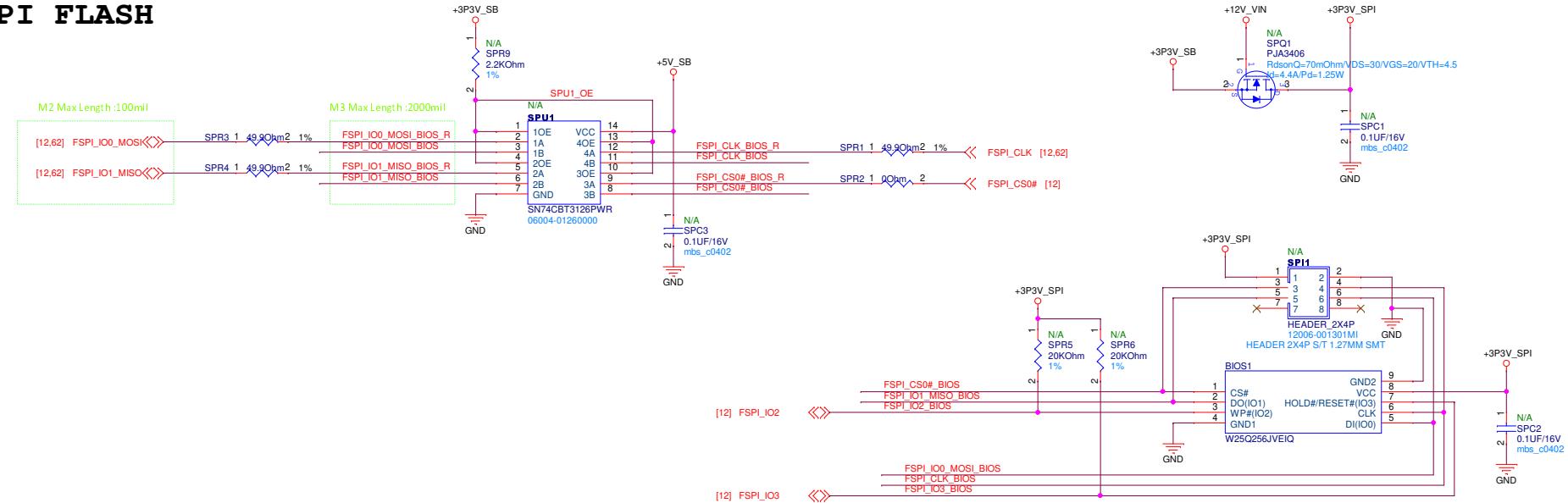


 Title : xxx
ASUSTek COMPUTER INC.
Engineer: -
Size A3 Project Name FAY-EHL Rev R1.02
Date: Tuesday, May 10, 2022 Sheet 59 of 90
1





SPI FLASH

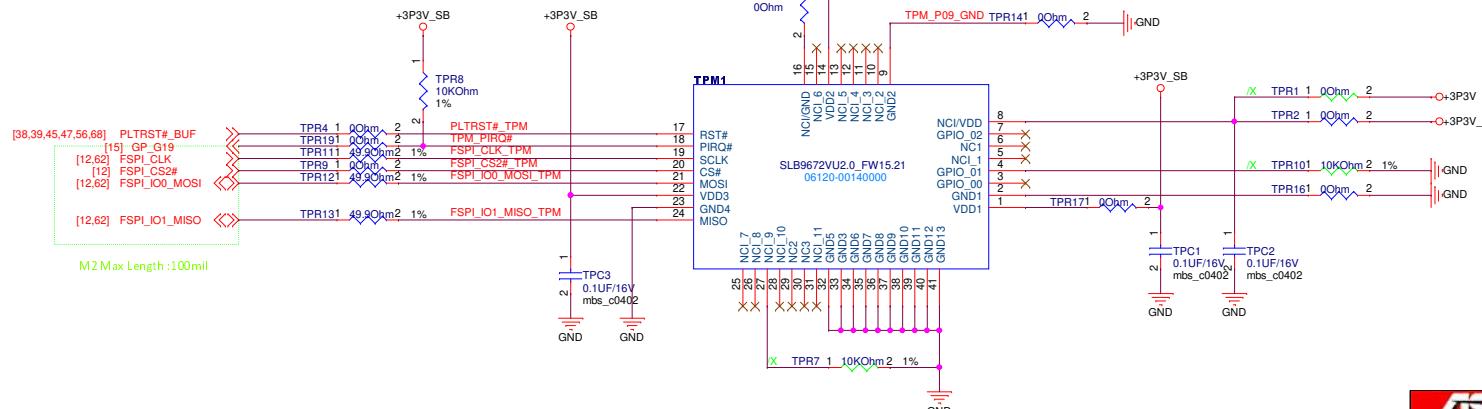


SPI TPM2.0

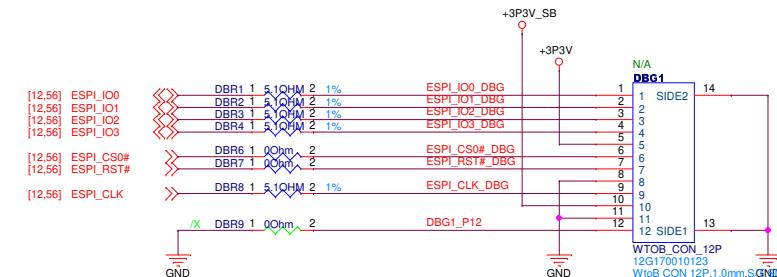
TPM2.0 SLB9672VU2.0 Co-lay /NPCT75x

06120-00010800 NPCT650ABBYX TPM2.0 F/W:1.3.1.0
06120-00080200 NPCT750AABYX TPM2.0 F/W:7.2.1.0
06120-00080400 NPCT750AABYX TPM2.0 F/W:7.2.2.0
06120-00140000 INFINEON PG-UQFN-32-1,-2 TPM SLB 9672VU2.0 FW15.21

	NPCT650	NPCT750	SLB 9672
TPR1	✓	✗	✗
TPR2	✗	✓	✗
TPR3	✓	✓	✗
TPR7	✓	✗	✗

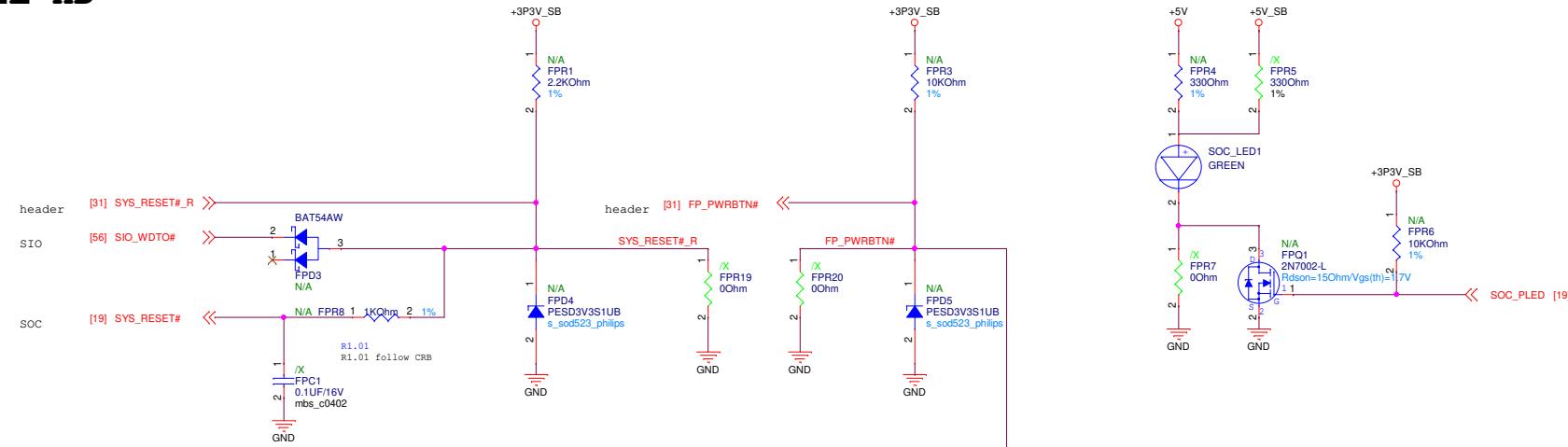


eSPI DEBUG PORT

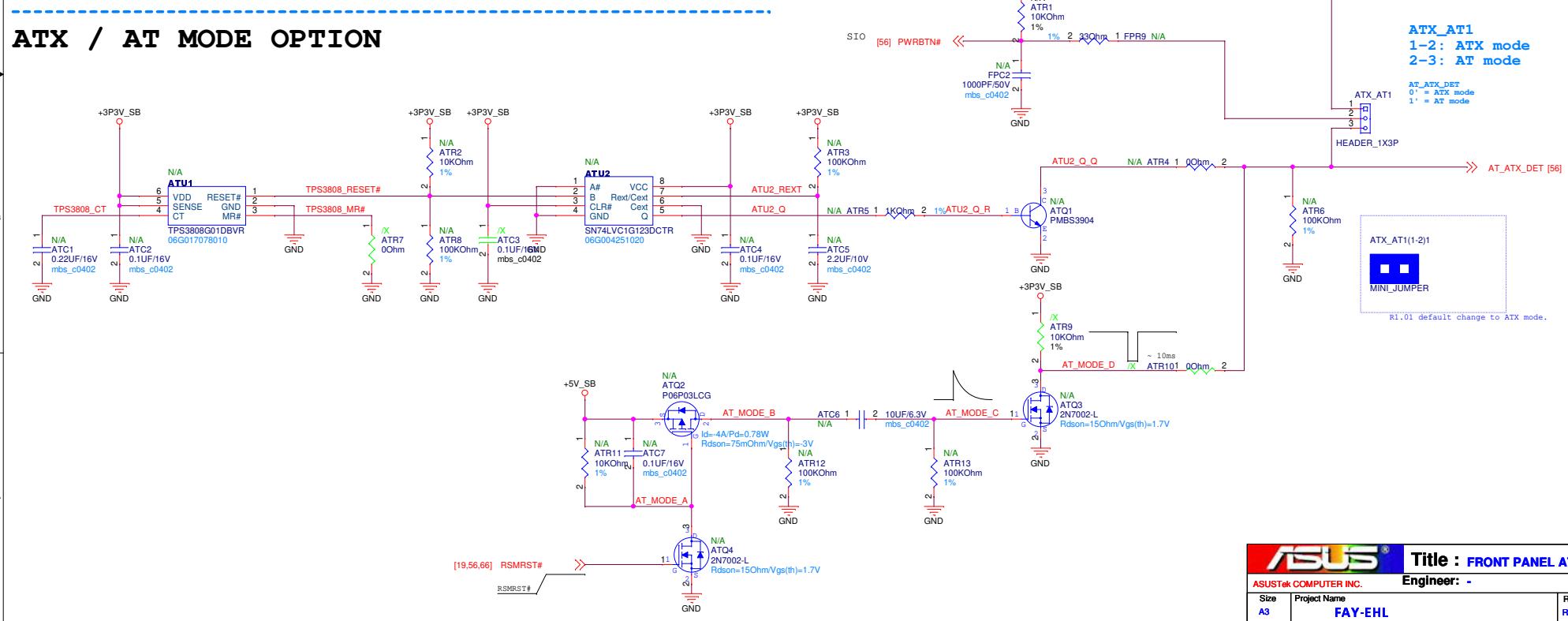


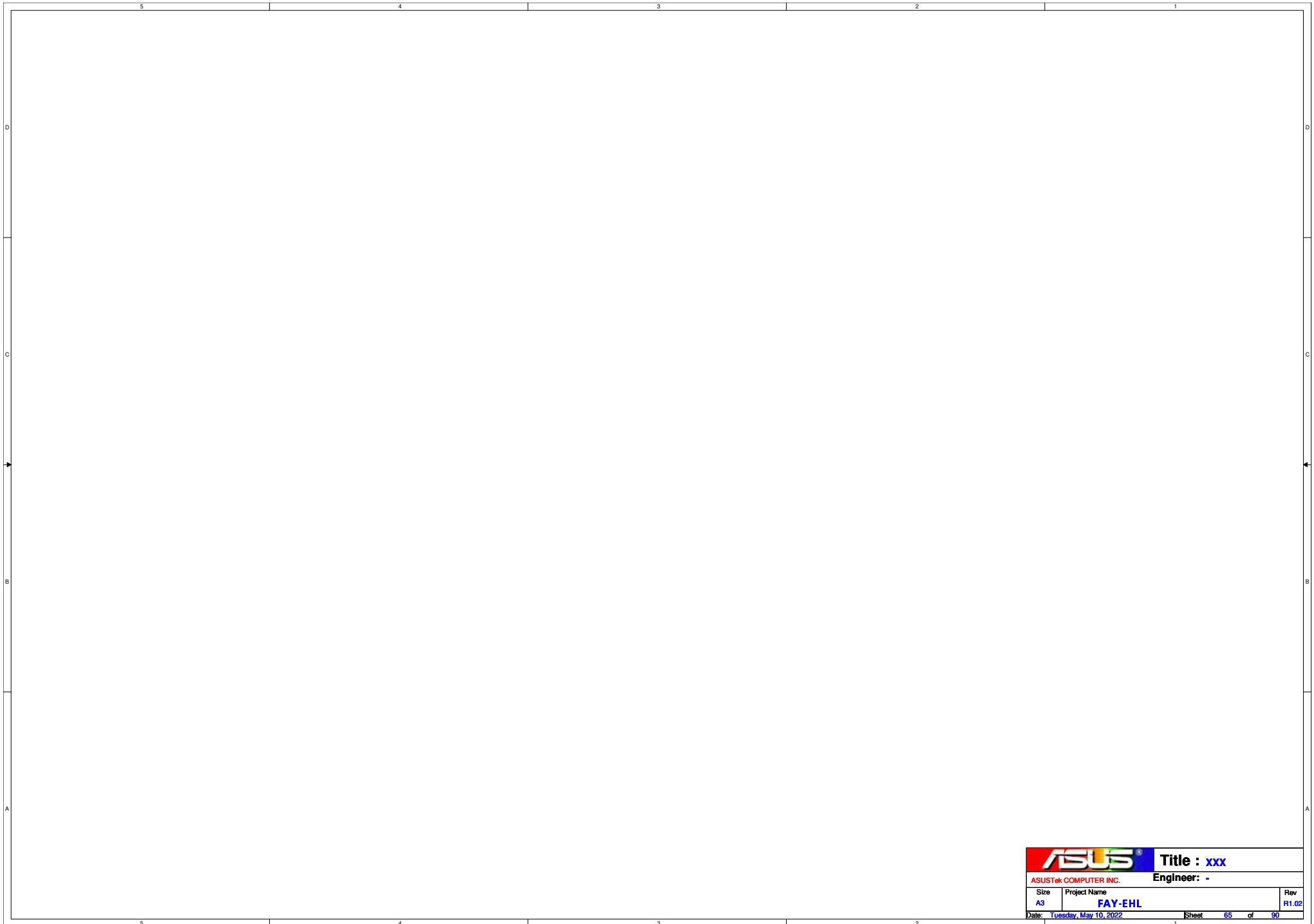
PSE DEBUG HEADER

FRONT PANEL HD



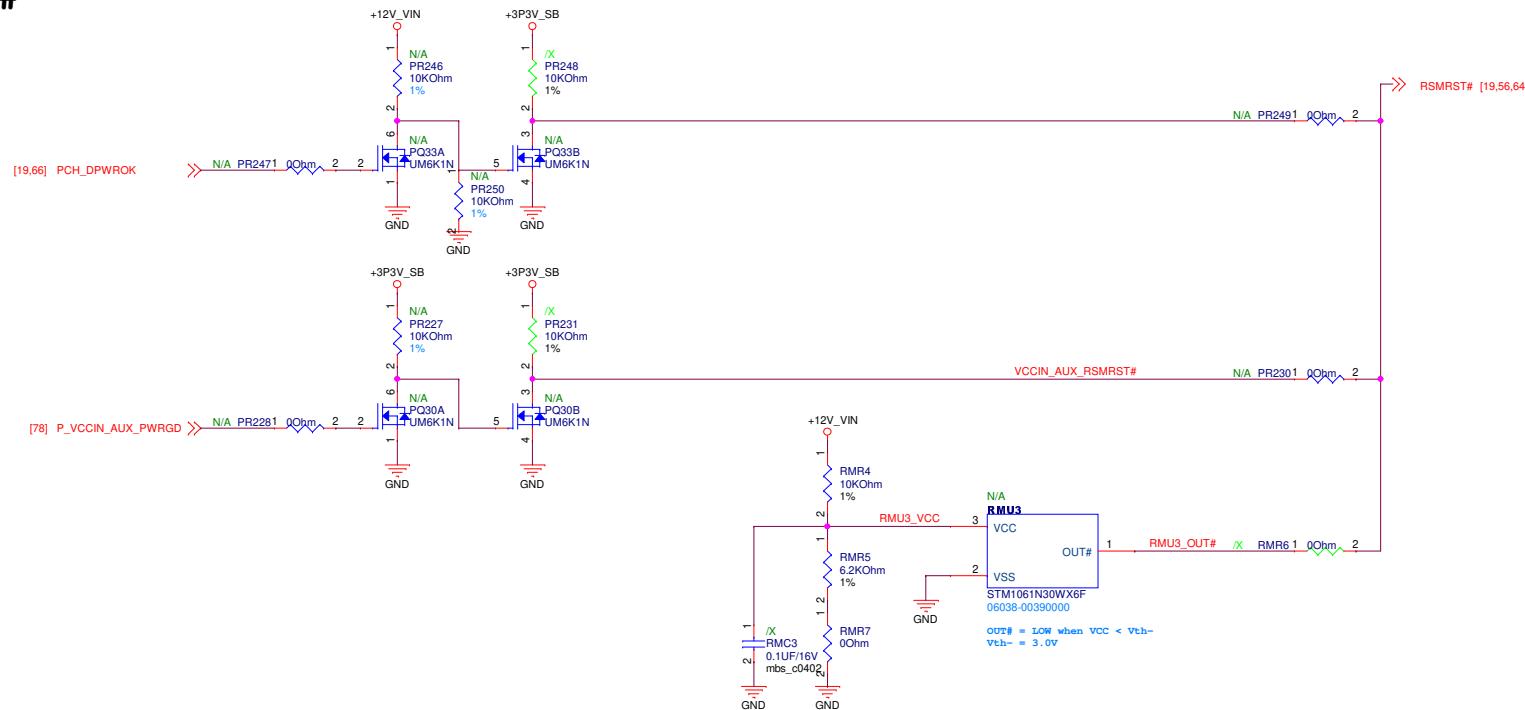
ATX / AT MODE OPTION



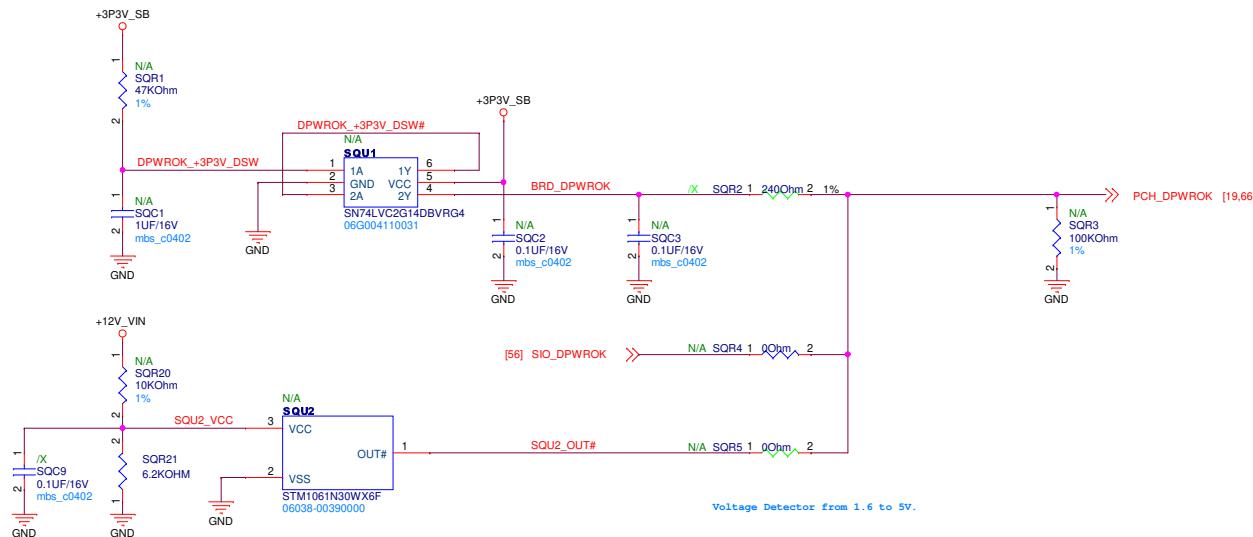


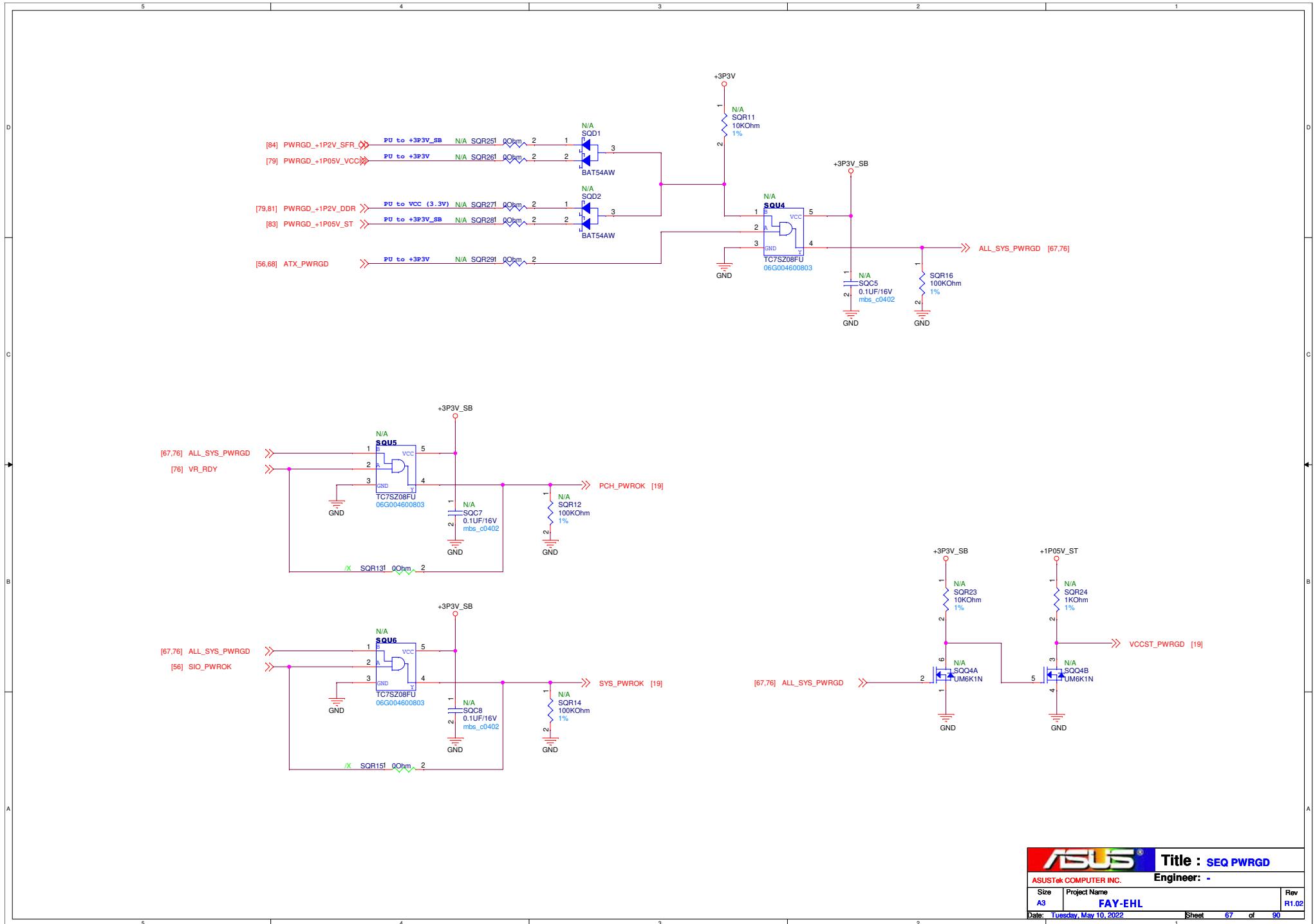
		Title : xxx	
ASUSTek COMPUTER INC.		Engineer: -	
Size	Project Name		Rev
A3	FAY-EHL		R1.02
Date: Tuesday, May 10, 2022	Sheet	65	of 90
		1	

RSMRST#

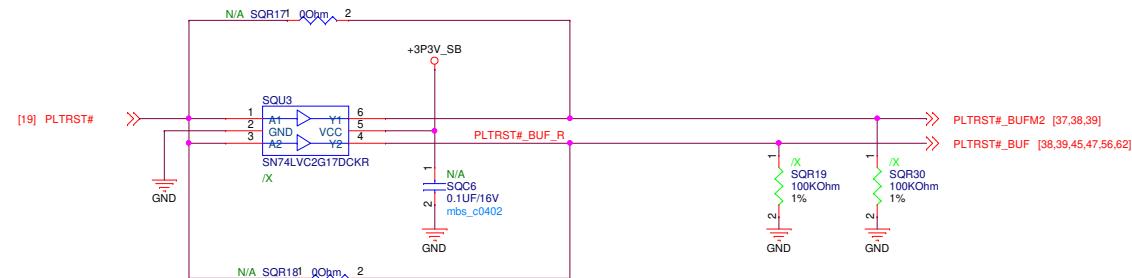


DPWROK

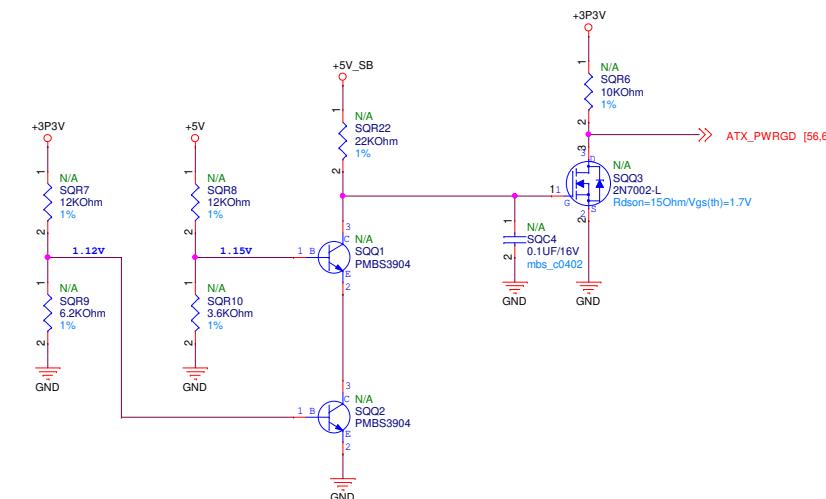


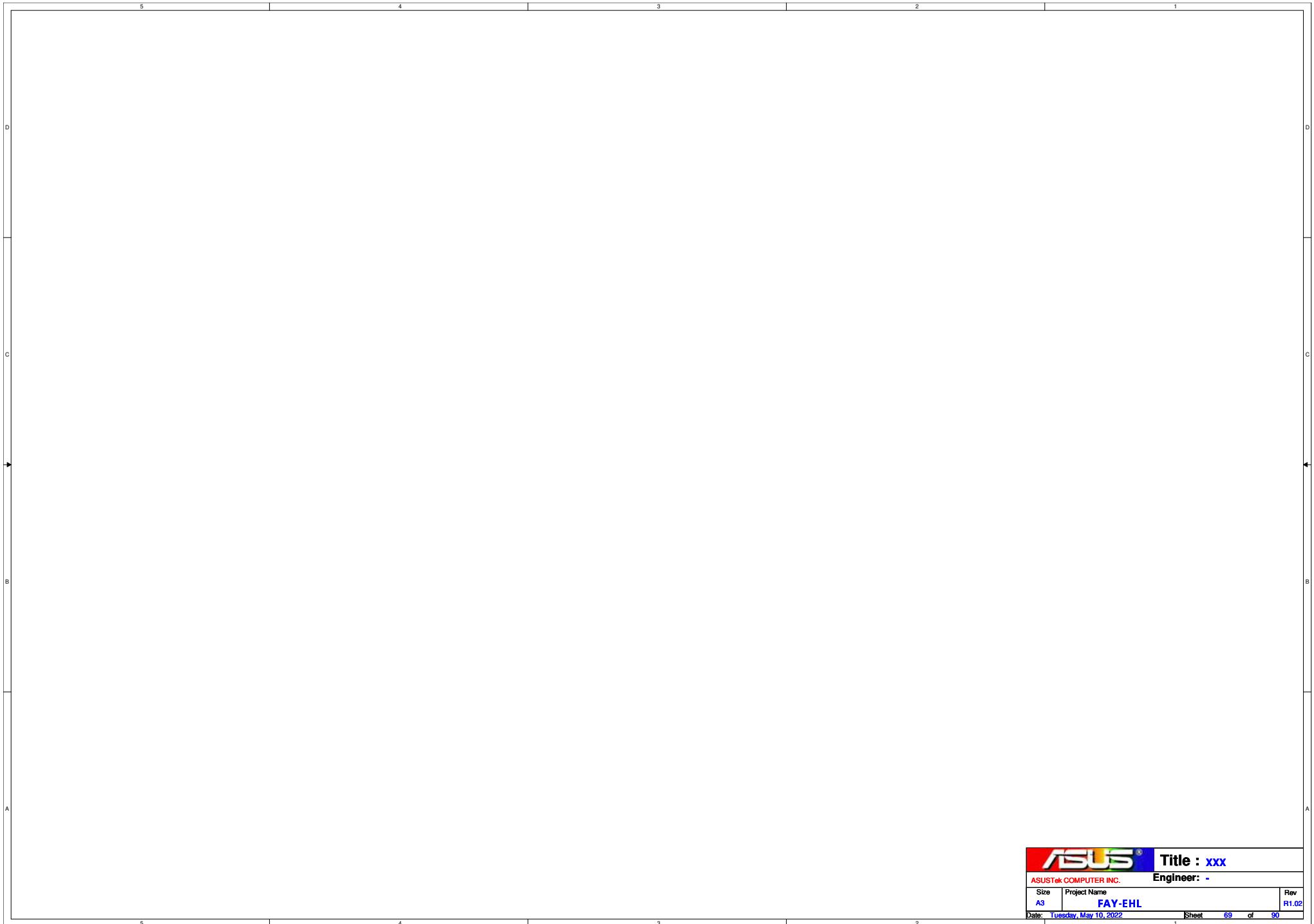


PLTRST#

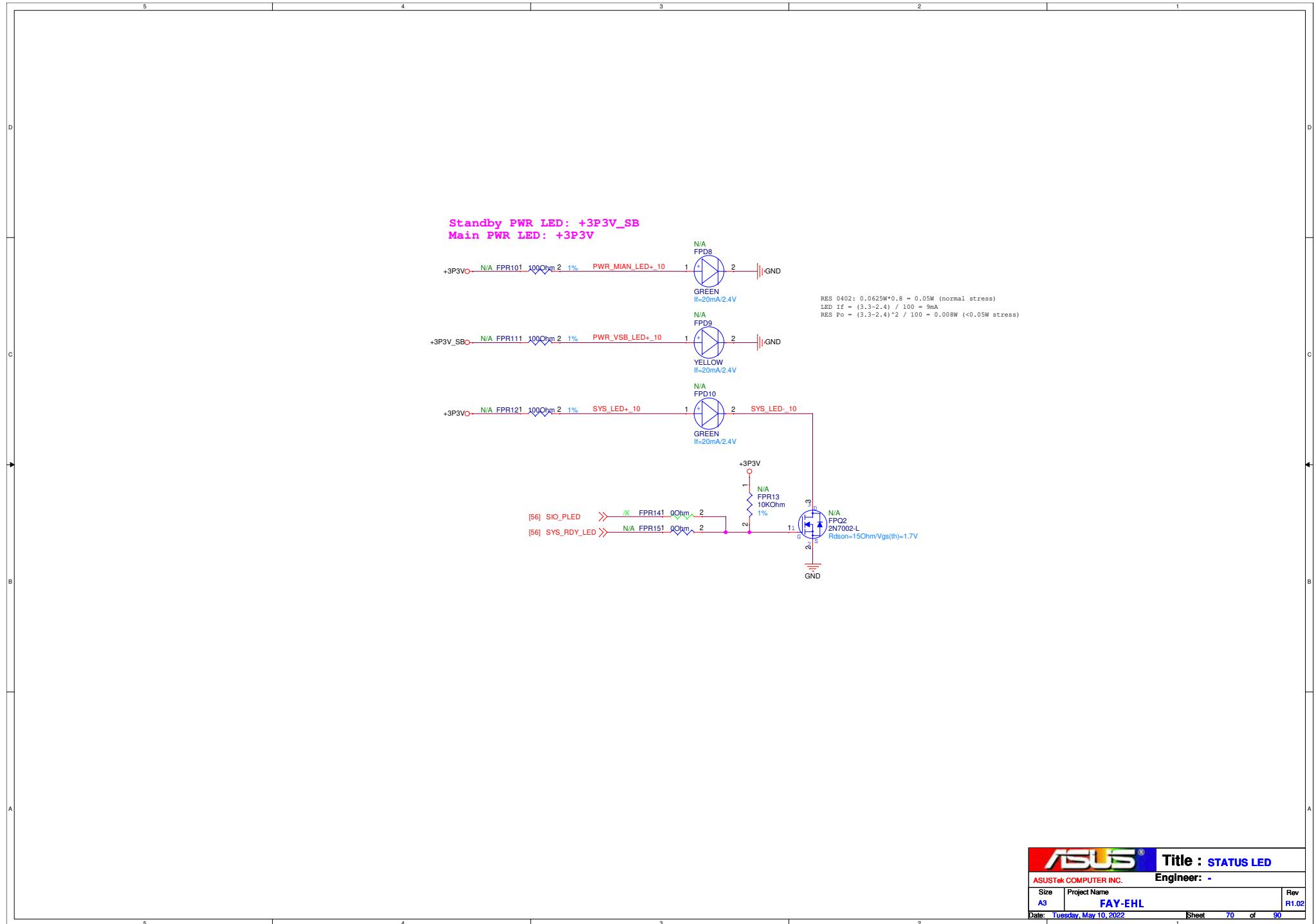


ATX_PWRGD



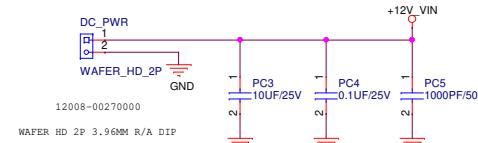


 Title : xxx	
ASUSTek COMPUTER INC.	
Engineer: -	
Size A3	Project Name FAY-EHL
	Rev R1.02
Date: Tuesday, May 10, 2022	Sheet 69 of 90
	1

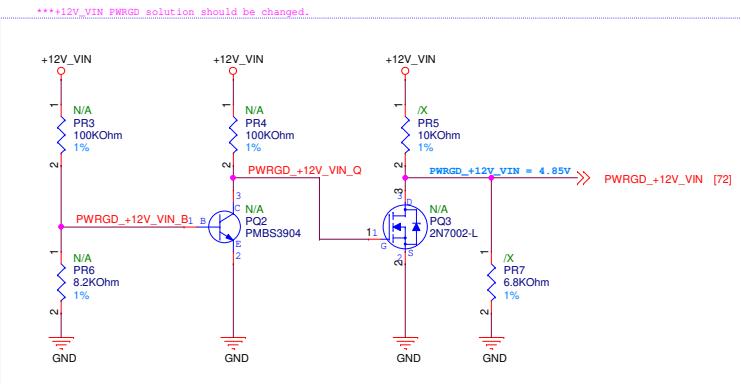


DC PWR INPUT

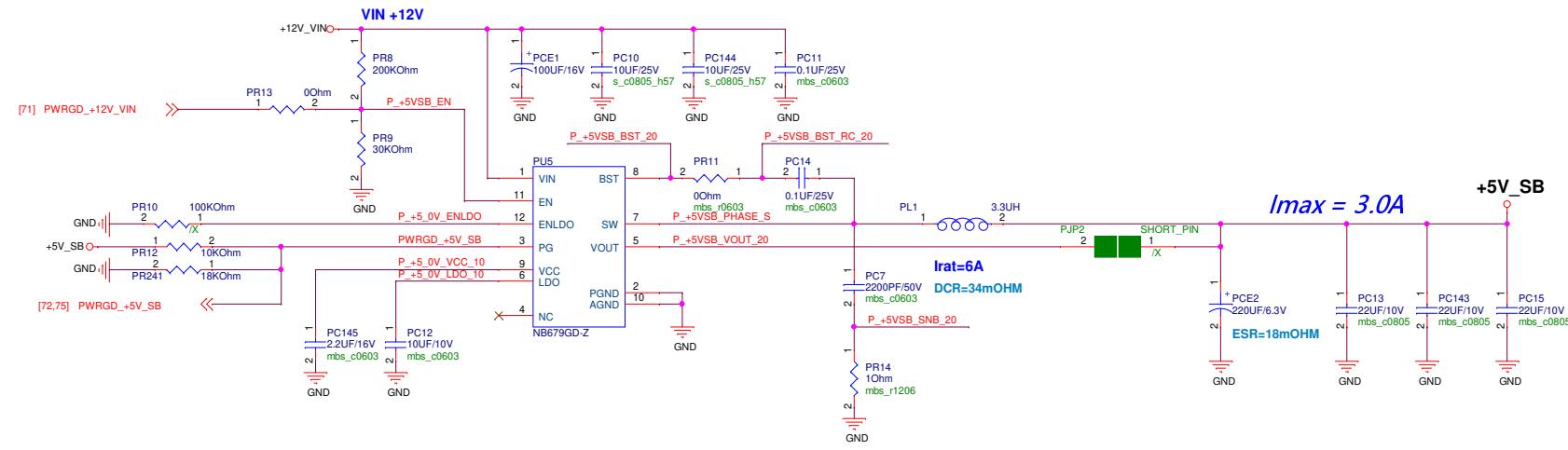
DC INPUT Connector



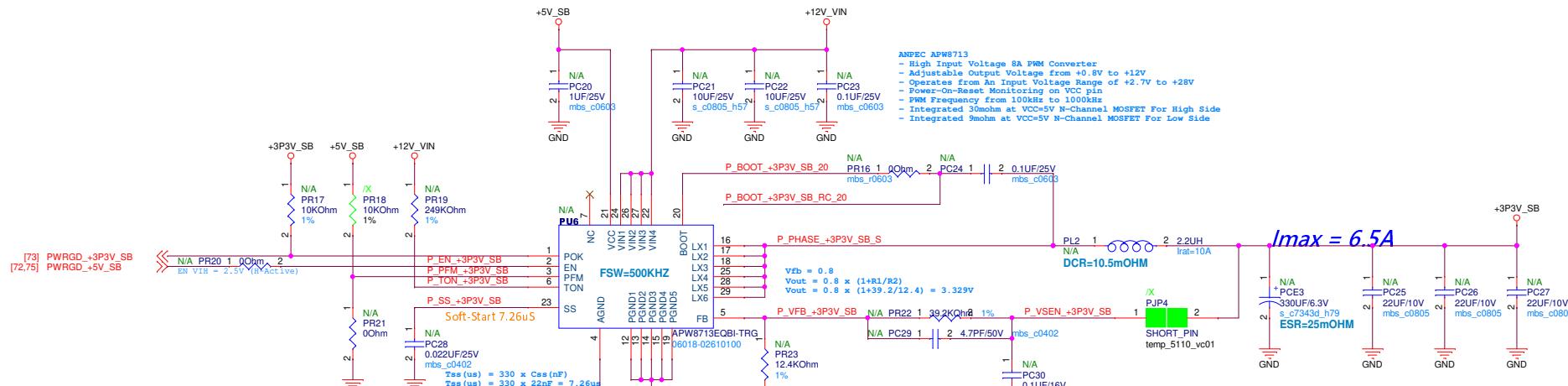
PWRGD +12V_VIN



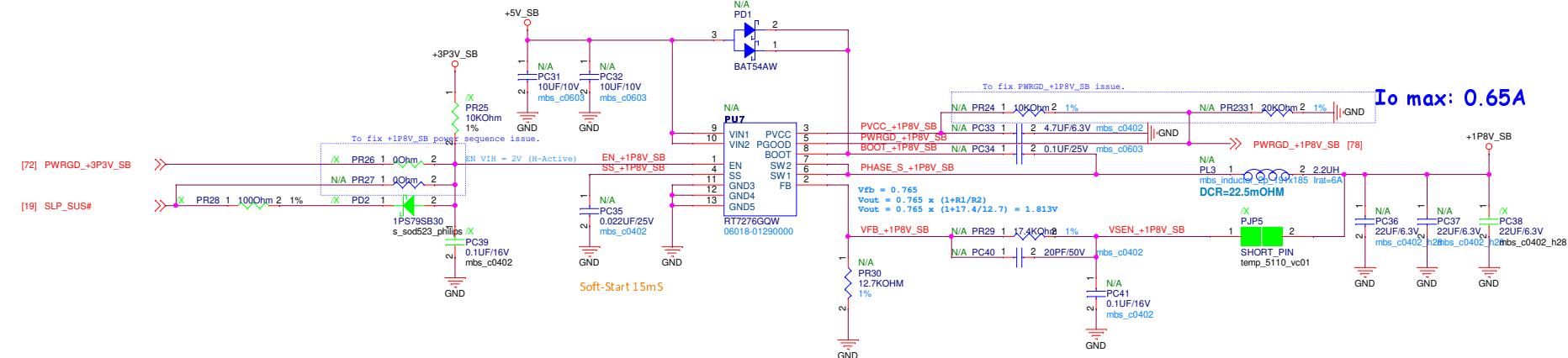
PWR +5V_SB



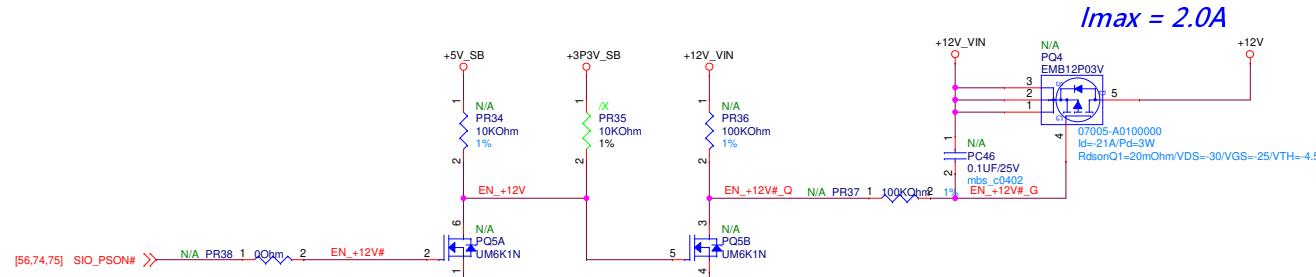
PWR +3P3V_SB



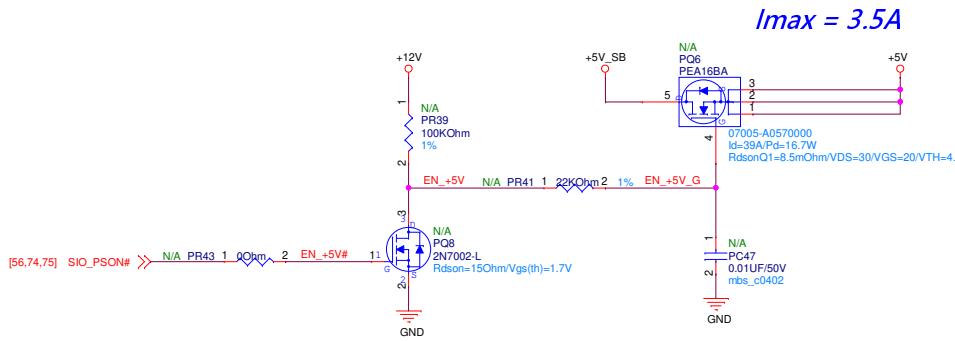
PWR +1P8V_SB



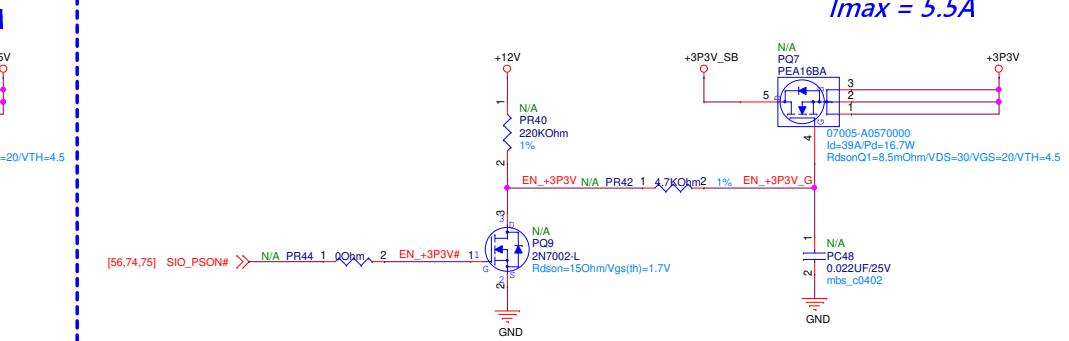
PWR +12V



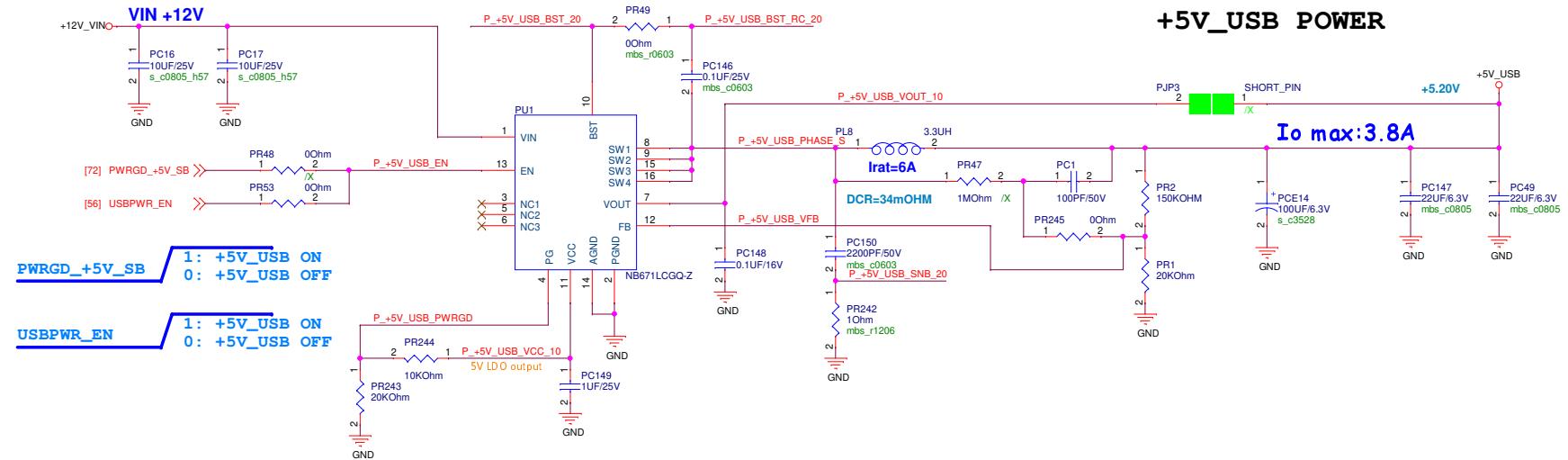
PWR +5V



PWR +3P3V

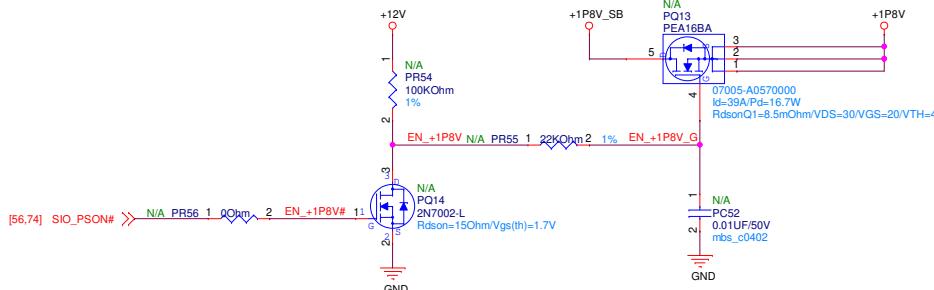


PWR +5V_USB

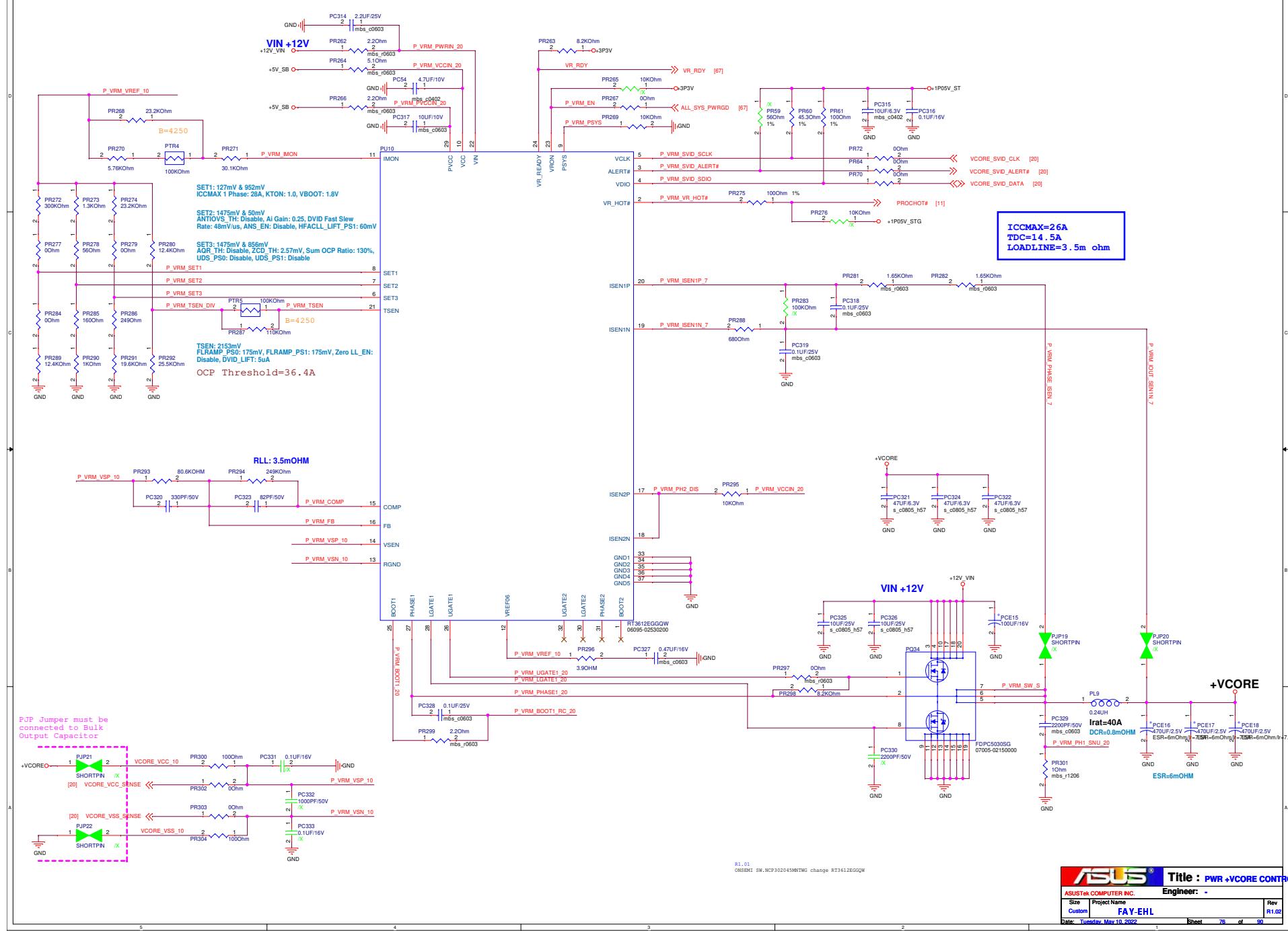


PWR +1P8V

N/A



PWR +VCORE



5 | 4 | 3 | 2 | 1 |

PWR +VCORE

D

D

C

C

B

B

A

A

		Title : PWR +VCORE	
ASUSTek COMPUTER INC.		Engineer: -	
Size	Project Name	Rev	
A3	FAY-EHL	R1.02	
Date:	Tuesday, May 10, 2022	Sheet	77 of 90

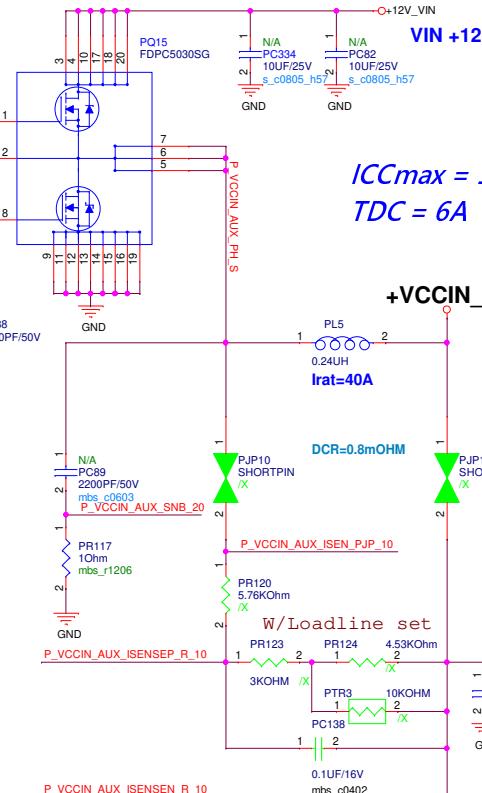
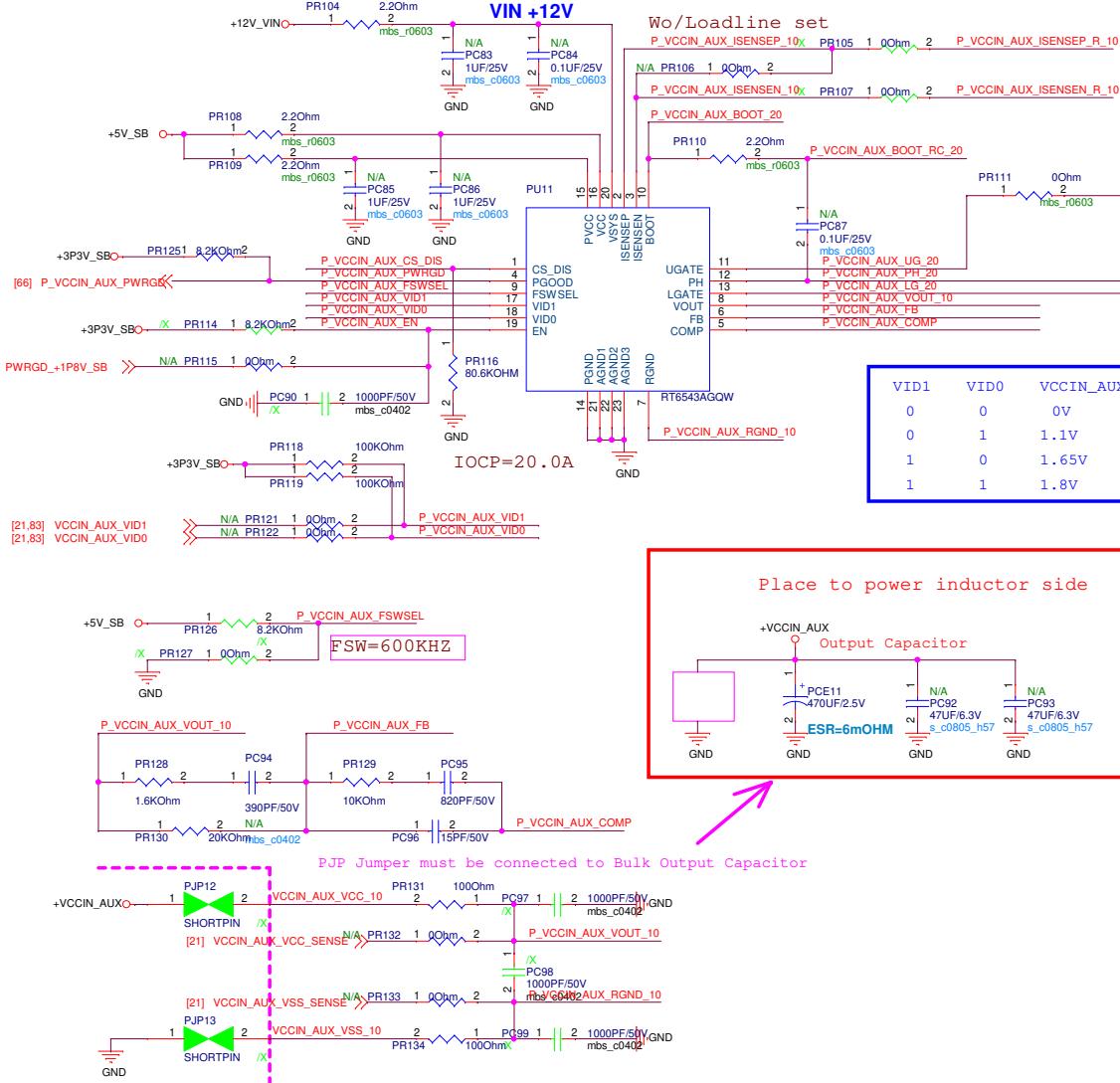
PWR +VCCIN_AUX

R1.01
PQ15 BSC0923NDI change FDPC5030SG

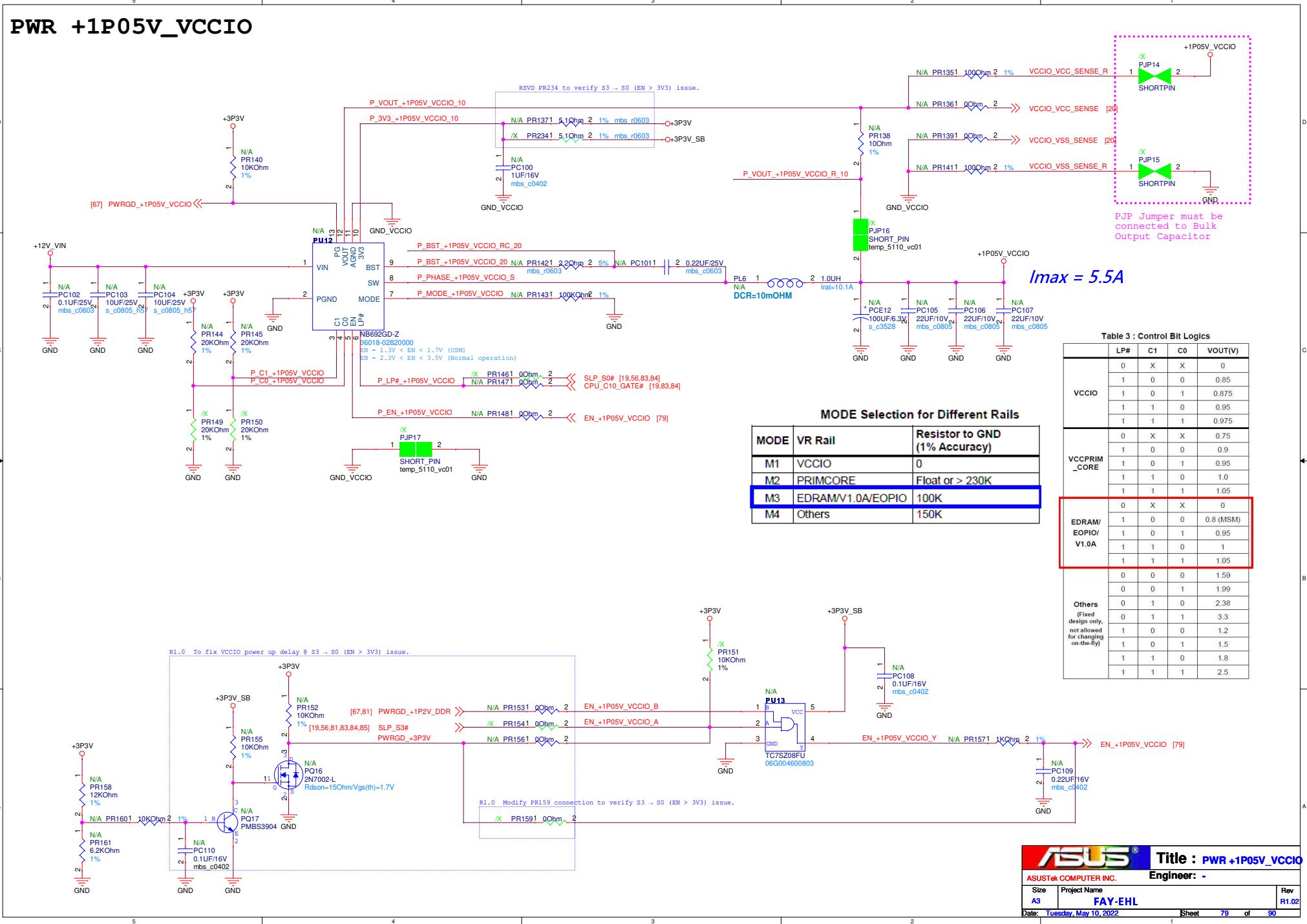
+VCCIN_AUX POWER

*ICCmax = 15A
TDC = 6A*

+VCCIN_AUX



PWR +1P05V_VCCIO



	5		4		3		2		1	
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C
A										A
B										B
N/A										
D										D
C										C

PWR +1P2V_DDR

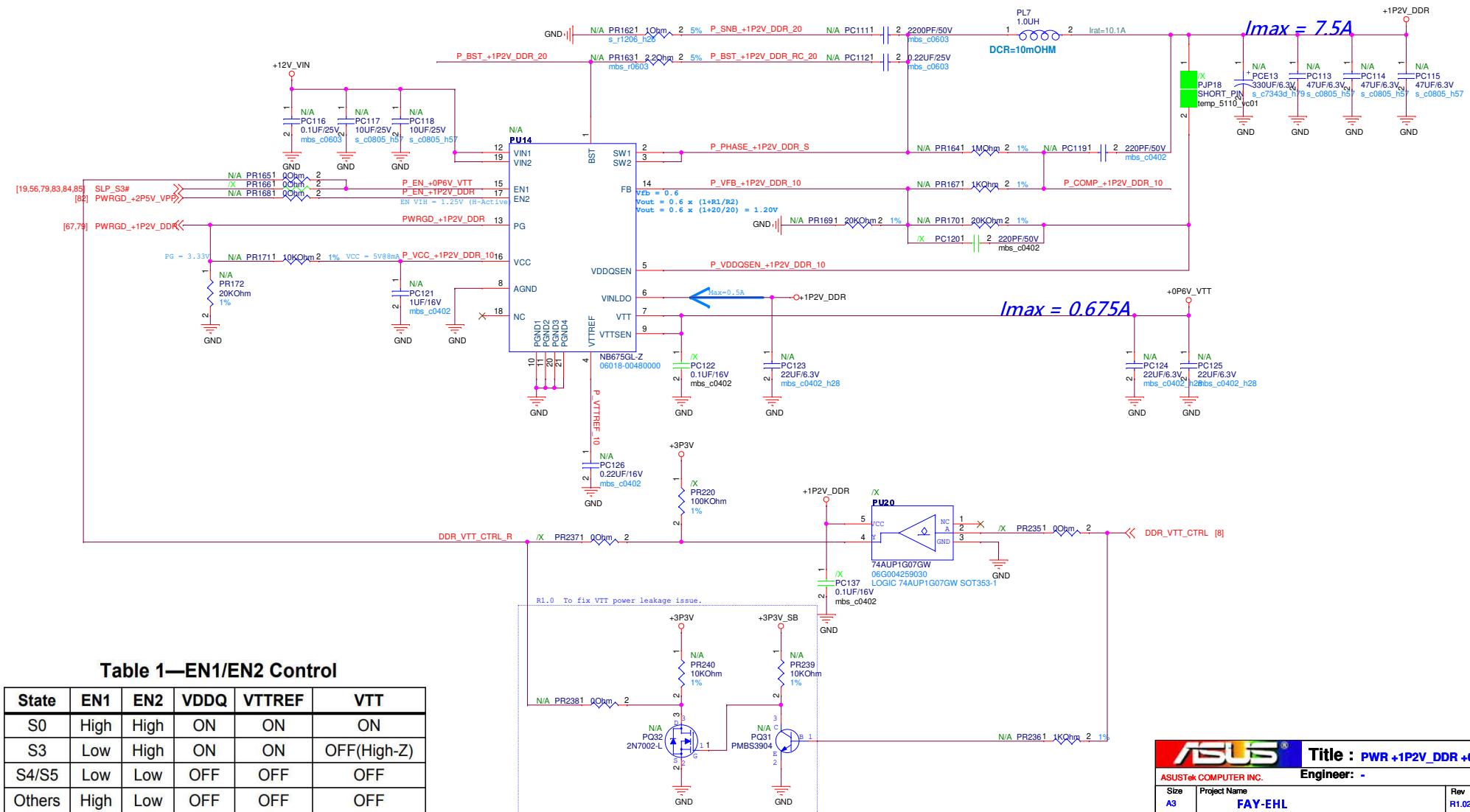
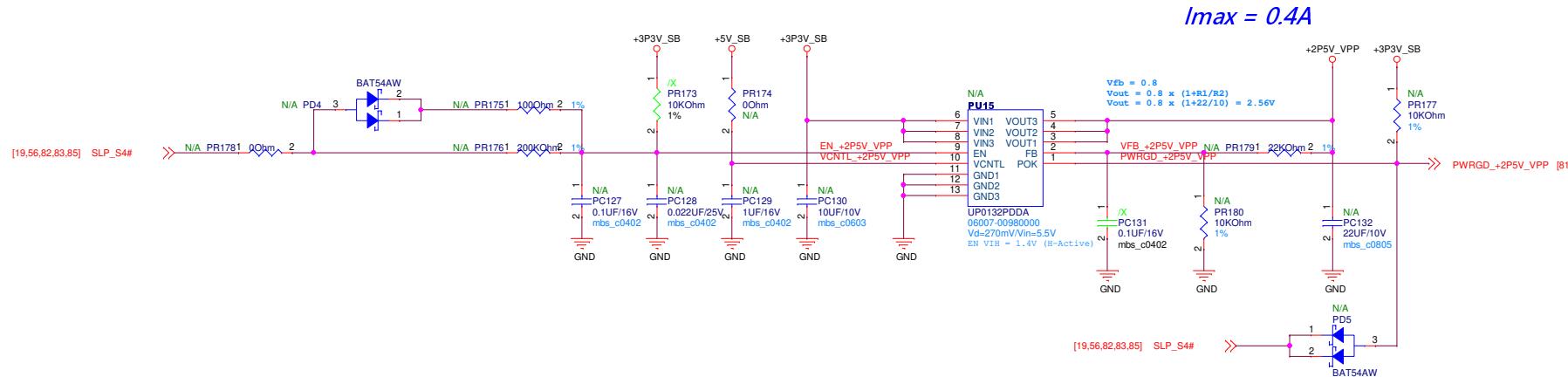


Table 1—EN1/EN2 Control

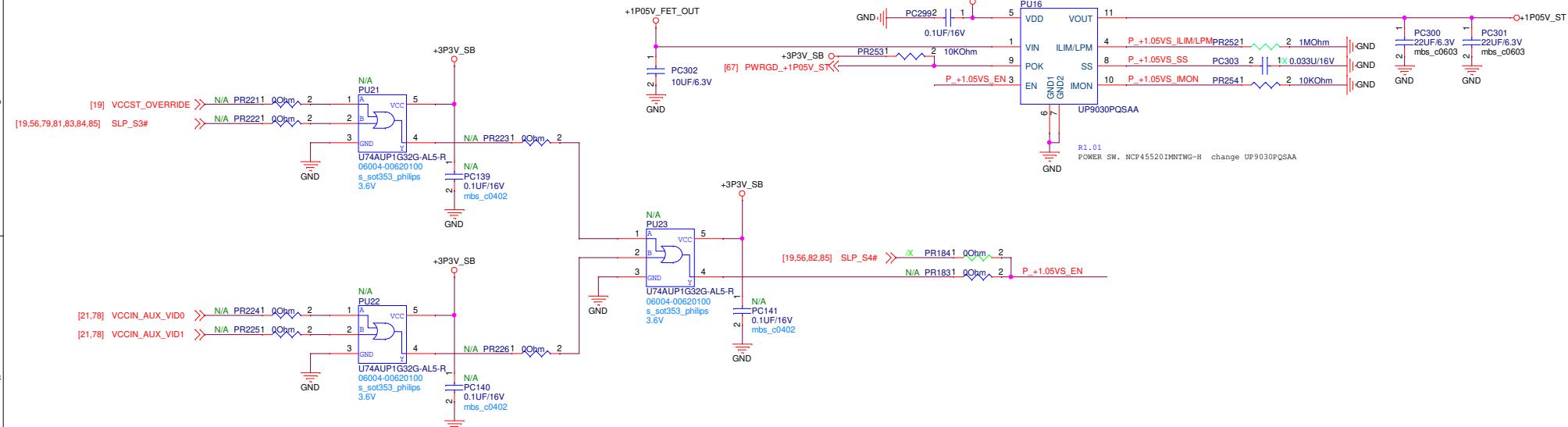
State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

PWR +2P5V_VPP



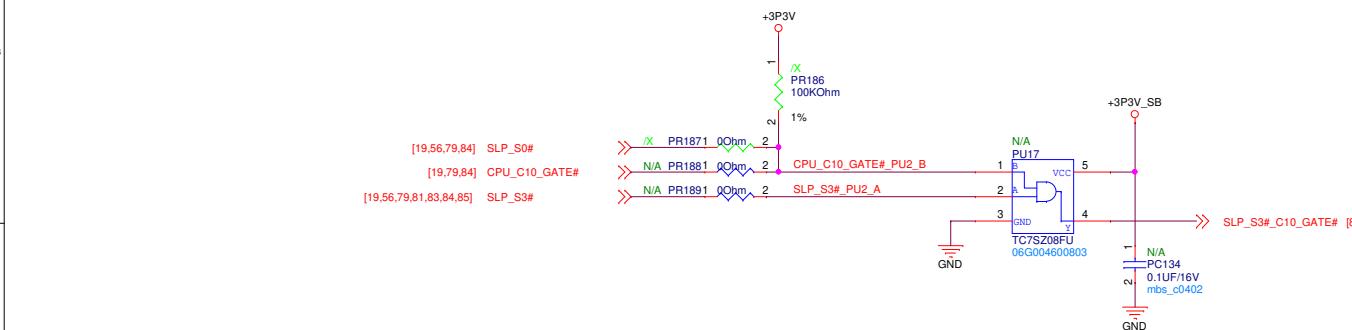
N/A

PWR +1P05V_ST

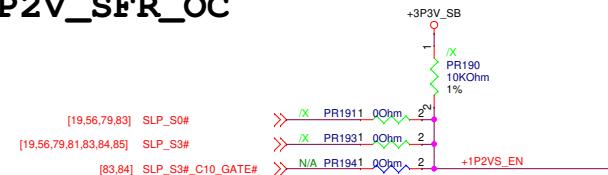


$I_{max} = 0.24A$ +VCCST_CPU

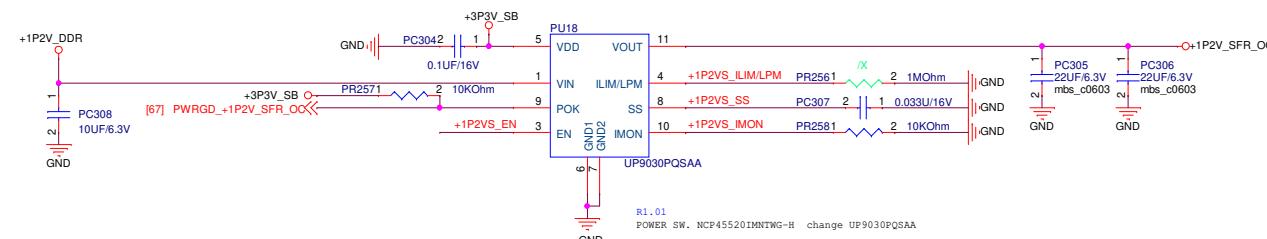
SEQ SLP_S3#_C10_GATE#



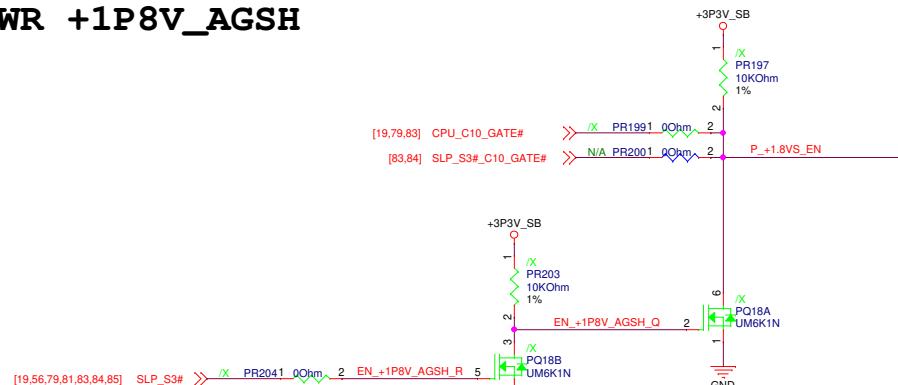
PWR +1P2V_SFR_OC



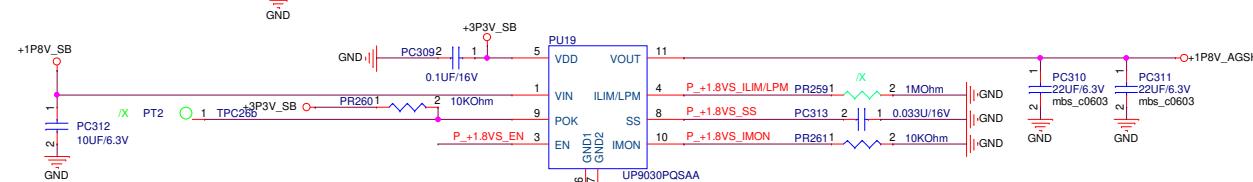
I_{max} = 0.15A +VCCSFR_OC



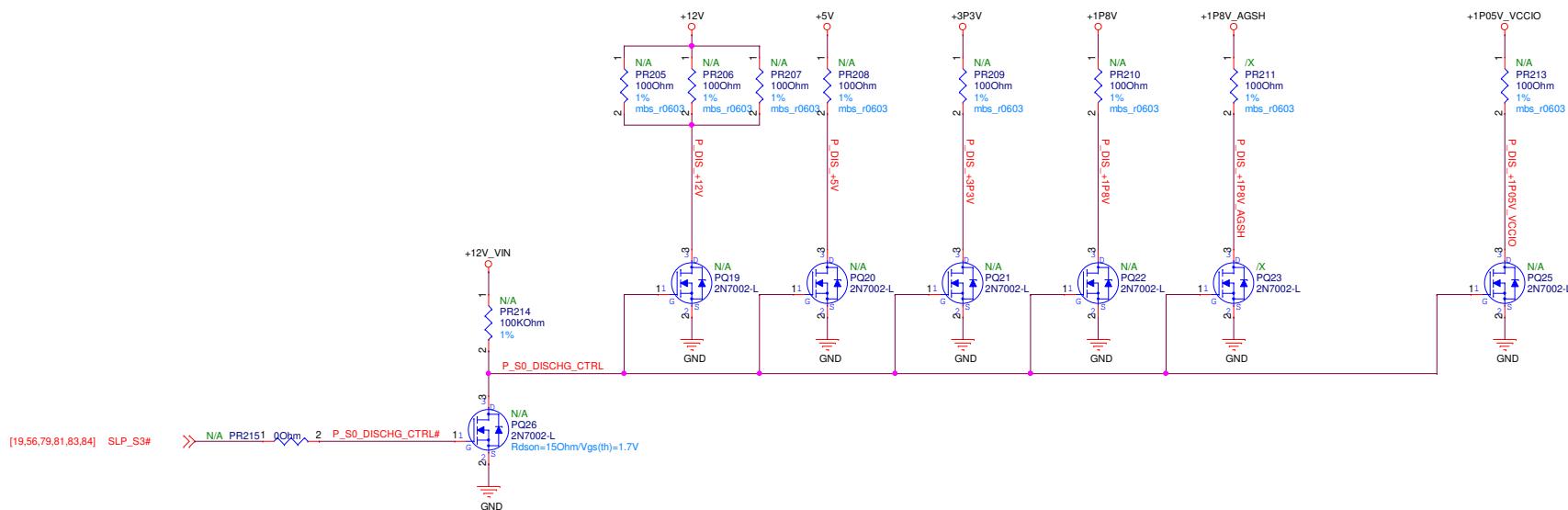
PWR +1P8V_AGSH



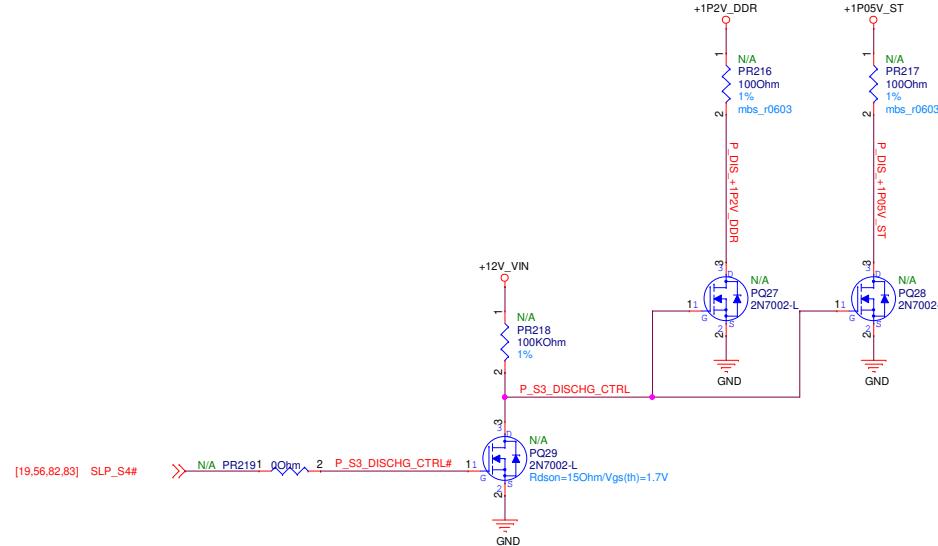
I_{max} = 0.5A +VCCAGSH_CPU



PWR S0 POWER DISCHARGE



PWR S3 POWER DISCHARGE



	5		4		3		2		1
D									D
C									C
B									B
A									A

N/A

ASUS  Title : **xxx**
ASUSTek COMPUTER INC. Engineer: -
Size Project Name Rev
A3 FAY-EHL R1.02
Date: **Tuesday, May 10, 2022** Sheet **86** of **90**

N/A

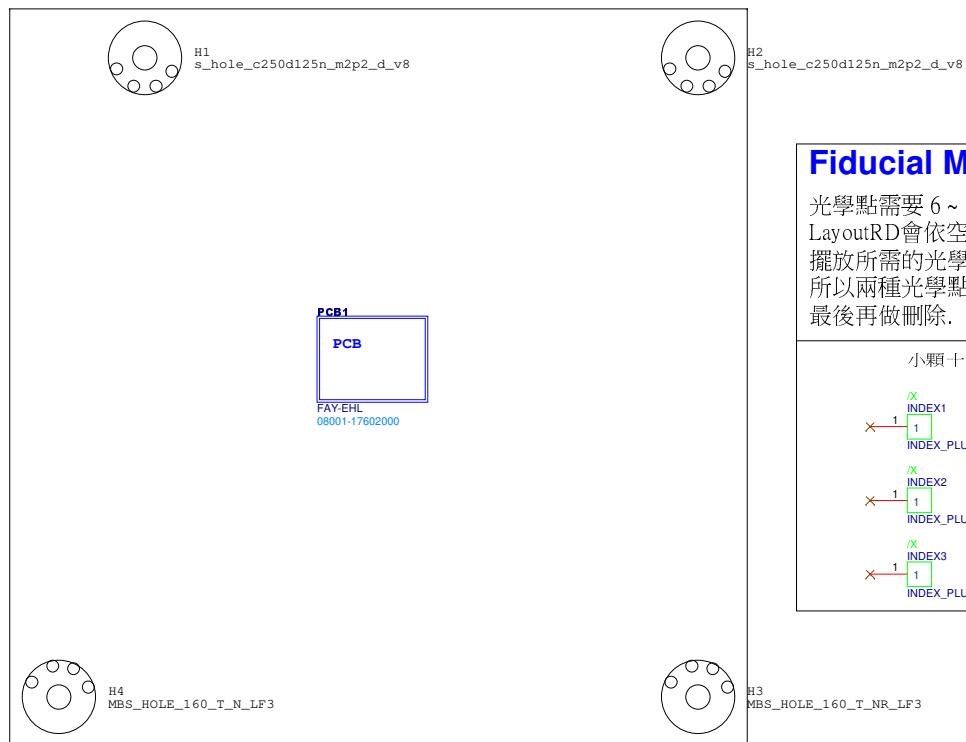
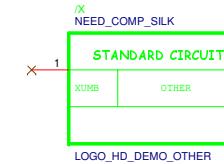
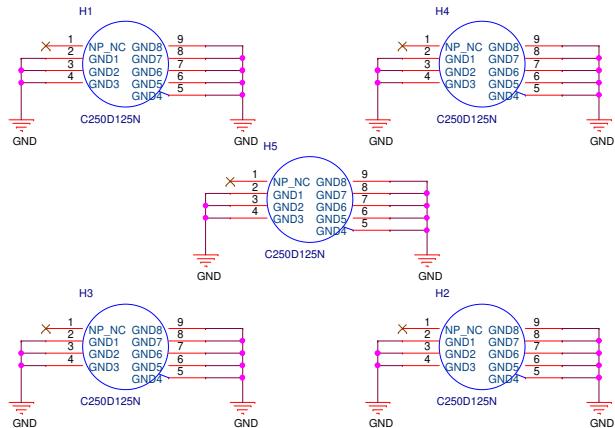


	5		4		3		2		1
D									D
C									C
B									B
A									A

N/A

ASUS  Title : **xxx**
ASUSTek COMPUTER INC. Engineer: -
Size Project Name Rev
A3 FAY-EHL R1.02
Date: **Tuesday, May 10, 2022** Sheet **88** of **90**

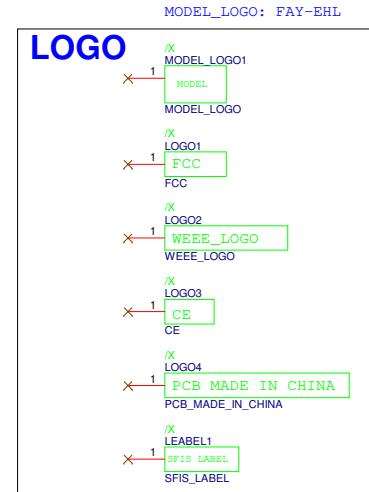
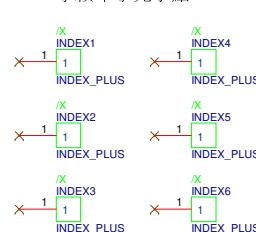
PCB & SCREW_HOLE & LOGO



Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD 會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

小顆十字光學點



Title : PCB&SCREW_HOLE&LOGO

Engineer: -

Size	Project Name	Rev
A3	FAY-EHL	R1.02

Date: Tuesday, May 10, 2022

Sheet 89 of 90

Revision History

R1.00 (First Release)

R1.01 Change List, Date: 2022/4

01. P.39 M2BR41 WAKE UP PULL HIGH
02. P.34 HDR16 change 5.6K for SI
03. P.56 Q2R39 BOM Del
04. P.62 add TPM 2.0
05. P.40 add INVERTER SIM DET
06. P.64 ATX_AT1 change default ATX mode
07. P.31 LVDS PWM change to SIO LVR67 , Remount LVDS brightness DC control
08. P.19 HR140 BOM change 100K PD
09. P.14 GBE_INT2: If not used,tied to GND through 20kOhm internal resistor.
10. P.46 RJ45 change TAB DOWN type ,POE CON change 12008-00244200
11. P.53 AMP CON1 change 12008-00244200
12. P.48 RJ45 change TAB DOWN type
13. P.31 LVDSDE CONNECTOR change 12007-00290200
14. P.58 add light sensor connector
15. P.83 Change PU16,PU18,PU19 NCP45520IMNTWG-H to UP9030 to solve sortage issue.
16. P.76 change PU10 to RT3612E
17. P.78 PQ15 change FDPC5030SG
18. AZC099-04SP.R7G change AZC399-04S.R7G
19. P.25 del HC114,HC103,HC77
20. 21.
21. 22.
22. 23.
23. 24.
24. 25.
- 25.

R1.02 Change List, Date: 2022/5

P.31 U48, U49 VCC change +3P3V add LVQ7A

Title : REVISION HISTORY		
ASUSTek COMPUTER INC. Engineer: -		
Size	Project Name	Rev
A3	FAY-EHL	R1.02
Date: Tuesday, May 10, 2022	Sheet	90 of 90