

NCT5582D
Nuvoton LPC/eSPI SI/O

Date: December 10th, 2018 Revision 1.1

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1. GENERAL DESCRIPTION

The NCT5582D is a member of Nuvoton's Super I/O product line. The NCT5582D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT5582D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT5582D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT5582D provides one high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT5582D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT5582D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT5582D supports the Intel® PECI (Platform Environment Control Interface), Advanced Power Saving function to further reduce the power consumption while the system is at S5 state, two-color LED control to indicate system power states, decode port 80 diagnostic messages on the LPC / eSPI bus to help system power on debugging and Consumer IR function for remote control purpose.

The configuration registers inside the NCT5582D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

- Meet LPC Specification 1.1
- Meet eSPI Specification
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Support selective pins of 5 V tolerance

UART

One high-speed, 16550-compatible UART with 16-byte send / receive FIFO

Support RS485

- Supports auto flow control

Fully programmable serial-interface characteristics:

- 5, 6, 7 or 8-bit characters
- Even, odd or no parity bit generation / detection
- 1, 1.5 or 2 stop-bit generation

Internal diagnostic capabilities:

- Loop-back controls for communications link fault isolation
- Break, parity, overrun, framing error simulation

Programmable baud rate generator allows division of clock source by any value from 1 to $(2^{16}-1)$

Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Keyboard Controller

8042-based keyboard controller

Asynchronous access to two data registers and one status register

Software-compatible with 8042

Support PS/2 mouse

Support Port 92

Support both interrupt and polling modes

Fast Gate A20 and Hardware Keyboard Reset

12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system

Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal CruiseTM mode

Support Current Mode (dual current source) temperature sensing method

Nine voltage inputs (CPUVCORE, VIN0, VIN1, VIN9, 3VCC, AVSB, 3VSB, VTT and VBAT)

Four fan-speed monitoring inputs

Four fan-speed controls

Dual mode for fan control (PWM and DC) for SYSFANOUT
Built-in case-open and CPU socket occupied detection circuit
Programmable hysteresis and setting points for all monitored items
Issue SMI#, OVT# (Over-temperature) to activate system protection
Nuvoton Health Manager support
Provide I²C master / slave interface to read / write registers

CIR and IR (Infrared)

Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
Support Consumer IR, including CIRRX

General Purpose I/O Ports

GPIO0 ~ GPIO8 programmable general purpose I/O ports
Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions
Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys
Mouse Wake-Up by programmable buttons
OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification
Support 2 CPU addresses and 2 domains per CPU address

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Fading LED driver control for power status and diagnostic indications

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

3.3 voltage

Package

64-pin LQFP

Green

3. BLOCK DIAGRAM

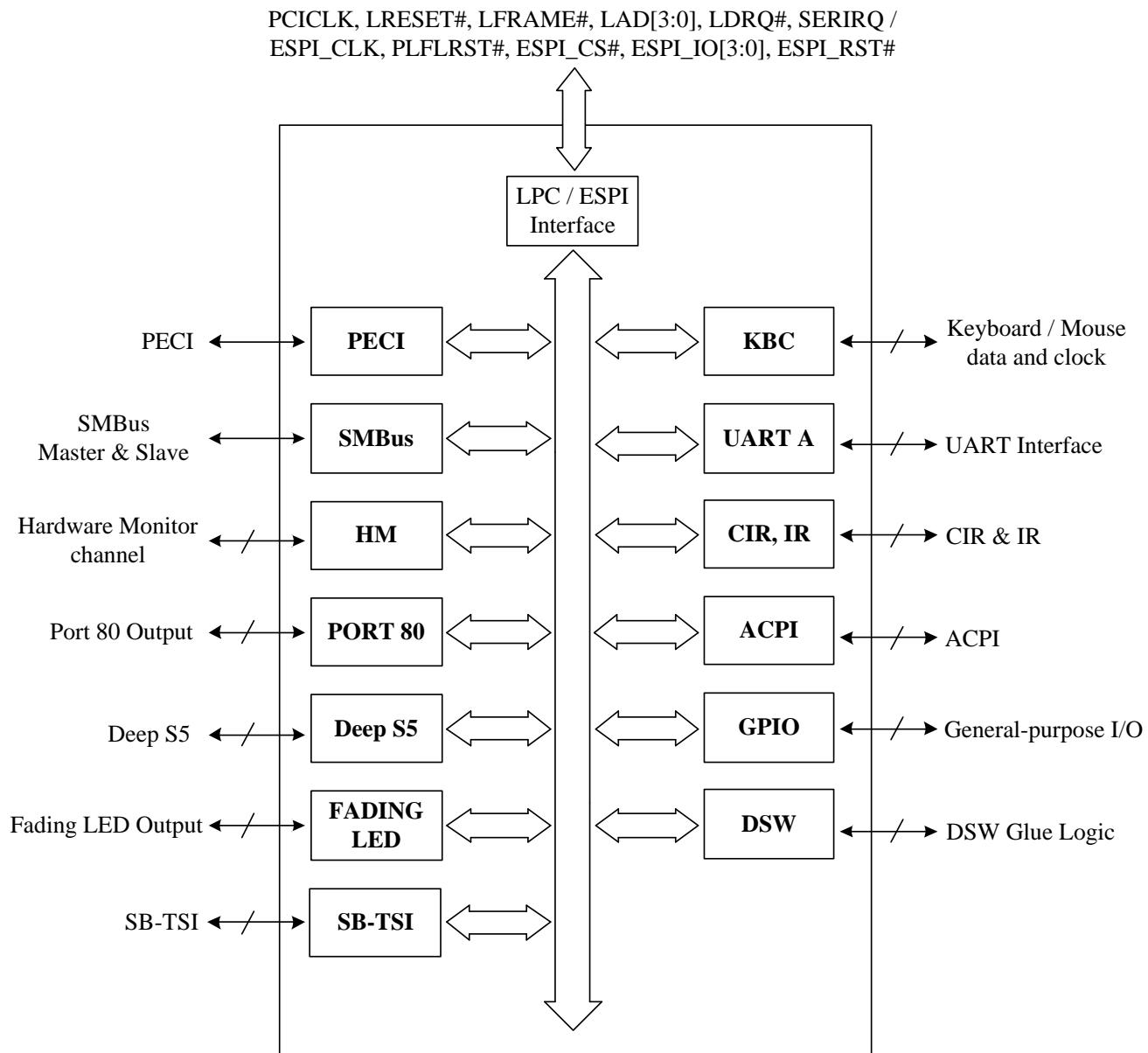


Figure 3-1 NCT5582D Block Diagram

4. PIN LAYOUT

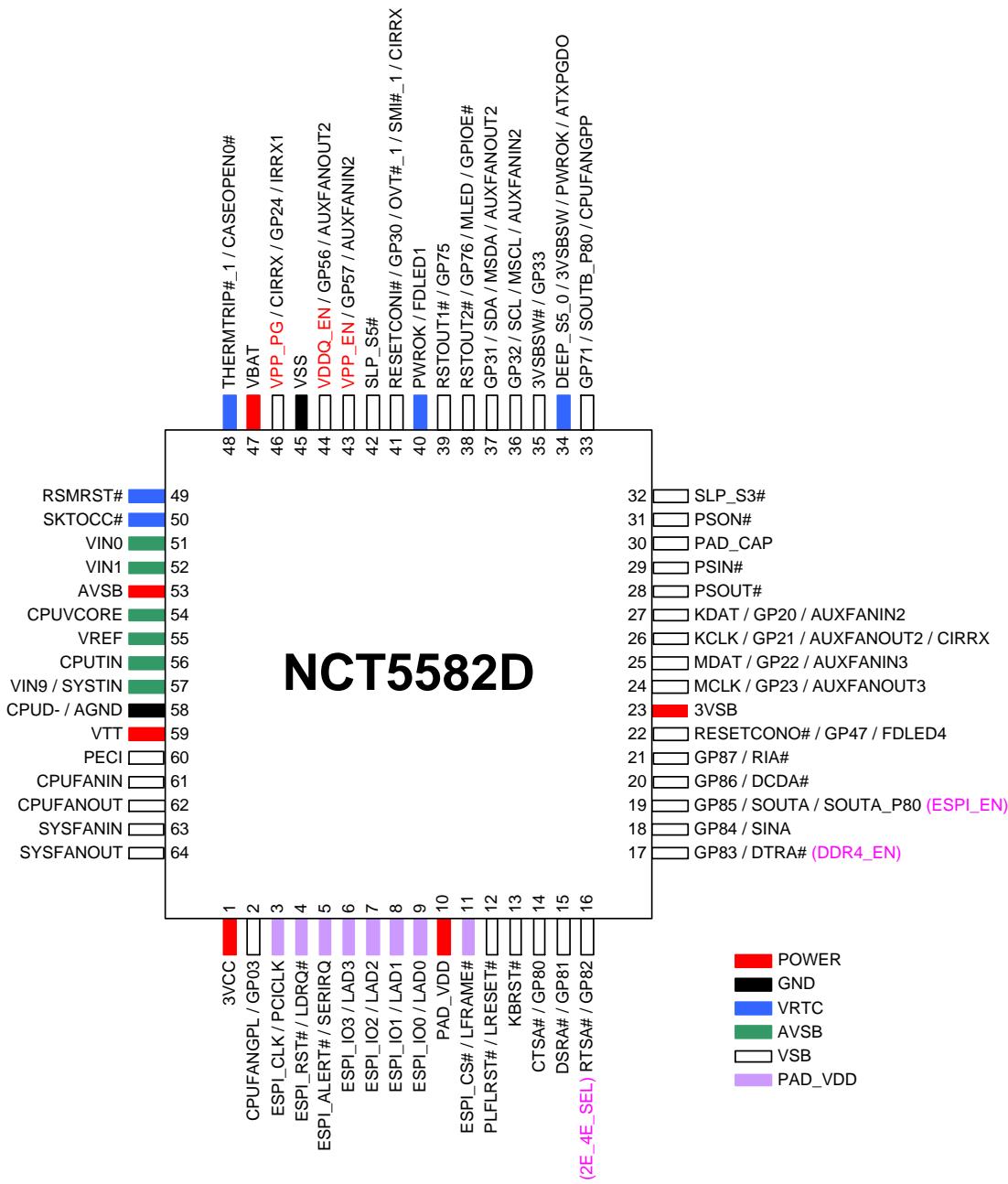


Figure 4-1 NCT5582D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 24.2 DC CHARACTERISTICS for details.

AOUT	- Analog output pin
AIN	- Analog input pin
IN _{tp318}	- 3.3V/1.8V TTL-level input pin
IN _{sp318}	- 3.3V/1.8V TTL-level, Schmitt-trigger input pin
IN _{tp3}	- 3.3V TTL-level input pin
IN _{sp3}	- 3.3V TTL-level, Schmitt-trigger input pin
IN _{gp3}	- 3.3V GTL-level input pin
IN _{tp5}	- 5V TTL-level input pin
IN _{tcup5}	- 5V TTL-level, input buffer with controllable pull-up
IN _{tscup5}	- 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN _{tsp5}	- 5V TTL-level, Schmitt-trigger input pin
IN _{tdp5}	- 5V TTL-level input pin with internal pull-down resistor
O ₈	- output pin with 8-mA source-sink capability
OD ₈	- open-drain output pin with 8-mA sink capability
O ₁₂	- output pin with 12-mA source-sink capability
OD ₁₂	- open-drain output pin with 12-mA sink capability
O ₁₆	- output pin with 16-mA source-sink capability
OD ₁₆	- open-drain output pin with 16-mA sink capability
O ₂₄	- output pin with 24-mA source-sink capability
OD ₂₄	- open-drain output pin with 24-mA sink capability
O ₄₈	- output pin with 48-mA source-sink capability
OD ₄₈	- open-drain output pin with 48-mA sink capability
I/O _{v3}	- Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O _{v4}	- Bi-direction pin with source capability of 6 mA
O _{12cu}	- output pin 12-mA source-sink capability with controllable pull-up
OD _{12cu}	- open-drain 12-mA sink capability output pin with controllable pull-up
OX ₈	- output pin with 8-mA source-sink capability and output voltage high level depend PAD_VDD
ODX ₈	- open-drain output pin with 8-mA sink capability and output voltage high level depend PAD_VDD

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
3	PCICLK	I	IN _{tp318}	PAD_VDD	PCI clock input.
4	LDRQ#	O	OX ₈	PAD_VDD	Encoded DMA Request signal.
5	SERIRQ	I/O	IN _{tp318} O ₈ OD ₈	PAD_VDD	Serialized IRQ input / output.
6-9	LAD[3:0]	I/O	IN _{tp318} ODX ₈	PAD_VDD	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
11	LFRAME#	I	IN _{sp318}	PAD_VDD	Indicates the start of a new cycle or the termination of a broken cycle.
12	LRESET#	I	IN _{sp318}	VSB	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 eSPI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
3	ESPI_CLK	I	IN _{tp318}	PAD_VDD	The eSPI_CLK provides the reference timing for all the serial input and output operations.
4	ESPI_RST#	I	IN _{tp318}	PAD_VDD	Reset the eSPI interface for both master and slaves.
5	ESPI_ALERT#	O	OX ₈ ODX ₈	PAD_VDD	A dedicated Alert# pin is used to signal the Alert event.
6-9	ESPI_IO[3:0]	I/O	IN _{tp318} ODX ₈	PAD_VDD	These are bi-directional input/output pins used to transfer data between master and slaves.
11	ESPI_CS#	I	IN _{sp318}	PAD_VDD	Driving Chip Select# low selects a particular eSPI slave for the transaction.
12	PLTRST#	I	IN _{sp318}	VSB	Platform reset can be used to communicate through the PLATFORM reset# vw command.

5.3 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
21	RIA#	I	IN _{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
20	DCDA#	I	IN _{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
19	SOUTA	O	O ₁₂	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
18	SINA	I	IN _{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
17	DTRA#	O	O ₁₂	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
16	RTSA#	O	O ₁₂	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
15	DSRA#	I	IN _{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
14	CTSA#	I	IN _{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

5.4 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
13	KBRST#	O	O ₁₂ OD ₁₂	VSB	Keyboard reset. This pin is high after system reset. (KBC P20)
26	KCLK	I/O	IN _{tp5} OD ₁₂	VSB	Keyboard Clock. Pull up is recommended if useless.
27	KDAT	I/O	IN _{tp5} OD ₁₂	VSB	Keyboard Data. Pull up is recommended if useless.
24	MCLK	I/O	IN _{tp5} OD ₁₂	VSB	PS2 Mouse Clock. Pull up is recommended if useless.
25	MDAT	I/O	IN _{tp5} OD ₁₂	VSB	PS2 Mouse Data. Pull up is recommended if useless.

5.5 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
26	CIRRX	I	IN _{tp5}	VSB	CIR input for long length
41	CIRRX	I	IN _{tp5}	VSB	CIR input for long length
46	CIRRX	I	IN _{tp5}	VSB	CIR input for long length

5.6 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
50	SKTOCC#	I	IN _{tp5}	VRTC	CPU socket occupied detection

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
48	CASEOPEN0#	I	IN _{tp5}	VRTC	CASE OPEN 0 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
57	VIN9	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
52	VIN1	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
51	VIN0	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
54	CPUVCORE	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
55	VREF	O	AOUT	AVSB	Reference Voltage (around 2.048 V).
56	CPUTIN	I	AIN	AVSB	The input of temperature sensor 2. It is used for CPU temperature sensing.
57	SYSTIN	I	AIN	AVSB	The input of temperature sensor 1. It is used for system temperature sensing.
41	OVT#_1	O	OD ₁₂	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#_1	O	OD ₁₂	VSB	System Management Interrupt channel output.
27	AUXFANIN2	I	IN _{tp5}	VSB	0 to +5 V amplitude fan tachometer input.
36	AUXFANIN2	I	IN _{tp5}	VSB	0 to +5 V amplitude fan tachometer input.
43	AUXFANIN2	I	IN _{tp5}	VSB	0 to +5 V amplitude fan tachometer input.
25	AUXFANIN3	I	IN _{tp5}	VSB	0 to +5 V amplitude fan tachometer input.
26	AUXFANOUT2	O	O ₁₂ OD ₁₂	VSB	PWM duty-cycle signal for fan speed control.
37	AUXFANOUT2	O	O ₁₂ OD ₁₂	VSB	PWM duty-cycle signal for fan speed control.
44	AUXFANOUT2	O	O ₁₂ OD ₁₂	VSB	PWM duty-cycle signal for fan speed control.
24	AUXFANOUT3	O	O ₁₂ OD ₁₂	VSB	PWM duty-cycle signal for fan speed control.
61	CPUFANIN	I	IN _{tp5}	VSB	0 to +5 V amplitude fan tachometer input.
62	CPUFANOUT	O	O ₁₂ OD ₁₂	VSB	PWM duty-cycle signal for fan speed control.
63	SYSFANIN	I	IN _{tp5}	VSB	0 to +5 V amplitude fan tachometer input.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
64	SYSFANOUT	O	O ₁₂ OD ₁₂ AOUT	VSB	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.

5.7 Intel® PECl Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
60	PECI	I/O	I/O _{V3}	VTT	INTEL® CPU PECl interface. Connect to CPU.

5.8 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
29	PSIN#	I	IN _{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
28	PSOUT#	O	OD ₁₂	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
49	RSMRST#	O	OD ₈	VRTC	Resume reset signal output.
32	SLP_S3#	I	IN _{tp318}	VSB	SLP_S3# input.
42	SLP_S5#	I	IN _{tp318}	VSB	SLP_S5# input.
34	ATXPGDO	O	OD ₂₄	VRTC	ATX power good signal output.
31	PSON#	O	OD ₁₂	VSB	Power supply on-off output.
34	PWROK	O	O ₈ OD ₈	VRTC	3VCC PWROK signal.
40	PWROK	O	O ₈ OD ₈	VRTC	3VCC PWROK signal.
41	RESETCONI#	I	IN _{tp5}	VSB	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
22	RESETCONO#	O	OD ₁₂	VSB	RESETCONO# output.
34	3VSBSW	O	OD ₂₄	VRTC	Switch 3VSB power to memory when in S3 state.
35	3VSBSW#	O	OD ₂₄	VSB	Switch 3VSB power to memory when in S3 state.
39	RSTOUT1#	O	O ₁₆ OD ₁₆	VSB	PCI Reset Buffer 1. (from pin LRESET#) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit6.
38	RSTOUT2#	O	O ₁₆ OD ₁₆	VSB	PCI Reset Buffer 2. (from pin LRESET#) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit7.

5.9 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
34	DEEP_S5_0	O	OD ₂₄	VRTC	This pin is to control system power for entering "more power saving mode".

5.10 Port 80 Message Display & LED Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
19	SOUTA_P80	O	O ₁₂	VSB	Serial PORT80 output.
33	SOUTB_P80	O	O ₁₂	VSB	Serial PORT80 output.
38	MLED	O	OD ₁₂	VSB	ASUS power LED output.

5.11 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	SCL	I/O	IN _{sp318} OD ₁₂	VSB	SMBus slave clock.
37	SDA	I/O	IN _{sp318} OD ₁₂	VSB	SMBus slave bi-directional Data.
36	MSCL	I/O	IN _{sp318} OD ₁₂	VSB	SMBus master clock.
37	MSDA	I/O	IN _{sp318} OD ₁₂	VSB	SMBus master bi-directional Data.

5.12 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
23	3VSB	I			+3.3 V stand-by power supply for the digital circuits.
47	VBAT	I			+3 V on-board battery for the digital circuits.
1	3VCC	I			+3.3 V power supply for driving 3 V on host interface.
10	PAD_VDD	I			+3.3 V / +1.8 V power supply for the LPC interface.
53	AVSB	I			Analog +3.3 V power input. Internally supply power to all analog circuits.
58	CPUD- / AGND	I			Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
45	VSS	I			Ground.
59	VTT	I			INTEL® CPU VTT power.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
30	PAD_CAP	O			External Filter Capacitor 4.7u (for internal VSB 1.8V)

5.13 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46	IRRX1	I	IN _{tsp5}	VSB	IR Receiver input.

5.14 GPIOE#

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
38	GPIOE#	I	IN _{tp5}	VSB	GPIOE#

5.15 DDR4 Power Sequence

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46	VPP_PG	I	IN _{tp5}	VSB	DDR4 VPP power on sequence ok signal
43	VPP_EN	O	OD ₁₂	VSB	VPP Power Enable
44	VDDQ_EN	O	OD ₁₂	VSB	VDDQ Power Enable

5.16 General Purpose I/O Port

5.16.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
2	GP03	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 0 bit 3.

5.16.2 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
27	GP20	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 2 bit 0.
26	GP21	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 2 bit 1.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
25	GP22	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 2 bit 2.
24	GP23	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 2 bit 3.
46	GP24	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 2 bit 4.

5.16.3 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
41	GP30	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 3 bit 0.
37	GP31	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 3 bit 1.
36	GP32	I/O	IN _{tsp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 3 bit 2.
35	GP33	I/O	IN _{tp5} O ₂₄ OD ₂₄	VSB	General-purpose I/O port 3 bit 3.

5.16.4 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
22	GP47	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 4 bit 7.

5.16.5 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
44	GP56	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 5 bit 6.
43	GP57	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 5 bit 7.

5.16.6 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
33	GP71	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 7 bit 1.
39	GP75	I/O	IN _{tp5} O ₁₆ OD ₁₆	VSB	General-purpose I/O port 7 bit 5.
38	GP76	I/O	IN _{tp5} O ₁₆ OD ₁₆	VSB	General-purpose I/O port 7 bit 6.

5.16.7 GPIO-8 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	GP80	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 0.
15	GP81	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 1.
16	GP82	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 2.
17	GP83	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 3.
18	GP84	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 4.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
19	GP85	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 5.
20	GP86	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 6.
21	GP87	I/O	IN _{tp5} O ₁₂ OD ₁₂	VSB	General-purpose I/O port 8 bit 7.

5.17 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
16	2E_4E_SEL	I	IN _{tdp5}	VSB	SIO I/O address selection. (Strapped by LRESET#) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
17	DDR4_EN	I	IN _{tdp5}	VSB	Enable DDR4PWR function. (Strapped by VSB power: internal RSMRST# signal.) Strapped to high: Enable DDR4PWR functioin Strapped to low: Disable DDR4PWR function
19	eSPI_EN	I	IN _{tdp5}	VSB	Host interface function selection. (Strapped by VSB power: internal RSMRST# signal.) Strapped to high: eSPI interface Strapped to low: LPC interface

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

- 1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
- 2) VCC Strapping result can be programming by LPC, and reset by PWROK.
- 3) LRESET# strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.18 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	16	3VSB	Pull-down	47.4K	1
DDR4_EN	17	3VSB	Pull-down	47.4K	2
eSPI_EN	19	3VSB	Pull-down	47.4K	2

Signal	Pin(s)	Power well	Type	Resistor	Note
Advanced Configuration & Power Interface					
PSIN#	29	3VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset

Note2. Active only during VSB Power-up reset

6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	42	SLP_S5# input.
RESETCONI#	41	RESETCONI# input signal. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
RESETCONO#	22	RESETCONO# output signal.
PWROK	40	This pin generates the PWROK signals while 3VCC is present.
RSMRST#	49	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT5582D detects the 3VSB voltage rises to "V1", it then starts a delay – "t1" before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below "V2", the RSMRST# de-asserts immediately.

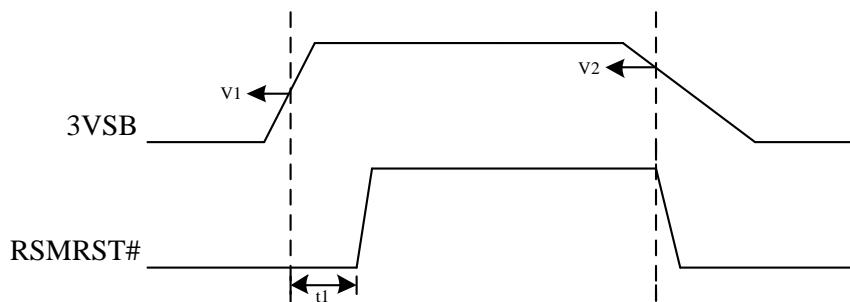


Figure 6-1 RSMRST#

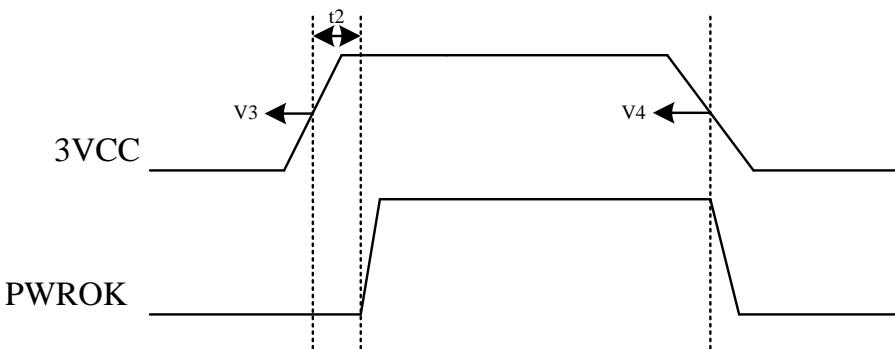


Figure 6-2 PWROK

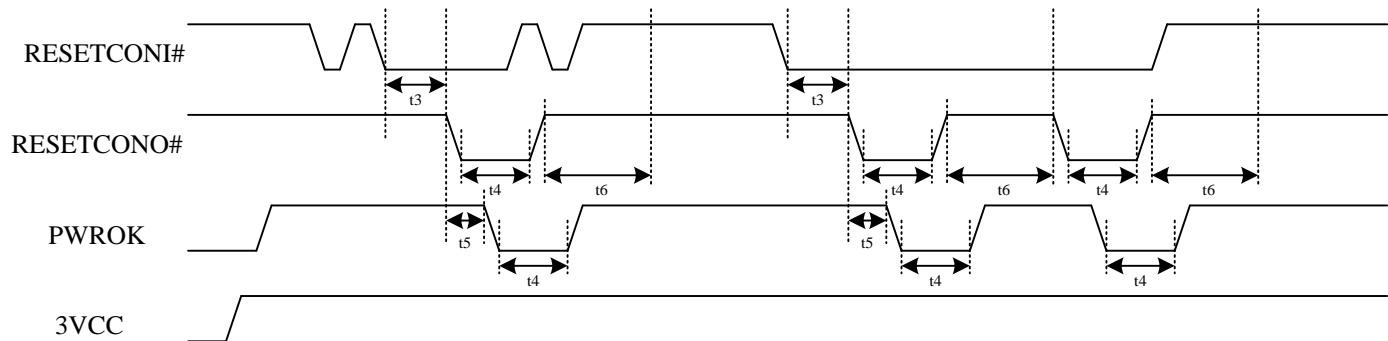


Figure 6-3 RESETCONI# and PWROK

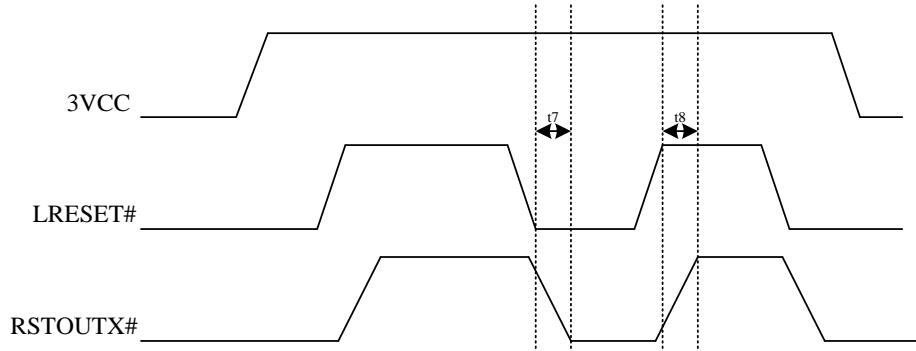


Figure 6-4 RSTOUTX# and LRESET#

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
t2	Valid 3VCC to PWROK active	50	500	mS
t3	RESETCONI# de-bounce	1	5	nS
t4	RESETCONO# and PWROK active	See LDB CRFA		
t5	RESETCONO# active to PWROK active	0	80	nS

TIMING	PARAMETER	MIN	MAX	UNIT
t6	RESETCONO# inactive to RESETCONI# detect	3	4	S
t7	LRESET# active to RSTOUTX# active	0	80	nS
t8	LRESET# inactive to RSTOUTX# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage		3.1	Volt
V2	3VSB Ineffective Voltage	2.92		Volt
V3	3VCC Valid Voltage	-	2.83	Volt
V4	3VCC Ineffective Voltage	2.68	-	Volt

Note : 1. The values above are the worst-case results of R&D simulation.

6.2 GPIOE#

NCT5582D supports GPIOE# functions, please refer the timing diagram below:

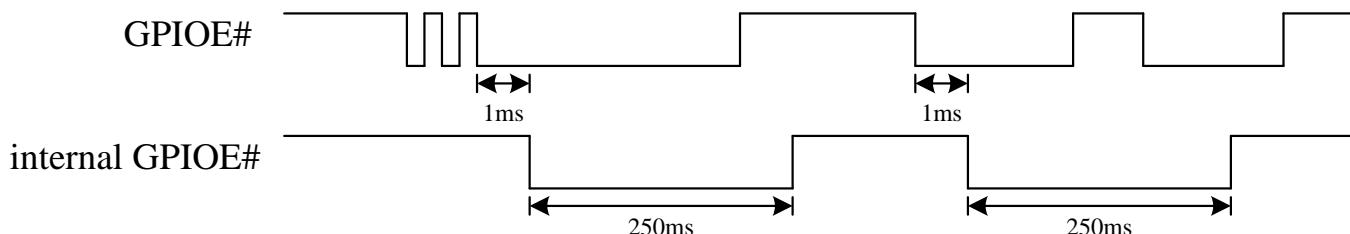


Figure 6-5 GPIOE#

6.3 3VSBSW#

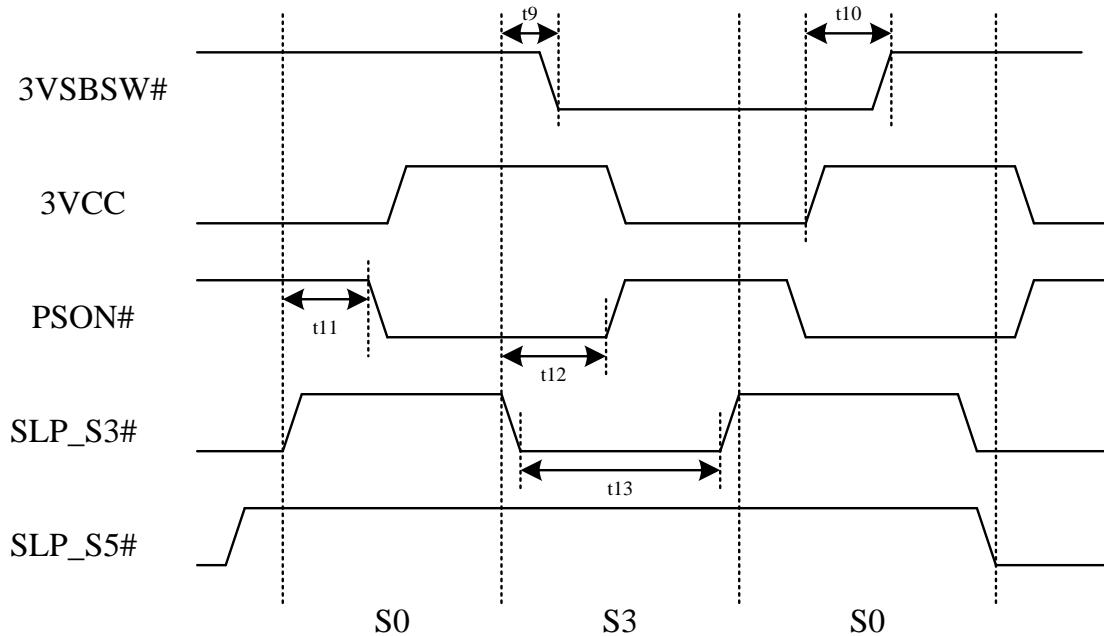


Figure 6-6 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t9	SLP_S3# active to 3VSBSW# active	0	10	mS
t10	3VCC active to 3VSBSW# inactive	120	190	mS
t11	SLP_S3# inactive to PSON# active	0	200	nS
t12	SLP_S3# active to PSON# inactive	15	45	mS
t13	SLP_S3# minimal Low Time	40	-	mS

6.4 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

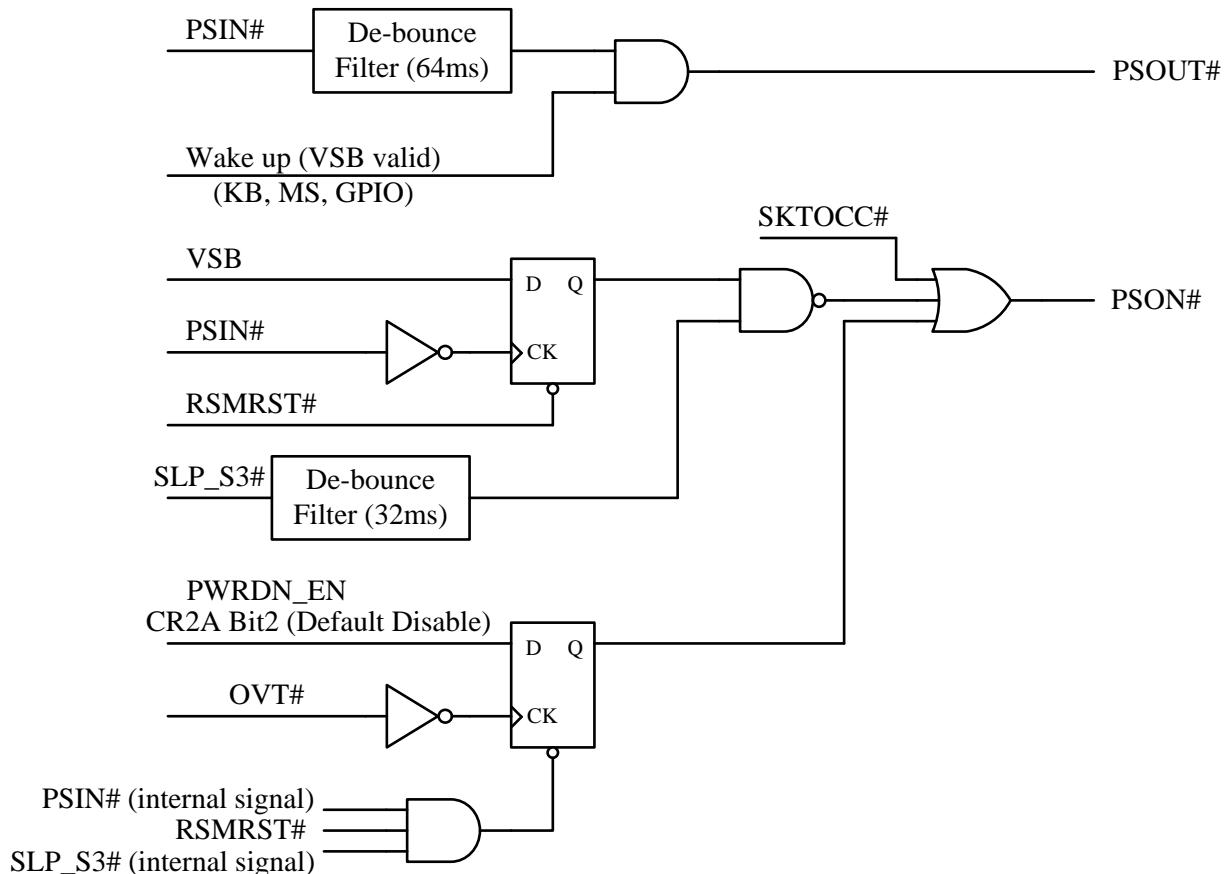


Figure 6-7 PSON# Block Diagram

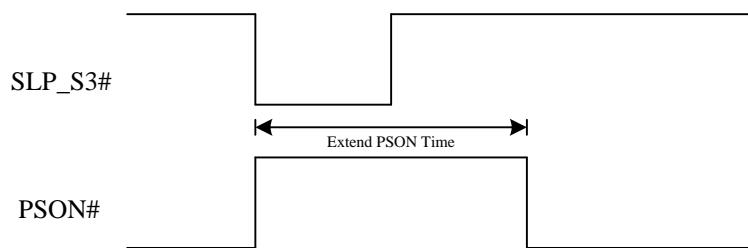
6.5 Extend PSON# after power off

When system goes from S0 state to S3/S5 state (ie. SLPS3# from high to low), PSON# is de-asserted (ie. From low to high). Then if SLPS3# goes back to high immediately, less than a certain period of time (LD12, CREA bit[1:0]), the PSON# signal should be kept high for above-mentioned duration.

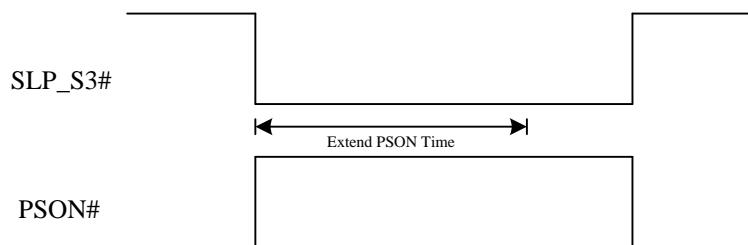
If SLPS3# stays at high longer than the certain period of time, PSON# follows state of SLPS3# again after said duration.

This certain period of time could be set to Disable 2/3/4 seconds. (Disable = 0 seconds).

Condition1 :

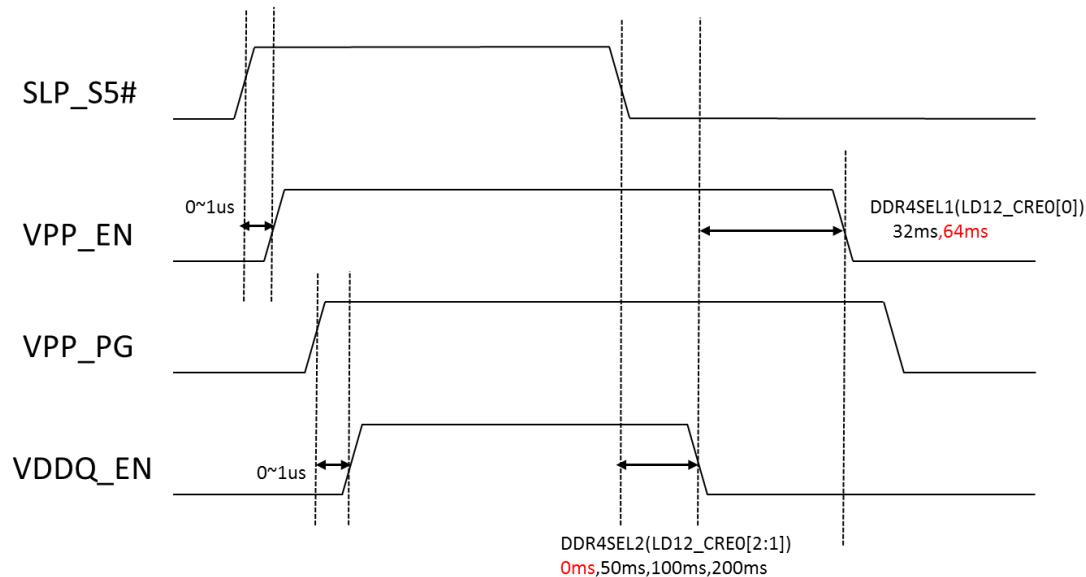


Condition2 :



6.6 DDR4PWR

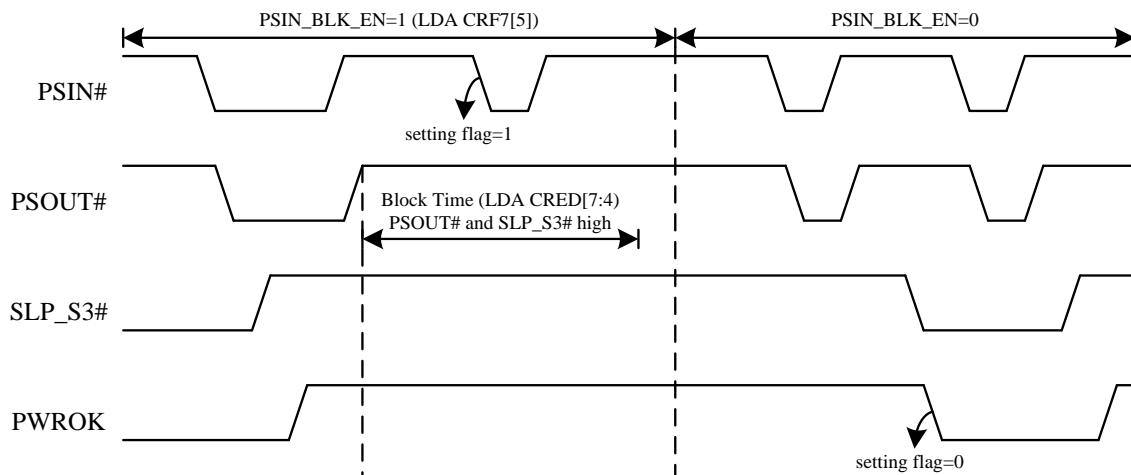
DDR4PWR is the power sequence control of DDR4 SDRAM. It is a high speed and low power platform. There are two timer register can be select in the sequence (DDR4SEL1: LD12 CRE0 bit[0], DDR4SEL2: LD12 CRE0 bit [2:1]).



6.7 PSIN#

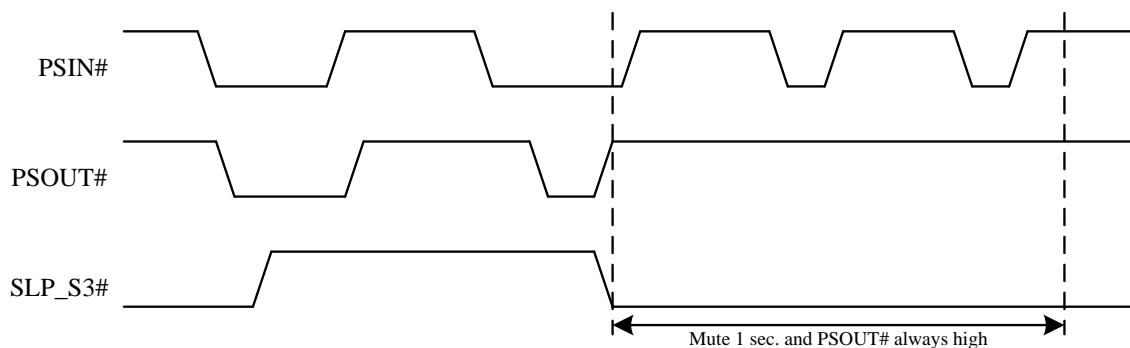
6.7.1 PSIN# Block Diagram (S5 → S0)

When system is at S5 to S0 state, we add block time to avoid system enter S5 again by PSIN# glitch. The block time can be set by LDA CRED bit[7:4] and the default is 0.5sec. If the glitch happen in the block time, the flag (LDA CREC bit[2]) will set high and can be observe when user enter S0 state. The function need to set enable bit (LDA CRF7 bit[5]: PSIN_BLK_EN).



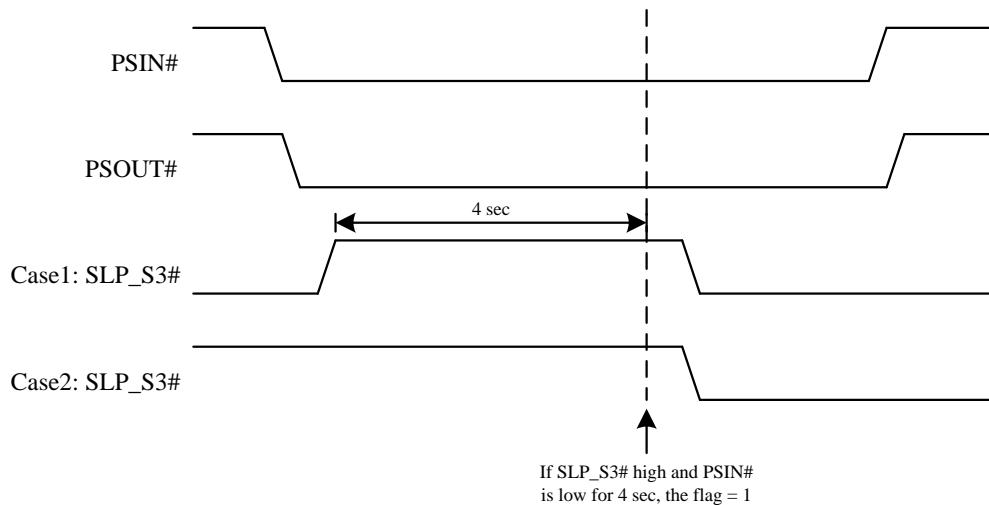
6.7.2 PSIN# Block 1sec Diagram (S0 → S5)

When system is at S0 to S5 state, we add block 1 sec to avoid system enter S0 again by PSIN# glitch. The block time is fix and can't be set. The function need to set enable bit (LDA CRF7 bit[5]: PSIN_BLK_EN).

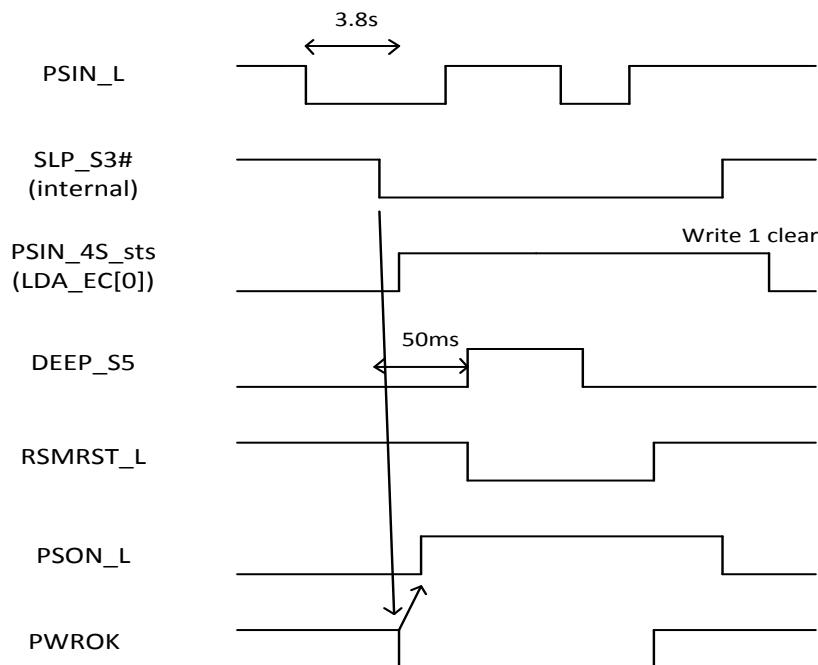


6.7.3 PSIN# 4sec Status Diagram

When user push PSIN button sustainably more than 4 sec and LD11_CRE0[2] =0, the system will enter S5 state and we have a flag to monitor (LDA CREC bit[0]).

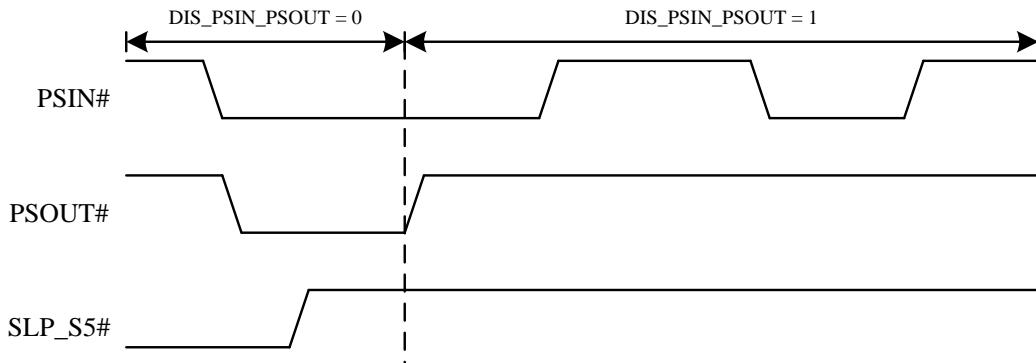


When user push PSIN button sustainably more than 3.8 sec and LD11_CREC[2] =1, the system will enter DeepS5 state and we have a flag to monitor (LDA CREC bit[0]).



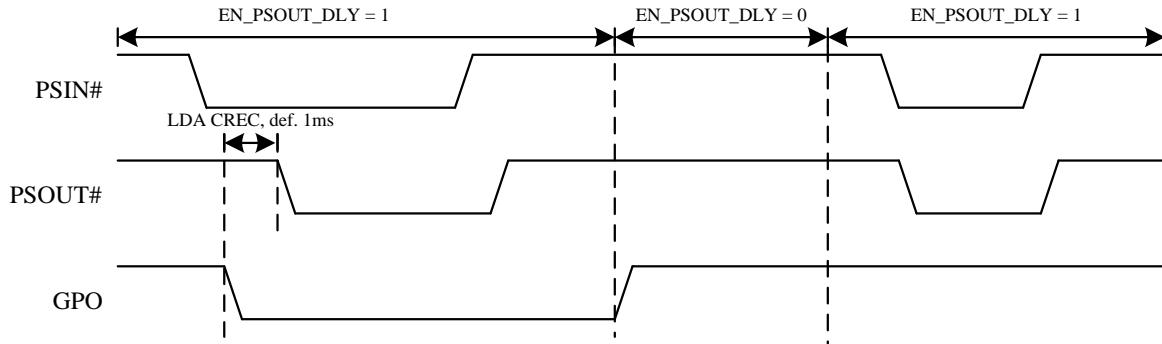
6.7.4 Disable PSIN# to PSOUT# Diagram

When system enter S0 from S5, user can monitor PSIN status by register (LDA CREC bit[7]) for several application. For example, user can set DIS_PSIN_PSOUT (LDA CREC bit[1]) to disconnect PSIN and PSOUT. If DIS_PSIN_PSOUT = 1, PSOUT will not follow PSIN. To avoid BIOS not clear this bit abnormally, it can be cleared automatically by PSIN rising signal to set LDA CREC bit[3] = 1.



6.7.5 Enable PSOUT# Delay Diagram

Normally, PSOUT follows PSIN. For particular case, we can add PSOUT delay from PSIN when system enters S0 state. The delay time can be set by LDA_CREC bit[6:5], and need to enable by LDA_CREC bit [4] (EN_PSOUT_DLY). As system enter S0 state, the enable bit need to clear to release GP73 bus, otherwise, GP73 will keep low. When system enter S5 state from S0, the function will not work even we set the enable bit.



6.8 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

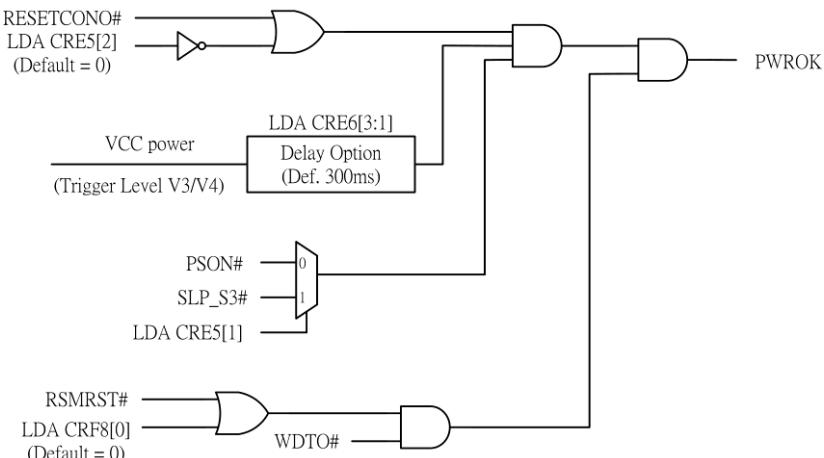


Figure 6-8 PWROK Block Diagram

6.9 Front Panel LEDs

NCT5582D supports two LED control pins – GRN_LED and YLW_LED.

For dual-color LED application:

(1)GRN_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the green LED and the anode of the yellow LED.

(2)YLW_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the yellow LED and the anode of the green LED.

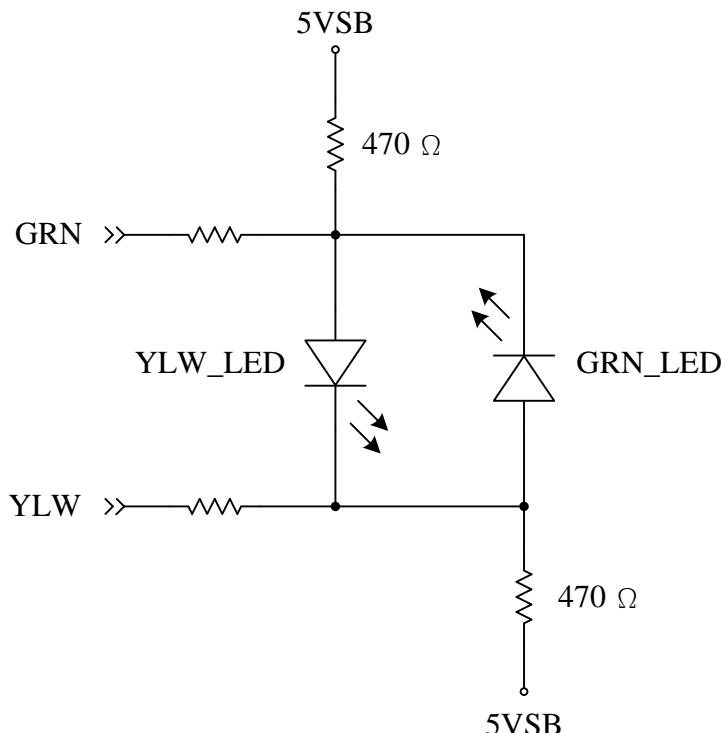


Figure 6-9 Illustration of Dual Color LED application

GRN_LED and YLW_LED pins are designed to show currently power states. There are Manual Mode and Automatic Mode:

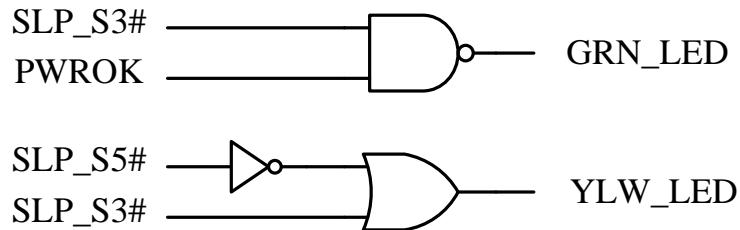
6.9.1 Automatic Mode

Power state is S0 or S1: GRN_LED will be asserted by default.

Power state is S3: YLW_LED will be asserted by default.

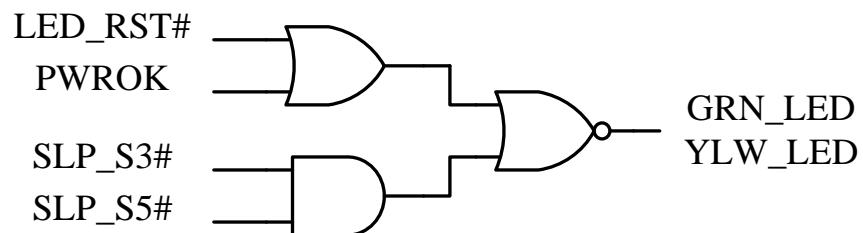
Power state is S4 or S5: Both GRN_LED and YLW_LED will be de-asserted by default.

AUTO_EN	GRN_LED_RST (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
1	X	S0,S1	1	1	GRN_BLK_FREQ	HIGH-Z
1	X	S3	0	1	HIGH-Z	YLW_BLK_FREQ
1	X	S4,S5	X	0	HIGH-Z	HIGH-Z



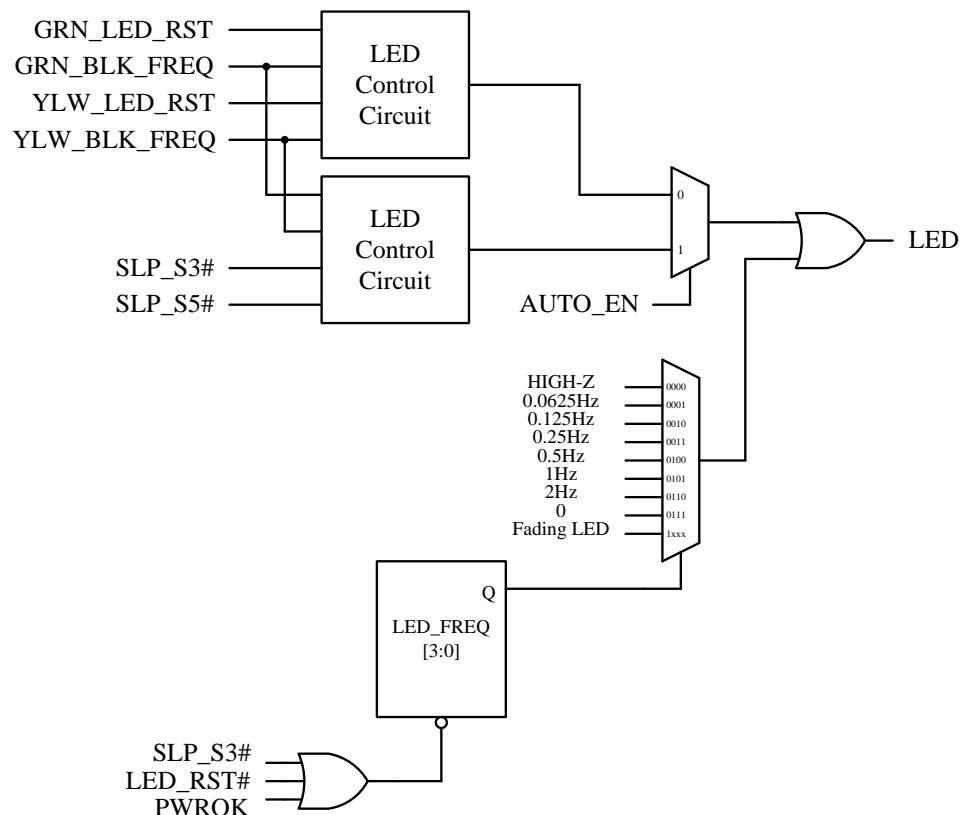
6.9.2 Manual Mode

AUTO_EN	GRN_LED_RST# (YLW_LED_RST#)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
0	0	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	0	S3	0	1	HIGH-Z	HIGH-Z
0	0	S4,S5	X	0	HIGH-Z	HIGH-Z
0	1	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S3	0	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S4,S5	X	0	GRN_BLK_FREQ	YLW_BLK_FREQ



Register Name	Register Location
AUTO_EN	Logic Device B, CRF7h, bit7
GRN_BLK_FREQ	Logic Device B, CRF7h, bit3~0
YLW_BLK_FREQ	Logic Device B, CRF8h, bit3~0
GRN_LED_RST#	Logic Device B, CRF7h, bit6
YLW_LED_RST#	Logic Device B, CRF8h, bit6

6.9.3 S0~S5 LED Blink Block Diagram



6.9.4 LED Pole (LED_POL)

Set to 0b, GRN_LED output is active low, as the following Figure(a)

Set to 1b, GRN_LED output is active high, as the following Figure(b)

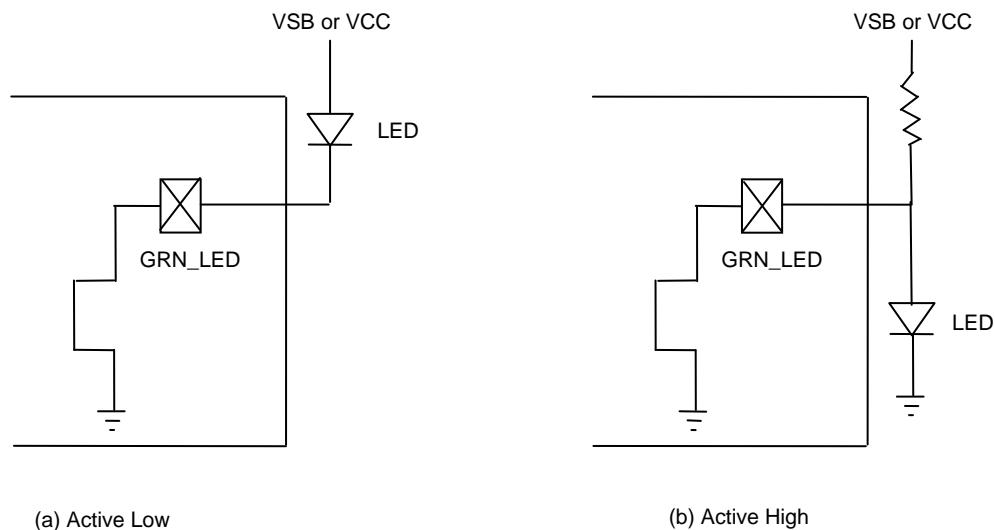
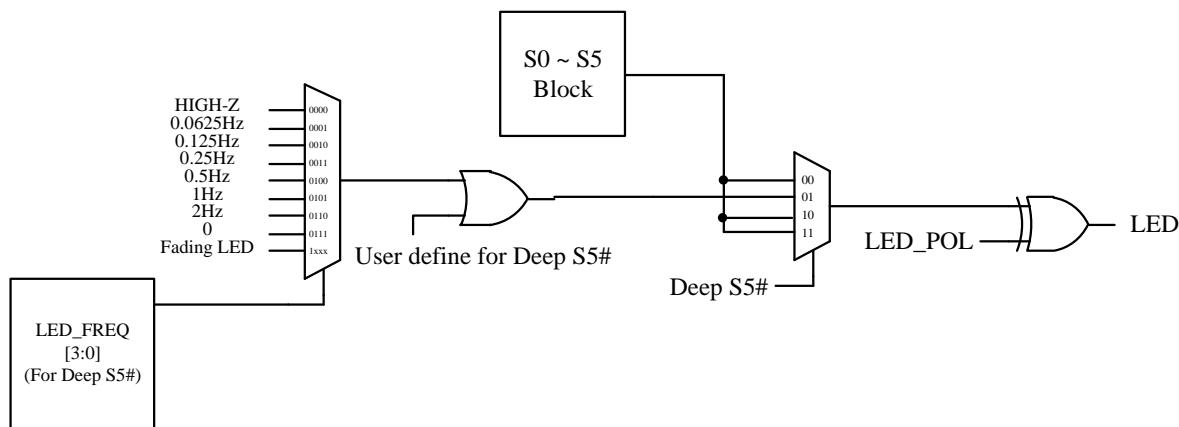


Figure 6-10 Illustration of LED polarity

6.9.5 Deeper Sleeping State Detect Function

These two LED pins could also be used to indicate if the system is in Deeper Sleeping State. For more detail, please refer to the section of Advanced Sleep State Control Function.

Enable_DEEP_S5	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S5	DeepS5_GRN_BLK_FREQ	DeepS5_YLW_BLK_FREQ
1	1	DEEP_S5	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior



6.10 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device 16 CRE0h ~ CRE3h.

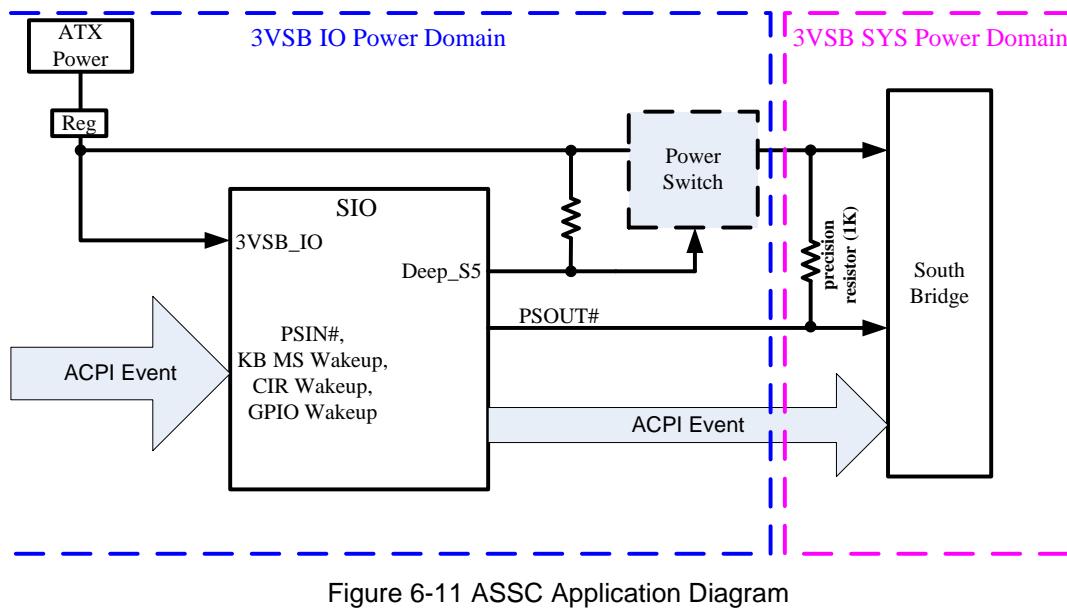
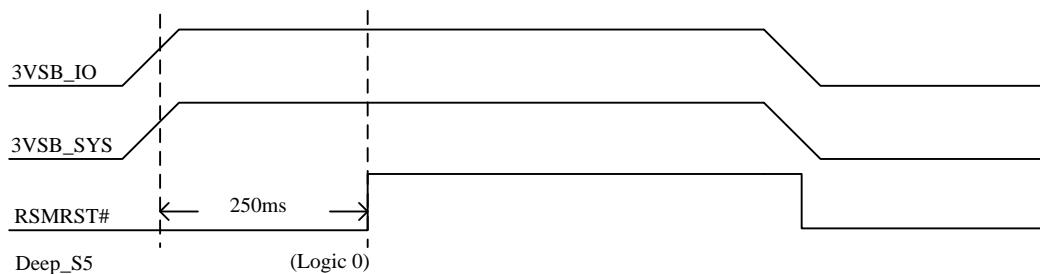


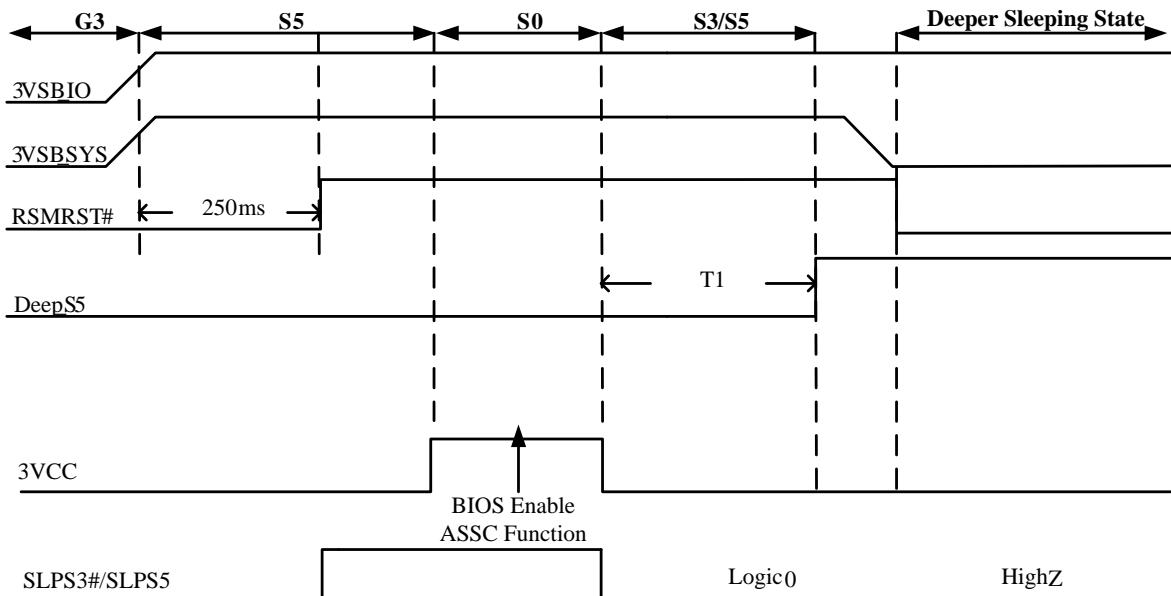
Figure 6-11 ASSC Application Diagram

6.10.1 When ASSC is disabled



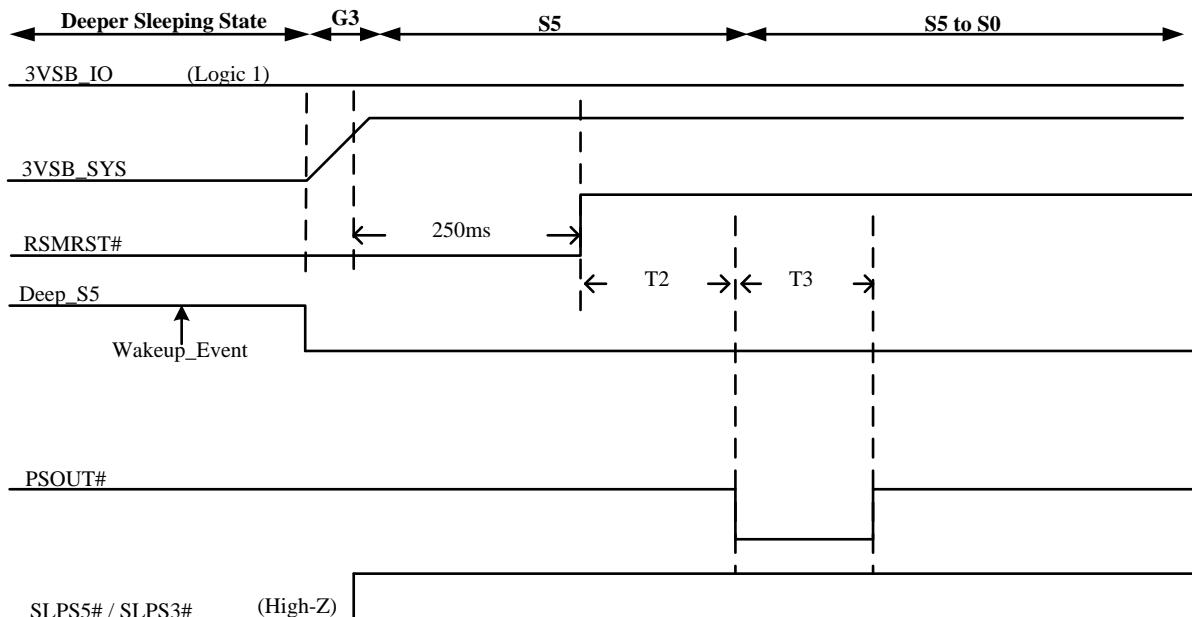
When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

6.10.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the “Deeper Sleeping State (DSS)” where system’s VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

6.10.3 When ASSC is enabled (Exit Deeper Sleeping State)

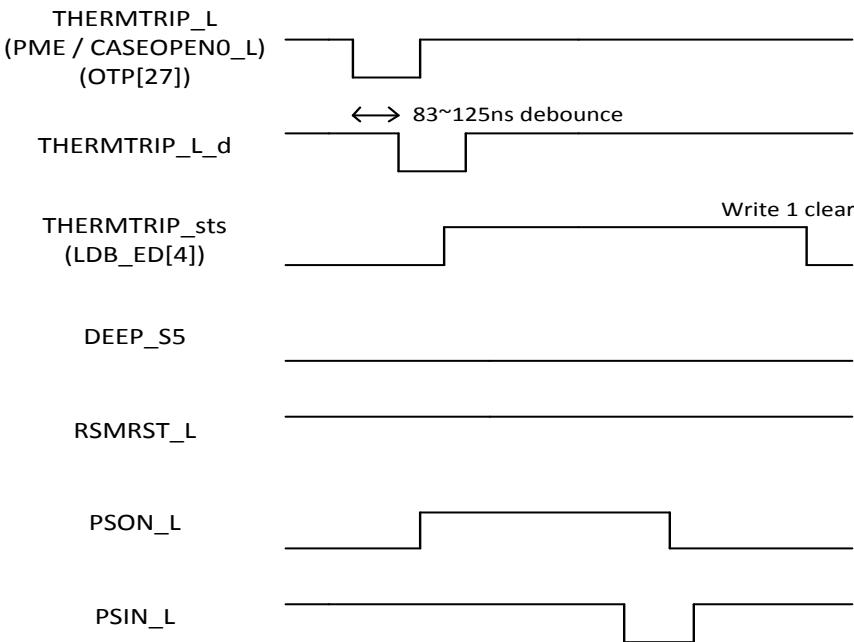


When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time

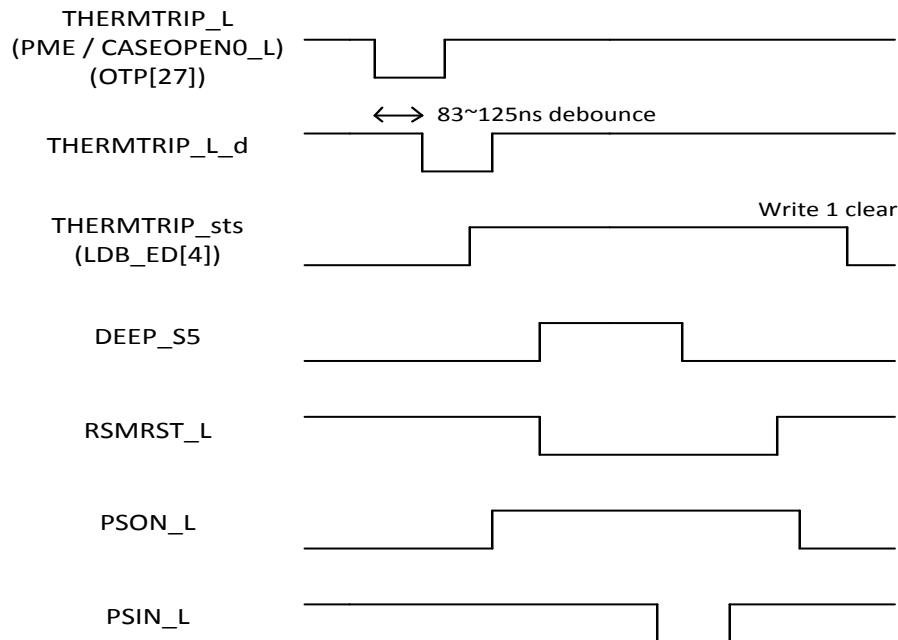
(wakeup delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

6.11 Thermtrip function

When user push Thermtrip button in S0 state and LDB_CRED[3] =0, the system will enter S5 state and we have a flag to monitor (LDB_CRED bit[4]).



When user push Thermtrip button in S0 state and LDB_CRED[3] =1, the system will enter DeepS5 state and we have a flag to monitor (LDB_CRED bit[4]).



7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT5582D uses a special protocol to access configuration registers to set up different types of configurations. The NCT5582D has several Logical Devices (from Logical Device 1 to Logical Device 16).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT5582D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

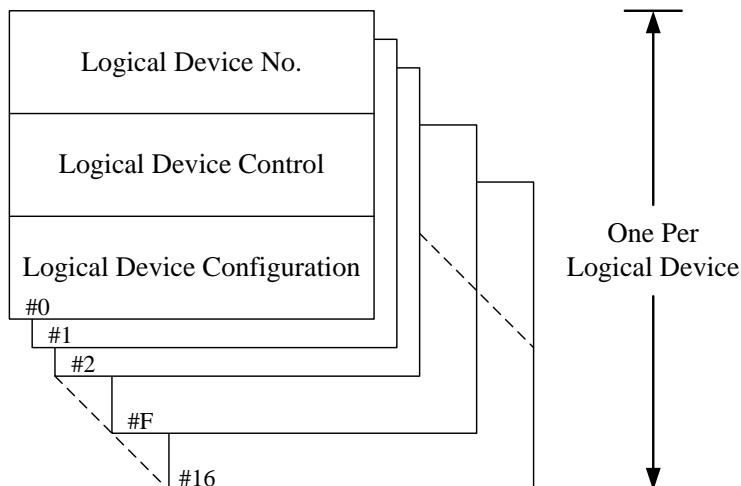


Figure 7-1 Structure of the Configuration Register

7.1 Configuration Sequence

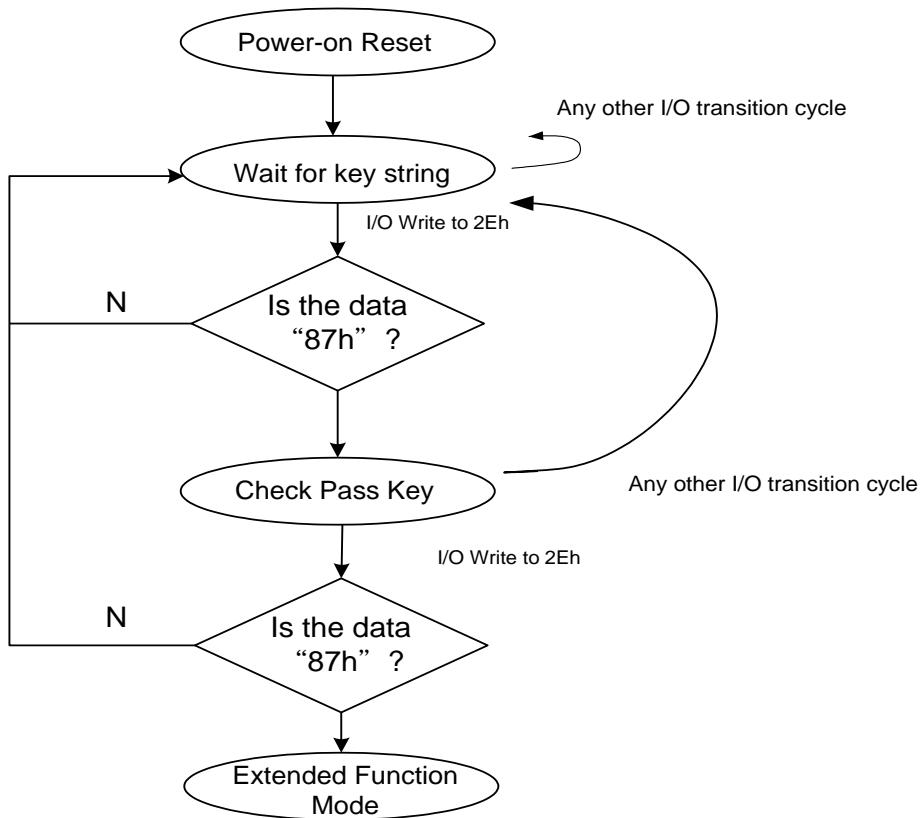


Figure 7-2 Configuration Register

To program the NCT5582D configuration registers, the following configuration procedures must be followed in sequence:

- (1). Enter the Extended Function Mode.
- (2). Configure the configuration registers.
- (3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----
; Enter the Extended Function Mode
;-----
MOV DX, 2EH
MOV AL, 87H
OUT DX, AL
OUT DX, AL
;-----
; Configure Logical Device 1, Configuration Register CRF0
;-----
MOV DX, 2EH
MOV AL, 07H
OUT DX, AL      ; point to Logical Device Number Reg.
MOV DX, 2FH
MOV AL, 01H
OUT DX, AL      ; select Logical Device 1
;
MOV DX, 2EH
MOV AL, F0H
OUT DX, AL      ; select CRF0
MOV DX, 2FH
MOV AL, 3CH
OUT DX, AL      ; update CRF0 with value 3CH
;-----
; Exit the Extended Function Mode
;-----
MOV DX, 2EH
MOV AL, AAH
OUT DX, AL
```

8. HARDWARE MONITOR

8.1 General Description

The NCT5582D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT5582D can simultaneously monitor all of the following inputs:

- Nine analog voltage inputs (Six internal voltages CPUVCORE, VBAT, VTT, 3VSB, 3VCC and AVSB; Three external voltage inputs)
- Four fan tachometer inputs
- Two remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- One case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT5582D can generate the following outputs:

- Four PWM (pulse width modulation) and one DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT5582D provides hardware access to all monitored parameters through the LPC or I²C interface and software access through application software, such as Nuvoton's Hardware DoctorTM, or BIOS.

The rest of this section introduces the various features of the NCT5582D hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT5582D provides two interfaces, LPC and I²C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed from an index/data pair of CPU I/O addresses. The

standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

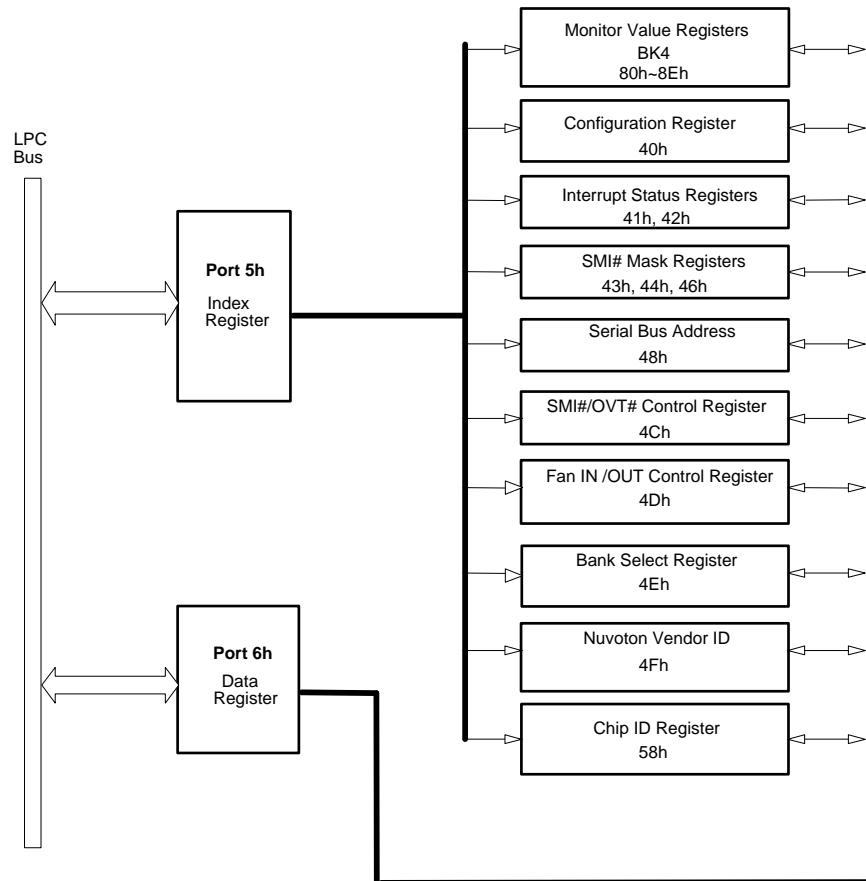


Figure 8-1 LPC Bus' Reads from / Write to Internal Registers

8.4 eSPI interface

The Enhanced Serial Peripheral Interface (eSPI) operates in master/slave mode of operation where the eSPI master dictates the flow of command and data between itself and the eSPI slave by controlling the Chip Select# pins for each of the eSPI slaves. At any one time, the eSPI must ensure that only one of the Chip Select# pins is asserted based on source code, thus allowing transactions to flow between the eSPI master and the corresponding eSPI slave associated with the Chip Select# pin. The eSPI master is the only component that is allowed to drive Chip Select# when eSPI Reset# is de-asserted.

For an eSPI bus, there is only the eSPI master and one or more eSPI slaves. In single Master-Single Slave configuration, a single eSPI master will be connected to a single eSPI slave.

The eSPI provided an alternative for connecting an SIO to the platform (besides the LPC interface). Note the LPC and eSPI co-exist on the platform but only one interface can be enabled at a time via a hardware strap.

The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed from an index/data pair of CPU I/O addresses. The NCT5582D's eSPI is only support IO Read and Write, Get PCH temperature by OOB, and virtual wire.

The basic protocol is shown as below. For the detail eSPI specification, please refer to [Enhanced Serial Peripheral Interface Base Specification \(for Client and Server Platform\) Rev 0.75](#)

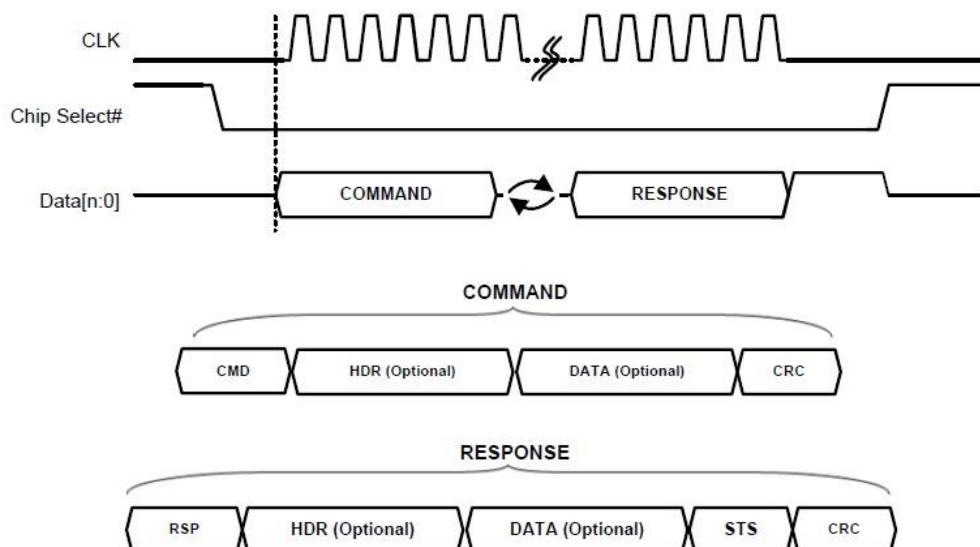


Table 8.4.1 eSPI Protocol Transaction

8.5 I²C interface

The I²C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the NCT5582D hardware monitor and control fan speeds. The address of the I²C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

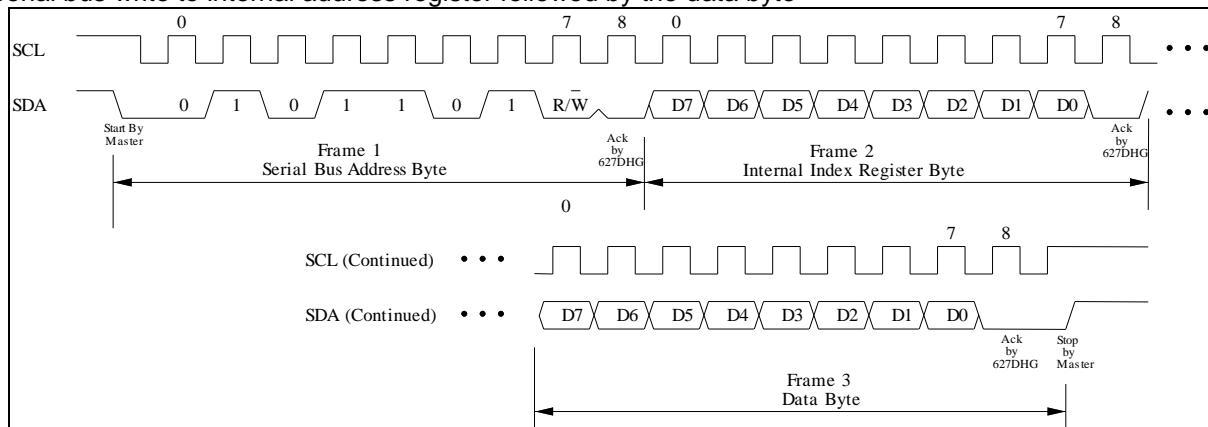


Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

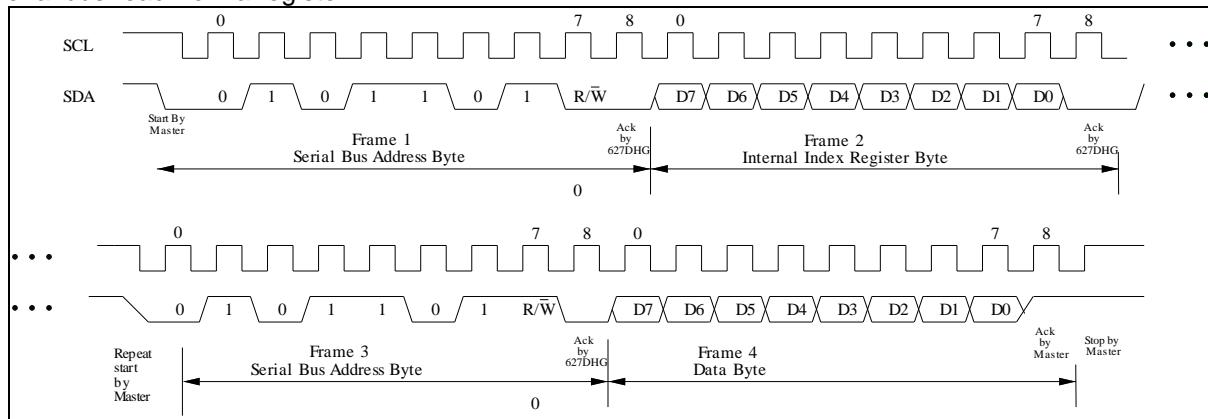


Figure 8-3 Serial Bus Read from Internal Address Register

8.6 Analog Inputs

The analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of general-purpose inputs connected to external device pins (VIN0, VIN1, VIN9) and Six internal signals connected to the power supplies (CPUVCORE, AVSB, VBAT, VTT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

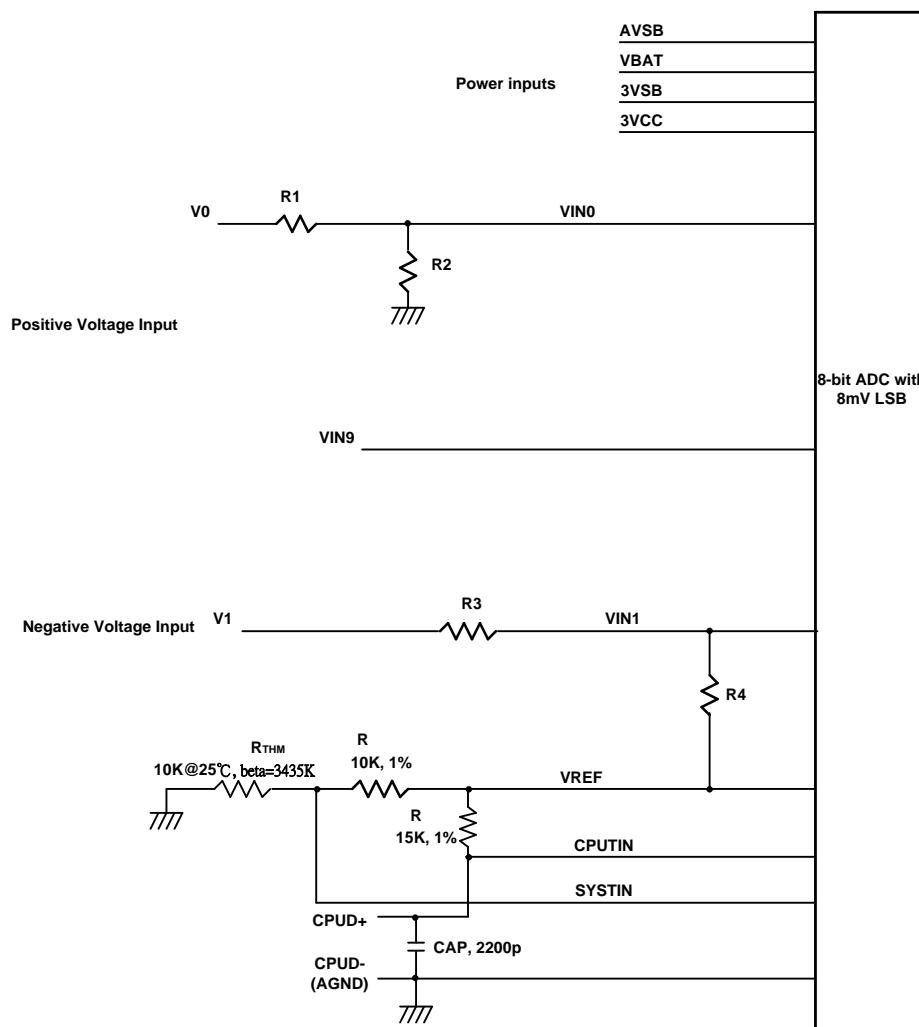


Figure 8-4 Analog Inputs and Application Circuit of the NCT5582D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.6.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R_1 and R_2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVSB, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \approx 1.65V, \text{ where } VCC \text{ is set to } 3.3V$$

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V_1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, \text{ where } V_1 = -12$$

R_3 and R_4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from -12 V to less than 2.048 V. Note that R_4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.6.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

$$\text{Detected Voltage} = \text{Reading} * 0.008 \text{ V}$$

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.6.2.1. Voltage Reading

NCT5582D has following voltage reading:

	CPUVCORE	VIN1	AVSB	3VCC	VIN0
Voltage reading	Bank4, Index80	Bank4, Index81	Bank4, Index82	Bank4, Index83	Bank4, Index84
	VIN9	3VSB	VBAT	VTT	
Voltage reading	Bank4, Index8F	Bank4, Index87	Bank4, Index88	Bank4, Index89	

Note: Bank0 CR BD bit 7:6 are lowest bit1:0 for ADC. These two bits accuracy is not guarantee.

8.6.3 Temperature Data Format

The data format for sensors SYSTIN and CPUTIN is 9-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125 °C	0111,1101	7Dh	0,1111,1010	0FAh
+25 °C	0001,1001	19h	0,0011,0010	032h
+1 °C	0000,0001	01h	0,0000,0010	002h
+0.5 °C	-	-	0,0000,0001	001h
+0 °C	0000,0000	00h	0,0000,0000	000h
-0.5 °C	-	-	1,1111,1111	1FFh
-1 °C	1111,1111	FFh	1,1111,1110	1FFh
-25 °C	1110,0111	E7h	1,1100,1110	1Ceh
-55 °C	1100,1001	C9h	1,1001,0010	192h

8.6.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 K Ω at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-K Ω resistor and then connects to VREF. The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 0, index 59h, 5Dh, and 5Eh.

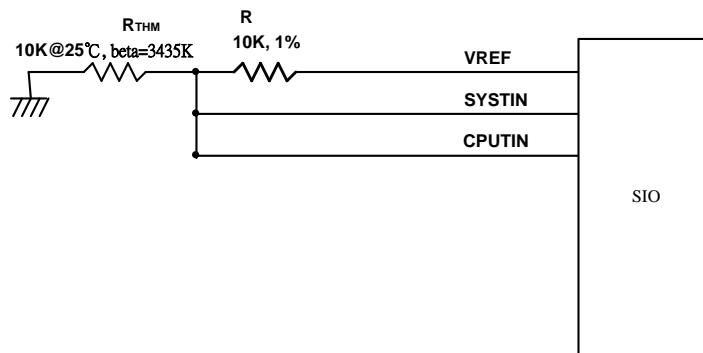


Figure 8-5 Monitoring Temperature from Thermistor

8.6.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND, and the D+ pin is connected to the temperature sensor pin in the NCT5582D. A 15-K Ω resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh, and 5Eh.

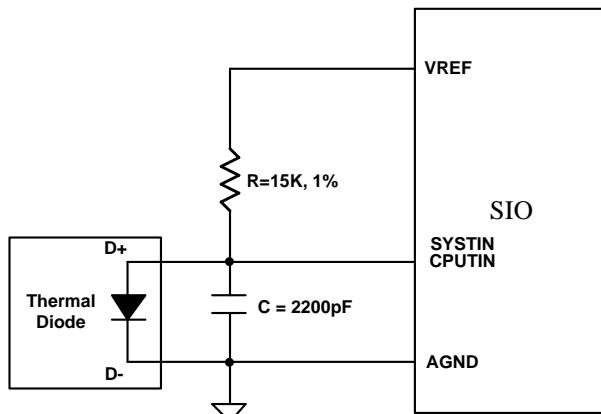


Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.6.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The NCT5582D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

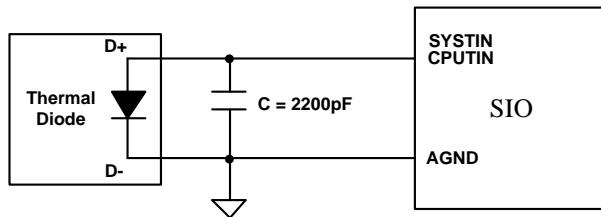


Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- and the pin D+ is connected to temperature sensor pin in the NCT5582D. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

8.6.3.4. Temperature Reading

NCT5582D has 6 temperature reading can monitor different temperature sources (ex. SYSTIN, CPUTIN, PECI...etc).

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4
Temperature source	Bank6,index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default:CPUTIN	BankC,index26 bit[4:0] default:	BankC,index27 bit[4:0] default:
Temperature reading	Bank0, index27	Bank1, index50	Bank6, index70	Bank6, index72

	SMIOVT5	SMIOVT6	SMIOVT7	SMIOVT8
Temperature source	BankC,index28 bit[4:0] default:	BankC,index29 bit[4:0] default:	BankC,index2A bit[4:0] default:	BankC,index2B bit[4:0] default: CPUTIN

Temperature reading	Bank6, index74	Bank6, index76	Bank6, index78	Bank6, index7A
---------------------	----------------	----------------	----------------	----------------

Note. If the temperature source is selecting to PECL, please set Bank0 Index Aeh first for reading correct value.

8.6.4 ADC Conversion Time and Cycle Time

The ADC conversion time of each channel is about 2ms and the period of Cycle time formula is conversion time approx. es total channel number and average time. For example, the NCT5582D support 9 voltage channels and 2 temperature channels, and average time is 8 times, so the period of update time is 2ms x (15 + 7) x 8 = 352ms.

8.7 PECL

PECL (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECL uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECL reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECL is one of the temperature sensing methods that the NCT5582D supports. The NCT5582D contains a PECL master and reads the CPU PECL temperature. The CPU is a PECL client.

The PECL temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECL temperatures. For further information, refer to the PECL specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-8 PECL Temperature shows a typical fan speed (PWM duty cycle) and PECL temperature relationship.

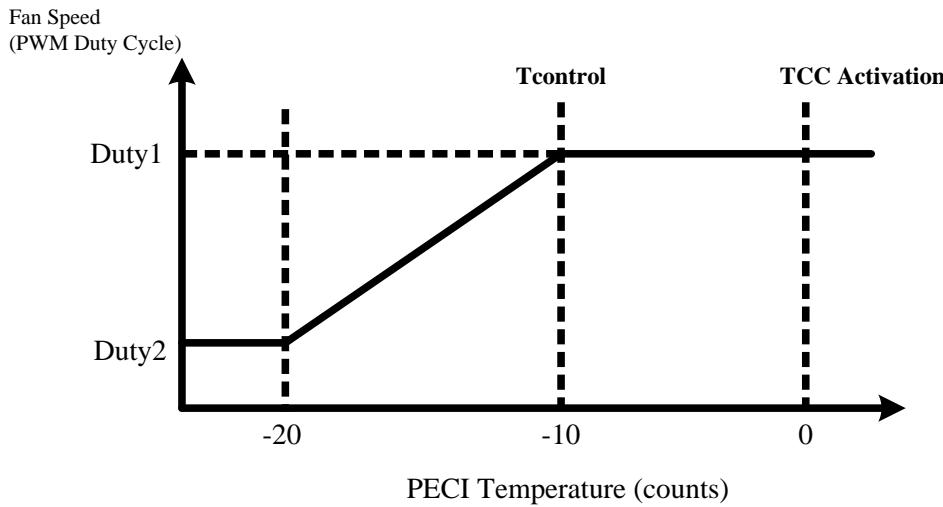


Figure 8-8 PECL Temperature

In this illustration, when PECL temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECL temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECL temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's

guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECL temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

The device also provides an offset register to ‘shift’ the negative PECL readings to positive values. The offset registers are called “Tbase”, which are located at Bank7 Index 09h for Agent0 and Bank7 Index 0Ah for Agent1. All default values of these Tbase registers are 8'h00. The unit of the Tbase register contents is “count” to match that of PECL values. The resultant value (Tbase + PECL) should not be interpreted as the “temperature” (whether in count or °C) of the PECL client (CPU).

The Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets, shows the temperature and fan-speed relationship after Tbase offset is applied (based on Figure 8-8 PECL Temperature). This view is from the perspective of the NCT5582D fan control circuit.

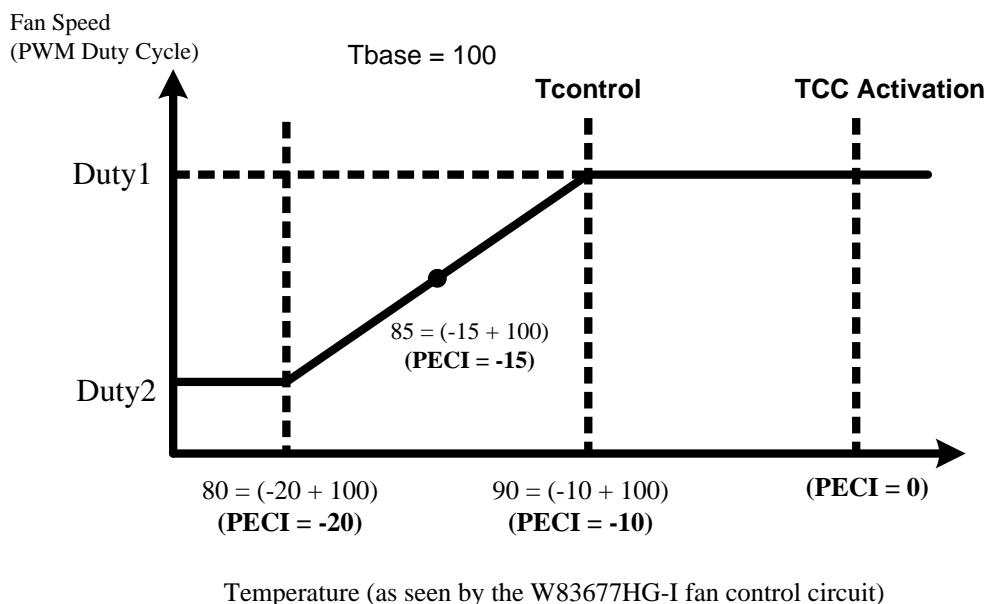


Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets

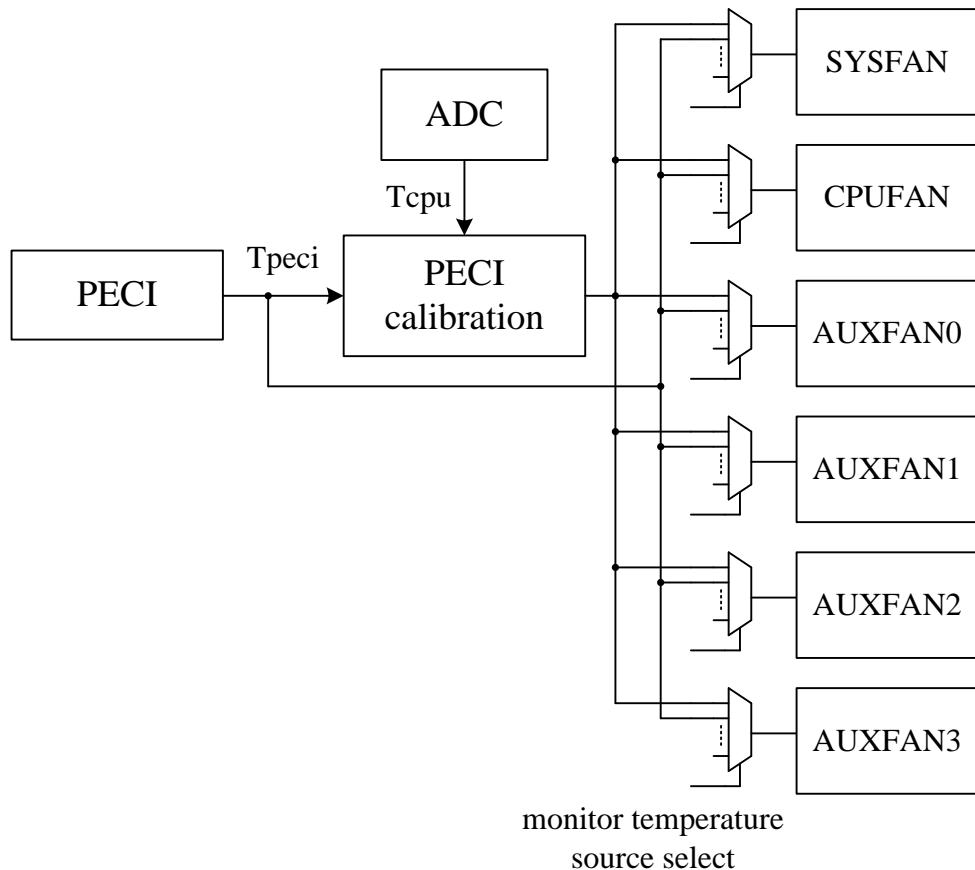
Assuming Tbase is set to 100 and the PECL temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT5582D, BIOS/software can include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 ⁽¹⁾, the threshold temperature value corresponding to the “100% fan duty-cycle” event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECL-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

8.7.1 PECL Calibration

NCT5582D support PECL calibration to adjust the temperature read from CPU to thermistor because the source of thermistor is more accurate than PECL. We have several register for user to set. Bank4 Index Fah, FBh [0] is the enable bit for two agents. If user disable the function, the output will be the original source of PECL. Index Fah, FBh [7:4] is interval time for each calibrate, for example, every 0.1 sec (default) will calibrate again. Index F8h, F9h [7:3] is the max number of update times, number = 0 means only update 1 times. Index F4h, F5h [2:0] is the unit step, unit = 0 means 1 degree. Index F4h, F5h is the result of calibration. We have the overflow and underflow mechanism to protect the system.



8.8 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.8.1 Fan Speed Reading

The fan speed reading at:

	FAN COUNT READING		FAN RPM READING	
	13-bit		16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	Bank4, indexB0	Bank4, indexB1	Bank4, indexC0	Bank4, indexC1
CPUFANIN	Bank4, indexB2	Bank4, indexB3	Bank4, indexC2	Bank4, indexC3
AUXFANIN2	Bank4, indexB8	Bank4, indexB9	Bank4, indexC8	Bank4, indexC9
AUXFANIN3	Bank4, indexBA	Bank4, indexBB	Bank4, indexCA	Bank4, indexCB

8.8.2 Fan Speed Calculation by Fan Count Reading

In 13-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.8.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.8.4 Fan Speed Control

The NCT5582D has four output pins for fan control, Only SYSFANOUT offers PWM duty cycle and DC voltage to control the fan speed.

	SYSFANOUT	CPUFANOUT
Output Type Select	Bank0, index04 bit0 0: PWM output 1: DC output (default)	Only PWM output
Output Type Select (in PWM output)	CR24 bit4 0: open-drain (default) 1: push-pull	CR24 bit3 0: open-drain (default) 1: push-pull
PWM Output Frequency	Bank0, Index00	Bank0, Index02
Fan Control Mode Select	Bank1, index02, bit[7:4]	Bank2, index02, bit[7:4]

		0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	PWM output (Duty)	Bank1, index09 bit[7:0]	Bank2, index09 bit[7:0]
	DC output (Voltage)	Bank1, index09 bit[7:2]	
Current Output Value (read only)		Bank0, index01	Bank0, index03

	AUXFANOUT2	AUXFANOUT3
Output Type Select	Only PWM output	Only PWM output
Output Type Select (in PWM output)	CR24 bit7 0: open-drain (default) 1: push-pull	CR24 bit1 0: open-drain (default) 1: push-pull
PWM Output Frequency	Bank0, Index14	Bank0, Index16
Fan Control Mode Select	Bank9, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	BankA, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	PWM output (Duty)	Bank9, index09 bit[7:0]
	DC output (Voltage)	
Current Output Value (read only)	Bank0, Index15	Bank0, Index17

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 09h for SYSFANOUT, Bank2 Index 09h for CPUFANOUT, Bank9 Index 09h for AUXFANOUT2 and BankA Index 09h for AUXFANOUT3. The duty cycle can be calculated using the following equation:

$$\text{Duty cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

The default duty cycle is 7Fh, or 50% for SYSFANOUT, CPUFANOUT, AUXFANOUT2 and AUXFANOUT3.

Note. The default speed of fan output is specified in registers CR[E0h], CR[E1h], CR[E4h] and CR[E7h] of Logical Device B.

The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, Index 14h and Index 16h.

For DC, the NCT5582D has a six bit digital-to-analog converter (DAC) that produces 0 to 2.048 Volts DC. The analog output is programmed at Bank1 Index 09h bit[7:2] for SYSFANOUT. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = V_{ref} \times \frac{\text{Programmed 6-bit Register Value}}{64}$$

The default value is 111111YY, or nearly 2.048 V, and Y is a reserved bit.

8.8.5 SMART FAN™ Control

The NCT5582D supports various different fan control features:

- ◆ SMART FAN™ I (Thermal Cruise & Speed Cruise)
- ◆ SMART FAN™ IV
- ◆ SMART FAN™ IV Close-Loop Fan Control RPM mode

	SYSFANOUT	CPUFANOUT
Fan Control Mode Select	Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
AUXFANOUT2	AUXFANOUT3	

	AUXFANOUT2	AUXFANOUT3
Fan Control Mode Select	Bank9, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	BankA, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
SYSFANOUT	CPUFANOUT	

8.8.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT
Fan Control Temperature Source Select	Bank1, index00 bit[4:0] Default: SYSTIN	Bank2, index00 bit[4:0] Default: CPUTIN
Fan Control Temperature Reading	Bank0, index73 & Bank0, index74 bit7	Bank0, index75 & Bank0, index76 bit7

	AUXFANOUT2	AUXFANOUT3
Fan Control Temperature Source Select	Bank9, index00 bit[4:0]	BankA, index00 bit[4:0]
SYSFANOUT	CPUFANOUT	

	Default: AUXTINO	Default: AUXTINO
Fan Control Temperature Reading	Bank0, index7B & Bank0, index7C bit7	Bank0, index7D & Bank0, index7E bit7

Note. If the temperature source is selecting to PECL, please set Bank0 Index Aeh first for reading correct value.

8.8.7 Temperature Source comparator

The NCT5582D support the priority of Temperature source and select the maximum temperature to be the fan temperature source. The enable bit and temperature source select is setting following Table.

	SYSFANOUT	CPUFANOUT
Fan Control Temperature Source Select2	Bank1, Index1D bit[4:0]	Bank2, Index1D bit[4:0]
Fan Control Temperature Source Select3	Bank1, Index1E bit[4:0]	Bank2, Index1E bit[4:0]
Enable	Bank1, Index1F bit[0]	Bank2, Index1F bit[0]
	AUXFANOUT2	AUXFANOUT3
Fan Control Temperature Source Select2	Bank9, Index1D bit[4:0]	BankA, Index1D bit[4:0]
Fan Control Temperature Source Select3	Bank9, Index1E bit[4:0]	BankA, Index1E bit[4:0]
Enable	Bank9, Index1F bit[0]	BankA, Index1F bit[0]

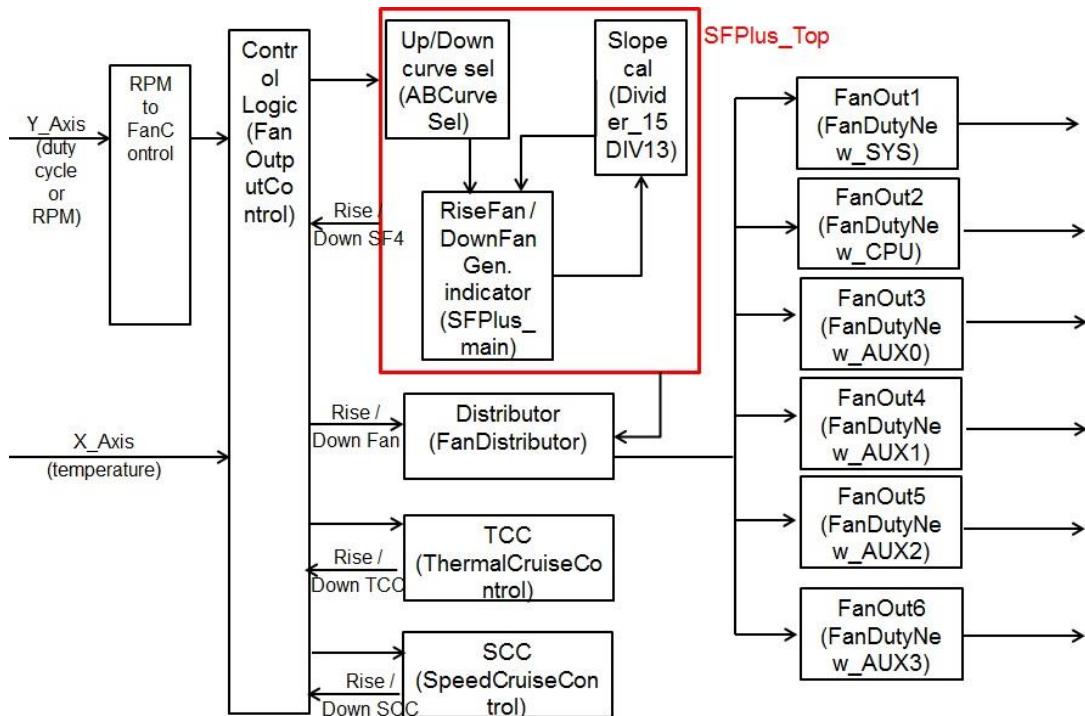


Figure 8-10 SMART FAN™ Function Block Diagram

8.9 SMART FAN™ I

8.9.1 Thermal Cruise Mode

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., $55^{\circ}\text{C} \pm 3^{\circ}\text{C}$). As long as the current temperature remains below the low end of this range (i.e., 52°C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

- (1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.
- (2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52°C), fan output remains the same.
- (3) If the temperature falls below the low end (e.g., 52°C), fan output decreases slowly to zero or to a specified "stop value".

This "stop value" is enabled by the Bank1, Index00h, Bit7 for SYSFANOUT; Bank2, Index00h, Bit7 for CPUFANOUT; Bank9, Index00h, Bit7 for AUXFANOUT2; BankA, Index00h, Bit7 for AUXFANOUT3.

The "stop value" itself is separately specified in Bank1 Index05h, Bank2 Index05h, Bank9 Index05h, BankA Index05h.

The "stop time" means fan remains at the stop value for the period of time also separately defined in Bank1 Index07h, Bank2 Index07h, Bank9 Index07h, BankA Index07h.

Note. The function only support for Thermal Cruise Mode.

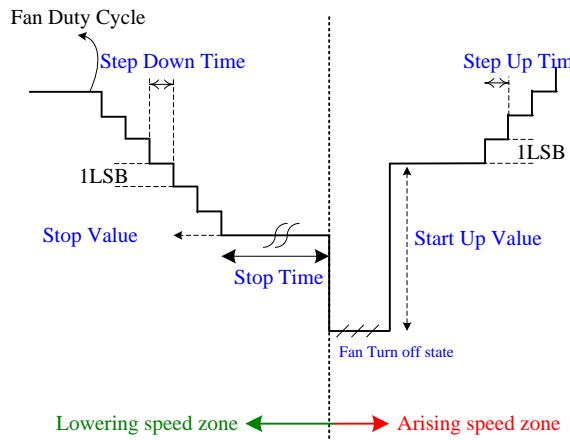


Figure 8-11 Thermal Cruise™ Mode Parameters Figure

In general, Thermal Cruise mode means

- If the current temperature is higher than the high end, increase the fan speed.
- If the current temperature is lower than the low end, decrease the fan speed.
- Otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

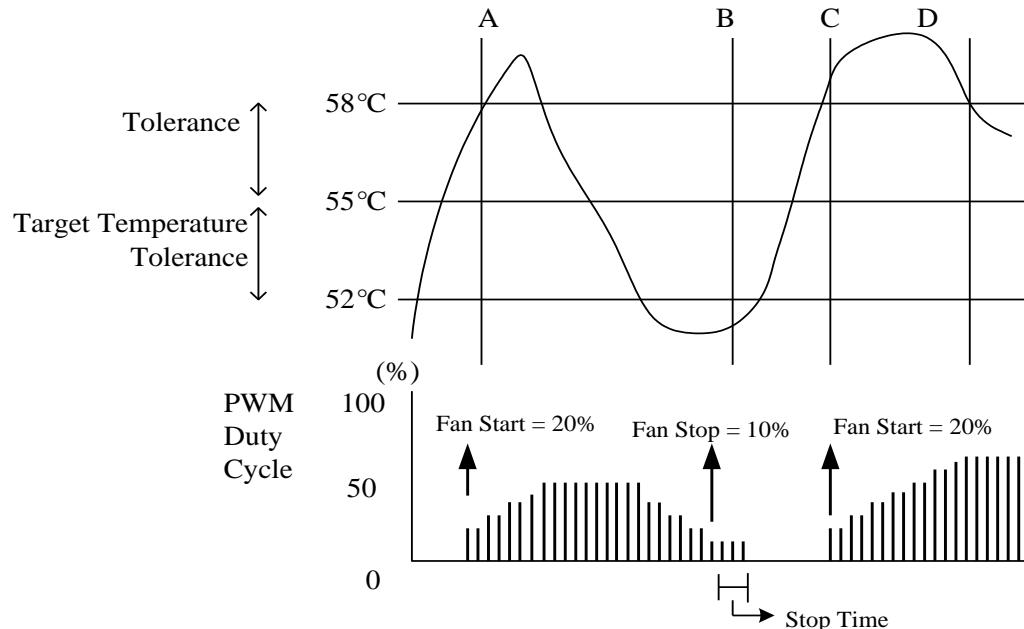


Figure 8-12 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

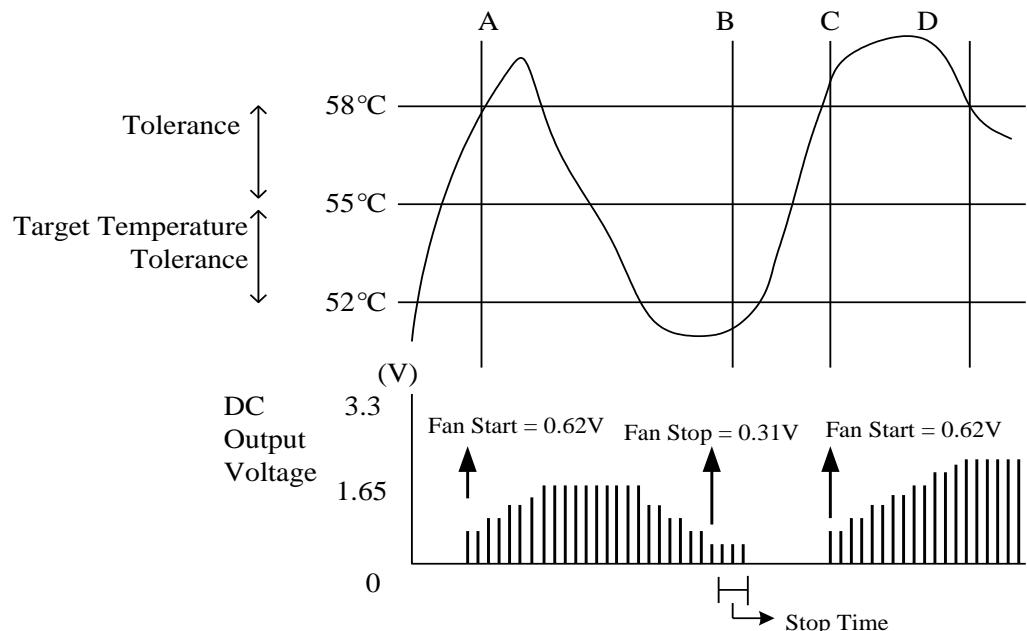


Figure 8-13 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.9.2 Speed Cruise Mode

Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

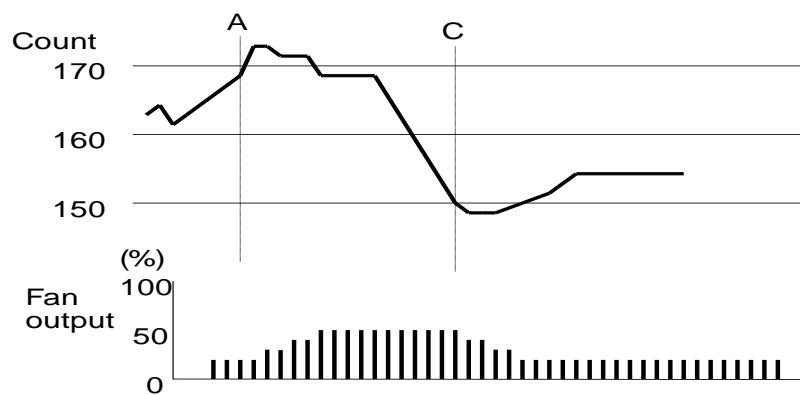


Figure 8-14 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-2 Relative Registers – at Thermal CruiseTM Mode

Publication Release Date: December 10, 2018

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP- UP TIME	STEP- DOWN TIME
SYSFANOUT	Bank 1, index 01h bit[7:0]	Bank 1, index 02h Bit[2:0]	Bank 1, index 06h	Bank 1, index 05h	Bank 1, Index 00h, bit7	Bank 1, index 07h	Bank 1, index 03h	Bank 1, index 04h
CPUFANOUT	Bank 2, index 01h bit[7:0]	Bank 2, index 02h Bit[2:0]	Bank 2, index 06h	Bank 2, index 05h	Bank 2, Index 00h, bit7	Bank 2, index 07h	Bank 2, index 03h	Bank 2, index 04h
AUXFANOUT2	Bank 9, index 01h bit[7:0]	Bank 9, index 02h Bit[2:0]	Bank 9, index 06h	Bank 9, index 05h	Bank 9, Index 00h, bit7	Bank 9, index 07h	Bank 9, index 03h	Bank 9, index 04h
AUXFANOUT3	Bank A, index 01h bit[7:0]	Bank A, index 02h Bit[2:0]	Bank A, index 06h	Bank A, index 05h	Bank A, Index 00h, bit7	Bank A, index 07h	Bank A, index 03h	Bank A, index 04h
THERMAL CRUISE MODE	CRITICAL TEMPERATURE	ENABLE THERMAL CRUISE MODE						
SYSFANOUT	Bank 1, index 35h	Bank 1, Index 02h, bit[7:4] = 01h						
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 02h, bit[7:4] = 01h						
AUXFANOUT2	Bank 9, Index 35h	Bank 9, Index 02h, bit[7:4] = 01h						
AUXFANOUT3	Bank A, Index 35h	Bank A, Index 02h, bit[7:4] = 01h						

Table 8-3 Relative Registers – at Speed CruiseTM Mode

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP-UP TIME	STEP-DOWN TIME	STEP-UP VALUE	STEP-DOWN VALUE	ENABLE SPEED CRUISE MODE
SYSFANOUT	Bank 1, Index 01h	Bank 1, Index 0C bit[3:0]	Bank 1, Index 02 bit[2:0]	Bank 1, Index 0C bit[6:4]	Bank 1, Index 03h	Bank 1, Index 04h	Bank1, Index66 Bit[7:4]	Bank1, Index66 Bit[3:0]	Bank 1, Index 02h bit[7:4] = 02h
CPUFANOUT	Bank 2, Index 01h	Bank 2, Index 0C bit[3:0]	Bank 2, Index 02 bit[2:0]	Bank 2, Index 0C bit[6:4]	Bank 2, Index 03h	Bank 2, Index 04h	Bank2, Index66 Bit[7:4]	Bank2, Index66 Bit[3:0]	Bank 2, Index 02h bit[7:4] = 02h

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP-UP TIME	STEP-DOWN TIME	STEP-UP VALUE	STEP-DOWN VALUE	ENABLE SPEED CRUISE MODE
AUXFANOUT2	Bank 9, Index 01h	Bank 9, Index 0C bit[3:0]	Bank 9, Index 02 bit[2:0]	Bank 9, Index 0C bit[6:4]	Bank 9, Index 03h	Bank 9, Index 04h	Bank9, Index66 Bit[7:4]	Bank9, Index66 Bit[3:0]	Bank 9, Index 02h bit[7:4] = 02h
AUXFANOUT3	Bank A, Index 01h	Bank A, Index 0C bit[3:0]	Bank A, Index 02 bit[2:0]	Bank A, Index 0C bit[6:4]	Bank A, Index 03h	Bank A, Index 04h	BankA, Index66 Bit[7:4]	BankA, Index66 Bit[3:0]	Bank A, Index 02h bit[7:4] = 02h

8.10 SMART FAN™ IV & Close Loop Fan Control Mode

SMART FAN™ IV and Close Loop Fan Control Mode offer 3 slopes to control the fan speed.

Set Critical Temperature, Bank1 Index 35_{HEX}, Bank2 Index 35_{HEX}, Bank9 Index 35_{HEX}, BankA Index 35_{HEX}.

- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
If fan control mode is set as Close Loop Fan Control, the unit step is 50RPM. So the maximum controllable RPM is 50*255=12,750RPM.
If Enable RPM High Mode (Bank6 index6 Bit0), unit is 100RPM.
- Set Tolerance of Target Temperature, Bank1 Index 02_{HEX} bit[2:0], Bank2 Index 02_{HEX} bit[2:0], Bank9 Index 02_{HEX} bit[2:0], BankA Index 02_{HEX} bit[2:0].

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X_3 = \frac{(FanDuty4 / RPM 4) - (FanDuty3 / RPM 3)}{(T4 - T3)}$$

Fan Output:

$$\text{Target FanDuty or RPM} = (FanDuty3 \text{ or } RPM 3) + (Tx - T3) \cdot X_3$$

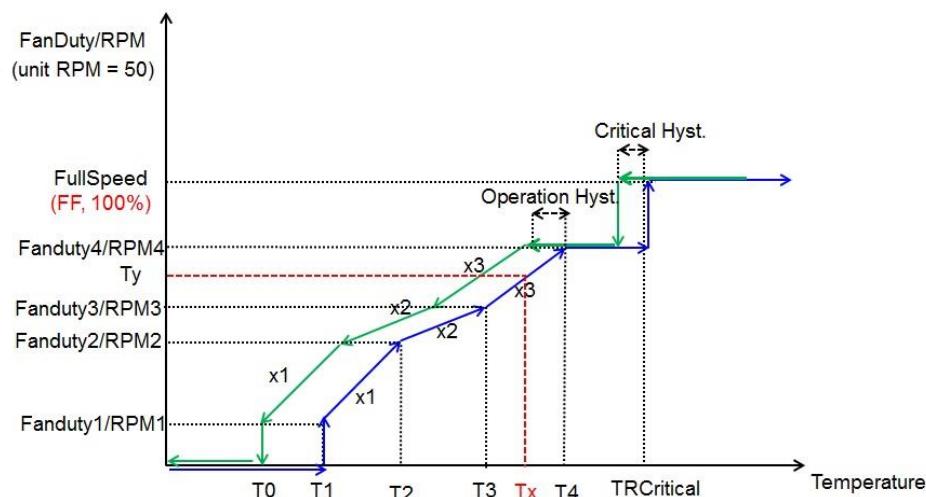


Figure 8-15 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-4 Relative Register-at SMART FAN™ IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 21h	Bank 1, Index 22h	Bank 1, Index 23h	Bank 1, Index 24h
DESCRIPTION	FD1/PWM1	FD2/PWM2	FD3/PWM3	FD4/PWM4
SYSFANOUT	Bank 1, Index 27h	Bank 1, Index 28h	Bank 1, Index 29h	Bank 1, Index 2Ah
CPUFANOUT	Bank 2, Index 21h	Bank 2, Index 22h	Bank 2, Index 23h	Bank 2, Index 24h
AUXFANOUT2	Bank 9, Index 21h	Bank 9, Index 22h	Bank 9, Index 23h	Bank 9, Index 24h
AUXFANOUT3	Bank A, Index 21h	Bank A, Index 22h	Bank A, Index 23h	Bank A, Index 24h

DESCRIPTION	CRITICAL TEMPERAT URE (TR Critical)	CRITICAL TOLERANCE (Critical Hyst)	TEMPERATURE TOLERANCE (Operation Hyst)	ENABLE RPM MODE	RPM TOLERANCE	ENABLE RPM HIGH MODE
SYSFANOUT	Bank 1, Index 35h	Bank 1, Index 38h, bit[2:0]	Bank 1, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit0	Bank 6, index 01h Bit[3:0]	Bank 6, Index 06h, Bit0
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 38h, bit[2:0]	Bank 2, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit1	Bank 6, index 02h Bit[3:0]	Bank 6, Index 06h, Bit1
AUXFANOUT2	Bank 9, Index 35h	Bank 9, Index 38h, bit[2:0]	Bank 9, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit4	Bank 6, index 05h Bit[3:0]	Bank 6, Index 06h, Bit4
AUXFANOUT3	Bank A, Index 35h	Bank A, Index 38h, bit[2:0]	Bank A, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit5	Bank 6, index 23h Bit[3:0]	Bank 6, Index 06h, Bit5

DESCRIPTION	STEP-	STEP-	STEP UP	STEP DOWN	Enable	ENABLE	CRITICAL

	UP TIME	DOWN TIME	VALUE	VALUE	SMART FAN IV	CRITICAL DUTY	DUTY
SYSFANOUT	Bank 1, index 03h	Bank 1, index 04h	Bank1, index66 Bit[7:4]	Bank1, index66 Bit[3:0]	Bank 1,Index 02h bit[7:4] = 04h	Bank 1, Index 36h, Bit0	Bank 1, index 37h
CPUFANOUT	Bank 2, index 03h	Bank 2, index 04h	Bank2, index66 Bit[7:4]	Bank2, index66 Bit[3:0]	Bank 2,Index 02h bit[7:4] = 04h	Bank 2, Index 36h, Bit0	Bank 2, index 37h
AUXFANOUT2	Bank 9, Index 03h	Bank 9, Index 04h	Bank9, index66 Bit[7:4]	Bank9, index66 Bit[3:0]	Bank 9,Index 02h bit[7:4] = 04h	Bank 9, Index 36h, Bit0	Bank 9, index 37h
AUXFANOUT3	Bank A, Index 03h	Bank A, Index 04h	BankA, index66 Bit[7:4]	BankA, index66 Bit[3:0]	Bank A,Index 02h bit[7:4] = 04h	Bank A, Index 36h, Bit0	Bank A, index 37h

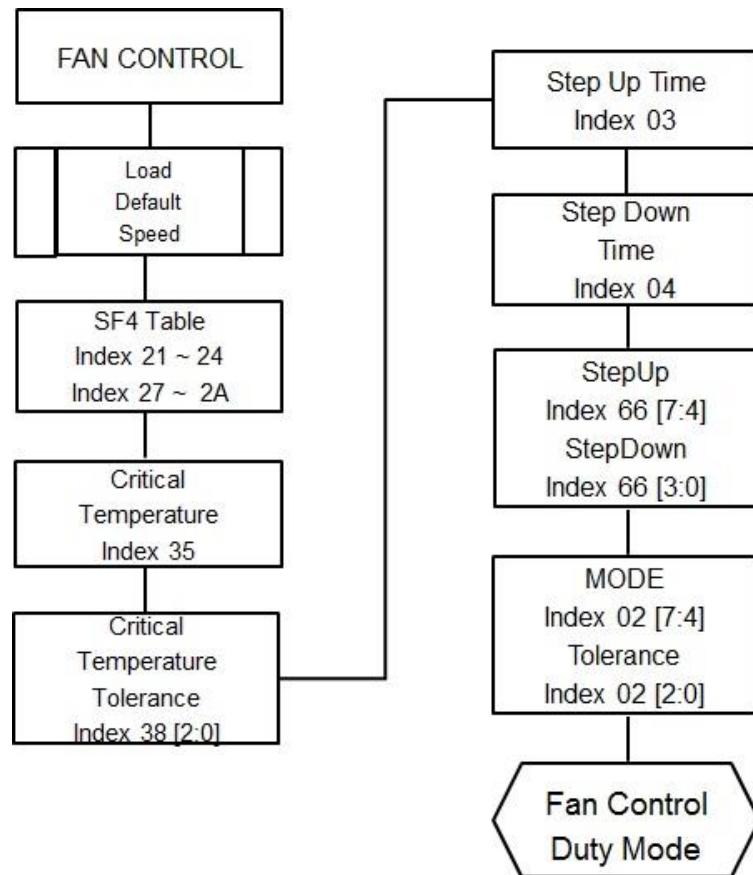


Figure 8-16 Fan Control Duty Mode Programming Flow

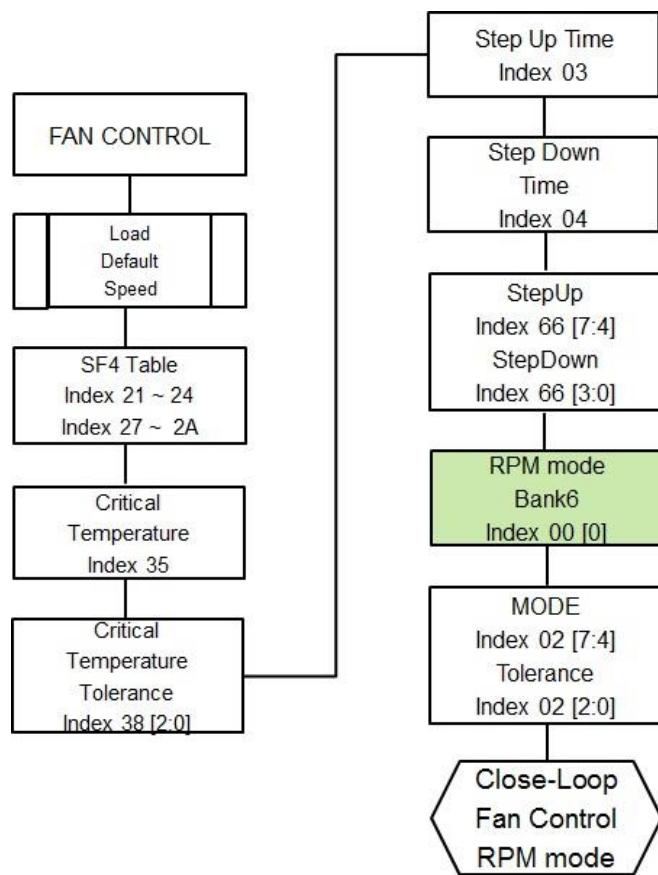


Figure 8-17 Close-Loop Fan Control RPM mode Programming Flow

8.10.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat.

8.10.2 Fan Output Step

The “Fanout Step” itself is separately specified in Bank1 Index20h bit0 for SYSFANOUT, Bank2 Index20h bit0 for CPUFANOUT, Bank9 Index20h bit0 for AUXFANOUT2, BankA Index20h bit0 for AUXFANOUT3.

This example for Fanout Step exposition:

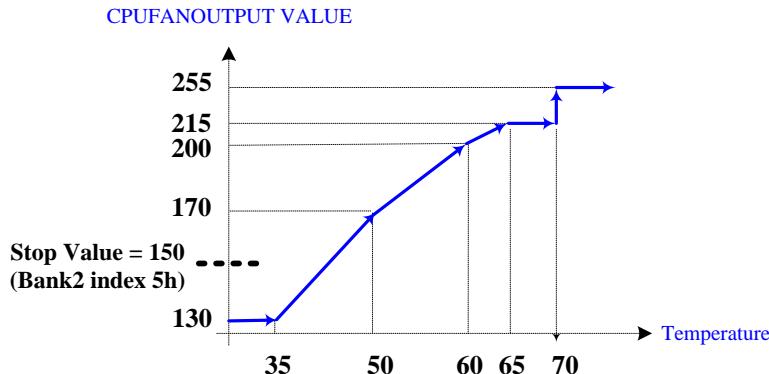


Figure 8-18 CPUFAN SMART FAN™ IV Table Parameters Figure

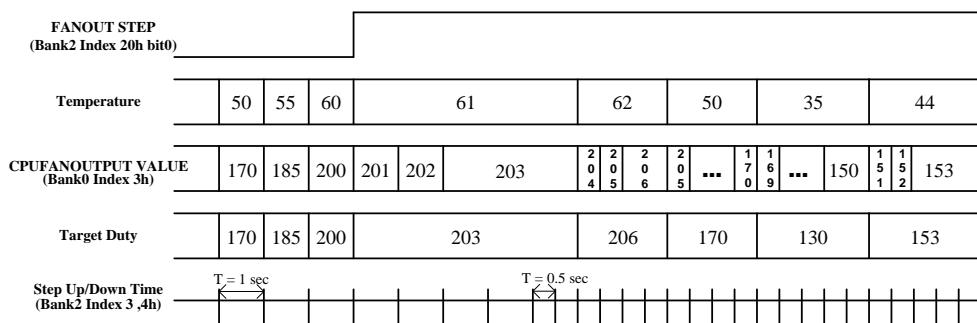


Figure 8-19 Fanout Step Relation of CPUFANOUT

8.10.3 Revolution Pulse Selection

The NCT5582D supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution. The others could be set by HM register at Bank6, Index44, Bit1-0 for SYSFANIN; Index45, Bit1-0 for CPUFANIN; Index48, Bit1-0 for AUXFANIN2; Index49, Bit1-0 for AUXFANIN3; Index4F. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for “Pulse Selection Bits”:

- 00:** 4 pulses per revolution
- 01:** 1 pulse per revolution
- 10:** 2 pulses per revolution (default)
- 11:** 3 pulses per revolution

8.10.4 Weight Value Control

The NCT5582D supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of SMART FAN™ I or IV and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

Figure 8-20 CPU TEMP and Weight Value Relations shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN

temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

Notes : This relative register should not be zero and not support negative temperature.

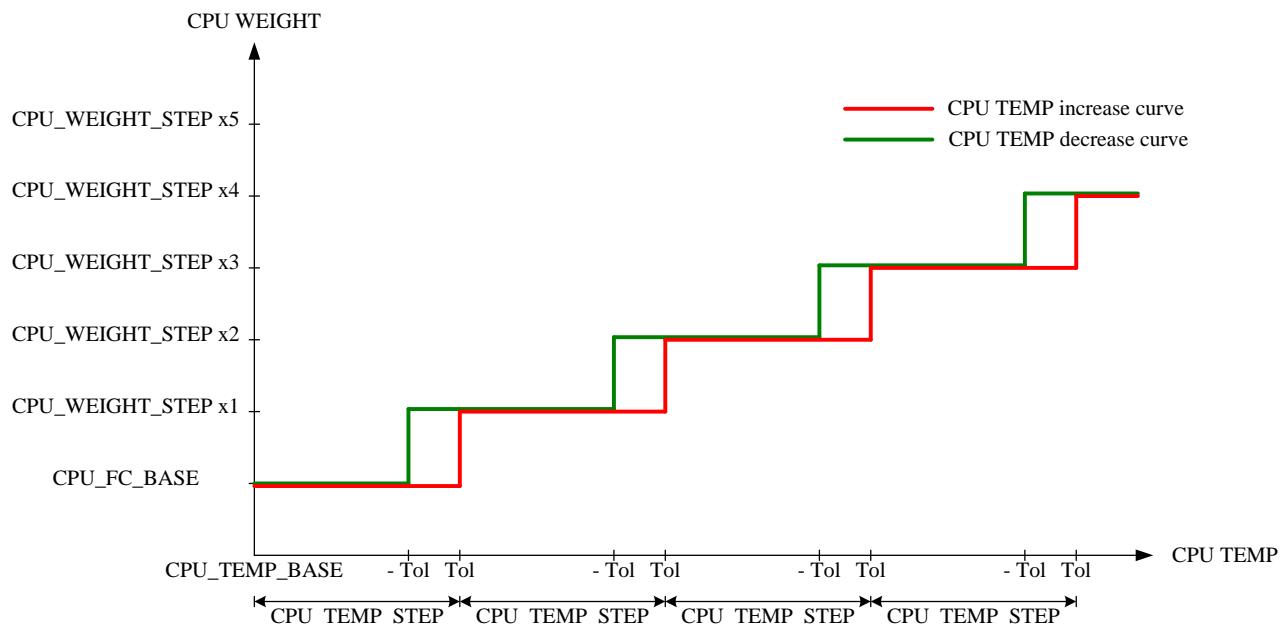


Figure 8-20 CPU TEMP and Weight Value Relations

Table 8-5 Relative Register-at Weight Value Control

DESCRIPTION	ENABLE WEIGHT MODE	WEIGHT TEMPERATURE SOURCE SELECT
CPUFANOUT	Bank 2, Index 39h, bit7	Bank 2, Index 39h, bit[4:0]

DESCRIPTION	TEMP BASE	DUTY BASE	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP
CPUFANOUT	Bank 2, Index 3Dh	Bank 2, Index 3Eh	Bank 2, Index 3Ah	Bank 2, Index 3Bh	Bank 2, Index 3Ch

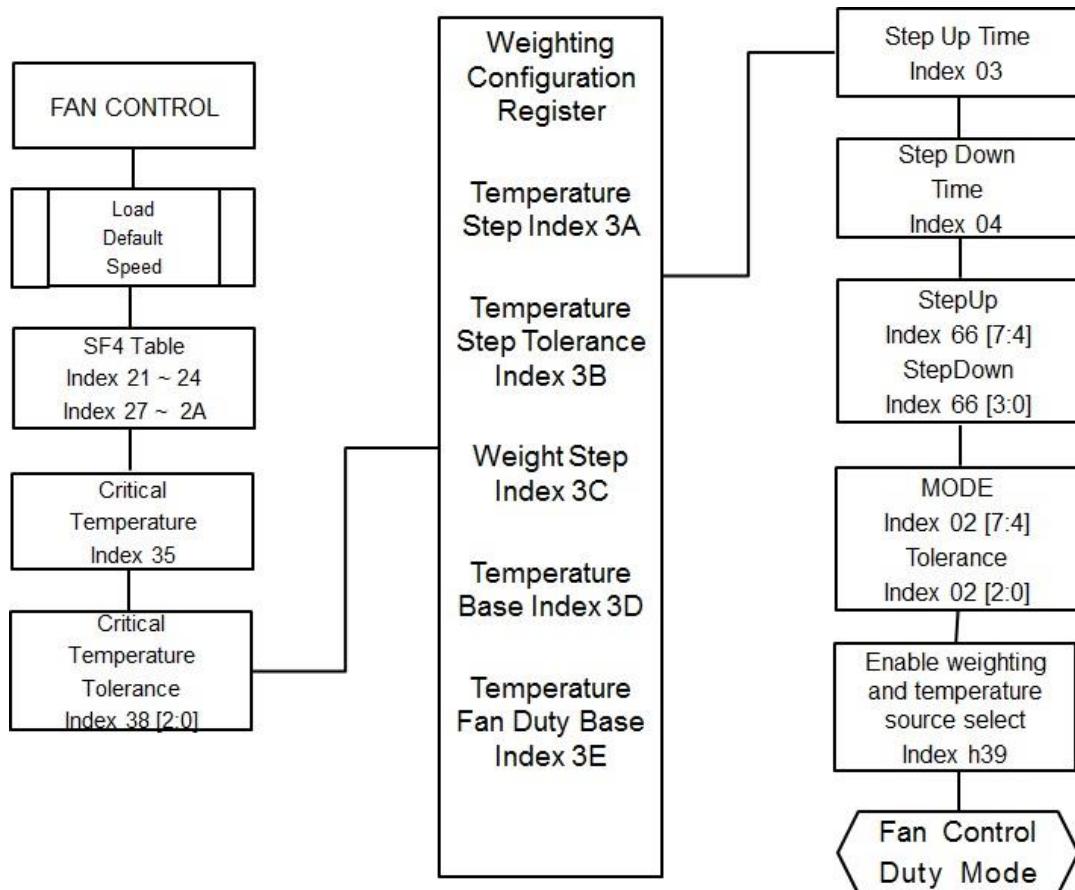


Figure 8-21 Fan Control Weighting Duty Mode Programming Flow

8.10.5 DTS2.0

When current temperature \geq Tcontrol, it will change from SMART FAN™ IV to DTS2.0, and when current temperature $<$ Tcontrol, it will change from DTS2.0 to SMART FAN™ IV. In DTS2.0, it compares the thermal margin (from PECI) and target thermal margin, when thermal margin $>$ target thermal margin, mean it's over-cooling and duty (RPM) will decrease, when thermal margin $<$ target thermal margin, mean it's poor-cooling and duty (RPM) increase.

Enable thermal margin and $T \geq T_{control}$, thermal margin correspond to duty (RPM) as follow figures

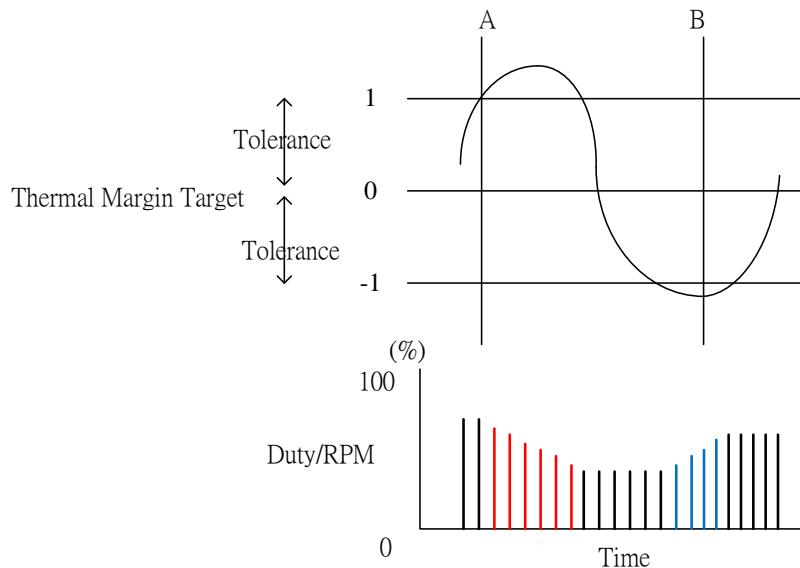


Figure 8-22 (a) Mechanism of thermal Margin

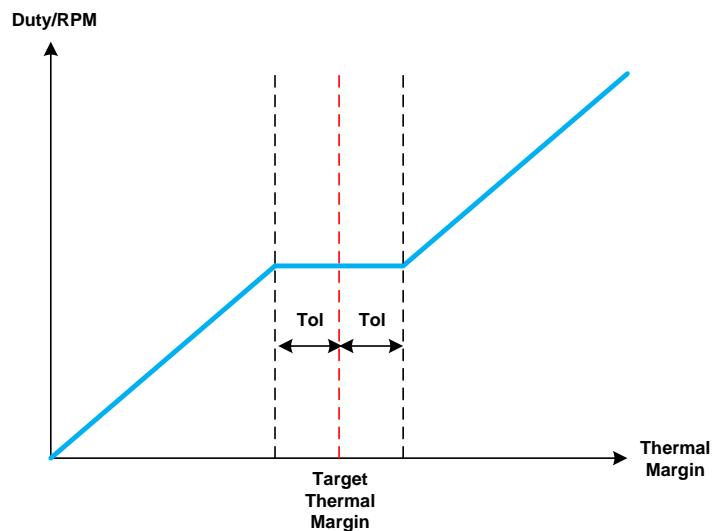


Figure 8-23 (b) Mechanism of thermal Margin

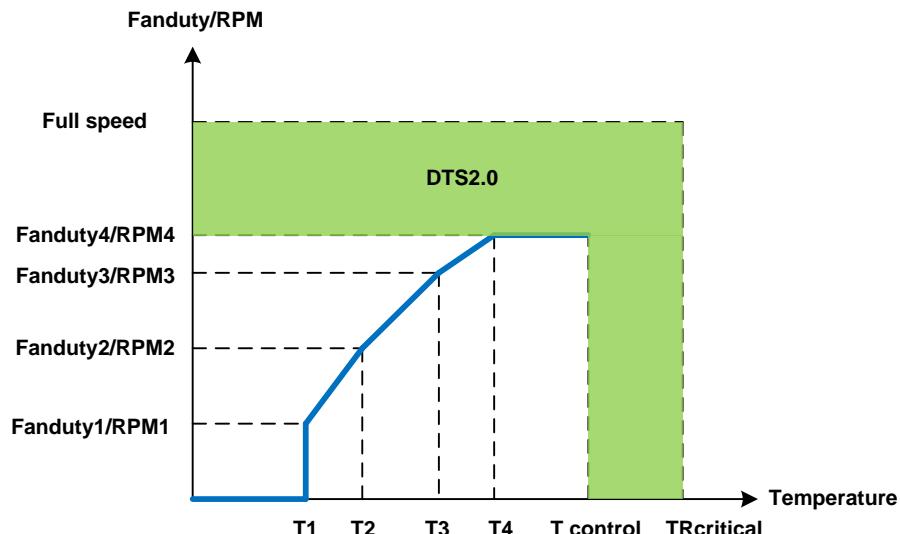


Figure 8-24 DTS2.0 region of SMART FAN™ IV

Table 8-6 Relative Registers – at DTS2.0

DESCRIPTION	THERMAL MARGIN ENABLE	T CONTROL	TARGET THERMAL MARGIN	THERMAL MARGIN TOLERANCE
CPUFANOUT	Bank 2, index 0Dh Bit[0]	Bank 2, index 0Fh	Bank2, index01	Bank2, index0D Bit[4:2]

8.10.6 Profile switch

The NCT5582D support SMART FAN™ IV dynamic switch the parameter of profile. This function can be enabled by selected the index_1C, bit7 of Bank1, Bank2, Bank3, Bank8, Bank9, BankA and BankB. When the temperature is greater or equal to the $T_{pf} + Thyst$, the parameter of profile will be into profile2, and the temperature is less than $T_{pf} - Thyst$, the parameter of profile will be into profile1, the detail operation sequence are shown in Figure 8-25 and Figure 8-26.

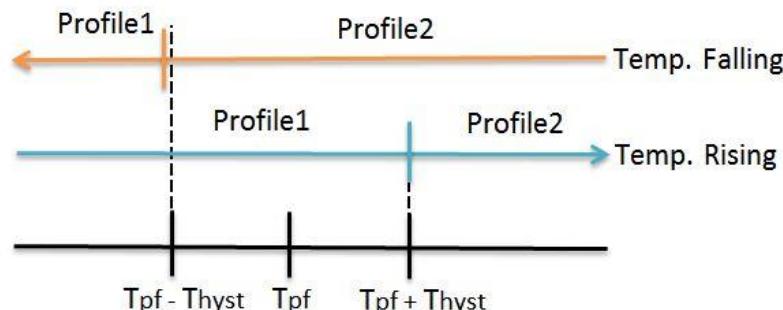


Figure 8-25 Profile Switching of SMART FAN™ IV

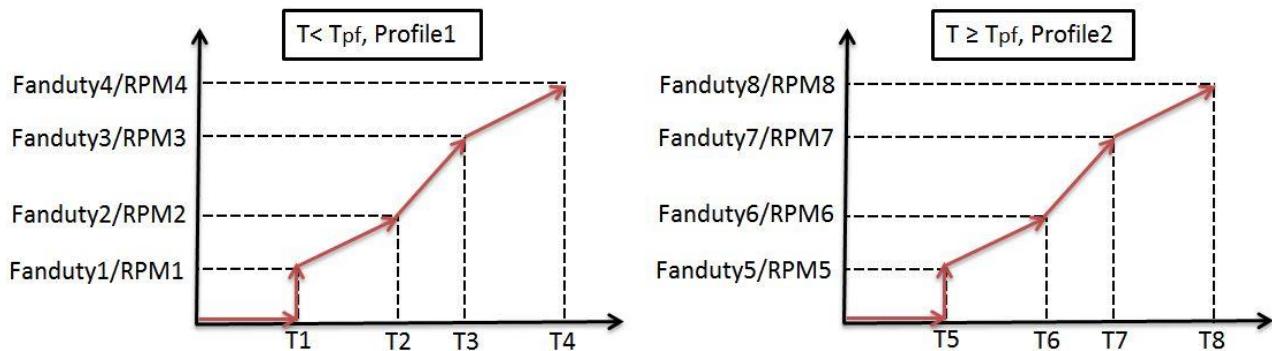


Figure 8-26 Parameter of Profile1 and Profile2 for SMART FAN™ IV

DESCRIPTION	T5	T6	T7	T8	T _{PF}
CPUFANOUT	Bank 2, Index 11h	Bank 2, Index 12h	Bank 2, Index 13h	Bank 2, Index 14h	Bank 2, Index 1Bh

DESCRIPTION	FD5/PWM5	FD6/PWM6	FD7/PWM7	FD8/PWM8	Enable / THYST
CPUFANOUT	Bank 2, Index 17h	Bank 2, Index 18h	Bank 2, Index 19h	Bank 2, Index 1Ah	Bank 2, Index 1Ch, bit7 / bit3-0(THYST)

8.10.7 Duty control

In SMART FANTM IV, the fan will be useless when the driven duty is smaller than the net friction torque. In order to solve this problem, the duty control will driven high duty to overcome net friction torque, and make fan working normly. The procedure of duty control is shown in Figure 8-27.

-Detect the frequency of fan stop running : User can defined the frequency of no fanin count. When the no fanin counts is satisfied the user defined, the driven duty will enable.

-Driven the specified duty : the specified duty value can be defined by user. When enable the driven duty, the duty hold timer is start working, until the count end of timer and release the duty control to SMART FANTM IV.

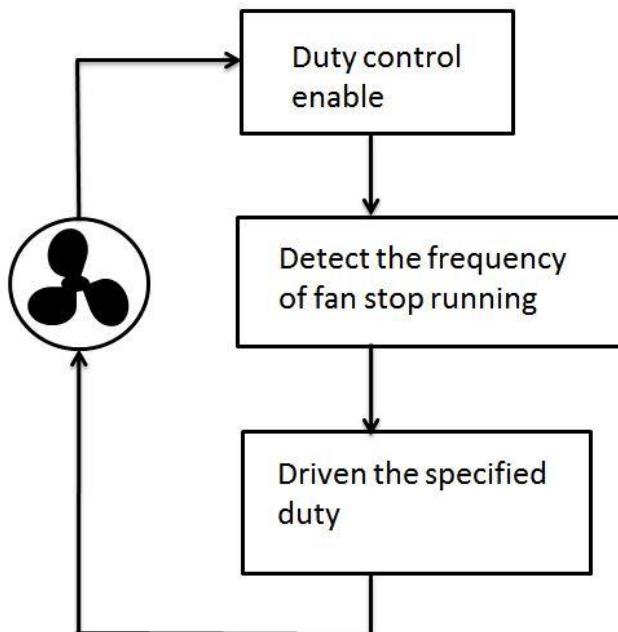


Figure 8-27 Procedure of duty control for SMART FAN™ IV

DESCRIPTION	Specified duty	Frequency count setting	Duty hold time	Duty control enable
SYSFANOUT	Bank C, Index 3Eh	Bank C, Index 3Dh, bit2-0	Bank C, Index 3Dh, bit6-4	Bank C, Index 3Dh, bit7
CPUFANOUT	Bank C, Index 40h	Bank C, Index 3Fh, bit2-0	Bank C, Index 3Fh, bit6-4	Bank C, Index 3Fh, bit7
AUXFANOUT2	Bank C, Index 46h	Bank C, Index 45h, bit2-0	Bank C, Index 45h, bit6-4	Bank C, Index 45h, bit7
AUXFANOUT3	Bank C, Index 48h	Bank C, Index 47h, bit2-0	Bank C, Index 47h, bit6-4	Bank C, Index 47h, bit7

8.11 Alert and Interrupt

NCT5582D supports 6 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4
Temperature source select	Bank6, index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default: CPUTIN	BankC, index26 bit[4:0] default:	BankC, index27 bit[4:0] default:
Temperature	Bank0,	Bank1,	Bank6,	Bank6,

reading (2's complement)	index27	index50 & index51 bit7	index70	index72
Temperature High Limit (TOL)	Bank0, index39	Bank1, index55 & index56 bit7	BankC, index1A	BankC, index1B
Temperature Low Limit (THTST)	Bank0, index3A	Bank1, index53 & index54 bit7	BankC, index20	BankC, index21

	SMIOVT5	SMIOVT6	SMIOVT7	SMIOVT8
Temperature source select	BankC, index28 bit[4:0] default:	BankC, index29 bit[4:0] default:	BankC, index2A bit[4:0] default:	BankC, index2B bit[4:0] default: CPUTIN
Temperature reading (2's complement)	Bank6, index74	Bank6, index76	Bank6, index78	Bank6, index7A
Temperature High Limit (TOL)	BankC, index1C	BankC, index1D	BankC, index1E	BankC, index1F
Temperature Low Limit (THTST)	BankC, index22	BankC, index23	BankC, index24	BankC, index25

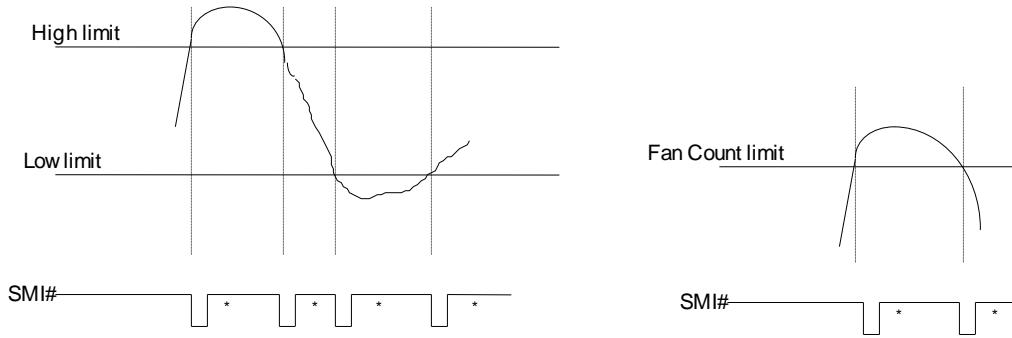
SMIOVT Relative Temperature Registers

8.11.1 SMI# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in HM_SMI# mode or in OVT# mode by setting Configuration Register CR24h, bit 2. In HM_SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.11.2 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage rises above a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-28 SMI Mode of Voltage and Fan Inputs

8.11.3 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.11.4 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN.

Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)

Temperature Sensor 3 SMI# Interrupt

Temperature Sensor 4 SMI# Interrupt

Temperature Sensor 5 SMI# Interrupt

Temperature Sensor 6 SMI# Interrupt

Temperature Sensor 7 SMI# Interrupt

Temperature Sensor 8 SMI# Interrupt (Default: CPUTIN)

The SMI# pin has four interrupt modes with Temperature Sensor 1, Sensor 3, Sensor 4, Sensor 5, Sensor 6, Sensor 7, and Sensor 8.

(1) Shut-down Interrupt Mode

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL} , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL} , until the temperature falls below T_{HYST} . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

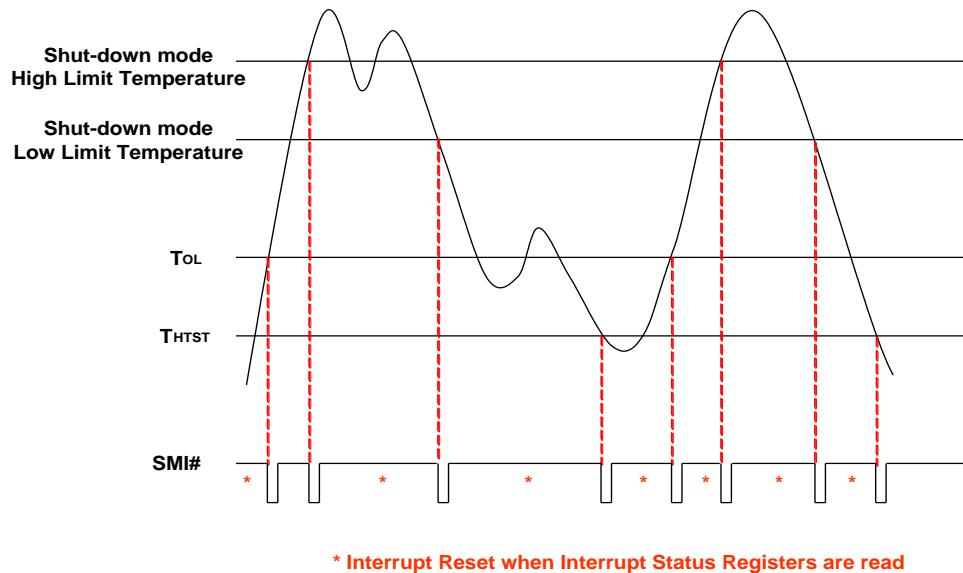


Figure 8-29 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature rises above T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O . This is illustrated in the figure below.

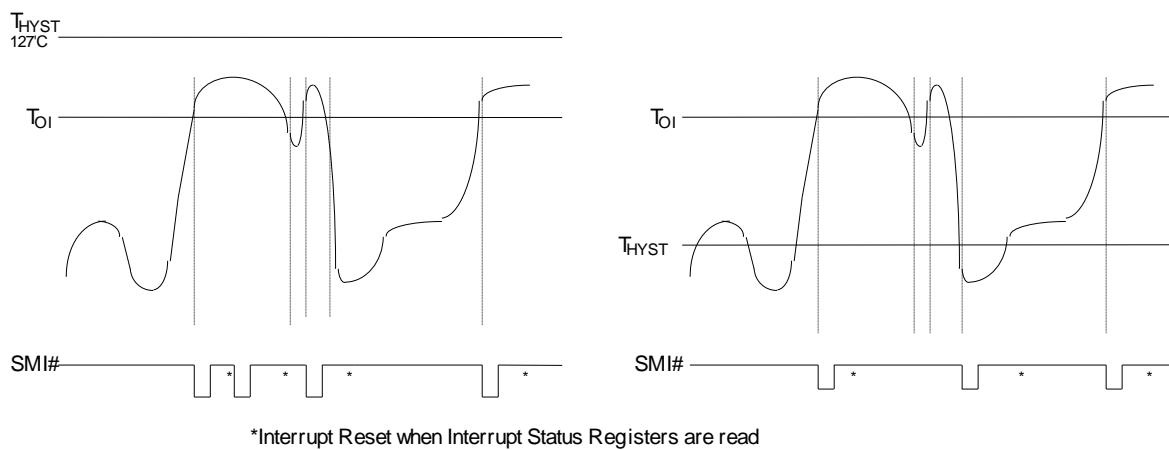


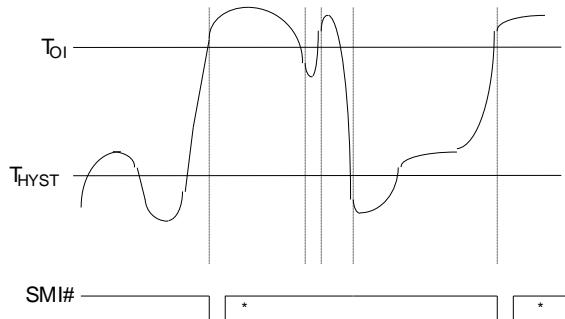
Figure 8-30 SMI Mode of Sensor1 I

(3) Two-Times Interrupt Mode

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST} . Once the temperature rises above T_O , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O , until the temperature falls below T_{HYST} . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(4) One-Times Interrupt Mode

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{O1} . Once the temperature rises above T_{O1} , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{O1} , until the temperature falls below T_{HYST} . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-31 SMI Mode of Sensor1 II

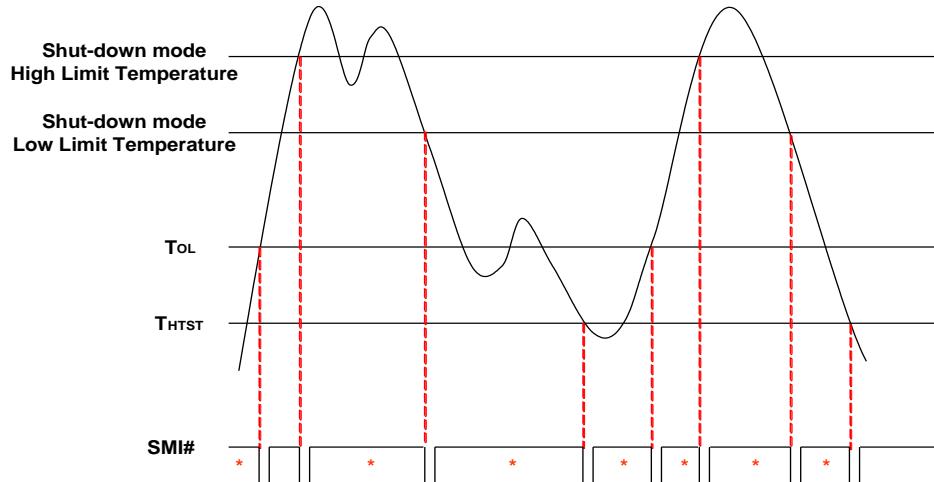
8.11.4.1. SMI# Interrupt of Temperature Sensor 2

The SMI# pin has 3 interrupt modes with Temperature Sensor 2.

(1) Shut-down Interrupt Mode

This mode is enabled by Bank0 Index 40h, bit5 to one for Temperature Sensor 2.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL} , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL} , until the temperature falls below T_{HYST} . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.



* Interrupt Reset when Interrupt Status Registers are read

Figure 8-32 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST} . This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.

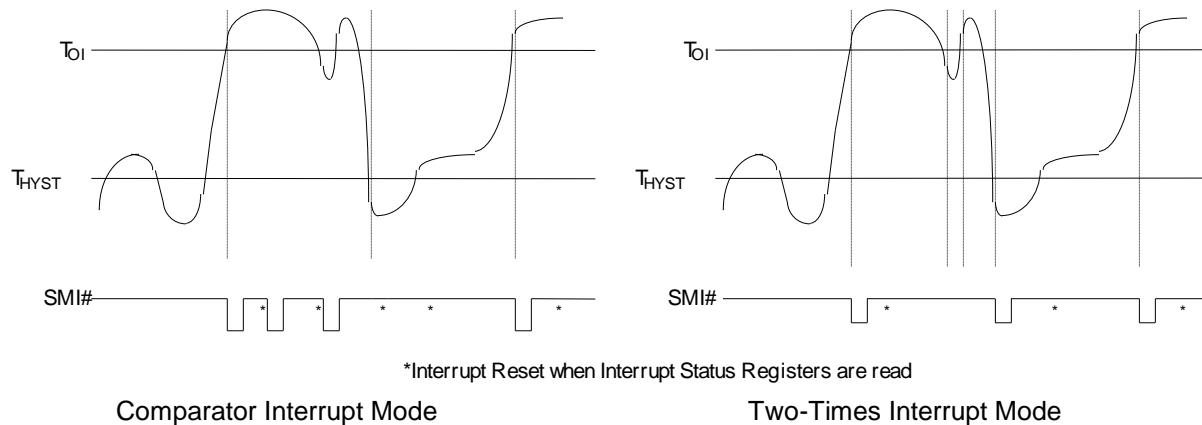


Figure 8-33 SMI Mode of Sensor2

(3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST} . Once the temperature rises above T_O , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O , until the temperature falls below T_{HYST} . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Table 8-7 Relative Register of SMI functions

	SHUTDOWN MODE	COMPARATOR MODE	TWO-TIME INTERRUPT MODE	ONE-TIME INTERRUPT MODE
SMIOVT1	Bank0,Index40_Bit4 (EN_WS=1) Bank0,Index43_Bit4(TIN=0) Bank0,Index46_Bit3 (Shut = 0)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index3A (Thyst = 8'h7F)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index4C_Bit5 (EN_T1_One = 0)	Bank0,Index43_Bit4 Bank0,Index4C_Bit5
SMIOVT2	Bank0,Index40_Bit5 (EN_WS=1) Bank0,Index43_Bit5(TIN=0) Bank0,Index46_	Bank0,Index43_Bit5 (TIN=0) Bank0,Index4C_Bit6 (T2T3_INT=1)	Bank0,Index43_Bit5(TIN=0) Bank0,Index4C_Bit6 (T2T3_INT=0)	

	Bit 4 (Shut = 0)			
SMIOVT3	BankC,Index09_Bit0(EN_WS=1) BankC,Index04_Bit0(TIN=0) BankC,Index05_Bit0(Shut = 0)	BankC,Index04_Bit0(TIN=0) BankC,Index20(Thyst = 8'h7F)	BankC,Index04_Bit0(TIN=0) BankC,Index0A_Bit2 (EN_T3_One = 0)	BankC,Index04_Bit0(TIN=0) BankC,Index0A_Bit2 (EN_T3_One = 1)
SMIOVT4	BankC,Index09_Bit1(EN_WS=1) BankC,Index04_Bit1(TIN=0) BankC,Index05_Bit1(Shut = 0)	BankC,Index04_Bit1(TIN=0) BankC,Index21(Thyst = 8'h7F)	BankC,Index04_Bit1(TIN=0) BankC,Index0A_Bit3 (EN_T4_One = 0)	BankC,Index04_Bit1(TIN=0) BankC,Index0A_Bit3 (EN_T4_One = 1)
SMIOVT5	BankC,Index09_Bit2(EN_WS=1) BankC,Index04_Bit2(TIN=0) BankC,Index05_Bit2(Shut = 0)	BankC,Index04_Bit2(TIN=0) BankC,Index22(Thyst = 8'h7F)	BankC,Index04_Bit2(TIN=0) BankC,Index0A_Bit4 (EN_T5_One = 0)	BankC,Index04_Bit2(TIN=0) BankC,Index0A_Bit4 (EN_T5_One = 1)
SMIOVT6	BankC,Index09_Bit3(EN_WS=1) BankC,Index04_Bit3(TIN=0) BankC,Index05_Bit3(Shut = 0)	BankC,Index04_Bit3(TIN=0) BankC,Index23(Thyst = 8'h7F)	BankC,Index04_Bit3(TIN=0) BankC,Index0A_Bit5 (EN_T6_One = 0)	BankC,Index04_Bit3(TIN=0) BankC,Index0A_Bit5 (EN_T6_One = 1)
SMIOVT7	BankC,Index09_Bit4(EN_WS=1) BankC,Index04_Bit4(TIN=0) BankC,Index05_Bit4(Shut = 0)	BankC,Index04_Bit4(TIN=0) BankC,Index24(Thyst = 8'h7F)	BankC,Index04_Bit4(TIN=0) BankC,Index0A_Bit6 (EN_T7_One = 0)	BankC,Index04_Bit4(TIN=0) BankC,Index0A_Bit6 (EN_T7_One = 1)
SMIOVT8	BankC,Index09_Bit5(EN_WS=1) BankC,Index04_Bit5(TIN=0) BankC,Index05_Bit5(Shut = 0)	BankC,Index04_Bit5(TIN=0) BankC,Index25(Thyst = 8'h7F)	BankC,Index04_Bit5(TIN=0) BankC,Index0A_Bit7 (EN_T8_One = 0)	BankC,Index04_Bit5(TIN=0) BankC,Index0A_Bit7 (EN_T8_One = 1)

Table 8-8 Relative Register of OVT functions

SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4
Bank0,Index18_Bit6=0 0: Enable SMIOVT1 temperature sensor over temperature output 1: Disable SMIOVT1 temperature sensor over temperature output	Bank 0, Index4C_Bit 3 0: Enable SMIOVT2 temperature sensor over temperature output 1: Disable SMIOVT2 temperature sensor over temperature output	Bank C, Index06_Bit 0 0: Enable SMIOVT3 temperature sensor over temperature output 1: Disable SMIOVT3 temperature sensor over temperature output	Bank C, Index06_Bit 1 0: Enable SMIOVT4 temperature sensor over temperature output 1: Disable SMIOVT4 temperature sensor over temperature output
Bank0,Index18_Bit4 0: Comparator Mode (def.) 1: Interrupt Mode	Bank 1, Index52_Bit 1 0: Comparator Mode (def.) 1: Interrupt Mode	Bank C, Index07_Bit 0 0: Comparator Mode (def.) 1: Interrupt Mode	Bank C, Index07_Bit 1 0: Comparator Mode (def.) 1: Interrupt Mode
Bank0, Index18_Bit0 0: Start to monitor the source of SMIOVT1 temperature. 1: Stop monitoring the source of SMIOVT1 temperature.	Bank1, Index52_Bit0 0: Start to monitor the source of SMIOVT2 temperature. 1: Stop monitoring the source of SMIOVT2 temperature.	Bank C, Index08_Bit0 0: Start to monitor the source of SMIOVT3 temperature. 1: Stop monitoring the source of SMIOVT3 temperature.	Bank C, Index08_Bit1 0: Start to monitor the source of SMIOVT4 temperature. 1: Stop monitoring the source of SMIOVT4 temperature.
Bank 0, IndexBE_Bit 4~5 Number of faults to detect before setting OVT# output.	Bank 1, Index52_Bit 3~4 Number of faults to detect before setting OVT# output.	Bank C, Index0C_Bit 0~1 Number of faults to detect before setting OVT# output.	Bank C, Index0C_Bit 2~3 Number of faults to detect before setting OVT# output.

SMIOVT5	SMIOVT6	SMIOVT7	SMIOVT8
Bank C, Index06_Bit 2 0: Enable SMIOVT5 temperature sensor over temperature output 1: Disable SMIOVT5 temperature sensor over temperature output	Bank C, Index06_Bit 3 0: Enable SMIOVT6 temperature sensor over temperature output 1: Disable SMIOVT6 temperature sensor over temperature output	Bank C, Index06_Bit 4 0: Enable SMIOVT7 temperature sensor over temperature output 1: Disable SMIOVT7 temperature sensor over temperature output	Bank C, Index06_Bit 5 0: Enable SMIOVT8 temperature sensor over temperature output 1: Disable SMIOVT8 temperature sensor over temperature output
Bank C, Index07_Bit 2 0: Comparator Mode (def.) 1: Interrupt Mode	Bank C, Index07_Bit 3 0: Comparator Mode (def.) 1: Interrupt Mode	Bank C, Index07_Bit 4 0: Comparator Mode (def.) 1: Interrupt Mode	Bank C, Index07_Bit 5 0: Comparator Mode (def.) 1: Interrupt Mode
Bank C, Index08_Bit2 0: Start to monitor the source of SMIOVT5 temperature. 1: Stop monitoring the source of SMIOVT5 temperature.	Bank C, Index08_Bit3 0: Start to monitor the source of SMIOVT6 temperature. 1: Stop monitoring the source of SMIOVT6 temperature.	Bank C, Index08_Bit4 0: Start to monitor the source of SMIOVT7 temperature. 1: Stop monitoring the source of SMIOVT7 temperature.	Bank C, Index08_Bit5 0: Start to monitor the source of SMIOVT8 temperature. 1: Stop monitoring the source of SMIOVT8 temperature.
Bank C, Index0C_Bit 4~5 Number of faults to detect before setting OVT# output.	Bank C, Index0C_Bit 6~7 Number of faults to detect before setting OVT# output.	Bank C, Index0D_Bit 0~1 Number of faults to detect before setting OVT# output.	Bank C, Index0D_Bit 2~3 Number of faults to detect before setting OVT# output.

8.11.5 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[24h], bit 2 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and OVT pin could be enabled to OVT output by Bank0 Index 18h, bit 6 for Temperature Sensor 1(default: SYSTIN); Bank1 Index 52h, bit 1 for Temperature Sensor 2(default: CPUTIN) ; BankC Index 06h, bit 0 for Temperature Sensor 3; BankC Index 06h, bit 1 for Temperature Sensor 4; BankC Index 06h, bit 2 for Temperature Sensor 5; BankC Index 06h, bit 3 for Temperature Sensor 6; BankC Index 06h, bit 4 for Temperature Sensor 7.

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.

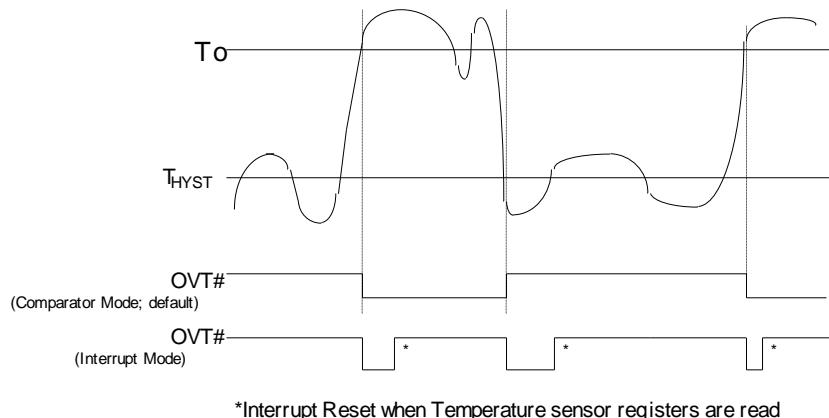


Figure 8-34 OVT# Modes of Temperature Inputs

In comparator mode, the OVT# pin can create an interrupt once the current temperature rises above T_O and continues to create interrupts until the temperature falls below T_{HYST} . The OVT# pin is asserted once the temperature has risen above T_O and has not yet fallen below T_{HYST} .

In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST} . Once the temperature rises above T_O , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O , until the temperature falls below T_{HYST} . This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.11.6 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possibly tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either VBAT or 3VSB. 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN0# must be pulled high by an externally pulled-up $2M\Omega$ resistor that is connected to VBAT. When the case is opened, CASEOPEN0# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The CASEOPEN0# status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to "1" first and then to "0".

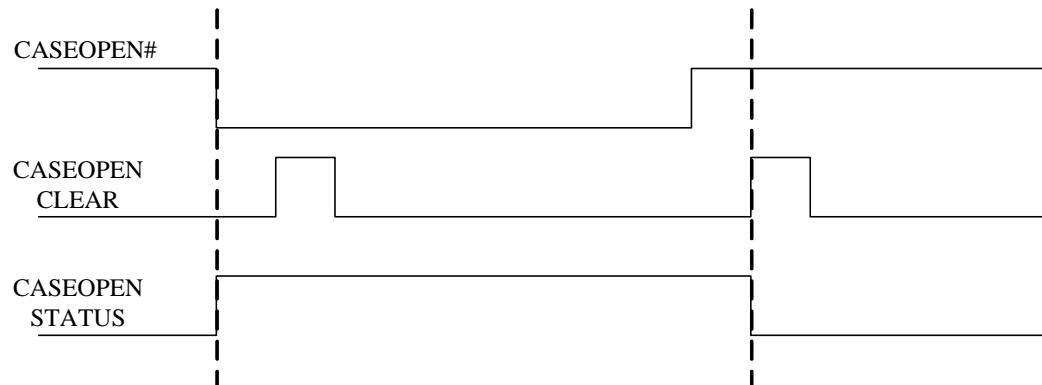


Figure 8-35 Caseopen Mechanism

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

NCT5582D added 91byte read-only registers for Hardware Monitor. The base address is specified in registers CR[64h] and CR[65h] of Logical Device B, the hardware monitor device. CR[64h] is the high byte, and CR[65h] is the low byte. The least byte of the base address recommend to be zero. For example, {CR[64h], CR[65h]} = {XX00h}.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at Bank0, index 04Eh.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7	RESERVED							
6-0	READ/WRITE.							

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	Data to be read from or to be written to Value RAM and Register.							

9.3 SYSFANOUT PWM Output Frequency Configuration Register – Index 00h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is programmed for PWM output (i.e., Bank0, Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select. This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider. The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.

If CKSEL equals 0, then the output clock is simply equal to **93.9/(Divisor[6:0]+1) KHz**

MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz			
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals 1, then the output clock is simply equal to **1008/ Mapped Divisor Hz**

MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.4 SYSFANOUT Output Value Select Register – Index 01h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. $\text{OUTPUT Voltage} = V_{ref} * \frac{FANOUT}{64}$ Note. VREF is approx. 2.048V.						Reserved	
This register could be programmed by Bank1, Index 09									

9.5 CPUFANOUT PWM Output Frequency Configuration Register – Index 02h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select. This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider. The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.

If CKSEL equals 0, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**

MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals 1, then the output clock is simply equal to **1008/ Mapped Divisor Hz**

MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.6 CPUFANOUT Output Value Select Register – Index 03h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0	
PWM Output	DESCRIPTION	CPUFANOUT PWM Duty. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.								
This register could be programmed by Bank2, Index 09										

9.7 SYSFANOUT Configuration Register I – Index 04h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
0	SYSFANOUT Output Mode Selection. 0: SYSFANOUT pin produces a PWM duty cycle output. (Default) 1: SYSFANOUT pin produces DC output.

9.8 AUXFANOUT2 PWM Output Frequency Configuration Register – Index 14h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_SCALE5							
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT2 is programmed for PWM output.

BIT	DESCRIPTION
7	PWM_CLK_SEL5. AUXFANOUT2 PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	PWM_CLK_SCALE5. AUXFANOUT2 PWM Pre-Scale divider. The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.

If CKSEL equals 0, then the output clock is simply equal to **93.9/(Divisor[6:0]+1) KHz**

MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz			
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals 1, then the output clock is simply equal to **1008/ Mapped Divisor Hz**

MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.9 AUXFANOUT2 Output Value Select Register – Index 15h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT2 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by Bank9, Index 09									

9.10 AUXFANOUT3 PWM Output Frequency Configuration Register – Index 16h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL6							
DEFAULT	0							

This register is only meaningful when AUXFANOUT3 is programmed for PWM output.

BIT	DESCRIPTION
7	PWM_CLK_SEL6. AUXFANOUT3 PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	PWM_CLK_SCALE6. AUXFANOUT3 PWM Pre-Scale divider. The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.

If CKSEL equals 0, then the output clock is simply equal to **93.9 / (Divisor[6:0]+1) KHz**

MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz			
0000001	2	46.95KHz			
0000010	3	31.3KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals 1, then the output clock is simply equal to **1008/ Mapped Divisor Hz**

MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.11 AUXFANOUT3 Output Value Select Register – Index 17h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT3 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by BankA, Index 09									

9.12 OVT# Configuration Register – Index 18h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
BIT	RESERVED	DIS_OVT1	RESERVED	OVT1_Mode	RESERVED			STOP
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION
0	

BIT	DESCRIPTION
7	Reserved
6	DIS_OVT1. 0: Enable SMIOVT1 OVT# output. (Default) 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output.
5	Reserved
4	OVT1_Mode. SMIOVT1 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.
3-1	Reserved
0	STOP. 0: Monitor SMIOVT1 temperature source. 1: Stop monitoring SMIOVT1 temperature source.

9.13 Value RAM — Index 27h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
27h	SMIOVT1 temperature source reading.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN1 High Limit
2Eh	VIN1 Low Limit
2Fh	AVSB High Limit
30h	AVSB Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN0 High Limit
34h	VIN0 Low Limit
35h - 38h	Reserved
39h	SMIOVT1 temperature sensor High Limit
3Ah	SMIOVT1 temperature sensor Hysteresis Limit

9.14 Configuration Register – Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	RESERVED	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION

BIT	DESCRIPTION
7	Initialization. A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	RESERVED
5	Output type of SMIOVT2: 1: SMI# output type of SMIOVT Source2 temperature (Default: CPUTIN) is Shut-down Interrupt Mode. 0: Depend on the value of Bank0, Index 4C, bit6.
4	Output type of SMIOVT1 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: Depend on the value of Bank0, Index 4C, bit5.
3	INT_Clear. A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	Reserved
1	SMI# Enable. A one enables the SMI# Interrupt output. 1: Enable SMI# function (Default) 0: Disable SMI# function
0	Start. A one enables startup of monitoring operations. A zero puts the part in standby mode. Note: Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.15 Interrupt Status Register 1 – Index 41h (Bank 0)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	SOURCE2 — SMI	SOURCE1 — SMI	3VCC	AVSB	VIN1	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	CPUFANIN. A one indicates the fan count limit of CPUFANIN has been exceeded.
6	SYSFANIN. A one indicates the fan count limit of SYSFANIN has been exceeded.
5	SMIOVT2. A one indicates the high limit of SMIOVT2 temperature has been exceeded. (CPUTIN is default temperature)
4	SMIOVT1. A one indicates the high limit of SMIOVT1 temperature has been exceeded. (SYSTIN is default temperature)
3	3VCC. A one indicates the high or low limit of 3VCC has been exceeded.
2	AVSB. A one indicates the high or low limit of AVSB has been exceeded.
1	VIN1. A one indicates the high or low limit of VIN1 has been exceeded.
0	CPUVCORE. A one indicates the high or low limit of CPUVCORE has been exceeded.

9.16 Interrupt Status Register 2 – Index 42h (Bank 0)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	CASEOPEN0	Reserved	Reserved	Reserved	VIN0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	Reserved
4	CASEOPEN0. A one indicates the case has been opened.
3	Reserved
2	Reserved
1	Reserved
0	VIN0. A one indicates the high or low limit of VIN0 has been exceeded.

9.17 SMI# Mask Register 1 – Index 43h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	SMIOVT2	SMIOVT1	3VCC	AVSB	VIN1	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7	CPUFANIN.
6	SYSFANIN.
5	SMIOVT2.
4	SMIOVT1.
3	3VCC.
2	AVSB.
1	VIN1.
0	CPUVCORE.

A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))

9.18 SMI# Mask Register 2 – Index 44h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	Reserved	CASEOPEN0	Reserved	Reserved	Reserved	VIN0

DEFAULT	1	1	0	1	1	1	1	1
---------	---	---	---	---	---	---	---	---

BIT	DESCRIPTION
7	TAR2.
6	TAR1.
5	Reserved
4	CASEOPEN0.
3	Reserved
2	Reserved
1	Reserved
0	VIN0.

9.19 Interrupt Status Register 4 – Index 45h (Bank 0)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	CPU FANOUT	SYS FANOUT	Reserved	Shut_SOURCE2_SMI	Shut_SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	Reserved
4	CPUFANOUT. "1" indicates that CPUFANOUT works for three minutes at the full fan speed.
3	SYSFANOUT. "1" indicates that SYSFANOUT works for three minutes at the full fan speed.
2	Reserved
1	Shut_SOURCE2_SMI. "1" indicates the high limit of SMIOVT_SOURCE2 temperature of SMI# Shutdown mode has been exceeded. (CPUTIN is default temperature)
0	Shut_SOURCE1_SMI. "1" indicates the high limit of SMIOVT_SOURCE1 temperature of SMI# Shutdown mode has been exceeded. (SYSTIN is default temperature)

9.20 SMI# Mask Register 3 – Index 46h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	AUXFANIN3	Shut_CPU	Shut_SYS	AUXFANIN2	Reserved	Reserved
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION							
7	CASEOPEN0 Clear Control. Writing 1 to this bit will clear CASEOPEN0 status. This bit will be cleared itself. The function is the same as LDA, CR[E6h], bit 5.							
6	Reserved							
5	AUXFANIN3							
4	Shut_SOURCE2_SMI							
3	Shut_SOURCE1_SMI							
2	AUXFANIN2							
1	Reserved							
0	Reserved							

9.21 Serial Bus Address Register – Index 48h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SERIAL BUS ADDRESS							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION							
7	Reserved							
6-0	Serial Bus Address <7:1>							

9.22 SMI/OVT Control Register1 – Index 4Ch (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	T2ToT6_INT MODE	EN_T1 _ONE	RESERVED	DIS_OVT2	OVTOL	RESERVED	
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION							

BIT	DESCRIPTION
7	Reserved
6	T2ToT6_INTMode. 1: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Comparator Interrupt mode. 0: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Two-Times Interrupt mode. (Default)
5	EN_T1_ONE. 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default)
4	Reserved
3	DIS_OVT2. 1: Disable SMIOVT Source2 temperature sensor (Default: CPUTIN) over-temperature (OVT) output. 0: Enable SMIOVT Source2 temperature OVT output through pin OVT#. (Default)
2	OVTPOL (Over-temperature polarity). 1: OVT# is active high. 0: OVT# is active low (Default).
1-0	Reserved

9.23 FAN IN/OUT Control Register – Index 4Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION
7-4	Reserved
3	FANOPV2. CPUFANIN output value , only if bit 2 is set to zero. 1: CPUFANIN generates a logic-high signal. 0: CPUFANIN generates a logic-low signal. (Default)
2	FANINC2. CPUFANIN Input Control. 1: CPUFANIN acts as a fan tachometer input. (Default) 0: CPUFANIN acts as a fan control signal, and the output value is set by bit 3.
1	FANOPV1. SYSFANIN output value , only if bit 0 is set to zero. 1: SYSFANIN generates a logic-high signal. 0: SYSFANIN generates a logic-low signal. (Default)
0	FANINC1. SYSFANIN Input Control. 1: SYSFANIN acts as a fan tachometer input. (Default) 0: SYSFANIN acts as a fan control signal, and the output value is set by bit 1.

9.24 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserved			BANK SEL3	BANK SEL2	BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	HBACS. HBACS – High Byte Access. 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.
6	Reserved
5	Reserved
4	Reserved
3	BANKSEL3.
2	BANKSEL2.
1	BANKSEL1.
0	BANKSEL0.

9.25 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only

Size: 16 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	Vendor ID High-Byte , if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	Vendor ID Low-Byte , if Index 4Eh, bit 7 is 0. Default A3h.

9.26 FAN IN/OUT Control Register – Index 50h (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

Bit	7	6	5	4	3	2	1	0	
NAME	Reserved					FANOPV6	FANINC6	FANOPV5	FANINC5

	Reserved Reserved							
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-4	Reserved
3	FANOPV6. AUXFANIN3 output value , only if bit 0 is set to zero. 1: AUXFANIN3 generates a logic-high signal. 0: AUXFANIN3 generates a logic-low signal. (Default)
2	FANINC6. AUXFANIN3 Input Control. 1: AUXFANIN3 acts as a fan tachometer input. (Default) 0: AUXFANIN3 acts as a fan control signal, and the output value is set by bit 1.
1	FANOPV5. AUXFANIN2 output value , only if bit 0 is set to zero. 1: AUXFANIN2 generates a logic-high signal. 0: AUXFANIN2 generates a logic-low signal. (Default)
0	FANINC5. AUXFANIN2 Input Control. 1: AUXFANIN2 acts as a fan tachometer input. (Default) 0: AUXFANIN2 acts as a fan control signal, and the output value is set by bit 1.

9.27 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only

Size: 16 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	15	14	13	12	11	10	9	8
NAME								
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME								
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	Vendor ID High-Byte , if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	Vendor ID Low-Byte , if Index 4Eh, bit 7 is 0. Default A3h.

9.28 Chip ID – Index 58h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME								
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.29 VBAT Monitor Control Register – Index 5Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	DIODES 2. Sensor type selection for CPUTIN. 1: Diode sensor. (default) 0: Thermistor sensor.
1	DIODES 1. Sensor type selection for SYSTIN. 1: Diode sensor. 0: Thermistor sensor. (default)
0	EN_VBAT_MNT. 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.30 Current Mode Enable Register – Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	EN_CPUTIN_CURRENT_MODE	EN_SYSTIN_CURRENT_MODE	Reserved
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	Reserved

BIT	DESCRIPTION
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Enable CPUTIN Current Mode. With CPUTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 2 = 1). 1: Temperature sensing of CPUTIN by Current mode. (Default) 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	Enable SYSTIN Current Mode. With SYSTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 1 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. (Default)
0	Reserved

9.31 CPUVCORE DE_NEGATIVE Register – Index 5F (Bank 0)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Rerserved.							De_negative
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-1	Rerseved
0	De-negative ; 1: cpuvcore will not show negative value. 0: cpuvcore will show negative value.

9.32 PORT 80 DATA INPUT Register – Index 60 (Bank 0)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	P80_IN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	PORT 80 DATA INPUT

9.33 MONITOR TEMPERATURE 1 Register (Integer Value)- Index 73h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	MONITOR TEMPERATURE 1 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	MONITOR TEMPERATURE 1 [8:1] SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])

9.34 MONITOR TEMPERATURE 1 Register (Fractional Value)- Index 74h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 1 [0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	MONITOR TEMPERATURE 1 [0] SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])
6-0	Reserved

9.35 MONITOR TEMPERATURE 2 Register (Integer Value)- Index 75h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 2 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	MONITOR TEMPERATURE 2 [8:1] CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])

9.36 MONITOR TEMPERATURE 2 Register (Fractional Value)- Index 76h (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 2							
DEFAULT	0	0	0	0	0	0	0	0

	[0]								
DEFAULT	0	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	MONITOR TEMPERATURE 2 [0] CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])
6-0	Reserved

9.37 MONITOR TEMPERATURE 5 Register (Integer Value)- Index 7Bh (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 5 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	MONITOR TEMPERATURE 5 [8:1] AUXFANOUT2 fan control temperature reading. (Source is selected by Bank9, Index00 bit[4:0])

9.38 MONITOR TEMPERATURE 5 Register (Fractional Value)- Index 7Ch (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 5 [0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	MONITOR TEMPERATURE 5 [0] AUXFANOUT2 fan control temperature reading. (Source is selected by Bank9, Index00 bit[4:0])
6-0	Reserved

9.39 MONITOR TEMPERATURE 6 Register (Integer Value)- Index 7Dh (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 6 [8:1]							

DEFAULT	0	0	0	0	0	0	0	0
---------	---	---	---	---	---	---	---	---

BIT	DESCRIPTION
7-0	MONITOR TEMPERATURE 6 [8:1] AUXFANOUT3 fan control temperature reading. (Source is selected by BankA, Index00 bit[4:0])

9.40 MONITOR TEMPERATURE 6 Register (Fractional Value)- Index 7Eh (Bank 0)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0	
NAME	MONITOR TEMPERATURE 6 [0]	Reserved							
DEFAULT	0	0	0	0	0	0	0	0	

BIT	DESCRIPTION
7	MONITOR TEMPERATURE 6 [0] AUXFANOUT3 fan control temperature reading. (Source is selected by BankA, Index00 bit[4:0])
6-0	Reserved

9.41 PECL Temperature Reading Enable for SMIOVT and SMART FAN Control Register – Index Aeh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_PECI1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	Reserved
1	Enable PECL Agent1
0	Enable PECL Agent0

Note. If the temperature source is selecting to PECL, please set Bank0 Index Aeh first for reading correct value.

9.42 BEEP Control Register 1 – Index B2h (Bank0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	En3VSB_BP	Reserved	Reserved	EnVIN0_BP	En3VCC_BP	EnAVSB_BP	EnVIN1_BP	EnCPUVCORE_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	En3VSB_BP 1 : Enable 3VSB Beep function 0 : Disable 3VSB Beep function
6	Reserved
5	Reserved
4	EnVIN0_BP 1 : Enable VIN0 Beep function 0 : Disable VIN0 Beep function
3	En3VCC_BP 1 : Enable 3VCC Beep function 0 : Disable 3VCC Beep function
2	EnAVSB_BP 1 : Enable AVSB Beep function 0 : Disable AVSB Beep function
1	EnVIN1_BP 1 : Enable VIN1 Beep function 0 : Disable VIN1 Beep function
0	EnCPUVCORE_BP 1 : Enable CPUVCORE Beep function 0 : Disable CPUVCORE Beep function

9.43 BEEP Control Register 2 – Index B3h (Bank0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EnVIN9_BP	Reserved	Reserved	Reserved	Reserved	Reserved	EnVTT_BP	EnVBAT_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	EnVIN9_BP 1 : Enable VIN9 Beep function 0 : Disable VIN9 Beep function
6	Reserved
5	Reserved
4	Reserved
3	Reserved

BIT	DESCRIPTION
2	Reserved
1	EnVTT_BP 1 : Enable VTT Beep function 0 : Disable VTT Beep function
0	EnVBAT_BP 1 : Enable VBAT Beep function 0 : Disable VBAT Beep function

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.44 BEEP Control Register 3 – Index B4h (Bank0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EnT8 _BP	EnT7 _BP	EnT6 _BP	EnT5 _BP	EnT4 _BP	EnT3 _BP	EnT2 _BP	EnT1 _BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	EnT8_BP 1 : Enable SMIOVT8 Beep function 0 : Disable SMIOVT8 Beep function
6	EnT7_BP 1 : Enable SMIOVT7 Beep function 0 : Disable SMIOVT7 Beep function
5	EnT6_BP 1 : Enable SMIOVT6 Beep function 0 : Disable SMIOVT6 Beep function
4	EnT5_BP 1 : Enable SMIOVT5 Beep function 0 : Disable SMIOVT5 Beep function
3	EnT4_BP 1 : Enable SMIOVT4 Beep function 0 : Disable SMIOVT4 Beep function
2	EnT3_BP 1 : Enable SMIOVT3 Beep function 0 : Disable SMIOVT3 Beep function
1	EnT2_BP 1 : Enable SMIOVT2 Beep function 0 : Disable SMIOVT2 Beep function
0	EnT1_BP 1 : Enable SMIOVT1 Beep function 0 : Disable SMIOVT1 Beep function

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.45 BEEP Control Register 4 – Index B5h (Bank0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	En Caseopen0_BP	En AUXFANIN2_BP	Reserved	Reserved	En CPUFANIN_BP	En SYSFANIN_BP	En_Beep
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	En Caseopen0_BP 1 : Enable Caseopen0_bp Beep function 0 : Disable Caseopen0_bp Beep function
5	En AUXFANIN2_BP 1 : Enable AUXFANIN2 Beep function 0 : Disable AUXFANIN2 Beep function
4	Reserved
3	Reserved
2	En CPUFANIN_BP 1 : Enable CPUFANIN Beep function 0 : Disable CPUFANIN Beep function
1	En SYSFANIN_BP 1 : Enable SYSFANIN Beep function 0 : Disable SYSFANIN Beep function
0	Enable Beep Function: 1 : Enable Beep Function 0 : Disable Beep Function

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.46 SMIOVT1 Temperature Source Configuration Register – Index Beh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Fault1				Reserved		
DEFAULT	0	0				0		

BIT	DESCRIPTION
7-6	Reserved
5-4	Fault1. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.

BIT	DESCRIPTION
	0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
3-0	Reserved

9.47 BEEP Control Register 5 – Index BFh (Bank0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	En AUXFANIN3 _BP						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
0	En AUXFANIN3_BP 1 : Enable AUXFANIN3 Beep function 0 : Disable AUXFANIN3 Beep function

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.48 SYSFAN Virtual1 Temperature Register – Index Eah (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN Virtual1 TEMP

9.49 CPUFAN Virtual1 Temperature Register – Index Ebh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Virtual1 Temperature							

DEFAULT	0	0	0	0	0	0	0	0
---------	---	---	---	---	---	---	---	---

BIT	DESCRIPTION
7-0	CPUFAN Virtual1 TEMP

9.50 AUXFAN2 Virtual1 Temperature Register – Index Eeh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 Virtual1 TEMP

9.51 AUXFAN3 Virtual1 Temperature Register – Index Efh (Bank 0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 Virtual1 TEMP

9.52 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved			SYSFAN SOURCE1[4:0]			
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7	Stopduty_En: 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to SYSFANOUT Stop Value (Bank1, index05h) at most if necessary.

BIT	DESCRIPTION
	(This function is for Thermal Cruise mode.)
6-5	Reserved
4-0	<p>SYSFAN Temperature Source1 Select:</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SYSFAN monitoring source.</p> <p>0 0 0 1 0: Select CPUTIN as SYSFAN monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as SYSFAN monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as SYSFAN monitoring source.</p> <p>0 1 0 1 0: Select Virtual_TEMP2 as SYSFAN monitoring source.</p> <p>0 1 0 1 1: Select Virtual_TEMP3 as SYSFAN monitoring source</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as SYSFAN monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as SYSFAN monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SYSFAN monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as SYSFAN monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as SYSFAN monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as SYSFAN monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as SYSFAN monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as SYSFAN monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as SYSFAN monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as SYSFAN monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as SYSFAN monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as SYSFAN monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as SYSFAN monitoring source.</p> <p>1 1 1 0 1: Select PECI Agent 1 Calibration as SYSFAN monitoring source.</p> <p>1 1 1 1 1: Select Virtual_TEMP1 as SYSFAN monitoring source.</p>

Note. If the temperature source is selecting to PECI, please set Bank0 Index Aeh first for reading correct value.

9.53 SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 01h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN Target Temperature / SYSFANIN Target Speed_L / CPUFANIN Target Thermal Margin							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	SYSFAN Target Temperature							

Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]
SMART FAN™ IV	DESCRIPTION	CPUFANIN Target Thermal Margin

9.54 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 02h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE					Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	SYSFANOUT Mode Select. 0000: SYSFANOUT is in Manual Mode. (Default) 0001: SYSFANOUT is in Thermal Cruise Mode. 0010: SYSFANOUT is in Speed Cruise Mode. 0100: SYSFANOUT is in SMART FAN IV Mode.
3	Reserved
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.55 SYSFANOUT Step Up Time Register – Index 03h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.56 SYSFANOUT Step Down Time Register – Index 04h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	SYSFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.57 SYSFANOUT Stop Value Register – Index 05h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.58 SYSFANOUT Start-up Value Register – Index 06h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.59 SYSFANOUT Stop Time Register – Index 07h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes SYSFANOUT value to fall from the stop value to zero.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.60 SYSFANOUT Output Value Select Register – Index 09h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E0h] is the Default Speed Configuration Register of SYSFANOUT.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. $\text{OUTPUT Voltage} = \text{AVSB} * \frac{\text{FANOUT}}{64}$						Reserved	

9.61 SYSFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0	
NAME	Reserved	SYSFANIN TOL_H				SYSFANIN Target Speed_H			
DEFAULT	0	0				0			

BIT	DESCRIPTION
7	Reserved
6-4	SYSFANIN Tolerance_H [5:3]
3-0	SYSFANIN Target Speed_H [11:8]

9.62 SYSFAN (SMART FAN™ IV) Temperature 5 Register(T5) – Index 11h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 5							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 5 Register (T5).

9.63 SYSFAN (SMART FAN™ IV) Temperature 6 Register(T6) – Index 12h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 6							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 6 Register (T6).

9.64 SYSFAN (SMART FAN™ IV) Temperature 7 Register(T7) – Index 13h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 7							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 7 Register (T7).

9.65 SYSFAN (SMART FAN™ IV) Temperature 8 Register(T8) – Index 14h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 8							

DEFAULT	0	0	1	1	0	1	1	1
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BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 8 Register (T8).

9.66 SYSFAN (SMART FAN™ IV) DC/PWM 5 Register – Index 17h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 5							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 5 Register.

9.67 SYSFAN (SMART FAN™ IV) DC/PWM 6 Register – Index 18h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 6							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 6 Register.

9.68 SYSFAN (SMART FAN™ IV) DC/PWM 7 Register – Index 19h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 7							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 6 Register.

9.69 SYSFAN (SMART FAN™ IV) DC/PWM 8 Register – Index 1Ah (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 8							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 8 Register.

9.70 SYSFAN (SMART FAN™ IV) Profile Temperature Register – Index 1Bh (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Profile Temperature							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Profile Temperature Register.

9.71 SYSFAN (SMART FAN™ IV) Profile Temperature Register – Index 1Ch (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	PF_Enable	Reserved				Profile Temperature Tolerance		
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7	PF_Enable : 0 : disable change profile function. 1 : enable change profile function.
6-3	Reserved
2-0	Profile Temperature Tolerance.

9.72 SYSFAN (SMART FAN™ IV) Compare Temperature Source2 Select Register – Index 1Dh (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	Reserved			SYSFAN SOURCE2[4:0]				
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-5	Reserved.
4-0	<p>SYSFAN Temperature Source2 Select:</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SYSFAN monitoring source.</p> <p>0 0 0 1 0: Select CPUTIN as SYSFAN monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as SYSFAN monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as SYSFAN monitoring source.</p> <p>0 1 0 1 0: Select Virtual_TEMP2 as SYSFAN monitoring source.</p> <p>0 1 0 1 1: Select Virtual_TEMP3 as SYSFAN monitoring source</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as SYSFAN monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as SYSFAN monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SYSFAN monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as SYSFAN monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as SYSFAN monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as SYSFAN monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as SYSFAN monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as SYSFAN monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as SYSFAN monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as SYSFAN monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as SYSFAN monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as SYSFAN monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as SYSFAN monitoring source.</p> <p>1 1 1 0 1: Select PECI Agent 1 Calibration as SYSFAN monitoring source.</p> <p>1 1 1 1 1: Select Virtual_TEMP1 as SYSFAN monitoring source.</p>

9.73 SYSFAN (SMART FAN™ IV) Compare Temperature Source3 Select Register – Index 1Eh (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			SYSFAN SOURCE3[4:0]				
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-5	Reserved.

	SYSFAN Temperature Source3 Select: Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as SYSFAN monitoring source. 0 0 0 1 0: Select CPUTIN as SYSFAN monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as SYSFAN monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as SYSFAN monitoring source. 0 1 0 1 0: Select Virtual_TEMP2 as SYSFAN monitoring source. 0 1 0 1 1: Select Virtual_TEMP3 as SYSFAN monitoring source 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 4-0 1 0 0 0 0: Select PECI Agent 0 as SYSFAN monitoring source. 1 0 0 0 1: Select PECI Agent 1 as SYSFAN monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SYSFAN monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as SYSFAN monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as SYSFAN monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as SYSFAN monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as SYSFAN monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as SYSFAN monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as SYSFAN monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as SYSFAN monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as SYSFAN monitoring source. 1 1 0 1 1: Select BYTE_TEMP1 as SYSFAN monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as SYSFAN monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as SYSFAN monitoring source. 1 1 1 1 1: Select Virtual_TEMP1 as SYSFAN monitoring source.
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9.74 SYSFAN (SMART FAN™ IV) Source Comparator Enable Register – Index 1Fh (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
1	Enable SYSFAN temperature source comparator.

9.75 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.76 SYSFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.77 SYSFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.78 SYSFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.79 SYSFAN (SMART FAN™ IV) DC/PWM 1 Register – Index 27h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION							
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 1 Register.							

9.80 SYSFAN (SMART FAN™ IV) DC/PWM 2 Register – Index 28h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION							
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 2 Register.							

9.81 SYSFAN (SMART FAN™ IV) DC/PWM 3 Register – Index 29h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION							
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 3 Register.							

9.82 SYSFAN (SMART FAN™ IV) DC/PWM 4 Register – Index 2Ah (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 4							

DEFAULT	1	1	1	0	0	1	1	0
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BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 4 Register.

9.83 SYSFAN 3-Wire Enable Register – Index 31h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0	
NAME	Reserved								EN_SYS_3WFAN
DEFAULT	0								0

BIT	DESCRIPTION
7-1	Reserved
0	EN_SYS_3WFAN (SYSFAN type setting) 0: 4-wire fan 1: 3-wire fan

9.84 SYSFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0	
NAME	SYSFAN (SMART FAN™ IV) Temperature Critical								
DEFAULT	0	0	1	1	1	1	0	0	

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Critical Temperature Register.

9.85 SYSFAN Enable Critical Duty – Index 36h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0	
NAME	Reserved								En_SYS_CRITICAL_DUTY
DEFAULT	0								0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Enable Critical Duty Register.

7-1	Reserved
0	En_SYS_CRITICAL_DUTY (set 0 in manual mode) 0: Load default Full Speed 8'hFF for SYSFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for SYSFANOUT.

9.86 SYSFAN Critical Duty Register – Index 37h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	SYSFAN Critical Duty.

9.87 SYSFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	Reserved
2-0	SYSFANOUT Critical Temperature Tolerance

9.88 SYSFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_SYS_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_SYS_PECIERR_DUTY 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 PECI_ERR_SYSOUT Value for SYSFANOUT.

	10,11: Keep Full Speed
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9.89 SYSFANOUT Pre-Configured Register For PECL Error – Index 41h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured register for PECL error (PECL_ERR_SYSOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SYSFANOUT pre-configured register for PECL error.

9.90 SMIOVT2 Temperature Source (High Byte) Register – Index 50h (Bank 1)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	Temperature <8:1> (default: CPUTIN temperature source). The nine-bit value is in units of 0.5°C.

9.91 SMIOVT2 Temperature Source (Low Byte) Register – Index 51h (Bank 1)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	Temperature <0> (default: CPUTIN temperature source). The nine-bit value is in units of 0.5°C.
6-0	Reserved

9.92 SMIOVT2 Temperature Source Configuration Register – Index 52h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP

DEFAULT	0	0	0	0	0	0	0	0
---------	---	---	---	---	---	---	---	---

BIT	DESCRIPTION
7-5	Reserved This bit should be set to zero.
4-3	Fault. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	Reserved This bit should be set to zero.
1	OVTMOD. SMIOVT2 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.
0	STOP. 0: Monitor SMIOVT2 temperature source. 1: Stop monitoring SMIOVT2 temperature source.

9.93 SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.94 SMIOVT2 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	THYST<0>. Hysteresis temperature bit 0. The nine-bit value is in units of 0.5°C.
6-0	Reserved

9.95 SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank1)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	TOVF<8:1> . Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.96 SMIOVT2 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	TOVF<0> . Over-temperature bit 0. The nine-bit value is in units of 0.5°C.
6-0	Reserved

9.97 DUTY PER STEP Register – Index 66h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.98 T1 Delay Time Register – Index 67h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.99 SYSFAN Max Duty compare Source Select Register – Index 68h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					SYSFAN Max Duty compare Source Select		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved
2	SYSFAN Max Duty Source Select Please keep 0.
1	SYSFAN Max Duty Source Select Please keep 0.
0	SYSFAN Max Duty Source Select 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty

9.100 SYSFAN Max Duty Output Register – Index 69h (Bank 1)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	SYSFAN Max Duty Output

9.101 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved			CPUFAN SOURCE[4:0]			
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	<p>Stopduty_En: 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to CPUFANOUT Stop Value (Bank2, index05h) at most if necessary. (This function is for Thermal Cruise mode.)</p>
6-5	Reserved
4-0	<p>CPUFAN Temperature Source Select: Bits 4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as CPUFAN monitoring source. 0 0 0 1 0: Select CPUTIN as CPUFAN monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as CPUFAN monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as CPUFAN monitoring source. 0 1 0 1 0: Select Virtual_TEMP2 as CPUFAN monitoring source. 0 1 0 1 1: Select Virtual_TEMP3 as CPUFAN monitoring source 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select PECI Agent 0 as CPUFAN monitoring source. 1 0 0 0 1: Select PECI Agent 1 as CPUFAN monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as CPUFAN monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as CPUFAN monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as CPUFAN monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as CPUFAN monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as CPUFAN monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as CPUFAN monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as CPUFAN monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as CPUFAN monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as CPUFAN monitoring source. 1 1 0 1 1: Select BYTE_TEMP1 as CPUFAN monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as CPUFAN monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as CPUFAN monitoring source. 1 1 1 1 1: Select Virtual_TEMP as CPUFAN monitoring source.</p>

Note. If the temperature source is selecting to PECI, please set Bank0 Index Aeh first for reading correct value.

9.102 CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 01h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	CPUFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.103 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 02h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE					Reserved	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-4	CPUFANOUT Mode Select. 0000: CPUFANOUT is in Manual Mode. (Default) 0001: CPUFANOUT is in Thermal Cruise Mode. 0010: CPUFANOUT is in Speed Cruise Mode. 0100: CPUFANOUT is in SMART FAN IV Mode.
3	Reserved
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.104 CPUFANOUT Step Up Time Register – Index 03h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.105 CPUFANOUT Step Down Time Register – Index 04h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	CPUFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.106 CPUFANOUT Stop Value Register – Index 05h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.107 CPUFANOUT Start-up Value Register – Index 06h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.108 CPUFANOUT Stop Time Register – Index 07h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes CPUFANOUT value to fall from the stop value to zero.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.109 CPUFANOUT Output Value Select Register – Index 09h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E1h] is the Default Speed Configuration Register of CPUFANOUT.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output Only	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.110 CPUFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CPUFANIN TOL_H			CPUFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION							
7	Reserved							
6-4	CPUFANIN Tolerance_H [5:3]							
3-0	CPUFANIN Target Speed_H [11:8]							

9.111 CPUFAN MODE Register / THERMAL MARGIN Register – Index 0Dh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			Thermal Margin tolerance			Reserve d	Thermal Margin enable
DEFAULT	0	0	0	0			0	0

BIT	DESCRIPTION							

7-5	Reserved
4-2	Thermal Margin tolerance
1	Reserved
0	Thermal Margin enable

9.112 CPUFAN MODE Register / T control Register – Index 0Fh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T control							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION							
7-0	T control							

9.113 CPUFAN (SMART FAN™ IV) Temperature 5 Register(T5) – Index 11h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 5							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION							
7-0	CPUFAN (SMART FAN™ IV) Temperature 5 Register (T5).							

9.114 CPUFAN (SMART FAN™ IV) Temperature 6 Register(T6) – Index 12h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 6							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION							
7-0	CPUFAN (SMART FAN™ IV) Temperature 6 Register (T6).							

9.115 CPUFAN (SMART FAN™ IV) Temperature 7 Register(T7) – Index 13h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 7							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION							
7-0	CPUFAN (SMART FAN™ IV) Temperature 7 Register (T7).							

9.116 CPUFAN (SMART FAN™ IV) Temperature 8 Register(T8) – Index 14h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 8							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION							
7-0	SYSFAN (SMART FAN™ IV) Temperature 8 Register (T8).							

9.117 SYSFAN (SMART FAN™ IV) DC/PWM 5 Register – Index 17h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/PWM 5							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION							
7-0	CPUFAN (SMART FAN™ IV) DC/PWM 5 Register.							

9.118 CPUFAN (SMART FAN™ IV) DC/PWM 6 Register – Index 18h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/PWM 6							

DEFAULT	1	0	1	0	1	0	1	0
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BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/PWM 6 Register.

9.119 CPUFAN (SMART FAN™ IV) DC/PWM 7 Register – Index 19h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/PWM 7							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/PWM 6 Register.

9.120 CPUFAN (SMART FAN™ IV) DC/PWM 8 Register – Index 1Ah (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/PWM 8							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/PWM 8 Register.

9.121 CPUFAN (SMART FAN™ IV) Profile Temperature Register – Index 1Bh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Profile Temperature							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Profile Temperature Register.

9.122 CPUFAN (SMART FAN™ IV) Profile Temperature Register – Index 1Ch (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	PF_Enable	Reserved				Profile Temperature Tolerance		
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7	PF_Enable : 0 : disable change profile function. 1 : enable change profile function.
6-3	Reserved
2-0	Profile Temperature Tolerance.

9.123 CPUFAN (SMART FAN™ IV) Compare Temperature Source2 Select Register – Index 1Dh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			CPUFAN SOURCE2[4:0]				
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-5	Reserved.
4-0	<p>CPUFAN Temperature Source2 Select:</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as CPUFAN monitoring source.</p> <p>0 0 0 1 0: Select CPUTIN as CPUFAN monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as CPUFAN monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as CPUFAN monitoring source.</p> <p>0 1 0 1 0: Select Virtual_TEMP2 as CPUFAN monitoring source.</p> <p>0 1 0 1 1: Select Virtual_TEMP3 as CPUFAN monitoring source</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as CPUFAN monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as CPUFAN monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as CPUFAN monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as CPUFAN monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as CPUFAN monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as CPUFAN monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as CPUFAN monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as CPUFAN monitoring source.</p>

	1 1 0 0 0: Select Agent1 Dimm0 as CPUFAN monitoring source.
	1 1 0 0 1: Select Agent1 Dimm1 as CPUFAN monitoring source.
	1 1 0 1 0: Select BYTE_TEMP0 as CPUFAN monitoring source.
	1 1 0 1 1: Select BYTE_TEMP1 as CPUFAN monitoring source.
	1 1 1 0 0: Select PECI Agent 0 Calibration as CPUFAN monitoring source.
	1 1 1 0 1: Select PECI Agent 1 Calibration as CPUFAN monitoring source.
	1 1 1 1 1: Select Virtual_TEMP1 as CPUFAN monitoring source.

9.124 CPUFAN (SMART FAN™ IV) Compare Temperature Source3 Select Register – Index 1Eh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			CPUFAN SOURCE3[4:0]				
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-5	Reserved.
4-0	<p>CPUFAN Temperature Source3 Select:</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as CPUFAN monitoring source.</p> <p>0 0 0 1 0: Select CPUTIN as CPUFAN monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as CPUFAN monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as CPUFAN monitoring source.</p> <p>0 1 0 1 0: Select Virtual_TEMP2 as CPUFAN monitoring source.</p> <p>0 1 0 1 1: Select Virtual_TEMP3 as CPUFAN monitoring source</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as CPUFAN monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as CPUFAN monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as CPUFAN monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as CPUFAN monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as CPUFAN monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as CPUFAN monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as CPUFAN monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as CPUFAN monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as CPUFAN monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as CPUFAN monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as CPUFAN monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as CPUFAN monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as CPUFAN monitoring source.</p> <p>1 1 1 0 1: Select PECI Agent 1 Calibration as CPUFAN monitoring source.</p> <p>1 1 1 1 1: Select Virtual_TEMP1 as CPUFAN monitoring source.</p>

9.125 CPUFAN (SMART FAN™ IV) Source Comparator Enable Register – Index 1Fh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-1	Reserved							
1	Enable CPUFAN temperature source comparator.							

9.126 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION							
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).							

9.127 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION							
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).							

9.128 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	CPUFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.129 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.130 CPUFAN (SMART FAN™ IV) PWM1 Register – Index 27h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM1 Register.

9.131 CPUFAN (SMART FAN™ IV) PWM2 Register – Index 28h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM2 Register.

9.132 CPUFAN (SMART FAN™ IV) PWM3 Register – Index 29h (Bank 2)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM3 Register.

9.133 CPUFAN (SMART FAN™ IV) PWM4 Register – Index 2Ah (Bank 2)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM4 Register.

9.134 CPUFAN 3-Wire FAN Enable Register – Index 31h (Bank 2)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_CPU_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved
0	EN_CPU_3WFAN (CPUFAN type setting) 0: 4-wire fan 1: 3-wire fan

9.135 CPUFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 2)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	CPUFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Critical Temperature Register.

9.136 CPUFAN Enable Critical Duty – Index 36h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPU_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved
0	En_CPU_CRITICAL_DUTY (set 0 in manual mode) 0: Load default Full Speed 8'hFF for CPUFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for CPUFANOUT.

9.137 CPUFAN Critical Duty Register – Index 37h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	CPUFAN Critical Duty.

9.138 CPUFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-0	CPUFANOUT Critical Temperature Tolerance.

7-3	Reserved
2-0	CPUFANOUT Critical Temperature Tolerance

9.139 Weight value Configuration Register – Index 39h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_WEIGHT	Reserved		CPU_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	EN_CPUFAN_WEIGHT. 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-5	Reserved
4-0	CPUFAN Weighting Temperature Source Select: Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as CPUFAN monitoring source. (Default) 0 0 0 1 0: Select CPUTIN as CPUFAN monitoring source. 0 0 1 1 1: Reserved 0 1 0 0 0: Select SMBUSMASTER 0 as CPUFAN monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as CPUFAN monitoring source. 0 1 0 1 0: Select SMBUSMASTER 2 as CPUFAN monitoring source. 0 1 0 1 1: Select SMBUSMASTER 3 as CPUFAN monitoring source. 0 1 1 0 0: Select SMBUSMASTER 4 as CPUFAN monitoring source. 0 1 1 0 1: Select SMBUSMASTER 5 as CPUFAN monitoring source. 0 1 1 1 0: Select SMBUSMASTER 6 as CPUFAN monitoring source. 0 1 1 1 1: Select SMBUSMASTER 7 as CPUFAN monitoring source. 1 0 0 0 0: Select PECI Agent 0 as CPUFAN monitoring source. 1 0 0 0 1: Select PECI Agent 1 as CPUFAN monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as CPUFAN monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as CPUFAN monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as CPUFAN monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as CPUFAN monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as CPUFAN monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as CPUFAN monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as CPUFAN monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as CPUFAN monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as CPUFAN monitoring source. 1 1 0 1 1: Select BYTE_TEMP1 as CPUFAN monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as CPUFAN monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as CPUFAN monitoring source.

9.140 CPUFANOUT Temperature Step Register – Index 3Ah (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
CPUFANOUT Temperature Step (CPU_TEMP_STEP)								
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Step

9.141 CPUFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)								
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Step Tolerance

9.142 CPUFANOUT Weight Step Register – Index 3Ch (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
CPUFANOUT Weight Step (CPU_WEIGHT_STEP)								
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Weight Step

9.143 CPUFANOUT Temperature Base Register – Index 3Dh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
CPUFANOUT Temperature Base (CPU_TEMP_BASE)								
NAME								

DEFAULT	0
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BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Base

9.144 CPUFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Start point of Fan Duty increasing

9.145 CPUFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_CPU_PECIERR_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_CPU_PECIERR_DUTY 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 PECL_ERR_CPUOUT Value for CPUFANOUT. 10,11: Keep Full Speed

9.146 CPUFANOUT Pre-Configured Register For PECL Error – Index 41h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured register for PECL error (PECL_ERR_CPUOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	CPUFANOUT pre-configured register for PECL error.

9.147 DUTY PER STEP Register – Index 66h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.148 T1 Delay Time Register – Index 67h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.149 CPUFAN Max Duty compare Source Select Register – Index 68h (Bank 2)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					CPUFAN Max Duty compare Source Select		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved
2	CPUFAN Max Duty Source Select Please keep 0.
1	CPUFAN Max Duty Source Select Please keep 0.
0	CPUFAN Max Duty Source Select 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty

9.150 CPUFAN Max Duty Output Register – Index 69h (Bank 2)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	CPUFAN Max Duty Output

9.151 PCH_CHIP_CPU_MAX_TEMP Register – Index 00h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_CPU_MAX_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	PCH_CHIP_CPU_MAX_TEMP: The maximum temperature in absolute degree C, of the CPU and MCH.

9.152 PCH_CHIP_TEMP Register – Index 01h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	PCH_CHIP_TEMP The IBX_CHIP temperature in degree C.

9.153 PCH_CPU_TEMP_H Register – Index 02h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
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NAME	PCH_CPU_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	PCH_CPU_TEMP_H	The CPU temperature in degree C. (Integer Part)						

9.154 PCH_CPU_TEMP_L Register – Index 03h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_L						Reserved	Reading_Flag
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-2	PCH_CPU_TEMP_L	The CPU temperature in degree C. (Fractional Part)						
1	Reserved							
0	Reading_Flag:	If there is an error when the IBX read the data from the CPU, then Bit0 is set to '1'.						

9.155 PCH_MCH_TEMP Register – Index 04h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_MCH_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	PCH_MCH_TEMP	The MCH temperature in degree C.						

9.156 Agent0 Dimm0 Register – Index 05h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent0 Dimm0							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	Agent0 Dimm0 The Agent0 Dimm0 temperature.							

9.157 Agent0 Dimm1 Register – Index 06h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent0 Dimm1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	Agent0 Dimm1 The Agent0 Dimm1 temperature.							

9.158 Agent1 Dimm0 Register – Index 07h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent1 Dimm0							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	Agent1 Dimm0 The Agent1 Dimm0 temperature.							

9.159 Agent1 Dimm1 Register – Index 08h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent1 Dimm1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	Agent1 Dimm1 The Agent1 Dimm1 temperature.							

9.160 PCH_TSI0_TEMP_H Register – Index 09h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	PCH_TSI0_TEMP_H The TSI High-Byte temperature in degree C.							

9.161 PCH_TSI0_TEMP_L Register – Index 0Ah (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-5	PCH_TSI0_TEMP_L The TSI Low-Byte temperature in degree C.							
4-0	Reserved							

9.162 PCH_TSI1_TEMP_H Register – Index 0Bh (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	PCH_TSI1_TEMP_H The TSI High-Byte temperature in degree C.							

9.163 PCH_TSI1_TEMP_L Register – Index 0Ch (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-5	PCH_TSI1_TEMP_L The TSI Low-Byte temperature in degree C.							

BIT	DESCRIPTION							
4-0	Reserved							

9.164 ByteTemp0 Register – Index 19h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	ByteTemp0 The Byte format Device0 Byte temperature in degree C.							

9.165 ByteTemp1 Register – Index 1Ah (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	ByteTemp1 The Byte format Device1 Byte temperature in degree C.							

9.166 VIN1 High Limit Compared Voltage Register – Index 23h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 High Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION							
7-0	VIN1 High Limit Compared Voltage. Default: 0x96h (1.2V)							

9.167 VIN1 Low Limit Compared Voltage Register – Index 24h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 Low Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	VIN1 Low Limit Compared Voltage. Default: 0x64h (0.8V)

9.168 VIN0 High Limit Compared Voltage Register – Index 25h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 High Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	VIN0 High Limit Compared Voltage. Default: 0x96h (1.2V)

9.169 VIN0 Low Limit Compared Voltage Register – Index 26h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 Low Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	VIN0 Low Limit Compared Voltage. Default: 0x64h (0.8V)

9.170 AVSB High Limit Compared Voltage Register – Index 27h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AVSB High Limit Compared Voltage (AVSB_LimtH)							
DEFAULT	1	1	1	0	0	0	0	1

BIT	DESCRIPTION
7-0	AVSB High Limit Compared Voltage. Default: 0xE1h (1.8V *2)

9.171 AVSB Low Limit Compared Voltage Register – Index 28h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AVSB Low Limit Compared Voltage (AVSB_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	AVSB Low Limit Compared Voltage (AVSB_LimtH). Default: 0x96h (1.2V *2)

9.172 Voltage Comparation Interrupt Status Register - Index 42h (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AVSB_Warn	VIN0_Warn	VIN1_Warn
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved
2	AVSB_Warn. A one indicates the limit of AVSB voltage has been exceeded.
1	VIN0_Warn. A one indicates the limit of VIN0 voltage has been exceeded.
0	VIN1_Warn A one indicates the limit of VIN1 voltage has been exceeded.

9.173 Interrupt Status Register 3 – Index 50h (Bank 4)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2	Reserved	AUXFANIN2	Reserved	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	AUXFANOUT2. “1” indicates that AUXFANOUT2 works for three minutes at the full fan speed.
6	Reserved
5	AUXFANIN2. A one indicates the fan count limit of AUXFANIN2 has been exceeded.

BIT	DESCRIPTION
4	Reserved
2-3	Reserved
1	VBAT. A one indicates the high or low limit of VBAT has been exceeded.
0	3VSB. A one indicates the high or low limit of 3VSB has been exceeded.

9.174 SMI# Mask Register 4 – Index 51h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	TAR5	TAR4	TAR3	RESERVED	SMSKVBAT	SMSKVSB	
DEFAULT	1	1	1	1	0	0	1	1

BIT	DESCRIPTION
7	Reserved
6	TAR5. A one disables the corresponding interrupt status bit for the <u>SMI</u> interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
5	TAR4. A one disables the corresponding interrupt status bit for the <u>SMI</u> interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
4	TAR3. A one disables the corresponding interrupt status bit for the <u>SMI</u> interrupt. (See Interrupt Status Register 3 – Index 45h (Bank 0))
3-2	Reserved
1	SMSKVBAT. A one disables the corresponding interrupt status bit for the <u>SMI</u> interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
0	SMSKVSB. A one disables the corresponding interrupt status bit for the <u>SMI</u> interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))

9.175 SYSTIN Temperature Sensor Offset Register – Index 54h (Bank 4)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSTIN Temperature Offset Value. The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.176 CPUTIN Temperature Sensor Offset Register – Index 55h (Bank 4)

Attribute: Read/Write
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUTIN Temperature Offset Value. The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.177 Real Time Hardware Status Register I – Index 59h (Bank 4)

Attribute: Read Only
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN_STS	SYSFANIN_STS	CPUTIN_STS	SYSTIN_STS	3VCC_STS	AVSB_STS	VIN1_STS	CPUVCORE_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	CPUFANIN_STS. CPUFANIN Status. 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	SYSFANIN_STS. SYSFANIN Status. 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
5	CPUTIN_STS. CPUTIN Temperature Sensor Status. 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	SYSTIN_STS. SYSTIN Temperature Sensor Status. 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	3VCC_STS. 3VCC Voltage Status. 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	AVSB_STS. AVSB Voltage Status. 1: AVSB voltage is over or under the allowed range. 0: AVSB voltage is in the allowed range.
1	VIN1_STS. VIN1 Voltage Status. 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.
0	CPUVCORE_STS. CPUVCORE Voltage Status. 1: CPUVCORE voltage is over or under the allowed range.

BIT	DESCRIPTION							
	0: CPUVCORE voltage is in the allowed range.							

9.178 Real Time Hardware Status Register II – Index 5Ah (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TAR2_STS	TAR1_STS	Reserved	CASEOPEN0_STS	Reserved	Reserved	Reserved	VIN0_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7	TAR2_STS. Smart Fan of CPUFANIN Warning Status. 1: Selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: Selected temperature has not reached the warning range.							
6	TAR1_STS. Smart Fan of SYSFANIN Warning Status. 1: SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: SYSTIN temperature has not reached the warning range.							
5	Reserved							
4	CASEOPEN0_STS. CaseOpen Status. 1: Caseopen0 is detected and latched. 0: Caseopen0 is not latched.							
3	Reserved							
2	Reserved							
1	Reserved							
0	VIN0_STS. VIN0 Voltage Status. 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.							

9.179 Real Time Hardware Status Register III – Index 5Bh (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2_STS	TAR5_STS	Reserved	Reserved	Reserved	Reserved	VBAT_STS	VSB_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7	AUXFANIN2_STS. AUXFANIN2 Status.							

BIT	DESCRIPTION
	1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	TAR5_STS. Smart Fan of AUXFANIN2 Warning Status. 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
5	Reserved
4	Reserved
3	Reserved
2	Reserved
	VBAT_STS. VBAT Voltage Status.
1	1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	VSB_STS. 3VSB Voltage Status. 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.180 Real Time Hardware Status Register III – Index 5Dh (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AUXFANIN3_STS	TAR6_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	RESERVED
1	AUXFANIN3 Status. 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
0	TAR6_STS. Smart Fan of AUXFANIN3 Warning Status. 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.

9.181 Value RAM — Index 80h ~ 96h (Bank 4)

ADDRESS A6-A0	DESCRIPTION
80h	CPUVCORE reading
81h	VIN1 reading
82h	AVSB reading

83h	3VCC reading
84h	VIN0 reading
85h	Reserved
86h	Reserved
87h	3VSB reading
88h	VBAT reading
89h	VTT reading
8Ah	Reserved
8Bh	Reserved
8Ch	Reserved
8Dh	Reserved
8Eh	Reserved
8Fh	VIN9 reading
90h	SYSTIN temperature reading
91h	CPUTIN temperature reading
92h	Reserved
93h	Reserved
94h	Reserved
95h	Reserved

9.182 (SYSFANIN) FANIN1 COUNT High-byte Register – Index B0h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT1 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION							
7-0	FANCNT1_H: 13-bit SYSFANIN Fan Count, High Byte							

9.183 (SYSFANIN) FANIN1 COUNT Low-byte Register – Index B1h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT1 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	Reserved
4-0	FANCNT1_L: 13-bit SYSFANIN Fan Count, Low Byte

9.184 (CPUFANIN) FANIN2 COUNT High-byte Register – Index B2h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT2 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	FANCNT2_H: 13-bit CPUFANIN Fan Count, High Byte

9.185 (CPUFANIN) FANIN2 COUNT Low-byte Register – Index B3h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				FANCNT2 [4:0]			
DEFAULT	0				1F			

BIT	DESCRIPTION
7-5	Reserved
4-0	FANCNT2_L: 13-bit CPUFANIN Fan Count, Low Byte

9.186 (AUXFANIN2) FANIN5 COUNT High-byte Register – Index B8h (Bank 4)

Attribute: Read

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT5 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	FANCNT5_H: 13-bit AUXFANIN2 Fan Count, High Byte

9.187 (AUXFANIN2) FANIN5 COUNT Low-byte Register – Index B9h (Bank 4)

Attribute: Read
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0	
NAME	RESERVED			FANCNT5 [4:0]					
DEFAULT	0			1F					

BIT	DESCRIPTION							
7-5	Reserved							
4-0	FANCNT5_L: 13-bit AUXFANIN2 Fan Count, Low Byte							

9.188 (AUXFANIN3) FANIN6 COUNT High-byte Register – Index Bah (Bank 4)

Attribute: Read
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT6 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION							
7-0	FANCNT6_H: 13-bit AUXFANIN3 Fan Count, High Byte							

9.189 (AUXFANIN3) FANIN6 COUNT Low-byte Register – Index BBh (Bank 4)

Attribute: Read
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0	
NAME	RESERVED			FANCNT6 [4:0]					
DEFAULT	0			1F					

BIT	DESCRIPTION							
7-5	Reserved							
4-0	FANCNT6_L: 13-bit AUXFANIN3 Fan Count, Low Byte							

9.190 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index C0h (Bank 4)

Attribute: Read Only
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
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NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFANIN SPEED HIGH-BYTE VALUE.

9.191 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index C1h (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFANIN SPEED LOW-BYTE VALUE.

9.192 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) – Index C2h (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFANIN SPEED HIGH-BYTE VALUE.

9.193 CPUFANIN SPEED LOW-BYTE VALUE (RPM) – Index C3h (Bank 4)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFANIN SPEED LOW-BYTE VALUE.

9.194 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) – Index C8h (Bank 4)

Attribute: Read Only
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED HIGH -BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	AUXFANIN2 SPEED HIGH-BYTE VALUE.							

9.195 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) – Index C9h (Bank 4)

Attribute: Read Only
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	AUXFANIN2 SPEED LOW-BYTE VALUE.							

9.196 AUXFANIN3 SPEED HIGH-BYTE VALUE (RPM) – Index Cah (Bank 4)

Attribute: Read Only
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN3 SPEED HIGH -BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-0	AUXFANIN3 SPEED HIGH-BYTE VALUE.							

9.197 AUXFANIN3 SPEED LOW-BYTE VALUE (RPM) – Index CBh (Bank 4)

Attribute: Read Only
 Size: 8 bits
 Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN3 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN3 SPEED LOW-BYTE VALUE.

9.198 PECL Agent0 Calibration Temp – Index F4h (Bank 4)

Attribute: Read / Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECL Agent0 Calibration Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The temperature is after PECL Agent0 Calibration

9.199 PECL Agent1 Calibration Temp – Index F5h (Bank 4)

Attribute: Read / Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECL Agent1 Calibration Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The temperature is after PECL Agent1 Calibration

9.200 PECL Agent0 Calibration Control Register – Index F8h (Bank 4)

Attribute: Read / Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	UP or Down Times					Adjust unit		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	UP or Down Times For PECL Agent0 Calibration
2-0	Adjust unit for PECL Agent0 Calibration

9.201 PECL Agent1 Calibration Control Register – Index F9h (Bank 4)

Attribute: Read / Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	UP or Down Times					Adjust unit		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	UP or Down Times For PECL Agent1 Calibration
2-0	Adjust unit for PECL Agent1 Calibration

9.202 PECL Agent0 Calibration Control Register – Index Fah (Bank 4)

Attribute: Read / Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Update Time					Reserved		Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Update Times For PECL Agent0 Calibration (0.1~3.2sec)
2-1	Reserved
0	Function Enable for PECL Agent0 Calibration

9.203 PECL Agent1 Calibration Control Register – Index FBh (Bank 4)

Attribute: Read / Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Update Time					Reserved		Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Update Times For PECL Agent1 Calibration (0.1~3.2sec)
2-1	Reserved
0	Function Enable for PECL Agent1 Calibration

9.204 Value RAM 2 — Index 50h-5Fh (Bank 5)

ADDRESS A6-A0	DESCRIPTION
54h	3VSB High Limit
55h	3VSB Low Limit

ADDRESS A6-A0	DESCRIPTION
56h	VBAT High Limit
57h	VBAT Low Limit
58h	VTT High Limit
59h	VTT Low Limit
5Ah	
5Bh	
5Ch	
5Dh	
5Eh	
5Fh	
60h	
61h	
62h	
63h	
64h	VIN9 High Limit
65h	VIN9 Low Limit

9.205 SMI# Mask Register 1 – Index 66h (Bank 5)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VTT						
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	VTT

A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))

9.206 Interrupt Status Register – Index 67h (Bank 5)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VTT						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	VTT. A one indicates the high or low limit of VTT has been exceeded.

9.207 Real Time Hardware Status Register – Index 68h (Bank 5)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VIN9_STS	Reserved	Reserved	Reserved	Reserved	Reserved	VTT_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	VIN9_STS. VIN9 Voltage Status. 1: VIN9 voltage is over or under the allowed range. 0: VIN9 voltage is in the allowed range.
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	VTT_STS. VTT Voltage Status. 1: VTT voltage is over or under the allowed range. 0: VTT voltage is in the allowed range.

9.208 Close-Loop Fan Control RPM mode Register – Index 00 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		En_AUX3_RPM	En_AUX2_RPM	Reserved	Reserved	En_CPU_RPM	En_SYS_RPM
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION							
7-6	RESERVED							
5	En_AUX3_RPM 0 : Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.							
4	En_AUX2_RPM 0 : Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.							
3	Reserved							
2	Reserved							
1	En_CPU_RPM 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.							
0	En_SYS_RPM 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.							

9.209 SYSFAN RPM Mode Tolerance Register – Index 01 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_SYS_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION							
7-4	RESERVED							
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode (Bank6 index6 bit0) , unit is 100 RPM.							

9.210 CPUFAN RPM Mode Tolerance Register – Index 02 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_CPU_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	RESERVED
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode (Bank6 index6 bit1) , unit is 100 RPM.

9.211 AUXFAN2 RPM Mode Tolerance Register – Index 05 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_AUX2_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	RESERVED
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode (Bank6 index6 bit4) , unit is 100 RPM.

9.212 Enable RPM High Mode Register – Index 06 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	En_AUX3_RPM_HIGH	En_AUX2_RPM_HIGH	Reserved	Reserved	En_CPU_RPM_HIGH	En_SYS_RPM_HIGH	
DEFAULT	0	0	0	0	0	0	0	

BIT	DESCRIPTION
7-6	RESERVED
5	En_AUX3_RPM_HIGH For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
4	En_AUX2_RPM_HIGH For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
3	Reserved

2	Reserved
1	En_CPU_RPM_HIGH For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
0	En_SYS_RPM_HIGH For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable

9.213 SMIOVT1 Temperature Source Select Register – Index 21 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC1				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	SMIOVT1 Temperature selection. Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as SMIOVT1 monitoring source. (Default) 0 0 0 1 0: Select CPUTIN as SMIOVT1 monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT1 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT1 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select PECI Agent 0 as SMIOVT1 monitoring source. 1 0 0 0 1: Select PECI Agent 1 as SMIOVT1 monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT1 monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT1 monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT1 monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT1 monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT1 monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT1 monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT1 monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT1 monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT1 monitoring source.

	1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT1 monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT1 monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT1 monitoring source. 1 1 1 1 1: Select Virtual TEMP as SMIOVT1 monitoring source.
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9.214 SMIOVT2 Temperature Source Select Register – Index 22 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC2				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	RESERVED
4-0	<p>SMIOVT2 Temperature selection.</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SMIOVT2 monitoring source. 0 0 0 1 0: Select CPUTIN as SMIOVT2 monitoring source. (Default) 0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT2 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT2 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select PECI Agent 0 as SMIOVT2 monitoring source. 1 0 0 0 1: Select PECI Agent 1 as SMIOVT2 monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT2 monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT2 monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT2 monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT2 monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT2 monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT2 monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT2 monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT2 monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT2 monitoring source. 1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT2 monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT2 monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT2 monitoring source. 1 1 1 1 1: Select Virtual TEMP as SMIOVT2 monitoring source.</p>

9.215 AUXFAN3 RPM Mode Tolerance Register – Index 23 (Bank 6)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_AUX3_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	RESERVED
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode (Bank6 index6 bit5), unit is 100 RPM.

9.216 SYSFANIN Revolution Pulses Selection Register – Index 44h (Bank 6)

Attribute: Read /Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					HM_Rev_Pulse_Fan1_Sel		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	SYSFANIN Revolution Pulses Selection = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.217 CPUFANIN Revolution Pulses Selection Register – Index 45h (Bank 6)

Attribute: Read /Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					HM_Rev_Pulse_Fan2_Sel		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	CPUFANIN Revolution Pulses Selection = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default)

	= 11, three pulses per revolution.
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9.218 AUXFANIN2 Revolution Pulses Selection Register – Index 48h (Bank 6)

Attribute: Read /Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan5_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	AUXFANIN2 Revolution Pulses Selection = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.219 AUXFANIN3 Revolution Pulses Selection Register – Index 49h (Bank 6)

Attribute: Read /Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan6_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	AUXFANIN3 Revolution Pulses Selection = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.220 PECI Enable Function Register – Index 01h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0	
NAME	PECI_En	Dimm_En	Margin_En	Reserved			Is_PECI30	Manual_En	Routine_En
DEFAULT	0	0	0	1	0	1	0	0	

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECl Function. (PECI_En)
6	R / W	Enable PECl Dimm Function. (Dimm_En)
5	R / W	Enable PECl Margin Function. (Margin_En)
4 ~ 3	R / W	Reserved
2	R / W	Enable PECl 3.0 Command function (Is_PECI30)
1	R / W	Enable PECl 3.0 Manual Function (Manual_En) (One-shot clear)
0	R / W	Enable PECl 3.0 Routine Function (Routine_En)

9.221 PECl Timing Config Register – Index 02h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TN_Extend			Adj[2:0]		PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserve
5	R / W	TN_Extend[1:0] Adjust Transaction Rate. 00_{BIN} = 1.5 MHz (Default) 01_{BIN} = 750 KHz 10_{BIN} = 375 KHz 11_{BIN} = 187.5 KHz
4	R / W	
3	R / W	Adj[2:0]
2	R / W	Compensate the effect of rising time on physical bus
1	R / W	Default Value = 001
0	R / W	Adjust PECl Tbit Duty cycle selection. (PECI_DC) 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

9.222 PECl Agent Config Register – Index 03h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0	
NAME	Reserved		En_Agt[1:0]			Reserved		Domain1_Agt1	Domain1_Agt0
DEFAULT	0	0	0	0	0	0	0	0	

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserved
5	R / W	En_Agt[1 :0] Enable Agent 00 = Disable Agent. 01= Enable Agent0. 10 = Reserved 11 = Enable Agent0 and Agent1.
4	R / W	10 = Reserved 11 = Enable Agent0 and Agent1.
3 ~ 2	R / W	Reserved
1	R / W	Enable domain 1 for Agent1 0 = Agent1 without domain1 1 = Agent1 with domain 1
0	R / W	Enable domain 1 for Agent0 0 = Agent0 without domain 1 1 = Agent0 with domain 1

9.223 PECI Temperature Config Register – Index 04h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Virtual_En	Reserved		Clamp	Reserved	RtDmn_Agt[1:0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Virtual Temp Function Enable.(Virtual_En) When enable this function, the temperature raw data can use LPC to write raw data to CR 17 _{HEX} ~ CR 1E _{HEX}
6 ~ 5	R / W	Reserved
4	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(Clamp)
3	R / W	Reserved
2	R / W	RtDmn_Agt[1:0] Agent 1 – Agent 0 always return the relative domain Temperature.
1	R / W	0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
0	R / W	Return High Temperature of doamin0 or domain1.(RtHigher) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04 _{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.224 PECI Command Address Register – Index 05h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Address							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX}.

9.225 PECI Command Write Length Register – Index 06h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Write Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX}.

9.226 PECI Command Read Length Register – Index 07h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Read Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX}.

9.227 PECI Command Code Register – Index 08h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Code							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX}.

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.228 PECI Command Tbase0 Register – Index 09h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Tbase 0							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.229 PECI Command Tbase1 Register – Index 0Ah (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Tbase 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.230 PECI Command Write Data 1 Register – Index 0Bh (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.231 PECI Command Write Data 2 Register – Index 0Ch (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX} .

9.232 PECI Command Write Data 3 Register – Index 0Dh (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX} .

9.233 PECI Command Write Data 4 Register – Index 0Eh (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX} .

9.234 PECI Command Write Data 5 Register – Index 0Fh (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.235 PECl Command Write Data 6 Register – Index 10h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECl Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.236 PECl Command Write Data 7 Register – Index 11h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECl Write Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.237 PECl Command Write Data 8 Register – Index 12h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECl Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00_{HEX}.							

9.238 PECI Command Write Data 9 Register – Index 13h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00 _{HEX} .							

9.239 PECI Command Write Data 10 Register – Index 14h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00 _{HEX} .							

9.240 PECI Command Write Data 11 Register – Index 15h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be sent to client. Default value is 00 _{HEX} .							

9.241 PECI Command Write Data 12 Register – Index 16h (Bank 7)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. Default value is 00_{HEX}.

9.242 PECI Agent Relative Temperature Register (ARTR) – Index 17h-1Eh (Bank 7)

These registers return the “raw data” retrieved from PECI GetTemp() command. These data could be the error codes (range: 8000H~81FFH) or relative temperatures to process the defined Tbase. The error code will only be updated in ARTR; while “Temperature Reading Register”, Bank7 Index 20h and 21h, will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is 8001_{HEX}, in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read / Write(When Virtual_En enable)

ADDRESS 17-1E	DESCRIPTION
17h[15:8],18h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
19h[15:8],1Ah[7:0]	Domain1 Relative Temperature Agent0 [15:0]
1Bh[15:8],1Ch[7:0]	Domain0 Relative Temperature Agent1 [15:0]
1Dh[15:8],1Eh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. (Sign) In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (Temperature[8:0])
5	TEMP_2. 0.5°C unit.
4	TEMP_4. 0.25°C unit.
3	TEMP_8. 0.125°C unit.
2	TEMP_16. 0.0625°C unit.
1	TEMP_32. 0.03125°C unit.
0	TEMP_64. 0.015625°C unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.

0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECL Temperature format

Error Code	Description	Host operation
8000 _{HEX}	General Sensor Error	No further processing.
8001 _{HEX}	Sensing Device Missing	
8002 _{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0°C back to the temperature readouts.
8003 _{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127 °C back to the temperature readouts.
8004 _{HEX}	Reserved	No further operation.
81FF _{HEX}		

9.243 PECL Alive Agent Register – Index 1Fh (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

Record which agentis able to respond to Ping().**Default value is 00_{HEX}.**

1: agent is able to respond to Ping() command. Agent alive

0: agent isn't able to respond to Ping() command. Agent is not alive

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECL Alive Agent	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~2	Reserve
1	1: agent1 is able to respond to Ping() command. Agent alive 0: agent1 isn't able to respond to Ping() command. Agent is not alive
0	1: agent0 is able to respond to Ping() command. Agent alive 0: agent0 isn't able to respond to Ping() command. Agent is not alive

9.244 PECL Temperature Reading Register (Integer) – Index 20h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	PECI Temperature Reading---Integer [9:2]							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7~0	Temperature value [9] (Sign bit) Temperature value [8:2] (Integer bits) Temperature value [1:0] (Fraction bits)

Note. Temperature reading register is count from raw data and Tbase, for example:

Raw data	+	Tbase	=	Temp Reading
Bank7, Index [17][18]	+	Bank7, Index [09]	=	Bank7, Index [20][21]

9.245 PECI Temperature Reading Register (Fraction) – Index 21h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							PECI Temperature Value[1:0]
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Temperature value [9] (Sign bit) Temperature value [8:2] (Integer bits) Temperature value [1:0] (Fraction bits)

9.246 PECI Command TN Count Value Register – Index 22h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Timing Negotiation count Value[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.247 PECI Command TN Count Value Register – Index 23h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				PECI Timing Negotiation count Value[11:8]			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.248 PECI Command Warning Flag Register – Index 24h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						Alert Value[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
1~0	Agent Alert Bit (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions. Default value is 00_{HEX}.

9.249 PECI Command FCS Data Register – Index 25h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserve		Wraning	CC_Fail	ZeroWFCS	AbortWFCS	BadRFCS	BadWFCS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
5~0	Retrieve PECI related data from client and host. Default value is 00_{HEX}.

9.250 PECI Command WFCS Data Register – Index 26h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI WFCS related data from client. Default value is 00 _{HEX} .

9.251 PECI RFCS Data Register – Index 27h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI RFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. Default value is 00 _{HEX} .

9.252 PECI AWFCs Data Register – Index 28h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI AWFCs							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PCI related data from client. Default value is 00 _{HEX} .

9.253 PECI CRC OUT WFCS Data Register – Index 29h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI CRC OUT WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. Default value is 00_{HEX}.

9.254 PECI Command Read Data 1 Register – Index 2Ah (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.255 PECI Command Read Data 2 Register – Index 2Bh (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.256 PECI Command Read Data 3 Register – Index 2Ch (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
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NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.257 PECI Command Read Data 4 Register – Index 2Dh (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.258 PECI Command Read Data 5 Register – Index 2Eh (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. Default value is 00_{HEX}.

9.259 PECI Command Read Data 6 Register – Index 2Fh (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be get from client. Default value is 00_{HEX}.							

9.260 PECl Command Read Data 7 Register – Index 30h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECl Read Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be get from client. Default value is 00_{HEX}.							

9.261 PECl Command Read Data 8 Register – Index 31h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECl Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be get from client. Default value is 00_{HEX}.							

9.262 PECl Command Read Data 9 Register – Index 32h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECl Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data would be get from client. Default value is 00_{HEX}.							

9.263 PECL Read Dimm Data 1 Register – Index 33h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECL Read CPU Agent0 Dimm0 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data will update when PECL Dimm enable. LSB bit is decimal point.							

9.264 PECL Read Dimm Data 2 Register – Index 34h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECL Read CPU Agent0 Dimm1 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data will update when PECL Dimm enable. LSB bit is decimal point.							

9.265 PECL Read Dimm Data 3 Register – Index 35h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECL Read CPU Agent1 Dimm0 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7~0	The data will update when PECL Dimm enable. LSB bit is decimal point.							

9.266 PECL Read Dimm Data 4 Register – Index 36h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent1 Dimm1 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Dimm enable. LSB bit is decimal point.

9.267 PECI Read Margin Data 1 Register – Index 37h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Read CPU Agent0 Margin Temp[9:8]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable. MSB bit is sign bit.

9.268 PECI Read Margin Data 2 Register – Index 38h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent0 Margin Temp[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable

9.269 PECI Read Margin Data 3 Register – Index 39h (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	Reserved						PECI Read CPU Agent1 Margin Temp[9:8]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable. MSB bit is sign bit.

9.270 PECI Read Margin Data 4 Register – Index 3Ah (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent1 Margin Temp[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable

9.271 PECI Read Dimm Index Data Register – Index 3Bh (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Dimm Index data							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	When PECI Read Dimm enable, the register will be index data

9.272 PECI Read Dimm Index Data Register – Index 3Ch (Bank 7)

Attribute: Read only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Margin Index data							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	When PECL Read Margin enable, the register will be index data

PECI Manual Command Address Table

Command Bank 7	Address CR 05 _{HEX}	WriteLength CR 06 _{HEX}	Read Length CR 07 _{HEX}	Command Code CR 08 _{HEX}
Ping	Addr	00	00	
GetDIB		01	08	F7
GetTemp		01	02	01
PCIRd30		06	02 / 03 / 05	61
PCIWr30		08 / 09 / 0B	01	65
PCIRdLocal30		05	02 / 03 / 05	E1
PCIWrLocal30		07 / 08 / 0A	01	E5
PKGrd30		05	02 / 03 / 05	A1
PKGWr30		07 / 08 / 0A	01	A5
IAMSRRd30		05	02 / 03 / 05 / 09	B1
IAMSRWr30		07 / 08 / 0A / 0E	01	B5

PECI Manual Command Read Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30	GetDIB	GetTemp
Command Code	61	65	E1	E5	A1	A5	B1	B5	F7	01
RdData 1 CR 2A _{HEX}	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	X	X
RdData 2 CR 2B _{HEX}	X	X	X	X	X	X	Data LSB_1	X	Device Info	X
RdData 3 CR 2C _{HEX}	X	X	X	X	X	X	Data LSB_2	X	Revision Number	X
RdData 4 CR 2D _{HEX}	X	X	X	X	X	X	Data LSB_3	X	Reserved 1	X
RdData 5 CR 2E _{HEX}	X	X	x	X	X	X	Data LSB_4	X	Reserved 2	X
RdData 6 CR 2F _{HEX}	Data LSB_1	X	Data LSB_1	X	Data LSB_1	X	Data LSB_5	X	Reserved 3	X
RdData 7 CR 30 _{HEX}	Data LSB_2	X	Data LSB_2	X	Data LSB_2	X	Data LSB_6	X	Reserved 4	X
RdData 8 CR 31 _{HEX}	Data LSB_3	X	Data LSB_3	X	Data LSB_3	X	Data LSB_7	X	Reserved 5	Temp_LB
RdData 9	Data	x	Data	X	Data	X	Data	X	Reserved	Temp_HB

CR 32 _{HEX}	MSB		MSB		MSB		MSB		6	
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PECI Manual Command Write Data Table

Command	PCI Rd30	PCI Wr30	PCI Rd Local30	PCI Wr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30
Command Code	61	65	E1	E5	A1	A5	B1	B5
WrData 1 CR 0B_{HEX}	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID
WrData 2 CR 0C_{HEX}	Addr LSB_1	Addr LSB_1	Addr LSB_1	Addr LSB_1	Index	Index	Processor ID	Processor ID
WrData 3 CR 0D_{HEX}	Addr LSB_2	Addr LSB_2	Addr LSB_2	Addr LSB_2	Param LSB	Param LSB	Addr LSB	Addr LSB
WrData 4 CR 0E_{HEX}	Addr LSB_3	Addr LSB_3	Addr MSB	Addr MSB	Param MSB	Param MSB	Addr MSB	Addr MSB
WrData 5 CR 0F_{HEX}	Addr MSB	Addr MSB	X	Data LSB_1	X	Data LSB_1	X	Data LSB_1
WrData 6 CR 10_{HEX}	X	Data LSB_1	X	Data LSB_2	X	Data LSB_2	X	Data LSB_2
WrData 7 CR 11_{HEX}	X	Data LSB_2	X	Data LSB_3	X	Data LSB_3	X	Data LSB_3
WrData 8 CR 12_{HEX}	X	Data LSB_3	X	Data MSB	X	Data MSB	X	Data LSB_4
WrData 9 CR 13_{HEX}	X	Data MSB	X	X	X	X	X	Data LSB_5
WrData10 CR 14_{HEX}	X	X	X	X	X	X	X	Data LSB_6
WrData11 CR 15_{HEX}	X	X	X	X	X	X	X	Data LSB_7
WrData12 CR 16_{HEX}	X	X	X	X	X	X	X	Data MSB

9.273 AUXFAN2 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved			AUXFAN2 SOURCE[4:0]			
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	<p>Stopduty_En: 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT2 Stop Value (Bank9, index05h) at most if necessary. (This function is for Thermal Cruise mode.)</p>
6-5	Reserved
4-0	<p>AUXFAN2 Temperature Source Select: Bits 4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as AUXFAN2 monitoring source. 0 0 0 1 0: Select CPUTIN as AUXFAN2 monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as AUXFAN2 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as AUXFAN2 monitoring source. 0 1 0 1 0: Select Virtual_TEMP2 as AUXFAN2 monitoring source. 0 1 0 1 1: Select Virtual_TEMP3 as AUXFAN2 monitoring source 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as AUXFAN2 monitoring source. 1 0 0 0 1: Select PECI Agent 1 as AUXFAN2 monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as AUXFAN2 monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as AUXFAN2 monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as AUXFAN2 monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as AUXFAN2 monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as AUXFAN2 monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as AUXFAN2 monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as AUXFAN2 monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as AUXFAN2 monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as AUXFAN2 monitoring source. 1 1 0 1 1: Select BYTE_TEMP1 as AUXFAN2 monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as AUXFAN2 monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as AUXFAN2 monitoring source. 1 1 1 1 1: Select Virtual_TEMP as AUXFAN2 monitoring source.</p>

Note. If the temperature source is selecting to PECI, please set Bank0 Index Aeh first for reading correct value.

9.274 AUXFAN2 Target Temperature Register / AUXFANIN2 Target Speed_L Register – Index 01h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN2 Target Temperature / AUXFANIN2 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
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Thermal Cruise™	DESCRIPTION	AUXFAN2 Target Temperature
Fan Speed Cruise™	DESCRIPTION	AUXFANIN2 Target Speed [7:0], [11:8] associate index 0C [3:0]

9.275 AUXFAN2 MODE Register / AUXFAN2 TOLERRANCE Register – Index 02h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 MODE					Reseved	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	AUXFANOUT2 Mode Select. 0000: AUXFANOUT2 is in Manual Mode. (Default) 0001: AUXFANOUT2 is in Thermal Cruise Mode. 0010: AUXFANOUT2 is as Speed Cruise Mode. 0100: AUXFANOUT2 is in SMART FAN IV Mode.
3	Reseved
2-0	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L.

9.276 AUXFANOUT2 Step Up Time Register – Index 03h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to increase its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.277 AUXFANOUT2 Step Down Time Register – Index 04h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FANTM mode, this register determines the amount of time AUXFANOUT2 takes to decrease its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.278 AUXFANOUT2 Stop Value Register – Index 05h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT2 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.279 AUXFANOUT2 Start-up Value Register – Index 06h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT2 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.280 AUXFANOUT2 Stop Time Register – Index 07h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT2 value to fall from the stop value to zero.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.281 AUXFANOUT2 Output Value Select Register – Index 09h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E4h] is the Default Speed Configuration Register of AUXFANOUT2.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.282 AUXFANIN2 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0	
NAME	Reserved	AUXFANIN2 TOL_H				AUXFANIN2 Target Speed_H			
DEFAULT	0	0				0			

BIT	DESCRIPTION								
7	Reserved								
6-4	AUXFANIN2 Tolerance_H [5:3]								
3-0	AUXFANIN2 Target Speed_H [11:8]								

9.283 AUXFAN2 (SMART FAN™ IV) Temperature 5 Register(T5) – Index 11h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 5							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION								
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 5 Register (T5).								

9.284 AUXFAN2 (SMART FAN™ IV) Temperature 6 Register(T6) – Index 12h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 6							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION							
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 6 Register (T6).							

9.285 AUXFAN2 (SMART FAN™ IV) Temperature 7 Register(T7) – Index 13h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 7							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION							
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 7 Register (T7).							

9.286 AUXFAN2 (SMART FAN™ IV) Temperature 8 Register(T8) – Index 14h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 8							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION							
7-0	SYSFAN (SMART FAN™ IV) Temperature 8 Register (T8).							

9.287 AUXFAN2 (SMART FAN™ IV) DC/PWM 5 Register – Index 17h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) DC/PWM 5							

DEFAULT	1	0	0	0	1	1	0	0
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BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) DC/PWM 5 Register.

9.288 AUXFAN2 (SMART FAN™ IV) DC/PWM 6 Register – Index 18h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) DC/PWM 6							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) DC/PWM 6 Register.

9.289 AUXFAN2 (SMART FAN™ IV) DC/PWM 7 Register – Index 19h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) DC/PWM 7							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) DC/PWM 6 Register.

9.290 AUXFAN2 (SMART FAN™ IV) DC/PWM 8 Register – Index 1Ah (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) DC/PWM 8							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) DC/PWM 8 Register.

9.291 AUXFAN2 (SMART FAN™ IV) Profile Temperature Register – Index 1Bh (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Profile Temperature							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Profile Temperature Register.

9.292 AUXFAN2 (SMART FAN™ IV) Profile Temperature Register – Index 1Ch (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	PF_Enable	Reserved				Profile Temperature Tolerance		
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7	PF_Enable : 0 : disable change profile function. 1 : enable change profile function.
6-3	Reserved
2-0	Profile Temperature Tolerance.

9.293 AUXFAN2 (SMART FAN™ IV) Compare Temperature Source2 Select Register – Index 1Dh (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			AUXFAN2 SOURCE2[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7-5	Reserved.
4-0	AUXFAN2 Temperature Source2 Select: Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as AUXFAN2 monitoring source. 0 0 0 1 0: Select CPUTIN as AUXFAN2 monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as AUXFAN2 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as AUXFAN2 monitoring source.

	0 1 0 1 0: Select Virtual_TEMP2 as AUXFAN2 monitoring source.
	0 1 0 1 1: Select Virtual_TEMP3 as AUXFAN2 monitoring source
	0 1 1 0 0: Reserved.
	0 1 1 0 1: Reserved.
	0 1 1 1 0: Reserved.
	0 1 1 1 1: Reserved.
	1 0 0 0 0: Select PECI Agent 0 as AUXFAN2 monitoring source.
	1 0 0 0 1: Select PECI Agent 1 as AUXFAN2 monitoring source.
	1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as AUXFAN2 monitoring source.
	1 0 0 1 1: Select PCH_CHIP_TEMP as AUXFAN2 monitoring source.
	1 0 1 0 0: Select PCH_CPU_TEMP as AUXFAN2 monitoring source.
	1 0 1 0 1: Select PCH_MCH_TEMP as AUXFAN2 monitoring source.
	1 0 1 1 0: Select Agent0 Dimm0 as AUXFAN2 monitoring source.
	1 0 1 1 1: Select Agent0 Dimm1 as AUXFAN2 monitoring source.
	1 1 0 0 0: Select Agent1 Dimm0 as AUXFAN2 monitoring source.
	1 1 0 0 1: Select Agent1 Dimm1 as AUXFAN2 monitoring source.
	1 1 0 1 0: Select BYTE_TEMP0 as AUXFAN2 monitoring source.
	1 1 0 1 1: Select BYTE_TEMP1 as AUXFAN2 monitoring source.
	1 1 1 0 0: Select PECI Agent 0 Calibration as AUXFAN2 monitoring source.
	1 1 1 0 1: Select PECI Agent 1 Calibration as AUXFAN2 monitoring source.
	1 1 1 1 1: Select Virtual_TEMP1 as AUXFAN2 monitoring source.

9.294 AUXFAN2 (SMART FAN™ IV) Compare Temperature Source3 Select Register – Index 1Eh (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 SOURCE3[4:0]							
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7-5	Reserved.
4-0	AUXFAN2 Temperature Source3 Select: Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as AUXFAN2 monitoring source. 0 0 0 1 0: Select CPUTIN as AUXFAN2 monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as AUXFAN2 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as AUXFAN2 monitoring source. 0 1 0 1 0: Select Virtual_TEMP2 as AUXFAN2 monitoring source. 0 1 0 1 1: Select Virtual_TEMP3 as AUXFAN2 monitoring source 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select PECI Agent 0 as AUXFAN2 monitoring source.

1 0 0 0 1: Select PECI Agent 1 as AUXFAN2 monitoring source.
1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as AUXFAN2 monitoring source.
1 0 0 1 1: Select PCH_CHIP_TEMP as AUXFAN2 monitoring source.
1 0 1 0 0: Select PCH_CPU_TEMP as AUXFAN2 monitoring source.
1 0 1 0 1: Select PCH_MCH_TEMP as AUXFAN2 monitoring source.
1 0 1 1 0: Select Agent0 Dimm0 as AUXFAN2 monitoring source.
1 0 1 1 1: Select Agent0 Dimm1 as AUXFAN2 monitoring source.
1 1 0 0 0: Select Agent1 Dimm0 as AUXFAN2 monitoring source.
1 1 0 0 1: Select Agent1 Dimm1 as AUXFAN2 monitoring source.
1 1 0 1 0: Select BYTE_TEMP0 as AUXFAN2 monitoring source.
1 1 0 1 1: Select BYTE_TEMP1 as AUXFAN2 monitoring source.
1 1 1 0 0: Select PECI Agent 0 Calibration as AUXFAN2 monitoring source.
1 1 1 0 1: Select PECI Agent 1 Calibration as AUXFAN2 monitoring source.
1 1 1 1 1: Select Virtual_TEMP1 as AUXFAN2 monitoring source.

9.295 AUXFAN2 (SMART FAN™ IV) Source Comparator Enable Register – Index 1Fh (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
1	Enable AUXFAN2 temperature source comparator.

9.296 AUXFAN2 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 1 Register (T1).

9.297 AUXFAN2 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	AUXFAN2 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 2 Register (T2).

9.298 AUXFAN2 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 3 Register (T3).

9.299 AUXFAN2 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 4 Register (T4).

9.300 AUXFAN2 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 1 Register.

9.301 AUXFAN2 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 9)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION							
7-0	AUXFAN2 (SMART FAN™ IV) PWM 2 Register.							

9.302 AUXFAN2 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 9)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION							
7-0	AUXFAN2 (SMART FAN™ IV) PWM 3 Register.							

9.303 AUXFAN2 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 9)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION							
7-0	AUXFAN2 (SMART FAN™ IV) PWM 4 Register.							

9.304 AUXFAN2 3-Wire Enable Register – Index 31h (Bank 9)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX2_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved
0	EN_AUX2_3WFAN (AUXFAN2 type setting) 0: 4-wire fan 1: 3-wire fan

9.305 AUXFAN2 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Critical Temperature Register

9.306 AUXFAN2 Enable Critical Duty – Index 36h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							
DEFAULT	0							

BIT	DESCRIPTION
7-1	Reserved
0	En_AUX2_CRITICAL_DUTY (set 0 in manual mode) 0: Load default Full Speed 8'hFF for AUXFANOUT2. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT2.

9.307 AUXFAN2 Critical Duty Register – Index 37h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	

7-0	AUXFAN2 Critical Duty.
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9.308 AUXFANOUT2 Critical Temperature Tolerance Register – Index 38h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							AUXFANOUT2 Critical Temperature Tolerance
DEFAULT	0				0	0	0	0

BIT	DESCRIPTION
7-3	Reserved
2-0	AUXFANOUT2 Critical Temperature Tolerance

9.309 AUXFAN2 PECLERR DUTY Enable Register – Index 3Fh (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX2_PECLERR_DUTY
DEFAULT	0				0	0	0	0

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_AUX2_PECLERR_DUTY 00 : Disable PECLERR DUTY FANOUT (default) 01: Enable PECLERR DUTY FANOUT, Used Index 41 PECL_ERR_AUXOUT2 Value for AUXFANOUT2. 10,11: Keep Full Speed

9.310 AUXFANOUT2 Pre-Configured Register For PECL Error – Index 41h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 pre-configured register for PECL error (PECL_ERR_AUXOUT2)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	AUXFANOUT2 pre-configured register for PECL error.

9.311 DUTY PER STEP Register – Index 66h (Bank 9)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.312 T1 Delay Time Register – Index 67h (Bank 9)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.313 AUXFAN3 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank A)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved			AUXFAN3 SOURCE[4:0]			
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	Stopduty_En: 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT2 Stop Value (Bank9, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	Reserved
4-0	AUXFAN3 Temperature Source Select: Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as AUXFAN3 monitoring source. 0 0 0 1 0: Select CPUTIN as AUXFAN3 monitoring source.

BIT	DESCRIPTION
	0 1 0 0 0: Select SMBUSMASTER 0 as AUXFAN3 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as AUXFAN3 monitoring source. 0 1 0 1 0: Select Virtual_TEMP2 as AUXFAN3 monitoring source. 0 1 0 1 1: Select Virtual_TEMP3 as AUXFAN3 monitoring source 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select PECI Agent 0 as AUXFAN3 monitoring source. 1 0 0 0 1: Select PECI Agent 1 as AUXFAN3 monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as AUXFAN3 monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as AUXFAN3 monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as AUXFAN3 monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as AUXFAN3 monitoring source. 1 0 1 1 0: Select Agent0 Dimm0 as AUXFAN3 monitoring source. 1 0 1 1 1: Select Agent0 Dimm1 as AUXFAN3 monitoring source. 1 1 0 0 0: Select Agent1 Dimm0 as AUXFAN3 monitoring source. 1 1 0 0 1: Select Agent1 Dimm1 as AUXFAN3 monitoring source. 1 1 0 1 0: Select BYTE_TEMP0 as AUXFAN3 monitoring source. 1 1 0 1 1: Select BYTE_TEMP1 as AUXFAN3 monitoring source. 1 1 1 0 0: Select PECI Agent 0 Calibration as AUXFAN3 monitoring source. 1 1 1 0 1: Select PECI Agent 1 Calibration as AUXFAN3 monitoring source. 1 1 1 1 1: Select Virtual_TEMP as AUXFAN3 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index Aeh first for reading correct value.

9.314 AUXFAN3 Target Temperature Register / AUXFANIN3 Target Speed_L Register – Index 01h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN3 Target Temperature / AUXFANIN2 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN3 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN3 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.315 AUXFAN3 MODE Register / AUXFAN2 TOLERRANCE Register – Index 02h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 MODE					Reseved	Tolerance of	

						AUXFAN3 Target Temperature or AUXFANIN3 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	AUXFANOUT3 Mode Select. 0000: AUXFANOUT3 is in Manual Mode. (Default) 0001: AUXFANOUT3 is in Thermal Cruise Mode. 0010: AUXFANOUT3 is as Speed Cruise Mode. 0100: AUXFANOUT3 is in SMART FAN IV Mode.
3	Reseved
2-0	Tolerance of AUXFAN3 Target Temperature or AUXFANIN3 Target Speed_L.

9.316 AUXFANOUT3 Step Up Time Register – Index 03h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FANTM mode, this register determines the amount of time AUXFANOUT3 takes to increase its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.317 AUXFANOUT3 Step Down Time Register – Index 04h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FANTM mode, this register determines the amount of time AUXFANOUT3 takes to decrease its value by one step.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.318 AUXFANOUT3 Stop Value Register – Index 05h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT3 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.319 AUXFANOUT3 Start-up Value Register – Index 06h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT3 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.320 AUXFANOUT3 Stop Time Register – Index 07h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT3 value to fall from the stop value to zero.

(211) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.321 AUXFANOUT3 Output Value Select Register – Index 09h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E4h] is the Default Speed Configuration Register of AUXFANOUT3.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.322 AUXFANIN3 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0	
NAME	Reserved	AUXFANIN3 TOL_H				AUXFANIN3 Target Speed_H			
DEFAULT	0	0				0			

BIT	DESCRIPTION							
7	Reserved							
6-4	AUXFANIN3 Tolerance_H [5:3]							
3-0	AUXFANIN3 Target Speed_H [11:8]							

9.323 AUXFAN3 (SMART FAN™ IV) Temperature 5 Register(T5) – Index 11h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 5							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION							
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 5 Register (T5).							

9.324 AUXFAN3 (SMART FAN™ IV) Temperature 6 Register(T6) – Index 12h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 6							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION							
7-0								

7-0	AUXFAN3 (SMART FAN™ IV) Temperature 6 Register (T6).
-----	--

9.325 AUXFAN3 (SMART FAN™ IV) Temperature 7 Register(T7) – Index 13h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 7							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION							
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 7 Register (T7).							

9.326 AUXFAN3 (SMART FAN™ IV) Temperature 8 Register(T8) – Index 14h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 8							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION							
7-0	SYSFAN (SMART FAN™ IV) Temperature 8 Register (T8).							

9.327 AUXFAN3 (SMART FAN™ IV) DC/PWM 5 Register – Index 17h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) DC/PWM 5							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION							
7-0	AUXFAN3 (SMART FAN™ IV) DC/PWM 5 Register.							

9.328 AUXFAN3 (SMART FAN™ IV) DC/PWM 6 Register – Index 18h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	AUXFAN3 (SMART FAN™ IV) DC/PWM 6							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) DC/PWM 6 Register.

9.329 AUXFAN3 (SMART FAN™ IV) DC/PWM 7 Register – Index 19h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) DC/PWM 7							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) DC/PWM 6 Register.

9.330 AUXFAN3 (SMART FAN™ IV) DC/PWM 8 Register – Index 1Ah (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) DC/PWM 8							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) DC/PWM 8 Register.

9.331 AUXFAN3 (SMART FAN™ IV) Profile Temperature Register – Index 1Bh (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Profile Temperature							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Profile Temperature Register.

9.332 AUXFAN3 (SMART FAN™ IV) Profile Temperature Register – Index 1Ch (Bank A)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	PF_Enable	Reserved				Profile Temperature Tolerance		
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7	PF_Enable : 0 : disable change profile function. 1 : enable change profile function.
6-3	Reserved
2-0	Profile Temperature Tolerance.

9.333 AUXFAN3 (SMART FAN™ IV) Compare Temperature Source2 Select Register – Index 1Dh (Bank A)

Attribute: Read/Write
 Size: 8 bits
 Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			AUXFAN3 SOURCE2[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7-5	Reserved.
4-0	AUXFAN3 Temperature Source2 Select: Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as AUXFAN3 monitoring source. 0 0 0 1 0: Select CPUTIN as AUXFAN3 monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as AUXFAN3 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as AUXFAN3 monitoring source. 0 1 0 1 0: Select Virtual_TEMP2 as AUXFAN3 monitoring source. 0 1 0 1 1: Select Virtual_TEMP3 as AUXFAN3 monitoring source 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select PECI Agent 0 as AUXFAN3 monitoring source. 1 0 0 0 1: Select PECI Agent 1 as AUXFAN3 monitoring source. 1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as AUXFAN3 monitoring source. 1 0 0 1 1: Select PCH_CHIP_TEMP as AUXFAN3 monitoring source. 1 0 1 0 0: Select PCH_CPU_TEMP as AUXFAN3 monitoring source. 1 0 1 0 1: Select PCH_MCH_TEMP as AUXFAN3 monitoring source.

	1 0 1 1 0: Select Agent0 Dimm0 as AUXFAN3 monitoring source.
	1 0 1 1 1: Select Agent0 Dimm1 as AUXFAN3 monitoring source.
	1 1 0 0 0: Select Agent1 Dimm0 as AUXFAN3 monitoring source.
	1 1 0 0 1: Select Agent1 Dimm1 as AUXFAN3 monitoring source.
	1 1 0 1 0: Select BYTE_TEMP0 as AUXFAN3 monitoring source.
	1 1 0 1 1: Select BYTE_TEMP1 as AUXFAN3 monitoring source.
	1 1 1 0 0: Select PECI Agent 0 Calibration as AUXFAN3 monitoring source.
	1 1 1 0 1: Select PECI Agent 1 Calibration as AUXFAN3 monitoring source.
	1 1 1 1 1: Select Virtual_TEMP1 as AUXFAN3 monitoring source.

9.334 AUXFAN3 (SMART FAN™ IV) Compare Temperature Source3 Select Register – Index 1Eh (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				AUXFAN3 SOURCE3[4:0]			
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7-5	Reserved.
4-0	<p>AUXFAN3 Temperature Source3 Select:</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as AUXFAN3 monitoring source.</p> <p>0 0 0 1 0: Select CPUTIN as AUXFAN3 monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as AUXFAN3 monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as AUXFAN3 monitoring source.</p> <p>0 1 0 1 0: Select Virtual_TEMP2 as AUXFAN3 monitoring source.</p> <p>0 1 0 1 1: Select Virtual_TEMP3 as AUXFAN3 monitoring source</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as AUXFAN3 monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as AUXFAN3 monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as AUXFAN3 monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as AUXFAN3 monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as AUXFAN3 monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as AUXFAN3 monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as AUXFAN3 monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as AUXFAN3 monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as AUXFAN3 monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as AUXFAN3 monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as AUXFAN3 monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as AUXFAN3 monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as AUXFAN3 monitoring source.</p>

	1 1 1 0 1: Select PECI Agent 1 Calibration as AUXFAN3 monitoring source. 1 1 1 1 1: Select Virtual_TEMP1 as AUXFAN3 monitoring source.
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9.335 AUXFAN3 (SMART FAN™ IV) Source Comparator Enable Register – Index 1Fh (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
1	Enable AUXFAN3 temperature source comparator.

9.336 AUXFAN3 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 1 Register (T1).

9.337 AUXFAN3 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 2 Register (T2).

9.338 AUXFAN3 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 3 Register (T3).

9.339 AUXFAN3 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 4 Register (T4).

9.340 AUXFAN3 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 1 Register.

9.341 AUXFAN3 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 2 Register.

9.342 AUXFAN3 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 3 Register.

9.343 AUXFAN3 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 4 Register.

9.344 AUXFAN3 3-Wire Enable Register – Index 31h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							
DEFAULT	0		0					

BIT	DESCRIPTION
7-1	Reserved
0	EN_AUX3_3WFAN (AUXFAN2 type setting) 0: 4-wire fan 1: 3-wire fan

9.345 AUXFAN3 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Critical Temperature Register

9.346 AUXFAN3 Enable Critical Duty – Index 36h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						En_AUX3_CRITICAL_DUTY	
DEFAULT	0						0	

BIT	DESCRIPTION
7-1	Reserved
0	En_AUX3_CRITICAL_DUTY (set 0 in manual mode) 0: Load default Full Speed 8'hFF for AUXFANOUT3. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT3.

9.347 AUXFAN3 Critical Duty Register – Index 37h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN3 Critical Duty.

9.348 AUXFANOUT3 Critical Temperature Tolerance Register – Index 38h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						AUXFANOUT3 Critical Temperature Tolerance	
DEFAULT	0						0	

BIT	DESCRIPTION
7-3	Reserved
2-0	AUXFANOUT3 Critical Temperature Tolerance

9.349 AUXFAN3 PECIERR DUTY Enable Register – Index 3Fh (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX3_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_AUX3_PECIERR_DUTY 00 : Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 PECL_ERR_AUXOUT3 Value for AUXFANOUT2. 10,11: Keep Full Speed

9.350 AUXFANOUT3 Pre-Configured Register For PECL Error – Index 41h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 pre-configured register for PECL error (PECL_ERR_AUXOUT3)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	AUXFANOUT3 pre-configured register for PECL error.

9.351 DUTY PER STEP Register – Index 66h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.

BIT	DESCRIPTION
3-0	DOWN unit.

9.352 T1 Delay Time Register – Index 67h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.353 AUXFANIN3 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank B)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN3 TOL_H			AUXFANIN3 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	Reserved
6-4	AUXFANIN3 Tolerance_H [5:3]
3-0	AUXFANIN3 Target Speed_H [11:8]

9.354 Real Time Hardware Status Register I – Index 01h (Bank C)

Attribute: Read Only

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		CPUTIN_STS	Reserved	Reserved	Reserved	Reserved	Reserved
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved.
5	CPUTIN_STS. CPUTIN Temperature Sensor Status. 1: Temperature exceeds the over-temperature value.

BIT	DESCRIPTION
	0: Temperature is under the hysteresis value.
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

9.355 Interrupt Status Register – Index 02h (Bank C)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.		SOURCE8 _SMI	SOURCE7 _SMI	SOURCE6 _SMI	SOURCE5 _SMI	SOURCE4 _SMI	SOURCE3 _SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved.
5	SMIOVT8. A one indicates the high limit of SMIOVT8 temperature has been exceeded.
4	SMIOVT7. A one indicates the high limit of SMIOVT7 temperature has been exceeded.
3	SMIOVT6. A one indicates the high limit of SMIOVT6 temperature has been exceeded.
2	SMIOVT5. A one indicates the high limit of SMIOVT5 temperature has been exceeded.
1	SMIOVT4. A one indicates the high limit of SMIOVT4 temperature has been exceeded.
0	SMIOVT3. A one indicates the high limit of SMIOVT3 temperature has been exceeded.

9.356 Interrupt Status Register – Index 03h (Bank C)

Attribute: Read Clear

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Shut_ SOURCE8_SMI	Shut_ SOURCE7_SMI	Shut_ SOURCE6_SMI	Shut_ SOURCE5_SMI	Shut_ SOURCE4_SMI	Shut_ SOURCE3_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved

BIT	DESCRIPTION
5	Shut_SOURCE8_SMI. "1" indicates the high limit of SMIOVT_SOURCE4 temperature of SMI# Shutdown mode has been exceeded.
4	Shut_SOURCE7_SMI. "1" indicates the high limit of SMIOVT_SOURCE4 temperature of SMI# Shutdown mode has been exceeded.
3	Shut_SOURCE6_SMI. "1" indicates the high limit of SMIOVT_SOURCE4 temperature of SMI# Shutdown mode has been exceeded.
2	Shut_SOURCE5_SMI. "1" indicates the high limit of SMIOVT_SOURCE4 temperature of SMI# Shutdown mode has been exceeded.
1	Shut_SOURCE4_SMI. "1" indicates the high limit of SMIOVT_SOURCE4 temperature of SMI# Shutdown mode has been exceeded.
0	Shut_SOURCE3_SMI. "1" indicates the high limit of SMIOVT_SOURCE3 temperature of SMI# Shutdown mode has been exceeded.

9.357 SMI3-8# Mask Register 1 – Index 04h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.	SMIOVT8	SMIOVT7	SMIOVT6	SMIOVT5	SMIOVT4	SMIOVT3	
DEFAULT	0		1	1	1	1	1	1

BIT	DESCRIPTION
7-6	Reserved.
5	SMIOVT8.
4	SMIOVT7.
3	SMIOVT6.
2	SMIOVT5.
1	SMIOVT4.
0	SMIOVT3.

A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register – Index 02h (BankC))

9.358 SMI3-8# Mask Register 3 – Index 05h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR0	Reserved	AUXFANIN3	Shut_CPU	Shut_SYS	AUXFANIN2	Reserved	Reserved
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION
7-6	Reserved.

BIT	DESCRIPTION
5	Shut_SOURCE8_SMI
4	Shut_SOURCE7_SMI
3	Shut_SOURCE6_SMI
2	Shut_SOURCE5_SMI
1	Shut_SOURCE4_SMI
0	Shut_SOURCE3_SMI

"1" disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register – Index 03h (Bank C)).

9.359 SMI/OVT3-8 Control Register – Index 06h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		DIS_OVT8	DIS_OVT7	DIS_OVT6	DIS_OVT5	DIS_OVT4	DIS_OVT3
DEFAULT	0		0	0	1	0	0	0

BIT	DESCRIPTION
7-6	Reserved
5	DIS_OVT8. 1: Disable SMIOVT Source8 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source8 temperature OVT output through pin OVT#. (Default)
4	DIS_OVT7. 1: Disable SMIOVT Source7 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source7 temperature OVT output through pin OVT#. (Default)
3	DIS_OVT6. 1: Disable SMIOVT Source6 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source6 temperature OVT output through pin OVT#. (Default)
2	DIS_OVT5. 1: Disable SMIOVT Source5 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source5 temperature OVT output through pin OVT#. (Default)
1	DIS_OVT4. 1: Disable SMIOVT Source4 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source4 temperature OVT output through pin OVT#. (Default)
0	DIS_OVT3. 1: Disable SMIOVT Source3 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source3 temperature OVT output through pin OVT#. (Default)

9.360 SMIOVT3-8 Temperature Source Configuration Register – Index 07h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		OVTMOD8	OVTMOD7	OVTMOD6	OVTMOD5	OVTMOD4	OVTMOD3
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-6	Reserved This bit should be set to zero.							
5	OVTMOD8. SMIOVT8 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.							
4	OVTMOD7. SMIOVT7 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.							
3	OVTMOD6. SMIOVT6 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.							
2	OVTMOD5. SMIOVT5 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.							
1	OVTMOD4. SMIOVT4 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.							
0	OVTMOD3. SMIOVT3 Mode Select. 0 : Compare Mode. (Default) 1 : Interrupt Mode.							

9.361 SMIOVT3-8 Temperature Source Configuration Register – Index 08h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		STOP8	STOP7	STOP6	STOP5	STOP4	STOP3
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION							
7-6	Reserved This bit should be set to zero.							
5	STOP8. 0: Monitor SMIOVT8 temperature source. 1: Stop monitoring SMIOVT38 temperature source.							

BIT	DESCRIPTION
4	STOP7. 0: Monitor SMIOVT7 temperature source. 1: Stop monitoring SMIOVT3 temperature source.
3	STOP6. 0: Monitor SMIOVT6 temperature source. 1: Stop monitoring SMIOVT6 temperature source..
2	STOP5. 0: Monitor SMIOVT5 temperature source. 1: Stop monitoring SMIOVT5 temperature source.
1	STOP4. 0: Monitor SMIOVT4 temperature source. 1: Stop monitoring SMIOVT4 temperature source.
0	STOP3. 0: Monitor SMIOVT3 temperature source. 1: Stop monitoring SMIOVT3 temperature source.

9.362 Configuration Register – Index 09h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		EN_WS1	EN_WS3	EN_WS3	EN_WS3	EN_WS3	EN_WS3
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION
7-6	RESERVED
5	Output type of SMIOVT8 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
4	Output type of SMIOVT7 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
3	Output type of SMIOVT6 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode..
2	Output type of SMIOVT5 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
1	Output type of SMIOVT4 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
0	Output type of SMIOVT3 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.

9.363 Configuration Register – Index 0Ah (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EN_ONE8	EN_ONE7	EN_ONE6	EN_ONE5	EN_ONE3	EN_ONE3	Reserved	
DEFAULT	0	0	0	0	0	0	0	

BIT	DESCRIPTION
7	Output type of SMIOVT8 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
6	Output type of SMIOVT7 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
5	Output type of SMIOVT6 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
4	Output type of SMIOVT5 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
3	Output type of SMIOVT4 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
2	Output type of SMIOVT3 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
1-0	RESERVED

9.364 SMIOVT3-8 Temperature Source Configuration Register – Index 0Ch (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Fault6	Fault5	Fault4	Fault3				
DEFAULT	0	0	0	0				

BIT	DESCRIPTION
7-6	Fault6. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times.

BIT	DESCRIPTION
	3 : Seven times.
5-4	Fault5. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
3-2	Fault4. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
1-0	Fault3. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.

9.365 SMIOVT3-8 Temperature Source Configuration Register – Index 0Dh (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				Fault8		Fault7	
DEFAULT	0				0		0	

BIT	DESCRIPTION
7-4	Reserved.
3-2	Fault8. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
1-0	Fault7. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.

9.366 SMIOVT3 Temperature Source Over-temperature (High Byte) Register – Index 1Ah (BankC)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	TOVF<8:1>. Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.367 SMIOVT4 Temperature Source Over-temperature (High Byte) Register – Index 1Bh (BankC)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	TOVF<8:1>. Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.368 SMIOVT5 Temperature Source Over-temperature (High Byte) Register – Index 1Ch (BankC)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	TOVF<8:1>. Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.369 SMIOVT6 Temperature Source Over-temperature (High Byte) Register – Index 1Dh (BankC)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							

DEFAULT	0	1	0	1	0	0	0	0
---------	---	---	---	---	---	---	---	---

BIT	DESCRIPTION
7-0	TOVF<8:1>. Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.370 SMIOVT7 Temperature Source Over-temperature (High Byte) Register – Index 1Eh (BankC)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	TOVF<8:1>. Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.371 SMIOVT8 Temperature Source Over-temperature (High Byte) Register – Index 1Fh (BankC)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	TOVF<8:1>. Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.372 SMIOVT3 Temperature Source Hysteresis (High Byte) Register – Index 20h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.373 SMIOVT4 Temperature Source Hysteresis (High Byte) Register – Index 21h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION							
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.							

9.374 SMIOVT5 Temperature Source Hysteresis (High Byte) Register – Index 22h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION							
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.							

9.375 SMIOVT6 Temperature Source Hysteresis (High Byte) Register – Index 23h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION							
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.							

9.376 SMIOVT7 Temperature Source Hysteresis (High Byte) Register – Index 24h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.377 SMIOVT8 Temperature Source Hysteresis (High Byte) Register – Index 25h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	THYST<8:1>. Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.378 SMIOVT3 Temperature Source Select Register – Index 26 (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	SMIOVT3 Temperature selection. Bits 4 3 2 1 0 0 0 0 0 1: Select SYSTIN as SMIOVT3 monitoring source. (Default) 0 0 0 1 0: Select CPUTIN as SMIOVT3 monitoring source. 0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT3 monitoring source. 0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT3 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved.

	0 1 1 1 1: Reserved.
	1 0 0 0 0: Select PECI Agent 0 as SMIOVT3 monitoring source.
	1 0 0 0 1: Select PECI Agent 1 as SMIOVT3 monitoring source.
	1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT3 monitoring source.
	1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT3 monitoring source.
	1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT3 monitoring source.
	1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT3 monitoring source.
	1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT3 monitoring source.
	1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT3 monitoring source.
	1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT3 monitoring source.
	1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT3 monitoring source.
	1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT3 monitoring source.
	1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT3 monitoring source.
	1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT3 monitoring source.
	1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT3 monitoring source.
	1 1 1 1 1: Select Virtual_TEMP as SMIOVT3 monitoring source.

9.379 SMIOVT4 Temperature Source Select Register – Index 27 (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	<p>SMIOVT4 Temperature selection.</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SMIOVT4 monitoring source. (Default)</p> <p>0 0 0 1 0: Select CPUTIN as SMIOVT4 monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT4 monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT4 monitoring source.</p> <p>0 1 0 1 0: Reserved.</p> <p>0 1 0 1 1: Reserved.</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as SMIOVT4 monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as SMIOVT4 monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT4 monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT4 monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT4 monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT4 monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT4 monitoring source.</p>

	1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT4 monitoring source.
	1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT4 monitoring source.
	1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT4 monitoring source.
	1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT4 monitoring source.
	1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT4 monitoring source.
	1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT4 monitoring source.
	1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT4 monitoring source.
	1 1 1 1 1: Select Virtual_TEMP as SMIOVT4 monitoring source.

9.380 SMIOVT5 Temperature Source Select Register – Index 28 (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	<p>SMIOVT5 Temperature selection.</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SMIOVT5 monitoring source. (Default)</p> <p>0 0 0 1 0: Select CPUTIN as SMIOVT5 monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT5 monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT5 monitoring source.</p> <p>0 1 0 1 0: Reserved.</p> <p>0 1 0 1 1: Reserved.</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as SMIOVT5 monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as SMIOVT5 monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT5 monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT5 monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT5 monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT5 monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT5 monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT5 monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT5 monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT5 monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT5 monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT5 monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT5 monitoring source.</p> <p>1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT5 monitoring source.</p> <p>1 1 1 1 1: Select Virtual_TEMP as SMIOVT5 monitoring source.</p>

9.381 SMIOVT6 Temperature Source Select Register – Index 29 (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	<p>SMIOVT6 Temperature selection.</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SMIOVT6 monitoring source. (Default)</p> <p>0 0 0 1 0: Select CPUTIN as SMIOVT6 monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT6 monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT6 monitoring source.</p> <p>0 1 0 1 0: Reserved.</p> <p>0 1 0 1 1: Reserved.</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as SMIOVT6 monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as SMIOVT6 monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT6 monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT6 monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT6 monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT6 monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT6 monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT6 monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT6 monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT6 monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT6 monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT6 monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT6 monitoring source.</p> <p>1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT6 monitoring source.</p> <p>1 1 1 1 1: Select Virtual_TEMP as SMIOVT6 monitoring source.</p>

9.382 SMIOVT7 Temperature Source Select Register – Index 2A (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
-----	---	---	---	---	---	---	---	---

NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	<p>SMIOVT7 Temperature selection.</p> <p>Bits</p> <p>4 3 2 1 0</p> <p>0 0 0 0 1: Select SYSTIN as SMIOVT7 monitoring source. (Default)</p> <p>0 0 0 1 0: Select CPUTIN as SMIOVT7 monitoring source.</p> <p>0 1 0 0 0: Select SMBUSMASTER 0 as SMIOVT7 monitoring source.</p> <p>0 1 0 0 1: Select SMBUSMASTER 1 as SMIOVT7 monitoring source.</p> <p>0 1 0 1 0: Reserved.</p> <p>0 1 0 1 1: Reserved.</p> <p>0 1 1 0 0: Reserved.</p> <p>0 1 1 0 1: Reserved.</p> <p>0 1 1 1 0: Reserved.</p> <p>0 1 1 1 1: Reserved.</p> <p>1 0 0 0 0: Select PECI Agent 0 as SMIOVT7 monitoring source.</p> <p>1 0 0 0 1: Select PECI Agent 1 as SMIOVT7 monitoring source.</p> <p>1 0 0 1 0: Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT7 monitoring source.</p> <p>1 0 0 1 1: Select PCH_CHIP_TEMP as SMIOVT7 monitoring source.</p> <p>1 0 1 0 0: Select PCH_CPU_TEMP as SMIOVT7 monitoring source.</p> <p>1 0 1 0 1: Select PCH_MCH_TEMP as SMIOVT7 monitoring source.</p> <p>1 0 1 1 0: Select Agent0 Dimm0 as SMIOVT7 monitoring source.</p> <p>1 0 1 1 1: Select Agent0 Dimm1 as SMIOVT7 monitoring source.</p> <p>1 1 0 0 0: Select Agent1 Dimm0 as SMIOVT7 monitoring source.</p> <p>1 1 0 0 1: Select Agent1 Dimm1 as SMIOVT7 monitoring source.</p> <p>1 1 0 1 0: Select BYTE_TEMP0 as SMIOVT7 monitoring source.</p> <p>1 1 0 1 1: Select BYTE_TEMP1 as SMIOVT7 monitoring source.</p> <p>1 1 1 0 0: Select PECI Agent 0 Calibration as SMIOVT7 monitoring source.</p> <p>1 1 1 0 1: Select PECI Agent 1 Calibration as SMIOVT7 monitoring source.</p> <p>1 1 1 1 1: Select Virtual_TEMP as SMIOVT7 monitoring source.</p>

9.383 SMIOVT8 Temperature Source Select Register – Index 2B (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	RESERVED
4-0	SMIOVT8 Temperature selection.

Bits	
4 3 2 1 0	
0 0 0 0 1:	Select SYSTIN as SMIOVT8 monitoring source. (Default)
0 0 0 1 0:	Select CPUTIN as SMIOVT8 monitoring source.
0 1 0 0 0:	Select SMBUSMASTER 0 as SMIOVT8 monitoring source.
0 1 0 0 1:	Select SMBUSMASTER 1 as SMIOVT8 monitoring source.
0 1 0 1 0:	Reserved.
0 1 0 1 1:	Reserved.
0 1 1 0 0:	Reserved.
0 1 1 0 1:	Reserved.
0 1 1 1 0:	Reserved.
0 1 1 1 1:	Reserved.
1 0 0 0 0:	Select PECI Agent 0 as SMIOVT8 monitoring source.
1 0 0 0 1:	Select PECI Agent 1 as SMIOVT8 monitoring source.
1 0 0 1 0:	Select PCH_CHIP_CPU_MAX_TEMP as SMIOVT8 monitoring source.
1 0 0 1 1:	Select PCH_CHIP_TEMP as SMIOVT8 monitoring source.
1 0 1 0 0:	Select PCH_CPU_TEMP as SMIOVT8 monitoring source.
1 0 1 0 1:	Select PCH_MCH_TEMP as SMIOVT8 monitoring source.
1 0 1 1 0:	Select Agent0 Dimm0 as SMIOVT8 monitoring source.
1 0 1 1 1:	Select Agent0 Dimm1 as SMIOVT8 monitoring source.
1 1 0 0 0:	Select Agent1 Dimm0 as SMIOVT8 monitoring source.
1 1 0 0 1:	Select Agent1 Dimm1 as SMIOVT8 monitoring source.
1 1 0 1 0:	Select BYTE_TEMP0 as SMIOVT8 monitoring source.
1 1 0 1 1:	Select BYTE_TEMP1 as SMIOVT8 monitoring source.
1 1 1 0 0:	Select PECI Agent 0 Calibration as SMIOVT8 monitoring source.
1 1 1 0 1:	Select PECI Agent 1 Calibration as SMIOVT8 monitoring source.
1 1 1 1 1:	Select Virtual_TEMP as SMIOVT8 monitoring source.

9.384 SYSFAN Virtual2 Temperature Register – Index 2Eh (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Virtual2 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN Virtual2 TEMP

9.385 SYSFAN Virtual3 Temperature Register – Index 2Fh (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Virtual3 Temperature							

DEFAULT	0	0	0	0	0	0	0	0
---------	---	---	---	---	---	---	---	---

BIT	DESCRIPTION
7-0	SYSFAN Virtual3 TEMP

9.386 CPUFAN Virtual2 Temperature Register – Index 30h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Virtual2 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN Virtual2 TEMP

9.387 CPUFAN Virtual3 Temperature Register – Index 31h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Virtual3 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN Virtual3 TEMP

9.388 AUXFAN2 Virtual2 Temperature Register – Index 36h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Virtual2 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 Virtual2 TEMP

9.389 AUXFAN2 Virtual3 Temperature Register – Index 37h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Virtual3 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 Virtual3 TEMP

9.390 AUXFAN3 Virtual2 Temperature Register – Index 38h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 Virtual2 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 Virtual2 TEMP

9.391 AUXFAN3 Virtual3 Temperature Register – Index 39h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 Virtual3 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 Virtual3 TEMP

9.392 SYSFAN Duty Control Register – Index 3Dh (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Hold time				Reserved	Enable force duty		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	

BIT	DESCRIPTION
7-4	Duty hold time : 0 0 0 : 0.5s.. 0 0 1 : 1s. 0 1 0 : 1.5s. 0 1 1 : 2s. 1 0 0 : 2.5s. 1 0 1 : 3s. 1 1 0 : 3.5s. 1 1 1 : 4s
3	Reserved
2-0	Enable fource duty : when the fanin count is larger than the following setting, the duty control will force output duty in specified value. 0 0 0 : 2 times. 0 0 1 : 6 times. 0 1 0 : 10 times. 0 1 1 : 14 times. 1 0 0 : 18 times. 1 0 1 : 22 times. 1 1 0 : 26 times. 1 1 1 : 30 times

9.393 SYSFAN Duty Control Register – Index 3Eh (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Value							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The output duty value

9.394 CPUFAN Duty Control Register – Index 3Fh (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Hold time				Reserved	Enable force duty		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Duty hold time :

BIT	DESCRIPTION
	0 0 0 : 0.5s.. 0 0 1 : 1s. 0 1 0 : 1.5s. 0 1 1 : 2s. 1 0 0 : 2.5s. 1 0 1 : 3s. 1 1 0 : 3.5s. 1 1 1 : 4s
3	Reserved
2-0	Enable fource duty : when the fanin count is larger than the following setting, the duty control will force output duty in specified value. 0 0 0 : 2 times. 0 0 1 : 6 times. 0 1 0 : 10 times. 0 1 1 : 14 times. 1 0 0 : 18 times. 1 0 1 : 22 times. 1 1 0 : 26 times. 1 1 1 : 30 times

9.395 CPUFAN Duty Control Register – Index 40h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Value							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The output duty value

9.396 AUXFAN2 Duty Control Register – Index 45h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0	
NAME	Duty Hold time				Reserved	Enable force duty			
DEFAULT	0	0	0	0	0	0	0	0	

BIT	DESCRIPTION
7-4	Duty hold time : 0 0 0 : 0.5s.. 0 0 1 : 1s.

BIT	DESCRIPTION
	0 1 0 : 1.5s. 0 1 1 : 2s. 1 0 0 : 2.5s. 1 0 1 : 3s. 1 1 0 : 3.5s. 1 1 1 : 4s
3	Reserved
2-0	Enable fource duty : when the fanin count is larger than the following setting, the duty control will force output duty in specified value. 0 0 0 : 2 times. 0 0 1 : 6 times. 0 1 0 : 10 times. 0 1 1 : 14 times. 1 0 0 : 18 times. 1 0 1 : 22 times. 1 1 0 : 26 times. 1 1 1 : 30 times

9.397 AUxFAN2 Duty Control Register – Index 46h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Value							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The output duty value

9.398 AUXFAN3 Duty Control Register – Index 47h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Hold time				Reserved	Enable force duty		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Duty hold time : 0 0 0 : 0.5s.. 0 0 1 : 1s. 0 1 0 : 1.5s. 0 1 1 : 2s.

BIT	DESCRIPTION
	1 0 0 : 2.5s. 1 0 1 : 3s. 1 1 0 : 3.5s. 1 1 1 : 4s
3	Reserved
2-0	Enable fource duty : when the fanin count is larger than the following setting, the duty control will force output duty in specified value. 0 0 0 : 2 times. 0 0 1 : 6 times. 0 1 0 : 10 times. 0 1 1 : 14 times. 1 0 0 : 18 times. 1 0 1 : 22 times. 1 1 0 : 26 times. 1 1 1 : 30 times

9.399 AUXFAN3 Duty Control Register – Index 48h (Bank C)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Duty Value							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The output duty value

9.400 HM Read Only Register

ADDRESS A6-A0	DESCRIPTION
00h	CPUVCORE reading
01h	VIN1 reading
02h	AVSB reading
03h	3VCC reading
04h	VIN0 reading
05h	Reserved
06h	Reserved
07h	3VSB reading
08h	VBAT reading
09h	VTT reading
0Ah	Reserved
0Bh	Reserved

ADDRESS A6-A0	DESCRIPTION
0Ch	Reserved
0Dh	Reserved
0Eh	Reserved
0Fh	VIN9 reading
10h	SYSTIN temperature reading
11h	CPUTIN temperature reading
12h	Reserved
13h	Reserved
14h	Reserved
15h	Reserved
16h	Reserved
17h	Reserved
18h	Reserved
19h	SYSFANOUT fan control temperature reading.
1Ah	CPUFANOUT fan control temperature reading.
1Bh	Reserved
1Ch	Reserved
1Dh	AUXFANOUT2 fan control temperature reading.
1Eh	AUXFANOUT3 fan control temperature reading.
1Fh	Reserved
20h	CPU_Weight temperature reading
21h	Reserved
22h	SYSFAN duty target reading.
23h	CPUFAN duty target reading.
24h	Reserved
25h	Reserved
26h	AUXFAN2 duty target reading.
27h	AUXFAN3 duty target reading.
28h	SYSFAN rpm target reading.
29h	CPUFAN rpm target reading.
2Ah	Reserved
2Bh	Reserved
2Ch	AUXFAN2 rpm target reading.
2Dh	AUXFAN3 rpm target reading.
2Eh	SYSFANIN COUNT High-byte reading
2Fh	SYSFANIN COUNT Low-byte reading
30h	CPUFANIN COUNT High-byte reading

ADDRESS A6-A0	DESCRIPTION
31h	CPUFANIN COUNT Low-byte reading
32h	Reserved
33h	Reserved
34h	Reserved
35h	Reserved
36h	AUXFANIN2 COUNT High-byte reading
37h	AUXFANIN2 COUNT Low-byte reading
38h	AUXFANIN3 COUNT High-byte reading
39h	AUXFANIN3 COUNT Low-byte reading
3Ah	SYSFANIN SPEED High-byte (rpm) reading
3Bh	SYSFANIN SPEED Low-byte (rpm) reading
3Ch	CPUFANIN SPEED High-byte (rpm) reading
3Dh	CPUFANIN SPEED Low-byte (rpm) reading
3Eh	Reserved
3Fh	Reserved
40h	Reserved
41h	Reserved
42h	AUXFANIN2 SPEED High-byte (rpm) reading
43h	AUXFANIN2 SPEED Low-byte (rpm) reading
44h	AUXFANIN3 SPEED High-byte (rpm) reading
45h	AUXFANIN3 SPEED Low-byte (rpm) reading
46h	Reserved
47h	Reserved
48h	Reserved
49h	Reserved
4Ah	Reserved
4Bh	Reserved
4Ch	SYSFANOUT Output Value reading
4Dh	CPUFANOUT Output Value reading
4Eh	Reserved
4Fh	Reserved
50h	AUXFANOUT2 Output Value reading
51h	AUXFANOUT3 Output Value reading
52h	PECI Agent 0 reading
53h	Reserved
54h	PECI Agent 1 reading
55h	Reserved

ADDRESS A6-A0	DESCRIPTION
56h	PCH_CHIP_CPU_MAX_TEMP reading
57h	PCH_CHIP_TEMP reading
58h	PCH_CPU_TEMP_H reading
59h	PCH_CPU_TEMP_L reading
5Ah	PCH_MCH_TEMP reading
5Bh	PCH_MCH_TEMP reading
5Ch	Agent0 Dimm0 reading
5Dh	Agent0 Dimm1 reading
5Eh	Agent1 Dimm0 reading
5Fh	Agent1 Dimm1 reading
60h	PCH_TSI0_TEMP_H reading
61h	PCH_TSI0_TEMP_L reading
62h	PCH_TSI1_TEMP_H reading
63h	PCH_TSI1_TEMP_L reading
64h	Reserved
65h	Reserved
66h	Reserved
67h	Reserved
68h	Reserved
69h	Reserved
6Ah	Reserved
6Bh	Reserved
6Ch	Reserved
6Dh	Reserved
6Eh	Reserved
6Fh	ByteTemp_H reading
70h	ByteTemp_L reading
71h	PECI Agent0 Calibration Temp reading
72h	PECI Agent1 Calibration Temp reading
73h	Reserved
74h	Reserved
75h	SMIOVT1 temperature source reading.
76h	SMIOVT2 temperature source reading.

10. UART PORT

10.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications; including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	BDLAB (Baud Rate Divisor Latch Access Bit). When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	SSE (Set Silence Enable). A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	PBFE (Parity Bit Fixed Enable). When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	EPE (Even Parity Enable). When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	PBE (Parity Bit Enable). When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	MSBE (Multiple Stop Bit Enable). Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	DLS1 (Data Length Select Bit 1). Defines the number of data bits that are sent or checked in each serial character.
0	DLS0 (Data Length Select Bit 0). Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits

DLS1	DLS0	DATA LENGTH
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 10-1 Register Summary for UART

Bit Number										
Register Address Base		0	1	2	3	4	5	6	7	
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable (PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

**: These bits are always 0 in 16450 Mode.

10.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	RF EI (RX FIFO Error Indication). In 16450 mode, this bit is always set to logical 0. In 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	TSRE (Transmitter Shift Register Empty). In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	TBRE (Transmitter Buffer Register Empty). In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	SBD (Silent Byte Detected). This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	NSER (No Stop Bit Error). This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	PBER (Parity Bit Error). This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	OER (Overrun Error). This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	RDR (RBR Data Ready). This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

10.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	Reserved
4	<p>Internal Loopback Enable. When this bit is set to logic 1, the UART enters diagnostic mode, as follows:</p> <ul style="list-style-type: none"> (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) → DSR#, RTS (bit 1 of HCR) → CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) → DCD#. <p>Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.</p>
3	IRQ Enable. The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	Loopback RI Input. This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	RTS (Request to Send). This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	DTR (Data Terminal Ready). This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

10.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	DCD (Data Carrier Detect). This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	RI (Ring Indicator). This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	DSR (Data Set Ready). This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	CTS (Clear to Send). This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	TDCD (DCD# Toggling). This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	FERI (RI Falling Edge). This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	TDSR (DSR# Toggling). This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	TCTS (CTS# Toggling). This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

10.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	MSB (RX Interrupt Active Level).	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	LSB (RX Interrupt Active Level).	
5-4	RESERVED	
3	DMS MODE SELECT. When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	TRANSMITTER FIFO RESET. Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	RECEIVER FIFO RESET. Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	FIFO ENABLE. This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

10.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION	
7-6	FIFOS ENABLED. Set to logical 1 when UFR, bit 0 = 1.	
5-4	RESERVED	
3	INTERRUPT STATUS BIT 2. In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table	

	below.						
2	INTERRUPT STATUS BIT 1.				These two bits identify the priority level of the pending interrupt, as shown in the table below.		
1	INTERRUPT STATUS BIT 0.						
0	0 IF INTERRUPT PENDING. This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.						

ISR				INTERRUPT SET AND FUNCTION				
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt	
0	0	0	1	-	-	No Interrupt pending	-	
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR	
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level	
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR	
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)	
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCCD = 1	Read HSR	

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

10.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	En_address_byte. 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	RX_ctrl. 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	RESERVED
3	EHSRI (Handshake Status Interrupt Enable). Set this bit to logical 1 to enable the handshake status register interrupt.
2	EUSRI (UART Receive Status Interrupt Enable). Set this bit to logical 1 to enable the UART status register interrupt.

BIT	DESCRIPTION
1	ETBREI (TBR Empty Interrupt Enable). Set this bit to logical 1 to enable the TBR empty interrupt.
0	ERDRI (RBR Data Ready Interrupt Enable). Set this bit to logical 1 to enable the RBR data ready interrupt.

10.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to $(2^{16} - 1)$. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode, the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	PRE-DIV: 1.625 14.769M HZ	PRE-DIV: 1.0 24M HZ	DECIMAL DIVISOR USED TO GENERATE 16X CLOCK	ERROR PERCENTAGE
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

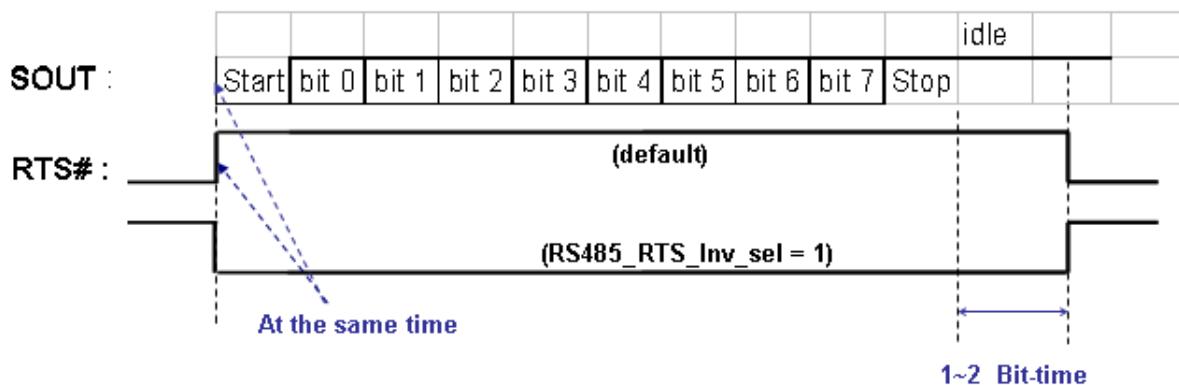
10.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

10.10 UART RS485 Auto Flow Control

NCT5582D supports RS485 auto flow control function for UARTA and UARTB. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA and UARTB when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA | UARTB.



The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1~2 x Bit-time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA and UARTB.

	UARTA	UARTB
RTS485_enable	Logic Device 2, CRF2_Bit7	Logic Device 3, CRF2_Bit7
RTS485_inv_sel	Logic Device 2, CRF2_Bit6	Logic Device 3, CRF2_Bit6

11. KEYBOARD CONTROLLER

The NCT5582D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

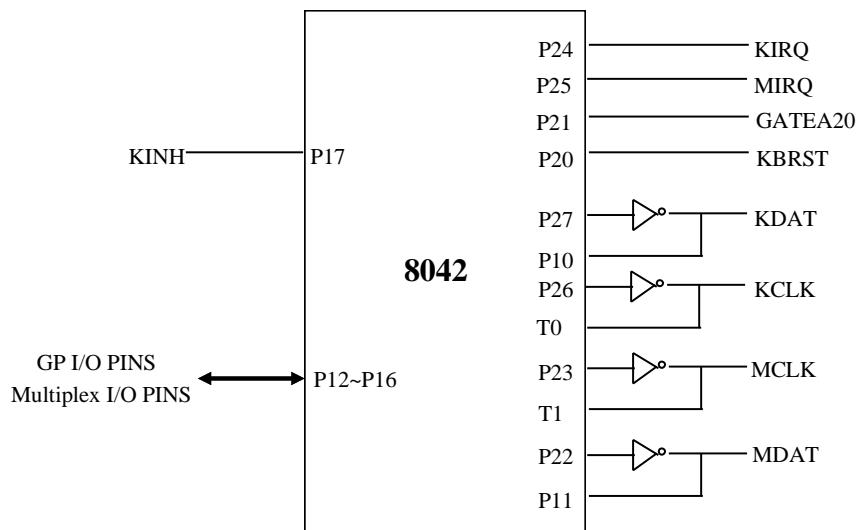


Figure 11-1 Keyboard and Mouse Interface

11.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

11.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

11.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 11-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

11.4 Commands

Table 11-2 KBC Command Sets

COMMAND	FUNCTION																		
20h	Read Command Byte of Keyboard Controller																		
60h	<p>Write Command Byte of Keyboard Controller</p> <table border="1"> <thead> <tr> <th>BIT</th><th>BIT DEFINITION</th></tr> </thead> <tbody> <tr> <td>7</td><td>Reserved</td></tr> <tr> <td>6</td><td>IBM Keyboard Translate Mode</td></tr> <tr> <td>5</td><td>Disable Auxiliary Device</td></tr> <tr> <td>4</td><td>Disable Keyboard</td></tr> <tr> <td>3</td><td>Reserve</td></tr> <tr> <td>2</td><td>System Flag</td></tr> <tr> <td>1</td><td>Enable Auxiliary Interrupt</td></tr> <tr> <td>0</td><td>Enable Keyboard Interrupt</td></tr> </tbody> </table>	BIT	BIT DEFINITION	7	Reserved	6	IBM Keyboard Translate Mode	5	Disable Auxiliary Device	4	Disable Keyboard	3	Reserve	2	System Flag	1	Enable Auxiliary Interrupt	0	Enable Keyboard Interrupt
BIT	BIT DEFINITION																		
7	Reserved																		
6	IBM Keyboard Translate Mode																		
5	Disable Auxiliary Device																		
4	Disable Keyboard																		
3	Reserve																		
2	System Flag																		
1	Enable Auxiliary Interrupt																		
0	Enable Keyboard Interrupt																		
A4h	<p>Test Password</p> <p>Returns 0Fah if Password is loaded</p> <p>Returns 0F1h if Password is not loaded</p>																		
A5h	<p>Load Password</p> <p>Load Password until a logical 0 is received from the system</p>																		
A6h	<p>Enable Password</p> <p>Enable the checking of keystrokes for a match with the password</p>																		
A7h	Disable Auxiliary Device Interface																		
A8h	Enable Auxiliary Device Interface																		
A9h	<p>Interface Test</p> <table border="1"> <thead> <tr> <th>BIT</th><th>BIT DEFINITION</th></tr> </thead> <tbody> <tr> <td>00</td><td>No Error Detected</td></tr> <tr> <td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr> <tr> <td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr> <tr> <td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr> <tr> <td>04</td><td>Auxiliary Device "Data" line is stuck high</td></tr> </tbody> </table>	BIT	BIT DEFINITION	00	No Error Detected	01	Auxiliary Device "Clock" line is stuck low	02	Auxiliary Device "Clock" line is stuck high	03	Auxiliary Device "Data" line is stuck low	04	Auxiliary Device "Data" line is stuck high						
BIT	BIT DEFINITION																		
00	No Error Detected																		
01	Auxiliary Device "Clock" line is stuck low																		
02	Auxiliary Device "Clock" line is stuck high																		
03	Auxiliary Device "Data" line is stuck low																		
04	Auxiliary Device "Data" line is stuck high																		
Aah	<p>Self-test</p> <p>Returns 055h if self-test succeeds</p>																		
Abh	<p>Interface Test</p> <table border="1"> <thead> <tr> <th>BIT</th><th>BIT DEFINITION</th></tr> </thead> <tbody> <tr> <td>00</td><td>No Error Detected</td></tr> <tr> <td>01</td><td>Keyboard "Clock" line is stuck low</td></tr> <tr> <td>02</td><td>Keyboard "Clock" line is stuck high</td></tr> <tr> <td>03</td><td>Keyboard "Data" line is stuck low</td></tr> <tr> <td>04</td><td>Keyboard "Data" line is stuck high</td></tr> </tbody> </table>	BIT	BIT DEFINITION	00	No Error Detected	01	Keyboard "Clock" line is stuck low	02	Keyboard "Clock" line is stuck high	03	Keyboard "Data" line is stuck low	04	Keyboard "Data" line is stuck high						
BIT	BIT DEFINITION																		
00	No Error Detected																		
01	Keyboard "Clock" line is stuck low																		
02	Keyboard "Clock" line is stuck high																		
03	Keyboard "Data" line is stuck low																		
04	Keyboard "Data" line is stuck high																		
Adh	Disable Keyboard Interface																		

COMMAND	FUNCTION
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6µs if the Command byte is even

11.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

11.5.1 KB Control Register (Logic Device 5, CR[F0])

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	KCLKS1.	Select the KBC clock rate. Bits 7 6 0 0: Reserved 0 1: Reserved 211 0: KBC clock input is 12 MHz. 1 1: Reserved
6	KCLKS0.	
5-3	RESERVED	
2	P92EN (Port 92 Enable). 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	HGA20 (Hardware GATEA 20). 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	HKBRST# (Hardware Keyboard Reset). 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a “D1” command, the hardware control logic sets or clears GATEA20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an “FE” command, the KBRESET is pulse low for 6 μ s (Min.) with a 14 μ s (Min.) delay.

GATEA20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATEA20 and KBRESET are merged with Port92 when the P92EN bit is set.

11.5.2 Port 92 Control Register (Default Value = 0x00)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						SGA20	PLKBRST#
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	RESERVED.
1	SGA20 (Special GATE A20 Control) 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	PLKBRST# (Pulled-low KBRESET). A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

12. CONSUMER INFRARED REMOTE (CIR)

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of H Level and L Level. The results are saved/stored in 32*8 RX FIFO. The max widths of H Level and L Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

12.1 CIR Register Table

Table 12-1 CIR Register Table

RC Block														
ExtAddr	Name	7	6	5	4	3	2	1	0					
base+0	IRCON	Reserved			RXEN	Reserved	RXINV	Sample Period Select						
base+1	IRSTS	RDR	RTR	PE	RFO	Reserved			GH					
base+2	IREN	RDR	RTR	PE	RFO	Reserved			GH					
base+3	RXFCONT	RXFIFO Count												
base+4	CP	Reserved												
base+5	CC	Reserved												
base+6	SLCH	Sample Limit Count High Byte												
base+7	SLCL	Sample Limit Count Low Byte												
base+8	FIFOCON	R				RXIFOCLR	R	Rx Trigger Level						
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	Reserved							
base+A	SRXFIFO	Sample RX FIFO												
base+B	TXFCONT	Reserved												
base+C	STXFIFO	Reserved												
base+D	FCCH	Reserved												
base+E	FCCL	Reserved												
base+F	IRFSM	R	Decoder FSM				Reserved							

12.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Received			RXEN	Reserved	RXINV	Sample Period Select	
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-5	Reserved
4	RX Enable
3	Reserved
2	IR Rx Invert Enable 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	Sample Period Select 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

12.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
Name	RDR	RTR	PE	RFO	Reserved			GH
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RX Data Ready (Writing 1 will clear the bit).
6	RX FIFO Trigger Level Reach (Writing 1 will clear the bit).
5	Packet End (Writing 1 will clear the bit).
4	RX FIFO Overrun (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3-1	Reserved
0	Min Length Detected (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

12.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	Reserved			GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	RX Data Ready
6	RX FIFO Trigger Level Reach
5	Packet End
4	RX FIFO Overrun (Overrun and Data Ready will be simultaneously generated).
3-1	Reserved
0	Min Length Detected

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

12.1.4 RX FIFO Count– Base Address + 3

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	RX FIFO Count

12.1.5 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

12.1.6 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

12.1.7 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Reserved
3	RX FIFO Cleared.
2	Reserved

1-0	RX Trigger Level Bits 2110 0 0: 1 0 1: 8 2110: 16 1 1: 24
-----	---

12.1.8 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	IR Pending 1: No Interrupt 0: Interrupt issue
6	Minimum Length Detect Status. This bit will be cleared when Packet End appears.
5	RX FIFO Trigger Level Active.
4	RX FIFO Empty Flag.
3	RX FIFO Full Flag.
2-0	Reserved

12.1.9 IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	Voltage Level 0: Low, 1: High
6-0	RX data length (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

12.1.10 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6	Decoder over status
5	Decoder continuing status
4	Decoder wait H status 1: idle, 0: RX busy
3-0	Encoder Level Output Status

12.1.11 IR Minimum Length Register – Base Address + F

Attribute: Write Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Min Length Register. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

13. CONSUMER INFRARED REMOTE (CIR) WAKE-UP

One of the features of the NCT5582D is system boot-up by a remote controller. The hardware will store a specifically appointed key command from the IR remote controller in the FIFO of 67Byte.

The same key is required to re-boot the system after the computer shut-down. Such way can be applied to any remote controllers. Learning is necessary only at the first time.

13.1 CIR WAKE-UP Register Table

RC Block															
ExtAddr	Name	7	6	5	4	3	2	1	0						
base+0	IRCON	DEC_RST	Mode[1]	Mode[0]	RXEN	IgnoreEN	RXINV	Sample Period Select							
base+1	IRSTS	RDR	RTR	PE	RFO	GH	R	R	IR Pending						
base+2	IREN	RDR	RTR	PE	RFO	GH	R								
Base+3		FIFO_COMPARE_DEEP													
base+4		FIFO_COMPARE_TOLERANCE													
base+5		FIFO_Count													
Base+6	SLCH	Sample Limit Count High Byte													
base+7	SLCL	Sample Limit Count Low Byte													
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level							
base+9	SRXFSTS	GS	FTA	Empty	Full	R									
base+A		Sample RX FIFO													
base+B		WR_FIFO_DATA													
Base+C		Read FIFO Only													
Base+D		Read FIFO Only Index													
Base+E		FIFO_Ignore													
Base+F	IRFSM	R	Decoder FSM			R		Wakeup Event							

13.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	DEC_RST	Mode[1]	Mode[0]	RXEN	Received	RXINV	Sample Period Select	
DEFAULT	0	0	1	0	0	1	1	0

BIT	DESCRIPTION
7	Reset CIR DECODER (Write 1 to clear)
6	Mode[1] : 0: FIFO can't be written 1: FIFO can be written
5	Mode[0] 0: Learning Mode 1: Wake up Mode (Before enter in Power S3 state, this bit should be set) This bit reset by VCC.
4	RX Enable
3	Ignore Bit Enable
2	IR Rx Invert Enable 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	Sample Period Select 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

13.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Received		IR_Pending
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RX Data Ready (Writing 1 will clear the bit).
6	RX FIFO Trigger Level Reach (Writing 1 will clear the bit).
5	Packet End (Writing 1 will clear the bit).
4	RX FIFO Overrun (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	Min Length Detected (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.
2-1	Reserved
0	IR Pending 1: No Interrupt 0: Interrupt issue

13.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	RX Data Ready
6	RX FIFO Trigger Level Reach
5	Packet End
4	RX FIFO Overrun (Overrun and Data Ready will be simultaneously generated).
3	Min Length Detected
2-0	Reserved

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

13.1.4 IR TX Configuration Register – Base Address + 3

Attribute: Read/Write

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Deep							
DEFAULT	0	1	0	0	0	0	1	1

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	When in S3 state, how many bytes need to compare. Default is 67 bytes.

13.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4

Attribute: Read/Write

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FIFO Data Tolerance between Learning mode and Wakeup mode. (Every byte) FIFO Date Tolerance = (Learning mode data) – (Wakeups mode data)

13.1.6 RX FIFO Count– Base Address + 5

Attribute: Read

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	RX FIFO Count

13.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

13.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

13.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Reserved
3	RX FIFO Cleared.
2	Reserved
1-0	RX Trigger Level Bits 2110 0 0: 67 0 1: 66 2110: 65 1 1: 64

13.1.10 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	GS	FTA	Empty	Full	Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Minimum Length Detect Status. This bit will be cleared when Packet End appears.
6	RX FIFO Trigger Level Active.
5	RX FIFO Empty Flag.
4	RX FIFO Full Flag.
3-0	Reserved

13.1.11 IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	Voltage Level 0: Low, 1: High
6-0	RX data length (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

13.1.12 Write FIFO – Base Address + B

Attribute: Write Only

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Write Sample RX FIFO						

BIT	DESCRIPTION
7	Voltage Level 0: Low, 1: High
6-0	RX data length (Unit : Sample Period)

Note. Before writing FIFO Data, mode[1] register should be set.

13.1.13 Read FIFO Only – Base Address + C

Attribute: Read Only

Size: 8 bits

Power Well: VRTC

Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION							
7	Voltage Level 0: Low, 1: High							
6-0	RX data length (Unit : Sample Period)							

Note. Only Read FIFO Data.

13.1.14 Read FIFO Index – Base Address + D

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Index							

BIT	DESCRIPTION							
7-0	Indicate that FIFO Index when only read FIFO data(Base Address + C)							

Note. Only Read FIFO Data.

13.1.15 Reserved – Base Address + E

13.1.16 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			Wake up event
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6-4	CIR State Machine
3-1	Reserved
0	Wake up event: 0: CIR wake up event has not been triggered. 1: CIR wake up event has been triggered. (Wake up event Read clear.)

13.1.17 IR Minimum Length Register – Base Address + F

Attribute: Write Only

Size: 8 bits

Power Well: VSB

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Min Length Register. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

14. POWER MANAGEMENT EVENT

14.1 Power Control Logic

This chapter describes how the NCT5582D implements its ACPI function via these power control pins: PSIN#, PSOUT#, SLP_S3# and PSON#. The following figure illustrates the relationships.

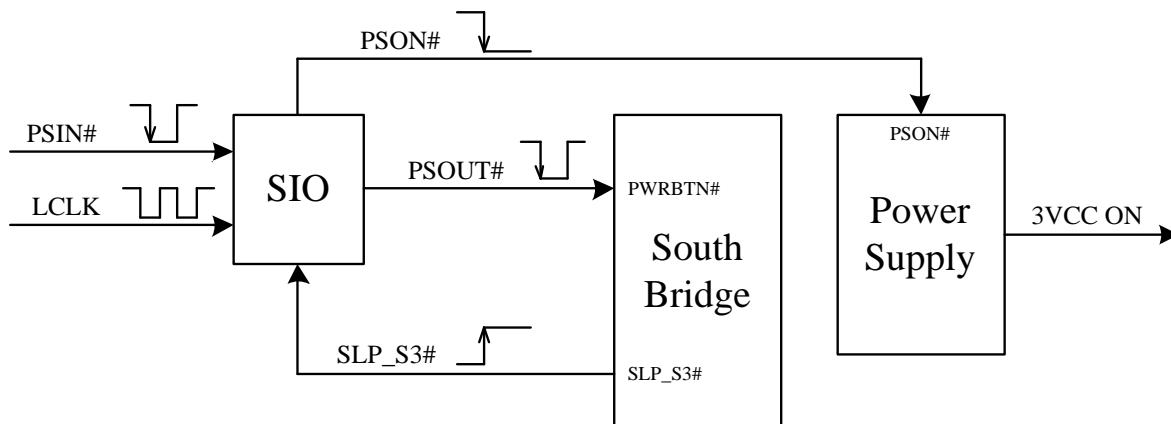


Figure 14-1 Power Control Mechanism

14.1.1 PSON# Logic

14.1.1.1 Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 14-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

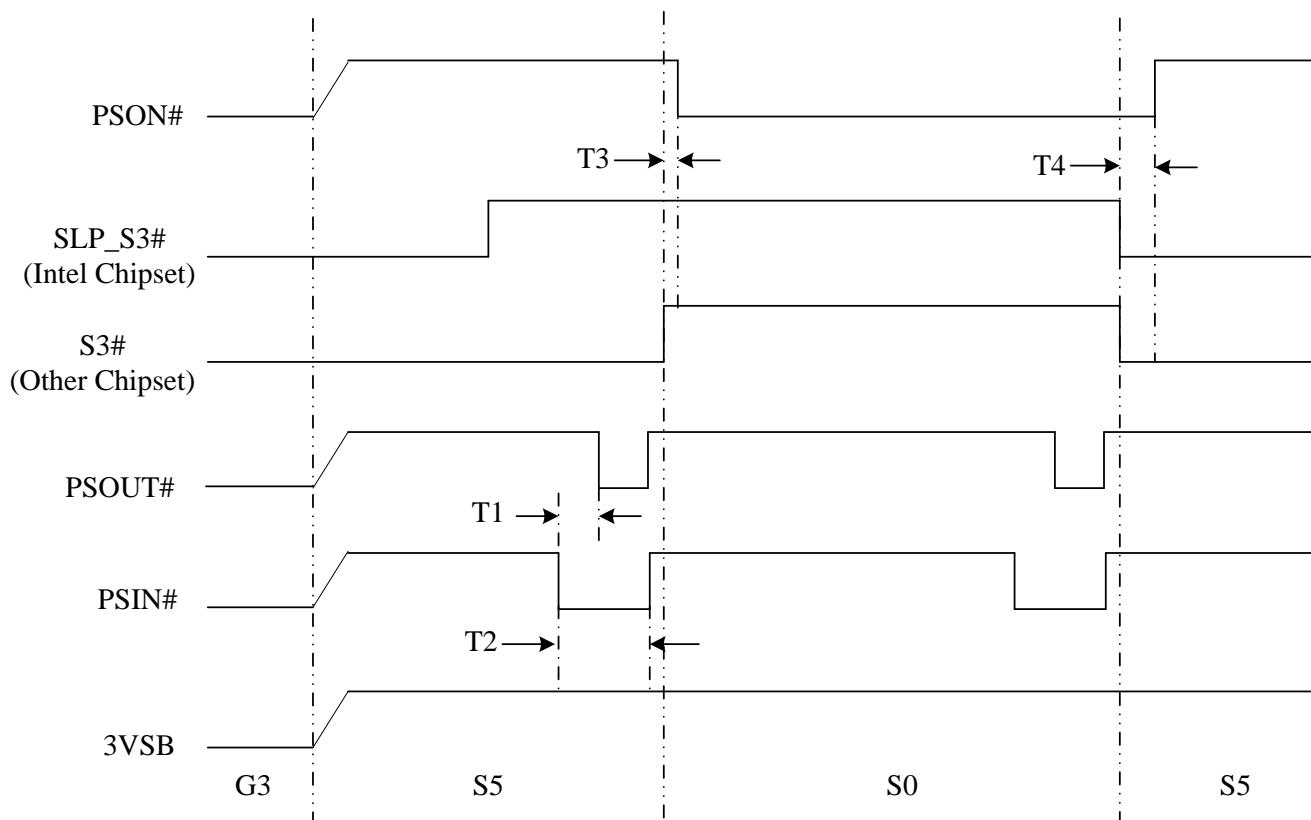


Figure 14-2 Power Sequence from S5 to S0, then Back to S5

14.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT5582D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 14-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
	Note 2)

Note1. The NCT5582D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

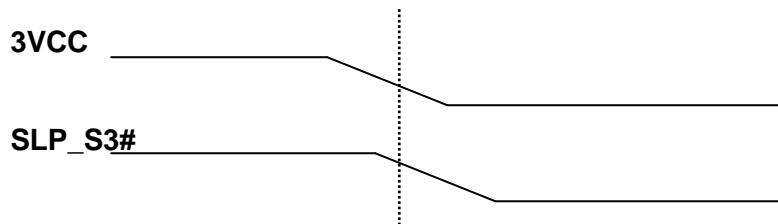


Figure 14-3 The previous state is “on”
3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

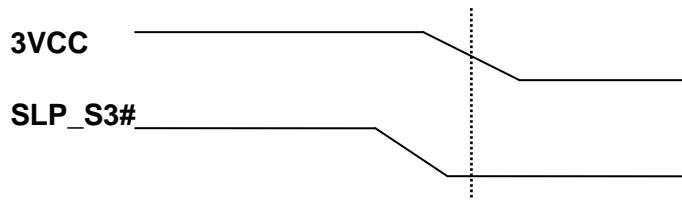


Figure 14-4 The previous state is “off”.
3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

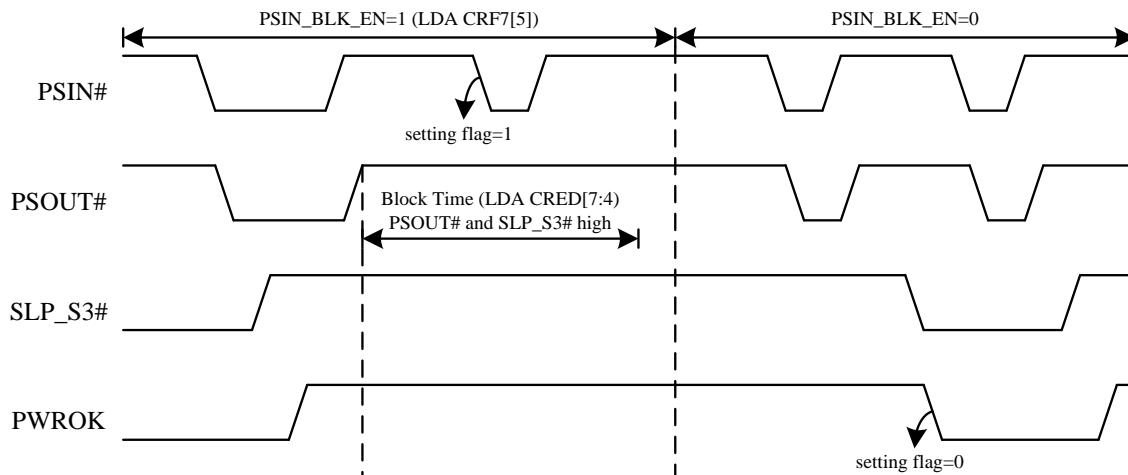
Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

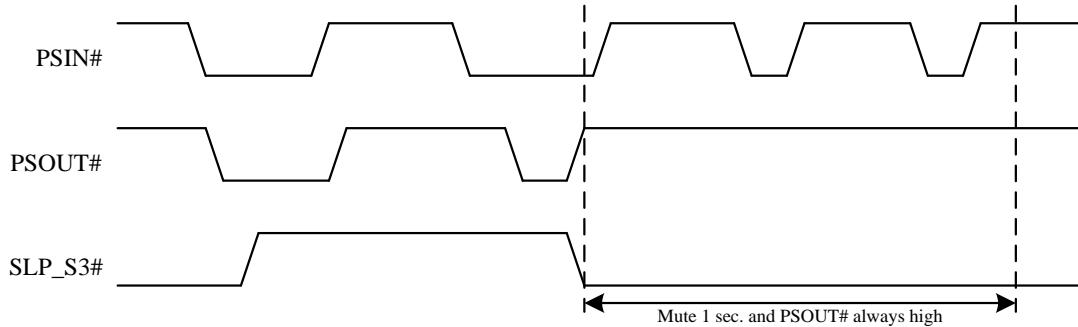
To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT5582D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

14.1.3 PSOUT Blocking Time

When PSOUT# and SLP_S3# signal is given, the time set by the user to block, the PSIN# signal will be not reaction PSOUT#, but can be recorded. When the system was S0 back to S5 and SLP_S3# Low, PSIN# signal will be isolated in one second, then PSOUT for high.



When the system was S0 back to S5 and SLP_S3 Low, PSIN# signal will be isolated in one second, the PSOUT# for high.



14.2 Wake Up the System by Keyboard and Mouse

The NCT5582D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT5582D works.

14.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to "1".

There are two keyboard events can be used for the wake-up

- 1) Any key – Set bit 0 at Logical Device A, CR[E0h] to "1" (Default).
- 2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to "0".

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of "0" is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

First sets of specific key can be set to serial or simultaneous password mode, second and third sets of specific keys only serial password mode. In simultaneous password mode, assume that we want to set "L Ctrl + L Alt + A" or "R Ctrl + R Alt + A" as the password (the password of simultaneous mode must be avoid ghost keys). The storage only fill the make code, except for the prefixed scan code of the password. The detail setting shows as below. Serial password mode descript as under section.

Index (CRE1)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data (CRE2)	14	11	1C	00	00	00	00	00	00	00	00	00	00	00	00

- L Ctrl / R Ctrl : 0x14h, 0xF0h, 0x14h / 0xE0h, 0x14h, 0xE0h, 0xF0h, 0x14h
- L Alt / R Alt : 0x11h, 0xF0h, 0x11h / 0xE0h, 0x11h, 0xE0h, 0xF0h, 0x11h
- A : 0x1Ch, 0xF0h, 0x1Ch

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index (CRE1)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data (CRE2)	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00

14.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to “1”.

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 14-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
0	1	0	Two clicks of the right button.

14.3 Resume Reset Logic

The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT5582D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 14-5 and Table 14-3.

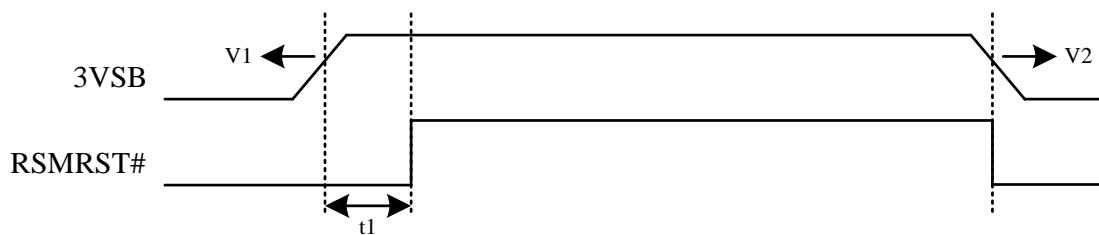


Figure 14-5 Mechanism of Resume Reset Logic

Table 14-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	2.94	3.00	V
V2	3VSB Ineffective Voltage	2.90	2.96	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

15. SERIALIZED IRQ

The NCT5582D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

15.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT5582D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT5582D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

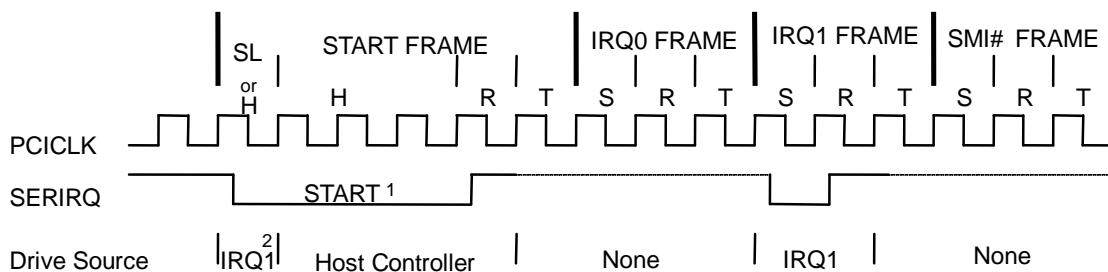


Figure 15-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control

SL=Slave Control

R=Recovery

T=Turn-around

S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT5582D because IRQ1 of the NCT5582D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

15.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT5582D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT5582D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT5582D device drives the SERIRQ high. During the Turn-around phase, the NCT5582D device leaves the SERIRQ tri-stated. The NCT5582D starts to drive the SERIRQ line from the beginning of “IRQ0 FRAME” based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 15-1.

Table 15-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	SIGNAL SAMPLED	# OF CLOCKS PAST START	EMPLOYED BY
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	IR
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

15.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

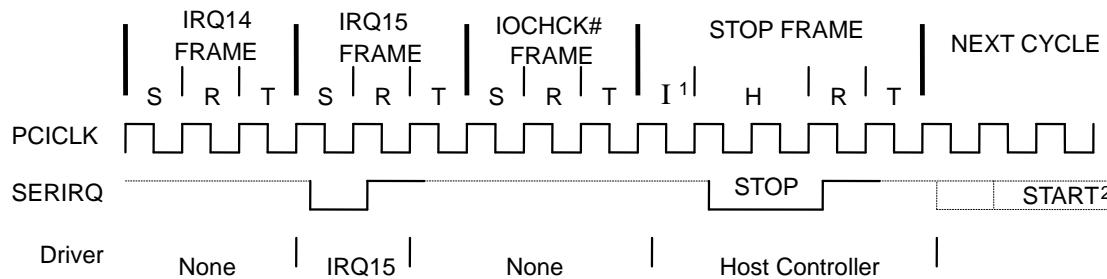


Figure 15-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I=Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

16. WATCHDOG TIMER

The Watchdog Timer 1 of the NCT5582D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7 provides an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0, GPIO2, GPIO4, GPIO6, bit[0],[4], GPIO3, bit[3], GPIO7, bit[0], PWROK and RESETCONO# will trigger a low pulse apporx 100mS or low level by Logical Device 8 CR[F5h], bit[0] and RSMRST# will trigger a low pulse electi 250ms. The PWROK, SLP_S3# and RSMRST# event also relate to acpi sequence, that can be control by Logical Device D, CR[F0h], bit[7] and bit[0], Logical Device D, CR[F0h], bit[7] and bit[0] as 2'b00 is normal acpi function, others timing illustrations are define in Figure 17-1 to Figure 17-3 In other words, when the value is counted down to zero, the timer stops, and the NCT5582D sets the WDT1 status bit in Logical Device 8, CR[F7h], bit[4]. Writing a zero will clear the status bit. It. This bit will also be cleared if LRESET# or PWROK signal is asserted.

The Watchdog Timer 3 of the NCT5582D consists of an 8-bit programmable time-out counter and a control and status register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F8h], bit[3]. The time-out value is set at Logical Device 8, CR[F9h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 3 time-out event is occurring, PWROK and RESETCONO# will trigger a low pluse apporx 100mS or low level by Logical Device 8 CR[F8h], bit[0]. In other words, when the value is counted down to zero, the timer stops, and the NCT5582D sets the WDT3 status bit in Logical Device 8, CR[Fah], bit[4]. Writing a zero will clear the status bit. It. This bit will also be cleared if LRESET# or PWROK signal is asserted.

The Watchdog Timer 4 of the NCT5582D consists of an status register (Logic Device D, CR[E7h] bit[6]). The timeout event will trigger RESETCONO pin to gerenate a pulse when RSTWDT_EN set to oen. CR[2Dh], bit[0] is RSTWDT_EN enable bit. When RSTWDT_EN set to one, if VCC3V is good, the timer will start count down, after 5 second, the timer time-out and to issue about 100ms low pulse to trigger pin.

Table 16-1 Watchdog Timer 1/3/4 Time-Out Trigger event

Watchdog Timer Time-Out Trigger Event	Watchdog Timer 1	Watchdog Timer 3	Watchdog Timer 4
			WDTRST_EN strapping, 5sec to issue RESETCON# if VCC3V is High
KBRST#	✓	✗	✗
PWROK	✗	✓	✗
GPIO Pin	✓	✗	✗
RESETCONO# Pin	✓	✓	✓

RSMRST# Event	✓	✗	✗
PWROK Event Then Into Deep S5	✓	✗	✗
Internal SLP_S3# Event Then Into Deep S5	✓	✗	✗

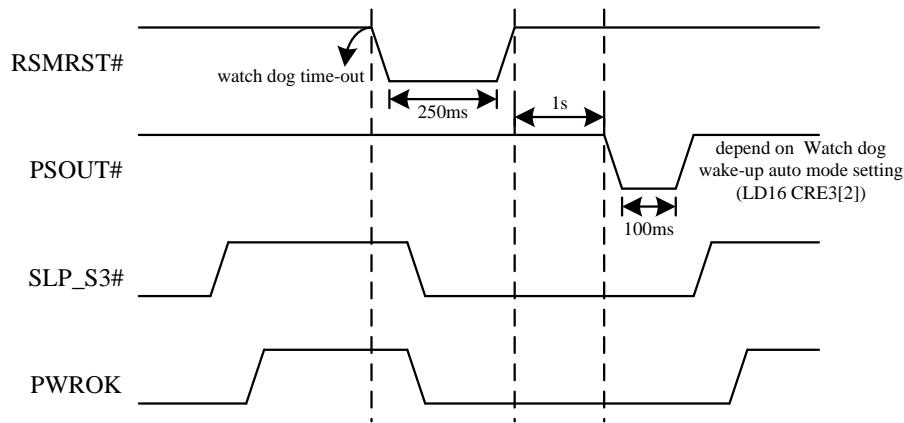


Figure 16-1 RSMRST# Event When Logical Device D CRF0 Bit[7] and Bit[0] as 2'b01

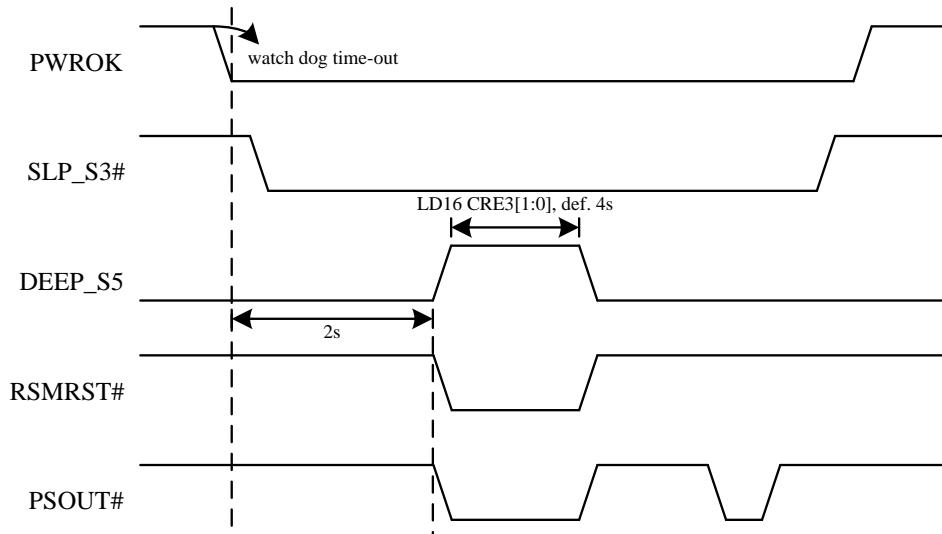


Figure 16-2 PWROK Event When Logical Device D CRF0 Bit[7] and Bit[0] as 2'b10

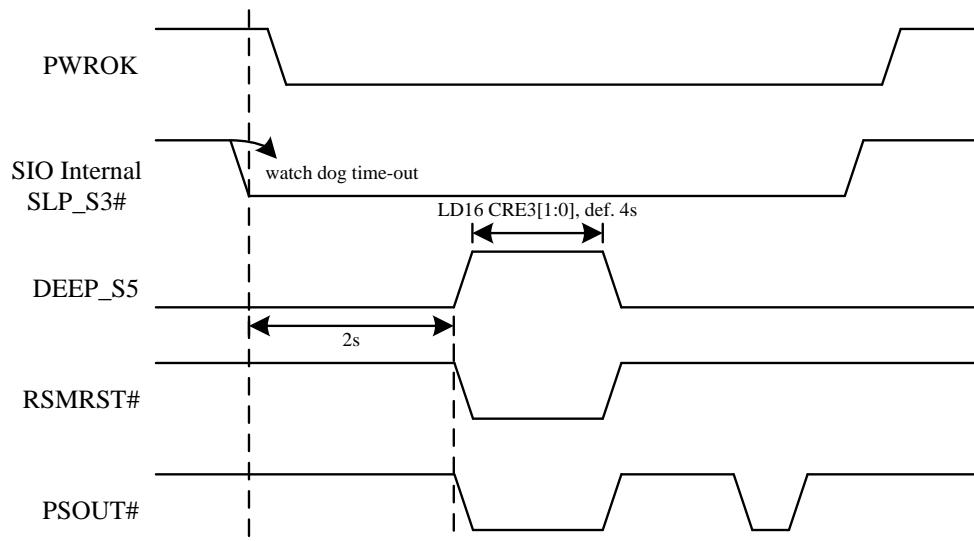


Figure 16-3 SLP_S3# Event When Logical Device D CRF0 Bit[7] and Bit[0] as 2'b11

17. GENERAL PURPOSE I/O

17.1 GPIO ARCHITECTURE

The NCT5582D provides 24 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non-inverse, 1 = inverse). Port value is read/write through data register.

In addition, only **GP31** and **GP32** are designed to be able to assert **PSOUT#** signal to wake up the system if any of them has falling transitions. The following table gives more detailed register map on GP31 and GP32.

Table 17-1 Relative Control Registers of GP31 and GP32 that Support Wake-Up Function

	EVENTROUTE I (PSOUT#)	EVENTROUTE II (PME#)
GP31	LDA, CR[Feh] bit[5]	LDA, CR[Feh] bit[1]
GP32	LDA, CR[Feh] bit[4]	LDA, CR[Feh] bit[0]

Table 17-2 GPIO Group Programming Table

Equips maximum 71-pin GPIOs.					
GPIO0 Group					
Enable: Logic Device 8, CR30[1] Data: Logic Device 8, E0~E3 Multi-function: WDT1, SMI, BEEP, MLED (Logic Device 8, CRE4[0~7]) Reset: Logic Device A, CRE9[0] OD/PP: Logic Device F, CRE9					
Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP03	2	GP03	Input	3VCC	
GPIO2 Group					
Enable: Logic Device 9, CR30[0] Data: Logic Device 9, E0~E3 Multi-function: WDT1, SMI, BEEP, GRN, OVT (Logic Device 9, CRE9[0~7]) Reset: Logic Device A, CRE9[2] OD/PP: Logic Device F, CRE1					
Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP20	27	KDAT	Bi-direction	3VSB	
GP21	26	KCLK	Bi-direction	3VSB	CR2A[0]=1
GP22	25	MDAT	Bi-direction	3VSB	
GP23	24	MCLK	Bi-direction	3VSB	CR2A[1]=1

GP24	46	CIRRX	Input	3VSB	CR1B[4]=0, CR27[3]=0
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GPIO3 Group

Enable: Logic Device 9, CR30[1]

Data: Logic Device 9, E4~E7

Multi-function: SMI, BEEP, GRN, WDT1, FDLED4 (Logic Device 9, CREA[0~7])

Reset: Logic Device A, CRE9[3]

OD/PP: Logic Device F, CRE2

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP30	41	RESETCONI#	Input	3VSB	CR1A[7:6]=01
GP31	37	GP31	Input	3VSB	
GP32	36	GP32	Input	3VSB	
GP33	35	3VSBSW#	Output (OD)	3VSB	CR2C[6:5]=01

GPIO4 Group

Enable: Logic Device 9, CR30[2]

Data: Logic Device 9, F0~F2, E8

Multi-function: WDT1, SMI, BEEP, YLW (Logic Device 9, CREE[0~7])

Reset: Logic Device A, CRE9[4]

OD/PP: Logic Device F, CRE3

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO		
GP47	22	0	RESETCONO#	0	Output (OD)	3VSB	CR1B[7]=1

GPIO5 Group

Enable: Logic Device 9, CR30[3]

Data: Logic Device 9, F4~F7

Multi-function: GRN, YLW, SLPS5_Lch, FDLED1 (Logic Device 8, CREB[0~7])

Reset: Logic Device A, CRE9[5]

OD/PP: Logic Device F, CRE4

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP56	44	{DDR4_EN}	{DDR4_EN}	3VSB	
		0 GP56	0 Input		
		1 VDDQ_EN	1 Output (OD)		
GP57	43	{DDR4_EN}	{DDR4_EN}	3VSB	
		0 GP57	0 Input		
		1 VPP_EN	1 Output (OD)		
		0 GP67	0 Input		
		1 DGH_L	1 Output		

GPIO7 Group

Enable: Logic Device 7, CR30[1]

Data: Logic Device 7, E0~E3

Multi-function: MLED, GRN, BEEP, SMI, WDT1 (Logic Device 7, CREC[0~7])

Reset: Logic Device A, CRE5[4]

OD/PP: Logic Device F, CRE6

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP71	33	{UARTBP80_EN}		{UARTBP80_EN}		3VSB	CR2B[1:0]=00
		0	GP71	0	Input		
		1	SOUT_PORT80	1	Output		
GP75	39	RSTOUT1#		Output		3VSB	CR2B[5:4]=01
GP76	38	RSTOUT2#		Output		3VSB	CR2B[7:6]=01

GPIO8 Group

Enable: Logic Device 7, CR30[2]

Data: Logic Device 7, E4~E7

Multi-function: GRN, YLW, BEEP, SMI, WDT1 (Logic Device 7, CRED[0~7])

Reset: Logic Device A, CRE5[5]

OD/PP: Logic Device F, CRE7

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP80	14	GP80		Input		3VSB	
GP81	15	GP81		Input		3VSB	
GP82	16	GP82		Input		3VSB	
GP83	17	GP83		Input		3VSB	
GP84	18	GP84		Input		3VSB	
GP85	19	{UARTAP80_EN}		{UARTAP80_EN}		3VSB	
		0	GP85	0	Input		
		1	SOUTA_P80	1	Output		
GP86	20	GP86		Input		3VSB	
GP87	21	GP87		Input		3VSB	

17.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 17-3. Base address plus 0 to 4 are GPIO registers, base address plus 5 to 7 are watchdog registers. Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#8 for GPIO0 ~ GPIO8 respectively). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time.

Table 17-3 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER											
		7	6	5	4	3	2	1	0				
Base + 0	GSR	Reserved				INDEX							
Base + 1	IOR	GPIO I/O Register											
Base + 2	DAT	GPIO Data Register											
Base + 3	INV	GPIO Inversion Register											
Base + 4	DST	GPIO Status Register											
Base + 5	Wdtmod	Watchdog Timer 1 (WDT1) and KBC P20 Control Mode Register											
Base + 6	Wdttim	Watchdog Timer 1 (WDT1) Control Register											
Base + 7	Wdtsts	Watchdog Timer 1 (WDT1) Status Register											

18. SMBUS MASTER INTERFACE

18.1 General Description

The SMBus interface module is two wire serial interface compatible to the SMBus physical layer. It is also compatible with Intel's SMBus and Philips' I²C bus.

The rest of this section introduces the various features of the SMBus master capability. These features are divided into the following sections:

- ◆ SMBus and I²C compliant
- ◆ PCH
- ◆ SMBus master

18.2 Introduction to the SMBus Master

18.2.1 Data Transfer Format

Every byte transferred on the bus consists of 8 bits. After the start condition, the master places the 7-bit address to the slave device it wants to address on the bus. The address followed an eight bit indicating the direction of the data transfer (R/W#); a zero indicates a transmission for data while a one indicates a request for data. Each byte is transferred with the most significant bit first, and after each byte, an acknowledge signal must follow. A data transfer is always terminated by stop condition generated by master.

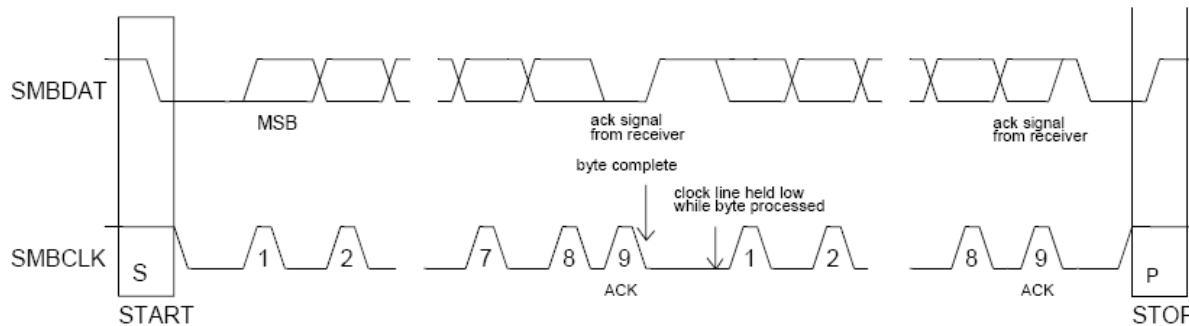


Figure 18-1 Data Transfer Format

18.2.2 Arbitration

Arbitration takes place on the SMBDAT data line while the SMBCLK line is high. Two devices may generate a start condition at the same time and enter the arbitration procedure. Arbitration continues until one master generates a HIGH level on the SMBDAT line while another competing master generates a LOW level on the SMBDAT line while SMBCLK is high. The master device which generated the HIGH level on SMBDAT loses arbitration. If a device loses arbitration during the first byte following a start condition i.e. while transmitting a slave address it becomes a slave receiver and monitors the address for a potential match. Arbitration may also be lost in the master receive mode during the acknowledge cycle.

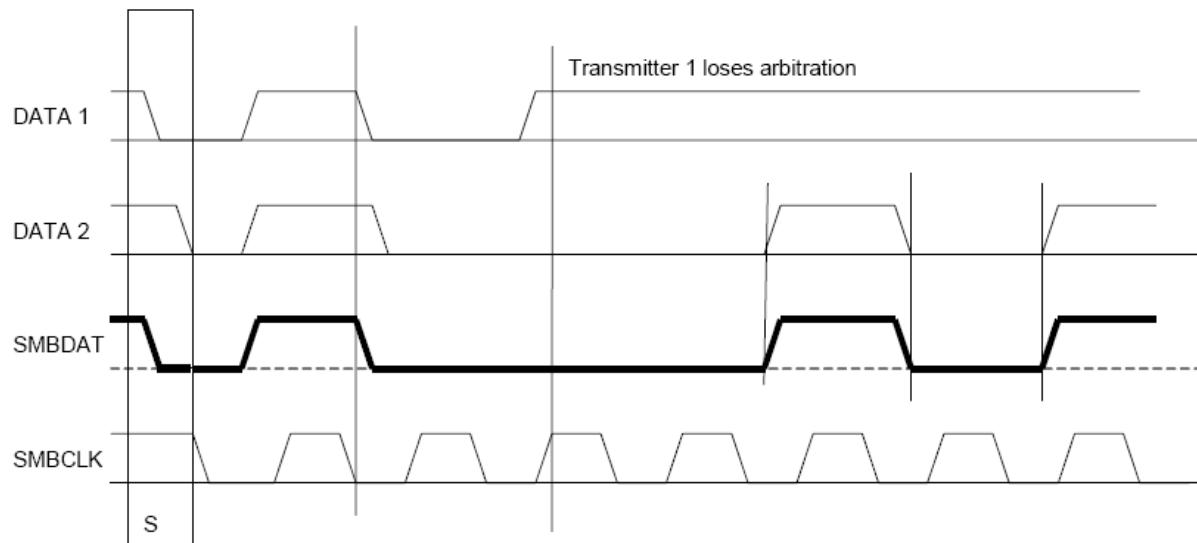


Figure 18-2 SMBus Arbitration

18.2.3 Clock Synchronization

Clock synchronization is performed while the arbitration procedure described above is in effect. Clock Synchronization takes place between two competing devices by utilizing the wired-AND nature of the SMBCLK line. The SMBCLK line will go low as soon as the master with the shortest high time pulls SMBCLK low. SMBCLK will remain low until the device with the longest SMBCLK low time relinquishes the SMBCLK line. Therefore the SMBCLK high time is determined by device with the shortest high time while the SMBCLK low time is determined by the device with the longest low time.

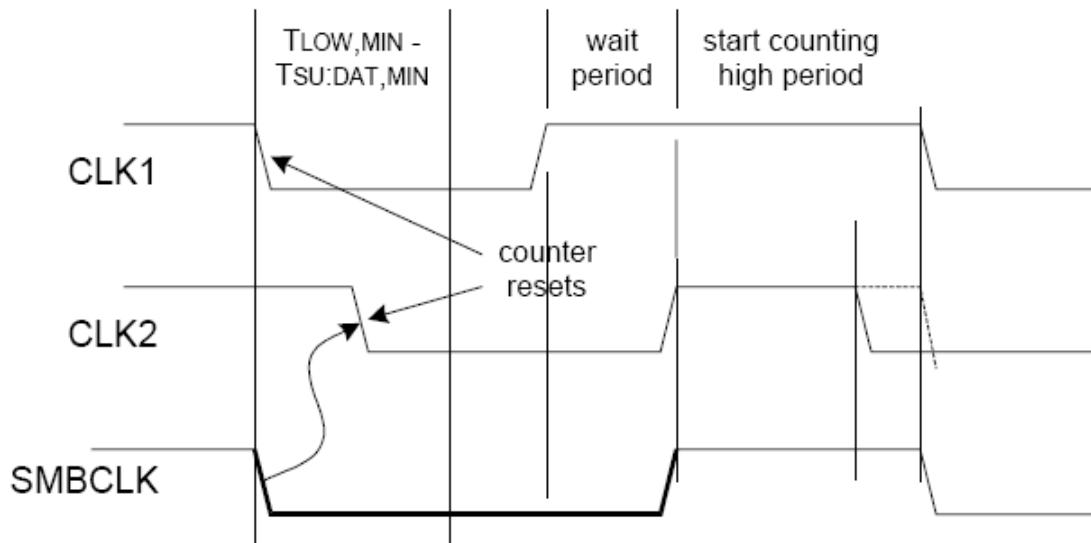


Figure 18-3 Clock synchronization

18.3 PCH

The PCH provide system thermal data to EC. The EC can manage the fans and other cooling elements based on this data. A subset of the thermal collection is that the PCH can be programmed to alert the EC when a device has gone outside of its temperature limits.

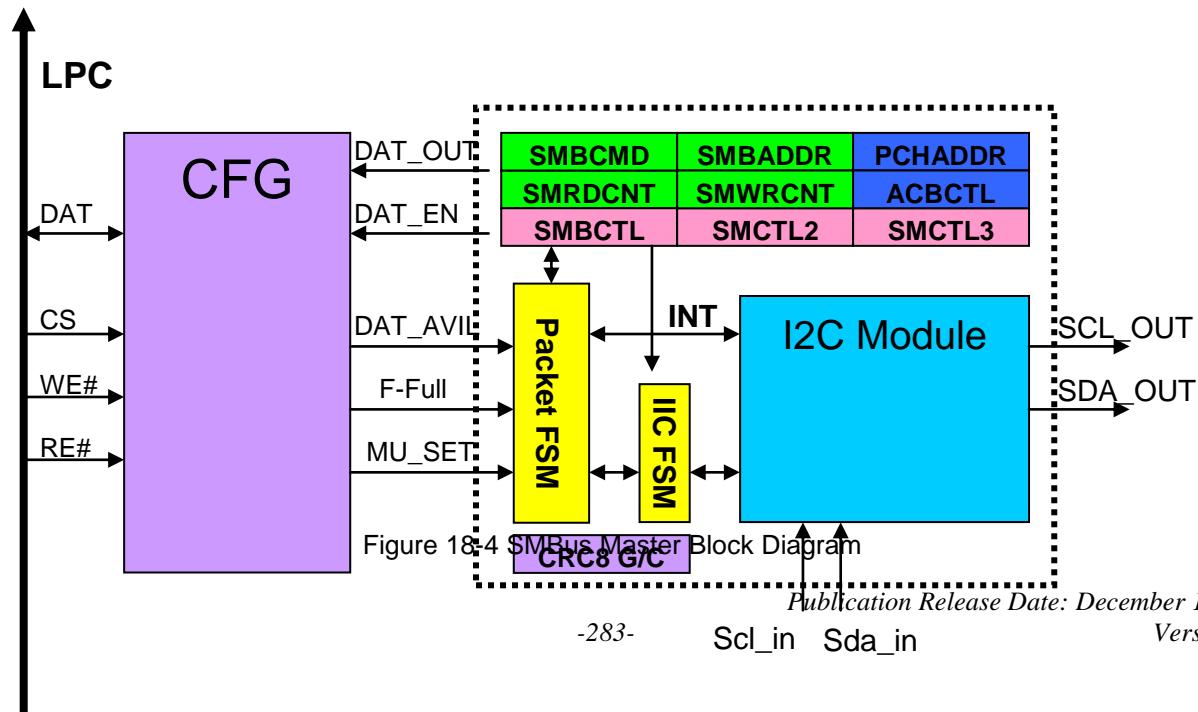
18.3.1 Command Summary

Table 18-1 PCH Command Summary

Trans-action	Slave Addr.	Data Byte 0 =Com mand	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write STS Preferences	I2C	0x41	0x6	STS [47:40]	STS [39:32]	STS [31:24]	STS [23:16]	STS [15:8]	STS [7:0]
Write CPU Temp Limits	I2C	0x42	0x6	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [15:8]		
Write MCH Temp Limits	I2C	0x43	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write IBX Temp Limits	I2C	0x44	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write DIMM Temp Limits	I2C	0x45	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write MPC CPU Power Clamp	I2C	0x50	0x2	Lower Limit [7:0]	Power Clamp [7:0]				
Block Read	Block Read Address	0x40	Block Read Address	Byte Count	Data 0	Data N	PEC (optional)		

18.4 SMBus Master

18.4.1 Block Diagram



18.4.2 Programming Flow

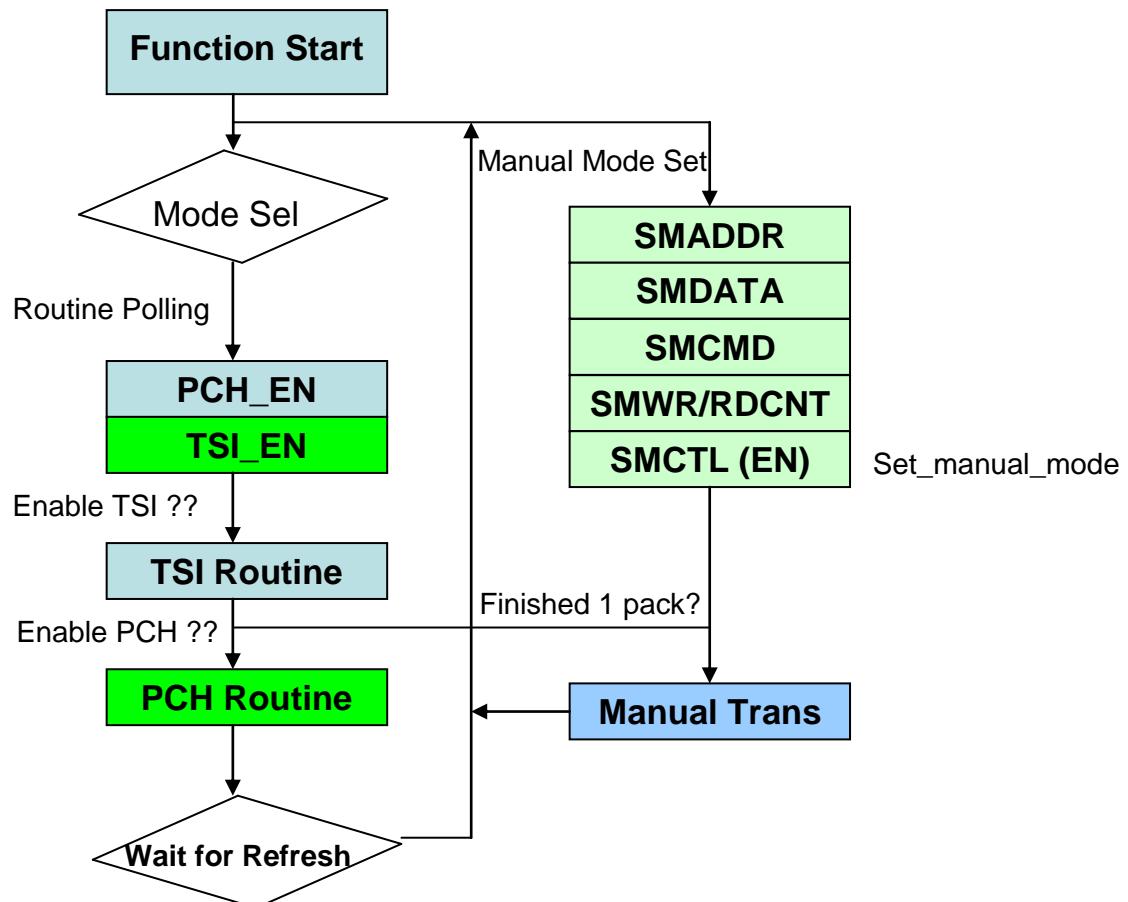


Figure 18-5 Programming Flow

18.4.3 TSI Routine

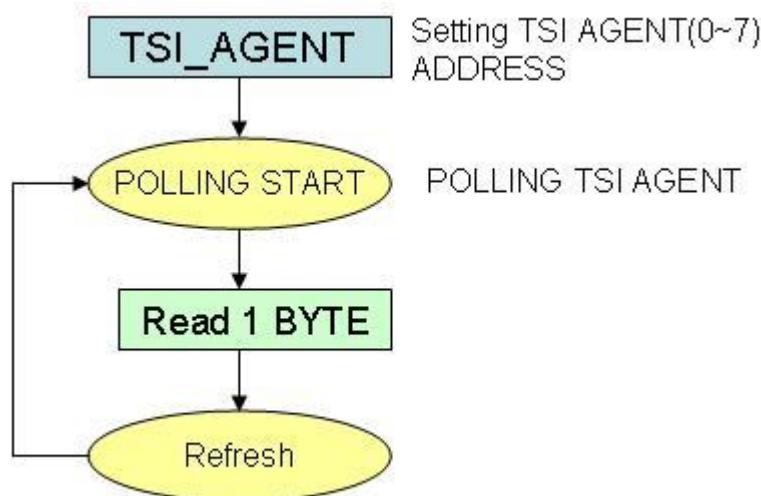


Figure 18-6 TSI Routine

18.4.4 PCH Routine

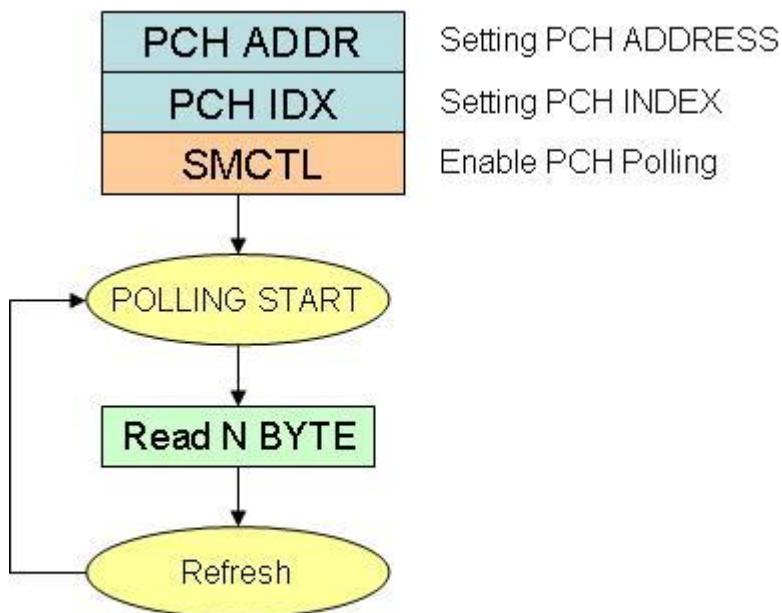


Figure 18-7 PCH Routine

18.4.5 BYTE Routine

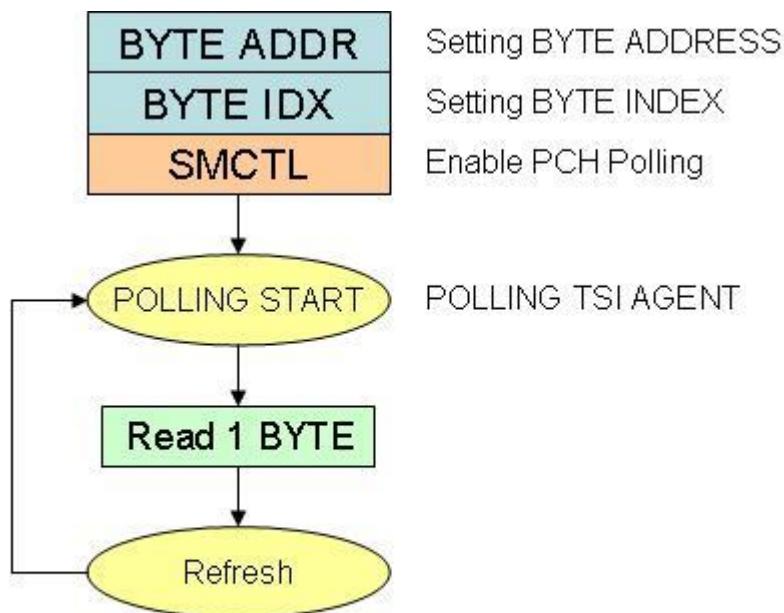


Figure 18-8 PCH Routine

18.4.6 Manual Mode interface

The SMBus host supports Block/Word/Byte Write and Block/Word/Byte read with PEC. The SMBus host can use the interface to access the smbus slave. The timing diagrams below illustrate how to use the smbus interface to write the data or read the data to the smbus slave.

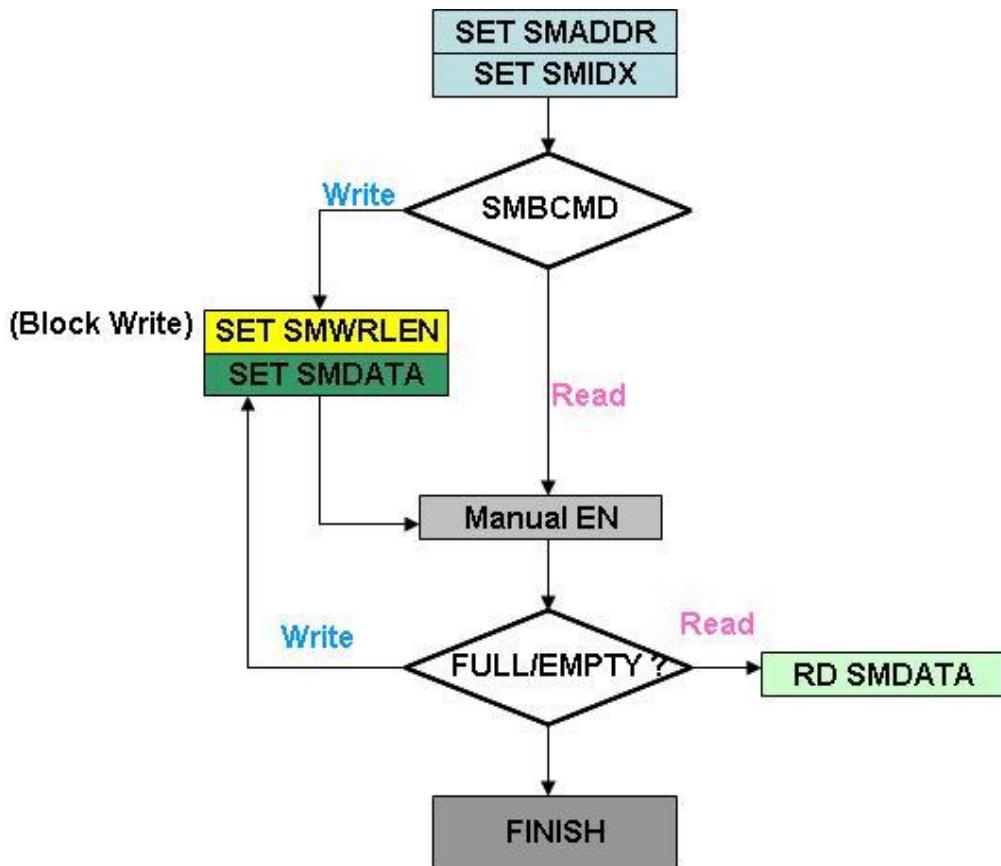


Figure 18-9 Manual Mode Programming Flow

18.5 Register Type Abbreviations

The following abbreviations are used to indicate the Register Type:

- ◆ R/W = Read/Write.
- ◆ R = Read from register.
- ◆ W = Write.
- ◆ RO = Read-only.

To program the SMBus master configuration registers, the following configuration procedures must be followed in sequence:

- (1). Enter the Extended Function Mode.
- (2). Configure the configuration registers.

18.5.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x26 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

18.5.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

18.6 SMBus Master Register Set

18.6.1 SMBus Register Map

SMBus Master base address in register Logic Device B CR62h(MSB), CR63h(LSB).

Table 18-2 SMBus Master Bank 0 Registers

Offset	Type	Name	Section
0	R/W	SMBus Data	19.7.2
1	R/W	SMBus Write Data Size	19.7.3
2	R/W	SMBus Command	19.7.4
3	R/W	SMBus Index	19.7.5
4	R/W	SMBus Control	19.7.6
5	R/W	SMBus Address	19.7.7
6	R/W	SMBCLK Frequency	19.7.8
7	RO	Reserved	--
8	R/W	PCH Address	19.7.9
9	R/W	Error status	19.7.10
A	R/W	Reserved	--
B	R/W	PCH Command	19.7.11
D	R/W	TSI Agent Enable	19.7.12
E	R/W	SMBus Control 3 Register	19.7.13
F	R/W	SMBus Control 3 Register	19.7.14
10	R/W	BYTE_ADDR	19.7.15
11	R/W	BYTE Index High Byte	19.7.16
12	R/W	BYTE Index Low Byte	19.7.17
13-15	R/W	Reserved	
16	R/W	TSI AGENT0 Address	19.7.19
17	R/W	TSI AGENT1 Address	19.7.20

18.6.2 SMBus Data (SMDATA) – Bank 0

This 32 bits register is the data in and out register of SMBus data register. Before writing to SMDATA register, this register contains the input data, after writing to SMDATA register, this register contains the output data.

Attribute: Read/Write

Offset: 0h

Power Well: VSB

Reset by: LRESET#

Byte	3	2	1	0
Name	SMFIFO3	SMFIFO2	SMFIFO1	SMFIFO0
Default	00h	00h	00h	00h

Byte	Description
3	SMFIFO3 (SMBus FIFO 3) . This byte represents the high byte of the 32 bits SMBus data.
2	SMFIFO2 (SMBus FIFO 2) . This byte represents the second byte of the 32 bits SMBus data.
1	SMFIFO1 (SMBus FIFO 1) . This byte represents the first byte of the 32 bits SMBus data.
0	SMFIFO0 (SMBus FIFO 0) . This byte represents the low byte of the 32 bits SMBus data.

18.6.3 SMBus Write Data Size (SMWRSIZE) – Bank 0

Attribute: Read/Write

Offset: 1h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	Reserved			SMWRSIZE				
Default	0	0	0	0	0	0	0	0

Byte	Description
7-5	Reserved
4-0	SMWRSIZE (SMBus Write Byte Counter) . This field sets the write byte counter, the max counter size is 32 bytes, and the minimal size is bytes.

18.6.4 SMBus Command (SMCMD) – Bank 0

Attribute: Read/Write

Offset: 2h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
NAME	REV					SMBus CMD		
Default	0	0	0	0	0	0	0	0

Byte	Description
7-4	Reserved
3-0	SMBCMD (SMBus Command). This field sets SMBus Command: 0000 : Read Byte (Default) 0001 : Read Word 0010 : Read Block 0011 : Block Write and Read Process Call 0100 : Process Call 1000 : Write Byte 1001 : Write Word 1010 : Write Block

18.6.5 SMBus INDEX (SMIDX) – Bank 0

Attribute: Read/Write

Offset: 3h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	SMCMD							
Default	0	0	0	0	0	0	0	0

Byte	Description
7-0	SMIDX (SMBus INDEX). This field represents the index data of the SMBus.

18.6.6 SMBus Control (SMCTL) – Bank 0

Attribute: Read/Write

Offset: 4h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	MMODE_S	S_RST	CRC8_EN	REFLASH_CLK			BYTE_EN	PCH_EN
Default	0	0	0	0	0	0	0	0

Byte	Description
7	MMODE_S (Manual Mode Set). 0: Disable. 1 : Enable.
6	S_RST (Soft Reset SMBus). 0: Disable. 1: Enable.
5	CRC8_EN (CRC8 Enable). 0: CRC8 function is disable. 1: CRC8 function is enable.
4-2	REFRASH_CLK (Refresh Clock Select). 000, 100 – 128ms 001, 101 – 256ms 010, 110 – 512ms 011, 111 – 64ms (1KHz)
1	BYTE_EN (BYTE Enable). 0: BYTE function is disable. 1: BYTE function is enable.
0	PCH_EN (PCH Enable). 0: PCH function is disable. 1 : PCH function is enable.

18.6.7 SMBus Address (SMADDR) – Bank 0

Attribute: Read/Write

Offset: 5h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	SMADDR							REV
Default	0	0	0	0	0	0	0	0

Byte	Description
7-1	SMADDR (SMBus Address). AMD-TSI only supports 7-bit SMBus address.
0	Reserved: 0 : Write. If the protocol is write, the WR_SIZE can't be zero. (Default)

18.6.8 SCL FREQ (SCLFREQ) – Bank 0

Attribute: Read/Write

Offset: 6h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	Reserved:				SCLFREQ			
Default	0	0	0	0	0	1	1	1

Byte	Description
7-4	Reserved
3-0	<p>SCLFQ (SMBCLK Frequency). This field defines the SMBCLK period (low time and high time). The clock low time and high time are defined as follows:</p> <p>0000 : 365KHz 0001 : 261KHz 0010 : 200KHz 0011 : 162KHz 0100 : 136KHz 0101 : 117KHz 0110 : 103KHz 0111 : 99KHz (Default) 1000 : 83KHz 1001 : 76KHz 1010 : 71KHz 1011 : 65KHz 1100 : 61KHz 1101 : 57KHz 1110 : 53KHz 1111 : 47KHz</p>

18.6.9 PCH Address (PCHADDR) – Bank 0

Attribute: Read/Write

Offset: 8h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	PCHADDR						REV	
Default	1	0	0	1	0	1	0	0

Byte	Description
7-1	PCHADDR (PCH Address). PCH supports 8-bit SMBus address. The default address is 94h. The last bit is read or write bit. It needs to set to "0".

18.6.10 SMBus Error Status (Error_status) – Bank 0

Attribute: Read/Write

Offset: 9h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	REV		ADNACK	Timeout	Reserved	BER	NACK	REV
Default	1	0	0	1	0	1	0	0

Byte	Description
7-6	Reserved
5	ADDR Non ACK. This bit reflects SMBus occurred ADDRESS NON ACK in Manual mode..
4	Timeout. This bit reflects when SMBus occurs timeout.
3	Reserved
2	BER (Bus Error). This bit reflects when a start or stop condition is detected during data transfer, or when an arbitration problem is detected.
1	NACK (Negative acknowledge). This bit is set by hardware when a transmission is not acknowledged on the ninth clock. While NACK is set SCL will be drive low and subsequent bus transactions are stalled until NACK is cleared.
0	Reserved

18.6.11 PCH Command (PCHCMD) – Bank 0

Attribute: Read/Write

Offset: Bh

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	PCHCMD							
Default	0	1	0	0	0	0	0	0

Byte	Description
7-0	PCHCMD (PCH Command). This field represents the command data of the PCH. The default command is block read (40h).

18.6.12 TSI Agent Enable Register (TSI_AGENT) – Bank

Attribute: Read/Write

Offset: Dh

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	Reserved						AG1	AG0
Default	0	0	0	0	0	0	0	0

Byte	Description
7-2	Reserved
1	TSI AGENT1 Enable. : This bit reflects AMD-TSI Agent elect. 0: Disable 1: Enable
0	TSI AGENT0 Enable. : This bit reflects AMD-TSI Agent elect. 0: Disable 1: Enable

18.6.13 SMBus Control 3 Register (SMCTL3) – Bank 0

Attribute: Read Only

Offset: Eh

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	Reserved				CRC_CHK	M_MODE	F_FULL	F_EMPT
Default	0	0	0	0	0	0	0	0

Byte	Description
7-4	Reserved
3	CRC_CHK (CRC Check). 0 : incorrect 1 : correct
2	M_MODE (Manual Mode). 0 : Non-active 1 : Active
1	F_FULL (fifo_full). : This bit reflects SMBus data fifo is full. 0 : Non-full 1 : Full

0	F_EMPT (fifo empty). : This bit reflects the SMBus data fifo is empty. 0 : Non-empty 1 : Empty
---	---

18.6.14 SMBus Control 2 Register (SMCTL2) – Bank 0

Attribute: Read/Write

Offset: Fh

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	Reserved		INT_LCH_E	Reserved		BYTE_SEL	BANKSEL	
Default	0	0	0	0	0	0	0	0

Byte	Description
7-6	Reserved
5	INT_LCH_E (Interrupt Latch Enable). : This bit will latch the I2CSTA register. 0 : Disable. 1 : Enable.
4-3	Reserved
2	BYTE_SEL :This field represents byte polling 8-bit/16bit select bits. 0: BYTE_TEMP is 16 bit data 1: BYTE_TEMP is 8 bit data
1-0	BANKSEL (Bank Select). 00 – Bank 0. 01 – Bank 1. 10 – Bank 2.

18.6.15 BYTE ADDRESS0 (BYTE ADDR) – Bank 0

Attribute: Read/Write

Offset: 10h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	BYTE_ADDRESS							
Default	0	0	0	0	0	0	0	0

Byte	Description
------	-------------

7-0	BYTE ADDRESS (BYTE ADDR). This field represents the address data of the BYTE.
-----	---

18.6.16 BYTE ADDRESS1 (BYTE ADDR) – Bank 0

Attribute: Read/Write

Offset: 11h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	BYTE_ADDRESS							
Default	0	0	0	0	0	0	0	0

Byte	Description
7-0	BYTE ADDRESS1 (BYTE ADDR). This field represents the address data of the BYTE.

18.6.17 BYTE INDEX0 (BYTE_IDX0) – Bank 0

Attribute: Read/Write

Offset: 12h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	BYTE_IDX_H							
Default	0	0	0	0	0	0	0	1

Byte	Description
7-0	BYTE_IDX_H (High BYTE INDEX). This field represents the high byte index of the Byte polling. The default command is byte read (01h).

18.6.18 BYTE INDEX1 (BYTE_IDX1) – Bank 0

Attribute: Read/Write

Offset: 13h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	BYTE_IDX_L							
Default	0	0	0	1	0	0	0	0

Byte	Description
7-0	BYTE_IDX_L (LOW BYTE INDEX). This field represents the low byte index of the Byte polling. The default command is byte read (10h).

18.6.19 TSI AGENT0 ADDRESS (TSI_AGENT0 ADDR) – Bank 0

Attribute: Read/Write

Offset: 16h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	TSI_AGNET0_ADDRESS							
Default	1	0	0	1	1	0	0	0

Byte	Description
7-1	TSI AGENT0 ADDRESS (TSI_AGENT0 ADDR). This field represents the address data of the BYTE.
0	Reserved

18.6.20 SI AGENT1 ADDRESS (TSI_AGENT1 ADDR) – Bank 0

Attribute: Read/Write

Offset: 17h

Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	TSI_AGNET1_ADDRESS							
Default	1	0	0	1	1	0	1	0

Byte	Description
7-1	TSI AGENT1 ADDRESS (TSI_AGENT1 ADDR). This field represents the address data of the BYTE.
0	Reserved

The EC may read thermal information from IBX using the SMBus block read command. The IBX doesn't support byte-read or word-read SMBus commands. The read use a different address than the writes. The address must be different so that the IBX knows which target is intended, either the I2C target or the block read buffer.

The IBX and EC are set up by BIOS with the length of the read that is supported by the platform. The EC must always do reads of the lengths set up by BIOS. There is no way to change the length of the read after BIOS has set things up.

An EC that only wants the single highest temperature among MCH, and CPU could read one byte. A 2 byte read would provide both IBX and CPU/MCH package temperature. An EC that wanted each components temperature would do a 4 byte read. An EC that also wanted DIMM information would read 9 bytes. If an EC wanted to read the HOST STS status, it must read 19 bytes. An EC can also read the energy data provided by the CPU by reading 12 bytes.

19. OVP & UVP DETECT

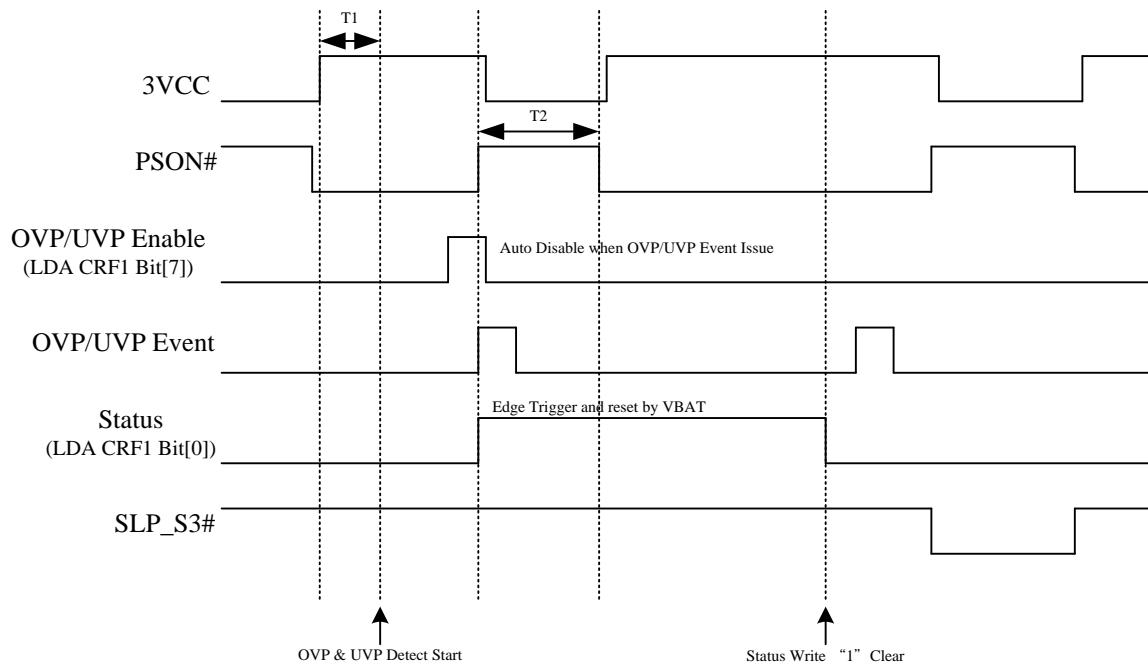


Figure 19-1 OVP & UVP Detect when SLP_S3# = 1

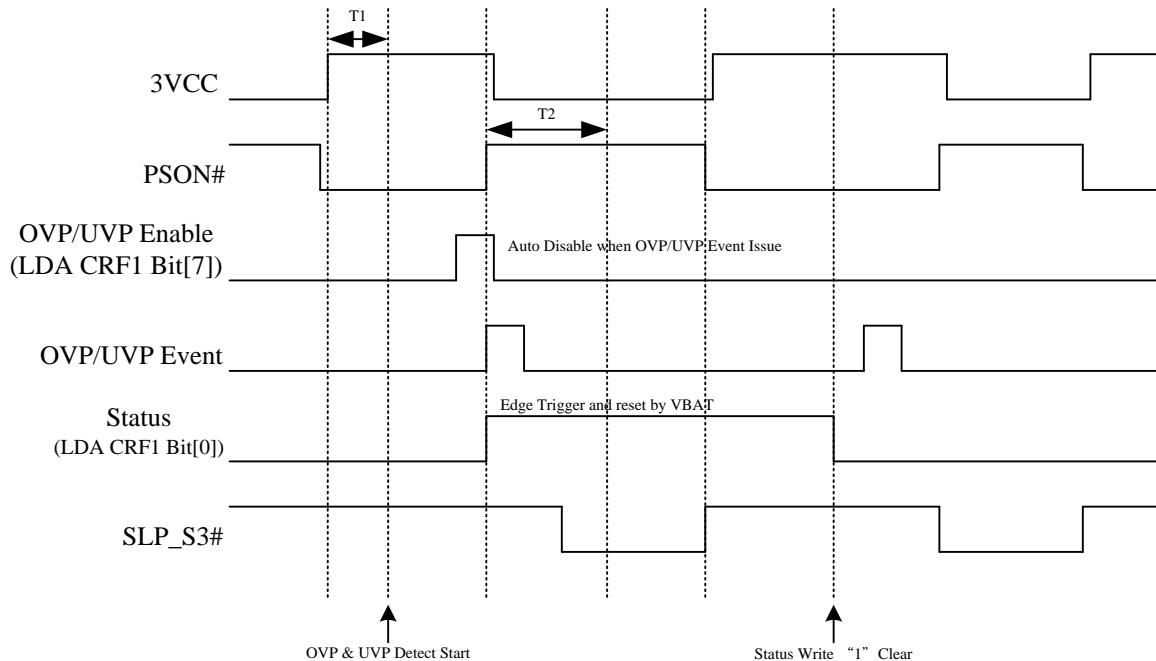


Figure 19-2 OVP & UVP Detect when SLP_S3# = 0

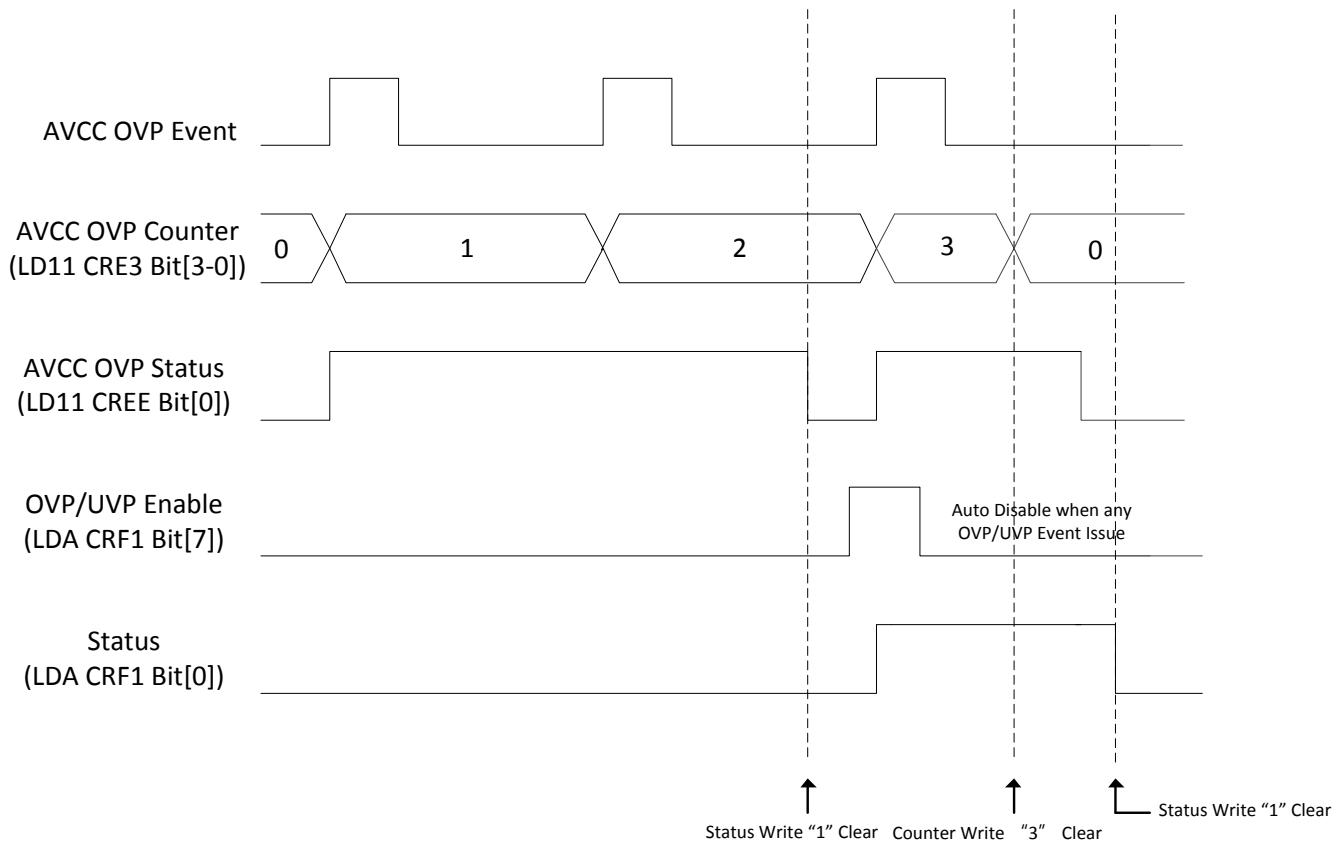


Figure 19-3 AVCC OVP Detect

Table 19-1 Timing Parameters of OVP/UVP

TIMING	PARAMETER
T1	3VCC to OVP/UVP Detect Start (See LDA CRF1 Bit6-5)
T2	PSON# inactive to SLP_S3# Detect (See LDA CRF1 Bit4-3)

20. PORT80 TO UART

The NCT5582D provides UART interface to transfer PORT80 information to other peripheral devices. Default baud rate is 115200Hz for universal UART protocol and it could be change by LD14 CRE2 and LD14 CRE3. When BIOS program PORT80 LED, in proportion to UART baud rate, it changes very frequently. Thus, some information might be lose. But we make sure the last one would be send.

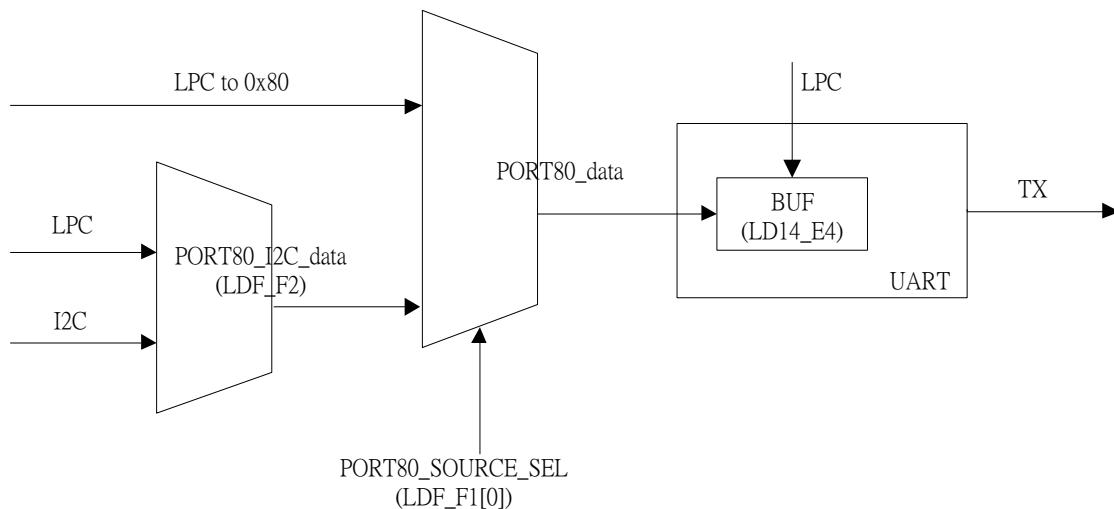


Figure 20-1 PORT80 to UART Block Diagram

After enter OS, we support other root to control PORT80 LED by write LDF CRF2 and LDF CRF1 to change other path. The UART could be control by other root, too. It is set by LD14 CRE4.

21. FADING LED

The NCT5582D provide Fading led interface that can be change led speed of bright or dark through different frequency or duty cycle. Furthermore, the contrast of led bright or dark can be decided by maximum duty cycle, minimum duty cycle, and middle value.

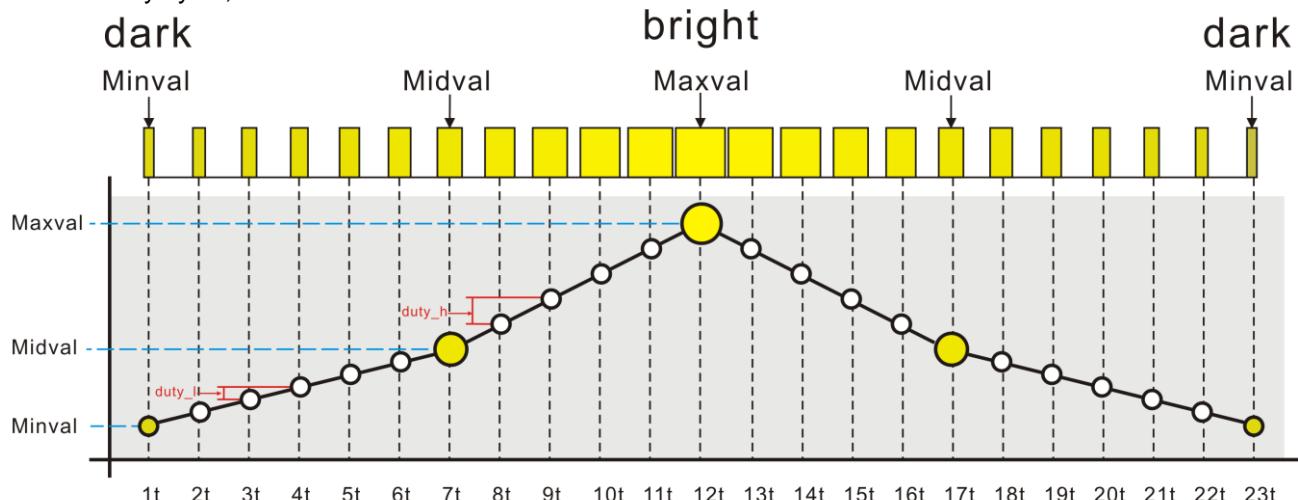


Figure 21-1 Example of Fading LED

NCT5582D GRN/YLW, MLED and FDLED1~4 supports fading led function. The duty cycle can be increase and decrease control by LD15 CRF3, CRF4, CRF9 and CRFA, as table 29-1. Besides LD15 CRF7 also supports dark extend control, as table 29-2.

Table 21-1 Duty cycle increase/decrease time

LD15 CRF3	LD15 CRF4	LD15 CRF9	LD15 CRFA	Increase Time	Decrease Time
0x0D	0x0E	0x03	0x03	0.61 sec	2.90 sec
0x08	0x08	0x08	0x08	1.06 sec	1.06 sec
0x06	0x05	0x06	0x05	1.57 sec	1.57 sec (default)
0x04	0x04	0x04	0x04	2.15 sec	2.15 sec

Table 21-2 Dark extend time

LD15 CRF7	Dark extend Time
0x0F	0.96 sec (default)
0x17	1.47 sec
0x1E	1.92 sec

22. OSCILLATOR FREE

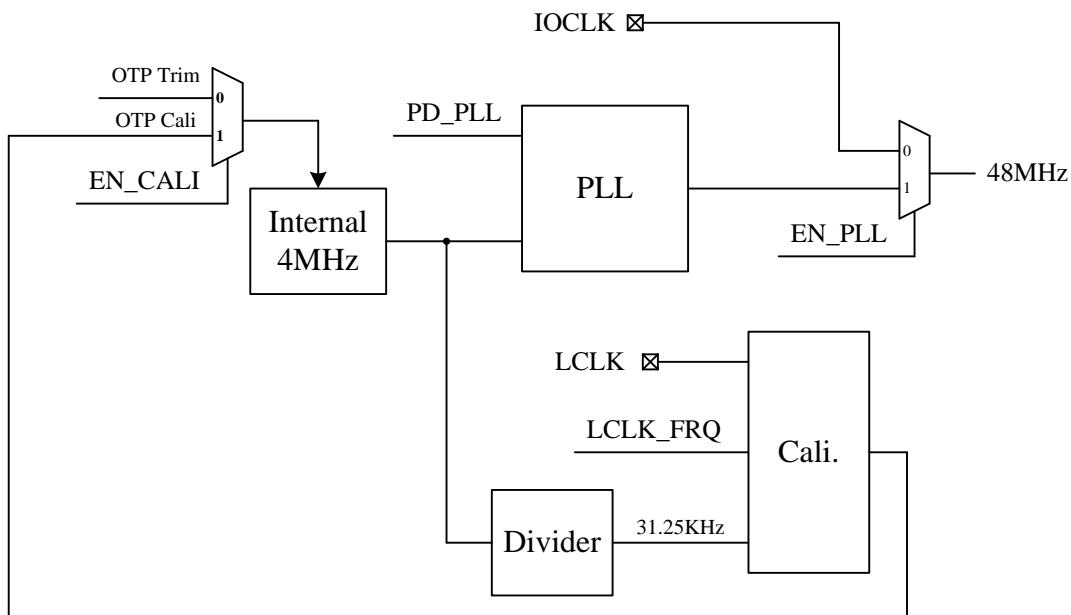


Figure 22-1 Oscillator free architecture

23. CONFIGURATION REGISTER

23.1 Chip (Global) Control Register

Default Value of Global Control Register:

Register	Default	Register	Default	Register	Default
CR 07h	00h	CR 20h	D4h (ID_H)	CR 2Bh	00h
CR 10h	FFh	CR 21h	21h (ID_L)	CR 2Ch	01h
CR 11h	FFh	CR 22h	FFh	CR 2Dh	0ss0_0000b
CR 13h	00h	CR 24h	04h	CR 2Fh	ssss_sss0b
CR 14h	00h	CR 25h	00h		
CR 1Ah	30h	CR 26h	0s00_0000b		
CR 1Bh	18h	CR 27h	03h		
CR 1Ch	00h	CR 28h	00h		
CR 1Dh	00h	CR 2Ah	C0h		

Note. The value of "s" means hardware strapping result: strapping high will report 1; strapping low will report 0.

In addition, BIOS can write the value of strapping result after hardware strapping.

Note. The CR21h is low-byte of the Chip-ID; the "X" means IC version. EX. 11=A version, 12=B version, 13=C version.

Reserved Registers of Global Control Register:

Register	Default	Register	Default
CR 02h	00h	CR 1Eh	FFh
CR 12h	FFh	CR 1Fh	FFh
CR 15h	FFh	CR 23h	00h
CR 16h	FFh	CR 29h	FFh
CR 17h	FFh	CR 2Eh	00h
CR 18h	FFh		
CR 19h	FFh		

Note. All reserved registers must keep default value.

Note. Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 07h. Logical Device Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	Reserved
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	Reserved
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	CIRWAKUP IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	WDT1 IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	WDT3 IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4-2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 30h

BIT	READ / WRITE	DESCRIPTION				
7-6	R / W	Pin41 function selection				
		LD12 CREB[Bit6]	CR1A [Bit7-6]	Pin41		
		1	x	CIRRX		
		0	00	RESETCONI#		
		0	01	GP30		
		0	10	OVT#_1		
		0	11	SMI#_1		
5	R / W	Pin37 function selection				
		CR1B [Bit2-0]	LD12 CRE0[Bit4]	CR1A [Bit5]	CR1C [bit2]	Pin37
		111	x	x	x	MSDA
		110	1	x	1	AUXFANOUT2
		110	0	0	x	SDA
		110	0	1	x	GP31
4-2	R / W	Pin36 function selection				
		CR1B [Bit0]	LD12 CRE0[Bit3]	CR1A [Bit4-2]	CR1C [bit7]	Pin36
		1	x	x	x	MSCL
		0	1	x	1	AUXFANIN2#
		0	0	010	x	SCL
		0	0	110	x	GP32
1	Reserved					
0	R / W	KBRST# output type selection 0: Push Pull 1: OD				

CR 1Bh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 10h

BIT	READ / WRITE	DESCRIPTION			
7	R / W	Pin22 function selection			
		CR27 [Bit6]	CR1B [Bit7]	Pin22	
		0	0	RESETCONO#	
		0	1	GP47	
		1	x	FDLED4	
6	R / W	Reserved			
5	R / W	Pin43 function Selection			
		DDR4_EN	CR1B [Bit5]	CR1C [bit7]	Pin43
		0	0	x	GP57
		1	0	x	VPP_EN
		x	1	1	AUXFANIN2
4	R / W	Pin46 function selection			
		DDR4_EN	CR1B [Bit4]	CR27 [Bit3]	Pin46
		1	x	x	VPP_PG
		0	1	x	CIRRX
		0	0	0	GP24
		0	0	1	IRRX1
3	R / W	Reserved			
2-1	R / W	Reserved			
0	R / W	Pin36 function selection			
		CR1B [Bit0]	LD12 CRE0[Bit3]	CR1A [Bit4-2]	CR1C [bit7]
		1	x	x	x
		0	1	x	1
		0	0	010	x
		0	0	110	x
Pin37 function selection					
		CR1B [Bit2-0]	LD12 CRE0[Bit4]	CR1A [Bit5]	CR1C [bit2]
		111	x	x	x
		110	1	x	1
		110	0	0	x
		110	0	1	x

CR 1Ch.

Attribute: Read/Write

Power Well: VSB

Reset by: PWROK

Default : 00h

BIT	READ / WRITE	DESCRIPTION			
7	R / W	Pin27 function selection			
		LD12 CREB [Bit5]	CR2A [Bit0]	CR1C [bit7]	Pin27
		0	0	x	KDAT
		0	1	1	GP20
		1	x	x	AUXFANIN2
		Pin36 function selection			
		CR1B [Bit0]	LD12 CRE0[Bit3]	CR1A [Bit4-2]	CR1C [bit7]
		1	x	x	x
		0	1	x	1
		0	0	010	x
		0	0	110	x
		Pin43 function Selection			
		DDR4_EN	CR1B [Bit5]	CR1C [bit7]	Pin43
		0	0	x	GP57
		1	0	x	VPP_EN
		x	1	1	AUXFANIN2
6	R / W	Reserved			
5	R / W	Reserved			
4-3	R / W	Pin2 function selection			
		LDD_CRE1[Bit1]	CR1C [Bit4-3]	Pin2	
		1	xx	CPUFANGPL	
		0	00	GP03	

BIT	READ / WRITE	DESCRIPTION			
2	R / W	Pin26 function selection			
		LD12 CREB [Bit4]	CR2A [Bit0]	CR1C [bit2]	Pin26
		0	0	x	KCLK
		0	1	x	GP21
		1	0	1	AUXFANOUT2
		1	1	x	CIRRX
		Pin37 function selection			
		CR1B [Bit2-0]	LD12 CRE0[Bit4]	CR1A [Bit5]	CR1C [bit2]
		111	x	x	x
		110	1	x	1
		110	0	0	SDA
		110	0	1	GP31
		Pin44 function Selection			
		DDR4_EN	CR2D [Bit7]	CR1C [bit2]	Pin44
		0	0	x	GP56
		1	0	x	VDDQ_EN
		x	1	1	AUXFANOUT2
1	R / W	Reserved			
0	R / W	Reserved			

CR 1Dh.

Attribute: Read/Write

Power Well: VSB

Reset by: PWROK(Bit7-5, 0), RSMRST#(Bit4-1)

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7	R / W	0: GPIOE# is inactive.	1: GPIOE# is active.
6	R / W	Issue GPIOE# to RESETCONO#. 0: Disable 1: Enable	
5	R / W	Issue GPIOE# to PWROK. 0: Disable 1: Enable	
4	R / W	0: Disable ANTISURGE event route to KBRST# 1: Enable ANTISURGE event route to KBRST#	
3-1	R / W	Reserved	
0	Reserved		

CR 20h. Chip ID (High Byte)

Attribute: Read Only

Power Well: VSB

Reset by: None

Default : D4h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = D4h (high byte).

CR 21h. Chip ID (Low Byte)

Attribute: Read Only

Power Well: VSB

Reset by: None

Default : 21h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 21h (low byte)

CR 22h. Device Power Down

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Reserved
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	Reserved
2-0	Reserved	

CR 24h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 04h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Select output type of AUXFANOUT2 =0 AUXFANOUT2 is Open-drain. =1 AUXFANOUT2 is Push-pull.
6	R / W	Reserved
5	R / W	Reserved
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. =1 SYSFANOUT is Push-pull.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Select output type of CPUFANOUT =0 CPUFANOUT is Open-drain. =1 CPUFANOUT is Push-pull.
2	R / W	Reserved
1	R / W	Select output type of AUXFANOUT3 =0 AUXFANOUT3 is Open-drain. =1 AUXFANOUT3 is Push-pull.
0	R / W	PNPCVS => = 0 The compatible PNP address-select registers have default values. = 1 The compatible PNP address-select registers have no default values.

CR 25h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	Reserved
3	R / W	Reserved
2	R / W	UARTATRI
1	R / W	Reserved
0	R / W	Reserved

CR 26h. s: value by strapping

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 0s00_0000b

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA#.
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4-3	Reserved	
2	R / W	Reserved

BIT	READ / WRITE	DESCRIPTION
1	R / W	<p>DSUALGRQ =></p> <p>= 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ.</p> <p>= 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.</p>
0	R / W	<p>DSUBLGRQ =></p> <p>= 0 Enable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ.</p> <p>= 1 Disable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.</p>

CR 27h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 03h

BIT	READ / WRITE	DESCRIPTION																				
7	R / W	<p>Pin40 function selection</p> <table border="1"> <tr> <td>CR27 [Bit7]</td> <td>LD12 CREB [Bit0]</td> <td>Pin40</td> </tr> <tr> <td>0</td> <td>0</td> <td>PWROK</td> </tr> <tr> <td>0</td> <td>1</td> <td>RESERVE</td> </tr> <tr> <td>1</td> <td>x</td> <td>FDLED1</td> </tr> </table>	CR27 [Bit7]	LD12 CREB [Bit0]	Pin40	0	0	PWROK	0	1	RESERVE	1	x	FDLED1								
CR27 [Bit7]	LD12 CREB [Bit0]	Pin40																				
0	0	PWROK																				
0	1	RESERVE																				
1	x	FDLED1																				
6	R / W	<p>Pin22 function selection</p> <table border="1"> <tr> <td>CR27 [Bit6]</td> <td>CR1B [Bit7]</td> <td>Pin22</td> </tr> <tr> <td>0</td> <td>0</td> <td>RESETCONO#</td> </tr> <tr> <td>0</td> <td>0</td> <td>RESERVE</td> </tr> <tr> <td>0</td> <td>1</td> <td>GP47</td> </tr> <tr> <td>1</td> <td>x</td> <td>FDLED4</td> </tr> </table>	CR27 [Bit6]	CR1B [Bit7]	Pin22	0	0	RESETCONO#	0	0	RESERVE	0	1	GP47	1	x	FDLED4					
CR27 [Bit6]	CR1B [Bit7]	Pin22																				
0	0	RESETCONO#																				
0	0	RESERVE																				
0	1	GP47																				
1	x	FDLED4																				
5		Reserved																				
4	R / W	Reserved																				
3	R / W	<p>Pin46 function selection</p> <table border="1"> <tr> <td>DDR4_EN</td> <td>CR1B [Bit4]</td> <td>CR27 [Bit3]</td> <td>Pin46</td> </tr> <tr> <td>1</td> <td>x</td> <td>x</td> <td>VPP_PG</td> </tr> <tr> <td>0</td> <td>1</td> <td>x</td> <td>CIRRX</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>GP24</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>IRRX1</td> </tr> </table>	DDR4_EN	CR1B [Bit4]	CR27 [Bit3]	Pin46	1	x	x	VPP_PG	0	1	x	CIRRX	0	0	0	GP24	0	0	1	IRRX1
DDR4_EN	CR1B [Bit4]	CR27 [Bit3]	Pin46																			
1	x	x	VPP_PG																			
0	1	x	CIRRX																			
0	0	0	GP24																			
0	0	1	IRRX1																			
2	R / W	Reserved																				
1-0		Reserved																				

CR 28h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	HM IO space lock enable 0 : Disable 1 : Enable
3	Reserved	
2-0	R / W	PRTMODS2 ~ 0 => Bits 2 1 0 = 0 x x Parallel Port Mode. = 1 x x Reserved

CR 2Ah.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#, GP2X_MRST(Bit1-0)

Default : C0h

BIT	READ / WRITE	DESCRIPTION
-----	--------------	-------------

BIT	READ / WRITE	DESCRIPTION																																										
7	R / W	<p>Pin14 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin14</td></tr> <tr><td>0</td><td>CTSA#</td></tr> <tr><td>1</td><td>GP80</td></tr> </table> <p>Pin15 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin15</td></tr> <tr><td>0</td><td>DSRA#</td></tr> <tr><td>1</td><td>GP81</td></tr> </table> <p>Pin16 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin16</td></tr> <tr><td>0</td><td>RTSA#</td></tr> <tr><td>1</td><td>GP82</td></tr> </table> <p>Pin17 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin17</td></tr> <tr><td>0</td><td>DTRA#</td></tr> <tr><td>1</td><td>GP83</td></tr> </table> <p>Pin18 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin18</td></tr> <tr><td>0</td><td>SINA</td></tr> <tr><td>1</td><td>GP84</td></tr> </table> <p>Pin19 function selection</p> <table border="1"> <tr><td>UARTA_P80_EN</td><td>CR2A [Bit7]</td><td>Pin19</td></tr> <tr><td>1</td><td>x</td><td>SOUTA_P80</td></tr> <tr><td>0</td><td>0</td><td>SOUTA</td></tr> <tr><td>0</td><td>1</td><td>GP85</td></tr> </table>	CR2A [Bit7]	Pin14	0	CTSA#	1	GP80	CR2A [Bit7]	Pin15	0	DSRA#	1	GP81	CR2A [Bit7]	Pin16	0	RTSA#	1	GP82	CR2A [Bit7]	Pin17	0	DTRA#	1	GP83	CR2A [Bit7]	Pin18	0	SINA	1	GP84	UARTA_P80_EN	CR2A [Bit7]	Pin19	1	x	SOUTA_P80	0	0	SOUTA	0	1	GP85
CR2A [Bit7]	Pin14																																											
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CR2A [Bit7]	Pin18																																											
0	SINA																																											
1	GP84																																											
UARTA_P80_EN	CR2A [Bit7]	Pin19																																										
1	x	SOUTA_P80																																										
0	0	SOUTA																																										
0	1	GP85																																										
7	R / W	<p>Pin20 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin20</td></tr> <tr><td>0</td><td>DCDA#</td></tr> <tr><td>1</td><td>GP86</td></tr> </table> <p>Pin21 function selection</p> <table border="1"> <tr><td>CR2A [Bit7]</td><td>Pin21</td></tr> <tr><td>0</td><td>RIA#</td></tr> <tr><td>1</td><td>GP87</td></tr> </table>	CR2A [Bit7]	Pin20	0	DCDA#	1	GP86	CR2A [Bit7]	Pin21	0	RIA#	1	GP87																														
CR2A [Bit7]	Pin20																																											
0	DCDA#																																											
1	GP86																																											
CR2A [Bit7]	Pin21																																											
0	RIA#																																											
1	GP87																																											
6	R / W	Reserved																																										
5	R / W	Reserved																																										
4	R / W	Reserved																																										
3	R / W	Reserved																																										

BIT	READ / WRITE	DESCRIPTION																																					
2	R/W	Enable Over Temperature shutdown Protection (OVT#) = 0 The thermal shutdown function is disabled. (Default) = 1 Enable thermal shutdown function. (If set this bit to 1, the relative registers of OVT# event are: Bank0, CR18 ,Bit6 → SMIOVT1 OVT# (Default SYSTIN) Bank0, CR4C ,Bit4 → SMIOVT3 OVT# Bank0, CR4C ,Bit3 → SMIOVT2 OVT# (Default CPUTIN) If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately.)																																					
1	R / W	Pin24 function selection <table border="1"> <tr> <td>LD12 CREB [Bit2]</td> <td>CR2A [Bit1]</td> <td>Pin24</td> </tr> <tr> <td>0</td> <td>0</td> <td>MCLK</td> </tr> <tr> <td>0</td> <td>1</td> <td>GP23</td> </tr> <tr> <td>1</td> <td>x</td> <td>AUXFANOUT3</td> </tr> </table> Pin25 function selection <table border="1"> <tr> <td>LD12 CREB [Bit3]</td> <td>CR2A [Bit1]</td> <td>Pin25</td> </tr> <tr> <td>0</td> <td>0</td> <td>MDAT</td> </tr> <tr> <td>0</td> <td>1</td> <td>GP22</td> </tr> <tr> <td>1</td> <td>x</td> <td>AUXFANIN3</td> </tr> </table>			LD12 CREB [Bit2]	CR2A [Bit1]	Pin24	0	0	MCLK	0	1	GP23	1	x	AUXFANOUT3	LD12 CREB [Bit3]	CR2A [Bit1]	Pin25	0	0	MDAT	0	1	GP22	1	x	AUXFANIN3											
LD12 CREB [Bit2]	CR2A [Bit1]	Pin24																																					
0	0	MCLK																																					
0	1	GP23																																					
1	x	AUXFANOUT3																																					
LD12 CREB [Bit3]	CR2A [Bit1]	Pin25																																					
0	0	MDAT																																					
0	1	GP22																																					
1	x	AUXFANIN3																																					
0	Pin26 function selection <table border="1"> <tr> <td>LD12 CREB [Bit4]</td> <td>CR2A [Bit0]</td> <td>CR1C [bit2]</td> <td>Pin26</td> </tr> <tr> <td>0</td> <td>0</td> <td>x</td> <td>KCLK</td> </tr> <tr> <td>0</td> <td>1</td> <td>x</td> <td>GP21</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>AUXFANOUT2</td> </tr> <tr> <td>1</td> <td>1</td> <td>x</td> <td>CIRRX</td> </tr> </table> Pin27 function selection <table border="1"> <tr> <td>LD12 CREB [Bit5]</td> <td>CR2A [Bit0]</td> <td>CR1C [bit7]</td> <td>Pin27</td> </tr> <tr> <td>0</td> <td>0</td> <td>x</td> <td>KDAT</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>GP20</td> </tr> <tr> <td>1</td> <td>x</td> <td>x</td> <td>AUXFANIN2</td> </tr> </table>			LD12 CREB [Bit4]	CR2A [Bit0]	CR1C [bit2]	Pin26	0	0	x	KCLK	0	1	x	GP21	1	0	1	AUXFANOUT2	1	1	x	CIRRX	LD12 CREB [Bit5]	CR2A [Bit0]	CR1C [bit7]	Pin27	0	0	x	KDAT	0	1	1	GP20	1	x	x	AUXFANIN2
LD12 CREB [Bit4]	CR2A [Bit0]	CR1C [bit2]	Pin26																																				
0	0	x	KCLK																																				
0	1	x	GP21																																				
1	0	1	AUXFANOUT2																																				
1	1	x	CIRRX																																				
LD12 CREB [Bit5]	CR2A [Bit0]	CR1C [bit7]	Pin27																																				
0	0	x	KDAT																																				
0	1	1	GP20																																				
1	x	x	AUXFANIN2																																				

CR 2Bh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION	

BIT	READ / WRITE	DESCRIPTION			
7-6	R / W	Pin38 function selection			
		CR2B [Bit7-6]	Pin38		
		00	RSTOUT2#		
		01	GP76		
		10	MLED		
		11	GPIOE#		
5-4	R / W	Pin39 function selection			
		CR2B [Bit5-4]	Pin39		
		00	RSTOUT1#		
		01	GP75		
		10	Tri-state		
		11	Reserved		
3	R / W	Reserved			
2	R / W	Reserved			
1-0	R / W	Pin33 function selection			
		UARTB_P80_EN	LDD CRE1[Bit1]	CR2B [Bit1-0]	Pin33
		0	0	00	GP71
		0	1	00	CPUFANGPP
		1	x	00	SOUTB_P80
		x	x	01	GP71
		x	x	11	Tri-state

CR 2Ch.

Attribute: Read/Write

Power Well: VSB, VRTC(Bit0)

Reset by: RSMRST#, Battery reset(Bit0)

Default : 01h

BIT	READ / WRITE	DESCRIPTION										
7	Reserved.											
6-5	R / W	Pin35 function selection <table border="1"><tr><td>CR2C [Bit6-5]</td><td>Pin35</td></tr><tr><td>00</td><td>3VSBSW#</td></tr><tr><td>01</td><td>GP33</td></tr><tr><td>10</td><td>Tri-state</td></tr><tr><td>11</td><td>3VSBSW#</td></tr></table>	CR2C [Bit6-5]	Pin35	00	3VSBSW#	01	GP33	10	Tri-state	11	3VSBSW#
CR2C [Bit6-5]	Pin35											
00	3VSBSW#											
01	GP33											
10	Tri-state											
11	3VSBSW#											
4-3	R / W	Reserved										
2	R / W	Reserved										
1	R / W	Reserved										
0	R / W	Pin60 function selection <table border="1"><tr><td>CR2C [Bit0]</td><td>Pin60</td></tr><tr><td>0</td><td>PECI</td></tr><tr><td>1</td><td>Reserved</td></tr></table>	CR2C [Bit0]	Pin60	0	PECI	1	Reserved				
CR2C [Bit0]	Pin60											
0	PECI											
1	Reserved											

CR 2Dh.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#(Bit6), RSMRST#(Bit7, Bit5, Bit0)

Default : 0ss0_0000b

BIT	READ / WRITE	DESCRIPTION			
7	R / W	Pin44 function Selection			
		DDR4_EN	CR2D [Bit7]	CR1C [bit2]	Pin44
		0	0	x	GP56
		1	0	x	VDDQ_EN
		x	1	1	AUXFANOUT2
6	R / W	Reserved			
5	R / W	ESPI_EN Strapping result reading			
4-0	Reserved				
0	R / W	Reserved			

CR 2Fh. Strapping Function Result

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit5-2), LRESET#(Bit7-6), PWROK(Bit1)

Default : ssss_sss0b

BIT	READ / WRITE	DESCRIPTION		
7	R / W	Reserved		
6	R / W	Reserved		
5	R / W	Reserved		
4	R / W	DDR4_EN Strapping result reading		
3	R / W	Reserved		
2	R / W	Reserved		
1	R / W	Reserved		
0	Reserved			

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

- 4) VSB Strapping result can be programming by LPC, and reset by RSMRST#
- 5) VCC Strapping result can be programming by LPC, and reset by PWROK
- 6) LRESET Strapping (2E_4E_SEL) : No change

23.2 Logical Device 2

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The UARTA logical device is inactive. 1: The UARTA logical device is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 03h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5-2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1-0	R / W	<p>Bits 1 0</p> <p>0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: UART A clock source is 14.769 MHz (24 MHz / 1.625).</p>

CR F2h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	<p>UARTA_RS485_enable</p> <p>0: Disable RS485 auto flow control function for UARTA 1: Enable RS485 auto flow control function for UARTA</p>
6	R / W	<p>UARTA_RS485_inv_sel (Available only when CRF2_Bit7=1)</p> <p>0: Do not invert the behavior of RTSA# pin for RS485 auto flow control. 1: Invert the behavior of RTSA# pin for RS485 auto flow control.</p>
5-0	Reserved	

23.3 Logical Device 3

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The UARTB logical device is inactive. 1: The UARTB logical device is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 02h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 03h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for IR.

CR F0h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5-2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1-0	R / W	<p>Bits 1 0</p> <p>0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: IR clock source is 2 MHz (24 MHz / 12). 1 0: IR clock source is 24 MHz (24 MHz / 1). 1 1: IR clock source is 14.769 MHz (24 MHz / 1.625).</p>

CR F1h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Reserved 1: Through IRRX / IRTX.
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 µS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

CR F2h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTB_RS485_enable 0: Disable RS485 auto flow control function for UARTB 1: Enable RS485 auto flow control function for UARTB
6	R / W	UARTB_RS485_inv_sel (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSB# pin for RS485 auto flow control. 1: Invert the behavior of RTSB# pin for RS485 auto flow control.
5-0	Reserved	

23.4 Logical Device 5

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The KBC logical device is inactive. 1: The KBC logical device is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 43h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection Bits 7 6 0 0: Reserved 0 1: 8MHz 1 0: Reserved 1 1: Reserved
5-3	Reserved	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

23.5 Logical Device 6

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for CIR.

23.6 Logical Device 7

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-3	Reserved		
2	R / W	0: GPIO8 is inactive.	1: GPIO8 is active.
1	R / W	0: GPIO7 is inactive.	1: GPIO7 is active.
0	R / W	Reserved	

CR E0h. GPIO7 I/O Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP7X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION	
7-0	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.	

CR E1h. GPIO7 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP7X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-0	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.	
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.	

CR E2h. GPIO7 Inversion Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP7X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-0	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)	

CR E3h. GPIO7 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP7X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO7 Event Status Bit 7-0 corresponds to GP77-GP70, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E4h. GPIO8 I/O Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP8X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 I/O register 0: The respective GPIO8 PIN is programmed as an output port 1: The respective GPIO8 PIN is programmed as an input port.

CR E5h. GPIO8 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO8 Inversion Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO8 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO8 Event Status Bit 7-0 corresponds to GP87-GP80, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR Ech. GPIO7 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP7X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	0: GPIO76 1: GPIO76 → MLED (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO75 1: GPIO75 → BEEP (Please also set this GPIO to “output” type.)
4	R / W	Reserved
3	R / W	Reserved
2	R / W	Reserved
1	R / W	0: GPIO71 1: GPIO71 → BEEP (Please also set this GPIO to “output” type.)
0	R / W	Reserved

CR Edh. GPIO8 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO87 1: GPIO87 → YLW
6	R / W	0: GPIO86 1: GPIO86 → BEEP

BIT	READ / WRITE	DESCRIPTION
5	R / W	0: GPIO85 1: GPIO85 → SMI
4	R / W	0: GPIO84 1: GPIO84 → GRN
3	R / W	0: GPIO83 1: GPIO83 → YLW
2	R / W	0: GPIO82 1: GPIO82 → BEEP
1	R / W	0: GPIO81 1: GPIO81 → YLW
0	R / W	0: GPIO80 1: GPIO80 → WDT1

23.7 Logical Device 8

CR 30h.

Attribute: Read/Write

Power Well: VSB, VSB

Reset by: LRESET#, RSMRST# (Bit7)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6-5	Reserved	
4	R / W	0: WDT3 is inactive. 1: WDT3 is active.
3	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
2	Reserved	
1	R / W	0: GPIO0 is inactive. 1: GPIO0 is active.
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR E0h. GPIO0 I/O Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP0X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP0X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP0X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP0X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP07-GP00, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E4h. GPIO0 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP0X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	Reserved

BIT	READ / WRITE	DESCRIPTION
5	R / W	Reserved
4	R / W	Reserved
3	R / W	0: GPIO03 1: GPIO03 → MLED (Please also set this GPIO to “output” type.)
2	R / W	Reserved
1	R / W	Reserved
0	R / W	Reserved

CR F5h. Watchdog Timer 1 (WDT1) and KBC P20 Control Mode Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CRE7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W Write “1” Only	Disable / Enable RESETCONO# One Shooting bit. This bit is self-clearing. 0: Disable 1: Enable
4	R / W	Watchdog Timer 1 count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer 1 count mode. 0: Second Mode. 1: Minute Mode.
2	Reversed	
1	R / W	Disable / Enable the Watchdog Timer 1 output low pulse to the KBRST# pin 0: Disable. 1: Enable.
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F6h. Watchdog Timer 1 (WDT1) Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CRE7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. The accuracy of watchdog timer 1 about one cycle deviation. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF5, bit[3], by analogy.

CR F7h. Watchdog Timer 1 (WDT1) Control & Status Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CRE7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer 1 is not affected by mouse interrupt. 1: Watchdog Timer 1 is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer 1 is not affected by keyboard interrupt. 1: Watchdog Timer 1 is reset by keyboard interrupt.
5	Write "1" Only	Trigger Watchdog Timer 1 event. This bit is self-clearing.
4	R / W Write "0" Clear	Watchdog Timer 1 status bit 0: Watchdog Timer 1 is running. 1: Watchdog Timer 1 issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer 1

CR F8h. Watchdog Timer 3 (WDT3) Control Mode Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CREE[2])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	

BIT	READ / WRITE	DESCRIPTION
4	R / W	Watchdog Timer 3 count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer 3 count mode. 0: Second Mode. 1: Minute Mode.
2-1	Reserved	
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F9h. Watchdog Timer 3 (WDT3) Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CREE[2])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watchdog Timer 3 Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watchdog Counter and start counting down. The accuracy of watchdog timer 3 about one cycle deviation. Reading this register returns the current value in the Watchdog Counter, not the Watchdog Timer 3 Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF8, bit[3], by analogy.

CR Fah. Watchdog Timer 3 (WDT3) Control & Status Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CREE[2])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W Write "1" Only	Trigger Watchdog Timer 3 event. This bit is self-clearing.
4	R / W Write "0" Clear	Watchdog Timer 3 status bit 0: Watchdog Timer 3 is running. 1: Watchdog Timer 3 issues time-out event.
3-0	R / W	These bits select the IRQ resource for Watchdog Timer 3

CR Feh. Watchdog Timer 1 (WDT1) Timeout Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W Write “1” Clear	Watchdog Timer 1 Timeout Counter.

CR FFh. Watchdog Timer 3 (WDT3) Timeout Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W Write “1” Clear	Watchdog Timer 3 Timeout Counter.

23.8 Logical Device 9

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-4	Reserved		
3	R / W	0: GPIO5 is inactive.	1: GPIO5 is active
2	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
1	R / W	0: GPIO3 is inactive.	1: GPIO3 is active.
0	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.

CR E0h. GPIO2 I/O Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP2X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION	
7-0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.	

CR E1h. GPIO2 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP2X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-0	R / W	GPIO2 Data register For output ports, the respective bits can be read and written by the pins.	
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.	

CR E2h. GPIO2 Inversion Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP2X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. GPIO2 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP2X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E4h. GPIO3 I/O Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP3X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR E5h. GPIO3 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP3X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 Data register For output ports, the respective bits can be read and written by the pins.

BIT	READ / WRITE	DESCRIPTION
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E6h. GPIO3 Inversion Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP3X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E7h. GPIO3 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP3X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	Read Only Read-Clear	GPIO3 Event Status Bit 6-0 corresponds to GP36-GP30, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E9h. GPIO2 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP2X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	Reserved
5	R / W	Reserved
4	R / W	0: GPIO24 1: GPIO24 → MLED (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
3	R / W	0: GPIO23 1: GPIO23 → GRN (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO22 1: GPIO22 → YLW (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO21 1: GPIO21 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO20 1: GPIO20 → WDT1 (Please also set this GPIO to “output” type.)

CR Eah. GPIO3 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP3X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	Reserved
5	R / W	Reserved
4	R / W	Reserved
3	R / W	0: GPIO33 1: GPIO33 → WDT1 (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO32 1: GPIO32 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO31 1: GPIO31 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO30 1: GPIO30 → WDT1 (Please also set this GPIO to “output” type.)

CR Ebh. GPIO5 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP5X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO56 1: GPIO56 → GRN (Please also set this GPIO to “output” type.)
5	R / W	Reserved
4	R / W	Reserved
3	R / W	Reserved
2	R / W	Reserved
1	R / W	Reserved
0	R / W	Reserved

CR F0h. GPIO4 I/O Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP4X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F1h. GPIO4 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP4X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F2h. GPIO4 Inversion Register

Attribute: Read/Write

Power Well: VSB
 Reset by: GP4X_MRST
 Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E8h. GPIO4 Status Register

Attribute: Read Only
 Power Well: VSB
 Reset by: GP4X_MRST
 Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR Eeh. GPIO4 Multi-function Select Register

Attribute: Read/Write
 Power Well: VSB
 Reset by: GP4X_MRST
 Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → BEEP (Please also set this GPIO to “output” type.)
6	R / W	Reserved
5	R / W	Reserved
4	R / W	Reserved
3	R / W	Reserved
2	R / W	Reserved
1	R / W	Reserved
0	R / W	Reserved

CR F4h. GPIO5 I/O Register

Attribute: Read/Write
 Power Well: VSB

Reset by: GP5X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

CR F5h. GPIO5 Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP5X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F6h. GPIO5 Inversion Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP5X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F7h. GPIO5 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP5X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

23.9 Logical Device A

CR E0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

BIT	READ / WRITE	DESCRIPTION																												
7	R / W	DIS_PSIN => Disable the panel switch input to turn on the system power supply. 0: PSIN is wire-AND and connected to PSOUT#. 1: PSIN is blocked and cannot affect PSOUT#.																												
6	R / W	Enable KBC wake-up 0: Disable keyboard wake-up function via PSOUT#. 1: Enable keyboard wake-up function via PSOUT#.																												
5	R / W	Enable Mouse wake-up 0: Disable mouse wake-up function via PSOUT#. 1: Enable mouse wake-up function via PSOUT#.																												
4	R / W	MSRKEY => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details. <table border="1"> <thead> <tr> <th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr> </thead> <tbody> <tr> <td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr> <tr> <td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr> </tbody> </table>	ENMDAT_UP	MSRKEY	MSXKEY	Wake-up event	1	x	1	Any button clicked or any movement.	1	x	0	One click of left or right button.	0	0	1	One click of the left button.	0	1	1	One click of the right button.	0	0	0	Two clicks of the left button.	0	1	0	Two clicks of the right button.
ENMDAT_UP	MSRKEY	MSXKEY	Wake-up event																											
1	x	1	Any button clicked or any movement.																											
1	x	0	One click of left or right button.																											
0	0	1	One click of the left button.																											
0	1	1	One click of the right button.																											
0	0	0	Two clicks of the left button.																											
0	1	0	Two clicks of the right button.																											
3	R / W	Enable CIR wake-up 0: Disable CIR wake-up function via PSOUT#. 1: Enable CIR wake-up function via PSOUT#.																												
2	R / W	Keyboard / Mouse swap enable 0: Normal mode. 1: Keyboard / Mouse ports are swapped.																												
1	R / W	MSXKEY => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.																												
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.																												

CR E1h. KBC Wake-Up Index Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Attribute: Read Only

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset, PWROK(Bit4), LRESET#(Bit3-2)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	<p>Power-loss control ^{Note} (These two bits will determine the system turn on or off after AC resume, from G3 to S5 state.)</p> <p>Bits 6 5</p> <p>0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before the power loss. Please check the definition of the pre-state is “ON” or “OFF” in chapter 26.2.) 1 1: User defined mode for power loss last-state. (The last-state flag is located on “CRE6h, bit4.”)</p>
4	R / W	3VSBSW# enable bit 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for wake-up events set in CRE0. This bit is cleared when any wake-up event is captured. (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1-0	Reserved	

Note. Whether “Always turn on”, “Pre-state” or “User defined mode”, the PSON#’s active condition for system to turn-on is S3# goes high. For south-bridge which S3# default is low while AC resume, please refer “CRE7h, bit4” to achieve the power-loss control application.

CR E5h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	GP8X_MRST 0: GP8X reset by RSMRST#. (Default) 1: GP8X reset by SLPS5.
4	R / W	GP7X_MRST 0: GP7X reset by RSMRST#. (Default) 1: GP7X reset by SLPS5.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Reserved
2	R / W	RESETCONO# signal to control PWROK 0: Disable (Default) 1: Enable
1	R / W	Route to PWROK source selection. 0: PSON#. 1: SLP_S3#. (Default)
0	R / W	ATXPGD signal to control PWROK 0: Enable. (Default) 1: Disable.

CR E6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7, Bit5, Bit3-1), Battery reset(Bit6, Bit4)

Default : 1Ah

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Read Only	SKTOCC# Status. This bit is '1' when SKTOCC# = 1.
5	R / W	CASEOPEN0 Clear Control. Write 1 to this bit to clear CASEOPEN0 status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF. (Default)
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK Bits 3 2 1 0 0 0: 50mS 0 0 1: 100mS 0 1 0: 150mS 0 1 1: 200mS 1 0 0: 250mS 1 0 1: 300mS (Default) 1 1 0: 500mS 1 1 1: 700mS
0	Reserved	

CR E7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7-5, Bit3), Battery reset(Bit4, Bit1-0)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	<p>ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.</p>
6	R / W	<p>ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.</p>
5	R / W	<p>ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.</p>
4	R / W	<p>EN_ONPSOUT (VBAT) Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (For southbridge which S3# default is low when AC resume, like VIA ...etc.) 0: Disable. (Default) 1: Enable.</p>
3	R / W	<p>Select Watchdog Timer 1 Reset Source 0: Watchdog timer 1 is reset by LRESET#. 1: Watchdog timer 1 is reset by PWROK.</p>
2	Reserved	
1	R / W	<p>SKTOCC# Clear Control. Write 1 to this bit to clear SKTOCC# status. This bit will clear the status itself.</p>
0	R / W	<p>Hardware Monitor RESET source select 0: PWROK or internal PWROK (LDA CRED[3]). 1: LRESET#.</p>

CR E9h. GPIOs Reset Source Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	GP5X_MRST 0: GP5X reset by RSMRST#. 1: GP5X reset by SLPS5.
4	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLPS5.
3	R / W	GP3X_MRST 0: GP3X reset by RSMRST#. 1: GP3X reset by SLPS5.
2	R / W	GP2X_MRST 0: GP2X reset by RSMRST#. 1: GP2X reset by SLPS5.
1	R / W	Reserved
0	R / W	GP0X_MRST 0: GP0X reset by LRESET#. 1: GP0X reset by PWROK.

CR Ech. ACPI Control and Status Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R	PSIN real time Status
6-5	R / W	Select PSOUT Delay time from GPO (GP73) to PSOUT. 00: 1ms 01: 2ms 10: 3ms 11: 4ms
4	R / W	Enable PSOUT Delay function from GPO (GP73) to PSOUT. 0: Disable. 1: Enable.
3	R / W	Auto clear PSOUT# to disconnect to PSIN# function select 0: Disable. Clear by RSMRST 1: Enable. Clear by PSIN rising and RSMRST

BIT	READ / WRITE	DESCRIPTION
2	R / W1C	Block PSIN# event, when PSOUT blocking time and push PSIN. (write "1" clear, and clear by PWROK) 0: No PSIN# event. 1: Have PSINT# event.
1	R / W	Enable to disconnect PSIN to PSOUT 0: Disable , PSOUT will bypass PSIN. 1: Enable.
0	R / W1C	PSIN# 4 sec status when PSIN is low and SLPS3 is high. (write "1" clear) 0: No 4 sec power down event. 1: 4 sec power down event

CR Edh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	PSIN# blocking time register from S5 to S0. 1bit for 0.5sec.. Min: 0.5sec Max: 8sec
3	R / W	Hardware monitor reset source select. 0: internal PWROK (no delay). 1: PWROK.
2-1	Reserved	
0	R / W	RSMRST reset source select. 0: VSB and PSOUT/PCHVSB 1: VSB and PSOUT/PCHVSB and Deep_S5_Ctrl

CR Eeh.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RESCON Reset source selection. 0: LRESET_L 1: PWROK
6	R / W	RIA Wakeup Enable 0: Disable 1: Enable
5	R / W	RIB Wakeup Enable 0: Disable 1: Enable

BIT	READ / WRITE	DESCRIPTION
4-3	Reserved	
2	R / W	Watchdog Timer 3 Reset Source Selection 0: LRESET_L 1: PWROK
1	R / W	CASEOPEN polarity 0: None inverse CASEOPEN0/1 INPUT 1: Inverse CASEOPEN0/1 INPUT
0	R / W	Reserved

CR F0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 10h

BIT	READ / WRITE	DESCRIPTION												
		Pin34 function selection												
7-5	R / W	<table border="1"> <tr> <td>LDA CRF0 [Bit7-5]</td> <td>Pin34</td> </tr> <tr> <td>000</td> <td>DEEP_S5_0</td> </tr> <tr> <td>001</td> <td>3VSBSW</td> </tr> <tr> <td>010</td> <td>Tri-state</td> </tr> <tr> <td>011</td> <td>ATXPGDO</td> </tr> <tr> <td>1xx</td> <td>PWROK</td> </tr> </table>	LDA CRF0 [Bit7-5]	Pin34	000	DEEP_S5_0	001	3VSBSW	010	Tri-state	011	ATXPGDO	1xx	PWROK
LDA CRF0 [Bit7-5]	Pin34													
000	DEEP_S5_0													
001	3VSBSW													
010	Tri-state													
011	ATXPGDO													
1xx	PWROK													
4	R / W	Reserved												
3	Reserved													
2	R / W	Reserved												
1	R / W	PSIN de-bounce 0: 62.4ms 1: 206ms												
0	R / W	Keyboard Auto-Swap Detect Enable. 0: Disable 1: Enable												

CR F1h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 48h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ASUSTEK OVP/UVP Enable

BIT	READ / WRITE	DESCRIPTION
6-5	R / W	TIME_PWRD (Power Fault and ANTISURGE function) 00: 3us ~ 4us(LDA CRFC[2]=0), 20ms ~35ms(LDA CRFC[2]=1) 01: 1.5s ~ 2s 10: 93.75ms ~ 125ms (Default) 11: 187.5ms ~ 250ms
4-3	R / W	TIME_ANTIDETS3 00: 0.5s ~ 0.625s 01: 1s ~ 1.25s(Default) 10: 2s ~ 2.5s 11: 4s ~ 5s
2-1	Reserved	
0	R / W	ASUSTEK OVP/UVP Status

CR F2h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 5Eh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#. (Default)
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#. (Default)
2	R / W	Reserved
1	R / W	Enable S3# Debounce function. 0: Disable Debounce. 1: Enable Debounce.
0	R / W	Reserved

CR F3h.

Attribute: Read/Write

Power Well: VSB

Reset by: WDT_L_RST(bit6), RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W Write "1" Clear	Watchdog Timer 4 status. When this bit is set to 1, it means timeout event occurs.
5	R / W-Clear	Reserved
4	R / W-Clear	Reserved
3	R / W-Clear	Reserved
2	Reserved	
1	R / W-Clear	Reserved
0	R / W-Clear	Reserved

CR F4h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	Reserved
6	R / W-Clear	Reserved
5	R / W-Clear	Reserved
4	R / W-Clear	Reserved
3	R / W-Clear	Reserved
2	R / W-Clear	Reserved
1	R / W-Clear	Reserved
0	R / W-Clear	Reserved

CR F5h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	Virtual 8048 Enable bit. This bit is used for KBC emulation without PS/2 keyboard and PS/2 mouse. When set "1" to auto response KBC command.
2-0	Reserved	

CR F6h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#(Bit7), RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.
6	Reserved	
5	R / W	Reserved
4	R / W	Reserved
3	R / W	Reserved
2	Reserved	
1	R / W	Reserved
0	R / W	Reserved

CR F7h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : C0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RSTOUT2# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
6	R / W	RSTOUT1# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
5	R / W	PSIN_BLK_EN. When S5->S0 or S0->S5, SIO will filter PSIN# a specific time. 0: Disable 1: Enable
4	R / W	Reserved
3	R / W	Reserved
2	R / W	Reserved
1	R / W	Reserved
0	R / W	Reserved

CR FC8.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 80h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	TIME_PWRD (Power Fault and ANTISURGE function) 00: 3us ~ 4us(LDA CRFC[2]=0), 20ms ~35ms(LDA CRFC[2]=1) 01: 1.5s ~ 2s 10: 93.75ms ~ 125ms (Default) 11: 187.5ms ~ 250ms
1-0	Reserved	

CR Feh. GP31 and GP32 Event Route Selection Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved

BIT	READ / WRITE	DESCRIPTION
6	R / W	Reserved
5	R / W	0: Disable GP31 event route to PSOUT#. 1: Enable GP31 event route to PSOUT#.
4	R / W	0: Disable GP32 event route to PSOUT#. 1: Enable GP32 event route to PSOUT#.
3	R / W	Reserved
2	R / W	Reserved
1	R / W	0: Disable GP31 event route to PME#. 1: Enable GP31 event route to PME#.
0	R / W	0: Disable GP32 event route to PME#. 1: Enable GP32 event route to PME#.

23.10 Logical Device B

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: Hardware Monitor & SB-TSI device is inactive. 1: Hardware Monitor & SB-TSI device is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 62h, 63h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the SB-TSI base address <100h : FFEh> along a two-byte boundary.

CR 64h, 65h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the read-only HM base address <100h : FFEh> along a two-byte boundary.

CR 70h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E4h. AUXFAN2 Duty Cycle Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN2 Duty Cycle Register

CR E5h. ANTISURGE Voltage Channel Configuration Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : A8h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	3VCC high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%
5-4	R / W	VIN0 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%
3-2	R / W	VIN1 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%
1	R / W	ANTISURGE Voltage Channel selection 0: VIN0 and VIN1 1: VIN2 and VIN3
0	Reserved	

CR E6h. Configuration Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit7, Bit4-0), WDT1&PWROK(Bit6)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	CR2A Bit1-0 reset source selection 0: WDT1 & PWROK 1: RSMRST#

BIT	READ / WRITE	DESCRIPTION
6	R / W	RESETCONI# and PSIN# input block 0: Enable 1: Disable
5	Reserved	
4	R / W	Block OVP/UVP detect signal by S5#. 0: Disable 1: Enable
3	R / W	Reserved
2	R / W	Reserved
1	R / W	Reserved
0	R / W	Block OVP/UVP detect signal by VCC or S3#. 0: VCC and S3# 1: VCC

CR E7h. AUXFAN3 Duty Cycle Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN3 Duty Cycle Register

CR Edh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 81h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	THERMTRIP Active Flag (write 1 clear) 0: No THERMTRIP event. 1: THERMTRIP Active event
3	R / W	THERMTRIP Deep S5 Enable 0: Disable. When THERMTRIP active at S0 state, system will go into S5 state. 1: Enable. When THERMTRIP active at S0 state, system will go into DeepS5 state.
2:0	Reserved	

CR F0h. FANIN De-bouncer Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit7), LRESET#(Bit6-1)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	1: Enable AUXFANIN3 input de-bouncer. 0: Disable AUXFANIN3 input de-bouncer.
5	R / W	1: Enable AUXFANIN2 input de-bouncer. 0: Disable AUXFANIN2 input de-bouncer.
4	R / W	Reserved
3	R / W	Reserved
2	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
1	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
0	Reserved	

CR F5h. SMBus de-bouncer Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 10h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable debug port. 1: Enable debug port.
6-5	Reserved	
4	R / W	1: Enable Antisurge input de-bouncer. 0: Disable Antisurge input de-bouncer.
3	R / W	1: Enable SDA0 input de-bouncer. 0: Disable SDA0 input de-bouncer.
2	R / W	1: Enable SCL0 input de-bouncer. 0: Disable SCL0 input de-bouncer.
1	R / W	1: Enable SCL input de-bouncer 160ns. 0: Disable SCL input de-bouncer.
0	R / W	1: Enable SDA input de-bouncer 160ns. 0: Disable SDA input de-bouncer.

CR F6h. Deep S5 Front Panel Green & Yellow LED control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Deep S5_YLW_BLK_FREQ bits (This function affects by LDB CRF9 Bit 5) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. 1XXX: Fading LED.
3-0	R / W	Deep S5_GRN_BLK_FREQ bits (This function affects by LDB CRF9 Bit 4) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. 1XXX: Fading LED.

CR F7h. Front Panel Green LED (GRN_LED) control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 87h

BIT	READ / WRITE	DESCRIPTION
7	R / W	AUTO_EN (Powered by VBAT , default = 1) 0: GRN_LED and YLW_LED are controlled by GRN_LED_RST or SLP_S3# and SLP_S5#. 1: GRN_LED is controlled by SLP_S3# and YLW_LED is controlled by SLP_S3# and SLP_S5#.
6	R / W	GRN_LED_RST# (Default= 0) 0: GRN_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: GRN_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	GRN_LED_POL 0: GRN_LED output is the same. (Default) 1: GRN_LED output is inverted.
4	Reserved	

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	GRN_BLK_FREQ bits (The reset depends on bit6, GRN_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. (Default) 1XXX: Fading LED.

CR F8h. Front Panel Yellow LED (YLW_LED) control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 47h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	YLW_LED_RST# (Default =1) 0: YLW_BLK_FREQ will be set to "0000" (High-Z) when into S3~S5 state. 1: YLW_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	YLW_LED_POL 0: YLW_LED output is the same. (Default) 1: YLW_LED output is inverted.
4	Reserved	
3-0	R / W	YLW_BLK_FREQ bits (The reset depends on bit6, YLW_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. (Default) 1XXX: Fading LED.

CR F9h. Deep Sleep LED Eanble register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Deep S5_YLW_BLK_FREQ : 0: Depend on setting of CRF6h, bit7~4. 1: Always output high.
4	R / W	Deep S5_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3~0. 1: Always output high.
3	Reserved	
2-0	R / W	RSMRST# V1/V2 adjust register 000: normal V1/V2 001: -3% ~ -6% of normal 011: -6% ~ -9% of normal 111: -9% ~ -12% of normal

CR Fah.RESETCONO# and PWROK active Pulse width selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-2	R / W	RESETCONO# and PWROK active Pulse width selection 00:50ms ~ 60ms 01:100ms ~ 130ms 10:200ms ~ 260ms 11:200ms ~ 260ms
1-0	Reserved	

CR FBh.GPIOE# status

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIOE# status. Write 1 to clear this status.
6-0	Reserved	

23.11 Logical Device D

CR E1h.

Attribute: Read/Write

Power Well: VSB

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

Default : 00h

BIT	READ / WRITE	DESCRIPTION																																
7	Reserved																																	
6	R / W	Reserved																																
5	R / W	Reserved																																
4	R / W	Reserved																																
3	R / W	Reserved																																
2	R / W	Reserved																																
1	R / W	Pin2 function selection <table border="1"> <tr> <td>LDD CRE1[Bit1]</td> <td>CR1C [Bit4-3]</td> <td>Pin2</td> </tr> <tr> <td>1</td> <td>xx</td> <td>CPUFANGPL</td> </tr> <tr> <td>0</td> <td>00</td> <td>GP03</td> </tr> </table>			LDD CRE1[Bit1]	CR1C [Bit4-3]	Pin2	1	xx	CPUFANGPL	0	00	GP03																					
LDD CRE1[Bit1]	CR1C [Bit4-3]	Pin2																																
1	xx	CPUFANGPL																																
0	00	GP03																																
Pin33 function selection <table border="1"> <tr> <td>UARTB_P80_EN</td> <td>LDD CRE1[Bit1]</td> <td>CR2B [Bit1-0]</td> <td>Pin33</td> </tr> <tr> <td>0</td> <td>0</td> <td>00</td> <td>GP71</td> </tr> <tr> <td>0</td> <td>1</td> <td>00</td> <td>CPUFANGPP</td> </tr> <tr> <td>1</td> <td>x</td> <td>00</td> <td>SOUTB_P80</td> </tr> <tr> <td>1</td> <td>x</td> <td>00</td> <td>SOUTB_P80</td> </tr> <tr> <td>x</td> <td>x</td> <td>01</td> <td>GP71</td> </tr> <tr> <td>x</td> <td>x</td> <td>10</td> <td>SOUTB_P80</td> </tr> <tr> <td>x</td> <td>x</td> <td>11</td> <td>Tri-state</td> </tr> </table>			UARTB_P80_EN	LDD CRE1[Bit1]	CR2B [Bit1-0]	Pin33	0	0	00	GP71	0	1	00	CPUFANGPP	1	x	00	SOUTB_P80	1	x	00	SOUTB_P80	x	x	01	GP71	x	x	10	SOUTB_P80	x	x	11	Tri-state
UARTB_P80_EN	LDD CRE1[Bit1]	CR2B [Bit1-0]	Pin33																															
0	0	00	GP71																															
0	1	00	CPUFANGPP																															
1	x	00	SOUTB_P80																															
1	x	00	SOUTB_P80																															
x	x	01	GP71																															
x	x	10	SOUTB_P80																															
x	x	11	Tri-state																															
Reserved																																		

CR E2h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 01h

BIT	READ / WRITE	DESCRIPTION	
7-2	Reserved		
1-0	R / W	Reserved	

CR E7h.

Attribute: Read/Write
 Power Well: VSB
 Reset by: RSMRST#
 Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	RSTOUT0# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
3-0	Reserved	

CR F0h. Watchdog Timer Mask Register

Attribute: Read/Write
 Power Well: VSB
 Reset by: RSMRST#
 Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mask Watchdog Timer 1 to affect PWROK, then enter Deep_S5 0: Mask enable. (WDT1 not affect PWROK) 1: Mask disable. (WDT1 default affect PWROK)
6	R / W	Mask Watchdog Timer 1 to affect RESETCONO# 0: Mask enable. (WDT1 not affect RESETCONO#) 1: Mask disable. (WDT1 default affect RESETCONO#)
5	R / W	DIS WAKEUP ESPI ESPI virtual wire WAKE# is controlled by SIO glue logic 0: Disable. 1: Enable.
4	R / W	Mask Watchdog Timer 3 to affect PWROK 0: Mask enable. (WDT3 not affect PWROK) 1: Mask disable. (WDT3 default affect PWROK)
3	R / W	Mask Watchdog Timer 3 to affect RESETCONO# 0: Mask enable. (WDT3 not affect RESETCONO#) 1: Mask disable. (WDT3 default affect RESETCONO#)
2-1	Reserved	
0	R / W	Mask Watchdog Timer 1 to affect RSMRST# 0: Mask enable. (WDT1 not affect RSMRST #) 1: Mask disable. (WDT1 default affect RSMRST#)

CR F3h.

Attribute: Read/Write
 Power Well: VSB
 Reset by: RSMRST#
 Default : 00h

BIT	READ / WRITE	DESCRIPTION
7~1	Reversed	
0	R	KBC Auto-Swap Detect Status. 0: Keyboard 1: Mouse

23.12 Logical Device E

CR 30h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: CIR Wake-up is inactive. 1: CIR Wake-up Interface is active.

CR 60h, 61h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Wake-up Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for CIR Wake-up.

CR F0h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	OOB Destination Slave Address.

CR F1h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 1Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	OOB Source Slave Address.

CR F4h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	Read OOB Temperature Enable.
0	Reserved	

CR F6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 17h

BIT	READ / WRITE	DESCRIPTION
7-3	R / W	OOB Power-ON Configuration [Bit7-3]
2	R / W	Core OOB Channel Enable. This Bit reflect in OOB Channel is ready. 0: Not Ready 1: Ready
1	R / W	Core Virtual Wire Channel Enable. This Bit reflect in Virtual Wire Channel is ready. 0: Not Ready 1: Ready
0	R / W	Core Peripheral Channel Enable. This Bit reflect in Peripheral Channel is ready. 0: Not Ready 1: Ready

CR F7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 0Bh

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	OOB Power-ON Configuration [Bit15-13]

BIT	READ / WRITE	DESCRIPTION
4-2	R / W	MAXFREQ (Maximum Frequency Supported) 000: 20MHz 001: 25MHz 010: 33MHz(Default) 011: 50MHz Others: Reserved
1-0	R / W	IO Mode Support. This field is reflected in IO Mode Support field of the Gerneral Purpose Capabilities Configurations register. 00: Single IO 01: Single and Dual IO 10: Single and Quad IO 11: Single, Dual and Quad IO

CR F8h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	OOB Power-ON Configuration [Bit23-16]

CR F9h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 07h

BIT	READ / WRITE	DESCRIPTION
7-3	R / W	OOB Power-ON Configuration [Bit31-27]
2	R / W	OOB Channel Support Control Bit. 0: OOB Channel is not support 1: OOB Channel is support
1	R / W	Virtual Wire Channel Support Control Bit. 0: Virtual Wire Channel is not support 1: Virtual Wire Channel is support
0	R / W	Peripheral Channel Support Control Bit. 0: Peripheral Channel is not support 1: Peripheral Channel is support

CR Fah.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	ESPI S5/S4 SEL If LDE CRFA [Bit0] = 1 0: Pin84 will drive SLP_S5# by espi internal signal 1: Pin84 will drive SLP_S4# by espi internal signal If LDE CRFA [Bit0] = 0 This bit will be don't care.
1	R / W	Reserved
0	R / W	Reserved

23.13 Logical Device F

CR E1h.

Attribute: Read/Write

Power Well: VSB

Reset by: GP2X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP2 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E2h.

Attribute: Read/Write

Power Well: VSB

Reset by: GP3X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GP3 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E3h.

Attribute: Read/Write

Power Well: VSB

Reset by: GP4X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP4 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E4h.

Attribute: Read/Write

Power Well: VSB

Reset by: GP5X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP5 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E6h.

Attribute: Read/Write

Power Well: VSB

Reset by: GP7X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP7 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E7h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP8 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E9h.

Attribute: Read/Write

Power Well: VSB

Reset by: GP0X_MRST#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR F0h. I2C Control & Address Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 9Dh

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable I2C_Slave
6-0	R / W	I2C Address

CR F1h. I2C to 80PORT Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#, SLP_S5#(Bit2),

Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	80PORT Display 0: Enable 1: Disable
0	R / W	LPC or I2C to 80PORT switch

CR F2h. I2C to 80PORT Data Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

23.14 Logical Device 11

CR E0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 08h

BIT	READ / WRITE	DESCRIPTION						
7-3	Reserved							
4	R / W	0: Disable PSOUT# monitor for RMARST# 1: Enable PSOUT# monitor for RSMRST#						
3	Reserved							
2	R / W	PSIN_4S_EN 0: Disable. When PSIN# low over 4 sec, system will go into S5 state 1: Enable. When PSIN# low over 3.8 sec, system will go into DeepS5 state						
1	R / W	0: There is no relationship between SKTOCC# and PSON# 1: SKTOCC# related to PSON#						
0	R / W	Pin48 function selection <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>LD11_CRE0 [Bit0]</td> <td>Pin48</td> </tr> <tr> <td>0</td> <td>THERMTRIP#_IN</td> </tr> <tr> <td>1</td> <td>CASEOPEN0#</td> </tr> </table>	LD11_CRE0 [Bit0]	Pin48	0	THERMTRIP#_IN	1	CASEOPEN0#
LD11_CRE0 [Bit0]	Pin48							
0	THERMTRIP#_IN							
1	CASEOPEN0#							

CR E1h. GPIO, RI PSOUT Wake-Up Status Register

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	Reserved
6	R / W-Clear	Reserved
5	R / W-Clear	PSOUT status of the GP31 event. Write 1 to clear this status.
4	R / W-Clear	PSOUT status of the GP32 event. Write 1 to clear this status.
3	R / W-Clear	PSOUT status of the RIA event. Write 1 to clear this status.
2	R / W-Clear	Reserved
1-0	Reserved.	

CR E2h. GPIO, RI PSOUT Wake-Up Control Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	GPIO and RI PSOUT Wake-Up Group Select. 0: GPIO 1: GPIO+RI
0	R / W	GPIO and RI PSOUT Wake-Up Mode Select 0: Sleep 1: Sleep+Deep

CR E3h. AVCC UVP, OVP Counter Register

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W-Clear	AVCC UVP Counter Register. Write 1 to clear this Counter Register.
3-0	R / W-Clear	AVCC OVP Counter Register Write 1 to clear this Counter Register.

CR E4h. VIN0 UVP, OVP Counter Register

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W-Clear	VIN0 UVP Counter Register. Write 1 to clear Counter Register.
3-0	R / W-Clear	VIN0 OVP Counter Register. Write 1 to clear Counter Register.

CR E5h. VIN1 UVP, OVP Counter Register

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W-Clear	VIN1 UVP Counter Register. Write 1 to clear this Counter Register.
3-0	R / W-Clear	VIN0 OVP Counter Register. Write 1 to clear this Counter Register.

CR E6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
2	R / W	ASUSTEK PSON Selct. 0: Disable 1: Enable
1	Reserved	
0	Reserved	

CR Eeh. AVCC, VIN0, VIN1 Status Register

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W-Clear	VIN1 status of the UV event. Write 1 to clear this status.
4	R / W-Clear	VIN1 status of the OV event. Write 1 to clear this status.
3	R / W-Clear	VIN0 status of the UV event. Write 1 to clear this status.
2	R / W-Clear	VIN0 status of the OV event. Write 1 to clear this status.
1	R / W-Clear	AVCC status of the UV event. Write 1 to clear this status.

BIT	READ / WRITE	DESCRIPTION
0	R / W-Clear	AVCC status of the OV event. Write 1 to clear this status.

23.15 Logical Device 12

CR E0h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION				
7	R / W	Reserved				
6	R / W	Reserved				
5	R / W	Reserved				
4	R / W	Pin37 function selection				
		CR1B [Bit2-0]	LD12 CRE0[Bit4]	CR1A [Bit5]	CR1C [bit2]	Pin37
		111	x	x	x	MSDA
		110	1	X	1	AUXFANOUT2
		110	0	0	x	SDA
		110	0	1	x	GP31
3	R / W	Pin36 function selection				
		CR1B [Bit0]	LD12 CRE0[Bit3]	CR1A [Bit4-2]	CR1C [bit7]	Pin36
		1	x	x	x	MSCL
		0	1	x	1	AUXFANIN2
		0	0	010	x	SCL
		0	0	110	x	GP32
2-1	R / W	DDR4SEL2 When S0 → S5 state, the delay timer of SLP_S5# to VDDQ_EN. 00: 0ms 01: 50ms 10: 100ms 11: 200ms				
0	R / W	DDR4SEL1 When S0 → S5 state, the delay timer of VDDQ_EN to VPP_EN. 0: 64ms 1: 32ms				

CR E1h. SW Error Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	

BIT	READ / WRITE	DESCRIPTION
3	R / W	Pre-video graphics error control bit. 0: Without error 1: Error
2	R / W	ROM fault control bit. 0: Without error 1: Error
1	R / W	System powers on but is unable to boot error control bit. 0: Without error 1: Error
0	R / W	Pre-video memory error control bit. 0: Without error 1: Error

CR E4h. MLED & FDLED1 Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	FDLED1 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led
3-0	R / W	MLED Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

CR E5h. FDLED2 & FDLED3 Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	FDLED3 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led
3-0	R / W	FDLED2 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

CR E6h. FDLED4 Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	FDLED4 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

CR E7h. KBC Short Detection Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	KBC Short Detection Enable. 0: Disable KBC Short Detection. 1: Enable KBC Short Detection.

CR Eah. PORT80 Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#, LRESET#(Bit3)

Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	Extend PSON time When system power off (S0->S3/S5), PSON# can keep high for a certain time to avoid power on signal coming immediately. 00: 0 sec 01: 2 sec 10: 3 sec 11: 4 sec

CR Ebh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION																		
7	Reserved																			
6	R / W	Pin41 function selection <table border="1"> <tr> <td>LD12 CREB[Bit6]</td> <td>CR1A [Bit7-6]</td> <td>Pin41</td> </tr> <tr> <td>1</td> <td>x</td> <td>CIRRX</td> </tr> <tr> <td>0</td> <td>00</td> <td>RESETCONI#</td> </tr> <tr> <td>0</td> <td>01</td> <td>GP30</td> </tr> <tr> <td>0</td> <td>10</td> <td>OVT#_1</td> </tr> <tr> <td>0</td> <td>11</td> <td>SMI#_1</td> </tr> </table>	LD12 CREB[Bit6]	CR1A [Bit7-6]	Pin41	1	x	CIRRX	0	00	RESETCONI#	0	01	GP30	0	10	OVT#_1	0	11	SMI#_1
LD12 CREB[Bit6]	CR1A [Bit7-6]	Pin41																		
1	x	CIRRX																		
0	00	RESETCONI#																		
0	01	GP30																		
0	10	OVT#_1																		
0	11	SMI#_1																		
5	R / W	Pin27 function selection <table border="1"> <tr> <td>LD12 CREB [Bit5]</td> <td>CR2A [Bit0]</td> <td>CR1C [bit7]</td> <td>Pin27</td> </tr> <tr> <td>0</td> <td>0</td> <td>x</td> <td>KDAT</td> </tr> <tr> <td>0</td> <td>1</td> <td>x</td> <td>GP20</td> </tr> <tr> <td>1</td> <td>x</td> <td>1</td> <td>AUXFANIN2</td> </tr> </table>	LD12 CREB [Bit5]	CR2A [Bit0]	CR1C [bit7]	Pin27	0	0	x	KDAT	0	1	x	GP20	1	x	1	AUXFANIN2		
LD12 CREB [Bit5]	CR2A [Bit0]	CR1C [bit7]	Pin27																	
0	0	x	KDAT																	
0	1	x	GP20																	
1	x	1	AUXFANIN2																	

BIT	READ / WRITE	DESCRIPTION			
4	R / W	Pin26 function selection			
		LD12 CREB [Bit4]	CR2A [Bit0]	CR1C [bit2]	Pin26
		0	0	x	KCLK
		0	1	x	GP21
		1	0	1	AUXFANOUT2
3	R / W	Pin25 function selection			
		LD12 CREB [Bit3]	CR2A [Bit1]	Pin25	
		0	0	MDAT	
		0	1	GP22	
2	R / W	Pin24 function selection			
		LD12 CREB [Bit2]	CR2A [Bit1]	Pin24	
		0	0	MCLK	
		0	1	GP23	
1	Reserved				
0	R / W	Pin40 function selection			
		CR27 [Bit7]	LD12 CREB [Bit0]	Pin40	
		0	0	PWROK	
		0	1	RESERVE	
		1	x	FDLED1	

CR Ech.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#, LRESET#(Bit7-6)

Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-3	Reserved		
2	R / W	Reserved	
1-0	R / W	Reserved	

CR Edh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
-----	--------------	-------------

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Reserved
4	R / W	Reserved
3	R / W	Reserved
2	R / W	Reserved
1	R / W	Reserved
0	R / W	Reserved

CR Efh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 40h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	RSMRST# inactive Timing 00: 90~130 ms 01: 190~230 ms 10: 290~330 ms 11: 390~430 ms
5-4	R / W	Reserved
3-0	Reserved	

23.16 Logical Device 14

CR E0h. PORT80 UART Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length election) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved	

CR E1h. PORT80 UART Status Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

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CR F0h. Fading Led Maximun Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : FFh

BIT	READ / WRITE	DESCRIPTION																					
7-0	R / W	<p>Fading_led_maxval This byte reference Led frequency select, CRF5 bit[1] and fading led enable, CRF5 bit[0], Led frequency select bit has higher priority, the combination of Led frequency select and fading led enable describe below. When solid led mode, this byte is duty cycle control register, and frequency control by CRF8.</p> <p>Led frequency before divider select = 1 and fading led enable = 1 is fading led The maximum duty cycle value.</p> <p>Led frequency before divider select = 0 or fading led enable = 0 is solid led</p> <table> <thead> <tr> <th>maxval</th> <th>ratio</th> <th>Duty cycle</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>1/255</td> <td>= 0.3%</td> </tr> <tr> <td>0x02</td> <td>2/255</td> <td>= 0.7%</td> </tr> <tr> <td></td> <td>...</td> <td></td> </tr> <tr> <td>0x40</td> <td>64/255</td> <td>= 25.1%</td> </tr> <tr> <td></td> <td>...</td> <td></td> </tr> <tr> <td>0xFF</td> <td>255/255</td> <td>= 100%</td> </tr> </tbody> </table>	maxval	ratio	Duty cycle	0x01	1/255	= 0.3%	0x02	2/255	= 0.7%		...		0x40	64/255	= 25.1%		...		0xFF	255/255	= 100%
maxval	ratio	Duty cycle																					
0x01	1/255	= 0.3%																					
0x02	2/255	= 0.7%																					
	...																						
0x40	64/255	= 25.1%																					
	...																						
0xFF	255/255	= 100%																					

CR F1h. Fading Led Middle Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	<p>Fading_led_midval This byte is the turning point duty cycle value between minimum and maximum duty cycle value.</p>

CR F2h. Fading Led Minimun Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	<p>Fading_led_minval This byte is the minimum duty cycle value.</p>

CR F3h. Fading Led Increase Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 06h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_duty_inc_l The increased duty cycle value between the minimum duty cycle value and turning point.

CR F4h. Fading Led Increase Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 05h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_duty_inc_h The increased duty cycle value between the turning point and the maximum duty cycle value.

CR F5h. Fading Led Control Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 17h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_led_prgval Repeat each duty cycle value for a few times.
3-2	R / W	Fading led extend enable bits 00 : No extend. 01 : Only extend the minimum duty cycle. 211: Only extend the maximum duty cycle. 11 : Both extend the minimum and the maximum duty cycle.
1	R / W	Led frequency before frequency divider select Fading led is only allowed when this bit select 1 (1kHz). When this bit turn to 0 (4Hz). It force to solid led mode regardless Fading led enable bit (LD15 CRF5 Bit0). 0 : 4Hz 1 : 1kHz (default)

BIT	READ / WRITE	DESCRIPTION											
0	R / W	Fading led enable 0 : Solid Led 1 : Fading Led	<table border="1"> <tr> <td>LD15 CRF5 bit[1:0]</td><td>Led mode</td></tr> <tr> <td>00</td><td>Solid led and 4Hz before divide</td></tr> <tr> <td>01</td><td>Solid led and 4Hz before divide</td></tr> <tr> <td>10</td><td>Solid led and 1kHz before divide</td></tr> <tr> <td>11</td><td>Fading led and 1kHz before divide</td></tr> </table>	LD15 CRF5 bit[1:0]	Led mode	00	Solid led and 4Hz before divide	01	Solid led and 4Hz before divide	10	Solid led and 1kHz before divide	11	Fading led and 1kHz before divide
LD15 CRF5 bit[1:0]	Led mode												
00	Solid led and 4Hz before divide												
01	Solid led and 4Hz before divide												
10	Solid led and 1kHz before divide												
11	Fading led and 1kHz before divide												
LD15 CRF5 bit[1:0]													
00													
01													
10													
11													

CR F6h. Fading Led Light Extend Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	This byte is the time for extend the maximum duty cycle value. The extend time reference to fading led frequency : $\text{Extend time} = (\text{extend value} * 4) / \text{fading led frequency}$

CR F7h. Fading Led Dark Extend Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 0Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	This byte is the time for extend the minimum duty cycle value. The extend time reference to fading led frequency : $\text{Extend time} = (\text{extend value} * 4) / \text{fading led frequency}$

CR F8h. Fading Led Frequency Divider Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 10h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION																																				
7-0	R / W	<p>Fading led frequency divide factor when fading frequency before divider select = 1 (It can select fading or solid mode depend on LD15 CRF5 bit0)</p> <p style="text-align: center;">led frequency</p> <table> <tbody> <tr><td>0x01:</td><td>1kHz/1</td><td>= 1kHz</td></tr> <tr><td>0x02:</td><td>1kHz/2</td><td>= 500Hz</td></tr> <tr><td></td><td></td><td>...</td></tr> <tr><td>0x10:</td><td>1kHz/16</td><td>= 62Hz (default)</td></tr> <tr><td></td><td></td><td>...</td></tr> <tr><td>0xFF:</td><td>1kHz/255</td><td>= 4Hz</td></tr> </tbody> </table> <p>When fading led frequency before divider select = 0 (It force to solid led mode)</p> <p style="text-align: center;">Solid led frequency</p> <table> <tbody> <tr><td>0x00:</td><td>Output low</td></tr> <tr><td>0x01:</td><td>High-z</td></tr> <tr><td>0x02:</td><td>4Hz</td></tr> <tr><td>0x03:</td><td>2Hz</td></tr> <tr><td>0x04:</td><td>1Hz</td></tr> <tr><td>0x05:</td><td>1/2Hz</td></tr> <tr><td>0x06:</td><td>1/4Hz</td></tr> <tr><td>0x07:</td><td>Output low</td></tr> <tr><td>others</td><td>High-z</td></tr> </tbody> </table>	0x01:	1kHz/1	= 1kHz	0x02:	1kHz/2	= 500Hz			...	0x10:	1kHz/16	= 62Hz (default)			...	0xFF:	1kHz/255	= 4Hz	0x00:	Output low	0x01:	High-z	0x02:	4Hz	0x03:	2Hz	0x04:	1Hz	0x05:	1/2Hz	0x06:	1/4Hz	0x07:	Output low	others	High-z
0x01:	1kHz/1	= 1kHz																																				
0x02:	1kHz/2	= 500Hz																																				
		...																																				
0x10:	1kHz/16	= 62Hz (default)																																				
		...																																				
0xFF:	1kHz/255	= 4Hz																																				
0x00:	Output low																																					
0x01:	High-z																																					
0x02:	4Hz																																					
0x03:	2Hz																																					
0x04:	1Hz																																					
0x05:	1/2Hz																																					
0x06:	1/4Hz																																					
0x07:	Output low																																					
others	High-z																																					

CR F9h. Fading Led Decrease Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 06h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	<p>Fading_led_duty_dec_l</p> <p>The decreased duty cycle value between the turning point and the minimum duty cycle value.</p>

CR Fah. Fading Led Decrease Duty Cycle Value Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 05h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	<p>Fading_led_duty_dec_h</p> <p>The decreased duty cycle value between the maximum duty cycle value and the turning point.</p>

23.18 Logical Device 16

CR 30h. Deep Sleep Configuration Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : A0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_SLPsus_PULLUP (test mode) 0: Enable SLP_SUS# internal pull-up. 1: Disable SLP_SUS# internal pull-up.
6-1	Reserved	
0	R / W	Deep S5 Enable 0: Disable Deep S5 function when into S5 state (SLP_S5#). 1: Enable Deep S5 function when into S5 state (SLP_S5#).

CR E0h. Deep Sleep wake up PSOUT# delay time

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : **20h** (Default: 512ms)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = (3F) _{hex} * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : **04h** (Default: 128 ms)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * 32ms Example : maximum pulse width = (F) _{hex} * 32ms = 480ms

CR E2h. Deep Sleep Delay Time Control

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 05h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6-0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

CR E3h. WDT1 to Deep Sleep Delay Time Control

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	Watchdog Timer 1 wake up auto mode. 0: SIO will not wake up system after RSMRST release 1: SIO will wake up system after RSMRST release.
1-0	R / W	Deep Sleep Watchdog Timer 1 Delay Time Control. When system will enter Deeps5 by watchdog timer 1, SIO will set a delay time to control. Delay time: 2, 4, 6, 8 sec = register: 0, 1, 2, 3

CR F3h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 80h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	<p>LCLK_FRQ[7:0]</p> <p>$LCLK / (31.25\text{KHz} * 2) = LCLK_FRQ$</p> <p>Example:</p> <p>$33\text{MHz} / (31.25\text{KHz} * 2) = 11'h210 = 11'd528$</p> <p>$24\text{MHz} / (31.25\text{KHz} * 2) = 11'h180 = 11'd384$</p>

CR F4h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	<p>LCLK_FRQ[10:8]</p> <p>$LCLK / (31.25\text{KHz} * 2) = LCLK_FRQ$</p> <p>Example:</p> <p>$33\text{MHz} / (31.25\text{KHz} * 2) = 11'h210 = 11'd528$</p> <p>$24\text{MHz} / (31.25\text{KHz} * 2) = 11'h180 = 11'd384$</p>

CR F5h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	<p>EN_CALI</p> <p>0: Disable Oscillator free calibrate</p> <p>1: Enable Oscillator free calibrate</p>

CR F8h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 20h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	EN_PLL 0: Disable Oscillator free 1: Enable Oscillator free
4-0	Reserved	

24. SPECIFICATIONS

24.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

24.2 DC CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 5\%$, $V_{DD} = 1.8\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	I _{BAT}			2.4	μA	$V_{BAT} = 2.5\text{ V}$
ACPI Stand-by Power Supply Quiescent Current	I _{VSB}			8.0	mA	$V_{SB} = 3.3\text{ V}$, All ACPI pins are not connected.
VCC Quiescent Current	I _{VCC}			25	mA	$V_{SB} (\text{AVSB})= 3.3\text{ V}$ $V_{CC}= 3.3\text{ V}$ $LRESET =$ High $CASEOPEN$ $\text{Pull-Up to } V_{BAT}$
VTT Quiescent Current	I _{VTT}			1	mA	$V_{SB} (\text{AVSB})= 3.3\text{ V}$ $V_{CC}= 3.3\text{ V}$ $V_{TT} = 1.2\text{V}$ $LRESET =$ High $CASEOPEN$ $\text{Pull-Up to } V_{BAT}$
AIN – Analog input						
AOUT – Analog output						
In_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	V _{IL}			0.8	V	
Input High Voltage	V _{IH}	2.0			V	

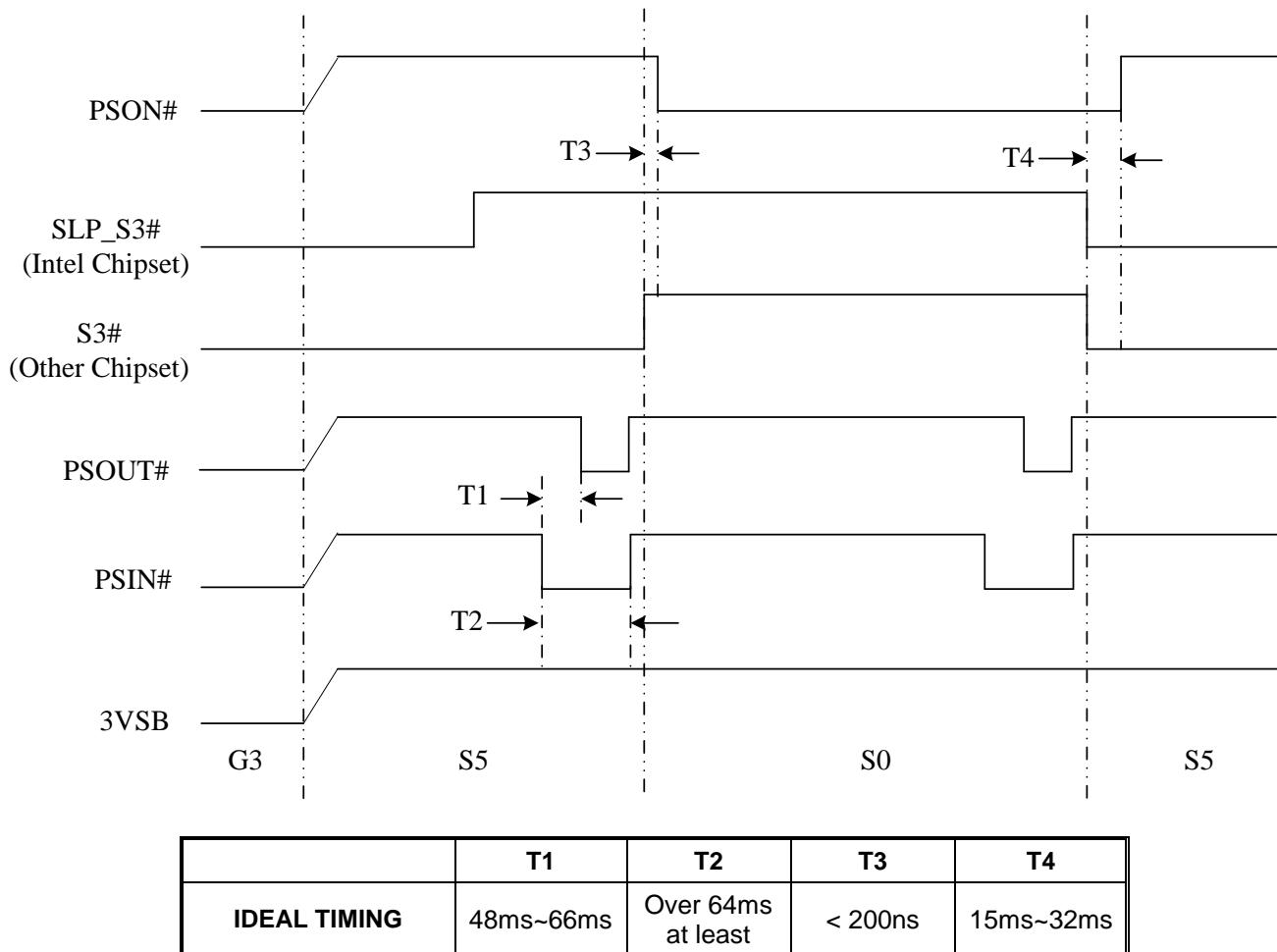
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{sp3} – 3.3V Schmitt-trigger input for AMD SB-TSI						
Input Low Threshold Voltage	V _{t-}			0.4*V _{TT}	V	
Input High Threshold Voltage	V _{t+}	0.6*V _{TT}			V	
Hystersis	V _{TH}		0.2*V _{TT}		V	
Input High Leakage	I _{LH}			+10	µA	V _{IN} = V _{TT}
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{tp318} – 3.3V/1.8V input pin						
Input Low Voltage	V _{IL}			0.8	V	
Input High Voltage	V _{IH}	1.5			V	
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{sp318} – 3.3V/1.8V Schmitt-trigger input pin						
Input Low Threshold Voltage	V _{t-}	0.8	0.9	1.1	V	
Input High Threshold Voltage	V _{t+}	1.1	1.2	1.4	V	
Hystersis	V _{TH}		0.2		V	
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{gp3} – 3.3V GTL-level input pin						
Input Low Voltage	V _{IL}		0.72		V	
Input High Voltage	V _{IH}		0.72		V	
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V _{IL}			0.8	V	
Input High Voltage	V _{IH}	2.0			V	
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V _{t-}	0.5	0.8	1.1	V	V _{IN} = 3.3 V
Input High Threshold Voltage	V _{t+}	1.6	2.0	2.4	V	V _{IN} = 3.3 V
Hystersis	V _{TH}	0.5	1.2		V	V _{IN} = 3.3 V
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3 V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
In_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V _{t-}	0.5	0.8	1.1	V	V _{IN} = 3.3 V
Input High Threshold Voltage	V _{t+}	1.6	2.0	2.4	V	V _{IN} = 3.3 V
Hysteresis	V _{TH}	0.5	1.2		V	V _{IN} = 3.3 V
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3 V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
In_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V _{IL}			0.8	V	
Input High Voltage	V _{IH}	2.0			V	
Input High Leakage	I _{LH}			+10	µA	V _{IN} = 3.3V
Input Low Leakage	I _{LIL}			-10	µA	V _{IN} = 0 V
O8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 8 mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -8 mA
OD8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 8 mA
OX8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 8 mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -8 mA, PAD_VDD=3.3V
Output High Voltage	V _{OH}	1.31			V	I _{OH} = -8 mA, PAD_VDD=1.8V
ODX8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 8 mA
O12 – Output pin with 12mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 12 mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -12 mA
OD12 – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 12 mA
O16 – Output pin with 16mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 16 mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -16 mA
OD16 – Open-drain output pin with 16mA sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 16 mA
O24 – Output pin with 24mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 24 mA

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -24 mA
OD24 – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 24 mA
O48 – Output pin with 48mA source-sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 48 mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -48 mA
OD48 – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECL						
Input Low Voltage	V _{IL}	0.275*V _{TT}		0.5*V _{TT}	V	
Input High Voltage	V _{IH}	0.55*V _{TT}		0.725*V _{TT}	V	
Output Low Voltage	V _{OL}			0.25*V _{TT}	V	
Output High Voltage	V _{OH}	0.75*V _{TT}			V	
Hysteresis	V _{Hys}	0.1*V _{TT}			V	
O12cu – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 12 mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} = -12 mA
OD12cu – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 12 mA

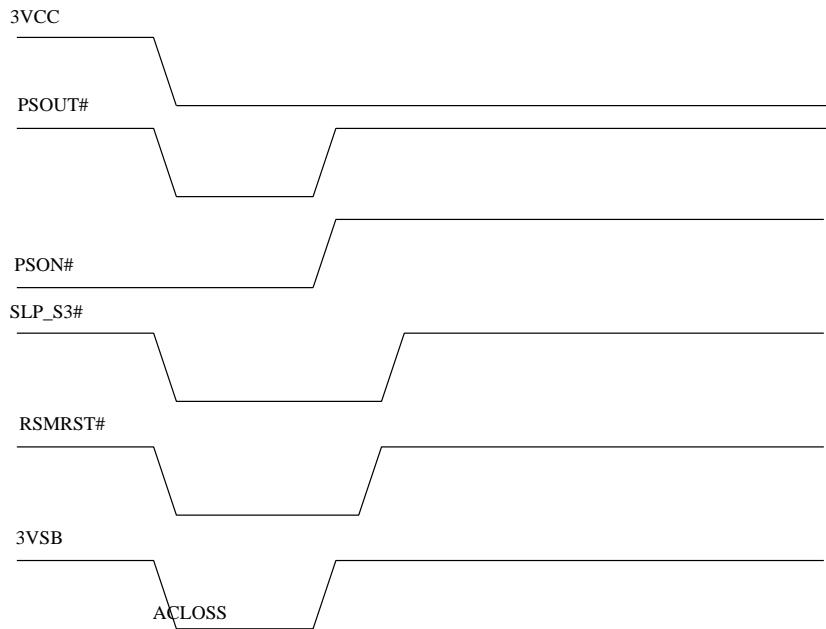
25. AC CHARACTERISTICS

25.1 Power On / Off Timing

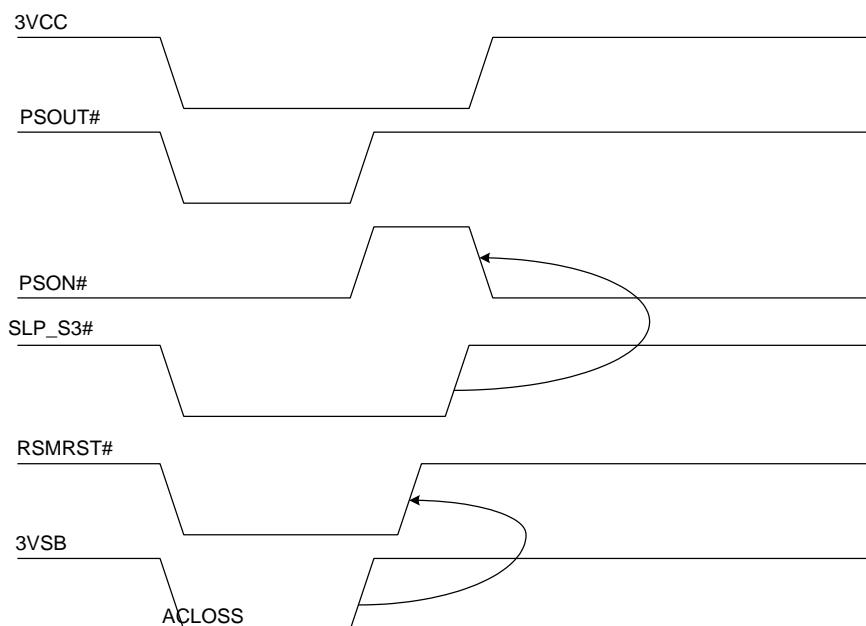


25.2 AC Power Failure Resume Timing

(1) Logical Device A, CR [E4h] bits [6:5]=00 means “OFF” state
 (“OFF” means the system is always turned off after the AC power loss recovered.)



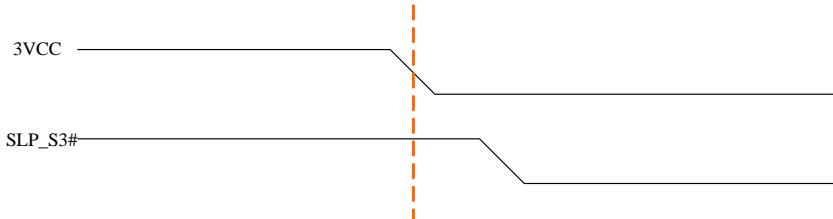
(2) Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.
 (“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

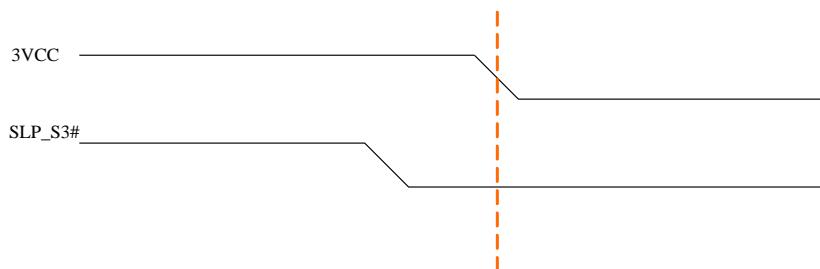
- 1) The previous state is “ON”

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



- 2) The previous state is “OFF”

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT5582D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be “On” or “Off”. According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

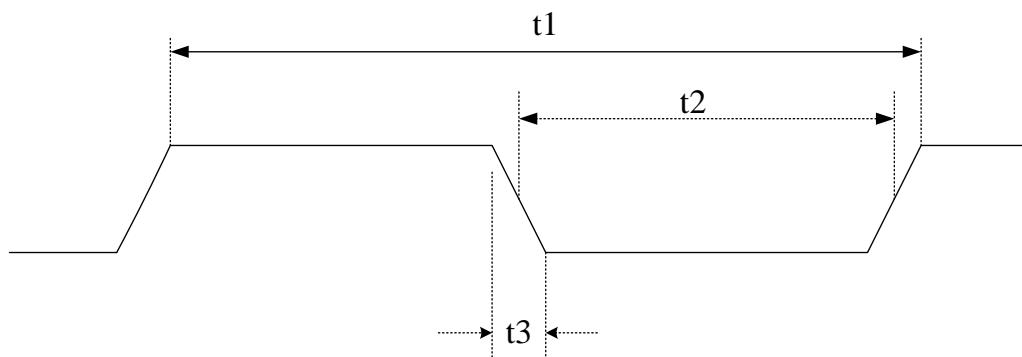
BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. (VBAT) 0: ON 1: OFF

25.3 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

25.4 LPC timing

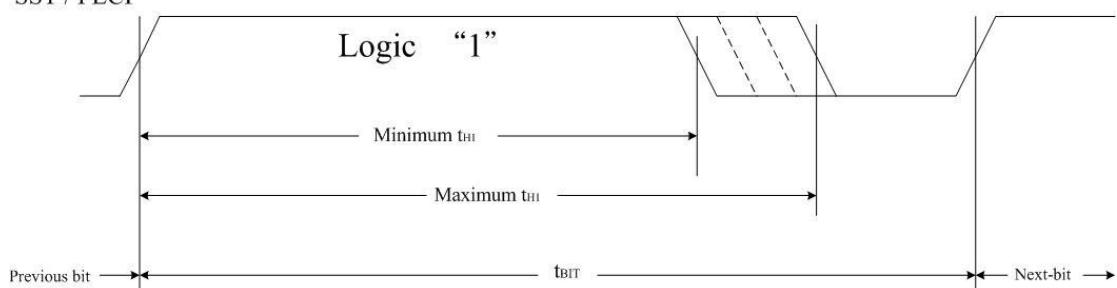
PCI_CLK AC Specification					
Symbol	Parameter	MIN	Typical	MAX	Units
T _{CYC}	PCI_CLK cycle	30		42	ns
T _{per}	PCI_CLK period	35	50	65	%

LPC AC Specification (24MHz)					
Symbol	Parameter	MIN	Typical	MAX	Units
T _{co}	Tx Rising Clock to Data Output Delay	3.3		7.8	ns
T _{SU}	Rx Data Setup Time to CLK Rising Edge	10.4			ns
T _{HD}	Rx Data Hold Time to CLK Rising Edge	0			ns
T _R	Input Rise Time			8.4	ns
T _F	Input Fall Time			8.4	ns

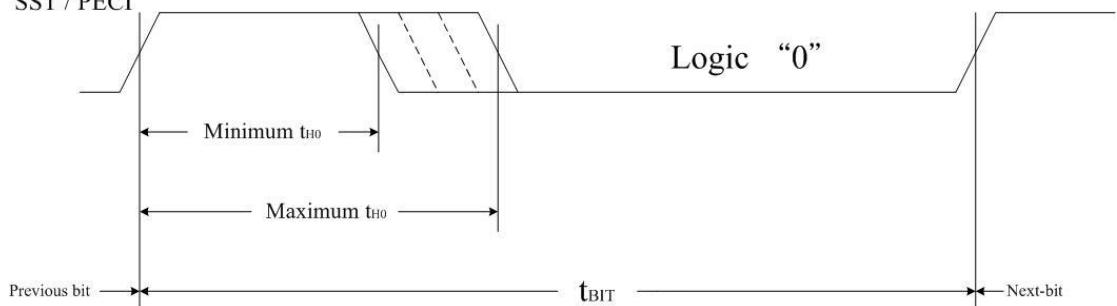
LPC AC Specification (33MHz)					
Symbol	Parameter	MIN	Typical	MAX	Units
T _{co}	Tx Rising Clock to Data Output Delay	3.3		7.8	ns
T _{SU}	Rx Data Setup Time to CLK Rising Edge	8			ns
T _{HD}	Rx Data Hold Time to CLK Rising Edge	0			ns
T _R	Input Rise Time			6	ns
T _F	Input Fall Time			6	ns

25.5 PECL Timing

SST / PECL

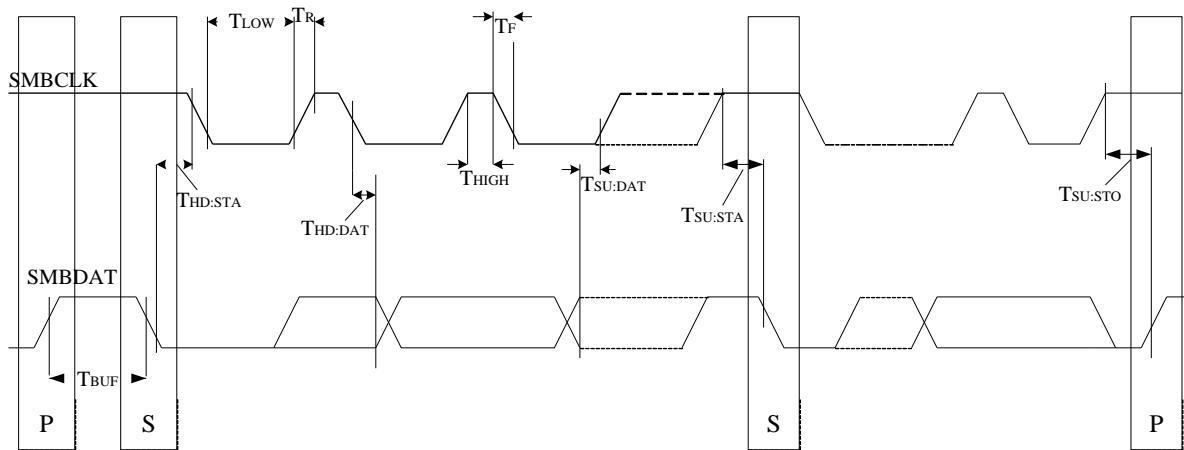


SST / PECL



SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	$\times t_{BIT}$
t_{H0}		0.2	1/4	0.4	$\times t_{BIT}$

25.6 SMBus Timing

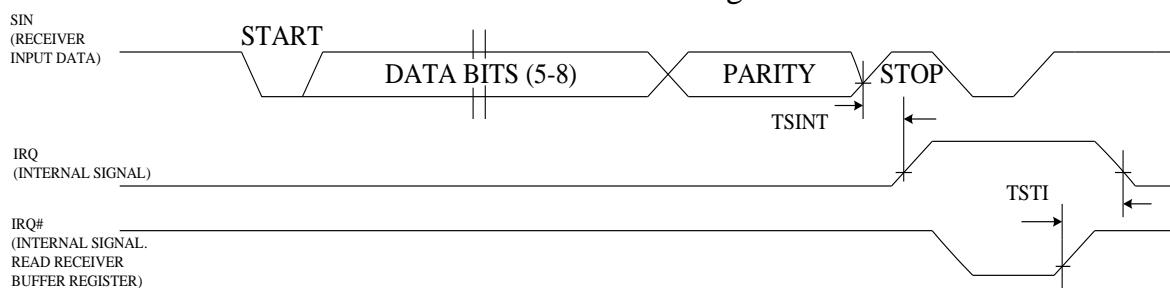


25.7 UART

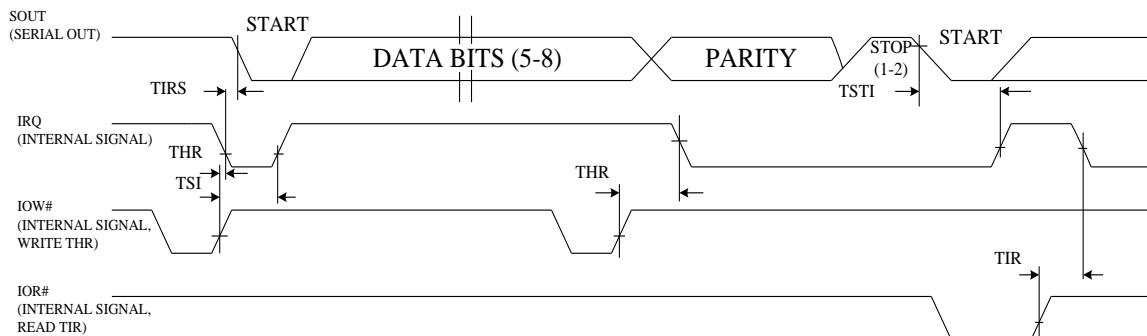
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from <u>IOR</u> Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial <u>IOW</u> to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from <u>IOR</u> to Reset Interrupt	TIR		8	250	nS
Delay from <u>IOR</u> to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from <u>IOR</u>	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		$2^{16}-1$	

UART Receiver Timing

Receiver Timing



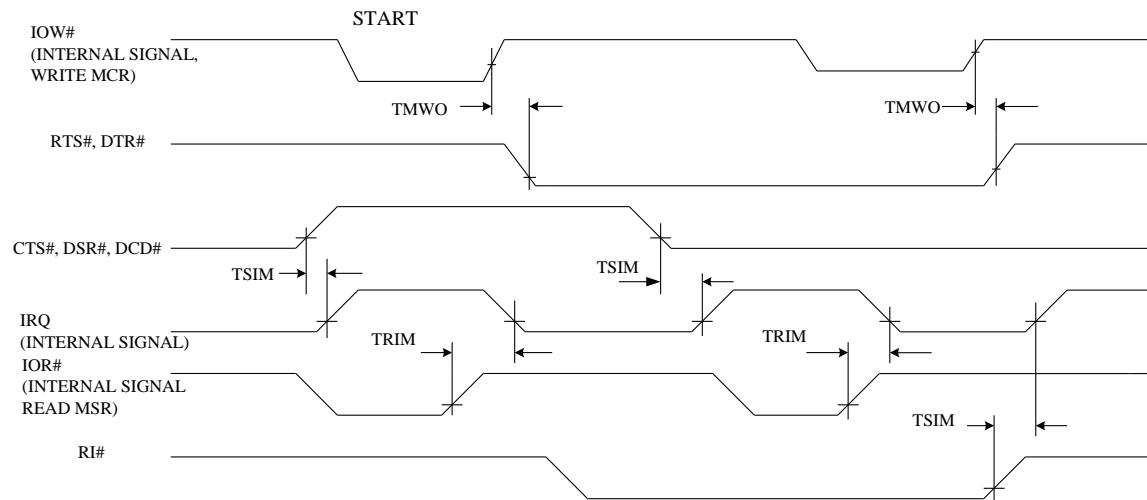
UART Transmitter Timing



25.8 Modem Control Timing

Modem Control Timing

MODEM Control Timing



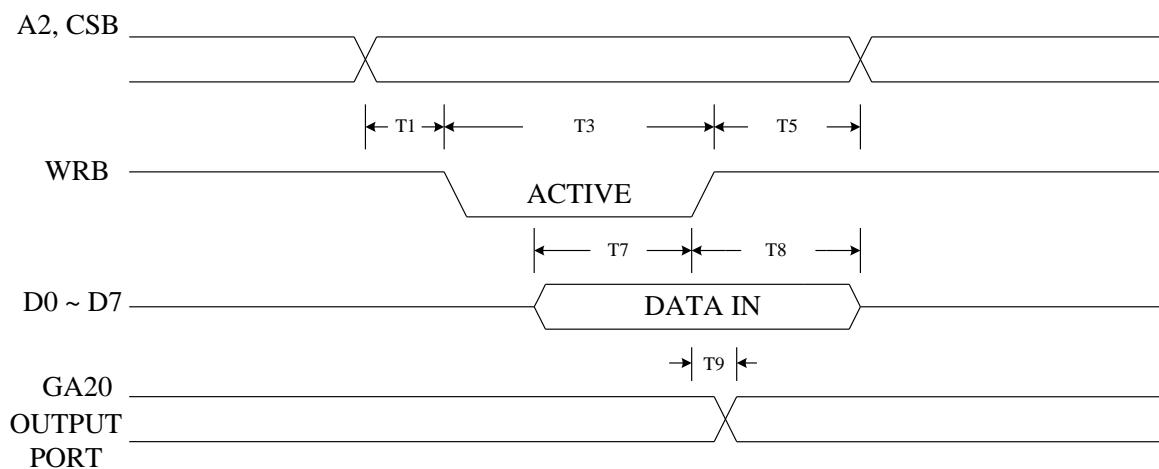
25.9 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS

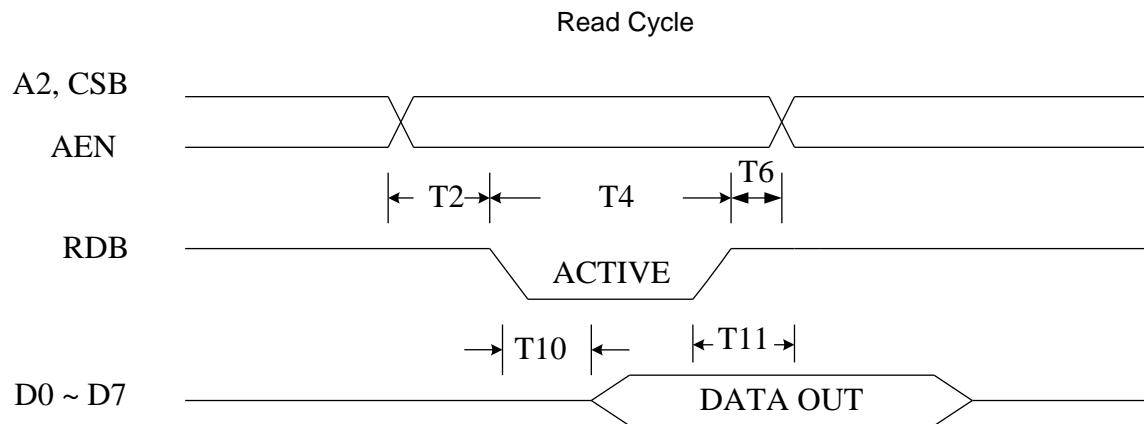
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	μS
T13	K/B Clock Period	20		μS
T14	K/B Clock Pulse Width	10		μS
T15	Data Valid Before Clock Falling (RECEIVE)	4		μS
T16	K/B ACK After Finish Receiving	20		μS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		μS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	μS
T23	Duration of CLK active	30	50	μS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	μS
T25	Time of inhibit mode	100	300	μS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	μS
T27	Duration of CLK inactive	30	50	μS
T28	Duration of CLK active	30	50	μS
T29	Time from DATA transition to falling edge of CLK	5	25	μS

25.9.1 Writing Cycle Timing

Write Cycle Timing

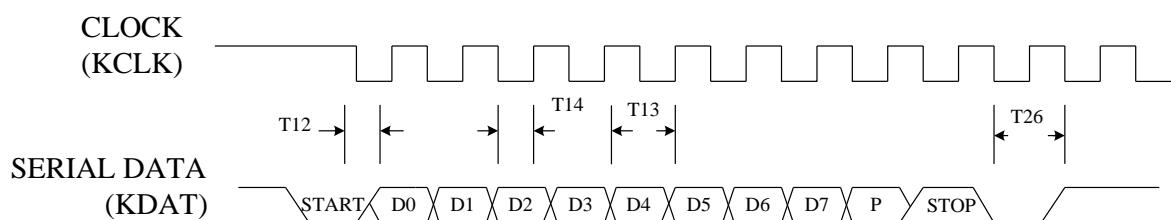


25.9.2 Read Cycle Timing



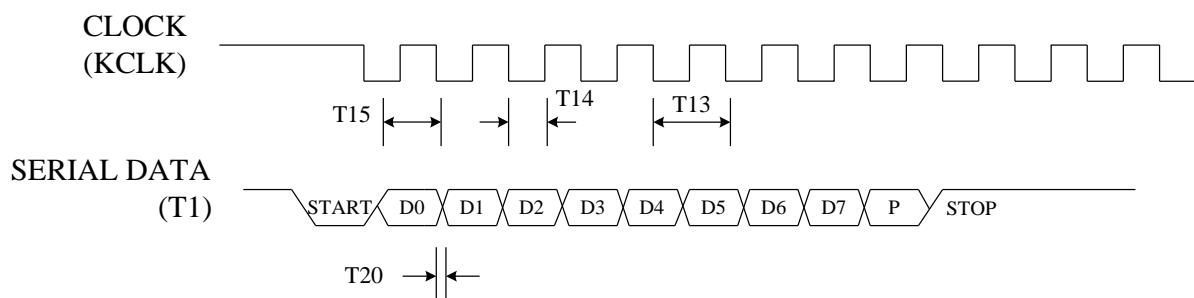
25.9.3 Send Data to K/B

Send Data to K/B



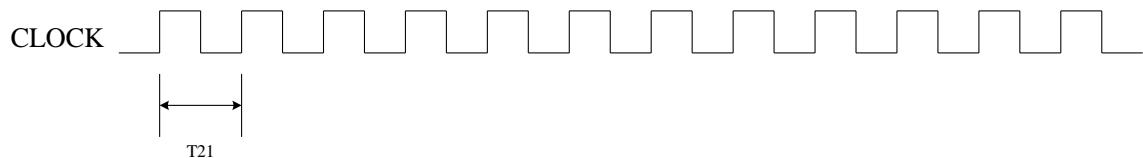
25.9.4 Receive Data from K/B

Receive Data from K/B



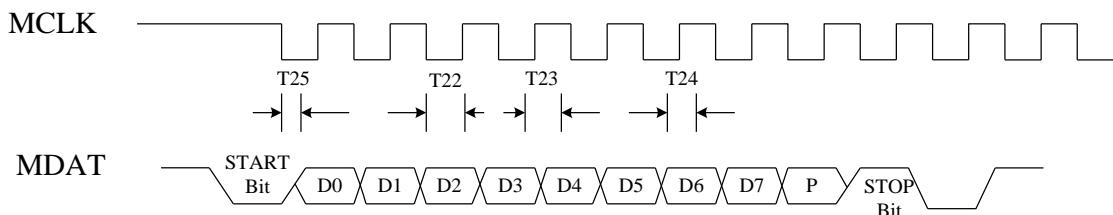
25.9.5 Input Clock

Input Clock



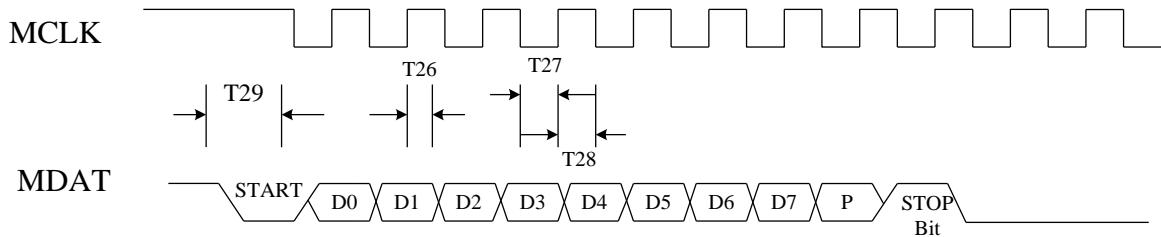
25.9.6 Send Data to Mouse

Send Data to Mouse



25.9.7 Receive Data from Mouse

Receive Data from Mouse



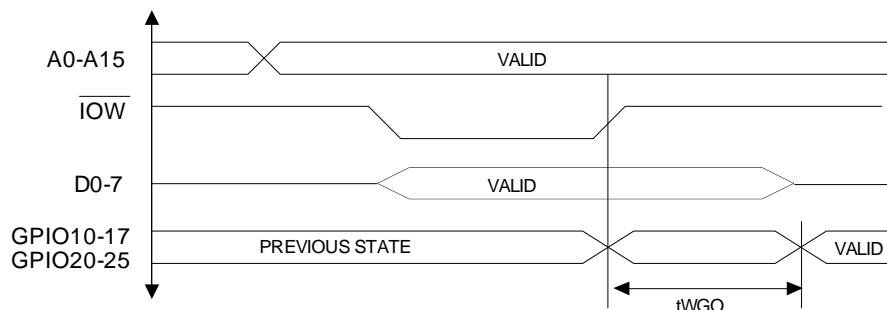
25.10 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns

Note: Refer to Microprocessor Interface Timing for Read Timing.

25.10.1 GPIO Write Timing

GPIO Write Timing diagram



26. TOP MARKING SPECIFICATIONS



1st line: Nuvoton logo

2nd line: part number NCT5582D

3rd line: wafer production series lot number 28201234

4th line: tracking code 734G7CFA

734: packages made in 2017, week 34

G: assembly house ID; G means GR, A means ASE, etc.

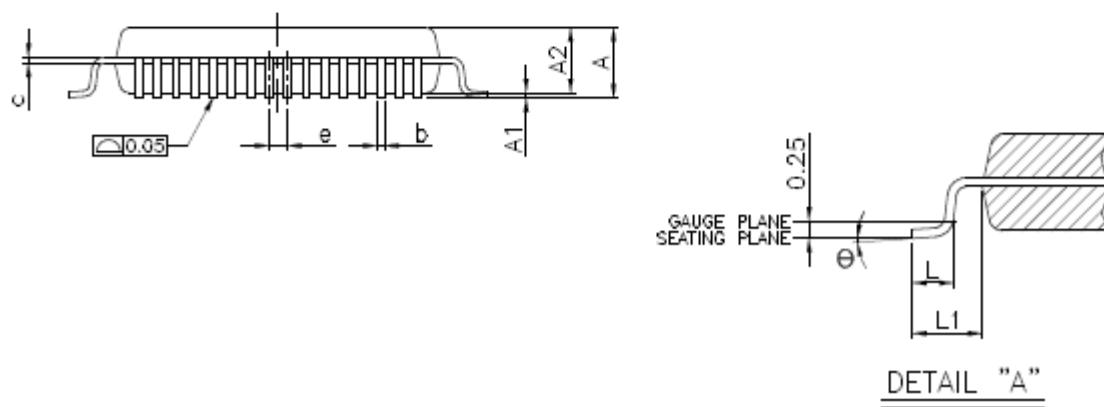
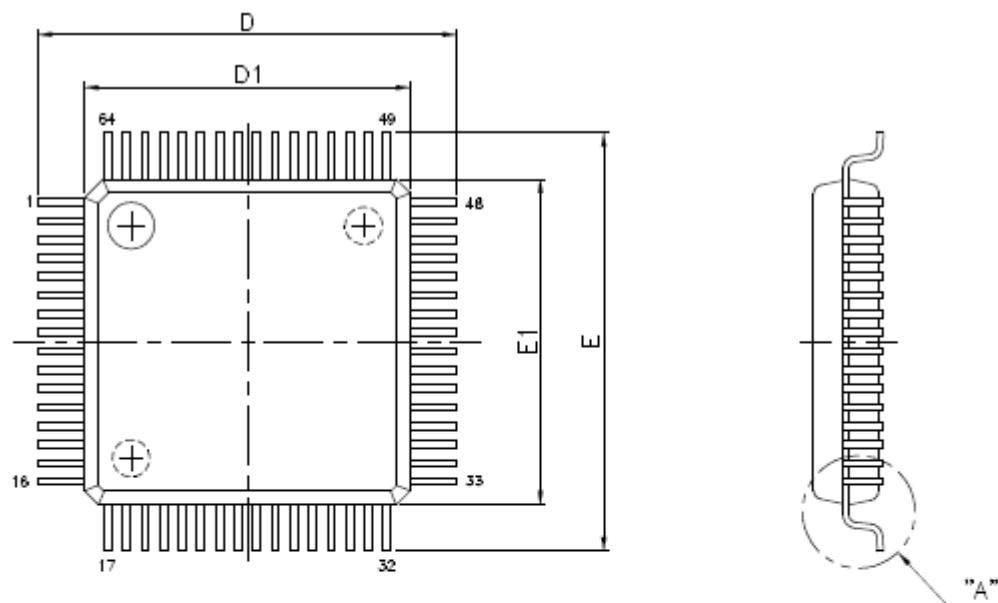
7: code version; 7 means code 007

C: IC revision; A means version A; B means version B, and C means version C

FA: Nuvoton internal use.

27. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT5582D	64Pin LQFP (Green package)	Commercial, 0°C to +70°C

28. PACKAGE SPECIFICATION

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
ε	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

64-pin (LQFP, 7x7x1.4mm)

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.5	09/08/2017	N.A.	First release datasheet
0.6	11/02/2017	308.309.310. 311.317.320. 383.386.387.	Modify AUXFAN2 register
1.0	01/22/2018	76	Modify OVT setting
1.1	12/10/2018	27 406	Modify PWROK block diagram Modify LPC timing

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