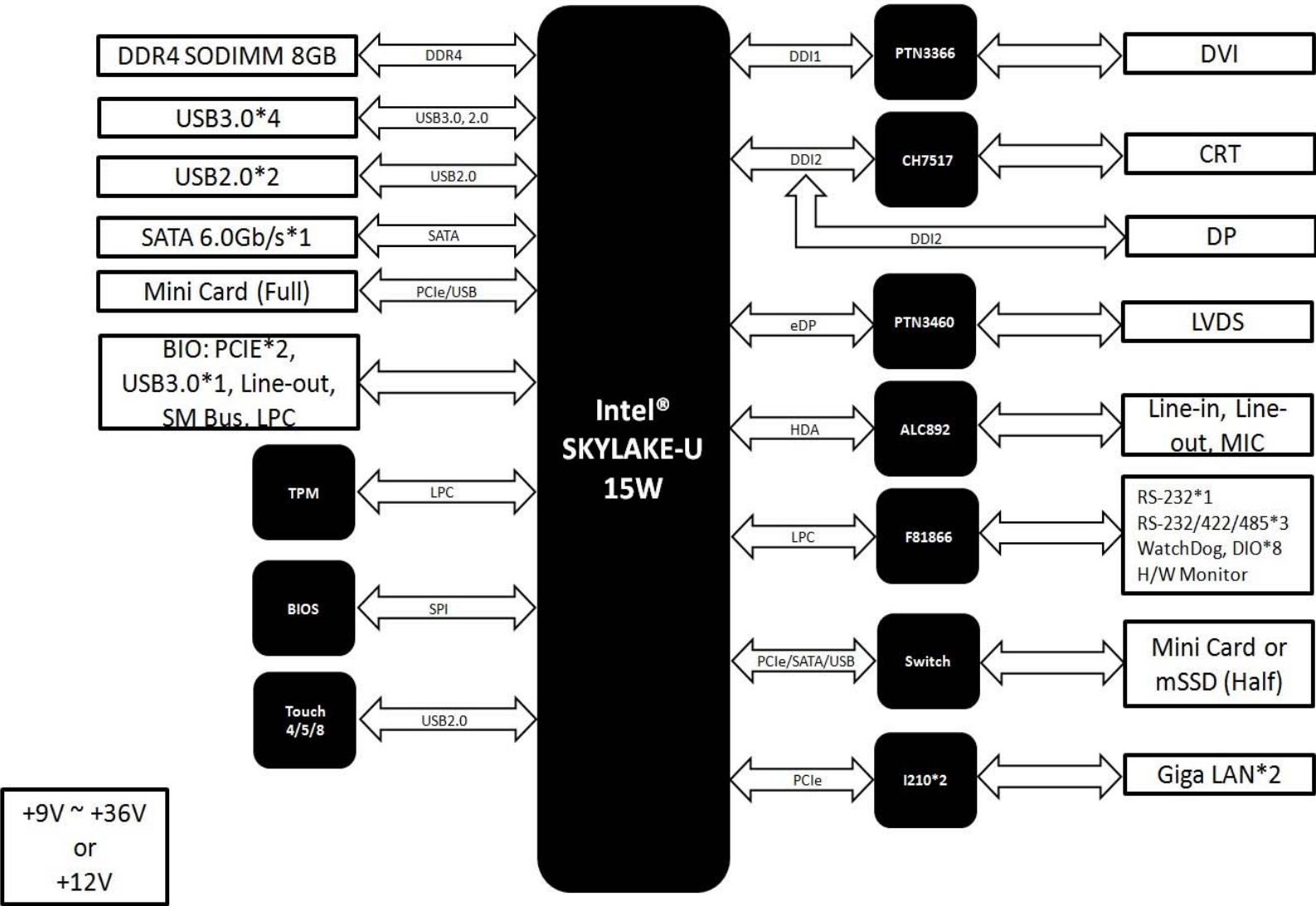
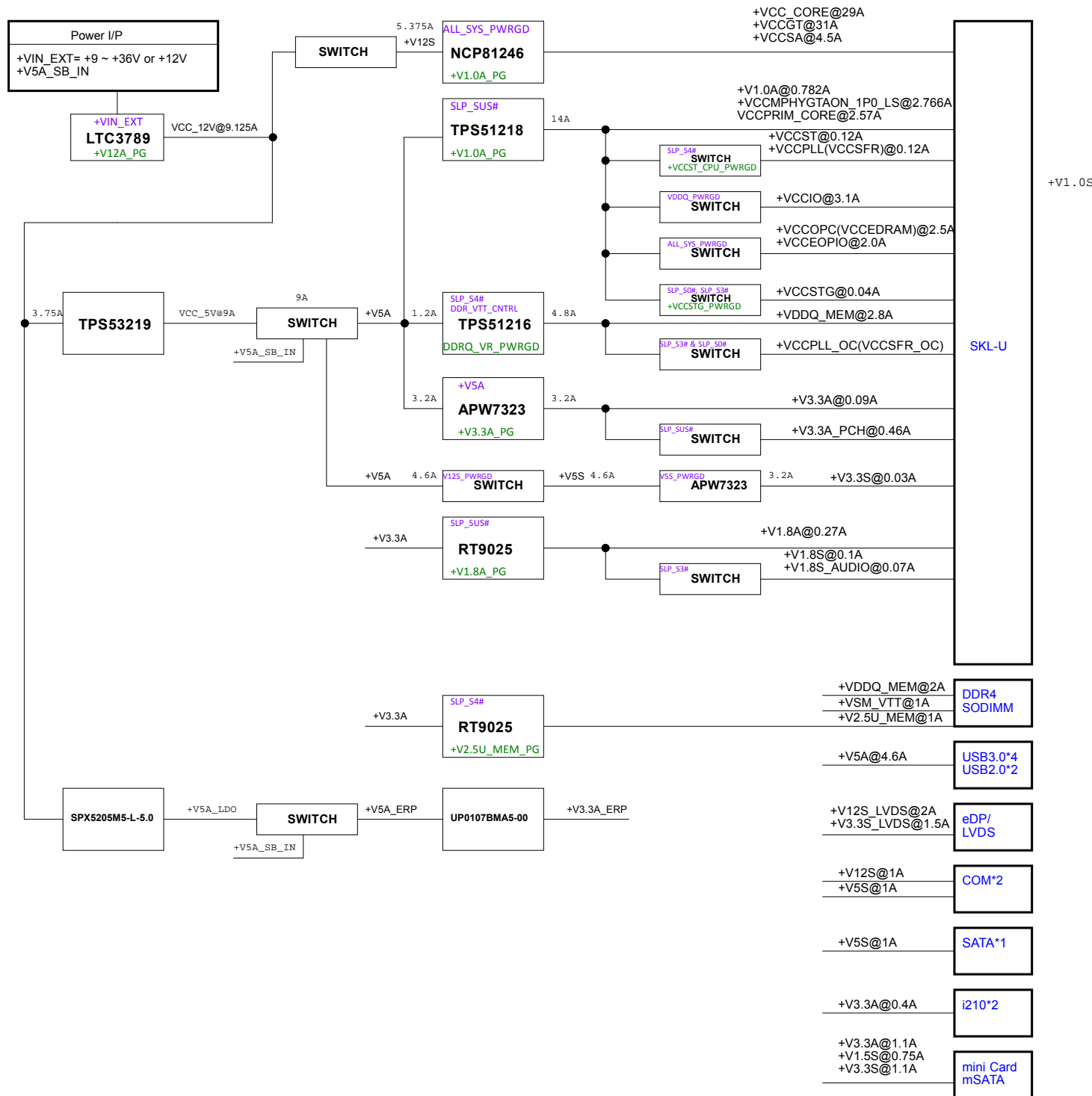


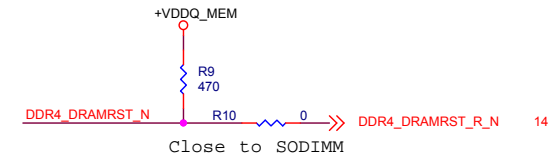
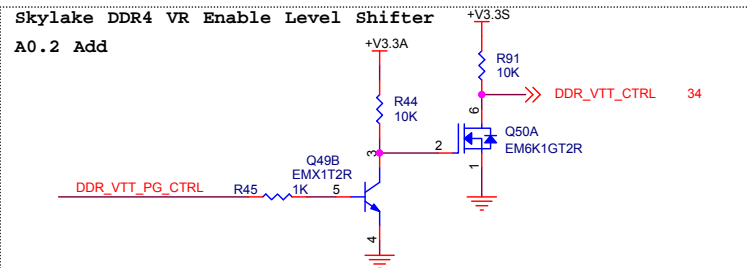
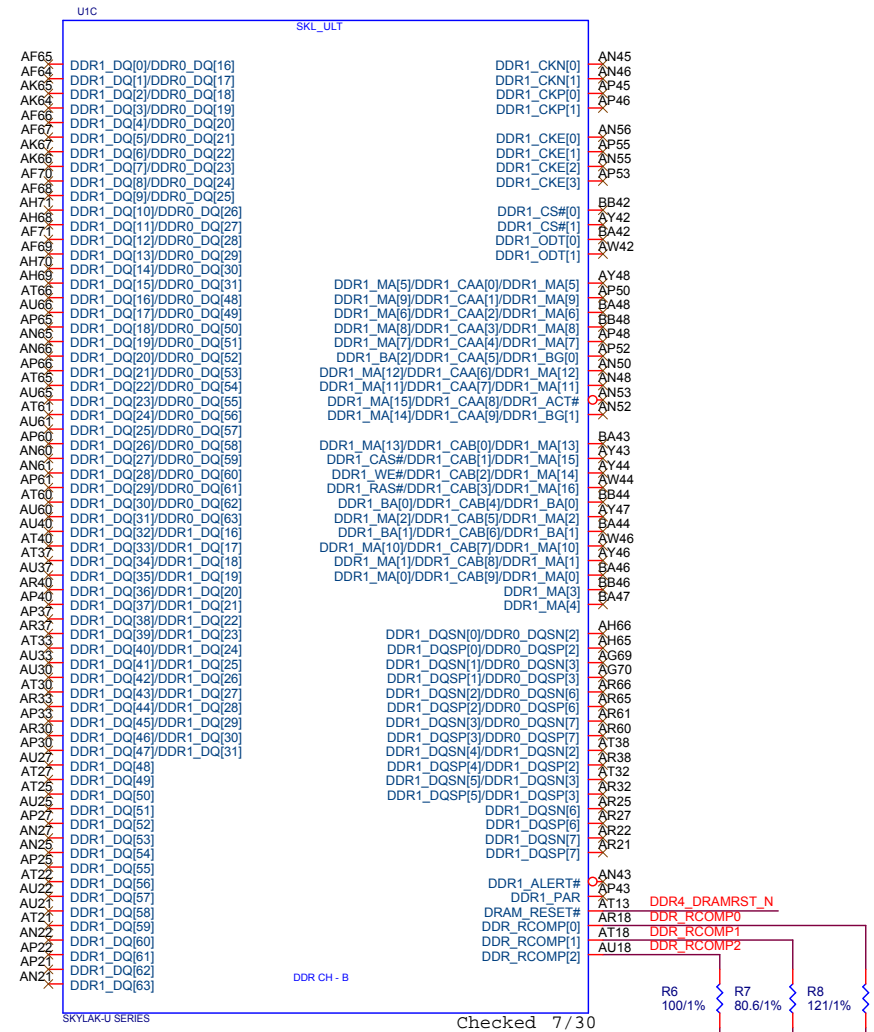
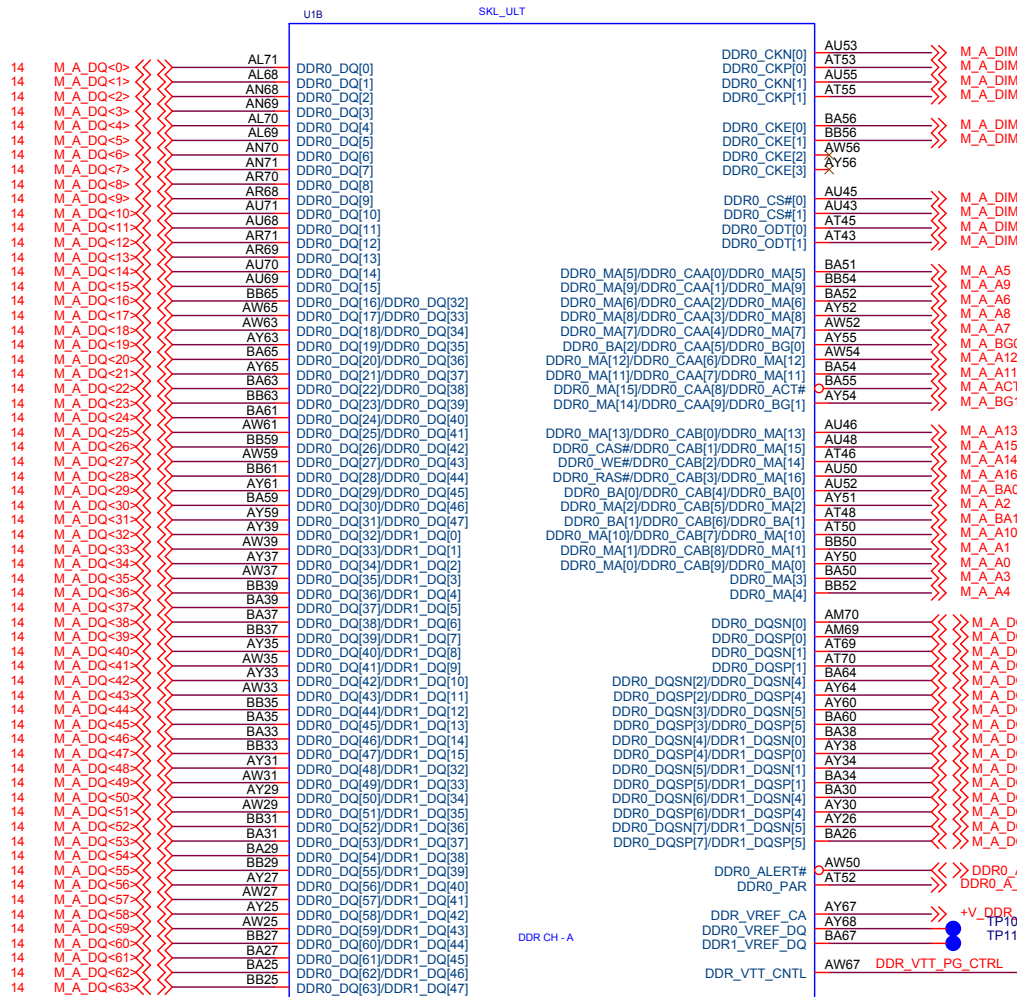
GENE-SKU6



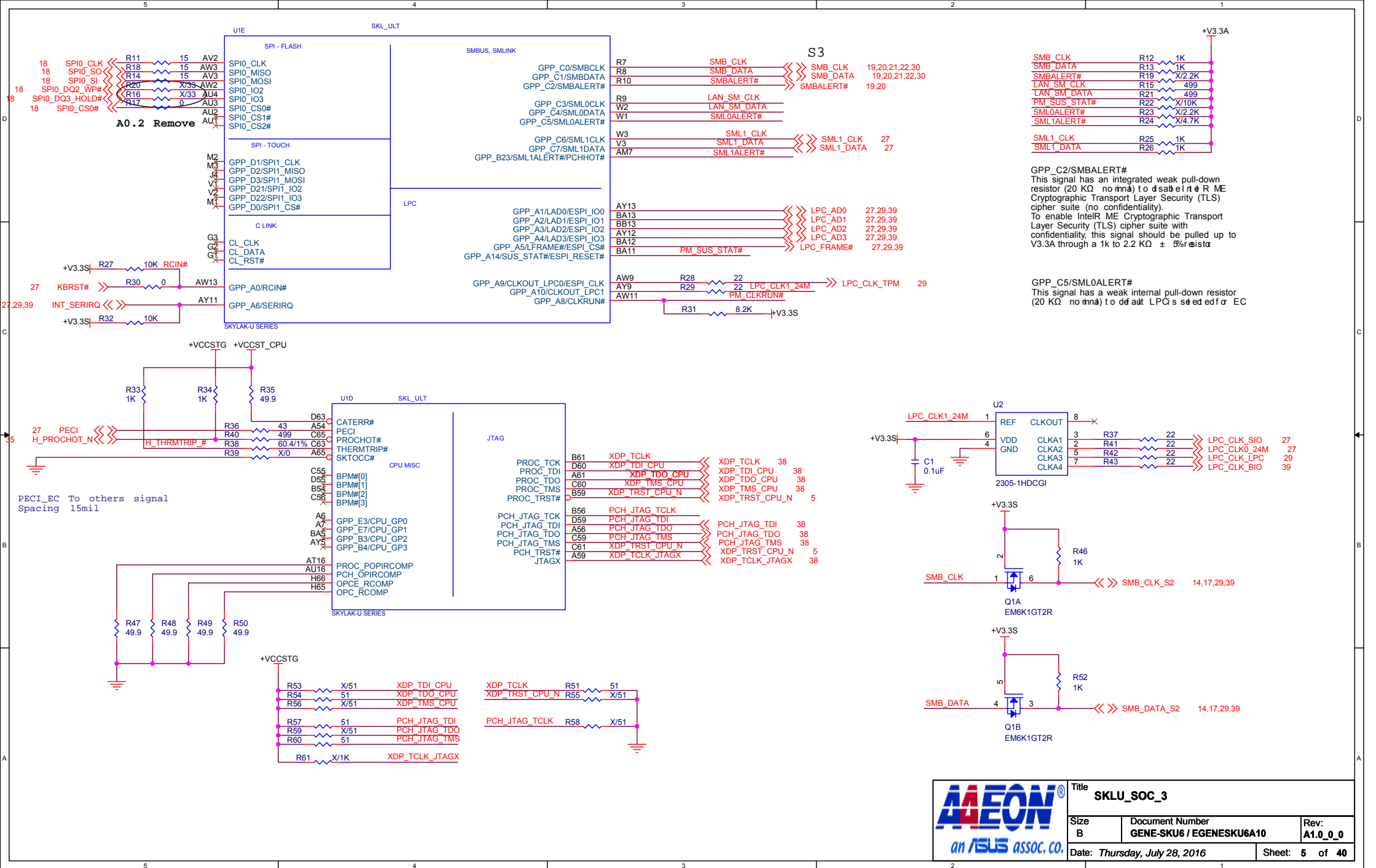
Title Block diagram		
Size B	Document Number GENE-SKU6 / EGENESKU6A10	Rev: A1.0_0_0
Date: Thursday, July 28, 2016		Sheet: 1 of 40

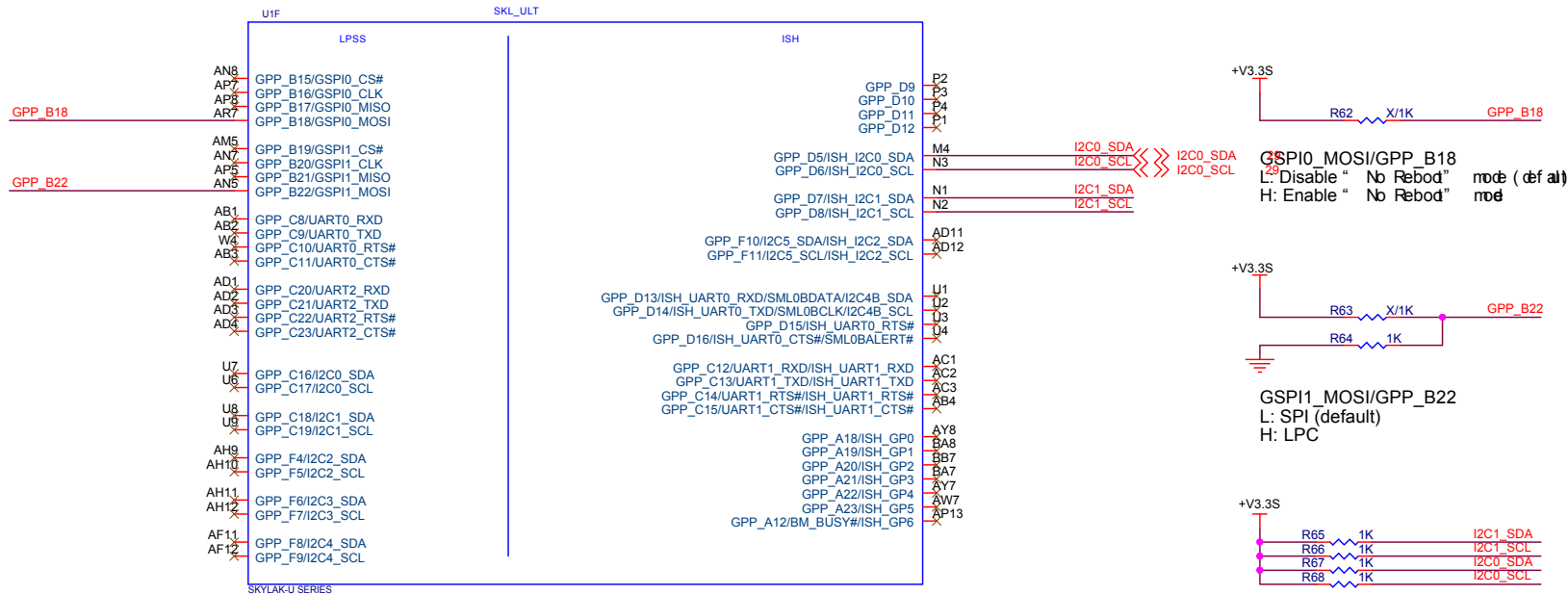






Title SKLU_SOC_2(DDR4)		
Size B	Document Number GENE-SKU6 / EGENESKU6A10	Rev: A1.0_0_0
Date: Thursday, July 28, 2016	Sheet: 4 of 40	





GSP10\_MOSI/GPP\_B18  
L: Disable " No Reboot" mode (default)  
H: Enable " No Reboot" mode


GSP11\_MOSI/GPP\_B22  
L: SPI (default)  
H: LPC

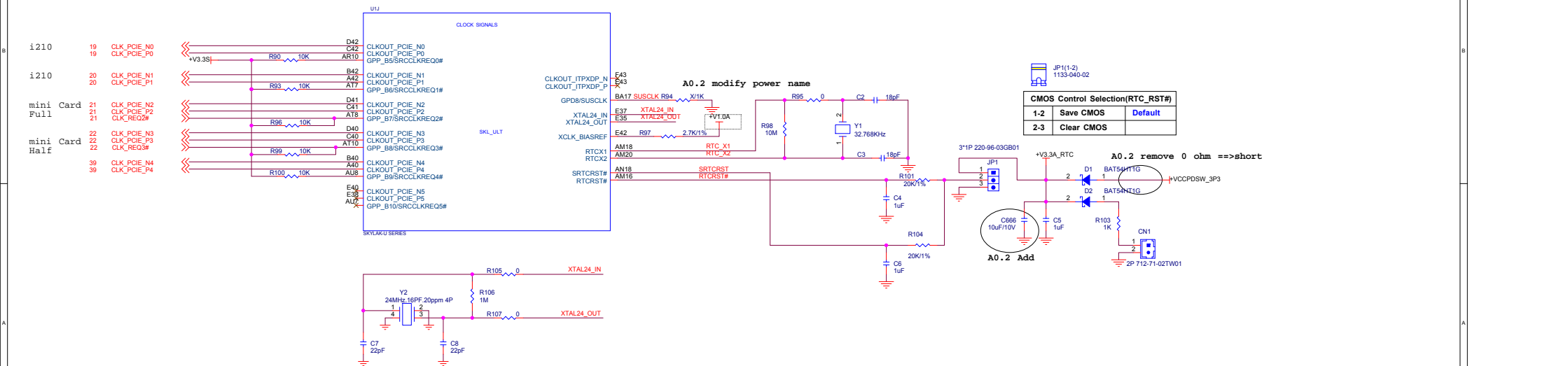
#### A0.2 modify power name

SPKR/GPP\_B14  
This signal has an integrated weak pull-down resistor (20 KΩ, no min) to disable Top Block Sway by default.  
To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 KΩ ± 5% resistor.

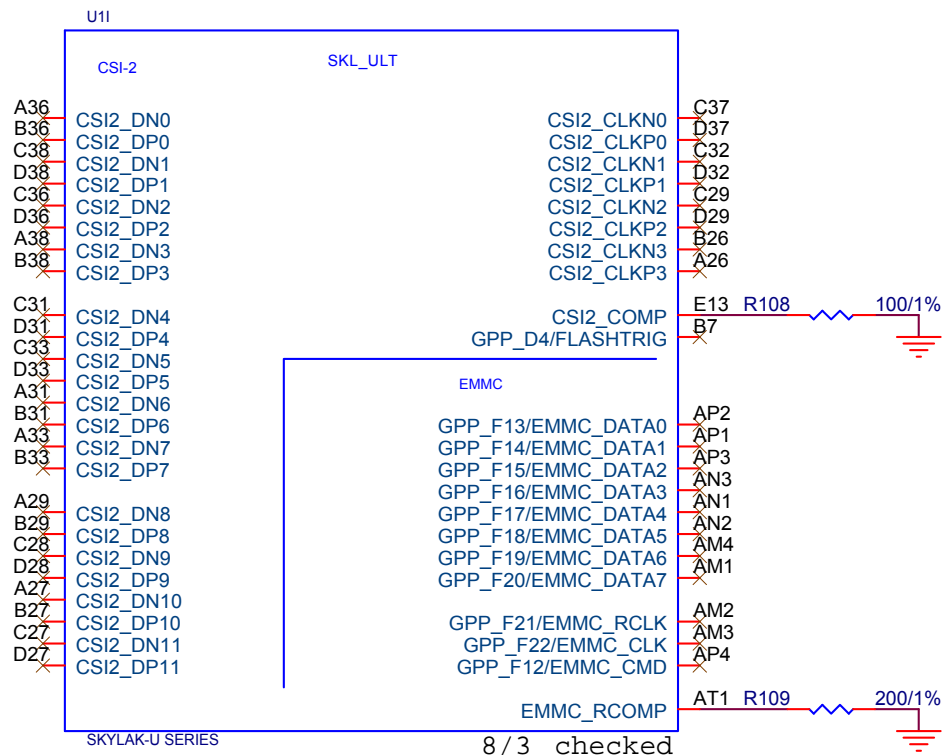
#### A0.2 modify power name

FLASH DESCRIPTOR SECURITY OVERRIDE  
HIGH: OVERRIDEN  
LOW: SECURITY MEASURES NOT OVERRIDEN  
WEAK INTERNAL PD

 an ASUS assoc. co.	Title SKLU_SOC_4		
	Size B	Document Number GENE-SKU6 / EGENESKU6A10	Rev: A1.0_0_0
	Date: Thursday, July 28, 2016		Sheet: 6 of 40

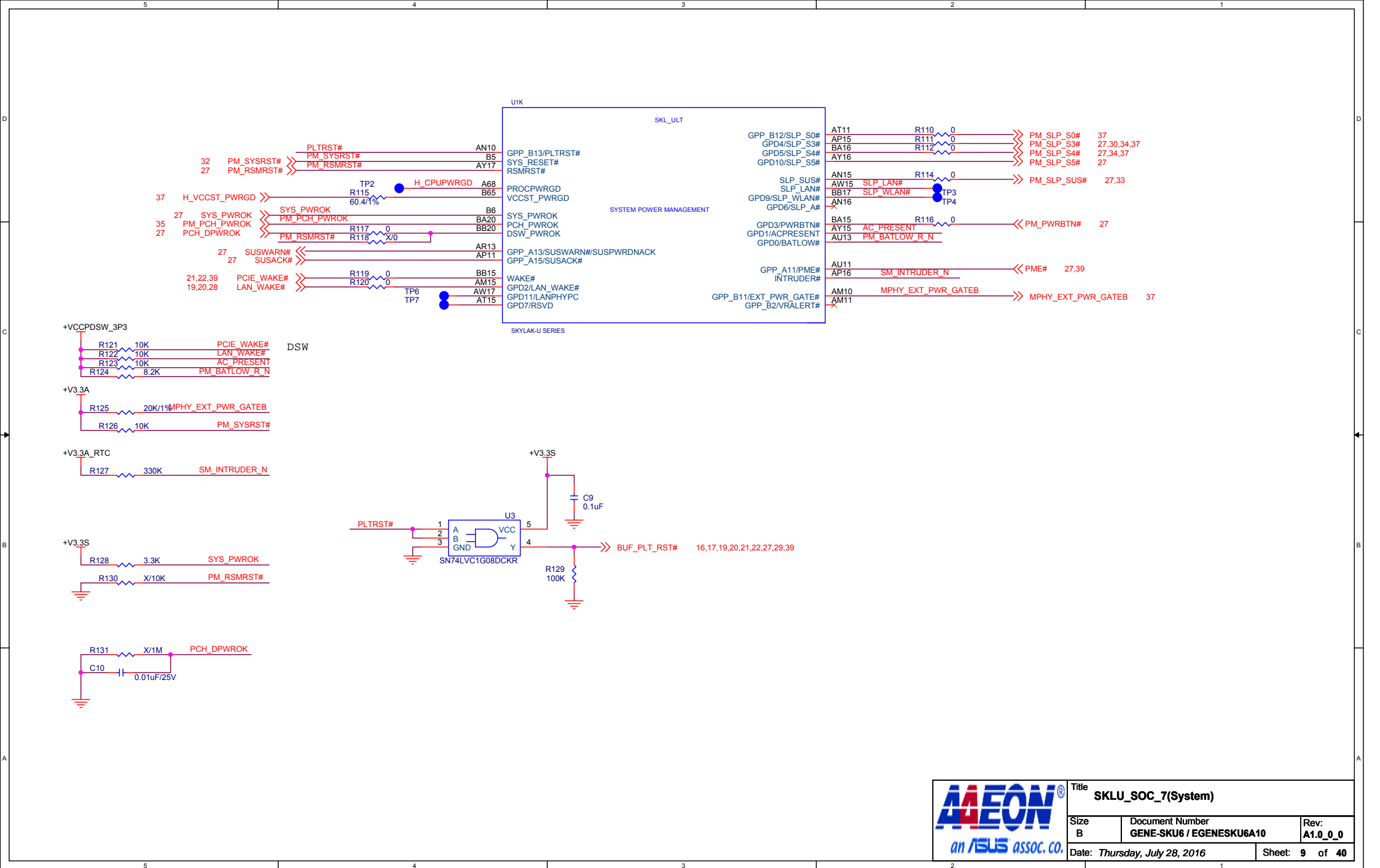






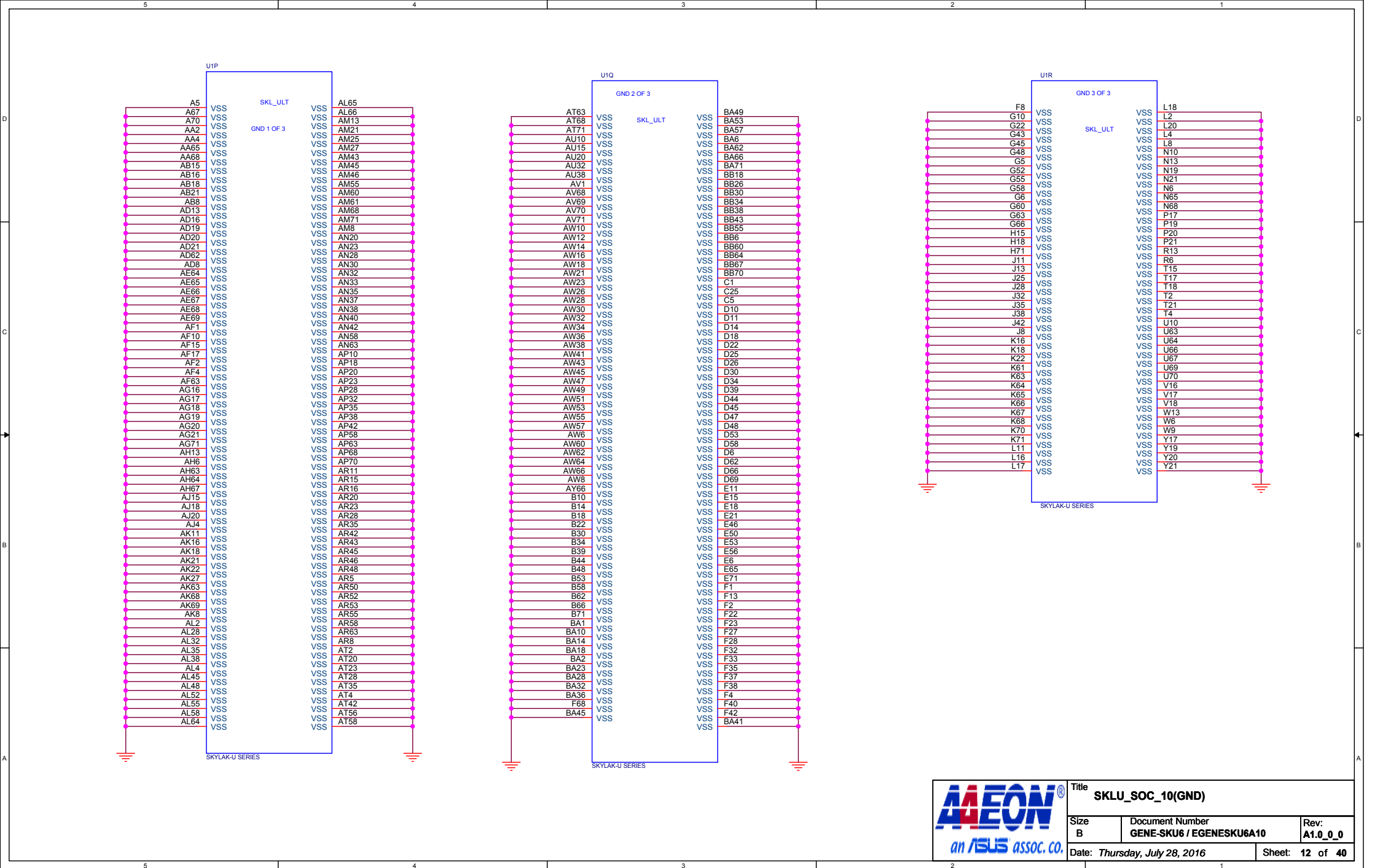
Title <b>SKLU_SOC_6(eMMC)</b>		
Size A	Document Number <b>GENE-SKU6 / EGENESKU6A10</b>	Rev: <b>A1.0_0_0</b>
Date: <i>Thursday, July 28, 2016</i>		Sheet: <b>8</b> of <b>40</b>



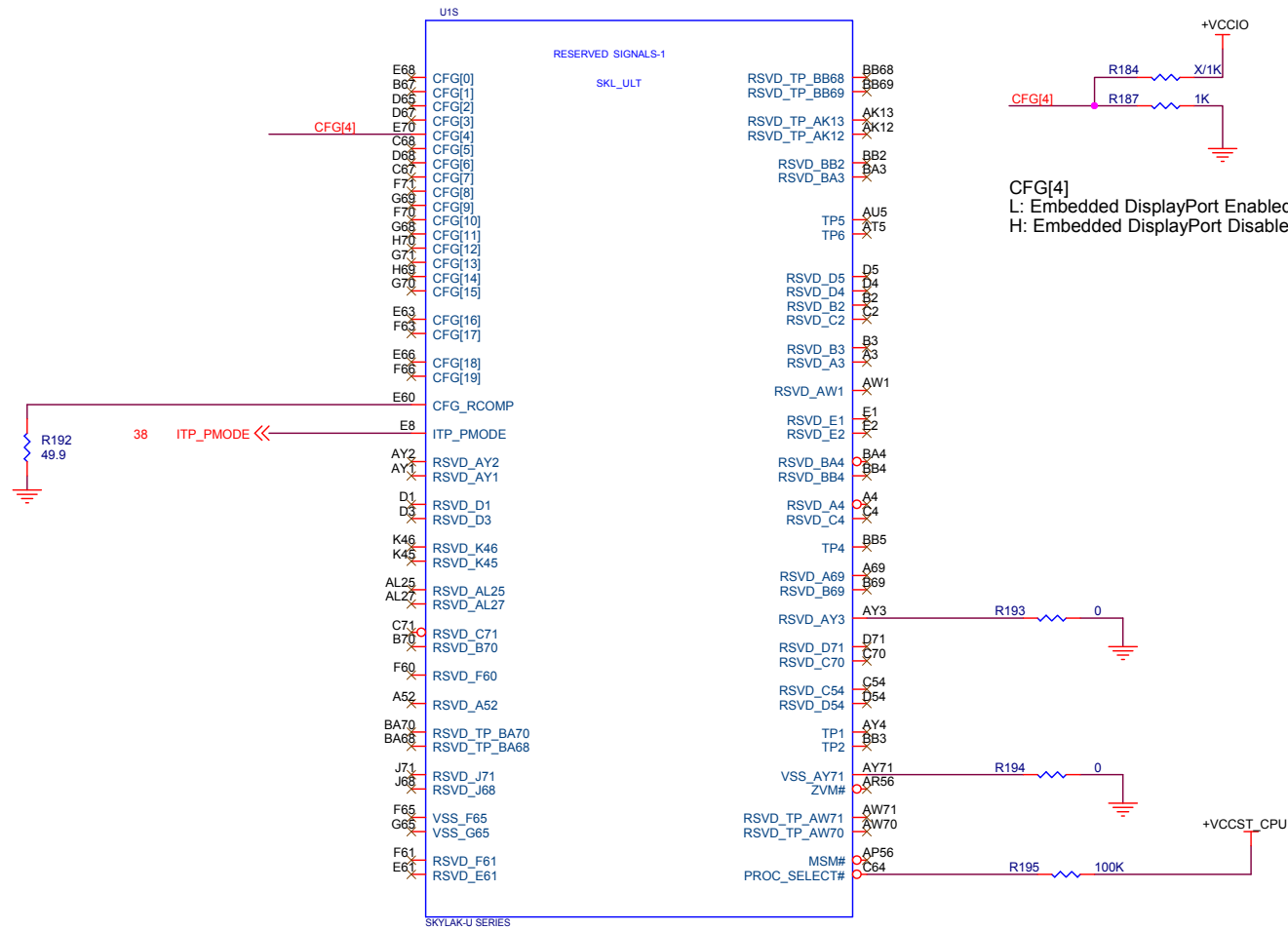




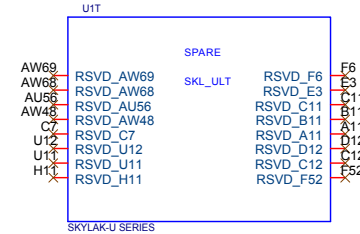




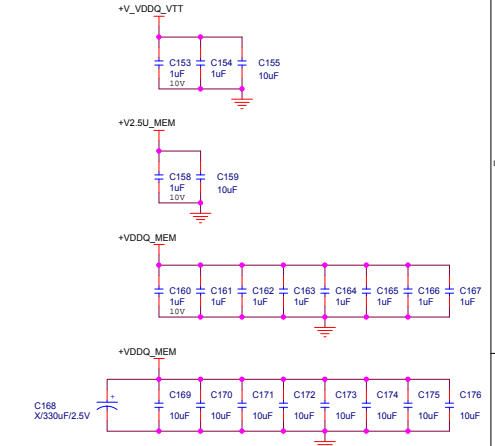
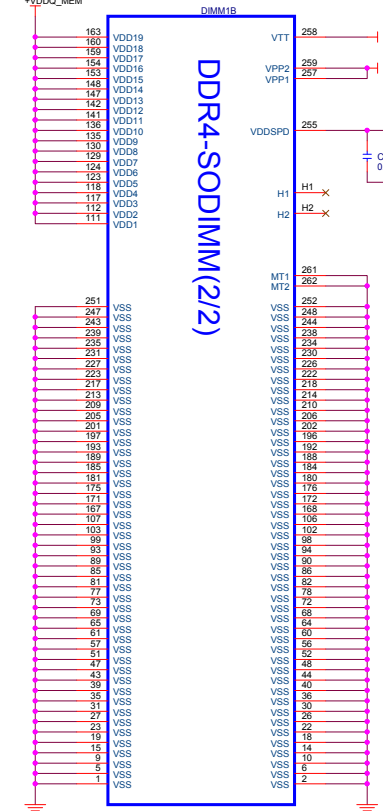
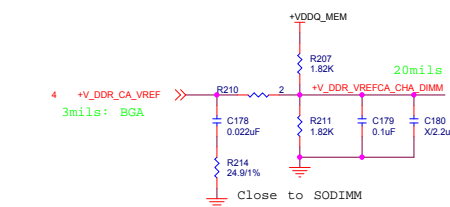
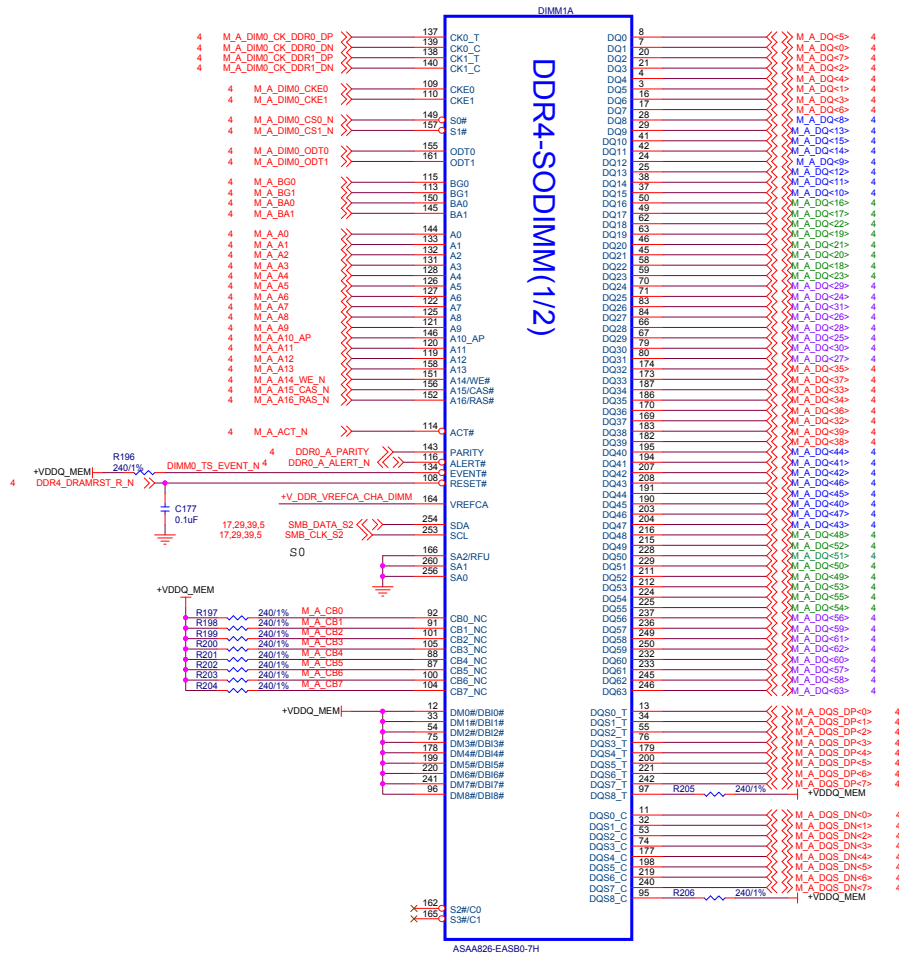
Title SKLU_SOC_10(GND)		
Size B	Document Number	
	GENE-SKU6 / EGENESKU6A10	
Date: Thursday, July 28, 2016		Rev: A1.0_0_0
Sheet: 12 of 40		

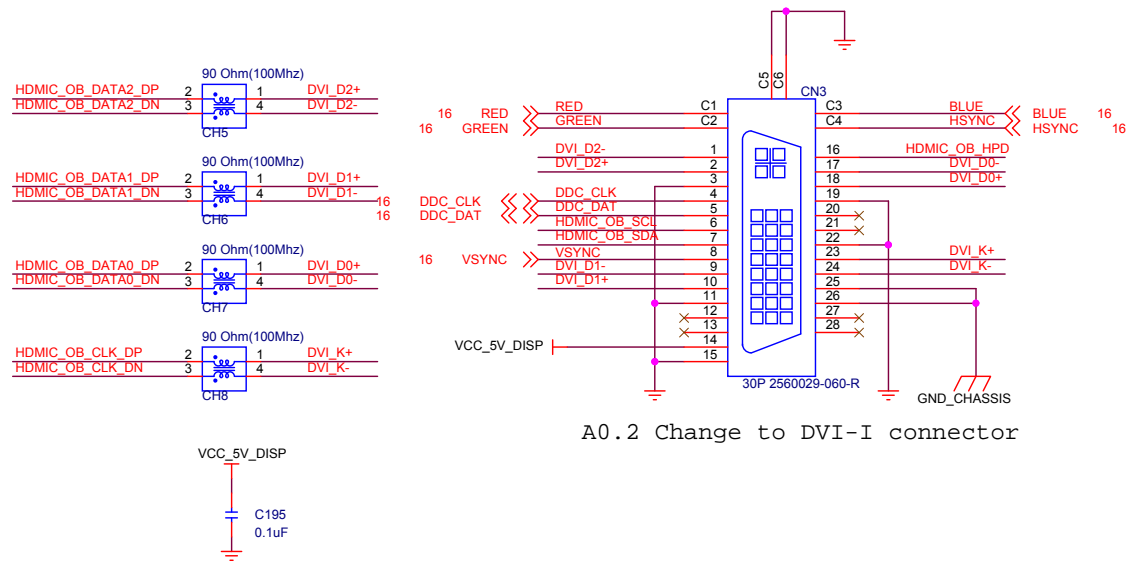
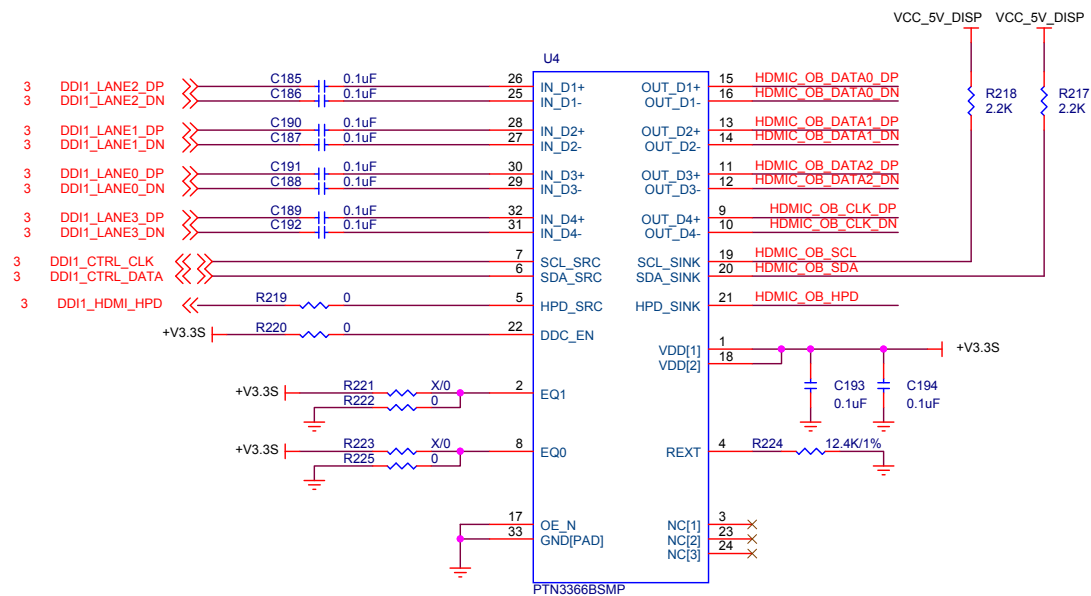


CFG[4]  
 L: Embedded DisplayPort Enabled  
 H: Embedded DisplayPort Disabled



DDR4 SODIMM





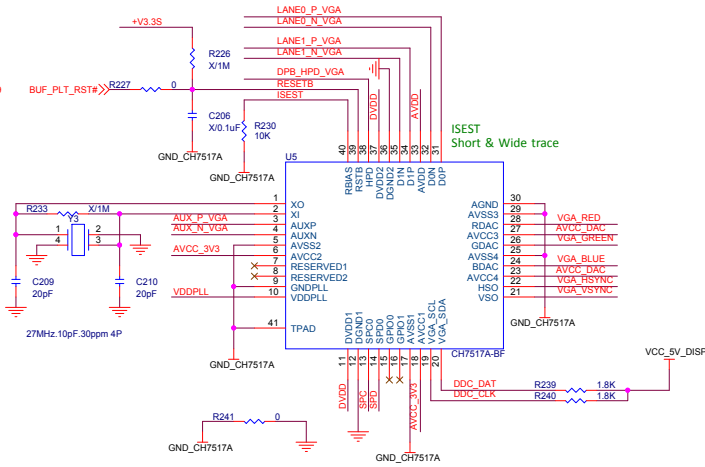
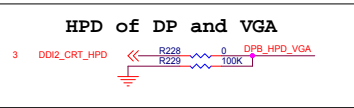
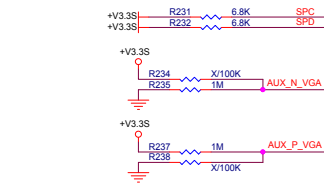
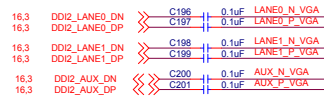
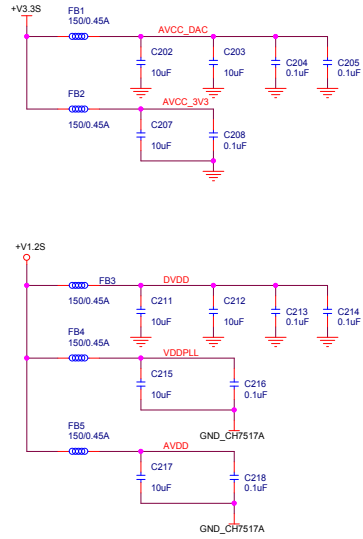
A0.2 Change to DVI-I connector



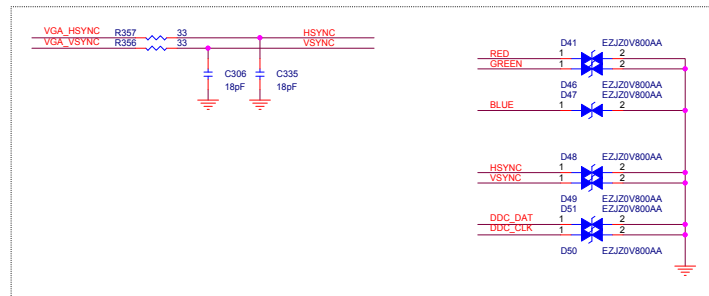
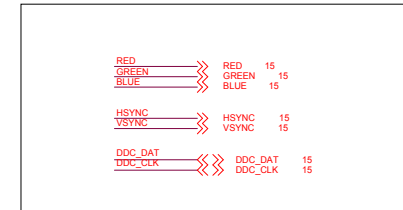
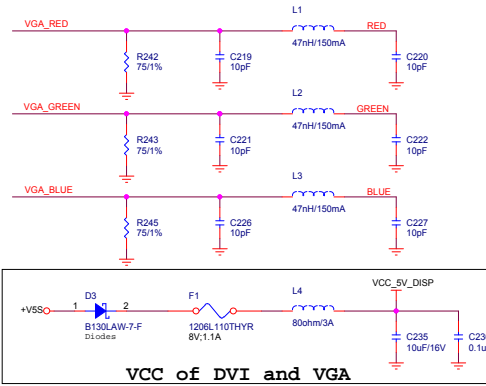
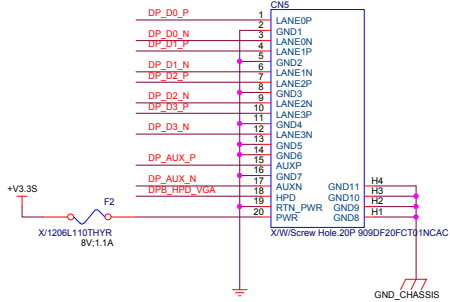
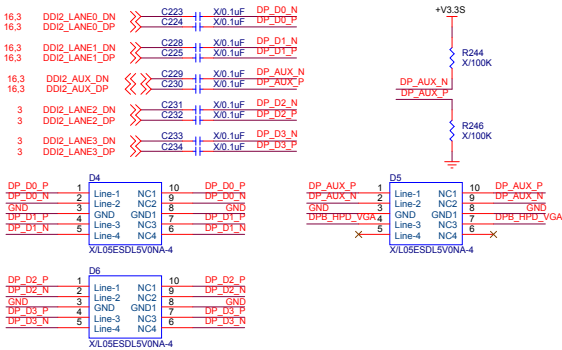
Title <b>HDMI</b>		
Size B	Document Number <b>GENE-SKU6 / EGENESKU6A10</b>	Rev: <b>A1.0_0_0</b>
Date: Thursday, July 28, 2016		Sheet: 15 of 40



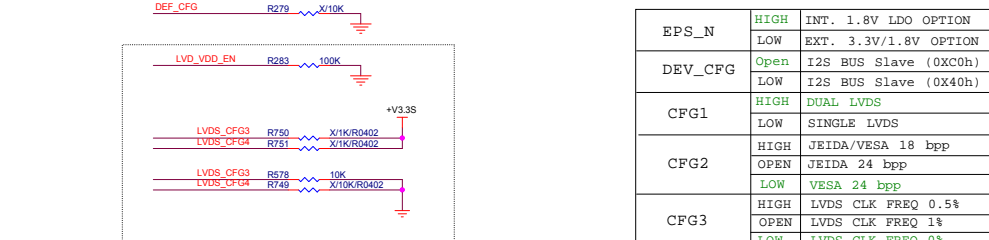
Note:  
 1. VDD12 (DVDD, AVDD, VDDPLL): +1V +1.2V +1.32V (113mA)  
 2. VDD33 (AVCC): +2.97V +3.3V +3.63V (78mA)



## Display Port

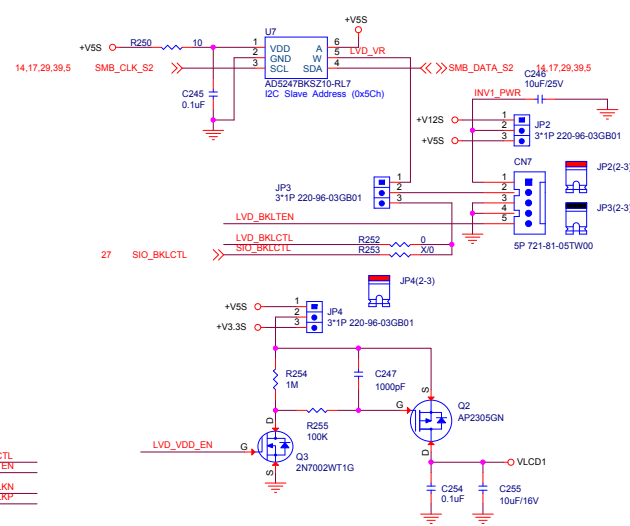
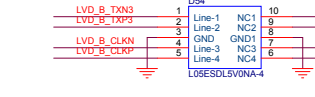
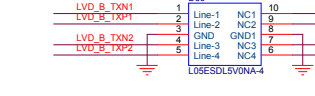
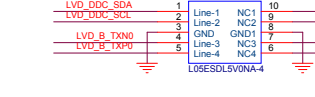
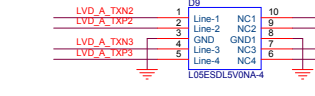
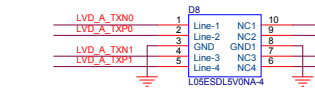
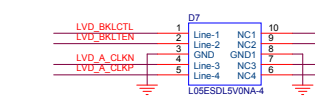
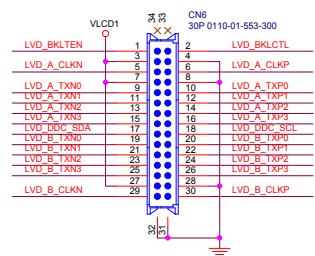


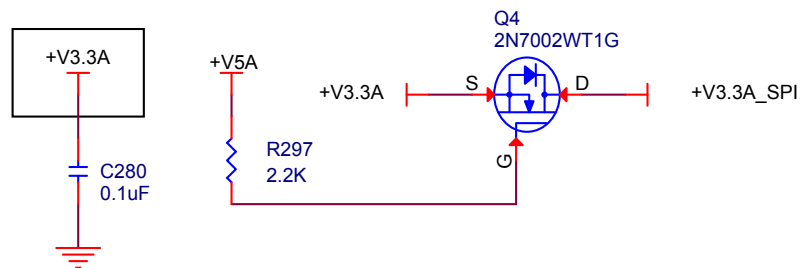
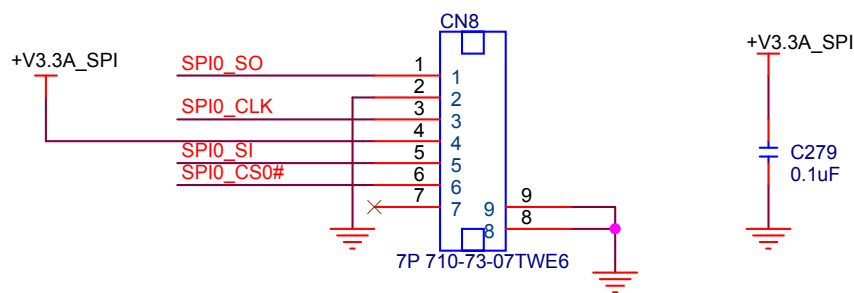
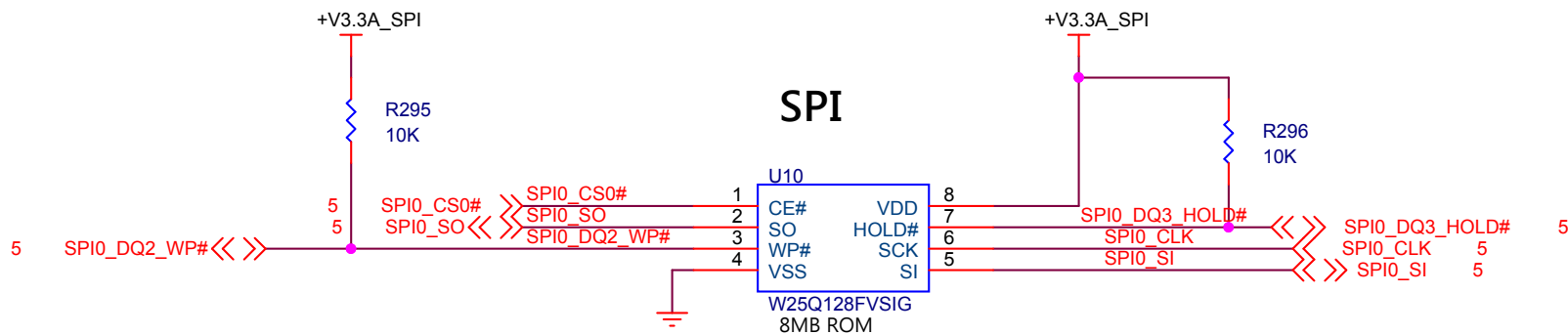
Change to ESD Diode



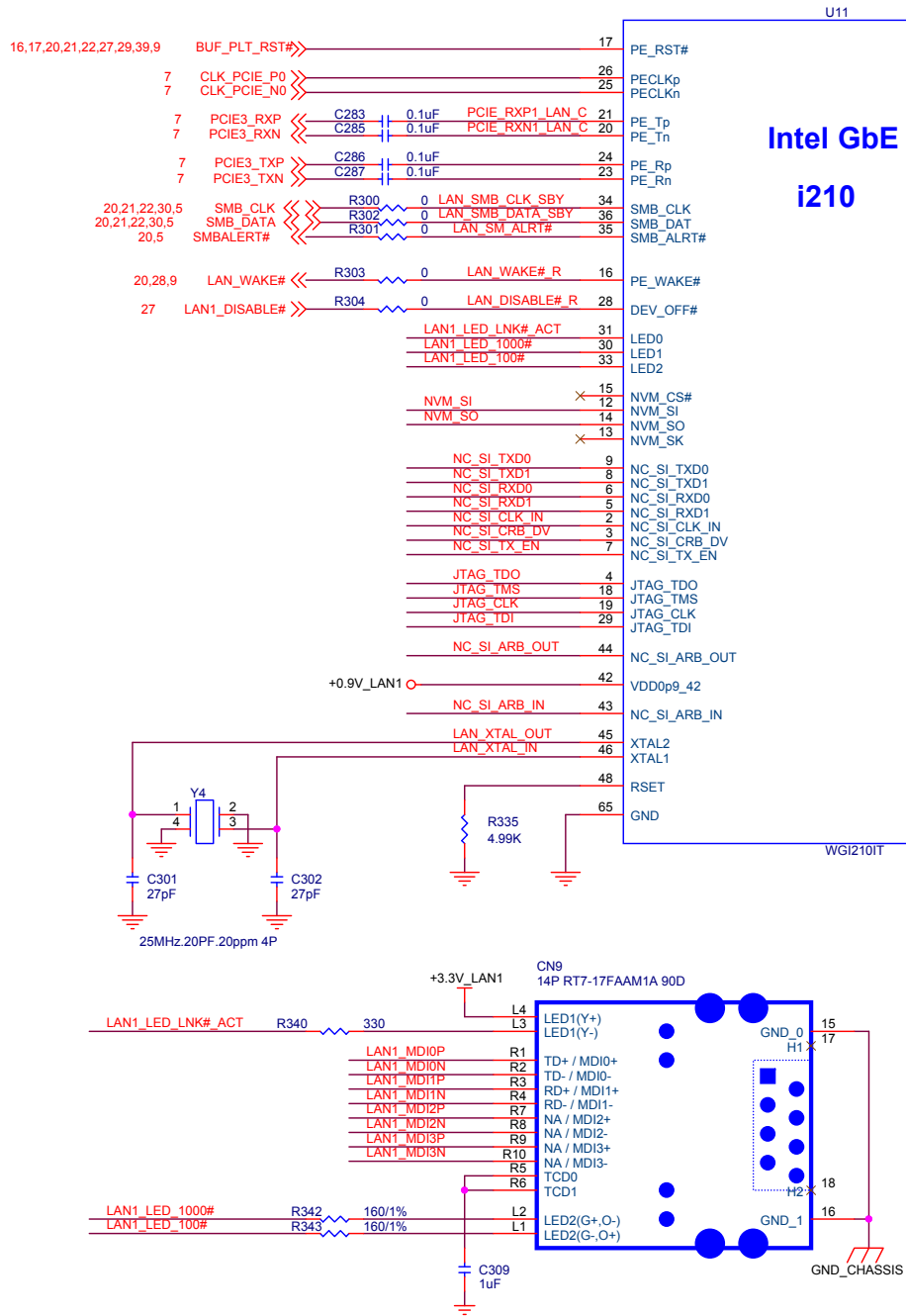
EPS_N	HIGH	INT. 1.8V LDO OPTION
	LOW	EXT. 3.3V/1.8V OPTION
DEV_CFG	Open	I2S BUS Slave (0XC0h)
	LOW	I2S BUS Slave (0X40h)
CFG1	HIGH	DUAL LVDS
	LOW	SINGLE LVDS
CFG2	HIGH	JEIDA/VEESA 18 bpp
	OPEN	JEIDA 24 bpp
CFG3	LOW	VEESA 24 bpp
	HIGH	LVDS CLK FREQ 0.5t
	OPEN	LVDS CLK FREQ 1t
	LOW	LVDS CLK FREQ 0t
CFG4	HIGH	SWING 400mV
	OPEN	SWING 300mV
	LOW	SWING 250mV

## A0.2 Chagne to only LVDS

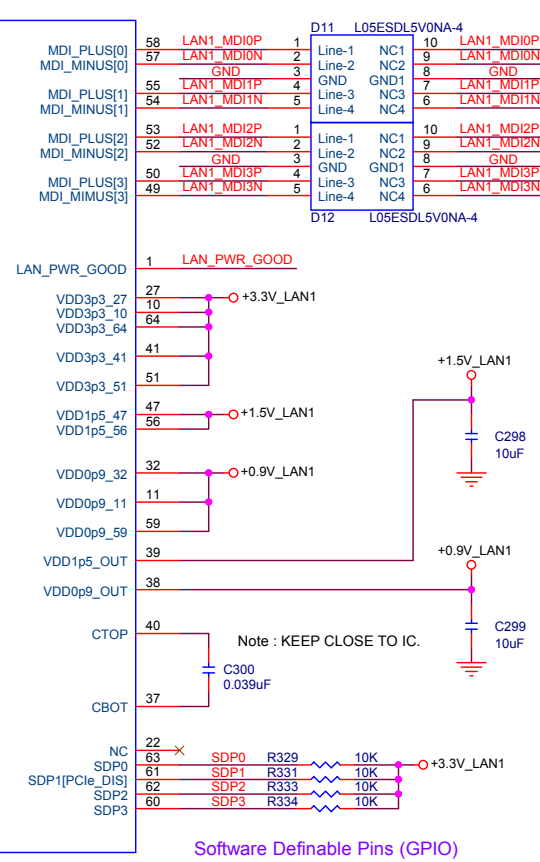




Title <b>BIOS_TPM_LV Shift_LCLK BUFF</b>		
Size A	Document Number <b>GENE-SKU6 / EGENESKU6A10</b>	Rev: <b>A1.0_0_0</b>
Date: <i>Thursday, July 28, 2016</i>		Sheet: <b>18 of 40</b>

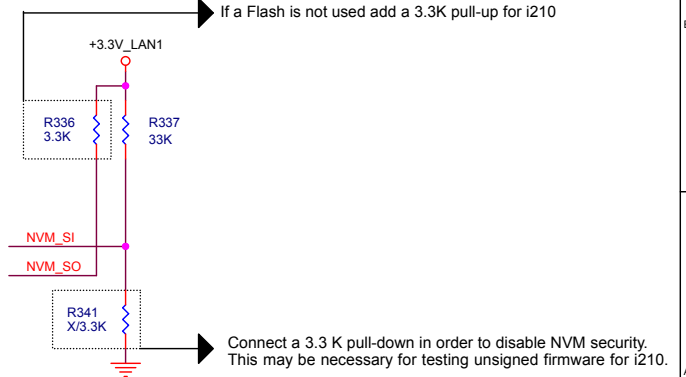
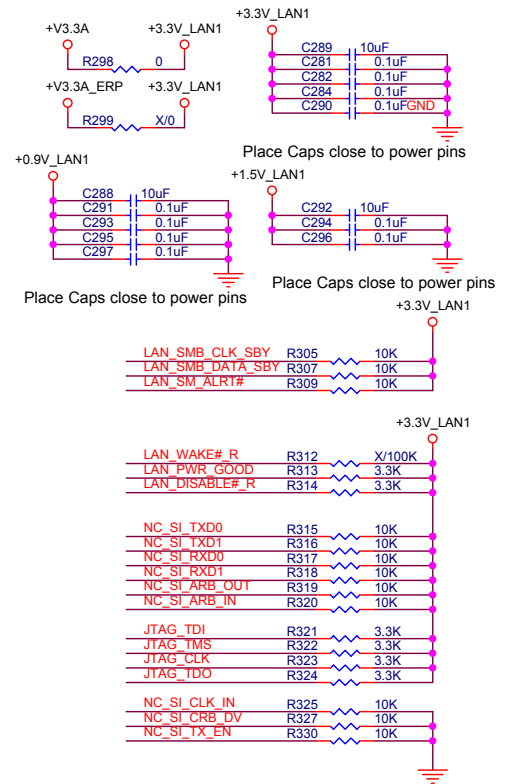


## Intel GbE i210

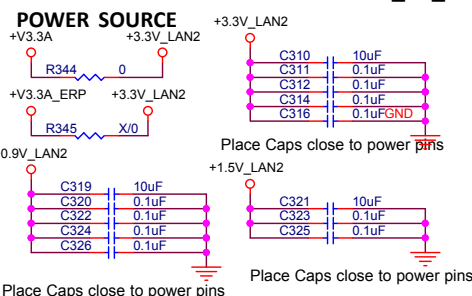


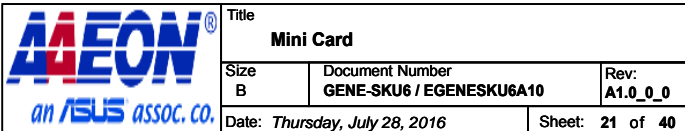
## POWER SOURCE

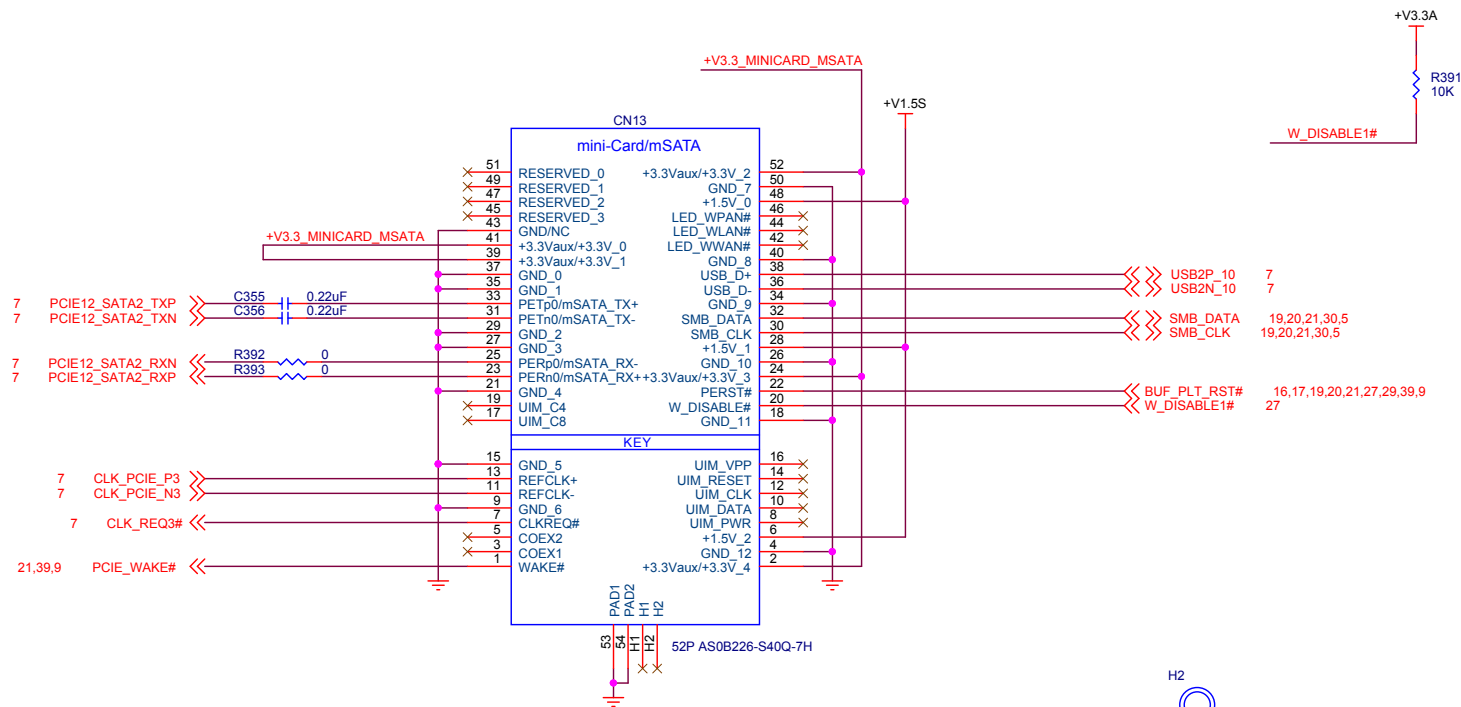
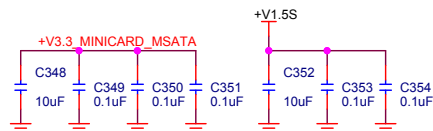
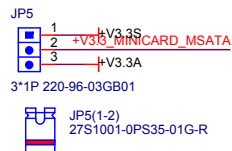
Ver:2014\_08\_28



Title			
Intel LAN i210IT			
Size	Document Number		Rev:
B	GENE-SKU6 / EGENESKU6A10		A1.0_0_0
Date:	Thursday, July 28, 2016		Sheet: 19 of 40

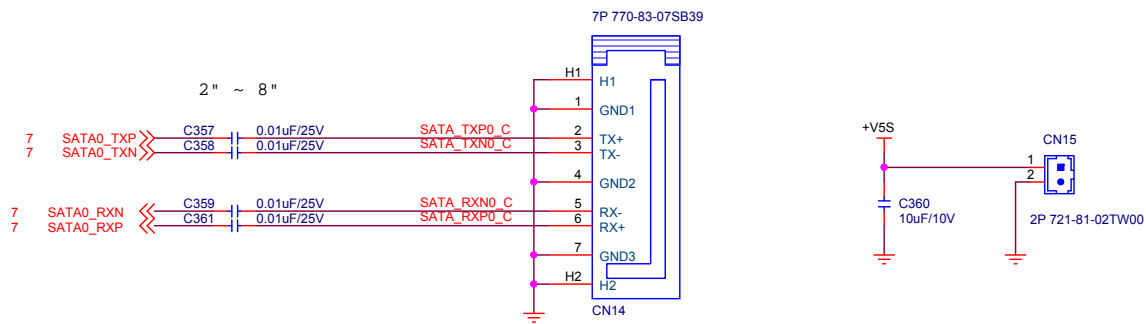




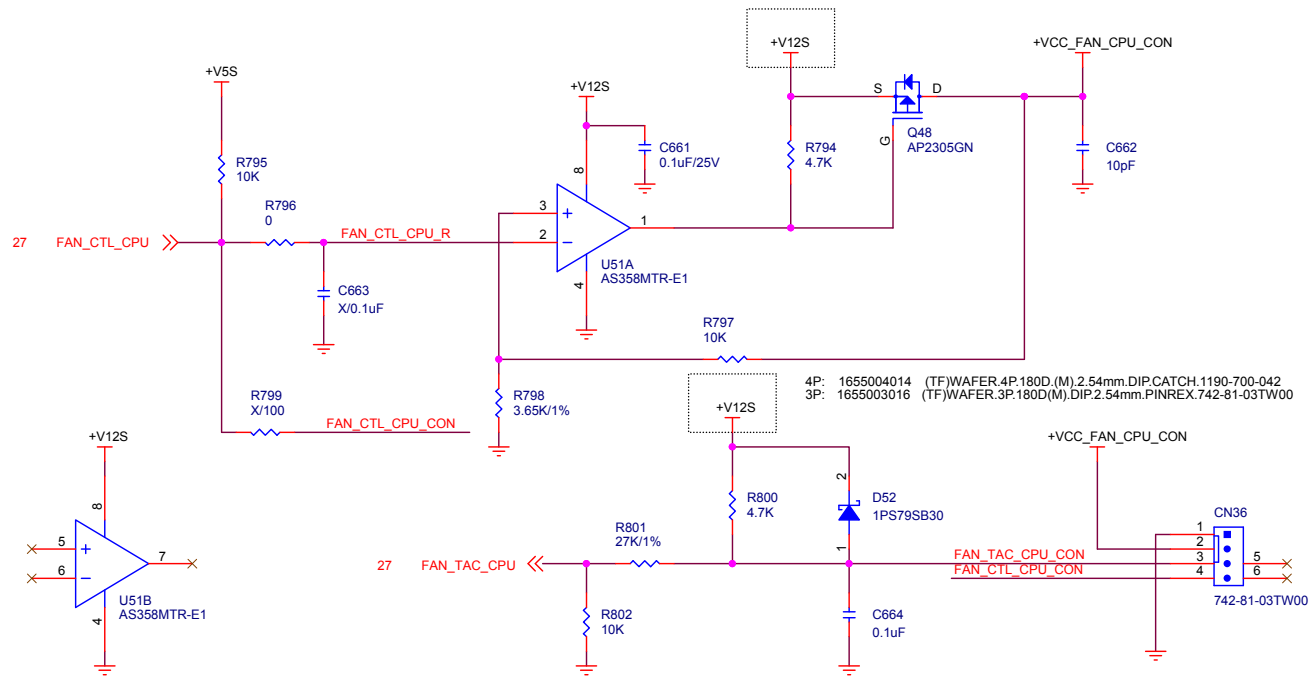


Title <b>mSATA</b>		
Size B	Document Number <b>GENE-SKU6 / EGENESKU6A10</b>	Rev: <b>A1.0_0_0</b>
Date: Thursday, July 28, 2016		Sheet: 22 of 40



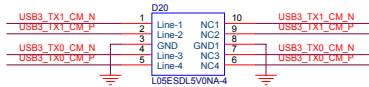
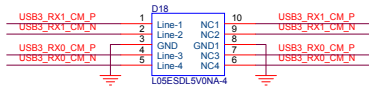
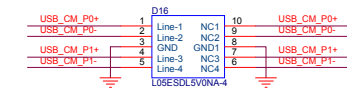
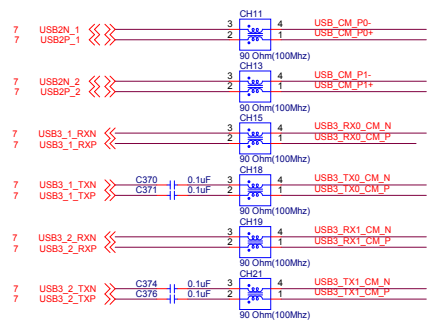
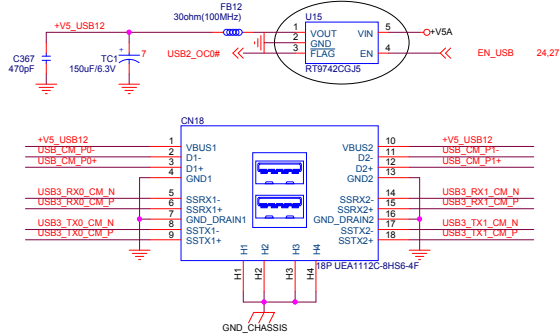


## CPU FAN

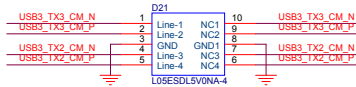
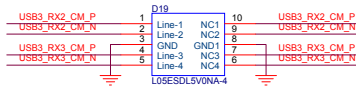
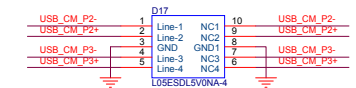
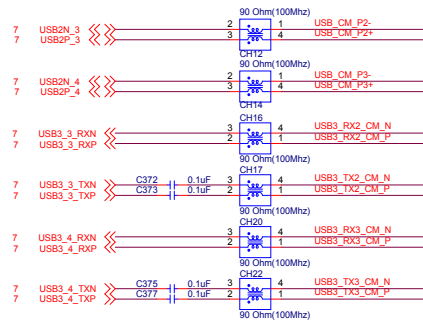
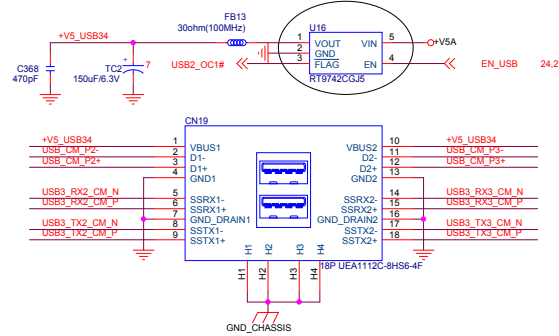


Title <b>SATA, FAN</b>		
Size B	Document Number <b>GENE-SKU6 / EGENESKU6A10</b>	Rev: <b>A1.0_0_0</b>
Date: Thursday, July 28, 2016		Sheet: 23 of 40

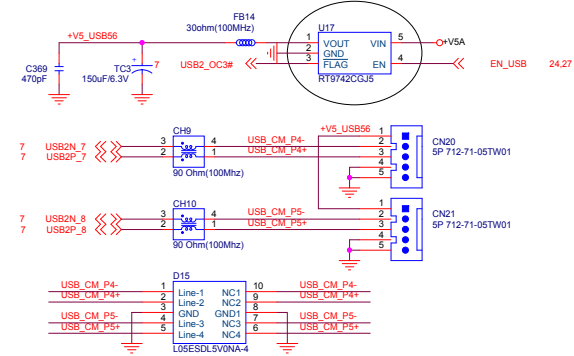
## A0.2 Change to RT9742

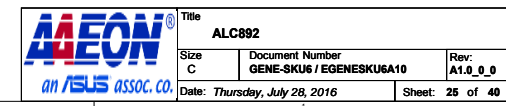


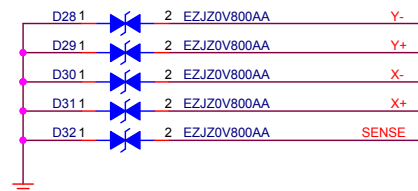
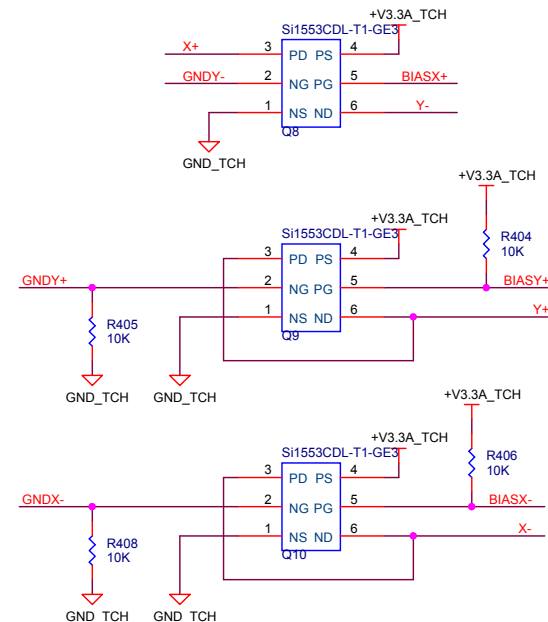
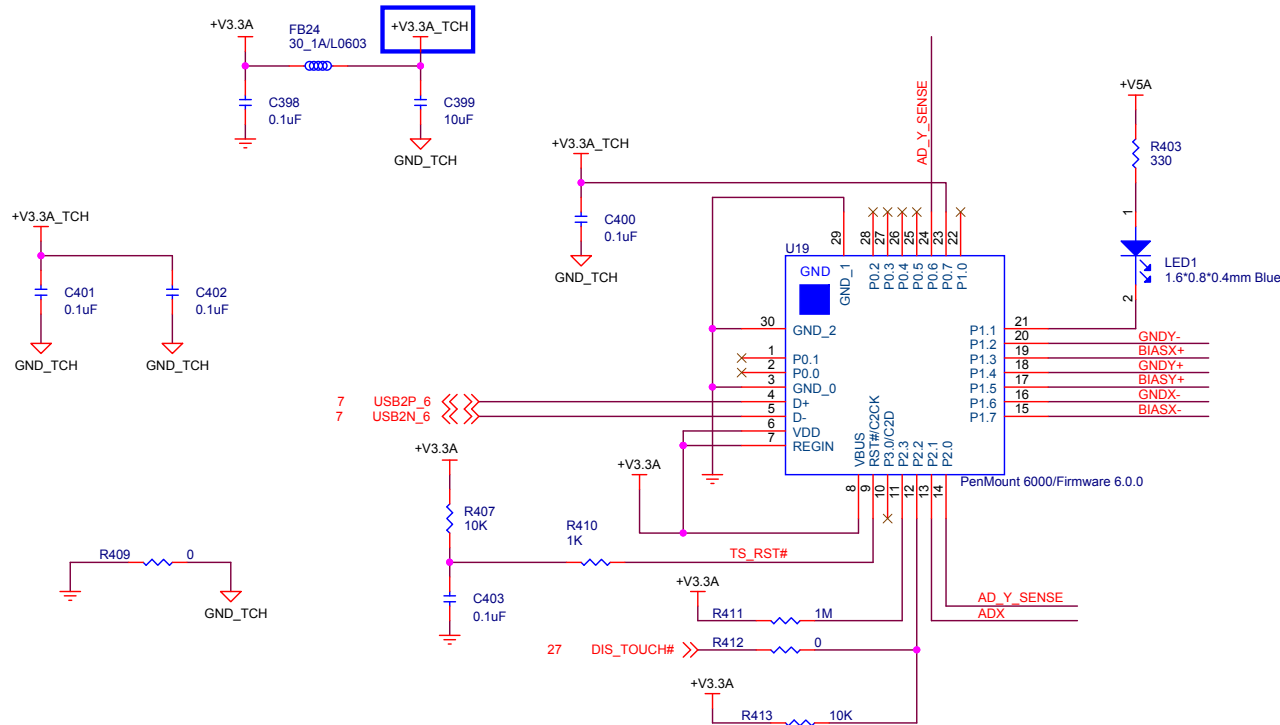
## A0.2 Change to RT9742



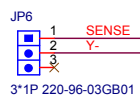
## A0.2 Change to RT9742



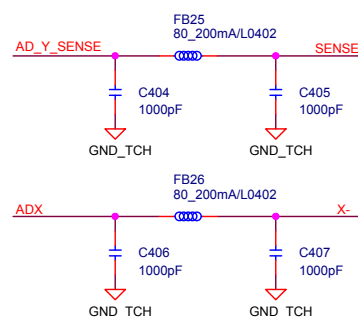




CN	Touch Screen Lines		
	8-Wire	4-Wire	5-Wire
PIN9	Right Sense	N/A	N/A
PIN8	Left Sense	N/A	N/A
PIN7	Bottom Sense	N/A	N/A
PIN6	TOP Sense	N/A	Sense(S)
PIN5	Right Excite	Right	LR(X)
PIN4	Left Excite	Left	LL(L)
PIN3	Bottom Excite	Bottom	UR(H)
PIN2	Top Excite	Top	UL(Y)
PIN1	GND	GND	GND



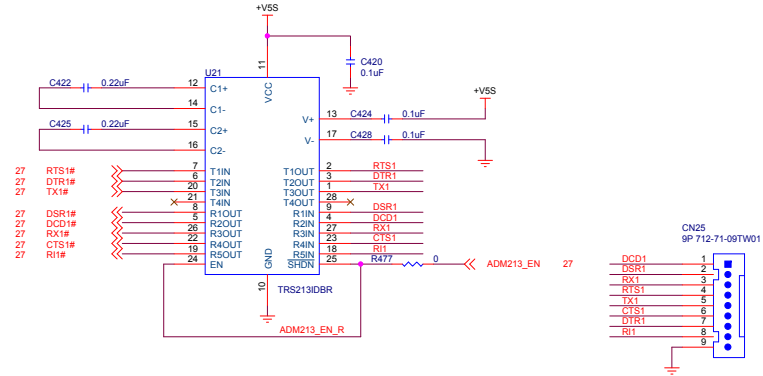
4,5,8 Wire Selection		
1-2	4,8 wire	Default
2-3	5 wire	



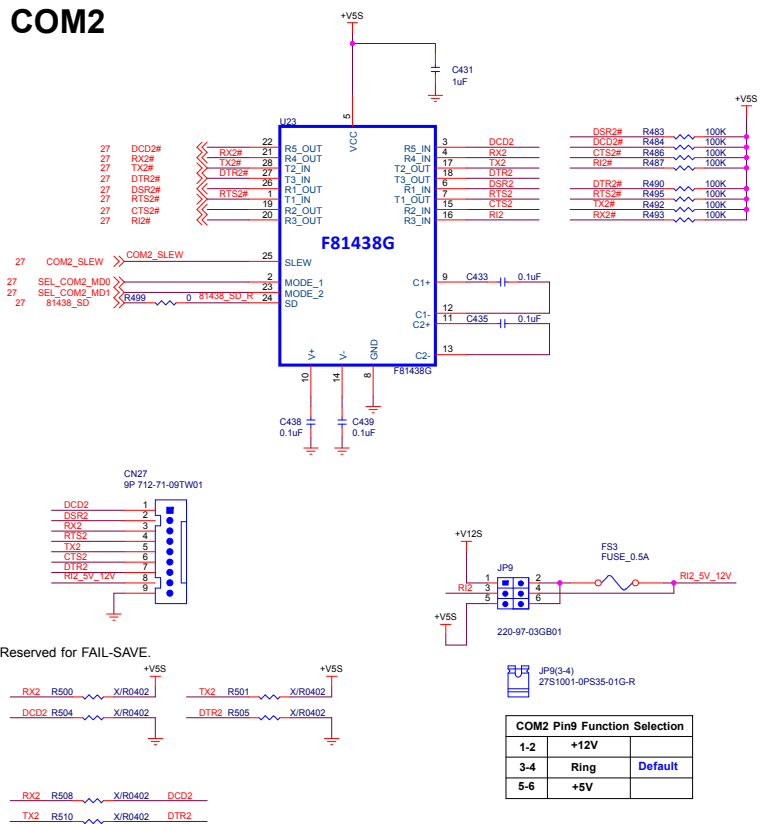
Title		
Touch		
Size B	Document Number GENE-SKU6 / EGENESKU6A10	Rev: A1.0_0_0
Date: Thursday, July 28, 2016	Sheet: 26 of 40	



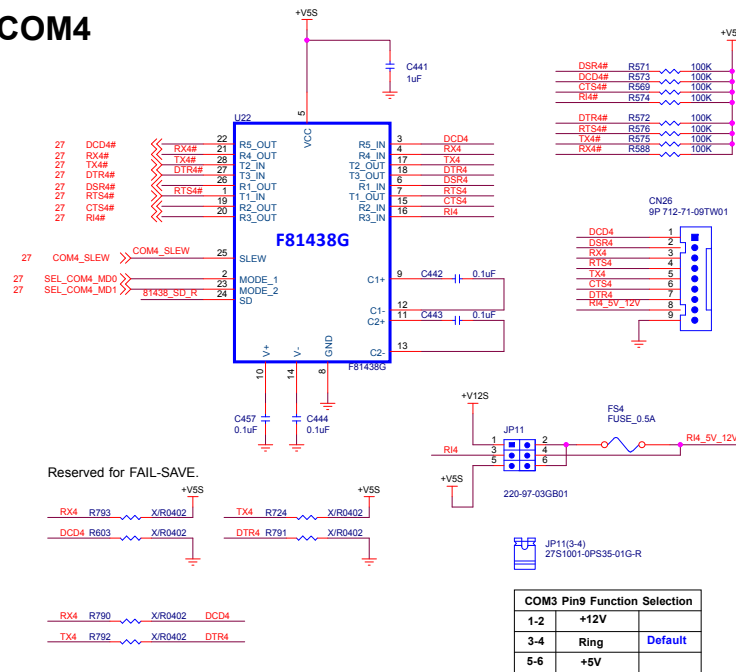
**COM1**



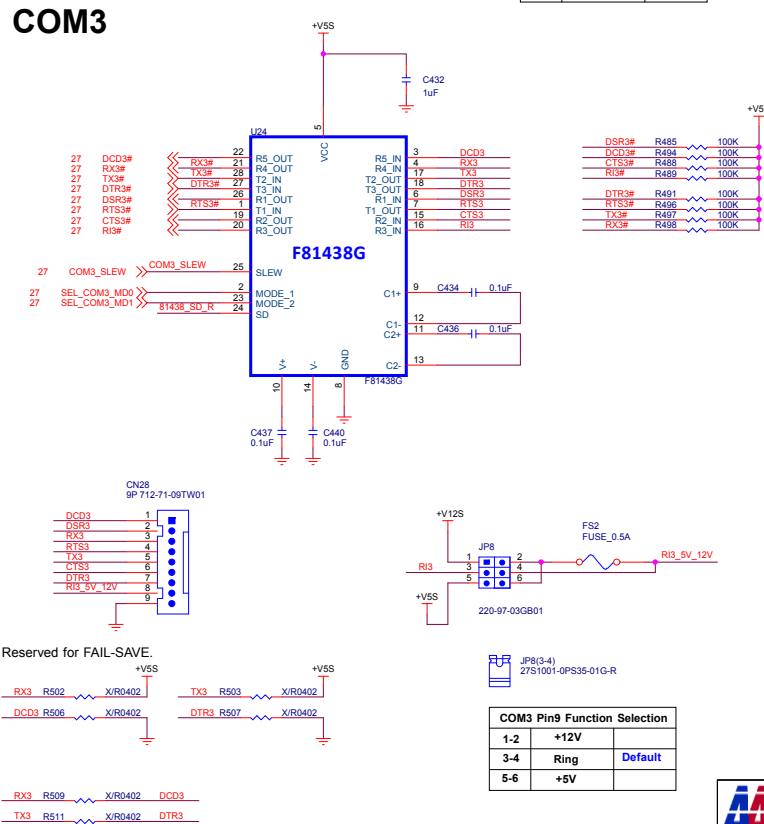
**COM2**



**COM4**



**COM3**



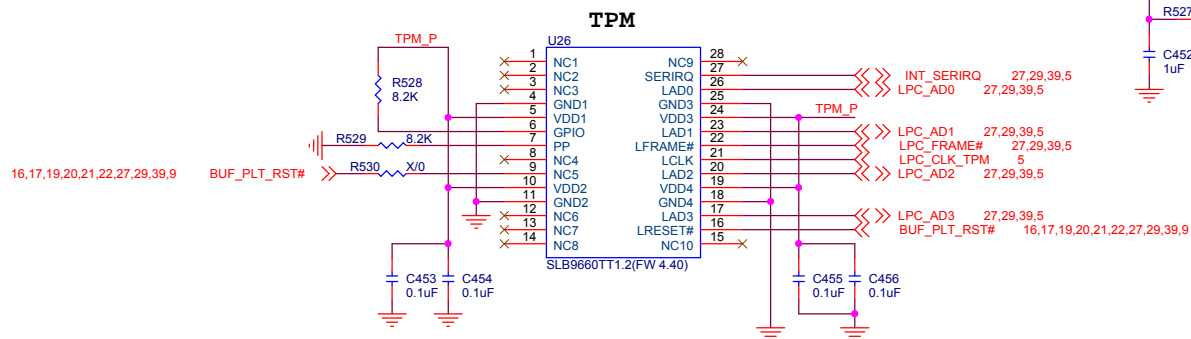
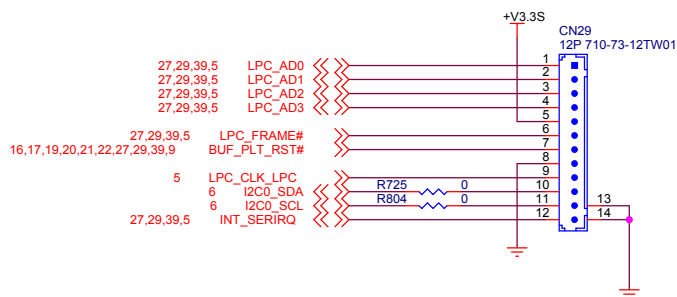
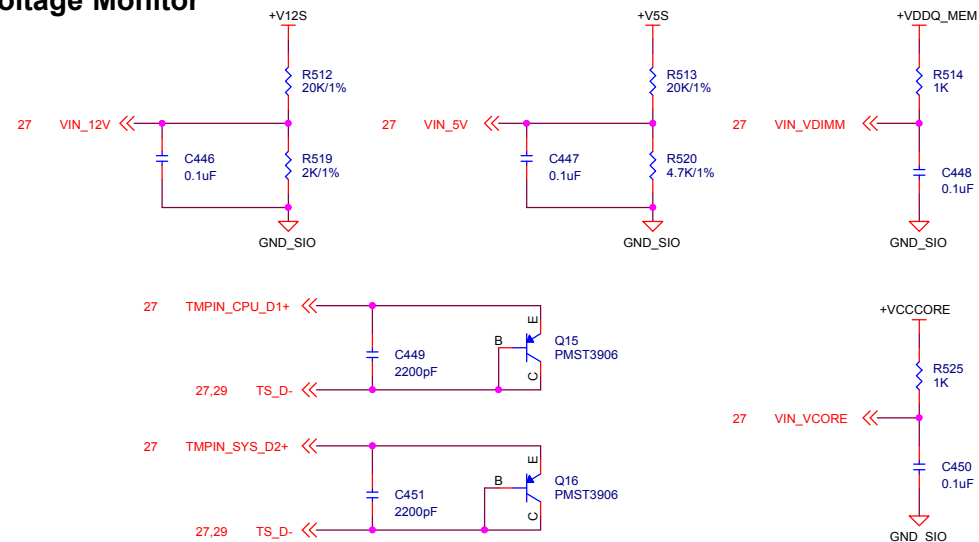
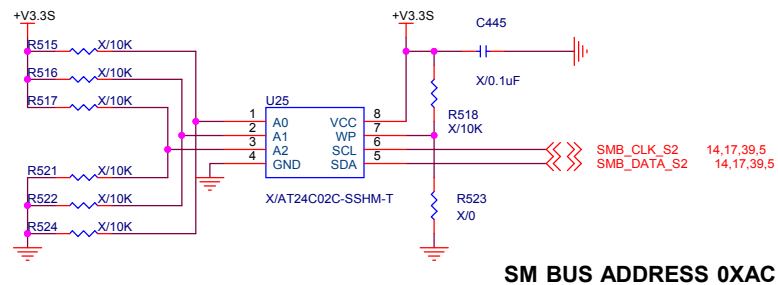
COM3 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

Pin Mapping			
	RS-232	RS-485	RS-422
N	DSR		
UT	RTS		
UT	TX		RS422_RX+ (A)
UT	DTR		RS422_RX- (B)
N	CTS		
N	Ri		
N	RX	RS485_D+ (A)	RS422_TX+ (A)
N	DCD	RS485_D- (B)	RS422_TX- (B)

Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

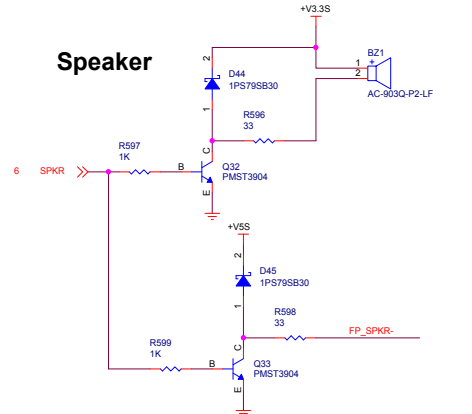
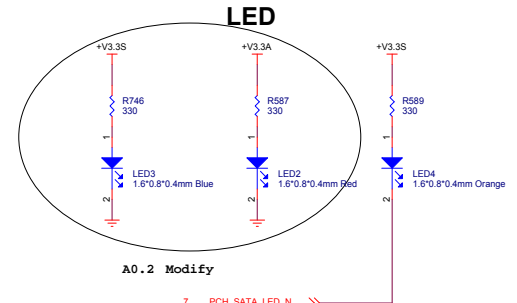
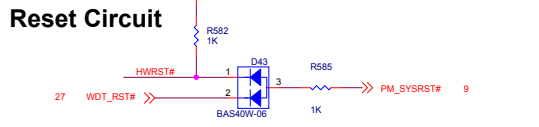
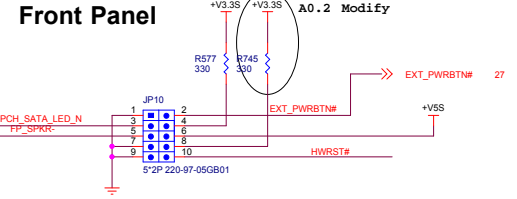
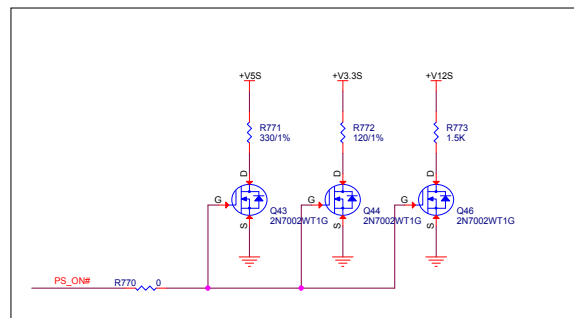
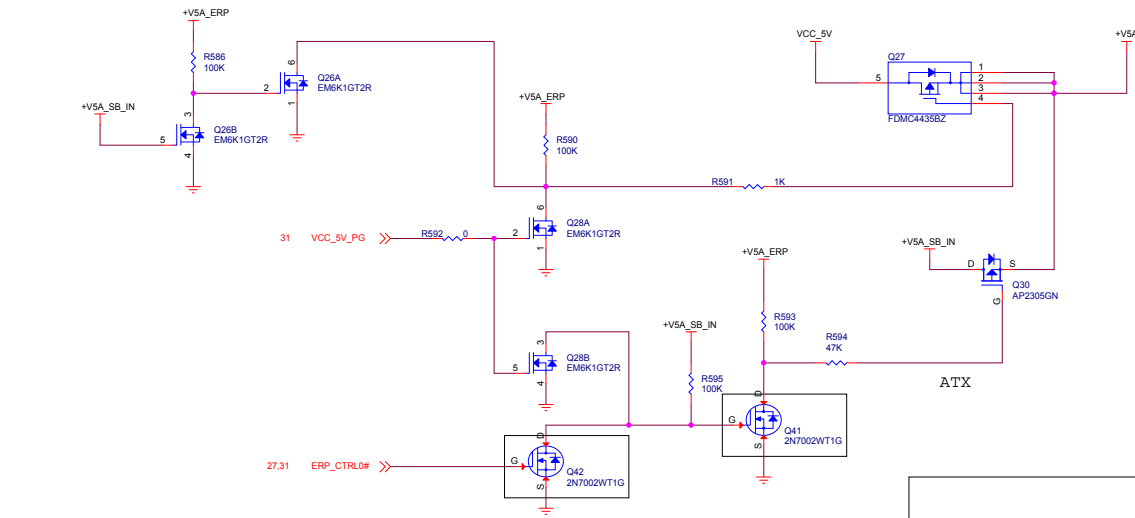
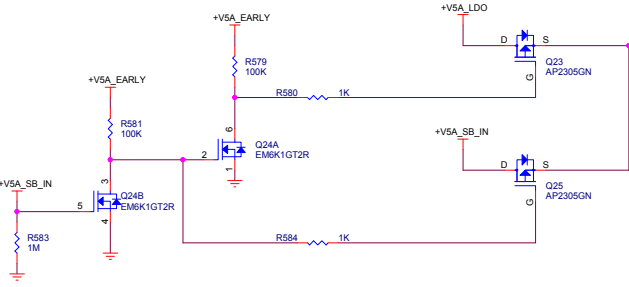
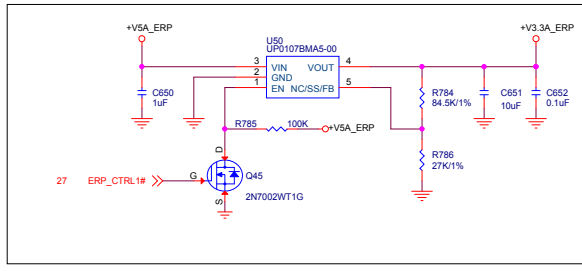
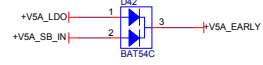
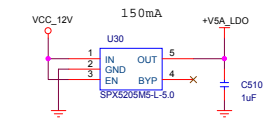
COM3 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	







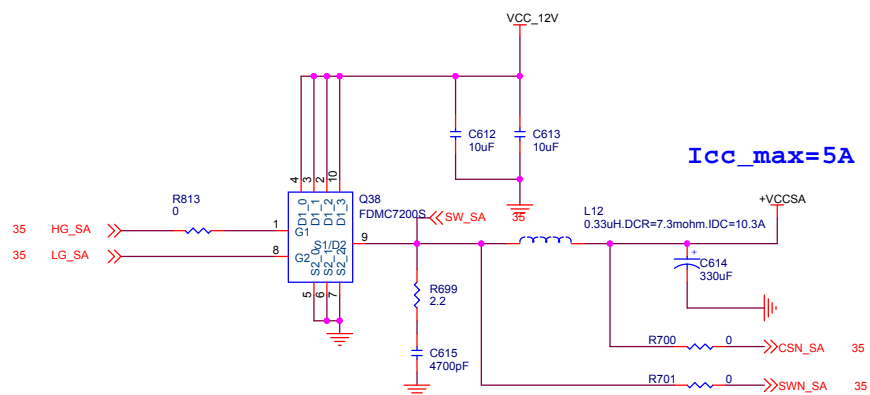
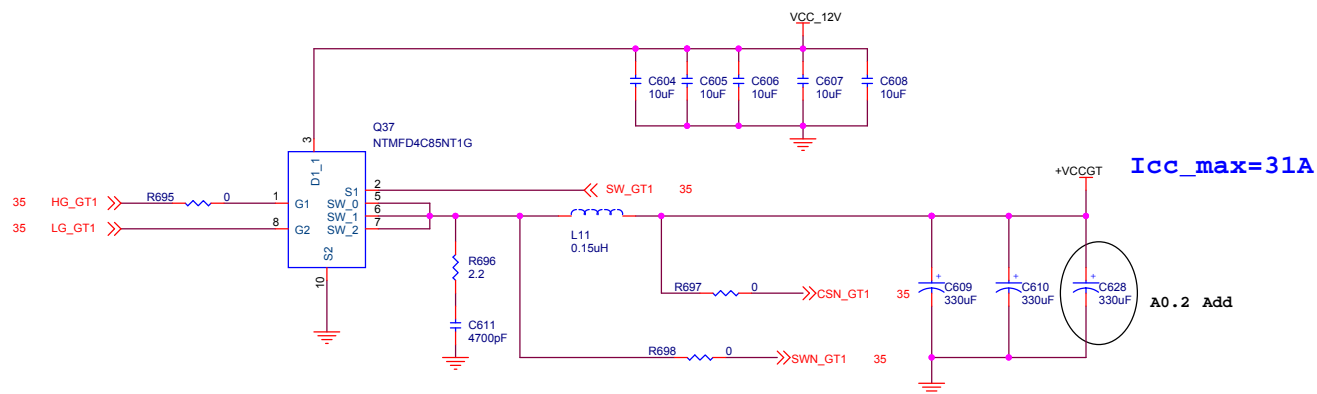
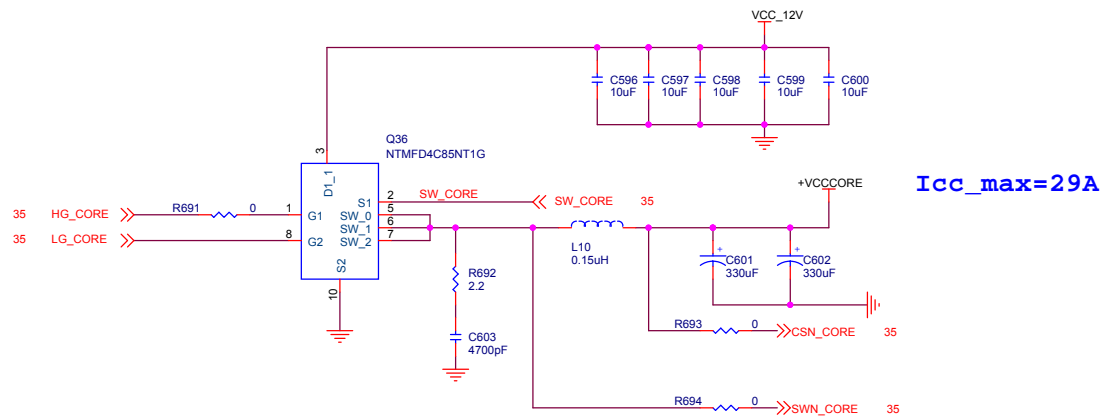








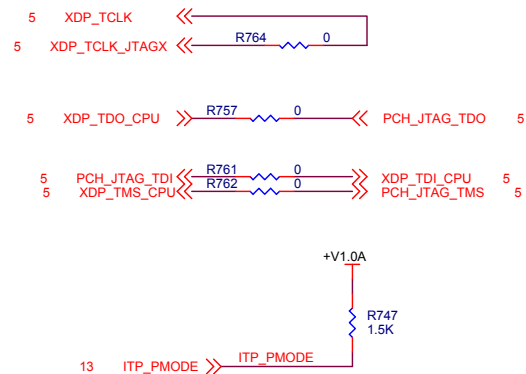




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POWER VR_VccGT_VCCSA		
Size	Document Number	Rev:
Custom	GENE-SKU6 / EGENESKU6A10	A1.0_0_0
Date: Thursday, July 28, 2016		Sheet: 36 of 40





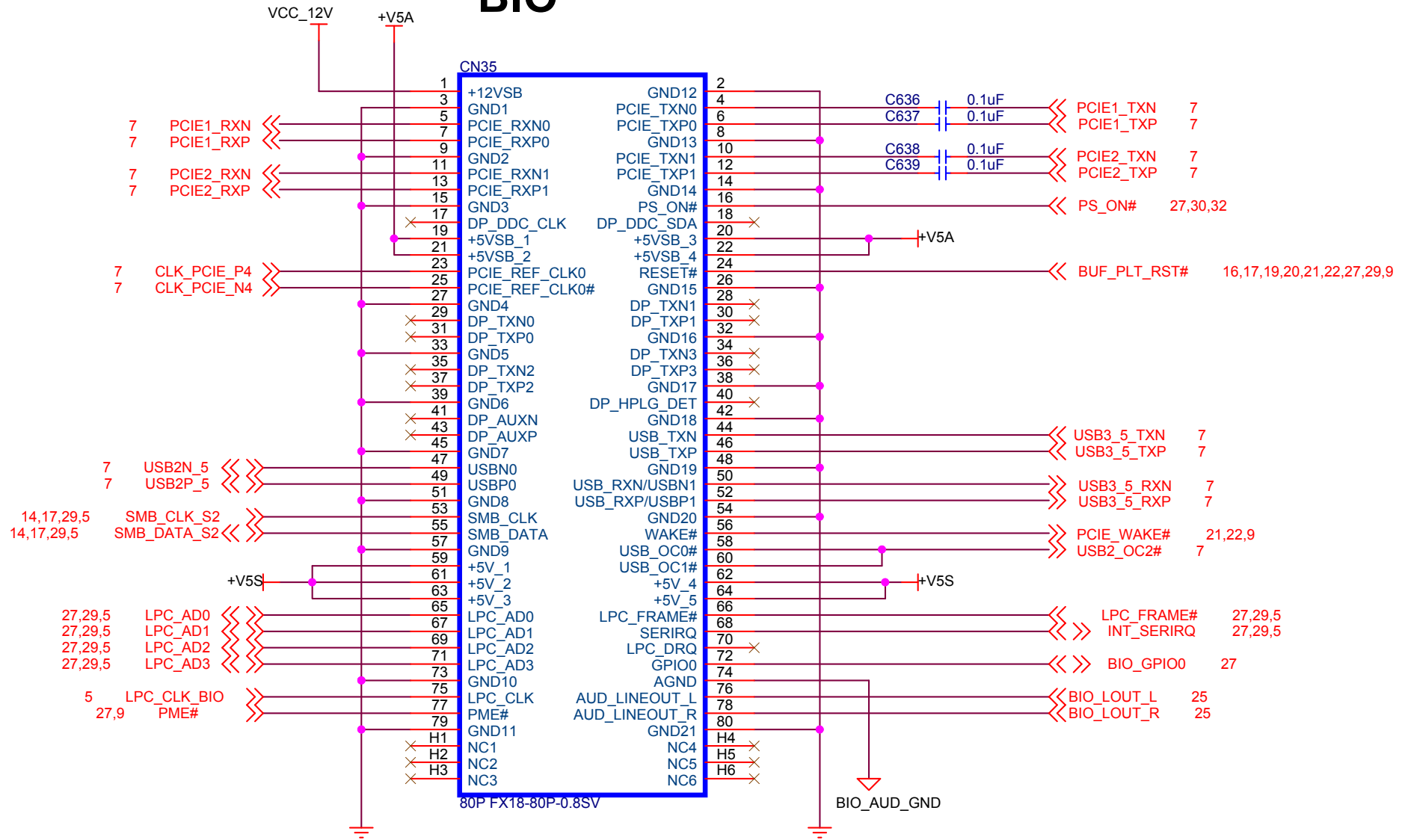


No XDP need keep  
R764, R757, R761, R762, R747



Title XDP		
Size B	Document Number GENE-SKU6 / EGENESKU6A10	Rev: A1.0_0_0
Date: Thursday, July 28, 2016		Sheet: 38 of 40

# BIO



Title <b>BIO</b>		
Size A	Document Number <b>GENE-SKU6 / EGENESKU6A10</b>	Rev: <b>A1.0_0_0</b>
Date: <i>Thursday, July 28, 2016</i>		Sheet: <b>39 of 40</b>

