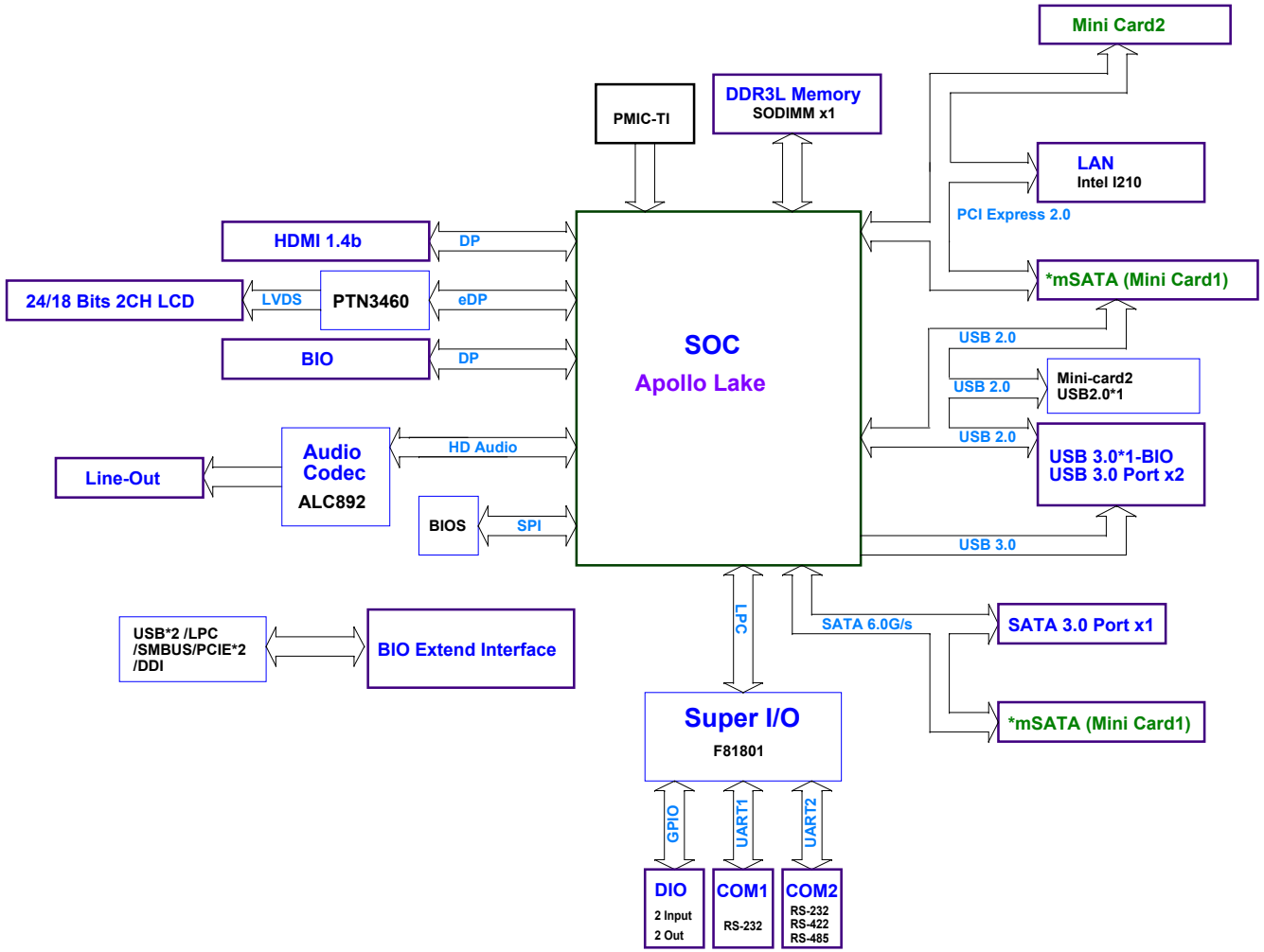
PICO-APL1 Rev.A1.0_0_0

Apollo Lake SoC Platform Cross Compatibility



Project Number : E161107

Production Line : Sub.EPI.AA2M

Title: Cover Sheet			
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SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	
GPIO_1	1.8V	20K PD/I	
GPIO_2	1.8V	20K PD/I	
GPIO_3	1.8V	20K PD/I	
GPIO_4	1.8V	20K PD/I	LVDS_RBIT0
GPIO_5	1.8V	20K PD/I	LVDS_RBIT1
GPIO_6	1.8V	20K PD/I	LVDS_RBIT2
GPIO_7	1.8V	20K PD/I	LVDS_RBIT3
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	WAKE_RI#
GPIO_15	1.8V	20K PD/I	EN_USB
GPIO_16	1.8V	20K PD/I	LAN1_DISABLE#
GPIO_17	1.8V	20K PD/I	W_DISABLE0#
GPIO_18	1.8V	20K PD/I	W_DISABLE1#
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GP[0]
GPIO_23	1.8V	20K PD/I	SATA_GP[1]
GPIO_24	1.8V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	1.8V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/IO	
GPIO_217	1.8V	20K PD/IO	
GPIO_218	1.8V	20K PD/IO	
GPIO_219	1.8V	20K PD/IO/OP	

The Mapping Table For Super I/O F81801U GPIOs :

Name	PIN No.	Power	Type	Description & setting
GPIO[6]	42	+3.3V_ALW	I/OOD12t	
GPIO[12]	35	+3.3V	I/OOD12t	WDTRST#
GPIO[15]	36	+3.3V	I/OOD12,st,lv	None
GPIO[16]	37	+3.3V	I/OOD12,st,lv	
GPIO[20]	38	+3.3V	I/OOD12,st,lv	
GPIO[21]	39	+3.3V	I/OOD12t	
GPIO[22]	40	+3.3V	I/OOD12t	
GPIO[23]	41	+3.3V	I/OOD12t	
GPIO[30]	9	+3.3V	I/OOD12t	DCDB#
GPIO[31]	10	+3.3V	I/OOD12t	RIB#
GPIO[32]	11	+3.3V	I/OOD12t	CTSB#
GPIO[33]	13	+3.3V	I/OOD12t	DTRB#
GPIO[34]	14	+3.3V	I/OOD12t	RTSB#
GPIO[35]	15	+3.3V	I/OOD12t	DSRB#
GPIO[36]	16	+3.3V	I/OOD12t	TXB#
GPIO[37]	17	+3.3V	I/OOD12t	RXB#

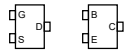
I/OOD12st,lv : Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.

I/OOD12t : TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability

F75111RG GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO10	5V	VSB3V	Native	BOARDID_BIT0
GPIO11	5V	VSB3V	Native	ADM213_EN
GPIO12	5V	VSB3V	Native	81438_SD
GPIO13	5V	VSB3V	Native	
GPIO14	5V	VSB3V	Native	BOARDID_BIT1
GPIO15	5V	VSB3V	Native	
GPIO16	5V	VSB3V	Native	
GPIO17	5V	VSB3V	Native	
GPIO20	5V	VSB3V	Native	SEL_COM2_MD0
GPIO21	5V	VSB3V	Native	SEL_COM2_MD1
GPIO22	5V	VSB3V	Native	COM2_SLEW
GPIO23	5V	VSB3V	Native	BIO-GPIO
GPIO24	5V	VSB3V	Native	DIO_P0
GPIO25	5V	VSB3V	Native	DIO_P1
GPIO26	5V	VSB3V	Native	DIO_P2
GPIO27	5V	VSB3V	Native	DIO_P3
GPIO30	5V	VSB3V	GPIO	LVDS_EN
GPIO31	5V	VSB3V	GPIO	
GPIO32	5V	VSB3V	GPIO	
GPIO33	5V	VSB3V	GPIO	LVDS_PD#

PCB Footprints

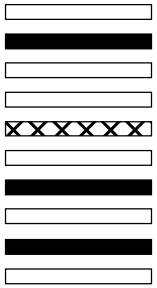


SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
GPIO IC	6Eh
PTN3460 Slave	C0h

PCB STACK :

Impedence 50ohm +/-15%.



- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : GND
- Layer 5 : Signal
- Layer 6 : VCC
- Layer 7 : Signal
- Layer 4 : Signal
- Layer 9 : GND
- Layer 10 : Solder

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Title: **System Settings**

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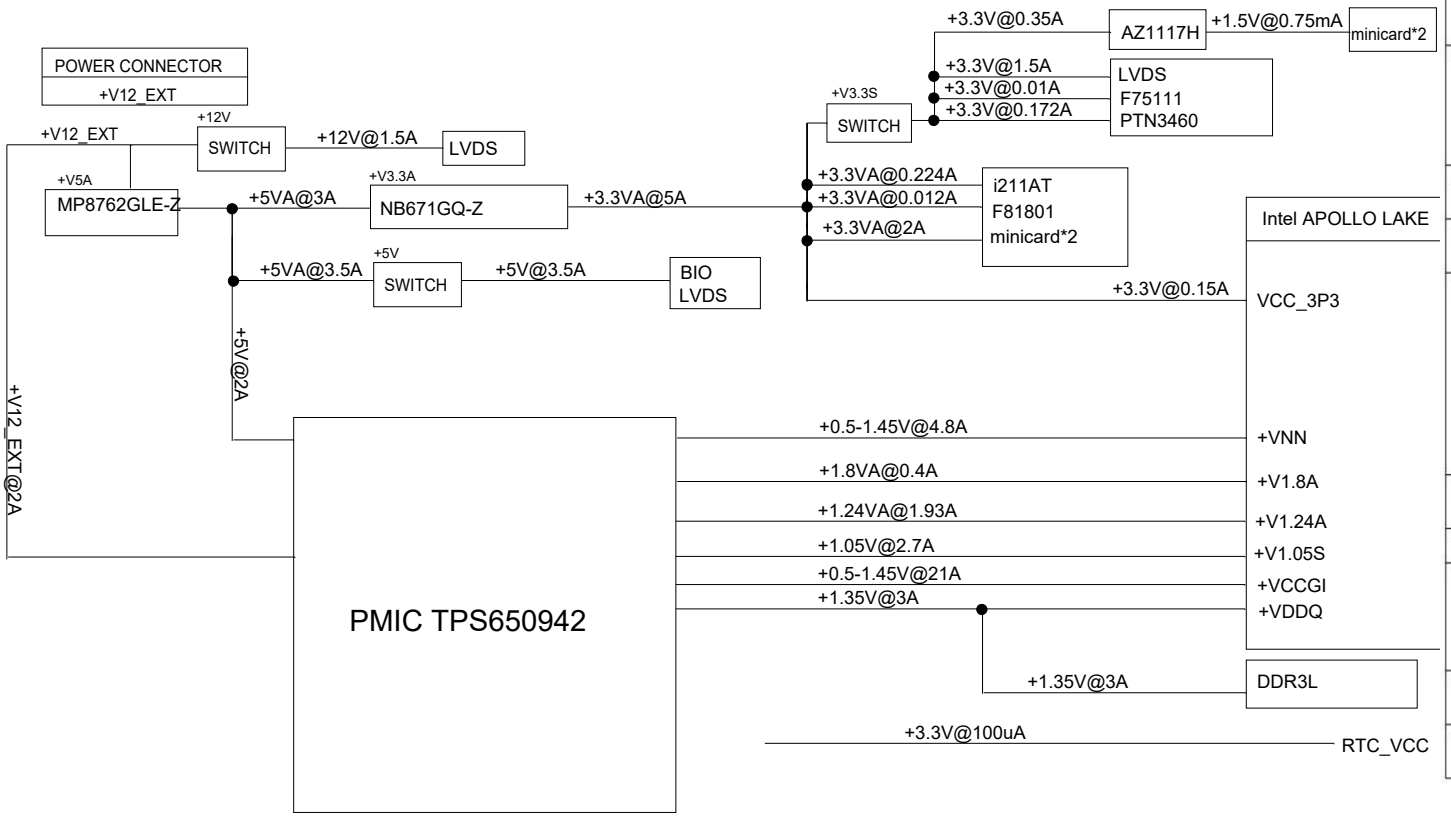

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Iccmax (A)
VCC_VCGI	0.45~1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	21
VNN	0.45~1.3	+/-50mV	4.8
VCC_V1P05	1.05	+/-5%	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	1.3
VCC_V1P24_A	1.24	+/-5%	TBD
VCC_V1P8V_A	1.8	+/-5%	0.4
VDDQ	1.35	+/-5%	2.8 (excluding DRAM)
	1.24	+/-5%	
VCC_3P3V_A	3.3	+/-5%	0.15
VCC_RTC_3P3V	2~3.47	N/A	TBD

+V5A -> +V3.3A -> +VNN -> +VCC -> +V1P8A- > +V1P24A -> +V1P8U -> +VDDQ
+V1.05S -> +VCC_VCGI

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Title: Power Tree

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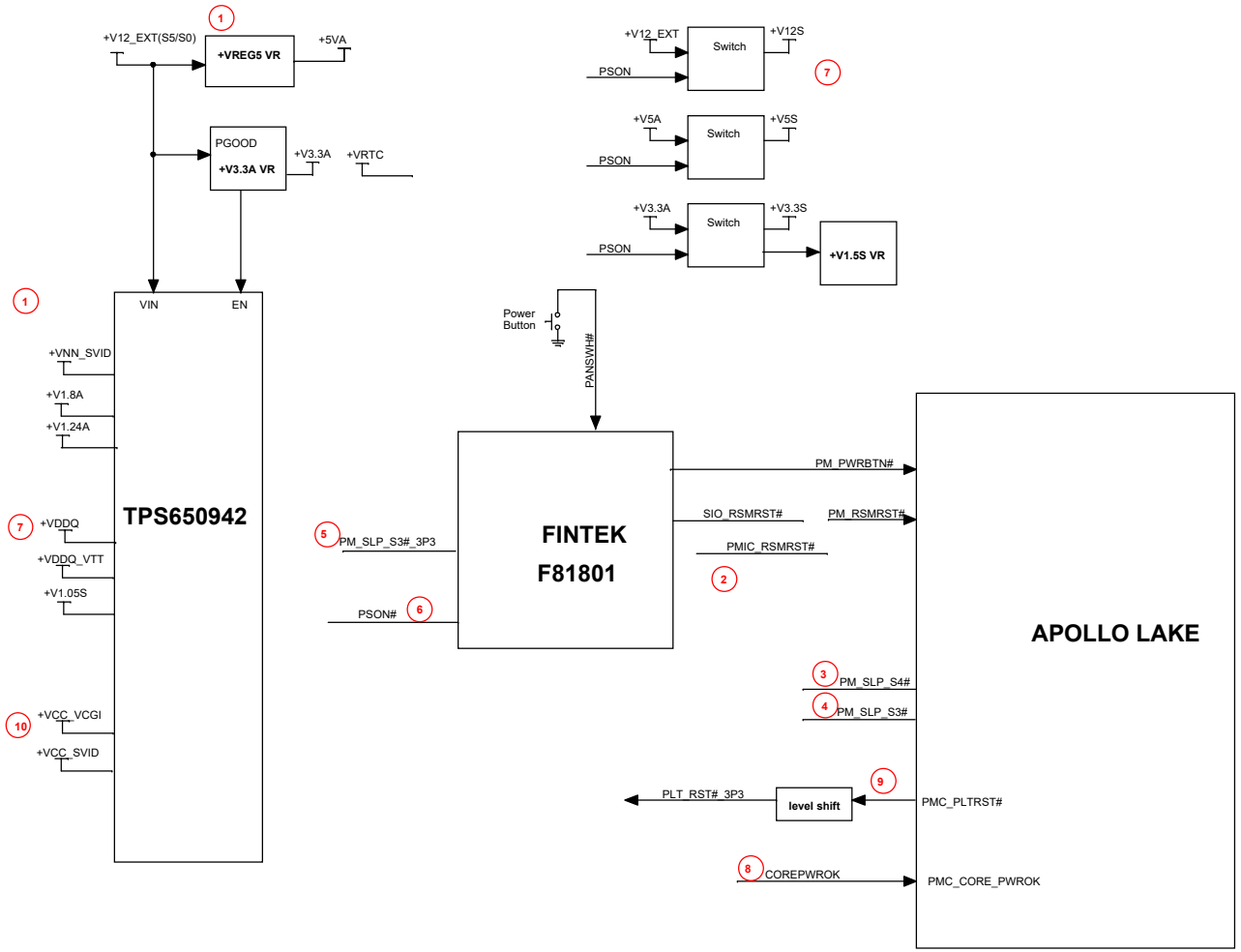
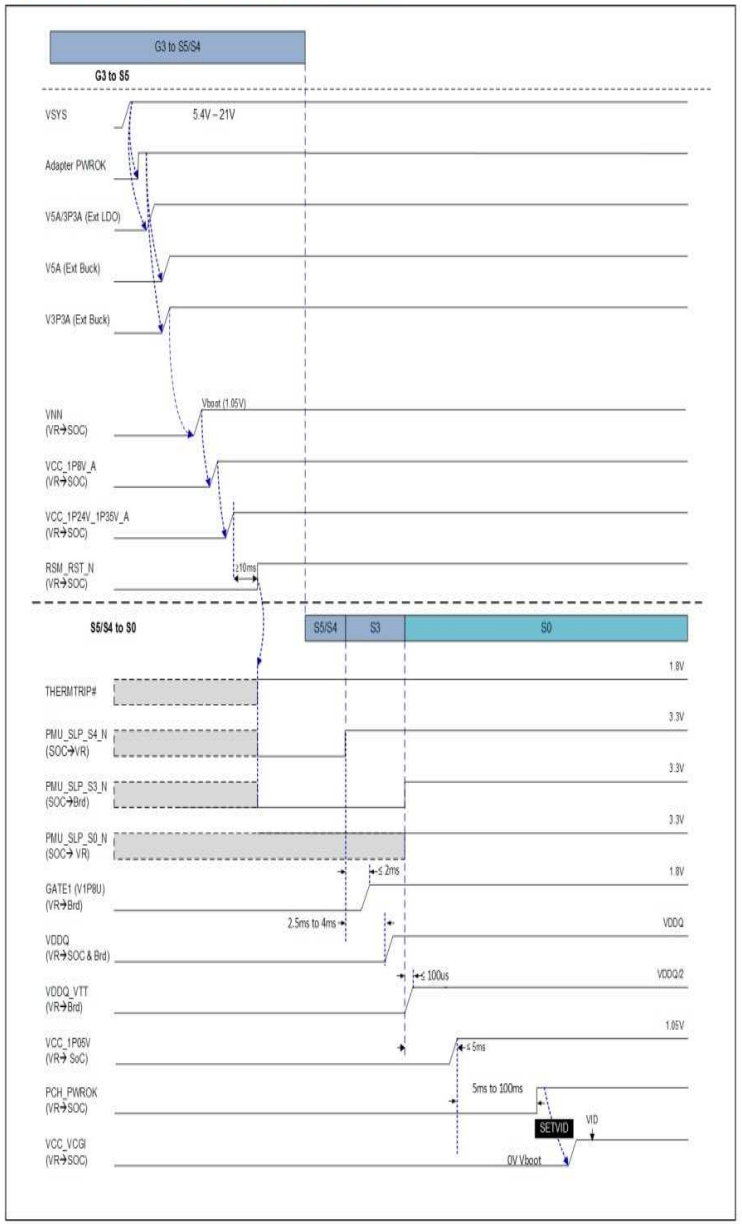


Power-Up Sequencing (G3 to S0)—Adapter



AAEON an ASUS assoc. co.	Title: Power Sequence	
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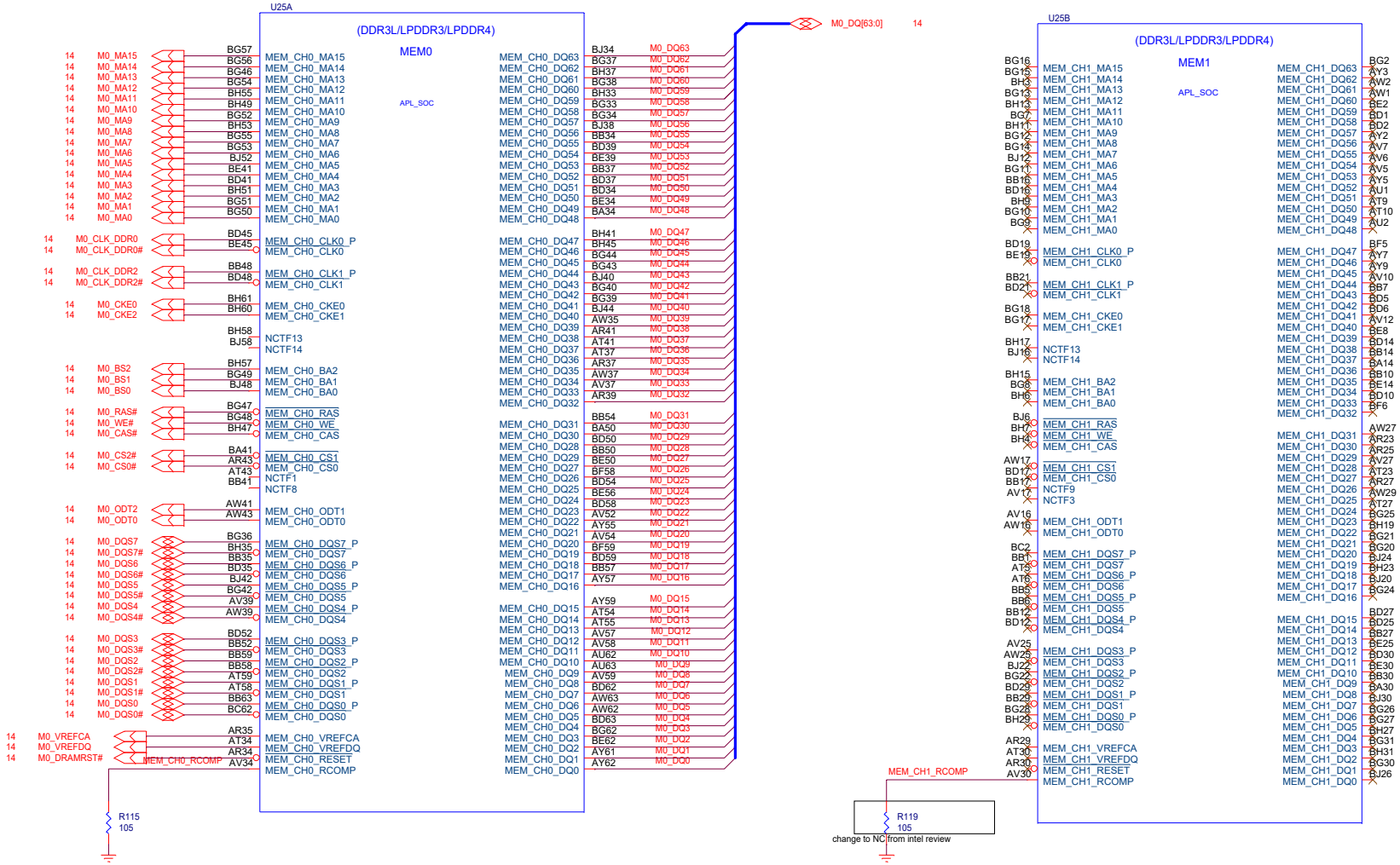

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Size: Custom	Document Number: PICOAPL1A10		Rev: A1.0_0_0
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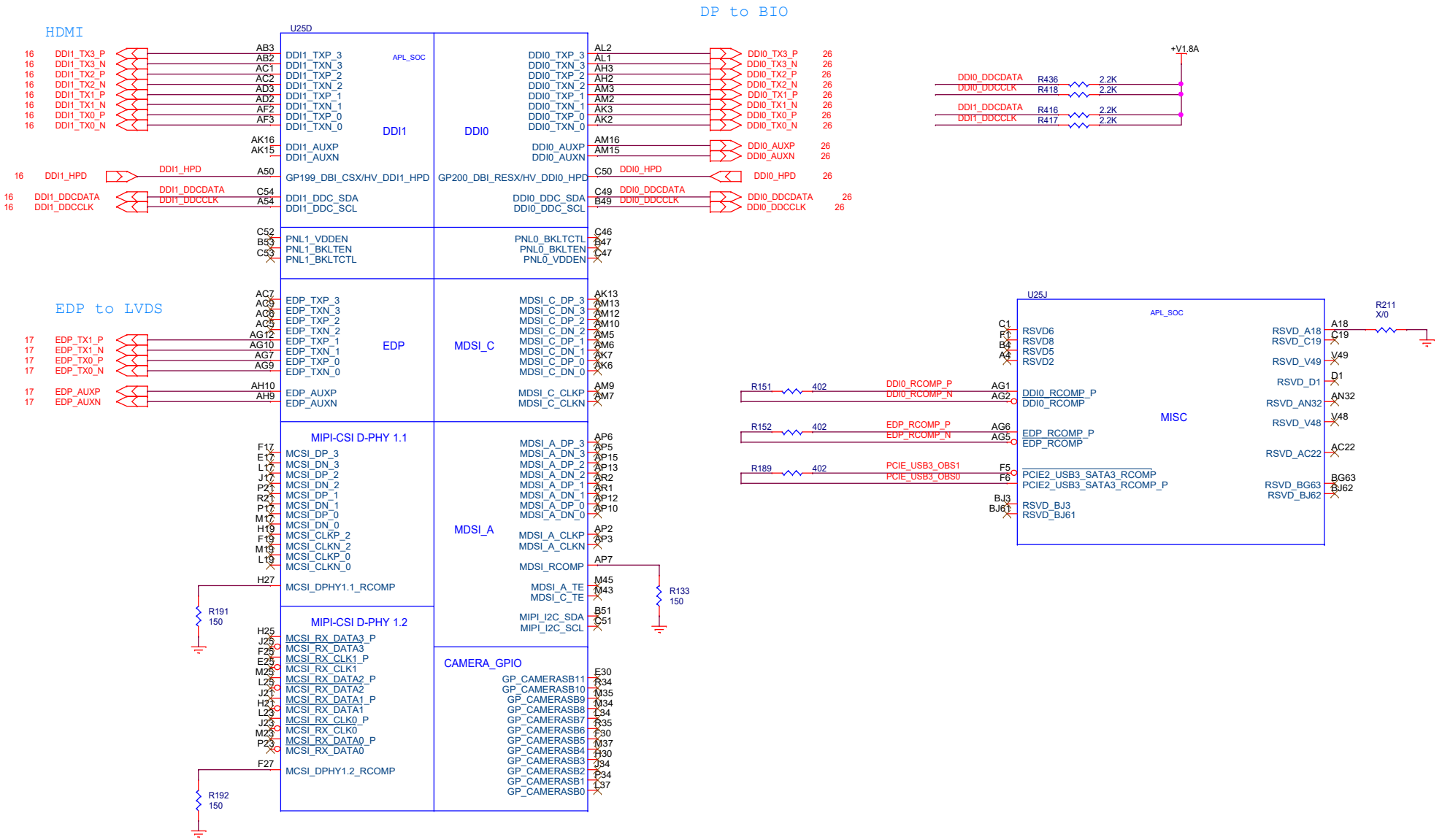

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	Size: Custom	Document Number: PICOAPL1A10 — Rev: A1.0_0_0
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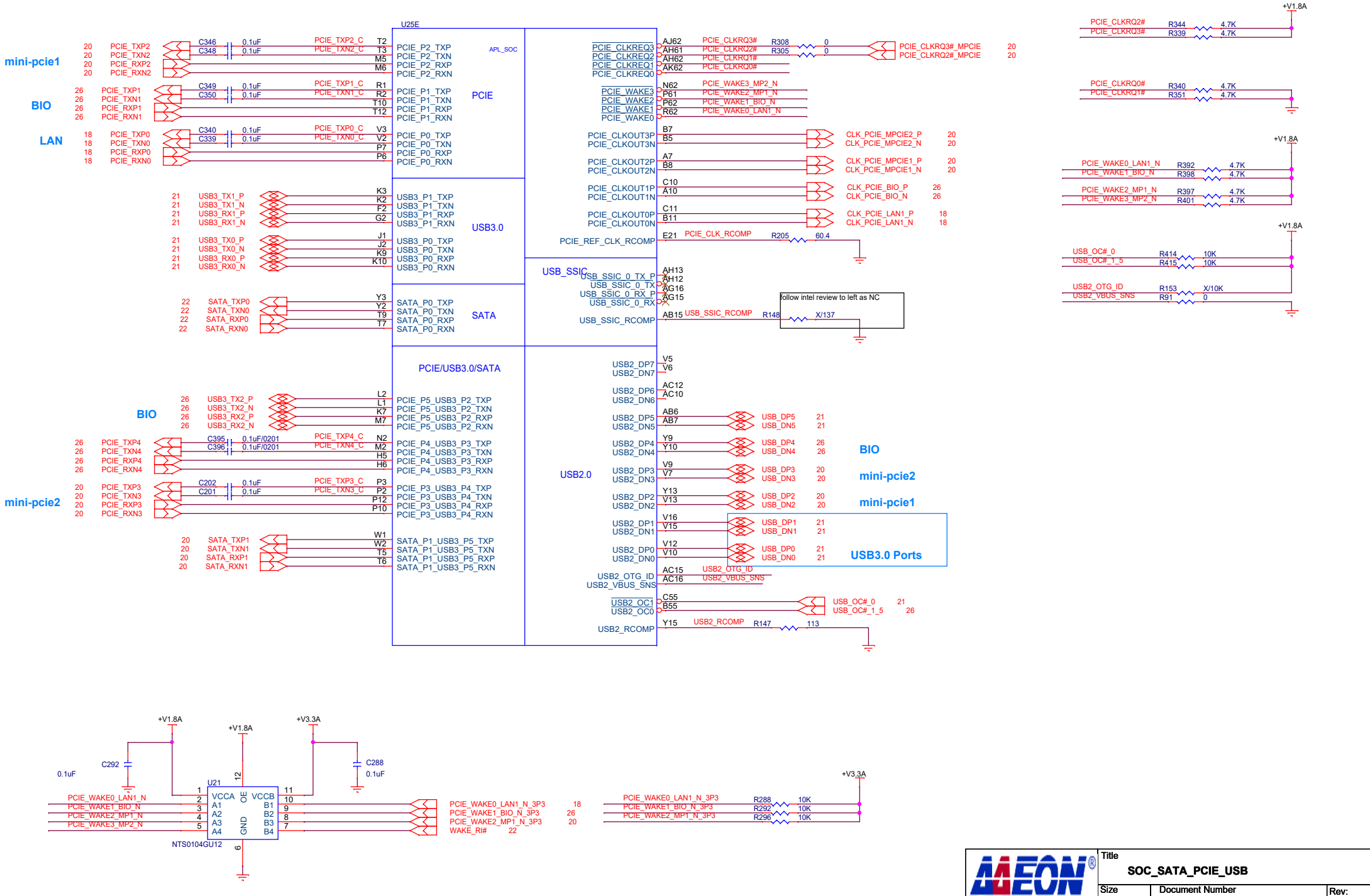

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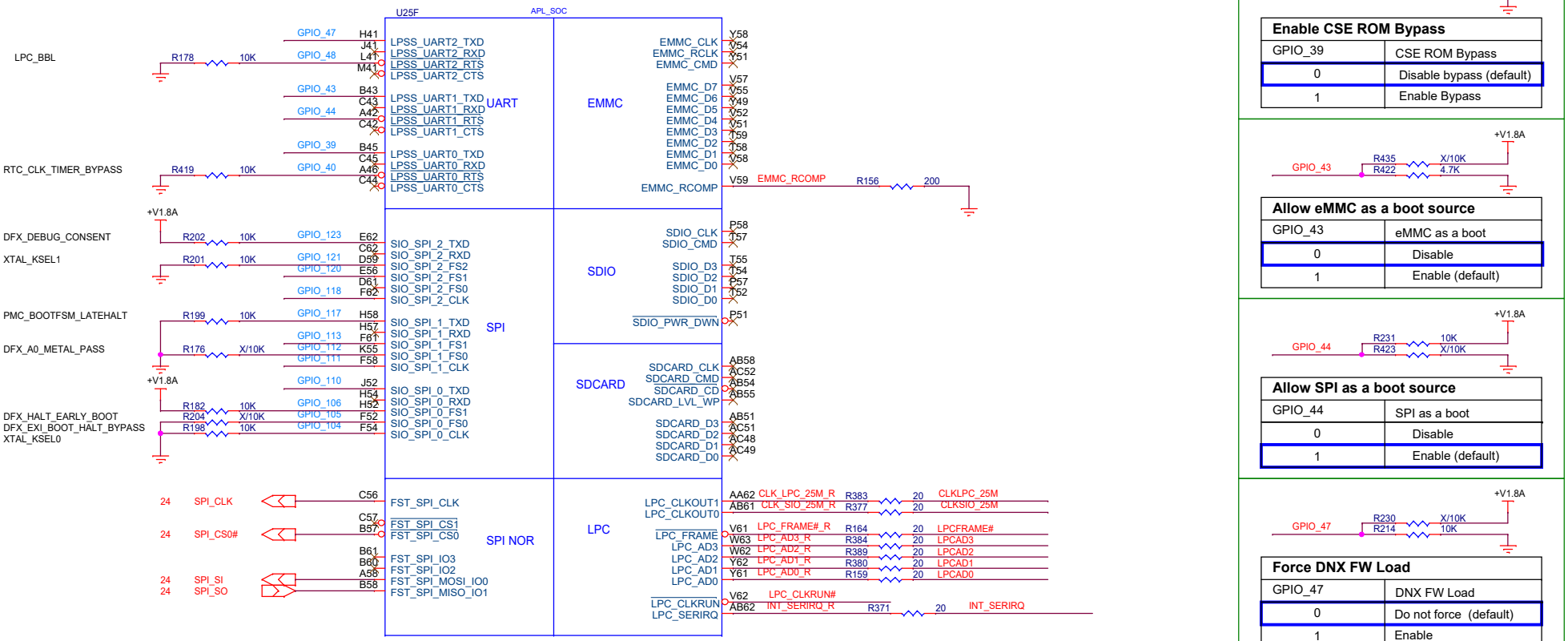
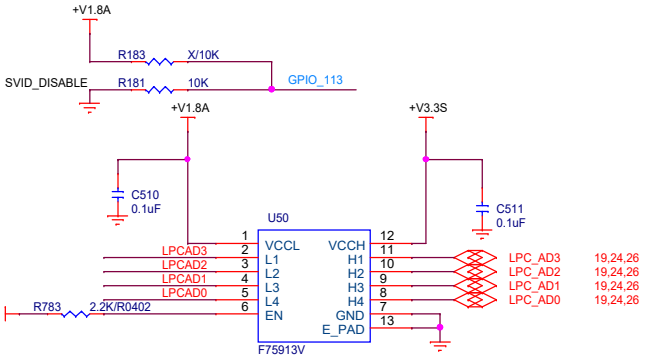
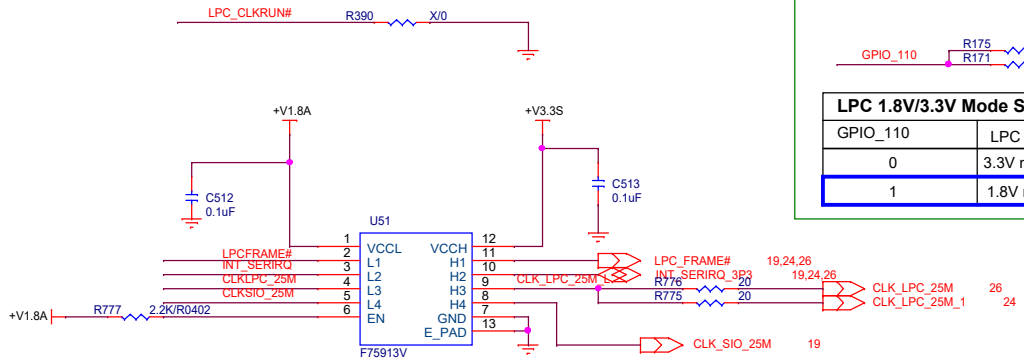






Enable CSE ROM Bypass

GPIO_39	CSE ROM Bypass
0	Disable bypass (default)
1	Enable Bypass

Allow eMMC as a boot source

GPIO_43	eMMC as a boot
0	Disable
1	Enable (default)

Allow SPI as a boot source

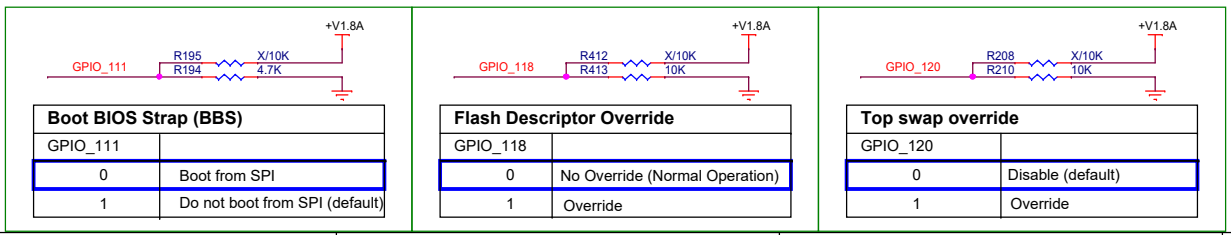
GPIO_44	SPI as a boot
0	Disable
1	Enable (default)

Force DNX FW Load

GPIO_47	DNX FW Load
0	Do not force (default)
1	Enable

LPC 1.8V/3.3V Mode Select

GPIO_110	LPC Voltage
0	3.3V mode
1	1.8V mode (default)



Boot BIOS Strap (BBS)

GPIO_111	
0	Boot from SPI
1	Do not boot from SPI (default)

Flash Descriptor Override

GPIO_118	
0	No Override (Normal Operation)
1	Override

Top swap override

GPIO_120	
0	Disable (default)
1	Override

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Title: SOC_LPC_SPI_EMMC_SD

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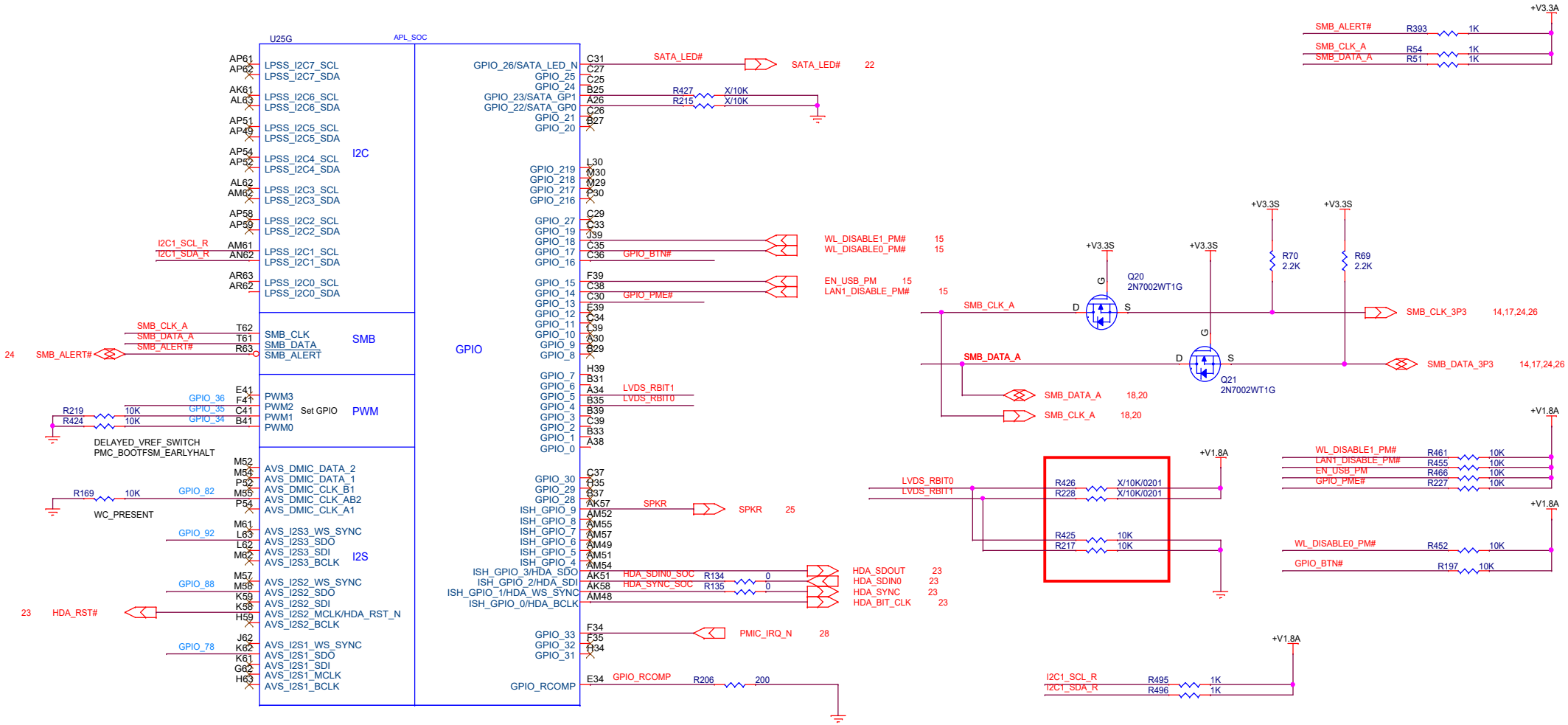
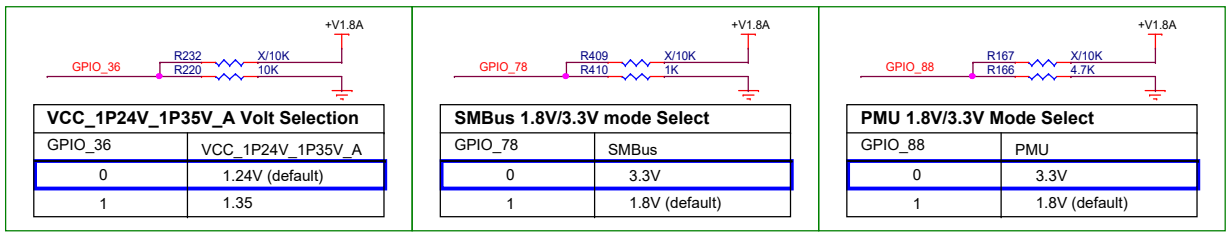


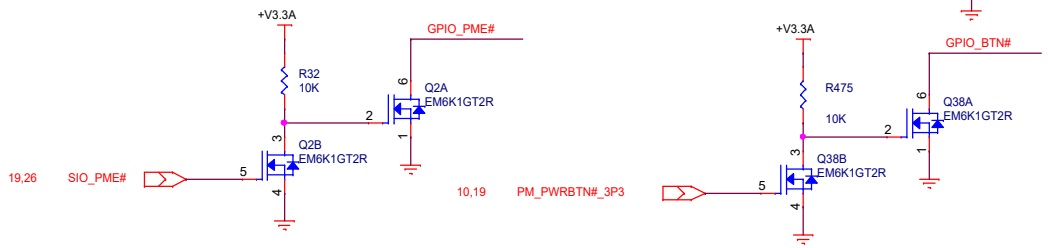


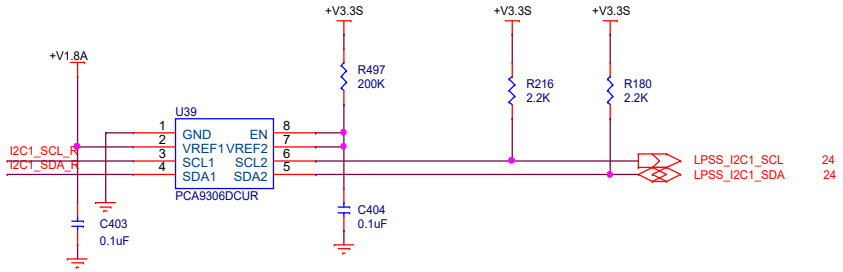
VCC_1P24V_1P35V_A Volt Selection	
GPIO_36	VCC_1P24V_1P35V_A
0	1.24V (default)
1	1.35

SMBus 1.8V/3.3V mode Select	
GPIO_78	SMBus
0	3.3V
1	1.8V (default)

PMU 1.8V/3.3V Mode Select	
GPIO_88	PMU
0	3.3V
1	1.8V (default)

SMBus No Re-Boot	
GPIO_92	No Re-Boot
0	Disable (default)
1	Enable





Title	SOC_SMBUS_GPIO
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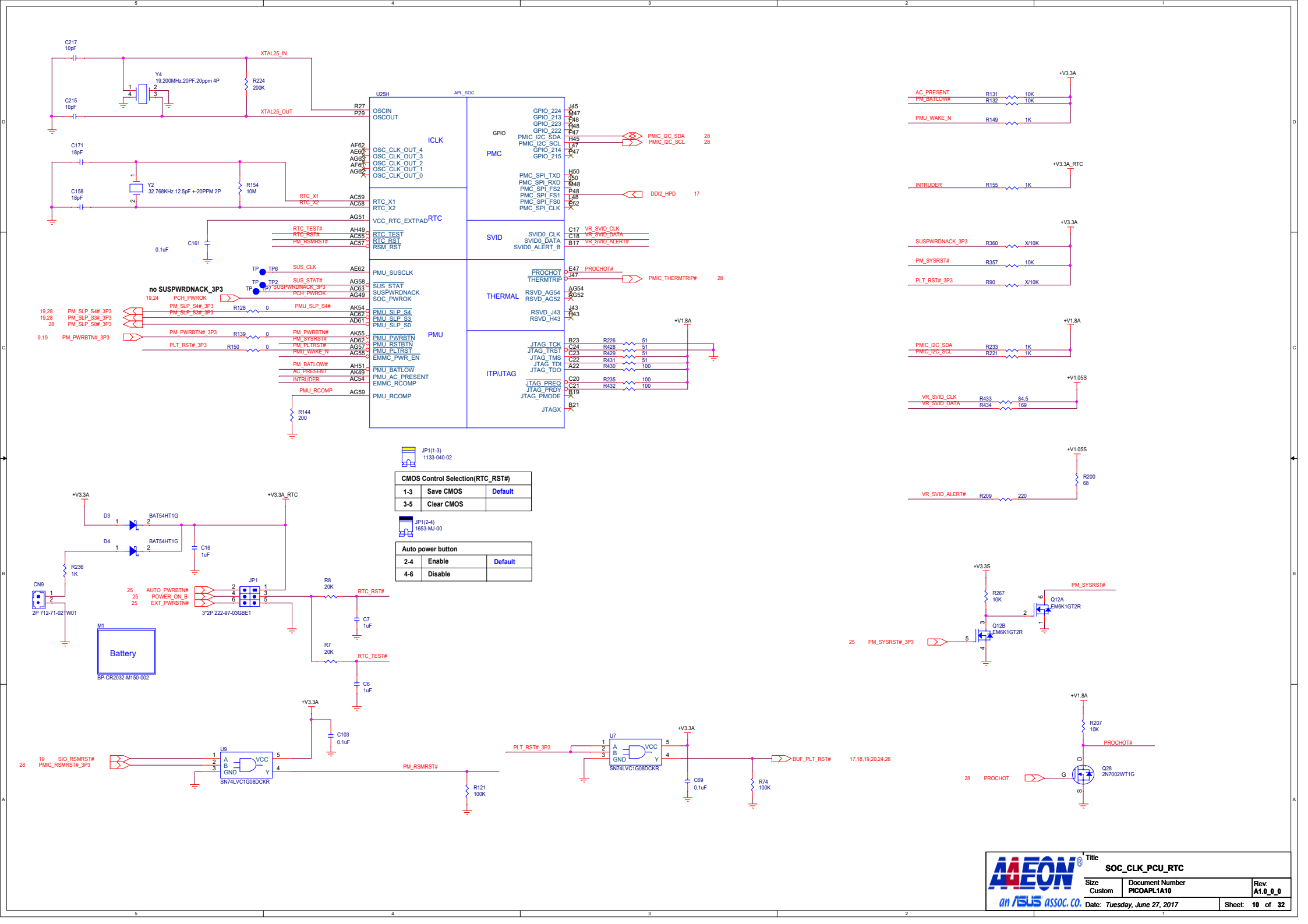
C217 10pF
C215 10pF
Y4 19.200MHz.20PF.20ppm 4P
R224 200K
XTAL25_IN
XTAL25_OUT
C171 18pF
C158 18pF
Y2 32.768KHz.12.5pF +-20PPM 2P
R154 10M
RTC_X1
RTC_X2
C161 0.1uF
U25H
APL_SOC
OSCIN
OSCOUT
ICLK
OSC_CLK_OUT_4
OSC_CLK_OUT_3
OSC_CLK_OUT_2
OSC_CLK_OUT_1
OSC_CLK_OUT_0
RTC_X1
RTC_X2
VCC_RTC_EXTPAD
RTC
RTC_TEST
RTC_RST
RSM_RST
PMU_SUSCLK
SUS_STAT
SUSPWRDNACK
SOC_PWROK
PMU_SLP_S4
PMU_SLP_S3
PMU_SLP_S0
PMU_PWRBTN
PMU_RSTBTN
PMU_PLTRST
EMMC_PWR_EN
PMU_BATLOW
PMU_AC_PRESENT
EMMC_RCOMP
PMU_RCOMP
PMU
GPIO
PMC
SVID
THERMAL
ITP/JTAG
PMIC_I2C_SDA
PMIC_I2C_SCL
DDI2_HPD
SVID0_CLK
SVID0_DATA
SVID0_ALERT_B
PROCHOT
THERMTRIP
RSVD_AG54
RSVD_AG52
RSVD_J43
RSVD_H43
JTAG_TCK
JTAG_TRST
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_PREQ
JTAG_PRDY
JTAG_PMODE
JTAGX
no SUSPWRDNACK_3P3
R144 200
R128 0
R139 0
R150 0
+V1.8A
JP1(1-3) 1133-040-02
CMOS Control Selection(RTC_RST#)
1-3 Save CMOS Default
3-5 Clear CMOS
JP1(2-4) 1653-MJ-00
Auto power button
2-4 Enable Default
4-6 Disable
+V3.3A
+V3.3A_RTC
D3 BAT54HT1G
D4 BAT54HT1G
C16 1uF
R236 1K
CN9
2P 712-71-02TW01
JP1
3*2P 222-97-03GBE1
AUTO_PWRBTN#
POWER_ON_B
EXT_PWRBTN#
R8 20K
R7 20K
C7 1uF
C6 1uF
RTC_RST#
RTC_TEST#
M1
Battery
BP-CR2032-M150-002
U9
SN74LVC1G08DCKR
C103 0.1uF
SIO_RSMRST#
PMIC_RSMRST#_3P3
PM_RSMRST#
R121 100K
U7
PLT_RST#_3P3
BUF_PLT_RST#
17,18,19,20,24,26
C69 0.1uF
R74 100K
AC_PRESENT
PM_BATLOW#
PMU_WAKE_N
R131 10K
R132 10K
R149 1K
INTRUDER
R155 1K
SUSPWRDNACK_3P3
PM_SYSRST#
PLT_RST#_3P3
R360 X/10K
R357 10K
R90 X/10K
PMIC_I2C_SDA
PMIC_I2C_SCL
R233 1K
R221 1K
VR_SVID_CLK
VR_SVID_DATA
R433 84.5
R434 169
+V1.05S
VR_SVID_ALERT#
R209 220
R200 68
R267 10K
Q12A EM6K1GT2R
Q12B EM6K1GT2R
PM_SYSRST#_3P3
R207 10K
PROCHOT#
Q28 2N7002WT1G
PROCHOT
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SOC_CLK_PCU_RTC
Size Custom
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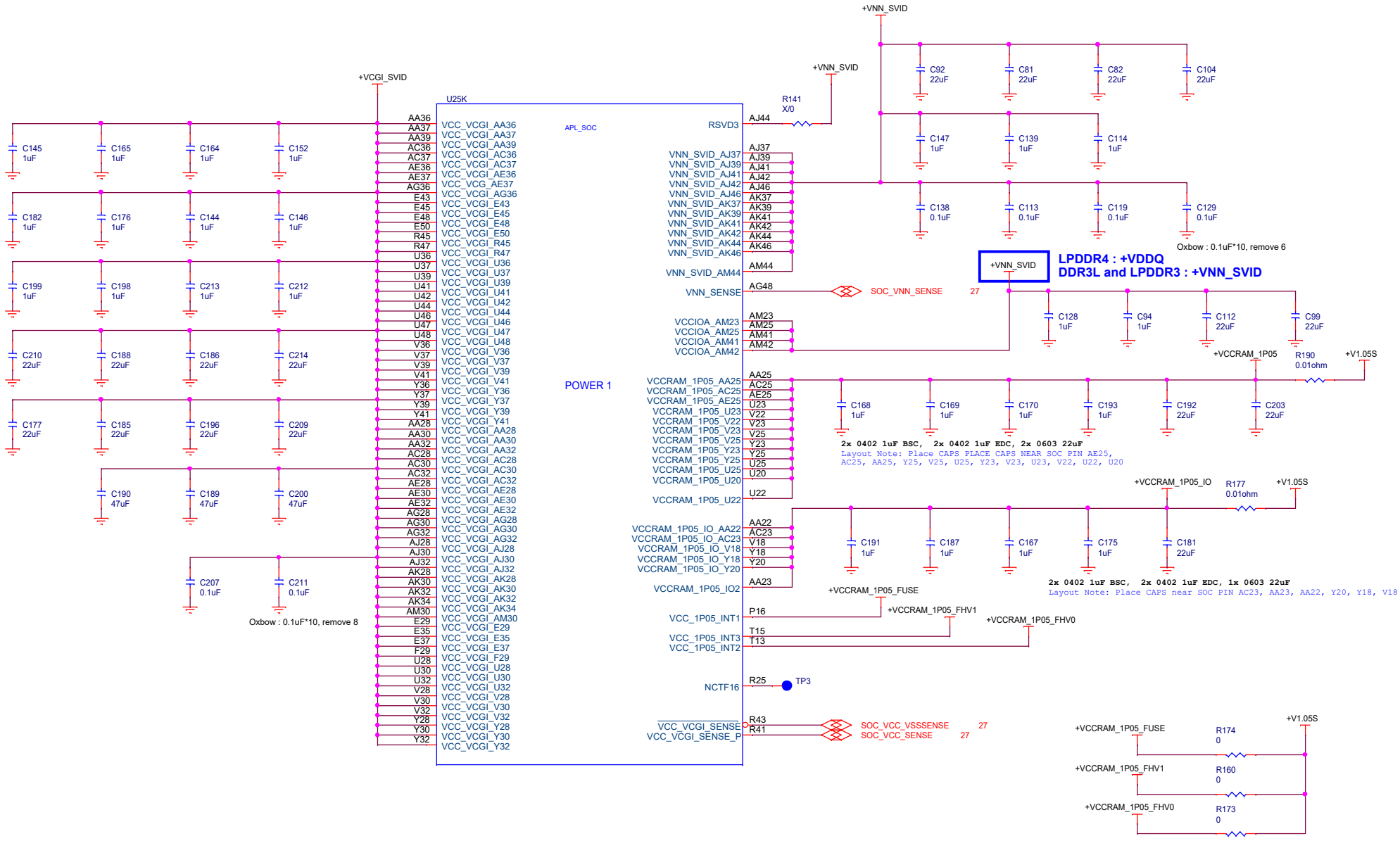

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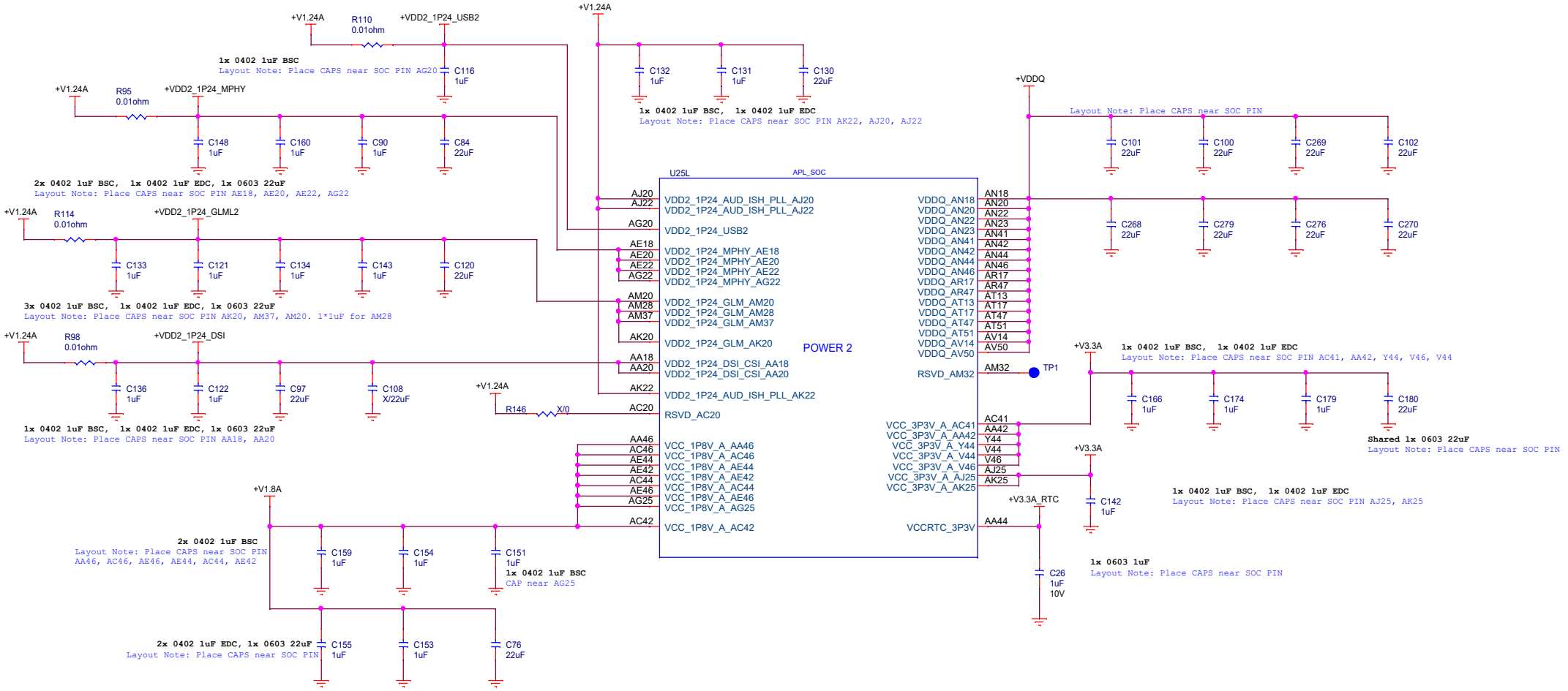

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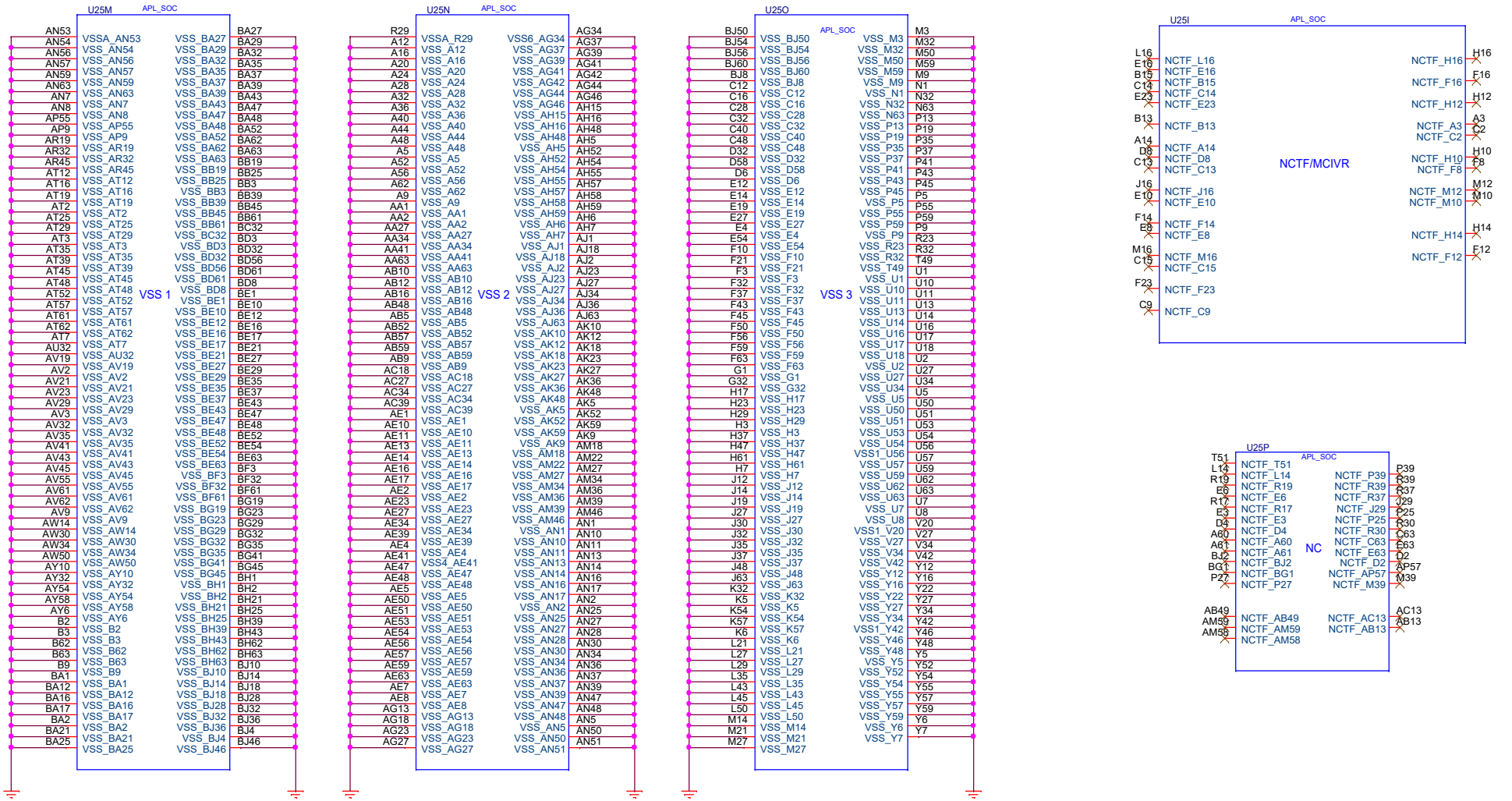

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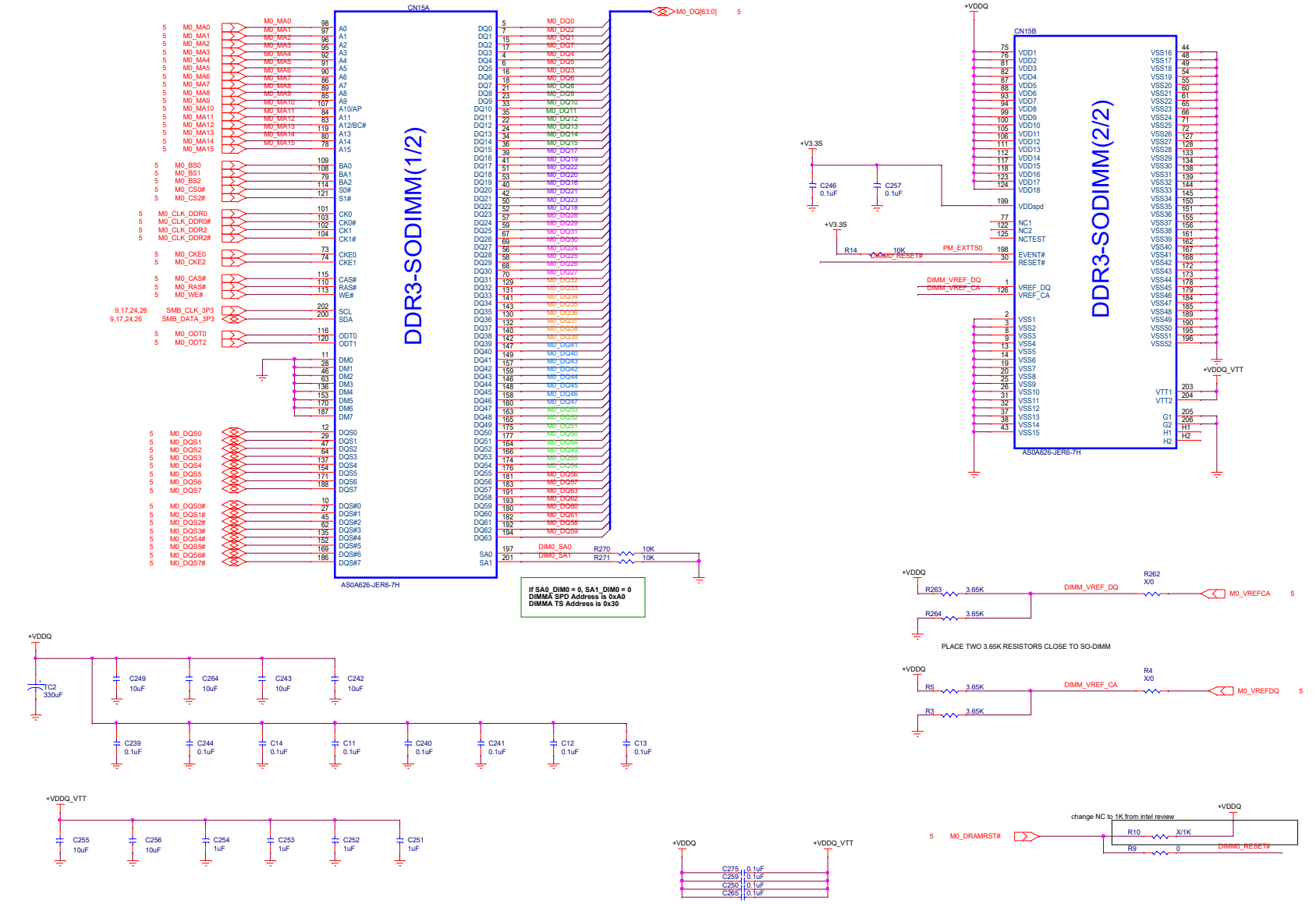
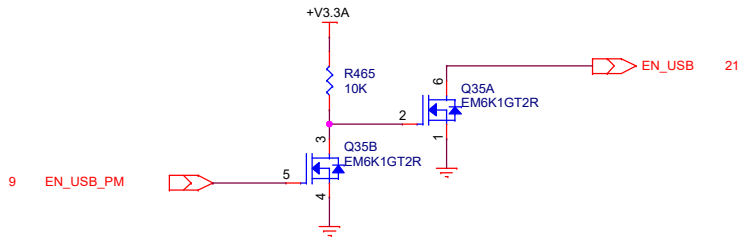
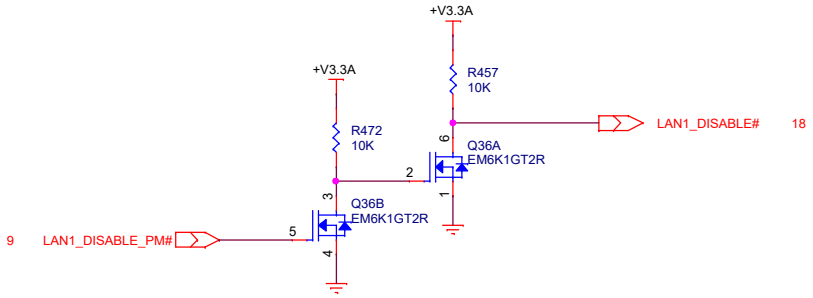
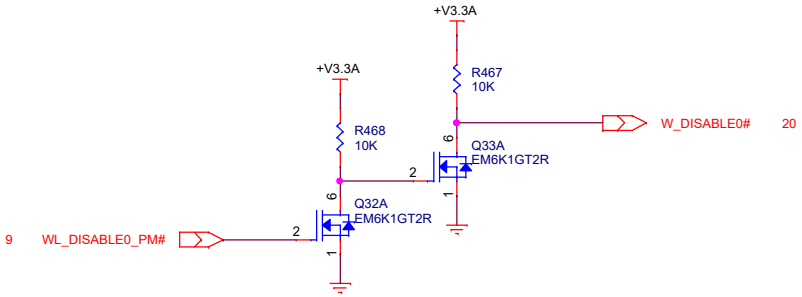
SODIMM#0

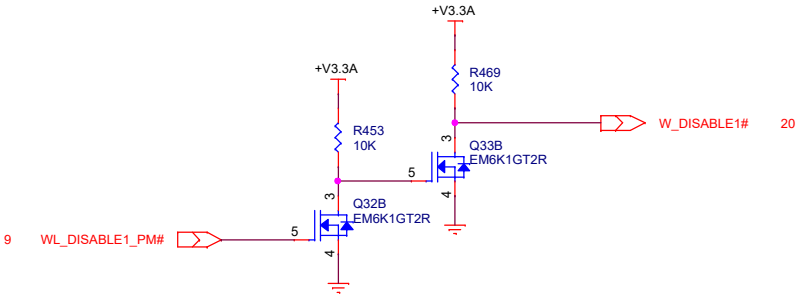


Title	DDR3L SODIMM		
Size C	Document Number PICOAPL1A10		Rev: A1.0_0_0
an ASUS ASSOC. CO.	Date: Tuesday, June 27, 2017	Sheet: 14 of 32	









AAEON an ASUS assoc. co.

Title: **Level Shift**

Size	Document Number	Rev:
B	PICOAPL1A10	A1.0_0_0

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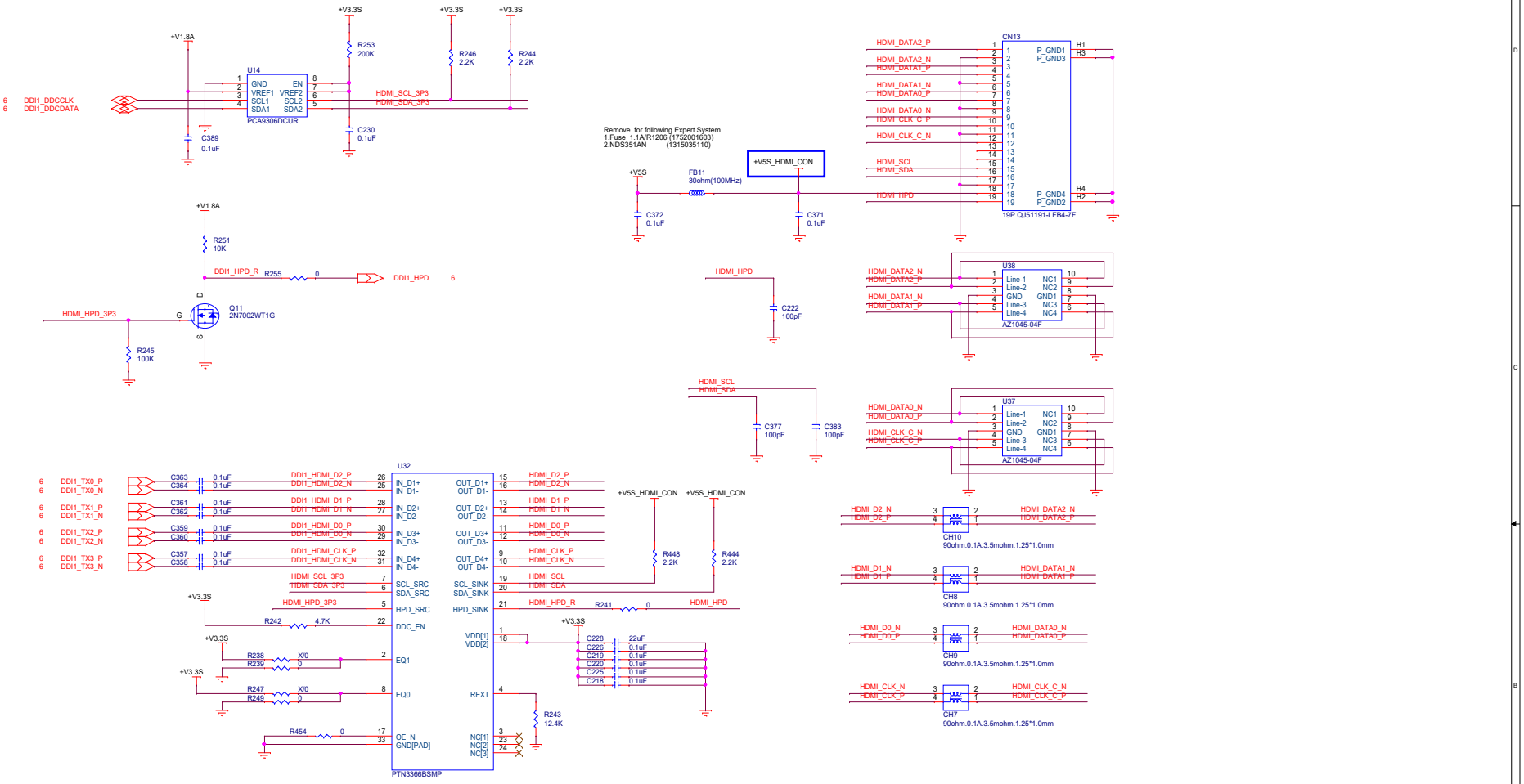
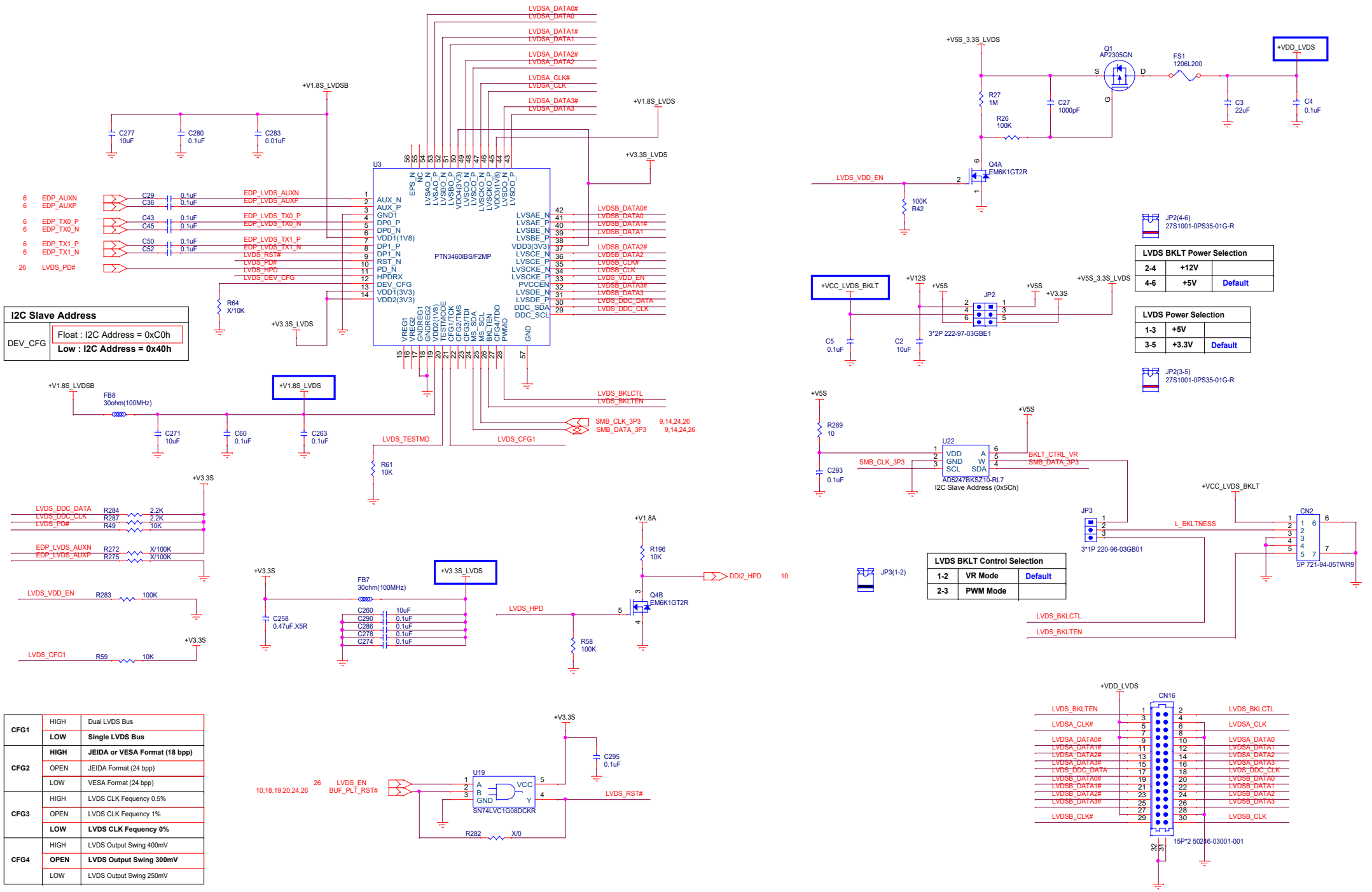
HDMI



AAEON an ASUS assoc. co.	Title: HDMI		
	Size: C	Document Number: PICOAPL1A10	Rev: A1.0_0_0
	Date: Tuesday, June 27, 2017	Sheet: 16 of 32	



CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

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Title: **PTN3460 eDP to LVDS**

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Custom	PICOAPL1A10	A1.0_0_0

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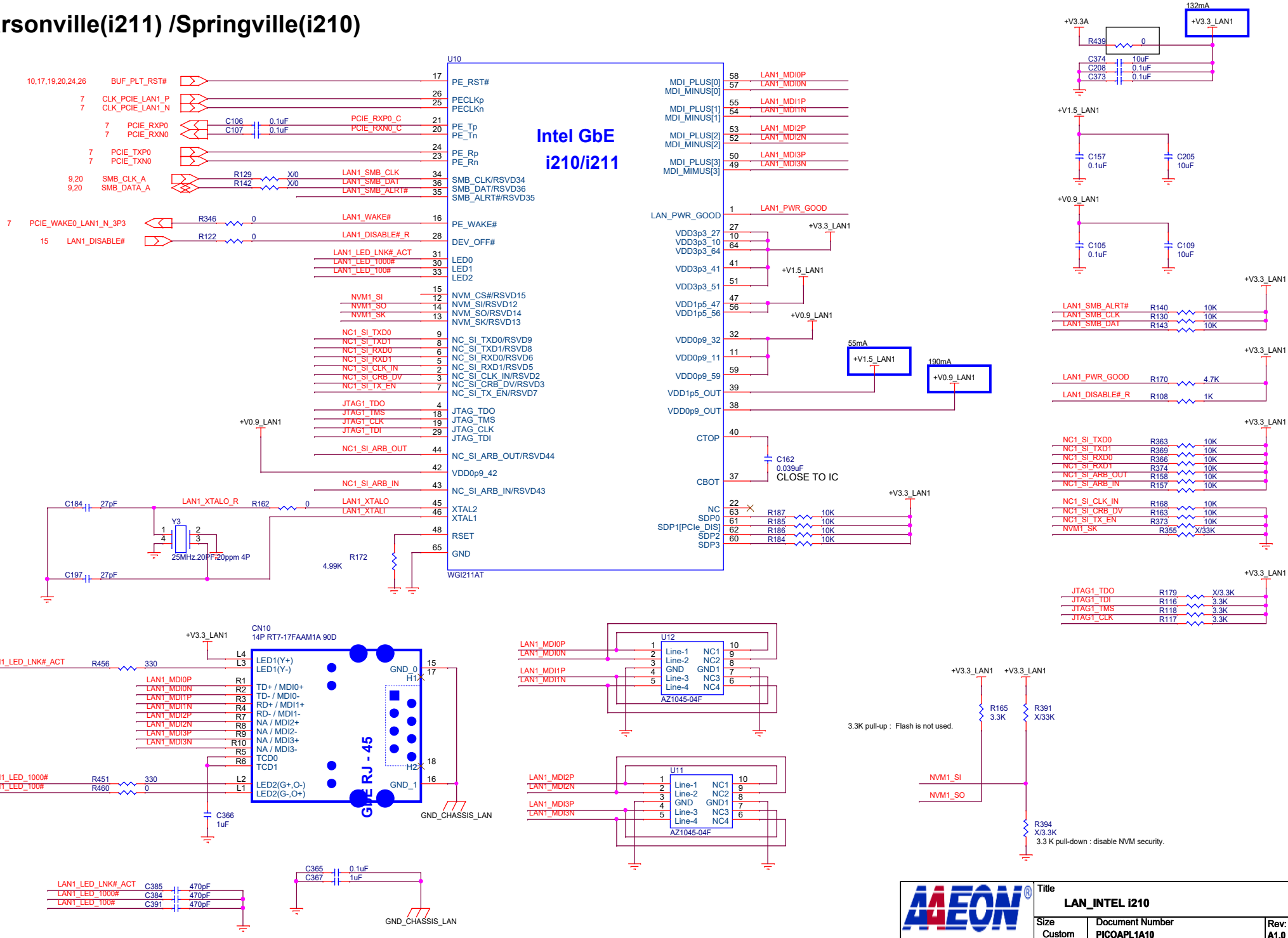
Pearsonville(i211) /Springville(i210)



Title: LAN_INTEL i210		
Size: Custom	Document Number: PICOAPL1A10	Rev: A1.0_0_0
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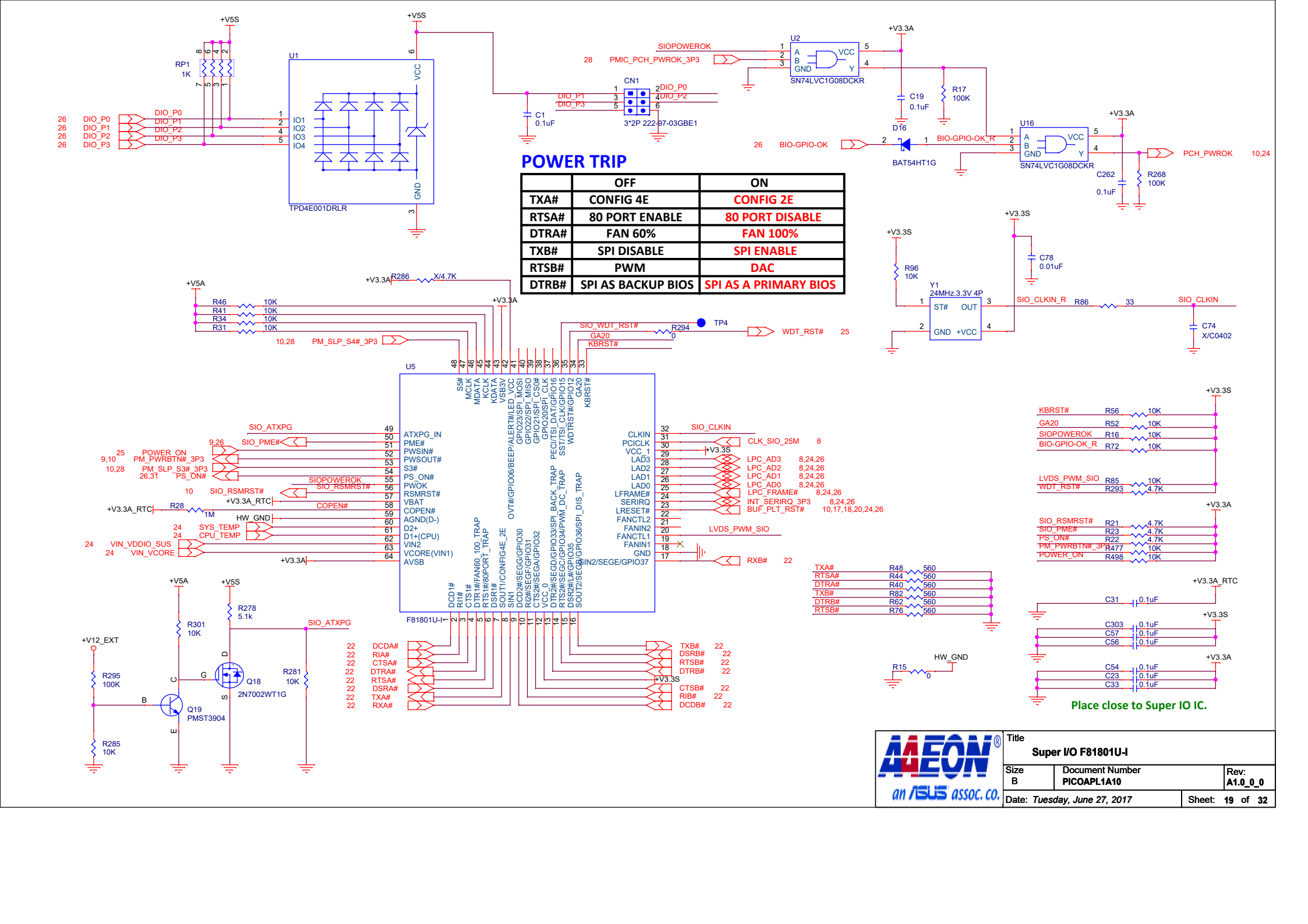
POWER TRIP
OFF
ON
TXA#
CONFIG 4E
CONFIG 2E
RTSA#
80 PORT ENABLE
80 PORT DISABLE
DTRA#
FAN 60%
FAN 100%
TXB#
SPI DISABLE
SPI ENABLE
RTSB#
PWM
DAC
DTRB#
SPI AS BACKUP BIOS
SPI AS A PRIMARY BIOS
U1
TPD4E001DRLR
U2
SN74LVC1G08DCKR
U16
SN74LVC1G08DCKR
D16
BAT54HT1G
CN1
3*2P 222-97-03GBE1
U5
F81801U-I
Q18
2N7002WT1G
Q19
PMST3904
Y1
24MHz,3.3V 4P
Place close to Super IO IC.
Super I/O F81801U-I
PICOAPL1A10
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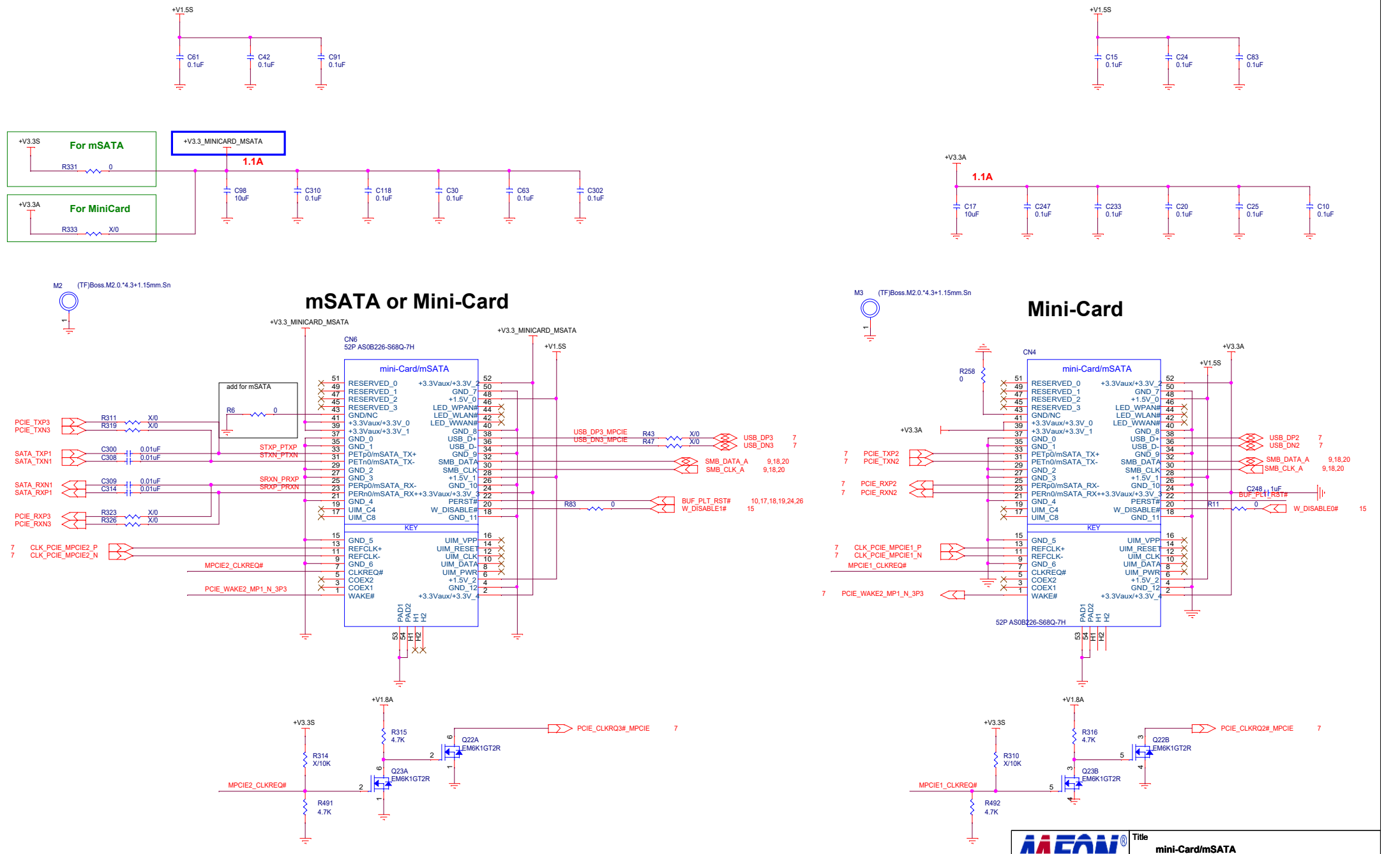
+V1.5S
C61 0.1uF
C42 0.1uF
C91 0.1uF
+V3.3S
For mSATA
R331 0
+V3.3_MINICARD_MSATA
1.1A
+V3.3A
For MiniCard
R333 X/0
C98 10uF
C310 0.1uF
C118 0.1uF
C30 0.1uF
C63 0.1uF
C302 0.1uF
+V1.5S
C15 0.1uF
C24 0.1uF
C83 0.1uF
+V3.3A
1.1A
C17 10uF
C247 0.1uF
C233 0.1uF
C20 0.1uF
C25 0.1uF
C10 0.1uF
M2 (TF)Boss.M2.0.*4.3+1.15mm.Sn
mSATA or Mini-Card
+V3.3_MINICARD_MSATA
CN6
52P AS0B226-S68Q-7H
mini-Card/mSATA
add for mSATA
R6 0
PCIE_TXP3
PCIE_TXN3
R311 X/0
R319 X/0
SATA_TXP1
SATA_TXN1
C300 0.01uF
C308 0.01uF
STXP_PTXP
STXN_PTXN
SATA_RXN1
SATA_RXP1
C309 0.01uF
C314 0.01uF
SRXN_PRXP
SRXP_PRXN
PCIE_RXP3
PCIE_RXN3
R323 X/0
R326 X/0
CLK_PCIE_MPCIE2_P
CLK_PCIE_MPCIE2_N
MPCIE2_CLKREQ#
PCIE_WAKE2_MP1_N_3P3
RESERVED_0
RESERVED_1
RESERVED_2
RESERVED_3
GND/NC
+3.3Vaux/+3.3V_0
+3.3Vaux/+3.3V_1
GND_0
GND_1
PETp0/mSATA_TX+
PETn0/mSATA_TX-
GND_2
GND_3
PERp0/mSATA_RX-
PERn0/mSATA_RX+
GND_4
UIM_C4
UIM_C8
KEY
GND_5
REFCLK+
REFCLK-
GND_6
CLKREQ#
COEX2
COEX1
WAKE#
+3.3Vaux/+3.3V_2
GND_7
+1.5V_0
LED_WPAN#
LED_WLAN#
LED_WWAN#
GND_8
USB_D+
USB_D-
GND_9
SMB_DATA
SMB_CLK
+1.5V_1
GND_10
PERST#
W_DISABLE#
GND_11
UIM_VPP
UIM_RESET
UIM_CLK
UIM_DATA
UIM_PWR
+1.5V_2
GND_12
+3.3Vaux/+3.3V_4
PAD1
PAD2
H1
H2
+V1.5S
USB_DP3_MPCIE
USB_DN3_MPCIE
R43 X/0
R47 X/0
USB_DP3
USB_DN3
SMB_DATA_A
SMB_CLK_A
9,18,20
R83 0
BUF_PLT_RST#
W_DISABLE1#
10,17,18,19,24,26
15
+V1.8A
+V3.3S
R315 4.7K
R314 X/10K
R491 4.7K
Q22A EM6K1GT2R
Q23A EM6K1GT2R
PCIE_CLKRQ3#_MPCIE
7
M3 (TF)Boss.M2.0.*4.3+1.15mm.Sn
Mini-Card
CN4
52P AS0B226-S68Q-7H
mini-Card/mSATA
R258 0
+V3.3A
+V1.5S
PCIE_TXP2
PCIE_TXN2
PCIE_RXP2
PCIE_RXN2
CLK_PCIE_MPCIE1_P
CLK_PCIE_MPCIE1_N
MPCIE1_CLKREQ#
PCIE_WAKE2_MP1_N_3P3
USB_DP2
USB_DN2
SMB_DATA_A
SMB_CLK_A
9,18,20
C248 1uF
BUF_PLT_RST#
R11 0
W_DISABLE0#
15
R316 4.7K
R310 X/10K
R492 4.7K
Q22B EM6K1GT2R
Q23B EM6K1GT2R
PCIE_CLKRQ2#_MPCIE
7
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an ASUS assoc. co.
Title
mini-Card/mSATA
Size
Custom
Document Number
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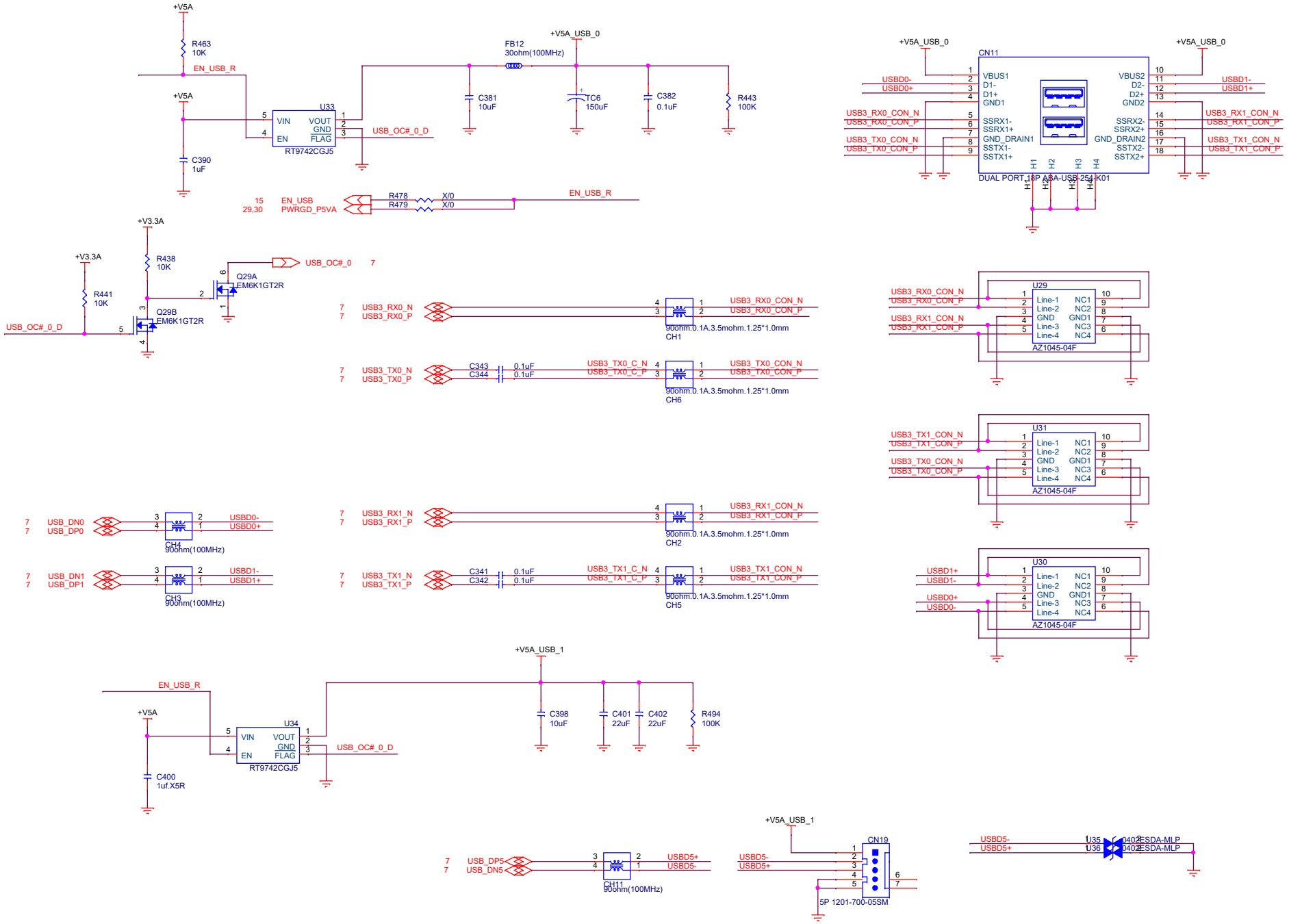
USB3.0 x 2



AAEON an ASUS assoc. co.	Title: USB 3.0/2.0 PORT	
Size: Custom	Document Number: PICOAPL1A10	Rev: A1.0_0_0
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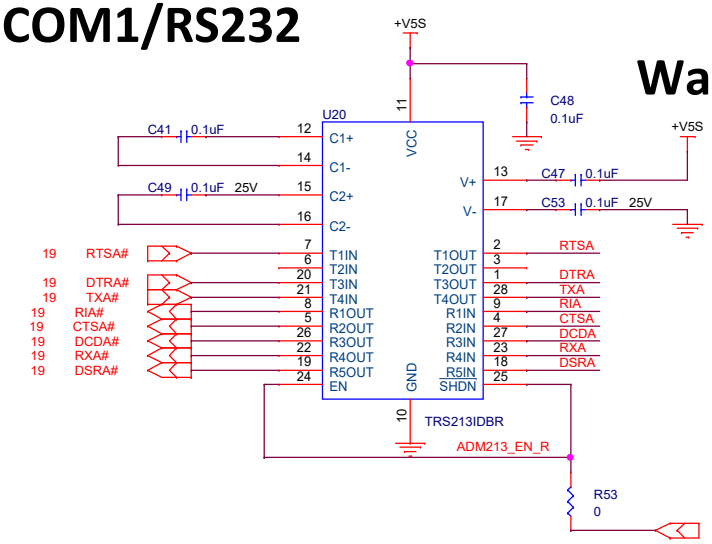
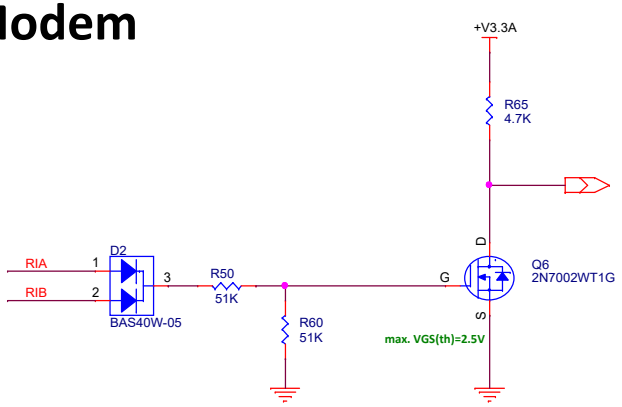
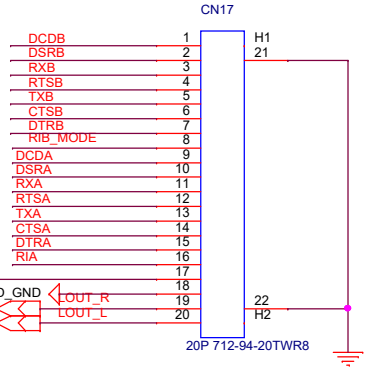
COM1/RS232

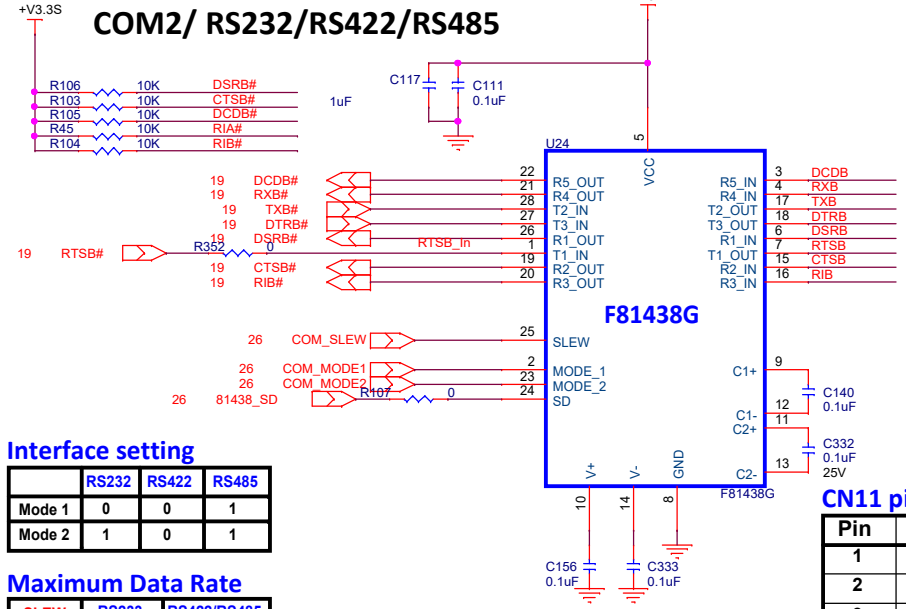


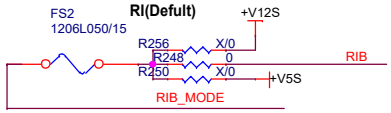
Wake on Modem

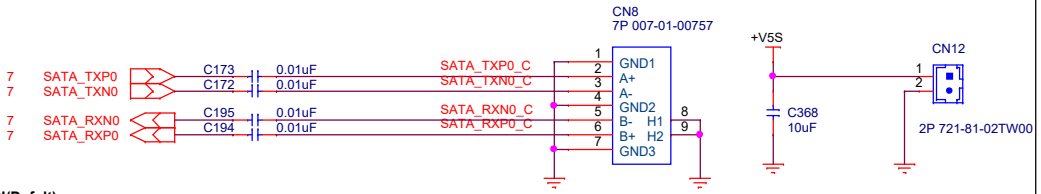


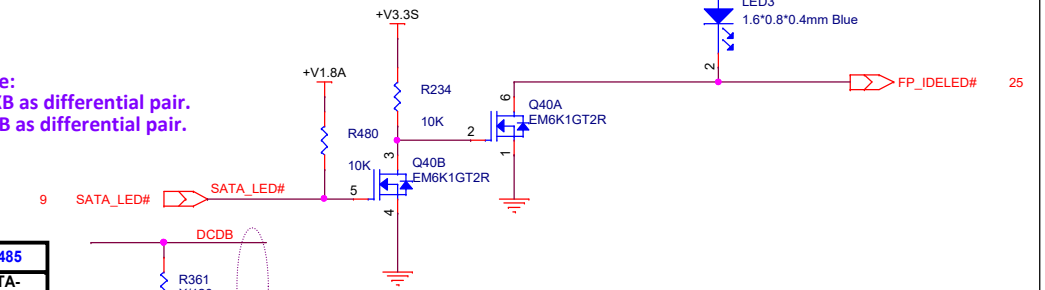


COM2/ RS232/RS422/RS485









Layout note:
DCDB & RXB as differential pair.
TXB & DTRB as differential pair.

Interface setting

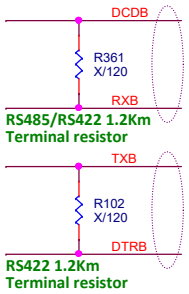
	RS232	RS422	RS485
Mode 1	0	0	1
Mode 2	1	0	1

Maximum Data Rate

SLEW	RS233	RS422/RS485
1	250kbps	250kbps
0	1Mbps	10Mbps

CN11 pin assignment

Pin	RS232	RS422	RS485
1	DCD	TX-	DATA-
2	DSR		
3	RX	TX+	DATA+
4	RTS		
5	TX	RX+	
6	CTS		
7	DTR	RX-	
8	RI		



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Title: **Serial Port 1/2/SATA**

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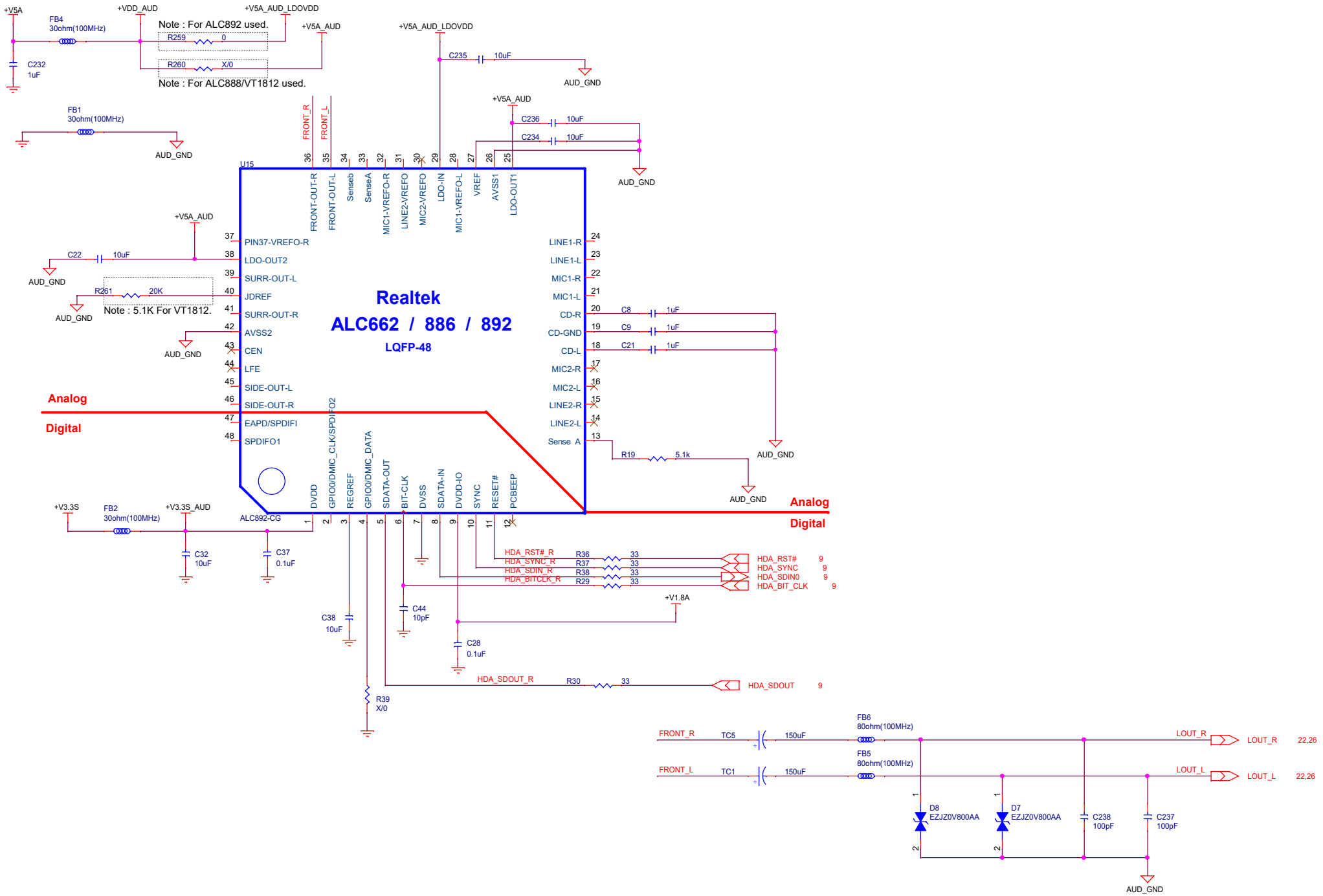

AAEON an ASUS assoc. co.	Title: HD Audio - ALC892	
Size: Custom	Document Number: PICOAPL1A10	Rev: A1.0_0_0
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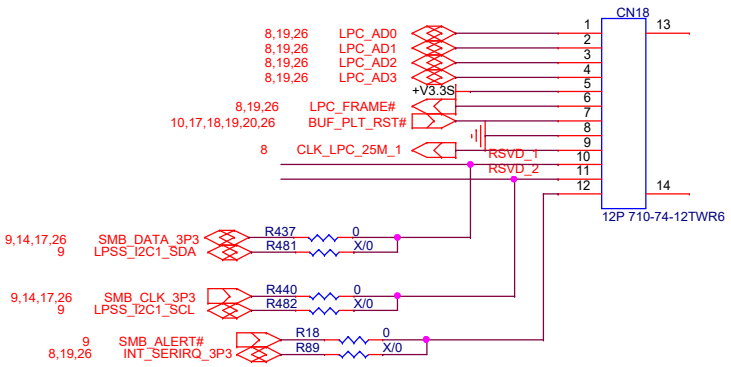
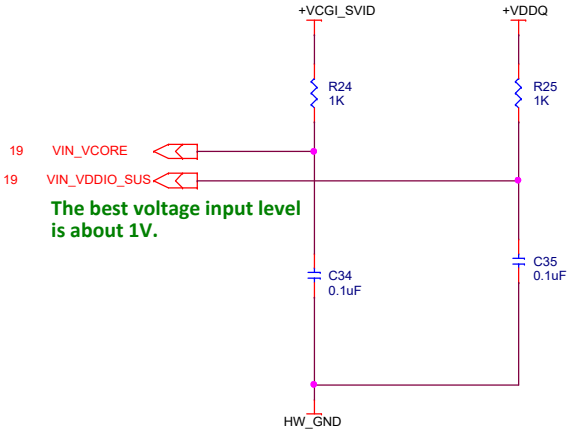
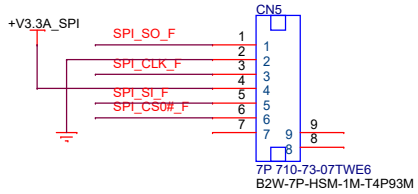
LPC Debug Connector

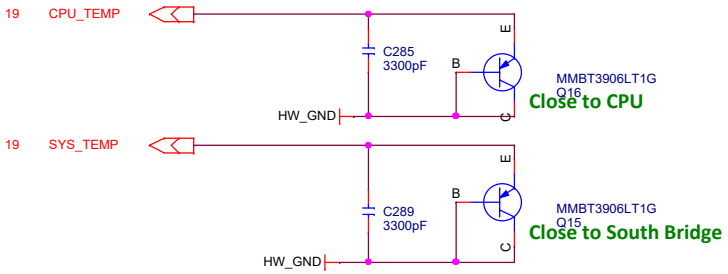


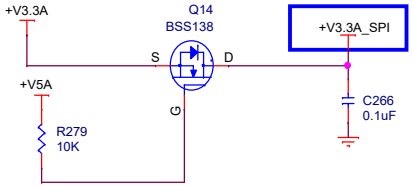
Voltage Monitor(Vcore, Vmem)



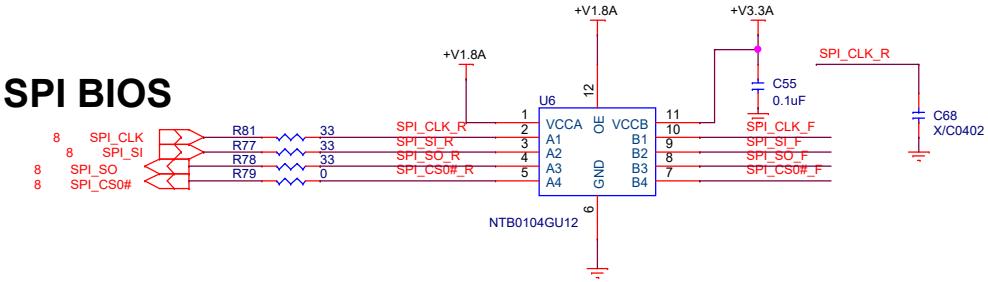


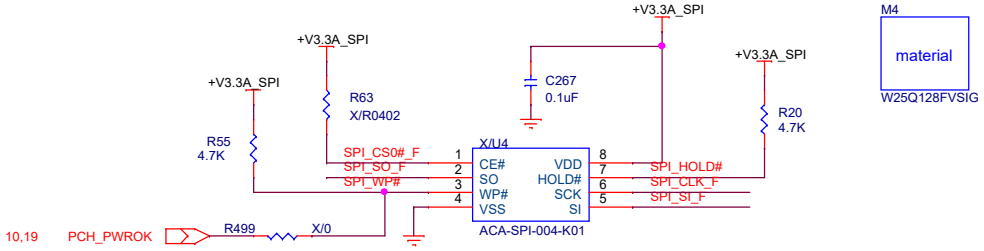
Temperature Monitor(CPU, SYS)





SPI BIOS





8 pin : 1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0
1462001280 (TF)IC.Flash Memory.128M Bit serial.SOIC-8(208mil).SMD.w/ Dual & Quad SPI.Winbond.W25Q128FVSIG

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Title: **H/W Mon/ Debug /CMOS**		
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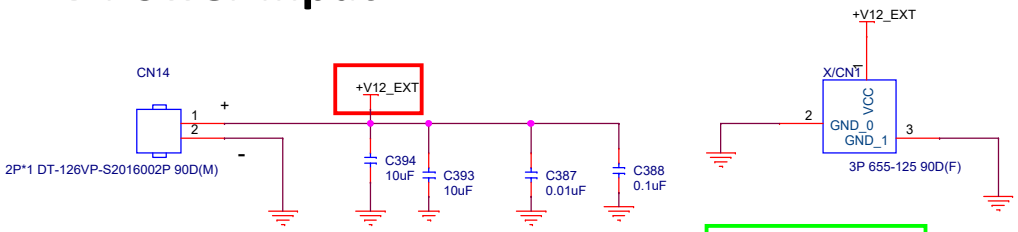
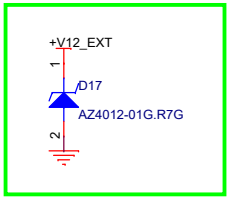
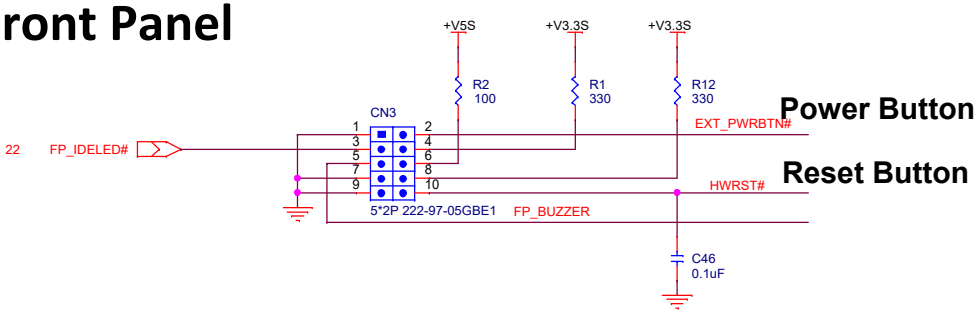
+12V Power Input

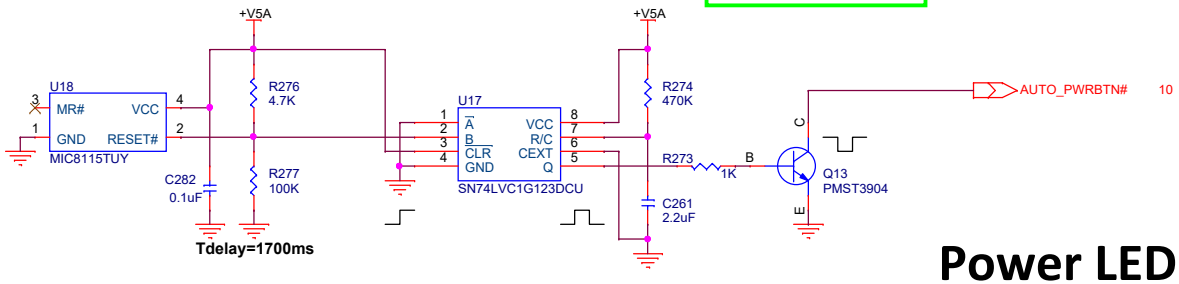


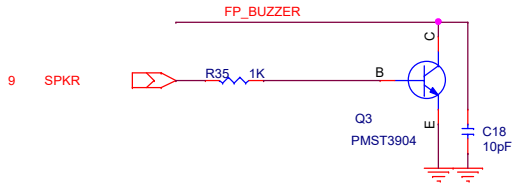


Front Panel

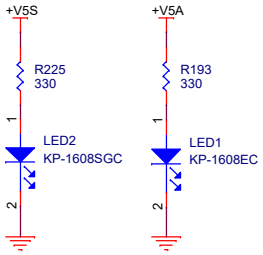


Auto Power Button

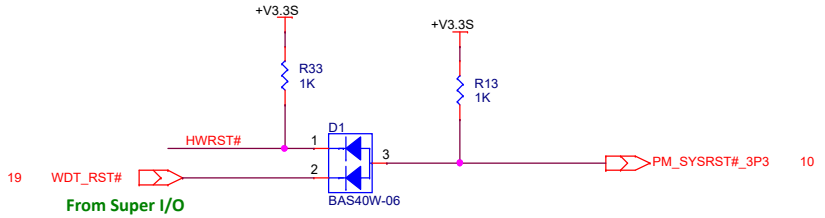


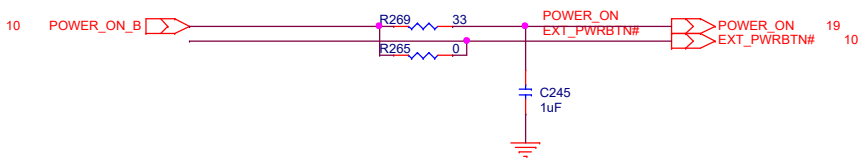


Power LED

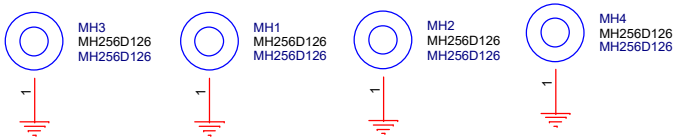


System Reset





Mounting Holes / Non-PTH



AAEON an ASUS assoc. co.

Title: Auto Power Button/Power in

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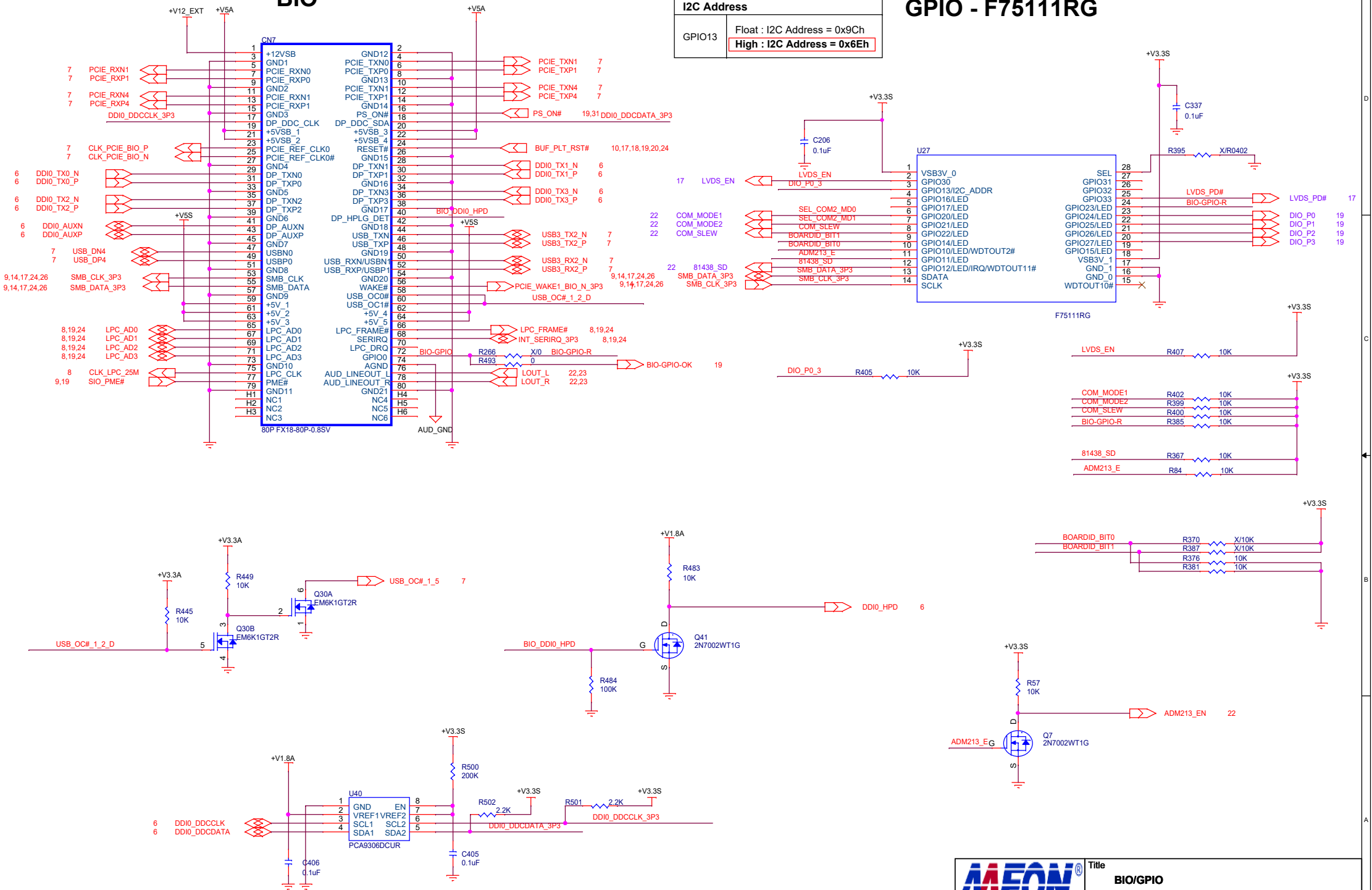
BIO

GPIO - F75111RG

I2C Address	
GPIO13	Float : I2C Address = 0x9Ch
	High : I2C Address = 0x6Eh



Title	**BIO/GPIO**
Size: Custom	Document Number: **PICOAPL1A10**
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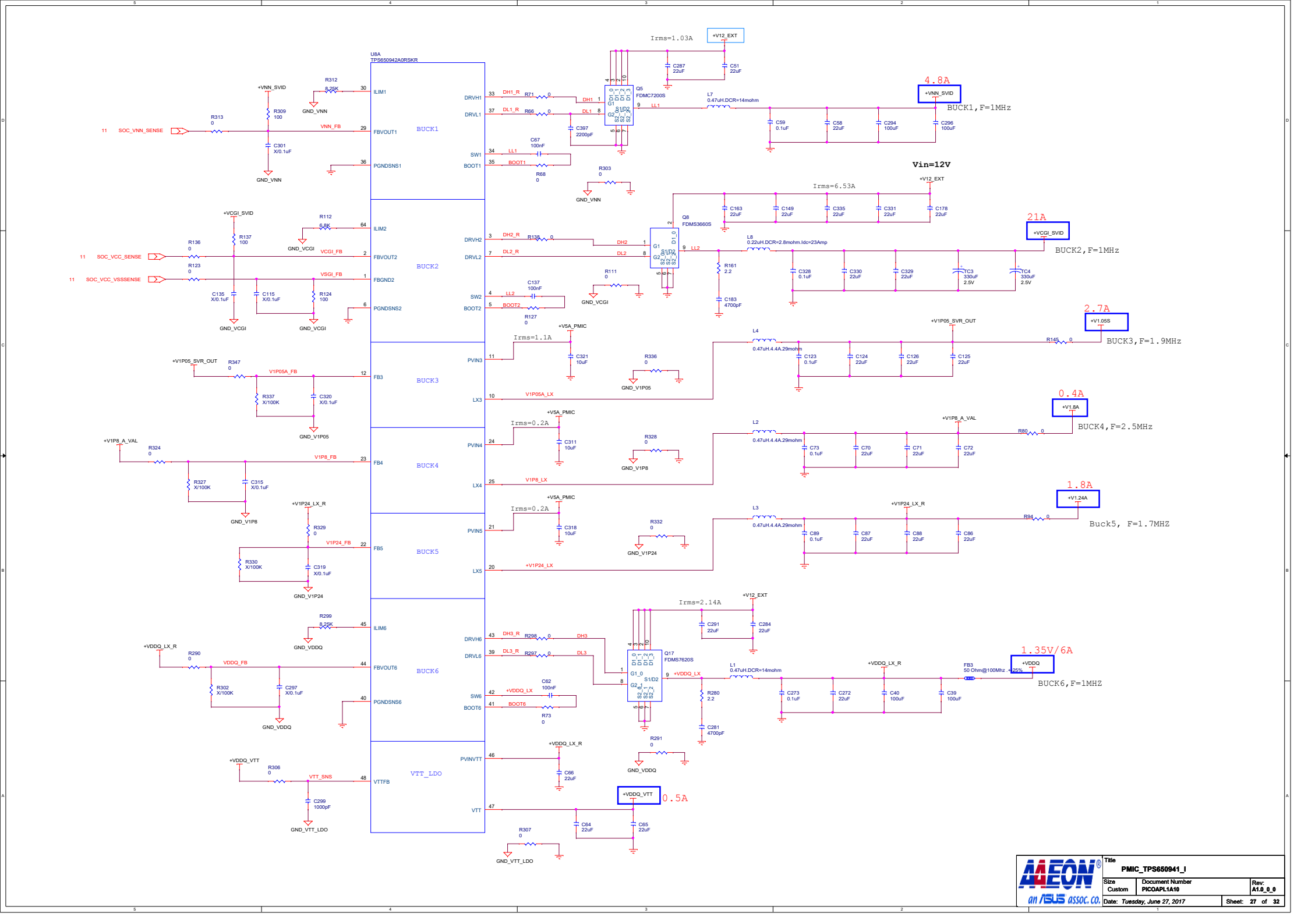
AAEON an ASUS assoc. co.



Title	PMIC_TPS650941_I		
Size: Custom	Document Number: PICOAPL1A10	Rev: A1.0_0_0	
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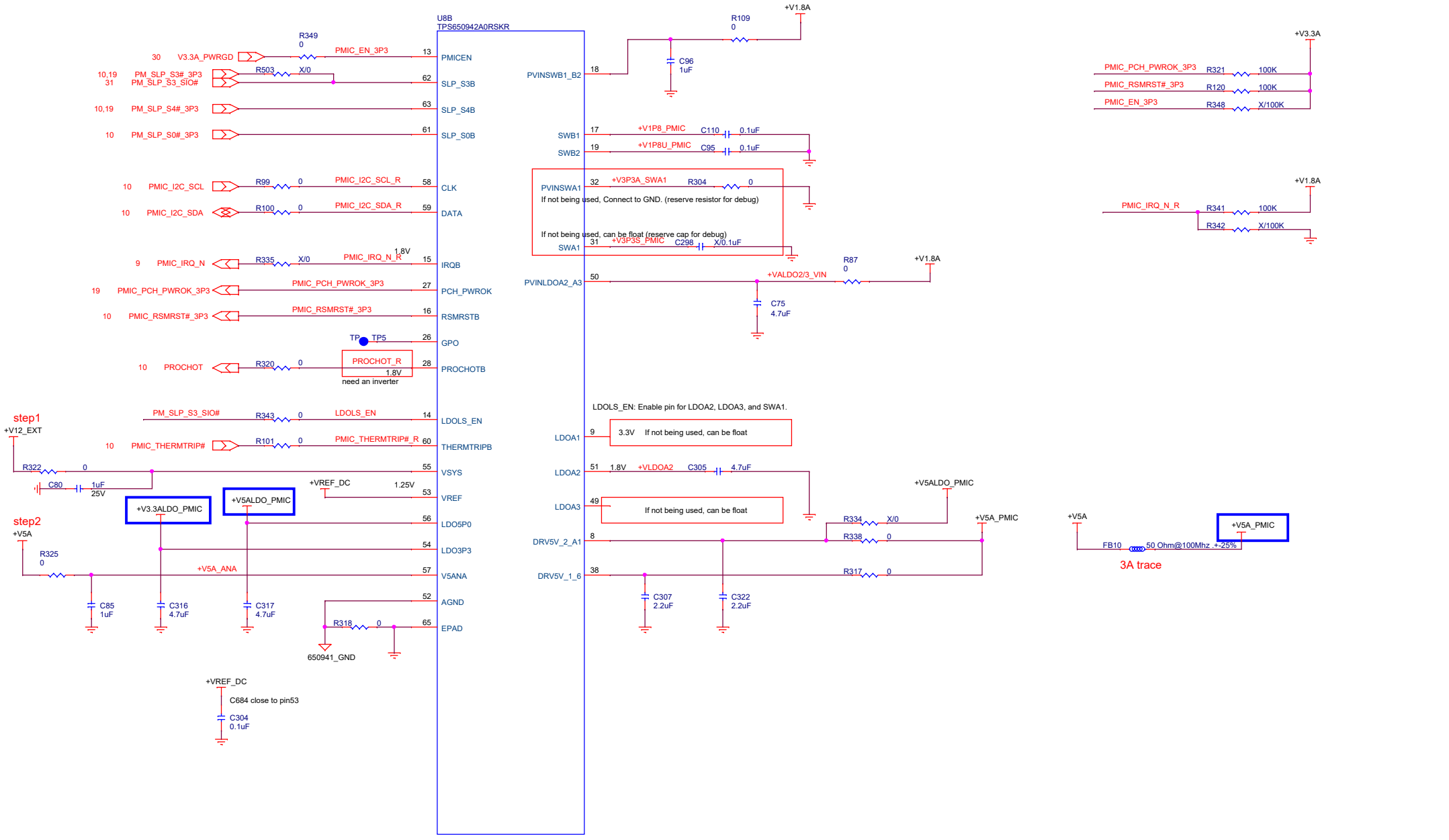
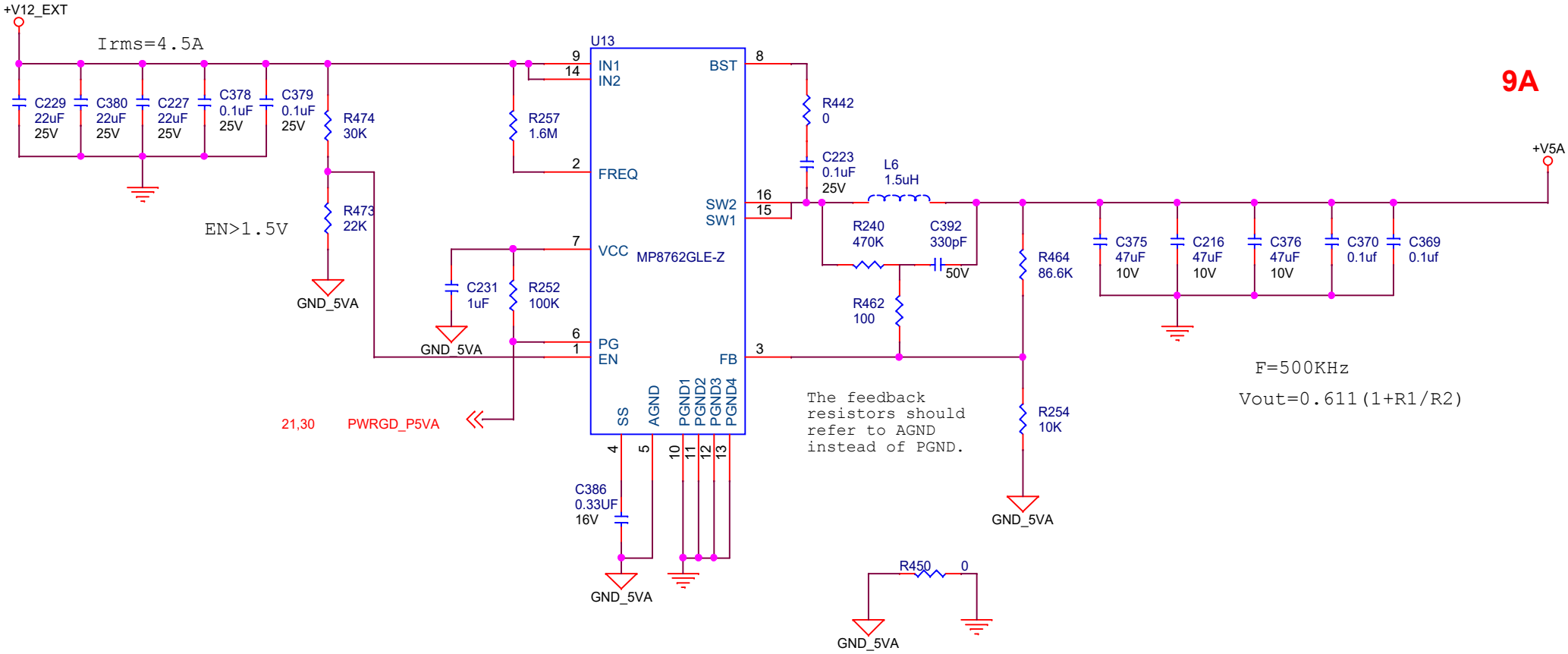


AAEON an ASUS assoc. co.	Title: PMIC_TPS650941_II	
	Size: Custom	Document Number: PICOAPL1A10 — Rev: A1.0_0_0
	Date: Tuesday, June 27, 2017	Sheet: 28 of 32



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Title: **Power VR : +V5A**		
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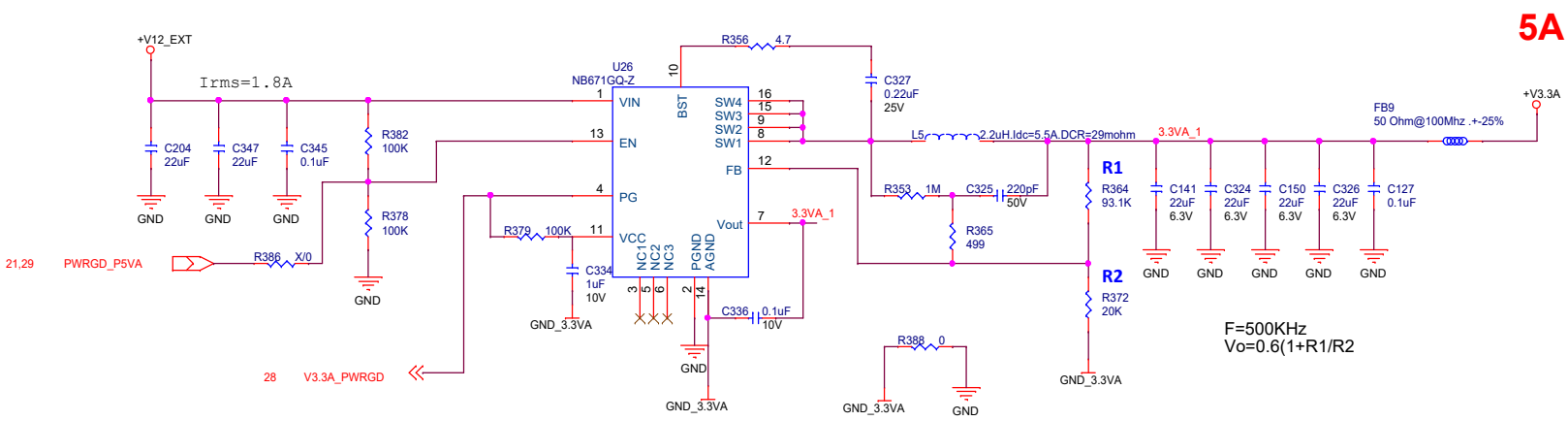
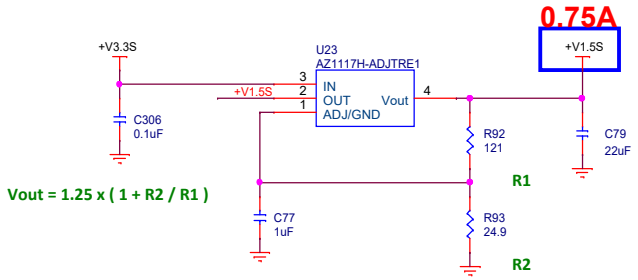
1.35V<EN<12V
EN voltage should be lower than 12V





AAEON an ASUS assoc. co.	Title: Power VR : +V3.3A.+V1.5S	
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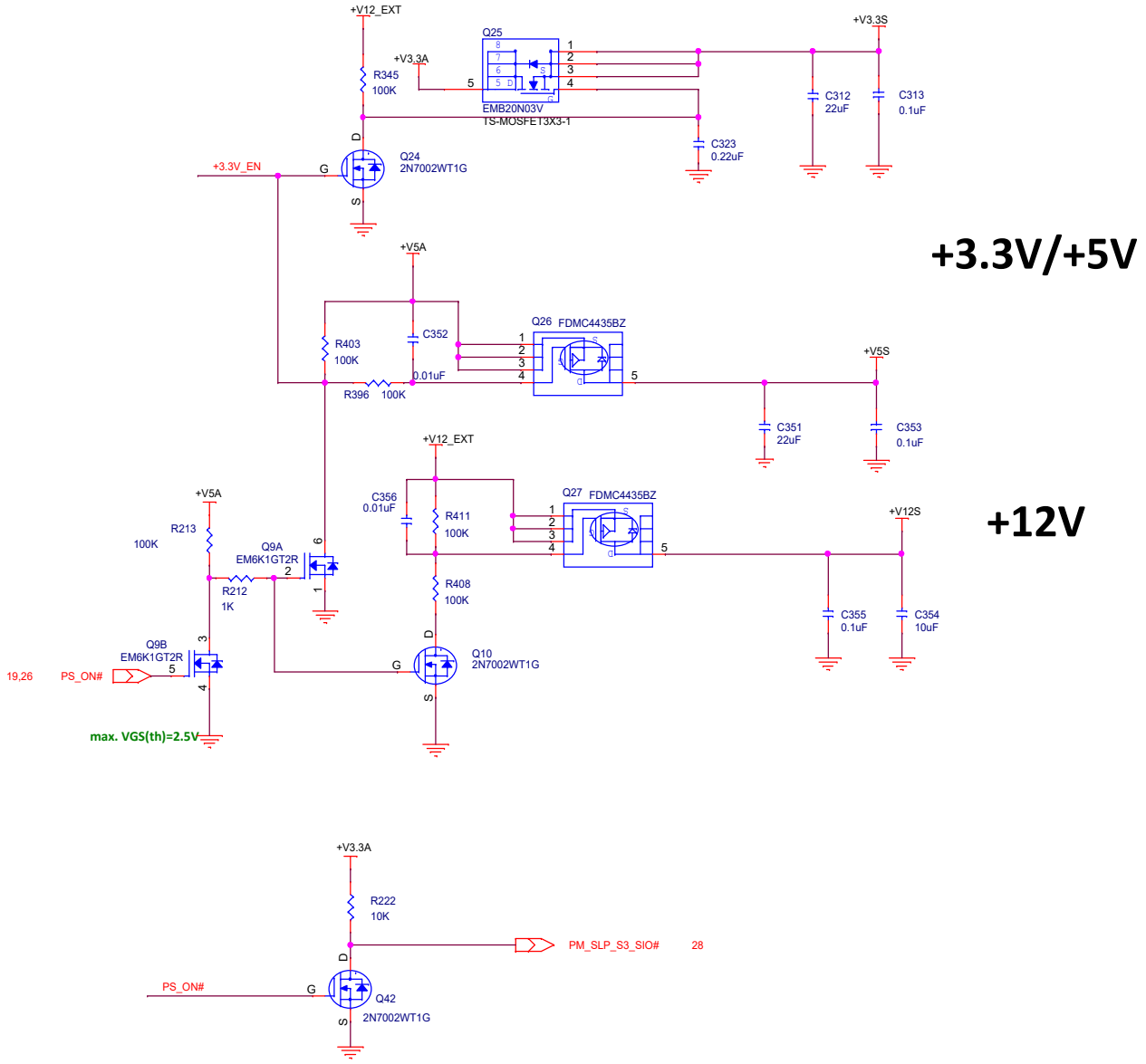

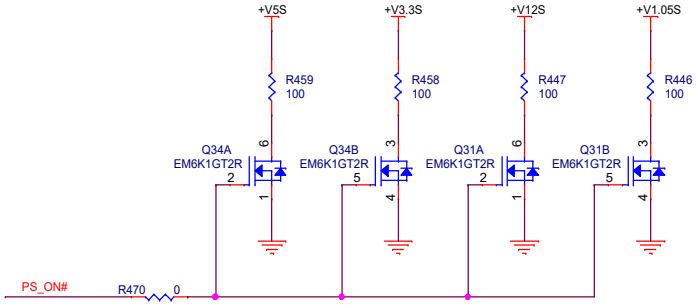

<Variant Name>

AAEON an ASUS assoc. co.	Title: **Power Sequence Logic**	
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HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2016/3/20	A0.1	First Release.	1-31	Daniel	Chienkow
2	2017/1/5	A0.2	1.Add R72 for BIO-GPIO-OK_R pull up Page19 2.Add R477 for pwrbtn/psout pull up Page19 3.Add R55,R20 for spi resister Page24 4.Add GPIO for pwrbtn(Q38.R475) Page09 5.Remove R102,R361 for 422/485 resister Page22 6.Add I2C to LPC connector Page24,26 7.Add Q40 for SATA LED Page22 8.Add R491,R492 for PCIE_CLKRQ2# PCIE_CLKRQ3# Page20 9.Enable USB by +5VAPWRGD Page21 10.Add U34,CN19 for USB port Page21 11.Add Q41 for DDI0_HPD Page26 12.Add PCIE port4 to BIO connector Page26 13.Add 2200pf(1124522290) at DL1 to GND for glitch adjust 14.Change R464,L6 for +V5A output voltage adjust. Page29 15.Change R112,R299,R312 for OCP adjust. Page27 16.Add C397 for VNN_SVIDglitch adjust. Page27	1-31	Daniel	Chienkow
3	2017/5/18	A0.3	1add power on reisiter(R498) 2LPC CN18change to 1655812130 (TF)WAFER BOX.12P.90D(M).SMD.1.0mm.W/Cap.PINREX.710-74-12TWR6 3.reverse pson(Q42) 4.DDICLK DDIDAT level shift(U40) 5.I2C level shift(U39) 6.BSS138 SPI(Q14) 7.PCH_PWROK to spi(R499) 8.LPC level shift(U50 U51)	1-31	Daniel	Chienkow

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Title: Revision History

Size	Document Number	Rev:
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