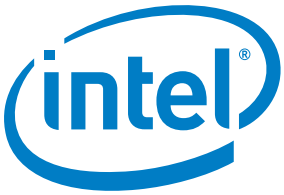


Intel Atom® E3900 and A3900 Processor Series

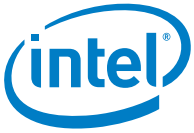
External Design Specification (EDS) Addendum

July 2017

Revision 2.0

Intel Confidential

Document Number: 558402-2.0



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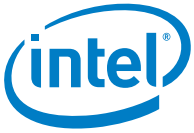

Revision History

Date	Revision	Description
July 2017	2.0	• Removed eMMC signals and Hardware Strap section as eMMC boot feature has been dropped. • Updated Table 14 with voltage range 0.8V to 1.5V. • Added A3900 series info. • Changed “SoC” wording to “processor”. • Updated Table 5. • Added Table 3 and Table 22. • Section 3.1, added note to mention cache parity and ECC support. • Updated Table 25.
April 2017	1.8	• Updated Table 2 with S state power. • Added Section 3.7 Time Coordinated Computing (TCC). • Added Figure 1 SoC Block Diagram. • Updated Table 20 on LPDDR4 VDDQ. • Added Table 7 PCI Device ID. • Added Section 2.8 RTC Signals. • Removed A3900 series information, to be added in the newly created A3900 Series EDS Addendum.
December 2016	1.71	• Section 3.1, renamed System Agent L2 Cache to CPU L2 Cache. • Fixed the typo in Table 20 (VNN_SCID to VNN_SVID). • Updated Table 1.
November 2016	1.7	• Updated product name to Intel Atom Processor E3900 Series, formally known as Apollo Lake-I SoC • Updated Table 2. • Added Table 4 (Split Automotive SKU into a separate table) • Updated Table 6 (added QS DCL and MOW Achieve) • Updated Table 18 (I_{CCMAX} for VCC_VCGI to refer to Table 20 and Table 21) • Added Table 19 and Table 20 for VCC_VCGI I_{CCMAX}.
July 2016	1.6	• Updated Table 2, Table 14, and Chapter 4.0 Apollo Lake I Ball Map, SoC Pin Locations, and SoC Package Design. • Added Section 2.6 Hardware Straps and Chapter 4.0 Electrical Specifications.
April 2016	1.5	• Section 2.4 Audio Interface Signals, 2.5 Serial I/O (SIO) (LPSS) SPI Signals
February 2016	1.1	• Updated Table 1, Section 1.2, and Chapter 4.0.

Date	Revision	Description
		• Added Section 2.4, 2.5 and 2.6.
November 2015	1.0	• Updated Section 1.0 Introduction and Chapter 5.0 Apollo Lake-I SoC Pin Naming and Symbols. • Updated Table 1, Table 6, Table 7, Table 8, and Table 11. • Removed some LPDDR4 information.
June 2015	0.7	• Added a guide for LPDDR, SDIO, and other registry information in the Introduction section. • Updated Figure 1. • Updated Table 1, Table 4, and Table 7. • Added Table 15 (SDIO features) and Table 16 (SDIO working modes). Renamed Chapter 4.0 title.
May 2015	0.6	• Updated Table 1, Table 8, and Table 9. • Added SDIO information.
May 2015	0.5	Initial release.

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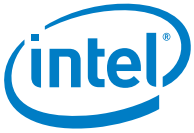


1.0 Introduction

This External Design Specification (EDS) Addendum is a supplement to the Intel® Pentium® and Celeron® Processor N- and J- Series (formerly known as Apollo Lake) External Design Specification. This Addendum contains additional information pertinent to the implementation and operation of the Intel Atom® processor E3900 and A3900 series (formerly known as Apollo Lake-I SoC).

The processor is the Intel® architecture processor that integrates the next-generation Intel processor core, graphics, memory controller, and I/O interfaces into a single system-on-chip solution.

Register information for the Intel Atom® E3900 and A3900 processors series is the same as of the N- and J- Series Processors. Refer to *Intel® Pentium® and Celeron® Processor N- and J- Series External Design Specification (EDS) Volume 2 of 4* (Document ID 557556) and *Intel® Pentium® and Celeron® Processor N- and J- Series External Design Specification (EDS) Volume 3 of 4* (Document ID 557557).

Table 1. Intel Atom® E3900 and A3900 Processor Series Features

Interface	Category	Intel Atom® E3900 and A3900 Processor Series
CPU	Number of Cores	Refer to Table 2 and Table 3 for details
	Burst Speed	Refer to Table 2 and Table 3 for details
	LFM/HFM	Refer to Table 2 and Table 3 for details
	Junction Temperature Tj	-40 to 110°C
	Temperature Tcase (E3930)	-40 to 103°C
	Temperature Tcase (E3940)	-40 to 100°C
	Temperature Tcase (E3950)	-40 to 98°C
Package	Type	Same as the N- and J- Series Processors
	I/O Count	Same as the N- and J- Series Processors
	Ball Count	Same as the N- and J- Series Processors
	Minimum Ball Pitch	Same as the N- and J- Series Processors
	Z-height (Pre-SMT)	2.426 mm ±0.113 mm
	Integrated Heat Spreader	Yes
Graphics	Generation	Same as the N- and J- Series Processors
	Frequency	Refer to Table 2 and Table 3 for details
	Execution Units	Refer to Table 2 and Table 3 for details
Display	MIPI*-DSI Ports	Same as the N- and J- Series Processors

Interface	Category	Intel Atom® E3900 and A3900 Processor Series
Display Cont.	Maximum MIPI*-DSI Resolution	Same as the N- and J- Series Processors
	Maximum DSI Data Rate	Same as the N- and J- Series Processors
	DDI Ports (External)	Same as the N- and J- Series Processors
	Maximum DDI (External) Resolution	Same as the N- and J- Series Processors
	Embedded DisplayPort* (eDP*) Ports	Same as the N- and J- Series Processors
	Maximum eDP Resolution	Same as the N- and J- Series Processors
	Maximum DDI Data Rate	Same as the N- and J- Series Processors
Memory	Interface	Up to 2x64 DDR3L (Non-ECC) Up to 2x72 DDR3L (ECC) Up to 4x32 Low-Power Double Data Rate memory technology (LPDDR4) (non-ECC)
	Supported Transfer Data Rates (MT/s)	DDR3L: Same as the N- and J- Series Processors DDR3L ECC: 1333/1600 MT/s LPDDR4: Same as the N- and J- Series Processors
Imaging (CSI D-PHY 1.1)	Number of Lanes	Same as the N- and J- Series Processors
	Speed	Same as the N- and J- Series Processors
	Still and Video	Same as the N- and J- Series Processors
	Maximum Vector Unit	Same as the N- and J- Series Processors
Imaging (CSI D-PHY 1.2)	Number of Lanes	Same as the N- and J- Series Processors
	Speed	Same as the N- and J- Series Processors
Imaging (CSI D-PHY 1.2) Cont.	Still and Video	Same as the N- and J- Series Processors
	Maximum Vector Unit	Same as the N- and J- Series Processors
Audio	Number of Ports	6x i2s 4x DMIC 1x HD Audio (HDA/mHDA Codec)
	Maximum i2s* Speed	Same as the N- and J- Series Processors
USB	SuperSpeed USB (USB 3.0) Ports	Same as the N- and J- Series Processors
	Maximum USB 3.0 Speed	Same as the N- and J- Series Processors
	USB 2.0 Ports	Same as the N- and J- Series Processors
	Maximum USB 2.0 Speed	Same as the N- and J- Series Processors
PCI Express* (PCIe*) Gen2	Number of Ports	Same as the N- and J- Series Processors

Interface	Category	Intel Atom® E3900 and A3900 Processor Series
PCI Express* (PCIe*) Gen2 Cont.	Maximum Speed	Same as the N- and J- Series Processors
Serial ATA* (SATA*) Gen3	Number of Ports	Same as the N- and J- Series Processors
	Maximum Speed	Same as the N- and J- Series Processors
Storage	SD* Card	Same as the N- and J- Series Processors
	Maximum SD Card Speed	Same as the N- and J- Series Processors
	eMMC*	Same as the N- and J- Series Processors
	Maximum eMMC Speed	Same as the N- and J- Series Processors
	Secure Digital I/O (SDIO)	1 port
	Maximum SDIO Speed	UHS-I at SDR 104/50/25/12 and DDR50
Low-Power subsystem (LPSS)	I^2C* Ports	Same as the N- and J- Series Processors
	Maximum I^2C Speed	Same as the N- and J- Series Processors
	High Speed UART (HSUART) (Maximum)	4 [1x Discrete GNSS (UART1), 1x Host OS Debug (UART2) and 2x Generic (UART0 and 3)]
Low-Power subsystem (LPSS) Cont.	Maximum HSUART Speed	Same as the N- and J- Series Processors
	Serial Peripheral Interface (SPI) (Maximum)	Controller: 3 Devices supported: 7
	Maximum SPI Speed	Same as the N- and J- Series Processors
Integrated Sensor Hub (ISH)	I^2C	Same as the N- and J- Series Processors
	Maximum I^2C Speed	Same as the N- and J- Series Processors
	GPIO	Same as the N- and J- Series Processors
Intel Legacy Block (iLB)	Fast SPI	Same as the N- and J- Series Processors
	Maximum Fast SPI Frequency	Same as the N- and J- Series Processors
Power Management Controller (PMC)	I^2C (PMIC)	Same as the N- and J- Series Processors
	Maximum I^2C Speed	Same as the N- and J- Series Processors
Low Pin Count (LPC)	Number of Ports	Same as the N- and J- Series Processors
	Maximum Speed	Same as the N- and J- Series Processors
System Management Bus (SMBus)	Number of Ports	Same as the N- and J- Series Processors
	Maximum Speed	Same as the N- and J- Series Processors

NOTE: Depending on Stock Keeping Unit (SKU).

1.1 SKU List

Table 2. Intel Atom® E3900 Processor Series SKU List

Processor	sSpec	MM#	Stepping	No. of Cores	Processor Frequency LFM/HFM/ Burst	Graphics Frequency LFM/HFM/ Burst	ISP Frequency Low/High/ Burst	GFX Industrial Reliability Frequency	GFX EU	TDP (W) at TjMax	S0i3 Power (mW) at 30°C	S3 Power (mW) at 30°C	S5 Power (mW) at 30°C	DDR3L ECC Option
Intel Atom® x5 E3930	R33Q	953086	D-0	2	800 MHz / 1.3 GHz / 1.8 GHz	100 MHz / 400 MHz / 550 MHz	200 MHz / 550 MHz / 675 MHz	400 MHz	12	6.5	15	13	13	Yes
Intel Atom® x5 E3940	R33M	953083	D-0	4	800 MHz / 1.6 GHz / 1.8 GHz	100 MHz / 400 MHz / 600 MHz	200 MHz / 550 MHz / 675 MHz	400 MHz	12	9.5	15	13	13	Yes
Intel Atom® x7 E3950	R33P	953085	D-0	4	800 MHz / 1.6 GHz / 2.0 GHz	100 MHz / 500 MHz / 650 MHz	200 MHz / 550 MHz / 700 MHz	400 MHz	18	12	18	16	16	Yes

Table 3. Intel Atom® A3900 Processor Series SKU List

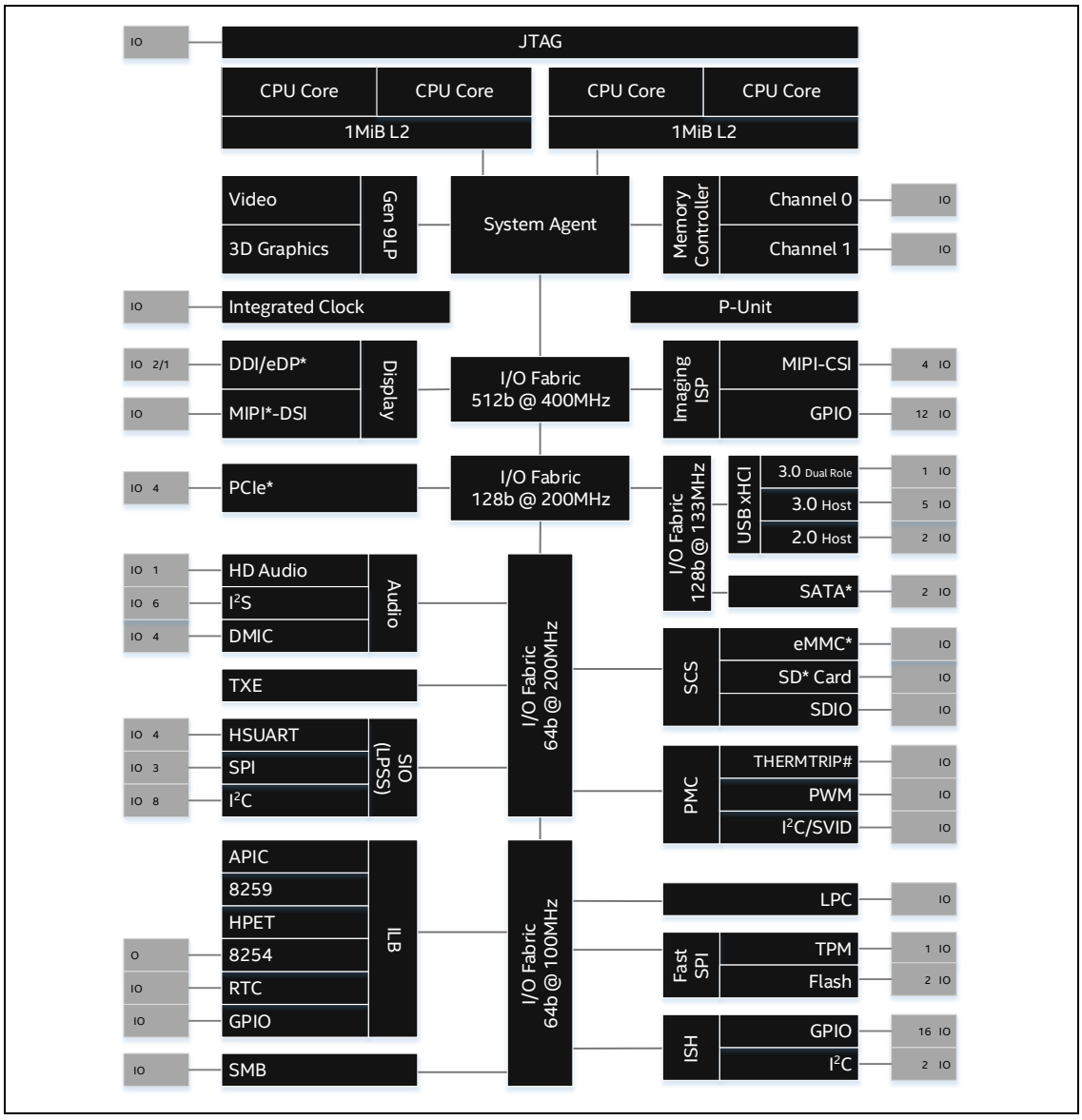
Note: Intel Atom® A3900 processor series are for automotive customers only. No support for non-automotive customer.

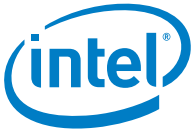
Processor	sSpec	MM#	Stepping	No. of Cores	Processor Frequency LFM/HFM/ Burst	Graphics Frequency LFM/HFM/ Burst	ISP Frequency Low/High/ Burst	GFX Industrial Reliability Frequency	GFX EU	TDP (W) at TjMax	S0i3 Power (mW) at 30°C	S3 Power (mW) at 30°C	S5 Power (mW) at 30°C	DDR3L ECC Option	AEC-Q100 Qualification
Intel Atom® x5 A3930	R33R	953087	D-0	2	800 MHz / 1.3 GHz / 1.8 GHz	100 MHz / 400 MHz / 550 MHz	200 MHz / 550 MHz / 675 MHz	NA	12	6	15	13	13	No	Yes
Intel Atom® x5 A3940	R33L	953082	D-0	4	800 MHz / 1.6 GHz / 1.8 GHz	100 MHz / 400 MHz / 600 MHz	200 MHz / 550 MHz / 675 MHz	NA	12	8	15	13	13	No	Yes

Processor	sSpec	MM#	Stepping	No. of Cores	Processor Frequency LFM/HFM/ Burst	Graphics Frequency LFM/HFM/ Burst	ISP Frequency Low/High/ Burst	GFX Industrial Reliability Frequency	GFX EU	TDP (W) at TjMax	S0i3 Power (mW) at 30°C	S3 Power (mW) at 30°C	S5 Power (mW) at 30°C	DDR3L ECC Option	AEC-Q100 Qualification
Intel Atom® x7 A3950	R33N	953084	D-0	4	800 MHz / 1.6 GHz / 2.0 GHz	100 MHz / 500 MHz / 650 MHz	200 MHz / 550 MHz / 700 MHz	NA	18	9.5	18	16	16	No	Yes
Intel Atom® x7 A3960	R33U	953096	D-0	4	800 MHz / 1.9 GHz / 2.4 GHz	100 MHz / 600 MHz / 750 MHz	200 MHz / 550 MHz / 700 MHz	NA	18	12.5	18	12	12	No	Yes

1.2 Processor Block Diagram

Figure 1. Processor Block Diagram





1.3 Terminology

Table 4. Terminology

Term	Description
DMIC	Digital Microphone
DQS	Data Strobe
ECC	Error Correcting Code
eDP*	Embedded DisplayPort
GNSS	Global Navigation Satellite System
HDMI*	High Definition Multimedia Interface
HSUART	High Speed UART
iLB	Intel Legacy Block
LPC	Low Pin Count
LPDDR	Low-Power Double Data Rate memory technology
LPSS	Low-Power subsystem
PCIe*	PCI Express*
PMC	Power Management Controller
PMIC	Power Management Integrated Circuit
RTC	Real Time Clock
SATA*	Serial ATA
SDIO	Secure Digital I/O
SDRAM	Synchronous Dynamic Random Access Memory
SIO	Serial I/O
SKU	Stock Keeping Unit
SMBus	System Management Bus
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Protocol
UART	Universal Asynchronous Receiver/Transmitter

1.4 Reference Documents

Table 5. Reference Documents

Document	Document No./Location
Intel® Pentium® and Celeron® Processor N- and J- External Design Specification (EDS) Volume 1 of 4	557555
Intel® Pentium® and Celeron® Processor N- and J- Series External Design Specification (EDS) Volume 2 of 4	557556
Intel® Pentium® and Celeron® Processor N- and J- Series External Design Specification (EDS) Volume 3 of 4	557557
Intel® Pentium® and Celeron® Processor N- and J- Series External Design Specification (EDS) Volume 4 of 4	559360
Intel Pentium and Celeron Processor N- and J- Series Design Guide	557775
Intel Atom® Processor E3900 and A3900 Series Platform Design Guide Addendum	558588
Apollo Lake-I IOTG Thermal and Mechanical Design Guide	568394
Manufacturing with the Intel® Mobile Products: Apollo Lake and Apollo Lake I	561676
IOTG Time Coordinated Computing SDK 1.0 for Apollo Lake-I	568821

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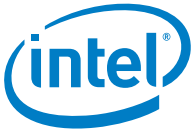


2.0 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and small size of the package, some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

2.1 PCI Device ID

Table 6. PCI Configuration Matrix

Device ID	Device Description	Device	Function
0x5ABC	UART 0	24	0
0x5AEE	UART 3	24	3
0x5AC4	SPI 1	25	1
0x5AC6	SPI 2	25	2
0x5AD0	SDIO	30	0

NOTE: Other PCI Device IDs are the same as the N- and J- Series Processors. Refer to Intel® Pentium® and Celeron® Processor N- and J- Series External Design Specification (EDS) Volume 1 of 4 (Document ID# 557555).

2.2 Memory Interface Signals

Table 7. DDR3L ECC System Memory Signals

Signal Name	Dir.	I/O Voltage	Type	Description
MEM_CH0_ECC_DQ[7:0] MEM_CH1_ECC_DQ[7:0]	I/O	VDDQ	DDR3L PHY	**ECC Data Buses:** Data signals interface to the Synchronous Dynamic Random Access Memory (SDRAM) data buses.
MEM_CH0_ECC_DQSP[8] MEM_CH0_ECC_DQSN[8] MEM_CH1_ECC_DQSP[8] MEM_CH1_ECC_DQSN[8]	I/O	VDDQ	DDR3L PHY	**ECC Data Strobes (DQS):** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.

NOTE: Signal names shown in this table are additional ECC signal names. The rest of the DDR3L signals are the same as the N- and J- Series Processors.

2.3 SDIO Interface Signals

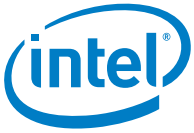
Table 8. SDIO Interface Signals

Signal Name	GPIO	Dir.	I/O Voltage	Type	Description
SDIO_CLK	GPIO_166	I/O	V1P8	GPIO	**SDIO Clock:** Port Clock.
SDIO_CMD	GPIO_171	I/O	V1P8	GPIO	**SDIO Command:** This signal is used for device initialization and transfer of commands.
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	GPIO_167 GPIO_168 GPIO_169 GPIO_170	I/O	V1P8	GPIO	**SDIO Data Bits 0 to 3:** Bidirectional ports used to transfer data to and from the SDIO device. By default, after power-up or reset, only D [0] is used for data transfer. A wider data bus can be configured for data transfer, using D [0]-D [3].
SDIO_PWR_DOWN_N	GPIO_183	I/O	V1P8	GPIO	**SDIO Bus Power:** Controls power for SDIO devices.

2.4 High-Speed Universal Asynchronous Receiver/Transmitter (UART) Interface Signals

Table 9. UART Interface Signals

Signal Name	GPIO#	Dir.	I/O Voltage	Type	Description
LPSS_UART0_RXD	GPIO_38	I	V1P8	GPIO	UART0 data input
LPSS_UART0_TXD	GPIO_39	O	V1P8	GPIO	UART0 data output
LPSS_UART0_RTS_N	GPIO_40	O	V1P8	GPIO	UART0 Ready to Send
LPSS_UART0_CTS_N	GPIO_41	I	V1P8	GPIO	UART0 Clear to Send
LPSS_UART1_RXD	GPIO_42	I	V1P8	GPIO	UART1 data input



Signal Name	GPIO#	Dir.	I/O Voltage	Type	Description
LPSS_UART1_TXD	GPIO_43	O	V1P8	GPIO	UART1 data output
LPSS_UART1_RTS_N	GPIO_44	O	V1P8	GPIO	UART1 Ready to Send
LPSS_UART1_CTS_N	GPIO_45/GPIO153 (Fn 3)	I	V1P8	GPIO	UART1 Clear to Send
LPSS_UART2_RXD	GPIO_46/GPIO_150 (Fn 3)	I	V1P8	GPIO	UART2 data input
LPSS_UART2_TXD	GPIO_47/GPIO_151 (Fn 3)	O	V1P8	GPIO	UART2 data output
LPSS_UART2_RTS_N	GPIO_48/GPIO_152 (Fn3)	O	V1P8	GPIO	UART2 Ready to Send
LPSS_UART2_CTS_N	GPIO_49	I	V1P8	GPIO	UART2 Clear to Send
LPSS_UART3_RXD	GPIO_112	I	V1P8	GPIO	UART3 data input
LPSS_UART3_TXD	GPIO_113	O	V1P8	GPIO	UART3 data output
LPSS_UART3_RTS_N	GPIO_116	O	V1P8	GPIO	UART3 Ready to Send
LPSS_UART3_CTS_N	GPIO_117	I	V1P8	GPIO	UART3 Clear to Send

NOTES:

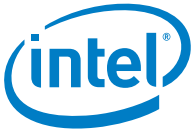
1. The E3900 and A3900 Series Processors support four LPSS_UART ports while the N- and J- Series Processors support only LPSS_UART [2:1] ports.
2. The LPSS_UART1 port is dedicated for discrete Global Navigation Satellite System (GNSS). This port can be used for generic UART functionality if GNSS is not used.
3. The LPSS_UART2 port is dedicated for host OS debug.
4. The LPSS_UART0 and LPSS_UART3 ports are for generic UART functionality.

2.5 Audio Interface Signals

Table 10. Audio Interface Signals

Signal Name	GPIO#	Dir.	I/O Voltage	Type	Description
AVS_I2S1_MCLK	GPIO_74	O	V1P8	GPIO	MCLK for Master Mode operation or GPIO
AVS_I2S1_BCLK	GPIO_75	I/O	V1P8	GPIO	Analog microphone i2s Bit Clock – bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input.

Signal Name	GPIO#	Dir.	I/O Voltage	Type	Description
AVS_I2S1_WS_SYNC	GPIO_76	I/O	V1P8	GPIO	Word Select or SYNC input – marks the beginning of serial sample.
AVS_I2S1_SDI	GPIO_77	I	V1P8	GPIO	Analog microphone i2s Data in – serial data input
AVS_I2S1_SDO	GPIO_78	I/O	V1P8	GPIO	Audio Codec i2s Data out – serial data output
AVS_I2S2_MCLK	GPIO_84	O	V1P8	GPIO	MCLK for Master Mode operation or GPIO
AVS_I2S2_BCLK	GPIO_85	I/O	V1P8	GPIO	Analog microphone i2s Bit Clock – bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input.
AVS_I2S2_WS_SYNC	GPIO_86	I/O	V1P8	GPIO	Word Select or SYNC input – marks the beginning of serial sample.
AVS_I2S2_SDI	GPIO_87	I	V1P8	GPIO	Analog microphone i2s Data in – serial data input
AVS_I2S2_SDO	GPIO_88	I/O	V1P8	GPIO	Audio Codec i2s Data out – serial data output
AVS_I2S3_BCLK	GPIO_89	I/O	V1P8	GPIO	Audio Codec i2s Bit Clock – bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input.
AVS_I2S3_WS_SYNC	GPIO_90	I/O	V1P8	GPIO	Audio Codec frame synchronization or word select signal. Bidirectional – may be configured for master or slave.
AVS_I2S3_SDI	GPIO_91	I	V1P8	GPIO	Audio Codec I^2S Data in – serial data input
AVS_I2S3_SDO	GPIO_92	I/O	V1P8	GPIO	Audio Codec I^2S Data out – serial data output



Signal Name	GPIO#	Dir.	I/O Voltage	Type	Description
AVS_I2S4_BCLK	GPIO_79	I/O	V1P8	GPIO	Audio Codec I²S Bit Clock – bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input.
AVS_I2S4_WS_SYNC	GPIO_80	I/O	V1P8	GPIO	Audio Codec frame synchronization or word select signal. Bi-directional – may be configured for master or slave.
AVS_I2S4_SDI	GPIO_81	I	V1P8	GPIO	Audio Codec I²S Data in – serial data input
AVS_I2S4_SDO	GPIO_82	I/O	V1P8	GPIO	Audio Codec I²S Data out – serial data output
AVS_I2S5_BCLK	GPIO_150	I/O	V1P8	GPIO	Audio Codec I²S Bit Clock – bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input.
AVS_I2S5_WS_SYNC	GPIO_151	I/O	V1P8	GPIO	Audio Codec frame synchronization or Word select signal. Bi-directional – may be configured for master or slave
AVS_I2S5_SDI	GPIO_152	I	V1P8	GPIO	Audio Codec I²S Data in – serial data input
AVS_I2S5_SDO	GPIO_153	I/O	V1P8	GPIO	Audio Codec I²S Data out – serial data output
AVS_I2S6_BCLK	GPIO_146	I/O	V1P8	GPIO	Audio Codec I²S Bit Clock – bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input.
AVS_I2S6_WS_SYNC	GPIO_147	I/O	V1P8	GPIO	Audio Codec frame synchronization or Word select signal. Bi-directional – may be configured for master or slave.
AVS_I2S6_SDI	GPIO_148	I	V1P8	GPIO	Audio Codec I²S Data in – serial data input

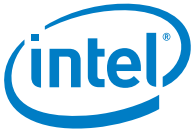
Signal Name	GPIO#	Dir.	I/O Voltage	Type	Description
AVS_I2S6_SDO	GPIO_149	I/O	V1P8	GPIO	Audio Codec I^2S Data out – serial data output

NOTE: The E3900 and A3900 Series Processors support six I^2S interfaces while the N- and J- Series Processors support only AVS_I2S2 and AVS_I2S6 interfaces.

2.6 Serial I/O (SIO) (LPSS) SPI Signals

Table 11. SIO (LPSS) SPI Signals

Signal Name	GPIO	Dir.	I/O Voltage	Type	Description
SIO_SPI_0_CLK	GPIO_104	I/O	V1P8	GPIO	**SIO SPI 0 Clock:** SPI Clock signal
SIO_SPI_0_FS0	GPIO_105	O	V1P8	GPIO	**SIO SPI 0 Frame Select 0:** Used as the SPI bus request signal
SIO_SPI_0_FS1	GPIO_106	O	V1P8	GPIO	**SIO SPI 0 Frame Select 1:** Used as the SPI bus request signal
SIO_SPI_0_RXD	GPIO_109	I	V1P8	GPIO	**SIO SPI 0 Data Pad:** Data Input pin for the processor
SIO_SPI_0_TXD	GPIO_110	O	V1P8	GPIO	**SIO SPI 0 Data Pad:** Data Output pin for the processor
SIO_SPI_1_CLK	GPIO_111	I/O	V1P8	GPIO	**SIO SPI 1 Clock:** SPI Clock signal
SIO_SPI_1_FS0	GPIO_112	O	V1P8	GPIO	**SIO SPI 1 Frame Select 0:** Used as the SPI bus request signal
SIO_SPI_1_FS1	GPIO_113	O	V1P8	GPIO	**SIO SPI 1 Frame Select 1:** Used as the SPI bus request signal
SIO_SPI_1_RXD	GPIO_116	I	V1P8	GPIO	**SIO SPI 1 Data Pad:** Data Input pin for the processor
SIO_SPI_1_TXD	GPIO_117	O	V1P8	GPIO	**SIO SPI 1 Data Pad:** Data Output pin for the processor
SIO_SPI_2_CLK	GPIO_118	I/O	V1P8	GPIO	**SIO SPI 2 Clock:** SPI Clock signal
SIO_SPI_2_FS0	GPIO_119	O	V1P8	GPIO	**SIO SPI 2 Frame Select 0:** Used as the SPI bus request signal



Signal Name	GPIO	Dir.	I/O Voltage	Type	Description
SIO_SPI_2_FS1	GPIO_120	O	V1P8	GPIO	**SIO SPI 2 Frame Select 1:** Used as the SPI bus request signal
SIO_SPI_2_FS2	GPIO_121	O	V1P8	GPIO	**SIO SPI 2 Frame Select 2:** Used as the SPI bus request signal
SIO_SPI_2_RXD	GPIO_122	I	V1P8	GPIO	**SIO SPI 2 Data Pad:** Data Input pin for the processor
SIO_SPI_2_TXD	GPIO_123	O	V1P8	GPIO	**SIO SPI 2 Data Pad:** Data Output pin for the processor

NOTE: The E3900 and A3900 Series Processors support three SPI ports while the N- and J- Series Processors support only the SIO_SPI_0 port.

2.7 GPIO Multiplexing

Table 12. GPIO Multiplexing

GPIO No.	Signal Name	Processor Pin No.	Community	Community Offset	I/O Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_20	GPIO_20	B27	N	320	1.8 V	20K PD	HSMV	GP-In	0	0	0	0	IERR	0
GPIO_21	GPIO_21	C26	N	336	1.8 V	20K PD	HSMV	GP-In	0	0	0	0	MCERR	0

2.8 RTC Signals

In addition to the internal RTC oscillator, an optional mode is available to supply the RTC clock from an external source. In this case, an oscillator or a single clock output can be used to drive into X1 with X2 left as no contact. Refer to *Intel Atom® Processor E3900 and A3900 Series Platform Design Guide Addendum* (Document ID# 558588) for this implementation.

Table 13. RTC Signals

Signal Name	Dir.	I/O Voltage	Type	Description
RTC_X1	I	NA	RTC PHY	Crystal Input 1: This signal is connected to a 32.768 kHz crystal (max 50K ESR). If using an external oscillator, the RTC_X1 Vih must be within the range of 0.8V to 1.5V (1.5V max).
RTC_X2	O	NA	RTC PHY	Crystal Input 2: This signal is connected to a 32.768 kHz crystal (Max 50K ESR). If using an external oscillator, RTC_X2 should be left floating.

2.9 Other Signals

Other signals not mentioned in this document, such as Digital Display Interface and SVID, have the same names as those used in the *Intel® Pentium® and Celeron® Processor N- and J- Series (Formerly Apollo Lake) External Design Specification (EDS)* Volume 1 of 4 (Document ID# 557555).

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3.0 Functional Description

3.1 Processor Core Overview

The processor core for Intel Atom® E3900 and A3900 processor series (formerly known as Apollo Lake-I) is the same as the processor core for Intel® Pentium® and Celeron® Processor N- and J- Series (formerly known as Apollo Lake). Figure 2 and Figure 3 show the CPU L2 Cache structure for the dual-core processor and the quad-core processor, respectively.

Note: L1 caches have Parity Protection and L2 cache has ECC Protection.

Figure 2. CPU L2 Cache Structure (Dual Core)

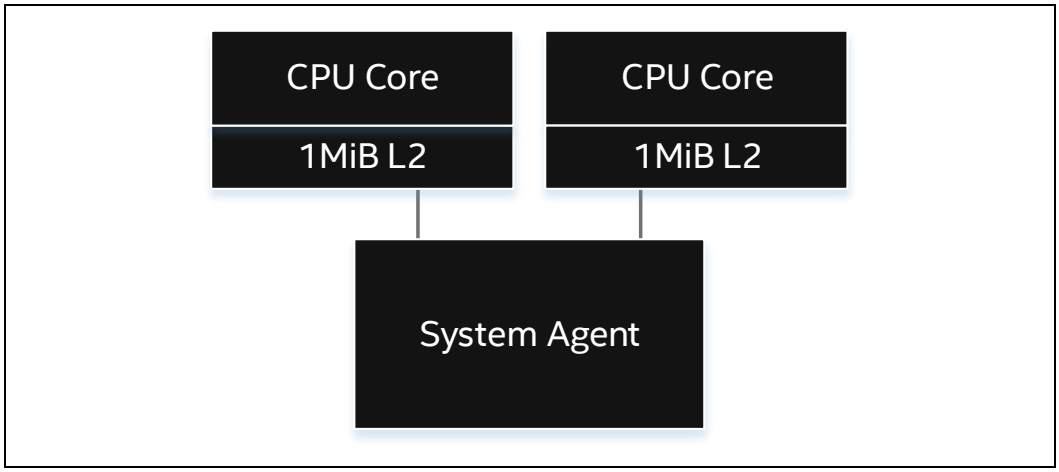
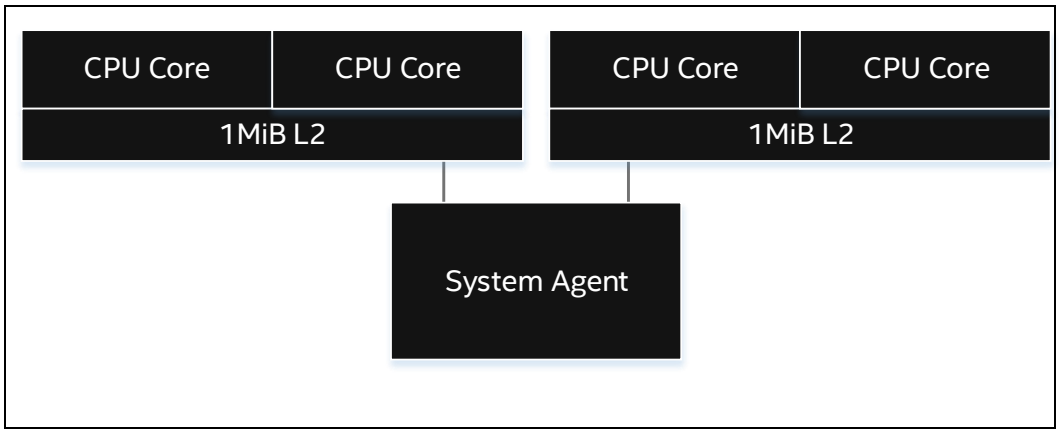


Figure 3. CPU L2 Cache Structure (Quad Core)



3.2 System Memory Controller

3.2.1 Supported Memory Overview

The processor Integrated Memory Controller (IMC) supports the following memory technologies on two independent 64-bit (72 bit for ECC) channels.

Table 14. Supported Memory Technologies

Technology Attributes	LPDDR4	DDR3L	DDR3L ECC
Channels	Up to 4 (x32)	Up to 2 (x64)	Up to 2 (x72)
Peak Bandwidth (GB/s)	Up to 38.4	Up to 29.86	Up to 25.6
Maximum Data Transfer Rate (MT/s)	NOTE	NOTE	1333/1600
Maximum Total System Capacity	NOTE	NOTE	8 GB
Raw Card Support	NOTE	NOTE	C(1Rx8) D(2Rx8)
Densities (GB)	NOTE	NOTE	4, 8
CMD/Adds pins per channel	NOTE	NOTE	16
DQ pins per channel	NOTE	NOTE	72
Voltage Rail (V)	NOTE	NOTE	1.35
Scrambling	Yes		
On Die Termination Control	Yes		
Same Rank Interleaving	Yes		
Refresh	No per bank-refresh, only at rank level		
Power-Saving Features	Fast Exit Power Down, Self-Refresh plus extra features, Power/Trunk gating		

NOTE: Same as the N- and J- Series Processors.

3.2.2 Memory Configurations

For further information, refer to the Memory Configurations section in *Intel® Pentium® and Celeron® Processor N- and J- Series (Formerly Apollo Lake) External Design Specification (EDS)* Volume 1 of 4 (Document ID# 557555).

Note: Disregard LPDDR3, the contents are not supported by the Intel Atom® E3900 and A3900 processor series.

3.3 SDIO

The processor has an integrated SDIO controller, which implements the following features.

Note: SD cards are not supported by this interface.

Table 15. SDIO Features

Category	Feature Supported
Specification	Supports SDIO Specification Version 3.00
Data Rate	Supports up to 104 MB/s data rate using 4 parallel data lines (SDR104 modes)
Transfer Modes	Supports transfer data in 1-bit and 4-bit SD modes
Mode of Operation	Supports both ADMA2/DMA and Non-DMA modes of operation
Cyclic Redundancy Check	Supports CRC7 for command and CRC16 for data integrity
Others	• Supports Async Interrupt Cards • Supports inband wake during S0 • Supports Interrupt Coalescing

Table 16. SDIO Working Modes

SDIO Mode	Data Rate	Maximum Clock Frequency	Maximum Data Throughput
Default Speed/SDR12(1)	Single	25 MHz	12.5 MB/s
High Speed/SDR25(2)	Single	50 MHz	25 MB/s
SDR50	Single	100 MHz	50 MB/s
DDR50	Dual	50 MHz	50 MB/s
SDR104	Single	208 MHz	104 MB/s

NOTES:
1. Default speed denotes 3.3-V signaling, SDR12 denotes 1.8-V signaling.
2. High speed denotes 3.3-V signaling, SDR25 denotes 1.8-V signaling.

3.4 Audio Controller

Table 17. Audio Controller Features

Category	Description
I2S/SSP Interfaces	Six I2S/SSP interfaces for platform peripherals
DSPs	Two high-performance DSPs configured with: • 32kB 4-way set associative L1 Instruction Cache • 64kB 4-way set associative L1 Data Cache
L2	• L2 memory controller with the local high-performance interconnect fabric • L2 cache controller with caching and prefetch capabilities
ROM Size	8kB ROM
DMA Interfaces	Two 8-channel universal DMA interfaces to transfer data between memory buffers and peripherals, and between memories
DMIC Interfaces	Two dual-channel DMIC interfaces
Intel® High Definition Audio (Intel® HD Audio) and LPE Audio	Supports Intel® HD Audio and LPE Audio for DDI [1:0] (DisplayPort* and High Definition Multimedia Interface (HDMI*))
CODEC	Supports one external CODEC for attaching audio peripherals
Burst Mode	Local power sequencer for burst-mode data processing in micropower modes (S0ix)
Debug Interface	DSP On-chip Debug interface with two JTAG ports

3.5 Serial I/O (SIO) (LPSS)

Table 18. I/O Supported Interfaces

Interface	Number of Ports	Maximum Speed
[SIO] I2C*	8	3.1 Mb/s
[SIO] HSUART	4	115,200 kb/s (standard 16550) 3.6864 Mb/s (high-speed 16750)
[SIO] SPI	3	25 Mb/s

3.6 Clocking

Table 19. Summary of Clock Signals

Interface	Clock Signal	Clock Frequency
Memory - DDR3L	NOTE	NOTE

Interface	Clock Signal	Clock Frequency
Memory - LPDDR4	NOTE	NOTE
PCIe*	NOTE	NOTE
Storage - eMMC* 4.51 and 5.0	NOTE	NOTE
Storage - SD Card	NOTE	NOTE
Storage - SDIO	SDIO_CLK	25, 50, 100, 208 MHz
Display - DisplayPort, HDMI	NOTE	NOTE
Display - MIPI*-DSI	NOTE	NOTE
Camera - MIPI-CSI	NOTE	NOTE
Audio - Intel® HD Audio	NOTE	NOTE
Audio Codec/Analog Microphone - I2S	AVS_I2S[1:6]_BCLK AVS_I2S[1:2]_MCLK	BCLK = <programmable> MCLK = <programmable>
Audio - Digital Microphone	NOTE	NOTE
SIO (LPSS) I2C	NOTE	NOTE
PMIC	NOTE	NOTE
SVID	NOTE	NOTE
LPC	NOTE	NOTE
SMBus	NOTE	NOTE
SIO (LPSS) SPI	SIO_SPI_[0:2]_CLK	25 MHz
FAST SPI - SPI NOR and TPM	NOTE	NOTE
SPI	NOTE	NOTE
Platform - OSC_CLK_OUT	NOTE	NOTE
Platform - SUSCLK	NOTE	NOTE
XTAL Source - RTC Clock	NOTE	NOTE
XTAL Source - processor Clock - as default	NOTE	NOTE

NOTE: Same as the N- and J- Series Processors.

3.7 Time Coordinated Computing (TCC)

Time Coordinated Computing (TCC) presents a new vector of compute, besides Power and Performance.

In the past, general purpose CPU design has focused on increasing throughput within a power envelope, often with the side effect of increased latencies and non-determinism of code execution in the system. For example, a cache miss will cause a piece of code to be non-deterministic, as a fetch from main memory becomes necessary.

TCC aims to address/reduce this by adding Time Synchronization and Real-Time (RT) features between and within CPU and Network.

Refer to *Time Sensitive Network Reference SW1.1* (Document ID# 568821) for Time Sensitive Networking (TSN) Reference SW, which covers the hardware capabilities together with the software components that are being used to enable the TCC.

3.8 Other Interfaces

For other interfaces that are not mentioned in this document, such as display controller, graphics and media engine, refer to *Intel® Pentium® and Celeron® Processor N- and J- Series (Formerly Apollo Lake) External Design Specification (EDS)* Volume 1 of 4 (Document ID# 557555).

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4.0 Electrical Specifications

Table 20 lists the Power Rail DC specifications and I_{CCMAX} for the processor. Table 23 and Table 24 list the DC and AC specifications, respectively, for SDIO. Refer to *Intel® Pentium® and Celeron® Processor N- and J- Series (Formerly Apollo Lake) External Design Specification (EDS)* Volume 1 of 4 (Document ID# 557555) for other electrical specifications.

4.1 Voltage and Current Specifications

Table 20. Power Rail DC Specifications and I_{CCMAX} Values

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	I_{CCMAX} (A)
VCC_VCGI	NOTE	With AVP: (NOTE) Without AVP: (NOTE)	NOTE	Refer to Table 21 and Table 22
VNN_SVID	NOTE (DDR3L)	NOTE	NOTE	4.4
	NOTE (LPDDR4)	NOTE	NOTE	2.9
VCCIOA	NOTE	NOTE	NOTE	Included in either VNN_SVID (DDR3L) or VDDQ (LPDDR4)
VCCRAM_1P05	NOTE	NOTE	NOTE	NOTE
VCCRAM_1P05_IO	NOTE	NOTE	NOTE	
VCC_1P05_INT	NOTE	NOTE	NOTE	
VDD2_1P24_GLM	NOTE	NOTE	NOTE	NOTE
VDD2_1P24_AUD_ ISH_ PLL	NOTE	NOTE	NOTE	
VDD2_1P24_MPHY	NOTE	NOTE	NOTE	
VDD2_1P24_USB2	NOTE	NOTE	NOTE	
VDD2_V1P24_DSI_CSI	NOTE	NOTE	NOTE	
VCC_1P8V_A	NOTE	NOTE	NOTE	NOTE
VDDQ	NOTE (DDR3L)	NOTE	NOTE	2.8
	NOTE (LPDDR4)	NOTE	NOTE	4.3
VCC_3P3V_A	NOTE	+5/-6.5%	NOTE	NOTE

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	I_{CCMAX} (A)
VCC_RTC_3P3V	3.3 (coin battery backed)	NOTE	NOTE	2 m (S0 state) 6 µ (G3 state)

NOTE: Same as the N- and J- Series Processors.

Table 21. Intel Atom® E3900 Processor Series V_{CC}_V_{CGI} Rail I_{CCMAX} Values

SKU Name	I_{CCMAX} (A)
E3950	16
E3940	15
E3930	10.5

Table 22. Intel Atom® A3900 Processor Series V_{CC}_V_{CGI} Rail I_{CCMAX} Values

SKU Name	I_{CCMAX} (A)
A3960	21
A3950	16
A3940	15
A3930	10.5

4.2 SDIO DC and AC Specifications

Table 23. SDIO Signal Group DC Specifications

Symbol	Parameter	Minimum Value	Maximum Value	Unit	Notes
VCC	I/O voltage	1.66	1.89	V	1.8 V nominal
VOH	Output high voltage	1.35	–	V	At 1.80 V nominal (Vcc-0.45), at 3 mA load.
VOL	Output low voltage	–	0.45	V	at -3 mA load
VIH	Input high voltage	1.17	–	V	at 1.80 V nominal (0.65xVcc)
VIL	Input low voltage	–	0.63	V	at 1.80 V nominal (0.35xVcc)
CL	Bus signal line capacitance	–	5	pF	–
IPAD	Pad leakage current	-5	5	µA	–

Symbol	Parameter	Minimum Value	Maximum Value	Unit	Notes
ZUP	Driver pull-up impedance	32	48	ohm	40 ohm nominal
ZDN	Driver pull-down impedance	32	48	ohm	40 ohm nominal
Wpup20K	Weak pull-up impedance 20 K	8	44	kohm	20 kohm nominal
Wpdn20K	Weak pull-down impedance 20 K	8	44	kohm	20 kohm nominal
Vhys	RX hysteresis	100	–	mV	–
Cin	Pad capacitance	–	5	pF	–
VOS	Overshoot voltage magnitude [time duration for 200 MHz < 0.4 ns]	–	2.15	V	(1), (2)
VUS	Undershoot voltage magnitude [time duration for 200 MHz < 0.4 ns]	–	-0.35	V	(1), (2)
VOS	Overshoot voltage magnitude [time duration for 200 MHz < 0.8 ns]	–	2.1	V	(1), (2)
VUS	Undershoot voltage magnitude [time duration for 200 MHz < 0.8 ns]	–	-0.3	V	(1), (2)
VOS	Overshoot voltage magnitude [time duration for 200 MHz < 1.25 ns]	–	2.06	V	(1), (2)
VUS	Undershoot voltage magnitude [time duration for 200 MHz < 1.25 ns]	–	-0.26	V	(1), (2)

NOTES:

1. Activity Factor = 0.25, that is, one out of four received cycles have the VOS/VUS.
2. Tj = 105°C

Table 24. SDIO Signal Group AC Specifications

Symbol	Parameter	Minimum Value	Maximum Value	Unit	Notes/ Figure
FCLK	Clock frequency	200	208	MHz	Typical
TDC	Clock duty cycle	39	61	%	Measured at 50%, 2 pF test load
TX slew rate	TX pad slew rate	0.5	0.875	V/ns	Test load at 10 pF
Twc (SDR104)	CLK cycle time for SDR104 mode	4.8	–	ns	–
Twc (SDR50)	CLK cycle time for SDR50 mode	10	–	ns	–
Twc (DDR50)	CLK cycle time for DDR50 mode	20		ns	
Twc (SDR25)	CLK cycle time for SDR25 mode	20		ns	
Twc (SDR12)	CLK cycle time for SDR12 mode	40		ns	
TCO (SDR104 Data)	TX rising clock to data output delay (SDR104)	1.717	2.578	ns	NOTE
TCO (DDR50 Data)	TX rising/falling clock to data output delay (DDR50)	2.696	4.984	ns	NOTE
TCO (SDR50 Data)	TX rising clock to data output delay (SDR50)	2.946	4.599	ns	NOTE
TCO (DS Data)	TX falling clock to data output delay (DS)	6.601	9.444	ns	NOTE
TCO (SDR104 CMD)	TX rising clock to CMD output delay (SDR104)	2.946	4.599	ns	NOTE
TCO (DDR50 CMD)	TX rising/falling clock to CMD output delay (DDR50)	4.763	6.782	ns	NOTE
TCO (SDR50 CMD)	TX rising clock to CMD output delay (SDR50)	2.946	4.599	ns	NOTE
TCO (DS CMD)	TX falling clock to CMD output delay (DS)	6.601	9.444	ns	NOTE
TDVW (SDR104 Data)	RX Data Valid Window to CLK rising/falling edge (SDR104)	0.997		ns	
TSU (DDR50 Data)	RX Data Set up Time to CLK rising/falling edge (DDR50)	2.270		ns	
TH (DDR50 Data)	RX Data Hold Time to CLK rising/falling edge (DDR50)	-0.848		ns	
TSU (SDR50 Data)	RX Data Set up Time to CLK rising/falling edge (SDR50)	1.845		ns	

Symbol	Parameter	Minimum Value	Maximum Value	Unit	Notes/ Figure
TH (SDR50 Data)	RX Data Hold Time to CLK rising/falling edge (SDR50)	-0.848		ns	
TSU (DS Data)	RX Data Set up Time to CLK rising/falling edge (DS)	5.345		ns	
TH (DS Data)	RX Data Hold Time to CLK rising/falling edge (DS)	-0.848		ns	
TDVW (SDR104 CMD)	RX CMD Valid Window to CLK rising/falling edge (SDR104)	1.191		ns	
TSU (DDR50 CMD)	RX Data Set up Time to CLK rising/falling edge (DDR50)	5.803		ns	
TH (DDR50 CMD)	RX Data Hold Time to CLK rising/falling edge (DDR50)	-0.812		ns	
TSU (SDR50 CMD)	RX Data Set up Time to CLK rising/falling edge (SDR50)	2.003		ns	
TH (SDR50 CMD)	RX Data Hold Time to CLK rising/falling edge (SDR50)	-0.812		ns	
TSU (DS CMD)	RX Data Set up Time to CLK rising/falling edge (DS)	5.345		ns	
TH (DS CMD)	RX Data Hold Time to CLK rising/falling edge (DS)	-0.848		ns	

NOTE: Processor output timings are measured at the processor pad with a test load of 2 pF (50% of the voltage).

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5.0 Ball Map, Processor Pin Locations, and Package Information

Table 25 compares the signal names of the N- and J- Series Processors to the E3900 and A3900 Series Processors. Refer to *Apollo Lake-I SoC 31x24 mm Package Ball Map – Ballout, Signal, and Mechanical Package* (Document ID# 559350) for other processor pin names.

Refer to *manufacturing with the Intel® Mobile Products: Apollo Lake and Apollo Lake I* (Document ID# 561676) for processor package design details.

Table 25. Signal Name Comparison between N- and J- Series Processors and E3900 and A3900 Series Processors

Pin Number	N- and J- Series Processors	E3900 and A3900 Series Processors
AW48	NCTF	MEM_CH0_ECC_DQ0(NOTE)
AW47	NCTF	MEM_CH0_ECC_DQ1(NOTE)
BB43	NCTF	MEM_CH0_ECC_DQ2(NOTE)
AW45	NCTF	MEM_CH0_ECC_DQ3(NOTE)
AV48	NCTF	MEM_CH0_ECC_DQ4(NOTE)
AV47	NCTF	MEM_CH0_ECC_DQ5(NOTE)
BD43	NCTF	MEM_CH0_ECC_DQ6(NOTE)
BA45	NCTF	MEM_CH0_ECC_DQ7(NOTE)
BD47	NCTF	MEM_CH0_ECC_DQS_P(NOTE)
BB47	NCTF	MEM_CH0_ECC_DQS_N(NOTE)
AR21	NCTF	MEM_CH1_ECC_DQ0(NOTE)
AT21	NCTF	MEM_CH1_ECC_DQ1(NOTE)
AW23	NCTF	MEM_CH1_ECC_DQ2(NOTE)
AW21	NCTF	MEM_CH1_ECC_DQ3(NOTE)
BA19	NCTF	MEM_CH1_ECC_DQ4(NOTE)
AW19	NCTF	MEM_CH1_ECC_DQ5(NOTE)
BA23	NCTF	MEM_CH1_ECC_DQ6(NOTE)
BB23	NCTF	MEM_CH1_ECC_DQ7(NOTE)
BD23	NCTF	MEM_CH1_ECC_DQS_P(NOTE)
BE23	NCTF	MEM_CH1_ECC_DQS_N(Note)
P58	GPIO_166	SDIO_CLK

Pin Number	N- and J- Series Processors	E3900 and A3900 Series Processors
T52	GPIO_167	SDIO_D0
P57	GPIO_168	SDIO_D1
T54	GPIO_169	SDIO_D2
T55	GPIO_170	SDIO_D3
T57	GPIO_171	SDIO_CMD
P51	GPIO_183	SDIO_PWR_DWN_N

NOTE: Applicable to the DDR3L ECC option only.

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