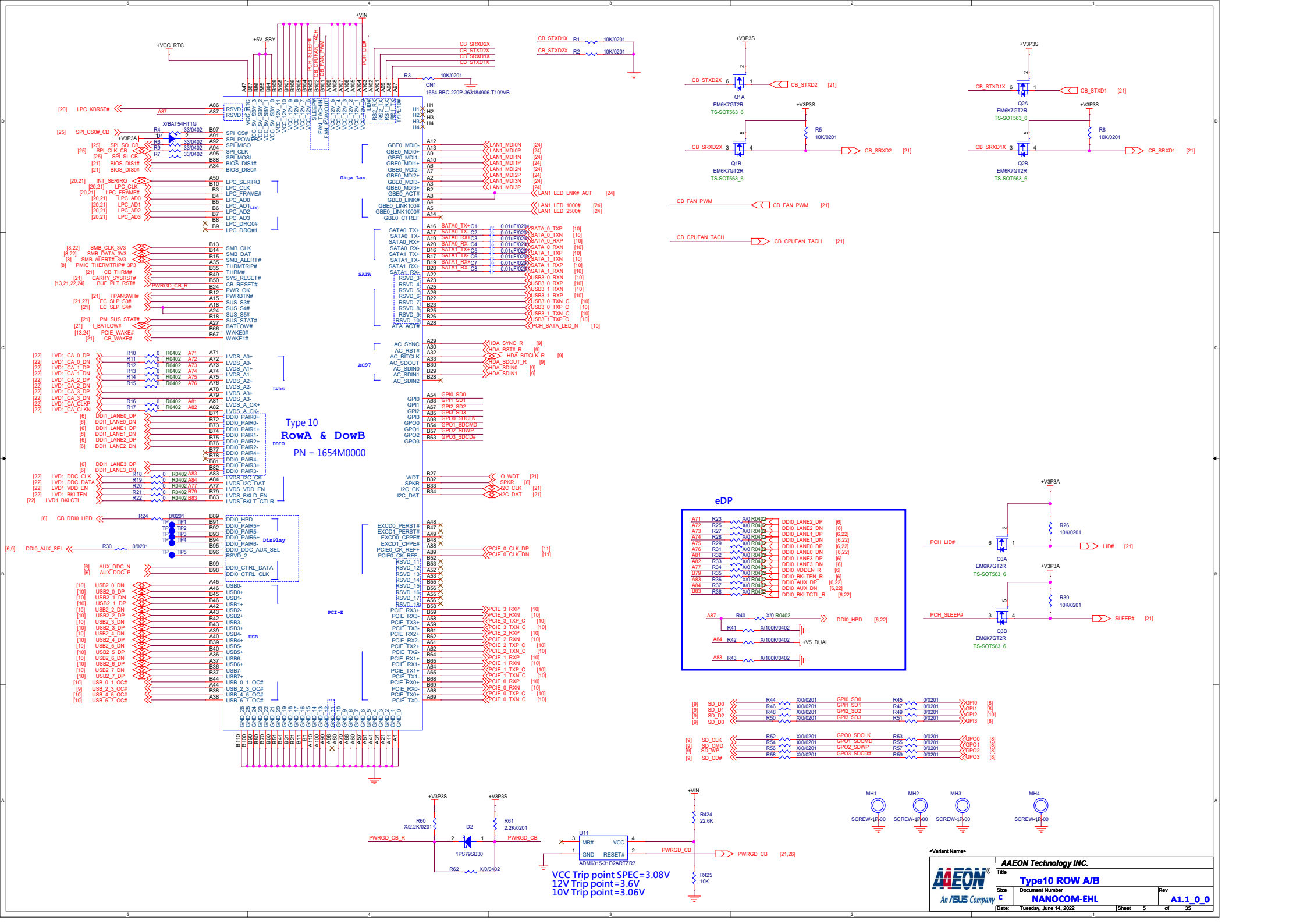
Type 10
RowA & DowB
PN = 1654M0000
eDP
Giga Lan
SATA
AC97
LVDS
DDIO
DisPlay
PCI-E
USB
LPC
VCC Trip point SPEC=3.08V
12V Trip point=3.6V
10V Trip point=3.06V
AAEON Technology INC.
Type10 ROW A/B
NANOCOM-EHL
A1.1_0_0
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SoC DDI

eDP/LVDS

ROWA/B

144000EHL0
(TF)INTEL CPU.Elkhart Lake .SERIES.BGA.1493P.SMD

GP_E19

GP_E19/ DDI0_DDC_SCL/ PSE_PWM13/ PSE_TGPIO24	GP_E18/ E19 pins VCC configu- ration	Rising edge of PMC_RSMRST_N	This strap has a 20 kohm ± 30% internal pull-down. 0 = GP_E18/E19 DDC pins at 1.8V 1 = GP_E18/E19 DDC pins at 3.3V **Notes:** 1. An external pull-up resistor is required if the muxed DDC signals are to be connected directly to the HDMI or DP++ connector. 2. The internal pull-down is disabled after PMC_RSMRST_N de-asserts. 3. This signal is in the primary well. 4. This strap will become RSVD in future (targeted BKC Beta release), DDC pin voltage is configurable via FIT tool soft strap.

U1A

DDI0_LANE0_DN G110 DDI0_LANE0_DP G112 DDI0_LANE1_DN J111 DDI0_LANE1_DP J109 DDI0_LANE2_DN K104 DDI0_LANE2_DP H104 DDI0_LANE3_DN P101 DDI0_LANE3_DP M101
DDI0_AUX_DN T104 DDI0_AUX_DP P104
DDI1_LANE0_DN T95 DDI1_LANE0_DP P98 DDI1_LANE1_DN F101 DDI1_LANE1_DP H101 DDI1_LANE2_DN P95 DDI1_LANE2_DP M95 DDI1_LANE3_DN K98 DDI1_LANE3_DP H98
DDI1_AUX_DN T98 DDI1_AUX_DP T101
R112 DDI2_TXN0 R110 DDI2_TXP0 W112 DDI2_TXN1 W110 DDI2_TXP1 N111 DDI2_TXN2 N109 DDI2_TXP2 L112 DDI2_TXN3 L110 DDI2_TXP3
U111 DDI2_AUXN U109 DDI2_AUXP
R78 1% 150 R0402 DDI0_RCOMP E109 DDI0_RCOMP

PNL0_BKLTCTL T2 DDI0_BKLTCTL R65 0 R0201 DDI0_BKLTCTL_R [5,22]
PNL0_BKLTEN T4 DDI0_BKLTEN R66 0 R0201 DDI0_BKLTEN_R [5]
PNL0_VDDEN U3 DDI0_VDDEN R67 0 R0201 DDI0_VDDEN_R [5]

EDP_UTILS_MDSI_DE_TE_1 D90 C103
MDSI_DE_TE_2

GP_E19_DDI0_DDC_SCL_PSE_PWM13_PSE_TGPIO24 M32
GP_E18_DDI0_DDC_SDA_PSE_PWM12_PSE_TGPIO23 H43 DDI0_CTRL_DATA
GP_E14_DDI0_HPD_PNL_MISC_DDI0_PSE_TGPIO19 K46 DDI0_HPD0

GP_E07_DDI1_DDC_SCL_CPU_GP1_PSE_TGPIO16 F36 DDI1_CTRL_CLK
GP_E05_DDI1_DDC_SDA_PSE_PWM09_PSE_TGPIO17 K36 DDI1_CTRL_DATA
GP_E03_DDI1_HPD_PNL_MISC_DDI1_CPU_GP0_PSE_TGPIO15 F39 DDI1_HPD0

GP_E23_PNL1_BKLTEN_PSE_PWM15_PSE_TGPIO19 H36
GP_E22_PNL1_BKLTCTL_PSE_PWM14_PSE_TGPIO18 H32
GP_E17_PNL1_VDDEN_PNL_MISC_DDI2_PSE_PWM11_PSE_TGPIO46 K43

14-CPU-ELKHART_LAKE-BGA1493-0
BGA1493X-35X24X2P54M

A0.4

+V3P3S
DDI0_CTRL_DATA R69 X/2.2K R0201
DDI1_CTRL_CLK R70 2.2K R0201
DDI1_CTRL_DATA R71 2.2K R0201
R72 X/10K R0201
DDI0_HPD0 R73 100K R0201
DDI1_HPD0 R74 X/100K R0201
DDI0_BKLTEN R75 X/100K R0201
DDI0_VDDEN R76 X/100K R0201

+VCC5V
Q4A
DDI0_HPD0 1 6 EM6K7GT2R TS-SOT563_6 DDI0_HPD [5,22]
R77 X/0 R0201

+VCC5V
Q4B
DDI1_HPD0 4 3 EM6K7GT2R TS-SOT563_6 CB_DDI0_HPD [5]
R79 X/0 R0201

DDI0_AUX_SEL:
H: DDC (HDMI/DVI)
L: AUX (DP/eDP)

[5,9] DDI0_AUX_SEL
+V3P3S
C9 0.1uF/6.3V

U2
DDI1_AUX_DP AUX_DDC_P C10 0.1uF C0201
DDI0_AUX_SEL
DDI1_AUX_DN AUX_DDC_N C11 0.1uF C0201
1OE 1A 1B 2OE 2A 2B GND VCC 4OE 4A 4B 3OE 3A 3B GND
DDI0_DDC_SEL DDI1_CTRL_DATA
DDI0_DDC_SEL DDI1_CTRL_CLK
14-T_C_L-74CBTLV3125BQ-0

+V3P3S
R82 100K R0201
AUX_DDC_N
AUX_DDC_N [5]

[5] AUX_DDC_P
AUX_DDC_P
R85 100K R0201

+V3P3S
R83 10K/0201
DDI0_DDC_SEL
+V3P3S
R81 10K/0201
To SOC GPI
DDC_AUX_SEL1 [12]
Q5A EM6K7GT2R TS-SOT563_6
Q5B EM6K7GT2R TS-SOT563_6
DDI0_AUX_SEL
R84 1M/0201

Must connect to SOC GPIO(Check 1.8 or 3.3V)

<Variant Name>

AAEON Technology INC.

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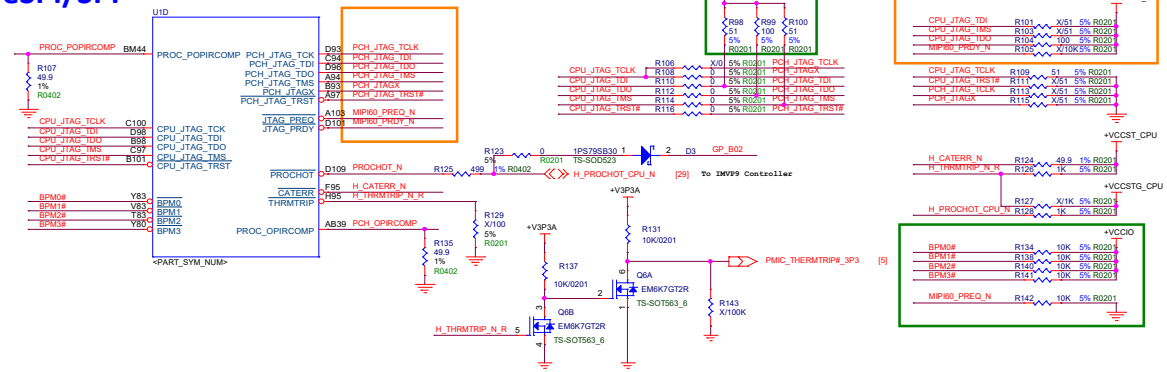
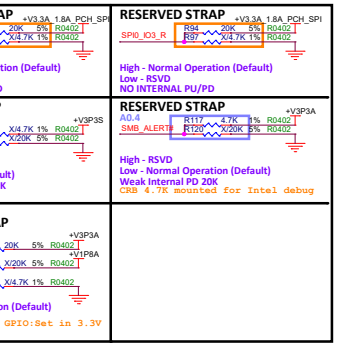
SoC JTAG/eSPI/SPI

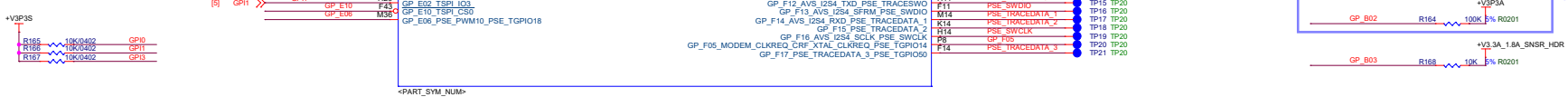




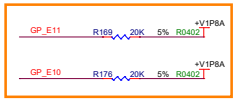
For GP_E06:
The pull-up rail will be V1P8A or V3P3A,
depending on what I/O voltage the GPIO is configured to.

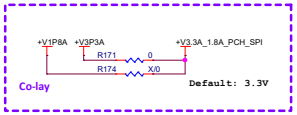
FSPI Interface supports 1.8V or 3.3V
For SPI Flash -> Default:3.3V

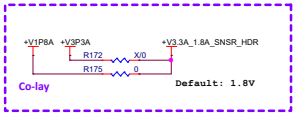
eSPI Interface supports 1.8V only



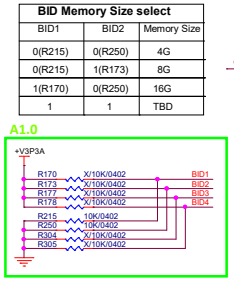
September 2021	1.6	Updated GP_D10, GP_D12, GP_E09, GP_E10, GP_E11 and GP_E21 Mixed Hardware Strap to "No"

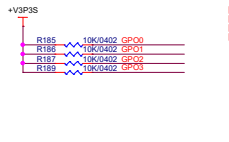


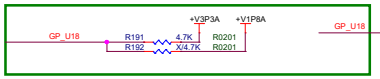


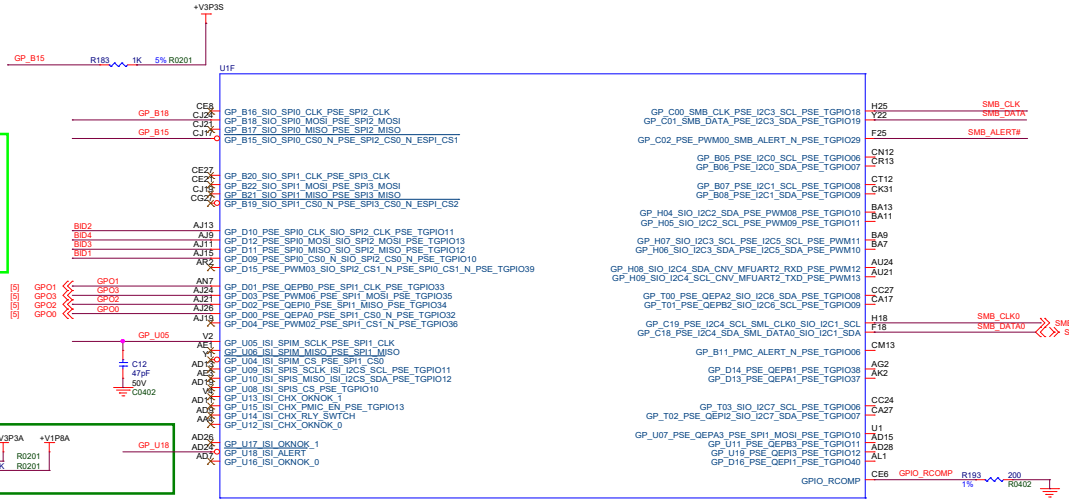


BID Memory Size select		
BID1	BID2	Memory Size
0(R215)	0(R250)	4G
0(R215)	1(R173)	8G
1(R170)	0(R250)	16G
1	1	TBD









<Variant Name>

AAEON Technology INC.		
AAEON An ASUS Company	Title: SoC JTAG/eSPI/SPI/GPIO	
	Size: Custom	Document Number: NANOCOM-EHL
	Rev: A1.1_0_0	
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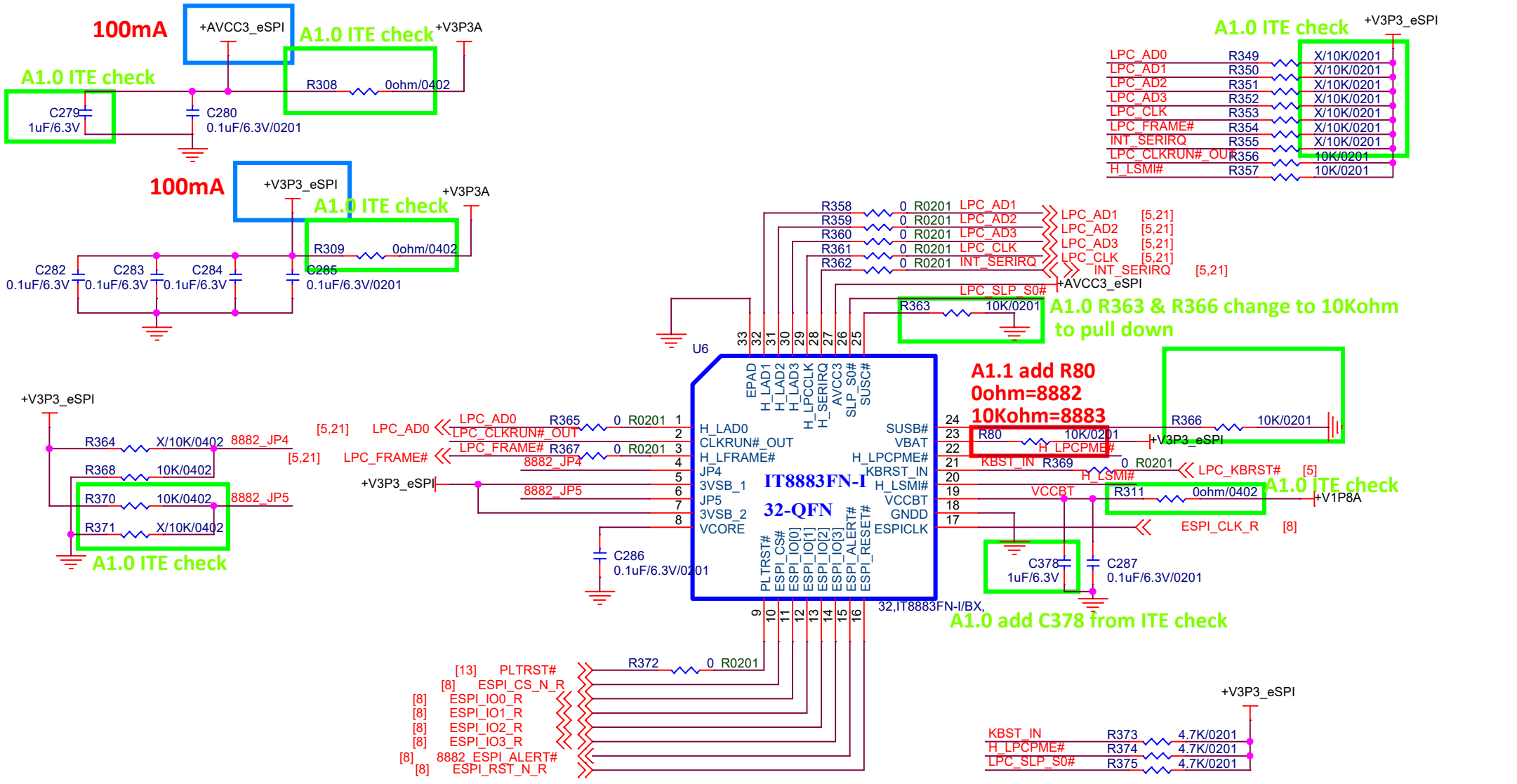

• Power-On Strapping

	Symbol	Value	Description
JP4	Enter key	1	2E/2F (87 01 55 55)
Pin-4		0	4E/4F (87 01 55 AA)*
JP5	CHIP_SEL	1	Chip selection
Pin-6		0	Chip selection*

<Variant Name>

AAEON Technology INC.

Title: eSPI to LPC_IT8882

Size: Custom | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

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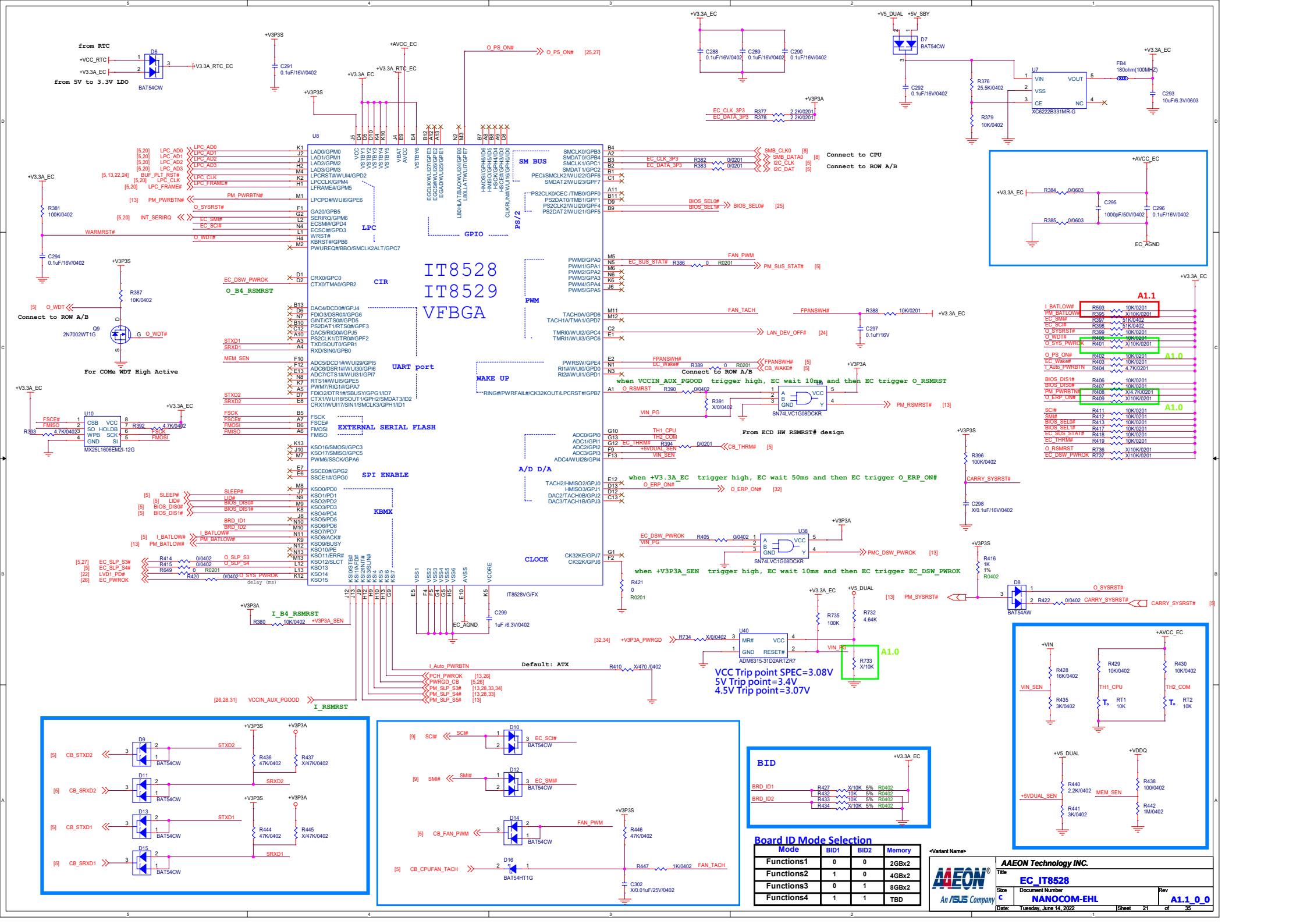
IT8528
IT8529
VFBGA
IT8528VG/FX
SM BUS
PS/2
LPC
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Connect to CPU
Connect to ROW A/B
Connect to ROW A/B
Connect to ROW A/B
O_B4_RSMRST
For COMe WDT High Active
when VCCIN_AUX_PGOOD trigger high, EC wait 10ms and then EC trigger O_RSMRST
From ECD HW RSMRST# design
when +V3.3A_EC trigger high, EC wait 50ms and then EC trigger O_ERP_ON#
when +V3P3A_SEN trigger high, EC wait 10ms and then EC trigger EC_DSW_PWROK
Default: ATX
I_B4_RSMRST
I_RSMRST
VCC Trip point SPEC=3.08V
5V Trip point=3.4V
4.5V Trip point=3.07V
A1.1
A1.0
A1.0
BID
Board ID Mode Selection
Mode | BID1 | BID2 | Memory
Functions1 | 0 | 0 | 2GBx2
Functions2 | 1 | 0 | 4GBx2
Functions3 | 0 | 1 | 8GBx2
Functions4 | 1 | 1 | TBD
AAEON Technology INC.
EC_IT8528
NANOCOM-EHL
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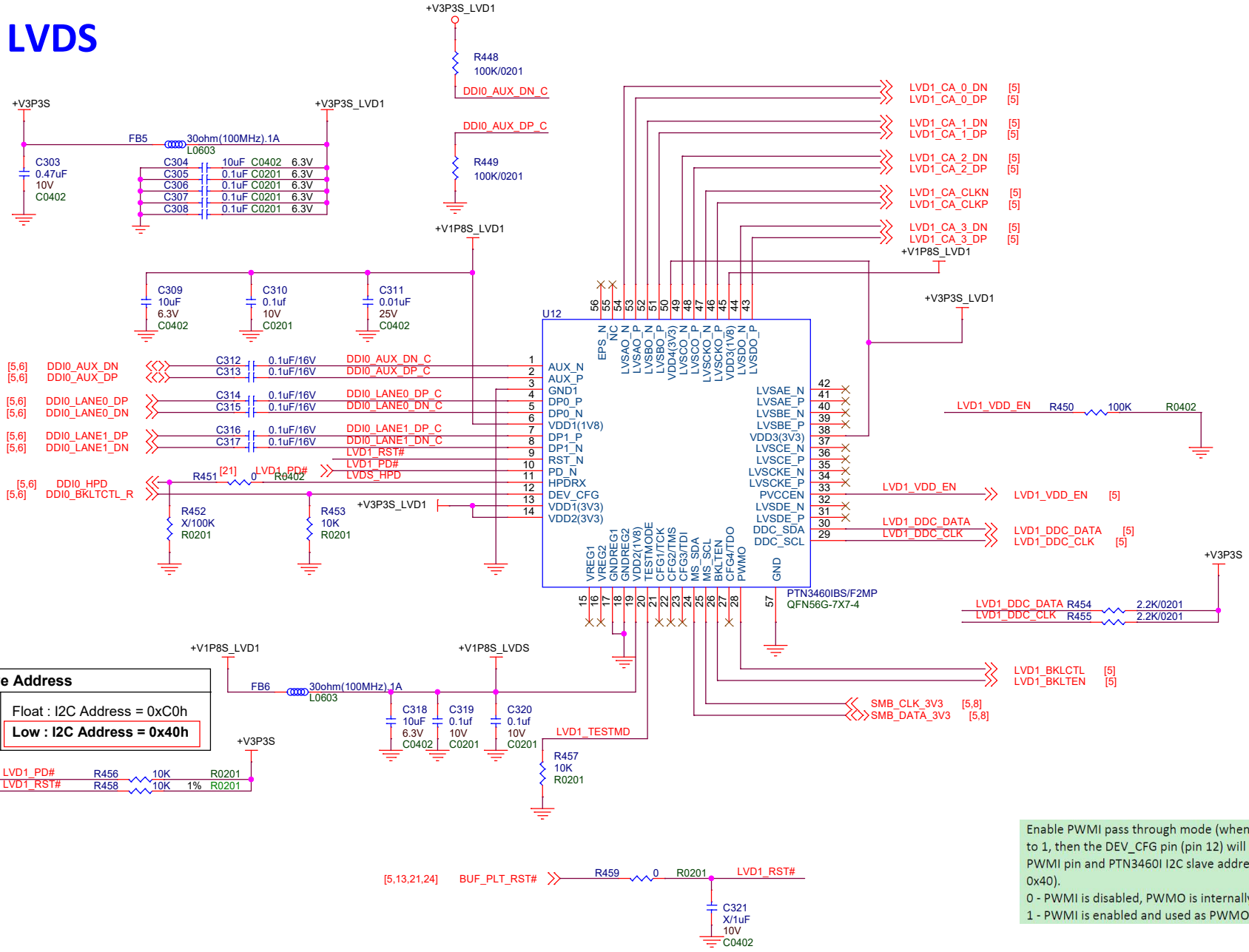
LVDS



I2C Slave Address	
DEV_CFG	Float : I2C Address = 0xC0h
	Low : I2C Address = 0x40h

Enable PWMI pass through mode (when this bit is set to 1, then the DEV_CFG pin (pin 12) will be used as PWMI pin and PTN3460I I2C slave address will be 0x40).
0 - PWMI is disabled, PWMO is internally generated
1 - PWMI is enabled and used as PWMO source

<Variant Name>

AAEON Technology INC.

Title	LVDS		
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