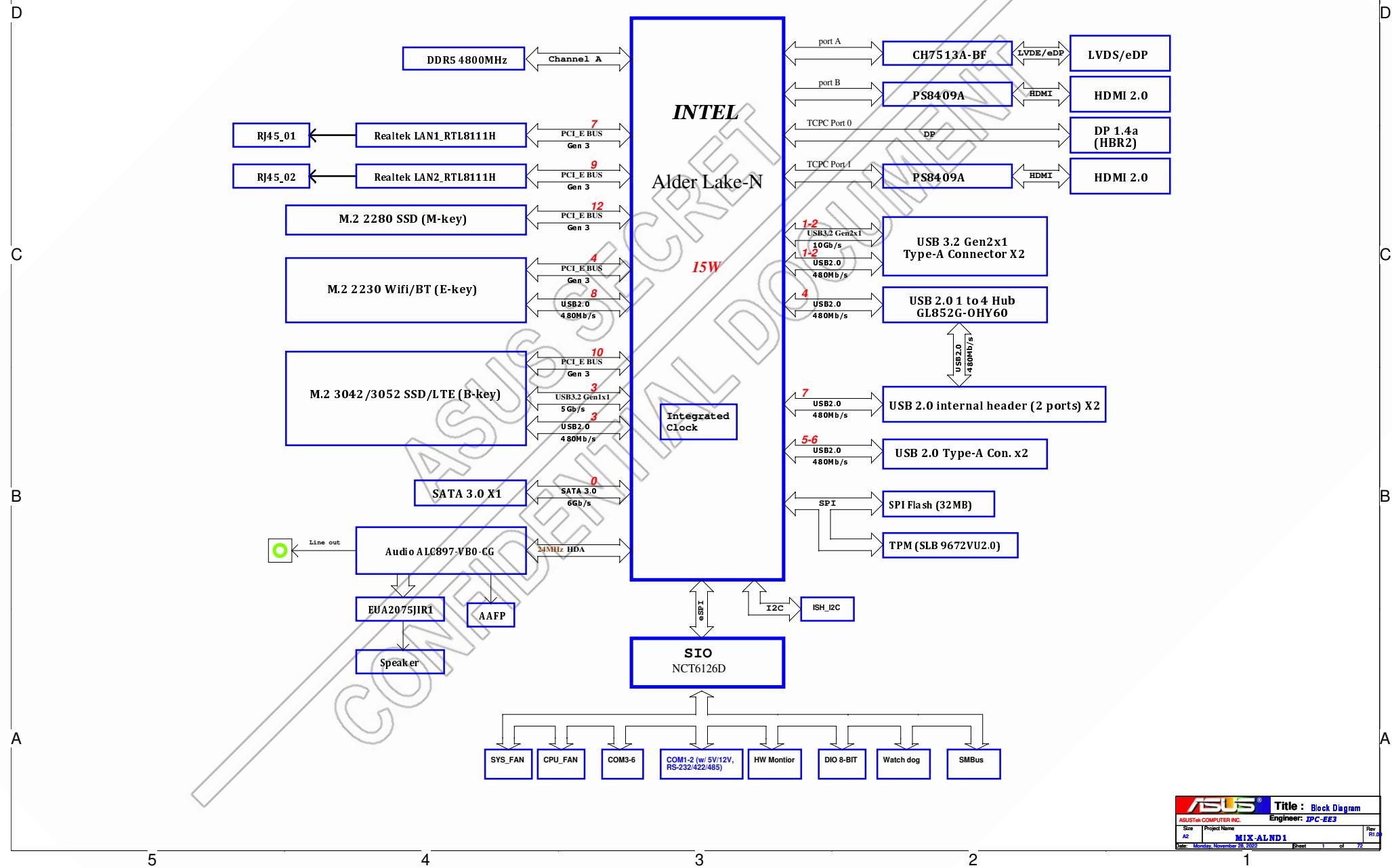
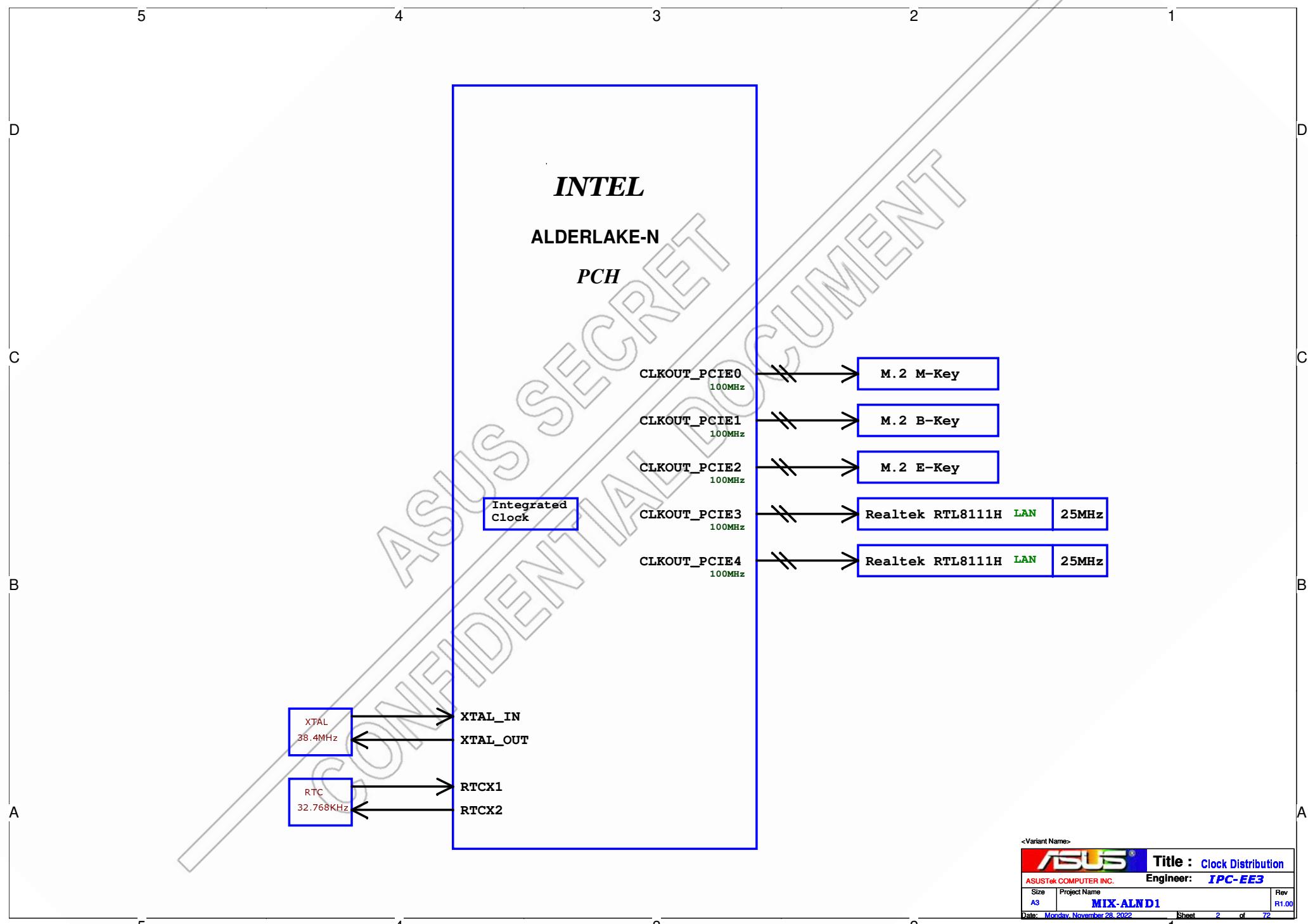
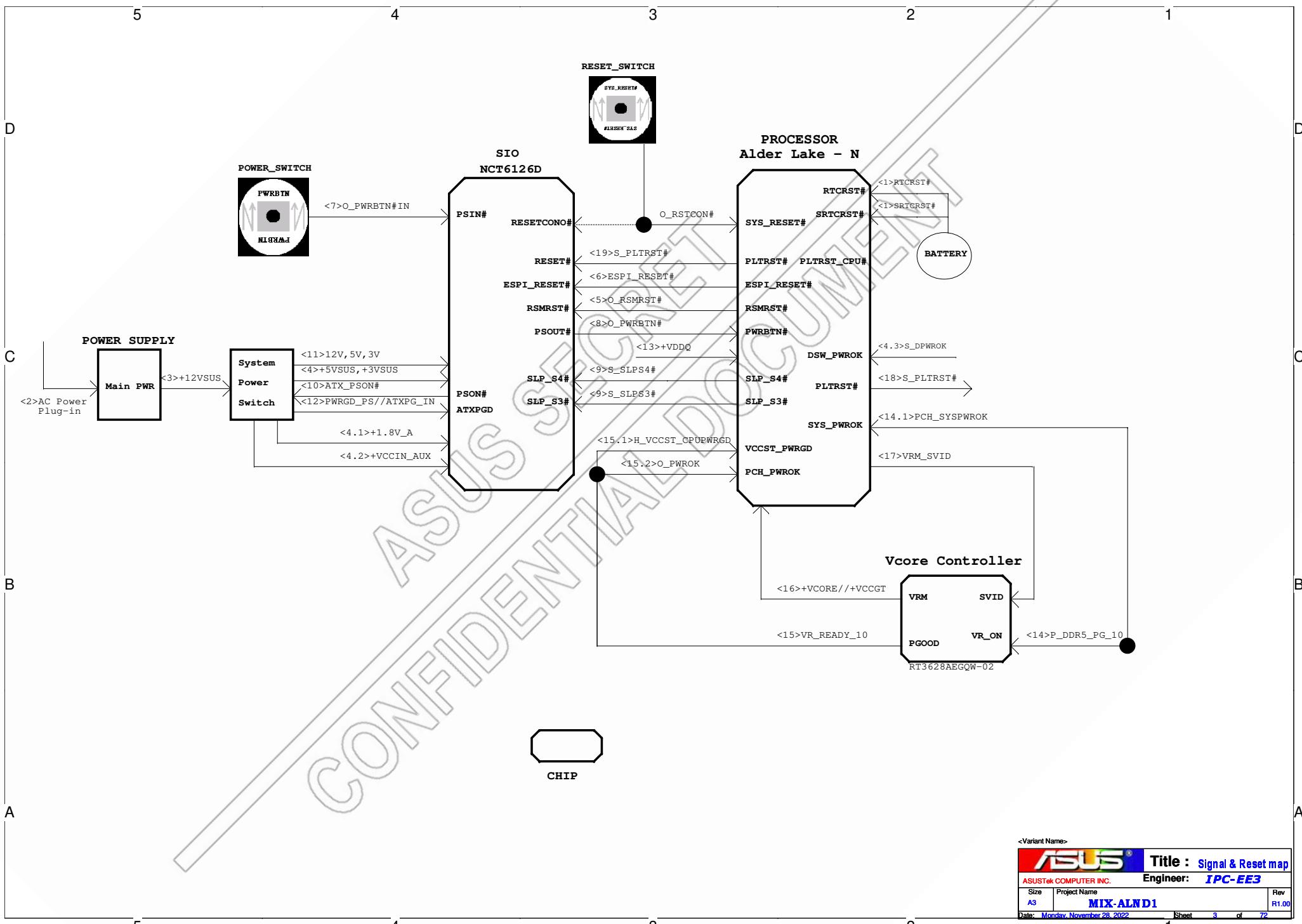


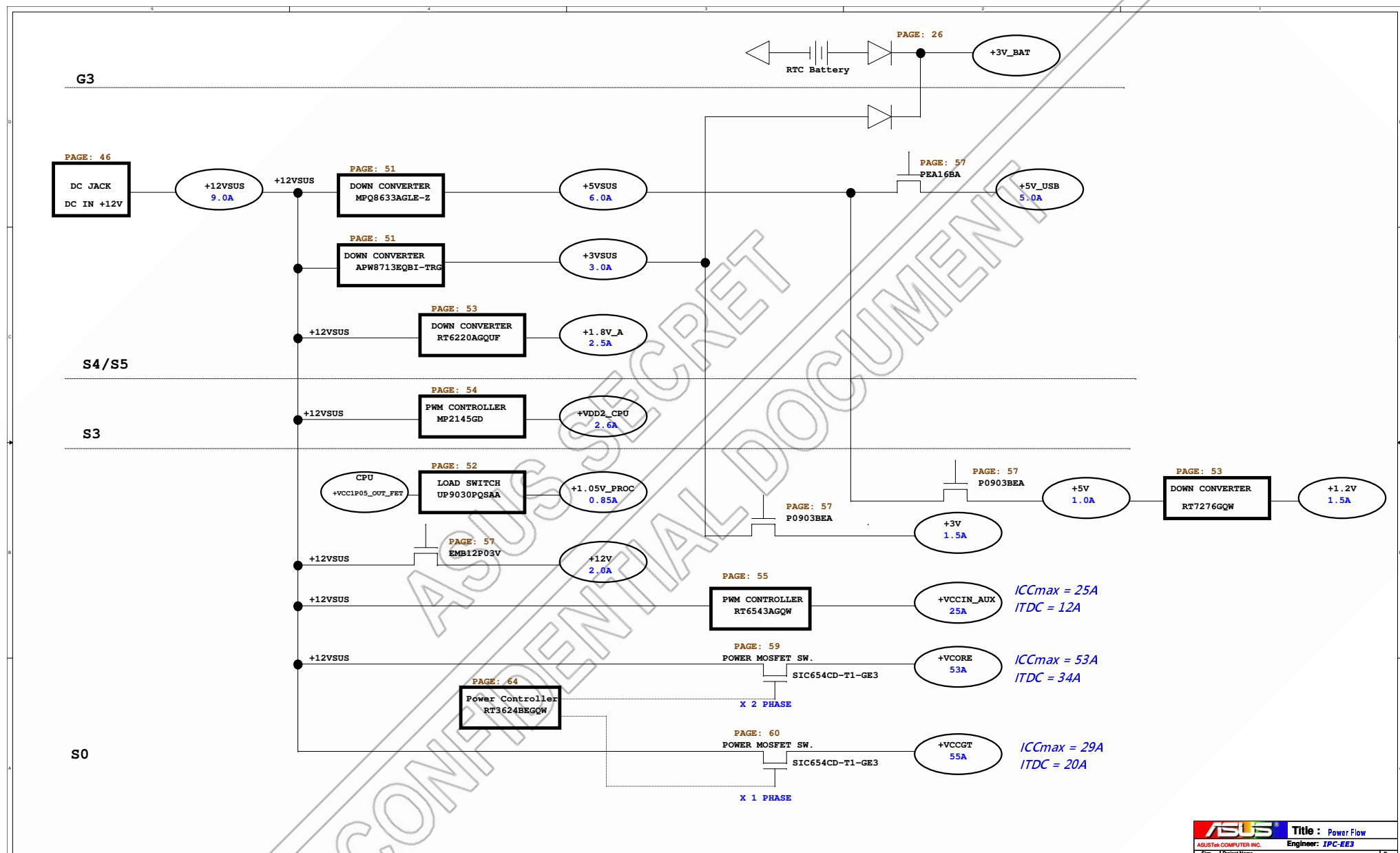
MIX-ALND1

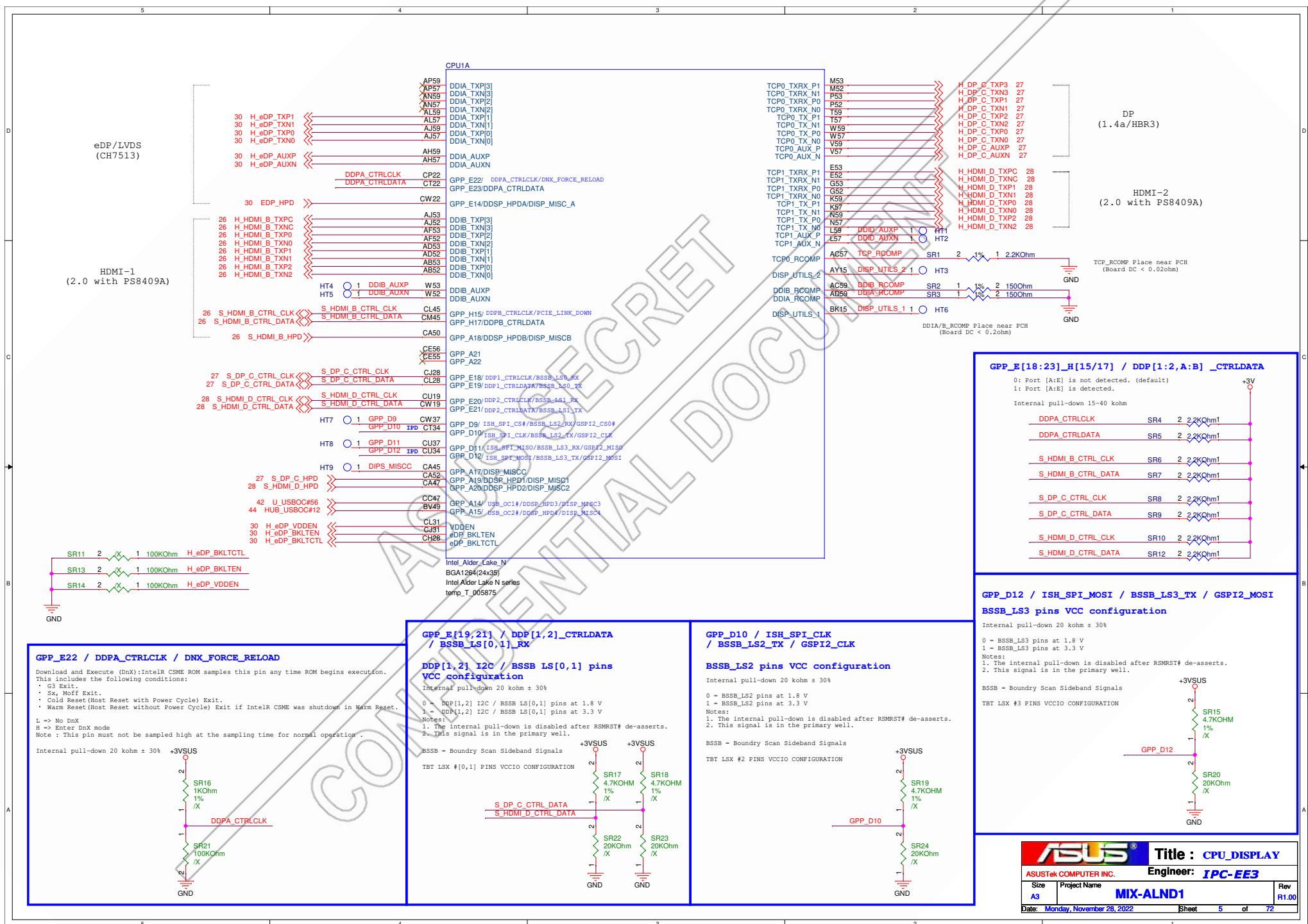
Block Diagram Rev 1.00

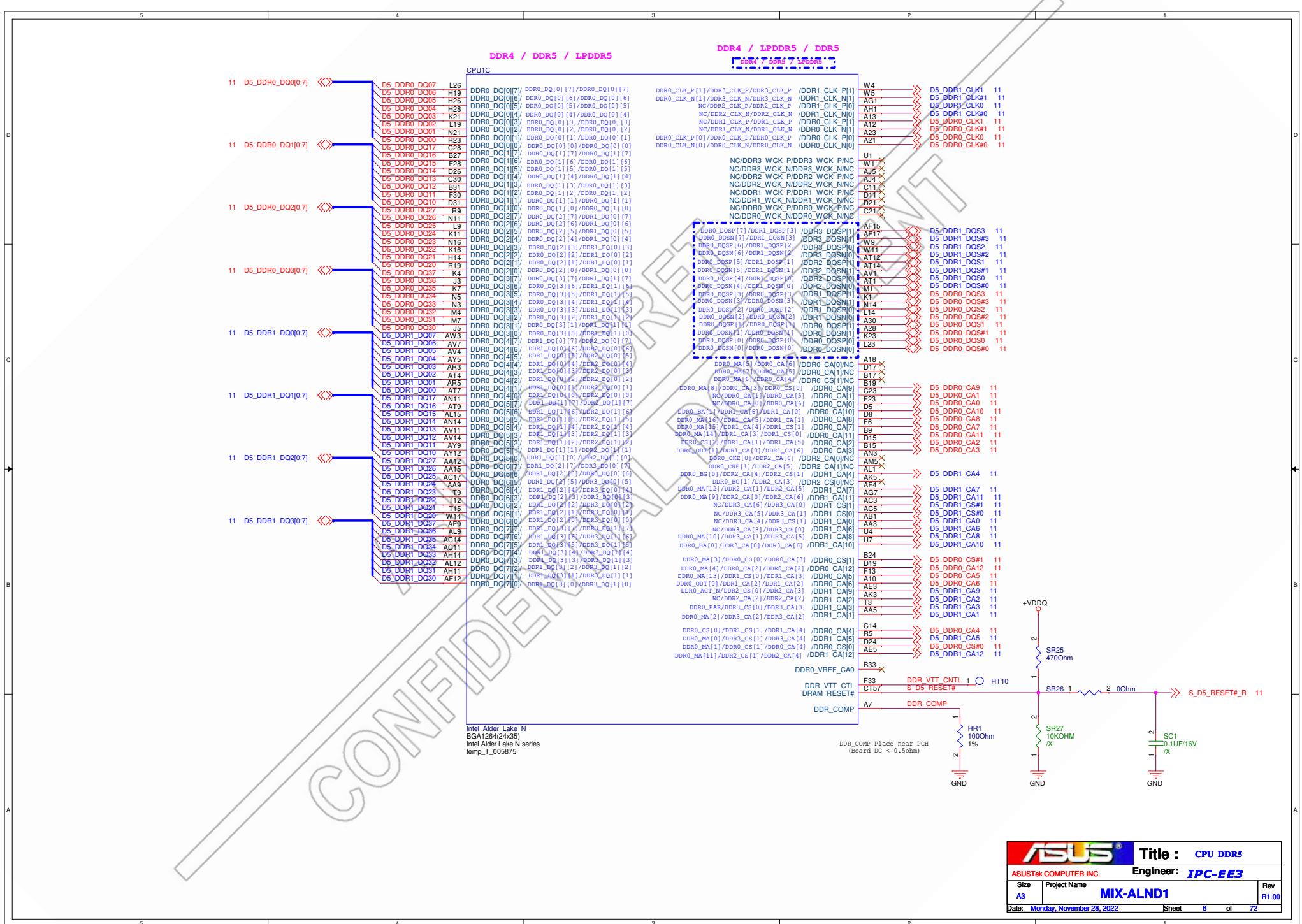


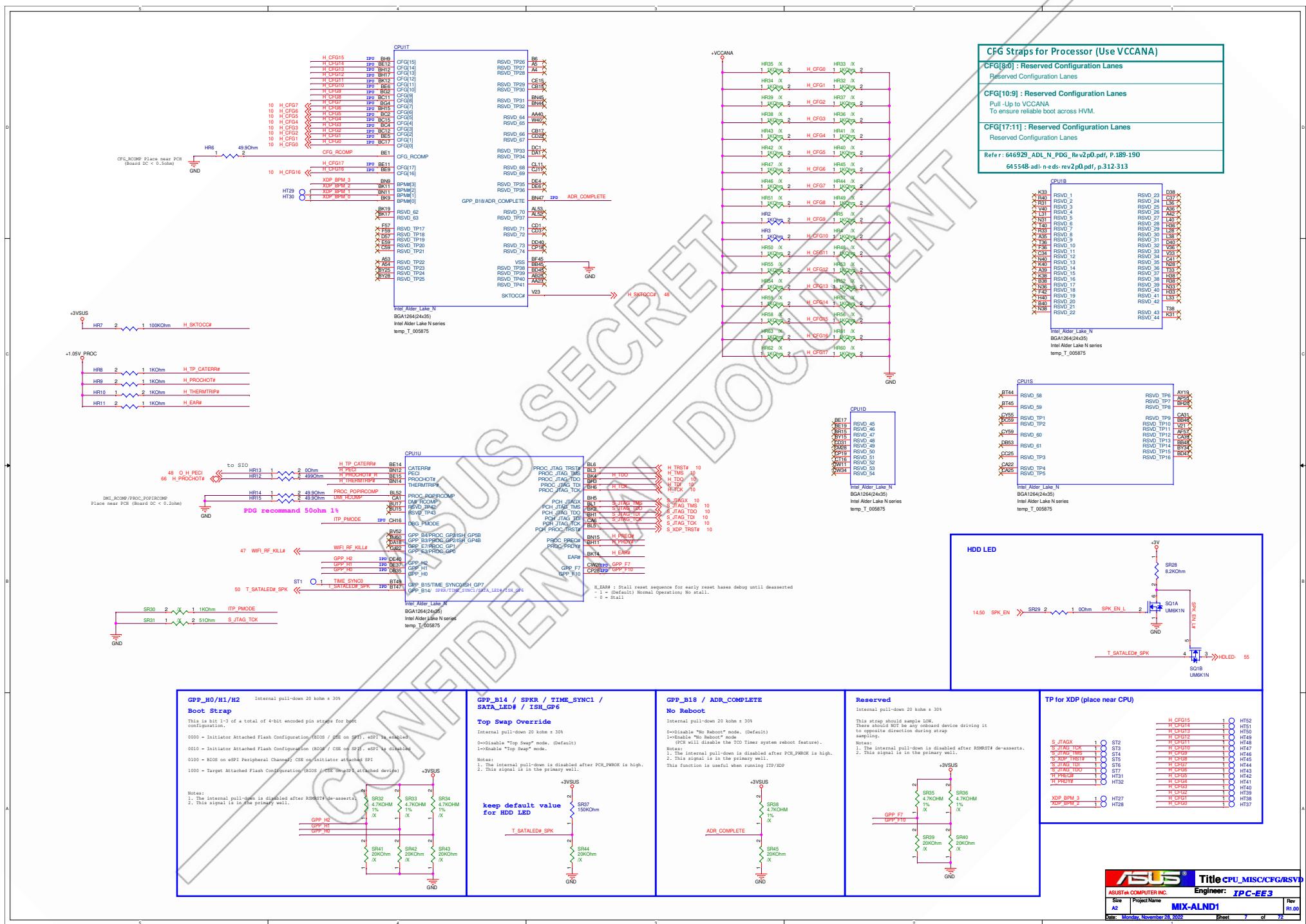


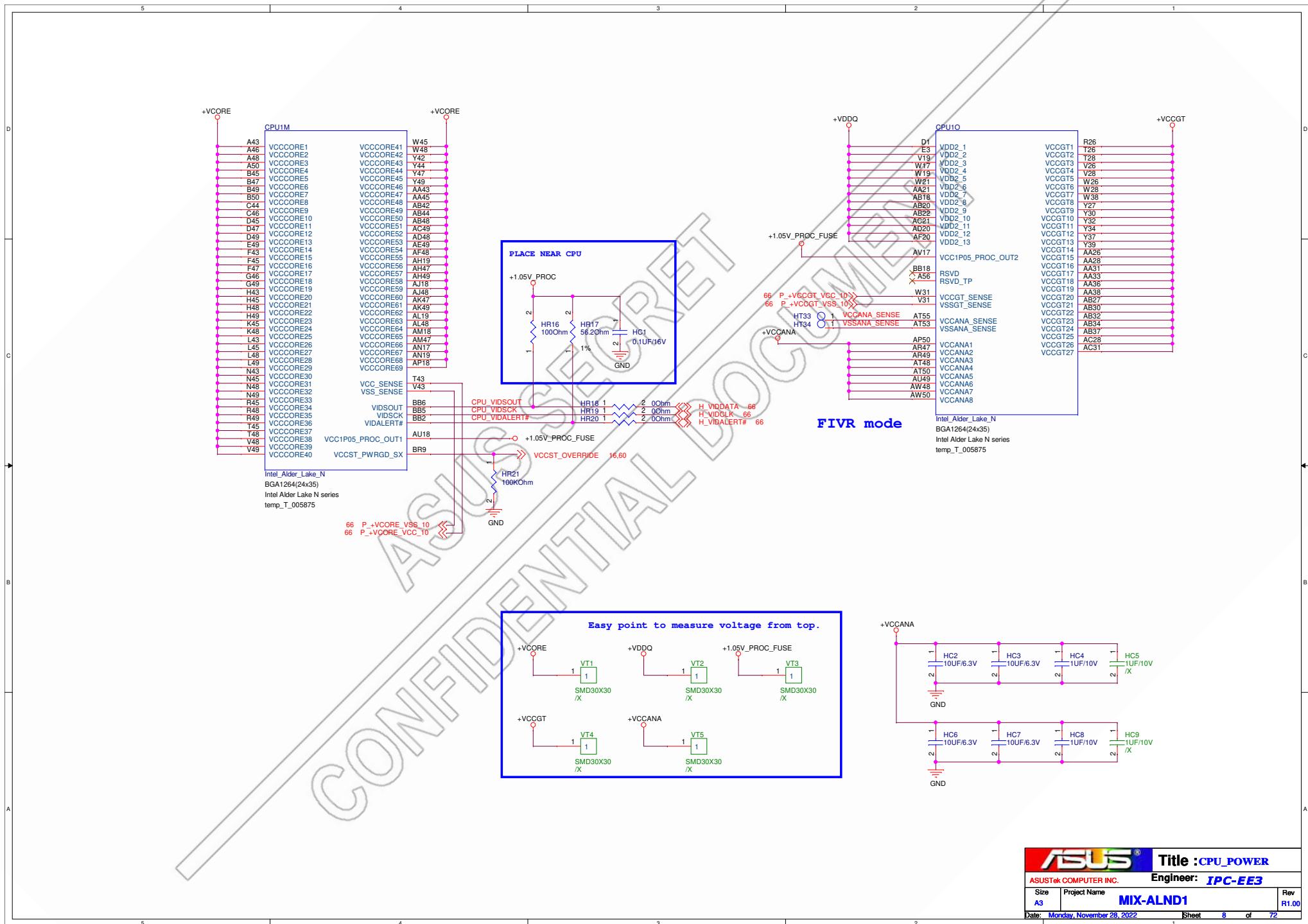


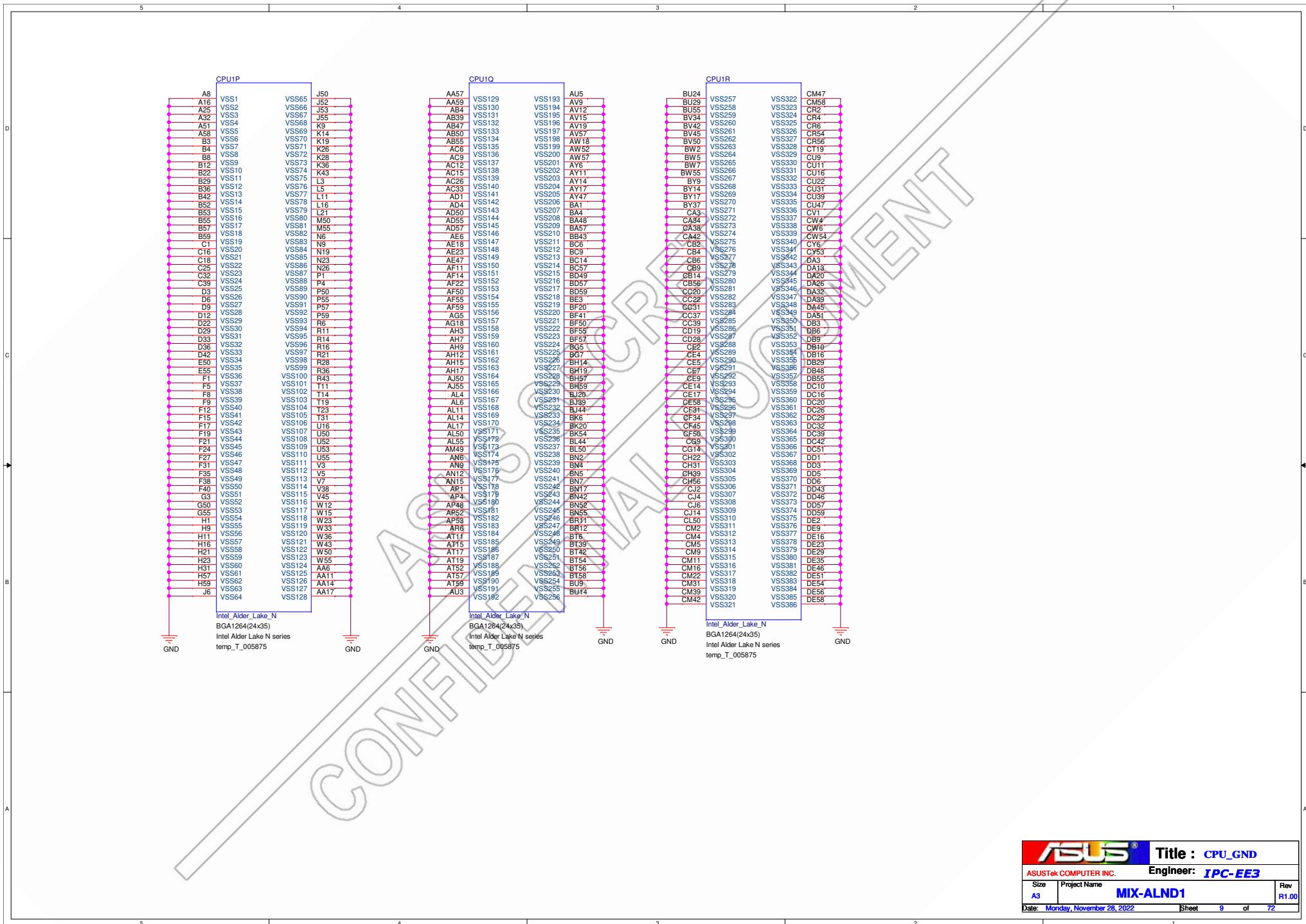




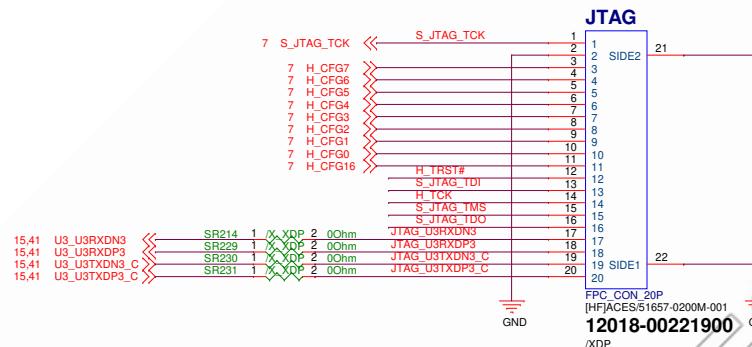




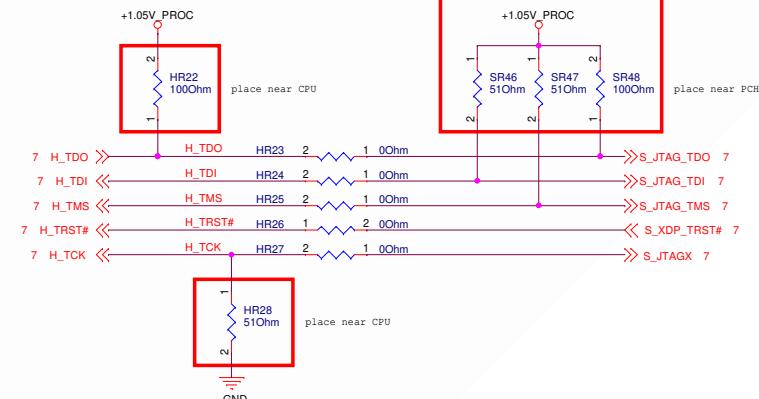


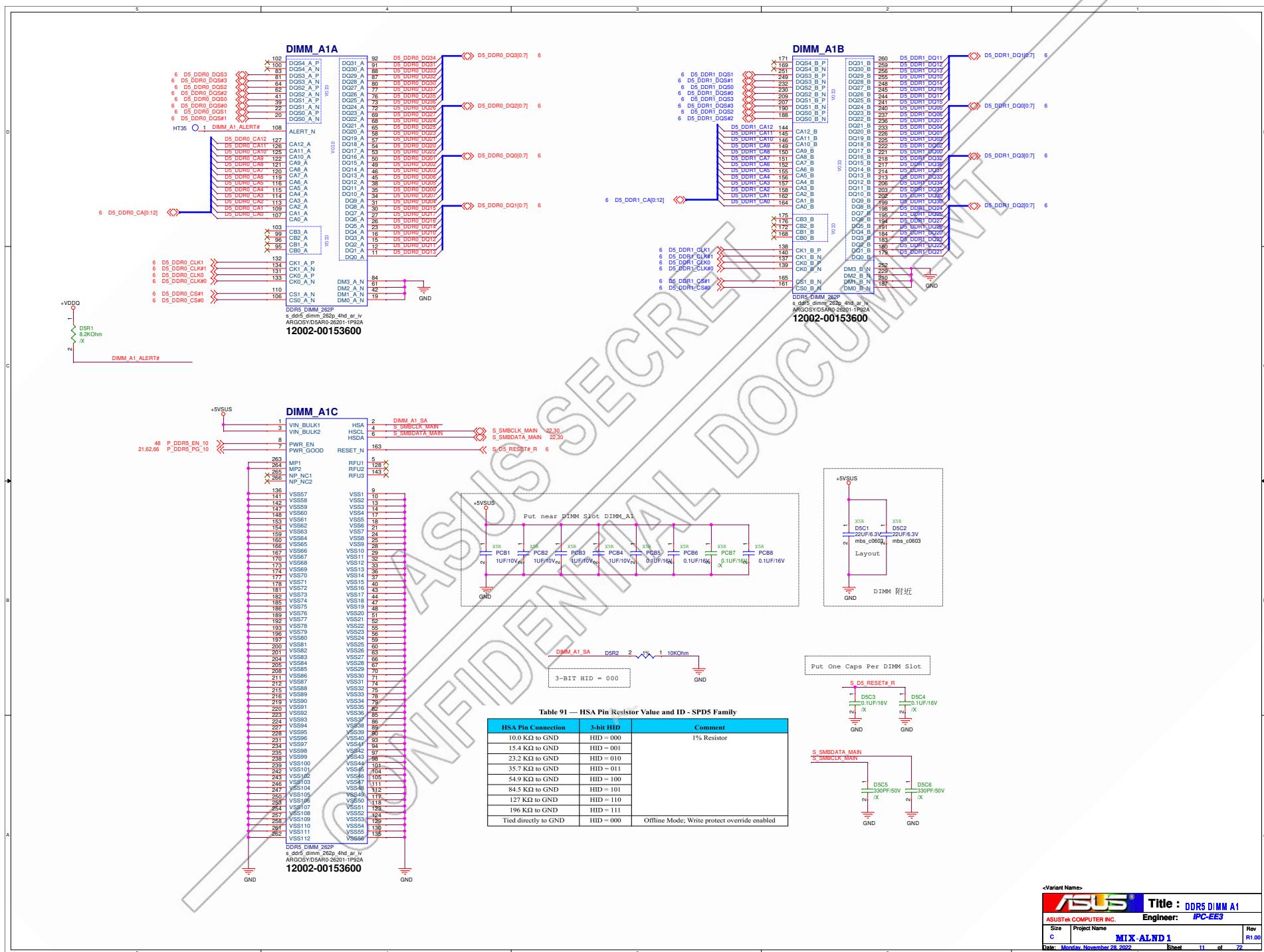


Intel® Small Form Factor Debug Connector



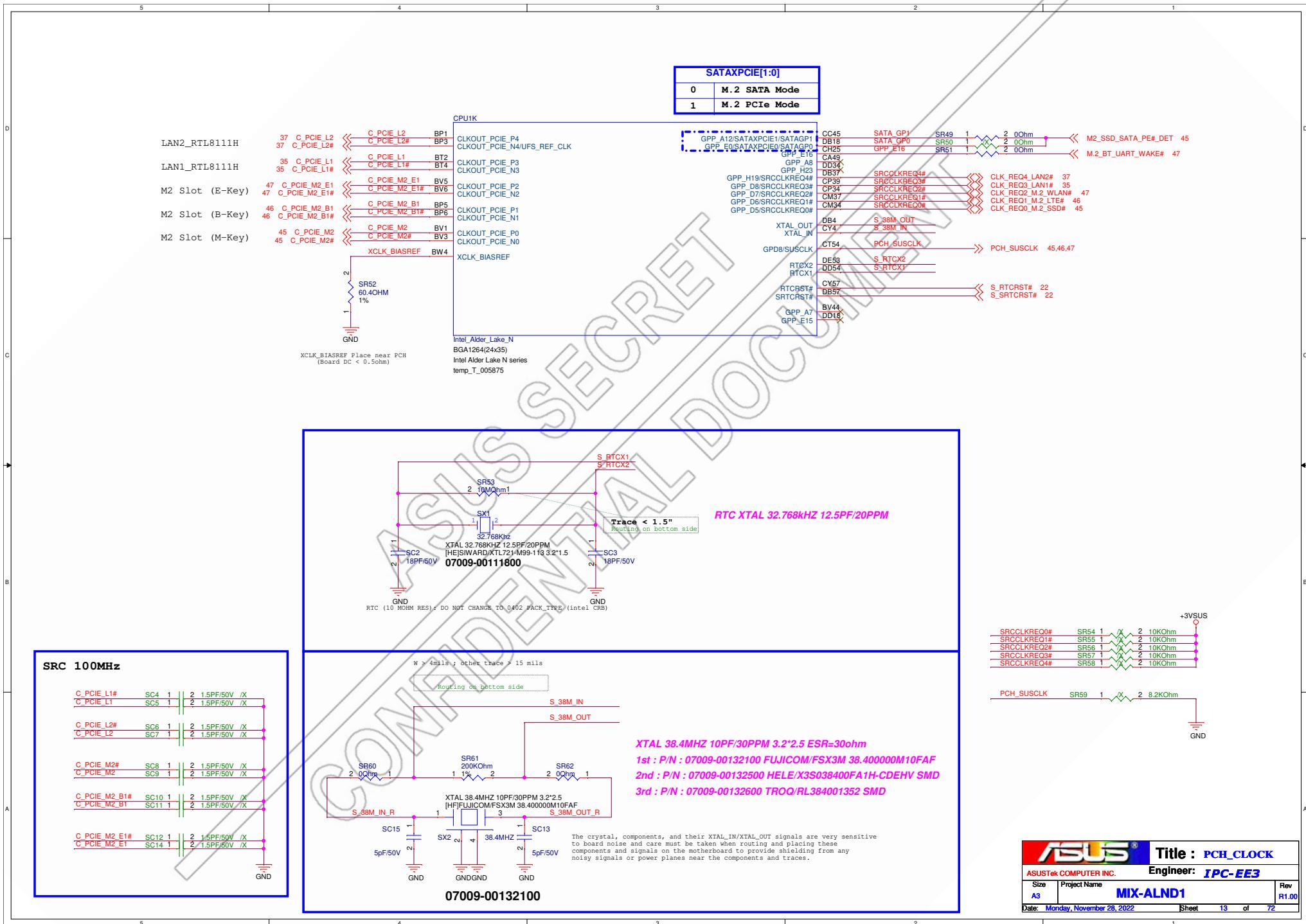
To PCH

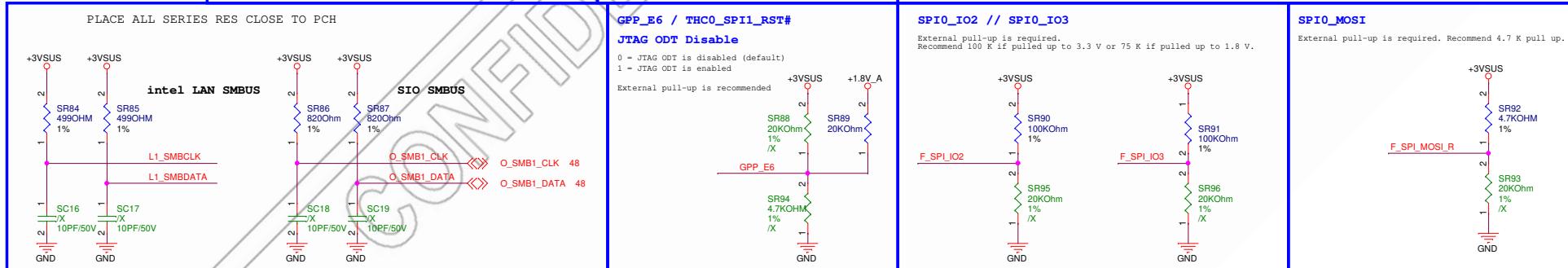
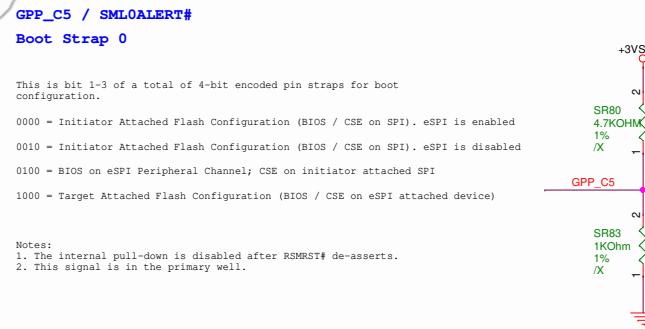
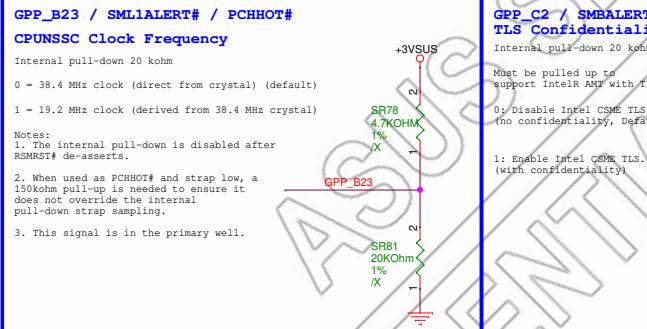


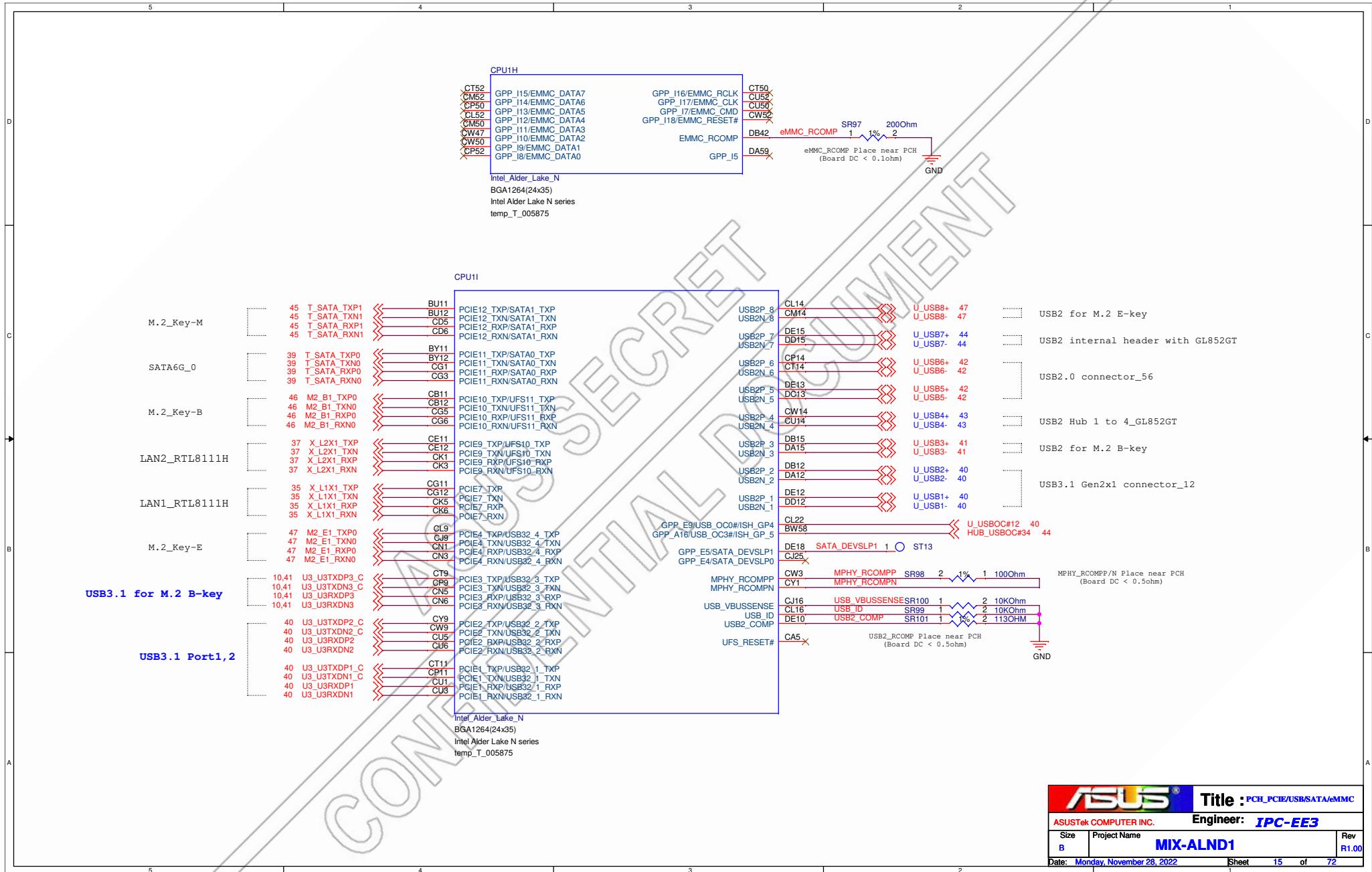


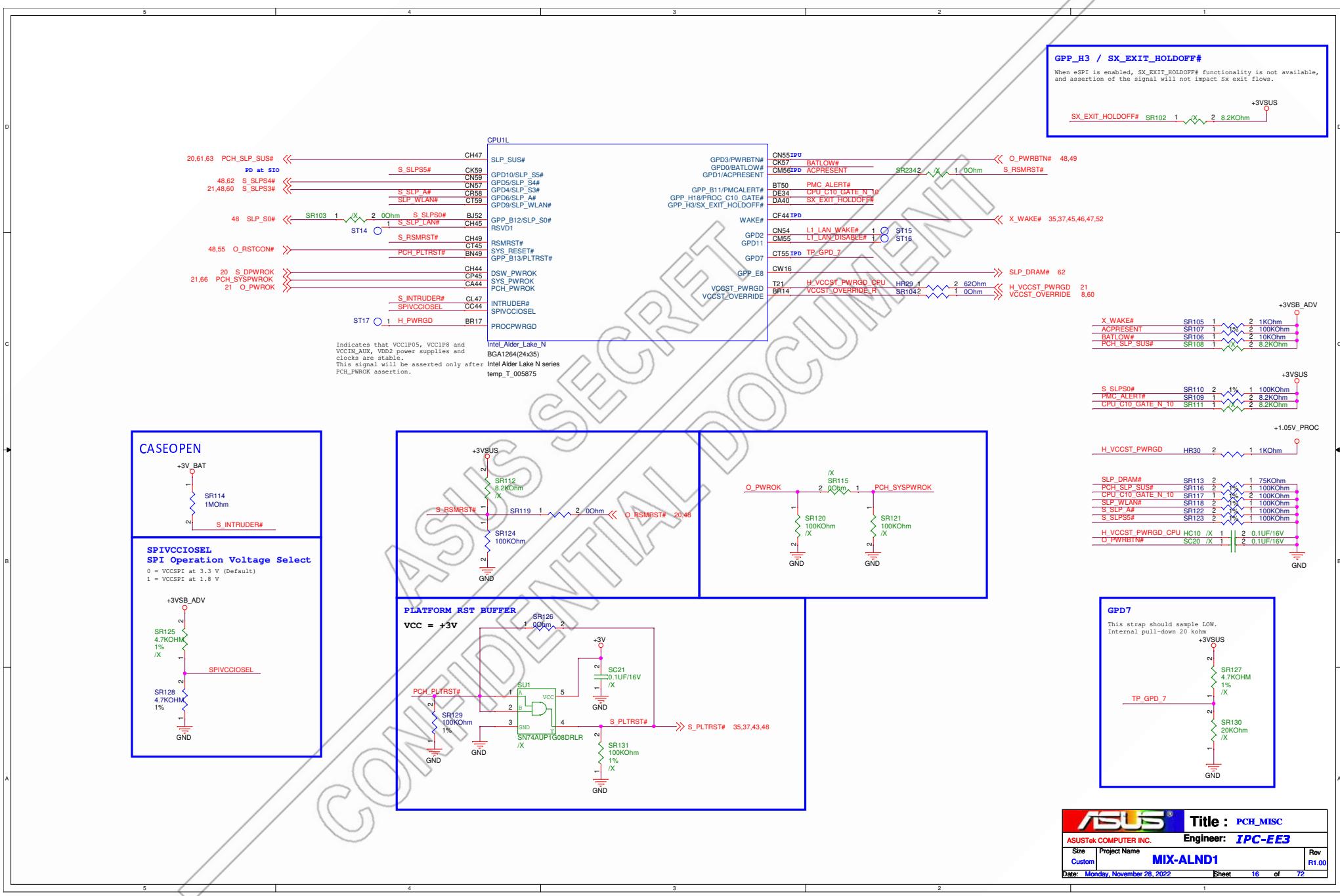
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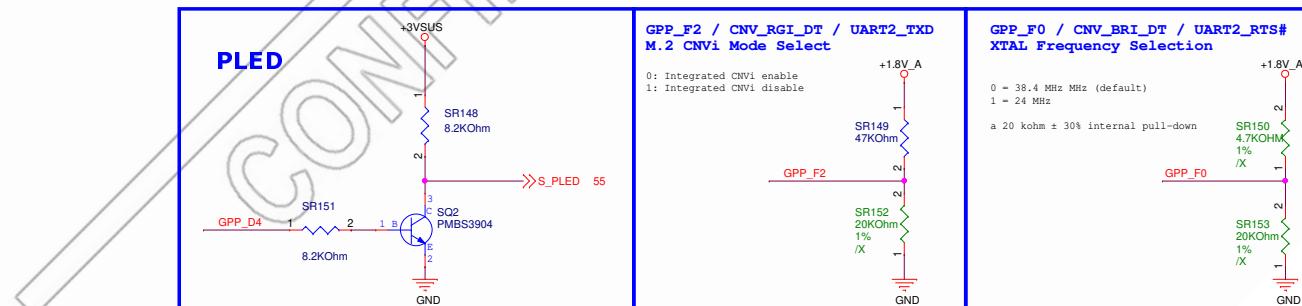
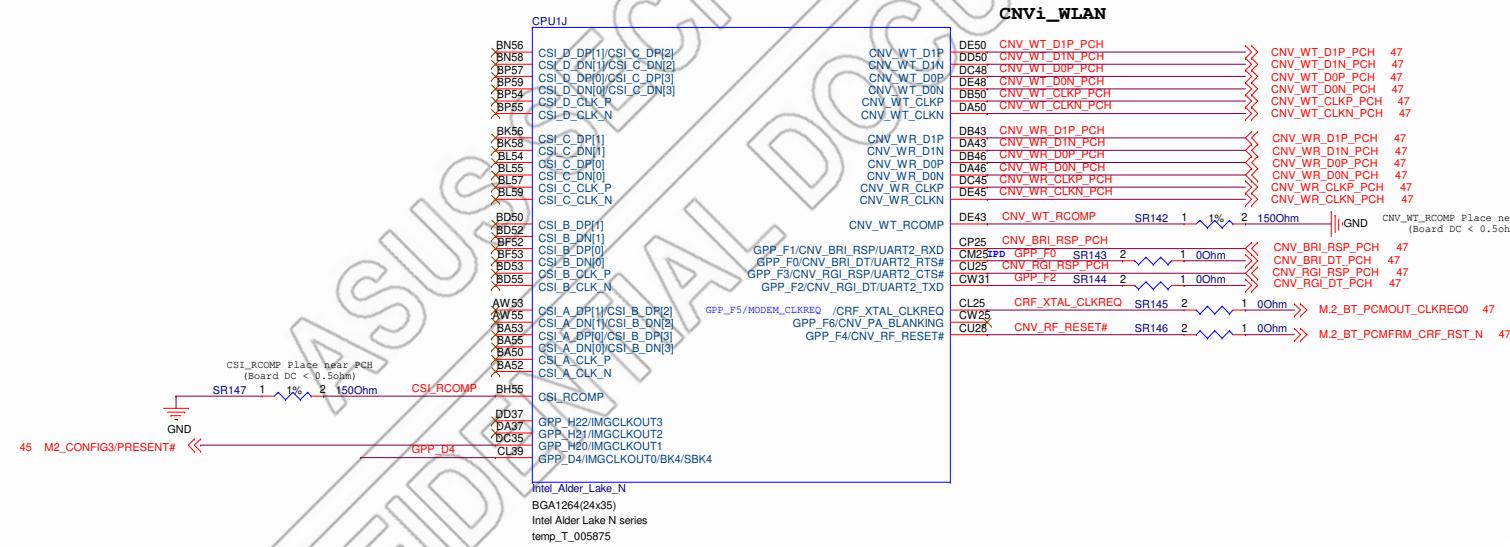
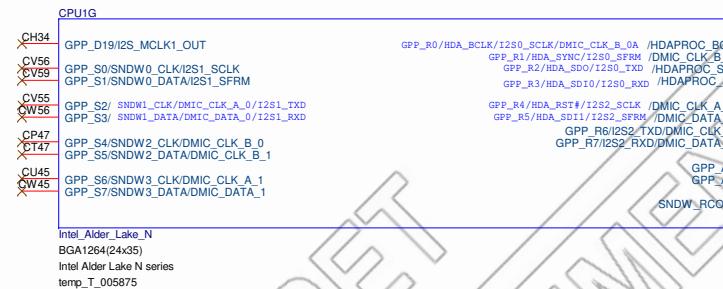
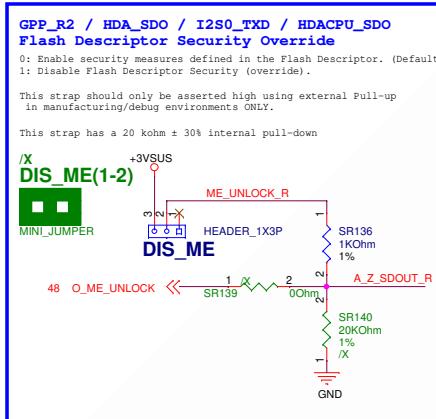
ASUS ®		Title : XXXX	
ASUSTek COMPUTER INC.		Engineer: IPC-EE3	
Size	Project Name	Rev	
Custom	MIX-ALND 1	R1.00	
Date: Monday, November 28, 2022	Sheet 1	of 72	

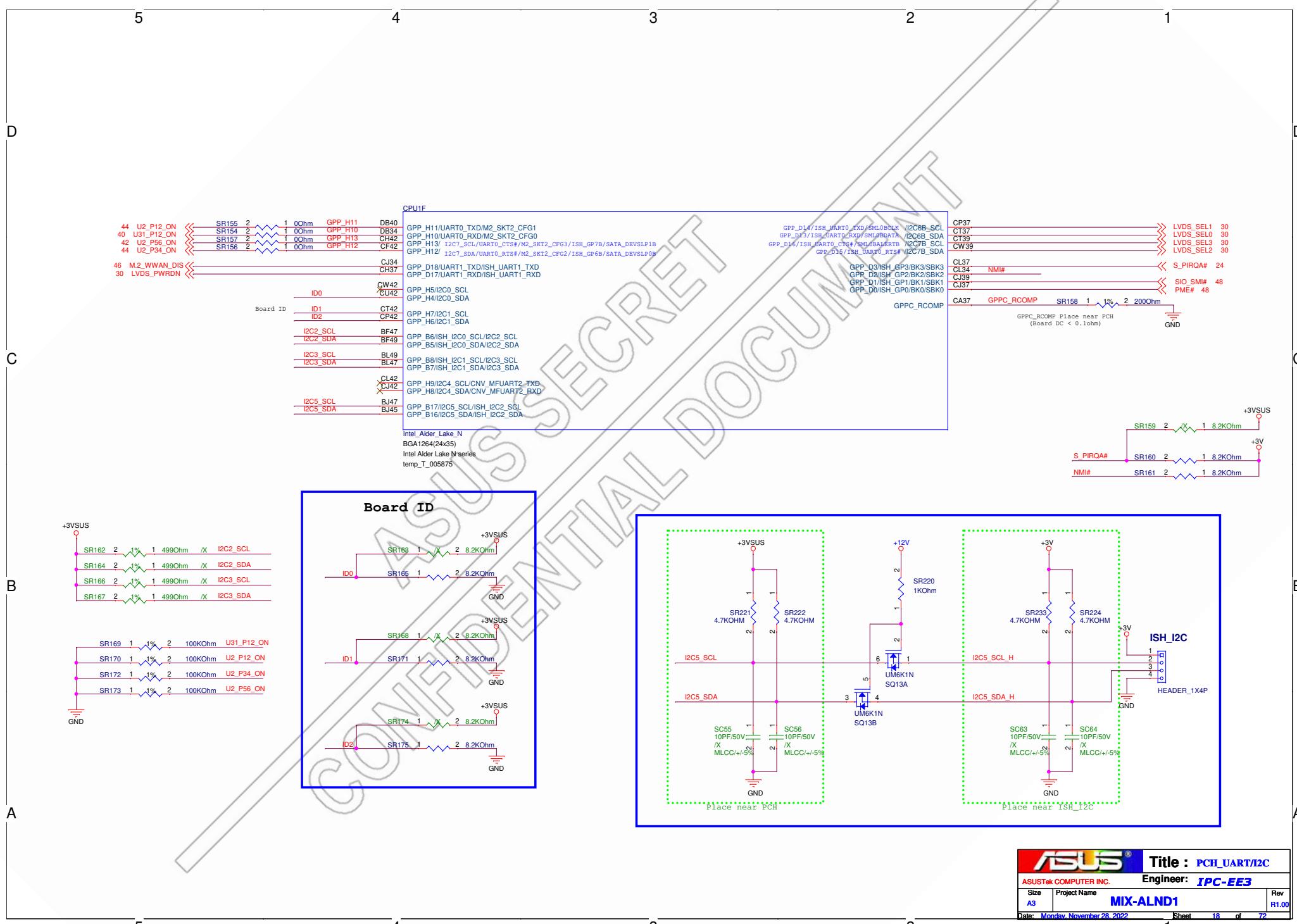


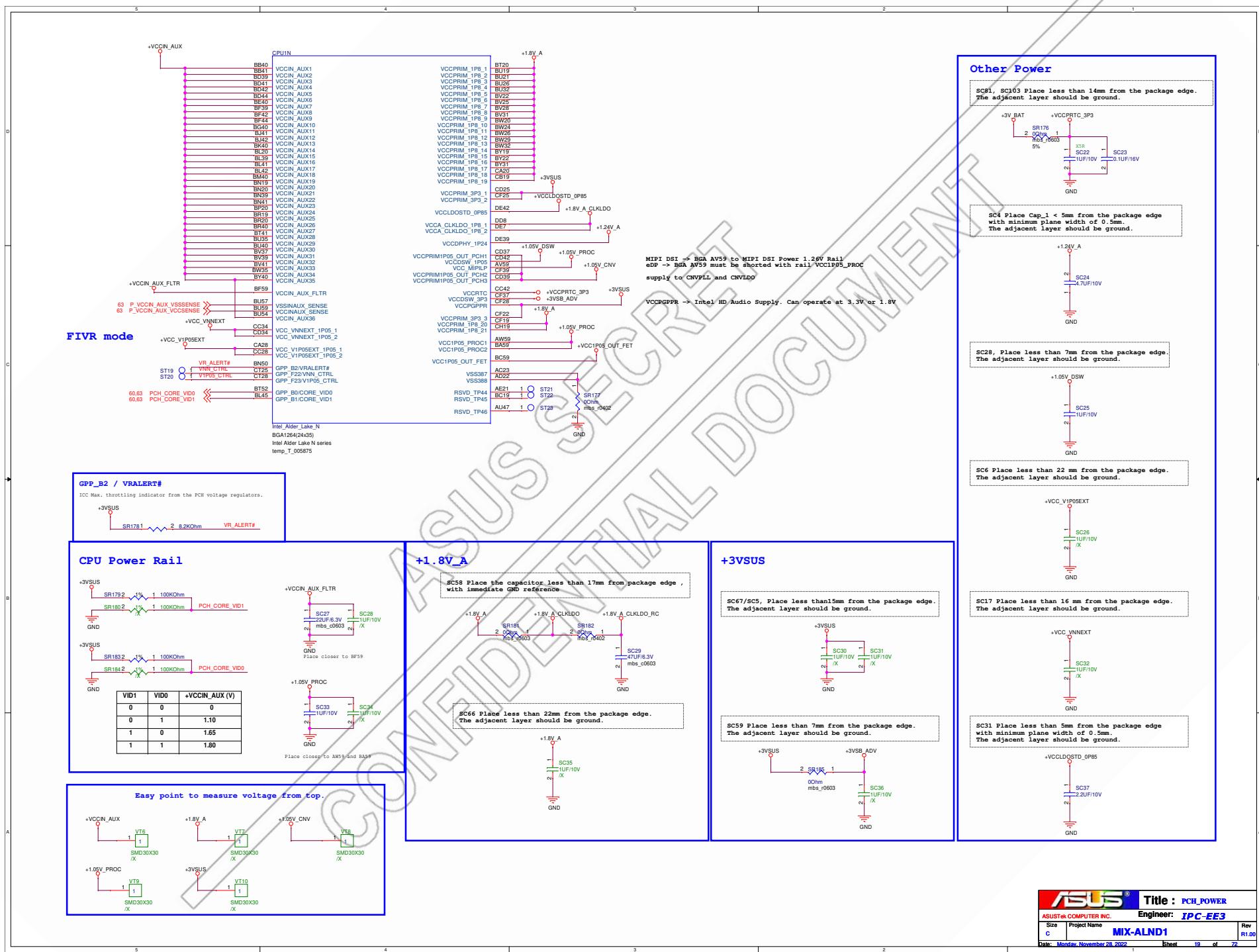












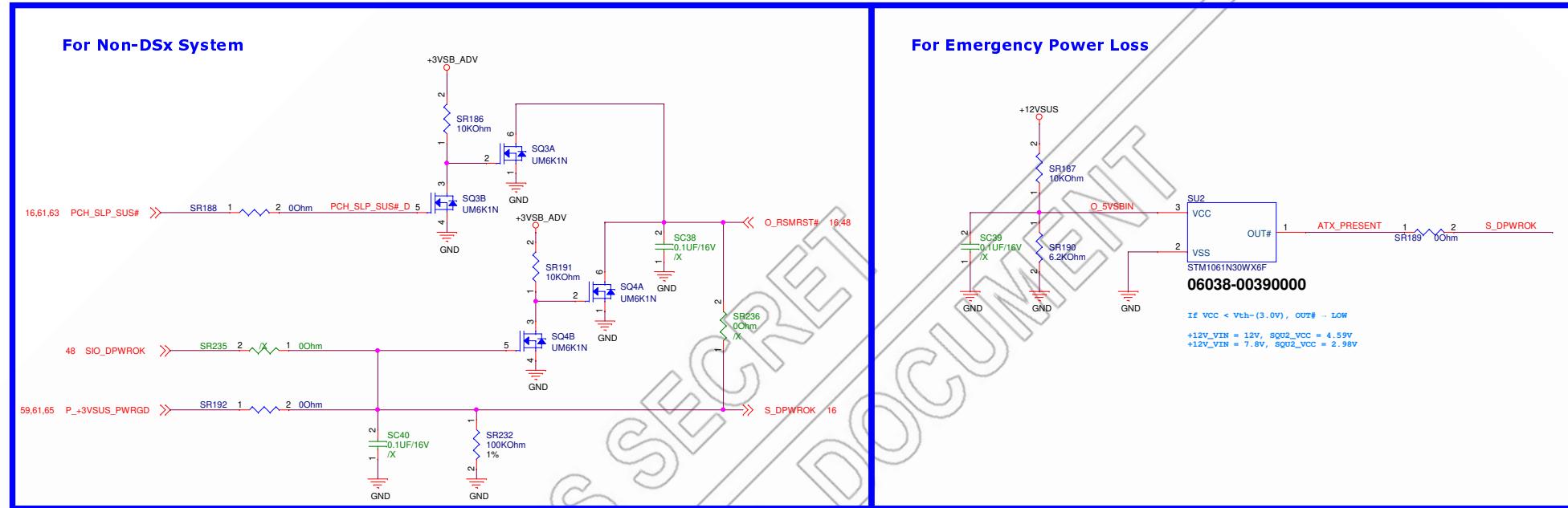
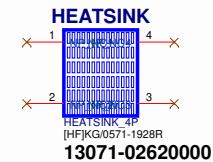
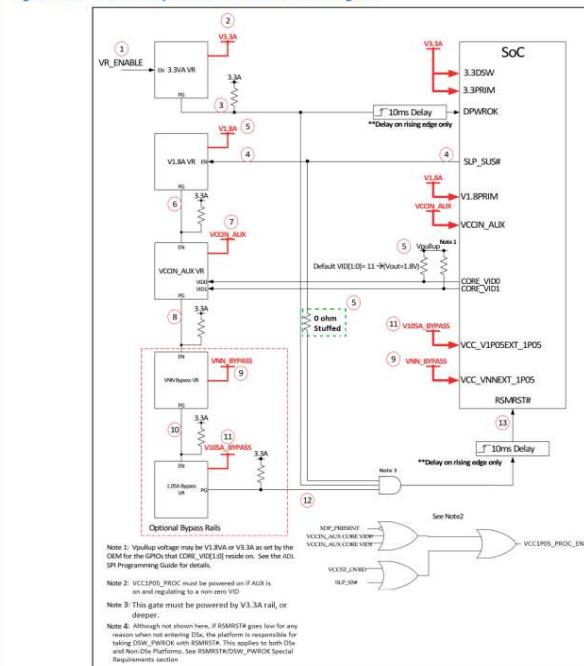


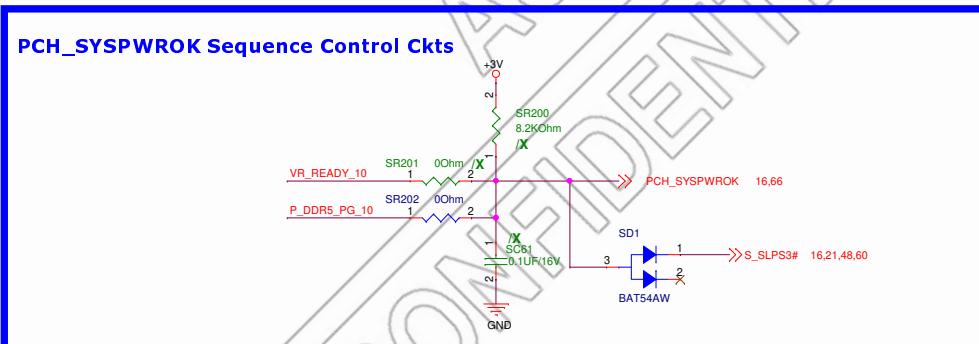
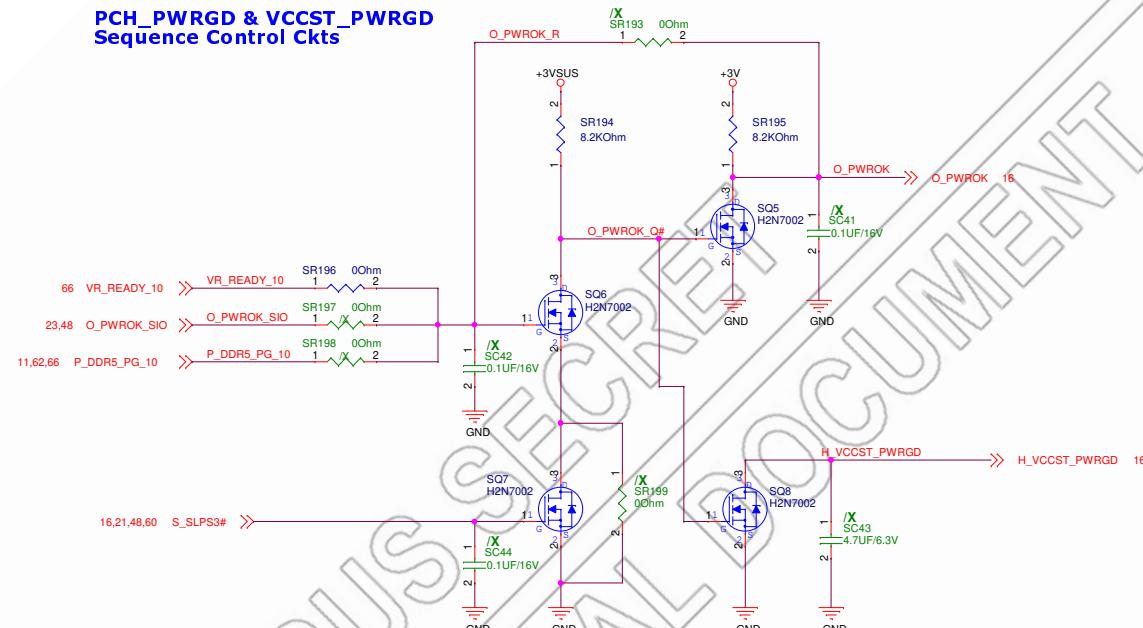
Figure 383. Non-DSx System Architecture Block Diagram



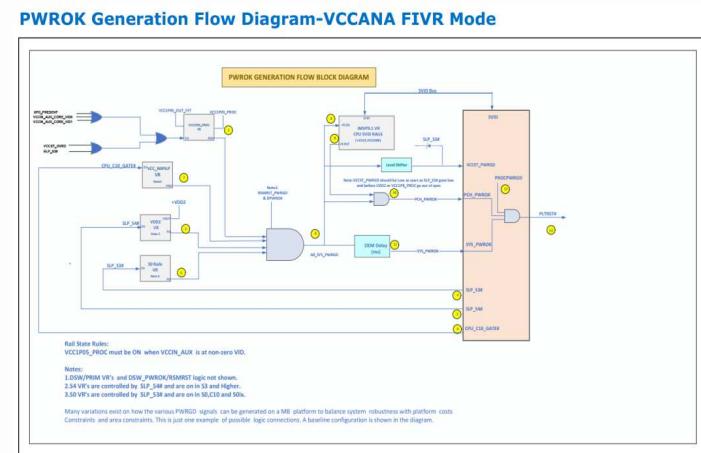
CPU HEATSINK

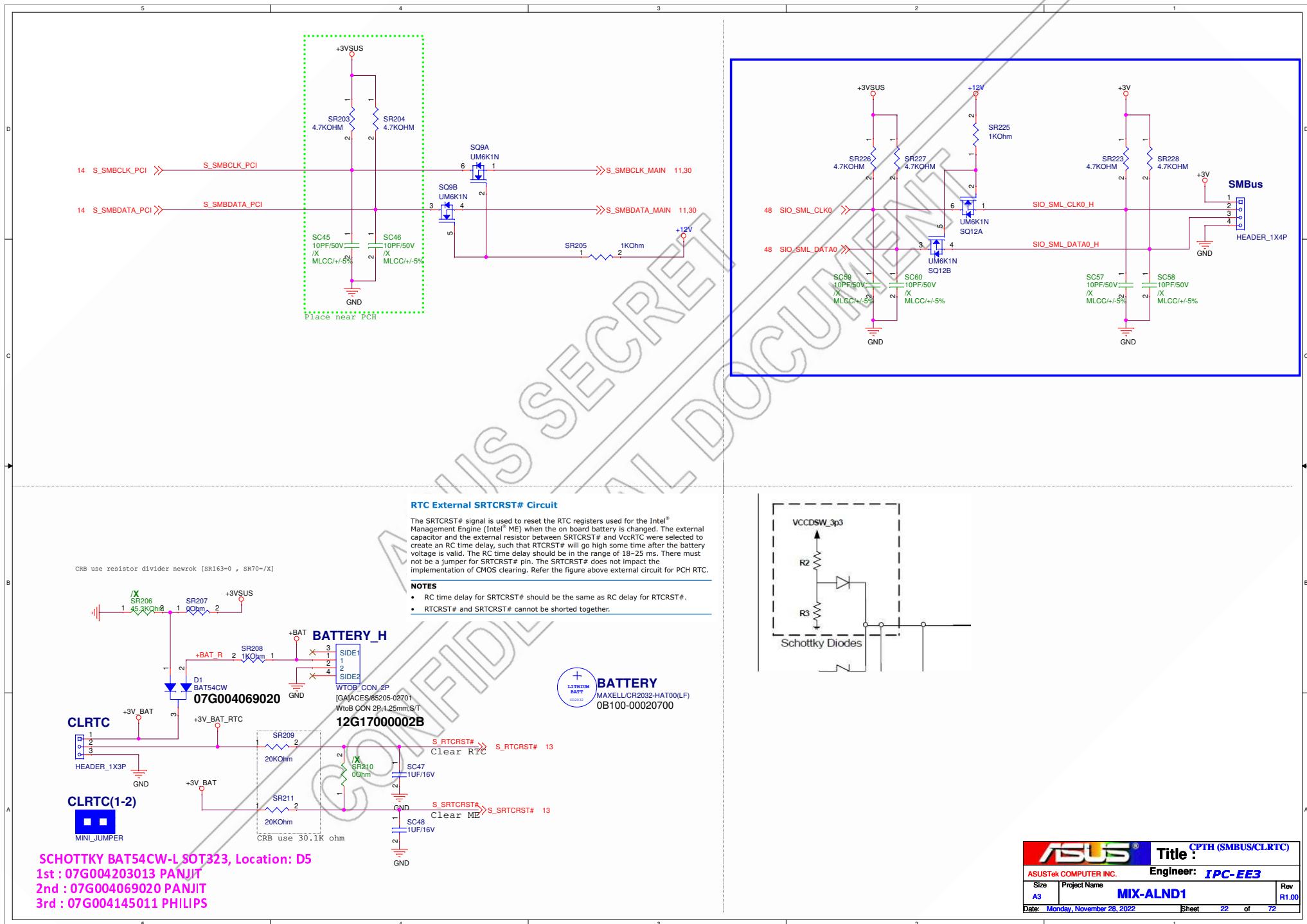
15W/9W -> P/N : 13071-02620000 KG/0571-192

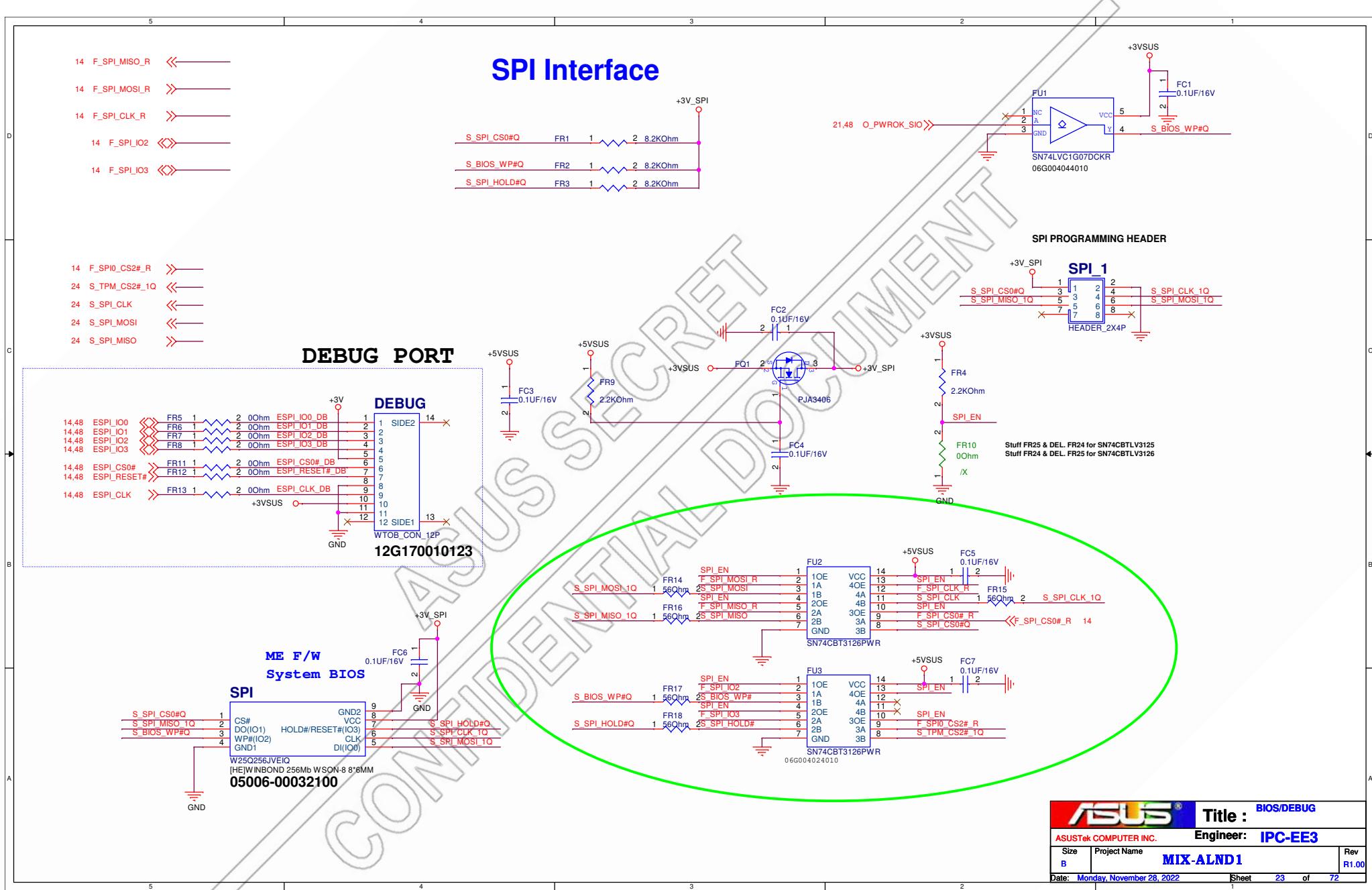
6W -> P/N : 13071-04110000 KG/0571-X2428-010F



1. tBLT05 -> ALL_SYS_PWRGD assertion to SYS_PWROK, no limit.
2. tCPU16 -> VCCST_PWRGD assertion to PCH_PWROK assertion ≥ 0 ns.
3. tCPU100 -> VDD2 ramped and stable to VCCST_PWRGD assertion ≥ 2 ms

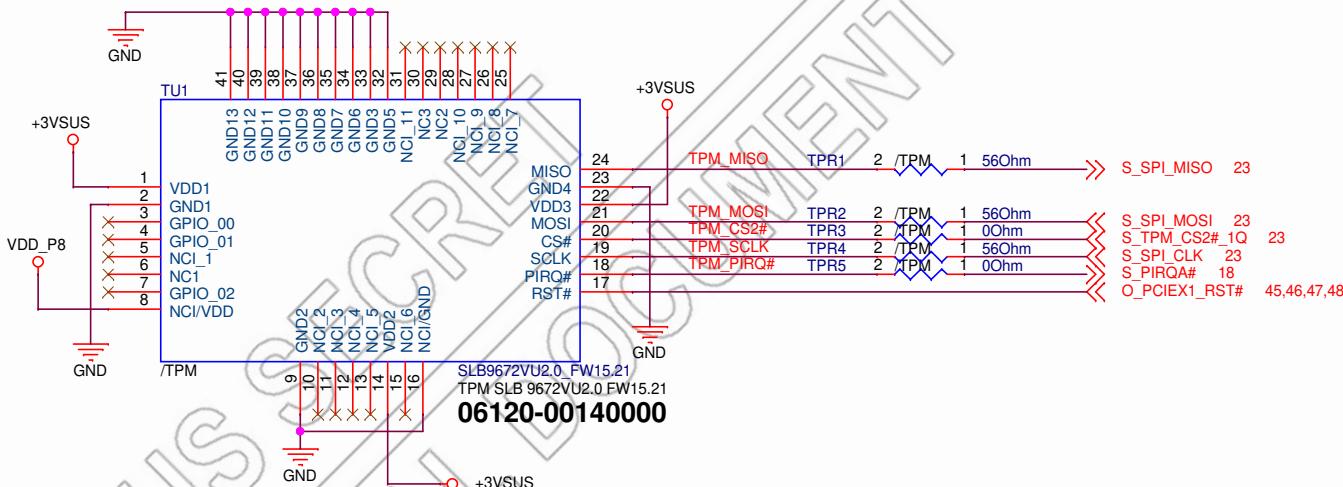






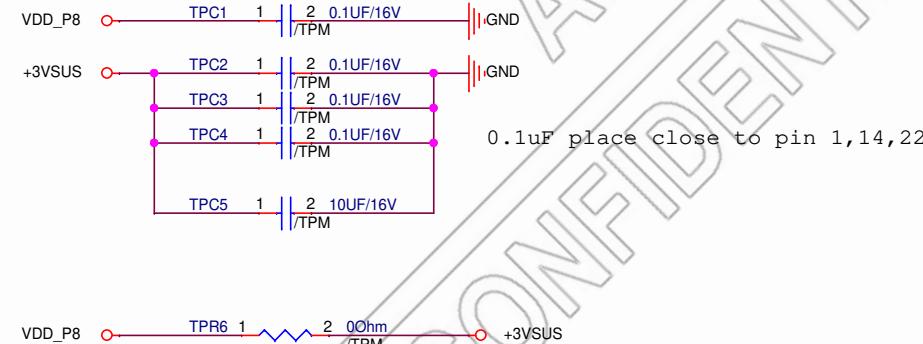
TPM

D



C

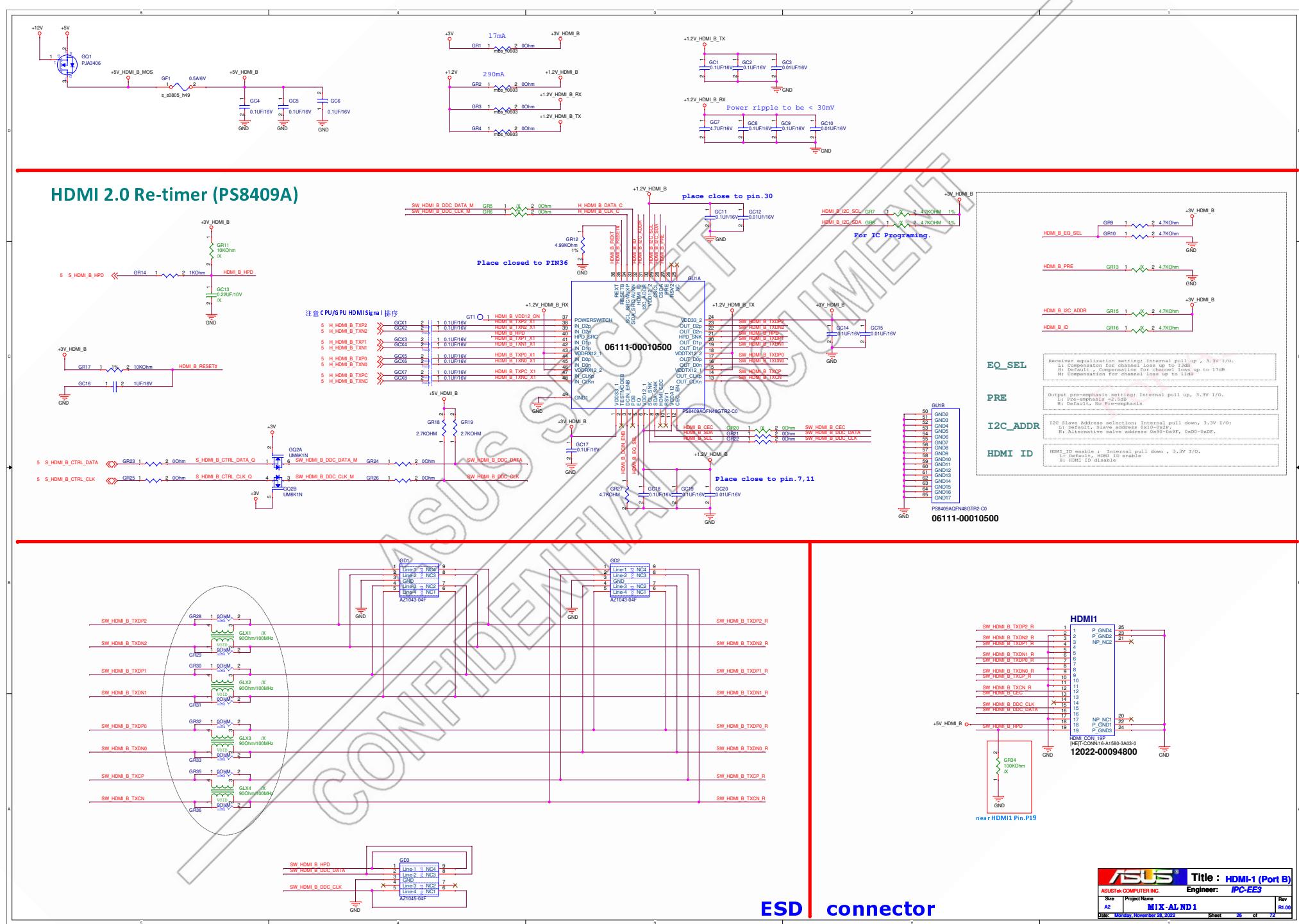
B

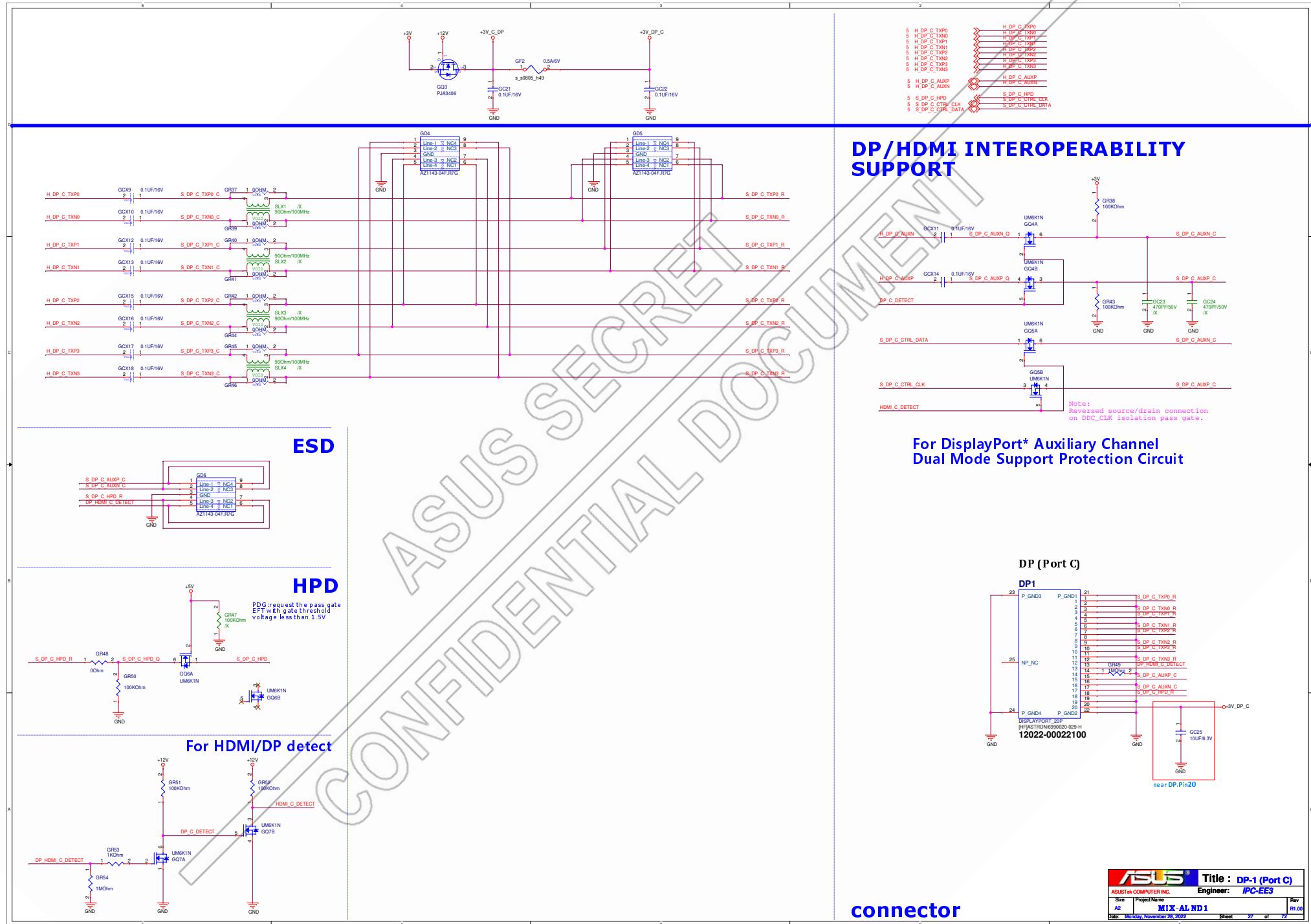


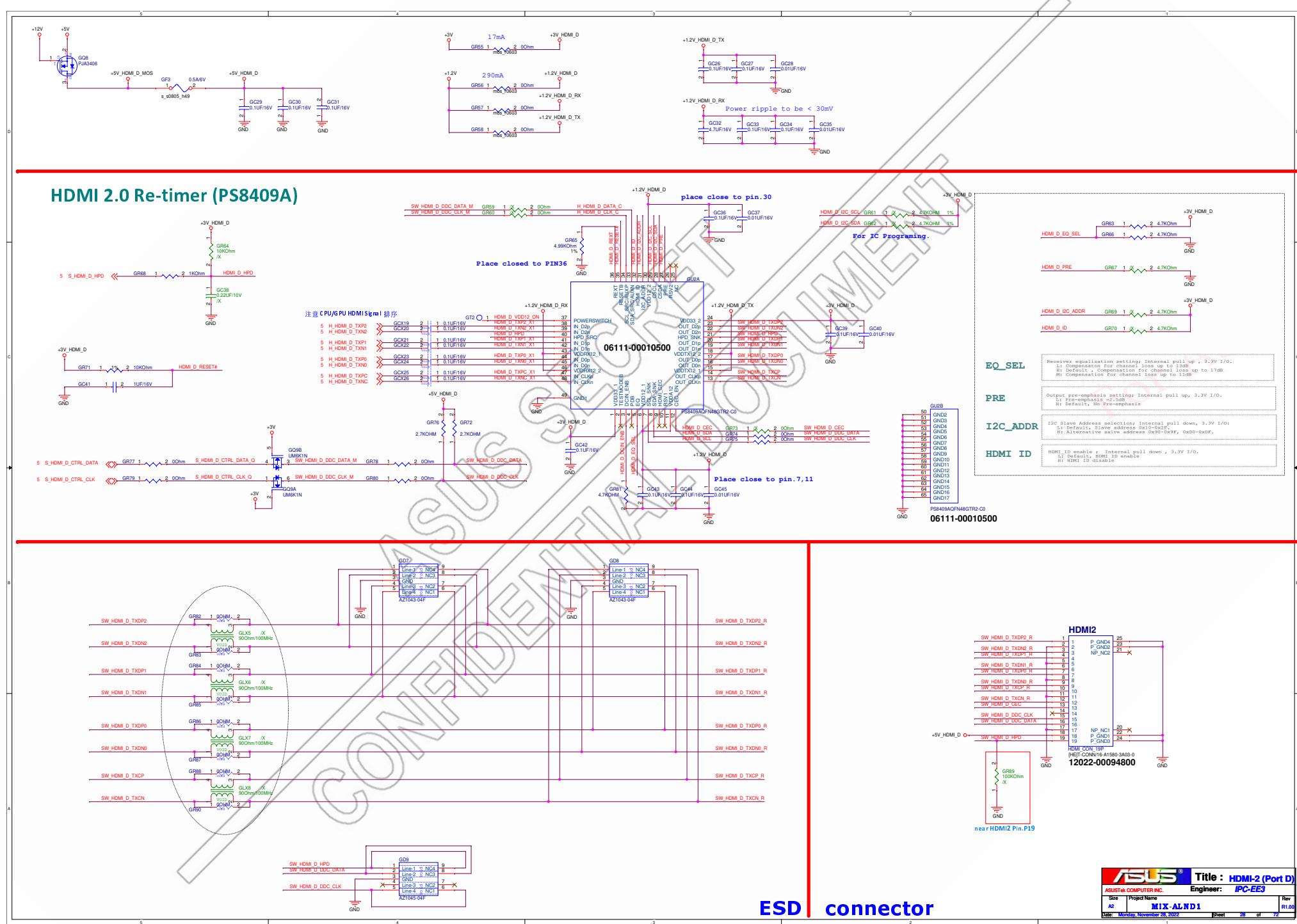
A

VDD_P8 → TPR6 1 → 0Ohm → +3VSUS

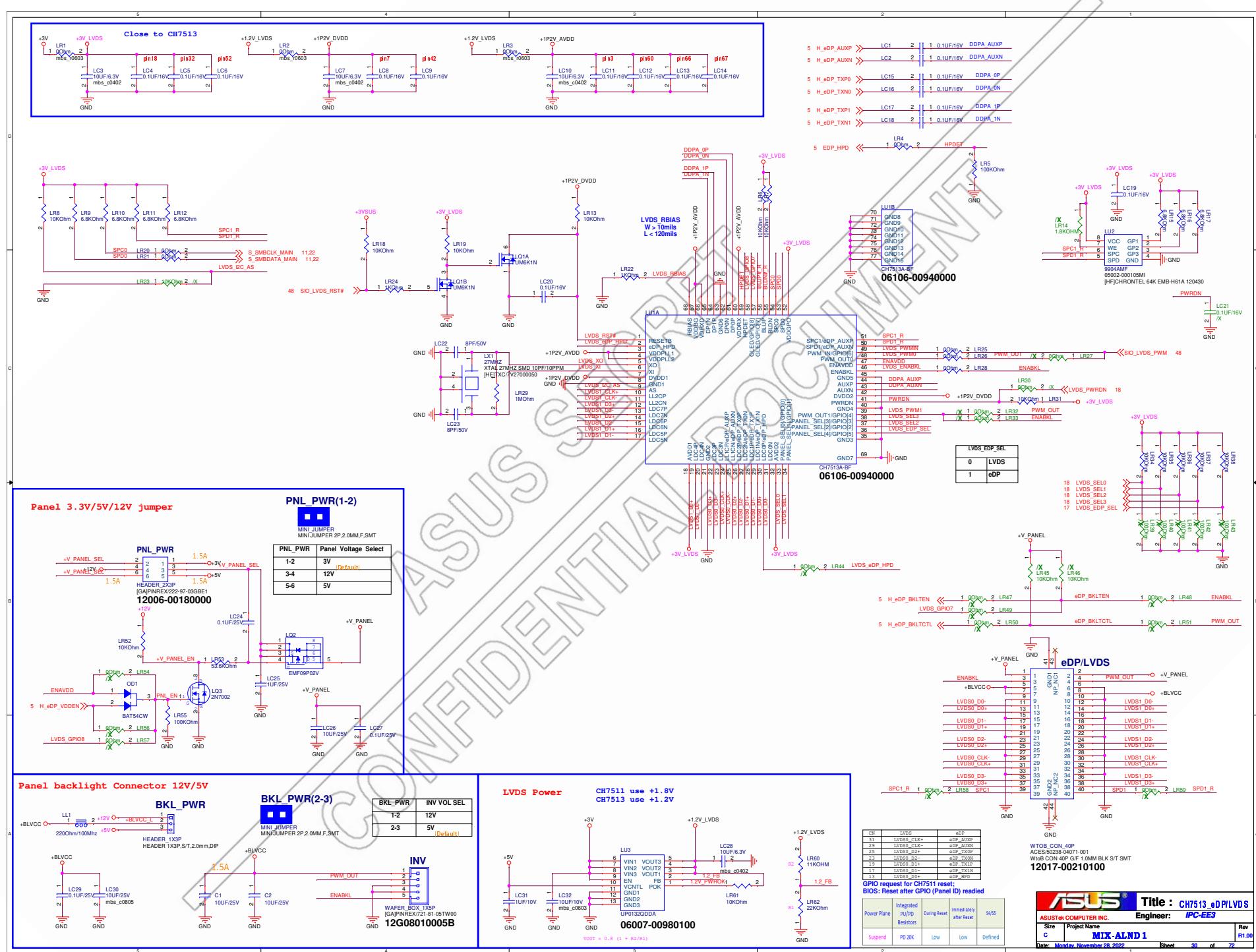
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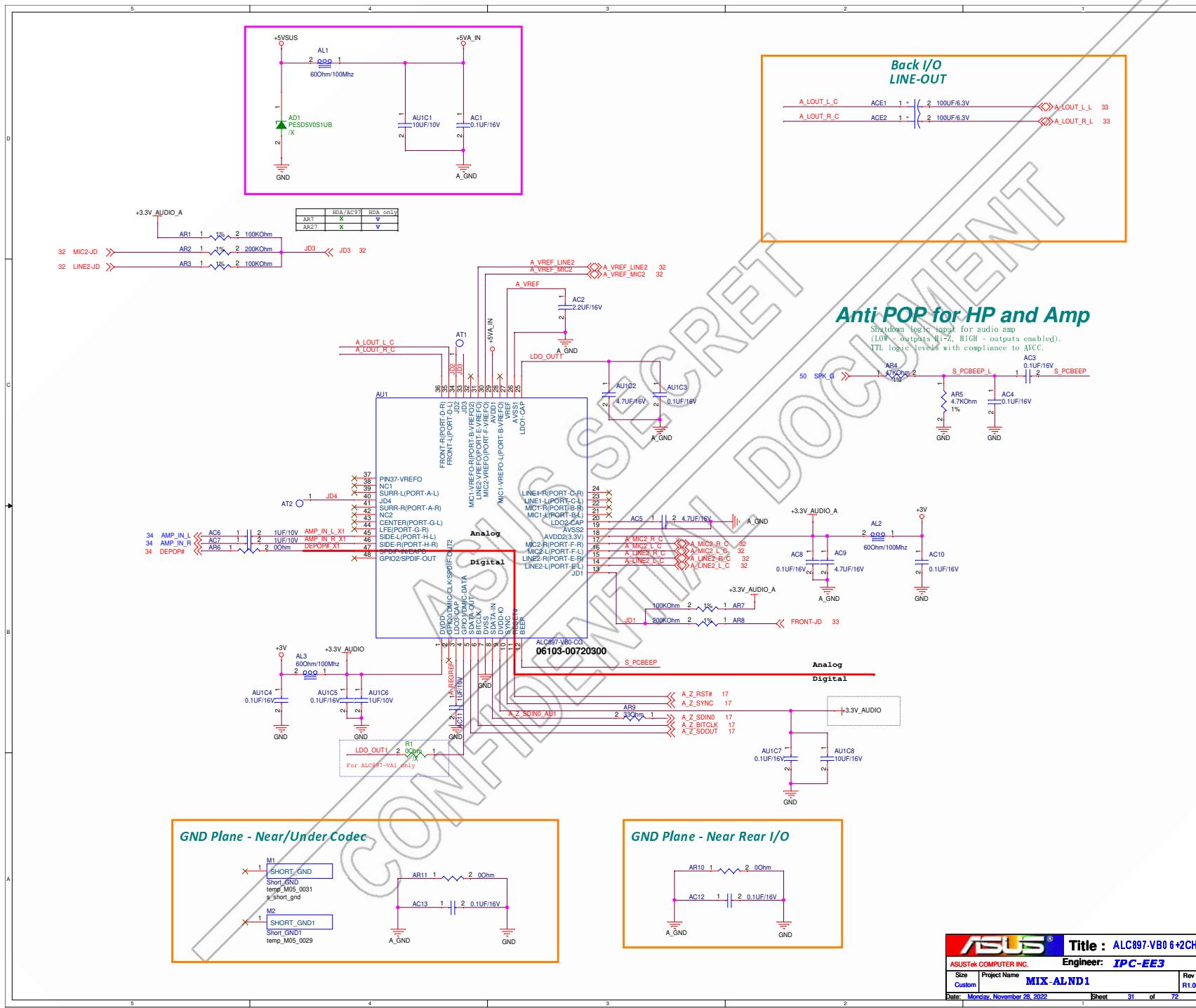


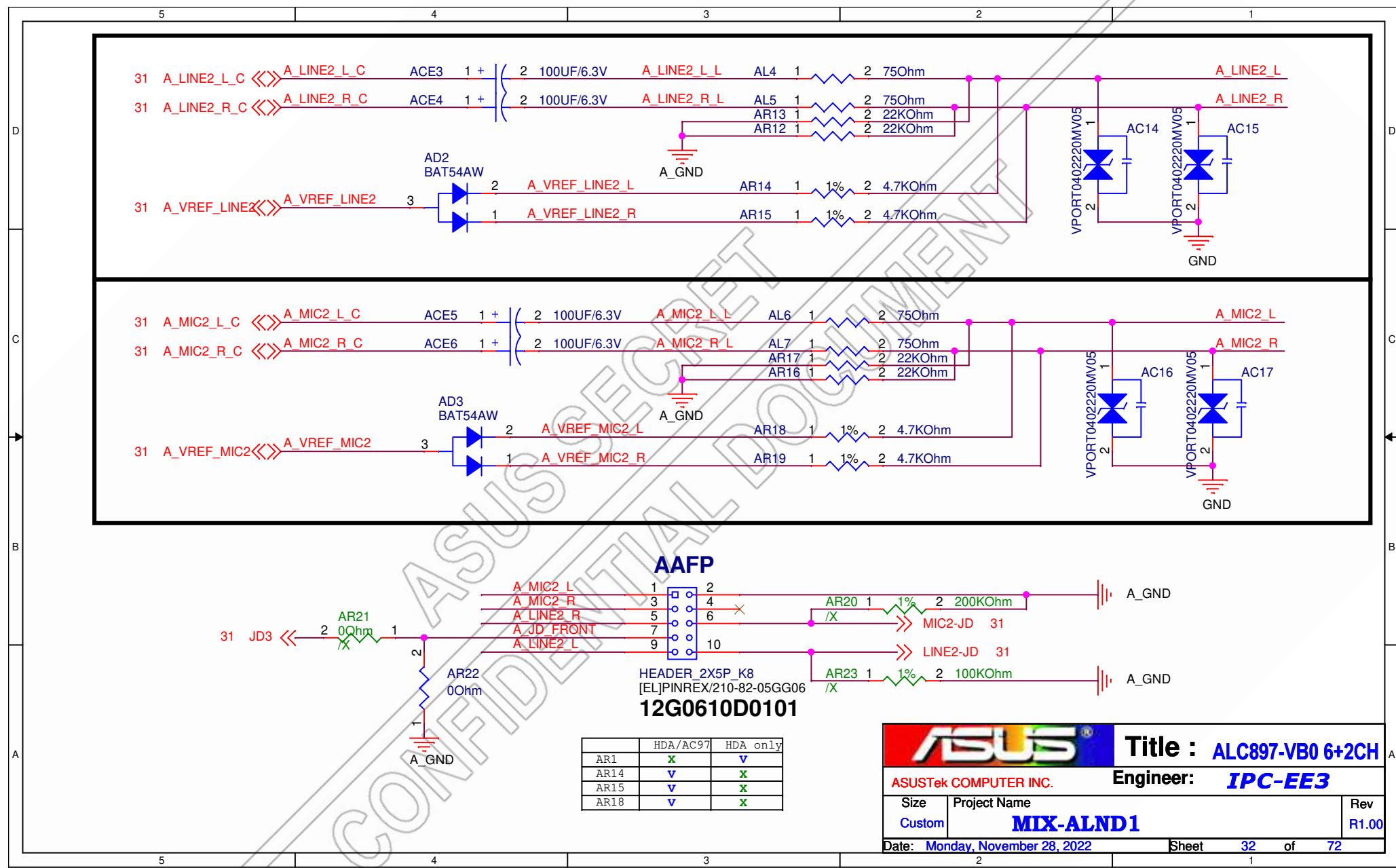




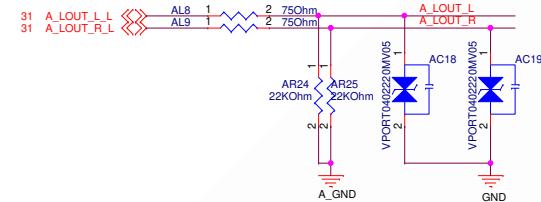
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**Back I/O
LINE-OUT/MIC-IN**



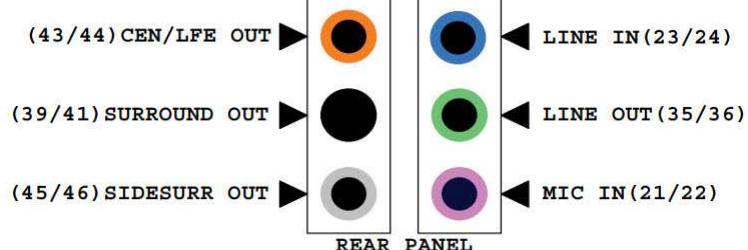
SPDIF Optical

A-11

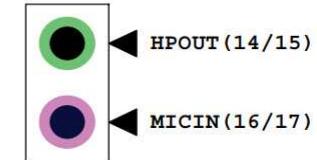
SPDIF Optical (High Rise)

A-12

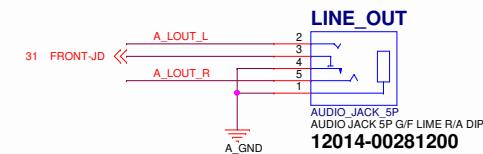
REAR PANEL PHONJACK



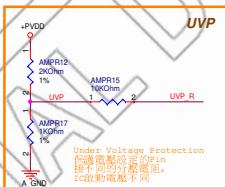
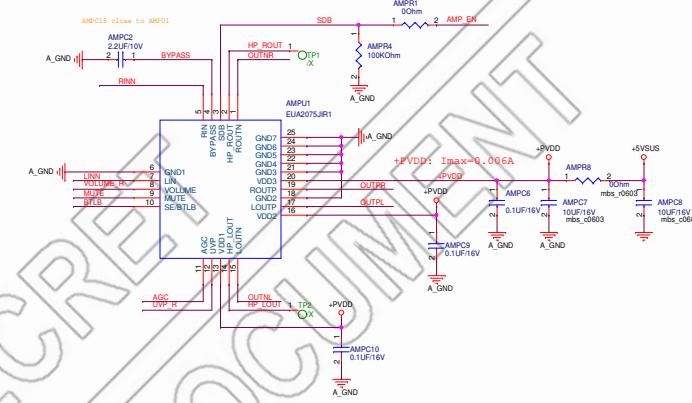
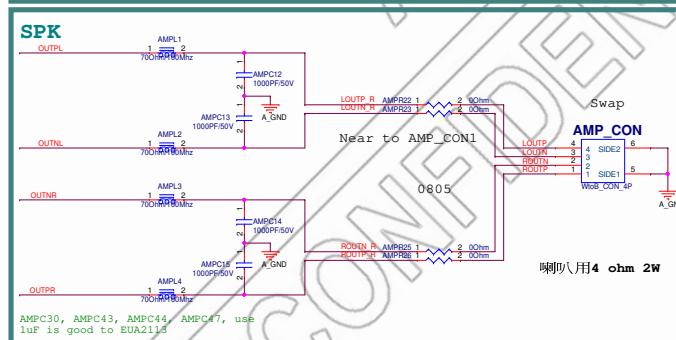
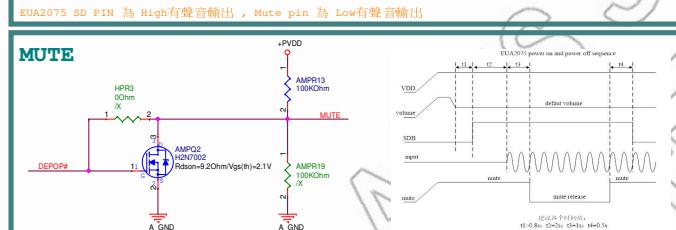
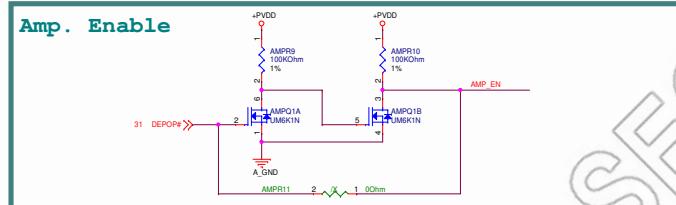
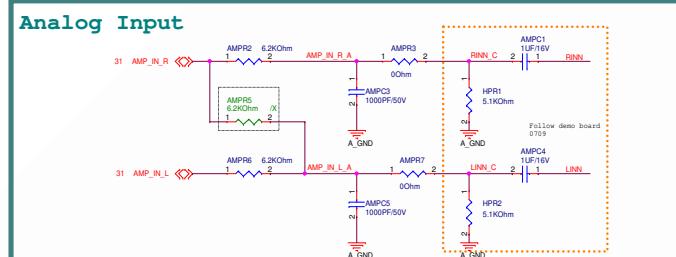
FRONT PANEL PHONJACK



ALC897Q (7.1 + 2 Channel)
REAR Panel: 6 re-tasking audio jacks
FRONT Panel: 2 re-tasking audio jacks



AMP - EUA2075JIR1 (Only Speaker)



The thresholds can be determined as below:

With the condition: $R_3 \gg R_1/R_2$

$V_{UVP} = [1.2 - (5.7 \cdot A \cdot R_3)] \cdot (R_1 + R_2) / R_2$

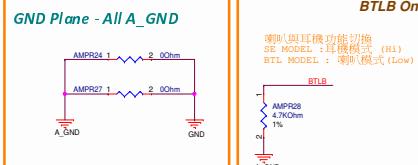
Hysteresis = $(4.6 \cdot A \cdot R_3) \cdot (R_1 + R_2) / R_2$

Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)
1	0.0 - 3.3	2.4 - 0.0	20.0
2	3.4 - 4.8	3.8 - 2.4	19.6
3	4.8 - 6.2	5.2 - 3.8	19.2
4	6.2 - 7.6	6.8 - 5.2	18.8
5	7.6 - 9.0	8.0 - 6.6	18.4
6	9.0 - 10.4	9.4 - 8.0	18.0
7	10.4 - 11.8	10.8 - 9.4	17.6
8	11.8 - 13.2	12.2 - 10.8	17.2
9	13.2 - 14.6	13.6 - 12.2	16.8
10	14.6 - 16.0	15.0 - 13.6	16.4
11	16.0 - 17.4	16.4 - 15.0	16.0
12	17.4 - 18.8	17.8 - 16.4	15.6
13	18.8 - 20.2	19.2 - 17.8	15.2
14	20.2 - 21.6	20.6 - 19.2	14.8
15	21.6 - 23.0	22.0 - 20.6	14.4
16	23.0 - 24.4	23.4 - 22.0	14.0
17	24.4 - 25.8	24.8 - 23.4	13.6
18	25.8 - 27.2	26.2 - 24.8	13.2
19	27.2 - 28.6	27.6 - 26.2	12.8
20	28.6 - 30.0	30.0 - 28.0	12.4
21	30.0 - 31.4	30.4 - 29.0	12.0

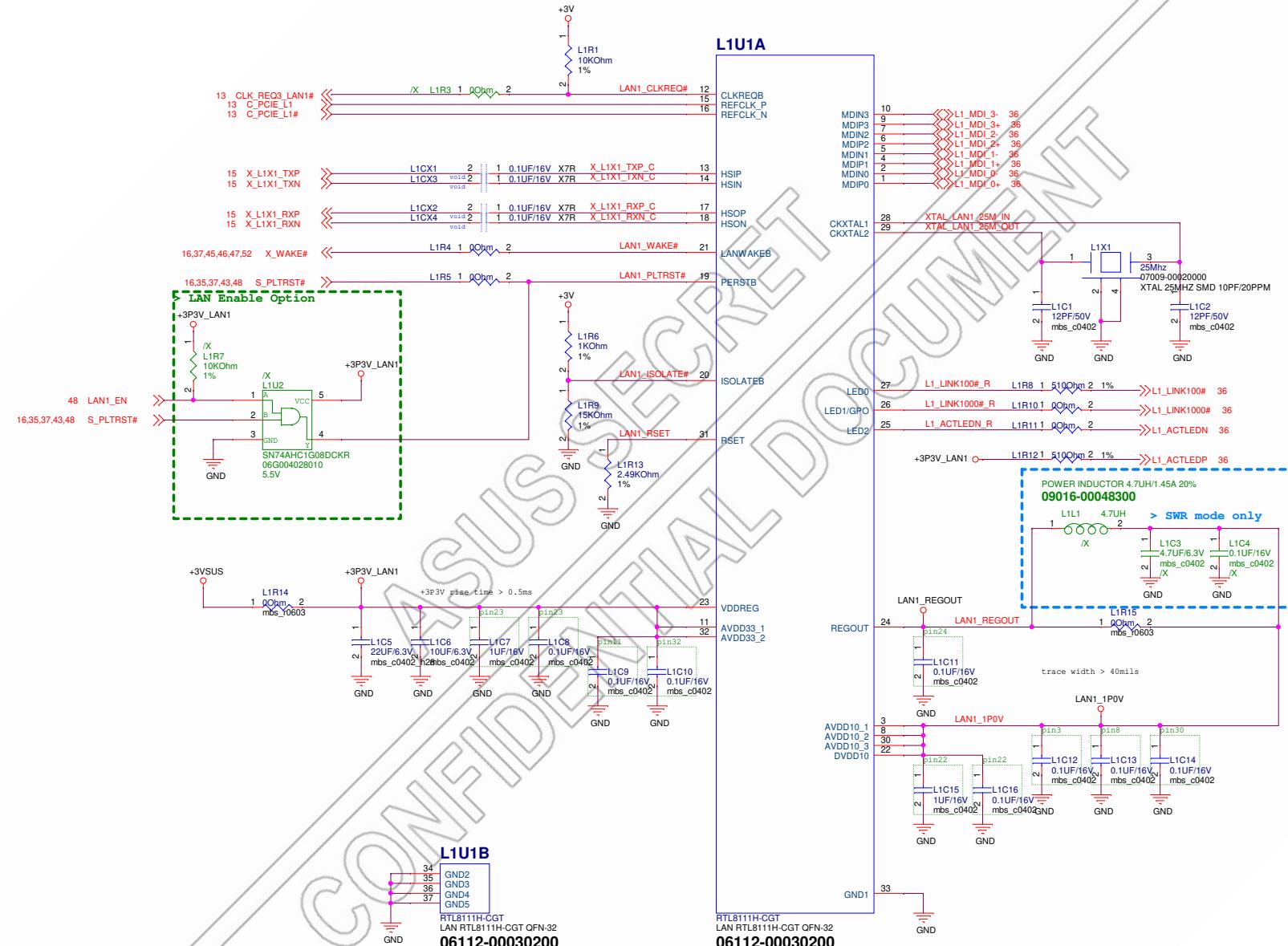
Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)
1	0.0 - 3.3	2.4 - 0.0	20.0
2	3.4 - 4.8	3.8 - 2.4	19.6
3	4.8 - 6.2	5.2 - 3.8	19.2
4	6.2 - 7.6	6.8 - 5.2	18.8
5	7.6 - 9.0	8.0 - 6.6	18.4
6	9.0 - 10.4	9.4 - 8.0	18.0
7	10.4 - 11.8	10.8 - 9.4	17.6
8	11.8 - 13.2	12.2 - 10.8	17.2
9	13.2 - 14.6	13.6 - 12.2	16.8
10	14.6 - 16.0	15.0 - 13.6	16.4
11	16.0 - 17.4	16.4 - 15.0	16.0
12	17.4 - 18.8	17.8 - 16.4	15.6
13	18.8 - 20.2	19.2 - 17.8	15.2
14	20.2 - 21.6	20.6 - 19.2	14.8
15	21.6 - 23.0	22.0 - 20.6	14.4
16	23.0 - 24.4	23.4 - 22.0	14.0
17	24.4 - 25.8	24.8 - 23.4	13.6
18	25.8 - 27.2	26.2 - 24.8	13.2
19	27.2 - 28.6	27.6 - 26.2	12.8
20	28.6 - 30.0	30.0 - 28.0	12.4
21	30.0 - 31.4	30.4 - 29.0	12.0

Speaker 4 ohm 2W 0.45VDD~0.27VDD: 1.93W

Auto Gain Control
最大功率的音頻喇叭進行保護
若輸出超過最大功率值
AGC 會自動降低到設定值



LAN RTL8111H



BTI 8111H

1st P/N : 06112-00030200 REALTEK/LAN RTL8111H-CGT QFN-32

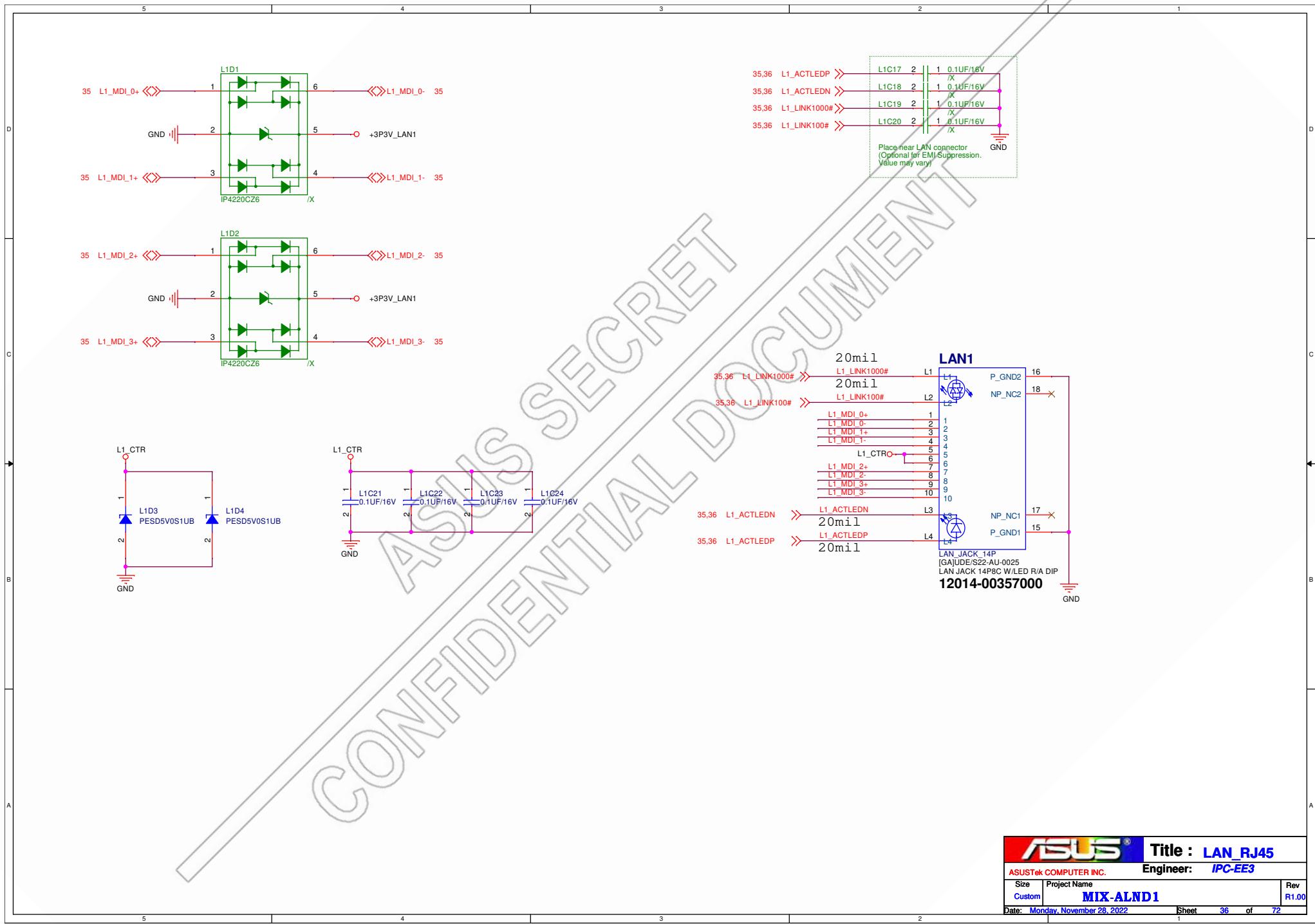
2nd P/N : 06112-00030500 REALTEK/LAN RTL8111H-VB-CG QFN-32

ASUS®

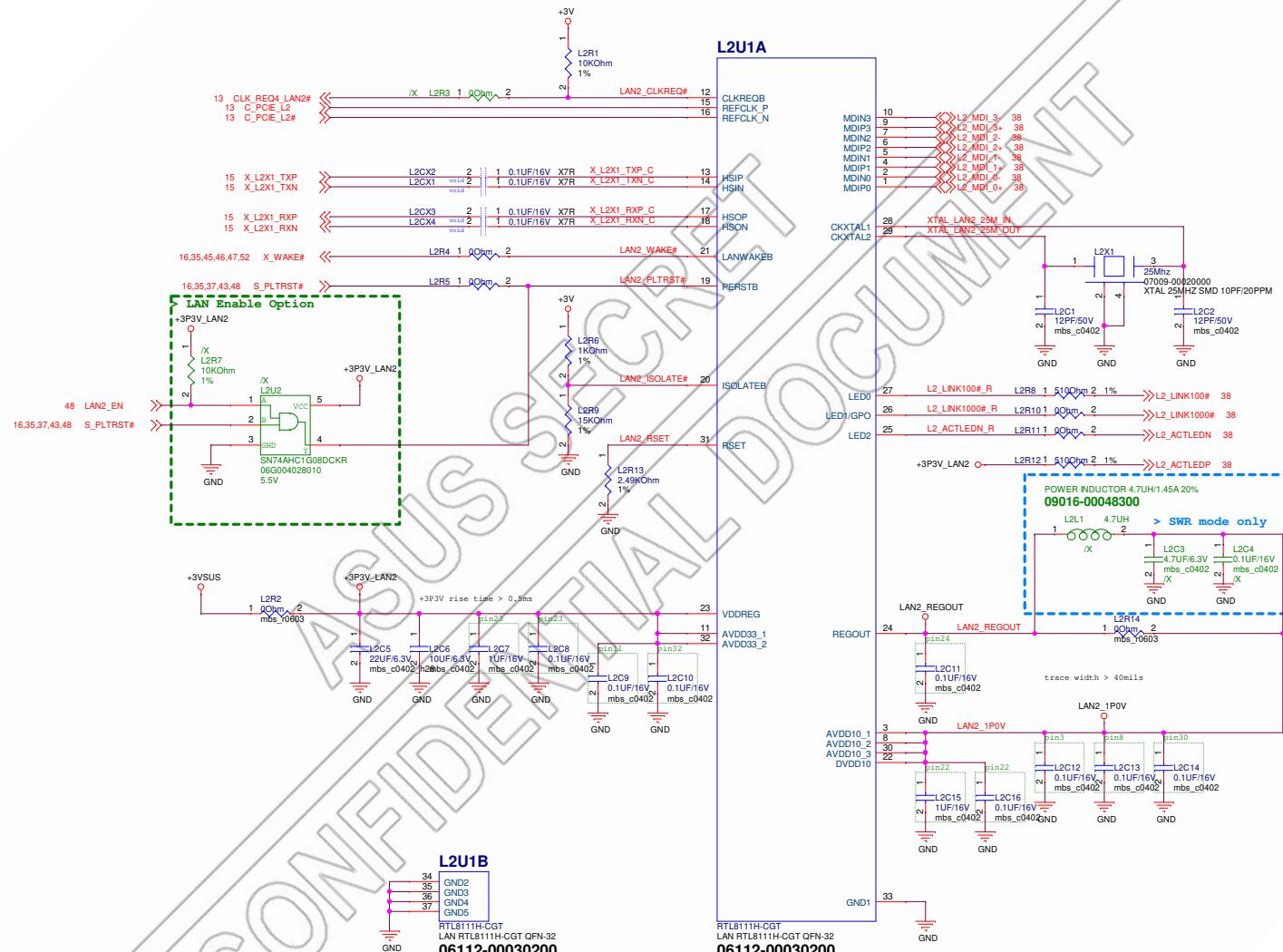
Title: [View Details](#)

Title : LAN RTI

ASUSTek COMPUTER INC.		Engineer: IPC-EE3		
Size A3	Project Name MIX-ALND1			Rev R1.00
Date: Monday, November 28, 2022	Sheet 25	of 72		



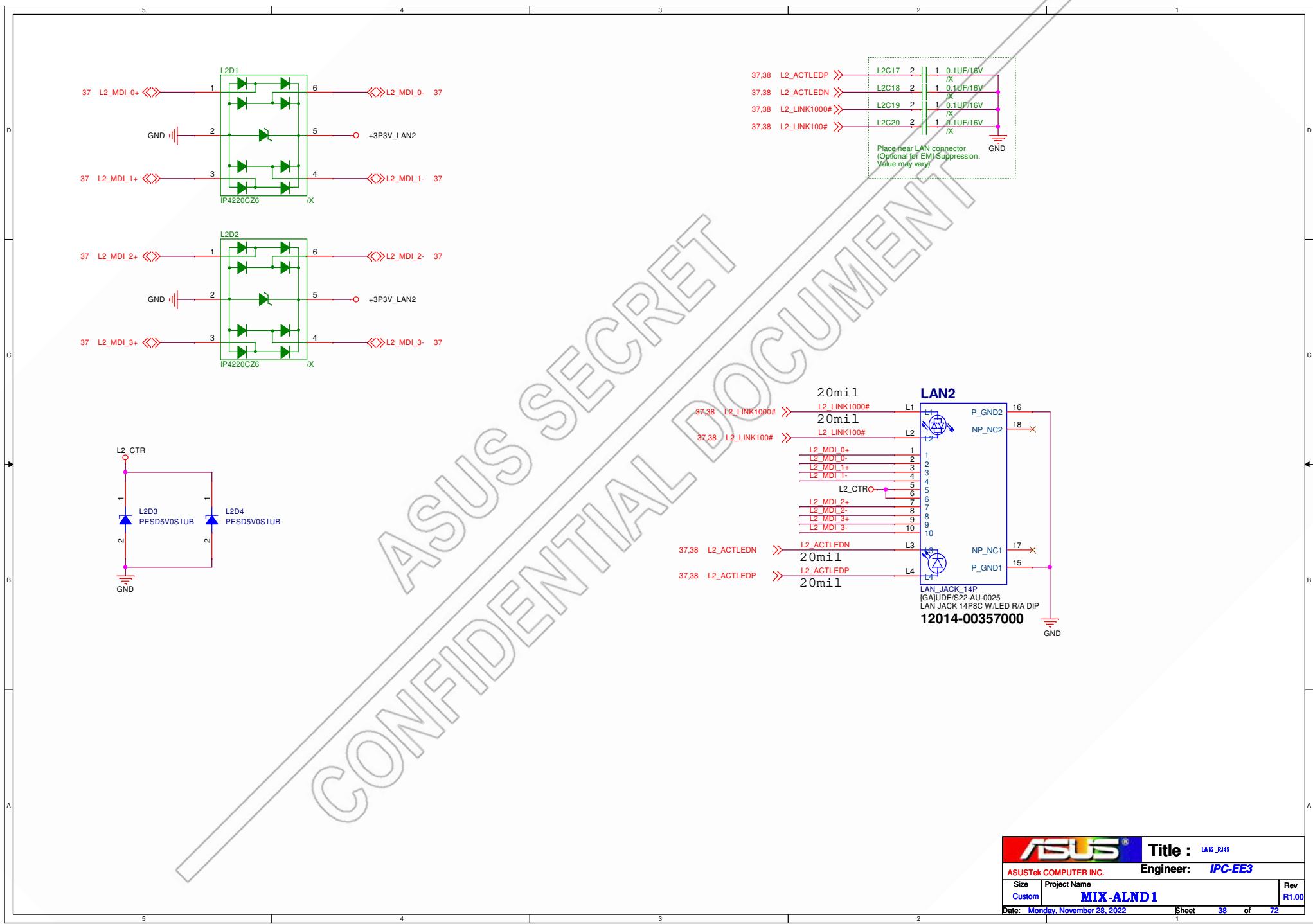
LAN RTL8111H



RTL8111H

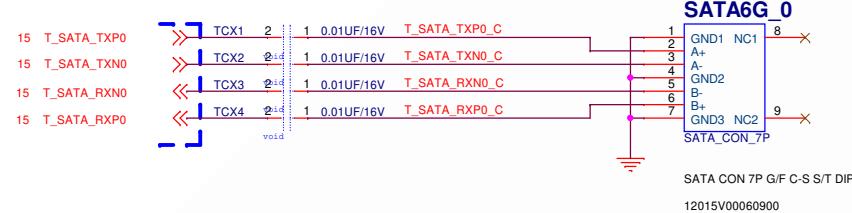
1st P/N : 06112-00030200 REALTEK/LAN RTL8111H-CGT QFN-32
2nd P/N : 06112-00030500 REALTEK/LAN RTL8111H-VB-CG QFN-32

Title : LAN2_RTL811H	
ASUSTek COMPUTER INC.	
Size	Project Name
Custom	MIX-ALND1
Rev	R1.00
Date	Monday, November 28, 2022
Sheet	37 of 72



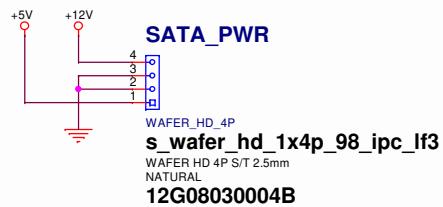
5 1 4 3 2 1

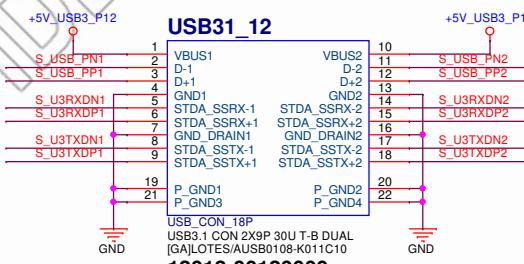
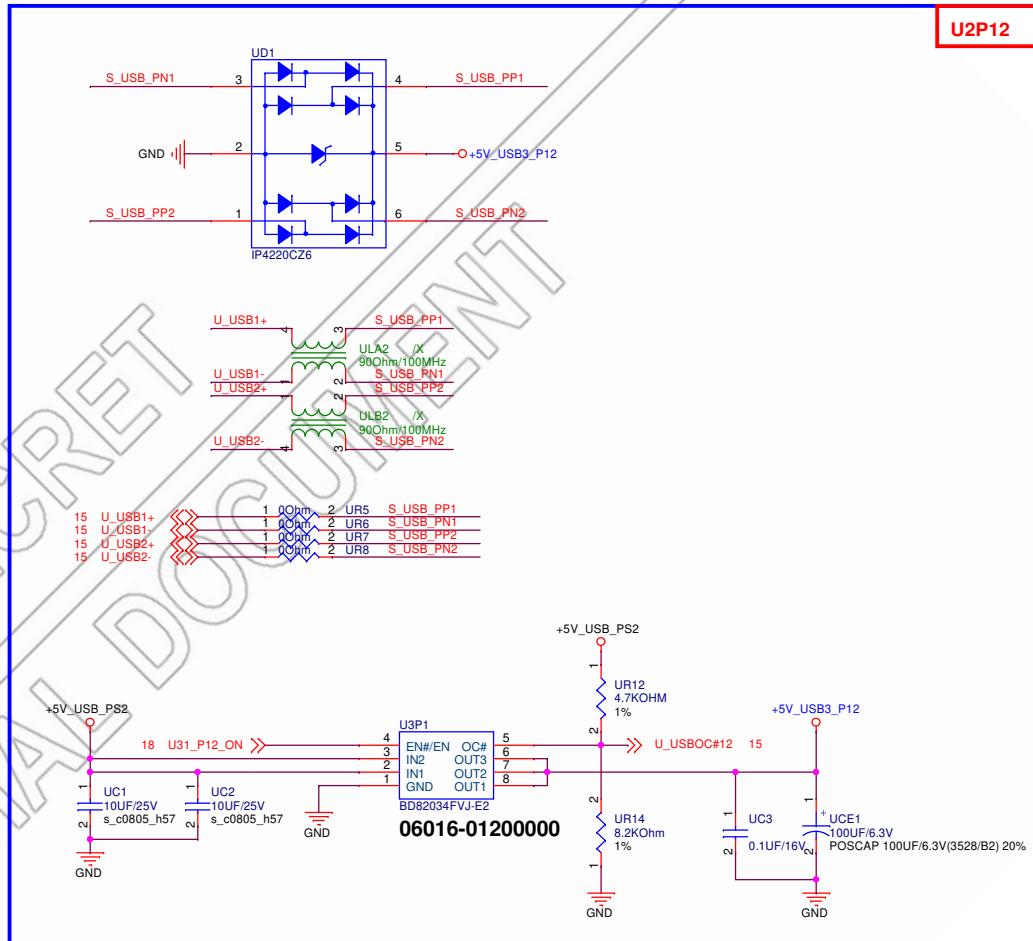
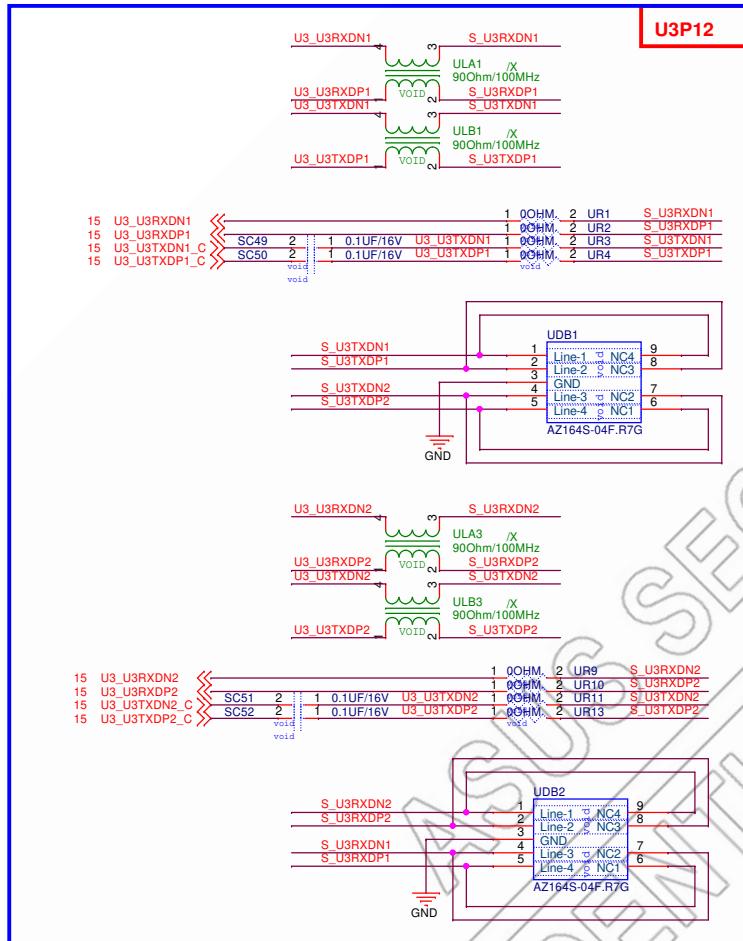
Near Connector (Void)



5 1 4 3 2 1

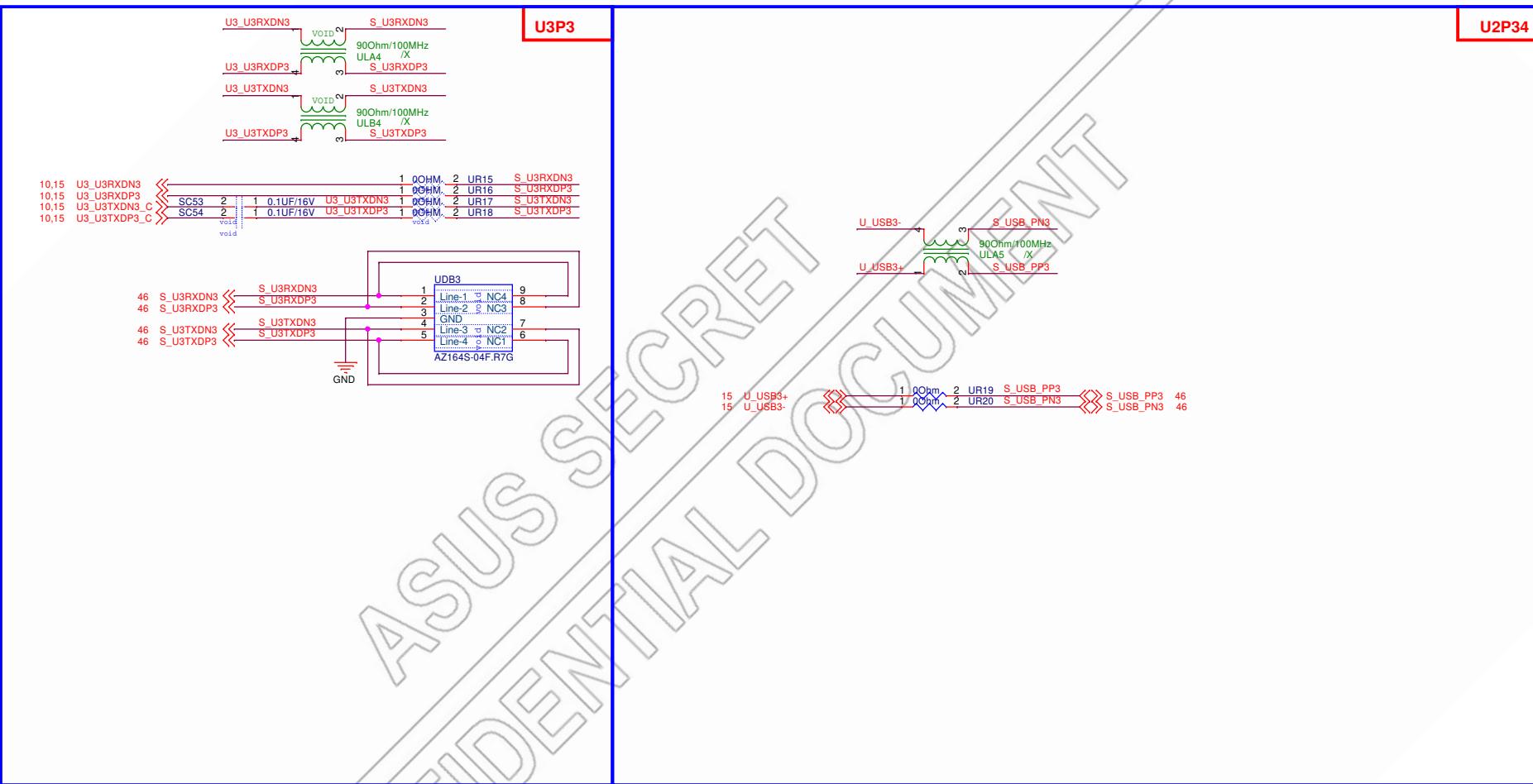
For SATA PWR

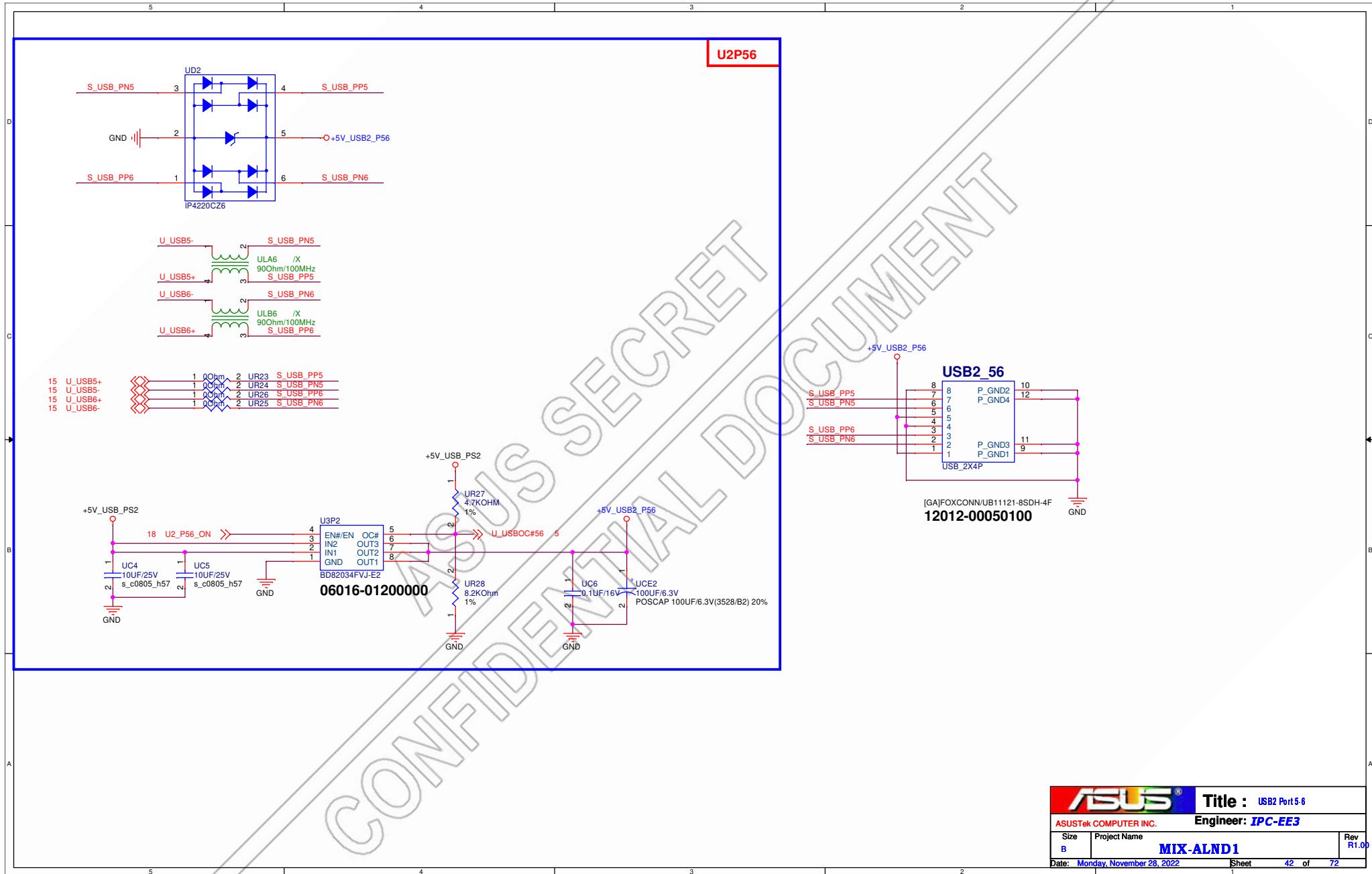


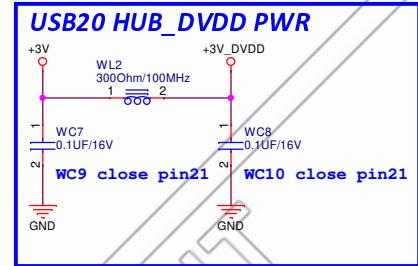
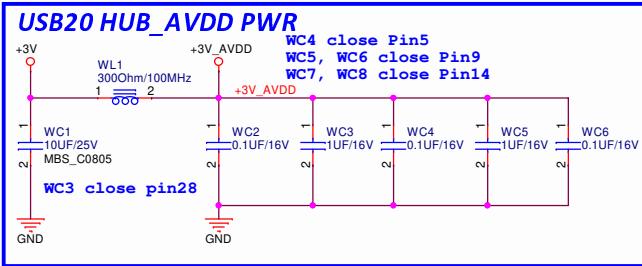
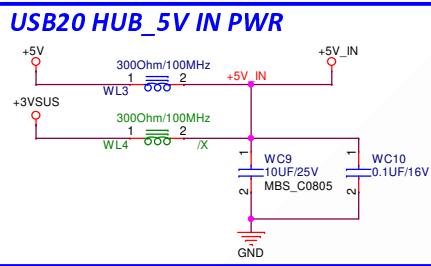


[GA]ESTES/AUSSB0100 R0113
12013-00120000

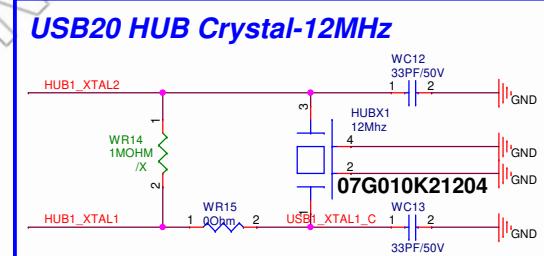
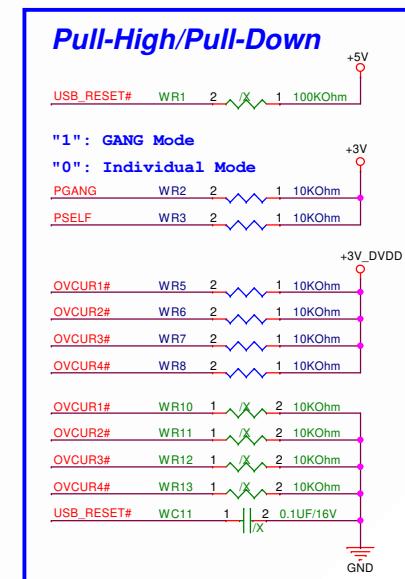
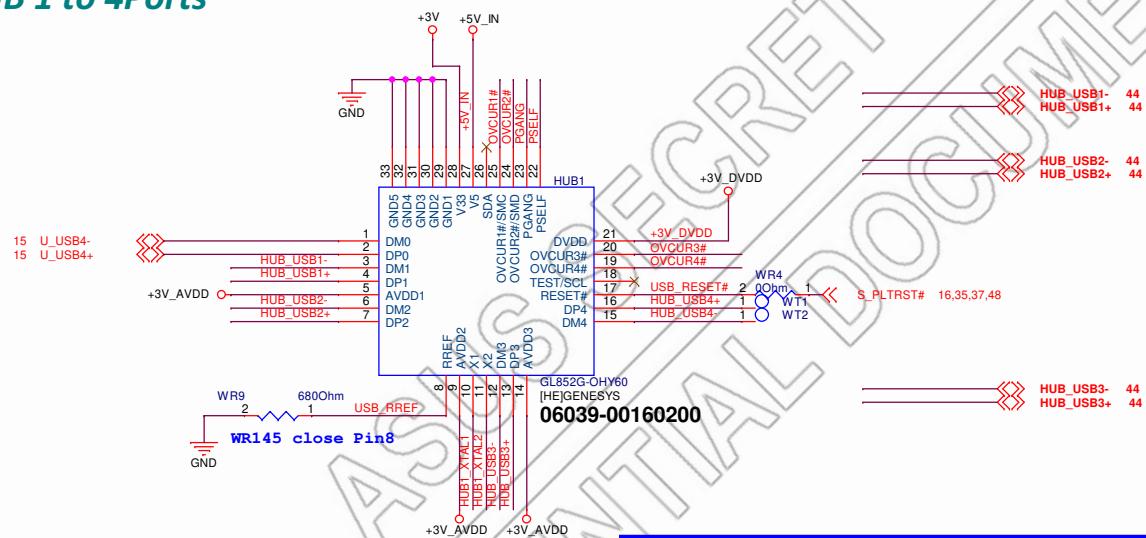
		Title : USB31 Port 1,2	
		Engineer: IPC-EE3	
ASUSTek COMPUTER INC.			
Size B	Project Name MIX-ALND1	Rev R1.00	
Date: Monday, November 28, 2022		Sheet 40	of 72

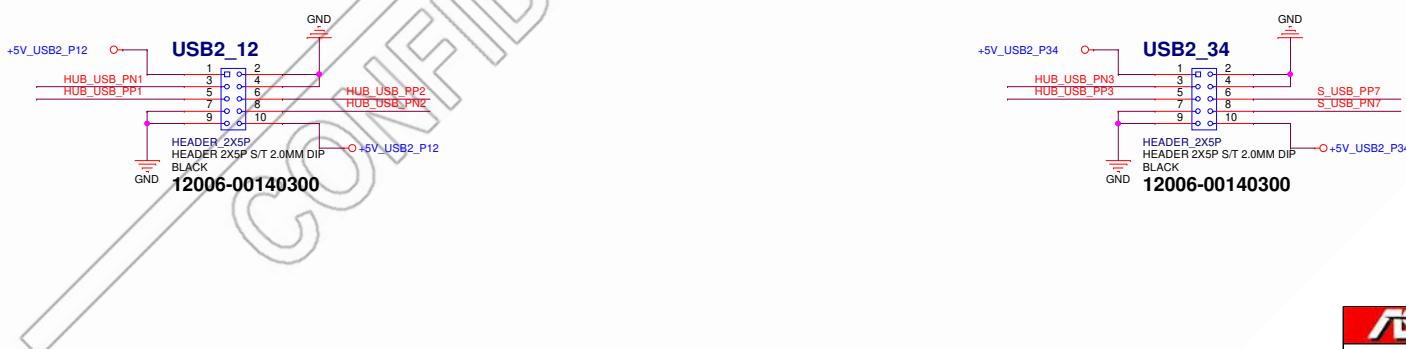
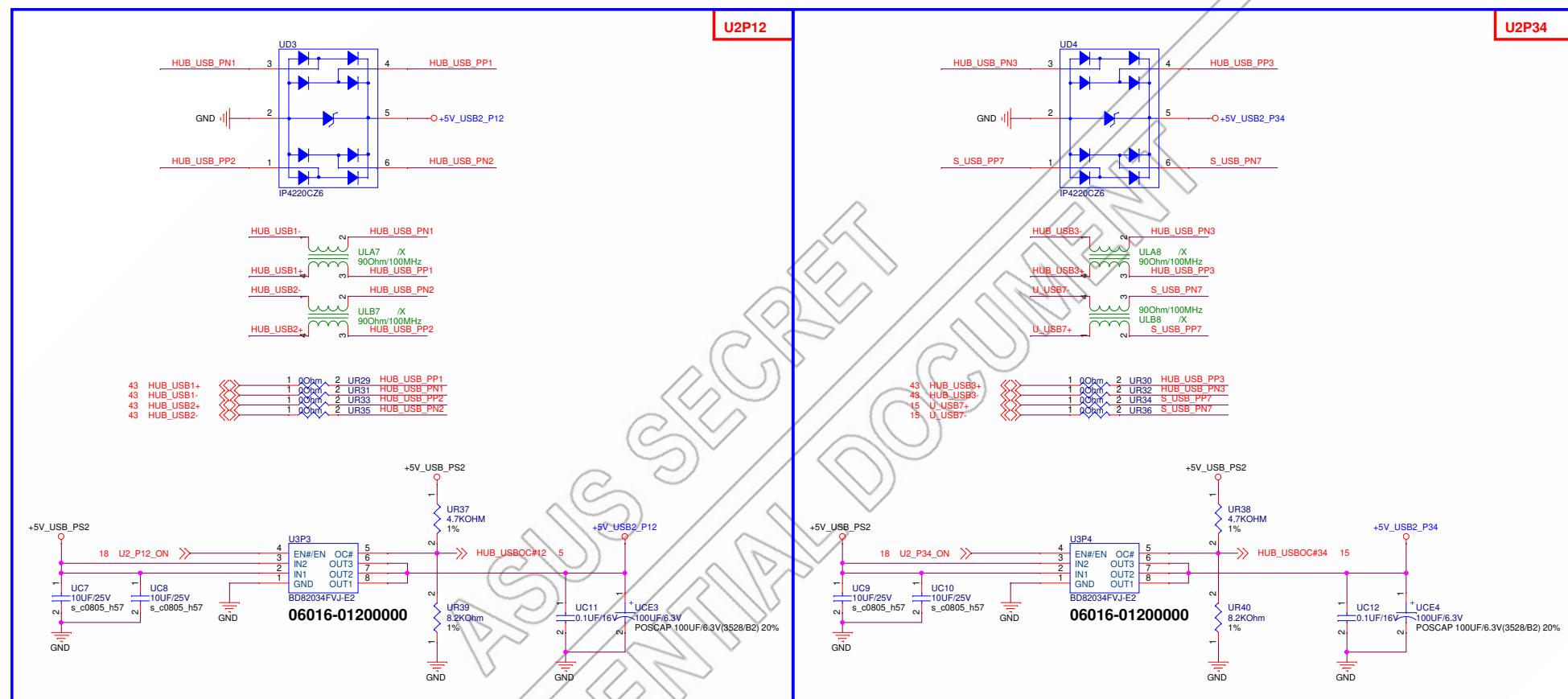


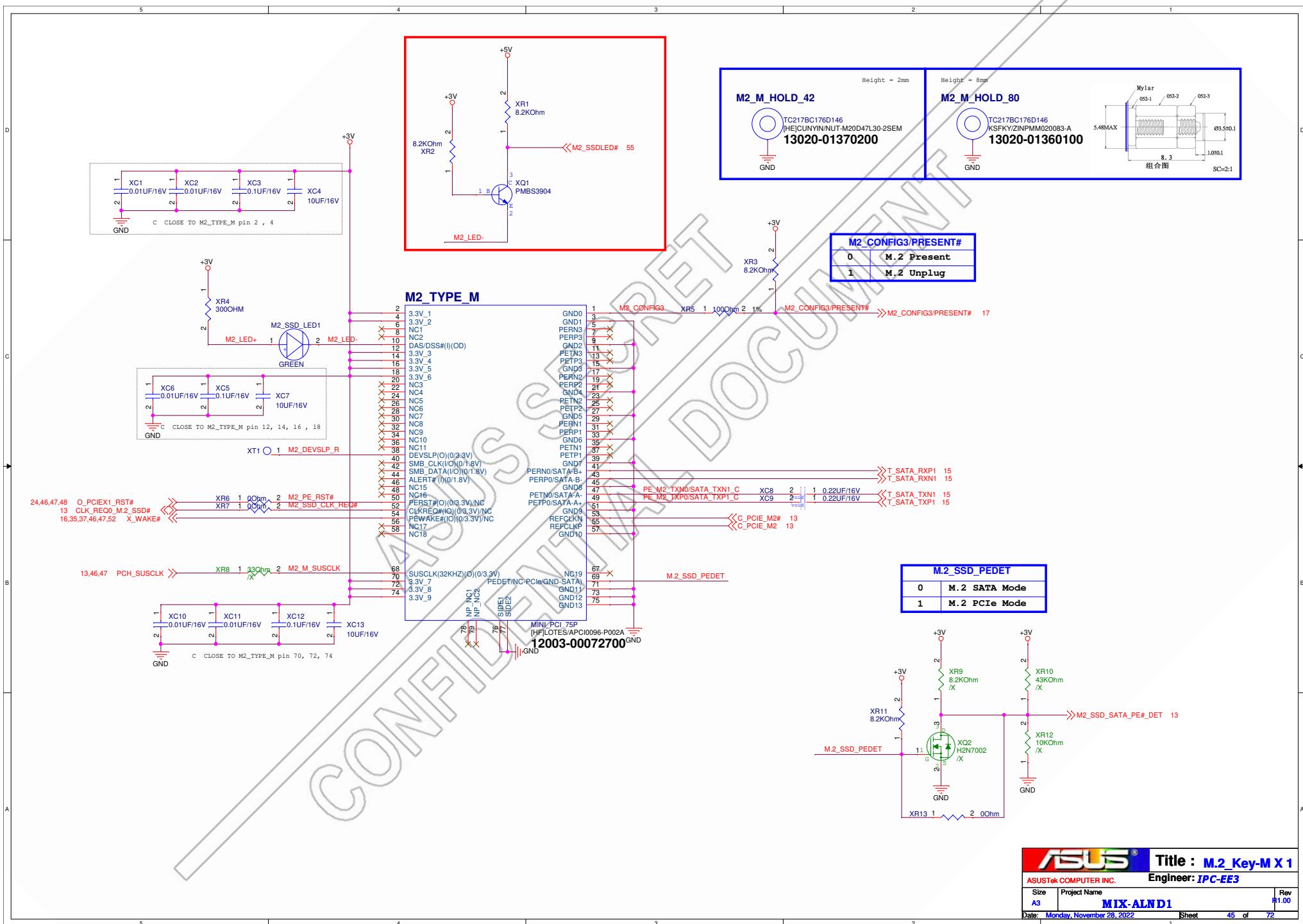


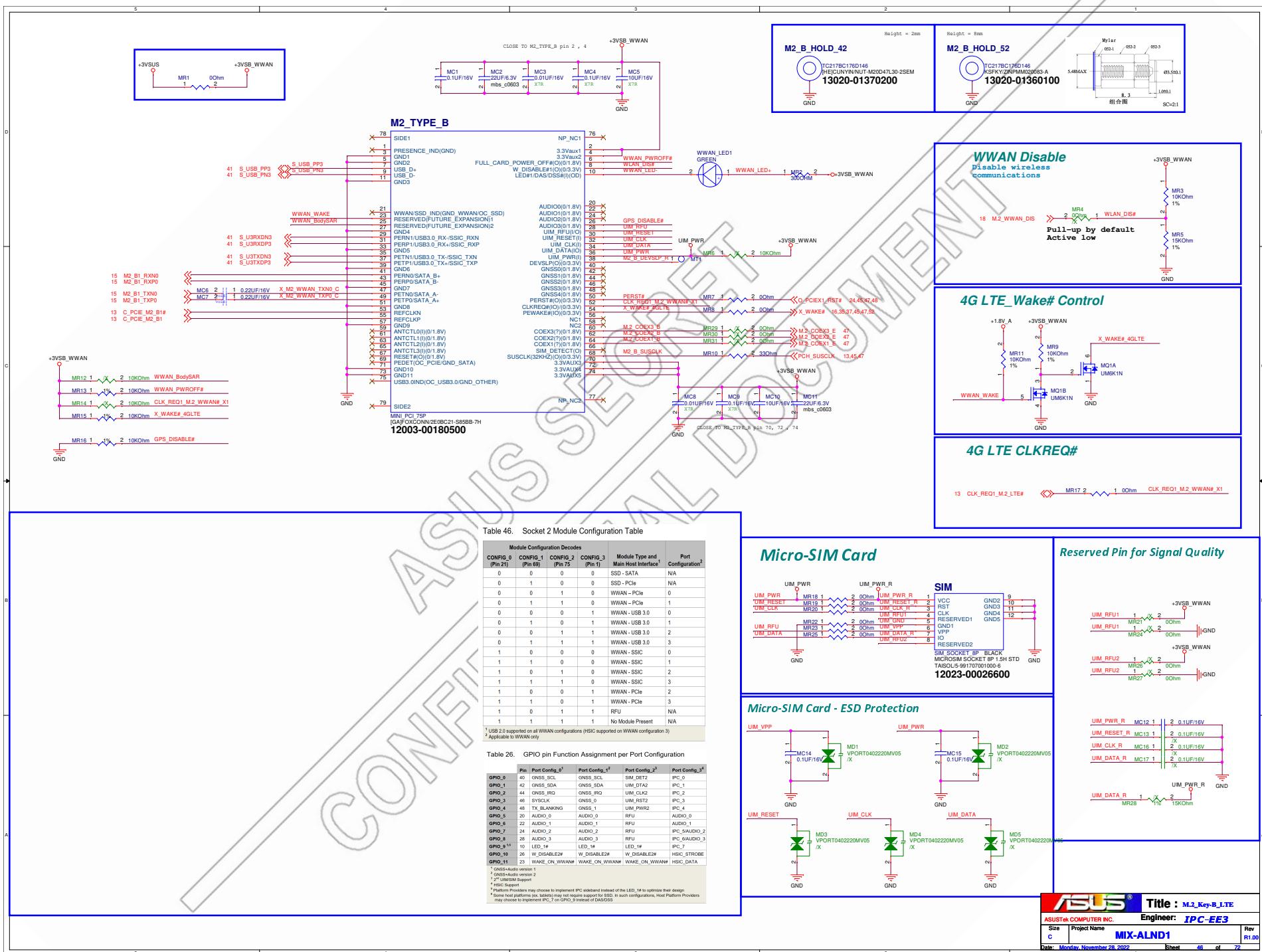


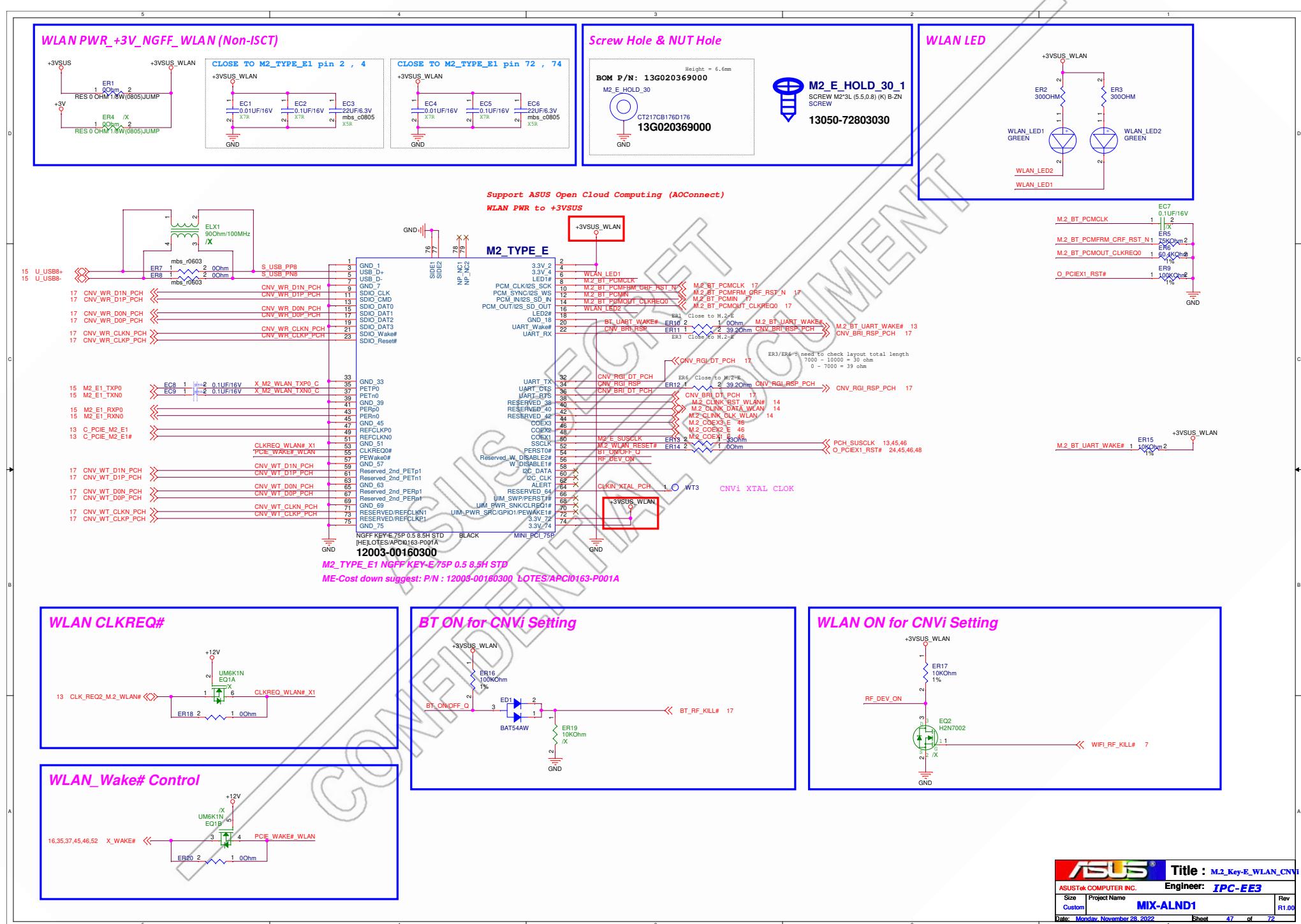
USB20 HUB 1 to 4Ports

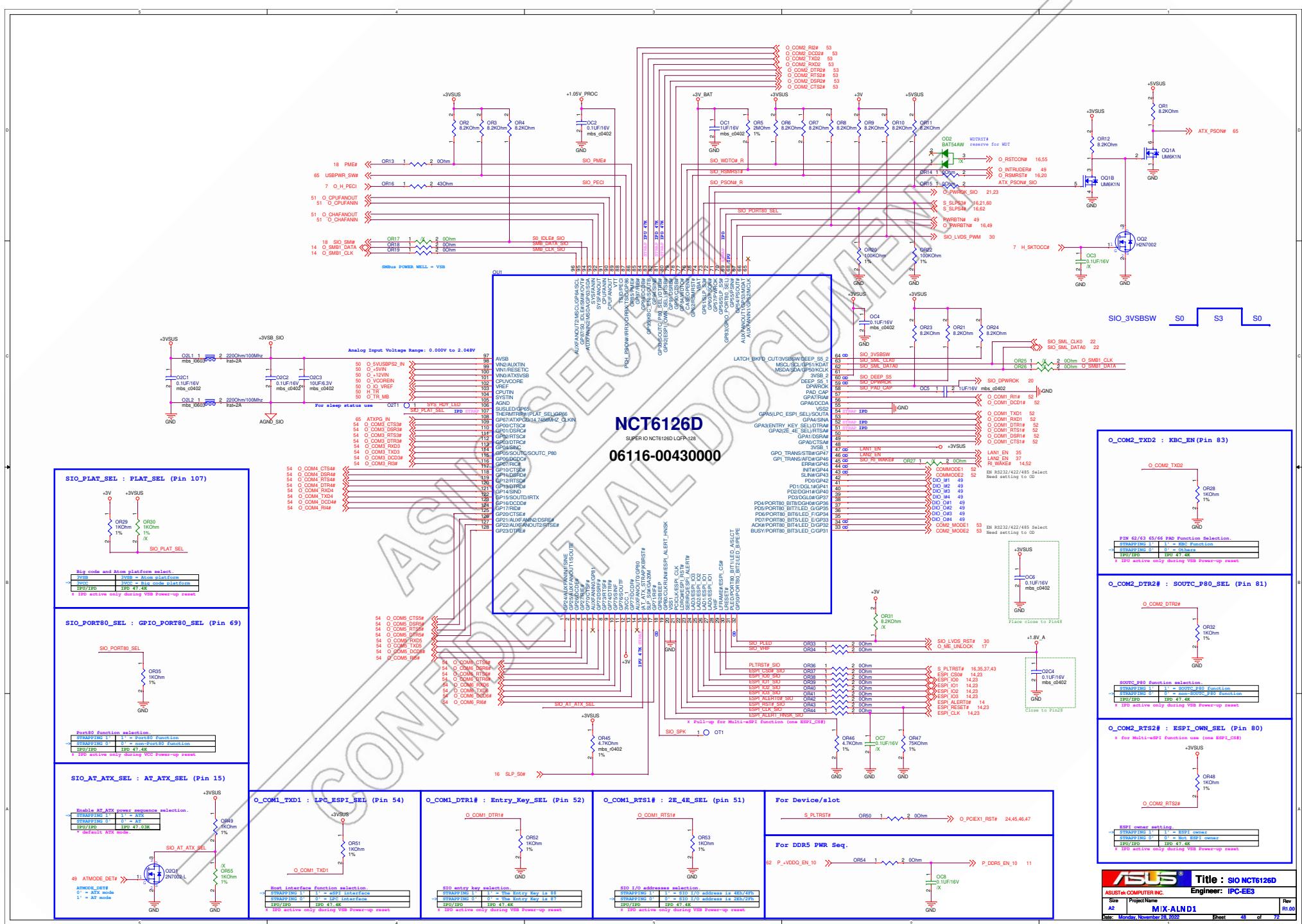






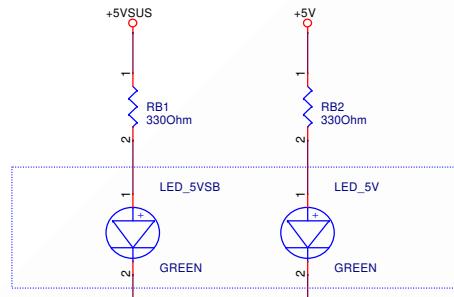






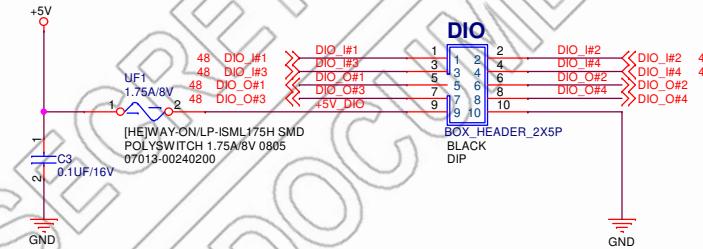
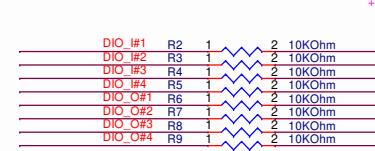
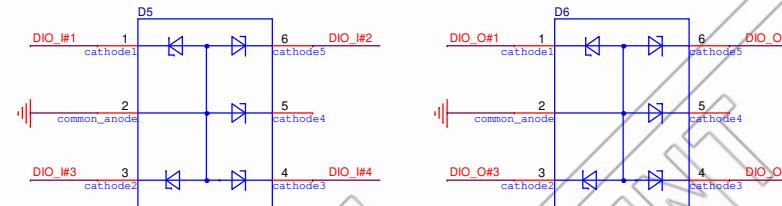
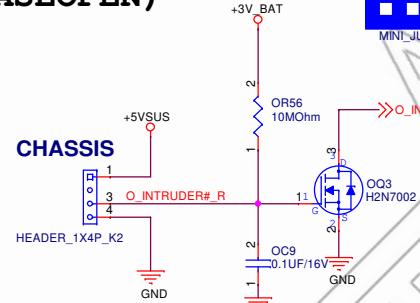
Digitital I/O from SIO

POWER_PWR



Intruder (CASEOPEN)

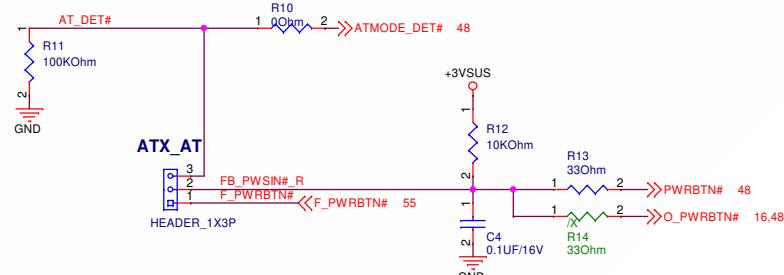
CHASSIS(3-4)



ATX_AT(1-2)



AT_ATX
1-2 : AT mode
2-3 : AT mode
ATMODE_DET#
AT mode=0
AT mode=1



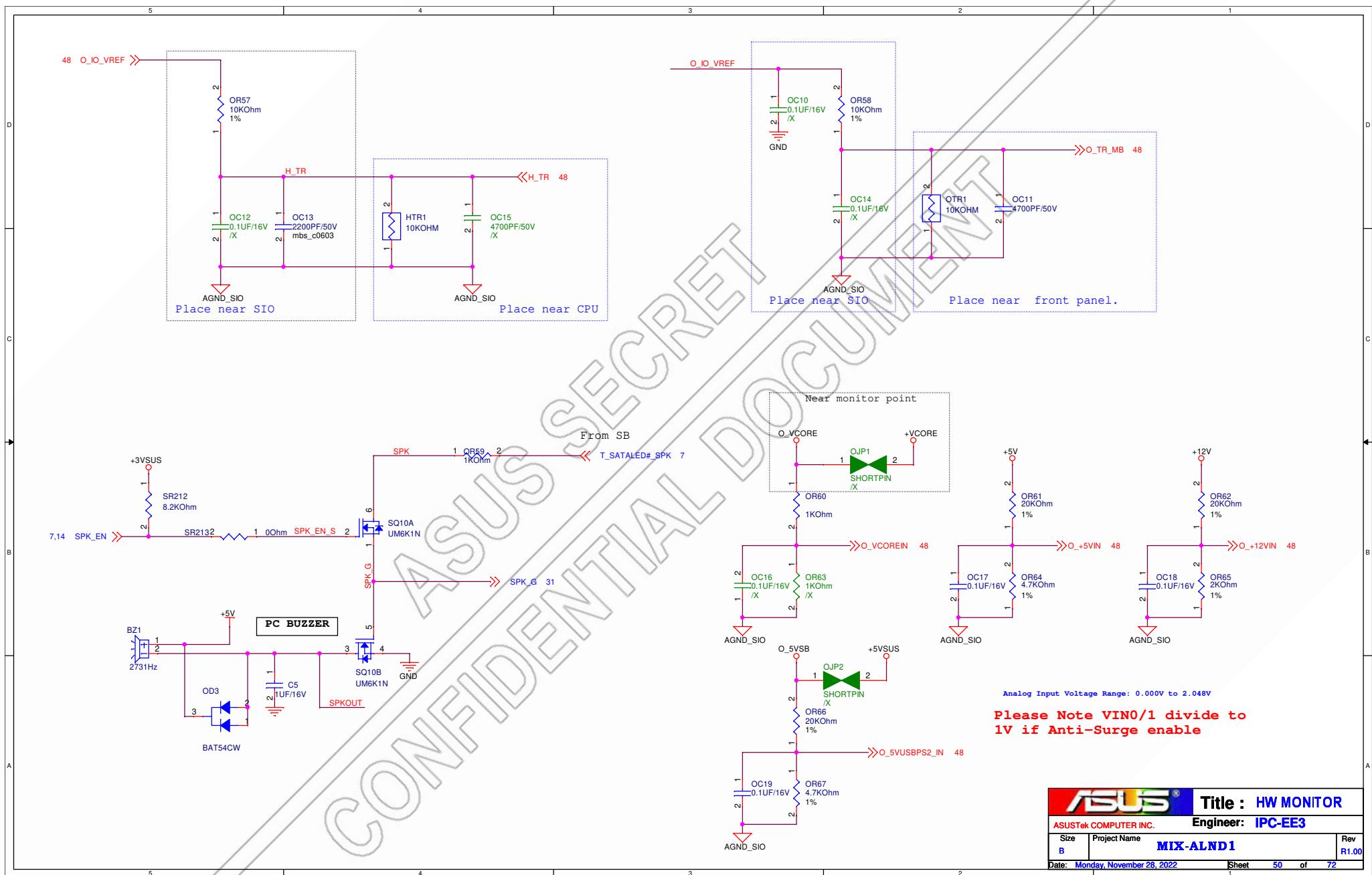
Title : Intruder/LED/DIO/AT&ATX

Engineer: IPC-EE3

Size	Project Name	MIX-ALND1	Rev
B			R1.00

Date: Monday, November 28, 2022

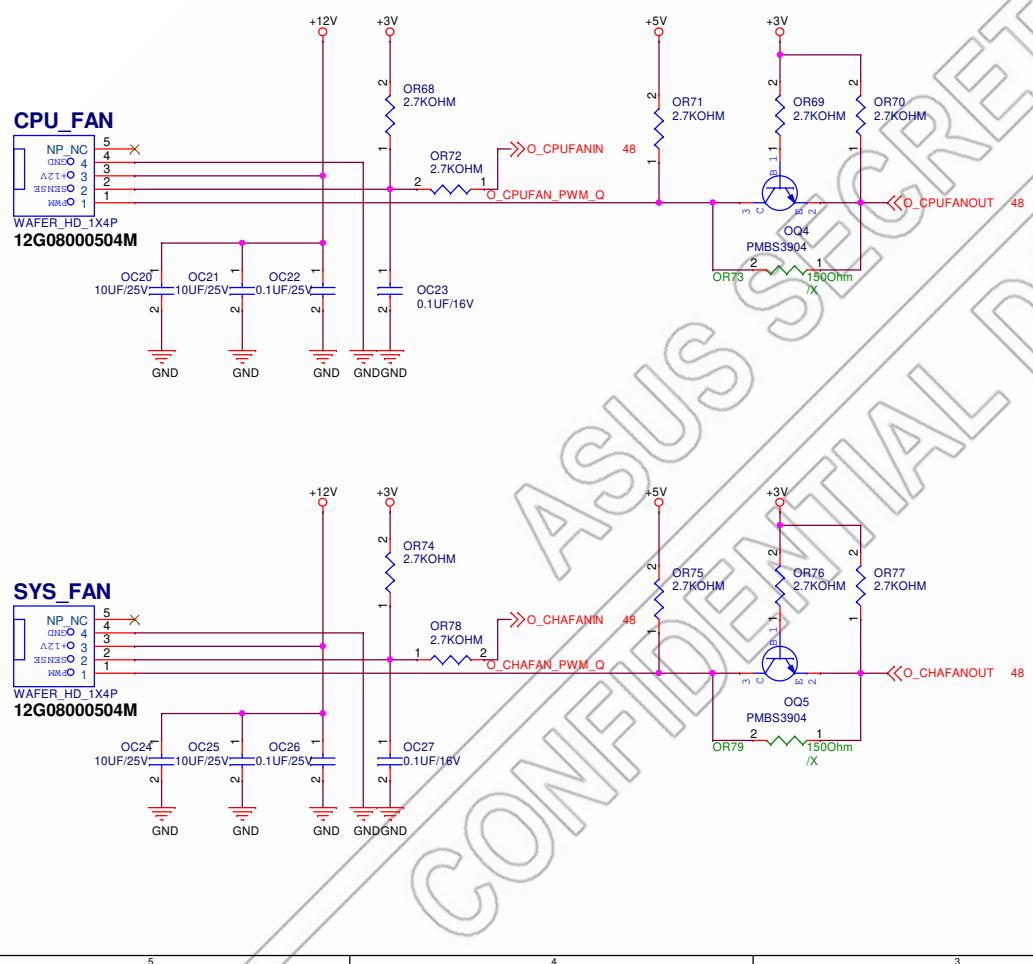
Sheet 49 of 72

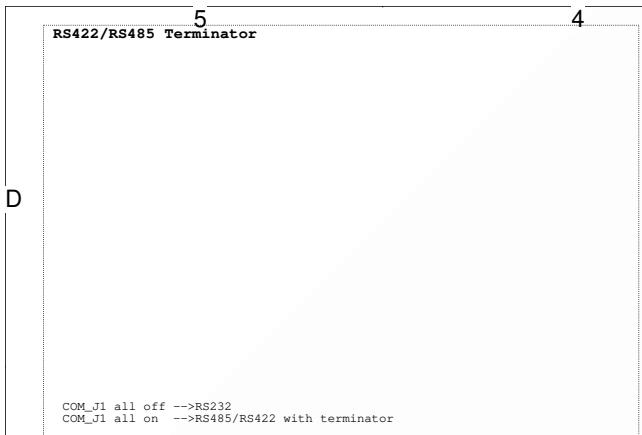


FAN CONTROL

PWM FAN CONTROL (New)

<i>Pin Number</i>	<i>Signal</i>
1	Control
2	Sense
3	+12V
4	GND

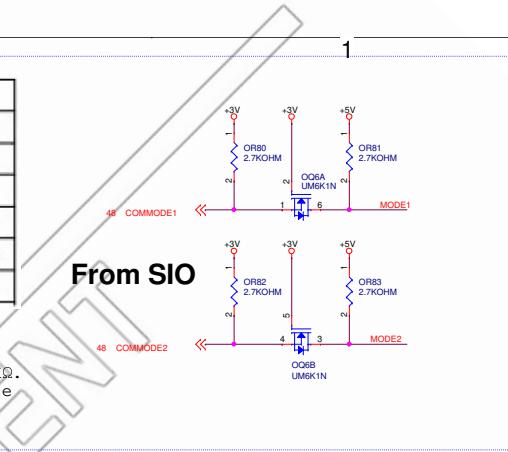




Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high = 625KΩ. As the current is very small (=15µA), please use the hardware strapping or GPIO (BIOS) to select the modes.



From SIC

F81438G

PARAMETER

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V _{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-	-	-	0.8	V	
Logic Input Pull-up Current	-	-	-	±15	µA	
Driver Input Pull High Current	I _{IT}	-	-	±15	µA	

COM1_V1(5-6) RI & Voltage SEL

1-2	12V
3-4	5V
5-6	RI (Default)

COM1_V1(5-6)
MINI JUMPER

COM1

DDDN	SINN
DSIN	DTRN
RSIN	DSRN
SOUT	CTSIN
RTSN	CTSIN
DDRN	SINN
DSRN	DTRN
RSRN	DSRN
RTRN	DSRN

BOX HEADER 2X8P [GA]PNRNX-S25-90-10GB00 12007-000201MI

Close to COM port connector

RS485 D+ (A) **RS485 D- (B)**

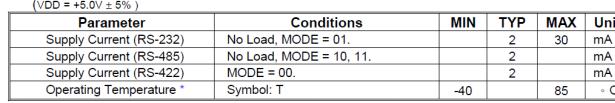
RS422 RX (B) **RS422 RX (A)**

RS422 TX (A) **RS422 TX (B)**

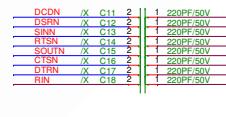
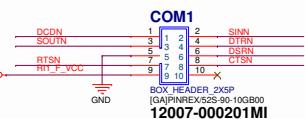
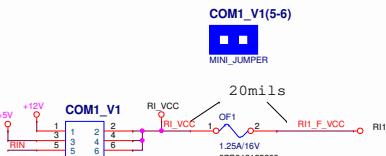
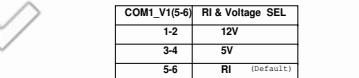
Maximum Slew rate control

SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

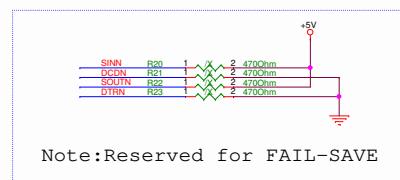
Note: Reserved for FAIL-SAVE



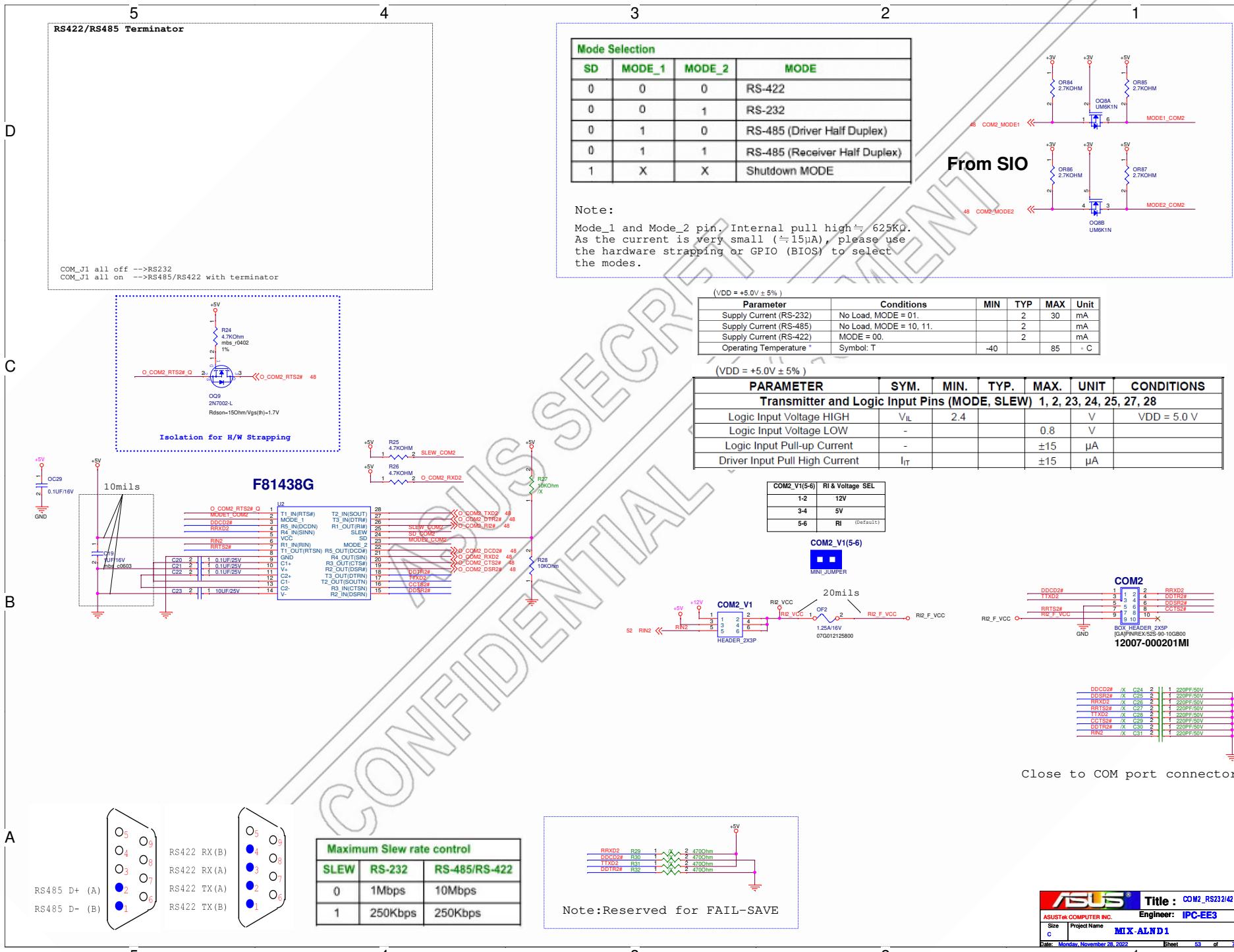
(VDD = +5.0V ± 5%)						
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V _{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	µA	
Driver Input Pull High Current	I _{HT}			±15	µA	



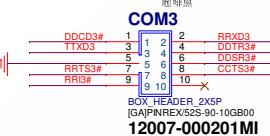
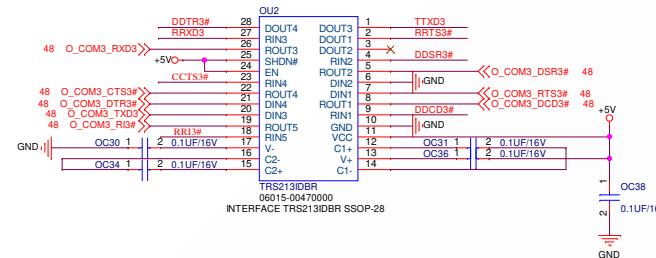
Close to COM port connector



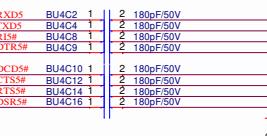
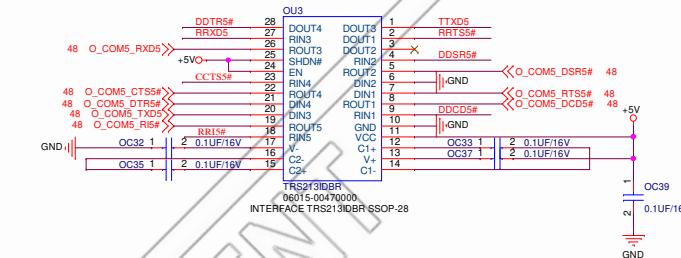
Note: Reserved for FAIL-SAVE



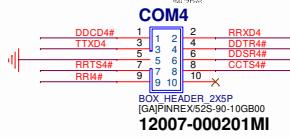
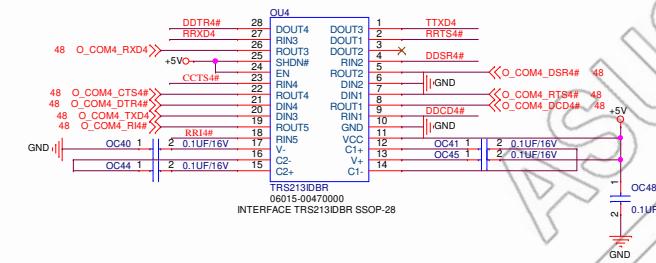
COM3



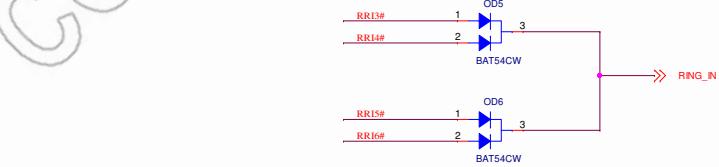
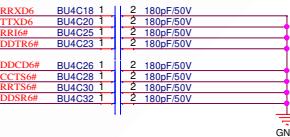
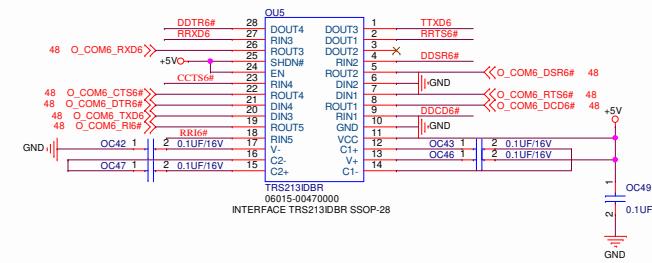
COM5

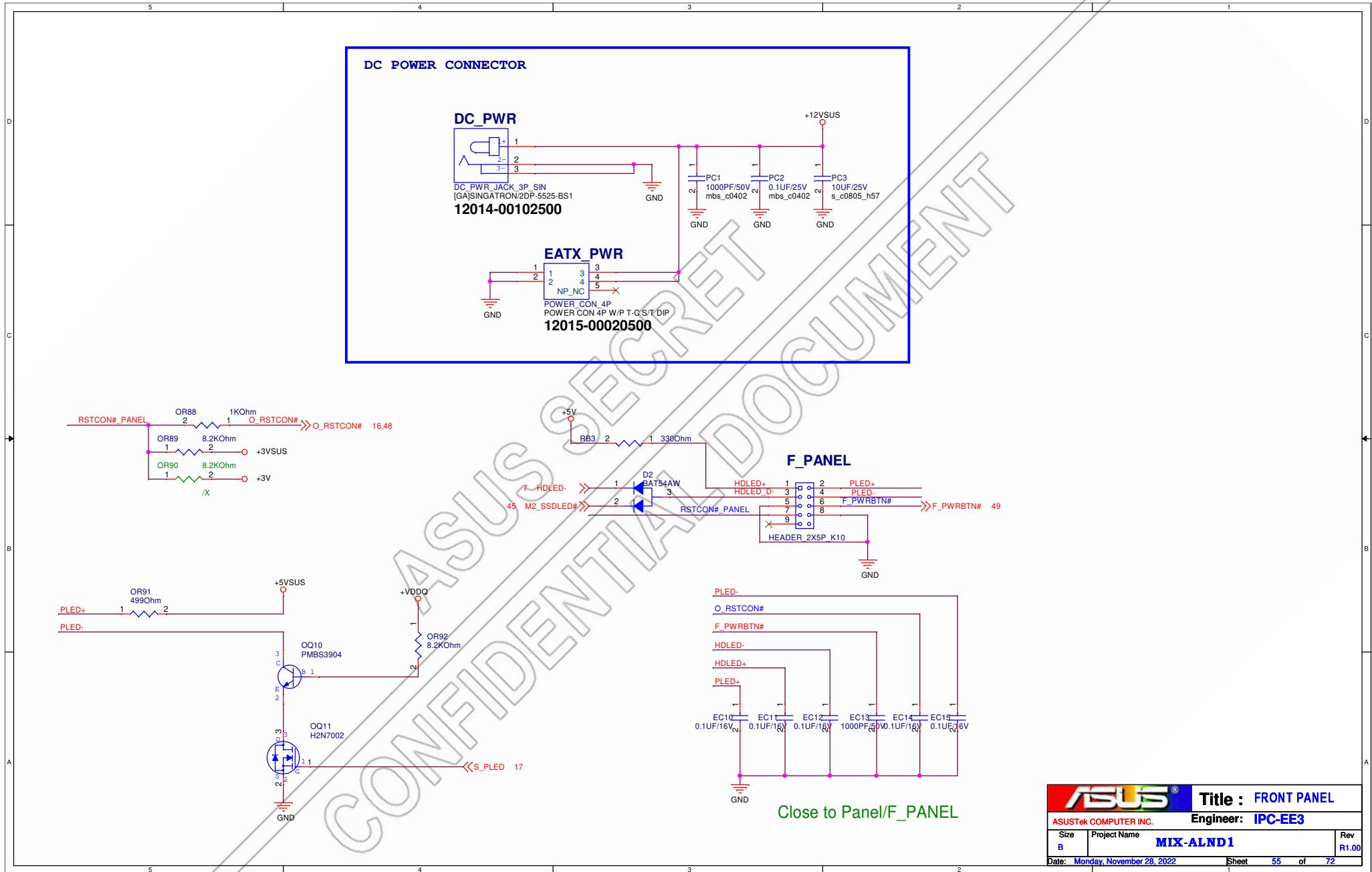


COM4

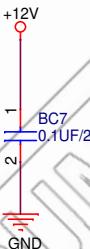
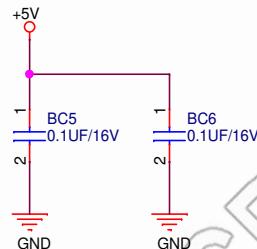
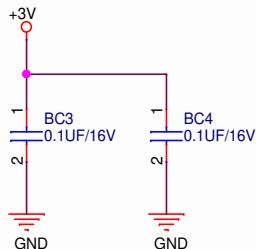
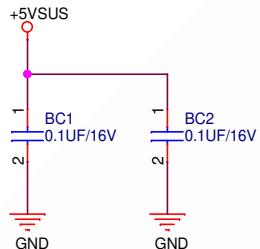


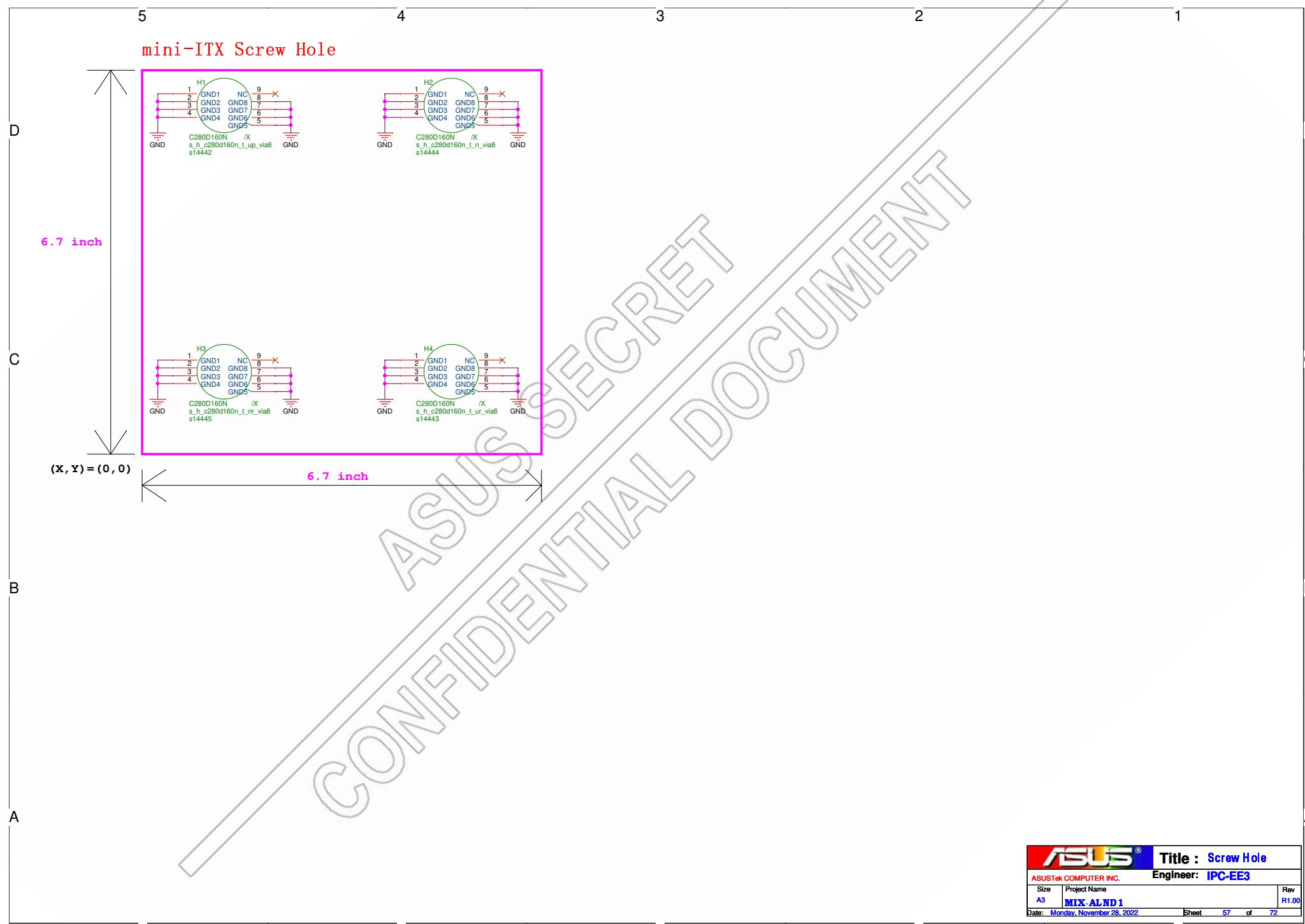
COM6





Bypass/EMI Capacitor





Selling Point

Logo

common Logo for all projects



FCC
FCC



WEEE_LOGO
WEEE_LOGO



CE
CE



PCB MADE IN CHINA
PCB MADE IN CHINA



UKCA
UKCA_LOGO



CHINA_ROHS_10YEAR
CHINA_ROHS_10YEAR

Fiducial Mask (光學點)

大顆十字光學點

光學點需要 6 ~ 10 顆,
LayoutRD 會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

2012/09/11

