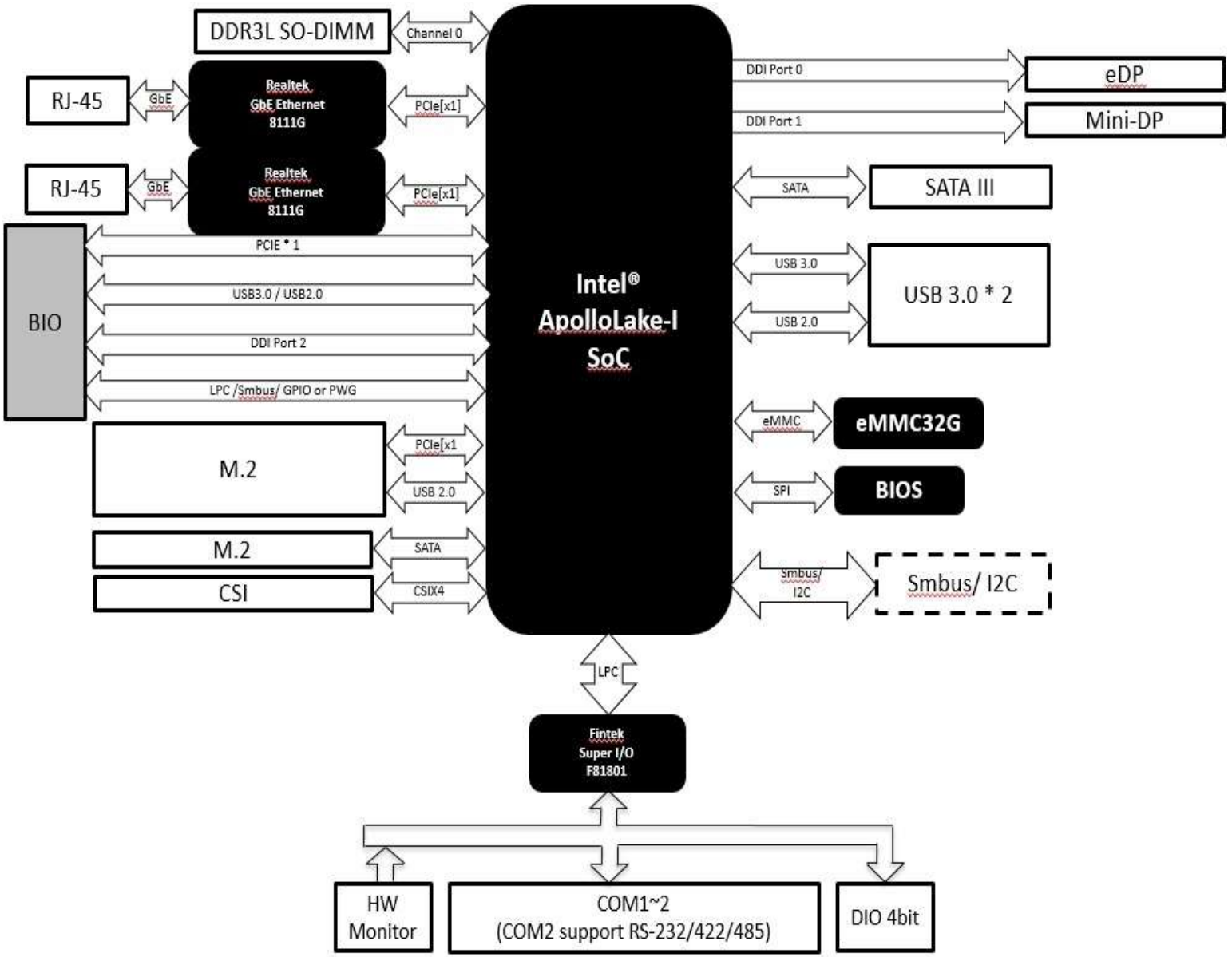
PICO-APL4 Rev.A0.1_0_0

Apollo Lake SoC Platform Cross Compatibility



Project Number : E16XXXX

Production Line : Sub.EPI.AA2M

AAEON an ASUS assoc. co.	Title: Cover Sheet		
	Size: C	Document Number: PICOAPL1A01	Rev: A0.1
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SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	BOARDID_BIT0
GPIO_1	1.8V	20K PD/I	BOARDID_BIT1
GPIO_2	1.8V	20K PD/I	
GPIO_3	1.8V	20K PD/I	
GPIO_4	1.8V	20K PD/I	LVDS_RBIT0
GPIO_5	1.8V	20K PD/I	LVDS_RBIT1
GPIO_6	1.8V	20K PD/I	LVDS_RBIT2
GPIO_7	1.8V	20K PD/I	LVDS_RBIT3
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	WAKE_RI#
GPIO_15	1.8V	20K PD/I	EN_USB
GPIO_16	1.8V	20K PD/I	LAN1_DISABLE#
GPIO_17	1.8V	20K PD/I	W_DISABLE0#
GPIO_18	1.8V	20K PD/I	W_DISABLE1#
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GP[0]
GPIO_23	1.8V	20K PD/I	SATA_GP[1]
GPIO_24	1.8V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	1.8V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/IO	
GPIO_217	1.8V	20K PD/IO	
GPIO_218	1.8V	20K PD/IO	
GPIO_219	1.8V	20K PD/IO/OP	

The Mapping Table For Super I/O F81801U GPIOs :

Name	PIN No.	Power	Type	Description & setting
GPIO[6]	42	+3.3V_ALW	I/OOD12t	
GPIO[12]	35	+3.3V	I/OOD12t	WDTRST#
GPIO[15]	36	+3.3V	I/OOD12,st,lv	None
GPIO[16]	37	+3.3V	I/OOD12,st,lv	
GPIO[20]	38	+3.3V	I/OOD12,st,lv	
GPIO[21]	39	+3.3V	I/OOD12t	
GPIO[22]	40	+3.3V	I/OOD12t	
GPIO[23]	41	+3.3V	I/OOD12t	
GPIO[30]	9	+3.3V	I/OOD12t	DCDB#
GPIO[31]	10	+3.3V	I/OOD12t	RIB#
GPIO[32]	11	+3.3V	I/OOD12t	CTSB#
GPIO[33]	13	+3.3V	I/OOD12t	DTRB#
GPIO[34]	14	+3.3V	I/OOD12t	RTSB#
GPIO[35]	15	+3.3V	I/OOD12t	DSRB#
GPIO[36]	16	+3.3V	I/OOD12t	TXB#
GPIO[37]	17	+3.3V	I/OOD12t	RXB#

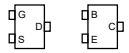
I/OOD12st,lv : Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.

I/OOD12t : TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability

F75111RG GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO10	5V	VSB3V	Native	BOARDID_BIT0
GPIO11	5V	VSB3V	Native	ADM213_EN
GPIO12	5V	VSB3V	Native	81438_SD
GPIO13	5V	VSB3V	Native	
GPIO14	5V	VSB3V	Native	BOARDID_BIT1
GPIO15	5V	VSB3V	Native	
GPIO16	5V	VSB3V	Native	
GPIO17	5V	VSB3V	Native	
GPIO20	5V	VSB3V	Native	SEL_COM2_MD0
GPIO21	5V	VSB3V	Native	SEL_COM2_MD1
GPIO22	5V	VSB3V	Native	COM2_SLEW
GPIO23	5V	VSB3V	Native	BIO-GPIO
GPIO24	5V	VSB3V	Native	DIO_P0
GPIO25	5V	VSB3V	Native	DIO_P1
GPIO26	5V	VSB3V	Native	DIO_P2
GPIO27	5V	VSB3V	Native	DIO_P3
GPIO30	5V	VSB3V	GPIO	LVDS_EN
GPIO31	5V	VSB3V	GPIO	
GPIO32	5V	VSB3V	GPIO	
GPIO33	5V	VSB3V	GPIO	LVDS_PD#

PCB Footprints

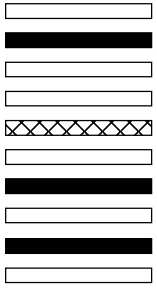


SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
GPIO IC	6Eh
PTN3460 Slave	C0h

PCB STACK :

Impedence 50ohm +/-15%.



- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : GND
- Layer 5 : Signal
- Layer 6 : VCC
- Layer 7 : Signal
- Layer 4 : Signal
- Layer 9 : GND
- Layer 10 : Solder

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Title: **System Settings**

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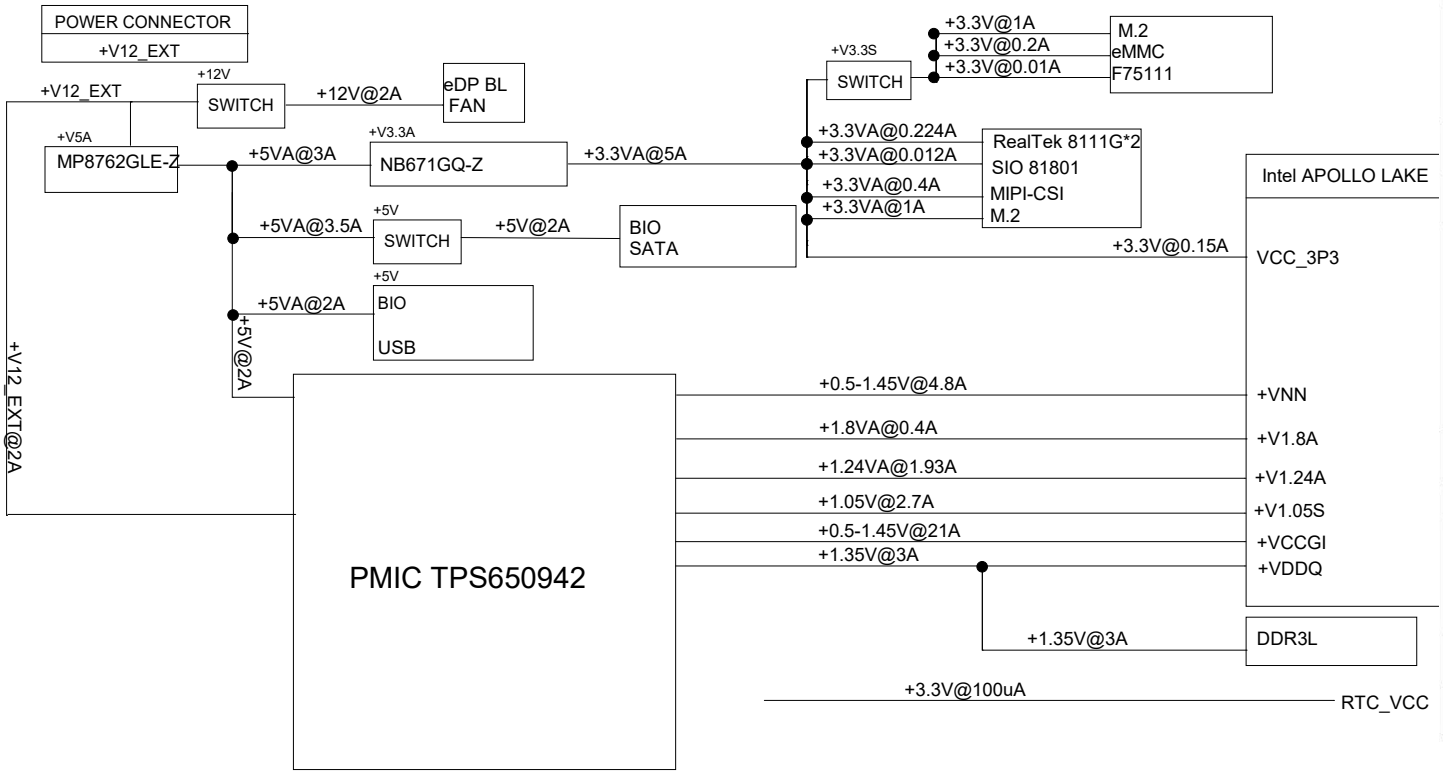

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Iccmax (A)
VCC_VCGI	0.45~1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	21
VNN	0.45~1.3	+/-50mV	4.8
VCC_V1P05	1.05	+/-5%	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	1.3
VCC_V1P24_A	1.24	+/-5%	TBD
VCC_V1P8V_A	1.8	+/-5%	0.4
VDDQ	1.35	+/-5%	2.8 (excluding DRAM)
	1.24	+/-5%	
VCC_3P3V_A	3.3	+/-5%	0.15
VCC_RTC_3P3V	2~3.47	N/A	TBD

+V5A -> +V3.3A -> +VNN -> +VCC -> +V1P8A- > +V1P24A -> +V1P8U -> +VDDQ
+V1.05S -> +VCC_VCGI

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Title: Power Tree

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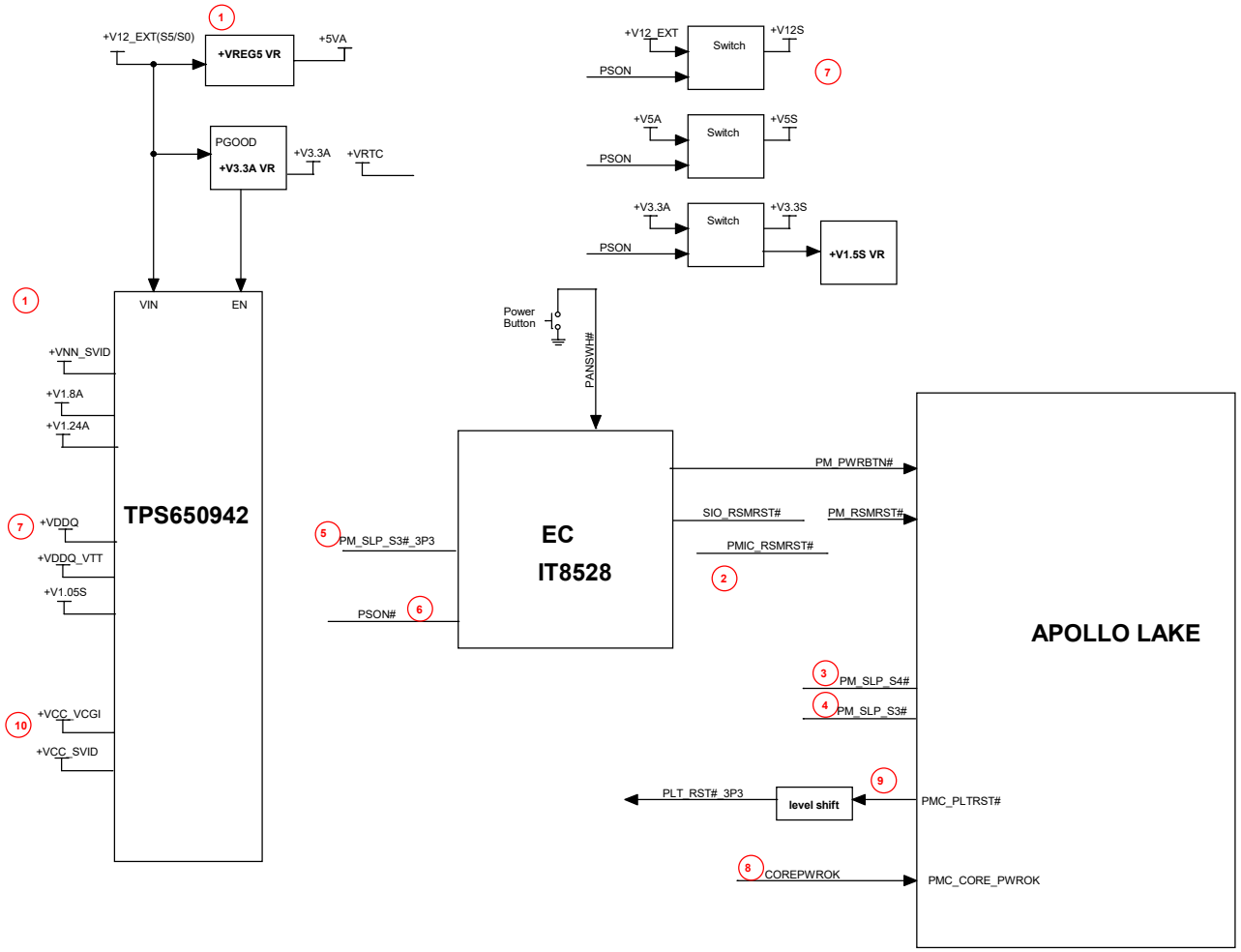
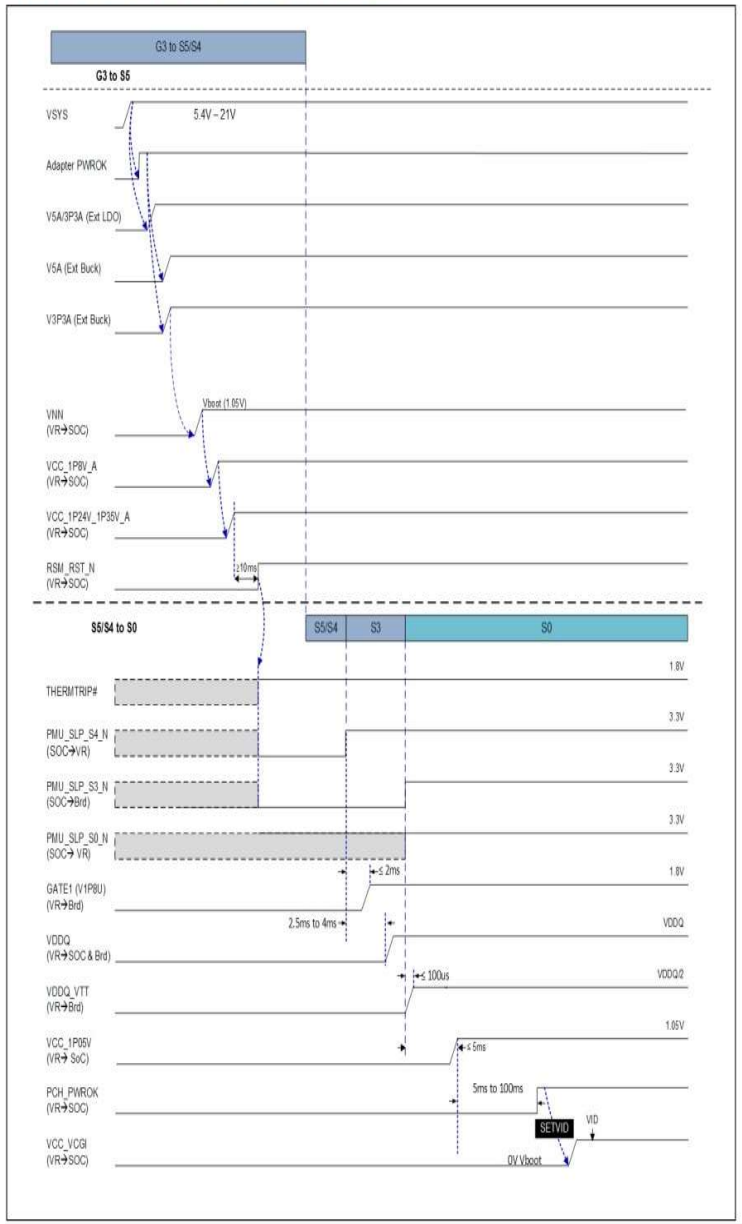


Power-Up Sequencing (G3 to S0)—Adapter



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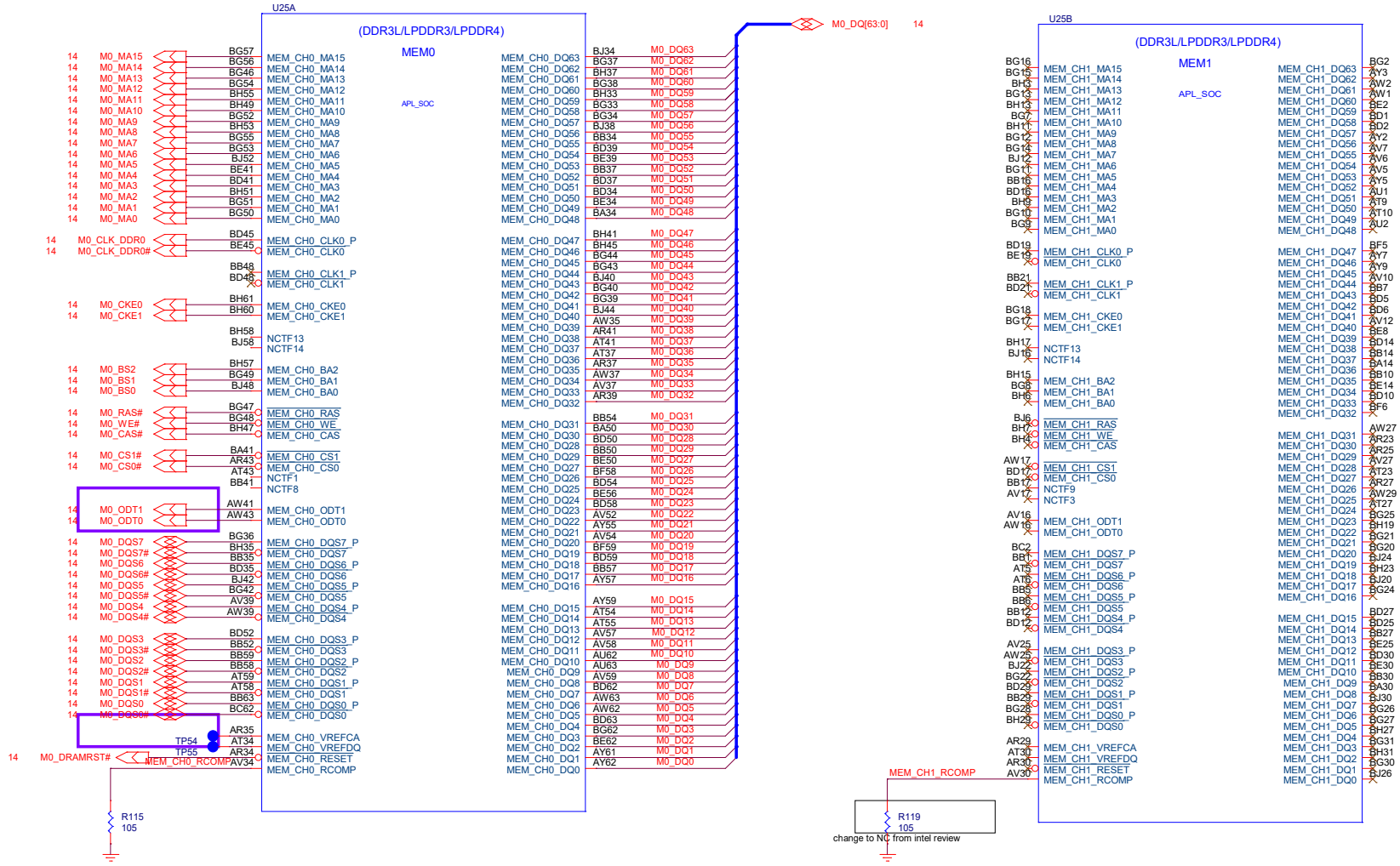

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Size: Custom	Document Number: PICOAPL1A01		Rev: A0.1
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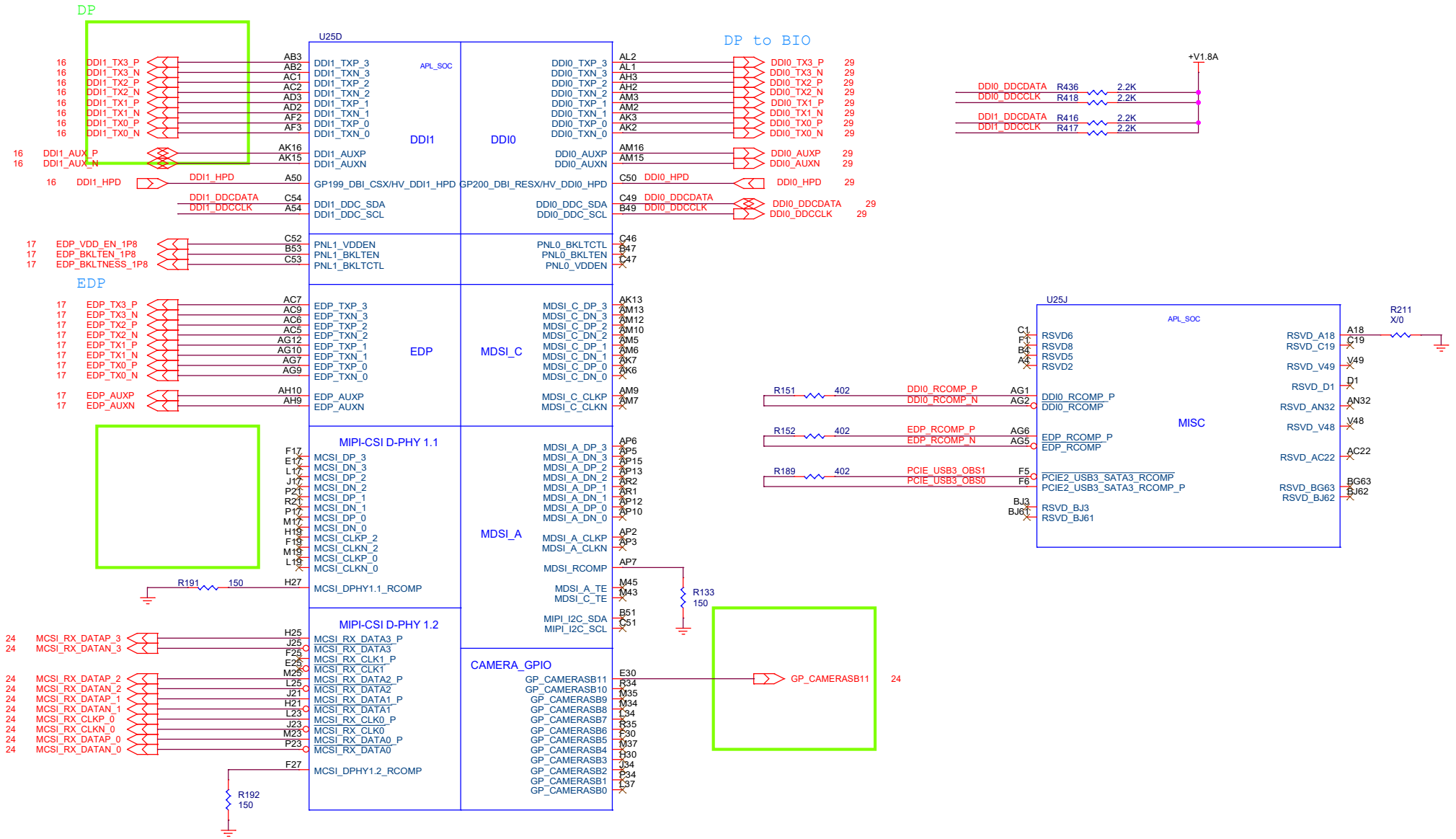

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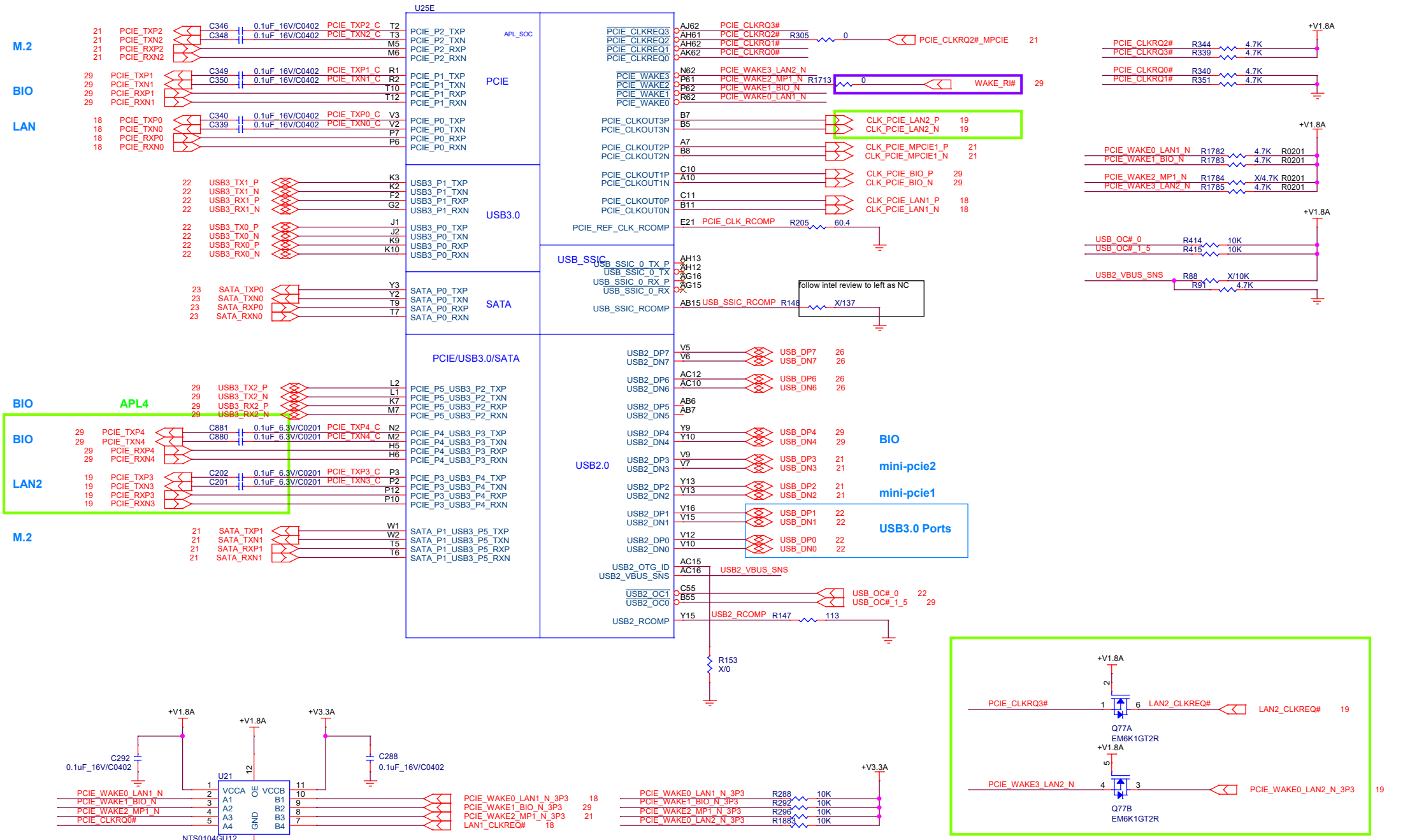

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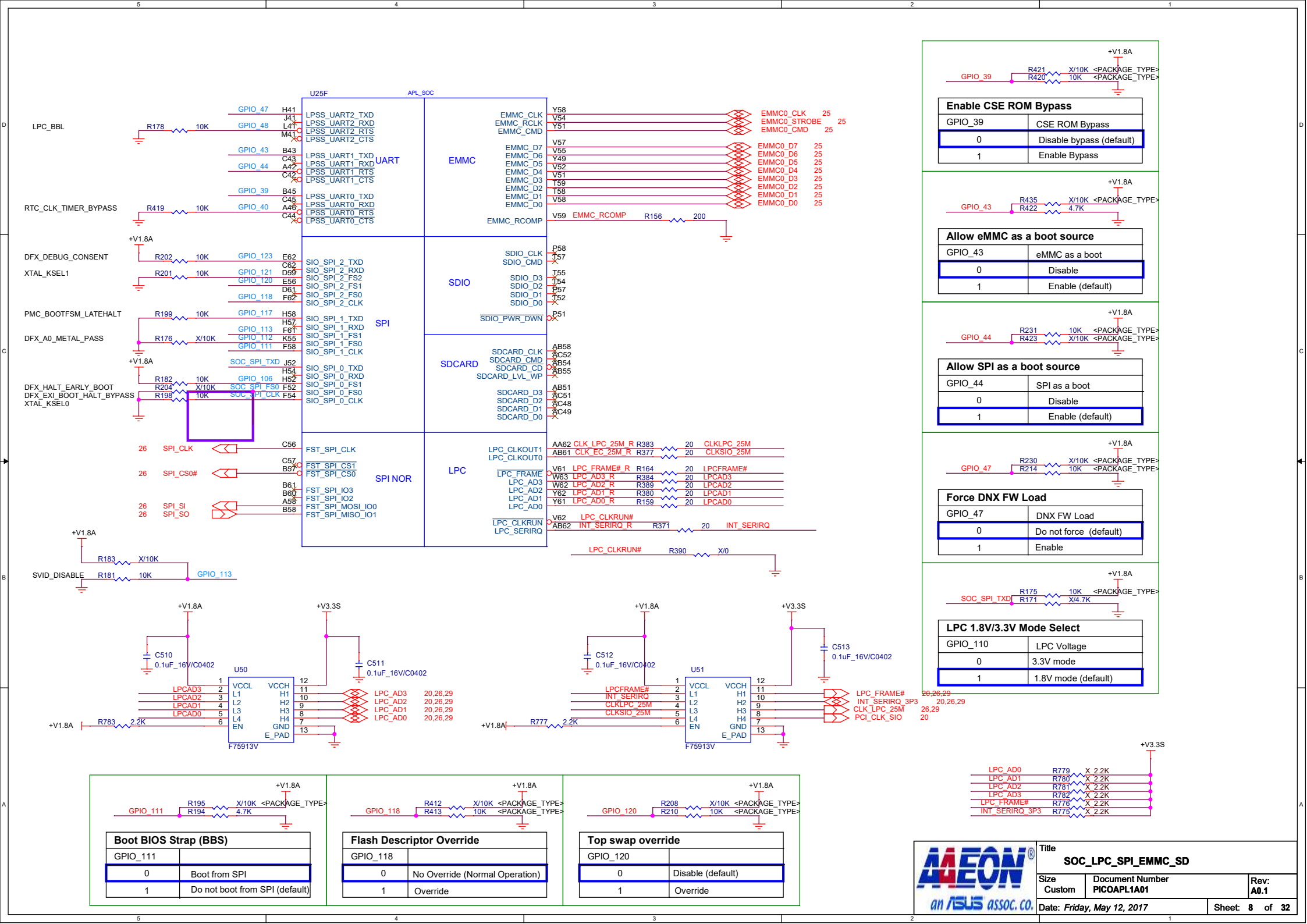
U25F
APL_SOC
UART
SPI
SPI NOR
EMMC
SDIO
SDCARD
LPC
LPC_BBL
RTC_CLK_TIMER_BYPASS
DFX_DEBUG_CONSENT
XTAL_KSEL1
PMC_BOOTFSM_LATEHALT
DFX_A0_METAL_PASS
DFX_HALT_EARLY_BOOT
DFX_EXI_BOOT_HALT_BYPASS
XTAL_KSEL0
SVID_DISABLE
GPIO_47
GPIO_48
GPIO_43
GPIO_44
GPIO_39
GPIO_40
GPIO_123
GPIO_121
GPIO_120
GPIO_118
GPIO_117
GPIO_113
GPIO_112
GPIO_111
GPIO_106
SOC_SPI_TXD
SOC_SPI_FS0
SOC_SPI_CLK
SPI_CLK
SPI_CS0#
SPI_SI
SPI_SO
LPSS_UART2_TXD
LPSS_UART2_RXD
LPSS_UART2_RTS
LPSS_UART2_CTS
LPSS_UART1_TXD
LPSS_UART1_RXD
LPSS_UART1_RTS
LPSS_UART1_CTS
LPSS_UART0_TXD
LPSS_UART0_RXD
LPSS_UART0_RTS
LPSS_UART0_CTS
SIO_SPI_2_TXD
SIO_SPI_2_RXD
SIO_SPI_2_FS2
SIO_SPI_2_FS1
SIO_SPI_2_FS0
SIO_SPI_2_CLK
SIO_SPI_1_TXD
SIO_SPI_1_RXD
SIO_SPI_1_FS1
SIO_SPI_1_FS0
SIO_SPI_1_CLK
SIO_SPI_0_TXD
SIO_SPI_0_RXD
SIO_SPI_0_FS1
SIO_SPI_0_FS0
SIO_SPI_0_CLK
FST_SPI_CLK
FST_SPI_CS1
FST_SPI_CS0
FST_SPI_IO3
FST_SPI_IO2
FST_SPI_MOSI_IO0
FST_SPI_MISO_IO1
EMMC_CLK
EMMC_RCLK
EMMC_CMD
EMMC_D7
EMMC_D6
EMMC_D5
EMMC_D4
EMMC_D3
EMMC_D2
EMMC_D1
EMMC_D0
EMMC_RCOMP
EMMC0_CLK
EMMC0_STROBE
EMMC0_CMD
EMMC0_D7
EMMC0_D6
EMMC0_D5
EMMC0_D4
EMMC0_D3
EMMC0_D2
EMMC0_D1
EMMC0_D0
SDIO_CLK
SDIO_CMD
SDIO_D3
SDIO_D2
SDIO_D1
SDIO_D0
SDIO_PWR_DWN
SDCARD_CLK
SDCARD_CMD
SDCARD_CD
SDCARD_LVL_WP
SDCARD_D3
SDCARD_D2
SDCARD_D1
SDCARD_D0
LPC_CLKOUT1
LPC_CLKOUT0
LPC_FRAME
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
LPC_CLKRUN
LPC_SERIRQ
CLK_LPC_25M_R
CLK_EC_25M_R
LPC_FRAME#_R
LPC_AD3_R
LPC_AD2_R
LPC_AD1_R
LPC_AD0_R
LPC_CLKRUN#
INT_SERIRQ_R
INT_SERIRQ
CLKLPC_25M
CLKSIO_25M
LPCFRAME#
LPCAD3
LPCAD2
LPCAD1
LPCAD0
U50
U51
F75913V
C510
C511
C512
C513
0.1uF_16V/C0402
R783
R777
2.2K
+V1.8A
+V3.3S
Enable CSE ROM Bypass
GPIO_39 | CSE ROM Bypass
0 | Disable bypass (default)
1 | Enable Bypass
Allow eMMC as a boot source
GPIO_43 | eMMC as a boot
0 | Disable
1 | Enable (default)
Allow SPI as a boot source
GPIO_44 | SPI as a boot
0 | Disable
1 | Enable (default)
Force DNX FW Load
GPIO_47 | DNX FW Load
0 | Do not force (default)
1 | Enable
LPC 1.8V/3.3V Mode Select
GPIO_110 | LPC Voltage
0 | 3.3V mode
1 | 1.8V mode (default)
Boot BIOS Strap (BBS)
GPIO_111
0 | Boot from SPI
1 | Do not boot from SPI (default)
Flash Descriptor Override
GPIO_118
0 | No Override (Normal Operation)
1 | Override
Top swap override
GPIO_120
0 | Disable (default)
1 | Override
Title
SOC_LPC_SPI_EMMC_SD
Size
Custom
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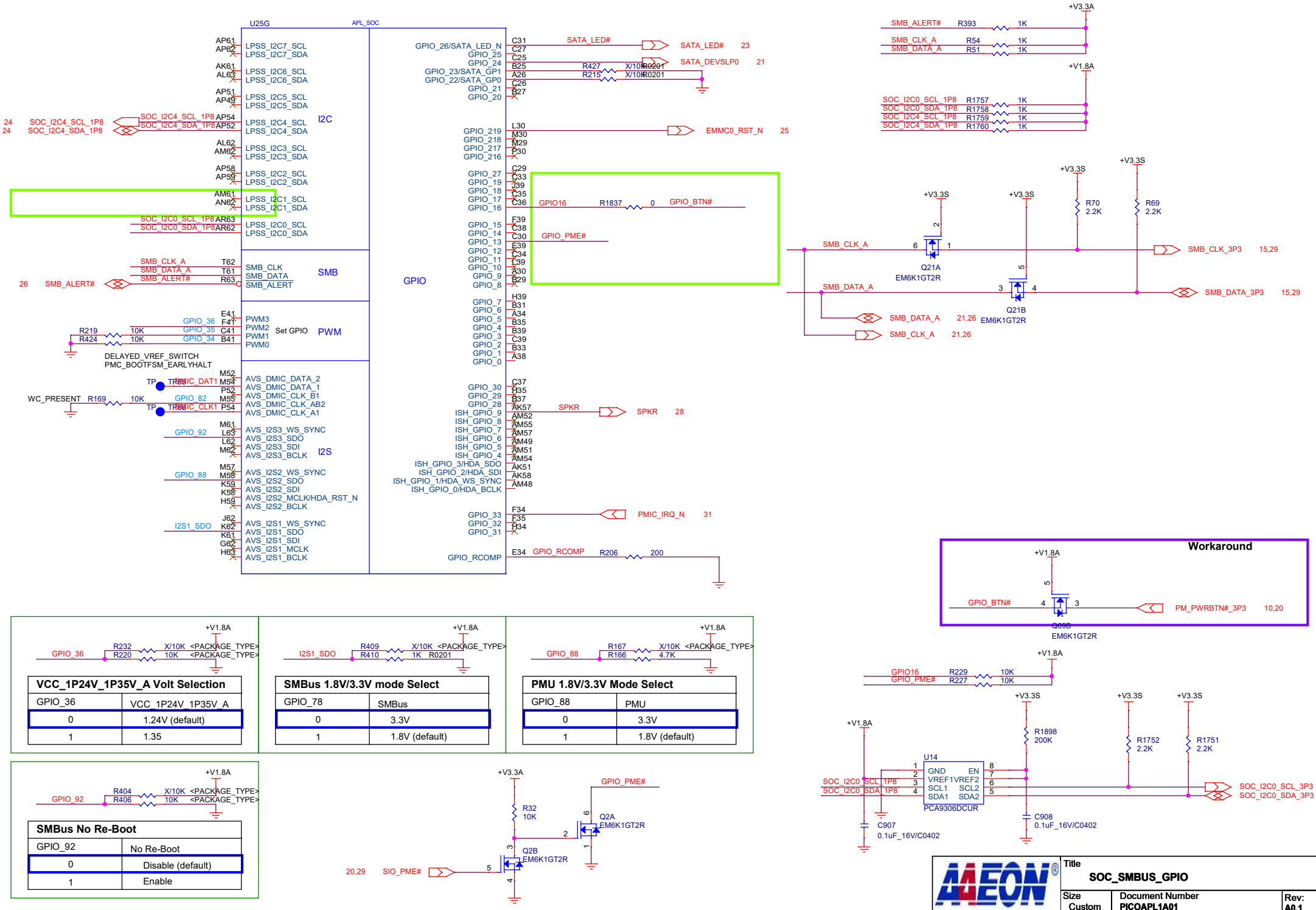

VCC_1P24V_1P35V_A Volt Selection	
GPIO_36	VCC_1P24V_1P35V_A
0	1.24V (default)
1	1.35

SMBus 1.8V/3.3V mode Select	
GPIO_78	SMBus
0	3.3V
1	1.8V (default)

PMU 1.8V/3.3V Mode Select	
GPIO_88	PMU
0	3.3V
1	1.8V (default)

SMBus No Re-Boot	
GPIO_92	No Re-Boot
0	Disable (default)
1	Enable

Title	SOC_SMBUS_GPIO
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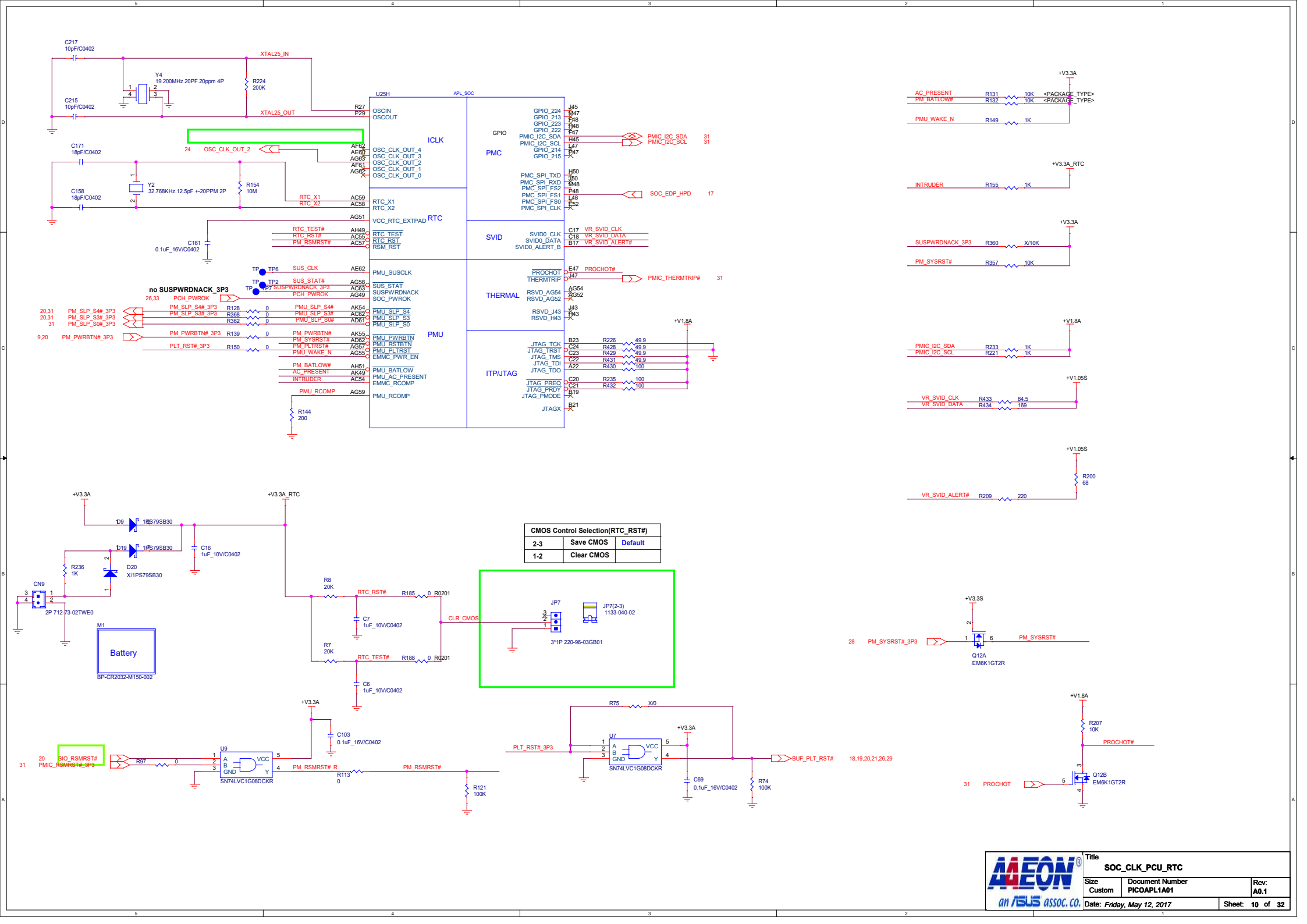

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Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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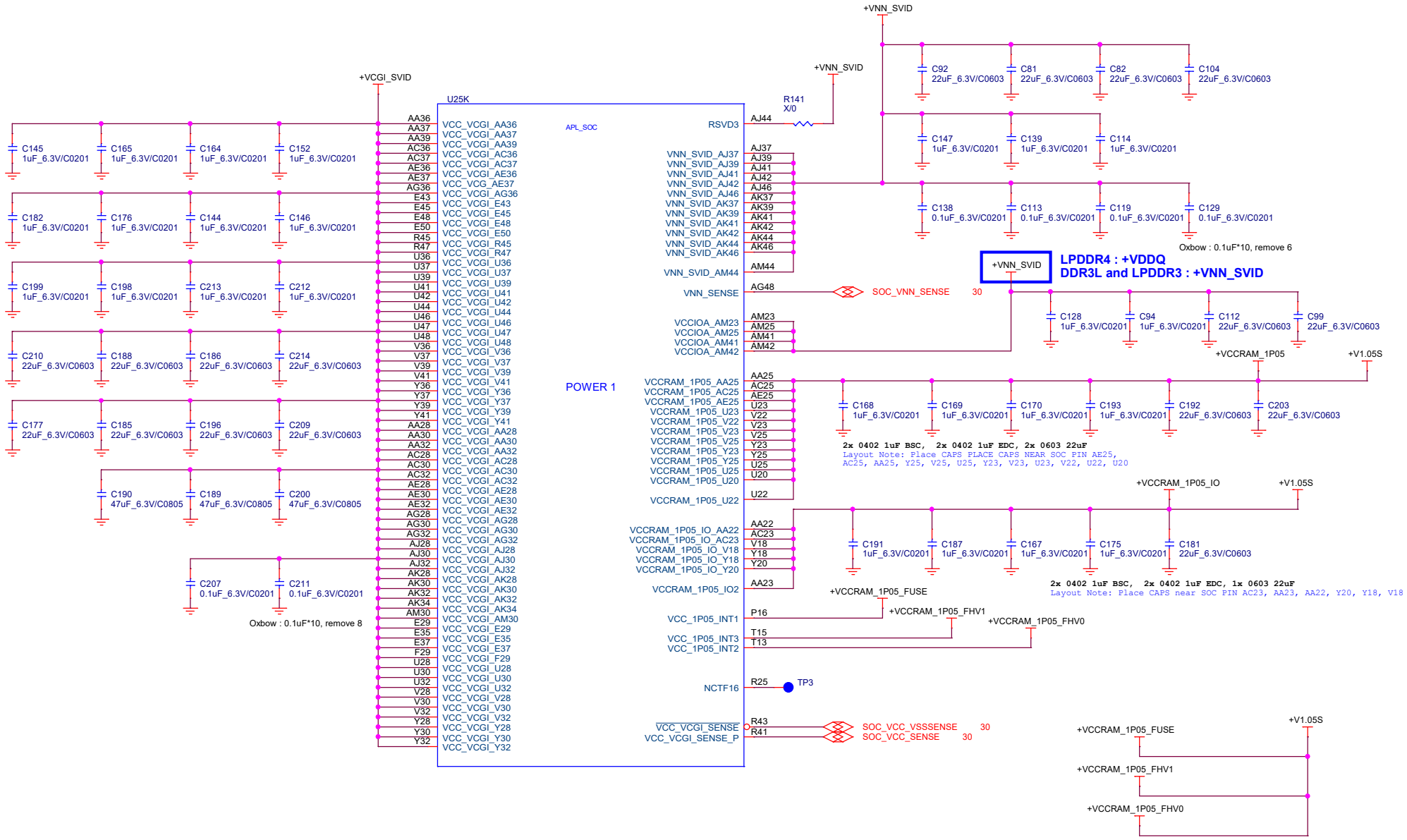

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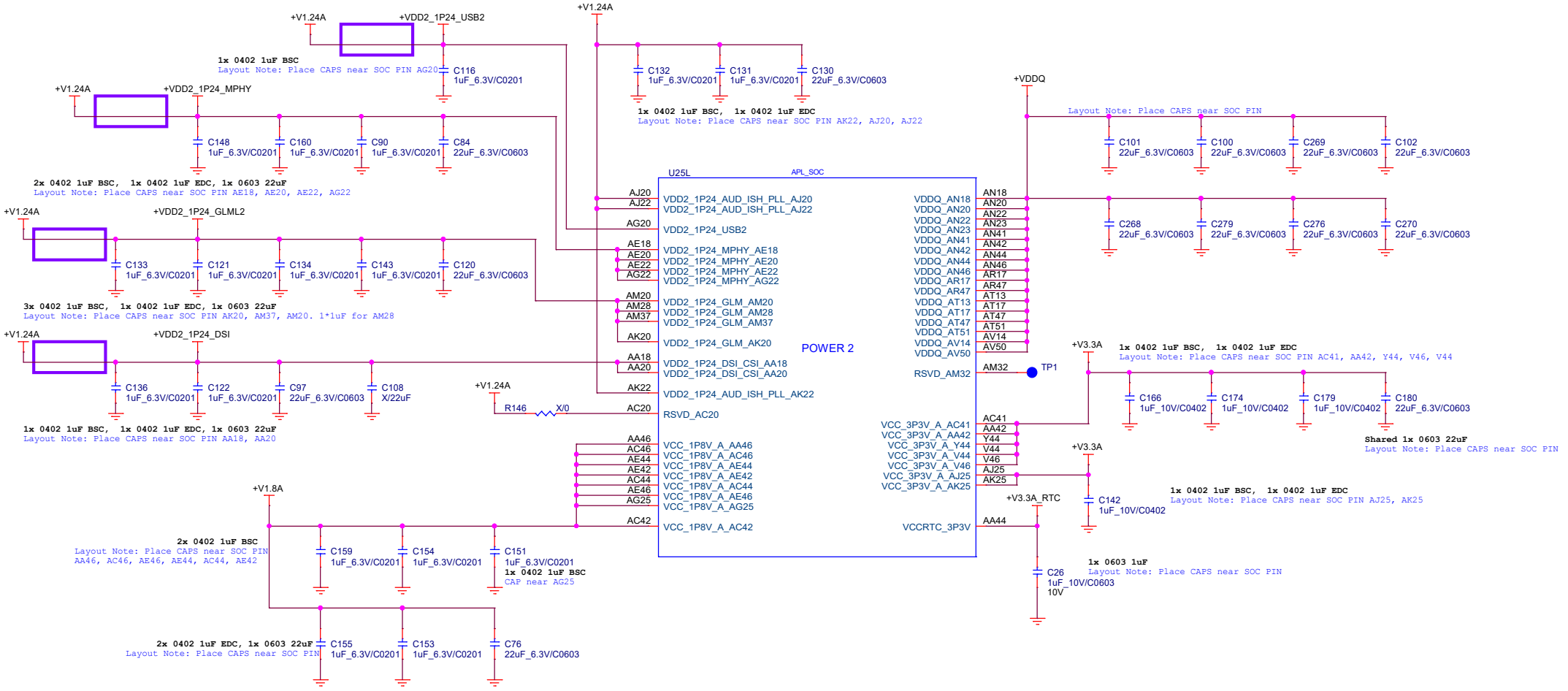

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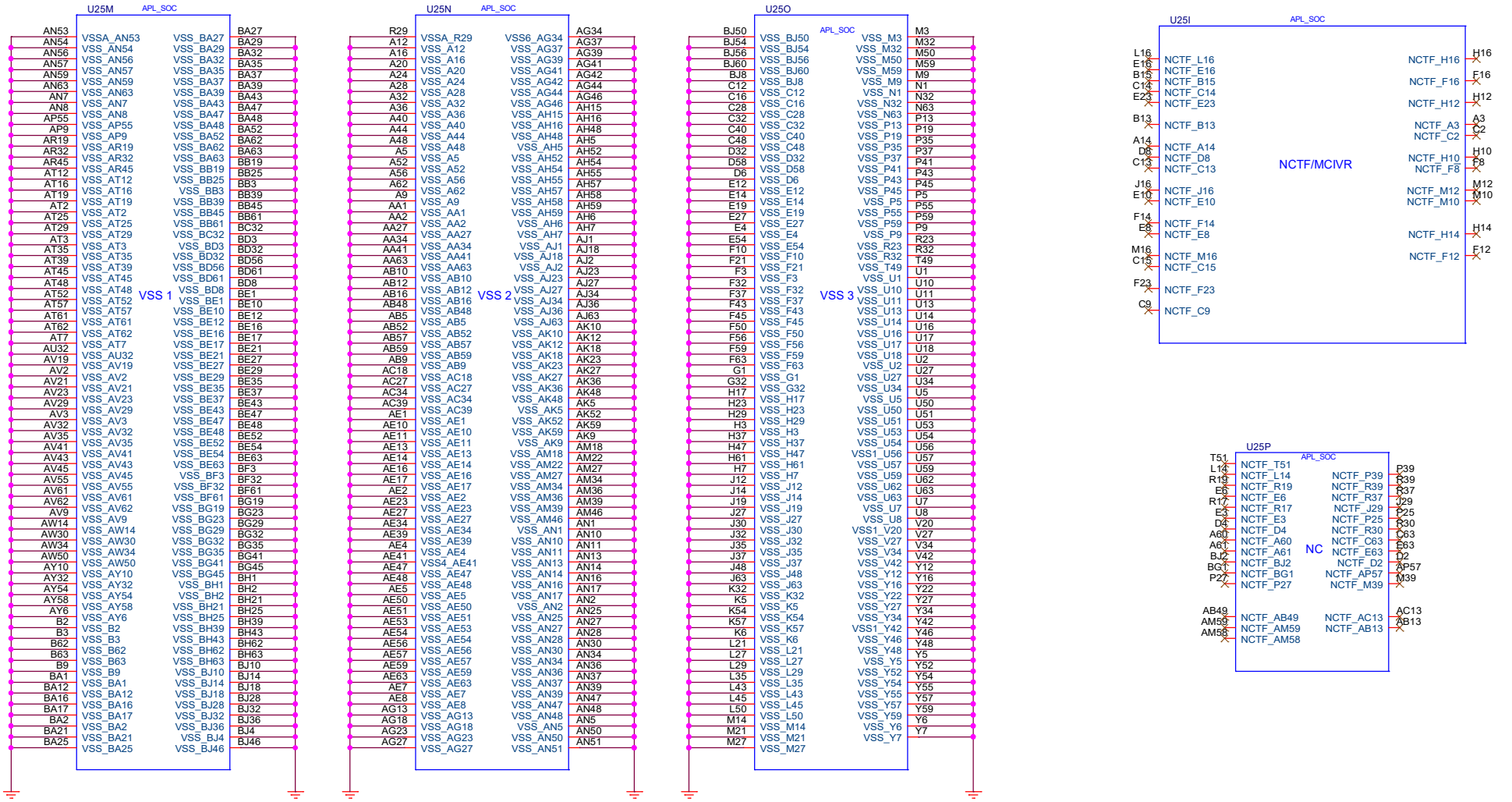

AAEON an ASUS assoc. co.

Title: SOC_GND

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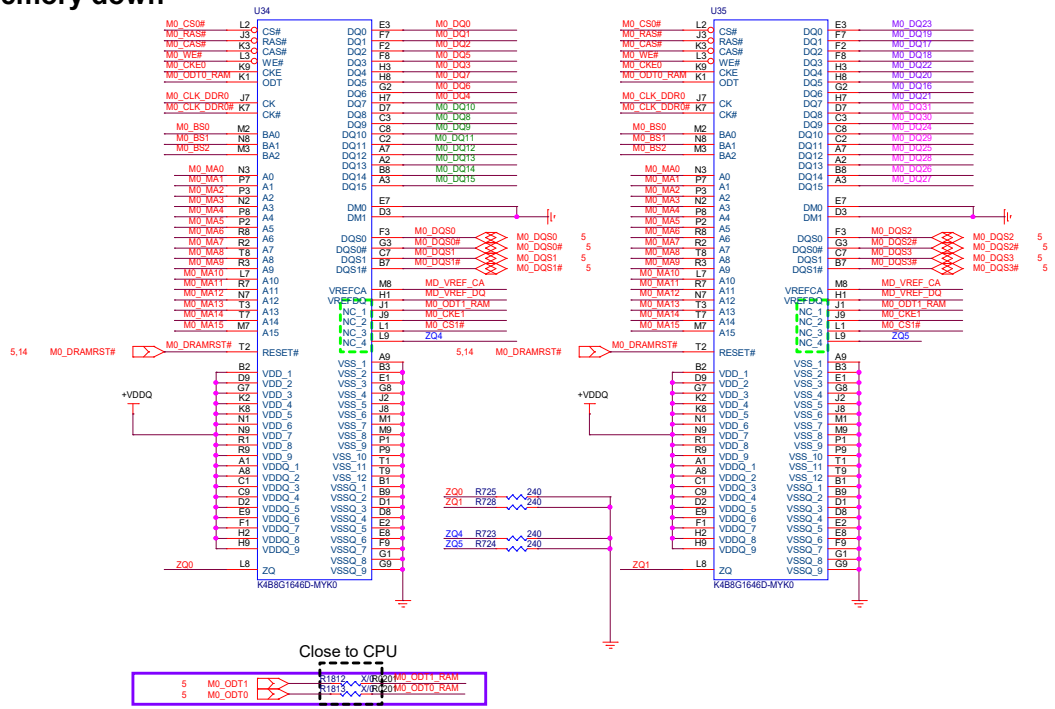
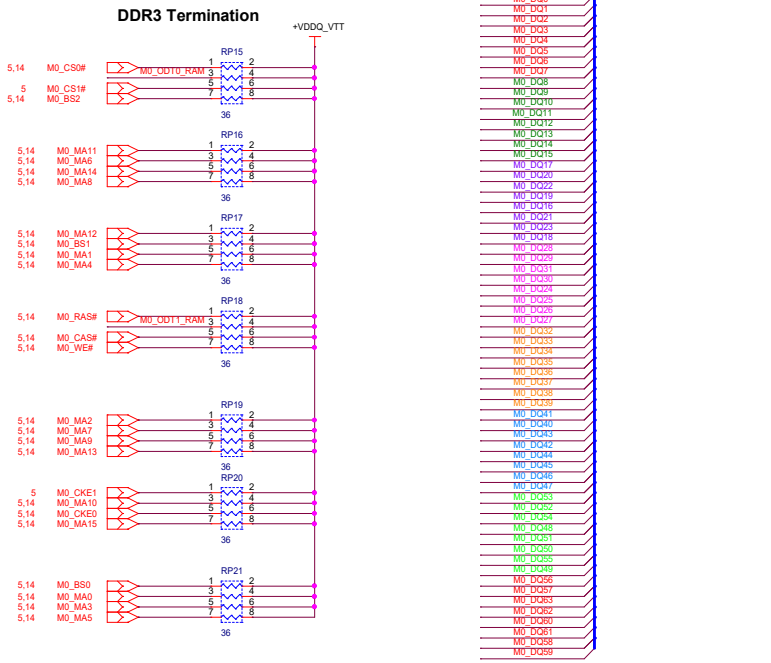
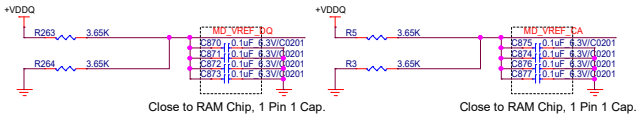
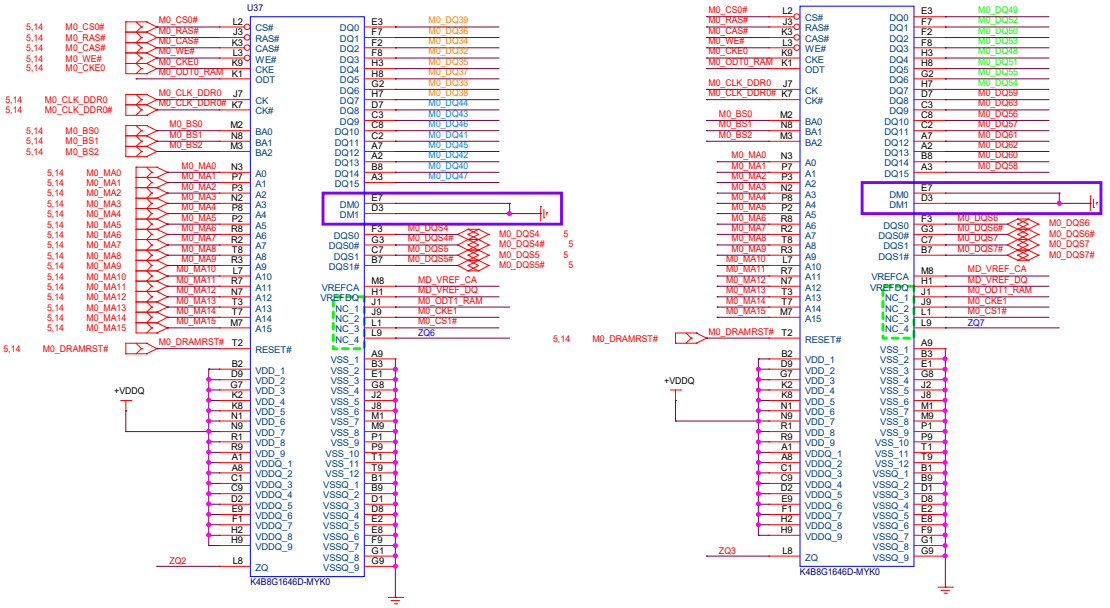
Memory down

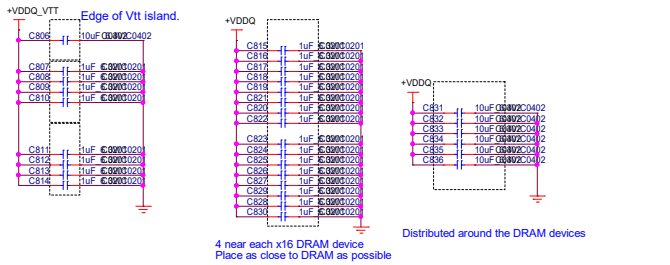


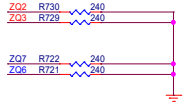


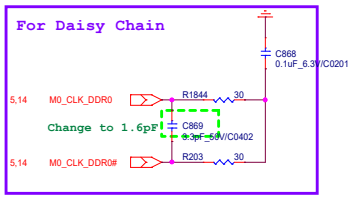


Memory down









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	Size: C	Document Number: PICOAPL1A01	Rev: A0.1
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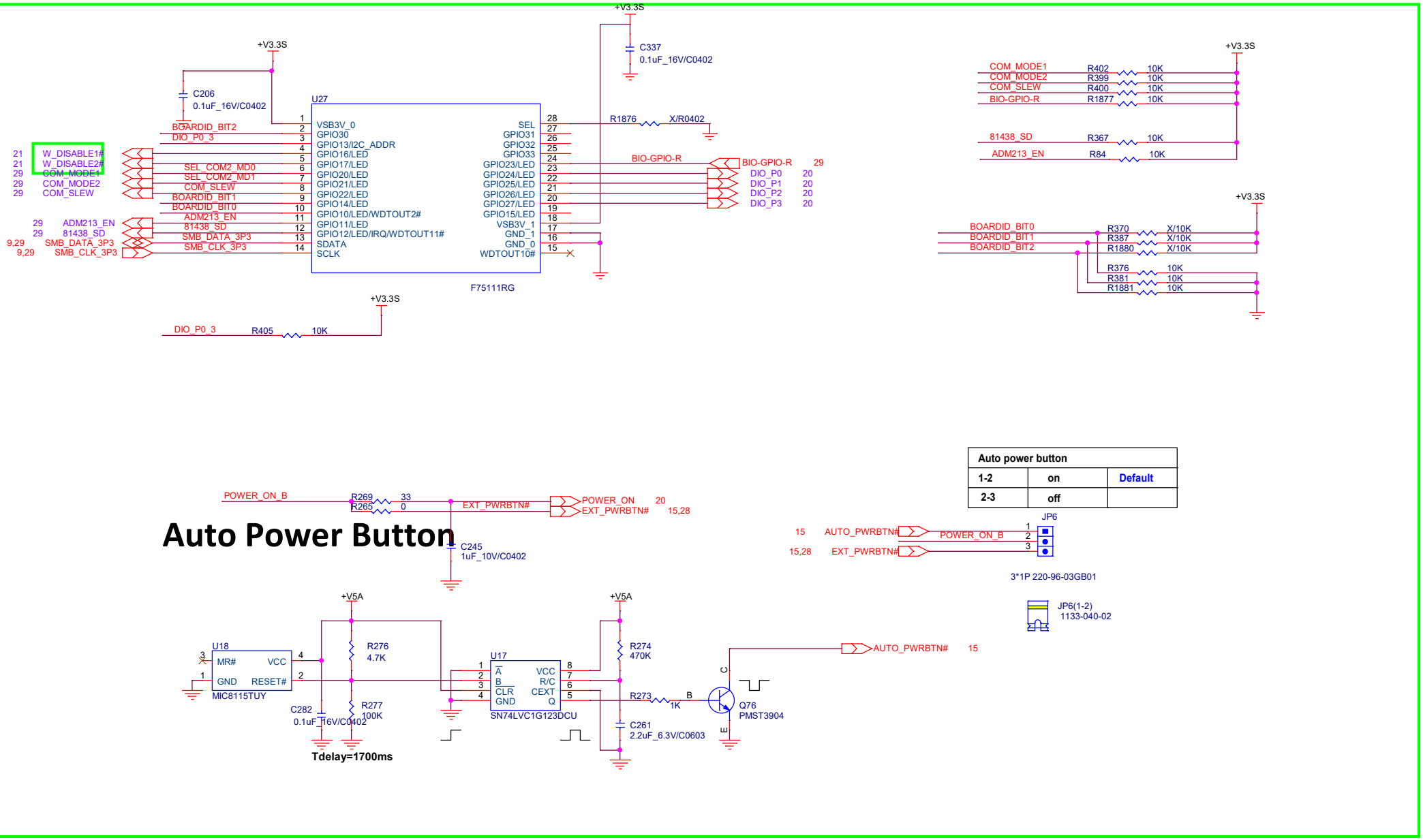
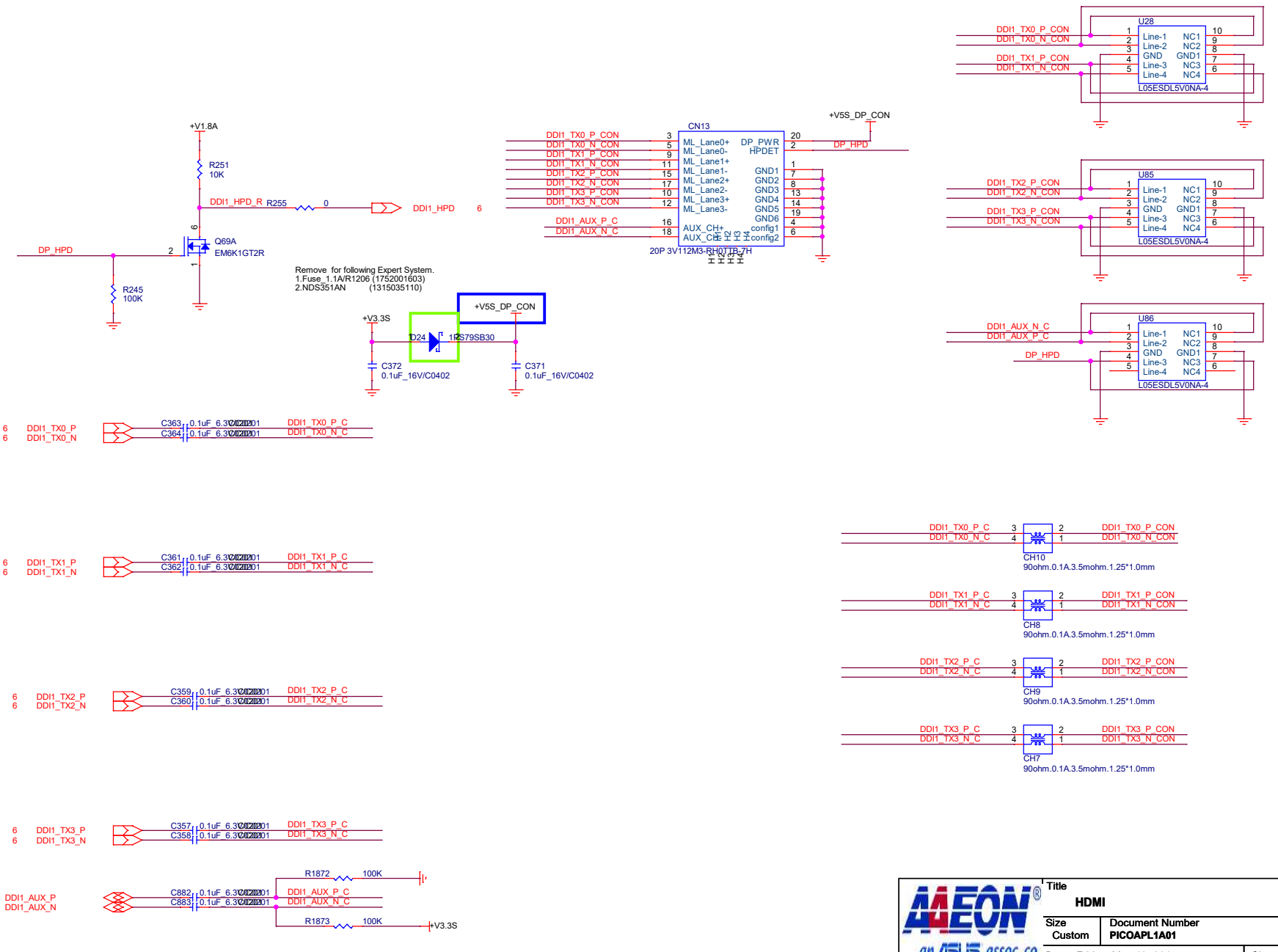


Auto Power Button

Auto power button		
1-2	on	Default
2-3	off	

AAEON an ASUS assoc. co.	Title: Level Shift		
	Size: B	Document Number: PICOAPL1A01	Rev: A0.1
	Date: Friday, May 12, 2017	Sheet: 15 of 32	

HDMI



Title	HDMI
Size	Custom
Document Number	PICOAPL1A01
Rev:	A0.1
Date:	Friday, May 12, 2017
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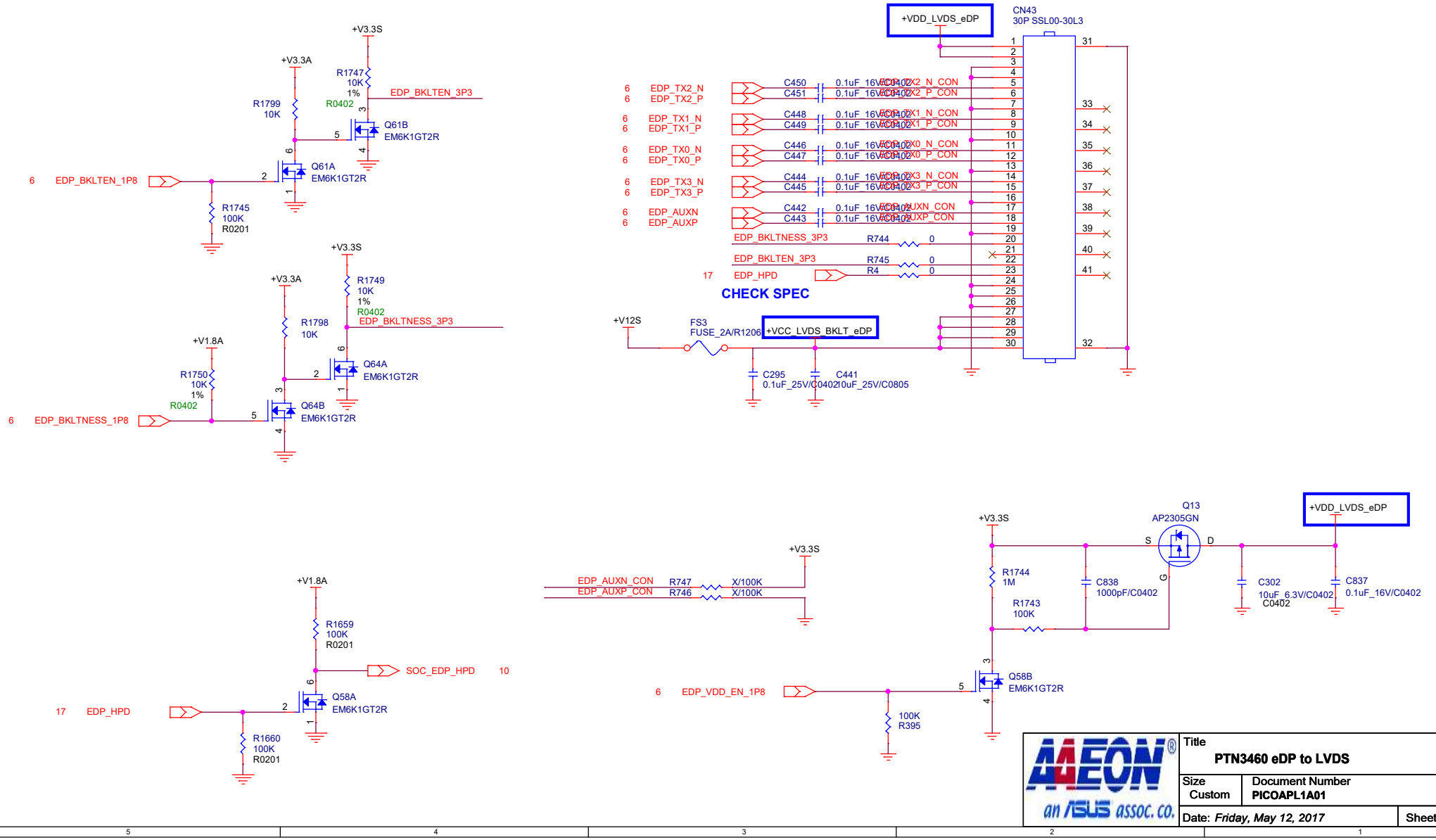


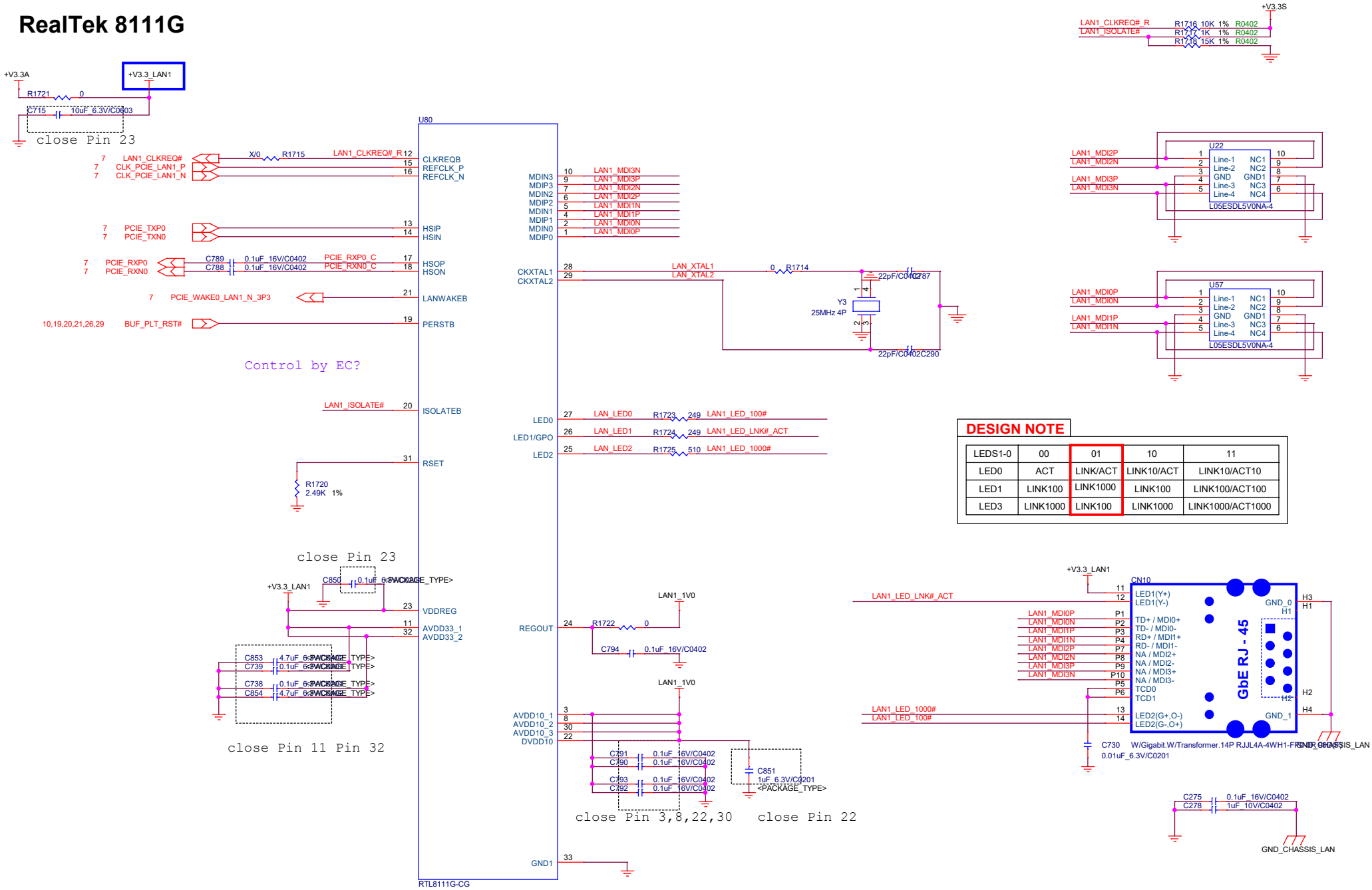
AAEON an ASUS assoc. co.

Title: **PTN3460 eDP to LVDS**

Size	Document Number	Rev:
Custom	PICOAPL1A01	A0.1

Date: *Friday, May 12, 2017* Sheet: **17** of **32**

RealTek 8111G



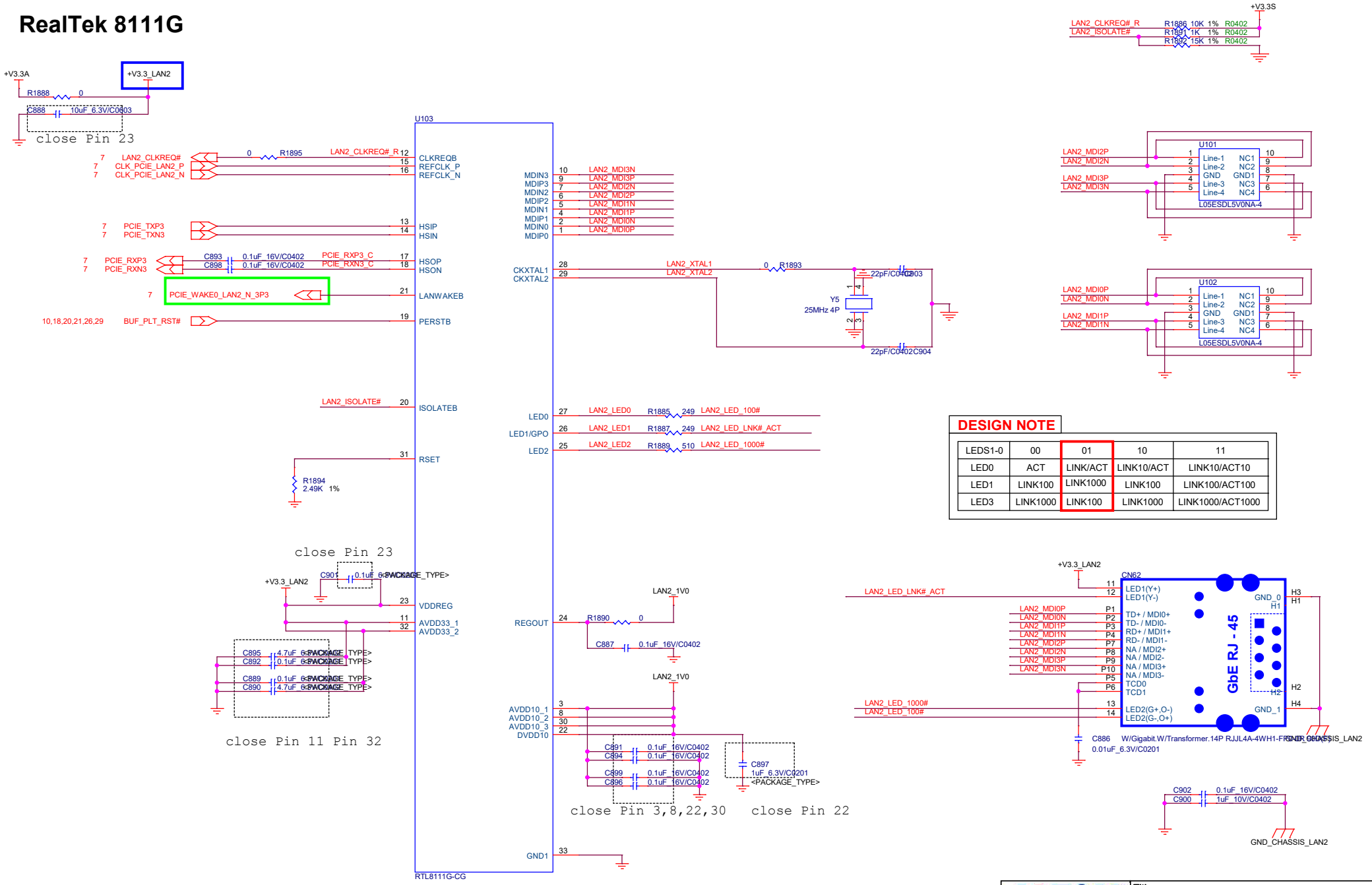
DESIGN NOTE

LEDS1-0	00	01	10	11
LED0	ACT	LINK/ACT	LINK10/ACT	LINK10/ACT10
LED1	LINK100	LINK1000	LINK100	LINK100/ACT100
LED3	LINK1000	LINK100	LINK1000	LINK1000/ACT1000

AAEON an ASUS assoc. co.

Title: LAN_INTEL i211		
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
Date: Friday, May 12, 2017		Sheet: 18 of 32

RealTek 8111G



DESIGN NOTE

LEDS1-0	00	01	10	11
LED0	ACT	LINK/ACT	LINK10/ACT	LINK10/ACT10
LED1	LINK100	LINK1000	LINK100	LINK100/ACT100
LED3	LINK1000	LINK100	LINK1000	LINK1000/ACT1000

AAEON an ASUS assoc. co.

Title: LAN2_INTEL i211

Size	Document Number	Rev:
Custom	PICOAPL1A01	A0.1

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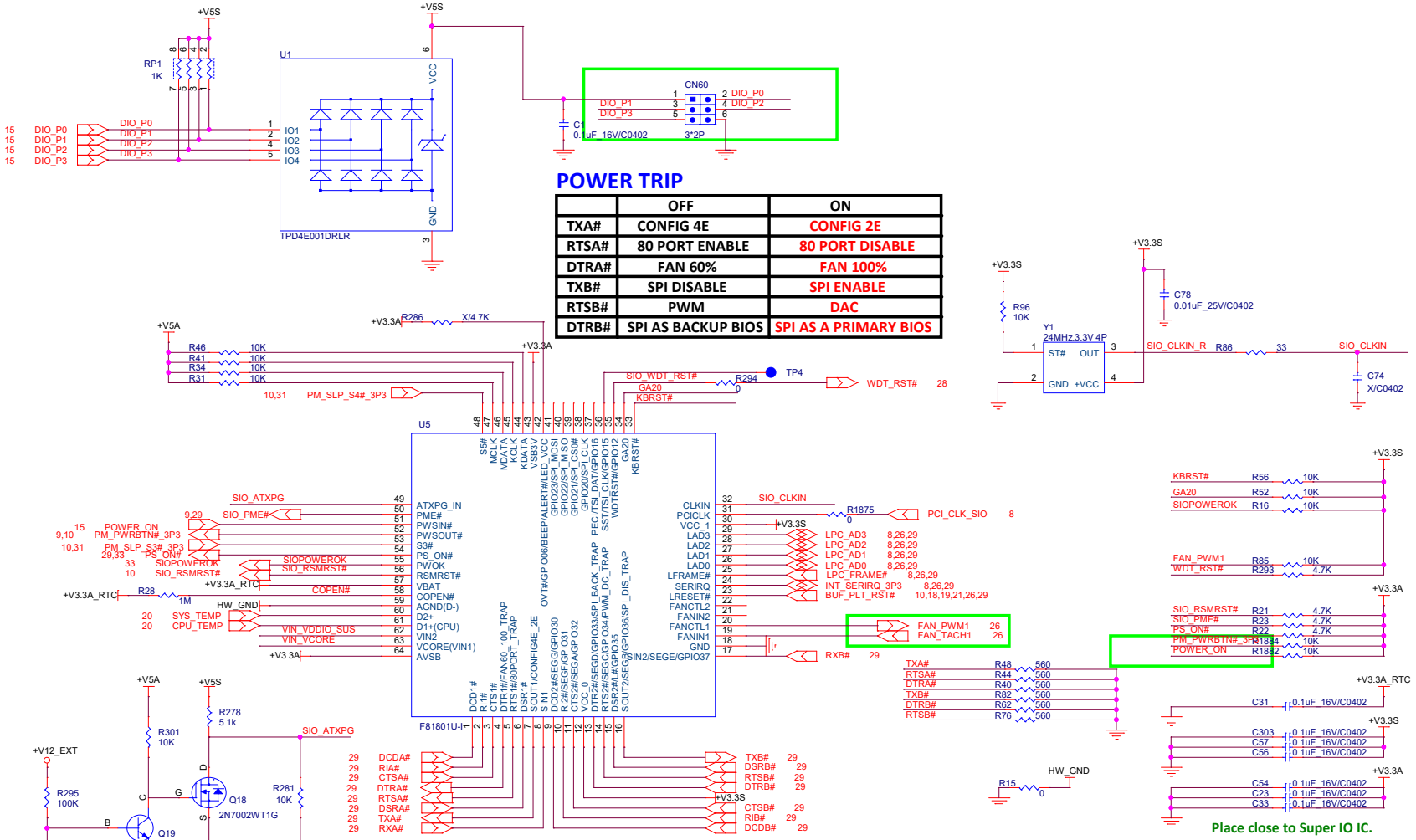
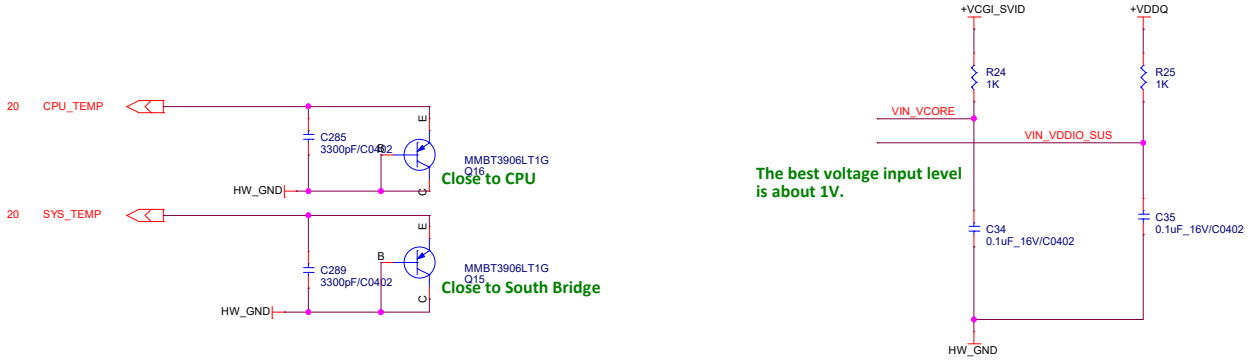


POWER TRIP

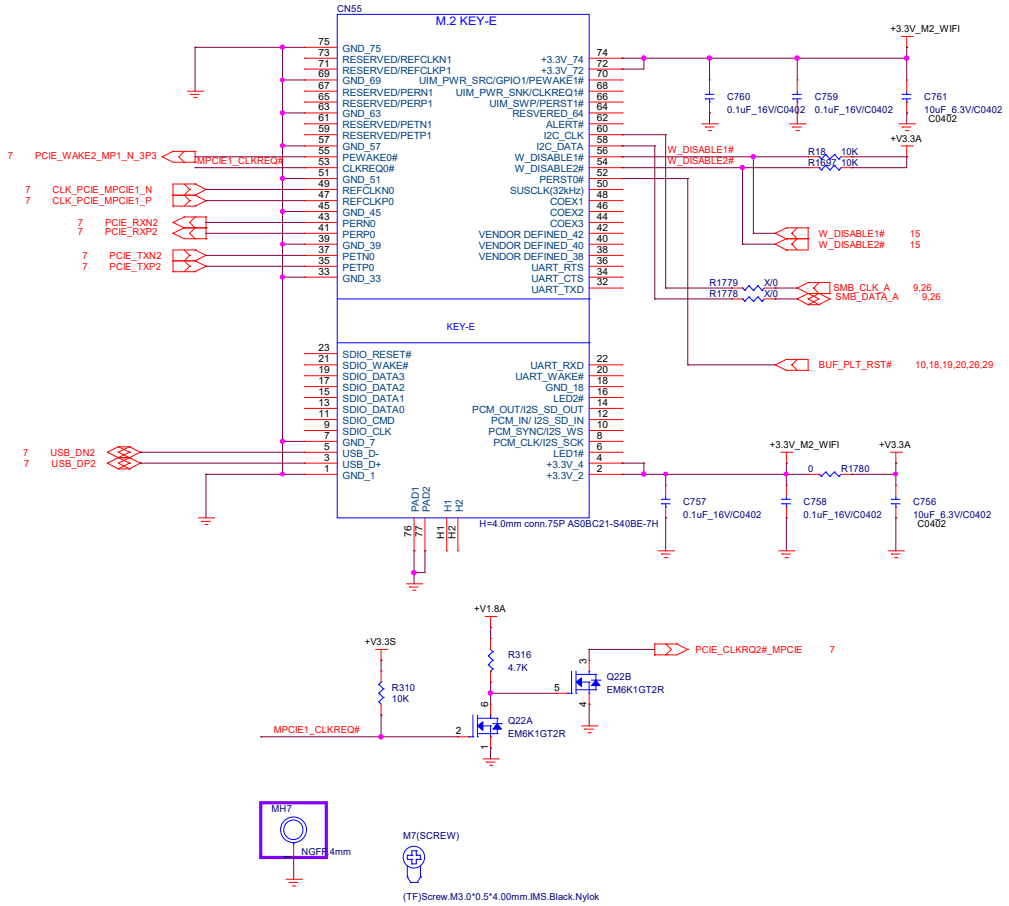
	OFF	ON
TXA#	CONFIG 4E	CONFIG 2E
RTSA#	80 PORT ENABLE	80 PORT DISABLE
DTRA#	FAN 60%	FAN 100%
TXB#	SPI DISABLE	SPI ENABLE
RTSB#	PWM	DAC
DTRB#	SPI AS BACKUP BIOS	SPI AS A PRIMARY BIOS

Temperature Monitor(CPU, SYS)

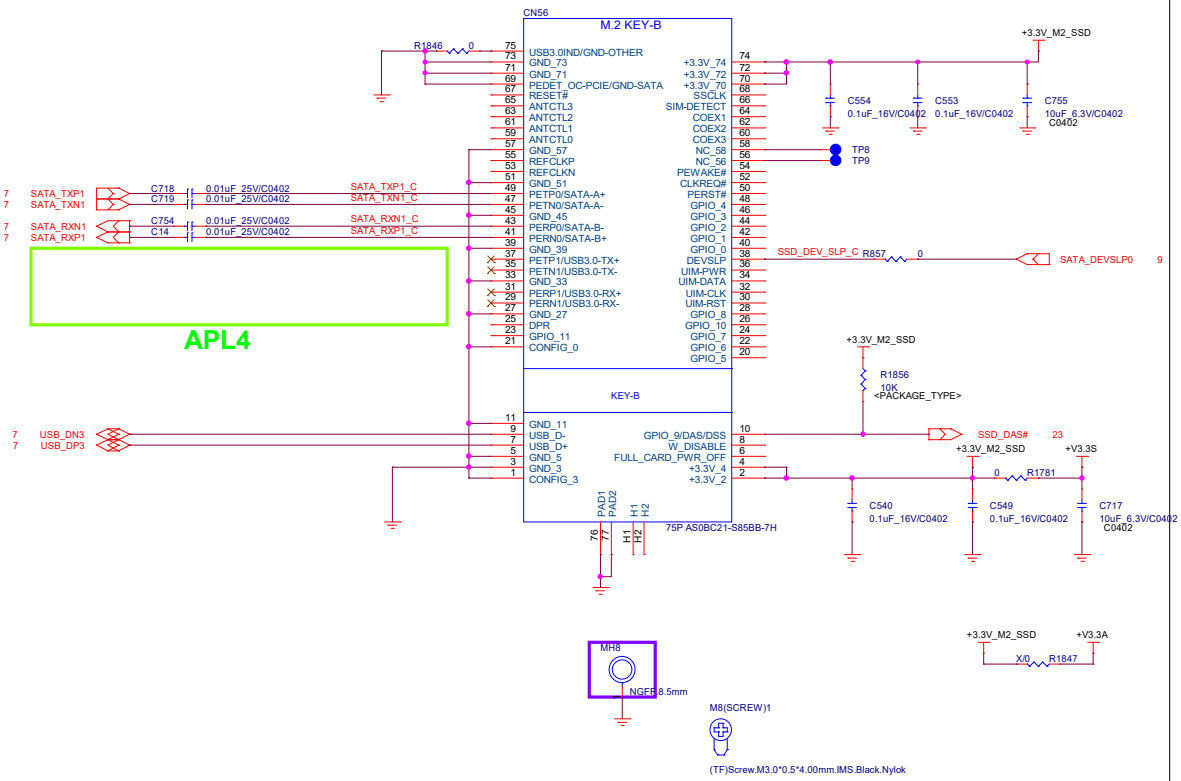


AAEON an ASUS assoc. co.	Title: Super I/O F81801U-I	
	Size: Custom	Document Number: PICOAPL1A01 Rev: A0.1
	Date: Friday, May 12, 2017	Sheet: 19 of 32

M.2 Key E



M.2 Key B



AAEON an ASUS assoc. co.	Title: mini-Card/mSATA		
	Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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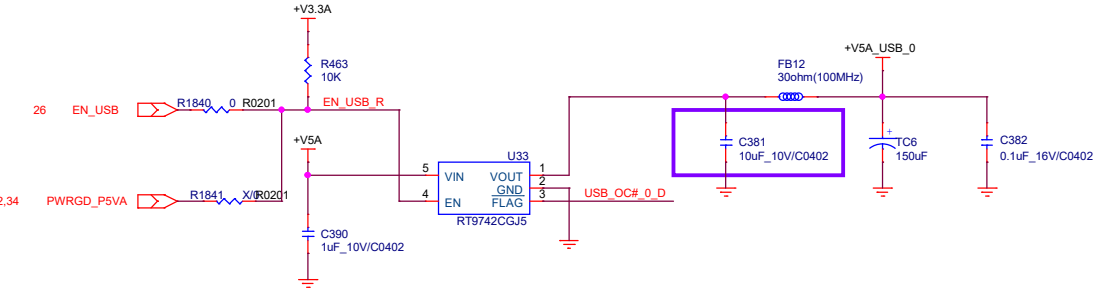
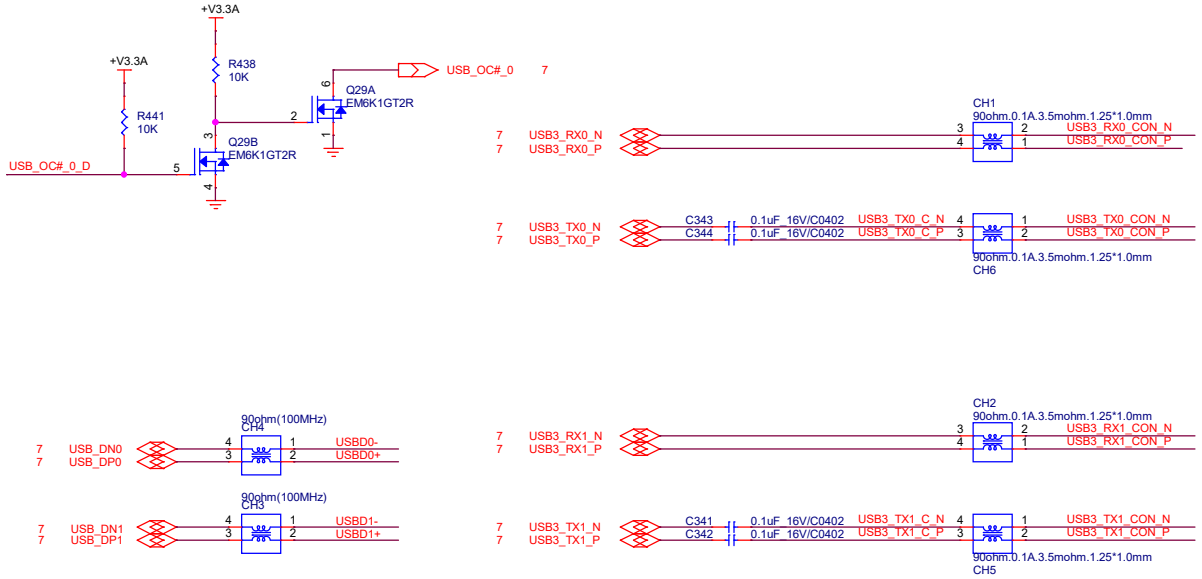
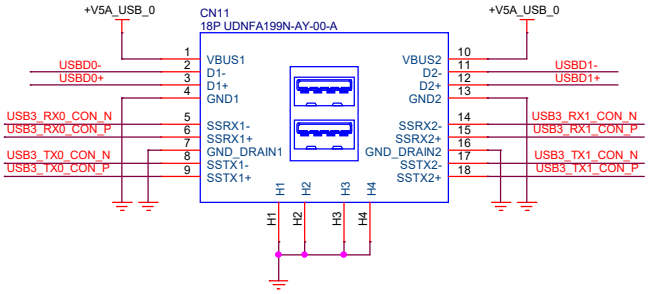
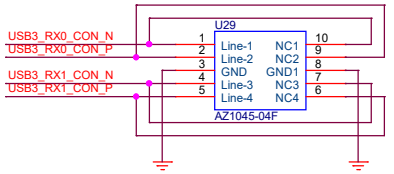
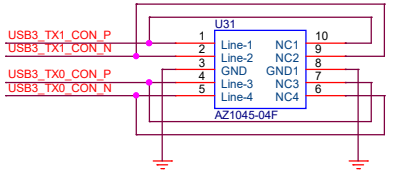
USB3.0 x 2

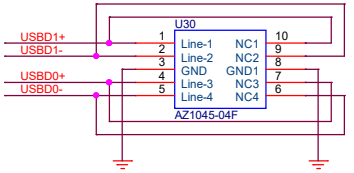












AAEON an ASUS assoc. co.

Title: USB 3.0/2.0 PORT		
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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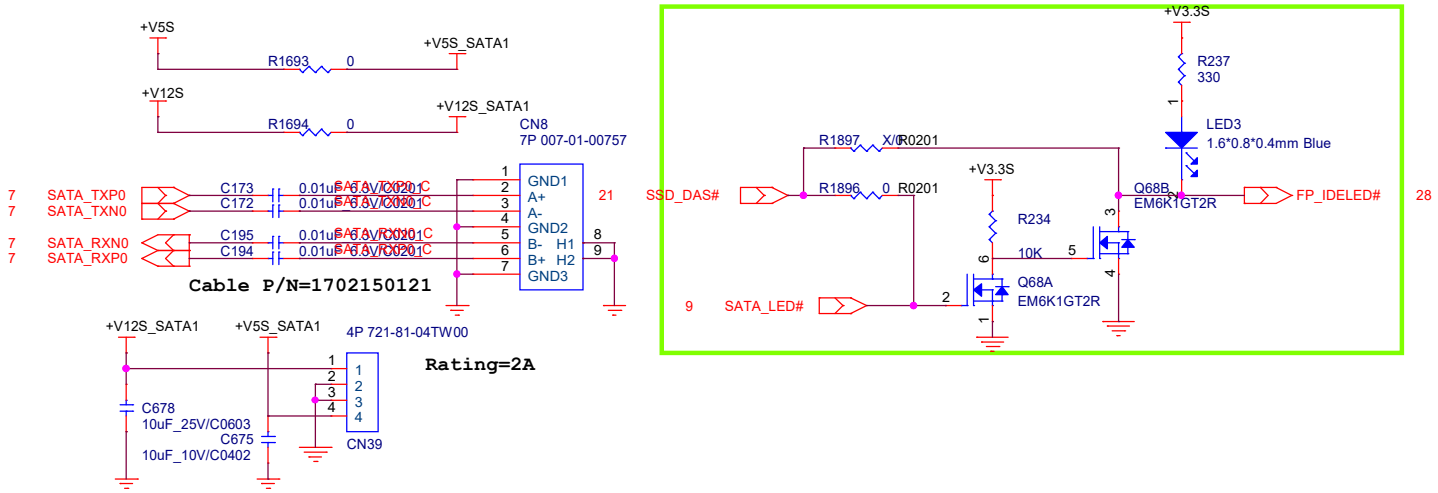
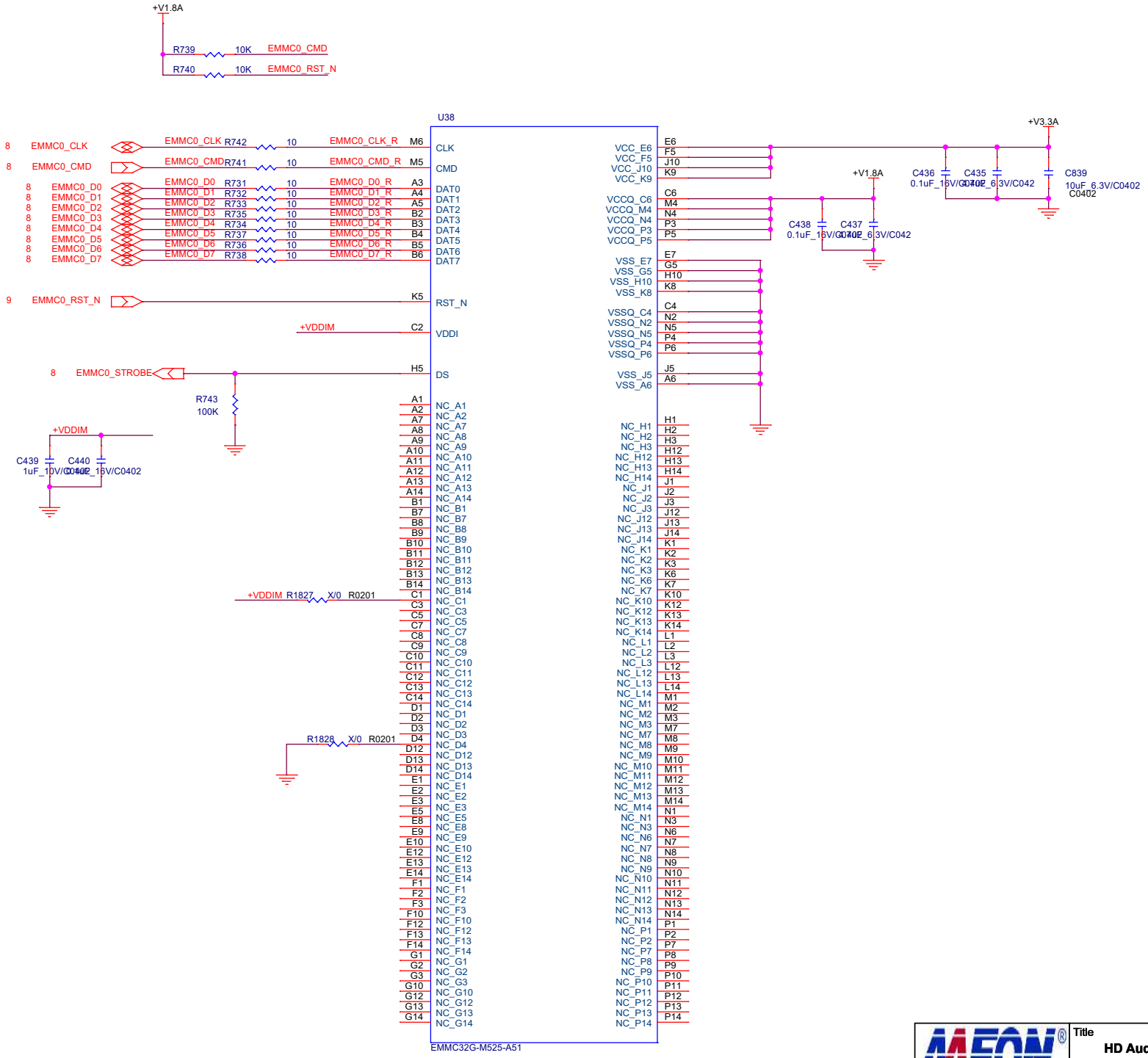


AAEON an ASUS assoc. co.	Title: **Serial Port 1/2/SATA**	
Size: Custom	Document Number: **PICOAPL1A01**	Rev: **A0.1**
Date: *Friday, May 12, 2017*	Sheet: **22** of **32**	


+V1.8A
R739 10K EMMC0_CMD
R740 10K EMMC0_RST_N
U38
8 EMMC0_CLK
8 EMMC0_CMD
8 EMMC0_D0
8 EMMC0_D1
8 EMMC0_D2
8 EMMC0_D3
8 EMMC0_D4
8 EMMC0_D5
8 EMMC0_D6
8 EMMC0_D7
9 EMMC0_RST_N
8 EMMC0_STROBE
+VDDIM
R743 100K
C439 1uF_10V/C0402
C440 0.1uF_16V/C0402
R742 10 EMMC0_CLK_R
R741 10 EMMC0_CMD_R
R731 10 EMMC0_D0_R
R732 10 EMMC0_D1_R
R733 10 EMMC0_D2_R
R735 10 EMMC0_D3_R
R734 10 EMMC0_D4_R
R737 10 EMMC0_D5_R
R736 10 EMMC0_D6_R
R738 10 EMMC0_D7_R
CLK
CMD
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
RST_N
VDDI
DS
+VDDIM R1827 X/0 R0201
R1828 X/0 R0201
EMMC32G-M525-A51
+V3.3A
+V1.8A
C436 0.1uF_16V/C0402
C435 1uF_6.3V/C042
C839 10uF_6.3V/C0402
C438 0.1uF_16V/C0402
C437 1uF_6.3V/C042
Title
HD Audio - ALC892
Size Custom
Document Number PICOAPL1A01
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Date: Friday, May 12, 2017
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AAEON an ASUS assoc. co.	Title: HD Audio - ALC892	
Size: B	Document Number: PICOAPL1A01	Rev: A0.1
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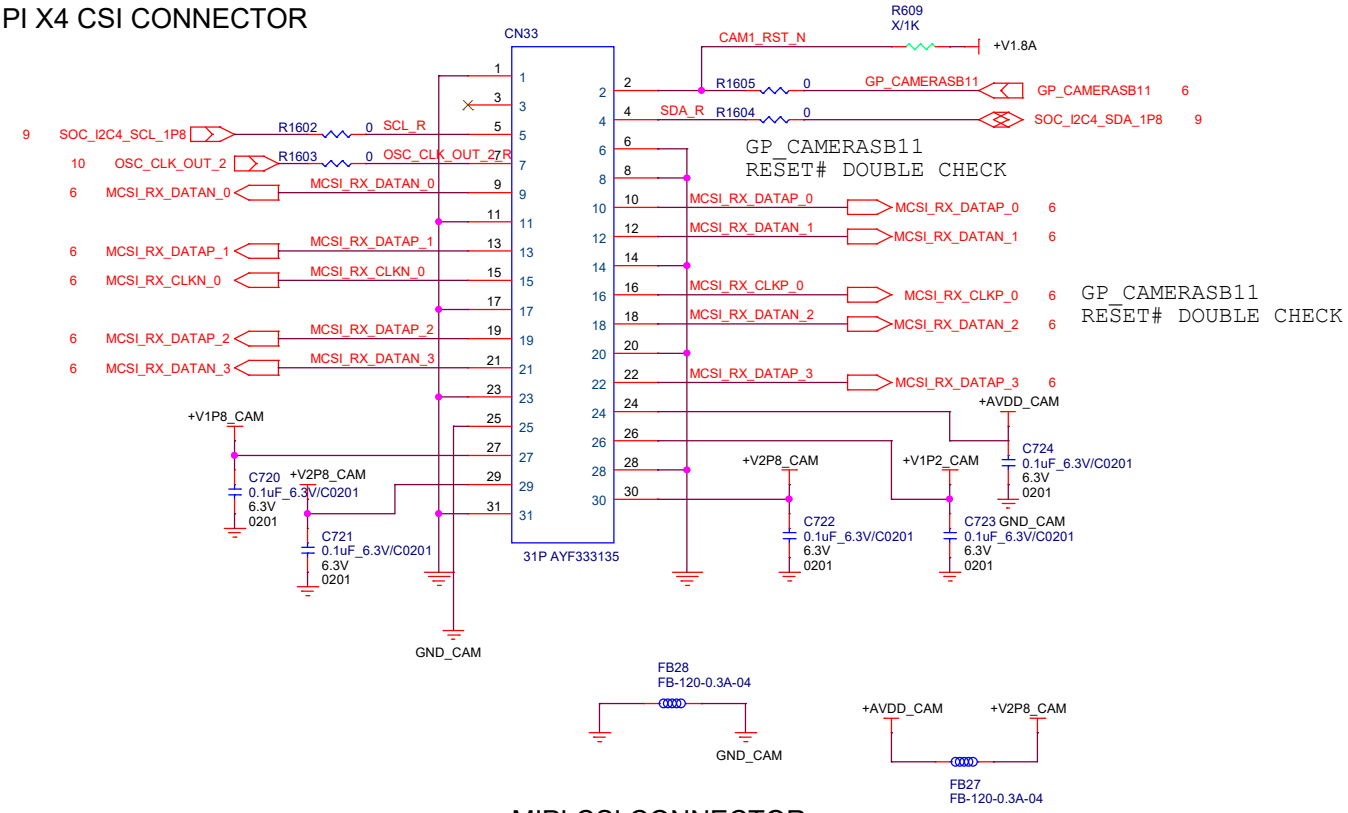
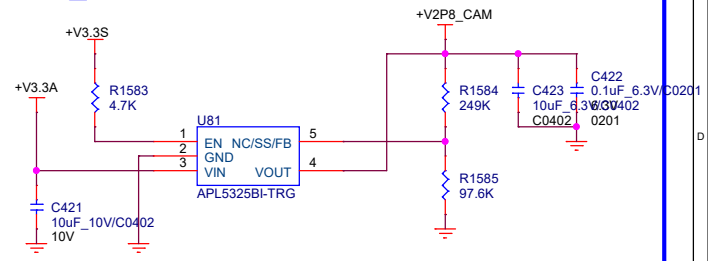
MIPI X4 CSI CONNECTOR



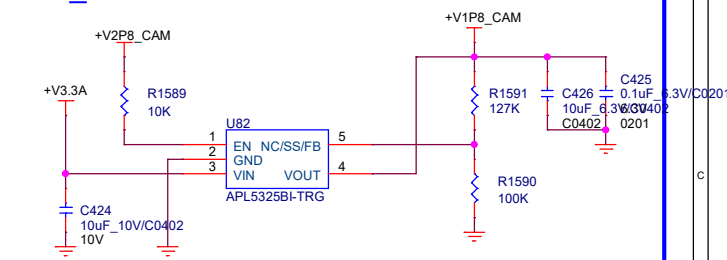
GP_CAMERASB11
RESET# DOUBLE CHECK

MIPI CSI CONNECTOR

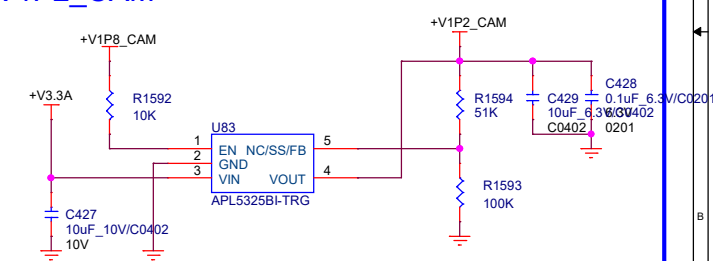
+V2P8_CAM



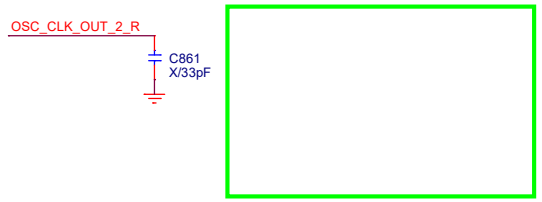
+V1P8_CAM



+V1P2_CAM



Reserved for OSC Clock Filter (Close to Connector)



AAEON an ASUS assoc. co.	Title: MIPI	
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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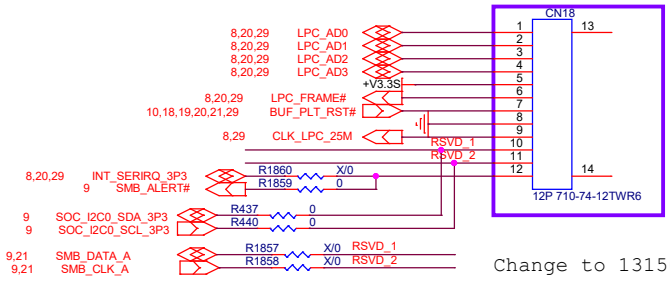
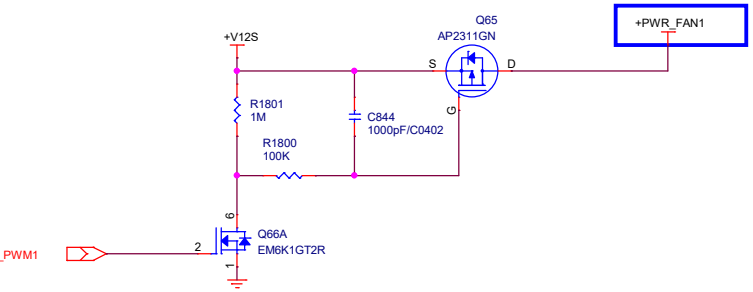
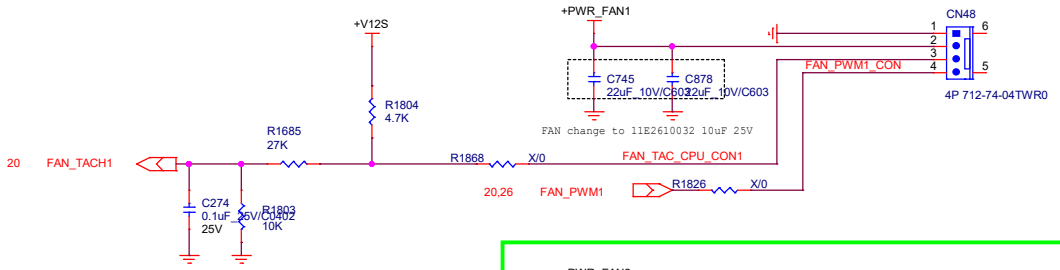
LPC Debug Connector

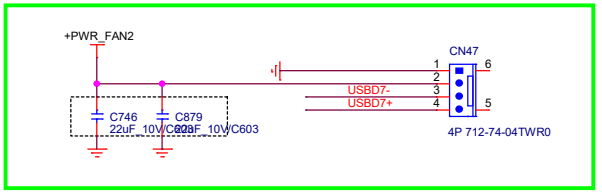


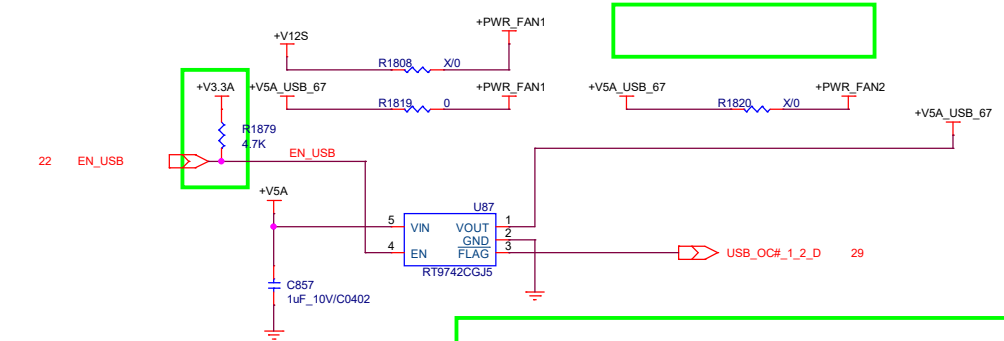
Change to 1315023110



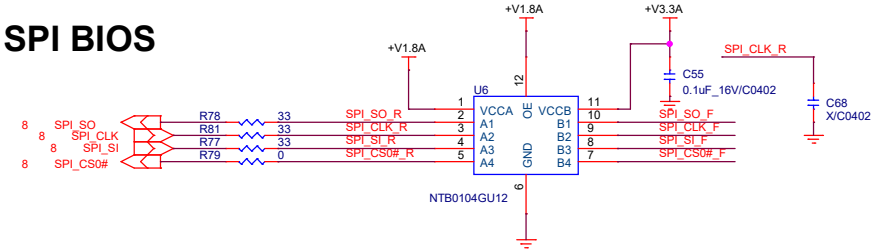
FAN1 Co-lay USB

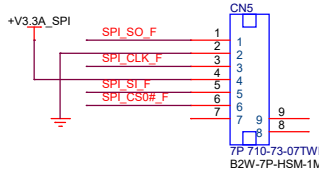


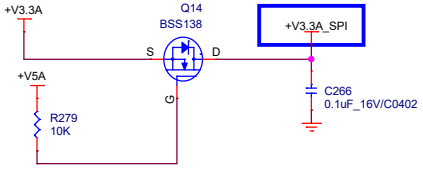


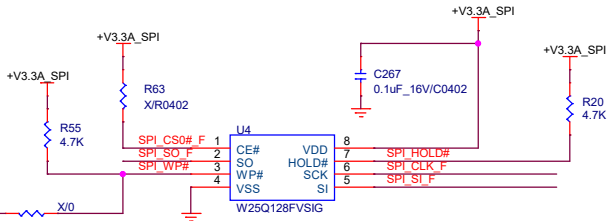


SPI BIOS









AAEON an ASUS assoc. co.	Title: H/W Mon/ Debug /CMOS	
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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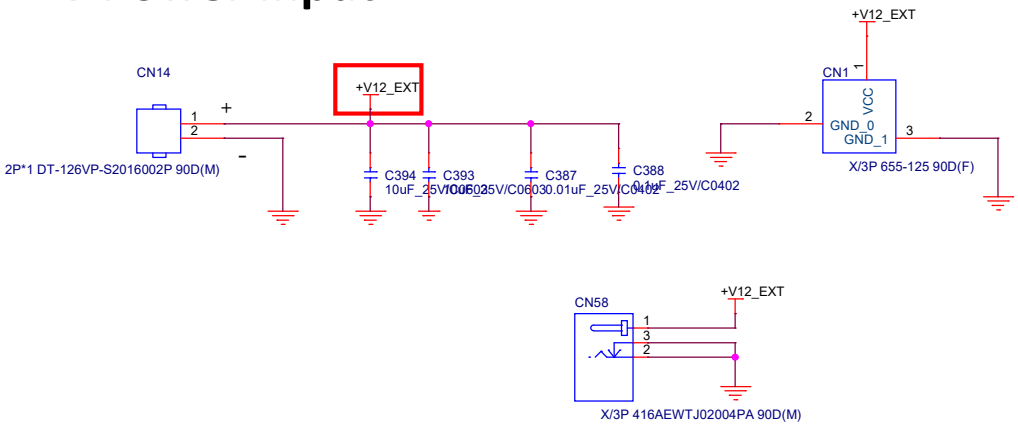
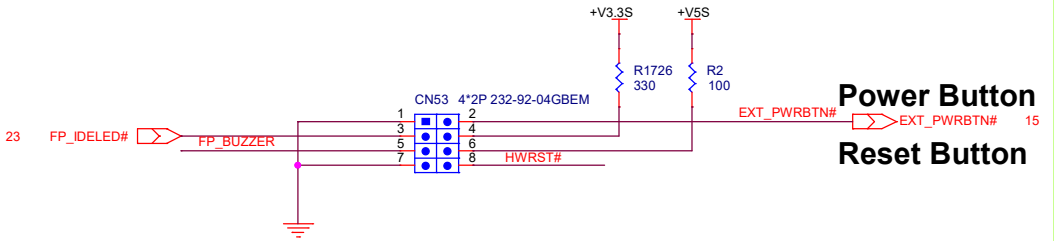
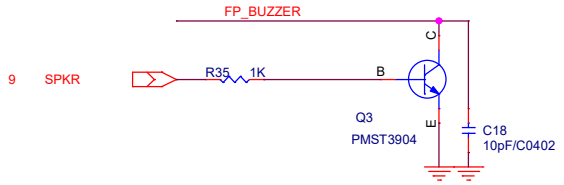
+12V Power Input



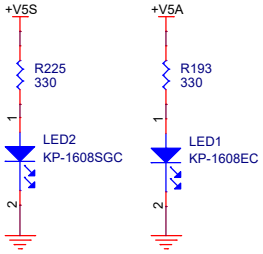
Front Panel



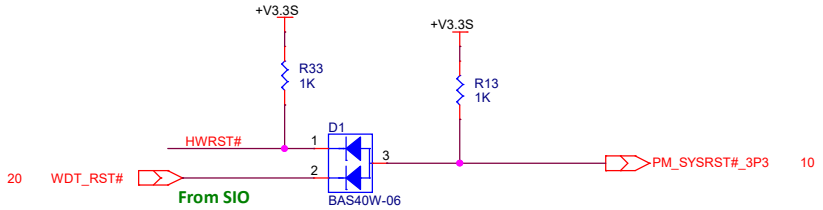
Auto power button		
No Stuff	ATX	Default
1-2	AT	



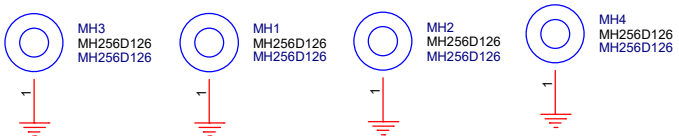
Power LED



System Reset



Mounting Holes / Non-PTH



AAEON an ASUS assoc. co.	Title: Auto Power Button/Power in		
	Size: B	Document Number: PICOAPL1A01	Rev: A0.1
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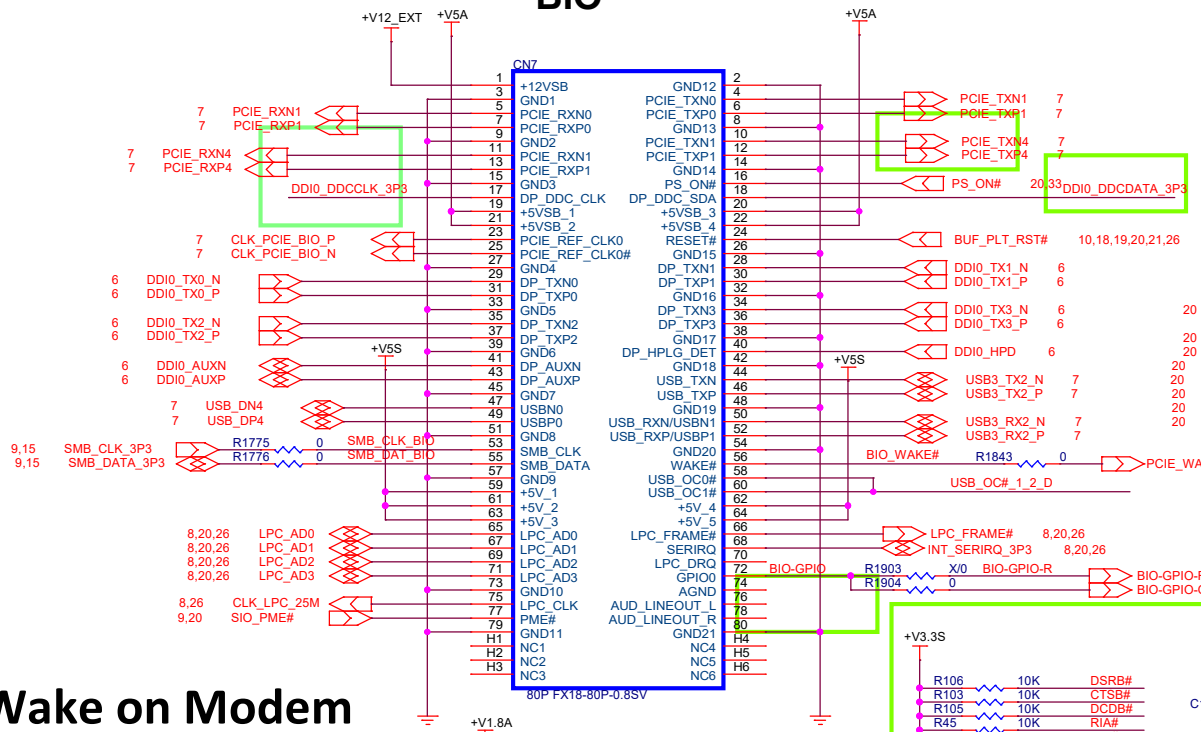
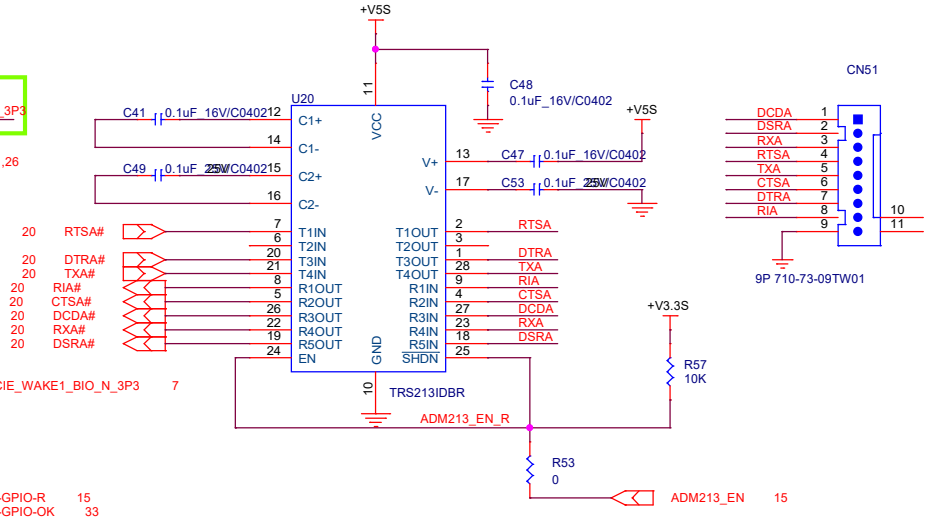
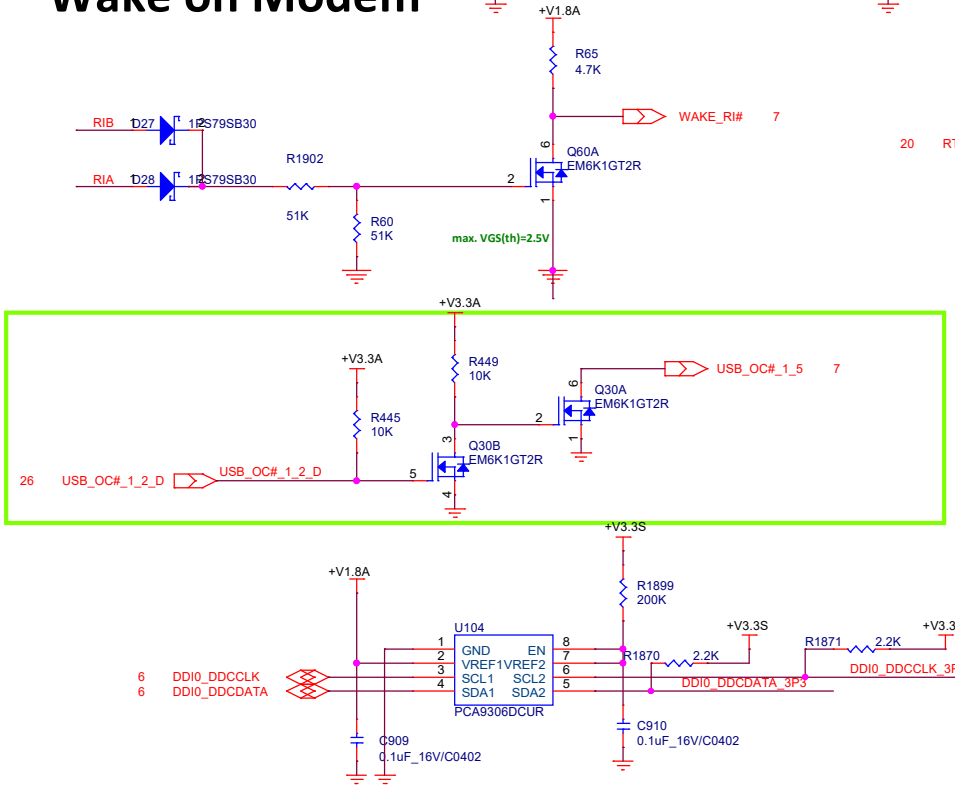
BIO



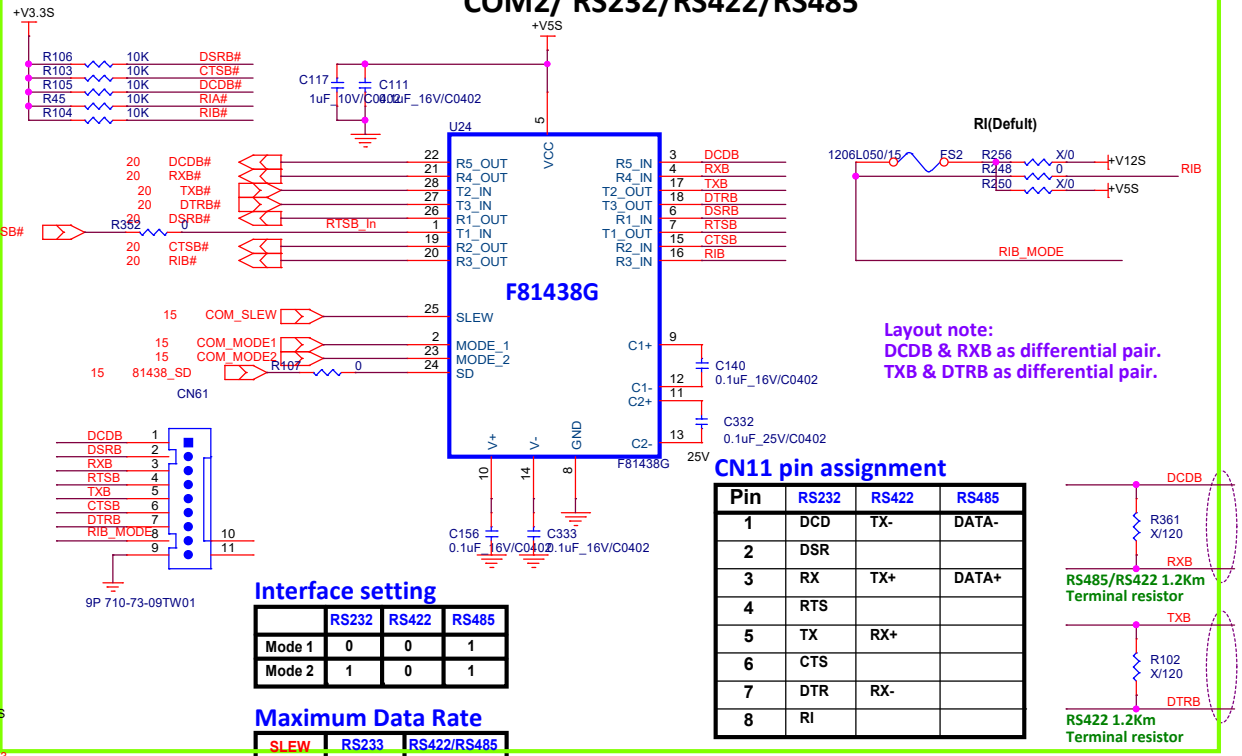
COM1/RS232



Wake on Modem



COM2/ RS232/RS422/RS485



Layout note:
DCDB & RXB as differential pair.
TXB & DTRB as differential pair.

CN11 pin assignment

Pin	RS232	RS422	RS485
1	DCD	TX-	DATA-
2	DSR		
3	RX	TX+	DATA+
4	RTS		
5	TX	RX+	
6	CTS		
7	DTR	RX-	
8	RI		

Interface setting

	RS232	RS422	RS485
Mode 1	0	0	1
Mode 2	1	0	1

Maximum Data Rate

SLEW	RS233	RS422/RS485
1	250kbps	250kbps

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Title: BIO/GPIO		
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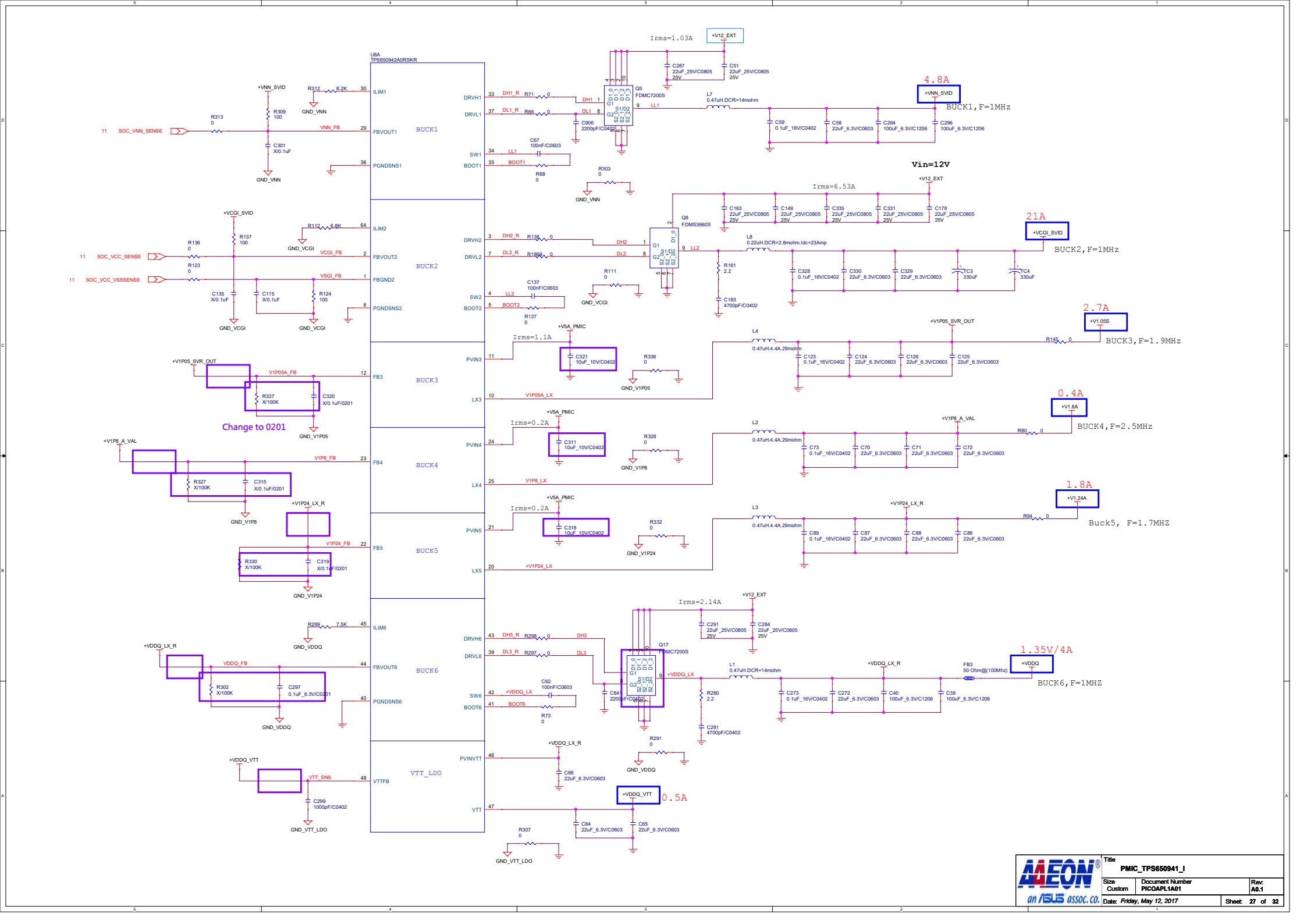
U8A
TPS650942A0RSKR
BUCK1
BUCK2
BUCK3
BUCK4
BUCK5
BUCK6
VTT_LDO
Irms=1.03A
+V12_EXT
4.8A
+VNN_SVID
BUCK1,F=1MHz
Vin=12V
Irms=6.53A
21A
+VCGI_SVID
BUCK2,F=1MHz
Irms=1.1A
2.7A
+V1.05S
BUCK3,F=1.9MHz
0.4A
+V1.8A
BUCK4,F=2.5MHz
Irms=0.2A
1.8A
+V1.24A
Buck5, F=1.7MHZ
Irms=2.14A
1.35V/4A
+VDDQ
BUCK6,F=1MHZ
0.5A
+VDDQ_VTT
Change to 0201
FDMC7200S
FDMS3660S
Title
PMIC_TPS650941_I
Size
Custom
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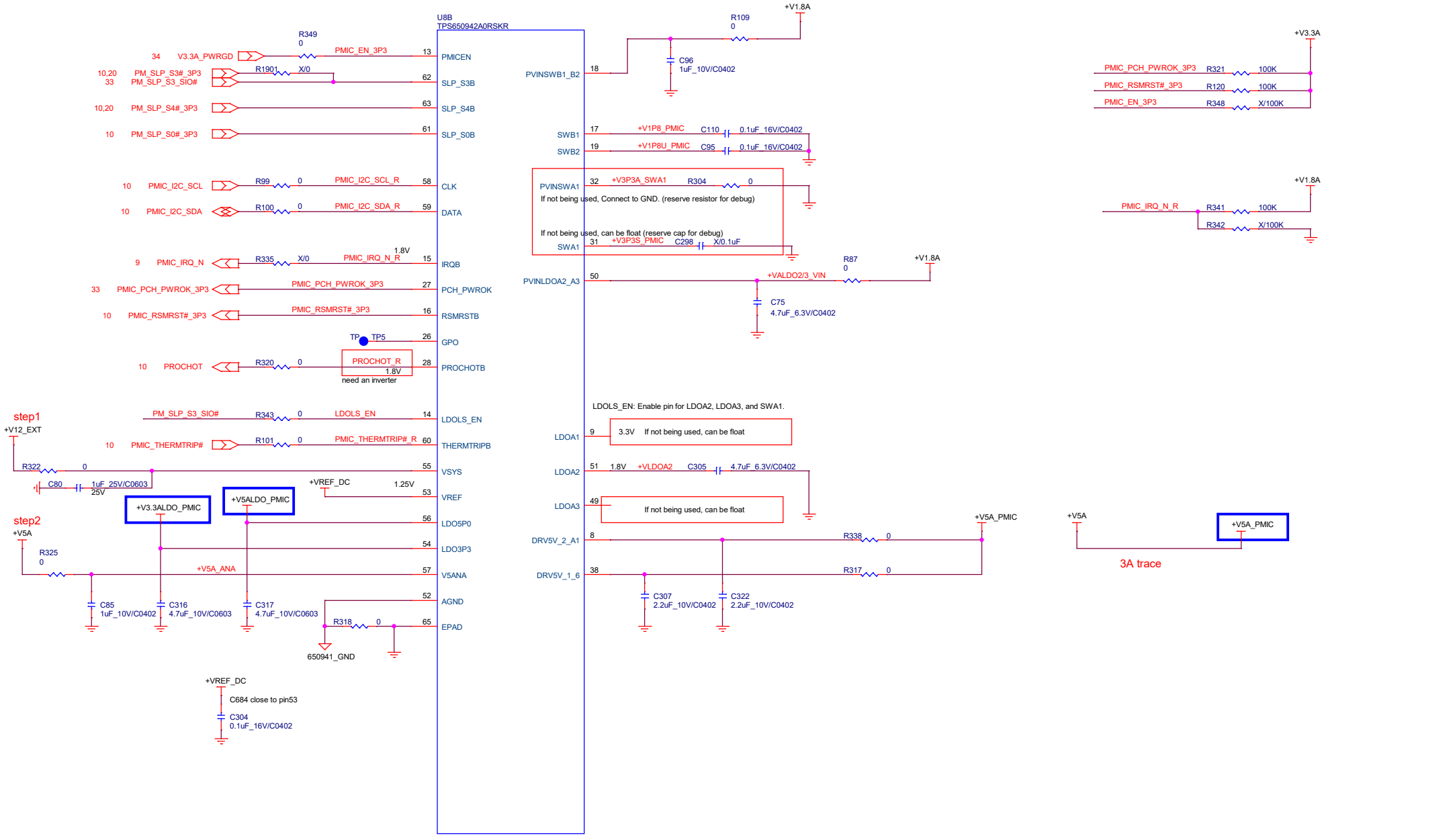

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	Size: Custom	Document Number: PICOAPL1A01 — Rev: A0.1
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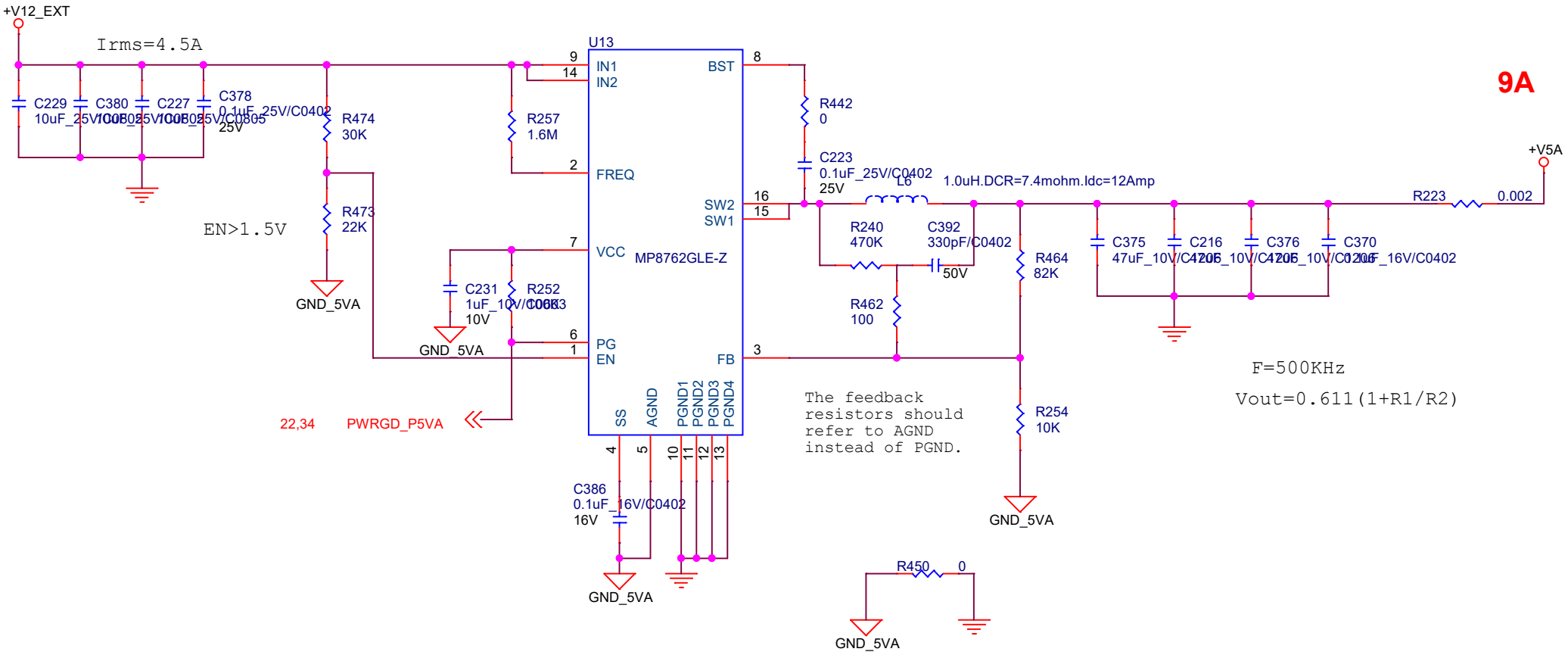

AAEON an ASUS assoc. co.	Title: **Power VR : +V5A**	
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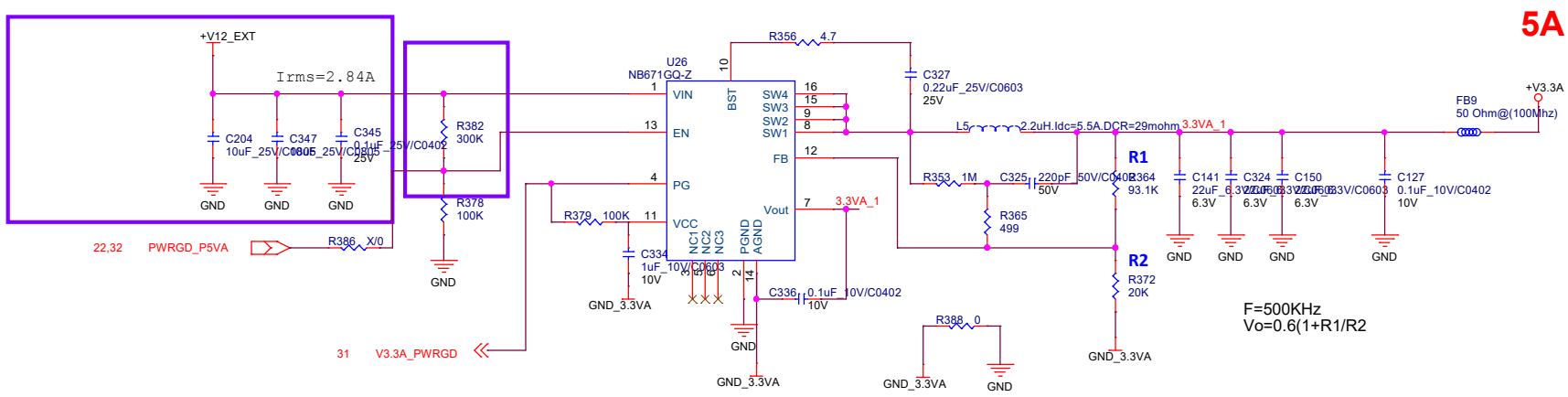
1.35V<EN<12V
EN voltage should be lower than 12V



Remove 1.5V

AAEON an ASUS assoc. co.	Title: Power VR : +V3.3A.+V1.5S	
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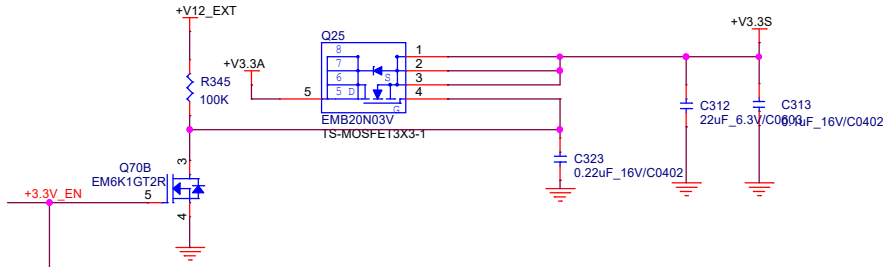
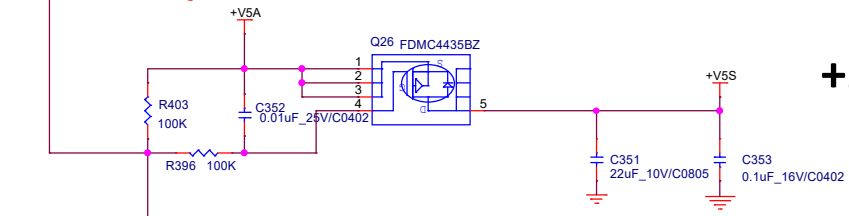
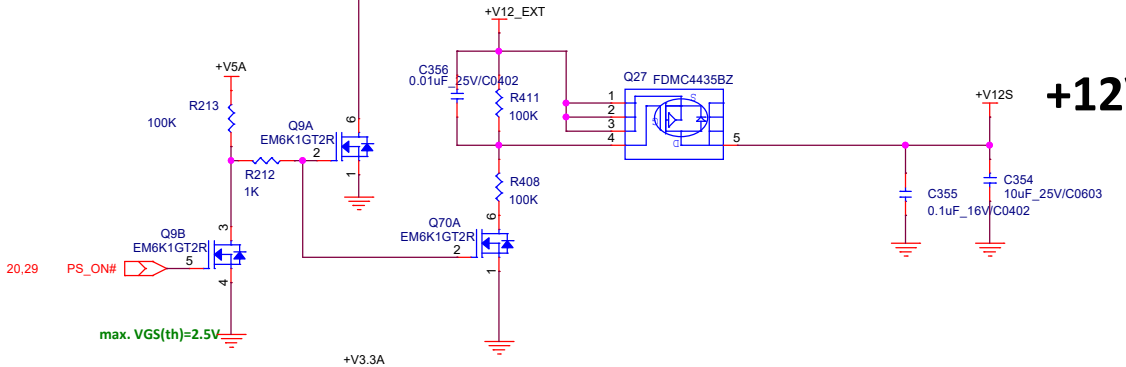
+3.3V

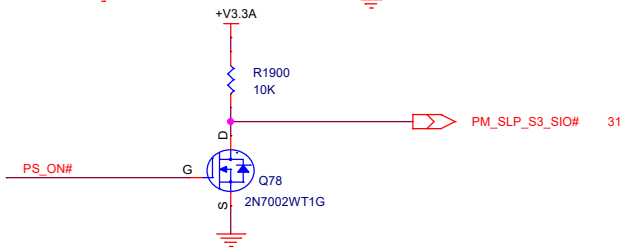


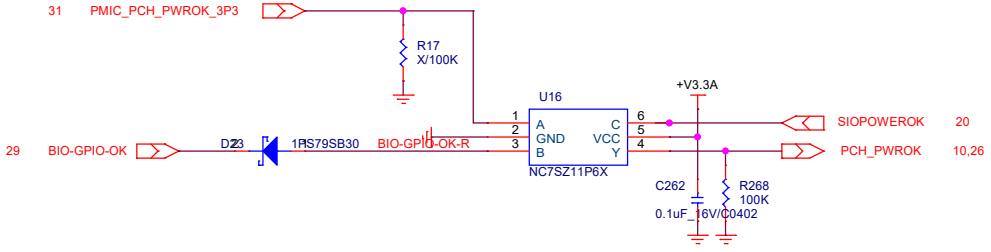
+5V

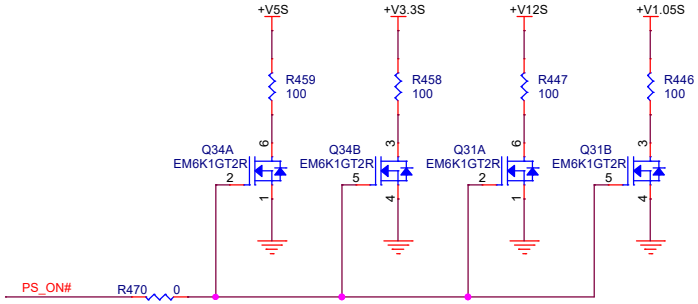


+12V









<Variant Name>

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Title: **Power Sequence Logic**

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Custom	PICOAPL1A01	A0.1

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HISTORY

Item	Date	Revision	Page	Modification List	Reason	Approve By
1	2016/12/20	A0.1	1-34	First Release.		

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Title: Revision History

Size	Document Number	Rev:
B	PICOAPL1A01	A0.1

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