<Illustration of I²C command for initialing PS8625>

1. I²C command Format :

[Slave Address, Offset, Value]

A. Write/Read Slave Address

PS8625 Device Slave address: 0x10~0x1F

0x10/0x11: Write/Read value to register at offset of **page 0**.

0x12/0x13: Write/Read value to register at offset of **page 1**.

0x14/0x15: Write/Read value to register at offset of **page 2**.

0x16/0x17: Write/Read value to register at offset of **page 3**.

0x18/0x19: Write/Read value to register at offset of **page 4**.

0x1A/0x1B: Write/Read value to register at offset of **page 5**.

0x1C/0x1D: Write/Read value to register at offset of **page 6**.

0x1E/0x1F: Write/Read value to register at offset of **page 7**.

B. Offset:

Range: 0x00 ~ 0xFF

C. Value:

Range: 0x00 ~ 0xFF

<Sample code for initialing PS8625 – compliant to PS8625 initial code Ver1.04>

```
void IICWrite(byte I2C_addr, byte reg_offset, byte data);

Wait(20ms);                 //wait 20ms then initialize PS8625 register after power on
IICWrite(0x14,0xa1,0x01);   //HPD = Low


IICWrite(0x18,0x14,0x01);
IICWrite(0x18,0xe3,0x20);
IICWrite(0x18,0xe2,0x80);
IICWrite(0x18,0x8a,0x0c);
IICWrite(0x18,0x89,0x08);
IICWrite(0x18,0x71,0x2d);
IICWrite(0x18,0x7d,0x07);
IICWrite(0x18,0x7b,0x00);
IICWrite(0x18,0x7a,0xfd);
IICWrite(0x18,0xc0,0x12);
IICWrite(0x18,0xc1,0x92);
IICWrite(0x18,0xc2,0x1c);
IICWrite(0x18,0x32,0x80);
```

```
IICWrite(0x18,0x00,0xb0);
IICWrite(0x18,0x15,0x40);
IICWrite(0x18,0x54,0x10);
IICWrite(0x10,0x52,0x20);
IICWrite(0x10,0xf1,0x03);
IICWrite(0x10,0x62,0x41);
IICWrite(0x10,0xf6,0x01);
IICWrite(0x10,0x77,0x06);
IICWrite(0x10,0x4c,0x04);
IICWrite(0x12,0xc0,0x00);
IICWrite(0x12,0xc1,0x1c);
IICWrite(0x12,0xc2,0xf8);
IICWrite(0x12,0xc3,0x44);
IICWrite(0x12,0xc4,0x32);
IICWrite(0x12,0xc5,0x44);
IICWrite(0x12,0xc6,0x4c);
IICWrite(0x12,0xc7,0x56);
IICWrite(0x12,0xc8,0x35);
IICWrite(0x12,0xca,0x01);
IICWrite(0x12,0xcb,0x04);
// --- Customized Setting (example) ---Start
IICWrite(0x12,0xa5,0xa0);     //Enable internal PWM output
IICWrite(0x12,0xa7,0xff);     //FFh for 100% PWM of brightness and 00h for 0% PWM of brightness
IICWrite(0x12,0xcc,0x10);     //Set LVDS output as 8bit-VESA mapping, single LVDS channel, this will
                              //overwrite pin configuration RLV_CFG & RLV_LNK
IICWrite(0x14,0xb1,0x20);     //Enable SSC set by register
IICWrite(0x18,0x10,0x16);     //Set SSC enabled and +/- 1% central spreading
// --- Customized Setting (example) ---End
IICWrite(0x18,0x59,0x60);
IICWrite(0x18,0x54,0x14);

IICWrite(0x14,0xa1,0x91);     //HPD = High
```

< PS8625 Customized Setting List>

PWM Control Configuration

Slave Address. Offset	Bit	Reset Value	Definition
Page1.0xa5	5	80h	PWM Select 0: Select external PWM (pass through mode) (default)

			1: Select internal PWM
Page1.0xa7	7:0	ffh	PWM Brightness for internal PWM mode, 8-bit resolution 00h = 0% brightness FFh = 100% brightness (default)
Page1.0xad	7:0	40h	PWM Frequency for internal PWM mode, 27MHz/(1024 x register value)

LVDS Output Configuration

Slave Address. Offset	Bit	Reset Value	Definition
Page1.0xcc	1:0	00h	LVDS color depth and data mapping selection 00: 8-bit LVDS, VESA mapping (default) 01: 8-bit LVDS, JEIDA mapping 10: Reserved 11: 6-bit LVDS, VESA and JEIDA mapping
	2		LVDS Link single link or dual link selection 0: Single link LVDS (default) 1: Dual link LVDS
	7:3		Reserved

LVDS Output SSC Configuration

Slave Address. Offset	Bit	Reset Value	Definition
Page2.0xb1	7:6	00h	Reserved
	5		RLV_SSC_SEL, select Spread Spectrum setting from register control 0: disable 1: enable
	4:0		Reserved
Page4.0x10	7:5	00h	Reserved
	4		Spread Spectrum enable controlled by register 0: disable 1: enable
	3:1		Spread Spectrum down depth select signal 000: +/-0.5% central spreading 001: +/-0.25% central spreading 010: +/-0.75% central spreading 011: +/-1% central spreading 100: +/-1.25% central spreading 101: +/-1.5% central spreading 110: +/-1.75% central spreading 111: +/-2% central spreading
	0		Reserved

LCD Power Sequence Timing Control

Slave Address.Offset	Bit	Reset Value	Definition
Page1.0xce	1:0	59h	LCD Power sequence T8 control 00: 10ms

			01: 20ms (default) 10: 30ms 11: 40ms
	3:2		LCD Power sequence T9 control 00: 100ms 01: 200ms 10: 250ms (default) 11: 300ms
	5:4		LCD Power sequence T10 control 00: 10ms 01: 15ms (default) 10: 20ms 11: 25ms
	7:6		LCD Power sequence T11 control 00: 5ms 01: 10ms (default) 10: 15ms 11: 20ms
Page1.0xcf	1:0	86h	LCD Power sequence T12 control 00: 100ms 01: 200ms 10: 250ms (default) 11: 300ms
	3:2		LCD Power sequence T13 control 00: 10ms 01: 20ms (default) 10: 30ms 11: 40ms
	5:4		LCD Power sequence T15 control 00: 600ms (default) 01: 700ms 10: 800ms 11: 1000ms
	6		Reserved
	7		LCD Power sequence control enable 0: Disable 1: Enable