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Project Name: NANOCOM-EHL
Version: A1.1_0_0

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34	PWR_+VCCIO / +V1P8A
35	Revision History

<Variant Name>

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Title: Cover Sheet

Size	Document Number	Rev
Custom	NANOCOM-EHL	A1.1_0_0

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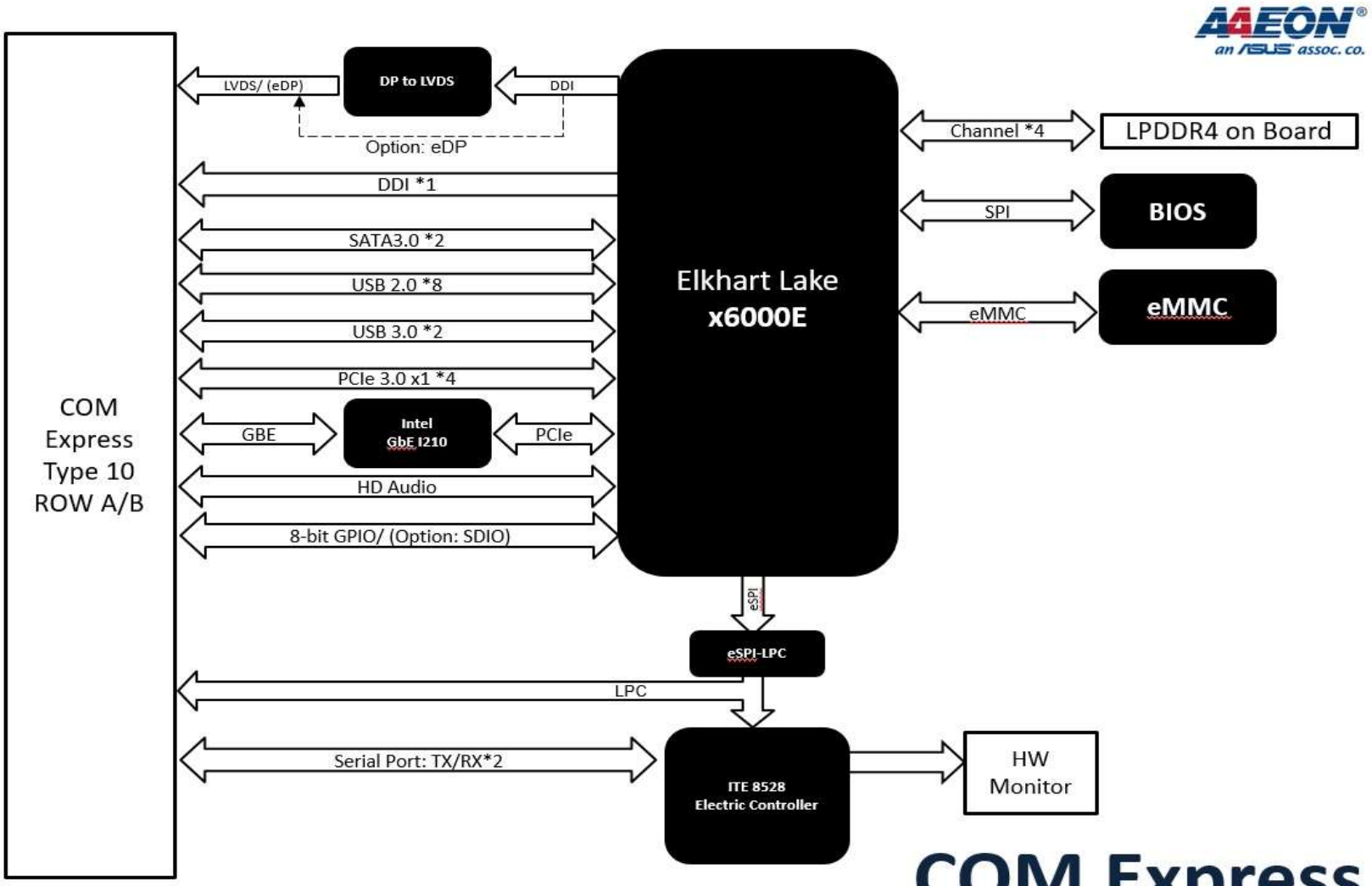
PCB STACK :

Board: FR4
Impedence 50ohm +/-10%
Thickness: 1.6mm +-10%

Layer 1 : TOP	
Layer 2 : GND	
Layer 3 : Signal	
Layer 4 : GND	
Layer 5 : Signal	
Layer 6 : Signal	
Layer 7 : Power	
Layer 8 : Power	
Layer 9 : Signal	
Layer 10 : Signal	
Layer 11 : GND	
Layer 12 : Signal	
Layer 13 : GND	
Layer 14 : BOT	



COM Express

<Variant Name>

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Title: System setting			
Size: B	Document Number: NANOCOM-EHL		Rev: A1.1_0_0
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Power Delivery

Power Connector

+5V_SBY@2A / +VIN(12V)@20A

Example:
Enable

Solution IC
Function
Power Good

5V_Dual_SW

+5V_SBY@2A
+VCC5V@6A
SY8288ARAC
DUAL MOS
VREG5_PG
+V5_DUAL@6A

+VIN

+VIN@2.96A
SY8288ARAC
DC/DC Converter
VREG5_PG
+VCC5V@6A

O_ERP_ON#(From EC)

+V5_DUAL@1.42A
SY8288ARAC
DC/DC Converter
+V3P3A_PWRGD
+V3P3A@3A

O_PS_ON(From EC)

+V3P3A@1A
NCP45520IMNTWG-H
Power Load Switch
+V3P3S_PG
+V3P3S@1A

PM_SLP_S4#

0.24A
NCP45520IMNTWG-H
Power Load Switch
+VCCST_CPU_PG
0.6A

+VCC_RTC@0.1A

+V5_DUAL@6A
XC6222B331MR-G
LDO
+V3P3A_LDO@0.1A

Elkhart Lake

VCC_OUT_FET_1P05A
+VCCST_CPU
RTC
+VCCPRIM_FIVR_1P05_SOC
+VCCPRIM_FIVR_1P05_EDGE_SOC
+VCCLDO_STD_OUT_0P85_SOC
+VCCREF_LV_SOC
+VCCSTG_OUT
VCC_OUT_1P05A
+VCCA_CLKLDO_1P8_SOC

PM_SLP_SUS#

+V5_DUAL@0.71A
SY8288ARAC
DC/DC Converter
+V1P8A_PG
+V1P8A@3A

CPU_C10_GATE_N_PM_SLP_S3#

0.2A
NCP45520IMNTWG-H
Power Load Switch
+VCCAGSH_CPU_PG
+VCCAGSH_CPU@0.2A

+V3P3A@0.2A
+V3P3A
+VCCAGSH_CPU

1.2A
+V1P8A
+VCCA_CLKLDO_1P8_SOC

+V1P8A_PG

+5V_SBY@2A
+VIN@9.64A
P-MOS
PE537BA
NCP81269MNTWG
DC/DC Converter
VCCIN_AUX_PG
+VCCIN_AUX@15A
+VCCIN_AUX

PM_SLP_S4#

+V5_DUAL@0.71A
SY8859QWC
DC/DC Converter
+VDDQ_VPP_PG
+V1.8U_MEM@1.5A

PM_SLP_S4#

+V5_DUAL@2.49A
NB685GQ-Z
DC/DC Converter
+VDDQ_PG
+VDDQ@6A

1A
Device
LPDDR4 8GB:1A

+VDDQ_PG&PM_SLP_S4#

+V5_DUAL@0.32A
TLV62084ADSGR
DC/DC Converter
+VDDQ_TX_PG
+VDDQ_TX 0.6V@1A

CPU_C10_GATE_N_PM_SLP_S3#

0.15A
NCP45520IMNTWG-H
Power Load Switch
+VCCSFR_OC_CPU_PG
+VCCSFR_OC_CPU@0.15A
+VCCSFR_OC_CPU

4.35A
+VDDQ

+VDDQ_PG&PM_SLP_S3#

+VIN@1.7A
TPS51372RJNR
DC/DC Converter
+VCCIO_PG
+VCCIO@6A
+VCCIO

ALL_SYS_PWRGD

+VIN@10A
NCP81305MNTWG
IMVP9 Controller
VR_RDY
+VCCIN@28A
+VCCIN

<Variant Name>

AAEON Technology INC.

Title: Power Delivery
Size: Custom
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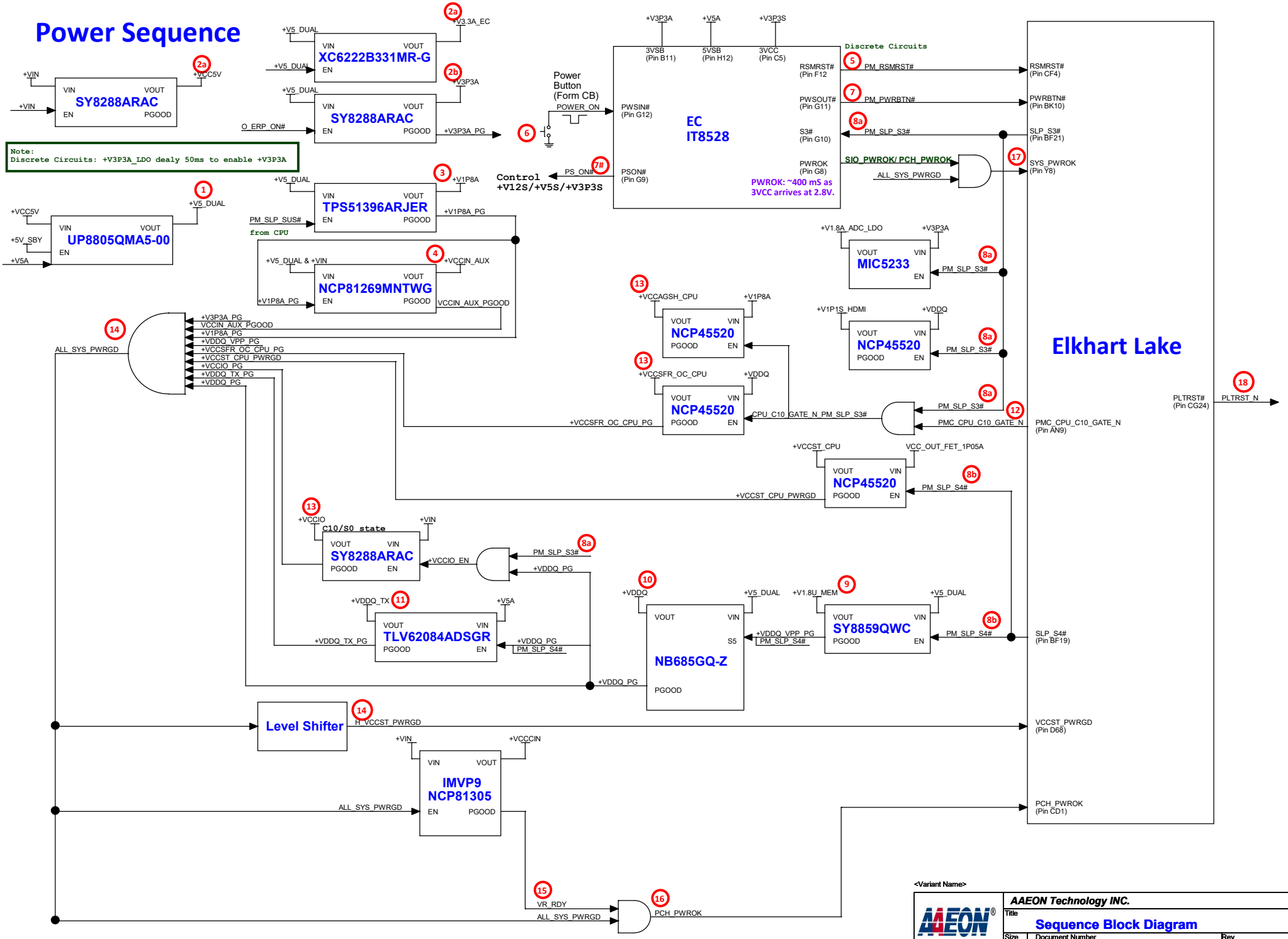
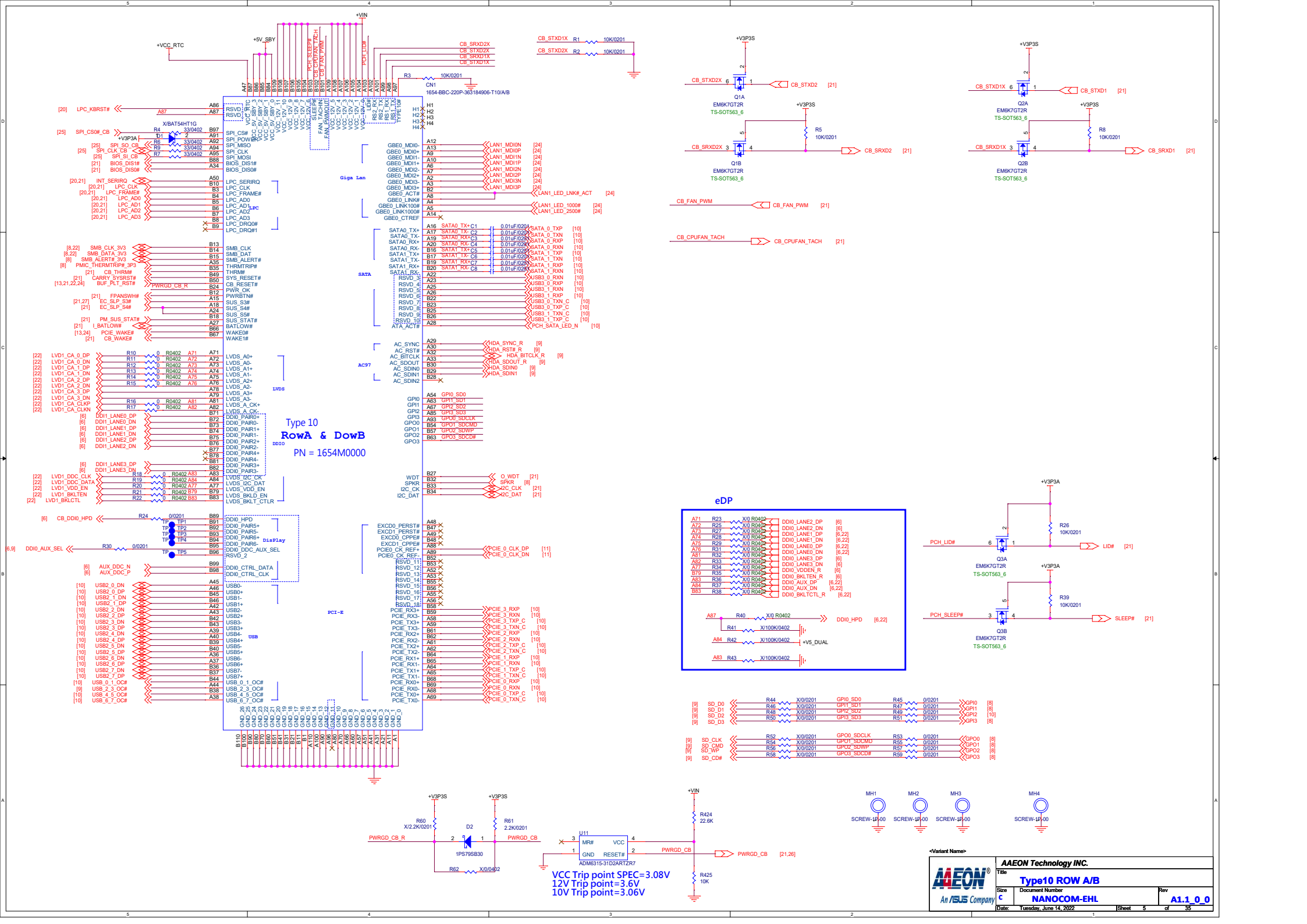
Power Sequence




Type 10
RowA & DowB
PN = 1654M0000
eDP
Giga Lan
SATA
AC97
LVDS
DDIO
DisPlay
PCI-E
USB
LPC
VCC Trip point SPEC=3.08V
12V Trip point=3.6V
10V Trip point=3.06V
AAEON Technology INC.
Type10 ROW A/B
NANOCOM-EHL
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SoC DDI

eDP/LVDS

ROWA/B

144000EHL0
(TF)INTEL CPU.Elkhart Lake .SERIES.BGA.1493P.SMD

GP_E19

GP_E19/ DDI0_DDC_SCL/ PSE_PWM13/ PSE_TGPIO24	GP_E18/ E19 pins VCC configu- ration	Rising edge of PMC_RSMRST_N	This strap has a 20 kohm ± 30% internal pull-down. 0 = GP_E18/E19 DDC pins at 1.8V 1 = GP_E18/E19 DDC pins at 3.3V **Notes:** 1. An external pull-up resistor is required if the muxed DDC signals are to be connected directly to the HDMI or DP++ connector. 2. The internal pull-down is disabled after PMC_RSMRST_N de-asserts. 3. This signal is in the primary well. 4. This strap will become RSVD in future (targeted BKC Beta release), DDC pin voltage is configurable via FIT tool soft strap.

U1A

DDI0_LANE0_DN G110 DDI0_LANE0_DP G112 DDI0_LANE1_DN J111 DDI0_LANE1_DP J109 DDI0_LANE2_DN K104 DDI0_LANE2_DP H104 DDI0_LANE3_DN P101 DDI0_LANE3_DP M101
DDI0_AUX_DN T104 DDI0_AUX_DP P104
DDI1_LANE0_DN T95 DDI1_LANE0_DP P98 DDI1_LANE1_DN F101 DDI1_LANE1_DP H101 DDI1_LANE2_DN P95 DDI1_LANE2_DP M95 DDI1_LANE3_DN K98 DDI1_LANE3_DP H98
DDI1_AUX_DN T98 DDI1_AUX_DP T101
R112 DDI2_TXN0 R110 DDI2_TXP0 W112 DDI2_TXN1 W110 DDI2_TXP1 N111 DDI2_TXN2 N109 DDI2_TXP2 L112 DDI2_TXN3 L110 DDI2_TXP3
U111 DDI2_AUXN U109 DDI2_AUXP
R78 1% 150 R0402 DDI0_RCOMP E109 DDI0_RCOMP

PNL0_BKLTCTL T2 DDI0_BKLTCTL R65 0 R0201 DDI0_BKLTCTL_R [5,22]
PNL0_BKLTEN T4 DDI0_BKLTEN R66 0 R0201 DDI0_BKLTEN_R [5]
PNL0_VDDEN U3 DDI0_VDDEN R67 0 R0201 DDI0_VDDEN_R [5]

EDP_UTILS_MDSI_DE_TE_1 D90 C103
MDSI_DE_TE_2

GP_E19_DDI0_DDC_SCL_PSE_PWM13_PSE_TGPIO24 M32
GP_E18_DDI0_DDC_SDA_PSE_PWM12_PSE_TGPIO23 H43 DDI0_CTRL_DATA
GP_E14_DDI0_HPD_PNL_MISC_DDI0_PSE_TGPIO19 K46 DDI0_HPD0

GP_E07_DDI1_DDC_SCL_CPU_GP1_PSE_TGPIO16 F36 DDI1_CTRL_CLK
GP_E05_DDI1_DDC_SDA_PSE_PWM09_PSE_TGPIO17 K36 DDI1_CTRL_DATA
GP_E03_DDI1_HPD_PNL_MISC_DDI1_CPU_GP0_PSE_TGPIO15 F39 DDI1_HPD0

GP_E23_PNL1_BKLTEN_PSE_PWM15_PSE_TGPIO19 H36
GP_E22_PNL1_BKLTCTL_PSE_PWM14_PSE_TGPIO18 H32
GP_E17_PNL1_VDDEN_PNL_MISC_DDI2_PSE_PWM11_PSE_TGPIO46 K43

14-CPU-ELKHART_LAKE-BGA1493-0
BGA1493X-35X24X2P54M

A0.4

+V3P3S
DDI0_CTRL_DATA R69 X/2.2K R0201
DDI1_CTRL_CLK R70 2.2K R0201
DDI1_CTRL_DATA R71 2.2K R0201
R72 X/10K R0201
DDI0_HPD0 R73 100K R0201
DDI1_HPD0 R74 X/100K R0201
DDI0_BKLTEN R75 X/100K R0201
DDI0_VDDEN R76 X/100K R0201

+VCC5V
Q4A
DDI0_HPD0 1 6 EM6K7GT2R TS-SOT563_6 DDI0_HPD [5,22]
R77 X/0 R0201

+VCC5V
Q4B
DDI1_HPD0 4 3 EM6K7GT2R TS-SOT563_6 CB_DDI0_HPD [5]
R79 X/0 R0201

DDI0_AUX_SEL:
H: DDC (HDMI/DVI)
L: AUX (DP/eDP)

[5,9] DDI0_AUX_SEL
+V3P3S
C9 0.1uF/6.3V

U2
DDI1_AUX_DP AUX_DDC_P C10 0.1uF C0201
DDI0_AUX_SEL
DDI1_AUX_DN AUX_DDC_N C11 0.1uF C0201
1OE 1A 1B 2OE 2A 2B GND VCC 4OE 4A 4B 3OE 3A 3B GND
DDI0_DDC_SEL DDI1_CTRL_DATA
DDI0_DDC_SEL DDI1_CTRL_CLK
14-T_C_L-74CBTLV3125BQ-0

+V3P3S
R82 100K R0201
AUX_DDC_N
AUX_DDC_N [5]

[5] AUX_DDC_P
AUX_DDC_P
R85 100K R0201

+V3P3S
R83 10K/0201
DDI0_DDC_SEL
+V3P3S
R81 10K/0201
To SOC GPI
DDC_AUX_SEL1 [12]
Q5A EM6K7GT2R TS-SOT563_6
Q5B EM6K7GT2R TS-SOT563_6
DDI0_AUX_SEL
R84 1M/0201

Must connect to SOC GPIO(Check 1.8 or 3.3V)

<Variant Name>

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Title	SoC DDI		
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SoC LPDDR4

<Variant Name>

AAEON Technology INC.

Title	SoC LPDDR4		
Size	Document Number		Rev
Custom	NANOCOM-EHL		A1.1_0_0
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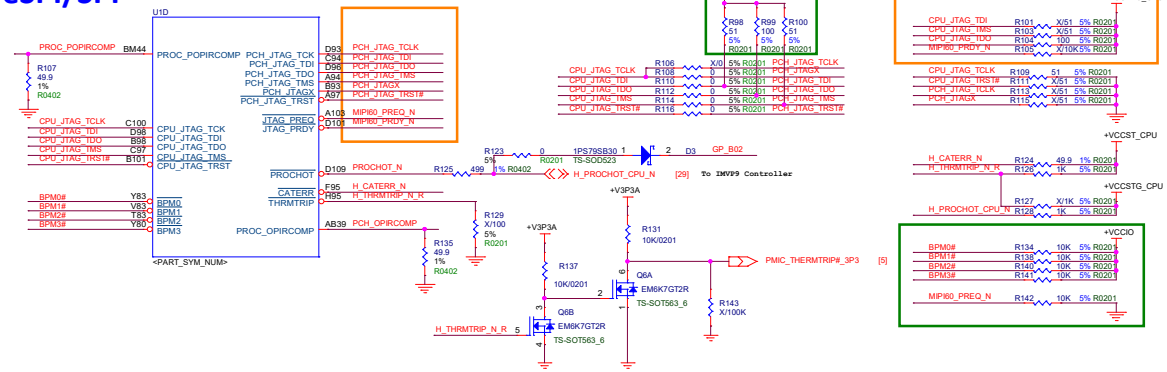
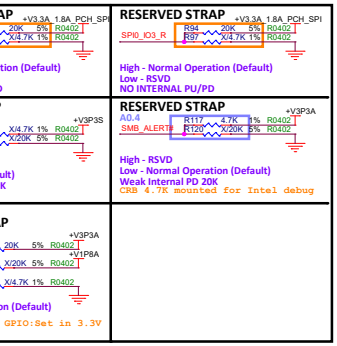
SoC JTAG/eSPI/SPI

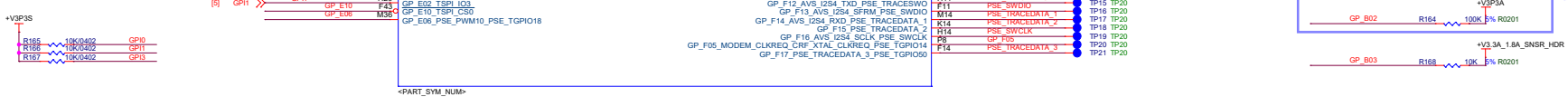




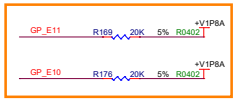
For GP_E06:
The pull-up rail will be V1P8A or V3P3A,
depending on what I/O voltage the GPIO is configured to.

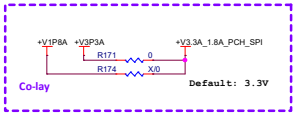
FSPI Interface supports 1.8V or 3.3V
For SPI Flash -> Default:3.3V

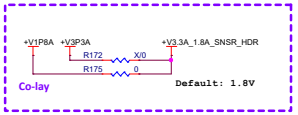
eSPI Interface supports 1.8V only



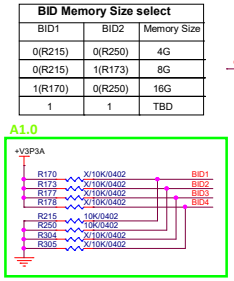
September 2021	1.6	Updated GP_D10, GP_D12, GP_E09, GP_E10, GP_E11 and GP_E21 Mixed Hardware Strap to "No"

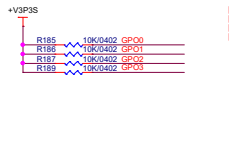


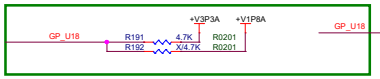


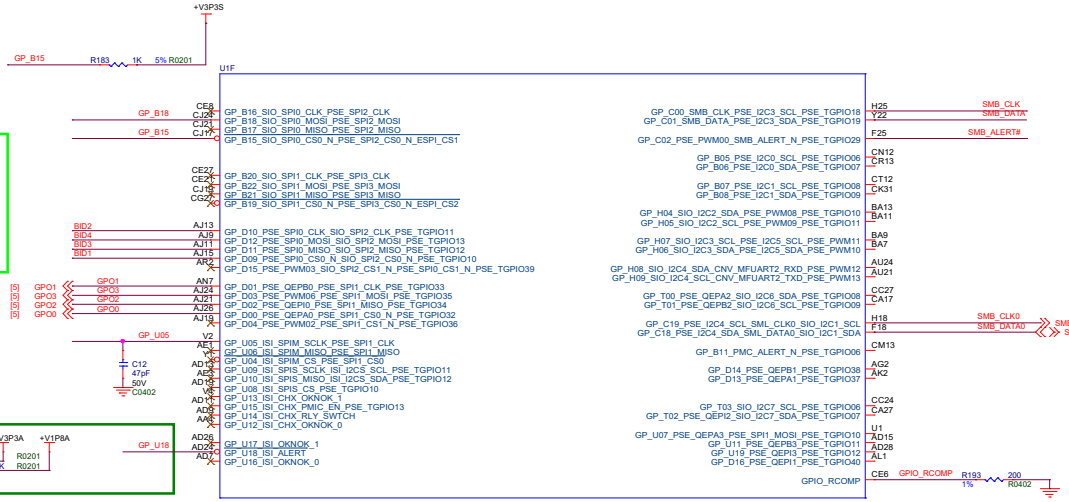


BID Memory Size select		
BID1	BID2	Memory Size
0(R215)	0(R250)	4G
0(R215)	1(R173)	8G
1(R170)	0(R250)	16G
1	1	TBD









<Variant Name>

AAEON Technology INC.		
AAEON An ASUS Company	Title: SoC JTAG/eSPI/SPI/GPIO	
	Size: Custom	Document Number: NANOCOM-EHL
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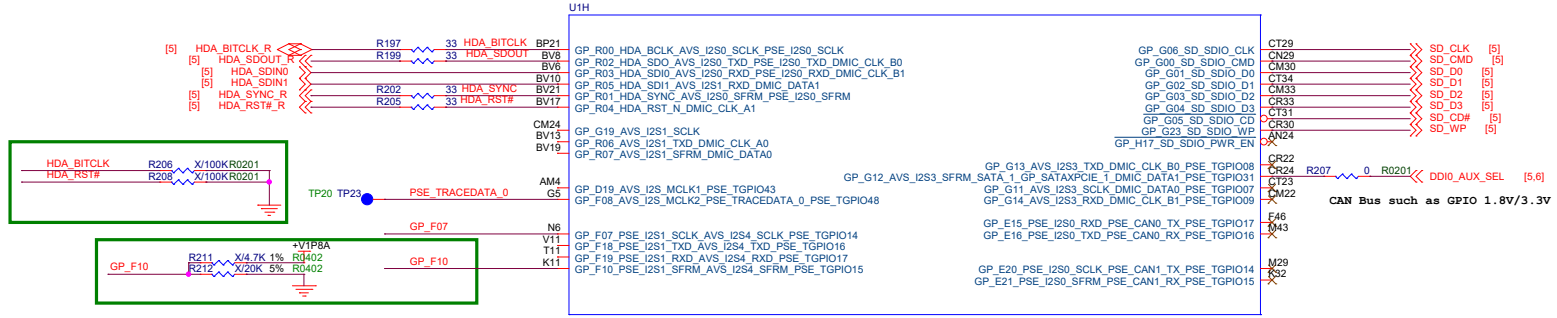
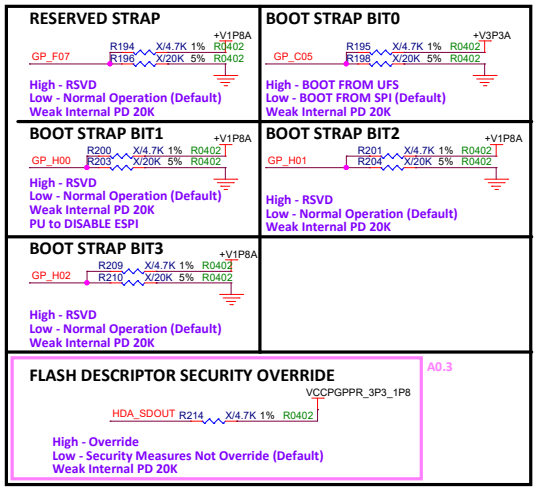
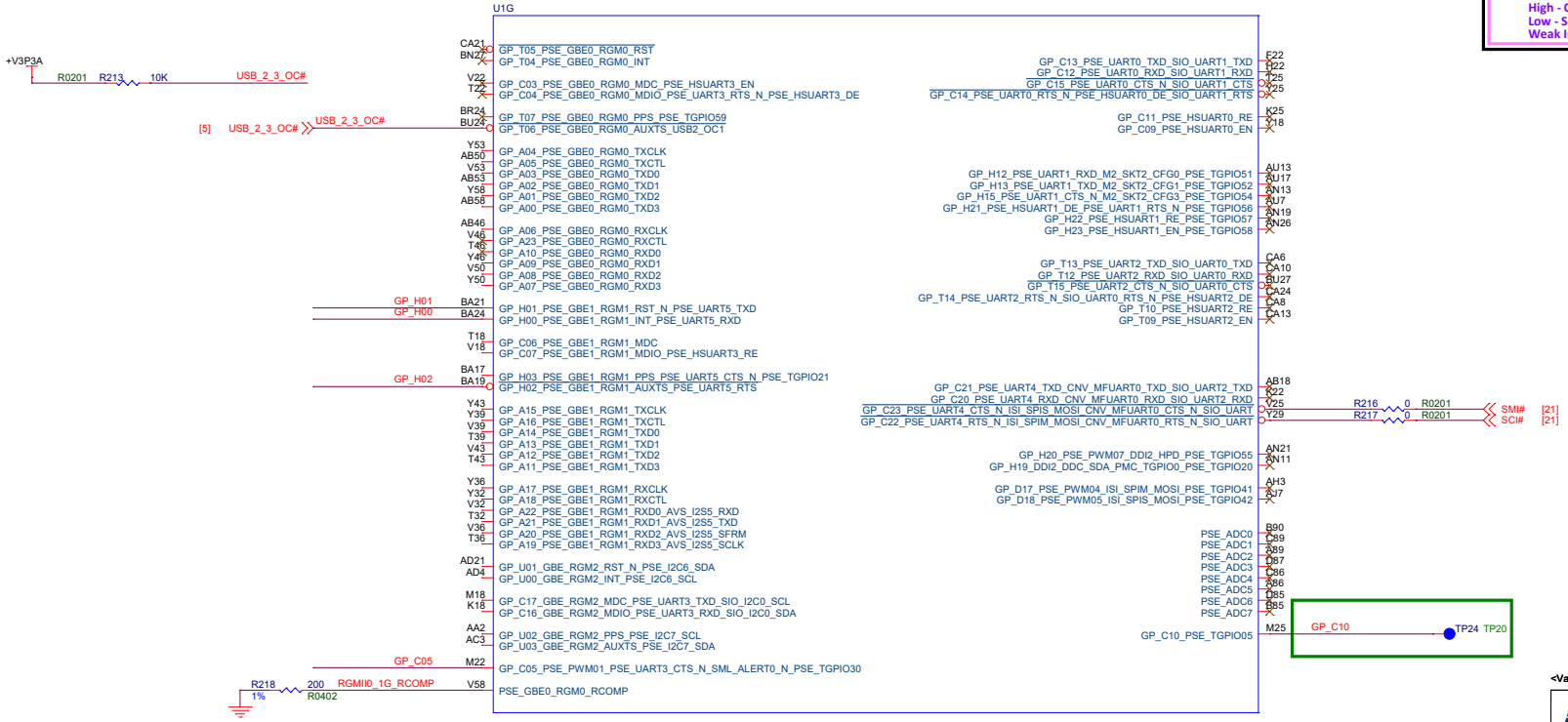
SoC HDA/CAN/RGMII







<Variant Name>

AAEON Technology INC.

Title: SoC HDA/CAN/RGMII

Size: Custom | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

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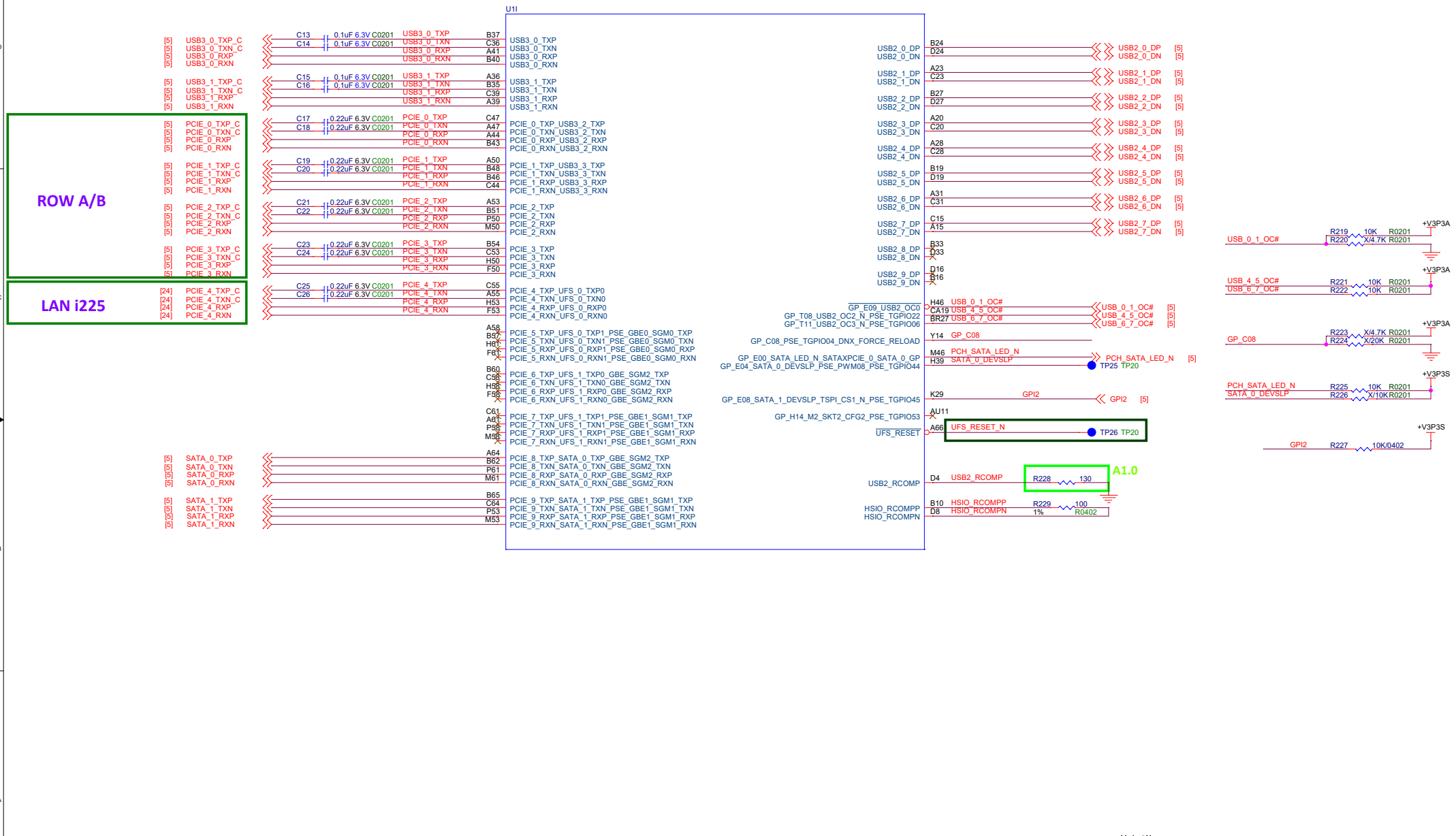
SoC PCIe/SATA/USB



<Variant Name>

AAEON Technology INC.

Title	SoC PCIe/SATA/USB	
Size: Custom	Document Number: NANOCOM-EHL	Rev: A1.1_0_0
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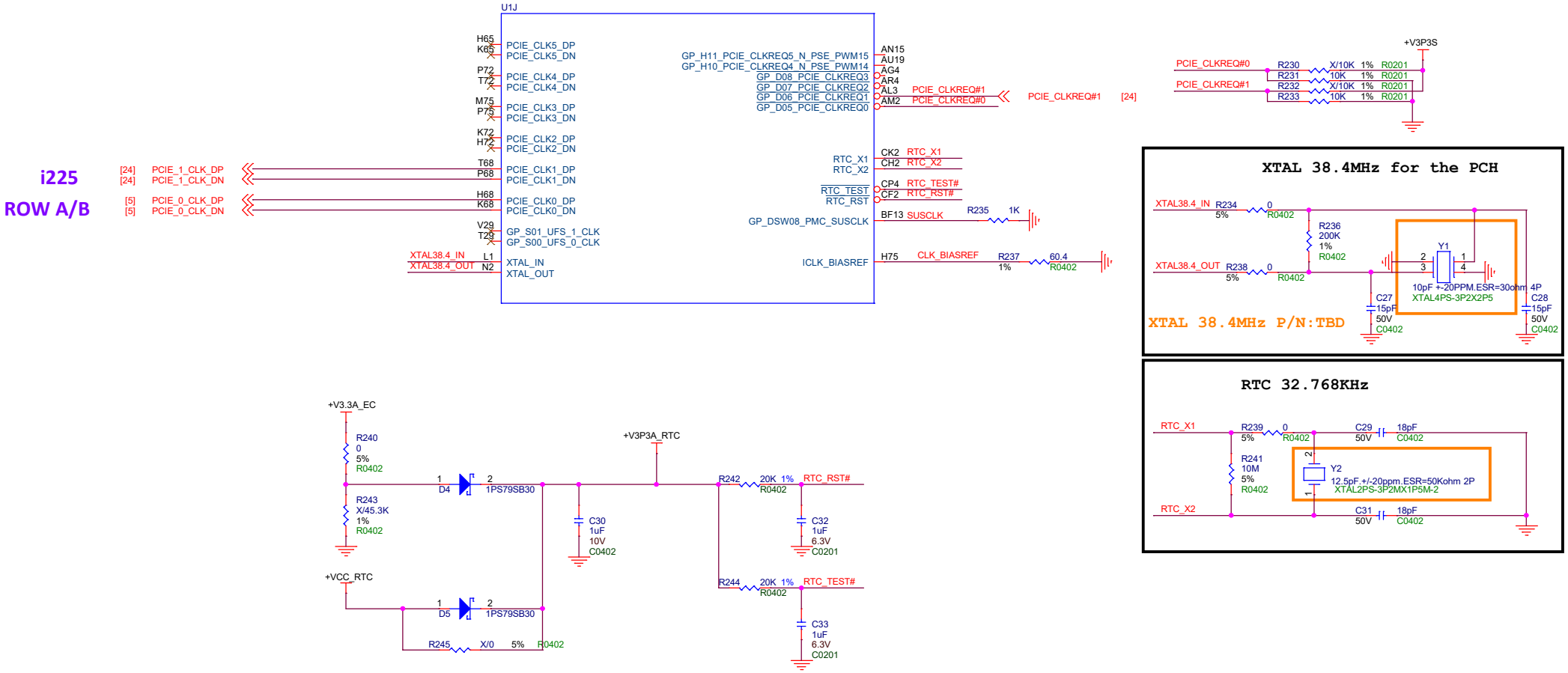
SoC PCIE_CLK/ RTC



<Variant Name>

AAEON Technology INC.

Title	SoC PCIE_CLK/ RTC		
Size: Custom	Document Number: NANOCOM-EHL		Rev: A1.1_0_0
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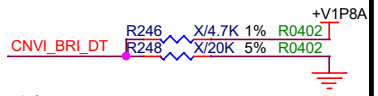
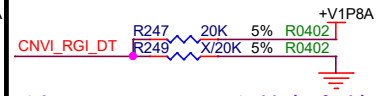
SoC eMMC/CNVI

RESERVED STRAP



High - RSVD
Low - Normal Operation (Default)
Weak Internal PD 20K

M.2 CNVI MODE



High - INTEGRATED CNVI Disable (Default)
Low - INTEGRATED CNVI Enable
NO Internal PU/PD

U1K

CC4 CNV_WT_CLKP
CC2 CNV_WT_CLKN
BW1 CNV_WT_D0P
BW3 CNV_WT_D0N
CB3 CNV_WT_D1P
BY2 CNV_WT_D1N
BR2 CNV_WR_CLKP
BT3 CNV_WR_CLKN
BU2 CNV_WR_D0P
BU4 CNV_WR_D0N
BN1 CNV_WR_D1P
BN3 CNV_WR_D1N
CB1 CNV_WT_RCOMP
CT26 GP_G07_AVS_I2S2_SCLK_DMIC_CLK_A0
CT20 GP_G09_AVS_I2S2_TXD_MODEM_CLKREQ_CRF_XTAL_CLKREQ_DMIC_CLK_A1
CN26 GP_G10_AVS_I2S2_RXD_DMIC_DATA1
CR27 GP_G08_AVS_I2S2_SFRM_CNV_RF_RESET_N_DMIC_DATA0
Y11 GP_F04_CNV_RF_RESET
AT3 GP_V12_PSE_TGPIO00
AV4 GP_V13_PSE_TGPIO01
AT1 GP_V14_PSE_TGPIO02
BA4 GP_V15_PSE_TGPIO03

GP_V10_EMMC_CLK BF2 EMMC0_CLK [23]
GP_V09_EMMC_RCLK BJ4 EMMC0_STROBE [23]
GP_V01_EMMC_DATA0 BB3 EMMC0_D0 [23]
GP_V02_EMMC_DATA1 BE1 EMMC0_D1 [23]
GP_V03_EMMC_DATA2 BH3 EMMC0_D2 [23]
GP_V04_EMMC_DATA3 BA2 EMMC0_D3 [23]
GP_V05_EMMC_DATA4 BE3 EMMC0_D4 [23]
GP_V06_EMMC_DATA5 BK3 EMMC0_D5 [23]
GP_V07_EMMC_DATA6 BC2 EMMC0_D6 [23]
GP_V08_EMMC_DATA7 BC4 EMMC0_D7 [23]
GP_V00_EMMC_CMD BH1 EMMC0_CMD [23]
GP_V11_EMMC_RST AV2 EMMC0_RST_N [23]

eMMC impedance 50ohm

EMMC_RCOMP BM4 EMMC_RCOMP R251 1% 200 R0402

GP_F00_CNV_BRI_DT_SIO_UART0_RTS V14 CNVI_BRI_DT
GP_F01_CNV_BRI_RSP_SIO_UART0_RXD H8
GP_F02_CNV_RPSE_DT_SIO_UART0_TXD E4 CNVI_RGI_DT
GP_F03_CNV_RPSE_RSP_SIO_UART0_CTS V8
GP_F06_CNV_PA_BLANKING_PSE_TGPIO47 U6 DDC_AUX_SEL1 [6]

<Variant Name>

AAEON Technology INC.

Title	SoC eMMC/CNVI		
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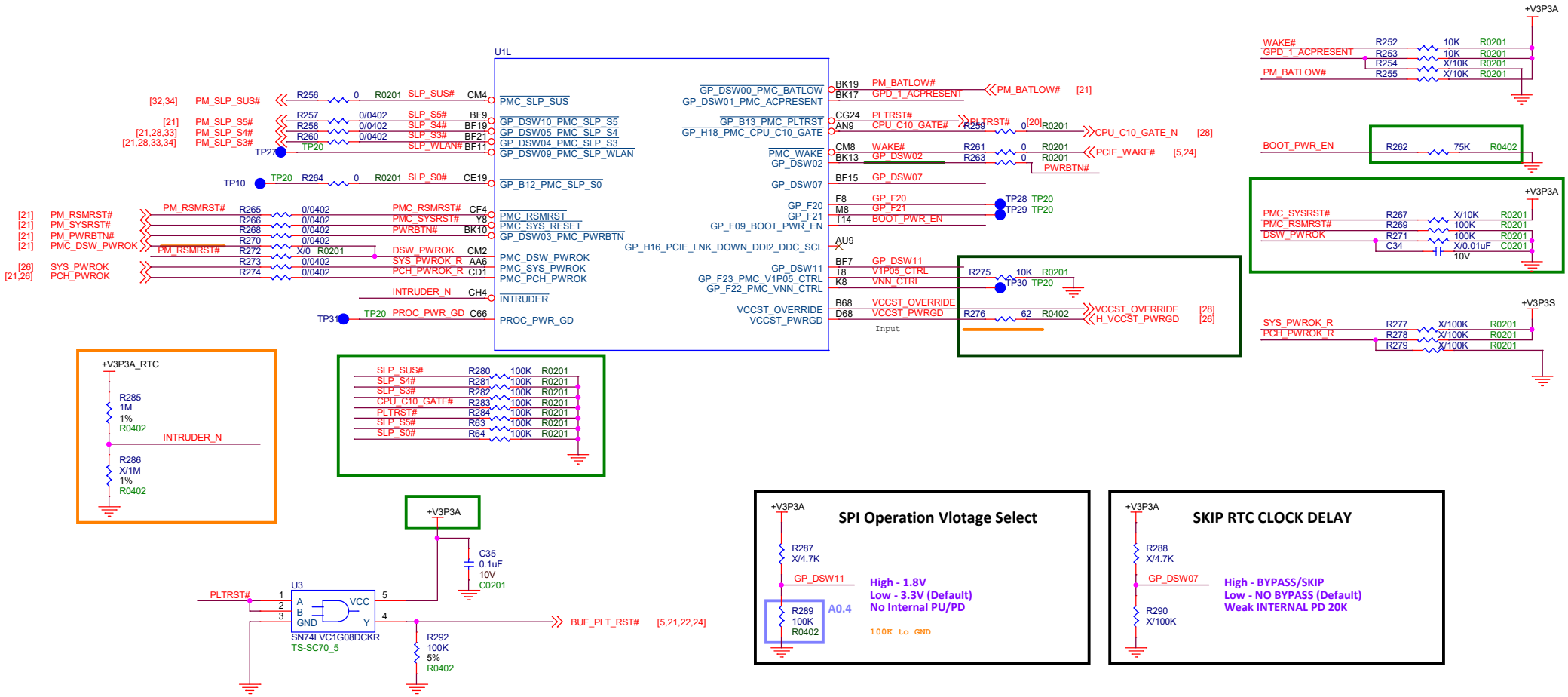
SoC System



<Variant Name>

AAEON Technology INC.

Title: SoC System

Size	Document Number	Rev
Custom	NANOCOM-EHL	A1.1_0_0

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SoC Power

28A

5.5A

6.5A

Place the PU resistors close to CPU

+VCCST_CPU

R294 56 1% R0402

R295 X/45.3 1% R0402

R296 100 1% R0402

VCCIN_SVIDALERT_N

VCCIN_SVIDSCK

VCCIN_SVIDSCOUT

U1M

U1N

+VCCIN

+VDDQ

+VCCIO

+VCCSFR_OC_CPU

+VCCSFR_CPU

+VCCST_CPU

+VCCAGSH_CPU

+VCCSTG_CPU

0.1A

0.6A

0.2A

0.1A

0.12A

A0.3

VCC_OUT_1P05A

VCC_OUT_FET_1P05A

R297 0 R0402

[29] VCCIN_SVIDSCK

[29] VCCIN_SVIDSCOUT

[29] VCCIN_SVIDALERT_N

SVID_CLK

SVID_DATA

SVID_ALERT

VCCIN_SENSE

VSSIN_SENSE

VCCIN_SENSE_DP [29]

VCCIN_SENSE_DN [29]

VCCIO_SENSE_DP [34]

VCCIO_SENSE_DN [34]

+VCCIN 28A

C53 330uF 2.5V TC-3P5X2P8X1P9M 330uF x 1

47uF x 8

22uF x 19

10uF x 4

1uF x 6

12pF x 12

+VCCIO 6.5A

100uF x 3

47uF x 4

22uF x 4

+VDDQ 5.5A

22uF x 5

10uF x 12

1uF x 18

0.1uF x 1

12pF x 3

<Variant Name>

AAEON Technology INC.

Title: SoC Power

Size: Custom | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

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PCH Power

+VCCIN_AUX **15A Max**

C150 330uF 2.5V TC-3P5X2P8X1P9M — **330uF x 1**

closed to C6F4 & C6E34

+VCCIN_AUX

C153–C161 47uF 6.3V C0603 — **47uF x 18**

C168–C176 47uF 6.3V C0603

C177–C188 10uF 6.3V C0402 — **10uF x 36**

C193–C204 10uF 6.3V C0402

C205–C216 10uF 6.3V C0402

C220–C226 1uF 6.3V C0201 — **1uF x 7**

C230–C239 12pF 25V C0201 — **12pF x 10**

15A Max

U1O

+VCCIN_AUX → VCCIN_AUX_1 … VCCIN_AUX_42

[31] VCCIN_AUX_VCCSENSE → AR59 VCCIN_AUX_VCCSENSE

[31] VCCIN_AUX_VSSSENSE → AV59 VCCIN_AUX_VSSSENSE

[31] VCCIN_AUX_VID0 → CE24 GP_B00_PMC_CORE_VID0

[31] VCCIN_AUX_VID1 → CE13 GP_B01_PMC_CORE_VID1

AH1 VCC_OUT_0P85A

+V3P3A **0.004A** — R300 0 R0402 — VCC_3P3A_DSW → BF28 VCC_3P3A_DSW_1, BF30 VCC_3P3A_DSW_2

+V3.3A_EC — R302 X/0 R0402

C228 1uF 6.3V C0201

AD37, AD40 VCC_ADC_1P8A_1, VCC_ADC_1P8A_2

+VCCA_CLKLDO_1P8_SOC → VCCA_CLKLDO_1P8 AC1

+V1P8A **2.17A** → VCC_1P8A_1 … VCC_1P8A_12 (AD32, AF32, AF35, AJ30, AJ32, AJ35, AJ37, AL32, AL35, AL37, AN35, AN37)

+V3P3A **0.202A** → VCC_3P3A_1 … VCC_3P3A_12 (AN30, AR32, AR35, AT36, AU28, AU30, AV32, AV35, AV32, AV35, BB35, BB37)

VCC_OUT_FET_1P05A → VCC_OUT_FET_1P05A_1 … VCC_OUT_FET_1P05A_5 (AB61, V65, Y61, V61, Y65) Output **1A**

VCC_OUT_1P05A → VCC_OUT_1P05A_1 … VCC_OUT_1P05A_7 (AJ43, AJ46, AL46, BF32, BH32, BK30, BM30) **1A**

+VCCDSW_1P05_SOC → VCCDSW_OUT_1P05 BK1

+VCCSTG_OUT **1A** Output → VCC_OUT_STG_1 A80, VCC_OUT_STG_2 C80

VCC_BYP_1P05 AY37 **0.2A**

VCC_BYP_VNN_1 BD35, VCC_BYP_VNN_2 BF35 **0.2A**

+VCCPHY_1P24_SOC → VCC_OUT_1P24A AP1

VCCPGPPR_3P3_1P8 → VCC_PGPPR_1 BA28, VCC_PGPPR_2 BA30 **0.005A**

+V3P3A_RTC → VCC_RTC_3P3 AW1 **0.002A**

+VCC_RTC_EXT_SOC → VCC_RTC_EXT CR10

+VCCREF_LV_SOC → VCC_OUT_ADC_LV_1 AB32, VCC_OUT_ADC_LV_2 AB36

C240 10uF 6.3V C0402

+V1P8A — R298 0 R0402 — +VCCA_CLKLDO_1P8_SOC

C151 47uF 6.3V C0603, C152 1uF 6.3V C0201

+V1P8A: C162 10uF 6.3V C0402, C163 10uF 6.3V C0402, C164 1uF 6.3V C0201

+V3P3A: C165 10uF 6.3V C0402, C166 1uF 6.3V C0201, C167 0.1uF 6.3V C0201

VCC_OUT_FET_1P05A: C189 10uF 6.3V C0402, C190 1uF 6.3V C0201

+VCCDSW_1P05_SOC: C191 10uF 6.3V C0402

+VCCDPHY_1P24_SOC: C192 4.7uF 6.3V C0402

+V3P3A — R299 0 R0201 — VCCPGPPR_3P3_1P8

Audio Voltage 3.3V[COMe]

+V3P3A_RTC: C217 1uF 6.3V C0201, C218 0.1uF 6.3V C0201

+VCC_RTC_EXT_SOC: C219 1uF 6.3V C0201

+VCCSTG_OUT — R301 0 R0402 — +VCCSTG_CPU **0.12A**

C229 1uF 6.3V C0201

+VCCDPHY_1P24_SOC: C241 47uF 6.3V C0603

VCC_OUT_1P05A: C242 10uF 6.3V C0402

+VCCDSW_1P05_SOC: C243 10uF 6.3V C0402

+VCCPRIM_FIVR_1P05_SOC: C244 1uF 6.3V C0201

+VCCPRIM_FIVR_1P05_EDGE_SOC: C245 1uF 6.3V C0201, C246 1uF 6.3V C0201

U1S

+VCCPRIM_FIVR_1P05_SOC → VCC_OUT_FIVR_1P05A_1 … VCC_OUT_FIVR_1P05A_5 (AD46, AF46, AF48, AJ48, AJ50, AL48, AL50)

+VCCPRIM_FIVR_1P05_EDGE_SOC → VCC_OUT_FIVR_1P05A_6 … VCC_OUT_FIVR_1P05A_10 (B76, C78, D79)

Note:
ISOLATE INNER AND EDGE BGA FOR VCCPRIM_FIVR_1P05

<Variant Name>

AAEON Technology INC.

Title: PCH Power

Size: Custom | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

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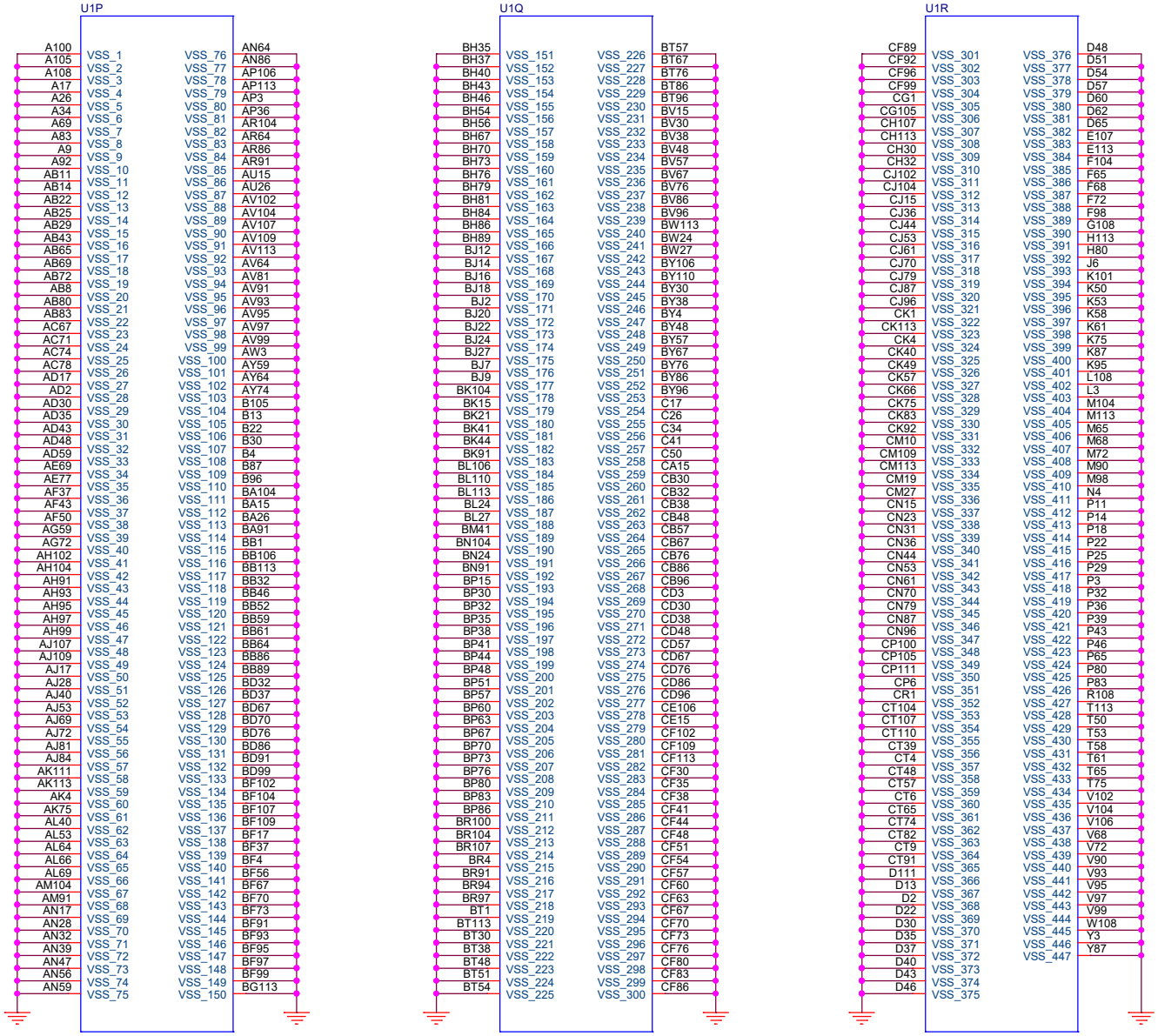
SoC GND



<Variant Name>

AAEON Technology INC.

An ASUS Company

Title	SoC GND		
Size	Document Number		Rev
B	NANOCOM-EHL		A1.1_0_0
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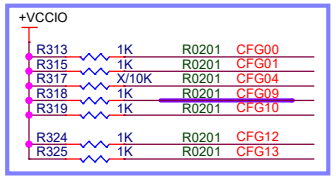
SoC Strap

A0.4

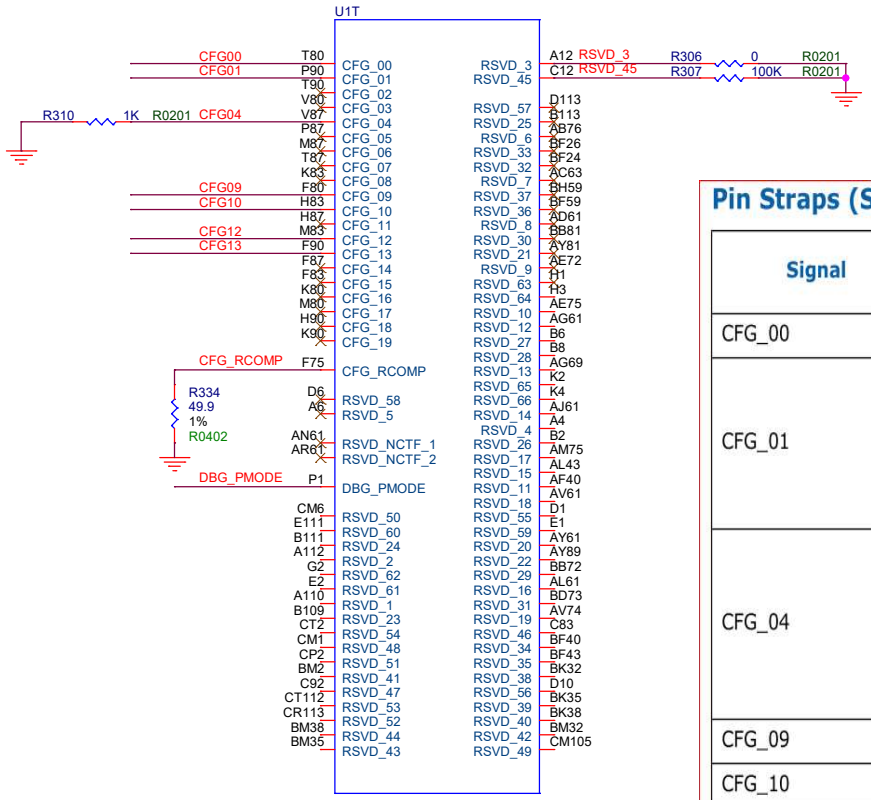
Co-lay

0/1/4/9-13 pull high to VCCIO & GND co-lay

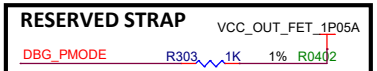


Follow PDG and not as same as CRB

R754,R743 from 10 K to 1K A0.4



RESERVED STRAP



High - Default
Weak Internal PU 20K
This strap shuld sample high

Pin Straps (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
CFG_00	Reserved	Between PMC_P-CH_PWROK assertion & PMC_PLTRST_N de-assertion	External pull-up is required. Recommend 10kΩ to VCCIO.
CFG_01	Reserved		This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
CFG_04	eDP Enable		0 = Enable eDP interface. External pull-down is required. Recommend 1kΩ to GND. 1 = Disable eDP interface. External pull-up is required. Recommend 10kΩ to VCCIO.
CFG_09	Reserved		External pull-up is required. Recommend 10kΩ to VCCIO.
CFG_10	Reserved		
CFG_11	Reserved		This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
CFG_12	Reserved		
CFG_13	Reserved		

CFG_00	Reserved	Between PMC_P-CH_PWROK assertion & PMC_PLTRST_N de-assertion	External pull-up is required. Recommend 1kΩ to VCCIO.
CFG_01	Reserved		This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
CFG_09	Reserved		
CFG_10	Reserved		
CFG_12	Reserved		
CFG_13	Reserved		

<Variant Name>

AAEON® An ASUS Company

AAEON Technology INC.

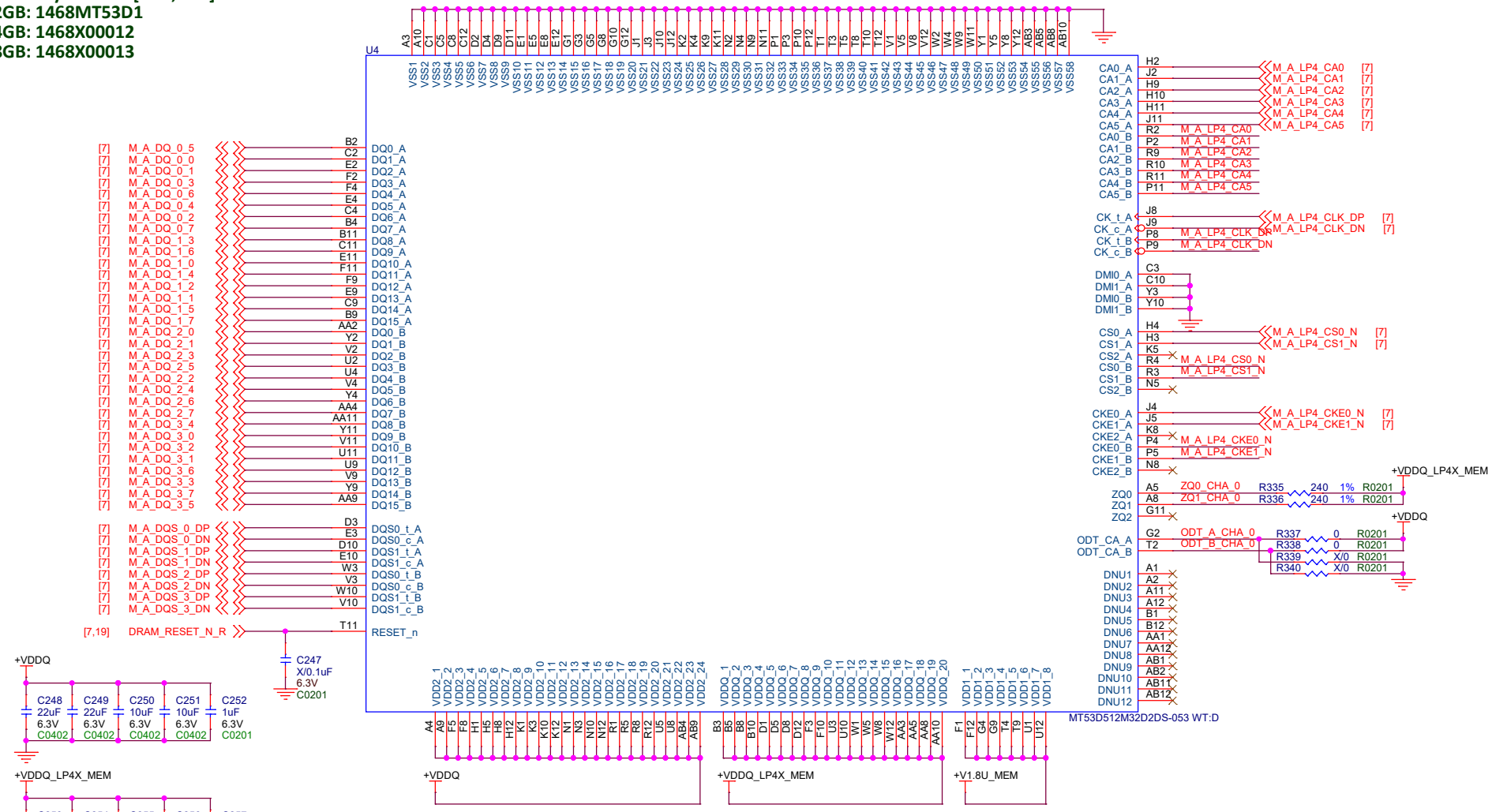
Title: SoC Strap

Size: B | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

Date: Tuesday, June 14, 2022 | Sheet 17 of 35

LPDDR4 CHA

Memory: Micron [U45,U41]
2GB: 1468MT53D1
4GB: 1468X00012
8GB: 1468X00013



<Variant Name>

AAEON Technology INC.			
Title: LPDDR4 CHA			
Size: B	Document Number: NANOCOM-EHL		Rev: A1.1_0_0
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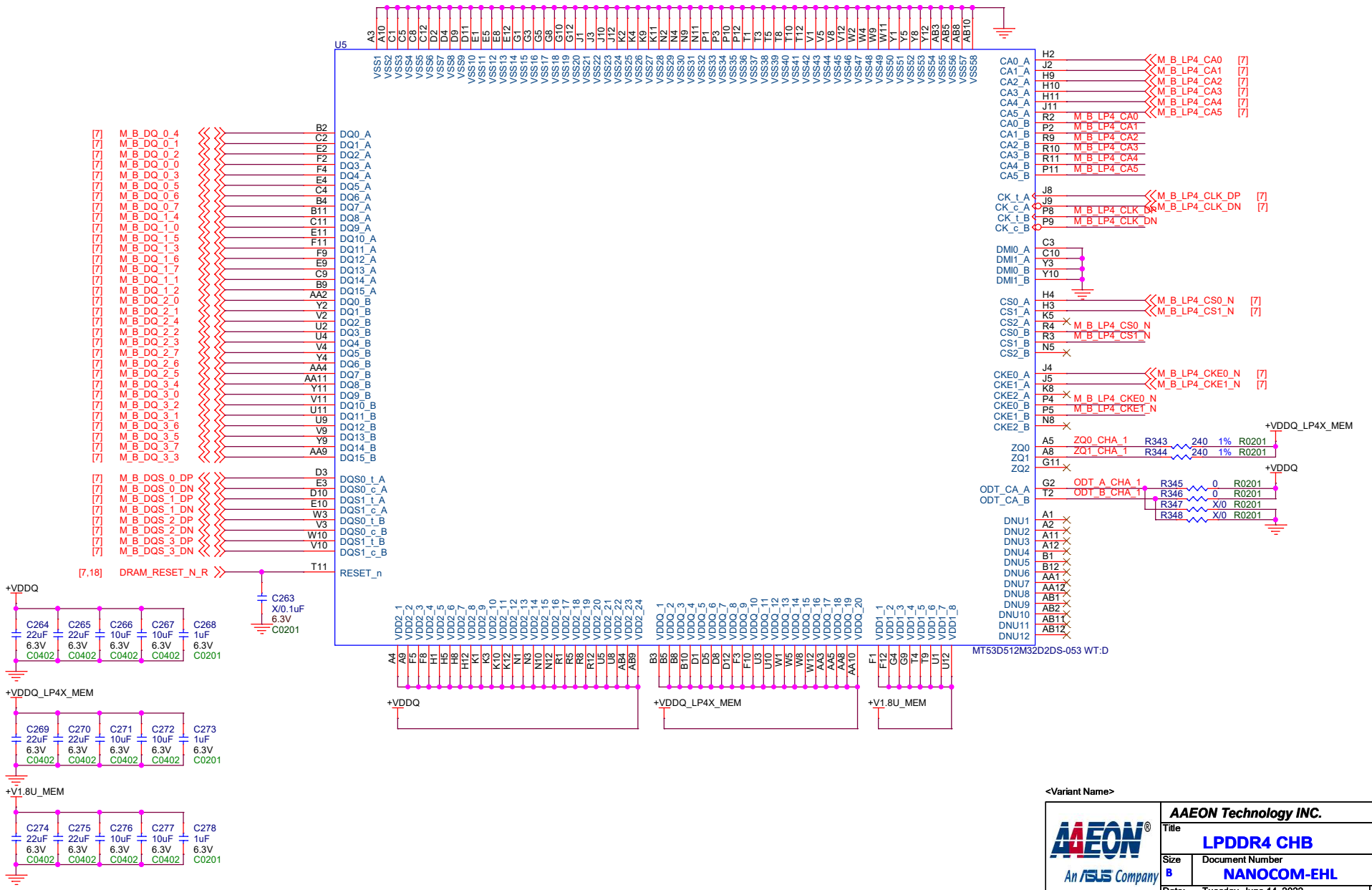
LPDDR4 CHB



<Variant Name>

AAEON Technology INC.

Title	LPDDR4 CHB		
Size B	Document Number NANOCOM-EHL		Rev A1.1_0_0
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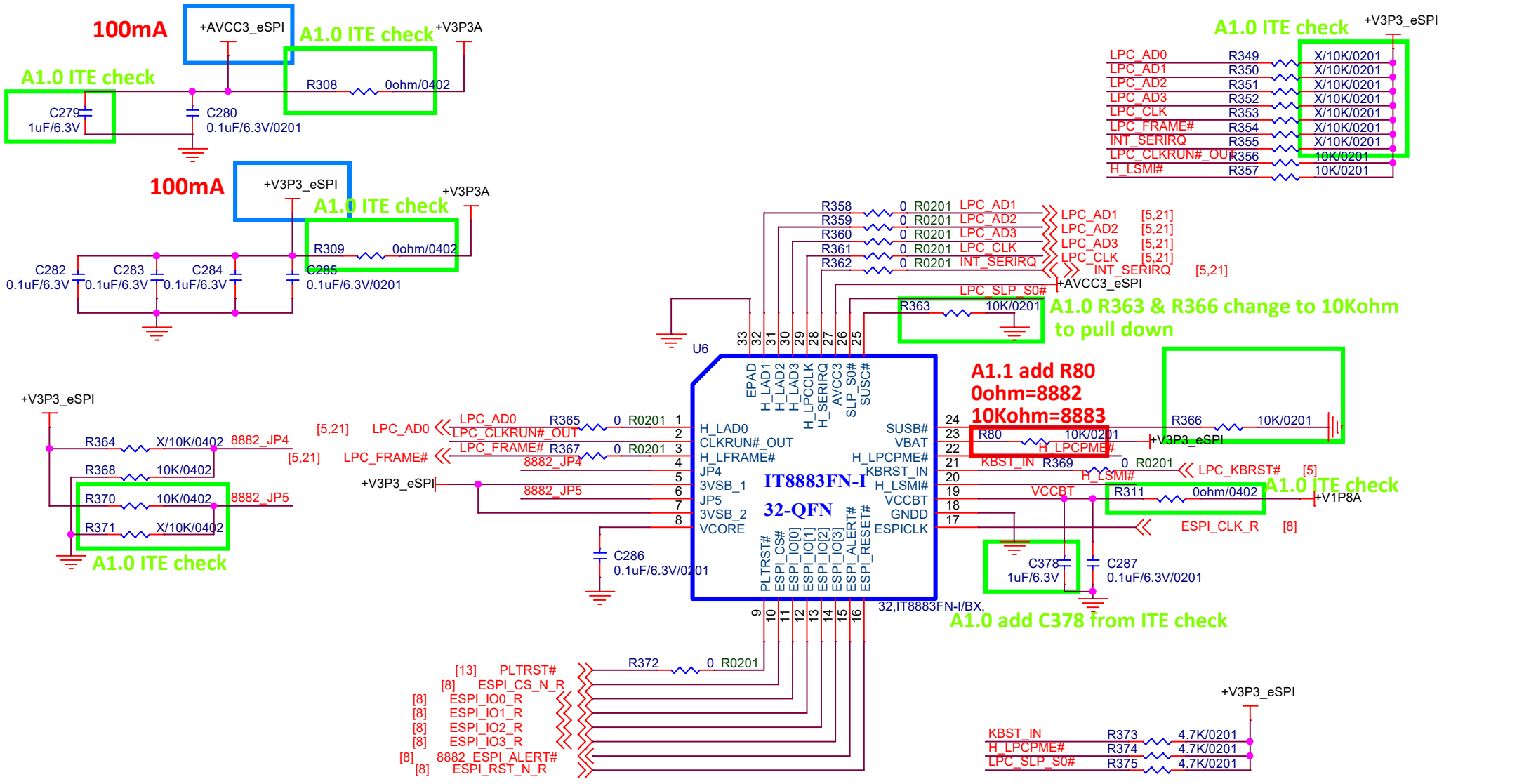

• Power-On Strapping

	Symbol	Value	Description
JP4	Enter key	1	2E/2F (87 01 55 55)
Pin-4		0	4E/4F (87 01 55 AA)*
JP5	CHIP_SEL	1	Chip selection
Pin-6		0	Chip selection*

<Variant Name>

AAEON Technology INC.

Title: eSPI to LPC_IT8882

Size: Custom | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

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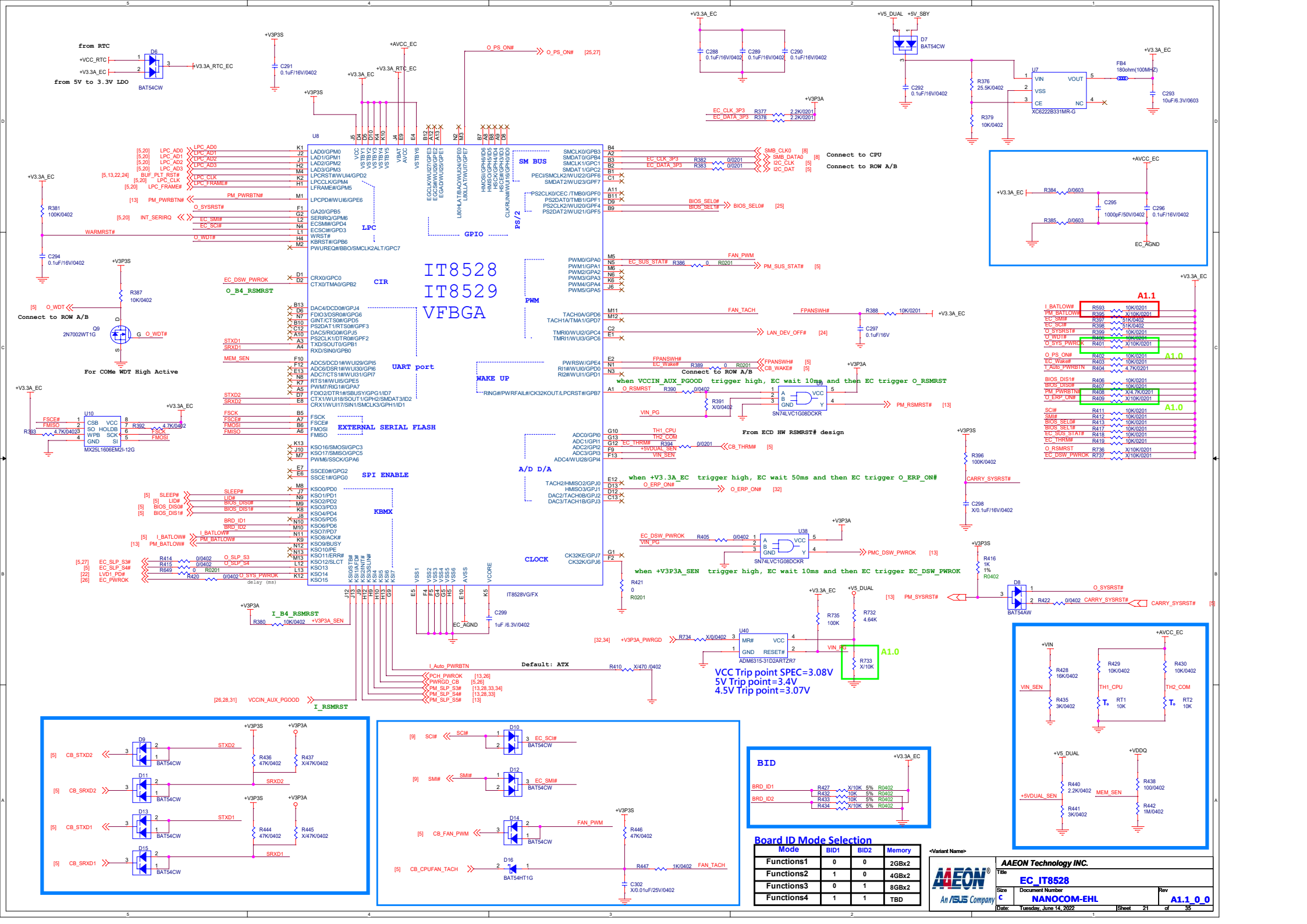
IT8528
IT8529
VFBGA
IT8528VG/FX
SM BUS
PS/2
LPC
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Connect to CPU
Connect to ROW A/B
Connect to ROW A/B
Connect to ROW A/B
O_B4_RSMRST
For COMe WDT High Active
when VCCIN_AUX_PGOOD trigger high, EC wait 10ms and then EC trigger O_RSMRST
From ECD HW RSMRST# design
when +V3.3A_EC trigger high, EC wait 50ms and then EC trigger O_ERP_ON#
when +V3P3A_SEN trigger high, EC wait 10ms and then EC trigger EC_DSW_PWROK
Default: ATX
I_B4_RSMRST
I_RSMRST
VCC Trip point SPEC=3.08V
5V Trip point=3.4V
4.5V Trip point=3.07V
A1.1
A1.0
A1.0
BID
Board ID Mode Selection
Mode | BID1 | BID2 | Memory
Functions1 | 0 | 0 | 2GBx2
Functions2 | 1 | 0 | 4GBx2
Functions3 | 0 | 1 | 8GBx2
Functions4 | 1 | 1 | TBD
AAEON Technology INC.
EC_IT8528
NANOCOM-EHL
A1.1_0_0
Tuesday, June 14, 2022
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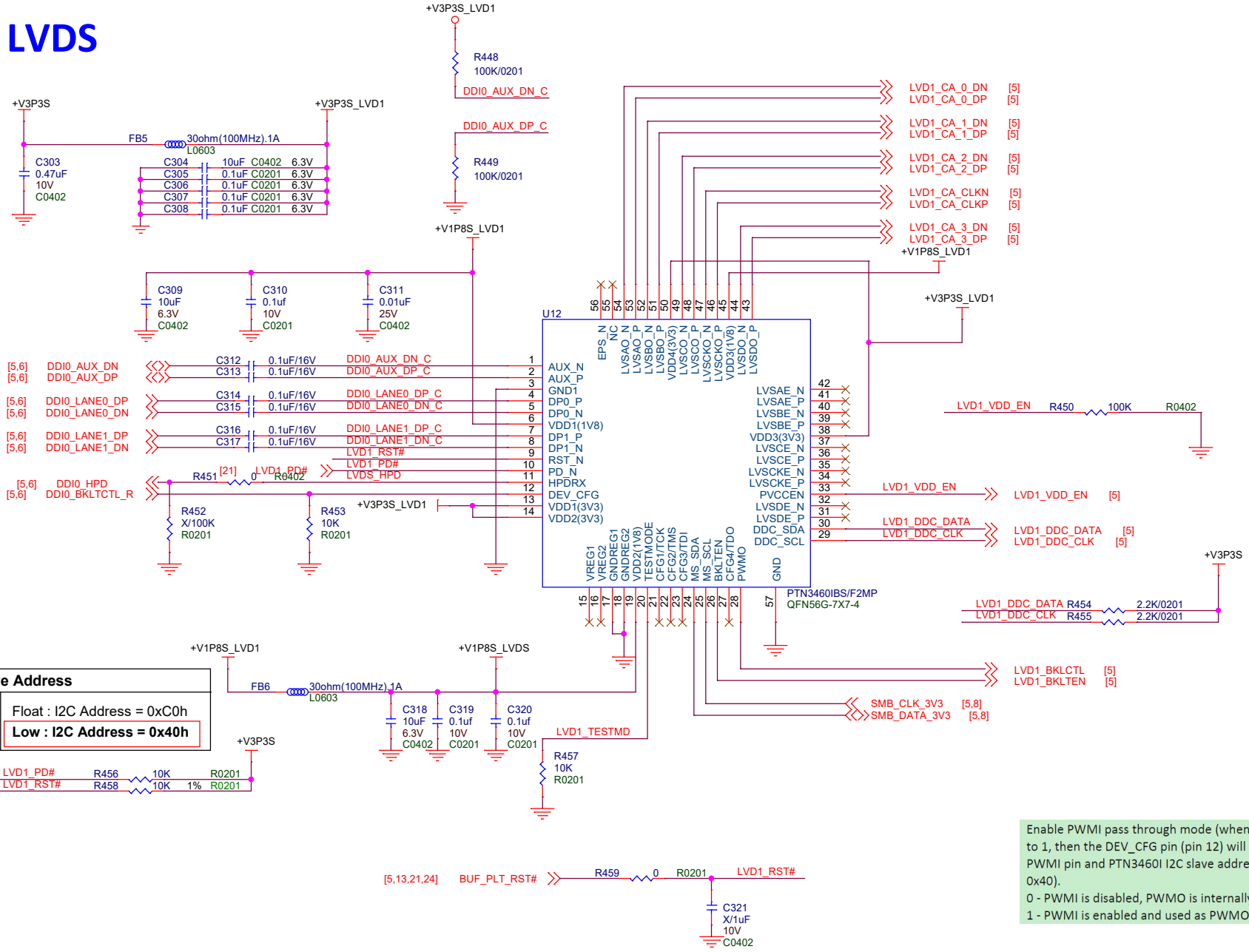
LVDS



I2C Slave Address	
DEV_CFG	Float : I2C Address = 0xC0h
	Low : I2C Address = 0x40h

Enable PWMI pass through mode (when this bit is set to 1, then the DEV_CFG pin (pin 12) will be used as PWMI pin and PTN3460I I2C slave address will be 0x40).
0 - PWMI is disabled, PWMO is internally generated
1 - PWMI is enabled and used as PWMO source

<Variant Name>

AAEON Technology INC.

Title	LVDS		
Size	Document Number		Rev
Custom	NANOCOM-EHL		A1.1_0_0
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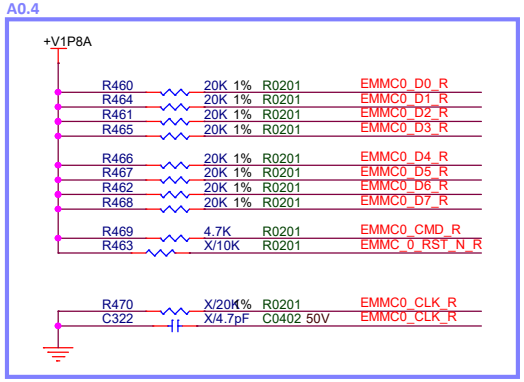
eMMC 5.1

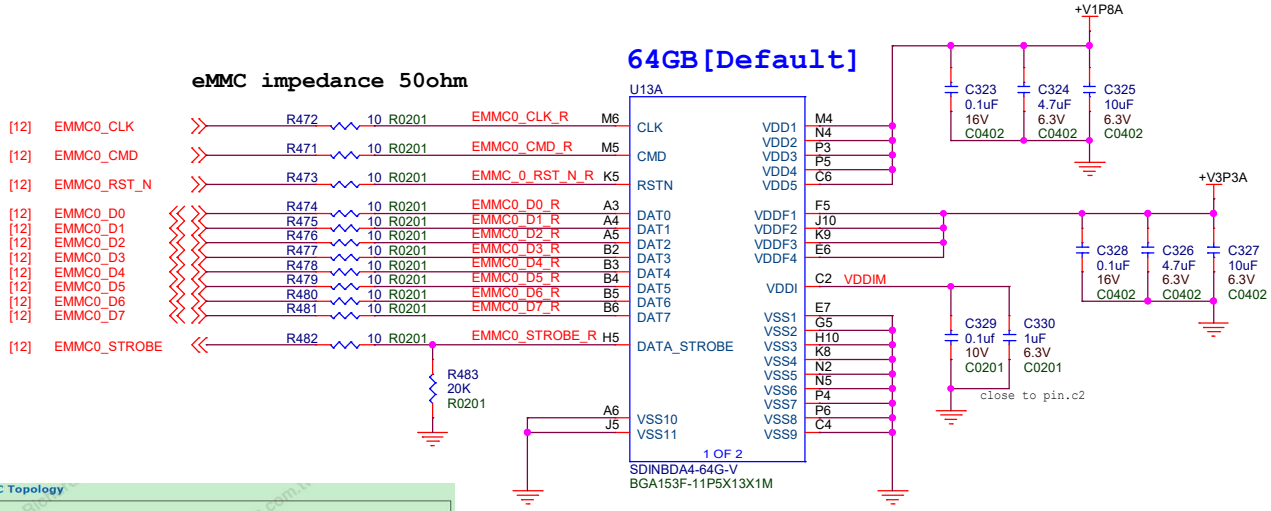
eMMC 5.1[U69]
32GB: 146900000N
64GB: 146900000K
128GB: 146900000H

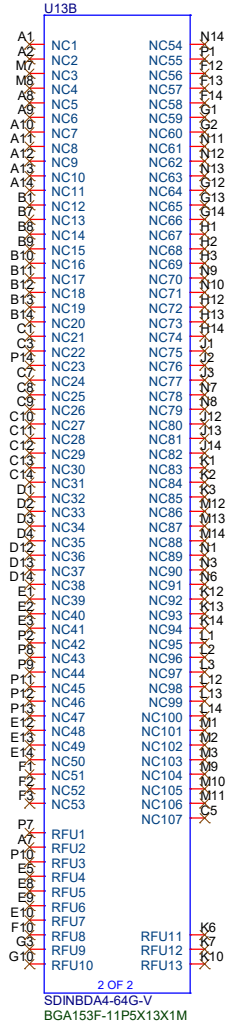
A0.4

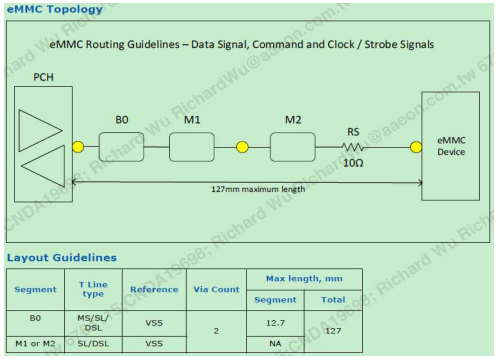


eMMC impedance 50ohm

64GB[Default]







Layout Guidelines

Segment	T Line type	Reference	Via Count	Max length, mm	
				Segment	Total
B0	MS/SL/DSL	VSS	2	12.7	127
M1 or M2	SL/DSL	VSS		NA	

<Variant Name>

AAEON Technology INC.

Title	eMMC		
Size B	Document Number NANOCOM-EHL		Rev A1.1_0_0
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LAN I225

20210303, A02, Change ethernet controller from I219 (1440219LM0) to I225(144X000026)(U8).

Place each one 22uF & one 0.1uF on pin9 & 38.
0.1uF one at each 0.9V pin

+V0P9A_LAN

C380 22uF 6.3V C0402 | C381 22uF 6.3V C0402 | C382 22uF 6.3V C0402 | C383 0.1uf 10V C0201 | C384 0.1uf 10V C0201 | C385 0.1uf 10V C0201 | C386 0.1uf 10V C0201 | C387 0.1uf 10V C0201 | C388 0.1uf 10V C0201

+V0P9A_LAN PWR plane Keep short and wide

+V0P9A_LAN_CRTL → L1 1uH.3.5A.45mohm → +V0P9A_LAN

R323 0 5% R0201

Place one 22uF & one 0.1uF on pin7.
0.1uF one at each 3.3V pin

0.67A

C389 22uF 6.3V C0402 | C390 22uF 6.3V C0402 | C391 22uF 6.3V C0402 | C392 0.1uf 10V C0201 | C393 0.1uf 10V C0201 | C394 0.1uf 10V C0201 | C395 0.1uf 10V C0201 | C396 0.1uf 10V C0201 | C397 0.1uf 10V C0201 | C398 0.1uf 10V C0201 | C399 0.1uf 10V C0201

+V3P3A_LAN → FB1 180ohm(100MHZ) L0603 → +V3P3A

A02, 20210316
Add C2351 for U8 pin decoupling.

*SMBUS DESIGN NOTE:
I225 Default SMBUS Address is 0x49.

*SMBUS DESIGN NOTE:
1. I225 SMBUS speed default is 1MHz so the pull-ups should be 499ohm.
2.When adding VoltageShifter/Buffer/Repeater on the SMBUS, the pull-up value might change to 1Kohm.
3.Change the pull-ups to 2.2Kohm when runs @400KHz or 10Kohm when runs @100KHz.

*PCIe DESIGN NOTE:
PCIe must be configured as a standard PCIe port. Do Not configure to the Gbe port (like I219).

U20

+1.0V_CTRL1, +1.0V_CTRL2, +1.0V_CORE1, +1.0V_CORE2, +1.0V_VP, +1.0V_A1, +1.0V_A2, +1.0V_A3, RESERVED, +3.3V_A1, +3.3V_A2, +3.3V_DC, +3.3V_PAD1, +3.3V_PAD2, +3.3V_VPH, +3.3V_XO, +3.3V_CDB

Foxville I226

[10] PCIE_4_RXP → C400 0.1uF 6.3V C0201 → LAN_RXP_C → PE_TX_P
[10] PCIE_4_RXN → C401 0.1uF 6.3V C0201 → LAN_RXN_C → PE_TX_N
[10] PCIE_4_TXP_C → PE_RX_P
[10] PCIE_4_TXN_C → PE_RX_N
[11] PCIE_1_CLK_DP → PE_CLK_P
[11] PCIE_1_CLK_DN → PE_CLK_N
[11] PCIE_CLKREQ#1 → R326 0 5% R0201 → PCIE_LAN_CLKREQ# → PE_CLKREQ_N
[5,13] PCIE_WAKE# → R327 0 5% R0201 → LANWAKE_N_R → PE_WAKE_N
[5,13,21,22] BUF_PLT_RST# → R329 0 5% R0201 → PLT_RST#_LAN → PE_RST_N

+V3P3A_LAN → R484 10K, R485 10K → LAN_SMBCLK, LAN_SMBDAT

LAN_SMBCLK, LAN_SMBDAT → SMB_CLK, SMB_DATA

Non - vPRO platform
R332 0 5% R0201 → LAN_ULP → ULP_WAKE_N

NVM1_SI, NVM1_SO, NVM1_SK, NVM1_CS# → SPI_DIN/AUX_PWR, SPI_DOUT, SPI_CLK, SPI_CS_N

LAN_XTAL2, LAN_XTAL1 → XTAL_IN, XTAL_OUT

JTAG_RSTN, JTAG_TMS, JTAG_TDO, JTAG_TDI, JTAG_CLK → JTAG_RSTN, JTAG_TMS/SDP2, JTAG_TDO/MDI_LANE_SWAP, JTAG_TDI/SDP1, JTAG_CLK

56,I226-IT.SRKTX,

MDI_A_P/N → LAN1_MDI0P/N [5] → LAN1_MDI0P/N [5]
MDI_B_P/N → LAN1_MDI1P/N [5] → LAN1_MDI1P/N [5]
MDI_C_P/N → LAN1_MDI2P/N [5] → LAN1_MDI2P/N [5]
MDI_D_P/N → LAN1_MDI3P/N [5] → LAN1_MDI3P/N [5]

LED0 → LAN1_LED_1000# → LAN1_LED_1000# [5]
LED1 → LAN1_LED_2500# → LAN1_LED_2500# [5]
LED2 → LAN1_LED_LNK#_ACT_R

LAN_PWR_GOOD → LAN_PWR_GOOD
LAN_DISABLE_N → LAN_DISABLE#_R → R574 0ohm/0402 → LAN_DEV_OFF# [21]

SDP0 → LAN_SDP0 → TP11 TP20

A02, 20210303
LAN_SDP0 reserve TP96 & Remove reserved PU 10k & PD 10k for saving PCB space

PHY_CAL → LAN_PHY_CAL

RBIAS → LAN_RBIAS → R578 200 1% R0402, R579 22K 1% R0402

EPAD → 57

+V3P3A_LAN → LAN_PWR_GOOD → R328 10K 1% R0201
+V3P3A_LAN → LAN_DISABLE#_R → R330 10K 1% R0201

*LED DESIGN NOTE:
There is no specific industrial standard for Ethernet LEDs.
This schematic just shows the most common SPEED LED configuration:
Highest Speed = Green
2nd Highest Speed = Yellow
All other lower Speeds = OFF
No Cable/Link = OFF
All LED pins are set active low. See Datasheet for additional info.

+V3P3A_LAN
R331 10K 1% R0201 JTAG_TDI
R333 10K 1% R0201 JTAG_TMS
R575 10K 1% R0201 JTAG_CLK
R576 10K 1% R0201 JTAG_TDO
R577 X/10K 1% R0201 JTAG_RSTN

*Nomal opeartion: unmount R52
At low, the JTAG is in the reset state and the multiplexed pins JTAG/SDPs act as SDPs. This pin has an internal weak pull-down that holds the JTAG controller in its reset state if the pin is left open.
*Enable Test Reset. Mount R52.
*If need PCB space, could remove R52 and add Test point.

A10, 20210820 EPSON Quartz Crystal Circuit Evaluation Report
Change C2346 and C2347 from 11A4310041 to 11A4962640 based on measurement result (6pF) and Luis suggestion (6.2pF cuz not exist 6pF 0402 in Aaeon).

LAN_XTAL1_R → R580 0 5% R0201 → LAN_XTAL1
Y4: 4, 1, 3, 2 → LAN_XTAL2
C402 6.2pF 50V C0402 | 25MHz 4P 10pF.30ppm.2.0*1.6*0.5mm;SMD | C403 6.2pF 50V C0402

*Crystal
Trace Length: The crystal trace lengths should be less than 1 inch.

+V3P3A_LAN
R582 10K 1% R0201 NVM1_WP#
R584 10K 1% R0201 NVM1_CS#
R585 10K 1% R0201 NVM1_SI

U27 W25Q80DVSSIG
CE# 1, SO 2, WP# 3, VSS 4, VDD 8, HOLD# 7, SCK 6, SI 5

NVM1_CS# → R588 0 5% R0201 → NVM1_R_CS#
NVM1_SI → R589 0 5% R0201 → NVM1_R_SI
NVM1_WP# → NVM1_R_WP#
NVM1_HOLD# → NVM1_R_HOLD#
NVM1_SK → R590 0 5% R0201 → NVM1_R_SK
NVM1_SO → R592 0 5% R0201 → NVM1_R_SO

+V3P3A_LAN → C404 0.1uf 10V C0201

+V3P3A_LAN → R591 10K 1% R0201 → NVM1_SK

+V3P3A_LAN
NVM1_HOLD# → R583 10K 1% R0201
NVM1_SO → R586 10K 1% R0201, R587 X/1K 5% R0201

Optional Security Strapping
1.For Development:Mount R51 to disable Flash Security. When updating, NVM.bin file is needed.
2.For Production & Normal Operation: Unmount R51.

EC SPI ROM P/N: 1469000007
(TF)IC.8 Mbit SPI Flash.SMD.SOIC-8P 208mil.Winbond.W25Q80DVSSIG

LAN1_LED_LNK#_ACT_R → PR63 10K 1% R0201 → LAN1_LED_LNK#_ACT [5]
+V3P3A_LAN → R581 10K 1% R0201 → LAN1_LED_LNK_ACT
Q10A EM6K7GT2R
Q10B EM6K7GT2R

ADD THE CIRCUIT FOR LAN LED LEAKAGE ISSUE

A10, 20211116
Add I225 MAC for offical BOM.

U27-1
I225 MAC
MAC
205X000288

Title: Intel LAN i226		
Size: Custom	Document Number: NANOCOM-EHL	Rev: A1.1_0_0
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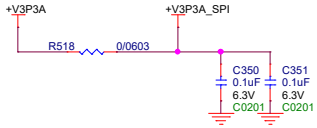
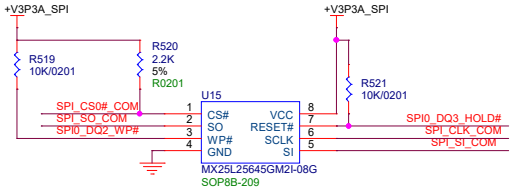
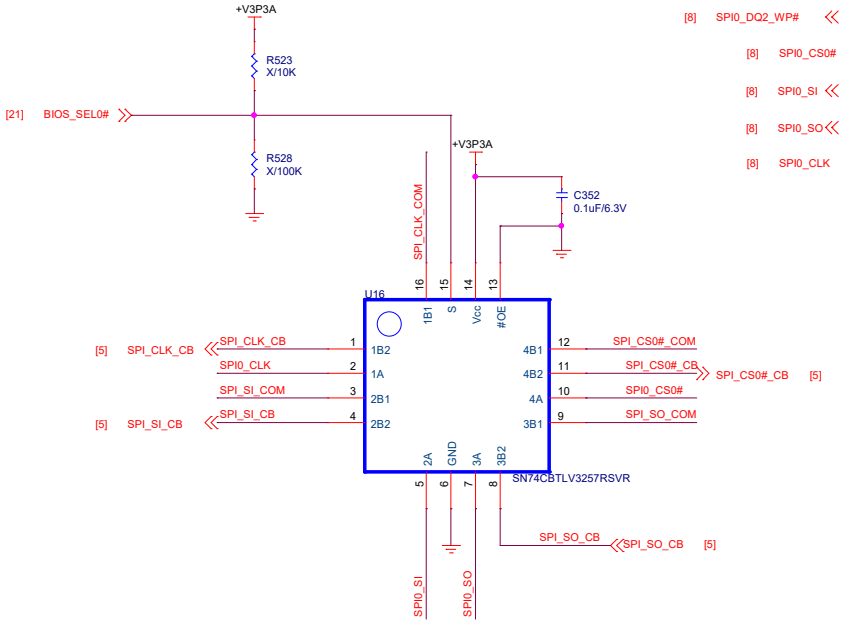
AAEON an ASUS assoc. co.

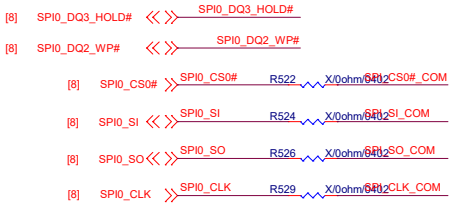
BIOS



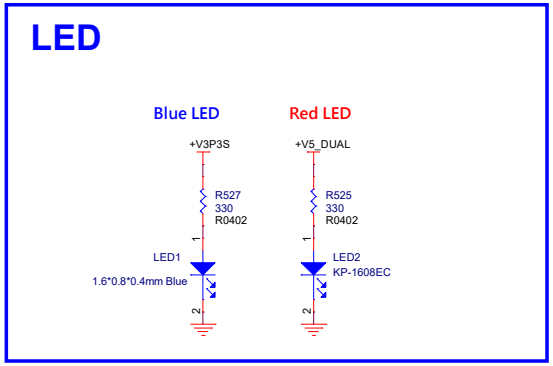


1462002564
(TF)IC.Flash Memory.256M Bit serial.SOP-8(209mil).w/ Dual & Quad SPI.SMD.MACRONIX.MX25L25645GM2I-08G

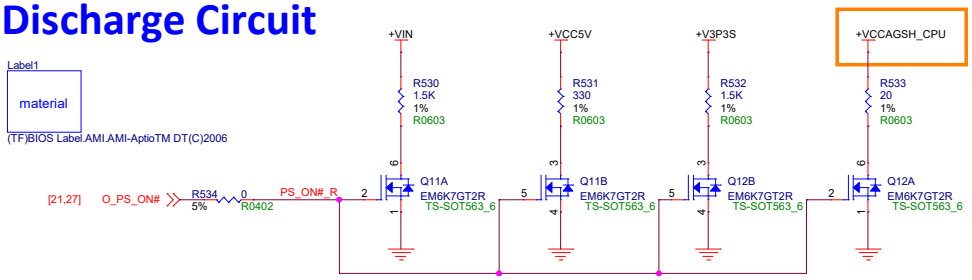




LED



Discharge Circuit



<Variant Name>

AAEON Technology INC.

Title	BIOS/Discharge/LED	
Size: Custom	Document Number: NANOCOM-EHL	Rev: A1.1_0_0
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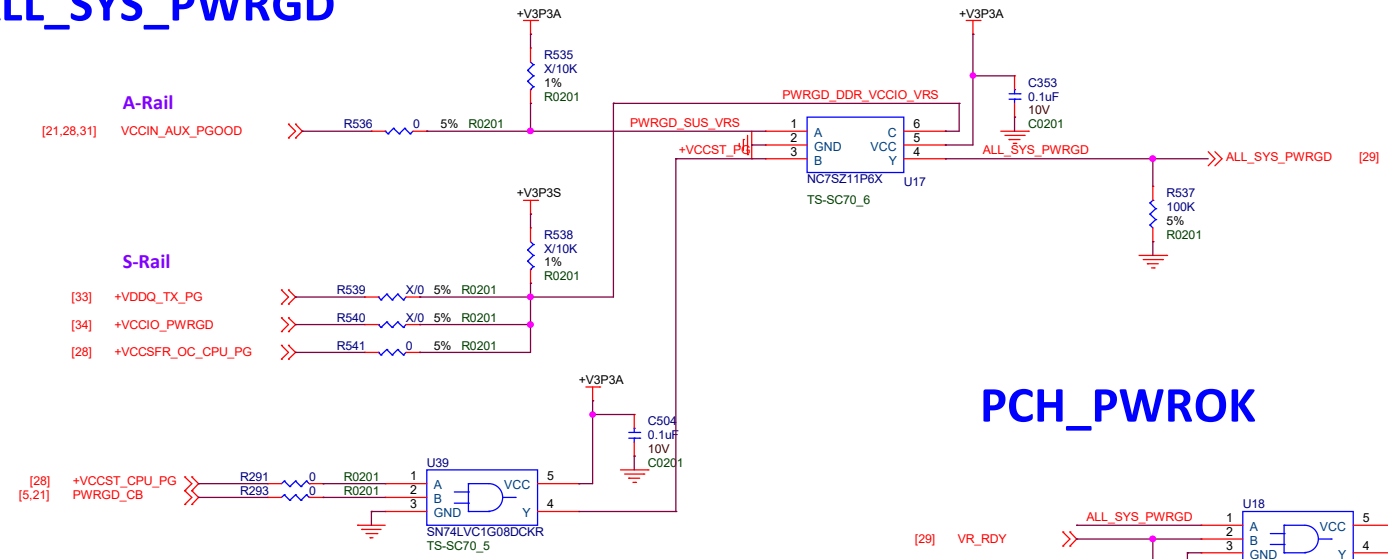
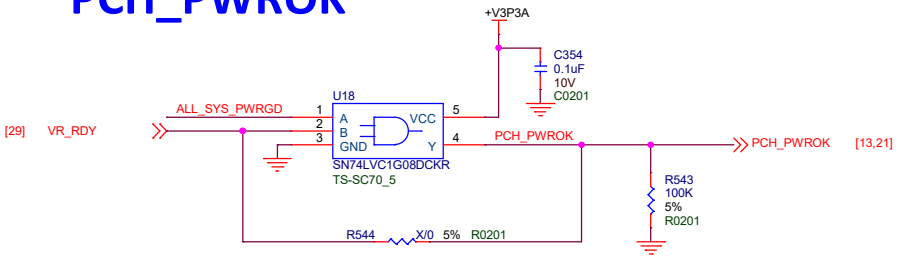
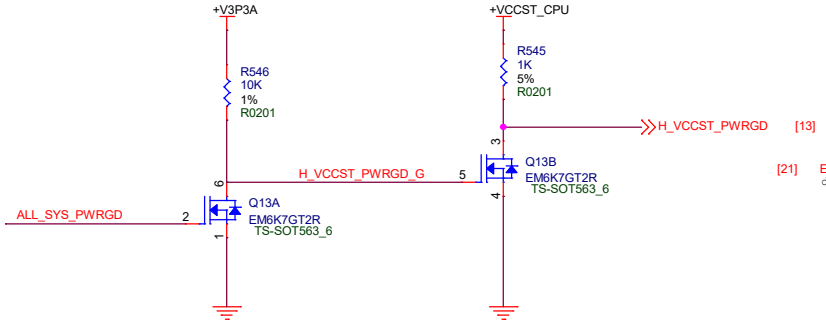
ALL_SYS_PWRGD



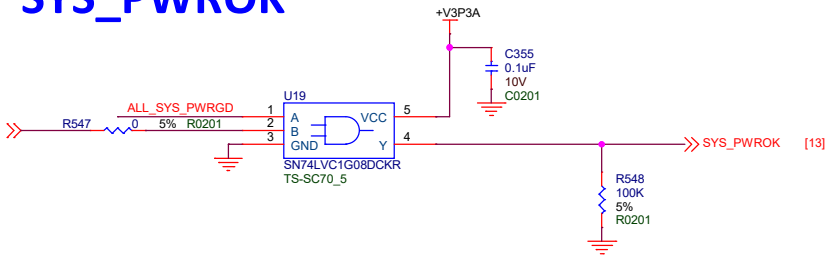
PCH_PWROK



VCCST_PWRGD [Level Shifter]



SYS_PWROK



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AAEON Technology INC.

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Title	Power Sequence		
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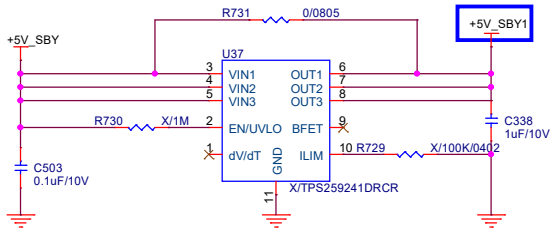
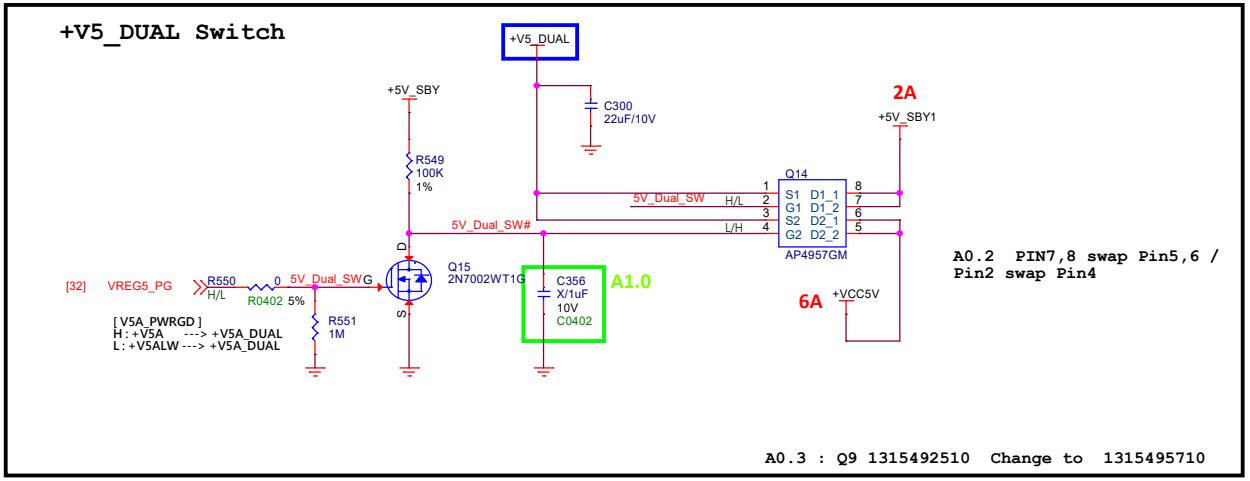
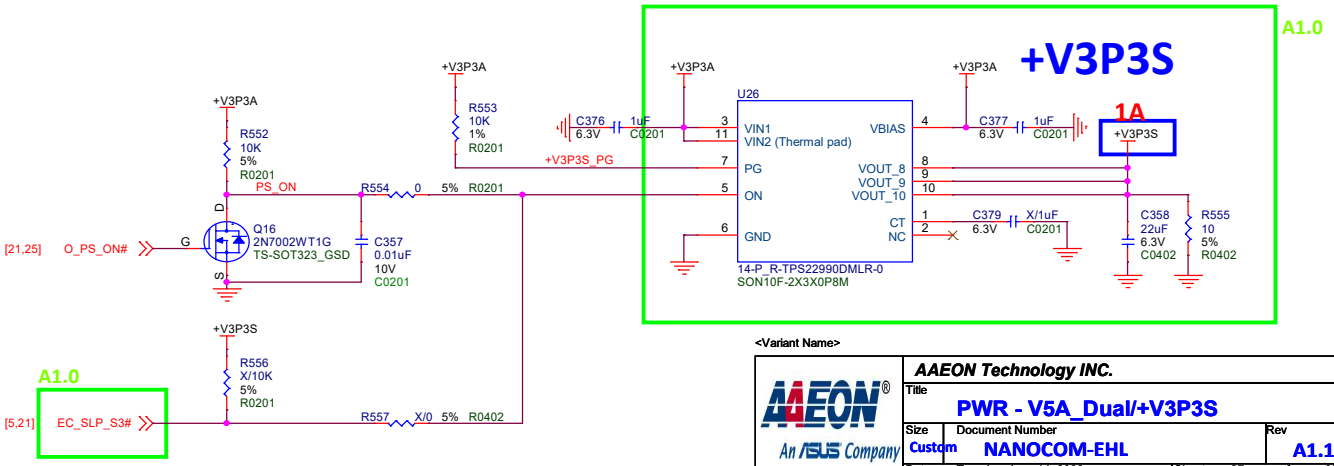
+V5_DUAL switch circuit







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AAEON Technology INC.

Title: PWR - V5A_Dual/+V3P3S		
Size: Custom	Document Number: NANOCOM-EHL	Rev: A1.1_0_0
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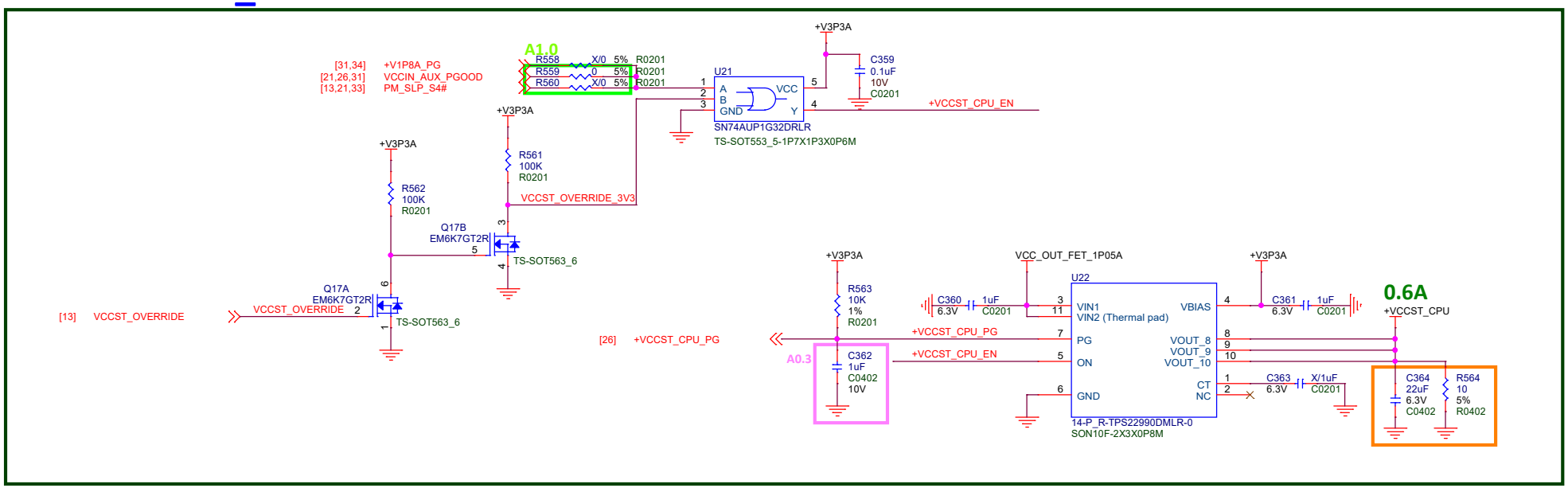
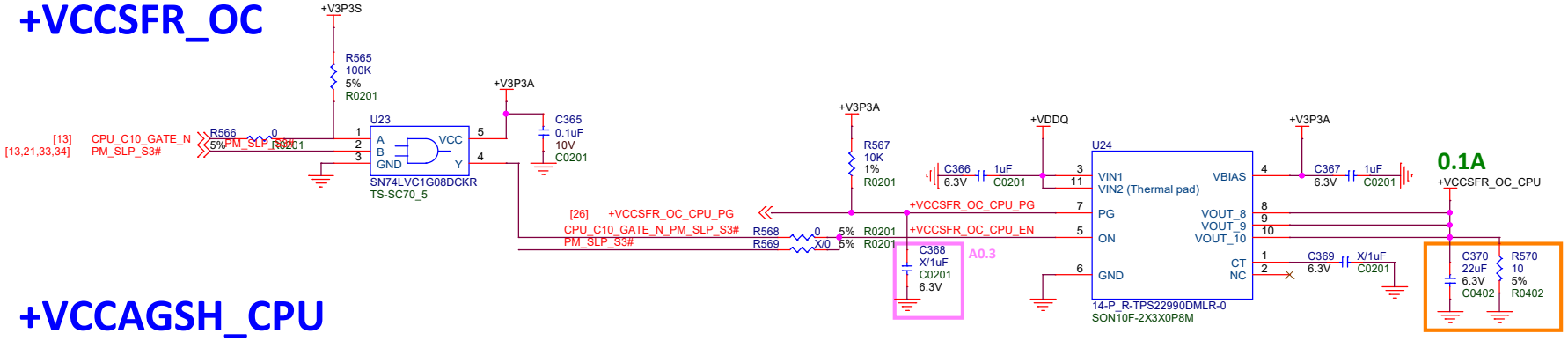
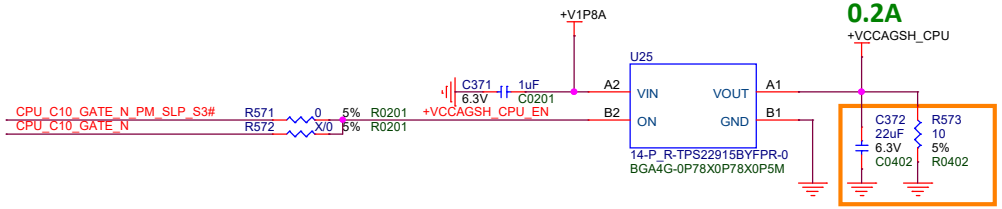
+VCCST_CPU



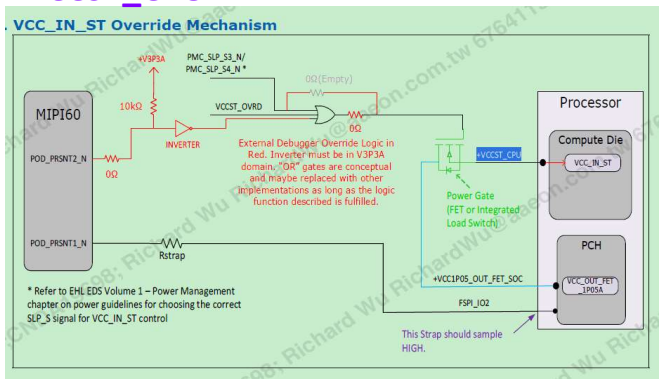
+VCCSFR_OC



+VCCAGSH_CPU



+VCCST_CPU



<Variant Name>

AAEON Technology INC.		
Title: PWR_+VCCSTG/+VCCSFR_OC		
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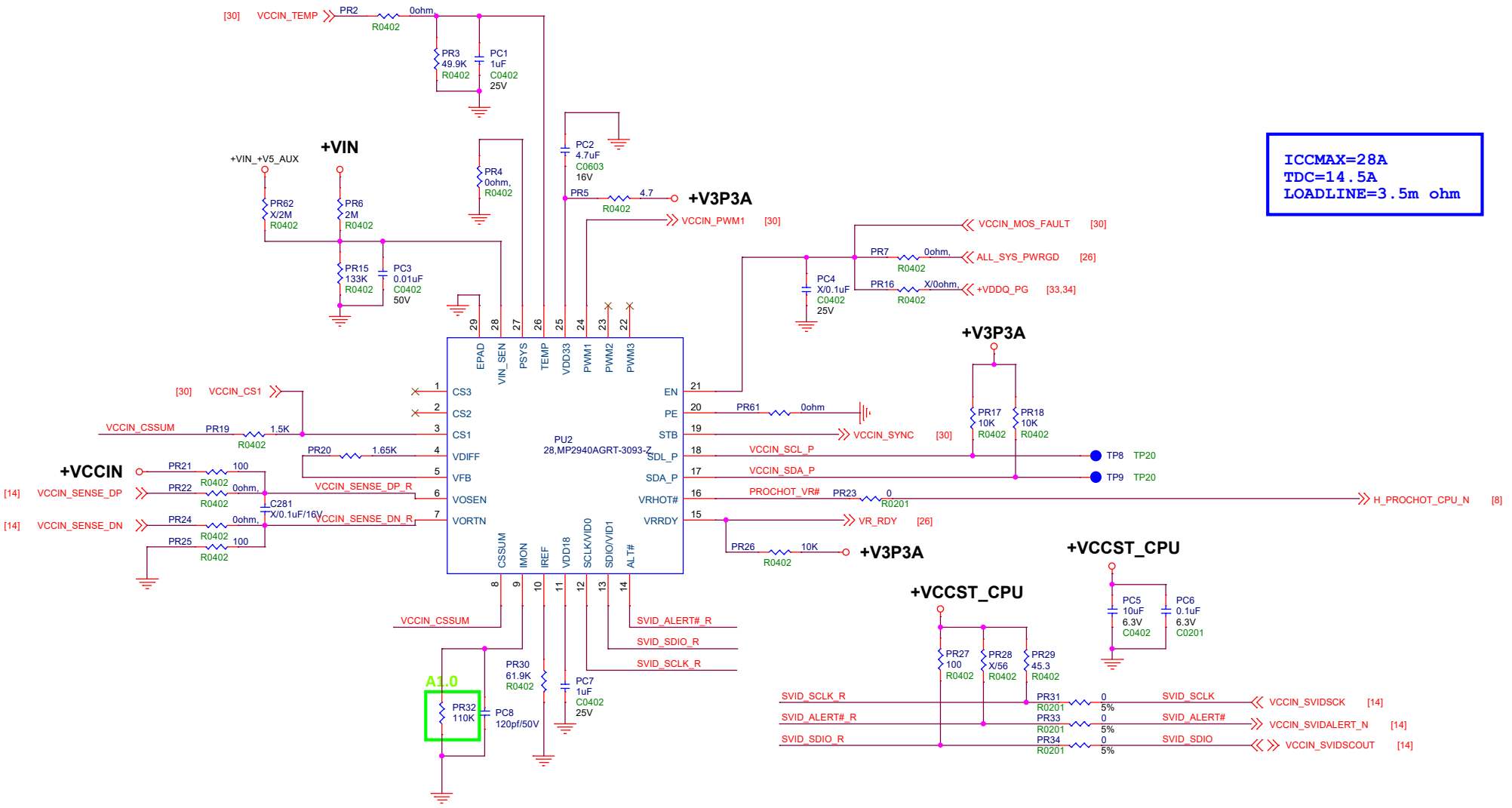
Elkhart Lake IMVP9



AAEON Technology INC.		
Title	PWR_IMVP9 Controller	
Size: Custom	Document Number: NANOCOM-EHL	Rev: A1.1_0_0
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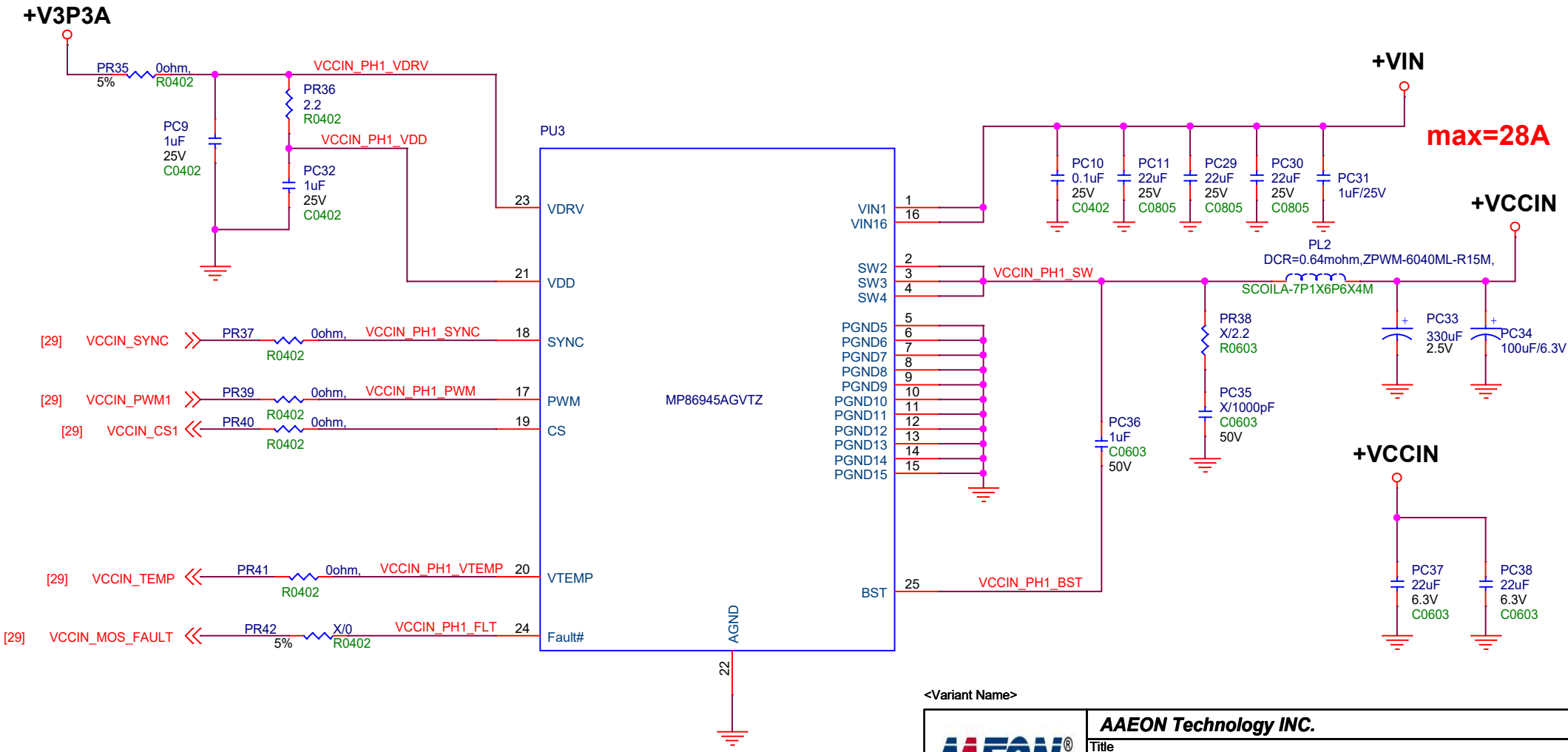
+VCCIN



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AAEON Technology INC.

Title: PWR_+VCCIN

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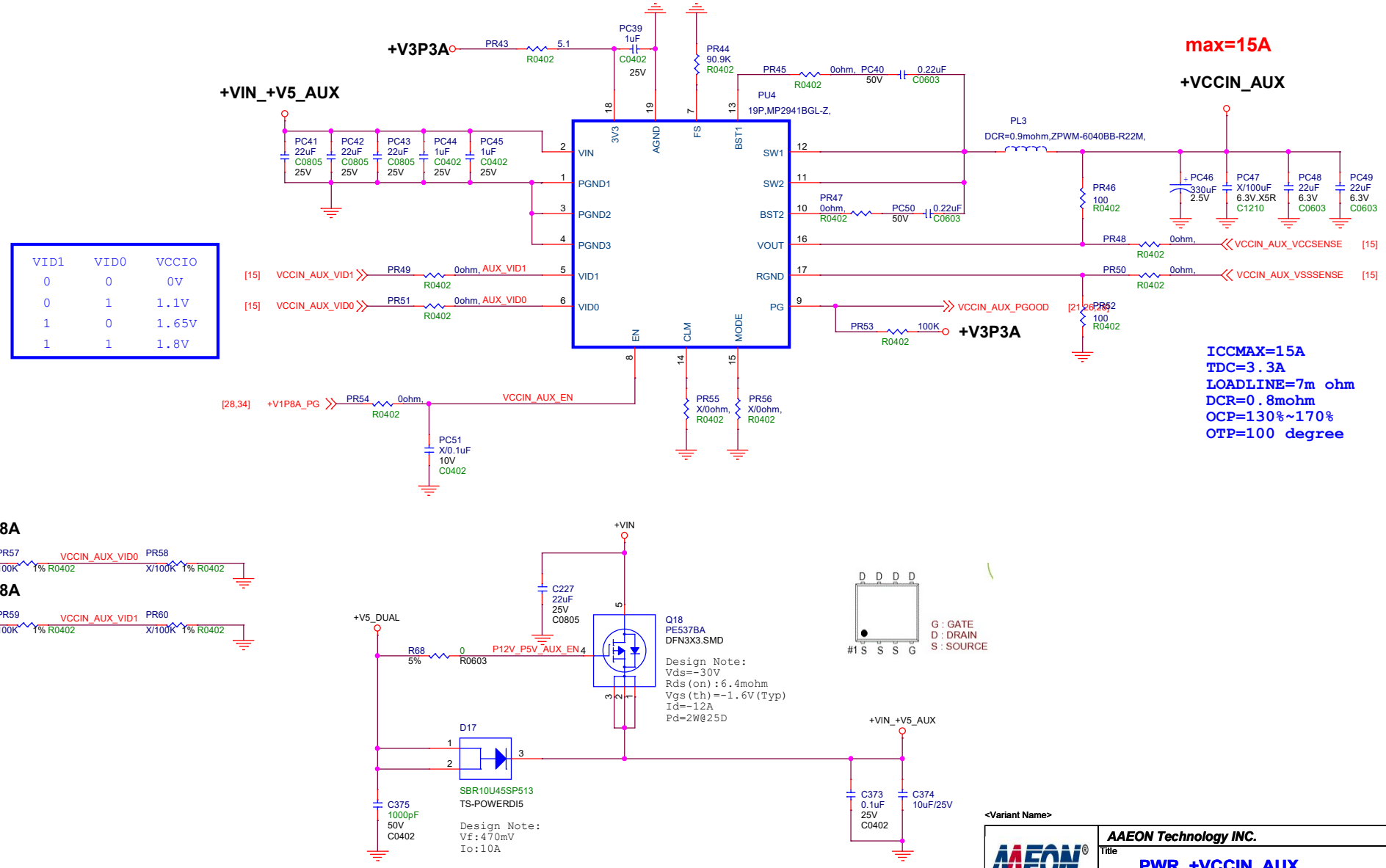
+VCCIN_AUX



VID1	VID0	VCCIO
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

ICCMAX=15A
TDC=3.3A
LOADLINE=7m ohm
DCR=0.8mohm
OCP=130%~170%
OTP=100 degree

<Variant Name>

AAEON Technology INC.

Title: PWR_+VCCIN_AUX

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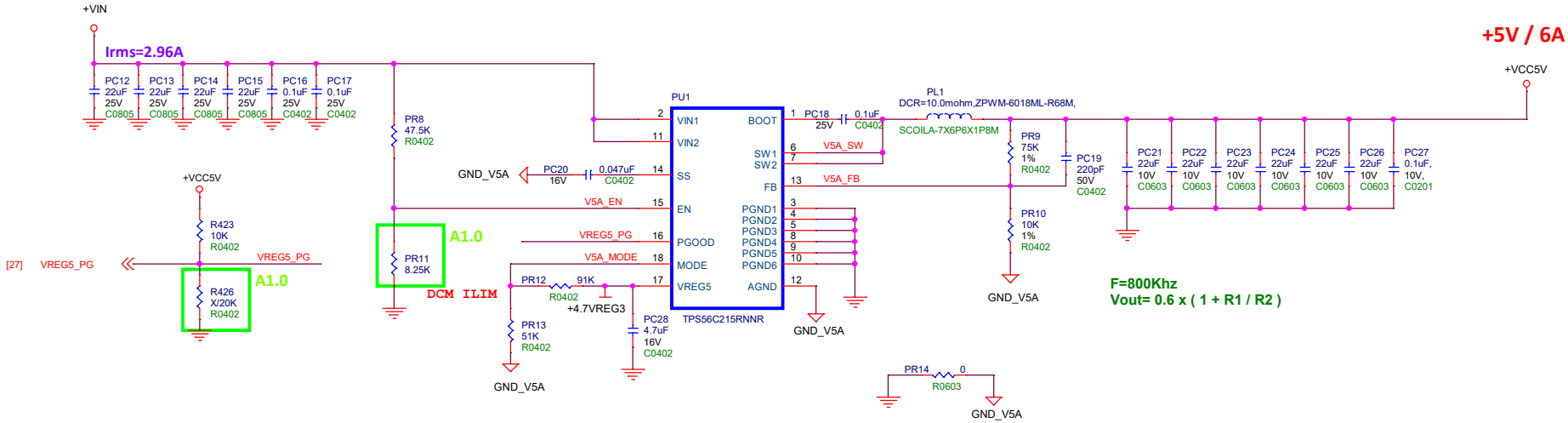
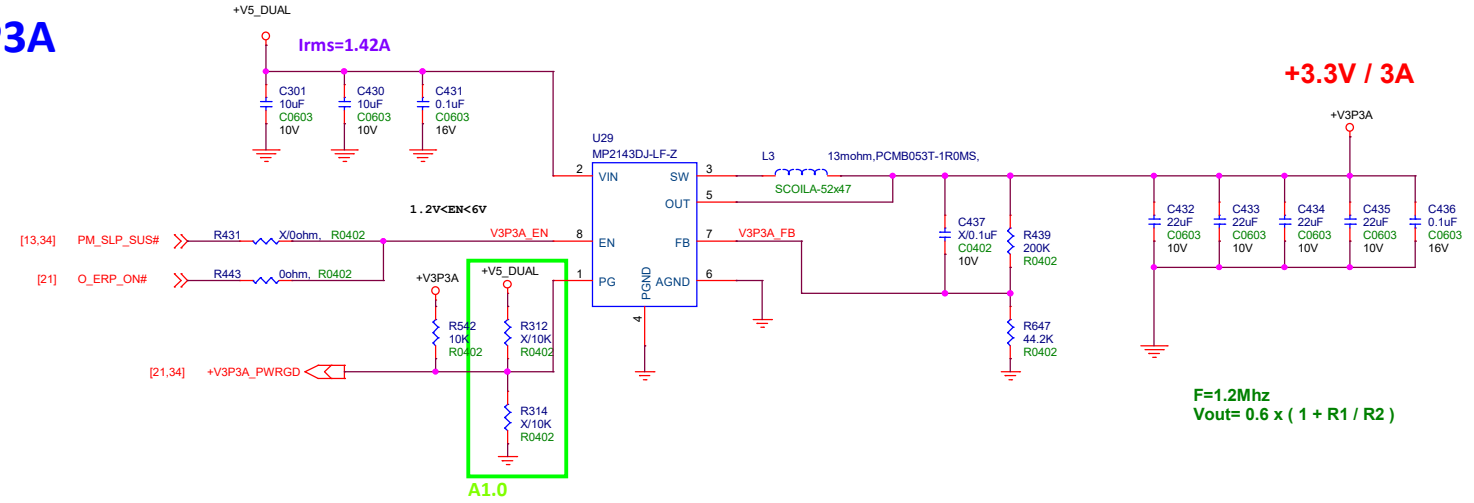
+V5A



+V3P3A



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AAEON An ASUS Company

AAEON Technology INC.

Title: PWR_+VCC5V/ +V3P3A

Size: Custom | Document Number: NANOCOM-EHL | Rev: A1.1_0_0

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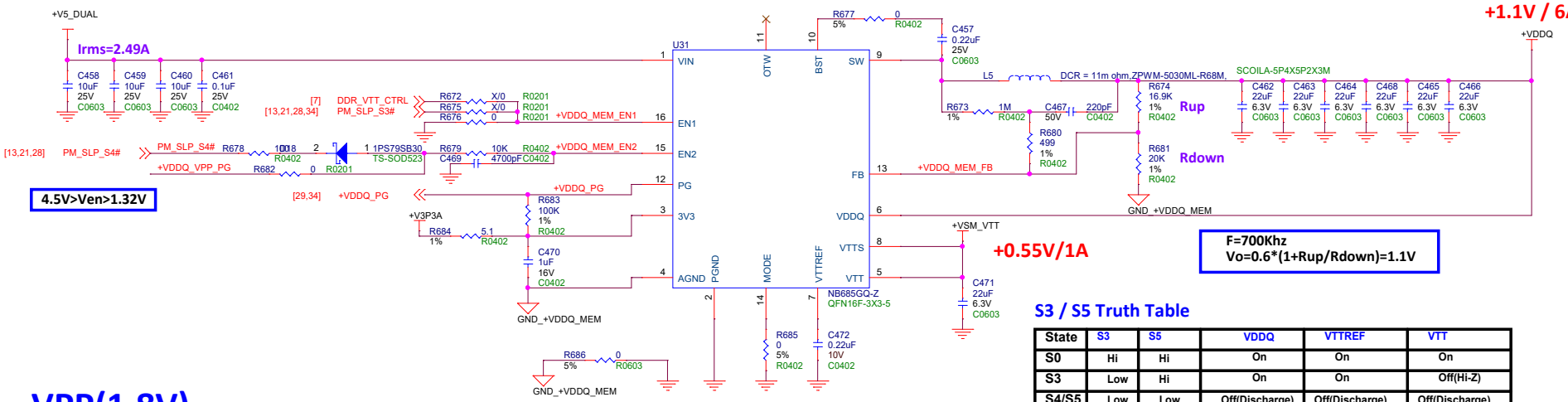
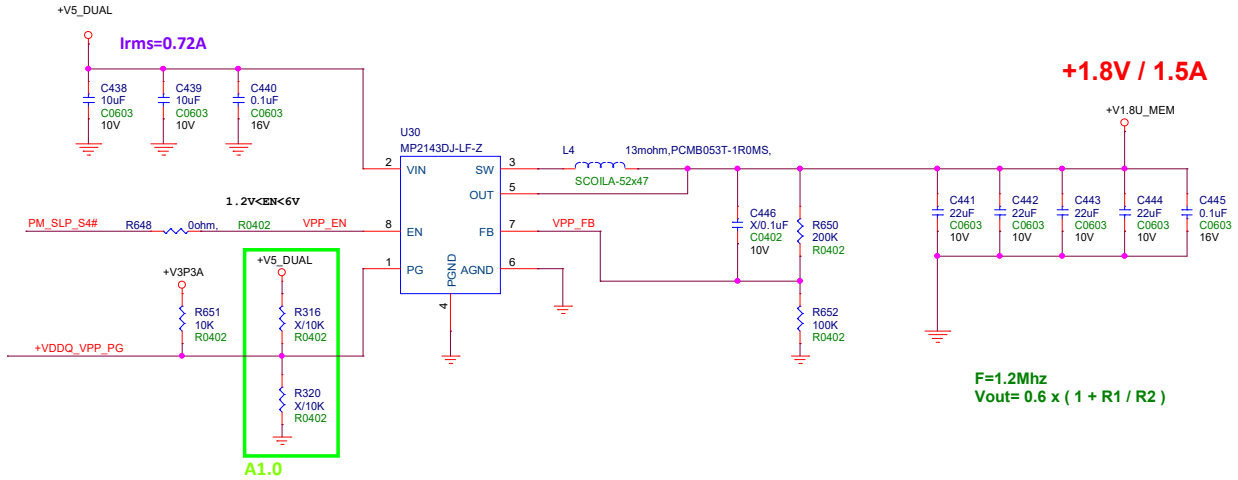
+VDDQ



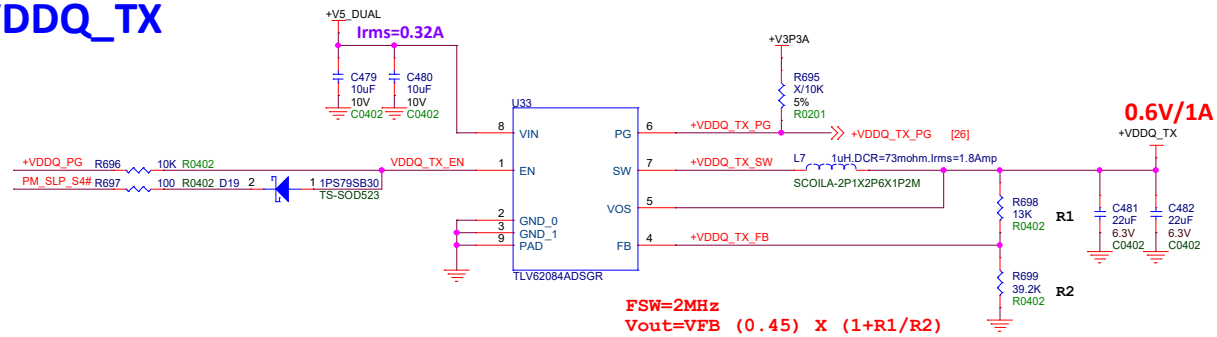
S3 / S5 Truth Table

State	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off(Hi-Z)
S4/S5	Low	Low	Off(Discharge)	Off(Discharge)	Off(Discharge)

VPP(1.8V)



+VDDQ_TX



<Variant Name>

AAEON Technology INC.

Title: PWR_+VDDQ/VPP/+VDDQ_TX

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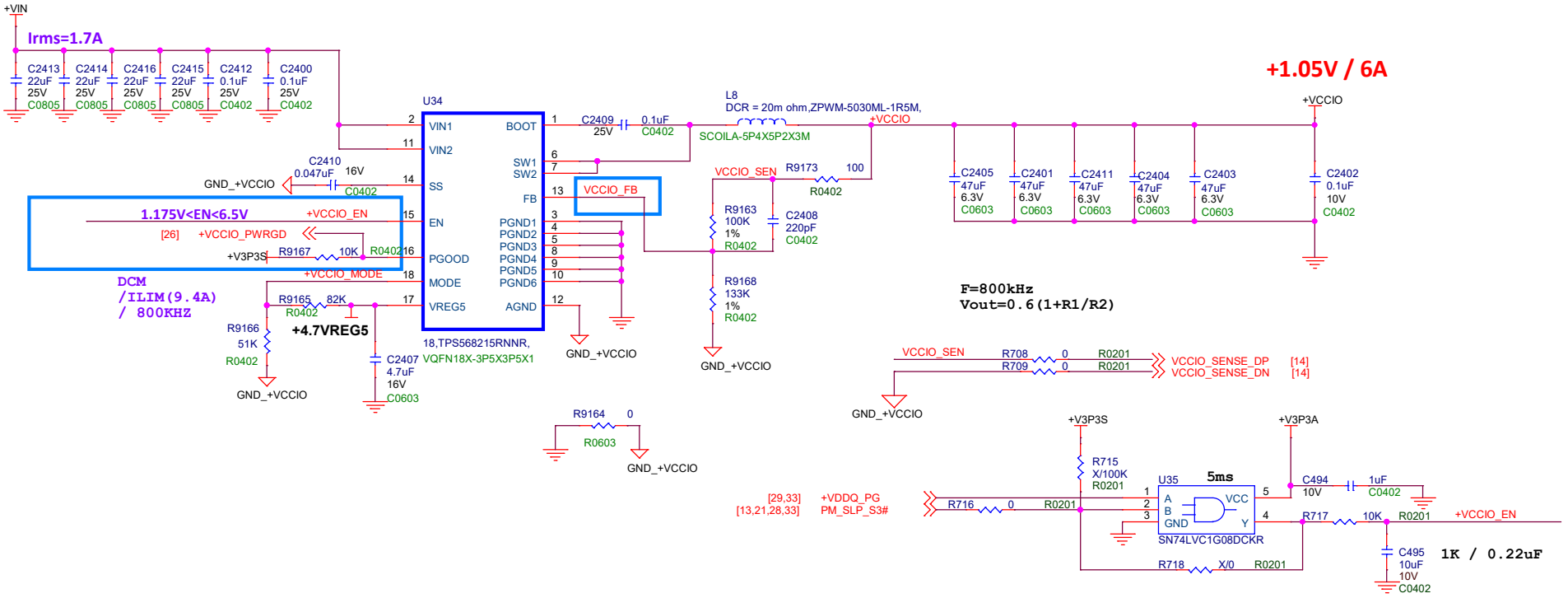
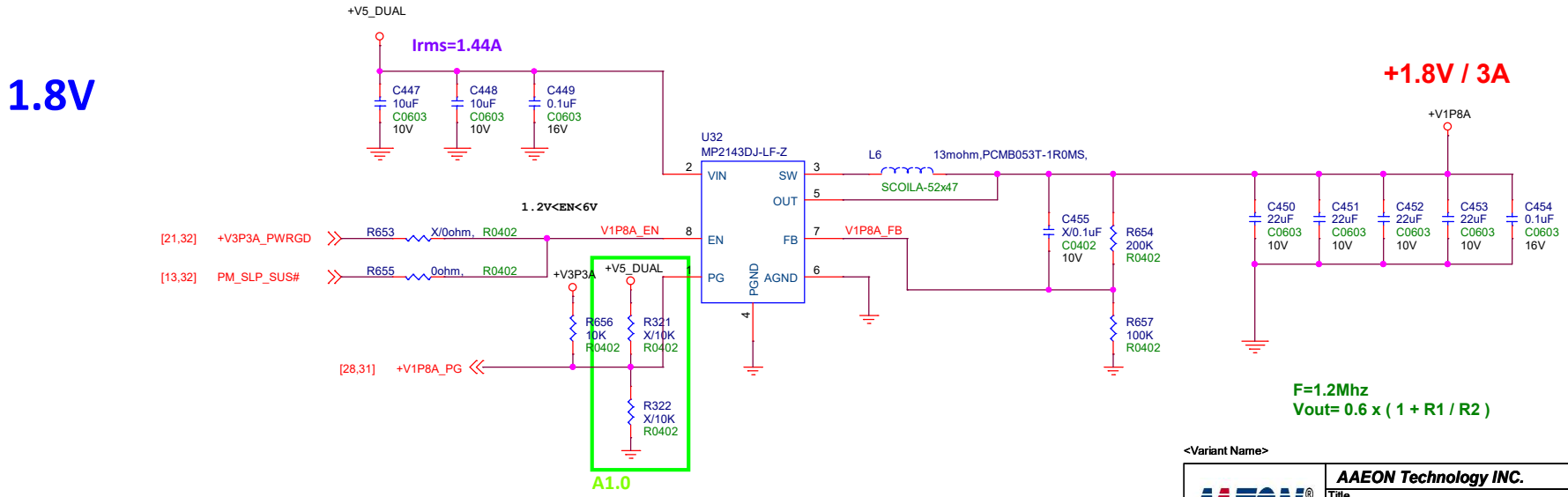
+VCCIO



1.8V



<Variant Name>

AAEON Technology INC.

Title: PWR_+VCCIO / +V1P8A

Size	Document Number	Rev
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NANOCOM-EHL

Revision History

DATA	Rev	Changed List Description	EOM Version / Gerber Version
20210827	A01	Initial Release	
20220427	A10	Remove C356, R426 for +V5_DUAL flutter issue	
20220427	A10	Remove R409, R395, R255 for A-rail power leakage issue	
20220427	A10	Remove R408 for power button leakage issue	
20220427	A10	Remove R560, Add R559 meet Intel Power up sequence	
20220427	A10	Remove R401 for S-rail power leakage issue	
20220427	A10	PR11 change to 8.25K from 18.2K for +VCC5V can't shutdown issue	
20220429	A10	ITE 8882 pin23 add R80 colay ITE 8883	
20220429	A10	ITE 8882 JP5 change to R370 and R363/R366 change to 10K to GND from ITE check	
20220429	A10	R228 change to 130ohm 1% for USB 2.0 eye diagram fail	
20220429	A10	Add BID from PCH for Memory size selection	
20220429	A10	Add BID from PCH for Memory size selection	
20220503	A10	Delet U20(NCP45520), change to U26(TPS22990)	
20220513	A10	U29, U30, U32 PG pin add bleeder chain	
20220516	A10	PR32 change to 110K ohm fix CPU base clock too low issue	
20220607	A11	ITE eSPI to LPC bridge change to IT-8883 from IT-8882	
20220608	A11	EC KSO8 add I_BATLOW# from carrier board	
20220608	A11	Intel i210 change to Intel i226	

<Variant Name>

AAEON An ASUS Company

AAEON Technology INC.

Title: Revision History

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