



Raptor Lake-P for IoT Platforms

External Design Specification (EDS) Addendum

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1.0 Revision History

Document Number	Revision Number	Description	Release Date
735978	1.2	Added <ul style="list-style-type: none">Chapter 7 - Added new subsection- BIOS Sub-Region Capsule Update Updated <ul style="list-style-type: none">Chapter 3, Display was revisedChapter 2, Thermal Management - Table 4- Updated cTDPFigure 1 was revised	October 2022
735978	1.0	Initial release	August 2022

2.0 Introduction

This Raptor Lake-P External Design Specification (EDS) Addendum is a supplementary document that covers IOT-specific features and complements for the Raptor Lake Processor External Design Specifications Volume 1 of 2 (RDC #[640555](#)), Raptor Lake Processor External Design Specifications Volume 2 of 2(RDC #[732067](#)), Intel® 600 Series Chipset Family and Intel® 700 Series Chipset Family On-Package Platform Controller Hub (PCH) External Design Specification, Volume 1 of 2 (RDC #[626817](#)) and Intel® 600 Series Chipset Family and Intel® 700 Series Chipset Family On-Package Platform Controller Hub (PCH) External Design Specification, Volume 2 of 2 (RDC #[630094](#))

Raptor Lake- P processor is a 64-bit, multi-core processor built on Intel® 7 process technology.

The P-Processor Line is a Multi-Chip Package (MCP) that consist of RPL-P CPU and RPL PCH-P die on the same package.

Throughout this document, RPL Processor EDS is used as a general term to refer to the Raptor Lake Processor External Design Specifications Volume 1 of 2 (RDC #[640555](#)), Raptor Lake Processor External Design Specifications Volume 2 of 2(RDC #[732067](#)) and all SKUs, unless mentioned otherwise.

Moreover, RPL PCH-P EDS is used as a general term to refer to the Intel® 600 Series Chipset Family On-Package Platform Controller Hub (PCH) External Design Specification Volume 1 of 2 (RDC #[626817](#)),Intel® 600 Series Chipset Family and Intel® 700 Series Chipset Family On-Package Platform Controller Hub (PCH) External Design Specification, Volume 2 of 2 (RDC #[630094](#)), and all SKUs, unless mentioned otherwise.

NOTE

This document serves as a supplementary documentation, please ensure all required specifications from the RPL Processor EDS and RPL PCH-P EDS are met prior to using this document, unless mentioned otherwise.

2.1 Terminology

Table 1. Terminology

Term	Description
AHCI	Advanced Host Controller Interface
API	Application Programming Interface
ART	Always Running Timer
BGA	Ball Grid Array
CAT	Cache Allocation Technology
<i>continued...</i>	

Term	Description
CML	Current-Mode Logic
CMTG	Common Master Timing Generator
Intel® CNVi	Intel® Integrated Connectivity
COE	Checksum Offload Engine
CRC	Cyclic Redundancy Check
CSR	Control and Status Register
cTDP	Assured Power (previously known as configurable TDP)
DMA	Direct Memory Access
DTR	Dynamic Temperature Range
EDS	External Design Specification
FLR	Function Level Reset
Intel® FSM	Intel® Flash Sector Manager
GbE	Gigabit Ethernet
GPIO	General Purpose Input/Output
gPTP	Generalized Precision Time Protocol
HSIO	High Speed Input/Output
IOTLB	I/O Translation Lookaside Buffer
ISH	Integrated Sensor Hub
MAC	Media Access Control
MCP	Multi Chip Package
MDIO	Management Data Input/Output
MMC	MAC Management Counters
MMIO	Memory Mapped I/O
MTL	Maximum Transfer Length
OS	Operating System
PCH	Platform Controller Hub
PCS	Physical Coding Sublayer
PMC	Power Management Controller - dedicated microprocessor running power management firmware
PSF	Processor Spec Finder
PTM	Precision Time Measurement
QoS	Quality of Service
RDC	Resource & Documentation Centre (Intel)
Intel® RDT	Intel® Resource Director Technology
RPL	Raptor Lake
SGMII	Serial Gigabit Media Independent Interface

continued...

Term	Description
SKU	Stock Keeping Unit
SPH	Split Headers
SPI	Serial Peripheral Interface
STA	Station Management
TBI	Ten Bit Interfaces
TBS	Time Based Scheduling
Intel® TCC	Intel® Time Coordinated Computing
TDP	Processor Base Power (a.k.a Thermal Design Power)
TSC	Time Stamp Counter
TSN	Time-Sensitive Networking
TSO	TCP Segmentation Offload
WCET	Worst-Case Execution Time
WOL	Wake on LAN

2.2 Reference Documents

Table 2. Reference Documents

Document	Document No./Location
Raptor Lake P Processor External Design Specification Volume 1 of 2	640555
Raptor Lake P Processor External Design Specification, Volume 2 of 2	732067
Raptor Lake U P H Platform Design Guide	686872
Raptor Lake Platform Design Guide Addendum for IoT Platforms	737640
Intel® 600 Series Chipset Family On-Package Platform Controller Hub (PCH) Electrical and Thermal Specifications	631116
Raptor Lake Platform Message of the Week	646469
Raptor Lake P for IoT Platforms Message of the Week (MoW)	739688
Intel® 600 Series Chipset Family and Intel® 700 Series Chipset Family On-Package Platform Controller Hub (PCH) External Design Specification, Volume 1 of 2	626817
Raptor Lake- U/P/H Platform Controller Hub External Design Specification - Volume 2 of 2	630094
Raptor Lake H/P/U Processor Lines BGA Package Ballout Mechanical Specification	710352
Intel® Power and Thermal Analysis Tool	637737
Raptor Lake U/P/H PCH GPIO Implementation Summary	627075
IOTG Raptor Lake-P Platform Gold Deck	730563
Raptor-P Design In for IoT Platforms	739186
Raptor Lake Mobile Platform TMDG for IOTG Specific Applications	739289

2.3 Supported Package and Die Plan

Table 3. Processor Lines Package and Die Plan

Processor Line Segment	Die Type	Package (mm3)	TDP (cTDP)	PCH
RPL-P (6+8)	6P + 8E + 2	25 x 50 x 1.185	45W (35W)	RPL PCH-P
RPL-P (4+8)			28 W (20W/35W)	
RPL-P (4+4)			28 W (20W/35W)	
RPL-P (4+8)			15W (12W/28W)	
RPL-P (4+4)			15W (12W/28W)	
RPL-P (2+8)	2P + 8E + 2		15W (12W/28W)	
RPL-P (2+4)			15W (12W/28W)	
RPL-P (1+4)				

3.0 Thermal Management

3.1 Thermal Management Introduction

The Raptor Lake processor is a 64-bit, multi-core processor built on a Intel® 7 process technology. The P-processor line is a Multi-Chip Package (MCP) that consist of RPL-P compute die and RPL PCH-P die on the same package.

Table 4. Raptor Lake-P Processor Line

Segment	Package	SKU Series	Processor Base Power (a.k.a TDP)	cTDP	Processor IA P-Cores	Processor IA E-Cores	Graphics Configuration
RPL-P (6+8)	BGA1744	Embedded	45W	35W / 65W	6	8	96EU
RPL-P (4+8)			45W	35W / 65W	4	8	80EU
RPL-P (4+4)			45W	35W / 65W	4	4	48EU
RPL-P (4+8)			28W	20W / 35W	4	8	96EU
RPL-P (4+8)			28W	20W / 35W	4	8	80EU
RPL-P (4+4)			28W	20W / 35W	4	4	48EU
RPL-P (2+8)			15W	12W / 28W	2	8	96EU
RPL-P (2+8)			15W	12W / 28W	2	8	80EU
RPL-P (2+4)			15W	12W / 28W	2	4	64EU
RPL-P (1+4)			15W	12W / 28W	1	4	48EU
RPL-P (6+8)	BGA1744	Industrial	45W	35W / 65W	6	8	96EU
RPL-P (4+8)			45W	35W / 65W	4	8	80EU
RPL-P (4+4)			45W	35W / 65W	4	4	48EU
RPL-P (4+8)			28W	20W / 35W	4	8	96EU
RPL-P (4+8)			28W	20W / 35W	4	8	80EU
RPL-P (4+4)			28W	20W / 35W	4	4	48EU
RPL-P (2+8)			15W	12W / 28W	2	8	96EU
RPL-P (2+8)			15W	12W / 28W	2	8	80EU
RPL-P (2+4)			15W	12W / 28W	2	4	64EU
RPL-P (1+4)			15W	12W / 28W	1	4	48EU

Notes:

1. Processor lines offer may change.
2. For more details, refer to, Raptor Lake Processor External Design Specification (EDS) Volume 1 of 2 (RDC #640555).

continued...

Segment	Package	SKU Series	Processor Base Power (a.k.a TDP)	cTDP	Processor IA P-Cores	Processor IA E-Cores	Graphics Configuration
3. The Processor Base Power (a.k.a TDP) is the average power dissipation in junction temperature operating condition limit, for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU. 4. TDP workload may consist of a combination of processor IA core intensive and graphics core intensive applications. 5. P-Cores refer to Performance-cores and E-Cores refer to Efficient-cores.							

3.2

P-Processor Line Thermal and Power Specifications

Additional note for Thermal and Power Specifications. This note is an addition to the other notes mentioned in Thermal Management of the Raptor Lake Processor External Design Specification (EDS) Volume 1 of 2.

Table 5. Processor Temperature Specifications

Segment	SKU Series	Symbol	Description	Temperature Range		TDP Specification Temperature Range		Notes
				Min	Max	Min	Max	
P-Processor Line BGA	Embedded	T_j	Junction Temperature Limit	0°C	100°C	35°C	100°C	1,2
	Industrial			-40°C	100°C			
	Embedded	DTR	DTR Temperature Limit	$T_{BOOT}-70$	$T_{BOOT}+70$	N/A	N/A	3
	Industrial			$T_{BOOT}-110$	$T_{BOOT}+110$			

Notes:

1. The processor supports extended ambient temperature range, and memory devices should operate in the same condition.
2. For other junction temperature specification, refer to the note mentioned in P-Processor Line Thermal and Power Specifications under Thermal Management in the Raptor Lake Processor External Design Specification (EDS) Volume 1 of 2 (RDC #640555).
3. DTR is the range of T_j starting from boot (T_{BOOT}) and transitioning Cold-to-Hot ($T_{BOOT}+DTR$) and/or Hot-to-Cold ($T_{BOOT} - DTR$). A T_j outside of the DTR range requires a re-boot but is not enforced by the hardware.

4.0 Display

Genlock and Pipelock are solutions for synchronizing clock and vsync signals between displays. Genlock is synchronizing display signals among multiple GPUs while Pipelock is synchronizing display signals among pipes in a single GPU.

4.1 Pipelock and Genlock

4.1.1 Overview

Pipelock is defined as synchronization between ports driven from a single GPU. Genlock is defined as synchronization between ports driven from multiple GPUs. For timing synchronization, display HW supports port sync, Common Master Timing (CMTG) and Genlock features.

NOTE

Pipelock is a sub-feature of Genlock where vsync timings for all secondary pipes are synced to the primary pipe's timings. Pipelock is activated by default when Genlock is enabled.

Figure 1. High Level Diagram of Single Host iGPU Pipelock



Figure 1 above illustrates the single host iGPU Pipelock where one of the pipes acts as a primary display, whereby its vsync timings are synchronized with the secondary displays.

5.0 Graphics

5.1 SRIOV Overview

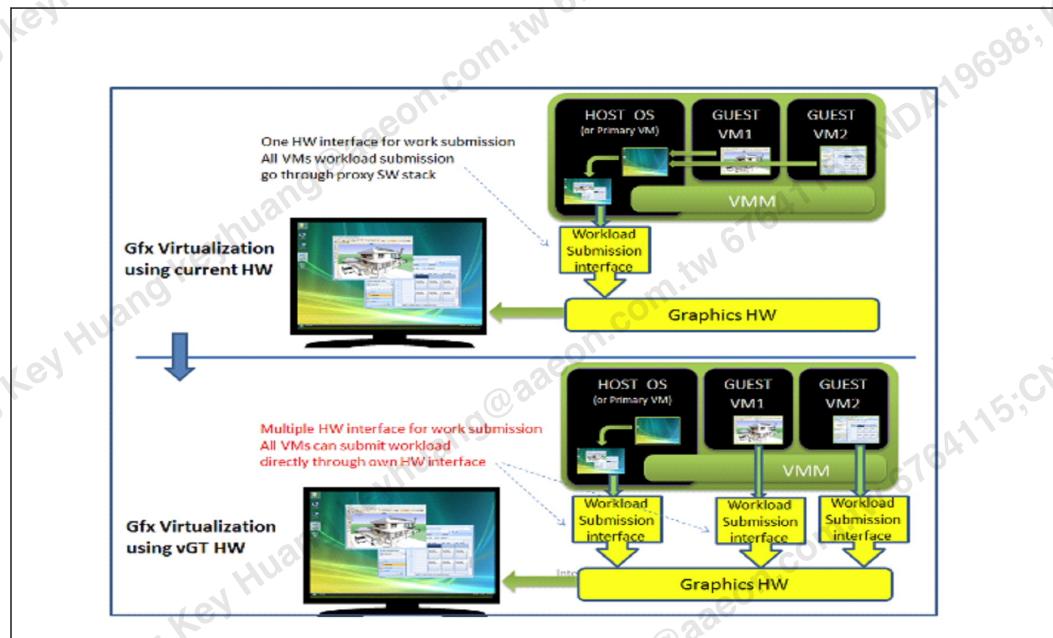
Graphics virtualization allows multiple Virtual Machines (VMs) to access high-quality, high-performance graphics, with minimal software overhead. The graphics virtualization feature adds hardware and firmware to improve performance and enable VMs to support Intel® HD Graphics, Iris graphics, and Iris Pro graphics in a standard way, eliminating special requirements that could be barriers to adoption.

Introduction

Intel® platforms have supported Virtualization Technology for Directed I/O (VT-d). The original Intel® Graphics Virtualization Technology (Intel® GVT) model using VT-d technologies is called GVT-d, which assigns the whole graphics to a single VM. It brings close-to-native GPU performance to the VM which owns the graphics. However, it prevents other VMs and the host sharing the capabilities of the graphics. By contrast, Graphics SR-IOV provides graphics sharing capabilities across multiple VMs and host without compromise in graphics performance.

Figure 2 shows the new concept of Intel® Graphics Virtualization Technology (Intel® GVT), where each VM can access fully accelerated graphics capabilities.

Figure 2. Fully Virtualized Graphics - Conceptual View

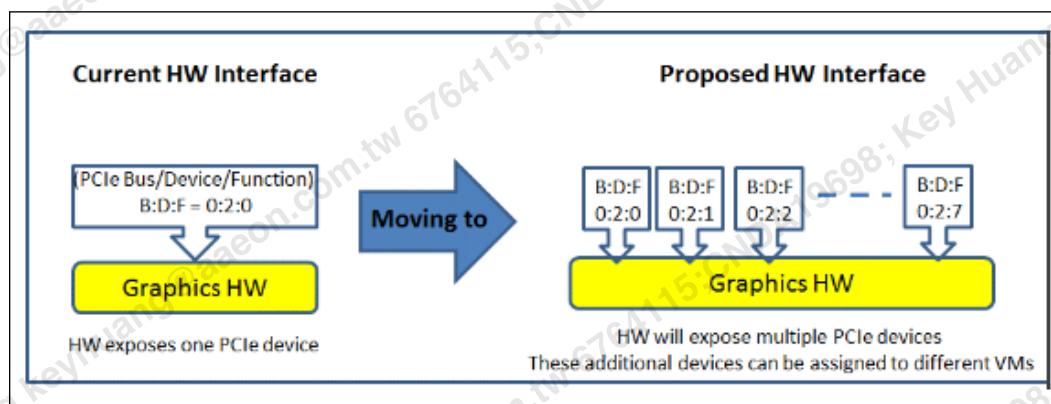


The capability depicted above requires the following infrastructure:

- Graphics hardware that exposes multiple hardware interfaces, for assignment to different VMs;
- Resources to submit the graphics workload:
 - Memory (aperture) allowing each VM to submit workload and associated data surfaces;
 - A graphics translation table (GTT) to manage aperture pages;
 - Some MMIO registers exposed to each VM;
- A signaling mechanism to invoke the hardware to execute the workload;
- A signaling mechanism for the hardware to convey relevant information by sending interrupts;
- A mechanism to display the output produced by the execution of the workload.

Figure 4 shows the proposed hardware interface used to allow multiple software stacks to each get their own “graphics device.”

Figure 3. **Proposed Hardware Interface**



5.2 Hardware Interface

5.2.1 Display Output from a Virtualized Environment

There are several possible ways to display content from a virtualized graphics environment:

- Rely on the virtual machine monitor (VMM) or PF driver to composite rendered surfaces from different VMs;
- Assign a display engine exclusively to a virtual function (VF), preferably a trusted VF from the VMM perspective, and use the corresponding planes/pipes to output data;
- Assign a display pipe or plane to a VF.

The graphics virtualization infrastructure is exposed to system software by the Single Root I/O virtualization standard (SR-IOV), of the PCIe standard. The exposure is accomplished using a PCIe device Physical function that includes the SR-IOV Extended Capability structure, within the PCIe Extended Capabilities list.

5.2.2

GuC

Graphics Micro Controller (GuC) is an embedded micro-controller in the graphics subsystem that is designed to perform graphics workload scheduling on the various graphics parallel engines. In this scheduling model, host software submits work through one of the 256 graphics doorbells, and this invokes the micro-kernel running on the GuC core to perform the scheduling operation on the appropriate graphics engine.

Scheduling operations include determining which workload to run next, submitting a workload to a command streamer, pre-empting existing workloads running on an engine, monitoring progress, and notifying host SW when work is done. To perform these actions, the GuC requires access to a wide range of assets within the graphics subsystem. The GuC has access to the entire graphics device MMIO register space to allow it to schedule work on any graphics engine.

5.2.2.1

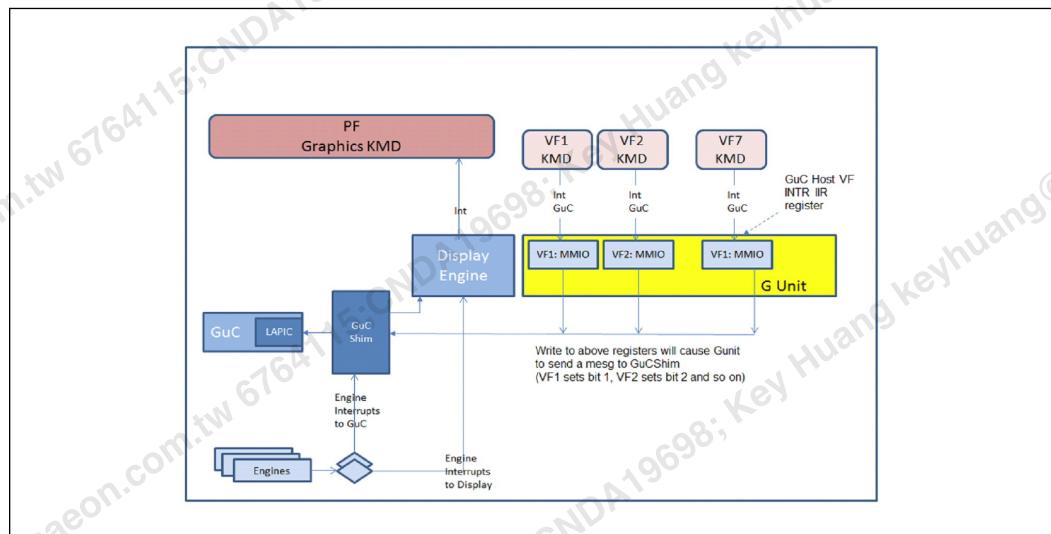
Virtual Function Communication with GuC

The Virtual Function (VF) software stack needs to be able to communicate with the GuC, for example to execute VM assigned task shown in Figure 5. This communication occurs via the VFs a GuC interrupt path (that is, Host2GuC path). Similarly, the VF software stack may require some services from the PF software stack.

An example communication sequence is as follows:

- VF Kernel Mode Driver (KMD) requires services from the PF stack.
- VF Kernel Mode Driver (KMD) writes to the VF-GuC-Interrupt MMIO register with a pre-defined message.
- The MMIO write triggers an interrupt to the GuC.
- The GuC firmware interrupt routine executes and inspects the MMIO register.
- GuC firmware uses message content to determine whether GuC or PF is the intended message target:
 - If GuC is the target, then GuC firmware consumes the message and provides the appropriate service; or
 - If PF software is the target, then GuC generates an interrupt to the PF. PF provides the appropriate service and communicates back to GuC upon completion.
- GuC generates an interrupt to the VF, to indicate that the service is completed.

Figure 4. Virtual Function to Physical Function Communication through GuC

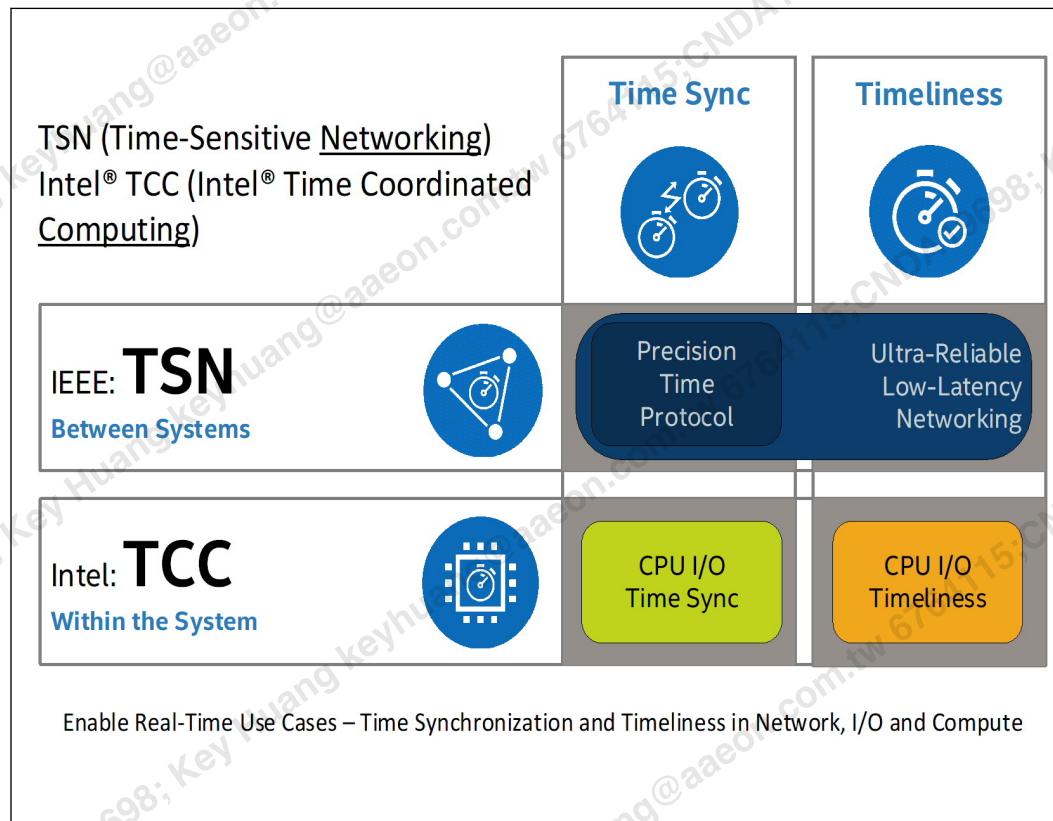


6.0 Intel® Time Coordinated Computing (Intel® TCC)

6.1 Introduction

Intel® Time Coordinated Computing (Intel® TCC) is ushering in a new era of coordination of computation scheduling to reduce jitter and improve performance of time-sensitive applications. Intel® TCC is not an IP block but a set of capabilities available across multiple IP blocks of the processor. Intel® TCC enhances performance along two vectors: Time Synchronization and Timeliness. Timeliness is traditionally referred to as “Real-Time” systems that are focused on the optimization. Time Synchronization provides a hardware mechanism to precisely determine how various IP specific clocks are related. Real-Time provides a hardware mechanism to minimize the latency of data packets from one IP block to another IP block. This chapter describes the key features and requirements that compose Intel® TCC, split into the respective performance vectors. For each feature, the motivation, description, software interface (if any), hardware dependencies (if any) and formal requirements are listed.

Figure 5. Intel® TCC Features within System and TSN between Systems



6.2

Intel® Time Coordinated Computing (Intel® TCC) Features

Intel® TCC helps real-time applications meet performance metrics, such as worst-case execution time (WCET). In addition, it keeps all software and hardware time-synchronized. Intel® TCC performance is measured by the temporal determinism afforded to the critical tasks. The following section outlines the platform capabilities that enable temporal determinism.

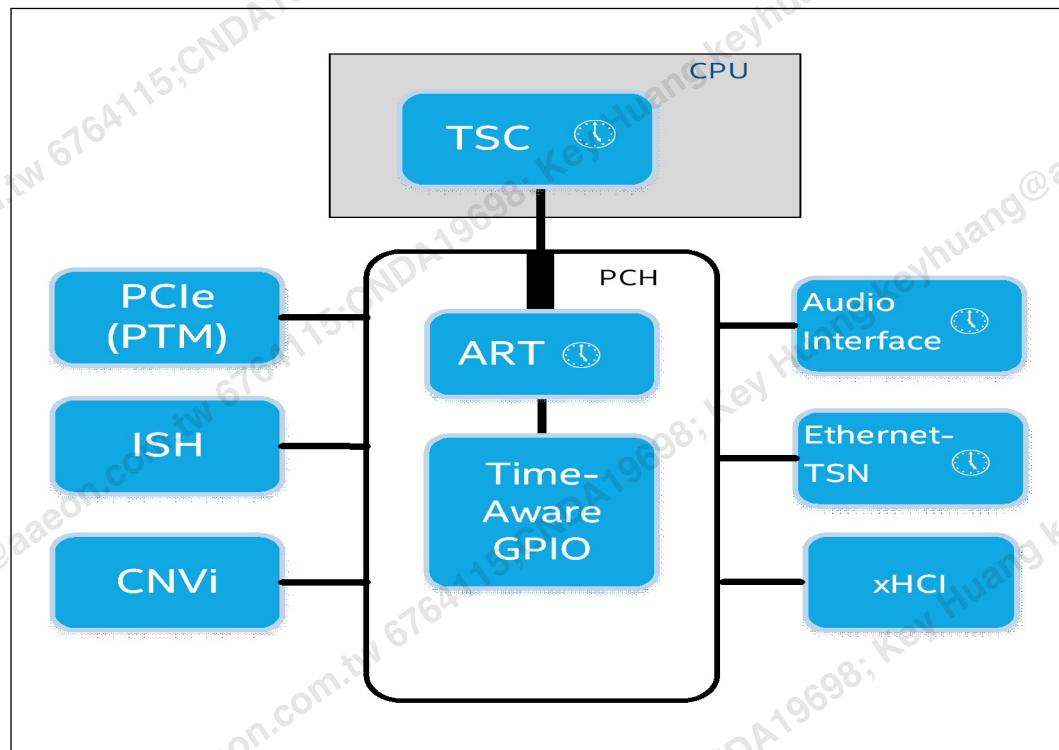
6.2.1

Time-Synchronization Support Features

The processor provides a common timekeeping framework, based on the Always Running Timer (ART) defined in Intel® 64 and IA-32 Architectures Software Developer's Manual. ART runs at the core crystal clock frequency. The ART clock is at 38.4MHz. This makes it possible for software to calculate the precise time relationship between numerous subsystems, including the CPU's timestamp counter (TSC), the network device, Time-Aware GPIOs, and other various IPs. This processor support makes deep sub-microsecond time-correlation / synchronization possible, which is a requirement of coordinated computing, sensing, and actuation.

Processor Time-Synchronization Support provides the following:

- Global time reference based on Always Running Timer (ART)
- IEEE Std 802.1AS, the TSN standard for time synchronization across wired Ethernet network
- Global time synchronization for the following local time bases with respect to ART:
 - Ethernet Time-Sensitive Networking (TSN)
 - High Definition Audio
 - PCI Express Root-ports Precision Time Measurement (PCIe* PTM)
 - Integrated Sensor Hub (ISH)
 - Time-Aware GPIO
 - Intel® Integrated Connectivity (CNVi)
 - xHCI Controllers

Figure 6. Platform Time-Synchronization Support

6.2.1.1 CPU Time Stamp Counter to I/O Time-Synchronization Support

The CPU Time Stamp Counter (TSC) Root in the Power Management Controller (PMC) is the global referenced time in the Time Synchronization architecture. The software can access the CPU TSC through the Read Time Stamp Counter (RDTSC) assembly instruction. RDTSC is based on the ART counter, which is the root of time in the system. The CPU TSC is derived from ART. ART is discoverable in the CPUID leaf 15H, and the ART relationship to all other clock domains is maintained in software.

The relation between the network device timestamp clock and ART (also TSC) is determined using cross-timestamp hardware. Using TSN the ART clock is extended outside of the platform. Refer to Section 5.2.1.3 for more information about IEEE Std 802.1AS network time synchronization. The relation between Audio hardware clock and ART (also TSC) is determined using crosstimestamp hardware. Refer to Section 5.2.1.4 for more information about audio crosstimestamping. The Time-Aware GPIO interface logic is driven by ART. Edge events (one shot and pulse train) can be sampled or driven with respect to the ART clock. Refer to Section 5.2.1.5 for details on Time-Aware GPIO.

6.2.1.2 Off-Chip Time-Synchronization Support via PCIe* PTM

Besides supporting known hardware, ART also extends to PCIe peripherals using Precision Time Measurement (PTM). PTM provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

6.2.1.3

IEEE Std 802.1AS Network Time-Synchronization Support

The IEEE Std 802.1AS TSN standard extends time synchronization across multiple platforms for time-sensitive applications such as audio and video when these platforms are Ethernet connected. The integrated Ethernet MAC supports the IEEE Std 802.1AS generalized Precision Time Protocol (gPTP) event messages for network path delay measurement between two time-aware systems.

Time Synchronization utilizes the standard IEEE Std 802.1AS capability as the base feature to enable cross-platform time synchronization. At the high level, the IEEE Std 802.1AS implements the following:

- Select the best clock source on the network using the algorithm specified in IEEE Standard 802.1AS.
- Determine the propagation delay through the network.
- Calculate the offset between the selected clock source and the local clock. The IEEE Std 802.1AS timer runs on its Local Time base. It supports a 38.4MHz crystal oscillator clock determined by a pin-strap based on platform configurations where it does not require any PLL to be running. The crystal oscillator continues running when IEEE Std 802.1AS time synchronization is enabled such that a valid time stamp is always available when gPTP event messages are transmitted or received.

6.2.1.4

Time-Aware GPIO

The PCH has two Time-Aware GPIO (TGPIO) controllers. Each controller can be independently configured to generate or capture timestamped events. TGPIO events are timestamped using the Always Running Timer (ART) clock.

Refer to Section 16.2.7 (RDC #[626817](#)) for detailed information on TGPIO.

6.2.2

Real-Time Features for I/O

The processor provides hardware mechanisms to improve the worst-case, which aims to put an upper bound on the latency for data coming into the system. The following features are required to provide a bounded latency for incoming transactions.

6.2.2.1

Upstream Virtual Channels

The processor provides support for upstream virtual channels through the processor fabric. I/O devices are expected to make use of the PCIe base specification definition around quality of service mechanisms for data movement, specifically those related to Traffic Class. Upstream transactions that are differentiated by Traffic Class have the ability to be mapped to a separate virtual channel in an attempt to provide a low latency path to the coherent domain. The PCH PCIe* controller supports 1 virtual channel on Ethernet-TSN controller.

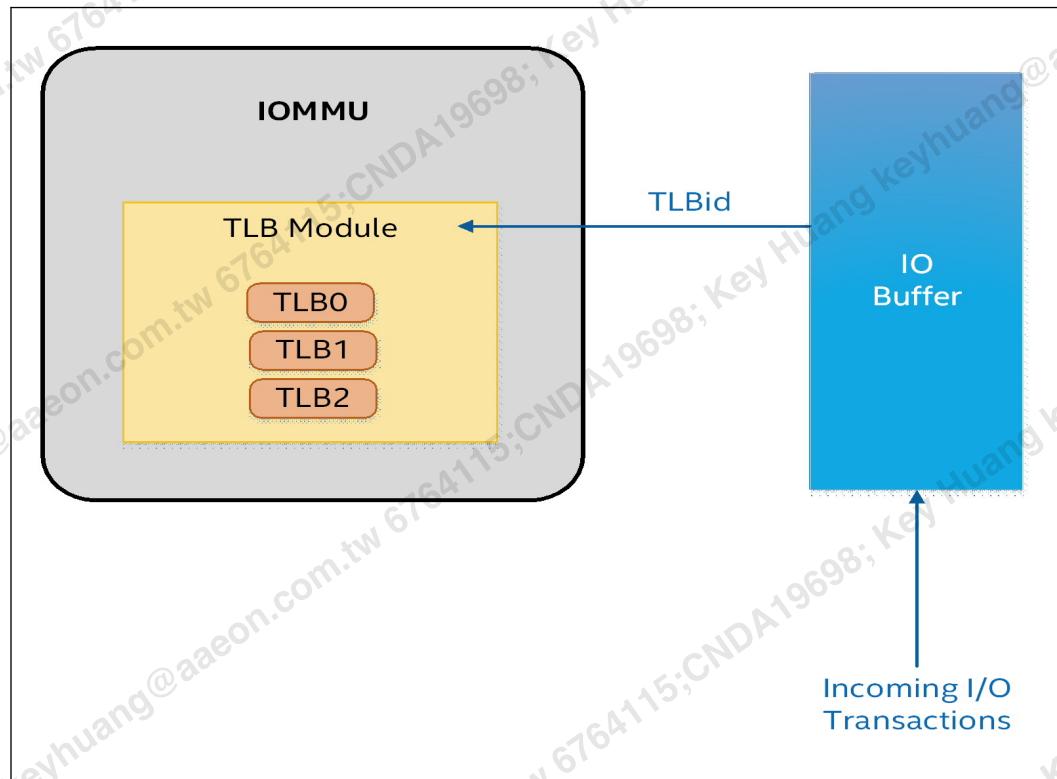
6.2.2.2

Dedicated IOTLB

The processor provides support for a dedicated I/O Translation Lookaside Buffer (IOTLB) to cache critical address translations for real-time I/O traffic. When workload consolidation is implemented with virtualization, the I/O transactions of real-time workloads running in a virtual machine are subject to increased jitter as a result of a page walk by the I/O Memory Management Unit (IOMMU). To avoid additional page walk latency on all I/O transactions, an IOTLB is implemented in the IOMMU to cache the guest physical address to host physical address translation. There are no Quality

of Service (QoS) mechanisms available on this cache, and therefore translations for time-critical addresses are subject to eviction as a result of concurrent best effort traffic.

Figure 7. IOTLB Usage



By providing a dedicated IOTLB for time-critical transactions, it is possible to minimize the additional latency and jitter previously introduced by the IOMMU. The processor specifies a TLBid based on the PCIe traffic class used, avoiding contention on the cache resources from concurrent best effort traffic.

6.2.3

Real-Time Features for Processor

The processor provides mechanisms to promote the reduction of execution jitter, leading to a more deterministic computing environment.

6.2.3.1

Multiple Outstanding MMIO

The processor provides support for tracking multiple downstream non-posted transactions simultaneously targeting the Memory Mapped I/O subsystem.

6.2.3.2

Alignment Check Exception on Split Lock

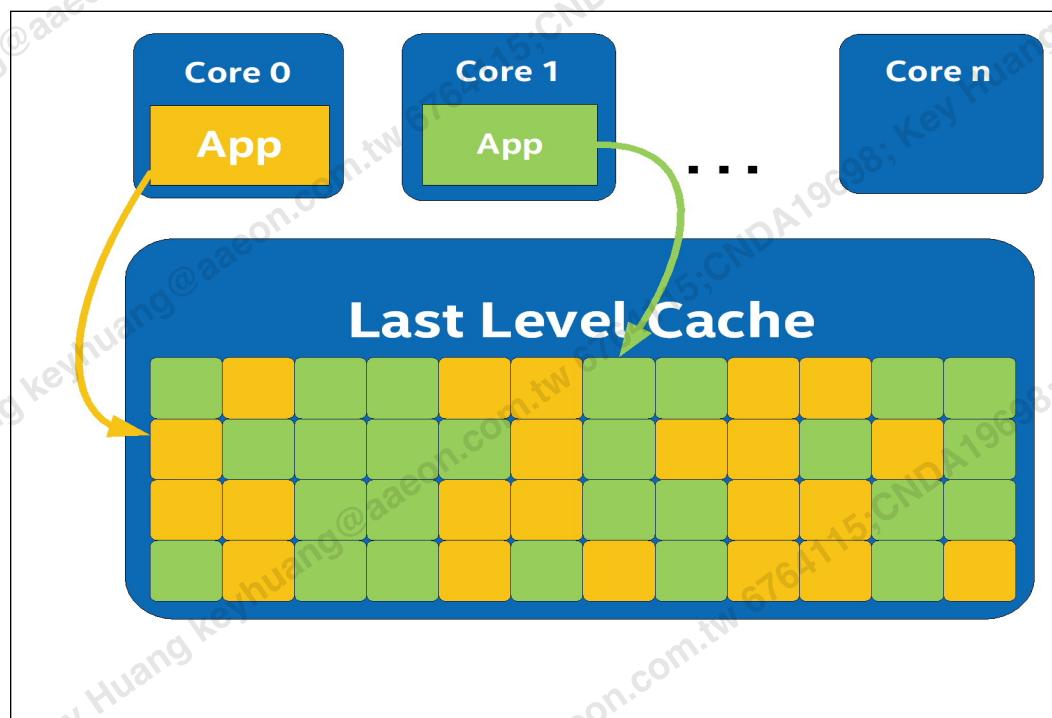
The processor provides support to generate an Alignment Check Exception (#AC) when an application attempts to issue a split lock. When the LOCK prefix is used on an unaligned operand, there is the potential for the operand to span multiple cache lines. In the case where an atomic operation is necessary across two cache lines, a bus lock

is executed. A bus lock stops all cores and I/Os from initiating transactions, resulting in an increase in latency. This increased latency can be significant, and many real-time applications cannot tolerate the jitter that a split lock introduces.

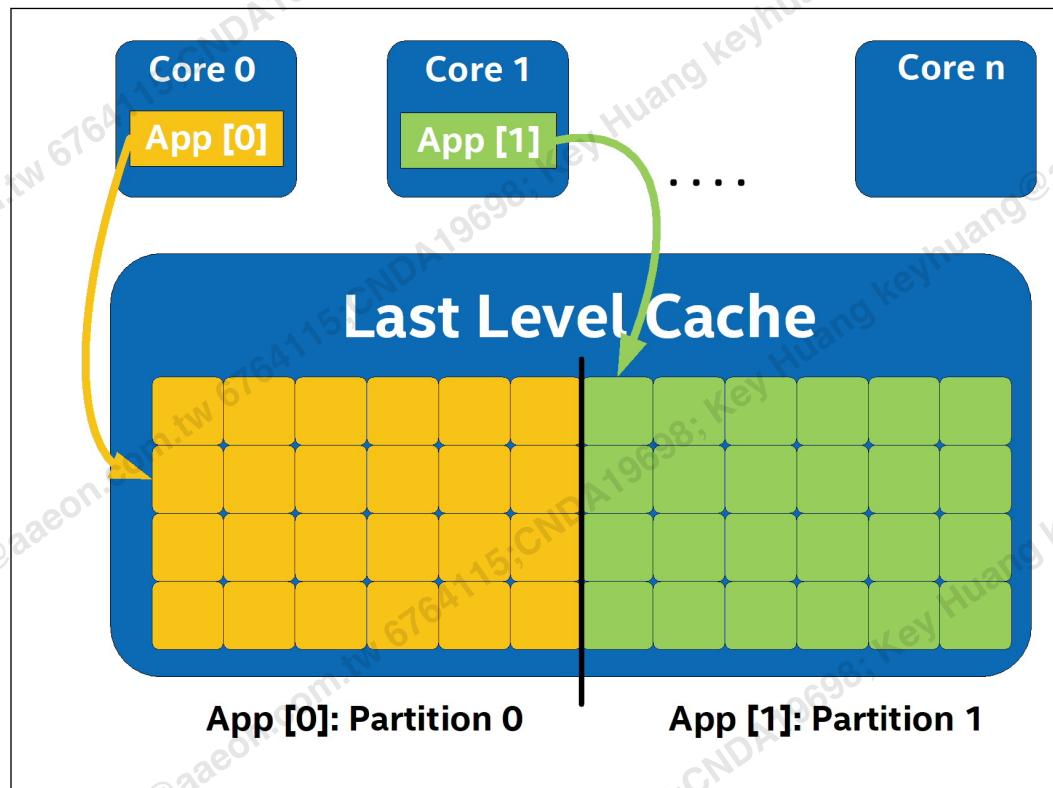
6.2.3.3 L2 and L3 Cache QoS

The processor provides support for Cache Allocation Technology (CAT), a Quality of Service (QoS) feature under the Intel® Resource Director Technology (Intel® RDT) portfolio. A model specific, non-architectural version of L3 CAT is supported. Support for this feature will not be enumerated via CPUID leafs as indicated in the Intel® Software Developers Manual. For details on how to use L3 CAT, including information on the number of classes of service, selecting the active class of service, and more, please consult the Cache Allocation Technology chapter in the Real Time Tuning Guide for Raptor Lake-P Processors. CAT helps address shared cache resource contention by providing software control of where data is allocated into the Level 2 (L2) cache and L3 cache, enabling isolation and prioritization of key applications. Without CAT, cache resources are shared between applications.

Figure 8. LLC without Cache QoS



With CAT, cache resources can be partitioned. This partitioning leads to improved performance determinism.

Figure 9. LLC with Cache QoS

6.3

Intel® Time Coordinated Computing Tools (Intel® TCC Technology)

Intel® TCC Tools provide application and middleware support, including APIs, tools, and sample applications that enable developers to access certain Intel® TCC features. Intel® TCC Tools also enable developers to analyze the behavior of real-time applications. For more information about Intel® TCC Tools beyond the scope of this document, see the Intel® TCC Tools product page listed in Intel® TCC Tools Product Page: <https://software.intel.com/content/www/us/en/develop/tools/time-coordinated-computing-tools.html>.

For supported OS refer to (RDC #730563), Raptor Lake-P Platform Gold Deck

7.0 Flexible High Speed Input/Output (I/O)

7.1 Overview

Flexible Input/Output (I/O) is a technology that allows some of the PCH High Speed I/O (HSIO) lanes to be configured for connection to a Gigabit Ethernet (GbE) Controller, a PCIe* Controller, an Extensible Host Controller Interface (XHCI) USB 3.2 Controller, TSM Controller or an Advanced Host Controller Interface (AHCI) SATA Controller. Flexible I/O enables customers to optimize the allocation of the PCH HSIO interfaces to better meet the I/O needs of their system.

NOTE

For any capability not mentioned in this section, refer to Section 1.3 of External Design Specification (EDS) Volume 1 (RDC #626817).

7.2 Flexible HSIO Lane Multiplexing

Figure 10. Flexible HSIO Lane Multiplexing in Raptor Lake -P

Flex HSIO Lane	HSIO Type and Lane		
0	USB 3.2 Gen 1x1/2x1 #1		PCIe * #1
1	USB 3.2 Gen 1x1/2x1 #2		PCIe * #2
2	USB 3.2 Gen 1x1/2x1 #3		PCIe * #3
3	USB 3.2 Gen 1x1/2x1 #4		PCIe * #4
4	PCIe * #5		
5	PCIe * #6		
6	PCIe * #7	Ethernet-TSN	GbE
7	PCIe * #8	Ethernet-TSN	GbE
8	PCIe * #9	GbE	UFS
9	PCIe * #10	1x2	Lane 0
10	PCIe * #11	SATA 0	
11	PCIe * #12	SATA 1	

The 12 Flexible HSIO Lanes [11:0] supports the following configurations:

Up to 12 PCIe* Lanes

- A maximum of 6 PCIe* Root Ports (or devices) can be enabled.
- PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), and 9-12 (PCIe* Controller #3) must be individually configured.

Up to two SATA Lanes

- A maximum of two SATA Ports (or devices) can be enabled.

Up to three GbE Lanes

- A maximum of one GbE Port (or device) can be enabled.

Up to 2 Ethernet Ports

- A maximum of 1 Ethernet-TSN port (or device) can be enabled.
- Raptor Lake-P supports concurrent Ethernet and Ethernet-TSN port. This makes 1 port of Ethernet 1Gb/Intel vPro® Technology capable Ethernet and 1 port of 2.5Gb/TSN capable Ethernet. In total, two Ethernet ports can be enabled at the same time.

7.2.1

Flexible I/O Lane Selection

HSIO lane configuration and type is statically selected by soft straps, which are managed through the platform Flash Image Tool, available as part of Intel® CSE releases. Refer to the SPI Programming Guide documentation for details on how to configure the Flexible I/O lanes via soft straps.

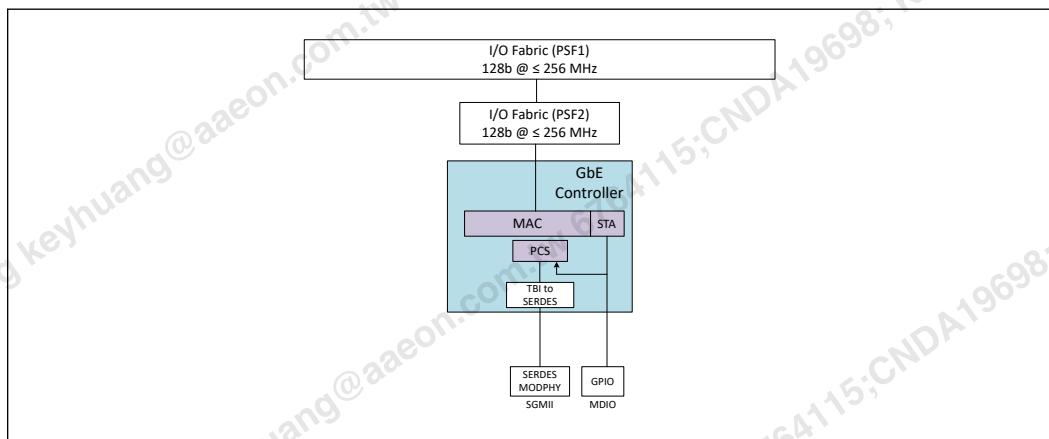
8.0 Gigabit Ethernet Controller and Time-Sensitive Networking

8.1 Overview

This section describes the behavior of the Gigabit Ethernet (GbE) Time-Sensitive Networking (TSN) controller that resides in PCH. The GbE-TSN controller can operate at multiple speeds, 10/100/1000 & 2500 Mbps Serial Gigabit Media-Independent Interface (SGMII) and in either full duplex or half duplex mode. Each integrated TSN Ethernet Media Access Controller (MAC) has a unique 48-bit MAC Address. This MAC Address is located in a BIOS Sub-Region and is assigned by the customer using the Capsule Update method which runs in an OS.

The figure below shows the location in the PCH.

Figure 11. GbE-TSN Controller Placement



The GbE-TSN controller is accessed by the IA Processor cores through system software via PCH IO Fabric (PSF2 and PSF1) and supports a SGMII interface.

The MAC has an IEEE Std 802.3 Station Management (STA) Entity that is accessible to software via the Memory Mapped IO (MMIO) registers to control the associated MDIO interface. See IEEE Std 802.3, Clause 22 and Clause 45 for MMIO registers. The Physical Coding Sublayer (PCS) module provides the sublayer circuitry between the GMII of the MAC and the Ten Bit Interface (TBI) of the SGMII SERrial-DESerial (SerDes) circuitry. See IEEE Std 802.3 Clause 35 for GMII and Clause 36 for TBI.

8.2 Features Description

The GbE-TSN controller features listed in this section.

8.2.1

Ethernet Features Description

The GbE-TSN controller instances supports the following Ethernet features:

- 10Mbps/100Mbps/1Gbps/2.5Gbps SGMII mode through SERDES interface.

NOTE

Auto-negotiation between 10Mbps/100Mbps/1Gbps and 2.5Gbps is not supported natively by the controller.

NOTE

The maximum line rate for 2.5Gbps is TBD (To Be Determined) but is expected to be less than 2.0Gbps for standard Ethernet frame sizes and less than 2.5Gbps for jumbo Ethernet frame sizes.

- MDIO (station management) interface.
- Wake on LAN (WOL) is not supported by the Gigabit Ethernet (GbE) Time-Sensitive Networking (TSN) controller that resides in the PCH. This behaviour is caused by the GBE_INT signal being unable to signal a wake event to the Power Management Controller (PMC).
- 4 TX queues and 6 RX queues with separate DMA channels and interrupts. Each TX/RX queue is 4KB for storing at least two normal packets with total of 40KB memory (TX+RX). Each queue size is programmable with TX queue size not to exceed 16KB and RX queue size not to exceed 24KB.

NOTE

The MTL Receive FIFO Size (RXFIFOSIZE) bits [4:0] in register MAC_HW_FEATURE1 (MMIO offset 120h) advertises 32 KB as the allowable RX FIFO size, while the implemented size is 24 KB. If software allocation of RX queues exceeds this amount, then data attempted to be queued greater than 24 KB will be lost. Software should not allocate an aggregate size of more than 24 KB for MTL RX queues.

- Supports normal (1518/1522 bytes) and jumbo (9018 bytes) packets:
 - On the receiving side, supports both cut-through and store and forward modes.
 - On the transmitting side, supports only store and forward mode.
- Support for TCP/IP Offloading:
 - Checksum Offload Engine (COE) that does Checksum insertion (on TX path) and detection (on RX path) for TCP/UDP/ICMP segments encapsulated in IPv4/IPv6 datagrams.
 - TCP Segmentation Offload (TSO) Engine where large TCP packets are split into multiple small packets to save application bus cycles. 4 TX DMA Channels with separate 1KB memory (256 bytes per channel).
- Double VLAN support:
 - Insertion, replacement, or deletion of up to four VLAN tags on TX path
 - Packet filtering (layer-2) and stripping based on any one of four VLAN tags on RX path

- MAC Management Counters (MMC) for gathering statistics on the received and transmitted packets. Interrupts are generated for various events.
 - On TX: Jabber Timeout, No Carrier or Loss of Carrier, Late Collision, Packet Underflow, Excessive Deferral and Excessive Collision
 - On RX: CRC error, Runt packet (shorter than 64 bytes), Alignment error (in 10/100Mbps only), Length error (non-Type packet only), Out of Range (non-Type packet only, longer than 1518 bytes), GMII_RXER Input error
- Low power management
 - IEEE Std 802.3az-2010 Energy Efficient Ethernet (EEE) with automatic entry/exit when link is Idle – Low Power Idle mode. Both link TX/RX clocks can be clock gated.
- RX Filtering
 - 64 Address (SA/DA) based layer-2 perfect and Hash table filtering
 - 4 VLAN tag layer-2 filters
 - Two Layer-3 and Layer-4 frame filters
- Functional Level Reset (FLR)
- FSM protection
 - 1–3 bits errors in the data and address
- Timeout on certain interfaces
 - Control and Status Register (CSR) Interfaces, MDIO Interfaces, AXI Primary Interfaces, and AXI Secondary

NOTE

The Split Headers (SPH) function is not supported by the processor. Platform firmware & software shall not set any DMA_CH[0:7]_CONTROL.SPH register field to 0x1.

8.2.2 TSN Features Description

TSN is a set of IEEE standards that are intended to ensure quality transmission of the time sensitive data over Ethernet networks. TSN standards are governed by an IEEE Std 802.1 task group driven by, in part, Avnu Alliance which is a consortium of organizations involved and invested in deterministic Ethernet Technology.

Table 6. TSN IEEE Standards

IEEE Standard	Description
IEEE Std 1588™-2008 v2	Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
IEEE Std 802.1AS	A specific profile of IEEE Std 1588-2008. IEEE Std 802.1AS specifies the generalized Precision Time Protocol (gPTP). It provides a Layer 2 time synchronizing service
IEEE Std 802.1Qav 2009	Forwarding and Queueing Enhancements for Time-Sensitive Streams, which specifies the Credit Based Shaper

continued...

IEEE Standard	Description
IEEE Std 802.1Qbu 2016	Frame Preemption. It allows a Bridge Port to suspend the transmission of non time critical frames while one or more time critical frames are transmitted
IEEE Std 802.3br 2015	Interspersed Express Traffic (IET)
IEEE Std 802.1Qbv 2015	Enhancements for Scheduled Traffic. It specifies time aware queue draining to schedule the transmission of frames relative to a known time scale

In addition to IEEE Standards above, the GbE-TSN controller instances supports the following TSN features.

- Time Based Scheduling (TBS)
 - Time deterministic transmission of the packet according to per packet transmit time specified by users.
- IEEE Std 1588TM-2002/2008 timestamp support for PTP packets
 - 80-bit internal system timer that runs at 200MHz for high-precision one-step time stamping
 - 64-bit ART timer that runs at 19.2MHz with Time Synchronization support for local and system timer correlation
 - The ART timer and system timer values are captured with precision less than 5ns for timing correlation
- GPIO Auxiliary Timestamp Trigger input (IEEE Std 802.1AS)
- GPIO based Pulse Per Second output with programmable pulse width
- Each Control List of 1K entries for all Tx queues. 32x128(x8) memory for Control List to support IEEE Std 802.1Qbv
- Provision to route traffic on low latency on low fabric channel with traffic class-based routing. Two virtual channels and traffic classes (TC) are supported. All express traffic is mapped to Virtual Channel-1(VC1) and best effort is mapped to Virtual Channel-0(VC0). Each queue is independently mapped to any of the supported VC/TC.

8.3

GbE Time-Stamping Logic

The Precision Time Protocol (PTP) over Ethernet is described in the IEEE Std 1588-2002 and 2008 versions. The subsystem provides the following features:

- IEEE Std 1588-2002 and 2008 formats
- Provides an option to take time snapshots of all packets or only PTP type packets
- Provides an option to take time snapshots of only event messages
- Provides an option to take the time snapshot based on the clock type: ordinary; boundary; end-to-end transparent; peer-to-peer transparent
- Provides an option to select the node to be a primary clock or secondary clock for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in the packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format
- Two time stamp sources, as follows:

1. External timestamp
2. Internal timestamp which is selected by software

8.4

GbE Cross-Timestamp Logic

Additional logic is included in the GbE design to provide time synchronization between the 64-bit timer Always Running Timer (ART) and the 80-bit system timer in the GbE-TSN controller.

When system software sets the cross-timestamp enable bit in the GbE ART MDIO register, it captures simultaneous snapshots of the values of the GbE system timer and the ART. System software can then read the captured time values to establish a relationship between ART and GbE system timer; When the GbE system timer value is X, the ART value is Y.

8.5

External Interfaces

The selection for the GbE-TSN controller is Serial Gigabit Media-Independent Interface (SGMII).

The PCH does not use any of the Precision Time Protocol (PTP) capture capabilities that may exist in the external PHY component. All the PTP events and timestamps are triggered in the MAC portion of the subsystem.

8.5.1

Serial Gigabit Media-Independent Interface (SGMII)

Serial Gigabit Media-Independent Interface (SGMII) is a de-facto industry standards for achieving Ethernet LAN speeds of 10Mbps, 100Mbps, 1Gbps and 2.5Gbps. It consists of two sets of Current-Mode Logic (CML) differential signal using one of the multiplexed PCH ModPHY lanes. The design embeds the SGMII transmit clock in the transmit data and expects the SGMII receive clock to be embedded in the receive data. This eliminates four of the standard GMII interface pins. For the controller's IEEE Std 802.3 Physical Sublayer configuration and management, it also provides two CMOS Management Data Input/Output (MDIO) interface signals. SGMII provides a reduced-pin implementation of GMII (IEEE Std 802.3, Clause 35) which would require 25 single-ended signals plus the two MDIO interface signals.

8.5.2

Management Data Input/Output (MDIO)

The External PHY can be accessed and configured through Management Data Input/Output (MDIO) from the GbE-TSN controller by SW/HW/BIOS. The IEEE Std 802.3 defines MDIO Management interface which serves to access the Management registers of IEEE Std 802.3 compliant devices. This is a two-line interface including MDC (clock) and MDIO (bidirectional data).

NOTE

The interface supports MDIO operation as defined in IEEE Std 802.3 Clause 45 except at a signal voltage of 1.8V, not 1.2V.

8.6

Signal Description

8.6.1 SGMII Signals

Table 7. SGMII GbE LAN Signals

Pin	Signal Name ¹	Type (Voltage Domain) ¹	Direction	Description
EL10	PCIE7_TXP / GBE_SGMII_TXP	CML differential signal (1.05V)	Output	Transmit P&N of the serial differential output
EL11	PCIE7_TXN / GBE_SGMII_TXN			
EG4	PCIE7_RXP / GBE_SGMII_RXP	CML differential signal (1.05V)	Input	Receive P&N of the serial differential input
EG6	PCIE7_RXN / GBE_SGMII_RXN			
<i>Note:</i>				
1. Refer to Section 6.0 for a description of how these signals are routed by the ModPHY lanes.				

8.6.2 MDIO Signals

Table 8. MDIO Signals

Pin	Signal Name	GPIO Type (Voltage Domain) ¹	Direction	Description
ER33	GPP_F17 / GBE_MDC / THC1_SPI2_RST#	CMOS (1.8V)	Output	Management Data Clock This clock signal is driven by the LAN controllers to clock the serial MDIO data. The clock period is programmable.
ET36	GPP_F18 / GBE_MDIO / THC1_SPI2_INT#	Open Drain (1.8V)	Input/Output	Management Data Input Output This signal is driven by either the LAN controller or the external PHY/Switch component during the MDIO transaction.
<i>Note:</i>				
1. The signals should be configured to 1.8V using the multiplexed GPIO's Individual Voltage Select soft strap.				

8.6.3 Miscellaneous Signals

Table 9. Miscellaneous Signals

Pin	Signal Name	GPIO Type (Voltage Domain) ¹	Direction	Description
EY53	GPP_S1 / GBE_INT / SNDW0_DATA / I2S1_SFRM	CMOS (1.8V)	Input	Interrupt This input signal is driven by the external SGMII PHY device.
EV53	GPP_S0 / GBE_AUXTS / SNDW0_CLK / I2S1_SCLK	CMOS (1.8V)	Input	Auxiliary Time Stamp Trigger This edge-sensitive input signal triggers the storing of the time stamp into a 4x64 deep FIFO on its rising edge.

continued...

Pin	Signal Name	GPIO Type (Voltage Domain)	Direction	Description
				<i>Note:</i> This signal may also be called External Time Stamp Trigger (EXTTS) on other platform's documentation.
FC50	GPP_S3 / GBE_PPS / SNDW1_DATA / DMIC_DATA_0 / I2S1_RXD	CMOS (1.8V)	Output	Pulse-Per-Second This output signal is generated as a pulse by the LAN controller each time its system timer indicates a new "seconds" value.

8.7

GbE-TSN Interrupts and Message Signaled Interrupt

The GbE-TSN subsystem has the following 13 interrupts. These interrupts are routed through the Message Signaled Interrupt (MSI). The MSI has separate Vector Number. The GbE-TSN interrupts and MSI Vector Number are tabulated in the table below.

Table 10. GbE-TSN interrupts and Message Signaled Interrupt (MSI) Vector Number

No	Interrupt Name	Direction	Description	MSI Vector No
1	Queue_TX0_IRQ	O	Per channel Transmit signal to host system	5'b00001
2	Queue_TX1_IRQ	O		5'b00011
3	Queue_TX2_IRQ	O		5'b00101
4	Queue_TX3_IRQ	O		5'b00111
5	Queue_RX0_IRQ	O	Per channel Receive signal to host system	5'b00000
6	Queue_RX1_IRQ	O		5'b00010
7	Queue_RX2_IRQ	O		5'b00100
8	Queue_RX3_IRQ	O		5'b00110
9	Queue_RX4_IRQ	O		5'b01000
10	Queue_RX5_IRQ	O		5'b01010
11	Low Power Idle (LPI) Interrupt	O	LPI RX exit interrupt output. This signal is high when the MAC receiver exits the LPI state. This is used for EEE and CSR clocks can be gated.	5'b11100
12	MAC_IRQ	O	Interrupt signal to the host system – generated by the MAC	5'b11101
13	PCS Interrupt	O	Interrupt signal to the host system – generated by the PCS	5'b11110

8.8

Supported System Configurations

The table below lists all the supported configurations, operating mode, and link partners for the LAN controllers. Selecting the desired PHY and system configuration is determined at power on through the use of soft strap and register configuration.

Table 11. Supported System Configurations

Connection	Speed	Electrical Interface	Third Party PHYs ¹
10BASE-T 100BASE-TX 1000BASE-T	10 Mb/s 100 Mb/s 1 Gb/s	SGMII	Marvell* 88E1512 MaxLinear* GPY115 TI* DP83867
10BASE-T 100BASE-TX 1000BASE-T 2.5GBASE-T	10 Mb/s 100 Mb/s 1 Gb/s 2.5 Gb/s	SGMII	Marvell* 88E2110 MaxLinear* GPY211 MaxLinear* GPY215
<i>Note:</i>			
1. Intel strongly recommends that only the PHYs listed be used in platform designs. Firmware and software incompatibilities may occur between other GbE PHYs and Intel's BKC due to per-vendor or per-model PHY-specific programming requirements.			

8.9 Registers

Please refer to Section 10.0 for a description of the registers associated with this section.

8.10 BIOS Sub-Region Capsule Update

The Raptor Lake-P BIOS has the following Ethernet TSN sub-region configuration support for the Raptor Lake PCH-P port.

- MAC address region

The Raptor Lake-P BIOS has the following Ethernet TSN sub-region configuration support for the Raptor Lake PCH-P port. Firmware and BIOS Utilities (FBU) is the configuration tool for provisioning data into the BIOS sub-regions. The latest open-source FBU release package can be downloaded from [iotg-fbu](#) page at the GitHub* software development platform. The Capsule Update process on the target are available through OS, in EFI Shell, For EFI shell, use CapsuleApp.efi to update the capsule. The CapsuleApp.efi is available in [GitHub*](#) page.

Refer to the MAC Address Programming for IoT Client Platforms, RDC #[633243](#), to understand on the command used to program the MAC Address via Capsule Update method and how to stitch Binary into IFWI image. The following table lists the configuration line format definition settings and definitions across Javascript* Object Notation (JSON).

Table 12. Configuration Line Format Definition Setting and Definition Across JSON

Variable Name (in String)	Variable Format (Decimal or Hexadecimal)	Variable Size (Always 4 bytes)	Variable Value (Decimal Value without Quotes or Hexadecimal Value with quotes)
"Version"	"DECIMAL"	4	1
"Version"	"HEXADECIMAL"	4	"00000001"

8.10.1 Common Configuration Setting and Definition Across JSON

Total number of ports for configuring the JSON file ('X' - minimum: 0; maximum: 4):

```
["NumPorts", "DECIMAL", 4, X],
```

To configure the subsequent JSON setting for Raptor Lake PCH-P Ethernet TSN port:

```
["BDF", "HEXADECIMAL", 4, "000F4000"],
```

To enable port configuration from the sub-region JSON file:

```
["PortValid", "DECIMAL", 4, 1],
```

To disable port configuration from the sub-region JSON file:

```
["PortValid", "DECIMAL", 4, 0],
```

8.10.2 MAC Address Sub-Region Configuration

This region configuration applies to the Raptor Lake PCH-P Ethernet TSN port

Configure the MAC address for the specific port (e.g. c6:70:09:b1:54:a9):

```
["MacAddressLow", "HEXADECIMAL", 4, "B10970C6"],
```

```
["MacAddressHigh", "HEXADECIMAL", 4, "0000A954"],
```

8.11 References

Specification	Location
IEEE Std 802.3-2015 Standard for Ethernet	https://standards.ieee.org/standard/802_3-2015.html
IEEE Std 802.1 AS-2011 Standard for Timing and Synchronization for Time-Sensitive Applications	https://standards.ieee.org/standard/802_1AS-2011.html
IEEE Std 1588 2008 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems	https://standards.ieee.org/standard/1588-2008.html
IEEE Std 802.1Qav 2009 Standard for Forwarding and Queuing Enhancements for Time-Sensitive Streams	https://standards.ieee.org/standard/802_1Qav-2009.html
IEEE Std 802.1Qbu 2016 Standard for Frame Preemption	https://standards.ieee.org/standard/802_1Qbu-2016.html
IEEE Std 802.3br 2016 Standard for Specification and Management Parameters for Interspersing Express Traffic	https://standards.ieee.org/standard/802_3br-2016.html
IEEE Std 802.1Qbv 2015 Standard for Enhancements for Scheduled Traffic	https://standards.ieee.org/standard/802_1Qbv-2015.html
IEEE Std 802.3az 2010 Standard for Media Access Control Parameters, Physical Layers, and Management Parameters for Energy-Efficient Ethernet	https://standards.ieee.org/standard/802_3az-2010.html

9.0 Processor and PCH Device IDs

9.1 PCH Device and Revision IDs

Table 13. PCH Device and Revision IDs

PCH Dev ID	Device Function - Device Description	Note
51ACh	D30: F4 - GbE-TSN Controller	

NOTE

For any device not mentioned in this section, refer to Section 2 of Intel®600 Series Chipset Family On-Package Platform Controller Hub (PCH) External Design Specification, Volume 1 of 2 (RDC# [626817](#)).

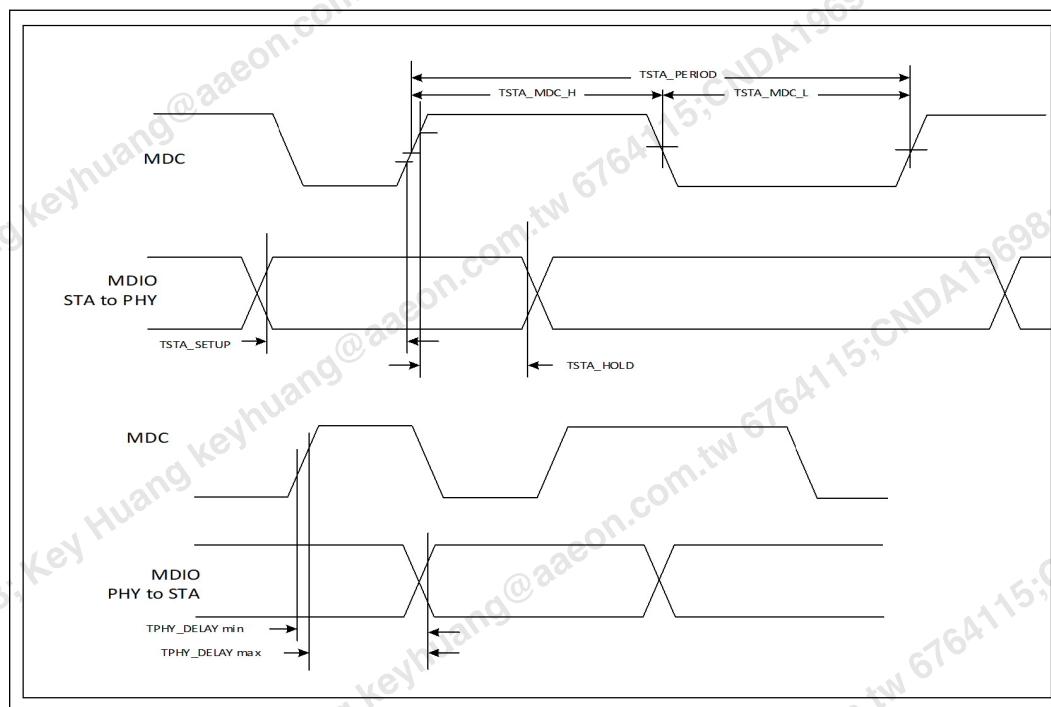
10.0 Electrical Specifications

10.1 GbE-TSN Sideband AC Specification (MDC/MDIO)

Table 14. GbE-TSN Sideband AC Specification (MDC/MDIO)

Symbol	Parameter	Minimum	Maximum	Units
TSTA_PERIOD	MDC period	400	-	ns
TSTA_MDC_H	STA MDC High	160	-	ns
TSTA_MDC_L	STA MDC Low	160	-	ns
TSTA_SETUP	STA MDC to STA MDIO setup time	10	-	ns
TSTA_HOLD	STA MDC to STA MDIO hold time	10	-	ns
TPHY_DELAY	PHY MDIO delay from STA MDC	0	300	ns

Figure 12. Timing Waveforms (MDC and MDIO Signals)



10.2 SGMII Driver AC Specification

Table 15. SGMII Driver AC Specification

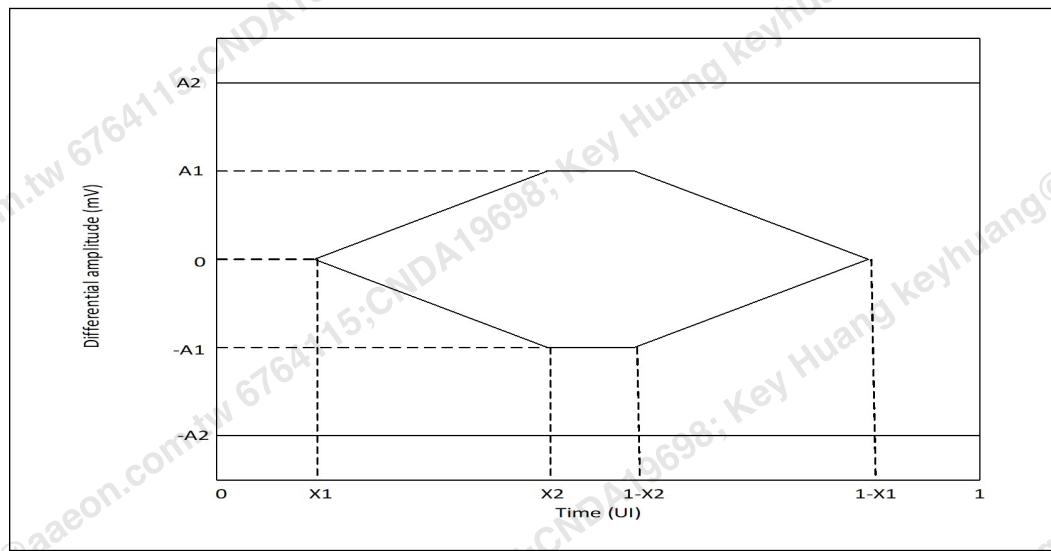
Parameter	Minimum	Maximum	Units	Notes
Bit Rate	1.25 Gb +/- 100 ppm	3.125 Gb +/- 100 ppm	Gb/ppm	
Nominal Unit Interval	320	800	ps	
Differential Amplitude Minimum and Maximum	800	1200	mVp-p	
Absolute Output Voltage Limits	-400	1800	mV	
Differential Output return loss minimum	-	-	dB	2
Output Total Jitter (near end maximum)	-	± 0.175 peak from the mean	UI	
Output Deterministic Jitter (near end maximum)	-	± 0.085 peak from the mean	UI	
Output Total Jitter (far end maximum)	-	± 0.275 peak from the mean	UI	
Output Deterministic Jitter (far end maximum)	-	± 0.185 peak from the mean	UI	

Notes:

1. The load is $100 \Omega \pm 5\%$ differential to 2.5 GHz for these measurements, unless otherwise noted.
2. For frequencies from 312.5 MHz to 3.125 GHz, the differential return loss of the driver shall exceed equation as:
 $S_{11} = -10\text{dB}$ for $312.5\text{MHz} < \text{Freq (f)} < 625\text{MHz}$, and
 $-10 + 10\log(f/625) \text{ dB}$ for $625\text{MHz} < \text{Freq (f)} < 3.125 \text{ GHz}$
(f = frequency in MHz)
3. Refer to Driver signals from [Table 7](#), Section 7.6.

Differential transitions time between 60 ps and 130 ps are recommended, measured between 20% to 80%.

The driver shall satisfy either the near-end eye template and jitter requirements, or the far-end eye template and jitter requirements.

Figure 13. Driver Template

Table 16. Driver Template Intervals

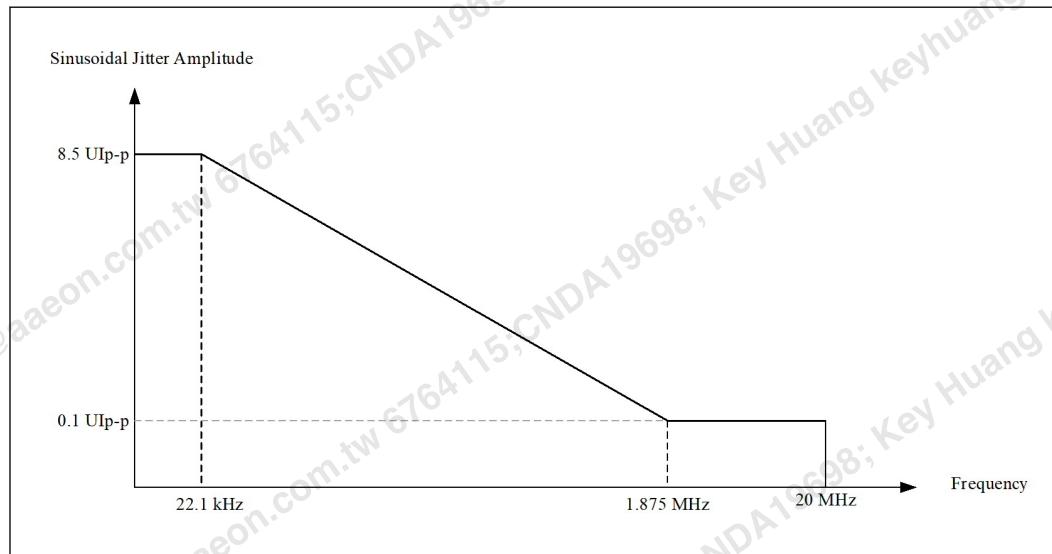
Symbol	Near-End Value	Far-End Value	Units	Symbol
X_1	0.175	0.275	UI	X_1
X_2	0.390	0.400	UI	X_2
A_1	400	100	mV	A_1
A_2	800	800	mV	A_2

10.3 SGMII Receiver AC Specifications

Table 17. SGMII Receiver AC Specifications

Parameter	Minimum	Maximum	Units	Notes
Bit Rate	1.25 Gb +/- 100 ppm	3.125 Gb +/- 100 ppm	Gb/ppm	
Nominal Unit Interval	320	800	ps	
Receiver Coupling	AC Coupled			
EEE Signal Detect deactivation time (TSD) from active to LPI quiet	-	750	ns	
EEE Signal Detect activation time (TSA) from LPI quiet to active	-	750	ns	
Return Loss Differential	-	10	dB	
Return Loss Common-Mode	-	6	dB	
Jitter Amplitude Tolerance	-	0.65	UIp-p	
Notes:				
1. The reference impedance for Return Loss measurements is 100Ω for Return Loss Differential and 25Ω for Return Loss Common-Mode.				
<i>continued...</i>				

Parameter	Minimum	Maximum	Units	Notes
2. Refer to Receiver signals from Table 7, Section 7.6.				
3. The total jitter is composed of deterministic jitter, random jitter, and sinusoidal jitter.				
4. Deterministic jitter tolerance shall be at least 0.37UI _{p-p} . Tolerance to the sum of deterministic and random jitter shall be at least 0.55UI _{p-p} . The receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of the Figure 10.				

Figure 14. Single-Tone Sinusoidal Jitter Mask**Table 18. XAUI Loss, Skew, and Jitter Budget**

	Loss (dB) ¹	Differential Skew (ps _{p-p})	Total Jitter (UI _{p-p}) ³	Deterministic Jitter (UI _{p-p}) ³
Driver	0	15	0.35	0.17
Interconnect	7.5	60	0.20	0.20
Other ²	4.5		0.10	0.10
Total	12.10	75	0.65	0.47

Notes:

1. Budgetary loss in height of eye opening.
2. Includes such effects as crosstalk noise and interaction between jitter and eye height.
3. Jitter specifications include all but 10-12 of the jitter population.

11.0 Registers

11.1 Ethernet TSN Configuration Registers Summary

This chapter documents the registers in:

- Bus 0, Device 30, Function 4 – Ethernet TSN Controller 1 - 51ACh

The Function is discovered by software as a Root Complex integrated Endpoint (RCiEP). The PCI Bus Number, Device Number, and Function Number are assigned by the PCH design and not enumerated. Because it is an RCiEP, some of the register fields are designed to be altered by BIOS for a particular system implementation.

NOTE

BIOS has the capability to disable software access to the PCI Configuration Space of this Function. When disabled, the Function returns Unsupported Request (UR) to requests to access its configuration registers.

Table 19. Summary of Bus: 0, Device: 30, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID Register (DEVVENDID) — Offset 0h on page 55	51AC0000h
4h	4	Status and Command (STATUSCOMMAND) — Offset 4h on page 55	00100000h
8h	4	Revision ID and Class Code (REVCLASSCODE) — Offset 8h on page 57	00000000h
Ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST) — Offset Ch on page 57	00000000h
10h	4	Base Address Register (BAR) — Offset 10h on page 57	00000000h
14h	4	Base Address Register High (BAR_HIGH) — Offset 14h on page 58	00000000h
18h	4	Base Address Register1 (BAR1) — Offset 18h on page 58	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) — Offset 1Ch on page 59	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) — Offset 2Ch on page 59	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) — Offset 30h on page 59	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) — Offset 34h on page 59	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) — Offset 3Ch on page 60	00000100h
40h	4	PCIe Capabilities Register (PCIECAPREG) — Offset 40h on page 60	00920010h
44h	4	PCIe Device Capability Register (DEVCAPREG) — Offset 44h on page 61	10008FC0h
48h	4	PCIe Device Control Status Register (DEVCTRLSTAT) — Offset 48h on page 61	00000000h

continued...

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64h	4	PCIe Device Capability2 Register (DEVCAPREG2) — Offset 64h on page 63	00000000h
68h	4	PCIe Device Control2 Status Register (DEVCTRLSTAT2) — Offset 68h on page 63	00000000h
80h	4	Power Management Capability ID (POWERCAPID) — Offset 80h on page 64	48030001h
84h	4	Power Management Control and Status Register (PMECTRLSTATUS) — Offset 84h on page 65	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) — Offset 90h on page 65	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) — Offset 94h on page 66	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h on page 66	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) — Offset 9Ch on page 67	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h on page 67	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) — Offset B0h on page 68	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) — Offset C0h on page 68	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) — Offset D0h on page 68	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) — Offset D4h on page 69	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) — Offset D8h on page 69	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) — Offset DCh on page 70	00000000h
E0h	4	MSI Mask Register (MSI_MASK) — Offset E0h on page 70	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) — Offset E4h on page 70	00000000h
F8h	4	Manufacturers ID (MANID) — Offset F8h on page 70	00000000h

11.1.1 Device ID and Vendor ID Register (DEVVENDID) — Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 0h	51AC0000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	51ACh RO/P	Device ID Field (DEVICEID): Device ID identifies the particular PCI device
15:0	0000h RO	Vendor ID Field (VENDORID): Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

11.1.2 Status and Command (STATUSCOMMAND) — Offset 4h

Command Register and Status Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 4h	0010000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	Detected Parity Error (DPE): Detected Parity Error
30	0h RW/1C	Signaled System Error (SSE): Signaled System Error
29	0h RW/1C	RHA Field (RHA): Received Host Abort
28	0h RW/1C	RTA Field (RTA): Received Target Abort
27:25	0h RO	Reserved
24	0h RW/1C	Host Data Parity Error (HDPE): Host Data Parity Error
23:21	0h RO	Reserved
20	1h RO	Cap List Field (CAPLIST): Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	Interrupt Status Field (INTR_STATUS): Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	Reserved
10	0h RW	Interrupt Disable Field (INTR_DISABLE): If '1', SB Interrupt generation is disabled If '0', SB Interrupt generation is enabled
9	0h RO	Reserved
8	0h RW	SERR Enable Field (SERR_ENABLE): SERR Enable Not implemented
7	0h RO	Reserved
6	0h RW	Parity Error Response Enable (PERE): Parity Error Response Enable
5:3	0h RO	Reserved
2	0h RW	BME Field (BME): Bus Host Enable
1	0h RW	MSE Field (MSE): Memory Space Enable
0	0h RO	Reserved

11.1.3 Revision ID and Class Code (REVCLASSCODE) — Offset 8h

Revision ID register and Class Code Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	Revision Id Field (CLASS_CODES): Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	Class Code Field (RID): Revision ID identifies the revision of particular PCI device.

11.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST) — Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23	0h RO	MultifunctionDevice Field (MULFNDEV): Multi-Function Device: This bit is set only if the device has multiple functions. For VF, this bit is set to 0
22:16	00h RO	Header Type Field (HEADERTYPE): Header Type: Implements Type 0 Configuration header
15:8	00h RO	Latency Timer Field (LATTIMER): Latency Timer:.. This register is implemented as R/W with default as 0
7:0	00h RW/P	Cache Line Size Field (CACHELINE_SIZE): Cache Line Size: Does not apply to PCI Express. PCI Express spec requires this to be implemented as an R/W register but has no functional impact on the AMBA Device connected. This field is RO and tied to 0 for VFs.

11.1.5 Base Address Register (BAR) — Offset 10h

Base Address Register low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 10h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	Base Address Field (BASEADDR): Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	Size Field (SIZEINDICATOR): Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	Prefetchable Field (PREFETCHABLE): Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	Type Field (TYPE0): If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	Message Space Field (MESSAGE_SPACE): Memory Space Indicator: 0 indicates this BAR is present in the memory space.

11.1.6 Base Address Register High (BAR_HIGH) — Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Base Address High Field (BASEADDR_HIGH): Base Address High - MSB

11.1.7 Base Address Register1 (BAR1) — Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	Base Address Field (BASEADDR1): Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	Size Field (SIZEINDICATOR1): Always is 0 as minimum size is 4K
3	0h RO	Prefetchable Field (PREFETCHABLE1): Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	Type Field (TYPE1): If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	Message Space Field (MESSAGE_SPACE1): Memory Space Indicator: 0 Indicates this BAR is present in the memory space

11.1.8 Base Address Register1 High (BAR1_HIGH) — Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH Register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Base Address High Field (BASEADDR1_HIGH): Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

11.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) — Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	Subsystem ID Field (SUBSYSTEMID): Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	Subsystem Vendor Field (SUBSYSTEMVENDORID): Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

11.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) — Offset 30h

Expansion ROM Base Address Register is a RO indicates support for Expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	Expansion Rom Base Address Field (EXPANSION_ROM_BASE): Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

11.1.11 Capabilities Pointer (CAPABILITYPTR) — Offset 34h

Capabilities Pointer Register indicates what the next capability is.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	80h RO	Capabilities Pointer Field (CAPPTR_POWER): Capabilities Pointer: Indicates what the next capability is.

11.1.12 Interrupt Register (INTERRUPTREG) — Offset 3Ch

Interrupt Line Register isn't used in Bridge directly Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT Register indicating the requirement of latency timers and MAX_LAT Register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	Max Latency Field (MAX_LAT): Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	Min GNT Field (MIN_GNT): Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved
11:8	1h RO	Interrupt Pin Field (INTPIN): Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	Interrupt Line Field (INTLINE): Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

11.1.13 PCIe Capabilities Register (PCIECAPREG) — Offset 40h

PCIe Capabilities Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 40h	00920010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:25	00h RO/V	Interrupt Message Number Field (INTR_MSG_NUM): PCIe Interrupt Message Number
24	0h RO	Slot Implemented Field (SLOT_IMPLEMENTED): Slot Implemented. Tied to 0
23:20	9h RO	Dev Port Type Field (DEV_PORT_TYPE): Device Port Type. Taken from strap

continued...

Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	Cap Version Field (CAP_VER): PCI Capability Version
15:8	00h RO	Next Capability Pointer Field (NEXT_CAP_PTR): Next Capability Pointer
7:0	10h RO	Capability ID Field (PCIE_CAP_ID): PCIe Capability ID

11.1.14 PCIe Device Capability Register (DEVCAPREG) — Offset 44h

PCIe Device Cap Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 44h	10008FC0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	1h RO	FLR Capability Field (FLR_CAP): FLR Capability
27:26	0h RO	Captured Slot Power Limit Scale Field (CAP_SLOT_PWR_LIM_SCALE): Captured Slot Power Limit Scale. Tied to 0
25:18	00h RO	Captured Slot Power Limit Value Field (CAP_SLOT_PWR_LIM_VAL): Captured Slot Power Limit Value. Tied to 0
17:16	0h RO	Reserved
15	1h RO	RB error PTR Field (RB_ERR_RPTR): Role Based Error Reporting
14:12	0h RO	Reserved
11:9	7h RO	EP L01 Acceptable Latency Field (EP_L1_ACC_LAT): L1 Acceptable Latency
8:6	7h RO	EP L0 Acceptable Latency Field (EP_L0_ACC_LAT): L0 Acceptable Latency
5	0h RO	ETF Support Field (ETF_SUPPORT): Extended Tag Field Support
4:3	0h RO	Phantom Functions Support Field (PHANTOM_FUNC_SUPPORT): Phantom Functions SUPPORT. NA for Bridge
2:0	0h RO	Max PI Size Support Field (MAX_PL_SIZE_SUPPORT): Max Payload Size

11.1.15 PCIe Device Control Status Register (DEVCTRLSTAT) — Offset 48h

PCIe Device Status Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21	0h RO/V	TXN Pending Field (TXN_PENDING): Transaction Pending bit
20	0h RO	Aux Power Detected Field (AUX_PWR_DETECTED): Aux Power Detected. Always tied to 0
19	0h RW/1C	UR Field (UR_DETECTED): Unsupported Request Detected
18	0h RW/1C	Fatal Error Detected Field (FER_DETECTED): Fatal Error Detected
17	0h RO	Non Fatal Err Detected Field (NFER_DETECTED): Non Fatal Error Detected
16	0h RO	Correctable Error Detected Field (CER_DETECTED): Correctable Error Detected
15	0h WO	Initiate FLR Field (INITIATE_FLR): Initiate Function Level Reset
14:12	0h RO	Max Read Request Size Field (MAX_RD_REQ_SIZE): Max Read Request Size
11	0h RW	Enable No Snoop Field (EN_NS): Enable No Snoop
10	0h RO	Aux Power Detected Field (AUX_PWR_PM_EN): Aux Power Enable
9	0h RO	Phantom Function En Field (PHANTOM_FUNC_EN): Phantom Function Enable. Not support by Bridge
8	0h RW	ETF En Field (ETF_EN): Extended Tag Field Enable
7:5	0h RO	Max Payload Size Field (MAX_PL_SIZE): Maximum Payload Size
4	0h RW	Enable Relaxed Ordering Field (EN_RO): Enable Relaxed Ordering
3	0h RW	UR Reporting En Field (URR_EN): Unsupported Request Reporting Enable
2	0h RW	Fatal Err Reporting En Field (FER_EN): Fatal Error Reporting Enable
1	0h RW	Non Fatal Err Reporting En Field (NFER_EN): Non Fatal Error Reporting Enable
0	0h RW	Correctable Error Reporting En Field (CER_EN): Correctable Error Reporting Enable

11.1.16 PCIe Device Capability2 Register (DEVCAPREG2) — Offset 64h

PCIe Device Cap Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 64h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:22	0h RO	Max End2end TLP Prefix Field (MAX_EE_TLP_PREFIXES): Max End2End TLP Prefixes
21	0h RO	End2end TLP Prefix Supported Field (EE_TLP_PREFIX_SUPPORT): End2End TLP Prefixes Support
20	0h RO	Ext Format Support Field (EXTD_FMT_SUPPORT): Extended Format Support
19:18	0h RO	OBFF Support Field (OBFF_SUPPORT): PCI OBFF Support
17:14	0h RO	Reserved
13:12	0h RO	TPH Completer Supported Field (TPH_CPL_SUPPORT): TPH Completer Support
11	0h RO	LTR Support Field (LTR_SUPPORT): LTR Support
10	0h RO	No RO Enable Field (NRO_EN_PRPR_PASS): No RO based PR-PR Passing
9	0h RO	CAS Cpl 128 Support Field (CAS_CPL_SUPPORT_128): CAS128 Support
8	0h RO	CAS Cpl 64 Support Field (ATM_OP_CPL_SUPPORT_64): CAS64 Completion Support
7	0h RO	CAS Cpl 32 Support Field (ATM_OP_CPL_SUPPORT_32): CAS32 Completion Support
6	0h RO	Atomic Operation Routing Field (ATOR_SUPPORT): Atomic Operation Routing Support
5	0h RO	PCI ARI Forwarding Support Field (ARI_FWD_SUPPORT): ARI Forwarding Support
4	0h RO	Cpl Timeout Disable Support Field (CPL_TO_DIS_SUPPORT): Completion Timeout Disable Support
3:0	0h RO	Cpl Timeout Range Support Field (CPL_TO_RNG_SUPPORT): Completion Timeout Ranges Support

11.1.17 PCIe Device Control2 Status Register (DEVCTRLSTAT2) — Offset 68h

PCIe Device Status Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RO	End2end TLP Prefix Blocking Field (EE_TLP_PREFIX_EN): End2End TLP Prefixes Blocking
14:13	0h RO	OBFF Enable Field (OBFF_EN): OBFF Enable
12:11	0h RO	Reserved
10	0h RW	LTR Mechanism Enable Field (LTR_MECH_EN): LTR Mechanism Enable
9	0h RO	IDO Based Cpl Enable Field (IDO_CPL_EN): IDO Completion Enable
8	0h RO	IDO Based Request Enable Field (IDO_REQ_EN): IDO Request Enable
7	0h RO	Atomic Op Egress Blocking Field (ATM_OP_EGR_BLK): Atomic Operation Egress Blocking
6	0h RO	Atomic Op Requester Enable Field (ATM_OP_REQ_EN): Atomic Operation Requester Enable
5	0h RO	ARI Fwd Enable Field (ARI_FWD_EN): ARI Forwarding Enable
4	0h RW	Cpl Timeout Disable Field (CPL_TO_DIS): Completion Timeout Disable Support
3:0	0h RW	Cpl Timeout Value Field (CPL_TO_VAL): Completion Timeout Value

11.1.18 Power Management Capability ID (POWERCAPID) — Offset 80h

Power Management Capability ID Register points to Next Capability Structure and Power Management Capability with Power Management Capabilities Register for PME Support and Version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	PME Support Field (PMESUPPORT): This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	Reserved
18:16	3h	Version Field (VERSION):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	Next Cap Field (NXTCAP): Next Capability: Points to the next capability structure.
7:0	01h RO	Power Capability ID Field (POWER_CAP): Power Management Capability: Indicates this is power management capability

11.1.19 Power Management Control and Status Register (PMECTRLSTATUS) — Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW/1C/P	PME Status Field (PMESTATUS): PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AMBA Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0h RO	Reserved
8	0h RW/P	PME Enable Field (PMEENABLE): PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on Sideband is disabled.
7:4	0h RO	Reserved
3	1h RO	No Soft Reset Field (NO_SOFT_RESET): This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	Reserved
1:0	0h RW	Power State Field (POWERSTATE): Power State: This field is used both to determine the current power state and to set a new power state

11.1.20 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision ID, Capability Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	Vendor Cap Field (VEND_CAP): Vendor Specific Capability ID
27:24	0h RO	Revision ID Field (REVID): Revision ID of capability structure
23:16	14h RO	Cap Length Field (CAP_LENGTH): Vendor Specific Capability Length
15:8	00h RO	Next Capability Field (NEXT_CAP): Next Capability
7:0	09h RO	Capability ID Field (CAPID): Capability ID

11.1.21 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) — Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	Vendor Specific ID Field (VSEC_LENGTH): Vendor Specific Extended Capability Length
19:16	0h RO	Vendor Specific Revision Field (VSEC_REV): Vendor specific Extended Capability revision
15:0	0010h RO	Vendor Specific Length Field (VSECID): Vendor Specific Extended Capability ID

11.1.22 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	SW LTR DWord Offset Field (SW_LAT_DWORD_OFFSET): SW LTR Update MMIO Offset Location (SWLTRLLOC)
3:1	0h	SW LTR Bar Number Field (SW_LAT_BAR_NUM):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	SW LTR Valid Field (SW_LAT_VALID): This value is reflected from the SW LTR valid strap at the top level

11.1.23 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE Pointer Register giving details on Device MMIO Offset, Location BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 9Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	D0i3 DWord Offset Field (DWORD_OFFSET): contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	BAR NUM Field (BAR_NUM): BAR NUM: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	D0i3 Valid Field (VALID): Valid: This value is reflected from the D0i3 valid strap at the top level.

11.1.24 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and Power Control Enable Register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21	0h RW/P	HAE: Hardware Autonomous Enable: If 1, then hardware may request power gating whenever it has reached an idle condition.
20	0h RO	Reserved
19	0h RW/P	Sleep Enable Field (SLEEP_EN): SE: Sleep Enable: If 1, then the function may assert Sleep during power gating. If 0, then function will never assert Sleep to the retention flops. Note that some platforms may default this bit to 0, others to 1.
18	0h	D3 Hen Field (D3HEN):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW/P	DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	0h RW/P	Device Idle En Field (DEVIDLEN): PMCRE: PMC Request Enable
16	0h RW/P	PMC Request Enable Field (PMCRE): D3-Hot Enable (D3HEN): If 1, then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3).
15:13	0h RO	Reserved
12:10	2h RW/O/P	Power Latency Scale Field (POW_LAT_SCALE): Power On Latency Scale
9:0	000h RW/O/P	Power Latency Value Field (POW_LAT_VALUE): Power On Latency Value

11.1.25 General Purpose Read Write Register1 (GEN_PCI_REGRW1) — Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	General Purpose Read Write Field (GEN_PCI_REG_RW1): General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

11.1.26 General Purpose Input Register (GEN_INPUT_REG) — Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	General Purpose Input Field (GEN_REG_INPUT_RW): General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

11.1.27 MSI Capability Register (MSI_CAP_REG) — Offset D0h

MSI Capability Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	1h RO	Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP): Per Vector Masking Capability
23	1h RO	MSI Capability Field (MSI_CAP_64B): 64 bit message address capability
22:20	0h RW	Multi Message En Field (MUL_MSG_EN): Multiple Message Enable
19:17	0h RO	Multi Message Cap Field (MUL_MSG_CAP): Multiple Message Capable
16	0h RW	MSI Enable Field (MSG_MSI_ENABLE): MSI Enable: If 1, then the PCI Device is allowed to use MSI to request service. The PCI Device is prohibited to use INTx, when MSI is enabled If 0, then the PCI Device is prohibited from using MSI to request service.
15:8	00h RO	Next Pointer Field (MSG_NXT_PTR): Next Capability Pointer
7:0	05h RO	MSI Capability Field (MSG_CAP_ID): MSI Capability ID

11.1.28 MSI Message Low Address (MSI_ADDR_LOW) — Offset D4h

MSI Message Low Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	MSI Message Low Address Field (MSI_ADDR_LOW): MSI Message Low Address
1:0	0h RO	Reserved

11.1.29 MSI Message High Address (MSI_ADDR_HIGH) — Offset D8h

MSI Message High Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	MSI Message High Address Field (MSI_ADDR_HIGH): MSI Message High Address

11.1.30 MSI Message Data (MSI_MSG_DATA) — Offset DCh

MSI Message Data.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:0	0000h RW	MSI Message Data Field (MSI_MSG_DATA): MSI Message Data

11.1.31 MSI Mask Register (MSI_MASK) — Offset E0h

MSI Mask Bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RW	MSI Mask Field (MSI_MASK): MSI Mask bits

11.1.32 MSI Pending Register (MSI_PENDING) — Offset E4h

MSI Pending Bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	MSI Pending Field (MSI_PENDING): MSI Pending bits

11.1.33 Manufacturers ID (MANID) — Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/P	Manufacturers ID Field (MANID): Manufacturer ID: Default value comes from straps.

11.2 Ethernet TSN Memory Mapped Registers Summary

These are the I/O Registers in Memory Space for this Function that are accessible to BIOS and software running on the Host Root (RS0) processor. The Base Address Register (BAR) is located at offset 10h in PCI Configuration Space.

Table 20. Summary of Ethernet TSN Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MAC_CONFIGURATION — Offset 0h on page 86	00000000h
4h	4	MAC_EXT_CONFIGURATION — Offset 4h on page 91	00000000h
8h	4	MAC_PACKET_FILTER — Offset 8h on page 92	00000000h
Ch	4	MAC_WATCHDOG_TIMEOUT — Offset Ch on page 95	00000000h
10h	4	MAC_HASH_TABLE_REG0 — Offset 10h on page 96	00000000h
14h	4	MAC_HASH_TABLE_REG1 — Offset 14h on page 96	00000000h
50h	4	MAC_VLAN_TAG_CTRL — Offset 50h on page 97	00000000h
54h	4	MAC_VLAN_TAG_DATA — Offset 54h on page 99	00000000h
58h	4	MAC_VLAN_HASH_TABLE — Offset 58h on page 101	00000000h
60h	4	MAC_VLAN_INCL — Offset 60h on page 101	00000000h
64h	4	MAC_INNER_VLAN_INCL — Offset 64h on page 103	00000000h
70h	4	MAC_Q0_TX_FLOW_CTRL — Offset 70h on page 104	00000000h
74h	4	MAC_Q1_TX_FLOW_CTRL — Offset 74h on page 106	00000000h
78h	4	MAC_Q2_TX_FLOW_CTRL — Offset 78h on page 107	00000000h
7Ch	4	MAC_Q3_TX_FLOW_CTRL — Offset 7Ch on page 108	00000000h
80h	4	MAC_Q4_TX_FLOW_CTRL — Offset 80h on page 109	00000000h
84h	4	MAC_Q5_TX_FLOW_CTRL — Offset 84h on page 111	00000000h
90h	4	MAC_RX_FLOW_CTRL — Offset 90h on page 112	00000000h
94h	4	MAC_RXQ_CTRL4 — Offset 94h on page 112	00000000h
98h	4	MAC_TXQ_PRTY_MAP0 — Offset 98h on page 113	00000000h
A0h	4	MAC_RXQ_CTRL0 — Offset A0h on page 114	00000000h
A4h	4	MAC_RXQ_CTRL1 — Offset A4h on page 115	00000000h
A8h	4	MAC_RXQ_CTRL2 — Offset A8h on page 117	00000000h
ACh	4	MAC_RXQ_CTRL3 — Offset ACh on page 118	00000000h
B0h	4	MAC_INTERRUPT_STATUS — Offset B0h on page 119	00000000h
B4h	4	MAC_INTERRUPT_ENABLE — Offset B4h on page 121	00000000h
B8h	4	MAC_RX_TX_STATUS — Offset B8h on page 123	00000000h
C0h	4	MAC_PMT_CONTROL_STATUS — Offset C0h on page 124	00000000h
C4h	4	MAC_RWK_PACKET_FILTER — Offset C4h on page 126	00000000h
D0h	4	MAC_LPI_CONTROL_STATUS — Offset D0h on page 126	00000000h

continued...

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D4h	4	MAC_LPI_TIMERS_CONTROL — Offset D4h on page 128	03E80000h
D8h	4	MAC_LPI_ENTRY_TIMER — Offset D8h on page 129	00000000h
DCh	4	MAC_1US_TIC_COUNTER — Offset DCh on page 129	00000063h
F8h	4	MAC_PHYIF_CONTROL_STATUS — Offset F8h on page 130	00000000h
110h	4	MAC_VERSION — Offset 110h on page 131	00005151h
114h	4	MAC_DEBUG — Offset 114h on page 131	00000000h
11Ch	4	MAC_HW_FEATURE0 — Offset 11Ch on page 132	0EFD73F7h
120h	4	MAC_HW_FEATURE1 — Offset 120h on page 134	119F79C8h
124h	4	MAC_HW_FEATURE2 — Offset 124h on page 136	220C50C5h
128h	4	MAC_HW_FEATURE3 — Offset 128h on page 138	3C390232h
140h	4	MAC_DPP_FSM_INTERRUPT_STATUS — Offset 140h on page 140	00000000h
144h	4	MAC_AXI_SLV_DPE_ADDR_STATUS — Offset 144h on page 142	00000000h
148h	4	MAC_FSM_CONTROL — Offset 148h on page 142	00000000h
14Ch	4	MAC_FSM_ACT_TIMER — Offset 14Ch on page 144	00000000h
150h	4	SNPS_SCS_REG1 — Offset 150h on page 145	00000000h
200h	4	MAC_MDIO_ADDRESS — Offset 200h on page 145	00000000h
204h	4	MAC_MDIO_DATA — Offset 204h on page 148	00000000h
208h	4	MAC_GPIO_CONTROL — Offset 208h on page 148	00000000h
20Ch	4	MAC_GPIO_STATUS — Offset 20Ch on page 148	00000000h
210h	4	MAC_ARP_ADDRESS — Offset 210h on page 149	00000000h
230h	4	MAC_CSR_SW_CTRL — Offset 230h on page 149	00000000h
234h	4	MAC_FPE_CTRL_STS — Offset 234h on page 149	00000000h
238h	4	MAC_EXT_CFG1 — Offset 238h on page 151	00000002h
240h	4	MAC_PRESN_TIME_NS — Offset 240h on page 151	00000000h
244h	4	MAC_PRESN_TIME_UPDT — Offset 244h on page 152	00000000h
300h	4	MAC_ADDRESS0_HIGH — Offset 300h on page 152	8000FFFFh
304h	4	MAC_ADDRESS0_LOW — Offset 304h on page 153	FFFFFFFFFh
308h	4	MAC_ADDRESS1_HIGH — Offset 308h on page 153	0000FFFFh
30Ch	4	MAC_ADDRESS1_LOW — Offset 30Ch on page 154	FFFFFFFFFh
310h	4	MAC_ADDRESS2_HIGH — Offset 310h on page 154	0000FFFFh
314h	4	MAC_ADDRESS2_LOW — Offset 314h on page 155	FFFFFFFFFh
318h	4	MAC_ADDRESS3_HIGH — Offset 318h on page 155	0000FFFFh
31Ch	4	MAC_ADDRESS3_LOW — Offset 31Ch on page 156	FFFFFFFFFh
320h	4	MAC_ADDRESS4_HIGH — Offset 320h on page 157	0000FFFFh
324h	4	MAC_ADDRESS4_LOW — Offset 324h on page 158	FFFFFFFFFh

continued...

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
328h	4	MAC_ADDRESS5_HIGH — Offset 328h on page 158	0000FFFFh
32Ch	4	MAC_ADDRESS5_LOW — Offset 32Ch on page 159	FFFFFFFh
330h	4	MAC_ADDRESS6_HIGH — Offset 330h on page 159	0000FFFFh
334h	4	MAC_ADDRESS6_LOW — Offset 334h on page 160	FFFFFFFh
338h	4	MAC_ADDRESS7_HIGH — Offset 338h on page 160	0000FFFFh
33Ch	4	MAC_ADDRESS7_LOW — Offset 33Ch on page 161	FFFFFFFh
340h	4	MAC_ADDRESS8_HIGH — Offset 340h on page 162	0000FFFFh
344h	4	MAC_ADDRESS8_LOW — Offset 344h on page 162	FFFFFFFh
348h	4	MAC_ADDRESS9_HIGH — Offset 348h on page 163	0000FFFFh
34Ch	4	MAC_ADDRESS9_LOW — Offset 34Ch on page 164	FFFFFFFh
350h	4	MAC_ADDRESS10_HIGH — Offset 350h on page 164	0000FFFFh
354h	4	MAC_ADDRESS10_LOW — Offset 354h on page 165	FFFFFFFh
358h	4	MAC_ADDRESS11_HIGH — Offset 358h on page 165	0000FFFFh
35Ch	4	MAC_ADDRESS11_LOW — Offset 35Ch on page 166	FFFFFFFh
360h	4	MAC_ADDRESS12_HIGH — Offset 360h on page 166	0000FFFFh
364h	4	MAC_ADDRESS12_LOW — Offset 364h on page 167	FFFFFFFh
368h	4	MAC_ADDRESS13_HIGH — Offset 368h on page 168	0000FFFFh
36Ch	4	MAC_ADDRESS13_LOW — Offset 36Ch on page 169	FFFFFFFh
370h	4	MAC_ADDRESS14_HIGH — Offset 370h on page 169	0000FFFFh
374h	4	MAC_ADDRESS14_LOW — Offset 374h on page 170	FFFFFFFh
378h	4	MAC_ADDRESS15_HIGH — Offset 378h on page 170	0000FFFFh
37Ch	4	MAC_ADDRESS15_LOW — Offset 37Ch on page 171	FFFFFFFh
380h	4	MAC_ADDRESS16_HIGH — Offset 380h on page 171	0000FFFFh
384h	4	MAC_ADDRESS16_LOW — Offset 384h on page 172	FFFFFFFh
388h	4	MAC_ADDRESS17_HIGH — Offset 388h on page 173	0000FFFFh
38Ch	4	MAC_ADDRESS17_LOW — Offset 38Ch on page 174	FFFFFFFh
390h	4	MAC_ADDRESS18_HIGH — Offset 390h on page 174	0000FFFFh
394h	4	MAC_ADDRESS18_LOW — Offset 394h on page 175	FFFFFFFh
398h	4	MAC_ADDRESS19_HIGH — Offset 398h on page 175	0000FFFFh
39Ch	4	MAC_ADDRESS19_LOW — Offset 39Ch on page 176	FFFFFFFh
3A0h	4	MAC_ADDRESS20_HIGH — Offset 3A0h on page 176	0000FFFFh
3A4h	4	MAC_ADDRESS20_LOW — Offset 3A4h on page 177	FFFFFFFh
3A8h	4	MAC_ADDRESS21_HIGH — Offset 3A8h on page 178	0000FFFFh
3ACh	4	MAC_ADDRESS21_LOW — Offset 3ACh on page 179	FFFFFFFh
3B0h	4	MAC_ADDRESS22_HIGH — Offset 3B0h on page 179	0000FFFFh

continued...

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3B4h	4	MAC_ADDRESS22_LOW — Offset 3B4h on page 180	FFFFFFFh
3B8h	4	MAC_ADDRESS23_HIGH — Offset 3B8h on page 180	0000FFFh
3BCh	4	MAC_ADDRESS23_LOW — Offset 3BCh on page 181	FFFFFFFh
3C0h	4	MAC_ADDRESS24_HIGH — Offset 3C0h on page 181	0000FFFh
3C4h	4	MAC_ADDRESS24_LOW — Offset 3C4h on page 182	FFFFFFFh
3C8h	4	MAC_ADDRESS25_HIGH — Offset 3C8h on page 183	0000FFFh
3CCh	4	MAC_ADDRESS25_LOW — Offset 3CCh on page 184	FFFFFFFh
3D0h	4	MAC_ADDRESS26_HIGH — Offset 3D0h on page 184	0000FFFh
3D4h	4	MAC_ADDRESS26_LOW — Offset 3D4h on page 185	FFFFFFFh
3D8h	4	MAC_ADDRESS27_HIGH — Offset 3D8h on page 185	0000FFFh
3DCh	4	MAC_ADDRESS27_LOW — Offset 3DCh on page 186	FFFFFFFh
3E0h	4	MAC_ADDRESS28_HIGH — Offset 3E0h on page 186	0000FFFh
3E4h	4	MAC_ADDRESS28_LOW — Offset 3E4h on page 187	FFFFFFFh
3E8h	4	MAC_ADDRESS29_HIGH — Offset 3E8h on page 188	0000FFFh
3ECh	4	MAC_ADDRESS29_LOW — Offset 3ECh on page 189	FFFFFFFh
3F0h	4	MAC_ADDRESS30_HIGH — Offset 3F0h on page 189	0000FFFh
3F4h	4	MAC_ADDRESS30_LOW — Offset 3F4h on page 190	FFFFFFFh
3F8h	4	MAC_ADDRESS31_HIGH — Offset 3F8h on page 190	0000FFFh
3FCh	4	MAC_ADDRESS31_LOW — Offset 3FCh on page 191	FFFFFFFh
400h	4	MAC_ADDRESS32_HIGH — Offset 400h on page 191	0000FFFh
404h	4	MAC_ADDRESS32_LOW — Offset 404h on page 192	FFFFFFFh
408h	4	MAC_ADDRESS33_HIGH — Offset 408h on page 192	0000FFFh
40Ch	4	MAC_ADDRESS33_LOW — Offset 40Ch on page 193	FFFFFFFh
410h	4	MAC_ADDRESS34_HIGH — Offset 410h on page 193	0000FFFh
414h	4	MAC_ADDRESS34_LOW — Offset 414h on page 194	FFFFFFFh
418h	4	MAC_ADDRESS35_HIGH — Offset 418h on page 194	0000FFFh
41Ch	4	MAC_ADDRESS35_LOW — Offset 41Ch on page 195	FFFFFFFh
420h	4	MAC_ADDRESS36_HIGH — Offset 420h on page 195	0000FFFh
424h	4	MAC_ADDRESS36_LOW — Offset 424h on page 195	FFFFFFFh
428h	4	MAC_ADDRESS37_HIGH — Offset 428h on page 196	0000FFFh
42Ch	4	MAC_ADDRESS37_LOW — Offset 42Ch on page 196	FFFFFFFh
430h	4	MAC_ADDRESS38_HIGH — Offset 430h on page 197	0000FFFh
434h	4	MAC_ADDRESS38_LOW — Offset 434h on page 197	FFFFFFFh
438h	4	MAC_ADDRESS39_HIGH — Offset 438h on page 197	0000FFFh
43Ch	4	MAC_ADDRESS39_LOW — Offset 43Ch on page 198	FFFFFFFh

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
440h	4	MAC_ADDRESS40_HIGH — Offset 440h on page 198	0000FFFFh
444h	4	MAC_ADDRESS40_LOW — Offset 444h on page 199	FFFFFFFh
448h	4	MAC_ADDRESS41_HIGH — Offset 448h on page 199	0000FFFFh
44Ch	4	MAC_ADDRESS41_LOW — Offset 44Ch on page 200	FFFFFFFh
450h	4	MAC_ADDRESS42_HIGH — Offset 450h on page 200	0000FFFFh
454h	4	MAC_ADDRESS42_LOW — Offset 454h on page 201	FFFFFFFh
458h	4	MAC_ADDRESS43_HIGH — Offset 458h on page 201	0000FFFFh
45Ch	4	MAC_ADDRESS43_LOW — Offset 45Ch on page 201	FFFFFFFh
460h	4	MAC_ADDRESS44_HIGH — Offset 460h on page 202	0000FFFFh
464h	4	MAC_ADDRESS44_LOW — Offset 464h on page 202	FFFFFFFh
468h	4	MAC_ADDRESS45_HIGH — Offset 468h on page 203	0000FFFFh
46Ch	4	MAC_ADDRESS45_LOW — Offset 46Ch on page 203	FFFFFFFh
470h	4	MAC_ADDRESS46_HIGH — Offset 470h on page 203	0000FFFFh
474h	4	MAC_ADDRESS46_LOW — Offset 474h on page 204	FFFFFFFh
478h	4	MAC_ADDRESS47_HIGH — Offset 478h on page 204	0000FFFFh
47Ch	4	MAC_ADDRESS47_LOW — Offset 47Ch on page 205	FFFFFFFh
480h	4	MAC_ADDRESS48_HIGH — Offset 480h on page 205	0000FFFFh
484h	4	MAC_ADDRESS48_LOW — Offset 484h on page 206	FFFFFFFh
488h	4	MAC_ADDRESS49_HIGH — Offset 488h on page 206	0000FFFFh
48Ch	4	MAC_ADDRESS49_LOW — Offset 48Ch on page 207	FFFFFFFh
490h	4	MAC_ADDRESS50_HIGH — Offset 490h on page 207	0000FFFFh
494h	4	MAC_ADDRESS50_LOW — Offset 494h on page 207	FFFFFFFh
498h	4	MAC_ADDRESS51_HIGH — Offset 498h on page 208	0000FFFFh
49Ch	4	MAC_ADDRESS51_LOW — Offset 49Ch on page 208	FFFFFFFh
4A0h	4	MAC_ADDRESS52_HIGH — Offset 4A0h on page 209	0000FFFFh
4A4h	4	MAC_ADDRESS52_LOW — Offset 4A4h on page 209	FFFFFFFh
4A8h	4	MAC_ADDRESS53_HIGH — Offset 4A8h on page 209	0000FFFFh
4ACh	4	MAC_ADDRESS53_LOW — Offset 4ACh on page 210	FFFFFFFh
4B0h	4	MAC_ADDRESS54_HIGH — Offset 4B0h on page 210	0000FFFFh
4B4h	4	MAC_ADDRESS54_LOW — Offset 4B4h on page 211	FFFFFFFh
4B8h	4	MAC_ADDRESS55_HIGH — Offset 4B8h on page 211	0000FFFFh
4BCh	4	MAC_ADDRESS55_LOW — Offset 4BCh on page 212	FFFFFFFh
4C0h	4	MAC_ADDRESS56_HIGH — Offset 4C0h on page 212	0000FFFFh
4C4h	4	MAC_ADDRESS56_LOW — Offset 4C4h on page 213	FFFFFFFh
4C8h	4	MAC_ADDRESS57_HIGH — Offset 4C8h on page 213	0000FFFFh

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4CCh	4	MAC_ADDRESS57_LOW — Offset 4CCh on page 213	FFFFFFFh
4D0h	4	MAC_ADDRESS58_HIGH — Offset 4D0h on page 214	0000FFFh
4D4h	4	MAC_ADDRESS58_LOW — Offset 4D4h on page 214	FFFFFFFh
4D8h	4	MAC_ADDRESS59_HIGH — Offset 4D8h on page 215	0000FFFh
4DCh	4	MAC_ADDRESS59_LOW — Offset 4DCh on page 215	FFFFFFFh
4E0h	4	MAC_ADDRESS60_HIGH — Offset 4E0h on page 215	0000FFFh
4E4h	4	MAC_ADDRESS60_LOW — Offset 4E4h on page 216	FFFFFFFh
4E8h	4	MAC_ADDRESS61_HIGH — Offset 4E8h on page 216	0000FFFh
4EcH	4	MAC_ADDRESS61_LOW — Offset 4EcH on page 217	FFFFFFFh
4F0h	4	MAC_ADDRESS62_HIGH — Offset 4F0h on page 217	0000FFFh
4F4h	4	MAC_ADDRESS62_LOW — Offset 4F4h on page 218	FFFFFFFh
4F8h	4	MAC_ADDRESS63_HIGH — Offset 4F8h on page 218	0000FFFh
4FcH	4	MAC_ADDRESS63_LOW — Offset 4FcH on page 219	FFFFFFFh
700h	4	MMC_CONTROL — Offset 700h on page 219	0000000h
704h	4	MMC_RX_INTERRUPT — Offset 704h on page 220	0000000h
708h	4	MMC_TX_INTERRUPT — Offset 708h on page 224	0000000h
70Ch	4	MMC_RX_INTERRUPT_MASK — Offset 70Ch on page 228	0000000h
710h	4	MMC_TX_INTERRUPT_MASK — Offset 710h on page 232	0000000h
714h	4	TX_OCTET_COUNT_GOOD_BAD — Offset 714h on page 235	0000000h
718h	4	TX_PACKET_COUNT_GOOD_BAD — Offset 718h on page 235	0000000h
71Ch	4	TX_BROADCAST_PACKETS_GOOD — Offset 71Ch on page 235	0000000h
720h	4	TX_MULTICAST_PACKETS_GOOD — Offset 720h on page 236	0000000h
724h	4	TX_64OCTETS_PACKETS_GOOD_BAD — Offset 724h on page 236	0000000h
728h	4	TX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 728h on page 236	0000000h
72Ch	4	TX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 72Ch on page 237	0000000h
730h	4	TX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 730h on page 237	0000000h
734h	4	TX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 734h on page 237	0000000h
738h	4	TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 738h on page 237	0000000h
73Ch	4	TX_UNICAST_PACKETS_GOOD_BAD — Offset 73Ch on page 238	0000000h
740h	4	TX_MULTICAST_PACKETS_GOOD_BAD — Offset 740h on page 238	0000000h
744h	4	TX_BROADCAST_PACKETS_GOOD_BAD — Offset 744h on page 238	0000000h
748h	4	TX_UNDERFLOW_ERROR_PACKETS — Offset 748h on page 239	0000000h
74Ch	4	TX_SINGLE_COLLISION_GOOD_PACKETS — Offset 74Ch on page 239	0000000h
750h	4	TX_MULTIPLE_COLLISION_GOOD_PACKETS — Offset 750h on page 239	0000000h
754h	4	TX_DEFERRED_PACKETS — Offset 754h on page 239	0000000h

continued...

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
758h	4	TX_LATE_COLLISION_PACKETS — Offset 758h on page 240	00000000h
75Ch	4	TX_EXCESSIVE_COLLISION_PACKETS — Offset 75Ch on page 240	00000000h
760h	4	TX_CARRIER_ERROR_PACKETS — Offset 760h on page 240	00000000h
764h	4	TX_OCTET_COUNT_GOOD — Offset 764h on page 240	00000000h
768h	4	TX_PACKET_COUNT_GOOD — Offset 768h on page 241	00000000h
76Ch	4	TX_EXCESSIVE_DEFERRAL_ERROR — Offset 76Ch on page 241	00000000h
770h	4	TX_PAUSE_PACKETS — Offset 770h on page 241	00000000h
774h	4	TX_VLAN_PACKETS_GOOD — Offset 774h on page 242	00000000h
778h	4	TX_OSIZE_PACKETS_GOOD — Offset 778h on page 242	00000000h
780h	4	RX_PACKETS_COUNT_GOOD_BAD — Offset 780h on page 242	00000000h
784h	4	RX_OCTET_COUNT_GOOD_BAD — Offset 784h on page 242	00000000h
788h	4	RX_OCTET_COUNT_GOOD — Offset 788h on page 243	00000000h
78Ch	4	RX_BROADCAST_PACKETS_GOOD — Offset 78Ch on page 243	00000000h
790h	4	RX_MULTICAST_PACKETS_GOOD — Offset 790h on page 243	00000000h
794h	4	RX_CRC_ERROR_PACKETS — Offset 794h on page 243	00000000h
798h	4	RX_ALIGNMENT_ERROR_PACKETS — Offset 798h on page 244	00000000h
79Ch	4	RX_RUNT_ERROR_PACKETS — Offset 79Ch on page 244	00000000h
7A0h	4	RX_JABBER_ERROR_PACKETS — Offset 7A0h on page 244	00000000h
7A4h	4	RX_UNDERSIZE_PACKETS_GOOD — Offset 7A4h on page 245	00000000h
7A8h	4	RX_OVERSIZE_PACKETS_GOOD — Offset 7A8h on page 245	00000000h
7ACh	4	RX_64OCTETS_PACKETS_GOOD_BAD — Offset 7ACh on page 245	00000000h
7B0h	4	RX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 7B0h on page 245	00000000h
7B4h	4	RX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 7B4h on page 246	00000000h
7B8h	4	RX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 7B8h on page 246	00000000h
7BCh	4	RX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 7BCh on page 246	00000000h
7C0h	4	RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 7C0h on page 247	00000000h
7C4h	4	RX_UNICAST_PACKETS_GOOD — Offset 7C4h on page 247	00000000h
7C8h	4	RX_LENGTH_ERROR_PACKETS — Offset 7C8h on page 247	00000000h
7CCh	4	RX_OUT_OF_RANGE_TYPE_PACKETS — Offset 7CCh on page 248	00000000h
7D0h	4	RX_PAUSE_PACKETS — Offset 7D0h on page 248	00000000h
7D4h	4	RX_FIFO_OVERFLOW_PACKETS — Offset 7D4h on page 248	00000000h
7D8h	4	RX_VLAN_PACKETS_GOOD_BAD — Offset 7D8h on page 248	00000000h
7DCh	4	RX_WATCHDOG_ERROR_PACKETS — Offset 7DCh on page 249	00000000h
7E0h	4	RX_RECEIVE_ERROR_PACKETS — Offset 7E0h on page 249	00000000h
7E4h	4	RX_CONTROL_PACKETS_GOOD — Offset 7E4h on page 249	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7ECh	4	TX_LPI_USEC_CNTR — Offset 7ECh on page 250	00000000h
7F0h	4	TX_LPI_TRAN_CNTR — Offset 7F0h on page 250	00000000h
7F4h	4	RX_LPI_USEC_CNTR — Offset 7F4h on page 250	00000000h
7F8h	4	RX_LPI_TRAN_CNTR — Offset 7F8h on page 250	00000000h
800h	4	MMC_IPC_RX_INTERRUPT_MASK — Offset 800h on page 251	00000000h
808h	4	MMC_IPC_RX_INTERRUPT — Offset 808h on page 254	00000000h
810h	4	RXIPV4_GOOD_PACKETS — Offset 810h on page 258	00000000h
814h	4	RXIPV4_HEADER_ERROR_PACKETS — Offset 814h on page 258	00000000h
818h	4	RXIPV4_NO_PAYLOAD_PACKETS — Offset 818h on page 258	00000000h
81Ch	4	RXIPV4_FRAGMENTED_PACKETS — Offset 81Ch on page 259	00000000h
820h	4	RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS — Offset 820h on page 259	00000000h
824h	4	RXIPV6_GOOD_PACKETS — Offset 824h on page 259	00000000h
828h	4	RXIPV6_HEADER_ERROR_PACKETS — Offset 828h on page 259	00000000h
82Ch	4	RXIPV6_NO_PAYLOAD_PACKETS — Offset 82Ch on page 260	00000000h
830h	4	RXUDP_GOOD_PACKETS — Offset 830h on page 260	00000000h
834h	4	RXUDP_ERROR_PACKETS — Offset 834h on page 260	00000000h
838h	4	RXTCP_GOOD_PACKETS — Offset 838h on page 261	00000000h
83Ch	4	RXTCP_ERROR_PACKETS — Offset 83Ch on page 261	00000000h
840h	4	RXICMP_GOOD_PACKETS — Offset 840h on page 261	00000000h
844h	4	RXICMP_ERROR_PACKETS — Offset 844h on page 261	00000000h
850h	4	RXIPV4_GOOD_OCTETS — Offset 850h on page 262	00000000h
854h	4	RXIPV4_HEADER_ERROR_OCTETS — Offset 854h on page 262	00000000h
858h	4	RXIPV4_NO_PAYLOAD_OCTETS — Offset 858h on page 262	00000000h
85Ch	4	RXIPV4_FRAGMENTED_OCTETS — Offset 85Ch on page 263	00000000h
860h	4	RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS — Offset 860h on page 263	00000000h
864h	4	RXIPV6_GOOD_OCTETS — Offset 864h on page 263	00000000h
868h	4	RXIPV6_HEADER_ERROR_OCTETS — Offset 868h on page 264	00000000h
86Ch	4	RXIPV6_NO_PAYLOAD_OCTETS — Offset 86Ch on page 264	00000000h
870h	4	RXUDP_GOOD_OCTETS — Offset 870h on page 264	00000000h
874h	4	RXUDP_ERROR_OCTETS — Offset 874h on page 265	00000000h
878h	4	RXTCP_GOOD_OCTETS — Offset 878h on page 265	00000000h
87Ch	4	RXTCP_ERROR_OCTETS — Offset 87Ch on page 265	00000000h
880h	4	RXICMP_GOOD_OCTETS — Offset 880h on page 265	00000000h
884h	4	RXICMP_ERROR_OCTETS — Offset 884h on page 266	00000000h
8A0h	4	MMC_FPE_TX_INTERRUPT — Offset 8A0h on page 266	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8A4h	4	MMC_FPE_TX_INTERRUPT_MASK — Offset 8A4h on page 267	00000000h
8A8h	4	MMC_TX_FPE_FRAGMENT_CNTR — Offset 8A8h on page 267	00000000h
8ACh	4	MMC_TX_HOLD_REQ_CNTR — Offset 8ACh on page 267	00000000h
8C0h	4	MMC_FPE_RX_INTERRUPT — Offset 8C0h on page 268	00000000h
8C4h	4	MMC_FPE_RX_INTERRUPT_MASK — Offset 8C4h on page 269	00000000h
8C8h	4	MMC_RX_PACKET_ASSEMBLY_ERR_CNTR — Offset 8C8h on page 269	00000000h
8CCh	4	MMC_RX_PACKET_SMD_ERR_CNTR — Offset 8CCh on page 270	00000000h
8D0h	4	MMC_RX_PACKET_ASSEMBLY_OK_CNTR — Offset 8D0h on page 270	00000000h
8D4h	4	MMC_RX_FPE_FRAGMENT_CNTR — Offset 8D4h on page 270	00000000h
900h	4	MAC_L3_L4_CONTROL0 — Offset 900h on page 271	00000000h
904h	4	MAC_LAYER4_ADDRESS0 — Offset 904h on page 273	00000000h
910h	4	MAC_LAYER3_ADDR0_REG0 — Offset 910h on page 274	00000000h
914h	4	MAC_LAYER3_ADDR1_REG0 — Offset 914h on page 274	00000000h
918h	4	MAC_LAYER3_ADDR2_REG0 — Offset 918h on page 274	00000000h
91Ch	4	MAC_LAYER3_ADDR3_REG0 — Offset 91Ch on page 275	00000000h
930h	4	MAC_L3_L4_CONTROL1 — Offset 930h on page 275	00000000h
934h	4	MAC_LAYER4_ADDRESS1 — Offset 934h on page 278	00000000h
940h	4	MAC_LAYER3_ADDR0_REG1 — Offset 940h on page 279	00000000h
944h	4	MAC_LAYER3_ADDR1_REG1 — Offset 944h on page 279	00000000h
948h	4	MAC_LAYER3_ADDR2_REG1 — Offset 948h on page 279	00000000h
94Ch	4	MAC_LAYER3_ADDR3_REG1 — Offset 94Ch on page 280	00000000h
B00h	4	MAC_TIMESTAMP_CONTROL — Offset B00h on page 280	00002000h
B04h	4	MAC_SUB_SECOND_INCREMENT — Offset B04h on page 283	00000000h
B08h	4	MAC_SYSTEM_TIME_SECONDS — Offset B08h on page 284	00000000h
B0Ch	4	MAC_SYSTEM_TIME_NANOSECONDS — Offset B0Ch on page 284	00000000h
B10h	4	MAC_SYSTEM_TIME_SECONDS_UPDATE — Offset B10h on page 284	00000000h
B14h	4	MAC_SYSTEM_TIME_NANOSECONDS_UPDATE — Offset B14h on page 285	00000000h
B18h	4	MAC_TIMESTAMP_ADDEND — Offset B18h on page 285	00000000h
B1Ch	4	MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS — Offset B1Ch on page 285	00000000h
B20h	4	MAC_TIMESTAMP_STATUS — Offset B20h on page 286	00000000h
B30h	4	MAC_TX_TIMESTAMP_STATUS_NANOSECONDS — Offset B30h on page 288	00000000h
B34h	4	MAC_TX_TIMESTAMP_STATUS_SECONDS — Offset B34h on page 289	00000000h
B40h	4	MAC_AUXILIARY_CONTROL — Offset B40h on page 289	00000000h
B48h	4	MAC_AUXILIARY_TIMESTAMP_NANOSECONDS — Offset B48h on page 290	00000000h
B4Ch	4	MAC_AUXILIARY_TIMESTAMP_SECONDS — Offset B4Ch on page 290	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B50h	4	MAC_TIMESTAMP_INGRESS_ASYM_CORR — Offset B50h on page 290	00000000h
B54h	4	MAC_TIMESTAMP_EGRESS_ASYM_CORR — Offset B54h on page 291	00000000h
B58h	4	MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND — Offset B58h on page 291	00000000h
B5Ch	4	MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND — Offset B5Ch on page 291	00000000h
B60h	4	MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC — Offset B60h on page 292	00000000h
B64h	4	MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC — Offset B64h on page 292	00000000h
B68h	4	MAC_TIMESTAMP_INGRESS_LATENCY — Offset B68h on page 292	00000000h
B6Ch	4	MAC_TIMESTAMP_EGRESS_LATENCY — Offset B6Ch on page 293	00000000h
B70h	4	MAC_PPS_CONTROL — Offset B70h on page 293	00000000h
B80h	4	MAC_PPS0_TARGET_TIME_SECONDS — Offset B80h on page 296	00000000h
B84h	4	MAC_PPS0_TARGET_TIME_NANOSECONDS — Offset B84h on page 296	00000000h
B88h	4	MAC_PPS0_INTERVAL — Offset B88h on page 297	00000000h
B8Ch	4	MAC_PPS0_WIDTH — Offset B8Ch on page 297	00000000h
B90h	4	MAC_PPS1_TARGET_TIME_SECONDS — Offset B90h on page 298	00000000h
B94h	4	MAC_PPS1_TARGET_TIME_NANOSECONDS — Offset B94h on page 298	00000000h
B98h	4	MAC_PPS1_INTERVAL — Offset B98h on page 298	00000000h
B9Ch	4	MAC_PPS1_WIDTH — Offset B9Ch on page 299	00000000h
BC0h	4	MAC_PTO_CONTROL — Offset BC0h on page 299	00000000h
BC4h	4	MAC_SOURCE_PORT_IDENTITY0 — Offset BC4h on page 300	00000000h
BC8h	4	MAC_SOURCE_PORT_IDENTITY1 — Offset BC8h on page 301	00000000h
BCCh	4	MAC_SOURCE_PORT_IDENTITY2 — Offset BCCh on page 301	00000000h
BD0h	4	MAC_LOG_MESSAGE_INTERVAL — Offset BD0h on page 301	00000000h
C00h	4	MTL_OPERATION_MODE — Offset C00h on page 302	00000000h
C08h	4	MTL_DBG_CTL — Offset C08h on page 303	00000000h
C0Ch	4	MTL_DBG_STS — Offset C0Ch on page 305	00000018h
C10h	4	MTL_FIFO_DEBUG_DATA — Offset C10h on page 307	00000000h
C20h	4	MTL_INTERRUPT_STATUS — Offset C20h on page 307	00000000h
C30h	4	MTL_RXQ_DMA_MAP0 — Offset C30h on page 308	00000000h
C34h	4	MTL_RXQ_DMA_MAP1 — Offset C34h on page 310	00000000h
C40h	4	MTL_TBS_CTRL — Offset C40h on page 311	00000000h
C50h	4	MTL_EST_CONTROL — Offset C50h on page 312	00000000h
C58h	4	MTL_EST_STATUS — Offset C58h on page 313	00000000h
C60h	4	MTL_EST_SCH_ERROR — Offset C60h on page 315	00000000h
C64h	4	MTL_EST_FRM_SIZE_ERROR — Offset C64h on page 315	00000000h
C68h	4	MTL_EST_FRM_SIZE_CAPTURE — Offset C68h on page 316	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C70h	4	MTL_EST_INTR_ENABLE — Offset C70h on page 316	00000000h
C80h	4	MTL_EST_GCL_CONTROL — Offset C80h on page 317	00000000h
C84h	4	MTL_EST_GCL_DATA — Offset C84h on page 319	00000000h
C90h	4	MTL_FPE_CTRL_STS — Offset C90h on page 319	00000000h
C94h	4	MTL_FPE_ADVANCE — Offset C94h on page 320	00000000h
CC0h	4	MTL_ECC_CONTROL — Offset CC0h on page 320	00000000h
CC4h	4	MTL_SAFETY_INTERRUPT_STATUS — Offset CC4h on page 321	00000000h
CC8h	4	MTL_ECC_INTERRUPT_ENABLE — Offset CC8h on page 321	00000000h
CCCh	4	MTL_ECC_INTERRUPT_STATUS — Offset CCCh on page 322	00000000h
CD0h	4	MTL_ECC_ERR_STS_RCTL — Offset CD0h on page 323	00000000h
CD4h	4	MTL_ECC_ERR_ADDR_STATUS — Offset CD4h on page 324	00000000h
CD8h	4	MTL_ECC_ERR_CNTR_STATUS — Offset CD8h on page 324	00000000h
CE0h	4	MTL_DPP_CONTROL — Offset CE0h on page 325	00000000h
D00h	4	MTL_TXQ0_OPERATION_MODE — Offset D00h on page 326	00000000h
D04h	4	MTL_TXQ0_UNDERFLOW — Offset D04h on page 328	00000000h
D08h	4	MTL_TXQ0_DEBUG — Offset D08h on page 328	00000000h
D14h	4	MTL_TXQ0_ETS_STATUS — Offset D14h on page 329	00000000h
D18h	4	MTL_TXQ0_QUANTUM_WEIGHT — Offset D18h on page 330	00000000h
D2Ch	4	MTL_Q0_INTERRUPT_CONTROL_STATUS — Offset D2Ch on page 330	00000000h
D30h	4	MTL_RXQ0_OPERATION_MODE — Offset D30h on page 331	00000000h
D34h	4	MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT — Offset D34h on page 333	00000000h
D38h	4	MTL_RXQ0_DEBUG — Offset D38h on page 334	00000000h
D3Ch	4	MTL_RXQ0_CONTROL — Offset D3Ch on page 335	00000000h
D40h	4	MTL_TXQ1_OPERATION_MODE — Offset D40h on page 335	00000000h
D44h	4	MTL_TXQ1_UNDERFLOW — Offset D44h on page 337	00000000h
D48h	4	MTL_TXQ1_DEBUG — Offset D48h on page 337	00000000h
D50h	4	MTL_TXQ1_ETS_CONTROL — Offset D50h on page 338	00000000h
D54h	4	MTL_TXQ1_ETS_STATUS — Offset D54h on page 339	00000000h
D58h	4	MTL_TXQ1_QUANTUM_WEIGHT — Offset D58h on page 339	00000000h
D5Ch	4	MTL_TXQ1_SENDSLOPECREDIT — Offset D5Ch on page 340	00000000h
D60h	4	MTL_TXQ1_HICREDIT — Offset D60h on page 341	00000000h
D64h	4	MTL_TXQ1_LOCREDIT — Offset D64h on page 341	00000000h
D6Ch	4	MTL_Q1_INTERRUPT_CONTROL_STATUS — Offset D6Ch on page 341	00000000h
D70h	4	MTL_RXQ1_OPERATION_MODE — Offset D70h on page 342	00000000h
D74h	4	MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT — Offset D74h on page 344	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D78h	4	MTL_RXQ1_DEBUG — Offset D78h on page 345	00000000h
D7Ch	4	MTL_RXQ1_CONTROL — Offset D7Ch on page 346	00000000h
D80h	4	MTL_TXQ2_OPERATION_MODE — Offset D80h on page 347	00000000h
D84h	4	MTL_TXQ2_UNDERFLOW — Offset D84h on page 348	00000000h
D88h	4	MTL_TXQ2_DEBUG — Offset D88h on page 348	00000000h
D90h	4	MTL_TXQ2_ETS_CONTROL — Offset D90h on page 349	00000000h
D94h	4	MTL_TXQ2_ETS_STATUS — Offset D94h on page 350	00000000h
D98h	4	MTL_TXQ2_QUANTUM_WEIGHT — Offset D98h on page 350	00000000h
D9Ch	4	MTL_TXQ2_SENDSLOPECREDIT — Offset D9Ch on page 351	00000000h
DA0h	4	MTL_TXQ2_HICREDIT — Offset DA0h on page 352	00000000h
DA4h	4	MTL_TXQ2_LOCREDIT — Offset DA4h on page 352	00000000h
DACh	4	MTL_Q2_INTERRUPT_CONTROL_STATUS — Offset DACh on page 352	00000000h
DB0h	4	MTL_RXQ2_OPERATION_MODE — Offset DB0h on page 354	00000000h
DB4h	4	MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT — Offset DB4h on page 355	00000000h
DB8h	4	MTL_RXQ2_DEBUG — Offset DB8h on page 356	00000000h
DBCh	4	MTL_RXQ2_CONTROL — Offset DBCh on page 357	00000000h
DC0h	4	MTL_TXQ3_OPERATION_MODE — Offset DC0h on page 358	00000000h
DC4h	4	MTL_TXQ3_UNDERFLOW — Offset DC4h on page 359	00000000h
DC8h	4	MTL_TXQ3_DEBUG — Offset DC8h on page 359	00000000h
DD0h	4	MTL_TXQ3_ETS_CONTROL — Offset DD0h on page 360	00000000h
DD4h	4	MTL_TXQ3_ETS_STATUS — Offset DD4h on page 361	00000000h
DD8h	4	MTL_TXQ3_QUANTUM_WEIGHT — Offset DD8h on page 361	00000000h
DDCh	4	MTL_TXQ3_SENDSLOPECREDIT — Offset DDCh on page 362	00000000h
DE0h	4	MTL_TXQ3_HICREDIT — Offset DE0h on page 363	00000000h
DE4h	4	MTL_TXQ3_LOCREDIT — Offset DE4h on page 363	00000000h
DECCh	4	MTL_Q3_INTERRUPT_CONTROL_STATUS — Offset DECCh on page 363	00000000h
DF0h	4	MTL_RXQ3_OPERATION_MODE — Offset DF0h on page 365	00000000h
DF4h	4	MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT — Offset DF4h on page 366	00000000h
DF8h	4	MTL_RXQ3_DEBUG — Offset DF8h on page 367	00000000h
DFCh	4	MTL_RXQ3_CONTROL — Offset DFCh on page 368	00000000h
E2Ch	4	MTL_Q4_INTERRUPT_CONTROL_STATUS — Offset E2Ch on page 369	00000000h
E30h	4	MTL_RXQ4_OPERATION_MODE — Offset E30h on page 369	00000000h
E34h	4	MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT — Offset E34h on page 371	00000000h
E38h	4	MTL_RXQ4_DEBUG — Offset E38h on page 372	00000000h
E3Ch	4	MTL_RXQ4_CONTROL — Offset E3Ch on page 373	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E6Ch	4	MTL_Q5_INTERRUPT_CONTROL_STATUS — Offset E6Ch on page 373	00000000h
E70h	4	MTL_RXQ5_OPERATION_MODE — Offset E70h on page 374	00000000h
E74h	4	MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT — Offset E74h on page 376	00000000h
E78h	4	MTL_RXQ5_DEBUG — Offset E78h on page 377	00000000h
E7Ch	4	MTL_RXQ5_CONTROL — Offset E7Ch on page 378	00000000h
1000h	4	DMA_MODE — Offset 1000h on page 378	00000000h
1004h	4	DMA_SYSBUS_MODE — Offset 1004h on page 380	01010000h
1008h	4	DMA_INTERRUPT_STATUS — Offset 1008h on page 382	00000000h
100Ch	4	DMA_DEBUG_STATUS0 — Offset 100Ch on page 383	00000000h
1010h	4	DMA_DEBUG_STATUS1 — Offset 1010h on page 385	00000000h
1020h	4	AXI4_TX_AR_ACE_CONTROL — Offset 1020h on page 386	00000000h
1024h	4	AXI4_RX_AW_ACE_CONTROL — Offset 1024h on page 387	00000000h
1028h	4	AXI4_TXRX_AWAR_ACE_CONTROL — Offset 1028h on page 388	00000000h
1040h	4	AXI_LPI_ENTRY_INTERVAL — Offset 1040h on page 389	00000000h
1050h	4	DMA_TBS_CTRL — Offset 1050h on page 389	00000000h
1080h	4	DMA_SAFETY_INTERRUPT_STATUS — Offset 1080h on page 390	00000000h
1084h	4	DMA_ECC_INTERRUPT_ENABLE — Offset 1084h on page 391	00000000h
1088h	4	DMA_ECC_INTERRUPT_STATUS — Offset 1088h on page 391	00000000h
1100h	4	DMA_CH0_CONTROL — Offset 1100h on page 391	00000000h
1104h	4	DMA_CH0_TX_CONTROL — Offset 1104h on page 392	00000000h
1108h	4	DMA_CH0_RX_CONTROL — Offset 1108h on page 394	00000000h
1110h	4	DMA_CH0_TXDESC_LIST_ADDRESS — Offset 1110h on page 395	00000000h
1114h	4	DMA_CH0_TXDESC_LIST_ADDRESS — Offset 1114h on page 396	00000000h
1118h	4	DMA_CH0_RXDESC_LIST_ADDRESS — Offset 1118h on page 397	00000000h
111Ch	4	DMA_CH0_RXDESC_LIST_ADDRESS — Offset 111Ch on page 397	00000000h
1120h	4	DMA_CH0_TXDESC_TAIL_POINTER — Offset 1120h on page 398	00000000h
1128h	4	DMA_CH0_RXDESC_TAIL_POINTER — Offset 1128h on page 398	00000000h
112Ch	4	DMA_CH0_TXDESC_RING_LENGTH — Offset 112Ch on page 398	00000000h
1130h	4	DMA_CH0_RXDESC_RING_LENGTH — Offset 1130h on page 399	00000000h
1134h	4	DMA_CH0_INTERRUPT_ENABLE — Offset 1134h on page 399	00000000h
1138h	4	DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1138h on page 401	00000000h
113Ch	4	DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS — Offset 113Ch on page 402	000007C0h
1144h	4	DMA_CH0_CURRENT_APP_TXDESC — Offset 1144h on page 403	00000000h
114Ch	4	DMA_CH0_CURRENT_APP_RXDESC — Offset 114Ch on page 403	00000000h
1150h	4	DMA_CH0_CURRENT_APP_TXBUFFER_H — Offset 1150h on page 403	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1154h	4	DMA_CH0_CURRENT_APP_TXBUFFER — Offset 1154h on page 403	00000000h
1158h	4	DMA_CH0_CURRENT_APP_RXBUFFER_H — Offset 1158h on page 404	00000000h
115Ch	4	DMA_CH0_CURRENT_APP_RXBUFFER — Offset 115Ch on page 404	00000000h
1160h	4	DMA_CH0_STATUS — Offset 1160h on page 404	00000000h
1164h	4	DMA_CH0_MISS_FRAME_CNT — Offset 1164h on page 407	00000000h
116Ch	4	DMA_CH0_RX_ERI_CNT — Offset 116Ch on page 408	00000000h
1180h	4	DMA_CH1_CONTROL — Offset 1180h on page 408	00000000h
1184h	4	DMA_CH1_TX_CONTROL — Offset 1184h on page 409	00000000h
1188h	4	DMA_CH1_RX_CONTROL — Offset 1188h on page 411	00000000h
1190h	4	DMA_CH1_TXDESC_LIST_HADDRESS — Offset 1190h on page 413	00000000h
1194h	4	DMA_CH1_TXDESC_LIST_ADDRESS — Offset 1194h on page 413	00000000h
1198h	4	DMA_CH1_RXDESC_LIST_HADDRESS — Offset 1198h on page 414	00000000h
119Ch	4	DMA_CH1_RXDESC_LIST_ADDRESS — Offset 119Ch on page 414	00000000h
11A0h	4	DMA_CH1_TXDESC_TAIL_POINTER — Offset 11A0h on page 415	00000000h
11A8h	4	DMA_CH1_RXDESC_TAIL_POINTER — Offset 11A8h on page 415	00000000h
11ACh	4	DMA_CH1_TXDESC_RING_LENGTH — Offset 11ACh on page 416	00000000h
11B0h	4	DMA_CH1_RXDESC_RING_LENGTH — Offset 11B0h on page 416	00000000h
11B4h	4	DMA_CH1_INTERRUPT_ENABLE — Offset 11B4h on page 416	00000000h
11B8h	4	DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER — Offset 11B8h on page 418	00000000h
11BCh	4	DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS — Offset 11BCh on page 419	000007C0h
11C4h	4	DMA_CH1_CURRENT_APP_TXDESC — Offset 11C4h on page 420	00000000h
11CCh	4	DMA_CH1_CURRENT_APP_RXDESC — Offset 11CCh on page 420	00000000h
11D0h	4	DMA_CH1_CURRENT_APP_TXBUFFER_H — Offset 11D0h on page 420	00000000h
11D4h	4	DMA_CH1_CURRENT_APP_TXBUFFER — Offset 11D4h on page 421	00000000h
11D8h	4	DMA_CH1_CURRENT_APP_RXBUFFER_H — Offset 11D8h on page 421	00000000h
11DCh	4	DMA_CH1_CURRENT_APP_RXBUFFER — Offset 11DCh on page 421	00000000h
11E0h	4	DMA_CH1_STATUS — Offset 11E0h on page 422	00000000h
11E4h	4	DMA_CH1_MISS_FRAME_CNT — Offset 11E4h on page 424	00000000h
11ECh	4	DMA_CH1_RX_ERI_CNT — Offset 11ECH on page 425	00000000h
1200h	4	DMA_CH2_CONTROL — Offset 1200h on page 425	00000000h
1204h	4	DMA_CH2_TX_CONTROL — Offset 1204h on page 426	00000000h
1208h	4	DMA_CH2_RX_CONTROL — Offset 1208h on page 428	00000000h
1210h	4	DMA_CH2_TXDESC_LIST_HADDRESS — Offset 1210h on page 430	00000000h
1214h	4	DMA_CH2_TXDESC_LIST_ADDRESS — Offset 1214h on page 430	00000000h
1218h	4	DMA_CH2_RXDESC_LIST_HADDRESS — Offset 1218h on page 431	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
121Ch	4	DMA_CH2_RXDESC_LIST_ADDRESS — Offset 121Ch on page 431	00000000h
1220h	4	DMA_CH2_TXDESC_TAIL_POINTER — Offset 1220h on page 432	00000000h
1228h	4	DMA_CH2_RXDESC_TAIL_POINTER — Offset 1228h on page 432	00000000h
122Ch	4	DMA_CH2_TXDESC_RING_LENGTH — Offset 122Ch on page 432	00000000h
1230h	4	DMA_CH2_RXDESC_RING_LENGTH — Offset 1230h on page 433	00000000h
1234h	4	DMA_CH2_INTERRUPT_ENABLE — Offset 1234h on page 433	00000000h
1238h	4	DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1238h on page 435	00000000h
123Ch	4	DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS — Offset 123Ch on page 436	000007C0h
1244h	4	DMA_CH2_CURRENT_APP_TXDESC — Offset 1244h on page 437	00000000h
124Ch	4	DMA_CH2_CURRENT_APP_RXDESC — Offset 124Ch on page 437	00000000h
1250h	4	DMA_CH2_CURRENT_APP_TXBUFFER_H — Offset 1250h on page 437	00000000h
1254h	4	DMA_CH2_CURRENT_APP_TXBUFFER — Offset 1254h on page 437	00000000h
1258h	4	DMA_CH2_CURRENT_APP_RXBUFFER_H — Offset 1258h on page 438	00000000h
125Ch	4	DMA_CH2_CURRENT_APP_RXBUFFER — Offset 125Ch on page 438	00000000h
1260h	4	DMA_CH2_STATUS — Offset 1260h on page 438	00000000h
1264h	4	DMA_CH2_MISS_FRAME_CNT — Offset 1264h on page 441	00000000h
126Ch	4	DMA_CH2_RX_ERI_CNT — Offset 126Ch on page 442	00000000h
1280h	4	DMA_CH3_CONTROL — Offset 1280h on page 442	00000000h
1284h	4	DMA_CH3_TX_CONTROL — Offset 1284h on page 443	00000000h
1288h	4	DMA_CH3_RX_CONTROL — Offset 1288h on page 445	00000000h
1290h	4	DMA_CH3_RXDESC_LIST_HADDRESS — Offset 1290h on page 447	00000000h
1294h	4	DMA_CH3_RXDESC_LIST_ADDRESS — Offset 1294h on page 447	00000000h
1298h	4	DMA_CH3_RXDESC_LIST_HADDRESS — Offset 1298h on page 448	00000000h
129Ch	4	DMA_CH3_RXDESC_LIST_ADDRESS — Offset 129Ch on page 448	00000000h
12A0h	4	DMA_CH3_RXDESC_TAIL_POINTER — Offset 12A0h on page 449	00000000h
12A8h	4	DMA_CH3_RXDESC_TAIL_POINTER — Offset 12A8h on page 449	00000000h
12ACh	4	DMA_CH3_RXDESC_RING_LENGTH — Offset 12ACh on page 449	00000000h
12B0h	4	DMA_CH3_RXDESC_RING_LENGTH — Offset 12B0h on page 450	00000000h
12B4h	4	DMA_CH3_INTERRUPT_ENABLE — Offset 12B4h on page 450	00000000h
12B8h	4	DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER — Offset 12B8h on page 452	00000000h
12BCh	4	DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS — Offset 12BCh on page 453	000007C0h
12C4h	4	DMA_CH3_CURRENT_APP_TXDESC — Offset 12C4h on page 454	00000000h
12CCh	4	DMA_CH3_CURRENT_APP_RXDESC — Offset 12CCh on page 454	00000000h
12D0h	4	DMA_CH3_CURRENT_APP_TXBUFFER_H — Offset 12D0h on page 454	00000000h
12D4h	4	DMA_CH3_CURRENT_APP_TXBUFFER — Offset 12D4h on page 454	00000000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
12D8h	4	DMA_CH3_CURRENT_APP_RXBUFFER_H — Offset 12D8h on page 455	00000000h
12DCh	4	DMA_CH3_CURRENT_APP_RXBUFFER — Offset 12DCh on page 455	00000000h
12E0h	4	DMA_CH3_STATUS — Offset 12E0h on page 455	00000000h
12E4h	4	DMA_CH3_MISS_FRAME_CNT — Offset 12E4h on page 458	00000000h
12EcH	4	DMA_CH3_RX_ERI_CNT — Offset 12EcH on page 459	00000000h
1300h	4	DMA_CH4_CONTROL — Offset 1300h on page 459	00000000h
1308h	4	DMA_CH4_RX_CONTROL — Offset 1308h on page 460	00000000h
1318h	4	DMA_CH4_RXDESC_LIST_HADDRESS — Offset 1318h on page 461	00000000h
131Ch	4	DMA_CH4_RXDESC_LIST_ADDRESS — Offset 131Ch on page 462	00000000h
1328h	4	DMA_CH4_RXDESC_TAIL_POINTER — Offset 1328h on page 462	00000000h
1330h	4	DMA_CH4_RXDESC_RING_LENGTH — Offset 1330h on page 463	00000000h
1334h	4	DMA_CH4_INTERRUPT_ENABLE — Offset 1334h on page 463	00000000h
1338h	4	DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1338h on page 465	00000000h
134Ch	4	DMA_CH4_CURRENT_APP_RXDESC — Offset 134Ch on page 465	00000000h
1358h	4	DMA_CH4_CURRENT_APP_RXBUFFER_H — Offset 1358h on page 466	00000000h
135Ch	4	DMA_CH4_CURRENT_APP_RXBUFFER — Offset 135Ch on page 466	00000000h
1360h	4	DMA_CH4_STATUS — Offset 1360h on page 466	00000000h
1364h	4	DMA_CH4_MISS_FRAME_CNT — Offset 1364h on page 469	00000000h
136Ch	4	DMA_CH4_RX_ERI_CNT — Offset 136Ch on page 470	00000000h
1380h	4	DMA_CH5_CONTROL — Offset 1380h on page 470	00000000h
1388h	4	DMA_CH5_RX_CONTROL — Offset 1388h on page 471	00000000h
1398h	4	DMA_CH5_RXDESC_LIST_HADDRESS — Offset 1398h on page 472	00000000h
139Ch	4	DMA_CH5_RXDESC_LIST_ADDRESS — Offset 139Ch on page 473	00000000h
13A8h	4	DMA_CH5_RXDESC_TAIL_POINTER — Offset 13A8h on page 473	00000000h
13B0h	4	DMA_CH5_RXDESC_RING_LENGTH — Offset 13B0h on page 474	00000000h
13B4h	4	DMA_CH5_INTERRUPT_ENABLE — Offset 13B4h on page 474	00000000h
13B8h	4	DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER — Offset 13B8h on page 475	00000000h
13CCh	4	DMA_CH5_CURRENT_APP_RXDESC — Offset 13CCh on page 476	00000000h
13D8h	4	DMA_CH5_CURRENT_APP_RXBUFFER_H — Offset 13D8h on page 476	00000000h
13DCh	4	DMA_CH5_CURRENT_APP_RXBUFFER — Offset 13DCh on page 477	00000000h
13E0h	4	DMA_CH5_STATUS — Offset 13E0h on page 477	00000000h
13E4h	4	DMA_CH5_MISS_FRAME_CNT — Offset 13E4h on page 480	00000000h
13EcH	4	DMA_CH5_RX_ERI_CNT — Offset 13EcH on page 480	00000000h

11.2.1 MAC_CONFIGURATION — Offset 0h

The MAC Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31	0h RW	ARP Offload Enable (ARPEN): When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. 0x0 (DISABLE): ARP Offload is disabled. 0x1 (ENABLE): ARP Offload is enabled.	
30:28	0h RW	Source Address Insertion or Replacement Control (SARC): This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: - The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: - Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field. 0x3 (MAC0 REP_SA): Contents of MAC Addr-0 replaces SA field. 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field. 0x7 (MAC1 REP_SA): Contents of MAC Addr-1 replaces SA field.	
27	0h RW	Checksum Offload (IPC): When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. 0x0 (DISABLE): IP header/payload checksum checking is disabled. 0x1 (ENABLE): IP header/payload checksum checking is enabled.	
26:24	0h RW	Inter-Packet Gap (IPG): These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG.	

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Bit Range	Default & Access	Field Name (ID): Description
		<p>The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register.</p> <p>0x0 (IPG96): 96 bit times IPG. 0x1 (IPG88): 88 bit times IPG. 0x2 (IPG80): 80 bit times IPG. 0x3 (IPG72): 72 bit times IPG. 0x4 (IPG64): 64 bit times IPG. 0x5 (IPG56): 56 bit times IPG. 0x6 (IPG48): 48 bit times IPG. 0x7 (IPG40): 40 bit times IPG.</p>
23	0h RW	<p>Giant Packet Size Limit Control Enable (GPSLCE):</p> <p>When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit.</p> <p>When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet).</p> <p>The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status.</p> <p>0x0 (DISABLE): Giant Packet Size Limit Control is disabled. 0x1 (ENABLE): Giant Packet Size Limit Control is enabled.</p>
22	0h RW	<p>IEEE 802.3as Support for 2K Packets (S2KP):</p> <p>When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets.</p> <p>When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets.</p> <p>Note: When the JE bit is set, setting this bit has no effect on the giant packet status.</p> <p>0x0 (DISABLE): Support upto 2K packet is disabled. 0x1 (ENABLE): Support upto 2K packet is Enabled.</p>
21	0h RW	<p>CRC stripping for Type packets (CST):</p> <p>When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application.</p> <p>0x0 (DISABLE): CRC stripping for Type packets is disabled. 0x1 (ENABLE): CRC stripping for Type packets is enabled.</p>
20	0h RW	<p>Automatic Pad or CRC Stripping (ACS):</p> <p>When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.</p> <p>When this bit is reset, the MAC passes all incoming packets to the application, without any modification.</p> <p>0x0 (DISABLE): Automatic Pad or CRC Stripping is disabled. 0x1 (ENABLE): Automatic Pad or CRC Stripping is enabled.</p>
19	0h RW	<p>Watchdog Disable (WD):</p> <p>When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes.</p> <p>When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes.</p> <p>0x0 (ENABLE): Watchdog is enabled. 0x1 (DISABLE): Watchdog is disabled.</p>

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Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	Packet Burst Enable (BE): When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0x0 (DISABLE): Packet Burst is disabled. 0x1 (ENABLE): Packet Burst is enabled.
17	0h RW	Jabber Disable (JD): When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. 0x0 (ENABLE): Jabber is enabled. 0x1 (DISABLE): Jabber is disabled.
16	0h RW	Jumbo Packet Enable (JE): When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0x0 (DISABLE): Jumbo packet is disabled. 0x1 (ENABLE): Jumbo packet is enabled.
15	0h RW	Port Select (PS): This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). 0x0 (M_1000_2500M): For 1000 or 2500 Mbps operations. 0x1 (M_10_100M): For 10 or 100 Mbps operations.
14	0h RW	FES: This bit selects the speed mode. 0x0 (M_10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0. 0x1 (M_100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0.
13	0h RW	Duplex Mode (DM): When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. 0x0 (HDUPLEX): Half-duplex mode. 0x1 (FDUPLEX): Full-duplex mode.
12	0h RW	Loopback Mode (LM): When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. 0x0 (DISABLE): Loopback is disabled. 0x1 (ENABLE): Loopback is enabled.
11	0h RW	Enable Carrier Sense Before Transmission in Full-Duplex Mode (ECRSFD): When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal. 0x0 (DISABLE): ECRSFD is disabled. 0x1 (ENABLE): ECRSFD is enabled.
10	0h RW	Disable Receive Own (DO): When this bit is set, the MAC disables the reception of packets when the GMII signal TX_EN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode. 0x0 (ENABLE): Enable Receive Own. 0x1 (DISABLE): Disable Receive Own.

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Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	Disable Carrier Sense During Transmission (DCRS): When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. 0x0 (ENABLE): Enable Carrier Sense During Transmission. 0x1 (DISABLE): Disable Carrier Sense During Transmission.
8	0h RW	Disable Retry (DR): When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. 0x0 (ENABLE): Enable Retry. 0x1 (DISABLE): Disable Retry.
7	0h RO	Reserved
6:5	0h RW	Back-Off Limit (BL): The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range $0 \leq r < 2^k$ This bit is applicable only in the half-duplex mode. 0x0 (MIN_N_10): $k = \min(n, 10)$. 0x1 (MIN_N_8): $k = \min(n, 8)$. 0x2 (MIN_N_4): $k = \min(n, 4)$. 0x3 (MIN_N_1): $k = \min(n, 1)$.
4	0h RW	Deferral Check (DC): When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. 0x0 (DISABLE): Deferral check function is disabled. 0x1 (ENABLE): Deferral check function is enabled.
3:2	0h RW	Preamble Length for Transmit packets (PRELEN): These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 0x0 (M_7BYTES): 7 bytes of preamble. 0x1 (M_5BYTES): 5 bytes of preamble. 0x2 (M_3BYTES): 3 bytes of preamble. 0x3 (RESERVED): Reserved.
1	0h RW	Transmitter Enable (TE):

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Bit Range	Default & Access	Field Name (ID): Description
		When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. 0x0 (DISABLE): Transmitter is disabled. 0x1 (ENABLE): Transmitter is enabled.
0	0h RW	Receiver Enable (RE): When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. 0x0 (DISABLE): Receiver is disabled. 0x1 (ENABLE): Receiver is enabled.

11.2.2 MAC_EXT_CONFIGURATION — Offset 4h

The MAC Extended Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:25	00h RW	Extended Inter-Packet Gap (EIPG): The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ----- 8'hFF - 2144 bit times
24	0h RW	Extended Inter-Packet Gap Enable (EIPGEN): When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. 0x0 (DISABLE): Extended Inter-Packet Gap is disabled. 0x1 (ENABLE): Extended Inter-Packet Gap is enabled.
23	0h RO	Reserved
22:20	0h RW	Maximum Size for Splitting the Header Data (HDSMS): These bits indicate the maximum header size allowed for splitting the header data in the received packet. 0x0 (M_64BYTES): Maximum Size for Splitting the Header Data is 64 bytes. 0x1 (M_128BYTES): Maximum Size for Splitting the Header Data is 128 bytes. 0x2 (M_256BYTES): Maximum Size for Splitting the Header Data is 256 bytes.

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Bit Range	Default & Access	Field Name (ID): Description
		0x3 (M_512BYTES): Maximum Size for Splitting the Header Data is 512 bytes. 0x4 (M_1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes. 0x5 (RSVD): Reserved.
19	0h RW	Packet Duplication Control (PDC): When this bit is set, the received packet with Multicast/Broadcast Destination address is routed to multiple Receive DMA Channels. The Receive DMA Channels is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Multicast/Broadcast Destination address in the received packet. The DCS field is interpreted to be a one-hot value, each bit corresponding to the Receive DMA Channel. When this bit is reset, the received packet is routed to single Receive DMA Channel. The Receive DMA Channel is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Destination address in the received packet. The DCS field is interpreted as a binary value. 0x0 (DISABLE): Packet Duplication Control is disabled. 0x1 (ENABLE): Packet Duplication Control is enabled.
18	0h RW	Unicast Slow Protocol Packet Detect (USP): When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. 0x0 (DISABLE): Unicast Slow Protocol Packet Detection is disabled. 0x1 (ENABLE): Unicast Slow Protocol Packet Detection is enabled.
17	0h RW	Slow Protocol Detection Enable (SPEN): When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. 0x0 (DISABLE): Slow Protocol Detection is disabled. 0x1 (ENABLE): Slow Protocol Detection is enabled.
16	0h RW	Disable CRC Checking for Received Packets (DCRCC): When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. 0x0 (ENABLE): CRC Checking is enabled. 0x1 (DISABLE): CRC Checking is disabled.
15:14	0h RO	Reserved
13:0	0000h RW	Giant Packet Size Limit (GPSL): If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

11.2.3 MAC_PACKET_FILTER — Offset 8h

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Receive All (RA): When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled. 0x1 (ENABLE): Receive All is enabled.
30:22	0h RO	Reserved
21	0h RW	Drop Non-TCP/UDP over IP Packets (DNTU): When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0 (FWD): Forward Non-TCP/UDP over IP Packets. 0x1 (DROP): Drop Non-TCP/UDP over IP Packets.
20	0h RW	Layer 3 and Layer 4 Filter Enable (IPFE): When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled. 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled.
19:17	0h RO	Reserved
16	0h RW	VLAN Tag Filter Enable (VTFE): When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. 0x0 (DISABLE): VLAN Tag Filter is disabled. 0x1 (ENABLE): VLAN Tag Filter is enabled.
15:11	0h RO	Reserved
10	0h RW	Hash or Perfect Filter (HPF): When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. 0x0 (DISABLE): Hash or Perfect Filter is disabled. 0x1 (ENABLE): Hash or Perfect Filter is enabled.
9	0h RW	Source Address Filter Enable (SAF): When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in Ethernet Controller, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): SA Filtering is disabled. 0x1 (ENABLE): SA Filtering is enabled.
8	0h RW	SA Inverse Filtering (SAIF): When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0 (DISABLE): SA Inverse Filtering is disabled. 0x1 (ENABLE): SA Inverse Filtering is enabled.
7:6	0h RW	Pass Control Packets (PCF): These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0x0 (FLTR_ALL): MAC filters all control packets from reaching the application. 0x1 (FW_XCPT_PAU): MAC forwards all control packets except Pause packets to the application even if they fail the Address filter. 0x2 (FW_ALL): MAC forwards all control packets to the application even if they fail the Address filter. 0x3 (FW_PASS): MAC forwards the control packets that pass the Address filter.
5	0h RW	Disable Broadcast Packets (DBF): When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. 0x0 (ENABLE): Enable Broadcast Packets. 0x1 (DISABLE): Disable Broadcast Packets.
4	0h RW	Pass All Multicast (PM): When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. 0x0 (DISABLE): Pass All Multicast is disabled. 0x1 (ENABLE): Pass All Multicast is enabled.
3	0h RW	DA Inverse Filtering (DAIF): When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. 0x0 (DISABLE): DA Inverse Filtering is disabled. 0x1 (ENABLE): DA Inverse Filtering is enabled.
2	0h RW	Hash Multicast (HMC): When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Multicast is disabled. 0x1 (ENABLE): Hash Multicast is enabled.
1	0h RW	Hash Unicast (HUC): When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Unicast is disabled. 0x1 (ENABLE): Hash Unicast is enabled.
0	0h RW	Promiscuous Mode (PR):

Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set.</p> <p>0x0 (DISABLE): Promiscuous Mode is disabled. 0x1 (ENABLE): Promiscuous Mode is enabled.</p>

11.2.4 MAC_WATCHDOG_TIMEOUT—Offset Ch

The Watchdog Timeout register controls the watchdog timeout for received packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RW	<p>Programmable Watchdog Enable (PWE): When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register.</p> <p>0x0 (DISABLE): Programmable Watchdog is disabled. 0x1 (ENABLE): Programmable Watchdog is enabled.</p>
7:4	0h RO	Reserved
3:0	0h RW	<p>Watchdog Timeout (WTO): When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet.</p> <p>Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped.</p> <p>0x0 (M_2KBYTES): 2 KB. 0x1 (M_3KBYTES): 3 KB. 0x2 (M_4KBYTES): 4 KB. 0x3 (M_5KBYTES): 5 KB. 0x4 (M_6KBYTES): 6 KB. 0x5 (M_7KBYTES): 7 KB. 0x6 (M_8KBYTES): 8 KB. 0x7 (M_9KBYTES): 9 KB. 0x08 (M_10KBYTES): 10 KB. 0x09 (M_11KBYTES): 11 KB. 0x0A (M_12KBYTES): 12 KB. 0x0B (M_13KBYTES): 13 KB. 0x0C (M_14KBYTES): 14 KB. 0x0D (M_15KBYTES): 15 KB. 0x0E (M_16383BYTES): 16383 Bytes. 0x0F (RESERVED): Reserved.</p>

11.2.5 MAC_HASH_TABLE_REG0 — Offset 10h

The Hash Table Register 0 contains the first 32 bits of the hash table, when the width of the hash table is 128 or 256 bits. This design has set the Hash Table Size (width of the hash table) to 64.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RW	MAC Hash Table First 32 Bits (HT31T0): This field contains the first 32 Bits [31:0] of the Hash table.

11.2.6 MAC_HASH_TABLE_REG1 — Offset 14h

The Hash Table Register 1 contains the second 32 bits of the hash table.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-

bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:0	0000000h RW	MAC Hash Table Second 32 Bits (HT63T32): This field contains the second 32 Bits [63:32] of the Hash table.	

11.2.7 MAC_VLAN_TAG_CTRL — Offset 50h

This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31	0h RW	Enable Inner VLAN Tag in Rx Status (EIVLRS): When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled. 0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled.	
30	0h RO	Reserved	
29:28	0h RW	Enable Inner VLAN Tag Stripping on Receive (EIVLS): This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0 (DONOT): Do not strip.	

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
27	0h RW	Enable Inner VLAN Tag Comparison (ERIVLT): When this bit, VTHM bit and the EDVLP field are set, the MAC receiver enables VLAN Hash filtering operation on the inner VLAN Tag (if present). When this bit is reset and VTHM bit is set, the MAC receiver enables VLAN Hash filtering operation on the outer VLAN Tag (if present). The ERSVLM bit and DOVLTC bit determines which VLAN type is enabled for filtering. 0x0 (DISABLE): Inner VLAN tag is disabled. 0x1 (ENABLE): Inner VLAN tag is enabled.
26	0h RW	Enable Double VLAN Processing (EDVLP): When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0 (DISABLE): Double VLAN Processing is disabled. 0x1 (ENABLE): Double VLAN Processing is enabled.
25	0h RW	VLAN Tag Hash Table Match Enable (VTHM): When this bit is set, the most significant four bits of CRC of VLAN Tag are (ones-complement of most significant four bits of CRC of VLAN Tag when ETV bit is reset) used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled. 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled.
24	0h RW	Enable VLAN Tag in Rx status (EVLRXS): When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. 0x0 (DISABLE): VLAN Tag in Rx status is disabled. 0x1 (ENABLE): VLAN Tag in Rx status is enabled.
23	0h RO	Reserved
22:21	0h RW	Enable VLAN Tag Stripping on Receive (EVLS): This field indicates the stripping operation on the outer VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
20	0h RW	Disable VLAN Type Check for VLAN Hash Filtering (DOVLTC): When this bit is set, the MAC VLAN Hash Filter does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC VLAN Hash Filter filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. 0x0 (ENABLE): VLAN Type Check is enabled. 0x1 (DISABLE): VLAN Type Check is disabled.
19	0h RW	Enable Receive S-VLAN Match for VLAN Hash Filtering (ERSVLM): When this bit is set, the MAC receiver enables VLAN Hash filtering or matching for SVLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables VLAN Hash filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for VLAN Hash filtering or matching.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	Enable S-VLAN (ESVL): When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. 0x0 (DISABLE): S-VLAN is disabled. 0x1 (ENABLE): S-VLAN is enabled.
17	0h RW	VLAN Tag Inverse Match Enable (VTIM): When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. 0x0 (DISABLE): VLAN Tag Inverse Match is disabled. 0x1 (ENABLE): VLAN Tag Inverse Match is enabled.
16	0h RW	Enable 12-Bit VLAN Tag Comparison for VLAN Hash Filtering (ETV): When this bit is set, a 12-bit VLAN identifier is used for VLAN Hash filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag in the received VLAN-tagged packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for VLAN hash filtering. 0x0 (DISABLE): 12-Bit VLAN Tag Comparison is disabled. 0x1 (ENABLE): 12-Bit VLAN Tag Comparison is enabled.
15:5	0h RO	Reserved
4:2	0h RW	OFS: This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	0h RW	Command Type (CT): This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation. 0x0 (WRITE): Write operation. 0x1 (READ): Read operation.
0	0h RW	Operation Busy (OB): This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset. 0x0 (DISABLE): Operation Busy is disabled. 0x1 (ENABLE): Operation Busy is enabled.

11.2.8 MAC_VLAN_TAG_DATA — Offset 54h

This register holds the read/write data for Indirect Access of the Per VLAN Tag registers. During the read access, this field contains valid read data only after the OB bit is reset.

During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27:25	0h RW	DMA Channel Number (DMACHN): The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	0h RW	DMA Channel Number Enable (DMACHEN): This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing. 0x0 (DISABLE): DMA Channel Number is disabled. 0x1 (ENABLE): DMA Channel Number is enabled.
23:21	0h RO	Reserved
20	0h RW	Enable Inner VLAN Tag Comparison (ERIVLT): This bit is valid only when Double VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). 0x0 (DISABLE): Inner VLAN tag comparison is disabled. 0x1 (ENABLE): Inner VLAN tag comparison is enabled.
19	0h RW	Enable S-VLAN Match for received Frames (ERSVLM): This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	Disable VLAN Type Comparison (DOVLTC): This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit. 0x0 (ENABLE): VLAN type comparison is enabled. 0x1 (DISABLE): VLAN type comparison is disabled.
17	0h RW	12bits or 16bits VLAN comparison (ETV): This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. 0x0 (M_16BIT): 16 bit VLAN comparison. 0x1 (M_12BIT): 12 bit VLAN comparison.
16	0h RW	VLAN Tag Enable (VEN): This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID.

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Bit Range	Default & Access	Field Name (ID): Description
		When this bit is reset, no comparison is performed irrespective of the programming of the other fields. 0x0 (DISABLE): VLAN Tag is disabled. 0x1 (ENABLE): VLAN Tag is enabled.
15:0	0000h RW	VLAN Tag ID (VID): This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

11.2.9 MAC_VLAN_HASH_TABLE – Offset 58h

When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. The upper four bits of the calculated hash value are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3).
- Perform bitwise reversal for the value obtained in step 1.
- Take the upper four bits from the value obtained in step 2.

If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] of this register are written.

- If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:0	0000h RW	VLAN Hash Table (VLHT): This field contains the 16-bit VLAN Hash Table.

11.2.10 MAC_VLAN_INCL – Offset 60h

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	<p>BUSY: This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register. 0x0 (INACTIVE): Busy status not detected. 0x1 (ACTIVE): Busy status detected.</p>
30	0h RW	<p>Read write control (RDWR): This bit controls the read or write operation for indirectly accessing the queue/channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset. 0x0 (READ): Read operation of indirect access. 0x1 (WRITE): Write operation of indirect access.</p>
29:26	0h RO	Reserved
25:24	0h RW	<p>ADDR: This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset.</p>
23:22	0h RO	Reserved
21	0h RW	<p>Channel based tag insertion (CBTI): When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTi, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTi, VLP, VLC and VLT fields of this register. 0x0 (DISABLE): Channel based tag insertion is disabled. 0x1 (ENABLE): Channel based tag insertion is enabled.</p>
20	0h RW	<p>VLAN Tag Input (VLTi): When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.</p>
19	0h RW	<p>C-VLAN or S-VLAN (CSVL): When this bit is set, S-VLAN type (0x88A8) is inserted in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted in the 13th and 14th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.</p>
18	0h RW	<p>VLAN Priority Control (VLP): When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.</p>
17:16	0h RW	<p>VLC: VLAN Tag Control in Transmit Packets <ul style="list-style-type: none"> - 2'00: No VLAN tag deletion, insertion, or replacement - 2'01: VLAN tag deletion <p>The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags.</p> <ul style="list-style-type: none"> - 2'b10: VLAN tag insertion <p>The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag.</p> <ul style="list-style-type: none"> - 2'b11: VLAN tag replacement <p>The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8).</p> <p>Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.</p> <p>0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.</p> </p>
15:0	0000h RW	<p>VLAN Tag for Transmit Packets (VLT): This field contains the value of the VLAN tag to be inserted. The value must only be changed when the transmit lines are inactive or during the initialization phase.</p> <p>Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag.</p> <p>The following list describes the bits of this field:</p> <ul style="list-style-type: none"> - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

11.2.11 MAC_INNER_VLAN_INCL – Offset 64h

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved
20	0h RW	<p>VLAN Tag Input (VLI): When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from:</p> <ul style="list-style-type: none"> - The Tx descriptor <p>0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.</p>
19	0h	C-VLAN or S-VLAN (CSVL):

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Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 17th and 18th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 17th and 18th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.
18	0h RW	VLAN Priority Control (VLP): When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	VLC: VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	VLAN Tag for Transmit Packets (VLT): This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

11.2.12 MAC_Q0_TX_FLOW_CTRL — Offset 70h

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The Busy bit remains set until the control packet is transferred onto the cable. The application must make sure that the Busy bit is cleared before writing to the register.

When the PFCE bit in the MAC_Rx_Flow_Ctrl register is enabled, this register controls the generation of Priority Flow Control (PFC) frames with priorities mapped according to PSRQ0 in the MAC_RxQ_Ctrl2 register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	<p>Pause Time (PT): This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.</p>
15:8	0h RO	Reserved
7	0h RW	<p>Disable Zero-Quanta Pause (DZPQ): When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal <code>sbd_flowctrl_i</code> or <code>mti_flowctrl_i</code>). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.</p>
6:4	0h RW	<p>Pause Low Threshold (PLT): This field configures the threshold of the Pause timer at which the input flow control signal <code>mti_flowctrl_i</code> (or <code>sbd_flowctrl_i</code>) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the <code>mti_flowctrl_i</code> signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.</p>
3:2	0h RO	Reserved
1	0h RW	<p>Transmit Flow Control Enable (TFE): Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.</p>
0	0h RW	<p>Flow Control Busy or Backpressure Activate (FCB_BPA): This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode:</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared.</p> <p>Half-Duplex Mode:</p> <p>When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled.</p> <p>0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.</p>

11.2.13 MAC_Q1_TX_FLOW_CTRL — Offset 74h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	<p>Pause Time (PT):</p> <p>This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.</p>
15:8	0h RO	<p>Reserved</p>
7	0h RW	<p>Disable Zero-Quanta Pause (DZPQ):</p> <p>When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i).</p> <p>When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled.</p> <p>0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled.</p> <p>0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.</p>
6:4	0h RW	<p>Pause Low Threshold (PLT):</p> <p>This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted.</p> <p>The following list provides the threshold values for different values.</p> <p>The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.</p> <p>This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.</p> <p>0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times).</p> <p>0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times).</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	Reserved
1	0h RW	Transmit Flow Control Enable (TFE): When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	Flow Control Busy (FCB_BPA): This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

11.2.14 MAC_Q2_TX_FLOW_CTRL — Offset 78h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	Pause Time (PT): This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	Reserved
7	0h RW	Disable Zero-Quanta Pause (DZPQ): When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mtl_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	Pause Low Threshold (PLT): This field configures the threshold of the Pause timer at which the input flow control signal mtl_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted.</p> <p>The following list provides the threshold values for different values.</p> <p>The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.</p> <p>This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.</p> <ul style="list-style-type: none"> 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	Reserved
1	0h RW	<p>Transmit Flow Control Enable (TFE):</p> <p>When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets.</p> <ul style="list-style-type: none"> 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	<p>Flow Control Busy (FCB_BPA):</p> <p>This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <ul style="list-style-type: none"> 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

11.2.15 MAC_Q3_TX_FLOW_CTRL — Offset 7Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	<p>Pause Time (PT):</p> <p>This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.</p>
15:8	0h RO	Reserved
7	0h RW	Disable Zero-Quanta Pause (DZPQ):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i).</p> <p>When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled.</p> <p>0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.</p>
6:4	0h RW	<p>Pause Low Threshold (PLT):</p> <p>This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted.</p> <p>The following list provides the threshold values for different values.</p> <p>The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.</p> <p>This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.</p> <ul style="list-style-type: none"> 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	Reserved
1	0h RW	<p>Transmit Flow Control Enable (TFE):</p> <p>When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets.</p> <p>0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.</p>
0	0h RW	<p>Flow Control Busy (FCB_BPA):</p> <p>This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.</p>

11.2.16 MAC_Q4_TX_FLOW_CTRL — Offset 80h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	<p>Pause Time (PT): This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.</p>
15:8	0h RO	Reserved
7	0h RW	<p>Disable Zero-Quanta Pause (DZPQ): When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.</p>
6:4	0h RW	<p>Pause Low Threshold (PLT): This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.</p>
3:2	0h RO	Reserved
1	0h RW	<p>Transmit Flow Control Enable (TFE): When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.</p>
0	0h RW	<p>Flow Control Busy (FCB_BPA): This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.</p>

11.2.17 MAC_Q5_TX_FLOW_CTRL — Offset 84h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	Pause Time (PT): This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	Reserved
7	0h RW	Disable Zero-Quanta Pause (DZPQ): When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sdb_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	Pause Low Threshold (PLT): This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sdb_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	Reserved
1	0h RW	Transmit Flow Control Enable (TFE): When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	Flow Control Busy (FCB_BPA):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.</p>

11.2.18 MAC_RX_FLOW_CTRL — Offset 90h

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RW	<p>Priority Based Flow Control Enable (PFCE): When this bit is set, it enables generation and reception of priority-based flow control (PFC) packets. When this bit is reset, it enables generation and reception of 802.3x Pause control packets.</p> <p>0x0 (DISABLE): Priority Based Flow Control is disabled. 0x1 (ENABLE): Priority Based Flow Control is enabled.</p>
7:2	0h RO	Reserved
1	0h RW	<p>Unicast Pause Packet Detect (UP): A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address.</p> <p>Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011.</p> <p>0x0 (DISABLE): Unicast Pause Packet Detect disabled. 0x1 (ENABLE): Unicast Pause Packet Detect enabled.</p>
0	0h RW	<p>Receive Flow Control Enable (RFE): When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled.</p> <p>When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time.</p> <p>0x0 (DISABLE): Receive Flow Control is disabled. 0x1 (ENABLE): Receive Flow Control is enabled.</p>

11.2.19 MAC_RXQ_CTRL4 — Offset 94h

The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:17	0h RW	VLAN Tag Filter Fail Packets Queue (VFFQ): This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	0h RW	VLAN Tag Filter Fail Packets Queuing Enable (VFFQE): When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled.
15:12	0h RO	Reserved
11:9	0h RW	Multicast Address Filter Fail Packets Queue. (MFFQ): This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
8	0h RW	Multicast Address Filter Fail Packets Queuing Enable. (MFFQE): When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled.
7:4	0h RO	Reserved
3:1	0h RW	Unicast Address Filter Fail Packets Queue. (UFFQ): This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	0h RW	Unicast Address Filter Fail Packets Queuing Enable. (UFFQE): When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled.

11.2.20 MAC_TXQ_PRTY_MAP0 — Offset 98h

The Transmit Queue Priority Mapping 0 register contains the priority values assigned to Tx Queue 0 through Tx Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	Priorities Selected in Transmit Queue 3 (PSTQ3): This bit is similar to the PSTQ0 bit.
23:16	00h RW	Priorities Selected in Transmit Queue 2 (PSTQ2): This bit is similar to the PSTQ0 bit.
15:8	00h RW	Priorities Selected in Transmit Queue 1 (PSTQ1): This bit is similar to the PSTQ0 bit.
7:0	00h RW	Priorities Selected in Transmit Queue 0 (PSTQ0): This field holds the priorities assigned to Tx Queue 0 by the software. This field determines if Tx Queue 0 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

11.2.21 MAC_RXQ_CTRL0 — Offset A0h

The Receive Queue Control 0 register controls the queue management in the MAC Receiver.

NOTE

In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:10	0h RW	Receive Queue 5 Enable (RXQ5EN): This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
9:8	0h RW	Receive Queue 4 Enable (RXQ4EN): This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
7:6	0h RW	Receive Queue 3 Enable (RXQ3EN): This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

continued...

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	Receive Queue 2 Enable (RXQ2EN): This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
3:2	0h RW	Receive Queue 1 Enable (RXQ1EN): This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
1:0	0h RW	Receive Queue 0 Enable (RXQ0EN): This field indicates whether Rx Queue 0 is enabled for AV or DCB. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

11.2.22 MAC_RXQ_CTRL1 — Offset A4h

The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved
26:24	0h RW	Frame Preemption Residue Queue (FPRQ): This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.
23:22	0h RW	Tagged PTP over Ethernet Packets Queuing Control. (TPQC): This field controls the routing of the VLAN Tagged PTPoE packets. The following programmable options are allowed. <ul style="list-style-type: none"> - 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). - 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). - 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. - 2'b11: Reserved. If DWC_EQOS_AV_ENABLE is not selected in the configuration, the following programmable options are allowed. <ul style="list-style-type: none"> - 1'b0: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for DCB/Generic enabled Rx Queues). - 1'b1: VLAN Tagged PTPoE packets are routed to Rx Queues specified by PTPQ field.

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Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	Tagged AV Control Packets Queueing Enable. (TACPQE): When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers. 0x0 (DISABLE): Tagged AV Control Packets Queueing is disabled. 0x1 (ENABLE): Tagged AV Control Packets Queueing is enabled.
20	0h RW	Multicast and Broadcast Queue Enable (MCBCQEN): This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. 0x0 (DISABLE): Multicast and Broadcast Queue is disabled. 0x1 (ENABLE): Multicast and Broadcast Queue is enabled.
19	0h RO	Reserved
18:16	0h RW	Multicast and Broadcast Queue (MCBCQ): This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
15	0h RO	Reserved
14:12	0h RW	Untagged Packet Queue (UPQ): This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
11	0h RO	Reserved
10:8	0h RW	DCB Control Packets Queue (DCBCPQ): This field specifies the Rx queue on which the received DCB control packets are routed. The DCB data packets are routed based on the PSRQ field of the Transmit Flow Control Register of corresponding queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6.

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Bit Range	Default & Access	Field Name (ID): Description
		0x7 (QUEUE7): Receive Queue 7.
7	0h RO	Reserved
6:4	0h RW	<p>PTP Packets Queue (PTPQ): This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPOE packets can be routed to this Rx Queue.</p> <ul style="list-style-type: none"> 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
3	0h RO	Reserved
2:0	0h RW	<p>AV Untagged Control Packets Queue (AVCPQ): This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field.</p> <ul style="list-style-type: none"> 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.

11.2.23 MAC_RXQ_CTRL2 – Offset A8h

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	<p>Priorities Selected in the Receive Queue 3 (PSRQ3): This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 3 crosses the flow control threshold settings.
23:16	00h RW	<p>Priorities Selected in the Receive Queue 2 (PSRQ2):</p> <p>This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2.</p> <p>For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.</p> <p>this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 2 crosses the flow control threshold settings.</p>
15:8	00h RW	<p>Priorities Selected in the Receive Queue 1 (PSRQ1):</p> <p>This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1.</p> <p>For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.</p> <p>this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.</p>
7:0	00h RW	<p>Priorities Selected in the Receive Queue 0 (PSRQ0):</p> <p>This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0.</p> <p>For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.</p> <p>this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.</p>

11.2.24 MAC_RXQ_CTRL3 — Offset ACh

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 4 to 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:8	00h RW	<p>Priorities Selected in the Receive Queue 5 (PSRQ5):</p> <p>This field decides the priorities assigned to Rx Queue 5. All packets with priorities that match the values set in this field are routed to Rx Queue 5.</p> <p>For example, if PSRQ5[6] is set, packets with USP field equal to 6 are routed to Rx Queue 5. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.</p> <p>this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 5 crosses the flow control threshold settings.</p>
7:0	00h RW	<p>Priorities Selected in the Receive Queue 4 (PSRQ4):</p> <p>This field decides the priorities assigned to Rx Queue 4. All packets with priorities that match the values set in this field are routed to Rx Queue 4.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		For example, if PSRQ4[7:4] is set, packets with USP field equal to 7, 6, 5, or 4 are routed to Rx Queue 4. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 4 crosses the flow control threshold settings.

11.2.25 MAC_INTERRUPT_STATUS — Offset B0h

The Interrupt Status register contains the status of interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved
20	0h RO/V	MMC FPE Receive Interrupt Status (MFRIS): This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active. 0x1 (ACTIVE): MMC FPE Receive Interrupt status active.
19	0h RO/V	MMC FPE Transmit Interrupt Status (MFTIS): This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active. 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active.
18	0h RO/V	MDIO Interrupt Status (MDIOIS): This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): MDIO Interrupt status not active. 0x1 (ACTIVE): MDIO Interrupt status active.
17	0h RO/V	Frame Preemption Interrupt Status (FPEIS): This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt. 0x0 (INACTIVE): Frame Preemption Interrupt status not active. 0x1 (ACTIVE): Frame Preemption Interrupt status active.
16	0h RO	Reserved
15	0h RO/V	GPI Interrupt Status (GPIIS): When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field of the MAC_GPIO_Status register and the corresponding GPIE bit is enabled in the MAC_GPIO_Control register. This bit is cleared on reading lane 0 (GPIS) of the MAC_GPIO_Status register. 0x0 (INACTIVE): GPI Interrupt status not active.

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): GPI Interrupt status active.
14	0h RO/V	<p>Receive Status Interrupt (RXSTSIS): This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.</p> <p>0x0 (INACTIVE): Receive Interrupt status not active. 0x1 (ACTIVE): Receive Interrupt status active.</p>
13	0h RO/V	<p>Transmit Status Interrupt (TXSTSIS): This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register:</p> <ul style="list-style-type: none"> - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) <p>This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.</p> <p>0x0 (INACTIVE): Transmit Interrupt status not active. 0x1 (ACTIVE): Transmit Interrupt status active.</p>
12	0h RO/V	<p>Timestamp Interrupt Status (TSIS): If the Timestamp feature is enabled, this bit is set when any of the following conditions is true:</p> <ul style="list-style-type: none"> - The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. - There is an overflow in the Seconds register. - The Target Time Error occurred, that is, programmed target time already elapsed. <p>If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted.</p> <p>In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers.</p> <p>When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets.</p> <p>This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register.</p> <p>0x0 (INACTIVE): Timestamp Interrupt status not active. 0x1 (ACTIVE): Timestamp Interrupt status active.</p>
11	0h RO/V	<p>MMC Receive Checksum Offload Interrupt Status (MMCRXIPIS): This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared.</p> <p>This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options.</p> <p>0x0 (INACTIVE): MMC Receive Checksum Offload Interrupt status not active. 0x1 (ACTIVE): MMC Receive Checksum Offload Interrupt status active.</p>
10	0h RO/V	<p>MMC Transmit Interrupt Status (MMCTXIS): This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared.</p> <p>This bit is valid only when you select the Enable MAC Management Counters (MMC) option.</p> <p>0x0 (INACTIVE): MMC Transmit Interrupt status not active. 0x1 (ACTIVE): MMC Transmit Interrupt status active.</p>

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Bit Range	Default & Access	Field Name (ID): Description
9	0h RO/V	MMC Receive Interrupt Status (MMCRXIS): This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Receive Interrupt status not active. 0x1 (ACTIVE): MMC Receive Interrupt status active.
8	0h RO/V	MMC Interrupt Status (MMCIS): This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Interrupt status not active. 0x1 (ACTIVE): MMC Interrupt status active.
7:6	0h RO	Reserved
5	0h RO/V	LPI Interrupt Status (LPIIS): When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): LPI Interrupt status not active. 0x1 (ACTIVE): LPI Interrupt status active.
4	0h RO/V	PMT Interrupt Status (PMTIS): This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. 0x0 (INACTIVE): PMT Interrupt status not active. 0x1 (ACTIVE): PMT Interrupt status active.
3	0h RO/V	PHY Interrupt (PHYIS): This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): PHY Interrupt not detected. 0x1 (ACTIVE): PHY Interrupt detected.
2:1	0h RO	Reserved
0	0h RO/V	RGMII or SMII Interrupt Status (RGSMIIIS): This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active. 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active.

11.2.26 MAC_INTERRUPT_ENABLE – Offset B4h

The Interrupt Enable register contains the masks for generating the interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved
18	0h RW	MDIO Interrupt Enable (MDIOIE): When this bit is set, it enables the assertion of the interrupt when MDIOS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): MDIO Interrupt is disabled. 0x1 (ENABLE): MDIO Interrupt is enabled.
17	0h RW	Frame Preemption Interrupt Enable (FPEIE): When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): Frame Preemption Interrupt is disabled. 0x1 (ENABLE): Frame Preemption Interrupt is enabled.
16:15	0h RO	Reserved
14	0h RW	Receive Status Interrupt Enable (RXSTSIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Receive Status Interrupt is disabled. 0x1 (ENABLE): Receive Status Interrupt is enabled.
13	0h RW	Transmit Status Interrupt Enable (TXSTSIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Status Interrupt is disabled. 0x1 (ENABLE): Timestamp Status Interrupt is enabled.
12	0h RW	Timestamp Interrupt Enable (TSIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Interrupt is disabled. 0x1 (ENABLE): Timestamp Interrupt is enabled.
11:6	0h RO	Reserved
5	0h RW	LPI Interrupt Enable (LPIIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): LPI Interrupt is disabled. 0x1 (ENABLE): LPI Interrupt is enabled.
4	0h RW	PMT Interrupt Enable (PMTIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PMT Interrupt is disabled. 0x1 (ENABLE): PMT Interrupt is enabled.
3	0h RW	PHY Interrupt Enable (PHYIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PHY Interrupt is disabled.

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ENABLE): PHY Interrupt is enabled.
2:1	0h RO	Reserved
0	0h RW	RGMII or SMII Interrupt Enable (RGSMIIIE): When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): RGMII or SMII Interrupt is disabled. 0x1 (ENABLE): RGMII or SMII Interrupt is enabled.

11.2.27 MAC_RX_TX_STATUS — Offset B8h

The Receive Transmit Status register contains the Receive and Transmit Error status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RO/V	Receive Watchdog Timeout (RWT): This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No receive watchdog timeout. 0x1 (ACTIVE): Receive watchdog timed out.
7:6	0h RO	Reserved
5	0h RO/V	Excessive Collisions (EXCOL): When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Excessive collision is sensed.
4	0h RO/V	Late Collision (LCOL): When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Late collision is sensed.
3	0h RO/V	Excessive Deferral (EXDEF):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled).</p> <p>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): No Excessive deferral. 0x1 (ACTIVE): Excessive deferral.</p>
2	0h RO/V	<p>Loss of Carrier (LCARR):</p> <p>When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision.</p> <p>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): Loss of carrier.</p>
1	0h RO/V	<p>No Carrier (NCARR):</p> <p>When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission.</p> <p>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): No carrier.</p>
0	0h RO/V	<p>Transmit Jabber Timeout (TJT):</p> <p>This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register.</p> <p>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): No Transmit Jabber Timeout. 0x1 (ACTIVE): Transmit Jabber Timeout occurred.</p>

11.2.28 MAC_PMT_CONTROL_STATUS — Offset C0h

The PMT Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	<p>Remote Wake-Up Packet Filter Register Pointer Reset (RWKFILTRST):</p> <p>When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Remote Wake-Up Packet Filter Register Pointer is not Reset. 0x1 (ENABLE): Remote Wake-Up Packet Filter Register Pointer is Reset.</p>
30:29	0h RO	Reserved
28:24	00h	Remote Wake-up FIFO Pointer (RWKPTR):

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Bit Range	Default & Access	Field Name (ID): Description
	RO/V	This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	0h RO	Reserved
10	0h RW	<p>Remote Wake-up Packet Forwarding Enable (RWKPFE): When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high.</p> <p>Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-up Packet Forwarding is disabled. 0x1 (ENABLE): Remote Wake-up Packet Forwarding is enabled.</p>
9	0h RW	<p>Global Unicast (GLBLUCAST): When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. 0x0 (DISABLE): Global unicast is disabled. 0x1 (ENABLE): Global unicast is enabled.</p>
8:7	0h RO	Reserved
6	0h RO/V	<p>Remote Wake-Up Packet Received (RWKPRCVD): When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Remote wake-up packet is received. 0x1 (ACTIVE): Remote wake-up packet is received.</p>
5	0h RO/V	<p>Magic Packet Received (MGKPRCVD): When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Magic packet is received. 0x1 (ACTIVE): Magic packet is received.</p>
4:3	0h RO	Reserved
2	0h RW	<p>Remote Wake-Up Packet Enable (RWKPKTEN): When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. 0x0 (DISABLE): Remote wake-up packet is disabled. 0x1 (ENABLE): Remote wake-up packet is enabled.</p>
1	0h RW	Magic Packet Enable (MGKPKTEN):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set, a power management event is generated when the MAC receives a magic packet.</p> <p>0x0 (DISABLE): Magic Packet is disabled. 0x1 (ENABLE): Magic Packet is enabled.</p>
0	0h RW	<p>Power Down (PWRDWN):</p> <p>When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high.</p> <p>Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Power down is disabled. 0x1 (ENABLE): Power down is enabled.</p>

11.2.29 MAC_RWK_PACKET_FILTER — Offset C4h

The TSN-Ethernet implements a filter lookup table programmed through the MAC_RWK_Packet_Filter register in which CRC, offset, and byte mask of the pattern embedded in the remote wakeup packet, and the filter-operation commands are programmed.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	<p>RWK Packet Filter (WKUPFRMFTR):</p> <p>This field contains the various controls of RWK Packet filter.</p>

11.2.30 MAC_LPI_CONTROL_STATUS — Offset D0h

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21	0h RW	<p>LPI Tx Clock Stop Enable (LPITCSE):</p> <p>When this bit is set, the MAC indicates that the Tx clock to MAC can be stopped.</p> <p>When this bit is reset, the MAC does not indicate that the Tx clock to MAC can be stopped after it enters Tx LPI mode.</p> <p>If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		programmed. 0x0 (DISABLE): LPI Tx Clock Stop is disabled. 0x1 (ENABLE): LPI Tx Clock Stop is enabled.
20	0h RW	LPI Timer Enable (LPIATE): This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. 0x0 (DISABLE): LPI Timer is disabled. 0x1 (ENABLE): LPI Timer is enabled.
19	0h RW	LPI Tx Automate (LPITXA): This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. 0x0 (DISABLE): LPI Tx Automate is disabled. 0x1 (ENABLE): LPI Tx Automate is enabled.
18	0h RW	PHY Link Status Enable (PLSEN): This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. 0x0 (DISABLE): PHY Link Status is disabled. 0x1 (ENABLE): PHY Link Status is enabled.
17	0h RW	PHY Link Status (PLS): This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. 0x0 (DISABLE): link is down. 0x1 (ENABLE): link is okay (UP).
16	0h RW	LPI Enable (LPIEN): When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. 0x0 (DISABLE): LPI state is disabled. 0x1 (ENABLE): LPI state is enabled.
15:10	0h RO	Reserved
9	0h RO/V	Receive LPI State (RLPIST):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.</p> <p>0x0 (INACTIVE): Receive LPI state not detected. 0x1 (ACTIVE): Receive LPI state detected.</p>
8	0h RO/V	<p>Transmit LPI State (TLPIST):</p> <p>When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.</p> <p>0x0 (INACTIVE): Transmit LPI state not detected. 0x1 (ACTIVE): Transmit LPI state detected.</p>
7:4	0h RO	Reserved
3	0h RO/V	<p>Receive LPI Exit (RLPIEX):</p> <p>When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).</p> <p>Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.</p> <p>0x0 (INACTIVE): Receive LPI exit not detected. 0x1 (ACTIVE): Receive LPI exit detected.</p>
2	0h RO/V	<p>Receive LPI Entry (RLPIEN):</p> <p>When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).</p> <p>Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.</p> <p>0x0 (INACTIVE): Receive LPI entry not detected. 0x1 (ACTIVE): Receive LPI entry detected.</p>
1	0h RO/V	<p>Transmit LPI Exit (TLPIEX):</p> <p>When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).</p> <p>0x0 (INACTIVE): Transmit LPI exit not detected. 0x1 (ACTIVE): Transmit LPI exit detected.</p>
0	0h RO/V	<p>Transmit LPI Entry (TLPIEN):</p> <p>When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).</p> <p>0x0 (INACTIVE): Transmit LPI entry not detected. 0x1 (ACTIVE): Transmit LPI entry detected.</p>

11.2.31 MAC_LPI_TIMERS_CONTROL – Offset D4h

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	03E80000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved
25:16	3E8h RW	<p>LPI LS Timer (LST): This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.</p>
15:0	0000h RW	<p>LPI TW Timer (TWT): This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.</p>

11.2.32 MAC_LPI_ENTRY_TIMER — Offset D8h

This register controls the Tx LPI entry timer. This counter is enabled only when bit[20] (LPITE) bit of MAC_LPI_Control_Status is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:3	00000h RW	<p>LPI Entry Timer (LPITE): This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPTX are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.</p>
2:0	0h RO	Reserved

11.2.33 MAC_1US_TIC_COUNTER — Offset DCh

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000063h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	063h RW	<p>1US TIC Counter (TIC_1US_CNTR): The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63).</p>

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Bit Range	Default & Access	Field Name (ID): Description
		This is required to generate the 1US events that are used to update some of the EEE related counters.

11.2.34 MAC_PHYIF_CONTROL_STATUS — Offset F8h

The PHY Interface Control and Status register indicates the status signals received by the SGMII or RGMII interface (selected at reset) from the PHY. This register is optional.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19	0h RO/V	Link Status (LNKSTS): This bit indicates whether the link is up (1'b1) or down (1'b0). 0x0 (INACTIVE): Link down. 0x1 (ACTIVE): Link up.
18:17	0h RO/V	Link Speed (LNKSPEED): This bit indicates the current speed of the link. 0x0 (M_2500K): 2.5 MHz. 0x1 (M_25M): 25 MHz. 0x2 (M_125M): 125 MHz. 0x3 (RSVD): Reserved.
16	0h RO/V	Link Mode (LNKMOD): This bit indicates the current mode of operation of the link. 0x0 (HDUPLEX): Half-duplex mode. 0x1 (FDUPLEX): Full-duplex mode.
15:2	0h RO	Reserved
1	0h RW	Link Up or Down (LUD): This bit indicates whether the link is up or down during transmission of configuration in the RGMII or SGMII interface. 0x0 (LINKDOWN): Link down. 0x1 (LINKUP): Link up.
0	0h RW	Transmit Configuration in RGMII or SGMII (TC): When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: - "Reduced Gigabit Media Independent Interface" - "Serial Media Independent Interface" - "Serial Gigabit Media Independent Interface" 0x0 (DISABLE): Disable Transmit Configuration in RGMII or SGMII. 0x1 (ENABLE): Enable Transmit Configuration in RGMII or SGMII.

11.2.35 MAC_VERSION — Offset 110h

The version register identifies the version of the Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	00005151h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:8	51h RO/V	USERVER: Version code
7:0	51h RO/V	SNPSVER: Version code

11.2.36 MAC_DEBUG — Offset 114h

The Debug register provides the debug status of various MAC blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved
18:17	0h RO/V	MAC Transmit Packet Controller Status (TFCSTS): This field indicates the state of the MAC Transmit Packet Controller module. 0x0 (IDLE): Idle state. 0x1 (WAITING): Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over. 0x2 (GEN_TX_PAU): Generating and transmitting a Pause control packet (in full-duplex mode). 0x3 (TRNSFR): Transferring input packet for transmission.
16	0h RO/V	MAC GMII or MII Transmit Protocol Engine Status (TPESTS): When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Transmit Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Transmit Protocol Engine Status detected.
15:3	0h RO	Reserved
2:1	0h RO/V	MAC Receive Packet Controller FIFO Status (RFCFCSTS): When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	0h RO/V	MAC GMII or MII Receive Protocol Engine Status (RPESTS): When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected.

11.2.37 MAC_HW_FEATURE0 — Offset 11Ch

This register indicates the presence of first set of the optional features or functions of the Ethernet Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	0EFD73F7h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:28	0h RO/V	Active PHY Selected (ACTPHYSEL): When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. 0x0 (GMII_MII): GMII or MII. 0x1 (RGMII): RGMII. 0x2 (SGMII): SGMII. 0x3 (TBI): TBI. 0x4 (RMII): RMII. 0x5 (RTBI): RTBI. 0x6 (SMII): SMII. 0x7 (REVMII): RevMII.
27	1h RO/V	Source Address or VLAN Insertion Enable (SAVLANINS): This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected 0x0 (INACTIVE): Source Address or VLAN Insertion Enable option is not selected. 0x1 (ACTIVE): Source Address or VLAN Insertion Enable option is selected.
26:25	3h RO/V	Timestamp System Time Source (TSSTSSEL): This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INTRNL): Internal. 0x1 (EXTRNL): External. 0x2 (BOTH): Both. 0x3 (RSVD): Reserved.
24	0h RO/V	MAC Addresses 64-127 Selected (MACADR64SEL): This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected 0x0 (INACTIVE): MAC Addresses 64-127 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 64-127 Select option is selected.
23	1h RO/V	MAC Addresses 32-63 Selected (MACADR32SEL): This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected 0x0 (INACTIVE): MAC Addresses 32-63 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 32-63 Select option is selected.
22:18	1Fh RO/V	MAC Addresses 1-31 Selected (ADDMACADRSEL): This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option
17	0h RO	Reserved
16	1h RO/V	Receive Checksum Offload Enabled (RXCOESEL): This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected 0x0 (INACTIVE): Receive Checksum Offload Enable option is not selected.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): Receive Checksum Offload Enable option is selected.
15	0h RO	Reserved
14	1h RO/V	Transmit Checksum Offload Enabled (TXCOESEL): This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected 0x0 (INACTIVE): Transmit Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Transmit Checksum Offload Enable option is selected.
13	1h RO/V	Energy Efficient Ethernet Enabled (EEESEL): This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected 0x0 (INACTIVE): Energy Efficient Ethernet Enable option is not selected. 0x1 (ACTIVE): Energy Efficient Ethernet Enable option is selected.
12	1h RO/V	IEEE 1588-2008 Timestamp Enabled (TSSEL): This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INACTIVE): IEEE 1588-2008 Timestamp Enable option is not selected. 0x1 (ACTIVE): IEEE 1588-2008 Timestamp Enable option is selected.
11:10	0h RO	Reserved
9	1h RO/V	ARP Offload Enabled (ARPOFFSEL): This bit is set to 1 when the Enable IPv4 ARP Offload option is selected 0x0 (INACTIVE): ARP Offload Enable option is not selected. 0x1 (ACTIVE): ARP Offload Enable option is selected.
8	1h RO/V	RMON Module Enable (MMCSEL): This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected 0x0 (INACTIVE): RMON Module Enable option is not selected. 0x1 (ACTIVE): RMON Module Enable option is selected.
7	1h RO/V	PMT Magic Packet Enable (MGKSEL): This bit is set to 1 when the Enable Magic Packet Detection option is selected 0x0 (INACTIVE): PMT Magic Packet Enable option is not selected. 0x1 (ACTIVE): PMT Magic Packet Enable option is selected.
6	1h RO/V	PMT Remote Wake-up Packet Enable (RWKSEL): This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected 0x0 (INACTIVE): PMT Remote Wake-up Packet Enable option is not selected. 0x1 (ACTIVE): PMT Remote Wake-up Packet Enable option is selected.
5	1h RO/V	SMA (MDIO) Interface (SMASEL): This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected 0x0 (INACTIVE): SMA (MDIO) Interface not selected. 0x1 (ACTIVE): SMA (MDIO) Interface selected.
4	1h RO/V	VLAN Hash Filter Selected (VLHASH): This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected 0x0 (INACTIVE): VLAN Hash Filter not selected. 0x1 (ACTIVE): VLAN Hash Filter selected.
3	0h RO/V	PCS Registers (TBI, SGMII, or RTBI PHY interface) (PCSSEL): This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected 0x0 (INACTIVE): No PCS Registers (TBI, SGMII, or RTBI PHY interface). 0x1 (ACTIVE): PCS Registers (TBI, SGMII, or RTBI PHY interface).
2	1h RO/V	Half-duplex Support (HDSEL): This bit is set to 1 when the half-duplex mode is selected

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (INACTIVE): No Half-duplex support. 0x1 (ACTIVE): Half-duplex support.
1	1h RO/V	1000 Mbps Support (GMIISSEL): This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 1000 Mbps support. 0x1 (ACTIVE): 1000 Mbps support.
0	1h RO/V	10 or 100 Mbps Support (MIISSEL): This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 10 or 100 Mbps support. 0x1 (ACTIVE): 10 or 100 Mbps support.

11.2.38 MAC_HW_FEATURE1 — Offset 120h

This register indicates the presence of second set of the optional features or functions of the Ethernet Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	119F79C8h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:27	2h RO/V	Total number of L3 or L4 Filters (L3L4FNUM): This field indicates the total number of L3 or L4 filters: 0x0 (NOFILT): No L3 or L4 Filter. 0x1 (M_1FILT): 1 L3 or L4 Filter. 0x2 (M_2FILT): 2 L3 or L4 Filters. 0x3 (M_3FILT): 3 L3 or L4 Filters. 0x4 (M_4FILT): 4 L3 or L4 Filters. 0x5 (M_5FILT): 5 L3 or L4 Filters. 0x6 (M_6FILT): 6 L3 or L4 Filters. 0x7 (M_7FILT): 7 L3 or L4 Filters. 0x8 (M_8FILT): 8 L3 or L4 Filters.
26	0h RO	Reserved
25:24	1h RO/V	Hash Table Size (HASHTBLSZ): This field indicates the size of the hash table: 0x0 (NO_HT): No hash table. 0x1 (M_64): 64. 0x2 (M_128): 128. 0x3 (M_256): 256.
23	1h RO/V	One Step for PTP over UDP/IP Feature Enable (POUOST): This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. 0x0 (INACTIVE): One Step for PTP over UDP/IP Feature is not selected. 0x1 (ACTIVE): One Step for PTP over UDP/IP Feature is selected.
22	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
21	0h RO/V	Rx Side Only AV Feature Enable (RAVSEL): This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. 0x0 (INACTIVE): Rx Side Only AV Feature is not selected. 0x1 (ACTIVE): Rx Side Only AV Feature is selected.
20	1h RO/V	AV Feature Enable (AVSEL): This bit is set to 1 when the Enable Audio Video Bridging option is selected. 0x0 (INACTIVE): AV Feature is not selected. 0x1 (ACTIVE): AV Feature is selected.
19	1h RO/V	DMA Debug Registers Enable (DBGMEMA): This bit is set to 1 when the Debug Mode Enable option is selected 0x0 (INACTIVE): DMA Debug Registers option is not selected. 0x1 (ACTIVE): DMA Debug Registers option is selected.
18	1h RO/V	TCP Segmentation Offload Enable (TSOEN): This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected 0x0 (INACTIVE): TCP Segmentation Offload Feature is not selected. 0x1 (ACTIVE): TCP Segmentation Offload Feature is selected.
17	1h RO/V	Split Header Feature Enable (SPHEN): This bit is set to 1 when the Enable Split Header Structure option is selected 0x0 (INACTIVE): Split Header Feature is not selected. 0x1 (ACTIVE): Split Header Feature is selected.
16	1h RO/V	DCB Feature Enable (DCBEN): This bit is set to 1 when the Enable Data Center Bridging option is selected 0x0 (INACTIVE): DCB Feature is not selected. 0x1 (ACTIVE): DCB Feature is selected.
15:14	1h RO/V	Address Width. (ADDR64): This field indicates the configured address width: 0x0 (M_32): 32. 0x1 (M_40): 40. 0x2 (M_48): 48. 0x3 (RSVD): Reserved.
13	1h RO/V	IEEE 1588 High Word Register Enable (ADVTHWORD): This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected 0x0 (INACTIVE): IEEE 1588 High Word Register option is not selected. 0x1 (ACTIVE): IEEE 1588 High Word Register option is selected.
12	1h RO/V	PTP Offload Enable (PTOEN): This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. 0x0 (INACTIVE): PTP Offload feature is not selected. 0x1 (ACTIVE): PTP Offload feature is selected.
11	1h RO/V	One-Step Timestamping Enable (OSTEN): This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. 0x0 (INACTIVE): One-Step Timestamping feature is not selected. 0x1 (ACTIVE): One-Step Timestamping feature is selected.
10:6	07h RO/V	MTL Transmit FIFO Size (TXFIFOSIZE): This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, $\text{Log}_2(\text{TXFIFO_SIZE}) - 7$: 0x0 (M_128B): 128 bytes.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x8 (M_32KB): 32 KB. 0x9 (M_64KB): 64 KB. 0xA (M_128KB): 128 KB. 0xB (RSVD): Reserved.
5	0h RO/V	Single Port RAM Enable (SPRAM): This bit is set to 1 when the Use single port RAM Feature is selected. 0x0 (INACTIVE): Single Port RAM feature is not selected. 0x1 (ACTIVE): Single Port RAM feature is selected.
4:0	08h RO/V	MTL Receive FIFO Size (RXFIFOSIZE): This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x8 (M_32KB): 32 KB. 0x9 (M_64KB): 64 KB. 0xA (M_128KB): 128 KB. 0xB (M_256KB): 256 KB. 0xC (RSVD): Reserved.

11.2.39 MAC_HW_FEATURE2 — Offset 124h

This register indicates the presence of third set of the optional features or functions of the Ethernet Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	220C50C5h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:28	2h RO/V	Number of Auxiliary Snapshot Inputs (AUXSNAPNUM): This field indicates the number of auxiliary snapshot inputs: 0x0 (NO_AUXI): No auxiliary input. 0x1 (M_1_AUXI): 1 auxiliary input. 0x2 (M_2_AUXI): 2 auxiliary input. 0x3 (M_3_AUXI): 3 auxiliary input.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x4 (M_4_AUXI): 4 auxiliary input. 0x5 (RSVD): Reserved.
27	0h RO	Reserved
26:24	2h RO/V	Number of PPS Outputs (PPSOUTNUM): This field indicates the number of PPS outputs: 0x0 (NO_PPSO): No PPS output. 0x1 (M_1_PPSO): 1 PPS output. 0x2 (M_2_PPSO): 2 PPS output. 0x3 (M_3_PPSO): 3 PPS output. 0x4 (M_4_PPSO): 4 PPS output. 0x5 (RSVD): Reserved.
23:22	0h RO	Tx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (TDCSZ): 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
21:18	3h RO/V	Number of DMA Transmit Channels (TXCHCNT): This field indicates the number of DMA Transmit channels: 0x0 (M_1TXCH): 1 MTL Tx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1TDCSZ): 4. 0x1 (M_2TXCH): 2 MTL Tx Channels. 0x2 (M_2TDCSZ): 8. 0x2 (M_3TXCH): 3 MTL Tx Channels. 0x3 (M_3TDCSZ): 16. 0x3 (M_4TXCH): 4 MTL Tx Channels. 0x4 (M_5TXCH): 5 MTL Tx Channels. 0x5 (M_6TXCH): 6 MTL Tx Channels. 0x6 (M_7TXCH): 7 MTL Tx Channels. 0x7 (M_8TXCH): 8 MTL Tx Channels.
17:16	0h RO	Rx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (RDCSZ): 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
15:12	5h RO/V	Number of DMA Receive Channels (RXCHCNT): This field indicates the number of DMA Receive channels: 0x0 (M_1RXCH): 1 MTL Rx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1RDCSZ): 4. 0x1 (M_2RXCH): 2 MTL Rx Channels. 0x2 (M_2RDCSZ): 8. 0x2 (M_3RXCH): 3 MTL Rx Channels. 0x3 (M_3RDCSZ): 16. 0x3 (M_4RXCH): 4 MTL Rx Channels. 0x4 (M_5RXCH): 5 MTL Rx Channels. 0x5 (M_6RXCH): 6 MTL Rx Channels. 0x6 (M_7RXCH): 7 MTL Rx Channels. 0x7 (M_8RXCH): 8 MTL Rx Channels.

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Bit Range	Default & Access	Field Name (ID): Description
11:10	0h RO	Reserved
9:6	3h RO/V	Number of MTL Transmit Queues (TXQCNT): This field indicates the number of MTL Transmit queues: 0x0 (M_1TXQ): 1 MTL Tx Queue. 0x1 (M_2TXQ): 2 MTL Tx Queues. 0x2 (M_3TXQ): 3 MTL Tx Queues. 0x3 (M_4TXQ): 4 MTL Tx Queues, 0x4 (M_5TXQ): 5 MTL Tx Queues. 0x5 (M_6TXQ): 6 MTL Tx Queues. 0x6 (M_7TXQ): 7 MTL Tx Queues. 0x7 (M_8TXQ): 8 MTL Tx Queues.
5:4	0h RO	Reserved
3:0	5h RO/V	Number of MTL Receive Queues (RXQCNT): This field indicates the number of MTL Receive queues: 0x0 (M_1RXQ): 1 MTL Rx Queue. 0x1 (M_2RXQ): 2 MTL Rx Queues. 0x2 (M_3RXQ): 3 MTL Rx Queues. 0x3 (M_4RXQ): 4 MTL Rx Queues. 0x4 (M_5RXQ): 5 MTL Rx Queues. 0x5 (M_6RXQ): 6 MTL Rx Queues. 0x6 (M_7RXQ): 7 MTL Rx Queues. 0x7 (M_8RXQ): 8 MTL Rx Queues.

11.2.40 MAC_HW_FEATURE3 — Offset 128h

This register indicates the presence of fourth set of optional features or functions of the Ethernet Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	3C390232h
Bit Range	Default & Access	Field Name (ID): Description	
31:30	0h RO	Reserved	
29:28	3h RO/V	Automotive Safety Package (ASP): Following are the encoding for the different Safety features 0x0 (NONE): No Safety features selected. 0x1 (ECC_ONLY): Only "ECC protection for external memory" feature is selected. 0x2 (AS_NPPE): All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature. 0x3 (AS_PPE): All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature.	
27	1h RO/V	Time Based Scheduling Enable (TBSSEL): This bit is set to 1 when the Time Based Scheduling feature is selected. 0x0 (INACTIVE): Time Based Scheduling Enable feature is not selected. 0x1 (ACTIVE): Time Based Scheduling Enable feature is selected.	

continued...

Bit Range	Default & Access	Field Name (ID): Description
26	1h RO/V	Frame Preemption Enable (FPESEL): This bit is set to 1 when the Enable Frame preemption feature is selected. 0x0 (INACTIVE): Frame Preemption Enable feature is not selected. 0x1 (ACTIVE): Frame Preemption Enable feature is selected.
25:22	0h RO	Reserved
21:20	3h RO/V	Width of the Time Interval field in the Gate Control List (ESTWID): This field indicates the width of the Configured Time Interval Field 0x0 (NOWIDTH): Width not configured. 0x1 (WIDTH16): 16. 0x2 (WIDTH20): 20. 0x3 (WIDTH24): 24.
19:17	4h RO/V	Depth of the Gate Control List (ESTDEP): This field indicates the depth of Gate Control list expressed as Log2(512)-5 0x0 (NODEPTH): No Depth configured. 0x1 (DEPTH64): 64. 0x2 (DEPTH128): 128. 0x3 (DEPTH256): 256. 0x4 (DEPTH512): 512. 0x5 (DEPTH1024): 1024. 0x6 (RSVD): Reserved.
16	1h RO/V	Enhancements to Scheduling Traffic Enable (ESTSEL): This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. 0x0 (INACTIVE): Enable Enhancements to Scheduling Traffic feature is not selected. 0x1 (ACTIVE): Enable Enhancements to Scheduling Traffic feature is selected.
15	0h RO	Reserved
14:13	0h RO/V	Flexible Receive Parser Table Entries size (FRPES): This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. 0x0 (M_64ENTR): 64 Entries. 0x1 (M_128ENTR): 128 Entries. 0x2 (M_256ENTR): 256 Entries. 0x3 (RSVD): Reserved.
12:11	0h RO/V	Flexible Receive Parser Buffer size (FRPBS): This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. 0x0 (M_64BYTES): 64 Bytes. 0x1 (M_128BYTES): 128 Bytes. 0x2 (M_256BYTES): 256 Bytes. 0x3 (RSVD): Reserved.
10	0h RO/V	Flexible Receive Parser Selected (FRPSEL): This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. 0x0 (INACTIVE): Flexible Receive Parser feature is not selected. 0x1 (ACTIVE): Flexible Receive Parser feature is selected.
9	1h RO/V	Broadcast/Multicast Packet Duplication (PDUPSEL): This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. 0x0 (INACTIVE): Broadcast/Multicast Packet Duplication feature is not selected. 0x1 (ACTIVE): Broadcast/Multicast Packet Duplication feature is selected.
8:6	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
5	1h RO/V	Double VLAN Tag Processing Selected (DVLAN): This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. 0x0 (INACTIVE): Double VLAN option is not selected. 0x1 (ACTIVE): Double VLAN option is selected.
4	1h RO/V	Queue/Channel based VLAN tag insertion on Tx Enable (CBTISEL): This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. 0x0 (INACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected. 0x1 (ACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is selected.
3	0h RO	Reserved
2:0	2h RO/V	Number of Extended VLAN Tag Filters Enabled (NRVF): This field indicates the Number of Extended VLAN Tag Filters selected: 0x0 (NO_ERVLAN): No Extended Rx VLAN Filters. 0x1 (M_4_ERVLAN): 4 Extended Rx VLAN Filters. 0x2 (M_8_ERVLAN): 8 Extended Rx VLAN Filters. 0x3 (M_16_ERVLAN): 16 Extended Rx VLAN Filters. 0x4 (M_24_ERVLAN): 24 Extended Rx VLAN Filters. 0x5 (M_32_ERVLAN): 32 Extended Rx VLAN Filters. 0x6 (RSVD): Reserved.

11.2.41 MAC_DPP_FSM_INTERRUPT_STATUS — Offset 140h

This register contains the status of Automotive Safety related Data Path Parity Errors, Interface Timeout Errors, FSM State Parity Errors and FSM State Timeout Errors. All the non-Reserved bits are cleared on read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:25	0h RO	Reserved	
24	0h RW	FSM State Parity Error Status (FSMPES): This field when set indicates one of the FSMs State registers has a parity error detected. 0x0 (INACTIVE): FSM State Parity Error Status not detected. 0x1 (ACTIVE): FSM State Parity Error Status detected.	
23:18	0h RO	Reserved	
17	0h RW	Agent Read/Write Timeout Error Status (SLVTES): This field when set indicates that an Application/CSR Timeout has occurred on the AXI agent interface. 0x0 (INACTIVE): Agent Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Agent Read/Write Timeout Error Status detected.	
16	0h RW	Host Read/Write Timeout Error Status (MSTTES):	

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field when set indicates that an Application/CSR Timeout has occurred on the host (AXI/AHB/ARI/ATI) interface. 0x0 (INACTIVE): Host Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Host Read/Write Timeout Error Status detected.
15:13	0h RO	Reserved
12	0h RW	PTP FSM Timeout Error Status (PTES): This field when set indicates that one of the PTP FSM Timeout has occurred. 0x0 (INACTIVE): PTP FSM Timeout Error Status not detected. 0x1 (ACTIVE): PTP FSM Timeout Error Status detected.
11	0h RW	APP FSM Timeout Error Status (ATES): This field when set indicates that one of the APP FSM Timeout has occurred. 0x0 (INACTIVE): APP FSM Timeout Error Status not detected. 0x1 (ACTIVE): APP FSM Timeout Error Status detected.
10	0h RW	CSR FSM Timeout Error Status (CTES): This field when set indicates that one of the CSR FSM Timeout has occurred. 0x0 (INACTIVE): CSR FSM Timeout Error Status not detected. 0x1 (ACTIVE): CSR FSM Timeout Error Status detected.
9	0h RW	Rx FSM Timeout Error Status (RTES): This field when set indicates that one of the Rx FSM Timeout has occurred. 0x0 (INACTIVE): Rx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Rx FSM Timeout Error Status detected.
8	0h RW	Tx FSM Timeout Error Status (TTES): This field when set indicates that one of the Tx FSM Timeout has occurred. 0x0 (INACTIVE): Tx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Tx FSM Timeout Error Status detected.
7	0h RW	AXI Agent Read data path Parity checker Error Status (ASRPES): This bit when set indicates that parity error is detected at the AXI Agent read data interface. 0x0 (INACTIVE): AXI Agent Read data path Parity checker Error Status not detected. 0x1 (ACTIVE): AXI Agent Read data path Parity checker Error Status detected.
6	0h RW	CSR Write data path Parity checker Error Status (CWPES): This bit when set indicates that parity error is detected at the CSR write data interface on mci_wdata_i (or at PC8 checker as shown in AXI agent Interface Data path parity protection diagram). When EPSI bit of MTL_DPP_Control register is set and if any parity mis-match is detected on the input agent parity ports (or at PC7 checker in the AXI agent Interface Data path parity protection diagram) sets this bit to one. 0x0 (INACTIVE): CSR Write data path Parity checker Error Status not detected. 0x1 (ACTIVE): CSR Write data path Parity checker Error Status detected.
5	0h RW	Application Receive interface data path Parity Error Status (ARPES): This bit when set indicates that a parity error is detected by the hardware internally at the interface with the application. 0x0 (INACTIVE): Application Receive interface data path Parity Error Status not detected. 0x1 (ACTIVE): Application Receive interface data path Parity Error Status detected.
4	0h RW	MTL TX Status data path Parity checker Error Status (MTSPES): This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL TX Status data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL TX Status data path Parity checker Error Status detected.

continued...

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	MTL data path Parity checker Error Status (MPES): This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL data path Parity checker Error Status detected.
2	0h RW	Read Descriptor Parity checker Error Status (RDPEs): This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): Read Descriptor Parity checker Error Status not detected. 0x1 (ACTIVE): Read Descriptor Parity checker Error Status detected.
1	0h RW	TSO data path Parity checker Error Status (TPES): This bit when set indicates that a parity error is detected at the DMA TSO parity checker (or at PC2 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): TSO data path Parity checker Error Status not detected. 0x1 (ACTIVE): TSO data path Parity checker Error Status detected.
0	0h RO	Reserved

11.2.42 MAC_AXI_SLV_DPE_ADDR_STATUS — Offset 144h

This register indicates the CSR address corresponding to the CSR write data on which parity error occurred.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved
13:0	0000h RO/V	AXI Agent data path Parity Error Address Status (ASPEAS): This field holds the CSR address for which parity error is detected on the CSR write data. This field holds the first address for which parity error is detected on the write data and is cleared on read.

11.2.43 MAC_FSM_CONTROL — Offset 148h

This register is used to control the FSM State parity and timeout error injection in Debug mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RW	PTP Large/Normal Mode Select (PLGRNML): This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): normal mode tic generation is used for PTP domain. 0x1 (ENABLE): large mode tic generation is used for PTP domain.
27	0h RW	APP Large/Normal Mode Select (ALGRNML): This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for APP domain. 0x1 (ENABLE): large mode tic generation is used for APP domain.
26	0h RW	CSR Large/Normal Mode Select (CLGRNML): This field when set indicates that large mode tic generation is used for CSR domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for CSR domain. 0x1 (ENABLE): large mode tic generation is used for CSR domain.
25	0h RW	Rx Large/Normal Mode Select (RLGRNML): This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Rx domain. 0x1 (ENABLE): large mode tic generation is used for Rx domain.
24	0h RW	Tx Large/Normal Mode Select (TLGRNML): This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Tx domain. 0x1 (ENABLE): large mode tic generation is used for Tx domain.
23:21	0h RO	Reserved
20	0h RW	PTP FSM Parity Error Injection (PPEIN): This field when set indicates that Error Injection for PTP FSM Parity is enabled. 0x0 (DISABLE): PTP FSM Parity Error Injection is disabled. 0x1 (ENABLE): PTP FSM Parity Error Injection is enabled.
19	0h RW	APP FSM Parity Error Injection (APEIN): This field when set indicates that Error Injection for APP FSM Parity is enabled. 0x0 (DISABLE): APP FSM Parity Error Injection is disabled. 0x1 (ENABLE): APP FSM Parity Error Injection is enabled.
18	0h RW	CSR FSM Parity Error Injection (CPEIN): This field when set indicates that Error Injection for CSR Parity is enabled. 0x0 (DISABLE): CSR FSM Parity Error Injection is disabled. 0x1 (ENABLE): CSR FSM Parity Error Injection is enabled.
17	0h RW	Rx FSM Parity Error Injection (RPEIN): This field when set indicates that Error Injection for RX FSM Parity is enabled. 0x0 (DISABLE): Rx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Rx FSM Parity Error Injection is enabled.
16	0h RW	Tx FSM Parity Error Injection (TPEIN): This field when set indicates that Error Injection for TX FSM Parity is enabled. 0x0 (DISABLE): Tx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Tx FSM Parity Error Injection is enabled.
15:13	0h RO	Reserved
12	0h RW	PTP FSM Timeout Error Injection (PTEIN): This field when set indicates that Error Injection for PTP FSM timeout is enabled.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): PTP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): PTP FSM Timeout Error Injection is enabled.
11	0h RW	APP FSM Timeout Error Injection (ATEIN): This field when set indicates that Error Injection for APP FSM timeout is enabled. 0x0 (DISABLE): APP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): APP FSM Timeout Error Injection is enabled.
10	0h RW	CSR FSM Timeout Error Injection (CTEIN): This field when set indicates that Error Injection for CSR timeout is enabled. 0x0 (DISABLE): CSR FSM Timeout Error Injection is disabled. 0x1 (ENABLE): CSR FSM Timeout Error Injection is enabled
9	0h RW	Rx FSM Timeout Error Injection (RTEIN): This field when set indicates that Error Injection for RX FSM timeout is enabled. 0x0 (DISABLE): Rx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Rx FSM Timeout Error Injection is enabled.
8	0h RW	Tx FSM Timeout Error Injection (TTEIN): This field when set indicates that Error Injection for TX FSM timeout is enabled. 0x0 (DISABLE): Tx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Tx FSM Timeout Error Injection is enabled.
7:2	0h RO	Reserved
1	0h RW	PRTYEN: This bit when set indicates that the FSM parity feature is enabled. 0x0 (DISABLE): FSM Parity feature is disabled. 0x1 (ENABLE): FSM Parity feature is enabled.
0	0h RW	TMOUTEN: This bit when set indicates that the FSM timeout feature is enabled. 0x0 (DISABLE): FSM timeout feature is disabled. 0x1 (ENABLE): FSM timeout feature is enabled.

11.2.44 MAC_FSM_ACT_TIMER — Offset 14Ch

This register is used to select the FSM and Interface Timeout values.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14Ch	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:24	0h RO	Reserved	
23:20	0h RW	LTMRMD: This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4ILLI_SEC): 1.024ms (~4ms). 0x3 (M_16ILLI_SEC): 16.384ms (~16ms). 0x4 (M_64ILLI_SEC): 65.536ms (~64ms).	

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Bit Range	Default & Access	Field Name (ID): Description
		0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
19:16	0h RW	NTMRMD: This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
15:10	0h RO	Reserved
9:0	000h RW	TMR: This field indicates the number of CSR clocks required to generate 1us tic.

11.2.45 SNPS_SCS_REG1 – Offset 150h

Reserved

Type	Size	Offset	Default
MMIO	32 bit	BAR + 150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	MAC_SCS1 DWC_ETHER_QOS (MAC_SCS1): Synopsys Reserved, All the bits must be set to "0". This field is reserved for Synopsys Internal use, and must always be set to "0" unless instructed by Synopsys. Setting any bit to "1" might cause unexpected behavior in the IP.

11.2.46 MAC_MDIO_ADDRESS – Offset 200h

The MDIO Address register controls the management cycles to external PHY through a management interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RW	<p>Preamble Suppression Enable (PSE): When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. 0x0 (DISABLE): Preamble Suppression disabled. 0x1 (ENABLE): Preamble Suppression enabled.</p>
26	0h RW	<p>Back to Back transactions (BTB): When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. 0x0 (DISABLE): Back to Back transactions disabled. 0x1 (ENABLE): Back to Back transactions enabled.</p>
25:21	00h RW	<p>Physical Layer Address (PA): This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.</p>
20:16	00h RW	<p>Register/Device Address (RDA): These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.</p>
15	0h RO	Reserved
14:12	0h RW	<p>Number of Trailing Clocks (NTC): This field controls the number of trailing clock cycles generated on the MDIO Clock (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.</p>
11:8	0h RW	<p>CSR Clock Range (CR): The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design:</p> <ul style="list-style-type: none"> - 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 - 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 - 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 - 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 - 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 - 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 - 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 - 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 <p>The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range.</p> <p>When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks:</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - 1000: CSR clock/4 - 1001: CSR clock/6 - 1010: CSR clock/8 - 1011: CSR clock/10 - 1100: CSR clock/12 - 1101: CSR clock/14 - 1110: CSR clock/16 - 1111: CSR clock/18
7:5	0h RO	Reserved
4	0h RW	<p>Skip Address Packet (SKAP): When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0x0 (DISABLE): Skip Address Packet is disabled. 0x1 (ENABLE): Skip Address Packet is enabled.</p>
3	0h RW	<p>GMII Operation Command 1 (GOC_1): This bit is higher bit of the operation command to the PHY or GOC_1 and GOC_0 are encoded as follows: - 00: Reserved - 01: Write - 10: Post Read Increment Address for Clause 45 PHY - 11: Read When Clause 22 PHY is enabled, only Write and Read commands are valid. 0x0 (DISABLE): GMII Operation Command 1 is disabled. 0x1 (ENABLE): GMII Operation Command 1 is enabled.</p>
2	0h RW	<p>GMII Operation Command 0 (GOC_0): This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO host) this bit along with GOC_1 determines the operation to be performed to the PHY. 0x0 (DISABLE): GMII Operation Command 0 is disabled. 0x1 (ENABLE): GMII Operation Command 0 is enabled.</p>
1	0h RW	<p>Clause 45 PHY Enable (C45E): When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0x0 (DISABLE): Clause 45 PHY is disabled. 0x1 (ENABLE): Clause 45 PHY is enabled.</p>
0	0h RW	<p>GMII Busy (GB): The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO agent. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDI field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): GMII Busy is disabled. 0x1 (ENABLE): GMII Busy is enabled.</p>

11.2.47 MAC_MDIO_DATA — Offset 204h

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	Register Address (RA): This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	0000h RW	GMII Data (GD): This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

11.2.48 MAC_GPIO_CONTROL — Offset 208h

The GPIO Control register controls the GPIO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved

11.2.49 MAC_GPIO_STATUS — Offset 20Ch

The General Purpose IO register provides the control to drive the following: up to 16 bits of output ports (GPO) and status of up to 16 input ports (GPIS).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17	0h RW	Trigger Snapshot (GPO1): Active-high signal. The rising edge of this signal triggers snapshot of current PMC ART and System timer values. The system timer value is stored into AUX FIFO. An interrupt is generated upon snapshotting. The PMC ART timer values is stored in 4x 16-bit ART snapshot register and is read through MDIO registers.
16	0h RW	P2P Clock Selector (GPO0): Used for selecting the P2P clock

continued...

Bit Range	Default & Access	Field Name (ID): Description
		1 -> 19.2MHz Local Clock Always Running Timer (ART) 0 -> 204.8MHz application clock
15:0	0h RO	Reserved

11.2.50 MAC_ARP_ADDRESS – Offset 210h

The ARP Address register contains the IPv4 Destination Address of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	ARP Protocol Address (ARPPA): This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

11.2.51 MAC_CSR_SW_CTRL – Offset 230h

This register contains SW programmable controls for changing the CSR access response and status bits clearing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RW	Agent Error Response Enable (SEEN): When this bit is set, the MAC responds with Agent Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space. 0x0 (DISABLE): Agent Error Response is disabled. 0x1 (ENABLE): Agent Error Response is enabled.
7:1	0h RO	Reserved
0	0h RW	Register Clear on Write 1 Enable (RCWE): When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. 0x0 (DISABLE): Register Clear on Write 1 is disabled. 0x1 (ENABLE): Register Clear on Write 1 is enabled.

11.2.52 MAC_FPE_CTRL_STS – Offset 234h

This register controls the operation of Frame Preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19	0h RW	<p>Transmitted Respond Frame (TRSP): Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Respond Frame. 0x1 (ACTIVE): transmitted Respond Frame.</p>
18	0h RW	<p>Transmitted Verify Frame (TVER): Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Verify Frame. 0x1 (ACTIVE): transmitted Verify Frame.</p>
17	0h RW	<p>Received Respond Frame (RRSP): Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Respond Frame. 0x1 (ACTIVE): Received Respond Frame.</p>
16	0h RW	<p>Received Verify Frame (RVER): Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Verify Frame. 0x1 (ACTIVE): Received Verify Frame.</p>
15:4	0h RO	Reserved
3	0h RW	Reserved
2	0h RW	<p>Send Respond mPacket (SRSP): When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Respond mPacket is disabled. 0x1 (ENABLE): Send Respond mPacket is enabled.</p>
1	0h RW	<p>Send Verify mPacket (SVER): When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Verify mPacket is disabled. 0x1 (ENABLE): Send Verify mPacket is enabled.</p>
0	0h	Enable Tx Frame Preemption (EFPE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When set Frame Preemption Tx functionality is enabled. 0x0 (DISABLE): Tx Frame Preemption is disabled. 0x1 (ENABLE): Tx Frame Preemption is enabled.

11.2.53 MAC_EXT_CFG1 — Offset 238h

This register contains Split mode control field and offset field for Split Header feature.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000002h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:8	0h RW	Split Mode (SPLM): These bits indicate the mode of splitting the incoming Rx packets. They are 0x0 (L3L4): Split at L3/L4 header. 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame. 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped. 0x3 (RSVD): Reserved.
7	0h RO	Reserved
6:0	02h RW	Split Offset (SPLOFST): These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

11.2.54 MAC_PRESN_TIME_NS — Offset 240h

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns.

DWC_EQOS_FLEXI_PPS_OUT_EN=1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	MAC 1722 Presentation Time in ns (MPTN): These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns

11.2.55 MAC_PRESN_TIME_UPDT — Offset 244h

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_Control register).

DWC_EQOS_FLEXI_PPS_OUT_EN=1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RW	MAC 1722 Presentation Time Update (MPTU): This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction

11.2.56 MAC_ADDRESS0_HIGH — Offset 300h

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] of the MAC Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 300h	8000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO/V	Address Enable (AE): This bit is always set to 1. 0x0 (DISABLE): INVALID : This bit must be always set to 1. 0x1 (ENABLE): This bit is always set to 1.
30:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	FFFFh RW	MAC Address0[47:32] (ADDRHI): This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

11.2.57 MAC_ADDRESS0_LOW – Offset 304h

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 304h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address0[31:0] (ADDRLO): This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

11.2.58 MAC_ADDRESS1_HIGH – Offset 308h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 308h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h	Mask Byte Control (MBC):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	<p>These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:</p> <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	<p>DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.</p>
15:0	FFFFh RW	<p>MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.</p>

11.2.59 MAC_ADDRESS1_LOW — Offset 30Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	<p>MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.</p>

11.2.60 MAC_ADDRESS2_HIGH — Offset 310h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 310h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.61 MAC_ADDRESS2_LOW — Offset 314h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 314h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.62 MAC_ADDRESS3_HIGH — Offset 318h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 318h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.63 MAC_ADDRESS3_LOW – Offset 31Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 31Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.64 MAC_ADDRESS4_HIGH — Offset 320h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 320h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - ... - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.65 MAC_ADDRESS4_LOW — Offset 324h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 324h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.66 MAC_ADDRESS5_HIGH — Offset 328h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 328h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.67 MAC_ADDRESS5_LOW – Offset 32Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 32Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.68 MAC_ADDRESS6_HIGH – Offset 330h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 330h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.69 MAC_ADDRESS6_LOW — Offset 334h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 334h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.70 MAC_ADDRESS7_HIGH — Offset 338h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 338h	0000FFFFh
Bit Range	Default & Access	Field Name (ID): Description	
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.	
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.	
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.	
23:22	0h RO	Reserved	
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.	
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.	

11.2.71 MAC_ADDRESS7_LOW – Offset 33Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 33Ch	FFFFFFFh
Bit Range	Default & Access	Field Name (ID): Description	
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.	

11.2.72 MAC_ADDRESS8_HIGH — Offset 340h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 340h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.73 MAC_ADDRESS8_LOW — Offset 344h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 344h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.74 MAC_ADDRESS9_HIGH — Offset 348h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 348h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.75 MAC_ADDRESS9_LOW — Offset 34Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.76 MAC_ADDRESS10_HIGH — Offset 350h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 350h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:</p> <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	<p>DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.</p>
15:0	FFFFh RW	<p>MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.</p>

11.2.77 MAC_ADDRESS10_LOW – Offset 354h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 354h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	<p>MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.</p>

11.2.78 MAC_ADDRESS11_HIGH – Offset 358h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 358h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.79 MAC_ADDRESS11_LOW — Offset 35Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 35Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.80 MAC_ADDRESS12_HIGH — Offset 360h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 360h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.81 MAC_ADDRESS12_LOW – Offset 364h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 364h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.82 MAC_ADDRESS13_HIGH — Offset 368h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 368h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.83 MAC_ADDRESS13_LOW — Offset 36Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 36Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.84 MAC_ADDRESS14_HIGH — Offset 370h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 370h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.85 MAC_ADDRESS14_LOW – Offset 374h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 374h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.86 MAC_ADDRESS15_HIGH – Offset 378h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 378h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h	Address Enable (AE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.87 MAC_ADDRESS15_LOW – Offset 37Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 37Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.88 MAC_ADDRESS16_HIGH – Offset 380h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 380h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.89 MAC_ADDRESS16_LOW — Offset 384h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 384h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.90 MAC_ADDRESS17_HIGH — Offset 388h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 388h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - ... - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.91 MAC_ADDRESS17_LOW — Offset 38Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.92 MAC_ADDRESS18_HIGH — Offset 390h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 390h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.93 MAC_ADDRESS18_LOW – Offset 394h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 394h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.94 MAC_ADDRESS19_HIGH – Offset 398h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 398h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h	Address Enable (AE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.95 MAC_ADDRESS19_LOW — Offset 39Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 39Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.96 MAC_ADDRESS20_HIGH — Offset 3A0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.97 MAC_ADDRESS20_LOW – Offset 3A4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.98 MAC_ADDRESS21_HIGH — Offset 3A8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.99 MAC_ADDRESS21_LOW — Offset 3ACh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3ACh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.100 MAC_ADDRESS22_HIGH — Offset 3B0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.101 MAC_ADDRESS22_LOW – Offset 3B4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.102 MAC_ADDRESS23_HIGH – Offset 3B8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h	Address Enable (AE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.103 MAC_ADDRESS23_LOW – Offset 3BCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3BCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.104 MAC_ADDRESS24_HIGH – Offset 3C0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.105 MAC_ADDRESS24_LOW — Offset 3C4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.106 MAC_ADDRESS25_HIGH — Offset 3C8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - ... - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.107 MAC_ADDRESS25_LOW — Offset 3CCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3CCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.108 MAC_ADDRESS26_HIGH — Offset 3D0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.109 MAC_ADDRESS26_LOW – Offset 3D4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.110 MAC_ADDRESS27_HIGH – Offset 3D8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D8h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h	Address Enable (AE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.111 MAC_ADDRESS27_LOW — Offset 3DCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3DCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.112 MAC_ADDRESS28_HIGH — Offset 3E0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.113 MAC_ADDRESS28_LOW – Offset 3E4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.114 MAC_ADDRESS29_HIGH — Offset 3E8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.115 MAC_ADDRESS29_LOW — Offset 3ECh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3ECh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.116 MAC_ADDRESS30_HIGH — Offset 3F0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] <p>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.</p>
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.117 MAC_ADDRESS30_LOW – Offset 3F4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.118 MAC_ADDRESS31_HIGH – Offset 3F8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h	Address Enable (AE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	Source Address (SA): When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	Mask Byte Control (MBC): These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: <ul style="list-style-type: none"> - Bit 29: MAC_Address\${i}_High[15:8] - Bit 28: MAC_Address\${i}_High[7:0] - Bit 27: MAC_Address\${i}_Low[31:24] - .. - Bit 24: MAC_Address\${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	Reserved
21:16	00h RW	DMA Channel Select (DCS): If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	MAC Address1 [47:32] (ADDRHI): This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

11.2.119 MAC_ADDRESS31_LOW – Offset 3FCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3FCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address1 [31:0] (ADDRLO): This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

11.2.120 MAC_ADDRESS32_HIGH – Offset 400h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 400h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.121 MAC_ADDRESS32_LOW — Offset 404h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 404h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.122 MAC_ADDRESS33_HIGH — Offset 408h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 408h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.123 MAC_ADDRESS33_LOW — Offset 40Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.124 MAC_ADDRESS34_HIGH — Offset 410h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 410h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.125 MAC_ADDRESS34_LOW — Offset 414h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 414h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.126 MAC_ADDRESS35_HIGH — Offset 418h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 418h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.127 MAC_ADDRESS35_LOW – Offset 41Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 41Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.128 MAC_ADDRESS36_HIGH – Offset 420h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 420h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.129 MAC_ADDRESS36_LOW – Offset 424h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 424h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.130 MAC_ADDRESS37_HIGH — Offset 428h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 428h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.131 MAC_ADDRESS37_LOW — Offset 42Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 42Ch	FFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.132 MAC_ADDRESS38_HIGH – Offset 430h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 430h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.133 MAC_ADDRESS38_LOW – Offset 434h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 434h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.134 MAC_ADDRESS39_HIGH – Offset 438h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 438h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.135 MAC_ADDRESS39_LOW — Offset 43Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 43Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.136 MAC_ADDRESS40_HIGH — Offset 440h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 440h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.137 MAC_ADDRESS40_LOW – Offset 444h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 444h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.138 MAC_ADDRESS41_HIGH – Offset 448h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 448h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h	DMA Channel Select (DCS):

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Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.139 MAC_ADDRESS41_LOW — Offset 44Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.140 MAC_ADDRESS42_HIGH — Offset 450h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 450h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.141 MAC_ADDRESS42_LOW – Offset 454h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 454h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.142 MAC_ADDRESS43_HIGH – Offset 458h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 458h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.143 MAC_ADDRESS43_LOW – Offset 45Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 45Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.144 MAC_ADDRESS44_HIGH — Offset 460h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 460h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.145 MAC_ADDRESS44_LOW — Offset 464h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 464h	FFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.146 MAC_ADDRESS45_HIGH – Offset 468h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 468h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.147 MAC_ADDRESS45_LOW – Offset 46Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 46Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.148 MAC_ADDRESS46_HIGH – Offset 470h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 470h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.149 MAC_ADDRESS46_LOW — Offset 474h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 474h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.150 MAC_ADDRESS47_HIGH — Offset 478h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 478h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.151 MAC_ADDRESS47_LOW – Offset 47Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 47Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.152 MAC_ADDRESS48_HIGH – Offset 480h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 480h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h	DMA Channel Select (DCS):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.153 MAC_ADDRESS48_LOW — Offset 484h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 484h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.154 MAC_ADDRESS49_HIGH — Offset 488h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 488h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.155 MAC_ADDRESS49_LOW – Offset 48Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48Ch	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.156 MAC_ADDRESS50_HIGH – Offset 490h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 490h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.157 MAC_ADDRESS50_LOW – Offset 494h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 494h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.158 MAC_ADDRESS51_HIGH — Offset 498h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 498h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.159 MAC_ADDRESS51_LOW — Offset 49Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 49Ch	FFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.160 MAC_ADDRESS52_HIGH – Offset 4A0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.161 MAC_ADDRESS52_LOW – Offset 4A4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.162 MAC_ADDRESS53_HIGH – Offset 4A8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.163 MAC_ADDRESS53_LOW — Offset 4ACh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4ACh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.164 MAC_ADDRESS54_HIGH — Offset 4B0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.165 MAC_ADDRESS54_LOW – Offset 4B4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.166 MAC_ADDRESS55_HIGH – Offset 4B8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h	DMA Channel Select (DCS):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.167 MAC_ADDRESS55_LOW — Offset 4BCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4BCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.168 MAC_ADDRESS56_HIGH — Offset 4C0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C0h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.169 MAC_ADDRESS56_LOW – Offset 4C4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.170 MAC_ADDRESS57_HIGH – Offset 4C8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.171 MAC_ADDRESS57_LOW – Offset 4CCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4CCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.172 MAC_ADDRESS58_HIGH — Offset 4D0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.173 MAC_ADDRESS58_LOW — Offset 4D4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D4h	FFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.174 MAC_ADDRESS59_HIGH – Offset 4D8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.175 MAC_ADDRESS59_LOW – Offset 4DCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4DCh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.176 MAC_ADDRESS60_HIGH – Offset 4E0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.177 MAC_ADDRESS60_LOW — Offset 4E4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.178 MAC_ADDRESS61_HIGH — Offset 4E8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.179 MAC_ADDRESS61_LOW – Offset 4ECh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4ECh	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.180 MAC_ADDRESS62_HIGH – Offset 4F0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h	DMA Channel Select (DCS):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.181 MAC_ADDRESS62_LOW — Offset 4F4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F4h	FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.182 MAC_ADDRESS63_HIGH — Offset 4F8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F8h	0000FFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Address Enable (AE): When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	Reserved
18:16	0h RW	DMA Channel Select (DCS): This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	MAC Address32 [47:32] (ADDRHI): This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

11.2.183 MAC_ADDRESS63_LOW – Offset 4FCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4FCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFh RW	MAC Address32 [31:0] (ADDRLO): This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

11.2.184 MMC_CONTROL – Offset 700h

This register establishes the operating mode of MAC Management Counters.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 700h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RW	Update MMC Counters for Dropped Broadcast Packets (UCDBC): Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. 0x0 (DISABLE): Update MMC Counters for Dropped Broadcast Packets is disabled. 0x1 (ENABLE): Update MMC Counters for Dropped Broadcast Packets is enabled.
7:6	0h RO	Reserved
5	0h RW	Full-Half Preset (CNTPRSTLVL): When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFFF. 0x0 (DISABLE): Full-Half Preset is disabled. 0x1 (ENABLE): Full-Half Preset is enabled.
4	0h RW	Counters Preset (CNTPRST): When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
3	0h RW	MMC Counter Freeze (CNTFREEZ): When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. 0x0 (DISABLE): MMC Counter Freeze is disabled. 0x1 (ENABLE): MMC Counter Freeze is enabled.
2	0h RW	Reset on Read (RSTONRD): When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. 0x0 (DISABLE): Reset on Read is disabled. 0x1 (ENABLE): Reset on Read is enabled.
1	0h RW	Counter Stop Rollover (CNTSTOPRO): When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0x0 (DISABLE): Counter Stop Rollover is disabled. 0x1 (ENABLE): Counter Stop Rollover is enabled.
0	0h RW	Counters Reset (CNTRST): When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.

11.2.185 MMC_RX_INTERRUPT — Offset 704h

This register maintains the interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur:

- Receive statistic counters reach half of their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter).
- Receive statistic counters cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter).

When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register

is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Note: R_SS_RC means that this register bit is set internally, and it is cleared when the Counter register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 704h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	<p>MMC Receive LPI transition counter interrupt status (RXLPIITRCIS): This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI transition Counter Interrupt Status detected.</p>
26	0h RO/V	<p>MMC Receive LPI microsecond counter interrupt status (RXLPIUSCIS): This bit is set when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI microsecond Counter Interrupt Status detected.</p>
25	0h RO/V	<p>MMC Receive Control Packet Counter Interrupt Status (RXCTRLPIS): This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Control Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Control Packet Counter Interrupt Status detected.</p>
24	0h RO/V	<p>MMC Receive Error Packet Counter Interrupt Status (RXRCVERRPIS): This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Error Packet Counter Interrupt Status detected.</p>
23	0h RO/V	<p>MMC Receive Watchdog Error Packet Counter Interrupt Status (RXWDOPGIS): This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected.</p>
22	0h RO/V	<p>MMC Receive VLAN Good Bad Packet Counter Interrupt Status (RXVLANGBPIS): This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status detected.</p>
21	0h RO/V	<p>MMC Receive FIFO Overflow Packet Counter Interrupt Status (RXFOVPIS): This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status detected.</p>
20	0h RO/V	<p>MMC Receive Pause Packet Counter Interrupt Status (RXPAUSPIS): This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected.</p>
19	0h	<p>MMC Receive Out Of Range Error Packet Counter Interrupt Status. (RXORANGEPIIS):</p> <p style="text-align: right;"><i>continued...</i></p>

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	<p>This bit is set when the rxoutofrangetype counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status detected.</p>
18	0h RO/V	<p>MMC Receive Length Error Packet Counter Interrupt Status (RXLENERPIS):</p> <p>This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Length Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Length Error Packet Counter Interrupt Status detected.</p>
17	0h RO/V	<p>MMC Receive Unicast Good Packet Counter Interrupt Status (RXUCGPIS):</p> <p>This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status detected.</p>
16	0h RO/V	<p>MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (RX1024TMAXOCTGBPIS):</p> <p>This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.</p>
15	0h RO/V	<p>MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (RX512T1023OCTGBPIS):</p> <p>This bit is set when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.</p>
14	0h RO/V	<p>MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status (RX256T511OCTGBPIS):</p> <p>This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.</p>
13	0h RO/V	<p>MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status (RX128T255OCTGBPIS):</p> <p>This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.</p>
12	0h RO/V	<p>MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status (RX65T127OCTGBPIS):</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.</p>
11	0h RO/V	<p>MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status (RX64OCTGBPIS):</p> <p>This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status detected.</p>
10	0h RO/V	<p>MMC Receive Oversize Good Packet Counter Interrupt Status (RXOSIZEGPIS):</p> <p>This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected.</p>
9	0h RO/V	<p>MMC Receive Undersize Good Packet Counter Interrupt Status (RXUSIZEGPIS):</p> <p>This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status detected.</p>
8	0h RO/V	<p>MMC Receive Jabber Error Packet Counter Interrupt Status (RXJABERPIS):</p> <p>This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status detected.</p>
7	0h RO/V	<p>MMC Receive Runt Packet Counter Interrupt Status (RXRUNTPIS):</p> <p>This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Runt Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive Runt Packet Counter Interrupt Status detected.</p>
6	0h RO/V	<p>MMC Receive Alignment Error Packet Counter Interrupt Status (RXALGNERPIS):</p> <p>This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status detected.</p>
5	0h RO/V	<p>MMC Receive CRC Error Packet Counter Interrupt Status (RXCRCERPIS):</p> <p>This bit is set when the rxrcrerror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status detected.</p>
4	0h RO/V	<p>MMC Receive Multicast Good Packet Counter Interrupt Status (RXMCGPIS):</p> <p>This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (INACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status detected.
3	0h RO/V	MMC Receive Broadcast Good Packet Counter Interrupt Status (RXBCGPIS): This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status detected.
2	0h RO/V	MMC Receive Good Octet Counter Interrupt Status (RXGOCTIS): This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Octet Counter Interrupt Status detected.
1	0h RO/V	MMC Receive Good Bad Octet Counter Interrupt Status (RXGBOCTIS): This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status detected.
0	0h RO/V	MMC Receive Good Bad Packet Counter Interrupt Status (RXGBPktIS): This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status detected.

11.2.186 MMC_TX_INTERRUPT — Offset 708h

This register maintains the interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values

(0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter).

When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read.

The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 708h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	<p>MMC Transmit LPI transition counter interrupt status (TXLPITRCIS): This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI transition Counter Interrupt Status detected.</p>
26	0h RO/V	<p>MMC Transmit LPI microsecond counter interrupt status (TXLPIUSCIS): This bit is set when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status detected.</p>
25	0h RO/V	<p>MMC Transmit Oversize Good Packet Counter Interrupt Status (TXOSIZEGPIS): This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status detected.</p>
24	0h RO/V	<p>MMC Transmit VLAN Good Packet Counter Interrupt Status (TXVLANGPIS): This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status detected.</p>
23	0h RO/V	<p>MMC Transmit Pause Packet Counter Interrupt Status (TXPAUSPIS): This bit is set when the txpausepacketerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected.</p>
22	0h RO/V	<p>MMC Transmit Excessive Deferral Packet Counter Interrupt Status (TXEXDEFPIS): This bit is set when the txexcessdef counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status detected.</p>
21	0h RO/V	<p>MMC Transmit Good Packet Counter Interrupt Status (TXGPKTIS): This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Packet Counter Interrupt Status detected.</p>
20	0h RO/V	<p>MMC Transmit Good Octet Counter Interrupt Status (TXGOCTIS): This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Octet Counter Interrupt Status detected.</p>
19	0h	<p>MMC Transmit Carrier Error Packet Counter Interrupt Status (TXCARERPIS):</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	<p>This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status detected.</p>
18	0h RO/V	<p>MMC Transmit Excessive Collision Packet Counter Interrupt Status (TXEXCOLPIS):</p> <p>This bit is set when the txexcesscol counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status detected.</p>
17	0h RO/V	<p>MMC Transmit Late Collision Packet Counter Interrupt Status (TXLATCOLPIS):</p> <p>This bit is set when the txlatecol counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status detected.</p>
16	0h RO/V	<p>MMC Transmit Deferred Packet Counter Interrupt Status (TXDEFPIS):</p> <p>This bit is set when the txdeferred counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status detected.</p>
15	0h RO/V	<p>MMC Transmit Multiple Collision Good Packet Counter Interrupt Status (TXMCOLGPIS):</p> <p>This bit is set when the txmulticol_g counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status detected.</p>
14	0h RO/V	<p>MMC Transmit Single Collision Good Packet Counter Interrupt Status (TXSCOLGPIS):</p> <p>This bit is set when the txsinglecol_g counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status detected.</p>
13	0h RO/V	<p>MMC Transmit Underflow Error Packet Counter Interrupt Status (TXUFLOWERPIS):</p> <p>This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status detected.</p>
12	0h RO/V	<p>MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status (TXBCGBPIS):</p> <p>This bit is set when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status detected.</p>
11	0h RO/V	<p>MMC Transmit Multicast Good Bad Packet Counter Interrupt Status (TXMCGBPIS):</p> <p>The bit is set when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status detected.
10	0h RO/V	MMC Transmit Unicast Good Bad Packet Counter Interrupt Status (TXUCGBPIS): This bit is set when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status detected.
9	0h RO/V	MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (TX1024TMAXOCTGBPIS): This bit is set when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
8	0h RO/V	MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (TX512T1023OCTGBPIS): This bit is set when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.
7	0h RO/V	MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status (TX256T511OCTGBPIS): This bit is set when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
6	0h RO/V	MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status (TX128T255OCTGBPIS): This bit is set when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
5	0h RO/V	MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status (TX65T127OCTGBPIS): This bit is set when the tx65to127octets_gb counter reaches half the maximum value, and also when it reaches the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
4	0h	MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status (TX64OCTGBPIS): <i>continued...</i>

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	This bit is set when the tx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status detected.
3	0h RO/V	MMC Transmit Multicast Good Packet Counter Interrupt Status (TXMCGPIS): This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status detected.
2	0h RO/V	MMC Transmit Broadcast Good Packet Counter Interrupt Status (TXBCGPIS): This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status detected.
1	0h RO/V	MMC Transmit Good Bad Packet Counter Interrupt Status (TXGBPKTIS): This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status detected.
0	0h RO/V	MMC Transmit Good Bad Octet Counter Interrupt Status (TXGBOCTIS): This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status detected.

11.2.187 MMC_RX_INTERRUPT_MASK — Offset 70Ch

This register maintains the masks for interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values.

This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RW	MMC Receive LPI transition counter interrupt Mask (RXLPITRCIM): Setting this bit masks the interrupt when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): MMC Receive LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI transition counter interrupt Mask is enabled.
26	0h RW	MMC Receive LPI microsecond counter interrupt Mask (RXLPIUSCIM): Setting this bit masks the interrupt when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI microsecond counter interrupt Mask is enabled.
25	0h RW	MMC Receive Control Packet Counter Interrupt Mask (RXCTRLPIM): Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Control Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Control Packet Counter Interrupt Mask is enabled.
24	0h RW	MMC Receive Error Packet Counter Interrupt Mask (RXRCVERRPIM): Setting this bit masks the interrupt when the rxrcerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Error Packet Counter Interrupt Mask is enabled.
23	0h RW	MMC Receive Watchdog Error Packet Counter Interrupt Mask (RXWDOGPIM): Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled.
22	0h RW	MMC Receive VLAN Good Bad Packet Counter Interrupt Mask (RXVLANGBPIM): Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is enabled.
21	0h RW	MMC Receive FIFO Overflow Packet Counter Interrupt Mask (RXFOVPIM): Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled.
20	0h RW	MMC Receive Pause Packet Counter Interrupt Mask (RXPAUSPIM): Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled.
19	0h RW	MMC Receive Out Of Range Error Packet Counter Interrupt Mask (RXORANGEPI): Setting this bit masks the interrupt when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is enabled.
18	0h RW	MMC Receive Length Error Packet Counter Interrupt Mask (RXLENERPI): Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Length Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Length Error Packet Counter Interrupt Mask is enabled.
17	0h RW	MMC Receive Unicast Good Packet Counter Interrupt Mask (RXUCGPIM): Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is enabled.
16	0h RW	MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask (RX1024TMAXOCTGBPIM): Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
15	0h RW	MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (RX512T1023OCTGBPIM): Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
14	0h RW	MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (RX256T511OCTGBPIM): Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
13	0h RW	MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (RX128T255OCTGBPIM): Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.
12	0h RW	MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (RX65T127OCTGBPIM): Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask (RX64OCTGBPIM): Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	MMC Receive Oversize Good Packet Counter Interrupt Mask (RXOSIZEGPIM): Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled.
9	0h RW	MMC Receive Undersize Good Packet Counter Interrupt Mask (RXUSIZEGPIM): Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is enabled.
8	0h RW	MMC Receive Jabber Error Packet Counter Interrupt Mask (RXJABERPIM): Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is enabled.
7	0h RW	MMC Receive Runt Packet Counter Interrupt Mask (RXRUNTPIM): Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Runt Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Runt Packet Counter Interrupt Mask is enabled.
6	0h RW	MMC Receive Alignment Error Packet Counter Interrupt Mask (RXALGNERPIM): Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is enabled.
5	0h RW	MMC Receive CRC Error Packet Counter Interrupt Mask (RXCRCERPI): Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is enabled.
4	0h RW	MMC Receive Multicast Good Packet Counter Interrupt Mask (RXMCGPIM): Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled.
3	0h RW	MMC Receive Broadcast Good Packet Counter Interrupt Mask (RXBCGPIM): Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is enabled.
2	0h RW	MMC Receive Good Octet Counter Interrupt Mask (RXGOCTIM): Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Octet Counter Interrupt Mask is enabled.
1	0h RW	MMC Receive Good Bad Octet Counter Interrupt Mask (RXGBOCTIM): Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is enabled.
0	0h RW	MMC Receive Good Bad Packet Counter Interrupt Mask (RXGBPDTIM): Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is enabled.

11.2.188 MMC_TX_INTERRUPT_MASK – Offset 710h

This register maintains the masks for interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 710h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RW	MMC Transmit LPI transition counter interrupt Mask (TXLPITRCIM): Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI transition counter interrupt Mask is enabled.
26	0h RW	MMC Transmit LPI microsecond counter interrupt Mask (TXLPIUSCIM): Setting this bit masks the interrupt when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI microsecond counter interrupt Mask is enabled.
25	0h RW	MMC Transmit Oversize Good Packet Counter Interrupt Mask (TXOSIZEGPIM): Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is enabled.
24	0h RW	MMC Transmit VLAN Good Packet Counter Interrupt Mask (TXVLANGPIM): Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is enabled.
23	0h RW	MMC Transmit Pause Packet Counter Interrupt Mask (TXPAUSPIM): Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled.
22	0h RW	MMC Transmit Excessive Deferral Packet Counter Interrupt Mask (TEXDEFPI): Setting this bit masks the interrupt when the txexcessdef counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is enabled.
21	0h RW	MMC Transmit Good Packet Counter Interrupt Mask (TXGPKTIM): Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Packet Counter Interrupt Mask is enabled.
20	0h	MMC Transmit Good Octet Counter Interrupt Mask (TXGOCTIM):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Octet Counter Interrupt Mask is enabled.
19	0h RW	MMC Transmit Carrier Error Packet Counter Interrupt Mask (TXCARERPIM): Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled.
18	0h RW	MMC Transmit Excessive Collision Packet Counter Interrupt Mask (TXEXCOLPIM): Setting this bit masks the interrupt when the txexcesscol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is enabled.
17	0h RW	MMC Transmit Late Collision Packet Counter Interrupt Mask (TXLATCOLPIM): Setting this bit masks the interrupt when the txlatecol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is enabled.
16	0h RW	MMC Transmit Deferred Packet Counter Interrupt Mask (TXDEFPIM): Setting this bit masks the interrupt when the txdeferred counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is enabled.
15	0h RW	MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask (TXMCOLGPIM): Setting this bit masks the interrupt when the txmulticol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is enabled.
14	0h RW	MMC Transmit Single Collision Good Packet Counter Interrupt Mask (TXSCOLGPIM): Setting this bit masks the interrupt when the txsinglecol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is enabled.
13	0h RW	MMC Transmit Underflow Error Packet Counter Interrupt Mask (TXUFLOWERPIM): Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled.
12	0h RW	MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask (TXBCGBPIM): Setting this bit masks the interrupt when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask (TXMCGBPIM): Setting this bit masks the interrupt when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is enabled.
10	0h	MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask (TXUCGBPIM):

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Bit Range	Default & Access	Field Name (ID): Description
	RW	<p>Setting this bit masks the interrupt when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is enabled.</p>
9	0h RW	<p>MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask (TX1024TMAXOCTGBPIM):</p> <p>Setting this bit masks the interrupt when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.</p>
8	0h RW	<p>MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (TX512T1023OCTGBPIM):</p> <p>Setting this bit masks the interrupt when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.</p>
7	0h RW	<p>MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (TX256T511OCTGBPIM):</p> <p>Setting this bit masks the interrupt when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.</p>
6	0h RW	<p>MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (TX128T255OCTGBPIM):</p> <p>Setting this bit masks the interrupt when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.</p>
5	0h RW	<p>MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (TX65T127OCTGBPIM):</p> <p>Setting this bit masks the interrupt when the tx65to127octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.</p>
4	0h RW	<p>MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask (TX64OCTGBPIM):</p> <p>Setting this bit masks the interrupt when the tx64octets_gb counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.</p>
3	0h RW	<p>MMC Transmit Multicast Good Packet Counter Interrupt Mask (TXMCGPIM):</p> <p>Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is enabled.</p>
2	0h	<p>MMC Transmit Broadcast Good Packet Counter Interrupt Mask (TXBCGPIM):</p>

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Bit Range	Default & Access	Field Name (ID): Description
	RW	Setting this bit masks the interrupt when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is enabled.
1	0h RW	MMC Transmit Good Bad Packet Counter Interrupt Mask (TXGBPDTIM): Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled.
0	0h RW	MMC Transmit Good Bad Octet Counter Interrupt Mask (TXGBOCTIM): Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled.

11.2.189 TX_OCTET_COUNT_GOOD_BAD — Offset 714h

This register provides the number of bytes transmitted by the Ethernet Controller, exclusive of preamble and retried bytes, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 714h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx Octet Count Good Bad (TXOCTGB): This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

11.2.190 TX_PACKET_COUNT_GOOD_BAD — Offset 718h

This register provides the number of good and bad packets transmitted by Ethernet Controller, exclusive of retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 718h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx Packet Count Good Bad (TXPKTGB): This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

11.2.191 TX_BROADCAST_PACKETS_GOOD — Offset 71Ch

This register provides the number of good broadcast packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 71Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Broadcast Packets Good (TXBCASTG): This field indicates the number of good broadcast packets transmitted.

11.2.192 TX_MULTICAST_PACKETS_GOOD — Offset 720h

This register provides the number of good multicast packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 720h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Multicast Packets Good (TXMCASTG): This field indicates the number of good multicast packets transmitted.

11.2.193 TX_64OCTETS_PACKETS_GOOD_BAD — Offset 724h

This register provides the number of good and bad packets transmitted by Ethernet Controller with length 64 bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 724h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx 64Octets Packets Good_Bad (TX64OCTGB): This field indicates the number of good and bad packets transmitted with length 64 bytes, exclusive of preamble and retried packets.

11.2.194 TX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 728h

This register provides the number of good and bad packets transmitted by Ethernet Controller with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 728h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	TX65_127OCTGB: Tx 65To127Octets Packets Good_Bad This field indicates the number of good and bad packets transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

11.2.195 TX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 72Ch

This register provides the number of good and bad packets transmitted by Ethernet Controller with length between 128 to 255 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 72Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx 128To255Octets Packets Good Bad (TX128_255OCTGB): This field indicates the number of good and bad packets transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried packets.

11.2.196 TX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 730h

This register provides the number of good and bad packets transmitted by Ethernet Controller with length between 256 to 511 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 730h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx 256To511Octets Packets Good Bad (TX256_511OCTGB): This field indicates the number of good and bad packets transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried packets.

11.2.197 TX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 734h

This register provides the number of good and bad packets transmitted by Ethernet Controller with length 512 to 1023 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 734h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx 512To1023Octets Packets Good Bad (TX512_1023OCTGB): This field indicates the number of good and bad packets transmitted with length between 512 and 1023 (inclusive) bytes, exclusive of preamble and retried packets.

11.2.198 TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 738h

This register provides the number of good and bad packets transmitted by Ethernet Controller with length 1024 to maxsize (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 738h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx 1024ToMaxOctets Packets Good Bad (TX1024_MAXOCTGB): This field indicates the number of good and bad packets transmitted with length between 1024 and maxsize (inclusive) bytes, exclusive of preamble and retried packets.

11.2.199 TX_UNICAST_PACKETS_GOOD_BAD — Offset 73Ch

This register provides the number of good and bad unicast packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 73Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx Unicast Packets Good Bad (TXUCASTGB): This field indicates the number of good and bad unicast packets transmitted.

11.2.200 TX_MULTICAST_PACKETS_GOOD_BAD — Offset 740h

This register provides the number of good and bad multicast packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 740h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx Multicast Packets Good Bad (TXMCASTGB): This field indicates the number of good and bad multicast packets transmitted.

11.2.201 TX_BROADCAST_PACKETS_GOOD_BAD — Offset 744h

This register provides the number of good and bad broadcast packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 744h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx Broadcast Packets Good Bad (TXBCASTGB): This field indicates the number of good and bad broadcast packets transmitted.

11.2.202 TX_UNDERFLOW_ERROR_PACKETS — Offset 748h

This register provides the number of packets aborted by Ethernet Controller because of packets underflow error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 748h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Underflow Error Packets (TXUNDRLW): This field indicates the number of packets aborted because of packets underflow error.

11.2.203 TX_SINGLE_COLLISION_GOOD_PACKETS — Offset 74Ch

This register provides the number of successfully transmitted packets by Ethernet Controller after a single collision in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Single Collision Good Packets (TXSNGLCOLG): This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

11.2.204 TX_MULTIPLE_COLLISION_GOOD_PACKETS — Offset 750h

This register provides the number of successfully transmitted packets by Ethernet Controller after multiple collisions in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 750h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Multiple Collision Good Packets (TXMULTCOLG): This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

11.2.205 TX_DEFERRED_PACKETS — Offset 754h

This register provides the number of successfully transmitted by Ethernet Controller after a deferral in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 754h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Deferred Packets (TXDEFRD): This field indicates the number of successfully transmitted after a deferral in the half-duplex mode.

11.2.206 TX_LATE_COLLISION_PACKETS — Offset 758h

This register provides the number of packets aborted by Ethernet Controller because of late collision error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 758h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Late Collision Packets (TXLATECOL): This field indicates the number of packets aborted because of late collision error.

11.2.207 TX_EXCESSIVE_COLLISION_PACKETS — Offset 75Ch

This register provides the number of packets aborted by Ethernet Controller because of excessive (16) collision errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 75Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Excessive Collision Packets (TXEXSCOL): This field indicates the number of packets aborted because of excessive (16) collision errors.

11.2.208 TX_CARRIER_ERROR_PACKETS — Offset 760h

This register provides the number of packets aborted by Ethernet Controller because of carrier sense error (no carrier or loss of carrier).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 760h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Carrier Error Packets (TXCARR): This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

11.2.209 TX_OCTET_COUNT_GOOD — Offset 764h

This register provides the number of bytes transmitted by Ethernet Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 764h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Octet Count Good (TXOCTG): This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

11.2.210 TX_PACKET_COUNT_GOOD — Offset 768h

This register provides the number of good packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 768h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Packet Count Good (TXPKTG): This field indicates the number of good packets transmitted.

11.2.211 TX_EXCESSIVE_DEFERRAL_ERROR — Offset 76Ch

This register provides the number of packets aborted by Ethernet Controller because of excessive deferral error (deferred for more than two max-sized packet times).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 76Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Excessive Deferral Error (TXEXSDEF): This field indicates the number of packets aborted because of excessive deferral error (deferred for more than two max-sized packet times).

11.2.212 TX_PAUSE_PACKETS — Offset 770h

This register provides the number of good Pause packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 770h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Pause Packets (TXPAUSE): This field indicates the number of good Pause packets transmitted.

11.2.213 TX_VLAN_PACKETS_GOOD — Offset 774h

This register provides the number of good VLAN packets transmitted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 774h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx VLAN Packets Good (TXVLANG): This field provides the number of good VLAN packets transmitted.

11.2.214 TX_OSIZE_PACKETS_GOOD — Offset 778h

This register provides the number of packets transmitted by Ethernet Controller without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 778h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx OSize Packets Good (TXOSIZG): This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

11.2.215 RX_PACKETS_COUNT_GOOD_BAD — Offset 780h

This register provides the number of good and bad packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 780h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Rx Packets Count Good Bad (RXPKTGB): This field indicates the number of good and bad packets received.

11.2.216 RX_OCTET_COUNT_GOOD_BAD — Offset 784h

This register provides the number of bytes received, exclusive of preamble, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 784h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Octet Count Good Bad (RXOCTGB): This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

11.2.217 RX_OCTET_COUNT_GOOD — Offset 788h

This register provides the number of bytes received by Ethernet Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 788h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Octet Count Good (RXOCTG): This field indicates the number of bytes received, exclusive of preamble, only in good packets.

11.2.218 RX_BROADCAST_PACKETS_GOOD — Offset 78Ch

This register provides the number of good broadcast packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Broadcast Packets Good (RXBCASTG): This field indicates the number of good broadcast packets received.

11.2.219 RX_MULTICAST_PACKETS_GOOD — Offset 790h

This register provides the number of good multicast packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 790h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Multicast Packets Good (RXMCASTG): This field indicates the number of good multicast packets received.

11.2.220 RX_CRC_ERROR_PACKETS — Offset 794h

This register provides the number of packets received by Ethernet Controller with CRC error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 794h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx CRC Error Packets (RXCRCERR): This field indicates the number of packets received with CRC error.

11.2.221 RX_ALIGNMENT_ERROR_PACKETS — Offset 798h

This register provides the number of packets received by Ethernet Controller with alignment (dribble) error. It is valid only in 10/100 mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 798h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Alignment Error Packets (RXALGNERR): This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode.

11.2.222 RX_RUNT_ERROR_PACKETS — Offset 79Ch

This register provides the number of packets received by Ethernet Controller with runt (length less than 64 bytes and CRC error) error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 79Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Runt Error Packets (RXRUNTERR): This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error.

11.2.223 RX_JABBER_ERROR_PACKETS — Offset 7A0h

This register provides the number of giant packets received by Ethernet Controller with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Jabber Error Packets (RXJABERR): This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

11.2.224 RX_UNDERSIZE_PACKETS_GOOD — Offset 7A4h

This register provides the number of packets received by Ethernet Controller with length less than 64 bytes, without any errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Undersize Packets Good (RXUNDERSZG): This field indicates the number of packets received with length less than 64 bytes, without any errors.

11.2.225 RX_OVERSIZE_PACKETS_GOOD — Offset 7A8h

This register provides the number of packets received by Ethernet Controller without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Ovsize Packets Good (RXOVERSZG): This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

11.2.226 RX_64OCTETS_PACKETS_GOOD_BAD — Offset 7ACh

This register provides the number of good and bad packets received by Ethernet Controller with length 64 bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ACh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx 64 Octets Packets Good Bad (RX64OCTGB): This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble.

11.2.227 RX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 7B0h

This register provides the number of good and bad packets received by Ethernet Controller with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RX65_127OCTGB: Rx 65-127 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

11.2.228 RX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 7B4h

This register provides the number of good and bad packets received by Ethernet Controller with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RX128_255OCTGB: Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

11.2.229 RX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 7B8h

This register provides the number of good and bad packets received by Ethernet Controller with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RX256_511OCTGB: Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

11.2.230 RX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 7BCh

This register provides the number of good and bad packets received by Ethernet Controller with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7BCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RX 512-1023 Octets Packets Good Bad (RX512_1023OCTGB):

Bit Range	Default & Access	Field Name (ID): Description
		This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

11.2.231 RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 7C0h

This register provides the number of good and bad packets received by Ethernet Controller with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx 1024-Max Octets Good Bad (RX1024_MAXOCTGB): This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

11.2.232 RX_UNICAST_PACKETS_GOOD — Offset 7C4h

This register provides the number of good unicast packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Unicast Packets Good (RXUCASTG): This field indicates the number of good unicast packets received.

11.2.233 RX_LENGTH_ERROR_PACKETS — Offset 7C8h

This register provides the number of packets received by Ethernet Controller with length error (Length Type field not equal to packet size), for all packets with valid length field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Length Error Packets (RXLENERR): This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

11.2.234 RX_OUT_OF_RANGE_TYPE_PACKETS — Offset 7CCh

This register provides the number of packets received by Ethernet Controller with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Rx Out of Range Type Packet (RXOUTOFRNG): This field indicates the number of packets received with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

11.2.235 RX_PAUSE_PACKETS — Offset 7D0h

This register provides the number of good and valid Pause packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Rx Pause Packets (RXPAUSEPKT): This field indicates the number of good and valid Pause packets received.

11.2.236 RX_FIFO_OVERFLOW_PACKETS — Offset 7D4h

This register provides the number of missed received packets because of FIFO overflow in Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Rx FIFO Overflow Packets (RXFIFOVFL): This field indicates the number of missed received packets because of FIFO overflow.

11.2.237 RX_VLAN_PACKETS_GOOD_BAD — Offset 7D8h

This register provides the number of good and bad VLAN packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx VLAN Packets Good Bad (RXVLANPKTGB): This field indicates the number of good and bad VLAN packets received.

11.2.238 RX_WATCHDOG_ERROR_PACKETS — Offset 7DCh

This register provides the number of packets received by Ethernet Controller with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7DCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Watchdog Error Packets (RXWDGERR): This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

11.2.239 RX_RECEIVE_ERROR_PACKETS — Offset 7E0h

This register provides the number of packets received by Ethernet Controller with Receive error or Packet Extension error on the GMII or MII interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Receive Error Packets (RXRCVERR): This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface.

11.2.240 RX_CONTROL_PACKETS_GOOD — Offset 7E4h

This register provides the number of good control packets received by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Control Packets Good (RXCTRLG): This field indicates the number of good control packets received.

11.2.241 TX_LPI_USEC_CNTR — Offset 7ECh

This register provides the number of microseconds Tx LPI is asserted by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx LPI Microseconds Counter (TXLPIUSC): This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

11.2.242 TX_LPI_TRAN_CNTR — Offset 7F0h

This register provides the number of times Ethernet Controller has entered Tx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx LPI Transition counter (TXLPITRC): This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments.

11.2.243 RX_LPI_USEC_CNTR — Offset 7F4h

This register provides the number of microseconds Rx LPI is sampled by Ethernet Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Rx LPI Microseconds Counter (RXLPIUSC): This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

11.2.244 RX_LPI_TRAN_CNTR — Offset 7F8h

This register provides the number of times Ethernet Controller has entered Rx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h	Rx LPI Transition counter (RXLPITRC):

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	This field indicates the number of times Rx LPI Entry has occurred.

11.2.245 MMC_IPC_RX_INTERRUPT_MASK — Offset 800h

This register maintains the mask for the interrupt generated from the receive IPC statistic counters.

The MMC Receive Checksum Off load Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Off load) statistic counters reach half their maximum value, and when they reach their maximum values. This register is 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29	0h RW	MMC Receive ICMP Error Octet Counter Interrupt Mask (RXICMPEROIM): Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled.
28	0h RW	MMC Receive ICMP Good Octet Counter Interrupt Mask (RXICMPGOIM): Setting this bit masks the interrupt when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is enabled.
27	0h RW	MMC Receive TCP Error Octet Counter Interrupt Mask (RXTCPEROIM): Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is enabled.
26	0h RW	MMC Receive TCP Good Octet Counter Interrupt Mask (RXTCPGOIM): Setting this bit masks the interrupt when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is enabled.
25	0h RW	MMC Receive UDP Good Octet Counter Interrupt Mask (RXUDPEROIM): Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is enabled.
24	0h RW	MMC Receive IPV6 No Payload Octet Counter Interrupt Mask (RXUDPGOIM): Setting this bit masks the interrupt when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is enabled.
23	0h	MMC Receive IPV6 Header Error Octet Counter Interrupt Mask (RXIPV6NOPAYOIM): <i>continued...</i>

Bit Range	Default & Access	Field Name (ID): Description
	RW	<p>Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled.</p>
22	0h RW	<p>MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6HEROIM):</p> <p>Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.</p>
21	0h RW	<p>MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6GOIM):</p> <p>Setting this bit masks the interrupt when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.</p>
20	0h RW	<p>MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask (RXIPV4UDSBLOIM):</p> <p>Setting this bit masks the interrupt when the rxipv4_udsl_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is enabled.</p>
19	0h RW	<p>MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask (RXIPV4FRAGOIM):</p> <p>Setting this bit masks the interrupt when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is enabled.</p>
18	0h RW	<p>MMC Receive IPV4 No Payload Octet Counter Interrupt Mask (RXIPV4NOPAYOIM):</p> <p>Setting this bit masks the interrupt when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is enabled.</p>
17	0h RW	<p>MMC Receive IPV4 Header Error Octet Counter Interrupt Mask (RXIPV4HEROIM):</p> <p>Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled.</p>
16	0h RW	<p>MMC Receive IPV4 Good Octet Counter Interrupt Mask (RXIPV4GOIM):</p> <p>Setting this bit masks the interrupt when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is enabled.</p>
15:14	0h RO	Reserved
13	0h RW	<p>MMC Receive ICMP Error Packet Counter Interrupt Mask (RXICMPERPIM):</p> <p>Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value.</p> <p>0x0 (DISABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled.</p>
12	0h RW	MMC Receive ICMP Good Packet Counter Interrupt Mask (RXICMPGPIM):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Setting this bit masks the interrupt when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is enabled.
11	0h RW	MMC Receive TCP Error Packet Counter Interrupt Mask (RXTCPERPIM): Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is enabled.
10	0h RW	MMC Receive TCP Good Packet Counter Interrupt Mask (RXTCPGPIM): Setting this bit masks the interrupt when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is enabled.
9	0h RW	MMC Receive UDP Error Packet Counter Interrupt Mask (RXUDPERPIM): Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is enabled.
8	0h RW	MMC Receive UDP Good Packet Counter Interrupt Mask (RXUDPGPIM): Setting this bit masks the interrupt when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is enabled.
7	0h RW	MMC Receive IPV6 No Payload Packet Counter Interrupt Mask (RXIPV6NOPAYPIM): Setting this bit masks the interrupt when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is enabled.
6	0h RW	MMC Receive IPV6 Header Error Packet Counter Interrupt Mask (RXIPV6HERPIM): Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled.
5	0h RW	MMC Receive IPV6 Good Packet Counter Interrupt Mask (RXIPV6GPIM): Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled.
4	0h RW	MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask (RXIPV4UDSBLPIM): Setting this bit masks the interrupt when the rxipv4_udsb_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is enabled.
3	0h RW	MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask (RXIPV4FRAGPIM): Setting this bit masks the interrupt when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is enabled.

continued...

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	MMC Receive IPV4 No Payload Packet Counter Interrupt Mask (RXIPV4NOPAYPIM): Setting this bit masks the interrupt when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is enabled.
1	0h RW	MMC Receive IPV4 Header Error Packet Counter Interrupt Mask (RXIPV4HERPIM): Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled.
0	0h RW	MMC Receive IPV4 Good Packet Counter Interrupt Mask (RXIPV4GPIM): Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled.

11.2.246 MMC_IPC_RX_INTERRUPT — Offset 808h

This register maintains the interrupt that the receive IPC statistic counters generate.

The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits[7:0]) must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29	0h RO/V	MMC Receive ICMP Error Octet Counter Interrupt Status (RXICMPEROIS): This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status detected.
28	0h RO/V	MMC Receive ICMP Good Octet Counter Interrupt Status (RXICMPGOIS): This bit is set when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status detected.

continued...

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO/V	MMC Receive TCP Error Octet Counter Interrupt Status (RXTCPEROIS): This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status detected.
26	0h RO/V	MMC Receive TCP Good Octet Counter Interrupt Status (RXTCPGOIS): This bit is set when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status detected.
25	0h RO/V	MMC Receive UDP Error Octet Counter Interrupt Status (RXUDPEROIS): This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status detected.
24	0h RO/V	MMC Receive UDP Good Octet Counter Interrupt Status (RXUDPGOIS): This bit is set when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status detected.
23	0h RO/V	MMC Receive IPV6 No Payload Octet Counter Interrupt Status (RXIPV6NOPAYOIS): This bit is set when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status detected.
22	0h RO/V	MMC Receive IPV6 Header Error Octet Counter Interrupt Status (RXIPV6HEROIS): This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected.
21	0h RO/V	MMC Receive IPV6 Good Octet Counter Interrupt Status (RXIPV6GOIS): This bit is set when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status detected.
20	0h RO/V	RXIPV4UDSBL0IS: MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status This bit is set when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status detected.

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Bit Range	Default & Access	Field Name (ID): Description
19	0h RO/V	MMC Receive IPV4 Fragmented Octet Counter Interrupt Status (RXIPV4FRAGOIS): This bit is set when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status detected.
18	0h RO/V	MMC Receive IPV4 No Payload Octet Counter Interrupt Status (RXIPV4NOPAYOIS): This bit is set when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status detected.
17	0h RO/V	MMC Receive IPV4 Header Error Octet Counter Interrupt Status (RXIPV4HEROIS): This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected.
16	0h RO/V	MMC Receive IPV4 Good Octet Counter Interrupt Status (RXIPV4GOIS): This bit is set when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status detected.
15:14	0h RO	Reserved
13	0h RO/V	MMC Receive ICMP Error Packet Counter Interrupt Status (RXICMPERPIS): This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status detected.
12	0h RO/V	MMC Receive ICMP Good Packet Counter Interrupt Status (RXICMPGPIS): This bit is set when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status detected.
11	0h RO/V	MMC Receive TCP Error Packet Counter Interrupt Status (RXTCPERPIS): This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status detected.
10	0h RO/V	MMC Receive TCP Good Packet Counter Interrupt Status (RXTCPGPIS): This bit is set when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status detected.
9	0h	MMC Receive UDP Error Packet Counter Interrupt Status (RXUDPERPIS):

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Bit Range	Default & Access	Field Name (ID): Description
	RO/V	This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status detected.
8	0h RO/V	MMC Receive UDP Good Packet Counter Interrupt Status (RXUDPGPIS): This bit is set when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status detected.
7	0h RO/V	MMC Receive IPV6 No Payload Packet Counter Interrupt Status (RXIPV6NOPAYPIS): This bit is set when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status detected.
6	0h RO/V	MMC Receive IPV6 Header Error Packet Counter Interrupt Status (RXIPV6HERPIS): This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected.
5	0h RO/V	MMC Receive IPV6 Good Packet Counter Interrupt Status (RXIPV6GPIS): This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status detected.
4	0h RO/V	MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status (RXIPV4UDSBLPIS): This bit is set when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status detected.
3	0h RO/V	MMC Receive IPV4 Fragmented Packet Counter Interrupt Status (RXIPV4FRAGPIS): This bit is set when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status detected.
2	0h RO/V	MMC Receive IPV4 No Payload Packet Counter Interrupt Status (RXIPV4NOPAYPIS): This bit is set when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status detected.
1	0h RO/V	MMC Receive IPV4 Header Error Packet Counter Interrupt Status (RXIPV4HERPIS): This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value.

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Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected.
0	0h RO/V	MMC Receive IPV4 Good Packet Counter Interrupt Status (RXIPV4GPIS): This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status detected.

11.2.247 RXIPV4_GOOD_PACKETS — Offset 810h

This register provides the number of good IPv4 datagrams received by Ethernet Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 Good Packets (RXIPV4GDPKT): This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

11.2.248 RXIPV4_HEADER_ERROR_PACKETS — Offset 814h

RxIPv4 Header Error Packets

This register provides the number of IPv4 datagrams received by Ethernet Controller with header (checksum, length, or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 Header Error Packets (RXIPV4HDRERRPKT): This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

11.2.249 RXIPV4_NO_PAYLOAD_PACKETS — Offset 818h

This register provides the number of IPv4 datagram packets received by Ethernet Controller that did not have a TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxIPv4 Payload Packets (RXIPV4NOPAYPKT): This field indicates the number of IPv4 datagram packets received that did not have a TCP, UDP, or ICMP payload.

11.2.250 RXIPV4_FRAGMENTED_PACKETS — Offset 81Ch

This register provides the number of good IPv4 datagrams received by Ethernet Controller with fragmentation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxIPv4 Fragmented Packets (RXIPV4FRAGPKT): This field indicates the number of good IPv4 datagrams received with fragmentation.

11.2.251 RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS — Offset 820h

This register provides the number of good IPv4 datagrams received by Ethernet Controller that had a UDP payload with checksum disabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxIPv4 UDP Checksum Disabled Packets (RXIPV4UDSBLPKT): This field indicates the number of good IPv4 datagrams received that had a UDP payload with checksum disabled.

11.2.252 RXIPV6_GOOD_PACKETS — Offset 824h

This register provides the number of good IPv6 datagrams received by Ethernet Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 824h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxIPv6 Good Packets (RXIPV6GDPKT): This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

11.2.253 RXIPV6_HEADER_ERROR_PACKETS — Offset 828h

This register provides the number of IPv6 datagrams received by Ethernet Controller with header (length or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxIPv6 Header Error Packets (RXIPV6HDRERRPKT): This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

11.2.254 RXIPV6_NO_PAYLOAD_PACKETS — Offset 82Ch

This register provides the number of IPv6 datagram packets received by Ethernet Controller that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 82Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxIPv6 Payload Packets (RXIPV6NOPAYPKT): This field indicates the number of IPv6 datagram packets received that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

11.2.255 RXUDP_GOOD_PACKETS — Offset 830h

This register provides the number of good IP datagrams received by Ethernet Controller with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxUDP Good Packets (RXUDPGDPKT): This field indicates the number of good IP datagrams received with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

11.2.256 RXUDP_ERROR_PACKETS — Offset 834h

This register provides the number of good IP datagrams received by Ethernet Controller whose UDP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h	RxUDP Error Packets (RXUDPERRPKT):

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

11.2.257 RXTCP_GOOD_PACKETS — Offset 838h

This register provides the number of good IP datagrams received by Ethernet Controller with a good TCP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxTCP Good Packets (RXTCPGDPKT): This field indicates the number of good IP datagrams received with a good TCP payload.

11.2.258 RXTCP_ERROR_PACKETS — Offset 83Ch

This register provides the number of good IP datagrams received by Ethernet Controller whose TCP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxTCP Error Packets (RXTCPERRPKT): This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

11.2.259 RXICMP_GOOD_PACKETS — Offset 840h

This register provides the number of good IP datagrams received by Ethernet Controller with a good ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxICMP Good Packets (RXICMPGDPKT): This field indicates the number of good IP datagrams received with a good ICMP payload.

11.2.260 RXICMP_ERROR_PACKETS — Offset 844h

This register provides the number of good IP datagrams received by Ethernet Controller whose ICMP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxICMP Error Packets (RXICMPERRPKT): This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

11.2.261 RXIPV4_GOOD_OCTETS — Offset 850h

This register provides the number of bytes received by Ethernet Controller in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 Good Octets (RXIPV4GDOCT): This field indicates the number of bytes received in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.262 RXIPV4_HEADER_ERROR_OCTETS — Offset 854h

This register provides the number of bytes received by Ethernet Controller in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 854h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 Header Error Octets (RXIPV4HDRERROCT): This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.263 RXIPV4_NO_PAYLOAD_OCTETS — Offset 858h

This register provides the number of bytes received by Ethernet Controller in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 858h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 Payload Octets (RXIPV4NOPAYOCT): This field indicates the number of bytes received in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.264 RXIPV4_FRAGMENTED_OCTETS — Offset 85Ch

This register provides the number of bytes received by Ethernet Controller in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 85Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 Fragmented Octets (RXIPV4FRAGOCT): This field indicates the number of bytes received in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.265 RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS — Offset 860h

This register provides the number of bytes received by Ethernet Controller in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 860h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv4 UDP Checksum Disable Octets (RXIPV4UDSBLOCT): This field indicates the number of bytes received in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.266 RXIPV6_GOOD_OCTETS — Offset 864h

This register provides the number of bytes received by Ethernet Controller in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 864h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv6 Good Octets (RXIPV6GDOCT):

Bit Range	Default & Access	Field Name (ID): Description
		This field indicates the number of bytes received in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.267 RXIPV6_HEADER_ERROR_OCTETS — Offset 868h

This register provides the number of bytes received by Ethernet Controller in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 868h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv6 Header Error Octets (RXIPV6HDRERROCT): This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.268 RXIPV6_NO_PAYLOAD_OCTETS — Offset 86Ch

This register provides the number of bytes received by Ethernet Controller in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

Type	Size	Offset	Default
MMIO	32 bit	BAR + 86Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxIPv6 Payload Octets (RXIPV6NOPAYOCT): This field indicates the number of bytes received in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.)

11.2.269 RXUDP_GOOD_OCTETS — Offset 870h

This register provides the number of bytes received by Ethernet Controller in a good UDP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 870h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxUDP Good Octets (RXUDPGDOCT): This field indicates the number of bytes received in a good UDP segment. This counter does not count IP header bytes.

11.2.270 RXUDP_ERROR_OCTETS — Offset 874h

This register provides the number of bytes received by Ethernet Controller in a UDP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 874h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxUDP Error Octets (RXUDPERROCT): This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

11.2.271 RXTCP_GOOD_OCTETS — Offset 878h

This register provides the number of bytes received by Ethernet Controller in a good TCP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 878h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxTCP Good Octets (RXTCPGDOCT): This field indicates the number of bytes received in a good TCP segment. This counter does not count IP header bytes.

11.2.272 RXTCP_ERROR_OCTETS — Offset 87Ch

This register provides the number of bytes received by Ethernet Controller in a TCP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 87Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	RxTCP Error Octets (RXTCPERROCT): This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

11.2.273 RXICMP_GOOD_OCTETS — Offset 880h

This register provides the number of bytes received by Ethernet Controller in a good ICMP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 880h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxICMP Good Octets (RXICMPGDOCT): This field indicates the number of bytes received in a good ICMP segment. This counter does not count IP header bytes.

11.2.274 RXICMP_ERROR_OCTETS — Offset 884h

This register provides the number of bytes received by Ethernet Controller in an ICMP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 884h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	RxICMP Error Octets (RXICMPERROCT): This field indicates the number of bytes received in an ICMP segment that had checksum errors. This counter does not count IP header bytes.

11.2.275 MMC_FPE_TX_INTERRUPT — Offset 8A0h

This register maintains the interrupts generated from all FPE related Transmit statistics counters. The MMC FPE Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved
1	0h RO/V	MMC Tx Hold Request Counter Interrupt Status (HRCIS): This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected.
0	0h RO/V	MMC Tx FPE Fragment Counter Interrupt status (FCIS): This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

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Bit Range	Default & Access	Field Name (ID): Description
		Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected. 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected.

11.2.276 MMC_FPE_TX_INTERRUPT_MASK — Offset 8A4h

This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved
1	0h RW	MMC Transmit Hold Request Counter Interrupt Mask (HRCIM): Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled.
0	0h RW	MMC Transmit Fragment Counter Interrupt Mask (FCIM): Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled.

11.2.277 MMC_TX_FPE_FRAGMENT_CNTR — Offset 8A8h

This register provides the number of additional mPackets transmitted due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Tx FPE Fragment counter (TXFFC): This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

11.2.278 MMC_TX_HOLD_REQ_CNTR — Offset 8ACh

This register provides the count of number of times a hold request is given to MAC

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8ACh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Tx Hold Request Counter (TXHRC): This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

11.2.279 MMC_FPE_RX_INTERRUPT — Offset 8C0h

This register maintains the interrupts generated from all FPE related Receive statistics counters. The MMC FPE Receive Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RO/V	MMC Rx FPE Fragment Counter Interrupt Status (FCIS): This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected.
2	0h RO/V	MMC Rx Packet Assembly OK Counter Interrupt Status (PAOCIS): This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected.
1	0h RO/V	MMC Rx Packet SMD Error Counter Interrupt Status (PSECIS): This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected.
0	0h RO/V	MMC Rx Packet Assembly Error Counter Interrupt Status (PAECIS):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.</p> <p>0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected.</p> <p>0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected.</p>

11.2.280 MMC_FPE_RX_INTERRUPT_MASK — Offset 8C4h

This register maintains the masks for interrupts generated from all FPE related Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	<p>MMC Rx FPE Fragment Counter Interrupt Mask (FCIM):</p> <p>Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value.</p> <p>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.</p> <p>0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled.</p>
2	0h RW	<p>MMC Rx Packet Assembly OK Counter Interrupt Mask (PAOCIM):</p> <p>Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value.</p> <p>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.</p> <p>0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled.</p>
1	0h RW	<p>MMC Rx Packet SMD Error Counter Interrupt Mask (PSECIM):</p> <p>Setting this bit masks the interrupt when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value.</p> <p>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.</p> <p>0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled.</p>
0	0h RW	<p>MMC Rx Packet Assembly Error Counter Interrupt Mask (PAECIM):</p> <p>Setting this bit masks the interrupt when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value.</p> <p>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.</p> <p>0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled.</p> <p>0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled.</p>

11.2.281 MMC_RX_PACKET_ASSEMBLY_ERR_CNTR — Offset 8C8h

This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Packet Assembly Error Counter (PAEC): This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

11.2.282 MMC_RX_PACKET_SMD_ERR_CNTR — Offset 8CCh

This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Packet SMD Error Counter (PSEC): This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

11.2.283 MMC_RX_PACKET_ASSEMBLY_OK_CNTR — Offset 8D0h

This register provides the number of MAC frames that were successfully reassembled and delivered to MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Rx Packet Assembly OK Counter (PAOC): This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

11.2.284 MMC_RX_FPE_FRAGMENT_CNTR — Offset 8D4h

This register provides the number of additional mPackets received due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h	Rx FPE Fragment Counter (FFC):

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

11.2.285 MAC_L3_L4_CONTROL0 – Offset 900h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 900h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RW	DMA Channel Select Enable (DMCHENO): When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	Reserved
26:24	0h RW	DMA Channel Number (DMCHNO): When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	Reserved
21	0h RW	Layer 4 Destination Port Inverse Match Enable (L4DPIMO): When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	Layer 4 Destination Port Match Enable (L4DPM0): When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	Layer 4 Source Port Inverse Match Enable (L4SPIMO): When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	Layer 4 Source Port Match Enable (L4SPM0): When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled.

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	Reserved
16	0h RW	<p>Layer 4 Protocol Enable (L4PENO): When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching.</p> <p>The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set.</p> <p>0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.</p>
15:11	00h RW	<p>L3HDBM0: Layer 3 IP DA Higher Bits Match</p> <p>IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field:</p> <ul style="list-style-type: none"> - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. <p>IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits:</p> <ul style="list-style-type: none"> - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. <p>This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.</p>
10:6	00h RW	<p>L3HSBM0: Layer 3 IP SA Higher Bits Match</p> <p>IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field:</p> <ul style="list-style-type: none"> - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. <p>IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.</p>
5	0h RW	<p>Layer 3 IP DA Inverse Match Enable (L3DAIM0): When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high.</p> <p>0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.</p>
4	0h RW	<p>Layer 3 IP DA Match Enable (L3DAM0): When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Note: When the L3PENO bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering.</p> <p>0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.</p>
3	0h RW	<p>Layer 3 IP SA Inverse Match Enable (L3SAIM0):</p> <p>When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Source Address field is enabled for perfect matching.</p> <p>This bit is valid and applicable only when the L3SAM0 bit is set.</p> <p>0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.</p>
2	0h RW	<p>Layer 3 IP SA Match Enable (L3SAM0):</p> <p>When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching.</p> <p>Note: When the L3PENO bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering.</p> <p>0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.</p>
1	0h RO	Reserved
0	0h RW	<p>Layer 3 Protocol Enable (L3PENO):</p> <p>When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets.</p> <p>The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set.</p> <p>0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.</p>

11.2.286 MAC_LAYER4_ADDRESS0 – Offset 904h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core.

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 904h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	<p>Layer 4 Destination Port Number Field (L4DPO):</p> <p>When the L4PENO bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		When the L4PENO and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	Layer 4 Source Port Number Field (L4SP0): When the L4PENO bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PENO and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

11.2.287 MAC_LAYER3_ADDR0_REG0 — Offset 910h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 910h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 0 Field (L3A00): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

11.2.288 MAC_LAYER3_ADDR1_REG0 — Offset 914h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 914h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 1 Field (L3A10): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

11.2.289 MAC_LAYER3_ADDR2_REG0 — Offset 918h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 918h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 2 Field (L3A20): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

11.2.290 MAC_LAYER3_ADDR3_REG0 — Offset 91Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 91Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 3 Field (L3A30): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

11.2.291 MAC_L3_L4_CONTROL1 — Offset 930h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 930h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RW	DMA Channel Select Enable (DMCHEN1): When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	Reserved
26:24	0h	DMA Channel Number (DMCHN1):

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Bit Range	Default & Access	Field Name (ID): Description
	RW	When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	Reserved
21	0h RW	Layer 4 Destination Port Inverse Match Enable (L4DPM1): When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	Layer 4 Destination Port Match Enable (L4DPM1): When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	Layer 4 Source Port Inverse Match Enable (L4SPM1): When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	Layer 4 Source Port Match Enable (L4SPM1): When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	Reserved
16	0h RW	Layer 4 Protocol Enable (L4PEN1): When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	L3HDBM1: Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked.

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Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. <p>This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.</p>
10:6	00h RW	<p>L3HSBM1: Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSB[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.</p>
5	0h RW	<p>Layer 3 IP DA Inverse Match Enable (L3DAIM1): When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.</p>
4	0h RW	<p>Layer 3 IP DA Match Enable (L3DAM1): When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PENO bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.</p>
3	0h RW	<p>Layer 3 IP SA Inverse Match Enable (L3SAIM1): When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	Layer 3 IP SA Match Enable (L3SAM1): When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	Reserved
0	0h RW	Layer 3 Protocol Enable (L3PEN1): When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

11.2.292 MAC_LAYER4_ADDRESS1 — Offset 934h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core.

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 934h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	Layer 4 Destination Port Number Field (L4DP1): When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	Layer 4 Source Port Number Field (L4SP1): When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

11.2.293 MAC_LAYER3_ADDR0_REG1 — Offset 940h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 940h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 0 Field (L3A01): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

11.2.294 MAC_LAYER3_ADDR1_REG1 — Offset 944h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 944h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 1 Field (L3A11): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

11.2.295 MAC_LAYER3_ADDR2_REG1 — Offset 948h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 948h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 2 Field (L3A21): When the L3PENO and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets.

Bit Range	Default & Access	Field Name (ID): Description
		When the L3PENO bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

11.2.296 MAC_LAYER3_ADDR3_REG1 — Offset 94Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Layer 3 Address 3 Field (L3A31): When the L3PENO and L3SAMO bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PENO and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PENO bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

11.2.297 MAC_TIMESTAMP_CONTROL — Offset B00h

This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RW	AV 802.1AS Mode Enable (AV8021ASMEN): When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. 0x0 (DISABLE): AV 802.1AS Mode is disabled. 0x1 (ENABLE): AV 802.1AS Mode is enabled.
27:25	0h RO	Reserved
24	0h RW	Transmit Timestamp Status Mode (TXTSSTSM): When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. 0x0 (DISABLE): Transmit Timestamp Status Mode is disabled. 0x1 (ENABLE): Transmit Timestamp Status Mode is enabled.

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Bit Range	Default & Access	Field Name (ID): Description
23:21	0h RO	Reserved
20	0h RW	<p>External System Time Input (ESTI): When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: - To take the timestamp provided as status - To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time. 0x0 (DISABLE): External System Time Input is disabled. 0x1 (ENABLE): External System Time Input is enabled.</p>
19	0h RW	<p>Enable checksum correction during OST for PTP over UDP/IPv4 packets (CSC): When this bit is set, the last two bytes of PTP message sent over UDP/IPv4 is updated to keep the UDP checksum correct, for changes made to origin timestamp and/or correction field as part of one step timestamp operation. The application shall form the packet with these two dummy bytes. When reset, no updates are done to keep the UDP checksum correct. The application shall form the packet with UDP checksum set to 0. 0x0 (DISABLE): checksum correction during OST for PTP over UDP/IPv4 packets is disabled. 0x1 (ENABLE): checksum correction during OST for PTP over UDP/IPv4 packets is enabled.</p>
18	0h RW	<p>Enable MAC Address for PTP Packet Filtering (TSENMACADDR): When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. 0x0 (DISABLE): MAC Address for PTP Packet Filtering is disabled. 0x1 (ENABLE): MAC Address for PTP Packet Filtering is enabled.</p>
17:16	0h RW	<p>Select PTP packets for Taking Snapshots (SNAPTYPESEL): These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.</p>
15	0h RW	<p>Enable Snapshot for Messages Relevant to Host (TSMSTRENA): When this bit is set, the snapshot is taken only for the messages that are relevant to the host node. Otherwise, the snapshot is taken for the messages relevant to the agent node. 0x0 (DISABLE): Snapshot for Messages Relevant to Host is disabled. 0x1 (ENABLE): Snapshot for Messages Relevant to Host is enabled.</p>
14	0h RW	<p>Enable Timestamp Snapshot for Event Messages (TSEVNTENA): When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. 0x0 (DISABLE): Timestamp Snapshot for Event Messages is disabled. 0x1 (ENABLE): Timestamp Snapshot for Event Messages is enabled.</p>
13	1h RW	<p>Enable Processing of PTP Packets Sent over IPv4-UDP (TSIPV4ENA): When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv4-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv4-UDP is enabled.</p>
12	0h	<p>Enable Processing of PTP Packets Sent over IPv6-UDP (TSIPV6ENA):</p>

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Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv6-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv6-UDP is enabled.
11	0h RW	Enable Processing of PTP over Ethernet Packets (TSIPENA): When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. 0x0 (DISABLE): Processing of PTP over Ethernet Packets is disabled. 0x1 (ENABLE): Processing of PTP over Ethernet Packets is enabled.
10	0h RW	Enable PTP Packet Processing for Version 2 Format (TSVER2ENA): When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. 0x0 (DISABLE): PTP Packet Processing for Version 2 Format is disabled. 0x1 (ENABLE): PTP Packet Processing for Version 2 Format is enabled.
9	0h RW	Timestamp Digital or Binary Rollover Control (TSCTRLSSR): When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. 0x0 (DISABLE): Timestamp Digital or Binary Rollover Control is disabled. 0x1 (ENABLE): Timestamp Digital or Binary Rollover Control is enabled.
8	0h RW	Enable Timestamp for All Packets (TSENALL): When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. 0x0 (DISABLE): Timestamp for All Packets disabled. 0x1 (ENABLE): Timestamp for All Packets enabled.
7	0h RO	Reserved
6	0h RW	Presentation Time Generation Enable (PTGE): When this bit is set the Presentation Time generation is enabled. 0x0 (DISABLE): Presentation Time Generation is disabled. 0x1 (ENABLE): Presentation Time Generation is enabled.
5	0h RW	Update Addend Register (TSADDREG): When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Addend Register is not updated. 0x1 (ENABLE): Addend Register is updated.
4	0h RO	Reserved
3	0h RW	Update Timestamp (TSUPDT): When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled, MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not updated. 0x1 (ENABLE): Timestamp is updated.

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Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	<p>Initialize Timestamp (TSINIT): When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled, MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not initialized. 0x1 (ENABLE): Timestamp is initialized.</p>
1	0h RW	<p>Fine or Coarse Timestamp Update (TSCFUPDT): When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. 0x0 (COARSE): Coarse method is used to update system timestamp. 0x1 (FINE): Fine method is used to update system timestamp.</p>
0	0h RW	<p>Enable Timestamp (TSENA): When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. 0x0 (DISABLE): Timestamp is disabled. 0x1 (ENABLE): Timestamp is enabled.</p>

11.2.298 MAC_SUB_SECOND_INCREMENT — Offset B04h

This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:16	00h RW	<p>Sub-second Increment Value (SSINC): The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.</p>
15:8	00h RW	<p>Sub-nanosecond Increment Value (SNSINC): This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C.</p>
7:0	0h RO	Reserved

11.2.299 MAC_SYSTEM_TIME_SECONDS – Offset B08h

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Timestamp Second (TSS): The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

11.2.300 MAC_SYSTEM_TIME_NANOSECONDS – Offset B0Ch

The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:0	00000000h RO/V	Timestamp Sub Seconds (TSSS): The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

11.2.301 MAC_SYSTEM_TIME_SECONDS_UPDATE – Offset B10h

The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both registers before setting the TSINIT or TSUPDT bits in MAC_Timestamp_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Timestamp Seconds (TSS): The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, $2^{32} - 2$).

11.2.302 MAC_SYSTEM_TIME_NANOSECONDS_UPDATE — Offset B14h

MAC System Time Nanoseconds Update register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B14h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Add or Subtract Time (ADDSUB): When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. 0x0 (ADD): Add time. 0x1 (SUB): Subtract time.
30:0	0000000h RW	Timestamp Sub Seconds (TSSS): The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be $10^9 - \text{<sub-second value>}$. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be $2^{31} - \text{<sub-second value>}$. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, $2^{31} - 1$), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, $10^9 - 1$), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

11.2.303 MAC_TIMESTAMP_ADDEND — Offset B18h

Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register). The content of this register is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	0000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:0	0000000h RW	Timestamp Addend Register (TSAR): This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.	

11.2.304 MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS — Offset B1Ch

System Time - Higher Word Seconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B1Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:0	0000h RW	<p>Timestamp Higher Word Register (TSHWR): This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register.</p> <p>Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.</p>

11.2.305 MAC_TIMESTAMP_STATUS — Offset B20h

Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:25	00h RO/V	<p>Number of Auxiliary Timestamp Snapshots (ATSNS): This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.</p>
24	0h RO/V	<p>Auxiliary Timestamp Snapshot Trigger Missed (ATSSTM): This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.</p> <p>0x0 (INACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status detected.</p>
23:20	0h RO	Reserved
19:16	0h RO/V	<p>Auxiliary Timestamp Snapshot Trigger Identifier (ATSSTN): These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list:</p> <ul style="list-style-type: none"> - Bit 16: Auxiliary trigger 0 - Bit 17: Auxiliary trigger 1 - Bit 18: Auxiliary trigger 2 - Bit 19: Auxiliary trigger 3 <p>The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>
15	0h RO/V	<p>Tx Timestamp Status Interrupt Status (TXTSSIS): In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets.</p> <p>This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set).</p> <p>0x0 (INACTIVE): Tx Timestamp Status Interrupt status not detected. 0x1 (ACTIVE): Tx Timestamp Status Interrupt status detected.</p>
14:6	0h RO	Reserved
5	0h RO/V	<p>Timestamp Target Time Error (TSTRGTER1):</p> <p>This bit is set when the latest target time programmed in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit.</p> <p>Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.</p>
4	0h RO/V	<p>Timestamp Target Time Reached for Target Time PPS1 (TSTARGT1):</p> <p>When this bit is set and MCGREN1 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers. Access restriction applies.</p> <p>When this bit is set and MCGREN1 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[1] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p>
3	0h RO/V	<p>Timestamp Target Time Error (TSTRGTER0):</p> <p>This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit.</p> <p>Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	<p>Auxiliary Timestamp Trigger Snapshot (AUXTSTRIG): This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Auxiliary Timestamp Trigger Snapshot status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Trigger Snapshot status detected.</p>
1	0h RO/V	<p>Timestamp Target Time Reached (TSTARTGT0): When this bit is set and MCGRENO of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGRENO of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[0] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.</p>
0	0h RO/V	<p>Timestamp Seconds Overflow (TSSOVF): When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Seconds Overflow status not detected. 0x1 (ACTIVE): Timestamp Seconds Overflow status detected.</p>

11.2.306 MAC_TX_TIMESTAMP_STATUS_NANOSECONDS — Offset B30h

This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled.

The MAC_Tx_Timestamp_Status_Nanoseconds register, along with MAC_Tx_Timestamp_Status_Seconds, gives the 64-bit timestamp captured for the PTP packet successfully transmitted by the MAC. This value is considered to be read by the application when the last byte (bits [31:24]) of MAC_Tx_Timestamp_Status_Nanoseconds is read.

If the application does not read these registers and timestamp of another packet is captured, then either the current timestamp is lost (overwritten) or the new timestamp is lost (dropped), depending on the setting of the TXTSSTM bit of the MAC_Timestamp_Control register. The status bit TXTSC bit [15] in MAC_Timestamp_Status register is set whenever the MAC transmitter captures the timestamp.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	<p>Transmit Timestamp Status Missed (TXTSSMIS): When this bit is set, it indicates one of the following: - The timestamp of the current packet is ignored if TXTSSTM bit of the MAC_Timestamp_Control register is reset - The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (INACTIVE): Transmit Timestamp Status Missed status not detected. 0x1 (ACTIVE): Transmit Timestamp Status Missed status detected.
30:0	00000000h RO/V	Transmit Timestamp Status Low (TXTSSLO): This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

11.2.307 MAC_TX_TIMESTAMP_STATUS_SECONDS — Offset B34h

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Transmit Timestamp Status High (TXTSSHI): This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

11.2.308 MAC_AUXILIARY_CONTROL — Offset B40h

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved
5	0h RW	Auxiliary Snapshot 1 Enable (ATSEN1): This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot \$i is disabled. 0x1 (ENABLE): Auxiliary Snapshot \$i is enabled.
4	0h RW	Auxiliary Snapshot 0 Enable (ATSENO): This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot \$i is disabled. 0x1 (ENABLE): Auxiliary Snapshot \$i is enabled.
3:1	0h RO	Reserved
0	0h RW	Auxiliary Snapshot FIFO Clear (ATSFC): When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Auxiliary Snapshot FIFO Clear is disabled. 0x1 (ENABLE): Auxiliary Snapshot FIFO Clear is enabled.

11.2.309 MAC_AUXILIARY_TIMESTAMP_NANOSECONDS — Offset B48h

The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected while configuring the core.

You can store multiple snapshots in this FIFO. Bits[29:25] in MAC_Timestamp_Status indicate the fill-level of the FIFO. The top of the FIFO is removed only when the last byte (bits [31:24]) of MAC_Auxiliary_Timestamp_Seconds register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:0	0000000h RO/V	Auxiliary Timestamp (AUXTSLO): Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

11.2.310 MAC_AUXILIARY_TIMESTAMP_SECONDS — Offset B4Ch

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Auxiliary Timestamp (AUXTSHI): Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

11.2.311 MAC_TIMESTAMP_INGRESS_ASYM_CORR — Offset B50h

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h	One-Step Timestamp Ingress Asymmetry Correction (OSTIAC):

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^{16} . For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

11.2.312 MAC_TIMESTAMP_EGRESS_ASYM_CORR — Offset B54h

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	One-Step Timestamp Egress Asymmetry Correction (OSTEAC): This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^{16} . For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFFD_8000, which is the 2's complement of 0x0002_8000 ($2.5 * 2^{16}$). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC ($3.3 * 2^{16}$).

11.2.313 MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND — Offset B58h

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Timestamp Ingress Correction (TSIC): This field contains the ingress path correction value as defined by the Ingress Correction expression.

11.2.314 MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND — Offset B5Ch

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h	Timestamp Egress Correction (TSEC):

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

11.2.315 MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC — Offset B60h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for ingress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:8	00h RW	Timestamp Ingress Correction, sub-nanoseconds (TSICSNS): This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression.
7:0	0h RO	Reserved

11.2.316 MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC — Offset B64h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for egress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:8	00h RW	Timestamp Egress Correction, sub-nanoseconds (TSECSNS): This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression.
7:0	0h RO	Reserved

11.2.317 MAC_TIMESTAMP_INGRESS_LATENCY — Offset B68h

This register holds the Ingress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27:16	000h RO/V	Ingress Timestamp Latency, in sub-nanoseconds (ITLNS): This register holds the average latency in sub-nanoseconds between the input ports (phy_rx_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken. Ingress correction value is computed as described in the section 7.1.2.4.1 of QoS Databook.
15:8	00h RO/V	Ingress Timestamp Latency, in nanoseconds (ITLSNS): This register holds the average latency in nanoseconds between the input ports (phy_rx_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken. Ingress correction value is computed as described in the section 7.1.2.4.1 of QoS Databook.
7:0	0h RO	Reserved

11.2.318 MAC_TIMESTAMP_EGRESS_LATENCY — Offset B6Ch

This register holds the Egress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27:16	000h RO/V	Egress Timestamp Latency, in nanoseconds (ETLNS): This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_tx_o) of the MAC.
15:8	00h RO/V	Egress Timestamp Latency, in sub-nanoseconds (ETLSNS): This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_tx_o) of the MAC.
7:0	0h RO	Reserved

11.2.319 MAC_PPS_CONTROL — Offset B70h

PPS Control register.

Bits[30:24] of this register are valid only when four Flexible PPS outputs are selected.
 Bits[22:16] are valid only when three or more Flexible PPS outputs are selected.
 Bits[14:8] are valid only when two or more Flexible PPS outputs are selected.

Bits[6:4] are valid only when Flexible PPS feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
15	0h RW	<p>MCGR Mode Enable for PPS1 Output (MCGREN1): This field enables the 1st PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (DISABLE): 1st PPS instance is disabled to operate in PPS or MCGR mode. 0x1 (ENABLE): 1st PPS instance is enabled to operate in PPS or MCGR mode.</p>
14:13	0h RW	<p>Target Time Register Mode for PPS1 Output (TIMESEL): This field indicates the Target Time registers (MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds) mode for PPS1 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARTT1 (MAC_Timestamp_Status[4]). 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.</p>
12	0h RO	Reserved
11:8	0h RW	<p>Flexible PPS1 Output Control (PPSCMD1): This field controls the flexible PPS1 output signal. This field is similar to the PPSCMD0 field. If MCGREN1 is set, then PPSCMD1 indicated by these 4 bits [11:8] are taken as Presentation Time Control bits for media clock generation and recovery for comparator instance 1. This field is similar to the PPSCMD0 Presentation Time Control bits. If MCGREN1 is not set then only 3 bits from [10:8] is used as PPSCMD1 and the 4th bit is to be set as 0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p>
7	0h RW	<p>MCGR Mode Enable for PPS0 Output (MCGRENO): This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode. 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode.</p>
6:5	0h RW	<p>Target Time Register Mode for PPS0 Output (TRGTMODSEL0): Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARTT0 (MAC_Timestamp_Status[1]). 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.</p>
4	0h RW	<p>Flexible PPS Output Mode Enable (PPSENO): When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). 0x0 (DISABLE): Flexible PPS Output Mode is disabled. 0x1 (ENABLE): Flexible PPS Output Mode is enabled.</p>
3:0	0h RW	PPS Output Frequency Control (PPSCTRL_PPSCMD):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>This field controls the frequency of the PPS0 output signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies:</p> <ul style="list-style-type: none"> - 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. - 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. - 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. - 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. - .. - 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. <p>Note:</p> <p>In the binary rollover mode, the PPS output signal has a duty cycle of 50 percent with these frequencies.</p> <p>In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example:</p> <ul style="list-style-type: none"> - When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms - When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) - When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high) <p>This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register.</p> <p>or</p> <p>Flexible PPS Output Control</p> <p>Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0:</p> <ul style="list-style-type: none"> - 0000: No Command - 0001: START Single Pulse <p>This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register.</p> <ul style="list-style-type: none"> - 0010: START Pulse Train <p>This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands.</p> <ul style="list-style-type: none"> - 0011: Cancel START <p>This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time.</p> <ul style="list-style-type: none"> - 0100: STOP Pulse train at time <p>This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses.</p> <ul style="list-style-type: none"> - 0101: STOP Pulse Train immediately <p>This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010).</p> <ul style="list-style-type: none"> - 110: Cancel STOP Pulse train <p>This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command.</p> <ul style="list-style-type: none"> - 0111-1111: Reserved <p>or</p>
		<p>Presentation Time Control</p> <p>If MCGRENO is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0:</p>

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed - 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0100-1000: Reserved - 1001: Toggle output on compare - 1010: Pulse output low on compare for one PTP-clock cycle - 1011: Pulse output high on compare for one PTP-clock cycle - 1100-1111: Reserved

11.2.320 MAC_PPS0_TARGET_TIME_SECONDS — Offset B80h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	<p>PPS Target Time Seconds Register (TSTRH0):</p> <p>This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register.</p> <p>If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.</p>

11.2.321 MAC_PPS0_TARGET_TIME_NANOSECONDS — Offset B84h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	<p>PPS Target Time Register Busy (TRGTBUSY0):</p> <p>The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain.</p> <p>The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain. The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted.</p> <p>0x0 (INACTIVE): PPS Target Time Register Busy status is not detected.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	<p>Target Time Low for PPS Register (TTSLO): This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p>

11.2.322 MAC_PPS0_INTERVAL — Offset B88h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	<p>PPS Output Signal Interval (PPSINT0): These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.</p>

11.2.323 MAC_PPS0_WIDTH — Offset B8Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	<p>PPS Output Signal Width (PPSWIDTH0): These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.</p>

11.2.324 MAC_PPS1_TARGET_TIME_SECONDS — Offset B90h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	PPS Target Time Seconds Register (TSTRH1): This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If the DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

11.2.325 MAC_PPS1_TARGET_TIME_NANOSECONDS — Offset B94h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	PPS Target Time Register Busy (TRGTBUSY1): The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain. The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	Target Time Low for PPS Register (TTSL1): This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

11.2.326 MAC_PPS1_INTERVAL — Offset B98h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	PPS Output Signal Interval (PPSINT1): These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

11.2.327 MAC_PPS1_WIDTH — Offset B9Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	PPS Output Signal Width (PPSWIDTH1): These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

11.2.328 MAC_PTO_CONTROL — Offset BC0h

This register controls the PTP Offload Engine operation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:8	00h RW	Domain Number (DN): This field indicates the domain Number in which the PTP node is operating.
7	0h RW	Disable Peer Delay Response response generation (PDRDIS): When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not generated for received Peer Delay Request (Pdelay_Req) request packet, as required by the programmed mode. Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in Hardware and/or Pdelay_Resp generation is handled by Software.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (ENABLE): Peer Delay Response response generation is enabled. 0x1 (DISABLE): Peer Delay Response response generation is disabled.
6	0h RW	Disable PTO Delay Request/Response response generation (DRRDIS): When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode. 0x0 (ENABLE): PTO Delay Request/Response response generation is enabled. 0x1 (DISABLE): PTO Delay Request/Response response generation is disabled.
5	0h RW	Automatic PTP Pdelay_Req message Trigger (APDREQTRIG): When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP Pdelay_Req message Trigger is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message Trigger is enabled.
4	0h RW	Automatic PTP SYNC message Trigger (ASYNCTRIG): When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP SYNC message Trigger is disabled. 0x1 (ENABLE): Automatic PTP SYNC message Trigger is enabled.
3	0h RO	Reserved
2	0h RW	Automatic PTP Pdelay_Req message Enable (APDREQEN): When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode. 0x0 (DISABLE): Automatic PTP Pdelay_Req message is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message is enabled.
1	0h RW	Automatic PTP SYNC message Enable (ASYNCEN): When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Host mode. 0x0 (DISABLE): Automatic PTP SYNC message is disabled. 0x1 (ENABLE): Automatic PTP SYNC message is enabled.
0	0h RW	PTP Offload Enable (PTOEN): When this bit is set, the PTP Offload feature is enabled. 0x0 (DISABLE): PTP Offload feature is disabled. 0x1 (ENABLE): PTP Offload feature is enabled.

11.2.329 MAC_SOURCE_PORT_IDENTITY0 — Offset BC4h

This register contains Bits[31:0] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h	Source Port Identity 0 (SPIO):

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field indicates bits [31:0] of sourcePortIdentity of PTP node.

11.2.330 MAC_SOURCE_PORT_IDENTITY1 — Offset BC8h

This register contains Bits[63:32] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Source Port Identity 1 (SPI1): This field indicates bits [63:32] of sourcePortIdentity of PTP node.

11.2.331 MAC_SOURCE_PORT_IDENTITY2 — Offset BCCh

This register contains Bits[79:64] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15:0	0000h RW	Source Port Identity 2 (SPI2): This field indicates bits [79:64] of sourcePortIdentity of PTP node.

11.2.332 MAC_LOG_MESSAGE_INTERVAL — Offset BD0h

This register contains the periodic intervals for automatic PTP packet generation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	Log Min Pdelay_Req Interval (LMPDRI): This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
10:8	0h RW	<p>DRSYNCR: Delay_Req to SYNC Ratio In Agent mode, it is used for controlling frequency of Delay_Req messages transmitted. - 0: DelayReq generated for every received SYNC - 1: DelayReq generated every alternate reception of SYNC - 2: for every 4 SYNC messages - 3: for every 8 SYNC messages - 4: for every 16 SYNC messages - 5: for every 32 SYNC messages - 6-7: Reserved The host sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the agent. The Ethernet Controller Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Agent mode, the host must not write/update this register unless it has to override the received value. In Host mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. 0x0 (SYNC1): DelayReq generated for every received SYNC. 0x1 (SYNC2): DelayReq generated every alternate reception of SYNC. 0x2 (SYNC4): for every 4 SYNC messages. 0x3 (SYNC8): for every 8 SYNC messages. 0x4 (SYNC16): for every 16 SYNC messages. 0x5 (SYNC32): for every 32 SYNC messages. 0x6 (RSVD): Reserved.</p>
7:0	00h RW	<p>LSI: Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Host. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.</p>

11.2.333 MTL_OPERATION_MODE — Offset C00h

The Operation Mode register establishes the Transmit and Receive operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9	0h RW	<p>Counters Reset (CNTCLR): When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.</p>
8	0h RW	<p>Counters Preset (CNTPRST): When this bit is set,</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.</p>
7	0h RO	Reserved
6:5	0h RW	Tx Scheduling Algorithm (SCHALG): This field indicates the algorithm for Tx scheduling: 0x0 (WRR): WRR algorithm. 0x1 (WFQ): WFQ algorithm when DCB feature is selected. Otherwise, Reserved. 0x2 (DWRR): DWRR algorithm when DCB feature is selected. Otherwise, Reserved. 0x3 (SP): Strict priority algorithm.
4:3	0h RO	Reserved
2	0h RW	Receive Arbitration Algorithm (RAA): This field is used to select the arbitration algorithm for the Rx side. <ul style="list-style-type: none"> - 0: Strict priority (SP) <p>Queue 0 has the lowest priority and the last queue has the highest priority. <ul style="list-style-type: none"> - 1: Weighted Strict Priority (WSP) 0x0 (SP): Strict priority (SP). 0x1 (WSP): Weighted Strict Priority (WSP). </p>
1	0h RW	Drop Transmit Status (DTXSTS): When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. 0x0 (DISABLE): Drop Transmit Status is disabled. 0x1 (ENABLE): Drop Transmit Status is enabled.
0	0h RO	Reserved

11.2.334 MTL_DBG_CTL — Offset C08h

The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved
18:17	0h RW	ECC Inject Error Control for Tx, Rx and TSO memories (EIEC): When EIEC bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
16	0h RW	ECC Inject Error Enable for Tx, Rx and TSO memories (EIEE): When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Tx, Rx and TSO memories is disabled. 0x1 (ENABLE): ECC Inject Error for Tx, Rx and TSO memories is enabled.
15	0h RW	Transmit Status Available Interrupt Status Enable (STSIE): When this bit is set, an interrupt is generated when Transmit status is available in agent mode. 0x0 (DISABLE): Transmit Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Transmit Packet Available Interrupt Status is enabled.
14	0h RW	Receive Packet Available Interrupt Status Enable (PKTIE): When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. 0x0 (DISABLE): Receive Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Receive Packet Available Interrupt Status is enabled.
13:12	0h RW	FIFO Selected for Access (FIFOSEL): This field indicates the FIFO selected for debug access: 0x0 (TXFIFO): Tx FIFO. 0x1 (TXSTS FIFO): Tx Status FIFO (only read access when SLVMOD is set). 0x2 (TSOFIFO): TSO FIFO (cannot be accessed when SLVMOD is set). 0x3 (RXFIFO): Rx FIFO.
11	0h RW	FIFO Write Enable (FIFOWREN): When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Write is disabled. 0x1 (ENABLE): FIFO Write is enabled.
10	0h RW	FIFO Read Enable (FIFORDEN): When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Read is disabled. 0x1 (ENABLE): FIFO Read is enabled.
9	0h RW	Reset Pointers of Selected FIFO (RSTSEL): When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset Pointers of Selected FIFO is disabled. 0x1 (ENABLE): Reset Pointers of Selected FIFO is enabled.
8	0h RW	Reset All Pointers (RSTALL): When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset All Pointers is disabled. 0x1 (ENABLE): Reset All Pointers is enabled.
7	0h RO	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	Encoded Packet State (PKTSTATE): This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
4	0h RO	Reserved
3:2	0h RW	Byte Enables (BYTEEN): This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
1	0h RW	Debug Mode Access to FIFO (DBGMOD): When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: - Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO - Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is agent access bypassing the DMA. In this mode, the following access are allowed: - Write access to the Tx FIFO - Read access to the Rx FIFO and Tx Status FIFO 0x0 (DISABLE): Debug Mode Access to FIFO is disabled. 0x1 (ENABLE): Debug Mode Access to FIFO is enabled.
0	0h RW	FIFO Debug Access Enable (FDBGEN): When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a host interface. 0x0 (DISABLE): FIFO Debug Access is disabled. 0x1 (ENABLE): FIFO Debug Access is enabled.

11.2.335, MTL_DBG_STS – Offset C0Ch

The FIFO Debug Status register contains the status of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0Ch	00000018h

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RO/V	<p>Remaining Locations in the FIFO (LOCR): Agent Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively.</p>
14:10	0h RO	Reserved
9	0h RW	<p>Transmit Status Available Interrupt Status (STSI): When set, this bit indicates that the Agent mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Transmit Status Available Interrupt Status not detected. 0x1 (ACTIVE): Transmit Status Available Interrupt Status detected.</p>
8	0h RW	<p>Receive Packet Available Interrupt Status (PKTI): When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Receive Packet Available Interrupt Status not detected. 0x1 (ACTIVE): Receive Packet Available Interrupt Status detected.</p>
7:5	0h RO	Reserved
4:3	3h RO/V	<p>Byte Enables (BYTEEN): This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.</p>
2:1	0h RO/V	<p>Encoded Packet State (PKTSTATE): This field is used to get the control or status information of the selected FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.</p>
0	0h RO/V	<p>FIFO Busy (FIFOBUSY): When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: - All other fields of this register - All fields of the MTL_FIFO_Debug_Data register 0x0 (INACTIVE): FIFO Busy not detected. 0x1 (ACTIVE): FIFO Busy detected.</p>

11.2.336 MTL_FIFO_DEBUG_DATA – Offset C10h

The FIFO Debug Data register contains the data to be written to or read from the FIFOs.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	FIFO Debug Data (FDBGDATA): During debug or agent access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or agent access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

11.2.337 MTL_INTERRUPT_STATUS – Offset C20h

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved
18	0h RO/V	EST (TAS- 802.1Qbv) Interrupt Status (ESTIS): This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt. 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected. 0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected.
17	0h RO/V	Debug Interrupt status (DBGIS): This bit indicates an interrupt event during the agent access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Debug Interrupt status not detected. 0x1 (ACTIVE): Debug Interrupt status detected.
16:6	0h RO	Reserved
5	0h RO/V	Queue 5 Interrupt status (Q5IS): This bit indicates that there is an interrupt from Queue 5. To reset this bit, the application must read the MTL_Q5_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 5 Interrupt status not detected. 0x1 (ACTIVE): Queue 5 Interrupt status detected.
4	0h RO/V	Queue 4 Interrupt status (Q4IS): This bit indicates that there is an interrupt from Queue 4. To reset this bit, the application must read the MTL_Q4_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 4 Interrupt status not detected. 0x1 (ACTIVE): Queue 4 Interrupt status detected.

continued...

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	Queue 3 Interrupt status (Q3IS): This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 3 Interrupt status not detected. 0x1 (ACTIVE): Queue 3 Interrupt status detected.
2	0h RO/V	Queue 2 Interrupt status (Q2IS): This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 2 Interrupt status not detected. 0x1 (ACTIVE): Queue 2 Interrupt status detected.
1	0h RO/V	Queue 1 Interrupt status (Q1IS): This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 1 Interrupt status not detected. 0x1 (ACTIVE): Queue 1 Interrupt status detected.
0	0h RO/V	Queue 0 Interrupt status (Q0IS): This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 0 Interrupt status not detected. 0x1 (ACTIVE): Queue 0 Interrupt status detected.

11.2.338 MTL_RXQ_DMA_MAP0 — Offset C30h

The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RW	Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection (Q3DDMACH): When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]). 0x0 (DISABLE): Queue 3 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 3 enabled for DA-based DMA Channel Selection.
27	0h RO	Reserved
26:24	0h RW	Queue 3 Mapped to DMA Channel (Q3MDMACH): This field controls the routing of the received packet in Queue 3 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 <p>This field is valid when the Q3DDMACH field is reset.</p> <p>Note: The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved</p>
23:21	0h RO	Reserved
20	0h RW	<p>Queue 2 Enabled for DA-based DMA Channel Selection (Q2DDMACH):</p> <p>When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address.</p> <p>When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]).</p> <p>0x0 (DISABLE): Queue 2 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 2 enabled for DA-based DMA Channel Selection.</p>
19	0h RO	Reserved
18:16	0h RW	<p>Queue 2 Mapped to DMA Channel (Q2MDMACH):</p> <p>This field controls the routing of the received packet in Queue 2 to the DMA channel:</p> <ul style="list-style-type: none"> - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 <p>This field is valid when the Q2DDMACH field is reset.</p>
15:13	0h RO	Reserved
12	0h RW	<p>Queue 1 Enabled for DA-based DMA Channel Selection (Q1DDMACH):</p> <p>When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address.</p> <p>When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]).</p> <p>0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection.</p>
11	0h RO	Reserved
10:8	0h RW	<p>Queue 1 Mapped to DMA Channel (Q1MDMACH):</p> <p>This field controls the routing of the received packet in Queue 1 to the DMA channel:</p> <ul style="list-style-type: none"> - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 <p>This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.</p>
7:5	0h RO	Reserved
4	0h RW	<p>Queue 0 Enabled for DA-based DMA Channel Selection (Q0DDMACH): When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field. 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection.</p>
3	0h RO	Reserved
2:0	0h RW	<p>Queue 0 Mapped to DMA Channel (Q0MDMACH): This field controls the routing of the packet received in Queue 0 to the DMA channel:</p> <ul style="list-style-type: none"> - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 <p>This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.</p>

11.2.339 MTL_RXQ_DMA_MAP1 — Offset C34h

The Receive Queue and DMA Channel Mapping 1 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved
12	0h RW	<p>Queue 5 Enabled for DA-based DMA Channel Selection (Q5DDMACH): When set, this bit indicates that the packets received in Queue 5 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When reset, this bit indicates that the packets received in Queue 5 are routed to the DMA Channel programmed in the Q5MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
11	0h RO	Reserved
10:8	0h RW	Queue 5 Mapped to DMA Channel (Q5MDMACH): This field controls the routing of the packets received in Queue 5 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q5DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	Reserved
4	0h RW	Queue 4 Enabled for DA-based DMA Channel Selection (Q4DDMACH): When set, this bit indicates that the packets received in Queue 4 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 4 are routed to the DMA Channel programmed in the Q4MDMACH field. 0x0 (DISABLE): Queue 4 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 4 enabled for DA-based DMA Channel Selection.
3	0h RO	Reserved
2:0	0h RW	Queue 4 Mapped to DMA Channel (Q4MDMACH): This field controls the routing of the packet received in Queue 4 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q4DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

11.2.340 MTL_TBS_CTRL — Offset C40h

This register controls the operation of Time Based Scheduling.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	Launch Expiry Offset (LEOS): The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	Reserved
6:4	0h RW	Launch Expiry GSN Offset (LEGOS): The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.
3:2	0h RO	Reserved
1	0h RW	Launch Expiry Offset Valid (LEOV): When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time. 0x0 (INVALID): LEOS field is invalid. 0x1 (VALID): LEOS field is valid.
0	0h RW	EST offset Mode (ESTM): When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8]. 0x0 (DISABLE): EST offset Mode is disabled. 0x1 (ENABLE): EST offset Mode is enabled.

11.2.341 MTL_EST_CONTROL – Offset C50h

This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	PTP Time Offset Value (PTOV): The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23:12	000h RW	Current Time Offset Value (CTOV): Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).
11	0h RO	Reserved
10:8	0h	Time Interval Left Shift Amount (TILS):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	<p>This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists.</p> <ul style="list-style-type: none"> - 000: No left shift needed (equal to x1ns) - 001: Left shift TI by 1 bit (equal to x2ns) - 010: Left shift TI by 2 bits (equal to x4ns) - . - . - 100: Left shift TI by 7 bits (equal to x128ns) <p>Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.</p>
7:6	0h RW	<p>Loop Count to report Scheduling Error (LCSE):</p> <p>Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register.</p> <p>0x0 (M_4_ITERNs): 4 iterations. 0x1 (M_8_ITERNs): 8 iterations. 0x2 (M_16_ITERNs): 16 iterations. 0x3 (M_32_ITERNs): 32 iterations.</p>
5	0h RW	<p>Drop Frames causing Scheduling Error (DFBS):</p> <p>When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped.</p> <p>0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error. 0x1 (DROP): Drop Frames causing Scheduling Error.</p>
4	0h RW	<p>Do not Drop frames during Frame Size Error (DDBF):</p> <p>When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register).</p> <p>0x0 (DROP): Drop frames during Frame Size Error. 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error.</p>
3:2	0h RO	Reserved
1	0h RW	<p>Switch to S/W owned list (SSWL):</p> <p>When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Switch to S/W owned list is disabled. 0x1 (ENABLE): Switch to S/W owned list is enabled.</p>
0	0h RW	<p>Enable EST (EEST):</p> <p>When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit is set.</p> <p>If any uncorrectable error is detected in the EST memory the hardware resets this bit and disables the EST function.</p> <p>0x0 (DISABLE): EST is disabled. 0x1 (ENABLE): EST is enabled.</p>

11.2.342 MTL_EST_STATUS – Offset C58h

This register provides Status related to Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C58h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	Current GCL Slot Number (CGSN): Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:12	0h RO	Reserved
11:8	0h RO/V	BTR Error Loop Count (BTRE): Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "1111111" indicates the iterations exceeded the value of 128 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	0h RO/V	S/W owned list (SWOL): When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default. 0x0 (INACTIVE): Gate control list number "0" is owned by software. 0x1 (ACTIVE): Gate control list number "1" is owned by software.
6:5	0h RO	Reserved
4	0h RW	Constant Gate Control Error (CGCE): This error occurs when the list length (LLR) is 1 and the Cycle Time (CTR) is less than or equal to the programmed Time Interval (TI) value after the optional Left Shifting. The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Constant Gate Control Error not detected. 0x1 (ACTIVE): Constant Gate Control Error detected.
3	0h RO/V	Head-Of-Line Blocking due to Scheduling (HLBS): Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected.
2	0h RO/V	Head-Of-Line Blocking due to Frame Size (HLBF): Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected.
1	0h RW	<p>BTR Error (BTRE): When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "11111111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "11111111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): BTR Error not detected. 0x1 (ACTIVE): BTR Error detected.</p>
0	0h RW	<p>Switch to S/W owned list Complete (SWLC): When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Switch to S/W owned list Complete not detected. 0x1 (ACTIVE): Switch to S/W owned list Complete detected.</p>

11.2.343 MTL_EST_SCH_ERROR — Offset C60h

This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3:0	00h RW	<p>Schedule Error Queue Number (SEQN): The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p>

11.2.344 MTL_EST_FRM_SIZE_ERROR — Offset C64h

This register provides the One Hot encoded Queue Numbers that are having the Frame Size related error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3:0	00h RW	Frame Size Error Queue Number (FEQN):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

11.2.345 MTL_EST_FRM_SIZE_CAPTURE — Offset C68h

This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RO/V	Queue Number of HLBF (HBFQ): Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	0h RO	Reserved
14:0	0000h RO/V	Frame Size of HLBF (HBFS): Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

11.2.346 MTL_EST_INTR_ENABLE — Offset C70h

This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved
4	0h RW	Interrupt Enable for CGCE (CGCE): When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt 0x0 (DISABLE): Interrupt for CGCE is disabled. 0x1 (ENABLE): Interrupt for CGCE is enabled.
3	0h	Interrupt Enable for HLBS (IEHS):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBS is disabled. 0x1 (ENABLE): Interrupt for HLBS is enabled.
2	0h RW	Interrupt Enable for HLBF (IEHF): When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBF is disabled. 0x1 (ENABLE): Interrupt for HLBF is enabled.
1	0h RW	Interrupt Enable for BTR Error (IEBE): When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for BTR Error is disabled. 0x1 (ENABLE): Interrupt for BTR Error is enabled.
0	0h RW	Interrupt Enable for Switch List (IECC): When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for Switch List is disabled. 0x1 (ENABLE): Interrupt for Switch List is enabled.

11.2.347 MTL_EST_GCL_CONTROL — Offset C80h

This register provides the control information for reading/writing to the Gate Control lists.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:22	0h RW	ECC Inject Error Control for EST Memory (ESTEIEC): When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
21	0h RW	EST ECC Inject Error Enable (ESTEIEE): When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): EST ECC Inject Error is disabled. 0x1 (ENABLE): EST ECC Inject Error is enabled.
20	0h RW	ERR0 DWC_ETHER_QOS (ERR0): When set indicates the last write operation was aborted as software writes to GCL and GCL registers is prohibited when SSWL bit of MTL_EST_Control Register is set. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
19:17	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
16:8	000h RW	<p>Gate Control List Address: (GCLA when GCRR is "0"). (ADDR): Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB.</p> <p>Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares.</p> <ul style="list-style-type: none"> - 000: BTR Low (31:0) - 001: BTR High (63:31) - 010: CTR Low (31:0) - 011: CTR High (39:32) - 100: TER (31:0) - 101: LLR (n:0) (where n is $\log\{512\} / \log 2$) - Others: Reserved
7:6	0h RO	Reserved
5	0h RW	<p>Debug Mode Bank Select (DBGB): When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used.</p> <p>0x0 (BANK0): R/W in debug mode should be directed to Bank 0. 0x1 (BANK1): R/W in debug mode should be directed to Bank 1.</p>
4	0h RW	<p>Debug Mode (DBGM): When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use.</p> <p>0x0 (DISABLE): Debug Mode is disabled. 0x1 (ENABLE): Debug Mode is enabled.</p>
3	0h RO	Reserved
2	0h RW	<p>Gate Control Related Registers (GCRR): When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA.</p> <p>0x0 (DISABLE): Gate Control Related Registers are disabled. 0x1 (ENABLE): Gate Control Related Registers are enabled.</p>
1	0h RW	<p>Read '1', Write '0': (R1W0): When set to '1': Read Operation When set to '0': Write Operation. 0x0 (WRITE): Write Operation. 0x1 (READ): Read Operation.</p>
0	0h RW	<p>Start Read/Write Op (SRWO): When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Start Read/Write Op disabled.</p>

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ENABLE): Start Read/Write Op enabled.

11.2.348 MTL_EST_GCL_DATA – Offset C84h

This register holds the read data or write data in case of reads and writes respectively.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	Gate Control Data (GCD): The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

11.2.349 MTL_FPE_CTRL_STS – Offset C90h

This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RO/V	HRS: Hold/Release Status - 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. - 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State.
27:12	0h RO	Reserved
11:8	00h RW	Preemption Classification (PEC): When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	0h RO	Reserved
1:0	0h RW	Additional Fragment Size (AFSZ): used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes

11.2.350 MTL_FPE_ADVANCE — Offset C94h

This register holds the Hold and Release Advance time.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	Release Advance (RADV): The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.
15:0	0000h RW	Hold Advance (HADV): The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

11.2.351 MTL_ECC_CONTROL — Offset CC0h

The MTL_ECC_Control register establishes the operating mode of ECC related to MTL memories.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RW	MTL ECC Error Address Status Over-ride (MEEAO): When set, the following error address fields hold the last valid address where the error is detected. When reset, the following error address fields hold the first address where the error is detected. EUEAS/ECEAS of MTL_ECC_Err_Addr_Status register. 0x0 (DISABLE): MTL ECC Error Address Status Over-ride is disabled. 0x1 (ENABLE): MTL ECC Error Address Status Over-ride is enabled.
7:5	0h RO	Reserved
4	0h RW	TSO memory ECC Enable (TSOEE): When set to 1, enables the ECC feature for TSO memory in DMA. When set to zero, disables the ECC feature for TSO memory in DMA. 0x0 (DISABLE): TSO memory ECC is disabled. 0x1 (ENABLE): TSO memory ECC is enabled.
3	0h RW	MTL Rx Parser ECC Enable (MRXPEE): When set to 1, enables the ECC feature for Rx Parser memory. When set to zero, disables the ECC feature for Rx Parser memory. 0x0 (DISABLE): MTL Rx Parser ECC is disabled. 0x1 (ENABLE): MTL Rx Parser ECC is enabled.
2	0h RW	MTL EST ECC Enable (MESTEE): When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory. 0x0 (DISABLE): MTL EST ECC is disabled.

continued...

Bit Range		Default & Access	Field Name (ID): Description
			0x1 (ENABLE): MTL EST ECC is enabled.
1	0h RW	MTL Rx FIFO ECC Enable (MRXEE): When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory. 0x0 (DISABLE): MTL Rx FIFO ECC is disabled. 0x1 (ENABLE): MTL Rx FIFO ECC is enabled.	
0	0h RW	MTL Tx FIFO ECC Enable (MTXEE): When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory. 0x0 (DISABLE): MTL Tx FIFO ECC is disabled. 0x1 (ENABLE): MTL Tx FIFO ECC is enabled.	

11.2.352 MTL_SAFETY_INTERRUPT_STATUS – Offset CC4h

The MTL_Safety Interrupt_Status registers provides Safety interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved
1	0h RO/V	MTL ECC Uncorrectable error Interrupt Status (MEUIS): This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Uncorrectable error Interrupt Status detected.
0	0h RO/V	MTL ECC Correctable error Interrupt Status (MECIS): This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Correctable error Interrupt Status detected.

11.2.353 MTL_ECC_INTERRUPT_ENABLE – Offset CC8h

The MTL_ECC_Interrupt_Enable register provides enable bits for the ECC interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved
8	0h RW	EST memory Correctable Error Interrupt Enable (ECEIE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): EST memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): EST memory Correctable Error Interrupt is enabled.
7:5	0h RO	Reserved
4	0h RW	Rx memory Correctable Error Interrupt Enable (RXCEIE): When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx memory Correctable Error Interrupt is enabled.
3:1	0h RO	Reserved
0	0h RW	Tx memory Correctable Error Interrupt Enable (TXCEIE): When set, generates an interrupt when a correctable error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Tx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Tx memory Correctable Error Interrupt is enabled.

11.2.354 MTL_ECC_INTERRUPT_STATUS – Offset CCCh

The MTL_ECC Interrupt_Status register provides MTL ECC Interrupt Status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved
10	0h RW	MTL EST memory Uncorrectable Error Status (EUES): When set, indicates that an uncorrectable error is detected at MTL EST memory interface. 0x0 (INACTIVE): MTL EST memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Uncorrectable Error Status detected.
9	0h RW	MTL EST memory Address Mismatch Status (EAMS): This bit when set indicates that address mismatch is found for address bus of MTL EST memory. 0x0 (INACTIVE): MTL EST memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL EST memory Address Mismatch Status detected.
8	0h RW	MTL EST memory Correctable Error Status (ECES): This bit when set indicates that correctable error is detected at the MTL EST memory. 0x0 (INACTIVE): MTL EST memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Correctable Error Status detected.
7	0h RO	Reserved
6	0h	MTL Rx memory Uncorrectable Error Status (RXUES):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface. 0x0 (INACTIVE): MTL Rx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory Uncorrectable Error Status detected.
5	0h RW	MTL Rx memory Address Mismatch Status (RXAMS): This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx memory Address Mismatch Status detected.
4	0h RW	MTL Rx memory Correctable Error Status (RXCES): This bit when set indicates that correctable error is detected at the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory correctable Error Status detected.
3	0h RO	Reserved
2	0h RW	MTL Tx memory Uncorrectable Error Status (TXUES): When set, indicates that an uncorrectable error is detected at the MTL TX memory interface. 0x0 (INACTIVE): MTL Tx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Uncorrectable Error Status detected.
1	0h RW	MTL Tx memory Address Mismatch Status (TXAMS): This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Tx memory Address Mismatch Status detected.
0	0h RW	MTL Tx memory Correctable Error Status (TXCES): This bit when set indicates that a correctable error is detected at the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Correctable Error Status detected.

11.2.355 MTL_ECC_ERR_STS_RCTL — Offset CD0h

The MTL_ECC_Err_Sts_Rctl register establishes the control for ECC Error status capture.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved
5	0h RW	Clear Uncorrectable Error Status (CUES): When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Uncorrectable Error Status not detected. 0x1 (ACTIVE): Clear Uncorrectable Error Status detected.
4	0h RW	Clear Correctable Error Status (CCES): When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values are cleared upon reading.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Correctable Error Status not detected. 0x1 (ACTIVE): Clear Correctable Error Status detected.
3:1	0h RW	MTL ECC Memory Selection (EMS): When EESRE bit of this register is set, this field indicates which memory's error status value to be read. The memory selection encoding is as described below. 0x0 (TX_MEM): MTL Tx memory. 0x1 (RX_MEM): MTL Rx memory. 0x2 (EST_MEM): MTL EST memory. 0x3 (RXP_MEM): MTL Rx Parser memory. 0x4 (TSO_MEM): DMA TSO memory.
0	0h RW	MTL ECC Error Status Read Enable (EESRE): When this bit is set, based on the EMS field of this register, the respective memory's error status values are captured as described: - The correctable and uncorrectable error count values are captured into MTL_ECC_Err_Cnt_Status register - The address location's of correctable and uncorrectable errors are captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers. 0x0 (DISABLE): MTL ECC Error Status Read is disabled. 0x1 (ENABLE): MTL ECC Error Status Read is enabled.

11.2.356 MTL_ECC_ERR_ADDR_STATUS – Offset CD4h

The MTL_ECC_Err_Addr_Status register provides the memory addresses for the correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	MTL ECC Uncorrectable Error Address Status (EUEAS): Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected.
15:0	0000h RO/V	MTL ECC Correctable Error Address Status (ECEAS): Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected.

11.2.357 MTL_ECC_ERR_CNTR_STATUS – Offset CD8h

The MTL_ECC_Err_Cntr_Status register provides ECC Error count for Correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	MTL ECC Uncorrectable Error Counter Status (EUECS): Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's uncorrectable error count value.
15:8	0h RO	Reserved
7:0	00h RO/V	MTL ECC Correctable Error Counter Status (ECECS): Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value.

11.2.358 MTL_DPP_CONTROL – Offset CE0h

The MTL_DPP_Control establishes the operating mode of Data Parity protection and error injection.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CE0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved
13	0h RW	Insert Parity error in CSR Read data parity generator (IPECW): When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in AXI Agent Interface Data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in CSR Read data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in CSR Read data parity generator is enabled.
12	0h RW	Insert Parity error in AXI Agent Write data parity generator (IPEASW): When set to 1, parity bit of first valid data generated by the AXI parity generator is (or at PG9 as shown in AXI agent Interface Data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in AXI Agent Write data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in AXI Agent Write data parity generator is enabled.
11	0h RW	Insert Parity error in Rx write-back Descriptor parity generator (IPERD): When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Receive data path parity protection diagram) is flipped. 0x0 (DISABLE): Insert Parity error in Rx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Rx write-back Descriptor parity generator is enabled.
10	0h RW	Insert Parity error in Tx write-back Descriptor parity generator (IPETD): When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in Tx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Tx write-back Descriptor parity generator is enabled.

continued...

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	Insert Parity Error in DMA TSO parity generator (IPETSO): When set to 1, parity bit of first valid data generated by the DMA TSO parity generator is (or at PG3 as shown in Transmit data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA TSO parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA TSO parity generator is enabled.
8	0h RW	Insert Parity Error in DMA DTX Control word parity generator (IPEDDC): When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA DTX Control word parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA DTX Control word parity generator is enabled.
7	0h RW	Insert Parity Error in MTL Rx FIFO read control parity generator (IPEMRF): When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Receive data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is enabled.
6	0h RW	Insert Parity Error in MTL Tx Status parity generator (IPEMTS): When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Tx Status parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Tx Status parity generator is enabled.
5	0h RW	Insert Parity Error in MTL checksum parity generator (IPEMC): When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL checksum parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL checksum parity generator is enabled.
4:3	0h RO	Reserved
2	0h RW	EPSI DWC_ETHER_QOS (EPSI): Enable Parity on Agent Interface port when set to 1, enables the parity check for the agent interface ports and disables the internal generation of parity for the input agent data port. When set to 0, disables the parity check for the agent interface ports and enables the internal parity generation for the input agent data port.
1	0h RW	Odd Parity Enable (OPE): When set to 1, enables odd parity protection on all the external interfaces and when set to 0, enables even parity protection on all the external interfaces. 0x0 (DISABLE): Odd Parity is disabled. 0x1 (ENABLE): Odd Parity is enabled.
0	0h RW	Enable Data path Parity Protection (EDPP): When set to 1, enables the parity protection for EQOS datapath by generating and checking the parity on EQOS datapath. When set to 0, disables the parity protection for EQOS datapath. 0x0 (DISABLE): Data path Parity Protection is disabled. 0x1 (ENABLE): Data path Parity Protection is enabled.

11.2.359 MTL_TXQ0_OPERATION_MODE — Offset D00h

The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21:16	00h RW	<p>Transmit Queue Size (TQS): This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes.</p> <p>When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value.</p> <p>The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits:</p> $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3 \text{ bits}$
15:7	0h RO	Reserved
6:4	0h RW	<p>TTC DWC_ETHER_QOS (TTC): Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.</p>
3:2	0h RW	<p>Transmit Queue Enable (TXQEN): This field is used to enable/disable the transmit queue 0.</p> <ul style="list-style-type: none"> - 2'b00: Not enabled - 2'b01: Reserved - 2'b10: Enabled - 2'b11: Reserved <p>This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations.</p> <p>Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.</p> <p>0x0 (DISABLE): Not enabled.</p> <p>0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV).</p> <p>0x2 (ENABLE): Enabled.</p> <p>0x3 (RSVD2): Reserved.</p>
1	0h RW	<p>Transmit Store and Forward (TSF): When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.</p> <p>0x0 (DISABLE): Transmit Store and Forward is disabled.</p> <p>0x1 (ENABLE): Transmit Store and Forward is enabled.</p> <p>Note: This bit should always be set as we do not support cut through mode.</p>
0	0h RW	<p>Flush Transmit Queue (FTQ): When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Flush Transmit Queue is disabled.</p> <p>0x1 (ENABLE): Flush Transmit Queue is enabled.</p>

11.2.360 MTL_TXQ0_UNDERFLOW — Offset D04h

The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D04h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11	0h RO/V	<p>Overflow Bit for Underflow Packet Counter (UFCNTOVF): This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter.</p> <p>0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.</p>
10:0	000h RO/V	<p>Underflow Packet Counter (UFFRMCNT): This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

11.2.361 MTL_TXQ0_DEBUG — Offset D08h

The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D08h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:20	0h RO/V	<p>Number of Status Words in Tx Status FIFO of Queue (STXSTS): This field indicates the current number of status in the Tx Status FIFO of this queue.</p> <p>When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.</p>
19	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
18:16	0h RO/V	Number of Packets in the Transmit Queue (PTXQ): This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	Reserved
5	0h RO/V	MTL Tx Status FIFO Full Status (TXSTSFSTS): When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO/V	MTL Tx Queue Not Empty Status (TXQSTS): When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO/V	MTL Tx Queue Write Controller Status (TWCSTS): When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO/V	MTL Tx Queue Read Controller Status (TRCSTS): This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO/V	Transmit Queue in Pause (TXQPAUSED): When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

11.2.362 MTL_TXQ0_ETS_STATUS — Offset D14h

The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:0	000000h RO/V	Average Bits per Slot (ABS): This field contains the average transmitted bits per slot.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

11.2.363 MTL_TXQ0_QUANTUM_WEIGHT — Offset D18h

The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved
20:0	000000h RW	<p>Quantum or Weights (ISCQW): When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes.</p> <p>When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth.</p> <p>When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.</p>

11.2.364 MTL_Q0_INTERRUPT_CONTROL_STATUS — Offset D2Ch

This register contains the interrupt enable and status bits for the queue 0 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RW	<p>Receive Queue Overflow Interrupt Enable (RXOIE): When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.</p> <p>0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.</p>
23:17	0h RO	Reserved
16	0h	Receive Queue Overflow Interrupt Status (RXOVFIS):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	Reserved
9	0h RW	Average Bits Per Slot Interrupt Enable (ABPSIE): When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	Transmit Queue Underflow Interrupt Enable (TXUIE): When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RW	Reserved
1	0h RW	Average Bits Per Slot Interrupt Status (ABPSIS): When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	Transmit Queue Underflow Interrupt Status (TXUNFIS): This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

11.2.365 MTL_RXQ0_OPERATION_MODE – Offset D30h

The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved
26:20	00h RW	<p>Receive Queue Size (RQS): This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes.</p> <p>When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value.</p> <p>The width of this field depends on the Rx memory size selected in your configuration.</p> <p>For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3$ bits</p>
19:14	00h RW	<p>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD): These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:</p> <ul style="list-style-type: none"> - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB <p>The de-assertion is effective only after flow control is asserted.</p> <p>Note: The value must be programmed in such a way to make sure that the threshold is a positive number.</p> <p>When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB.</p> <p>For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register.</p> <p>The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.</p>
13:8	00h RW	<p>Threshold for Activating Flow Control (in half-duplex and full-duplex) (RFA): These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.</p>
7	0h RW	<p>Enable Hardware Flow Control (EHFC): When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.</p> <p>0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.</p>
6	0h RW	<p>Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF): When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC.</p> <p>When this bit is reset, all error packets are dropped if the FEP bit is reset.</p> <p>0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.</p>
5	0h RW	<p>Receive Queue Store and Forward (RSF):</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set, the Ethernet Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.</p> <p>0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.</p>
4	0h RW	<p>Forward Error Packets (FEP): When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped.</p> <p>When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA.</p> <p>0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.</p>
3	0h RW	<p>Forward Undersized Good Packets (FUP): When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.</p> <p>0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.</p>
2	0h RO	Reserved
1:0	0h RW	<p>Receive Queue Threshold Control (RTC): These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred.</p> <p>This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.</p> <p>0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.</p>

11.2.366 MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT — Offset D34h

The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D34h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	<p>Missed Packet Counter Overflow Bit (MISCNTOVF): When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit.</p> <p style="text-align: right;"><i>continued...</i></p>

Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO/V	Missed Packet Counter (MISPKTCNT): This field indicates the number of packets missed by the Ethernet Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	Reserved
11	0h RO/V	Overflow Counter Overflow Bit (OVFCNTOVF): When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO/V	Overflow Packet Counter (OVFPKTCNT): This field indicates the number of packets discarded by the Ethernet Controller because of Receive queue overflow. This counter is incremented each time the Ethernet Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.367 MTL_RXQ0_DEBUG — Offset D38h

The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D38h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:16	0000h RO/V	Number of Packets in Receive Queue (PRXQ): This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	0h RO	Reserved
5:4	0h RO/V	MTL Rx Queue Fill-Level Status (RXQSTS): This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THRESHOLD): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THRESHOLD): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
2:1	0h RO/V	MTL Rx Queue Read Controller State (RRCSTS): This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO/V	MTL Rx Queue Write Controller Active Status (RWCSTS): When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

11.2.368 MTL_RXQ0_CONTROL — Offset D3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D3Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	Receive Queue Packet Arbitration (RXQ_FRM_ARBIT): When this bit is set, the Ethernet Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the Ethernet Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	Receive Queue Weight (RXQ_WEGT): This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

11.2.369 MTL_TXQ1_OPERATION_MODE — Offset D40h

The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:16	00h RW	<p>Transmit Queue Size (TQS): This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits</p>
15:7	0h RO	Reserved
6:4	0h RO	Reserved
3:2	0h RW	<p>Transmit Queue Enable (TXQEN): This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.</p>
1	0h RW	<p>Transmit Store and Forward (TSF): When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.</p>
0	0h RW	<p>Flush Transmit Queue (FTQ): When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

11.2.370 MTL_TXQ1_UNDERFLOW — Offset D44h

The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11	0h RO/V	Overflow Bit for Underflow Packet Counter (UFCNTOVF): This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO/V	Underflow Packet Counter (UFFRMCNT): This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.371 MTL_TXQ1_DEBUG — Offset D48h

The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:20	0h RO/V	Number of Status Words in Tx Status FIFO of Queue (STXSTS): This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	Reserved
18:16	0h RO/V	Number of Packets in the Transmit Queue (PTXQ): This field indicates the current number of packets in the Tx Queue.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	Reserved
5	0h RO/V	MTL Tx Status FIFO Full Status (TXSTSFSTS): When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO/V	MTL Tx Queue Not Empty Status (TXQSTS): When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO/V	MTL Tx Queue Write Controller Status (TWCSTS): When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO/V	MTL Tx Queue Read Controller Status (TRCSTS): This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO/V	Transmit Queue in Pause (TXQPAUSED): When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

11.2.372 MTL_TXQ1_ETS_CONTROL — Offset D50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved
6:4	0h RW	Slot Count (SLC): If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	Credit Control (CC): When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	AV Algorithm (AVALG): When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	Reserved

11.2.373 MTL_TXQ1_ETS_STATUS — Offset D54h

The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D54h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:0	000000h RO/V	Average Bits per Slot (ABS): This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

11.2.374 MTL_TXQ1_QUANTUM_WEIGHT — Offset D58h

The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D58h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved
20:0	000000h RW	<p>ISCQW: idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.</p>

11.2.375 MTL_TXQ1_SENDSLOPECREDIT — Offset D5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved
13:0	0000h RW	<p>sendSlopeCredit Value (SSC): When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.</p>

11.2.376 MTL_TXQ1_HICREDIT — Offset D60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D60h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28:0	0000000h RW	hiCredit Value (HC): When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is $131,072 * 1,024 = 134,217,728$ or 0x0800_0000.

11.2.377 MTL_TXQ1_LOCREDIT — Offset D64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D64h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28:0	0000000h RW	loCredit Value (LC): When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then $(8192 * 2) * 8 * 1024 = 134,217,728$ or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

11.2.378 MTL_Q1_INTERRUPT_CONTROL_STATUS — Offset D6Ch

This register contains the interrupt enable and status bits for the queue 1 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D6Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h	Receive Queue Overflow Interrupt Enable (RXOIE):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	Reserved
16	0h RW	Receive Queue Overflow Interrupt Status (RXOVFIS): This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	Reserved
9	0h RW	Average Bits Per Slot Interrupt Enable (ABPSIE): When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	Transmit Queue Underflow Interrupt Enable (TXUIE): When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RO	Reserved
1	0h RW	Average Bits Per Slot Interrupt Status (ABPSIS): When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	Transmit Queue Underflow Interrupt Status (TXUNFIS): This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

11.2.379 MTL_RXQ1_OPERATION_MODE — Offset D70h

The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D70h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:27	0h RO	Reserved	
26:20	00h RW	<p>Receive Queue Size (RQS): This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3$ bits </p>	
19:14	00h RW	<p>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD): These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:</p> <ul style="list-style-type: none"> - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB <p>The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.</p>	
13:8	00h RW	<p>Threshold for Activating Flow Control (in half-duplex and full-duplex) (RFA): These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.</p>	
7	0h RW	<p>Enable Hardware Flow Control (EHFC): When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.</p>	
6	0h RW	<p>Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF): When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.</p>	

continued...

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	Receive Queue Store and Forward (RSF): When this bit is set, the Ethernet Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	Forward Error Packets (FEP): When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	Forward Undersized Good Packets (FUP): When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	Reserved
1:0	0h RW	Receive Queue Threshold Control (RTC): These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

11.2.380 MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT — Offset D74h

The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h	Missed Packet Counter Overflow Bit (MISCNTOVF):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO/V	Missed Packet Counter (MISPKTCNT): This field indicates the number of packets missed by the Ethernet Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	Reserved
11	0h RO/V	Overflow Counter Overflow Bit (OVFCNTOVF): When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO/V	Overflow Packet Counter (OVFPKTCNT): This field indicates the number of packets discarded by the Ethernet Controller because of Receive queue overflow. This counter is incremented each time the Ethernet Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.381 MTL_RXQ1_DEBUG — Offset D78h

The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:16	0000h RO/V	Number of Packets in Receive Queue (PRXQ): This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	0h RO	Reserved
5:4	0h RO/V	MTL Rx Queue Fill-Level Status (RXQSTS): This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.

continued...

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	Reserved
2:1	0h RO/V	MTL Rx Queue Read Controller State (RRCSTS): This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO/V	MTL Rx Queue Write Controller Active Status (RWCSTS): When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

11.2.382 MTL_RXQ1_CONTROL — Offset D7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D7Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	Receive Queue Packet Arbitration (RXQ_FRM_ARBIT): When this bit is set, the Ethernet Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the Ethernet Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	Receive Queue Weight (RXQ_WEGT): This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

11.2.383 MTL_TXQ2_OPERATION_MODE — Offset D80h

The Queue 2 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D80h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:16	00h RW	Transmit Queue Size (TQS): This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3 \text{ bits}$
15:7	0h RO	Reserved
6:4	0h RO	Reserved
3:2	0h RW	Transmit Queue Enable (TXQEN): This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	Transmit Store and Forward (TSF): When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	Flush Transmit Queue (FTQ): When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Flush Transmit Queue is disabled.</p> <p>0x1 (ENABLE): Flush Transmit Queue is enabled.</p>

11.2.384 MTL_TXQ2_UNDERFLOW — Offset D84h

The Queue 2 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11	0h RO/V	<p>Overflow Bit for Underflow Packet Counter (UFCNTOVF): This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter.</p> <p>0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.</p>
10:0	000h RO/V	<p>Underflow Packet Counter (UFFRMCNT): This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

11.2.385 MTL_TXQ2_DEBUG — Offset D88h

The Queue 2 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:20	0h RO/V	<p>Number of Status Words in Tx Status FIFO of Queue (STXSTS): This field indicates the current number of status in the Tx Status FIFO of this queue.</p> <p>When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.</p>
19	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
18:16	0h RO/V	Number of Packets in the Transmit Queue (PTXQ): This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	Reserved
5	0h RO/V	MTL Tx Status FIFO Full Status (TXSTSFSTS): When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO/V	MTL Tx Queue Not Empty Status (TXQSTS): When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO/V	MTL Tx Queue Write Controller Status (TWCSTS): When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO/V	MTL Tx Queue Read Controller Status (TRCSTS): This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO/V	Transmit Queue in Pause (TXQPAUSED): When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

11.2.386 MTL_TXQ2_ETS_CONTROL — Offset D90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved
6:4	0h	Slot Count (SLC):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	Credit Control (CC): When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	AV Algorithm (AVALG): When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	Reserved

11.2.387 MTL_TXQ2_ETS_STATUS — Offset D94h

The Queue 2 ETS Status register provides the average traffic transmitted in Queue 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:0	000000h RO/V	Average Bits per Slot (ABS): This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

11.2.388 MTL_TXQ2_QUANTUM_WEIGHT — Offset D98h

The Queue 2 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D98h	0000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:21	0h RO	Reserved	
20:0	000000h RW	<p>ISCQW: idleSlopeCredit, Quantum or Weights</p> <ul style="list-style-type: none"> - idleSlopeCredit <p>When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero.</p> <ul style="list-style-type: none"> - Quantum <p>When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes.</p> <ul style="list-style-type: none"> - Weights <p>When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero.</p> <p>When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64.</p> <p>Bits [20:7] must be written to zero.</p> <ul style="list-style-type: none"> - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time. 	

11.2.389 MTL_TXQ2_SENDSLOPECREDIT — Offset D9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D9Ch	0000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:14	0h RO	Reserved	
13:0	0000h RW	<p>sendSlopeCredit Value (SSC):</p> <p>When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and</p>	

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

11.2.390 MTL_TXQ2_HIREDIT — Offset DA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DA0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28:0	0000000h RW	hiCredit Value (HC): When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is $131,072 * 1,024 = 134,217,728$ or 0x0800_0000.

11.2.391 MTL_TXQ2_LOREDIT — Offset DA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DA4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28:0	0000000h RW	loCredit Value (LC): When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then $(8192 * 2) * 8 * 1024 = 134,217,728$ or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

11.2.392 MTL_Q2_INTERRUPT_CONTROL_STATUS — Offset DACH

This register contains the interrupt enable and status bits for the queue 2 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DACH	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RW	Receive Queue Overflow Interrupt Enable (RXOIE): When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	Reserved
16	0h RW	Receive Queue Overflow Interrupt Status (RXOVFIS): This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	Reserved
9	0h RW	Average Bits Per Slot Interrupt Enable (ABPSIE): When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	Transmit Queue Underflow Interrupt Enable (TXUIE): When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RO	Reserved
1	0h RW	Average Bits Per Slot Interrupt Status (ABPSIS): When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	Transmit Queue Underflow Interrupt Status (TXUNFIS): This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

11.2.393 MTL_RXQ2_OPERATION_MODE — Offset DB0h

The Queue 2 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved
26:20	00h RW	<p>Receive Queue Size (RQS): This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3$ bits </p>
19:14	00h RW	<p>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD): These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:</p> <ul style="list-style-type: none"> - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB <p>The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.</p>
13:8	00h RW	<p>Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA): These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.</p>
7	0h RW	<p>Enable Hardware Flow Control (EHFC): When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled. </p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF): When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.
5	0h RW	Receive Queue Store and Forward (RSF): When this bit is set, the Ethernet Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	Forward Error Packets (FEP): When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	Forward Undersized Good Packets (FUP): When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	Reserved
1:0	0h RW	Receive Queue Threshold Control (RTC): These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

11.2.394 MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT – Offset DB4h

The Queue 2 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	Missed Packet Counter Overflow Bit (MISCNTOVF): When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO/V	Missed Packet Counter (MISPKTCNT): This field indicates the number of packets missed by the Ethernet Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1'b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	Reserved
11	0h RO/V	Overflow Counter Overflow Bit (OVFCNTOVF): When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO/V	Overflow Packet Counter (OVFPKTCNT): This field indicates the number of packets discarded by the Ethernet Controller because of Receive queue overflow. This counter is incremented each time the Ethernet Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.395 MTL_RXQ2_DEBUG — Offset DB8h

The Queue 2 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:16	0000h RO/V	Number of Packets in Receive Queue (PRXQ): This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	0h RO	Reserved
5:4	0h RO/V	MTL Rx Queue Fill-Level Status (RXQSTS): This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty.

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	Reserved
2:1	0h RO/V	MTL Rx Queue Read Controller State (RRCSTS): This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO/V	MTL Rx Queue Write Controller Active Status (RWCSTS): When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

11.2.396 MTL_RXQ2_CONTROL – Offset DBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DBCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	Receive Queue Packet Arbitration (RXQ_FRM_ARBIT): When this bit is set, the Ethernet Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the Ethernet Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	Receive Queue Weight (RXQ_WEGT): This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

11.2.397 MTL_TXQ3_OPERATION_MODE — Offset DC0h

The Queue 3 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:16	00h RW	Transmit Queue Size (TQS): This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3 \text{ bits}$
15:7	0h RO	Reserved
6:4	0h RO	Reserved
3:2	0h RW	Transmit Queue Enable (TXQEN): This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	Transmit Store and Forward (TSF): When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	Flush Transmit Queue (FTQ): When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission.

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (<code>clk_tx_i</code>) should be active.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Flush Transmit Queue is disabled.</p> <p>0x1 (ENABLE): Flush Transmit Queue is enabled.</p>

11.2.398 MTL_TXQ3_UNDERFLOW — Offset DC4h

The Queue 3 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11	0h RO/V	<p>Overflow Bit for Underflow Packet Counter (UFCNTOVF):</p> <p>This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter.</p> <p>0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.</p>
10:0	000h RO/V	<p>Underflow Packet Counter (UFFRMCNT):</p> <p>This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with <code>mci_be_i[0]</code> at 1'b1.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

11.2.399 MTL_TXQ3_DEBUG — Offset DC8h

The Queue 3 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:20	0h RO/V	<p>Number of Status Words in Tx Status FIFO of Queue (STXSTS):</p> <p>This field indicates the current number of status in the Tx Status FIFO of this queue.</p> <p>When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.</p>
19	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
18:16	0h RO/V	Number of Packets in the Transmit Queue (PTXQ): This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	Reserved
5	0h RO/V	MTL Tx Status FIFO Full Status (TXSTSFSTS): When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO/V	MTL Tx Queue Not Empty Status (TXQSTS): When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO/V	MTL Tx Queue Write Controller Status (TWCSTS): When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO/V	MTL Tx Queue Read Controller Status (TRCSTS): This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO/V	Transmit Queue in Pause (TXQPAUSED): When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

11.2.400 MTL_TXQ3_ETS_CONTROL — Offset DD0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved
6:4	0h	Slot Count (SLC):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	Credit Control (CC): When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	AV Algorithm (AVALG): When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	Reserved

11.2.401 MTL_TXQ3_ETS_STATUS – Offset DD4h

The Queue 3 ETS Status register provides the average traffic transmitted in Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved
23:0	000000h RO/V	Average Bits per Slot (ABS): This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

11.2.402 MTL_TXQ3_QUANTUM_WEIGHT – Offset DD8h

The Queue 3 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved
20:0	000000h RW	<p>ISCQW: idleSlopeCredit, Quantum or Weights - idleSlopeCredit</p> <p>When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero.</p> <p>- Quantum</p> <p>When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes.</p> <p>- Weights</p> <p>When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero.</p> <p>When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64.</p> <p>Bits [20:7] must be written to zero.</p> <p>- Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register.</p> <p>- Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size))</p> <p>- Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.</p>

11.2.403 MTL_TXQ3_SENDSLOPECREDIT — Offset DDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DDCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved
13:0	0000h RW	<p>sendSlopeCredit Value (SSC):</p> <p>When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

11.2.404 MTL_TXQ3_HIREDIT — Offset DE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DE0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28:0	0000000h RW	hiCredit Value (HC): When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is $131,072 * 1,024 = 134,217,728$ or 0x0800_0000.

11.2.405 MTL_TXQ3_LOCREDIT — Offset DE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DE4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28:0	0000000h RW	loCredit Value (LC): When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then $(8192*2) * 8 * 1024 = 134,217,728$ or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

11.2.406 MTL_Q3_INTERRUPT_CONTROL_STATUS — Offset DECh

This register contains the interrupt enable and status bits for the queue 3 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DECh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RW	Receive Queue Overflow Interrupt Enable (RXOIE): When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	Reserved
16	0h RW	Receive Queue Overflow Interrupt Status (RXOVFIS): This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	Reserved
9	0h RW	Average Bits Per Slot Interrupt Enable (ABPSIE): When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	Transmit Queue Underflow Interrupt Enable (TXUIE): When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RW	Reserved
1	0h RW	Average Bits Per Slot Interrupt Status (ABPSIS): When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	Transmit Queue Underflow Interrupt Status (TXUNFIS): This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

11.2.407 MTL_RXQ3_OPERATION_MODE — Offset DF0h

The Queue 3 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved
26:20	00h RW	Receive Queue Size (RQS): This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3$ bits
19:14	00h RW	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD): These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: <ul style="list-style-type: none"> - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA): These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	Enable Hardware Flow Control (EHFC): When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.

continued...

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF): When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.
5	0h RW	Receive Queue Store and Forward (RSF): When this bit is set, the Ethernet Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	Forward Error Packets (FEP): When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	Forward Undersized Good Packets (FUP): When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	Reserved
1:0	0h RW	Receive Queue Threshold Control (RTC): These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

11.2.408 MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT – Offset DF4h

The Queue 3 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	Missed Packet Counter Overflow Bit (MISCNTOVF): When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO/V	Missed Packet Counter (MISPKTCNT): This field indicates the number of packets missed by the Ethernet Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1'b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	Reserved
11	0h RO/V	Overflow Counter Overflow Bit (OVFCNTOVF): When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO/V	Overflow Packet Counter (OVFPKTCNT): This field indicates the number of packets discarded by the Ethernet Controller because of Receive queue overflow. This counter is incremented each time the Ethernet Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.409 MTL_RXQ3_DEBUG — Offset DF8h

The Queue 3 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:16	0000h RO/V	Number of Packets in Receive Queue (PRXQ): This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	0h RO	Reserved
5:4	0h RO/V	MTL Rx Queue Fill-Level Status (RXQSTS): This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (BLW_THRESHOLD): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THRESHOLD): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	Reserved
2:1	0h RO/V	MTL Rx Queue Read Controller State (RRCTS): This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO/V	MTL Rx Queue Write Controller Active Status (RWCTS): When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

11.2.410 MTL_RXQ3_CONTROL — Offset DFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DFCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	Receive Queue Packet Arbitration (RXQ_FRM_ARBIT): When this bit is set, the Ethernet Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the Ethernet Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	Receive Queue Weight (RXQ_WEGT): This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

11.2.411 MTL_Q4_INTERRUPT_CONTROL_STATUS – Offset E2Ch

This register contains the interrupt enable and status bits for the queue 4 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E2Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RW	Receive Queue Overflow Interrupt Enable (RXOIE): When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	Reserved
16	0h RW	Receive Queue Overflow Interrupt Status (RXOVFIS): This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:0	0h RO	Reserved

11.2.412 MTL_RXQ4_OPERATION_MODE – Offset E30h

The Queue 4 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + E30h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved
26:20	00h RW	Receive Queue Size (RQS): This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value.

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Bit Range	Default & Access	Field Name (ID): Description
		<p>The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3$ bits</p>
19:14	00h RW	<p>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD): These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:</p> <ul style="list-style-type: none"> - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB <p>The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number.</p> <p>When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB.</p> <p>For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register.</p> <p>The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.</p>
13:8	00h RW	<p>Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA): These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.</p>
7	0h RW	<p>Enable Hardware Flow Control (EHFC): When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.</p>
6	0h RW	<p>Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF): When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.</p>
5	0h RW	<p>Receive Queue Store and Forward (RSF): When this bit is set, the Ethernet Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.</p>
4	0h RW	<p>Forward Error Packets (FEP): When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	Forward Undersized Good Packets (FUP): When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	Reserved
1:0	0h RW	Receive Queue Threshold Control (RTC): These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

11.2.413 MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT — Offset E34h

The Queue 4 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	Missed Packet Counter Overflow Bit (MISCNTOVF): When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO/V	Missed Packet Counter (MISPKTCNT): This field indicates the number of packets missed by the Ethernet Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	Reserved
11	0h	Overflow Counter Overflow Bit (OVFCNTOVF):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	<p>When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Overflow Counter overflow not detected.</p> <p>0x1 (ACTIVE): Overflow Counter overflow detected.</p>
10:0	000h RO/V	<p>Overflow Packet Counter (OVFPKTCNT):</p> <p>This field indicates the number of packets discarded by the Ethernet Controller because of Receive queue overflow. This counter is incremented each time the Ethernet Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

11.2.414 MTL_RXQ4_DEBUG — Offset E38h

The Queue 4 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E38h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:16	0000h RO/V	<p>Number of Packets in Receive Queue (PRXQ):</p> <p>This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.</p>
15:6	0h RO	Reserved
5:4	0h RO/V	<p>MTL Rx Queue Fill-Level Status (RXQSTS):</p> <p>This field gives the status of the fill-level of the Rx Queue:</p> <p>0x0 (EMPTY): Rx Queue empty.</p> <p>0x1 (BLWTHR): Rx Queue fill-level below flow-control deactivate threshold.</p> <p>0x2 (ABVTHR): Rx Queue fill-level above flow-control activate threshold.</p> <p>0x3 (FULL): Rx Queue full.</p>
3	0h RO	Reserved
2:1	0h RO/V	<p>MTL Rx Queue Read Controller State (RRCSTS):</p> <p>This field gives the state of the Rx queue Read controller:</p> <p>0x0 (IDLE): Idle state.</p> <p>0x1 (READ_DATA): Reading packet data.</p> <p>0x2 (READ_STS): Reading packet status (or timestamp).</p> <p>0x3 (FLUSH): Flushing the packet data and status.</p>
0	0h RO/V	<p>MTL Rx Queue Write Controller Active Status (RWCSTS):</p> <p>When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue.</p> <p>0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected.</p> <p>0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.</p>

11.2.415 MTL_RXQ4_CONTROL – Offset E3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E3Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	Receive Queue Packet Arbitration (RXQ_FRM_ARBIT): When this bit is set, the Ethernet Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the Ethernet Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: <ul style="list-style-type: none"> - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	Receive Queue Weight (RXQ_WEGT): This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

11.2.416 MTL_Q5_INTERRUPT_CONTROL_STATUS – Offset E6Ch

This register contains the interrupt enable and status bits for the queue 5 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E6Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RW	Receive Queue Overflow Interrupt Enable (RXOIE): When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	Receive Queue Overflow Interrupt Status (RXOVFIS): This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	Reserved
9	0h RW	Average Bits Per Slot Interrupt Enable (ABPSIE): When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	Transmit Queue Underflow Interrupt Enable (TXUIE): When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RO	Reserved
1	0h RW	Average Bits Per Slot Interrupt Status (ABPSIS): When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	Transmit Queue Underflow Interrupt Status (TXUNFIS): This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

11.2.417 MTL_RXQ5_OPERATION_MODE — Offset E70h

The Queue 5 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + E70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved
26:20	00h RW	<p>Receive Queue Size (RQS): This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes.</p> <p>When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value.</p> <p>The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits:</p> $\text{LOG2}(2048/256) = \text{LOG2}(8) = 3 \text{ bits}$
19:14	00h RW	<p>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD): These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:</p> <ul style="list-style-type: none"> - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB <p>The de-assertion is effective only after flow control is asserted.</p> <p>Note: The value must be programmed in such a way to make sure that the threshold is a positive number.</p> <p>When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB.</p> <p>For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register.</p> <p>The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.</p>
13:8	00h RW	<p>Threshold for Activating Flow Control (in half-duplex and full-duplex) (RFA): These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.</p>
7	0h RW	<p>Enable Hardware Flow Control (EHFC): When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.</p> <p>0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.</p>
6	0h RW	<p>Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF): When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC.</p> <p>When this bit is reset, all error packets are dropped if the FEP bit is reset.</p> <p>0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.</p>
5	0h RW	<p>Receive Queue Store and Forward (RSF):</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set, the Ethernet Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.</p> <p>0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.</p>
4	0h RW	<p>Forward Error Packets (FEP):</p> <p>When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped.</p> <p>When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA.</p> <p>0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.</p>
3	0h RW	<p>Forward Undersized Good Packets (FUP):</p> <p>When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.</p> <p>0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.</p>
2	0h RO	Reserved
1:0	0h RW	<p>Receive Queue Threshold Control (RTC):</p> <p>These bits control the threshold level of the MTL Rx queue (in bytes):</p> <p>The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred.</p> <p>This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.</p> <p>0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.</p>

11.2.418 MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT – Offset E74h

The Queue 5 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved
27	0h RO/V	<p>Missed Packet Counter Overflow Bit (MISCNTOVF):</p> <p>When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO/V	Missed Packet Counter (MISPKTCNT): This field indicates the number of packets missed by the Ethernet Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	Reserved
11	0h RO/V	Overflow Counter Overflow Bit (OVFCNTOVF): When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO/V	Overflow Packet Counter (OVFPKTCNT): This field indicates the number of packets discarded by the Ethernet Controller because of Receive queue overflow. This counter is incremented each time the Ethernet Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.419 MTL_RXQ5_DEBUG — Offset E78h

The Queue 5 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:16	0000h RO/V	Number of Packets in Receive Queue (PRXQ): This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	0h RO	Reserved
5:4	0h RO/V	MTL Rx Queue Fill-Level Status (RXQSTS): This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THRESHOLD): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THRESHOLD): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
2:1	0h RO/V	MTL Rx Queue Read Controller State (RRCSTS): This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO/V	MTL Rx Queue Write Controller Active Status (RWCSTS): When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

11.2.420 MTL_RXQ5_CONTROL — Offset E7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E7Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3	0h RW	Receive Queue Packet Arbitration (RXQ_FRM_ARBIT): When this bit is set, the Ethernet Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the Ethernet Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	Receive Queue Weight (RXQ_WEGT): This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

11.2.421 DMA_MODE — Offset 1000h

The Bus Mode register establishes the bus operating modes for the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	<p>Interrupt Mode (INTM): This field defines the interrupt mode of Ethernet Controller. The behavior of the following outputs changes depending on the following settings: - sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) - sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) - sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. - 00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. - 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 11: Reserved 0x0 (MODE0): See above description. 0x1 (MODE1): See above description. 0x2 (MODE2): See above description. 0x3 (RSVD): Reserved.</p>
15:11	0h RO	Reserved
10	0h RW	<p>SCSW DWC_ETHER_QOS (SCSW): SCSW is Synopsys Reserved, This field must be set to "0". This field is reserved for Synopsys Internal use, and must always be set to "0" unless instructed by Synopsys. Setting this field to "1" might cause unexpected behavior in the IP.</p>
9	0h RO	Reserved
8	0h RW	<p>Descriptor Posted Write (DSPW): When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. 0x0 (DISABLE): Descriptor Posted Write is disabled. 0x1 (ENABLE): Descriptor Posted Write is enabled.</p>
7:1	0h RO	Reserved
0	0h RW	<p>Software Reset (SWR): When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all Ethernet Controller clock domains. Before reprogramming any Ethernet Controller register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.</p> <p>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.</p> <p>0x0 (DISABLE): Software Reset is disabled. 0x1 (ENABLE): Software Reset is enabled.</p>

11.2.422 DMA_SYSBUS_MODE — Offset 1004h

The System Bus mode register controls the behavior of the AHB or AXI host. It mainly controls burst splitting and number of outstanding requests.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	01010000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Enable Low Power Interface (LPI) (EN_LPI): When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. 0x0 (DISABLE): Low Power Interface (LPI) is disabled. 0x1 (ENABLE): Low Power Interface (LPI) is enabled.
30	0h RW	Unlock on Magic Packet or Remote Wake-Up Packet (LPI_XIT_PKT): When set to 1, this bit enables the AXI host to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI host to come out of the LPI mode when any packet is received. 0x0 (DISABLE): Unlock on Magic Packet or Remote Wake-Up Packet is disabled. 0x1 (ENABLE): Unlock on Magic Packet or Remote Wake-Up Packet is enabled.
29:28	0h RO	Reserved
27:24	1h RW	AXI Maximum Write Outstanding Request Limit (WR_OSR_LMT): This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1
23:20	0h RO	Reserved
19:16	1h RW	AXI Maximum Read Outstanding Request Limit (RD_OSR_LMT): This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1
15:14	0h RO	Reserved
13	0h RW	1 KB Boundary Crossing Enable for the EQOS-AXI Host (ONEKBBE): When set, the burst transfers performed by the EQOS-AXI host do not cross 1 KB boundary. When reset, the burst transfers performed by the EQOS-AXI host do not cross 4 KB boundary. 0x0 (DISABLE): 1 KB Boundary Crossing for the EQOS-AXI Host Beats is disabled. 0x1 (ENABLE): 1 KB Boundary Crossing for the EQOS-AXI Host Beats is enabled.
12	0h RW	Address-Aligned Beats (AAL):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>When this bit is set to 1, the EQOS-AXI or EQOS-AHB host performs address-aligned burst transfers on Read and Write channels.</p> <p>0x0 (DISABLE): Address-Aligned Beats is disabled. 0x1 (ENABLE): Address-Aligned Beats is enabled.</p>
11	0h RW	<p>Enhanced Address Mode Enable. (EAME):</p> <p>When this bit is set to 1, the DMA host enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration.</p> <p>0x0 (DISABLE): Enhanced Address Mode is disabled. 0x1 (ENABLE): Enhanced Address Mode is enabled.</p>
10	0h RW	<p>Automatic AXI LPI enable (AALE):</p> <p>When set to 1, enables the AXI host to enter into LPI state when there is no activity in the Ethernet Controller for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register.</p> <p>0x0 (DISABLE): Automatic AXI LPI is disabled. 0x1 (ENABLE): Automatic AXI LPI is enabled.</p>
9:8	0h RO	Reserved
7	0h RW	<p>AXI Burst Length 256 (BLEN256):</p> <p>When this bit is set to 1, the EQOS-AXI host can select a burst length of 256 on the AXI interface.</p> <p>0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 256.</p>
6	0h RW	<p>AXI Burst Length 128 (BLEN128):</p> <p>When this bit is set to 1, the EQOS-AXI host can select a burst length of 128 on the AXI interface.</p> <p>0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 128.</p>
5	0h RW	<p>AXI Burst Length 64 (BLEN64):</p> <p>When this bit is set to 1, the EQOS-AXI host can select a burst length of 64 on the AXI interface.</p> <p>0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 64.</p>
4	0h RW	<p>AXI Burst Length 32 (BLEN32):</p> <p>When this bit is set to 1, the EQOS-AXI host can select a burst length of 32 on the AXI interface.</p> <p>0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 32.</p>
3	0h RW	<p>AXI Burst Length 16 (BLEN16):</p> <p>When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI host can select a burst length of 16 on the AXI interface.</p> <p>When the FB bit is set to 0, setting this bit has no effect.</p> <p>0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 16.</p>
2	0h RW	<p>AXI Burst Length 8 (BLEN8):</p> <p>When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI host can select a burst length of 8 on the AXI interface.</p> <p>When the FB bit is set to 0, setting this bit has no effect.</p> <p>0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 8.</p>
1	0h RW	<p>AXI Burst Length 4 (BLEN4):</p> <p>When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI host can select a burst length of 4 on the AXI interface.</p> <p>When the FB bit is set to 0, setting this bit has no effect.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 4.
0	0h RW	<p>FB: Fixed Burst Length When this bit is set to 1, the EQOS-AXI host initiates burst transfers of specified lengths as given below.</p> <ul style="list-style-type: none"> - Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field - Burst transfers of length 1 <p>When this bit is set to 0, the EQOS-AXI host initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1].</p> <p>0x0 (DISABLE): Fixed Burst Length is disabled. 0x1 (ENABLE): Fixed Burst Length is enabled.</p>

11.2.423 DMA_INTERRUPT_STATUS – Offset 1008h

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17	0h RO/V	<p>MAC Interrupt Status (MACIS): This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source.</p> <p>0x0 (INACTIVE): MAC Interrupt Status not detected. 0x1 (ACTIVE): MAC Interrupt Status detected.</p>
16	0h RO/V	<p>MTL Interrupt Status (MTLIS): This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source.</p> <p>0x0 (INACTIVE): MTL Interrupt Status not detected. 0x1 (ACTIVE): MTL Interrupt Status detected.</p>
15:6	0h RO	Reserved
5	0h RO/V	<p>DMA Channel 5 Interrupt Status (DC5IS): This bit indicates an interrupt event in DMA Channel 5. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 5 to get the exact cause of the interrupt and clear its source.</p> <p>0x0 (INACTIVE): DMA Channel 5 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 5 Interrupt Status detected.</p>
4	0h RO/V	<p>DMA Channel 4 Interrupt Status (DC4IS): This bit indicates an interrupt event in DMA Channel 4. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 4 to get the exact cause of the interrupt and clear its source.</p> <p>0x0 (INACTIVE): DMA Channel 4 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 4 Interrupt Status detected.</p>

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Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	DMA Channel 3 Interrupt Status (DC3IS): This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 3 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 3 Interrupt Status detected.
2	0h RO/V	DMA Channel 2 Interrupt Status (DC2IS): This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 2 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 2 Interrupt Status detected.
1	0h RO/V	DMA Channel 1 Interrupt Status (DC1IS): This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 1 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 1 Interrupt Status detected.
0	0h RO/V	DMA Channel 0 Interrupt Status (DC0IS): This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 0 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 0 Interrupt Status detected.

11.2.424 DMA_DEBUG_STATUS0 — Offset 100Ch

The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	DMA Channel 2 Transmit Process State (TPS2): This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO/V	DMA Channel 2 Receive Process State (RPS2): This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor).

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>0x2 (RSVD): Reserved for future use.</p> <p>0x3 (RUN_WRP): Running (Waiting for Rx packet).</p> <p>0x4 (SUSPND): Suspended (Rx Descriptor Unavailable).</p> <p>0x5 (RUN_CRD): Running (Closing the Rx Descriptor).</p> <p>0x6 (TSTMP): Timestamp write state.</p> <p>0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).</p>
23:20	0h RO/V	<p>DMA Channel 1 Transmit Process State (TPS1):</p> <p>This field indicates the Tx DMA FSM state for Channel 1.</p> <p>The MSB of this field always returns 0. This field does not generate an interrupt.</p> <p>0x0 (STOP): Stopped (Reset or Stop Transmit Command issued).</p> <p>0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor).</p> <p>0x2 (RUN_WS): Running (Waiting for status).</p> <p>0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)).</p> <p>0x4 (TSTMP_WS): Timestamp write state.</p> <p>0x5 (RSVD): Reserved for future use.</p> <p>0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow).</p> <p>0x7 (RUN_CTD): Running (Closing Tx Descriptor).</p>
19:16	0h RO/V	<p>DMA Channel 1 Receive Process State (RPS1):</p> <p>This field indicates the Rx DMA FSM state for Channel 1.</p> <p>The MSB of this field always returns 0. This field does not generate an interrupt.</p> <p>0x0 (STOP): Stopped (Reset or Stop Receive Command issued).</p> <p>0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor).</p> <p>0x2 (RSVD): Reserved for future use.</p> <p>0x3 (RUN_WRP): Running (Waiting for Rx packet).</p> <p>0x4 (SUSPND): Suspended (Rx Descriptor Unavailable).</p> <p>0x5 (RUN_CRD): Running (Closing the Rx Descriptor).</p> <p>0x6 (TSTMP): Timestamp write state.</p> <p>0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).</p>
15:12	0h RO/V	<p>DMA Channel 0 Transmit Process State (TPS0):</p> <p>This field indicates the Tx DMA FSM state for Channel 0.</p> <p>The MSB of this field always returns 0. This field does not generate an interrupt.</p> <p>0x0 (STOP): Stopped (Reset or Stop Transmit Command issued).</p> <p>0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor).</p> <p>0x2 (RUN_WS): Running (Waiting for status).</p> <p>0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)).</p> <p>0x4 (TSTMP_WS): Timestamp write state.</p> <p>0x5 (RSVD): Reserved for future use.</p> <p>0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow).</p> <p>0x7 (RUN_CTD): Running (Closing Tx Descriptor).</p>
11:8	0h RO/V	<p>DMA Channel 0 Receive Process State (RPS0):</p> <p>This field indicates the Rx DMA FSM state for Channel 0.</p> <p>The MSB of this field always returns 0. This field does not generate an interrupt.</p> <p>0x0 (STOP): Stopped (Reset or Stop Receive Command issued).</p> <p>0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor).</p> <p>0x2 (RSVD): Reserved for future use.</p> <p>0x3 (RUN_WRP): Running (Waiting for Rx packet).</p> <p>0x4 (SUSPND): Suspended (Rx Descriptor Unavailable).</p> <p>0x5 (RUN_CRD): Running (Closing the Rx Descriptor).</p> <p>0x6 (TSTMP): Timestamp write state.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:2	0h RO	Reserved
1	0h RO/V	AXI Host Read Channel Status (AXRHSTS): When high, this bit indicates that the read channel of the AXI host is active, and it is transferring the data. 0x0 (INACTIVE): AXI Host Read Channel Status not detected. 0x1 (ACTIVE): AXI Host Read Channel Status detected.
0	0h RO/V	AXI Host Write Channel (AXWHSTS): When high, this bit indicates that the write channel of the AXI host is active, and it is transferring data. 0x0 (INACTIVE): AXI Host Write Channel or AHB Host Status not detected. 0x1 (ACTIVE): AXI Host Write Channel or AHB Host Status detected.

11.2.425 DMA_DEBUG_STATUS1 — Offset 1010h

The Debug Status1 register gives the Receive and Transmit process status for DMA Channel 3-Channel 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	DMA Channel 5 Receive Process State (RPS5): This field indicates the Rx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
15:12	0h RO	Reserved
11:8	0h RO/V	DMA Channel 4 Receive Process State (RPS4): This field indicates the Rx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor).

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:4	0h RO/V	DMA Channel 3 Transmit Process State (TPS3): This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO/V	DMA Channel 3 Receive Process State (RPS3): This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

11.2.426 AXI4_TX_AR_ACE_CONTROL — Offset 1020h

This register is used to control the AXI4 Cache Coherency Signals for read transactions by all the Transmit DMA channels. The following signals of the AXI4 interface are driven with different values as programmed

for corresponding type (descriptor, buffer1, buffer2) of access.

- arcache_m_o[3:0]
- ardomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21:20	0h RW	Transmit DMA First Packet Buffer or TSO Header Domain Control (THD): When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO Header data.
19:16	0h RW	Transmit DMA First Packet Buffer or TSO Header Cache Control (THC): When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO Header data.
15:14	0h RO	Reserved
13:12	0h RW	Transmit DMA Extended Packet Buffer or TSO Payload Domain Control (TED): When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO payload data.
11:8	0h RW	Transmit DMA Extended Packet Buffer or TSO Payload Cache Control (TEC): When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO payload data.
7:6	0h RO	Reserved
5:4	0h RW	Transmit DMA Read Descriptor Domain Control (TDRD): This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the Descriptor.
3:0	0h RW	Transmit DMA Read Descriptor Cache Control (TDRC): This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor.

11.2.427 AXI4_RX_AW_ACE_CONTROL – Offset 1024h

This register is used to control the AXI4 Cache Coherency Signals for write transactions by all the Receive DMA channels. The following signals of the AXI4 interface are driven with different values as programmed

for corresponding type (descriptor, buffer1, buffer2) of access.

- awcache_m_o[3:0]
- awdomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29:28	0h RW	Receive DMA Buffer Domain Control (RDD): This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.

continued...

Bit Range	Default & Access	Field Name (ID): Description
27:24	0h RW	Receive DMA Buffer Cache Control (RDC): This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
23:22	0h RO	Reserved
21:20	0h RW	Receive DMA Header Domain Control (RHD): This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
19:16	0h RW	Receive DMA Header Cache Control (RHC): This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
15:14	0h RO	Reserved
13:12	0h RW	Receive DMA Payload Domain Control (RPD): This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
11:8	0h RW	Receive DMA Payload Cache Control (RPC): This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
7:6	0h RO	Reserved
5:4	0h RW	Receive DMA Write Descriptor Domain Control (RDWD): This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor.
3:0	0h RW	Receive DMA Write Descriptor Cache Control (RDWC): This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor.

11.2.428 AXI4_TXRX_AWAR_ACE_CONTROL — Offset 1028h

This register is used to control the AXI4 Cache Coherency Signals for Descriptor write transactions by all the TxDMA channels and Descriptor read transactions by all the RxDMA channels. It also controls the values to be driven on awprot_m_o and arprot_m_o.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved
22:20	0h RW	DMA Write Protection control (WRP): This field is used to drive awprot_m_o[2:0] signal on the AXI Write Channel.
19	0h RO	Reserved
18:16	0h RW	DMA Read Protection control (RDP): This field is used to drive arprot_m_o[2:0] signal during all read requests.

continued...

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved
13:12	0h RW	Receive DMA Read Descriptor Domain control (RDRD): This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor.
11:8	0h RW	Receive DMA Read Descriptor Cache control (RDRC): This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor.
7:6	0h RO	Reserved
5:4	0h RW	Transmit DMA Write Descriptor Domain control (TDWD): This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor.
3:0	0h RW	Transmit DMA Write Descriptor Cache control (TDWC): This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor.

11.2.429 AXI_LPI_ENTRY_INTERVAL — Offset 1040h

This register is used to control the AXI LPI entry interval.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved
3:0	0h RW	LPI Entry Interval (LPIEI): Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the GbE Controller to enter into the AXI low power state 0 indicates 64 clock cycles

11.2.430 DMA_TBS_CTRL — Offset 1050h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	Fetch Time Offset (FTOS): The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	Reserved
6:4	0h RW	Fetch GSN Offset (FGOS): The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
0	0h RW	<p>Fetch Time Offset Valid (FTOV): Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions.</p> <p>0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.</p>

11.2.431 DMA_SAFETY_INTERRUPT_STATUS – Offset 1080h

This register indicates summary (whether error occurred in DMA/MTL/MAC and correctable/uncorrectable) of the Automotive Safety related error interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1080h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	<p>MAC Safety Uncorrectable Interrupt Status (MCSIS): Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC.</p> <p>0x0 (INACTIVE): MAC Safety Uncorrectable Interrupt Status not detected. 0x1 (ACTIVE): MAC Safety Uncorrectable Interrupt Status detected.</p>
30	0h RO	Reserved
29	0h RO/V	<p>MTL Safety Uncorrectable error Interrupt Status (MSUIS): This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register.</p> <p>0x0 (INACTIVE): MTL Safety Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Uncorrectable error Interrupt Status detected.</p>
28	0h RO/V	<p>MTL Safety Correctable error Interrupt Status (MSCIS): This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register.</p> <p>0x0 (INACTIVE): MTL Safety Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Correctable error Interrupt Status detected.</p>
27:2	0h RO	Reserved
1	0h RO/V	<p>DMA ECC Uncorrectable error Interrupt Status (DEUIS): This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register.</p> <p>0x0 (INACTIVE): DMA ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Uncorrectable error Interrupt Status detected.</p>
0	0h RO/V	<p>DMA ECC Correctable error Interrupt Status (DECIS): This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register.</p> <p>0x0 (INACTIVE): DMA ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Correctable error Interrupt Status detected.</p>

11.2.432 DMA_ECC_INTERRUPT_ENABLE — Offset 1084h

This register is used to enable the Automotive Safety related TSO memory ECC error interrupt.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1084h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved
0	0h RW	TSO memory Correctable Error Interrupt Enable (TCEIE): When set, generates an interrupt when a correctable error is detected at the DMA TSO memory interface. It is indicated in the TCES bit of DMA_ECC_Interrupt_Status register. When reset this event does not generate an interrupt. 0x0 (DISABLE): TSO memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): TSO memory Correctable Error Interrupt is enabled.

11.2.433 DMA_ECC_INTERRUPT_STATUS — Offset 1088h

This register indicates the Automotive Safety related TSO memory ECC error interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1088h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved
2	0h RW	DMA TSO memory Uncorrectable Error status (TUES): When set, indicates that an uncorrectable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Uncorrectable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Uncorrectable Error status detected.
1	0h RW	DMA TSO memory Address Mismatch status (TAMS): This bit when set indicates that address mismatch is found for address bus of DMA TSO memory. 0x0 (INACTIVE): DMA TSO memory Address Mismatch status not detected. 0x1 (ACTIVE): DMA TSO memory Address Mismatch status detected.
0	0h RW	DMA TSO memory Correctable Error status (TCES): This bit when set indicates that correctable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Correctable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Correctable Error status detected.

11.2.434 DMA_CH0_CONTROL — Offset 1100h

The DMA Channel Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1100h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RO	Reserved Platform firmware and software shall not set this field to 0x1.
23:21	0h RO	Reserved
20:18	0h RW	Descriptor Skip Length (DSL): This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	Reserved
16	0h RW	8xPBL mode (PBLX8): When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	Reserved
13:0	0000h RW	Maximum Segment Size (MSS): This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

11.2.435 DMA_CH0_TX_CONTROL — Offset 1104h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved
28	0h RW	Enhanced Descriptor Enable (EDSE): When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	Transmit QOS. (TQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.

continued...

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RO	Reserved
21:16	00h RW	<p>Transmit Programmable Burst Length (TxPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.</p> <p>To transfer more than 32 beats, perform the following steps:</p> <ol style="list-style-type: none"> 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. <p>Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.</p>
15	0h RW	<p>Ignore PBL Requirement (IPBL): When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA.</p> <p>Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.</p> <p>0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.</p>
14:13	0h RW	<p>TSE_MODE: TSE Mode</p> <ul style="list-style-type: none"> - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved <p>0x0 (TSO_USO): TSO/USO. 0x1 (UFWOC): UFO with Checksum. 0x2 (UFWOC): UFO without Checksum. 0x3 (RSVD): Reserved.</p>
12	0h RW	<p>TCP Segmentation Enabled (TSE): When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor. When this bit is set, the TxPBL value must be greater than 4.</p> <p>0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.</p>
11:5	0h RO	Reserved
4	0h RW	<p>Operate on Second Packet (OSF): When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained.</p> <p>0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.</p>
3:1	0h	Transmit Channel Weight (TCW):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	<p>This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.</p>
0	0h RW	<p>Start or Stop Transmission Command (ST): When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.</p>

11.2.436 DMA_CH0_RX_CONTROL — Offset 1108h

The DMA Channel Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1108h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	<p>Rx Packet Flush. (RPF): When this bit is set to 1, then Ethernet Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the Ethernet Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.</p>
30:28	0h RO	Reserved
27:24	0h RW	<p>Rx AXI4 QOS. (RQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RO	Reserved
21:16	00h RW	<p>Receive Programmable Burst Length (RXPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.</p> <p>To transfer more than 32 beats, perform the following steps:</p> <ol style="list-style-type: none"> 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. <p>Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.</p>
15	0h RO	Reserved
14:4	000h RW	<p>Receive Buffer size High (RBSZ_13_Y): RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled.</p> <p>Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).</p>
3:1	0h RO/V	<p>Receive Buffer size Low (RBSZ_X_0): RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration.</p> <p>This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).</p>
0	0h RW	<p>Start or Stop Receive (SR): When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets.</p> <p>The DMA tries to acquire descriptor from either of the following positions:</p> <ul style="list-style-type: none"> - The current position in the list <p>This is the address set by the DMA_CH0_RxDesc_List_Address register.</p> <ul style="list-style-type: none"> - The position at which the Rx process was previously stopped <p>If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable.</p> <p>When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state.</p> <p>0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.</p>

11.2.437 DMA_CH0_TXDESC_LIST_ADDRESS — Offset 1110h

The Channel Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Transmit List (TDESHA): This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

11.2.438 DMA_CH0_TXDESC_LIST_ADDRESS — Offset 1114h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Transmit List (TDESLA): This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.439 DMA_CH0_RXDESC_LIST_HADDRESS – Offset 1118h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1118h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Receive List (RDESHA): This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

11.2.440 DMA_CH0_RXDESC_LIST_ADDRESS – Offset 111Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 111Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Receive List (RDESLA): This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration

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Bit Range	Default & Access	Field Name (ID): Description
		- 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.441 DMA_CH0_TXDESC_TAIL_POINTER — Offset 1120h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Transmit Descriptor Tail Pointer (TDTP): This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.442 DMA_CH0_RXDESC_TAIL_POINTER — Offset 1128h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Receive Descriptor Tail Pointer (RDTP): This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.443 DMA_CH0_TXDESC_RING_LENGTH — Offset 112Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 112Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Transmit Descriptor Ring Length (TDRL): This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel® recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.444 DMA_CHO_RXDESC_RING_LENGTH — Offset 1130h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Receive Descriptor Ring Length (RDRL): This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.445 DMA_CHO_INTERRUPT_ENABLE — Offset 1134h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW	Normal Interrupt Summary Enable (NIE): When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CHO_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt

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Bit Range	Default & Access	Field Name (ID): Description
		When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	Abnormal Interrupt Summary Enable (AIE): When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	Context Descriptor Error Enable (CDEE): When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	Fatal Bus Error Enable (FBEE): When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	Early Receive Interrupt Enable (ERIE): When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout Enable (RWTE): When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.
8	0h RW	Receive Stopped Enable (RSE): When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	Receive Buffer Unavailable Enable (RBUE): When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	Receive Interrupt Enable (RIE): When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	Reserved
2	0h RW	Transmit Buffer Unavailable Enable (TBUE): When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	Transmit Stopped Enable (TXSE): When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	Transmit Interrupt Enable (TIE): When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

11.2.446 DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1138h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CH*i*_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	Receive Interrupt Watchdog Timer Count Units (RWTU): This field indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	Reserved
7:0	00h RW	Receive Interrupt Watchdog Timer Count (RWT): This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(<i>#i</i>)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30].

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Bit Range	Default & Access	Field Name (ID): Description
		When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

11.2.447 DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS – Offset 113Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 113Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	Reference Slot Number (RSN): This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	Slot Interval Value (SIV): This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us
3:2	0h RO	Reserved
1	0h RW	Advance Slot Check (ASC): When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is <ul style="list-style-type: none"> - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots <p>This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.</p>
0	0h RW	Enable Slot Comparison (ESC): When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is <ul style="list-style-type: none"> - equal to the reference slot number or - ahead of the reference slot number by one slot <p>When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed.</p> <p>Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.</p> <p>0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.</p>

11.2.448 DMA_CH0_CURRENT_APP_TXDESC — Offset 1144h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Transmit Descriptor Address Pointer (CURTDESAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.449 DMA_CH0_CURRENT_APP_RXDESC — Offset 114Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Descriptor Address Pointer (CURRDESAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.450 DMA_CH0_CURRENT_APP_TXBUFFER_H — Offset 1150h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTRH): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.451 DMA_CH0_CURRENT_APP_TXBUFFER — Offset 1154h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.452 DMA_CH0_CURRENT_APP_RXBUFFER_H — Offset 1158h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1158h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTRH): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.453 DMA_CH0_CURRENT_APP_RXBUFFER — Offset 115Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 115Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.454 DMA_CH0_STATUS — Offset 1160h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

NOTE

The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1160h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h	Reserved

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Bit Range	Default & Access	Field Name (ID): Description
	RO	
21:19	0h RO/V	<p>Rx DMA Error Bits (REB):</p> <p>This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
18:16	0h RO/V	<p>Tx DMA Error Bits (TEB):</p> <p>This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
15	0h RW	<p>Normal Interrupt Summary (NIS):</p> <p>Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt <p>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Normal Interrupt Summary status not detected.</p> <p>0x1 (ACTIVE): Normal Interrupt Summary status detected.</p>
14	0h RW	<p>Abnormal Interrupt Summary (AIS):</p> <p>Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error <p>Only unmasked bits affect the Abnormal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Abnormal Interrupt Summary status not detected.</p> <p>0x1 (ACTIVE): Abnormal Interrupt Summary status detected.</p>
13	0h RW	<p>Context Descriptor Error (CDE):</p> <p>This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Context Descriptor Error status not detected.</p> <p>0x1 (ACTIVE): Context Descriptor Error status detected.</p>
12	0h RW	<p>Fatal Bus Error (FBE):</p> <p>This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Fatal Bus Error status not detected.</p> <p>0x1 (ACTIVE): Fatal Bus Error status detected.</p>
11	0h RW	<p>Early Receive Interrupt (ERI):</p> <p>This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory.</p> <p>In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.</p> <p>The setting of RI bit automatically clears this bit.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Early Receive Interrupt status not detected.</p> <p>0x1 (ACTIVE): Early Receive Interrupt status detected.</p>
10	0h RO	Reserved
9	0h RW	<p>Receive Watchdog Timeout (RWT):</p> <p>This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received.</p> <p>0x0 (INACTIVE): Receive Watchdog Timeout status not detected.</p> <p>0x1 (ACTIVE): Receive Watchdog Timeout status detected.</p>
8	0h RW	<p>Receive Process Stopped (RPS):</p> <p>This bit is asserted when the Rx process enters the Stopped state.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Process Stopped status not detected.</p> <p>0x1 (ACTIVE): Receive Process Stopped status detected.</p>
7	0h RW	<p>Receive Buffer Unavailable (RBU):</p> <p>This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Buffer Unavailable status not detected.</p> <p>0x1 (ACTIVE): Receive Buffer Unavailable status detected.</p>
6	0h RW	Receive Interrupt (RI):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>The reception remains in the Running state.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Interrupt status not detected.</p> <p>0x1 (ACTIVE): Receive Interrupt status detected.</p>
5:3	0h RO	Reserved
2	0h RW	<p>Transmit Buffer Unavailable (TBU):</p> <p>This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions.</p> <p>To resume processing the Transmit descriptors, the application should do the following:</p> <ol style="list-style-type: none"> 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. <p>For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Buffer Unavailable status not detected.</p> <p>0x1 (ACTIVE): Transmit Buffer Unavailable status detected.</p>
1	0h RW	<p>Transmit Process Stopped (TPS):</p> <p>This bit is set when the transmission is stopped.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Process Stopped status not detected.</p> <p>0x1 (ACTIVE): Transmit Process Stopped status detected.</p>
0	0h RW	<p>Transmit Interrupt (TI):</p> <p>This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Interrupt status not detected.</p> <p>0x1 (ACTIVE): Transmit Interrupt status detected.</p>

11.2.455 DMA_CH0_MISS_FRAME_CNT – Offset 1164h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH\${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1164h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:16	0h RO	Reserved	
15	0h RO/V	<p>Overflow status of the MFC Counter (MFCO):</p> <p>When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Miss Frame Counter overflow not occurred.</p>	

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	Reserved
10:0	000h RO/V	Dropped Packet Counters (MFC): This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH\${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.456 DMA_CH0_RX_ERI_CNT — Offset 116Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 116Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	000h RO/V	ERI Counter (ECNT): When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

11.2.457 DMA_CH1_CONTROL — Offset 1180h

The DMA Channel1 Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RO	Reserved Platform firmware & software will not set this field to 0x1.
23:21	0h RO	Reserved
20:18	0h RW	Descriptor Skip Length (DSL): This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.

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Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	Reserved
16	0h RW	8xPBL mode (PBLX8): When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	Reserved
13:0	0000h RW	Maximum Segment Size (MSS): This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

11.2.458 DMA_CH1_TX_CONTROL — Offset 1184h

The DMA Channel1 Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:29	0h RW	Time Select (TFSEL): Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	Enhanced Descriptor Enable (EDSE): When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	Transmit QOS. (TQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Transmit Programmable Burst Length (TXPBL):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.</p> <p>To transfer more than 32 beats, perform the following steps:</p> <ol style="list-style-type: none"> 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. <p>Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.</p>
15	0h RW	<p>Ignore PBL Requirement (IPBL):</p> <p>When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA.</p> <p>Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.</p> <p>0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.</p>
14:13	0h RW	<p>TSE_MODE:</p> <p>TSE Mode</p> <ul style="list-style-type: none"> - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved <p>0x0 (TSO_USO): TSO/USO. 0x1 (UFWOC): UFO with Checksum. 0x2 (UFWOC): UFO without Checksum. 0x3 (RSVD): Reserved.</p>
12	0h RW	<p>TCP Segmentation Enabled (TSE):</p> <p>When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor. When this bit is set, the TxPBL value must be greater than 4.</p> <p>0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.</p>
11:5	0h RO	Reserved

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Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	Operate on Second Packet (OSF): When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	Transmit Channel Weight (TCW): This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	Start or Stop Transmission Command (ST): When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

11.2.459 DMA_CH1_RX_CONTROL — Offset 1188h

The DMA Channel 1 Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Rx Packet Flush. (RPF): When this bit is set to 1, then Ethernet Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the Ethernet Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control

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Bit Range	Default & Access	Field Name (ID): Description
		register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	Reserved
27:24	0h RW	Rx AXI4 QOS. (RQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Receive Programmable Burst Length (RXPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	Reserved
14:4	000h RW	Receive Buffer size High (RBSZ_13_Y): RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO/V	Receive Buffer size Low (RBSZ_X_0): RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	Start or Stop Receive (SR): When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable.

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Bit Range	Default & Access	Field Name (ID): Description
		When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

11.2.460 DMA_CH1_TXDESC_LIST_HADDRESS — Offset 1190h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Transmit List (TDESHA): This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

11.2.461 DMA_CH1_TXDESC_LIST_ADDRESS — Offset 1194h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1194h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	<p>Start of Transmit List (TDESLA): This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration </p>
2:0	0h RO	Reserved

11.2.462 DMA_CH1_RXDESC_LIST_HADDRESS — Offset 1198h

The Channel Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CH1_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1198h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	<p>Start of Receive List (RDESHA): This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list. </p>

11.2.463 DMA_CH1_RXDESC_LIST_ADDRESS — Offset 119Ch

The Channel Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 119Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Receive List (RDESLA): This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.464 DMA_CH1_TXDESC_TAIL_POINTER — Offset 11A0h

The Channel1 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Transmit Descriptor Tail Pointer (TDTP): This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.465 DMA_CH1_RXDESC_TAIL_POINTER — Offset 11A8h

The Channel1 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Receive Descriptor Tail Pointer (RDTP): This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration:

continued...

Bit Range	Default & Access	Field Name (ID): Description
		- 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.466 DMA_CH1_TXDESC_RING_LENGTH — Offset 11ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Transmit Descriptor Ring Length (TDRL): This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel® recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.467 DMA_CH1_RXDESC_RING_LENGTH — Offset 11B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Receive Descriptor Ring Length (RDRL): This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.468 DMA_CH1_INTERRUPT_ENABLE — Offset 11B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW	<p>Normal Interrupt Summary Enable (NIE): When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.</p>
14	0h RW	<p>Abnormal Interrupt Summary Enable (AIE): When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.</p>
13	0h RW	<p>Context Descriptor Error Enable (CDEE): When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.</p>
12	0h RW	<p>Fatal Bus Error Enable (FBEE): When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.</p>
11	0h RW	<p>Early Receive Interrupt Enable (ERIE): When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.</p>
10	0h RO	Reserved
9	0h RW	<p>Receive Watchdog Timeout Enable (RWTE): When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.</p>
8	0h RW	<p>Receive Stopped Enable (RSE): When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	Receive Buffer Unavailable Enable (RBUE): When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	Receive Interrupt Enable (RIE): When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	Reserved
2	0h RW	Transmit Buffer Unavailable Enable (TBUE): When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	Transmit Stopped Enable (TXSE): When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	Transmit Interrupt Enable (TIE): When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

11.2.469 DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER — Offset 11B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	Receive Interrupt Watchdog Timer Count Units (RWTU): This field indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048

continued...

Bit Range	Default & Access	Field Name (ID): Description
		For example, when RWT=2 and RWTU=1, the watchdog timer is set for $2 \times 512 = 1024$ system clock cycles.
15:8	0h RO	Reserved
7:0	00h RW	<p>Receive Interrupt Watchdog Timer Count (RWT): This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set.</p> <p>The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30].</p> <p>When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.</p>

11.2.470 DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS – Offset 11BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	<p>Reference Slot Number (RSN): This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.</p>
15:4	07Ch RW	<p>Slot Interval Value (SIV): This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us</p>
3:2	0h RO	Reserved
1	0h RW	<p>Advance Slot Check (ASC): When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is <ul style="list-style-type: none"> - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled. </p>
0	0h RW	<p>Enable Slot Comparison (ESC): When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is <ul style="list-style-type: none"> - equal to the reference slot number </p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>or</p> <ul style="list-style-type: none"> - ahead of the reference slot number by one slot <p>When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed.</p> <p>Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.</p> <p>0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.</p>

11.2.471 DMA_CH1_CURRENT_APP_TXDESC — Offset 11C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Transmit Descriptor Address Pointer (CURTDESAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.472 DMA_CH1_CURRENT_APP_RXDESC — Offset 11CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Receive Descriptor Address Pointer (CURRDESAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.473 DMA_CH1_CURRENT_APP_TXBUFFER_H — Offset 11D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
7:0	00h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTRH): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.474 DMA_CH1_CURRENT_APP_TXBUFFER — Offset 11D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.475 DMA_CH1_CURRENT_APP_RXBUFFER_H — Offset 11D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTRH): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.476 DMA_CH1_CURRENT_APP_RXBUFFER — Offset 11DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.477 DMA_CH1_STATUS — Offset 11E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

NOTE

The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21:19	0h RO/V	<p>Rx DMA Error Bits (REB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
18:16	0h RO/V	<p>Tx DMA Error Bits (TEB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
15	0h RW	<p>Normal Interrupt Summary (NIS): Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt <p>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.
14	0h RW	Abnormal Interrupt Summary (AIS): Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	Context Descriptor Error (CDE): This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	Fatal Bus Error (FBE): This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	Early Receive Interrupt (ERI): This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout (RWT): This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	Receive Process Stopped (RPS): This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	Receive Buffer Unavailable (RBU): This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	Receive Interrupt (RI): This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	Reserved
2	0h RW	Transmit Buffer Unavailable (TBU): This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	Transmit Process Stopped (TPS): This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	Transmit Interrupt (TI): This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

11.2.478 DMA_CH1_MISS_FRAME_CNT — Offset 11E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH\${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E4h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RO/V	Overflow status of the MFC Counter (MFCO): When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	Reserved
10:0	000h RO/V	Dropped Packet Counters (MFC): This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programming RPF field in DMA_CH\${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.479 DMA_CH1_RX_ERI_CNT — Offset 11ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ECh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	000h RO/V	ERI Counter (ECNT): When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

11.2.480 DMA_CH2_CONTROL — Offset 1200h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1200h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
24	0h RO	Reserved Platform firmware & software will not set this field to 0x1.
23:21	0h RO	Reserved
20:18	0h RW	Descriptor Skip Length (DSL): This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	Reserved
16	0h RW	8xPBL mode (PBLX8): When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	Reserved
13:0	0000h RW	Maximum Segment Size (MSS): This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

11.2.481 DMA_CH2_TX_CONTROL — Offset 1204h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:29	0h RW	Time Select (TFSEL): Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	Enhanced Descriptor Enable (EDSE): When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	Transmit QOS. (TQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Transmit Programmable Burst Length (TxPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	Ignore PBL Requirement (IPBL): When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	TSE_MODE: TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFWC): UFO with Checksum. 0x2 (UFWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	TCP Segmentation Enabled (TSE): When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDESO[19]) is set in the Tx Normal descriptor. When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	<p>Operate on Second Packet (OSF): When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.</p>
3:1	0h RW	<p>Transmit Channel Weight (TCW): This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.</p>
0	0h RW	<p>Start or Stop Transmission Command (ST): When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.</p>

11.2.482 DMA_CH2_RX_CONTROL — Offset 1208h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1208h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	<p>Rx Packet Flush. (RPF): When this bit is set to 1, then Ethernet Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the Ethernet Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	Reserved
27:24	0h RW	Rx AXI4 QOS. (RQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Receive Programmable Burst Length (RXPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	Reserved
14:4	000h RW	Receive Buffer size High (RBSZ_13_Y): RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO/V	Receive Buffer size Low (RBSZ_X_0): RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	Start or Stop Receive (SR): When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

11.2.483 DMA_CH2_TXDESC_LIST_HADDRESS – Offset 1210h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Transmit List (TDESHA): This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

11.2.484 DMA_CH2_TXDESC_LIST_ADDRESS – Offset 1214h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Transmit List (TDESLA): This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.485 DMA_CH2_RXDESC_LIST_HADDRESS – Offset 1218h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1218h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Receive List (RDESHA): This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

11.2.486 DMA_CH2_RXDESC_LIST_ADDRESS – Offset 121Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 121Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Receive List (RDESLA): This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration

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Bit Range	Default & Access	Field Name (ID): Description
		- 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.487 DMA_CH2_TXDESC_TAIL_POINTER — Offset 1220h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Transmit Descriptor Tail Pointer (TDTP): This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.488 DMA_CH2_RXDESC_TAIL_POINTER — Offset 1228h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Receive Descriptor Tail Pointer (RDTP): This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.489 DMA_CH2_TXDESC_RING_LENGTH — Offset 122Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 122Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Transmit Descriptor Ring Length (TDRL): This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel® recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.490 DMA_CH2_RXDESC_RING_LENGTH — Offset 1230h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Receive Descriptor Ring Length (RDRL): This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.491 DMA_CH2_INTERRUPT_ENABLE — Offset 1234h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW	Normal Interrupt Summary Enable (NIE): When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt

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Bit Range	Default & Access	Field Name (ID): Description
		When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	Abnormal Interrupt Summary Enable (AIE): When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	Context Descriptor Error Enable (CDEE): When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	Fatal Bus Error Enable (FBEE): When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	Early Receive Interrupt Enable (ERIE): When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout Enable (RWTE): When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.
8	0h RW	Receive Stopped Enable (RSE): When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	Receive Buffer Unavailable Enable (RBUE): When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	Receive Interrupt Enable (RIE): When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	Reserved
2	0h RW	Transmit Buffer Unavailable Enable (TBUE): When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	Transmit Stopped Enable (TXSE): When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	Transmit Interrupt Enable (TIE): When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

11.2.492 DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1238h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CH*i*_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	Receive Interrupt Watchdog Timer Count Units (RWTU): This field indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	Reserved
7:0	00h RW	Receive Interrupt Watchdog Timer Count (RWT): This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(<i>#i</i>)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30].

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Bit Range	Default & Access	Field Name (ID): Description
		When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

11.2.493 DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS – Offset 123Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 123Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	Reference Slot Number (RSN): This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	Slot Interval Value (SIV): This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us
3:2	0h RO	Reserved
1	0h RW	Advance Slot Check (ASC): When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is <ul style="list-style-type: none"> - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots <p>This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.</p>
0	0h RW	Enable Slot Comparison (ESC): When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is <ul style="list-style-type: none"> - equal to the reference slot number or - ahead of the reference slot number by one slot <p>When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed.</p> <p>Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.</p> <p>0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.</p>

11.2.494 DMA_CH2_CURRENT_APP_TXDESC — Offset 1244h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Transmit Descriptor Address Pointer (CURTDESAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.495 DMA_CH2_CURRENT_APP_RXDESC — Offset 124Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Descriptor Address Pointer (CURRDESAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.496 DMA_CH2_CURRENT_APP_TXBUFFER_H — Offset 1250h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1250h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTRH): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.497 DMA_CH2_CURRENT_APP_TXBUFFER — Offset 1254h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1254h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.498 DMA_CH2_CURRENT_APP_RXBUFFER_H — Offset 1258h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1258h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTRH): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.499 DMA_CH2_CURRENT_APP_RXBUFFER — Offset 125Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 125Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.500 DMA_CH2_STATUS — Offset 1260h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

NOTE

The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1260h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h	Reserved

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Bit Range	Default & Access	Field Name (ID): Description
	RO	
21:19	0h RO/V	<p>Rx DMA Error Bits (REB):</p> <p>This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
18:16	0h RO/V	<p>Tx DMA Error Bits (TEB):</p> <p>This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
15	0h RW	<p>Normal Interrupt Summary (NIS):</p> <p>Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt <p>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Normal Interrupt Summary status not detected.</p> <p>0x1 (ACTIVE): Normal Interrupt Summary status detected.</p>
14	0h RW	<p>Abnormal Interrupt Summary (AIS):</p> <p>Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error <p>Only unmasked bits affect the Abnormal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Abnormal Interrupt Summary status not detected.</p> <p>0x1 (ACTIVE): Abnormal Interrupt Summary status detected.</p>
13	0h RW	<p>Context Descriptor Error (CDE):</p> <p>This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Context Descriptor Error status not detected.</p> <p>0x1 (ACTIVE): Context Descriptor Error status detected.</p>
12	0h RW	<p>Fatal Bus Error (FBE):</p> <p>This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Fatal Bus Error status not detected.</p> <p>0x1 (ACTIVE): Fatal Bus Error status detected.</p>
11	0h RW	<p>Early Receive Interrupt (ERI):</p> <p>This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory.</p> <p>In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.</p> <p>The setting of RI bit automatically clears this bit.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Early Receive Interrupt status not detected.</p> <p>0x1 (ACTIVE): Early Receive Interrupt status detected.</p>
10	0h RO	Reserved
9	0h RW	<p>Receive Watchdog Timeout (RWT):</p> <p>This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received.</p> <p>0x0 (INACTIVE): Receive Watchdog Timeout status not detected.</p> <p>0x1 (ACTIVE): Receive Watchdog Timeout status detected.</p>
8	0h RW	<p>Receive Process Stopped (RPS):</p> <p>This bit is asserted when the Rx process enters the Stopped state.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Process Stopped status not detected.</p> <p>0x1 (ACTIVE): Receive Process Stopped status detected.</p>
7	0h RW	<p>Receive Buffer Unavailable (RBU):</p> <p>This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Buffer Unavailable status not detected.</p> <p>0x1 (ACTIVE): Receive Buffer Unavailable status detected.</p>
6	0h RW	Receive Interrupt (RI):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>The reception remains in the Running state.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Interrupt status not detected.</p> <p>0x1 (ACTIVE): Receive Interrupt status detected.</p>
5:3	0h RO	Reserved
2	0h RW	<p>Transmit Buffer Unavailable (TBU):</p> <p>This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions.</p> <p>To resume processing the Transmit descriptors, the application should do the following:</p> <ol style="list-style-type: none"> 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. <p>For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Buffer Unavailable status not detected.</p> <p>0x1 (ACTIVE): Transmit Buffer Unavailable status detected.</p>
1	0h RW	<p>Transmit Process Stopped (TPS):</p> <p>This bit is set when the transmission is stopped.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Process Stopped status not detected.</p> <p>0x1 (ACTIVE): Transmit Process Stopped status detected.</p>
0	0h RW	<p>Transmit Interrupt (TI):</p> <p>This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Interrupt status not detected.</p> <p>0x1 (ACTIVE): Transmit Interrupt status detected.</p>

11.2.501 DMA_CH2_MISS_FRAME_CNT – Offset 1264h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH\${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1264h	00000000h
Bit Range	Default & Access	Field Name (ID): Description	
31:16	0h RO	Reserved	
15	0h RO/V	<p>Overflow status of the MFC Counter (MFCO):</p> <p>When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Miss Frame Counter overflow not occurred.</p>	

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	Reserved
10:0	000h RO/V	Dropped Packet Counters (MFC): This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH\${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.502 DMA_CH2_RX_ERI_CNT — Offset 126Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 126Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	000h RO/V	ERI Counter (ECNT): When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

11.2.503 DMA_CH3_CONTROL — Offset 1280h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1280h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RO	Reserved Platform firmware & software will not set this field to 0x1.
23:21	0h RO	Reserved
20:18	0h RW	Descriptor Skip Length (DSL): This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.

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Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	Reserved
16	0h RW	8xPBL mode (PBLX8): When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	Reserved
13:0	0000h RW	Maximum Segment Size (MSS): This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

11.2.504 DMA_CH3_TX_CONTROL — Offset 1284h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1284h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved
30:29	0h RW	Time Select (TFSEL): Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	Enhanced Descriptor Enable (EDSE): When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	Transmit QOS. (TQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Transmit Programmable Burst Length (TXPBL):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.</p> <p>To transfer more than 32 beats, perform the following steps:</p> <ol style="list-style-type: none"> 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. <p>Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.</p>
15	0h RW	<p>Ignore PBL Requirement (IPBL):</p> <p>When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA.</p> <p>Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.</p> <p>0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.</p>
14:13	0h RW	<p>TSE_MODE:</p> <p>TSE Mode</p> <ul style="list-style-type: none"> - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved <p>0x0 (TSO_USO): TSO/USO. 0x1 (UFWOC): UFO with Checksum. 0x2 (UFWOC): UFO without Checksum. 0x3 (RSVD): Reserved.</p>
12	0h RW	<p>TCP Segmentation Enabled (TSE):</p> <p>When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor. When this bit is set, the TxPBL value must be greater than 4.</p> <p>0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.</p>
11:5	0h RO	Reserved

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Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	Operate on Second Packet (OSF): When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	Transmit Channel Weight (TCW): This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	Start or Stop Transmission Command (ST): When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

11.2.505 DMA_CH3_RX_CONTROL — Offset 1288h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1288h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Rx Packet Flush. (RPF): When this bit is set to 1, then Ethernet Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the Ethernet Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled.

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	Reserved
27:24	0h RW	Rx AXI4 QOS. (RQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Receive Programmable Burst Length (RxPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	Reserved
14:4	000h RW	Receive Buffer size High (RBSZ_13_Y): RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO/V	Receive Buffer size Low (RBSZ_X_0): RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	Start or Stop Receive (SR): When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

11.2.506 DMA_CH3_TXDESC_LIST_HADDRESS — Offset 1290h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1290h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Transmit List (TDESHA): This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

11.2.507 DMA_CH3_TXDESC_LIST_ADDRESS — Offset 1294h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1294h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Start of Transmit List (TDESLA): This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.508 DMA_CH3_RXDESC_LIST_HADDRESS — Offset 1298h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1298h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Receive List (RDESHA): This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

11.2.509 DMA_CH3_RXDESC_LIST_ADDRESS — Offset 129Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 129Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Receive List (RDESLA): This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration

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Bit Range	Default & Access	Field Name (ID): Description
		- 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.510 DMA_CH3_TXDESC_TAIL_POINTER — Offset 12A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Transmit Descriptor Tail Pointer (TDTP): This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.511 DMA_CH3_RXDESC_TAIL_POINTER — Offset 12A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Receive Descriptor Tail Pointer (RDTP): This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.512 DMA_CH3_TXDESC_RING_LENGTH — Offset 12ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Transmit Descriptor Ring Length (TDRL): This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel® recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.513 DMA_CH3_RXDESC_RING_LENGTH — Offset 12B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Receive Descriptor Ring Length (RDRL): This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.514 DMA_CH3_INTERRUPT_ENABLE — Offset 12B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW	Normal Interrupt Summary Enable (NIE): When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: <ul style="list-style-type: none"> - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	Abnormal Interrupt Summary Enable (AIE): When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	Context Descriptor Error Enable (CDEE): When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	Fatal Bus Error Enable (FBEE): When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	Early Receive Interrupt Enable (ERIE): When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RO	reserved
9	0h RW	Receive Watchdog Timeout Enable (RWTE): When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.
8	0h RW	Receive Stopped Enable (RSE): When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	Receive Buffer Unavailable Enable (RBUE): When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	Receive Interrupt Enable (RIE): When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	Reserved
2	0h RW	Transmit Buffer Unavailable Enable (TBUE): When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	Transmit Stopped Enable (TXSE): When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	Transmit Interrupt Enable (TIE): When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

11.2.515 DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER — Offset 12B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CH*i*_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	Receive Interrupt Watchdog Timer Count Units (RWTU): This field indicates the number of system clock cycles corresponding to one unit in RWT field. <ul style="list-style-type: none"> - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	Reserved
7:0	00h RW	Receive Interrupt Watchdog Timer Count (RWT): This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(<i>#i</i>)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30].

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Bit Range	Default & Access	Field Name (ID): Description
		When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

11.2.516 DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS – Offset 12BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved
19:16	0h RO/V	Reference Slot Number (RSN): This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	Slot Interval Value (SIV): This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us
3:2	0h RO	Reserved
1	0h RW	Advance Slot Check (ASC): When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is <ul style="list-style-type: none"> - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	Enable Slot Comparison (ESC): When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is <ul style="list-style-type: none"> - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

11.2.517 DMA_CH3_CURRENT_APP_TXDESC — Offset 12C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Transmit Descriptor Address Pointer (CURTDESAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.518 DMA_CH3_CURRENT_APP_RXDESC — Offset 12CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Descriptor Address Pointer (CURRDESAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.519 DMA_CH3_CURRENT_APP_TXBUFFER_H — Offset 12D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTRH): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.520 DMA_CH3_CURRENT_APP_TXBUFFER — Offset 12D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Transmit Buffer Address Pointer (CURTBUFAPTR): The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

11.2.521 DMA_CH3_CURRENT_APP_RXBUFFER_H — Offset 12D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTRH): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.522 DMA_CH3_CURRENT_APP_RXBUFFER — Offset 12DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12DCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.523 DMA_CH3_STATUS — Offset 12E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

NOTE

The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h	Reserved

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Bit Range	Default & Access	Field Name (ID): Description
	RO	
21:19	0h RO/V	<p>Rx DMA Error Bits (REB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
18:16	0h RO/V	<p>Tx DMA Error Bits (TEB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface.</p> <ul style="list-style-type: none"> - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
15	0h RW	<p>Normal Interrupt Summary (NIS): Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt <p>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Normal Interrupt Summary status not detected.</p> <p>0x1 (ACTIVE): Normal Interrupt Summary status detected.</p>
14	0h RW	<p>Abnormal Interrupt Summary (AIS): Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error <p>Only unmasked bits affect the Abnormal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	Context Descriptor Error (CDE): This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	Fatal Bus Error (FBE): This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	Early Receive Interrupt (ERI): This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout (RWT): This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	Receive Process Stopped (RPS): This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	Receive Buffer Unavailable (RBU): This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	Receive Interrupt (RI):

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Bit Range	Default & Access	Field Name (ID): Description
		<p>This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>The reception remains in the Running state.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.</p>
5:3	0h RO	Reserved
2	0h RW	<p>Transmit Buffer Unavailable (TBU):</p> <p>This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions.</p> <p>To resume processing the Transmit descriptors, the application should do the following:</p> <ol style="list-style-type: none"> 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. <p>For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.</p>
1	0h RW	<p>Transmit Process Stopped (TPS):</p> <p>This bit is set when the transmission is stopped.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.</p>
0	0h RW	<p>Transmit Interrupt (TI):</p> <p>This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.</p>

11.2.524 DMA_CH3_MISS_FRAME_CNT — Offset 12E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH\${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RO/V	<p>Overflow status of the MFC Counter (MFC0):</p> <p>When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Miss Frame Counter overflow not occurred.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	Reserved
10:0	000h RO/V	Dropped Packet Counters (MFC): This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programming RPF field in DMA_CH\${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

11.2.525 DMA_CH3_RX_ERI_CNT — Offset 12ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ECh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	000h RO/V	ERI Counter (ECNT): When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

11.2.526 DMA_CH4_CONTROL — Offset 1300h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1300h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RO	Reserved Platform firmware & software will not set this field to 0x1.
23:21	0h RO	Reserved
20:18	0h RW	Descriptor Skip Length (DSL): This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.

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Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	Reserved
16	0h RW	8xPBL mode (PBLX8): When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	Reserved

11.2.527 DMA_CH4_RX_CONTROL – Offset 1308h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1308h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Rx Packet Flush (RPF): When this bit is set to 1, then Ethernet Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the Ethernet Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	Reserved
27:24	0h RW	Rx AXI4 QOS. (RQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Receive Programmable Burst Length (RXPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL.

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Bit Range	Default & Access	Field Name (ID): Description
		Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	Reserved
14:4	000h RW	Receive Buffer size High (RBSZ_13_Y): RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO/V	Receive Buffer size Low (RBSZ_X_0): RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	Start or Stop Receive (SR): When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

11.2.528 DMA_CH4_RXDESC_LIST_HADDRESS — Offset 1318h

The Channel Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1318h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	Start of Receive List (RDESHA): This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

11.2.529 DMA_CH4_RXDESC_LIST_ADDRESS — Offset 131Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 131Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	Start of Receive List (RDESLA): This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.530 DMA_CH4_RXDESC_TAIL_POINTER — Offset 1328h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1328h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h	Receive Descriptor Tail Pointer (RDTP):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.531 DMA_CH4_RXDESC_RING_LENGTH — Offset 1330h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1330h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Receive Descriptor Ring Length (RDRL): This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0xFF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.532 DMA_CH4_INTERRUPT_ENABLE — Offset 1334h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1334h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW	Normal Interrupt Summary Enable (NIE): When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.

continued...

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	<p>Abnormal Interrupt Summary Enable (AIE): When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register:</p> <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error <p>When this bit is reset, the abnormal interrupt summary is disabled.</p> <p>0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.</p>
13	0h RW	<p>Context Descriptor Error Enable (CDEE): When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled.</p> <p>0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.</p>
12	0h RW	<p>Fatal Bus Error Enable (FBEE): When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled.</p> <p>0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.</p>
11	0h RW	<p>Early Receive Interrupt Enable (ERIE): When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.</p> <p>0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.</p>
10	0h RO	Reserved
9	0h RW	<p>Receive Watchdog Timeout Enable (RWTE): When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled.</p> <p>0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.</p>
8	0h RW	<p>Receive Stopped Enable (RSE): When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.</p> <p>0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.</p>
7	0h RW	<p>Receive Buffer Unavailable Enable (RBUE): When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled.</p> <p>0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.</p>
6	0h RW	<p>Receive Interrupt Enable (RIE): When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.</p> <p>0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.</p>
5:0	0h	Reserved

Bit Range	Default & Access	Field Name (ID): Description
	RO	

11.2.533 DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1338h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1338h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	Receive Interrupt Watchdog Timer Count Units (RWTU): This field indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	Reserved
7:0	00h RW	Receive Interrupt Watchdog Timer Count (RWT): This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

11.2.534 DMA_CH4_CURRENT_APP_RXDESC — Offset 134Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 134Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Descriptor Address Pointer (CURRDESAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.535 DMA_CH4_CURRENT_APP_RXBUFFER_H – Offset 1358h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1358h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTRH): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.536 DMA_CH4_CURRENT_APP_RXBUFFER – Offset 135Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 135Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.537 DMA_CH4_STATUS – Offset 1360h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1360h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21:19	0h RO/V	Rx DMA Error Bits (REB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<p>-- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
18:16	0h RO/V	<p>Tx DMA Error Bits (TEB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
15	0h RW	<p>Normal Interrupt Summary (NIS): Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.</p>
14	0h RW	<p>Abnormal Interrupt Summary (AIS): Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.</p>
13	0h RW	<p>Context Descriptor Error (CDE): This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p>

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Bit Range	Default & Access	Field Name (ID): Description
		0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	Fatal Bus Error (FBE): This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	Early Receive Interrupt (ERI): This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout (RWT): This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	Receive Process Stopped (RPS): This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	Receive Buffer Unavailable (RBU): This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	Receive Interrupt (RI): This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	Reserved
2	0h	Transmit Buffer Unavailable (TBU):

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Bit Range	Default & Access	Field Name (ID): Description
	RW	<p>This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions.</p> <p>To resume processing the Transmit descriptors, the application should do the following:</p> <ol style="list-style-type: none"> 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. <p>For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.</p>
1	0h RW	<p>Transmit Process Stopped (TPS):</p> <p>This bit is set when the transmission is stopped.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.</p>
0	0h RW	<p>Transmit Interrupt (TI):</p> <p>This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.</p>

11.2.538 DMA_CH4_MISS_FRAME_CNT – Offset 1364h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH\${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1364h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RO/V	<p>Overflow status of the MFC Counter (MFCO):</p> <p>When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.</p>
14:11	0h RO	Reserved
10:0	000h RO/V	<p>Dropped Packet Counters (MFC):</p> <p>This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing</p> <p>RPF field in DMA_CH\${i}_Rx_Control register. The counter gets cleared when this register is read.</p> <p>Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

11.2.539 DMA_CH4_RX_ERI_CNT — Offset 136Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 136Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	000h RO/V	ERI Counter (ECNT): When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

11.2.540 DMA_CH5_CONTROL — Offset 1380h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1380h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved
24	0h RO	Reserved Platform firmware & software will not set this field to 0x1.
23:21	0h RO	Reserved
20:18	0h RW	Descriptor Skip Length (DSL): This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	Reserved
16	0h RW	8xPBL mode (PBLX8): When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	Reserved

11.2.541 DMA_CH5_RX_CONTROL — Offset 1388h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1388h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	Rx Packet Flush (RPF): When this bit is set to 1, then Ethernet Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the Ethernet Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	Reserved
27:24	0h RW	Rx AXI4 QOS. (RQOS): This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	Reserved
21:16	00h RW	Receive Programmable Burst Length (RXPBL): These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	Reserved
14:4	000h RW	Receive Buffer size High (RBSZ_13_Y): RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled.

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Bit Range	Default & Access	Field Name (ID): Description
		<p>Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).</p>
3:1	0h RO/V	<p>Receive Buffer size Low (RBSZ_X_0): RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).</p>
0	0h RW	<p>Start or Stop Receive (SR): When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.</p>

11.2.542 DMA_CH5_RXDESC_LIST_HADDRESS — Offset 1398h

The Channel Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1398h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RW	<p>Start of Receive List (RDESHA): This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.</p>

11.2.543 DMA_CH5_RXDESC_LIST_ADDRESS – Offset 139Ch

The Channel Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 139Ch	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Start of Receive List (RDESLA): This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.544 DMA_CH5_RXDESC_TAIL_POINTER – Offset 13A8h

The Channel Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A8h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0000000h RW	Receive Descriptor Tail Pointer (RDTP): This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	Reserved

11.2.545 DMA_CH5_RXDESC_RING_LENGTH — Offset 13B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved
9:0	000h RW	Receive Descriptor Ring Length (RDRL): This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0xFF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

11.2.546 DMA_CH5_INTERRUPT_ENABLE — Offset 13B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RW	Normal Interrupt Summary Enable (NIE): When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	Abnormal Interrupt Summary Enable (AIE): When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.

continued...

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	Context Descriptor Error Enable (CDEE): When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	Fatal Bus Error Enable (FBEE): When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	Early Receive Interrupt Enable (ERIE): When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout Enable (RWTE): When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.
8	0h RW	Receive Stopped Enable (RSE): When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	Receive Buffer Unavailable Enable (RBUE): When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	Receive Interrupt Enable (RIE): When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:0	0h RO	Reserved

11.2.547 DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER — Offset 13B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved
17:16	0h RW	Receive Interrupt Watchdog Timer Count Units (RWTU): This field indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	Reserved
7:0	00h RW	Receive Interrupt Watchdog Timer Count (RWT): This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

11.2.548 DMA_CH5_CURRENT_APP_RXDESC — Offset 13CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	Application Receive Descriptor Address Pointer (CURRDESAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.549 DMA_CH5_CURRENT_APP_RXBUFFER_H — Offset 13D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	00h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTRH): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.550 DMA_CH5_CURRENT_APP_RXBUFFER — Offset 13DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13DCh	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000000h RO/V	Application Receive Buffer Address Pointer (CURRBUFAPTR): The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

11.2.551 DMA_CH5_STATUS — Offset 13E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

NOTE

The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E0h	0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved
21:19	0h RO/V	Rx DMA Error Bits (REB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO/V	Tx DMA Error Bits (TEB): This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access

continued...

Bit Range	Default & Access	Field Name (ID): Description
		<ul style="list-style-type: none"> - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer <p>This field is valid only when the FBE bit is set. This field does not generate an interrupt.</p>
15	0h RW	<p>Normal Interrupt Summary (NIS):</p> <p>Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt <p>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.</p>
14	0h RW	<p>Abnormal Interrupt Summary (AIS):</p> <p>Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:</p> <ul style="list-style-type: none"> - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error <p>Only unmasked bits affect the Abnormal Interrupt Summary bit.</p> <p>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.</p>
13	0h RW	<p>Context Descriptor Error (CDE):</p> <p>This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.</p>
12	0h RW	<p>Fatal Bus Error (FBE):</p> <p>This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses.</p> <p>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.</p>
11	0h RW	<p>Early Receive Interrupt (ERI):</p> <p>This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory.</p> <p>In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.</p> <p>The setting of RI bit automatically clears this bit.</p>

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RO	Reserved
9	0h RW	Receive Watchdog Timeout (RWT): This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	Receive Process Stopped (RPS): This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	Receive Buffer Unavailable (RBU): This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	Receive Interrupt (RI): This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	Reserved
2	0h RW	Transmit Buffer Unavailable (TBU): This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	Transmit Process Stopped (TPS): This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected.

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	<p>Transmit Interrupt (TI): This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.</p> <p>0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.</p>

11.2.552 DMA_CH5_MISS_FRAME_CNT — Offset 13E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH\${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved
15	0h RO/V	<p>Overflow status of the MFC Counter (MFCO): When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.</p> <p>0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.</p>
14:11	0h RO	Reserved
10:0	000h RO/V	<p>Dropped Packet Counters (MFC): This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH\${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.</p>

11.2.553 DMA_CH5_RX_ERI_CNT — Offset 13ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved
11:0	000h	ERI Counter (ECNT):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

11.3 PHY Sublayer Registers Accessible via the MDIO Interface Controller

The Management Data Input/Output (MDIO) Interface is defined in IEEE Standard 802.3-2018:

Clause 22 – Chapter 22.2.4 of the IEEE standard specifies the MDIO interface and registers. The MAC device controlling the MDIO is called the Station Management (STA) entity. The STA issues MDIO frames that have the 2-bit, start-of-frame Symbol Time (ST) code of 01 to access registers. See Table below for the Clause 22 frame format and terminology.

Clause 45 – See Chapter 45 of the IEEE standard. This MDIO interface and register format are extensions to the two-signal MDIO Interface specified in Clause 22. For Clause 45, additional registers are added to the address space by defining MDIO frames that use a start-of-frame Symbol Time (ST) code of 00. See Table below for the Clause 45 frame format and terminology.

The Ethernet TSN Controller supports both formats. The C45E bit (bit 1) of the MAC_MDIO_Address register at MMIO offset 200h can be programmed to select the Clause 22 or Clause 45 mode of operation of the STA for the particular MDIO frame. The C45E bit must be programmed to support the capability of the PHY that is connected to MDIO.

The PHY sublayer, or grouping of sublayers, is an individually manageable entity referred to as an MDIO Manageable Device (MMD).

Table 21. MDIO Clause 22 Management Frame Format

Operation	32-bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	PHY Address (PHYAD)	PHY Register Address (REGAD)	2-Bit Turn-around (TA) Time	Data (16 bits)	High-Z (Idle)
Write	1111...1	01	01	AAAAAA	RRRRR	10	16-bit Data to be written to the register	Z
Read	1111...1	01	10	AAAAAA	RRRRR	Z0	16-bit Data read from the register	Z

For the Clause 22 frame, the PHY Address (PHYAD) selects one of 32 PHYs attached to the MDIO interface. The PHY Register Address (REGAD) selects one of 32 16-bit registers within each MMD.

Table 22. MDIO Clause 45 Management Frame Format

Operation	32-bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	Port Address (PRTAD)	Device Address (DEVAD)	2-Bit Turn-around (TA) Time	Address/ Data (16 bits)	High-Z (Idle)
Address	1111...1	00	00	ppppp	EEEEEE	Z0	16-bit Address of the register to be accessed on the next cycle	z
Write	1111...1	00	01	ppppp	EEEEEE	Z0	16-bit Data to be written to the register	z
Post-Read-Increment Address	1111...1	00	10	ppppp	EEEEEE	Z0	16-bit Data read from the register	z
Read	1111...1	00	11	ppppp	EEEEEE	Z0	16-bit Data read from the register	z

For the Clause 45 frame, the Port Address (PRTAD) selects one of 32 Ports attached to the MDIO interface. The Device Address (DEVAD) selects one of 32 unique MDDs per Port. Notice that the register address and register data are separate MDIO frames.

11.3.1 MDIO – PCS PHY Sublayer Registers – PHY Port Address 16h

The MAC uses the GMII as the data interface to the PHY sublayers of the Ethernet LAN Controller including the Physical Coding Sublayer (PCS). The MAC uses the MDIO as the configuration and management interface to the PHY sublayers. This section describes the PCS MDIO registers which follow the IEEE 802.3 standard register sets for the different MMIO Management Devices (MMD).

The PCS PHY sublayer is an IEEE Std 802.3 Clause-45-capable MDIO entity with the following IEEE 802.3 MDIO frame fields:

- Start-of-Frame Symbol Time (ST) 2-bit code: 00b – Indicates a Clause 45 MDIO frame.
- Port Address (PRTAD) 5-bit ID: 10110b (16h) – This Port contains two MMDs:
 - MMD (DEVAD) 5-bit ID: 11110b (1Eh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h through 000Fh. This MMD is named Vendor-Specific 1 (Control MMD). The registers are used to control the other MMDs of the LAN Controller.
 - MMD (DEVAD) 5-bit ID: 11111b (1Fh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h through 0E2h. This MMD is named Vendor-Specific MII MMD (VR MII MMD). [SR_VSMMD_PMA_ID1 DWC_XCPS \(SR_VSMMD_PMA_ID1\)](#) - Offset 1E00000000h on page 483

Table 23. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Eh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1E0000 0000h	2	SR_VSMMMD_PMA_ID1 DWC_XCPS (SR_VSMMMD_PMA_ID1) - Offset 1E00000000h on page 483 SR_VSMMMD_PMA_ID1 DWC_XCPS (SR_VSMMMD_PMA_ID1) - Offset 1E00000000h on page 483	0000h
1E0000 0002h	2	SR_VSMMMD_PMA_ID2 DWC_XCPS_ (SR_VSMMMD_PMA_ID2) - Offset 1E00000002h on page 484 SR_VSMMMD_PMA_ID2 DWC_XCPS_ (SR_VSMMMD_PMA_ID2) - Offset 1E00000002h on page 484	0000h
1E0000 0004h	2	SR_VSMMMD_DEV_ID1 DWC_XCPS (SR_VSMMMD_DEV_ID1) - Offset 1E00000004h on page 484	0000h
1E0000 0006h	2	SR_VSMMMD_DEV_ID2 DWC_XCPS (SR_VSMMMD_DEV_ID2) - Offset 1E00000006h on page 484 SR_VSMMMD_DEV_ID2 DWC_XCPS (SR_VSMMMD_DEV_ID2) - Offset 1E00000006h on page 484 SR_VSMMMD_DEV_ID2 DWC_XCPS (SR_VSMMMD_DEV_ID2) - Offset 1E00000006h on page 484	000h
1E0000 0008h	2	SR_VSMMMD_PCS_ID1 DWC_XCPS (SR_VSMMMD_PCS_ID1) - Offset 1E00000008h on page 485	7996h
1E0000 000Ah	2	SR_VSMMMD_PCS_ID2 DWC_XCPS (SR_VSMMMD_PCS_ID2) - Offset 1E0000000Ah on page 485 SR_VSMMMD_PCS_ID2 DWC_XCPS (SR_VSMMMD_PCS_ID2) - Offset 1E0000000Ah on page 485	CED0h
1E0000 000Ch	2	SR_VSMMMD_AN_ID1 DWC_XCPS (SR_VSMMMD_AN_ID1) - Offset 1E0000000Ch on page 486 SR_VSMMMD_AN_ID1 DWC_XCPS (SR_VSMMMD_AN_ID1) - Offset 1E0000000Ch on page 486	0000h
1E0000 000Eh	2	SR_VSMMMD_AN_ID2 DWC_XCPS (SR_VSMMMD_AN_ID2) - Offset 1E0000000Eh on page 486 SR_VSMMMD_AN_ID2 DWC_XCPS (SR_VSMMMD_AN_ID2) - Offset 1E0000000Eh on page 486	0000h
1E0000 0010h	2	SR_VSMMMD_STS DWC_XCPS (SR_VSMMMD_STS) - Offset 1E00000010h on page 486	8000h
1E0000 0012h	2	SR_VSMMMD_CTRL DWC_XCPS (SR_VSMMMD_CTRL) - Offset 1E00000012h on page 487	0004h
1E0000 001Ch	2	SR_VSMMMD_PKGID1 DWC_XCPS (SR_VSMMMD_PKGID1) - Offset 1E0000001Ch on page 487	0000h
1E0000 001Eh	2	SR_VSMMMD_PKGID2 DWC_XCPS (SR_VSMMMD_PKGID2) - Offset 1E0000001Eh on page 488	0000h

11.3.1.1 SR_VSMMMD_PMA_ID1 DWC_XCPS (SR_VSMMMD_PMA_ID1) - Offset 1E00000000h

Type	Size	Offset	Default
MMIO	16 bit	1E00000000h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None
Bit Range		Default & Access	Field Name (ID): Description
15:0		0h RO	Reserved

11.3.1.2 SR_VSMMD_PMA_ID2 DWC_XPCS_ (SR_VSMMD_PMA_ID2) - Offset 1E00000002h

SR Control MMD PMA Device Identifier Register 2

NOTE

Bit definitions are the same as SR_VSMMD_PMA_ID1, Offset 1E00000000h.

11.3.1.3 SR_VSMMD_DEV_ID1 DWC_XCPS (SR_VSMMD_DEV_ID1) - Offset 1E00000004h

SR Control MMD Device Identifier Register 1

Type	Size	Offset	Default
MMIO	16 bit	1E00000004h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	VSDOUI_3_18 DWC_XCPS (VSDOUI_3_18): Organizationally Unique Identifier [3:18] for Vendor-Specific MMD1 This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The DWC_xcps offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. You can configure the value of each MMD using coreConsultant. Access Type:- RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. RO: For all other configurations.

11.3.1.4 SR_VSMMD_DEV_ID2 DWC_XCPS (SR_VSMMD_DEV_ID2) - Offset 1E00000006h

SR Control MMD Device Identifier Register 2

Type	Size	Offset	Default
MMIO	16 bit	1E00000006h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW	VSDOUI_19_24 DWC_XCPS (VSDOUI_19_24): Organizationally Unique Identifier [19:24] for Vendor-Specific MMD1 This field contains Bits [24:19] of the device manufacturer's 24-bit OUI. The DWC_xcps offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. You can configure the value of each MMD using coreConsultant. Access Type:- RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. RO: For all other configurations.
9:4	00h	VSDMMN_5_0 DWC_XCPS (VSDMMN_5_0):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	Model Number for Vendor-Specific MMD1 This field contains the 6-bit Model number of vendor-specific MMD1. You can configure the default value through coreConsultant. Access Type:- RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. - RO: For all other configurations.
3:0	0h RW	VSDRN_3_0 DWC_XCPS (VSDRN_3_0): Revision Number for Vendor-Specific MMD1 This field contains the 4-bit Revision number of the vendor-specific MMD1. You can configure the default value through coreConsultant. Access Type:- RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. -RO: For all other configurations.

11.3.1.5 SR_VSMMD_PCS_ID1_DWC_XCPS (SR_VSMMD_PCS_ID1) - Offset 1E00000008h

SR Control MMD PCS Device Identifier Register 1

Type	Size	Offset	Default
MMIO	16 bit	1E00000008h	7996h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	7996h RW	PCSDOUI_3_18 DWC_XCPS (PCSDOUI_3_18): Organizationally Unique Identifier[3:18] for PCS MMD This field contains Bits[18:3] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer.The default value of this register is similar to the default value of SR XS or PCS MMD Device Identifier Register 1. The value written in this register is reflected in SR XS or PCS MMD Device Identifier Register 1. Access Type:- RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. - RO: For all other configurations.

11.3.1.6 SR_VSMMD_PCS_ID2_DWC_XCPS (SR_VSMMD_PCS_ID2) - Offset 1E0000000Ah

SR Control MMD PCS Device Identifier Register 2

Type	Size	Offset	Default
MMIO	16 bit	1E0000000Ah	CED0h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	33h RW	PCSDOUI_19_24 DWC_XCPS (PCSDOUI_19_24):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Organizationally Unique Identifier[19:24] for PCS MMD This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. - RO: For all other configurations.
9:4	2Dh RW	PCSDMMN_5_0 DWC_XCPS (PCSDMMN_5_0): Model Number for XS or PCS MMD This field contains the 6-bit Model number of vendor-specific XS or PCS MMD. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled - RO: For all other configurations.
3:0	0h RW	PCSDRN_3_0 DWC_XCPS (PCSDRN_3_0): Revision Number for XS or PCS MMD This field contains the 4-bit Revision number of vendor-specific XS or PCS MMD. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled - RO: For all other configurations.

11.3.1.7 SR_VSMMD_AN_ID1 DWC_XCPS (SR_VSMMD_AN_ID1) - Offset 1E0000000Ch

SR Control MMD AN Device Identifier Register 1

NOTE

Bit definitions are the same as SR_VSMMD_PMA_ID1, Offset 1E00000000h.

11.3.1.8 SR_VSMMD_AN_ID2 DWC_XCPS (SR_VSMMD_AN_ID2) - Offset 1E0000000Eh

SR Control MMD AN Device Identifier Register 2

NOTE

Bit definitions are the same as SR_VSMMD_PMA_ID1, Offset 1E00000000h.

11.3.1.9 SR_VSMMD_STS DWC_XCPS (SR_VSMMD_STS) - Offset 1E00000010h

SR Control MMD Status Register

Type	Size	Offset	Default
MMIO	16 bit	1E00000010h	8000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:14	2h RO/V	VSDP DWC_XCPS (SVSDP): Control MMD Device Present This field indicates if the control MMD device is present and responding to this address: - 10: Device responding at this address - 11, 01, or 00: No device responding at this address
13:0	0h RO	Reserved

11.3.1.10 SR_VSMMD_CTRL DWC_XCPS (SR_VSMMD_CTRL) - Offset 1E00000012h

SR Control MMD Control Register

Type	Size	Offset	Default
MMIO	16 bit	1E00000012h	0004h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4	0h RW	FASTSIM DWC_XCPS (FASTSIM): Fast Simulation Enable When set, this bit indicates that the Fast simulation is enabled. When this bit is set to 1, all IEEE Std 802.3 defined long timers, implemented in the DWC_xpcs are reduced to shorter time period to reduce the simulation time. The long timers are implemented in Clause 73 and Clause 37 autonegotiation modules and also EEE Tx and Rx modules.
3	0h RO	Reserved
2	1h RW	MII_MMD_EN DWC_XCPS (MII_MMD_EN): VS MMD Enable When set, this bit indicates that the vendor-specific MMD1 device is accessible. When reset, this bit indicates that the vendor-specific MMD2 (MII MMD) device is not accessible.
1	0h RO	Reserved

11.3.1.11 SR_VSMMD_PKGID1 DWC_XCPS (SR_VSMMD_PKGID1) - Offset 1E0000001Ch

SR Control MMD Package Identifier Register 1

NOTE

Bit definitions are the same as SR_VSMMD_PMA_ID1, Offset 1E00000000h.

11.3.1.12 SR_VSMMD_PKGID2 DWC_XCPS (SR_VSMMD_PKGID2) - Offset 1E0000001Eh

SR Control MMD Package Identifier Register 2 Note: The values written in the fields of this register are reflected in the corresponding fields of the following registers: - SR_PMA_PKG2 Register - SR_XS_PCS_PKG2 Register - SR_AN_PKG2 Register

NOTE

Bit definitions are the same as SR_VSMMD_PMA_ID1, Offset 1E00000000h.

Table 24. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Fh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F0000 0000h	2	SR_MII_CTRL DWC_XCPS (SR_MII_CTRL) - Offset 1F00000000h on page 492	1140h
1F0000 0002h	2	SR_MII_STS DWC_XCPS (SR_MII_STS) - Offset 1F00000002h on page 494	0109h
1F0000 0004h	2	SR_MII_DEV_ID1 DWC_XCPS (SR_MII_DEV_ID1) - Offset 1F00000004h on page 495	7996h
1F0000 0006h	2	SR_MII_DEV_ID2 DWC_XCPS (SR_MII_DEV_ID2) - Offset 1F00000006h on page 496	CED0h
1F0000 0008h	2	SR_MII_AN_ADV DWC_XCPS (SR_MII_AN_ADV) - Offset 1F00000008h on page 496	0020h
1F0000 000Ah	2	SR_MII_LP_BABL DWC_XCPS (SR_MII_LP_BABL) - Offset 1F0000000Ah on page 497	0000h
1F0000 000Ch	2	SR_MII_AN_EXPN DWC_XCPS (SR_MII_AN_EXPN) - Offset 1F0000000Ch on page 498	0000h
1F0000 001Eh	2	SR_MII_MMD_EXT_STS DWC_XCPS (SR_MII_EXT_STS) - Offset 1F0000001Eh on page 499	C000h
1F0000 0E10h	2	SR_MII_TIME_SYNC_ABL DWC_XCPS (SR_MII_TIME_SYNC_ABL) - Offset 1F00000E10h on page 499	0003h
1F0000 0E12h	2	SR_MII_TIME_SYNC_TX_MAX_DLY_LWR DWC_XCPS (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR) - Offset 1F00000E12h on page 500	0038h
1F0000 0E14h	2	SR_MII_TIME_SYNC_TX_MAX_DLY_UPR DWC_XCPS (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR) - Offset 1F00000E14h on page 500	0000h
1F0000 0E16h	2	SR_MII_TIME_SYNC_TX_MIN_DLY_LWR DWC_XCPS (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR) - Offset 1F00000E16h on page 501	0038h
1F0000 0E18h	2	SR_MII_TIME_SYNC_TX_MIN_DLY_UPR DWC_XCPS (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR) - Offset 1F00000E18h on page 501	0000h
1F0000 0E1Ah	2	SR_MII_TIME_SYNC_RX_MAX_DLY_LWR DWC_XCPS (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR) - Offset 1F00000E1Ah on page 502	00B8h
1F0000 0E1Ch	2	SR_MII_TIME_SYNC_RX_MAX_DLY_UPR DWC_XCPS (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR) - Offset 1F00000E1Ch on page 502	0000h
1F0000 0E1Eh	2	SR_MII_TIME_SYNC_RX_MIN_DLY_LWR DWC_XCPS (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR) - Offset 1F00000E1Eh on page 502	0088h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F0000 0E20h	2	SR_MII_TIME_SYNC_RX_MIN_DLY_UPR DWC_XCPS (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR) - Offset 1F00000E20h on page 503	0000h
1F0001 0000h	2	VR_MII_DIG_CTRL1 DWC_XCPS (VR_MII_DIG_CTRL1) - Offset 1F00010000h on page 503	2400h
1F0001 0002h	2	VR_MII_AN_CTRL DWC_XCPS (VR_MII_AN_CTRL) - Offset 1F00010002h on page 506	0000h
1F0001 0004h	2	VR_MII_AN_INTR_STS DWC_XCPS (VR_MII_AN_INTR_STS) - Offset 1F00010004h on page 507	000Ah
1F0001 0006h	2	VR_MII_TC DWC_XCPS (VR_MII_TC) - Offset 1F00010006h on page 508	0000h
1F0001 000Ah	2	VR_MII_DBG_CTRL DWC_XCPS (VR_MII_DBG_CTRL) - Offset 1F0001000Ah on page 508	0000h
1F0000 000Ch	2	VR_MII_EEE_MCTRL0 DWC_XCPS (VR_MII_EEE_MCTRL0) - Offset 1F0001000Ch on page 509	899Ch
1F0001 0010h	2	VR_MII_EEE_TXTIMER DWC_XCPS (VR_MII_EEE_TXTIMER) - Offset 1F00010010h on page 511	0000h
1F0001 0012h	2	VR_MII_EEE_RXTIMER DWC_XCPS (VR_MII_EEE_RXTIMER) - Offset 1F00010012h on page 511	0000h
1F0001 0014h	2	VR_MII_LINK_TIMER_CTRL DWC_XCPS (VR_MII_LINK_TIMER_CTRL) - Offset 1F00010014h on page 512	0000h
1F0001 0016h	2	VR_MII_EEE_MCTRL1 DWC_XCPS (VR_MII_EEE_MCTRL1) - Offset 1F00010016h on page 513	0000h
1F0001 0020h	2	VR_MII_DIG_STS DWC_XCPS (VR_MII_DIG_STS) - Offset 1F00010020h on page 513	0010h
1F0001 0022h	2	VR_MII_ICG_ERRCNT1 DWC_XCPS (VR_MII_ICG_ERRCNT1) - Offset 1F00010022h on page 514	0000h
1F0001 0030h	2	VR_MII_MISC_STS DWC_XCPS (VR_MII_MISC_STS) - Offset 1F00010030h on page 515	0000h
1F0001 0040h	2	VR_MII_RX_LSTS DWC_XCPS (VR_MII_RX_LSTS) - Offset 1F00010040h on page 515	0000h
1F0000 0060h	2	VR_MII_MP_12G_16G_25G_TX_GENCTRL0 DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_GENCTRL0) - Offset 1F00010060h on page 516	1000h
1F0001 0062h	2	VR_MII_MP_12G_16G_25G_TX_GENCTRL1 DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_GENCTRL1) - Offset 1F00010062h on page 517	1510h
1F0001 0064h	2	VR_MII_MP_12G_16G_TX_GENCTRL2 DWC_XCPS (VR_MII_MP_12G_16G_TX_GENCTRL2) - Offset 1F00010064h on page 518	0100h
1F0001 0066h	2	VR_MII_MP_12G_16G_25G_TX_BOOST_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_BOOST_CTRL) - Offset 1F00010066h on page 518	000Fh
1F0001 0068h	2	VR_MII_MP_12G_16G_25G_TX_RATE_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_RATE_CTRL) - Offset 1F00010068h on page 519	0006h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F0001006Ah	2	VR_MII_MP_12G_16G_25G_TX_POWER_STATE_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_POWER_STATE_CTRL) - Offset 1F0001006Ah on page 519	0000h
1F0001006Ch	2	VR_MII_MP_12G_16G_25G_TX_EQ_CTRL0 DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_EQ_CTRL0) - Offset 1F0001006Ch on page 520	2800h
1F0001006Eh	2	VR_MII_MP_12G_16G_25G_TXEQ_CTRL1 DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_EQ_CTRL1) - Offset 1F0001006Eh on page 520	0000h
1F00010078h	2	VR_MII_MP_16G_25G_TX_GENCTRL3 DWC_XCPS (VR_MII_MP_16G_25G_TX_GENCTRL3) - Offset 1F00010078h on page 521	0000h
1F0001007Ah	2	VR_MII_MP_16G_25G_TX_GENCTRL4 DWC_XCPS (VR_MII_MP_16G_25G_TX_GENCTRL4) - Offset 1F0001007Ah on page 521	0000h
1F0001007Ch	2	VR_MII_MP_16G_25G_TX_MISC_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_TX_MISC_CTRL0) - Offset 1F0001007Ch on page 522	0000h
1F00010080h	2	VR_MII_MP_12G_16G_25G_TX_STS DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_STS) - Offset 1F00010080h on page 522	0000h
1F000100A0h	2	VR_MII_MP_12G_16G_25G_RX_GENCTRL0 DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_GENCTRL0) - Offset 1F000100A0h on page 523	0101h
1F000100A2h	2	VR_MII_MP_12G_16G_25G_RX_GENCTRL1 DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_GENCTRL1) - Offset 1F000100A2h on page 524	0100h
1F000100A4h	2	VR_MII_MP_12G_16G_25G_RX_GENCTRL2 DWC_XCPS (VR_MII_MP_12G_16G_RX_GENCTRL2) - Offset 1F000100A4h on page 524	0100h
1F000100A6h	2	VR_MII_MP_12G_16G_25G_RX_GENCTRL3 DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_GENCTRL3) - Offset 1F000100A6h on page 525	0002h
1F000100A8h	2	VR_MII_MP_12G_16G_25G_RX_RATE_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_RATE_CTRL) - Offset 1F000100A8h on page 526	0003h
1F000100AAh	2	VR_MII_MP_12G_16G_25G_RX_POWER_STATE_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_POWER_STATE_CTRL) - Offset 1F000100AAh on page 526	0000h
1F000100ACh	2	VR_MII_MP_12G_16G_25G_RX_CDR_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_CDR_CTRL) - Offset 1F000100ACh on page 527	0000h
1F000100AEh	2	VR_MII_MP_12G_16G_25G_RX_ATTN_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_ATTN_CTRL) - Offset 1F000100AEh on page 527	0000h
1F000100B0h	2	VR_MII_MP_16G_25G_RX_EQ_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_EQ_CTRL0) - Offset 1F000100B0h on page 528	4406h
1F000100B8h	2	VR_MII_MP_12G_16G_25G_RX_EQ_CTRL4 DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_EQ_CTRL4) - Offset 1F000100B8h on page 528	0010h
1F000100BAh	2	VR_MII_MP_16G_25G_RX_EQ_CTRL5 DWC_XCPS (VR_MII_MP_16G_25G_RX_EQ_CTRL5) - Offset 1F000100BAh on page 529	0000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F000100BCh	2	VR_MII_MP_12G_16G_25G_DFE_TAP_CTRL0 DWC_XCPS (VR_MII_MP_12G_16G_25G_DFE_TAP_CTRL0) - Offset 1F000100BCh on page 530	0000h
1F000100C0h	2	VR_MII_MP_12G_16G_25G_RX_STS DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_STS) - Offset 1F000100C0h on page 530	0000h
1F000100C2h	2	VR_MII_MP_16G_25G_RX_PPM_STS0 DWC_XCPS (VR_MII_MP_16G_25G_RX_PPM_STS0) - Offset 1F000100C2h on page 531	0000h
1F000100C8h	2	VR_MII_MP_16G_RX_CDR_CTRL1 DWC_XCPS (VR_MII_MP_16G_RX_CDR_CTRL1) - Offset 1F000100C8h on page 531	0110h
1F000100CAh	2	VR_MII_MP_16G_25G_RX_PPM_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_PPM_CTRL0) - Offset 1F000100CAh on page 532	0013h
1F000100D0h	2	VR_MII_MP_16G_25G_RX_GENCTRL4 DWC_XCPS (VR_MII_MP_16G_25G_RX_GENCTRL4) - Offset 1F000100D0h on page 532	0100h
1F000100D2h	2	VR_MII_MP_16G_25G_RX_MISC_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_MISC_CTRL0) - Offset 1F000100D2h on page 533	0047h
1F000100D6h	2	VR_MII_MP_16G_25G_RX_IQ_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_IQ_CTRL0) - Offset 1F000100D6h on page 533	0000h
1F000100E0h	2	VR_MII_MP_12G_16G_25G_MPLL_CMN_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_MPLL_CMN_CTRL) - Offset 1F000100E0h on page 534	0011h
1F000100E2h	2	VR_MII_MP_12G_16G_MPLLA_CTRL0 DWC_XCPS (VR_MII_MP_12G_16G_MPLLA_CTRL0) - Offset 1F000100E2h on page 534	00C1h
1F000100E4h	2	VR_MII_MP_16G_MPLLA_CTRL1 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL1) - Offset 1F000100E4h on page 535	3100h
1F000100E6h	2	VR_MII_MP_12G_16G_MPLLA_CTRL2 DWC_XCPS (VR_MII_MP_12G_16G_MPLLA_CTRL2) - Offset 1F000100E6h on page 535	0200h
1F000100E8h	2	VR_MII_MP_12G_16G_MPLL_B_CTRL0 DWC_XCPS (VR_MII_MP_12G_16G_MPLL_B_CTRL0) - Offset 1F000100E8h on page 536	00CEh
1F000100EAh	2	VR_MII_MP_16G_MPLL_B_CTRL1 DWC_XCPS (VR_MII_MP_16G_MPLL_B_CTRL1) - Offset 1F000100EAh on page 537	3100h
1F000100EcH	2	VR_MII_MP_12G_16G_MPLL_B_CTRL2 DWC_XCPS (VR_MII_MP_12G_16G_MPLL_B_CTRL2) - Offset 1F000100EcH on page 537	029Eh
1F000100EEh	2	VR_MII_MP_16G_MPLLA_CTRL3 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL3) - Offset 1F000100EEh on page 538	F01Ch
1F000100F0h	2	VR_MII_MP_16G_MPLL_B_CTRL3 DWC_XCPS (VR_MII_MP_16G_MPLL_B_CTRL3) - Offset 1F000100F0h on page 538	A02Ch
1F000100F2h	2	VR_MII_MP_16G_MPLLA_CTRL4 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL4) - Offset 1F000100F2h on page 539	0000h
1F000100F4h	2	VR_MII_MP_16G_MPLLA_CTRL5 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL5) - Offset 1F000100F4h on page 539	0000h
1F000100F6h	2	VR_MII_MP_16G_MPLL_B_CTRL4 DWC_XCPS (VR_MII_MP_16G_MPLL_B_CTRL4) - Offset 1F000100F6h on page 540	0000h
1F000100F8h	2	VR_MII_MP_16G_MPLL_B_CTRL5 DWC_XCPS (VR_MII_MP_16G_MPLL_B_CTRL5) - Offset 1F000100F8h on page 540	0000h

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Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F00010120h	2	VR_MII_MP_12G_16G_25G_MISC_CTRL0 DWC_XCPS (VR_MII_MP_12G_16G_25G_MISC_CTRL0) - Offset 1F00010120h on page 541	5100h
1F00010122h	2	VR_MII_MP_12G_16G_25G_REF_CLK_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_REF_CLK_CTRL) - Offset 1F00010122h on page 542	0001h
1F00010124h	2	VR_MII_MP_12G_16G_25G_VCO_CAL_LD0 DWC_XCPS (VR_MII_MP_12G_16G_25G_VCO_CAL_LD0) - Offset 1F00010124h on page 543	05B2h
1F0001012Ch	2	VR_MII_MP_16G_25G_VCO_CAL_REF0 DWC_XCPS (VR_MII_MP_16G_25G_VCO_CAL_REF0) - Offset 1F0001012Ch on page 543	0007h
1F00010130h	2	VR_MII_MP_12G_16G_25G_MISC_STS DWC_XCPS (VR_MII_MP_12G_16G_25G_MISC_STS) - Offset 1F00010130h on page 543	0400h
1F00010132h	2	VR_MII_MP_12G_16G_25G_MISC_CTRL1 DWC_XCPS (VR_MII_MP_12G_16G_25G_MISC_CTRL1) - Offset 1F00010132h on page 544	FFFFh
1F00010136h	2	VR_MII_MP_12G_16G_25G_SRAM DWC_XCPS (VR_MII_MP_12G_16G_25G_SRAM) - Offset 1F00010136h on page 545	0001h
1F00010138h	2	VR_MII_MP_16G_25G_MISC_CTRL2 DWC_XCPS (VR_MII_MP_16G_25G_MISC_CTRL2) - Offset 1F00010138h on page 545	0001h
1F00010140h	2	VR_MII_SNPS_CR_CTRL DWC_XCPS (VR_MII_SNPS_CR_CTRL) - Offset 1F00010140h on page 546	0000h
1F00010142h	2	VR_MII_SNPS_CR_ADDR DWC_XCPS (VR_MII_SNPS_CR_ADDR) - Offset 1F00010142h on page 546	0000h
1F00010144h	2	VR_MII_SNPS_CR_DATA DWC_XCPS (VR_MII_SNPS_CR_DATA) - Offset 1F00010144h on page 547	0000h
1F000101C2h	2	VR_MII_DIG_CTRL2 DWC_XCPS (VR_MII_DIG_CTRL2) - Offset 1F000101C2h on page 547	0000h
1F000101C4h	2	VR_MII_DIG_ERRCNT_SEL DWC_XCPS (VR_MII_DIG_ERRCNT_SEL) - Offset 1F000101C4h on page 548	0000h

11.3.1.13 SR_MII_CTRL DWC_XCPS (SR_MII_CTRL) - Offset 1F00000000h

SR MII MMD Control Register The host can use this register to control (enable or disable) some of the features supported by the DWC_Xcps with 1G (1000BASE-X) or USXGMII support and Clause 37 auto-negotiation support.

Type	Size	Offset	Default
MMIO	16 bit	1F00000000h	1140h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h	RST DWC_XCPS (RST):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the software reset process in which all internal blocks are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is self-cleared when PSEQ_STATE in VR_XS_PCS_DIG_STS Register is equal to 3'b100, that is, Tx/Rx clocks are stable and in Power_Good state. Note: For description of read or write access for registers during reset process, see "Special Case Register Access" section of the Databook.
14	0h RW	LBE DWC_XCP (LBE): Loopback Enable When set, this bit loops the PHY Tx lanes back to the PHY Rx lanes. - 0: The DWC_xpcs de-asserts xpcs_loopback_en_o signal. - 1: The DWC_xpcs asserts xpcs_loopback_en_o signal.
13	0h RW	SS13 DWC_XCP (SS13): Speed Selection (LSB) This bit, along with the SS6 bit and SS5 bit of this register, indicates the speed. For USXGMII configurations: - When SS5=1, SS6=0 and SS13=1, speed is 5 Gbps - When SS5=1, SS6=0 and SS13=0, speed is 2.5 Gbps - When SS5=0, SS6=1 and SS13=1, speed is 10 Gbps - When SS5=0, SS6=1 and SS13=0, speed is 1000 Mbps - When SS5=0, SS6=0 and SS13=1, speed is 100 Mbps - When SS5=0, SS6=0 and SS13=0, speed is 10 Mbps For SGMII configurations: - When SS6=1 and SS13=0, speed is 1000 Mbps - When SS6=0 and SS13=1, speed is 100 Mbps - When SS6=0 and SS13=0, speed is 10 Mbps This bit is reserved when SGMII_EN = Disabled and QSGMII_EN=Disabled and USXGMII_EN = Disabled.
12	1h RW	AN_ENABLE DWC_XPCS (AN_ENABLE): Enable Auto-Negotiation When set to 1, this bit enables the Clause 37 autonegotiation process.
11	0h RW	LPM DWC_XCP (LPM): Power-Down Mode This bit controls the power-down mode of the DWC_xpcs. - 0: Normal operation - 1: The DWC_xpcs goes to the power-down mode along with the PHY. For non-Synopsys PHY, the xpcs_pdown_o port is asserted. For Synopsys PHY, the DWC_xpcs does the following to trigger the power-down mode: - Turns off the PHY Receiver and Transmitter - Switches off all the clocks When the host clears this bit, the DWC_xpcs resumes the normal operation. In a Synopsys PHY configuration, after clearing this bit, the host must wait until Bits[4:2] of VR_XS_PCS_DIG_STS Register indicate that the DWC_xpcs is in the normal state. Note: For information about read or write access to registers during power-down mode, see "Special Case Register Access" section of the Databook.
10	0h RO	Reserved
9	0h RW	RESTART_AN DWC_XCP (RESTART_AN): Restart Auto-Negotiation (RW,SC Type) When the host writes this bit, the DWC_xpcs initiates the auto-negotiation process. This bit is used to restart the auto-negotiation which is already initiated by setting Bit 12. The DWC_xpcs clears this bit after restarting the auto-negotiation.
8	1h RW	DUPLEX_MODE DWC_XCP (DUPLEX_MODE): Duplex Mode This bit specifies the duplex mode of the DWC_xpcs. - 0: Half duplex - 1: Full duplex If Bit 12 is set to 0, this bit determines the PHY link duplex mode. If Bit 12 is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 autonegotiation process. Note: USXGMII mode supports only FULL duplex mode, irrespective of the value programmed to this bit.
7	0h RO	Reserved
6	1h RW	SS6 DWC_XCP (SS6): Speed Selection This bit, along with the SS13 bit (and SS5 bit, in case of USXGMII configuration) of this register indicates the speed. For more information, see description of the SS13 bit. This bit is reserved when SGMII_EN = Disabled and QSGMII_EN =Disabled and USXGMII_EN=Disabled.
5:0	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	

11.3.1.14 SR_MII_STS DWC_XPCS (SR_MII_STS) - Offset 1F00000002h

SR MII MMD Control Register The host can use this register to know the features supported by the DWC_xcps in the 1000BASE-X mode. Note: This register is present if the selected configuration has 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	1F00000002h	0109h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	ABL100T4 DWC_XPCS (ABL100T4): 100BASE-T4 Ability The DWC_xpcs always returns 0 because it does not support this functionality.
14	0h RO/V	FD100ABL DWC_XPCS (FD100ABL): 100BASE-X Full-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
13	0h RO/V	HD100ABL DWC_XPCS (HD100ABL): 100BASE-X Half-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
12	1h RO/V	FD10ABL DWC_XPCS (FD10ABL): 10 Mbps Full-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
11	0h RO/V	HD10ABL DWC_XPCS (HD10ABL): 10 Mbps Half-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
10	0h RO/V	FD100T DWC_XPCS (FD100T): 100BASE-T2 Full-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
9	0h RO/V	HD100T DWC_XPCS (HD100T): 100BASE-T2 Half-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
8	1h RO/V	EXT_STS_ABL DWC_XPCS (EXT_STS_ABL): Extended Status Information - 0: No Extended Status information is present at register address 16'h000F of this MMD device. - 1: Extended Status information is present at register address 16'h000F of this MMD device. DWC_xpcs returns this bit as 1.
7	0h RO/V	UN_DIR_ABL DWC_XPCS (UN_DIR_ABL): Unidirectional Ability - 1: The DWC_xcps is able to transmit GMII irrespective of whether device has determined the valid link or not. - 0: The DWC_xcps is able to transmit GMII only when the device has determined the valid link. The DWC_xcps always returns this bit as 0.
6	0h	MF_PRE_SUP DWC_XPCS (MF_PRE_SUP):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	MF Preamble Suppression - 1: The DWC_xpcs accepts the MDIO frames with preamble suppressed. - 0: The DWC_xpcs does not accept the MDIO frames with preamble suppressed. This bit is always set to 0.
5	0h RO/V	AN_CMPL DWC_XPCS (AN_CMPL): Auto-negotiation Complete - 1: The AN process is complete - 0: The AN process is not complete When this bit is set to 1, the contents of the AN MMD Advertisement, AN MMD Link partner Ability, and AN MMD Expansion registers are valid. This bit returns 0 if AN_ENABLE is set to 0.
4	0h RO/V	RF DWC_XPCS (RF): Remote Fault (RO,LH Type) When set to 1, this bit indicates that the receive link of the link partner is down. This bit is set based on the auto-negotiated (1000BASE-X auto-negotiation) information from the link partner. - 1: The DWC_xpcs detected a remote fault. - 0: The DWC_xpcs did not detect a remote fault. This bit is not valid in SGMII/QSGMII/USXGMII Modes.
3	1h RO/V	AN_ABL DWC_XPCS (AN_ABL): Auto-negotiation Ability The DWC_xpcs always returns this bit as 1. - 1: The DWC_xpcs is able to perform auto-negotiation. - 0: The DWC_xpcs is not able to perform auto-negotiation.
2	0h RO/V	LINK_STS DWC_XPCS (LINK_STS): Link Status (RO,LL Type) When the DWC_xpcs sets this bit to 1, it indicates that the Rx link is up. If the link goes down, it is latched until the host performs the read operation to this register. - 1: Link Up - 0: Link Down
1	0h RO/V	Reserved
0	1h RO/V	EXT_REG_CAP DWC_XPCS (EXT_REG_CAP): Extended Register Capability - 1: Extended Register capability exists. This bit is always set to 1. - 0: Extended Register capability does not exist.

11.3.1.15 SR_MII_DEV_ID1 DWC_XCPS (SR_MII_DEV_ID1) - Offset 1F00000004h

SR MII MMD Device Identifier Register 1 This register returns the configurable Organizationally Unique Identifier (OUI) to the host.

Type	Size	Offset	Default
MMIO	16 bit	1F00000004h	7996h

Register Access Level:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	7996h RO/V	VS_MII_DEV_OUI_3_18 DWC_XPCS (VS_MII_DEV_OUI_3_18): Organizationally Unique Identifier[3:18] This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable Bits[24:1] for identifying the device manufacturer. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 1. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[15:0] of SR XS or PCS MMD Device Identifier Register 1 modifies the content of this register.

11.3.1.16 SR_MII_DEV_ID2 DWC_XPCS (SR_MII_DEV_ID2) - Offset 1F00000006h

SR MII MMD Device Identifier Register 2 This register returns the configurable Organizationally Unique Identifier (OUI), Model Number, and Revision Number of the device to the host.

Type	Size	Offset	Default
MMIO	16 bit	1F00000006h	CED0h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	33h RO/V	VS_MMD_DEV_OUI_19_24 DWC_XPCS (VS_MMD_DEV_OUI_19_24): Organizationally Unique Identifier [19:24] This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable Bits[24:1] for identifying the device manufacturer. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 2. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[15:10] of SR XS or PCS MMD Device Identifier Register 2 modifies the content of this register.
9:4	2Dh RO/V	VS_MMD_DEV_MMN_5_0 DWC_XPCS (VS_MMD_DEV_MMN_5_0): Model Number This field contains the 5-bit Model Number of the device. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 2. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[9:4] of SR XS or PCS MMD Device Identifier Register 2 modifies the content of this register.
3:0	0h RO/V	VS_MMD_DEV_RN_3_0 DWC_XPCS (VS_MMD_DEV_RN_3_0): Revision Number This field contains the 4-bit Revision Number of the device. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 2. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[3:0] of SR XS or PCS MMD Device Identifier Register 2 modifies the content of this register.

11.3.1.17 SR_MII_AN_ADV DWC_XPCS (SR_MII_AN_ADV) - Offset 1F00000008h

SR MII MMD AN Advertisement Register The host uses this register to advertise the abilities and status of the local device to its link partner through Clause 37 auto-negotiation protocol. Note: This register is present only for configurations with 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	1F00000008h	0020h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	NP DWC_XPCS (NP): Next Page The DWC_xpcs always returns this bit as 0 because it does not support the Next Page feature.
14	0h RO/V	Reserved
13:12	0h RW	RF DWC_XPCS (RF): Remote Fault This field indicates the fault signaling of the local device to be communicated to the link partner. - 00: No Error - 01: Offline - 10: Link Failure - 11: Auto-negotiation Error
11:9	0h RO	Reserved
8:7	0h RW	PAUSE DWC_XPCS (PAUSE): Pause Ability This field indicates the Pause ability of the device: - 00: No Pause - 01: Asymmetric Pause towards the link partner - 10: Symmetric Pause - 11: Symmetric Pause and Asymmetric Pause towards the local device. Software can program suitable values based on the capability of the MAC.
6	0h RW	HD DWC_XPCS (HD): Half Duplex When this bit is set, it indicates that the device can operate in the half-duplex mode.
5	1h RW	D DWC_XPCS (FD): Full Duplex When this bit is set, it indicates that the device can operate in the full-duplex mode.
4:0	0h RO	Reserved

11.3.1.18 SR_MII_LP_BABL DWC_XCPS (SR_MII_LP_BABL) - Offset 1F000000Ah

SR MII MMD AN Link Partner Base Ability Register The host uses this page to know the link partner's ability when the base page is received through Clause 37 auto-negotiation. The content of this register is valid only for 1000BASE-X auto-negotiation. It is not valid in SGMII/QSGMII/USXGMII auto-negotiation. Note: This register is present only for configurations with 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	1F000000Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	LP_NP DWC_XPCS (LP_NP):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Next Page This bit indicates that the link partner can handle Next Page. Note: To exchange information through Next Page, both devices (local and remote) should have the capability to handle Next Page. The DWC_xpcs does not support Next Page. Therefore, the Next Page exchange does not happen.
14	0h RO/V	LP_ACK DWC_XPCS (LP_ACK): ACK bit from the Link Partner This bit indicates that the link partner has successfully received the page sent by the local device.
13:12	0h RO/V	LP_RF DWC_XPCS (LP_RF): Remote Fault This field indicates the fault signaling of the link partner: - 00: No Error - 01: Offline - 10: Link Failure - 11: Auto-negotiation Error
11:9	0h RO	Reserved
8:7	0h RO/V	LP_PAUSE DWC_XPCS (LP_PAUSE): Pause Ability This field indicates the Pause ability of the link partner: - 00: No Pause - 01: Asymmetric Pause towards the link partner - 10: Symmetric Pause - 11: Both Symmetric Pause and Asymmetric Pause towards the local device
6	0h RO/V	LP_HD DWC_XPCS (LP_HD): Half Duplex When this bit is set, it indicates that the link partner is capable of operating in the half-duplex mode.
5	0h RO/V	LP_FD DWC_XPCS (LP_FD): Full Duplex When this bit is set, it indicates that the link partner is capable of operating in the full-duplex mode.
4:0	0h RO	Reserved

11.3.1.19 SR_MII_AN_EXPN DWC_XCPs (SR_MII_AN_EXPN) - Offset 1F0000000Ch

SR MII MMD AN Expansion Register

Type	Size	Offset	Default
MMIO	16 bit	1F0000000Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved
2	0h RO/V	LD_NP_ABL DWC_XPCS (LD_NP_ABL): Local Device NP Able - 1: The local device has the next page ability - 0: The local device does not have the next page ability The DWC_xpcs always returns this bit as 0 because it does not support Next Page.
1	0h RO/V	PG_RCVD DWC_XPCS (PG_RCVD):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Page Received (RO,LH Type) This bit indicates that the local device received a page from the link partner. - 1: The local device received a new page - 0: The local device did not receive a new page
0	0h RO	Reserved

11.3.1.20 SR_MII_MMD_EXT_STS DWC_XPCS (SR_MII_EXT_STS) - Offset 1F0000001Eh

SR MII MMD Extended Status Register This register is present only for configurations with 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	1F0000001Eh	C000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO/V	CAP_1G_X_FD DWC_XPCS (CAP_1G_X_FD): 1000BASE-X Full-Duplex Capable - 1: 1000BASE-X full-duplex capable - 0: Not 1000BASE-X full-duplex capable The DWC_xpcs always returns 1 because it supports this feature.
14	1h RO/V	CAP_1G_X_HD DWC_XPCS (CAP_1G_X_HD): 1000BASE-X Half-Duplex Capable - 1: 1000BASE-X half-duplex capable - 0: Not 1000BASE-X half-duplex capable The DWC_xpcs always returns 1 because it supports this feature.
13	0h RO/V	CAP_1G_T_FD DWC_XPCS (CAP_1G_T_FD): 1000BASE-T Full-Duplex Capable - 1: 1000BASE-T full-duplex capable - 0: Not 1000BASE-T full-duplex capable The DWC_xpcs always returns 0 because it does not support this feature.
12	0h RO/V	CAP_1G_T_HD DWC_XPCS (CAP_1G_T_HD): 1000BASE-T Half-Duplex Capable - 1: 1000BASE-T half-duplex capable - 0: Not 1000BASE-T half-duplex capable The DWC_xpcs always returns 0 because it does not support this feature.
11:0	0h RO	Reserved

11.3.1.21 SR_MII_TIME_SYNC_ABL DWC_XPCS (SR_MII_TIME_SYNC_ABL) - Offset 1F00000E10h

SR MII MMD Time Sync Capability Register. This register is present only in 1000BaseXOnly PCS configurations

Type	Size	Offset	Default
MMIO	16 bit	1F00000E10h	0003h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved
1	1h RO/V	MII_TX_DLY_ABL DWC_XPCS (MII_TX_DLY_ABL): DWC_xpcs Transmit Path Data Delay Information Available. If this bit is set, it indicates that the information regarding the maximum and minimum transmit data delay of DWC_xpcs is available in MII MMD Tx Time Delay Registers
0	1h RO/V	MII_RX_DLY_ABL DWC_XPCS (MII_RX_DLY_ABL): DWC_xpcs Receive Path Data Delay Information Available. If this bit is set, it indicates that the information regarding the maximum and minimum receive data delay of DWC_xpcs is available in MII MMD Rx Time Delay Registers

11.3.1.22 SR_MII_TIME_SYNC_TX_MAX_DLY_LWR DWC_XCPs (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR) - Offset 1F00000E12h

SR MII MMD Time Sync Tx Max Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E12h	0038h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0038h RO/V	MII_TX_MAX_DLY_LWR DWC_XPCS (MII_TX_MAX_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path (in nanoseconds) of DWC_xpcs.

11.3.1.23 SR_MII_TIME_SYNC_TX_MAX_DLY_UPR DWC_XCPs (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR) - Offset 1F00000E14h

SR MII MMD Time Sync Tx Max Delay Upper Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E14h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MII_TX_MAX_DLY_UPR DWC_XPCS (MII_TX_MAX_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path (in nanoseconds) of DWC_xpcs.

11.3.1.24 SR_MII_TIME_SYNC_TX_MIN_DLY_LWR DWC_XCPS (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR) - Offset 1F00000E16h

SR MII MMD Time Sync Tx Min Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E16h	0038h

Register Level Access

:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0038h RO/V	MII_TX_MIN_DLY_LWR DWC_XPCS (MII_TX_MIN_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path (in nanoseconds) of DWC_xpcs.

11.3.1.25 SR_MII_TIME_SYNC_TX_MIN_DLY_UPR DWC_XCPS (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR) - Offset 1F00000E18h

SR MII MMD Time Sync Tx Min Delay Upper Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E18h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MII_TX_MIN_DLY_UPR DWC_XPCS (MII_TX_MIN_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path (in nanoseconds) of DWC_xpcs.

11.3.1.26 SR_MII_TIME_SYNC_RX_MAX_DLY_LWR DWC_XCPs (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR) - Offset 1F00000E1Ah

SR MII MMD Time Sync Rx Max Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E1Ah	00B8h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	00B8h RO/V	MII_RX_MAX_DLY_LWR DWC_XPCS (MII_RX_MAX_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path (in nanoseconds) of DWC_xpcs.

11.3.1.27 SR_MII_TIME_SYNC_RX_MAX_DLY_UPR DWX_XCPs (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR) - Offset 1F00000E1Ch

SR MII MMD Time Sync Rx Max Delay Upper Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E1Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MII_RX_MAX_DLY_UPR DWC_XPCS (MII_RX_MAX_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path (in nanoseconds) of DWC_xpcs.

11.3.1.28 SR_MII_TIME_SYNC_RX_MIN_DLY_LWR DWC_XCPs (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR) - Offset 1F00000E1Eh

SR MII MMD Time Sync Rx Min Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E1Eh	0088h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0088h RO/V	MII_RX_MIN_DLY_LWR DWC_XPCS (MII_RX_MIN_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path (in nanoseconds) of PCS.

11.3.1.29 SR_MII_TIME_SYNC_RX_MIN_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR) - Offset 1F00000E20h

SR MII MMD Time Sync Rx Min Delay Upper Register This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00000E20h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MII_RX_MIN_DLY_UPR DWC_XPCS (MII_RX_MIN_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path (in nanoseconds) of PCS

11.3.1.30 VR_MII_DIG_CTRL1 DWC_XPCS (VR_MII_DIG_CTRL1) - Offset 1F00010000h

VR MII MMD Digital Control1 Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010000h	2400h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	VR_RST DWC_XPCS (VR_RST): Vendor-Specific Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the vendor-specific software reset process in which all internal blocks, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is self cleared under the following conditions: For Synopsys

continued...

Bit Range	Default & Access	Field Name (ID): Description
		PHY: This bit is self cleared when Bits[4:2] in VR_XS_PCS_DIG_STS Register are equal to 3'b100, that is, Tx/Rx clocks are stable and in Power_Good state. For NonSynopsys PHY: This bit is self cleared after the following: - 32 clk_csr_i clocks for the MCI interface - 1 MDC clock period for the MDIO interface Note: For information about the read or write access for any register during the reset process, see "Special Case Register Access" section.
14	0h RW	R2TLBE DWC_XPCS (R2TLBE): Rx to Tx Loopback Enable This bit controls the loopback path from the GMII Rx to the GMII Tx at the GMII interface. * 0: Loopback path is disabled * 1: Loopback path is enabled In configurations with CL37_AN=Enabled and MAIN_MODE!=1000BaseXOnly PCS, thought this bit is read-only,it reflects the value programmed to R2TLBE bit of VR_XS_PCS_DIG_CTRL1 Register
13	1h RW	EN_VSMMD1 DWC_XPCS (EN_VSMMD1): Enable Vendor-Specific MMD1 When this bit is set to 1, the vendor-specific MMD1 (VSMMD1) is enabled. When this bit is set to zero, VSMMD1 is disabled.
12	0h RO/V	CL37_BP DWC_XPCS (CL37_BP): Enable Clause 37 AN in Backplane Configuration This bit is present when MAIN_MODE = Backplane Ethernet PCS and CL37_AN = Enabled. This is a read-only bit and it reflects the value programmed to CL37_BP bit of VR PCS MMD Digital Control 1 Register.
11	0h RW	PWRSV DWC_XPCS (PWRSV): Power Save This bit is present only when the DWC_xpcs is configured for Synopsys PHY. - 0: Normal operation. - 1: DWC_xpcs and the PHY enter the power-save mode. When this bit is set, the DWC_xpcs triggers the power-down mode by turning off the PHY Receiver and Transmitter, and without turning off PLL. For Synopsys Multiprotocol 12G/16G PHY, DWC_xpcs asserts xpcs_tx_lpd_o{lane} and xpcs_rx_lpd_o{lane} when this bit is set. When the host clears this bit, DWC_xpcs resumes normal operation. After clearing this bit, the host must wait until Bits[4:2] of the VR_XS_PCS_DIG_STS Register indicate that the DWC_xpcs is in a normal state. Note: For a description of read or write access for any register while this bit is set, see "Special Case Register Access" section of Databook.
10	1h RW	CS_EN DWC_XPCS (CS_EN): Clock Stop Enable - 1: The PHY may stop the clock during LPI mode - 0: The clock cannot be stopped during LPI mode You should program this bit based on the capability of the MAC during Rx LPI mode. Access Type: - For configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled, this bit is RW. - For all other configurations, this bit is reserved and RO.
9	0h RW	MAC_AUTO_SW DWC_XPCS (MAC_AUTO_SW): Automatic Speed Mode Change after CL37 AN When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII_EN=Enabled: If this field is set to 1, DWC_xpcs automatically switches to the negotiated SGMII/USXGMII/QSGMII(port0) speed, after the completion of Clause 37 auto-negotiation. This mode is valid only when DWC_xpcs is configured as MAC-side SGMII/USXGMII/QSGMII and should be set only when Auto-negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, DWC_xpcs will operate at the speed/duplex mode as per the values programmed to SR_MII_CTRL Register. In that case, after the completion of CL37 AN, application has to read the negotiated Speed/Duplex Mode from VR_MII_AN_INTR_STS Register and then program SR_MII_CTRL Register appropriately. If this bit is set to 1 in SGMII mode, xpcs_sgmii_link_sts_o, xpcs_link_speed_o and xpcs_sgmii_full_duplex_o outputs will reflect the auto-negotiated values i.e., values from CL37_ANSGM_STS field of VR_MII_AN_INTR_STS Register. For USXGMII mode, if clk_xgmii_tx_i and clk_xgmii_rx_i do not stabilize at the new operating frequency (based on the selected speed) immediately after the completion of auto-negotiation, then software might need to program 'USR_A_RST' bit prior to starting packet transfer in the new speed mode. Note: This bit should be set only when DWC_xpcs is configured as SGMII/USXGMII/QSGMII MAC i.e., TX_CONFIG=0 Note: When this bit is set, the values programmed to SS5,SS6 and SS13 bits are ignored. Moreover, the values of these bits do not change based on auto-negotiation outcome. For other configurations: This is a read-only reserved field and returns 0.
8	0h RW	INIT DWC_XPCS (INIT):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Datapath Initialization Control This bit can be set to flush/initialize the various FIFOs implemented inside DWC_xpcs. This is Self-Clear bit. After writing 1 to this bit, software should poll this bit continuously. Software should proceed to any other operation, only after reading this bit as 0. When this bit is programmed to 1, RXFIFO_OVF/RXFIFO_UNF bits of VR_MII_DIG_STS Register might get set incorrectly. Hence, read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIFO_UNF and RXFIFO_UNF bits would be reliable
7	0h RO/V	MSK_RD_ERR DWC_XPCS (MSK_RD_ERR): Mask Running Disparity Error. In QSGMII mode of operation, an error in data received from a particular port of a far-end device can result in unprecedent running disparity errors for other ports (even if data is received correctly). In order to resolve this issue, DWC_xpcs provides an option to mask the running disparity errors. If this register bit is set, then running disparity errors are ignored by DWC_xpcs receiver in evaluating the validity of received code-groups.
6	0h RW	PRE_EMP DWC_XPCS (PRE_EMP): Pre-emption Packet Enable. This bit should be set to 1 to allow the DWC_xpcs to properly receive/transmit pre-emption packets in SGMII 10M/100M Modes.
5	0h RO/V	EN_100M DWC_XPCS (EN_100M): Enable 100Mbps PCS Mode. This bit should be set to 1 to enable 100Mbps PCS Mode of operation. This bit drives the output port 'xpcs_100m_o'.
4	0h RW	DTXLANED_0 DWC_XPCS (DTXLANED_0): Tx Lane 0 Disable When this bit is set, the DWC_xpcs disables the Tx Lane 0 of the PHY. When reset, the DWC_xpcs enables the Tx Lane 0 of the PHY. This bit is ReadWrite only when MAIN_MODE= 1000BASEX-Only PCS. Notes: This bit is shared with the following bits: - Bit 4 of VR_XS_PCS_DIG_CTRL1 Register and VR_MIID_DIG_CTRL1 Register - Bit 1 of SR_PMA_TX_DIS Register - Bit 0 of SR_PMA_KX_CTRL Register
3	0h RW	CL37_TMR_OVR_RIDE DWC_XPCS (CL37_TMR_OVR_RIDE): Over-Ride Control for CL37 Link Timer. This bit can be set to override the default value of Clause 37 link_timer used by DWC_xpcs for auto-negotiation. If this bit is set, the value programmed to VR_MII_LINK_TIMER_CTRL Register is used to compute the duration of Link Timer. This bit should be set, only after programming the appropriate value to VR_MII_LINK_TIMER_CTRL Register
2	0h RW	EN_2_5G_MODE DWC_XPCS (EN_2_5G_MODE): Enable 2.5G GMII Mode. This bit should be set to 1 to enable 2.5G GMII Mode of operation. This bit drives the output port 'xpcs_2pt5g_mode_o'. This bit is shared with bit[2] of VR_XS_PCS_DIG_CTR1 Register.
1	0h RW	BYP_PWRUP DWC_XPCS (BYP_PWRUP): Bypass Power-Up Sequence When this bit is set to 1, the DWC_xpcs bypasses the normal flow of the power-up sequence and reaches the Power_Good state to enable transmission or reception. When this bit is set, the DWC_xpcs does not wait for the PLL and Transmit or Receive PLL status from the Synopsys PHY. You can use this feature in the following scenarios: - When the DWC_xpcs is configured to interface with a specific Synopsys PHY. - When the data path needs to be interfaced to some other PHY. When this bit is set to 0, the DWC_xpcs waits for the PLL, Tx, or Rx PLL status from the Synopsys PHY before resuming the normal transmission and reception. Note: This bit is shared with Bit 1 of following registers: - VR_XS_PCS_DIG_CTRL1 Register - VR_AN_DIG_CTRL1 Register - VR_PMA_DIG_CTRL1 Register Access Type: If SNPS_XAUI_PHY= Enabled, this bit is RW. Otherwise, this bit is RO.
0	0h RW	PHY_MODE_CTRL DWC_XPCS (PHY_MODE_CTRL): When SGMII_PHY_AN_AUTO_RESTART=Enabled or QSGMII_PHY_AN_AUTO_RESTART=Enabled or USXG_PHY_AN_AUTO_RESTART=Enabled: PHY mode control This bit controls the Clause 37 auto-negotiation when operating in SGMII/QSGMII/USXGMII (Port 0) PHY mode. SGMII/QSGMII: When this bit is set to 1, DWC_xpcs advertises the values of input ports xpcs_sgmii_link_sts_i, xpcs_sgmii_link_speed_i and xpcs_sgmii_full_duplex_i during SGMII/(Port0)QSGMII auto-negotiation. When this bit is set to 0, SGMII/QSGMII(Port0) auto-negotiation advertises the values programmed to: - bit 4 (SGMII_LINK_STS) of VR_MII_AN_CTRL Register - bit 13 (ss13) and 6 (ss6) of SR_MII_CTRL Register and - bit 5 (FD) of SR_MII_AN_ADV Register USXGMII: When this bit is set to 1, DWC_xpcs advertises the values of input ports xpcs_usxg_link_sts_i,

Bit Range	Default & Access	Field Name (ID): Description
		xpcs_usxg_link_speed_i,xpcs_usxg_full_duplex_i,xpcs_usxg_eee_abl_i and xpcs_usxg_ck_stp_abl_i during USXGMII (port 0) auto-negotiation. When this bit is set to 0, USXGMI (Port0) auto-negotiation advertises the following: - bit 4 (SGMII_LINK_STS) of VR_MII_AN_CTRL Register - bit 13 (ss13) and 6 (ss6) and 5 (ss5) of SR_MII_CTRL Register and - Value of 1 for Duplex-Mode - Value of 1 for EEEcapability, if EEE=Enabled; Value of 0 if EEE_EN=Disabled - Value of 1 for EEE clockstop capability,if EEE=Enabled; Value of 0 if EEE_EN=Disabled Note: This bit should be set only when DWC_xpcs is configured as SGMII/QSGMII/USXGMII PHY, that is, TX_CONFIG=1 In other configurations, this field is reserved and read-only.

11.3.1.31 VR_MII_AN_CTRL DWC_XPCS (VR_MII_AN_CTRL) - Offset 1F00010002h

VR MII MMD AN Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010002h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved
9	0h RW	IND_TX_EN DWC_XPCS (IND_TX_EN): Independent Transmit Enable in 1000BASE-X/KX mode. If this bit is set to 1, DWC_xpcs will be able to transmit the GMII Tx data, irrespective of its receive link status (provided auto-negotiation is not enabled). If this bit is set to 0, DWC_xpcs will send IDLE till its receiver has attained synchronization.
8	0h RW	MII_CTRL DWC_XPCS (MII_CTRL): MII Control When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII_EN=Enabled: This bit controls the width of the MAC interface when operating at SGMII/QSGMII/USXGMII speed modes of 10 Mbps or 100 Mbps - 0: 4-bit MII - 1: 8-bit MII This bit also controls the xpcs_mii_ctrl_o signal which is used for external clock multiplexing of the clk_mii_tx_i and clk_mii_rx_i signals. For other configurations: This is a read-only reserved field and returns 0.
7:5	0h RO	Reserved
4	0h RW	SGMII_LINK_STS DWC_XPCS (SGMII_LINK_STS): When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII Link Status: SGMII Link Status/ USXGMII Link Status /QSGMII Port0 Link Status This bit is used in Bit 15 of the Config_Reg during Clause 37 auto-negotiation when the TX_CONFIG bit of this register is set to 1 in the SGMII/QSGMII/USXGMII mode and when PHY_MODE_CTRL bit of VR_MII_DIG_CTRL1 Register is 0. - 0: Link Down - 1: Link Up >For other configurations: This is a read-only reserved field and returns 0.
3	0h RW	TX_CONFIG DWC_XPCS (TX_CONFIG):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII_EN=Enabled: Transmit Configuration This bit controls the Config_Reg value to be used during the Clause 37 auto-negotiation in the SGMII/QSGMII/USXGMII mode. - 1: Configures the DWC_xpcs as the PHY side SGMII/QSGMII/USXGMII. - 0: Configures the DWC_xpcs as the MAC side SGMII/QSGMII/USXGMII. For other configurations: This is a readonly reserved field and returns 0.
2:1	0h RW	PCS_MODE DWC_XPCS (PCS_MODE): When SGMII_EN=Enabled or QSGMII_EN=Enabled: PCS Mode This field controls the auto-negotiation (and operating) mode. - 00: 1000BASE-X mode (clause 37 autonegotiation is as per 1000BaseX). - 10: SGMII mode (clause 37 auto-negotiation is as per SGMII). - 11: QSGMII mode (clause 37 auto-negotiation conforms to QSGMII) If this field is set as 2'b11, then DWC_xpcs asserts the 'gxss_qsgmii_mode_o' port. For other configurations: This is a read-only reserved field and returns 0.
0	0h RW	MII_AN_INTR_EN DWC_XPCS (MII_AN_INTR_EN): Clause 37 AN Complete Interrupt Enable When set to 1, this bit enables the generation of Clause 37 auto-negotiation complete interrupt output. When set to 0, it disables the generation of Clause 37 auto-negotiation complete interrupt.

11.3.1.32 VR_MII_AN_INTR_STS DWC_XCPs (VR_MII_AN_INTR_STS) - Offset 1F00010004h

VR MII MMD AN Interrupt and Status Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010004h	000Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	Reserved
6	0h RO/V	LP_CK_STP DWC_XPCS (LP_CK_STP): Link Partner EEE Clock Stop Capability This field indicates the EEE clock stop capability (or clock-stop enable - in case far-end is acting as QSGMII MAC) advertised by the far-end device. This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 0. Note: This field is present only in configurations with QSGMII_EN=Enabled
5	0h RO/V	LP_EEE_CAP DWC_XPCS (LP_EEE_CAP): Link Partner EEE Capability This field indicates the EEE capability advertised by the far-end device (Port 0 QSGMII PHY). This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 0. Note: This field is present only in configurations with QSGMII_EN=Enabled
4:1	5h RO/V	CL37_ANSGM_STS DWC_XPCS (CL37_ANSGM_STS): When SGMII_EN=Enabled or QSGMII_EN=Enabled: Clause 37 AN SGMII Status/QSGMII Port 0 Status This field is valid only when the PCS_MODE[1:0] is set to the SGMII/QSGMII mode and the auto-negotiation is complete. It indicates the status received from remote link after the SGMII/QSGMII (Port 0) autonegotiation is complete. CL37_ANSGM_STS[0] -

continued...

Bit Range	Default & Access	Field Name (ID): Description
		0: Half Duplex - 1: Full Duplex CL37_ANSGM_STS[2:1] - 00: 10 Mbps speed link - 01: 100 Mbps speed link - 10: 1000 Mbps speed link CL37_ANSGM_STS[3] - 0: Link is Down - 1: Link is Up For other configurations: This is a read-only reserved field and returns 0.
0	0h RW	CL37_ANCMLT_INTR DWC_XPCS (CL37_ANCMLT_INTR) Clause 37 AN Complete Interrupt (SS,WC Type) The DWC_xpcs sets this bit when Clause 37 auto-negotiation is complete. The host must clear this bit by writing 0 to it.

11.3.1.33 VR_MII_TC DWC_XCPs (VR_MII_TC) - Offset 1F00010006h

VR MII MMD Test Control Register. Note: This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00010006h	0000h

Register Level Access

:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved
2	0h RW	TPE DWC_XPCS (TPE): Test Pattern Enable Lanes This bit indicates that a test pattern can be enabled in the Tx path after the current normal frame transmission is complete. - 0: Test pattern disabled - 1: Test pattern enabled Dependencies: The specific test pattern that is generated is based on Bits[1:0] of this register.
1:0	0h RW	TP DWC_XPCS (TP): Test Pattern Select This field indicates the pattern type that is enabled with Bit 2 of this register. The following are the supported test patterns: - 2'b00: High Frequency Test Pattern - 2'b01: Low Frequency Test Pattern - 2'b10: Mixed Frequency Test Pattern - 2'b11: Reserved The definition of these test patterns is specified in IEEE Std 802.3ae, Annex 48A.

11.3.1.34 VR_MII_DBG_CTRL DWC_XCPs (VR_MII_DBG_CTRL) - Offset 1F0001000Ah

VR MII MMD Debug Control Register Note: This register is present only in 1000BaseXOnly PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F0001000Ah	0000h

Register Access Level:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved
8	0h RW	TX_PMBL_CTL DWC_XPCS (TX_PMBL_CTL): TX_PMBL_CTL DWC_XPCS (TX_PMBL_CTL): Transmit Preamble Control This bit can be set to 1 to prevent possible preamble truncation in the DWC_xpcs transmitter when operating in 1000BASE-X (or 2.5G Mode over GMII) Mode. As per IEEE spec, it is permissible for a compliant 1000BASEX PCS transmit process to truncate the first byte of preamble in order to align the start of the packet on the EVEN boundary. If this bit is set to 1, DWC_xpcs does not delete any preamble bytes (received from GMII Tx interface) and passes on the same number of preamble bytes to its output. DWC_xpcs carries out this operation by adjusting the IPG. This mode is a deviation from Clause 36 of IEEE802.3 specification. But it can prove useful when operating at 2.5G Mode (over clocked 1000BASE-X Mode) and the far-end device is compliant to IEEE802.3bz/cb specification.
7	0h RW	RX_SYNC_CTL DWC_XPCS (RX_SYNC_CTL): RX_SYNC_CTL DWC_XPCS (RX_SYNC_CTL): Receive Synchronization Control DWC_xpcs, by default, does not monitor the 'xgxs_rx_valid_i' input signal to determine Receive Synchronization Status. Receive Synchronization (sync_status) is attained by merely monitoring and detecting COMMA pattern in the input data, irrespective of the value of 'xgxs_rx_valid_i' signal. If this bit is set to 1, DWC_xpcs starts looking for COMMA in the input data stream only after PHY has asserted 'xgxs_rx_valid_i'.
6	0h RW	RX_DT_EN_CTL DWC_XPCS (RX_DT_EN_CTL): RX_DT_EN_CTL DWC_XPCS (RX_DT_EN_CTL): Rx Data Enable Control. This bit controls the behavior of xpcs_rx_data_en_o[0] output from DWC_xpcs. During normal operation DWC_xpcs de-asserts xpcs_rx_data_en_o[0] on detecting of Loss-of-Signal. However, if this bit is set, DWC_xpcs does not de-assert xpcs_rx_data_en_o[0] on detection of Loss of Signal. Instead, the value of RX_DT_EN_0 bit from VR_MII_MP_12G_16G_25G_RX_GENCTRL0 Register is driven on xpcs_rx_data_en_o[0] output port.
5	0h RW	SUPPRESS_EEE_LOS_DET DWC_XPCS (SUPPRESS_EEE_LOS_DET): SUPPRESS_EEE_LOS_DET DWC_XPCS (SUPPRESS_EEE_LOS_DET): Suppress EEE Loss of Signal Detection. When this field is set to 1, Loss of Signal indicated by the PHY (based on input port xpcs_los_i) is ignored by DWC_xpcs while evaluating the Receive link when operating in EEE mode. Receive link is evaluated based the on data received by DWC_xpcs from PHY. When this field is set to 0, Loss of signal indicated by the PHY is considered by the DWC_xpcs while evaluating the Receive link status in EEE mode.
4	0h RW	SUPPRESS_LOS_DET DWC_XPCS (SUPPRESS_LOS_DET): SUPPRESS_LOS_DET DWC_XPCS (SUPPRESS_LOS_DET): Suppress Loss of Signal Detection When this field is set to 1, Loss of Signal indicated by the PHY (based on input port xpcs_los_i) is ignored by DWC_xpcs while evaluating the Receive link. Receive link is evaluated based the Rx data received on the 'xgxs_rx_data_{lane}_i' port of DWC_xpcs. When this field is set to 0, Loss of signal indicated by the PHY is considered by the DWC_xpcs while evaluating the Receive link status. Note: This register bit has an impact on the EEE Rx behaviour of DWC_xpcs when operating in QSGMII Mode for Multi-protocol 12G/16G/25G PHY configurations. If this register bit is set to 1, then entry to RX QUIET state is based on 'code_sync_status' (generated by PCS Synchronization State Diagram) instead of 'signal_detect'.
3:1	0h RO	Reserved
0	0h RW	RESTART_SYNC_0 DWC_XPCS (RESTART_SYNC_0): RESTART_SYNC_0 DWC_XPCS (RESTART_SYNC_0): Restart Synchronization When set to 1, this bit restarts the Rx Synchronization State machine on Lane 0. The host must clear this bit to 0 before setting it to 1 next time.

11.3.1.35 VR_MII_EEE_MCTRL0 DWC_XCPs (VR_MII_EEE_MCTRL0) - Offset 1F0001000Ch

VR MII MMD EEE Mode Control Register This register enables or disables the Energy Efficient Ethernet (EEE) support. This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	1F0001000Ch	899Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	8h RW	CLKSTOP DWC_XPCS (CLKSTOP): Clock Stop This field holds the count value after which the Rx clock to the MAC can be stopped. The default value is 8. The host should program this value depending on the capability of the MAC. This field is used to control the assertion of the xpcs_lrx_clk_gat_o signal (to gate the Rx clock of the MAC) By default, the xpcs_lrx_clk_gat_o signal is asserted after the PCS Rx module detects the LPI pattern followed by the following: Number of clk_xgxs_rx0_i or clk_rpcs_rx_i clocks (specified in this field) + clk_eee_i synchronization delay + FIFO initialization delay
11:8	9h RW	MULT_FACT_100NS DWC_XPCS (MULT_FACT_100NS): 100 ns Clock Tic Multiplying Factor This bit is the multiplying factor to the clk_eee_i clock time period to make it closer to 100 ns. For example, if the clk_eee_i clock time period (clk_eee_i_time_period) is 10 ns, the value of this field is 9, that is, 1 less than 10. This value should be programmed such that the clk_eee_i_time_period * (MULT_FACT_100NS + 1) should be within 80 ns to 120 ns. The default value of this register is 9, assuming that the default clk_eee_i time period to be 10 ns.
7	1h RW	RX_EN_CTRL DWC_XPCS (RX_EN_CTRL): Rx Control Enable This bit controls the generation of the xpcs_rx_en_o{lane} signal. When this bit is set to 1, the xpcs_rx_en_o{lane} signal is de-asserted when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_rx_en_o{lane} signal is not de-asserted when the EEE transmit controller reaches the Quiet state.
6	0h RW	SIGN_BIT DWC_XPCS (SIGN_BIT): Effective 100 ns Tic Value The host should use this bit to fine tune the EEE timing requirement. The host should set this bit to 0 when the clk_eee_i_time_period * (MULT_FACT_100NS + 1) value is more than 100 ns. The host should set this bit to 1 when the clk_eee_i clock period * (MULT_FACT_100NS + 1) value is less than or equal to 100 ns.
5	0h RO	Reserved
4	1h RW	TX_EN_CTRL DWC_XPCS (TX_EN_CTRL): Tx Control Enable This bit controls the generation of the following signals: - xgxs_tx{lane}_en_o (for Synopsys PHY) - xpcs_tx_en_o{lane} (for non-Synopsys PHY) When this bit is set to 1, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is de-asserted when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is not deasserted when the EEE transmit controller reaches the Quiet state.
3	1h RW	RX QUIET EN DWC_XPCS (RX QUIET_EN): Rx Quiet Enable This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
2	1h RW	TX QUIET EN DWC_XPCS (TX QUIET_EN): Tx Quiet Enable This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
1	0h RW	LRX_EN DWC_XPCS (LRX_EN):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		LPI Rx Enable When set to 1, this bit enables the Energy Efficient Ethernet support in the DWC_xpcs receive path. When set to 0, it disables the support for Energy Efficient Ethernet in the DWC_xpcs receive path.
0	0h RW	LTX_EN DWC_XPCS (LTX_EN): LPI Tx Enable When set to 1, this bit enables the Energy Efficient Ethernet support in the DWC_xpcs Transmit path. When set to 0, it disables the support for Energy Efficient Ethernet in the DWC_xpcs Transmit path.

11.3.1.36 VR_MII_EEE_TXTIMER DWC_XCPS (VR_MII_EEE_TXTIMER) - Offset 1F00010010h

VR MII MMD EEE Tx Timer Register This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	1F00010010h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved
5:0	0h RW	TSL_RES DWC_XPCS (TSL_RES): TSL Resolution This field stores the resolution value for the TSL timer. When the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TSL timer. The DWC_xpcs maintains the default value of the TSL timer as 199, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns to produce 19900 ns (19.9 us) as per the TSL requirement in the IEEE standard. If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 90, the default TSL timer produces 17910 ns (17.91 us) which is lesser than the standard 19.9 us. To make it 19.9 us, you should program this register such that (199 +/- TSL_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) is greater than 19.9 us and less than 20.1 us (max limit), that is, (199 + TSL_RES)*90 = 19.9 us. TWL_RES = 23 meets the requirement which produces 19.98 us. The SIGN_BIT should be programmed as 1.

11.3.1.37 VR_MII_EEE_RXTIMER DWC_XCPS (VR_MII_EEE_RXTIMER) - Offset 1F00010012h

VR MII MMD EEE Rx Timer Register This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	1F00010012h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved
13:8	00h RW	<p>TWR_RES DWC_XPCS (TWR_RES): TWR Resolution This field stores the resolution value for the TWR timer. When the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TWR timer. The default value is 11 us for 1000BASEX-Only PCS mode. This value is as per the requirements specified in the standard assuming that $\text{clk_eee_i_time_period} * (\text{MULT_FACT_100NS} + 1)$ produces 100 ns tick. Example: For KX mode, the time requirement is 11 us. The DWC_xpcs maintains the default value of the TWR timer as 110, assuming $\text{clk_eee_i_time_period} * (\text{MULT_FACT_100NS} + 1)$ is equal to 100 ns to produce 11000 ns (11 us). If $\text{clk_eee_i_time_period} * (\text{MULT_FACT_100NS} + 1)$ is 110, the default TWR timer produces 12100 ns (12.1 us) which is more than 11 us. To make it 11 us, you must program this register such that $(110 \pm \text{TWR_RES}) * (\text{MULT_FACT_100NS} + 1) * \text{clk_eee_i_time_period} = 11$ us. Therefore, use the following equation: $(110 - \text{TWR_RES}) * 110 = 11000$ ns $\text{TWL_RES} = 10$ meets the requirement which produces 11 us. The SIGN_BIT should be programmed as 0.</p>
7:0	00h RW	<p>RES_100U DWC_XPCS (RES_100U): 100 us Resolution This field stores the resolution value for the 100 us timer. If the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the 100 us timer. This field is used to control the generation of 100 us time tick using the clk_eee_i clock and MULT_FACT_100NS field. By default, the 100 us timer is generated assuming $\text{clk_eee_i_time_period} * (\text{MULT_FACT_100NS} + 1)$ is equal to 100 ns. Therefore, the DWC_xpcs maintains the default value of the 100 us timer as 1000 to achieve 100000 ns (100 us). You should use this field if $\text{clk_eee_i_time_period} * (\text{MULT_FACT_100NS} + 1)$ is not equal to 100 ns. To program this field, use the following equation: $(1000 \pm \text{RES_100US}) * (\text{MULT_FACT_100NS} + 1) * \text{clk_eee_i_time_period} = 100$ us The SIGN_BIT should be programmed as 1 for (+) and 0 for (-).</p>

11.3.1.38 VR_MII_LINK_TIMER_CTRL DWC_XCPs (VR_MII_LINK_TIMER_CTRL) - Offset 1F00010014h

VR MII MMD Link Timer Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010014h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	<p>CL37_LINK_TIME DWC_XPCS (CL37_LINK_TIME): Programmable Link Timer Value for Clause 37 auto-negotiation. This field can be programmed to any desired value if application wishes to override the standard specified values for Link Timer used during Clause 37 Auto negotiation. Link timer is implemented in DWC_xpcs using a 24-bit timer. When operating in USXGMII mode, link timer runs at 156.25 MHz. When operating in 1000BaseX/SGMII mode, this timer operates at 125 MHz. For</p>

Bit Range	Default & Access	Field Name (ID): Description
		USXGMII configurations: This field forms the upper 16-bit of the 24-bit value that gets loaded to the link timer. The lower 8-bits are hard-coded as zero. For example, if CL37_LINK_TIME = 1, the value that is loaded to the timer is 24'h100, which corresponds to a duration of 1638 ns (256*6.4ns) in USXGMII mode or 2048 ns (256*8ns) in 1000BaseX/SGMII mode. For configurations without USXGMII: This field forms the upper 16-bit of the 24-bit value that gets loaded to the link timer. The lower 8-bits are hardcoded as 8'h7D. For example, if CL37_LINK_TIME = 1, the value that is loaded to the timer is 24'h17D, which corresponds to a duration of 3048 ns (381*8ns). After programming this register, application should perform either of the following steps, so that the new values takes effect: - Set CL37_TMR_OVR_RIDE bit (bit[3]) of VR_MII_DIG_CTRL1 Register to 1 - FAST_SIM bit of SR Control MMD Control Register should be cleared (if already set) and then set back to 1.

11.3.1.39 VR_MII_EEE_MCTRL1 DWC_XCPS (VR_MII_EEE_MCTRL1) - Offset 1F00010016h

VR MII MMD EEE Mode Control 1 Register This register also controls the Energy Efficient

Ethernet (EEE) related settings of DWC_xpcs. This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	1F00010016h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	Reserved
0	0h RW	TRN_LPI DWC_XPCS (TRN_LPI): Transparent Tx LPI Mode Enable. When set to 1 (along with LTX_EN=1), transparent LPI mode gets activated in the DWC_xpcs Transmit path. In this mode, the transmit LPI state-machine does not move to TX QUIET state. On detecting Lower-Power Idle on GMII Tx interface, DWC_xpcs goes to the TX_SLEEP state and remains in this state till MAC stops sending LPI. In this mode, DWC_xpcs merely sends the encoded LPI pattern to the serdes. This mode does not involve gating-off of any clocks to DWC_xpcs. In addition, the serdes transmitter is not disabled (xpcs_tx_data_en_o signal remains high). MAC should ensure that it does not gate-off XGMII/GMII Tx clock to DWC_xpcs during this mode of operation.

11.3.1.40 VR_MII_DIG_STS DWC_XCPS (VR_MII_DIG_STS) - Offset 1F00010020h

VR MII MMD Digital Status Register.

NOTE

This register is present only in 1000BaseXOnly PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	1F00010020h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	LTX_STATE DWC_XPCS (LTX_STATE): LPI Transmit State. This field indicates the current state of the LPI Transmit state Machine. This is a 2-bit field if the selected configuration does not have RPCS. Otherwise, it is a 3-bit field. - 000: LTX_ACTIVE - 001: LTX_SLEEP - 010: LTX QUIET - 011: LTX_REF_WAKE - 100: LTX_ALERT (valid only if RPCS is present) - 101: LTX_SCR_BYP (valid only if RPCS is present)
12:10	0h RO/V	LRX_STATE DWC_XPCS (LRX_STATE): LPI Receive State This field indicates the current state of the LPI Receive State Machine: - 000: LRX_ACTIVE - 001: LRX_SLEEP - 010: LRX QUIET - 011: LRX_WAKE - 100: LRX_WTF - 101: LRX_LINK_FAIL - 110: LRX_LPI_K
9:7	0h RO	Reserved
6	0h RO/V	RXFIFO_OVF DWC_XPCS (RXFIFO_OVF): Rx FIFO Overflow (RO,LH Type) This bit indicates the clock rate compensation FIFO overflow. - 0: Normal operation - 1: FIFO overflow
5	0h RO/V	RXFIFO_UNDF DWC_XPCS (RXFIFO_UNDF): Rx FIFO Underflow (RO,LH Type) This bit indicates the clock rate compensation FIFO underflow. - 0: Normal operation - 1: FIFO underflow
4:2	4h RO/V	PSEQ_STATE DWC_XPCS (PSEQ_STATE): Power Up Sequence State This field indicates the state variable value of the power-up sequence module. For Synopsys Multi-protocol PHY: * 3'b000: Wait for MPLL ON * 3'b001: Wait for TX up * 3'b010: Wait for RX up * 3'b011/3'b100: Tx/Rx Stable (Power_Good state) * 3'b101: Wait for Rx down (MPLL still ON) * 3'b110: MPLL OFF For Synopsys Multi-protocol 12G/16G PHY * 3'b000: Wait for ACK High 0 * 3'b001: Wait for ACK Low 0 * 3'b010: Wait for ACK High 1 * 3'b011: Wait for ACK Low 1 * 3'b100: Tx/Rx stable (Power_Good state) * 3'b101: Power Save state * 3'b110: Power Down state
1:0	0h RO	Reserved

11.3.1.41 VR_MII_ICG_ERRCNT1 DWC_XCPS (VR_MII_ICG_ERRCNT1) - Offset 1F00010022h

VR MII MMD Invalid Code Group Error Count1 Register.

NOTE

This register is present only for 1000BaseX-Only PCS configurations

Type	Size	Offset	Default
MMIO	16 bit	1F00010022h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved
7:0	00h RO/V	EC0 DWC_XPCS (EC0): Invalid Code Group Count Lane 0 (RO,LH Type) This field gives the invalid code group count in Lane 0 when Bit 4 of VR_MII_DIG_ERRCNT_SEL Register is set to 1.

11.3.1.42 VR_MII_MISC_STS DWC_XCPS (VR_MII_MISC_STS) - Offset 1F00010030h

VR MII MMD Miscellaneous Status Register. This register is present only when the DWC_xpcs is configured in 1000BASEX-Only PCS mode.

Type	Size	Offset	Default
MMIO	16 bit	1F00010030h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	Reserved
3:0	00h RO/V	BIT_SFT DWC_XPCS (BIT_SFT): Bit Shift This field indicates the number of bit-shifts carried-out by comma-detect logic so as to align the incoming 10-bit XGXS Rx data Default Value: The default value of this field can be any value, depending on the status of comma-detect logic.

11.3.1.43 VR_MII_RX_LSTS DWC_XCPS (VR_MII_RX_LSTS) - Offset 1F00010040h

VR MII PHY Rx Lane Status Register In KX_Only, KR_Only, KR_KX, 10GBASE-R PCS, and 1000BASEX-Only PCS configurations, only Lane 0 control and status information is present. In configurations with both 1G (KX) and 10G (XGXS PCS, 10GBASE-X PCS, or KX4) modes, only Lane 0 control and status information is used when the DWC_xpcs is operating in the 1G mode.

Type	Size	Offset	Default
MMIO	16 bit	1F00010040h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	RX_VALID_3_1 DWC_XPCS (RX_VALID_3_1): DPLL Lock Status for Lanes[3:1] This field indicates that the DPLL in the PHY is locked on the serial data in the corresponding lane. - 3'b**1: Lane 1 DPLL bit locked - 3'b*1*: Lane 2 DPLL bit locked - 3'b1**: Lane 3 DPLL bit locked Dependency: This field is present only the following configurations: - Synopsys PHY configurations - Backplane Ethernet PCS configurations with non-Synopsys PHY
12	0h RO/V	RX_VALID_0 DWC_XPCS (RX_VALID_0): DPLL Lock Status for Lane 0 This field indicates that the DPLL in the PHY is locked on the serial data in Lane 0. The value 1'b1 indicates that Lane 0 DPLL bit is locked. Dependency: This field is present only the following configurations: - Synopsys PHY configurations - Backplane Ethernet PCS configurations with non-Synopsys PHY
11:9	0h RO	Reserved
8	0h RO/V	RX_PLL_STATE_0 DWC_XPCS (RX_PLL_STATE_0): Rx DPLL State for Lane 0 This field indicates that the Rx has successfully reached the PLL Power_Good state during the power up sequence on Lane 0. The value 1'b1 indicates that Lane 0 Rx is successful.
7:5	0h RO	Reserved
4	0h RO/V	SIG_DET_0 DWC_XPCS (SIG_DET_0): Rx Signal Detect for Lane 0 This bit indicates that the Rx detected the signal on Lane 0. This bit is the complement value of the signals input from PHY (xpcs_los_i[0]) on Lane 0. The value 1'b1 indicates that Lane 0 signal is detected.
3:0	0h RO	Reserved

11.3.1.44 VR_MII_MP_12G_16G_25G_TX_GENCTRL0 DWC_XCPs (VR_MII_MP_12G_16G_25G_TX_GENCTRL0) - Offset 1F00010060h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx General Register 0

Type	Size	Offset	Default
MMIO	16 bit	1F00010060h	1000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	1h RW	TX_DT_EN_0 DWC_XPCS (TX_DT_EN_0): Tx Data Enable on lane 0 of PHY When this bit is set, Transmit Output Driver in the PHY is enabled. This bit controls the output port 'xgxs_tx_data_en_o[0]'. This field should be cleared when PHY Tx is not in P0 power state
11:9	0h RO	Reserved
8	0h	TX_RST_0 DWC_XPCS (TX_RST_0):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	Tx Reset on lane 0 of PHY When this bit is set, PHY transmitter is reset, including common-mode adjustment and receiver detection state machines. This signal drives the output port 'xgxs_tx_reset_o[0]' when DWC_xpcs is in POWER_GOOD state.
7:5	0h RO	Reserved
4	0h RW	TX_INV_0 DWC_XPCS (TX_INV_0): Tx Invert on lane 0 of PHY When this bit is set, the data on PHY Tx serial lines are logically inverted. This signal drives the output port 'xgxs_tx_invert_o[0]'.
3:1	0h RO	Reserved
0	0h RW	TXBCN_EN_0 DWC_XPCS (TXBCN_EN_0): Tx Beacons Enable on lane 0 of PHY When this bit is set, PHY enables transmitter beaconing (LFPS). The period for transmit pulses is between 20-50ns. This field drives the output port 'xgxs_tx_beacon_en_o[0]'.

11.3.1.45 VR_MII_M_12G_16G_25G_TX_GENCTRL1 DWC_XCPs (VR_MII_MP_12G_16G_25G_TX_GENCTRL1) - Offset 1F00010062h

VR MII Synopsys Multi-protocol 12G/16G/25G PHY Tx General Register 1

Type	Size	Offset	Default
MMIO	16 bit	1F00010062h	1510h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	1h RW	TX_CLK_RDY_0 DWC_XPCS (TX_CLK_RDY_0): Transmitter Input clock ready on lane 0 This field drives the output xpcs_tx_clk_rdy_o[0]. This field should remain high, as long as PHY Tx Clock is active
11	0h RO	Reserved
10:8	5h RW	VBOOST_LVL DWC_XPCS (VBOOST_LVL): Tx Voltage Boost Maximum Level This field controls the maximum achievable Tx swing in the PHY This field drives the output port 'xpcs_tx_vboost_lvl_o[2:0]'.
7:5	0h RO	Reserved
4	1h RW	VBOOST_EN_0 DWC_XPCS (VBOOST_EN_0): Tx voltage Boost Enable on lane 0 of PHY When this bit is set, the current mode Tx Swing boost in the PHY is enabled. This bit drives the output port 'xpcs_tx_vboost_en_o[0]'.
3:1	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
0	0h RW	DET_RX_REQ_0 DWC_XPCS (DET_RX_REQ_0): Transmitter Rx-Detection request on lane 0 of PHY. This field drives the output port 'xpcs_tx_detrx_req_o[0]'. Whenever this bit is set, a receiver detection request is made towards the PHY on lane 0. Once this bit is set, it should remain high till 'TX_ACK_0' bit is read as high. When 'TX_ACK_0' is read as high, the result of the Rx Detection operation is available at field 'DETRX_RSLT_0'. After obtaining the result of 'Rx-Detect operation', this bit should be cleared. Rx Detection operation is valid only when transmitter is in P1 power state

11.3.1.46 VR_MII_MP_12G_16G_TX_GENCTRL2 DWC_XCPS (VR_MII_MP_12G_16G_TX_GENCTRL2) - Offset 1F00010064h

VR MII Synopsis Multi-protocol 12G/16G PHY Tx General Register 2

Type	Size	Offset	Default
MMIO	16 bit	1F00010062h	1510h

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved
9:8	1h RW	TX0_WIDTH DWC_XPCS (TX0_WIDTH): Tx Datapath Width on lane 0 of the PHY This field controls the width of input transmit data on lane 0. The encoding of the width is as follows: - 2'b00: 8 bit - 2'b01: 10 bit - 2'b10: 16 bit - 2'b11: 20 bit This field drives the output port xpcs_tx0_width_o[1:0].
7:5	0h RO	Reserved
4	0h RW	TX_LPD_0 DWC_XPCS (TX_LPD_0): Transmitter Lane Power Down on lane 0 of PHY This field drives the output port 'xpcs_tx_lpd_o[3:1]'. This field can be asserted to put the phy transmitter to a power state equivalent to that of P1.
3:1	0h RO	Reserved
0	0h RW	TX_REQ_0 DWC_XPCS (TX_REQ_0): Transmitter operation request on lane 0 of PHY (RW,SC Type) This bit drives the output port 'xpcs_tx_req_o[0]'. This bit can be set to initiate a new transmitter setting request. This bit should be set only if TX_ACK_0 field is low. Once this bit is set, application should monitor TX_ACK_0 field till it becomes 1'b1. This implies that the transmitter request operation has been successfully completed. Then application should clear this bit. This bit should be asserted to make sure that the PHY accepts any change to the following signals: - xpcs_tx0_pstate_o - xpcs_tx0_lpd_o - xpcs_tx0_rate_o - xpcs_tx0_width_o - xpcs_tx0_mpilbb_sel.

11.3.1.47 VR_MII_MP_12G_16G_25G_TX_BOOST_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_BOOST_CTRL) - Offset 1F00010066h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx Boost Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010066h	000Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	Reserved
3:0	Fh RW	TX0_IBOOST DWC_XPCS (TX0_IBOOST): Tx current boost level on lane 0 of the PHY This bit drives the output port xpcs_tx0_iboot_lv[3:0]. For details on how to set this field, see the PHY Databook.

11.3.1.48 VR_MII_MP_12G_16G_25G_TX_RATE_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_RATE_CTRL) - Offset 1F00010068h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx Rate Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010068h	0006h

BIOS Access	SMM Access	OS Access
None	None	None

Register Level Access:

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved
2:0	6h RW	TX0_RATE DWC_XPCS (TX0_RATE): Tx rate on lane 0 of the PHY Data rate encoding is as follows: - 3'b000: baud - 3'b001: baud/2 - 3'b010: baud/4 - 3'b011: baud/8 - 3'b111: baud/10 - 3'b100-3'b110: Not supported

11.3.1.49 VR_MII_MP_12G_16G_25G_TX_POWER_STATE_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_POWER_STATE_CTRL) - Offset 1F0001006Ah

Type	Size	Offset	Default
MMIO	16 bit	1F0001006Ah	0000h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx Power State Register

BIOS Access	SMM Access	OS Access
None	None	None

Register Level Access:

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved
8	0h RW	TX_DISABLE_0 DWC_XPCS (TX_DISABLE_0): Transmitter Disable on lane 0 This field drives the output port 'xpcs_tx_disable_o[0]'.
7:2	0h RO	Reserved
1:0	0h RW	TX0_PSTATE DWC_XPCS (TX0_PSTATE): Tx power state control for lane 0 of PHY Power state encoding is as follows: - 2'b00: P0 - 2'b01: P0s - 2'b10: P1 - 2'b11: P2

**11.3.1.50 VR_MII_MP_12G_16G_25G_TX_EQ_CTRL0 DWC_XCPS
(VR_MII_MP_12G_16G_25G_TX_EQ_CTRL0) - Offset 1F0001006Ch**

Type	Size	Offset	Default
MMIO	16 bit	1F0001006Ch	2800h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx Equalization Control 0 Register

BIOS Access	SMM Access	OS Access
None	None	None

Register Level Access:

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved
13:8	28h RW	TX_EQ_MAIN DWC_XPCS (TX_EQ_MAIN): Control for setting Tx driver output amplitude This field drives the output port 'rpcs_ktx_main_o' if 'TX_EQ_OVR_RIDE' bit of R_MII_MP_12G_16G_TX_EQ_CTRL1 Register is set or in configurations with CL72_EN=Disabled.
7:6	0h RO	Reserved
5:0	00h RW	TX_EQ_PRE DWC_XPCS (TX_EQ_PRE): Tx Pre-Emphasis level adjustment Control This field controls the transmitter driver output pre-emphasis (pre-shoot coefficient).This field drives the output port 'rpcs_ktx_pre_o' if 'TX_EQ_OVR_RIDE' bit of VR_MII_MP_12G_16G_25G_TX_EQ_CTRL1 Register is set or in configurations with CL72_EN=Disabled.

**11.3.1.51 VR_MII_MP_12G_16G_25G_TXEQ_CTRL1 DWC_XCPS
(VR_MII_MP_12G_16G_25G_TX_EQ_CTRL1) - Offset 1F0001006Eh**

Type	Size	Offset	Default
MMIO	16 bit	1F0001006Eh	0000h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx Equalization Control 1 Register

BIOS Access	SMM Access	OS Access
None	None	None

Register Level Access:

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved
5:0	00h RW	TX_EQ_POST DWC_XPCS (TX_EQ_POST): Tx Post-Emphasis level adjustment Control This field controls the transmitter driver output pre-emphasis (pre-shoot coefficient). This field drives the output port 'rpcs_ktx_post_o' if 'TX_EQ_OVR_RIDE' bit is set or in configurations with CL72_EN=Disabled.

11.3.1.52 VR_MII_MP_16G_25G_TX_GENCTRL3 DWC_XCPS (VR_MII_MP_16G_25G_TX_GENCTRL3) - Offset 1F00010078h

Type	Size	Offset	Default
MMIO	16 bit	1F00010078h	0000h

VR MII Synopsis Multi-protocol 16G/25G PHY Tx General Control 3 Register

BIOS Access	SMM Access	OS Access
None	None	None

Register Level Access:

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved
8:0	000h RW	TXUP_TERM_OFFSET DWC_XPCS (TXUP_TERM_OFFSET): Offset for TX Up Termination. This field drives the output port xpcs_txup_term_offset_o[8:0].

11.3.1.53 VR_MII_MP_16G_25G_TX_GENCTRL4 DWC_XCPS (VR_MII_MP_16G_25G_TX_GENCTRL4) - Offset 1F0001007Ah

VR MII Synopsis Multi-protocol 16G/25G PHY Tx General Control 4 Register

Type	Size	Offset	Default
MMIO	16 bit	1F0001007Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved
8:0	000h RW	TXDN_TERM_OFFSET DWC_XPCS (TXDN_TERM_OFFSET): Offset for TX Down Termination. This field drives the output port xpcs_txdn_term_offset_o[8:0]

11.3.1.54 VR_MII_MP_16G_25G_TX_MISC_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_TX_MISC_CTRL0) - Offset 1F0001007Ch

VR MII Synopsis Multi-protocol 16G/25G PHY Tx Miscellaneous Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F0001007Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved
7:0	000h RW	TX0_MISC DWC_XPCS (TX0_MISC): TX Miscellaneous control for lane0. This field drives the output port xpcs_tx0_misc_o[7:0].

11.3.1.55 VR_MII_MP_12G_16G_25G_TX_STS DWC_XCPS (VR_MII_MP_12G_16G_25G_TX_STS) - Offset 1F00010080h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Tx Status Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010080h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4	0h RO/V	DETRX_RSLT_0 DWC_XPCS (DETRX_RSLT_0): Receiver Detection Result on lane 0 This field captures the value of the input port 'xpcs_tx_detrx_result_i[0]'. The value of this field is valid when 'TX_ACK_0' is high. - 1'b0: Receiver not detected - 1'b1: Receiver detected
3:1	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
0	0h RO/V	TX_ACK_0 DWC_XPCS (TX_ACK_0): Tx Acknowledge on lane 0 of PHY This bit captures the value of the input port 'xpcs_tx_ack_i[0]'. Whenever this bit is read as high, it indicates that the requested transmitter setting is complete or the requested RX-detection operation is complete. After this bit is read high, it remains high till bit TX_REQ_0 or DET_RX_REQ_0 is cleared

11.3.1.56 VR_MII_MP_12G_16G_25G_RX_GENCTRL0 DWC_XCPs (VR_MII_MP_12G_16G_25G_RX_GENCTRL0) - Offset 1F000100A0h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx General Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100A0h	0101h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RO/V	RX_CLKSFT_0 DWC_XPCS (RX_CLKSFT_0): Rx clock shift on lane 0 of Multi-protocol 12G PHY When this bit is set, a 1-bit shift of receive data happens relate to receive clock. This operation works only if alignment enable is disabled. This bit drives the output port 'xpcs_rx_clk_shift_o[0]'. This field is reserved for multi-protocol 16G/25G PHY configurations.
11:9	0h RO	Reserved
8	1h RW	RX_DT_EN_0 DWC_XPCS (RX_DT_EN_0): Rx Data Enable on lane 0 of PHY This bit should be set to enable the PHY receiver data output on lane 0. This bit drives the output port 'xgxs_rx_data_en_o[0]'.
7:5	0h RO	Reserved
4	0h RO/V	RX_ALIGN_EN_0 DWC_XPCS (RX_ALIGN_EN_0): Rx Data Alignment Enable on lane 0 of Multi-protocol 12G PHY This bit can be set to enable word alignment (based on k28.5 character) in the PHY. This field drives the output port 'xgxs_rx_align_en_o[0]'. This field is reserved for multi-protocol 16G/25G PHY configurations.
3:1	0h RO	Reserved
0	1h RW	RX_TERM_EN_0 DWC_XPCS (RX_TERM_EN_0): Rx Termination Enable on lane 0 of PHY When this bit is set, PHY Rx is terminated with a nominal 50 ohm resistance. Otherwise, the termination is in high impedance. This field drives the output port 'xpcs_rx_term_en_o[0]'.

11.3.1.57 VR_MII_MP_12G_16G_25G_RX_GENCTRL1 DWC_XPCS (VR_MII_MP_12G_16G_25G_RX_GENCTRL1) - Offset 1F000100A2h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx General Control 1 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100A2h	0100h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RW	RX_DIV16P5_CLK_EN_0 DWC_XPCS (RX_DIV16P5_CLK_EN_0): Receiver Divide by 16.5 output clock on lane 0 When this bit is set, it enables the divide by 16.5 Rx VCO recovered clock. This clock is available at rx0_div16p5_clk output port of PHY. This bit must be set when operating in PCS-R mode.
11:9	0h RO	Reserved
8	1h RW	RX_TERM_ACDC_0 DWC_XPCS (RX_TERM_ACDC_0): Rx Termination control on lane 0 of PHY. - 0: DC Termination (Floating Rx) - 1: AC Termination (Grounded Rx) This field drives the output port xpcs_rx_term_acdc_o[0].
7:5	0h RO	Reserved
4	0h RO/V	RX_RST_0 DWC_XPCS (RX_RST_0): Rx reset on lane 0 of PHY When this bit is set, RX data path, all the receiver settings and state machines of the PHY are reset This field drives the output port xgxs_rx_reset_o[0] when DWC_xpcs is in POWER_GOOD state.
3:1	0h RO	Reserved
0	0h RW	RX_INV_0 DWC_XPCS (RX_INV_0): Rx Data Invert on lane 0 of PHY When this bit is set, the data on PHY Rx serial lines are logically inverted. This signal drives the output port xgxs_rx_invert_o[0].

11.3.1.58 VR_MII_MP_12G_16G_25G_RX_GENCTRL2 DWC_XPCS (VR_MII_MP_12G_16G_RX_GENCTRL2) - Offset 1F000100A4h

VR MII Synopsis Multi-protocol 12G/16G PHY Rx General Control 2 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100A4h	0100h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved
9:8	1h RW	RX0_WIDTH DWC_XPCS (RX0_WIDTH): Rx Datapath Width on lane 0 of the PHY This field controls the width of output receive data from PHY on lane 3. The encoding of the width is as follows: - 2'b00: 8-bit - 2'b01: 10-bit - 2'b10: 16-bit - 2'b11: 20-bit This field drives the output port xpcs_rx0_width[1:0].
7:5	0h RO	Reserved
4	0h RO/V	RX_LPD_0 DWC_XPCS (RX_LPD_0): Receiver Lane Power Down on lane 0 of PHY This bit can be set to power down the receiver to a power state equivalent to that of P1. This bit drives the output port 'xpcs_rx_lpd_o[0]'.
3:1	0h RO	Reserved
0	0h RW	RX_REQ_0 DWC_XPCS (RX_REQ_0): Receiver operation request on lane 0 of PHY (RW,SC Type). This bit can be set to 1 by the application. This bit is self-cleared when 'xpcs_tx_ack_i[0]' is asserted. When this bit is set, a new receiver setting request is made towards the PHY. This bit drives the output port xpcs_rx_req_o[0]. Whenever this bit is set, PHY captures its following input signals: - rx0_pstate[1:0] - rx0_lpd - rx0_rate[1:0] - rx0_width[1:0] - rx0_data_en - rx0_adapt_afe_en - rx0_adapt_dfe_en - rx0_eq_att_lv[2:0] - rx0_eq_vga1_gain[3:0] - rx0_eq_vga2_gain[3:0] - rx0_eq_ctle_pole[2:0] - rx0_eq_ctle_boost[4:0] - rx0_eq_dfe_tap1[7:0] A successful completion of receiver request operation on lane 0 is indicated by bit RX_ACK_0.

11.3.1.59 VR_MII_MP_12G_16G_25G_RX_GENCTRL3 DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_GENCTRL3) - Offset 1F000100A6h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx General Control 3 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100A6h	0002h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RW	LOS_LFPS_EN_0 DWC_XPCS (LOS_LFPS_EN_0): Rx LOS LFPS Enable on lane 0 of the PHY This field drives the output port xpcs_rx_los_lfps_en_o[0] to enable the LFPS filter on lane 0 of the PHY.
11:3	0h RO	Reserved
2:0	0h RO/V	LOS_TRSHLD_0 DWC_XPCS (LOS_TRSHLD_0): Loss of signal threshold on lane 0 of PHY. This field drives the output port xpcs_rx0_los_threshold_o[2:0]. Threshold voltages for various values are as follows: - 3'b000: Reserved - 3'b001: 90 mVpp - 3'b010: 120 mVpp - 3'b011: 150 mVpp - 3'b100: 180 mVpp - 3'b101: 210 mVpp - 3'b110: 240 mVpp - 3'b111: 270 mVpp

11.3.1.60 VR_MII_MP_12G_16G_25G_RX_RATE_CTRL DWC_XCPs (VR_MII_MP_12G_16G_25G_RX_RATE_CTRL) - Offset 1F000100A8h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx Rate Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100A8h	0003h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved
1:0	3h RW	RX0_RATE DWC_XPCS (RX0_RATE): Rx date rate on lane 0 of the PHY Data Rate Encoding for Multi-protocol 25G PHY is as follows: - 3'b000: baud - 3'b001: baud/2 - 3'b010: baud/4 - 3'b011: baud/8 - 3'b100: baud/16 Data Rate Encoding for Multi-protocol 12G/16G PHY is as follows: - 2'b00: baud - 2'b01: baud/2 - 2'b10: baud/4 - 2'b11: baud/8

11.3.1.61 VR_MII_MP_12G_16G_25G_RX_POWER_STATE_CTRL DWC_XCPs (VR_MII_MP_12G_16G_25G_RX_POWER_STATE_CTRL) - Offset 1F000100AAh

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx Power State Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100AAh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RW	EEE_OVR_RIDE DWC_XPCS (EEE_OVR_RIDE): Rx Power state override control during EEE DWC_xpcs switches Rx power state to P0s by itself during Rx QUIET state of EEE to save power in the PHY. Set this bit to 1, to override this behavior. When this bit is set, Rx power state remains unchanged during Rx EEE and retains the values as programmed in the 'RX{lane}_PSTATE' fields of this register.
11:9	0h RO	Reserved
8	0h RW	RX_DISABLE_0 DWC_XPCS (RX_DISABLE_0):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Receiver Disable on lane 0 This bit can be set in P1 power state to put the receiver in a low-power mode. This field drives the output port 'xpcs_rx_disable_o[0]'.
7:2	0h RO	Reserved
1:0	0h RW	RX0_PSTATE DWC_XPCS (RX0_PSTATE): Rx power state control for lane 0 of PHY Power state encoding is as follows: - 2'b00: P0 - 2'b01: P0s - 2'b10: P1 - 2'b11: P2

11.3.1.62 VR_MII_MP_12G_16G_25G_RX_CDR_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_CDR_CTRL) - Offset 1F000100ACh

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx CDR Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100ACh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4	0h RW	CDR_SSC_EN_0 DWC_XPCS (CDR_SSC_EN_0): Rx CDR SSC Mode Enable on lane 0 of the PHY This field controls the CDR tracking gains and duration. This bit should be set to 1 when receive data has a spread spectrum clock and should be cleared if receive data does not have SSC. This bit drives the output port 'xpcs_rx_cdr_ssc_en_o[0]'.
3:0	0h RO	Reserved

11.3.1.63 VR_MII_MP_12G_16G_25G_RX_ATTN_CTRL DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_ATTN_CTRL) - Offset 1F000100AEh

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx Attenuation Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100AEh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
2:0	0h RW	RX0_EQ_ATT_LVL DWC_XPCS (RX0_EQ_ATT_LVL): Rx Equalization Attenuation level for lane 0 of the PHY This field drives the output port xpcs_rx0_eq_att_lvl_o[2:0]. This field controls the AFE attenuation level of the PHY.

11.3.1.64 VR_MII_MP_16G_25G_RX_EQ_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_EQ_CTRL0) - Offset 1F000100B0h

VR MII Synopsis Multi-protocol 16G/25G PHY Rx Equalization Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100B0h	4406h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved
14:12	4h RW	VGA1_GAIN_0 DWC_XPCS (VGA1_GAIN_0): Rx Equalization VGA1 Gain on lane 0 of the PHY This field drives the output port xpcs_rx0_eq_vga1_gain_o[3:0]. This field controls the AFE first stage Variable Gain amplifier gain.
11	0h RO	Reserved
10:8	4h RW	VGA2_GAIN_0 DWC_XPCS (VGA2_GAIN_0): Rx Equalization VGA2 Gain on lane 0 of the PHY This field drives the output port xpcs_rx0_eq_vga2_gain_o[3:0].This field controls the AFE second stage Variable Gain amplifier gain.
7	0h RO	Reserved
6:5	0h RW	CTLE_POLE_0 DWC_XPCS (CTLE_POLE_0): Rx Equalization CTLE Pole Value on lane 0 of the PHY This field drives the output port xpcs_rx0_eq_ctle_pole_o[2:0].This field controls the continuous time linear equalizer boost pole location of the PHY.
4:0	06h RW	CTLE_BOOST_0 DWC_XPCS (CTLE_BOOST_0): Rx Equalization CTLE Boost value on lane 0 of the PHY This field drives the output port xpcs_rx0_eq_ctle_boost_o[4:0].This field controls the CTLE boost level.

11.3.1.65 VR_MII_MP_12G_16G_25G_RX_EQ_CTRL4 DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_EQ_CTRL4) - Offset 1F000100B8h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx Equalization Control 4 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100B8h	0010h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RW	RX_AD_REQ DWC_XPCS (RX_AD_REQ): Receive Adaptation Request This bit drives the 'rpcs_krx_adapt_req_o' port. Software can set this bit to make an Receiver Adaptation Request to the PHY. The acknowledgment from the PHY (for the adaptation request made) is reflected in bit[12] (RX_ADPT_ACK) of VR_MII_MP_12G_16G_25G_MISC_STS Register. After receiving the acknowledgment, software should clear this register field.
11:5	0h RO	Reserved
4	1h RW	CONT_OFF_CAN_0 DWC_XPCS (CONT_OFF_CAN_0): Receiver offset cancellation continuous operation on lane 0 This bit can be set if continuous receiver offset cancellation is required. If this bit is 0, offset cancellation runs when receiver exits P2 power state. This bit drives the output port 'xpcs_rx_offcan_cont_o[0]'.
7	0h RO	Reserved
3:1	0h RO	Reserved
0	0h RW	CONT_ADAPT_0 DWC_XPCS (CONT_ADAPT_0): Receiver Adaptation Continuous Operation on lane 0 This bit can be set to enable continuous receiver adaptation in the PHY. This bit drives the output port 'xpcs_rx_offcan_cont_o'.

11.3.1.66 VR_MII_MP_16G_25G_RX_EQ_CTRL5 DWC_XCPs (VR_MII_MP_16G_25G_RX_EQ_CTRL5) - Offset 1F000100BAh

VR MII Synopsis Multi-protocol 16G/25G PHY Rx Equalization Control 5 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100BAh	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RW	RX_ADPT_PROG_0 DWC_XPCS (RX_ADPT_PROG_0): Receiver Adaptation in Progress -lane 0 This field drives the output port xpcs_rx_adpt_in_prog_o[0].
11:6	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO	
5:4	0h RW	RX0_ADPT_MODE DWC_XPCS (RX0_ADPT_MODE): RX Adaptation for lane0 This field drives the output port xpcs_rx0_adpt_mode_o[1:0].
3:1	0h RO	Reserved
0	0h RW	RX_ADPT_SEL_0 DWC_XPCS (RX_ADPT_SEL_0): Select Storage Bank for RX adaptation on Lane0 This field drives the output port xpcs_rx_dfe_adapt_sel_o[0].

11.3.1.67 VR_MII_MP_12G_16G_25G_DFE_TAP_CTRL0 DWC_XCPS (VR_MII_MP_12G_16G_25G_DFE_TAP_CTRL0) - Offset 1F000100BCh

VR MII Synopsis Multi-protocol 12G/16G/25G PHY DFE Tap Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100BCh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved
7:0	00h RW	DFE_TAP1_0 DWC_XPCS (DFE_TAP1_0): Rx Equalization DFE Tap1 value on lane 0 of the PHY This field drives the output port xpcs_rx0_eq_dfe_tap1_o[7:0]

11.3.1.68 VR_MII_MP_12G_16G_25G_RX_STS DWC_XCPS (VR_MII_MP_12G_16G_25G_RX_STS) - Offset 1F000100C0h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Rx Status Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100C0h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved
8	0h	HF_SD_0 DWC_XPCS (HF_SD_0):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	Multi-protocol 25G PHY or For Multi-protocol 10G Gen2 PHY configurations: Highfrequency Signal Detect on lane 0. This field captures the value of the input port 'xpcs_rx_sigdet_hf_i[0]'. >For Other configurations: Reserved
7:5	0h RO	Reserved
4	0h RO/V	LF_SD_0 DWC_XPCS (LF_SD_0): For Multi-protocol 25G PHY or Multi-protocol 10G Gen2 PHY configurations: Lowfrequency Signal Detect on lane 0. This field captures the value of the input port 'xpcs_rx_sigdet_lf_i[0]'. For Other configurations: Reserved
3:1	0h RO	Reserved
0	0h RO/V	RX_ACK_0 DWC_XPCS (RX_ACK_0): Rx Acknowledge on lane 0 of PHY This bit captures the value of the input port xpcs_rx_ack_i[0]. If this bit is set, it indicates that the requested receiver setting is complete. This bit forms a hand-shake with 'RX_REQ_0' bit. Once this bit is set, RX_REQ_0 bit is self-cleared.

11.3.1.69 VR_MII_MP_16G_25G_RX_PPM_STS0 DWC_XCPS (VR_MII_MP_16G_25G_RX_PPM_STS0) - Offset 1F000100C2h

VR MII Synopsis Multi-protocol 16G/25G PHY Rx PPM Status 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100C2h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved
5:0	00h RO/V	RX0_PPM_DRIFT DWC_XPCS (RX0_PPM_DRIFT): RX CDR PPM Drift on lane 0 This field is driven by the input port xpcs_rx0_ppm_drift_i[5:0].

11.3.1.70 VR_MII_MP_16G_RX_CDR_CTRL1 DWC_XCPS (VR_MII_MP_16G_RX_CDR_CTRL1) - Offset 1F000100C8h

VR MII Synopsis Multi-protocol 16G PHY Rx CDR Control 1 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100C8h	0110h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved
9:8	1h RW	VCO_FRQBAND_0 DWC_XPCS (VCO_FRQBAND_0): RX CDR VCO Frequency Band lane0 This field drives the output port xpcs_vco_freqband0_o[1:0].
7:5	0h RO	Reserved
4	1h RW	VCO_STEP_CTRL_0 DWC_XPCS (VCO_STEP_CTRL_0): RX_CDR VCO Step Control Lane 0 This field drives the output port xpcs_vco_step_ctrl_o[0].
3:1	0h RO	Reserved
0	0h RW	VCO_TEMP_COMP_EN_0 DWC_XPCS (VCO_TEMP_COMP_EN_0): RX_CDR VCO Temperature Compensation Enable Lane 0 This field drives the output port xpcs_vco_temp_comp_en_o[0].

11.3.1.71 VR_MII_MP_16G_25G_RX_PPM_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_PPM_CTRL0) - Offset 1F000100CAh

VR MII Synopsis Multi-protocol 16G/25G PHY Rx PPM Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100CAh	0013h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4:0	13h RW	RX0_CDR_PPM_MAX DWC_XPCS (RX0_CDR_PPM_MAX): Maximum Allowed PPM on the RX0 CDR Clock This field drives the output port xpcs_rx0_cdr_ppm_max_o[4:0].

11.3.1.72 VR_MII_MP_16G_25G_RX_GENCTRL4 DWC_XCPS (VR_MII_MP_16G_25G_RX_GENCTRL4) - Offset 1F000100D0h

VR MII Synopsis Multi-protocol 16G/25G PHY Rx General Control 4 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100D0h	0100h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RO/V	RX_125MHZ_CLK_EN_0 DWC_XPCS (RX_125MHZ_CLK_EN_0): RX 125MHz clock generation Enable on Lane 0 This field drives the output port xpcs_rx_125mhz_clk_en_o[0].
11:9	0h RO	Reserved
8	1h RW	RX_DFE_BYP_0 DWC_XPCS (RX_DFE_BYP_0): RX DFE Bypass Enable on Lane 0 This field drives the output port xpcs_rx_dfe_bypass_o[0].
7:5	0h RO	Reserved
4:0	00h RW	RX_TERM_OFFSET DWC_XPCS (RX_TERM_OFFSET): Offset for RX Termination This field drives the output port xpcs_rx_term_offset_o[4:0].

11.3.1.73 VR_MII_MP_16G_25G_RX_MISC_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_MISC_CTRL0) - Offset 1F000100D2h

VR MII Synopsis Multi-protocol 16G/25G PHY Rx General Control 4 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100D2h	0047h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved
7:0	47h RW	RX0_MISC DWC_XPCS (RX0_MISC): RX Miscellaneous control for lane0. This field drives the output port xpcs_rx0_misc_o[7:0].

11.3.1.74 VR_MII_MP_16G_25G_RX_IQ_CTRL0 DWC_XCPS (VR_MII_MP_16G_25G_RX_IQ_CTRL0) - Offset 1F000100D6h

VR MII Synopsis Multi-protocol 16G/25G PHY Rx IQ Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100D6h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	Reserved
11:8	0h RW	RX0_DELTA_IQ DWC_XPCS (RX0_DELTA_IQ): RX IQ Offset Value for lane0. This field drives the output port xpcs_rx0_delta_iq_o[3:0].
7	0h RO	Reserved
6:0	00h RW	RX0_MARGIN_IQ DWC_XPCS (RX0_MARGIN_IQ): Value of RX IQ Margining on lane0. This field drives the output port xpcs_rx0_margin_iq_o[6:0].

11.3.1.75 VR_MII_MP_12G_16G_25G_MPLL_CMN_CTRL_DWC_XCPS (VR_MII_MP_12G_16G_25G_MPLL_CMN_CTRL) - Offset 1F000100E0h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY MPLL Common Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100E0h	0011h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4	1h RW	MPLL_B_SEL_0 DWC_XPCS (MPLL_B_SEL_0): Tx MPLL Select-lane 0 When this bit is set, PHY selects MPLL_B to generate Tx analog clocks on lane 0
3:1	0h RO	Reserved
0	1h RW	MPLL_EN_0 DWC_XPCS (MPLL_EN_0): Tx MPLL Enable-lane 0 This bit should be set to power-up the MPLL. This bit should be 1, for normal operation.

11.3.1.76 VR_MII_MP_12G_16G_MPLLA_CTRL0_DWC_XCPS (VR_MII_MP_12G_16G_MPLLA_CTRL0) - Offset 1F000100E2h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY MPLLA Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100E2h	00C1h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	MPLLA_CAL_DISABLE DWC_XPCS (MPLLA_CAL_DISABLE): MPLLA Calibration Disable This field can be programmed to 1, to disable calibration of MPLLA by PHY firmware.
14:11	0h RO	Reserved
10:8	0h RO/V	MPLLA_SSC_CLK_SEL DWC_XPCS (MPLLA_SSC_CLK_SEL): This field controls MPLLA spread-spectrum clock select of Multi-protocol 10G PHY. For other configurations, this is a reserved field.
7:0	C1h RW	MPLLA_MULTIPLIER DWC_XPCS (MPLLA_MULTIPLIER): MPLLA frequency Multiplier Control This field controls the multiplication of reference clock to a frequency suitable for operating speed Any change in this field should be followed by a Vendor-specific Soft Reset to ensure that PHY is properly powered-up in the desired mode.

11.3.1.77 VR_MII_MP_16G_MPLLA_CTRL1 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL1) - Offset 1F000100E4h

VR MII Synopsis Multi-protocol 16G PHY MPLLA Control 1 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100E4h	3100h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	188h RW	MPLLA_FRACN_CTRL DWC_XPCS (MPLLA_FRACN_CTRL): MPLLA Fractional Control This field drives the output port xpcs_mplla_fracn_ctrl_o.
4	0h RW	MPLLA_SSC_CLK_SEL DWC_XPCS (MPLLA_SSC_CLK_SEL): MPLLA SSC Clock Select This field drives the output port xpcs_mplla_ssc_clk_sel_o.
3:1	0h RO	Reserved
0	0h RW	MPLLA_SSC_EN DWC_XPCS (MPLLA_SSC_EN): MPLLA SSC Enable This field can be set to enable spread-spectrum generation on mplla_div_clk output.

11.3.1.78 VR_MII_MP_12G_16G_MPLLA_CTRL2 DWC_XCPS (VR_MII_MP_12G_16G_MPLLA_CTRL2) - Offset 1F000100E6h

VR MII Synopsis Multi-protocol 12G/16G PHY MPLLA Control 2 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100E6h	0200h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved
14:13	0h RW	MPLL_A_RECAL_BANK_SEL DWC_XPCS (MPLL_A_RECAL_BANK_SEL): MPLL_B Re-calibration Bank Select This field drives the output port 'xpc_s_mplla_recal_bank_sel_o [1:0]'.
12:11	0h RW	MPLL_A_TX_CLK_DIV DWC_XPCS (MPLL_A_TX_CLK_DIV): MPLL_A Tx Clock Divider This field drives the output port 'xpc_s_mplla_tx_clk_div_o[1:0]'. This field is present only for Multi-protocol 16G configurations and Multi-protocol 10G PHY configurations.
10	0h RW	MPLL_A_DIV16P5_CLK_EN DWC_XPCS (MPLL_A_DIV16P5_CLK_EN): MPLL_A Divide by 16.5 Enable This bit can be set to enable output clocks derived from MPLL_A based on 16.5,33 and 66 division ratios.
9	1h RW	MPLL_A_DIV10_CLK_EN DWC_XPCS (MPLL_A_DIV10_CLK_EN): MPLL_A Divide by 10 Enable When this bit is set, the frequency of the mpla_word_clk output clock from PHY is MPLL_A frequency divided by 10.
8	0h RW	MPLL_A_DIV8_CLK_EN DWC_XPCS (MPLL_A_DIV8_CLK_EN): MPLL_A Divide by 8 Enable When this bit is set, the frequency of the mpla_word_clk output clock from PHY is MPLL_A frequency divided by 8.
7	0h RW	MPLL_A_DIV_CLK_EN DWC_XPCS (MPLL_A_DIV_CLK_EN): Enable mpla_div_clk from PHY. When asserted, the frequency of mpla_div_clk from PHY is the MPLL_A frequency divided by 'mplla_div_multiplier'.
6:0	00h RW	MPLL_A_DIV_MULT DWC_XPCS (MPLL_A_DIV_MULT): MPLL_A Output Frequency Multiplier Control This field controls the frequency multiplication factor used to generate MPLL_A clock output from the reference clock input as seen by the MPLL.

11.3.1.79 VR_MII_MP_12G_16G_MPLL_B_CTRL0 DWC_XCPs (VR_MII_MP_12G_16G_MPLL_B_CTRL0) - Offset 1F000100E8h

VR MII Synopsis Multi-protocol 12G/16G PHY MPLL_B Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100E8h	00CEh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	MPLL_B_CAL_DISABLE DWC_XPCS (MPLL_B_CAL_DISABLE): MPLL_B Calibration Disable This field can be programmed to 1, to disable calibration of MPLL_B by PHY firmware.
14:11	0h	Reserved

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	
10:8	0h RW	MPLL_A_TX_CLK_DIV DWC_XPCS (MPLL_A_TX_CLK_DIV): MPLL_A Tx Clock Divider This field drives the output port 'xpcs_mplla_tx_clk_div_o[1:0]'. This field is present only for Multi-protocol 16G configurations and Multi-protocol 10G PHY configurations.
7:0	CEh RW	MPLL_B_MULTIPLIER DWC_XPCS (MPLL_B_MULTIPLIER): MPLL_B frequency Multiplier Control This field controls the multiplication of reference clock to a frequency suitable for operating speed Any change in this field should be followed by a Vendor-specific Soft Reset to ensure that PHY is properly powered-up in the desired mode.

11.3.1.80 VR_MII_MP_16G_MPLL_B_CTRL1 DWC_XCPs (VR_MII_MP_16G_MPLL_B_CTRL1) - Offset 1F000100EAh

VR MII Synopsis Multi-protocol 16G PHY MPLL_B Control 1 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100EAh	3100h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	188h RW	MPLL_B_FRACN_CTRL DWC_XPCS (MPLL_B_FRACN_CTRL): MPLL_B Fractional Control This field drives the output port 'xpcs_mpllb_fracn_ctrl_o'.
4	0h RW	MPLL_B_SSC_CLK_SEL DWC_XPCS (MPLL_B_SSC_CLK_SEL): MPLL_B Spread Spectrum Clock Select This field drives the output port 'xpcs_mpllb_ssc_clk_sel_o'
3:1	0h RO	Reserved
0	0h RW	MPLL_B_SSC_EN DWC_XPCS (MPLL_B_SSC_EN): MPLL_B Spread Spectrum Enable This field can be set to enable spread-spectrum generation on mplla_div_clk output.This bit drives the output port xpcs_mpllb_ssc_en_o.

11.3.1.81 VR_MII_MP_12G_16G_MPLL_B_CTRL2 DWC_XCPs (VR_MII_MP_12G_16G_MPLL_B_CTRL2) - Offset 1F000100ECh

VR MII Synopsis Multi-protocol 12G/16G PHY MPLL_B Control 2 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100EAh	029Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved
14:13	0h RW	MPLL_B_RECAL_BANK_SEL DWC_XPCS (MPLL_B_RECAL_BANK_SEL): MPLL_B Re-calibration Bank Select This field drives the output port 'xpcs_mpllb_recal_bank_sel_o [1:0]'
12:11	0h RW	MPLL_B_TX_CLK_DIV DWC_XPCS (MPLL_B_TX_CLK_DIV): MPLL_B Tx Clock Divider This field drives the output port 'xpcs_mpllb_tx_clk_div_o[1:0]'. This field is present only for Multi-protocol 16G/Multi-protocol 10G PHY configurations.
10	0h RO	Reserved
9	1h RW	MPLL_B_DIV10_CLK_EN DWC_XPCS (MPLL_B_DIV10_CLK_EN): MPLL_B Divide by 10 Enable When this bit is set, the frequency of the mpllb_word_clk output clock from PHY is MPLLB frequency divided by 10.
8	0h RW	MPLL_B_DIV8_CLK_EN DWC_XPCS (MPLL_B_DIV8_CLK_EN): MPLL_B Divide by 8 Enable When this bit is set, the frequency of the mpllb_word_clk output clock from PHY is MPLLB frequency divided by 8.
7	1h RW	MPLL_B_DIV_CLK_EN DWC_XPCS (MPLL_B_DIV_CLK_EN): Enable mpllb_div_clk from PHY When asserted, the frequency of mpllb_div_clk output from PHY is MPLLB frequency divided by 'mpllb_div_multiplier'
6:0	1Eh RW	MPLL_B_DIV_MULT DWC_XPCS (MPLL_B_DIV_MULT): MPLL_B Output Frequency Multiplier Control This field controls the frequency multiplication factor used to generate MPLLB clock output from the reference clock input as seen by the MPLL.

11.3.1.82 VR_MII_MP_16G_MPLLA_CTRL3 DWC_XCPs (VR_MII_MP_16G_MPLLA_CTRL3) - Offset 1F000100EEh

VR MII Synopsis Multi-protocol 16G PHY MPLLA Control 3 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100EEh	F01Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	F01Ch RW	MPLL_A_BANDWIDTH DWC_XPCS (MPLL_A_BANDWIDTH): MPLL_A Bandwidth Control This field controls the bandwidth of MPLLA present in Multiprotocol 16G PHY. This field drives the output port 'xpcs_mplla_bandwidth_o'.

11.3.1.83 VR_MII_MP_16G_MPLL_B_CTRL3 DWC_XCPs (VR_MII_MP_16G_MPLL_B_CTRL3) - Offset 1F000100F0h

VR MII Synopsis Multi-protocol 16G PHY MPLLA Control 3 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100F0h	A02Ch

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	A02Ch RW	MPLL_B_BANDWIDTH DWC_XPCS (MPLL_B_BANDWIDTH): MPLL Bandwidth Control This field controls the bandwidth of MPLLB present in Multiprotocol 16G PHY. This field drives the output port 'xpcs_mpllb_bandwidth_o'.

11.3.1.84 VR_MII_MP_16G_MPLLA_CTRL4 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL4) - Offset 1F000100F2h

VR MII Synopsis Multi-protocol 16G PHY MPLLA Control 4 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100F2h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	Reserved
11:0	000h RW	MPLL_A_SSC_FRQ_CNT_INIT DWC_XPCS (MPLL_A_SSC_FRQ_CNT_INIT): MPLL_A SSC Frequency Counter Initialization. This field drives the output port xpcs_mplla_ssc_freq_cnt_init_o[11:0].

11.3.1.85 VR_MII_MP_16G_MPLLA_CTRL5 DWC_XCPS (VR_MII_MP_16G_MPLLA_CTRL5) - Offset 1F000100F4h

VR MII Synopsis Multi-protocol 16G PHY MPLLA Control 5 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100F4h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved
9	000h	MPLL_ST_LK_EN DWC_XPCS (MPLL_ST_LK_EN):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	MPLL A Short Lock Enable This field drives the xpcs_mpll_a_short_lock_en_o port.
8	0h RW	MPLL A SSC SPD_EN DWC_XPCS (MPLL_A_SSC_SPD_EN): MPLL A SSC Up Spread Enable. This field drives the output port xpcs_mpll_a_ssc_spd_en_o.
7:0	00 RW	MPLL A SSC FRQ_CNT_PK DWC_XPCS (MPLL_A_SSC_FRQ_CNT_PK): MPLL A SSC Frequency Counter Peak. This field drives the output port xpcs_mpll_a_ssc_freq_cnt_pk_o[7:0].

11.3.1.86 VR_MII_MP_16G_MPLL_B_CTRL4 DWC_XCPS (VR_MII_MP_16G_MPLL_B_CTRL4) - Offset 1F000100F6h

VR MII Synopsis Multi-protocol 16G PHY MPLL B Control 4 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100F6h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	Reserved
11:0	000h RW	MPLL B SSC FRQ_CNT_INIT DWC_XPCS (MPLL_B_SSC_FRQ_CNT_INIT): MPLL B SSC Frequency Counter Initialization. This field drives the output port xpcs_mpll_b_ssc_freq_cnt_init_o[11:0].

11.3.1.87 VR_MII_MP_16G_MPLL_B_CTRL5 DWC_XCPS (VR_MII_MP_16G_MPLL_B_CTRL5) - Offset 1F000100F8h

VR MII Synopsis Multi-protocol 16G PHY MPLL B Control 5 Register

Type	Size	Offset	Default
MMIO	16 bit	1F000100F8h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved
9	0h	MPLL B ST_LK_EN DWC_XPCS (MPLL_B_ST_LK_EN):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RO/V	MPLL Short Lock Enable This field drives the xpcs_mplla_short_lock_en_o port.
8	0h RW	MPLL_SSC_SPD_EN DWC_XPCS (MPLL_SSC_SPD_EN): MPLL SSC Up Spread Enable. This field drives the output port xpcs_mpllb_ssc_spd_en_o.
7:0	00h RW	MPLL_SSC_FRQ_CNT_PK DWC_XPCS (MPLL_SSC_FRQ_CNT_PK): MPLL SSC Frequency Counter Peak. This field drives the output port xpcs_mpllb_ssc_freq_cnt_pk_o[7:0].

11.3.1.88 VR_MII_MP_12G_16G_25G_MISC_CTRL0 DWC_XCPs (VR_MII_MP_12G_16G_25G_MISC_CTRL0) - Offset 1F00010120h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Miscellaneous Control 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010120h	5100h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	PLL_CTRL DWC_XPCS (PLL_CTRL): PLL Re-initialization Control If the PHY PLL does not lock for a long time, DWC_xpcs initiates a Rx power-state change from P0 to P1 and then back to P0, if this bit is set. This process is done to re-initialize the PLL. The time duration to wait before reinitializing the PLL is determined by VR_MII_MP_12G_16G_25G_MISC_CTRL1 Register
14	1h RW	CR_PARA_SEL DWC_XPCS (CR_PARA_SEL): Select CR Para Port This bit select the interface for accessing PHY registers * 0 -JTAG * 1 - CR parallel port This bit should be changed only after disabling 'jtag_tck' to PHY.
13	0h RW	RTUNE_REQ DWC_XPCS (RTUNE_REQ): Resistor Tuning Request This bit can be set to trigger a resistor tune request to the PHY. This bit controls the 'xgxs_rtune_req_o' output port.
12:8	11h RW	RX_VREF_CTRL DWC_XPCS (RX_VREF_CTRL): Rx Biasing Current Control This field drives the output port 'xpcs_rx_vref_ctrl_o[4:0]'. This field sets the Rx biasing current for Rx analog front end.
7:5	0h RO	Reserved
4	0h RW	RX2TX_LB_EN_0 DWC_XPCS (RX2TX_LB_EN_0): Enable Parallel Rx-to-Tx Loopback on lane 0 When this bit is set, recovered parallel data from PHY receiver is looped back to the transmit serializer. This loop-back takes place internal to the PHY (not within DWC_xpcs).
3:1	0h RO	Reserved
0	0h RW	TX2RX_LB_EN_0 DWC_XPCS (TX2RX_LB_EN_0): Enable Analog Tx-to-Rx Serial Loopback on lane 0 This bit can be set to enable serial loopback in the PHY from Tx pre-driver to Rx analog front-end.

11.3.1.89 VR_MII_MP_12G_16G_25G_REF_CLK_CTRL DWC_XPCS (VR_MII_MP_12G_16G_25G_REF_CLK_CTRL) - Offset 1F00010122h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY Reference Control Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010122h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	REF_MPLL_B_DIV DWC_XPCS (REF_MPLL_B_DIV): For Multi-protocol 25G PHY or Multi-protocol 10G Gen2 PHY configurations: This field drives the xpcs_ref_clk_mppll_b_div_o port. For other configurations: Reserved
12:10	0h RO/V	REF_MPLLA_DIV DWC_XPCS (REF_MPLLA_DIV): For Multi-protocol 25G PHY or Multi-protocol 10G Gen2 PHY configurations: This field drives the xpcs_ref_clk_mplla_div_o port. For other configurations: Reserved
9	0h RO	Reserved
8	0h RW	REF_RPT_CLK_EN DWC_XPCS (REF_RPT_CLK_EN): Repeat Reference Clock Enable If this bit is set, ref_repeat_clk_{p,m} clock from PHY is enabled.
7	0h RW	REF_MPLL_B_DIV2 DWC_XPCS (REF_MPLL_B_DIV2): MPPLL_B Reference Clock Divider Control The reference clock used for MPPLL_B calibration and locking can be divided by 2 by setting this bit to 1. This division is applied after ref_clk_div2_en. Therefore, the total division ratio (from the input reference clock) can be 1, 2 or 4
6	0h RW	REF_MPLLA_DIV2 DWC_XPCS (REF_MPLLA_DIV2): MPPLA Reference Clock Divider Control The reference clock used for MPPLA calibration and locking can be divided by 2 by setting this bit to 1. This division is applied after ref_clk_div2_en. Therefore, the total division ratio (from the input reference clock) can be 1, 2 or 4
5:3	0h RW	REF_RANGE DWC_XPCS (REF_RANGE): Input Reference Clock Range This field specifies the frequency range of the input reference clock (post ref_clk_div2_en division if any). The code mapping of REF_RANGE is as follows: - 3'b000: 20 - 26 MHz - 3'b001: 26.1 - 52 MHz - 3'b010: 52.1 - 78 MHz - 3'b011: 78.1 - 104 MHz - 3'b100: 104.1 - 130 MHz - 3'b101: 130.1 - 156 MHz - 3'b110: 156.1 - 182 MHz - 3'b111: 182.1 - 200 MHz This field should be set to appropriate values based on your reference clock frequency.
2	0h RW	REF_CLK_DIV2 DWC_XPCS (REF_CLK_DIV2): Reference Clock divide by 2 If this bit is set, reference clock provided to PHY gets divided by 2 internally in the PHY.
1	0h RW	REF_USE_PAD DWC_XPCS (REF_USE_PAD): Use Pad Clk as Reference Clock If this bit is set, PHY selects the clock connected to ref_pad_clk_p/m as its reference clock; otherwise it selects the clock connected to ref_alt_clk_p/m.
0	1h RW	REF_CLK_EN DWC_XPCS (REF_CLK_EN): Reference Clock Enable This bit should be set to enable reference clock to the PHY. This bit controls the xpcs_ref_clk_en_o output port. The value programmed to this bit is driven on xpcs_ref_clk_en_o when LPM (power-down) bit is programmed to 1. When the LPM bit is programmed to 0, xpcs_ref_clk_en_o remains high.

11.3.1.90 VR_MII_MP_12G_16G_25G_VCO_CAL_LD0 DWC_XCPs (VR_MII_MP_12G_16G_25G_VCO_CAL_LD0) - Offset 1F00010124h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY VCO Calibration Load 0 Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010124h	05B2h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12:0	05B2h RW	VCO_LD_VAL_0 DWC_XPCS (VCO_LD_VAL_0): Rx VCO calibration load value on lane 0 of the PHY This field is used to load internal calibration registers in the PHY to perform Rx VCO calibration on lane 0. This field drives the output port 'xpcs_rx0_vco_id_val_o[5:0]'.

11.3.1.91 VR_MII_MP_16G_25G_VCO_CAL_REF0 DWC_XCPs (VR_MII_MP_16G_25G_VCO_CAL_REF0) - Offset 1F0001012Ch

VR MII Synopsis Multi-protocol 16G/25G PHY VCO Calibration Reference Register 0

Type	Size	Offset	Default
MMIO	16 bit	1F0001012Ch	0007h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	Reserved
6:0	07h RW	VCO_REF_LD_0 DWC_XPCS (VCO_REF_LD_0): Rx VCO calibration reference load value -lane 0 This field controls the PHY's internal calibration registers used to perform Rx VCO calibration on lane 0. This field drives the output port 'xpcs_rx0_ref_id_val_o[6:0]'.

11.3.1.92 VR_MII_MP_12G_16G_25G_MISC_STS DWC_XCPs (VR_MII_MP_12G_16G_25G_MISC_STS) - Offset 1F00010130h

VR MII Synopsis Multi-protocol 12/G16G/25G PHY Miscellaneous Status Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010130h	0400h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved
12	0h RO/V	RX_ADPT_ACK DWC_XPCS (RX_ADPT_ACK): Receive Adaptation Acknowledgment from PHY. This field reflects the value of rpcs_krx_adapt_ack_i port.
11	0h RO/V	REF_CLKDET_RESULT DWC_XPCS (REF_CLKDET_RESULT): For Multi-protocol 16G/25G PHY configurations: Reference Clock Detect enable This field is driven by the input xpcs_ref_clkdet_result_i. For other configurations: Reserved
10	1h RO/V	MPLLSTS DWC_XPCS (MPLLSTS): Status of MPLLB from PHY This bit denotes the value of xpcs_mpllb_state_i input.
9	0h RO/V	MPLLA_STS DWC_XPCS (MPLLA_STS): Status of MPLLA from PHY. This bit denotes the value of xpcs_mplla_state_i input
8	0h RO/V	RTUNE_ACK DWC_XPCS (RTUNE_ACK): Acknowledgment for Resistor Tune Request This bit denotes the value of 'xgxs_rtune_ack_i' input.
7:0	00h RO/V	FOM DWC_XPCS (FOM): Figure of Merit from the PHY. This field reflects the value of rpcs_krx_fom_i port.

11.3.1.93 VR_MII_MP_12G_16G_25G_MISC_CTRL1_DWC_XCPs (VR_MII_MP_12G_16G_25G_MISC_CTRL1) - Offset 1F00010132h

VR MII Synopsis Multi-protocol 12/G16G/25G PHY Miscellaneous Control 1 Register

Type	Size	Offset	Default
MMIO	16 bit	1F00010132h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	FFFFh RW	RX_LNK_UP_TIME DWC_XPCS (RX_LNK_UP_TIME): Wait Time before PLL Re-initialization This field determines the number of 'clk_csr_i' clock cycles that can elapse before the Rx link is established (after DWC_xpcs has reached POWER_GOOD state). This field is relevant only if 'PLL_CTRL' bit of VR_MII_MP_12G_16G_25G_MISC_CTRL0 Register is programmed to 1. If the receive link is not up (or if frame lock does not happen during CL72 Training or if AN page is not received), within this specified interval, DWC_xpcs programs the PHY Rx power state to P1 and then bring it back to P0 (thus re-initializing the PHY PLL).

11.3.1.94 VR_MII_MP_12G_16G_25G_SRAM_DWC_XCPs (VR_MII_MP_12G_16G_25G_SRAM) - Offset 1F00010136h

VR MII Synopsis Multi-protocol 12G/16G/25G PHY SRAM Register. Note: This is a special register which can be read/written even before DWC_xcps completes its reset/initialization sequence.

Type	Size	Offset	Default
MMIO	16 bit	1F00010136h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved
2	0h RO/V	BTLD_BYP DWC_XPCS (BTLD_BYP): SRAM Bootload Bypass. This field drives the xpcs_sram_bootload_byp_o port. Note: This field is present only for Multi-protocol 25G/8G PHY configurations.
1	0h RW	EXT_LD_DN DWC_XPCS (EXT_LD_DN): SRAM External Loading Done. This field drives the output port 'xpcs_sram_ext_ld_done_o' of DWC_xpcs. Software should set this bit to 1, after PHY has completed its SRAM initialization and after software has completed the (optional) external loading of the SRAM attached to the PHY. The PHY completes its initialization sequence only after this register bit is set to 1. Notes: - After the software has set this bit as 1, it should remain 1 throughout normal operation. - This bit gets cleared during standard soft reset (RST) - This bit does not get cleared during vendor soft reset (VR_RST). - Whenever software asserts VR_RST, this bit should be cleared prior to that (in case, software wishes to alter the SRAM contents initialized by the PHY).
0	1h RO/V	INIT_DN DWC_XPCS (INIT_DN): SRAM Initialization Done. This register field reflects the value of the 'xpcs_sram_init_done_i' port of DWC_xpcs. Whenever PHY gets reset, the bootloader in the Raw PCS loads the code from the internal look-up table to the SRAM. After this SRAM initialization is complete, PHY asserts this signal. After the SRAM initialization is done, software can optionally change the SRAM contents using the CR port interface by addressing the SRAM address space in the register map of the PHY. During power-on-reset or whenever RST or VR_RST register bits are programmed to 1, the PHY also gets reset. Therefore, the software should first poll this register bit to become 1. Thereafter, it should set the 'EXT_LD_DN' bit to 1. Only then the PHY and the DWC_xpcs proceeds to complete its reset sequence. Note: Though default value of this register bit is given as 1, this is the value provided by the PHY after the completion of SRAM initialization.

11.3.1.95 VR_MII_MP_16G_25G_MISC_CTRL2_DWC_XCPs (VR_MII_MP_16G_25G_MISC_CTRL2) - Offset 1F00010138h

VR MII Synopsis Multi-protocol 16G/25G PHY Miscellaneous Control 2 Register.

Type	Size	Offset	Default
MMIO	16 bit	1F00010138h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved
8	0h RW	REF_CLK_DET_EN DWC_XPCS (REF_CLK_DET_EN): Reference Clock Detect enable. This field drives the output port xpcs_ref_clkdet_en_o.
7:0	01h RW	SUP_MISC DWC_XPCS (SUP_MISC): Support Miscellaneous Controls. This field drives the output port xpcs_sup_misc_o[7:0].

11.3.1.96 VR_MII_SNPS_CR_CTRL DWC_XPCS (VR_MII_SNPS_CR_CTRL) - Offset 1F00010140h

VR MII Synopsis PHY CR Control Register.

Type	Size	Offset	Default
MMIO	16 bit	1F00010140h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved
1	0h RW	WR_RDN DWC_XPCS (WR_RDN): Write or Read Indicator This bit indicates whether a read or write operation is to be performed to the Synopsys PHY registers: - 0: Read - 1: Write
0	0h RW	START_BUSY DWC_XPCS (START_BUSY): Start CR Port Access or Busy Indicator (WS,SC Type) This bit indicates if CR port access is in progress: - 0: CR port not busy - 1: CR port busy The sequence is: 1. The host sets this bit to start a read or write transfer through the CR port to the Synopsys PHY registers. 2. This bit remains set during the CR port access. 3. The DWC_xpcs clears this bit when the CR port access is complete. Dependencies: The host must read this bit as 0 before writing to any of the following registers: - VR_MII_SNPS_CTRL Register (this register) - VR_MII_SNPS_CR_ADDR Register - VR_MII_SNPS_CR_DATA Register During read, the data from the CR port interface is placed into the VR_MII_SNPS_CR_DATA Register.

11.3.1.97 VR_MII_SNPS_CR_ADDR DWC_XPCS (VR_MII_SNPS_CR_ADDR) - Offset 1F00010142h

VR MII Synopsis PHY CR Address Register.

Type	Size	Offset	Default
MMIO	16 bit	1F00010142h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	ADDRESS DWC_XPCS (ADDRESS): CR Port Address This field indicates the address of the register to be accessed through the CR port. Dependency: * The host must not change this field when Bit 0 of the VR_MII_SNPS_CR_CTRL Register is set. * This field must be written before writing to any of the following registers: - VR_MII_SNPS_CR_CTRL Register - VR_MII_SNPS_CR_ADDR Register (this register) - VR_MII_SNPS_CR_DATA Register

11.3.1.98 VR_MII_SNPS_CR_DATA DWC_XCPS (VR_MII_SNPS_CR_DATA) - Offset 1F00010144h

VR MII Synopsis PHY CR Data Register.

Type	Size	Offset	Default
MMIO	16 bit	1F00010144h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	DATA DWC_XPCS (DATA): CR Port Data This field contains the data for CR Port access. - During a write operation, the data in this register is written to the Synopsys PHY register pointed by the CR Port Address. - During a read operation, the data read from the Synopsys PHY is written to this register. The content becomes valid only when the DWC_xpcs clears Bit 0 of the VR_MII_SNPS_CR_CTRL Register. The host must not change this field when Bit 0 of VR_MII_SNPS_CR_CTRL Register is set.

11.3.1.99 VR_MII_DIG_CTRL2 DWC_XCPS (VR_MII_DIG_CTRL2) - Offset 1F000101C2h

VR MII MMD Digital Control 2 Register. This register is present only when the DWC_xcps is configured in 1000BASEX-Only PCS mode.

Type	Size	Offset	Default
MMIO	16 bit	1F000101C2h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4	0h RW	TX_POL_INV_0 DWC_XPCS (TX_POL_INV_0):

continued...

Bit Range	Default & Access	Field Name (ID): Description
		Tx Polarity Invert on Lane 0 When set to 1, this bit reverses the data polarity on the Tx differential lines of Lane 0.
3:1	0h RO	Reserved
0	0h RW	RX_POL_INV_0 DWC_XPCS (RX_POL_INV_0): Rx Polarity Invert on Lane 0 When set, the bits within this field indicate that the data received on Rx serial line is inverted on Lane 0. This reverses the polarity on the data received from the PHY core. The value 1 indicates that Rx data on Lane 0 is inverted.

11.3.1.100 VR_MII_DIG_ERRCNT_SEL DWC_XPCS (VR_MII_DIG_ERRCNT_SEL) - Offset 1F000101C4h

VR MII MMD Digital Error Count Select Register. This register is present only when the DWC_xcps is configured in 1000BASEX-Only PCS mode.

Type	Size	Offset	Default
MMIO	16 bit	1F000101C4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved
4	0h RW	INV_EC_EN DWC_XPCS (INV_EC_EN): Invalid Code Group Error Counter Enable When this bit is set, the counting of invalid code group errors is enabled. - 0: The counting of errors is disabled - 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR_MII_ICG_ERRCNT1 Register.
3:1	0h RO	Reserved
0	0h RW	COR DWC_XPCS (COR): Clear on Read When this bit is set and the host reads any error counter, that counter is cleared after the read cycle. - 0: Normal operation - 1: Clear any error counter that is read

11.3.2 MDIO – Adhoc PHY Sublayer Registers – PHY Address 15h

The Adhoc Registers are accessible as an IEEE Std 802.3 Clause 22 capable PHY MDIO Manageable Device (MMD). Its 5-bit PHY Address (PHYAD) is 15h. Its 32 16-bit data registers are accessible using the 5-bit PHY Register Address (REGAD).

The Adhoc Registers consist of a PHY Global Configuration Register (GCR), one captured 64-bit Always Running Timer (ART) Time Stamp, one six-byte, unique MAC Address provided by the Intel® product customer via the system Flash Device, and various status registers and configuration registers related to the PCH internal PHY sublayer circuitry and debug circuitry.

Table 25. Summary of BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1500000000h	2	GCR mgbe_mdio (GCR) - Offset 1500000000h on page 550	0826h
1500000002h	2	PMC_ART0 mgbe_mdio (PMC_ART0) - Offset 1500000002h on page 551	0000h
1500000004h	2	PMC_ART1 mgbe_mdio (PMC_ART1) - Offset 1500000004h on page 551	0000h
1500000006h	2	PMC_ART2 mgbe_mdio (PMC_ART2) - Offset 1500000006h on page 552	0000h
1500000008h	2	PMC_ART3 mgbe_mdio (PMC_ART3) - Offset 1500000008h on page 552	0000h
150000000Ah	2	GPSR0 mgbe_mdio (GPSR0) - Offset 150000000Ah on page 552	0000h
150000000Ch	2	GPSR1 mgbe_mdio (GPSR1) - Offset 150000000Ch on page 553	0000h
150000000Eh	2	GPSR2 mgbe_mdio (GPSR2) - Offset 150000000Eh on page 553	0000h
15000000010h	2	GPSR3 mgbe_mdio (GPSR3) - Offset 15000000010h on page 553	0000h
15000000012h	2	GPSR4 mgbe_mdio (GPSR4) - Offset 15000000012h on page 554	0000h
15000000014h	2	GPSR5 mgbe_mdio (GPSR5) - Offset 15000000014h on page 554	0000h
15000000016h	2	GPCR0 mgbe_mdio (GPCR0) - Offset 15000000016h on page 554	0000h
15000000018h	2	GPCR1 mgbe_mdio (GPCR1) - Offset 15000000018h on page 555	0000h
1500000001Ah	2	GPCR2 mgbe_mdio (GPCR2) - Offset 1500000001Ah on page 555	0000h
1500000001Ch	2	GPCR3 mgbe_mdio (GPCR3) - Offset 1500000001Ch on page 555	0000h
1500000001Eh	2	GPCR4 mgbe_mdio (GPCR4) - Offset 1500000001Eh on page 556	0000h
15000000020h	2	GPCR5 mgbe_mdio (GPCR5) - Offset 15000000020h on page 556	0000h
15000000022h	2	GPCR6 mgbe_mdio (GPCR6) - Offset 15000000022h on page 556	0000h
15000000024h	2	GPCR7 mgbe_mdio (GPCR7) - Offset 15000000024h on page 557	0000h
15000000026h	2	MACADDR0 mgbe_mdio (MACADDR0) - Offset 15000000026h on page 557	0000h
15000000028h	2	MACADDR1 mgbe_mdio (MACADDR1) - Offset 15000000028h on page 557	0000h

continued...

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0028h			
150000002Ah	2	MACADDR2 mgbe_mdio (MACADDR2) - Offset 150000002Ah on page 558	0000h
150000002Ch	2	MGBE_HH_STATUS mgbe_mdio (MGBE_HH_STATUS) - Offset 150000002Ch on page 558	0000h
150000002Eh	2	MGBE_DLLSR mgbe_mdio (MGBE_STATUS1) - Offset 150000002Eh on page 559	0000h
1500000030h	2	MGBE_STATUS2 mgbe_mdio (MGBE_STATUS2) - Offset 1500000030h on page 559	0000h
1500000032h	2	MGBE_STATUS3 mgbe_mdio (MGBE_STATUS3) - Offset 1500000032h on page 560	0000h
1500000034h	2	MGBE_DLLCR1 mgbe_mdio (MGBE_CONFIG1) - Offset 1500000034h on page 560	0000h
1500000036h	2	MGBE_DLLCR2 mgbe_mdio (MGBE_CONFIG2) - Offset 1500000036h on page 560	0000h
1500000038h	2	MGBE_CONFIG3 mgbe_mdio (MGBE_CONFIG3) - Offset 1500000038h on page 561	0000h
150000003Ah	2	MGBE_CONFIG4 mgbe_mdio (MGBE_CONFIG4) - Offset 150000003Ah on page 561	0000h
150000003Ch	2	MGBE_CONFIG5 (MGBE_CONFIG5) - Offset 150000003Ch on page 562	0000h
150000003Eh	2	MGBE_CONFIG6 mgbe_mdio (MGBE_CONFIG6) - Offset 150000003Eh on page 562	0000h

11.3.2.1 GCR mgbe_mdio (GCR) - Offset 1500000000h

Global Control Register

Type	Size	Offset	Default
MMIO	16 bit	1500000000h	0826h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	USER_FLD1 mgBE_mdio (USER_FLD1): Spare bits in global config register for future use
11:8	8h RW	ART_SKEW mgBE_mdio (ART_SKEW): ART timer capture skew. The default is 8 cycles for 19.2MHz ART clock
7	0h RW	USER_FLD mgBE_mdio (USER_FLD): Spare bits for global config for future use
6	0h	PHY2MAC_INTR_POL mgBE_mdio (PHY2MAC_INTR_POL):

continued...

Bit Range	Default & Access	Field Name (ID): Description
	RW	Controls the polarity of the phy2mac_intr_i signal coming from GPIO before it is routed to MAC 0 -> non-inverted, active-high
5	1h RW	SOFT_RESETB mgBE_mdio (SOFT_RESETB): Chicken bit to disable reset of MAC and PCS during FLR flow. By default this is enabled.
4	0h RW	PHYIF_STRAPOVR mgBE_mdio (PHYIF_STRAPOVR): PHY interface strap override. 0 -> Override is disabled 1 -> Override is enabled
3	0h RW	PHYIF_MODE mgBE_mdio (PHYIF_MODE): Phy interface mode PHY interface mode. These bits are effective only if phyif_strapovr bit is set 0 -> RGMII Mode 1 -> SGMII mode
2:1	3h RW	LINK_MODE mgBE_mdio (LINK_MODE): mgbe Link speed selection 11 -> 2.5Gbps (this is applicable only in SGMII mode) 10 -> 1Gbps 01 -> 100Mbps 00 -> 10Mbps
0	0h RW	AUTONEG_DISABLE mgBE_mdio (AUTONEG_DISABLE): Disable Auto negotiation. When this bit is enabled the link speed is determined by the 'link_mode' bits

11.3.2.2 PMC_ART0 mgbe_mdio (PMC_ART0) - Offset 1500000002h

PMC ART Time Capture Register 0

Type	Size	Offset	Default
MMIO	16 bit	1500000002h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	PMC_ART0_FLD mgBE_mdio (PMC_ART0_FLD): Reads PMC_ART [15:0] timer value

11.3.2.3 PMC_ART1 mgbe_mdio (PMC_ART1) - Offset 1500000004h

Reads PMC_ART [31:16] timer value

Type	Size	Offset	Default
MMIO	16 bit	1500000004h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	PMC_ART1_FLD mgBE_mdio (PMC_ART1_FLD): Reads PMC_ART [31:16] timer value

11.3.2.4 PMC_ART2 mgbe_mdio (PMC_ART2) - Offset 1500000006h

PMC ART Time Capture Register 2

Type	Size	Offset	Default
MMIO	16 bit	1500000006h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	PMC_ART2_FLD mgBE_mdio (PMC_ART2_FLD): Reads PMC_ART [47:32] timer value

11.3.2.5 PMC_ART3 mgbe_mdio (PMC_ART3) - Offset 1500000008h

PMC ART Time Capture Register 3

Type	Size	Offset	Default
MMIO	16 bit	1500000008h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	PMC_ART3_FLD mgBE_mdio (PMC_ART3_FLD): Reads PMC_ART [63:48] timer value

11.3.2.6 GPSR0 mgbe_mdio (GPSR0) - Offset 150000000Ah

General Purpose

Type	Size	Offset	Default
MMIO	16 bit	150000000Ah	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	GPSR0_FLD mgBE_mdio (GPSR0_FLD): General Purpose Status Register1 [15:0]. This register returns the value of input signal status_reg_1[15:0].

11.3.2.7 GPSR1 mgbe_mdio (GPSR1) - Offset 150000000Ch

General Purpose

Type	Size	Offset	Default
MMIO	16 bit	150000000Ch	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	GPSR1_FLD mgBE_mdio (GPSR1_FLD): General Purpose Status Register 1 [31:16]. This register returns the value of input signal status_reg_1[31:16].

11.3.2.8 GPSR2 mgbe_mdio (GPSR2) - Offset 150000000Eh

General Purpose

Type	Size	Offset	Default
MMIO	16 bit	150000000Eh	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	GPSR2_FLD mgBE_mdio (GPSR2_FLD): General Purpose Status Register2 [15:0]. This register returns the value of input signal status_reg_2[15:0].

11.3.2.9 GPSR3 mgbe_mdio (GPSR3) - Offset 1500000010h

General Purpose

Type	Size	Offset	Default
MMIO	16 bit	1500000010h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	GPSR3_FLD mgBE_mdio (GPSR3_FLD): General Purpose Status Register2 [31:16], This register returns the value of input signal status_reg_2[31:16].

11.3.2.10 GPSR4 mgbe_mdio (GPSR4) - Offset 1500000012h

General Purpose

Type	Size	Offset	Default
MMIO	16 bit	1500000012h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	GPSR4_FLD mgBE_mdio (GPSR4_FLD): General Purpose Status Register3 [15:0]. This register returns the value of input signal status_reg_3[15:0].

11.3.2.11 GPSR5 mgbe_mdio (GPSR5) - Offset 1500000014h

General Purpose

Type	Size	Offset	Default
MMIO	16 bit	1500000014h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	GPSR5_FLD mgBE_mdio (GPSR5_FLD): General Purpose Status Register3 [31:16]. This register returns the value of input signal status_reg_3[31:16].

11.3.2.12 GPCRO mgbe_mdio (GPCRO) - Offset 1500000016h

General Purpose Configuration Register 0

Type	Size	Offset	Default
MMIO	16 bit	1500000016h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR0_FLD mgBE_mdio (GPCR0_FLD): General Purpose Config Register1 [15:0]

11.3.2.13 GPCR1 mgbe_mdio (GPCR1) - Offset 1500000018h

General Purpose Configuration Register 1

Type	Size	Offset	Default
MMIO	16 bit	1500000018h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR1_FLD mgBE_mdio (GPCR1_FLD): General Purpose Config Register 1 [31:16]

11.3.2.14 GPCR2 mgbe_mdio (GPCR2) - Offset 150000001Ah

General Purpose Configuration Register 2

Type	Size	Offset	Default
MMIO	16 bit	150000001Ah	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR2_FLD mgBE_mdio (GPCR2_FLD): General Purpose Config Register2 [15:0]

11.3.2.15 GPCR3 mgbe_mdio (GPCR3) - Offset 150000001Ch

General Purpose Configuration Register 3

Type	Size	Offset	Default
MMIO	16 bit	150000001Ch	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR3_FLD mgBE_mdio (GPCR3_FLD): General Purpose Config Register 2 [31:16]

11.3.2.16 GPCR4 mgbe_mdio (GPCR4) - Offset 150000001Eh

General Purpose Configuration Register 4

Type	Size	Offset	Default
MMIO	16 bit	150000001Eh	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR4_FLD mgBE_mdio (GPCR4_FLD): General Purpose Config Register3 [15:0]

11.3.2.17 GPCR5 mgbe_mdio (GPCR5) - Offset 1500000020h

General Purpose Configuration Register 5

Type	Size	Offset	Default
MMIO	16 bit	1500000020h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR5_FLD mgBE_mdio (GPCR5_FLD): General Purpose Config Register3 [31:16]

11.3.2.18 GPCR6 mgbe_mdio (GPCR6) - Offset 1500000022h

General Purpose Configuration Register 6

Type	Size	Offset	Default
MMIO	16 bit	1500000022h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR6_FLD mgBE_mdio (GPCR6_FLD): General Purpose Config Register4 [15:0]

11.3.2.19 GPCR7 mgbe_mdio (GPCR7) - Offset 1500000024h

General Purpose Configuration Register 7

Type	Size	Offset	Default
MMIO	16 bit	1500000024h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	GPCR7_FLD mgBE_mdio (GPCR7_FLD): General Purpose Config Register4 [31:16]

11.3.2.20 MACADDR0 mgbe_mdio (MACADDR0) - Offset 1500000026h

MAC Address Strap Value 0

Type	Size	Offset	Default
MMIO	16 bit	1500000026h	0000h

Register Level Access:

BIOS Access		SMM Access	OS Access
None		None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MAC_ADDR_STRAP0_FLD mgBE_mdio (MAC_ADDR_STRAP0_FLD): MAC Address Strap Values [15:0] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition

11.3.2.21 MACADDR1 mgbe_mdio (MACADDR1) - Offset 1500000028h

MAC Address Strap Value 1

Type	Size	Offset	Default
MMIO	16 bit	1500000028h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MAC_ADDR_STRAP1_FLD mgBE_mdio (MAC_ADDR_STRAP1_FLD): MAC Address Strap Values [31:16] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition

11.3.2.22 MACADDR2 mgbe_mdio (MACADDR2) - Offset 150000002Ah

MAC Address Strap Value 2

Type	Size	Offset	Default
MMIO	16 bit	150000002Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	MAC_ADDR_STRAP2_FLD mgBE_mdio (MAC_ADDR_STRAP2_FLD): MAC Address Strap Values [47:32] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition

11.3.2.23 MGBE_HH_STATUS mgbe_mdio (MGBE_HH_STATUS) - Offset 150000002Ch

Hammock Harbour Status

Type	Size	Offset	Default
MMIO	16 bit	150000002Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:4	000h RW	MGBE_RSVD_FLD mgBE_mdio (MGBE_RSVD_FLD): Reserved
3	0h RW	MGBE_SBD_SFTY_UE mgBE_mdio (MGBE_SBD_SFTY_UE): MAC Safety Uncorrectable error status: This bit is set on mac_sbd_ue_intr and cleared by software

continued...

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	MGBE_SBD_SFTY_CE mgBE_mdio (MGBE_SBD_SFTY_CE): MAC Safety Correctable error status: This bit is set on mac_sbd_ce_intr and cleared by software
1	0h RW	MGBE_TSW_ERR mgBE_mdio (MGBE_TSW_ERR): Timestamp error status: Iosf2axi_hh_tsw_status output from bridge latched on avail
0	0h RW	MGBE_SNAPSHOT_DONE mgBE_mdio (MGBE_SNAPSHOT_DONE): Snapshot done bit: Set when mgbe received LocalSync for tsw sync timestamp from iosf2axibr (opcode = 51) Cleared when new request gpo1 is initiated.

11.3.2.24 MGBE_DLLSR mgbe_mdio (MGBE_STATUS1) - Offset 150000002Eh

Reserved

Type	Size	Offset	Default
MMIO	16 bit	150000002Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	Reserved
14:8	0h RO	Reserved
7:4	0h RO/V	Reserved
3:0	0h RO/V	Reserved

11.3.2.25 MGBE_STATUS2 mgbe_mdio (MGBE_STATUS2) - Offset 1500000030h

Reserved

Type	Size	Offset	Default
MMIO	16 bit	1500000030h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	Reserved

11.3.2.26 MGBE_STATUS3 mgbe_mdio (MGBE_STATUS3) - Offset 1500000032h

Reserved

NOTE

Bit definitions are the same as MGBE_STATUS2, Offset 1500000030h

11.3.2.27 MGBE_DLLCR1 mgbe_mdio (MGBE_CONFIG1) - Offset 1500000034h

Reserved

Type	Size	Offset	Default
MMIO	16 bit	1500000034h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	Reserved
14	0h RW	Reserved
13	0h RW	Reserved
12	0h RW	Reserved
11	0h RO	Reserved
10:8	0h RW	Reserved
7:4	0h RW	Reserved
3:0	0h RW	Reserved

11.3.2.28 MGBE_DLLCR2 mgbe_mdio (MGBE_CONFIG2) - Offset 1500000036h

Reserved

Type	Size	Offset	Default
MMIO	16 bit	1500000036h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	Reserved
13:8	00h RW	Reserved
7:6	0h RO	Reserved
5:0	00h RW	Reserved

11.3.2.29 MGBE CONFIG3 mgbe_mdio (MGBE_CONFIG3) - Offset 1500000038h

MGBE Config Register 3

Type	Size	Offset	Default
MMIO	16 bit	1500000038h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	Reserved
13:8	00h RW	Reserved
7:6	0h RO	Reserved
5:0	00h RW	Reserved

11.3.2.30 MGBE CONFIG4 mgbe_mdio (MGBE_CONFIG4) - Offset 150000003Ah

MGBE Config Register 4

Type	Size	Offset	Default
MMIO	16 bit	150000003Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	MGBE_CONFIG4_FLD mgBE_mdio (MGBE_CONFIG4_FLD): Reserved

11.3.2.31 MGBE CONFIG5 (MGBE_CONFIG5) - Offset 150000003Ch

MGBE Config Register 5

Type	Size	Offset	Default
MMIO	16 bit	150000003Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	MGBE_CONFIG5_FLD mgBE_mdio (MGBE_CONFIG5_FLD): Reserved

11.3.2.32 MGBE CONFIG6 mgbe_mdio (MGBE_CONFIG6) - Offset 150000003Eh

MGBE Config Register 6

Type	Size	Offset	Default
MMIO	16 bit	150000003Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	MGBE_CONFIG6_FLD mgBE_mdio (MGBE_CONFIG6_FLD): Reserved

11.3.3 MDIO – External PHY Sublayer Registers

The MDIO Controller provides the MDIO interface to PHY components that are external to the PCH component. Both Clause 22 capable and Clause 45 capable PHY components are supported. See IEEE Std 802.3-2015 for the MDIO interface and electrical specifications.

11.4 Time-Aware GPIO Registers

Offset	Size	Register name (Register Symbol)	Default Value
1210h	32-bit	Timed GPIO Control 0 (TGPIOCTL0)	00000000h
1220h	32-bit	Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0)	00000000h
1224h	32-bit	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32)	00000000h
1228h	32-bit	Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0)	00000000h
122Ch	32-bit	Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32)	00000000h

continued...

Offset	Size	Register name (Register Symbol)	Default Value
1230h	32-bit	Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0)	00000000h
1234h	32-bit	Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32)	00000000h
1238h	32-bit	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0)	00000000h
123Ch	32-bit	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32)	00000000h
1240h	32-bit	Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)	00000000h
1244h	32-bit	Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)	00000000h
1310h	32-bit	Timed GPIO Control 1 (TGPIOCTL1)	00000000h
1320h	32-bit	Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0)	00000000h
1324h	32-bit	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32)	00000000h
1328h	32-bit	Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0)	00000000h
132Ch	32-bit	Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32)	00000000h
1330h	32-bit	Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0)	00000000h
1334h	32-bit	Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32)	00000000h
1338h	32-bit	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0)	00000000h
133Ch	32-bit	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32)	00000000h
1340h	32-bit	Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)	00000000h
1344h	32-bit	Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)	00000000h