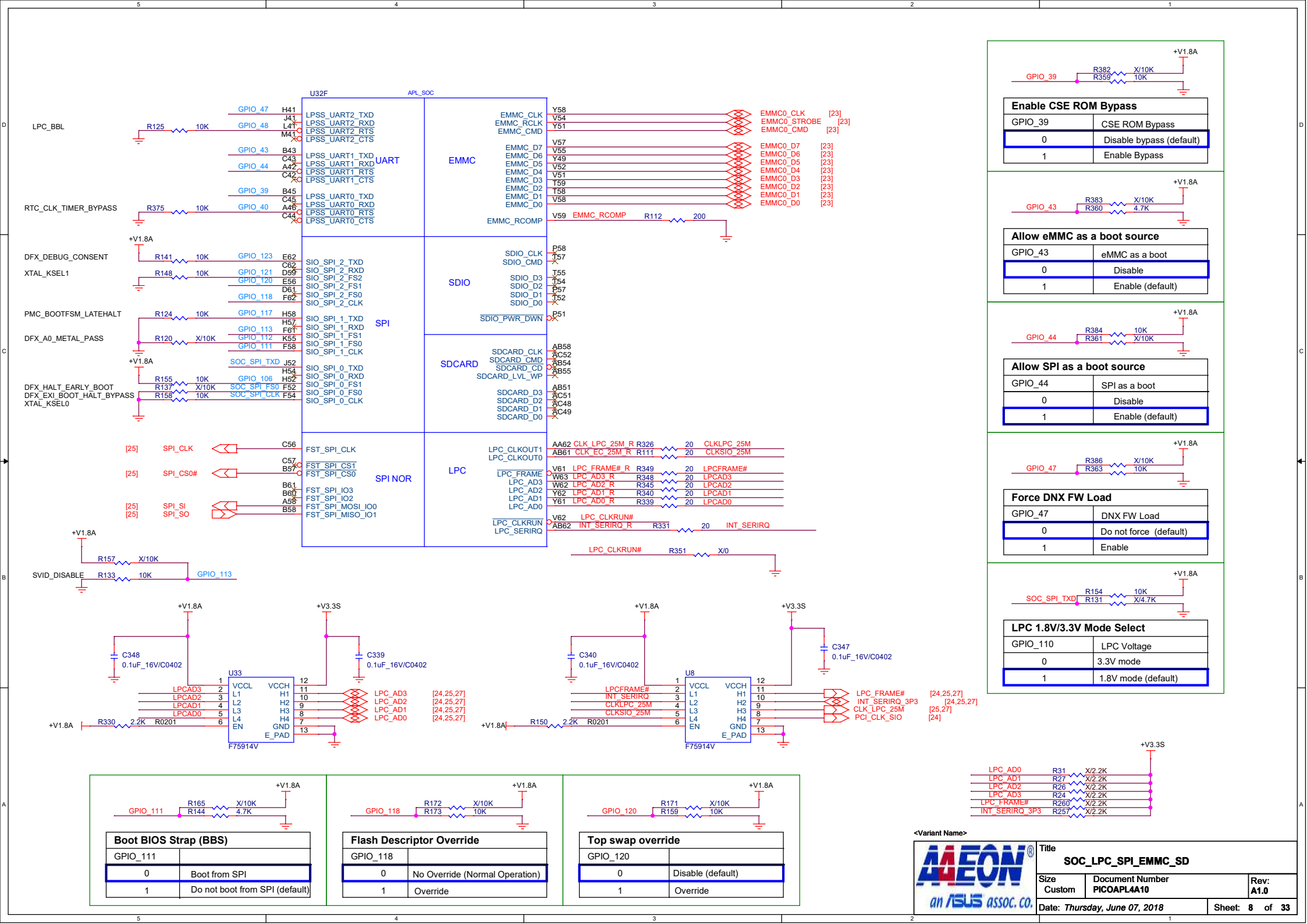
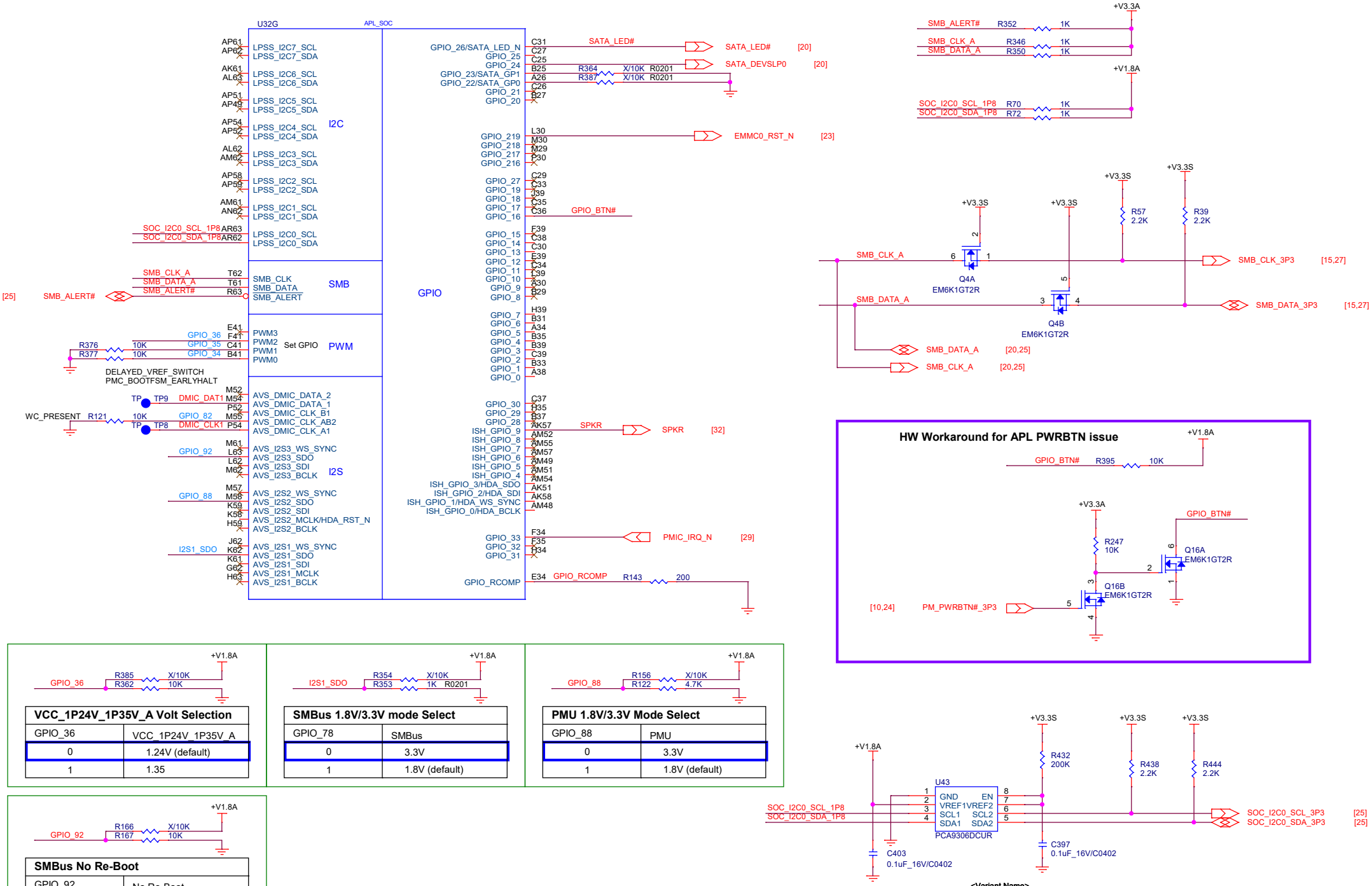

U32F
APL_SOC
UART
EMMC
SDIO
SPI
SDCARD
SPI NOR
LPC
LPC_BBL
RTC_CLK_TIMER_BYPASS
DFX_DEBUG_CONSENT
XTAL_KSEL1
PMC_BOOTFSM_LATEHALT
DFX_A0_METAL_PASS
DFX_HALT_EARLY_BOOT
DFX_EXI_BOOT_HALT_BYPASS
XTAL_KSEL0
SVID_DISABLE
LPC_CLKRUN#
U33
U8
F75914V
Enable CSE ROM Bypass
GPIO_39 | CSE ROM Bypass
0 | Disable bypass (default)
1 | Enable Bypass
Allow eMMC as a boot source
GPIO_43 | eMMC as a boot
0 | Disable
1 | Enable (default)
Allow SPI as a boot source
GPIO_44 | SPI as a boot
0 | Disable
1 | Enable (default)
Force DNX FW Load
GPIO_47 | DNX FW Load
0 | Do not force (default)
1 | Enable
LPC 1.8V/3.3V Mode Select
GPIO_110 | LPC Voltage
0 | 3.3V mode
1 | 1.8V mode (default)
Boot BIOS Strap (BBS)
GPIO_111
0 | Boot from SPI
1 | Do not boot from SPI (default)
Flash Descriptor Override
GPIO_118
0 | No Override (Normal Operation)
1 | Override
Top swap override
GPIO_120
0 | Disable (default)
1 | Override
<Variant Name>
AAEON an ASUS assoc. co.
Title
SOC_LPC_SPI_EMMC_SD
Size Custom
Document Number PICOAPL4A10
Rev: A1.0
Date: Thursday, June 07, 2018
Sheet: 8 of 33



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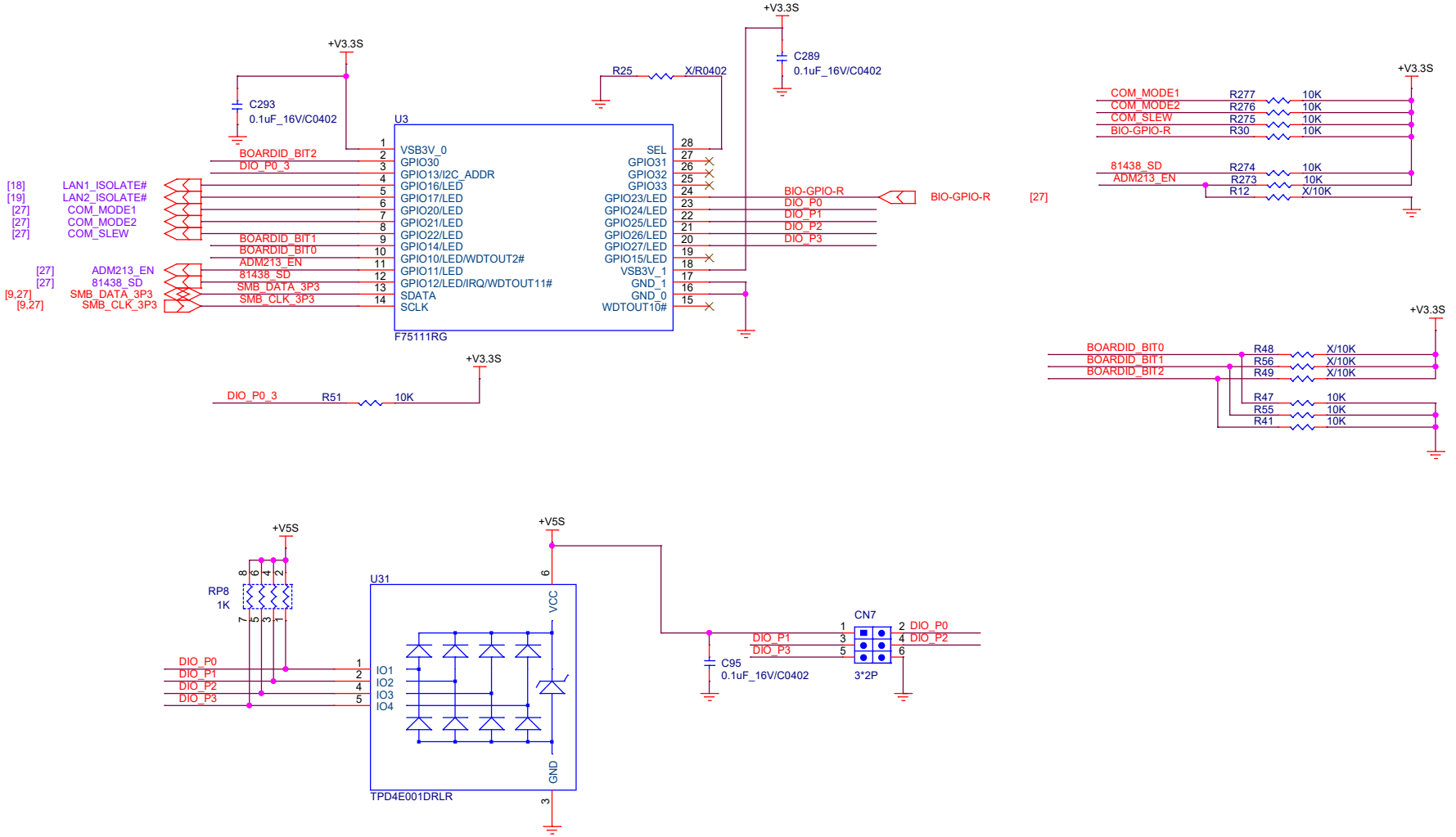
AAEON an ASUS assoc. co.	Title: SOC_SMBUS_GPIO		
	Size: Custom	Document Number: PICOAPL4A10	Rev: A1.0
	Date: Thursday, June 07, 2018	Sheet: 9 of 33	



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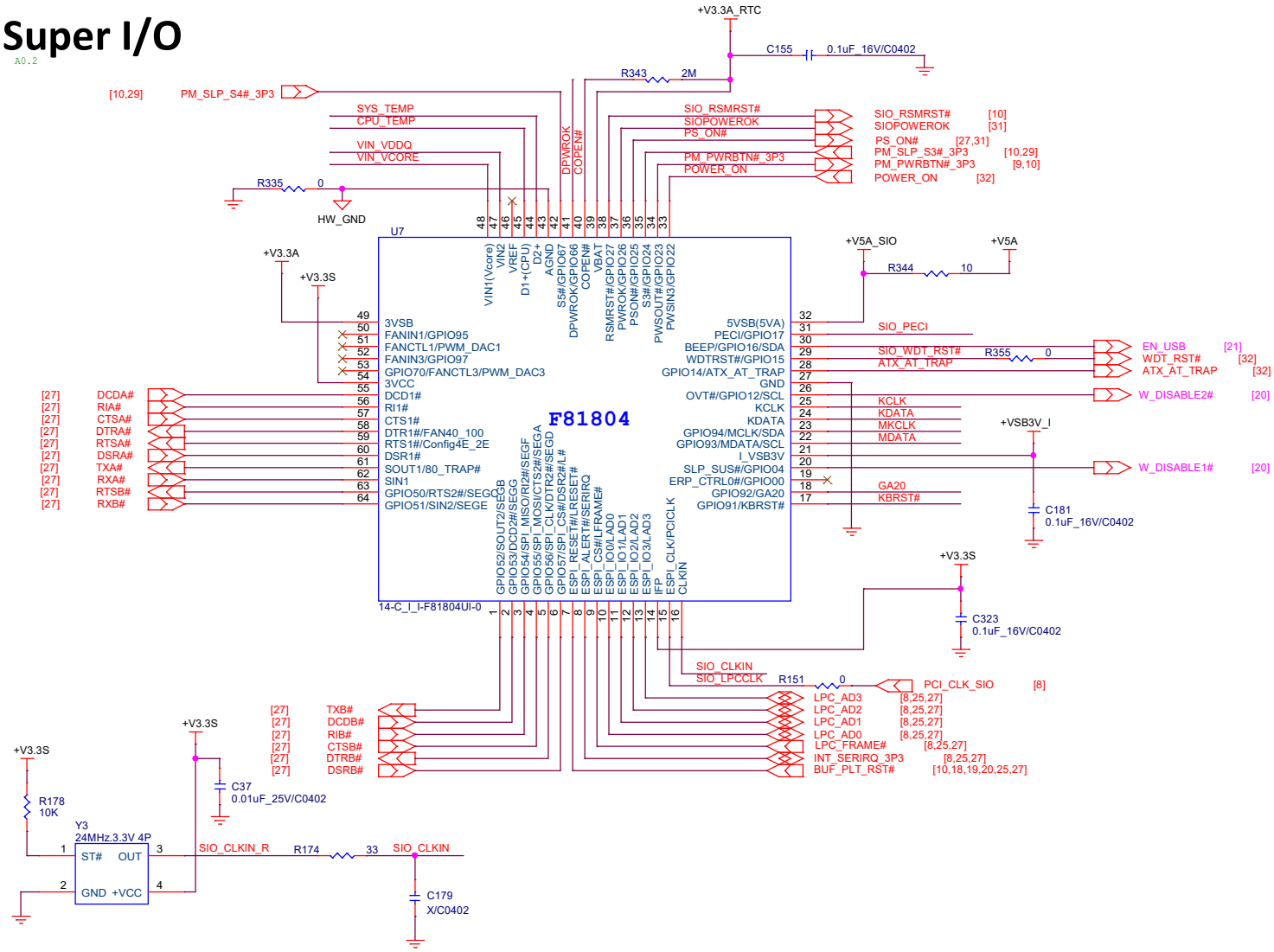
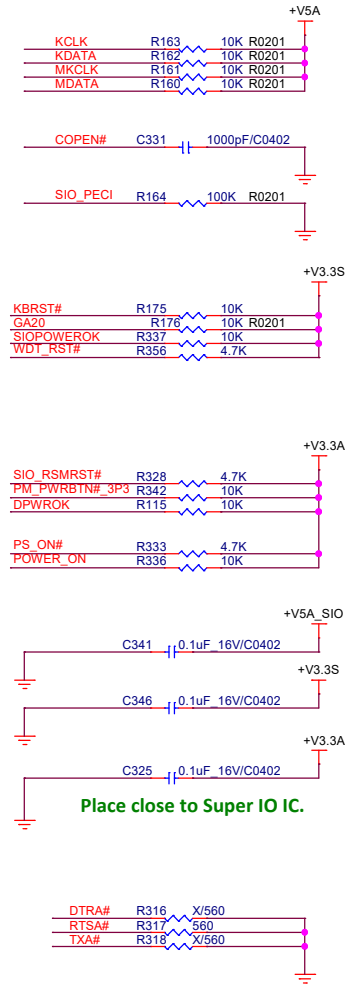
AAEON an ASUS assoc. co.	Title: F75111, DIO	
	Size: Custom	Document Number: PICOAPL4A10 — Rev: A1.0
	Date: *Thursday, June 07, 2018*	Sheet: 15 of 33

Super I/O

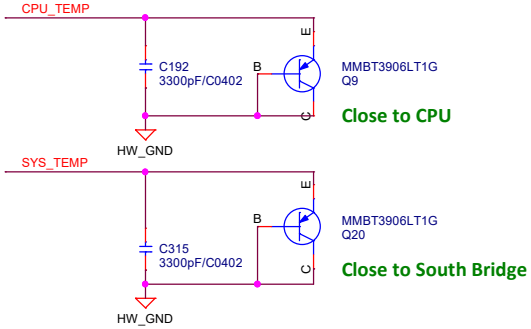


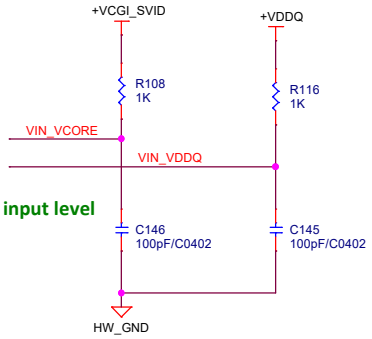


POWER TRIP

	High	Low
DTRA#	FAN 40%	FAN 100%
RTSA#	CONFIG 4E	CONFIG 2E
TXA#	80 PORT DISABLE	80 PORT ENABLE
ATX_AT_TRAP	ATX	AT

Temperature Monitor(CPU, SYS)



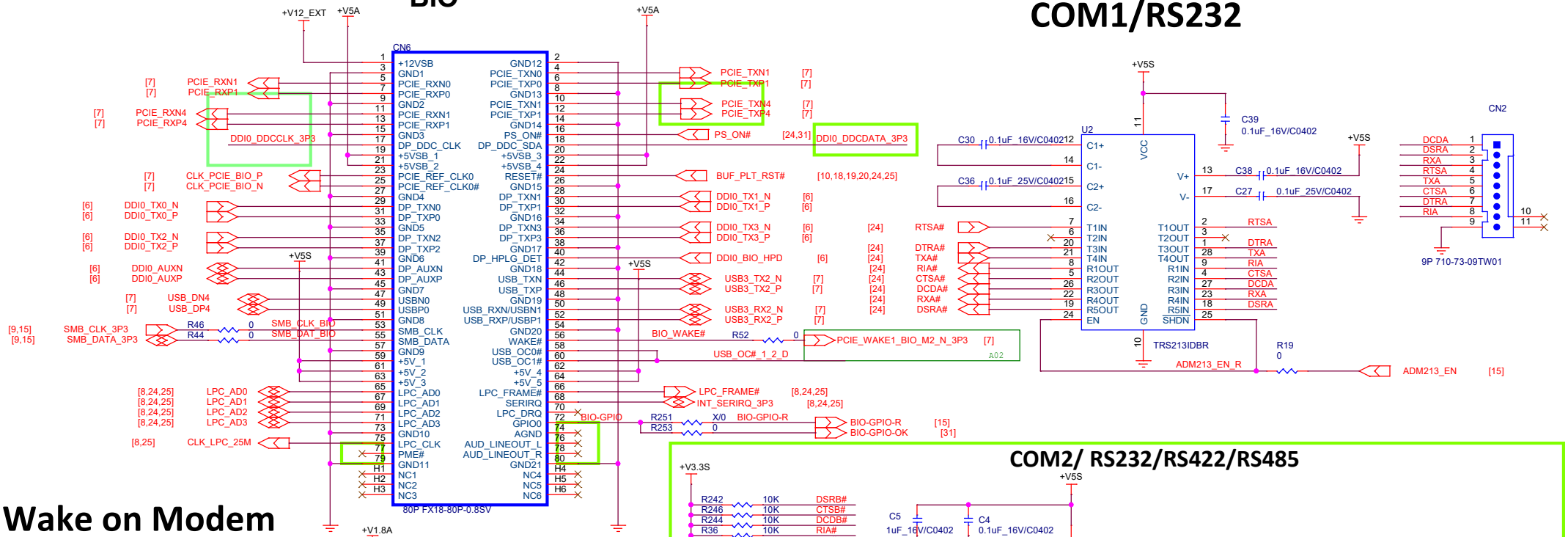


The best voltage input level is about 1V.

<Variant Name>

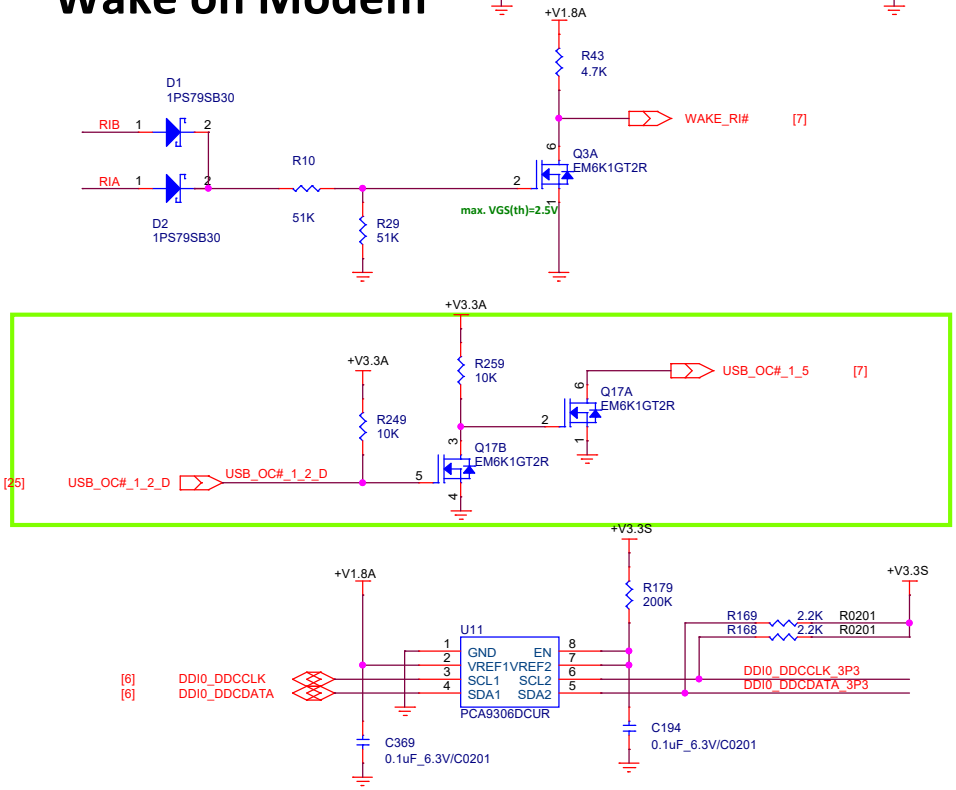
AAEON an ASUS assoc. co.	Title: Super I/O F81804	
	Size: Custom	Document Number: PICOAPL4A10 — Rev: A1.0
	Date: Thursday, June 07, 2018	Sheet: 24 of 33

BIO

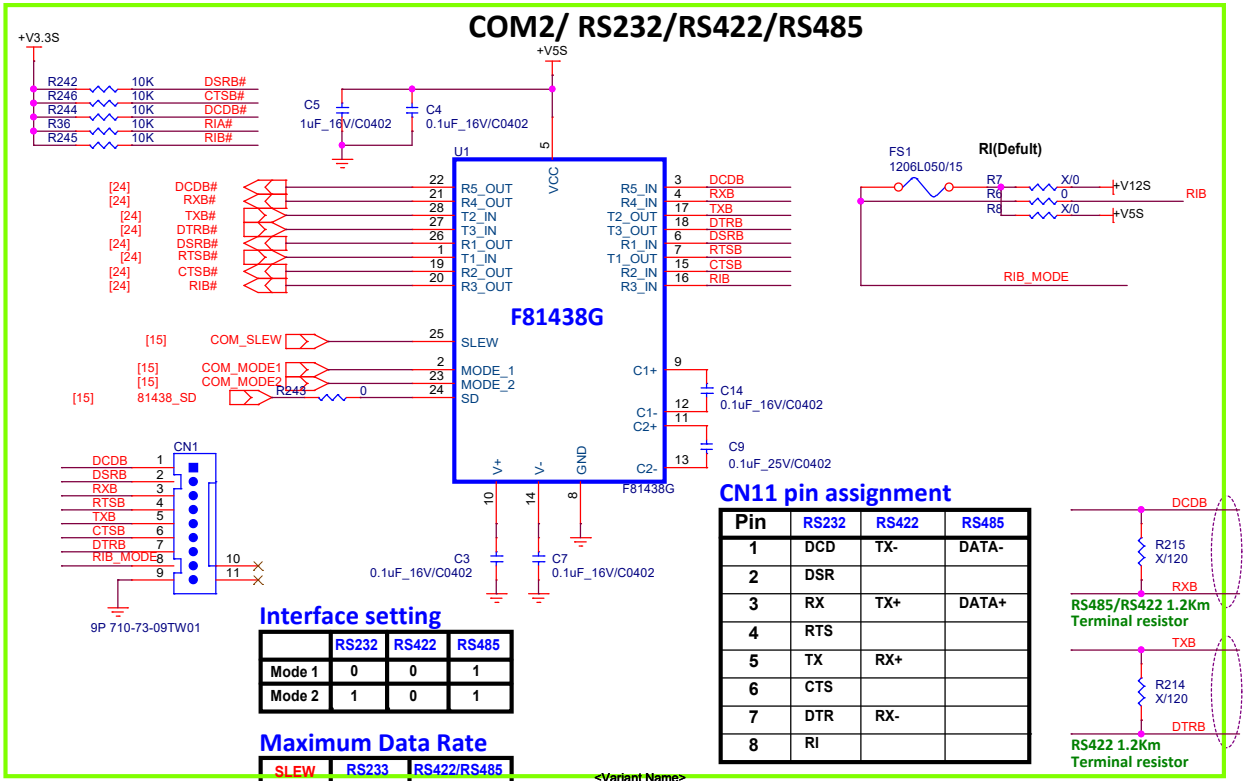


COM1/RS232

Wake on Modem



COM2/ RS232/RS422/RS485



Interface setting

	RS232	RS422	RS485
Mode 1	0	0	1
Mode 2	1	0	1

Maximum Data Rate

SLEW	RS233	RS422/RS485
1	250kbps	250kbps
0	1Mbps	10Mbps

CN11 pin assignment

Pin	RS232	RS422	RS485
1	DCD	TX-	DATA-
2	DSR		
3	RX	TX+	DATA+
4	RTS		
5	TX	RX+	
6	CTS		
7	DTR	RX-	
8	RI		

<variant_name>

AAEON an ASUS assoc. co.

Title: BIO/GPIO		
Size: Custom	Document Number: PICOAPL4A10	Rev: A1.0
Date: Thursday, June 07, 2018	Sheet: 27 of 33	