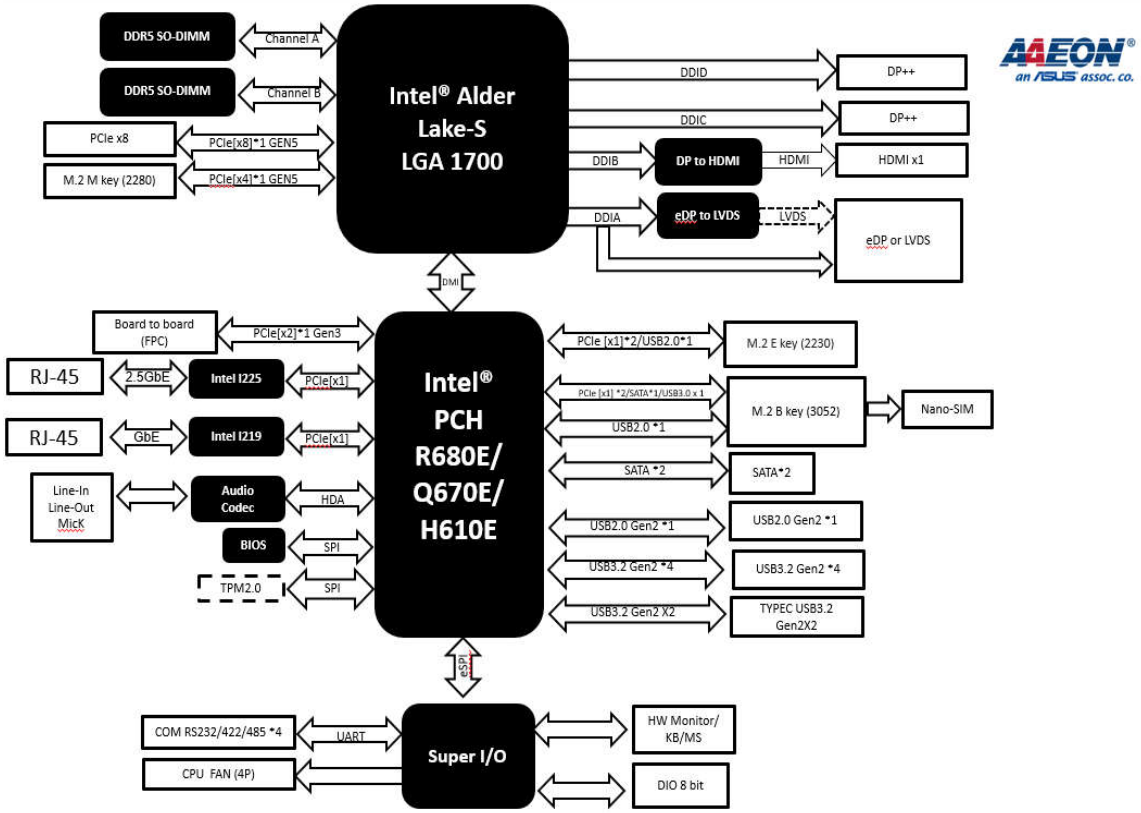
Project Name: EPIC-ADS7
Project Number:
Version: A0.2_0_0

Block diagram



Page	Index
1	Cover Sheet
2	SYSTEM SETTING
3	Power Sequence
4	Power Delivery tree
5	PROCESSOR 1_DMI/PEG
6	PROCESSOR 2_DDI/EDP
7	PROCESSOR 3_DDR5
8	PROCESSOR 4_CLK/CFG/RSVD
9	PROCESSOR 5_POWER1
10	PROCESSOR 6_POWER2
11	PROCESSOR 7-VSS
12	DDR5_SODIMMA
13	DDR5_SODIMMB
14	PCH1_CLK
15	PCH2_DMI
16	PCH3_PCIE/SATA
17	PCH4_USB3.2/USB2
18	PCH5_I2C/SMLINK/UART/SMB
19	PCH6_CNVi/GSPI/SNDW/HDA
20	PCH7_SPI/JTAG/MISC/ESPI
21	PCH8_POWER
22	PCH9_VSS
23	LAN1_INTEL i219
24	LAN2_I225LM
25	SPI_TPM
26	PCIe X 4 FPC
27	DDIC/D to DP1/2
28	HDMI2.0
29	eDP to LVDS/eDP
30	M.2(Key M)
31	M.2(Key E)
32	M.2(Key B)
33	SUPERIO_FINTEK 81966
34	BIOS/ LPC/ HW Monitor
35	COM1~COM4
36	USB3.2/ USB2.0
37	TYPE C
38	SATA/DIO/FAN
39	Audio
40	PCIE X8
41	PWR_IMVP9.1
42	PWR_+VCCCORE_Phase1/2
43	PWR_+VCCCORE_Phase3/4/5
44	PWR_+VCCGT
45	PWR_+VCCIN_AUX
46	PWR_+VREG5,+V3.3A
47	PWR_+VDDQ
48	PWR_+V0P82A
49	PWR_+V1P8A_PROC/+V1P8A_PCH
50	PWR+V1P05A_PROC/+V1P05A
51	STANDBY POWER+RSMRST
52	BOOT SEQUENCE
53	PWR_+V12S/ +V5S/ +V3P3S
54	POWER INPUT,MISC
55	Revision History

<Variant Name>

AAEON Technology INC.

Title: Cover Sheet		
Size: Custom	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 1 of 57	

PCH

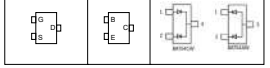
Group	GPIO Name	Power Rail	Default	GPIO Fun.	External PU/PD
A	GPP_A0	+V1P8A	PU	ESPI_IO_0	
	GPP_A1			ESPI_IO_1	
	GPP_A2			ESPI_IO_2	
	GPP_A3			ESPI_IO_3	
	GPP_A4			ESPI_CS0#	
	GPP_A5			ESPI_CLK	
	GPP_A6			ESPI_RESET#	
B	GPP_B2	+V3P3A	PU	VRALERT#	PU_10K
	GPP_B5		PU	SX_EXIT_HOLDOFF#	PU_10K
	GPP_B13		PU	PLTRST#	
	GPP_B14		PD	SPKR	
	GPP_B18		PU	PMCALERT#	PU_10K
	GPP_B23		PU	SML1ALERTB	PU_150K
C	GPP_C0	+V3P3A	PU	SMB_CLK	PU_1K
	GPP_C1			SMB_DATA	PU_1K
	GPP_C2			SMBALERT#	PU_4.7K
	GPP_C3			I2C2_SDA	PU_1K
	GPP_C4			I2C2_SCL	PU_1K
	GPP_C5			SML0ALERT#	PU_150K
	GPP_C6			I2C3_SDA	PU_47K
	GPP_C7			I2C3_SCL	PU_47K
	GPP_C16			I2C0_SDA	PU_1K
	GPP_C17			I2C0_SCL	PU_1K
	GPP_C18			I2C1_SDA	PU_1K
	GPP_C19			I2C1_SCL	PU_1K
D	GPP_D0	+V3P3A	PD	PCIE_CB_CLKREQ0#	PD_10K
	GPP_D1		PD	PCIE_CLKREQ1#	PD_10K
	GPP_D2		PD	PCIE_CLKREQ2#	PD_10K
	GPP_D4		PU	SML1_CLK	PU_1K
	GPP_D5		PD	CNV_RF_RESET#	PD_100K
	GPP_D9		PU	SML0_CLK	PU_2.2K
	GPP_D10		PU	SML0_DATA	PU_2.2K
	GPP_D11		PD	PCIE_LAN1_CLKREQ#	PD_10K
	GPP_D12		PD	PCIE_LAN2_CLKREQ#	PD_10K
	GPP_D13		PD	PCIE_CLKREQ6#	PD_10K
	GPP_D14		PD	PCIE_CLKREQ7#	PD_10K
	GPP_D15		PU	SML1_DATA	PU_1K
E	GPP_E0	+V3P3S	PU	SATAGP0	PU_10K
	GPP_E1			SATAGP1	PU_10K
	GPP_E8			SATALED#	PU_10K
	GPP_E9	+V3P3A		USB2_OC0#	PU_1K
	GPP_E10			USB2_OC1#	
	GPP_E11			USB2_OC2#	
	GPP_E12			USB2_OC3#	
F	GPP_F15	+V3P3S	PU	H_SKTOCC_N	
	GPP_F17	+V3P3A		TPM_PIRQ#	
	GPP_F19			EDP_VDD_EN	
	GPP_F20			EDP_BKLT_EN	
	GPP_F21			EDP_BKLT_CTRL	
	GPP_F22			USBC_PSON_OVERRIDE#	PU_10K
	GPP_F23			CODEC_INT#	PU_10K

G	GPP_G1	+V3P3A	PU	PLTRST_I225#	
	GPP_G2			DNX_FORCE_RELOAD	
	GPP_G5			SLP_DRAM#	
H	GPP_H0	+V3P3A	PU	GPP_H_0_SRCCLKREQB_18	PU_20K
	GPP_H1		PU	GPP_H1	PU_10K
	GPP_H2		PD	PCIE_CB_CLKREQ8#	PD_10K
	GPP_H3			PCIE_BMC_CLKREQ9#	PD_10K
	GPP_H10	+V3P3A	PU	SML2CLK	PU_1K
	GPP_H11		PU	SML2DATA	PU_1K
	GPP_H12		PD	SML2ALERT#	PU_150K
	GPP_H13		PU	SML3CLK	PU_1K
	GPP_H14		PU	SML3DATA	PU_1K
	GPP_H15		PU	SML3ALERT#	PU_100K
	GPP_H16		PU	SML4CLK	PU_1K
	GPP_H17		PU	SML4DATA	PU_1K
	GPP_H18		PD	SML4ALERT#	PU_150K
	GPP_H19		PU	ISH_I2C0_SDA	PU_1K
	GPP_H20		PU	SMI#	
	GPP_H21		PU	ISH_I2C0_SCL	PU_1K
	GPP_H22		PU	SCI#	
	GPP_H23	+V3P3S	PU	EC_KBRST#	PU_10K
I	GPP_I2	+V3P3A	PU	EXT_PWR_GATE#	PU_100K
	GPP_I3	+V3P3S		DDIB_HPD	PU_1M
	GPP_I4	+V3P3S		DDIC_HPD	PU_1M
	GPP_I5	+V3P3S		DDID_HPD	PU_1M
	GPP_I11	+V3P3A	PU	USB2_OC4#	PU_10K
	GPP_I12			USB2_OC5#	
	GPP_I13			USB2_OC6#	
	GPP_I14			USB2_OC7#	
	GPP_I18			GSPI0_MOSI	
	GPP_I22			GSPI1_MOSI	
J	GPP_J1	+V1P8A	PU	CPU_C10_GATE#	
	GPP_J2		PD	GPP_J2	
	GPP_J4	+V1P8A	PU	GPP_J4	PU_4.7K
	GPP_J8	+V1P8S		GPP_J_8_SRCCLKREQB_16	PU_20K
	GPP_J9	+V1P8S		GPP_H_0_SRCCLKREQB_18	PU_20K
K	GPP_K9	+V3P3A	PU	PCH_CORE_VID_1_VR	
	GPP_K11			GPP_K11	PU_10K
S	GPP_S0	+V3P3A	PU	SNDW_CLK1	
	GPP_S1			SNDW_DATA1	
	GPP_S2			SNDW_CLK2	
	GPP_S3			SNDW_DATA2	
	GPP_S4			SNDW3_DMIC1_CLK	
	GPP_S5			SNDW3_DMIC1_DATA	
	GPP_S6			SNDW4_DMIC0_CLK	
	GPP_S7			SNDW4_DMIC0_DATA	
R	GPP_R2	+V3P3A	PD	HDA_SDO_R	
	GPP_R9			CB_EDP_HPD	PD_100K
	GPP_R12		PU	DDIC_CTRL_CLK	
	GPP_R13			DDIC_CTRL_DATA	
	GPP_R14			DDID_CTRL_CLK	
	GPP_R15			DDID_CTRL_DATA	
	GPP_R18			DDIB_CTRL_CLK	
	GPP_R19			DDIB_CTRL_DATA	

OTHER CONFIGURE

PCB FOOTPRINT

MOSFET | BJT | DIODE

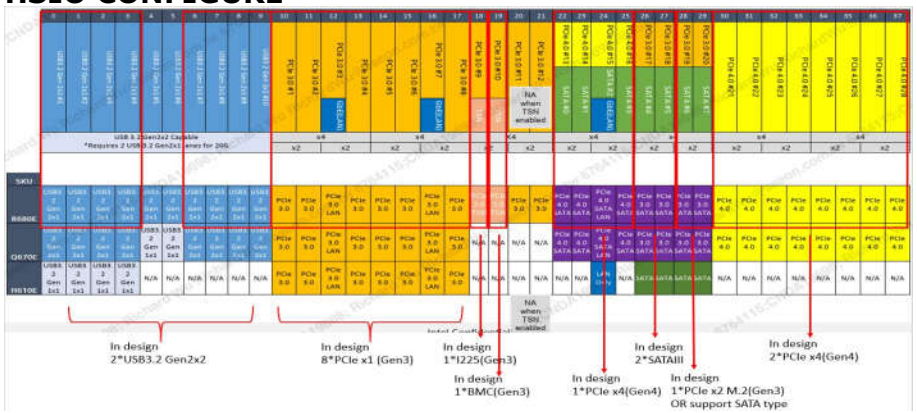


PCB STACK :

Board: FR4
Impedence: 50ohm +/-10%
Thickness: 2.0mm +-10%

- Layer 1 : Component (Top)
- Layer 2 : GND (GND1)
- Layer 3 : Signal (IN1)
- Layer 4 : Signal (IN2)
- Layer 5 : GND (GND2)
- Layer 6 : POWER (VCC)
- Layer 7 : POWER (VCC)
- Layer 8 : GND (GND3)
- Layer 9 : Signal (IN3)
- Layer 10 : Signal (IN4)
- Layer 11 : GND (GND4)
- Layer 12 : Signal (IN5)
- Layer 13 : GND (GND5)
- Layer 14 : Solder (Bottom)

HSIO CONFIGURE



<Variant Name>

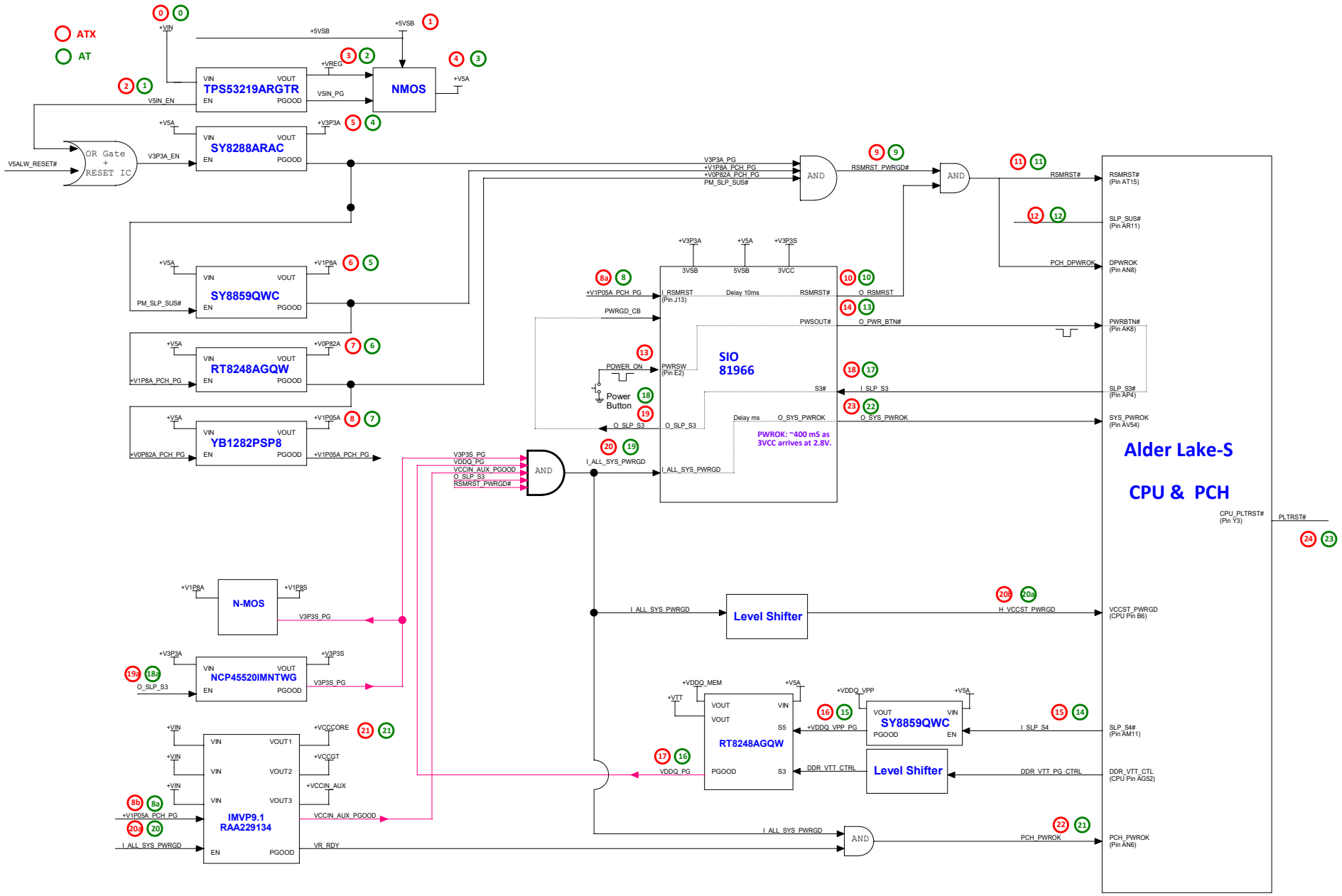
AAEON Technology INC.

Title: SYSTEM SETTING

Size | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

Date: Thursday, January 20, 2022 | Sheet 2 of 57

POWER SEQUENCE_1

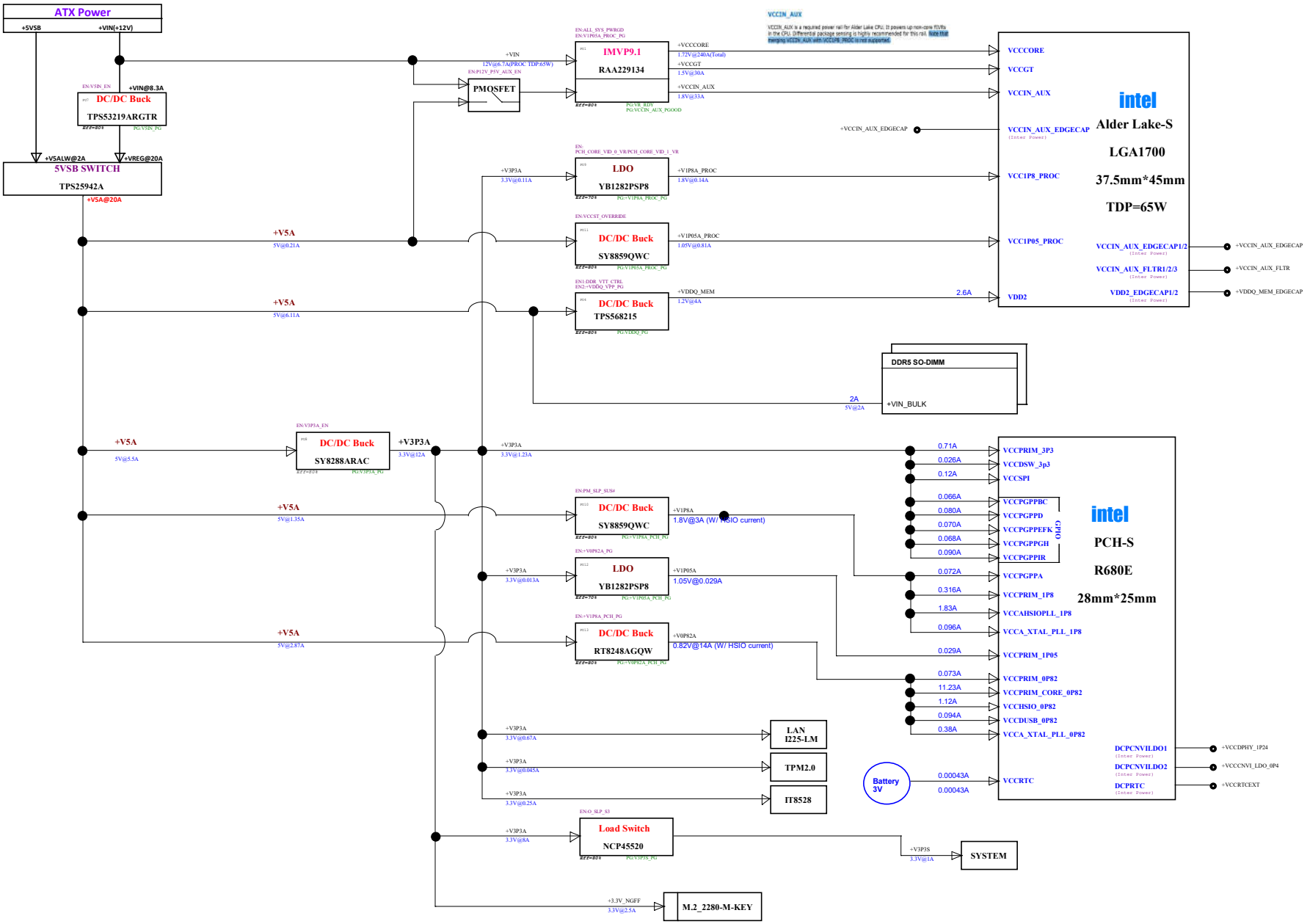


<Variant Name>

AAEON Technology INC.

Title	POWER SEQUENCE_1	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 3 of 57	

POWER DELIVERY TREE



Alder Lake-S		
VCCCORE	1.72V	240A
VCCGT	1.5V	30A
VCCIN_AUX	1.8V	40A
VCC1P8_PROC	1.8V	0.14A
VCC1P05_PROC	1.05V	0.81A
VDD2	1.2V	13A

PCH-S		
VCCPRIM_3P3	3.3V	0.142A
VCCDSW_3p3	3.3V	0.026A
VCCSPI	3.3V	0.12A
VCCPGPPBC	3.3V	0.066A
VCCPGPPD	3.3V	0.080A
VCCPGPPEFK	3.3V	0.068A
VCCPGPPGH	3.3V	0.068A
VCCPGPPIR	3.3V	0.090A
VCCPGPPA	1.8V	0.072A
VCCPRIM_1P8	1.8V	0.316A
VCCAHSIOPLL_1P8	1.8V	1.83A
VCCA_XTAL_PLL_1P8	1.8V	0.096A
VCCPRIM_1P05	1.05V	0.029A
VCCPRIM_0P82	0.82V	0.073A
VCCPRIM_CORE_0P82	0.82V	11.23A
VCCHSIO_0P82	0.82V	1.12A
VCCDUSB_0P82	0.82V	0.094A
VCCA_XTAL_PLL_0P82	0.82V	0.38A
VCCRTC	3.3V	0.00043A

DDR4 SODIMM*2		
+VDDQ_MEM	1.2V	13A
VTT	0.6V	0.4A
VPP	2.5V	2A

LAN-I225		
+V3P3A_LAN	3.3V	0.67A

LAN_XXV710-AM2		
VCC3P3	3.3V	0.45A
AVDD	1V	4.5A
VCC0P85	0.86V	6A

TPM2.0		
+V3P3A	3.3V	0.045A

SIO F81966		
+V3.3A_EC	3.3V	0.25A

ESPI to LPC		
+V3P3A_ESPI	3.3V	0.015A
+V1P8A_ESPI	1.8V	0.0013A

M.2_2280 (M-Key)		
+3.3V_NGFF	3.3V	2.5A

AAEON Technology INC.

POWER DELIVERY TREE

EPIC-ADS7

A0.2_0_0

PROCESSOR 1_DMI/PEG

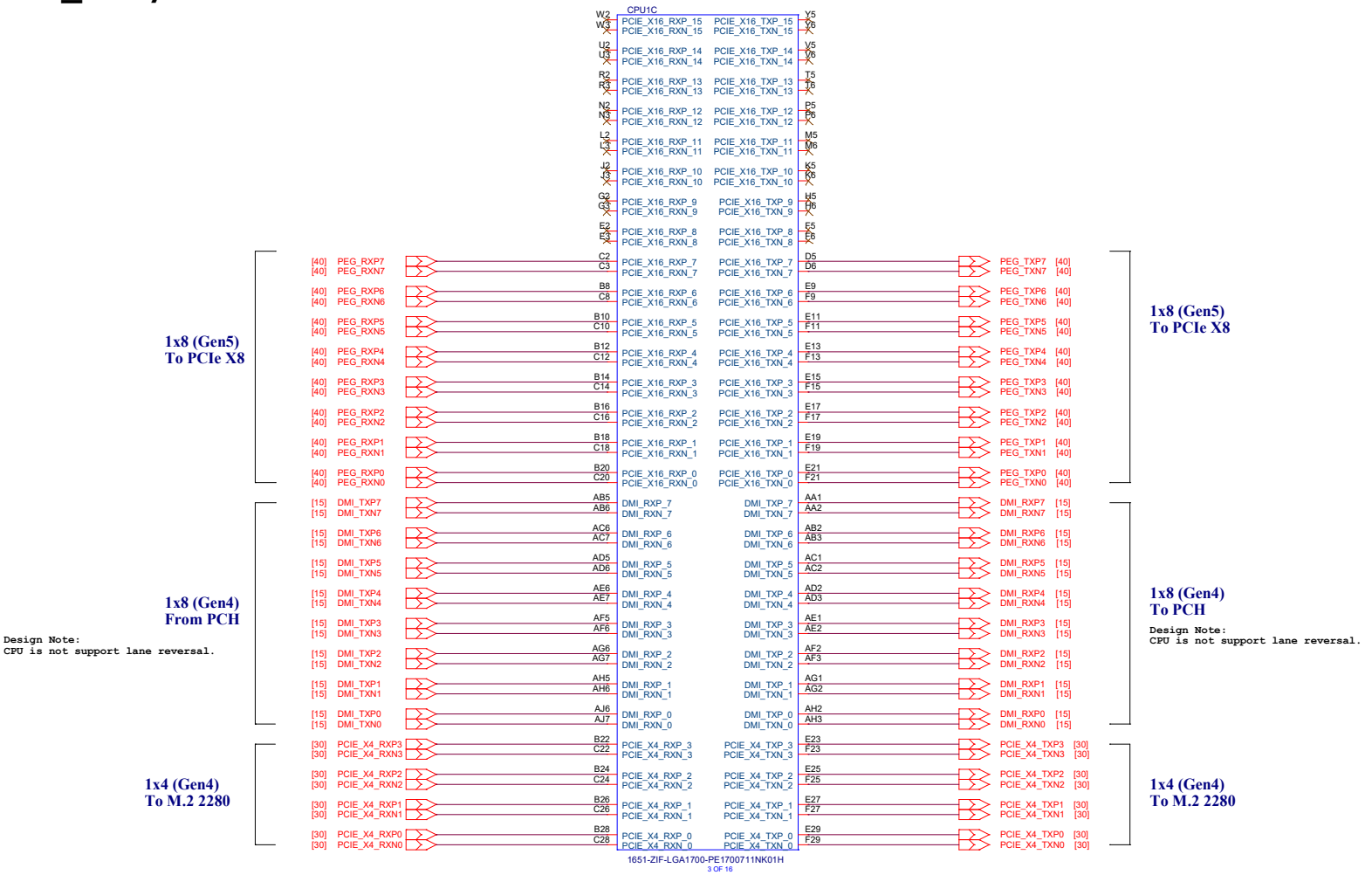


Table 51. PCI Express* 16 -lane Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width		CFG Signals			Lanes															
	0:1:0	0:1:1	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe controller						PCIe 010															
1x16	x16	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCIe controller						PCIe 010								PCIe 011							
2x8	x8	x8	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

Processor to PCH DMI Lane Connections

Link Width	Component	Lane Reversal	DMI Package Pin Lane Connections							
x8	Processor	No	0	1	2	3	4	5	6	7
	PCH	No	0	1	2	3	4	5	6	7
	Processor	No	0	1	2	3	4	5	6	7
	PCH	Yes	7	6	5	4	3	2	1	0

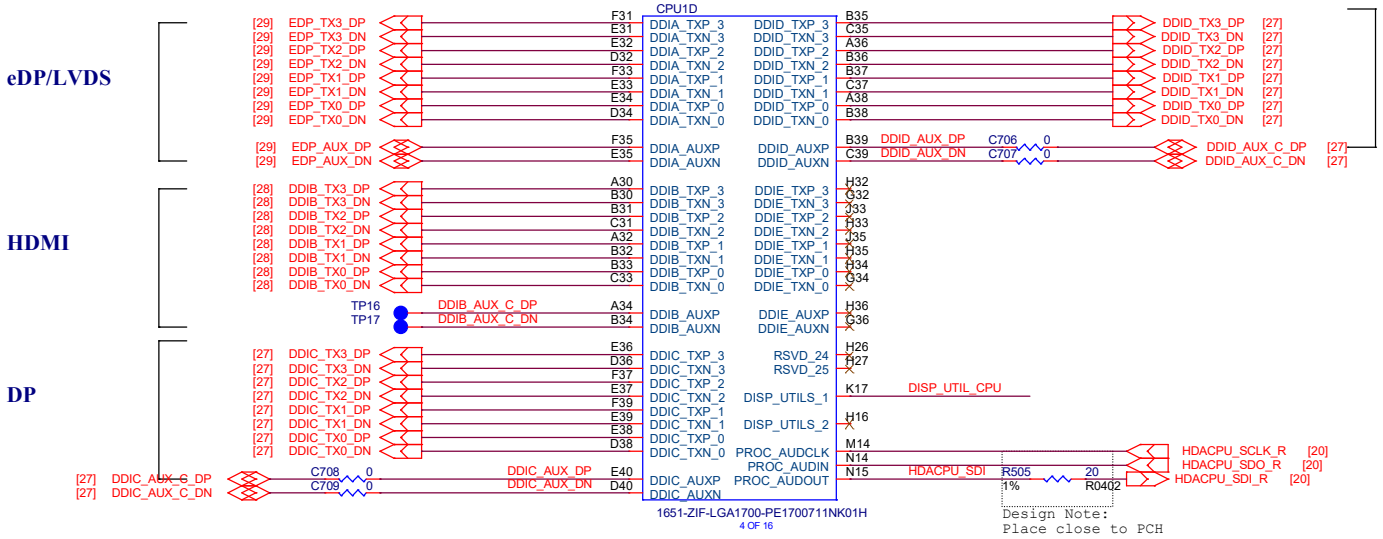
Notes:
- NC = No Connect
- PCH DMI Controller supports x8 static end-to-end Lane Reversal on its Lanes [7:0]
- Processor DMI Controller does not supports static end-to-end Lane Reversal on its Logical Lanes

<Variant Name>

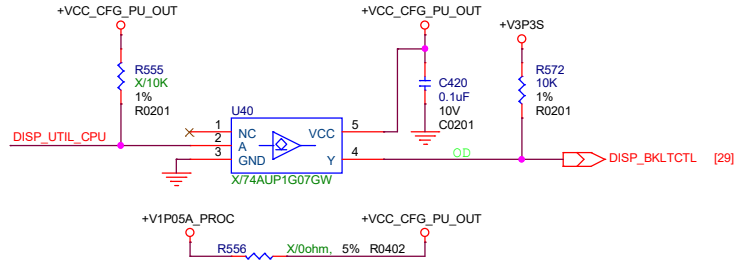
AAEON Technology INC.

Title	PROCESSOR 1_DMI/PEG	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 5 of 57	

PROCESSOR 2_DDI/EDP



RESERVED



DISP_UTILS_1 / DSI_DE_TE_1	Digital Display Interface Utility Pin. MIPI DSI Tearing effect signal

DDI Ports Availability

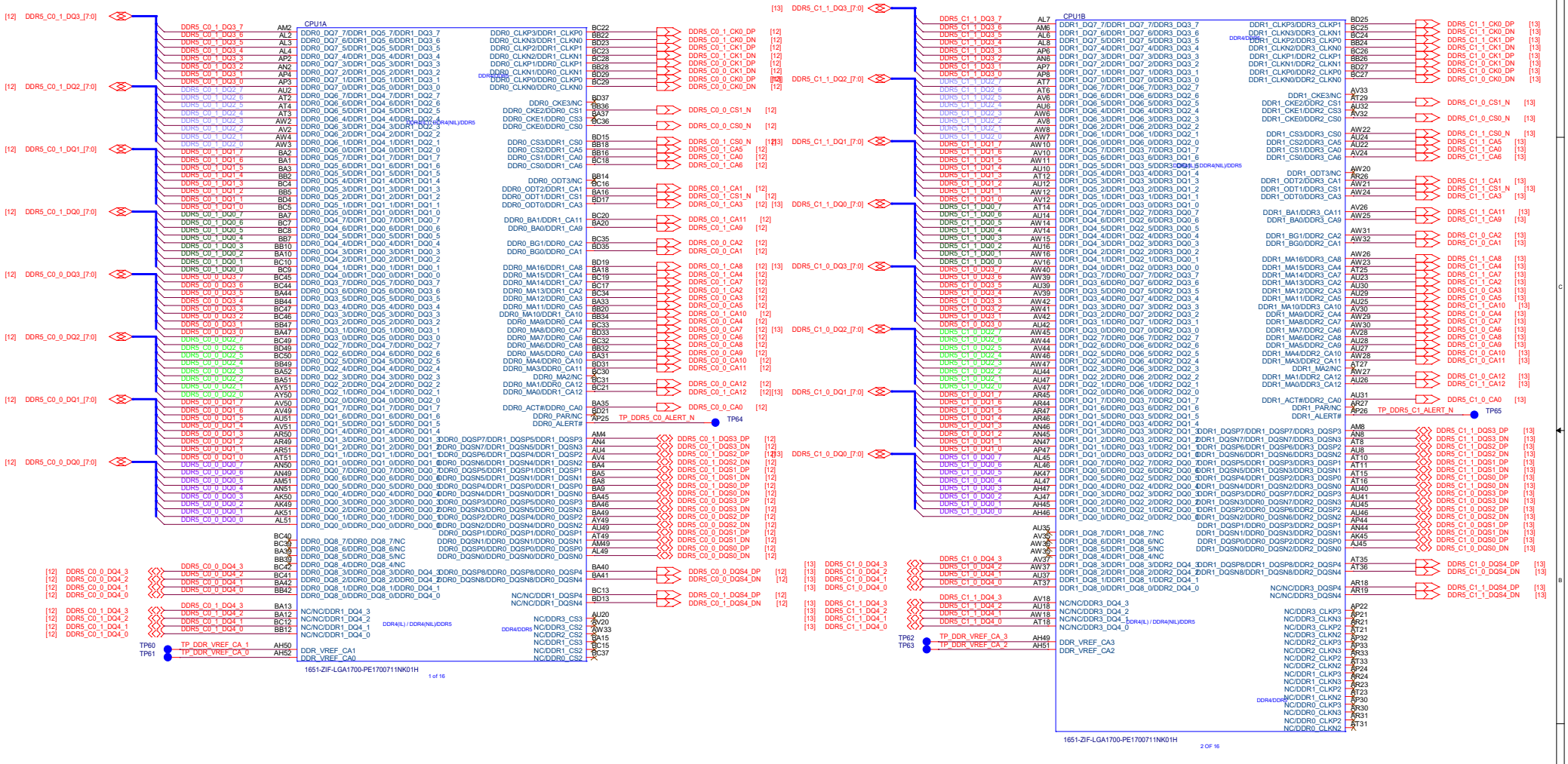
SKU	Processor Line
DDI A	eDP*/DP*/HDMI*
DDI B	DP*/HDMI*
DDI C	DP*/HDMI*
DDI D	DP*/HDMI*
DDI E	DP*/HDMI*

<Variant Name>

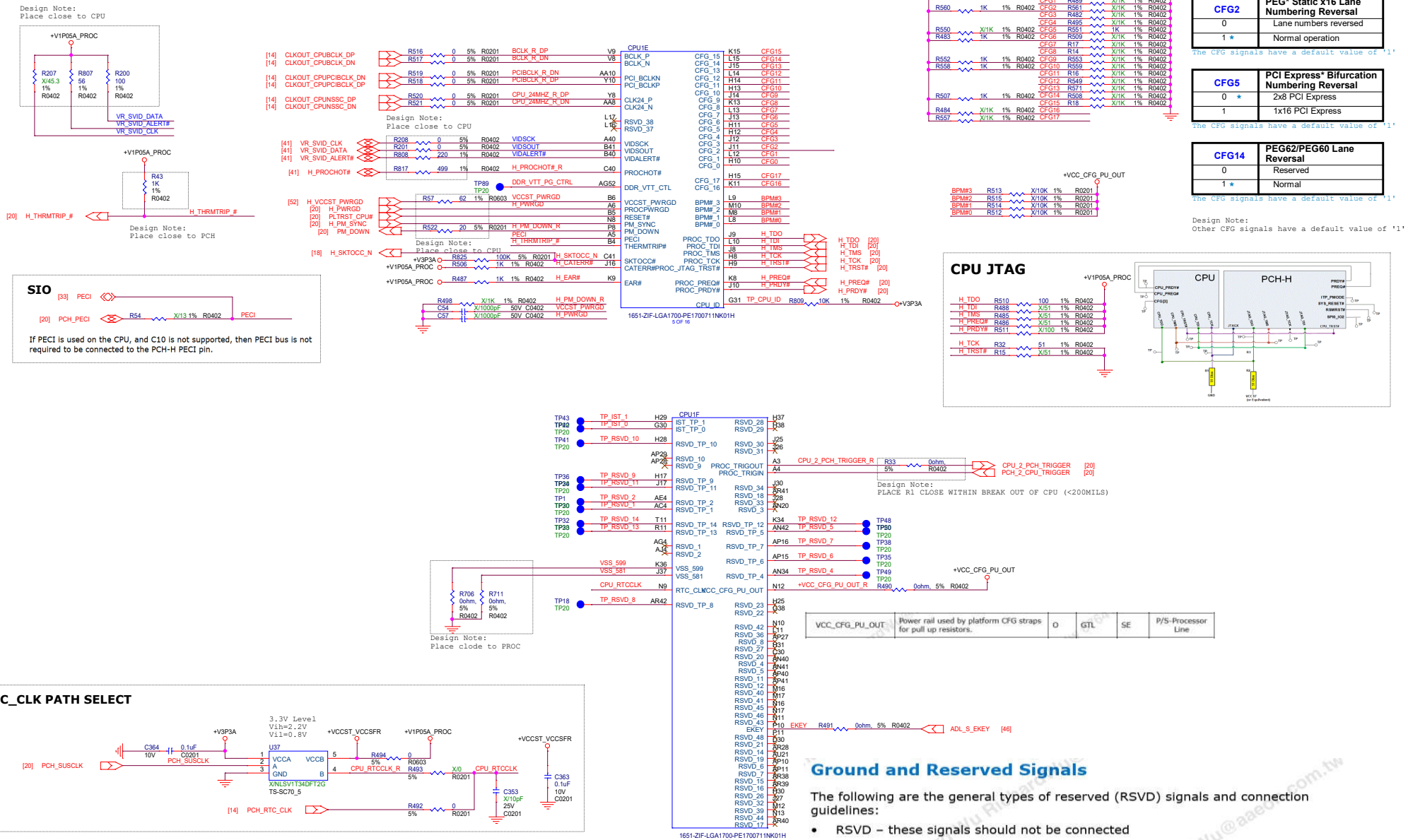
AAEON Technology INC.

Title: PROCESSOR 2_DDI/EDP		
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 6 of 57	

PROCESSOR 3_DDR4



PROCESSOR 4_CLK/CFG/RSVD

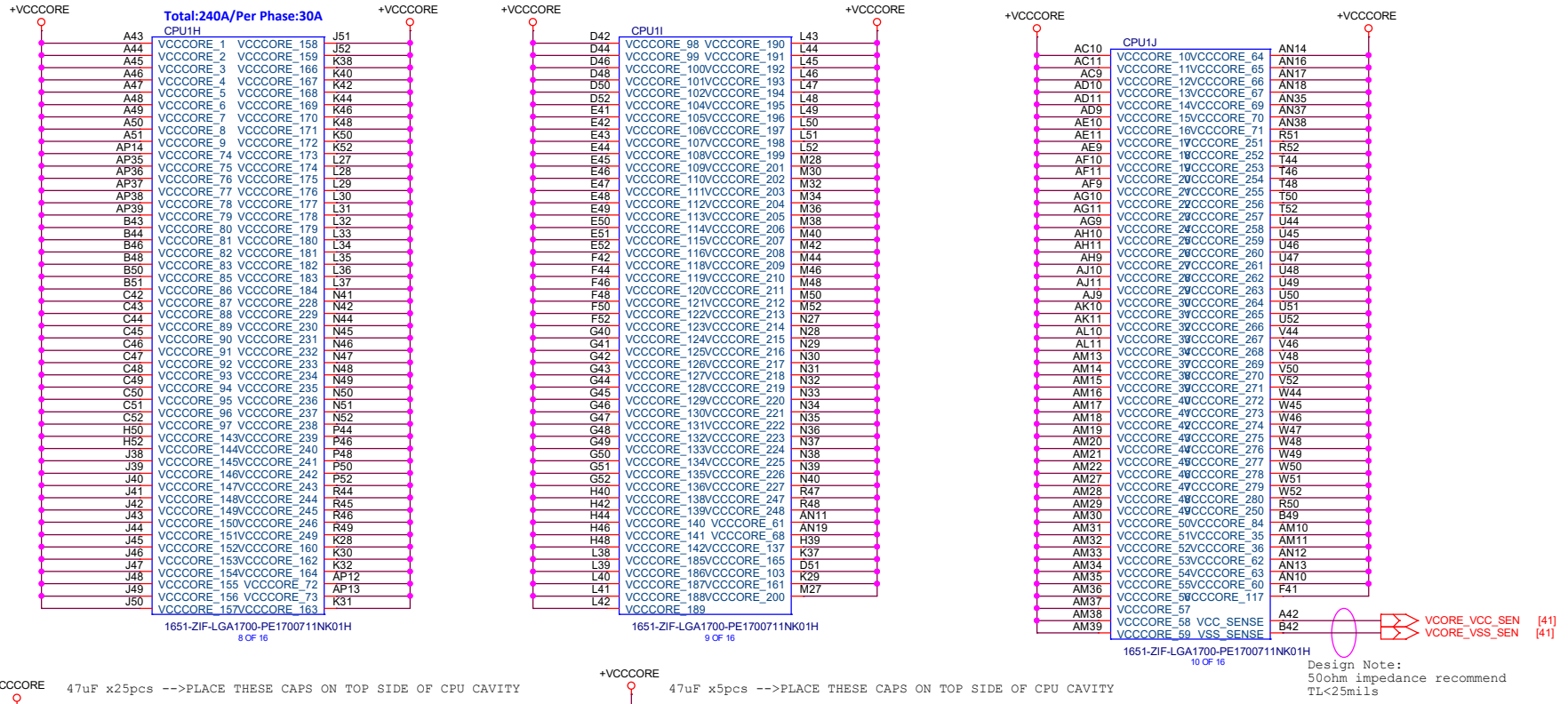


<Variant Name>

AAEON Technology INC.

Title	PROCESSOR 4_CLK/CFG/RSVD	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 8 of 57	

PROCESSOR 5_POWR1



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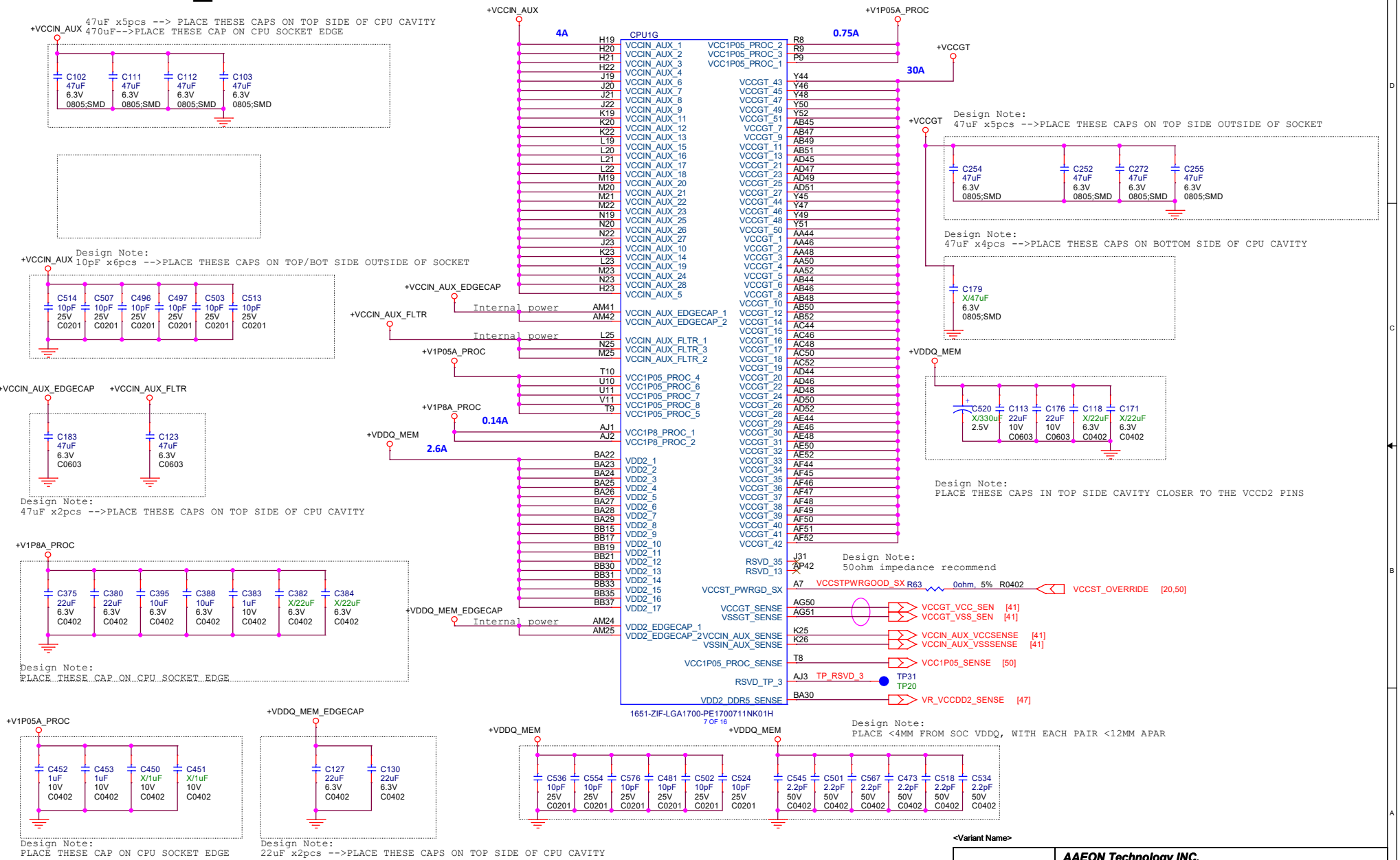
AAEON Technology INC.

Title	PROCESSOR 5_POWR1	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 9 of 57	

PROCESSOR 6_POWR2



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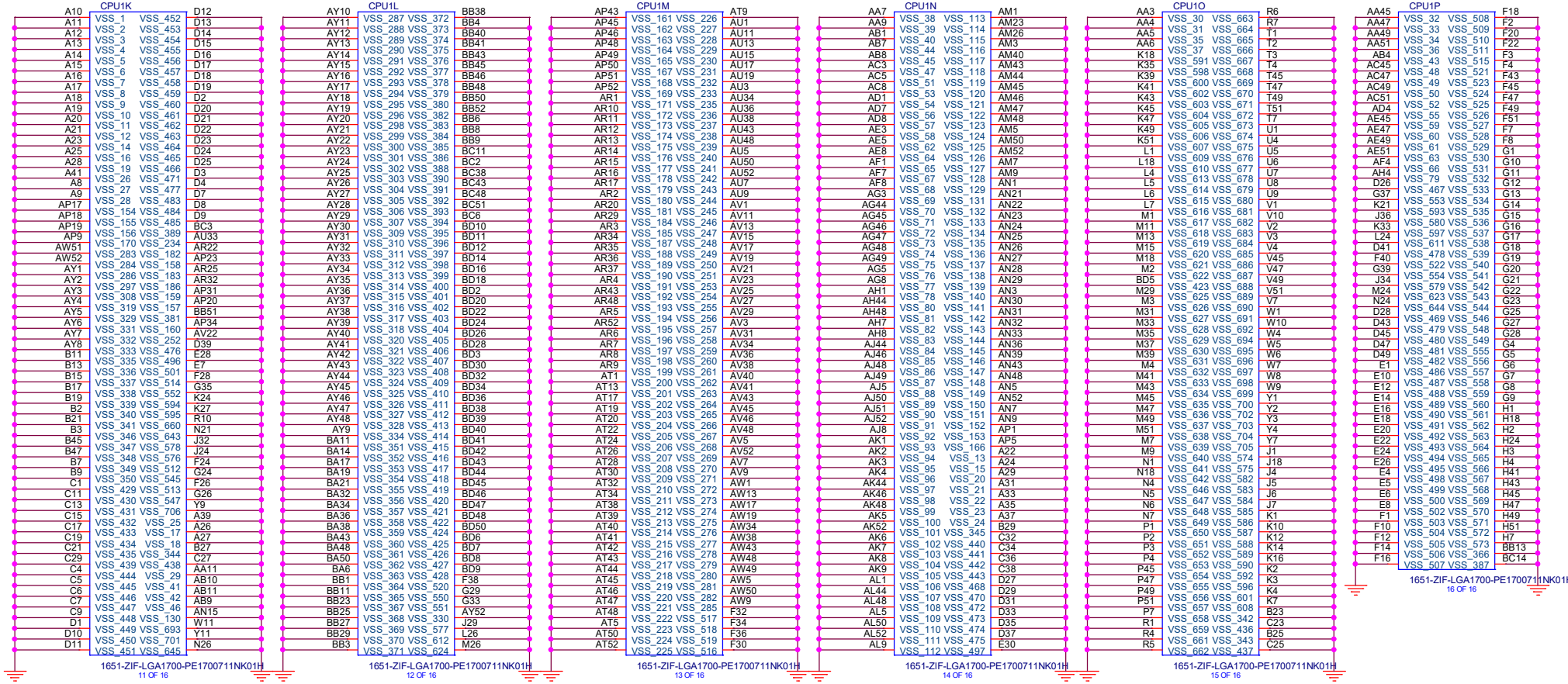
AAEON Technology INC.

Title	PROCESSOR 6_POWR2		
Size	Document Number		Rev
	EPIC-ADS7		A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 10	of 57	

PROCESSOR 7-VSS

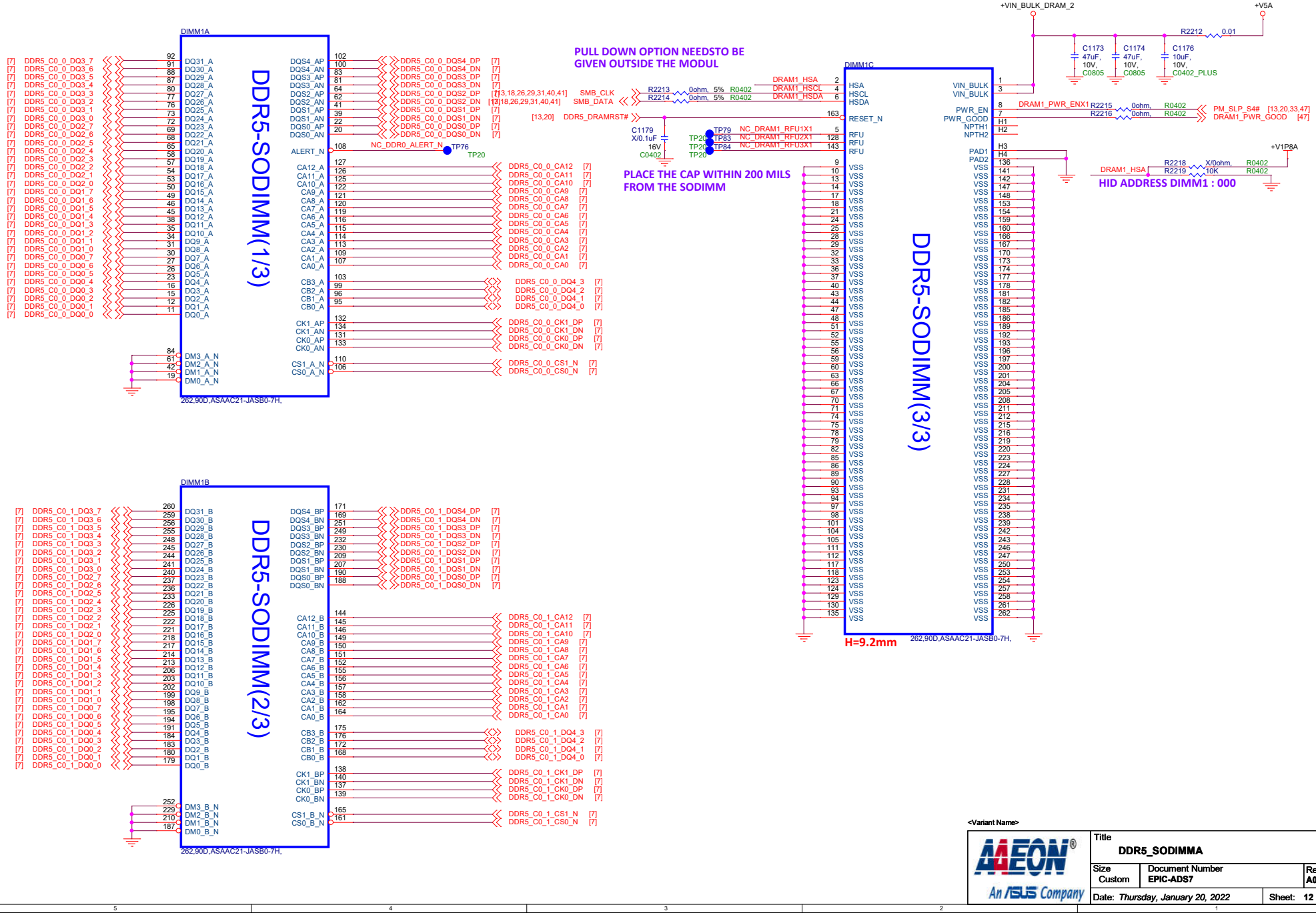


<Variant Name>

AAEON Technology INC.

Title	PROCESSOR 7_VSS	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 11 of 57	

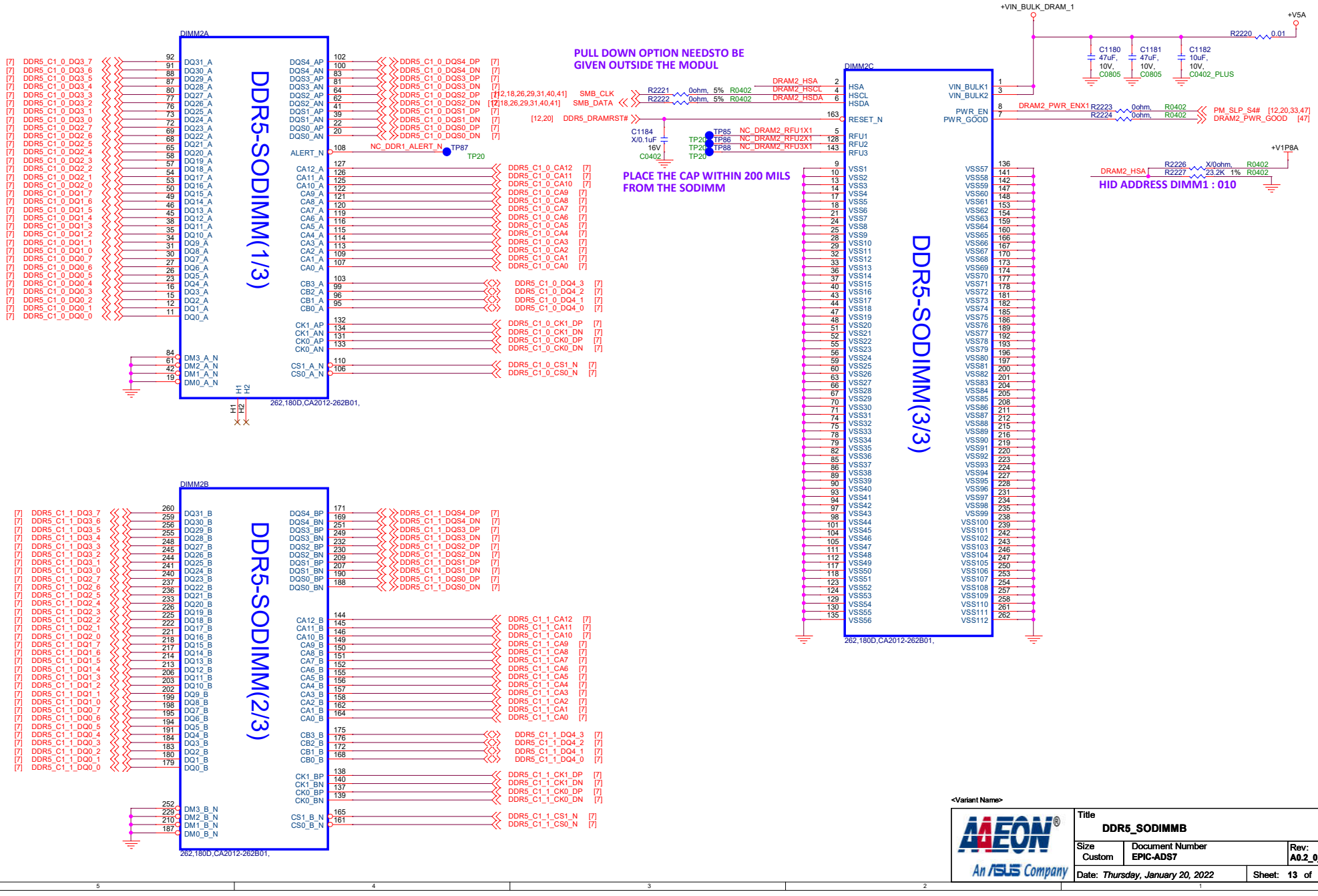
DDR5 SODIMM 1



<Variant Name>

AAEON An ASUS Company	Title: DDR5_SODIMMA	
	Size: Custom	Document Number: EPIC-ADS7 — Rev: A0.2_0_0
	Date: Thursday, January 20, 2022	Sheet: 12 of 57

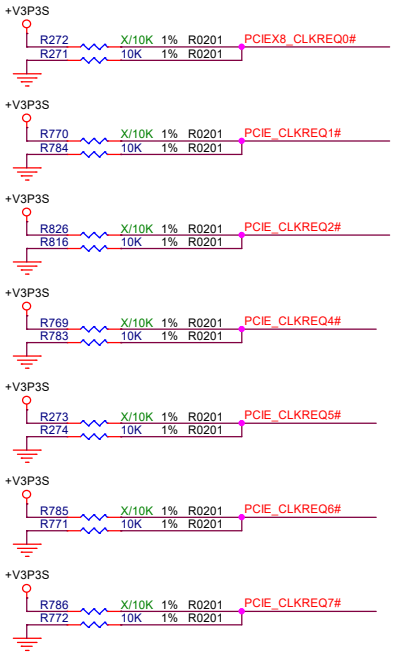
DDR5 SODIMM 2

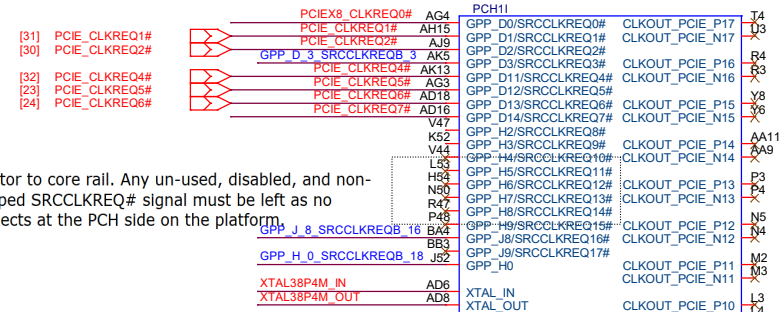


<Variant Name>

Title: DDR5_SODIMMB		
Size: Custom	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022		Sheet: 13 of 57

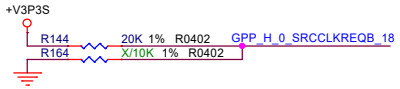
PCH1_CLK



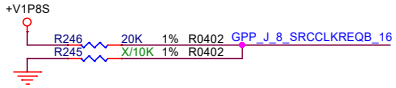


resistor to core rail. Any un-used, disabled, and non-mapped SRCCLKREQ# signal must be left as no connects at the PCH side on the platform.

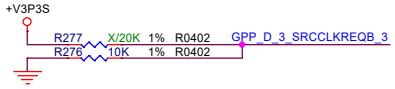
GPP_H0	SV ADVANCE MENU TABLE
0	SV ADVANCE MENU
1 *	NORMAL MENU (DEFAULT)



GPP_J8	TEST SETUP MENU TABLE
0	TEST SETUP MENU ENABLED
1 *	DISABLED (DEFAULT)



GPP_D3	GFX SELECT TABLE
0 *	NORMAL GFX
1	CUSTOMER GFX



To FPC

To I225

To I219

To M.2 B Key 3042/3052

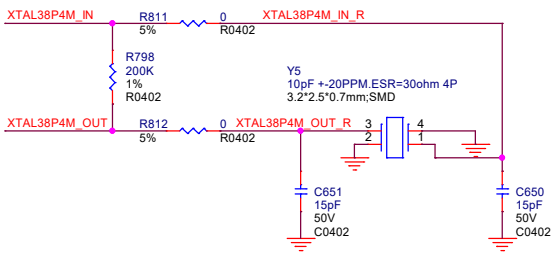
To M.2 M Key

To M.2 E Key

To PCIE X 8

To CPU

XTAL-38.4MHz



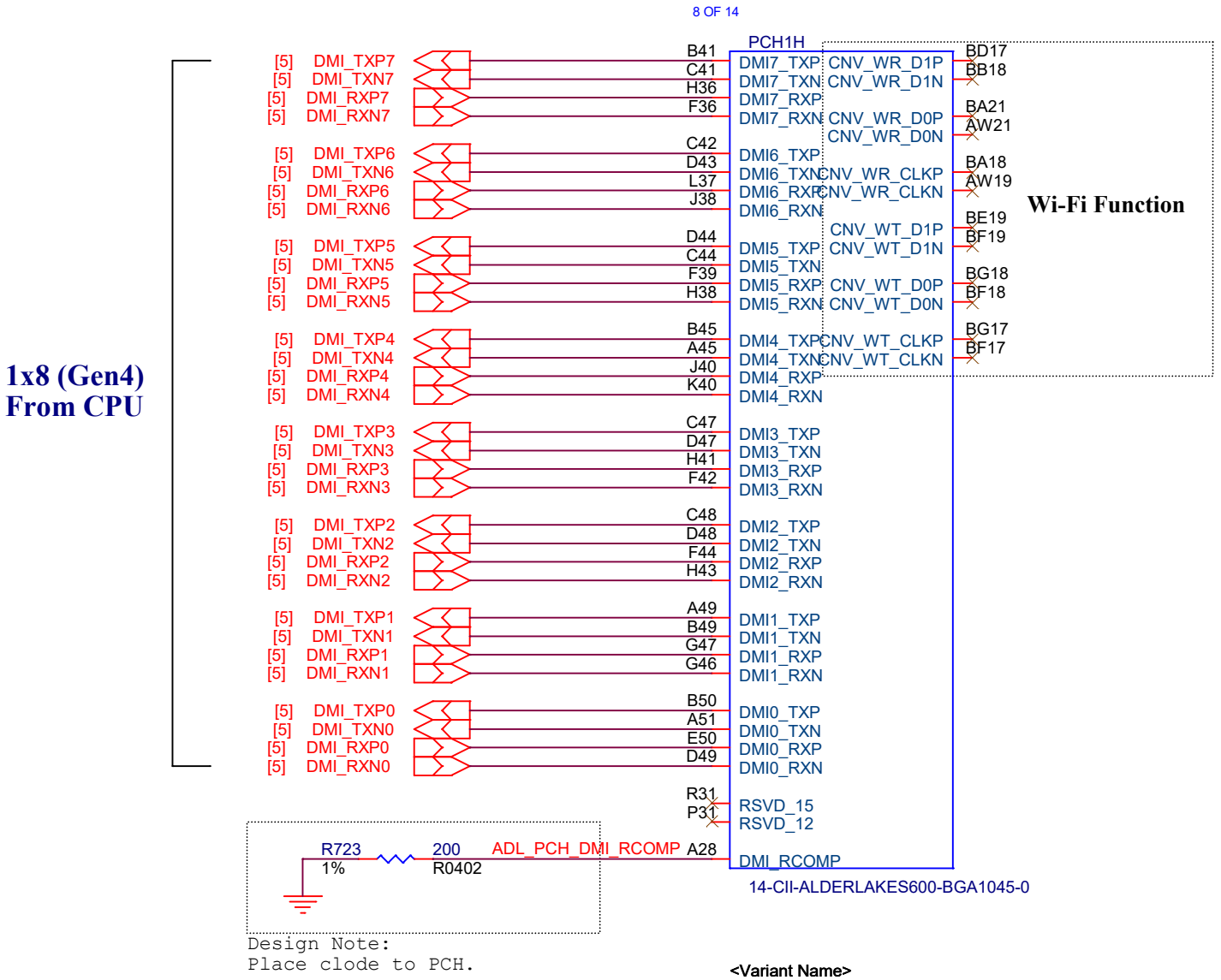
Signal Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[17:0] CLKOUT_PCIE_N[17:0]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N[3:0] can be used for PCIe Gen5 support. • CLKOUT_PCIE_P/N[17:4] can be used for PCIe Gen4 support.

<Variant Name>

AAEON Technology INC.

Title	PCH1_CLK	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 14 of 57	

PCH2_DMI



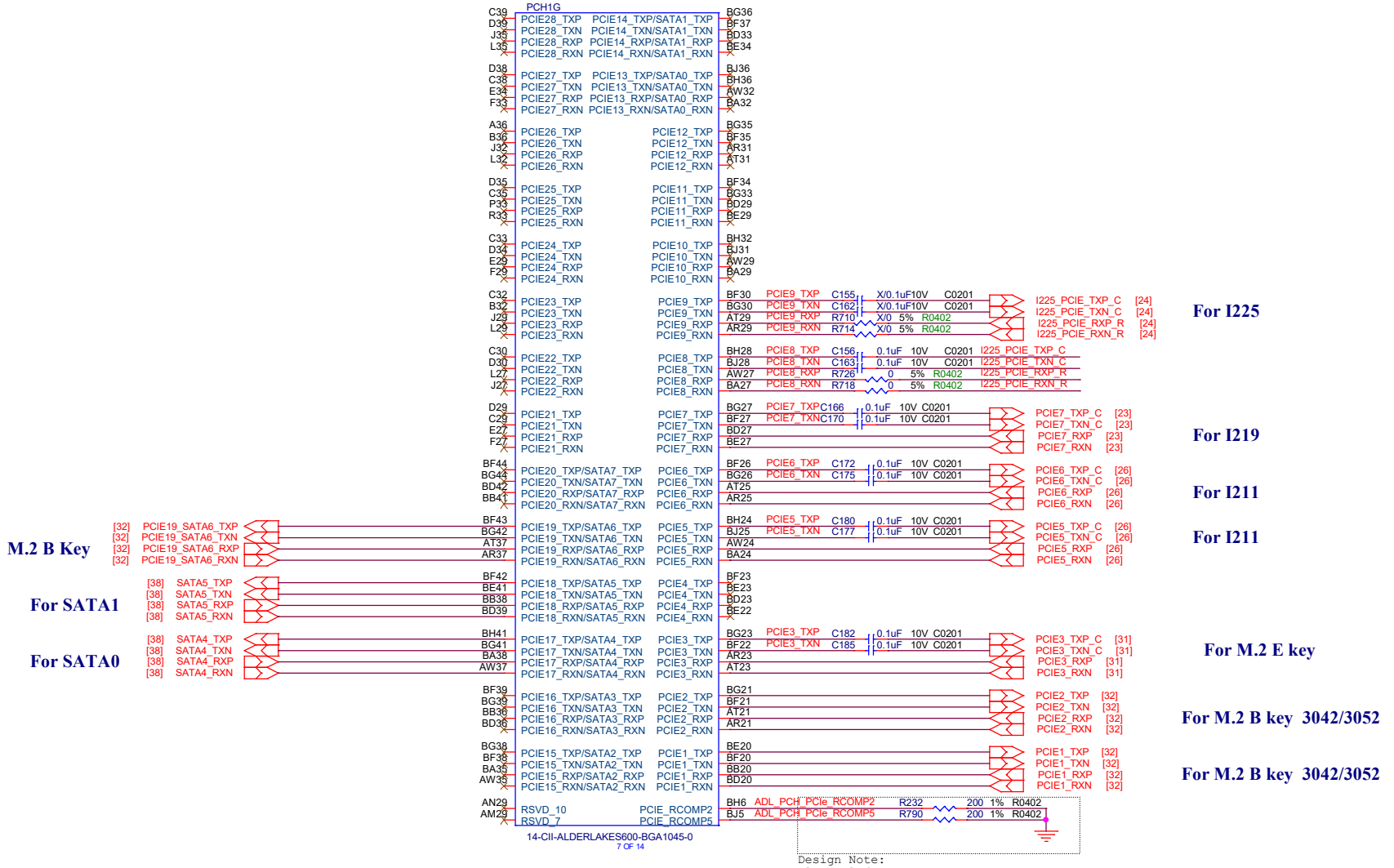
<Variant Name>

AAEON An ASUS Company

AAEON Technology INC.

Title			
PCH2_DMI			
Size	Document Number		Rev
	EPIC-ADS7		A0.2_0_0
Date: Thursday, January 20, 2022		Sheet 15 of 57	

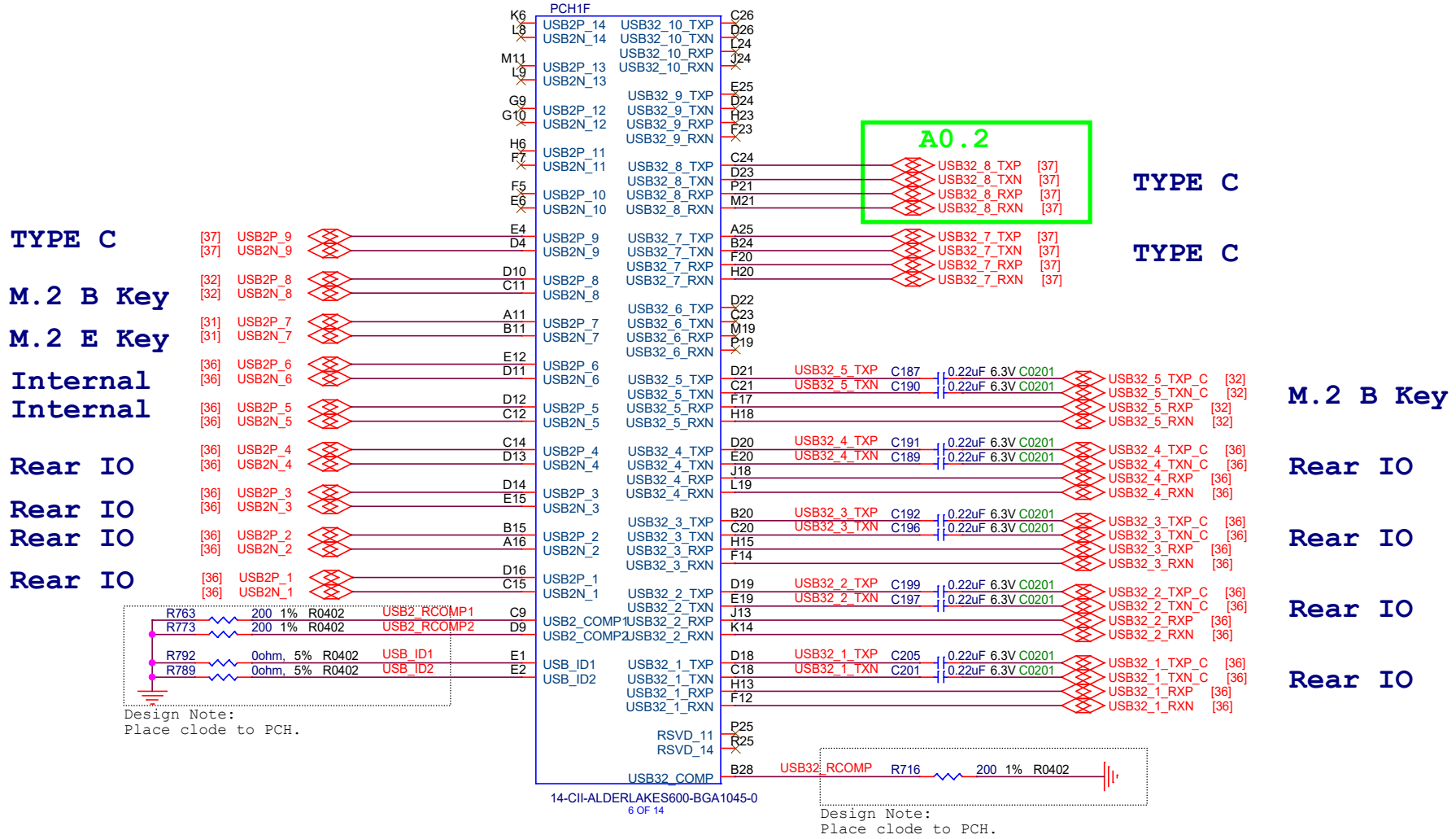
PCH3_PCIE/SATA



<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.	
	Title: PCH3_PCIE/SATA	
	Size:	Document Number: EPIC-ASD7 — Rev: A0.2_0_0
	Date: Thursday, January 20, 2022	Sheet 16 of 57

PCH4_USB3.2/USB2



4. Up to eight USB 3.2 Gen 2x2 Lanes
   - A maximum of four USB 3.2 Gen 2x2 Ports can be enabled
   - USB 3.2 Gen 2x2 = 20 GT\s

<Variant Name>

AAEON Technology INC.

Title	PCH4_USB3.2/USB2	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 17 of 57	

PCH5_I2C/SMLINK/UART/SMB

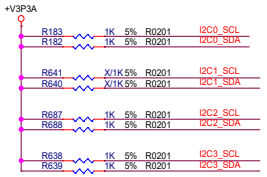
SCI / SMI# and NMI

SCI capability is available on all GPIOs, while SMI and NMI capability is available on only select GPIOs.

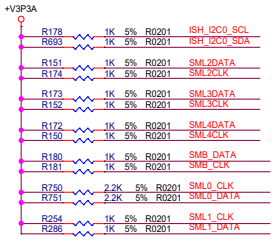
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:

- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0], GPP_E[16:13]

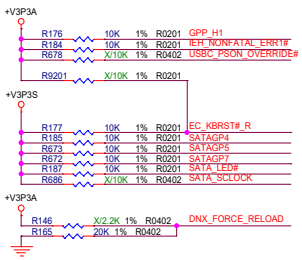
I2C Pull-Up



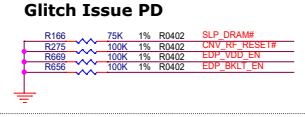
SMLink Pull-Up

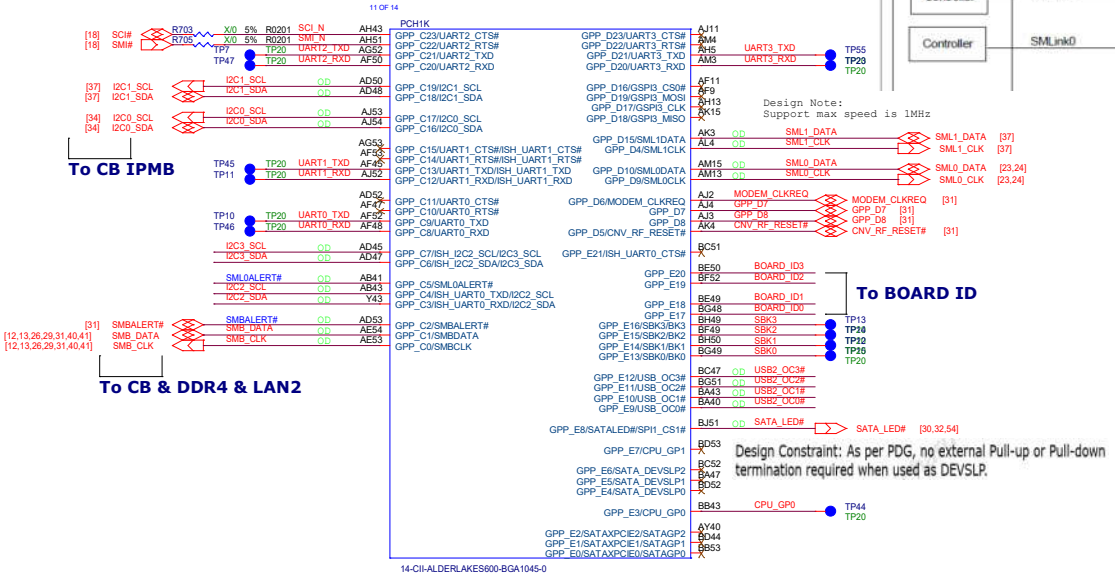


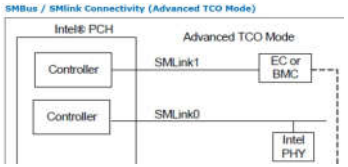
Others PU/PD



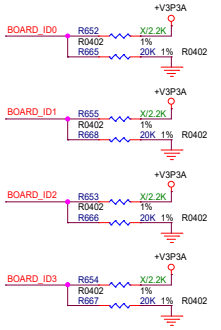
Glitch Issue PD



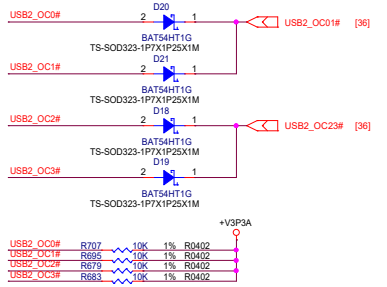




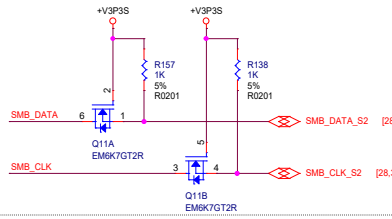
Design Note:
Support max speed is 1MHz

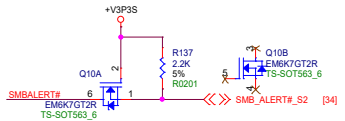


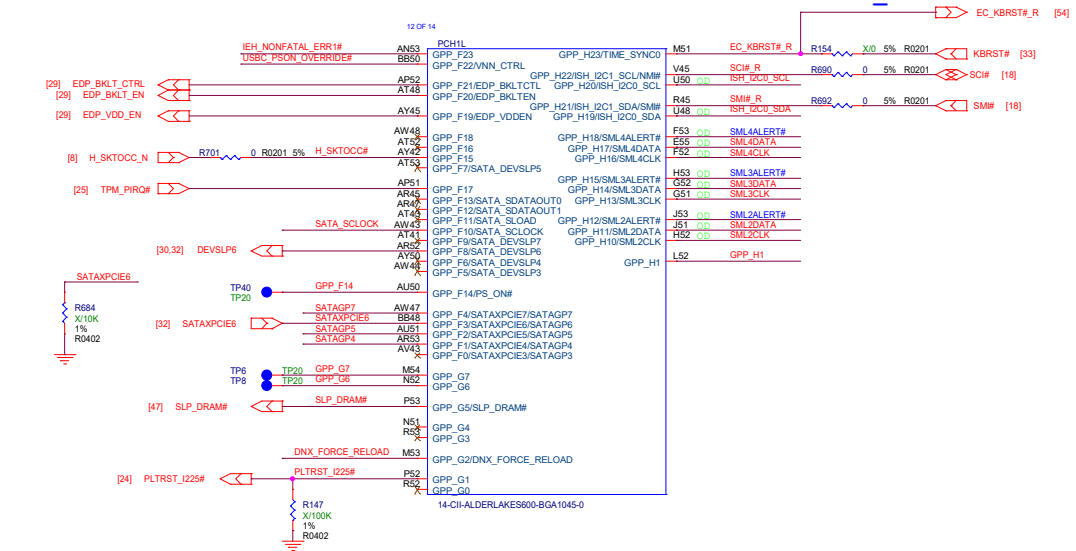
USB2.0 OC#



SMBus Level Shifter To DDR4

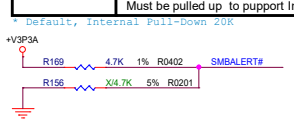






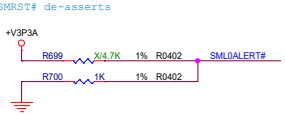
GPP_C2 SMBALERT#	TLS confidentiality
0	Disable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 *	Enable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to pupport IntelR AMT with TLS.

* Default, Internal Pull-Down 20K



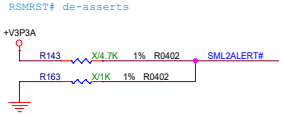
GPP_C5 SML0ALERT#	ESPI DISABLE
0 *	Enabled (Default)
1	Disabled

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts



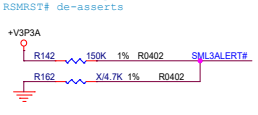
GPP_H12 SML2ALERT#	ESPI Flash Sharing Mode
0 *	Master Attached Flash Sharing (MAFS)
1	Slave Attached Flash Sharing (SAFS)

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts



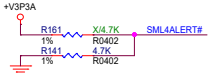
GPP_H15 SML3ALERT#	JTAG ODT Disable
0 *	JTAG ODT is disabled
1	JTAG ODT is enabled

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts



GPP_H18 SML4ALERT#	VCCSPI voltage configuration
0 *	VCCSPI at 3.3 V
1	VCCSPI at 1.8 V

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts



<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.		
	Title: PCH5_I2C/SMLINK/UART/SMB		
	Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
	Date: Thursday, January 20, 2022	Sheet 18 of 57	

PCH6_CNVi/GSPI/SNDW/HDA

GSPI0_MOSI	No Reboot
0 *	Disable
1	Enable

* Default, Internal Pull-Down 20K

+V3P3A — R214 X/4.7K 1% R0402 — GSPI0_MOSI

GPP_J4	M.2 CNVi Mode Select
0 *	Integrated CNVi enabled.
1	Integrated CNVi disabled.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.

+V1P8A — R242 4.7K 1% R0402 — GPP_J4; R241 X/20K 1% R0402

GPP_J2	XTAL FREQUENCY SEL0 (Bit 0)
	00 : 24MHz 01 : Reserved * 10 : 38.4MHz 11 : 25MHz

* Default, Internal Pull-Down 20K
* The internal pull-down is disabled after RSMRST# de-asserts

+V1P8A — R819 X/4.7K 1% R0402 — GPP_J2; R804 X/4.7K 1% R0402

GSPI1_MOSI	BOOT BIOS STRAP (BBS)
0 *	SPI(MAF) or eSPI(SAF)
1	eSPI

* Default, Internal Pull-Down 20K

+V3P3A — R198 X/4.7K 1% R0402 — GSPI1_MOSI; R197 20K 1% R0402

HDA_SDO	Flash Descriptor Security Override [ME]
0 *	Enable (Debug only)
1	Disabled (Default)

* Default, Internal Pull-Down 20K

+V3P3A — R229 X/1K 1% R0402; R231 10K 1% R0402 — HDA_SDO_R

Reserved Glitch Recommend

+V1P8A — R249 100K 1% R0402 — CPU_C10_GATE#; R248 X/100K 1% R0402
R752 X/33K 1% R0402 — GPP_R7; R219 X/100K 1% R0402 — HDA_BCLK_R; R228 X/33K 1% R0402 — HDA_RST#_R

13 OF 14

1. GPP_J and GPIO S groups support 1.8 V only.

PCH1M

GPP_J11/BSSB_LS_TX	AY4	BE15	GPP_I20/GSPI1_CLK
GPP_J10/BSSB_LS_RX	AT6	BF13	GPP_I21/GSPI1_MISO
GPP_J7/CNV_MFUART2_TXD	BB4	BF14	GPP_I10/GSPI1_CS1#/TIME_SYNC1
GPP_J6/CNV_MFUART2_RXD	AV12	BG14	GPP_I19/GSPI1_CS0#
GPP_J5/CNV_RGI_RSP/UART0_CTS#	BC4	BG15	GPP_I22/GSPI1_MOSI
GPP_J4/CNV_RGI_DT/UART0_TXD	BC5	BG11	GPP_I9/GSPI0_CS1#
GPP_J3/CNV_BRI_RSP/UART0_RXD	BA5	BH11	GPP_I16/GSPI0_CLK
GPP_J2/CNV_BRI_DT/UART0_RTS#	AU6	BF10	GPP_I17/GSPI0_MISO
GPP_J1/CPU_C10_GATE#	BA3	BE12	GPP_I18/GSPI0_MOSI
GPP_J0/CNV_PA_BLANKING	BB2	BF11	GPP_I15/GSPI0_CS0#
GPP_K11	BB54	BB13	GPP_I13/USB_OC6#/I2C5_SDA
GPP_K9/CORE_VID1	AW53	BD12	GPP_I14/USB_OC7#/I2C5_SCL
GPP_K3/GSXSRESET#	BA51	BA16	GPP_I11/USB_OC4#/I2C4_SDA
GPP_K2/GSXDIN	AY52	AY16	GPP_I12/USB_OC5#/I2C4_SCL
GPP_K1/GSXSLOAD	BA53	BE10	GPP_I8/DDPC_CTRLDATA
GPP_K0/GSXDOUT	BA52	BG9	GPP_I7/DDPC_CTRLCLK
GPP_K8/CORE_VID0	AW52	BG12	GPP_I6/DDPB_CTRLDATA
GPP_K4/GSXCLK	BB52	BF12	GPP_I5/DDPB_CTRLCLK
GPP_K5/ADR_COMPLETE	AV51	BA13	GPP_I4/DDSP_HPD4/DISP_MISC4
		BB15	GPP_I3/DDSP_HPD3/DISP_MISC3
		BD14	GPP_I2/DDSP_HPD2/DISP_MISC2
		BH15	GPP_I1/DDSP_HPD1/DISP_MISC1
		BJ16	GPP_I0/EXT_PWR_GATE#

TP22 TP20 CNV_MFUART2_TXD; TP52 TP20 CNV_MFUART2_RXD
GPP_J4; GPP_J2; CPU_C10_GATE#; GPP_K11
[49] PCH_CORE_VID_1_VR — GSXRESET#
[41,49] PCH_CORE_VID_0_VR — GSXCLK
TP5 TP20 ADR_COMPLETE

Design Note:

CORE VID0/1:
In default mode this pin is driven high.

14-CII-ALDERLAKES600-BGA1045-0

+V3P3S — R977 10K 1% R0402 — TIME_SYNC1 — TIME_SYNC1 [54]
GPP_J1/CPU_C10_GATE# — TP19 — GSPI1_MOSI
GPP_J0/CNV_PA_BLANKING — TP20 — GSPI0_MOSI; GSPI0_CLK; GSPI0_CS0#
GPP_K11 — USB2_OC6#; USB2_OC7#
GPP_K3/GSXSRESET# — USB2_OC4#; USB2_OC5# — USB2_OC4# [36]
GPP_K5/ADR_COMPLETE — DDID_HPD; DDIC_HPD; DDIB_HPD
GPP_I0/EXT_PWR_GATE# — EXT_PWR_GATE#

+V3P3A
EXT_PWR_GATE# R199 100K 5% R0201
GPP_K11 R170 X/10K 1% R0201
GSXRESET# R160 X/10K 1% R0402
GSXCLK R158 X/10K 1% R0402

USB2.0 OC#

+V3P3A
USB2_OC4# R747 10K 1% R0402
USB2_OC5# R736 10K 1% R0402
USB2_OC6# R202 10K 1% R0402
USB2_OC7# R209 10K 1% R0402

DDPx_CTRLCLK/CTRLDATA PU

+V3P3S
DDIA_CTRL_DATA R235 2.2K 1% R0402
DDIA_CTRL_CLK R759 2.2K 1% R0402
DDIB_CTRL_DATA R238 2.2K 1% R0402
DDIB_CTRL_CLK R239 2.2K 1% R0402
DDID_CTRL_DATA R781 2.2K 1% R0402
DDID_CTRL_CLK R780 2.2K 1% R0402
DDIC_CTRL_DATA R767 2.2K 1% R0402
DDIC_CTRL_CLK R760 2.2K 1% R0402

GSPI PU

+V3P3S
GSPI0_CLK R210 X/49.9K 1% R0201
GSPI0_MISO R213 X/49.9K 1% R0201
GSPI0_CS0# R206 X/49.9K 1% R0201

Digital Display Signals

Port	Name	Type	Description
A	GPP_R9 / **DDSP_HPDA** / DISP_MISCA	I	HPD Hot-Plug Detect.
Unconnected	GPP_R10 / **DDSP_HPDB** / DISP_MISCB	I	HPD Hot-Plug Detect.
Unconnected	GPP_R11 / **DDSP_HPDC** / DISP_MISCC	I	HPD Hot-Plug Detect.
B	GPP_I1 / **DDSP_HPD1** / DISP_MISC1	I	HPD Hot-Plug Detect.
C	GPP_I2 / **DDSP_HPD2** / DISP_MISC2	I	HPD Hot-Plug Detect.
D	GPP_I3 / **DDSP_HPD3** / DISP_MISC3	I	HPD Hot-Plug Detect.
E	GPP_I4 / **DDSP_HPD4** / DISP_MISC4	I	HPD Hot-Plug Detect.

[29] HPDA — Q23B — R724 1M 5% R0201 — EDP_HPD; R725 100K 1% R0402
[28] HDMI_HPD — Q23A — R730 1M 5% R0201 — DDIB_HPD; R731 100K 1% R0402
[27] DP1_HPD — Q22B — R717 1M 5% R0201 — DDIC_HPD; R719 100K 1% R0402
[27] DP2_HPD — Q22A — R713 1M 5% R0201 — DDID_HPD; R712 100K 1% R0402
EM6K7GT2R TS-SOT563_6

PCH1N

GPP_S7/SNDW4_DATA/DMIC_DATA0	BF48	BA9	DDIA_CTRL_DATA
GPP_S6/SNDW4_CLK/DMIC_CLKA0	BF47	AY14	DDIA_CTRL_CLK
GPP_S5/SNDW3_DATA/DMIC_DATA1	BG47	BD4	DDIC_CTRL_DATA
GPP_S4/SNDW3_CLK/DMIC_CLKA1	BE46	BE1	DDIC_CTRL_CLK
GPP_S3/SNDW2_DATA/DMIC_CLKB1	BF46	BE2	DDIB_CTRL_DATA
GPP_S2/SNDW2_CLK/DMIC_CLKB0	BG45	BB8	DDIB_CTRL_CLK
GPP_S1/SNDW1_DATA	BH45	AW8	
GPP_S0/SNDW1_CLK	BJ45	AY6	
GPP_R15/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI		AW9	DDID_CTRL_DATA
GPP_R14/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO		AV11	DDID_CTRL_CLK
GPP_R13/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK		BC9	
GPP_R12/ISH_SPI_CS#/DDP3_CTRLCLK/GSPI2_CS0#		BH7	
GPP_R11/DDSP_HPDC/DISP_MISCC		BD3	EDP_HPD
GPP_R10/DDSP_HPDB/DISP_MISCB		BE6	
GPP_R9/DDSP_HPDA/DISP_MISCA		AY11	GPP_R7
GPP_R8		BB6	
GPP_R7		BJ7	HDA_SDI1_R
GPP_R6		BE7	HDA_RST#_R
GPP_R5/HDA_SDI1		BF9	HDA_SDI0_R
GPP_R4/HDA_RST#		BF7	HDA_SDO_R
GPP_R3/HDA_SDI0/HDACPU_SDI		BF8	HDA_SYNC_R
GPP_R2/HDA_SDO/HDACPU_SDO		BG8	HDA_BCLK_R
GPP_R1/HDA_SYNC			
14 OF 14 GPP_R0/HDA_BCLK/HDACPU_BCLK			

DDIA_CTRL_DATA — DDIC_CTRL_DATA [27] — DDIC_CTRL_CLK [27] — DP1
DDIB_CTRL_DATA — DDIB_CTRL_DATA [28] — DDIB_CTRL_CLK [28] — HDMI
DDID_CTRL_DATA — DDID_CTRL_DATA [27] — DDID_CTRL_CLK [27] — DP2

TP21
HDA_SDI1_R — R223 33/R0201 — HDA_RST# [39]
HDA_RST#_R — HDA_SDI0_R [39]
HDA_SDO_R — R224 33/R0201 — HDA_SDOUT [39]
HDA_SYNC_R — R218 33/R0201 — HDA_SYNC [39]
HDA_BCLK_R — R222 33/R0201 — HDA_BIT_CLK [39]

14-CII-ALDERLAKES600-BGA1045-0

A0.2

DDPx_CTRLDATA		To disable DDI ports leave as No Connect. To enable Port 1 and 2, pull-up to 3.3 V with 2.2 KΩ ±5% resistor

<Variant Name>

AAEON Technology INC.

Title	PCH6_CNVi/GSPI/SNDW/HDA	
Size	Document Number	Rev
	EPIC-ADS7	A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 19 of 57	

PCH7_SPI/JTAG/MISC/ESPI

SPI0_MOSI	Reserved
	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on- board device driving it to opposite direction during strap sampling.

External pull-up is required. Recommend 4.7 kohm pull up.

+V3P3A R635 4.7K 1% R0402 SPI0_SI_R

SPI0_IO2	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

External pull-up is required.

+V3P3A R636 100K 1% R0402 SPI0_IO2_WP#

SPI0_IO3	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

External pull-up is required.

+V3P3A R633 100K 1% R0402 SPI0_IO3_HOLD#

DBG_PMODE	Reserved
	This strap should sample high. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-up.

R299 X/1K 1% R0402 DBG_PMODE

SPKR	Top Swap Override
0 *	Disabled
1	Enable

* Default, Internal Pull-Down 20k

+V3P3A R149 X/4.7K 1% R0402 SPKR
R148 X/20K 1% R0402

SPI0_CS0#	Chip Select0	SPI0 chip select 0
SPI0_CS1#	Chip Select1	SPI0 chip select 1, signal is used as the second chip select when 2 flash devices are used. Do not use when only one SPI0 flash is used
SPI0_CS2#	Chip Select2	Chip Select 2 is dedicated to support TPM on SPI0

To TPM

DSW_PWROK and RSMRST# can be short together and can be driven High only after DSW and all PRIM rail are ON and stable

PCH1E
SPI0_CLK SPI0_CS2# SPI0_MISO SPI0_IO3 SPI0_MOSI SPI0_IO2 SPI0_CS0# SPI0_CS1#
PCH_JTAGX PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TCK PCH_JTAG_TMS
CL_CLK CL_DATA CL_RST#
GPD12 GPD11/LANPHYPC GPD10/SLP_S5# GPD9/SLP_WLAN# GPD8/SUSCLK GPD7 GPD6/SLP_A# GPD5/SLP_S4# GPD4/SLP_S3# GPD3/PWRBTN# GPD2/LAN_WAKE# GPD1/ACPRESENT GPD0/BATLOW#
RSVD_2 RSVD_1
TRIGGER_IN TRIGGER_OUT
RSVD_6 RSVD_5
RSVD_17 WAKE# VCCST_OVERRIDE
RSVD_16 RSVD_13
SYS_PWROK SYS_RESET#
SLP_SUS# SLP_LAN# RSMRST# PCH_PWROK DSW_PWROK DBG_PMODE INTRUDER# DRAM_RESET#
PREQ# PRDY#
PM_DOWN PM_SYNC
RSVD_9 RSVD_8 VSS_102 VSS_101
HDACPU_BCLK HDACPU_SDO HDACPU_SDI
EXT_INJ_PCIEPHY_P EXT_INJ_PCIEPHY_N EXT_INJ_PCIEPHY
RSVD_3 RSVD_4
RTCX2 RTCX1 RTCRST#
PECI PLTRST_CPU#
SRTCRST# THRMTRIP#
CPU_TRST# CPUPWRGD C10_WAKE
SNDW_RCOMP
5 OF 14
14-CII-ALDERLAKES600-BGA1045-0

Design Note: 1.8V support only

PCH1J
GPP_A14 GPP_A0/ESPI_IO0 GPP_A1/ESPI_IO1 GPP_A2/ESPI_IO2/SUSWARN#/SUSPWRDNACK GPP_A3/ESPI_IO3/SUSACK# GPP_A4/ESPI_CS0# GPP_A5/ESPI_CLK GPP_A6/ESPI_RESET# GPP_A7/ESPI_CS1# GPP_A8/ESPI_CS2# GPP_A9/ESPI_CS3# GPP_A10/ESPI_ALERT0# GPP_A11/ESPI_ALERT1# GPP_A12/ESPI_ALERT2# GPP_A13/ESPI_ALERT3#
GPP_B23/SML1ALERT#/PCHHOT# GPP_B22 GPP_B21 GPP_B20/RSVD GPP_B19/RSVD GPP_B18/PMCALERT# GPP_B17/ISH_GP5 GPP_B16/ISH_GP4 GPP_B15/ISH_GP3 GPP_B14/SPKR GPP_B13/PLTRST# GPP_B12/SLP_S0# GPP_B11 GPP_B10/ISH_GP2 GPP_B9/ISH_GP1 GPP_B8/ISH_GP0 GPP_B7/ISH_GP7 GPP_B6/CLKOUT_48 GPP_B5/SX_EXIT_HOLDOFF#/ISH_GP6 GPP_B4/CPU_GP3 GPP_B3/CPU_GP2 GPP_B2/VRALERT# GPP_B1/ISH_UART0_RTS#/GSPI2_CS1# GPP_B0/PCIE_LNK_DOWN
14-CII-ALDERLAKES600-BGA1045-0
10 OF 14

CPU_GP can be used from external sensors for the thermal manageme

Design Note: Place close to PCH.

U8 SN74LVC1G08DCKR TS-SC70_5

Others PU/PD

+V3P3A
PCIE_WAKE# R749 4.7K 5% R0201
LAN_WAKE# R292 4.7K 5% R0201
O_BATLOW_R# R287 10K 1% R0201
AC_PRESENT R799 10K 1% R0201
PWRBTN# R768 10K 1% R0201
VRALERT# R689 10K 1% R0201
PMCALERT# R155 10K 1% R0201
SX_EXIT_HOLDOFF# R179 10K 1% R0201
SPI0_SO_R R637 X/20K 1% R0201

PCH_PECI R285 X/1K 1% R0402
+VDDQ_MEM
DDR5_DRAMRST# R821 470 1% R0402
+V3P3A_RTC
SM_INTRUDER# R748 1M 5% R0201
PCH_DPWROK R729 1M 5% R0201
C588 X/0.01uF 10V C0201

Glitch Recommend

PM_SLP_S5# R250 X/100K 1% R0402
SLP_S4# R805 100K 1% R0402
SLP_S3# R264 100K 1% R0402
SLP_A# R266 100K 1% R0402
PM_SLP_S0# R167 100K 1% R0402
SLP_SUS# R778 100K 1% R0402
SLP_LAN# R764 100K 1% R0402
SPI0_CLK_R R634 100K 1% R0402
SLP_WLAN# R735 100K 1% R0402
ESPI_CS_EC_R_N R2175 75K 1% R0402
ESPI_RST_EC_R_N R2176 75K 1% R0402

EMI Recommend

PCH_RSMRST# C603 X/1000pF 50V C0402
PCH_PWROK_R C645 X/1000pF 50V C0402
PCH_DPWROK C583 X/1000pF 50V C0402
CPUPWRGD_PCH_R C218 X/1000pF 50V C0402
O_SYS_PWROK C105 X/1000pF 50V C0402

GPP_B23 SML1ALERTB	XTAL FREQUENCY SEL0 (Bit 1)
	00 : 24MHz 01 : Reserved * 10 : 38.4MHz 11 : 25MHz

* Default, Internal Pull-Down 20k
* The internal pull-down is disabled after RSMRST# de-asserts

+V3P3A R145 4.7K 1% R0402 SML1ALERTB
R168 X/4.7K 1% R0402

GPD7	XTAL INPUT MODE (Reserved)
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A R823 X/150K 1% R0402 GPD_7
R806 20K 1% R0402

RTC Battery

+V3P3A_RTC
D10 1PS79SB30 TS-SOD523
D9 1PS79SB30 TS-SOD523
VCC_RTC level can't over 3.2V
+V3P3A R457 0/R0402
R456 X/45.3K/R0402
TP28 TP40
R464 1K/R0201
TP29 TP40
RTCRST# R23 20K/R0402
SRTCRST# R24 20K/R0402
C36 1uF/C0402 10V
C37 1uF/C0402 10V
C334 1uF/C0201 6.3V
JP1 3*1P 220-96-03GB01

Clear CMOS Jumper

Mode	
1-2(Default)	Save CMOS
2-3	Clear CMOS

JP1(1-2) 2.0mm 200-72-PBGB03
CN1(BATTERY)1 BP-CR2032-M150-002
CN1 2P 712-H74-025WR1
A0.2

XTAL-32.768KHz

RTC_X1 R802 0 5% R0402 RTC_32K_IN C648 18pF
R797 10M 5% R0402
Y4 12.5pF,32.768KHz,FC135,
RTC_X2 R803 0 5% R0402 RTC_32K_OUT C649 18pF

PCH JTAG

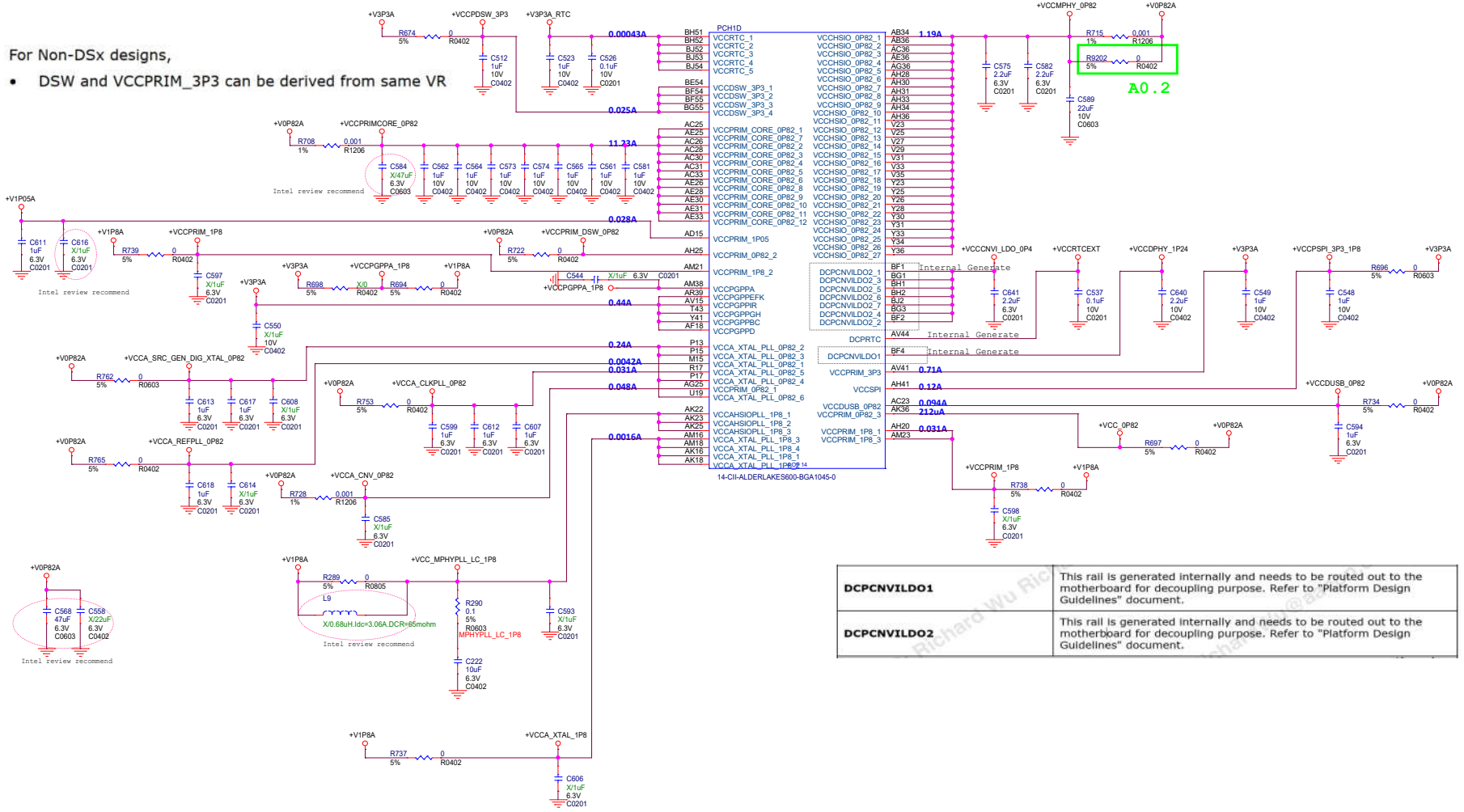
+V1P05A_PROC
PCH_JTAG_TDO R306 100 1% R0402
PCH_JTAG_TDI R307 51 1% R0402
PCH_JTAG_TMS R308 51 1% R0402
PCH_JTAG_TCK R775 X/51 1% R0402
PCH_JTAG_TRST# R300 X/51 1% R0402
PCH_JTAGX R298 X/51 1% R0402

<Variant Name>

AAEON Technology INC.
An ASUS Company

Title	PCH7_SPI/JTAG/MISC/ESPI	
Size	Document Number	Rev
	EPIC-ADS7	A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 20 of 57	

PCH8_POWER



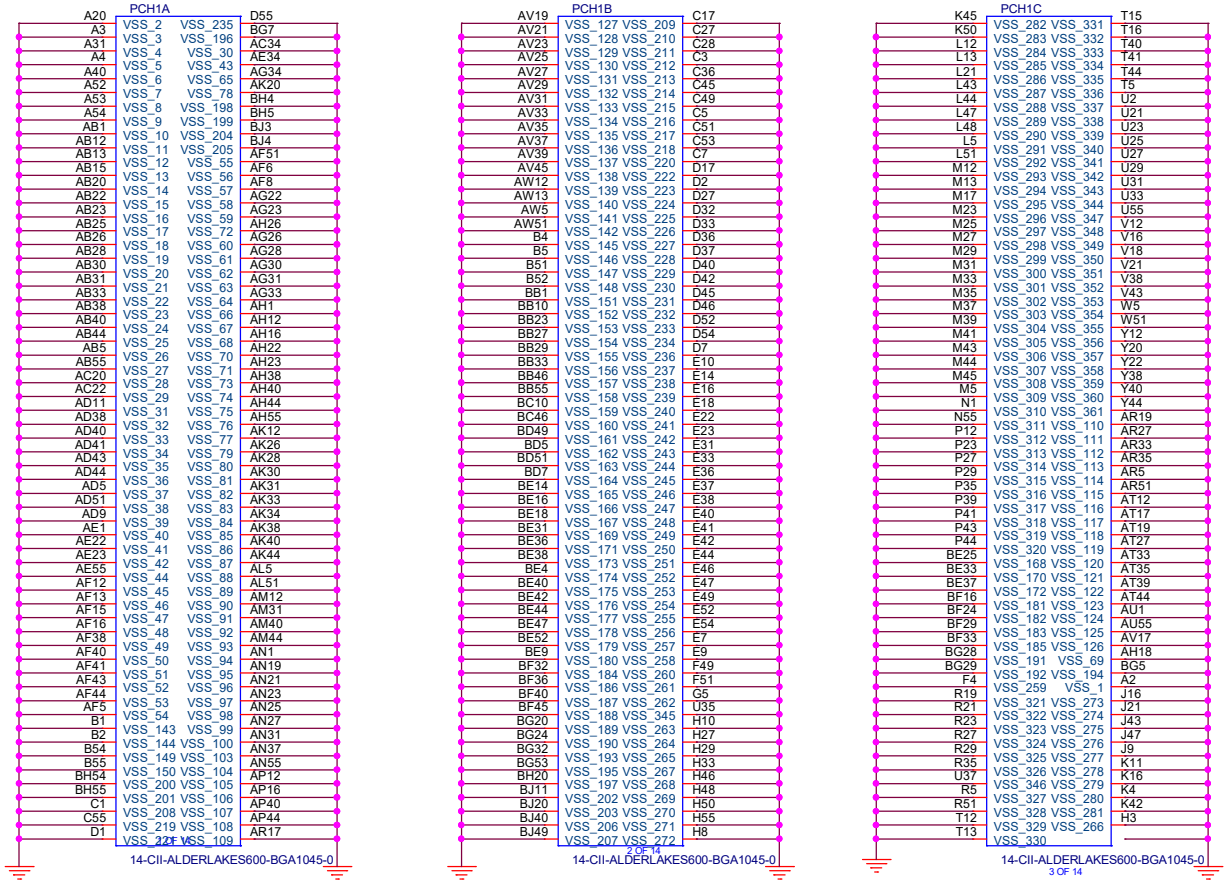
DCPCNVILDO1	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose. Refer to "Platform Design Guidelines" document.
DCPCNVILDO2	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose. Refer to "Platform Design Guidelines" document.

<Variant Name>

AAEON Technology INC.

Title	PCH8_POWER		
Size	Document Number		Rev
	EPIC-ADS7		A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 21	of 57	

PCH9_VSS



<Variant Name>

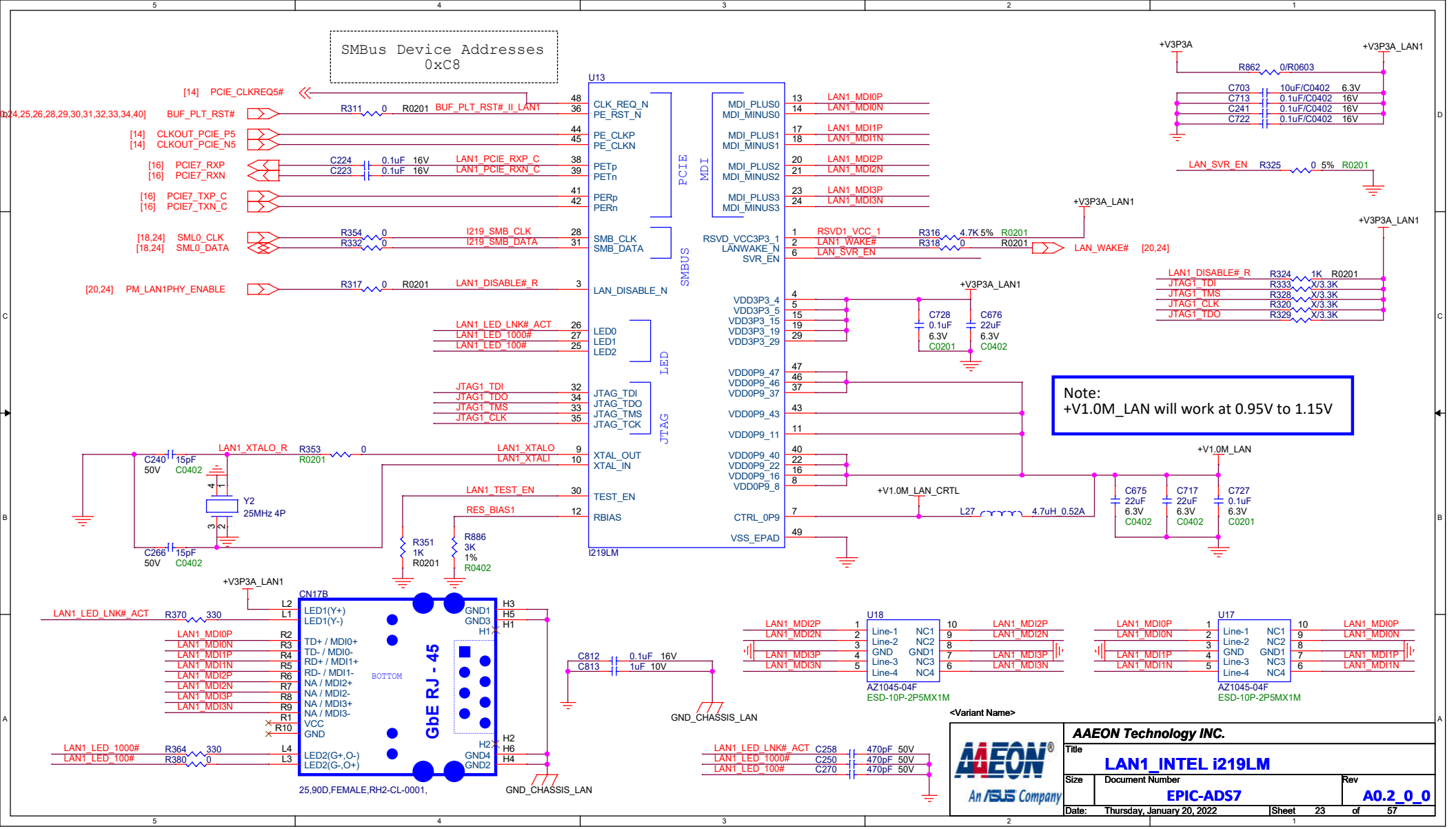
AAEON Technology INC.

Title: PCH9_VSS

Size | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

Date: Thursday, January 20, 2022 | Sheet 22 of 57

SMBus Device Addresses
0xC8



<Variant Name>

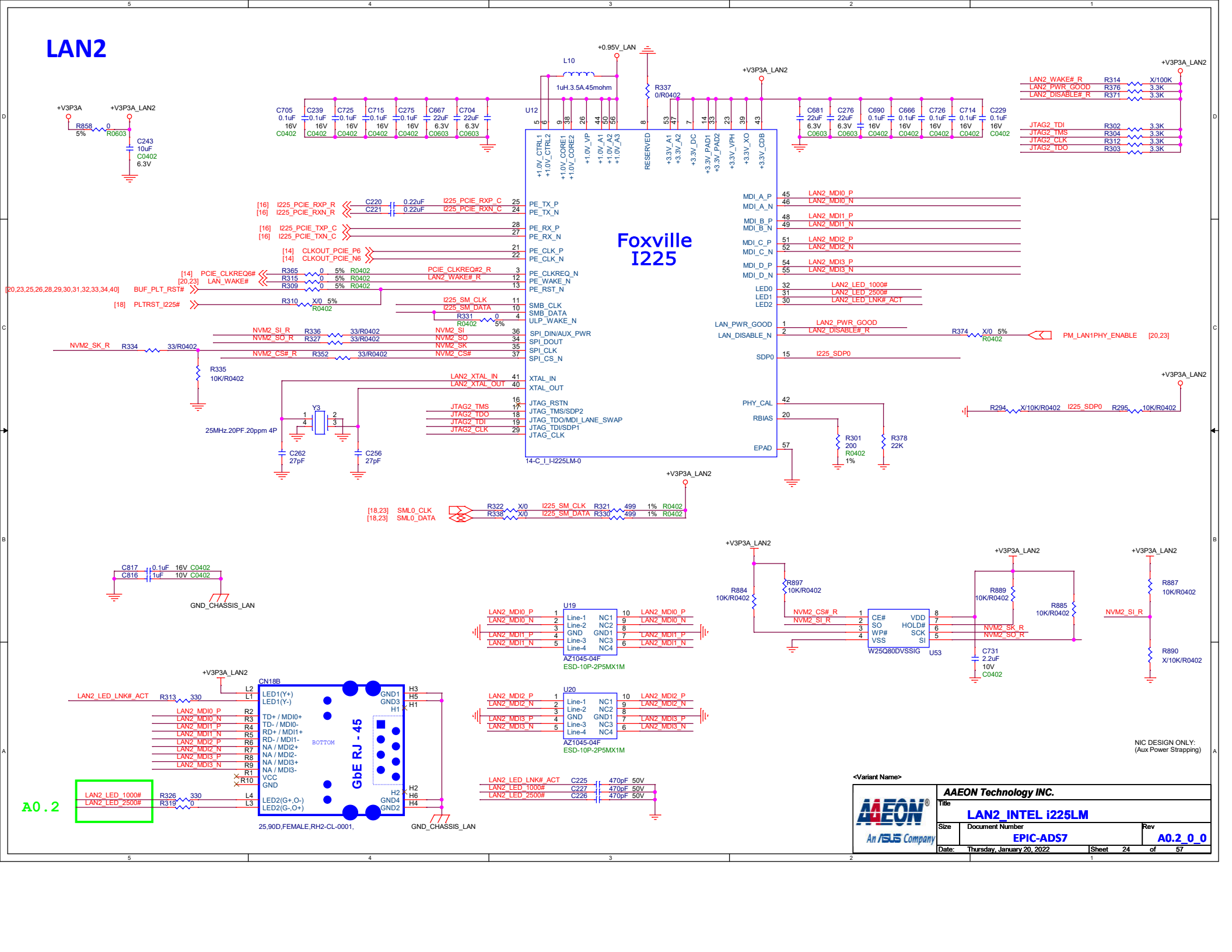
AAEON Technology INC.

Title: LAN1_INTEL i219LM

Size	Document Number	Rev
	EPIC-ADS7	A0.2_0_0

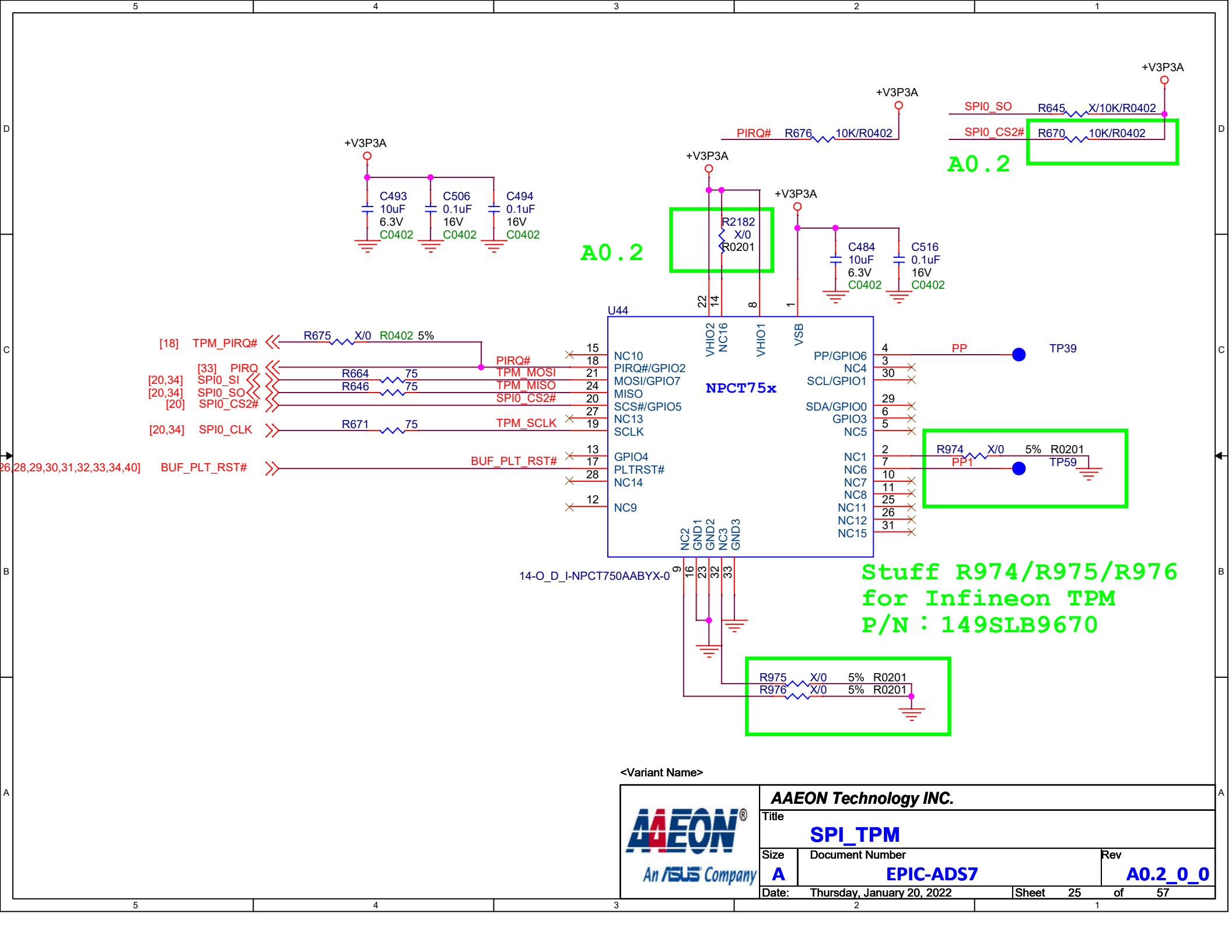
Date: Thursday, January 20, 2022 Sheet 23 of 57

LAN2

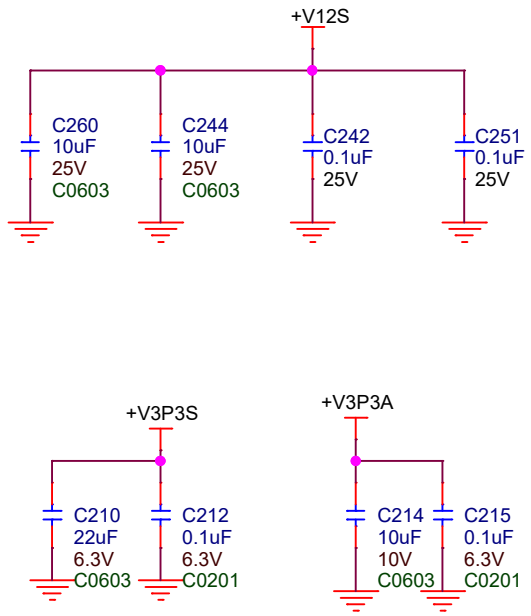


<Variant Name>

AAEON Technology INC.		
Title: LAN2_INTEL i225LM		
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 24 of 57	

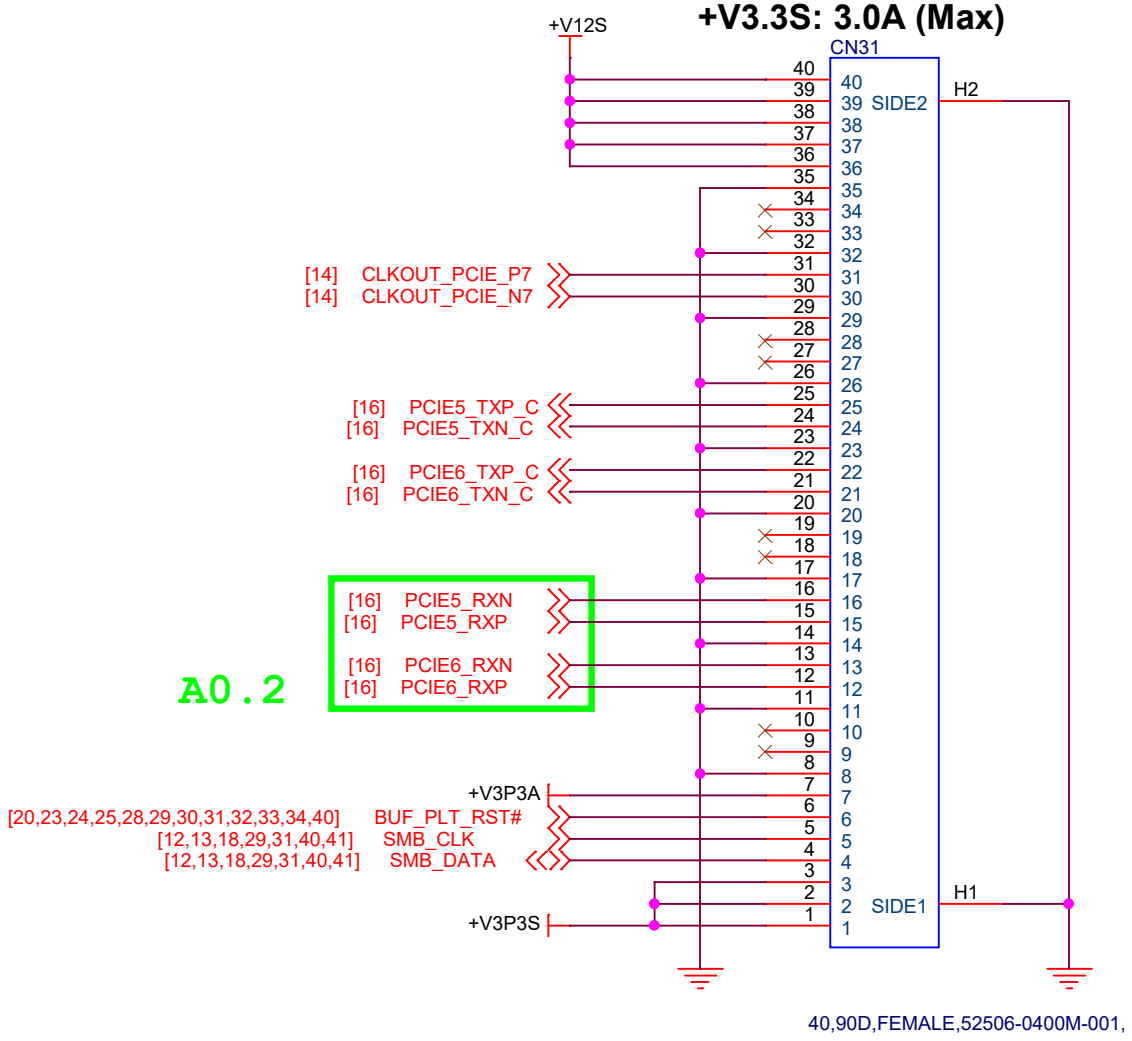

+V3P3A
C493
10uF
6.3V
C0402
C506
0.1uF
16V
C0402
C494
0.1uF
16V
C0402
A0.2
PIRQ# R676 10K/R0402
+V3P3A
SPI0_SO R645 X/10K/R0402
SPI0_CS2# R670 10K/R0402
+V3P3A
A0.2
R2182
X/0
R0201
+V3P3A
C484
10uF
6.3V
C0402
C516
0.1uF
16V
C0402
U44
NPCT75x
22 14 8 1
VHIO2 NC16 VHIO1 VSB
[18] TPM_PIRQ# R675 X/0 R0402 5%
[33] PIRQ
[20,34] SPI0_SI
[20,34] SPI0_SO
[20] SPI0_CS2#
[20,34] SPI0_CLK
[26,28,29,30,31,32,33,34,40] BUF_PLT_RST#
R664 75
R646 75
R671 75
PIRQ#
TPM_MOSI
TPM_MISO
SPI0_CS2#
TPM_SCLK
BUF_PLT_RST#
15 NC10
18 PIRQ#/GPIO2
21 MOSI/GPIO7
24 MISO
20 SCS#/GPIO5
27 NC13
19 SCLK
13 GPIO4
17 PLTRST#
28 NC14
12 NC9
4 PP/GPIO6
3 NC4
30 SCL/GPIO1
29 SDA/GPIO0
6 GPIO3
5 NC5
2 NC1
7 NC6
10 NC7
11 NC8
25 NC11
26 NC12
31 NC15
PP
TP39
R974 X/0 5% R0201
PP1
TP59
NC2 GND1 GND2 NC3 GND3
9 16 23 32 33
14-O_D_I-NPCT750AABYX-0
R975 X/0 5% R0201
R976 X/0 5% R0201
Stuff R974/R975/R976
for Infineon TPM
P/N : 149SLB9670
<Variant Name>
AAEON Technology INC.
Title
SPI_TPM
Size
A
Document Number
EPIC-ADS7
Rev
A0.2_0_0
Date: Thursday, January 20, 2022
Sheet 25 of 57

To FPC x4



+V12S: 2.1A (Max)
+V3P3A: 0.375A(Max)
+V3P3S: 3A (Max)

+V12S: 2.1A (Max)
+V3.3A: 0.375A(Max)
+V3.3S: 3.0A (Max)

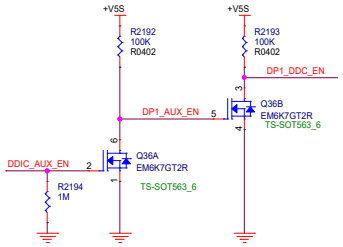


40,90D,FEMALE,52506-0400M-001,

<Core Design>

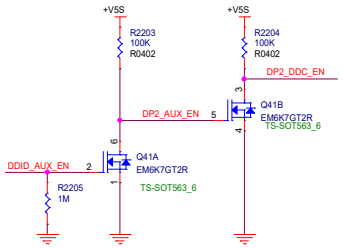
Title: **PCIe X 4 FPC**		
Size: A	Document Number: **EPIC-ADS7**	Rev: **A0.2_0_0**
Date: *Thursday, January 20, 2022*	Sheet: **26** of **57**	

DDIC/D to DP++



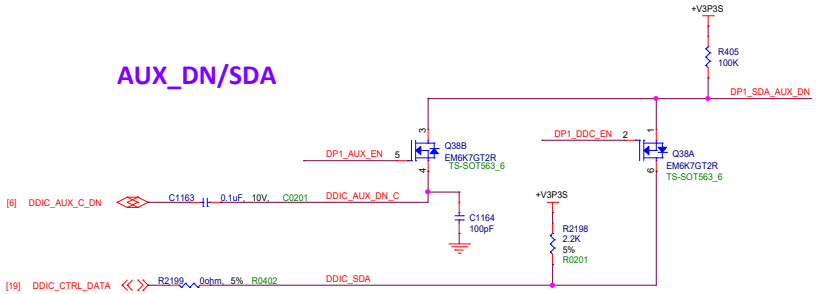
DDIC_AUX_EN	Type
High	HDMI dongle
Low	DP

A0.2

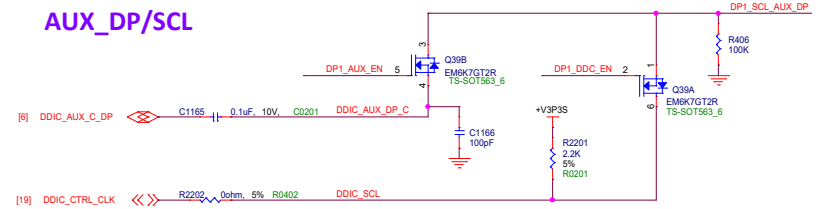


DDIC_AUX_EN	Type
High	HDMI dongle
Low	DP

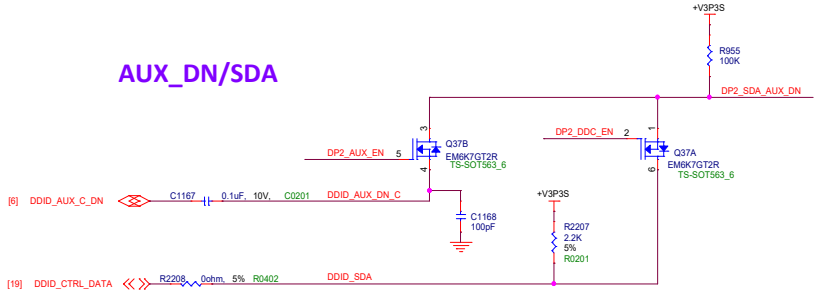
AUX_DN/SDA



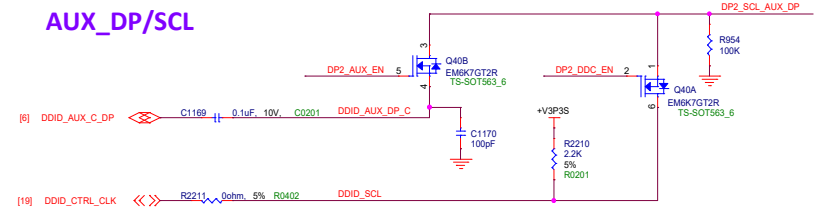
AUX_DP/SCL

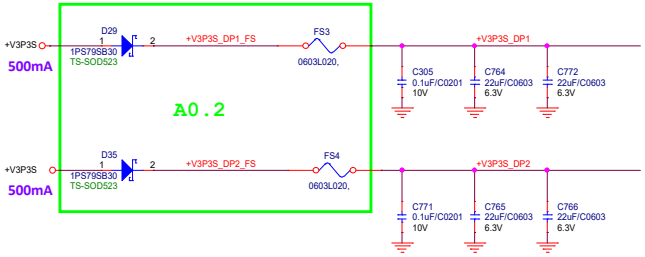


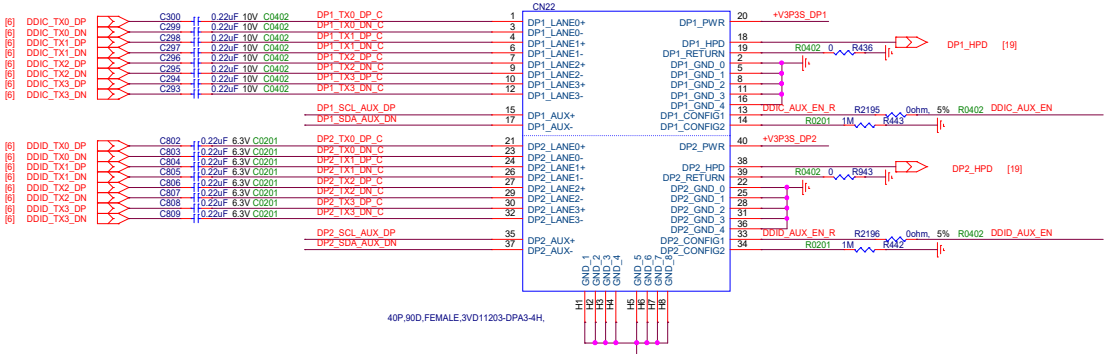
AUX_DN/SDA



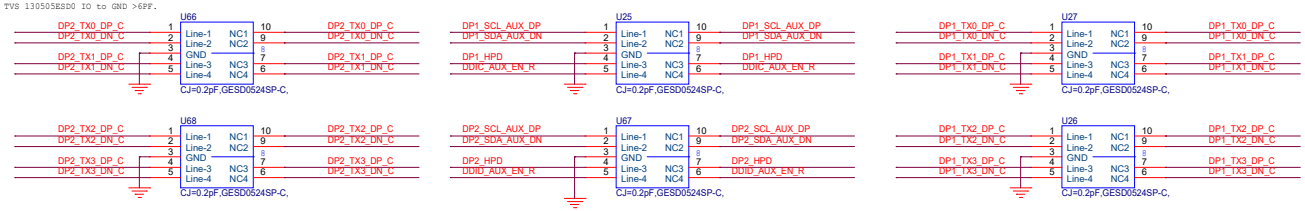
AUX_DP/SCL







TVS 130505ESD0 IO to GND >6PF.

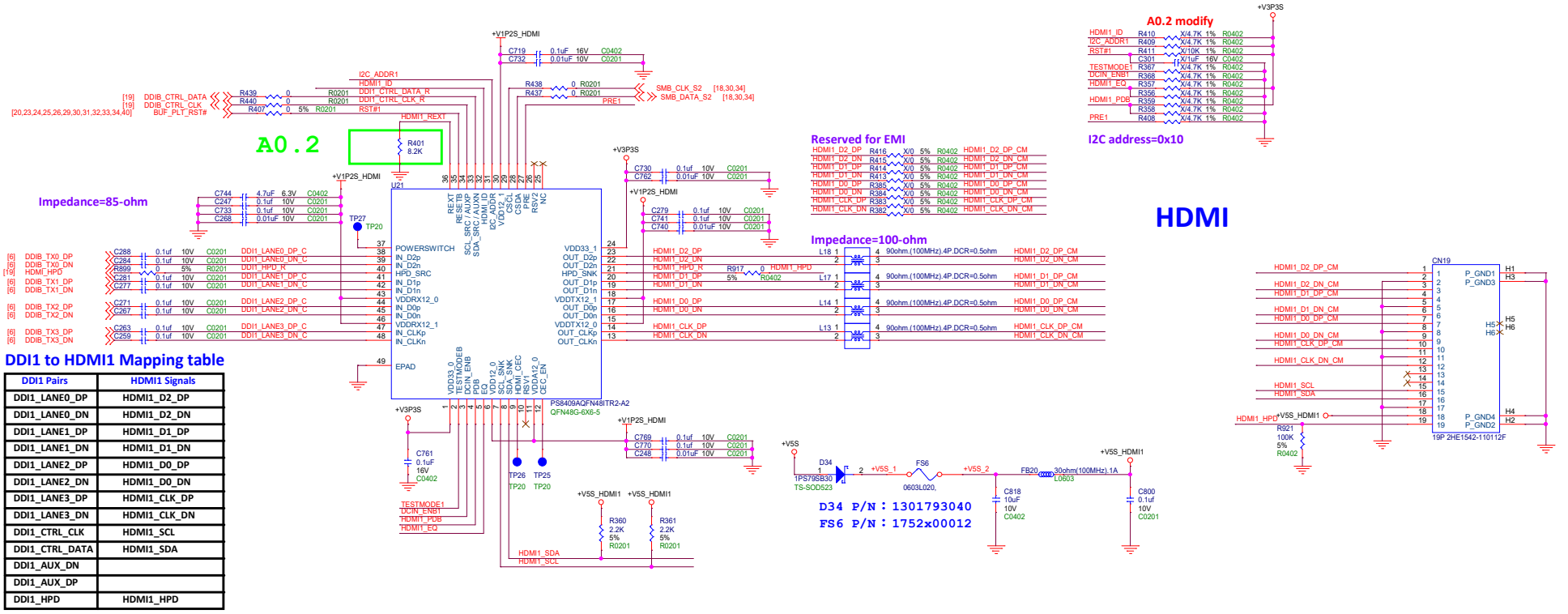


<Variant Name>

AAEON Technology INC.

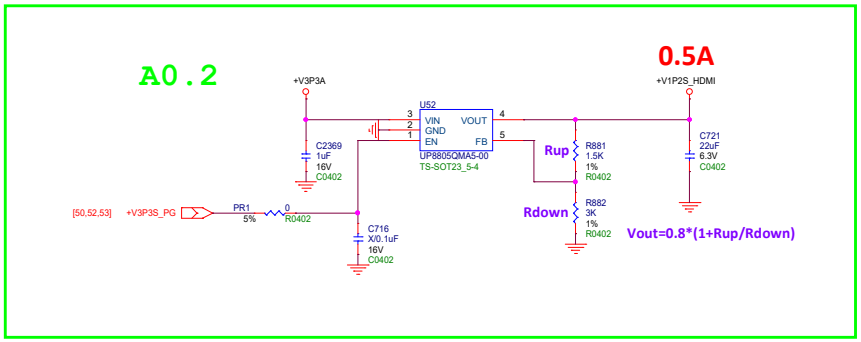
Title		
HDMI/DP2		
Size: C	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 27 of 57	

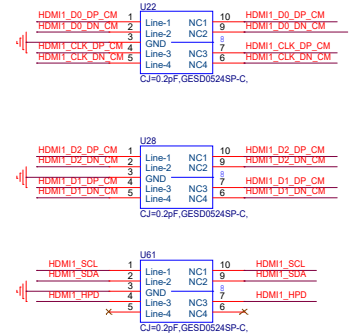
DDIB to HDMI1



DDI1 to HDMI1 Mapping table

DDI1 Pairs	HDMI1 Signals
DDI1_LANE0_DP	HDMI1_D2_DP
DDI1_LANE0_DN	HDMI1_D2_DN
DDI1_LANE1_DP	HDMI1_D1_DP
DDI1_LANE1_DN	HDMI1_D1_DN
DDI1_LANE2_DP	HDMI1_D0_DP
DDI1_LANE2_DN	HDMI1_D0_DN
DDI1_LANE3_DP	HDMI1_CLK_DP
DDI1_LANE3_DN	HDMI1_CLK_DN
DDI1_CTRL_CLK	HDMI1_SCL
DDI1_CTRL_DATA	HDMI1_SDA
DDI1_AUX_DN	
DDI1_AUX_DP	
DDI1_HPD	HDMI1_HPD

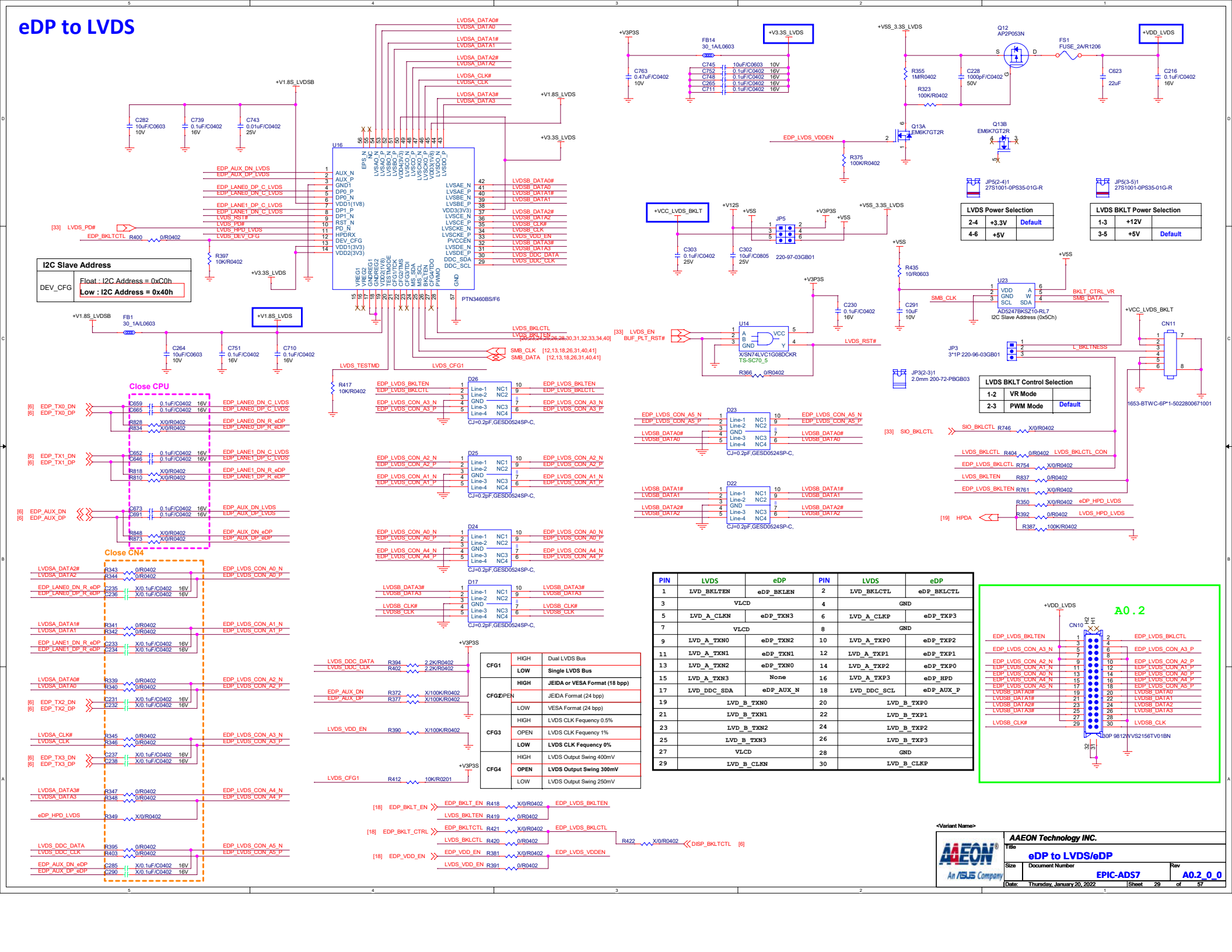




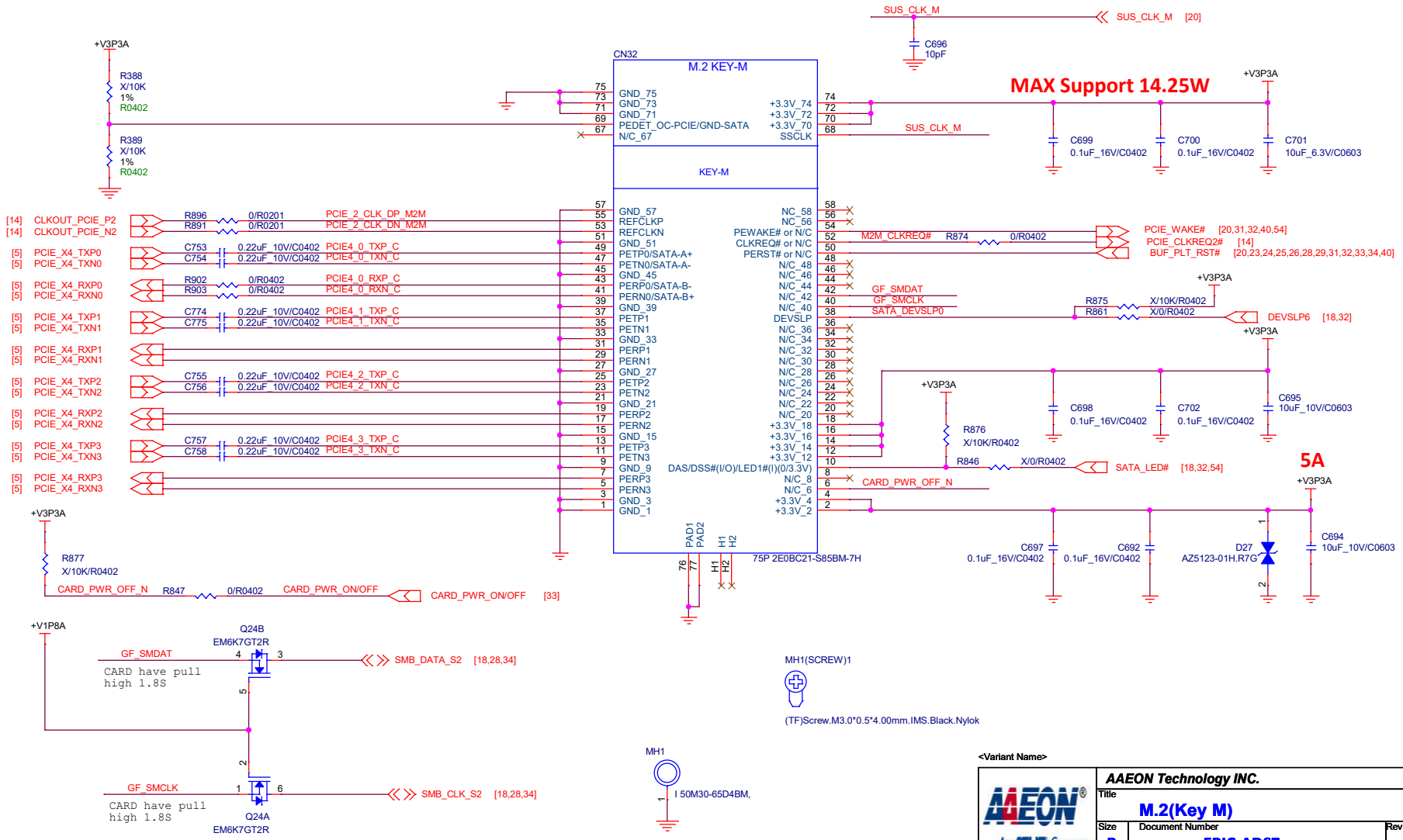
<Variant Name>

AAEON Technology INC.			
Title: HDMI			
Size	Document Number: EPIC-ADS7		Rev: A0.2_0_0
Date: Thursday, January 20, 2022		Sheet 28 of 57	

eDP to LVDS


I2C Slave Address
DEV_CFG
Float : I2C Address = 0xC0h
Low : I2C Address = 0x40h
PTN3460BS/F6
Close CPU
Close CN4
LVDS Power Selection
2-4 +3.3V Default
4-6 +5V
LVDS BKLT Power Selection
1-3 +12V
3-5 +5V Default
LVDS BKLT Control Selection
1-2 VR Mode
2-3 PWM Mode Default
CFG1 HIGH Dual LVDS Bus
LOW Single LVDS Bus
CFG2 HIGH JEIDA or VESA Format (18 bpp)
OPEN JEIDA Format (24 bpp)
LOW VESA Format (24 bpp)
CFG3 HIGH LVDS CLK Fequency 0.5%
OPEN LVDS CLK Fequency 1%
LOW LVDS CLK Fequency 0%
CFG4 HIGH LVDS Output Swing 400mV
OPEN LVDS Output Swing 300mV
LOW LVDS Output Swing 250mV
PIN LVDS eDP PIN LVDS eDP
1 LVD_BKLTEN eDP_BKLEN 2 LVD_BKLCTL eDP_BKLCTL
3 VLCD 4 GND
5 LVD_A_CLKN eDP_TXN3 6 LVD_A_CLKP eDP_TXP3
7 VLCD 8 GND
9 LVD_A_TXN0 eDP_TXN2 10 LVD_A_TXP0 eDP_TXP2
11 LVD_A_TXN1 eDP_TXN1 12 LVD_A_TXP1 eDP_TXP1
13 LVD_A_TXN2 eDP_TXN0 14 LVD_A_TXP2 eDP_TXP0
15 LVD_A_TXN3 None 16 LVD_A_TXP3 eDP_HPD
17 LVD_DDC_SDA eDP_AUX_N 18 LVD_DDC_SCL eDP_AUX_P
19 LVD_B_TXN0 20 LVD_B_TXP0
21 LVD_B_TXN1 22 LVD_B_TXP1
23 LVD_B_TXN2 24 LVD_B_TXP2
25 LVD_B_TXN3 26 LVD_B_TXP3
27 VLCD 28 GND
29 LVD_B_CLKN 30 LVD_B_CLKP
A0.2
Variant Name
AAEON Technology INC.
Title
eDP to LVDS/eDP
Size
Document Number
EPIC-ADS7
Rev
A0.2_0_0
Date: Thursday, January 20, 2022
Sheet 29 of 57

M.2(Key M)



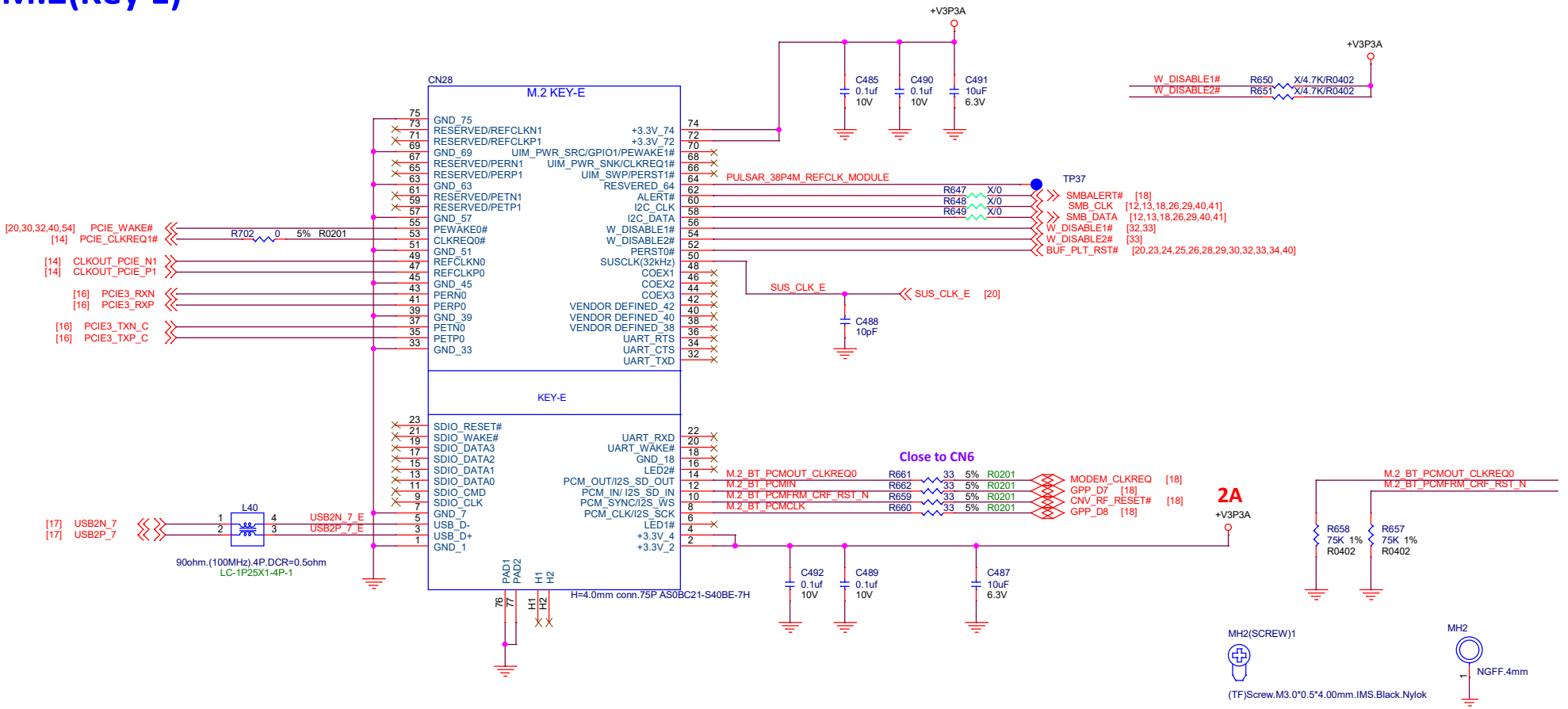
<Variant Name>

AAEON Technology INC.

An ASUS Company

Title	M.2(Key M)		
Size	Document Number		Rev
B	EPIC-ADS7		A0.2_0_0
Date:	Thursday, January 20, 2022	Sheet 30 of 57	

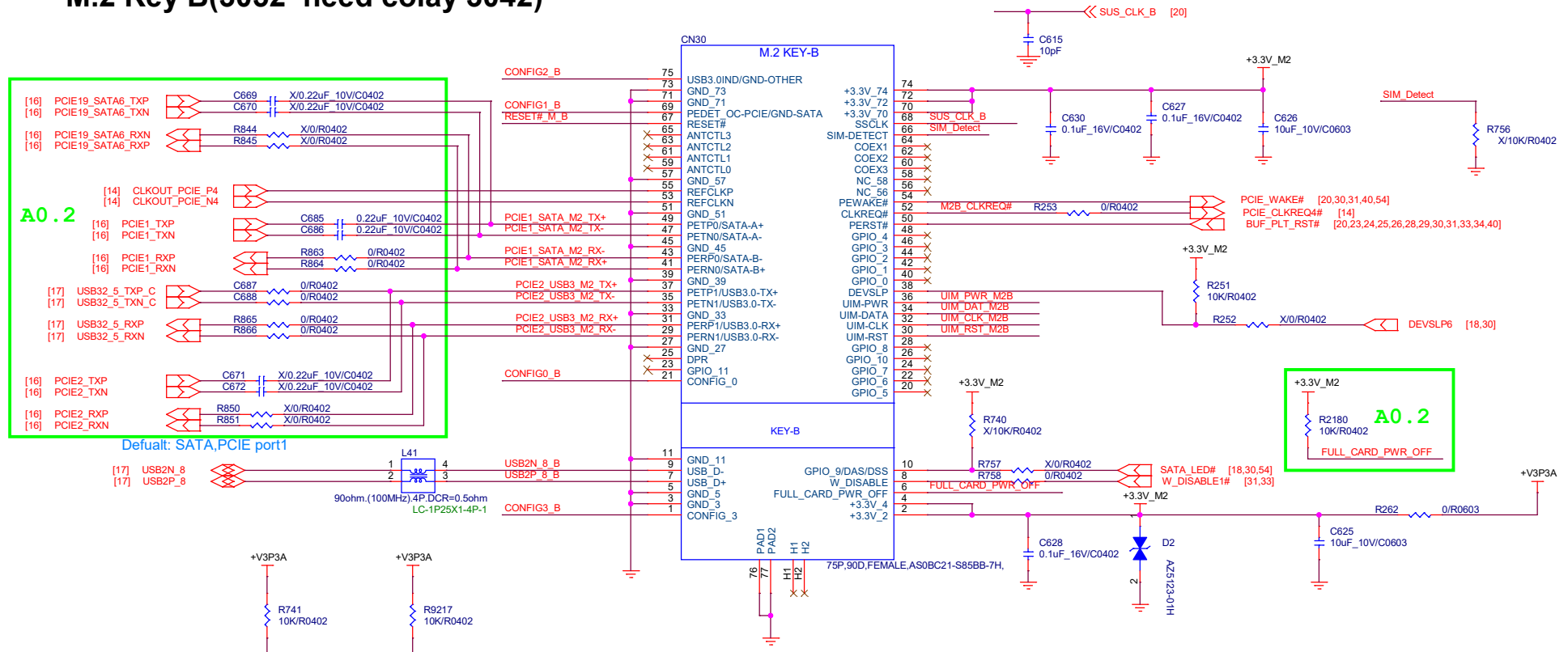
M.2(Key E)



<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.		
	Title: M.2(Key E)		
	Size: B	Document Number: EPIC-ADS7	Rev: A0.2_0_0
	Date: Thursday, January 20, 2022	Sheet 31 of 57	

M.2 Key B(3052 need colay 3042)

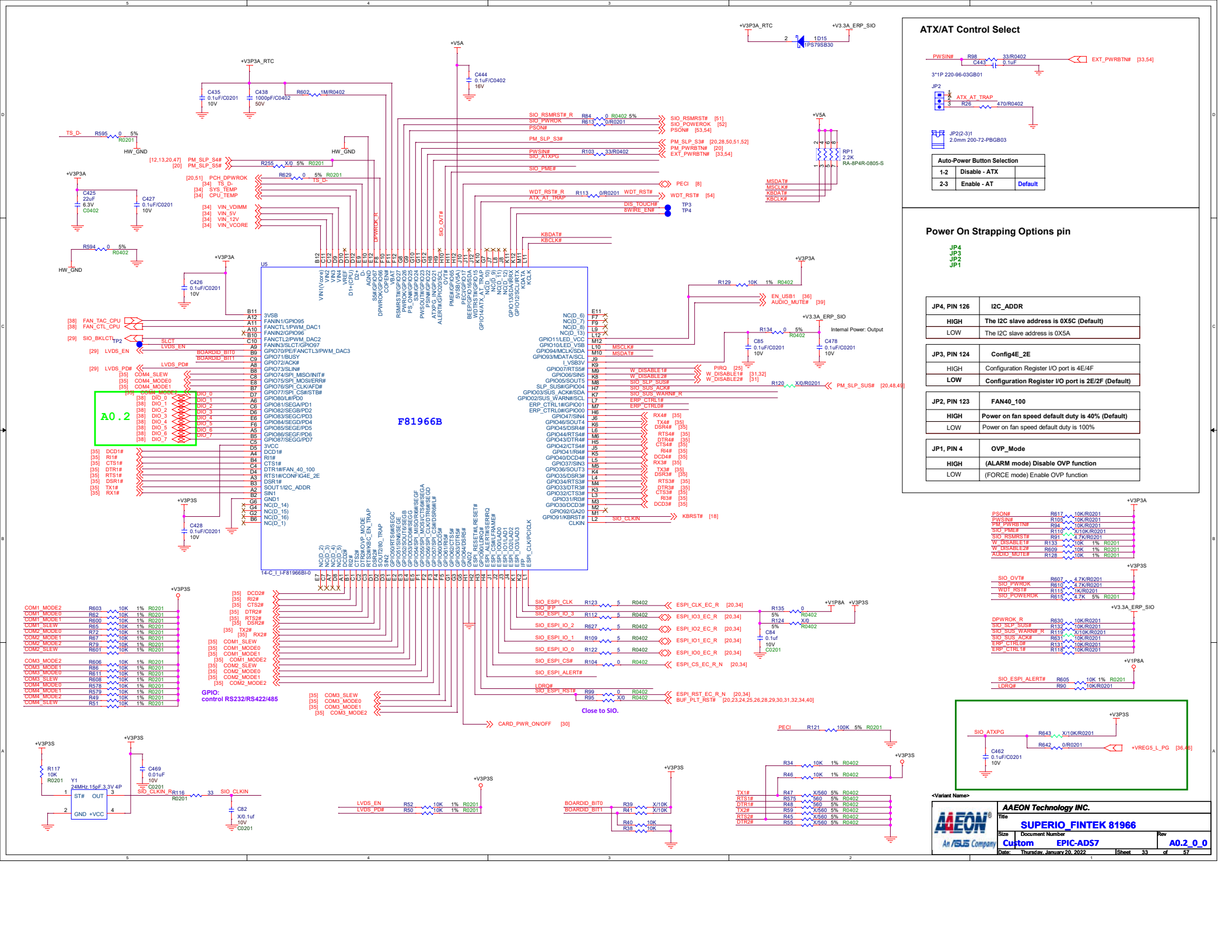


CONFIG 0	1	2	3	Type	Port Config
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIE	N/A
0	0	1	0	WWAN - PCIe	0
0	1	1	0	WWAN - PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3

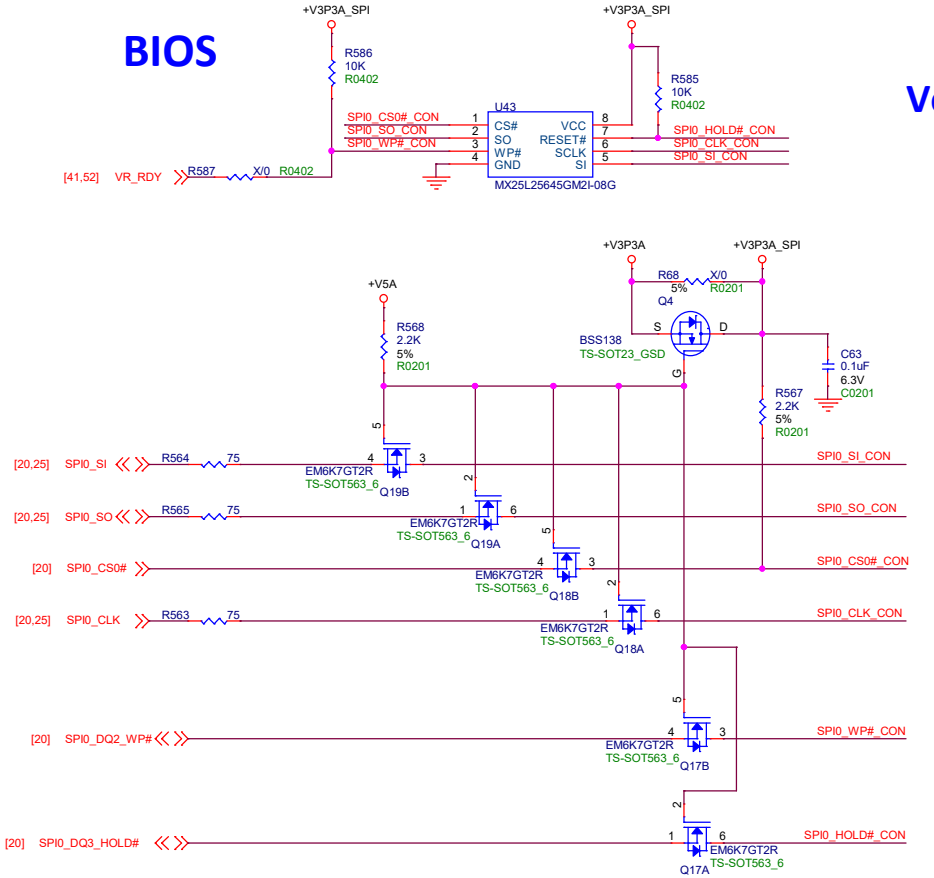
<Variant Name>

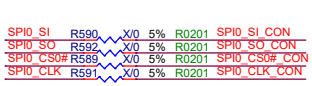
AAEON Technology INC.

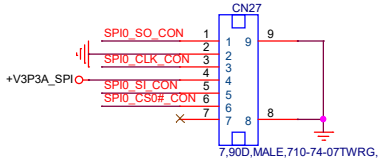
Title: M.2 B-KEY		
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 32 of 57	


ATX/AT Control Select
PWSIN#
R98
33/R0402
C443
0.1uF
EXT_PWRBTN# [33,54]
3*1P 220-96-03GB01
JP2
ATX_AT_TRAP
R26
470/R0402
JP2(2-3)1
2.0mm 200-72-PBGB03
Auto-Power Button Selection
1-2 Disable - ATX
2-3 Enable - AT Default
Power On Strapping Options pin
JP4
JP3
JP2
JP1
JP4, PIN 126 I2C_ADDR
HIGH The I2C slave address is 0X5C (Default)
LOW The I2C slave address is 0X5A
JP3, PIN 124 Config4E_2E
HIGH Configuration Register I/O port is 4E/4F
LOW Configuration Register I/O port is 2E/2F (Default)
JP2, PIN 123 FAN40_100
HIGH Power on fan speed default duty is 40% (Default)
LOW Power on fan speed default duty is 100%
JP1, PIN 4 OVP_Mode
HIGH (ALARM mode) Disable OVP function
LOW (FORCE mode) Enable OVP function
A0.2
F81966B
14-C_I_I-F81966BI-0
GPIO:
control RS232/RS422/485
Close to SIO.
AAEON Technology INC.
SUPERIO_FINTEK 81966
Custom
EPIC-ADS7
A0.2_0_0
Date: Thursday, January 20, 2022
Sheet 33 of 57

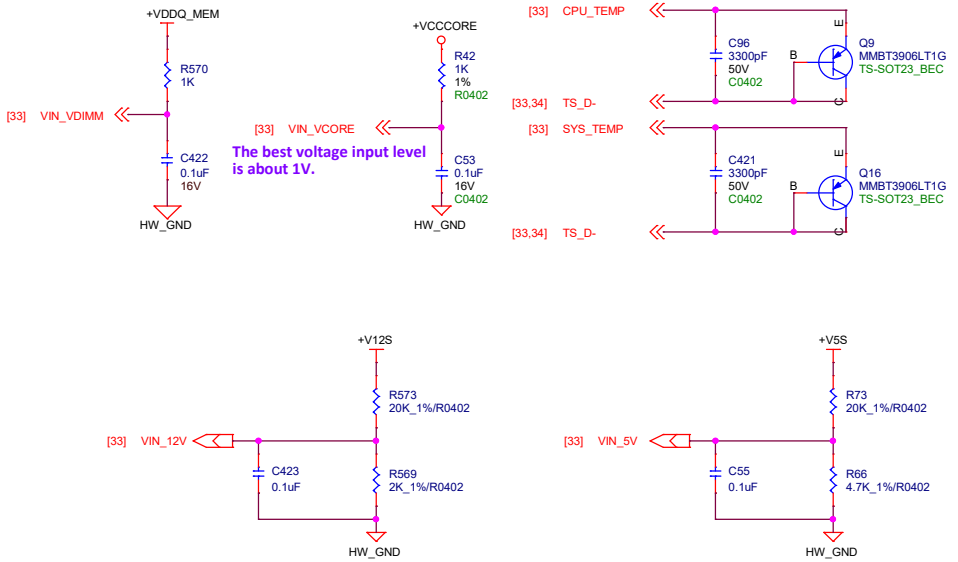
BIOS



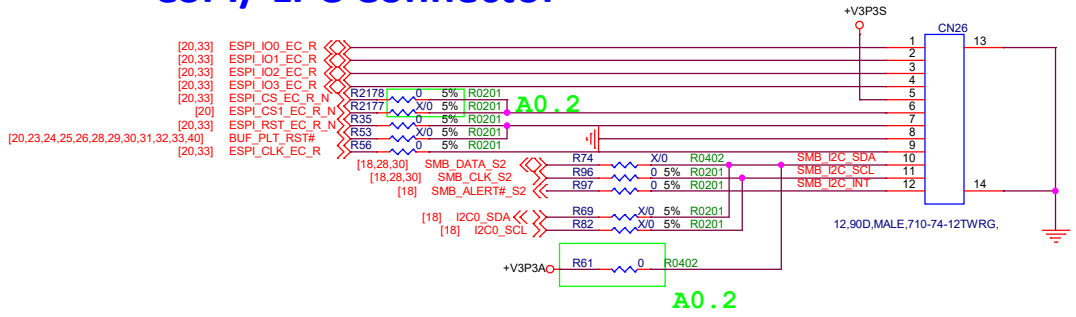




Voltage Monitor(Vcore, Vmem) Temperature Monitor(CPU, SYS)



eSPI/ LPC Connector



<Variant Name>

AAEON Technology INC.

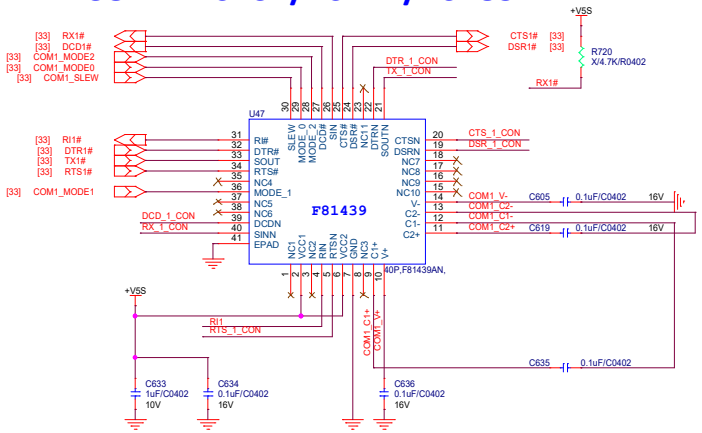
Title: BIOS/ LPC/ HW Monitor

Size	Document Number	Rev
Custom	EPIC-ADS7	A0.2_0_0

Date: Thursday, January 20, 2022 Sheet 34 of 57

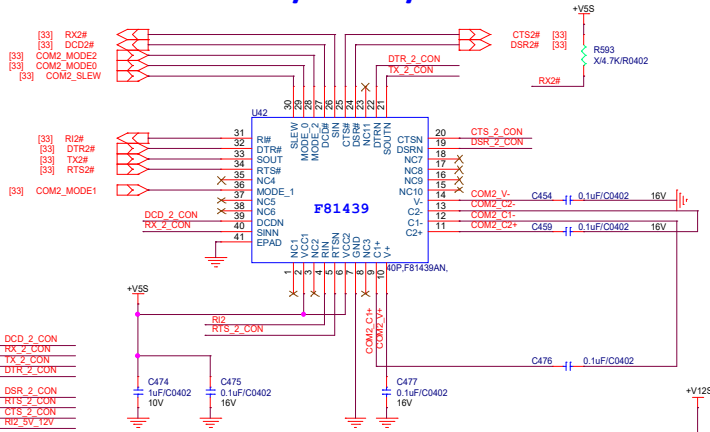
COM1

COM1-RS232/RS422/RS485

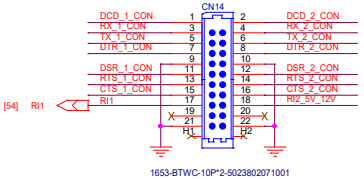


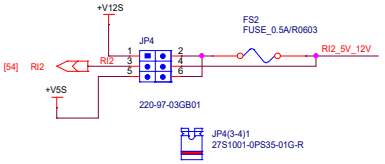
COM2

COM2-RS232/RS422/RS485



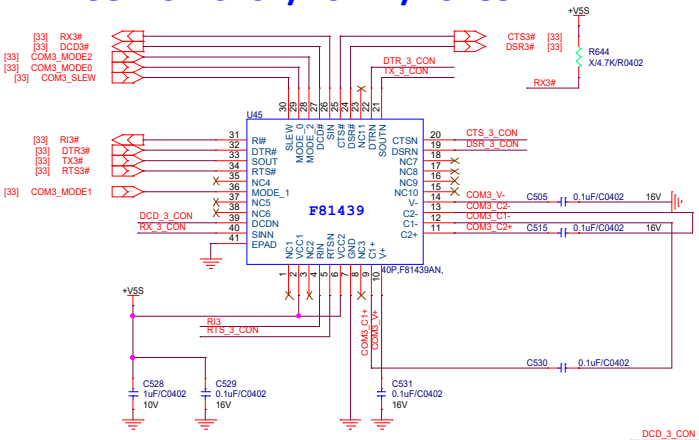
COM2 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

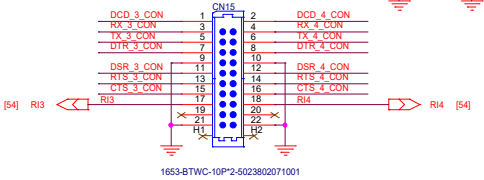




COM3

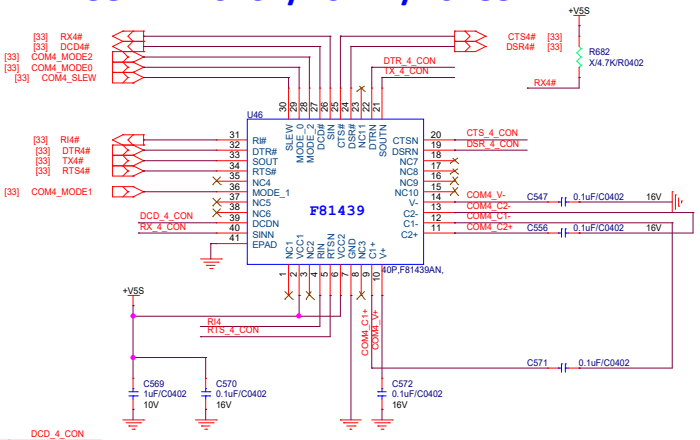
COM3-RS232/RS422/RS485





COM4

COM4-RS232/RS422/RS485



Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

Pin Mapping			
	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

<Variant Name>

AAEON Technology INC.

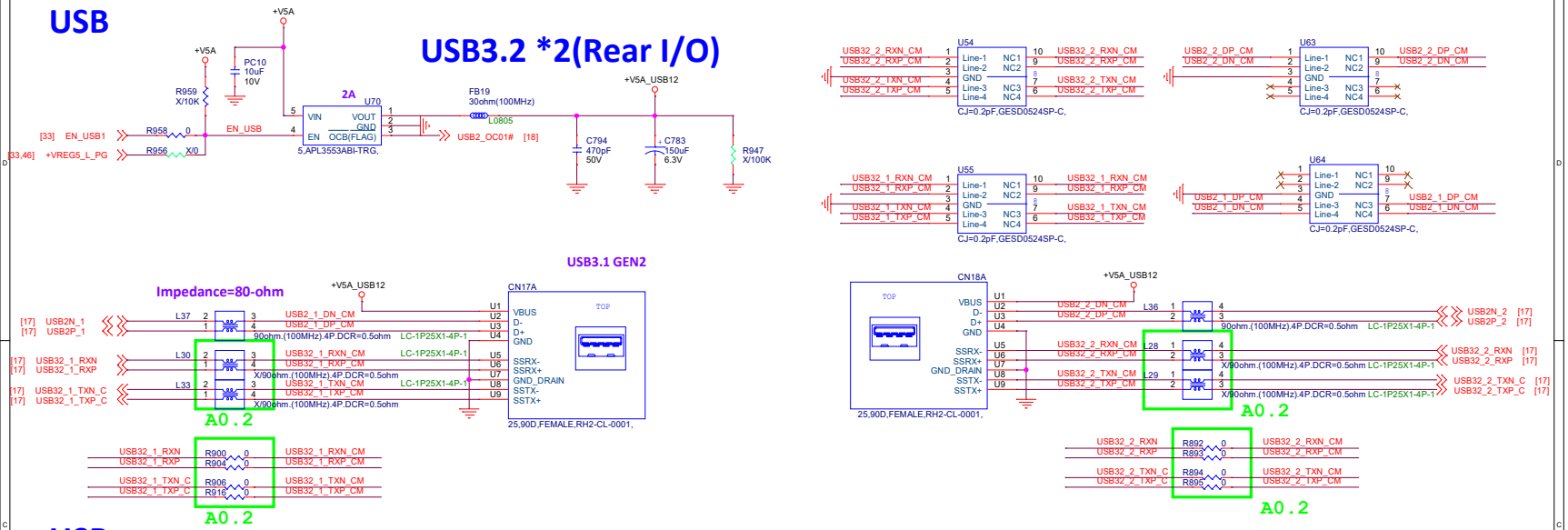
Title: COM1~COM4

Size: Custom | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

Date: Thursday, January 20, 2022 | Sheet 35 of 57

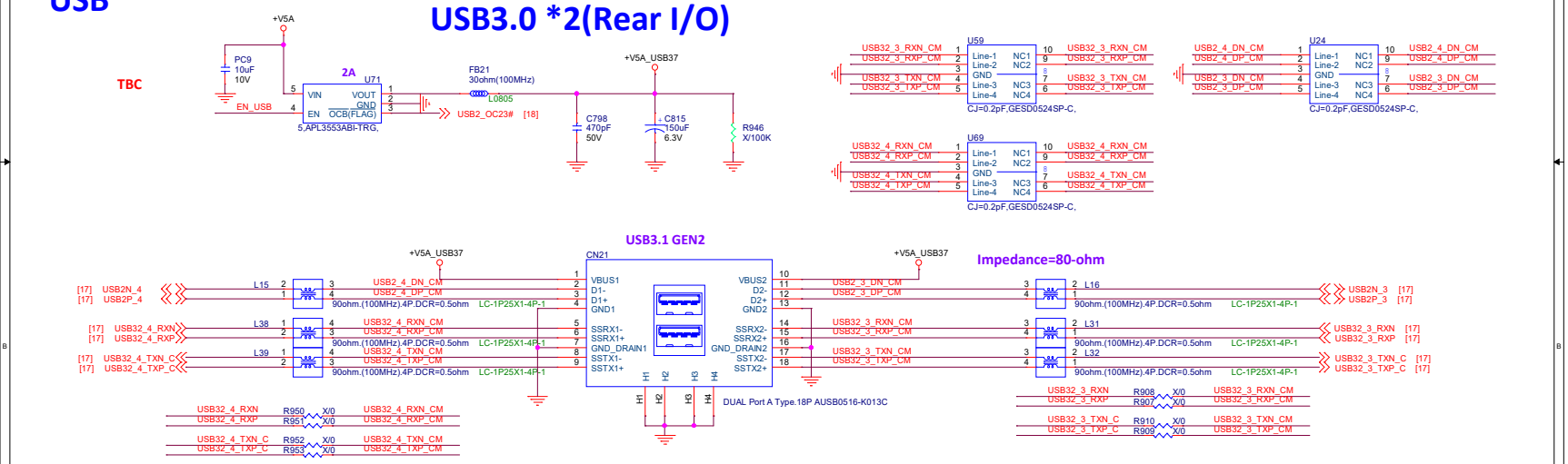
USB

USB3.2 *2(Rear I/O)

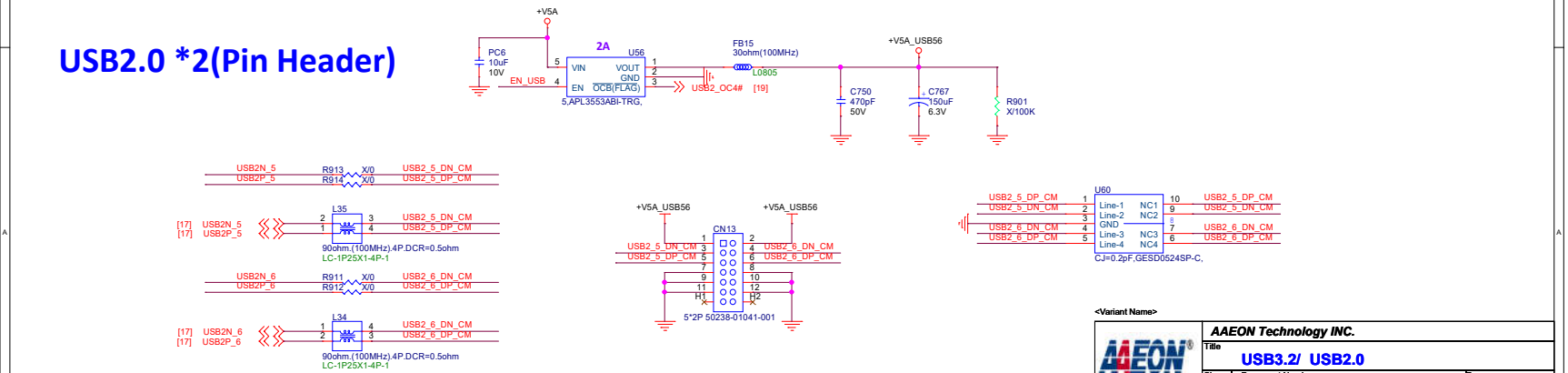


USB

USB3.0 *2(Rear I/O)



USB2.0 *2(Pin Header)

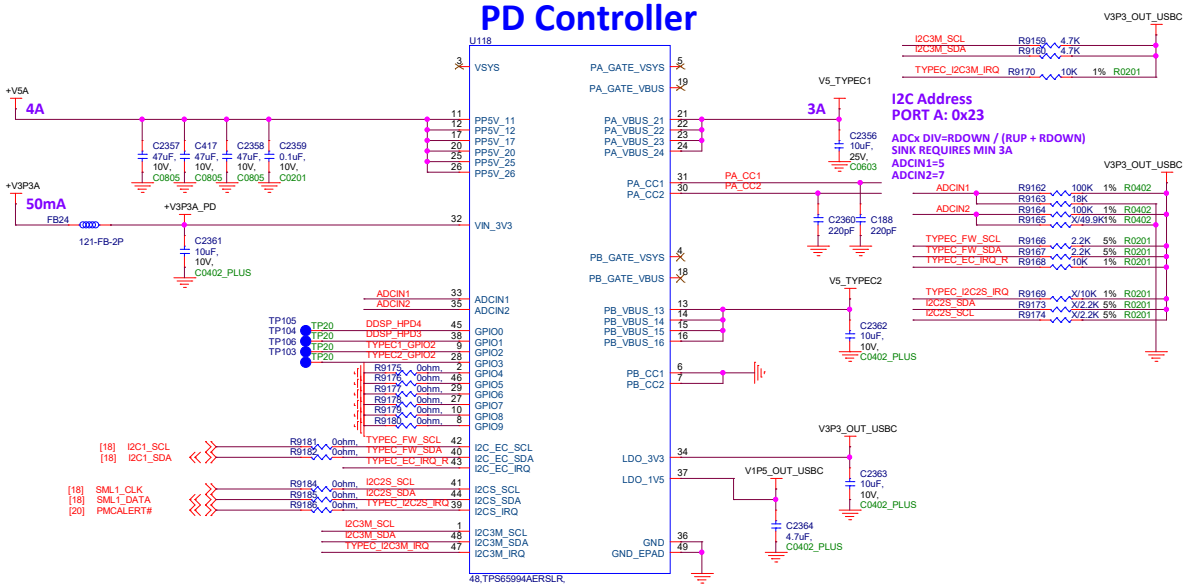


<Variant Name>

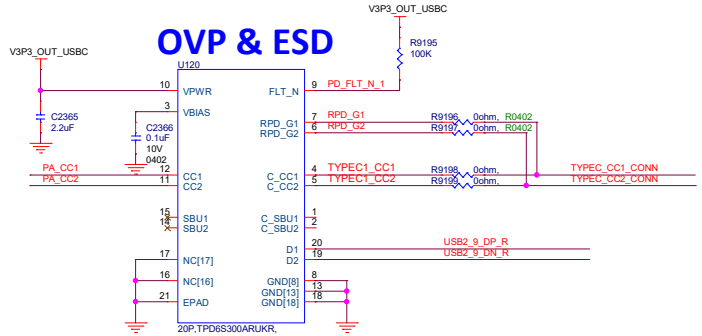
AAEON Technology INC.

Title	USB3.2/ USB2.0		
Size	Document Number		Rev
Custom	EPIC-ADS7		A0.2_0_0
Date:	Thursday, January 20, 2022	Sheet 36	of 57

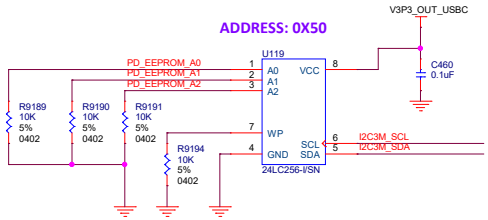
PD Controller

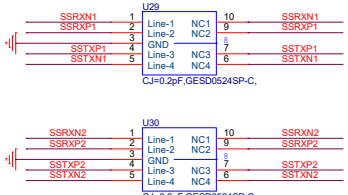


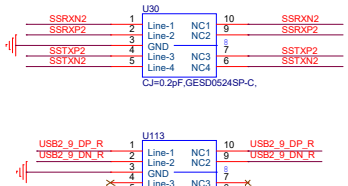
OVP & ESD

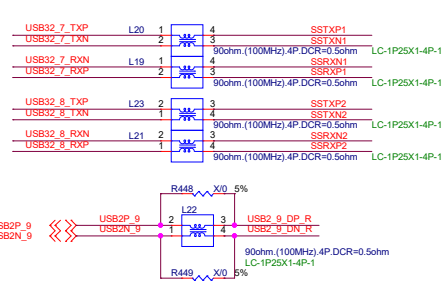


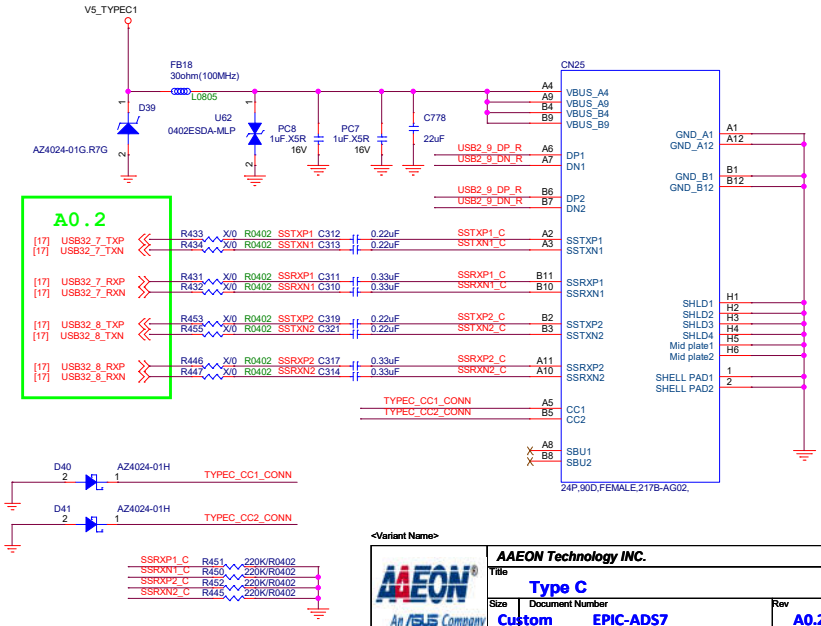
ADDRESS: 0X50











<Variant Name>

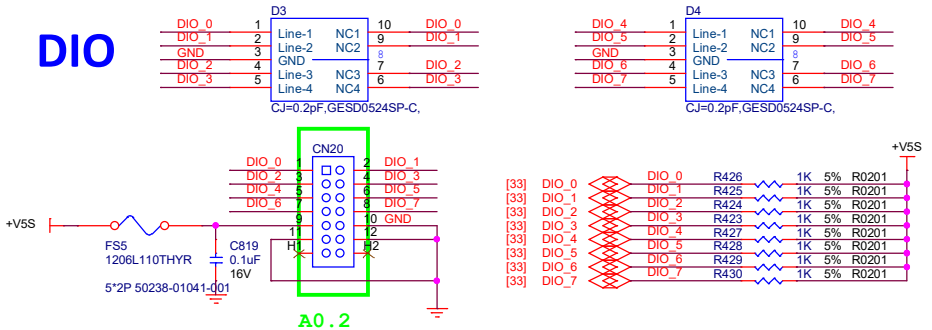
AAEON Technology INC.

Title: Type C

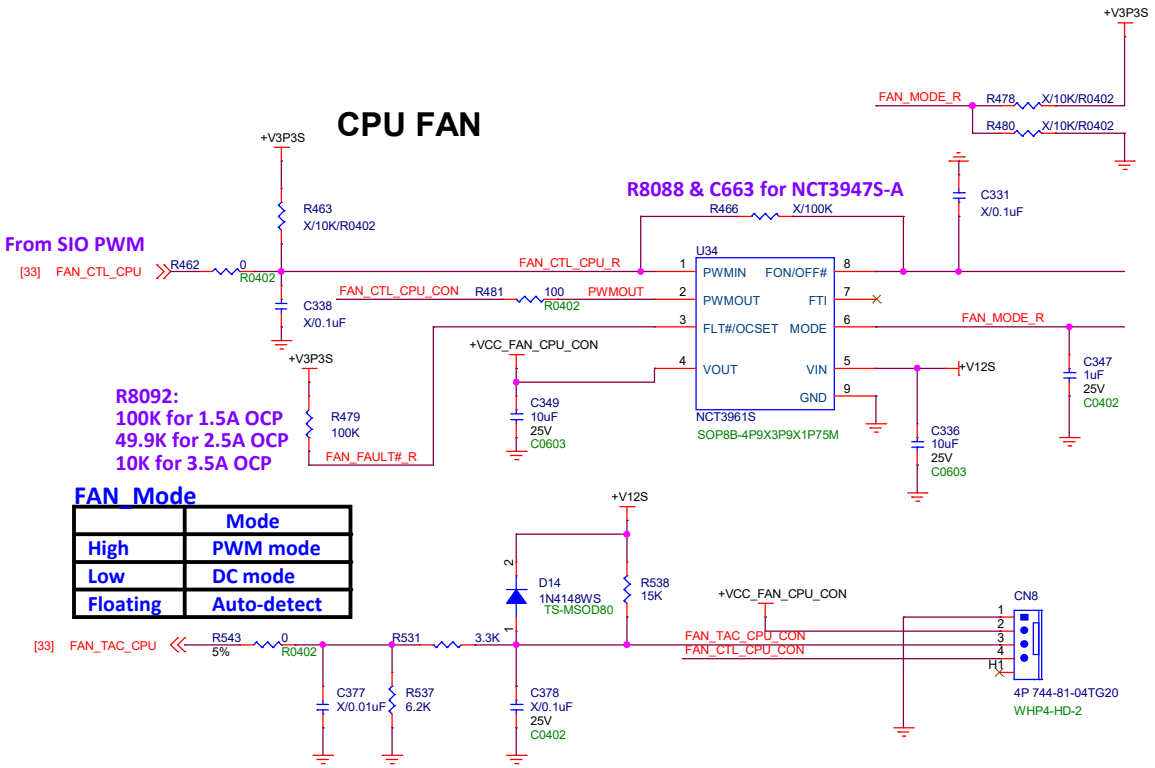
Size	Document Number	Rev
Custom	EPIC-ADS7	A0.2_0_0

Date: Thursday, January 20, 2022 Sheet 37 of 57

DIO



CPU FAN

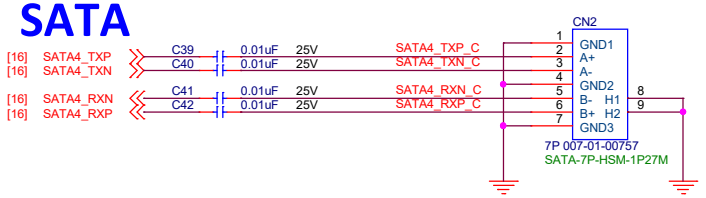


FAN_Mode

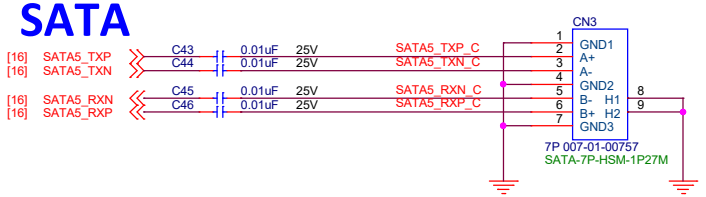
	Mode
High	PWM mode
Low	DC mode
Floating	Auto-detect

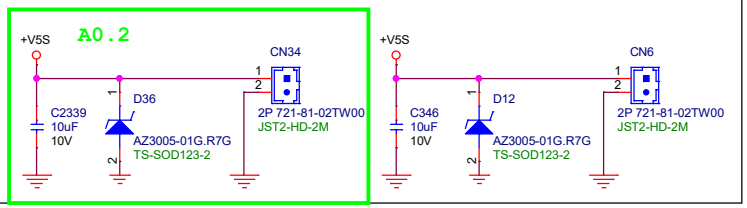
4P: 1655004018 (TF)WAFER.4P.180D(M).DIP.2.54mm.W/LOCK.PINREX.744-81-04TG20

SATA



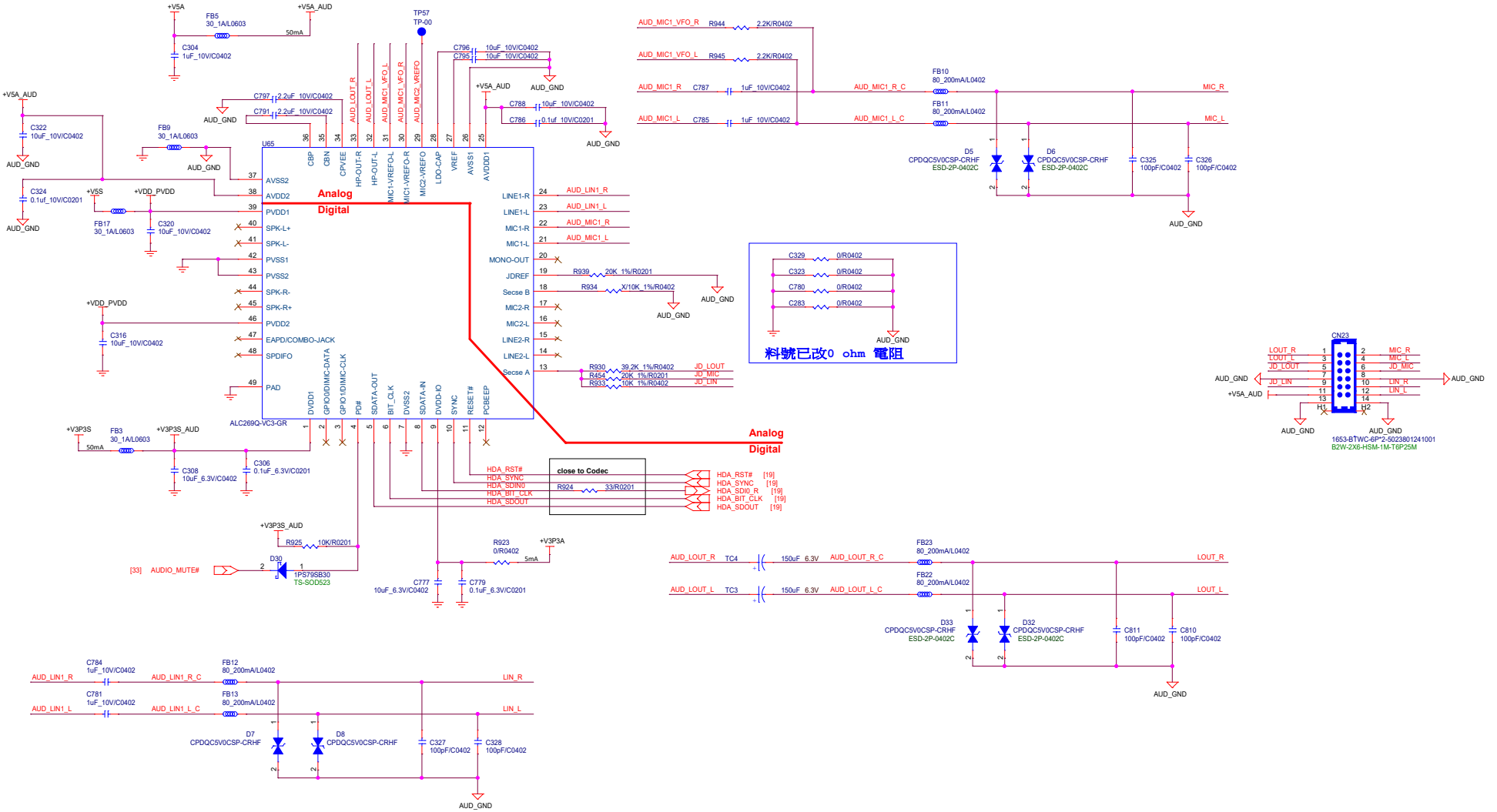
SATA





<Variant Name>

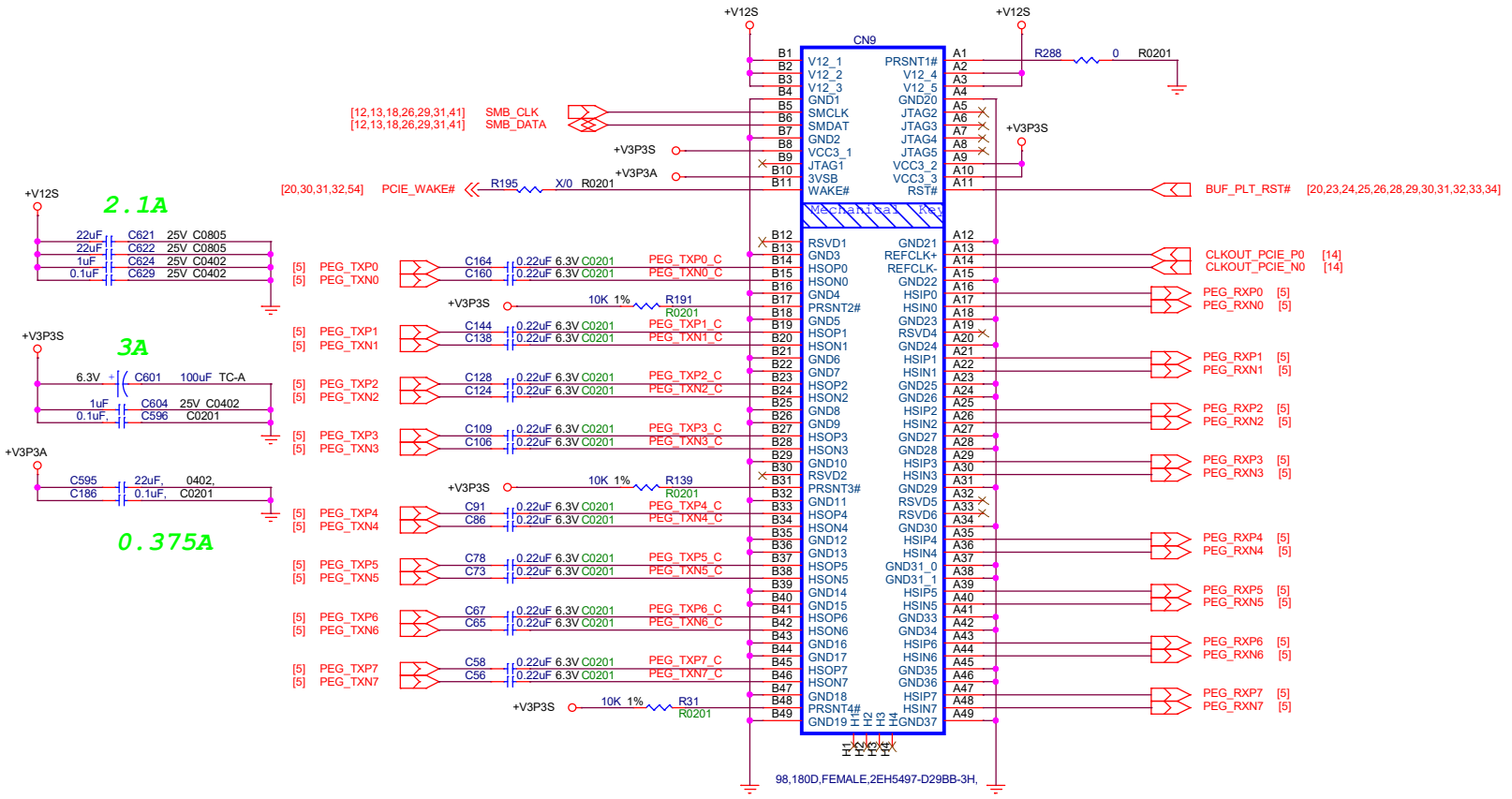
AAEON Technology INC.			
Title: SATA/DIO			
Size: B	Document Number: EPIC-ADS7		Rev: A0.2_0_0
Date: Thursday, January 20, 2022		Sheet 38 of 57	



<Variant Name>

AAEON Technology INC.

Title	Audio/Amp	
Size	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 39 of 57	



<Variant Name>

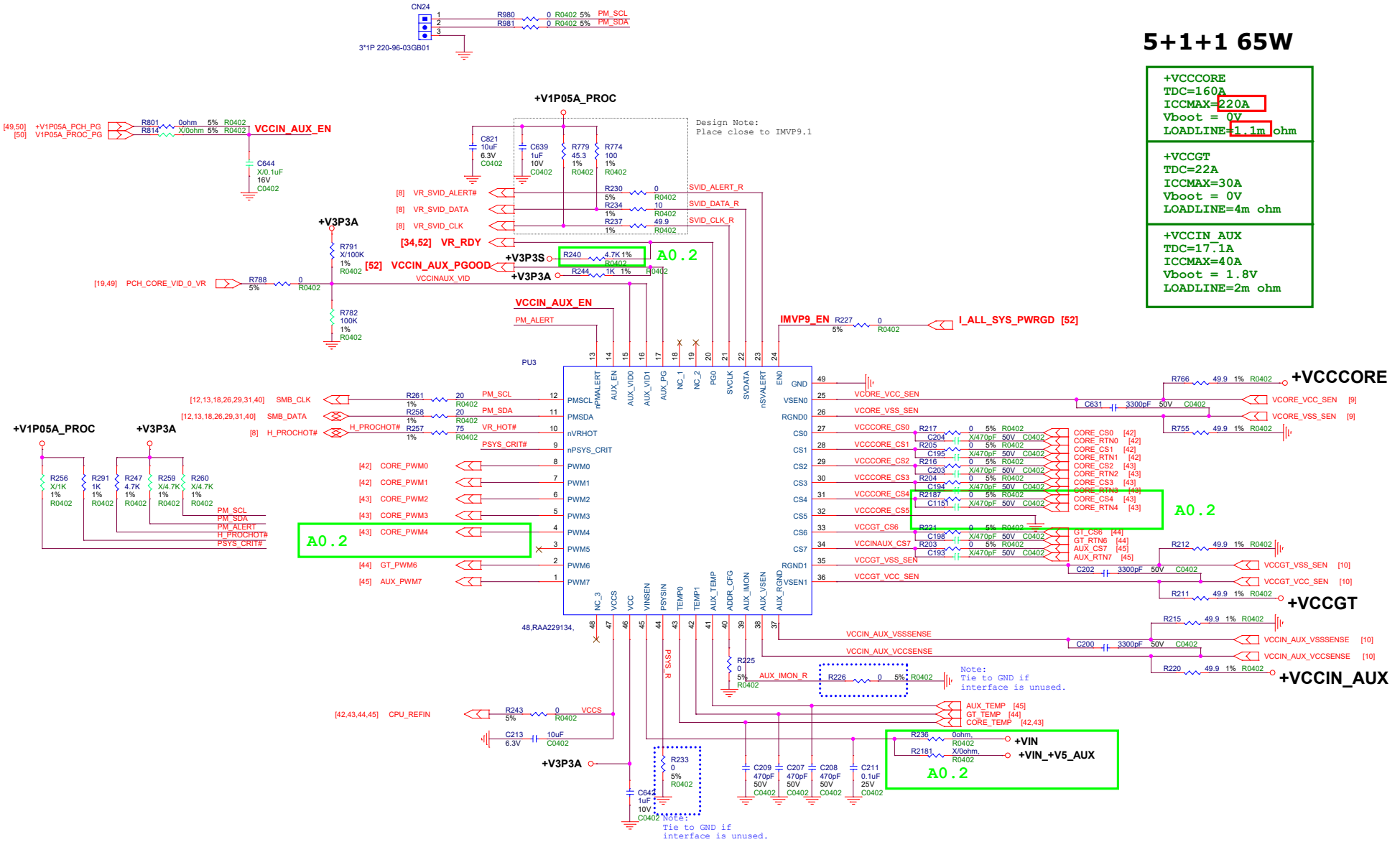
AAEON Technology INC.

Title: PCIE X8

Size | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

Date: Thursday, January 20, 2022 | Sheet 40 of 57

PWR_IMVP9.1@Total_220A

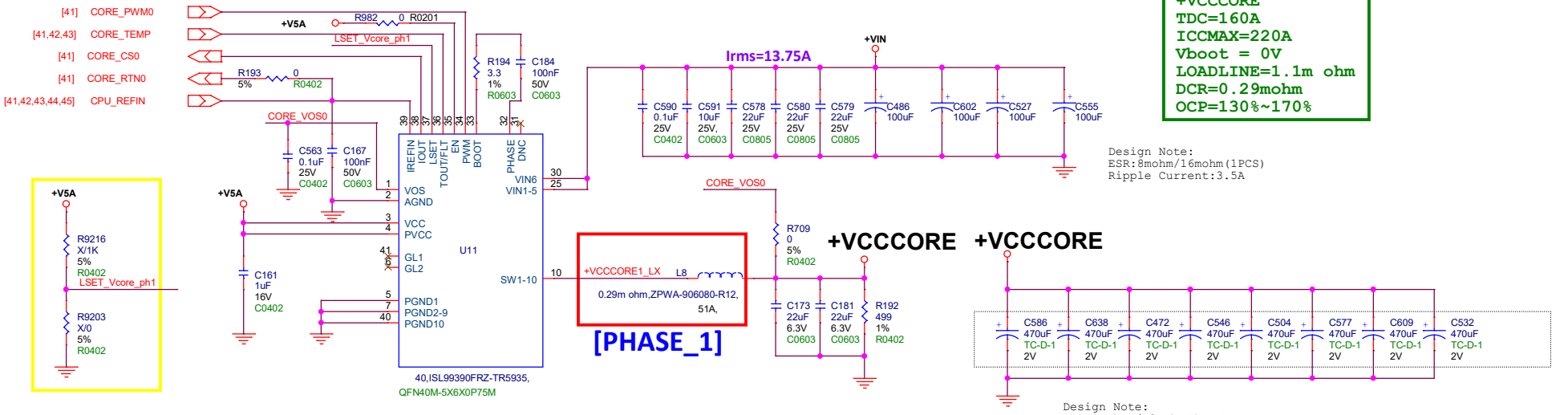


<Variant Name>

AAEON Technology INC.

Title	PWR_IMVP9 Controller	
Size: Custom	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 41 of 57	

PWR_+VCCCORE_Phase1/2

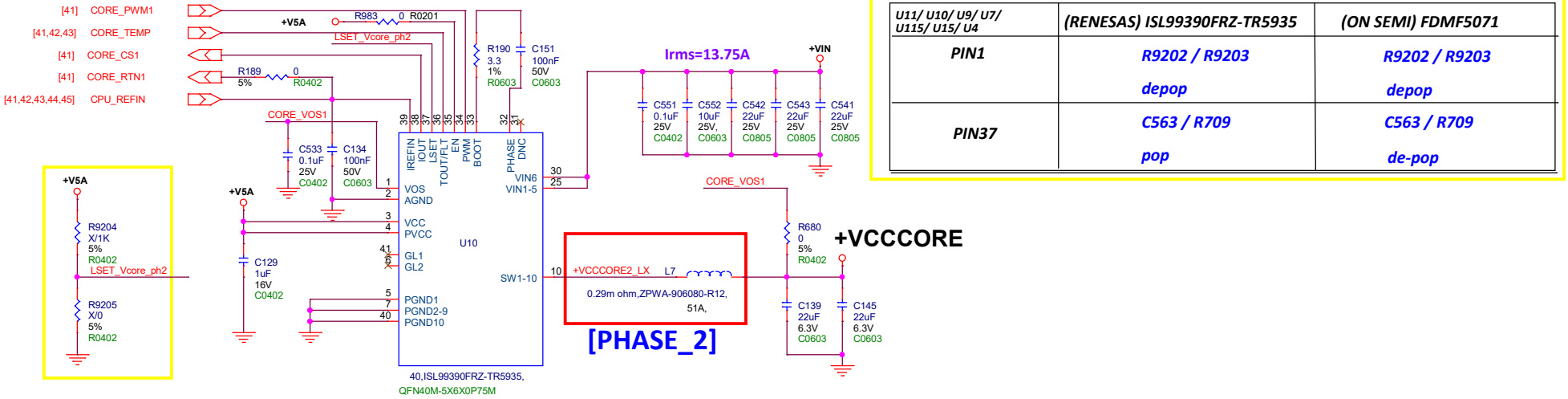


+VCCCORE
TDC=160A
ICCMAX=220A
Vboot = 0V
LOADLINE=1.1m ohm
DCR=0.29mohm
OCP=130%~170%

Design Note:
ESR:8mohm/16mohm(1PCS)
Ripple Current:3.5A

Design Note:
ESR:1mohm / 9mohm(1PCS)
Ripple Current:3A

8 PCS 470uF OSCON OR SP



U11/ U10/ U9/ U7/ U115/ U15/ U4	(RENESAS) ISL99390FRZ-TR5935	(ON SEMI) FDMF5071
PIN1	R9202 / R9203 depop	R9202 / R9203 depop
PIN37	C563 / R709 pop	C563 / R709 de-pop

<Variant Name>

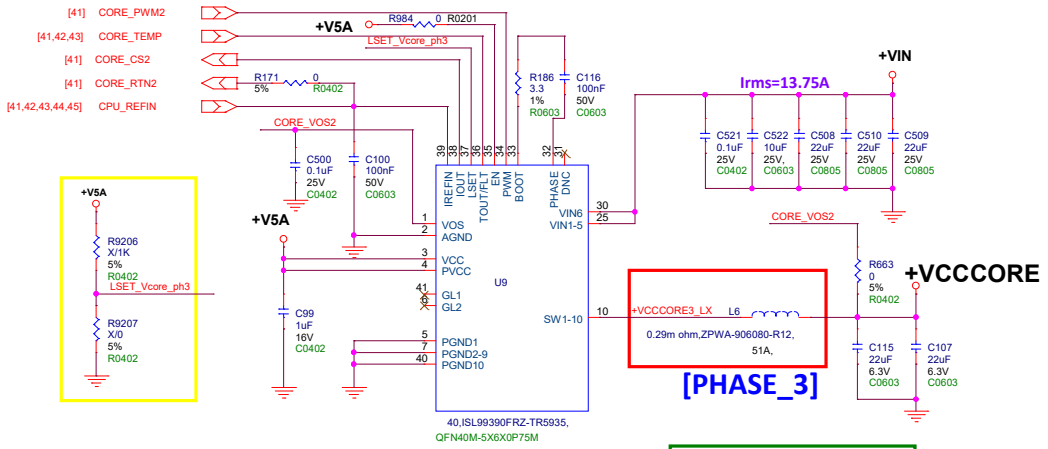
AAEON Technology INC.

Title: PWR_+VCCCORE

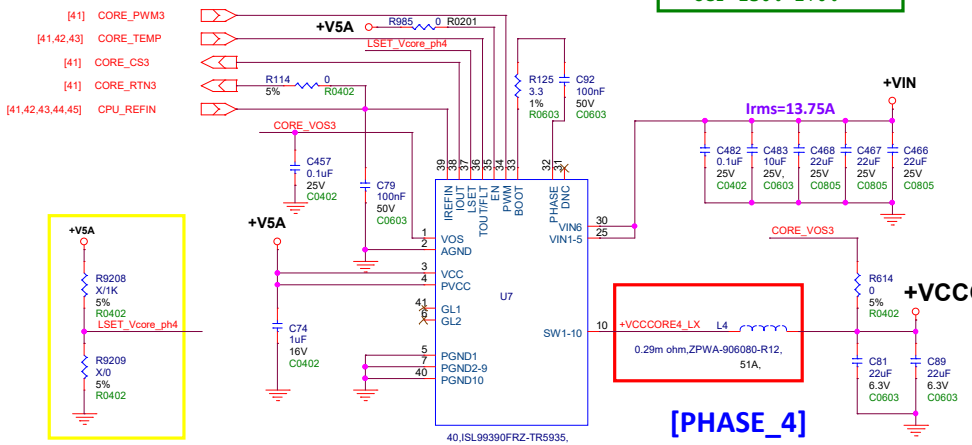
Size: Custom | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

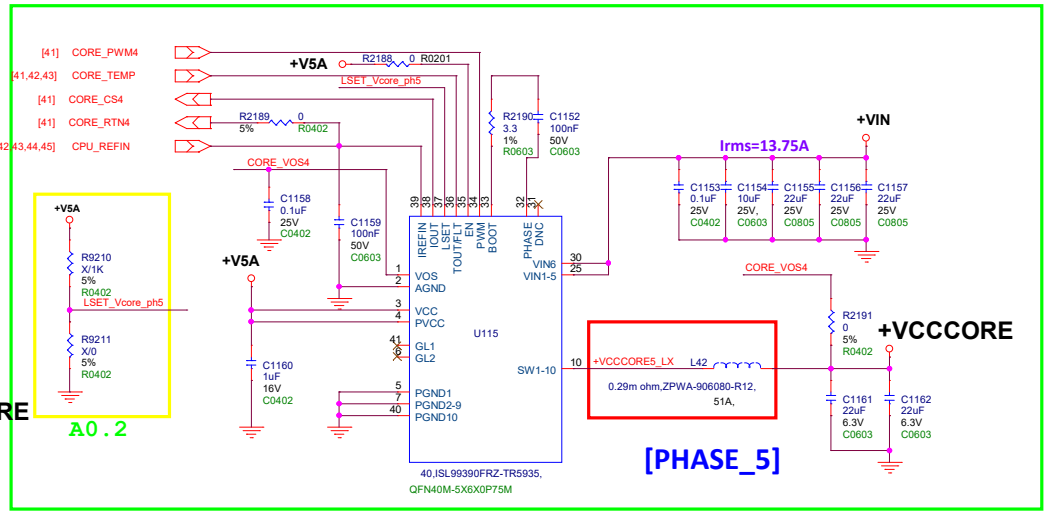
Date: Thursday, January 20, 2022 | Sheet 42 of 57

PWR_+VCCCORE_Phase3/4/5



+VCCCORE
TDC=160A
ICCMAX=220A
Vboot = 0V
LOADLINE=1.1m ohm
DCR=0.29mohm
OCP=130%~170%



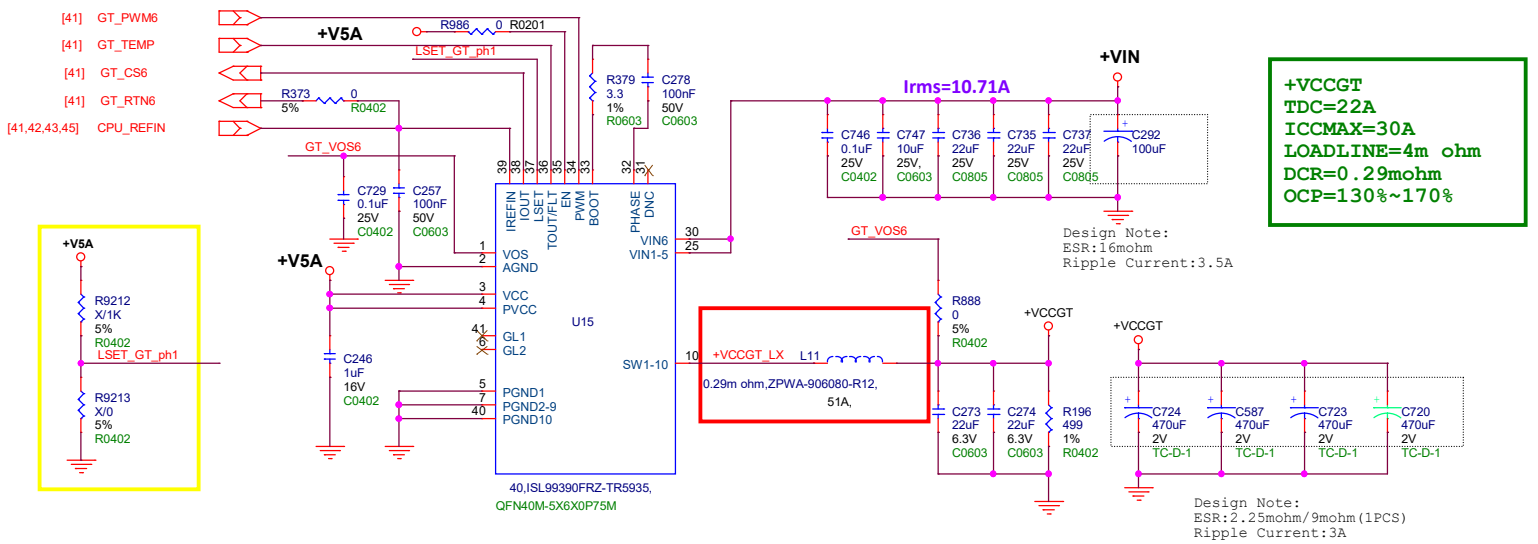


<Variant Name>

AAEON Technology INC.

Title	PWR_+VCCCORE_Phase3/4	
Size: Custom	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 43 of 57	

PWR_+VCCGT@30A



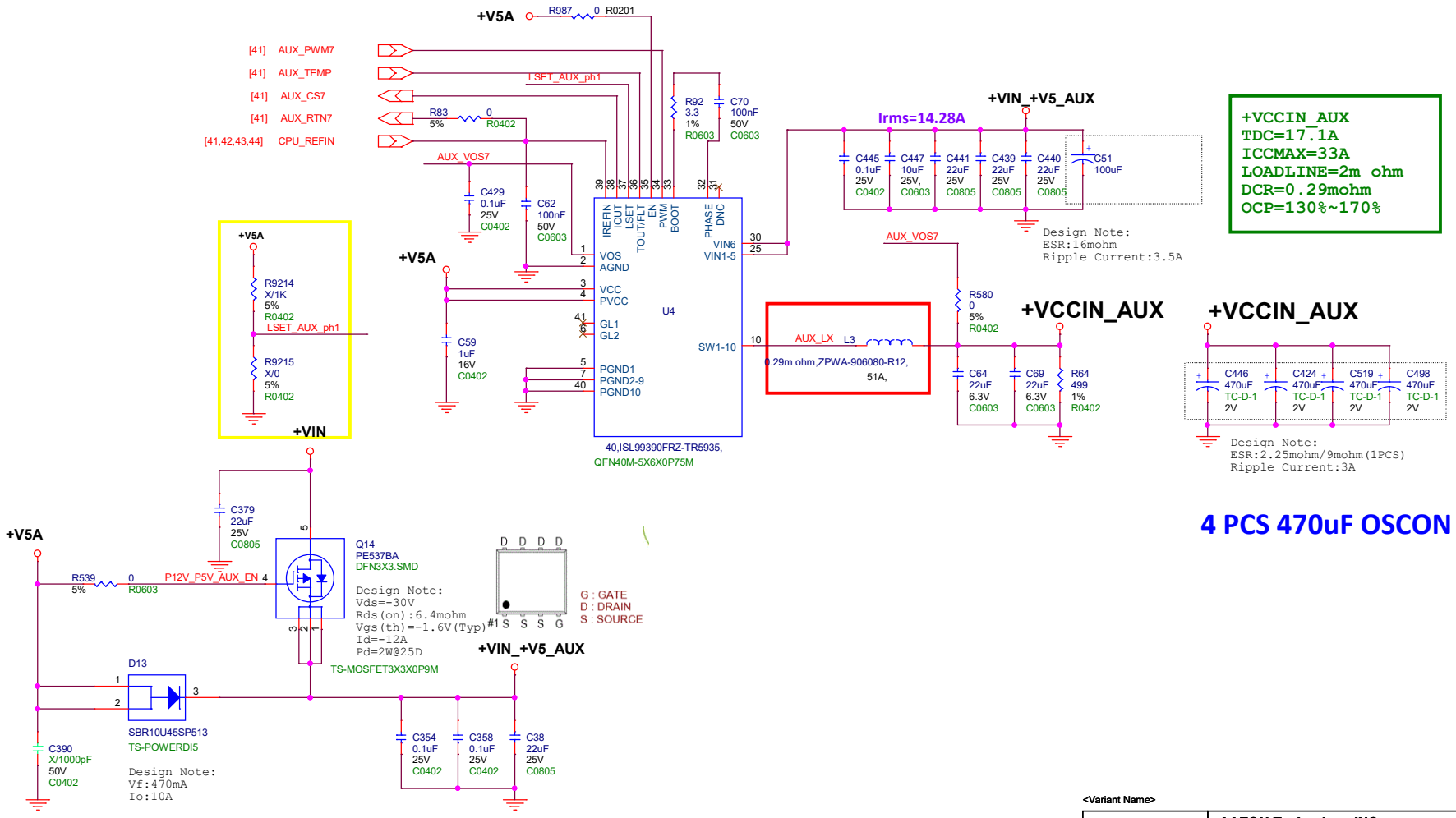
+VCCGT
TDC=22A
ICCMAX=30A
LOADLINE=4m ohm
DCR=0.29mohm
OCP=130%~170%

4 PCS 470uF OSCON OR SP

<Variant Name>

AAEON An ASUS Company	AAEON Technology INC.		
	Title: PWR_+VCCGT		
	Size: B	Document Number: EPIC-ADS7	Rev: A0.2_0_0
	Date: Thursday, January 20, 2022	Sheet 44 of 57	

PWR_+VCCIN_AUX@33A



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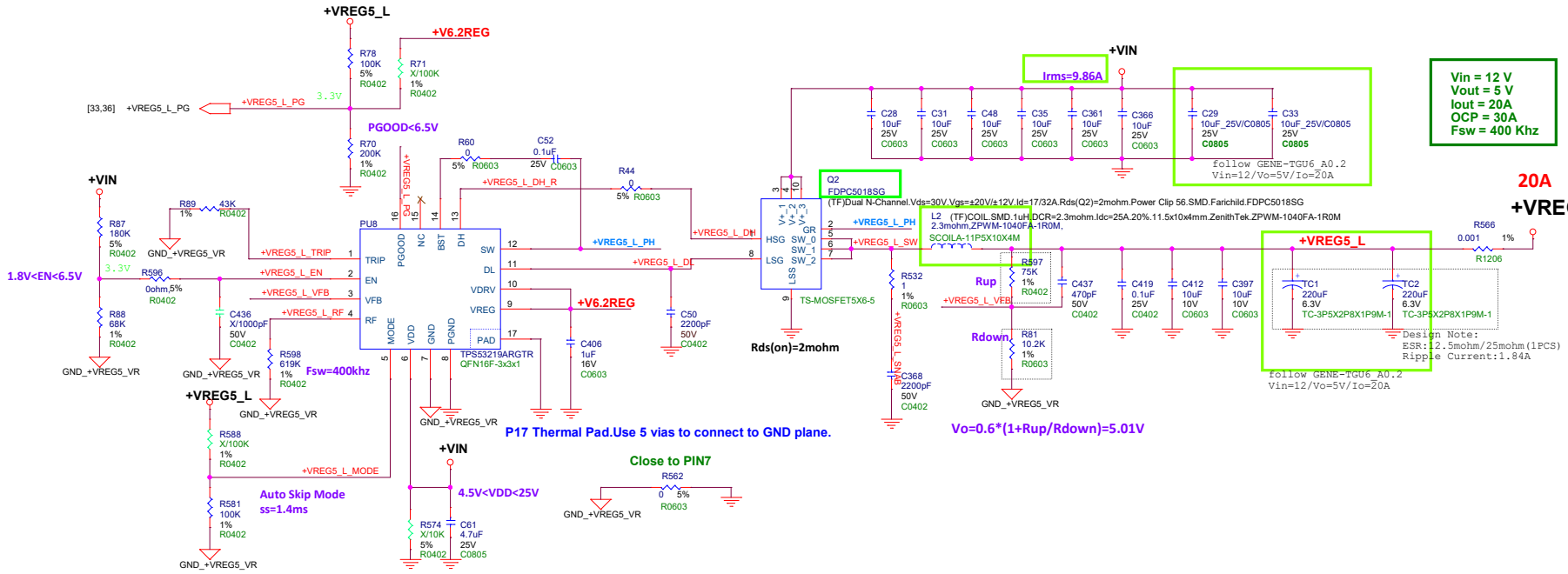
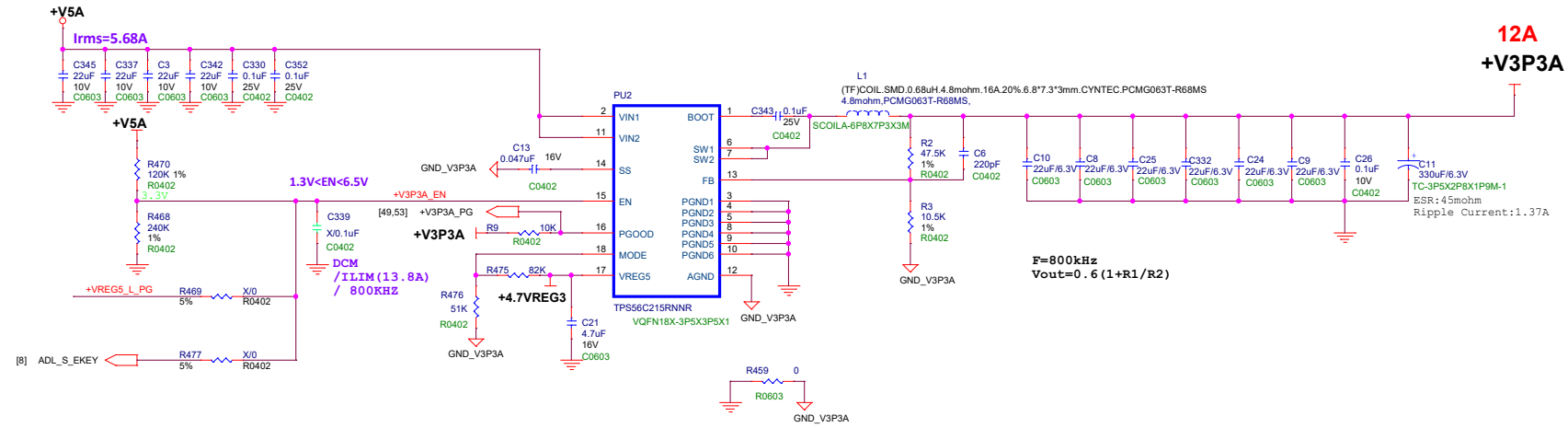
AAEON Technology INC.

Title	PWR_+VCCIN_AUX	
Size: B	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 45 of 57	

PWR +VREG5



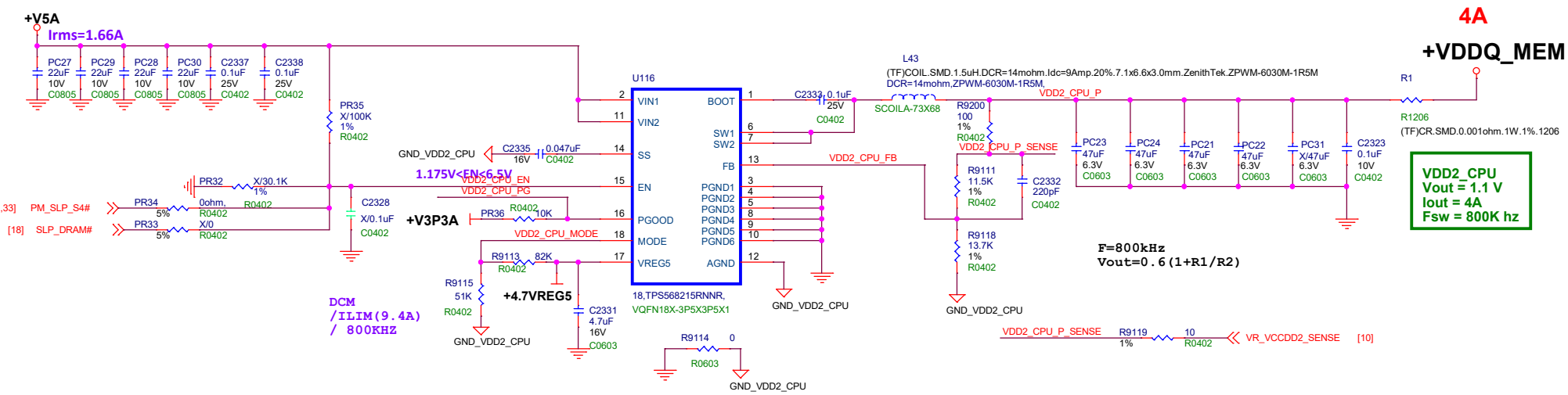
PWR +V3P3A

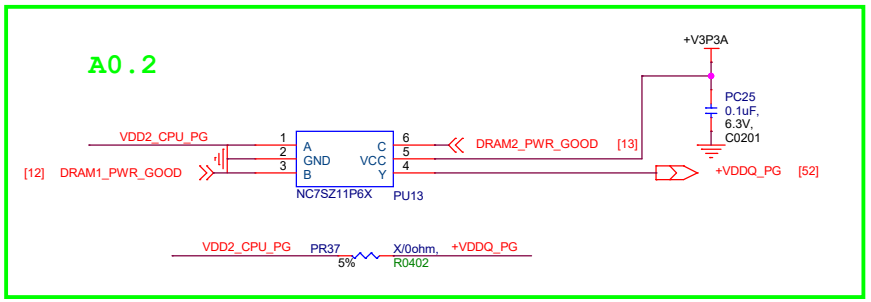


<Variant Name>

AAEON Technology INC.			
Title: +V5IN/+V3P3A			
Size: Custom	Document Number: EPIC-ADS7		Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 46 of 57		

PWR +VDDQ_MEM





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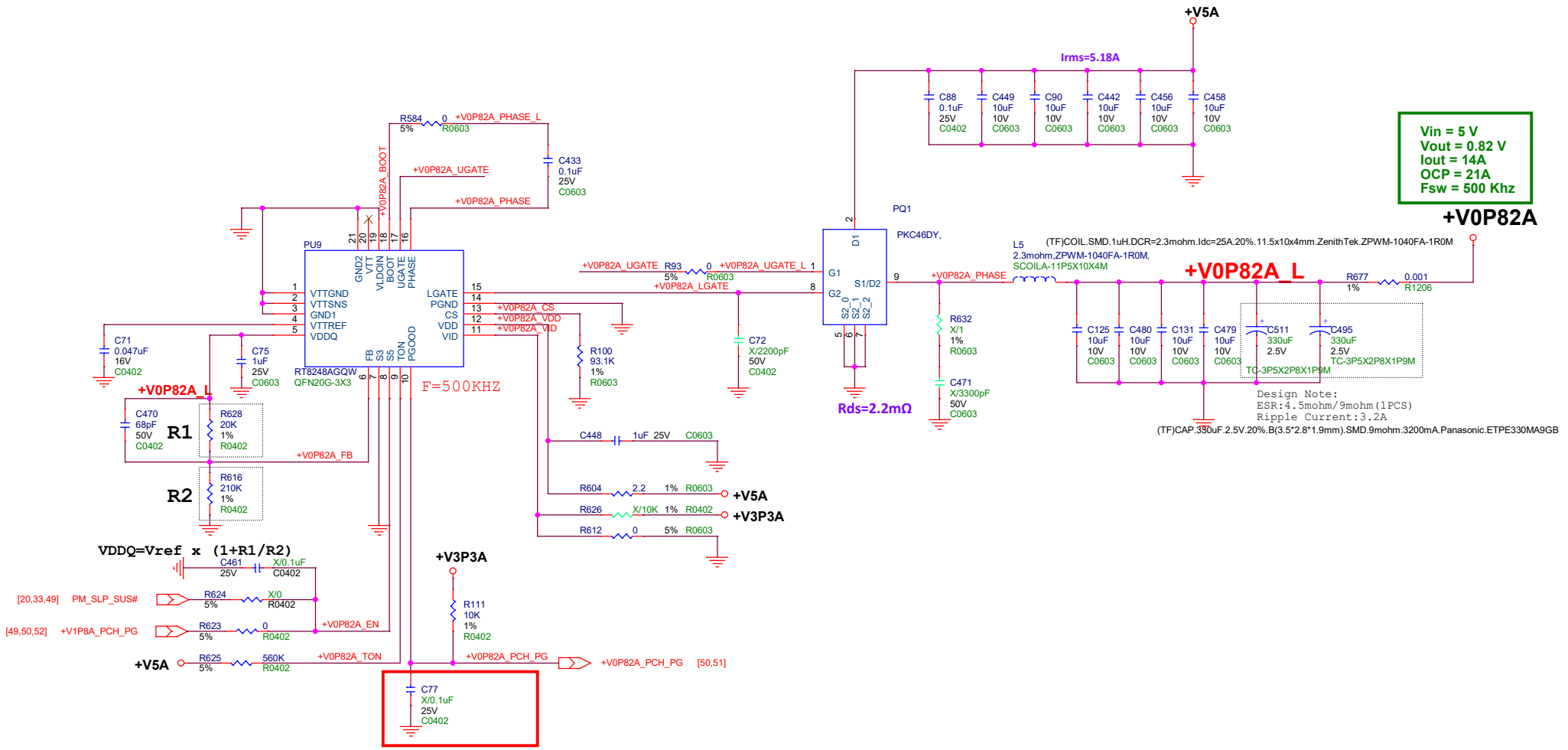
AAEON Technology INC.

Title	PWR_+VDDQ	
Size: B	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 47 of 57	

PWR +V0P82A



VOUT Select Table

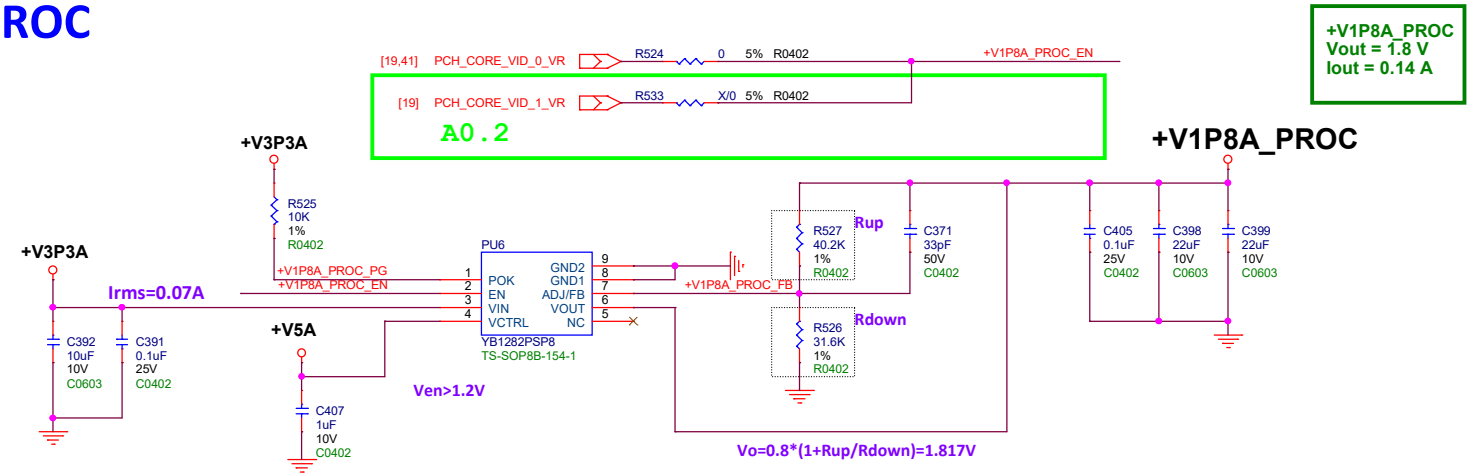
VID	Reference Voltage
HI	+0.675V
Low	+0.75V

<Variant Name>

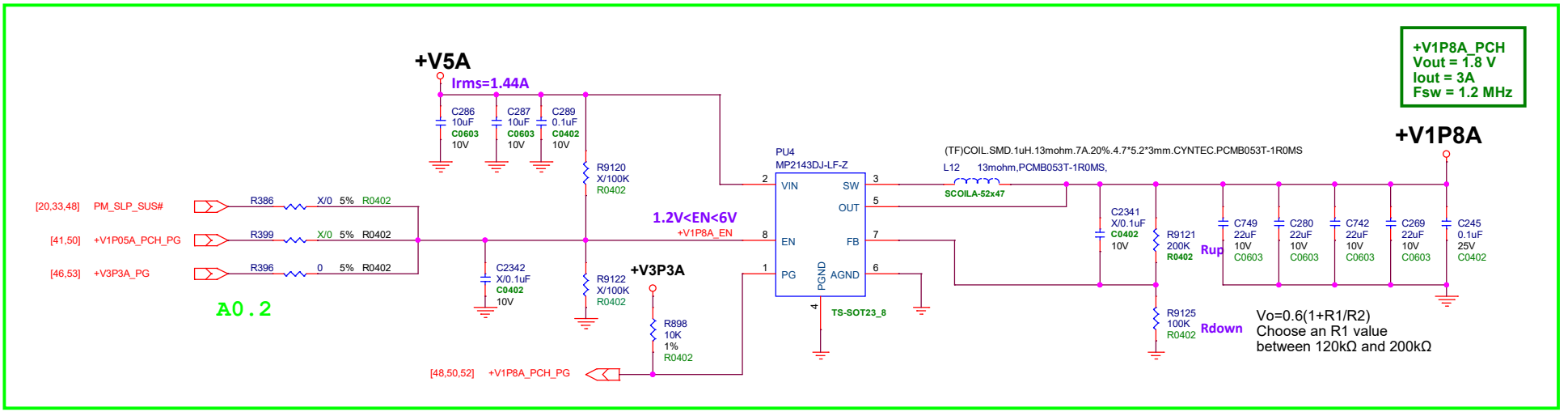
AAEON Technology INC.

Title: +V0P82A		
Size: B	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 48 of 57	

PWR +V1P8A_PROC



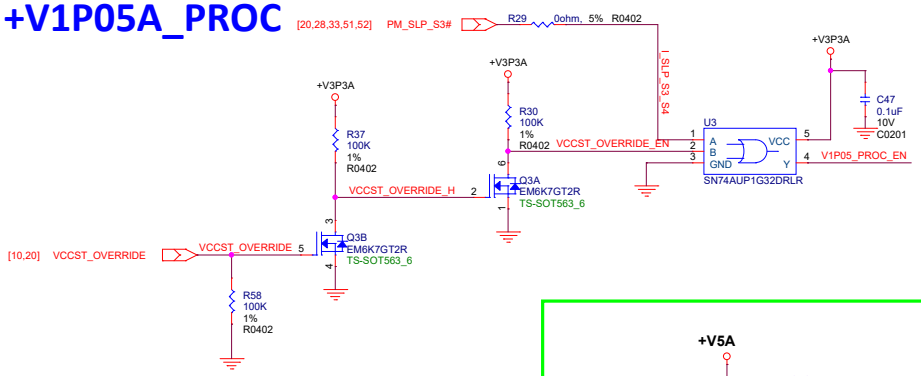
PWR +V1P8A_PCH

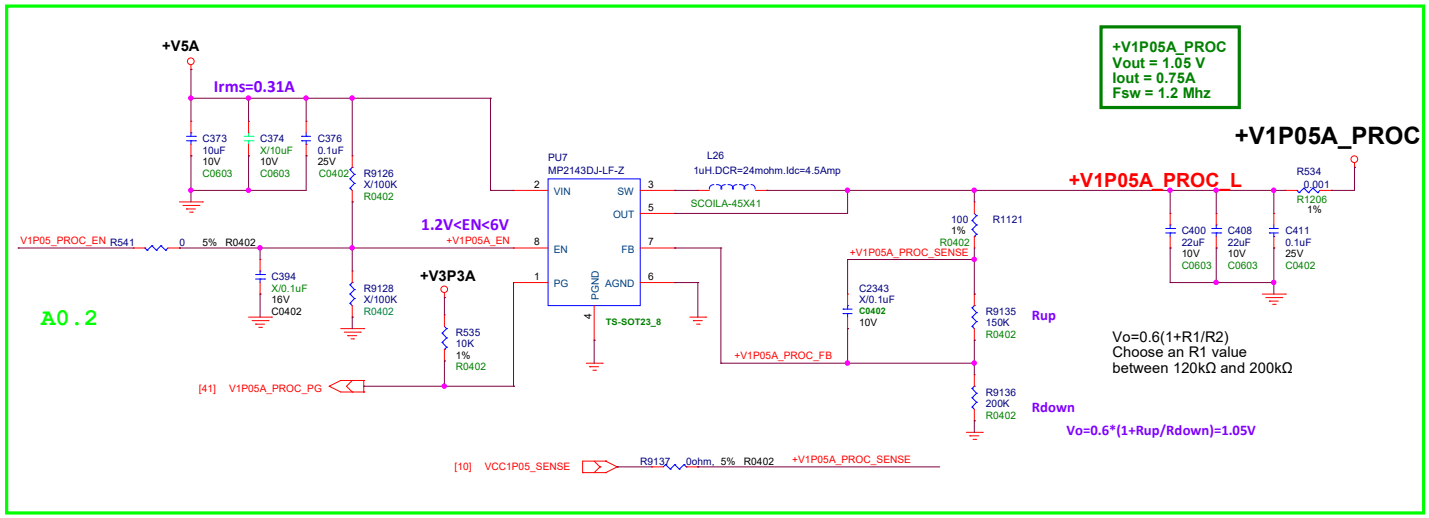


<Variant Name>

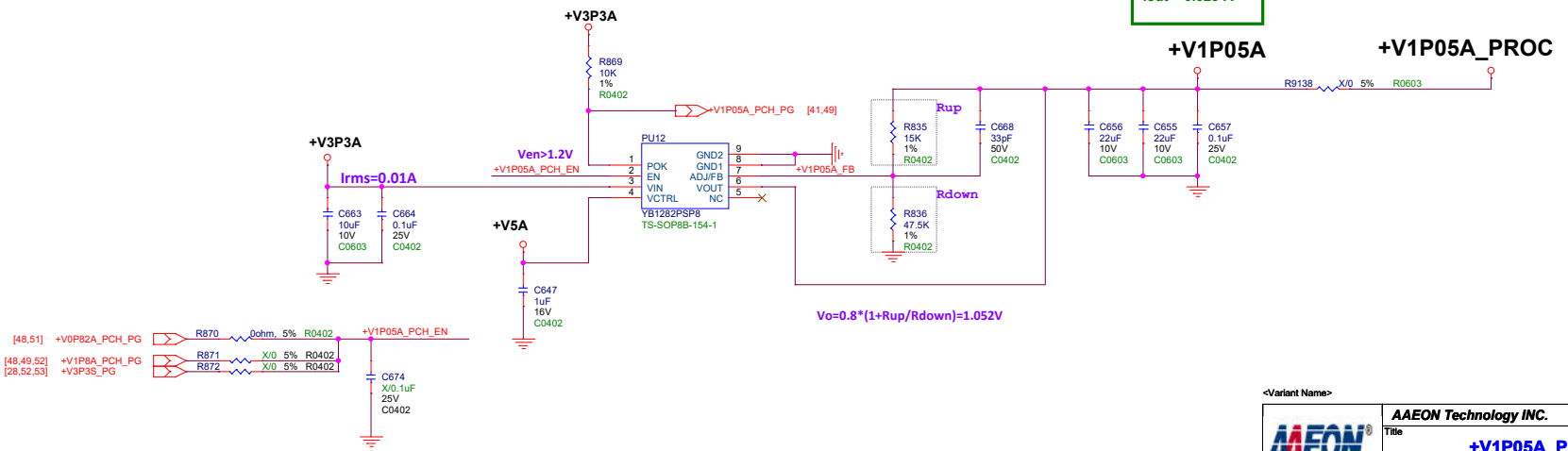
AAEON An ASUS Company	AAEON Technology INC.	
	Title: +V1P8A_PROC/+V1P8A	
	Size: B	Document Number: EPIC-ADS7 Rev: A0.2_0_0
	Date: Thursday, January 20, 2022	Sheet 49 of 57

PWR +V1P05A_PROC





PWR +V1P05A

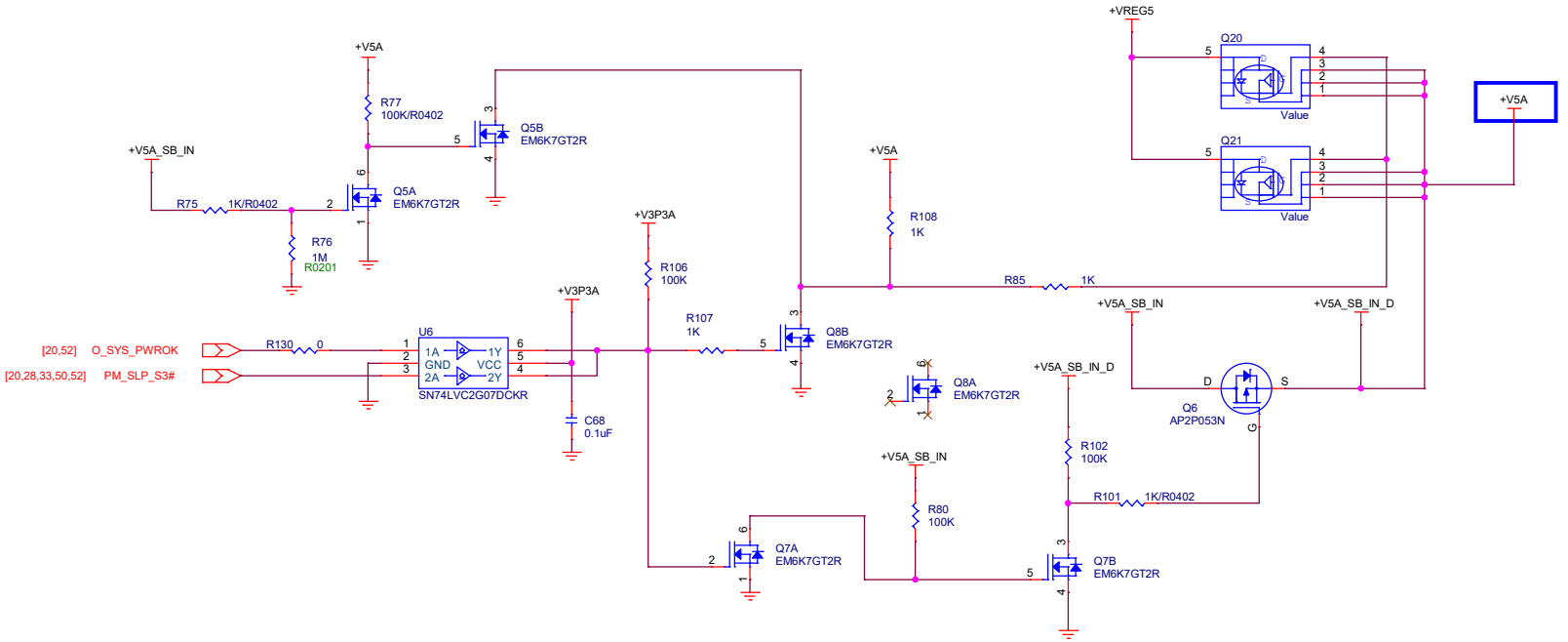


<Variant Name>

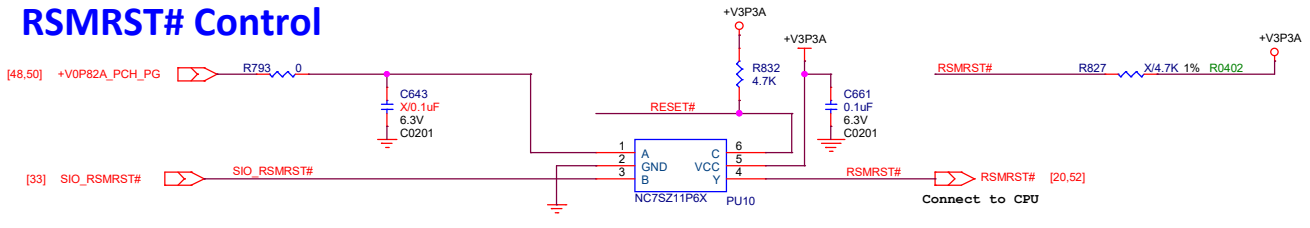
AAEON Technology INC.

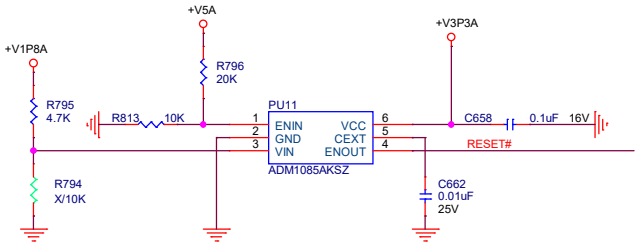
Title	+V1P05A_PROC/+V1P05A	
Size: Custom	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 50 of 57	

5VDAUL Switch Circuit



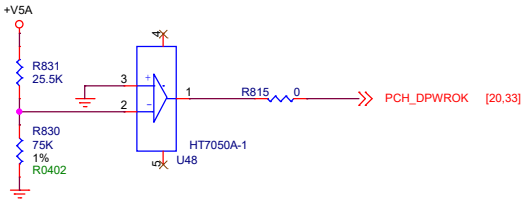
RSMRST# Control





NOTE:
PDG PAGE422, RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band. This is true for all power states transitions including emergency power loss.

RSMRST# is de-asserted by EC of O_RSMRSTon G3->S5, Asserted by VR of V3P3A_EN at S5->G3 before VccPRIM dropping.

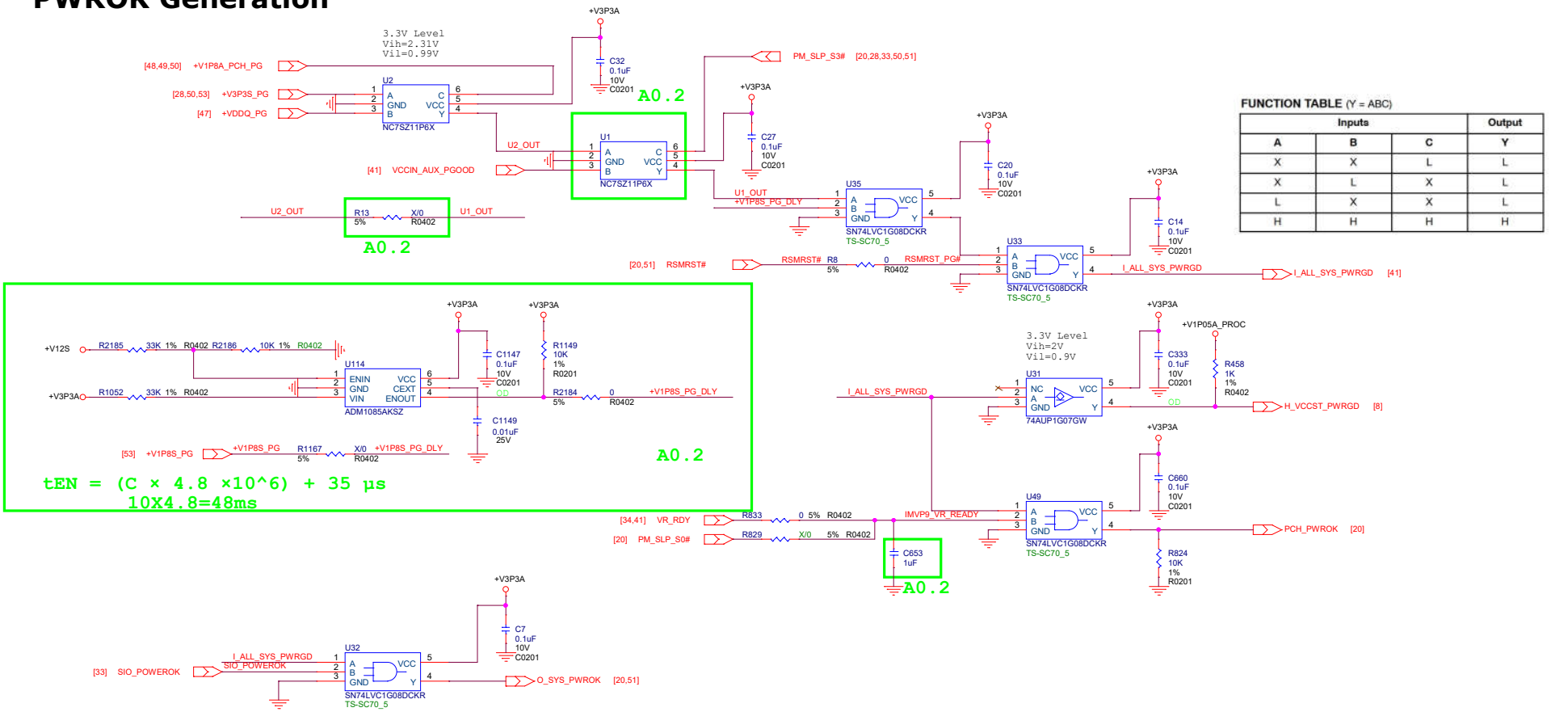


<Variant Name>

AAEON Technology INC.

Title: STANDBY POWER		
Size: Custom	Document Number: EPIC-ADS7	Rev: A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 51 of 57	

PWROK Generation



FUNCTION TABLE (Y = ABC)

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

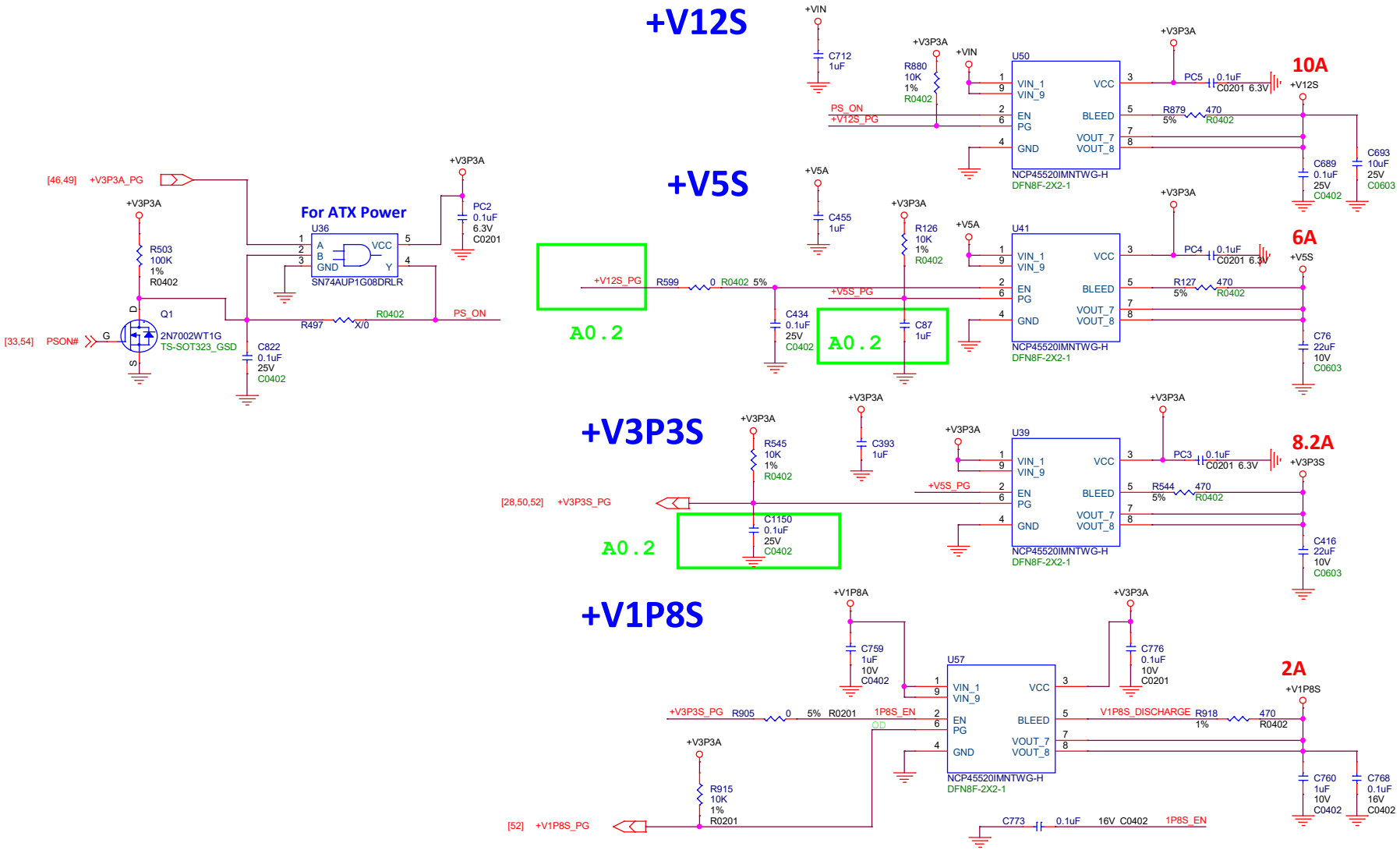
<Variant Name>

AAEON Technology INC.

Title: Boot Sequence

Size: Custom | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

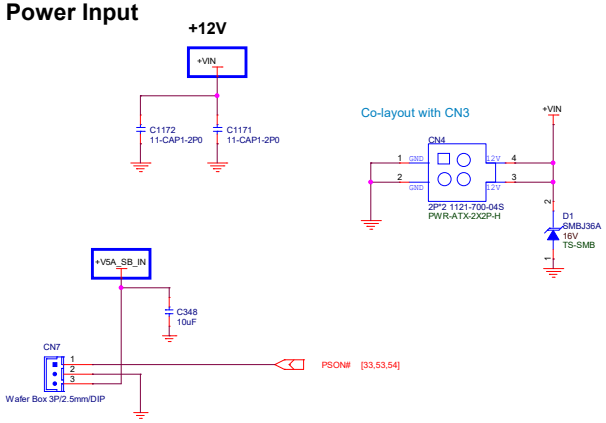
Date: Thursday, January 20, 2022 | Sheet 52 of 57



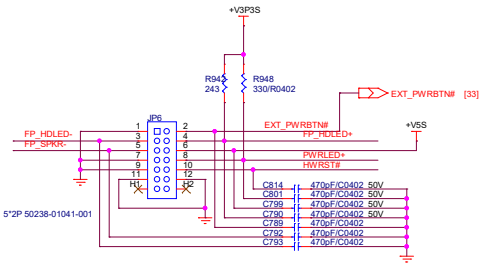
<Core Design>

AAEON Technology INC.	
Title	PWR_+V12S/ +V5S/ +V3P3S
Size: B	Document Number: EPIC-ADS7
Rev	A0.2_0_0
Date: Thursday, January 20, 2022	Sheet 53 of 57

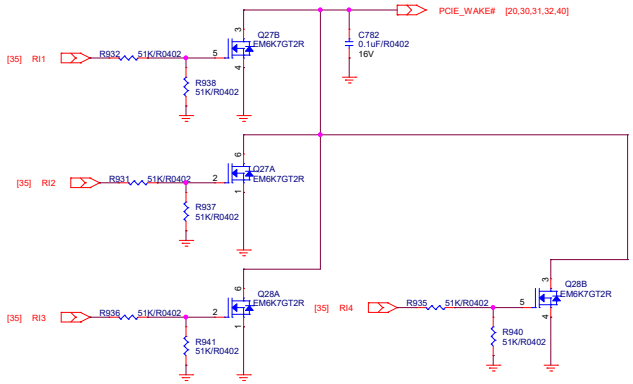
Power Input



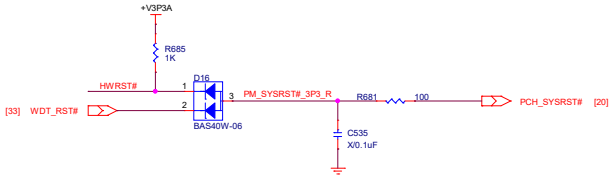
Front Panel



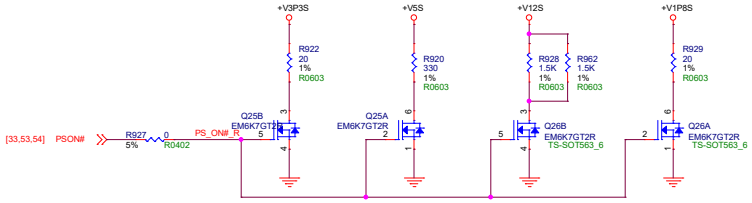
Wake On Modem



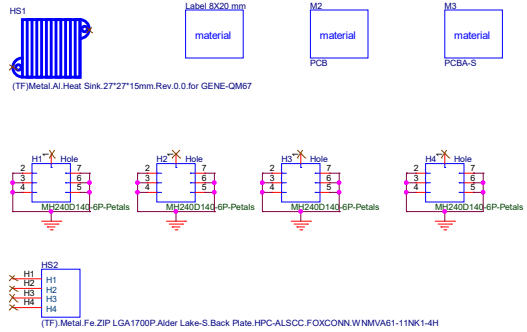
Reset Circuit



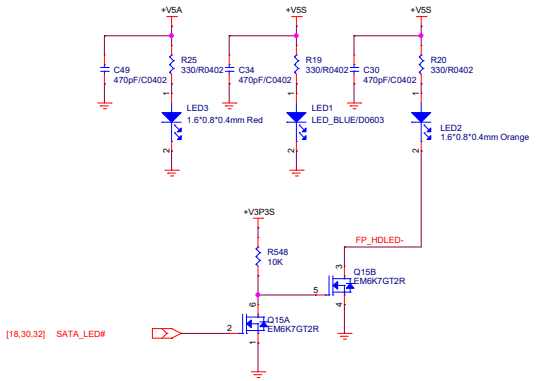
Discharge Circuit



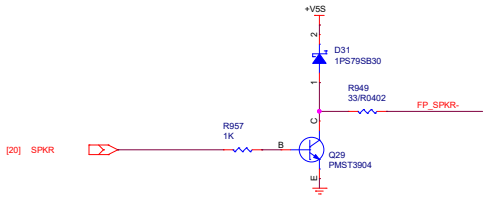
Mounting Holes
Need to be updated

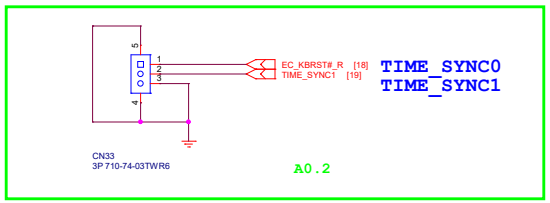


LED



Speaker





Design Note:
CPU Cooler Use

H5 MH276D167 (TF)BOSS.M3*2.45mm.Sn.EMISTOP.F55M30-250740P1D4M
H6 MH276D167 (TF)BOSS.M3*2.45mm.Sn.EMISTOP.F55M30-250740P1D4M
H7 MH276D167 (TF)BOSS.M3*2.45mm.Sn.EMISTOP.F55M30-250740P1D4M
H8 (TF)BOSS.M3*2.45mm.Sn.EMISTOP.F55M30-250740P1D4M MH276D167

<Variant Name>

AAEON Technology INC.

Title: POWER INPUT,MISC

Size	Document Number	Rev
Custom	EPIC-ADS7	A0.2_0_0

Date: Thursday, January 20, 2022 Sheet 54 of 57

HISTORY

HW

Date	Revision	Page	Modification list	Reason
20220112	A0.2	43	Vcore change to 5 phase.	VCORE
	A0.2	07/12/13/47	Change DDR4 to DDR5.	DDR5
	A0.2	29	Change LVDS CONN.	LVDS
	A0.2	33/38	Change DIO CONN.From SIO.	DIO
	A0.2	38	Add CN34 For SATA power.	SATA power
	A0.2	54	Add CN33 for TIME_SYNC.	TIME_SYNC
	A0.2	37	TYPEC add PD.	TYPEC
	A0.2	49	Remove R386,Stuff R396 for +V1P8A_EN.	+V1P8A
	A0.2	20	Remove R727,Stuff R732 for DSW_PWROK.	DSW_PWROK
	A0.2	25	Stuff R670 with 10k_0402 for TPM	TPM
	A0.2	34	Remove R2177,Stuff R2178 for espi/LPC.	espi/LPC
	A0.2	34	Remove R74,Stuff R61 for Debug card.	Debug card
	A0.2	41/52	Change R240 to 4.7k 0402 and C653 to 1uF.	PCH_PWROK
	A0.2	52	Add U114 for Vcore_EN delay.	VCORE
	A0.2	27	Add schematic for DP++	DP++

<Variant Name>

AAEON Technology INC.

Title: Revision History

Size: Custom | Document Number: EPIC-ADS7 | Rev: A0.2_0_0

Date: Thursday, January 20, 2022 | Sheet 55 of 57