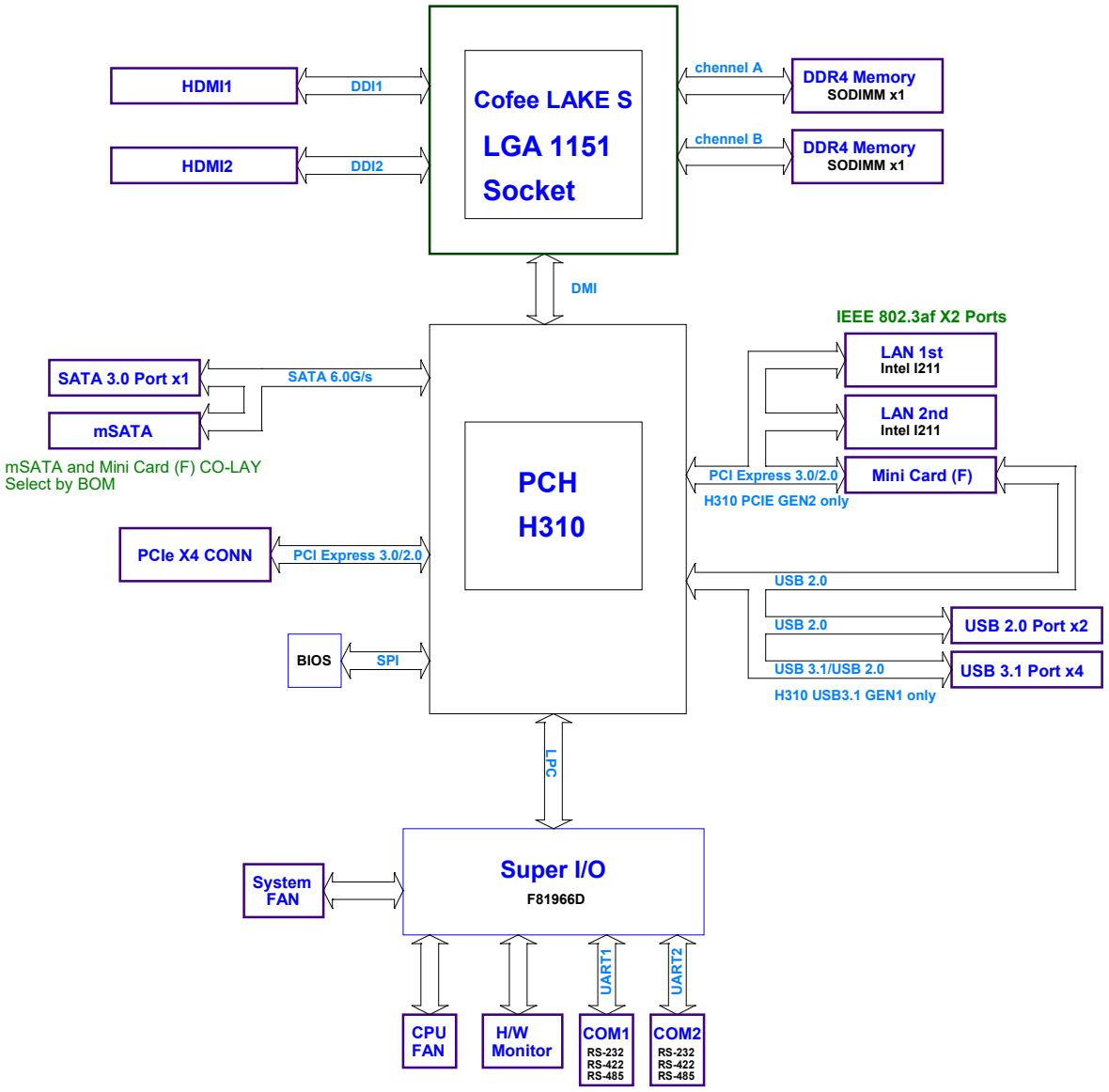
EPIC -CFS7 A0.2



Page	Index
1	COVER SHEET
2	SYSTEM SETTINGS
3	POWER DELIVERY
4	POWER SEQUENCE
5	PROCESSOR 1-DMI/PEG
6	PROCESSOR 2-DDR4
7	PROCESSOR 3-DDI/EDP
8	PROCESSOR 4-CLK/CFG/RSVD
9	PROCESSOR 5-PWR1
10	PROCESSOR 6-PWR2
11	PROCESSOR 7-VSS
12	DDR4_SODIMMA
13	Reserved
14	PCH 1-SPI/SMLINK/UART/I2C
15	PCH 2-CLK
16	PCH 3-DMI/USB2.0/PCIE/USB3
17	PCH 4-DDI/USB3/LPC/eSPI
18	PCH 5-PCIE/SATA/FAN
19	PCH 6-HDA/SMB/MISC/I2S/RTC
20	PCH 7-PWR
21	PCH 8-VSS
22	HDMI1
23	HDMI2
24	LAN1_INTEL i211
25	LAN2_INTEL i211
26	POE controller
27	POE Power
28	MINI CARD & mSATA
29	SATA
30	USB
31	RJ45
32	Reserved
33	Reserved
34	SUPERIO_FINTEK 81966
35	COM1~COM2
36	SPI BIOS,LPC
37	DIO,HWMONITOR,FAN
38	POWER INPUT,MISC
39	POWER_+V5A_+V3P3A
40	POWER_+VDDQ_MEM/VPP
41	ON-SEMI_CORE & VCC_GT
42	ON-SEMI VCC_CORE
43	ON-SEMI VCC_GT
44	POWER_ VCCSA
45	POWER_+V1.0A_+VCCIO
46	Boot Sequence
47	SYSTEM POWER
48	HISTORY

<Variant Name>

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Title: COVER SHEET

Size: Custom | Document Number: EPIC-CFS7 | Rev: A0.2

Date: Thursday, June 13, 2019 | Sheet: 1 of 48

SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	3.3V	20K PD/I	
GPIO_1	3.3V	20K PD/I	
GPIO_2	3.3V	20K PD/I	
GPIO_3	3.3V	20K PD/I	
GPIO_4	3.3V	20K PD/I	BOARDID_BIT0
GPIO_5	3.3V	20K PD/I	BOARDID_BIT1
GPIO_6	3.3V	20K PD/I	BOARDID_BIT2
GPIO_7	3.3V	20K PD/I	BOARDID_BIT3
GPIO_8	3.3V	20K PD/I	BOARDID_BIT4
GPIO_9	3.3V	20K PD/I	
GPIO_10	3.3V	20K PD/I	
GPIO_11	3.3V	20K PD/I	
GPIO_12	3.3V	20K PD/I	
GPIO_13	3.3V	20K PD/I	GPIO_PME#
GPIO_14	3.3V	20K PD/I	WAKE_RI#
GPIO_15	3.3V	20K PD/I	
GPIO_16	3.3V	20K PD/I	
GPIO_17	3.3V	20K PD/I	
GPIO_18	3.3V	20K PD/I	
GPIO_19	3.3V	20K PD/I	
GPIO_20	3.3V	20K PD/I	
GPIO_21	3.3V	20K PD/I	
GPIO_22	3.3V	20K PD/I	SATA_GP[0]
GPIO_23	3.3V	20K PD/I	SATA_GP[1]
GPIO_24	3.3V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	3.3V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	3.3V	20K PD/I/OP	SATA_LED_N
GPIO_27	3.3V	20K PD/I	
GPIO_28	3.3V	20K PD/I	
GPIO_29	3.3V	20K PD/I	
GPIO_30	3.3V	20K PD/I	
GPIO_31	3.3V	20K PD/I	
GPIO_32	3.3V	20K PD/I	
GPIO_33	3.3V	20K PD/I	PMIC_IRQ
GPIO_216	3.3V	20K PD/IO	
GPIO_217	3.3V	20K PD/IO	
GPIO_218	3.3V	20K PD/IO	
GPIO_219	3.3V	20K PD/IO/OP	

F81966D GPIO Pins :

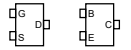
Name	Tolerance	Power Well	Default	Function
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#(REV)
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#(REV)
GPIO02	5V	I_VSB3V	Native	PM_SUS_WARN#(REV)
GPIO03	5V	I_VSB3V	Native	PM_SUS_ACK#(REV)
GPIO04	5V	I_VSB3V	Native	PM_SLP_SUS#(REV)
GPIO05	5V	I_VSB3V	Native	LAN1_DISABLE#
GPIO06	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO07	5V	I_VSB3V	Native	W_DISABLE0#
GPIO10	5V	I_VSB3V	Native	W_DISABLE1#(REV)
GPIO11	5V	I_VSB3V	Native	EN_USB(REV)
GPIO12	5V	I_VSB3V	Native	DIS_TOUCH#
GPIO13	5V	I_VSB3V	Native	
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP
GPIO15	5V	I_VSB3V	Native	WDT_RST#
GPIO16	5V	I_VSB3V	Native	
GPIO17	5V	I_VSB3V	Native	SIO_PECI
GPIO20	5V	I_VSB3V	Native	mSATA_PCIE_SEL(REV)
GPIO21	5V	I_VSB3V	Native	SIO_ATXPG
GPIO22	5V	I_VSB3V	Native	EXT_PWRBTN#
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#
GPIO24	5V	I_VSB3V	Native	PM_SLP_S3#
GPIO25	5V	I_VSB3V	Native	PSON#
GPIO26	5V	VBAT	Native	PWOK
GPIO27	5V	VBAT	Native	SIO_RSMRST#
GPIO30	5V	3VCC	Native	
GPIO31	5V	3VCC	Native	
GPIO32	5V	3VCC	Native	
GPIO33	5V	3VCC	Native	
GPIO34	5V	3VCC	Native	
GPIO35	5V	3VCC	Native	
GPIO36	5V	3VCC	Native	
GPIO37	5V	3VCC	Native	
GPIO40	5V	3VCC	Native	
GPIO41	5V	3VCC	Native	
GPIO42	5V	3VCC	Native	
GPIO43	5V	3VCC	Native	
GPIO44	5V	3VCC	Native	
GPIO45	5V	3VCC	Native	AUDIO_MUTE#
GPIO46	5V	3VCC	Native	LAN4_DISABLE#
GPIO47	5V	3VCC	Native	LAN3_DISABLE#
GPIO50	5V	3VCC	Native	COM1_SLEW
GPIO51	5V	3VCC	Native	SEL_COM1_MD0
GPIO52	5V	3VCC	Native	SEL_COM1_MD1
GPIO53	5V	3VCC	Native	COM1_SD
GPIO54	5V	3VCC	Native	COM2_SLEW
GPIO55	5V	3VCC	Native	SEL_COM2_MD0
GPIO56	5V	3VCC	Native	SEL_COM2_MD1
GPIO57	5V	3VCC	Native	COM2_SD
GPIO60	5V	3VCC	Native	
GPIO61	5V	3VCC	Native	
GPIO62	5V	3VCC	Native	
GPIO63	5V	3VCC	Native	
GPIO64	5V	3VCC	Native	CH7517_RST#
GPIO65	5V	I_VSB3V	Native	SIO_PME#
GPIO66	5V	VBAT	Native	DPWROK_R
GPIO67	5V	I_VSB3V	Native	PM_SLP_S4#
GPIO70	5V	3VCC	Native	PE(REV)
GPIO71	5V	3VCC	Native	BUSY(REV)
GPIO72	5V	3VCC	Native	ACK#(REV)
GPIO73	5V	3VCC	Native	SLIN#(REV)
GPIO74	5V	3VCC	Native	PINIT#(REV)
GPIO75	5V	3VCC	Native	ERR#(REV)
GPIO76	5V	3VCC	Native	AFD#(REV)
GPIO77	5V	3VCC	Native	STB#(REV)
GPIO80	5V	3VCC	Native	DIO0
GPIO81	5V	3VCC	Native	DIO1
GPIO82	5V	3VCC	Native	DIO2
GPIO83	5V	3VCC	Native	DIO3
GPIO84	5V	3VCC	Native	DIO4
GPIO85	5V	3VCC	Native	DIO5
GPIO86	5V	3VCC	Native	DIO6
GPIO87	5V	3VCC	Native	DIO7

Note:
REV means reserved

SMBus/I2C Addresses :

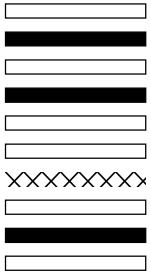
Device	Address
SODIMMA	A0h
SODIMMB	A2h
CMOS Backup EEPROM	AEh
PTN3366 Slave	C0h
GPIO IC (SIO 81966)	6Eh

PCB Footprints



PCB STACK :

Impedence 50ohm +/-10%.



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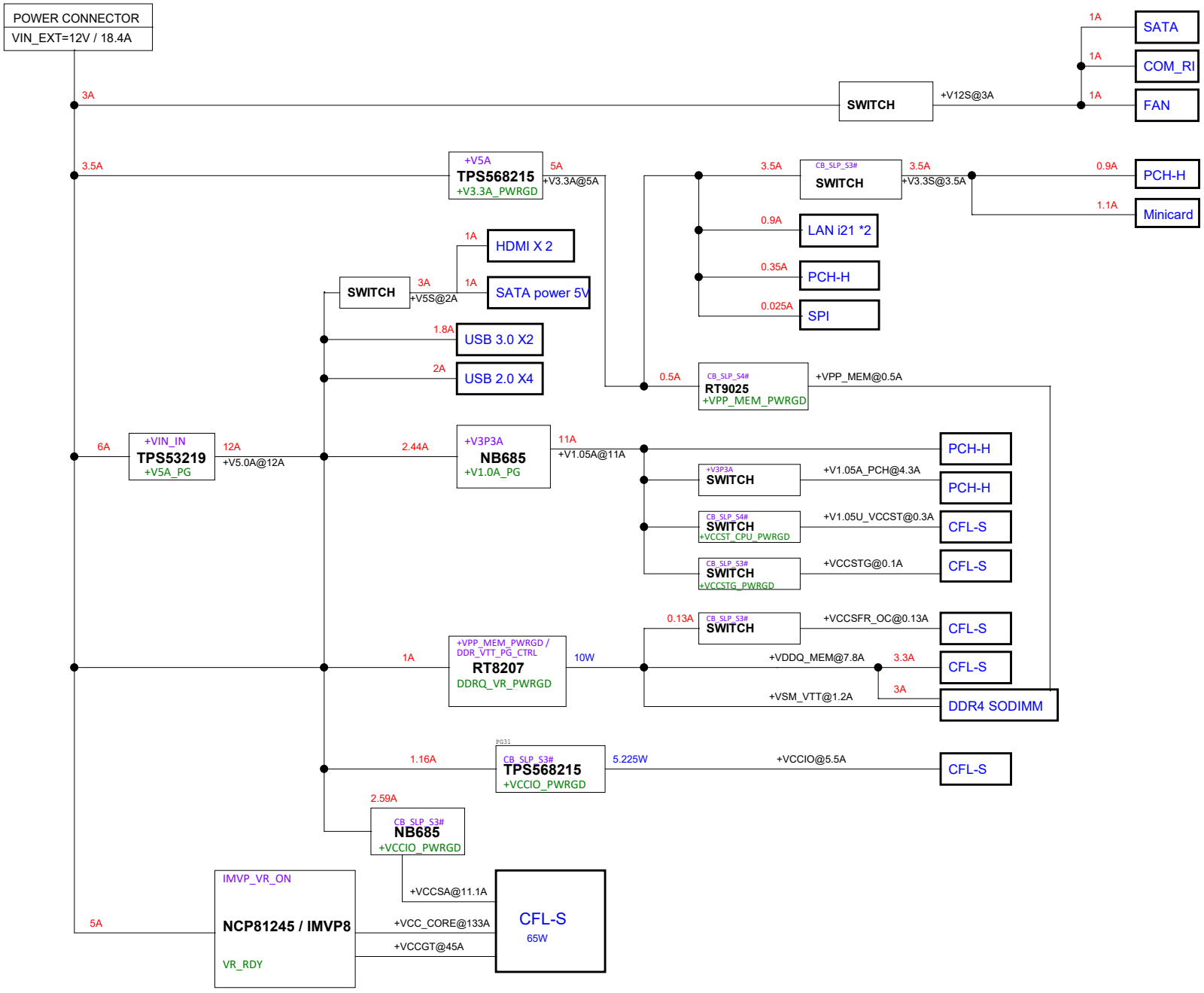
Title: SYSTEM SETTINGS

Size	Document Number	Rev:
Custom	EPIC-CFS7	A0.2

Date: Thursday, June 13, 2019 | Sheet: 2 of 48



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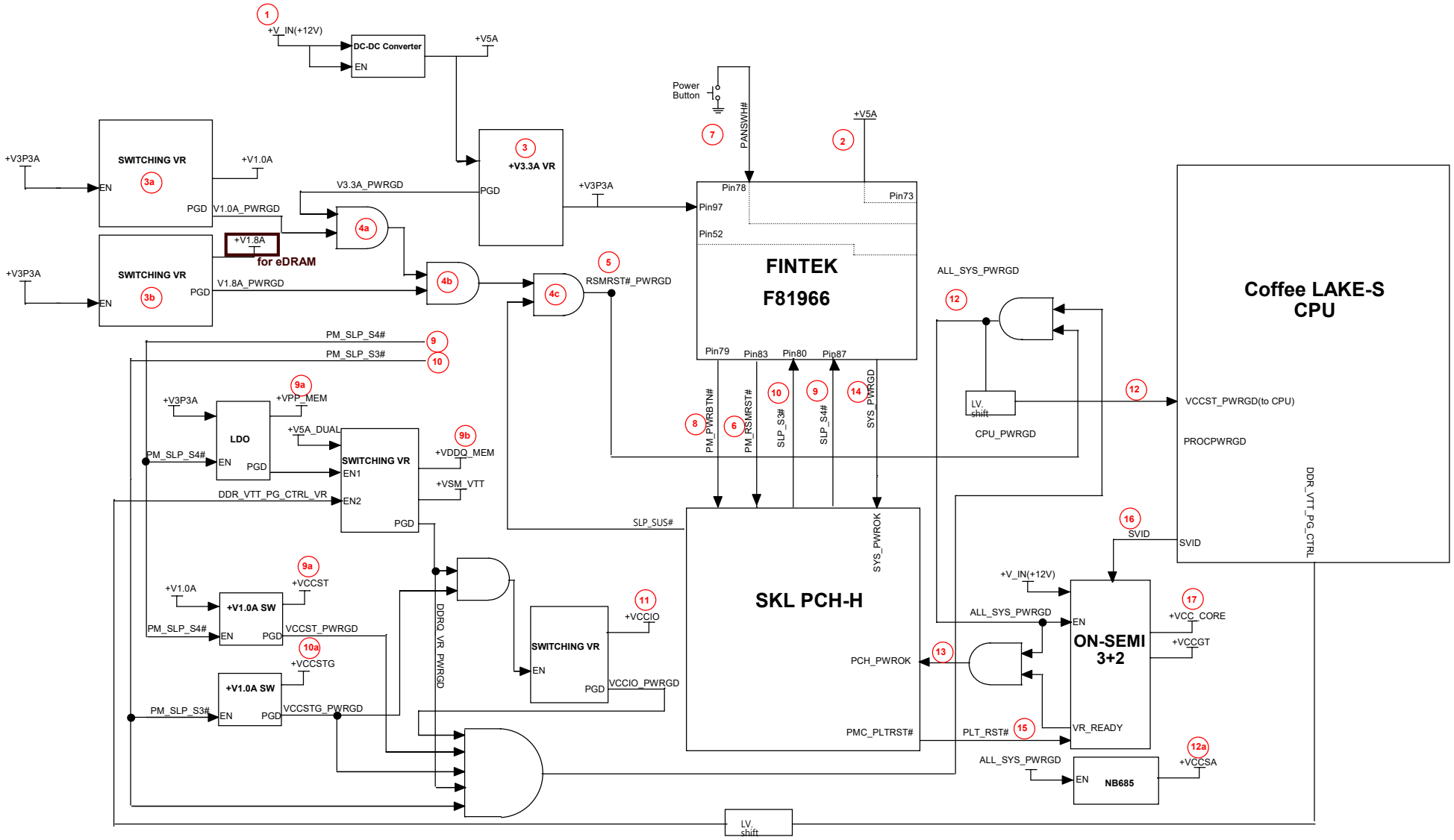
C	EPIC-CFS7	A0.2

Date: Thursday, June 13, 2019 | Sheet: 3 of 48



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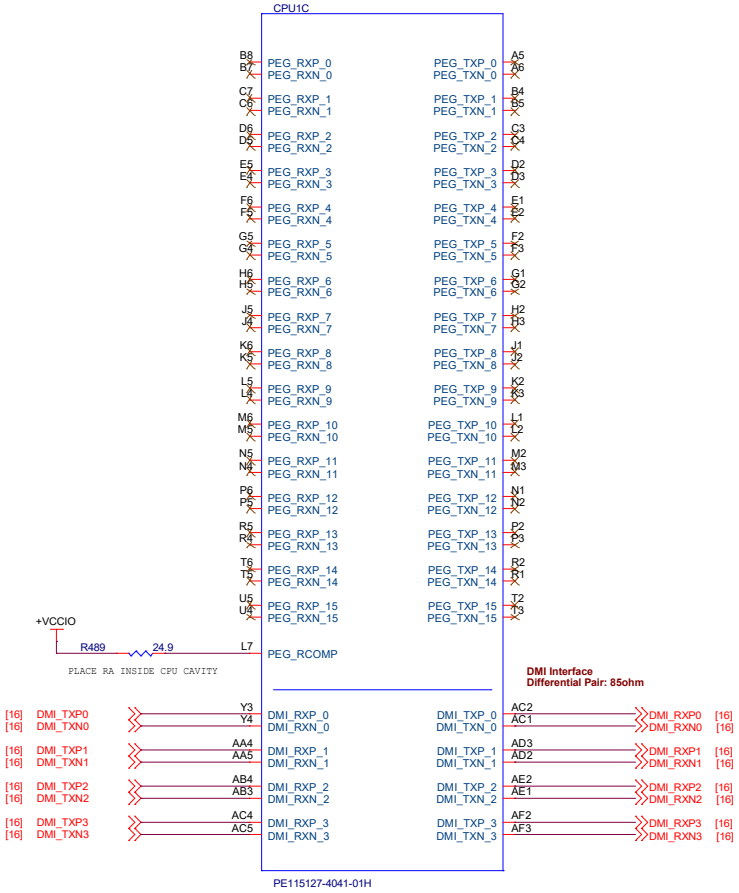
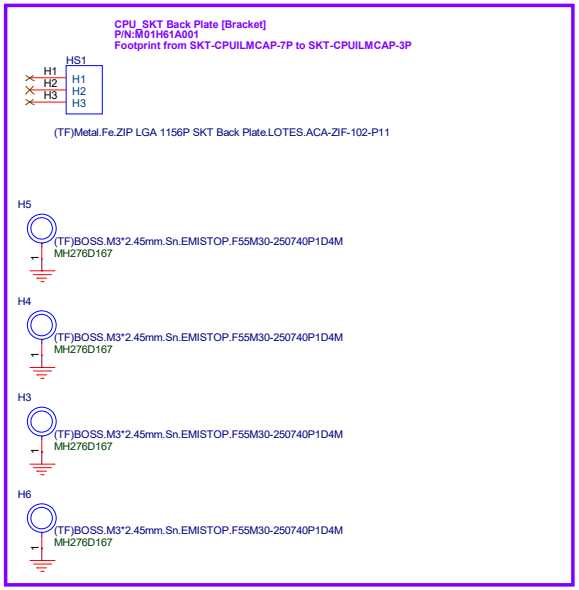
Title: POWER SEQUENCE		
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*	Sheet: 4 of 48	

SKYLAKE-H BGA PROCESSOR(DMI/PEG)





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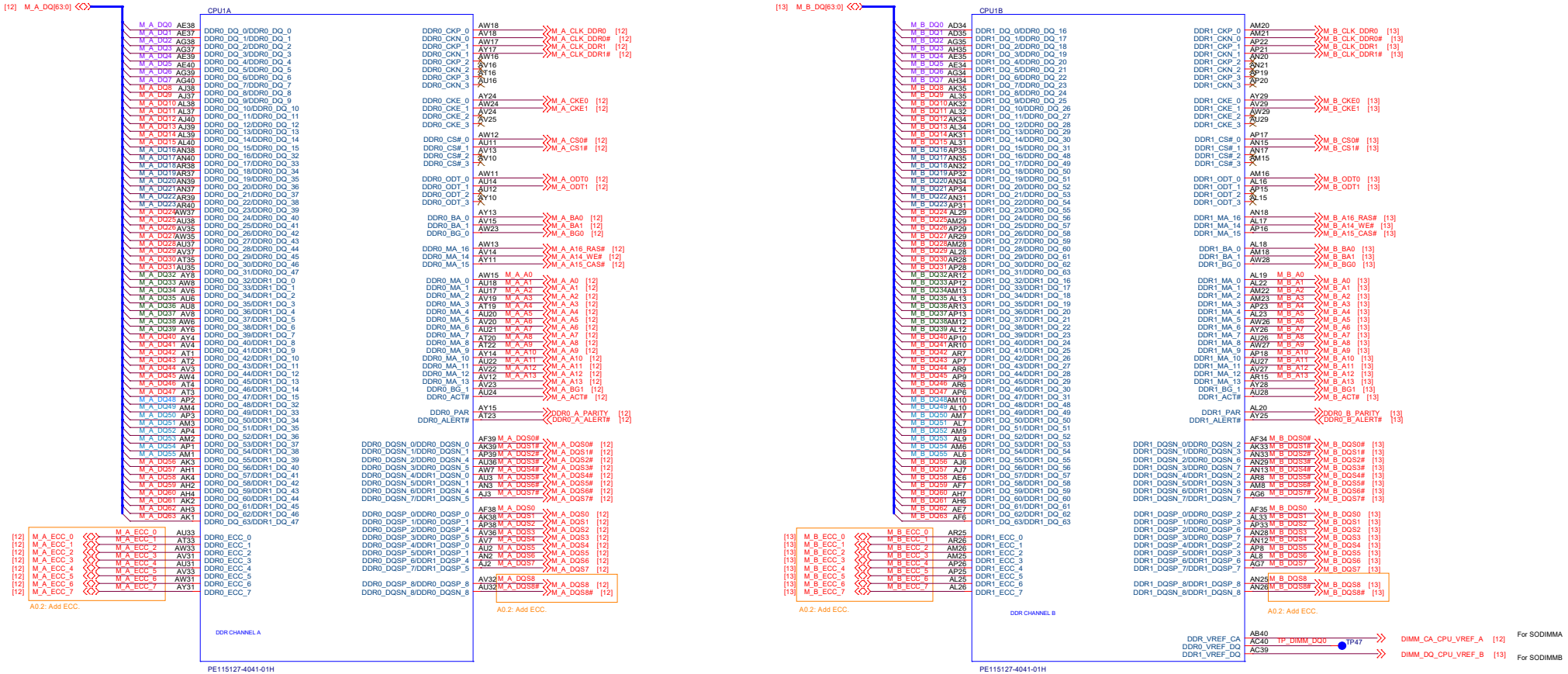
Title: **PROCESSOR 1-DMI/PEG**		
Size: A	Document Number: **EPIC-CFS7**	Rev: **A0.2**
Date: *Thursday, June 13, 2019*	Sheet: **5** of **48**	



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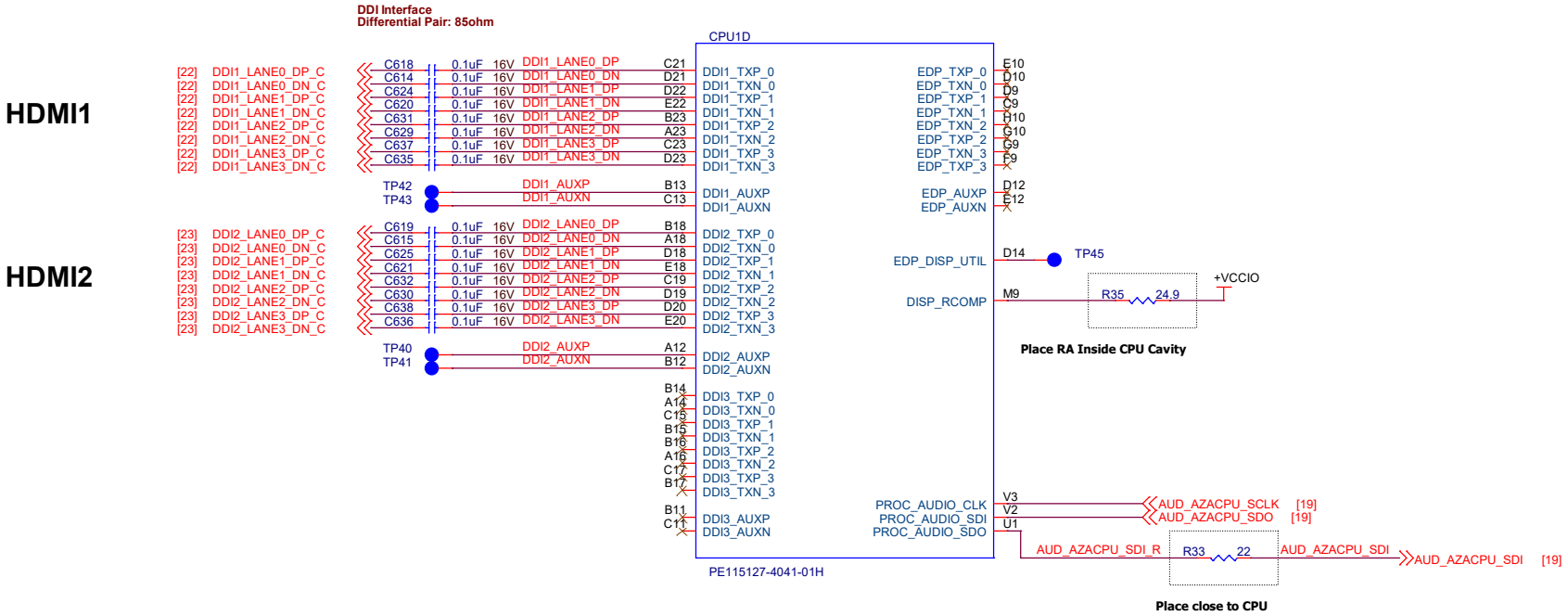
Date: *Thursday, June 13, 2019*	Sheet: **6** of **48**	



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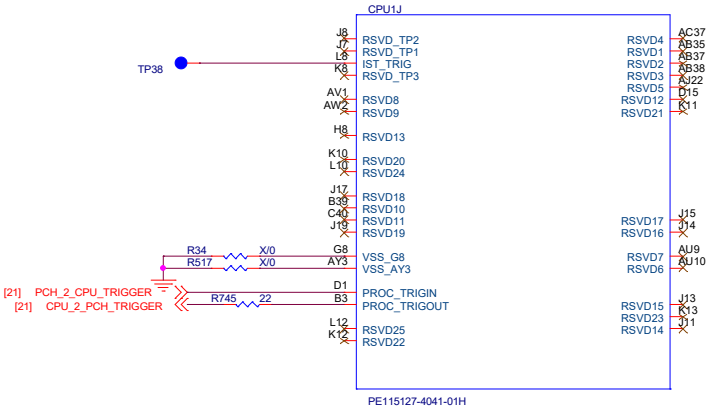
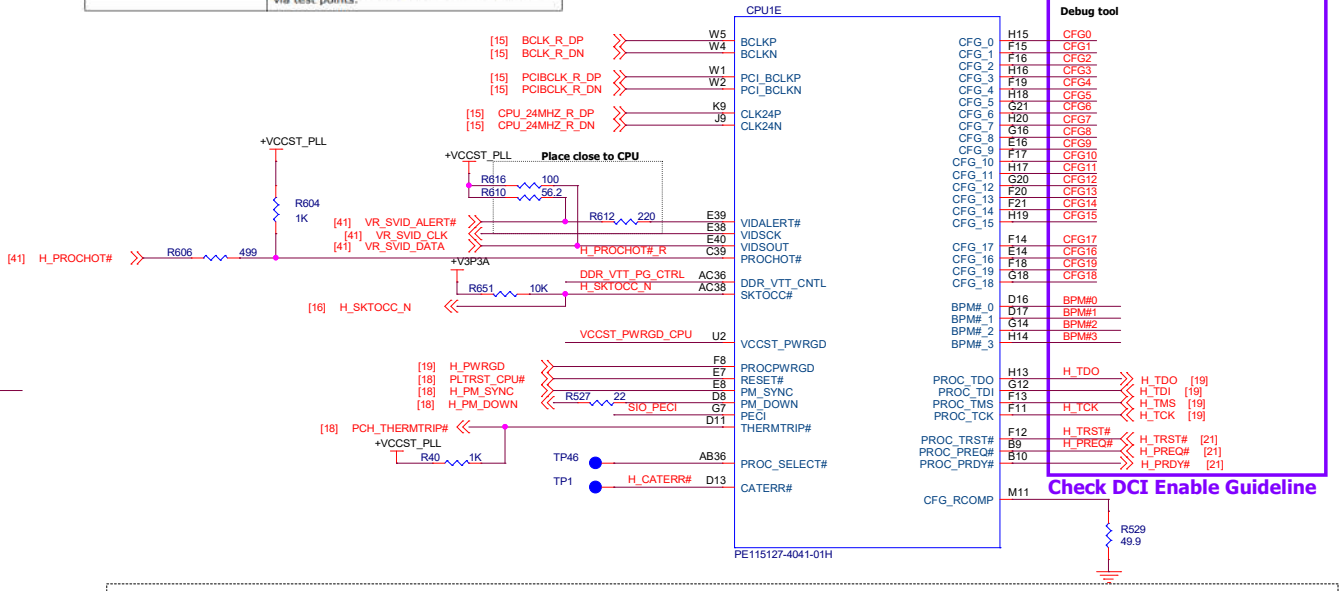
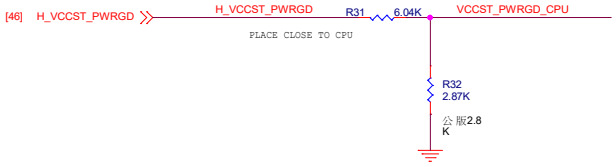
Title: PROCESSOR 3-DDI/EDP		
Size: B	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*	Sheet: 7 of 48	

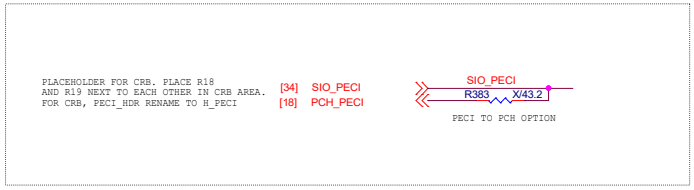
GND, RSVD, and NCTF Signals

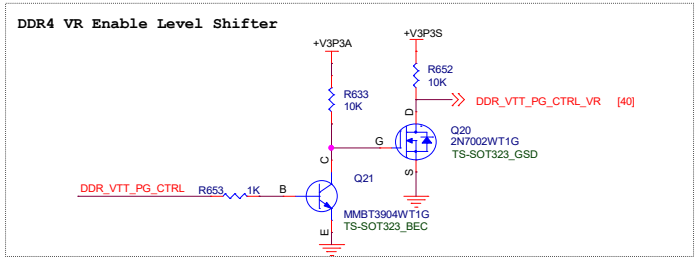
Signal Name	Description
Vss	Processor ground node
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.

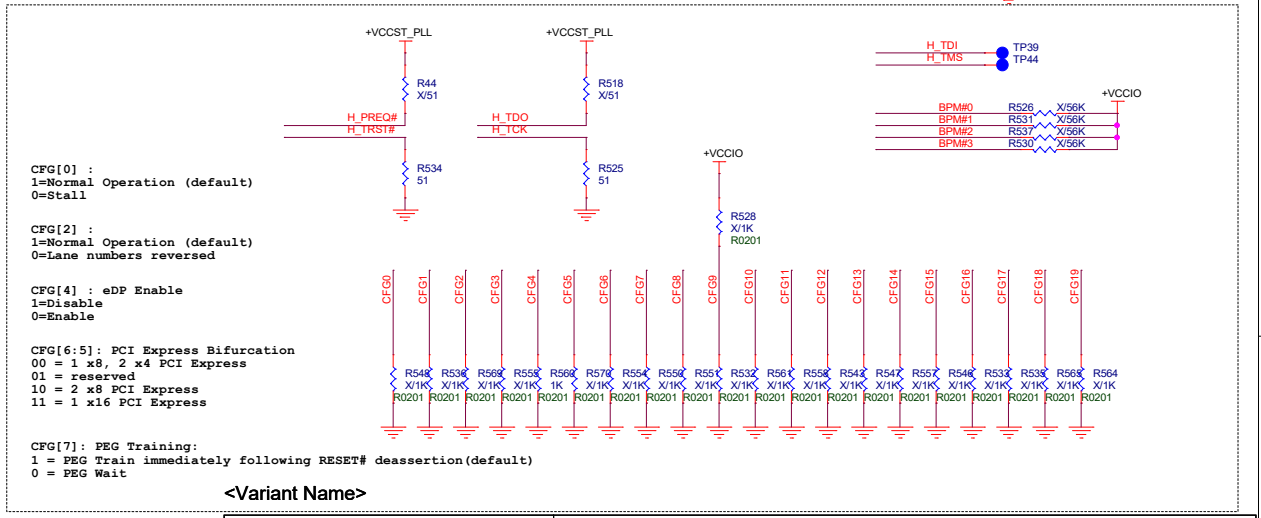












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Title: **PROCESSOR 4-CLK/CFG/RSVD**		
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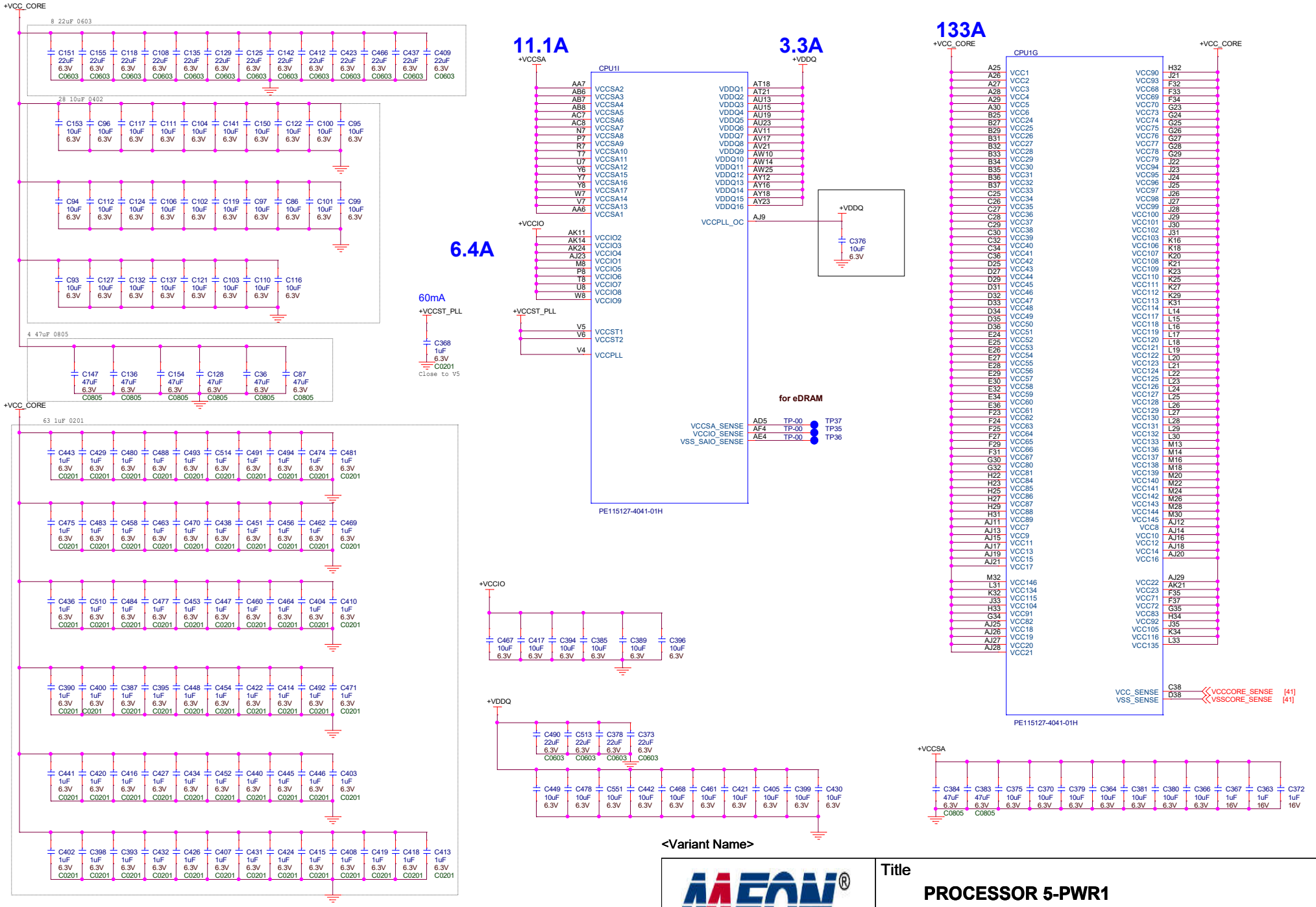
Date: *Thursday, June 13, 2019*	Sheet: **8** of **48**	



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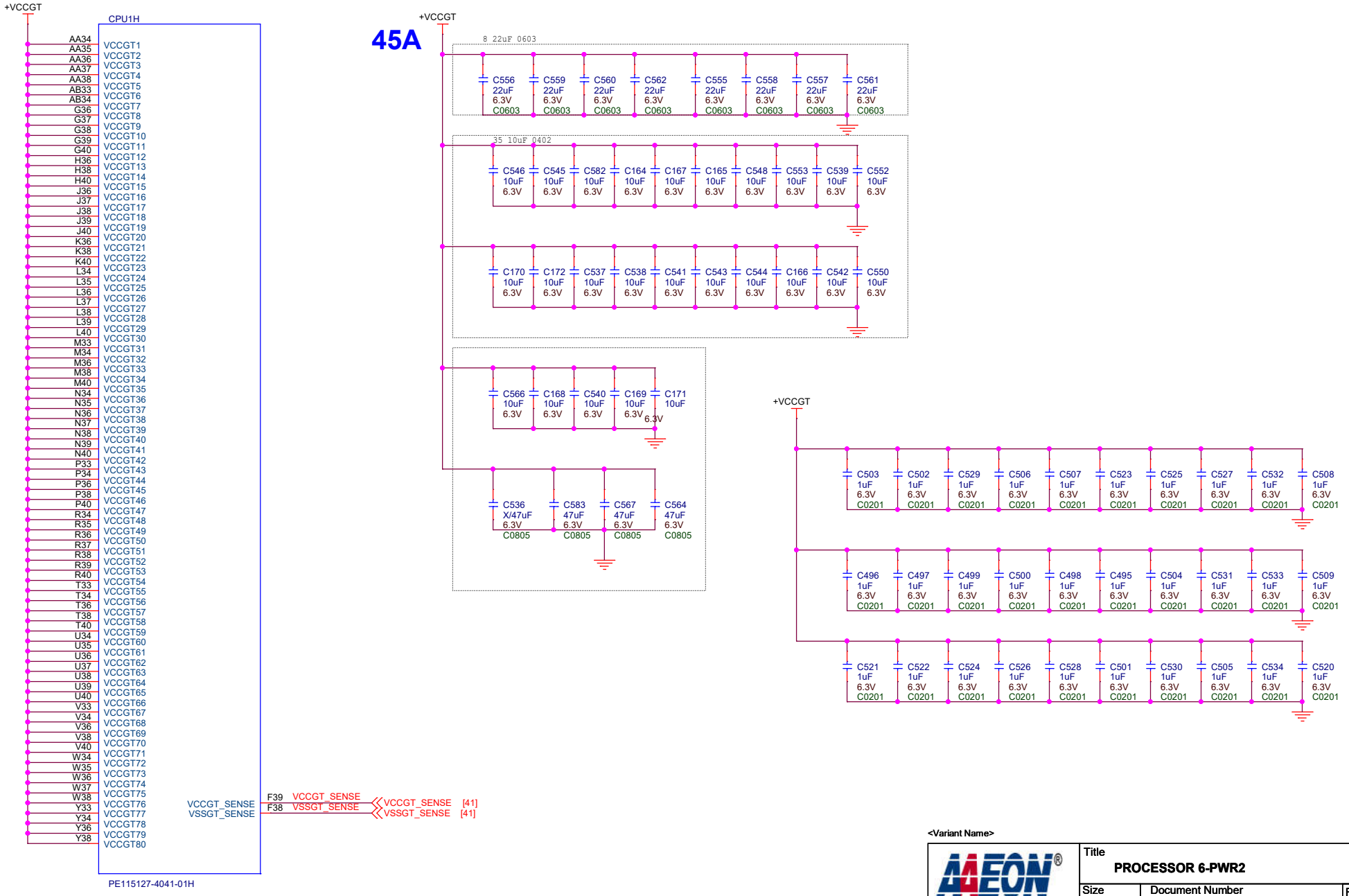
Date: *Thursday, June 13, 2019*	Sheet: **9** of **48**	



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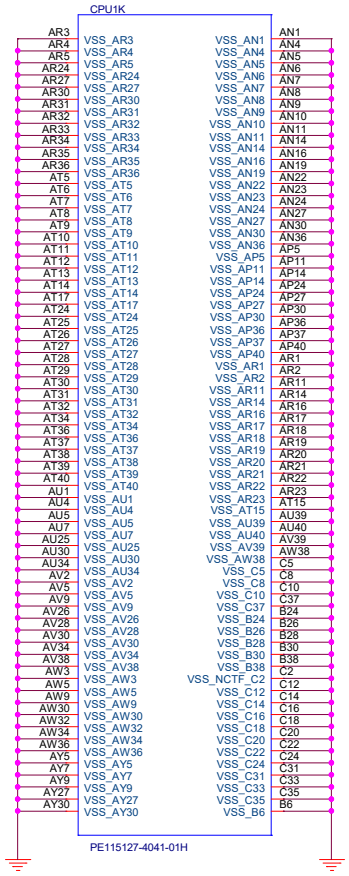
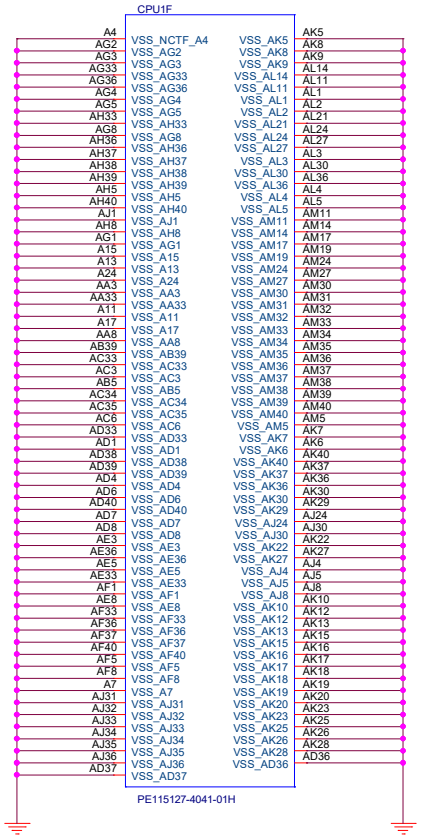
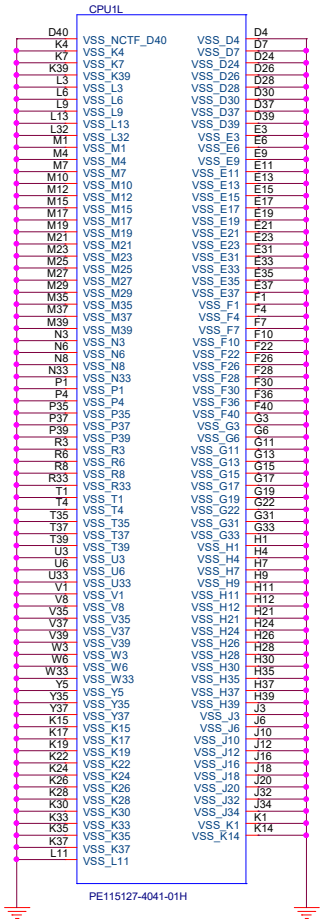
Date: *Thursday, June 13, 2019*	Sheet: 10 of 48	







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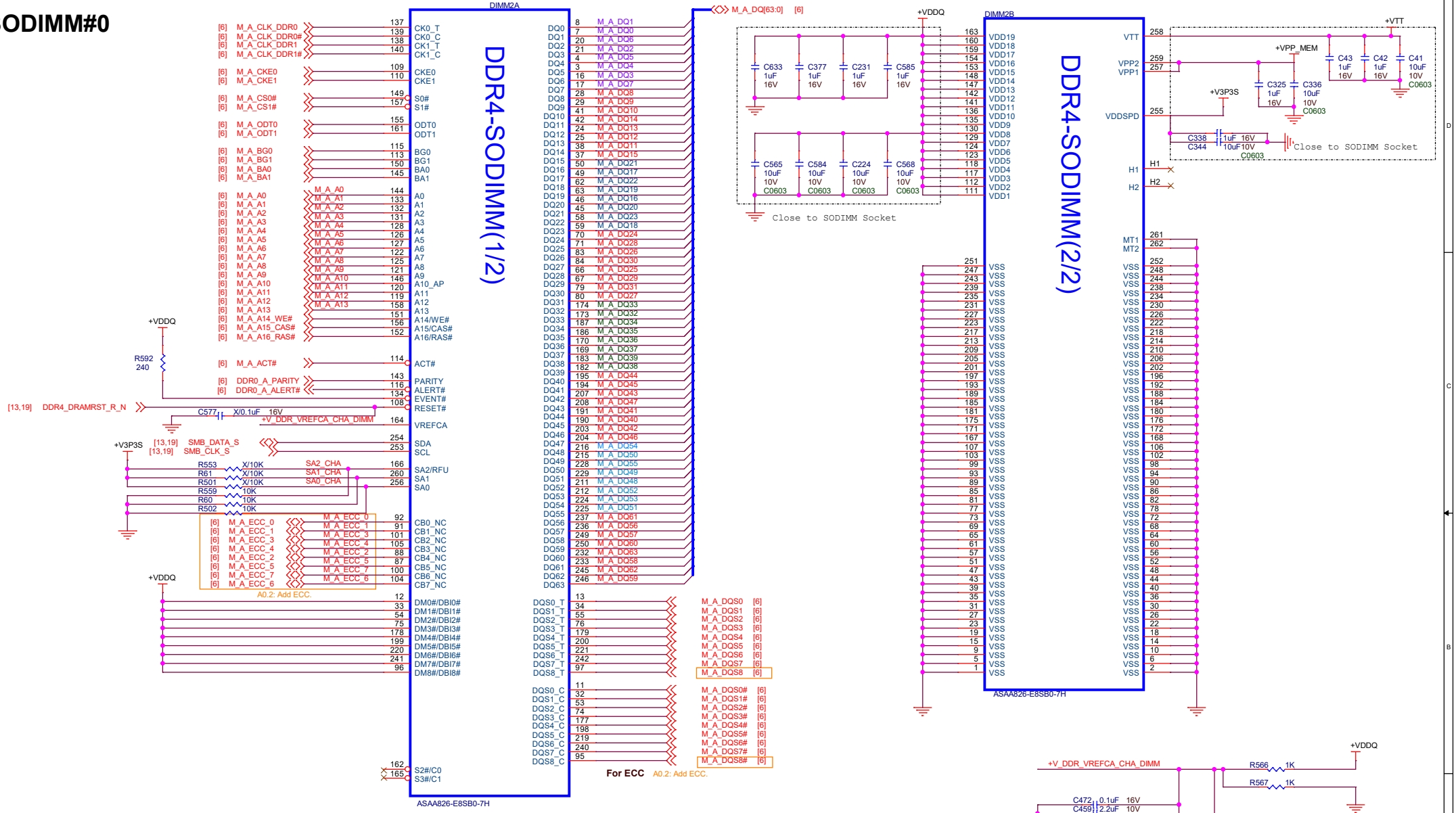
Title
PROCESSOR 7-VSS

Size	Document Number	Rev:
A	**EPIC-CFS7**	**A0.2**

Date: *Thursday, June 13, 2019* Sheet: **11** of **48**

SODIMM#0



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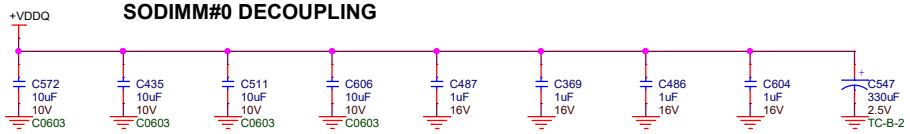

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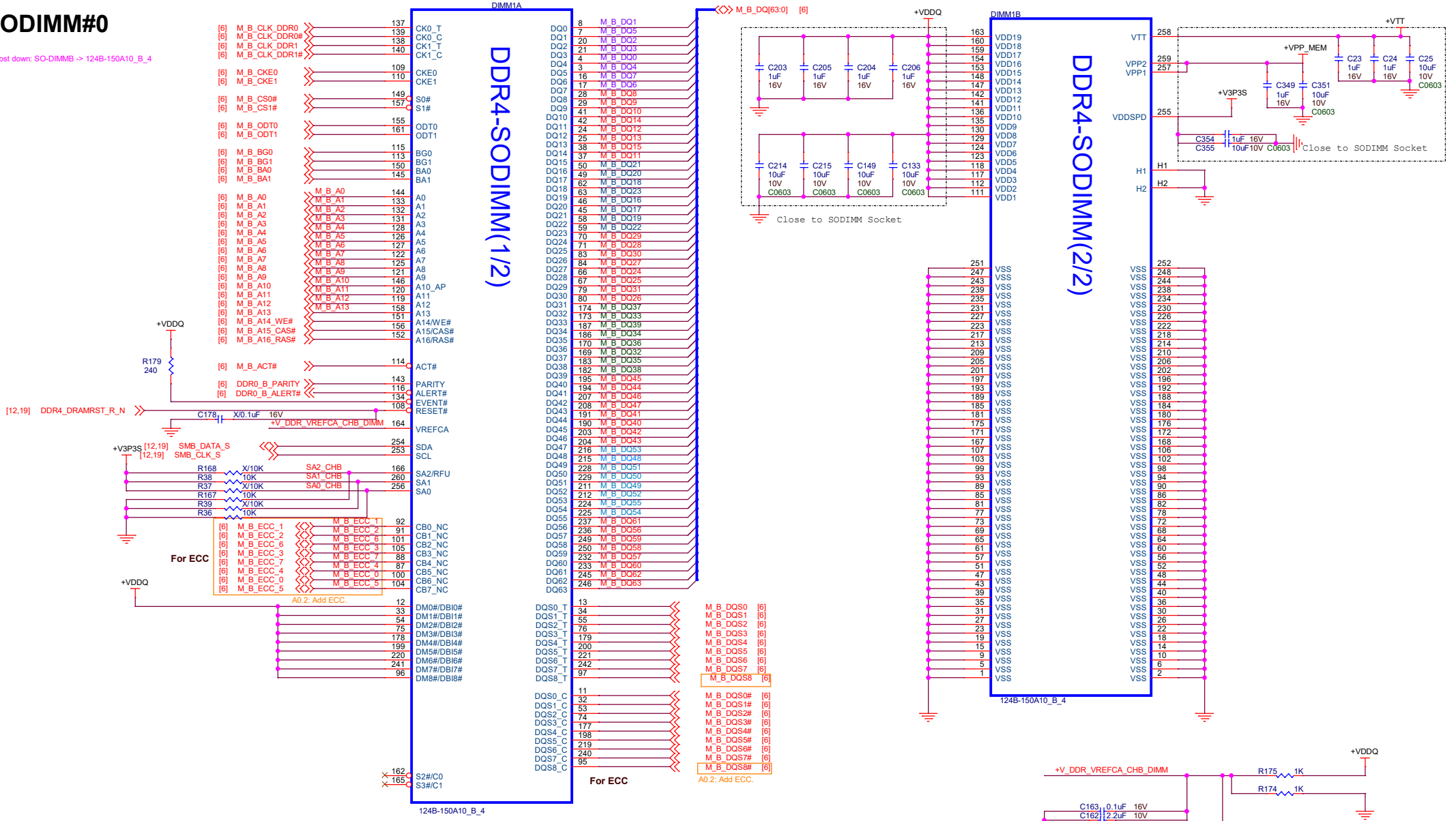
Title: DDR4_SODIMMA

Size: Custom | Document Number: EPIC-CFS7 | Rev: A0.2

Date: Thursday, June 13, 2019 | Sheet: 12 of 48

SODIMM#0

for cost down: SO-DIMMB -> 124B-150A10_B_4



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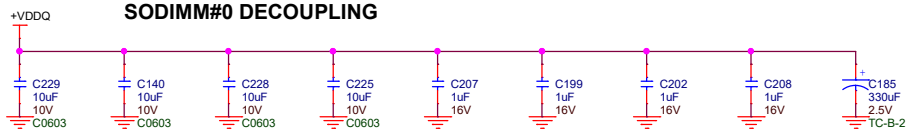

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AAEON An ASUS Company	Title: DDR4_SODIMMB	
	Size: Custom	Document Number: EPIC-CFS7 — Rev: A0.2
	Date: Thursday, June 13, 2019	Sheet: 13 of 48

SPI_IO2

This signal has an internal pull-up.

R649 X/4.7K SPI_IO2

SPI_IO3

This signal has an internal pull-up.

R646 X/4.7K SPI_IO3

GSPI1_MOSI / GPP_B22

This signal has an internal pull-up.

BOOT_BIOS_STRAP
H:LPC
L:SPI

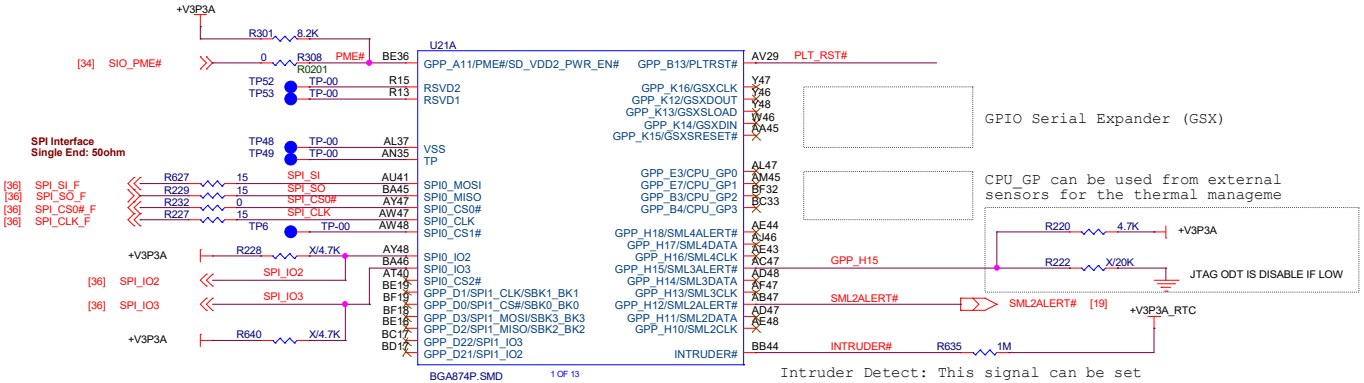
R692 1K BOOT_BIOS_STRAP

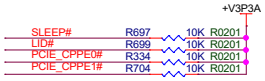
GSPI0_MOSI / GPP_B18

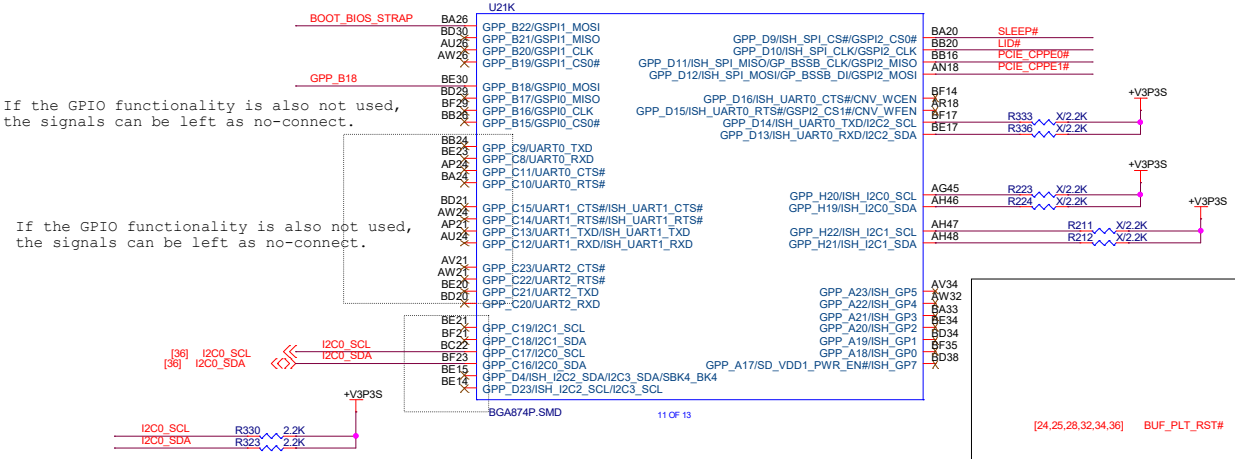
This signal has an internal pull-up.

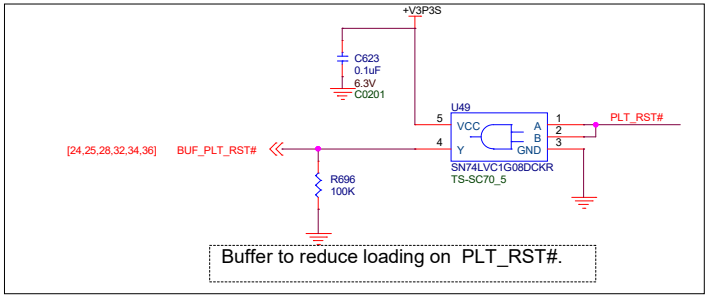
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful
when running ITP/XDP.

R317 1K GPP_B18









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Size: A	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*	Sheet: 14 of 48	

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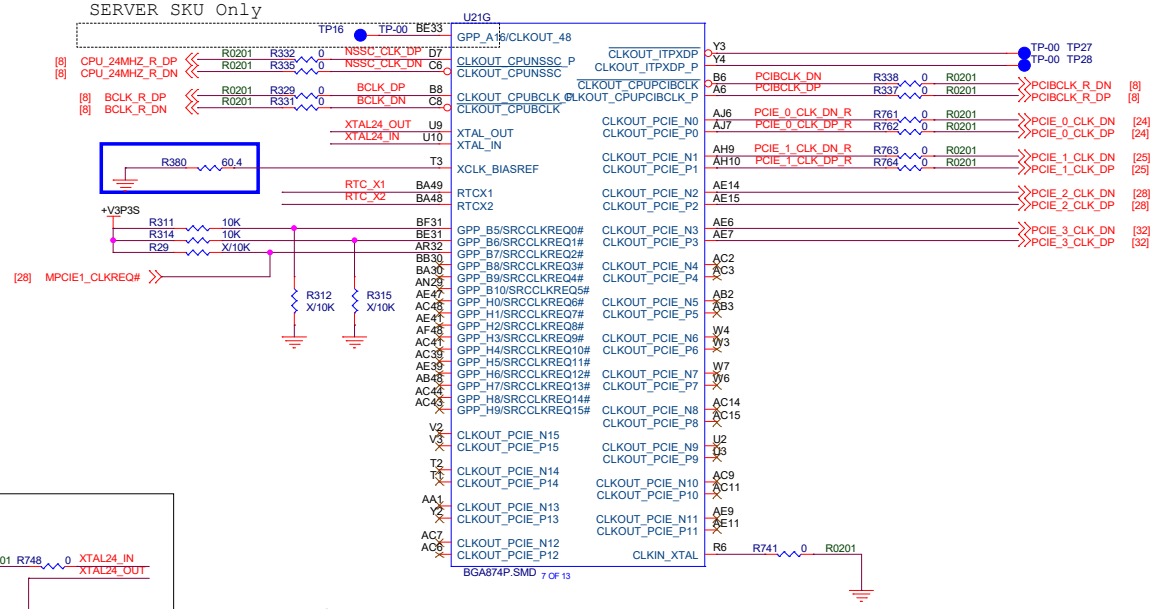
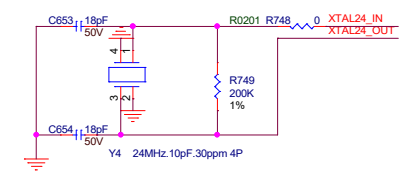


NOTE:

Any differential clock pair not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel ME FW

Any single ended clock signal not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel ME FW.

24Mhz X'tal



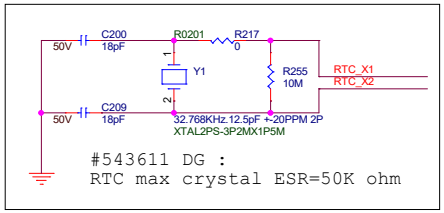


Figure 12-1. Clock Integration Distribution Diagram

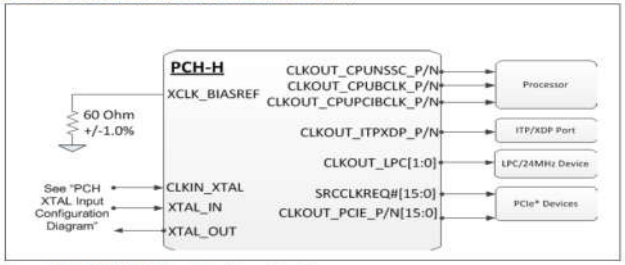
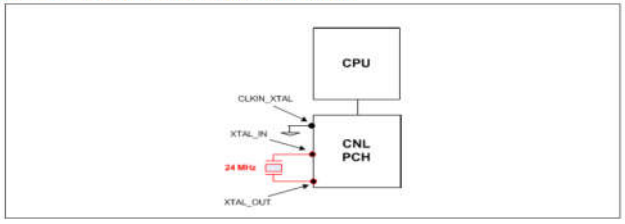


Figure 12-2. PCH XTAL Input Configuration Diagram



<Variant Name>

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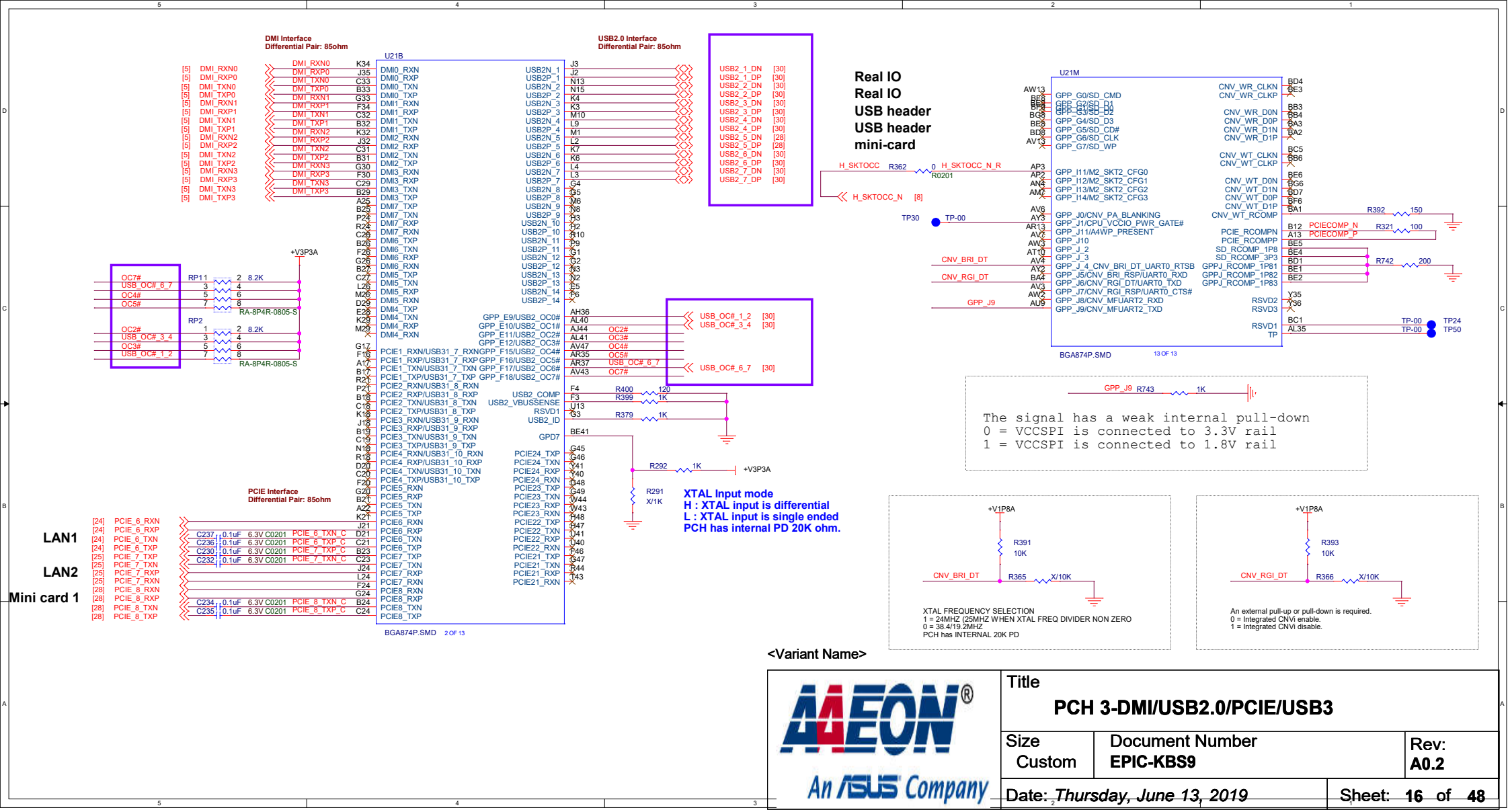
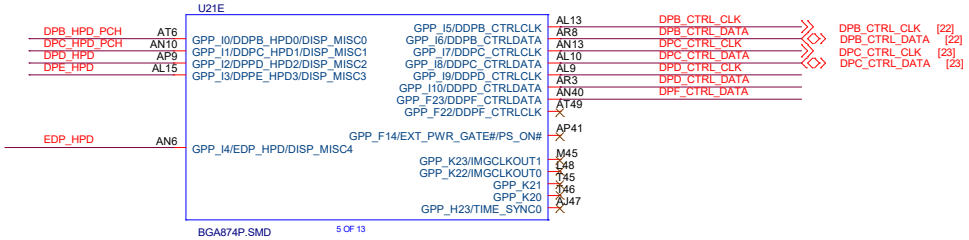
Title		
PCH 2-CLK		
Size: A	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*		Sheet: 15 of 48

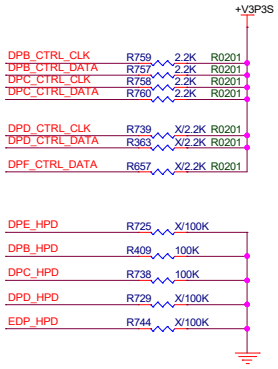

DMI Interface
Differential Pair: 85ohm
USB2.0 Interface
Differential Pair: 85ohm
U21B
BGA874P.SMD 2 OF 13
Real IO
Real IO
USB header
USB header
mini-card
U21M
BGA874P.SMD 13 OF 13
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
XTAL Input mode
H : XTAL input is differential
L : XTAL input is single ended
PCH has internal PD 20K ohm.
PCIE Interface
Differential Pair: 85ohm
LAN1
LAN2
Mini card 1
XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO
0 = 38.4/19.2MHZ
PCH has INTERNAL 20K PD
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
<Variant Name>
Title
PCH 3-DMI/USB2.0/PCIE/USB3
Size
Custom
Document Number
EPIC-KBS9
Rev:
A0.2
Date: Thursday, June 13, 2019
Sheet: 16 of 48

	HPD	DDC	DDI(CPU)
Port1	DDPB_HPD	DDCB	DDI1
Port2	DDPC_HPD	DDCC	DDI2
Port3	DDPD_HPD	DDCD	DDI3

HDMI1
HDMI2

A01 U19E.A13,AR8 and AN13,AL10 net_name exchange (refer PCH defined)_2017-10-24





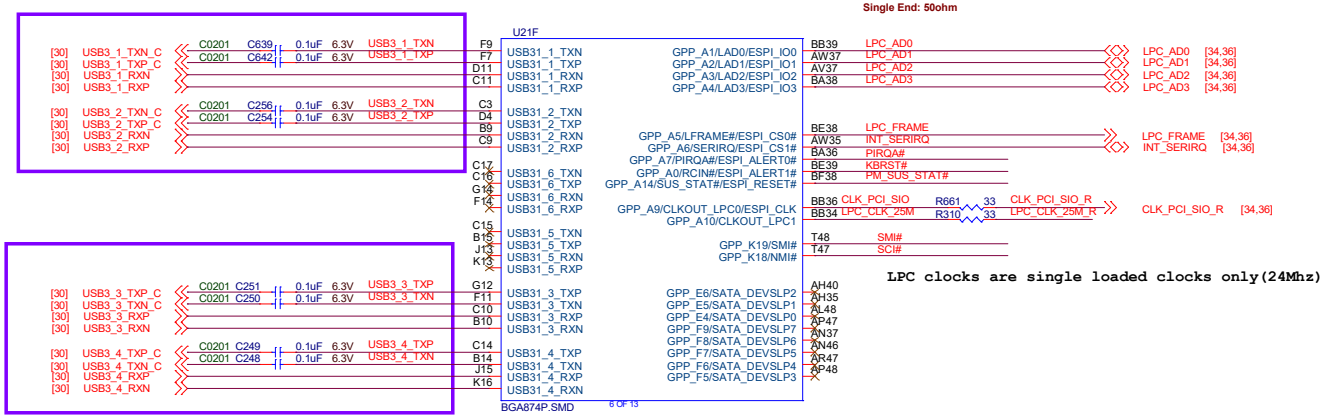
Real IO

Real IO

Internal 3.0

USB3.0 Interface
Differential Pair: 85ohm

LPC
Single End: 50ohm

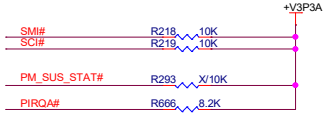


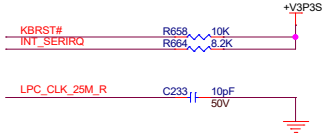
LPC clocks are single loaded clocks only(24Mhz)

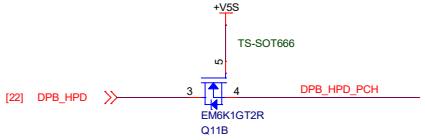
DDPB_CTRLDATA / GPP_I6
This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

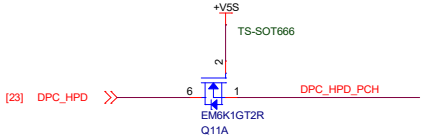
DDPC_CTRLDATA / GPP_I8
This signal has a weak internal pull-down.
0 = Port C is not detected. (Default)
1 = Port C is detected.

DDPD_CTRLDATA / GPP_I10
This signal has a weak internal pull-down.
0 = Port D is not detected. (Default)
1 = Port D is detected.









<Variant Name>

AAEON An ASUS Company

Title
PCH 4-DDI/USB3/LPC/eSPI

Size	Document Number	Rev:
A	EPIC-KBS9	A0.2

Date: *Thursday, June 13, 2019* Sheet: **17** of **48**

CNL PCH H Flexible I/O

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE		SATA 0a	GbE	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5						
Intel® RST Support							No Support				No Support				Yes				No Support				Yes					Yes		

If an AMT capable Intel WLAN device is not implemented, then this signal can be left as NO CONNECT (NC).

PCIE Interface
Differential Pair: 85ohm

Controller Link
The Controller Link is used to manage the wireless LN device

TP25 TP26 TP23 TP5 TP4

U21C

CL_CLK CL_DATA CL_RST#
GPP_K8 GPP_K9 GPP_K10 GPP_K11 GPP_K0 GPP_K1 GPP_K2 GPP_K3 GPP_K4 GPP_K5 GPP_K6 GPP_K7

PCIE9_RXN PCIE9_RXP PCIE9_TXN PCIE9_TXP
PCIE10_RXN PCIE10_RXP PCIE10_TXN PCIE10_TXP
PCIE15_RXN/SATA2_RXN PCIE15_RXP/SATA2_RXP PCIE_15_SATA_2_TXN PCIE15_TXP/SATA2_TXP
PCIE16_RXN/SATA3_RXN PCIE16_RXP/SATA3_RXP PCIE16_TXN/SATA3_TXN PCIE16_TXP/SATA3_TXP
PCIE17_RXN/SATA4_RXN PCIE17_RXP/SATA4_RXP PCIE17_TXN/SATA4_TXN PCIE17_TXP/SATA4_TXP
PCIE18_RXN/SATA5_RXN PCIE18_RXP/SATA5_RXP PCIE18_TXN/SATA5_TXN PCIE18_TXP/SATA5_TXP

PCIE_9_TXN_C_C64 0.1uF 6.3V C0201 PCIE_9_RXN [32]
PCIE_9_TXP_C_C62 0.1uF 6.3V C0201 PCIE_9_RXP [32]
PCIE_9_TXN [32]
PCIE_9_TXP [32]

PCIE_10_TXN_C_C69 0.1uF 6.3V C0201 PCIE_10_RXN [32]
PCIE_10_TXP_C_C65 0.1uF 6.3V C0201 PCIE_10_RXP [32]
PCIE_10_TXN [32]
PCIE_10_TXP [32]

SATA_2_RXN [28]
SATA_2_RXP [28]
SATA_2_TXN [28]
SATA_2_TXP [28]

[32] PCIE_11_TXP C70 0.1uF 6.3V C0201 PCIE_11_TXP_C
[32] PCIE_11_TXN C75 0.1uF 6.3V C0201 PCIE_11_TXN_C
[32] PCIE_11_RXP
[32] PCIE_11_RXN

SGPIO
GPP_F10/SATA_SCLOCK GPP_F11/SATA_SLOAD GPP_F13/SATA_SDATAOUT0 GPP_F12/SATA_SDATAOUT1

STAT3.0 Interface
Differential Pair: 85ohm

[29] SATA_0_TXN
[29] SATA_0_TXP
[29] SATA_0_RXN
[29] SATA_0_RXP

[32] PCIE_12_TXP C78 0.1uF 6.3V C0201 PCIE_12_TXP_C
[32] PCIE_12_TXN C84 0.1uF 6.3V C0201 PCIE_12_TXN_C
[32] PCIE_12_RXP
[32] PCIE_12_RXN

PCIE11_TXP/SATA0A_TXP PCIE11_TXN/SATA0A_TXN PCIE11_RXP/SATA0A_RXP PCIE11_RXN/SATA0A_RXN
PCIE14_TXN/SATA1B_TXN PCIE14_TXP/SATA1B_TXP PCIE14_RXN/SATA1B_RXN PCIE14_RXP/SATA1B_RXP
PCIE13_TXN/SATA0B_TXN PCIE13_TXP/SATA0B_TXP PCIE13_RXN/SATA0B_RXN PCIE13_RXP/SATA0B_RXP
PCIE12_TXP/SATA1A_TXP PCIE12_TXN/SATA1A_TXN PCIE12_RXP/SATA_1A_RXP PCIE12_RXN/SATA1A_RXN
PCIE20_TXP/SATA7_TXP PCIE20_TXN/SATA7_TXN PCIE20_RXP/SATA7_RXP PCIE20_RXN/SATA7_RXN
PCIE19_TXP/SATA6_TXP PCIE19_TXN/SATA6_TXN PCIE19_RXP/SATA6_RXP PCIE19_RXN/SATA6_RXN

GPP_E8/SATA_LED# GPP_E0/SATAXPCIE0/SATAGP0 GPP_E1/SATAXPCIE1/SATAGP1 GPP_E2/SATAXPCIE2/SATAGP2 GPP_F0/SATAXPCIE3/SATAGP_3 GPP_F1/SATAXPCIE4/SATAGP4 GPP_F2/SATAXPCIE5/SATAGP5 GPP_F3/SATAXPCIE6/SATAGP6 GPP_F4/SATAXPCIE7/SATAGP7
GPP_F21/EDP_BKLTCTL GPP_F20/EDP_BKLTEN GPP_F19/EDP_VDDEN
THRMTRIP# PECI PM_SYNC PLTRST_CPU# PM_DOWN

SATA_LED# SATAGP0 SATAGP1 SATAGP2 SATAGP3
EDP_BKLT_CTRL EDP_BKLT_EN EDP_VDD_EN

Default SATAXPCIE is set by a soft strap.

R381 560 PCH_THERMTRIP# [8]
H_PM_SYNC_R R353 33R0201 H_PM_SYNC [8]
PLTRST_CPU#_R R354 0 R0201 PLTRST_CPU# [8]
H_PM_DOWN_R R371 0 R0201 H_PM_DOWN [8]
PCH_PECI [8]
R384 1K

BGA874P.SMD 3 OF 13

+V3P3S
EDP_BKLT_CTRL R230 X/1K
EDP_BKLT_EN R231 X/1K
EDP_VDD_EN R644 X/1K

+V3P3S
SATAGP0 R238 10K R0201
SATAGP1 R239 10K R0201
SATAGP2 R240 10K R0201
SATAGP3 R241 10K R0201

+V3P3S
R225 10K
SATA_LED# SATA_LED# [38]

<Variant Name>

AAEON An ASUS Company

Title		
PCH 5-PCIE/SATA/FAN		
Size A	Document Number EPIC-KBS9	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 18 of 48

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device dr

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.

SML0_ALERT# has a weak internal pull-down resistor (20k ohm nominal) to default LPC is selected for EC

Remove HDA

HDA
Single End: 50ohm

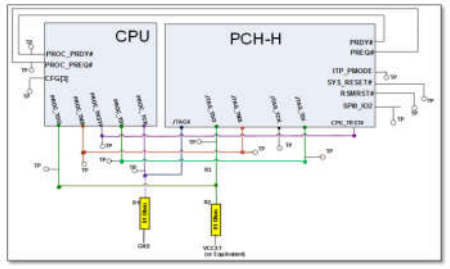
Place close to PCH

I2S/DMIC

(VCCRTC<3.2V)

Chceck Disable or DCI

Implementation of DCI Debug tool



CMOS Control Selection(RTC_RST#)		
1-2	Save CMOS	Default
2-3	Clear CMOS	

Add Test Point:
Location BOT. point to point .60mils

Battery

BP-CR2032-M150-002
3V

SMBus

To DDR

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override)

<Variant Name>

AAEON An ASUS Company	Title: PCH 6-HDA/SMB/MISC/I2S/RTC	
	Size: Custom	Document Number: EPIC-KBS9 — Rev: A0.2
	Date: Thursday, June 13, 2019	Sheet: 19 of 48

+V1P05A
R693 0 +VCCPRIM_1P05
R698 0 +VCCDUSB_1P05
R274 0 +VCCDSW_1P05
R669 0 +VCCCLPLLEBB_1P05
R645 0 +VCCAMPHYPLL_1P05
R407 0 +VCCA_XTAL_1P05
R705 0 +VCCA_SRC_1P05
R747 0 +VCCA_OCPLL1_1P05
R700 0 +VCCA_OC_1P05

+VCCDSW_1P05 — close to BG45 — C219 1uF 6.3V C0201
+VCCA_XTAL_1P05 — C259 22uF 6.3V C0603
+VCCAMPHYPLL_1P05 — C598 22uF 6.3V C0603, C597 1uF 6.3V C0201 — close to D49

+VCCPRIM_1P05 — 5.95A
C626 22uF 6.3V C0603, C612 1uF 6.3V C0201
C616 1uF 6.3V C0201, C613 1uF 6.3V C0201
C617 22uF 6.3V C0603, C647 1uF 6.3V C0201

U21H — BGA874P.SMD — 8 OF 13

AA22	VCCPRIM_1P051	VCCPRIM_3P32	AW9 — C645 1uF 16V
AA23	VCCPRIM_1P052	DCPRTC1	BF47 VCC_RTCEXT_CAP
AB20	VCCPRIM_1P053	DCPRTC2	BG47 — C222 1uF 16V
AB22	VCCPRIM_1P054	VCCPRIM_3P35	V23 — +VCCPRIM_3P3
AB23	VCCPRIM_1P055	VCCSPI	AN44 — +V3P3A_V1P8A_PCH_SPI
AB27	VCCPRIM_1P056	VCCRTC1	BC49 — +V3P3A_RTC
AB28	VCCPRIM_1P057	VCCRTC2	BD49
AB30	VCCPRIM_1P058	VCCPGPPG_3P3	AN21 — +VCCPGPPC_G_3P3
AD20	VCCPRIM_1P059	VCCPRIM_3P33	AY8
AD23	VCCPRIM_1P0510	VCCPRIM_3P34	BB7
AD27	VCCPRIM_1P0511	VCCPGPPHK1	AC35
AD28	VCCPRIM_1P0512	VCCPGPPHK2	AC36 — +V3P3A_V1P8A_VCCPGPPHK
AD30	VCCPRIM_1P0513	VCCPGPPEF1	AE35 — C607 0.1uF 6.3V C0201
AF23	VCCPRIM_1P0516	VCCPGPPEF2	AE36 — +V3P3A_V1P8A_VCCPGPPEF
AF27	VCCPRIM_1P0517	VCCPGPPD	AN24 — +V3P3A_V1P8A_VCCPGPPD
AF30	VCCPRIM_1P0518	VCCPGPPBC1	AN26
U26		VCCPGPPBC2	AP26 — +V3P3A_V1P8A_VCCPGPPBC
U29	VCCPRIM_1P0523	VCCPGPPA	AN32 — +V3P3A_V1P8A_VCCPGPPA
V25	VCCPRIM_1P0524	VCCPRIM_3P31	AT44 — +VCCPRIM_3P3
V27	VCCPRIM_1P0525	VCCDSW_3P31	BE48
V28	VCCPRIM_1P0526	VCCDSW_3P32	BE49 — +VCCPDSW_3P3
V30	VCCPRIM_1P0527	VCCHDA	BB14 — +V3P3A_V1P8A_VCCPAZIO
V31	VCCPRIM_1P0528	VCCPRIM_1P83	AG19
AD31	VCCPRIM_1P0529	VCCPRIM_1P84	AG20
AE17	VCCPRIM_1P0514	VCCPRIM_1P85	AN15
	VCCPRIM_1P0515	VCCPRIM_1P86	AR15
W22	VCCDUSB_1P051	VCCPRIM_1P87	BB11
W23	VCCDUSB_1P052	VCCPRIM_1P81	AF19
BG45	VCCDSW_1P051	VCCPRIM_1P82	AF20
BG46	VCCDSW_1P052	VCCPRIM_1P0520	AG31
W31	VCCPRIM_MPHY_1P05	VCCPRIM_1P0519	AF31
D1	VCCPRIM_1P0521	VCCPRIM_1P241	AK22
E1	VCCPRIM_1P0522	VCCPRIM_1P242	AK23 — +V1P24A
C49	VCCAMPHYPLL_1P051	VCCDPHY_1P241	AJ22
D49	VCCAMPHYPLL_1P052	VCCDPHY_1P242	AJ23
E49	VCCAMPHYPLL_1P053	VCCDPHY_1P243	BG5 — +V1P24A_MAR
P2	VCCA_XTAL_1P051	VCCMPHY_SENSE	K47 TP-00 TP3
P3	VCCA_XTAL_1P052	VSSMPHY_SENSE	K46 TP-00 TP2
W19	VCCA_SRC_1P051		
W20	VCCA_SRC_1P052		
C1	VCCAPLL_1P054		
C2	VCCAPLL_1P055		
V19	VCCA_BCLK_1P05		
B1	VCCAPLL_1P051		
B2	VCCAPLL_1P052		
B3	VCCAPLL_1P053		

+VCCDUSB_1P05 — C627 1uF 6.3V C0201
+VCCDSW_1P05
+VCCCLPLLEBB_1P05
+VCCPRIM_1P05
+VCCAMPHYPLL_1P05
+VCCA_XTAL_1P05
+VCCA_SRC_1P05
+VCCA_OCPLL1_1P05 — C649 1uF 6.3V C0201
+VCCA_OC_1P05
+VCCA_OCPLL1_1P05 — C648 1uF 6.3V C0201, C650 1uF 6.3V C0201

close to BC49 , BD49 — C595 0.1uF 6.3V, C592 1uF 16V — +V3P3A_RTC

+VCCPRIM_3P3 — close to AY8 , BB7 — C622 0.1uF 6.3V C0201, C599 0.1uF 6.3V C0201

C605 0.1uF 6.3V C0201

C217 X/0.1uF 6.3V C0201

+V1P8A — R703 0 R0603 — +VCCPHVLDO_1P8 — R702 0 — +VCCPRIM_1P05

C258 4.7uF 16V — close to BG5

For CNVi

Internal LDO

+V3P3A
R740 0 R0603 +VCCPRIM_3P3
R226 0 +V3P3A_V1P8A_PCH_SPI
R701 0 +VCCPGPPC_G_3P3
R668 0 +V3P3A_V1P8A_VCCPGPPHK
R663 0 +V3P3A_V1P8A_VCCPGPPEF
R694 0 +V3P3A_V1P8A_VCCPGPPD
R695 0 +V3P3A_V1P8A_VCCPGPPBC
R667 0 +V3P3A_V1P8A_VCCPGPPA
R268 0 +VCCPDSW_3P3
R339 0 +V3P3A_V1P8A_VCCPAZIO

+VCCPRIM_1P8 — close to AG19 — C634 4.7uF 16V

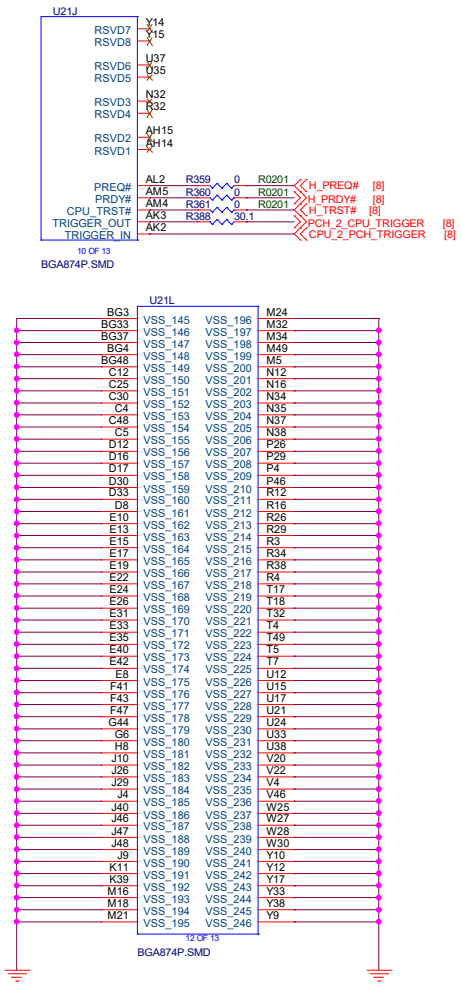
+V1P24A — R350 X/0 — +V1P24A_MAR

HS2 — PCH Heat Sink
(TF)Metal.Al.Heat Sink.27*27*15mm.Rev.0.0.for GENE-QM67

<Variant Name>

AAEON An ASUS Company

Title: PCH 7-PWR		
Size: B	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 20 of 48



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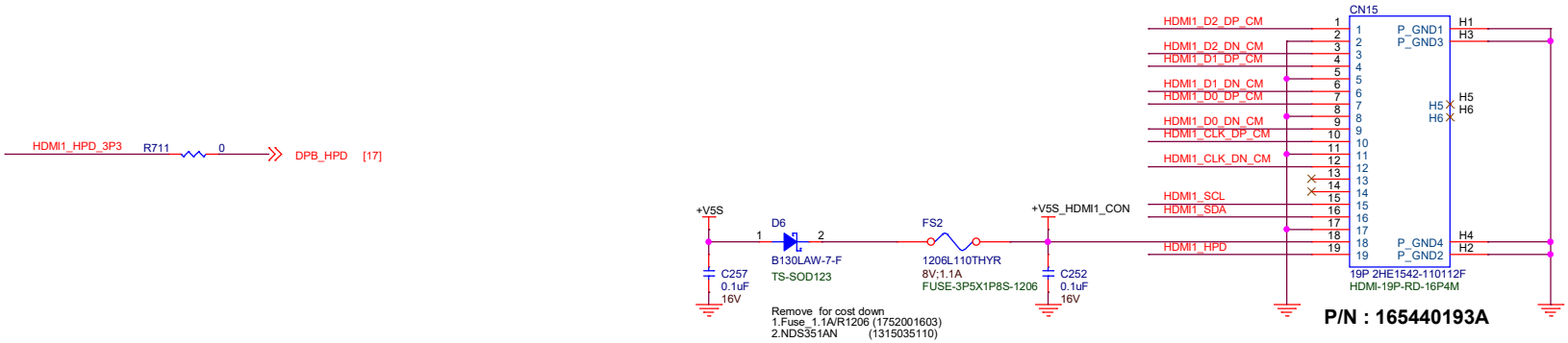
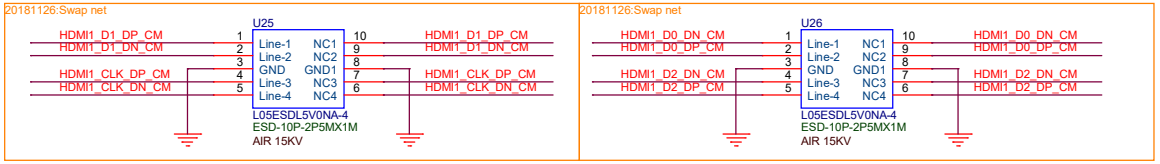
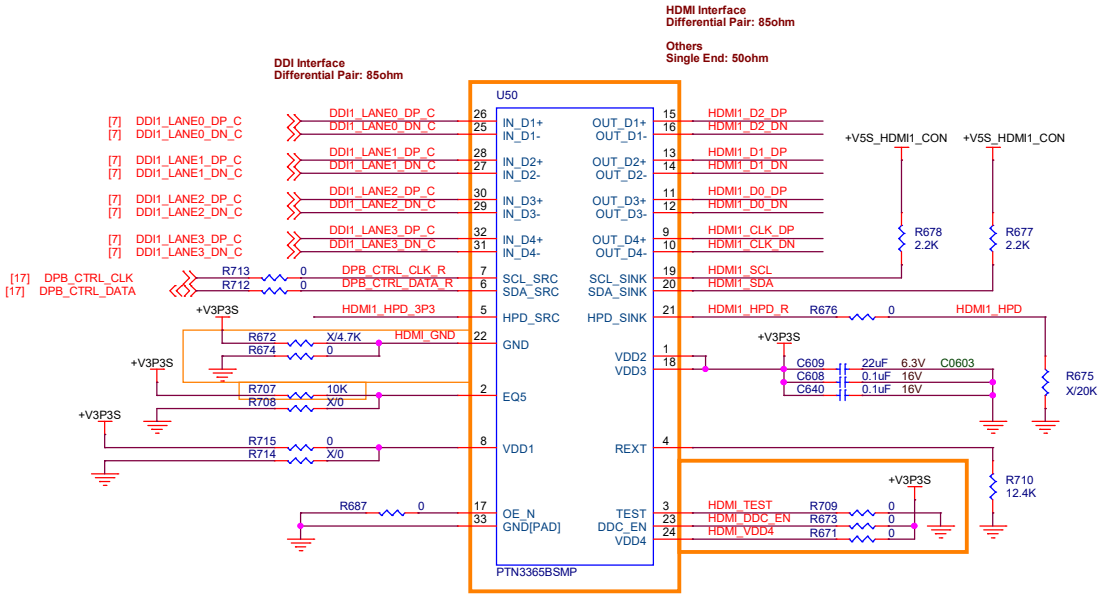
AAEON® An ASUS Company

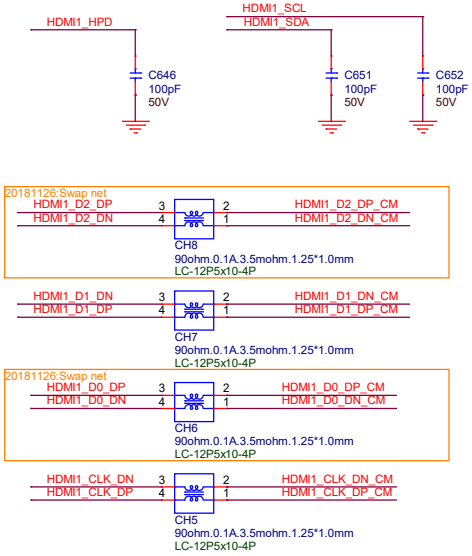
Title: **PCH 8-VSS**		
Size: A	Document Number: **EPIC-CFS7**	Rev: **A0.2**
Date: *Thursday, June 13, 2019*	Sheet: **21** of **48**	

HDMI









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An ASUS Company

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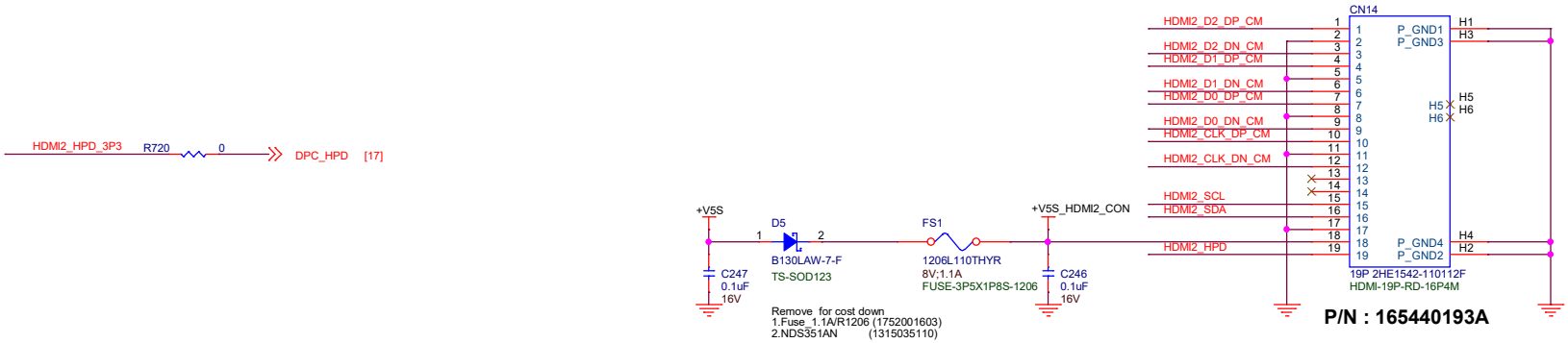
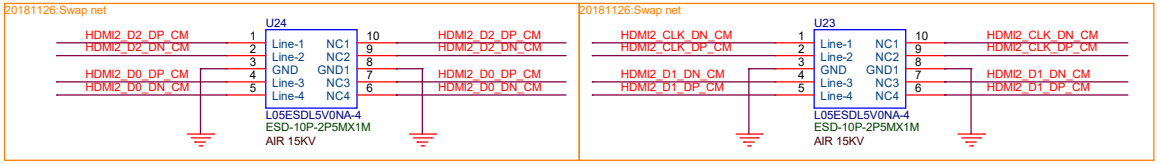
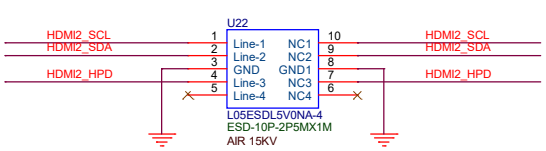
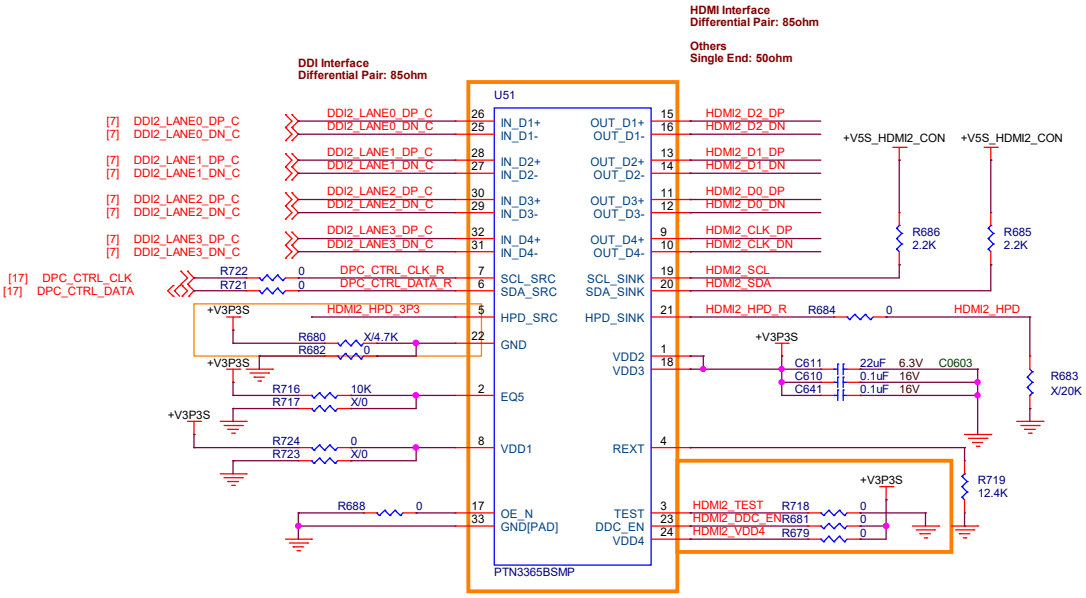
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 22 of 48

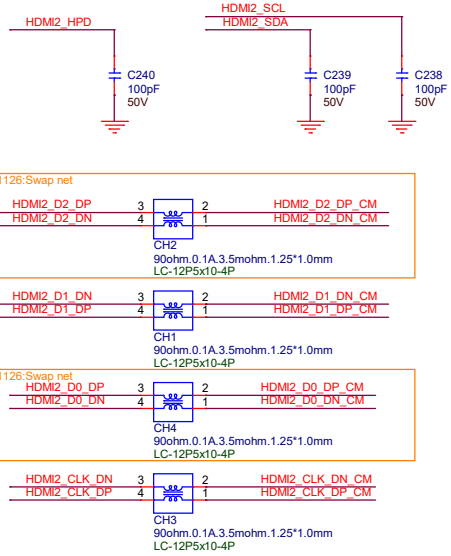
HDMI











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AAEON An ASUS Company

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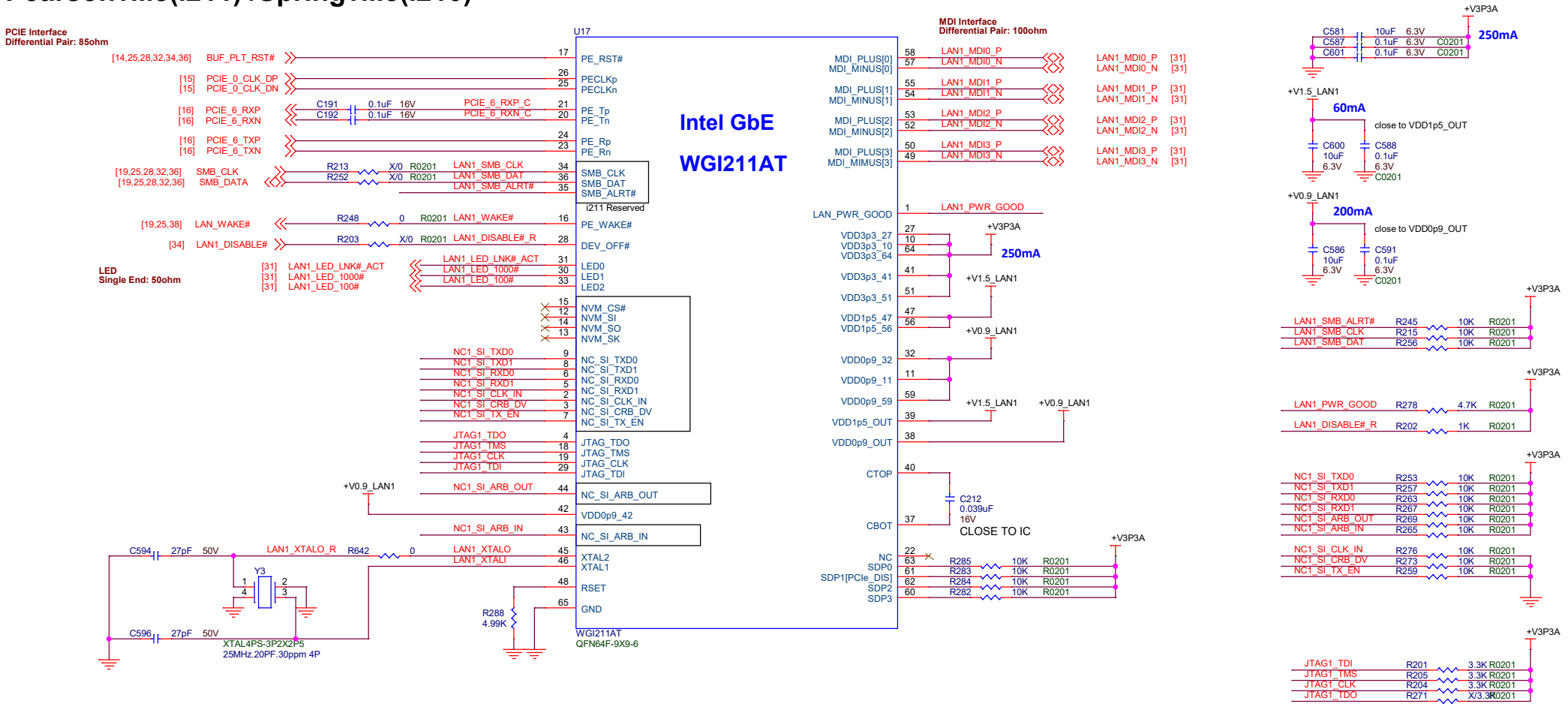
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 23 of 48

Pearsonville(i211) /Springville(i210)



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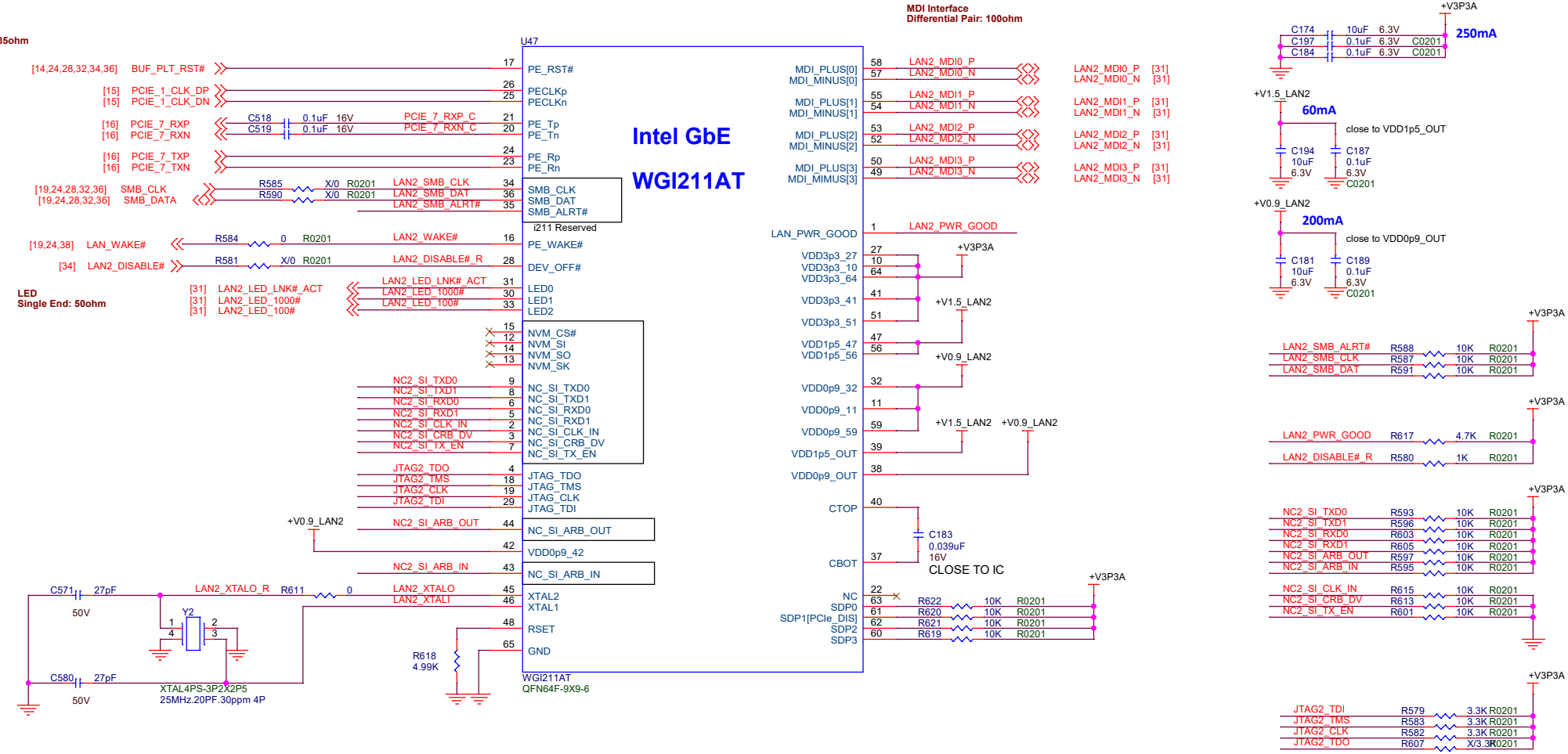
AAEON An ASUS Company	Title: LAN1_INTEL I211	
	Size: Custom	Document Number: EPIC-CFS7 — Rev: A0.2
	Date: Thursday, June 13, 2019	Sheet: 24 of 48

Pearsonville(i211) /Springville(i210)



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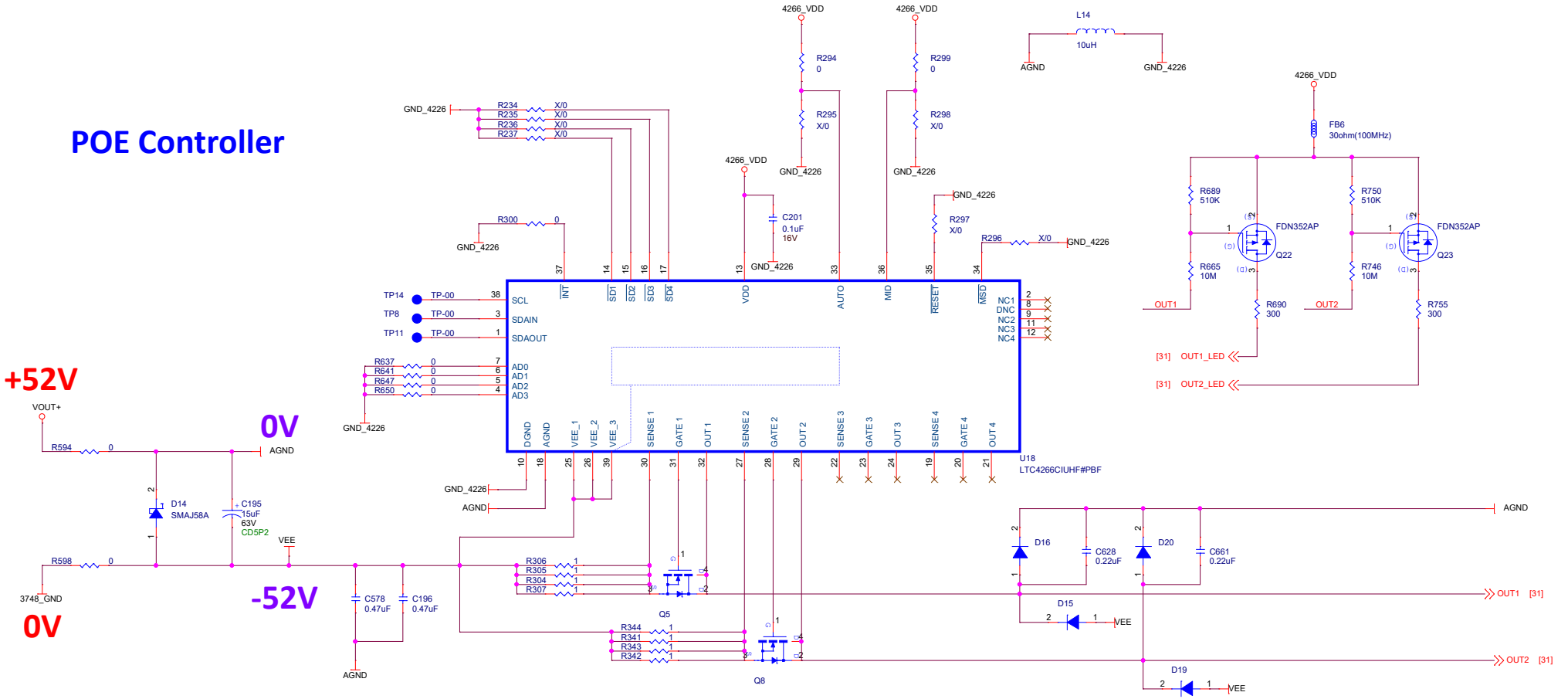
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019	Sheet: 25 of 48	

POE Controller



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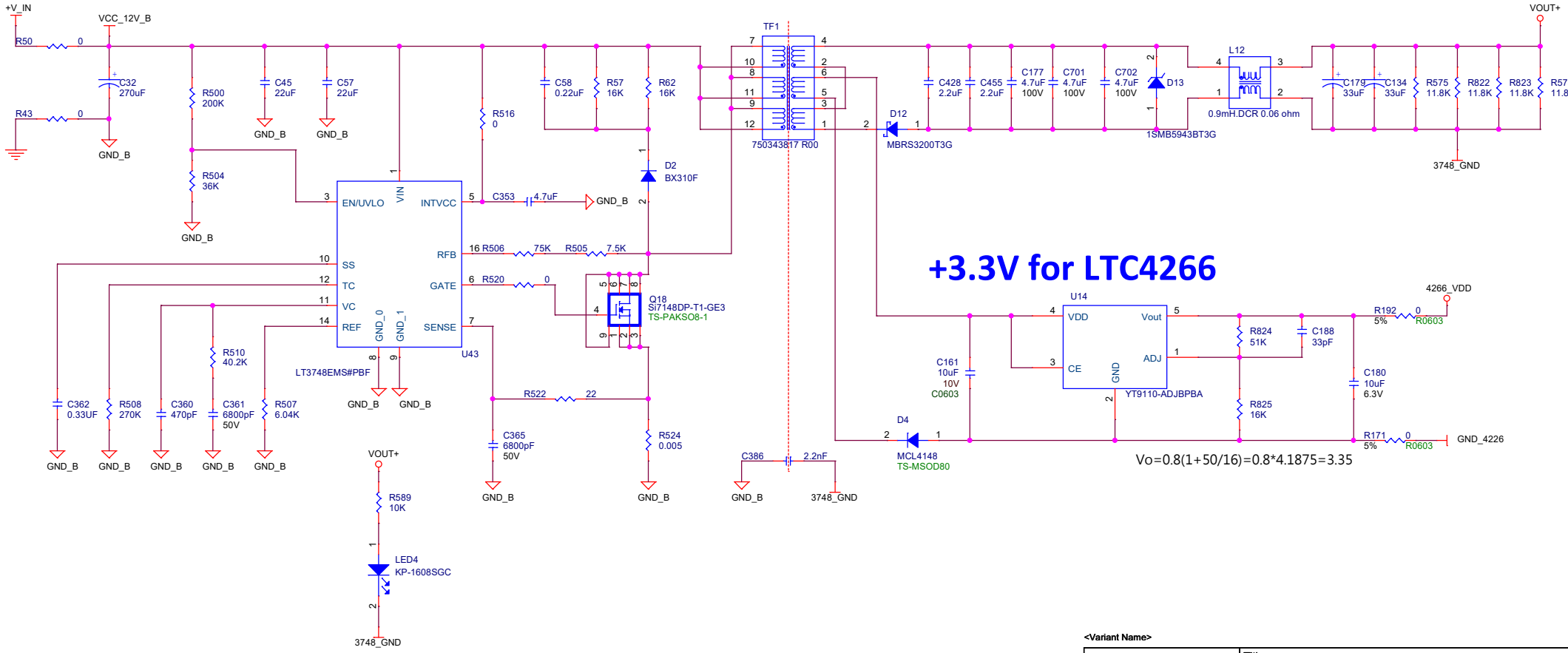
	Date: Thursday, June 13, 2019	Sheet: 26 of 48



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AAEON An ASUS Company

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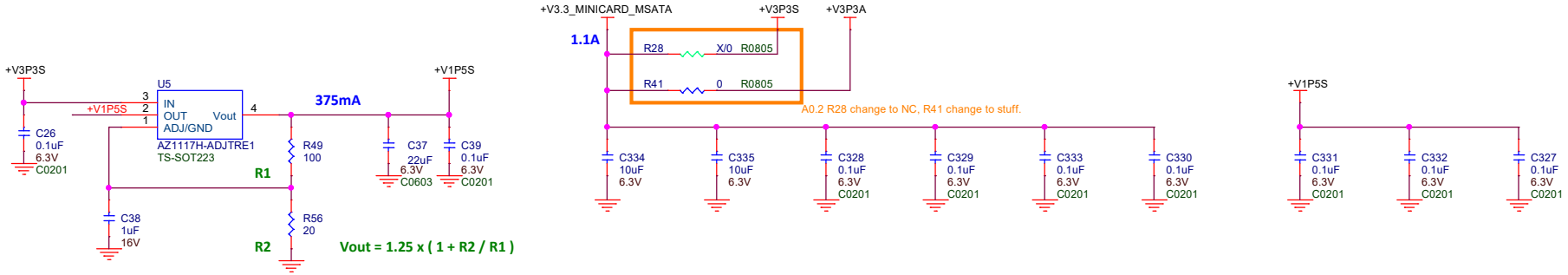
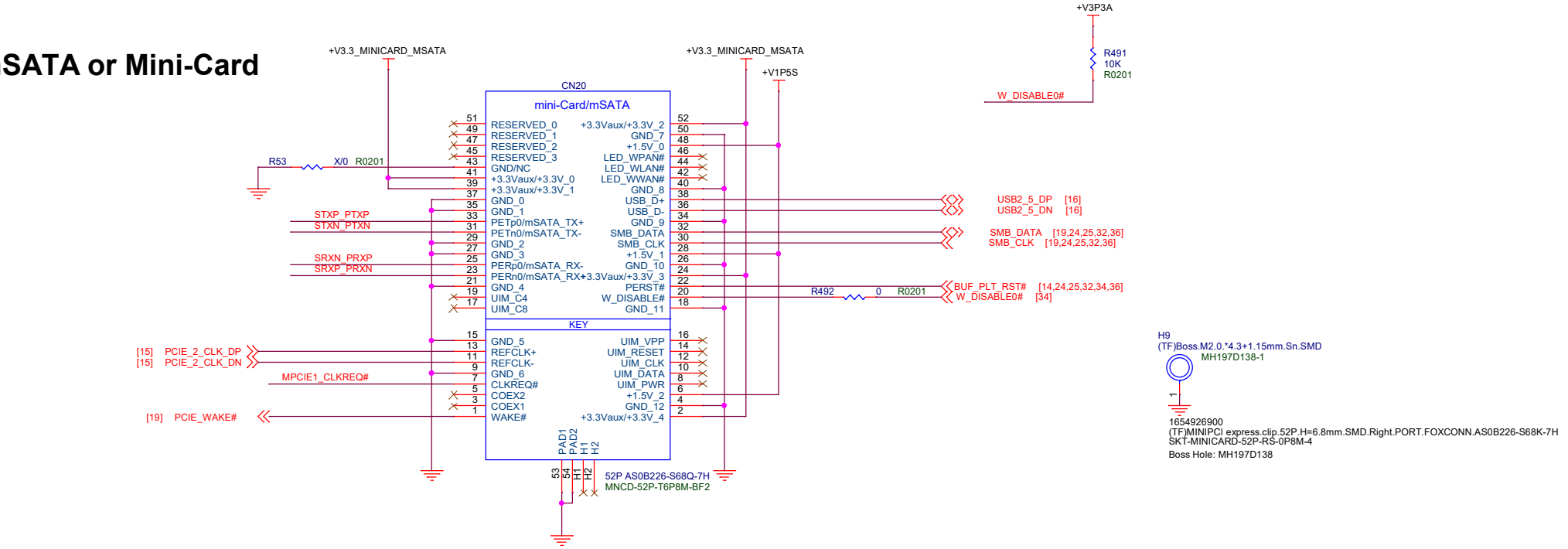
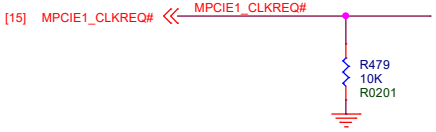
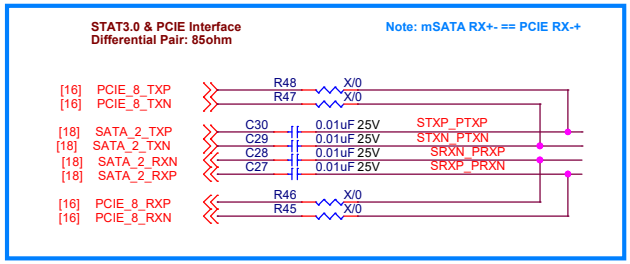
Date: *Thursday, June 13, 2019*	Sheet: 27 of 48	



mSATA or Mini-Card







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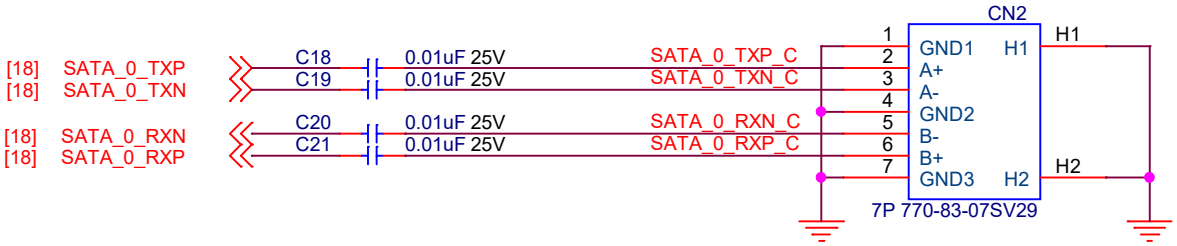
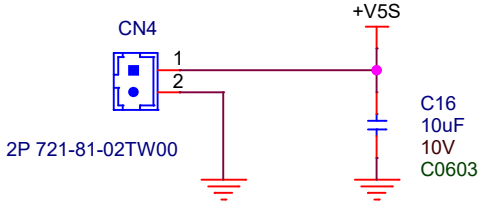
AAEON An ASUS Company

Title: MINI CARD & mSATA		
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019	Sheet: 28 of 48	

SATA 3.0

STAT3.0 Interface
Differential Pair: 85ohm





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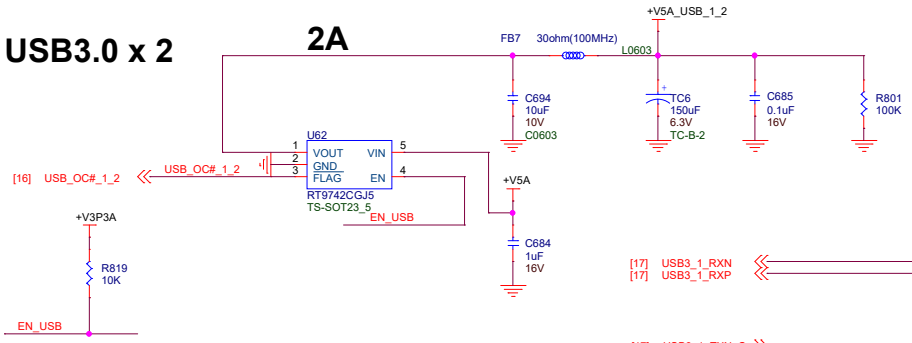
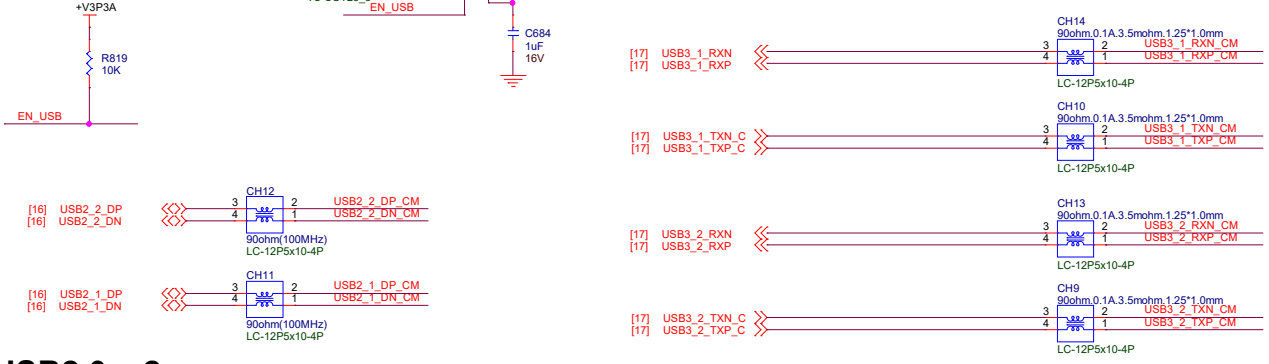
AAEON An ASUS Company

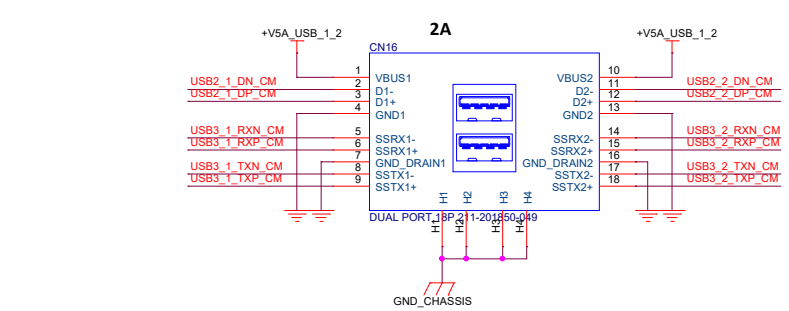
Title: **SATA**		
Size: A	Document Number: **EPIC-CFS7**	Rev: **A0.2**
Date: *Thursday, June 13, 2019*	Sheet: **29** of **48**	

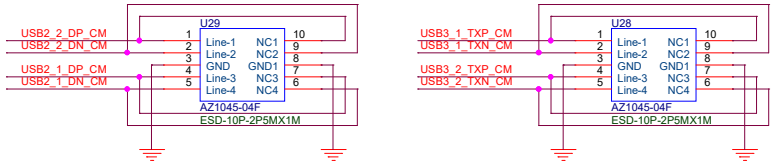
USB3.0 x 2

2A



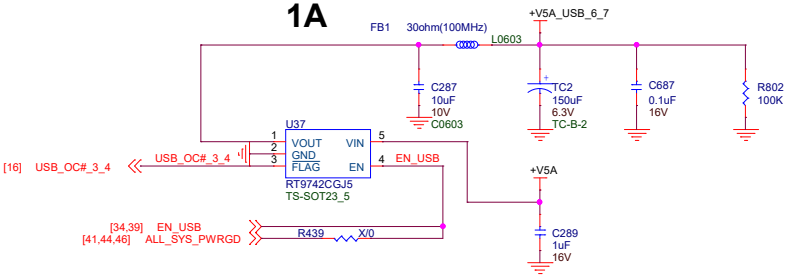


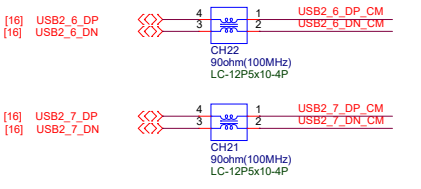


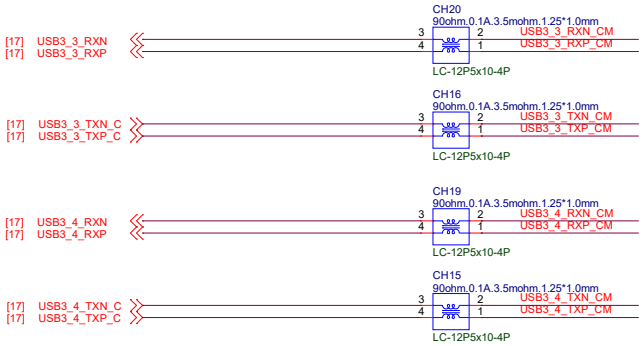


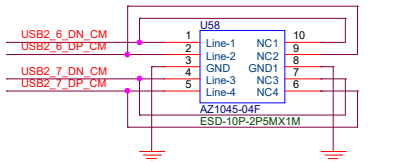
USB2.0 x 2

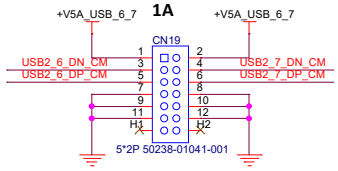
1A





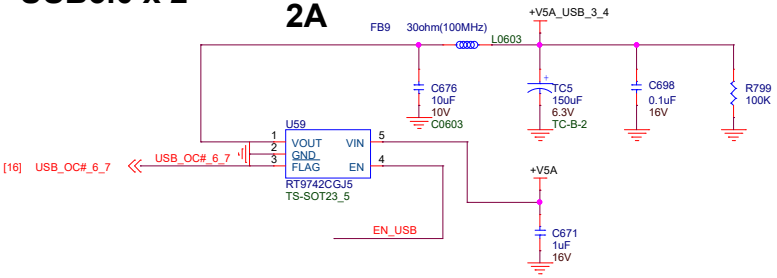


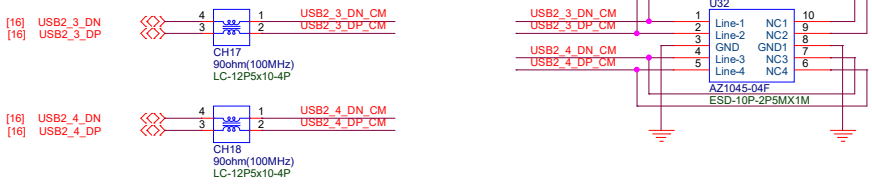


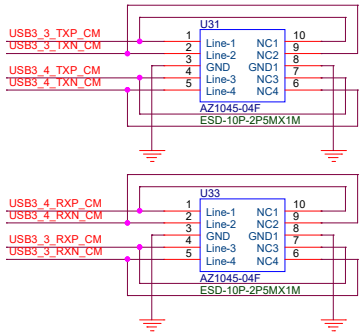


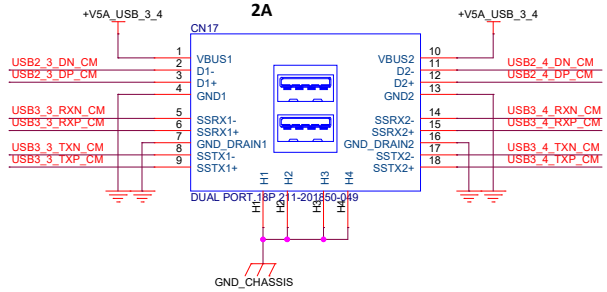
USB3.0 x 2

2A









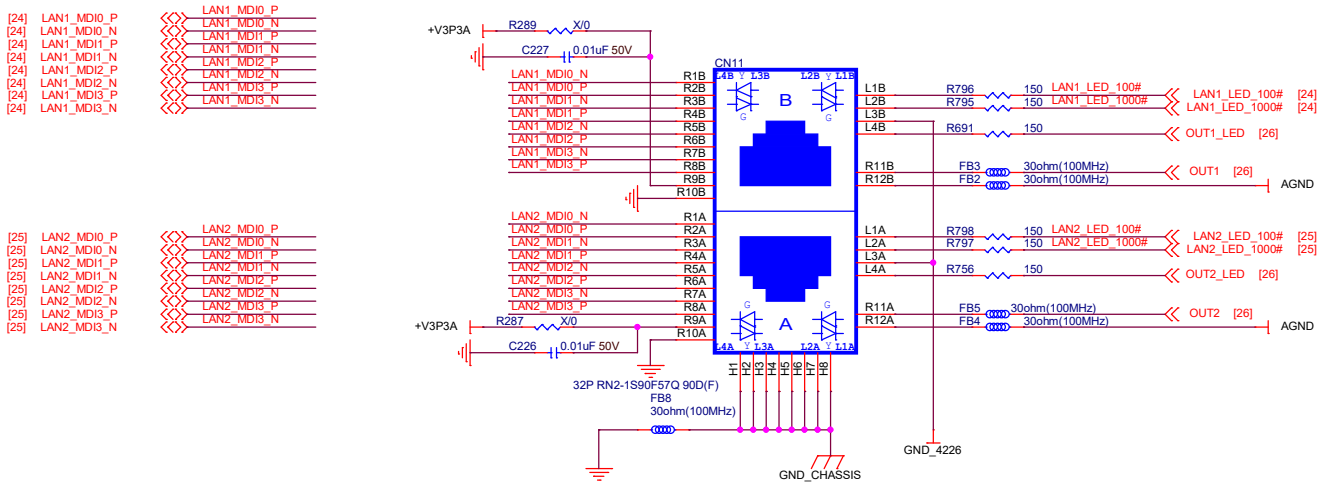
<Variant Name>

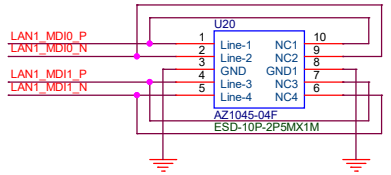
AAEON An ASUS Company	Title: USB	
	Size: Custom	Document Number: EPIC-CFS7 — Rev: A0.2
	Date: Thursday, June 13, 2019	Sheet: 30 of 48

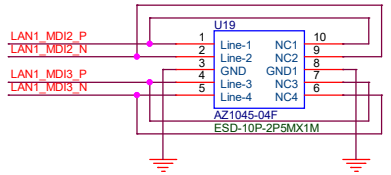
RJ45

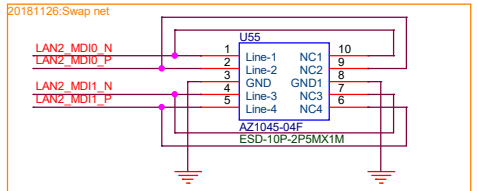
LED
Single End: 50ohm

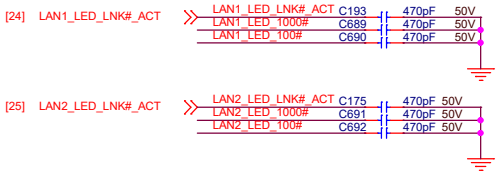
MDI Interface
Differential Pair: 100ohm

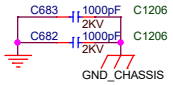












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AAEON An ASUS Company

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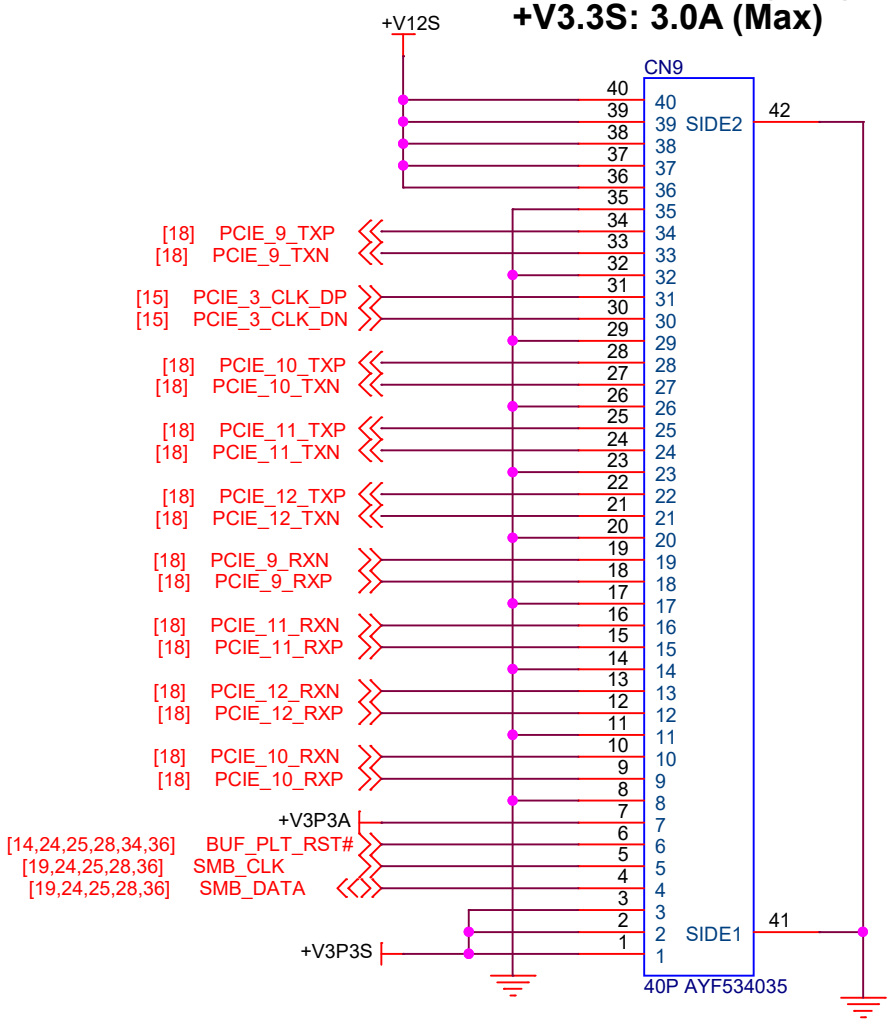
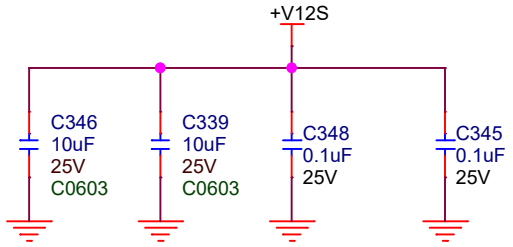
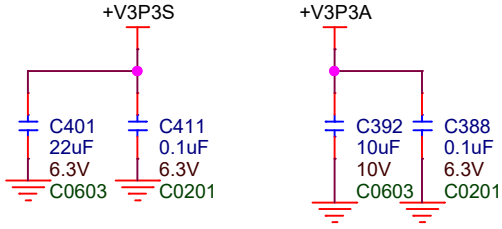
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 31 of 48

20181126:Swap net

+V12S: 2.1A (Max)
+V3.3A: 0.375A(Max)
+V3.3S: 3.0A (Max)







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AAEON An ASUS Company

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Size: A	Document Number: **EPIC-CFS7**	Rev: **A0.2**
Date: *Thursday, June 13, 2019*	Sheet: **32** of **48**	

Remove HD AUDIO ALC269

<Variant Name>

AAEON An ASUS Company

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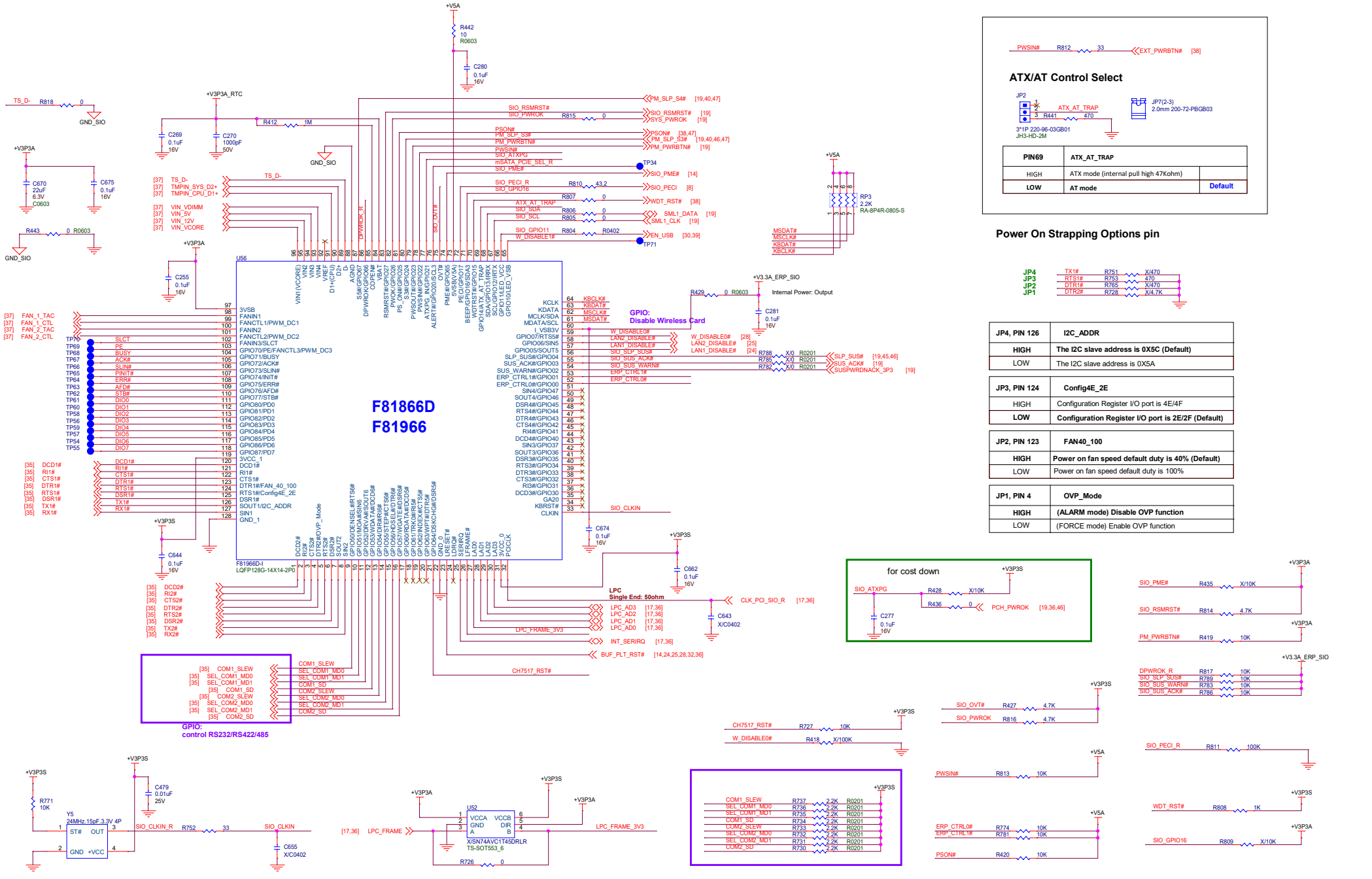
Date: *Thursday, June 13, 2019*	Sheet: 33 of 48	


F81866D
F81966
U56
3VSB
FANIN1
FANCTL1/PWM_DC1
FANIN2
FANCTL2/PWM_DC2
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GPIO70/PEF/FANCTL3/PWM_DC3
GPIO71/BUSY
GPIO72/ACK#
GPIO73/SLIN#
GPIO74/INIT#
GPIO75/ERR#
GPIO76/AFD#
GPIO77/STB#
GPIO80/PD0
GPIO81/PD1
GPIO82/PD2
GPIO83/PD3
GPIO84/PD4
GPIO85/PD5
GPIO86/PD6
GPIO87/PD7
3VCC_1
DCD1#
RI1#
CTS1#
DTR1#/FAN_40_100
RTS1#/Config4E_2E
DSR1#
SOUT1/I2C_ADDR
SIN1
GND_1
F81966D-1
LQFP128G-14X14-2P0
GPIO:
Disable Wireless Card
GPIO:
control RS232/RS422/485
LPC
Single End: 50ohm
for cost down
ATX/AT Control Select
Power On Strapping Options pin
JP4
JP3
JP2
JP1
PIN69
ATX_AT_TRAP
HIGH
ATX mode (internal pull high 47Kohm)
LOW
AT mode
Default
JP4, PIN 126
I2C_ADDR
HIGH
The I2C slave address is 0X5C (Default)
LOW
The I2C slave address is 0X5A
JP3, PIN 124
Config4E_2E
HIGH
Configuration Register I/O port is 4E/4F
LOW
Configuration Register I/O port is 2E/2F (Default)
JP2, PIN 123
FAN40_100
HIGH
Power on fan speed default duty is 40% (Default)
LOW
Power on fan speed default duty is 100%
JP1, PIN 4
OVP_Mode
HIGH
(ALARM mode) Disable OVP function
LOW
(FORCE mode) Enable OVP function
<Variant Name>
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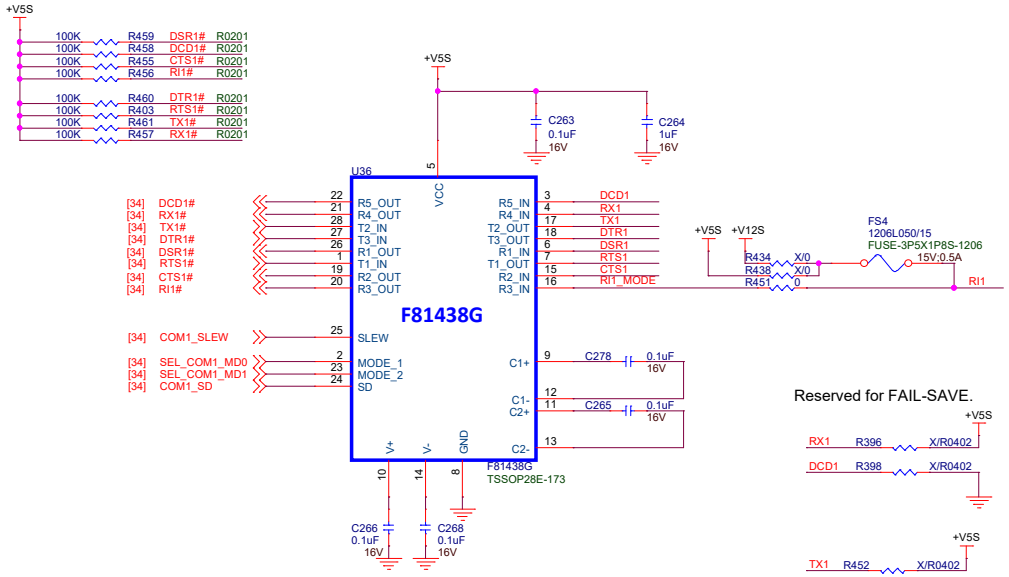
SUPERIO_FINTEK 81966
Size
Custom
Document Number
EPIC-CFS7
Rev:
A0.2
Date: Thursday, June 13, 2019
Sheet: 34 of 48
AAEON
An ASUS Company

COM1



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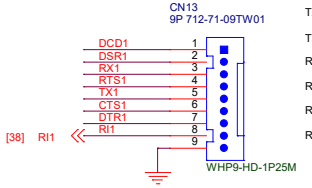
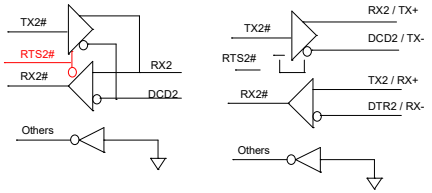


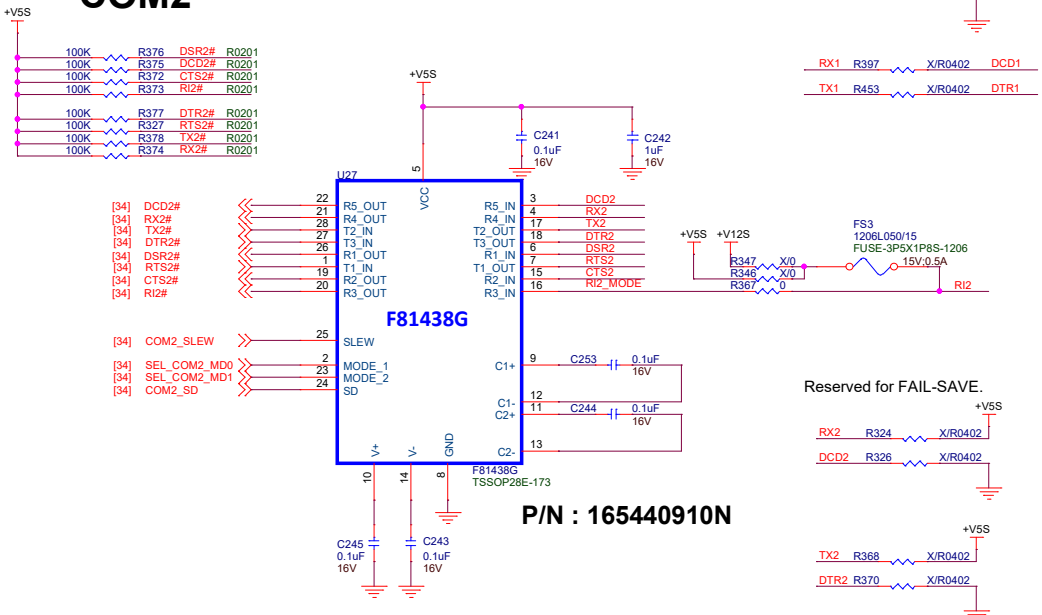
Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

Pin Mapping			
	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

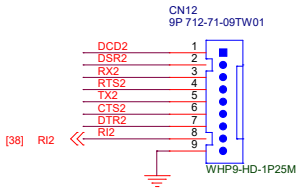
Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE



COM2



Reserved for FAIL-SAVE.

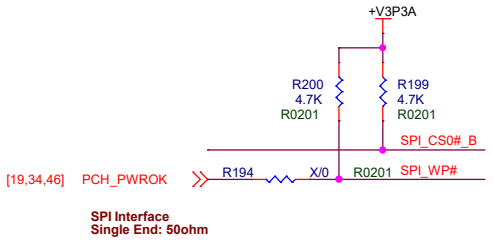


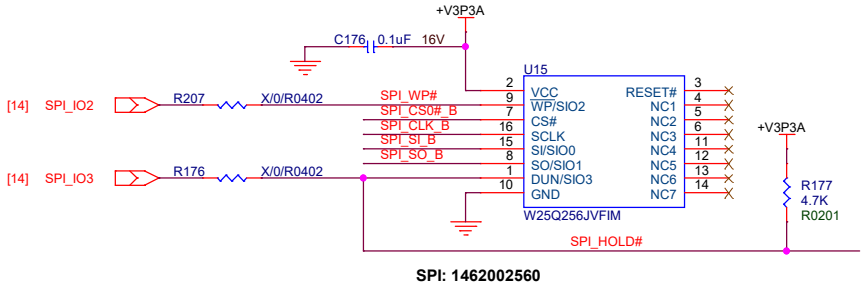
P/N : 165440910N

<Variant Name>

AAEON An ASUS Company	Title: COM1~COM2	
	Size: Custom / Document Number: EPIC-CFS7	Rev: A0.2
	Date: Thursday, June 13, 2019	Sheet: 35 of 48

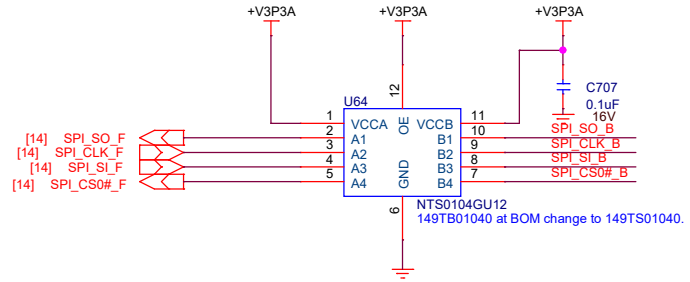
SPI BIOS

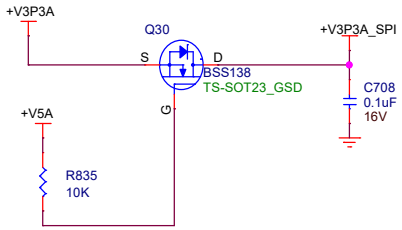


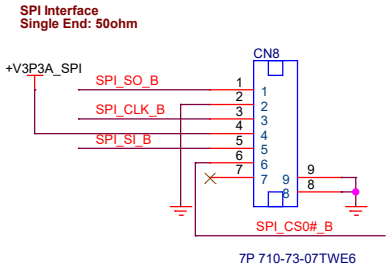


SPI: 1462002560

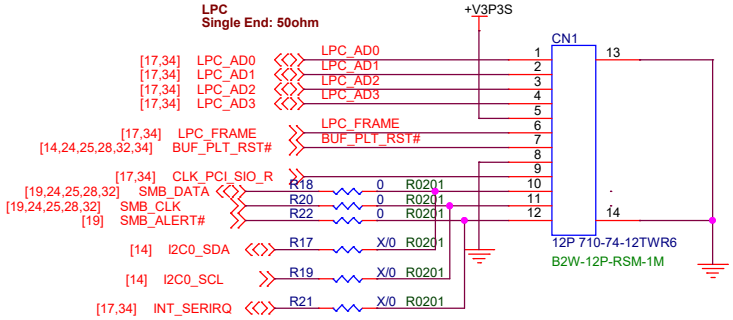
A0.2 Add

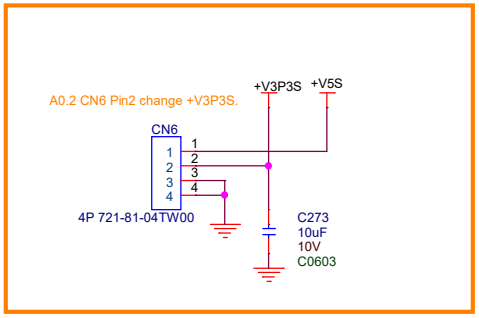






LPC Connector

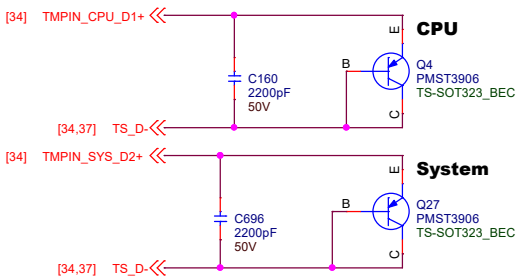




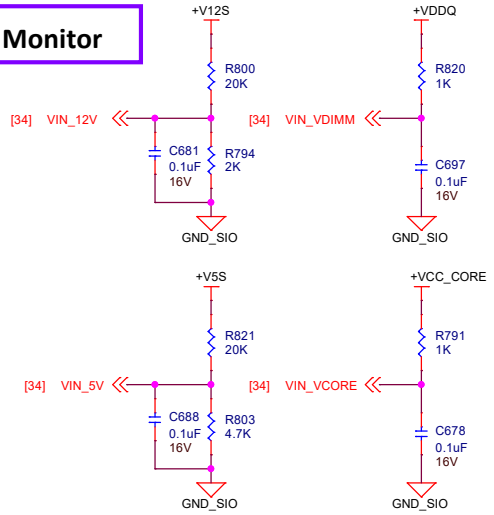
<Variant Name>

AAEON An ASUS Company	Title: SPI BIOS,LPC	
Size: B	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*	Sheet: 36 of 48	

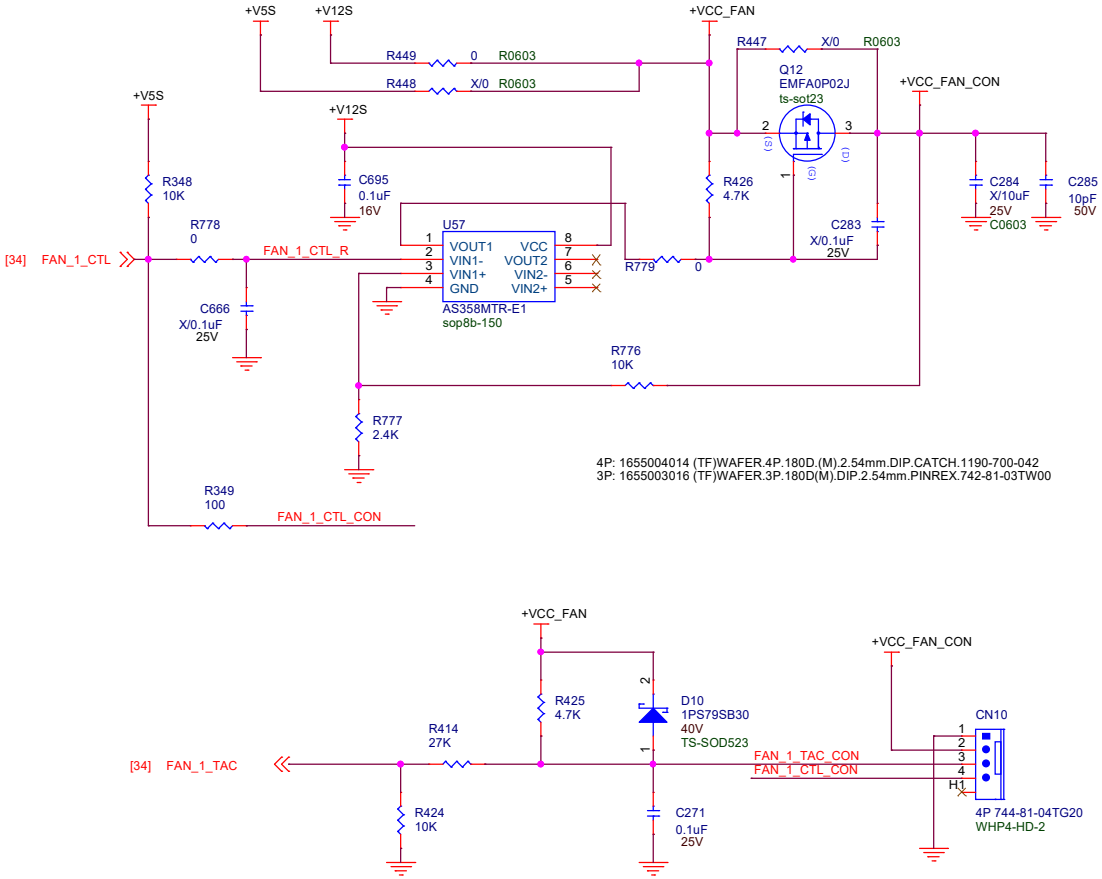
Temperature Monitor



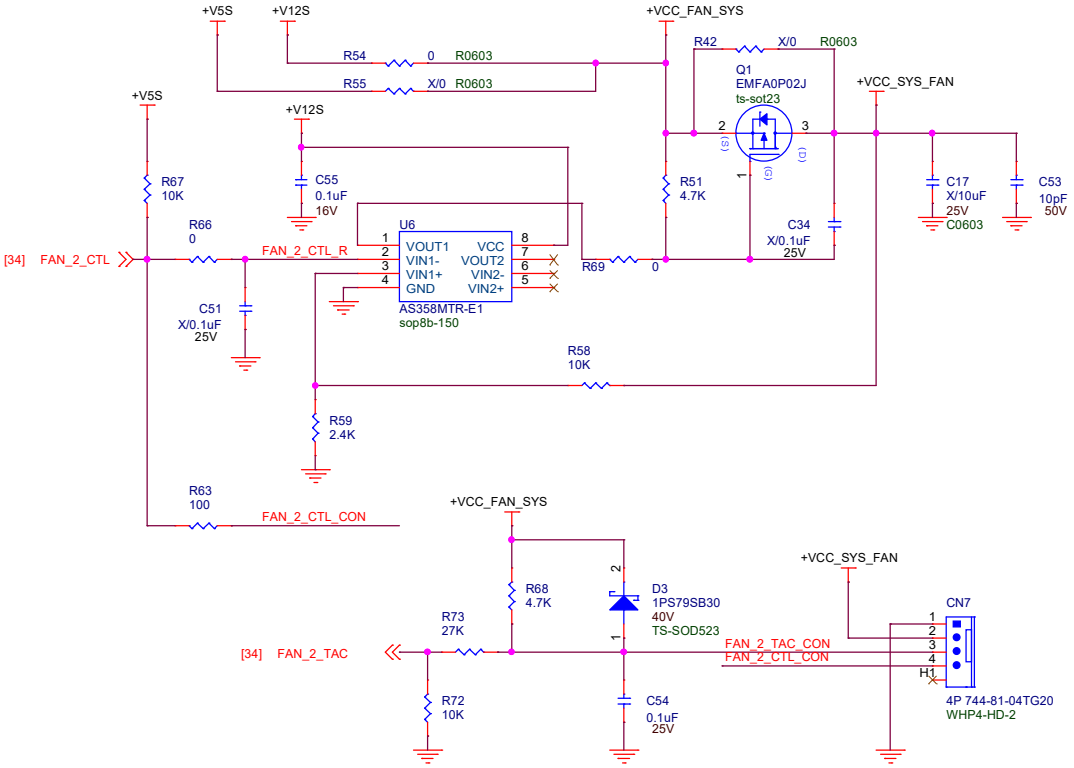
Voltage Monitor



CPU FAN



SYS FAN



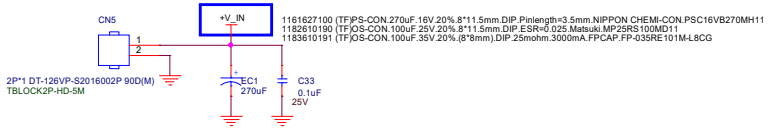
<Variant Name>

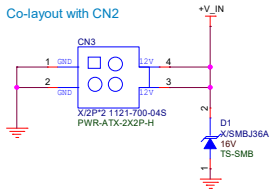
AAEON An ASUS Company

Title: DIO,HWMONITOR,FAN		
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019	Sheet: 37 of 48	

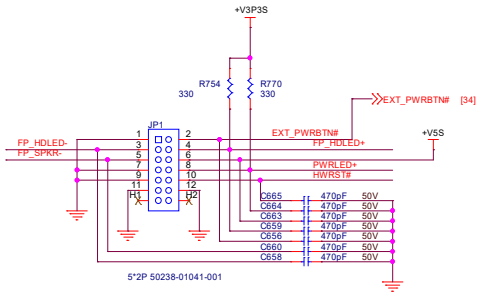
Power Input

+V12A

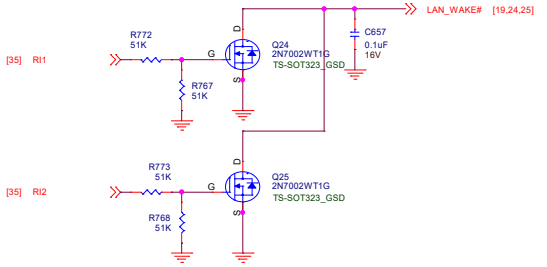




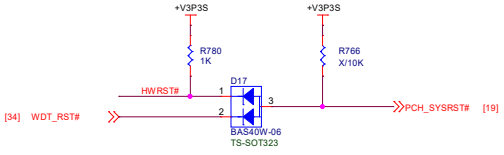
Front Panel



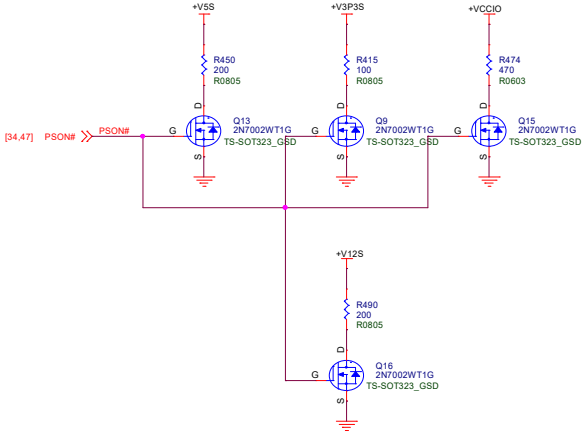
Wake On Modem



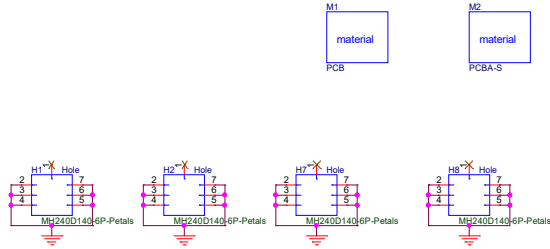
Reset Circuit



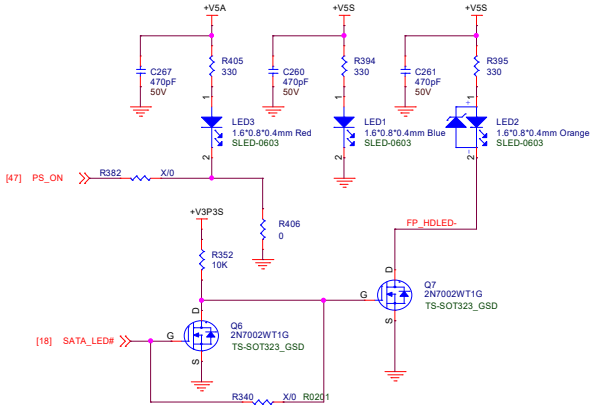
Discharge Circuit



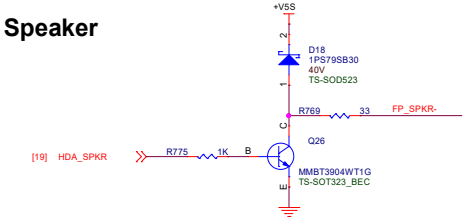
Mounting Holes
Need to be updated



LED



Speaker



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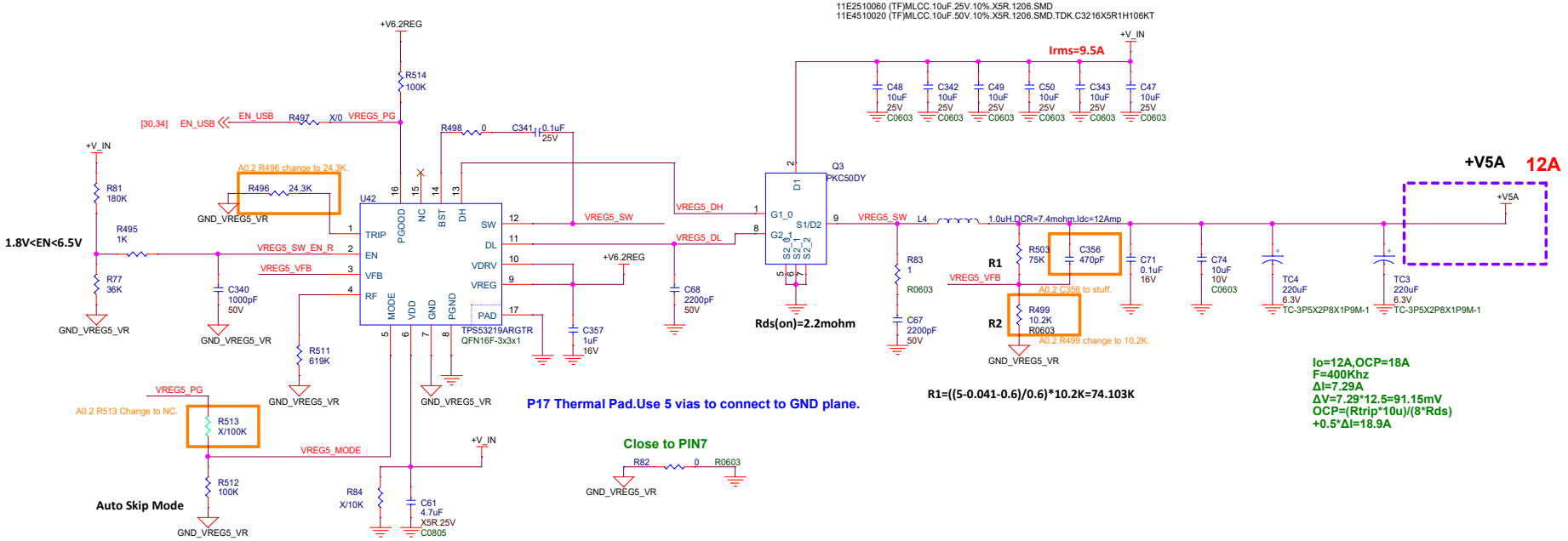
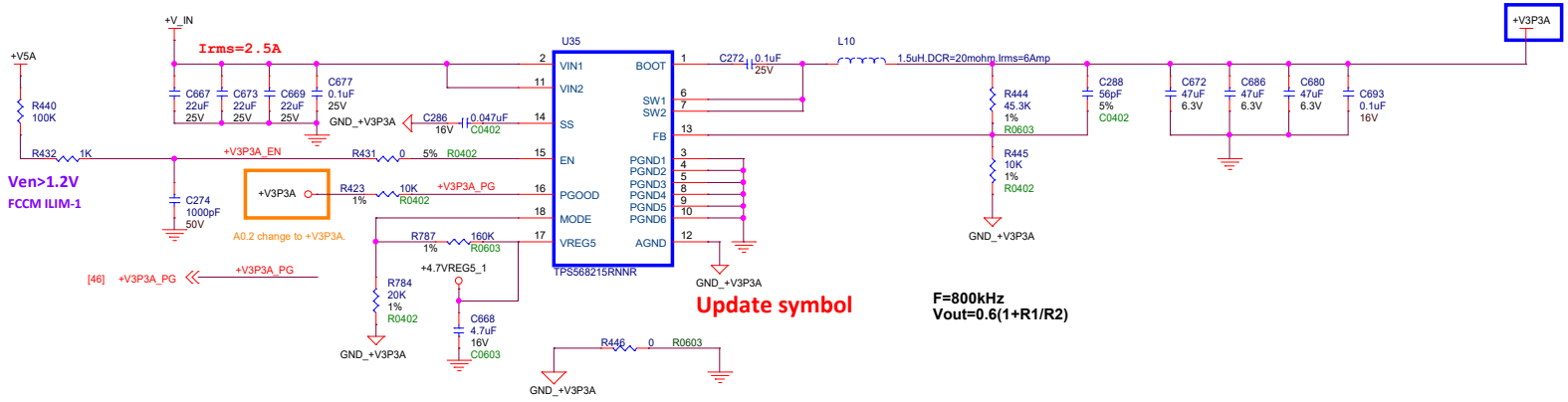
AAEON An ASUS Company

Title: POWER INPUT,MISC		
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 38 of 48

+V5A



+V3P3A



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AAEON An ASUS Company

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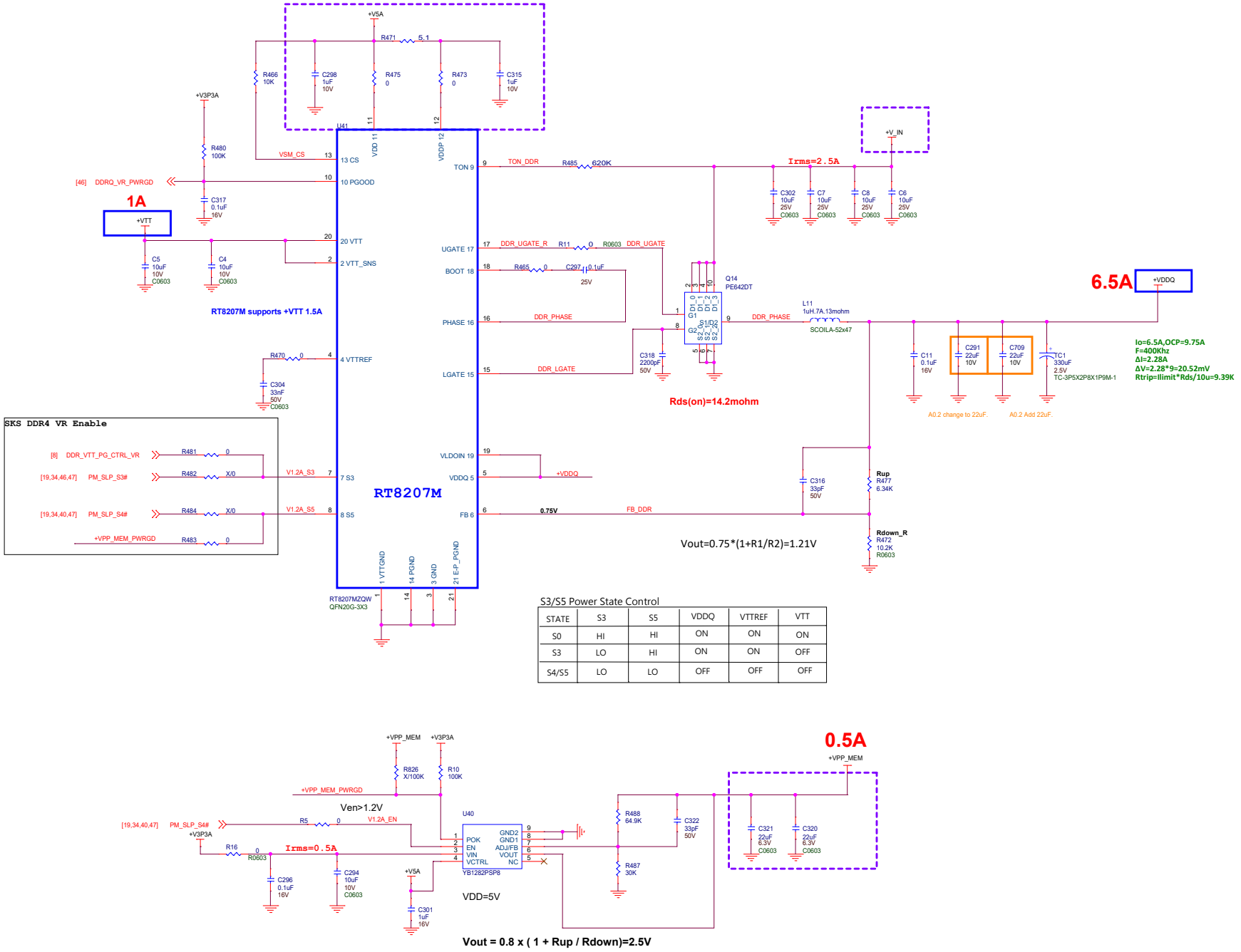
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019	Sheet: 39 of 48	



S3/S5 Power State Control

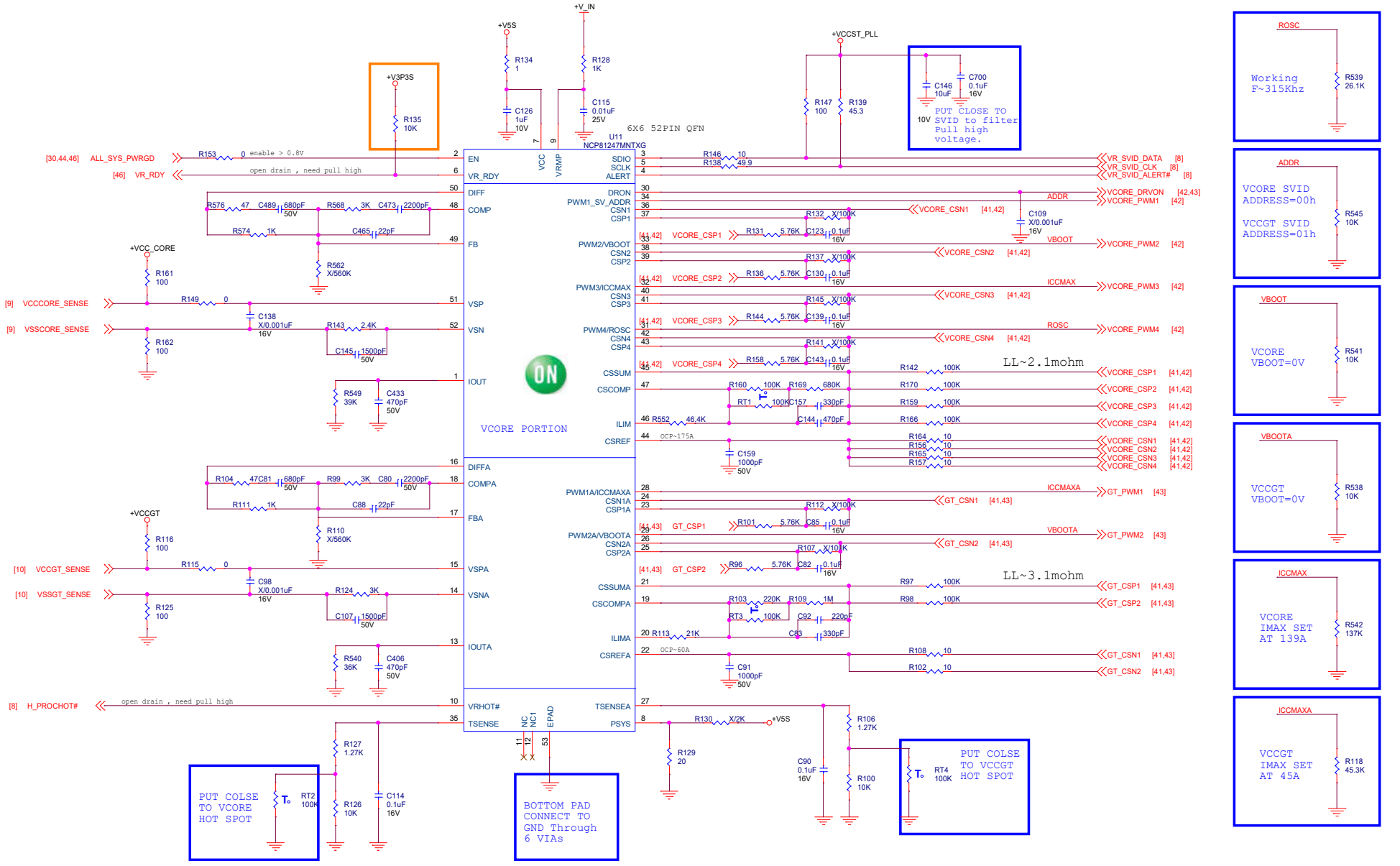
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S4/S5	LO	LO	OFF	OFF	OFF

<Variant Name>

AAEON An ASUS Company

Title: POWER_+VDDQ_MEM/VPP		
Size: C	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019	Sheet: 40 of 48	

S-Line 62 65W CPU power spec
Vcore ICCMAX=133A
VCCSA ICCMAX=11.1A



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AAEON An ASUS Company

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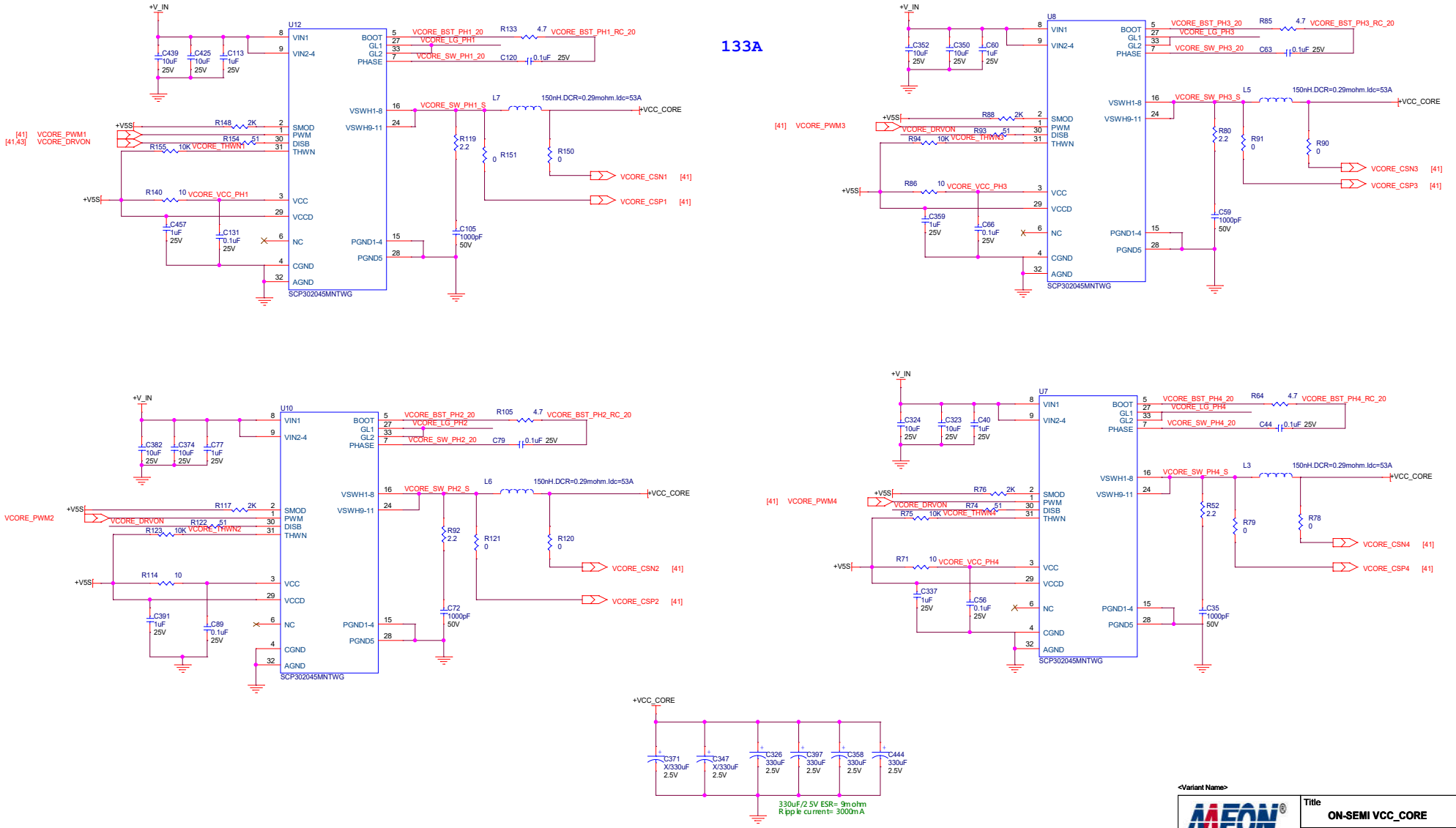
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019		Sheet: 41 of 48



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AAEON An ASUS Company

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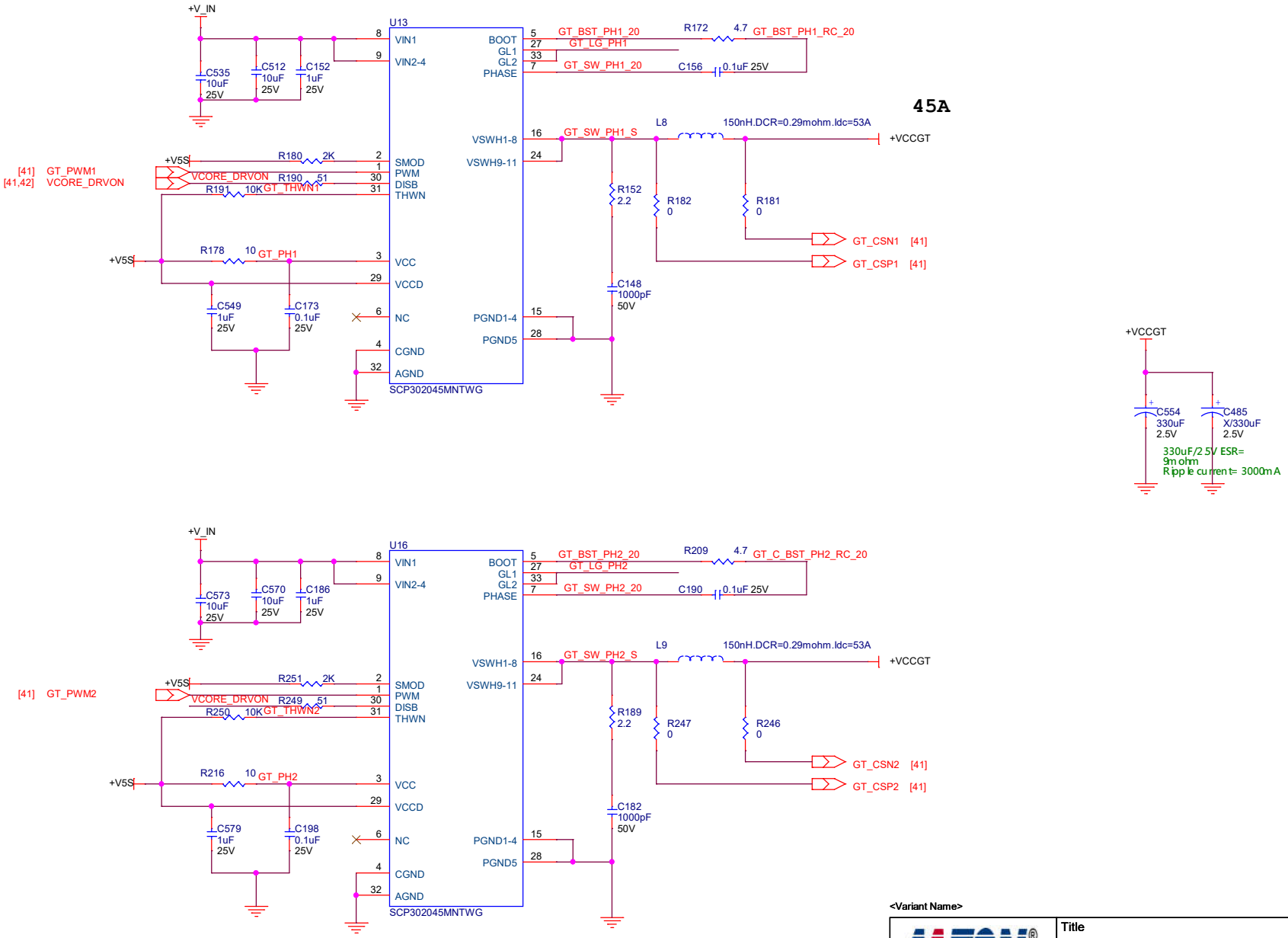
Size: Custom	Document Number: EPIC-CFS7	Rev: A0.2
Date: Thursday, June 13, 2019	Sheet: 42 of 48	



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AAEON An ASUS Company

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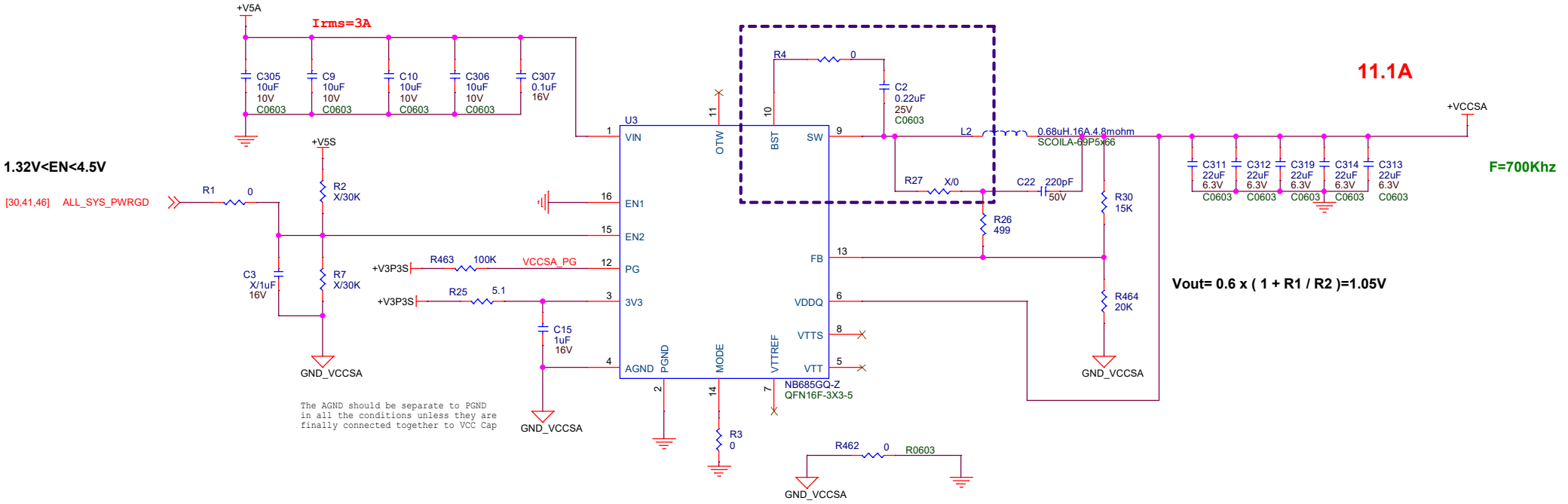
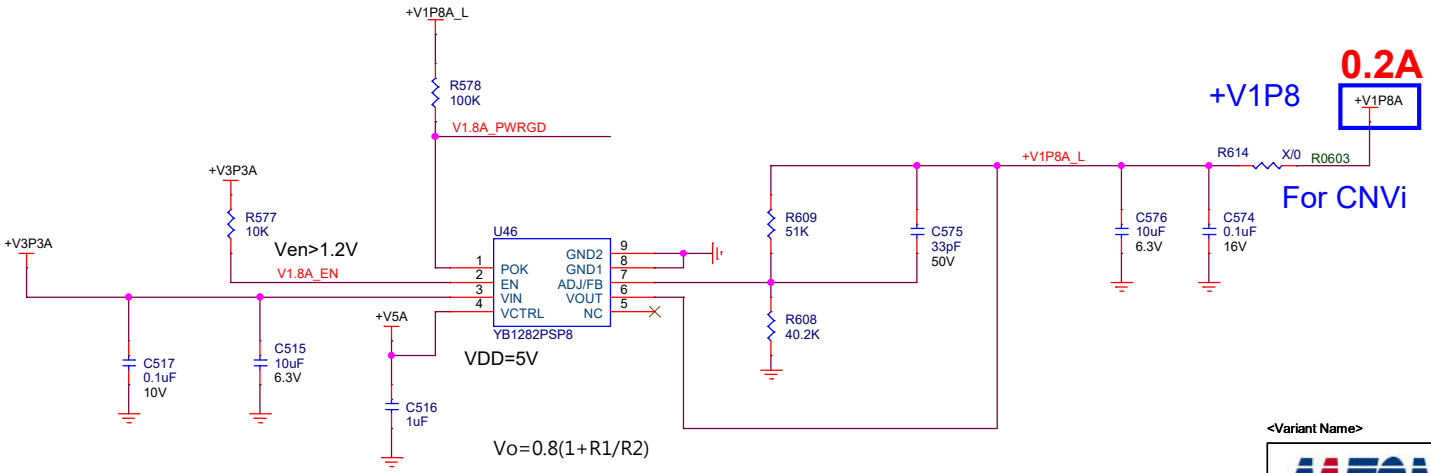
Date: *Thursday, June 13, 2019*	Sheet: 43 of 48	

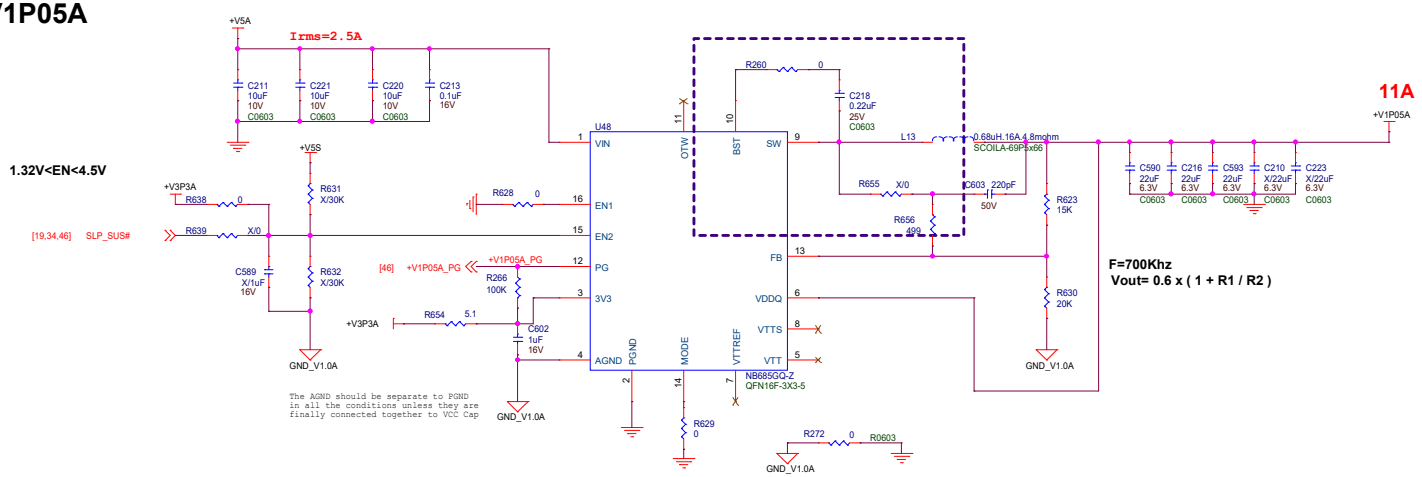




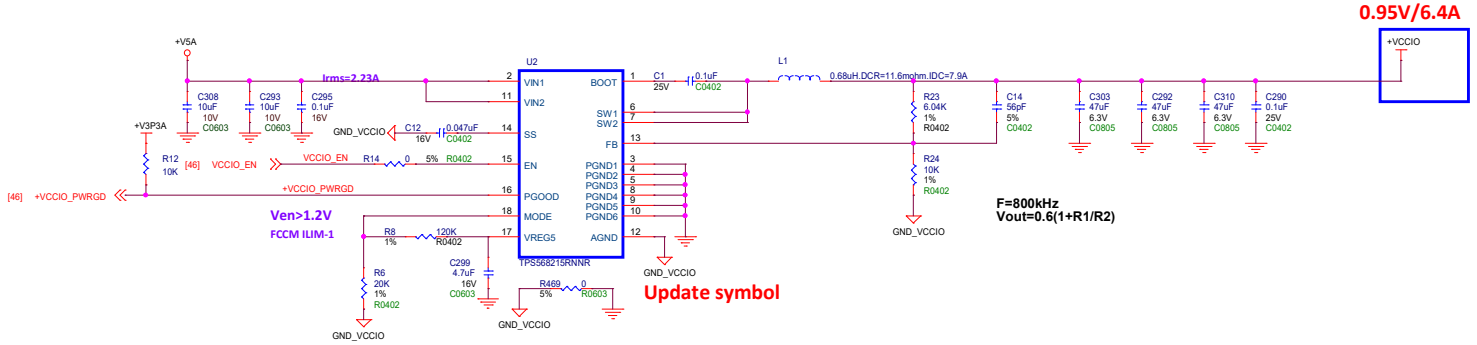
<Variant Name>

AAEON An ASUS Company	Title: POWER_ VCCSA	
	Size: B	Document Number: EPIC-CFS7 / Rev: A0.2
	Date: *Thursday, June 13, 2019*	Sheet: 44 of 48

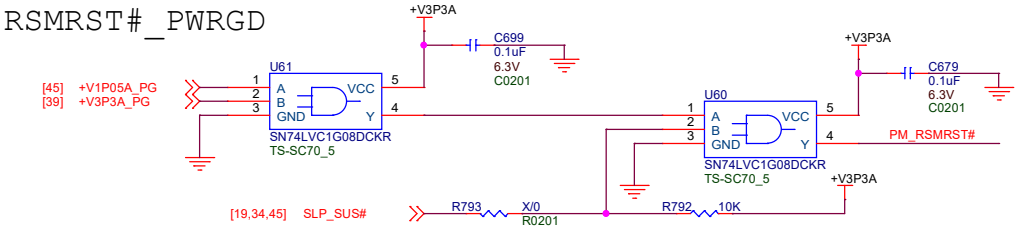
+V1P05A



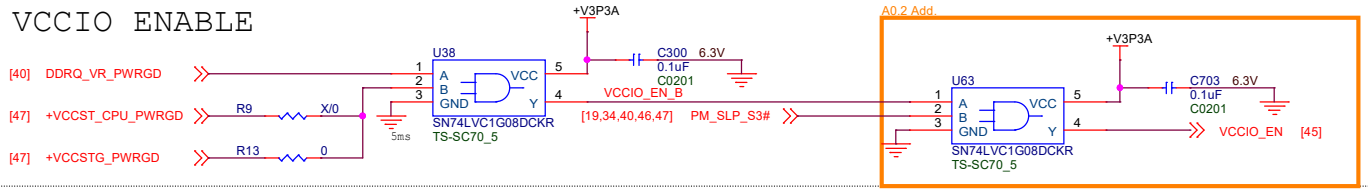
+VCCIO



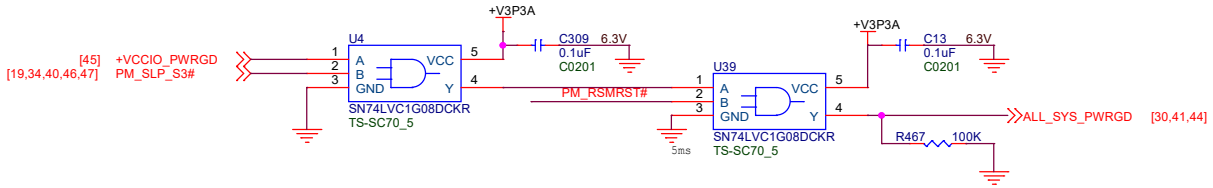
RSMRST#_PWRGD

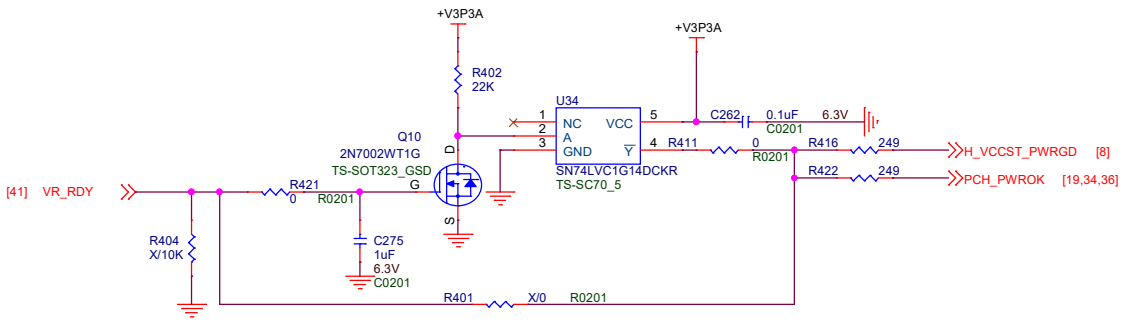


VCCIO ENABLE



ALL_SYS_PWRGD



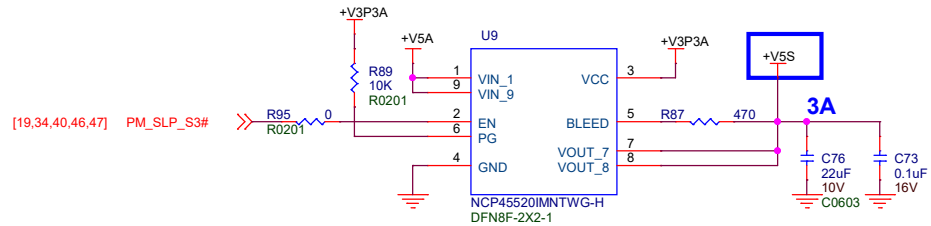


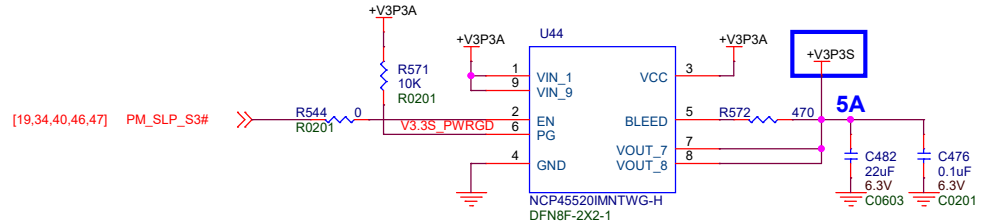
PCH_PWRGD & VCCST_PWRGD & SYS_PWROK

<Variant Name>

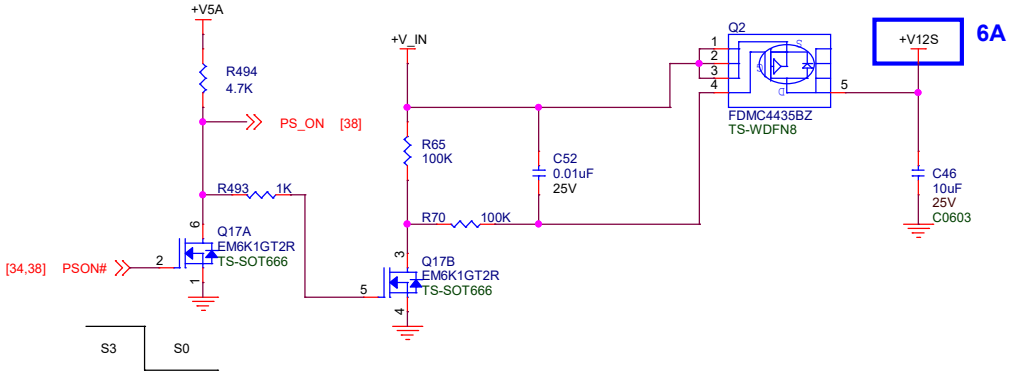
AAEON An ASUS Company

Title: **Boot Sequence**		
Size: Custom	Document Number: **EPIC-CFS7**	Rev: **A0.2**
Date: *Thursday, June 13, 2019*	Sheet: **46** of **48**	

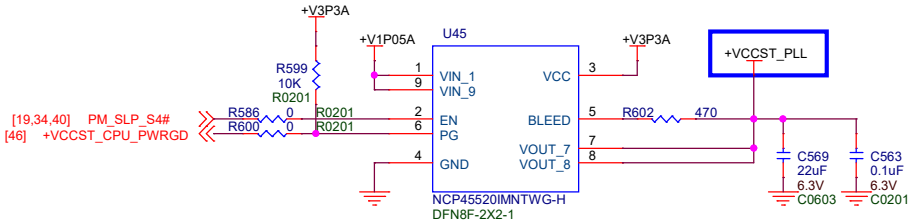


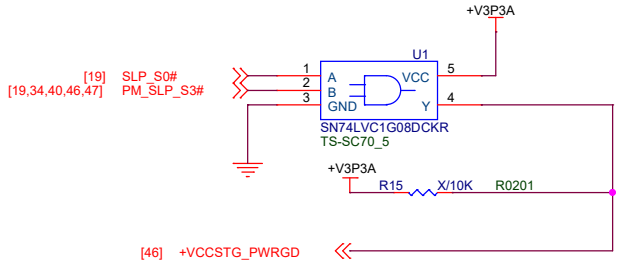


Del +V1P05A_PCH SW



To CPU





<Variant Name>

AAEON An ASUS Company

Title: SYSTEM POWER		
Size: B	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*	Sheet: 47 of 48	

EPIC-CFS7 A0.1

Revision History

<Variant Name>

AAEON® An ASUS Company

Title: HISTORY		
Size: A	Document Number: EPIC-CFS7	Rev: A0.2
Date: *Thursday, June 13, 2019*	Sheet: 48 of 48	