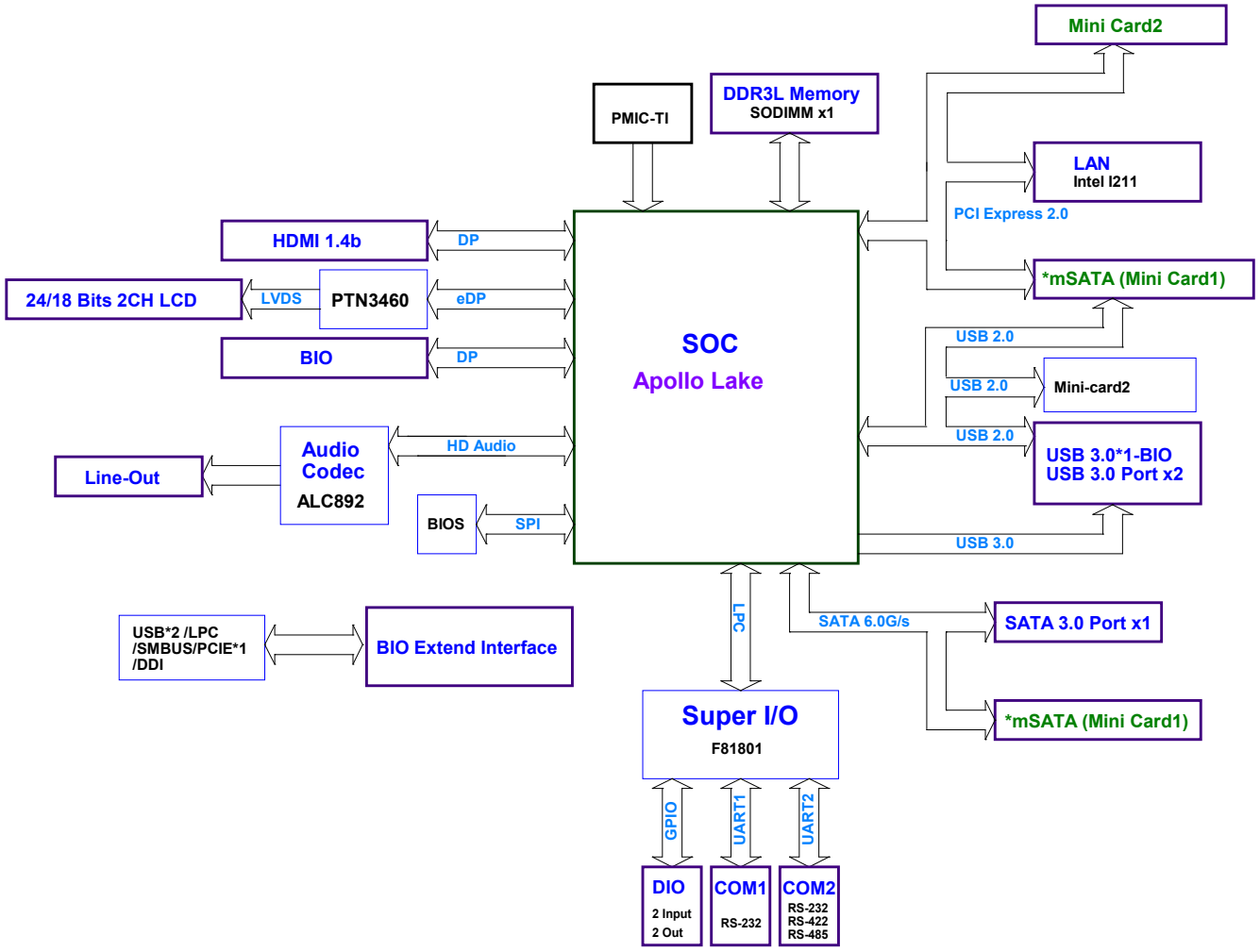
PICO-APL1 Rev.A0.1_0_0

Apollo Lake SoC Platform Cross Compatibility



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Project Number : E16XXXX

Production Line : Sub.EPI.AA2M

Title: Cover Sheet			
Size: C	Document Number: PICOAPL1A01		Rev: A0.1
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SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	BOARDID_BIT0
GPIO_1	1.8V	20K PD/I	BOARDID_BIT1
GPIO_2	1.8V	20K PD/I	
GPIO_3	1.8V	20K PD/I	
GPIO_4	1.8V	20K PD/I	LVDS_RBIT0
GPIO_5	1.8V	20K PD/I	LVDS_RBIT1
GPIO_6	1.8V	20K PD/I	LVDS_RBIT2
GPIO_7	1.8V	20K PD/I	LVDS_RBIT3
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	WAKE_RI#
GPIO_15	1.8V	20K PD/I	EN_USB
GPIO_16	1.8V	20K PD/I	LAN1_DISABLE#
GPIO_17	1.8V	20K PD/I	W_DISABLE0#
GPIO_18	1.8V	20K PD/I	W_DISABLE1#
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GP[0]
GPIO_23	1.8V	20K PD/I	SATA_GP[1]
GPIO_24	1.8V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	1.8V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/IO	
GPIO_217	1.8V	20K PD/IO	
GPIO_218	1.8V	20K PD/IO	
GPIO_219	1.8V	20K PD/IO/OP	

The Mapping Table For Super I/O F81801U GPIOs :

Name	PIN No.	Power	Type	Description & setting
GPIO[6]	42	+3.3V_ALW	I/OOD12t	
GPIO[12]	35	+3.3V	I/OOD12t	WDTRST#
GPIO[15]	36	+3.3V	I/OOD12,st,lv	None
GPIO[16]	37	+3.3V	I/OOD12,st,lv	
GPIO[20]	38	+3.3V	I/OOD12,st,lv	
GPIO[21]	39	+3.3V	I/OOD12t	
GPIO[22]	40	+3.3V	I/OOD12t	
GPIO[23]	41	+3.3V	I/OOD12t	
GPIO[30]	9	+3.3V	I/OOD12t	DCDB#
GPIO[31]	10	+3.3V	I/OOD12t	RIB#
GPIO[32]	11	+3.3V	I/OOD12t	CTSB#
GPIO[33]	13	+3.3V	I/OOD12t	DTRB#
GPIO[34]	14	+3.3V	I/OOD12t	RTSB#
GPIO[35]	15	+3.3V	I/OOD12t	DSRB#
GPIO[36]	16	+3.3V	I/OOD12t	TXB#
GPIO[37]	17	+3.3V	I/OOD12t	RXB#

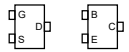
I/OOD12st,lv : Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.

I/OOD12t : TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability

F75111RG GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO10	5V	VSB3V	Native	BOARDID_BIT0
GPIO11	5V	VSB3V	Native	ADM213_EN
GPIO12	5V	VSB3V	Native	81438_SD
GPIO13	5V	VSB3V	Native	
GPIO14	5V	VSB3V	Native	BOARDID_BIT1
GPIO15	5V	VSB3V	Native	
GPIO16	5V	VSB3V	Native	
GPIO17	5V	VSB3V	Native	
GPIO20	5V	VSB3V	Native	SEL_COM2_MD0
GPIO21	5V	VSB3V	Native	SEL_COM2_MD1
GPIO22	5V	VSB3V	Native	COM2_SLEW
GPIO23	5V	VSB3V	Native	BIO-GPIO
GPIO24	5V	VSB3V	Native	DIO_P0
GPIO25	5V	VSB3V	Native	DIO_P1
GPIO26	5V	VSB3V	Native	DIO_P2
GPIO27	5V	VSB3V	Native	DIO_P3
GPIO30	5V	VSB3V	GPIO	LVDS_EN
GPIO31	5V	VSB3V	GPIO	
GPIO32	5V	VSB3V	GPIO	
GPIO33	5V	VSB3V	GPIO	LVDS_PD#

PCB Footprints

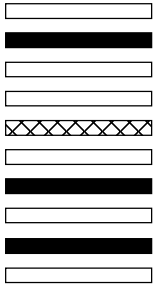


SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
GPIO IC	6Eh
PTN3460 Slave	C0h

PCB STACK :

Impedence 50ohm +/-15%.



- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : GND
- Layer 5 : Signal
- Layer 6 : VCC
- Layer 7 : Signal
- Layer 4 : Signal
- Layer 9 : GND
- Layer 10 : Solder

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Title: **System Settings**

Size	Document Number	Rev:
B	PICOAPL1A01	A0.1

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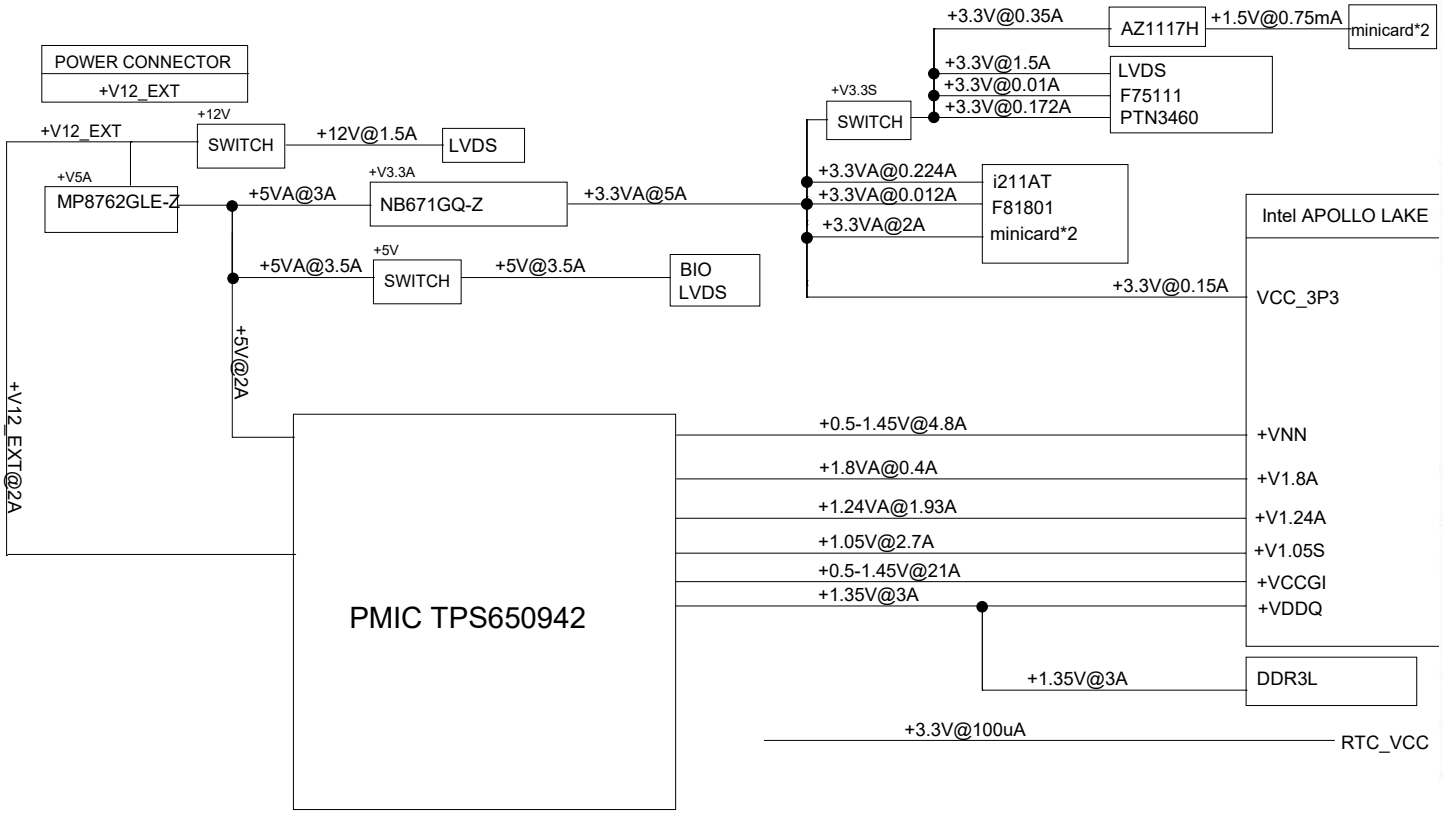

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Iccmax (A)
VCC_VCGI	0.45~1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	21
VNN	0.45~1.3	+/-50mV	4.8
VCC_V1P05	1.05	+/-5%	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	1.3
VCC_V1P24_A	1.24	+/-5%	TBD
VCC_V1P8V_A	1.8	+/-5%	0.4
VDDQ	1.35	+/-5%	2.8 (excluding DRAM)
	1.24	+/-5%	
VCC_3P3V_A	3.3	+/-5%	0.15
VCC_RTC_3P3V	2~3.47	N/A	TBD

+V5A -> +V3.3A -> +VNN -> +VCC -> +V1P8A- > +V1P24A -> +V1P8U -> +VDDQ
+V1.05S -> +VCC_VCGI

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Title: Power Tree

Size: Custom | Document Number: PICOAPL1A01 | Rev: A0.1

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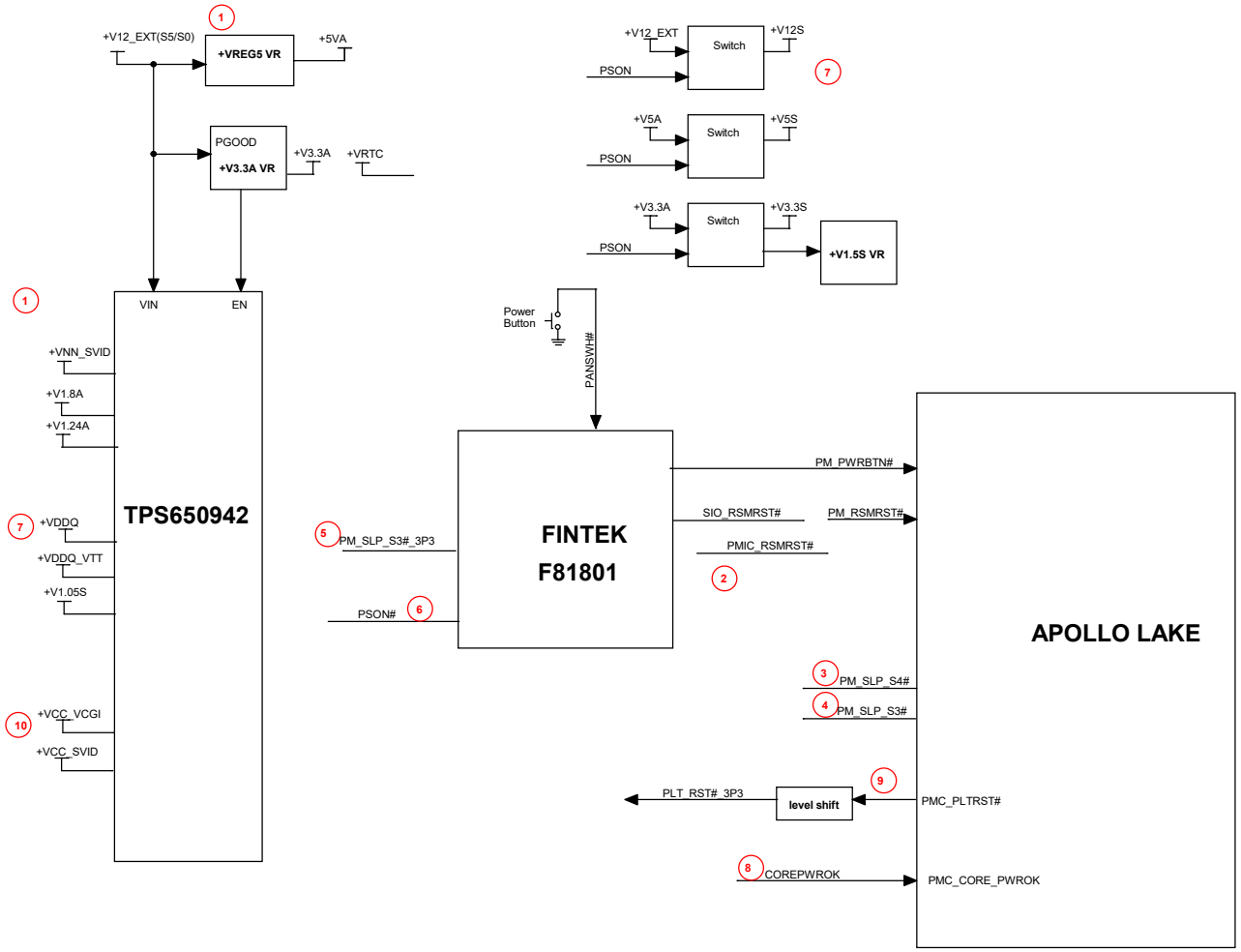
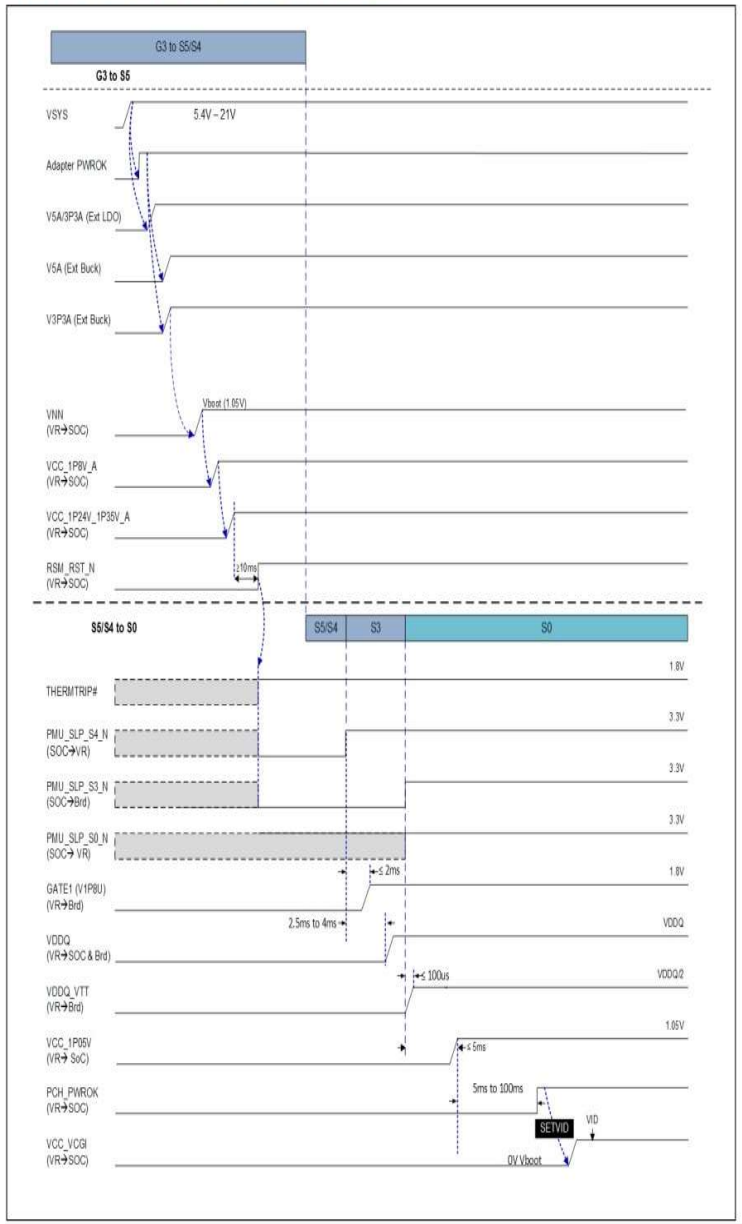


Power-Up Sequencing (G3 to S0)—Adapter



AAEON an ASUS assoc. co.	Title: Power Sequence	
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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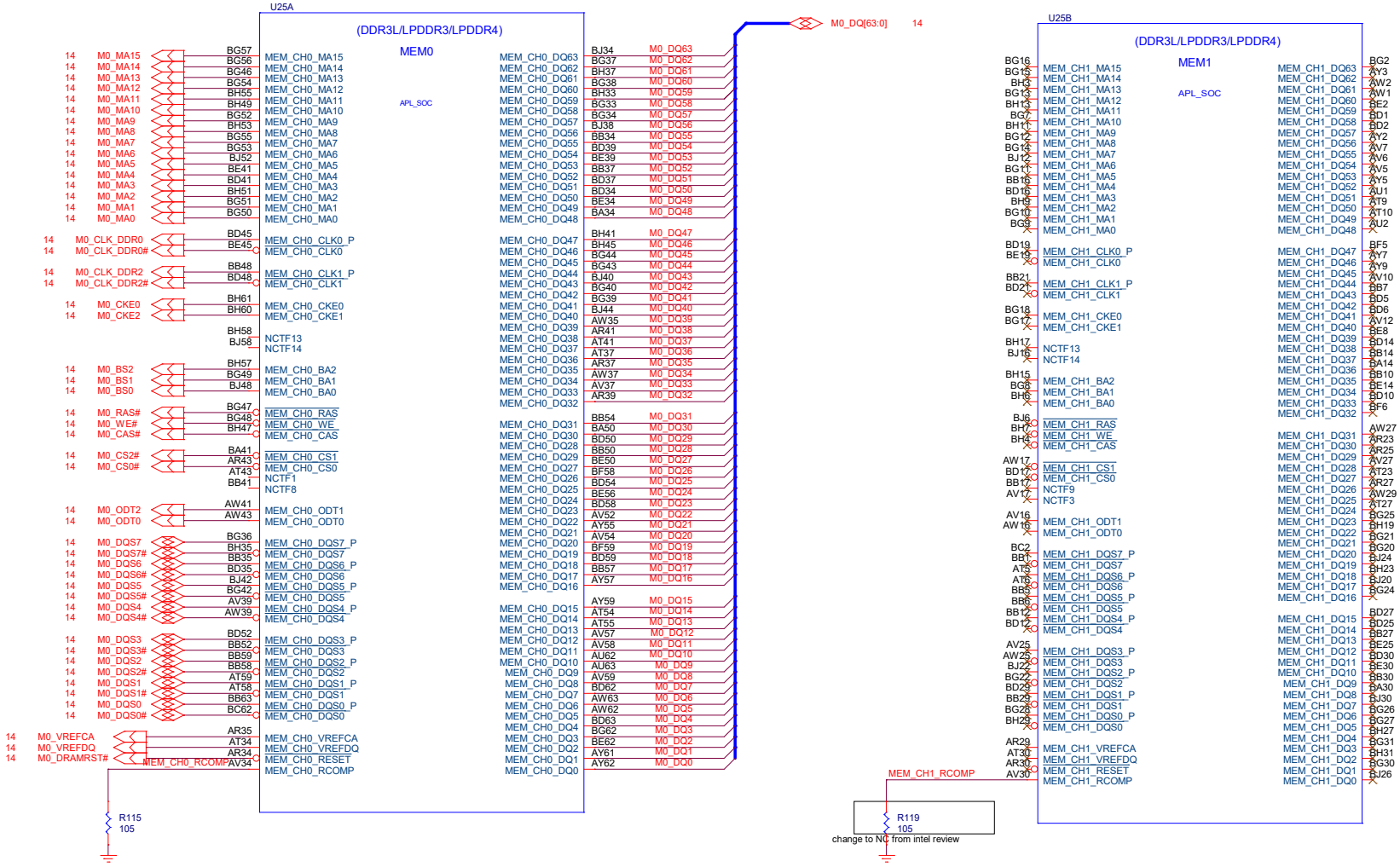

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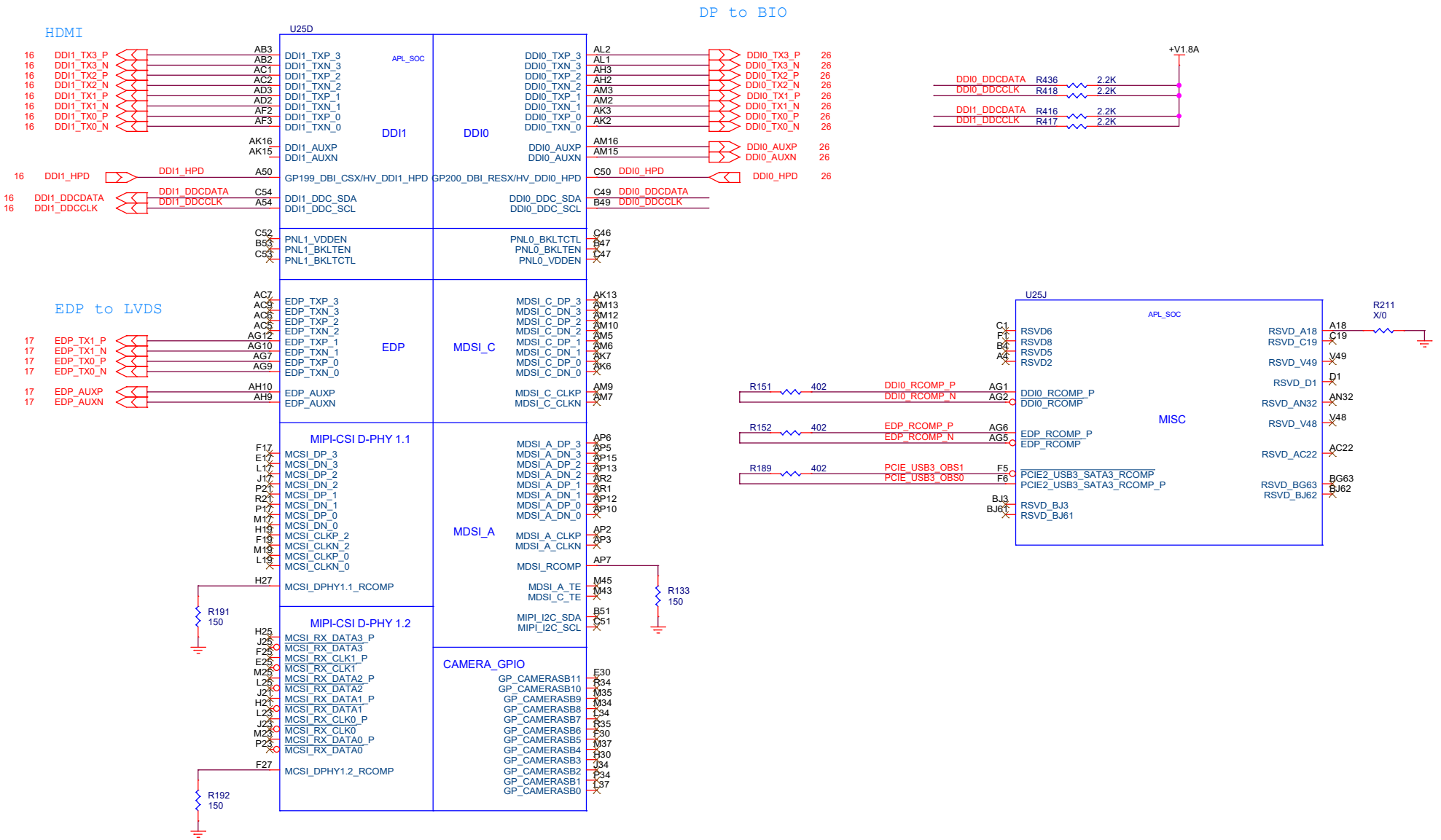

AAEON an ASUS assoc. co.	Title: SOC_DISPLAY		
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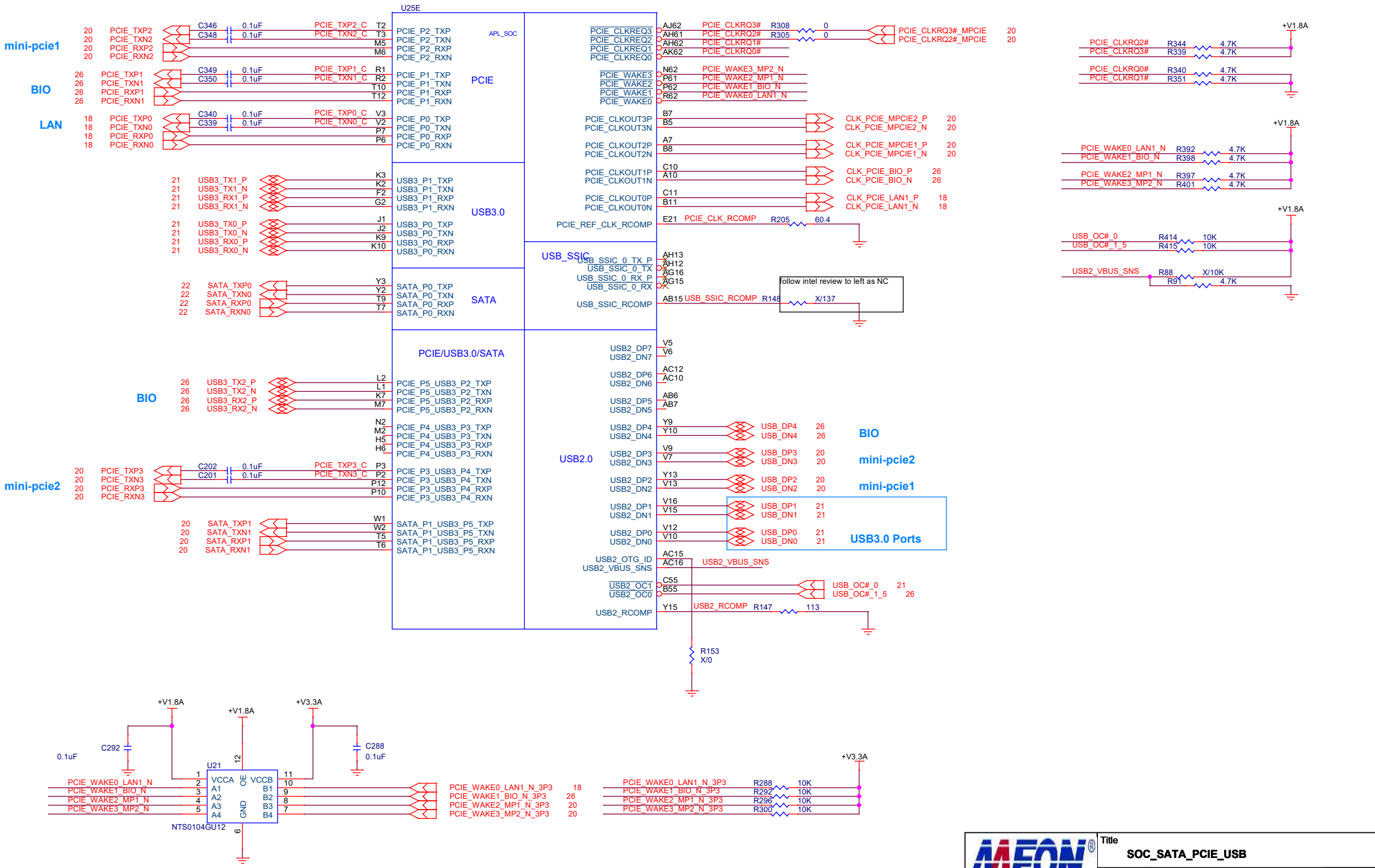

AAEON an ASUS assoc. co.	Title: SOC_SATA_PCIE_USB		
	Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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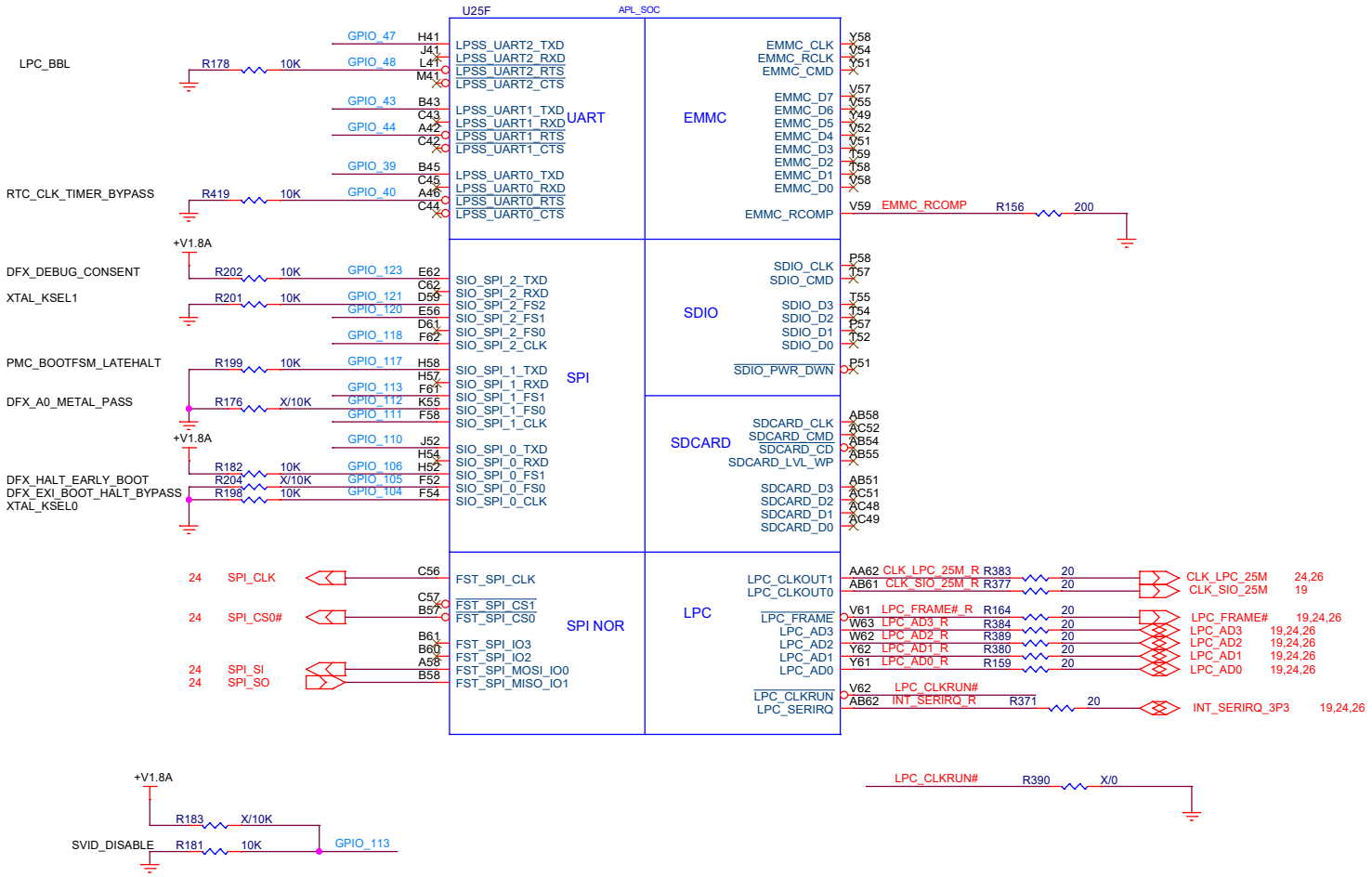
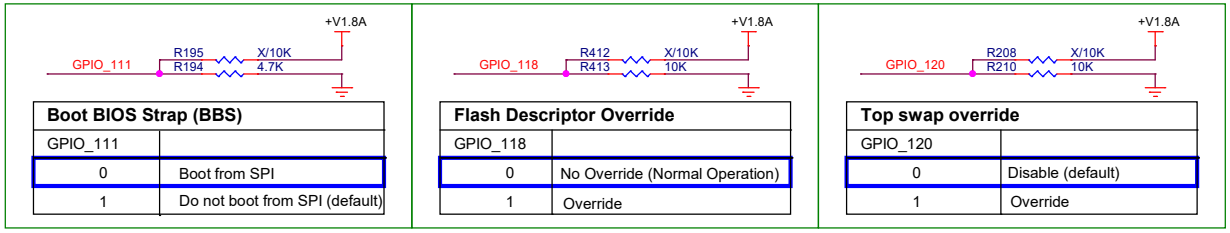
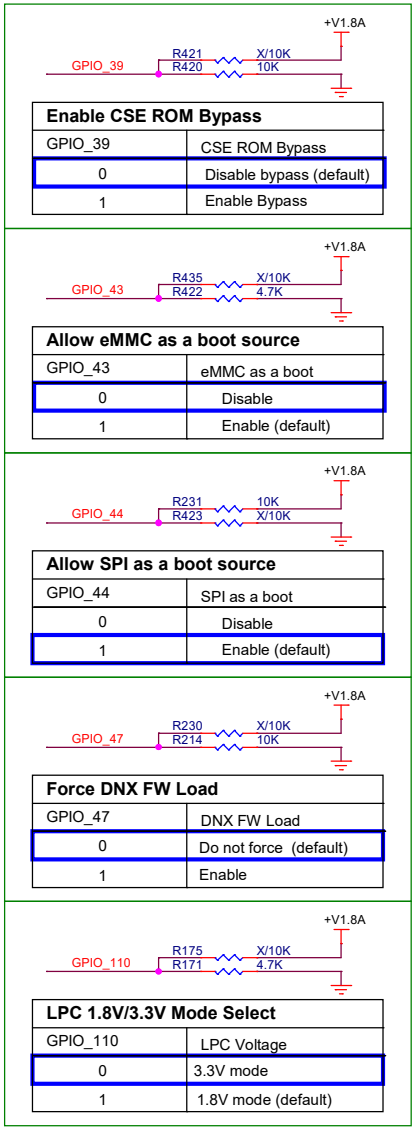




Boot BIOS Strap (BBS)	
GPIO_111	
0	Boot from SPI
1	Do not boot from SPI (default)

Flash Descriptor Override	
GPIO_118	
0	No Override (Normal Operation)
1	Override

Top swap override	
GPIO_120	
0	Disable (default)
1	Override



Enable CSE ROM Bypass	
GPIO_39	CSE ROM Bypass
0	Disable bypass (default)
1	Enable Bypass

Allow eMMC as a boot source	
GPIO_43	eMMC as a boot
0	Disable
1	Enable (default)

Allow SPI as a boot source	
GPIO_44	SPI as a boot
0	Disable
1	Enable (default)

Force DNX FW Load	
GPIO_47	DNX FW Load
0	Do not force (default)
1	Enable

LPC 1.8V/3.3V Mode Select	
GPIO_110	LPC Voltage
0	3.3V mode
1	1.8V mode (default)

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Title: SOC_LPC_SPI_EMMC_SD		
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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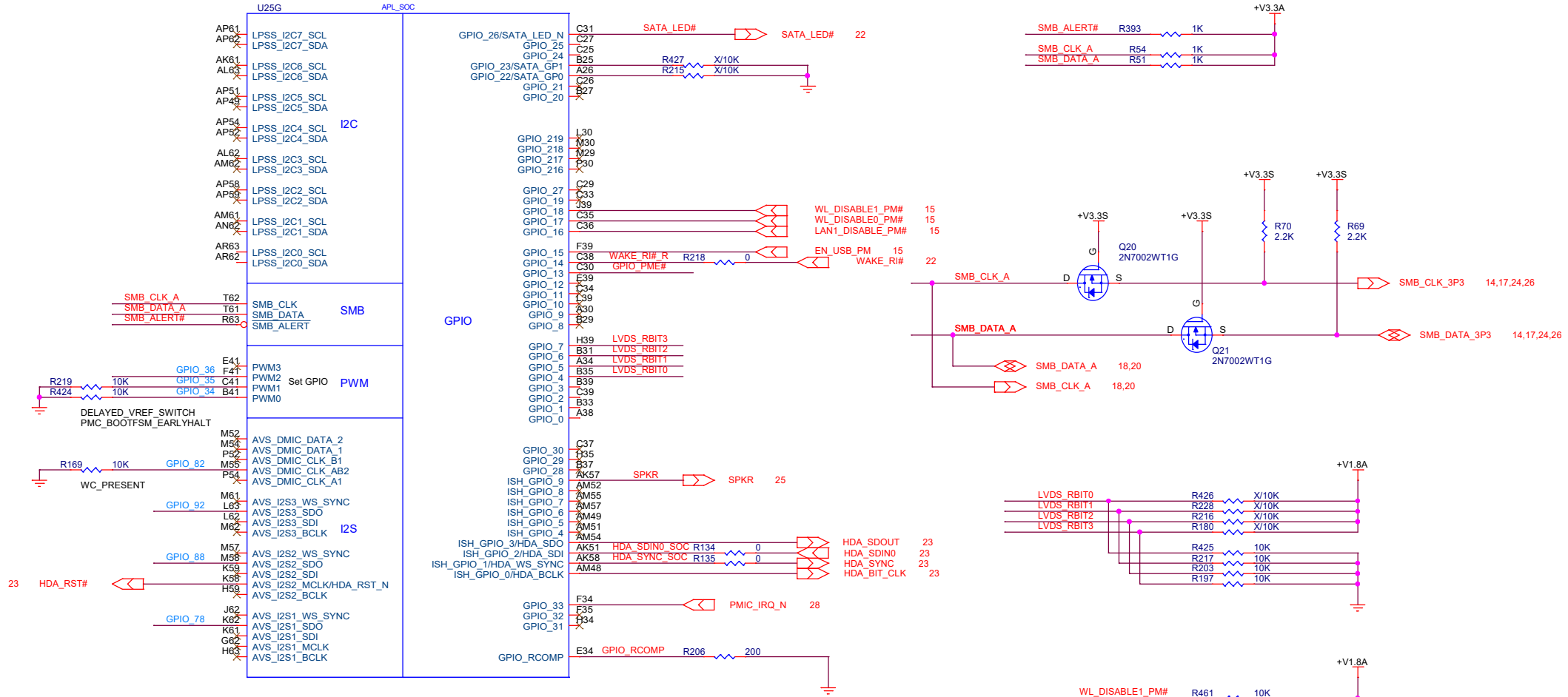

VCC_1P24V_1P35V_A Volt Selection	
GPIO_36	VCC_1P24V_1P35V_A
0	1.24V (default)
1	1.35

SMBus 1.8V/3.3V mode Select	
GPIO_78	SMBus
0	3.3V
1	1.8V (default)

PMU 1.8V/3.3V Mode Select	
GPIO_88	PMU
0	3.3V
1	1.8V (default)

SMBus No Re-Boot	
GPIO_92	No Re-Boot
0	Disable (default)
1	Enable

HW Workaround for SDI issue of Apollo lake ES sample

There are no strict placement rules for two resistors.

AAEON an ASUS assoc. co.	Title: SOC_SMBUS_GPIO		
	Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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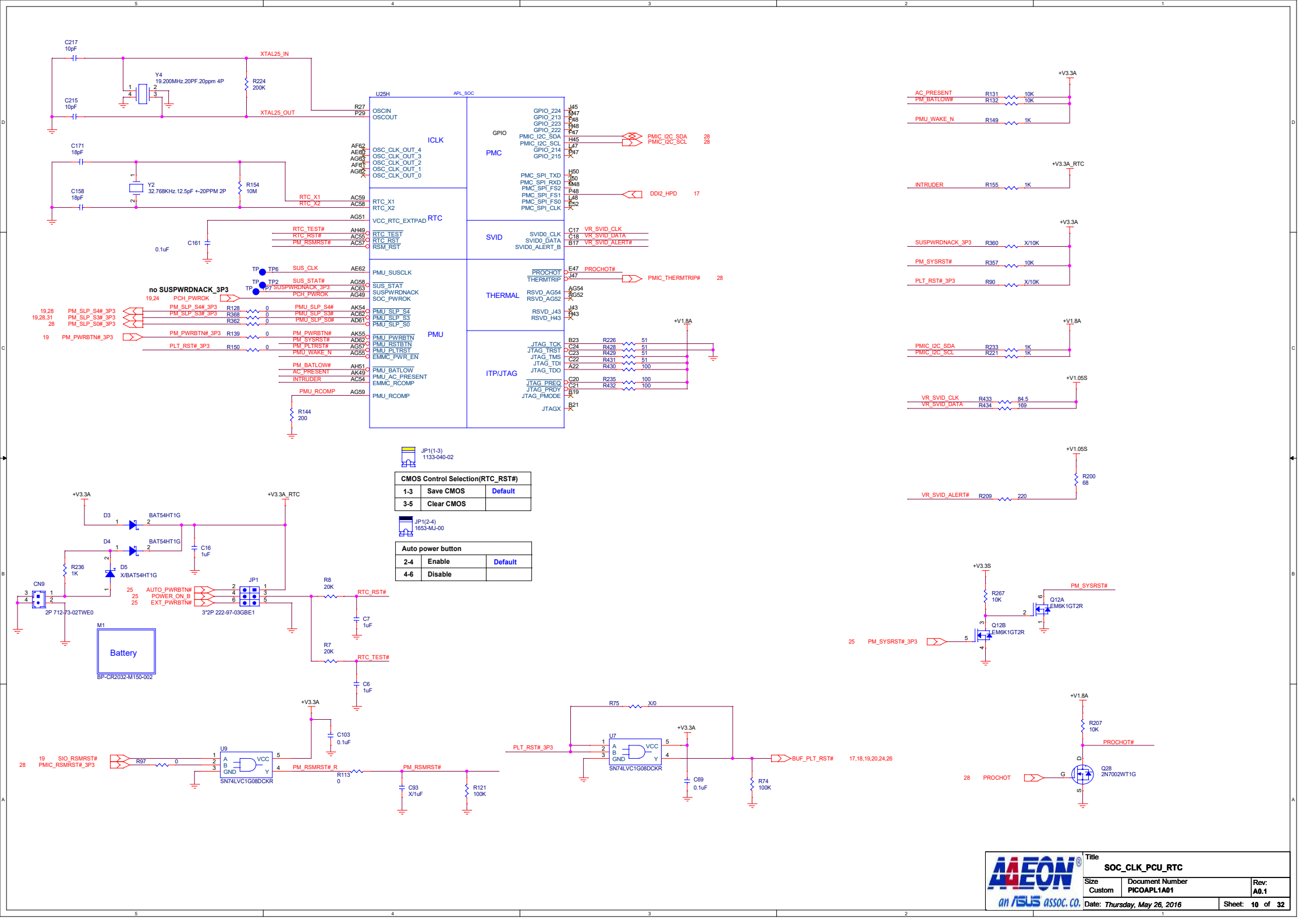
C217 10pF
C215 10pF
Y4 19.200MHz.20PF.20ppm 4P
XTAL25_IN
XTAL25_OUT
R224 200K
U25H
APL_SOC
OSCIN
OSCOUT
ICLK
OSC_CLK_OUT_4
OSC_CLK_OUT_3
OSC_CLK_OUT_2
OSC_CLK_OUT_1
OSC_CLK_OUT_0
C171 18pF
C158 18pF
Y2 32.768KHz.12.5pF +-20PPM 2P
R154 10M
RTC_X1
RTC_X2
VCC_RTC_EXTPAD
RTC
C161 0.1uF
RTC_TEST#
RTC_RST#
PM_RSMRST#
RTC_TEST
RTC_RST
RSM_RST
no SUSPWRDNACK_3P3
PCH_PWROK
SUS_CLK
SUS_STAT#
SUSPWRDNACK_3P3
PMU_SUSCLK
SUS_STAT
SUSPWRDNACK
SOC_PWROK
PM_SLP_S4#_3P3
PM_SLP_S3#_3P3
PM_SLP_S0#_3P3
PMU_SLP_S4
PMU_SLP_S3
PMU_SLP_S0
PM_PWRBTN#_3P3
PM_SYSRST#
PM_PLTRST#
PMU_WAKE_N
PMU_PWRBTN
PMU_RSTBTN
PMU_PLTRST
EMMC_PWR_EN
PM_BATLOW#
AC_PRESENT
INTRUDER
PMU_BATLOW
PMU_AC_PRESENT
EMMC_RCOMP
PMU_RCOMP
PMU
R144 200
GPIO
GPIO_224
GPIO_213
GPIO_223
GPIO_222
PMIC_I2C_SDA
PMIC_I2C_SCL
GPIO_214
GPIO_215
PMC
PMC_SPI_TXD
PMC_SPI_RXD
PMC_SPI_FS2
PMC_SPI_FS1
PMC_SPI_FS0
PMC_SPI_CLK
DDI2_HPD
SVID
SVID0_CLK
SVID0_DATA
SVID0_ALERT_B
VR_SVID_CLK
VR_SVID_DATA
VR_SVID_ALERT#
THERMAL
PROCHOT
THERMTRIP
PROCHOT#
PMIC_THERMTRIP#
RSVD_AG54
RSVD_AG52
RSVD_J43
RSVD_H43
ITP/JTAG
JTAG_TCK
JTAG_TRST
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_PREQ
JTAG_PRDY
JTAG_PMODE
JTAGX
+V1.8A
JP1(1-3) 1133-040-02
CMOS Control Selection(RTC_RST#)
1-3 Save CMOS Default
3-5 Clear CMOS
JP1(2-4) 1653-MJ-00
Auto power button
2-4 Enable Default
4-6 Disable
+V3.3A
+V3.3A_RTC
D3 BAT54HT1G
D4 BAT54HT1G
D5 X/BAT54HT1G
C16 1uF
R236 1K
CN9
2P 712-73-02TWE0
JP1
3*2P 222-97-03GBE1
AUTO_PWRBTN#
POWER_ON_B
EXT_PWRBTN#
R8 20K
R7 20K
RTC_RST#
RTC_TEST#
C7 1uF
C6 1uF
M1
Battery
BP-CR2032-M150-002
U9
SN74LVC1G08DCKR
SIO_RSMRST#
PMIC_RSMRST#_3P3
R97 0
C103 0.1uF
PM_RSMRST#_R
R113 0
PM_RSMRST#
C93 X/1uF
R121 100K
R75 X/0
U7
PLT_RST#_3P3
BUF_PLT_RST#
C69 0.1uF
R74 100K
AC_PRESENT
PM_BATLOW#
R131 10K
R132 10K
PMU_WAKE_N
R149 1K
INTRUDER
R155 1K
SUSPWRDNACK_3P3
R360 X/10K
PM_SYSRST#
R357 10K
PLT_RST#_3P3
R90 X/10K
PMIC_I2C_SDA
PMIC_I2C_SCL
R233 1K
R221 1K
VR_SVID_CLK
VR_SVID_DATA
R433 84.5
R434 169
+V1.05S
R200 68
VR_SVID_ALERT#
R209 220
+V3.3S
R267 10K
Q12A EM6K1GT2R
Q12B EM6K1GT2R
PM_SYSRST#_3P3
R207 10K
PROCHOT#
Q28 2N7002WT1G
PROCHOT
AAEON
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Title
SOC_CLK_PCU_RTC
Size Custom
Document Number PICOAPL1A01
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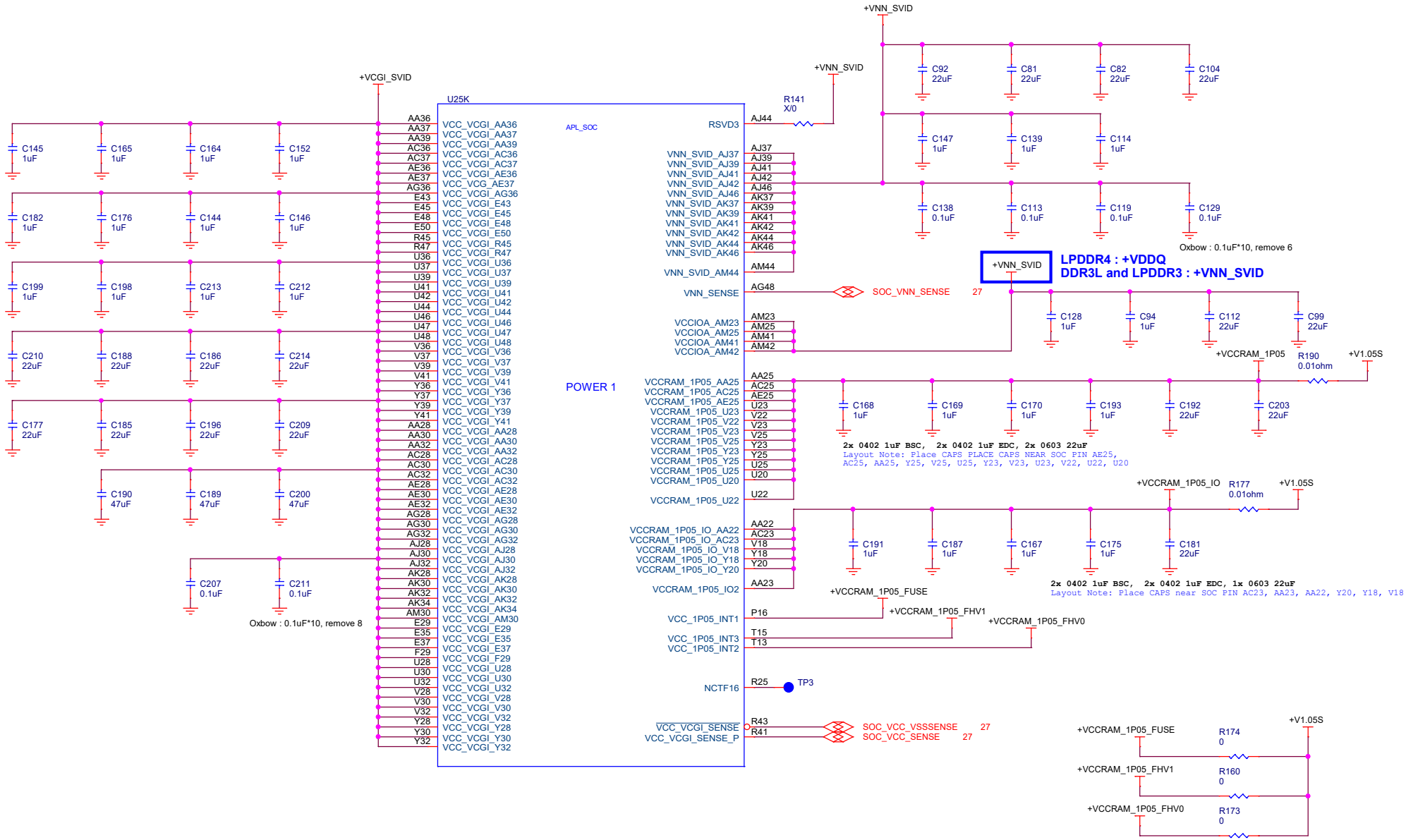

AAEON an ASUS assoc. co.	Title: SOC_POWER I	
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
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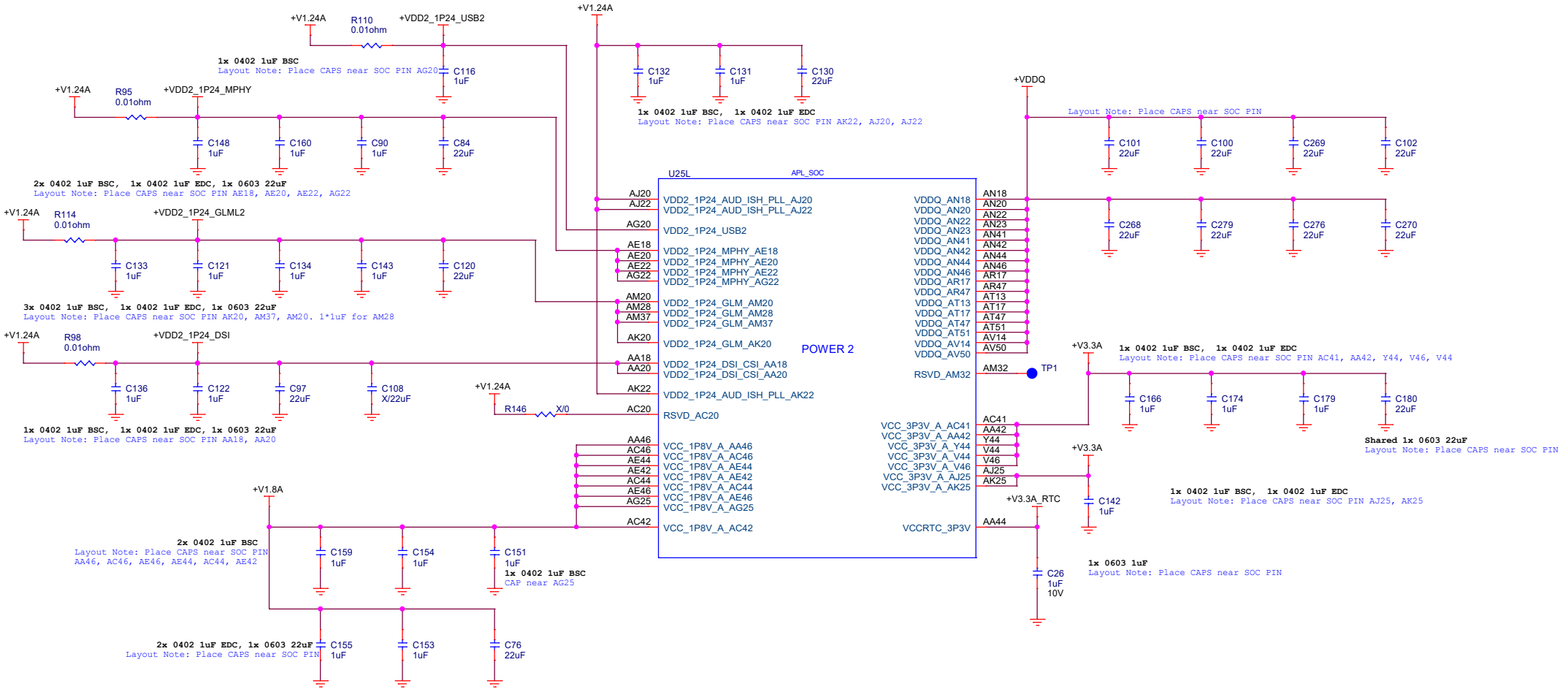

AAEON an ASUS assoc. co.

Title: SOC_POWER II

Size	Document Number	Rev:
Custom	PICOAPL1A01	A0.1

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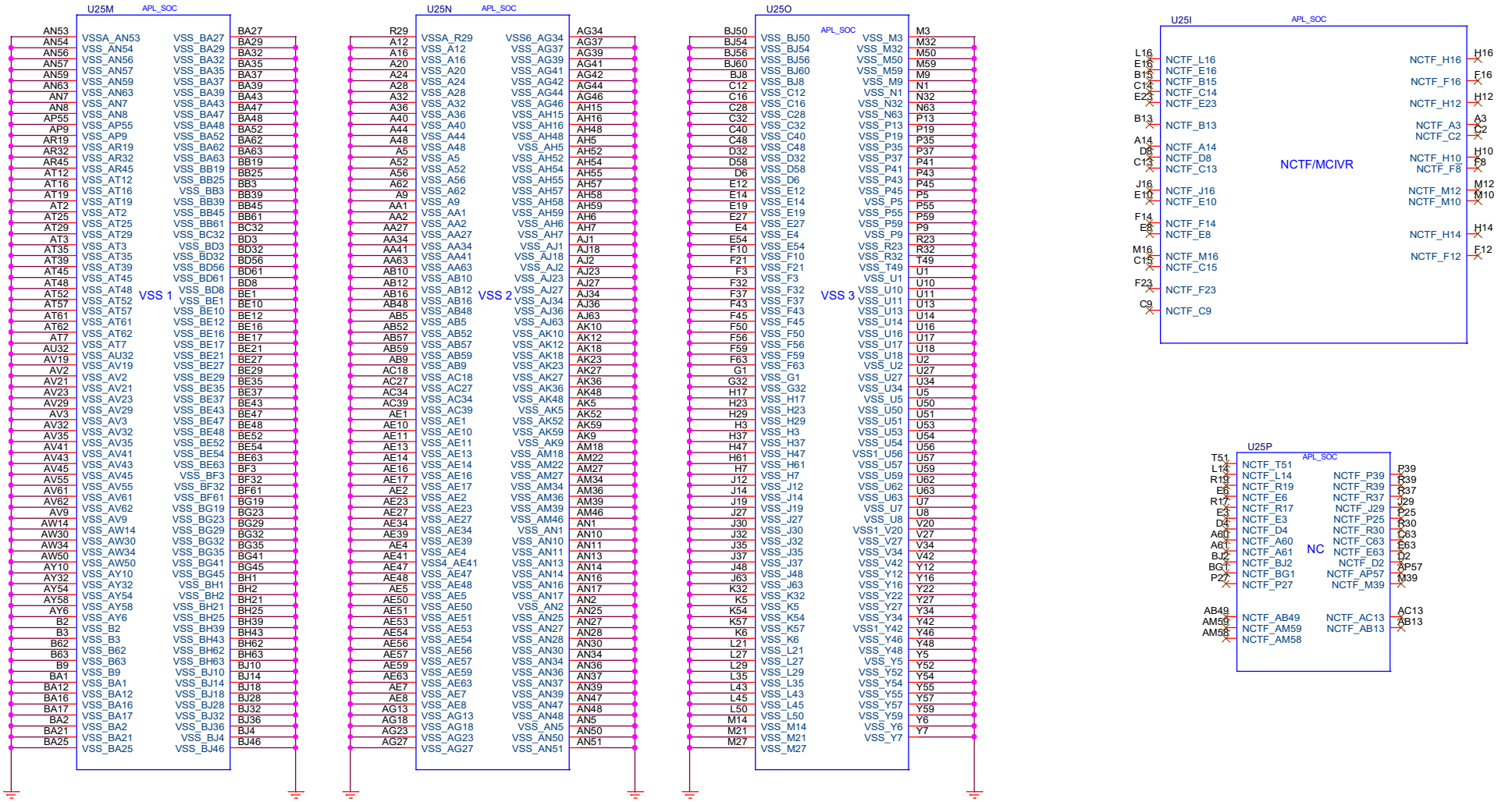

AAEON an ASUS assoc. co.

Title: SOC_GND

Size	Document Number	Rev:
Custom	PICOAPL1A01	A0.1

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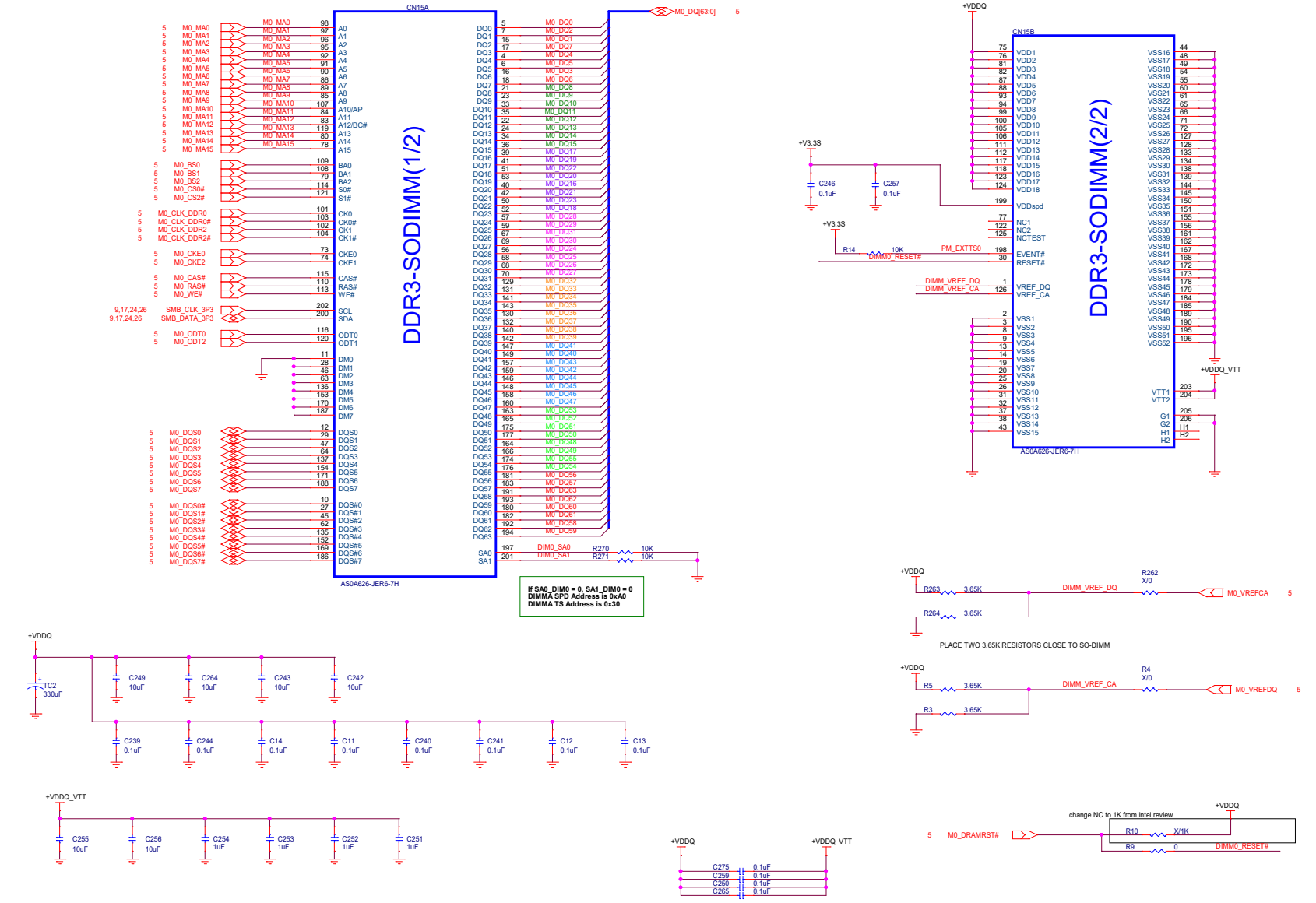
SODIMM#0



AAEON an ASUS assoc. co.	Title: DDR3L SODIMM		
	Size: C	Document Number: PICOAPL1A01	Rev: A0.1
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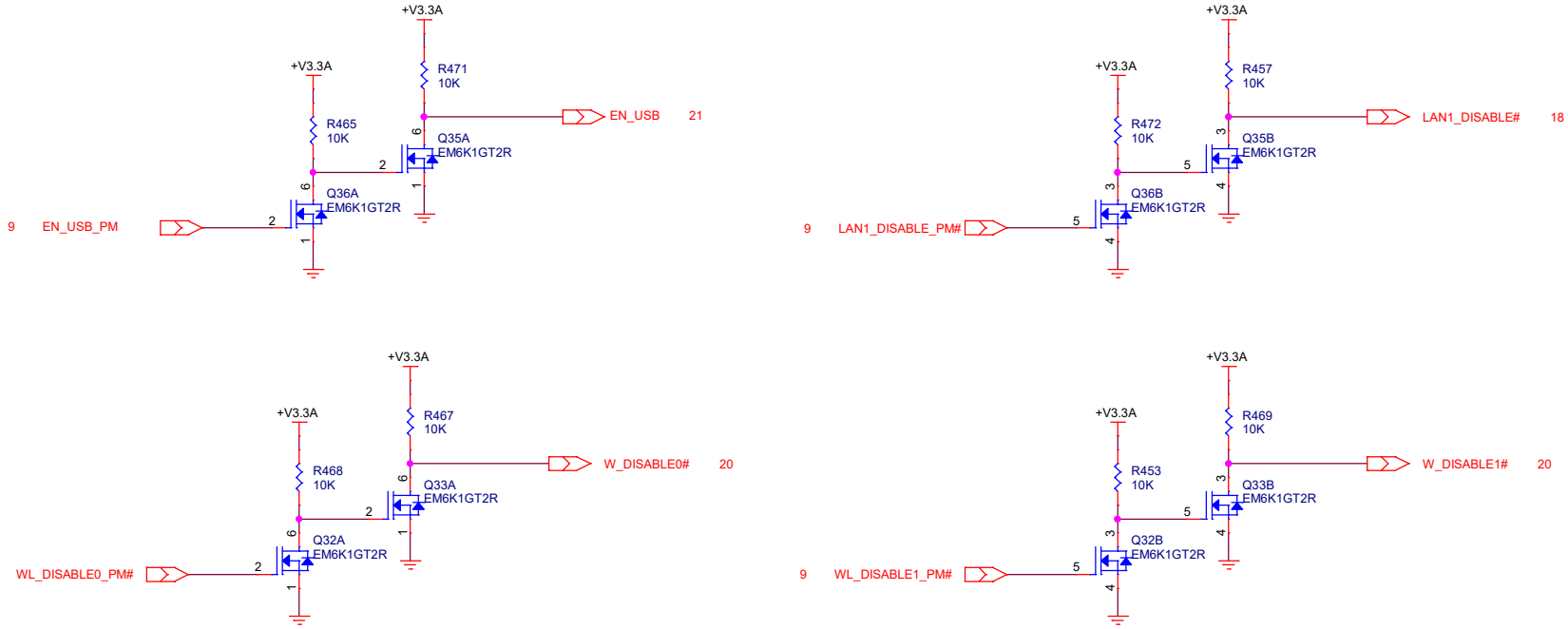
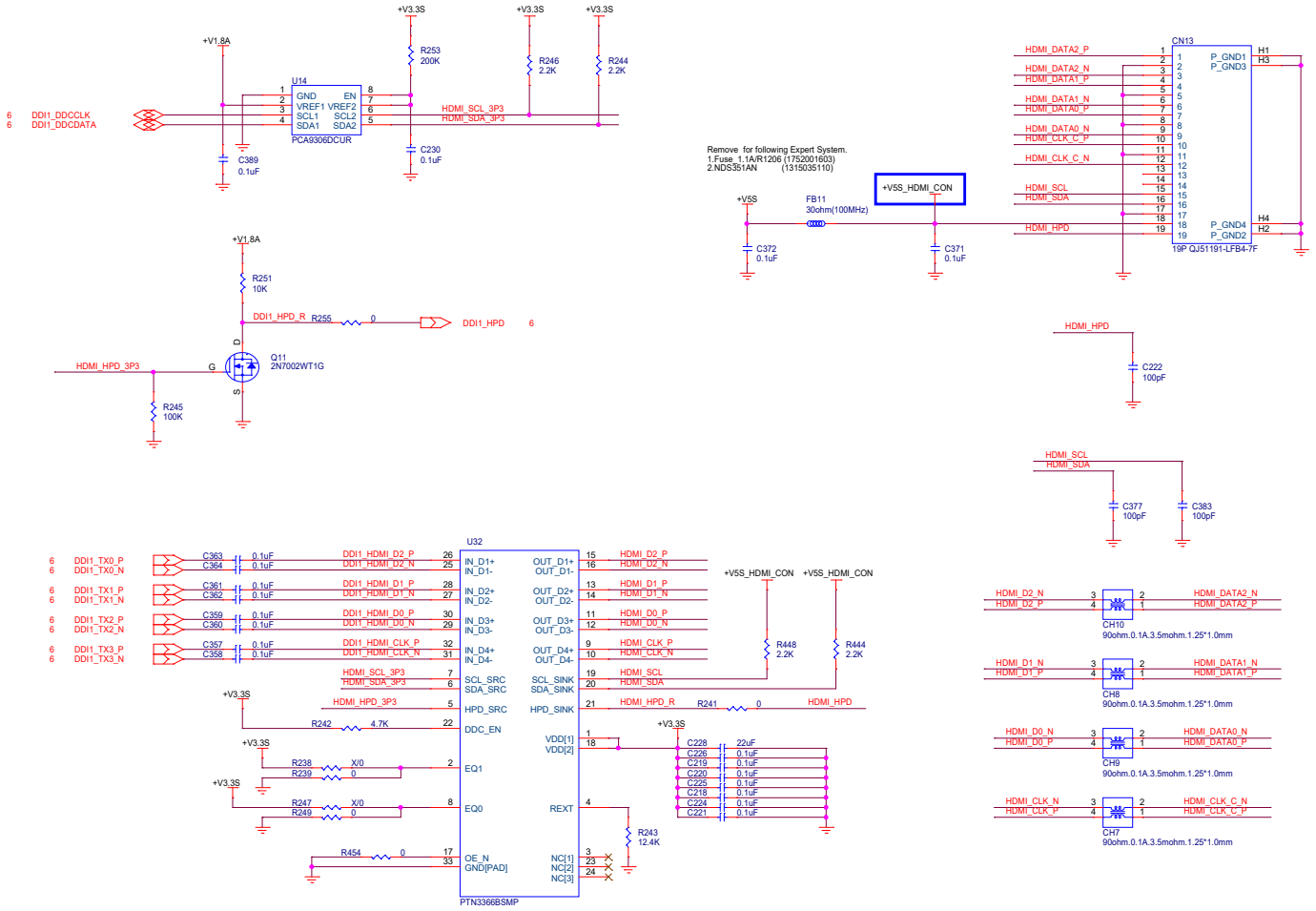


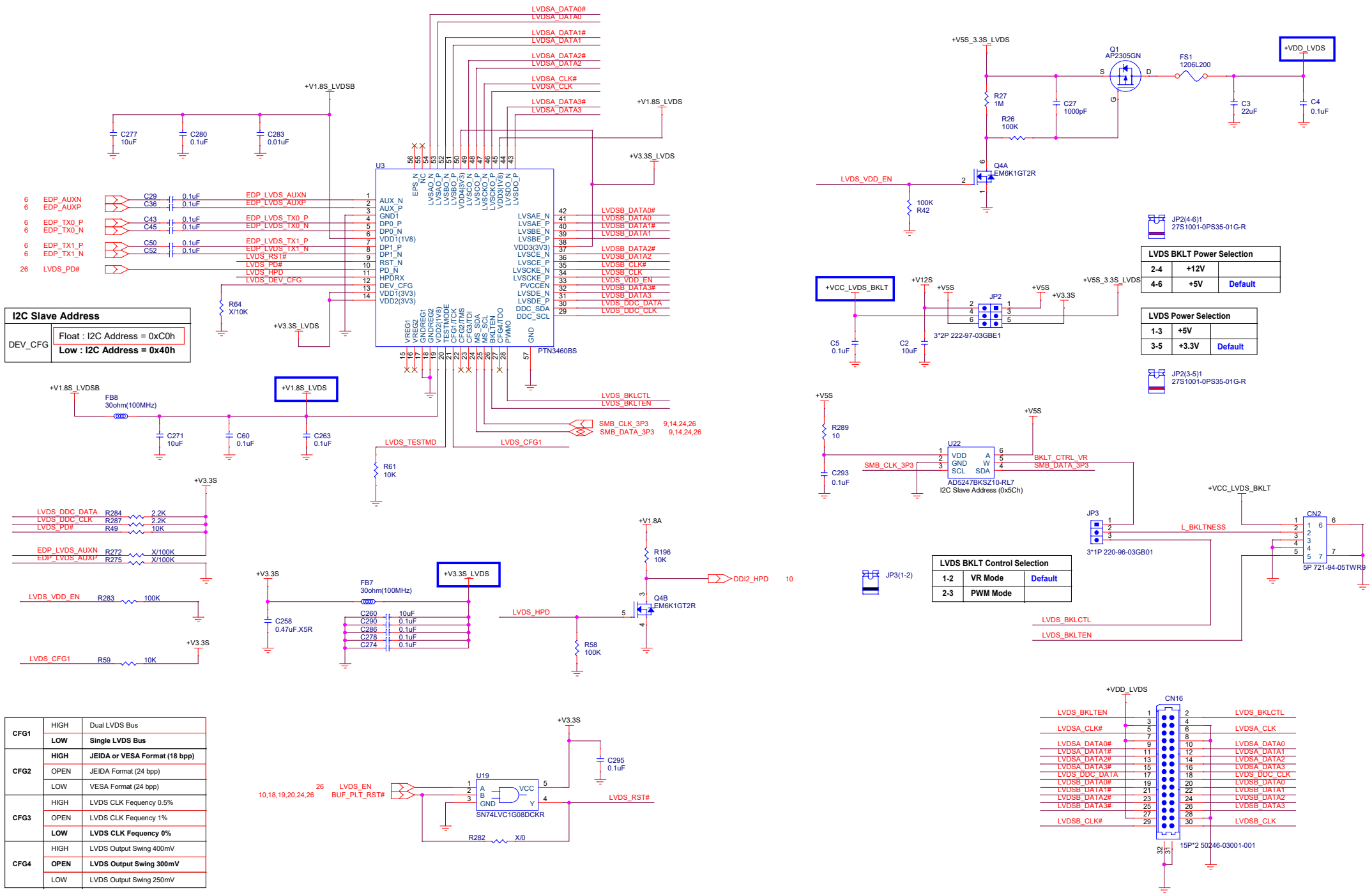
AAEON an ASUS assoc. co.

Title: **Level Shift**		
Size: B	Document Number: **PICOAPL1A01**	Rev: **A0.1**
Date: *Thursday, May 26, 2016*	Sheet: **15** of **32**	

HDMI



Title: HDMI			
Size: C	Document Number: PICOAPL1A01		Rev: A0.1
Date: Thursday, May 26, 2016		Sheet: 16 of 32	


U3
PTN3460BS
+V1.8S_LVDSB
+V1.8S_LVDS
+V3.3S_LVDS
LVDSA_DATA0#
LVDSA_DATA0
LVDSA_DATA1#
LVDSA_DATA1
LVDSA_DATA2#
LVDSA_DATA2
LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA3#
LVDSA_DATA3
LVDSB_DATA0#
LVDSB_DATA0
LVDSB_DATA1#
LVDSB_DATA1
LVDSB_DATA2#
LVDSB_DATA2
LVDSB_CLK#
LVDSB_CLK
LVDS_VDD_EN
LVDSB_DATA3#
LVDSB_DATA3
LVDS_DDC_DATA
LVDS_DDC_CLK
LVDS_BKLCTL
LVDS_BKLTEN
SMB_CLK_3P3
SMB_DATA_3P3
LVDS_TESTMD
LVDS_CFG1
EDP_AUXN
EDP_AUXP
EDP_TX0_P
EDP_TX0_N
EDP_TX1_P
EDP_TX1_N
LVDS_RS1#
LVDS_PD#
LVDS_HPD
LVDS_DEV_CFG
LVDS_PD#
I2C Slave Address
DEV_CFG
Float : I2C Address = 0xC0h
Low : I2C Address = 0x40h
+V5S_3.3S_LVDS
+VDD_LVDS
Q1
AP2305GN
FS1
1206L200
R27
1M
R26
100K
C27
1000pF
C3
22uF
C4
0.1uF
Q4A
EM6K1GT2R
LVDS_VDD_EN
100K
R42
JP2(4-6)1
27S1001-0PS35-01G-R
LVDS BKLT Power Selection
2-4 +12V
4-6 +5V Default
+VCC_LVDS_BKLT
+V12S
+V5S
+V3.3S
JP2
3*2P 222-97-03GBE1
C5
0.1uF
C2
10uF
LVDS Power Selection
1-3 +5V
3-5 +3.3V Default
JP2(3-5)1
27S1001-0PS35-01G-R
R289
10
C293
0.1uF
U22
AD5247BKSZ10-RL7
I2C Slave Address (0x5Ch)
BKLT_CTRL_VR
JP3
3*1P 220-96-03GB01
L_BKLTNESS
CN2
5P 721-94-05TWR9
JP3(1-2)
LVDS BKLT Control Selection
1-2 VR Mode Default
2-3 PWM Mode
FB8
30ohm(100MHz)
C271
10uF
C60
0.1uF
C263
0.1uF
R61
10K
R64
X/10K
R284
2.2K
R287
2.2K
R49
10K
R272
X/100K
R275
X/100K
R283
100K
R59
10K
FB7
30ohm(100MHz)
C258
0.47uF.X5R
C260
10uF
C290
0.1uF
C286
0.1uF
C278
0.1uF
C274
0.1uF
R196
10K
DDI2_HPD
Q4B
EM6K1GT2R
R58
100K
CFG1 HIGH Dual LVDS Bus
CFG1 LOW Single LVDS Bus
CFG2 HIGH JEIDA or VESA Format (18 bpp)
CFG2 OPEN JEIDA Format (24 bpp)
CFG2 LOW VESA Format (24 bpp)
CFG3 HIGH LVDS CLK Fequency 0.5%
CFG3 OPEN LVDS CLK Fequency 1%
CFG3 LOW LVDS CLK Fequency 0%
CFG4 HIGH LVDS Output Swing 400mV
CFG4 OPEN LVDS Output Swing 300mV
CFG4 LOW LVDS Output Swing 250mV
U19
SN74LVC1G08DCKR
LVDS_EN
BUF_PLT_RST#
LVDS_RST#
R282
X/0
C295
0.1uF
CN16
15P*2 50246-03001-001
AAEON
an ASUS assoc. co.
Title
PTN3460 eDP to LVDS
Size Custom
Document Number PICOAPL1A01
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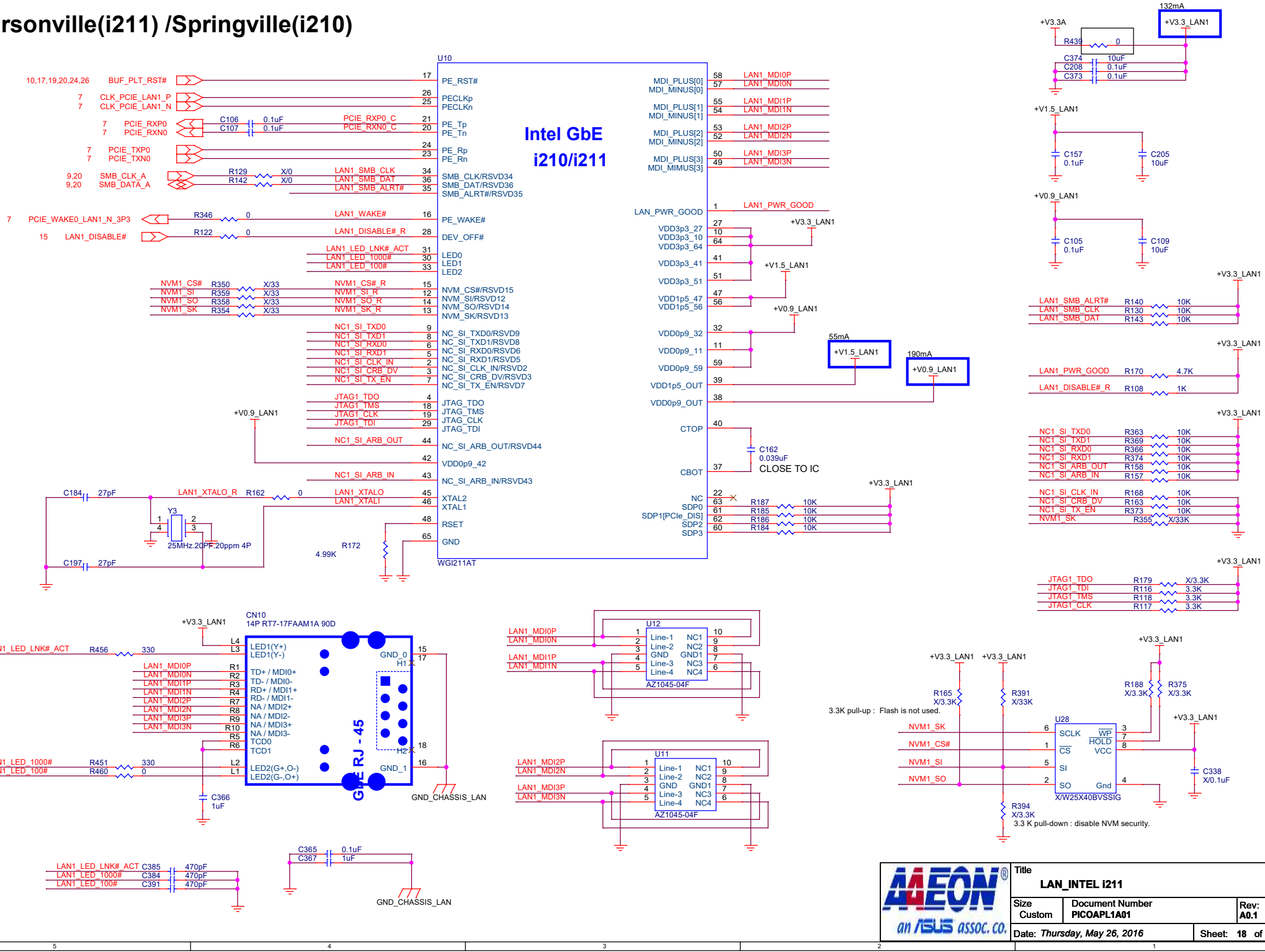
Pearsonville(i211) /Springville(i210)



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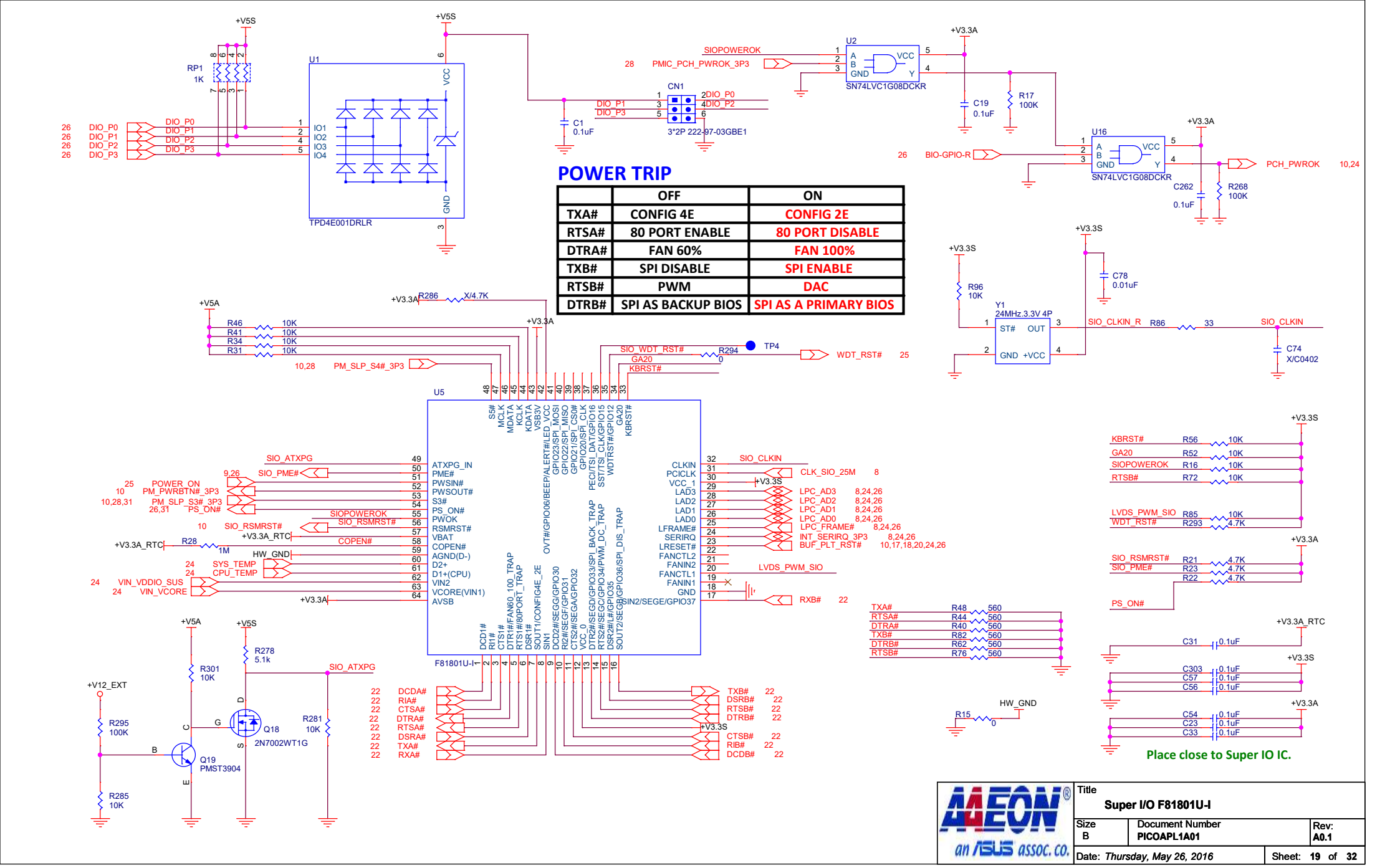
Size: Custom	Document Number: PICOAPL1A01		Rev: A0.1
Date: Thursday, May 26, 2016		Sheet: 18 of 32	


POWER TRIP
OFF
ON
TXA#
CONFIG 4E
CONFIG 2E
RTSA#
80 PORT ENABLE
80 PORT DISABLE
DTRA#
FAN 60%
FAN 100%
TXB#
SPI DISABLE
SPI ENABLE
RTSB#
PWM
DAC
DTRB#
SPI AS BACKUP BIOS
SPI AS A PRIMARY BIOS
U1
TPD4E001DRLR
U2
SN74LVC1G08DCKR
U16
SN74LVC1G08DCKR
CN1
3*2P 222-97-03GBE1
U5
F81801U-I
Y1
24MHz,3.3V 4P
Q18
2N7002WT1G
Q19
PMST3904
Place close to Super IO IC.
Title
Super I/O F81801U-I
Size
B
Document Number
PICOAPL1A01
Rev:
A0.1
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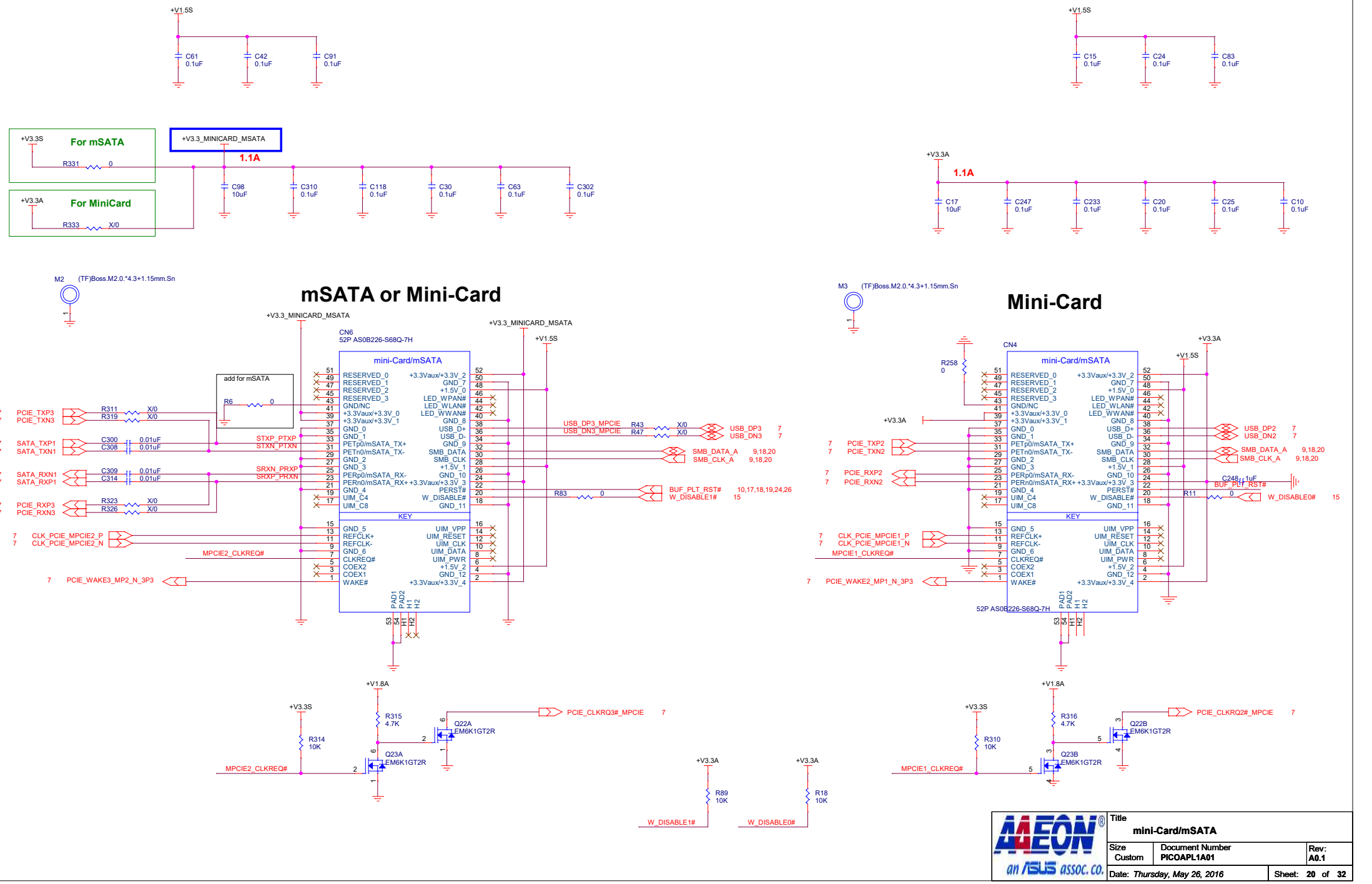
+V1.5S
C61 0.1uF
C42 0.1uF
C91 0.1uF
+V3.3S
For mSATA
R331 0
+V3.3A
For MiniCard
R333 X/0
+V3.3_MINICARD_MSATA
1.1A
C98 10uF
C310 0.1uF
C118 0.1uF
C30 0.1uF
C63 0.1uF
C302 0.1uF
+V1.5S
C15 0.1uF
C24 0.1uF
C83 0.1uF
+V3.3A
1.1A
C17 10uF
C247 0.1uF
C233 0.1uF
C20 0.1uF
C25 0.1uF
C10 0.1uF
M2 (TF)Boss.M2.0.*4.3+1.15mm.Sn
mSATA or Mini-Card
+V3.3_MINICARD_MSATA
CN6
52P AS0B226-S68Q-7H
mini-Card/mSATA
add for mSATA
R6 0
PCIE_TXP3
PCIE_TXN3
R311 X/0
R319 X/0
SATA_TXP1
SATA_TXN1
C300 0.01uF
C308 0.01uF
STXP_PTXP
STXN_PTXN
SATA_RXN1
SATA_RXP1
C309 0.01uF
C314 0.01uF
SRXN_PRXP
SRXP_PRXN
PCIE_RXP3
PCIE_RXN3
R323 X/0
R326 X/0
CLK_PCIE_MPCIE2_P
CLK_PCIE_MPCIE2_N
MPCIE2_CLKREQ#
PCIE_WAKE3_MP2_N_3P3
RESERVED_0
RESERVED_1
RESERVED_2
RESERVED_3
GND/NC
+3.3Vaux/+3.3V_0
+3.3Vaux/+3.3V_1
GND_0
GND_1
PETp0/mSATA_TX+
PETn0/mSATA_TX-
GND_2
GND_3
PERp0/mSATA_RX-
PERn0/mSATA_RX+
GND_4
UIM_C4
UIM_C8
+3.3Vaux/+3.3V_2
GND_7
+1.5V_0
LED_WPAN#
LED_WLAN#
LED_WWAN#
GND_8
USB_D+
USB_D-
GND_9
SMB_DATA
SMB_CLK
+1.5V_1
GND_10
+3.3Vaux/+3.3V_3
PERST#
W_DISABLE#
GND_11
KEY
GND_5
REFCLK+
REFCLK-
GND_6
CLKREQ#
COEX2
COEX1
WAKE#
UIM_VPP
UIM_RESET
UIM_CLK
UIM_DATA
UIM_PWR
+1.5V_2
GND_12
+3.3Vaux/+3.3V_4
PAD1
PAD2
H1
H2
USB_DP3_MPCIE
USB_DN3_MPCIE
R43 X/0
R47 X/0
USB_DP3
USB_DN3
SMB_DATA_A 9,18,20
SMB_CLK_A 9,18,20
R83 0
BUF_PLT_RST# 10,17,18,19,24,26
W_DISABLE1# 15
+V1.8A
+V3.3S
R315 4.7K
R314 10K
Q22A EM6K1GT2R
Q23A EM6K1GT2R
PCIE_CLKRQ3#_MPCIE
MPCIE2_CLKREQ#
+V3.3A
R89 10K
R18 10K
W_DISABLE1#
W_DISABLE0#
M3 (TF)Boss.M2.0.*4.3+1.15mm.Sn
Mini-Card
CN4
52P AS0B226-S68Q-7H
R258 0
PCIE_TXP2
PCIE_TXN2
PCIE_RXP2
PCIE_RXN2
CLK_PCIE_MPCIE1_P
CLK_PCIE_MPCIE1_N
MPCIE1_CLKREQ#
PCIE_WAKE2_MP1_N_3P3
C248 1uF
BUF_PLT_RST#
R11 0
W_DISABLE0# 15
R316 4.7K
R310 10K
Q22B EM6K1GT2R
Q23B EM6K1GT2R
PCIE_CLKRQ2#_MPCIE
AAEON
an ASUS assoc. co.
Title
mini-Card/mSATA
Size Custom
Document Number PICOAPL1A01
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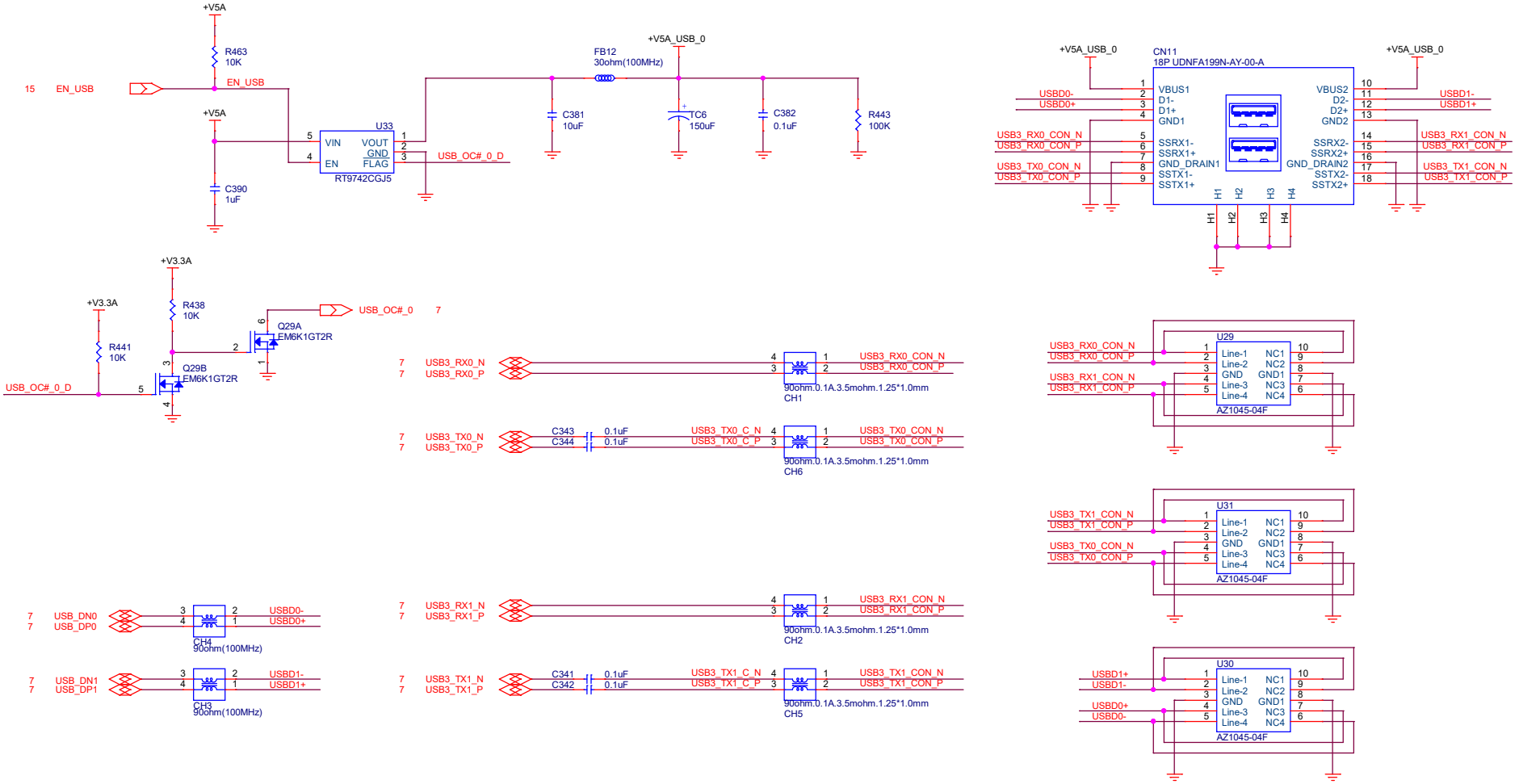
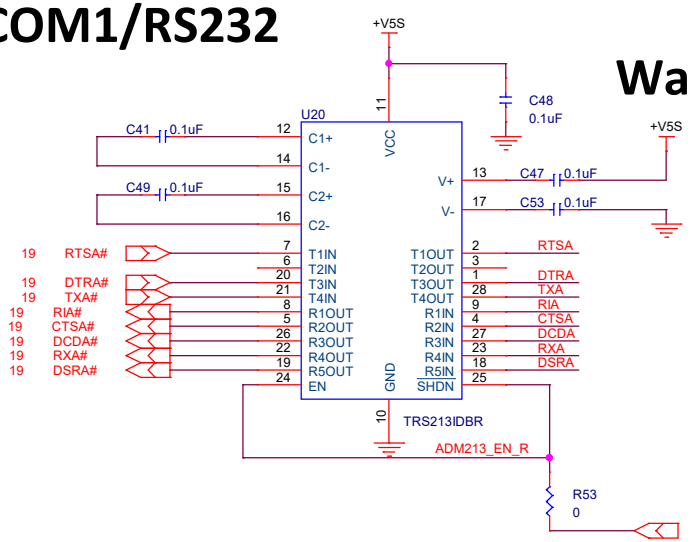
USB3.0 x 2

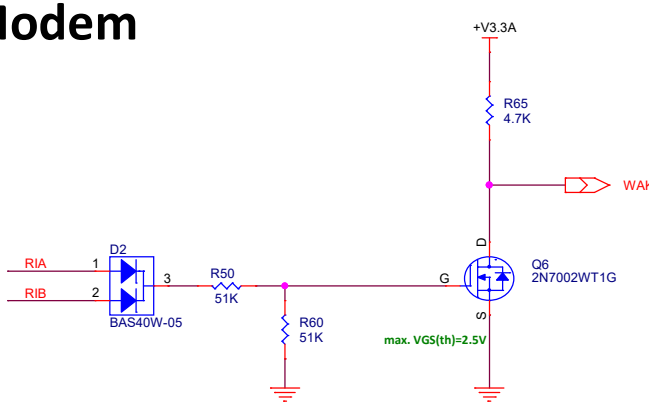


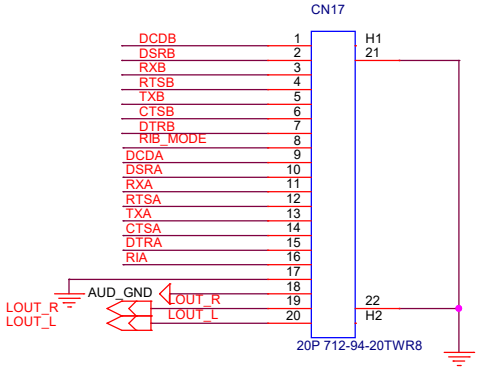
AAEON an ASUS assoc. co.	Title: USB 3.0/2.0 PORT	
Size: Custom	Document Number: PICOAPL1A01	Rev: A0.1
Date: Thursday, May 26, 2016		Sheet: 21 of 32

COM1/RS232

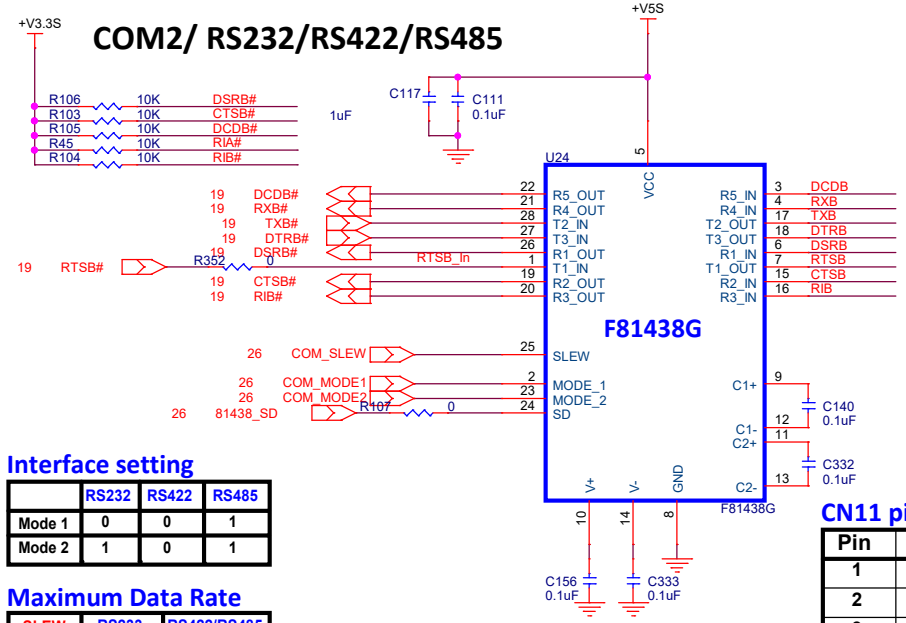


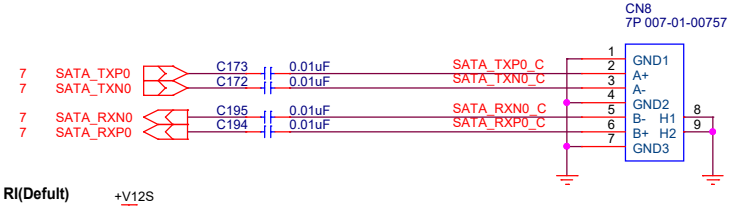
Wake on Modem

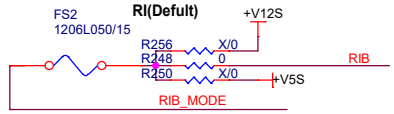


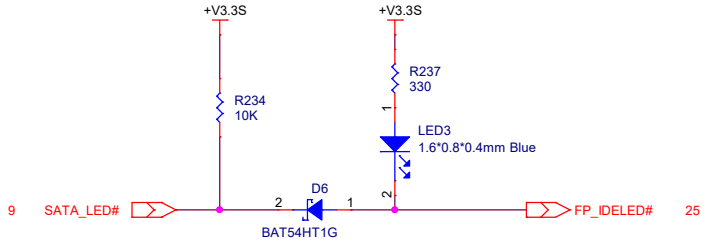


COM2/ RS232/RS422/RS485









Interface setting

	RS232	RS422	RS485
Mode 1	0	0	1
Mode 2	1	0	1

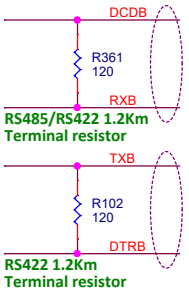
Maximum Data Rate

SLEW	RS233	RS422/RS485
1	250kbps	250kbps
0	1Mbps	10Mbps

Layout note:
DCDB & RXB as differential pair.
TXB & DTRB as differential pair.

CN11 pin assignment

Pin	RS232	RS422	RS485
1	DCD	TX-	DATA-
2	DSR		
3	RX	TX+	DATA+
4	RTS		
5	TX	RX+	
6	CTS		
7	DTR	RX-	
8	RI		



AAEON an ASUS assoc. co.

Title: Serial Port 1/2/SATA		
Size: B	Document Number: PICOAPL1A01	Rev: A0.1
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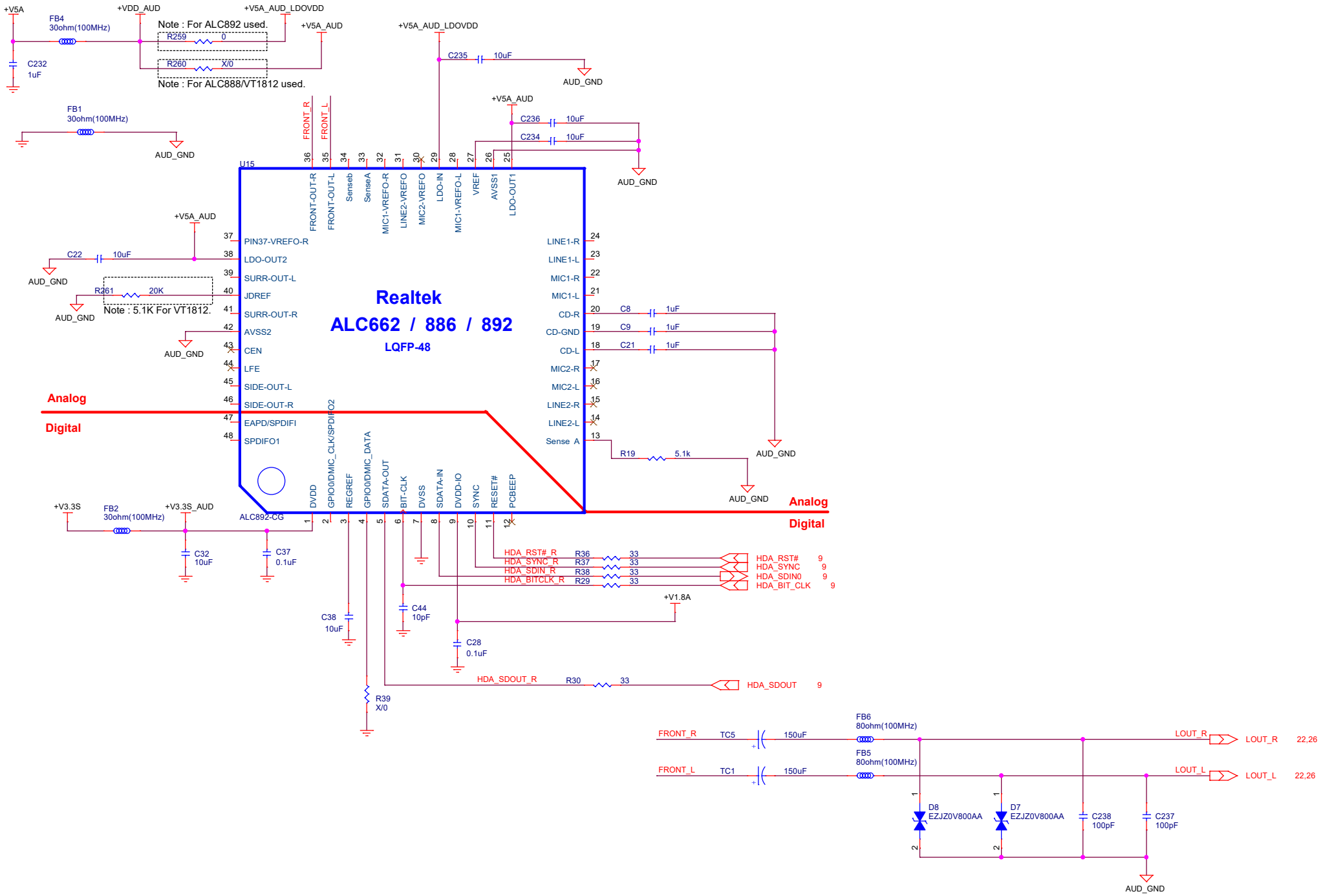
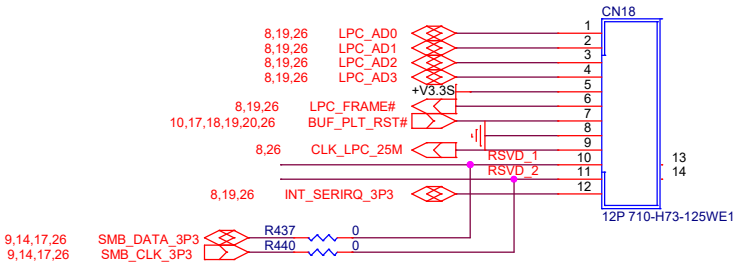
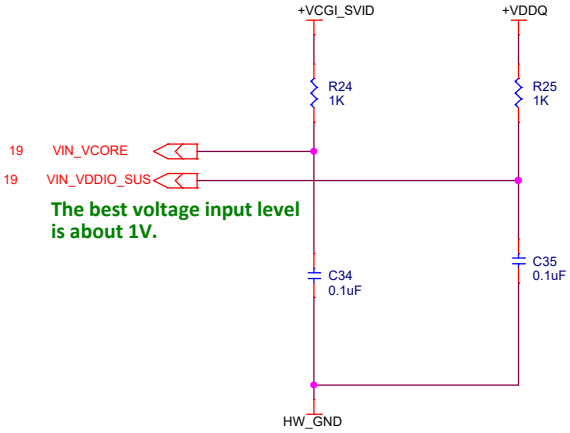


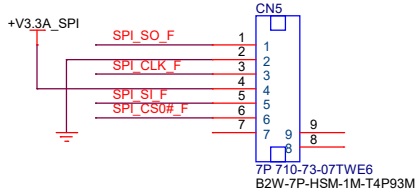
AAEON an ASUS assoc. co.	Title: HD Audio - ALC892	
	Size: Custom	Document Number: PICOAPL1A01 — Rev: A0.1
	Date: Thursday, May 26, 2016	Sheet: 23 of 32

LPC Debug Connector

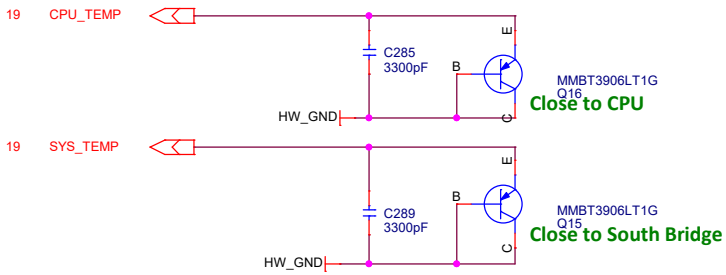


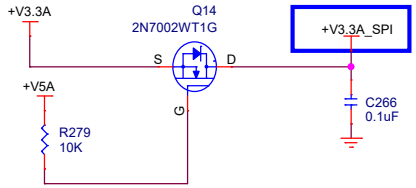
Voltage Monitor(Vcore, Vmem)



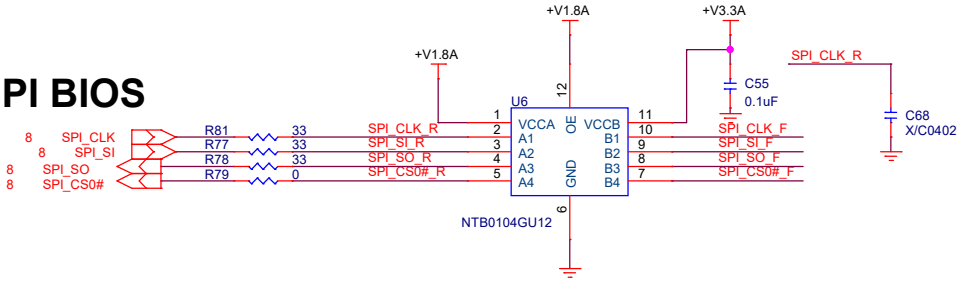


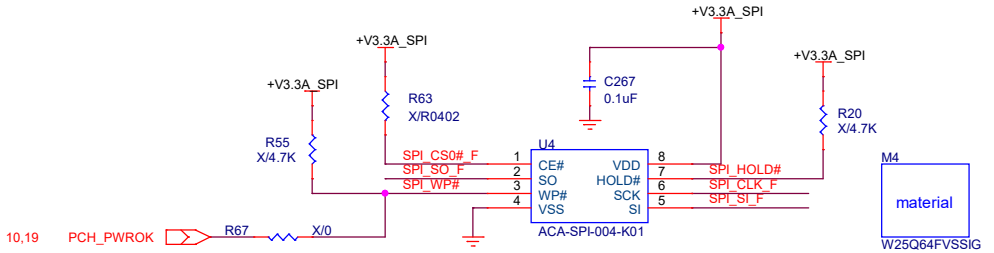
Temperature Monitor(CPU, SYS)





SPI BIOS

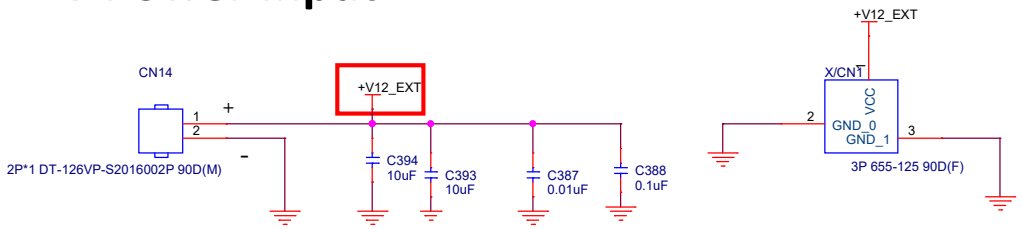




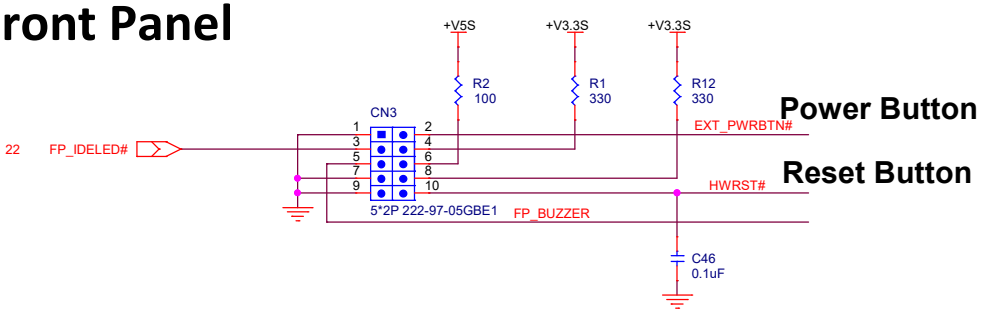
8 pin : 1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0
14S6206403 (TF)IC.64 Mbit SPI Flash.SOIC-8P 208mil.SMD.Winbond.W25Q64FVSSIG

AAEON an ASUS assoc. co.	Title: **H/W Mon/ Debug /CMOS**		
	Size: **B**	Document Number: **PICOAPL1A01**	Rev: **A0.1**
	Date: *Thursday, May 26, 2016*	Sheet: **24** of **32**	

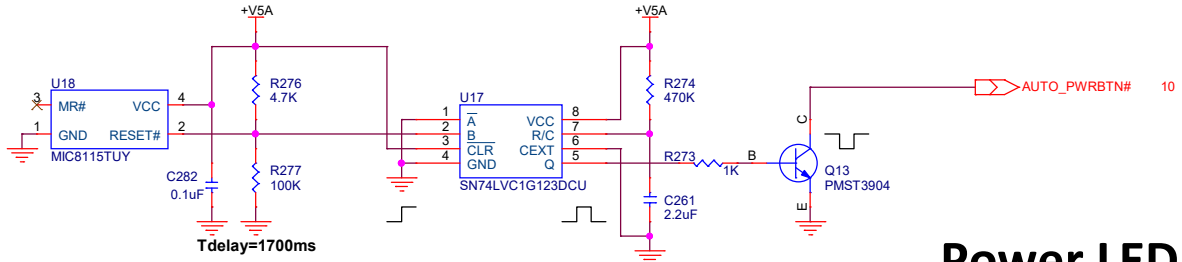
+12V Power Input

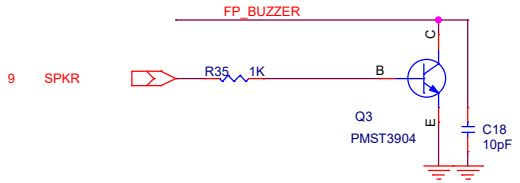


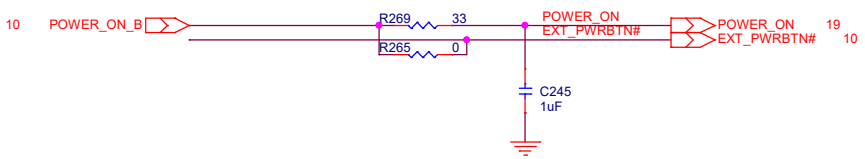
Front Panel



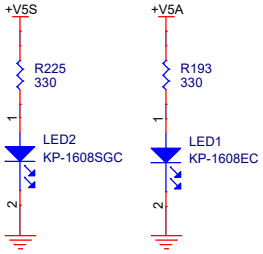
Auto Power Button



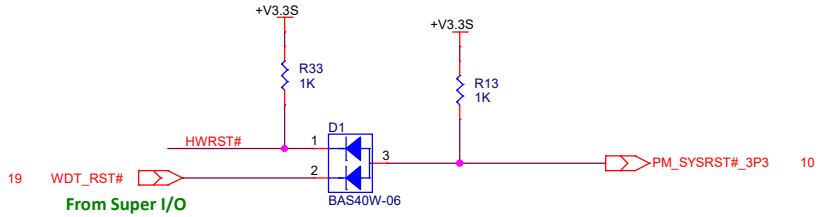




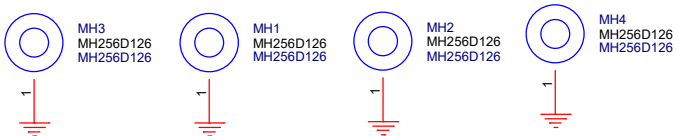
Power LED



System Reset



Mounting Holes / Non-PTH

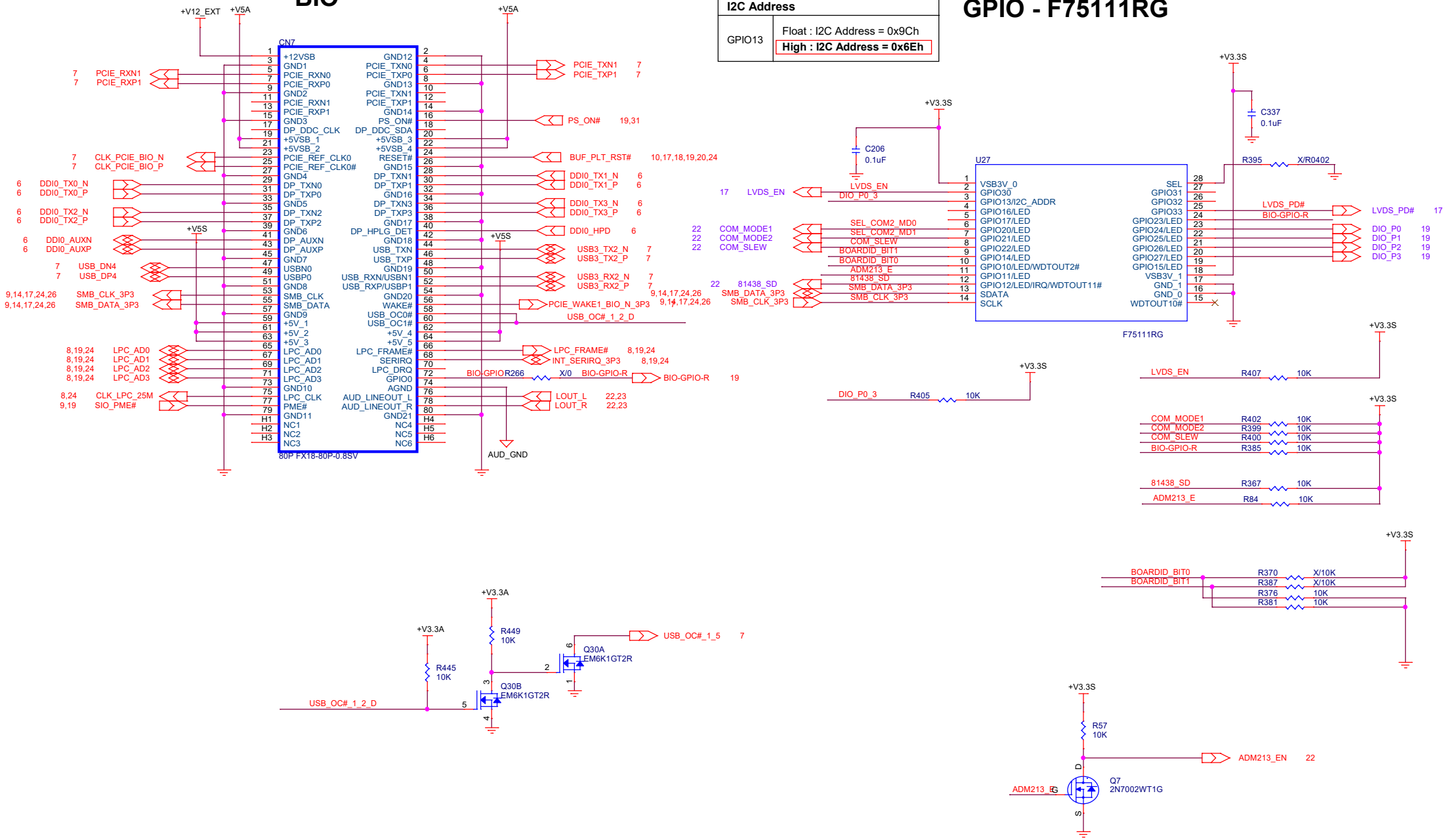


AAEON an ASUS assoc. co.	Title: Auto Power Button/Power in	
Size: B	Document Number: PICOAPL1A01	Rev: A0.1
Date: Thursday, May 26, 2016	Sheet: 25 of 32	

BIO

GPIO - F75111RG

I2C Address	
GPIO13	Float : I2C Address = 0x9Ch
	High : I2C Address = 0x6Eh



Title	**BIO/GPIO**
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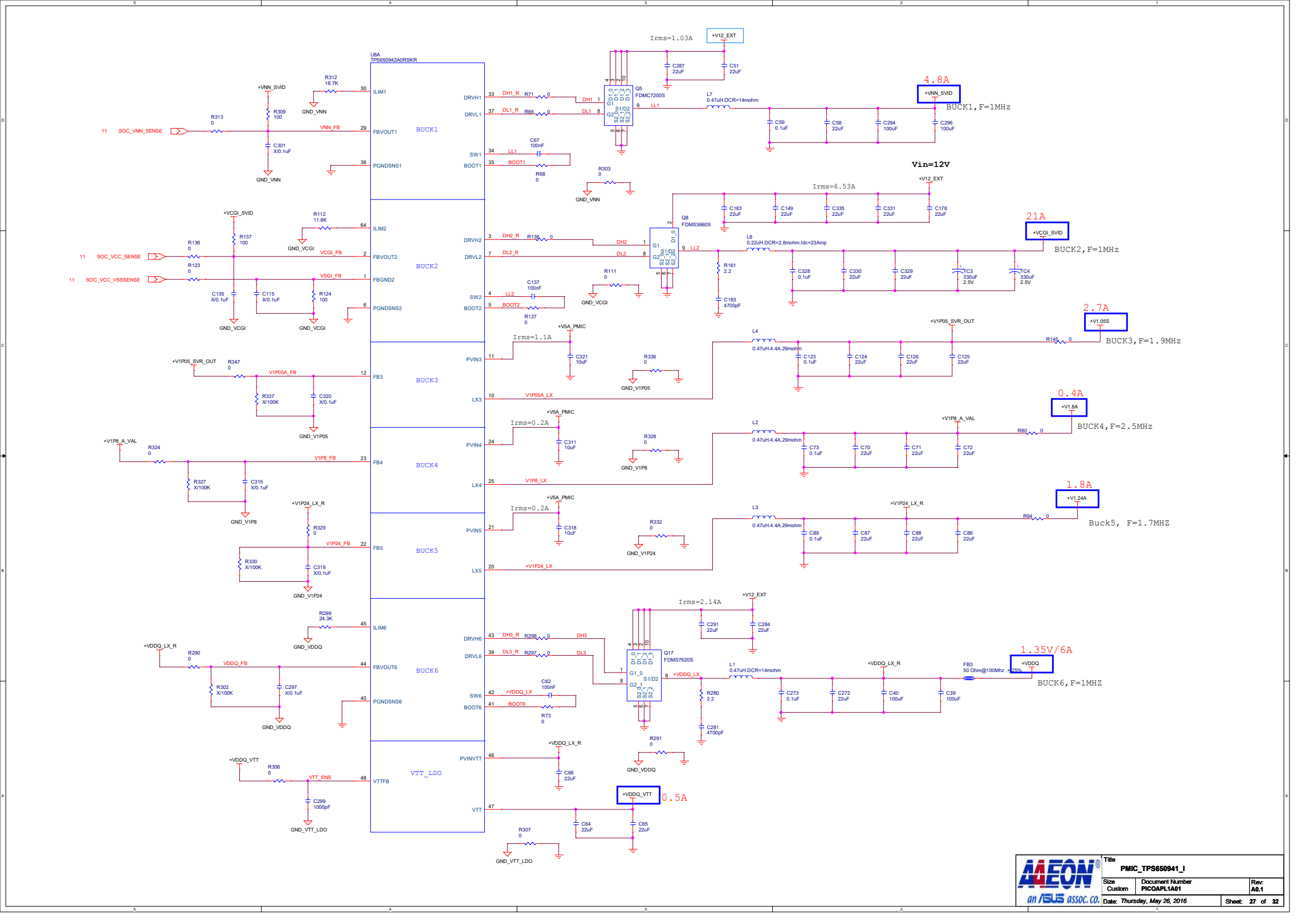
U8A
TPS650942A0RSKR
BUCK1
BUCK2
BUCK3
BUCK4
BUCK5
BUCK6
VTT_LDO
ILIM1
FBVOUT1
PGNDSNS1
ILIM2
FBVOUT2
FBGND2
PGNDSNS2
FB3
FB4
FB5
ILIM6
FBVOUT6
PGNDSNS6
VTTFB
DRVH1
DRVL1
SW1
BOOT1
DRVH2
DRVL2
SW2
BOOT2
PVIN3
LX3
PVIN4
LX4
PVIN5
LX5
DRVH6
DRVL6
SW6
BOOT6
PVINVTT
VTT
+V12_EXT
+VNN_SVID
+VCGI_SVID
+V1P05S
+V1.8A
+V1P24A
+VDDQ
+VDDQ_VTT
Irms=1.03A
Irms=6.53A
Irms=1.1A
Irms=0.2A
Irms=0.2A
Irms=2.14A
4.8A
21A
2.7A
0.4A
1.8A
1.35V/6A
0.5A
Vin=12V
BUCK1,F=1MHz
BUCK2,F=1MHz
BUCK3,F=1.9MHz
BUCK4,F=2.5MHz
Buck5, F=1.7MHZ
BUCK6,F=1MHZ
Q5 FDMC7200S
Q8 FDMS3660S
Q17 FDMS7620S
L7 0.47uH.DCR=14mohm
L8 0.22uH.DCR=2.8mohm.Idc=23Amp
L4 0.47uH.4.4A.29mohm
L2 0.47uH.4.4A.29mohm
L3 0.47uH.4.4A.29mohm
L1 0.47uH.DCR=14mohm
SOC_VNN_SENSE
SOC_VCC_SENSE
SOC_VCC_VSSSENSE
+VNN_SVID
+VCGI_SVID
+V5A_PMIC
+V1P05_SVR_OUT
+V1P8_A_VAL
+V1P24_LX_R
+VDDQ_LX_R
+VDDQ_VTT
+VDDQ_LX
V1P05A_FB
V1P8_FB
V1P24_FB
VDDQ_FB
VTT_SNS
V1P05A_LX
V1P8_LX
+V1P24_LX
VSGI_FB
VCGI_FB
VNN_FB
DH1
DL1
DH2
DL2
DH3
DL3
LL1
LL2
BOOT1
BOOT2
BOOT6
GND_VNN
GND_VCGI
GND_V1P05
GND_V1P8
GND_V1P24
GND_VDDQ
GND_VTT_LDO
Title
PMIC_TPS650941_I
Size
Custom
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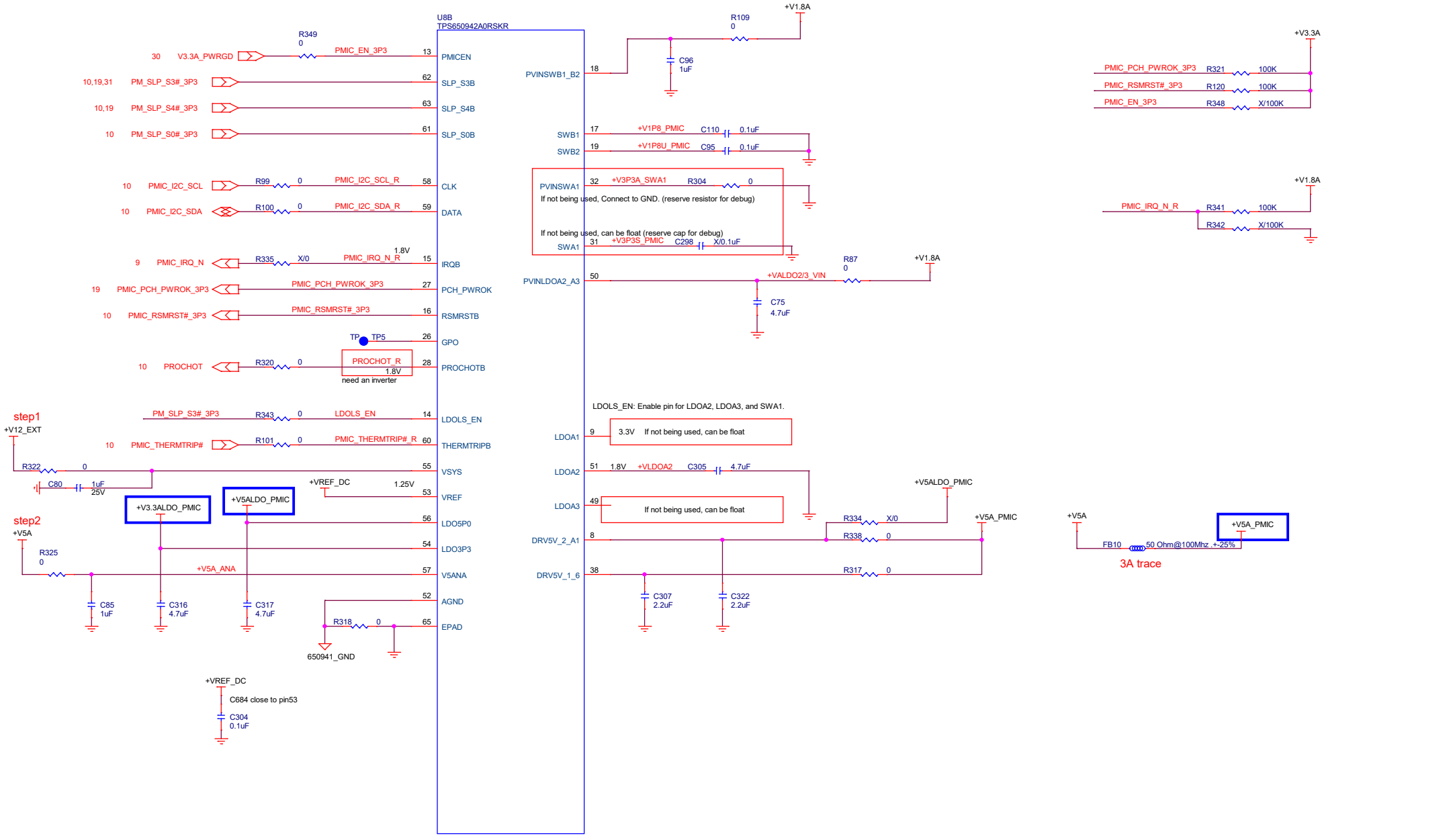
an ASUS assoc. co.



AAEON an ASUS assoc. co.	Title: PMIC_TPS650941_II	
	Size: Custom	Document Number: PICOAPL1A01 — Rev: A0.1
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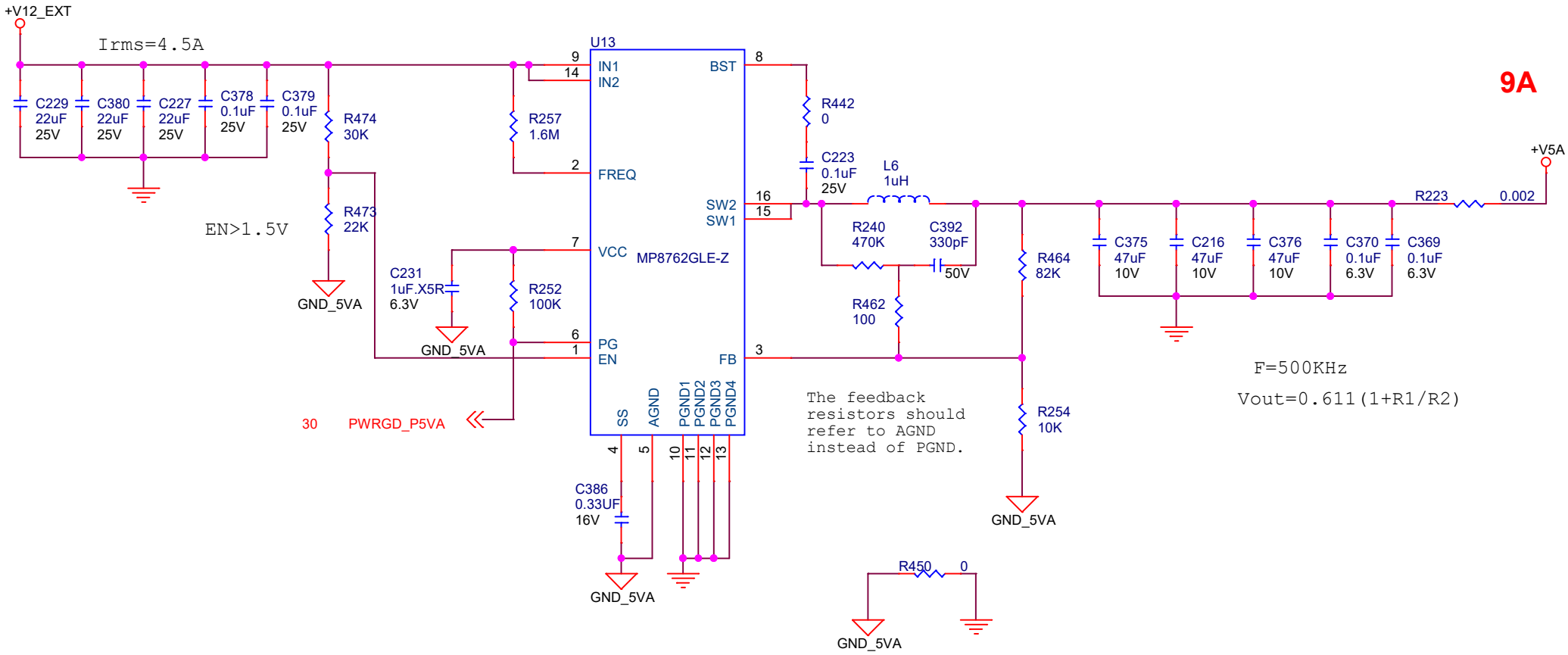

AAEON an ASUS assoc. co.	Title: **Power VR : +V5A**	
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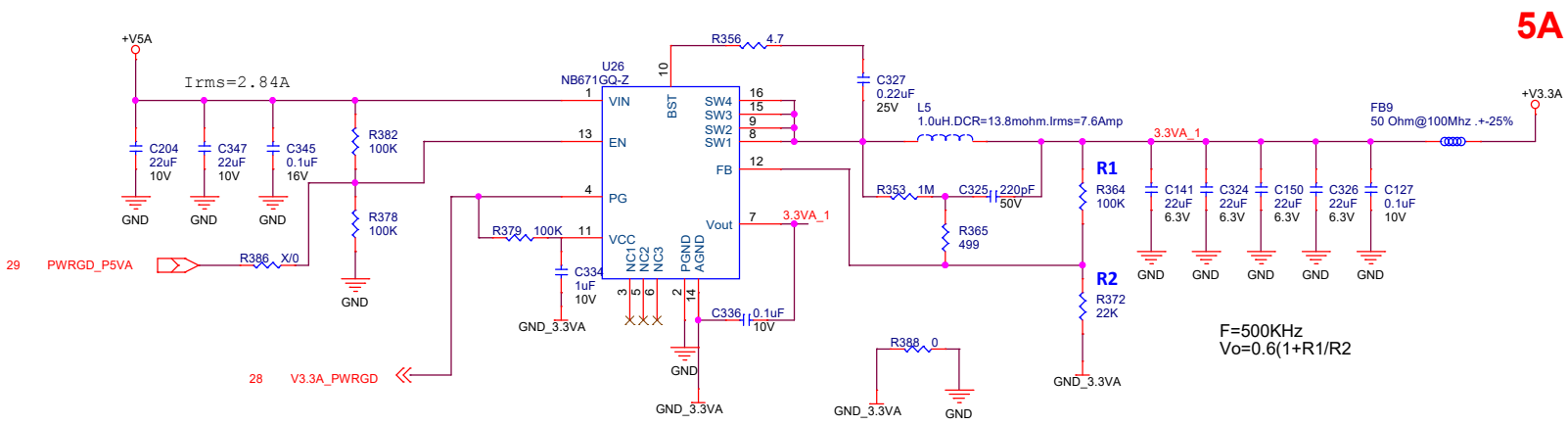
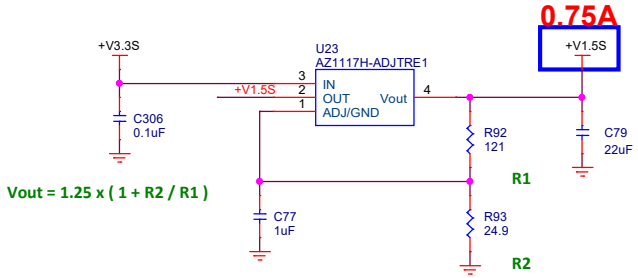
1.35V<EN<12V
EN voltage should be lower than 12V





AAEON an ASUS assoc. co.	Title: Power VR : +V3.3A.+V1.5S	
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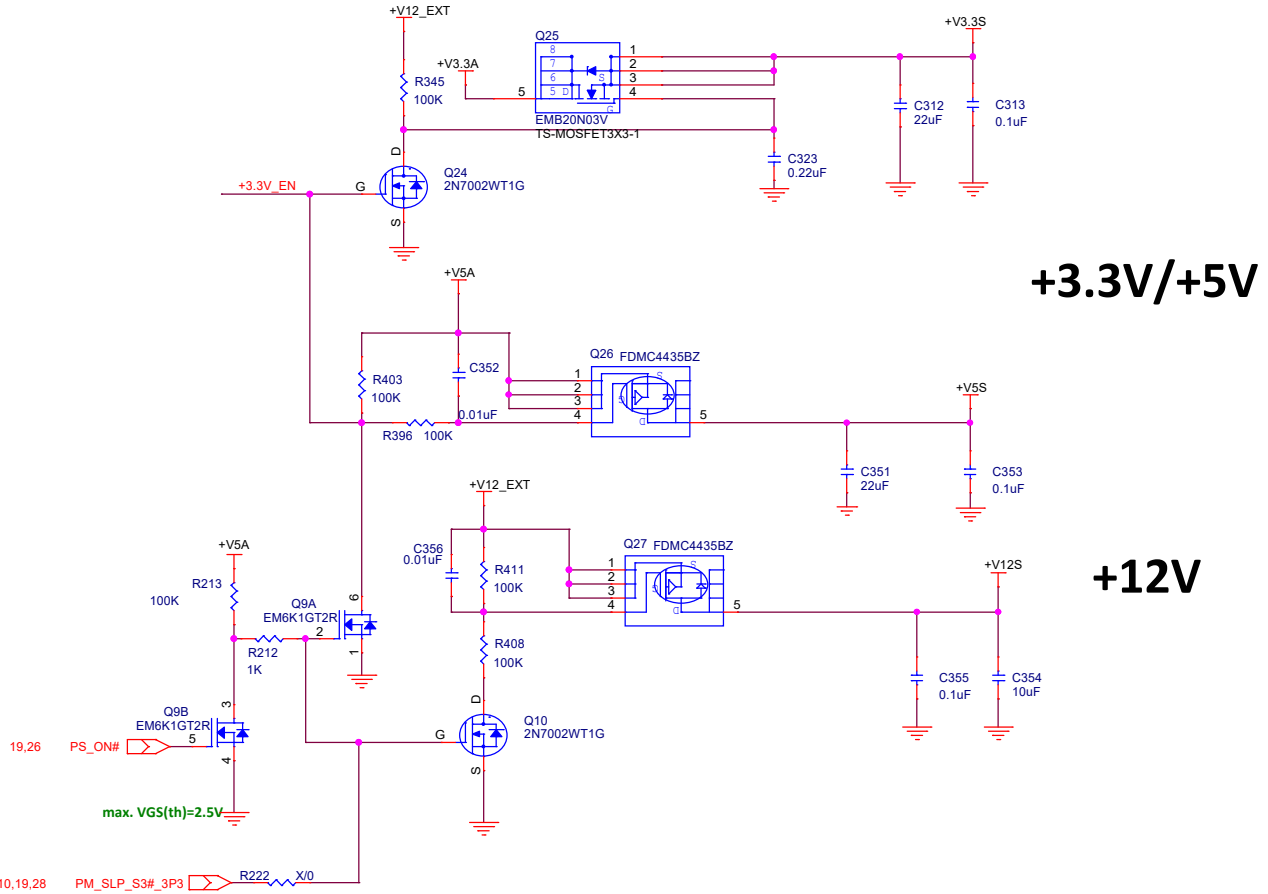

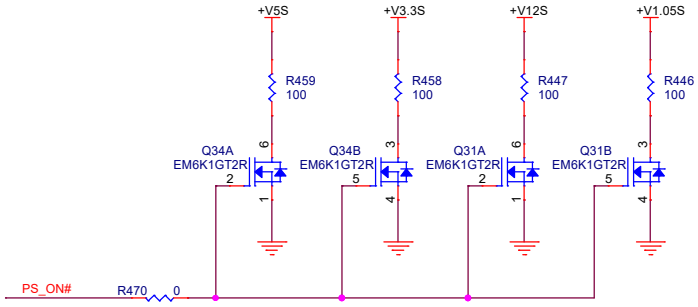

<Variant Name>

AAEON an ASUS assoc. co.	Title: **Power Sequence Logic**	
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HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2016/3/20	A0.1	First Release.	1-31	Daniel	Chienkow

AAEON an ASUS assoc. co.

Title: Revision History

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