PARADE TECHNOLOGIES INC.

TEL : 408-329-5540
FAX : 408-329-5541
Email: sales@paradetech.com
Website: www.paradetech.com

PS8625 Embedded DisplayPort™ to LVDS Converter Datasheet

Version 2.1

July 17, 2014

REVISION HISTORY

Version 0.5, 11/10/2010

1. Initial Release

Version 0.8, 03/23/2010

1. Separated the P/N as PS8625 without HDCP key and PS8625HDE with HDCP key

Version 0.85, 04/06/2011

1. Separated Package & Order Information for PS8625 and PS8625HDE

Version 0.9, 06/09/2011

1. Updated Physical Dimension

Version 1.0, 08/23/2011

1. Updated characteristics data
2. Added Spread Spectrum descriptions
3. Added On-chip switching regulator layout guide

Version 1.1, 12/06/2011

1. Updated LVDS interface descriptions
2. Updated Pin33 from ENPVCC to ENPVCC/I2C_ADDR

Version 1.2, 1/5/2012

1. Updated power up and reset timing sequence

Version 1.3, 5/16/2012

1. Updated Thermal Pad layout Guidelines

Version 1.4, 7/13/2012

1. Updated Operating Temperature Range to -20°C to 70°C

Version 1.5, 7/26/2012

1. Added Cu wire order information
2. Updated T1 Min value

Version 1.6, 10/10/2012

1. Added 1.35V core power supply support
2. Updated power consumption

Version 1.7, 3/1/2013

1. Updated T1 Min value

Version 1.8, 2/6/2014

1. Updated order information

Version 1.9, 4/8/2014

1. Remove sDRRS support

Version 2.0, 7/9/2014

1. Updated order information

Version 2.1, 7/17/2014

1. Updated order information

KEY FEATURES

- **DisplayPort Input**
  - Compliant to VESA DisplayPort™ Specification 1.1a
  - Compliant to VESA Embedded DisplayPort ™ Specification 1.2
  - Supports 1-lane and 2-lane main link configuration
  - Supports link rates 2.7Gbps and 1.62Gbps
  - Supports fast link training, no link training and full link training
  - Supports 18/24/30 bpp RGB color format input, up to 1920x1200@60Hz, 30-bit color depth
  - Supports HDCP 1.3 for Content Protection, integrated HDCP key ROM (PS8625HDE only)
  - Supports eDP display authentication option *Alternate Scrambler Seed Reset (ASSR)* and *Alternate Framing*
  - Supports eDP power saving scheme of *Dynamic Refresh Rate* (DRR) and nvDPS
  - Supports DisplayPort™ standard SSC 0.5% down spreading
- **LVDS Interface**
  - Supports single link or dual link LVDS output, clock rate up to 135MHz
  - Supports up to 1920x1200@60Hz resolution
  - Supports 18-bpp or 24-bpp LVDS output
  - Supports VESA or JEIDA data mapping formats
  - Supports LVDS clock central spreading of 0.25%, 0.5%, 0.75%, 1.0%, 1.25%, 1.5%, 1.75% and 2.0%, modulation frequency of 10kHz, 20kHz, 30kHz and 40kHz with +/-5% error
  - Supports LCD panel power sequence control
  - Supports PWM pass through and on-chip PWM signal generation
- CrystalFree technology – no external timing reference needed
- Optional I2C slave interface for chip control
- Supports I2C over AUX protocol for EDID relay from panel to DP source
- Firmware-less operation, supports hardware pin configuration or initial code configuration
- Supports various LVDS output modes configured by pins, control I2C or AUX channel
- Optional I2C master for external EEPROM initial code loading and configurations
- Single 3.3V/2.5V supply when using on-chip integrated switching regulator from 3.3V/2.5V to 1.2V core power
- 3.3V/2.5V and 1.2V/1.35V power supply when not using on-chip integrated switching regulator
- Ultra low power consumption
- ESD: HBM 8kV at connector pins
- -20°C to 70°C Operating Temperature Range
- 56-pin 7x7mm Halogen free QFN RoHS package

APPLICATIONS

- Notebook motherboard with LVDS panel
- All-In-One PC

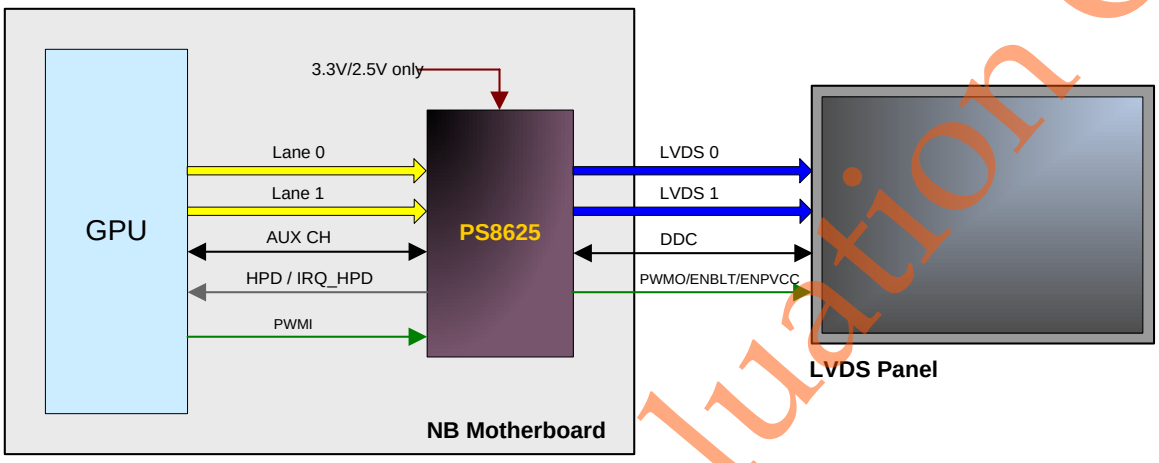


Figure1. Typical Application

DESCRIPTION

PS8625 is an embedded DisplayPort™ (eDP) to LVDS converter which receives video streams from DisplayPort™ link and converts to LVDS output to support LVDS panels on new mobile PC platforms which has no LVDS interface. PS8625 provides the DP to LVDS conversion for any possible close box applications such as in All-In-One desk top application too.

PS8625 DP receiver supports link rate 2.7Gbps (HBR) and 1.62Gbps (RBR) over 1 or 2 lanes main link. It can accept 18/24/30 bpp RGB video formats from GPU eDP interface with maximum 1920x1200@60Hz, 30-bit color depth. The half-duplex, bi-directional AUX channel supports link services, EDID relay from LVDS panel or LVDS output mode configuration.

PS8625 LVDS interface supports both single link and dual link output with clock rate up to 135MHz. Each LVDS channel has 4 data pairs and 1 clock pair which support 18-bpp and 24-bpp color depth RGB output, VESA or JEIDA data mapping formats. The LVDS interface output mode can be flexibly configured by pins, control I2C or AUX channel.

The system level block diagram of PS8625 is described in Figure 2. Detailed descriptions of each functional block are given in the following sections.

FUNCTIONAL BLOCK DIAGRAM

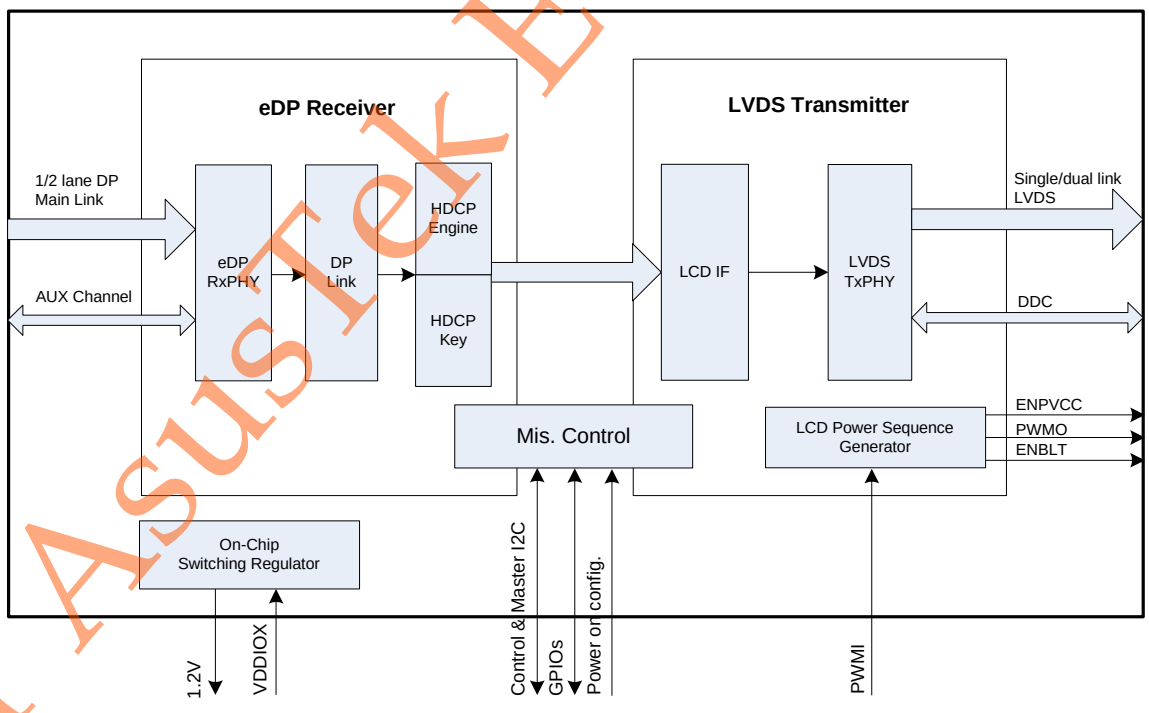


Figure2. PS8625 Functional Block Diagram

EMBEDDED DISPLAYPORT™ RECEIVER

The Embedded DisplayPort™ Receiver interface implemented in the PS8625 is fully compliant to the *VESA DisplayPort Standard, Version 1.1a* and *VESA Embedded DisplayPort Standard, Version 1.2*.

Physical Layer (PHY)

PS8625 DisplayPort™ main link operates at a fixed data rate of 2.7Gbps (High Bit Rate – HBR) or 1.62Gbps (Reduced Bit Rate – RBR). The DisplayPort™ receiver PHY receives video data stream in serial format, de-serializes, decodes, and unscrambles data stream into link symbol stream. It monitors Link Status and Quality. PS8625 DisplayPort™ receiver supports 1-lane or 2-lane configurations. The number of lanes and link rate can be configured according to the bandwidth requirements.

The DisplayPort™ AUX channel is a half-duplex, bi-directional channel which supports bit rate at 1 Mbps. The logical sub-block of AUX channel generates and detects Start/Stop condition and locks to Sync pattern, encodes or decodes of data using Manchester-II coding. The AUX channel provides Link Configuration, Link maintenance. And it's also used as a bridge for DDC/I2C transactions for EDID access.

The Hot Plug Detection (HPD) is also supported in PS8625. In embedded applications, the use of HPD is not mandatory. The low-going pulse HPD signal is also used as Interrupt Request (IRQ) by sink device.

Link Layer

PS8625 Link Layer receives link data and recovers video streams, video clock timing stamps, video timing information and InfoFrame. It also handles AUX Channel link service and device service.

The isochronous transport services of Link Layer provide packing/un-packing, stuffing/un-stuffing, framing/un-framing, inter-lane skewing/de-skewing, stream clock recovery, insertion/extraction of Main Stream Attributes data and/or inserting/extracting of secondary data.

High-bandwidth Digital Content Protection (HDCP) – PS8625HDE only

The High-bandwidth Digital Content Protection (HDCP) provides a secure link layer service between the DisplayPort™ transmitter and receiver. PS8625HDE is compliant with HDCP version 1.3 specification for DisplayPort™ and it integrates the HDCP key ROM.

Customers must have signed HDCP license agreement with Digital Content Protection, LLC, before receiving samples from Parade Technologies for products with HDCP support.

LVDS INTERFACE

PS8625 LVDS interface supports both single link and dual link output with clock rate up to 135MHz. Each LVDS channel has 4 data pairs and 1 clock pair which support 18-bpp and 24-bpp color depth RGB output, VESA or JEIDA data mapping formats. The LVDS interface output mode can be flexibly configured by pins, control I2C or AUX channel.

PS8625 can automatically detect video signal from eDP input. If no valid video signals detected, PS8625 will set LVDS output to tri-state. Once valid video signals detected, the LVDS output will be turned on.

For flexibility, the LVDS interface also provides following options:

- Channel 0/1 swap ***(Dual channel LVDS output only)***
- Channel data order swap
- P/N swap

The mappings of internal video pixel bus to LVDS interface are defined in Table1 to Table6. For 18-bpp LVDS output, the data will be MSB aligned.

Table1. Single link LVDS – JEIDA format 18-bpp, VESA format 18-bpp

BIT	6	5	4	3	2	1	0
TA0	GRN0[2]	RED0[7]	RED0[6]	RED0[5]	RED0[4]	RED0[3]	RED0[2]
TB0	BLU0[3]	BLU0[2]	GRN0[7]	GRN0[6]	GRN0[5]	GRN0[4]	GRN0[3]
TC0	DE	VSYNC	HSYNC	BLU0[7]	BLU0[6]	BLU0[5]	BLU0[4]
TD0							

Table2. Single link LVDS – JEIDA format 24-bpp

BIT	6	5	4	3	2	1	0
TA0	GRN0[2]	RED0[7]	RED0[6]	RED0[5]	RED0[4]	RED0[3]	RED0[2]
TB0	BLU0[3]	BLU0[2]	GRN0[7]	GRN0[6]	GRN0[5]	GRN0[4]	GRN0[3]
TC0	DE	VSYNC	HSYNC	BLU0[7]	BLU0[6]	BLU0[5]	BLU0[4]
TD0	BLU0[1]	BLU0[1]	BLU0[0]	GRN0[1]	GRN0[0]	RED0[1]	RED0[0]

Table3. Single link LVDS – VESA format, 24-bpp

BIT	6	5	4	3	2	1	0
TA0	GRN0[0]	RED0[5]	RED0[4]	RED0[3]	RED0[2]	RED0[1]	RED0[0]
TB0	BLU0[1]	BLU0[0]	GRN0[5]	GRN0[4]	GRN0[3]	GRN0[2]	GRN0[1]
TC0	DE	VSYNC	HSYNC	BLU0[5]	BLU0[4]	BLU0[3]	BLU0[2]
TD0	BLU0[7]	BLU0[7]	BLU0[6]	GRN0[7]	GRN0[6]	RED0[7]	RED0[6]

Table4. Dual link LVDS – JEIDA format 18-bpp, VESA format 18-bpp

BIT	6	5	4	3	2	1	0
TA0	GRN0[2]	RED0[7]	RED0[6]	RED0[5]	RED0[4]	RED0[3]	RED0[2]
TB0	BLU0[3]	BLU0[2]	GRN0[7]	GRN0[6]	GRN0[5]	GRN0[4]	GRN0[3]
TC0	DE	VSYNC	HSYNC	BLU0[7]	BLU0[6]	BLU0[5]	BLU0[4]
TD0							
TA1	GRN1[2]	RED1[7]	RED1[6]	RED1[5]	RED1[4]	RED1[3]	RED1[2]
TB1	BLU1[3]	BLU1[2]	GRN1[7]	GRN1[6]	GRN1[5]	GRN1[4]	GRN1[3]
TC1	DE	VSYNC	HSYNC	BLU1[7]	BLU1[6]	BLU1[5]	BLU1[4]
TD1							

Table5. Dual link LVDS – JEIDA format 24-bpp

BIT	6	5	4	3	2	1	0
TA0	GRN0[2]	RED0[7]	RED0[6]	RED0[5]	RED0[4]	RED0[3]	RED0[2]
TB0	BLU0[3]	BLU0[2]	GRN0[7]	GRN0[6]	GRN0[5]	GRN0[4]	GRN0[3]
TC0	DE	VSYNC	HSYNC	BLU0[7]	BLU0[6]	BLU0[5]	BLU0[4]
TD0	BLU0[1]	BLU0[1]	BLU0[0]	GRN0[1]	GRN0[0]	RED0[1]	RED0[0]
TA1	GRN1[2]	RED1[7]	RED1[6]	RED1[5]	RED1[4]	RED1[3]	RED1[2]
TB1	BLU1[3]	BLU1[2]	GRN1[7]	GRN1[6]	GRN1[5]	GRN1[4]	GRN1[3]
TC1	DE	VSYNC	HSYNC	BLU1[7]	BLU1[6]	BLU1[5]	BLU1[4]
TD1	BLU1[1]	BLU1[1]	BLU1[0]	GRN1[1]	GRN1[0]	RED1[1]	RED1[0]

Table6. Dual link LVDS – VESA format 24-bpp

BIT	6	5	4	3	2	1	0
TA0	GRN0[0]	RED0[5]	RED0[4]	RED0[3]	RED0[2]	RED0[1]	RED0[0]
TB0	BLU0[1]	BLU0[0]	GRN0[5]	GRN0[4]	GRN0[3]	GRN0[2]	GRN0[1]
TC0	DE	VSYNC	HSYNC	BLU0[5]	BLU0[4]	BLU0[3]	BLU0[2]
TD0	BLU0[7]	BLU0[7]	BLU0[6]	GRN0[7]	GRN0[6]	RED0[7]	RED0[6]
TA1	GRN1[0]	RED1[5]	RED1[4]	RED1[3]	RED1[2]	RED1[1]	RED1[0]
TB1	BLU1[1]	BLU1[0]	GRN1[5]	GRN1[4]	GRN1[3]	GRN1[2]	GRN1[1]
TC1	DE	VSYNC	HSYNC	BLU1[5]	BLU1[4]	BLU1[3]	BLU1[2]
TD1	BLU1[7]	BLU1[7]	BLU1[6]	GRN1[7]	GRN1[6]	RED1[7]	RED1[6]

PS8625 provides flexibility for LVDS configuration by GPU through AUX channel. The DPCD register for configure LVDS output as shown following table.

Table7. PS8625 DPCD register definition for LVDS configuration

DPCD Address	Bit	Reset Value[Note1]	Definition
DPCD 40C	1:0	00h	LVDS color depth and data mapping selection 00: 8-bit LVDS, VESA mapping (default) 01: 8-bit LVDS, JEIDA mapping 10: Reserved 11: 6-bit LVDS, VESA and JEIDA mapping
	2		LVDS Link single link or dual link selection 0: Single link LVDS (default) 1: Dual link LVDS
	3		Reserved
	5:4		LVDS SSC Control 00: SSC off (default) 01: +/-0.5% central spreading 10: Reserved 11: +/-1% central spreading
	7:6		Reserved

Note1: The reset value will be updated by external power on configuration pins RLV_CFG and RLV_LNK

SPREAD SPECTRUM CONTROL

PS8625 supports DisplayPort™ standard 0.5% down-spreading Spread Spectrum clocking with the modulation frequency between 30kHz and 33kHz

PS8625 also supports extra central Spread Spectrum clocking on LVDS output. The spreading amplitude is programmable of 0.25%, 0.5%, 0.75%, 1.0%, 1.25%, 1.5%, 1.75% and 2.0%. And the modulation frequency is programmable of 10kHz, 20kHz, 30kHz or 40kHz, with +/-5% error.

If both DisplayPort™ Source Spread Spectrum clocking and LVDS extra central Spread Spectrum clocking are enabled, the maximum Spread Spectrum amplitude is lower than 3% and the maximum Spread Spectrum modulation frequency is lower than 300 kHz.

LCD Panel Power Sequence Control

PS8625 supports LCD panel power sequence control which generates LCD power sequence including LVDS output control, LCD power control (ENPVCC), panel backlight control (ENBLT), and pulse width modulation output for panel backlight adjust (PWMO). The operation principal and timing diagram are illustrated in following figure.

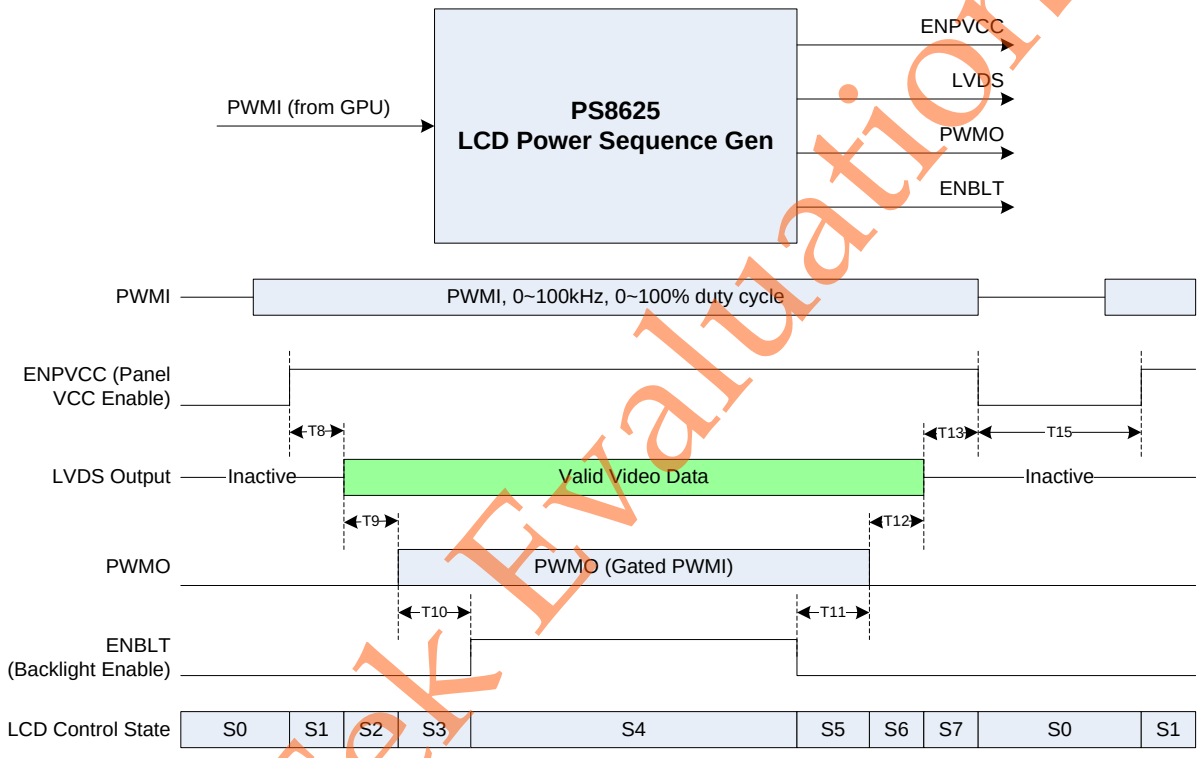


Figure3. PS8625 LCD Panel Power Sequence Control

Notes:

1. ENPVCC is the power control signal to turn on or off LCD power
2. PWMI is the PWM input signal from DP source. It has the range of 0 (DC) to 100kHz frequency, and 0 to 100% duty cycle.
3. PWMO is the gated output of PMWI, with the same PWM frequency and same duty cycle.
4. ENBLT is the panel back light control signal
5. T8, T9, T10, T11, T12, T13, T15 definition refer to *Table11. PS8625 power sequence timing parameters*

PWM Control

PS8625 supports two schemes for panel back light PWM control.

PWM Pass-through

In this mode, PWM signal from PWMI pin will be passed through to the PWMO pin with the gating control in the panel power on sequence logic. PS8625 does not do any modification on the PWM signal frequency or duty cycle.

On-chip PWM Generation

PS8625 also supports on-chip PWM signals generation if there is no PWMI input. The frequency and the duty cycle of the on-chip PWM signal can be programmed through either AUX channel (DPCD) or I2C registers.

The PWM frequency range is programmable from 100Hz to 27KHz and the duty cycle is 8-bit register control from 0 to 255/256.

Table8. PS8625 DPCD register definition for PWM Control

DPCD Address	Bit	Reset Value	Definition
DPCD 720	5	80h	PWM Select 0: Select external PWM (pass through mode) (default) 1: Select internal PWM
DPCD 722	7:0	ffh	PWM Brightness for internal PWM mode, 8-bit resolution 00h = 0% brightness FFh = 100% brightness (default)
DPCD 728	7:0	40h	PWM Frequency for internal PWM mode, 27MHz/(1024 x register value)

DISPLAY RESOLUTIONS

The following tables provide the popular video modes which PS8625 can support. PS8625 can also support other video modes within the available DisplayPort™ bandwidth.

Table9. PS8625 supported video modes for 1-lane main link configuration

Mode	Resolution	Refresh Rate	Blank Mode	Pixel clock Rate	2.7Gbps		1.62Gbps	
					6-bit	8-bit	6-bit	8-bit
VGA	640x480	60Hz	Normal	25.175MHz	Yes	Yes	Yes	Yes
SVGA	800x600	60Hz	Normal	40MHz	Yes	Yes	Yes	Yes
XGA	1024x768	60Hz	Reduced	56MHz	Yes	Yes	Yes	
XGA	1024x768	60Hz	Normal	65MHz	Yes	Yes	Yes	
XGA(portrait)	768x1024	60Hz	Reduced	58.5Mhz	Yes	Yes	Yes	
WXGA	1200x800	60Hz	Reduced	67MHz	Yes	Yes	Yes	
WXGA	1280x768	60Hz	Reduced	68.25MHz	Yes	Yes	Yes	
WXGA	1280x800	60Hz	Reduced	71MHz	Yes	Yes	Yes	
WSXGA	1280x854	60Hz	Reduced	75.75Mhz	Yes	Yes		
WXGA(portrait)	960x1280	60Hz	Reduced	88.5MHz	Yes	Yes		
WXGA	1366x768	60Hz	Normal	85.5MHz	Yes	Yes		
WXGA+	1440x900	60Hz	Reduced	88.75MHz	Yes	Yes		
WXGA+	1440x900	60Hz	Normal	106.5MHz	Yes			
WXGA+	1600x900	60Hz	Reduced	97.75MHz	Yes			
WXGA+	1600x900	60Hz	Normal	118.25MHz				
SXGA	1280x1024	60Hz	Normal	108MHz	Yes			
SXGA+	1400x1050	60Hz	Reduced	101MHz	Yes			
SXGA+	1400x1050	60Hz	Normal	121.75MHz				
WSXGA+	1680x945	60Hz	Reduced	107.25MHz	Yes			
WSXGA+	1680x945	60Hz	Normal	130.75MHz				
WSXGA+	1680x1050	60Hz	Reduced	119MHz	Yes			
WSXGA+	1680x1050	60Hz	Normal	146.25MHz				
UXGA	1600x1200	60Hz	Reduced	130.25MHz				
UXGA	1600x1200	60Hz	Normal	162MHz				
WUXGA	1920x1200	60Hz	Reduced	154MHz				
	1280x720	60Hz	Prog	74.25MHz	Yes	Yes		
	1920x1080	60Hz	Prog	148.5MHz				

Table10. PS8625 supported video modes for 2-lane main link configuration

Mode	Resolution	Refresh Rate	Blank Mode	Pixel clock Rate	2.7Gbps		1.62Gbps	
					6-bit	8-bit	6-bit	8-bit
VGA	640x480	60Hz	Normal	25.175MHz	Yes	Yes	Yes	Yes
SVGA	800x600	60Hz	Normal	40MHz	Yes	Yes	Yes	Yes
XGA	1024x768	60Hz	Reduced	56MHz	Yes	Yes	Yes	Yes
XGA	1024x768	60Hz	Normal	65MHz	Yes	Yes	Yes	Yes
XGA(portrait)	768x1024	60Hz	Reduced	58.5Mhz	Yes	Yes	Yes	Yes
WXGA	1200x800	60Hz	Reduced	67MHz	Yes	Yes	Yes	Yes
WXGA	1280x768	60Hz	Reduced	68.25MHz	Yes	Yes	Yes	Yes
WXGA	1280x800	60Hz	Reduced	71MHz	Yes	Yes	Yes	Yes
WSXGA	1280x854	60Hz	Reduced	75.75Mhz	Yes	Yes	Yes	Yes
WXGA(portrait)	960x1280	60Hz	Reduced	88.5MHz	Yes	Yes	Yes	Yes
WXGA	1366x768	60Hz	Normal	85.5MHz	Yes	Yes	Yes	Yes
WXGA+	1440x900	60Hz	Reduced	88.75MHz	Yes	Yes	Yes	Yes
WXGA+	1440x900	60Hz	Normal	106.5MHz	Yes	Yes	Yes	Yes
WXGA+	1600x900	60Hz	Reduced	97.75MHz	Yes	Yes	Yes	Yes
WXGA+	1600x900	60Hz	Normal	118.25MHz	Yes	Yes	Yes	
SXGA	1280x1024	60Hz	Normal	108MHz	Yes	Yes	Yes	Yes
SXGA+	1400x1050	60Hz	Reduced	101MHz	Yes	Yes	Yes	Yes
SXGA+	1400x1050	60Hz	Normal	121.75MHz	Yes	Yes	Yes	
WSXGA+	1680x945	60Hz	Reduced	107.25MHz	Yes	Yes	Yes	Yes
WSXGA+	1680x945	60Hz	Normal	130.75MHz	Yes	Yes	Yes	
WSXGA+	1680x1050	60Hz	Reduced	119MHz	Yes	Yes	Yes	
WSXGA+	1680x1050	60Hz	Normal	146.25MHz	Yes	Yes		
UXGA	1600x1200	60Hz	Reduced	130.25MHz	Yes	Yes	Yes	
UXGA	1600x1200	60Hz	Normal	162MHz	Yes	Yes		
WUXGA	1920x1200	60Hz	Reduced	154MHz	Yes	Yes		
	1280x720	60Hz	Prog	74.25MHz	Yes	Yes	Yes	Yes
	1920x1080	60Hz	Prog	148.5MHz	Yes	Yes		

HOT PLUG DETECTION

PS8625 HPD is an output signal at eDP receiver side. A high on this signal indicates that PS8625 is ready to take eDP input. PS8625 will assert HPD after it finishes initial code loading. If no initial code loading required, PS8625 will assert HPD after its power up and the de-assertion of the RST#.

Besides hot plug detection, HPD signal also supports HPD IRQ with low-going pulse (0.5ms ~ 1ms) defined by DisplayPort™ spec for following cases

- DisplayPort™ link status changes such as loss of CR, loss of symbol lock, loss of inter lane alignment, or loss of video sync
- AUTOMATED_TEST_REQEST

EDID

PS8625 integrates AUX to I2C bridge which supports EDID relay from DDC bus in LCD panel interface to the AUX CH of eDP receiver interface. When relaying the EDID from LCD panel to eDP source, PS8625 does not do any modification on the EDID data.

CONTROL I2C SLAVE

Control I2C slave is the programming interface for external device to access internal registers, including DPCD registers. This bus is used to configure, control or debug PS8625 internal functions.

In real application, this I2C bus may also be used as the interface for handshaking with external micro-controller.

I2C MASTER

PS8625 also supports an I2C master shared with control I2C slave to support initial code loading from external EEPROM.

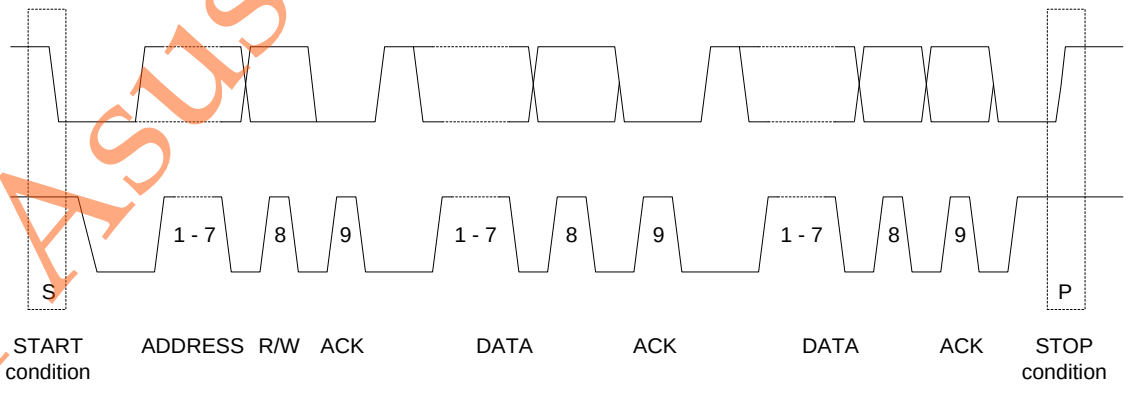
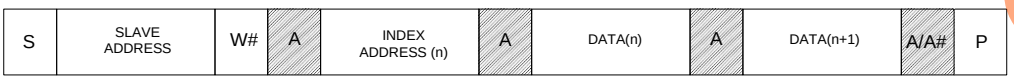


Figure4. I2C Complete Data Transfer

I2C Read Command



I2C Write Command

From Master to Slave

From Slave to Master

S:	START condition
P:	STOP condition
A:	Acknowlegde (SDA Low)
A#:	not acknowledge (SDA High)
W#:	Write command (SDA Low)
R:	Read command (SDA High)
Slave Address:	7 bits
Index Address:	8 bits, index n
Data:	8 bits, reference to index n

Figure5. I2C Read and Write Command

POWER ON HARDWARE CONFIGURATION

PS8625 initial setting like LVDS output mode selection can be configured by power on hardware configuration. Two hardware configuration mechanisms are provided for flexible initial setting.

The first configuration mechanism is through configuration pins as shown following table.

Table11. Power on Pins Configuration

Configuration Signal	Purpose	Definition
I2C_ADDR	I2C Slave address selection	L: 0x10h~0x1Fh H: 0x90h~0x9Fh
RLV_CFG	LVDS color depth and data mapping selection	L: 8-bit LVDS, VESA mapping M: 8-bit LVDS, JEIDA mapping H: 6-bit LVDS, both VESA and JEIDA mapping
RLV_LNK	LVDS single link or dual link selection	L: Single link LVDS H: Dual link LVDS

Another mechanism to achieve configuration is by an external EEPROM through MSCL/MSDA.

POWER-UP AND POWER-DOWN SEQUENCE

PS8625 power-up and power-down sequence meets to the timing spec defined in eDP specification 1.2. Figure6 describes the power up/down sequence for normal operation which includes the display of video from eDP input to LVDS output. Figure7 describes the power up/down sequence when the source executes an AUX channel transaction only.

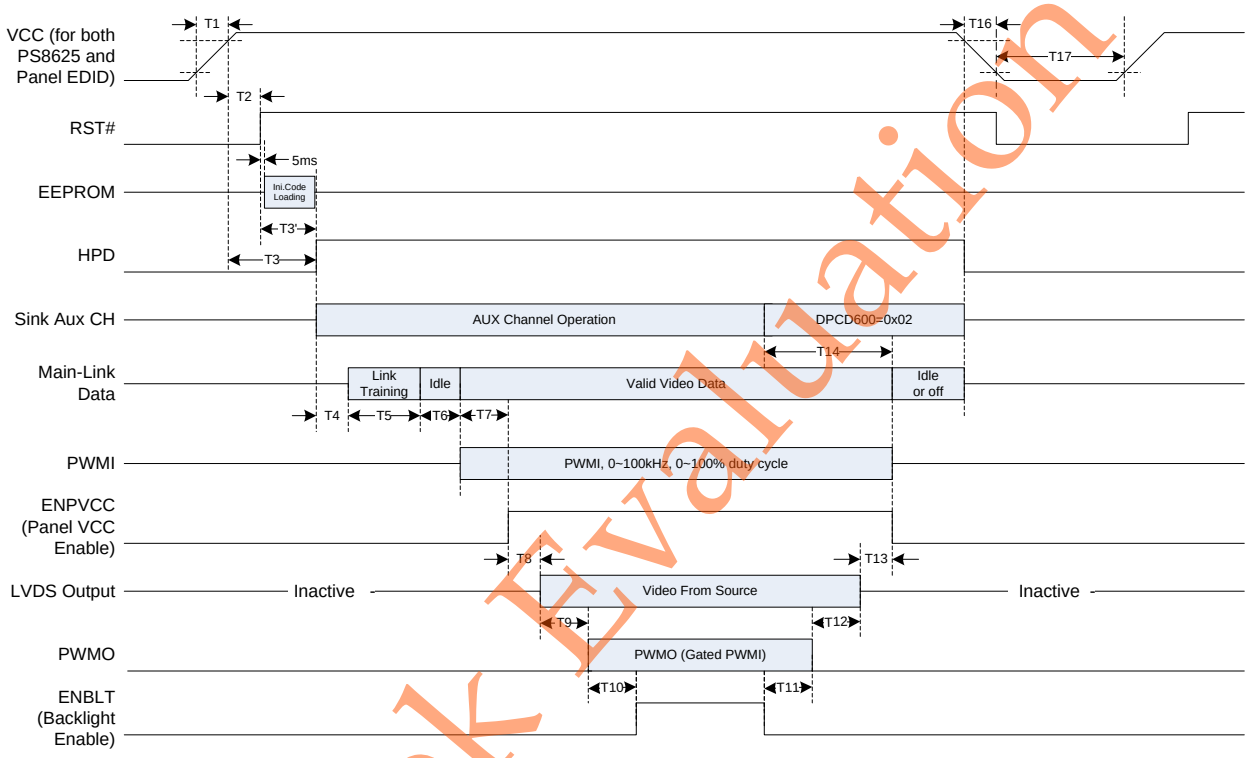


Figure6. PS8625 Power up/down sequence, normal operation

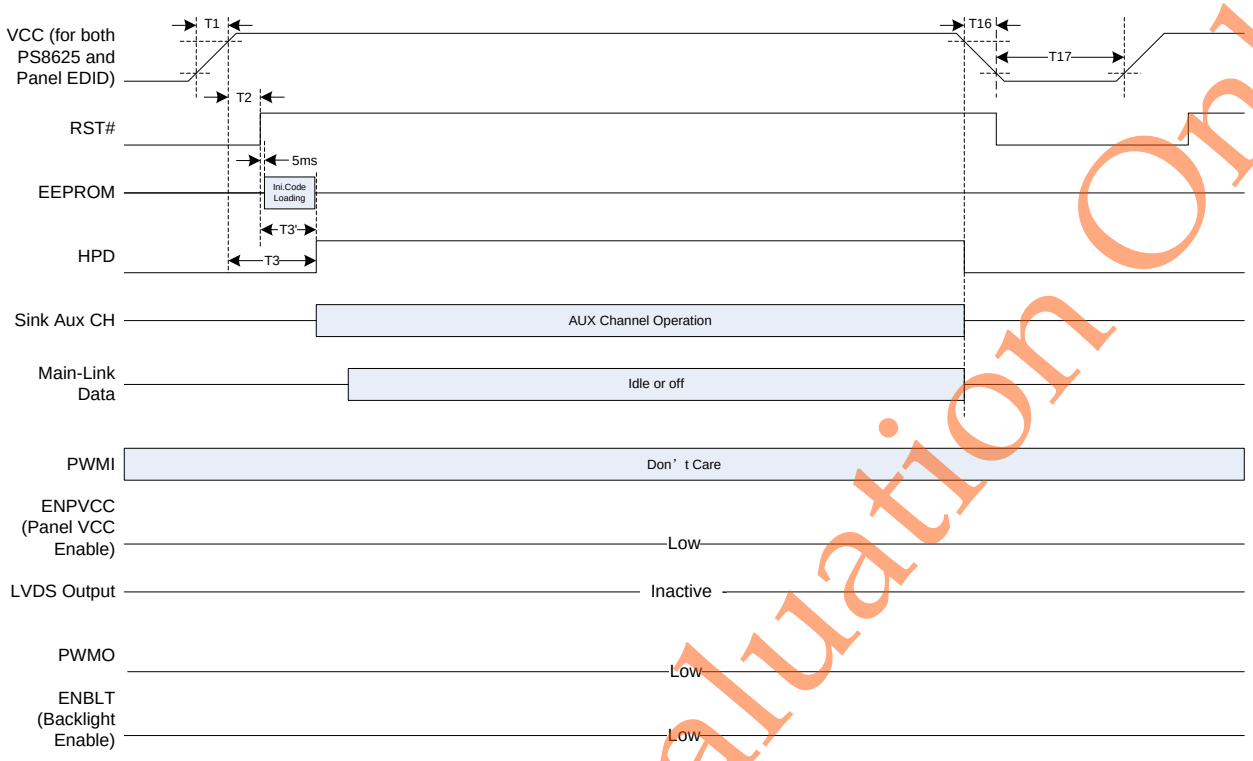


Figure7. PS8625 Power up/down sequence, AUX channel transaction only

Table12. PS8625 power sequence timing parameters

Timing Parameter	Description	Required by	Min	Max	Note
T1	Power rail rise time, 10% to 90%	Source	0.01ms	10ms	
T2	Delay from VCC good to RST# high	Source & PS8625	3ms	30ms	
T3'	Delay from RST# high to HPD high	PS8625	5ms	60ms	
T3	Delay from VCC good to HPD high	Source & PS8625	8ms	200ms	PS8625 AUX channel will be operational upon HPD high.
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from source to ENPVCC high	PS8625	0ms	50ms	PS8625 will output valid video on LVDS within this time

T8	Delay from ENPVCC high to valid LVDS output	PS8625	0ms	50ms	
T9	Delay from LVDS output to PWMO output	PS8625	200ms	-	
T10	Delay from PWMO output to ENBLT high	PS8625	12ms	-	
T11	Delay from ENBLT low to the end of PWMO output	PS8625	0ms	-	
T12	Delay from end of PWMO output to the end of LVDS output	PS8625	200ms	-	
T13	Delay from end of valid LVDS output to ENPVCC low	PS8625	0ms	50ms	
T14	Delay from DPCD 0x600 = 0x02 to end of valid video data	Source	250ms		
T15	ENPVCC low time	PS8625	500ms		
T16	Power rail fall time, 90% to 10%	Source	0.5ms	10ms	
T17	Power off time	Source	500ms	-	

Table13. PS8625 DPCD registers for power sequence timing control

DPCD Address	Bit	Reset Value	Definition
DPCD 40E	1:0	59h	LCD Power sequence T8 control 00: 10ms 01: 20ms (default) 10: 30ms 11: 40ms
	3:2		LCD Power sequence T9 control 00: 100ms 01: 200ms 10: 250ms (default) 11: 300ms
	5:4		LCD Power sequence T10 control 00: 10ms 01: 15ms (default) 10: 20ms 11: 25ms
	7:6		LCD Power sequence T11 control 00: 5ms

			01: 10ms (default) 10: 15ms 11: 20ms
DPCD 40F	1:0	86h	LCD Power sequence T12 control 00: 100ms 01: 200ms 10: 250ms (default) 11: 300ms
	3:2		LCD Power sequence T13 control 00: 10ms 01: 20ms (default) 10: 30ms 11: 40ms
	5:4		LCD Power sequence T15 control 00: 600ms (default) 01: 700ms 10: 800ms 11: 1000ms
	6		Reserved
	7		LCD Power sequence control enable 0: Disable 1: Enable

INTEGRATED ON-CHIP DC/DC SWITCHING REGULATOR

PS8625 integrates an on-chip switching regulator from 3.3V/2.5V to 1.2V core power supply for BOM cost saving. The following application diagram shows the typical application of the switching regulator.

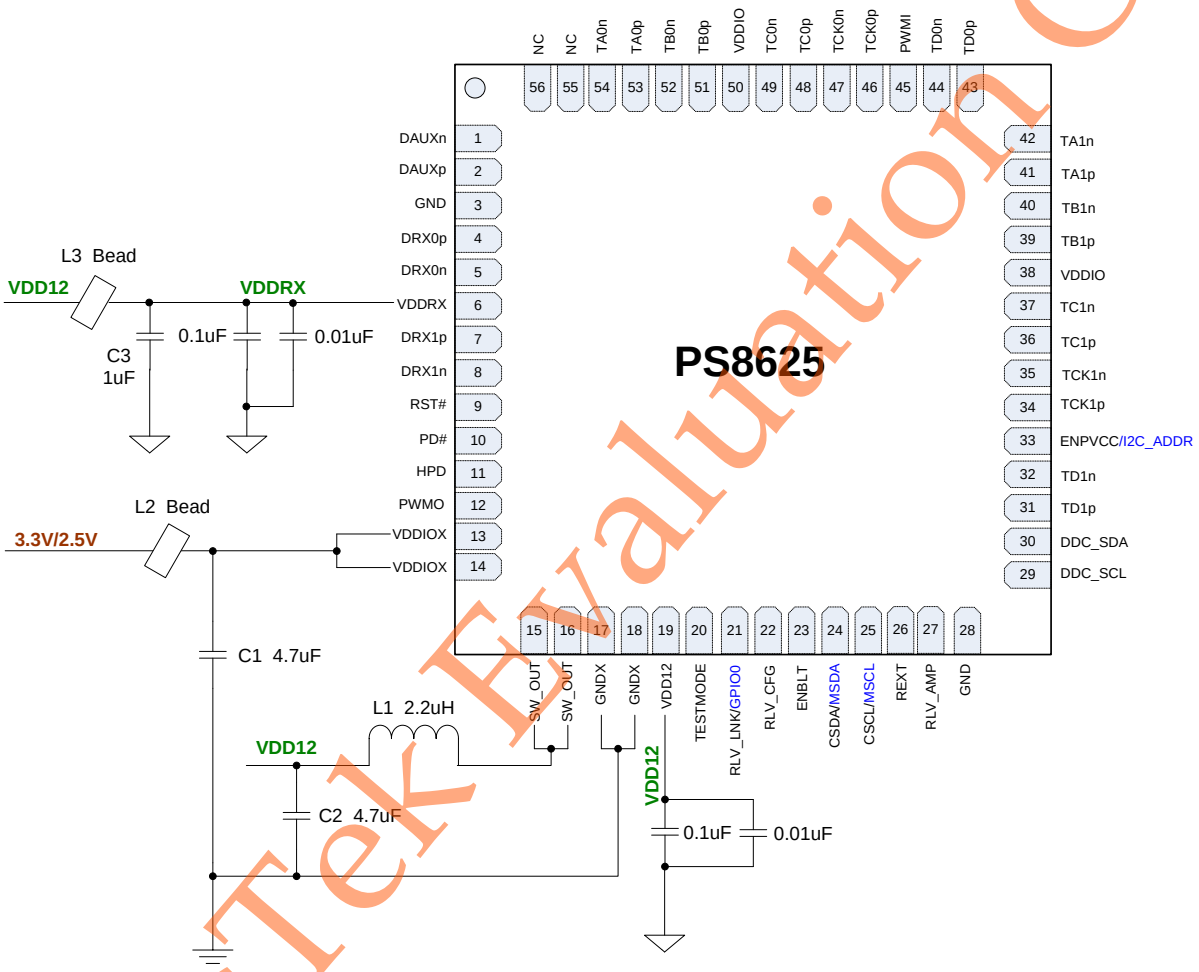


Figure8. PS8625 Switching Regulator Typical Application

Note:

- For buck capacitor (C2), one 4.7uF or 10uF ceramic capacitor is recommended. The ESR of the capacitor should be small.
- For buck inductor (L1), one 2.2uH +/-20% inductor is required.
- One bead (L2) and one 4.7uF (C1) filter capacitor are required on VDDIOX pin to improve the EMI.
- One bead (L3) and one 1uF buck capacitor (C3) are required on VDDRX.

PIN ASSIGNMENT & DESCRIPTION

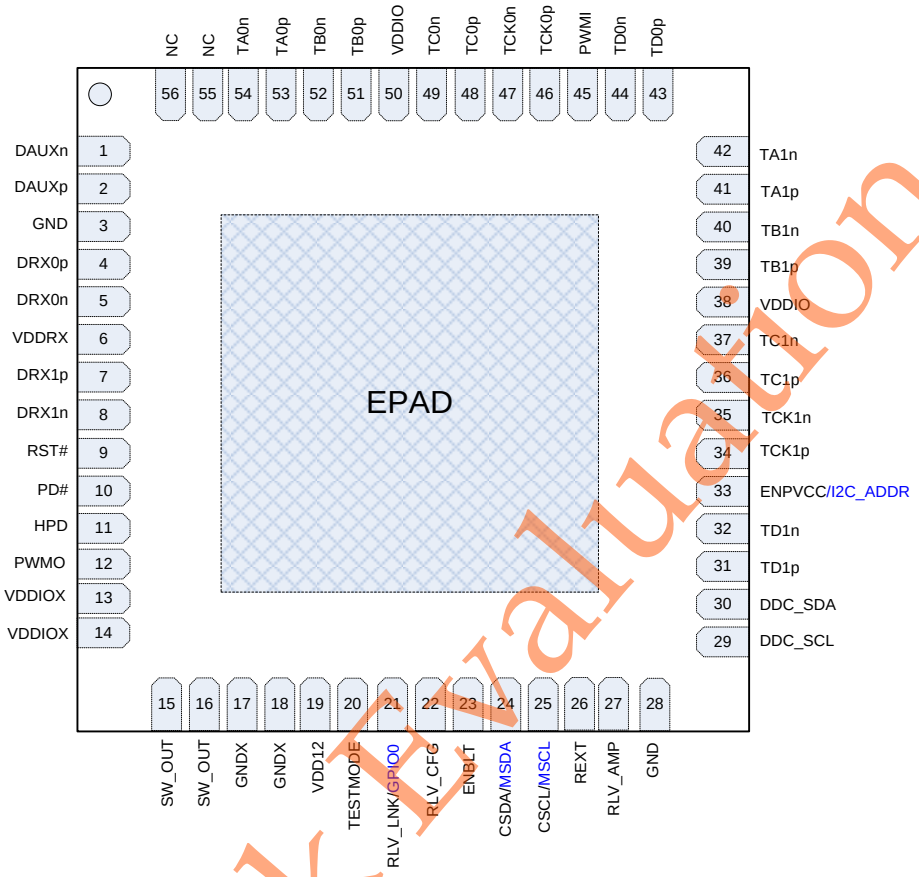


Figure9. PS8625 Pin Assignment

Table14. PS8625 Pin Descriptions

Pin #	Pad Name	I/O Type	I/O Dir	Description
1	DAUXn	Analog	I/O	DP AUX CH differential negative
2	DAUXp	Analog	I/O	DP AUX CH differential positive
3	GND			Ground
4	DRX0p	Analog	I	DP RX lane 0 positive
5	DRX0n	Analog	I	DP RX lane 0 negative
6	VDDRX	Power		DP power supply at 1.2V or 1.35V
7	DRX1p	Analog	I	DP RX lane 1 positive
8	DRX1n	Analog	I	DP RX lane 1 negative
9	RST#	Schmitt	I	Reset, active low, 3.3V or 2.5V input Internal pull-up at ~100kΩ
10	PD#	Schmitt	I	Power down, active low, 3.3V or 2.5V input Internal pull-up at ~100kΩ
11	HPD	LVTTL	O	DP Rx hot plug detection output
12	PWMO	LVTTL	O	Panel backlight PWM output
13	VDDIOX	Power		Switching regulator power supply at 3.3V or 2.5V
14	VDDIOX	Power		Switching regulator power supply at 3.3V or 2.5V
15	SW_OUT	Analog	I/O	Switching regulator output
16	SW_OUT	Analog	I/O	Switching regulator output
17	GNDX			Switching regulator ground
18	GNDX			Switching regulator ground
19	VDD12	Power		Core power supply at 1.2V or 1.35V
20	TESTMODE	Schmitt	I	Test mode control, NC for normal operation
21	RLV_LNK/GPIO0	LVTTL	I I/O	LVDS single link or dual link selection, internal pull-down at ~80kΩ RLV_LNK = L: Single link LVDS H: Dual link LVDS General purpose I/O, internal pull-down at ~80kΩ
22	RLV_CFG	Tri-state	I	LVDS color depth and data mapping selection, internal pull-down at ~80kΩ RLV_CFG = L: 8-bit LVDS, VESA mapping M: 8-bit LVDS, JEIDA mapping H: 6-bit LVDS, both VESA and JEIDA mapping
23	ENBLT	LVTTL	O	Panel backlight enable
24	CSDA/MSDA	Schmitt, OD	I/O	Control I2C slave data Master I2C data
25	CSCL/MSCL	Schmitt, OD	I/O	Control I2C slave clock Master I2C clock
26	REXT	Analog	I/O	Connect to a 4.99kΩ, 1% precision resistor to ground.
27	RLV_AMP	Analog	I	LVDS output swing control

				Connect to a 4.99kΩ resistor to ground for default output swing. The output swing can be adjusted by changing the resistor value.
28	GND			Ground
29	DDC_SCL	Schmitt, OD	I/O	LVDS DDC I2C clock, 5V tolerant
30	DDC_SDA	Schmitt, OD	I/O	LVDS DDC I2C data, 5V tolerant
31	TD1p	Analog	O	LVDS link1 data D output, positive (Even data)
32	TD1n	Analog	O	LVDS link1 data D output, negative (Even data)
33	ENPVCC/I2C_ADDR	LVTTL	I/O I	Panel VCC enable I2C slave address selection, internal pull-down at ~80kΩ I2C_ADDR = L: 0x10h~0x1Fh H: 0x90h~0x9Fh
34	TCK1p	Analog	O	LVDS link1 clock output, positive (Even clock)
35	TCK1n	Analog	O	LVDS link1 clock output, negative (Even clock)
36	TC1p	Analog	O	LVDS link1 data C output, positive (Even data)
37	TC1n	Analog	O	LVDS link1 data C output, negative (Even data)
38	VDDIO	Power		I/O power supply at 3.3V or 2.5V
39	TB1p	Analog	O	LVDS link1 data B output, positive (Even data)
40	TB1n	Analog	O	LVDS link1 data B output, negative (Even data)
41	TA1p	Analog	O	LVDS link1 data A output, positive (Even data)
42	TA1n	Analog	O	LVDS link1 data A output, negative (Even data)
43	TD0p	Analog	O	LVDS link0 data D output, positive (Odd data)
44	TD0n	Analog	O	LVDS link0 data D output, negative (Odd data)
45	PWMI	LVTTL	I	Panel backlight PWM input 0~100KHz and 0~100% duty cycle
46	TCK0p	Analog	O	LVDS link0 clock output, positive (Odd clock)
47	TCK0n	Analog	O	LVDS link0 clock output, negative (Odd clock)
48	TC0p	Analog	O	LVDS link0 data C output, positive (Odd data)
49	TC0n	Analog	O	LVDS link0 data C output, negative (Odd data)
50	VDDIO	Power		I/O power supply at 3.3V or 2.5V
51	TB0p	Analog	O	LVDS link0 data B output, positive (Odd data)
52	TB0n	Analog	O	LVDS link0 data B output, negative (Odd data)
53	TA0p	Analog	O	LVDS link0 data A output, positive (Odd data)
54	TA0n	Analog	O	LVDS link0 data A output, negative (Odd data)
55	NC			Reserved
56	NC			Reserved
	EPAD			Connects to Ground plane through thermal via

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Min	Typ	Max	Unit
Supply Voltage Range:					
VDDIO, VDDIOX		-0.5		4	V
VDD12, VDDRX		-0.5		1.65	V
Normal I/O Voltage Range		-0.5		4	V
5V Safe I/O Voltage Range	DDC_SCL, DDC_SDA	-0.5		6	V
T_J	Junction temperature			125	°C
T_S	Storage temperature	-40		150	°C
ESD	Human Body Model				
	- contact pins		+/- 8000		V
	- all other pins		+/- 4000		V
	Machine Model		+/- 200		V
	Charged Device Model		+/- 2000		V

ESD Standard:

Human Body Mode: JESD22-A114-D
Machine Mode: JESD22-A115-A
Charged Device Mode: JESD22-C101-A
Latch-up Standard: JESD78; I-Test: +/- 100 mA; V-Test: 1.5X of Vcc

NORMAL OPERATING CONDITIONS AND POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit
Supply Voltage:				
VDDIO, VDDIOX (3.3V supply)	3.0	3.3	3.6	V
VDDIO, VDDIOX (2.5V supply)	2.4	2.5	2.6	V
VDD12, VDDRX (when on-chip regulator is not used)	1.14	1.2	1.42	V
Operation Temperature:				
Ta - Ambient Temperature	-20		70	°C
Tc - Case Temperature			85	°C
With on-chip switching regulator				
Supply Current				
I_{DD33} – Single 3.3V supply				
1 lane eDP input and single link LVDS 1440x900 (6-bit)		68		mA
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		119		mA
I_{DD25} – Single 2.5V supply				
1 lane eDP input and single link LVDS 1440x900 (6-bit)		77		mA
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		131		mA
Power Consumption				
3.3V single supply				
1 lane eDP input and single link LVDS, 1440x900 (6-bit)		224		mW
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		393		mW
2.5V single supply				
1 lane eDP input and single link LVDS, 1440x900 (6-bit)		193		mW
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		328		mW
Standby Power Consumption AUX channel is active for Link handshaking communication Cable connected, DPCD 600h=02h			50	mW
Power Down Power Consumption Pin PD# is asserted			1	mW
Without on-chip switching regulator				
Supply Current				
I_{DD33} – 3.3V supply				
1 lane eDP input and single link LVDS 1440x900 (6-bit)		30		mA
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		56		mA

I_{DD12} – 1.2V supply				
1 lane eDP input and single link LVDS 1440x900 (6-bit)		114		mA
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		154		mA
I_{DD135} – 1.35V supply				
1 lane eDP input and single link LVDS 1440x900 (6-bit)		130		mA
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		178		mA
Power Consumption				
3.3V + 1.2V supply				
1 lane eDP input and single link LVDS, 1440x900 (6-bit)		236		mW
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		370		mW
3.3V + 1.35V supply				
1 lane eDP input and single link LVDS, 1440x900 (6-bit)		275		mW
2 lane eDP input and dual link LVDS, 1920x1080 (8-bit)		425		mW
Standby Power Consumption				
3.3V + 1.2V supply			38	mW
3.3V + 1.35V supply			41	mW
AUX channel is active for Link handshaking communication				
Cable connected, DPCD 600h=02h				
Power Down Power Consumption				
3.3V + 1.2V supply			2.3	mW
3.3V + 1.35V supply			3	mW
Pin PD# is asserted				

PACKAGE DISSIPATION RATINGS

56-pin QFN	Still air, 4-layer PCB
θ_{JA} - Junction to Ambient Thermal Resistance	38 °C/W
θ_{JC} - Junction to Case Thermal Resistance	14.5 °C/W
Maximum Power Dissipation Rating, Ta = 70 °C	1447 mW

I/O DC CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
I2C pins:					
CSCL/MSCL, CSDA/MSDA					
V_{OH} High-level output voltage	External 1.5 kΩ pull-up to		VDDIO		V
V_{OL} Low-level output voltage	VDD33, I_{OL} = 8 mA			0.4	V
Control input pins:					
RST#, PD#, RLV_LNK, PWMI, I2C_ADDR					
V_{IH} Input High-level voltage		0.7VDDIO			V
V_{IL} Input Low-level voltage				0.3VDDIO	V
Control output pins:					
ENPVCC, ENBLT, PWMO					
V_{OH} High-level output voltage		0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V
Tri-state control input pins:					
RLV_CFG					
V_{IH} Input High-level voltage		0.7VDDIO			V
V_{IM} Input Mid-level voltage		VDDIO/2-0.3		VDDIO/2+0.3	V
V_{IL} Input Low-level voltage				0.3VDDIO	V
Status I/O pins:					
GPIO0, HPD					
V_{OH} High-level output voltage		0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V

I/O AC CHARACTERISTICS

Parameter	Test Conditions	Min	Typ[4]	Max	Unit
Supply ramp up time:					
t_{VDDIO} VDDIO supply ramp up time	10% to 90% of the supply voltage			+10	ms
t_{VDDIOX} VDDIOX supply ramp up time	10% to 90% of the supply voltage			+10	ms
dt VDDIO and VDDIOX power ramp up separation	Time difference between the mid points of VDDIO and VDDIOX	-10		+10	ms
CMOS output pins: GPIOx	CL = 10 pF				
tr Output rise time				6	ns
tf Output fall time				6	ns
Hot plug detection pin: HPD IRQ HPD pulse width (driven by sink device)		0.5		1.0	ms

POWER UP AND RESET TIMING SEQUENCE

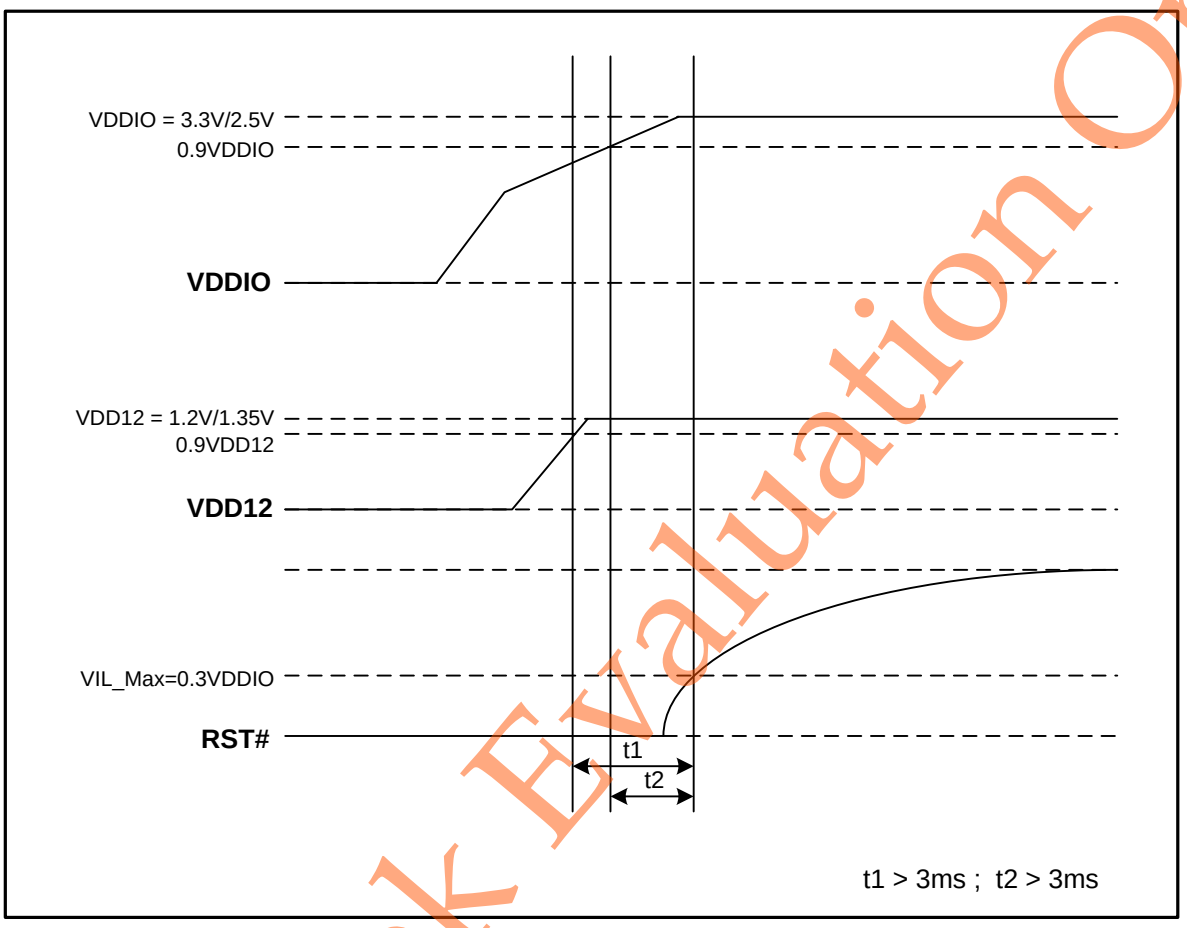


Figure10. Power Up and Reset Timing Sequence

Note: The de-assertion of the RST# shall follow the timing sequence as given in the above diagram when VDD12 is from system power instead of on-chip switching regulator.

DISPLAYPORT™ AUX CHANNEL CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
UI: Unit Interval for AUX channel		0.4	0.5	0.6	µs
$V_{AUX-DIFF-p-p}$: AUX differential peak-to-peak voltage at TP1 When AUX CH is driving the bus		400		1000	mV
$V_{AUX-DIFF-p-p}$: AUX differential peak-to-peak voltage at TP2 When AUX CH is receiving the bus		200		1360	mV
$V_{AUX-DC-CM-RX}$: AUX common mode voltage when receiving			GND		V
$V_{AUX-DC-CM-TX}$: AUX common mode voltage when transmitting			0.20		V
$I_{AUX-SHORT}$: AUX channel short circuit current				20	mA
C_{AUX}: AUX AC coupling capacitor		75		200	nF

DISPLAYPORT™ MAIN LINK RECEIVER CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
Spread spectrum clock, down-spreading by SOURCE			0.5		%
Modulation frequency		30		33	kHz
$V_{RX-DIFFp-p}$: Differential peak-to-peak input voltage at package pins		100		1360	mV
Maximum adaptive RX equalization level at 2.7Gbps			16		dB
$V_{RX\_DC\_CM}$: RX input DC common mode voltage			GND		V
$R_{RX-DIFF}$: Differential termination resistance		80	100	120	Ω
R_{RX-SE}: Single-ended termination resistance		40	50	60	Ω
I_{RX_SHORT}: Rx short circuit current limit				20	mA
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (HBR)				150	ps
RX intra-pair skew tolerance at HBR					
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (RBR)				300	ps
RX intra-pair skew tolerance at RBR					
Receiver Jitter Tolerance for High Bit Rate (HBR)					
Total jitter tolerance at 2MHz		1227			mUI
Total jitter tolerance at 10MHz		548			mUI
Total jitter tolerance at 20MHz		505			mUI
Total jitter tolerance at 100MHz		491			mUI
Receiver Jitter Tolerance for Reduced Bit Rate (RBR)					
Total jitter tolerance at 2MHz		1648			mUI
Total jitter tolerance at 10MHz		778			mUI
Total jitter tolerance at 20MHz		747			mUI
Note: Jitter Tolerance Testing follows *VESA DisplayPort™ PHY Compliance Testing Standard, Version 1.1a.*					

LVDS TRANSMITTER CHARACTERISTICS

Symbol and Parameter		Test Conditions	Min	Typ	Max	Unit
LVDS clock central spread spectrum						
Modulation frequency			10		40	kHz
Central spreading amplitude (programmable)			-1.0		1.0	%
DC Characteristics						
V_{OD}	Peak-to-peak differential output swing	RL = 100 Ω		250		mV
V_{OD}	Programmable low amplitude		175			mV
V_{OD}	Programmable high amplitude				500	mV
ΔV_{OD}	Steady state change in V_{OD}				20	mV
V_{OC}	Common mode voltage		1.125		1.375	V
ΔV_{OC}	Steady state change in V_{OC}				20	mV
I_{OS}	Output short circuit current				24	mA
I_{OZ}	Output tri-state current				10	uA
AC Characteristics						
t_r	LVDS differential rise time	RL = 100 Ω	0.20		1.0	ns
t_f	LVDS differential fall time		0.20		1.0	ns

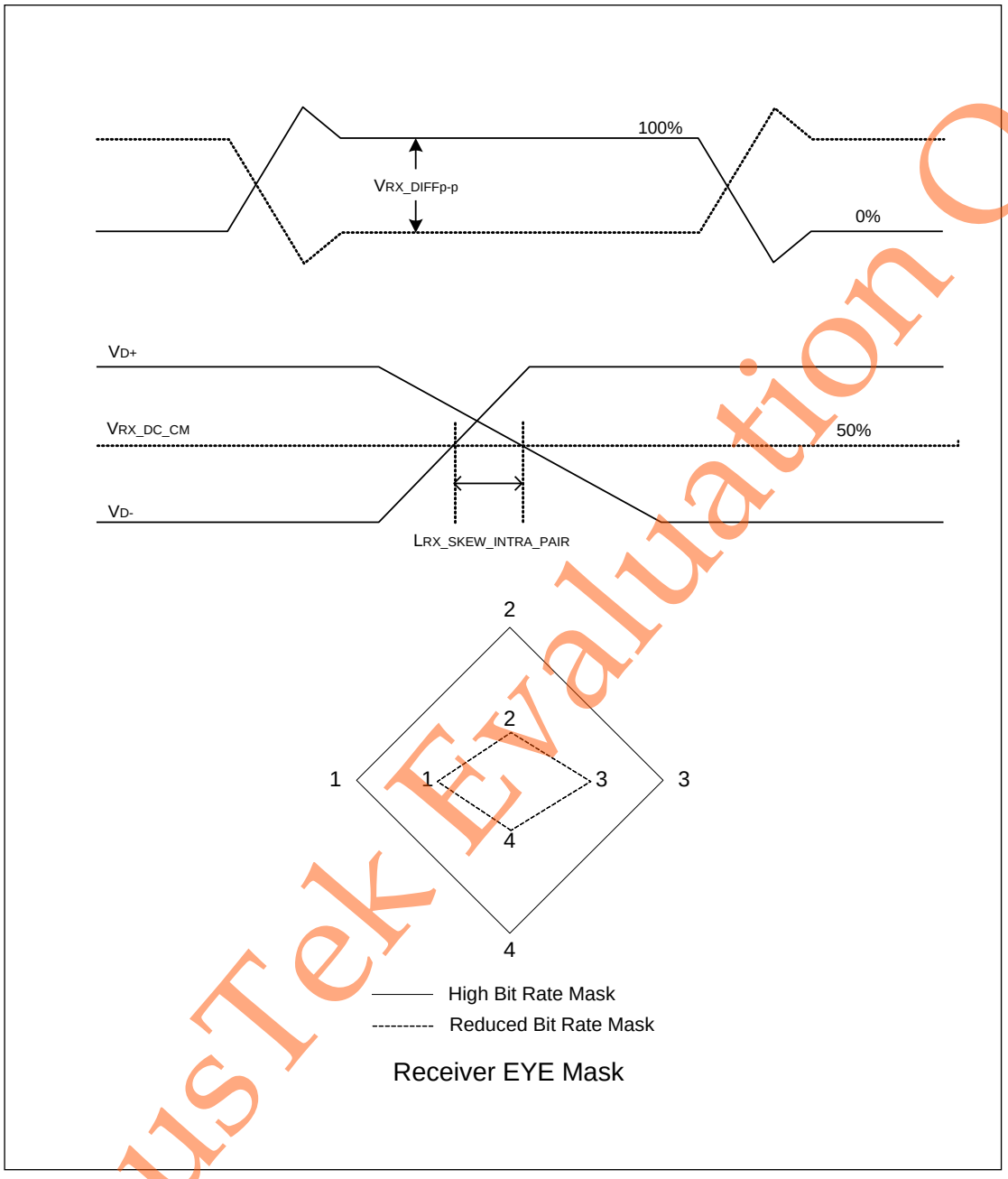


Figure11. Definition of Key Parameters

MEASUREMENT INFORMATION

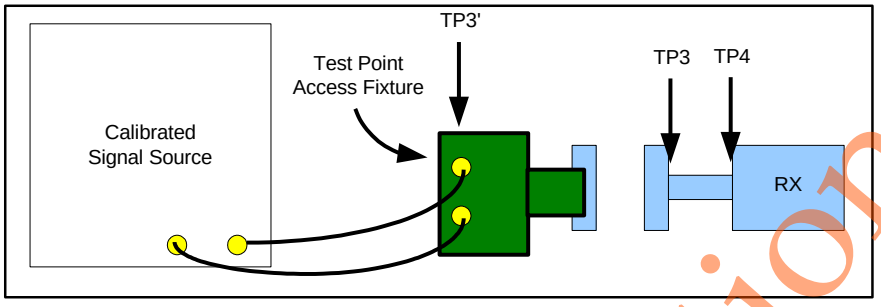


Figure12. Measurement Setup for DisplayPort Sink Device

LAYOUT GUIDELINES

High Speed Interfaces

- Select proper PCB stack up and trace width for 100 ohm differential transmission line impedance for high speed eDP main link and LVDS signals
- Avoid tight bend for differential signals
- Match intra-pair and inter-pair traces length within each differential pair
- Keep uninterrupted ground plane beneath differential signals
- Keep wide and shortest traces for both power and ground path to DP receiver

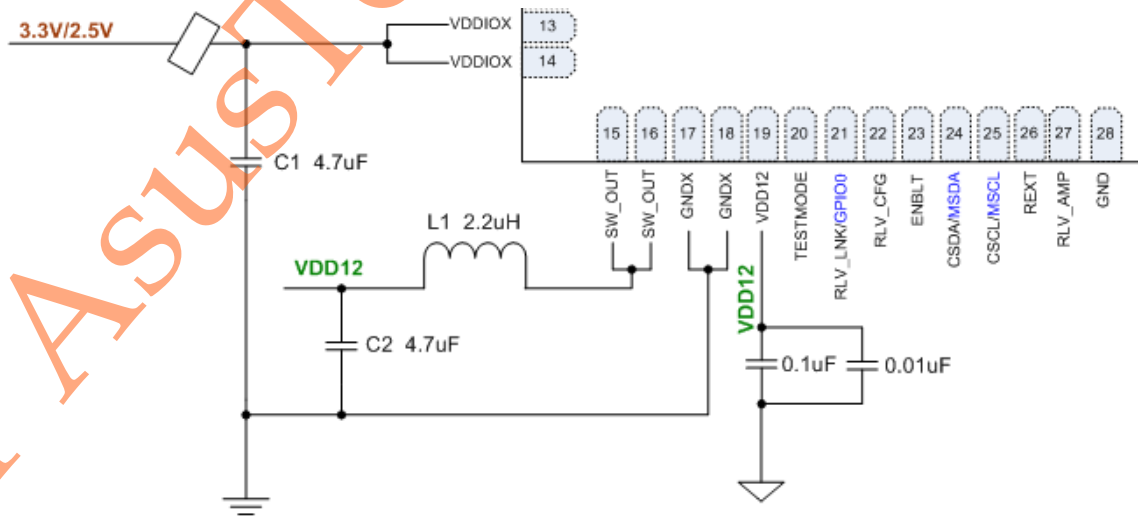
Buck Capacitors and Inductors

- Place a 1uF buck ceramic capacitor on VDDIO rails after the bead
- Place a serial 2.2uH buck inductor and a 4.7uF or 10uF buck ceramic capacitor on switching regulator output

Filtering Capacitors

- Place 0.1uF capacitors on all VDDIO, VDD12 and VDDRX power pins. The capacitors shall be placed as close as possible to the chip package pins
- Place additional 0.01uF capacitor on the VDDRX and VDD12 pins. These capacitor shall be placed as close as possible to the chip package pins
- Place a serial bead and a 4.7uF capacitor to GND on VDDIOX pins. The capacitor shall be placed as close as possible to the chip package pins.

On-chip Switching Regulator



- One bead (L2) and one 4.7uF (C1) input bypass capacitor are required on VDDIOX pin to improve the EMI. They should be placed as close as possible to the VDDIOX pins (Pin13/Pin14).
- For the output capacitor (C2), one 4.7uF or 10uF ceramic capacitor is recommended. The ESR of the capacitor should be small. For inductor (L1), one 2.2uH +/-20% inductor is required. L1 should be placed as close as possible to SW_OUT pins (Pin15/Pin16).
- The ground terminals of C1 and C2 should be placed as close as possible. Connect them to the ground plane with multiple vias. Use a thick trace/plane to connect the capacitor ground terminals to their respective power ground pin GNDX (Pin17/Pin18). Use as wide of a trace as possible when connecting to GNDX.
- Minimize the electrical length and loop area of the current paths described below. Minimizing the electrical length of these paths reduces parasitic resistance; minimizing loop area reduces radiated noise.
  - From the positive terminal of the input capacitor C1 into VDDIOX → out of SW_OUT → through the inductor L1 → through the output capacitors C2 → back to the input capacitor ground terminal.
  - From SW_OUT → through the inductor L1 → through the output capacitors C2 → to the power ground pin (GNDX)
- Route each sense line away from noise sources such as the inductor at the SW_OUT node

ORDER & PACKAGING INFORMATION – PS8625 (without HDCP key, Au wire)

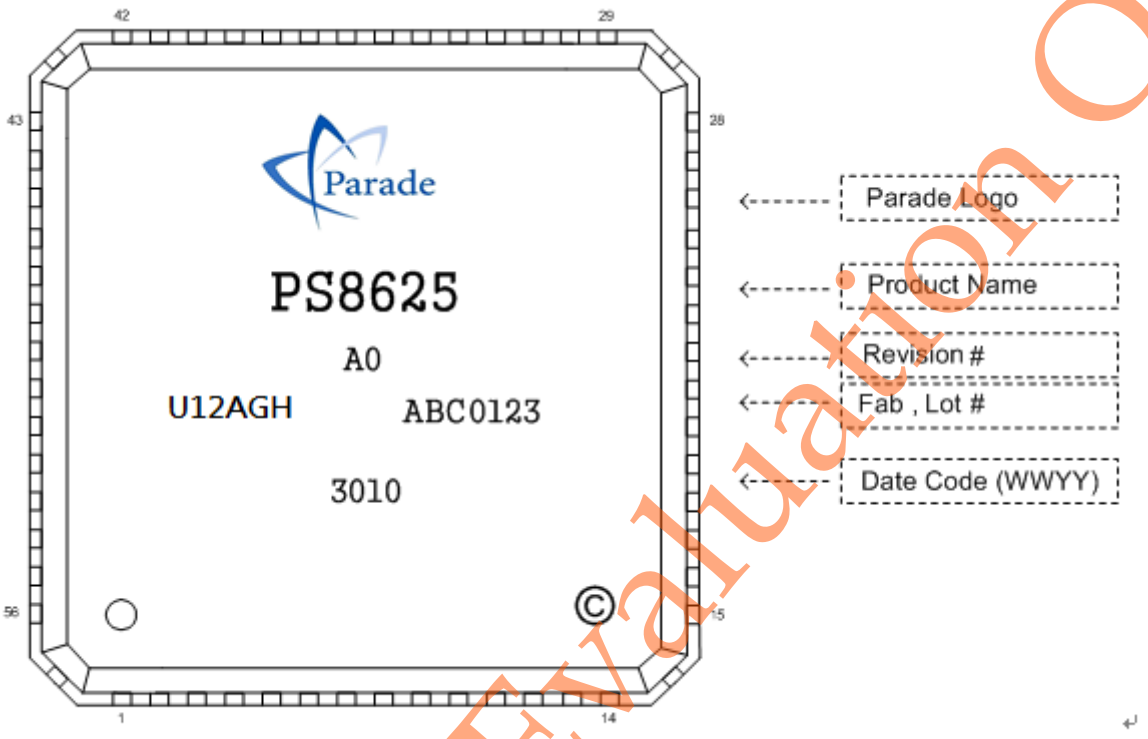
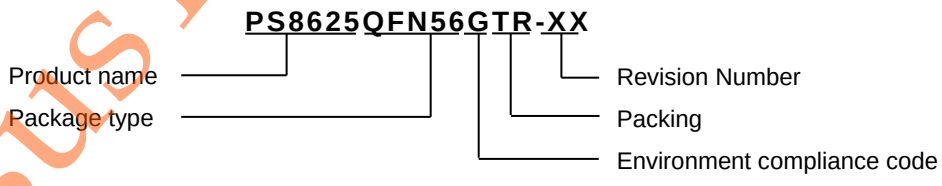


Figure14. Top Side Marking

Order Information

Part number:



Part Number		Packing
PS8625QFN56G-XX	(without HDCP key)	Tray
PS8625QFN56GTR-XX	(without HDCP key)	Tape and Reel

Lead Finish: 100% Sn

ORDER & PACKAGING INFORMATION – PS8625HDE (with HDCP key, Au wire)

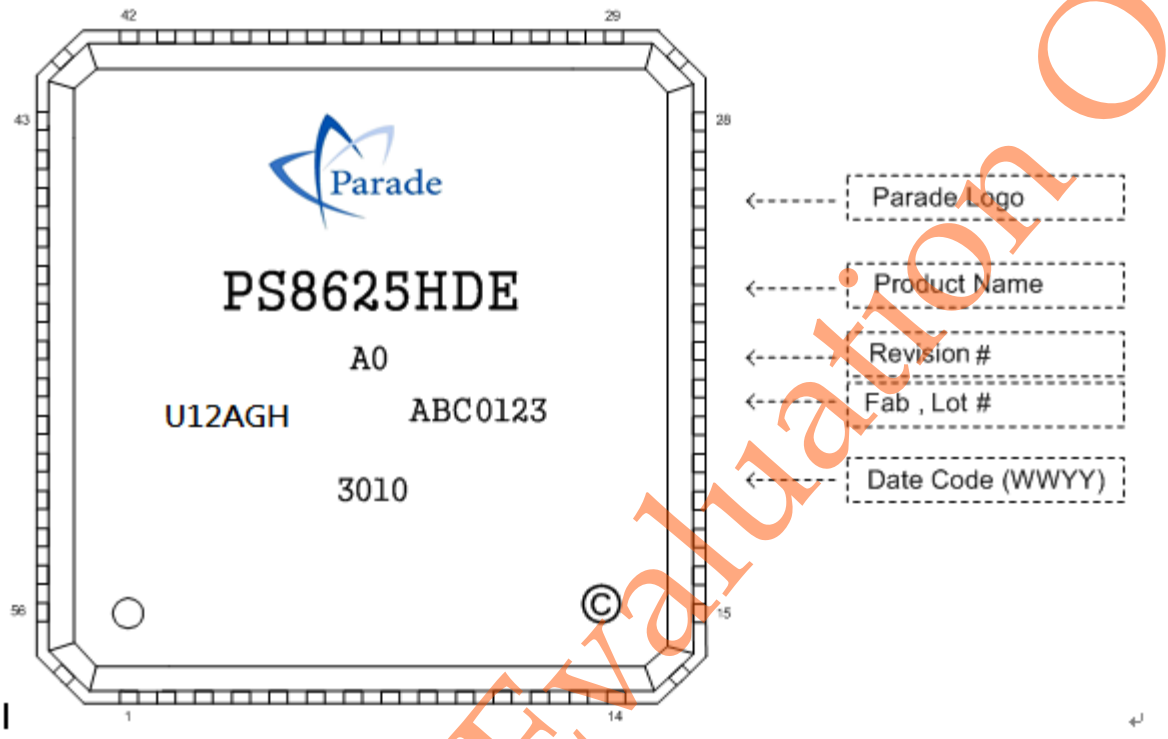
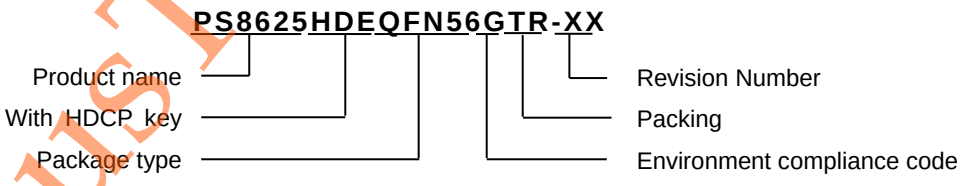


Figure15. Top Side Marking

Order Information

Part number:



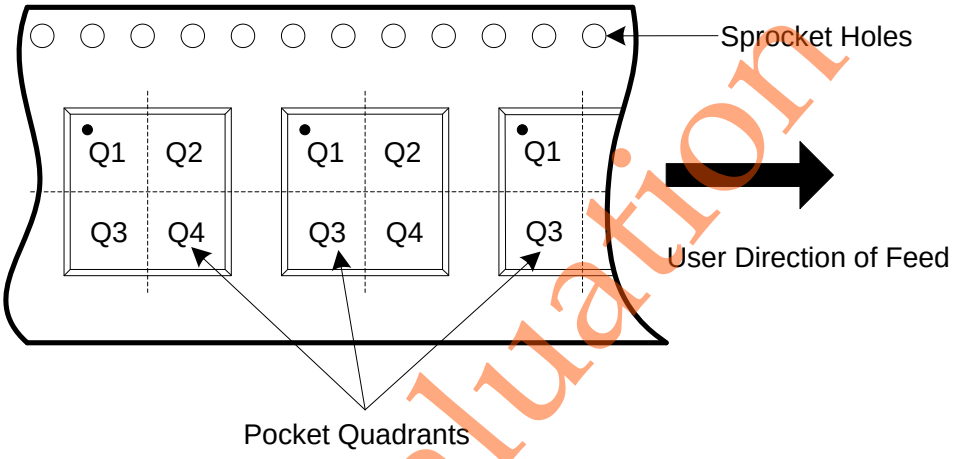
Part Number		Packing
PS8625HDEQFN56G-XX	(with HDCP key)	Tray
PS8625HDEQFN56GTR-XX	(with HDCP key)	Tape and Reel

Lead Finish: 100% Sn

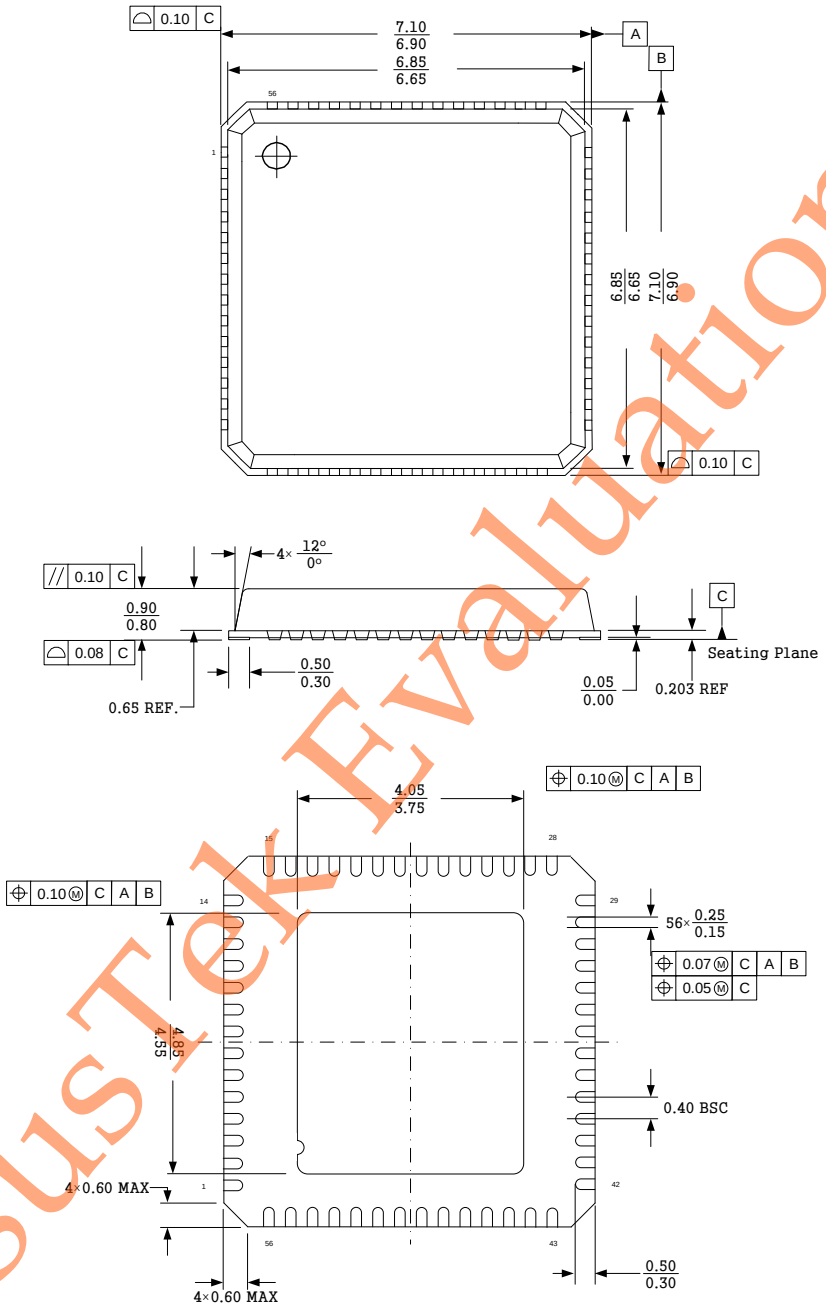
TAPE AND REEL PACKING PIN1 ORIENTATION

QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE

TR
(EIA conforming)



PHYSICAL DIMENSIONS



NOTES:

1. All dimensions are in mm. Angels in degrees.
2. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
3. Refer JEDEC M0-220 modified.

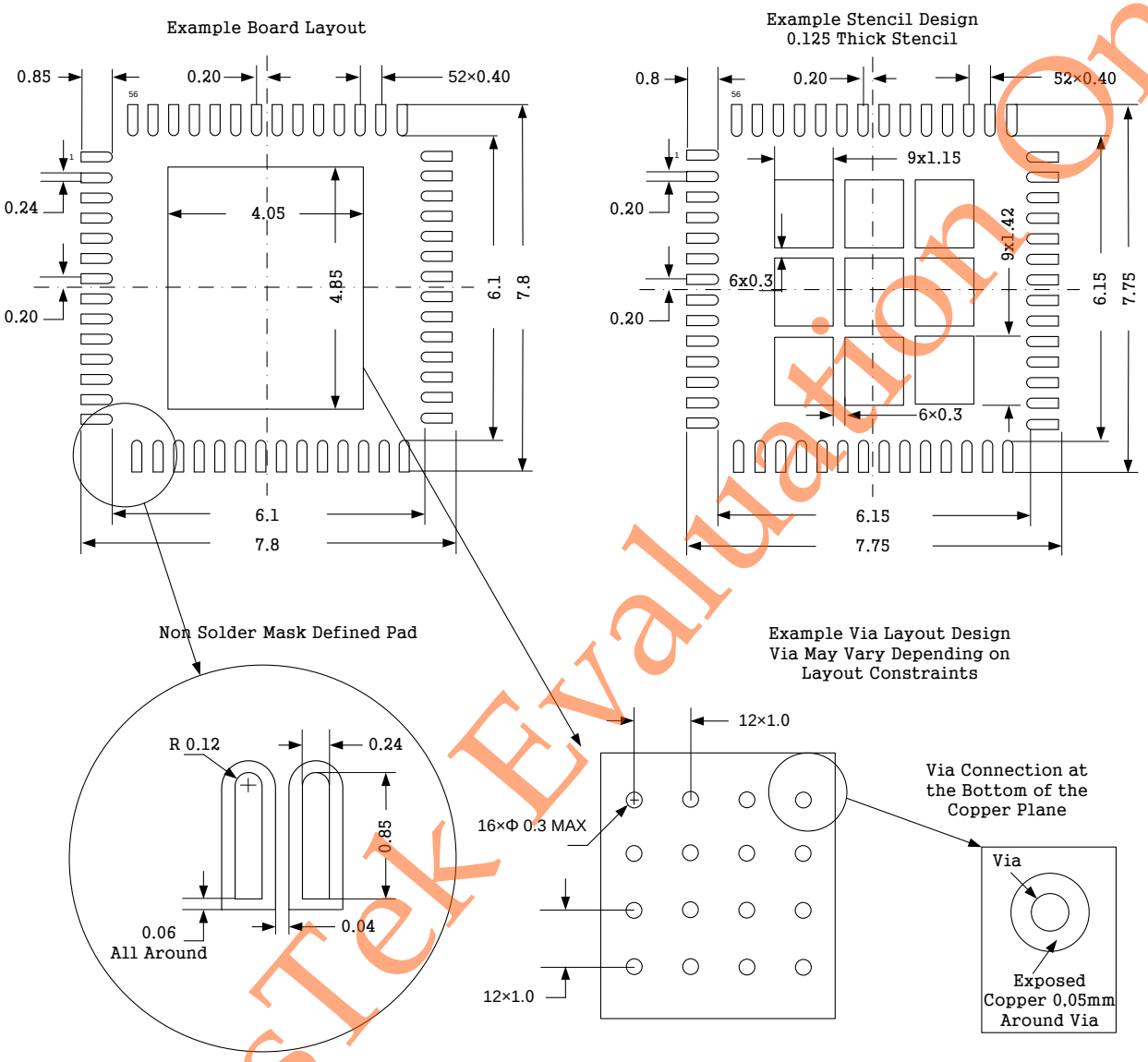


Figure13. The Exposed Thermal Pad Layout Guidelines

NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommend solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

ORDER & PACKAGING INFORMATION – PS8625 (without HDCP key, Cu wire)

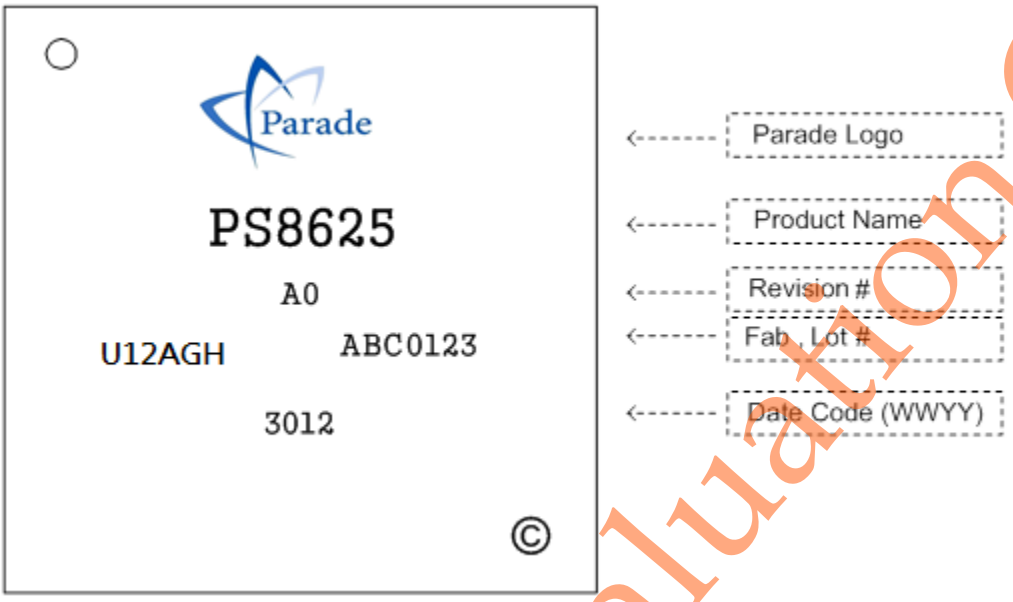
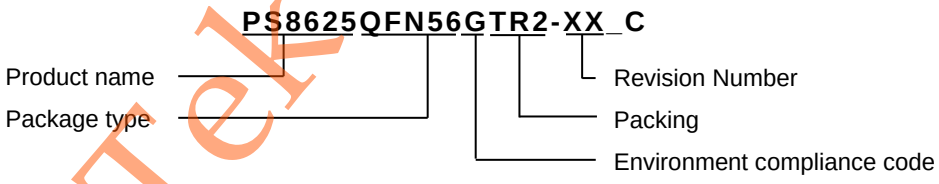


Figure14. Top Side Marking

Order Information

Part number:



Part Number		Packing
PS8625QFN56G-XX_C	(without HDCP key)	Tray
PS8625QFN56GTR2-XX_C	(without HDCP key)	Tape and Reel (EIA conforming)

Lead Finish: 100% Sn

ORDER & PACKAGING INFORMATION – PS8625HDE (with HDCP key, Cu wire)

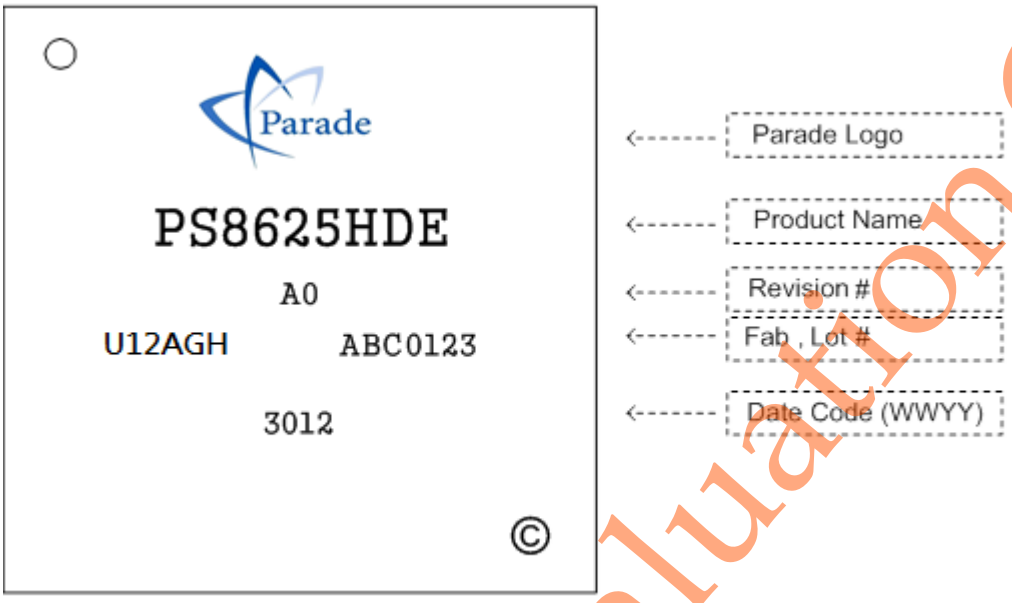
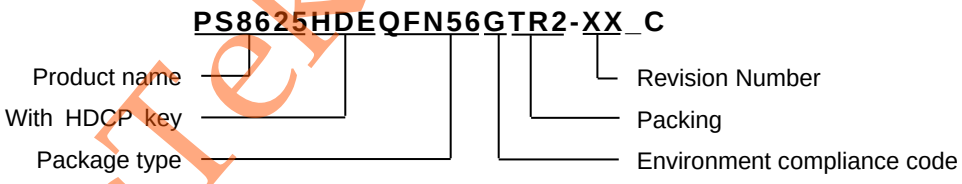


Figure15. Top Side Marking

Order Information

Part number:



Part Number		Packing
PS8625HDEQFN56G-XX_C	(with HDCP key)	Tray
PS8625HDEQFN56GTR2-XX_C	(with HDCP key)	Tape and Reel (EIA conforming)

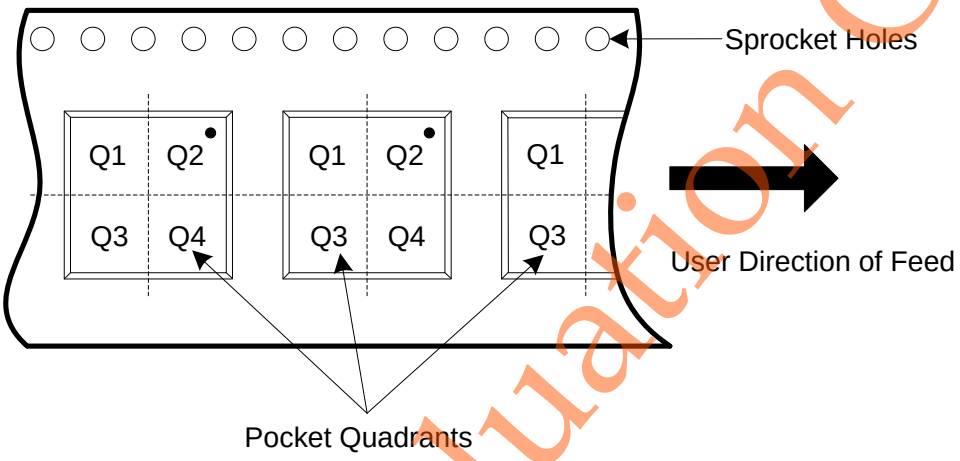
Lead Finish: 100% Sn

TAPE AND REEL PACKING PIN1 ORIENTATION

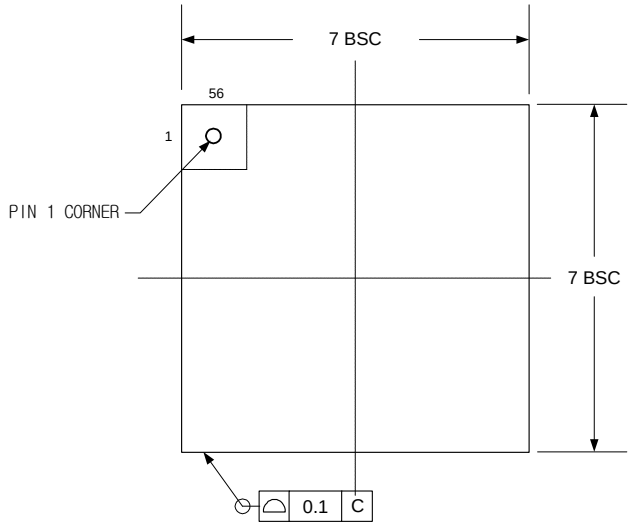
QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE

TR2

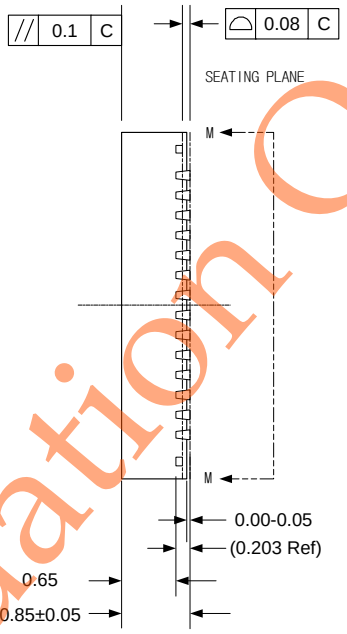
(EIA conforming)



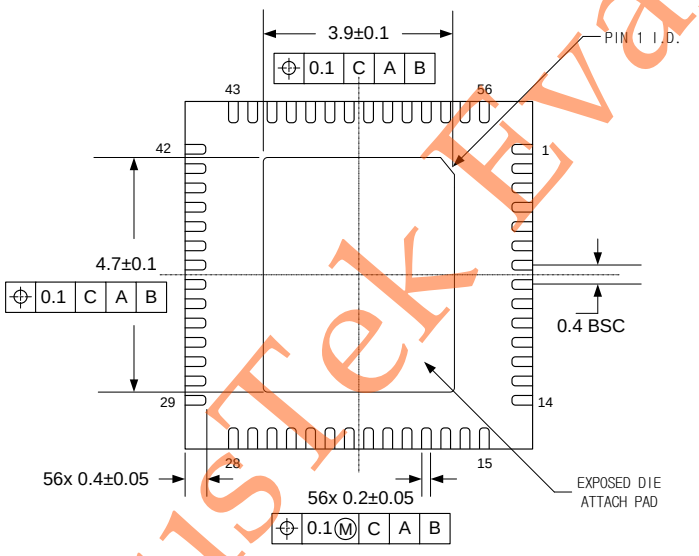
PHYSICAL DIMENSIONS



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:

1. All dimensions are in mm. Angels in degrees.
2. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
3. Refer JEDEC M0-220 modified.

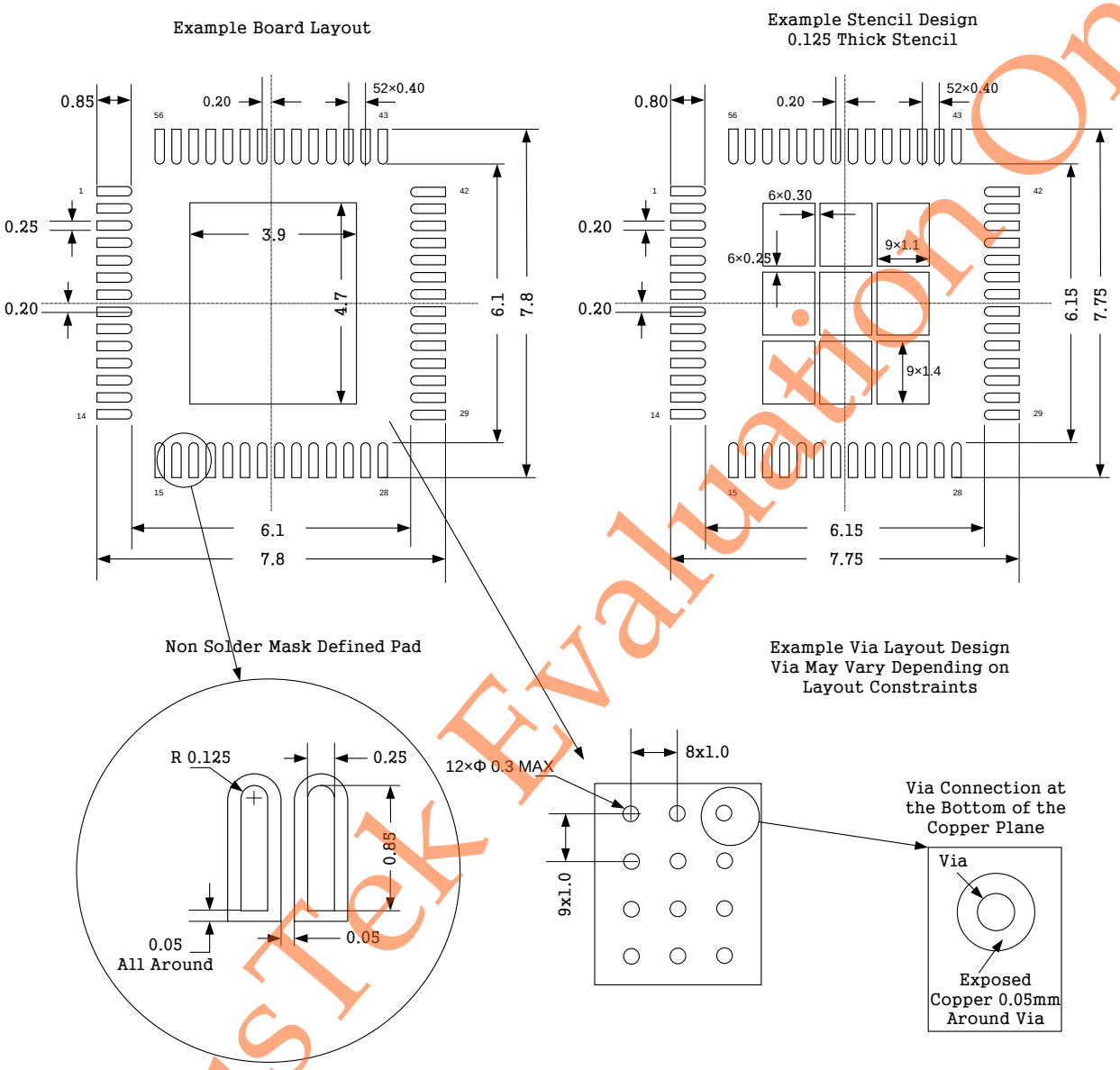


Figure14. The Exposed Thermal Pad Layout Guidelines

NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommend solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.