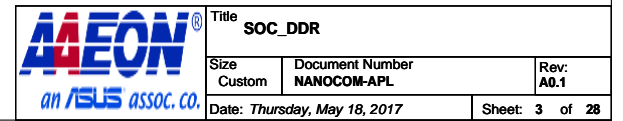
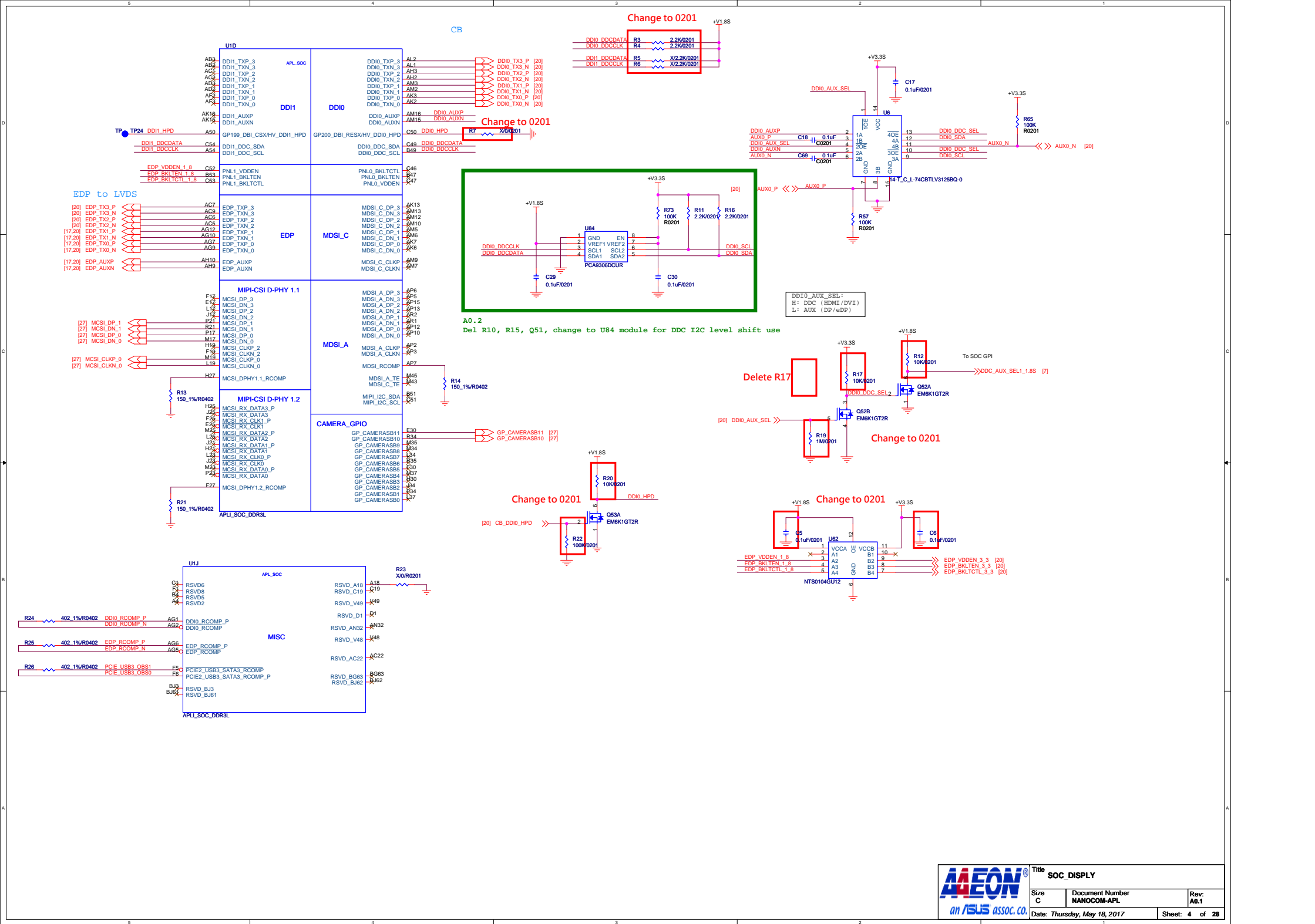


Title POWER_SEQUENCE		
Size Custom	Document Number NANOCOM-APL	Rev: A0.1
Date: <i>Thursday, May 18, 2017</i>		Sheet: 2 of 28





Change to 0201

Change to 0201

Change to 0201

Change to 0201

Change to 0201

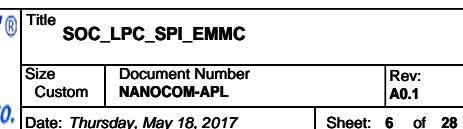
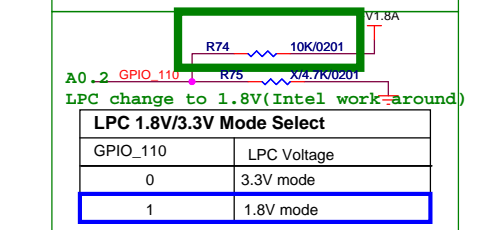
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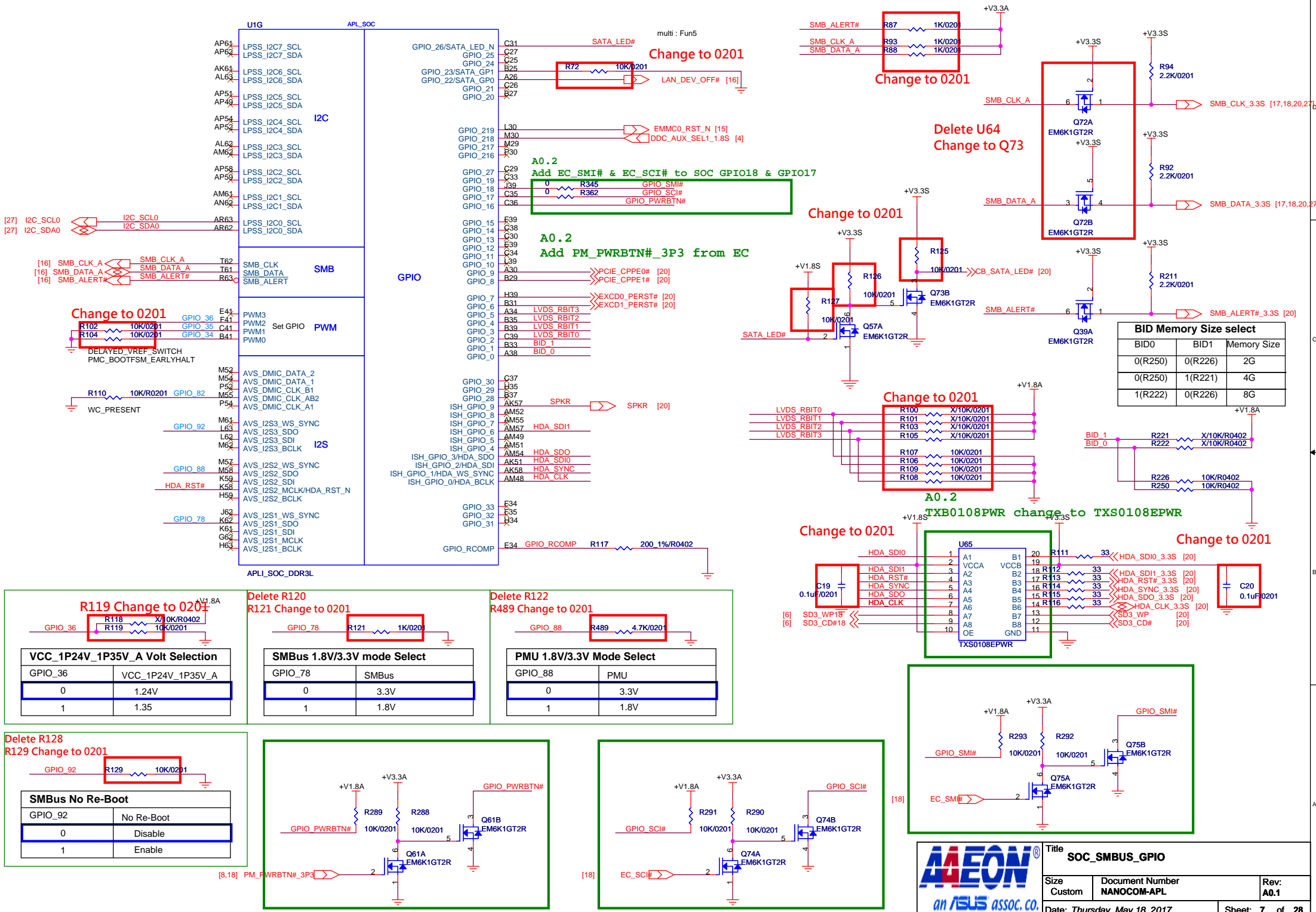
LAN

A0.2
113 ohm change to 100 ohm for USB2.0 eye diagram

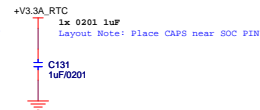
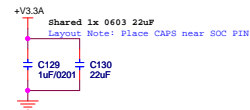
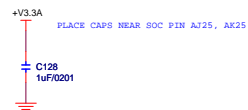
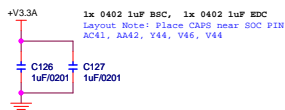
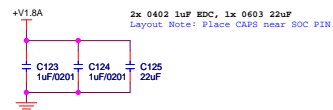
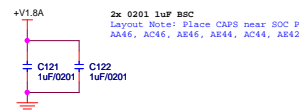
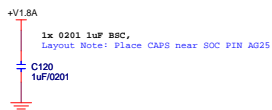
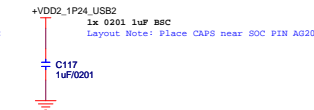
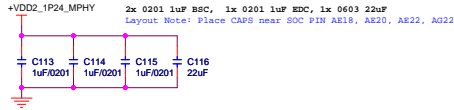
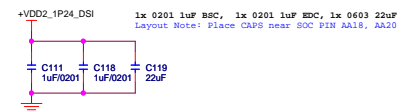
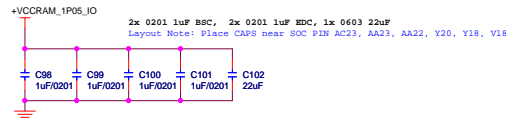
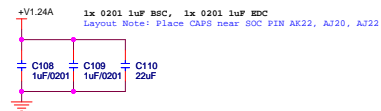
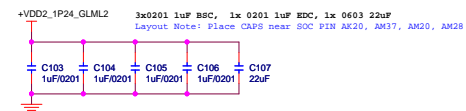
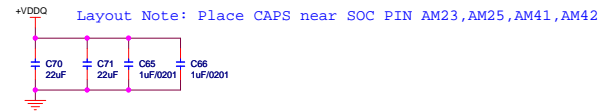
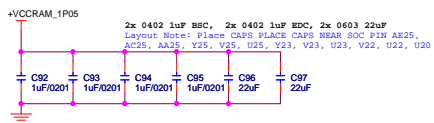
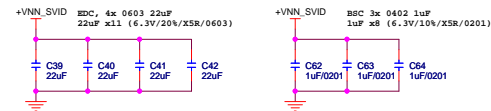
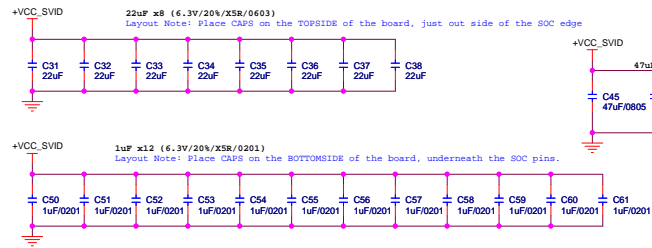


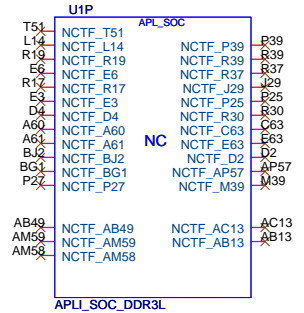
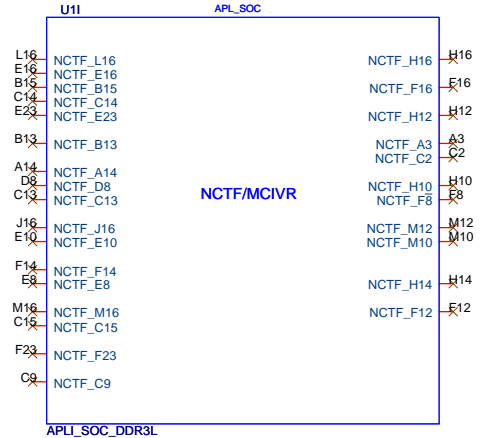
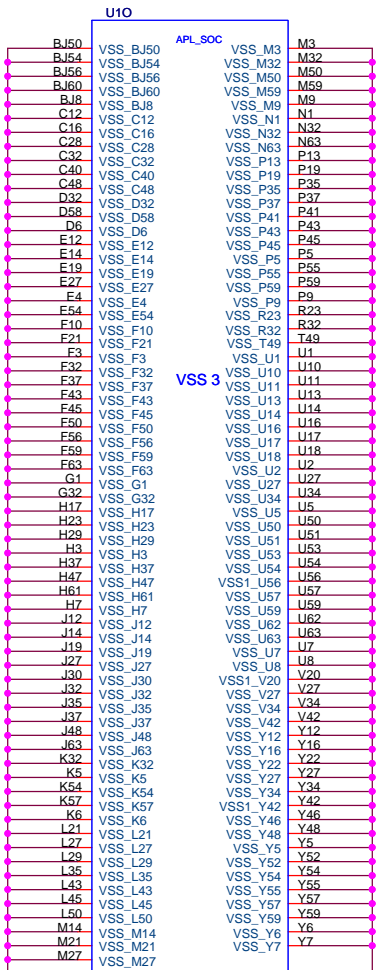
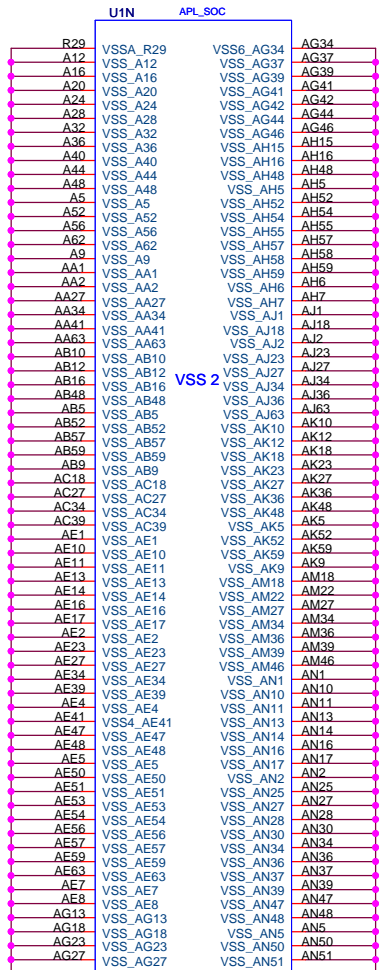
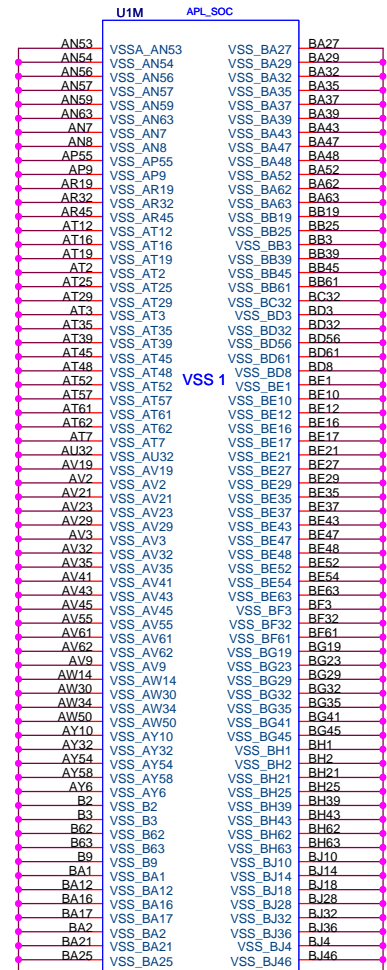
Title SOC_SATA_PCIE_USB		
Size Custom	Document Number NANOCOM-APL	Rev: A0.1
Date: Thursday, May 18, 2017		Sheet: 5 of 28

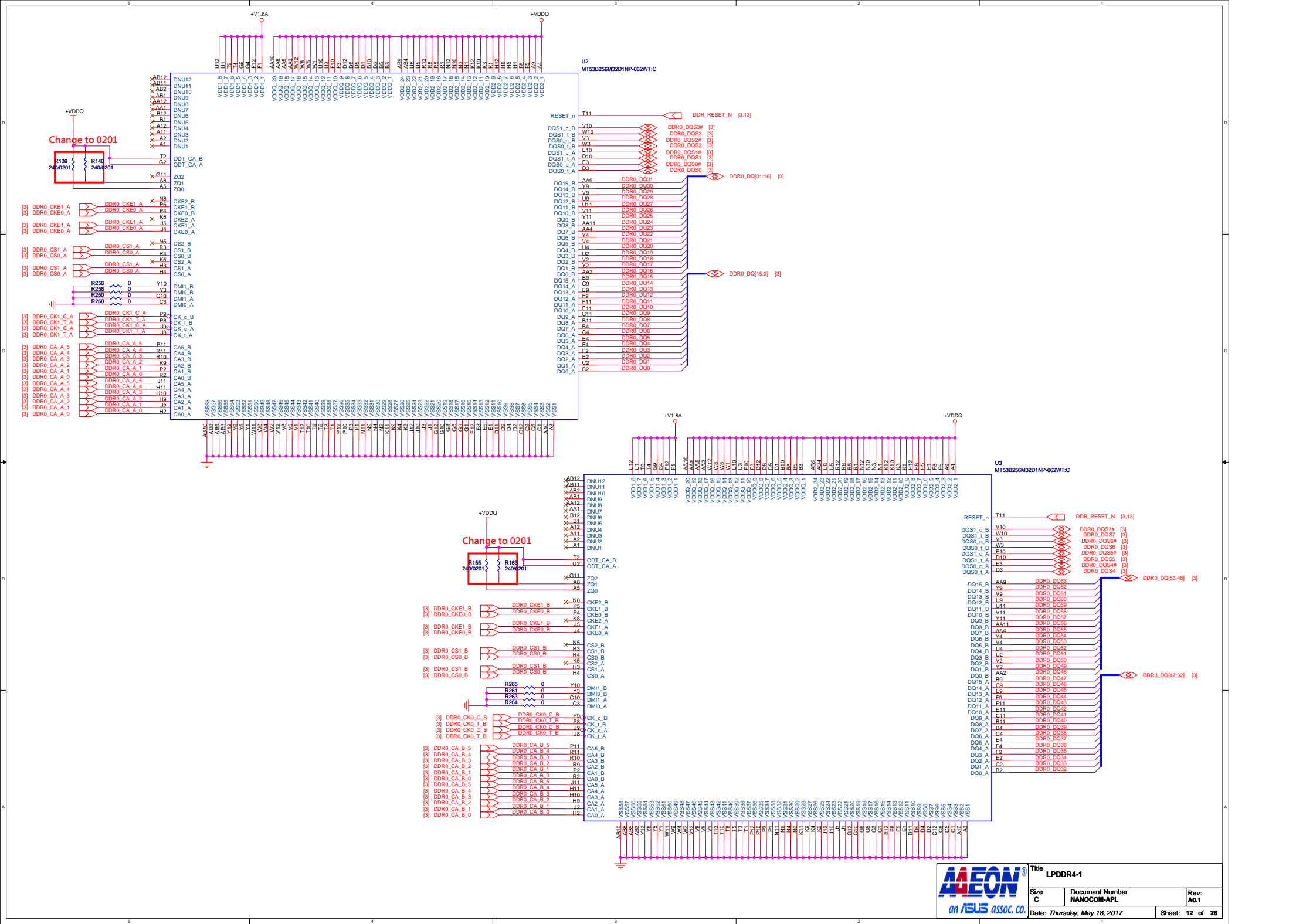


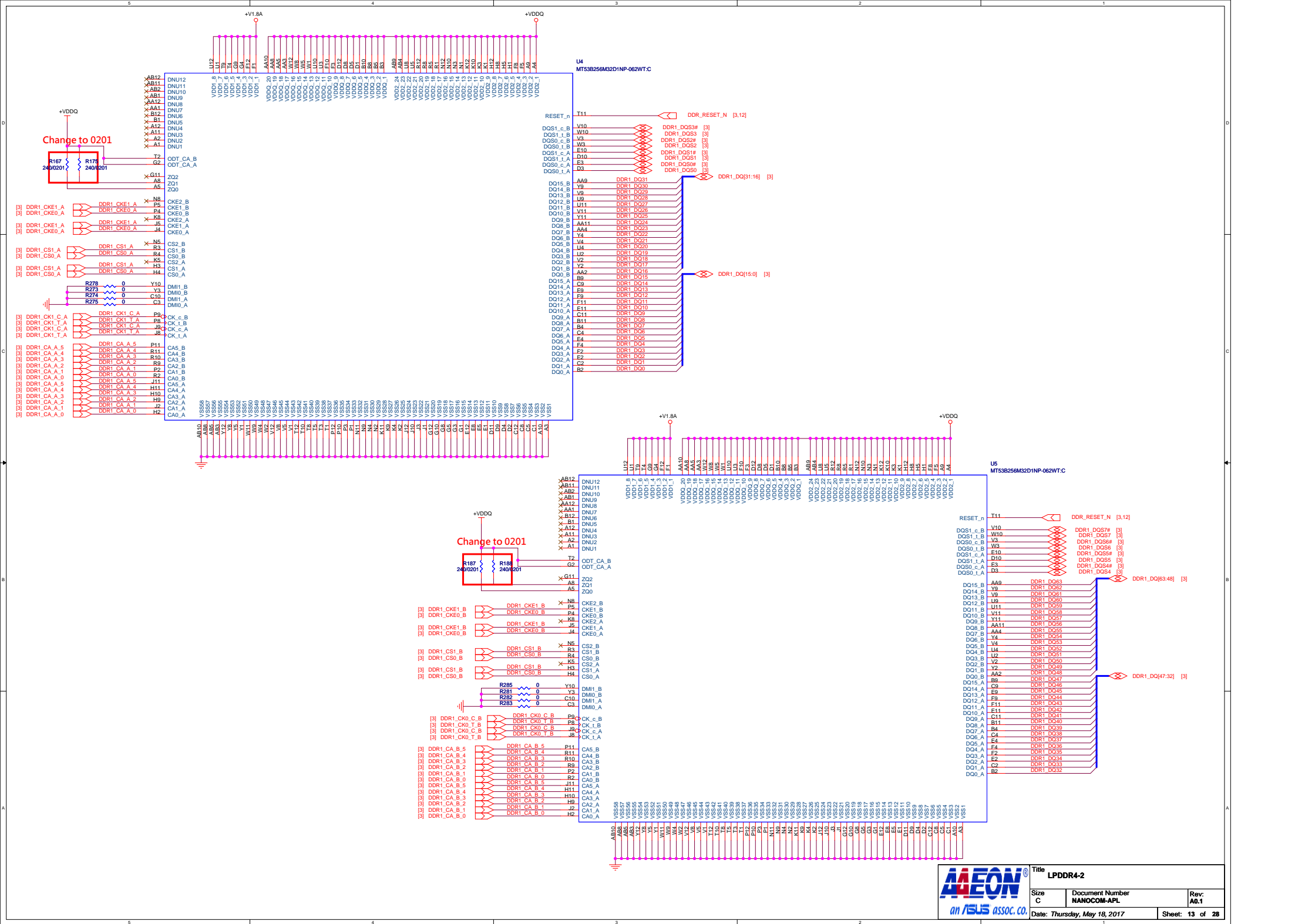


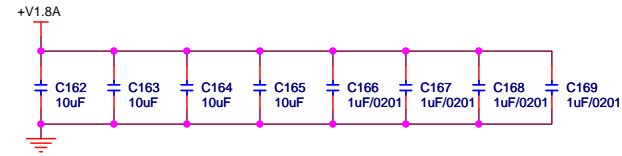
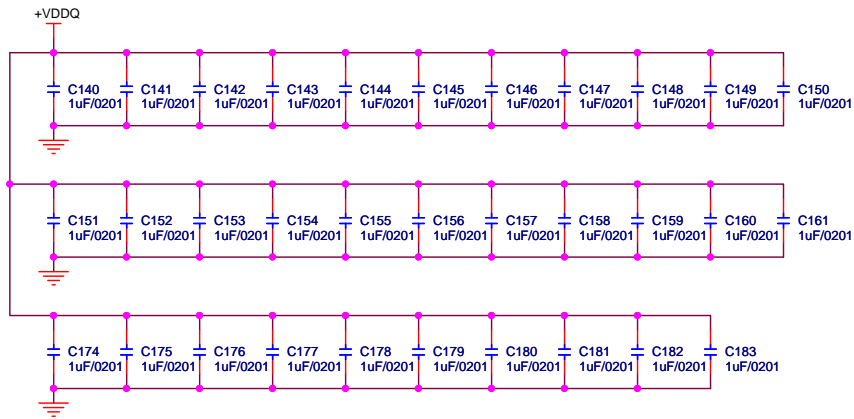
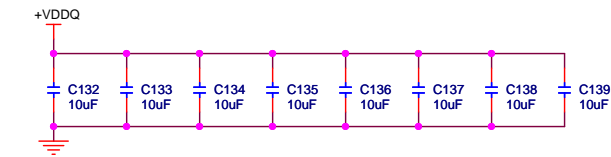
VCC_SVID





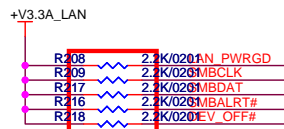




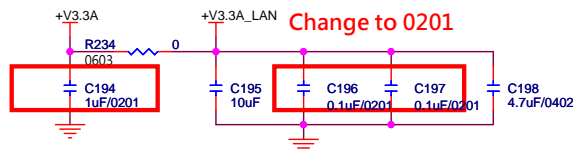
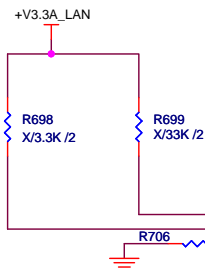


Title LPDDR4_PWR CAP		
Size B	Document Number NANOCOM-APL	Rev: A0.1
Date: Thursday, May 18, 2017		Sheet: 14 of 28

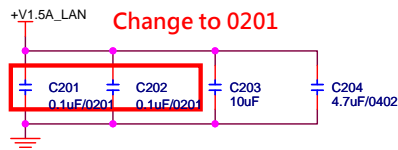
[LAN_SW_SEL]
H: AN = CN (I211 DEF_ON)
L: AN = BN (I211 DEF_OFF)



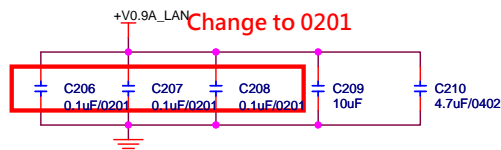
Change to 0201



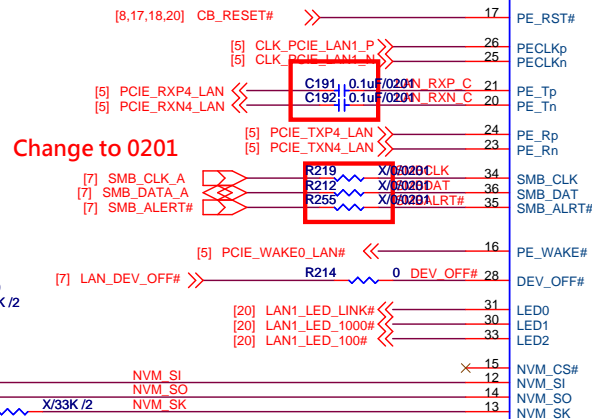
Change to 0201



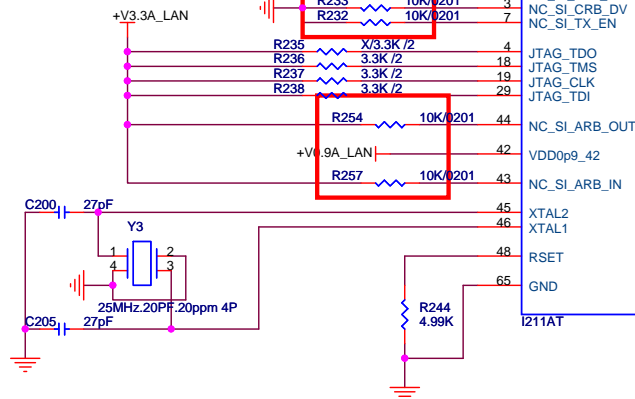
Change to 0201



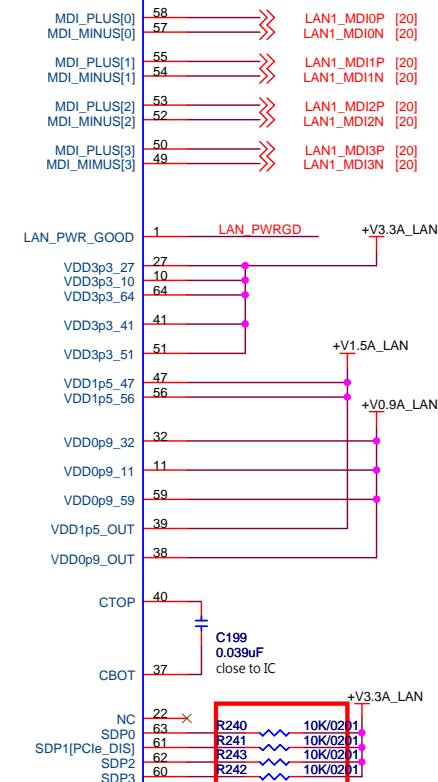
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Change to 0201



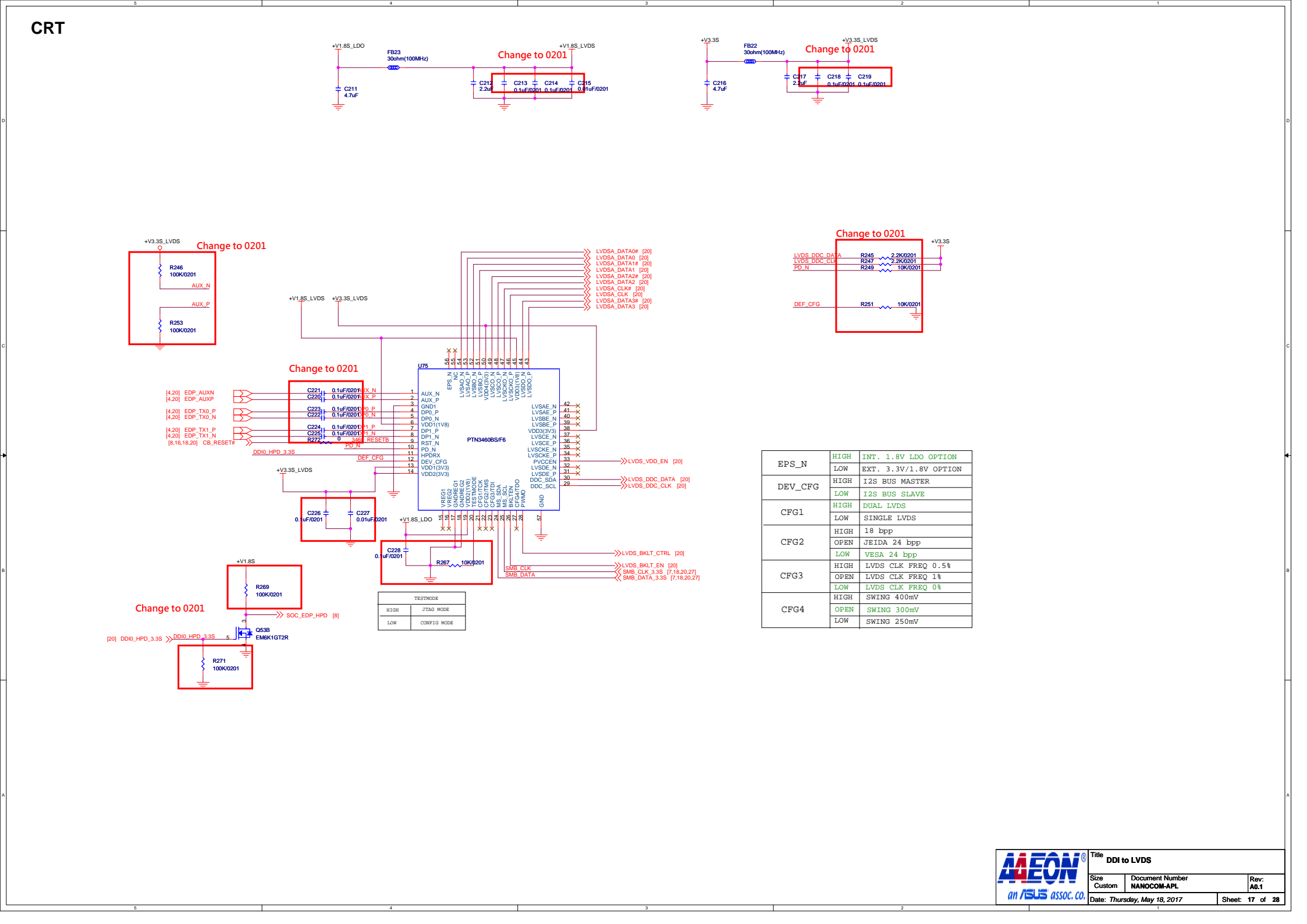
Intel GbE
i211



Change to 0201

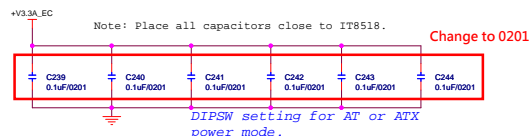
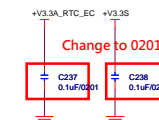
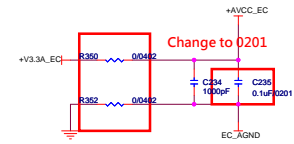
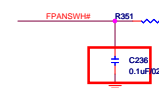
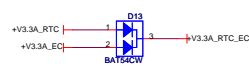
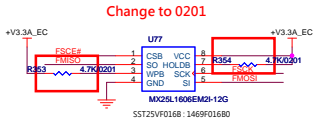
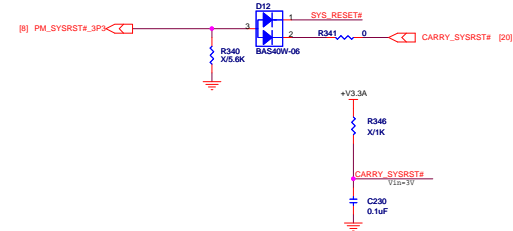
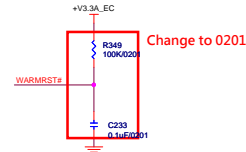
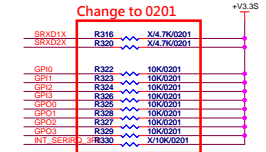
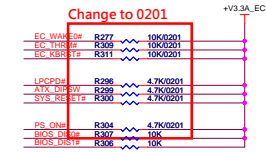
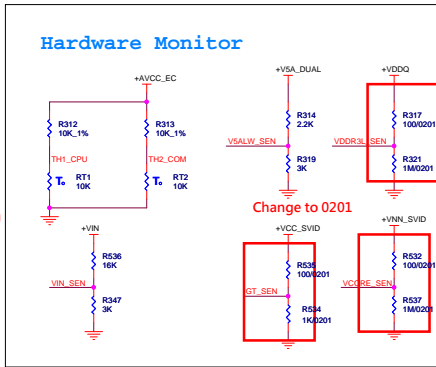
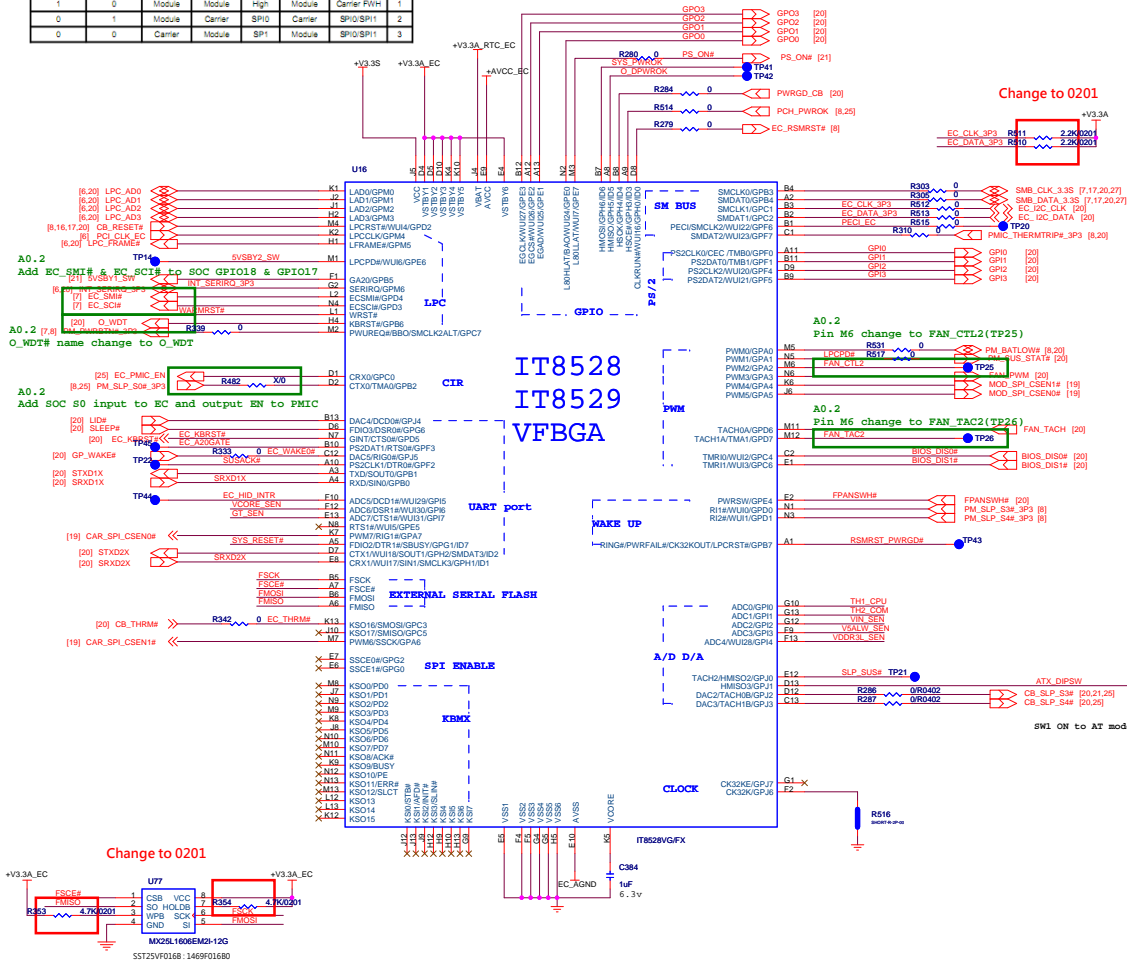


Title LAN i211		
Size B	Document Number NANOCOM-APL	Rev: A0.1
Date: Thursday, May 18, 2017		Sheet: 16 of 28

[illegible]

CRT

BIOS_DIS#	BIOS_DIS#	Chipset	Chipset	Carrier	SPI	Bios Entry	Ref
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	1	Module	Module	High	Carrier	Carrier	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3



GA20/ECSCI/ECSCI/KBRST# pay attention for leak current

(1) Each input pin should be driven or pulled.

(2) Open-drain output pin should be pulled.

DO NOT place any pull up resistor on G0, G2, G6

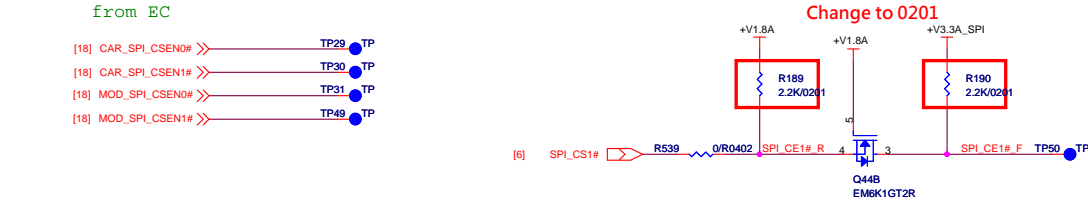
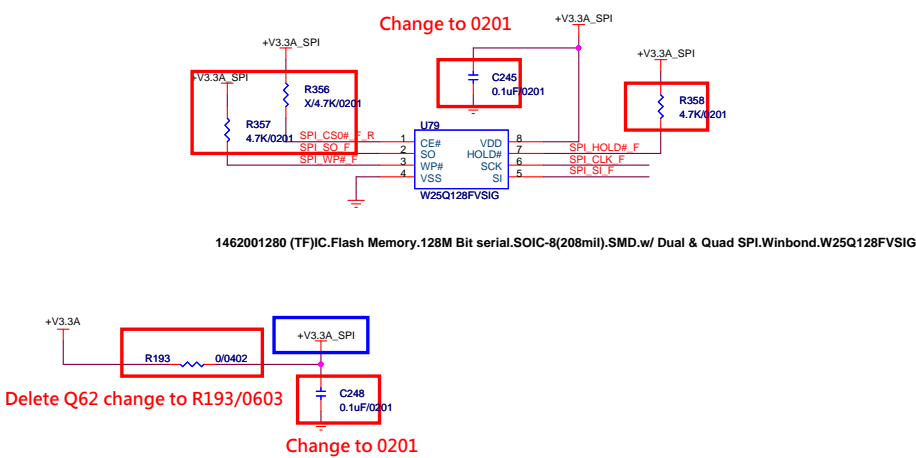
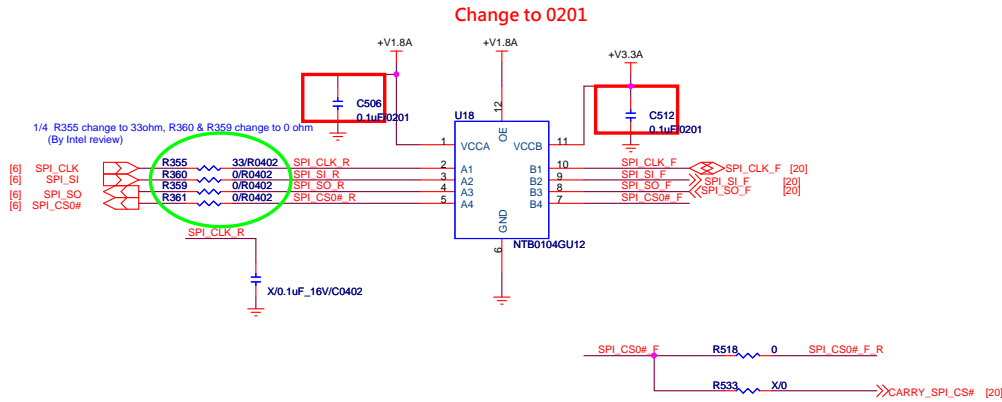
(Reserved for Hardware strapping)

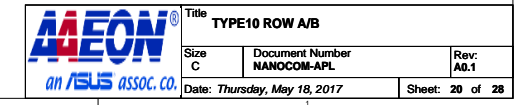
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:

(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.

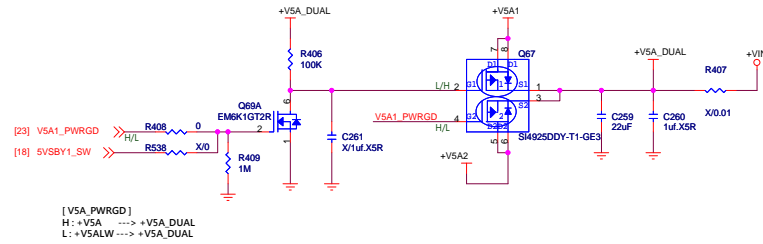
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

SPI BIOS

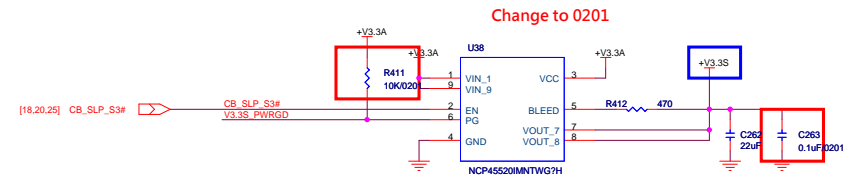
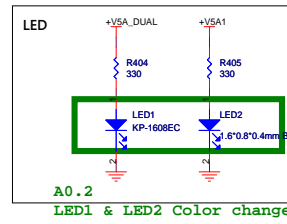
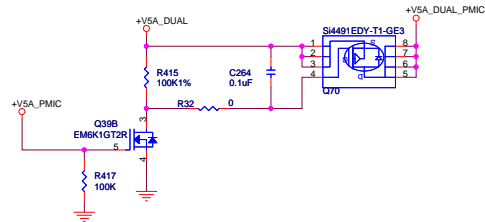
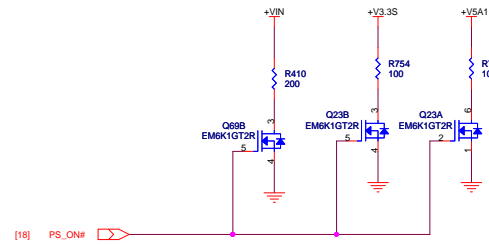




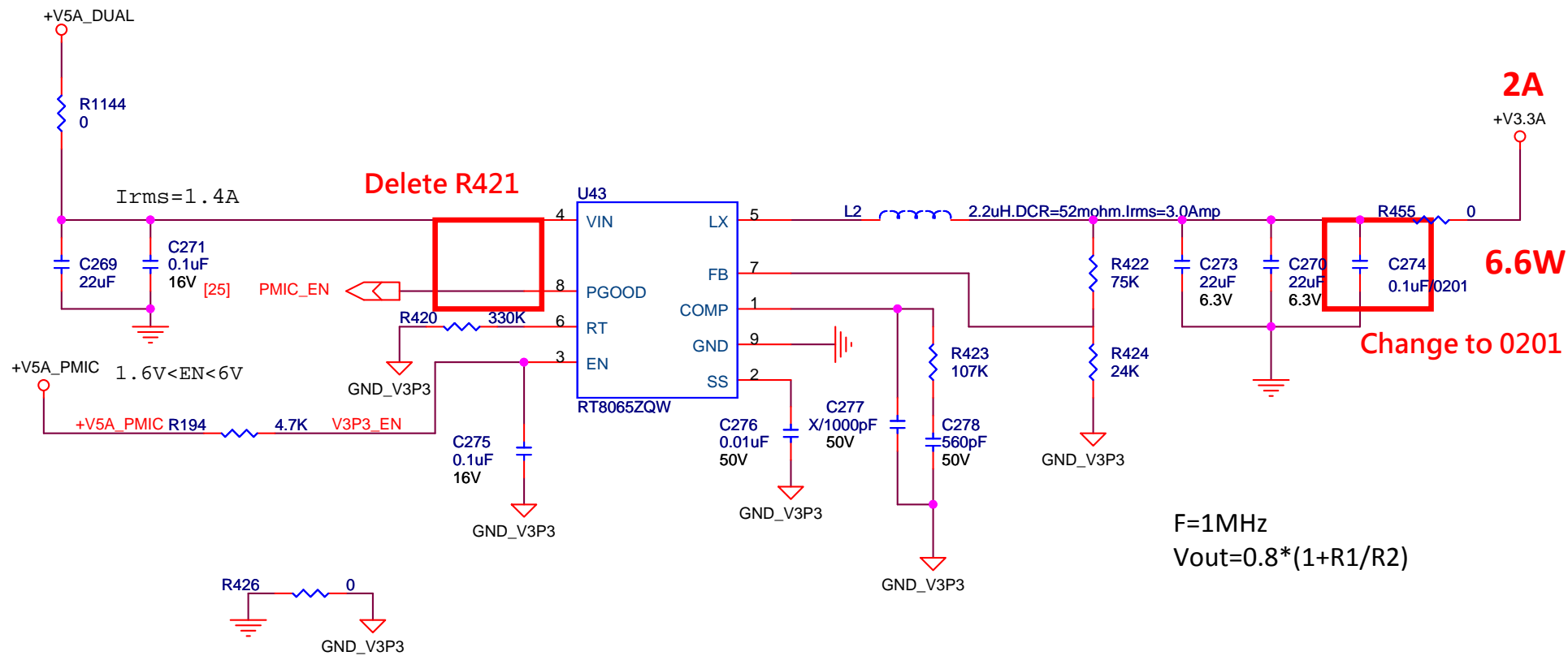
V5A_DUAL Switch



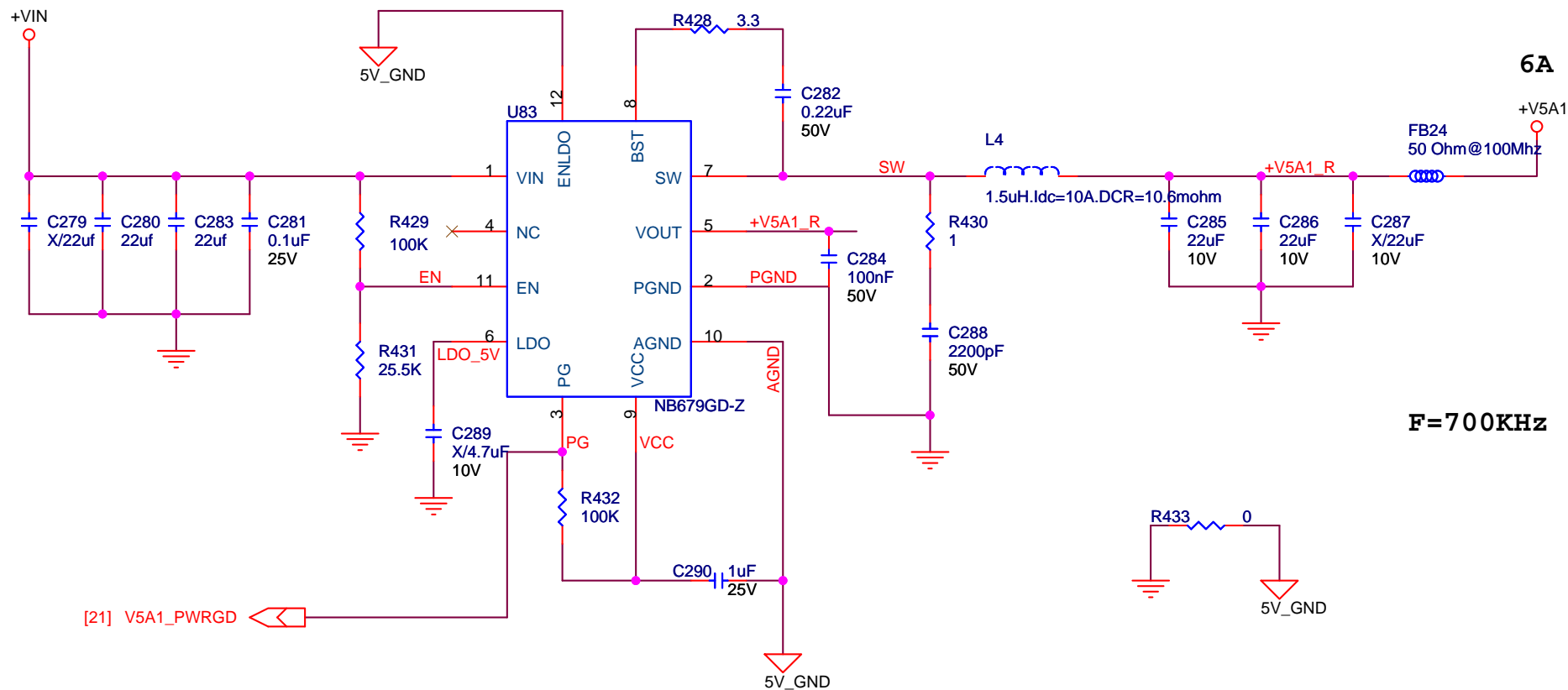
Discharge



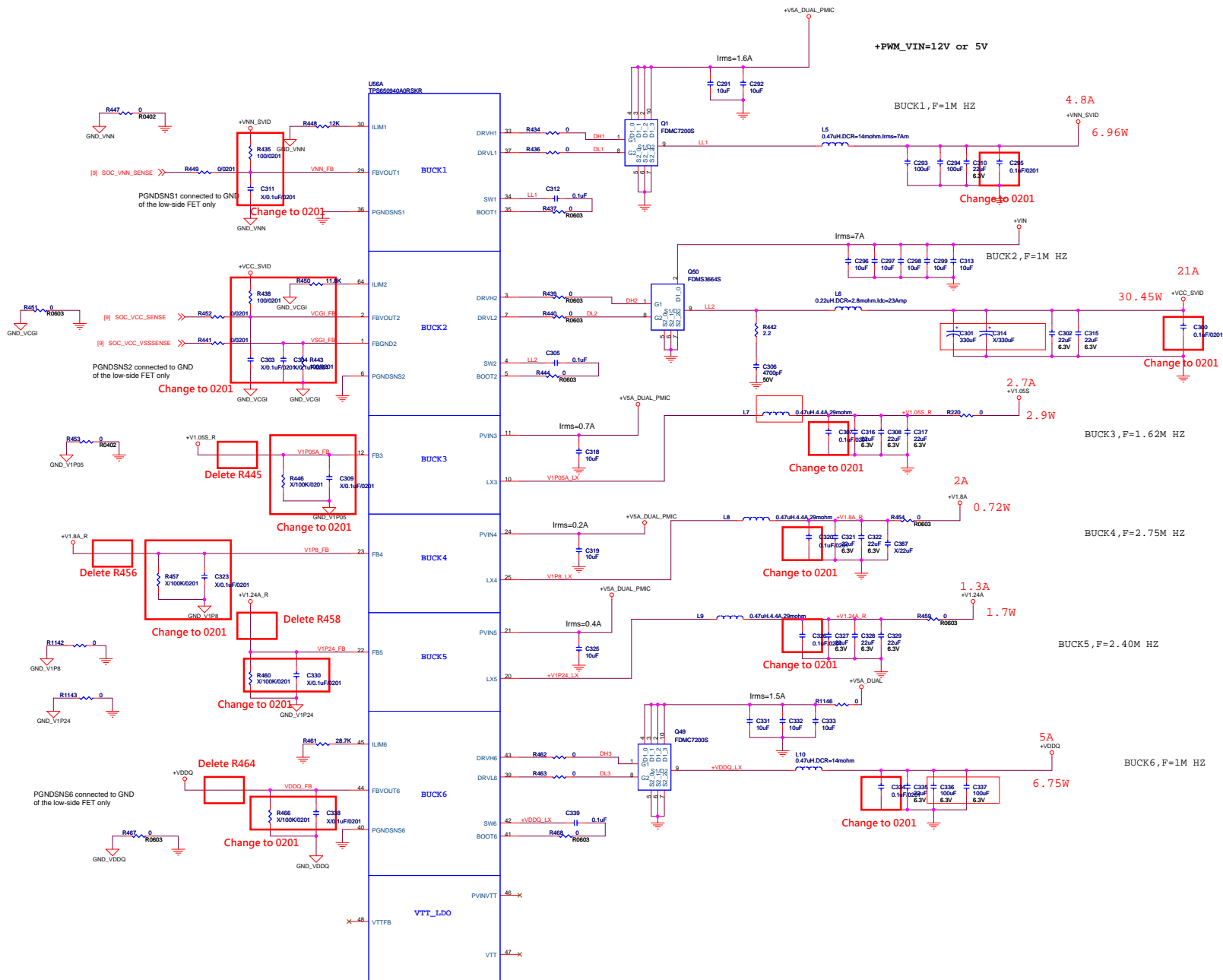
Delete U85 Load switch module

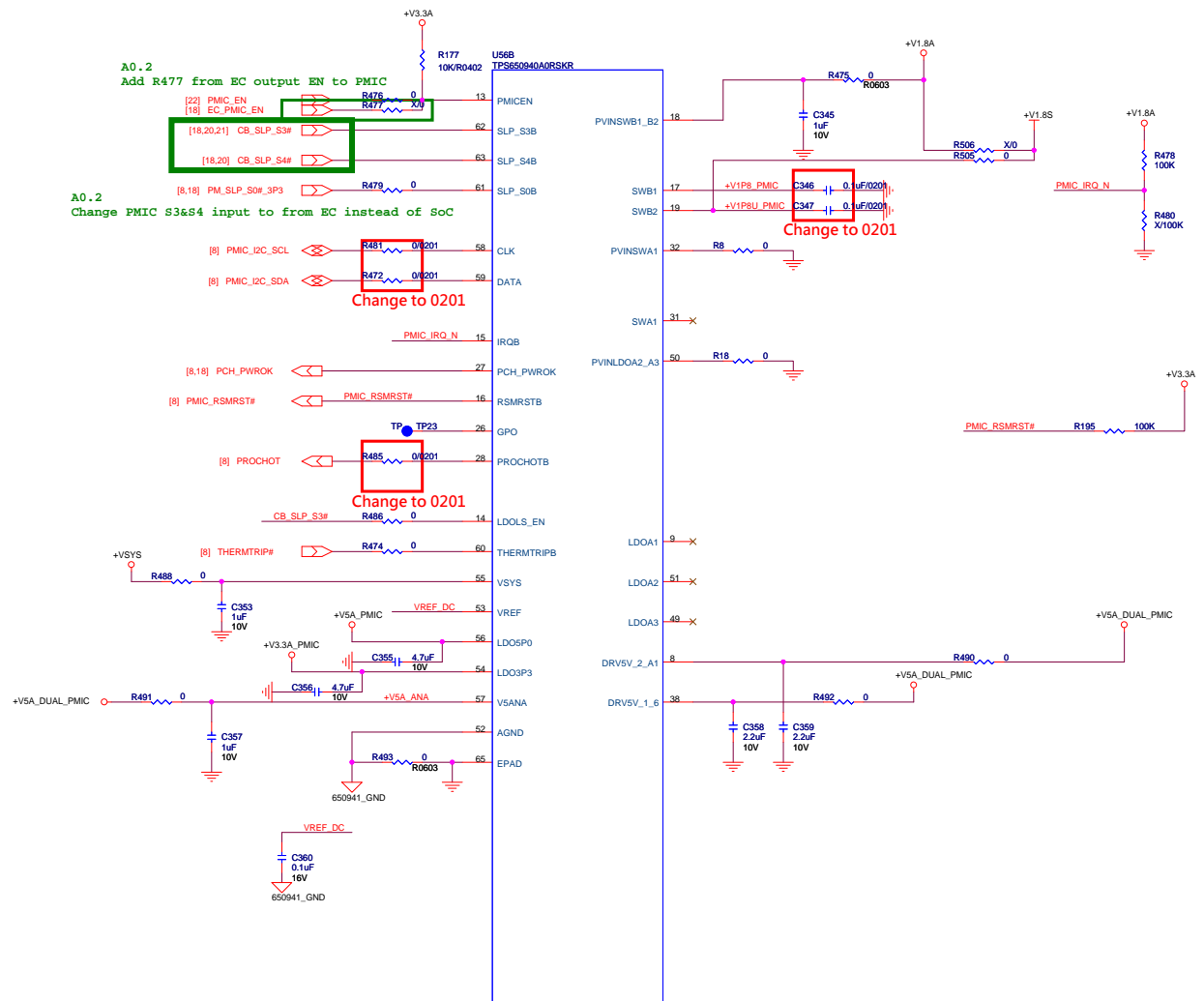


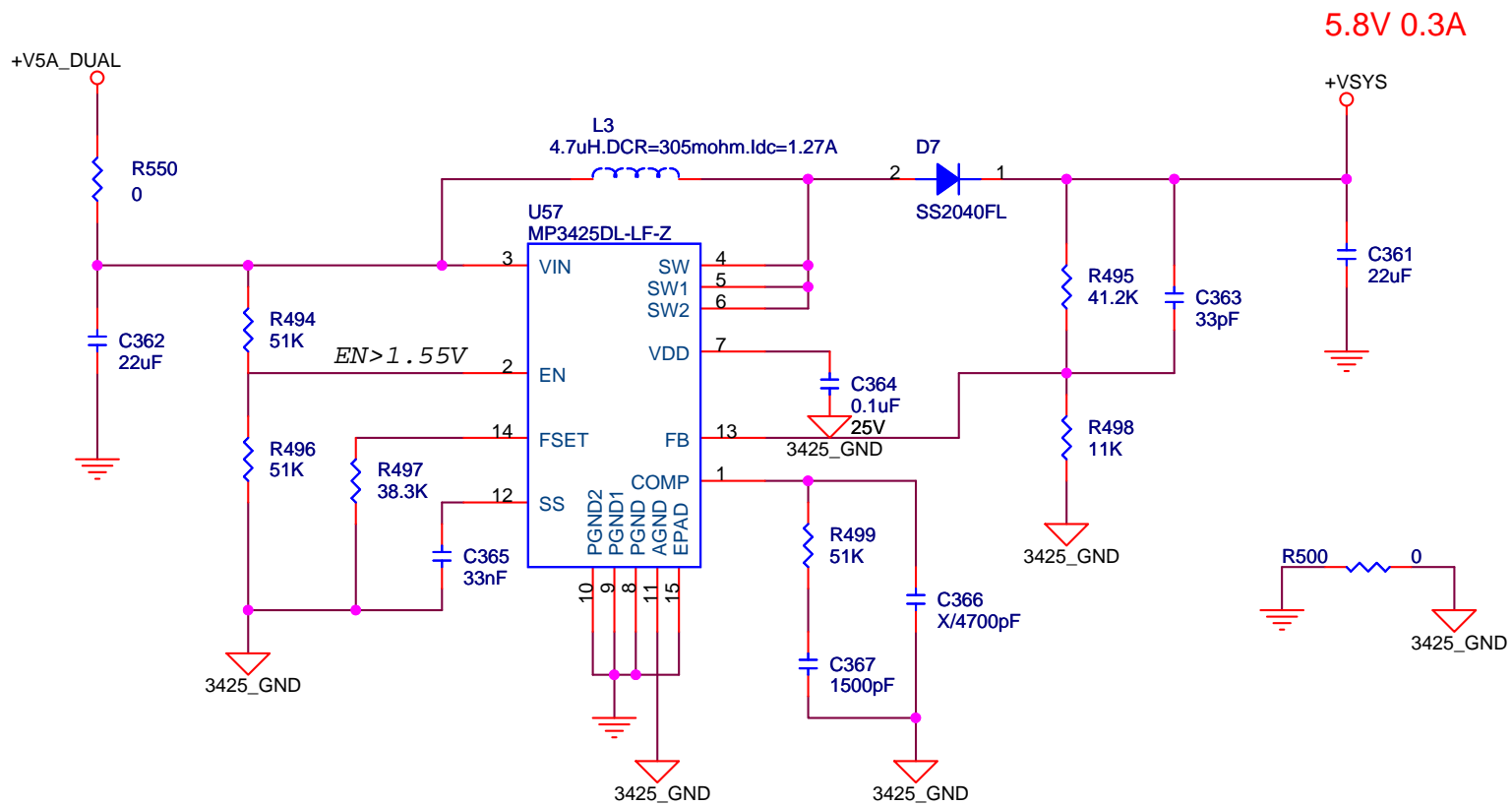
Vin=12V



Title NB679GD_+V5A		
Size A	Document Number NANOCOM-APL	Rev: A0.1
Date: <i>Thursday, May 18, 2017</i>		Sheet: 23 of 28

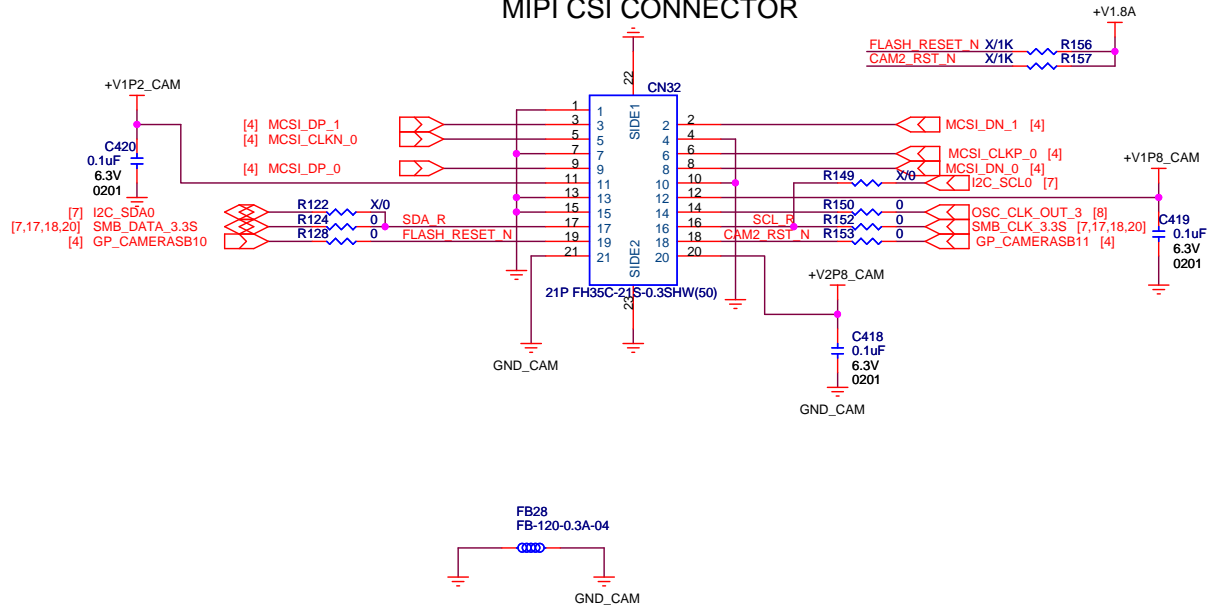




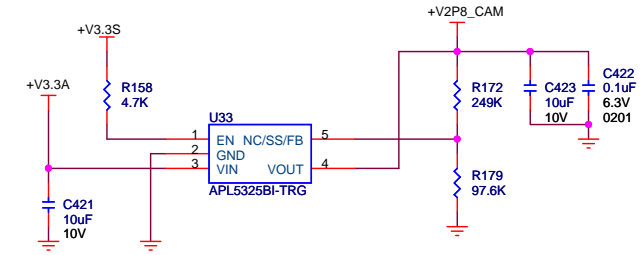


Title MP3425_+VSYS		
Size A	Document Number NANOCOM-APL	Rev: A0.1
Date: <i>Thursday, May 18, 2017</i>		Sheet: 26 of 28

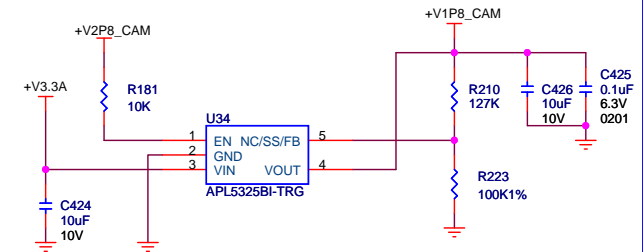
MIPI CSI CONNECTOR



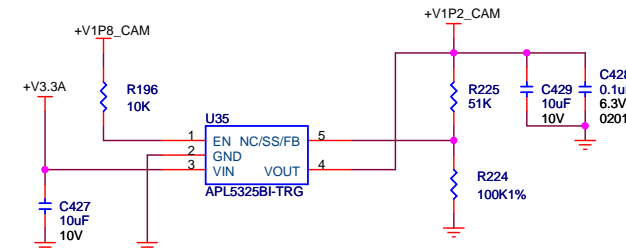
+V2P8_CAM



+V1P8_CAM



+V1P2_CAM



Title MIPI-CSI		
Size B	Document Number NANOCOM-APL	Rev: A0.1
Date: Thursday, May 18, 2017		Sheet: 27 of 28

