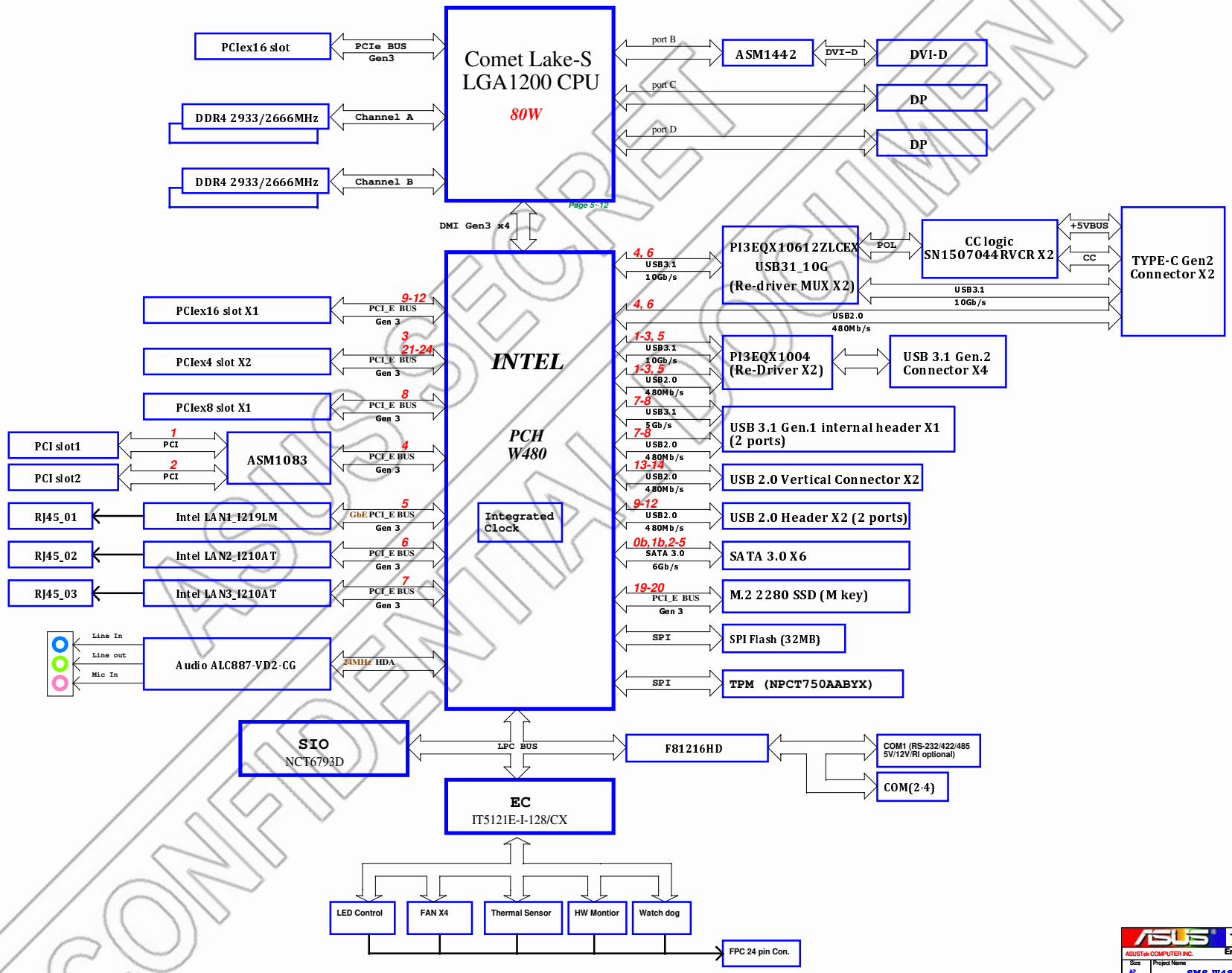
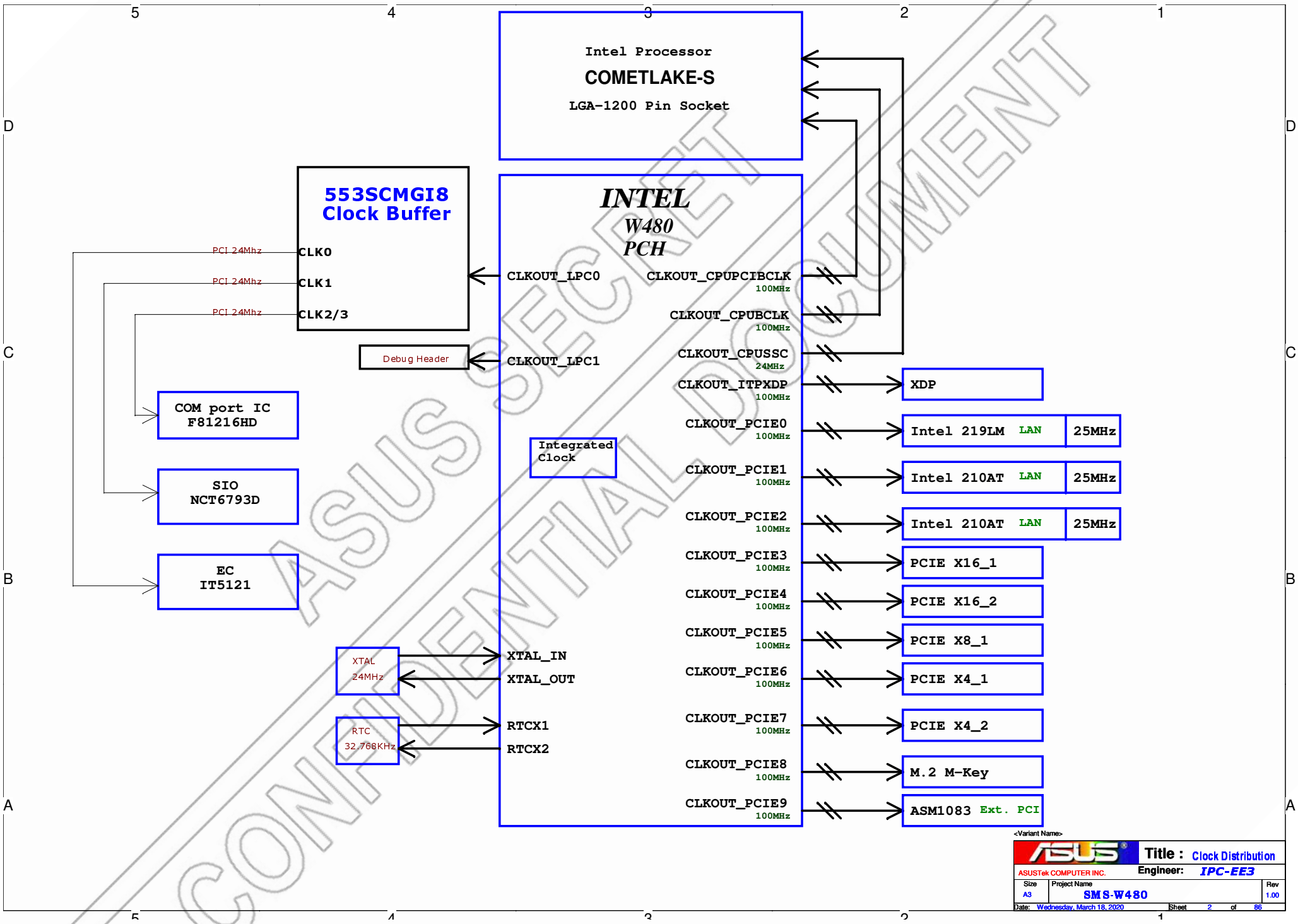
SMS-W480-A10
Block Diagram Rev 1.00



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS ASUSTeK COMPUTER INC.
Title : Block Diagram
Engineer: IPC-EE3
Size A2 | Project Name SMS-W480 | Rev 1.00
Date: Wednesday, March 18, 2020 | Sheet 1 of 86



<Variant Name>

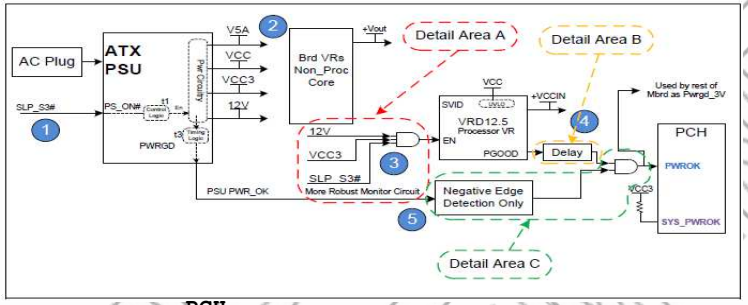
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: IPC-EE3

Size	Project Name	Rev
A3	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 2 of 86



RESET_SWITCH

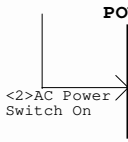
POWER_SWITCH

SIO
NCT6793D

PCH
LYNX POINT
W480

PROCESSOR
Comet Lake

POWER SUPPLY



<2>AC Power Switch On

<5>O_PWRBTN#IN
PSIN#
RESETCONO#
O_RSTCON#
SYS_RESET#
<16>S_PLTRST#
LRESET#
PLTRST#
PLTRST_CPU#
*4
<19>H_CPURST_SB#
RESET#
O_KB_RST#
KBRST#
RCIN#
<4>O_RSMRST#
RSMRST#
RSMRST#
RTCRST#
<1>RTCRST#
<6>O_PWRBTN#
PSOUT#
PWRBTN#
SRTCRST#
<1>SRTCRST#
BATTERY
<10>12V,5V,3V
<3>+5VSB_ATX,+3VSB_ATX
<9>ATX_PSON#
<11>PWRGD_PS//ATXPG_IN
PSON#
*1
ATXPGD
*2
<8>S_SLPS4#
SLP_S5#
SLP_S5#
SLP_S4#
<9>S_SLPS3#
SLP_S3#
SLP_S3#
<11>+VCCIO
<12>+VCCSA
<15>H_PWRGD
CPUPWRGD
PROCPWRGD
<4.1>S_DPWROK
DSW_PWROK
<14>H_VCCST_CPUPWRGD
VCCST_PWRGD
<10>PCH_SYSPWROK
SYS_PWROK
PCH_PWROK
<17>VRM_SVID
<18>+VCCCORE//+VCCGT
SVID
+VCCCORE//+VCCGT

*1
PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2
PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3
Come with +3VSB_ATX and gated by SLP_S3#, P_+VCCIO_PG_10

*4
PLTRST_CPU#=PLTRST#, voltage=1V, directly connect to CPU

Vcore Controller

SVID
VCORE
VR_ON
PGOOD
RT3609BEGQW

<13>VR_READY_10
*3
S_SLPS3#
P_+VCCIO_PG_10

CHIP

SOCKET or SLOT

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<Variant Name>

ASUS

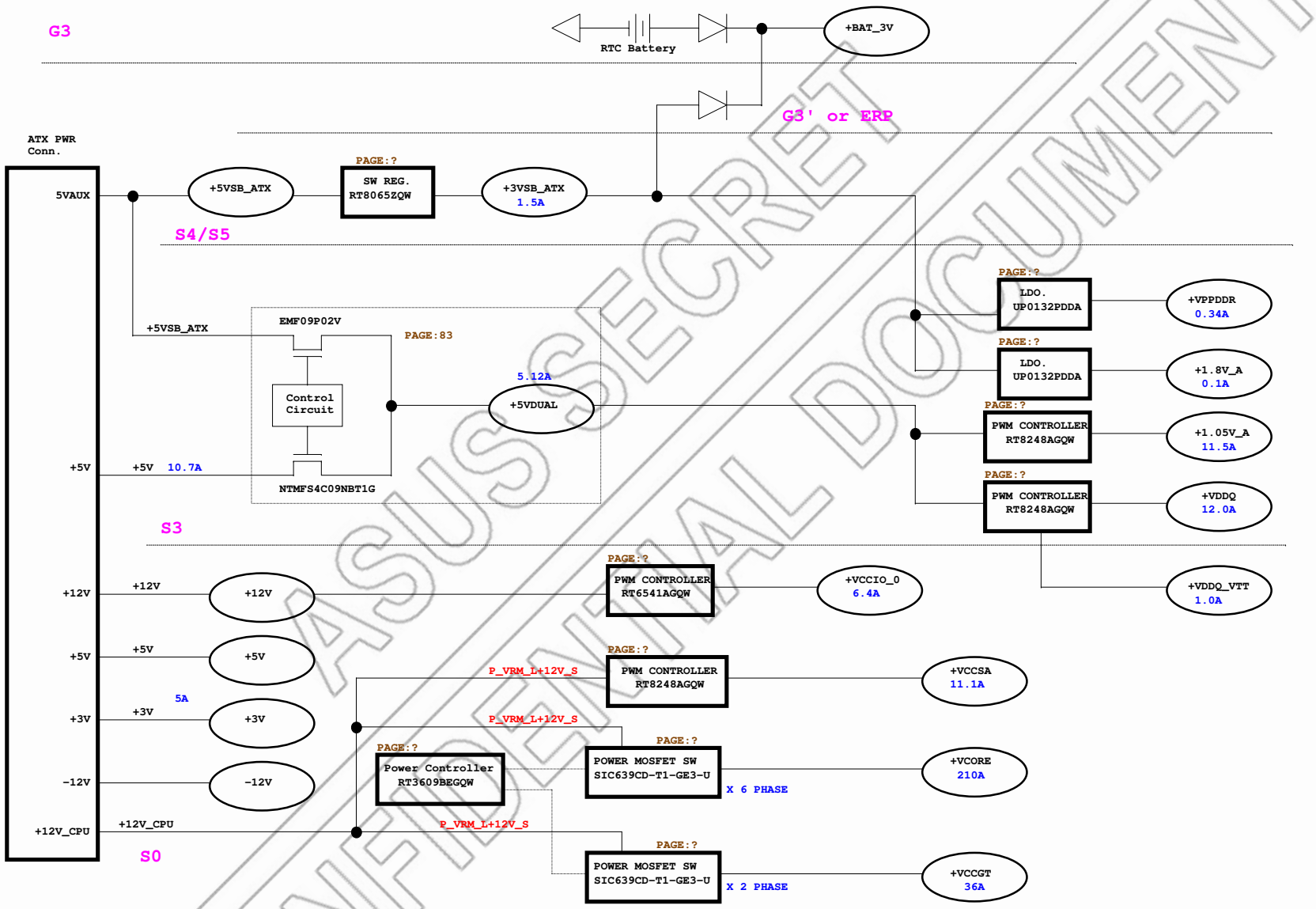
Title : Signal & Reset map

ASUSTek COMPUTER INC.

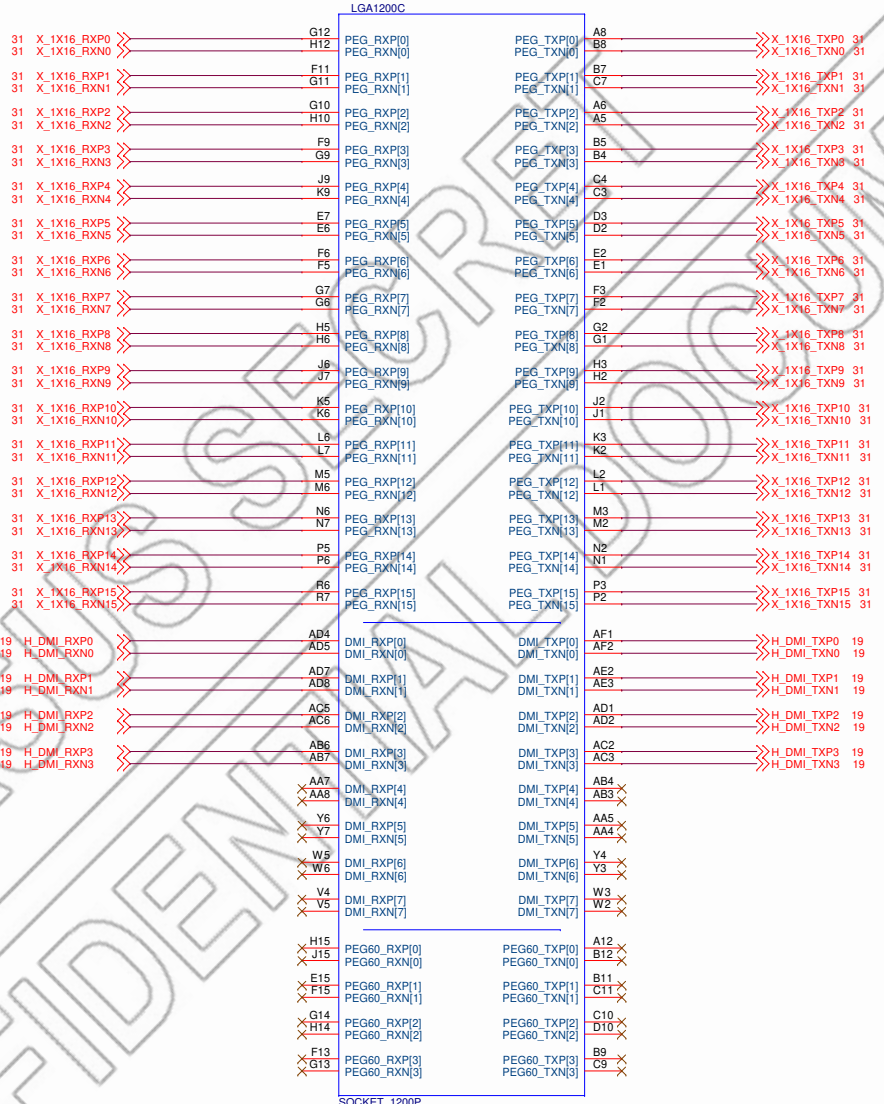
Engineer: IPC-EE3

Size	Project Name	Rev
A3	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 3 of 86



ASUS SECRET
CONFIDENTIAL DOCUMENT



[GA]FOXCONN/PE12001-11AJ1-1H

12001-00280400

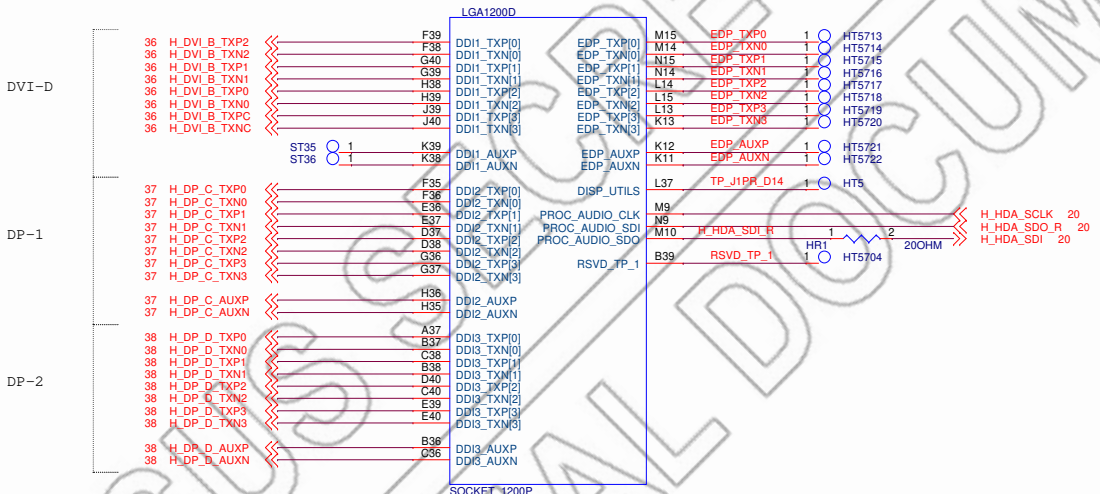
LGA1200 LGA 1200P SOCKET 15U SMT

1st P/N : 12001-00280400 FOXCONN/PE12001-11AJ1-1H

2nd P/N : 12001-00280300 LOTES/AZIF0181-P001C

ASUSTek Computer Inc.	Title : LGA1200 (DMI/PEG)	
	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 5 of 86	

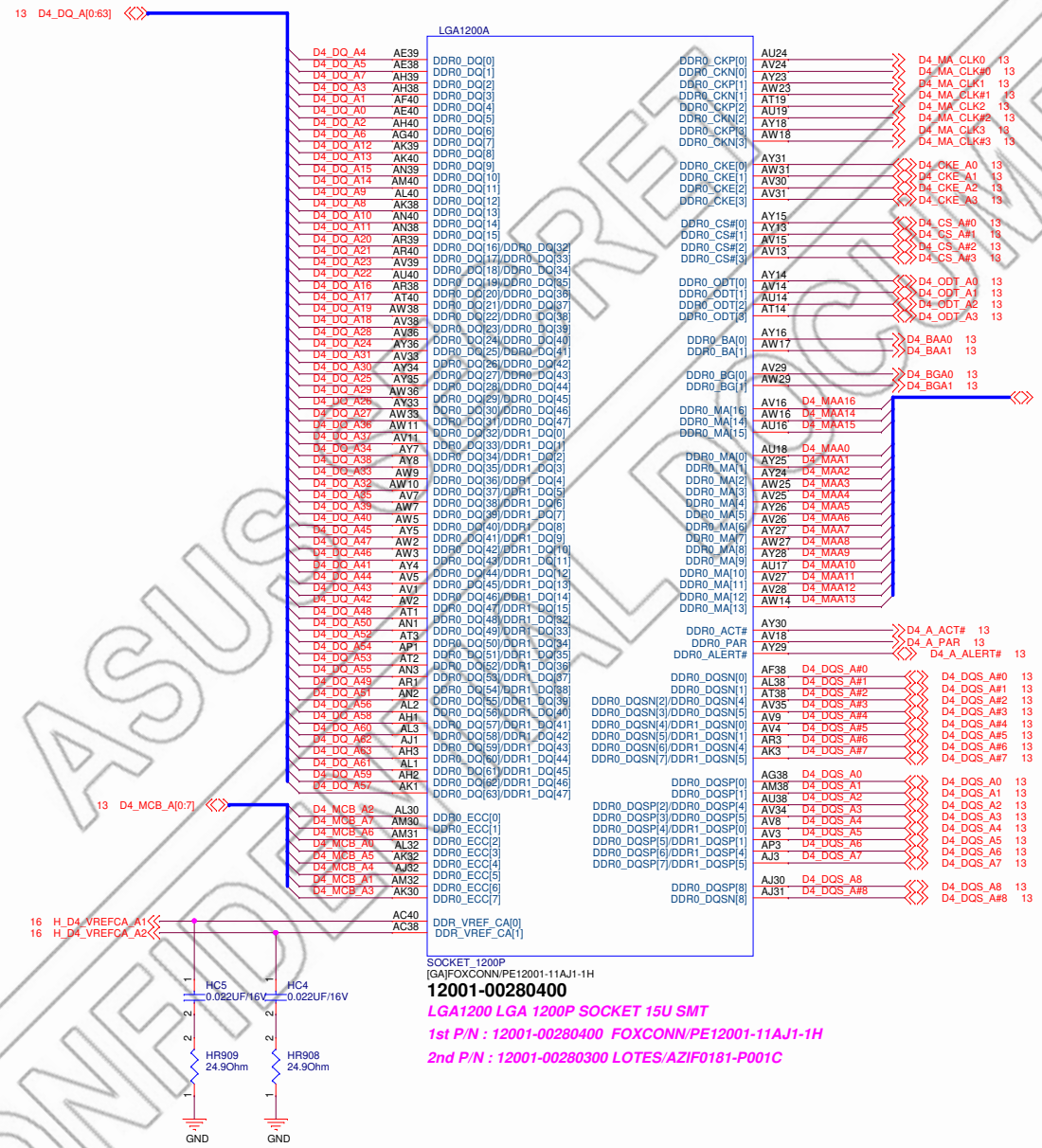
ASUS SECRET
CONFIDENTIAL DOCUMENT



ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUSTek Computer Inc.	Title: LGA1200 (FDI/DISPLAY)	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480		Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 6 of 86		

Channel A
4 Layer routing



SOCKET_1200P
[GA]FOXCONN/PE12001-11AJ1-1H

12001-00280400

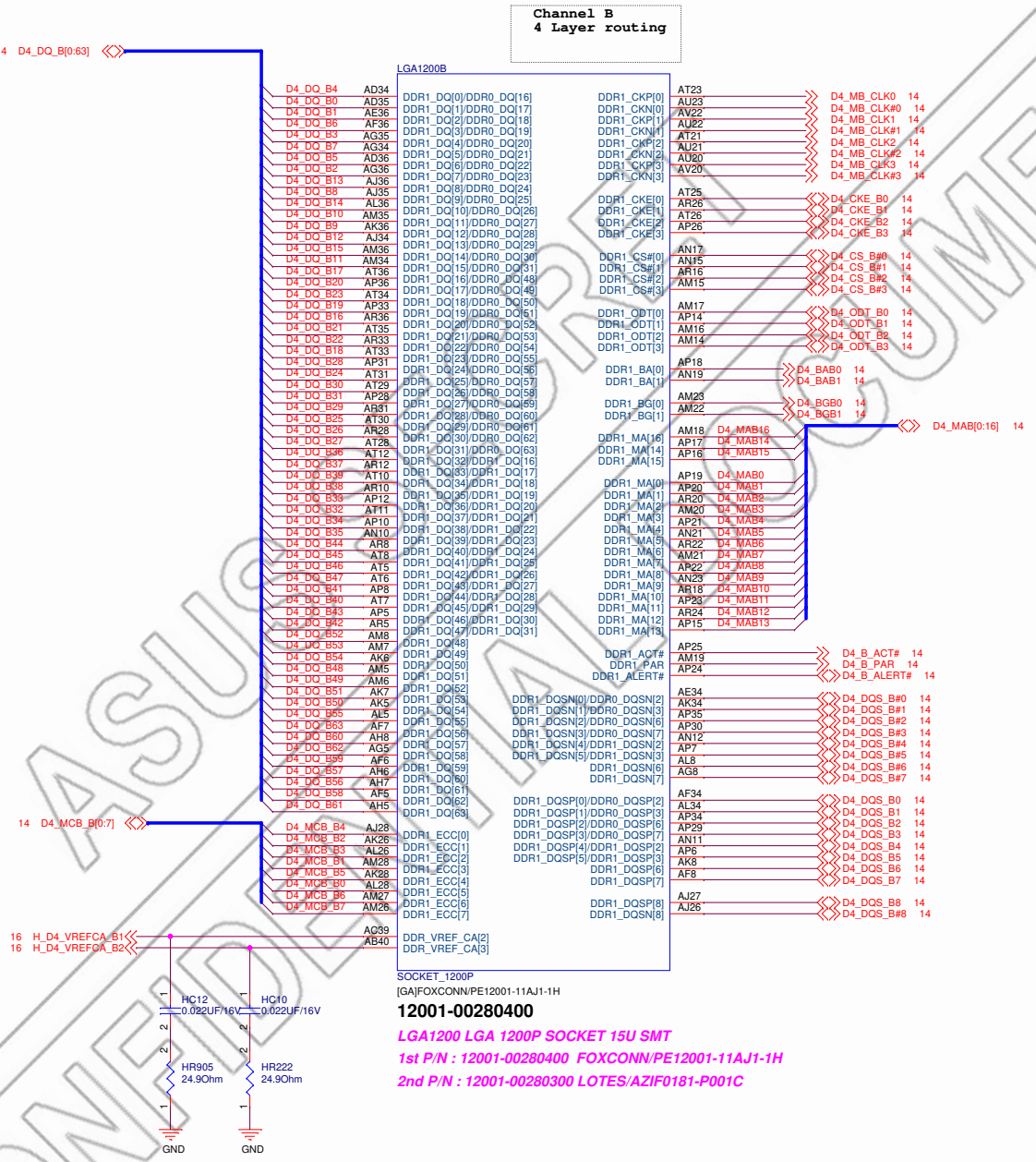
LGA1200 LGA 1200P SOCKET 15U SMT

1st P/N : 12001-00280400 FOXCONN/PE12001-11AJ1-1H

2nd P/N : 12001-00280300 LOTES/AZIF0181-P001C

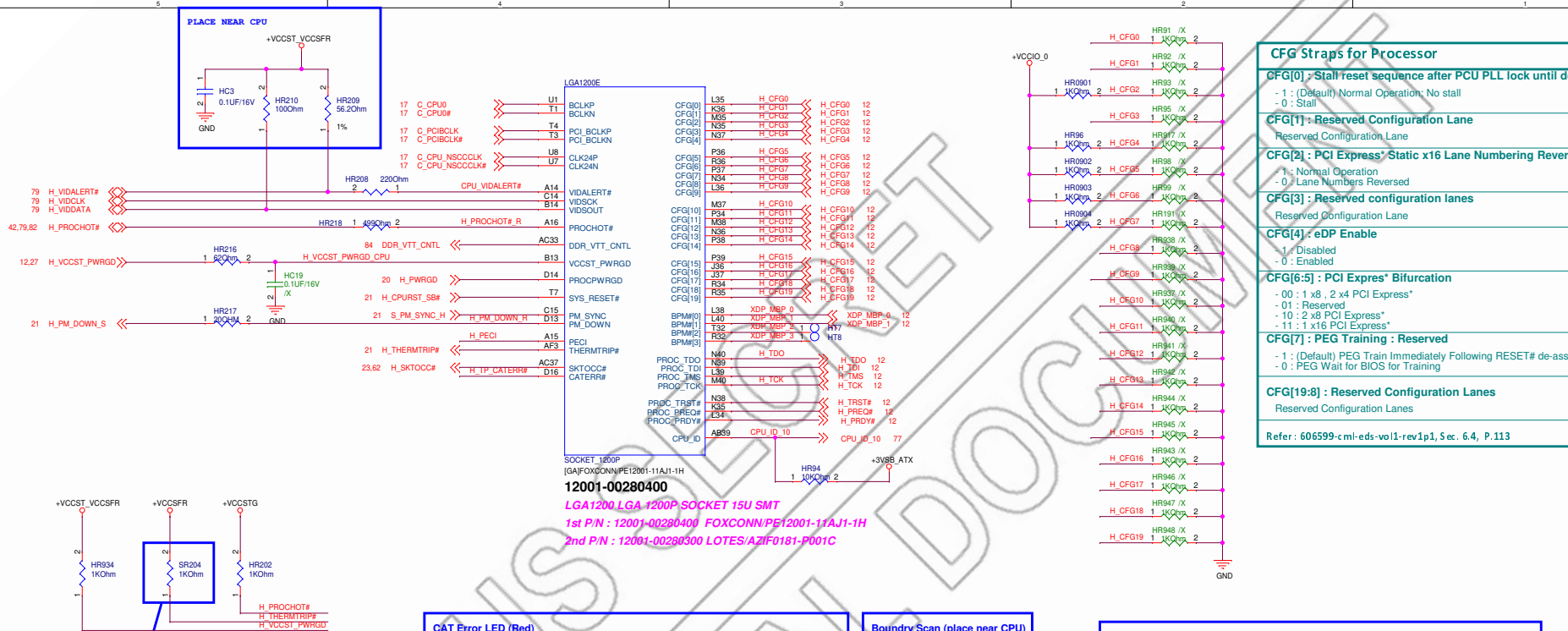
ASUS	Title: LGA1200 (DDR4_A Control)		
ASUSTek Computer Inc.	Engineer: IPC-EE3		
Size A3	Project Name SMS-W480		Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 7 of 86		

ASUS CONFIDENTIAL DOCUMENT



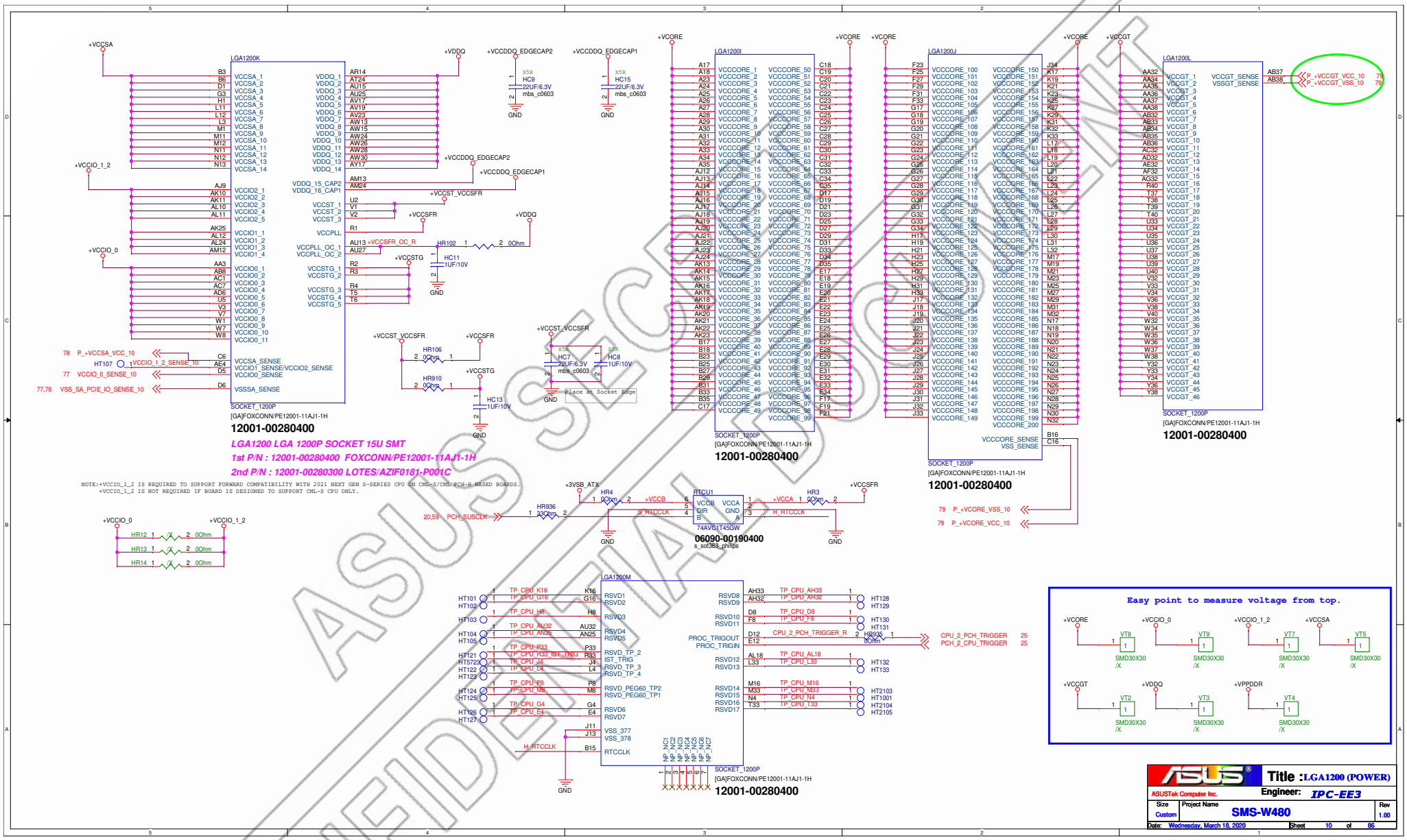
ASUS	Title: LGA1200 (DDR4_B Control)		
ASUSTek Computer Inc.	Engineer: IPC-EE3		
Size A3	Project Name SMS-W480		Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 8 of 86		

ASUS CONFIDENTIAL DOCUMENT

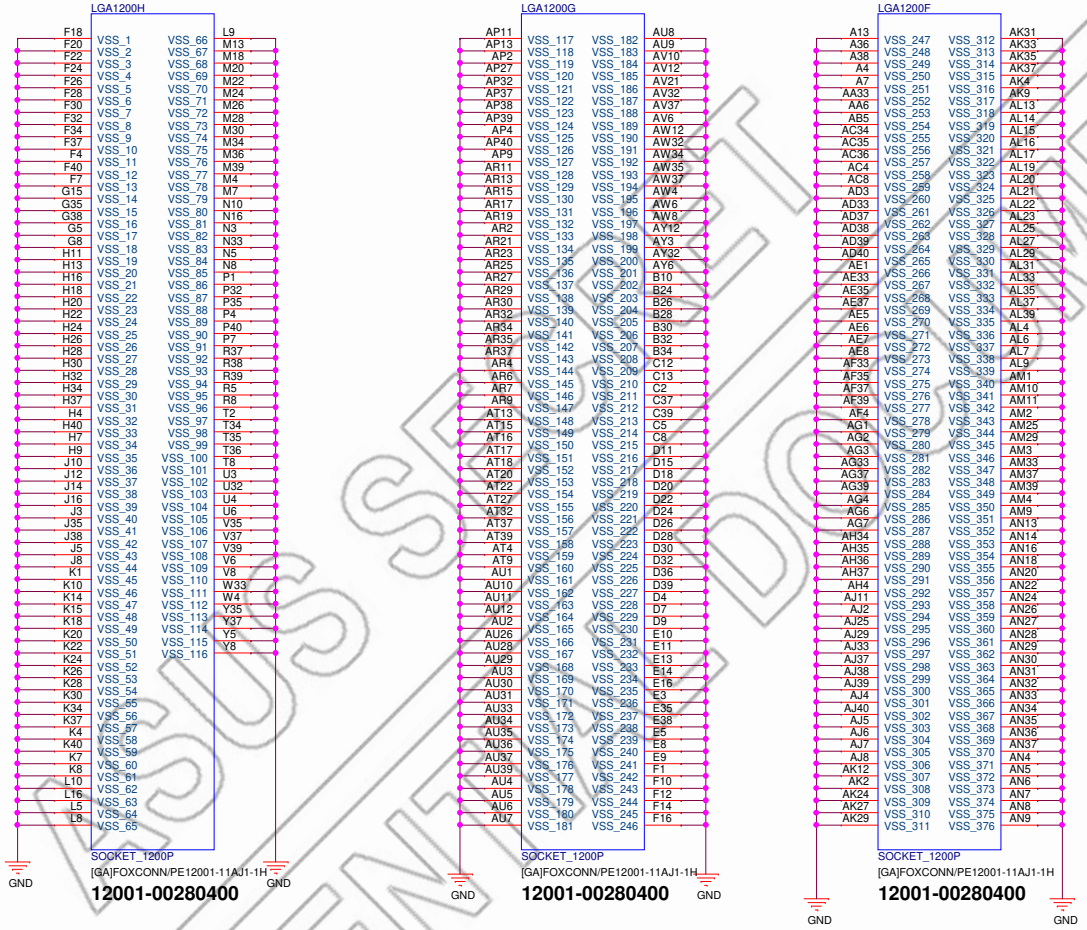


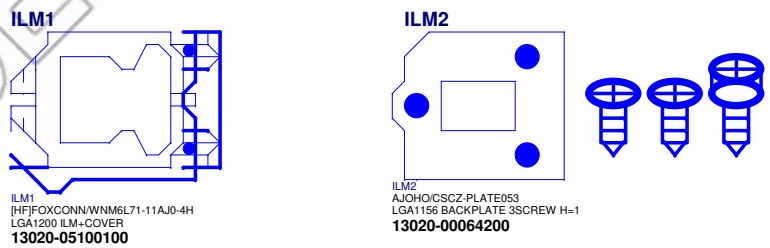
ASUSTek Computer Inc.	Title : LGA1200 (Control)
	Engineer: IPC-EE3
Size: Custom	Project Name: SMS-W480
	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 9 of 86

ASUS SECRET
CONFIDENTIAL DOCUMENT



ASUS SECRET
CONFIDENTIAL DOCUMENT



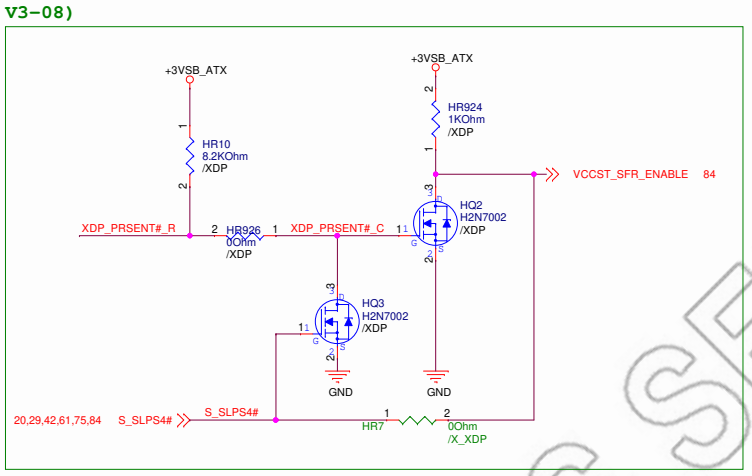


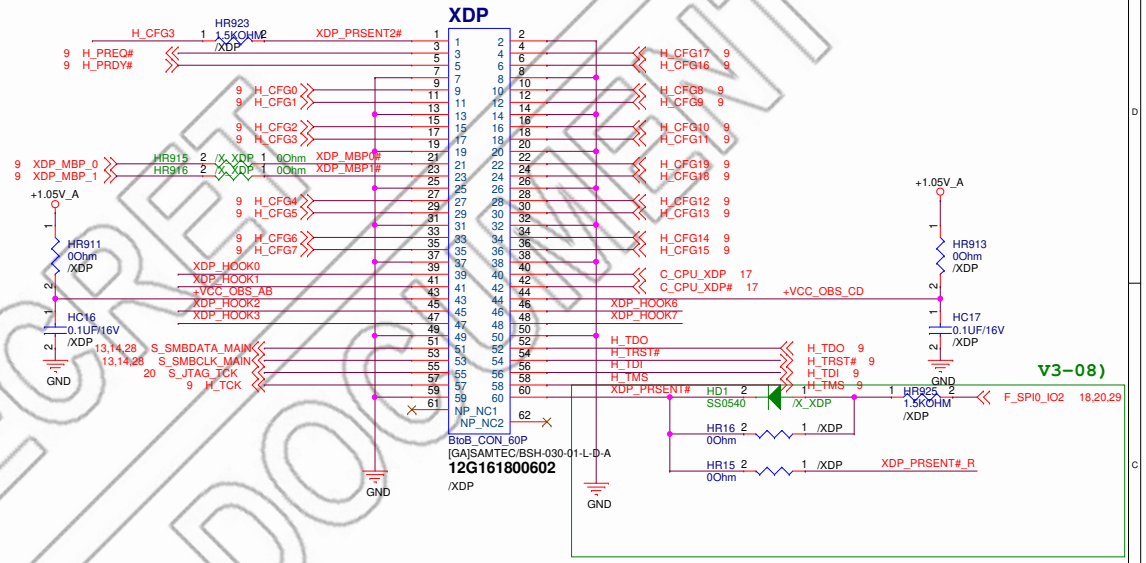
ILM+COVER Module-LGA1200

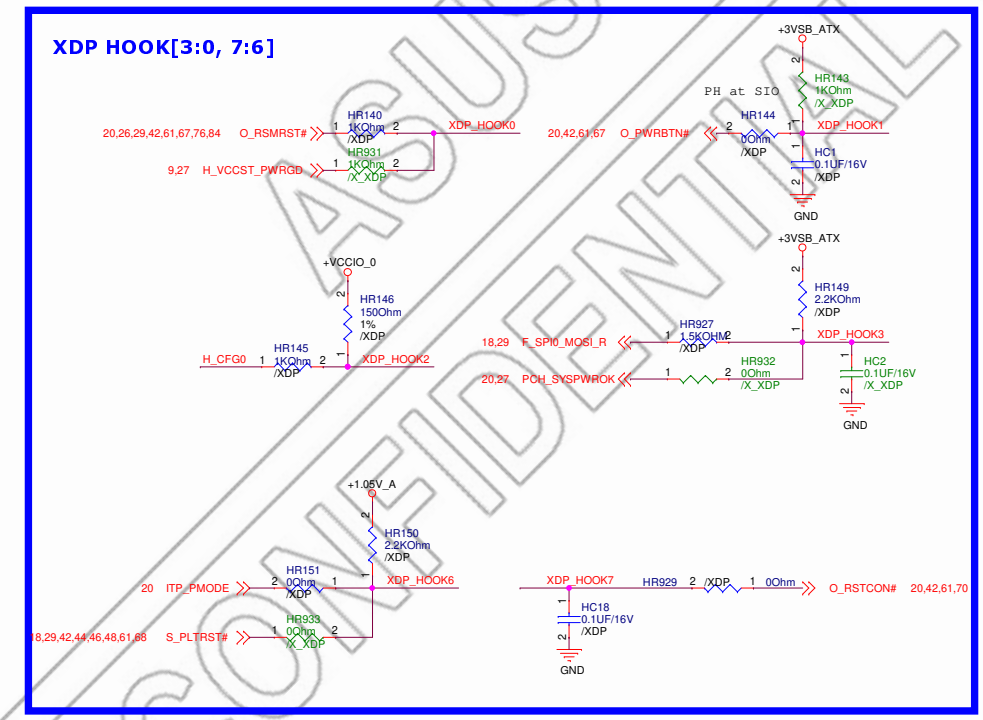
BACKPLATE Module-LGA1200

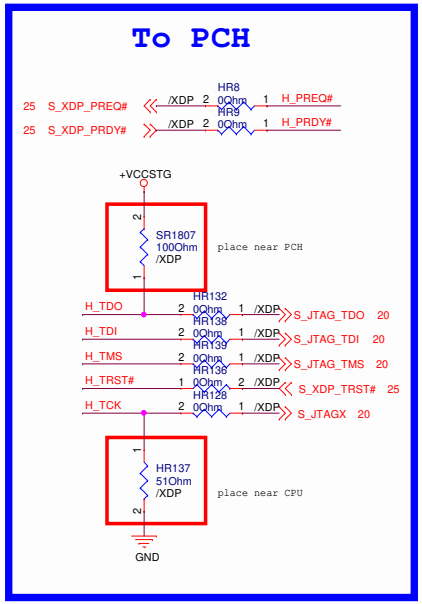
ASUS	Title : LGA1200 (GND)		
ASUSTek Computer Inc.	Engineer: IPC-EE3		
Size A3	Project Name SMS-W480		Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 11 of 86		

CONFIDENTIAL ASUS SECRET DOCUMENT



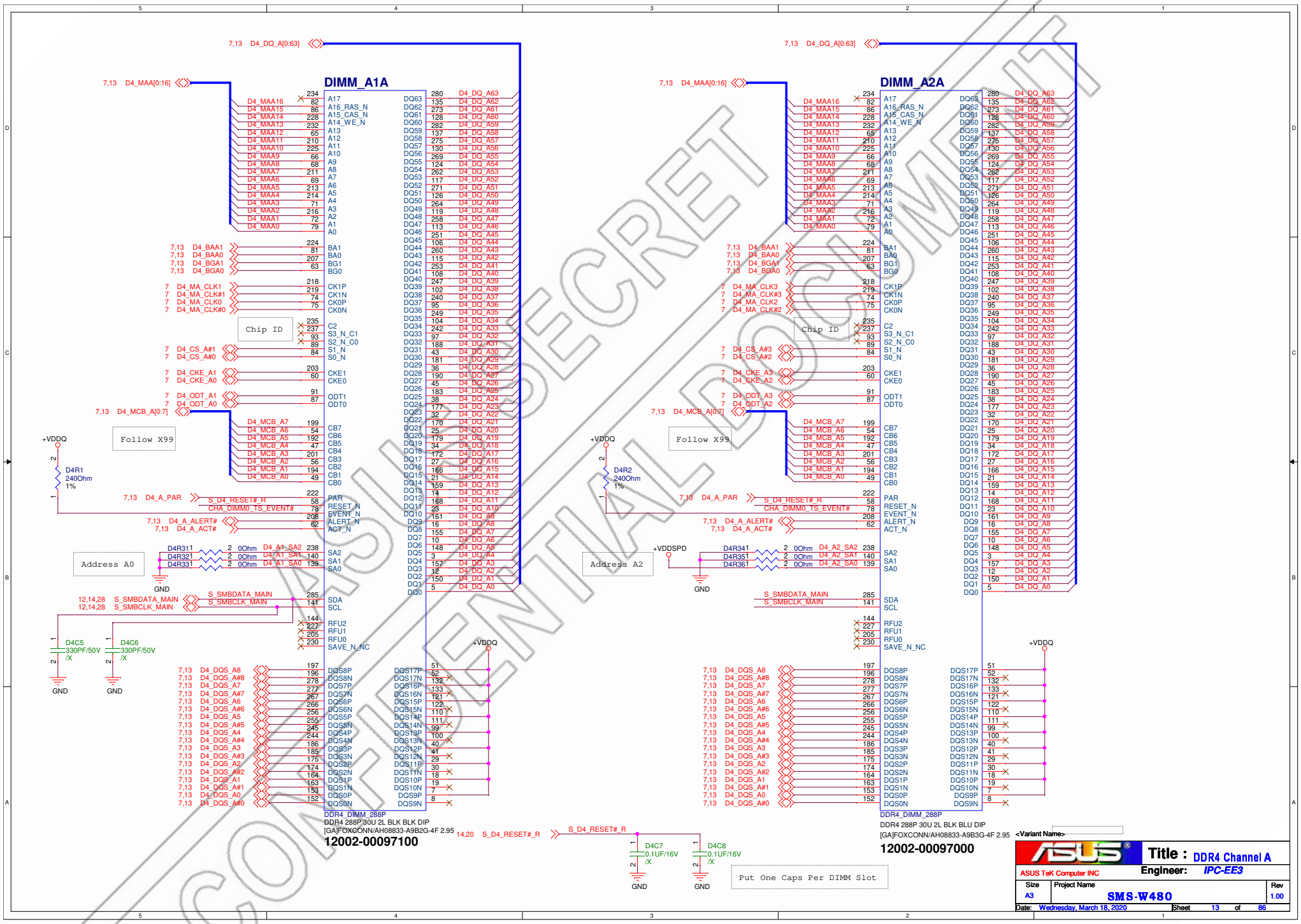






ASUS	Title : LGA1200 (XDP)		
ASUSTek Computer Inc.	Engineer: IPC-EE3		
Size A3	Project Name SMS-W480		Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 12 of 86		

ASUS SECRET
CONFIDENTIAL DOCUMENT



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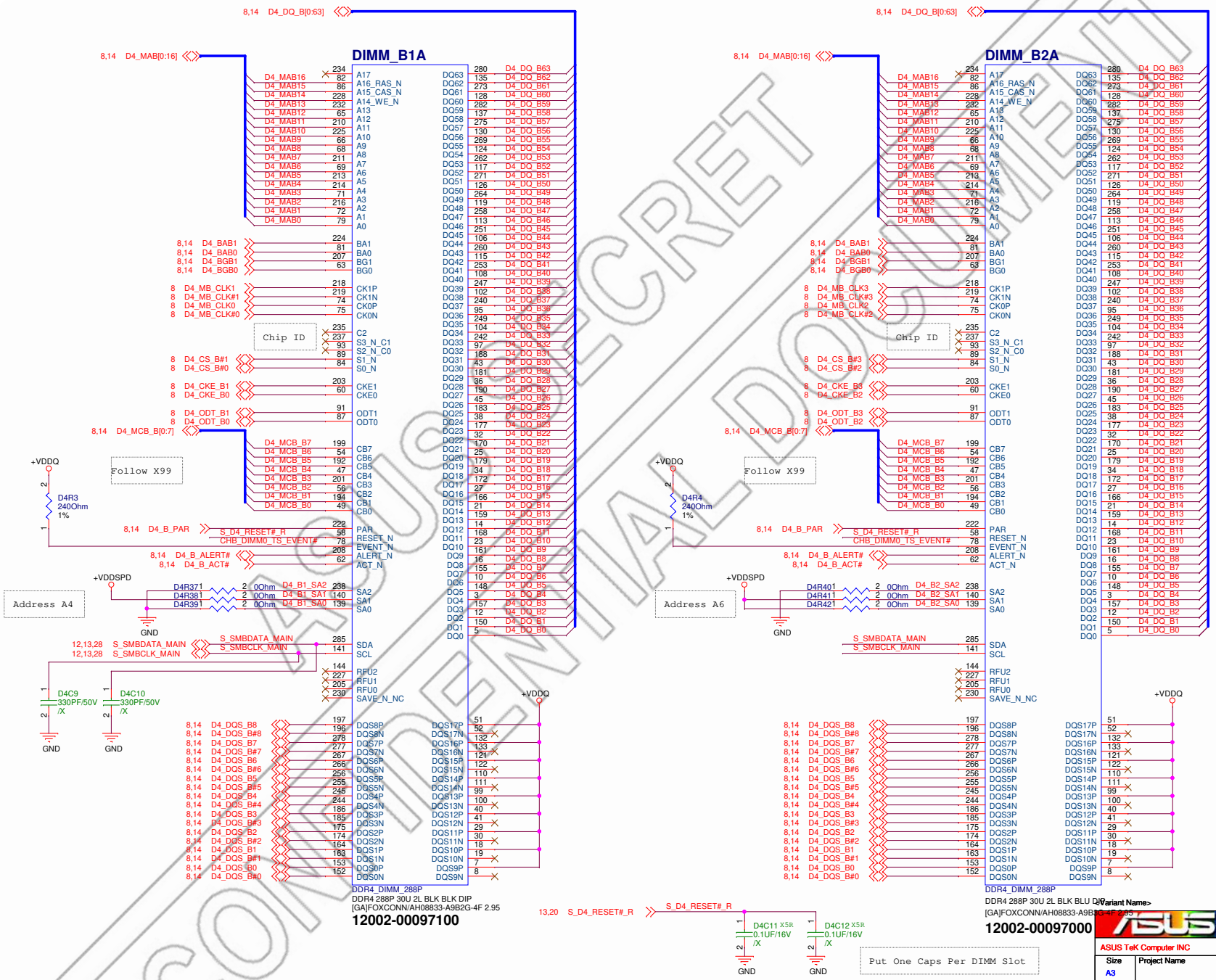
CONFIDENTIAL DOCUMENT



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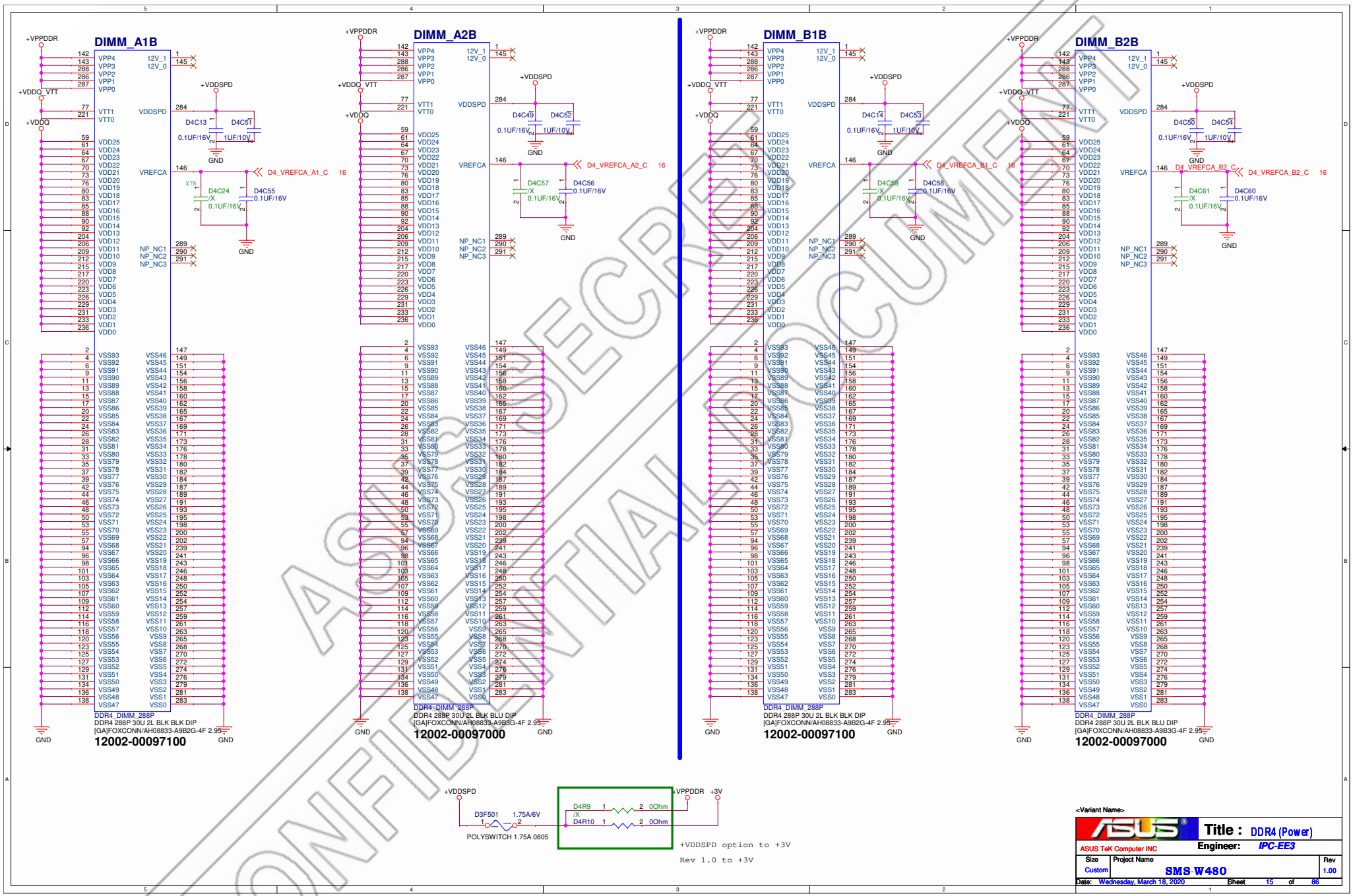
CONFIDENTIAL DOCUMENT



CONFIDENTIAL DOCUMENT
ASUS SECRET

<Variant Name>

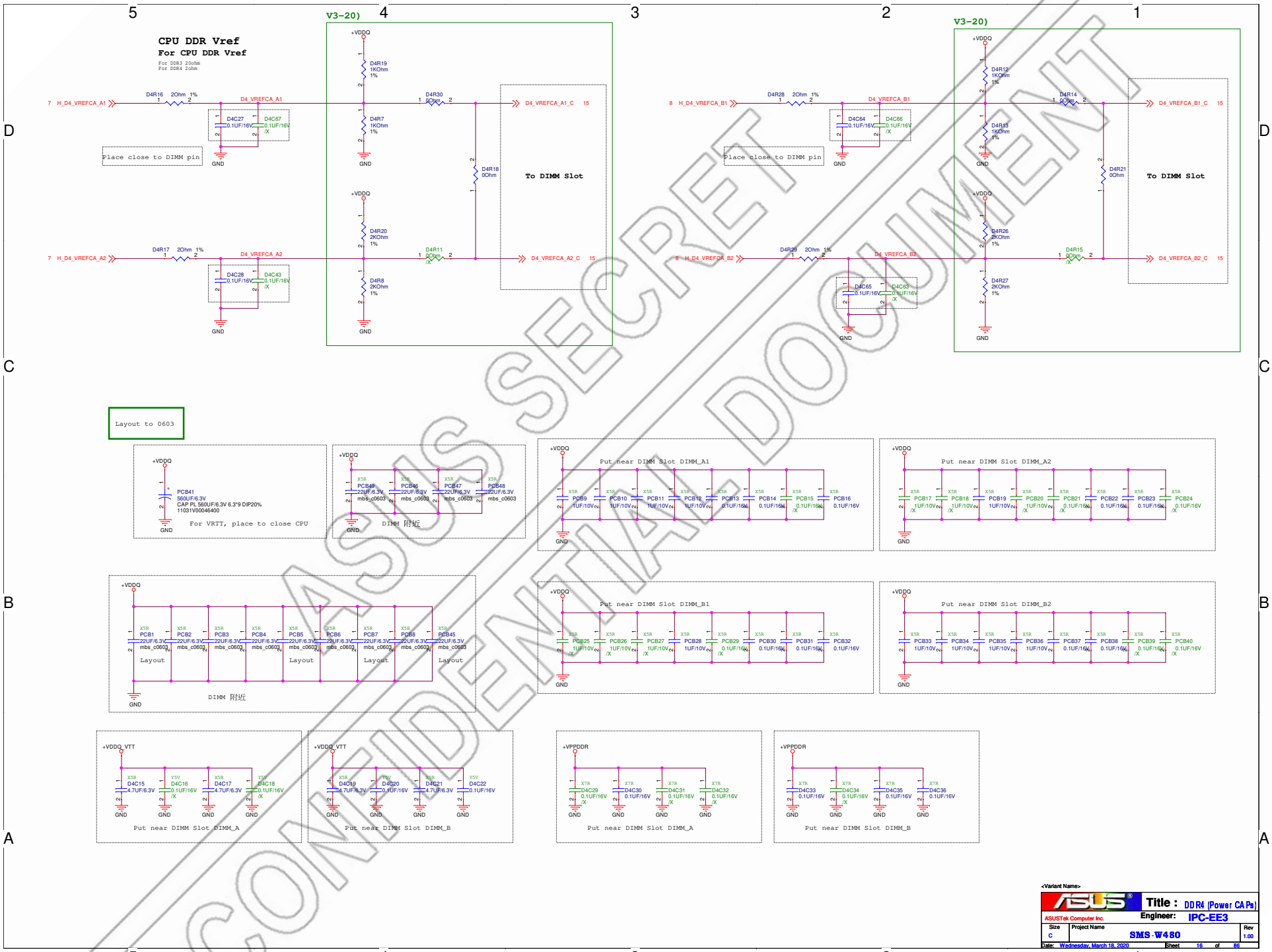
ASUS TeK Computer INC

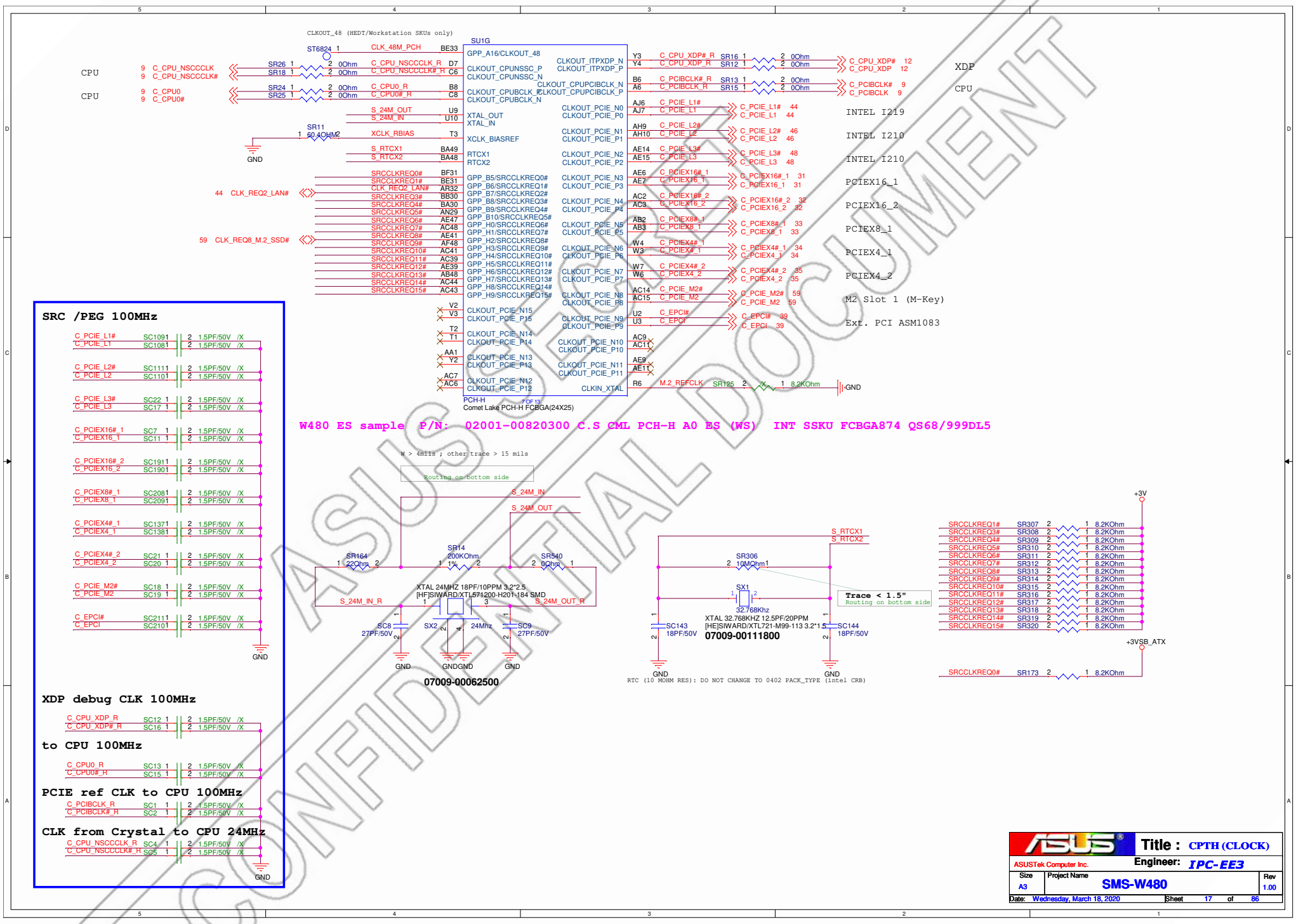
Title : DDR4 (Power)

Engineer: IPC-EE3

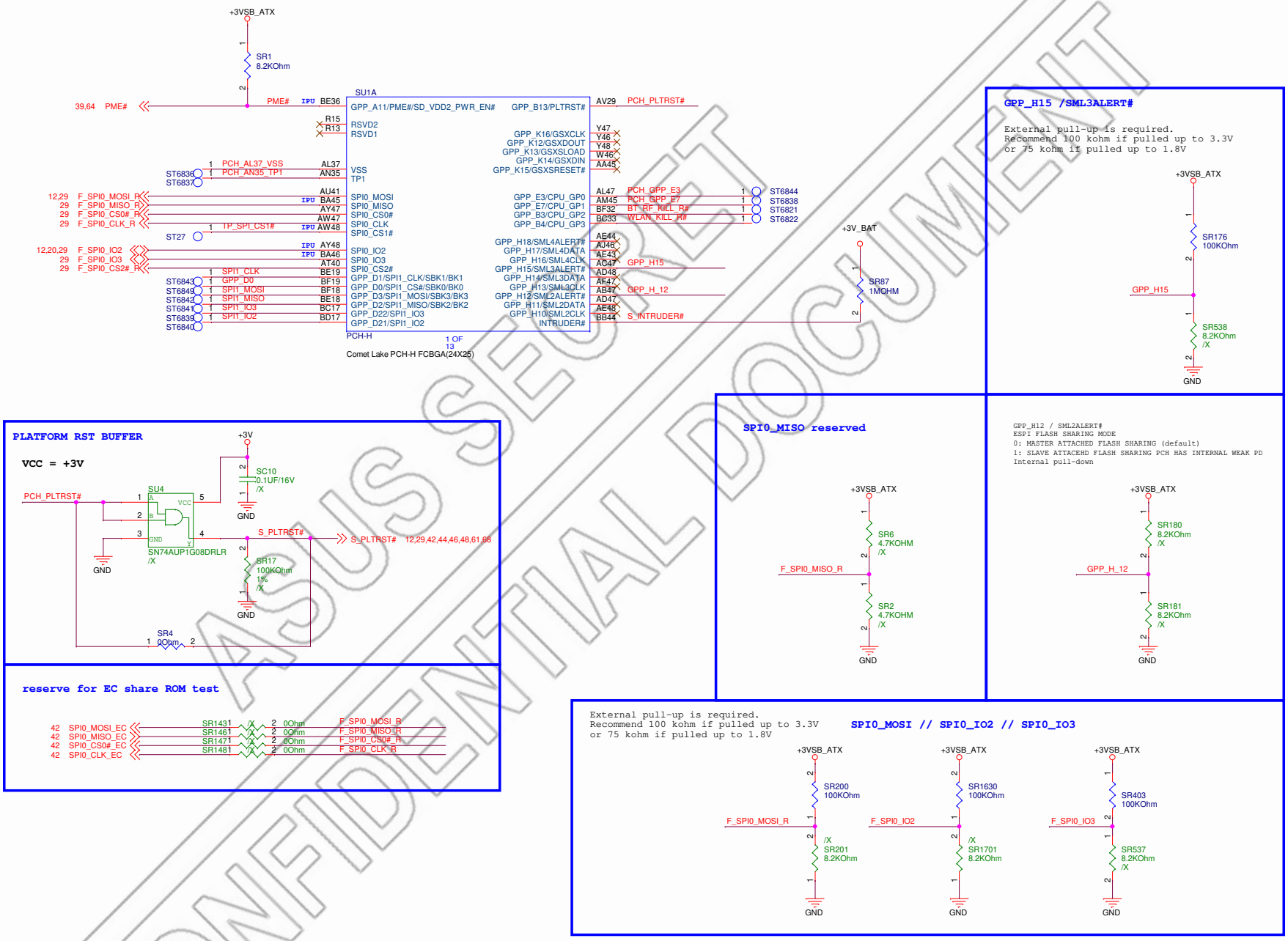
Size	Project Name	Rev
Custom	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 15 of 86


CPU DDR Vref
For CPU DDR Vref
For DDR3 20ohm
For DDR4 2ohm
V3-20)
+VDDQ
D4R19 1KOhm 1%
D4R7 1KOhm 1%
D4R20 2KOhm 1%
D4R8 2KOhm 1%
D4R18 0Ohm
D4R30 0Ohm
D4R11 0Ohm
D4R16 2Ohm 1%
D4R17 2Ohm 1%
D4_VREFCA_A1
D4_VREFCA_A2
D4_VREFCA_A1_C
D4_VREFCA_A2_C
H_D4_VREFCA_A1
H_D4_VREFCA_A2
D4C27 0.1UF/16V
D4C67 0.1UF/16V /X
D4C28 0.1UF/16V
D4C43 0.1UF/16V /X
Place close to DIMM pin
To DIMM Slot
GND
D4R12 1KOhm 1%
D4R13 1KOhm 1%
D4R26 2KOhm 1%
D4R27 2KOhm 1%
D4R21 0Ohm
D4R14 0Ohm
D4R15 0Ohm
D4R28 2Ohm 1%
D4R29 2Ohm 1%
D4_VREFCA_B1
D4_VREFCA_B2
D4_VREFCA_B1_C
D4_VREFCA_B2_C
H_D4_VREFCA_B1
H_D4_VREFCA_B2
D4C64 0.1UF/16V
D4C66 0.1UF/16V /X
D4C65 0.1UF/16V
D4C63 0.1UF/16V /X
Layout to 0603
PCB41 560UF/6.3V
CAP PL 560UF/6.3V 6.3*9 DIP20% 11031V00046400
For VRTT, place to close CPU
PCB45 22UF/6.3V mbs_c0603
DIMM 附近
Put near DIMM Slot DIMM_A1
Put near DIMM Slot DIMM_A2
Put near DIMM Slot DIMM_B1
Put near DIMM Slot DIMM_B2
Layout
+VDDQ_VTT
D4C15 4.7UF/6.3V
D4C16 0.1UF/16V /X
D4C17 4.7UF/6.3V
D4C18 0.1UF/16V /X
D4C19 4.7UF/6.3V
D4C20 0.1UF/16V
D4C21 4.7UF/6.3V
D4C22 0.1UF/16V
Put near DIMM Slot DIMM_A
Put near DIMM Slot DIMM_B
+VPPDDR
D4C29 0.1UF/16V /X
D4C30 0.1UF/16V
D4C31 0.1UF/16V /X
D4C32 0.1UF/16V /X
D4C33 0.1UF/16V
D4C34 0.1UF/16V /X
D4C35 0.1UF/16V
D4C36 0.1UF/16V
Put near DIMM Slot DIMM_A
Put near DIMM Slot DIMM_B
CONFIDENTIAL
ASUS SECRET DOCUMENT
<Variant Name>
ASUSTeK Computer Inc.
Title : DDR4 (Power CAPs)
Engineer:
IPC-EE3
Size C
Project Name SMS-W480
Rev 1.00
Date: Wednesday, March 18, 2020
Sheet 16 of 86

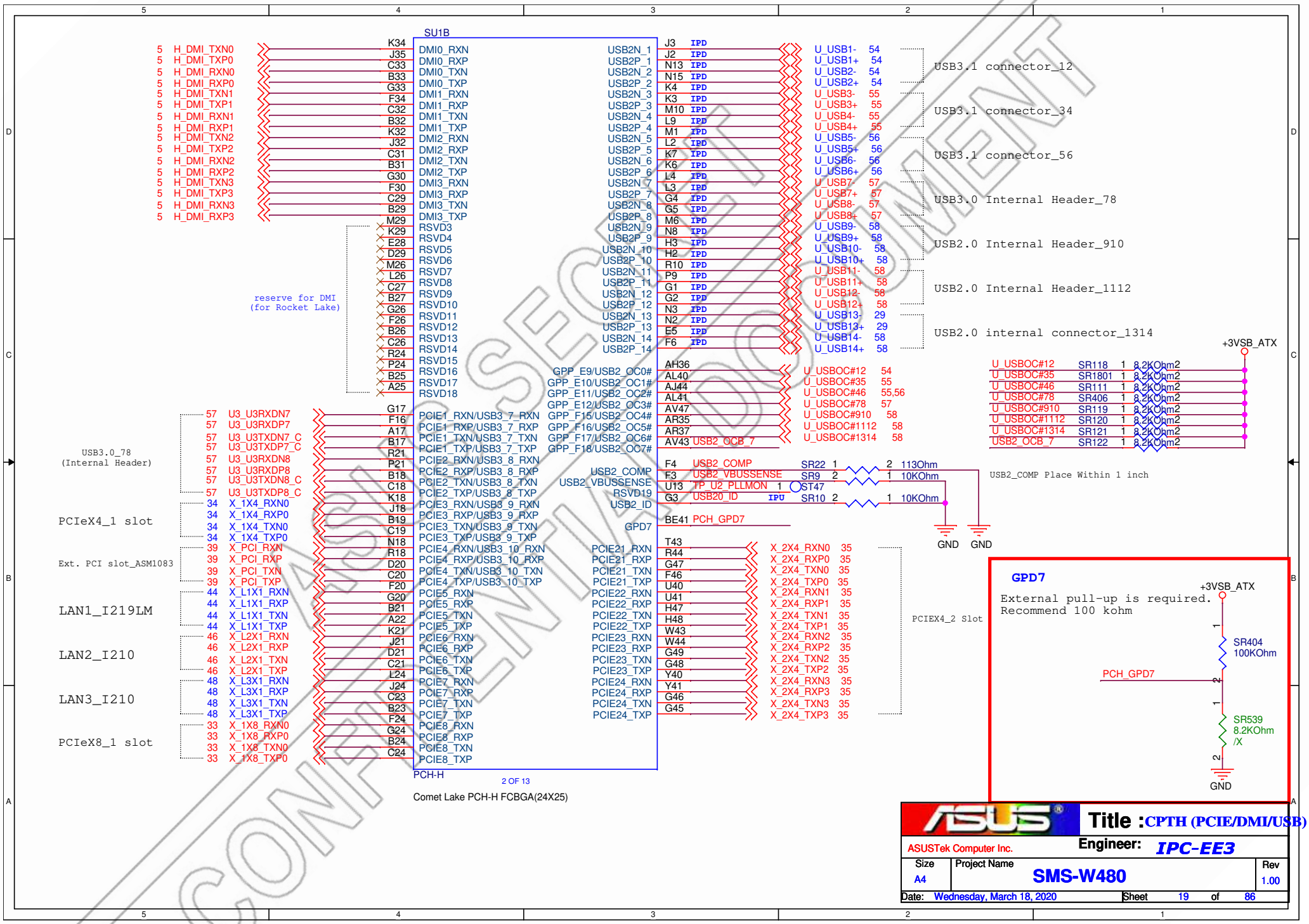


ASUS CONFIDENTIAL DOCUMENT

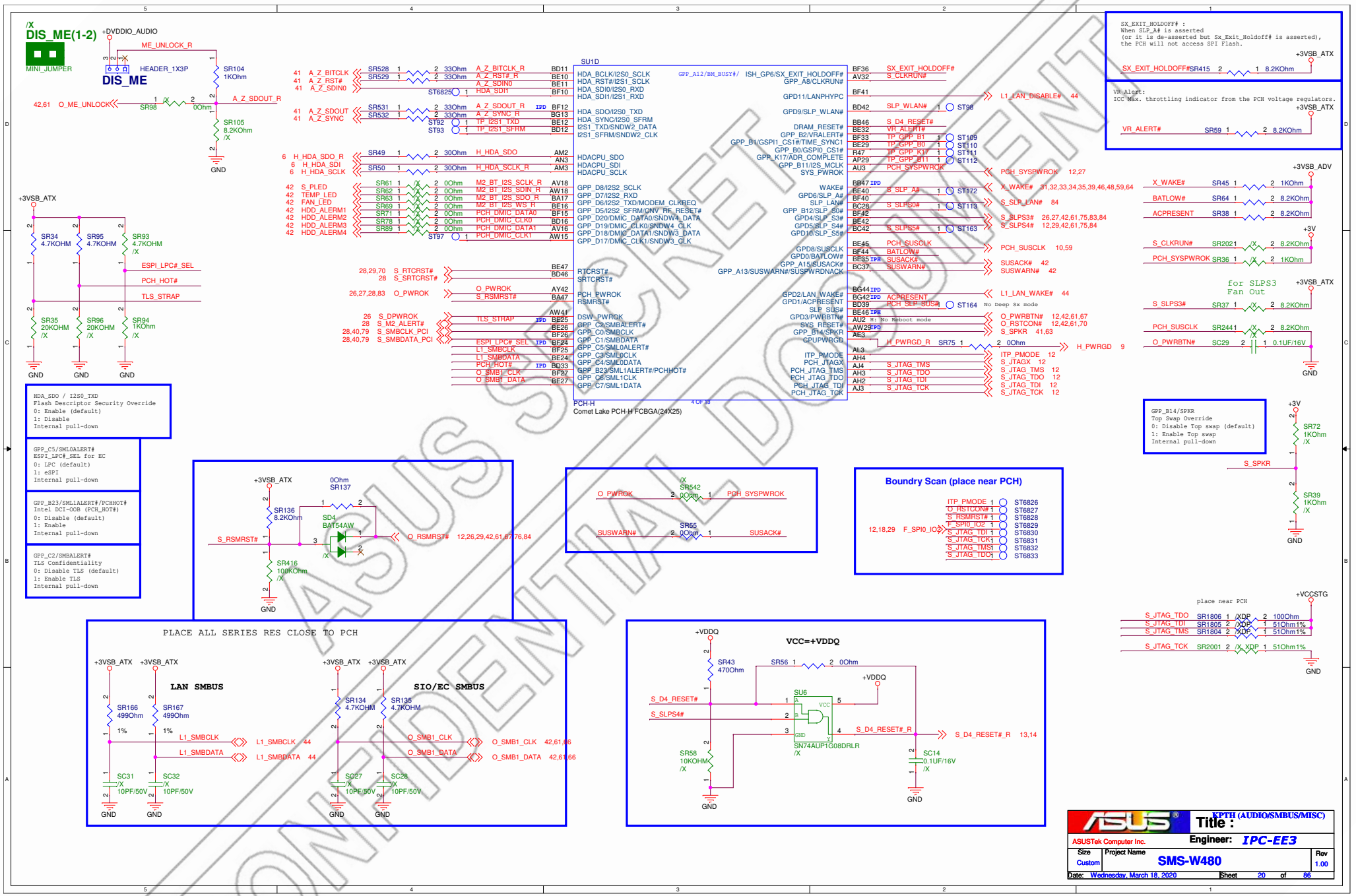


CONFIDENTIAL DOCUMENT
ASUS SECRET

ASUS	Title :	CPTH (PCI/SPI)
ASUSTek Computer Inc.	Engineer:	IPC-EE3
Size: A3	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 18 of 86	

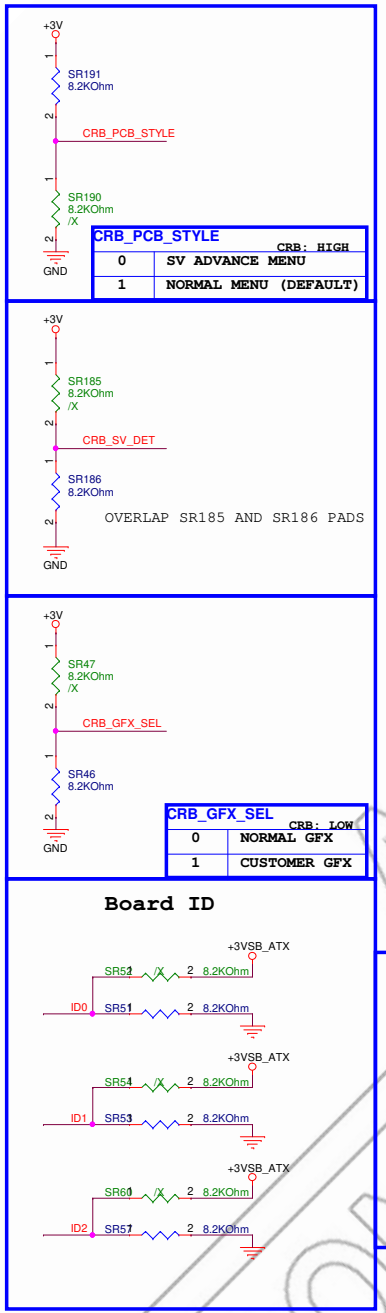


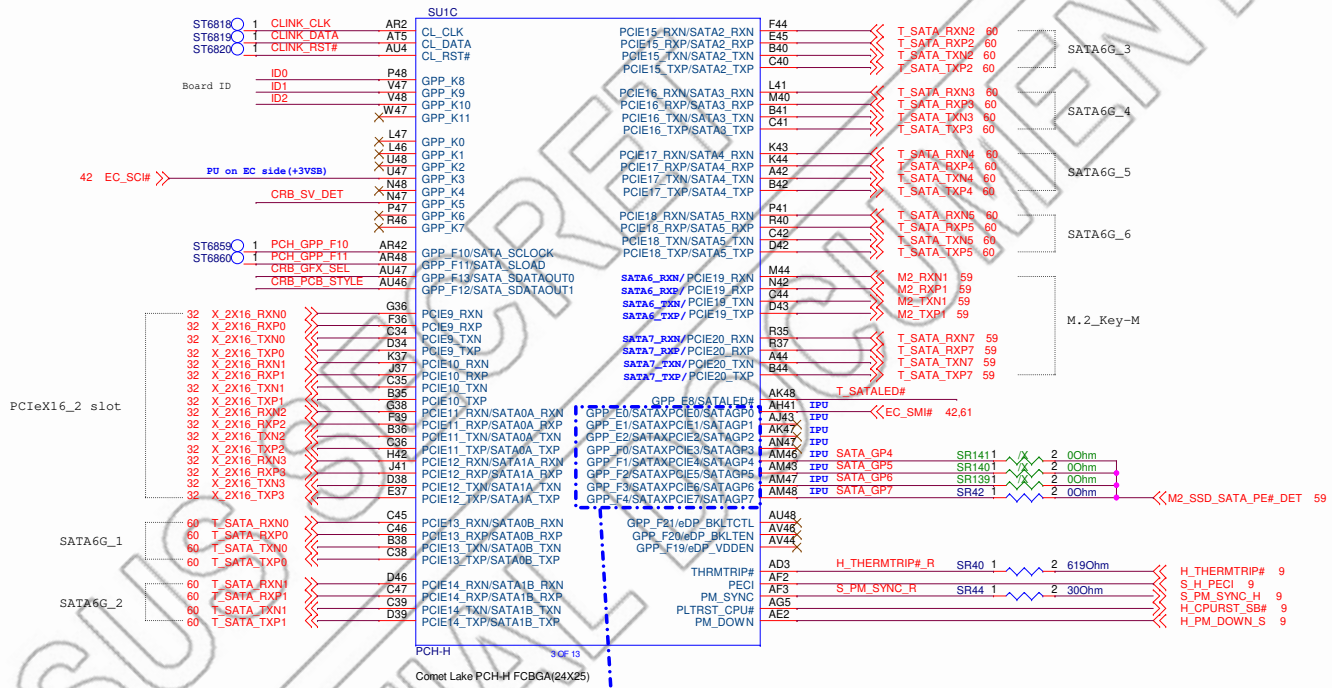
CONFIDENTIAL DOCUMENT



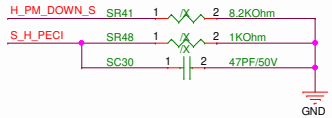
ASUSTek Computer Inc.	Title : KPTH (AUDIO/SMBUS/MISC)
	Engineer: IPC-EE3
Size: Custom	Project Name: SMS-W480
	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 20 of 86

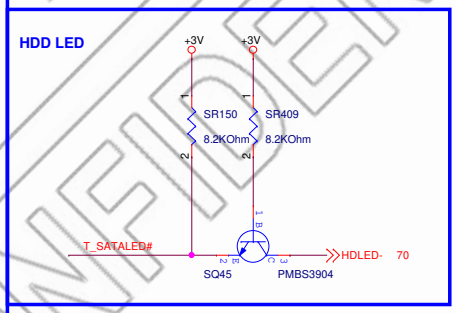
ASUS SECRET
CONFIDENTIAL DOCUMENT





Serial ATA Port [0:7] General Purpose Inputs: When configured as SATAGP[0:7], this is an input pin that is used as an interlock switch status indicator for SATA Port [0:7]. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPIO. Pin defaults to Native mode as SATAXPCIE[0:7] depends on soft-strap.



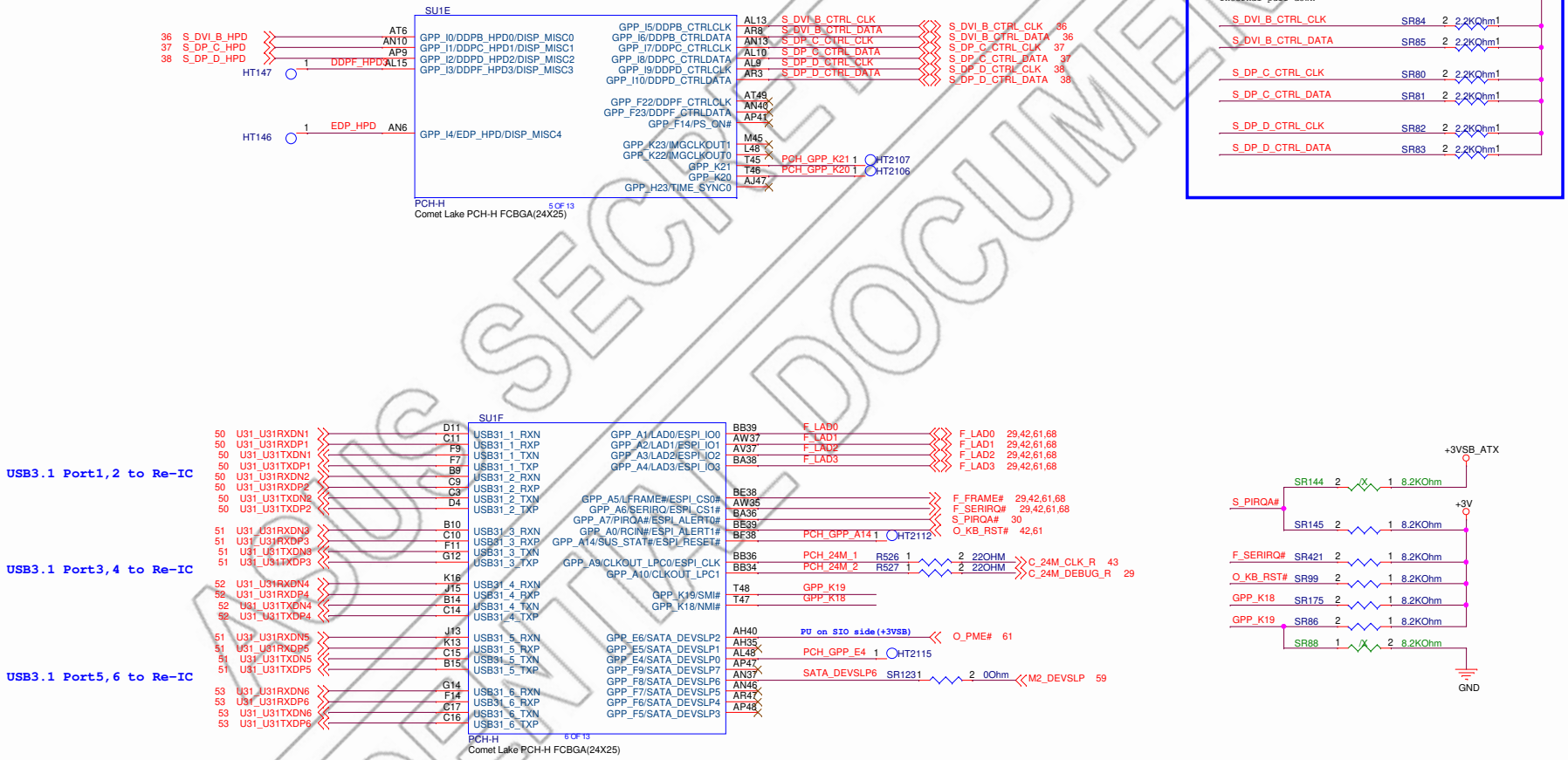


Supported PCH PCI Express* Link Configurations

PCH-H Details	PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4				PCIe* Controller #5				PCIe* Controller #6			
Flex I/O Lane #	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1x4	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
1x4 LR	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
2x2 LR	RP 3		RP 1		RP 7		RP 5		RP 11		RP 9		RP 15		RP 13		RP 19		RP 17		RP 23		RP 21	
1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24

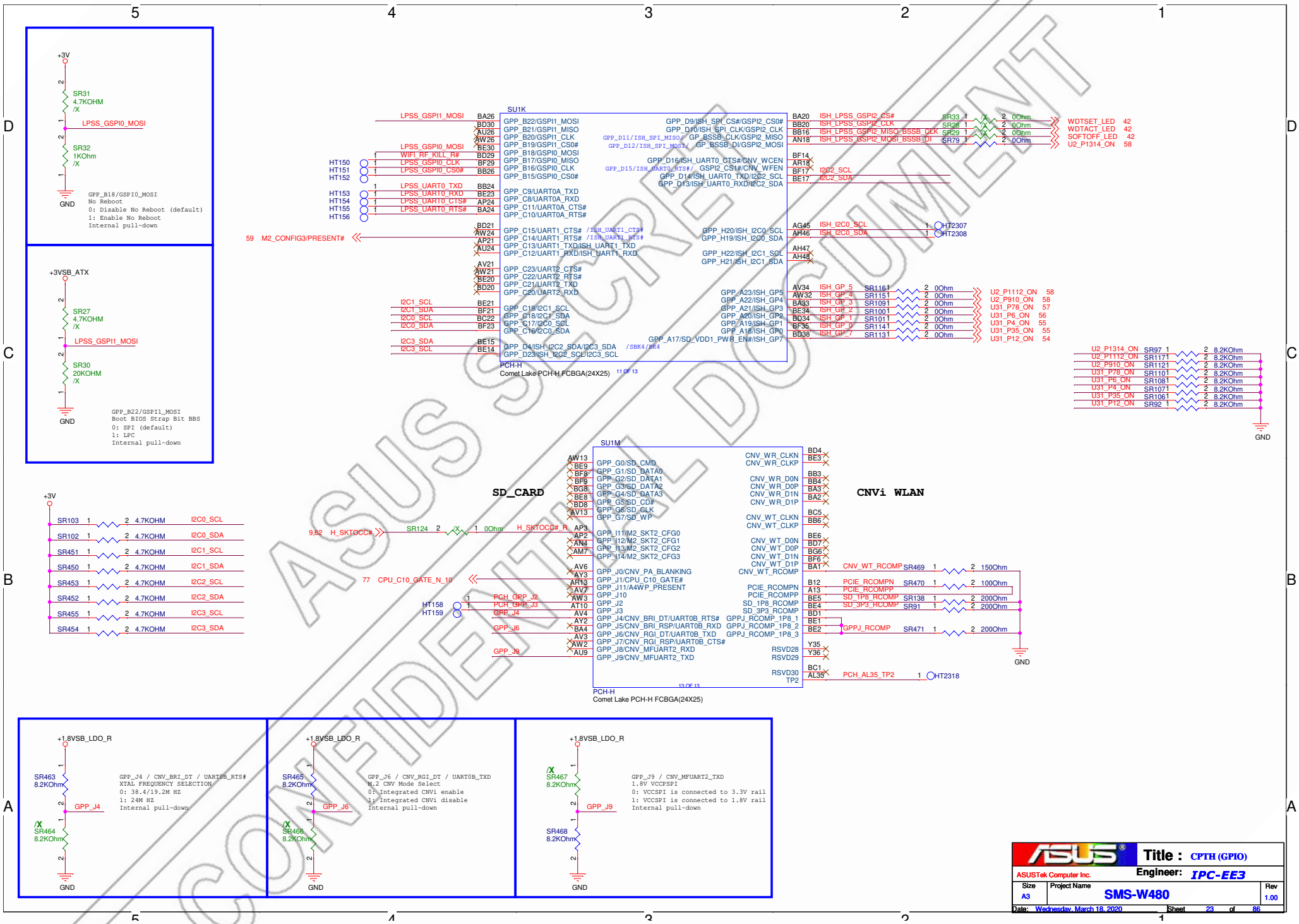
ASUS
ASUSTek Computer Inc.
Title : KPTH (HOST/FAN/SATA)
Engineer: IPC-EE3
Size: Custom
Project Name: SMS-W480
Rev: 1.00
Date: Wednesday, March 18, 2020
Sheet 21 of 86

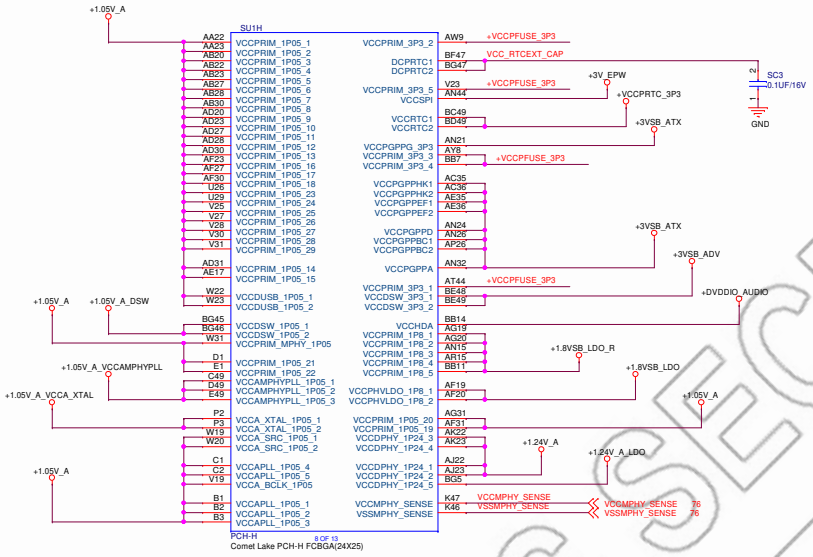
ASUS CONFIDENTIAL DOCUMENT



ASUS	Title : KPTH (DISPLAY/USB3)		
ASUSTek Computer Inc.	Engineer: IPC-EE3		
Size A3	Project Name SMS-W480		Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 22 of 86		

ASUS SECRET DOCUMENT
CONFIDENTIAL

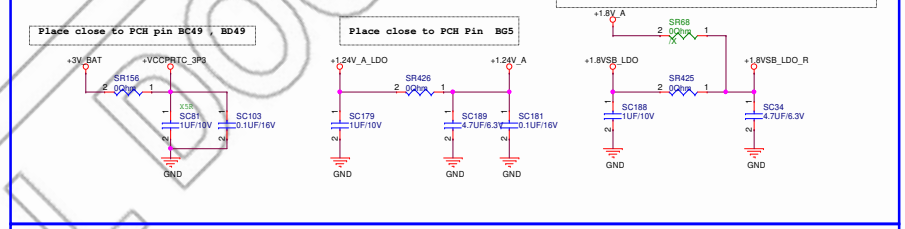

+3V
SR31 4.7KOHM /X
LPSS_GSPI0_MOSI
SR32 1KOhm /X
GND
GPP_B18/GSPI0_MOSI
No Reboot
0: Disable No Reboot (default)
1: Enable No Reboot
Internal pull-down
+3VSB_ATX
SR27 4.7KOHM /X
LPSS_GSPI1_MOSI
SR30 20KOHM /X
GND
GPP_B22/GSPI1_MOSI
Boot BIOS Strap Bit BBS
0: SPI (default)
1: LPC
Internal pull-down
SU1K
PCH-H
Comet Lake PCH-H FCBGA(24X25)
11 OF 13
LPSS_GSPI1_MOSI
LPSS_GSPI0_MOSI
WIFI_RF_KILL_R#
LPSS_GSPI0_CLK
LPSS_GSPI0_CS0#
LPSS_UART0_TXD
LPSS_UART0_RXD
LPSS_UART0_CTS#
LPSS_UART0_RTS#
59 M2_CONFIG3/PRESENT#
I2C1_SCL
I2C1_SDA
I2C0_SCL
I2C0_SDA
I2C3_SDA
I2C3_SCL
ISH_LPSS_GSPI2_CS#
ISH_LPSS_GSPI2_CLK
ISH_LPSS_GSPI2_MISO_BSSB_CLK
ISH_LPSS_GSPI2_MOSI_BSSB_DI
WDTSET_LED 42
WDTACT_LED 42
SOFTOFF_LED 42
U2_P1314_ON 58
I2C2_SCL
I2C2_SDA
ISH_I2C0_SCL
ISH_I2C0_SDA
HT2307
HT2308
ISH_GP_5
ISH_GP_4
ISH_GP_3
ISH_GP_2
ISH_GP_1
ISH_GP_0
ISH_GP_7
U2_P1112_ ON 58
U2_P910_ ON 58
U31_P78_ ON 57
U31_P6_ ON 56
U31_P4_ ON 55
U31_P35_ ON 55
U31_P12_ ON 54
U2_P1314_ ON SR97 8.2KOhm
U2_P1112_ ON SR1171 8.2KOhm
U2_P910_ ON SR1121 8.2KOhm
U31_P78_ ON SR1101 8.2KOhm
U31_P6_ ON SR1081 8.2KOhm
U31_P4_ ON SR1071 8.2KOhm
U31_P35_ ON SR1061 8.2KOhm
U31_P12_ ON SR92 8.2KOhm
GND
+3V
SR103 4.7KOHM I2C0_SCL
SR102 4.7KOHM I2C0_SDA
SR451 4.7KOHM I2C1_SCL
SR450 4.7KOHM I2C1_SDA
SR453 4.7KOHM I2C2_SCL
SR452 4.7KOHM I2C2_SDA
SR455 4.7KOHM I2C3_SCL
SR454 4.7KOHM I2C3_SDA
SU1M
SD_CARD
CNVi WLAN
9,62 H_SKTOCC#
SR124 0Ohm
H_SKTOCC# R
77 CPU_C10_GATE_N_10
HT158
HT159
PCH_GPP_J2
PCH_GPP_J3
GPP_J4
GPP_J6
GPP_J9
CNV_WT_RCOMP SR469 150Ohm
PCIE_RCOMPN SR470 100Ohm
SD_1P8_RCOMP SR138 200Ohm
SD_3P3_RCOMP SR91 200Ohm
GPPJ_RCOMP SR471 200Ohm
PCH_AL35_TP2 HT2318
PCH-H
Comet Lake PCH-H FCBGA(24X25)
13 OF 13
+1.8VSB_LDO_R
SR463 8.2KOhm
GPP_J4
/X SR464 8.2KOhm
GND
GPP_J4 / CNV_BRI_DT / UART0B_RTS#
XTAL FREQUENCY SELECTION
0: 38.4/19.2M HZ
1: 24M HZ
Internal pull-down
+1.8VSB_LDO_R
SR465 8.2KOhm
GPP_J6
/X SR466 8.2KOhm
GND
GPP_J6 / CNV_RGI_DT / UART0B_TXD
M.2 CNV Mode Select
0: Integrated CNVi enable
1: Integrated CNVi disable
Internal pull-down
+1.8VSB_LDO_R
/X SR467 8.2KOhm
GPP_J9
SR468 8.2KOhm
GND
GPP_J9 / CNV_MFUART2_TXD
1.8V VCCPSPI
0: VCCSPI is connected to 3.3V rail
1: VCCSPI is connected to 1.8V rail
Internal pull-down
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUSTek Computer Inc.
Title : CPTH (GPIO)
Engineer: IPC-EE3
Size A3
Project Name SMS-W480
Rev 1.00
Date: Wednesday, March 18, 2020
Sheet 23 of 86



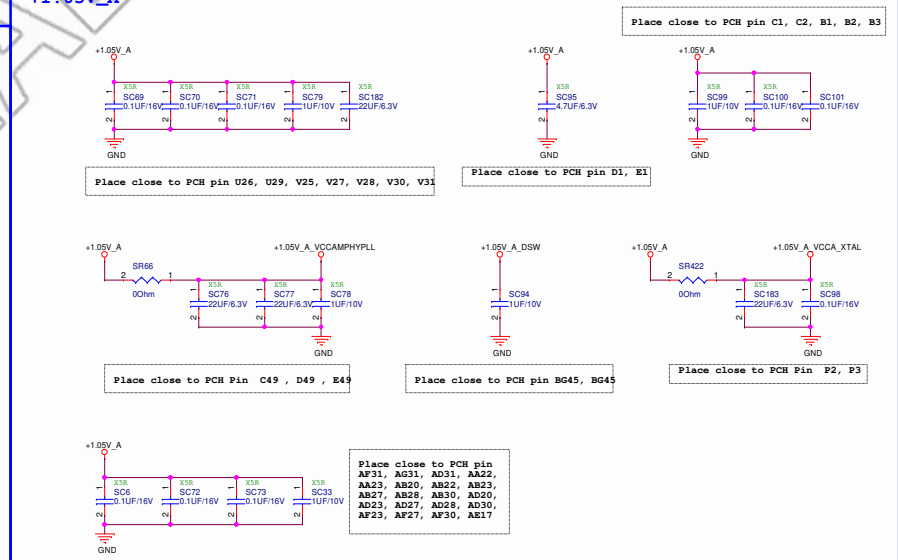
GPIO Voltage Level

Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+3VSB_ATX
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSB_ATX
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSB_ATX
GPP_D	VCCPGPPD	1.8V or 3.3V	+3VSB_ATX
GPP_E	VCCPGPPEF	1.8V or 3.3V	+3VSB_ATX
GPP_F	VCCPGPPEF	1.8V or 3.3V	+3VSB_ATX
GPP_G	VCCPGPPG_3P3 VCCPRIM_1P8	Dynamic voltage to be config SDIO	+3VSB_ATX +1.8V_A
GPP_H	VCCPGPPHK	1.8V or 3.3V	+3VSB_ATX
GPP_I	VCCPRIM_3P3	3.3V Only	+3VSB_ATX
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPP_K	VCCPGPPHK	1.8V or 3.3V	+3VSB_ATX
GPD	VCCDSW_3P3	3.3V Only	+3VSB_ATX

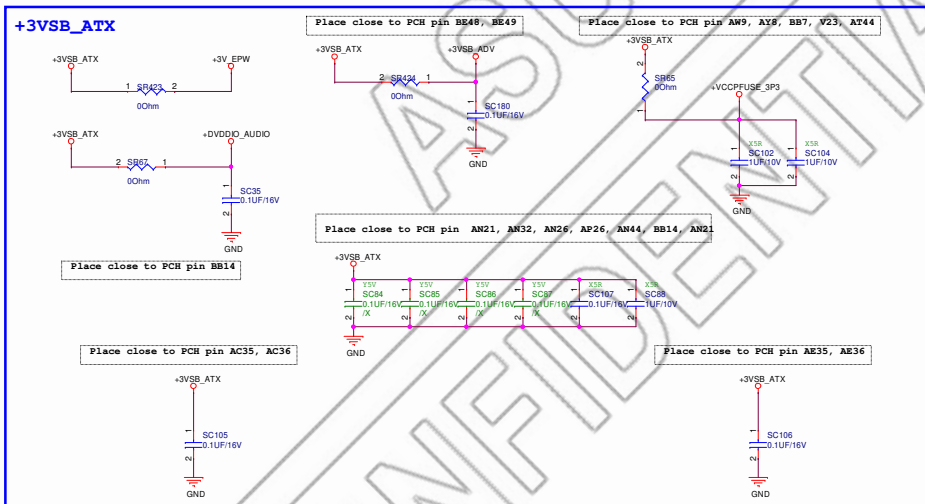
Other Power



+1.05V_A



+3VSB_ATX



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ASUS SECRET

ASUS

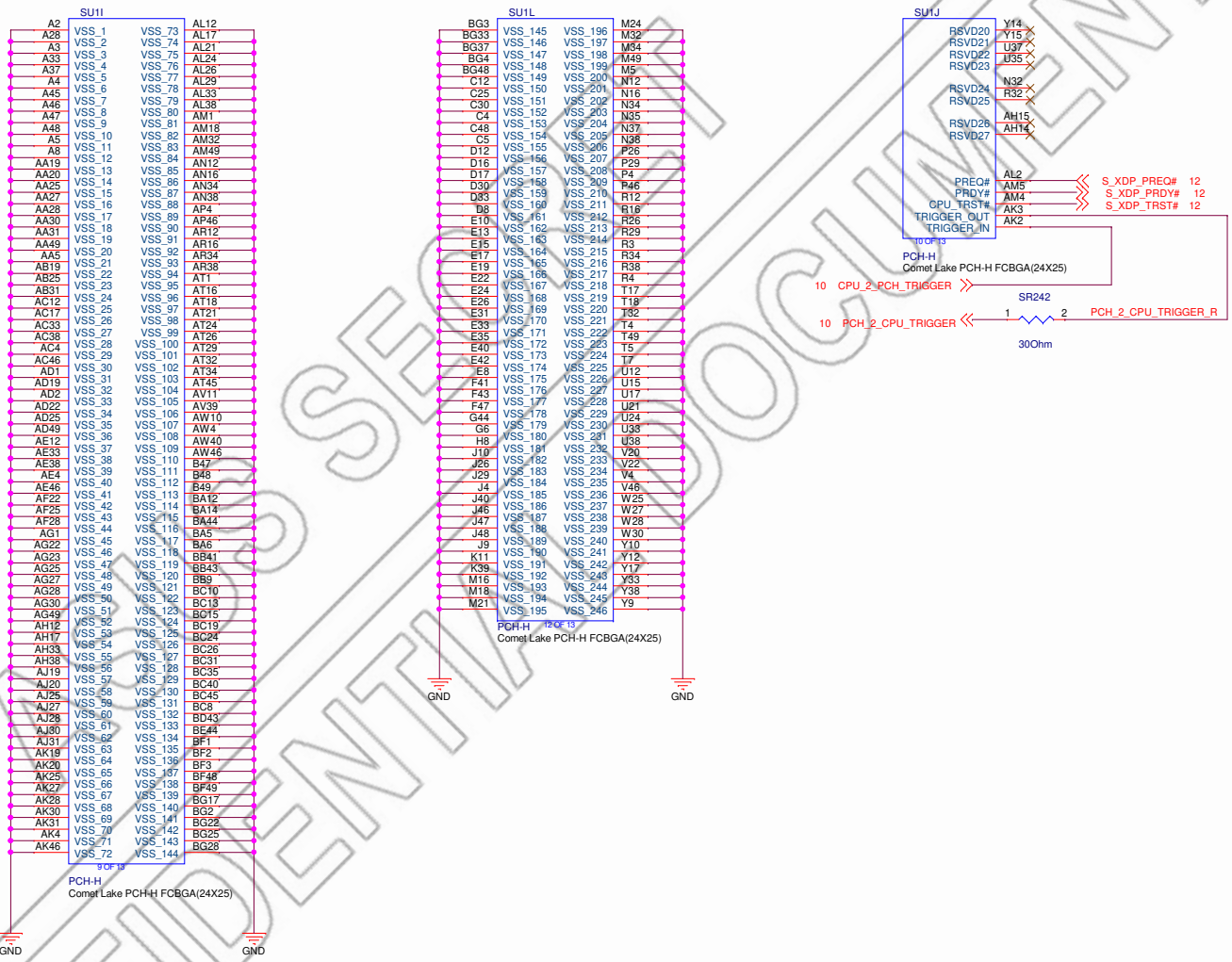
Title : KPTH (POWER)

ASUSTek Computer Inc.

Engineer: IPC-EE3

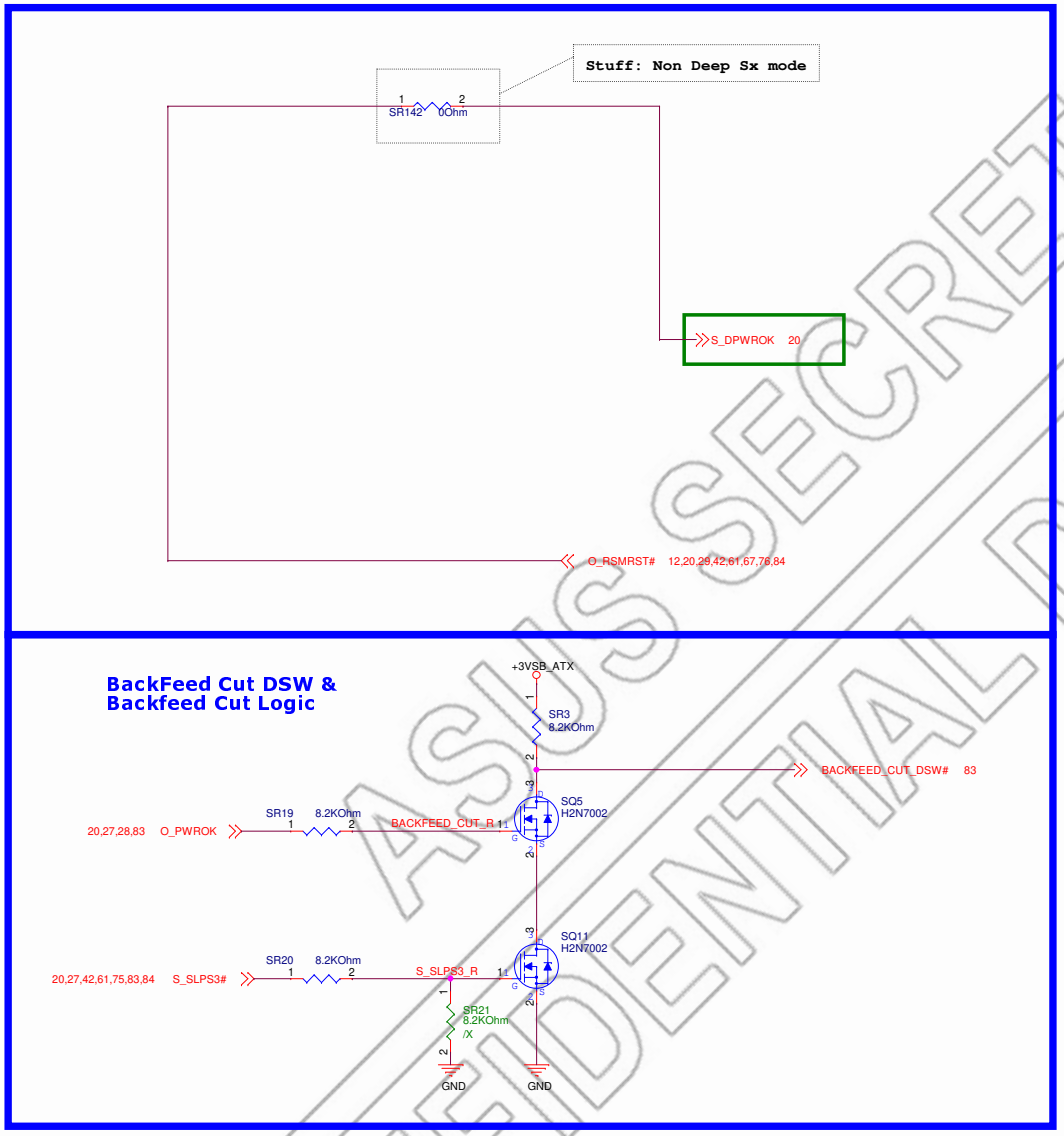
Size	Project Name	Rev
C	SMS-W480	1.00

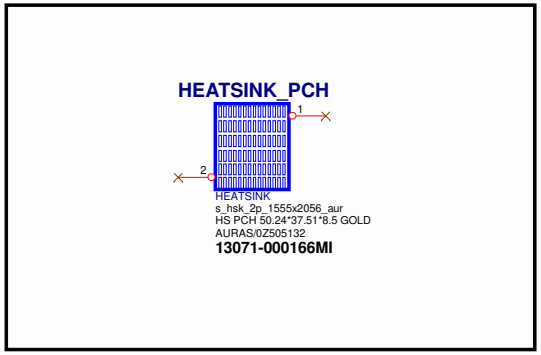
Date: Wednesday, March 18, 2020 Sheet 24 of 86



CONFIDENTIAL DOCUMENT

ASUS	Title :	CPTH (GND)
ASUSTek Computer Inc.	Engineer:	IPC-EE3
Size: A3	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 25 of 86	

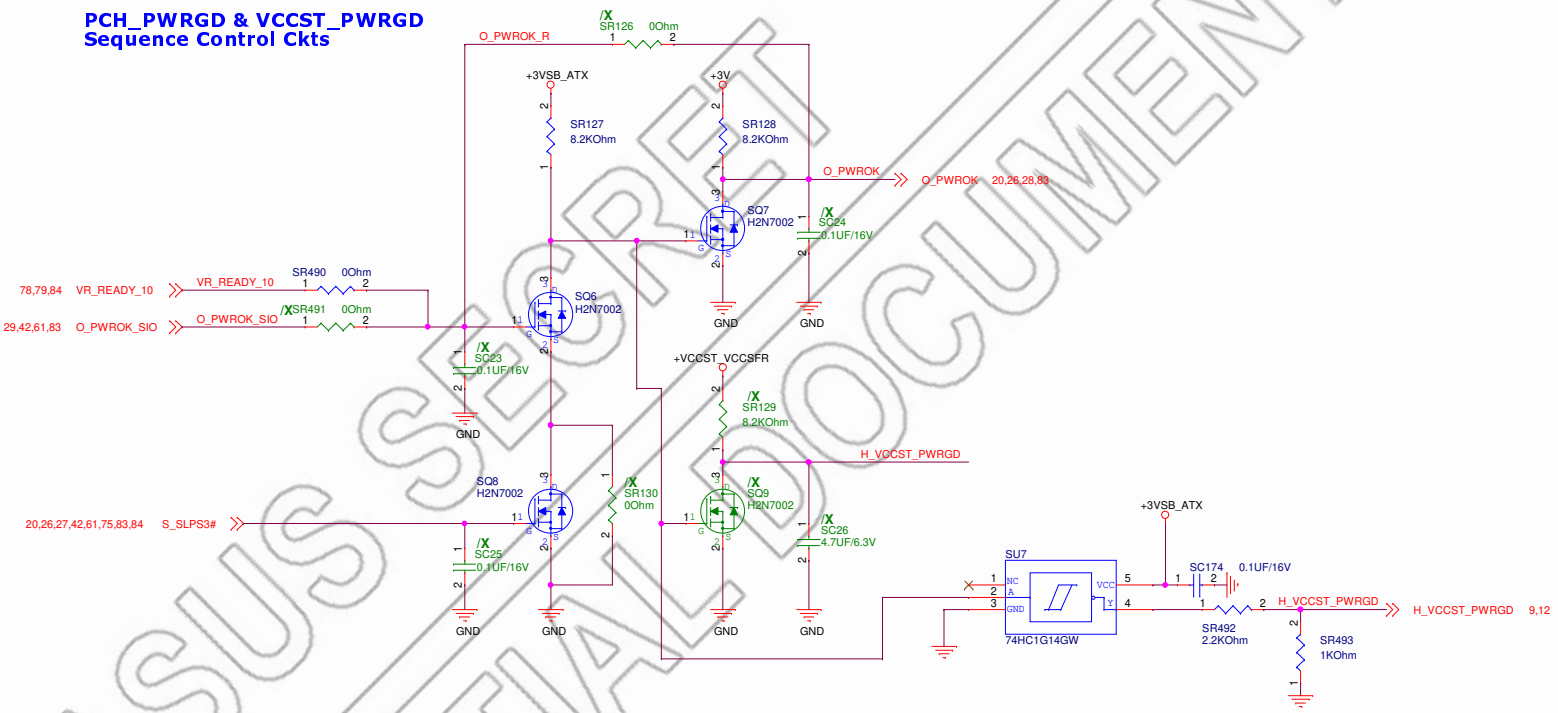




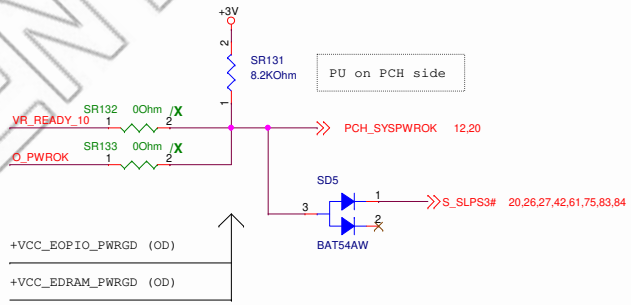
ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : CPTH (DSW SEQUENCE)	
ASUSTek Computer Inc.	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 26 of 86	

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

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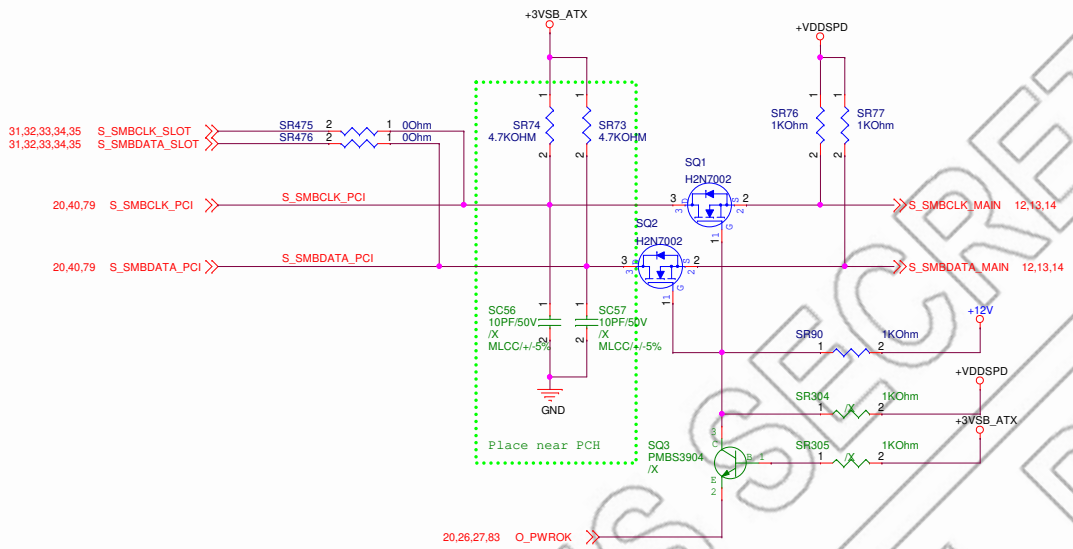
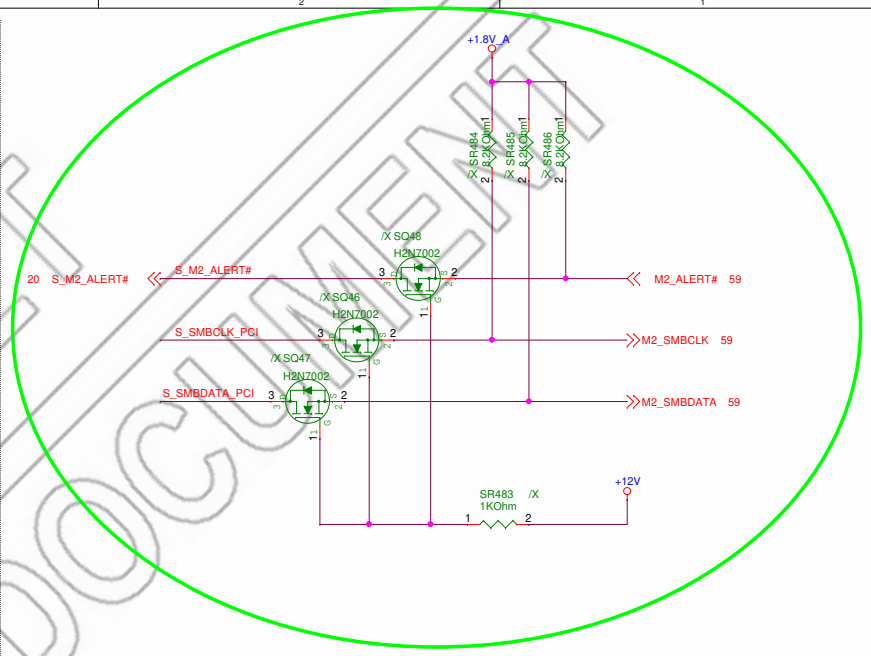
ASUS	Title : CFTH (PCH/SYS/PROC_PWROK)	
ASUSTek Computer Inc.	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 27 of 86	



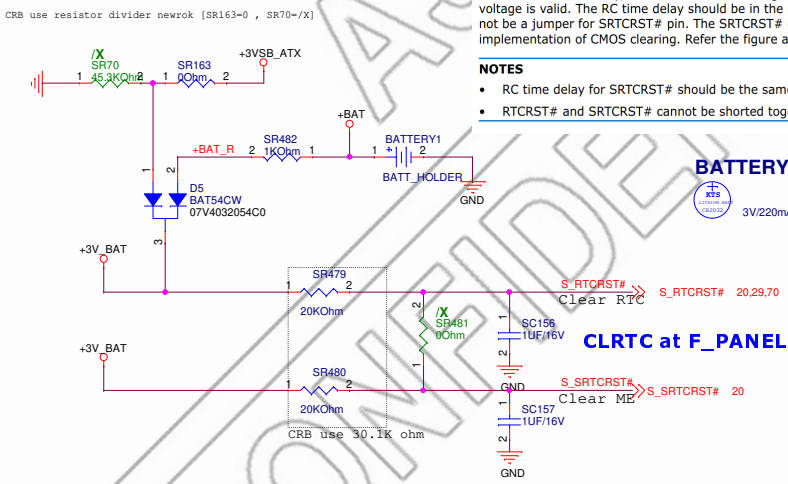


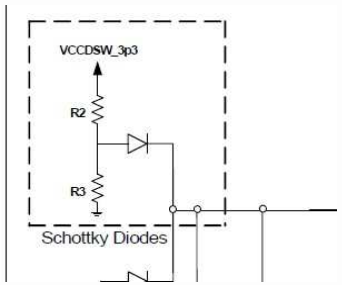
RTC External SRTCRST# Circuit

The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18~25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer the figure above external circuit for PCH RTC.

NOTES

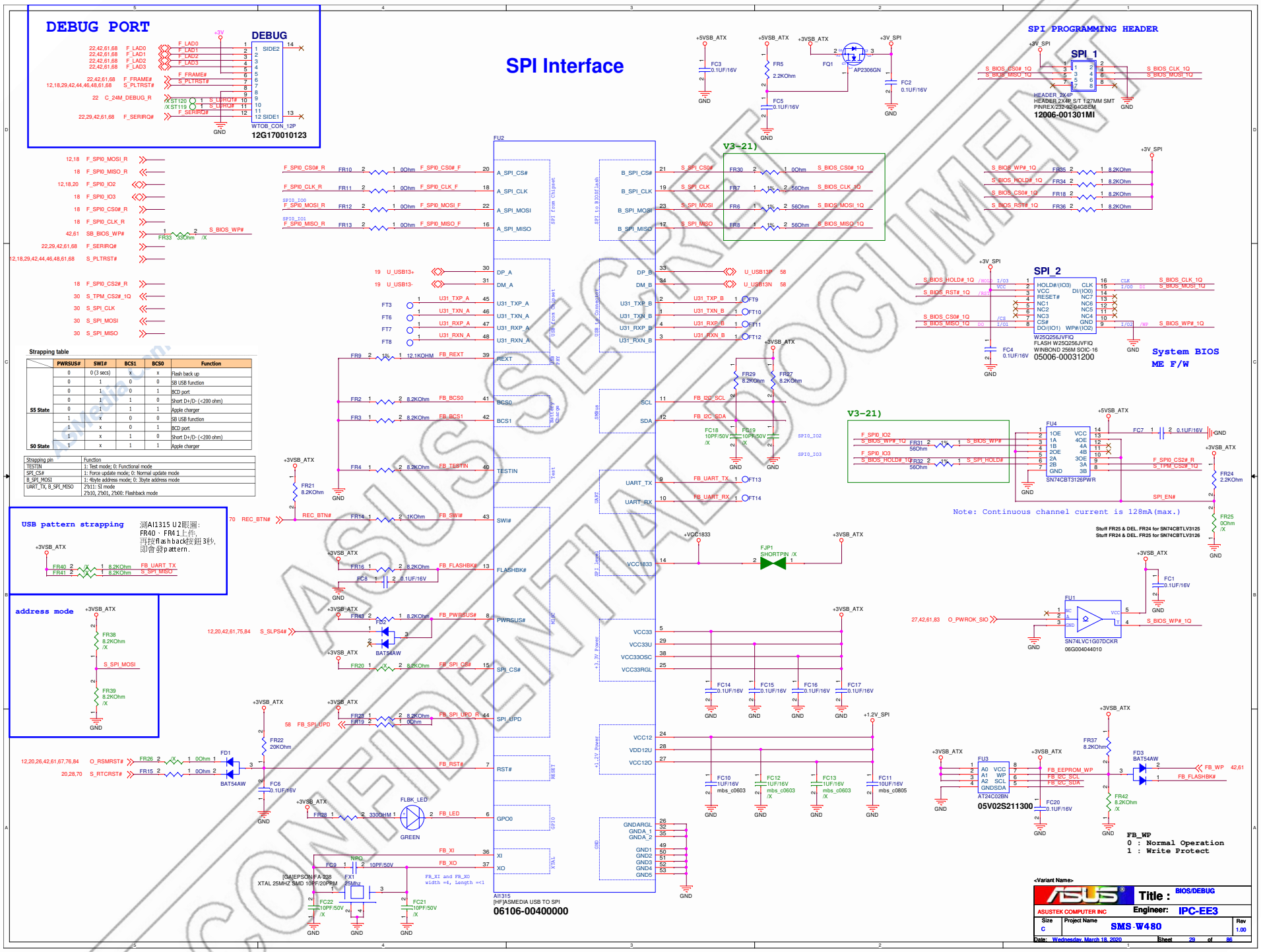
- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.





ASUS SECRET
CONFIDENTIAL DOCUMENT

ASUS	Title : CPTH (SMBUS/CLRTC)	
ASUSTek Computer Inc.	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 28 of 86	



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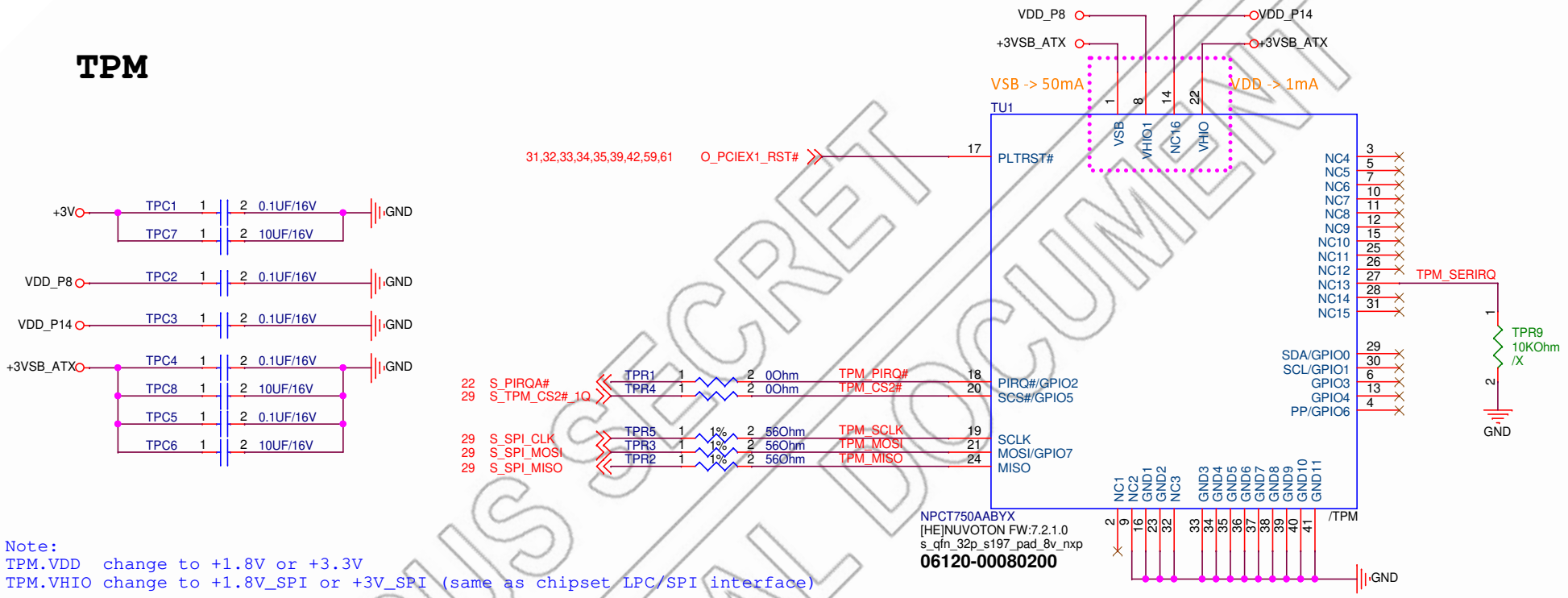
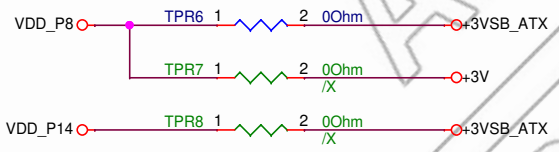
CONFIDENTIAL DOCUMENT

TPM



Note:
TPM.VDD change to +1.8V or +3.3V
TPM.VHIO change to +1.8V_SPI or +3V_SPI (same as chipset LPC/SPI interface)



	NPCT650	NPCT750
TPR6	x	v
TPR7	v	x
TPR8	v	x
TPR9	v	x

06120-00010800 NPCT650ABBYX TPM2.0 F/W:1.3.1.0
06120-00080200 NPCT750AABYX TPM2.0 F/W:7.2.1.0

(Pin.18) PIRQ#
It should be connected to one of PIRQ[A:D]# of Chipset inputs

(Pin.27) SERIRQ
for LPC interface use only

(Pin.17) SPI_RST#
PCI system reset used for LPC/SPI bus (Hardware reset)

(Pin.4) PP (Physical Presense Input)
By default the PP functionality is disabled.

GPIO[0:6] and PP are optional.
Leave them open if not used.

GPIO[0] contact to SLP_S0# for Connected Standby, if supported.

Windows10 Hardware Compatibility Specifications for RS3
Mandatory: The TPM must support driven communication.
Mandatory: The TPM interrupt pin must be connected to an interrupt controller.

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CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS

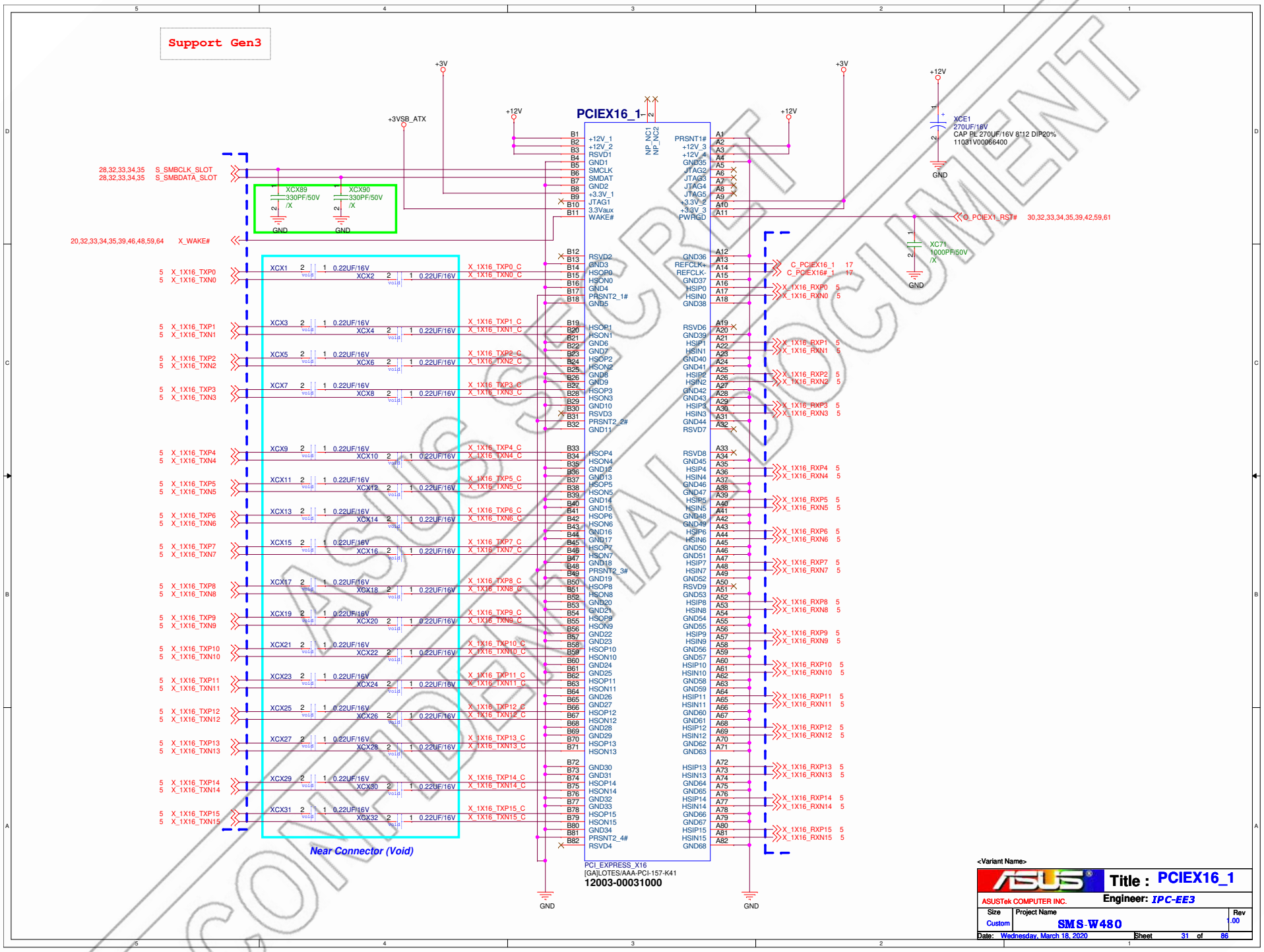
Title : TPM_NPCT750AABYX

ASUSTek COMPUTER INC.

Engineer: IPC-EE3

Size	Project Name	Rev
A4	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 30 of 86



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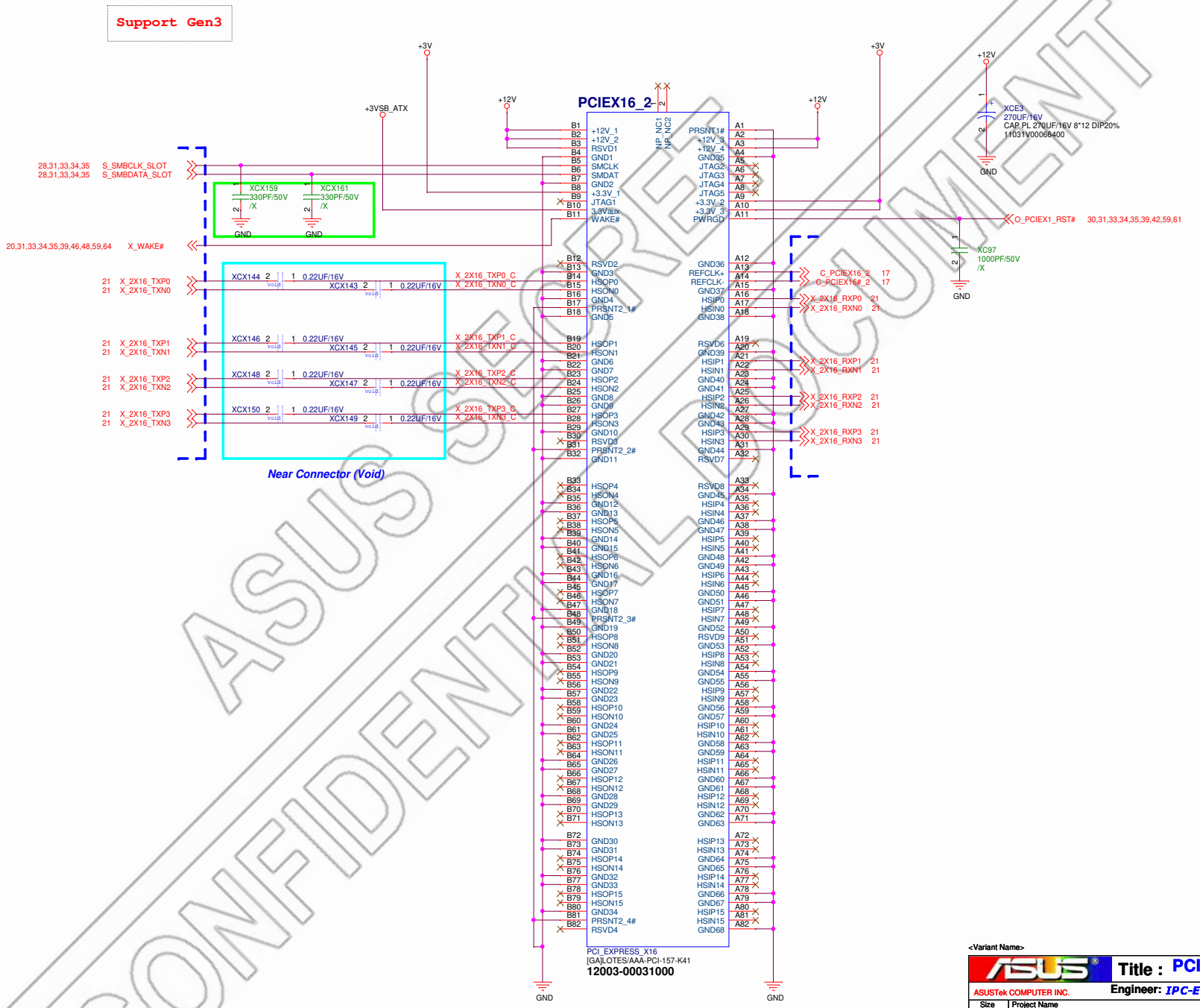
CONFIDENTIAL DOCUMENT



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<Variant Name>

ASUS

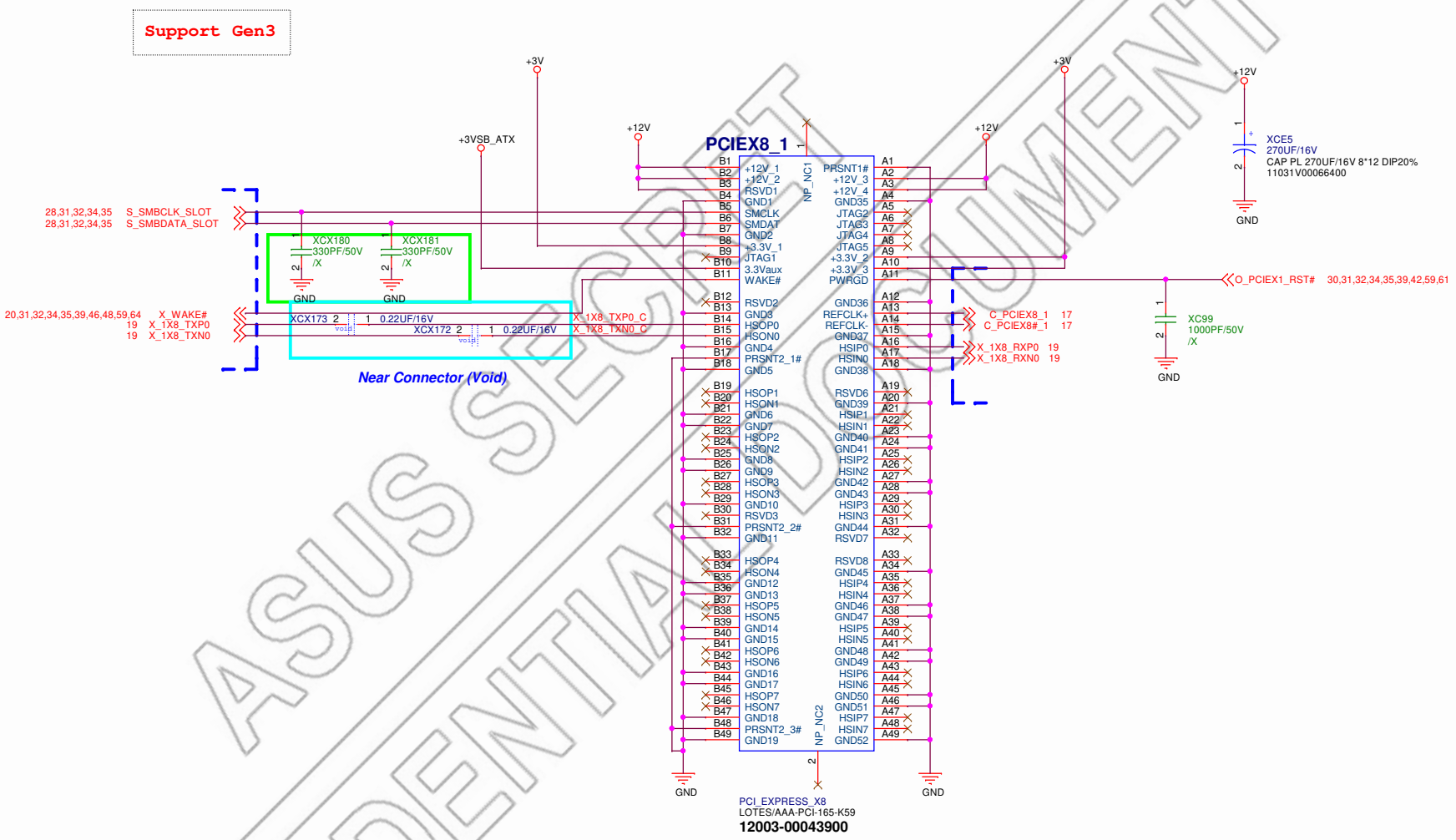
Title : PCIEX16_2

ASUSTek COMPUTER INC.

Engineer: IPC-EE3

Size	Project Name	Rev
Custom	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 32 of 86



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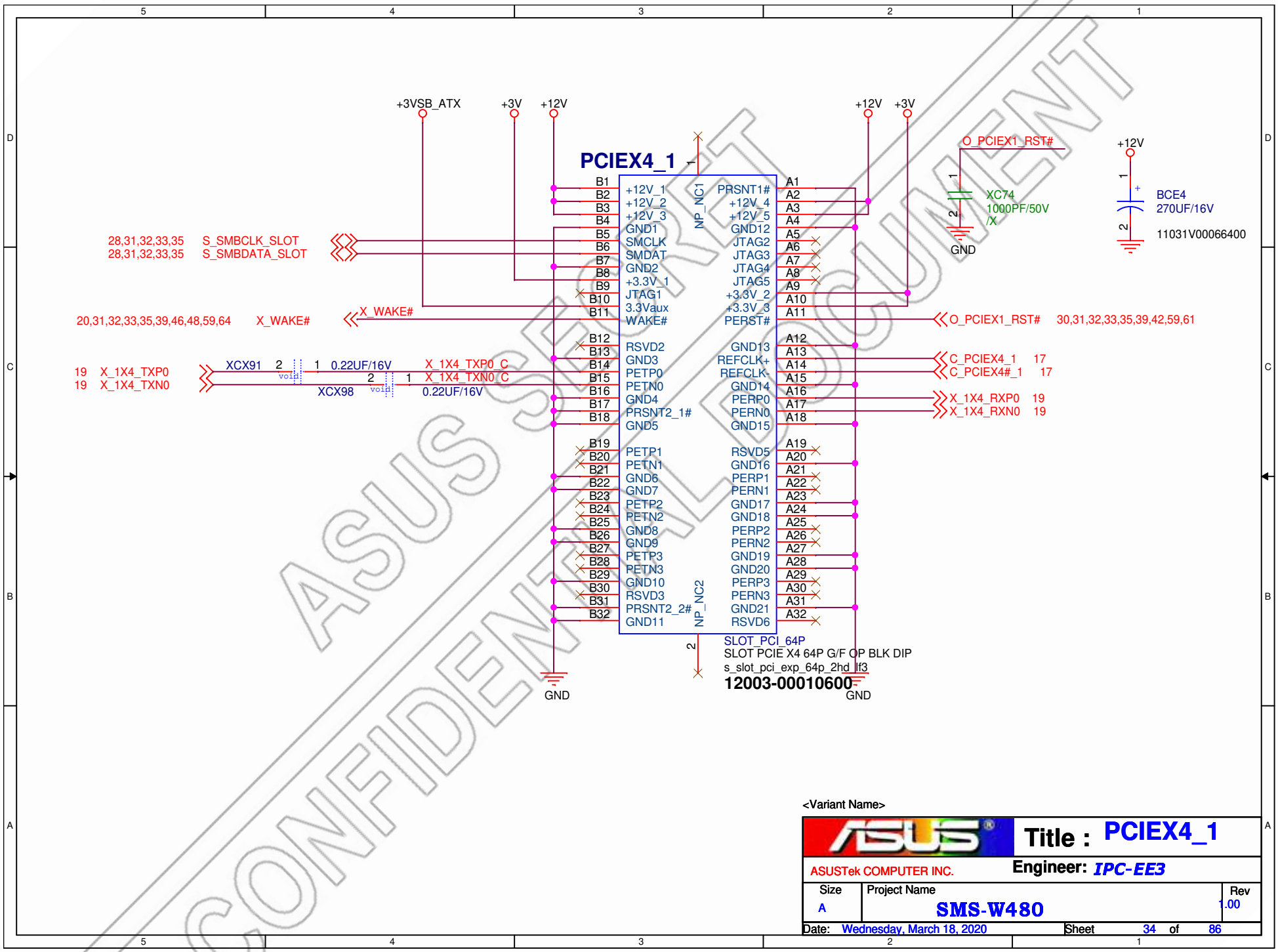
CONFIDENTIAL DOCUMENT

<Variant Name>

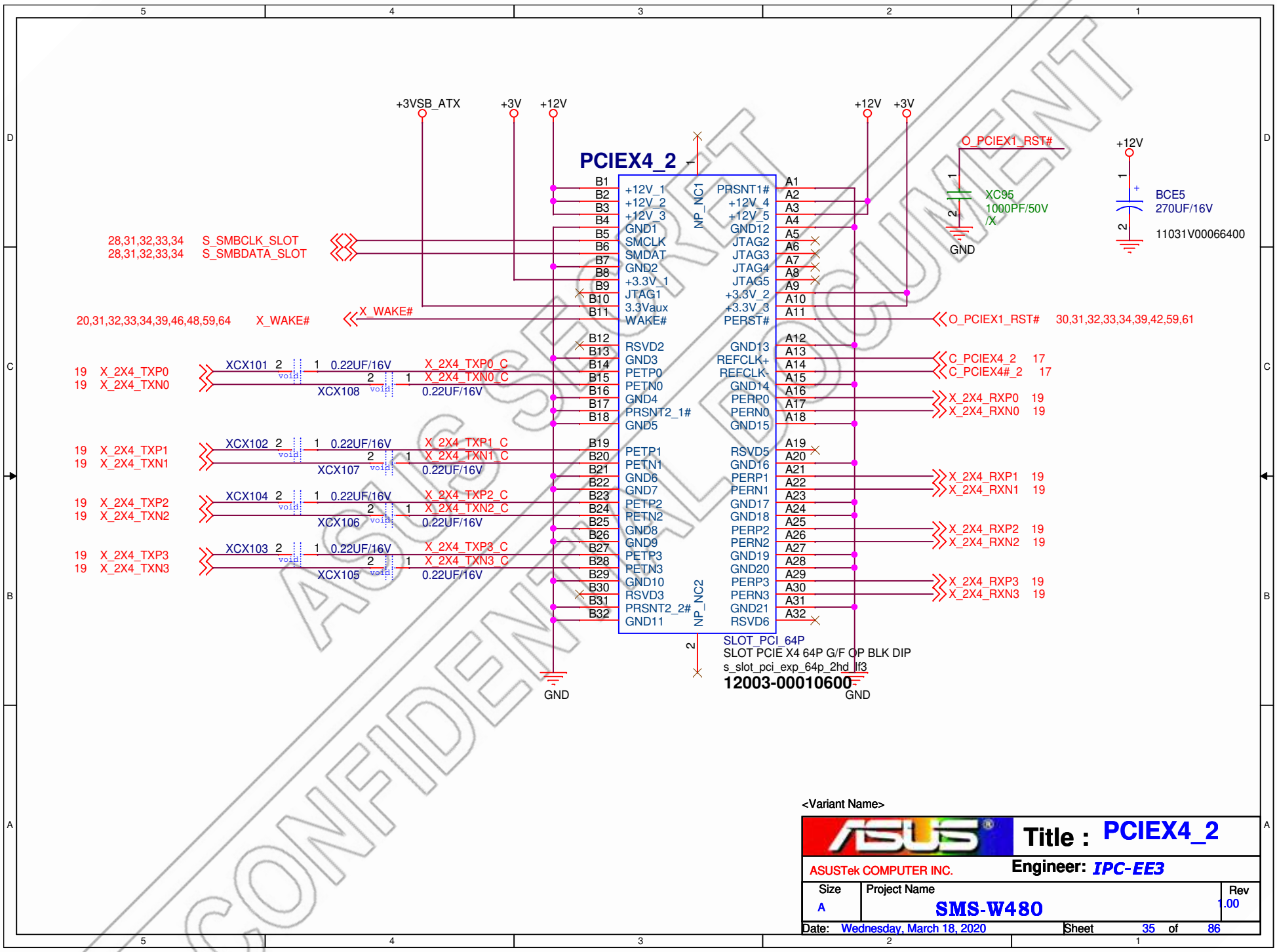
ASUS	Title : PCIEX8	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 33 of 86	



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS	Title : PCIEX4_1	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 34 of 86	



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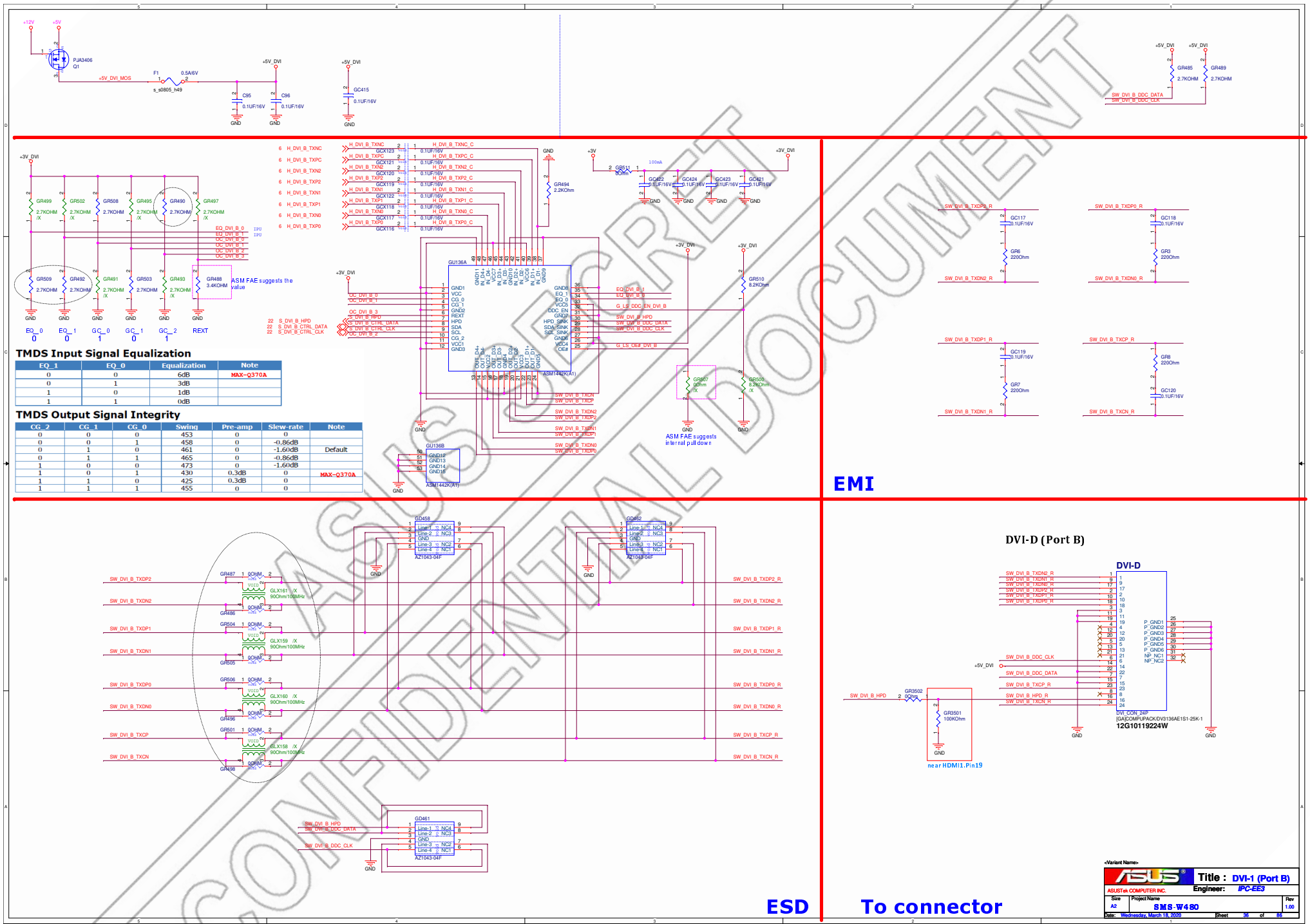
<Variant Name>

ASUS	Title : PCIEX4_2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: A	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 35 of 86	



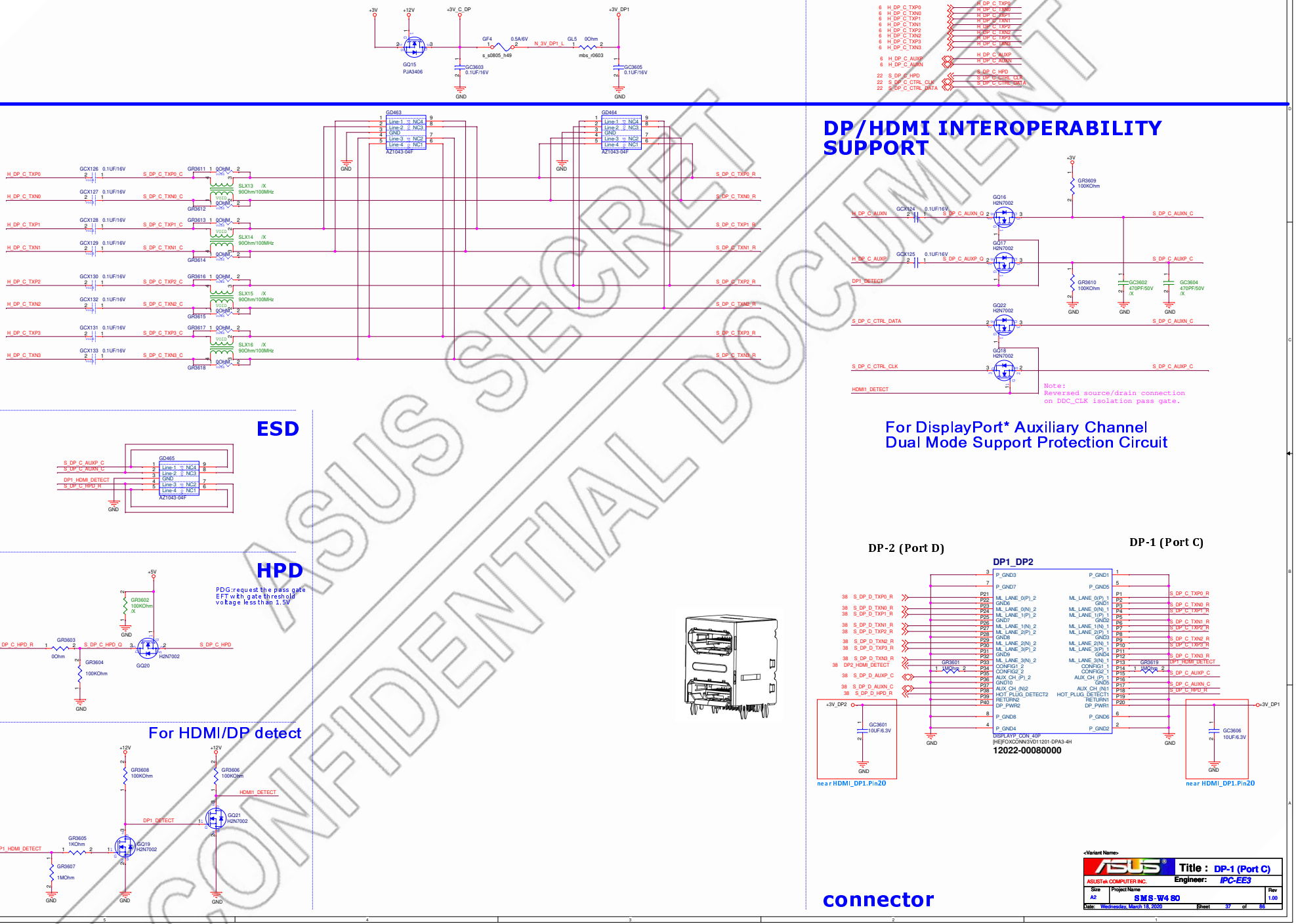
TMDS Input Signal Equalization

EQ_1	EQ_0	Equalization	Note
0	0	6dB	MAX-Q370A
0	1	3dB	
1	0	1dB	
1	1	0dB	

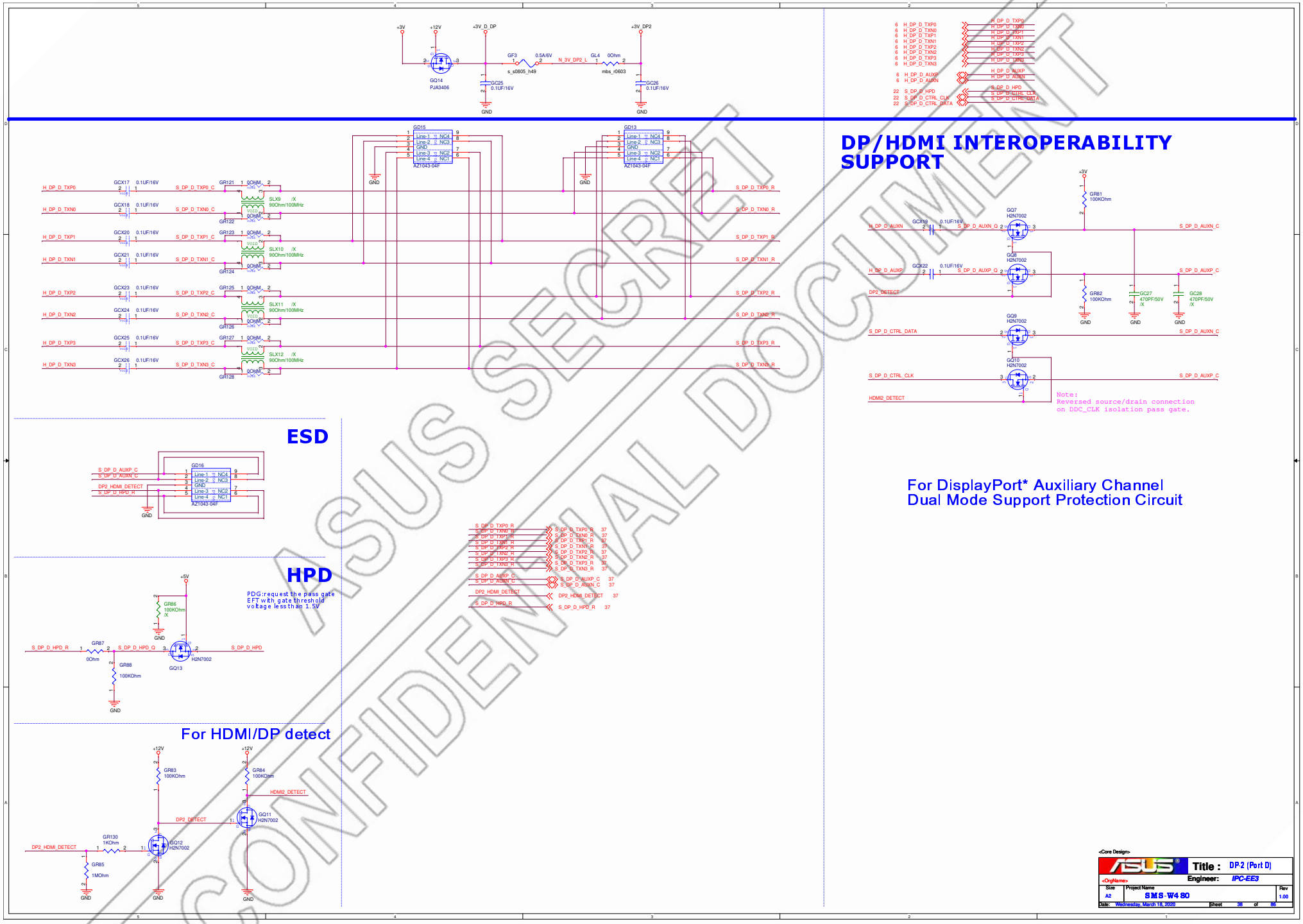
TMDS Output Signal Integrity

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note
0	0	0	453	0	0	
0	0	1	458	0	-0.86dB	
0	1	0	461	0	-1.60dB	Default
0	1	1	465	0	-0.86dB	
1	0	0	473	0	-1.60dB	
1	0	1	430	0.3dB	0	MAX-Q370A
1	1	0	425	0.3dB	0	
1	1	1	455	0	0	

ASUS SECRET
CONFIDENTIAL DOCUMENT



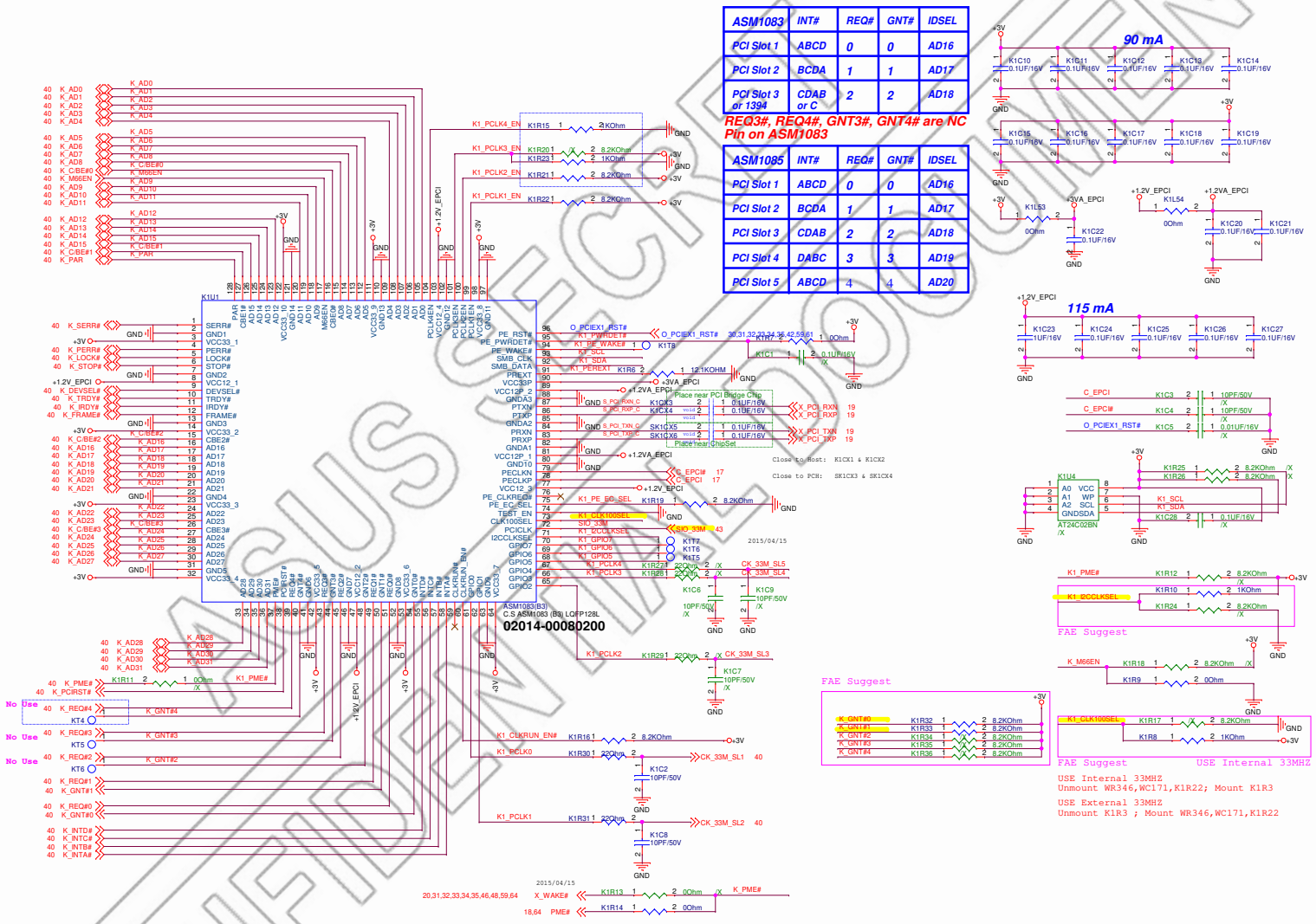
ASUS SECRET
CONFIDENTIAL DOCUMENT


DP/HDMI INTEROPERABILITY SUPPORT
For DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit
ESD
HPD
PDG:request the pass gate EFT with gate threshold voltage less than 1.5V
For HDMI/DP detect
Note: Reversed source/drain connection on DDC_CLK isolation pass gate.
Title : DP-2 (Port D)
Engineer: IPC-EE3
SMS-W480
Date: Wednesday, March 18, 2020
Sheet 38 of 85
ASUS SECRET CONFIDENTIAL DOCUMENT

ASM1083	INT#	REQ#	GNT#	IDSEL
PCI Slot 1	ABCD	0	0	AD16
PCI Slot 2	BCDA	1	1	AD17
PCI Slot 3 or 1394	CDAB or C	2	2	AD18

REQ3#, REQ4#, GNT3#, GNT4# are NC Pin on ASM1083

ASM1085	INT#	REQ#	GNT#	IDSEL
PCI Slot 1	ABCD	0	0	AD16
PCI Slot 2	BCDA	1	1	AD17
PCI Slot 3	CDAB	2	2	AD18
PCI Slot 4	DABC	3	3	AD19
PCI Slot 5	ABCD	4	4	AD20



ASUS SECRET DOCUMENT
CONFIDENTIAL

<Variant Name>

ASUSTek COMPUTER INC.

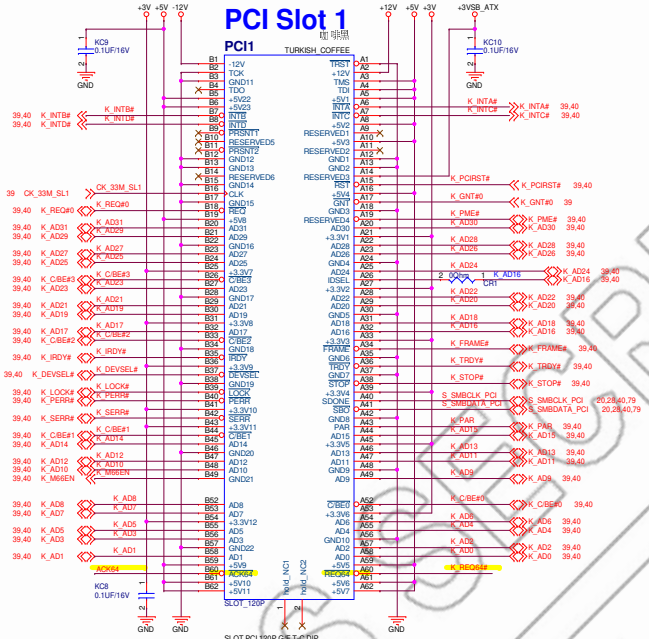
Title : PCI_ASM1083

Engineer: IPC-EE3

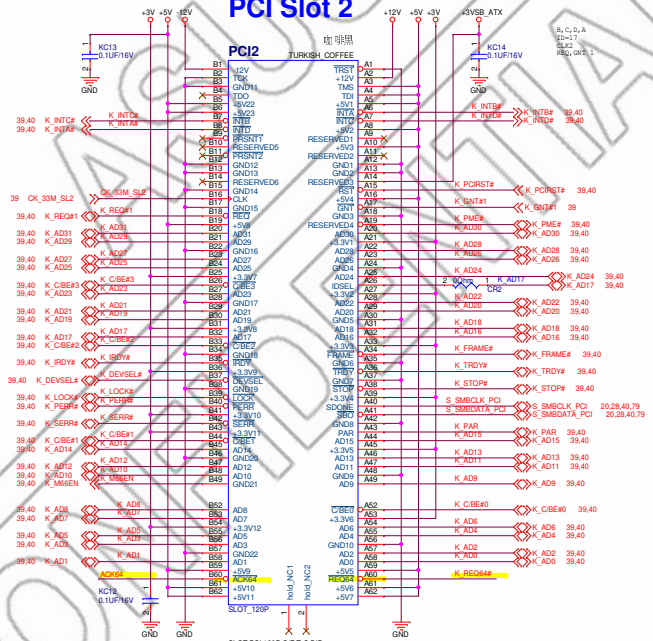
Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 39 of 86

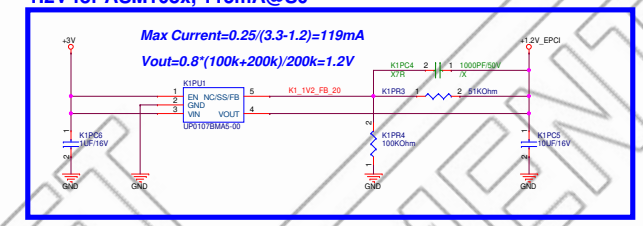
PCI Slot 1



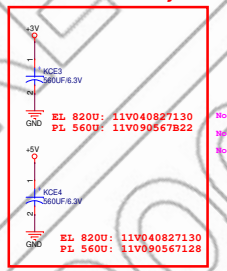
PCI Slot 2



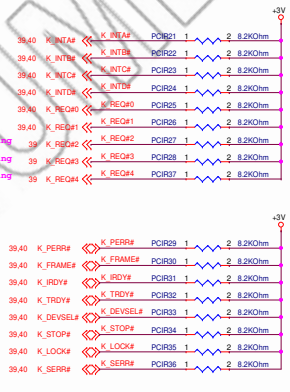
1.2V for ASM108x, 115mA@S0



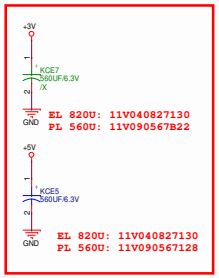
PL & EL CAP co-lay



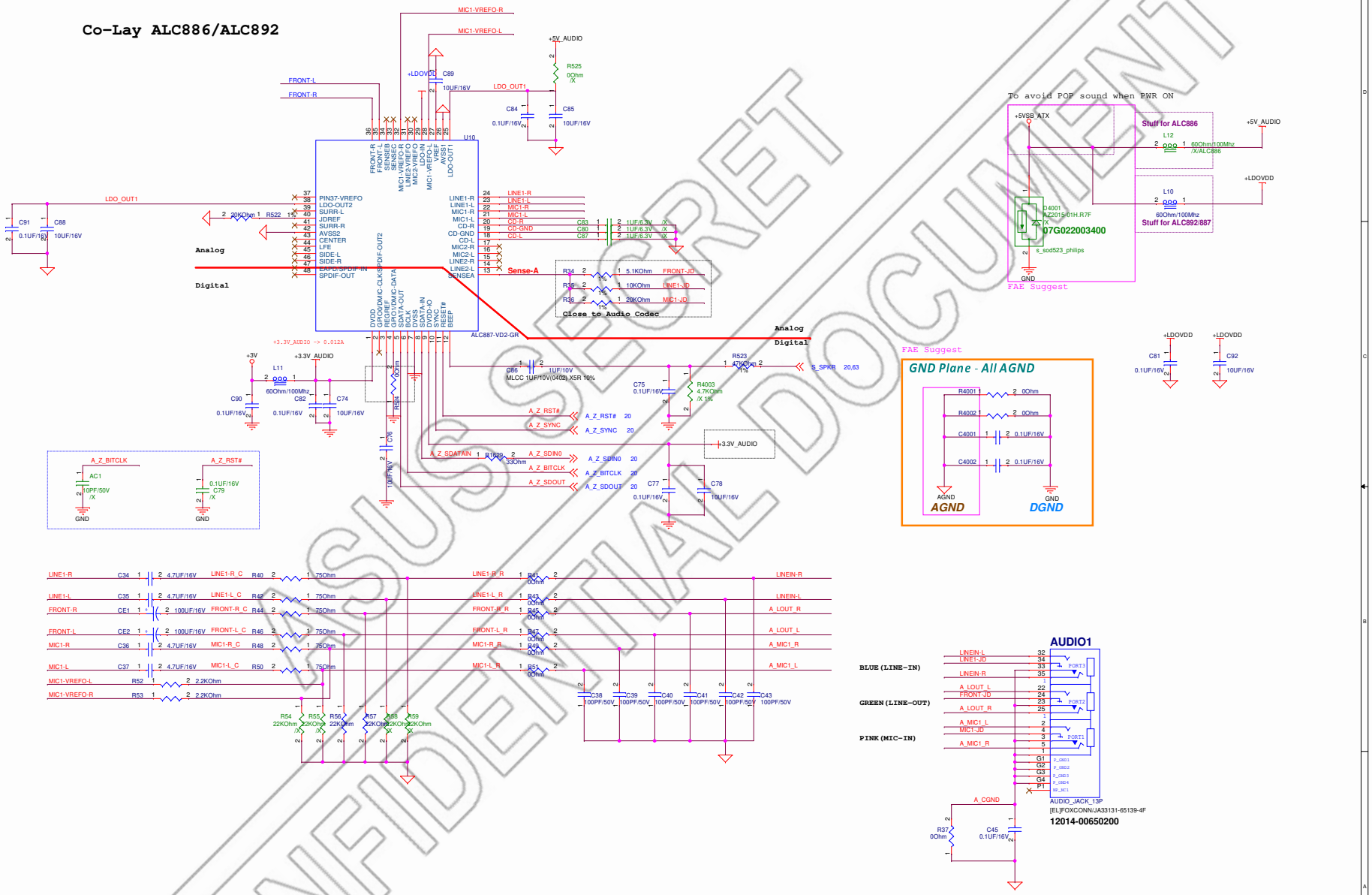
No Use, Avriod Floating
No Use, Avriod Floating
No Use, Avriod Floating



PL & EL CAP co-lay



ASUS CONFIDENTIAL DOCUMENT



CONFIDENTIAL ASUS SECRET DOCUMENT

<Variant Name>

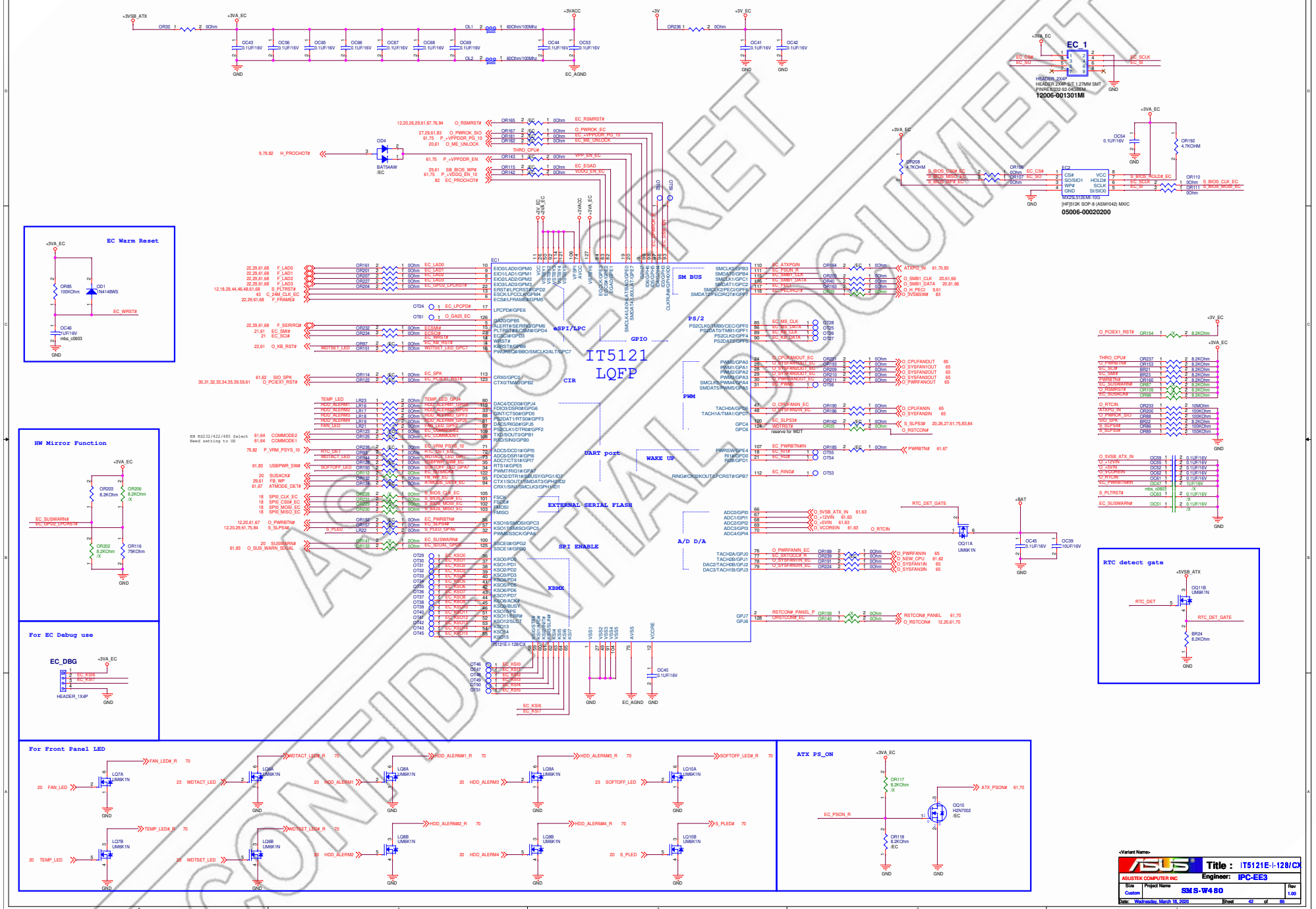
ASUSTEK COMPUTER INC

Title : AUDIO CODEC ALC887

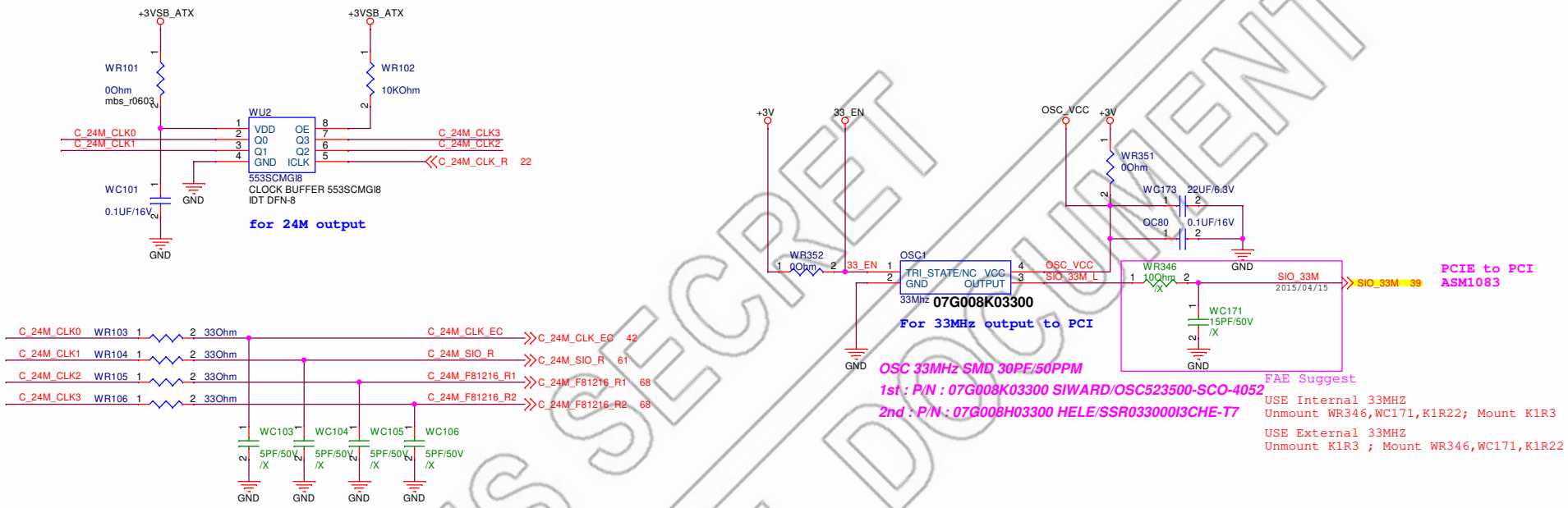
Engineer: IPC-EE3

Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 41 of 86



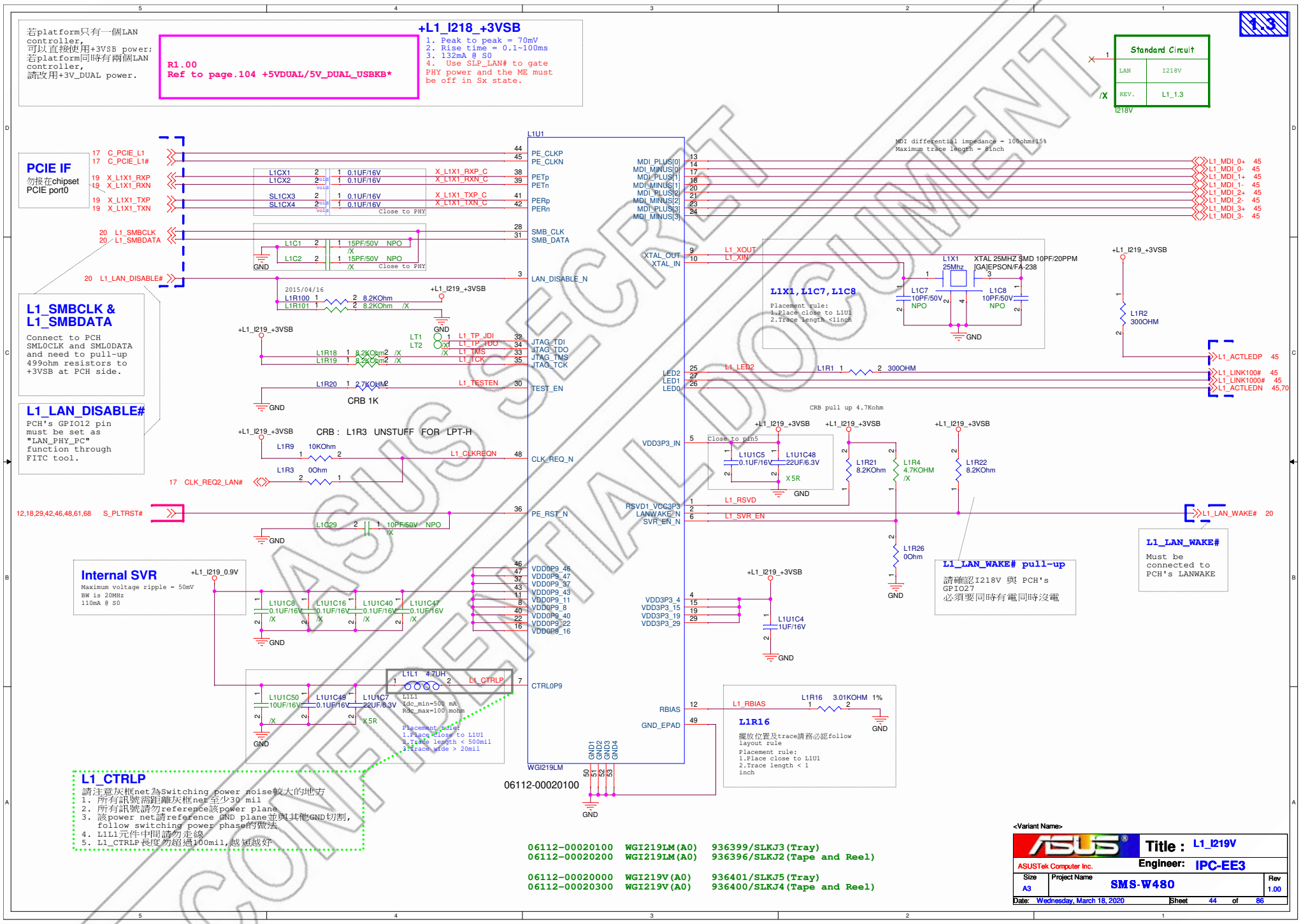
CONFIDENTIAL DOCUMENT

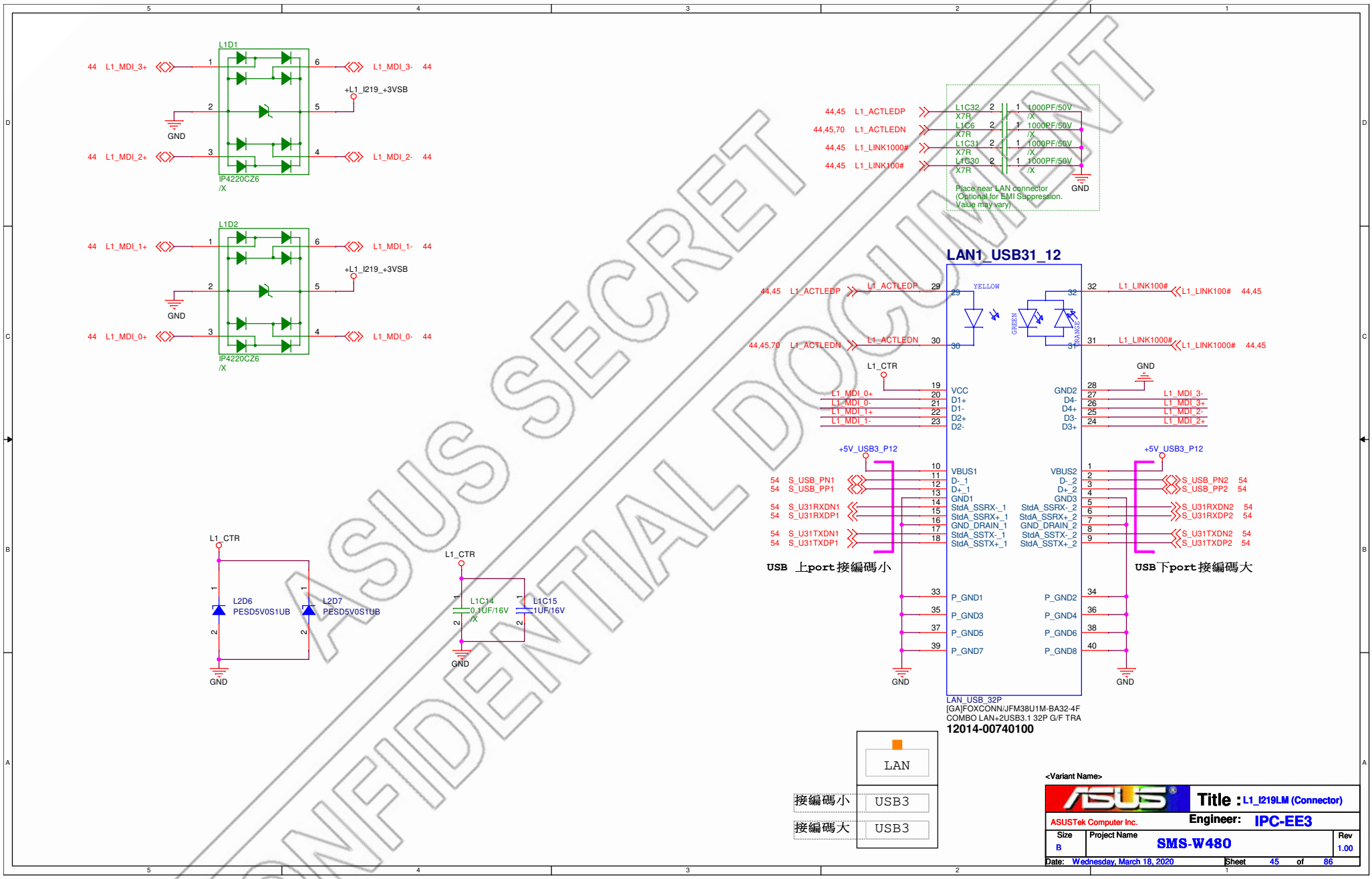


ASUS SECRET
CONFIDENTIAL DOCUMENT

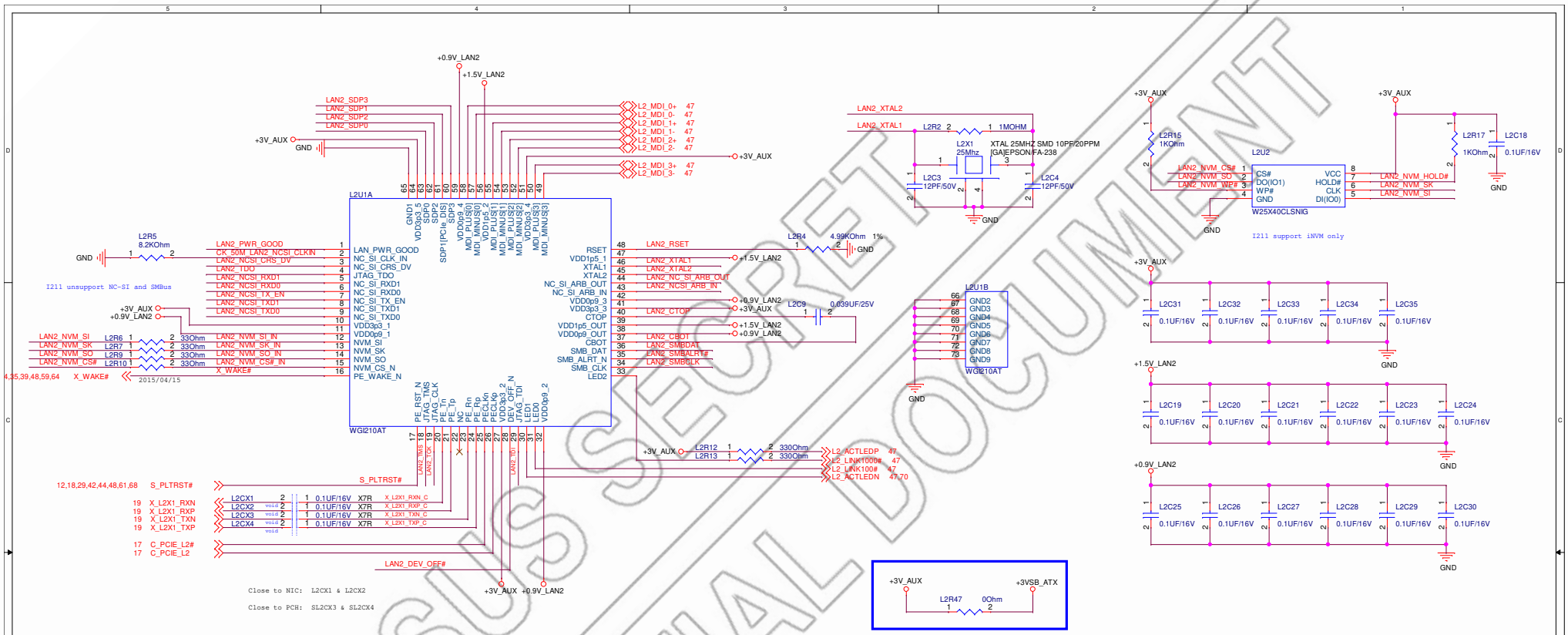
<Variant Name>

ASUS	Title : Clock Buffer	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 43 of 86	

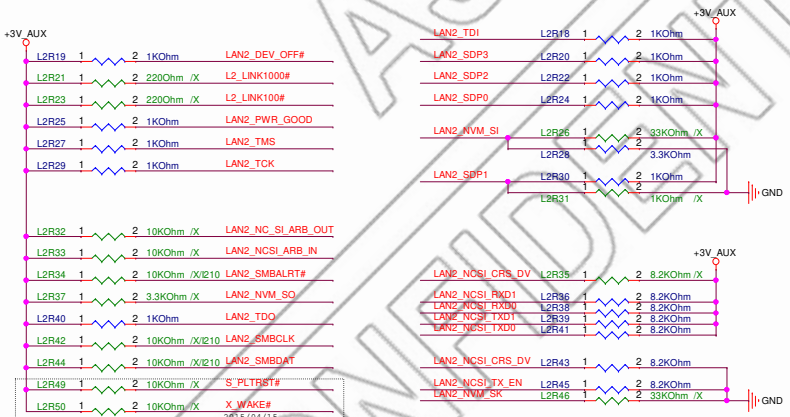

若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.
R1.00
Ref to page.104 +5VDUAL/5V_DUAL_USBKB*
+L1_I218_+3VSB
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.
Standard Circuit
LAN I218V
REV. L1_1.3
PCIE IF
勿接在chipset PCIE port0
L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.
L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.
L1U1
WGI219LM
06112-00020100
MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch
L1X1,L1C7,L1C8
Placement rule:
1.Place close to L1U1
2.Trace length <1inch
XTAL 25MHZ SMD 10PF/20PPM [GA]EPSON/FA-238
CRB pull up 4.7Kohm
CRB : L1R3 UNSTUFF FOR LPT-H
L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電
L1_LAN_WAKE#
Must be connected to PCH's LANWAKE
Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0
L1_CTRLP
請注意灰框net為Switching power noise較大的地方
1. 所有訊號需距離灰框net至少30 mil
2. 所有訊號請勿reference該power plane
3. 該power net請reference GND plane並與其他GND切割, follow switching power phase的做法
4. L1L1元件中間請勿走線
5. L1_CTRLP長度勿超過100mil,越短越好
L1R16
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch
06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)
06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)
ASUS SECRET
CONFIDENTIAL DOCUMENT
ASUSTek Computer Inc.
Title : L1_I219V
Engineer: IPC-EE3
Size A3
Project Name SMS-W480
Rev 1.00
Date: Wednesday, March 18, 2020
Sheet 44 of 86



ASUS SECRET
CONFIDENTIAL DOCUMENT



Follow CRB A.B.



Strapping Options

DEV_OFF_N
I210.28 (DEV_OFF_N)
1: Exit Device off mode (Default)
0: Enter Device off mode

AUX_PWR
I210.28 (DEV_OFF_N)
I210.60 (SDP3)
11: Enable AUX power mode (Default)

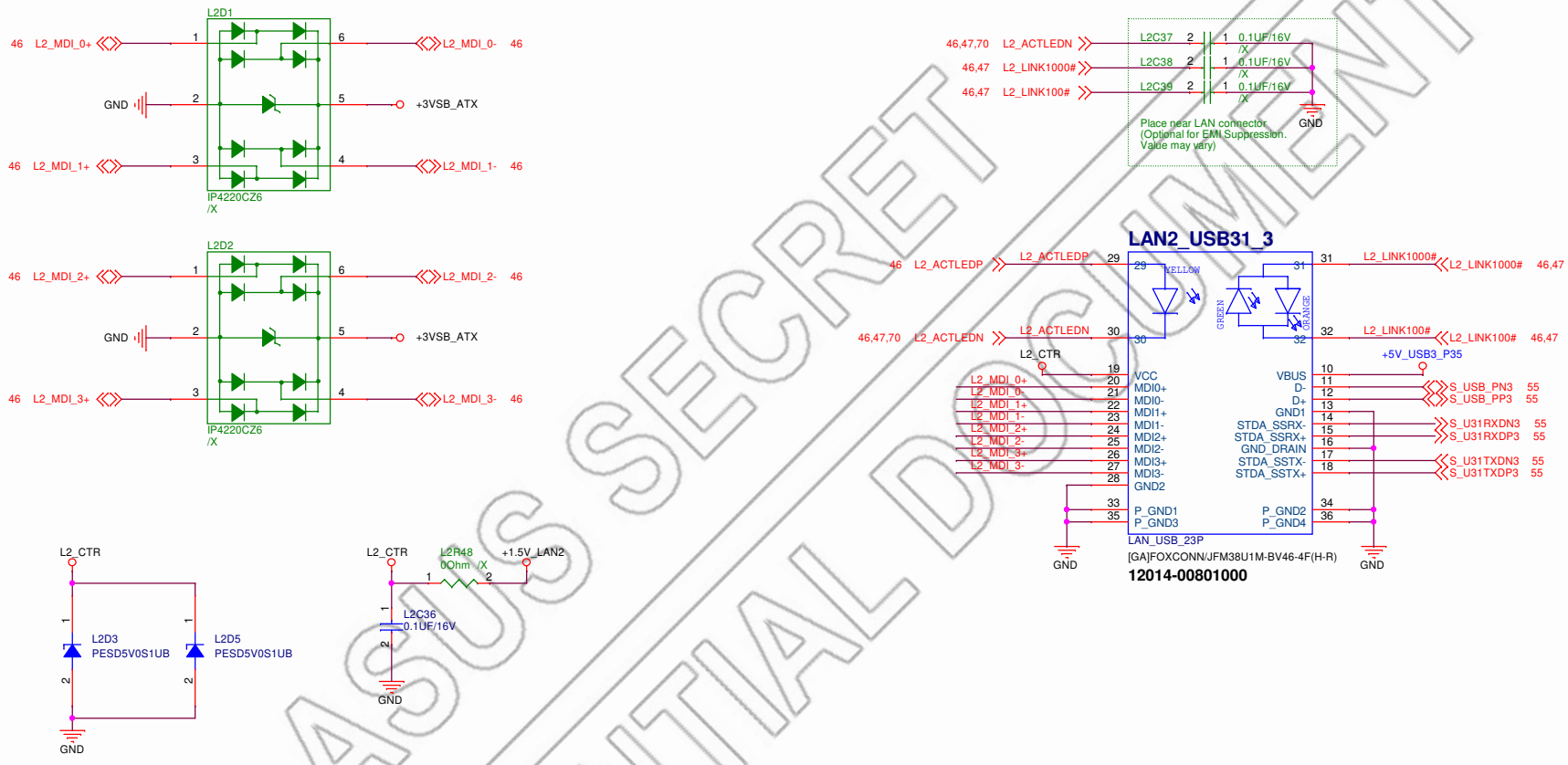
Security_EN
I210.12 (NVM_SI)
1: Enable Flash security
0: Disable Flash security (Default)

PCIE_DIS_N
I210.61 (SDP1[PCIe_DIS])
1: Enable PCIe function (Default)
0: Disable PCIe function

ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

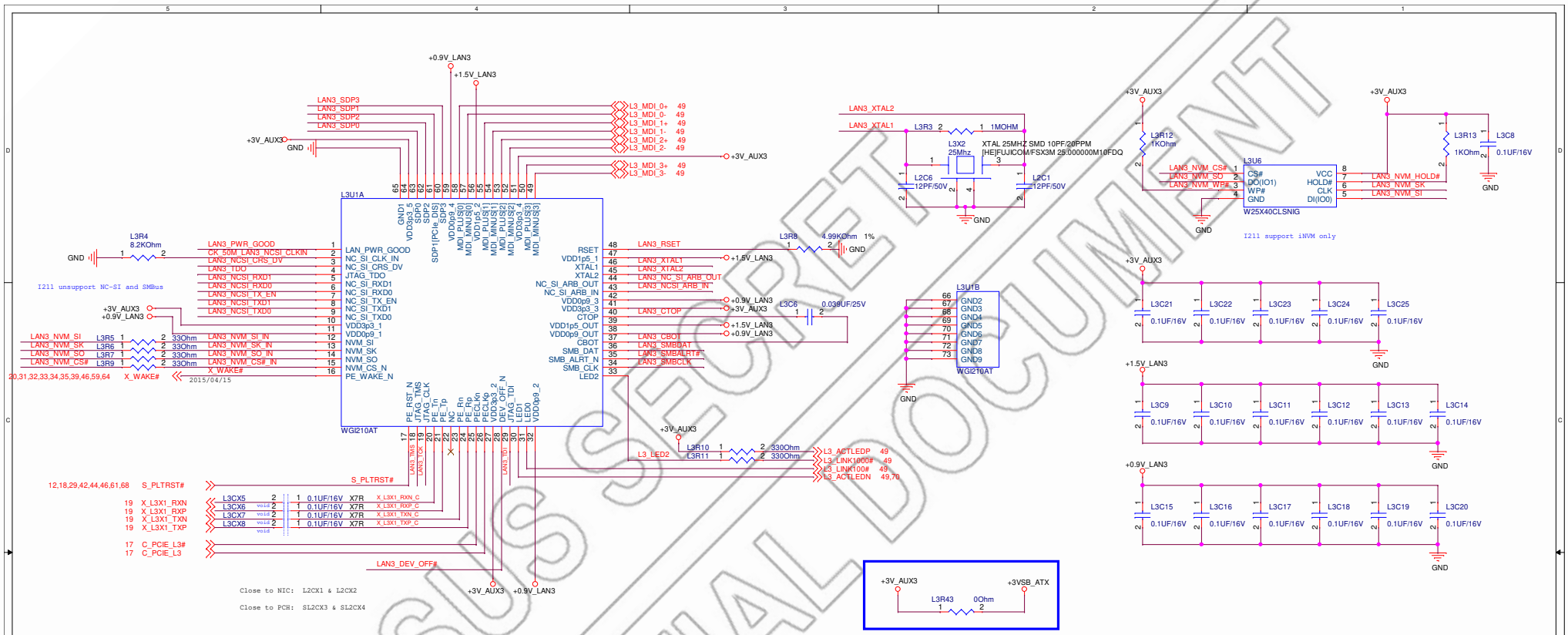
ASUS	Title : LAN2_I210-AT		
ASUSTek COMPUTER INC.	Engineer: IPC-EE3		
Size: Custom	Project Name: SMS-W480		Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 46 of 86		



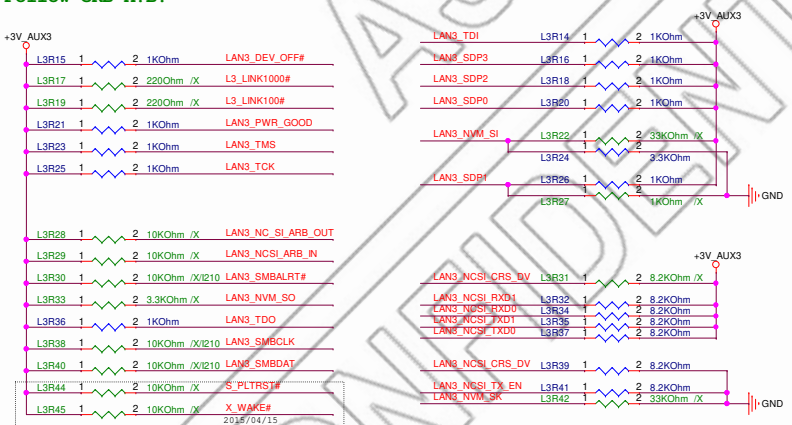
ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS	Title : LAN2_RJ45	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 47 of 86	



Follow CRB A.B.



Strapping Options

DEV_OFF_N
I210.28 (DEV_OFF_N)
1: Exit Device off mode (Default)
0: Enter Device off mode

AUX_PWR
I210.28 (DEV_OFF_N)
I210.60 (SDP3)
11: Enable AUX power mode (Default)

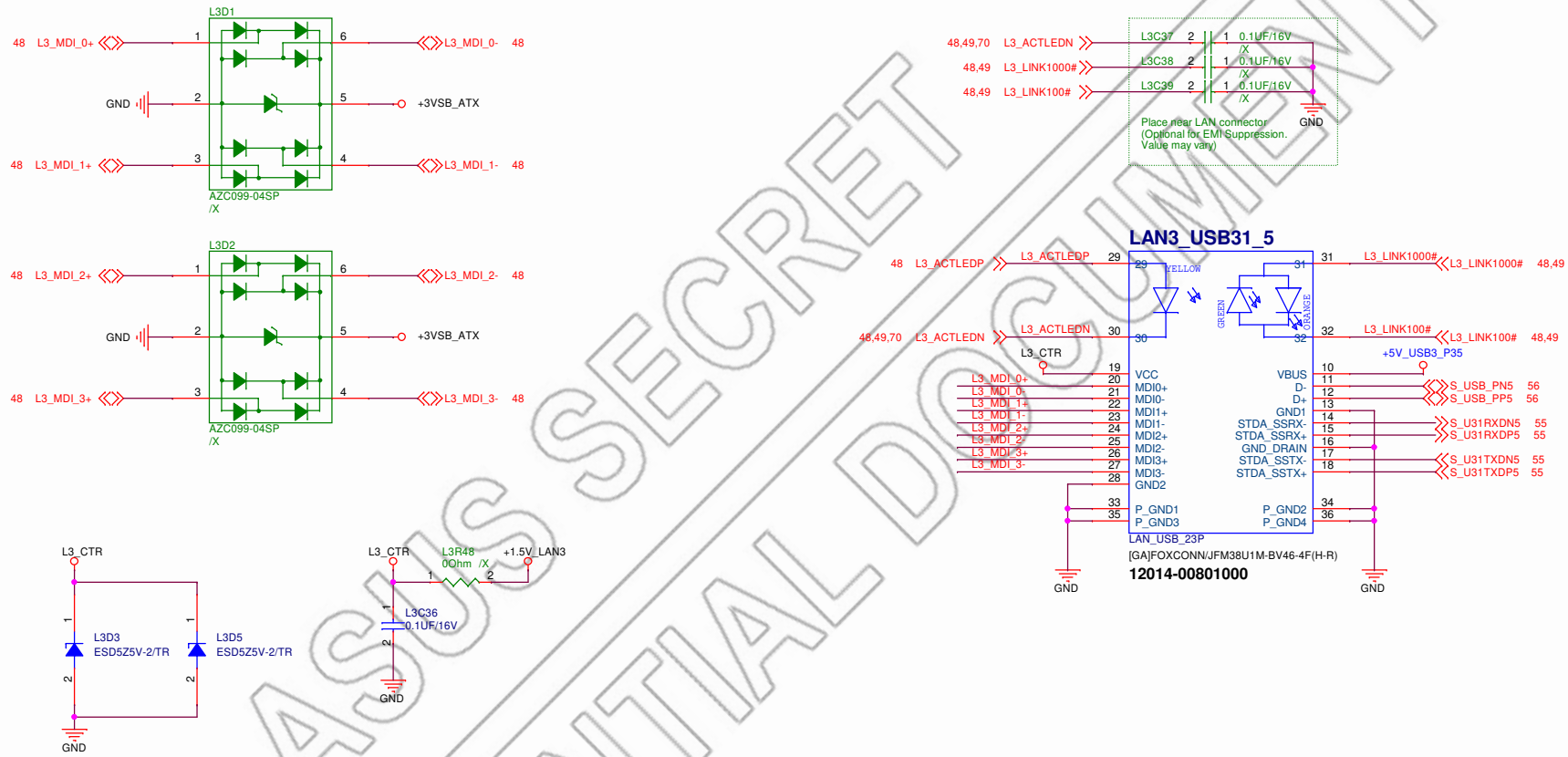
Security_EN
I210.12 (NVM_SI)
1: Enable Flash security
0: Disable Flash security (Default)

PCIE_DIS_N
I210.61 (SDP1[PCIe_DIS])
1: Enable PCIe function (Default)
0: Disable PCIe function

ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

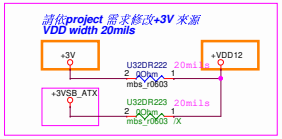
ASUS	Title : LAN3_I210-AT		
ASUSTEK COMPUTER INC	Engineer: IPC-EE3		
Size: Custom	Project Name: SMS-W480		Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 48 of 86		

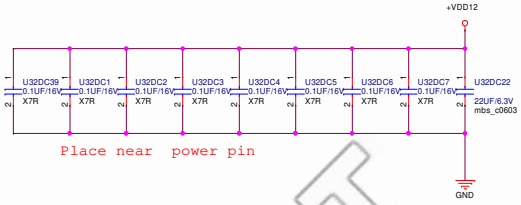


ASUS SECRET
CONFIDENTIAL DOCUMENT

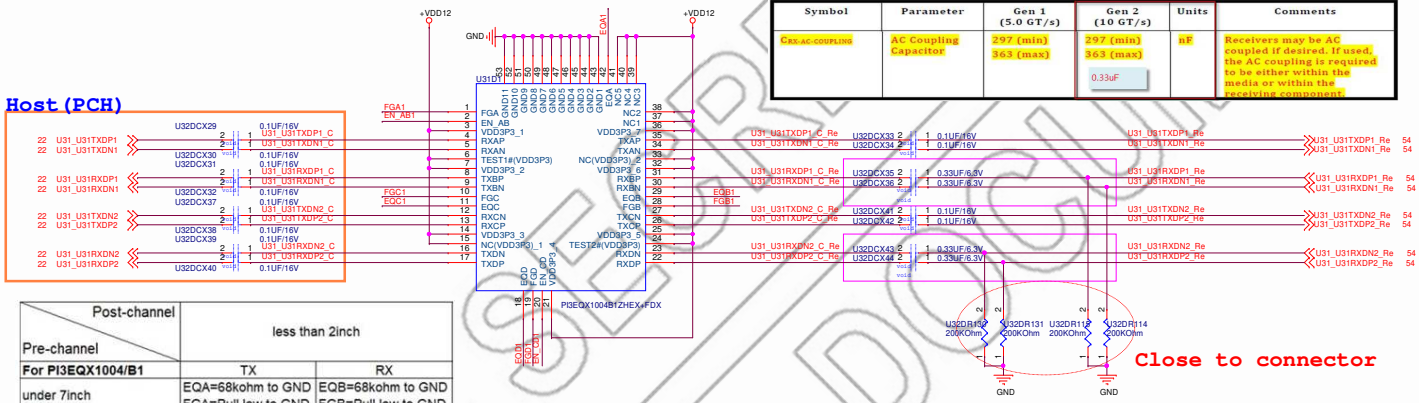
<Variant Name>

ASUS	Title : LAN3_RJ45	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size: Custom	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 49 of 86	





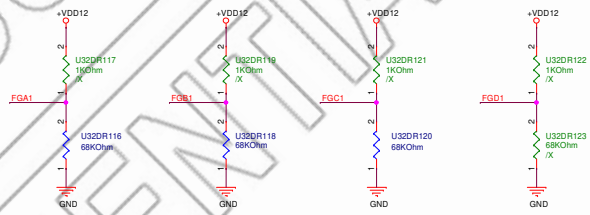
Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
CTX-AC-COUPLING	AC Coupling Capacitor	297 (min) 363 (max)	297 (min) 363 (max) 0.33uF	nF	Receivers may be AC coupled if desired. If used, the AC coupling is required to be either within the media or within the receiving component.



Post-channel / Pre-channel	less than 2inch	
For PI3EQX1004/B1	TX	RX
under 7inch	EQA=68kohm to GND FGA=Pull low to GND	EQB=68kohm to GND FGB=Pull low to GND
7inch to 9inch	EQA=Floating FGA=Pull low to GND	EQB=68kohm to GND FGB=Floating
up to 12inch	EQA=1kohm to VDD FGA=Pull low to GND	EQB=68kohm to GND FGB=1kohm to VDD

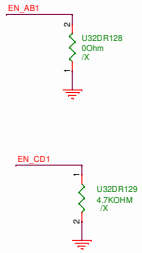
Strapping pin

FGA1/B1/C1/D1	Flat Gain(db)
pull up	+2.7
pull down	-0.5
F(Leave oprn)	1.0(Default)
R (Tie Rext to Gnd)	-1.6



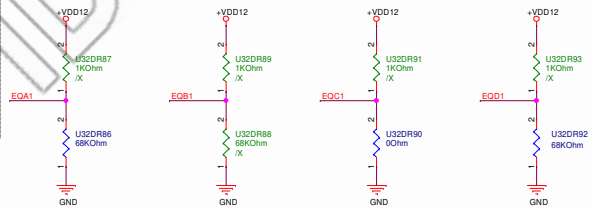
Channel Enable

EN	Setting
Pull up (Internal P-U)	Enable(Default)
pull down	Disable



Strapping pin

EQA1/B1/C1/D1	Equalizer 2.5G/5G (db)
pull up	8.4/14.6
pull down	6.7/12.4
F(Leave oprn)	5.3/10.6(Default)
R (Tie Rext to Gnd)	3.5/8



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

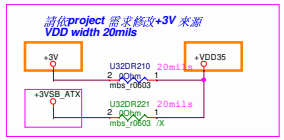
ASUSTeK COMPUTER INC.

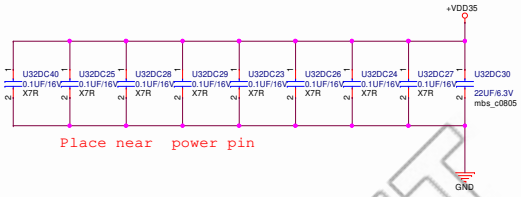
Title : U31 Port 1,2 Re driver IC

Engineer: IPC-EE3

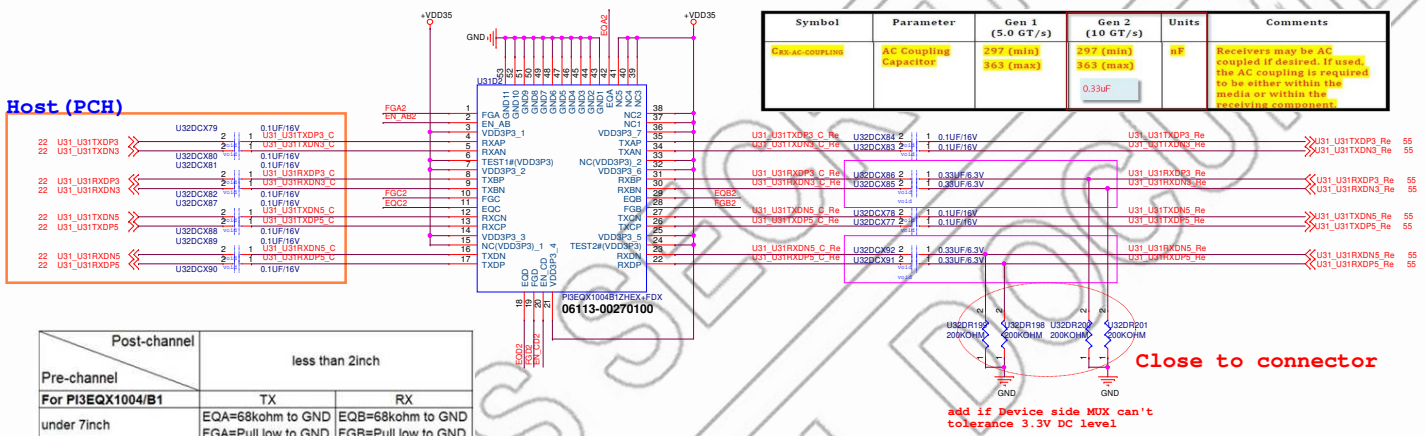
Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 50 of 86





Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$C_{RX-AC-COUPLING}$	AC Coupling Capacitor	297 (min) 363 (max)	297 (min) 363 (max) 0.33uF	nF	Receivers may be AC coupled if desired. If used, the AC coupling is required to be either within the media or within the receiving component.



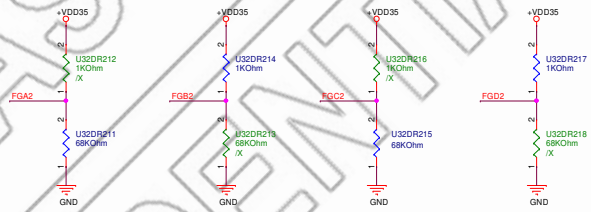
Post-channel / Pre-channel	less than 2inch	
For PI3EQX1004/B1	TX	RX
under 7inch	EQA=68kohm to GND FGA=Pull low to GND	EQB=68kohm to GND FGB=Pull low to GND
7inch to 9inch	EQA=Floating FGA=Pull low to GND	EQB=68kohm to GND FGB=Floating
up to 12inch	EQA=1kohm to VDD FGA=Pull low to GND	EQB=68kohm to GND FGB=1kohm to VDD

Strapping pin

FGA2/B2/C2/D2	Flat Gain(db)
pull up	+2.7
pull down	-1.6
F(Leave oprn)	1.0(Default)
R (Tie Rext to Gnd)	-0.5

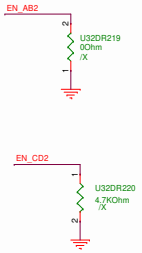
Rext = 68Kohm

Rext = 1Kohm for Current Limit



Channel Enable

EN	Setting
Pull up (Internal P-U)	Enable(Default)
pull down	Disable

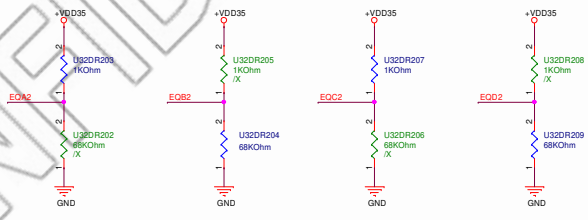


Strapping pin

EQA2/B2/C2/D2	Equalizer 2.5G/5G (db)
pull up	8.4/14.6
pull down	6.7/12.4
F(Leave oprn)	5.3/10.6(Default)
R (Tie Rext to Gnd)	3.5/8

Rext = 68Kohm

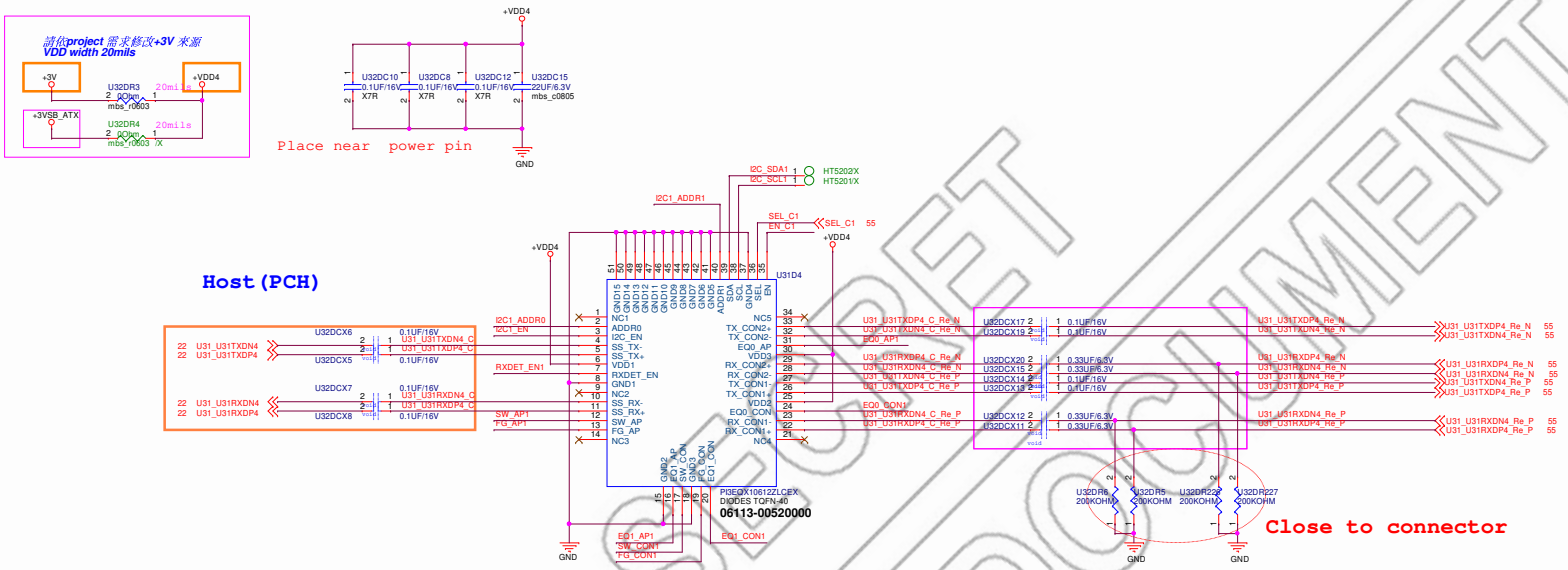
Rext = 1Kohm for Current Limit



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

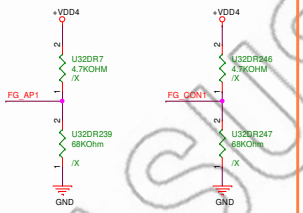
ASUS	Title : U31 Port3,5 Redriver IC	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size C	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 51 of 86	



Strapping pin

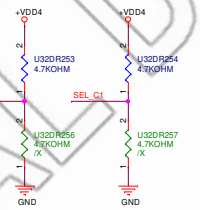
FG_AP1/CON1	Flat Gain(db)
R (Tie Rext to Gnd)	-2.7
F(Leave oprn)	-0.24(Default)
pull down	0.62
pull up	1.77

Rext = 68Kohm

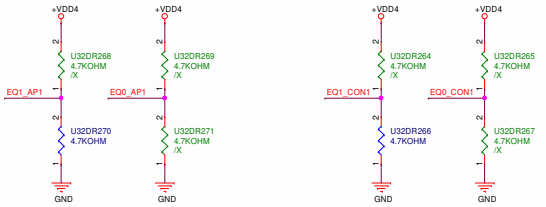


Strapping pin

EN_C1	SEL_C1	Redriver Connection
0	X	Inactive
1	1	TX/RX_CON1 Active
1	0	TX/RX_CON2 Active



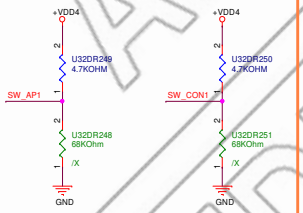
Equalization Setting



Strapping pin

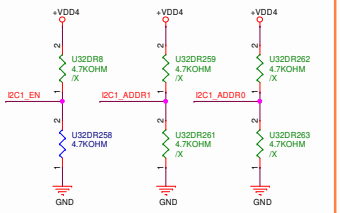
SW_AP1/CON1	Swing Setting (ppd)
R (Tie Rext to Gnd)	1200mV
F(Leave oprn)	1100mV
pull down	900mV
pull up	1000mV (Default)

Rext = 68Kohm



I2C Strapping pin

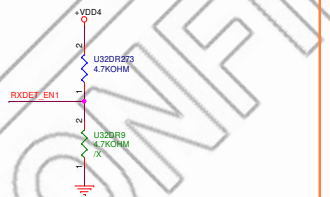
I2C_EN1	I2C_ADDR1	I2C_ADDR1	Redriver I2C Address
1	0	0	A0h
1	0	1	A2h
1	1	0	A4h
1	1	1	A6h
0	X	X	Pin Mode



Equalization Setting (dB):

EQ1pin	EQ0pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
0	F	0	0	0	0	3.57	4.22	5.44	6.42	7.27	Default
0	1	0	0	0	1	3.83	4.56	5.93	7.04	8.00	
0	0	0	0	1	0	4.13	4.93	6.47	7.71	8.76	
0	R	0	0	1	1	4.41	5.29	6.95	8.29	9.42	
R	1	0	1	0	0	4.98	5.89	7.61	8.99	10.14	
R	F	0	1	0	1	5.25	6.23	8.05	9.50	10.70	
R	R	0	1	1	0	5.55	6.59	8.51	10.04	11.28	
R	0	0	1	1	1	5.82	6.92	8.93	10.51	11.78	
F	0	1	0	0	0	6.39	7.44	9.39	10.93	12.16	
F	R	1	0	0	1	6.63	7.74	9.76	11.34	12.60	
F	F	1	0	1	0	6.90	8.05	10.14	11.77	13.05	
F	1	1	0	1	1	7.14	8.34	10.49	12.15	13.44	
1	R	1	1	0	0	7.51	8.71	10.87	12.53	13.81	
1	0	1	1	0	1	7.74	8.97	11.18	12.87	14.15	
1	1	1	1	1	0	7.98	9.25	11.51	13.23	14.51	
1	F	1	1	1	1	8.20	9.51	11.81	13.54	14.82	

ReDriver Loading Detection Enable Pin



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

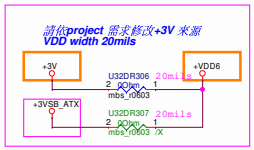
ASUSTeK COMPUTER INC.

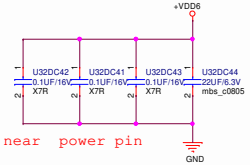
Title : U31 Port4 Redriver IC

Engineer: IPC-EE3

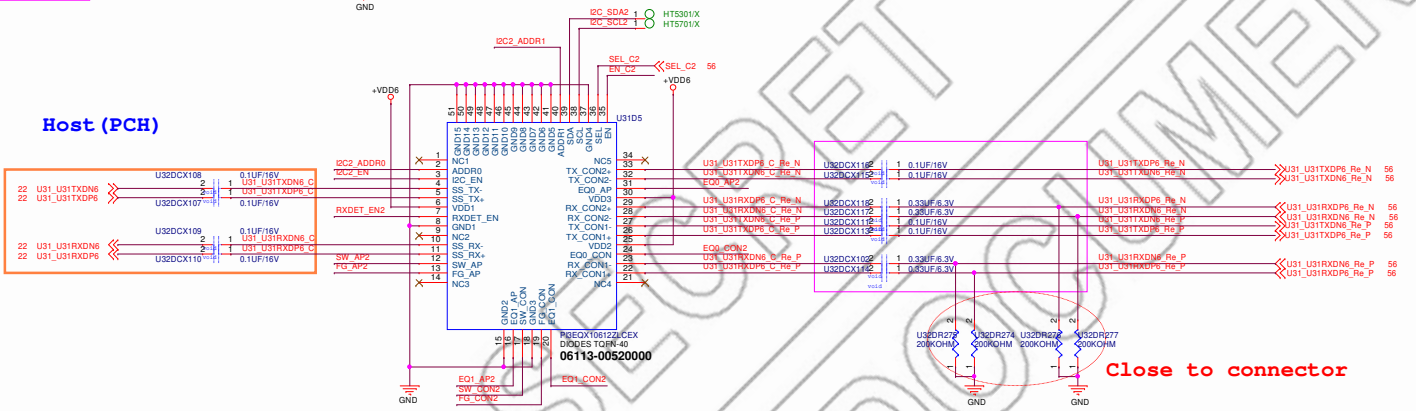
Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 52 of 86





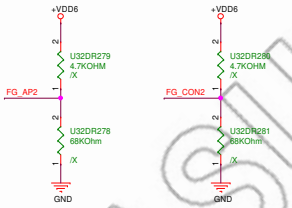
Host (PCH)



Strapping pin

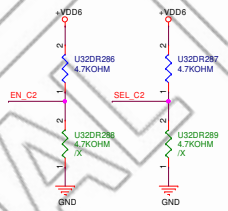
FG_AP1/CON1	Flat Gain(db)
R (Tie Rext to Gnd)	-2.7
F(Leave open)	-0.24(Default)
pull down	0.62
pull up	1.77

Rext = 68Kohm

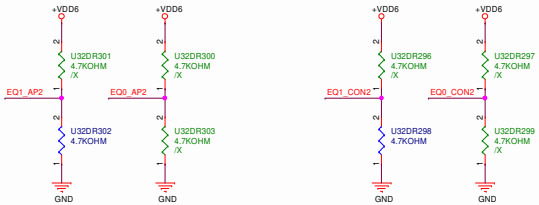


Strapping pin

EN_C1	SEL_C1	Redriver Connection
0	X	Inactive
1	1	TX/RX_CON1 Active
1	0	TX/RX_CON2 Active



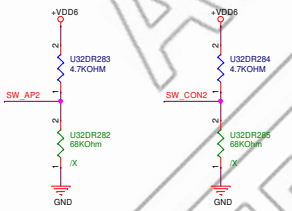
Equalization Setting



Strapping pin

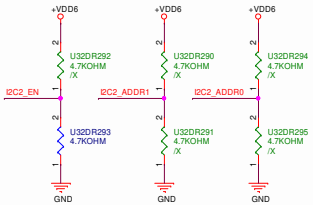
SW_AP1/CON1	Swing Setting (ppd)
R (Tie Rext to Gnd)	1200mV
F(Leave open)	1100mV
pull down	900mV
pull up	1000mV (Default)

Rext = 68Kohm



I2C Strapping pin

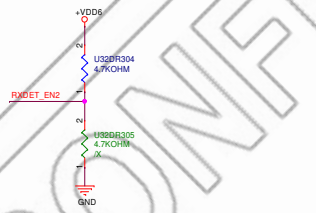
I2C_EN1	I2C_ADDR1	I2C_ADDR1	Redriver I2C Address
1	0	0	A0h
1	0	1	A2h
1	1	0	A4h
1	1	1	A6h
0	X	X	Pin Mode



Equalization Setting (dB):

EQ1pin	EQ0pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
0	F	0	0	0	0	3.57	4.22	5.44	6.42	7.27	Default
0	1	0	0	0	1	3.83	4.56	5.93	7.04	8.00	
0	0	0	0	1	0	4.13	4.93	6.47	7.71	8.76	
0	R	0	0	1	1	4.41	5.29	6.95	8.29	9.42	
R	1	0	1	0	0	4.98	5.89	7.61	8.99	10.14	
R	F	0	1	0	1	5.25	6.23	8.05	9.50	10.70	
R	R	0	1	1	0	5.55	6.59	8.51	10.04	11.28	
R	0	0	1	1	1	5.82	6.92	8.93	10.51	11.78	
F	0	1	0	0	0	6.39	7.44	9.39	10.93	12.16	
F	R	1	0	0	1	6.63	7.74	9.76	11.34	12.60	
F	F	1	0	1	0	6.90	8.05	10.14	11.77	13.05	
F	1	1	0	1	1	7.14	8.34	10.49	12.15	13.44	
1	R	1	1	0	0	7.51	8.71	10.87	12.53	13.81	
1	0	1	1	0	1	7.74	8.97	11.18	12.87	14.15	
1	1	1	1	1	0	7.98	9.25	11.51	13.23	14.51	
1	F	1	1	1	1	8.20	9.51	11.81	13.54	14.82	

ReDriver Loading Detection Enable Pin



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<Variant Name>

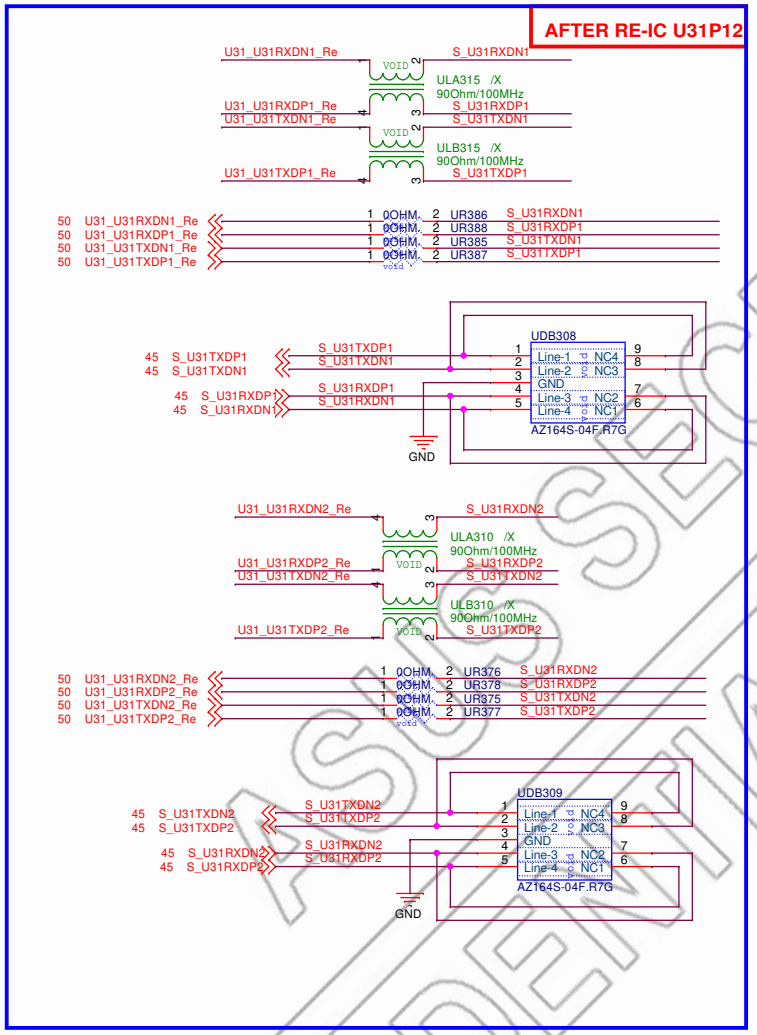
ASUSTeK COMPUTER INC.

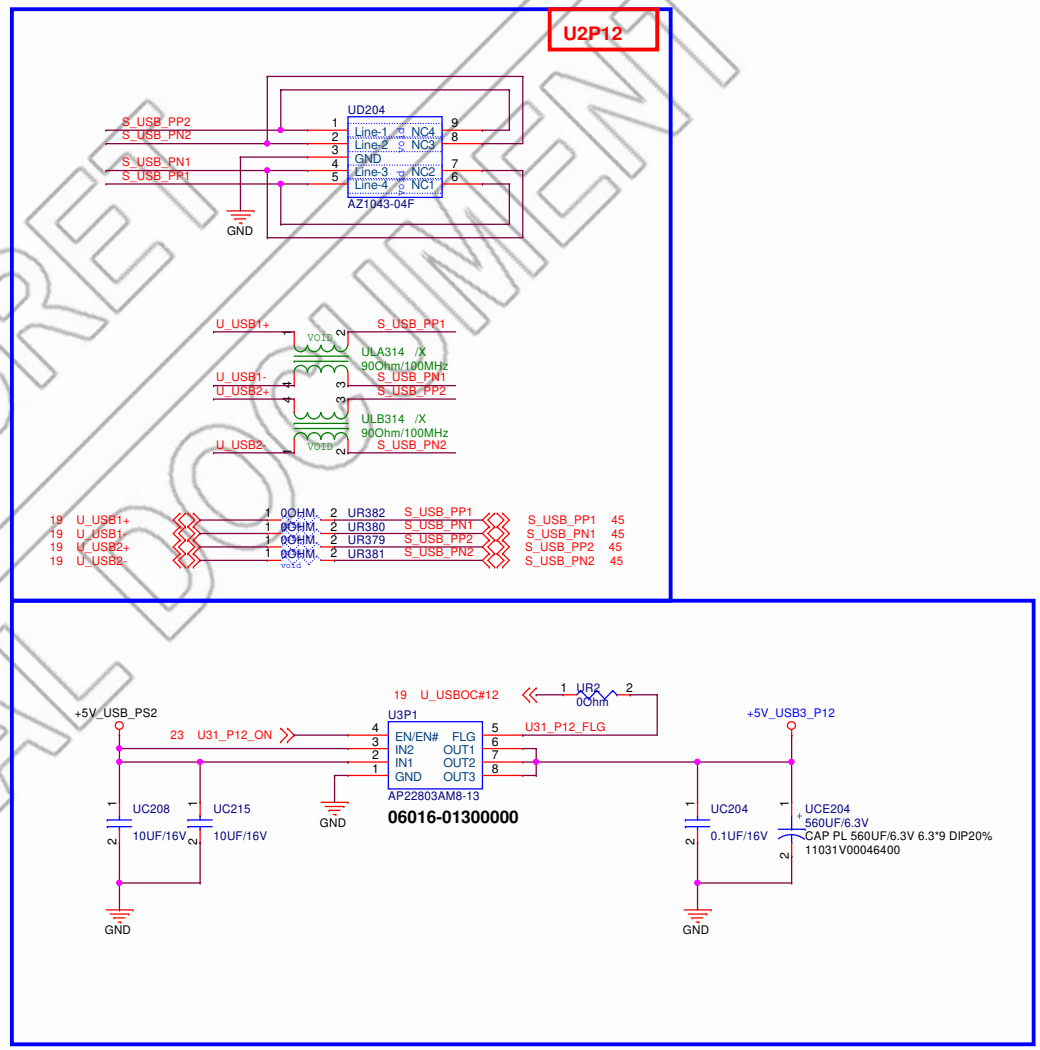
Title : U31 Port 6 Re-driver IC

Engineer: IPC-EE3

Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 53 of 86

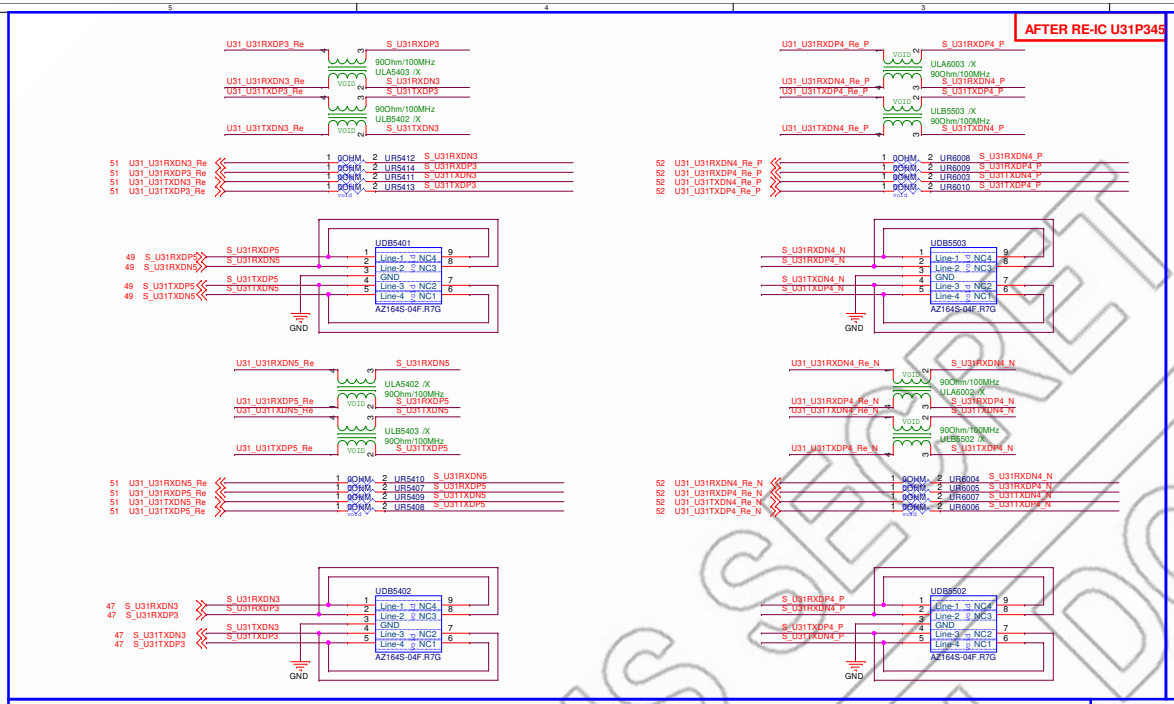


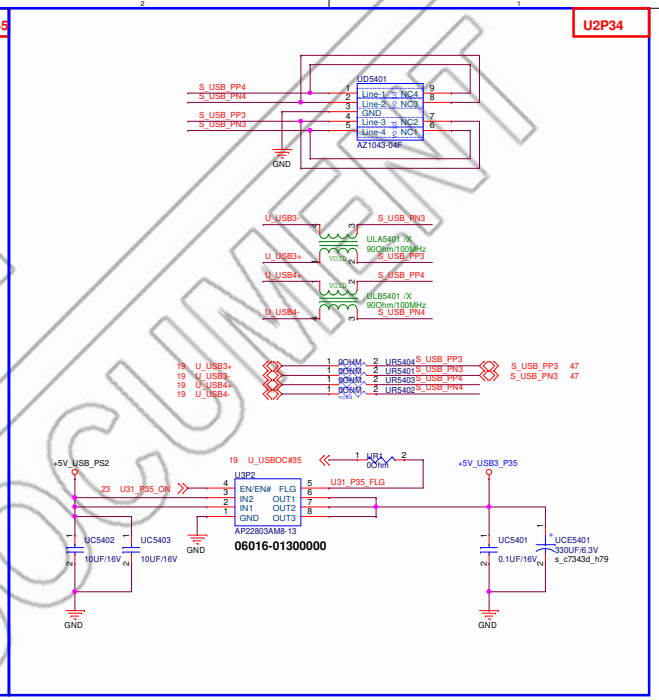


CONFIDENTIAL DOCUMENT
ASUS SECRET

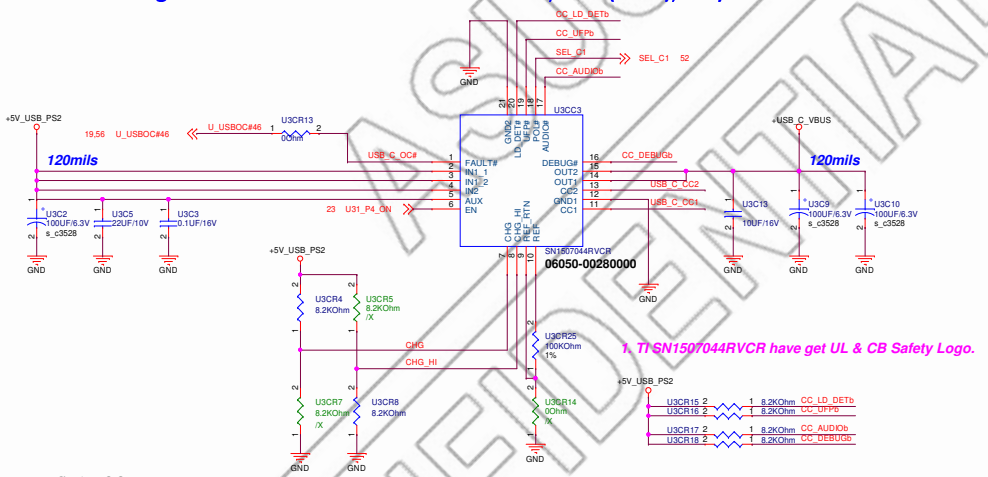
<Variant Name>

ASUS	Title : U31_Port1,2	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 54 of 86	

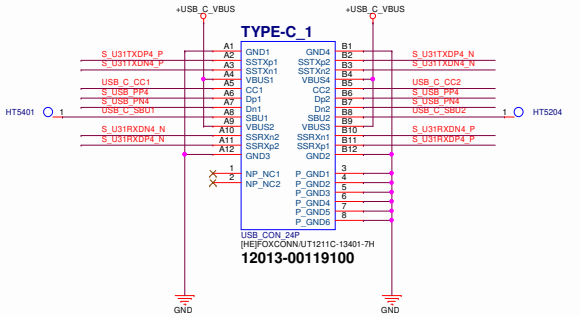




TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A



1. TI SN1507044RVCR have get UL & CB Safety Logo.



Set CC
I limit = 1.7A

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

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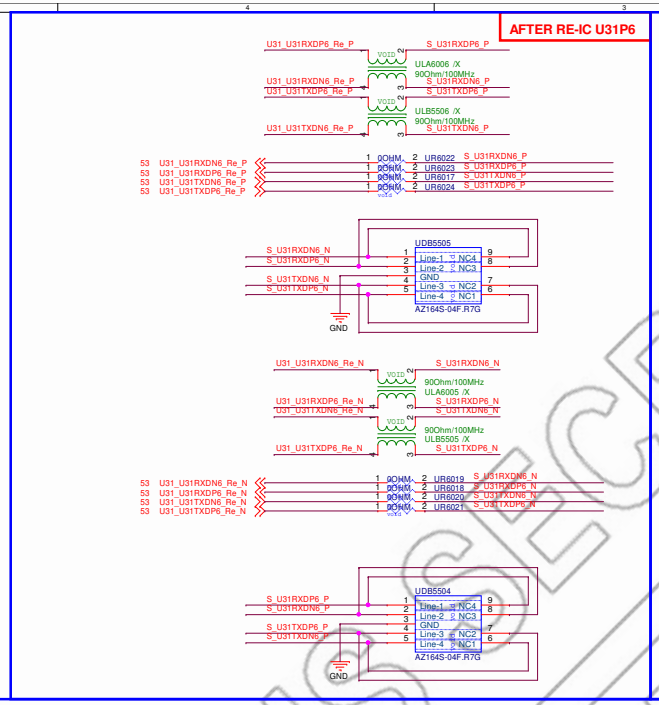
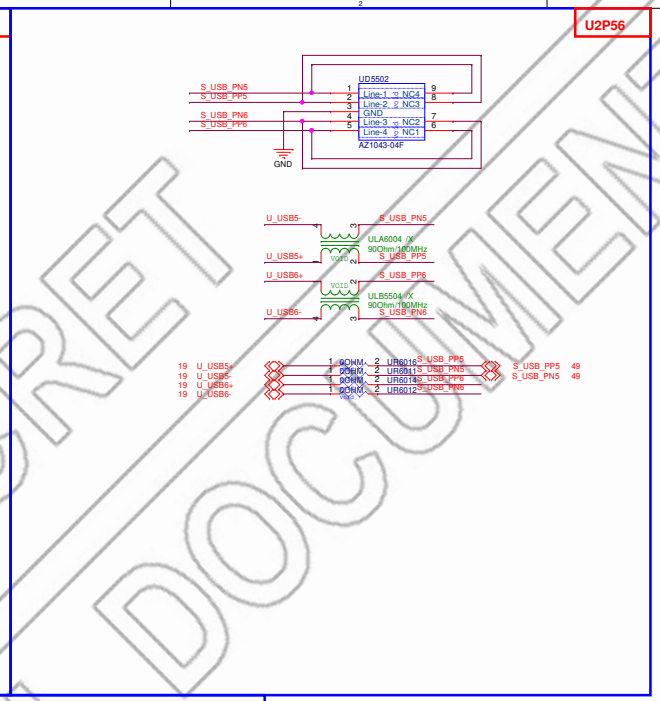
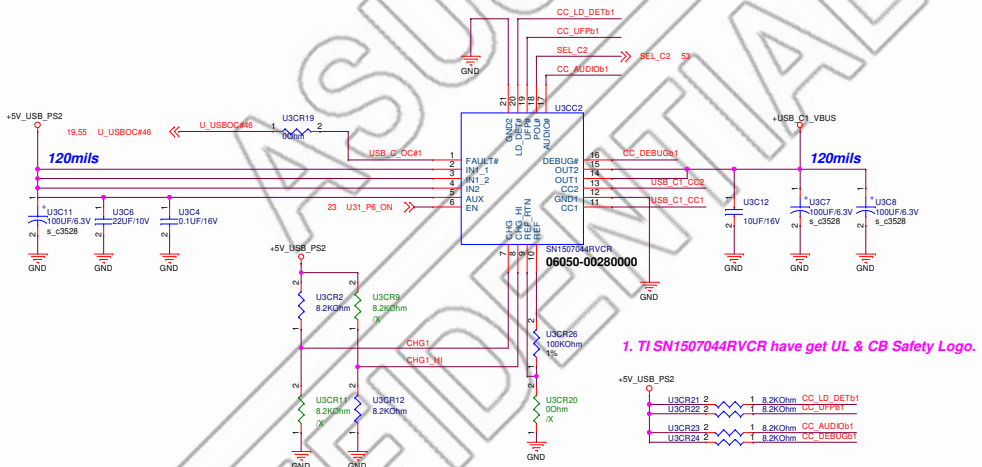
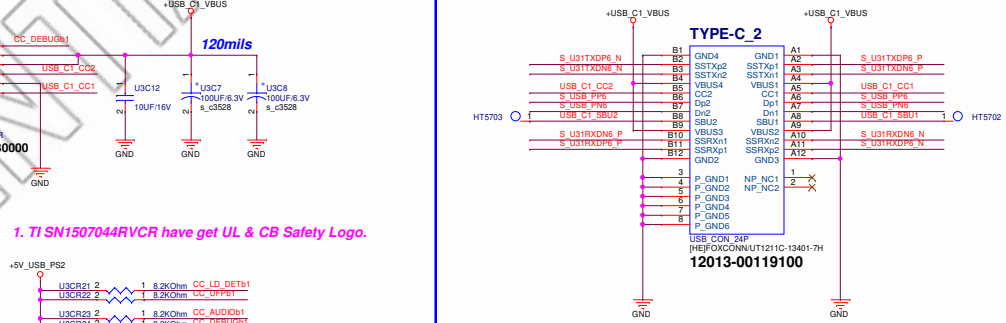




TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A



1. TI SN1507044RVCR have get UL & CB Safety Logo.



Set CC
I limit = 1.7A

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

ASUS SECRET
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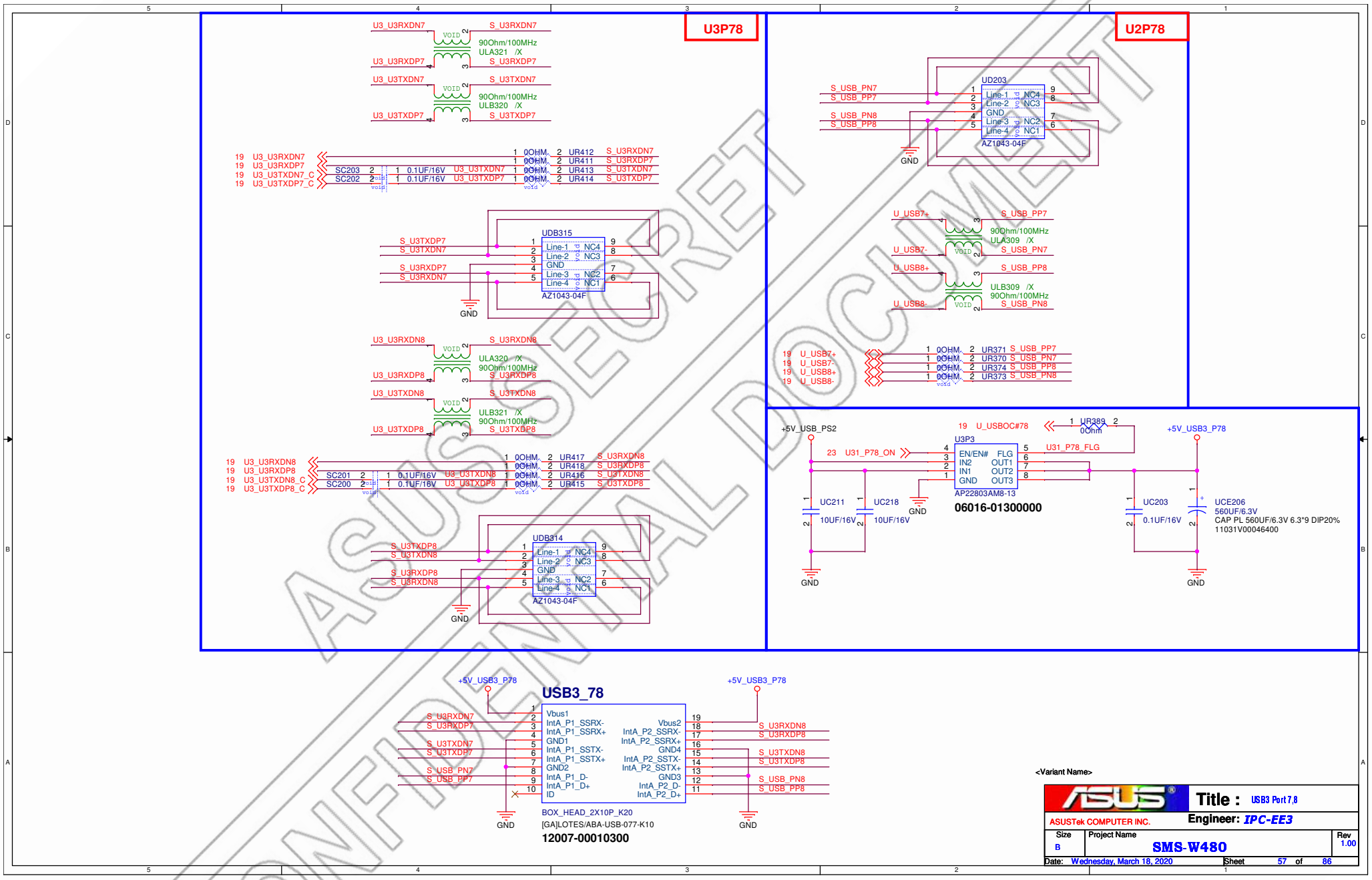
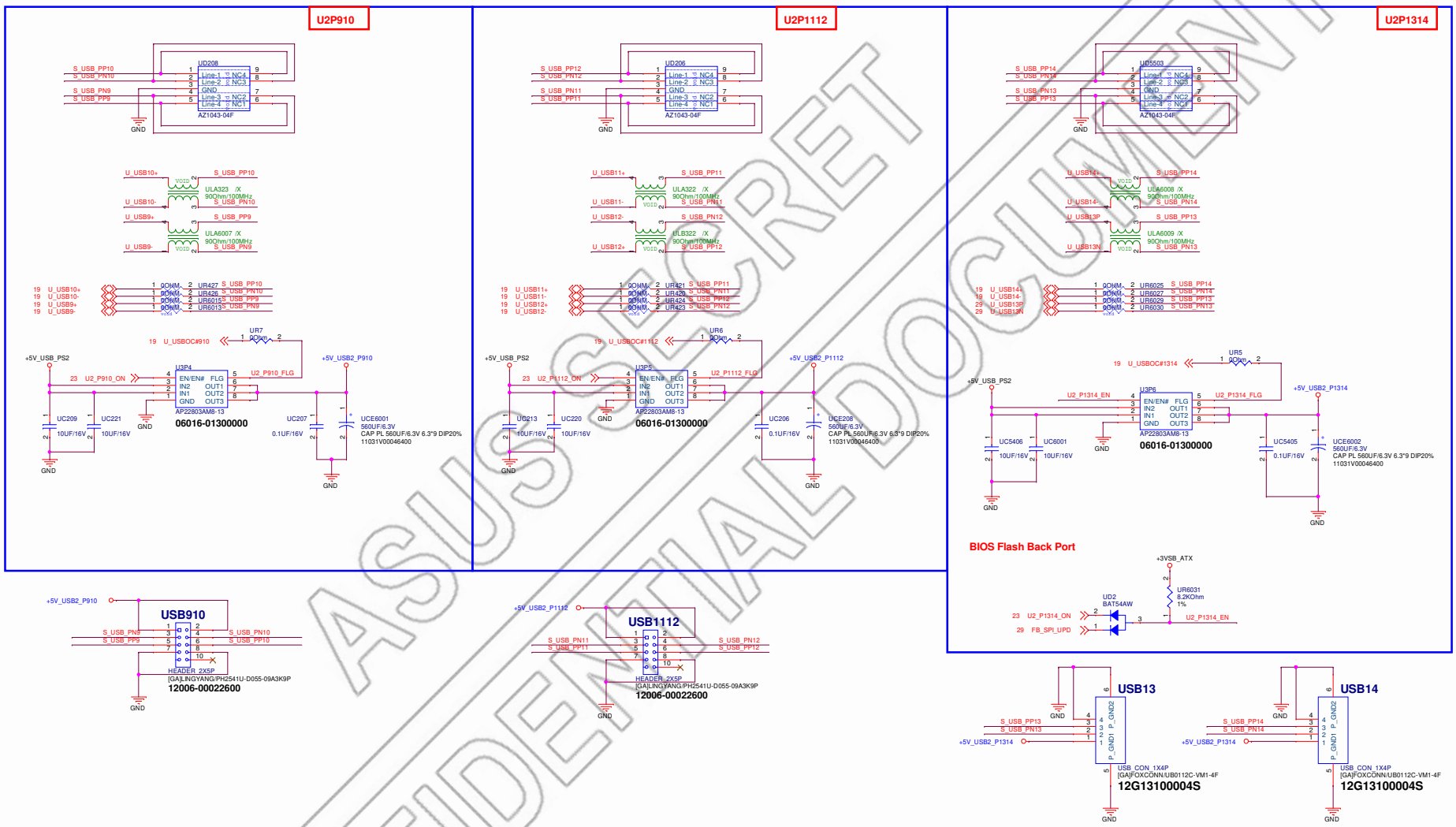


ASUS SECRET
CONFIDENTIAL DOCUMENT



CONFIDENTIAL DOCUMENT
ASUS SECRET

<Variant Name>

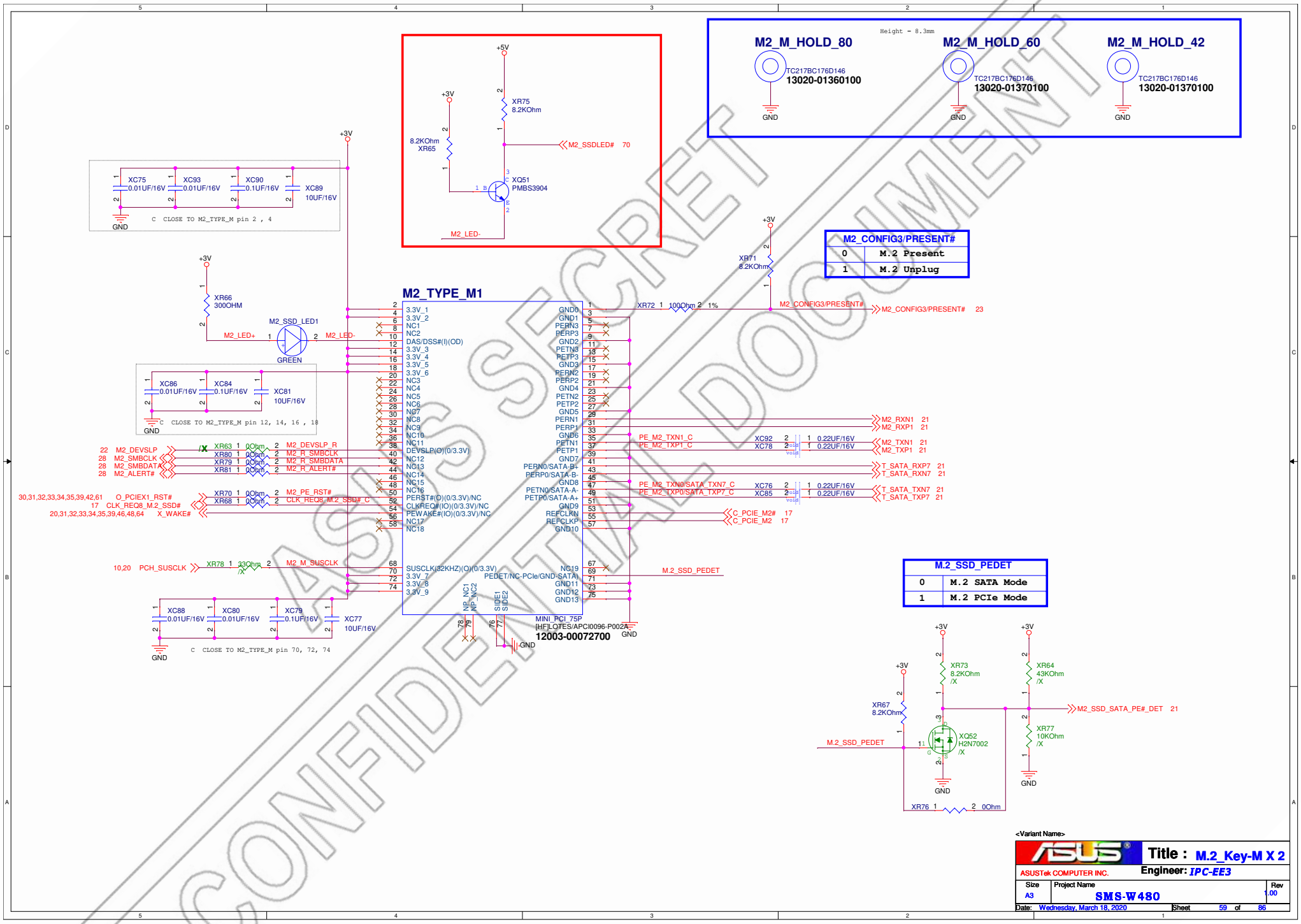
ASUSTeK Computer Inc.

Title: USB2 Port X 6 Internal

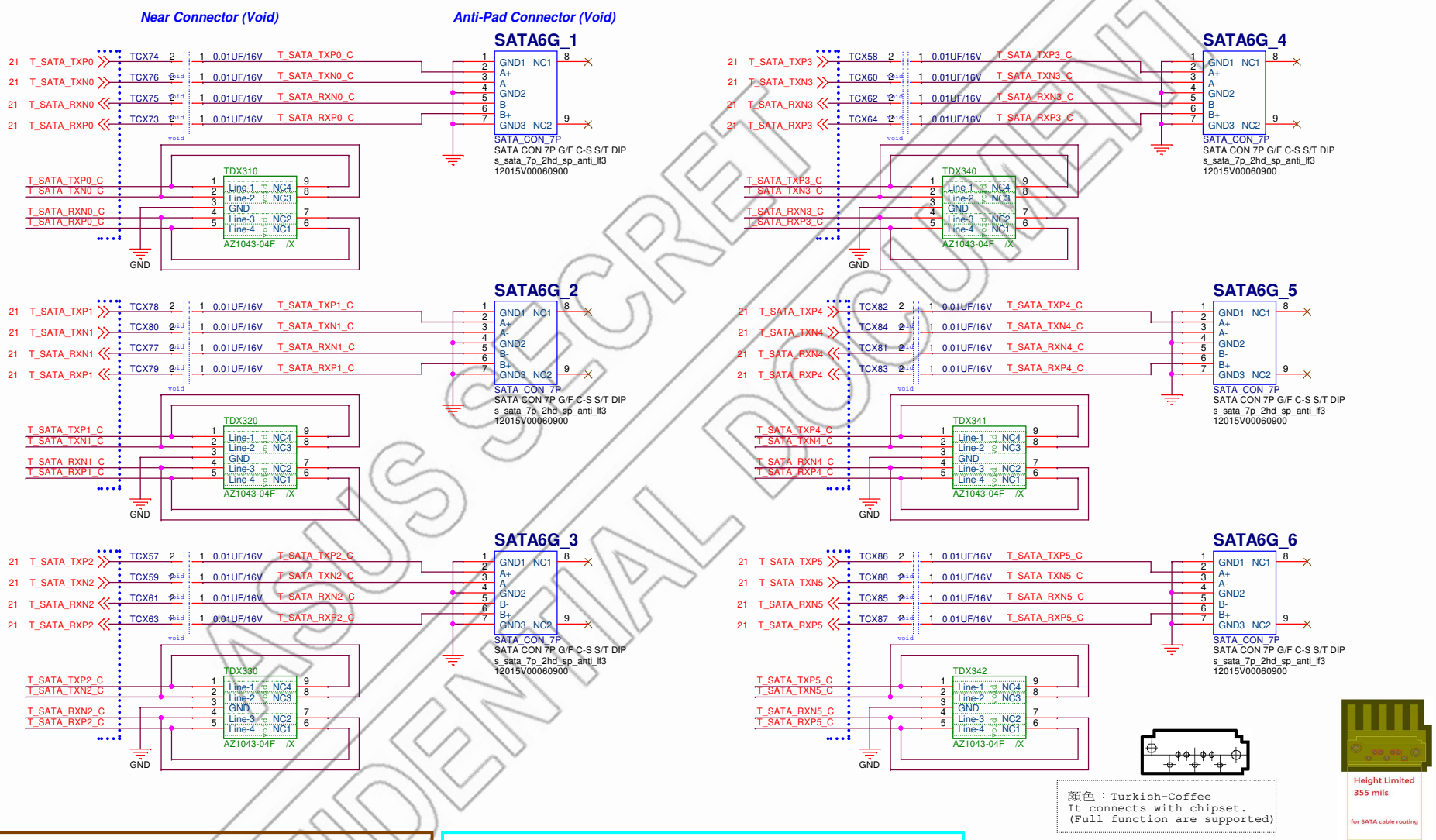
Engineer: IPC-EE3

Size	Project Name	Rev
C	SMS-W480	1.00

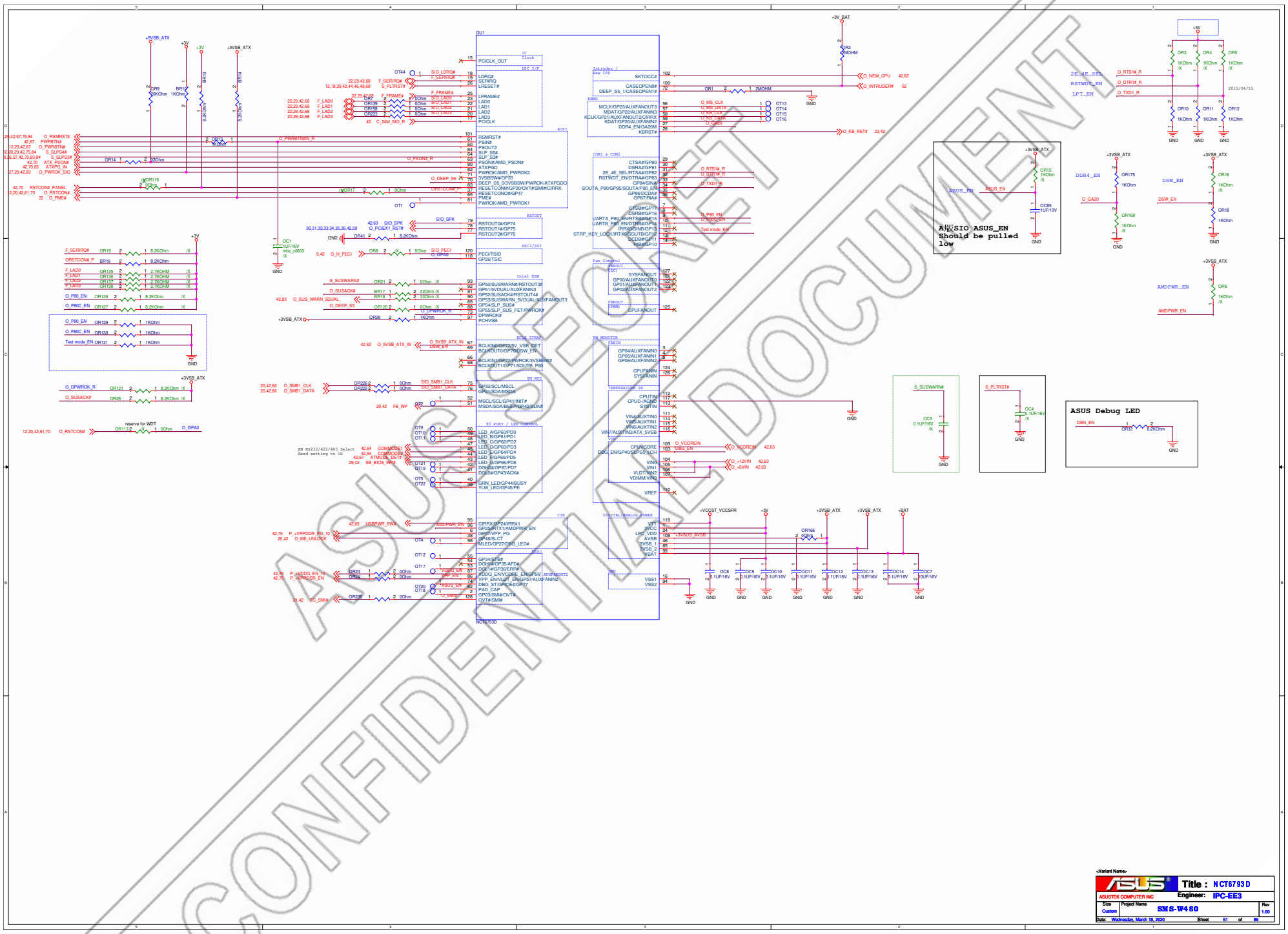
Date: Wednesday, March 18, 2020 Sheet 58 of 86



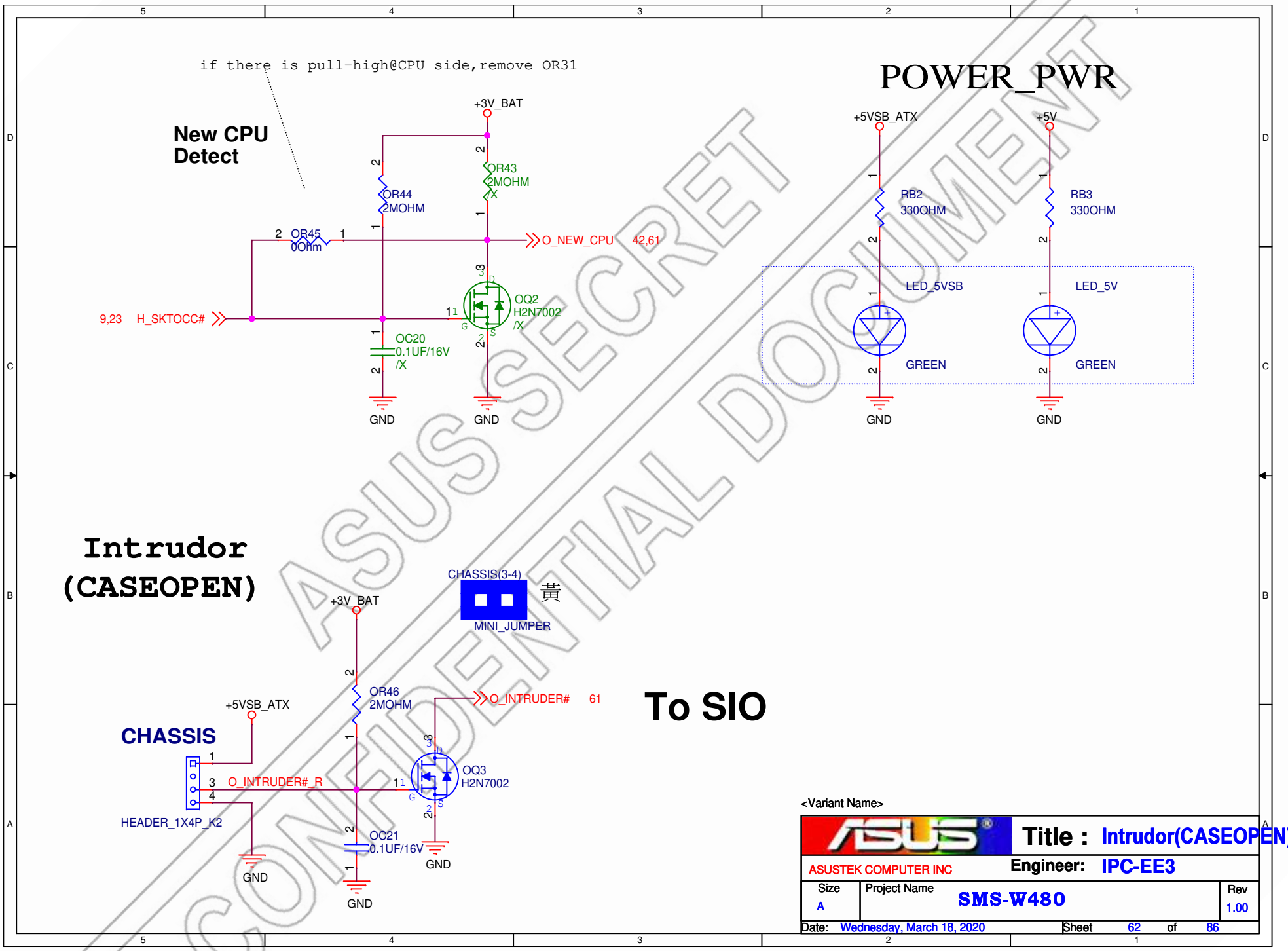
ASUS SECRET
CONFIDENTIAL DOCUMENT

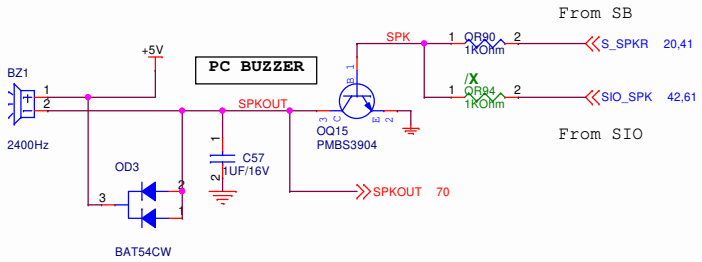


ASUS SECRET
CONFIDENTIAL DOCUMENT

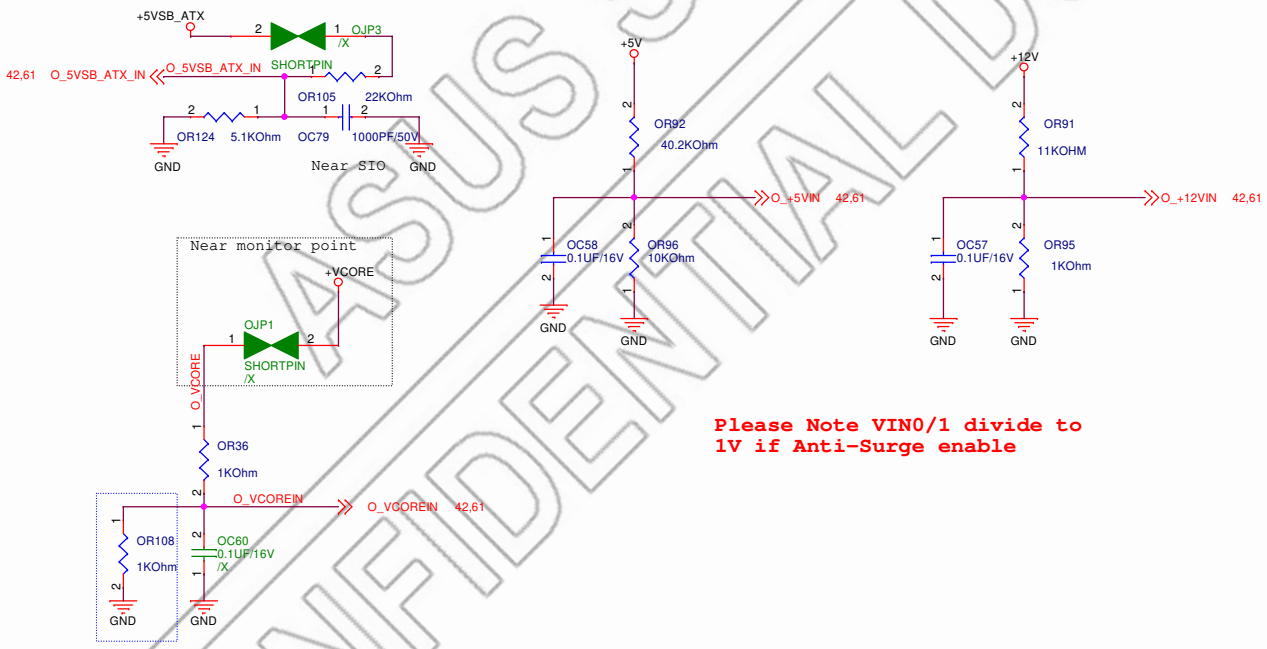


CONFIDENTIAL DOCUMENT


if there is pull-high@CPU side,remove OR31
New CPU Detect
+3V_BAT
OR43
2MOHM
/X
OR44
2MOHM
OR45
0Ohm
O_NEW_CPU
42,61
OQ2
H2N7002
/X
9,23
H_SKTOCC#
OC20
0.1UF/16V
/X
GND
GND
POWER_PWR
+5VSB_ATX
+5V
RB2
330OHM
RB3
330OHM
LED_5VSB
LED_5V
GREEN
GREEN
GND
GND
Intrudor
(CASEOPEN)
CHASSIS(3-4)
黄
MINI_JUMPER
+3V_BAT
OR46
2MOHM
O_INTRUDER#
61
To SIO
+5VSB_ATX
CHASSIS
O_INTRUDER#_R
OQ3
H2N7002
HEADER_1X4P_K2
OC21
0.1UF/16V
GND
GND
GND
ASUS SECRET
CONFIDENTIAL DOCUMENT
<Variant Name>
Title : Intrudor(CASEOPEN)
ASUSTEK COMPUTER INC
Engineer: IPC-EE3
Size
A
Project Name
SMS-W480
Rev
1.00
Date: Wednesday, March 18, 2020
Sheet 62 of 86



Voltage Monitor



Please Note VIN0/1 divide to 1V if Anti-Surge enable

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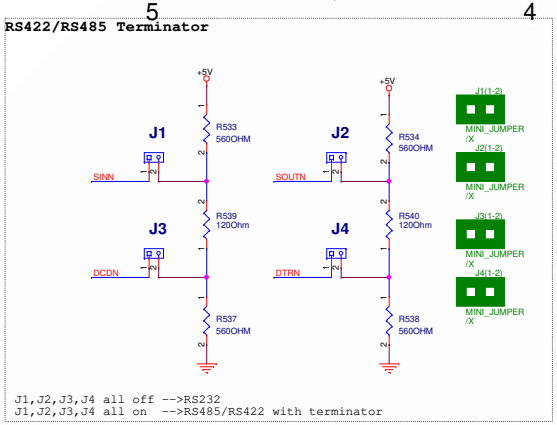
<Variant Name>

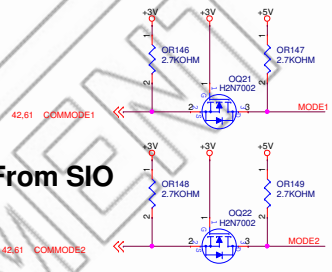
ASUS	Title : HW MONITOR	
ASUSTEK COMPUTER INC	Engineer: IPC-EE3	
Size B	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 63 of 86	



Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ.
As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.

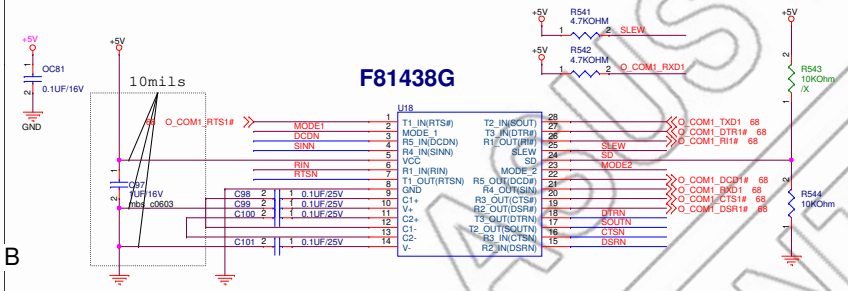


(VDD = +5.0V ± 5%)

Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01.		2	30	mA
Supply Current (RS-485)	No Load, MODE = 10, 11.		2		mA
Supply Current (RS-422)	MODE = 00.		2		mA
Operating Temperature *	Symbol: T	-40		85	◦ C

(VDD = +5.0V ± 5%)

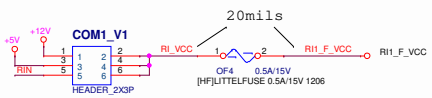
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V_{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	μA	
Driver Input Pull High Current	I_{IT}			±15	μA	

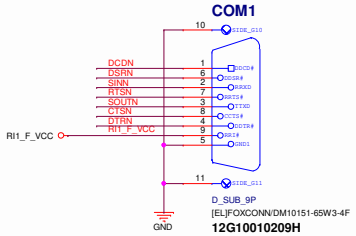


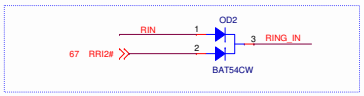
COM1_V1(5-6)	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

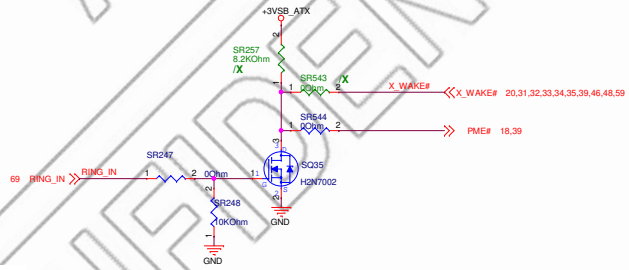
COM1_V1(5-6)

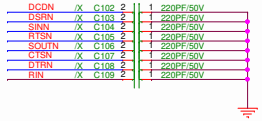
MINI_JUMPER



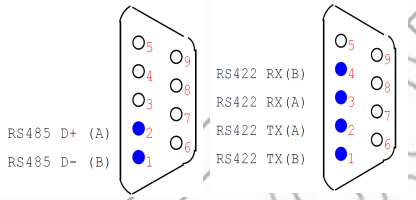




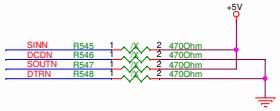




Close to COM port connector



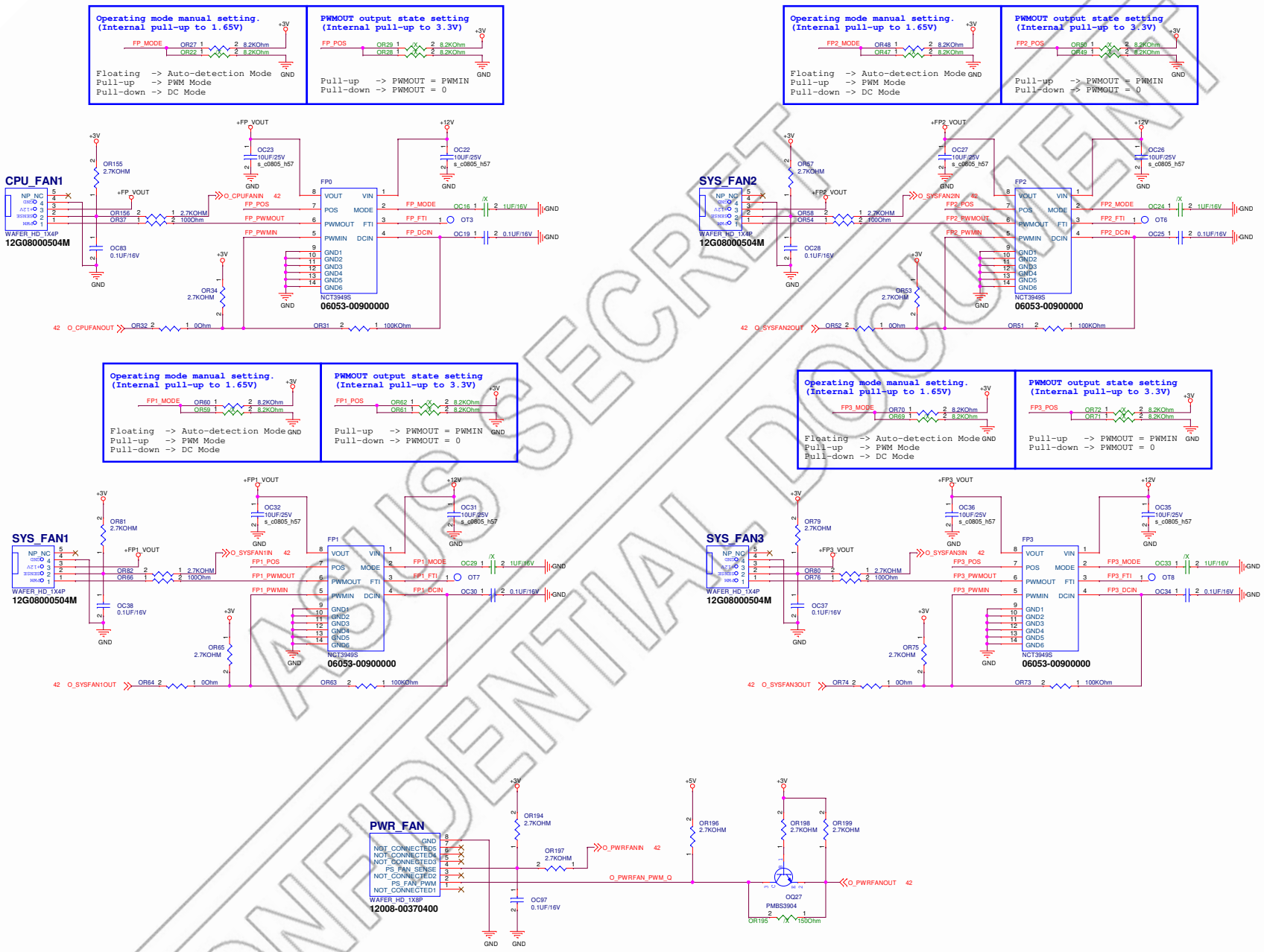
Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps



Note:Reserved for FAIL-SAVE

ASUS SECRET CONFIDENTIAL DOCUMENT

<Variant Name>
ASUSTEK COMPUTER INC
Title : COM1_RS232/422/485
Engineer: IPC-EE3
Size Custom
Project Name SMS-W480
Rev 1.00
Date: Wednesday, March 18, 2020
Sheet 64 of 86



CONFIDENTIAL DOCUMENT
ASUS SECRET

<Variant Name>

ASUS

ASUSTEK COMPUTER INC

Title : CPU/SYS/PWR_FAN

Engineer: IPC-EE3

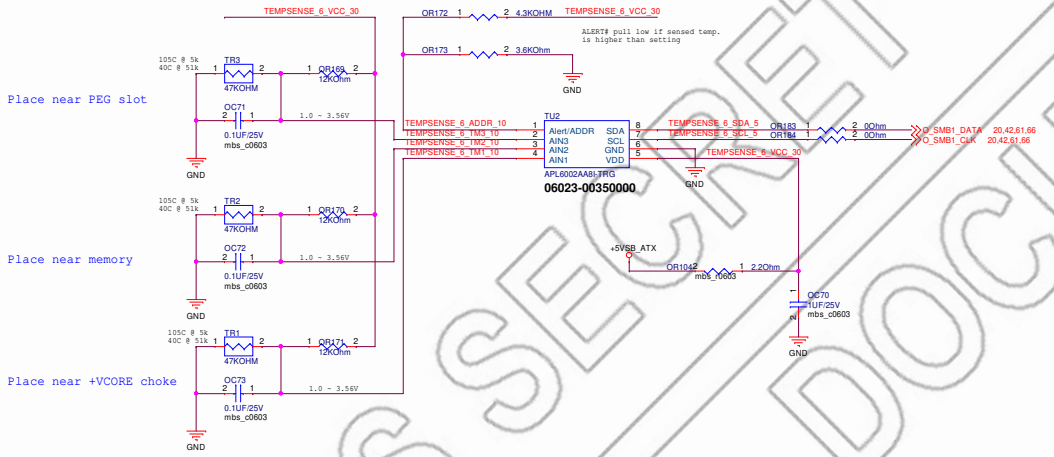
Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 65 of 86

For EC

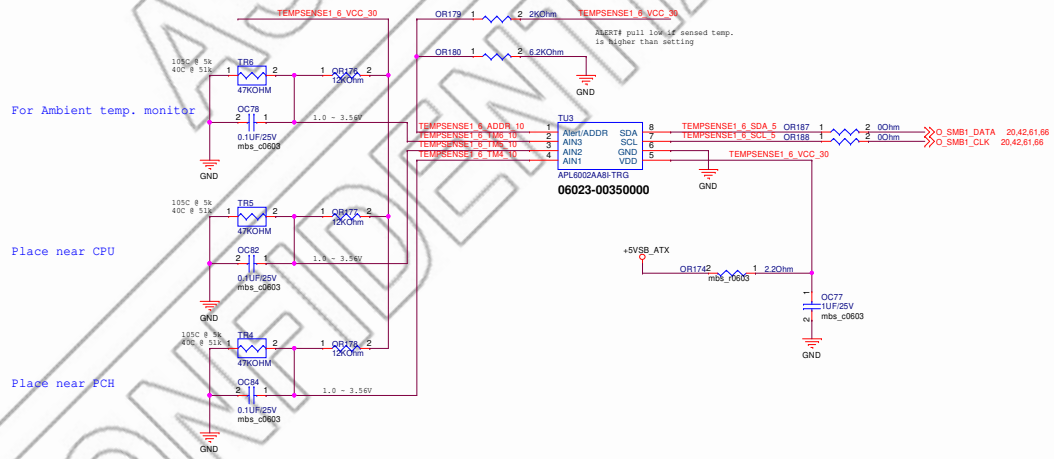
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
OR172	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
OR173	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
OR179	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
OR180	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



ASUS SECRET
CONFIDENTIAL DOCUMENT

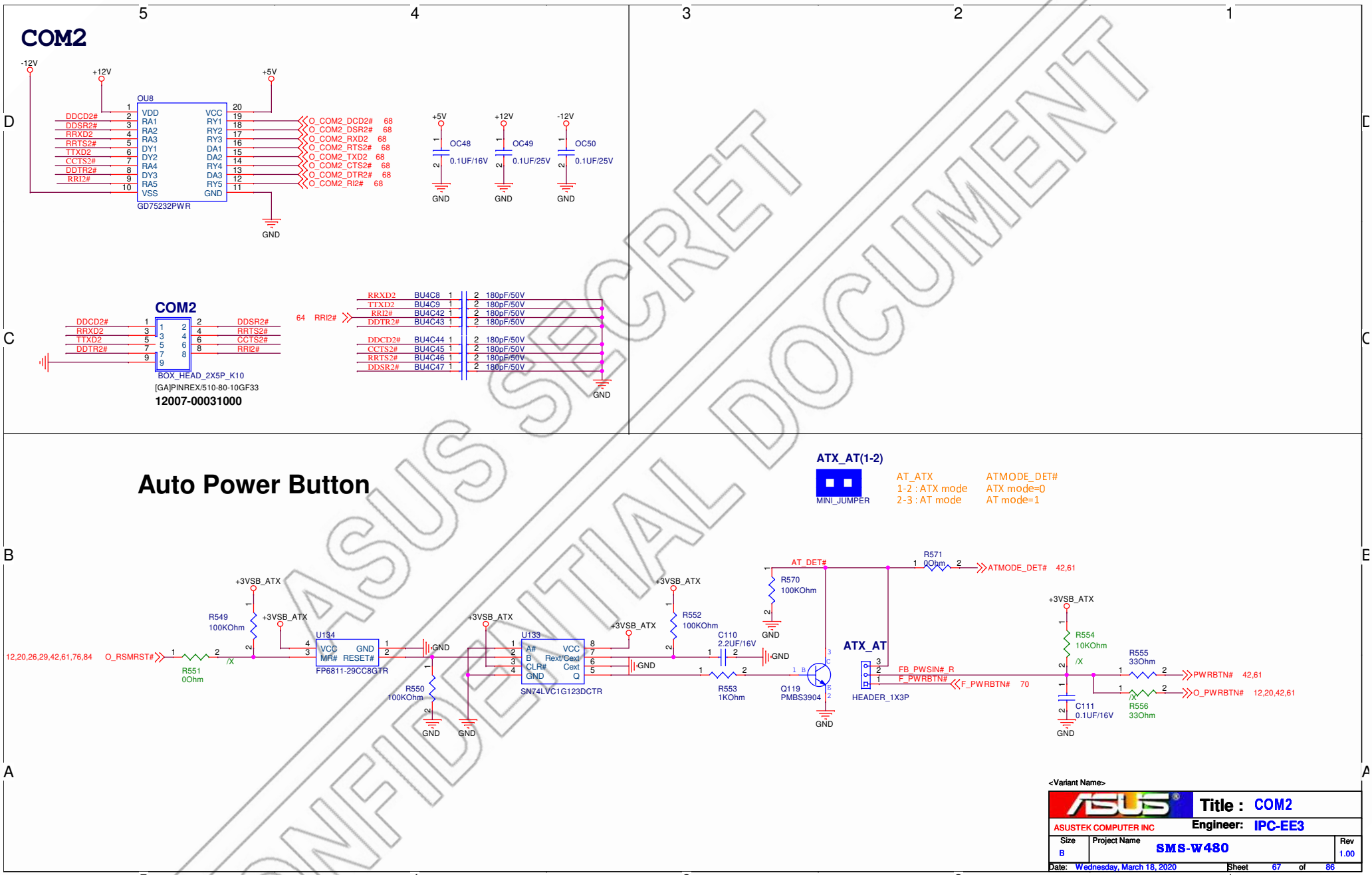
ASUSTEK COMPUTER INC

Title : Thermal Sensor

Engineer: IPC-EE3

Size	Project Name	Rev
C	SMS-W480	1.00

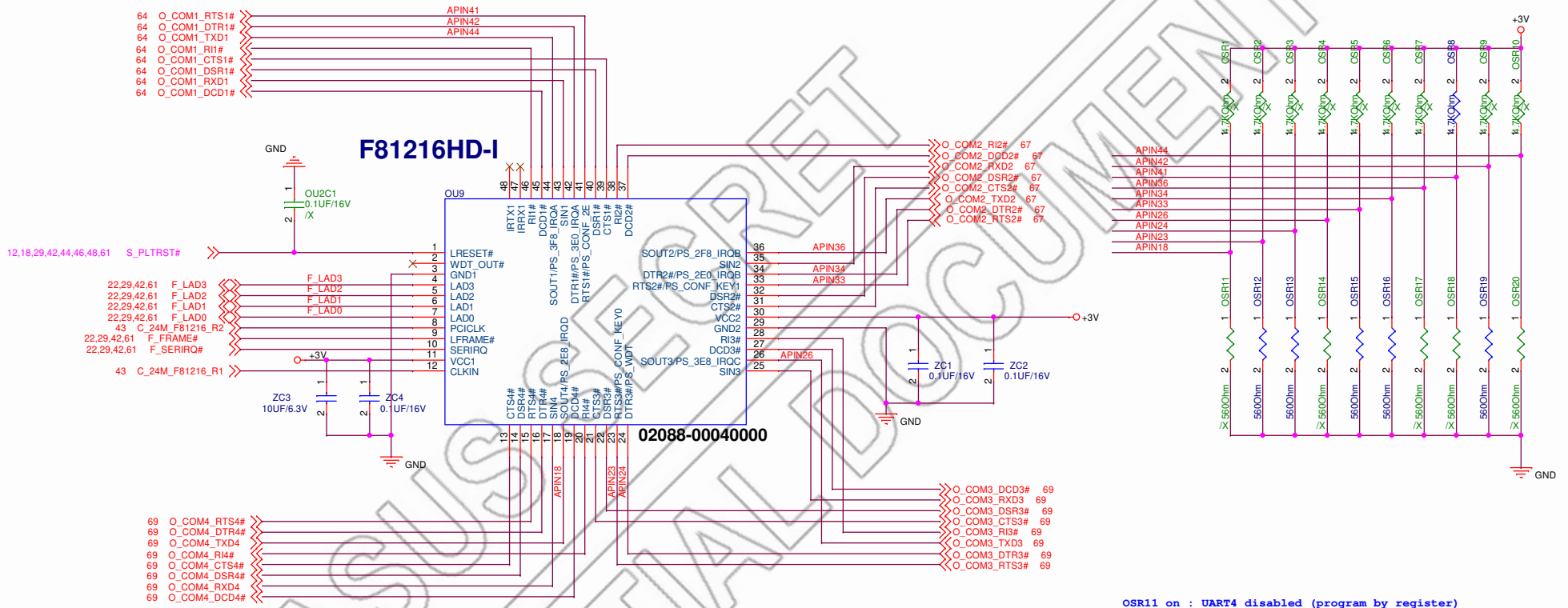
Date: Wednesday, March 18, 2020 Sheet 66 of 86



CONFIDENTIAL DOCUMENT
ASUS SECRET

<Variant Name>

ASUSTEK COMPUTER INC	Title : COM2
	Engineer: IPC-EE3
Size B	Project Name SMS-W480
	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 67 of 86



OSR15	OSR12	OSR18	Address	Entry Key
0	0	0	0x4e/0x4f	0x77
0	0	1	0x2e/0x2f	0x77
0	1	0	0x4e/0x4f	0xa0
0	1	1	0x2e/0x2f	0xa0
1	0	0	0x4e/0x4f	0x87
1	0	1	0x2e/0x2f	0x87
1	1	0	0x4e/0x4f	0x87
1	1	1	0x2e/0x2f	0x87

OSR11 on : UART4 disabled (program by register)
OSR11 off : UART 4 address : 0x2e8 IRQ9

OSR14 on : UART3 disabled (program by register)
OSR14 off : UART 3 address : 0x3e8 IRQ5

OSR16 on and OSR17 off : UART 2 address : 0x2f8 IRQ4
OSR16 off and OSR17 on : UART 2 address : 0x2e0 IRQ4;
OSR16 and OSR17 on :UART 2 disabled (program by register).

OSR19 on and OSR20 off : UART 1 address : 0x3f8 IRQ3;
OSR19 off and OSR20 on : UART 1 address : 0x3e0 IRQ3;
OSR19 and OSR20 on :UART 1 disabled (program by register).

OSR13 on : disabled
OSR13 off : Watch Dog Timer enabled and setting to 10 second when the clock input is 24Mhz. If the clock input is 48Mhz , the timer is setting to 5 second.

<Variant Name>

ASUSTEK COMPUTER INC

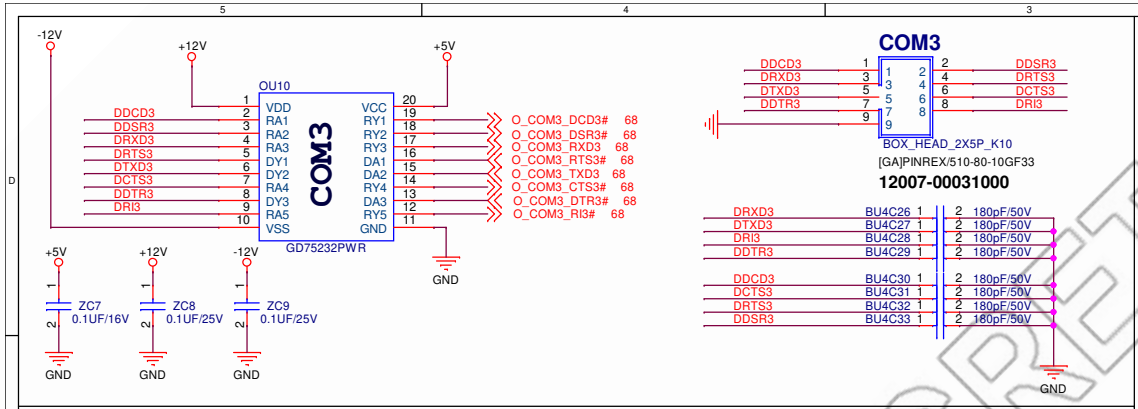
Title : F81216 COM

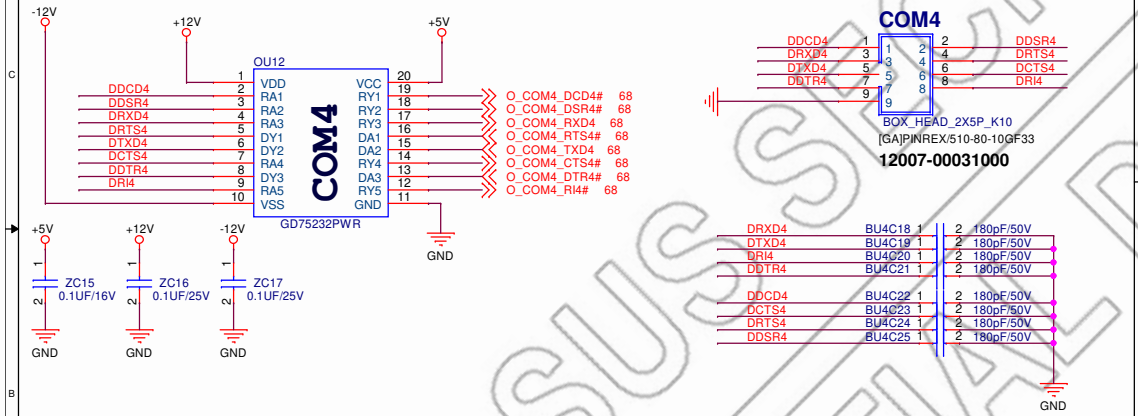
Engineer: IPC-EE3

Size	Project Name	Rev
B	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 68 of 86

ASUS SECRET
CONFIDENTIAL DOCUMENT



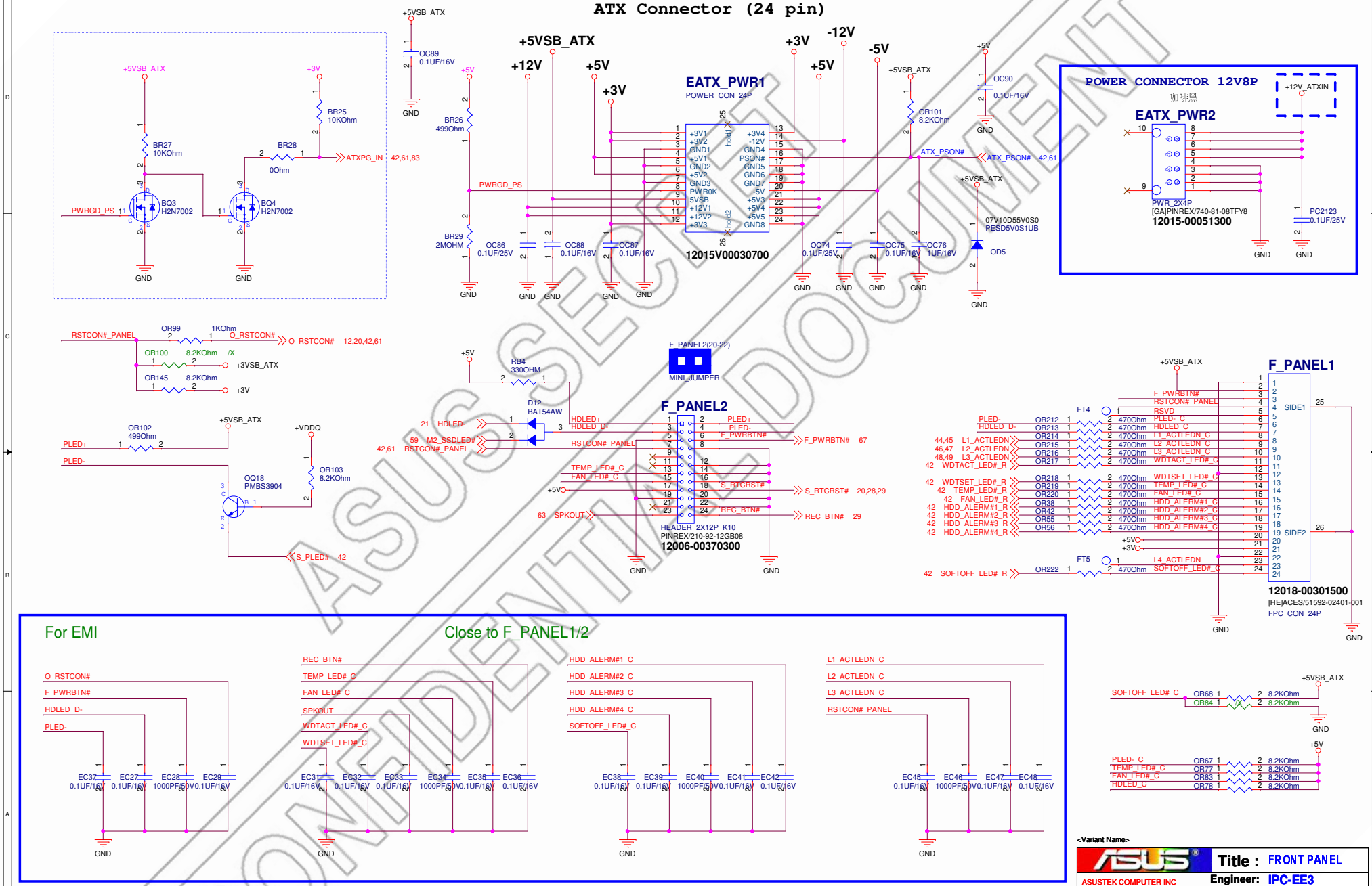


ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS	Title : COM3-4	
ASUSTEK COMPUTER INC	Engineer: IPC-EE3	
Size B	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 69 of 86	

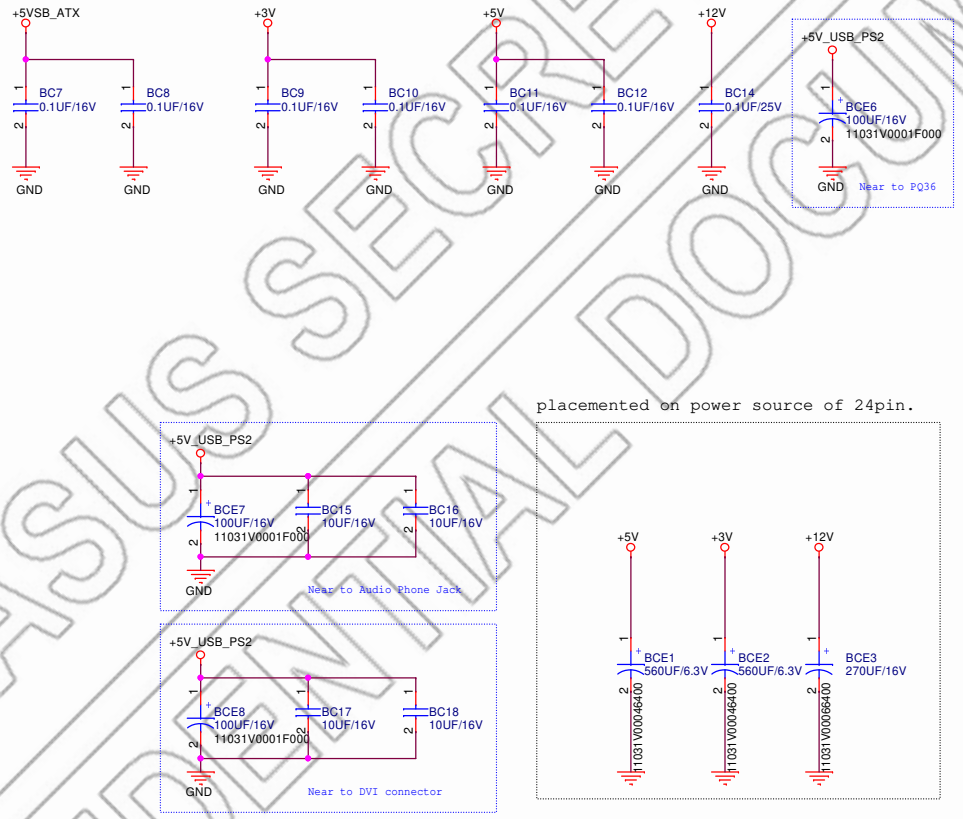
ATX Connector (24 pin)



<Variant Name>

ASUSTEK COMPUTER INC	Title : FRONT PANEL	
	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 70 of 86	

Bypass/EMI Capacitor

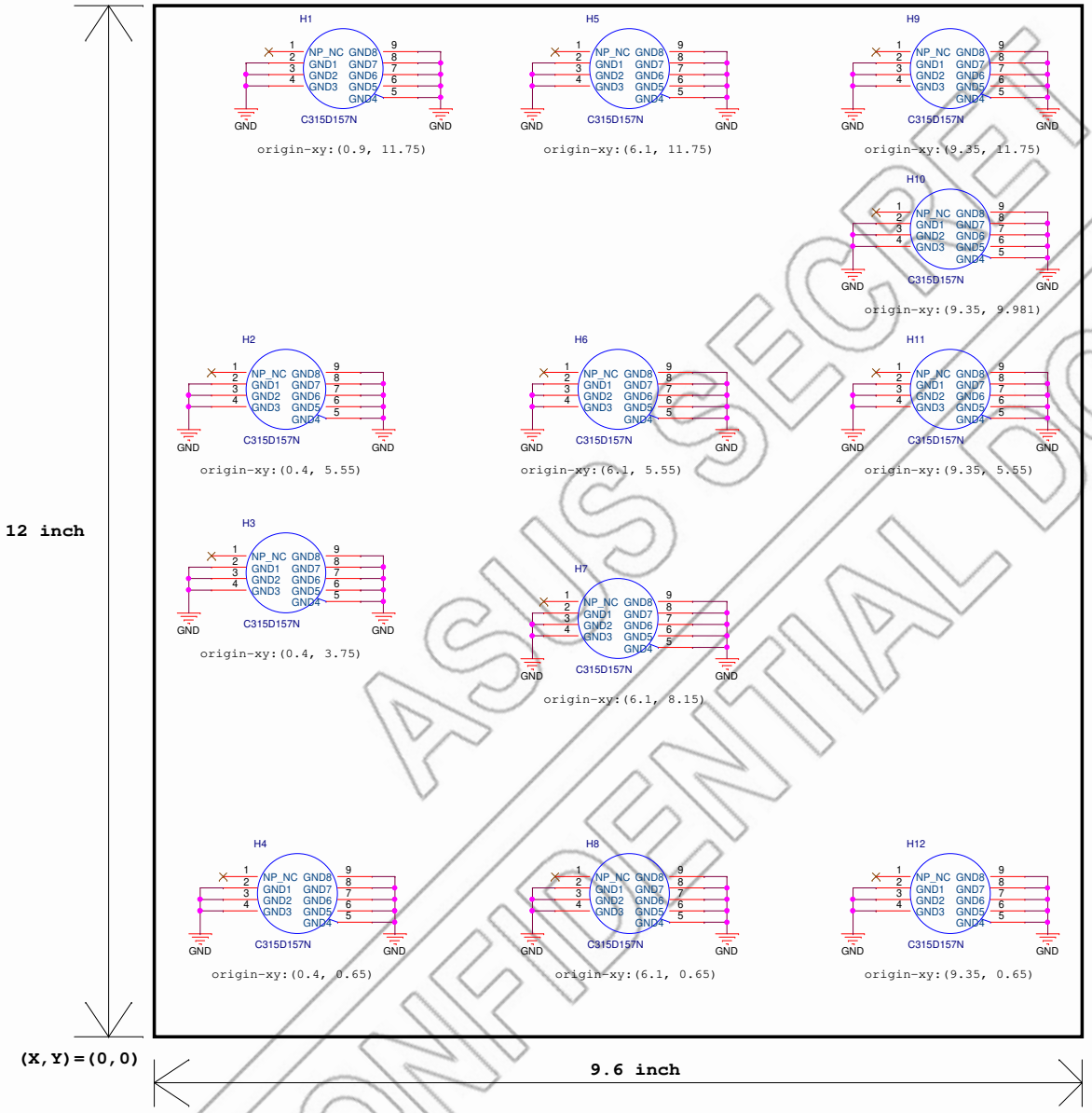


ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS	Title : EMICap	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 71 of 86	

ATX Screw Hole

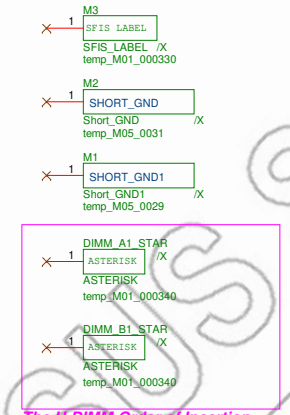


ASUS SECRET
CONFIDENTIAL DOCUMENT

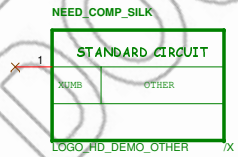
<Variant Name>

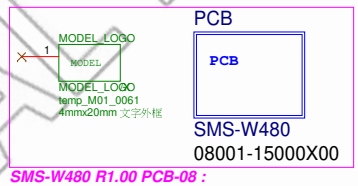
ASUS	Title : Screw Hole	
ASUSTEK COMPUTER INC	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 72 of 86	

Selling Point



The U-DIMM Order of Insertion





SMS-W480 R1.00 PCB-08 :

R1.00 PCB_ : 08001-15000000 DF 12*9.6,6L(1)1.6,1080

R1.00 PCB_ : 08001-15000200 TRUSTECH 12*9.6,6L(1)1.6,1080

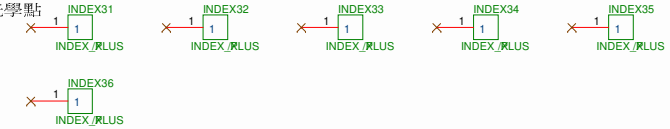
R1.00 PCB_ : 08001-15000400 VICTORY 12*9.6,6L(1)1.6,1080

Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

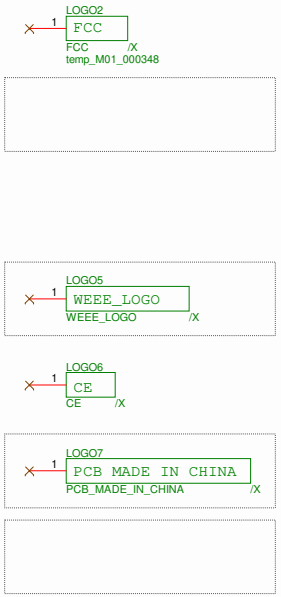
小顆十字光學點



2012/09/11

Logo

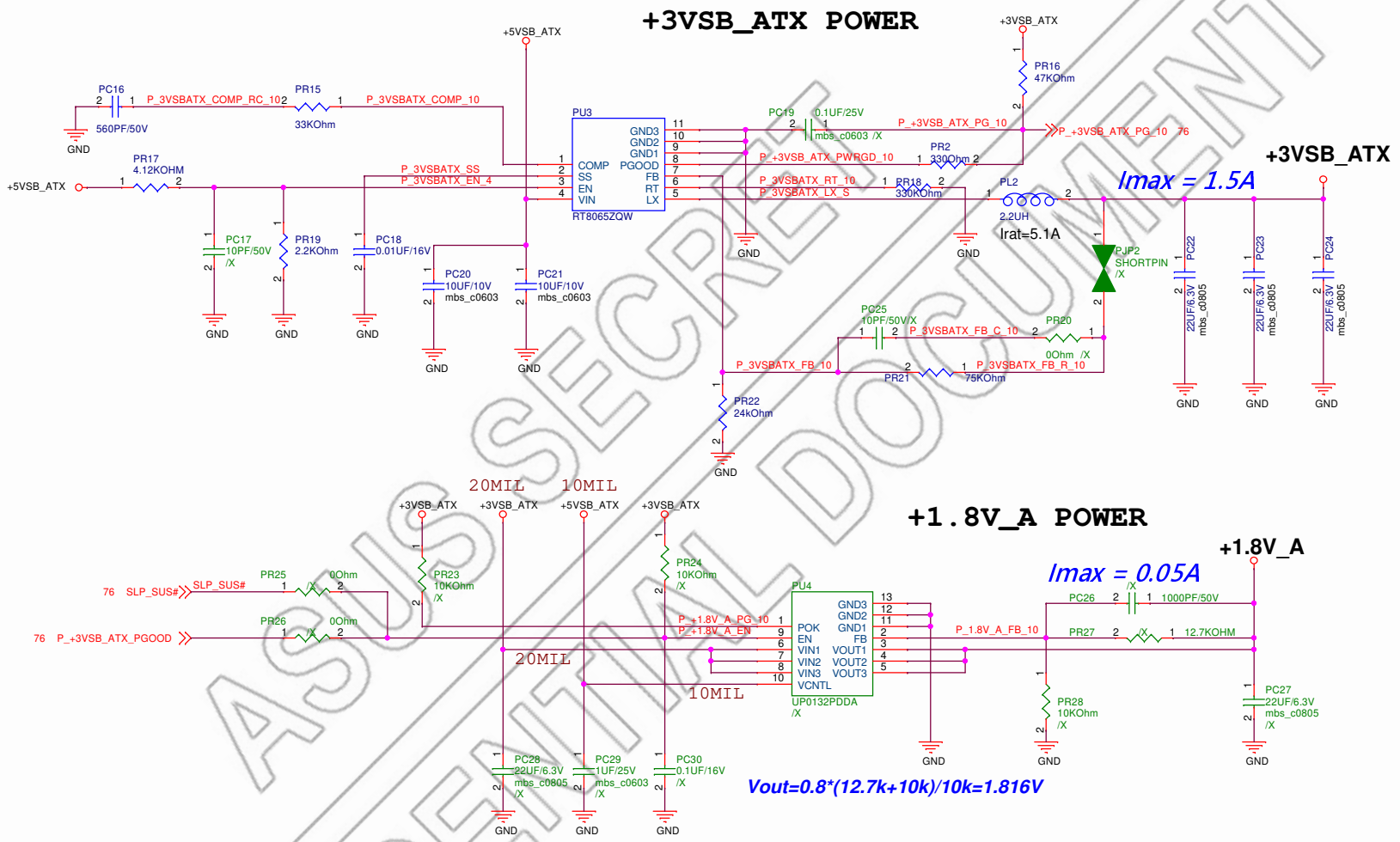
common Logo for all projects



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

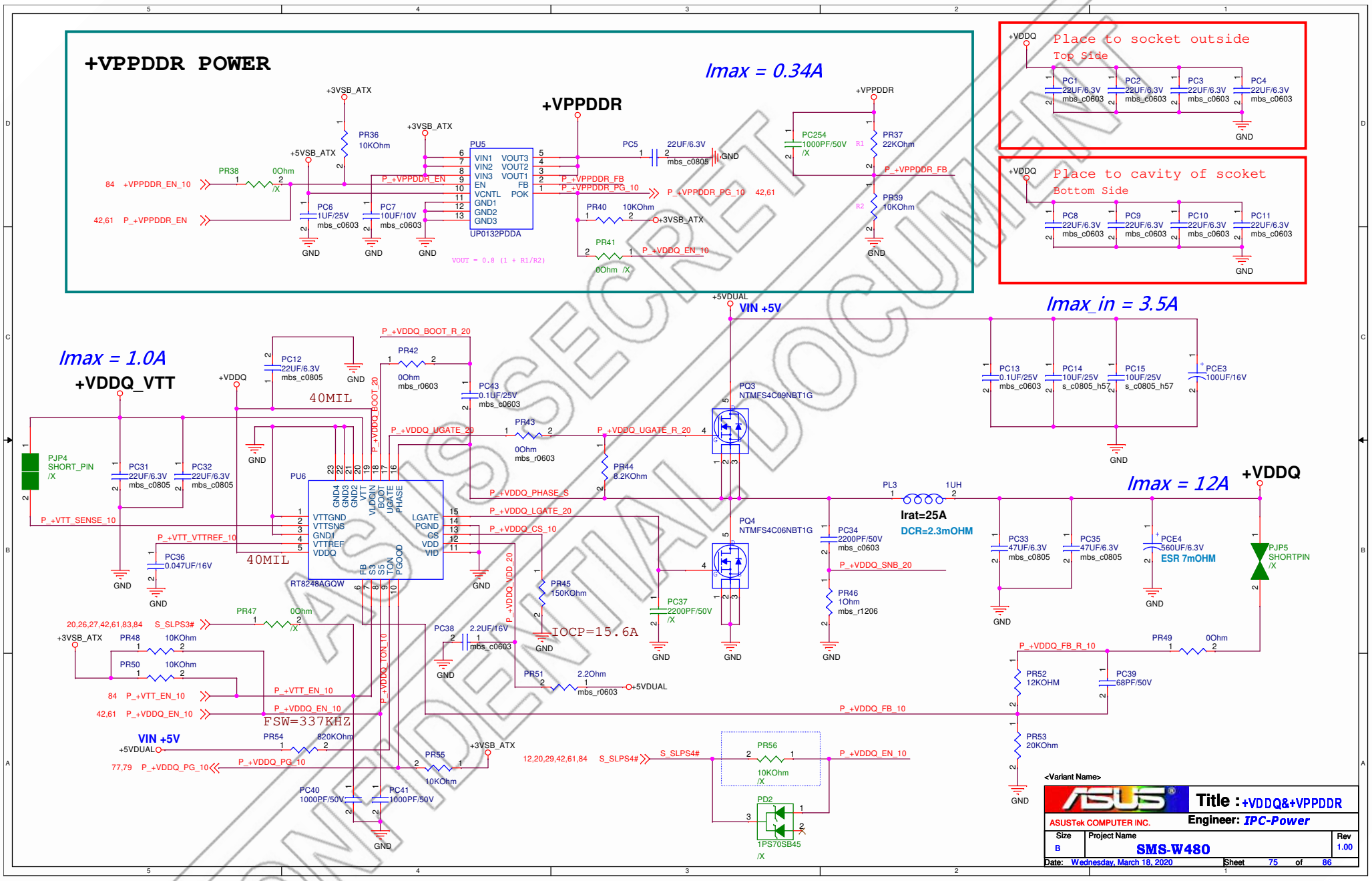
ASUSTEK COMPUTER INC	Title : Selling Point_Logo	
	Engineer: IPC-EE3	
Size A3	Project Name SMS-W480	Rev 1.00
Date: Wednesday, March 18, 2020	Sheet 73 of 86	

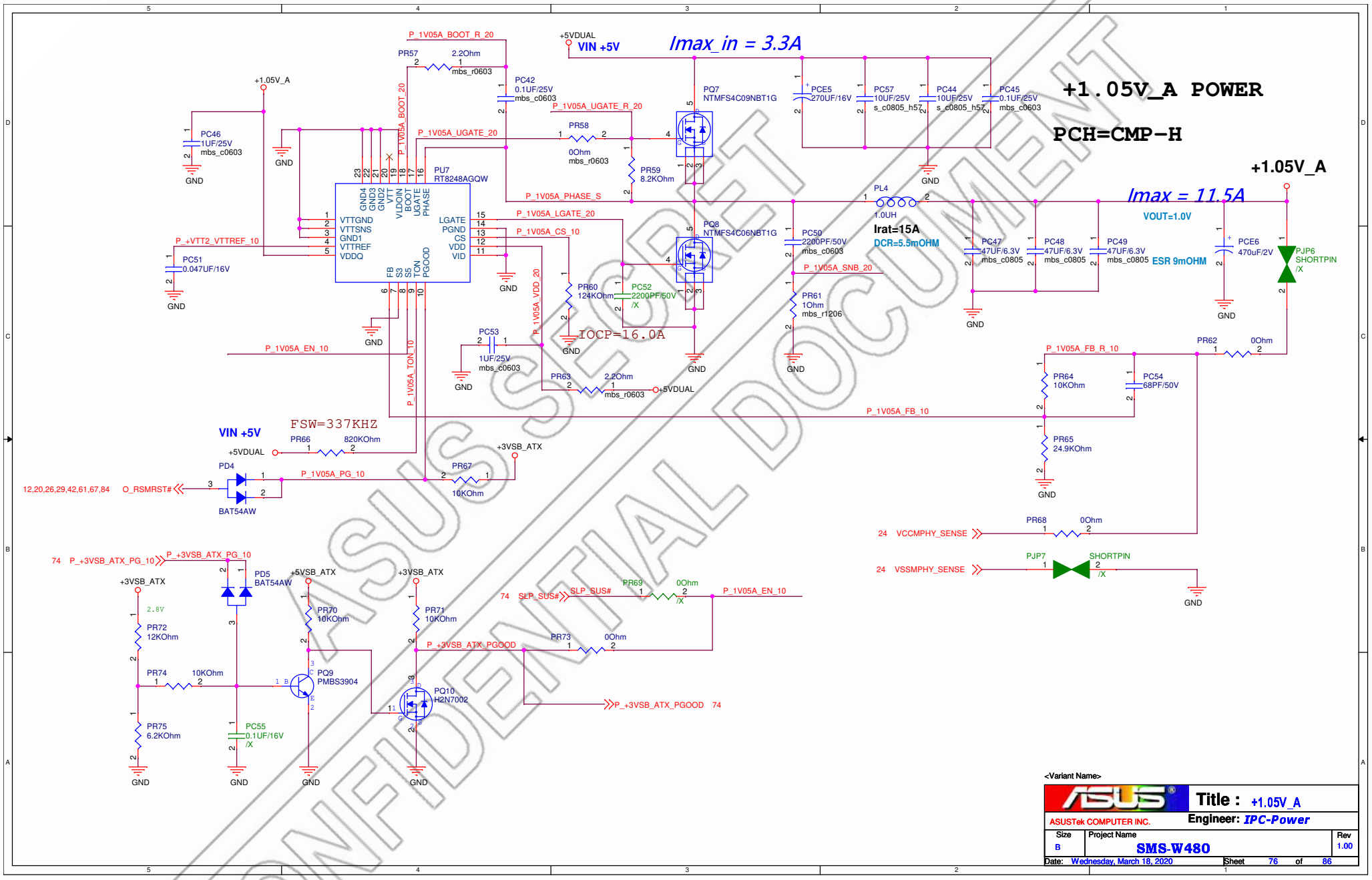


ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS	Title : +3VSB_ATX/+1.8V	
ASUSTek COMPUTER INC.	Engineer: IPC-Power	
Size: B	Project Name: SMS-W480	Rev: 1.00
Date: Wednesday, March 18, 2020	Sheet 74 of 86	


+VPPDDR POWER
Imax = 0.34A
+VPPDDR
PU5
UP0132PDDA
VIN1 VIN2 VIN3 EN VCNTL GND1 GND2 GND3
VOUT3 VOUT2 VOUT1 FB POK
VOUT = 0.8 (1 + R1/R2)
+3VSB_ATX
+5VSB_ATX
PR36 10KOhm
PR38 0Ohm /X
84 +VPPDDR_EN_10
42,61 P_+VPPDDR_EN
PC6 1UF/25V mbs_c0603
PC7 10UF/10V mbs_c0603
PC5 22UF/6.3V mbs_c0805
P_+VPPDDR_FB
P_+VPPDDR_PG_10
42,61
PR40 10KOhm
PR41 0Ohm /X
P_+VDDQ_EN_10
PC254 1000PF/50V /X
PR37 22KOhm
PR39 10KOhm
R1
R2
GND
+VDDQ
Place to socket outside
Top Side
PC1 22UF/6.3V mbs_c0603
PC2 22UF/6.3V mbs_c0603
PC3 22UF/6.3V mbs_c0603
PC4 22UF/6.3V mbs_c0603
Place to cavity of scoket
Bottom Side
PC8 22UF/6.3V mbs_c0603
PC9 22UF/6.3V mbs_c0603
PC10 22UF/6.3V mbs_c0603
PC11 22UF/6.3V mbs_c0603
Imax = 1.0A
+VDDQ_VTT
PJP4 SHORT_PIN /X
PC31 22UF/6.3V mbs_c0805
PC32 22UF/6.3V mbs_c0805
PC12 22UF/6.3V mbs_c0805
40MIL
PU6
RT8248AGQW
VTTGND VTTSNS GND1 VTTREF VDDQ
GND4 GND3 GND2 VTT VLDOIN BOOT UGATE PHASE
LGATE PGND CS VDD VID
FB SS S5 TON PGOOD
P_+VTT_SENSE_10
P_+VTT_VTTREF_10
PC36 0.047UF/16V
P_+VDDQ_BOOT_R_20
PR42 0Ohm mbs_r0603
PC43 0.1UF/25V mbs_c0603
P_+VDDQ_BOOT_20
P_+VDDQ_UGATE_20
PR43 0Ohm mbs_r0603
P_+VDDQ_UGATE_R_20
PR44 8.2KOhm
P_+VDDQ_PHASE_S
P_+VDDQ_LGATE_20
P_+VDDQ_CS_10
P_+VDDQ_VDD_20
P_+VDDQ_TON_10
PR45 150KOhm
IOCP=15.6A
PC38 2.2UF/16V mbs_c0603
PR51 2.2Ohm mbs_r0603
+5VDUAL
PR47 0Ohm /X
20,26,27,42,61,83,84 S_SLPS3#
PR48 10KOhm
PR50 10KOhm
84 P_+VTT_EN_10
42,61 P_+VDDQ_EN_10
P_+VTT_EN_10
P_+VDDQ_EN_10
FSW=337KHZ
VIN +5V
PR54 820KOhm
77,79 P_+VDDQ_PG_10
PR55 10KOhm
PC40 1000PF/50V
PC41 1000PF/50V
+5VDUAL
VIN +5V
Imax_in = 3.5A
PQ3 NTMFS4C09NBT1G
PQ4 NTMFS4C06NBT1G
PC13 0.1UF/25V mbs_c0603
PC14 10UF/25V s_c0805_h57
PC15 10UF/25V s_c0805_h57
PCE3 100UF/16V
PL3 1UH
Irat=25A
DCR=2.3mOHM
PC34 2200PF/50V mbs_c0603
P_+VDDQ_SNB_20
PR46 1Ohm mbs_r1206
PC37 2200PF/50V /X
Imax = 12A
+VDDQ
PC33 47UF/6.3V mbs_c0805
PC35 47UF/6.3V mbs_c0805
PCE4 560UF/6.3V
ESR 7mOHM
PJP5 SHORTPIN /X
P_+VDDQ_FB_R_10
PR49 0Ohm
PR52 12KOHM
PC39 68PF/50V
P_+VDDQ_FB_10
PR53 20KOhm
12,20,29,42,61,84 S_SLPS4#
S_SLPS4#
PR56 10KOhm /X
P_+VDDQ_EN_10
PD2 1PS70SB45 /X
<Variant Name>
Title : +VDDQ&+VPPDDR
ASUSTek COMPUTER INC.
Engineer: IPC-Power
Size B
Project Name SMS-W480
Rev 1.00
Date: Wednesday, March 18, 2020
Sheet 75 of 86
CONFIDENTIAL DOCUMENT
ASUS SECRET



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

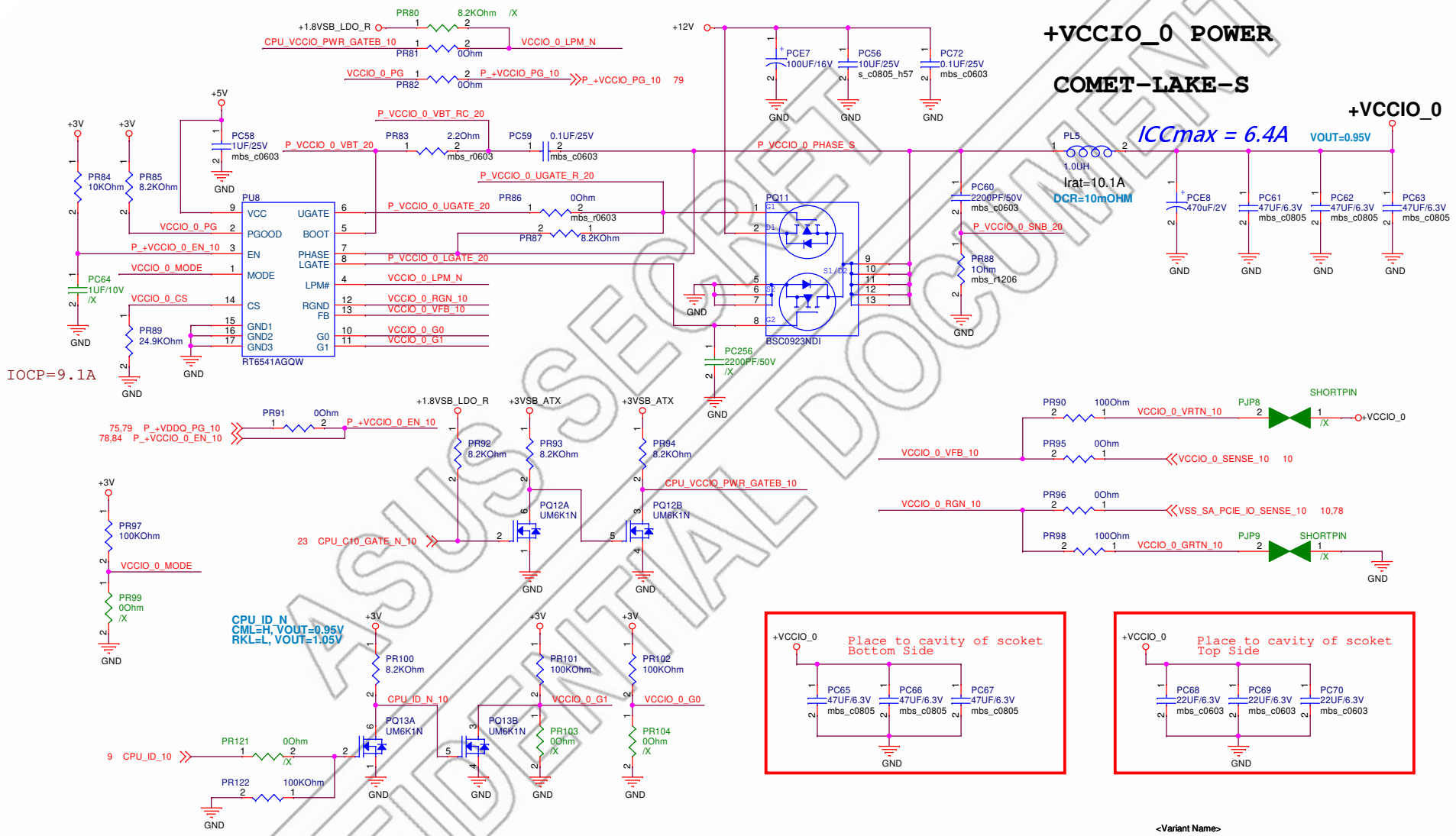
Title : +1.05V_A

ASUSTek COMPUTER INC.

Engineer: IPC-Power

Size	Project Name	Rev
B	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 76 of 86



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

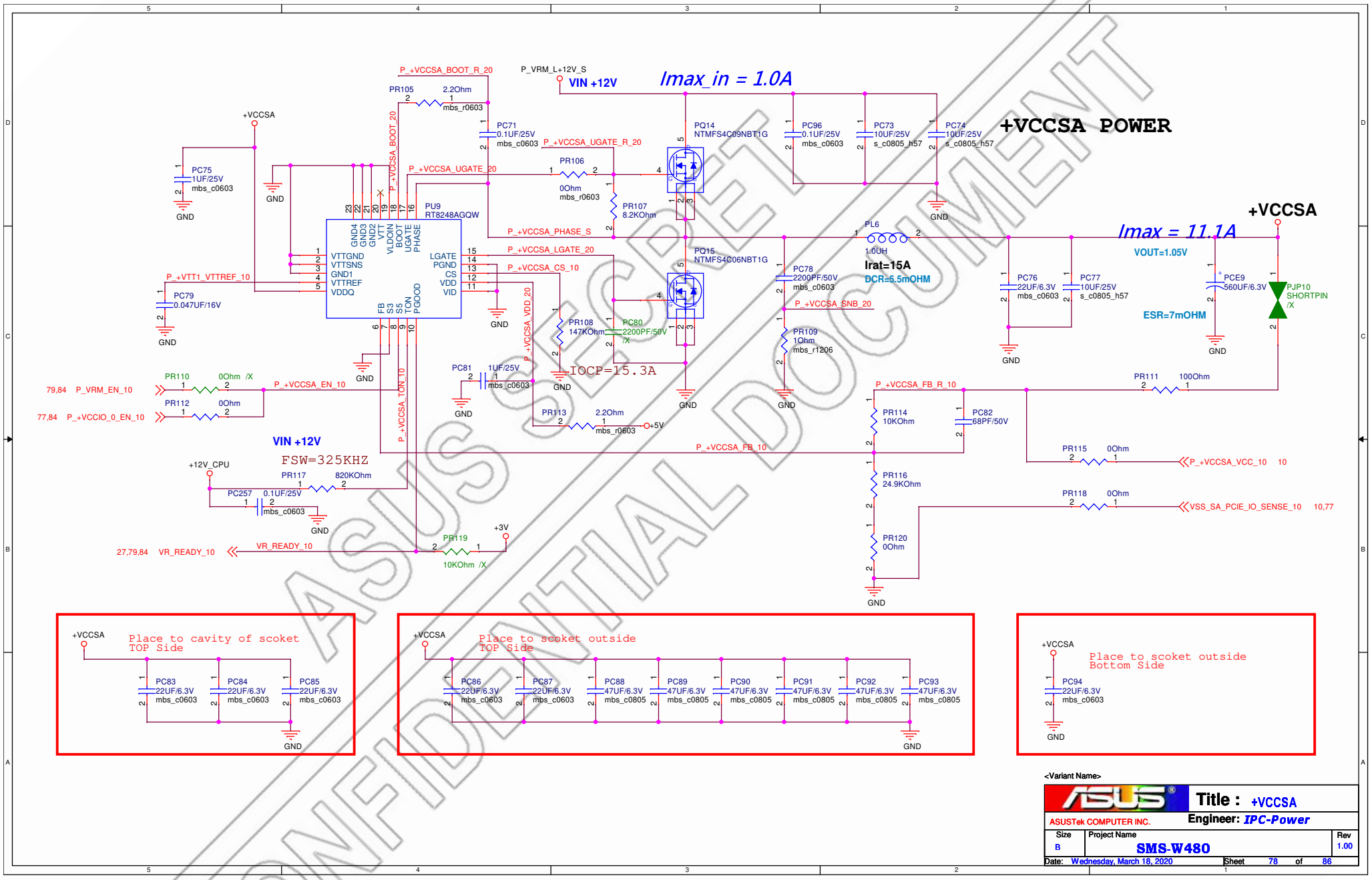
Title : +VCCIO_0

ASUSTek COMPUTER INC.

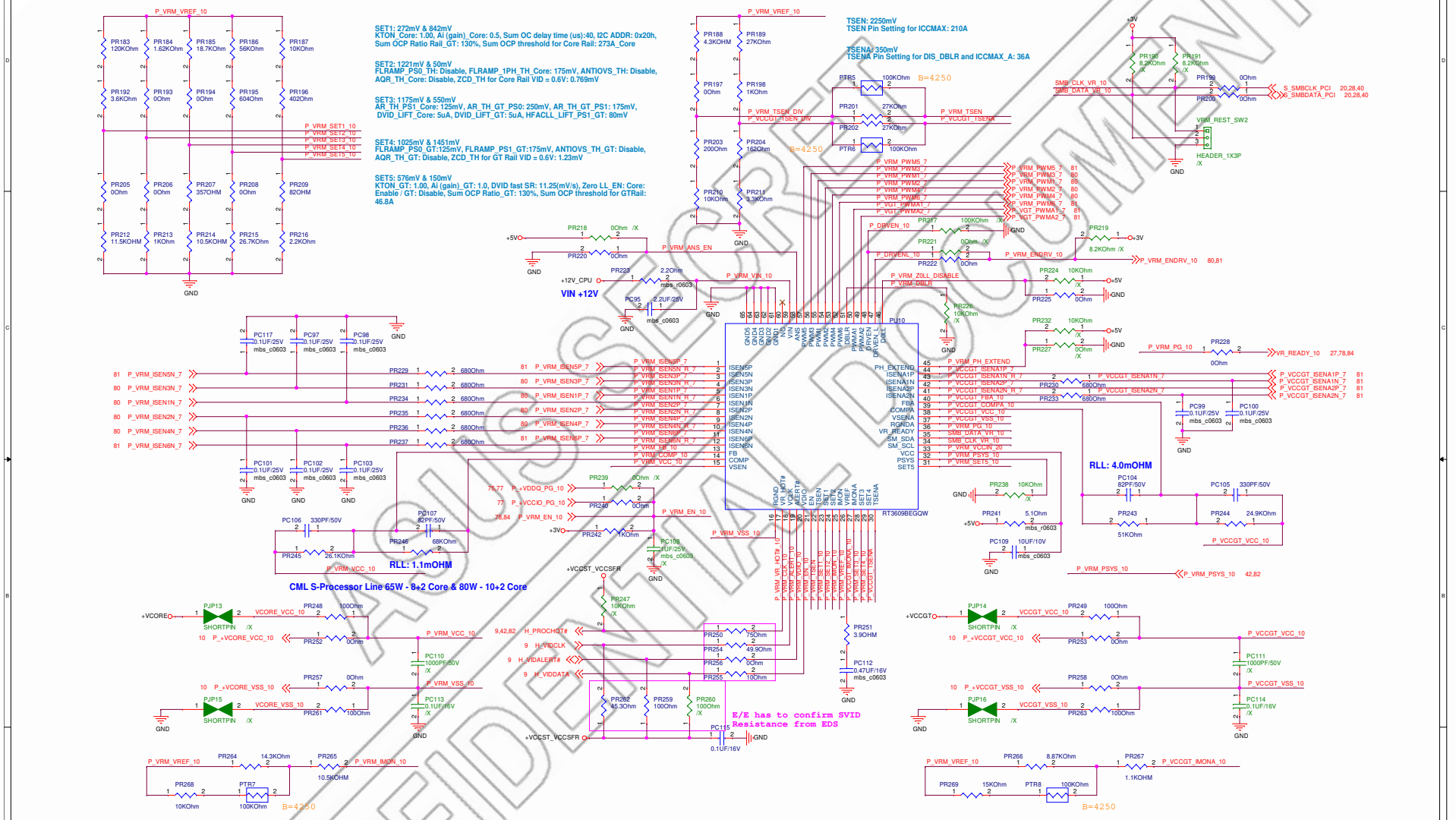
Engineer: IPC-Power

Size	Project Name	Rev
B	SMS-W480	1.00

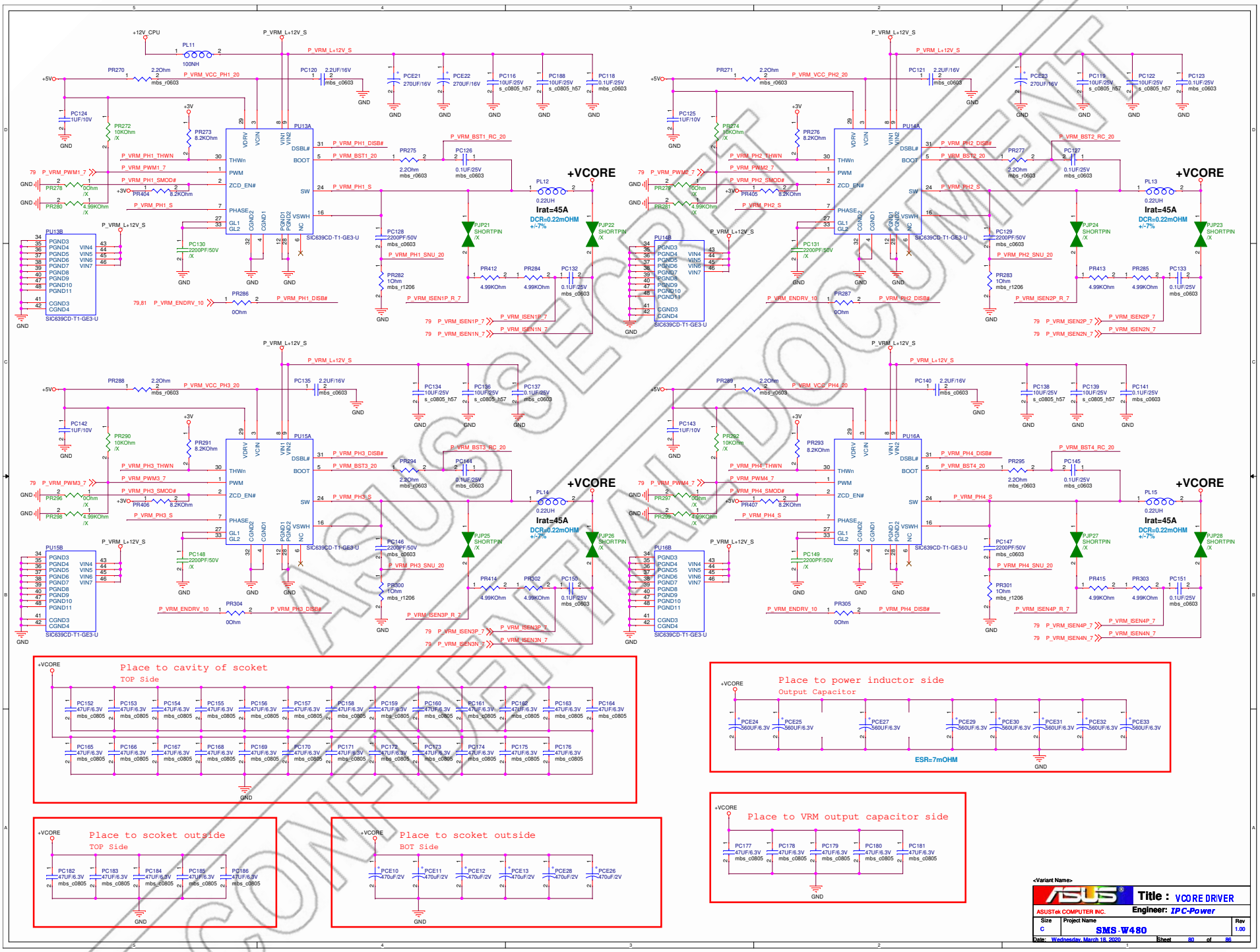
Date: Wednesday, March 18, 2020 Sheet 77 of 86



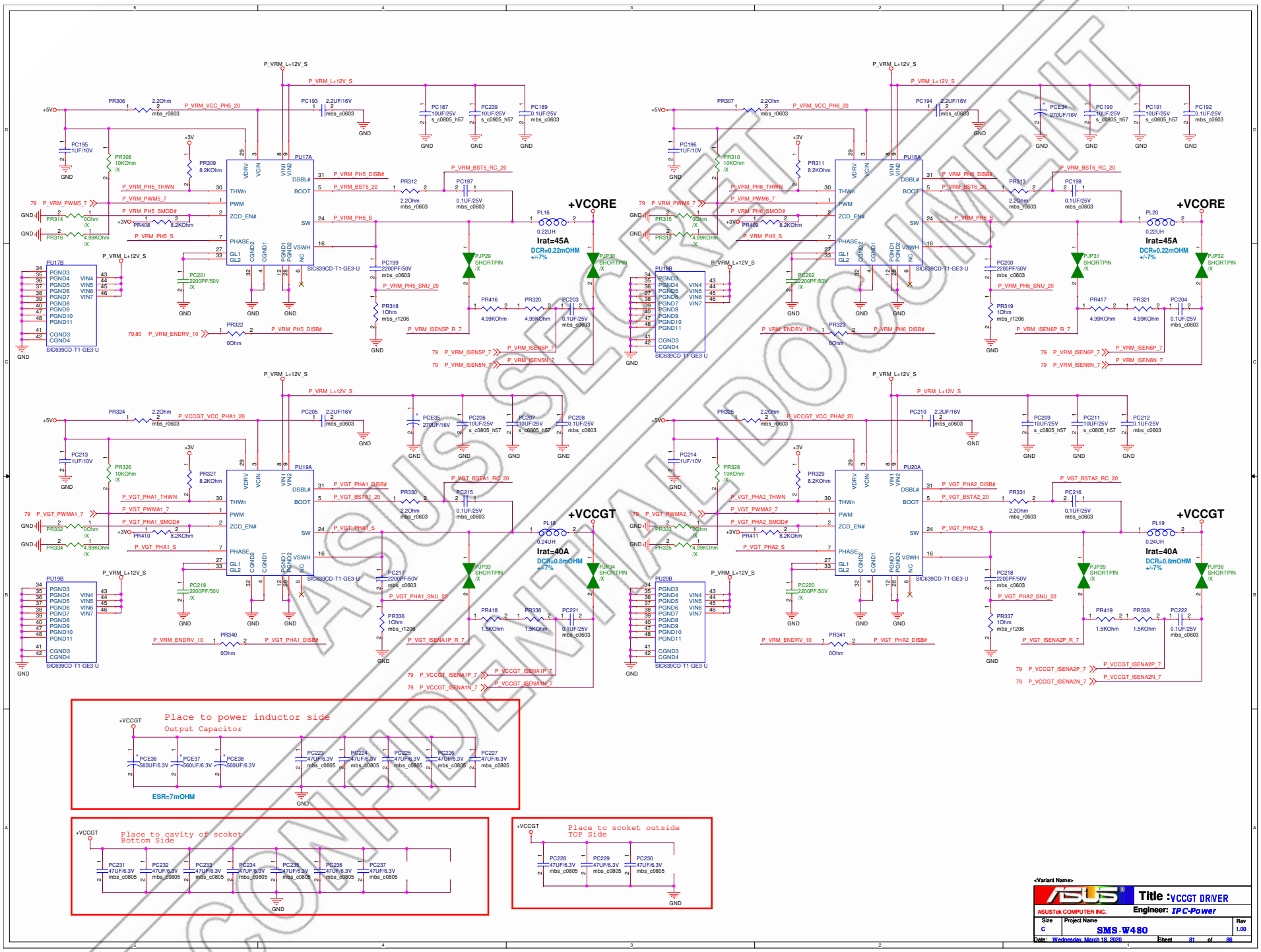
ASUS SECRET
CONFIDENTIAL DOCUMENT



CONFIDENTIAL DOCUMENT



ASUS SECRET
CONFIDENTIAL DOCUMENT



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

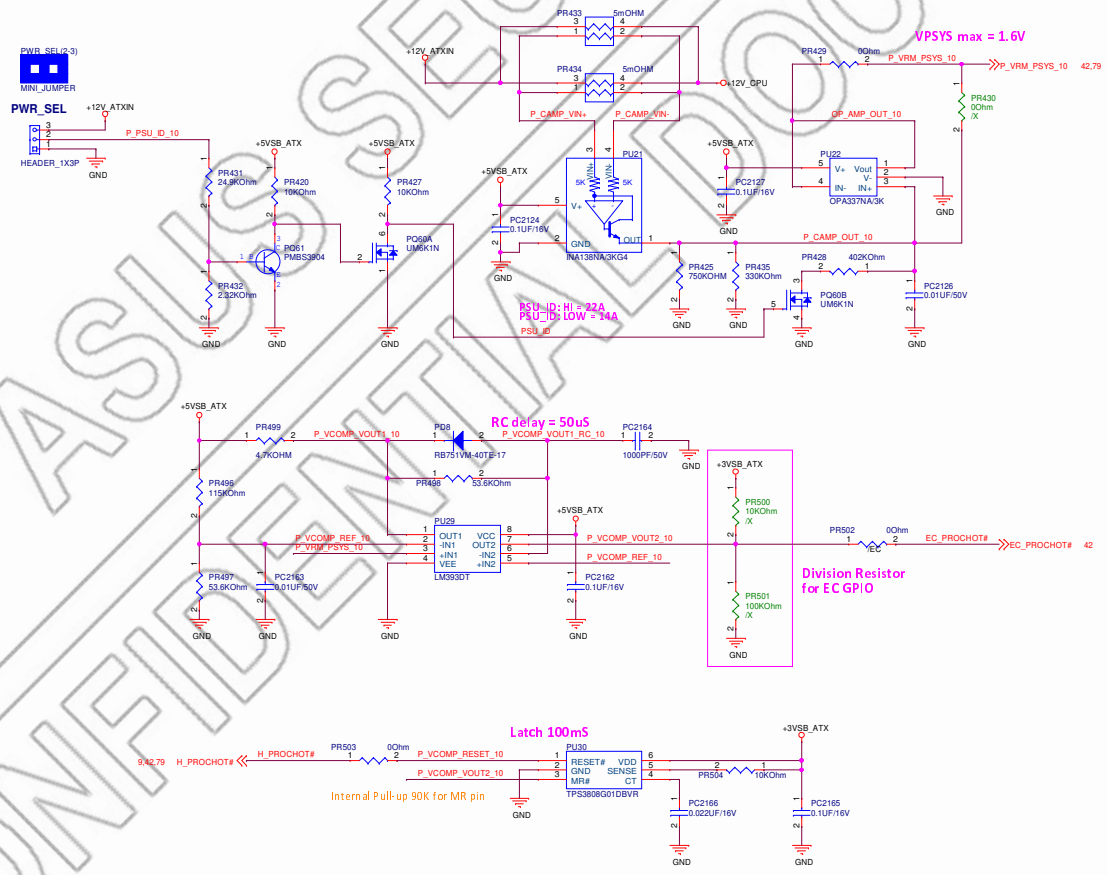
ASUSTeK COMPUTER INC.

Title : VCCGT DRIVER

Engineer: IPC-Power

Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 81 of 86



ASUS SECRET
CONFIDENTIAL DOCUMENT

<Variant Name>

ASUS

Title : External Power Sense

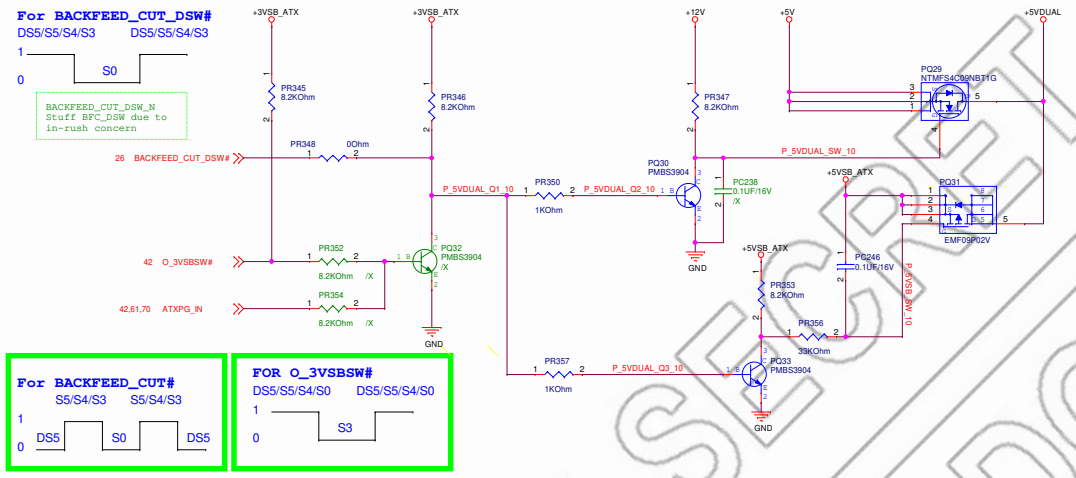
ASUSTeK COMPUTER INC.

Engineer: IPC-Power

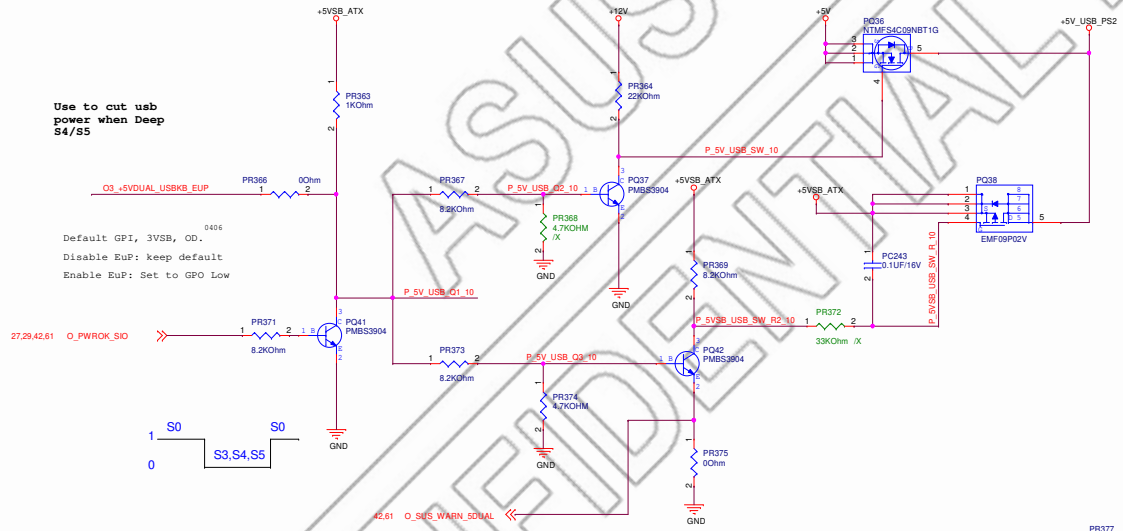
Size	Project Name	Rev
C	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 82 of 86

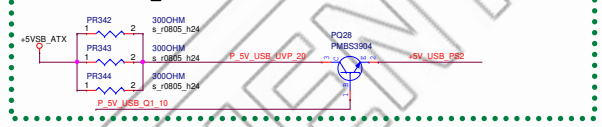
+5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT

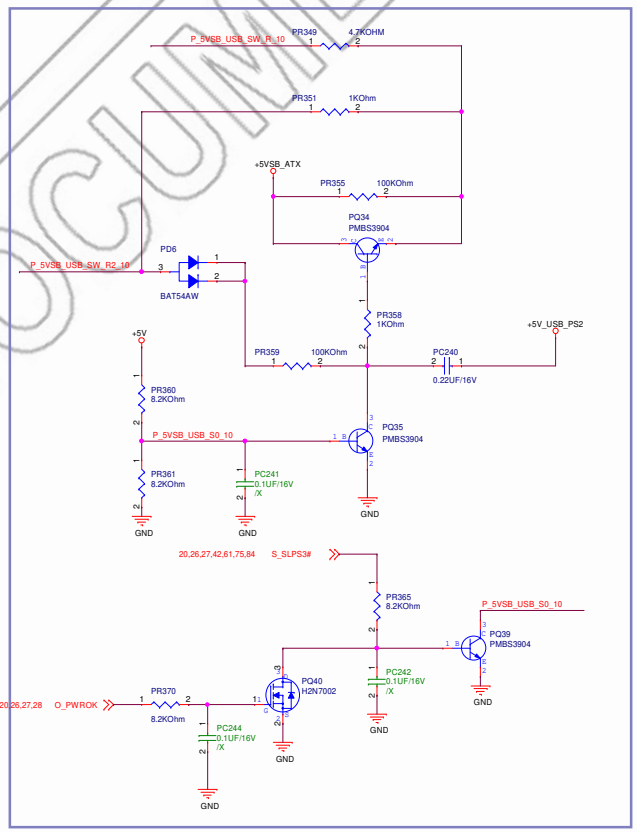


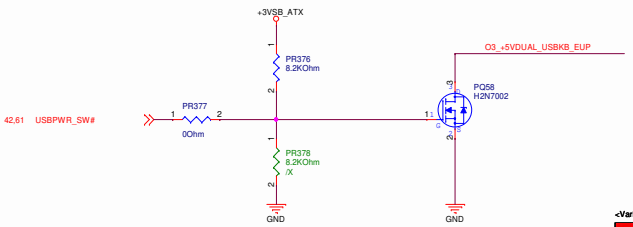
+5VSB_USBKB VOLTAGE & POWER CIRCUIT



+5VDUAL_USBKB UVP CIRCUIT







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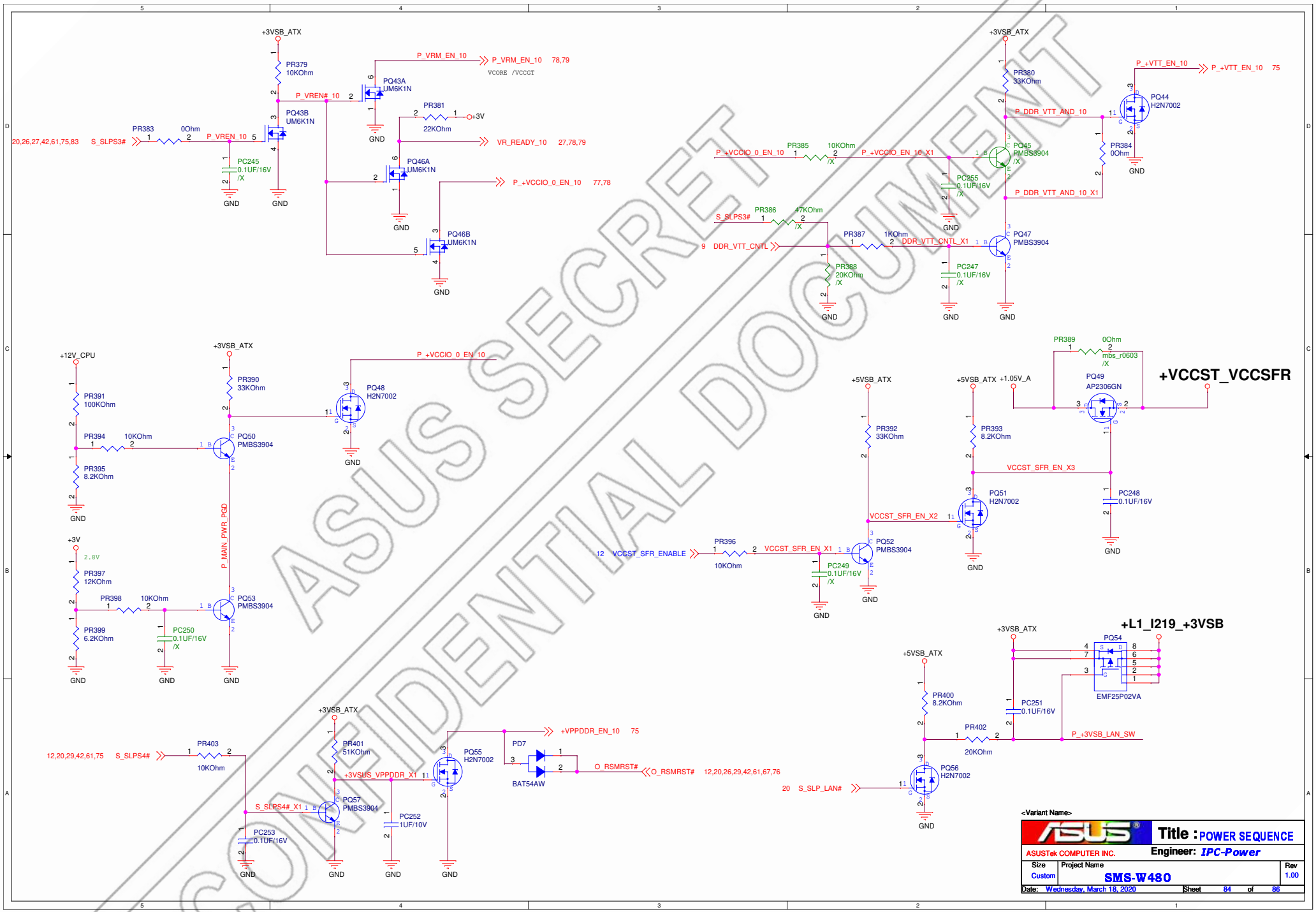
+3VSB_ATX
PR379
10KOhm
P_VRM_EN_10
P_VRM_EN_10 78,79
VCORE /VCCGT
PQ43A
UM6K1N
P_VREN#_10
PQ43B
UM6K1N
PR381
22KOhm
+3V
VR_READY_10 27,78,79
PQ46A
UM6K1N
P_+VCCIO_0_EN_10 77,78
PQ46B
UM6K1N
20,26,27,42,61,75,83 S_SLPS3#
PR383
0Ohm
P_VREN_10
PC245
0.1UF/16V
/X
GND
PR380
33KOhm
P_+VTT_EN_10
P_+VTT_EN_10 75
PQ44
H2N7002
P_DDR_VTT_AND_10
PR384
0Ohm
PQ45
PMBS3904
/X
P_+VCCIO_0_EN_10
PR385
10KOhm
/X
P_+VCCIO_EN_10_X1
PC255
0.1UF/16V
/X
P_DDR_VTT_AND_10_X1
S_SLPS3#
PR386
47KOhm
/X
9 DDR_VTT_CNTL
PR387
1KOhm
DDR_VTT_CNTL_X1
PQ47
PMBS3904
PR388
20KOhm
/X
PC247
0.1UF/16V
/X
+12V_CPU
PR391
100KOhm
PR394
10KOhm
PR395
8.2KOhm
PR390
33KOhm
PQ48
H2N7002
PQ50
PMBS3904
P_MAIN_PWR_PGD
+3V
2.8V
PR397
12KOhm
PR398
10KOhm
PR399
6.2KOhm
PC250
0.1UF/16V
/X
PQ53
PMBS3904
PR389
0Ohm
mbs_r0603
/X
PQ49
AP2306GN
+VCCST_VCCSFR
+5VSB_ATX
+1.05V_A
PR392
33KOhm
PR393
8.2KOhm
VCCST_SFR_EN_X3
PQ51
H2N7002
PC248
0.1UF/16V
VCCST_SFR_EN_X2
12 VCCST_SFR_ENABLE
PR396
10KOhm
VCCST_SFR_EN_X1
PQ52
PMBS3904
PC249
0.1UF/16V
/X
+L1_I219_+3VSB
PQ54
EMF25P02VA
PR400
8.2KOhm
PC251
0.1UF/16V
PR402
20KOhm
P_+3VSB_LAN_SW
PQ56
H2N7002
20 S_SLP_LAN#
12,20,29,42,61,75 S_SLPS4#
PR403
10KOhm
PR401
51KOhm
+3VSUS_VPPDDR_X1
PQ57
PMBS3904
S_SLPS4#_X1
PC253
0.1UF/16V
PC252
1UF/10V
PQ55
H2N7002
+VPPDDR_EN_10 75
PD7
BAT54AW
O_RSMRST#
O_RSMRST# 12,20,26,29,42,61,67,76
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<Variant Name>
Title : POWER SEQUENCE
ASUSTek COMPUTER INC.
Engineer: IPC-Power
Size Custom
Project Name SMS-W480
Rev 1.00
Date: Wednesday, March 18, 2020
Sheet 84 of 86

History 2020/01/21 R1.00 V1

01) First release

History 2020/01/22 V2

01) Change default to PD at SOFTOFF_LED_C, p.70
02) Reserve S_SLPS4# to BIOS Flash Back AI1315 at p.29
03) Mount 22UF at VBUS input and change 0.1uF to 10uF at VBUS output for TPS25810, p.55, 56
04) Modify VBUS MLCC cap. voltage to 16V at p.55, 56, 58
05) Change USB Power Switch at port 13/14 for BIOS flash back, p.29, 58

History 2020/02/07 V3

01) add 0 ohm at PCH to CPU CLK P/N, p.17 (Siemens request)
02) modfiy SPI Power from +3V_SPI to +3VSB_ATX at p.29, 30 (Siemens request)
03) reserve ESD at LAN MDI signal and remove LAN_GND at p.45, 47, 49 (Siemens request)
04) add ESD protect at USB_OC# pin, p. 54, 55, 57, 58 (Siemens request)
05) mount U3CR13/U3CR19 for USB_OC# at p.55, 56
06) change CPU ILM1/ILM2 module at p.11
07) change SIO monitor RTC power rail at p.28, 61 (Siemens request)
08) modify XDP_PRSENT# circuit at p.12
09) reserve JTAG_TCK PD resister, SR2001 at p.20
10) add XDP BOM option at p.12, 20
11) remove XDP_HOOK7 PH resister at p.12 (already PH OR145 at p.70)
12) modify USB Power Cap. UCE5401 for layout placement at p.55
13) modify PCH Power description at p.24
14) use SLP_S4# to drive FB_PWRSUS# and modify net name FB_SPI_UPD at p.29
15) change OR84 to 0ohm for SOFTOFF_LED drive at p.70
16) modify Thermal sensor TR4, TR6 net name at p.61, 66
17) swap net for layout placement at p.55, 56
18) follow Intel PDG modify memory support speed (remove 3200MHz) at p.1
19) add 560uF/6.3V (PCB41) for +VDDQ at p.16
20) modify DDR VREF circuit at p.16 (Non-compatibility Board with 2021 next gen. design)
21) modify SPI series resister to 56ohm at p.29, 30 (follow CML-S PDG, SPI 2 load topology)
22) update Power circuit at p.4, 74-75, 77-81 (please refer Siemens_Questions.docx)

History 2020/02/24 V4

01) add External Power Sense Circuit at p.79, 82
02) swap DP signal at ESD side for layotu request, p.37
03) modify DDR4 SMBus Power to +VDDSPD from +3V at p.28 (Siemens advise)
04) swap DDR4 DQ at CPU side for layout request at p.7, 8
05) Correct Block diagram for DDI mapping at p.1
06) reserve PC256 at +VCCIO MOS Gate, p.77
07) remove PCH reserve TP for layout request at p.17, 18, 21-23
08) modify SSD net name at con. side, P.59
09) mount expasion ROM for LAN chip i210 at p.46, 48
10) swap USB port 7,8 signal at ESD side for layout request, p.57
11) reserve Pull-down resister at M.2_REFCLK, p. 17
12) add 0.1uF at VCCHDA power pin for intel request at p.24
13) change SATA_DEVSLP to Port 6 at p.22
14) change poly fuse to power switch for USB power and control by PCH at p.19, 23, 54-58
15) correct +VCORE choke(PL12~PL16, PL20) footprint at p.80, 81
16) add 0.1uF and 220ohm between DVI TX P/N at p.36
17) modify CPU +VCORE Power circuit at p.79~81
18) correct PCH heatsink footprint for layout at p.26
19) PCE28 chagne to 7343 cap. from DIP package for layout placement at p.80
20) add EC IT5121 and modify SIO circuit at p.22, 42, 61
21) move Temp, Fan relation control to EC form SIO at p.42, 61, 66
22) change LED control to EC from SIO at p.18, 28, 42, 61, 70
23) reserve LED control from PCH at p.20, 23
24) change DIO#1~#4 to HDD_ALERT#1~#4 and control by EC at p.42, 61, 70
25) Swap LPC Clock at p. 22, 43
26) modify COM port design at p.61, 64, 68, 69
27) add diode at FB_PWRSUS# for S_SLPS4# control from EC at p.29

History 2020/03/09 V5

01) add 0.1uF cap. PC257 at +12V_CPU for noise concern, p.85
02) move Cap. value = 560uF to USB connector side at p.54, 55, 57, 58
03) modify EC_SCI#/SMI# circuit and add PME# at SIO p.22, 42, 61
04) unmount PECI path at SIO, p.61
05) unmount O_PCIEX1_RST# PH at p.42
06) reserve 0 ohm at SPI path for EC share ROM test, p.18, 42
07) add BOM option for EC, p.42
08) Thermal Sensor from UP1905 change to APL6002AASI-TRG/ANPEC SOT23-8 at p.66.
09) saperate SD_1P8_RCOMP/SD_3P3_RCOMP/GPPJ_RCOMP resistor at p.23 (follow Intel PDG)
10) modify +1.8V_A power to reserve at p.28, 74, 77
11) change U3C5/U3C6 for USB voltage rating at p.55, 56
12) change XTAL_24MHz resister to 200Kohm at p.17 (follow Intel PDG)
13) modify CPU +VCORE Power Solution, 6 phase to 8 phase at p. 79-82, 85
14) swap M.2 SATA/PCIe lane cofigure at p. 21, 59
15) change TPM to FW ver.: 7.2.1.0 by vendor advise at p.30
16) change MLCC 0.33uF/6.3V for BOM

History 2020/03/18 V6

01) change Type-C Con. for Siemens request at p.55, 56
02) add PROCHOT circuit at p.42, 82
03) modify CPU +VCORE Power Solution, 8 phase down to 6 phase at p. 79-82, 85
04) change/reserve SKTOCC# to PCH/EC at p.22, 23, 42

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ATX Connector (8 pin)
EATX_PWR2 for CPU

+12V_ATXIN	+12V_ATXIN 70,82
+12V_CPU	+12V_CPU 78,79,80,82,84
P_VRM_L+12V_S	P_VRM_L+12V_S 78,80,81

ATX Connector (24 pin)
EATX_PWR1 for System

+12V	+12V 28,31,32,33,34,35,36,37,38,40,63,64,65,67,69,70,71,77,83
-12V	-12V 40,67,69,70
+5VSB_ATX	+5VSB_ATX 29,41,42,61,62,63,66,70,71,74,75,76,82,83,84
+5V	+5V 36,37,38,40,59,61,62,63,64,65,67,69,70,71,77,78,79,80,81,83
-5V	-5V 70
+5VDUAL	+5VDUAL 75,76,83
+3V	+3V 9,15,17,18,20,21,22,23,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,50,51,52,53,59,61,64,65,68,70,71,77,78,79,80,81,84
+3VSB_ATX	+3VSB_ATX 9,10,12,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,40,42,43,46,47,48,49,50,51,52,53,58,61,64,67,70,74,75,76,77,82,83,84

+VCORE	+VCORE 10,63,79,80,81
+VCCGT	+VCCGT 10,79,81
+VCCSA	+VCCSA 10,78
+VCCIO_0	+VCCIO_0 9,10,12,77
+VCCIO_1_2	+VCCIO_1_2 10
+VCCST_VCCSFR	+VCCST_VCCSFR 9,10,27,61,79,84
+VCCSFR	+VCCSFR 9,10
+VCCSTG	+VCCSTG 9,10,12,20
+VDDQ	+VDDQ 10,13,14,15,16,20,70,75
+VDDQ_VTT	+VDDQ_VTT 15,16,75
+VPPDDR	+VPPDDR 10,15,16,75
+3V +VDDSPD	+VDDSPD 13,14,15,28
+VCCDDQ_EDGECAP2	+VCCDDQ_EDGECAP2 10
+VCCDDQ_EDGECAP1	+VCCDDQ_EDGECAP1 10
+1.05V_A	+1.05V_A 12,24,76,84
+1.05V_A_DSW	+1.05V_A_DSW 24
+1.05V_A_VCCA_XTAL	+1.05V_A_VCCA_XTAL 24
+1.05V_A_VCCAMPHYPLL	+1.05V_A_VCCAMPHYPLL 24
+3VSB_ATX +DVDDIO_AUDIO	+DVDDIO_AUDIO 20,24
+3VSB_ADV	+3VSB_ADV 20,24
+3V_EPW	+3V_EPW 24
+VCCPFUSE_3P3	+VCCPFUSE_3P3 24
+3V_BAT +VCCPRTC_3P3	+VCCPRTC_3P3 24
+3V_BAT	+3V_BAT 18,24,28,61,62
+1.8V_A	+1.8V_A 24,28,74
+1.8VSB_LDO	+1.8VSB_LDO 24
+1.8VSB_LDO_R	+1.8VSB_LDO_R 23,24,77
+1.24V_A_LDO	+1.24V_A_LDO 24
+1.24V_A	+1.24V_A 24

RTC PWR. P28

+3V_BAT +BAT	+BAT 28,42,61

System SPI ROM PWR.P29,30

+3VSB_ATX +3V_SPI	+3V_SPI 29
+3V_SPI +VCC1833	+VCC1833 29
+1.2V_SPI	+1.2V_SPI 29

TPM2.0_NPCT750AAAYX PWR.P30

+3V_SPI VDD_P8	VDD_P8 30
VDD_P14	VDD_P14 30

DVI-D PWR. P36

+3V +3V_DVI	+3V_DVI 36
+5V +5V_DVI	+5V_DVI 36

DP Port PWR. P37

+3V +3V_C_DP	+3V_C_DP 37
+3V_DP1	+3V_DP1 37

DP Port PWR. P38

+3V +3V_D_DP	+3V_D_DP 38
+3V_DP2	+3V_DP2 37,38

PCI_Asmedia1083 PWR. P39,40.

+3V +3VA_EPCI	+3VA_EPCI 39
+1.2V_EPCI	+1.2V_EPCI 39,40
+1.2V_EPCI +1.2VA_EPCI	+1.2VA_EPCI 39

LAN PHY_I219V PWR. P44,45.

Enable :P_+3VSB_LAN_SW

+3VSB_ATX +L1_I219_+3VSB	+L1_I219_+3VSB 44,45,84
+L1_I219_0.9V	+L1_I219_0.9V 44
L1_CTR	L1_CTR 45

LAN PHY_I210AT PWR. P46,47.

+3VSB_ATX +3V_AUX	+3V_AUX 46
+1.5V_LAN2	+1.5V_LAN2 46,47
+0.9V_LAN2	+0.9V_LAN2 46
L2_CTR	L2_CTR 47

LAN PHY_I210AT PWR. P48,49.

+3VSB_ATX +3V_AUX3	+3V_AUX3 48
+1.5V_LAN3	+1.5V_LAN3 48,49
+0.9V_LAN3	+0.9V_LAN3 48
L3_CTR	L3_CTR 49

Audio ALC887-VD2-GR PWR. P41

+3V +3.3V_AUDIO	+3.3V_AUDIO 41
Stuff for ALC886	
+5VSB_ATX +5V_AUDIO	+5V_AUDIO 41
Stuff for ALC892/887	
+5VSB_ATX +LDOVDD	+LDOVDD 41

IT5121E-I-128/CX. P42

+3VSB_ATX +3VA_EC	+3VA_EC 42
+3VACC	+3VACC 42
+3V +3V_EC	+3V_EC 42

+5V_USB PWR

+5V_USB_PS2 +5V_USB_PS2	+5V_USB_PS2 54,55,56,57,58,71,83

USB31 Gen2 Type-A in LAN1. P45,50, 54

+5V_USB_PS2 +5V_USB3_P12	+5V_USB3_P12 45,54
+3V +VDD12	+VDD12 50

USB31 Gen2 Type-A in LAN2,3. P47, 49, 51, 55

+5V_USB_PS2 +5V_USB3_P35	+5V_USB3_P35 47,49,55
+3V +VDD35	+VDD35 51

USB31 Gen2 Type-C. P52, 53, 55, 56

+5V_USB_PS2 +USB_C_VBUS	+USB_C_VBUS 55
+USB_C1_VBUS	+USB_C1_VBUS 56
+3V +VDD4	+VDD4 52
+VDD6	+VDD6 53

USB31 Gen1 Internal Header. P57

+5V_USB_PS2 +5V_USB3_P78	+5V_USB3_P78 57

USB20 Header Port PWR. P58

+5V_USB_PS2 +5V_USB2_P910	+5V_USB2_P910 58
+5V_USB2_P1112	+5V_USB2_P1112 58

USB20 Vertivcal Type-A Port PWR. P57

+5V_USB_PS2 +5V_USB2_P1314	+5V_USB2_P1314 58

COM1 Port PWR. P64

+5V RI1_F_VCC	RI1_F_VCC 64

CPU&SYS-NCT3949S/Power Fan PWR. P65

+12V +FP_VOUT	+FP_VOUT 65
+12V +FP1_VOUT	+FP1_VOUT 65
+12V +FP2_VOUT	+FP2_VOUT 65
+12V +FP3_VOUT	+FP3_VOUT 65

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ASUSTek COMPUTER INC.

Title : Power Net Name

Engineer: IPC-EE3

Size	Project Name	Rev
Custom	SMS-W480	1.00

Date: Wednesday, March 18, 2020 Sheet 86 of 86