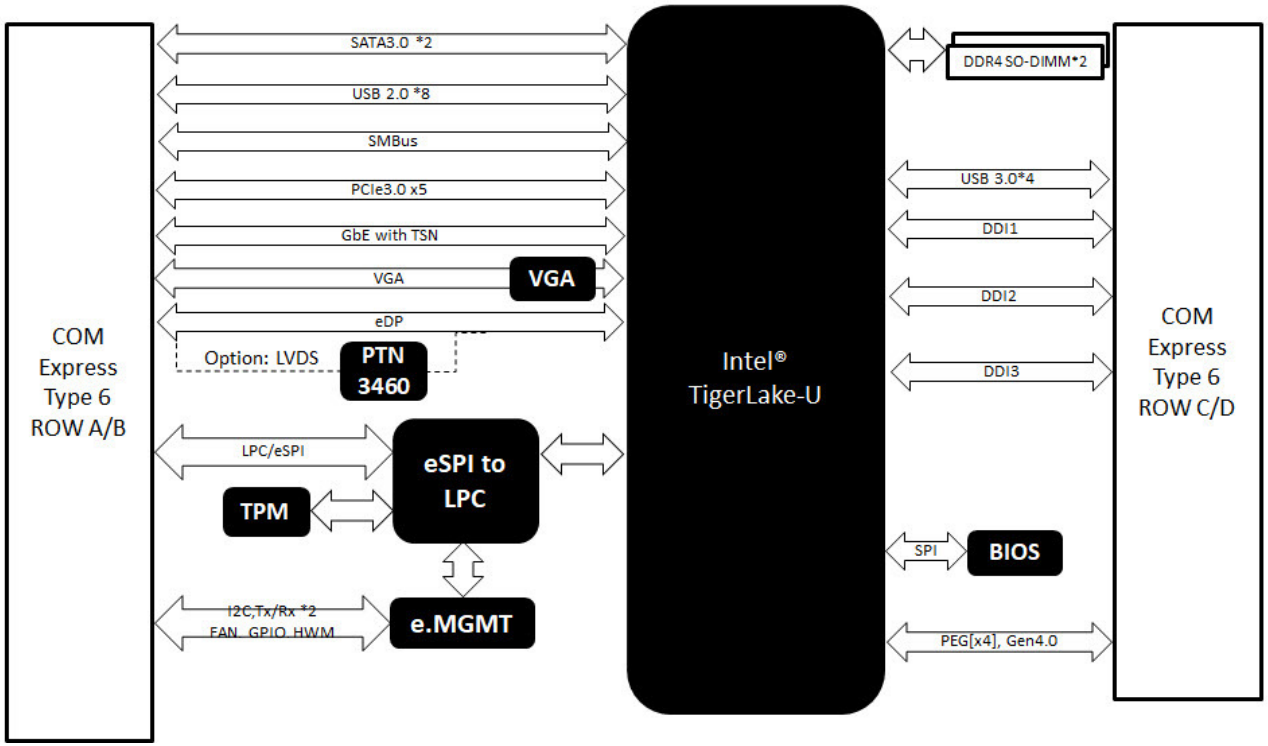
Project Name : COM-TGUC6
Project Number: E191211
Version: A0.2_0_0

COM-TGUC6 Block Diagram



<Variant Name>

AAEON Technology INC.

Title: Cover Sheet		
Size	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 1 of 36	

SoC GPIO Pins :

Name	Power Well	Default	GPIO Function	Location
GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	+V3P3S	PD	DDI3_HPD	DH52
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK	+V3P3S	PD	DDI4_HPD	DK45
GPP_E4/DEVSLP0	+V3P3A	PU	USB2_OC2#	DG8
GPP_E5/DEVSLP1	+V3P3A	PU	USB2_OC1#	DN6
GPP_E3/CPU_GP0	+V3P3A	PU	SMI#	DU5
GPP_E7/CPU_GP1	+V3P3A	PU	SCI#	DF8
GPP_T2	+V3P3A	PD	BOARD_ID1	DT35
GPP_T3	+V3P3A	PD	BOARD_ID0	DN33
GPP_U4	+V3P3A	PD	BOARD_ID3	DG19
GPP_U5	+V3P3A	PD	BOARD_ID2	DG17
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#	+V3P3A	PU	ESPI_ALT#	CY50
GPP_H19/TIME_SYNC0	+V3P3S	PU	EC_KBRST#	DJ27

EC GPIO Pins :

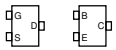
Name	Power Well	Default	GPIO Function	Location	Note
KSI1/AFD#	+V3P3A	Input	I_RSMRST	J13	
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7	+V3P3A	Output	O_RSMRST	A1	When J13 active HIGH, then PU A1 after 10ms
KSO5/PD5	+V3P3A	Output	ESPI_EN#	J8	PU to Enable COM eSPI out
L80HLAT/BAO/WUI24/GPE0	+V3P3A	Input	GPI0	N2	
EGAD/WUI25/GPE1	+V3P3A	Input	GPI1	A13	
EGCS#/WUI26/GPE2	+V3P3A	Input	GPI2	A12	
EGCLK/WUI27/GPE3	+V3P3A	Input	GPI3	B12	
HSCE#/GPH3/ID3	+V3P3A	Output	GPO0	A9	
HSCK/GPH4/ID4	+V3P3A	Output	GPO1	B8	
HMISO/GPH5/ID5	+V3P3A	Output	GPO2	A8	
HMOSI/GPH6/ID6	+V3P3A	Output	GPO3	B7	

SMBus/I2C Addresses :

Device	address
I219	0XC8
PTN3460BS/F6	0C0h

PCB Footprints

MOSFET BJT



PCB STACK :

Board: FR4
Impedence: 50ohm +/-10%
Thickness: 2.0mm +-10%

- Layer 1 : Component (Top)
- Layer 2 : GND (GND1)
- Layer 3 : Signal (IN1)
- Layer 4 : GND (GND2)
- Layer 5 : Signal (IN2)
- Layer 6 : POWER (VCC)
- Layer 7 : POWER (VCC)
- Layer 8 : Signal (IN3)
- Layer 9 : GND (GND3)
- Layer 10 : Signal (IN4)
- Layer 11 : GND (GND4)
- Layer 12 : Signal (IN5)
- Layer 13 : GND (GND5)
- Layer 14 : Solder (Bottom)

<Variant Name>

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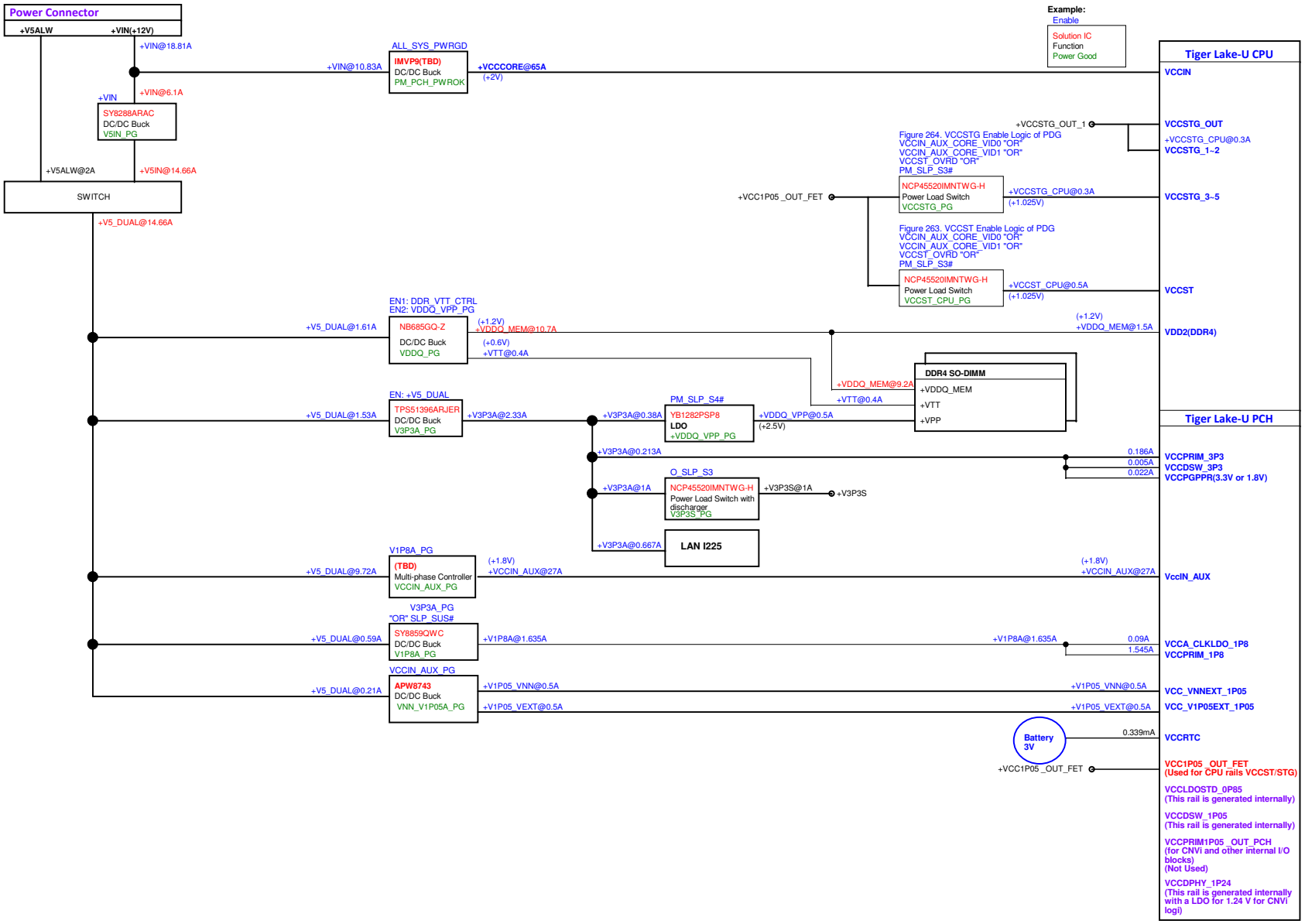
AAEON Technology INC.

Title: System Setting

Size | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 2 of 36

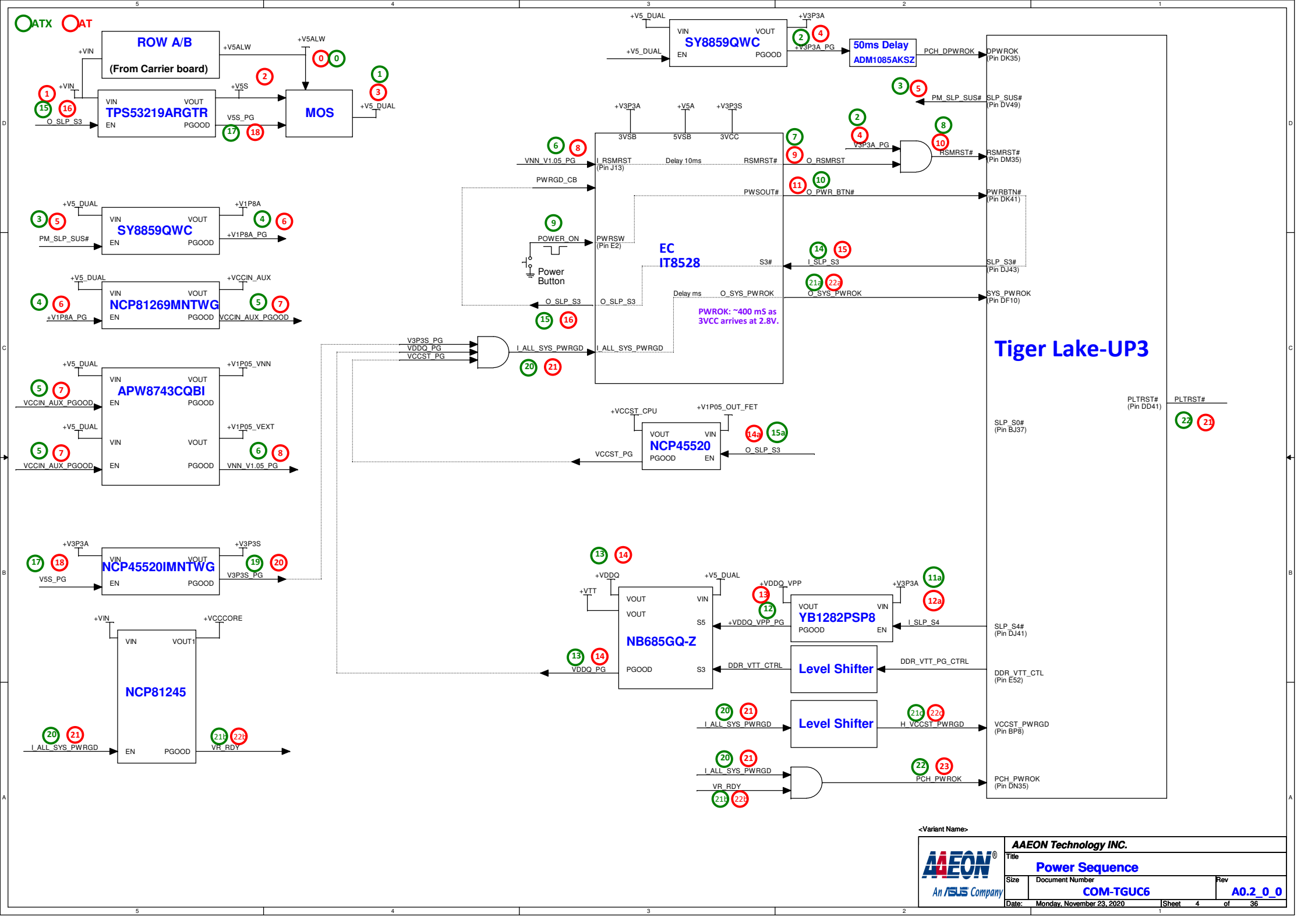
Power Delivery



<Variant Name>

AAEON Technology INC.

Title	Power Delivery	
Size	Document Number	Rev
	COM-TGUC6	A0.2_0_0
Date:	Monday, November 23, 2020	Sheet 3 of 36


ATX
AT
ROW A/B
(From Carrier board)
+VIN
+V5ALW
+V5S
+V5_DUAL
O_SLP_S3
VIN
VOUT
TPS53219ARGTR
EN
PGOOD
V5S_PG
MOS
SY8859QWC
+V1P8A
+V1P8A_PG
PM_SLP_SUS#
NCP81269MNTWG
+VCCIN_AUX
VCCIN_AUX_PGOOD
APW8743CQBI
+V1P05_VNN
+V1P05_VEXT
VNN_V1.05_PG
NCP45520IMNTWG
+V3P3A
+V3P3S
V3P3S_PG
NCP81245
+VCCCORE
VOUT1
I_ALL_SYS_PWRGD
VR_RDY
+V5_DUAL
SY8859QWC
+V3P3A_PG
50ms Delay
ADM1085AKSZ
PCH_DPWROK
DPWROK
(Pin DK35)
PM_SLP_SUS#
SLP_SUS#
(Pin DV49)
+V3P3A
+V5A
+V3P3S
3VSB
5VSB
3VCC
VNN_V1.05_PG
I_RSMRST
(Pin J13)
Delay 10ms
RSMRST#
O_RSMRST
RSMRST#
(Pin DM35)
PWRGD_CB
PWSOUT#
O_PWR_BTN#
PWRBTN#
(Pin DK41)
POWER_ON
PWRSW
(Pin E2)
Power
Button
EC
IT8528
S3#
I_SLP_S3
SLP_S3#
(Pin DJ43)
O_SLP_S3
Delay ms
O_SYS_PWROK
SYS_PWROK
(Pin DF10)
PWROK: ~400 mS as
3VCC arrives at 2.8V.
V3P3S_PG
VDDQ_PG
VCCST_PG
I_ALL_SYS_PWRGD
Tiger Lake-UP3
+VCCST_CPU
+V1P05_OUT_FET
NCP45520
PGOOD
EN
VCCST_PG
O_SLP_S3
PLTRST#
(Pin DD41)
PLTRST#
SLP_S0#
(Pin BJ37)
+VDDQ
+VTT
+V5_DUAL
NB685GQ-Z
S5
S3
+VDDQ_VPP_PG
YB1282PSP8
+VDDQ_VPP
+V3P3A
I_SLP_S4
SLP_S4#
(Pin DJ41)
DDR_VTT_CTRL
Level Shifter
DDR_VTT_PG_CTRL
DDR_VTT_CTL
(Pin E52)
VDDQ_PG
I_ALL_SYS_PWRGD
Level Shifter
H_VCCST_PWRGD
VCCST_PWRGD
(Pin BP8)
I_ALL_SYS_PWRGD
VR_RDY
PCH_PWROK
PCH_PWROK
(Pin DN35)
<Variant Name>
AAEON Technology INC.
Title
Power Sequence
Size
Document Number
COM-TGUC6
Rev
A0.2_0_0
Date: Monday, November 23, 2020
Sheet 4 of 36

GPP_D10	TBT LSX #2 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

The internal pull-down 20k is disabled after RSMRST# de-asserts.

GPP_D12	TBT LSX #3 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

The internal pull-down 20k is disabled after RSMRST# de-asserts.

TBT_LSX0_RXD	TBT LSX #0 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

This strap has a 20 kohm ± 30% internal pull-down.

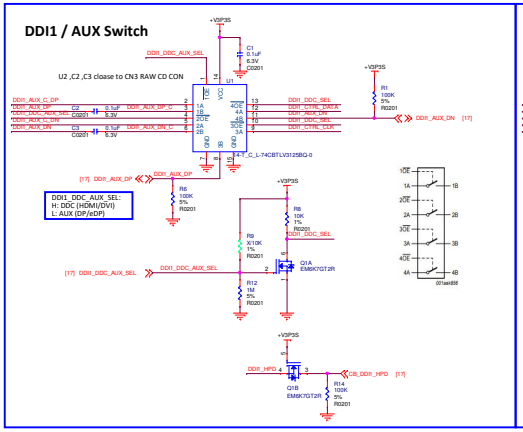
TBT_LSX1_RXD	TBT LSX #1 PINS VCCIO CONFIGURATION
0	1.8V
1 *	3.3V

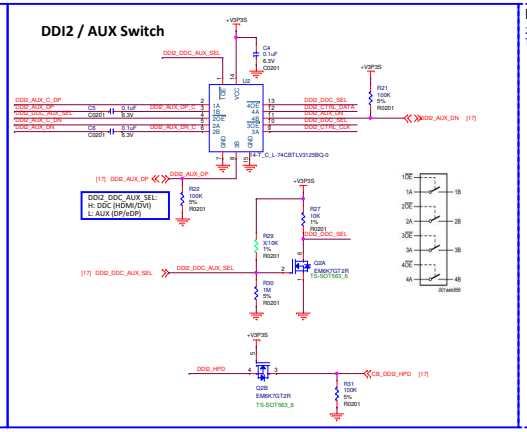
This strap has a 20 kohm ± 30% internal pull-down.

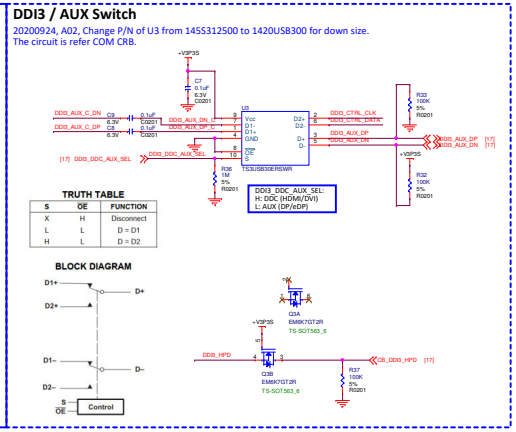
Table 41. TCP Port Signal Mapping For DisplayPort*

Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3

Note: Apply to TCP ports only.

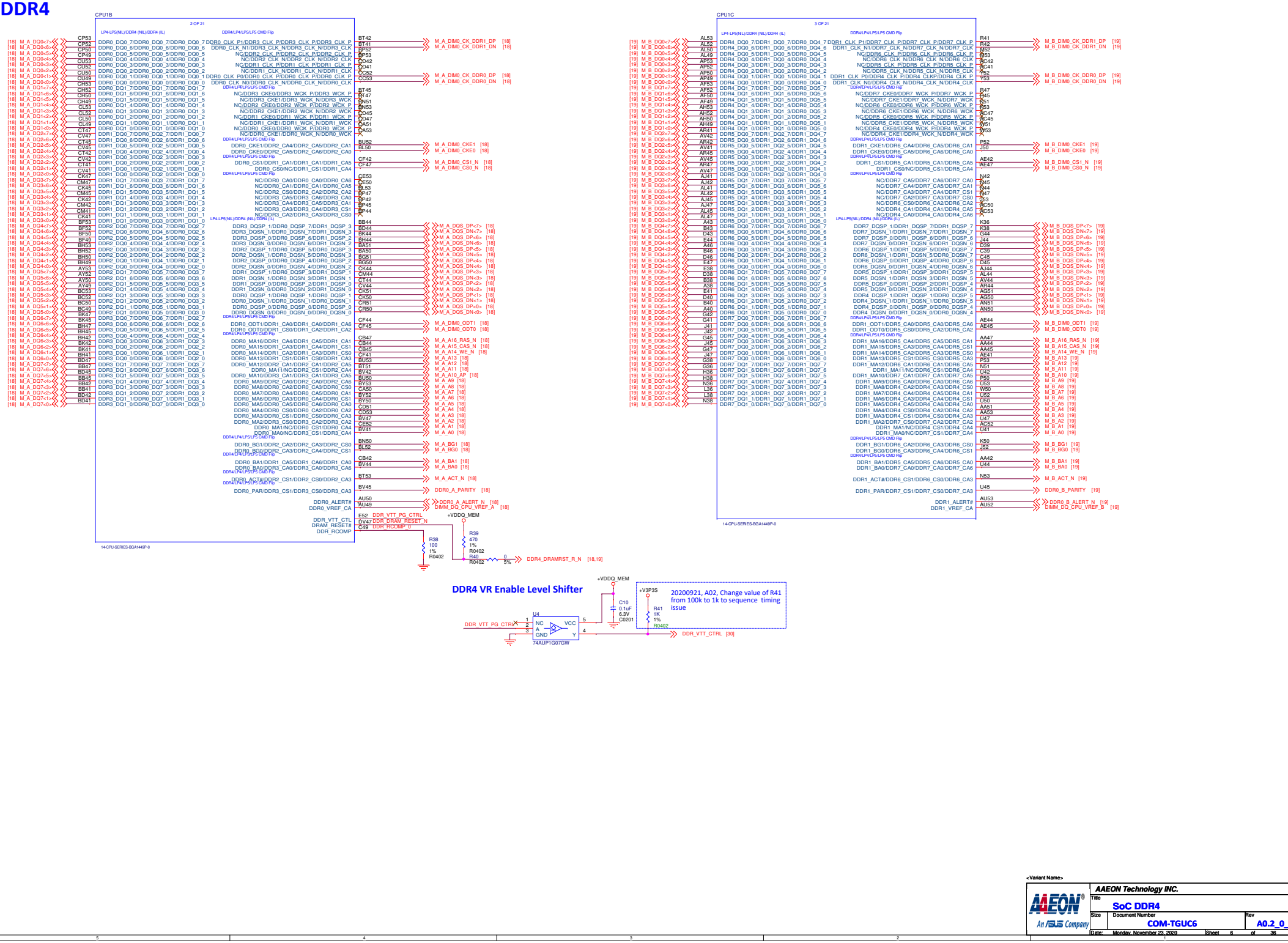






AAEON Technology INC.
SoC DDI
COM-TGUC6
A0.2_0_0
Monday, November 23, 2020

SoC DDR4



DDR4 VR Enable Level Shifter

20200921, A02, Change value of R41 from 100k to 1k to sequence timing issue

SoC SPI/LPC/SMBus

SPI0_MOSI	Reserved
	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on- board device driving it to opposite direction during strap sampling.

External pull-up is required. Recommend 4.7 kohm pull up.

+V3P3A — R45 R0402 4.7K 1% — SPI0_SI_R

SPI0_IO2	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

External pull-up is required.

+V3P3A — R57 R0402 100K 1% — SPI0_DQ2_WP#

SPI0_IO3	Reserved
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

External pull-up is required.

+V3P3A — R66 R0402 100K 1% — SPI0_DQ3_HOLD#

GPP_E6	JTAG ODT Disable
0	JTAG ODT is disabled
1 *	JTAG ODT is enabled

This strap does not have an internal pull-up or pull-down. External pull-up is recommended

+V3P3A — R72 R0402 100K 1% — GPP_E6

+V1P8A — R75 R0402 X/100K 1% — R77 R0402 X/4.7K 1%

DBG_PMODE	Reserved
	This strap should sample high. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-up.

R82 R0402 X/1K 1% — DBG_PMODE

GPP_H0	BFX STRAP 1- BIT 2

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R91 R0402 X/4.7K 1% — R92 R0402 X/20K 1% — GPP_H0

GPP_H1	BFX STRAP 2- BIT 3

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R96 R0402 X/4.7K 1% — R97 R0402 X/20K 1% — GPP_H1

GPP_H2	BFX STRAP 3- BIT 4

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — R103 R0402 X/4.7K 1% — R104 R0402 X/20K 1% — GPP_H2

20200930, A02, Add R568~R570 for 2 SPI device.

[23,26] SPI0_CLK — R568 R0201 5.1ohm, 1% — SPI0_CLK_R — R43 100K 5% R0201

[23] SPI0_DQ3_HOLD# — SPI0_DQ3_HOLD#
[23] SPI0_DQ2_WP# — R569 5.1ohm, 1% R0201 — SPI0_DQ2_WP#
[23,26] SPI0_SO — R570 5.1ohm, 1% R0201 — SPI0_SI_R
[23,26] SPI0_SI

TPM

20200917, A02, Add SPI0_TPM_CS2# to support SPI TPM.

[23] SPI0_CS0# — SPI0_CS0#
[26] SPI0_TPM_CS2# — SPI0_TPM_CS2#

CPU1E — 5 OF 21

SPI0_CLK DJ37
SPI0_IO3 DG35
SPI0_IO2 DJ39
SPI0_MISO DJ33
SPI0_MOSI DJ35
SPI0_CS1# DF35
SPI0_CS0# DG37
SPI0_CS2# DF39

GPP_E11/THC0_SPI1_CLK DJ6
GPP_E2/THC0_SPI1_IO3 DN5
GPP_E1/THC0_SPI1_IO2 DR5
GPP_E12/THC0_SPI1_IO1 DM5
GPP_E13/THC0_SPI1_IO0 DK5
GPP_E10/THC0_SPI1_CS# DV1
GPP_E8/SATA_LED# DW3
GPP_E17/THC0_SPI1_INT# DT6
GPP_E6/THC0_SPI1_RST# DT8

GPP_F11/THC1_SPI2_CLK DN15
GPP_F15/GSXSRESET#/THC1_SPI2_IO3 DK13
GPP_F14/GSXDIN/THC1_SPI2_IO2 DM13
GPP_F13/GSXSLOAD/THC1_SPI2_IO1 DN13
GPP_F12/GSXDOUT/THC1_SPI2_IO0 DJ15
GPP_F16/GSXCLK/THC1_SPI2_CS# DK15
GPP_F18/THC1_SPI2_INT# DN11
GPP_F17/THC1_SPI2_RST# DV14

CL_CLK DH3
CL_DATA DH5
CL_RST# DP2

14-CPU-SERIES-BGA1449P-0

+V3P3S — R59 R0201 10K 1% — [17] SATALED# — SATALED#

GPP_E6

GPP_F15 — TP4 TP20

GPP_C0/SMBCLK DK21 — SMB_CLK — SMB_CLK [17]
GPP_C1/SMBDATA DM19 — SMB_DATA — SMB_DATA [17]
GPP_C2/SMBALERT# DN19 — SMBALERT# — SMBALERT# [17]

Carrier board/DDR4/ Debug Card/LVDS

GPP_C3/SML0CLK DK19 — LAN_SM_CLK — LAN_SM_CLK [20]
GPP_C4/SML0DATA DM17 — LAN_SM_DATA — LAN_SM_DATA [20]
GPP_C5/SML0ALERT# DN17 — SML0ALERT#

I225

GPP_C6/SML1CLK DK17 — EC_SMCLK0 — EC_SMCLK0 [21]
GPP_C7/SML1DATA DJ17 — EC_SMDAT0 — EC_SMDAT0 [21]
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# CY50 — SML1ALERT#

EC

GPP_A5/ESPI_CLK DN53 — ESPI_CLK — R60 R0402 49.9 1% — BDG_ESPI_CLK — BDG_ESPI_CLK [17,27]
GPP_A3/ESPI_IO3/SUSACK# DJ53 — ESPI_IO_3 — R61 R0402 15 5% — BDG_ESPI_IO_3 — BDG_ESPI_IO_3 [17,27]
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK DH50 — ESPI_IO_2 — R62 R0402 15 5% — BDG_ESPI_IO_2 — BDG_ESPI_IO_2 [17,27]
GPP_A1/ESPI_IO1 DP50 — ESPI_IO_1 — R63 R0402 15 5% — BDG_ESPI_IO_1 — BDG_ESPI_IO_1 [17,27]
GPP_A0/ESPI_IO0 DP52 — ESPI_IO_0 — R64 R0402 15 5% — BDG_ESPI_IO_0 — BDG_ESPI_IO_0 [17,27]
GPP_A4/ESPI_CS# DK52 — ESPI_CS# — R65 R0402 0 5% — BDG_ESPI_CS# — BDG_ESPI_CS# [17,27]
GPP_A6/ESPI_RESET# DL50 — ESPI_RESET# — R67 75K 1% R0402

R70 R0402 0 5% — BDG_ESPI_RST# — BDG_ESPI_RST# [17,27]
R71 75K 1% R0402

Note: SUSPWRDNACK is not available as hard signals when eSPI, SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered

20201106, A02, Change R46/R47 from 1k(0201) to 499ohm (0402) for I225.

+V3P3A

SMB_CLK — R42 R0201 1K 5%
SMB_DATA — R44 R0201 1K 5%
LAN_SM_CLK — R46 R0402 499 1%
LAN_SM_DATA — R47 R0402 499 1%
EC_SMCLK0 — R49 R0201 1K 5%
EC_SMDAT0 — R50 R0201 1K 5%

XDP

[21] PECI_EC — PECI_EC — R73 R0402 43 5%

+V1P05_VCCSTG_LGC — R78 1K 1% R0402

[21,31] H_PROCHOT# — H_PROCHOT# — R79 R0402 499 1%

+VCCST_CPU — R521 1K 1% R0402

+VCCST_CPU — R80 1K 1% R0402

H_THRMTRIP# — R81 R0402 60.4 1%

R83 R0402 49.9 1% — PROC_POPIRCOMP
R85 R0402 49.9 1% — PCH_OPIRCOMP

CPU1U — 21 OF 21

CATERR# M7
PECI BK9
PROCHOT# E2
THRMTRIP# M5

PROC_POPIRCOMP CT39
PCH_OPIRCOMP CB9
TP_1 CW12
TP_2 CM39

DBG_PMODE — DBG_PMODE DF4

GPP_B4/CPU_GP3 DB42
GPP_B3/CPU_GP2 DB44
GPP_E7/CPU_GP1 DP8
GPP_E3/CPU_GP0 DU5

EAR_N/EAR_N_TEST_NCTF

GPP_H2 DF31
GPP_H1 DV33
GPP_H0 DW32

GPP_H19/TIME_SYNC0

PROC_TRST# K4 — XDP_CPU_JTAG_TRST#
PROC_TMS B9 — XDP_CPU_JTAG_TMS
PROC_TDO D12 — XDP_CPU_JTAG_TDO
PROC_TDI A12 — XDP_CPU_JTAG_TDI
PROC_TCK B6 — XDP_CPU_JTAG_TCLK

PCH_JTAGX D8 — XDP_CPU_JTAG_TCLK
PCH_TMS A9 — XDP_CPU_JTAG_TMS
PCH_TDO E12 — XDP_CPU_JTAG_TDO
PCH_TDI B12 — XDP_CPU_JTAG_TDI
PCH_TCK A7 — XDP_PCH_JTAG_TCLK
PCH_TRST# H4 — XDP_CPU_JTAG_TRST#

PROC_PREQ# C11
PROC_PRDY# D11

G1 — CPU_EAR
DT15 — GPP_F7
DR15 — GPP_F9
DT14 — GPP_F10

14-CPU-SERIES-BGA1449P-0

+V3P3S — R87 R0201 10K 1% — EC_KBRST# — [17] EC_KBRST# — EC_KBRST# DJ27

[17,21] SMI# — SMI#
[17,21] SCI# — SCI# DU5

DBG_PMODE

SMB level-shift

+V3P3S — R105 2.2K 5% R0201 — Q5B — SMB_DATA — EM6K7GT2R TS-SOT563_6 — SMB_DATA_S [18,19,24]

+V3P3S — R108 2.2K 5% R0201 — Q5A — SMB_CLK — EM6K7GT2R TS-SOT563_6 — SMB_CLK_S [18,19,24]

THRMTRIP# level-shift

+VCCST_CPU — C363 0.1uF 6.3V C0201 — +V3P3A — R572 10K 1% R0201

H_THRMTRIP# — U8 SN74AUP1G07DRLR SOT-553.5P;SMD — PCH_THRMTRIP# — PCH_THRMTRIP# [17]

20201021, A02, Change level shifter to Drive IC to fit input voltage level of 1.05V

SMBALERT#	TLS confidentiality
0	Disable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 *	Enable IntelR CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to pupport IntelR AMT with TLS

* Default, Internal Pull-Down 20K

+V3P3A — SMBALERT# R48 R0402 4.7K 1%

SML0ALERT#	This is bit 0 (LSB) of a total of 4-bit boot strap configuration encodings
0 *	
1	

* Default, Internal Pull-Down 20K

+V3P3A — SML0ALERT# R58 R0402 150K 1%

SML1ALERT#	CPUNSSC CLOCK FREQ
0 *	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

* Default, Internal Pull-Down 20k
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

+V3P3A — SML1ALERT# R102 R0402 150K 1%

20200922, A02, Remove BDG_ESPI_ALT_3P3# level-shift
The eSPI_IO1 presents the ALERT# state while the eSPI bus is idle by datasheet.

20200902, A02, remove R107, Q6, R106 for AT ON/OFF test issue (hang 5d), it's follow COM CRB.
TGP-LP SUPPORTS IN-BAND ESPI ALERT by COM CRB.

GPP_F7	Reserved
	This strap should sample LOW. There should NOT be any on- board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — GPP_F7 — R68 R0402 X/4.7K 1% — R69 R0402 X/20K 1%

GPP_F10	Reserved
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A — GPP_F10 — R74 R0402 X/4.7K 1% — R76 R0402 X/20K 1%

CPU_EAR	Stall CPU reset sequence until de-asserted:
1 *	(Default) Normal Operation; No stall.
0	Stall

+VCCSTG_CPU — CPU_EAR — R84 R0402 1K 1% — R86 R0402 X/1K 1%

XDP PU/PD

+V1P05_VCCSTG_LGC

XDP_CPU_JTAG_TDO — R88 100 1% R0402
XDP_CPU_JTAG_TDI — R89 X/51 1% R0402
XDP_CPU_JTAG_TMS — R90 X/51 1% R0402
XDP_CPU_JTAG_TCLK — R93 51 1% R0402
XDP_CPU_JTAG_TRST# — R94 X/51 1% R0402
XDP_PCH_JTAG_TCLK — R95 X/51 1% R0402

<Variant Name>

AAEON Technology INC.

Title	SoC SPI/LPC/SMBus	
Size	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 7 of 36	

SoC HDA/SD

HDA_SDO	Flash Descriptor Security Override
0 *	Disabled (Default)
1	Enable (Disable ME)(debug ONLY)

* Default, Internal Pull-Down 20K

+V3P3A — R115 X/1K HDA_SDO_R — R0402 1%

SPKR	Top Swap Override
0 *	Disabled
1	Enable

* Default, Internal Pull-Down 20K
CRB: PULL UP 100K RESISTOR PRESENT ON THIS NET

+V3P3A — R117 150K SPKR — R0402 1%

GSPI1_MOSI	No Reboot
0 *	REBOOT ENABLED
1	NO REBOOT

* Default, Internal Pull-Down 20K

+V3P3A — R118 X/4.7K GSPI0_MOSI — R0402 1%

All HDA R close to SOC

CPU1G — 7 OF 21

[17] HDA_BCLK — R111 33R0201 HDA_BCLK_R — DR38 GPP_R0/HDA_BCLK/I2S0_SCLK
[17] HDA_SYNC — R112 33R0201 HDA_SYNC_R — DU37 GPP_R1/HDA_SYNC/I2S0_SFRM
[17] HDA_SDO — R109 33R0201 HDA_SDO_R — DT37 GPP_R2/HDA_SDO/I2S0_TXD
[17] HDA_SDI0 — R110 0 R0201 HDA_SDI0_R — DV37 GPP_R3/HDA_SDI0/I2S0_RXD
[17] HDA_RST# — R113 33R0201 HDA_RST#_R — DV41 GPP_R4/HDA_RST#
DL53 GPP_A7/I2S2_SCLK/DMIC_CLK_A0
DG51 GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
DG50 GPP_A10/I2S2_RXD/DMIC_DATA1
DL49 GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
DL52 GPP_A11/PMC_I2C_SDA/I2S3_SCLK
DH49 GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
R116 200 SNDW_RCOMP — DF33 SNDW_RCOMP
1% R0402

GPP_F8/I2S_MCLK2_INOUT — DW15
GPP_D19/I2S_MCLK1 — DW24
GPP_A23/I2S1_SCLK — DG41
GPP_R7/I2S1_SFRM — DT38
GPP_R6/I2S1_TXD — DV38
GPP_R5/HDA_SDI1/I2S1_RXD — DW38 HDA_SDI1_R R114 0 R0201 HDA_SDI1 [17]
GPP_S6/SNDW3_CLK/DMIC_CLK_A0 — DN31
GPP_S7/SNDW3_DATA/DMIC_DATA0 — DM31
GPP_S4/SNDW2_CLK/DMIC_CLK_A1 — DK33
GPP_S5/SNDW2_DATA/DMIC_DATA1 — DK31
GPP_S2/SNDW1_CLK/DMIC_CLK_B0 — DW35
GPP_S3/SNDW1_DATA/DMIC_CLK_B1 — DV35
GPP_S0/SNDW0_CLK — DT32
GPP_S1/SNDW0_DATA — DR35

14-CPU-SERIES-BGA1449P-0

A01, 20200506, change R109 from 0R to 33R by PDG request.

CPU1F — 6 OF 21

GSPI0_MOSI — DC53 GPP_B16/GSPI0_CLK
DA51 GPP_B18/GSPI0_MOSI
DC49 GPP_B17/GSPI0_MISO
[17] SPKR — SPKR — DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
DC52 GPP_B15/GSPI0_CS0#
CY49 GPP_B20/GSPI1_CLK
CY53 GPP_B22/GSPI1_MOSI
CY52 GPP_B21/GSPI1_MISO
DA50 GPP_B19/GSPI1_CS0#
TP31 TP20 GPP_C9 — DV21 GPP_C9/UART0_TXD
TP30 TP20 GPP_C8 — DT21 GPP_C8/UART0_RXD
DR21 GPP_C11/UART0_CTS#
DW21 GPP_C10/UART0_RTS#
20200717, A02, Add TP30~TP33 for BIOS request.
DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD
DT19 GPP_C12/UART1_RXD/ISH_UART1_RXD
DR19 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
[26] TPM_PIRQ# — DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
TP33 TP20 GPP_C21 — DJ21 GPP_C21/UART2_TXD
TP32 TP20 GPP_C20 — DG23 GPP_C20/UART2_RXD
DJ19 GPP_C23/UART2_CTS#
DF21 GPP_C22/UART2_RTS#
DV18 GPP_C17/I2C0_SCL
DW18 GPP_C16/I2C0_SDA
DJ23 GPP_C19/I2C1_SCL
DT19 GPP_C18/I2C1_SDA
20201105, A02, the nets of CPU1.DJ29 & CPU1.DJ31 (I2C fuction for 80 port) for the PCB spacing of EEPROM of Intel I225.
DJ29 GPP_H5/I2C2_SCL
DJ31 GPP_H4/I2C2_SDA
COM — [17] I2C3_SCL — I2C3_SCL — DF29 GPP_H7/I2C3_SCL
[17] I2C3_SDA — I2C3_SDA — DG29 GPP_H6/I2C3_SDA
DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

14-CPU-SERIES-BGA1449P-0

GPP_D14/ISH_UART0_TXD — DR27
GPP_D13/ISH_UART0_RXD — DW27
GPP_D16/ISH_UART0_CTS# — DV25
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5 — DT25
GPP_B6/ISH_I2C0_SCL — DB45
GPP_B5/ISH_I2C0_SDA — DB44
GPP_B8/ISH_I2C1_SCL — CY39
GPP_B7/ISH_I2C1_SDA — DB47
GPP_B10/I2C5_SCL/ISH_I2C2_SCL — DD47
GPP_B9/I2C5_SDA/ISH_I2C2_SDA — DD44
GPP_E16/ISH_GP7 — DJ8
GPP_E15/ISH_GP6 — DR7
GPP_D18/ISH_GP5 — DR24
GPP_D17/ISH_GP4 — DU25
GPP_D3/ISH_GP3/BK3/SBK3 — DV31
GPP_D2/ISH_GP2/BK2/SBK2 — DU31
GPP_D1/ISH_GP1/BK1/SBK1 — DT27
GPP_D0/ISH_GP0/BK0/SBK0 — DV27
GPP_RCOMP — DR51 GPPC_RCOMP R123 1% 200 R0402
GPP_T3 — DN33 BOARD_ID0
GPP_T2 — DT35 BOARD_ID1
GPP_U5 — DG17 BOARD_ID2
GPP_U4 — DG19 BOARD_ID3

BOARD ID

BOARD_ID0 — R418 X/2.2K R0402 1% — R419 20K R0201 1% — +V3P3A
BOARD_ID1 — R420 X/2.2K R0402 1% — R421 20K R0201 1% — +V3P3A
BOARD_ID2 — R422 X/2.2K R0402 1% — R423 20K R0201 1% — +V3P3A
BOARD_ID3 — R424 X/2.2K R0402 1% — R425 20K R0201 1% — +V3P3A

+V3P3S — R122 1K R0201 5% I2C3_SCL — R121 1K R0201 5% I2C3_SDA

<Variant Name>

AAEON Technology INC.

Title: SoC HDA/I2C

Size	Document Number	Rev
	COM-TGUC6	A0.2_0_0

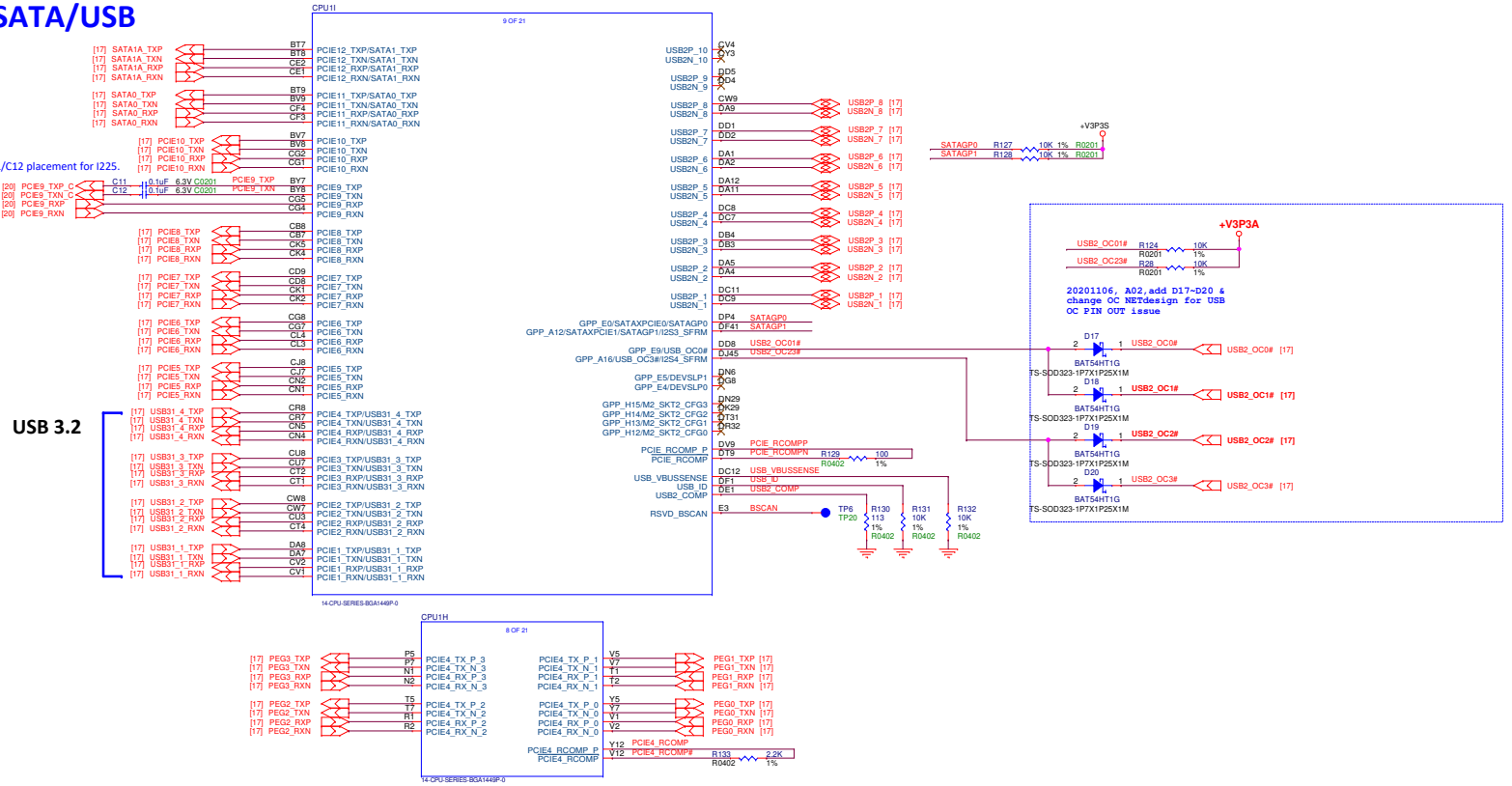
Date: Monday, November 23, 2020 Sheet 8 of 36

SoC PCIe/SATA/USB

20201106, A02, Change C11/C12 placement for I225.

LAN_GbE

USB 3.2



Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4			GbE	GbE	GbE		SATA 0	SATA 1

<Variant Name>

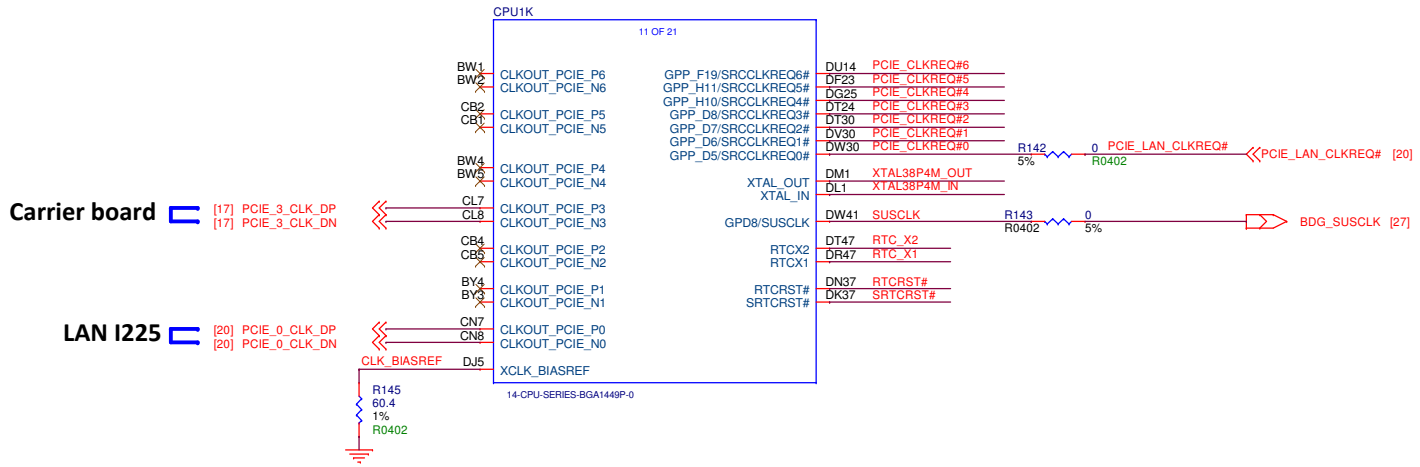
AAEON Technology INC.

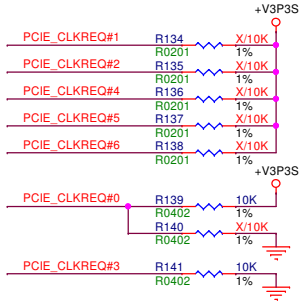
Title: SoC PCIe/SATA/USB

Size | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 9 of 36

SoC PCIE_CLK/ RTC/ XTAL

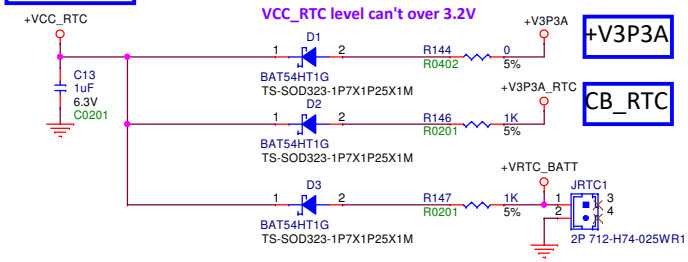


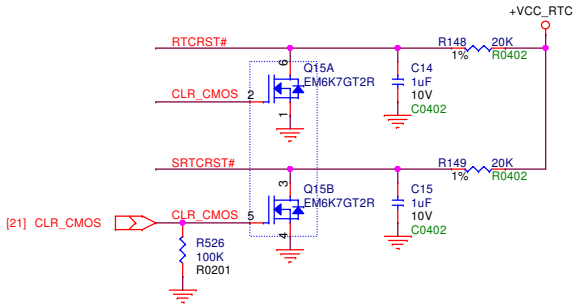


CLKOUT_PCIE_P /N [6:4, 2:1] = Support up to PCIe Gen3
CLKOUT_PCIE_P /N [3, 0] = Support up to PCIe Gen4

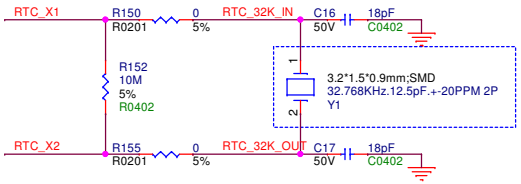
+VCC_RTC

SOC_RTC



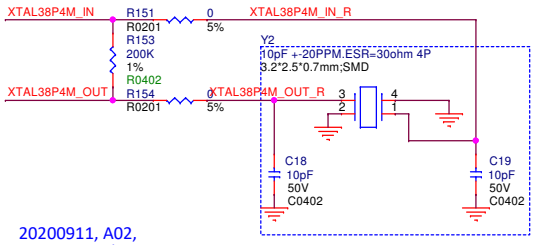


XTAL 32.768KHz



20200911, A02, Change P/N of Y1 from 1231327631 to 1231327632 by test result.

XTAL 38.4MHz



20200911, A02,
1. Change P/N of Y2 from 1231038450 to 1231038451 by test result.
2. Change value of C18/C19 from 15pF to 10pF by test result.

RTC_RESET

Status of CLR_CMOS at G3/S5/S0		
CLR_CMOS	RTCRST#	SRTCRST
HIGH (SW"SHORT")	RESET	RESET
LOW (SW"OPEN")	Normal Operation	Normal Operation

<Variant Name>

AAEON Technology INC.

Title	SoC PCIE_CLK/ RTC		
Size	Document Number		Rev
A3	COM-TGUC6		A0.2_0_0
Date:	Monday, November 23, 2020	Sheet 10	of 36

SoC CNVi

GPP_F0	XTAL SEL1
0 *	38.4/19.2MHZ (DEFAULT)
1	24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

* Default, Internal Pull-Down 20k
24 MHz crystal is not supported

+V3P3A

R156 R0402 X/4.7K 1% GPP_F0

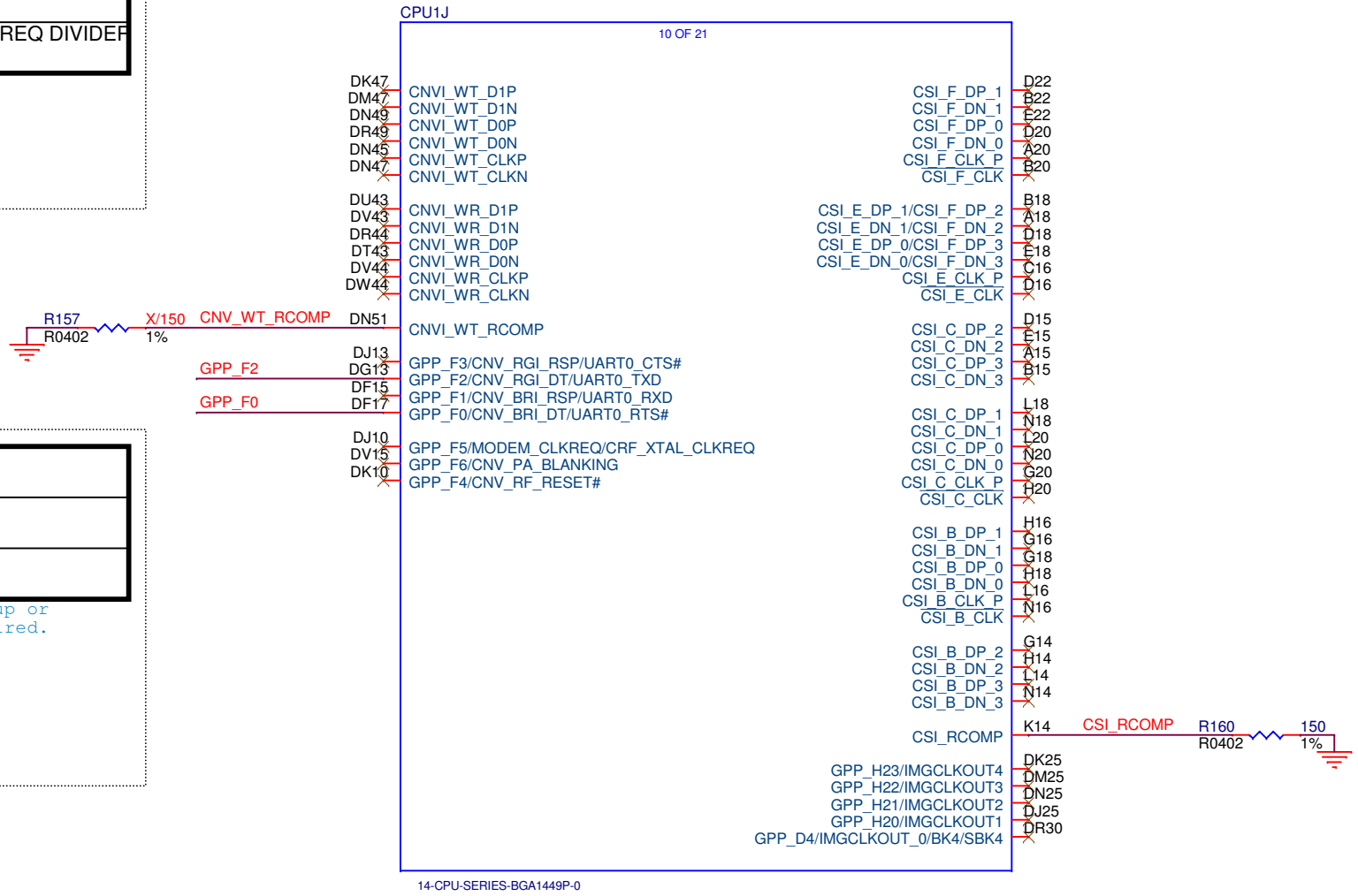
GPP_F2	M.2 CNVi Mode Select
0 *	Integrated CNVi enabled.
1	Integrated CNVi disabled.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.

+V3P3A

R158 R0402 4.7K 1% GPP_F2

R159 R0402 X/20K 1%



<Variant Name>

AAEON Technology INC.

Title: SoC CNVi

Size | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 11 of 36

SoC System

GPD7	Reserved
	This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

This strap has a 20 kohm ± 30% internal pull-down.

+V3P3A

R167 R0402 X/4.7K 1% GPD_7
R169 R0402 X/20K 1%

SPIVCCIOSEL	STRAP FOR SPI 1.8V/3.3V SELECTION
0 *	3.3 V
1	1.8 V

An external resistor is required.

+V3P3A

R172 R0402 X/4.7K 1% SPIVCCIOSEL
R176 R0402 4.7K 1%

+VCC_RTC

R179 R0402 1M 1% SM_INTRUDER#

PDG: DSW_PWROK and RSMRST# are always separate power good signals

R184 R0201 1M 5% PCH_DPWROK
C20 C0201 X/0.01uF 10V

+V3P3S

R185 R0201 X/100K 5% O_SYS_PWROK

R544 R0201 X/100K 5% I_SLP_S4
R545 R0201 X/100K 5% I_SLP_S3
R186 R0201 100K 5% PM_SLP_S0#

20201106, A02, Mount R162 for I225.

+V3P3A

PCIE_WAKE# R161 R0402 1K 1%
LAN_WAKE# R162 R0402 10K 1%
O_BATLOW_R# R163 R0402 8.2K
AC_PRESENT R164 R0201 10K 1%
PWRBTN# R165 R0402 8.2K 1%
EXT_PWR_GATE# R166 R0201 100K 5%
EXT_PWR_GATE2# R168 R0201 100K 5%
PMCALERT# R522 R0402 10K 1%
SX_EXIT_HOLDOFF# R523 R0402 10K 1%

CPU1L

12 OF 21

[33] PM_SLP_SUS# PM_SLP_SUS# DV49
[21] I_SLP_S5 R171 0 5% R0201 SLP_S5# DM43
[21,30,35] I_SLP_S4 R173 0 5% R0201 SLP_S4# DJ41
[21] I_SLP_S3 R174 0 5% R0201 SLP_S3# DJ43
TP8 TP20 SLP_A# DR41
TP9 TP20 SLP_WLAN# DT44
[35] PM_SLP_S0# PM_SLP_S0# R177 0 5% R0201 SLP_S0# DD42
TP10 TP20 SLP_LAN# DN39
RSMRST# DM35
PCH_SYSRST# DD10
PLTRST# DD41
R178 R0402 X/0 5%
[22] PCH_DPWROK PCH_DPWROK R180 R0402 0 5% DSW_PWROK DK35
[21] O_SYS_PWROK O_SYS_PWROK DF10
PCH_PWROK DN35
[35] PCH_PWROK
SM_INTRUDER# DM37
SPIVCCIOSEL DT49

SLP_SUS#
GPD10/SLP_S5#
GPD5/SLP_S4#
GPD4/SLP_S3#
GPD6/SLP_A#
GPD9/SPL_WLAN#
GPP_B12/SLP_S0#
SLP_LAN#
RSMRST#
SYS_RESET#
GPP_B13/PLTRST#
DSW_PWROK
SYS_PWROK
PCH_PWROK
INTRUDER#
SPIVCCIOSEL

PROCPWRGD
GPD3/PWRBTN#
GPD0/BATLOW#
GPD1/ACPRESENT
GPP_B11/PMCALERT#
GPP_H18/CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON
GPD7
VCCSTPWRGOOD_TCSS
VCCST_PWRGD
VCCST_OVERRIDE
GPP_F20/EXT_PWR_GATE#
GPP_F21/EXT_PWR_GATE2#

BM9 CPUPWRGD TP20 TP7
DK41 PWRBTN# R170 0 5% R0201 O_BATLOW# O_PWR_BTN# [21]
DN41 O_BATLOW_R# R175 0 5% R0201 O_BATLOW# [21]
DK43 AC_PRESENT
CW40 PMCALERT#
DN27 CPU_C10_GATE# CPU_C10_GATE# [35]
DG31 SX_EXIT_HOLDOFF#
DK39 PCIE_WAKE# PCIE_WAKE# [17]
DM41 LAN_WAKE# LAN_WAKE# [20]
DT41 GPD11_GPO GPD11_GPO [20]
DN43 GPD_7
CE5 VCCSTPWRGOOD
BP8 VCCST_PWRGOOD R182 R0402 60.4 1% H_VCCST_PWRGD [35]
BP9 VCCST_OVERRIDE
DR12 EXT_PWR_GATE#
DW12 EXT_PWR_GATE2#

14-CPU-SERIES-BGA1449P-0

VCCSTPWRGOOD R181 R0201 0 5% VCCST_OVERRIDE_R VCCST_OVERRIDE_R [35]
VCCST_OVERRIDE R183 R0201 0 5%

Dual Bus Buffer Gate with 3-State Outputs

+V3P3A

C21 0.1uF 6.3V C0201

U5
SN74LVC2G125DCUR
1 1OE
2 1A
3 2Y
4 GND
8 VCC
7 2OE
6 1Y
5 2A

PLTRST#
R187 100K 5% R0201
BUF_CB_RST# BUF_CB_RST# [17]
R190 X/100K 1% R0402
PLTRST#
BUF_PLT_RST#
PCIE_RST COMe is RSVD , R Default Empty
BUF_PLT_RST# [20,21,23,24,25,26,27]

Carry Board
PCIE_RST*2

eSPI to LPC
eDP to LVDS
DDI to VGA
LAN
EC
TPM

SYSRST#

+V3P3A

R192 10K 1% R0201
PCH_SYSRST#
D4 40V 1PS79SB30 TS-SOD523 O_SYSRST# O_SYSRST# [21]
D5 40V 1PS79SB30 TS-SOD523 CARRY_SYSRST# CARRY_SYSRST# [17]

<Variant Name>

AAEON Technology INC.
Title: SoC System
Size: A3 | Document Number: COM-TGUC6 | Rev: A0.2_0_0
Date: Monday, November 23, 2020 | Sheet 12 of 36

SoC Strap

CFG14	PEG* Static x4 Lane Numbering Reversal
0	Lane numbers reversed
1 *	Normal operation

The CFG signals have a default value of '1'

+VCCIO_OUT
R193 X/10K R0402 1% CFG14
R194 X/1K R0402 1%

+VCCIO_OUT
R197 1K R0402 1% CFG1
R195 1K R0402 1% CFG2
R198 1K R0402 1% CFG3
R199 1K R0402 1% CFG9
R200 1K R0402 1% CFG10
R201 1K R0402 1% CFG11

CFG4	eDP Presence
0 *	ENABLE
1	DISABLE

The CFG signals have a default value of '1'

+VCCIO_OUT
R207 X/10K R0402 1% CFG4
R209 1K R0402 1%

CFG7	PEG Training
0	PEG Wait for BIOS for training
* 1	PEG Train immediately following RESET# de assertion

The CFG signals have a default value of '1'

+VCCIO_OUT
R211 X/10K R0402 1% CFG7
R212 X/1K R0402 1%

[17] PEG_LANE_RV#
TP11 TP20 R196 1K R0402 1% TP13 TP20 TP14 TP20 TP12 TP20 TP15 TP20 TP16 TP20 TP17 TP20 R202 49.9 R0402 1% TP18 TP20 TP19 TP20 +VCCIO_OUT
R203 X/10K 1% R0201 R204 X/10K 1% R0201 R205 X/10K 1% R0201 R206 X/10K 1% R0201
R208 2.2K R0402 1%

CPU1T
20 OF 21

CFG_15	CFG15	T15	
CFG_14	CFG14	V17	
CFG_13	CFG13	U15	
CFG_12	CFG12	K11	
CFG_11	CFG11	K12	
CFG_10	CFG10	K9	
CFG_9	CFG9	T17	
CFG_8	CFG8	K7	
CFG_7	CFG7	H7	
CFG_6	CFG6	K8	
CFG_5	CFG5	H9	
CFG_4	CFG4	E6	
CFG_3	CFG3	H5	
CFG_2	CFG2	E9	
CFG_1	CFG1	D9	
CFG_0	CFG0	E7	
CFG_RCOMP	CFG_RCOMP	B5	
CFG_17	CFG17	U17	
CFG_16	CFG16	H11	
BPM#_3	BPM3	Y1	
BPM#_2	BPM2	M4	
BPM#_1	BPM1	AB4	
BPM#_0	BPM0	Y2	
RSVD_6		A3	
RSVD_7		B3	
TCP0_MBIAS_RCOMP	TCP0_MBIAS_RCOMP	AR2	
RSVD_TP_2		AL10	
RSVD_TP_3		AM12	
RSVD_TP_4		AH12	
RSVD_TP_5		AJ10	
RSVD_TP_6		AR1	
RSVD_8		BN10	
RSVD_9		BM12	
RSVD_10		DD13	
RSVD_11		DF13	

RSVD_TP_7	A51
RSVD_TP_8	B51
RSVD_TP_9	C1
RSVD_TP_10	D2
RSVD_TP_11	CP39
RSVD_TP_12	CU40
RSVD_12	AK9
RSVD_13	AH9
RSVD_14	DW6
RSVD_15	DV6
RSVD_TP_13	DV4
RSVD_TP_14	DW3
RSVD_TP_15	DU1
RSVD_TP_16	DT2
RSVD_TP_17	DW2
RSVD_TP_18	DV2
RSVD_TP_19	E1
RSVD_TP_20	F1
RSVD_16	AB2
RSVD_TP_21	DR1
RSVD_TP_22	DR2
RSVD_TP_23	DR53
RSVD_TP_24	DW5
VSS_1	DV51
TP_3	DW52
TP_4	DV53
RSVD_17	W34
RSVD_18	V35
SKTOCC#	D52

VSS_1 TP20 TP20
+V3P3A
SKTOCC# R210 R0402 X/100K 1%

14-CPU-SERIES-BGA1449P-0

<Variant Name>

AAEON® An ASUS Company

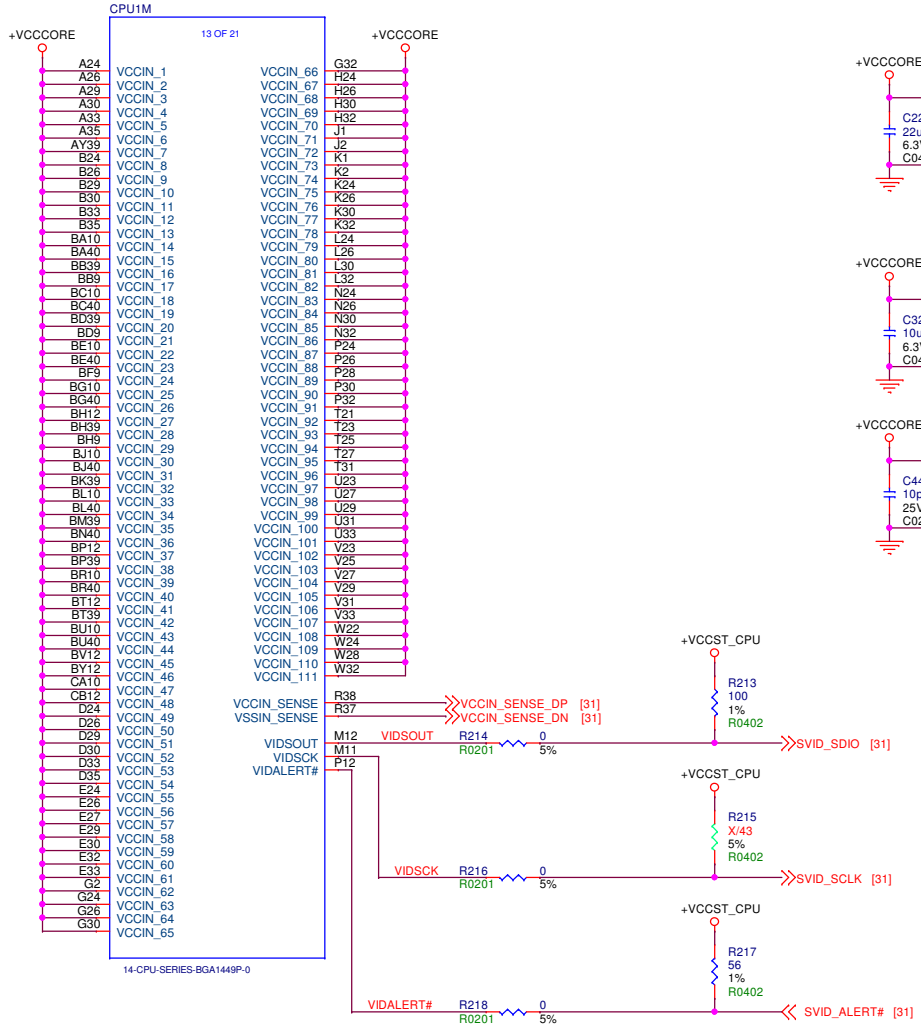
AAEON Technology INC.

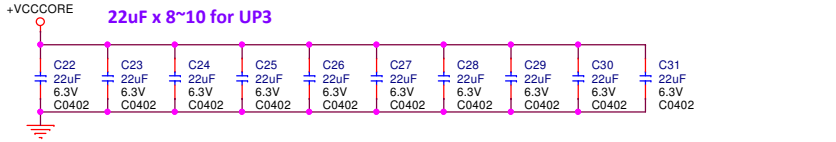
Title: SoC Strap

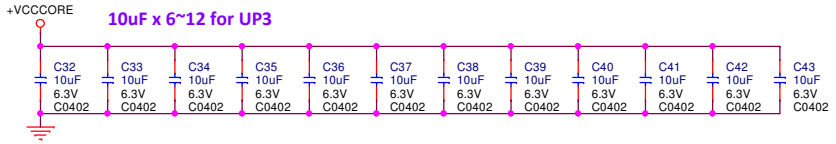
Size	Document Number	Rev
A4	COM-TGUC6	A0.2_0_0

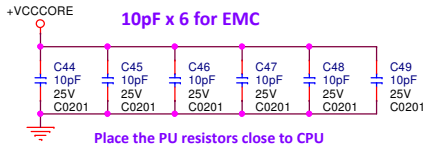
Date: Monday, November 23, 2020 Sheet 13 of 36

SoC Power









<Variant Name>

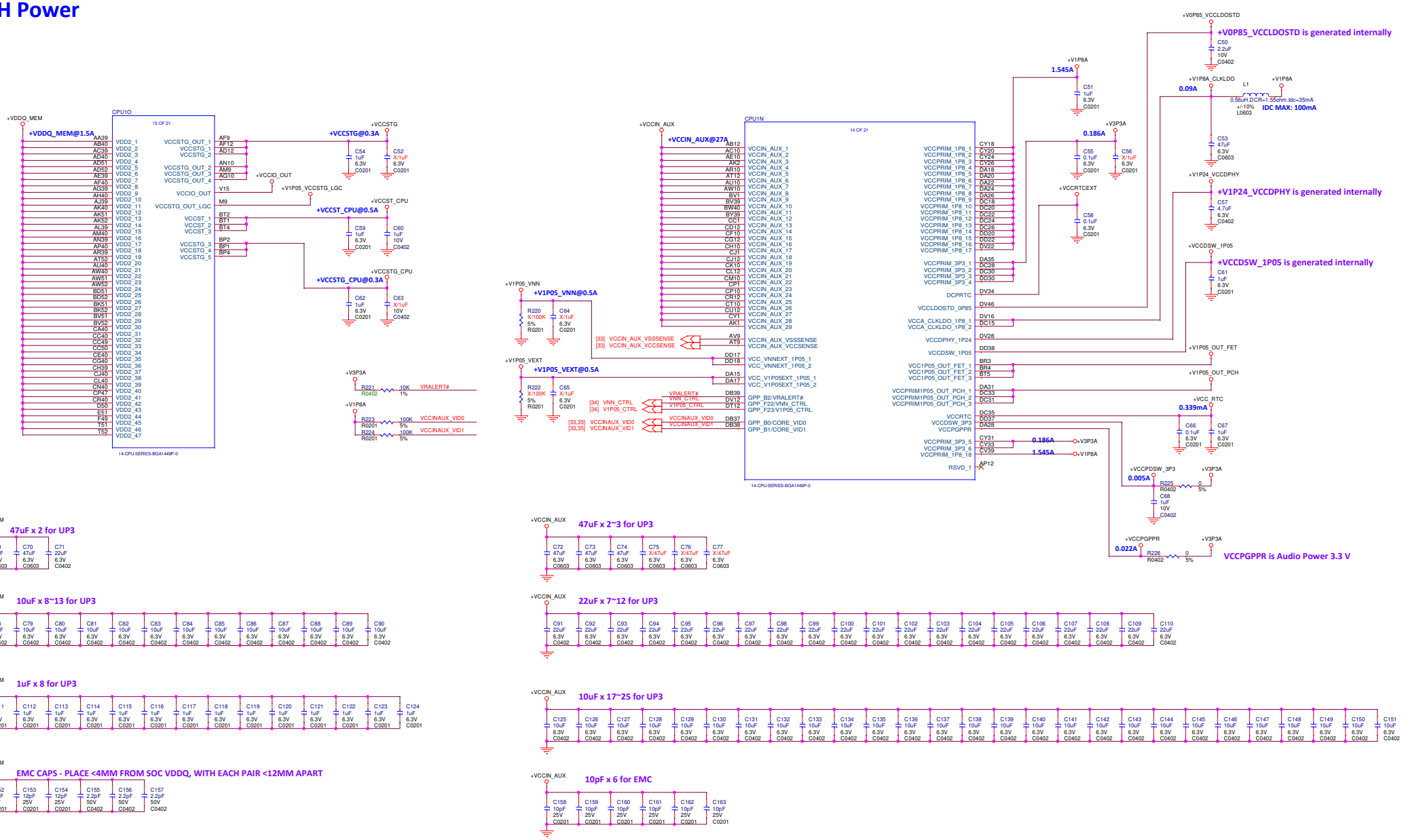
AAEON Technology INC.

Title: SoC Power1

Size | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 14 of 36

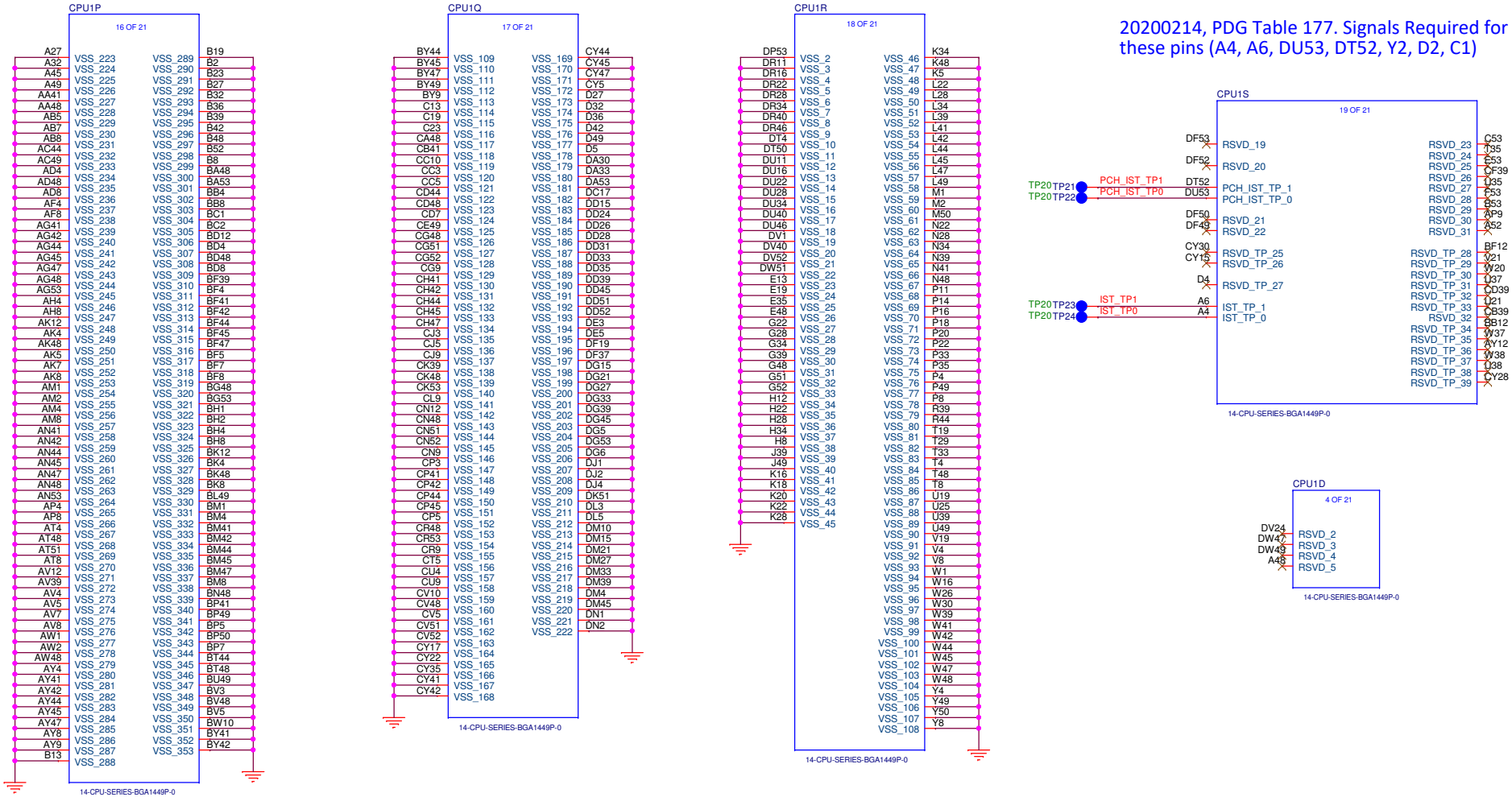
PCH Power



<variant_name>

AAEON Technology INC.			
Title: PCH Power			
Size: A2	Document Number: COM-TGUC6		Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 15 of 36		

SoC GND

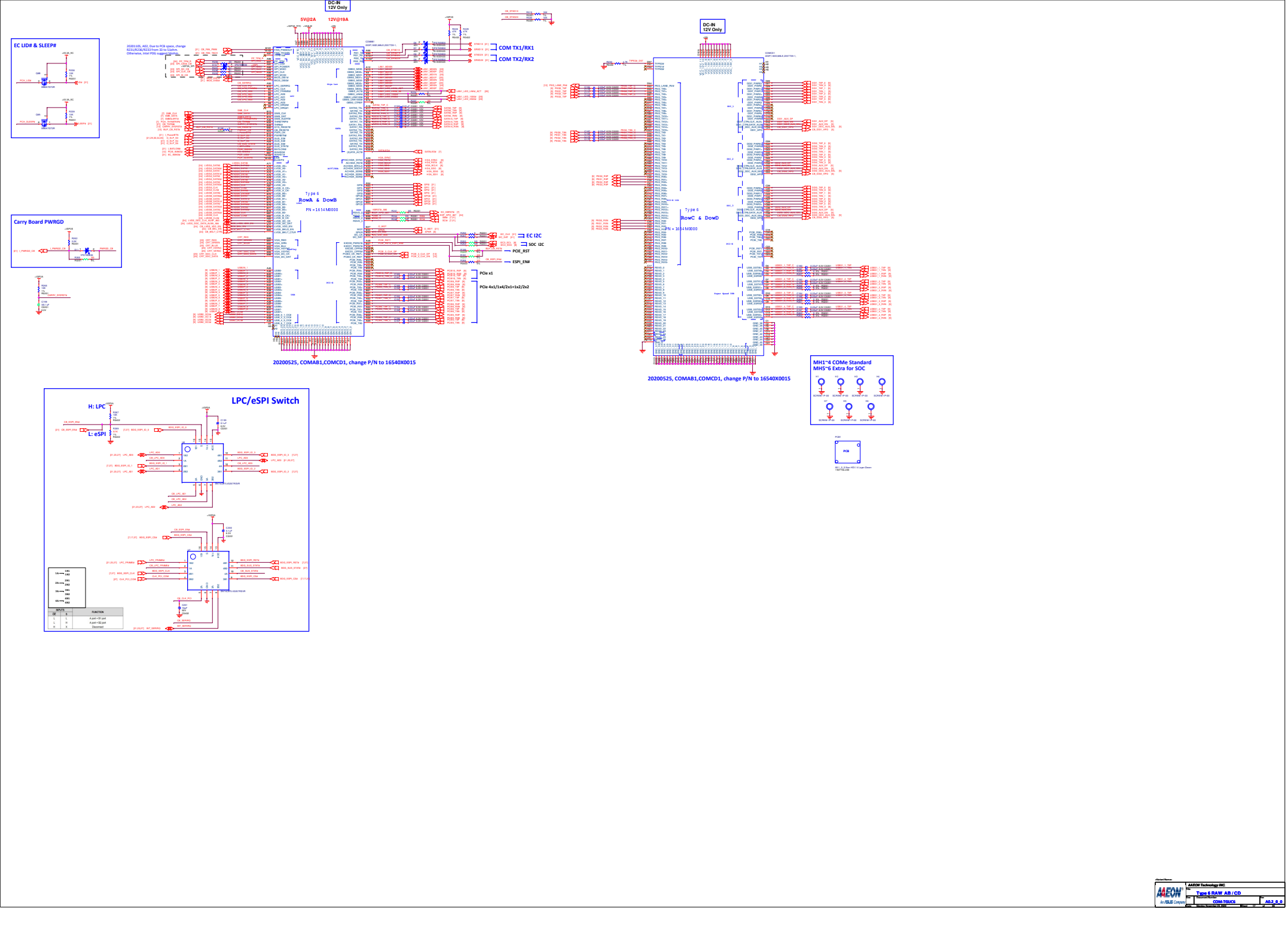


20200214, PDG Table 177. Signals Required for IFDIM at these pins (A4, A6, DU53, DT52, Y2, D2, C1)

<Variant Name>

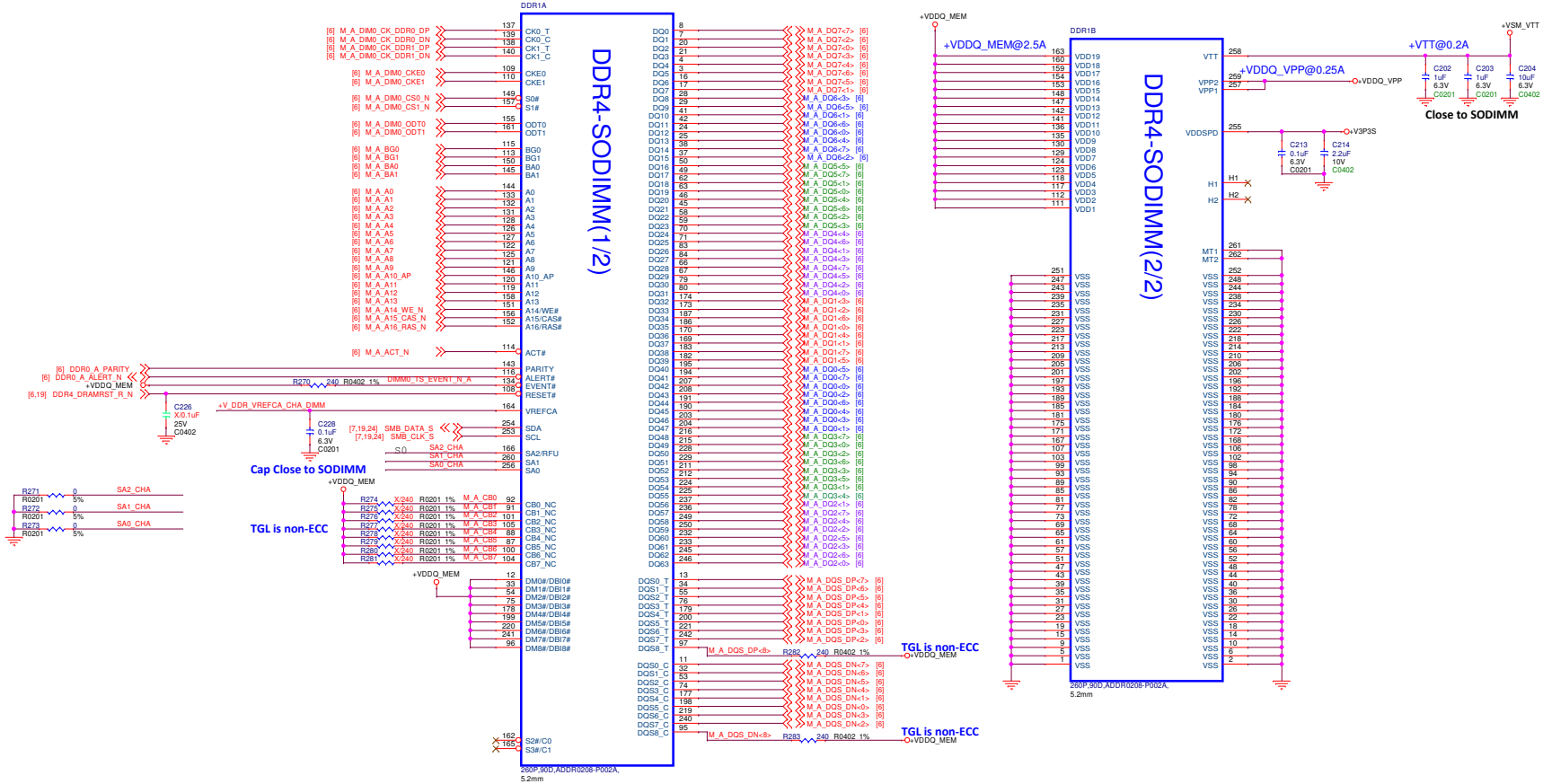
AAEON Technology INC.

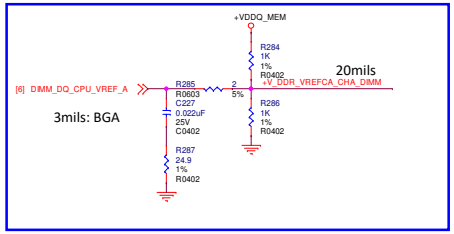
Title	SoC GND	
Size	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 16 of 36	


EC LID# & SLEEP#
Carry Board PWRGD
DC-IN
12V Only
5V@2A
12V@19A
COM TX1/RX1
COM TX2/RX2
EC I2C
SOC I2C
PCIE_RST
ESPI_EN#
PCIe x1
PCIe 4x1/1x4/2x1+1x2/2x2
Type 6
RowA & DowB
PN = 1654M0000
20200525, COMAB1,COMCD1, change P/N to 16540X0015
Type 6
RowC & DowD
PN = 1654M0000
20200525, COMAB1,COMCD1, change P/N to 16540X0015
MH1~4 COMe Standard
MH5~6 Extra for SOC
LPC/eSPI Switch
H: LPC
L: eSPI
INPUTS
OE
S
FUNCTION
L
L
A port = B1 port
L
H
A port = B2 port
H
X
Disconnect
AAEON Technology INC.
Type 6 RAW AB / CD
COM-TGUC6
A0.2_0_0

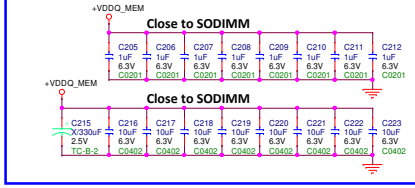
DDR4 SODIMM_A

H= 5.2mm

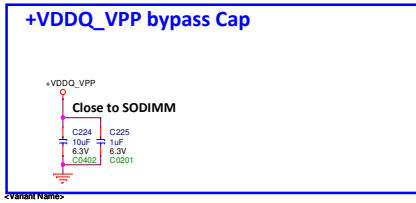




+VDDQ_MEM bypass Cap



+VDDQ_VPP bypass Cap



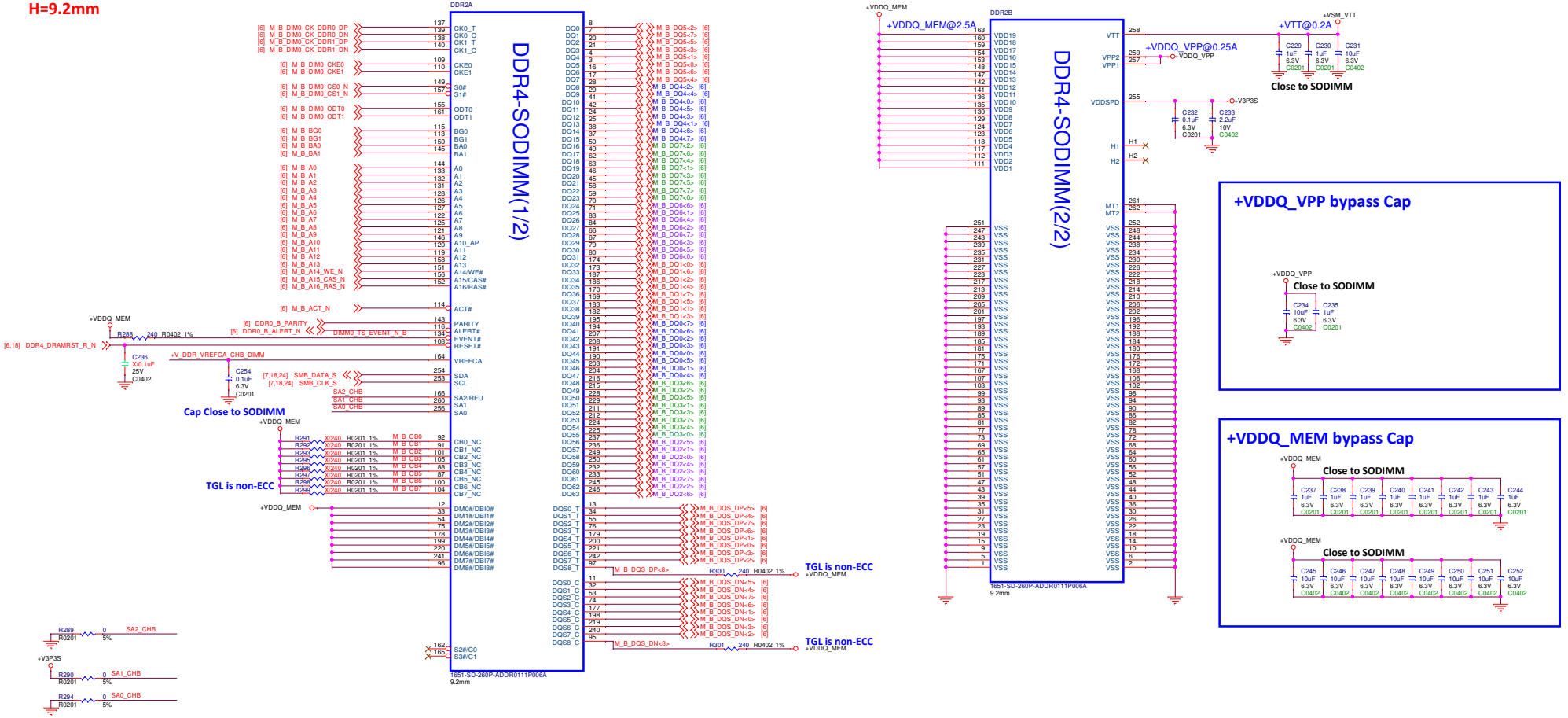
<Variant Name>

AAEON Technology INC.

Title	DDR4 MEM		
Size	Document Number		Rev
A2	COM-TGUC6		A0.2_0_0
Date:	Monday, November 23, 2020	Sheet 18	of 36

DDR4 SODIMM_B

H=9.2mm



<variant_name>

AAEON Technology INC.

Title	DDR4 MEM	
Size: A2	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 19 of 36	

LAN I225

20201106, A02, Change ethernet controller from I219 to I225.

Place each one 22uF & one 0.1uF on pin9 & 38.
0.1uF one at each 0.9V pin

+V0P9A_LAN

C369 22uF 6.3V C0402 | C368 22uF 6.3V C0402 | C367 22uF 6.3V C0402 | C366 0.1uf 10V C0201 | C365 0.1uf 10V C0201 | C364 0.1uf 10V C0201 | C255 0.1uf 10V C0201 | C256 0.1uf 10V C0201 | C257 0.1uf 10V C0201

+V0P9A_LAN_CRTL & +V0P9A_LAN
PWR plane keep short and wide

+V0P9A_LAN_CRTL — L36 1uH,3.5A,45mohm — +V0P9A_LAN

R573 R0201 0 5%

Place one 22uF & one 0.1uF on pin7.
0.1uF one at each 3.3V pin

0.67A

+V3P3A_LAN

C261 22uF 6.3V C0402 | C371 22uF 6.3V C0402 | C370 22uF 6.3V C0402 | C372 0.1uf 10V C0201 | C375 0.1uf 10V C0201 | C376 0.1uf 10V C0201 | C373 0.1uf 10V C0201 | C258 0.1uf 10V C0201 | C259 0.1uf 10V C0201 | C260 0.1uf 10V C0201

R53 R0603 0 5% — +V3P3A

*SMBUS DESIGN NOTE:
1225 Default SMBUS Address is 0x49.

*SMBUS DESIGN NOTE:
1. I225 SMBUS speed default is 1MHz so the pull-ups should be 499ohm.
2.When adding VoltageShifter/Buffer/Repeater on the SMBUS, the pull-up value might change to 1Kohm.
3.Change the pull-ups to 2.2Kohm when runs @400KHz or 10Kohm when runs @100KHz.

*PCIe DESIGN NOTE:
PCIe must be configured as a standard PCIe port. Do Not configure to the Gbe port (like I219).

U29

+1.0V_CTRL1, +1.0V_CTRL2, +1.0V_CORE1, +1.0V_CORE2, +1.0V_VP, +1.0V_A1, +1.0V_A2, +1.0V_A3, RESERVED, +3.3V_A1, +3.3V_A2, +3.3V_DC, +3.3V_PAD1, +3.3V_PAD2, +3.3V_VPH, +3.3V_XO, +3.3V_CDB

Foxville I225

[9] PCIE9_RXP — C374 0.1uF 6.3V C0201 — LAN1_PET_P — PE_TX_P
[9] PCIE9_RXN — C377 0.1uF 6.3V C0201 — LAN1_PET_N — PE_TX_N
(9) PCIE9_TXP_C — PE_RX_P
(9) PCIE9_TXN_C — PE_RX_N
[10] PCIE_0_CLK_DP — PCIE_0_CLK_DP — PE_CLK_P
[10] PCIE_0_CLK_DN — PCIE_0_CLK_DN — PE_CLK_N
[10] PCIE_LAN_CLKREQ# — R577 0 5% R0201 — PCIE_LAN_CLKREQ# — PE_CLKREQ_N
[12] LAN_WAKE# — R578 0 5% R0201 — LANWAKE_N_R — PE_WAKE_N
[12,21,23,24,25,26,27] BUF_PLT_RST# — PLT_RST#_LAN — PE_RST_N
[7] LAN_SM_CLK — SMB_CLK
[7] LAN_SM_DATA — SMB_DATA
R580 R0201 0 5% — LAN_ULP — ULP_WAKE_N

NVM1_SI — SPI_DIN/AUX_PWR
NVM1_SO — SPI_DOUT
NVM1_SK — SPI_CLK
NVM1_CS# — SPI_CS_N

LAN_XTAL2 — XTAL_IN
LAN_XTAL1 — XTAL_OUT

JTAG_RSTN — JTAG_RSTN
JTAG_TMS — JTAG_TMS/SDP2
JTAG_TDO — JTAG_TDO/MDI_LANE_SWAP
JTAG_TDI — JTAG_TDI/SDP1
JTAG_CLK — JTAG_CLK

MDI_A_P — LAN1_MDI0P — LAN1_MDI0P [17]
MDI_A_N — LAN1_MDI0N — LAN1_MDI0N [17]
MDI_B_P — LAN1_MDI1P — LAN1_MDI1P [17]
MDI_B_N — LAN1_MDI1N — LAN1_MDI1N [17]
MDI_C_P — LAN1_MDI2P — LAN1_MDI2P [17]
MDI_C_N — LAN1_MDI2N — LAN1_MDI2N [17]
MDI_D_P — LAN1_MDI3P — LAN1_MDI3P [17]
MDI_D_N — LAN1_MDI3N — LAN1_MDI3N [17]

LED0 — LAN1_LED_1000# — LAN1_LED_1000# [17]
LED1 — LAN1_LED_2500# — LAN1_LED_2500# [17]
LED2 — LAN1_LED_LNK#_ACT_R

LAN_PWR_GOOD — LAN_PWR_GOOD
LAN_DISABLE_N — LAN_DISABLE#_R — R581 0 5% R0201 — GPD11_GPO [12]

SDP0 — LAN_SDP0
*LAN_SDP0
If need PCB space, could remove R585 & R587 and add Test point.

PHY_CAL — LAN_PHY_CAL
RBIAS — LAN_RBIAS — R589 200 1% R0201 — R590 22K 1% R0402
EPAD — 57

56P,I225-LM SLNNH(version.B3),
TA=0 to 70 °C
QFN56G-7X7-1
(TF)IC.Ethernet.SMD.PCI-E 2.5G GigaBit Ethernet Chipset.VQFN.56P.Intel.I225-LM SLNNH(version.B3)

A02, 20201111 R589 change to 0201

+V3P3A_LAN

LAN_PWR_GOOD — R575 R0201 10K 1%
LAN_DISABLE#_R — R576 R0201 10K 1%
R579 R0201 X/10K 1%

*LAN DISABLE DESIGN NOTE:
Connect I225's LAN_DISABLE_N to PCH's GPIO output is required to support ULP and RTD3 conditions. If not used, keep pull-up R70. (Do not config as PCH's LANPHYPC, which is I219 specific).

+V3P3A_LAN

LAN_SDP0 — R585 R0201 X/10K 1% — R587 R0201 X/10K 1%

*LED DESIGN NOTE:
There is no specific industrial standard for Ethernet LEDs.
This schematic just shows the most common SPEED LED configuration:
Highest Speed = Green
2nd Highest Speed = Yellow
All other lower Speeds = OFF
No Cable/Link = OFF
All LED pins are set active low. See Datasheet for additional info.

+V3P3A_LAN

R582 R0201 10K 1% JTAG_TDI
R583 R0201 10K 1% JTAG_TMS
R584 R0201 10K 1% JTAG_CLK
R586 R0201 10K 1% JTAG_TDO
R52 R0201 X/10K 1% JTAG_RSTN

*Nomal opearation: unmount R52
At low, the JTAG is in the reset state and the multiplexed pins JTAG/SDPs act as SDPs. This pin has an internal weak pull-down that holds the JTAG controller in its reset state if the pin is left open.
*Enable Test Reset. Mount R52.
*If need PCB space, could remove R52 and add Test point.

LAN_XTAL1_R — R588 R0201 0 5% — LAN_XTAL1
Y6 — 25MHz 4P — LAN_XTAL2
C380 10pF 50V C0402 — 10pF.30ppm.2.0*1.6*0.5mm;SMD — C381 10pF 50V C0402

> Intel validated I225 with Cload=18pF Crystals.
I225 might work with Cload=10pF crystal.
When selecting the Cload=10pF crystal component, suggest starting C1=C2=10pF and consult with selected Crystal Part Vendor for their specific requirements.

*Crystal
Trace Length: The crystal trace lengths should be less than 1 inch.

+V3P3A_LAN

R591 R0201 10K 1% NVM1_WP#
R592 R0201 10K 1% NVM1_CS#
R34 R0201 10K 1% NVM1_SI

+V3P3A_LAN

NVM1_HOLD# — R593 R0201 10K 1%
NVM1_SO — R35 R0201 10K 1%
R51 R0201 X/1K 5%

Optional Security Strapping
1.For Development:Mount R51 to disable Flash Security. When updating, NVM.bin file is needed.
2.For Production & Normal Operation: Unmount R51.

+V3P3A_LAN

C382 0.1uf 10V C0201

NVM1_CS# — R594 0 5% R0201 — NVM1_CS#_R
NVM1_SI — R595 0 5% R0201 — NVM1_SI_R
NVM1_WP#

U30
CE# 1 | SO 2 | WP# 3 | VSS 4 | VDD 8 | HOLD# 7 | SCK 6 | SI 5
W25Q80DVSSIG

NVM1_HOLD#
NVM1_SK_R — R596 0 5% R0201 — NVM1_SK — R597 10K 1% R0201
NVM1_SO_R — R598 0 5% R0201 — NVM1_SO

LAN1_LED_LNK#_ACT_R — R599 R0201 10K 1% — LAN1_LED_LNK#_ACT — LAN1_LED_LNK#_ACT [17]

+V3P3A_LAN

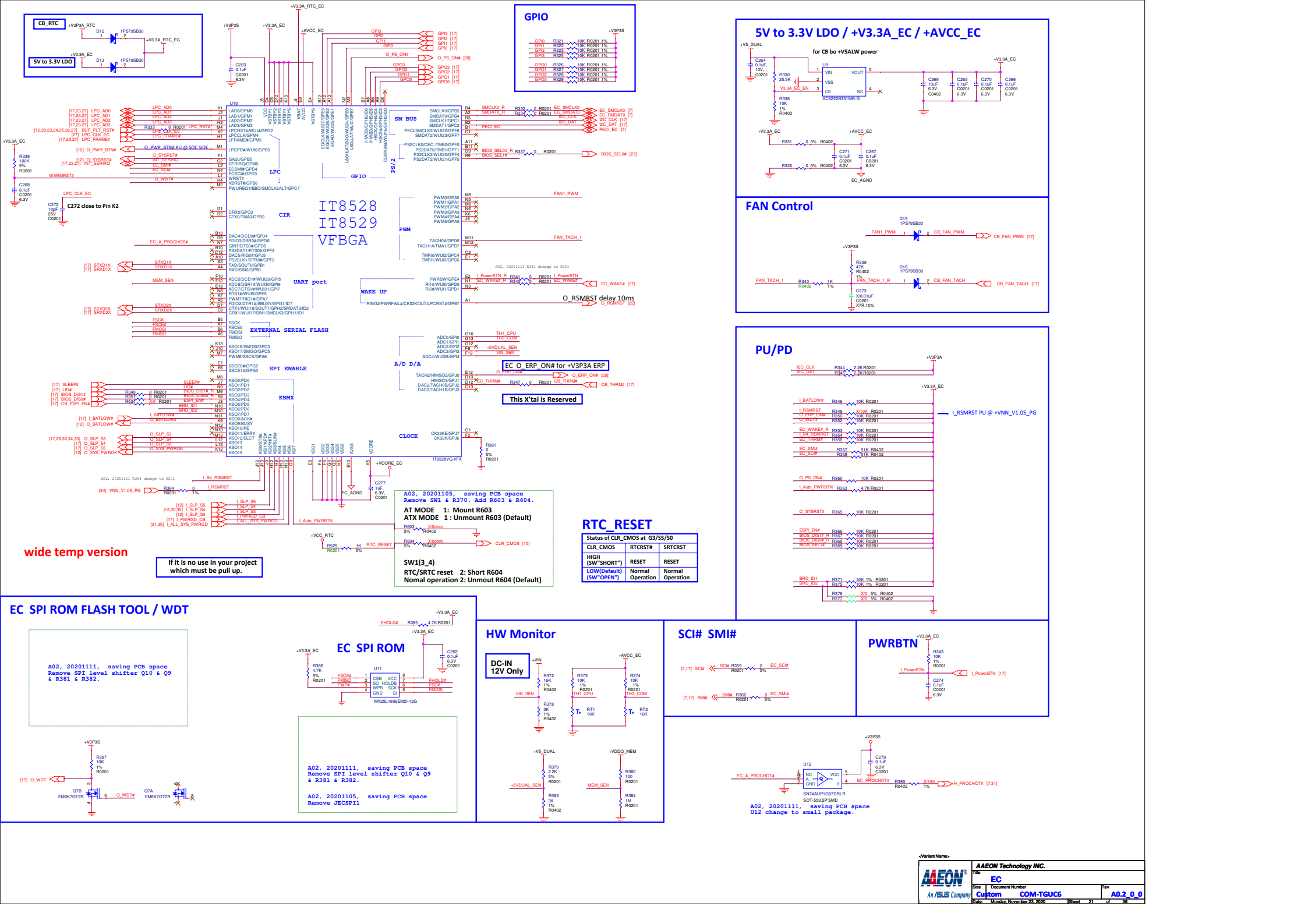
R600 10K 1% R0201 — LAN1_LED_LNK_ACT
Q20B EM6K7GT2R
Q20A EM6K7GT2R

20200904, A02, ADD THE CIRCUIT FOR LAN LED LEAKAGE ISSUE

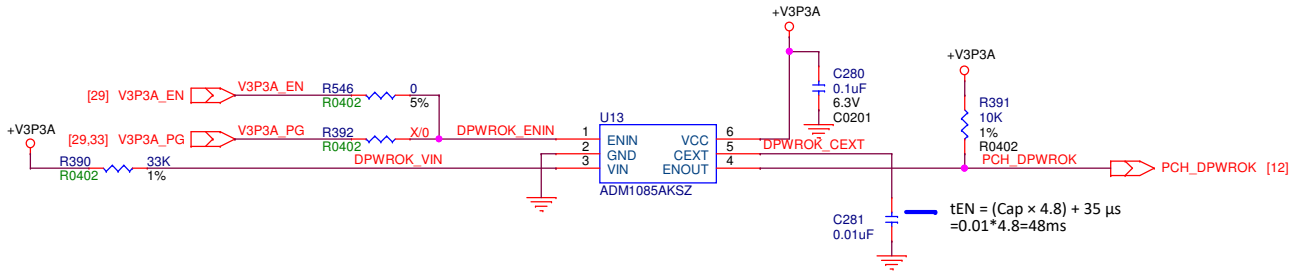
<Core Design>

AAEON Technology INC.

Title	LAN I225	
Size	Document Number	Rev
Custom	COM-TGUC6	A0.2_0_0
Date: Monday, November 23, 2020	Sheet 20 of 36	


CB_RTC
5V to 3.3V LDO
IT8528
IT8529
VFBGA
LPC
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
SM BUS
PS/2
C272 close to Pin K2
This X'tal is Reserved
EC_O_ERP_ON# for +V3P3A ERP
O_RSMRST delay 10ms
wide temp version
If it is no use in your project which must be pull up.
GPIO
5V to 3.3V LDO / +V3.3A_EC / +AVCC_EC
for CB bo +V5ALW power
XC6222B331MR-G
FAN Control
PU/PD
I_RSMRST PU @ +VNN_V1.05_PG
RTC_RESET
Status of CLR_CMOS at G3/S5/S0
CLR_CMOS
RTCRST#
SRTCRST
HIGH (SW"SHORT")
RESET
RESET
LOW(Default) (SW"OPEN")
Normal Operation
Normal Operation
A02, 20201105, saving PCB space
Remove SW1 & R370. Add R603 & R604.
AT MODE 1: Mount R603
ATX MODE 1 : Unmount R603 (Default)
SW1(3_4)
RTC/SRTC reset 2: Short R604
Nomal operation 2: Unmout R604 (Default)
EC SPI ROM FLASH TOOL / WDT
EC SPI ROM
A02, 20201111, saving PCB space
Remove SPI level shifter Q10 & Q9
& R381 & R382.
A02, 20201111, saving PCB space
Remove SPI level shifter Q10 & Q9
& R381 & R382.
A02, 20201105, saving PCB space
Remove JECSPI1
HW Monitor
DC-IN 12V Only
SCI# SMI#
PWRBTN
A02, 20201111, saving PCB space
U12 change to small package.
SN74AUP1G07DRLR
SOT-553.5P;SMD
MX25L1606EM2I-12G
IT8528VG-IFX
AAEON Technology INC.
EC
Custom
COM-TGUC6
A0.2_0_0
Monday, November 23, 2020

DSW_PWROK Control



3.3V x 10 / (10+33) = 0.767

ENIN VIH = 0.3*VCC+0.2 =1.19V

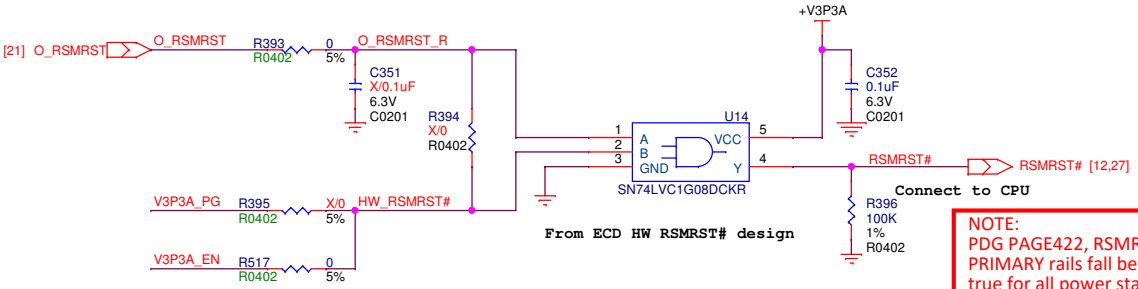
ENIN VIL = 0.3*VCC- 0.2 = 0.79V

ENOUT/ENOUT# Voltage Low (MAX =0.4V),When Vin < Vth_falling (ENOUT) / Vin > Vth_rising (ENOUT#)

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	2.25		3.6	V	
V_{IN} Operating Voltage Range	0		22	V	
Supply Current		10	15	µA	
V_{IN} Rising Threshold, V_{TH_RISING}	0.56	0.6	0.64	V	V_{CC} = 3.3 V
V_{IN} Falling Threshold, $V_{TH\_FALLING}$	0.545	0.585	0.625	V	V_{CC} = 3.3 V
V_{IN} Hysteresis		15		mV	

RSMRST# Control



NOTE:
PDG PAGE422, RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band. This is true for all power states transitions including emergency power loss.

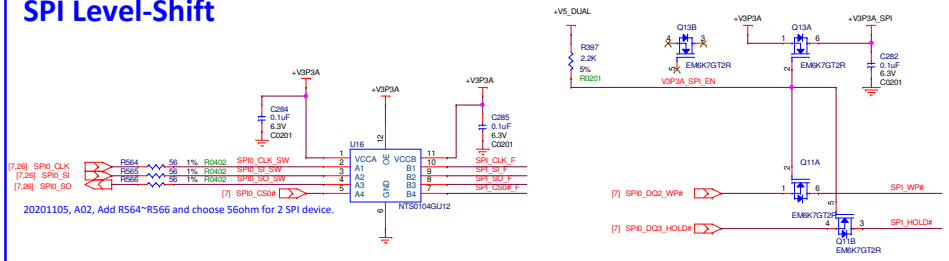
RSMRST# is de-asserted by EC of O_RSMRSTon G3->S5, Asserted by VR of V3P3A_EN at S5->G3 before VccPRIM dropping.

<Variant Name>

AAEON Technology INC.

Title: RSMEST# Control		
Size: B	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 22 of 36	

SPI Level-Shift

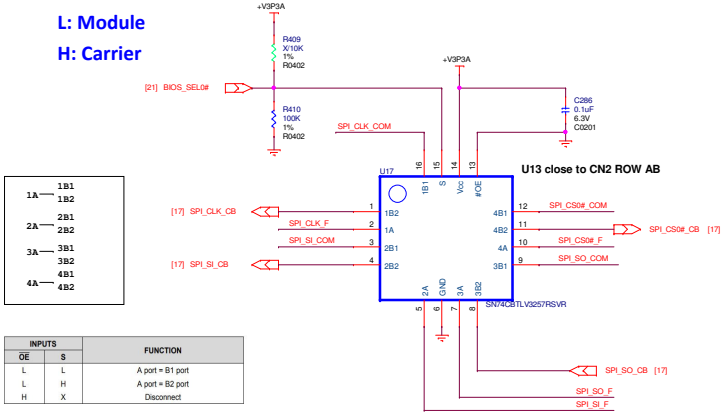


20201105, A02, Add R564~R566 and choose 56ohm for 2 SPI device.

BIOS Switch MB/CB

L: Module

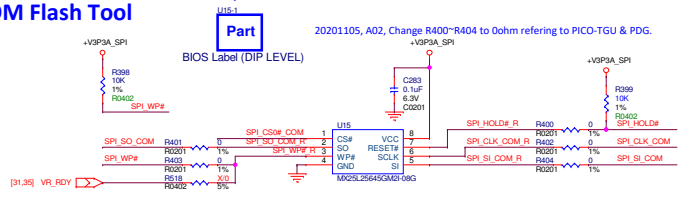
H: Carrier



INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

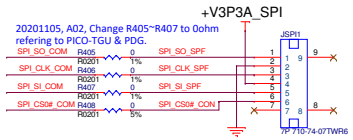
20200526, Add BIOS Label

SPI ROM Flash Tool



20201105, A02, Change R400~R404 to 0ohm refering to PICO-TGU & PDG.

1462002564 / (TF)IC.Flash Memory.256M Bit serial.SOP-8(209mil).w/ Dual & Quad SPI.SMD.MACRONIX.MX25L25645GM2I-08G



20201105, A02, Change R405~R407 to 0ohm refering to PICO-TGU & PDG.

20201105, A02, Remove JLPC1 circuit (80 port conn.) for the PCB spacing of EEPROM of Intel I225.

<Variant Name>

AAEON Technology INC.

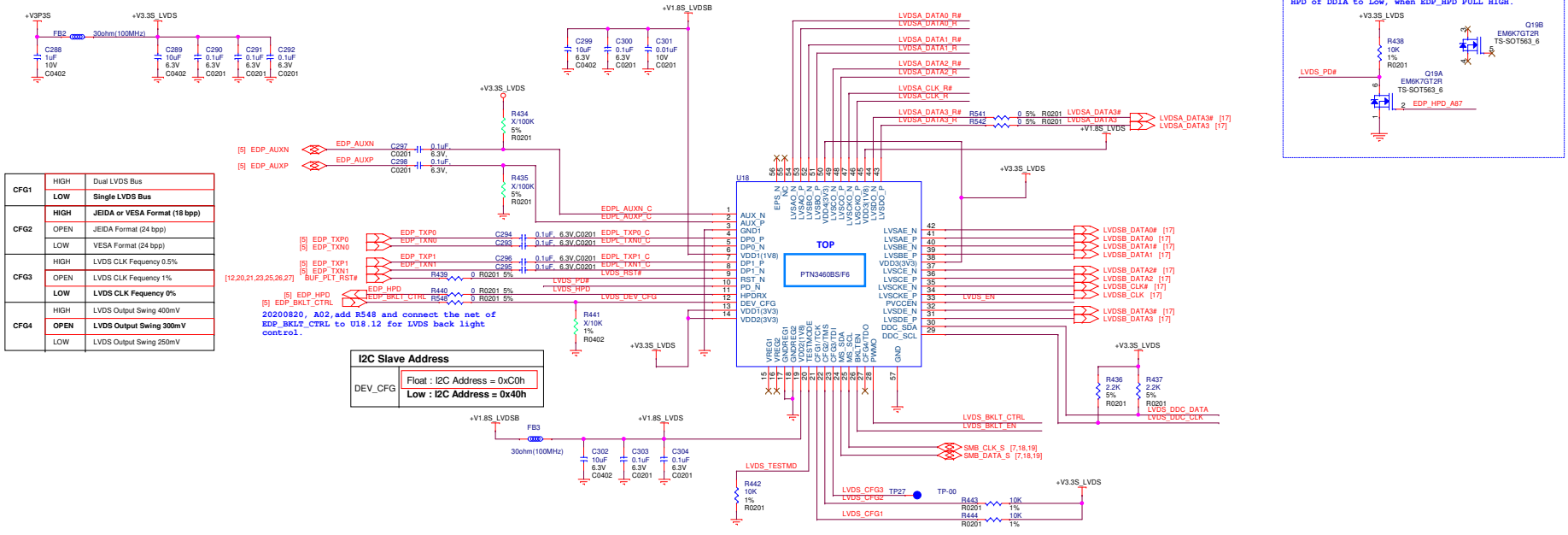
An ASUS Company

Title: FAN/BIOS/ LPC

Size: Custom | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 23 of 36

eDP to LVDS_PTN3460



CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

I2C Slave Address	
DEV_CFG	Float : I2C Address = 0xC0h **Low : I2C Address = 0x40h**

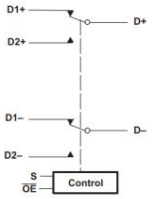
20200901, A02,add Q19 to disable LVDS and pull HPD of DDIA to Low, when EDP_HPD PULL HIGH.

eDP / LVDS CONTROL SWITCH

TRUTH TABLE

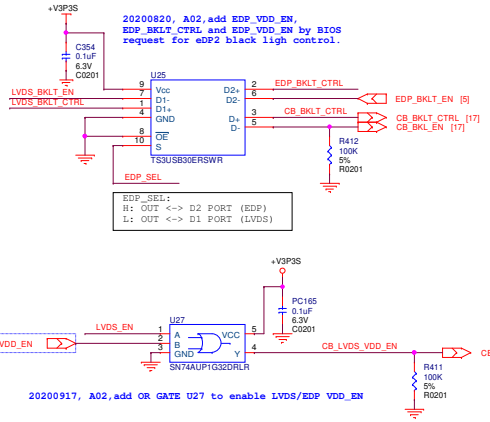
S	OE	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM



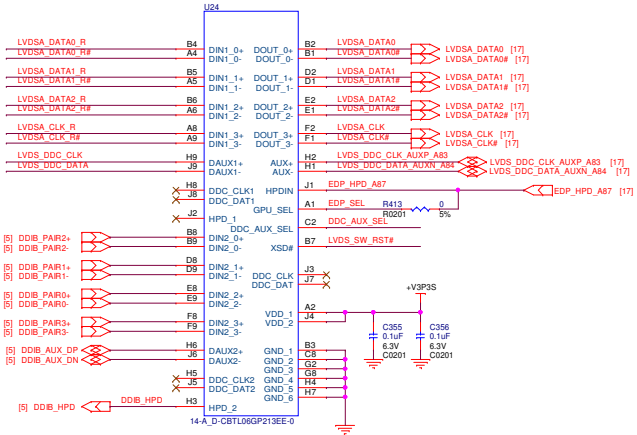
20200922, Change Switch from 142LV32571 to 1420USB300 for down size.

20200820, A02,add EDP_VDD_EN, EDP_BKLT_CTRL and EDP_VDD_EN by BIOS request for eDP2 black ligh control.



20200917, A02,add OR GATE U27 to enable LVDS/EDP VDD_EN

eDP to LVDS SWITCH



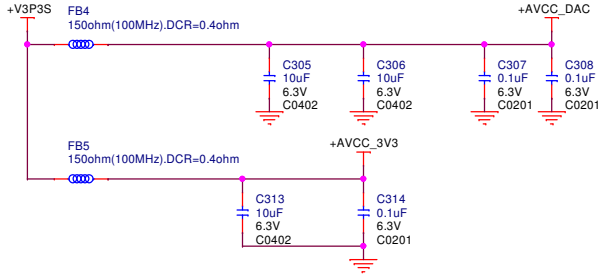
<Variant Name>

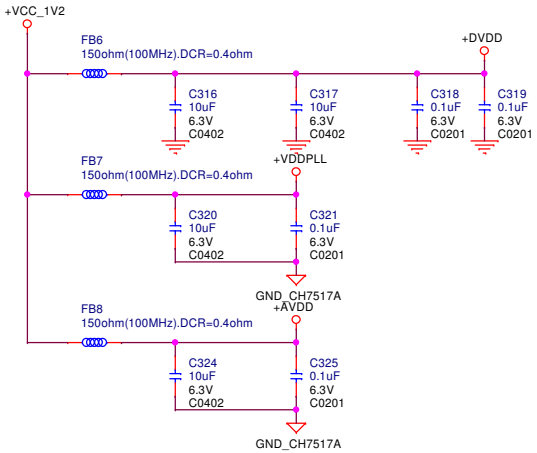
AAEON Technology INC.

Title	eDP to LVDS	
Size	Document Number	Rev
	COM-TGUC6	A0.2_0_0
Date: Monday, November 23, 2020	Sheet 24 of 36	

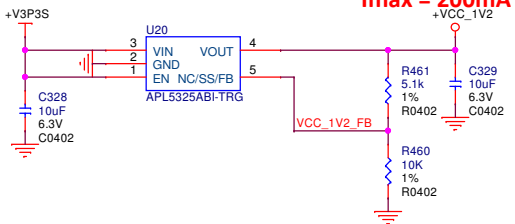
DP to VGA (CH7517)

Note:
1. +1.05V power spply tolerance range -5%~+25%
2. +3.3V power spply tolerance range +/-10%





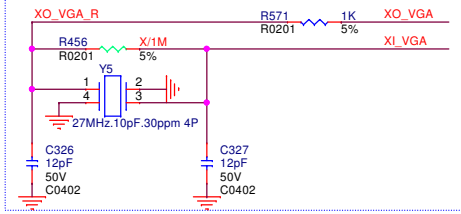
Imax = 200mA



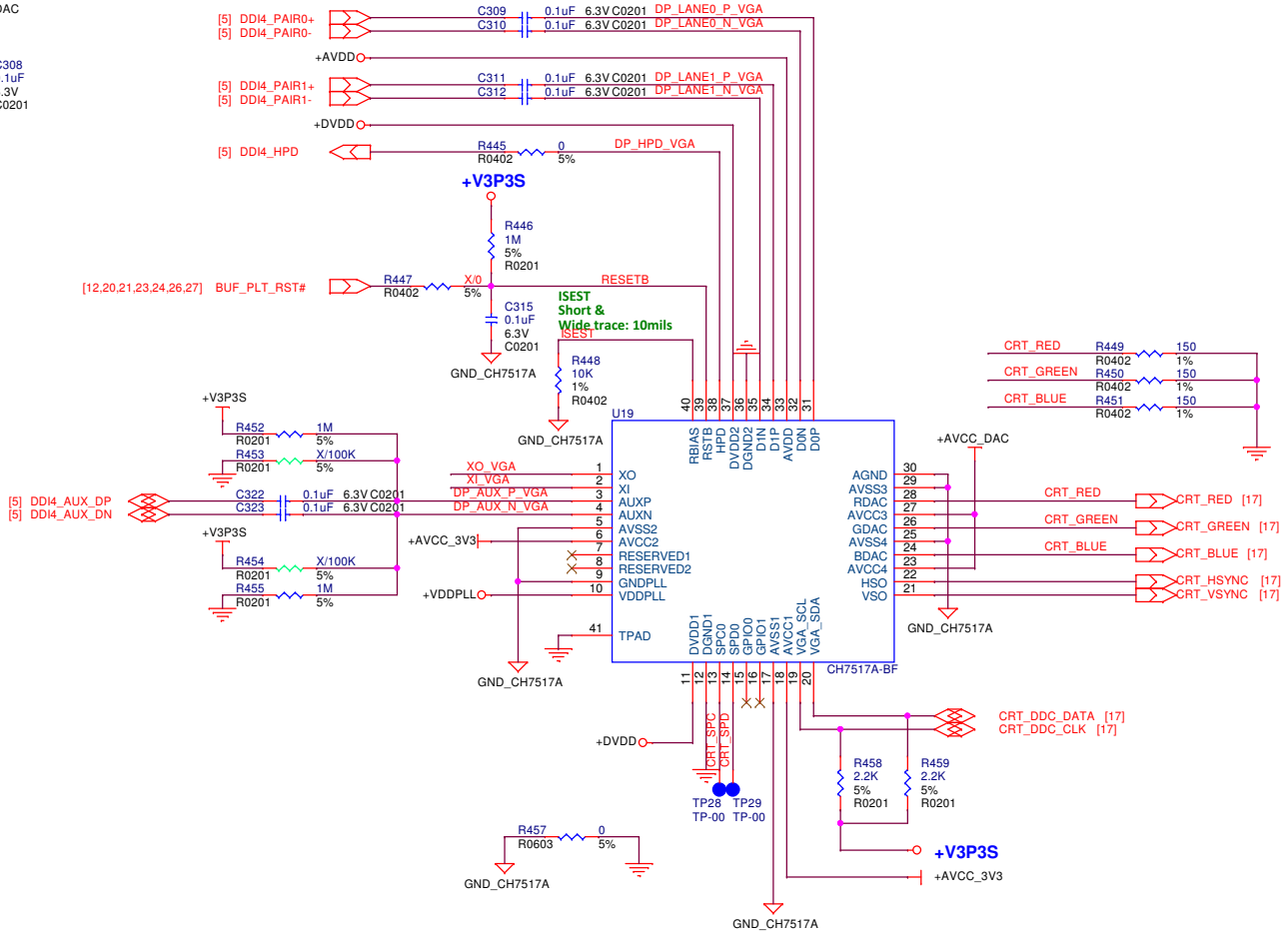
Imax = 200mA

20201007, A02, Change value of C327/C326 from 20pF to 12pF and add R571 for FAE suggestion.

20201110, A02, After confirm with Jake, change R571 from 1.8k ohm(0402) to R54 1k (0201).



CH7517



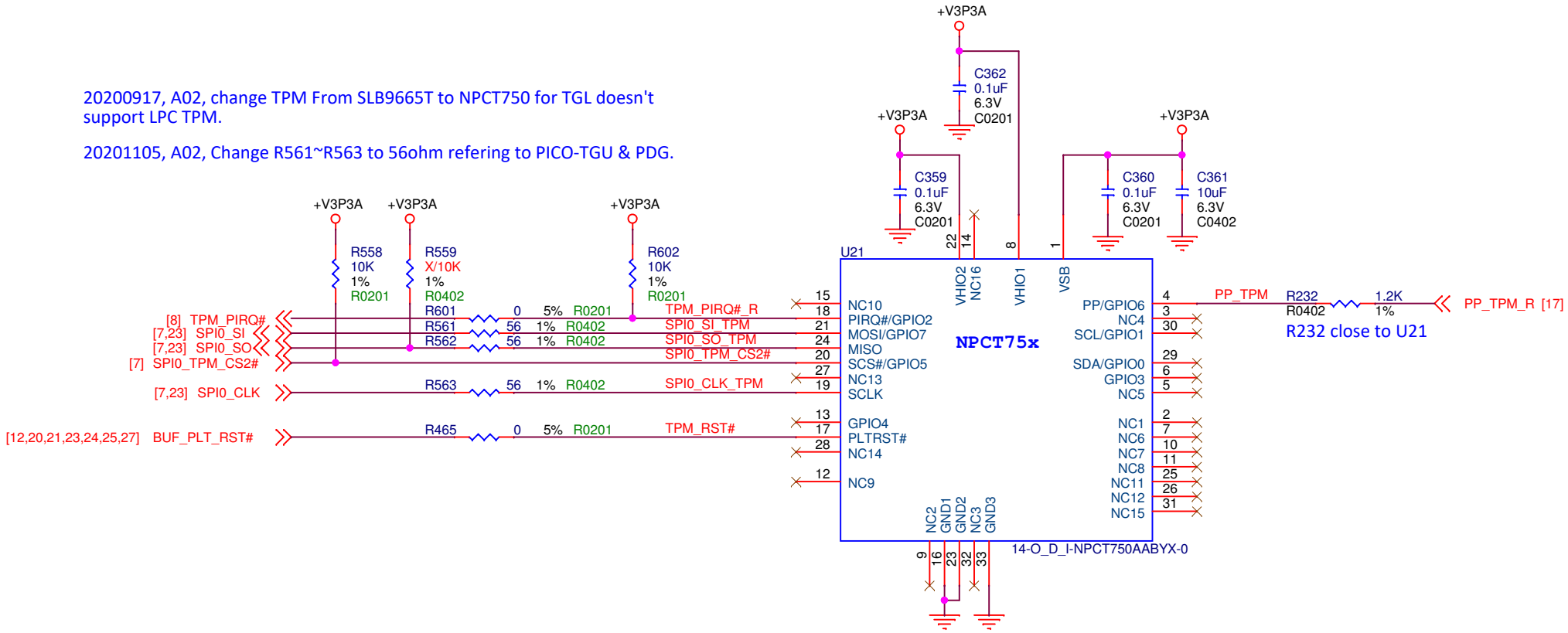
<Variant Name>

AAEON Technology INC.

Title	DDI to VGA	
Size	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 25 of 36	

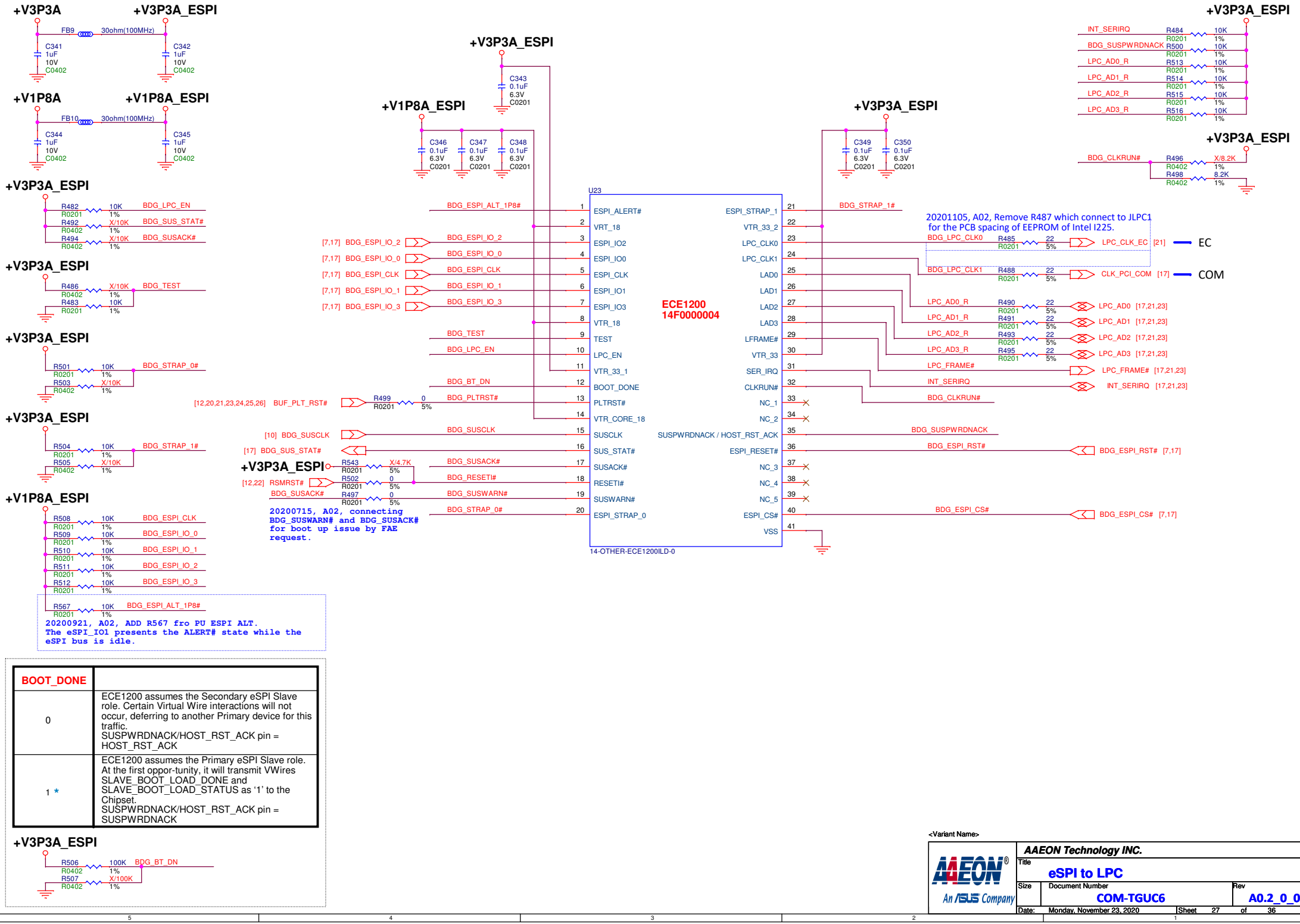
20200917, A02, change TPM From SLB9665T to NPCT750 for TGL doesn't support LPC TPM.

20201105, A02, Change R561~R563 to 56ohm refering to PICO-TGU & PDG.



<Variant Name>

AAEON® An ASUS Company	AAEON Technology INC.	
	Title: TPM	
Size	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 26 of 36	



BOOT_DONE	
0	ECE1200 assumes the Secondary eSPI Slave role. Certain Virtual Wire interactions will not occur, deferring to another Primary device for this traffic. SUSPWRDNACK/HOST_RST_ACK pin = HOST_RST_ACK
1 *	ECE1200 assumes the Primary eSPI Slave role. At the first oppor-tunity, it will transmit VWires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS as '1' to the Chipset. SUSPWRDNACK/HOST_RST_ACK pin = SUSPWRDNACK

<Variant Name>

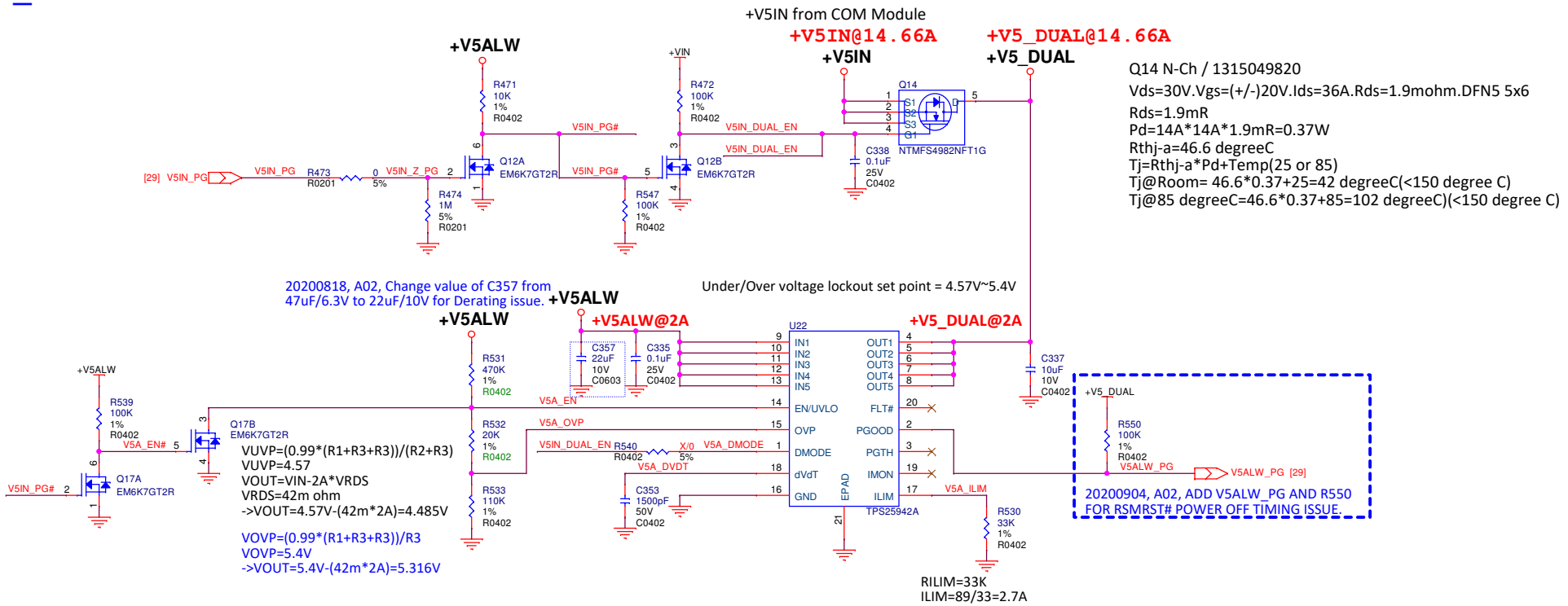
AAEON Technology INC.

Title: eSPI to LPC

Size | Document Number: COM-TGUC6 | Rev: A0.2_0_0

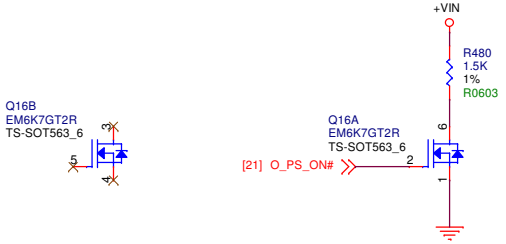
Date: Monday, November 23, 2020 | Sheet 27 of 36

+V5_DUAL switch circuit

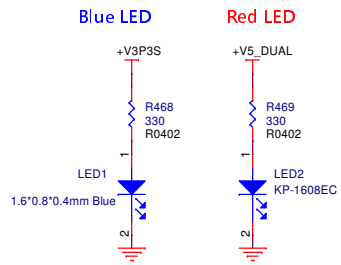


	+V5ALW	V5A_EN S5 -> S0
ATX	ture	H -> L
AT with 5VSB	ture	H -> L
AT without 5VSB	false	L -> L (U22 Always disable)

Discharge Circuit



LED

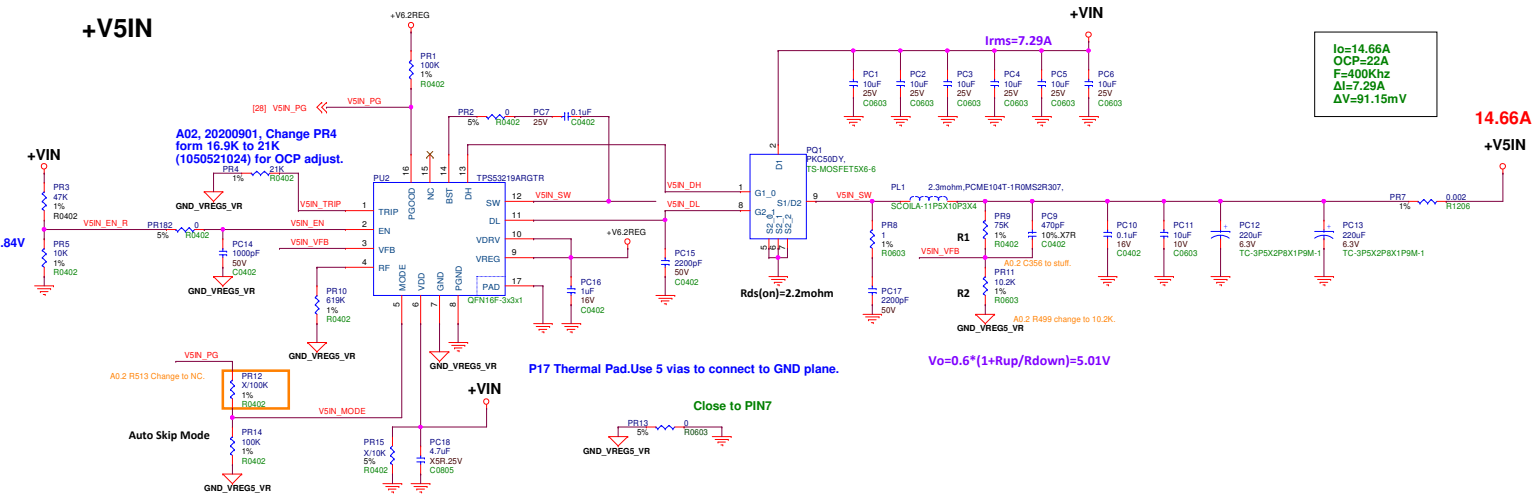


<Variant Name>

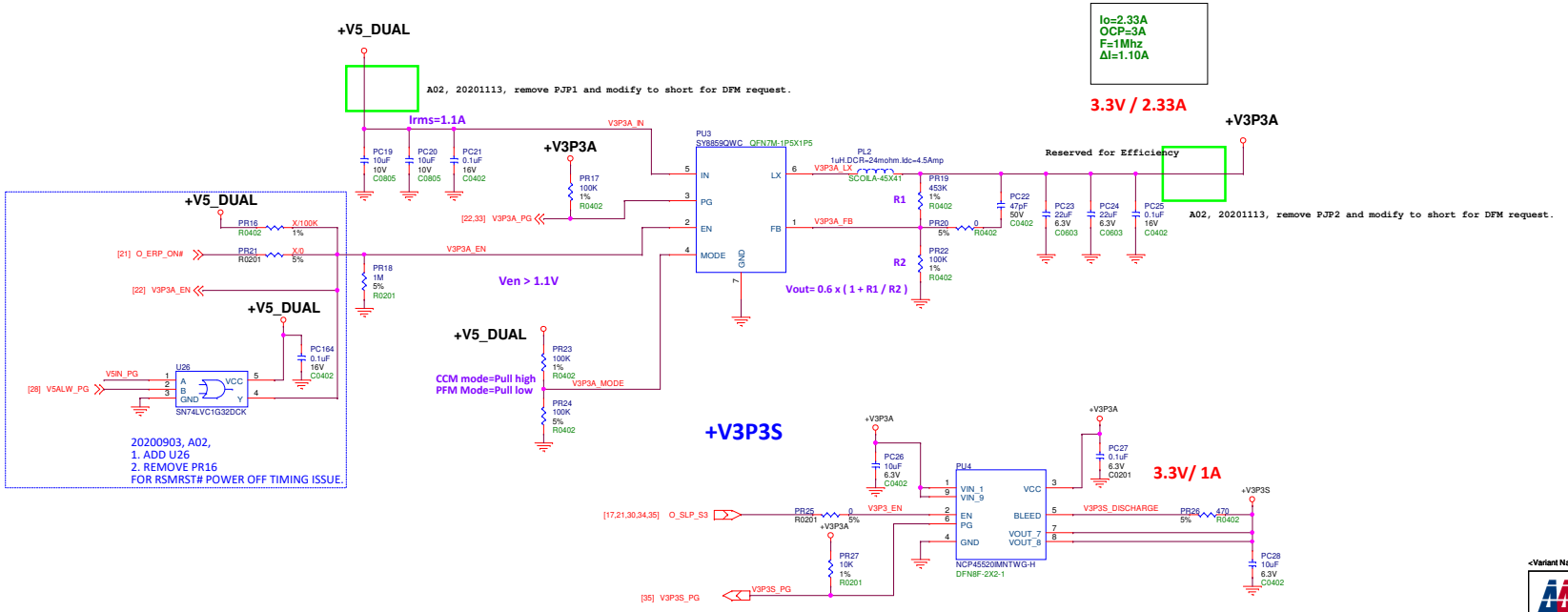
AAEON An ASUS Company

Title: +V5_Dual/ Discharge/ LED		
Size: A3	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet: 28 of 36	

+V5IN



+V3P3A

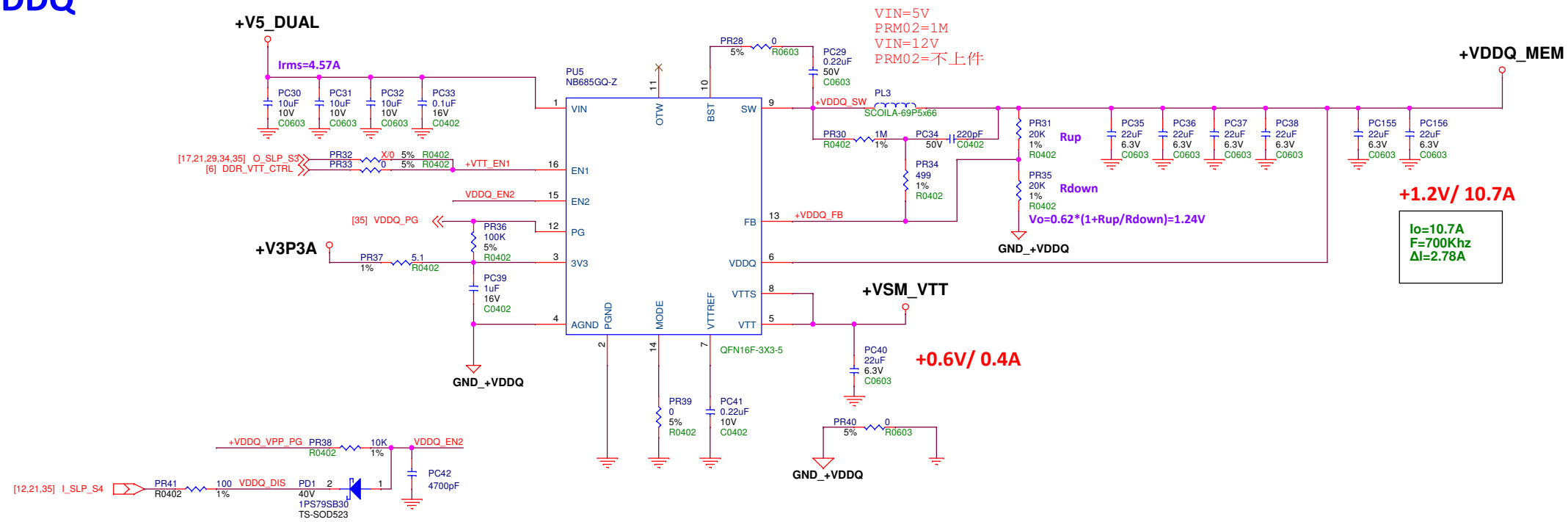


<Variant Name>

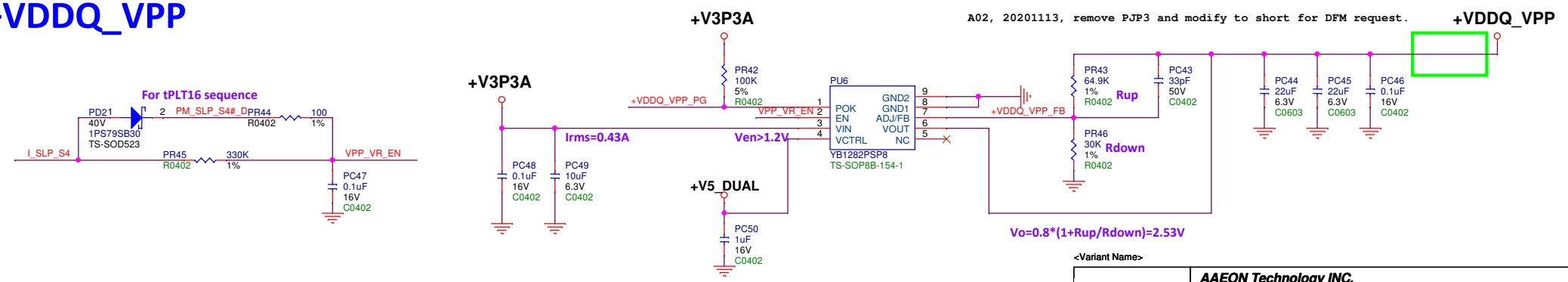
Title: POWER_+V5S_+V3P3A		
Size: A2	Document Number	Rev: A0.2_0_0
Date: Monday, November 23, 2020		Sheet: 29 of 36

AAEON An ASUS Company

+VDDQ



+VDDQ_VPP



<Variant Name>

AAEON Technology INC.

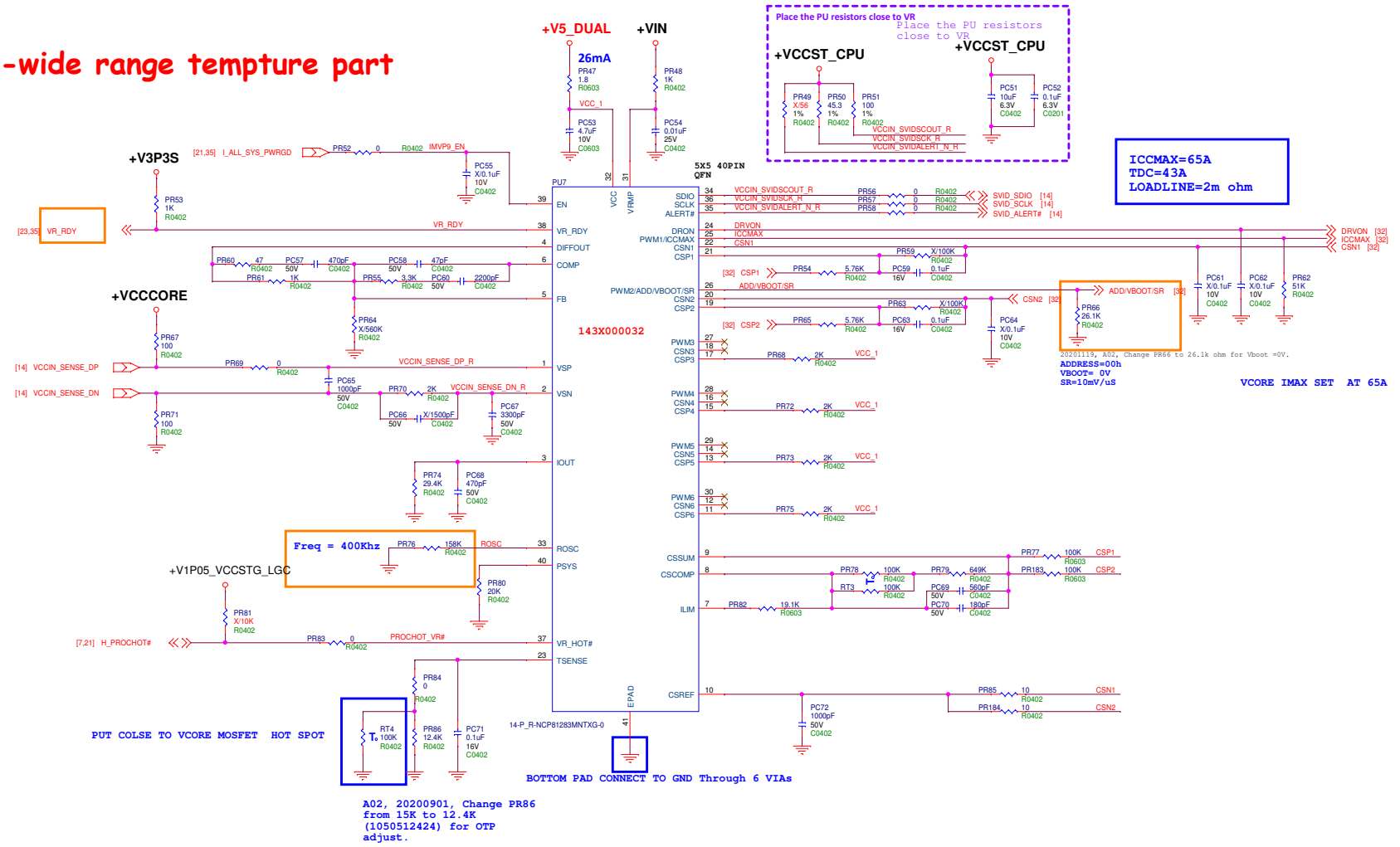
Title: PWR_+VDDQ/ +VDDQ_VPP/ +V1P8A

Size: Custom | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 30 of 36

Tiger Lake IMVP9

143X000032 is non-wide range tempture part

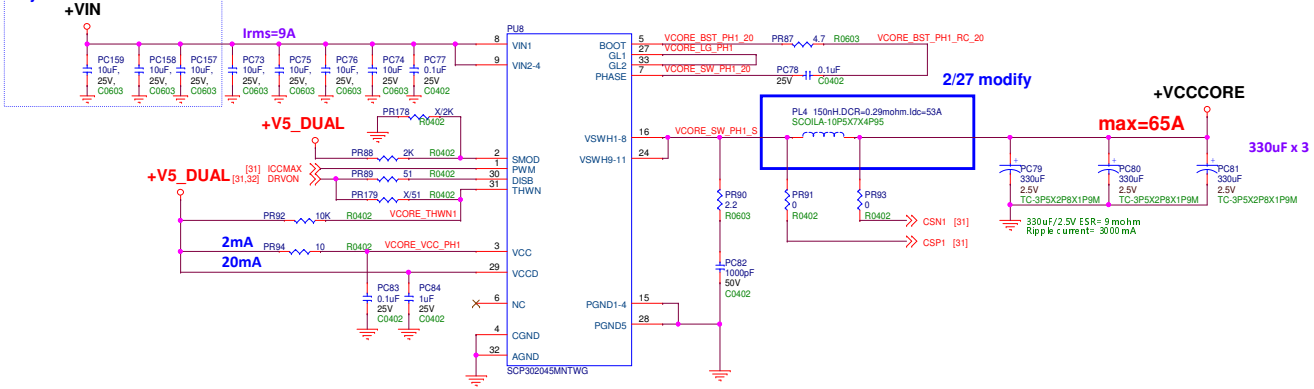


<Variant Name>

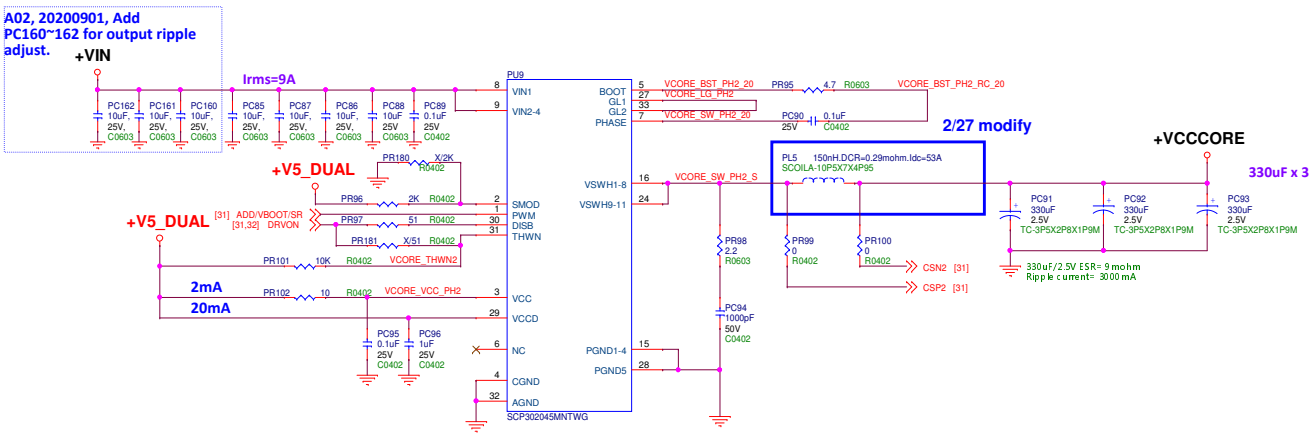
AAEON Technology INC.			
Title: PWR_IMVP9 Controller			
Size: C	Document Number: COM-TGUC6		Rev: A0.2_0_0
Date: Monday, November 23, 2020		Sheet 31 of 36	

+VCCIN

A02, 20200901, Add PC157~159 for output ripple adjust.



A02, 20200901, Add PC160~162 for output ripple adjust.

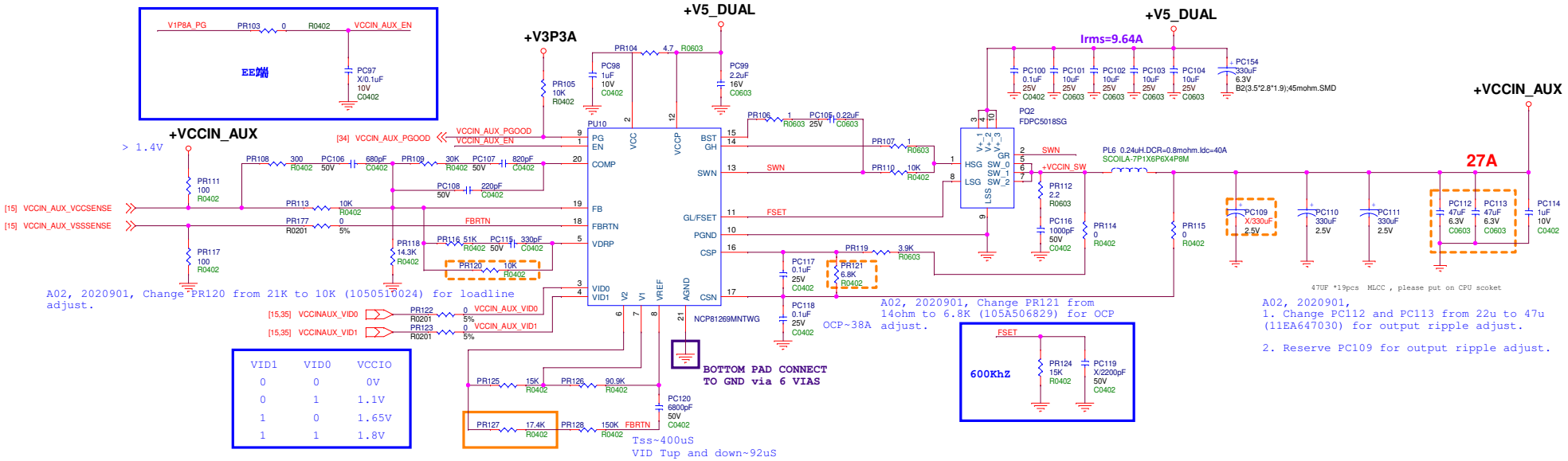


<Variant Name>

AAEON Technology INC.

Title	PWR_+VCCCORE	
Size: C	Document Number: COM-TGUC6	Rev: A0.2_0_0
Date: Monday, November 23, 2020	Sheet 32 of 36	

+VCCIN_AUX



VID1	VID0	VCCIO
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

A02, 2020901, Change PR120 from 21K to 10K (1050510024) for loadline adjust.

A02, 2020901, Change PR121 from 14ohm to 6.8K (105A506829) for OCP OCP~38A adjust.

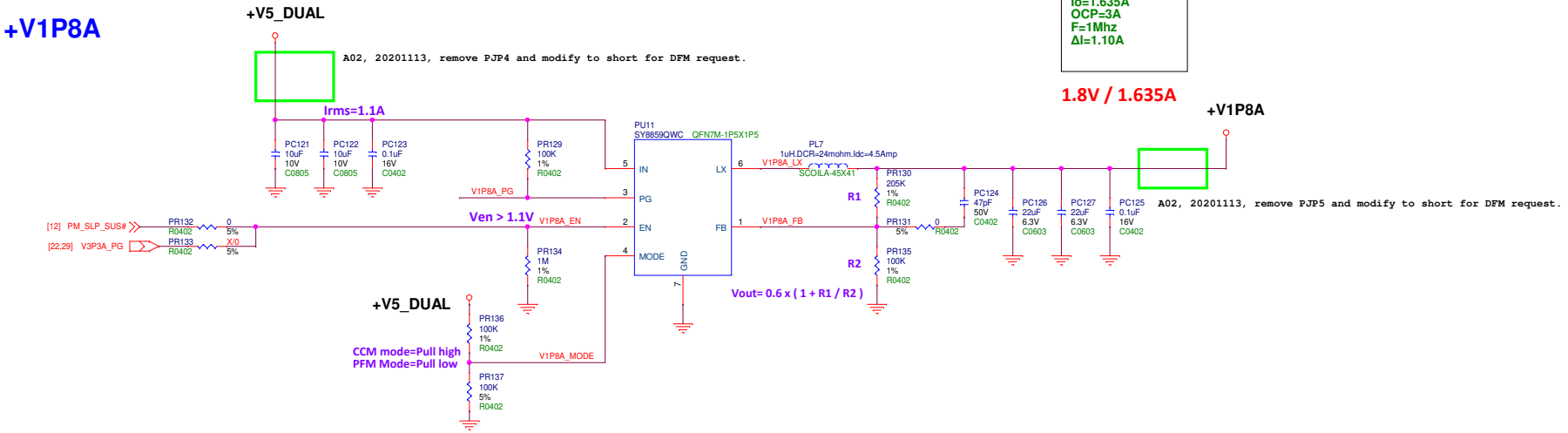
A02, 2020901,
1. Change PC112 and PC113 from 22u to 47u (11EA647030) for output ripple adjust.

2. Reserve PC109 for output ripple adjust.

BOTTOM PAD CONNECT TO GND via 6 VIAS

Tss~400uS
VID Tup and down~92uS

+V1P8A



<Variant Name>

AAEON Technology INC.

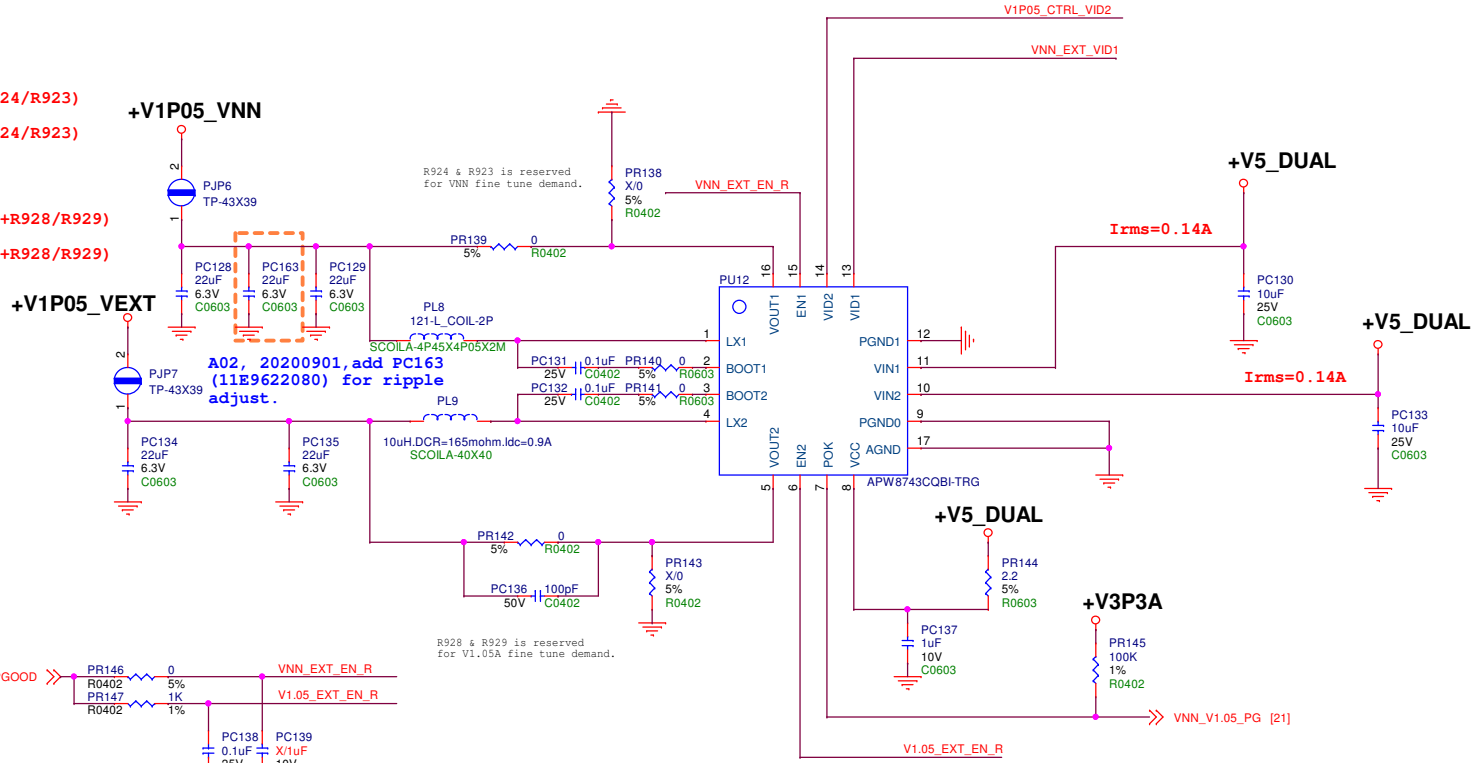
Title: PWR_+VCCIN_AUX/+V1P8A

Size: Custom | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 33 of 36

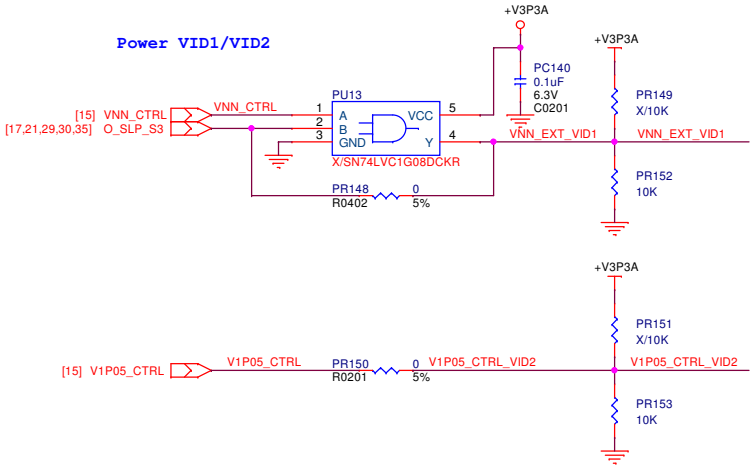
VID1 = 1,
VNN = 0.78V x (1+R924/R923)
VID1 = 0,
VNN = 1.05V x (1+R924/R923)
Imax=0.5A
FSW=500K

VID2 = 1,
V1.05A = 0.96V x (1+R928/R929)
VID2 = 0,
V1.05A = 1.05V x (1+R928/R929)
Imax=0.5A
FSW=500K



Power Enable

Power VID1/VID2



Part Number	VID=0(VNN)	VID=1(VNN)	VID=0(V1P05A)	VID=1(V1P05A)
APW8743CQBI(QBGI)	1.05V	0.78V	1.05V	0.96V
APW8743DQBI(QBGI)	0.78V	0.7V	1.05V	0.96V
APW8743EQBI(QBGI)	1.05V	0.7V	1.05V	0.96V

AAEON an ASUS assoc. co.

Title: PWR_+V1P05_VNN/+V1P05_VEXT

Size: A3 | Document Number | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet: 34 of 36

A02, 20201110, Reserve PR6 & PR155 for intel sighting #632245
CUZ:Due to improper initialization of logic on the VCCST
power domain in the Tiger Lake-UP3, the system may fail
to exit S3.
Workaround:Intel recommends a rework of the platform by
keeping the VCCST enabled during S3. Unmount PR6 & mount PR155.

+VCCST_CPU

+V5_DUAL

+VCCST_CPU@0.5A

VIN: 0.5V~13.5V

(12,21,30) I_SLP_S4 — PR29 R0201 X/0 5%
(17,21,29,30,34) O_SLP_S3 — PR154 R0201 0 5%
O_SLP_S3_S4_VCCST# → 3P3VCCST_OVERRIDE
PU1 SN74AUP1G32DRLR
PC8 0.1uF 6.3V C0201
PM_SLP_VCCST_OVRD
PR6 R0201 0 5% PM_SLP_VCCST_OVRD_R
PR155 X10K 1% R0201
VCCINAUX_PRESENT
PU15 SN74AUP1G32DRLR
PC143 0.1uF 6.3V C0201
VCCST_EN
PR158 R0201 10K 1%
VCCST_PG
+V1P05_OUT_FET
PC144 10uF 6.3V C0402
PU16 NCP45520IMNTWG-H DFN8F-2X2-1
VIN_1 VIN_9 VCC BLEED EN PG VOUT_7 VOUT_8 GND
PC142 0.1uF 6.3V C0201
VCCST_CPU_DISCHARGE
PR156 470 5% R0402
+VCCST_CPU

PR157 100K 5% R0201 3P3VCCST_OVERRIDE
PR159 100K 5% R0201
VCCST_OVERRIDE#
PQ3A EM6K7GT2R
PQ3B EM6K7GT2R
[12] VCCST_OVERRIDE_R
PR160 100K 5% R0201
VIH of VCCST_OVERRIDE_R is 1.5V

If VccST has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal Rdischarge <= VccST Rdischarge.

+VCCSTG_CPU

+V5_DUAL

+VCCSTG_CPU@ 0.3A

VIN: 0.5V~13.5V

[12] PM_SLP_S0# — PR161 R0201 X/0 5%
[12] CPU_C10_GATE# — PR162 R0201 0 5%
CPU_C10_GATE_R# → 3P3VCCST_OVERRIDE
PU17 SN74AUP1G32DRLR
PC145 0.1uF 6.3V C0201
VCCSTG_DIS
VCCINAUX_PRESENT
PU19 SN74AUP1G32DRLR
PC147 0.1uF 6.3V C0201
VCCSTG_EN
PR164 R0201 10K 1%
VCCSTG_PG
+V1P05_OUT_FET
PC148 10uF 6.3V C0402
PU18 NCP45520IMNTWG-H DFN8F-2X2-1
VIN_1 VIN_9 VCC BLEED EN PG VOUT_7 VOUT_8 GND
PC146 0.1uF 6.3V C0201
VCCSTG_CPU_DISCHARGE
PR163 300 1% R0402
+VCCSTG_CPU

+V1P8A
PU20 SN74AUP1G32DRLR
[15,33] VCCINAUX_VID0
[15,33] VCCINAUX_VID1
PC149 0.1uF 6.3V C0201
VCCINAUX_PRESENT_1P8
PU24 74AUP1G07GW
PC153 0.1uF 6.3V C0201
PR168 1K 1% R0402
VCCINAUX_PRESENT

VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal Rdischarge <= 300 Ohms to GND.

[30] VDDQ_PG
[29] V3P3S_PG
VCCST_PG
PU21 NC7SZ11P6X
PC150 0.1uF 6.3V C0201
I_ALL_SYS_PWRGD → I_ALL_SYS_PWRGD [21,31]

PU22 74AUP1G07GW
PC151 0.1uF 6.3V C0201
PR165 1K 1% R0402
H_VCCST_PWRGD [12]

[23,31] VR_RDY — PR166 R0201 0 5%
IMVP9_VR_READY
PC56 X/0.1uF 10V C0402
PU23 SN74LVC1G08DCKR
PC152 0.1uF 6.3V C0201
PR167 10K 1% R0201
PCH_PWROK [12]

Reserve PC56 for softstart

<Variant Name>

AAEON® An ASUS Company

AAEON Technology INC.

Title: PWR_+VCCST_CPU/+VCCSTG_CPU

Size | Document Number: COM-TGUC6 | Rev: A0.2_0_0

Date: Monday, November 23, 2020 | Sheet 35 of 36

COM-TGUC6 Revision History

COM-TGUC6 A0.2_0_0 PCB: 1907TGLU01 BOM: 9697TGLU01 Date: 2020/11/19

01. Project code: E191211
02. Model name: COM-TGUC6
03. Model revision: A0.2_0_0
04. 96-Level: 9697TGLU01
05. PCB 料號: 1907TGLU01
06. PCB 厚度: 2.0 mm
07. PCB 層數: 14 Layer
08. 連板數量: 2 pcs

Revision History Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.	Bug ID
1	5	DDI AUX SW	09/24	HW	Downsize Swith IC for Saving PCB space	Change P/N of U3 from 145S312500 to 1420USB300.	A02	
2	6	PWR sequence	09/21	HW	Mismatch PWR sequence	Due to cap. of IC, change value of R41 from 100k to 1k to meet power sequence.	A02	
3	7	1.No use fucntion 2.Hang code 5D in AT mode	09/22	HW	1.The eSPI ALERT# is including in eSPI IO pin and CPU don't have eSPI ALERT# pin. 2.AT ON/OFF test issue (hang 5d).	Remove BDG_ESPI_ALT_3P3# level-shift (R107, Q6, R106). The eSPI_IO1 presents the ALERT# state while the eSPI bus is idle by datasheet. And resolve AT problem.	A02	
4	7	Change to SPI TPM	09/30	HW	Change TPM IC from LPC to SPI, cuz Tiger Lake don't support LPC TPM. Adjust SPI circuit for supporting two SPI device.	Add SPI0_TPM_CS2#. Change serie R568 / R569 / R570 to 5.1ohm for SPI0_CLK / SPI0_SO / SPI0_SI.	A02	
5	7	Change Level-shifter	09/21	HW	CUZ the VIH (1.05V) of NMOS is too margin, change IC to aviod it.	Change U8 level shifter to 145901G070.	A02	
6	7	LAN I2C	11/06	HW	Change R value for Intel I225.	Change R46 / R47 from 1k to 499 to meet I225 checklist.	A02	
7	8	Debug	07/17	HW	Reserve UART test point for Debugging BIOS.	Add TP30~TP33 for BIOS request.	A02	
8	8	Save PCB space	11/05	HW	Remove parts to save PCB space	The nets of CPU1.DJ29 & CPU1.DJ31 (I2C fuction for 80 port) for the PCB spacing of EEPROM of Intel I225.	A02	
9	9	USB OC# pin	09/24	HW	Change design for USB OC# pin for multi-OC# pin.	Add D17~D20 & change OC NETdesign for USB OC PIN OUT issue	A02	
10	9	Change placement	11/06	HW	I225 checklist mentioned TX cap need to close to CPU.	Change C11/C12 placement for I225.	A02	
11	10	Change X'TAL	0911	HW	After vendor mesurement result, change X'TAL & cap,	1. Change P/N of Y1 from 1231327631 to 1231327632 by test result. 2. Change P/N of Y2 from 1231038450 to 1231038451 by test result. 3. Change value of C18/C19 from 15pF to 10pF by test result.	A02	
12	12	LAN Wake pin	1106	HW	Pull up 10kohm based on I225 CRB.	Mount R162 for I225.	A02	
13	17	SPI serie R	1105	HW	Adjust SPI circuit for supporting two SPI device.	Due to PCB space, change R231/R236/R233 from 33 to 51ohm. Otherwise, Intel PDG suggest 56ohm.	A02	
14	31	Vboot	1119	HW	Choose correct Vboot value	Change PR66 to 26.1k ohm for Vboot =0V.	A02	
15	20	LAN I225	1106	HW	Due to PM modifying spec. change LAN form I219 to I225.	Add U29 w/ Peripheral Circuitry. ADD Q20 CIRCUIT FOR LAN LED LEAKAGE ISSUE	A02	
16	21	Multi-change for saving PCB space	1111	HW	Change parts to save PCB space for I225.	1. Change AT/ATX SW to R603 & R604. 2. Remove Q10 & Q9 & R381 & R382 & JECSPI1. 3. Change U12 to small package. PN:145901G070 4. Change R341 & R364 to 0201 package.	A02	
17	23	1.SPI serie R 2.Spacing PCB space	1105	HW	1.Adjust SPI circuit for supporting two SPI device. 2. Modify parts to save PCB space.	1. Add R564~R566 and choose 56ohm for 2 SPI device. Change R400~R404 and R405~R407 to 0ohm refering to PICO-TGU & PDG. 2. Remove JLPC1 circuit (80 port conn.) for the PCB spacing of EEPROM of Intel I225.	A02	
18	24	LVDS CTRL Signals	0922	HW	Modify the circuit of LVDS back light control and EDP_VDD_EN for eDP and LVDS.	1. add R548 and connect the net of EDP_BKLT_CTRL to U18.12 for LVDS back light control. 2. Change U25 from 142LV32571 to 1420USB300 for IC downsizing. 3. Add EDP_VDD_EN, EDP_BKLT_CTRL and EDP_VDD_EN by BIOS request for eDP2 black light control. 4. Add Q19 to disable LVDS and pull HPD of DDIA to Low, when EDP_HPD PULL HIGH. 5. Add OR GATE U27 to enable LVDS/EDP VDD_EN/	A02	
19	25	X'TAL modification	1007	HW	After vendor mesurement result, change cap and add R,	1. Change value of C327/C326 from 20pF to 12pF and add R571 for FAE suggestion. 2. After confirm with Jake, change R571 from 1.8k ohm(0402) to R54 1k (0201).	A02	
20	26	SPI TPM	1105	HW	Change TPM IC from LPC to SPI, cuz Tiger Lake don't support LPC TPM.	change TPM U21 From SLB9665T to NPCT750 for TGL doesn't support LPC TPM.	A02	
21	27	ECE1200	1105	HW	Debug eSPi to LPC IC and add solution.	1. Connecting BDG_SUSWARN# and BDG_SUSACK# with R497 for boot up issue by FAE request. 2. ADD R567 fro PU ESPI ALT. The eSPI_IO1 presents the ALERT# state while the eSPI bus is idle. 3. Remove R487 which connect to JLPC1 for the PCB spacing of EEPROM of Intel I225.	A02	
22	28	PWR	0904	HW	Derating issue and PWR sequence solution.	1. Change value of C357 from 47uF/6.3V to 22uF/10V for Derating issue. 2. ADD VSALW_PG AND R550 FOR RSMRST# POWER OFF TIMING ISSUE.	A02	
23	29	PWR	0901	HW	Adjust OCP value.	Change PR4 form 16.9K to 21K (1050521024) for adjusting OCP.	A02	
24	28	PWR	0904	HW	PWR sequence solution for RSMRST# POWER OFF.	1. ADD U26 2. REMOVE PR16 FOR RSMRST# POWER OFF TIMING ISSUE.	A02	
25	29 & 30 & 33	Shor pad	0904	HW	Remove short pad for PE suggestion.	Remove PJP1 / PJP2 / PJP3 / PJP4 / PJP5 and modify to short for DFM request.	A02	
26	31	PWR	0901	HW	Adjust OTP value.	Change PR86 from 15K to 12.4K (1050512424) for adjusting OTP.	A02	
27	32	PWR	0901	HW	Add caps after fine tuning output ripple.	1. Add PC157~159 for output ripple. 2. Add PC160~162 for output ripple.	A02	
28	33	PWR	0901	HW	Change R after fine tuning loadline and OCP value.	1. Change PR120 from 21K to 10K (1050510024) for loadline. 2. Change PR121 from 14ohm to 6.8K (105A506829) for OCP. 3. Change PC112 and PC113 from 22u to 47uF (11EA647030) for output ripple. 4. Reserve PC109 for output ripple.	A02	
29	34	PWR	0901	HW	Add caps after fine tuning output ripple.	Add PC163 (11E9622080) for ripple.	A02	
30	35	Sighting report #632245	0901	HW	Due to improper initialization of logic on the VCCST power domain in the Tiger Lake-UP3, the system may fail to exit S3.	Add PR6 & PR155 for Workaround.	A02	

<Variant Name>

AAEON Technology INC.

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Date: Monday, November 23, 2020 Sheet 36 of 36