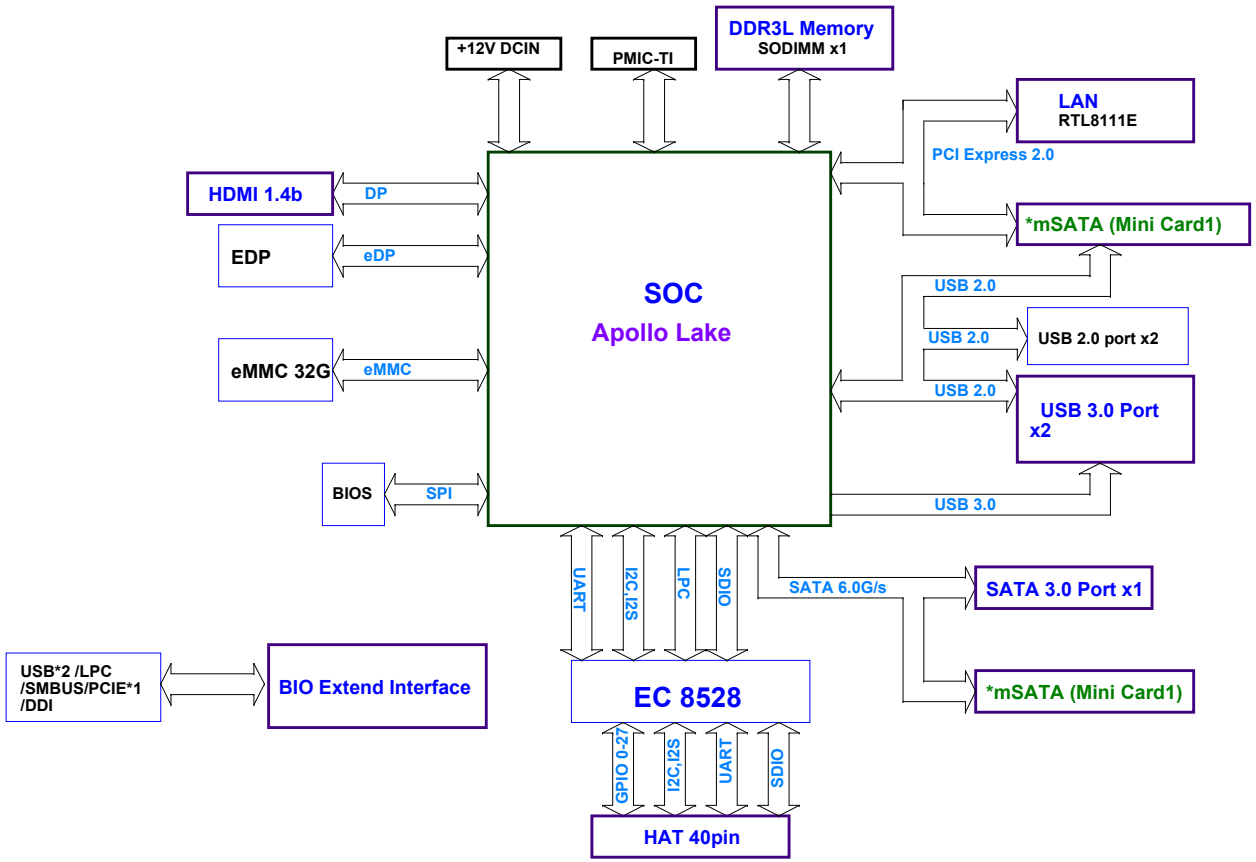
PICO-APL2 Rev.A0.1_0_0

Apollo Lake SoC Platform Cross Compatibility



Project Number : E16XXXX

Production Line : Sub.EPI.AA2M

<Core Design>

Title: Cover Sheet			
Size: C	Document Number: PICOAPL2A01		Rev: A0.1_0_0
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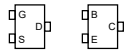
SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_0	1.8V	20K PD/I	
GPIO_1	1.8V	20K PD/I	
GPIO_2	1.8V	20K PD/I	
GPIO_3	1.8V	20K PD/I	
GPIO_4	1.8V	20K PD/I	LVDS_RBIT0
GPIO_5	1.8V	20K PD/I	LVDS_RBIT1
GPIO_6	1.8V	20K PD/I	LVDS_RBIT2
GPIO_7	1.8V	20K PD/I	LVDS_RBIT3
GPIO_8	1.8V	20K PD/I	
GPIO_9	1.8V	20K PD/I	
GPIO_10	1.8V	20K PD/I	
GPIO_11	1.8V	20K PD/I	
GPIO_12	1.8V	20K PD/I	
GPIO_13	1.8V	20K PD/I	GPIO_PME#
GPIO_14	1.8V	20K PD/I	WAKE_RI#
GPIO_15	1.8V	20K PD/I	EN_USB
GPIO_16	1.8V	20K PD/I	LAN1_DISABLE#
GPIO_17	1.8V	20K PD/I	W_DISABLE0#
GPIO_18	1.8V	20K PD/I	W_DISABLE1#
GPIO_19	1.8V	20K PD/I	
GPIO_20	1.8V	20K PD/I	
GPIO_21	1.8V	20K PD/I	
GPIO_22	1.8V	20K PD/I	SATA_GP[0]
GPIO_23	1.8V	20K PD/I	SATA_GP[1]
GPIO_24	1.8V	20K PD/I	SATA_DEVSLP[0]
GPIO_25	1.8V	20K PD/I	SATA_DEVSLP[1]
GPIO_26	1.8V	20K PD/I/OP	SATA_LED_N
GPIO_27	1.8V	20K PD/I	
GPIO_28	1.8V	20K PD/I	
GPIO_29	1.8V	20K PD/I	
GPIO_30	1.8V	20K PD/I	
GPIO_31	1.8V	20K PD/I	
GPIO_32	1.8V	20K PD/I	
GPIO_33	1.8V	20K PD/I	PMIC_IRQ
GPIO_216	1.8V	20K PD/IO	
GPIO_217	1.8V	20K PD/IO	
GPIO_218	1.8V	20K PD/IO	
GPIO_219	1.8V	20K PD/IO/OP	

PCB Footprints



SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
LCD Backlight Contoller	5Ch
GPIO IC	6Eh
PTN3460 Slave	C0h

PCB STACK :

Impedence 50ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : GND
- Layer 5 : Signal
- Layer 6 : VCC
- Layer 7 : Signal
- Layer 4 : Signal
- Layer 9 : GND
- Layer 10 : Solder

<Core Design>

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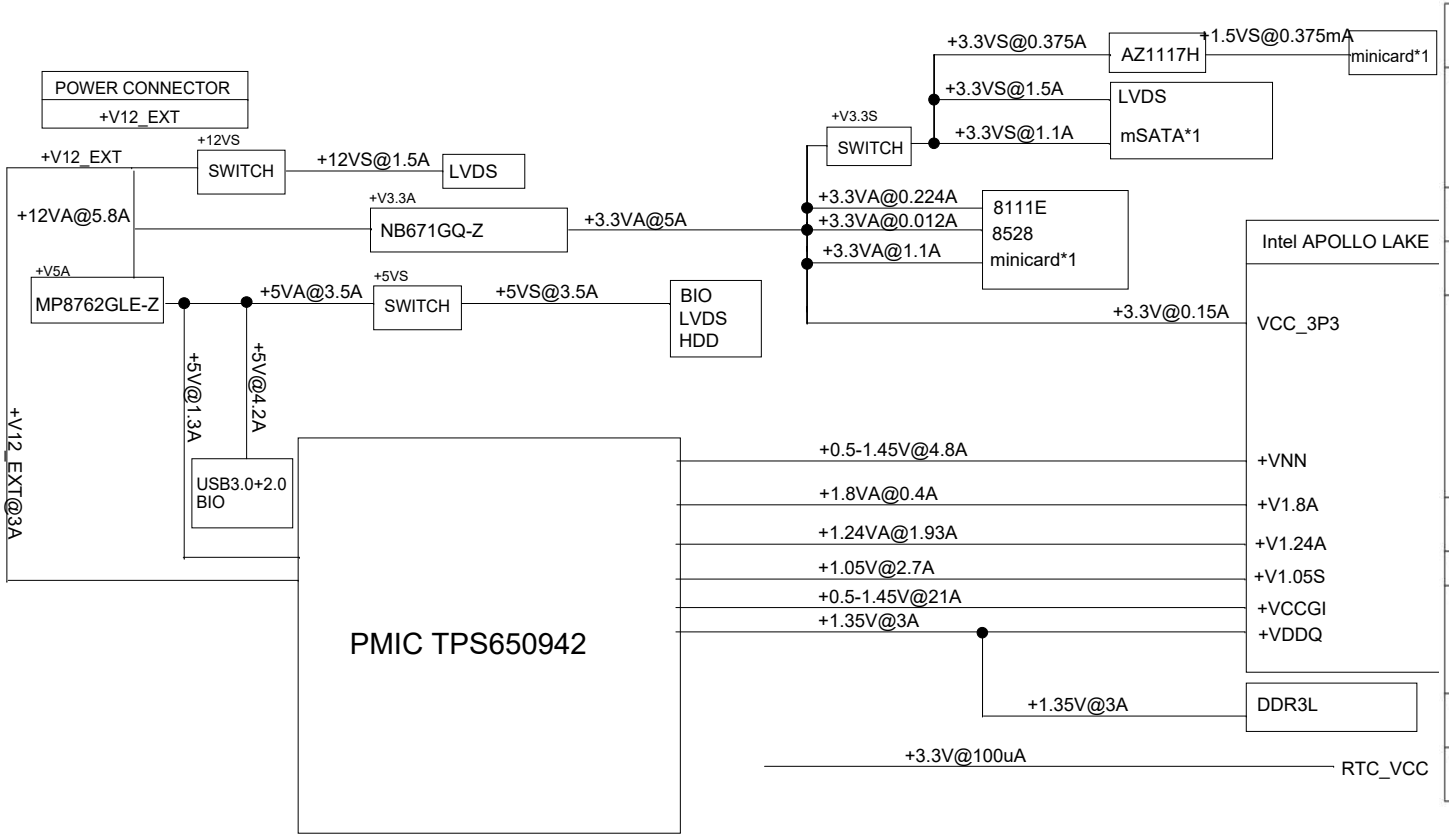
Title: **System Settings**

Size	Document Number	Rev:
B	PICOAPL2A01	A0.1_0_0

Date: *Tuesday, December 20, 2016* Sheet: **2** of **32**



Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Iccmax (A)
VCC_VCGI	0.45~1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	21
VNN	0.45~1.3	+/-50mV	4.8
VCC_V1P05	1.05	+/-5%	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	1.3
VCC_V1P24_A	1.24	+/-5%	TBD
VCC_V1P8V_A	1.8	+/-5%	0.4
VDDQ	1.35	+/-5%	2.8 (excluding DRAM)
	1.24	+/-5%	
VCC_3P3V_A	3.3	+/-5%	0.15
VCC_RTC_3P3V	2~3.47	N/A	TBD

+V5A -> +V3.3A -> +VNN -> +VCC -> +V1P8A- > +V1P24A -> +V1P8U -> +VDDQ
+V1.05S -> +VCC_VCGI

<Core Design>

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Title: Power Tree

Size: Custom | Document Number: PICOAPL2A01 | Rev: A0.1_0_0

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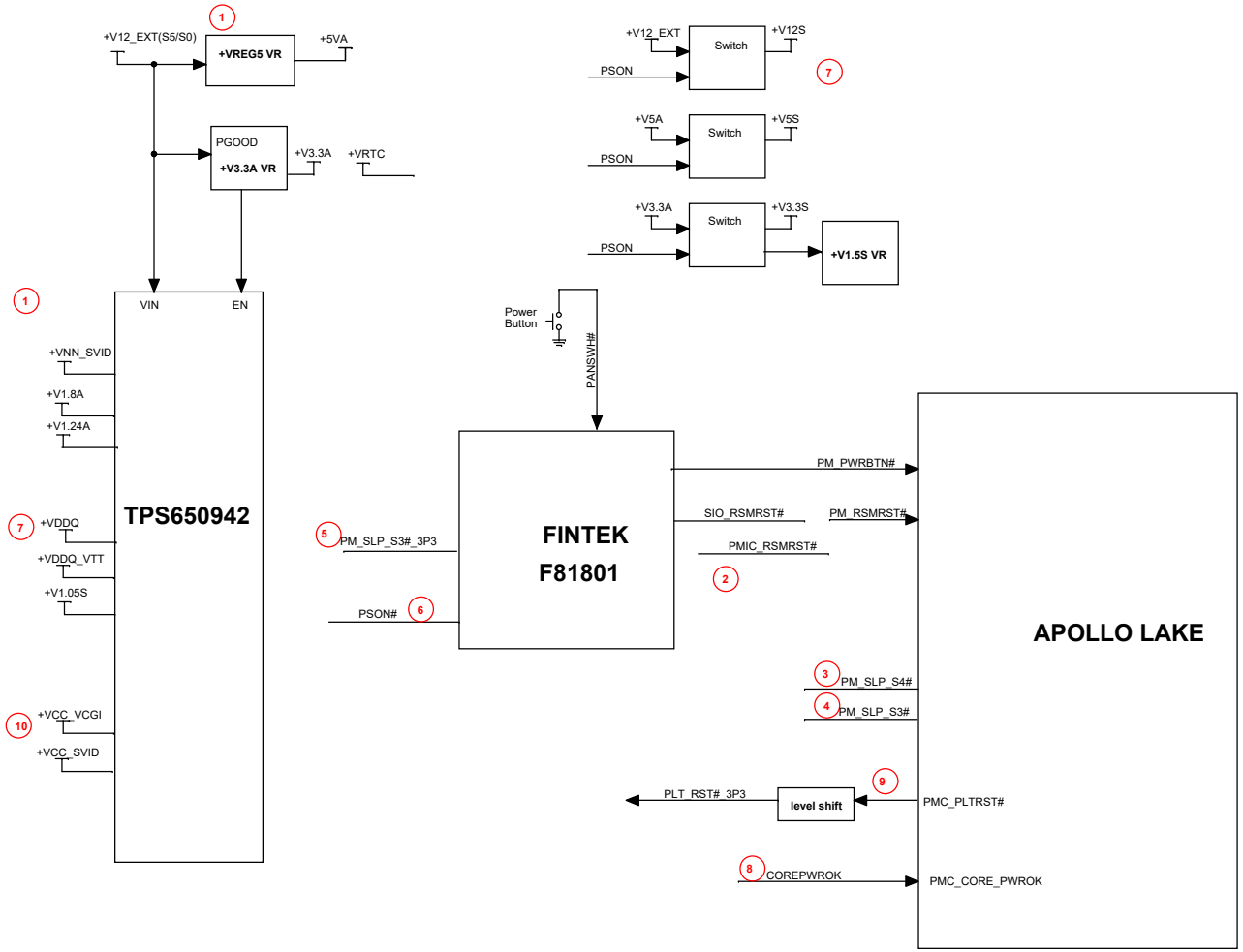
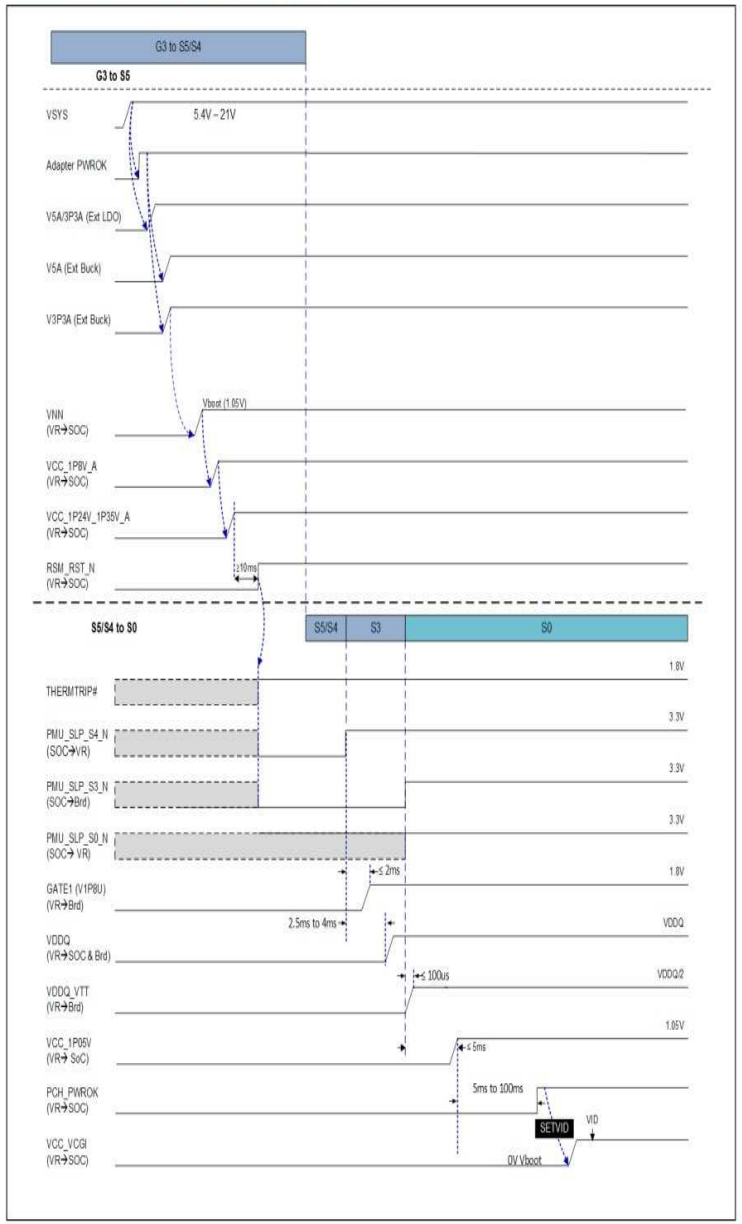


Power-Up Sequencing (G3 to S0)—Adapter



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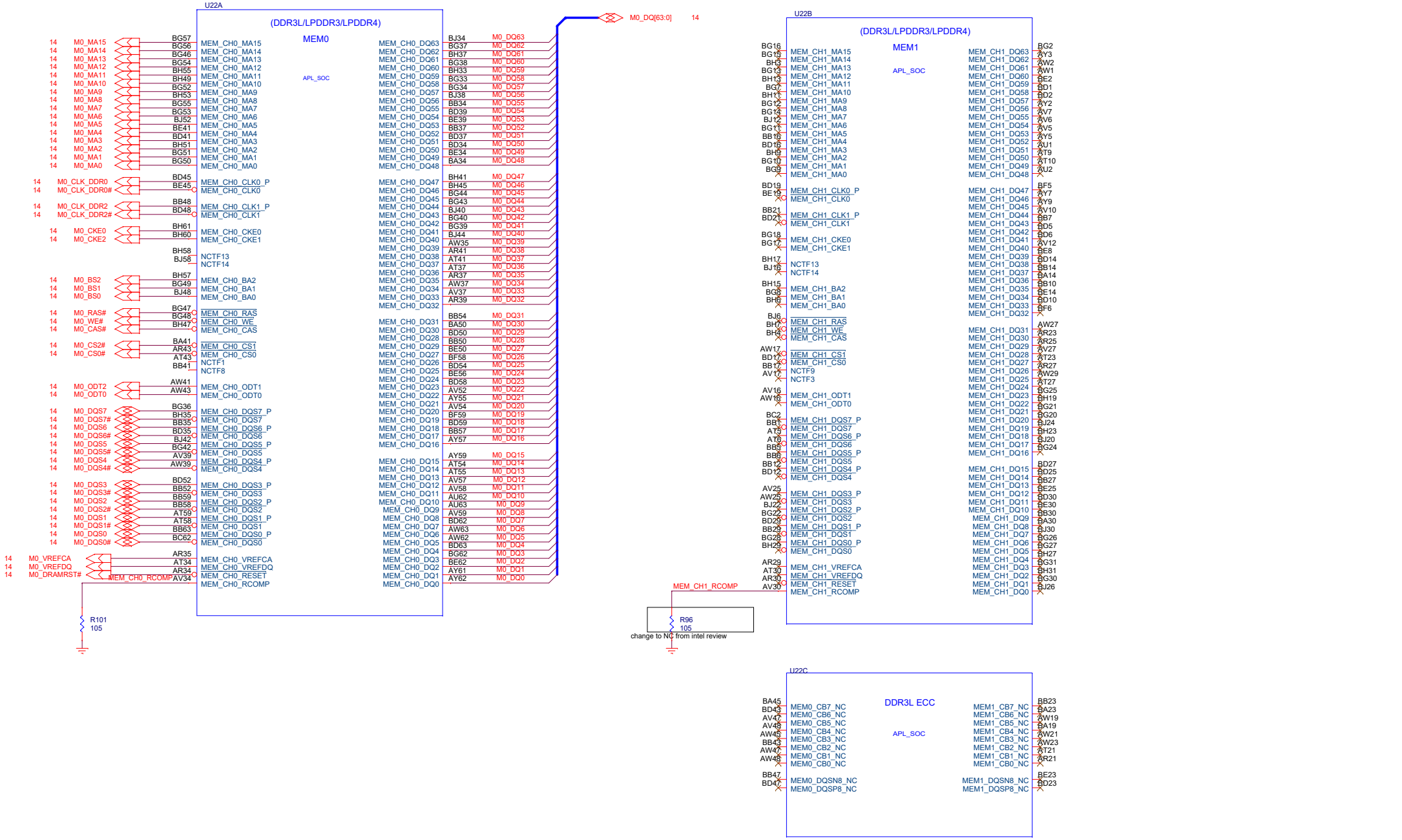
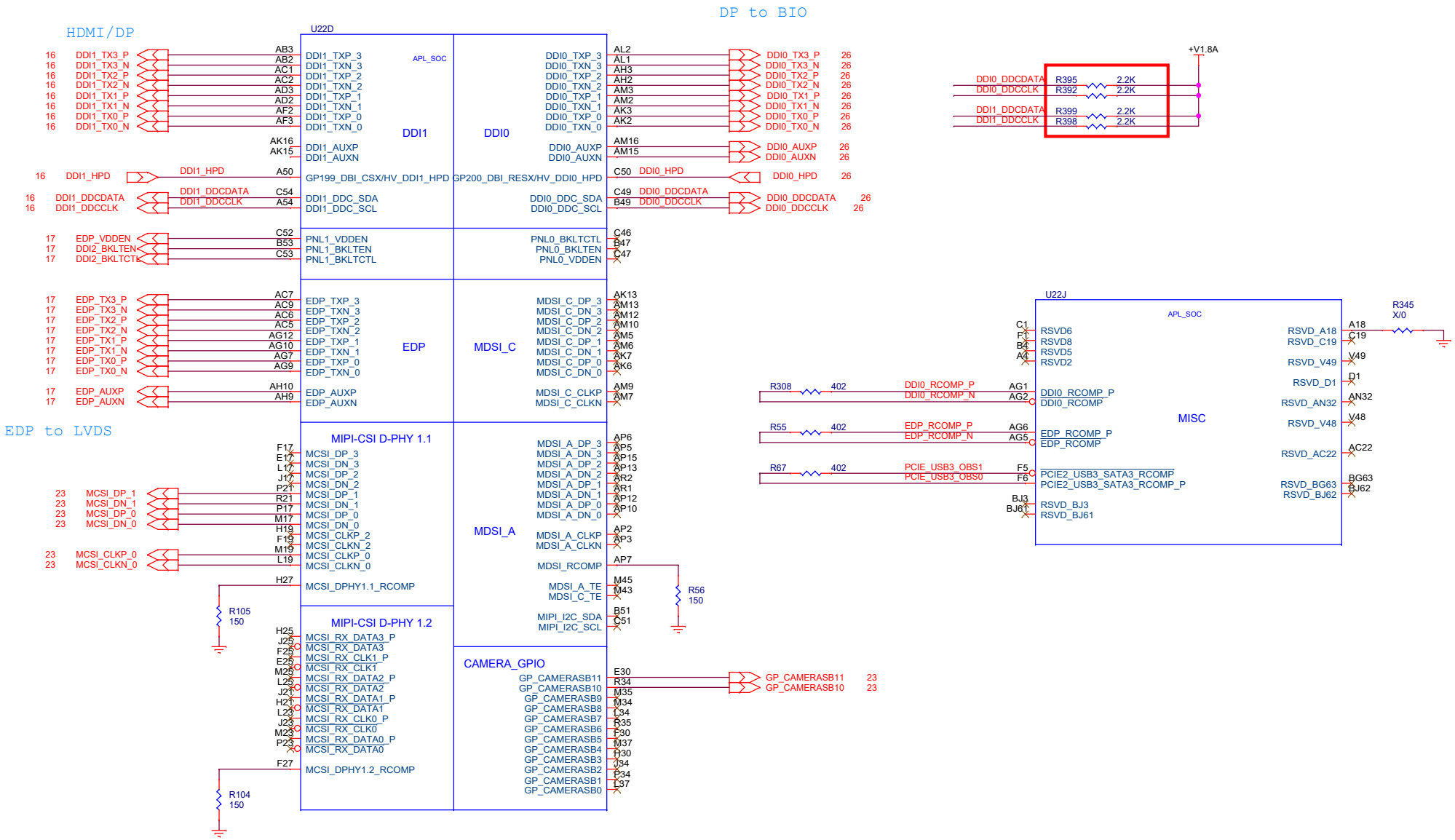
Title: Power Sequence		
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
Date: Tuesday, December 20, 2016		Sheet: 4 of 32


U22A
(DDR3L/LPDDR3/LPDDR4)
MEM0
APL_SOC
M0_DQ[63:0]
14
U22B
(DDR3L/LPDDR3/LPDDR4)
MEM1
APL_SOC
MEM_CH1_RCOMP
R96
105
change to NC from intel review
R101
105
U22C
DDR3L ECC
APL_SOC



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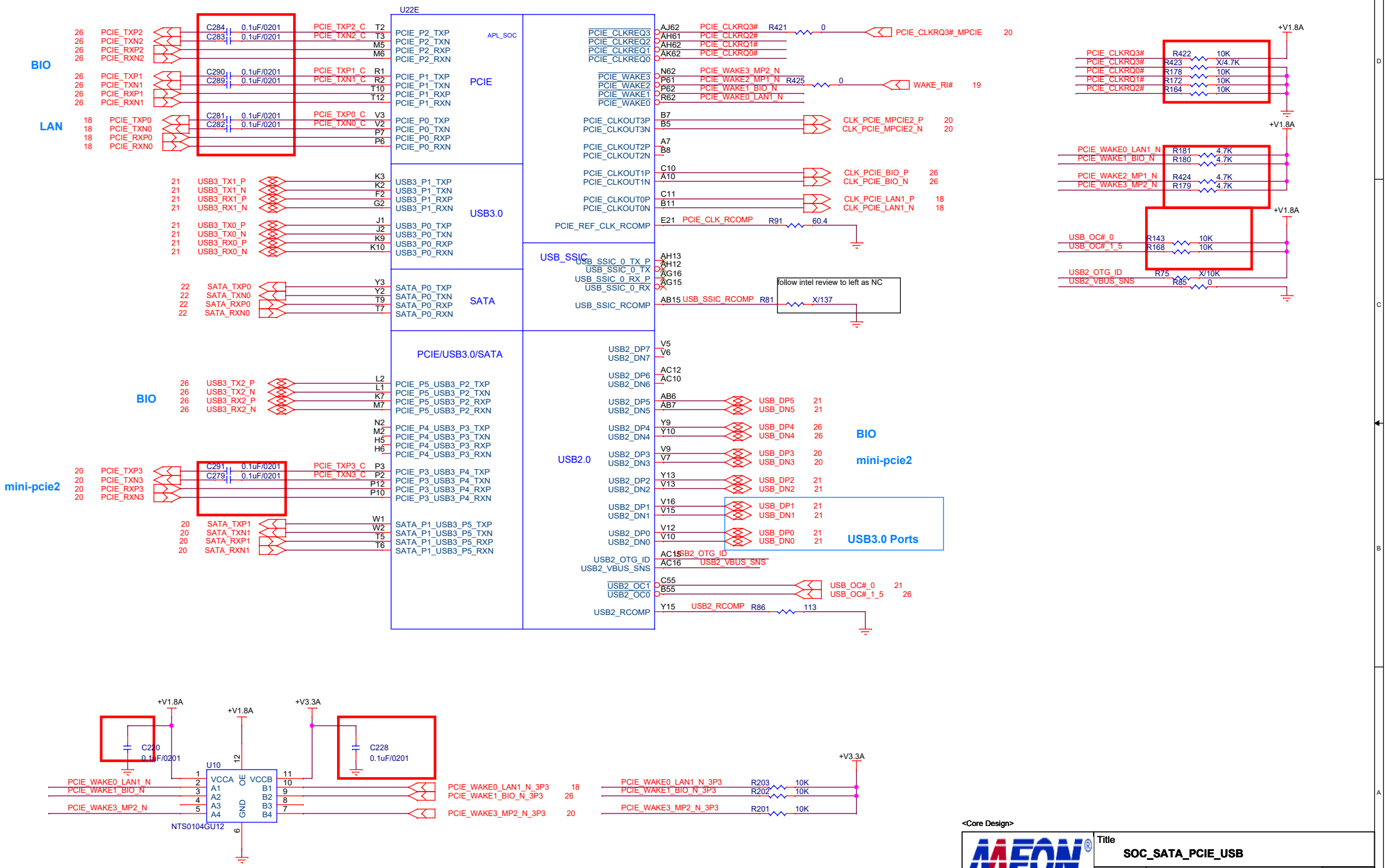
Title: SOC_DISPLAY		
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
Date: Tuesday, December 20, 2016	Sheet: 6 of 32	



Title	SOC_SATA_PCIE_USB
Size	Custom
Document Number	PICOAPL2A01
Rev:	A0.1_0_0
Date:	Tuesday, December 20, 2016
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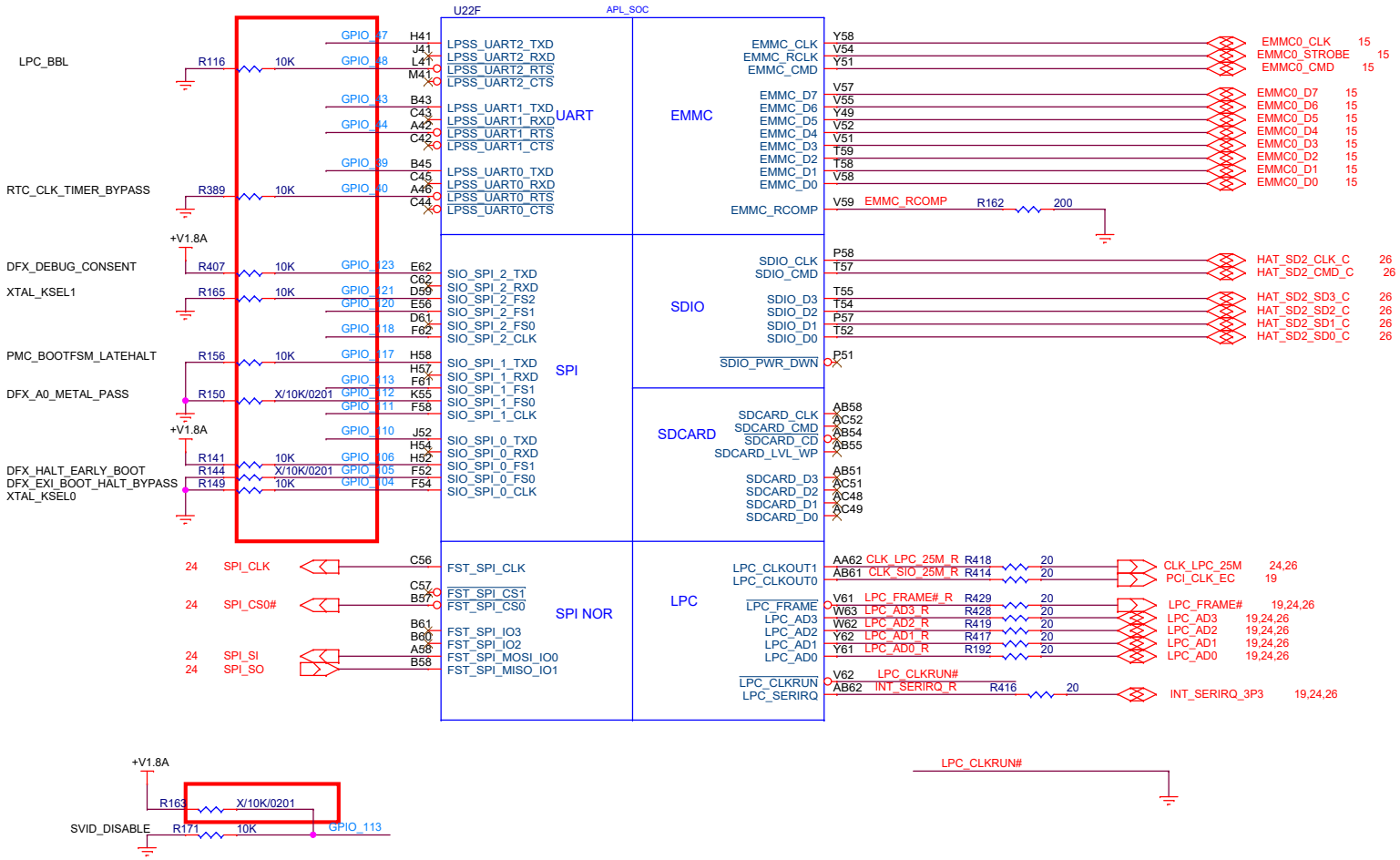
an ASUS assoc. co.



Enable CSE ROM Bypass	
GPIO_39	CSE ROM Bypass
0	Disable bypass (default)
1	Enable Bypass

Allow eMMC as a boot source	
GPIO_43	eMMC as a boot
0	Disable
1	Enable (default)

Allow SPI as a boot source	
GPIO_44	SPI as a boot
0	Disable
1	Enable (default)

Force DNX FW Load	
GPIO_47	DNX FW Load
0	Do not force (default)
1	Enable

LPC 1.8V/3.3V Mode Select	
GPIO_110	LPC Voltage
0	3.3V mode
1	1.8V mode (default)

Boot BIOS Strap (BBS)	
GPIO_111	
0	Boot from SPI
1	Do not boot from SPI (default)

Flash Descriptor Override	
GPIO_118	
0	No Override (Normal Operation)
1	Override

Top swap override	
GPIO_120	
0	Disable (default)
1	Override

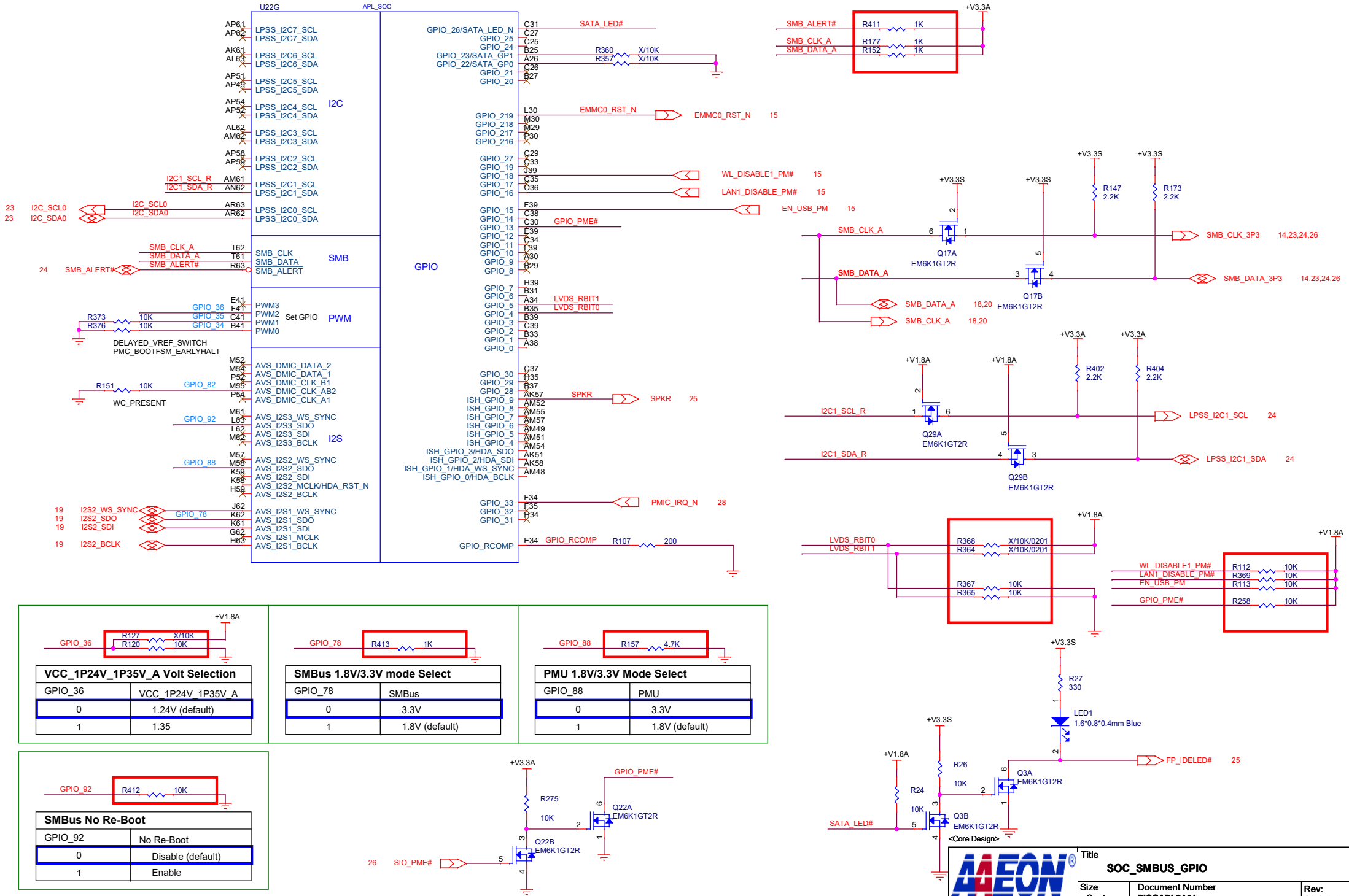
<Core Design>

AAEON an ASUS assoc. co.

Title: SOC_LPC_SPI_EMMC_SD

Size: Custom | Document Number: PICOAPL2A01 | Rev: A0.1_0_0

Date: Tuesday, December 20, 2016 | Sheet: 8 of 32


U22G
APL_SOC
I2C
SMB
PWM
I2S
GPIO
LPSS_I2C7_SCL
LPSS_I2C7_SDA
LPSS_I2C6_SCL
LPSS_I2C6_SDA
LPSS_I2C5_SCL
LPSS_I2C5_SDA
LPSS_I2C4_SCL
LPSS_I2C4_SDA
LPSS_I2C3_SCL
LPSS_I2C3_SDA
LPSS_I2C2_SCL
LPSS_I2C2_SDA
LPSS_I2C1_SCL
LPSS_I2C1_SDA
LPSS_I2C0_SCL
LPSS_I2C0_SDA
I2C1_SCL_R
I2C1_SDA_R
I2C_SCL0
I2C_SDA0
SMB_CLK
SMB_DATA
SMB_ALERT
SMB_CLK_A
SMB_DATA_A
SMB_ALERT#
PWM3
PWM2
PWM1
PWM0
Set GPIO
GPIO_36
GPIO_35
GPIO_34
R373
R376
10K
DELAYED_VREF_SWITCH
PMC_BOOTFSM_EARLYHALT
R151
GPIO_82
WC_PRESENT
AVS_DMIC_DATA_2
AVS_DMIC_DATA_1
AVS_DMIC_CLK_B1
AVS_DMIC_CLK_AB2
AVS_DMIC_CLK_A1
GPIO_92
AVS_I2S3_WS_SYNC
AVS_I2S3_SDO
AVS_I2S3_SDI
AVS_I2S3_BCLK
GPIO_88
AVS_I2S2_WS_SYNC
AVS_I2S2_SDO
AVS_I2S2_SDI
AVS_I2S2_MCLK/HDA_RST_N
AVS_I2S2_BCLK
I2S2_WS_SYNC
I2S2_SDO
I2S2_SDI
I2S2_BCLK
GPIO_78
AVS_I2S1_WS_SYNC
AVS_I2S1_SDO
AVS_I2S1_SDI
AVS_I2S1_MCLK
AVS_I2S1_BCLK
GPIO_26/SATA_LED_N
GPIO_25
GPIO_24
GPIO_23/SATA_GP1
GPIO_22/SATA_GP0
GPIO_21
GPIO_20
SATA_LED#
R360
R357
X/10K
GPIO_219
GPIO_218
GPIO_217
GPIO_216
EMMC0_RST_N
GPIO_27
GPIO_19
GPIO_18
GPIO_17
GPIO_16
WL_DISABLE1_PM#
LAN1_DISABLE_PM#
GPIO_15
GPIO_14
GPIO_13
GPIO_12
GPIO_11
GPIO_10
GPIO_9
GPIO_8
EN_USB_PM
GPIO_PME#
GPIO_7
GPIO_6
GPIO_5
GPIO_4
GPIO_3
GPIO_2
GPIO_1
GPIO_0
LVDS_RBIT1
LVDS_RBIT0
GPIO_30
GPIO_29
GPIO_28
SPKR
ISH_GPIO_9
ISH_GPIO_8
ISH_GPIO_7
ISH_GPIO_6
ISH_GPIO_5
ISH_GPIO_4
ISH_GPIO_3/HDA_SDO
ISH_GPIO_2/HDA_SDI
ISH_GPIO_1/HDA_WS_SYNC
ISH_GPIO_0/HDA_BCLK
GPIO_33
GPIO_32
GPIO_31
PMIC_IRQ_N
GPIO_RCOMP
R107
200
R411
R177
R152
1K
+V3.3A
+V3.3S
+V1.8A
R147
R173
2.2K
Q17A
Q17B
EM6K1GT2R
R402
R404
Q29A
Q29B
LPSS_I2C1_SCL
LPSS_I2C1_SDA
R368
R364
R367
R365
X/10K/0201
R112
R369
R113
R258
R27
330
LED1
1.6*0.8*0.4mm Blue
FP_IDELED#
R26
R24
Q3A
Q3B
SATA_LED#
R275
Q22A
Q22B
SIO_PME#
R127
R120
R413
R157
4.7K
VCC_1P24V_1P35V_A Volt Selection
GPIO_36 | VCC_1P24V_1P35V_A
0 | 1.24V (default)
1 | 1.35
SMBus 1.8V/3.3V mode Select
GPIO_78 | SMBus
0 | 3.3V
1 | 1.8V (default)
PMU 1.8V/3.3V Mode Select
GPIO_88 | PMU
0 | 3.3V
1 | 1.8V (default)
SMBus No Re-Boot
GPIO_92 | No Re-Boot
0 | Disable (default)
1 | Enable
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AAEON
an ASUS assoc. co.
Title
SOC_SMBUS_GPIO
Size
Custom
Document Number
PICOAPL2A01
Rev:
A0.1_0_0
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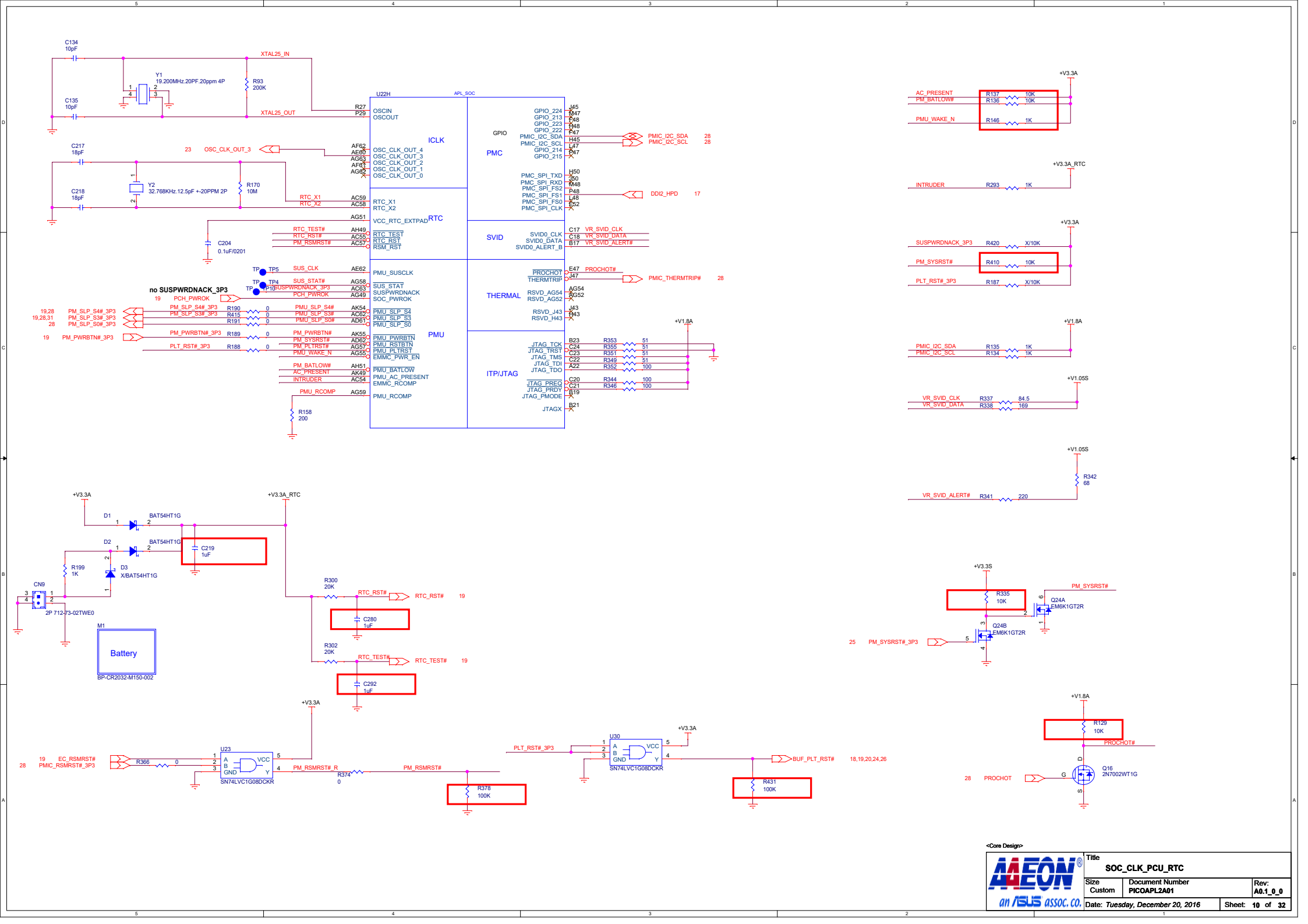

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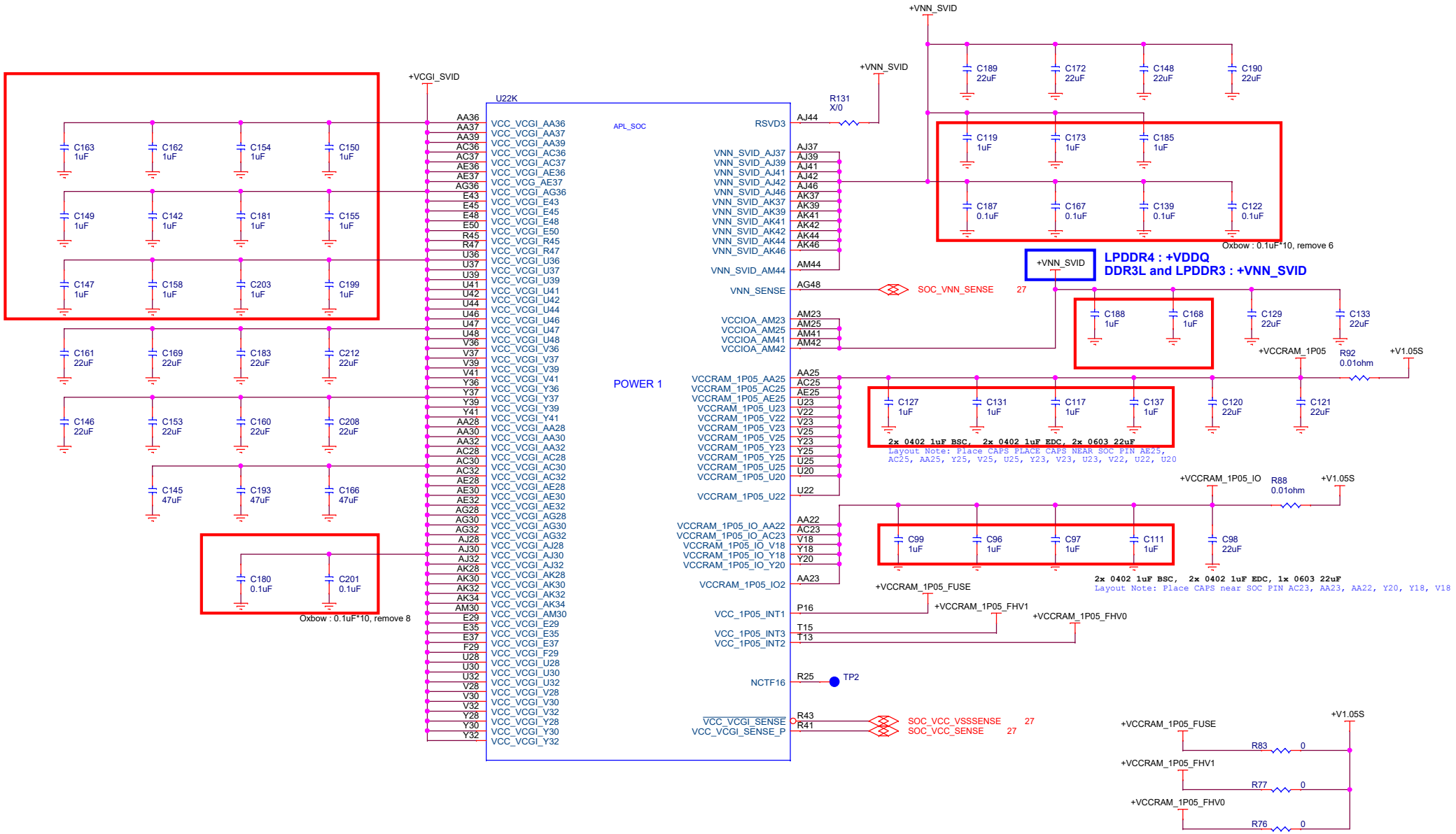
AAEON an ASUS assoc. co.	Title: SOC_CLK_PCU_RTC	
	Size: Custom	Document Number: PICOAPL2A01 Rev: A0.1_0_0
	Date: Tuesday, December 20, 2016	Sheet: 10 of 32



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Title: SOC_POWER I		
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
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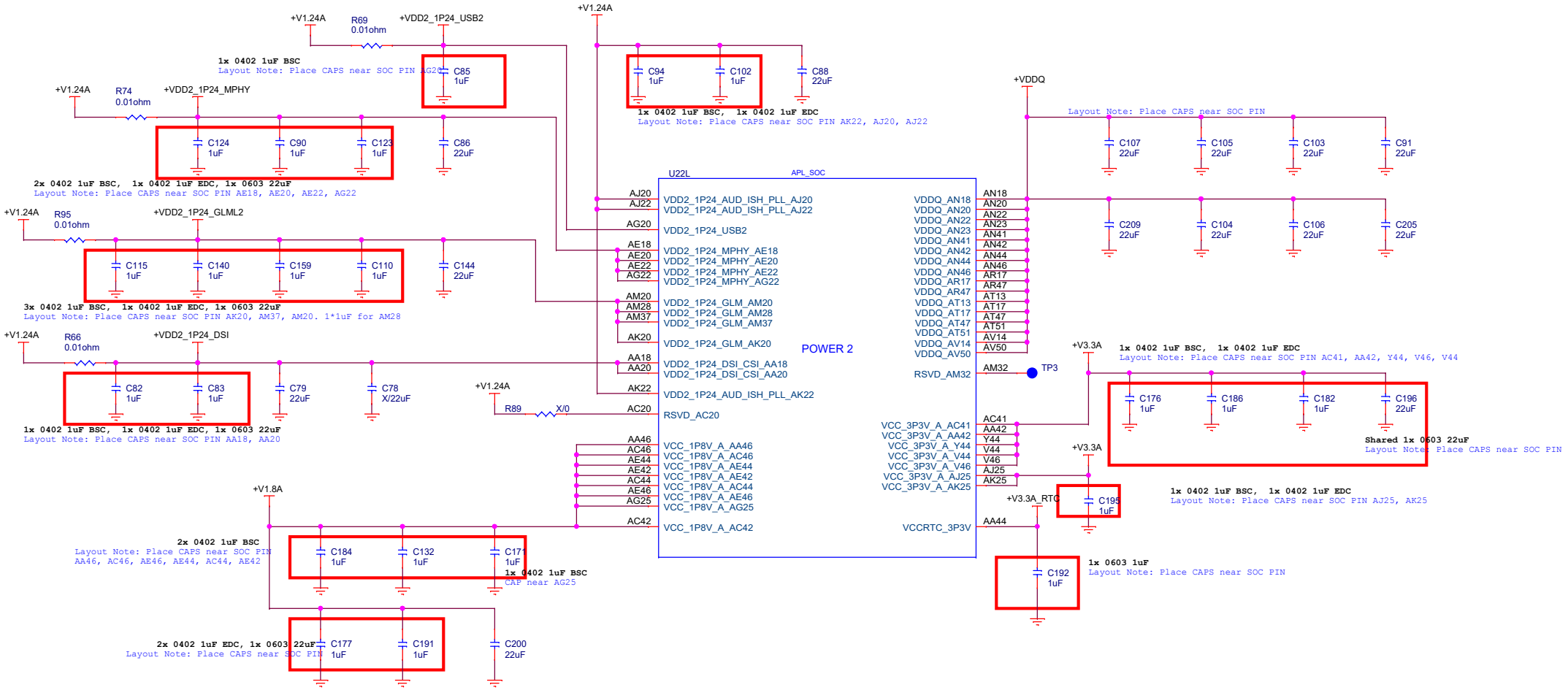

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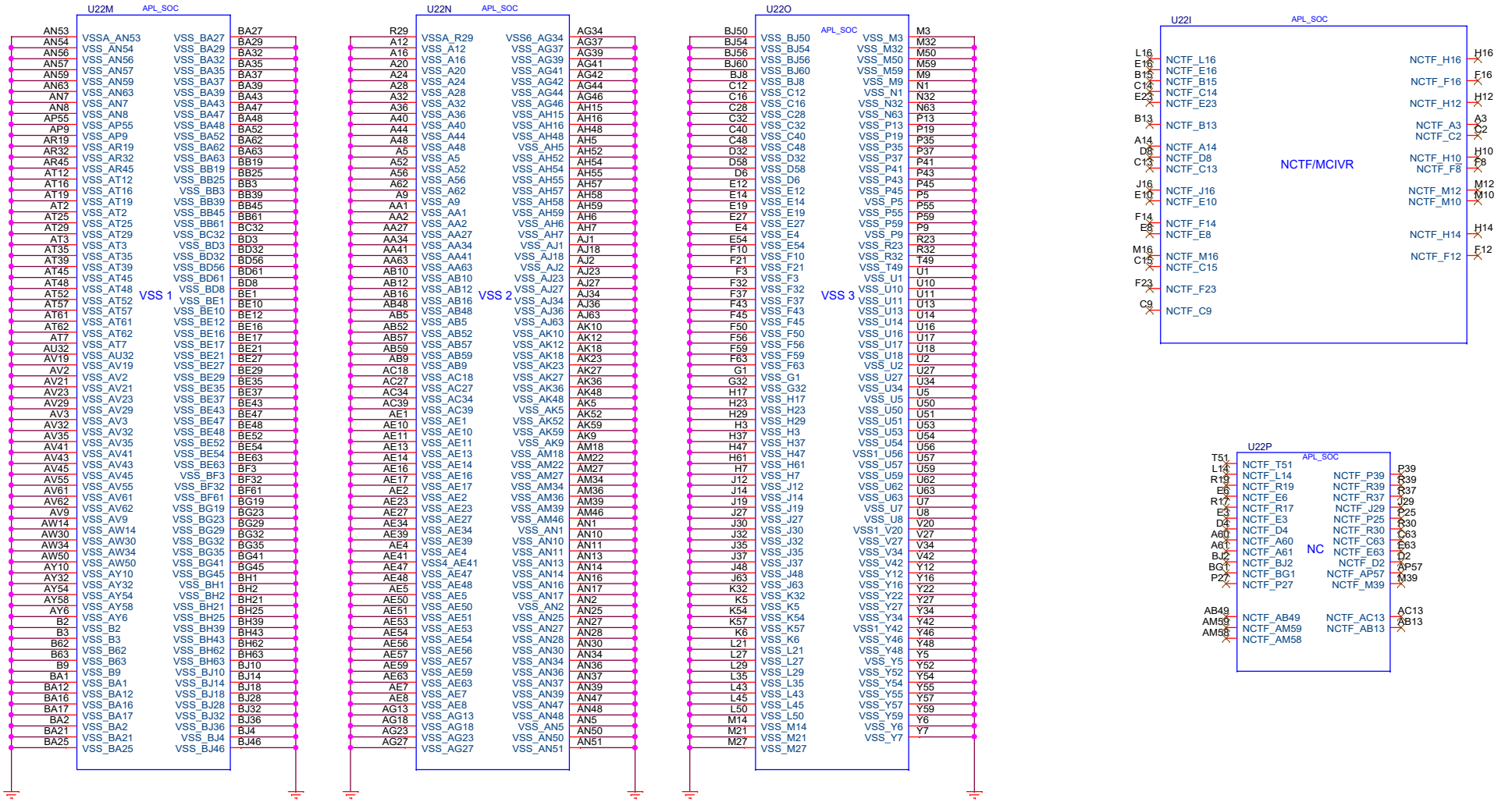
Title: SOC_POWER II

Size: Custom | Document Number: PICOAPL2A01 | Rev: A0.1_0_0

Date: Tuesday, December 20, 2016 | Sheet: 12 of 32



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AAEON an ASUS assoc. co.

Title: SOC_GND

Size: Custom | Document Number: PICOAPL2A01 | Rev: A0.1_0_0

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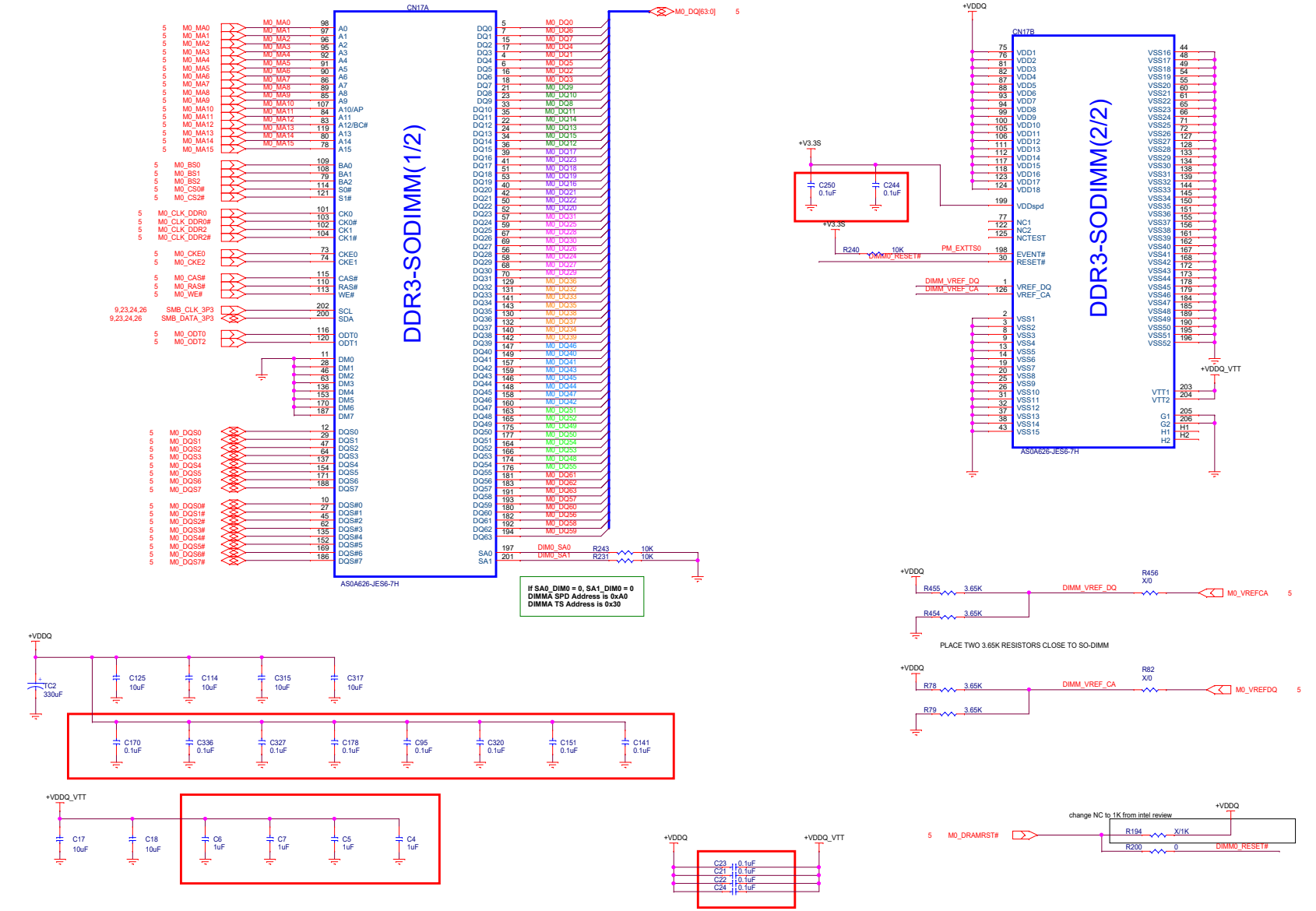
SODIMM#0



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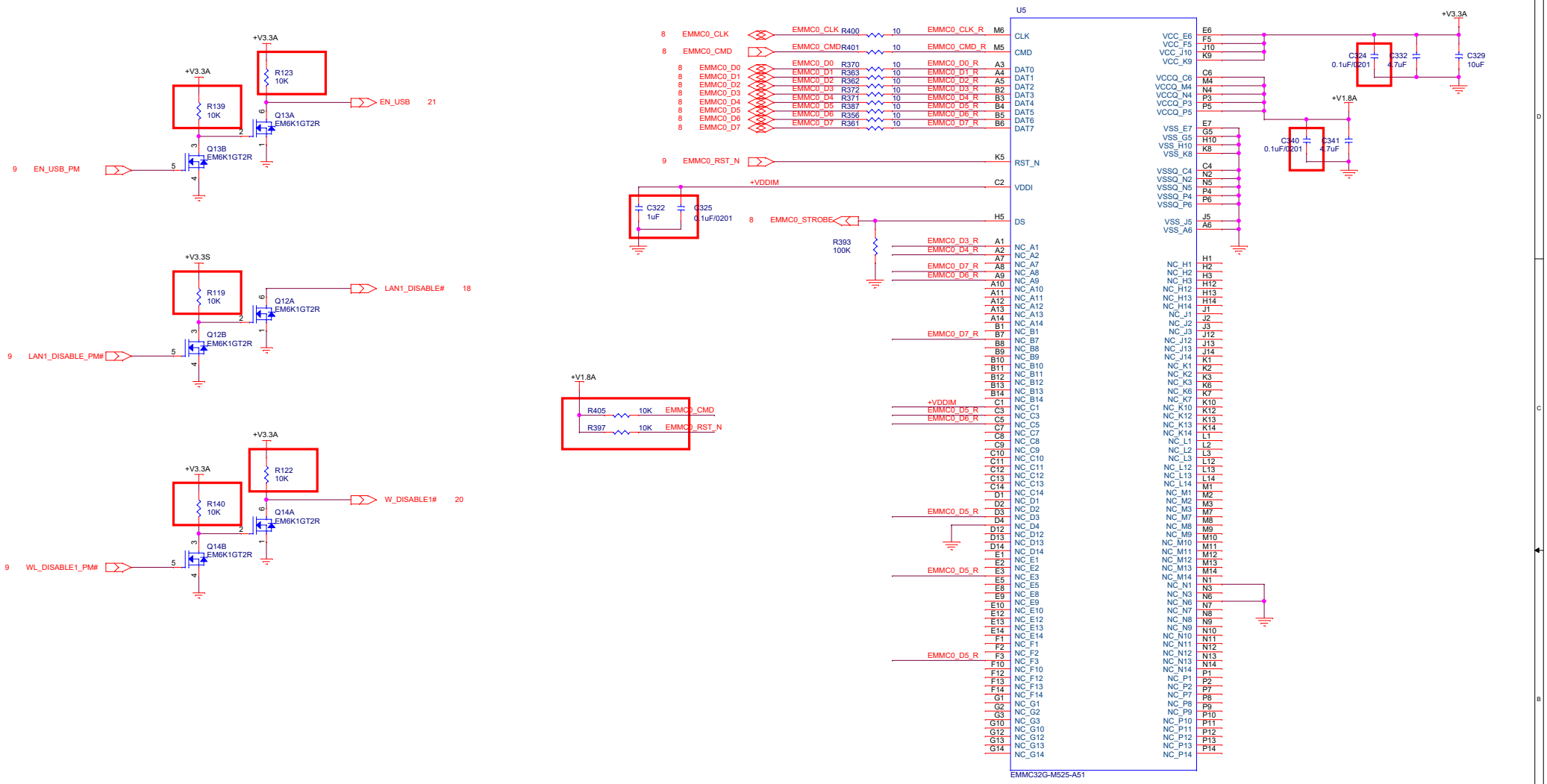
Title	DDR3L SODIMM		
Size C	Document Number PICOAPL2A01		Rev: A0.1_0_0
Date: Tuesday, December 20, 2016		Sheet: 14 of 32	



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AAEON an ASUS assoc. co.

Title: Level Shift-EMMC

Size	Document Number	Rev:
Custom	PICOAPL2A01	A0.1_0_0
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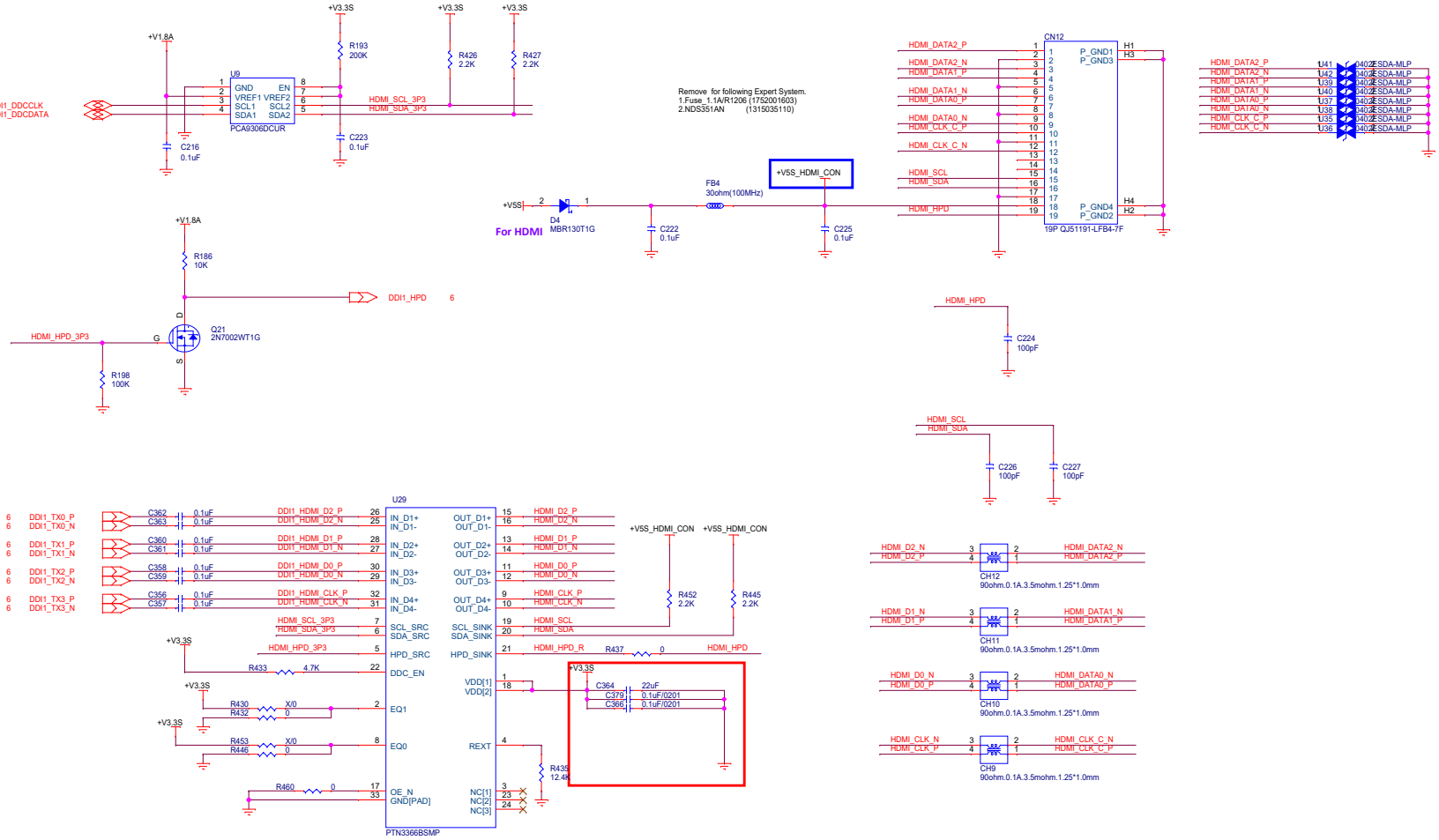
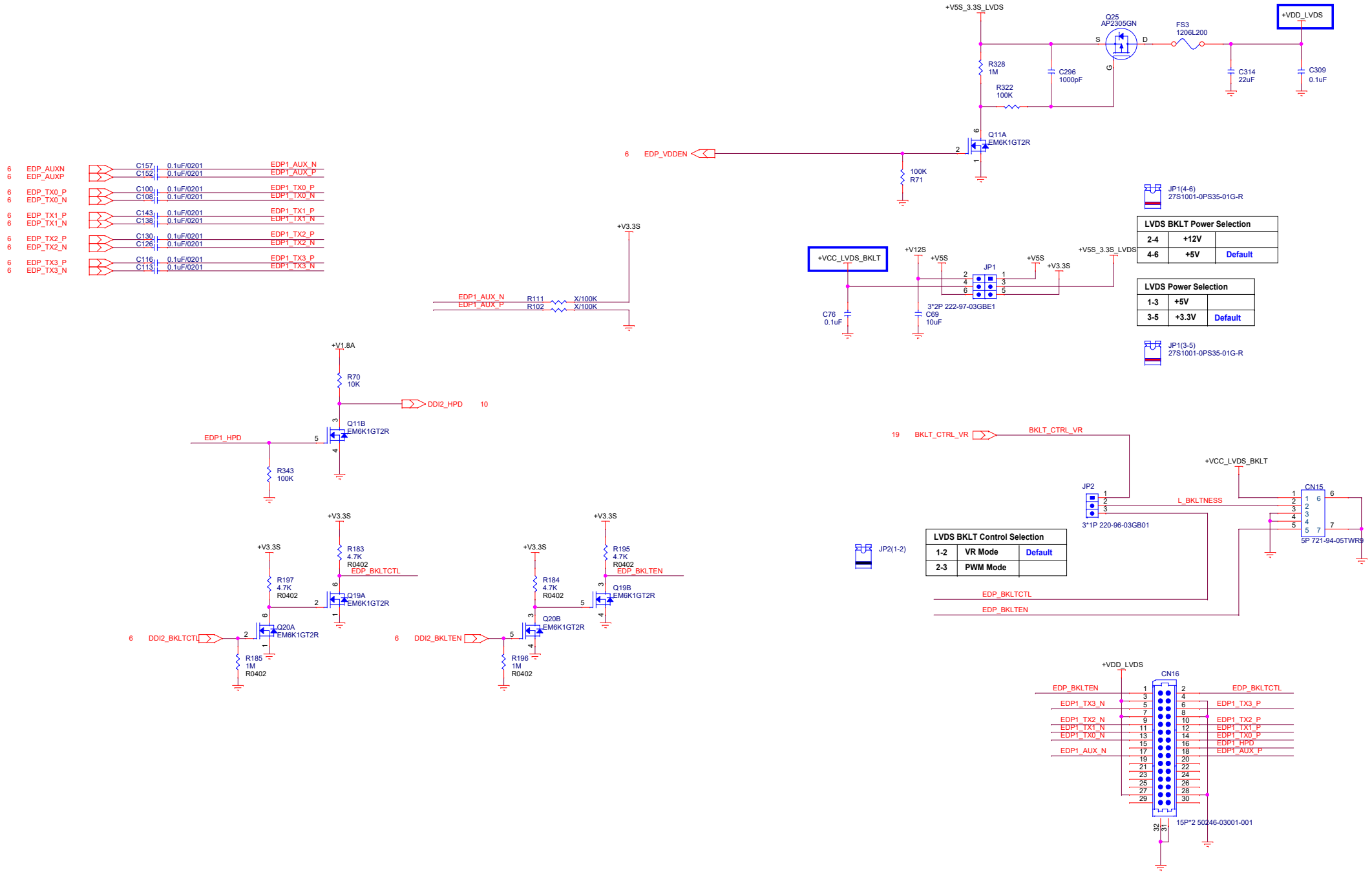
HDMI


+V1.8A
+V3.3S
U9
PCA9306DCUR
R193 200K
R426 2.2K
R427 2.2K
C216 0.1uF
C223 0.1uF
DDI1_DDCCLK
DDI1_DDCDATA
HDMI_SCL_3P3
HDMI_SDA_3P3
Remove for following Expert System.
1.Fuse_1.1A/R1206 (1752001603)
2.NDS351AN (1315035110)
+V5S
D4
MBR130T1G
For HDMI
FB4
30ohm(100MHz)
+V5S_HDMI_CON
C222 0.1uF
C225 0.1uF
CN12
19P QJ51191-LFB4-7F
HDMI_DATA2_P
HDMI_DATA2_N
HDMI_DATA1_P
HDMI_DATA1_N
HDMI_DATA0_P
HDMI_DATA0_N
HDMI_CLK_C_P
HDMI_CLK_C_N
HDMI_SCL
HDMI_SDA
HDMI_HPD
R186 10K
Q21
2N7002WT1G
HDMI_HPD_3P3
R198 100K
DDI1_HPD
C224 100pF
C226 100pF
C227 100pF
U29
PTN3366BSMP
DDI1_TX0_P
DDI1_TX0_N
DDI1_TX1_P
DDI1_TX1_N
DDI1_TX2_P
DDI1_TX2_N
DDI1_TX3_P
DDI1_TX3_N
C362 0.1uF
C363 0.1uF
C360 0.1uF
C361 0.1uF
C358 0.1uF
C359 0.1uF
C356 0.1uF
C357 0.1uF
DDI1_HDMI_D2_P
DDI1_HDMI_D2_N
DDI1_HDMI_D1_P
DDI1_HDMI_D1_N
DDI1_HDMI_D0_P
DDI1_HDMI_D0_N
DDI1_HDMI_CLK_P
DDI1_HDMI_CLK_N
HDMI_SCL_3P3
HDMI_SDA_3P3
HDMI_HPD_3P3
R433 4.7K
R430 X/0
R432 0
R453 X/0
R446 0
R460 0
R452 2.2K
R445 2.2K
R437 0
R439 12.4K
C364 22uF
C378 0.1uF/0201
C366 0.1uF/0201
HDMI_HPD_R
CH12
CH11
CH10
CH9
90ohm.0.1A.3.5mohm.1.25*1.0mm


+V5S_3.3S_LVDS
Q25
AP2305GN
FS3
1206L200
+VDD_LVDS
R328
1M
C296
1000pF
R322
100K
C314
22uF
C309
0.1uF
Q11A
EM6K1GT2R
6 EDP_VDDEN
100K
R71
JP1(4-6)
27S1001-0PS35-01G-R
LVDS BKLT Power Selection
2-4 +12V
4-6 +5V Default
+VCC_LVDS_BKLT
+V12S
+V5S
JP1
+V3.3S
+V5S_3.3S_LVDS
C76
0.1uF
C69
10uF
3*2P 222-97-03GBE1
LVDS Power Selection
1-3 +5V
3-5 +3.3V Default
JP1(3-5)
27S1001-0PS35-01G-R
6 EDP_AUXN
6 EDP_AUXP
C157
C152
0.1uF/0201
EDP1_AUX_N
EDP1_AUX_P
6 EDP_TX0_P
6 EDP_TX0_N
C100
C108
EDP1_TX0_P
EDP1_TX0_N
6 EDP_TX1_P
6 EDP_TX1_N
C143
C138
EDP1_TX1_P
EDP1_TX1_N
6 EDP_TX2_P
6 EDP_TX2_N
C130
C126
EDP1_TX2_P
EDP1_TX2_N
6 EDP_TX3_P
6 EDP_TX3_N
C116
C113
EDP1_TX3_P
EDP1_TX3_N
+V3.3S
EDP1_AUX_N
EDP1_AUX_P
R111
R102
X/100K
+V1.8A
R70
10K
DDI2_HPD 10
Q11B
EM6K1GT2R
EDP1_HPD
R343
100K
19 BKLT_CTRL_VR
BKLT_CTRL_VR
+VCC_LVDS_BKLT
JP2
L_BKLTNESS
CN15
3*1P 220-96-03GB01
5P 721-94-05TWR9
JP2(1-2)
LVDS BKLT Control Selection
1-2 VR Mode Default
2-3 PWM Mode
EDP_BKLTCTL
EDP_BKLTEN
+V3.3S
R183
4.7K
R0402
EDP_BKLTCTL
R197
4.7K
R0402
Q19A
EM6K1GT2R
Q20A
EM6K1GT2R
6 DDI2_BKLTCTL
R185
1M
R0402
R195
4.7K
R0402
EDP_BKLTEN
R184
4.7K
R0402
Q19B
EM6K1GT2R
Q20B
EM6K1GT2R
6 DDI2_BKLTEN
R196
1M
R0402
+VDD_LVDS
CN16
EDP_BKLTEN
EDP_BKLTCTL
EDP1_TX3_N
EDP1_TX3_P
EDP1_TX2_N
EDP1_TX2_P
EDP1_TX1_N
EDP1_TX1_P
EDP1_TX0_N
EDP1_TX0_P
EDP1_HPD
EDP1_AUX_N
EDP1_AUX_P
15P*2 50246-03001-001
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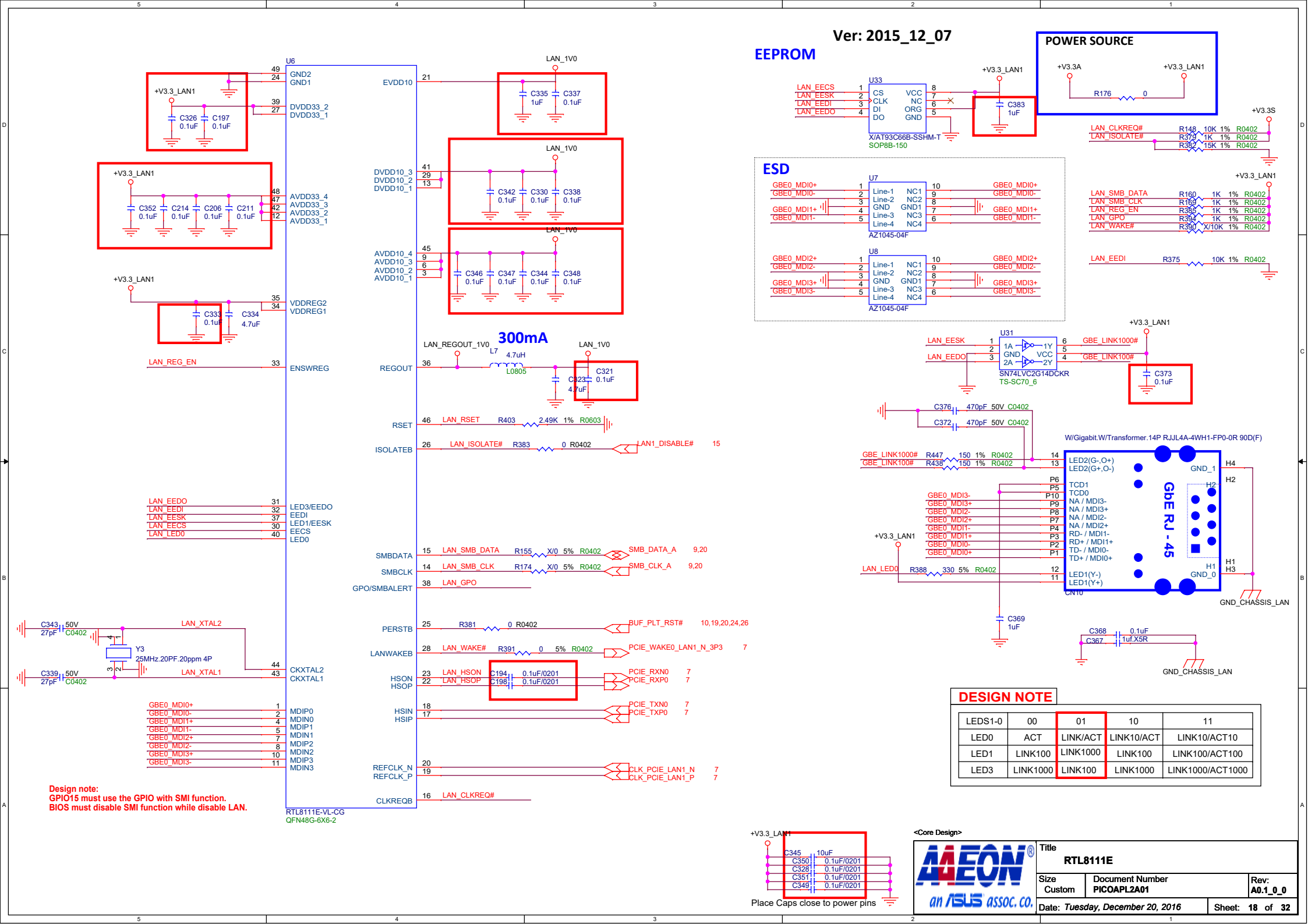
AAEON
an ASUS assoc. co.
Title
PTN3460 eDP to LVDS
Size
Custom
Document Number
PICOAPL2A01
Rev:
A0.1_0_0
Date: Tuesday, December 20, 2016
Sheet: 17 of 32

Ver: 2015_12_07



DESIGN NOTE

LEDS1-0	00	01	10	11
LED0	ACT	LINK/ACT	LINK10/ACT	LINK10/ACT10
LED1	LINK100	LINK1000	LINK100	LINK100/ACT100
LED3	LINK1000	LINK100	LINK1000	LINK1000/ACT1000

Title	RTL8111E		
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0	
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BIOS_DIS1#	BIOS_DIS0#	Chipset SPI_CS1# Destination	Chipset SPI_CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SP1	Module	SPI0/SPI1	3

Hardware Monitor

IT8528
IT8529
VFBGA

GA20/ECSCI/ECSMI/KBRST# pay attention for leak current

(1) Each input pin should be driven or pulled.
(2) Open-drain output pin should be pulled.

DO NOT place any pull up resistor on G0,G2,G6 (Reserved for Hardware strapping)

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

COM1/RS232

Wake on Modem

Auto power button		
1	Enable	Default
2	Disable	

CMOS Control Selection(RTC_RST#)		
3	Save CMOS	Default
4	Clear CMOS	

Note: Place all capacitors close to IT8528.

DIPSW setting for AT or ATX power mode.

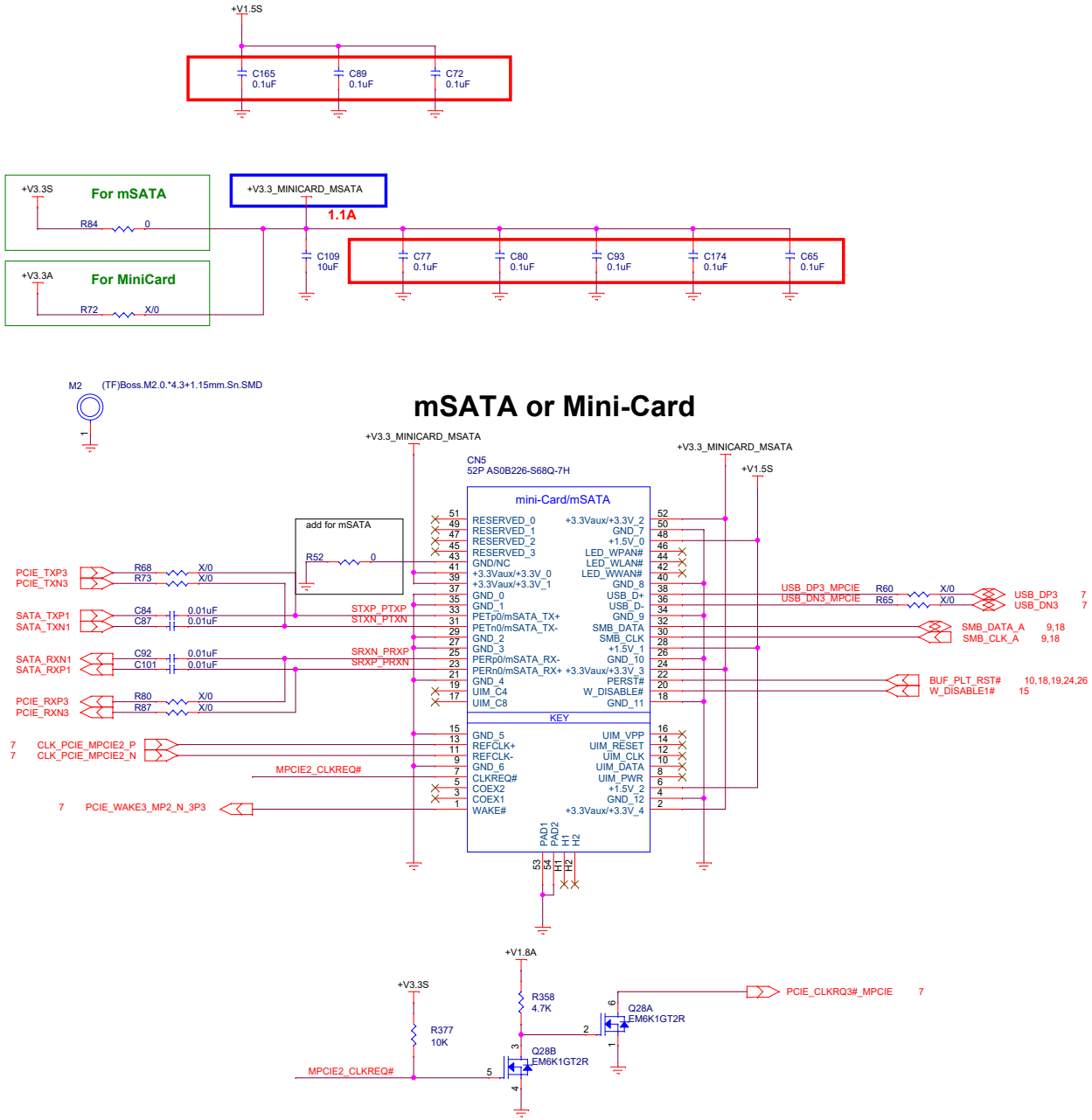
<Core Design>

AAEON an /SUS assoc. co.

Title: EC ITE8528

Size: Custom | Document Number: PICOAPL2A01 | Rev: A0.1_0_0

Date: Tuesday, December 20, 2016 | Sheet: 19 of 32

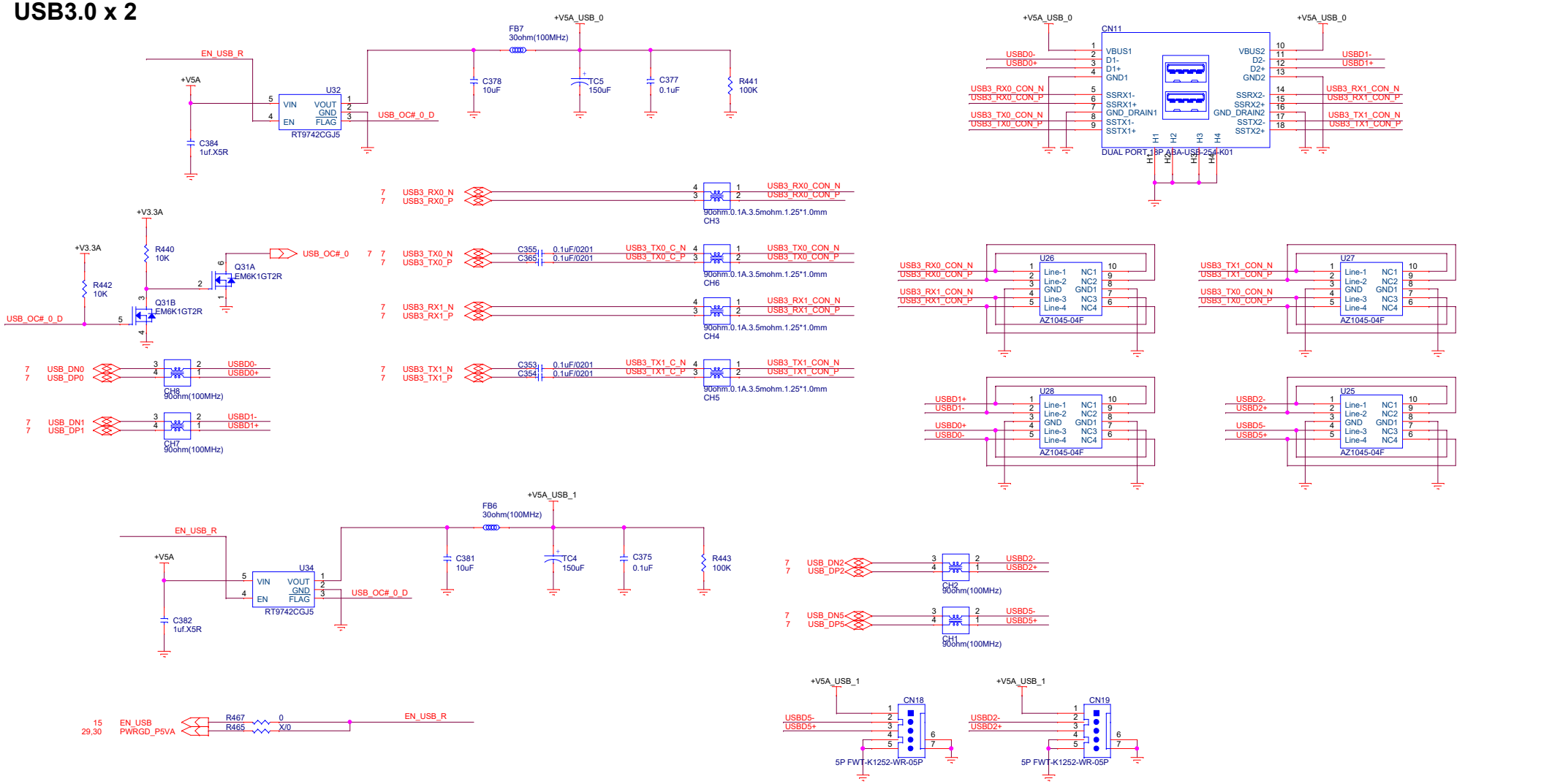


<Core Design>

AAEON an ASUS assoc. co.

Title: mini-Card/mSATA		
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
Date: *Tuesday, December 20, 2016*	Sheet: 20 of 32	

USB3.0 x 2



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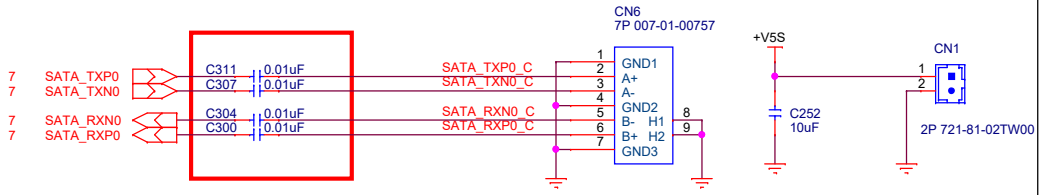
AAEON an ASUS assoc. co.	Title: USB 3.0/2.0 PORT	
	Size: Custom	Document Number: PICOAPL2A01 — Rev: A0.1_0_0
	Date: *Tuesday, December 20, 2016*	Sheet: 21 of 32



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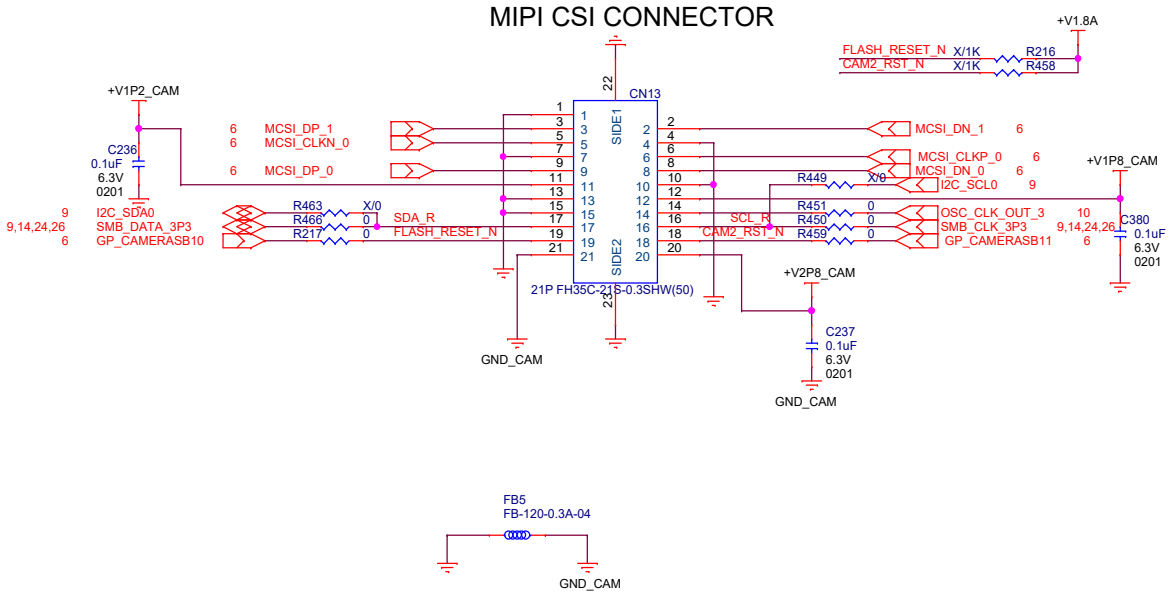
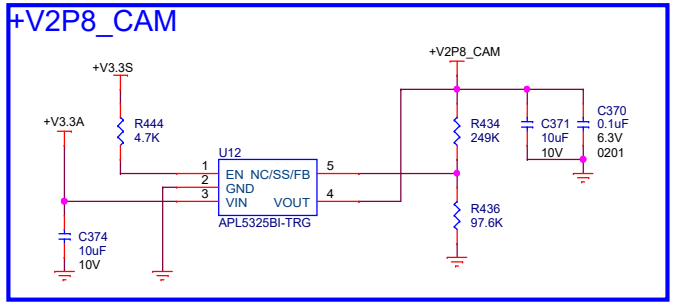
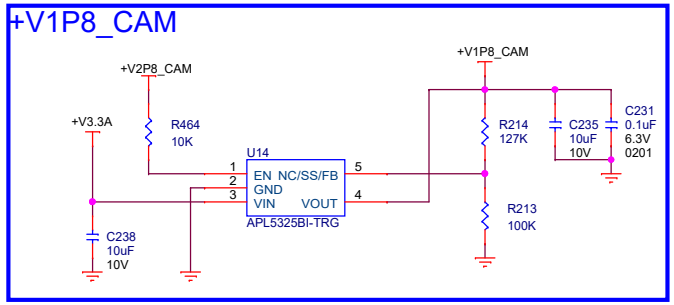
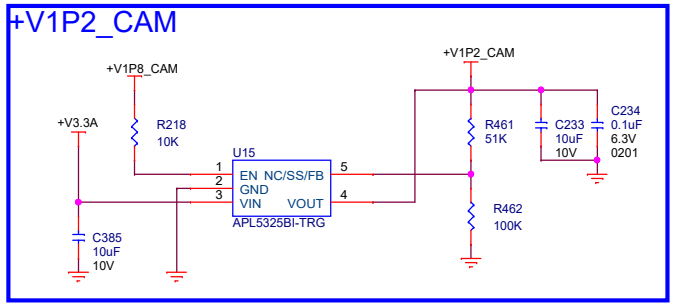
AAEON an ASUS assoc. co.	Title: **Serial Port 1/2/SATA**	
Size: B	Document Number: **PICOAPL2A01**	Rev: **A0.1_0_0**
Date: *Tuesday, December 20, 2016*	Sheet: **22** of **32**	









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AAEON an ASUS assoc. co.

Title: CSI		
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
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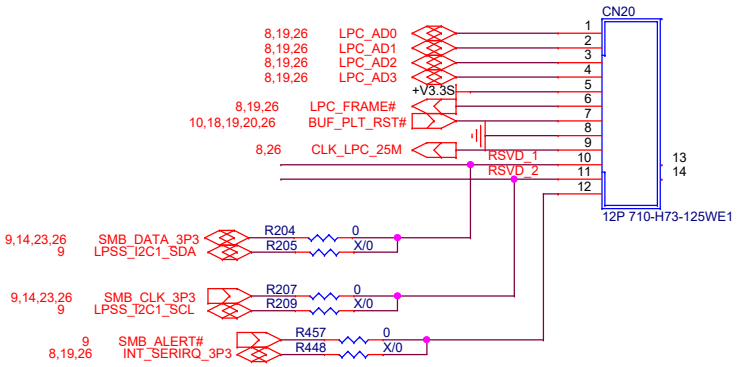
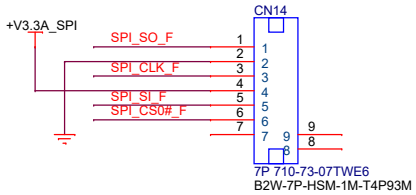
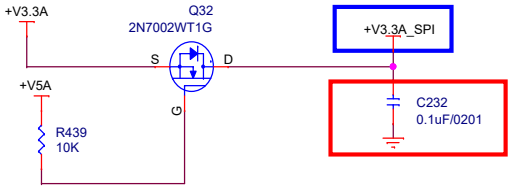
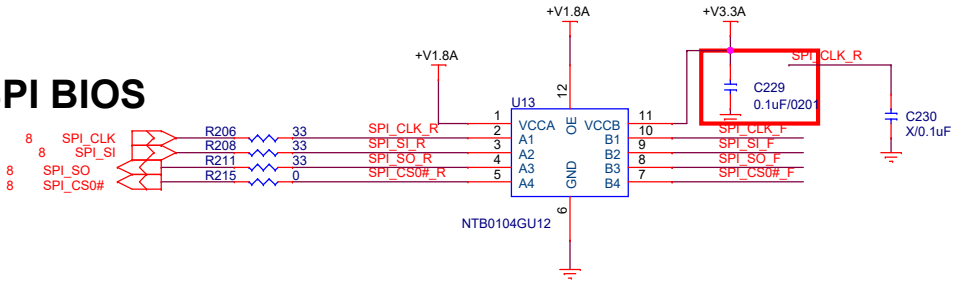
LPC Debug Connector

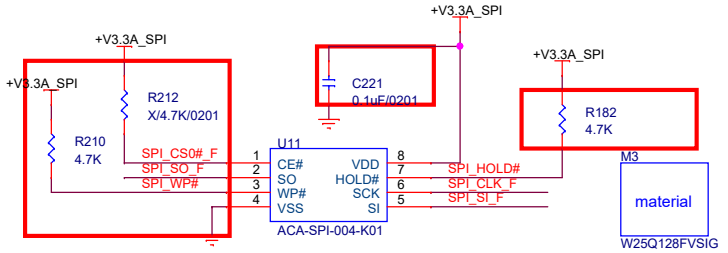






SPI BIOS





8 pin : 1651900860 (TF)IC SKT.SMD.8Pin.SOIC.LOTES.ACA-SPI-004-K0
1462001280 (TF)IC.Flash Memory.128M Bit serial.SOIC-8(208mil).SMD.w/ Dual & Quad SPI.Winbond.W25Q128FVSIG

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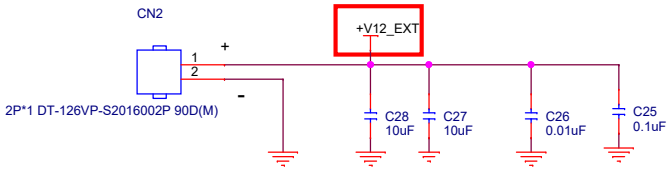
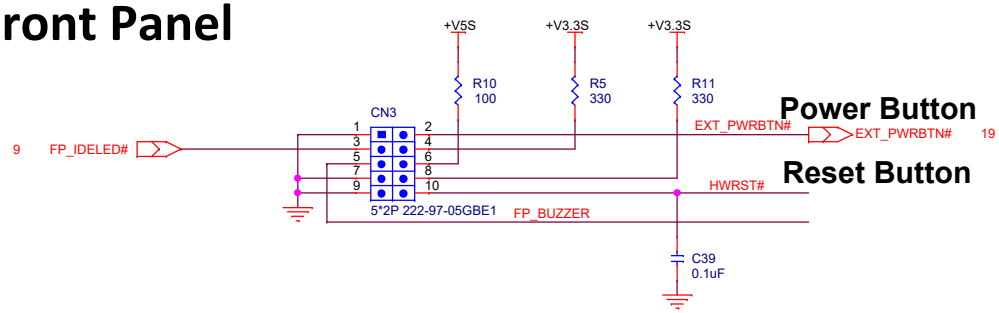
AAEON an ASUS assoc. co.

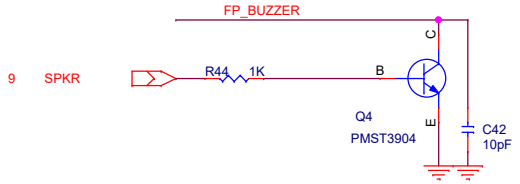
Title: **H/W Mon/ Debug /CMOS**		
Size: B	Document Number: **PICOAPL2A01**	Rev: **A0.1_0_0**
Date: *Tuesday, December 20, 2016*	Sheet: **24** of **32**	

+12V Power Input

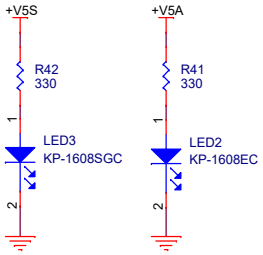


Front Panel

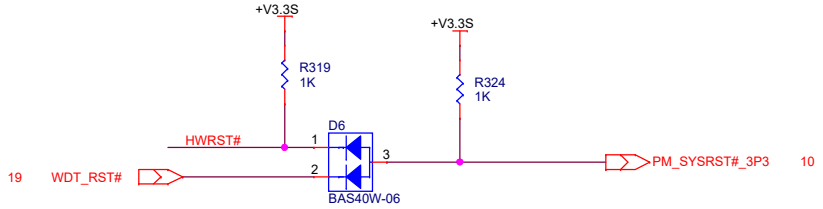




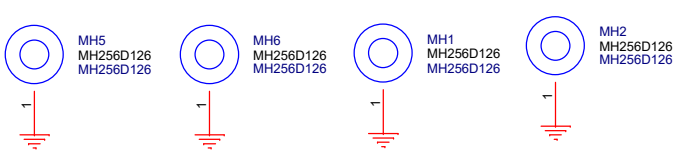
Power LED

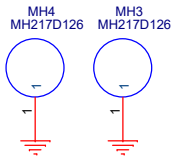


System Reset



Mounting Holes / Non-PTH





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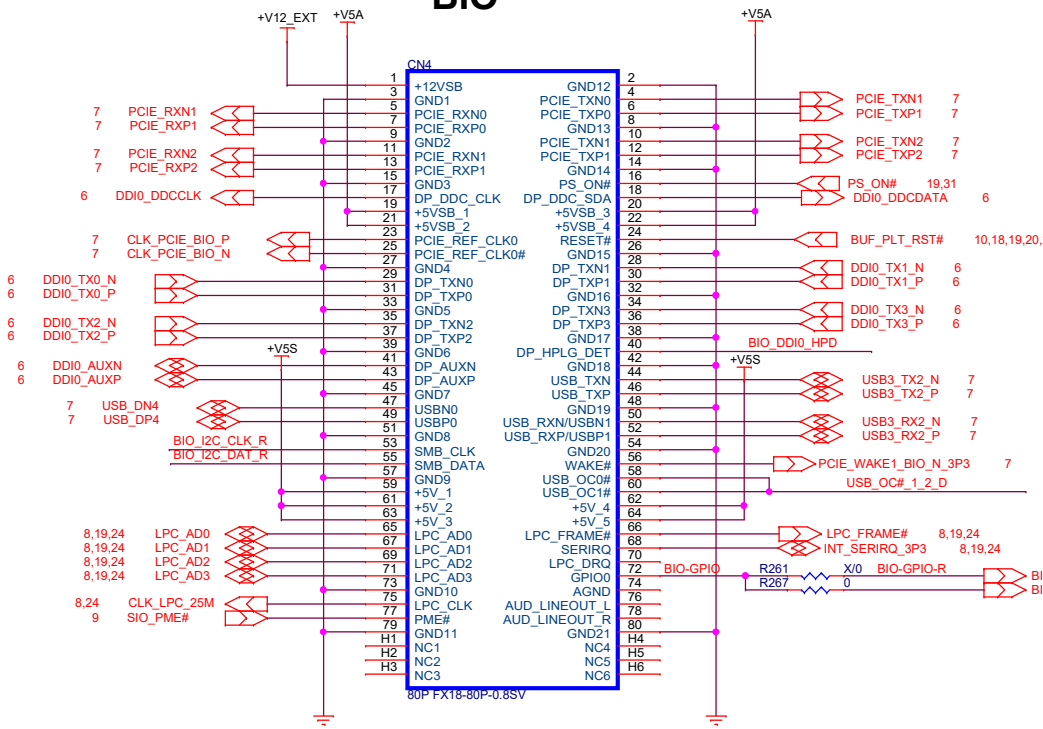
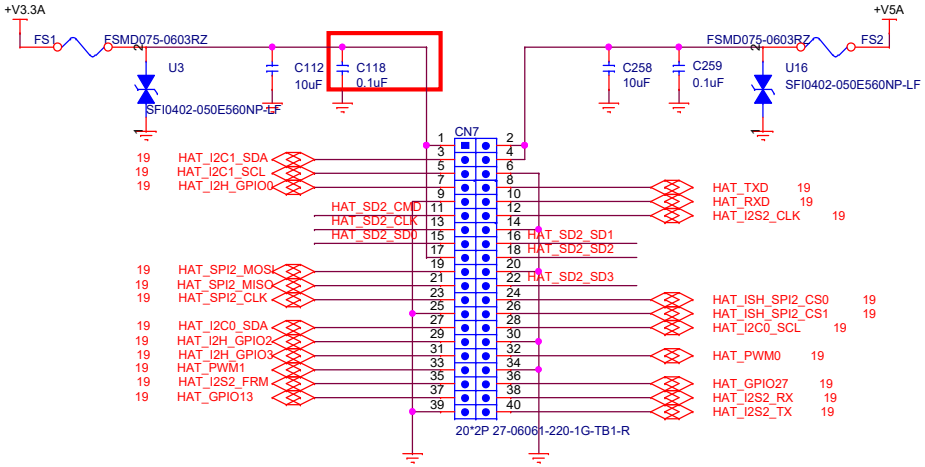
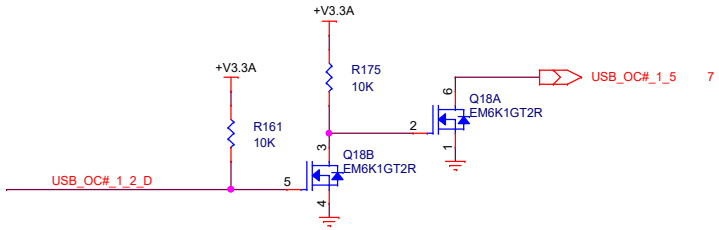
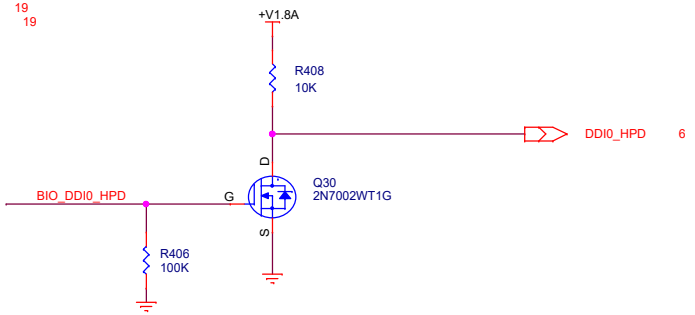
AAEON an ASUS assoc. co.	Title: Power in	
Size: B	Document Number: PICOAPL2A01	Rev: A0.1_0_0
Date: Tuesday, December 20, 2016	Sheet: 25 of 32	

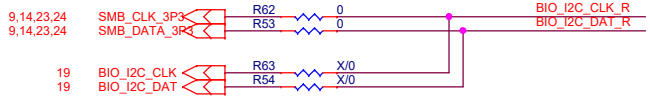
BIO

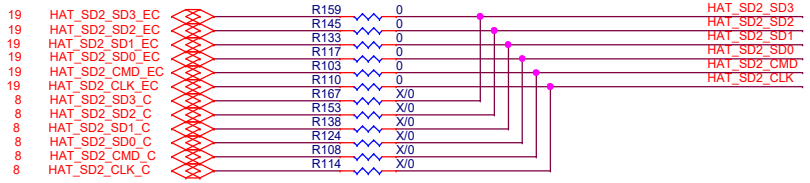












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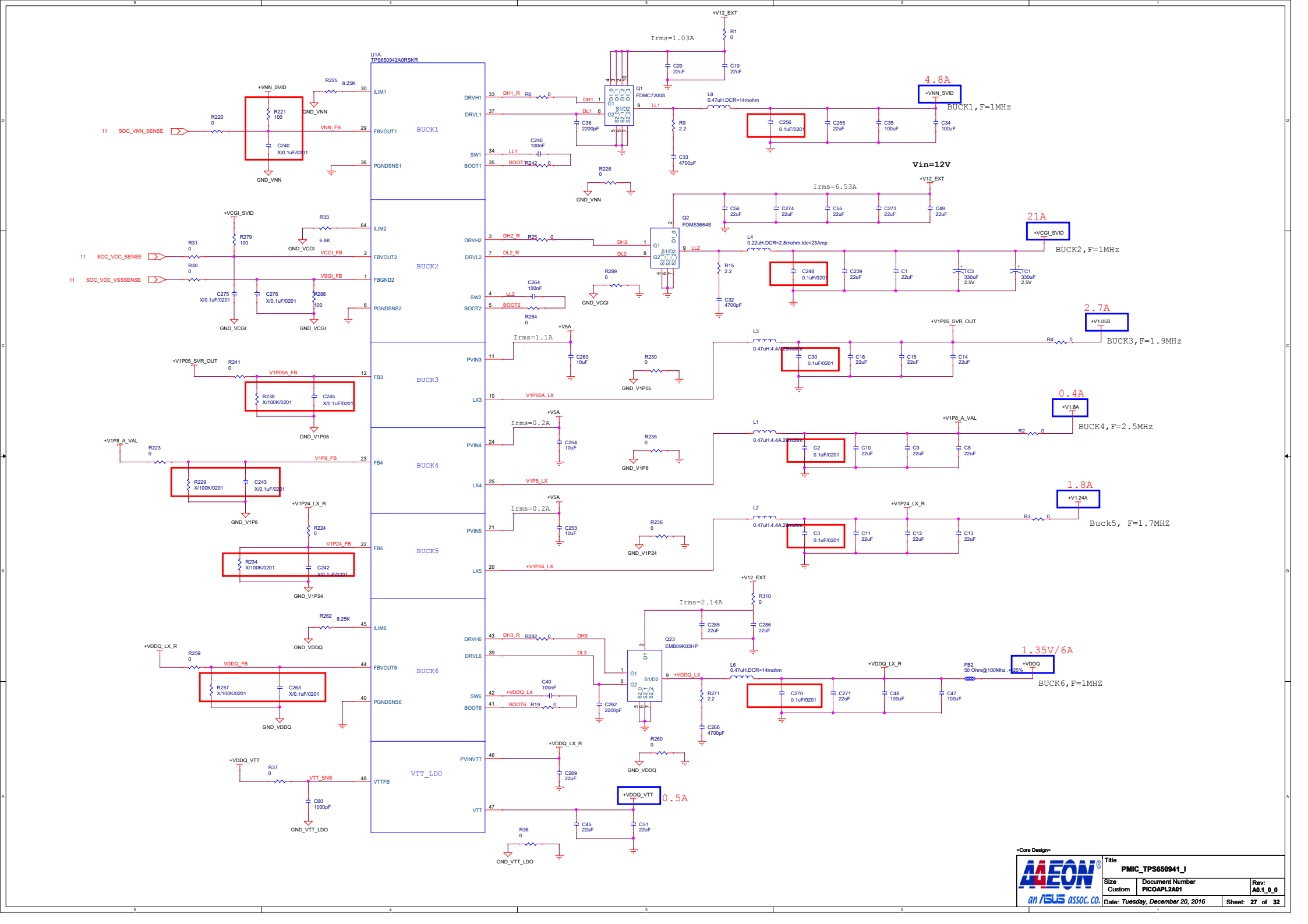
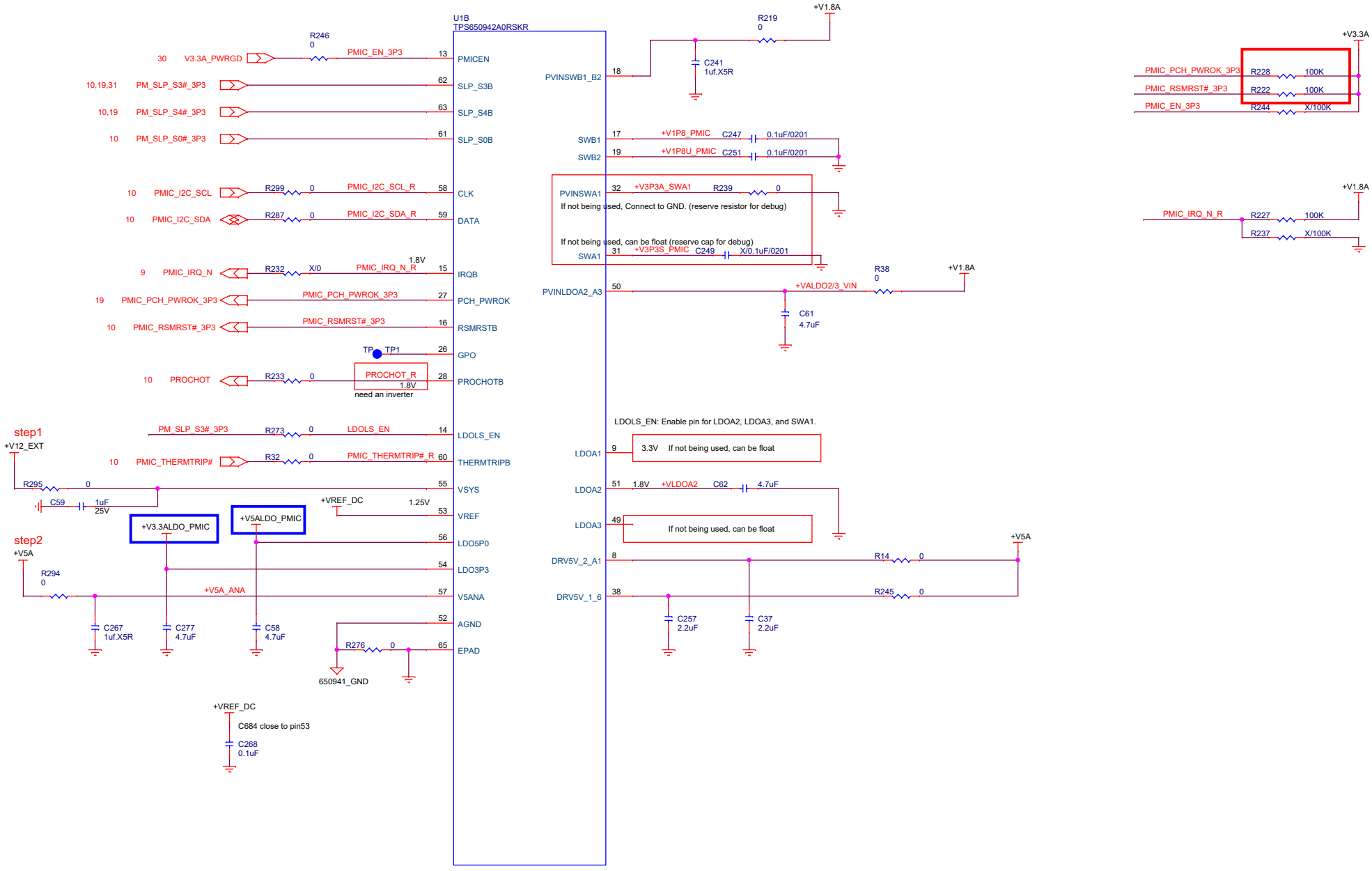
AAEON an ASUS assoc. co.	Title: BIO/ HAT	
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
Date: Tuesday, December 20, 2016	Sheet: 26 of 32	


U1A
TPS650942A0RSKR
BUCK1
BUCK2
BUCK3
BUCK4
BUCK5
BUCK6
VTT_LDO
+V12_EXT
Irms=1.03A
Q1
FDMC7200S
4.8A
+VNN_SVID
BUCK1,F=1MHz
Vin=12V
Irms=6.53A
Q2
FDMS3664S
21A
+VCGI_SVID
BUCK2,F=1MHz
2.7A
+V1.05S
BUCK3,F=1.9MHz
0.4A
+V1.8A
BUCK4,F=2.5MHz
1.8A
+V1.24A
Buck5, F=1.7MHZ
Irms=2.14A
Q23
EMB09K03HP
1.35V/6A
+VDDQ
BUCK6,F=1MHZ
0.5A
+VDDQ_VTT
SOC_VNN_SENSE
SOC_VCC_SENSE
SOC_VCC_VSSSENSE
GND_VNN
GND_VCGI
GND_V1P05
GND_V1P8
GND_V1P24
GND_VDDQ
GND_VTT_LDO



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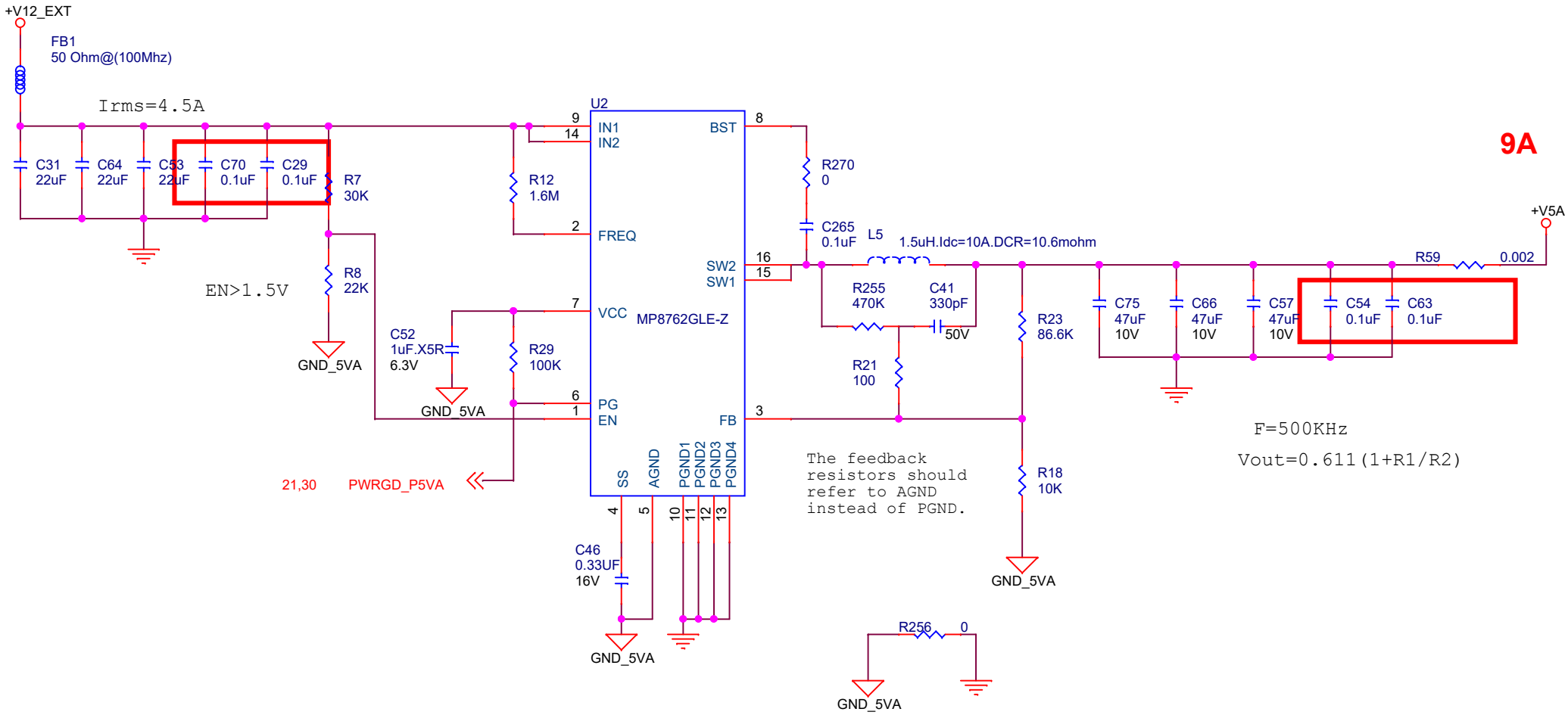
AAEON an ASUS assoc. co.	Title: PMIC_TPS650941_II	
	Size: Custom	Document Number: PICOAPL2A01 — Rev: A0.1_0_0
	Date: Tuesday, December 20, 2016	Sheet: 28 of 32



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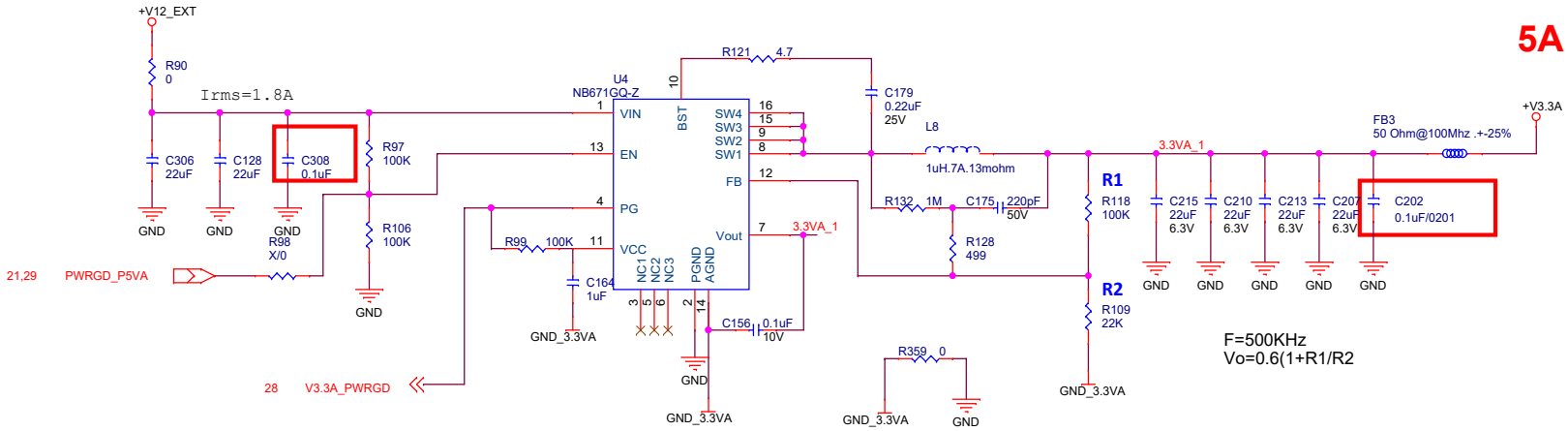
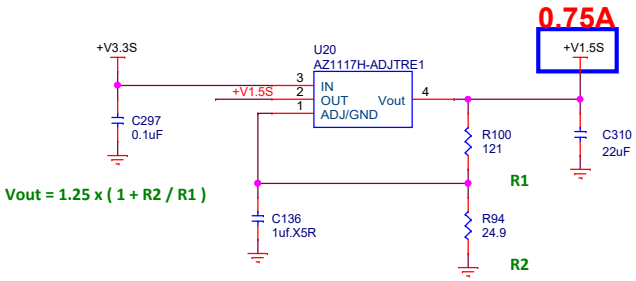
AAEON an ASUS assoc. co.	Title: **Power VR : +V5A**	
Size: Custom	Document Number: **PICOAPL2A01**	Rev: **A0.1_0_0**
Date: *Tuesday, December 20, 2016*	Sheet: **29** of **32**	

1.35V<EN<12V
EN voltage should be lower than 12V





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AAEON an ASUS assoc. co.	Title: Power VR : +V3.3A.+V1.5S	
Size: Custom	Document Number: PICOAPL2A01	Rev: A0.1_0_0
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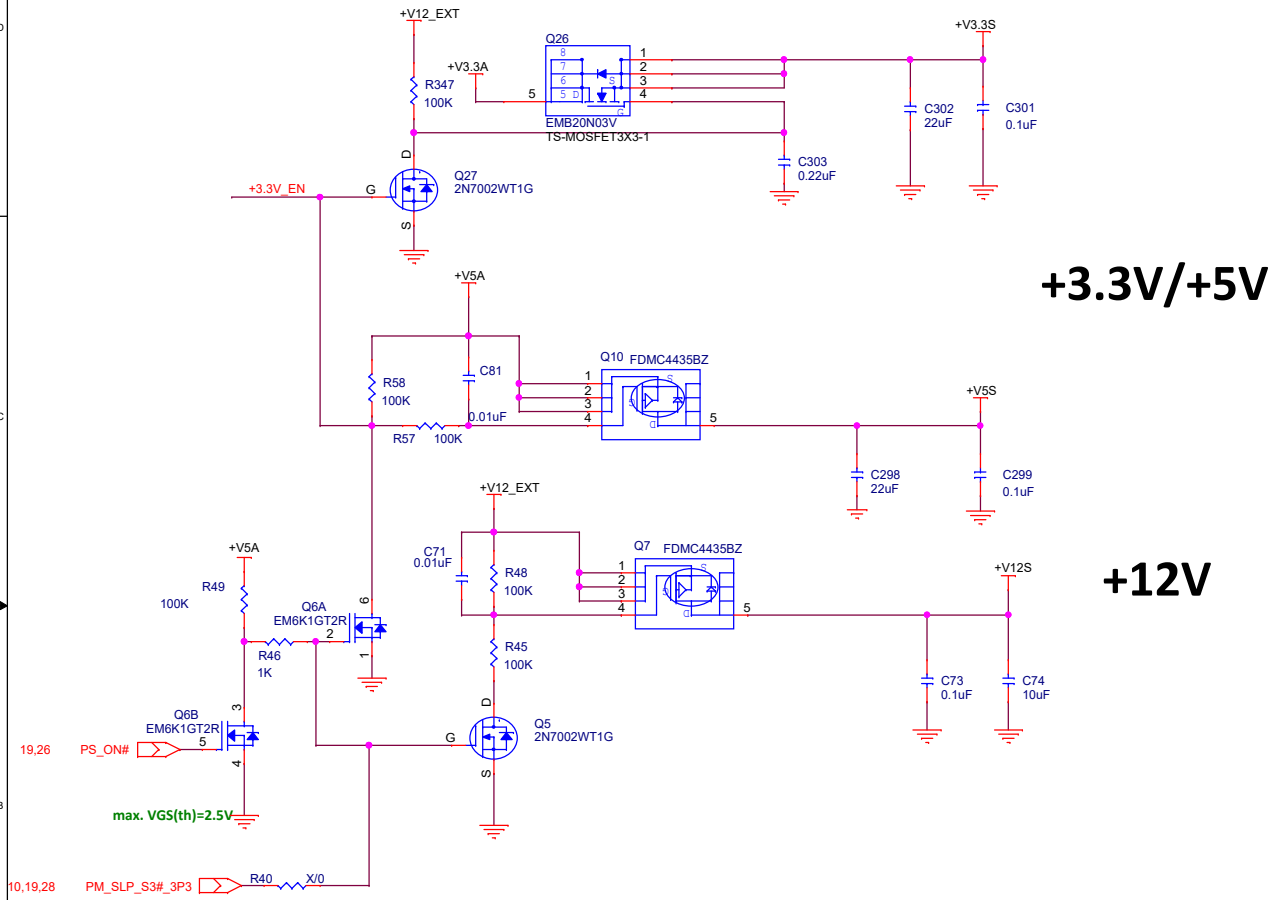
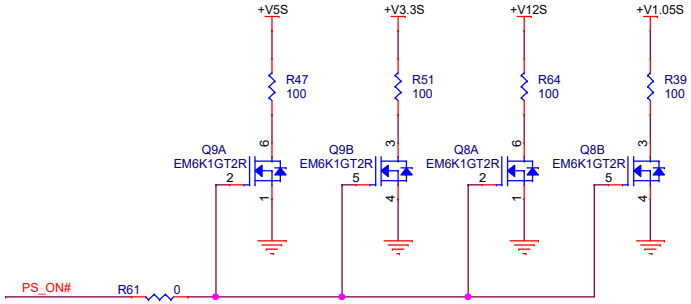


+3.3V/+5V

+12V



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AAEON an ASUS assoc. co.

Title: **Power Sequence Logic**

Size	Document Number	Rev:
Custom	PICOAPL2A01	A0.1_0_0

Date: *Tuesday, December 20, 2016* Sheet: **31** of **32**

HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2016/3/20	A0.1	First Release.	1-32	Daniel	Chienkow

<Core Design>

AAEON an ASUS assoc. co.

Title: Revision History

Size: B | Document Number: PICOAPL2A01 | Rev: A0.1_0_0

Date: *Tuesday, December 20, 2016* | Sheet: 32 of 32