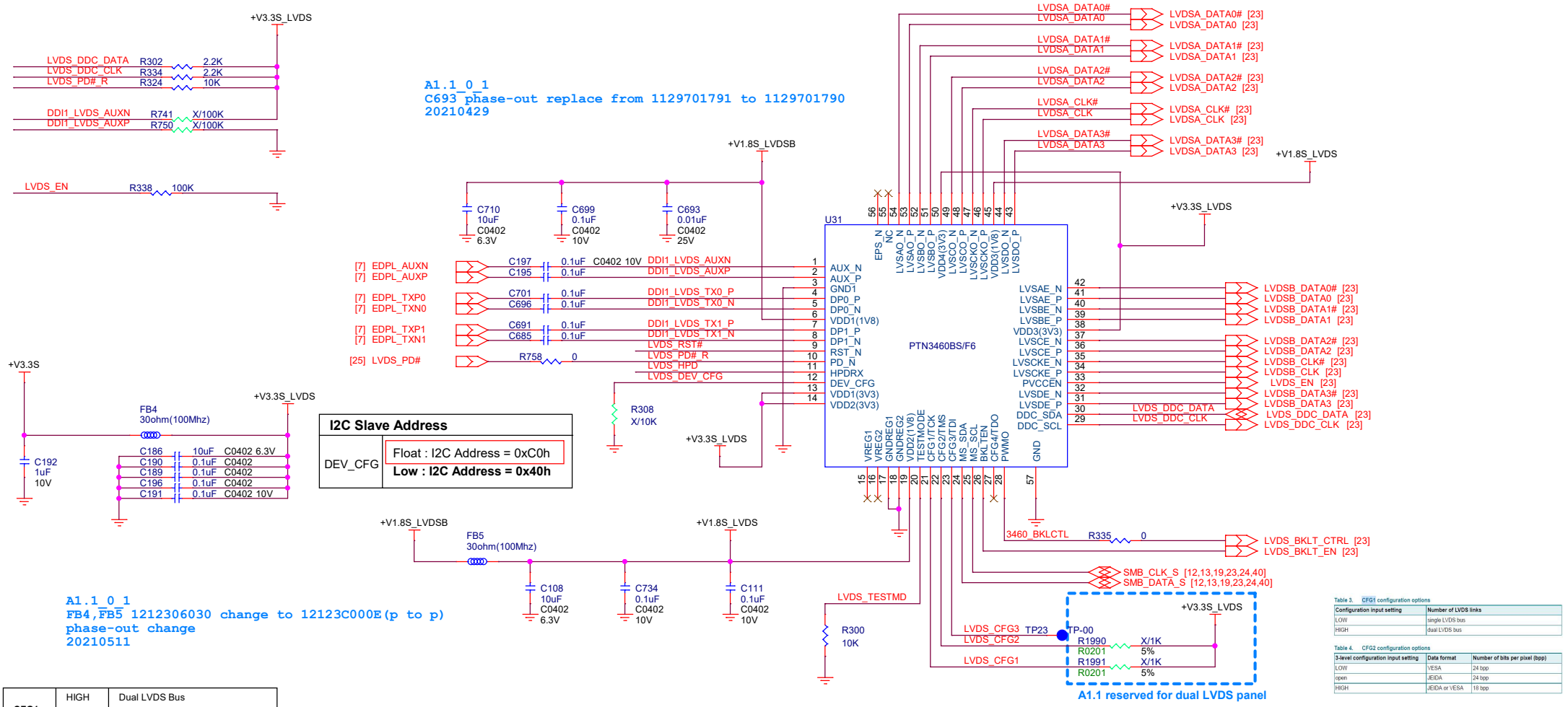
PTN3460



I2C Slave Address

DEV_CFG	Float : I2C Address = 0xC0h **Low : I2C Address = 0x40h**

A1.1_0_1
FB4,FB5 1212306030 change to 12123C000E(p to p)
phase-out change
20210511

CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

Table 3. CFG1 configuration options

Configuration input setting	Number of LVDS links
LOW	single LVDS bus
HIGH	dual LVDS bus

Table 4. CFG2 configuration options

3-level configuration input setting	Data format	Number of bits per pixel (bpp)
LOW	VESA	24 bpp
open	JEIDA	24 bpp
HIGH	JEIDA or VESA	18 bpp

AAEON an ASUS assoc. co.

Title: **DP TO LVDS**

Size	Document Number	Rev:
B	COM-CFHB6	A1.1_0_1

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