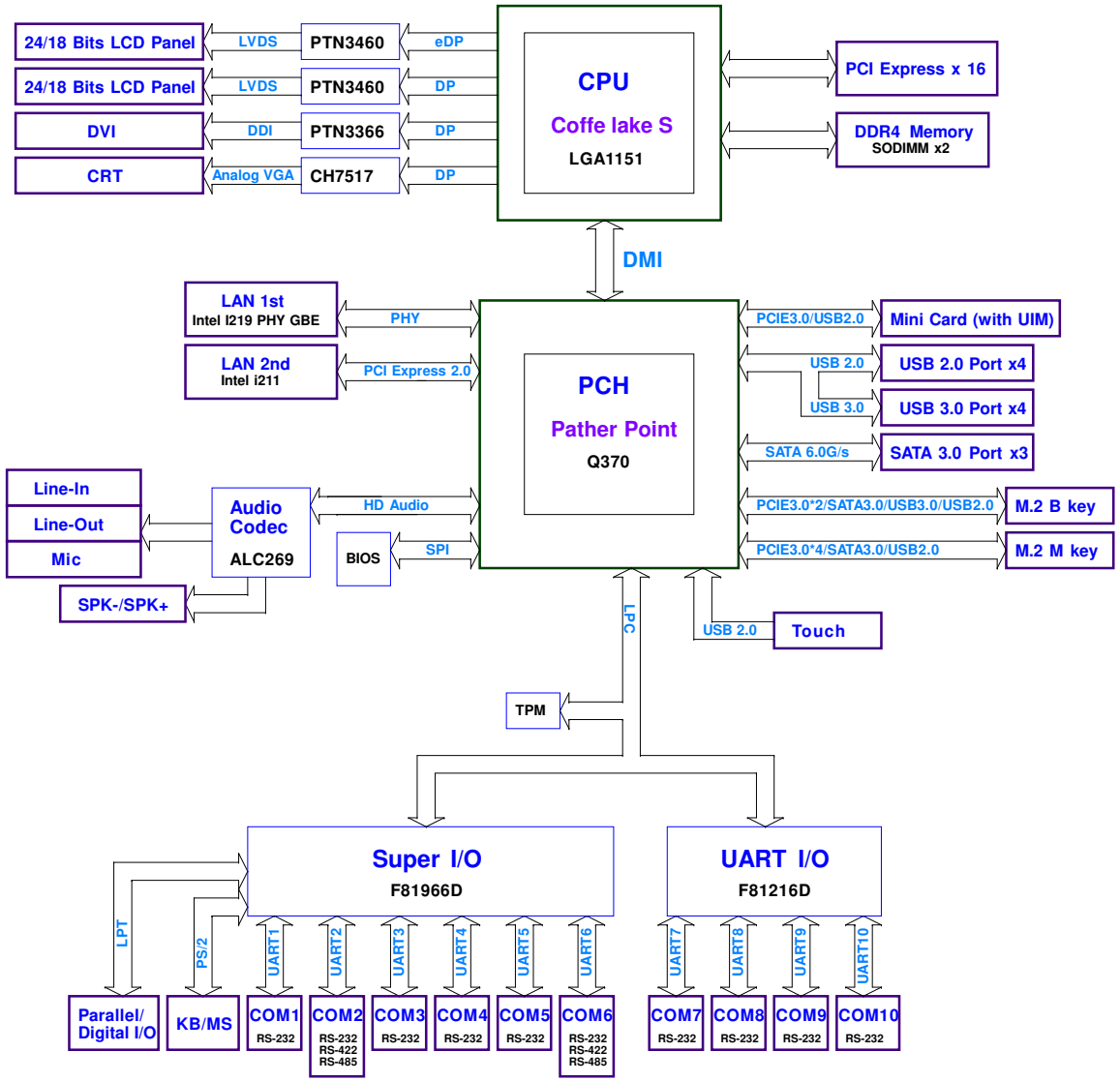
PCM-CFS Rev.A0.2

Sub Compact Board



Project Number : E120808

Production Line : Sub.ECM.AACM

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Title: Cover Sheet		
Size: Custom	Document Number: PCM-CFS	Rev: A0.2
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PCH GPIO Pins :

Group	Name	Power Well	Default	GPIO Function
Group A	GPP_A0			KBRST
	GPP_A1			LPC_AD0
	GPP_A2			LPC_AD1
	GPP_A3			LPC_AD2
	GPP_A4			LPC_AD3
	GPP_A5			LPC_FRAME#
	GPP_A6			INT_SERIRQ
	GPP_A7			PIRQA#
	GPP_A8			PM_CLKRUN#
	GPP_A9			PCH_CLK_LPC0
	GPP_A10			PCI_CLK_EC
	GPP_A11			EC_LPC_PME#
	GPP_A12			
	GPP_A13			SUS_PWR_ACK
	GPP_A14			PM_SUS_STAT#
	GPP_A15			SUSACK#
	GPP_A16			
	GPP_A17~A23			
Group B	GPP_B0	Primary Core 3.3V		
	GPP_B1			
	GPP_B2			GP_VRALERTB
	GPP_B3			
	GPP_B4			
	GPP_B5			CLK_PCIE_LAN1_REQ#
	GPP_B6~10			
	GPP_B11			MPHY_EXT_PWR_GATEB
	GPP_B12			SLP_S0#
	GPP_B13			PLT_RST#
	GPP_B14			HDA_SPKR
	GPP_B15~22			
	GPP_B23			SML1_ALERT#
Group C	GPP_C0			SMB_CLK
	GPP_C1			SMB_DATA
	GPP_C2			SMB_ALERT#
	GPP_C3			SML0_CLK
	GPP_C4			SML0_DATA
	GPP_C5			SML0_ALERT#
	GPP_C6			
	GPP_C7			
	GPP_C8~23			

Group	Name	Power Well	Default	GPIO Function
Group D	GPP_D0~8	Deep Sleep Power 3.3V		
	GPP_D9			SLEEP#
	GPP_D10			LID#
	GPP_D11			PCIE_CPPE0#
	GPP_D12			PCIE_CPPE1#
	GPP_D13			W_DISABLE1#
	GPP_D14			CONFIG2_B
	GPP_D15~D23			
Group E	GPP_E0~3	Primary Core 3.3V		
	GPP_E4			SCI#
	GPP_E5			SMI#
	GPP_E6~7			
	GPP_E8			SATA_LED#
	GPP_E9			USB_OC#_0_1
	GPP_E10			USB_OC#_2_3
	GPP_E11			USB_OC#_4_5
	GPP_E12			USB_OC#_6_7
Group F	GPP_F0~14			
	GPP_F15			
	GPP_F16			
	GPP_F17			
	GPP_F18			
	GPP_F19			EDP_VDD_EN
	GPP_F20			EDP_BKLT_EN
	GPP_F21			EDP_BKLT_CTRL
	GPP_F22~23			
Group G	GPP_G0~23			
Group H	GPP_H0~23			CLK_PCIE6_X16.REQ#
Group I	GPP_I0			DPB_HPD
	GPP_I1			DPC_HPD
	GPP_I2			DPD_HPD
	GPP_I3			
	GPP_I4			EDP_HPD
	GPP_I5			DPB_CTRLCLK
	GPP_I6			DPB_CTRLDATA
	GPP_I7			DPC_CTRLCLK
	GPP_I8			DPC_CTRLDATA
	GPP_I9			DPD_CTRLCLK
	GPP_I10			DPD_CTRLDATA

PM_LAN1PHY_ENABLE

DRAMRST_CNTRL_PCH

F81966D GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO00	5V	I_VSB3V	Native	ERP_CTRL0#
GPIO01	5V	I_VSB3V	Native	ERP_CTRL1#
GPIO02	5V	I_VSB3V	Native	PM_SUS_WARN#
GPIO03	5V	I_VSB3V	Native	PM_SUS_ACK#
GPIO04	5V	I_VSB3V	Native	PM_SLP_SUS#
GPIO05	5V	I_VSB3V	Native	TX5#
GPIO06	5V	I_VSB3V	Native	RX5#
GPIO07	5V	I_VSB3V	Native	RTS5#
GPIO10	5V	I_VSB3V	Native	AUDIO_MUTE#
GPIO11	5V	I_VSB3V	Native	EN_USB
GPIO12	5V	I_VSB3V	Native	LAN2_DISABLE#
GPIO13	5V	I_VSB3V	Native	W_DISABLE0#
GPIO14	5V	I_VSB3V	Native	ATX_AT_TRAP
GPIO15	5V	I_VSB3V	Native	WDT_RST#
GPIO16	5V	I_VSB3V	Native	SML1_DATA
GPIO17	5V	I_VSB3V	Native	SIO_PECI
GPIO20	5V	I_VSB3V	Native	SML1_CLK
GPIO21	5V	I_VSB3V	Native	SIO_ATXPG
GPIO22	5V	I_VSB3V	Native	EXT_PWRBTN#
GPIO23	5V	I_VSB3V	Native	PM_PWRBTN#
GPIO24	5V	I_VSB3V	Native	PM_SLP_S3#
GPIO25	5V	I_VSB3V	Native	PSON#
GPIO26	5V	VBAT	Native	PWOK
GPIO27	5V	VBAT	Native	SIO_RSMRST#
GPIO30	5V	3VCC	Native	DCD3#
GPIO31	5V	3VCC	Native	RI3#
GPIO32	5V	3VCC	Native	CTS3#
GPIO33	5V	3VCC	Native	DTR3#
GPIO34	5V	3VCC	Native	RTS3#
GPIO35	5V	3VCC	Native	DSR3#
GPIO36	5V	3VCC	Native	TX3#
GPIO37	5V	3VCC	Native	RX3#
GPIO40	5V	3VCC	Native	DCD4#
GPIO41	5V	3VCC	Native	RI4#
GPIO42	5V	3VCC	Native	CTS4#
GPIO43	5V	3VCC	Native	DTR4#
GPIO44	5V	3VCC	Native	RTS4#
GPIO45	5V	3VCC	Native	DSR4#
GPIO46	5V	3VCC	Native	TX4#
GPIO47	5V	3VCC	Native	RX4#
GPIO50	5V	3VCC	Native	RTS6#
GPIO51	5V	3VCC	Native	RX6#
GPIO52	5V	3VCC	Native	TX6#
GPIO53	5V	3VCC	Native	DCD6#
GPIO54	5V	3VCC	Native	RI6#
GPIO55	5V	3VCC	Native	CTS6#
GPIO56	5V	3VCC	Native	DTR6#
GPIO57	5V	3VCC	Native	DSR6#
GPIO60	5V	3VCC	Native	DCD5#
GPIO61	5V	3VCC	Native	RI5#
GPIO62	5V	3VCC	Native	CTS5#
GPIO63	5V	3VCC	Native	DTR5#
GPIO64	5V	3VCC	Native	DSR5#
GPIO65	5V	I_VSB3V	Native	LPC_PME#
GPIO66	5V	VBAT	Native	DPWROK
GPIO67	5V	I_VSB3V	Native	PM_SLP_S5#
GPIO70	5V	3VCC	Native	PE
GPIO71	5V	3VCC	Native	BUSY
GPIO72	5V	3VCC	Native	ACK#
GPIO73	5V	3VCC	Native	SLIN#
GPIO74	5V	3VCC	Native	PINIT#
GPIO75	5V	3VCC	Native	ERR#
GPIO76	5V	3VCC	Native	AFD#
GPIO77	5V	3VCC	Native	STB#
GPIO80	5V	3VCC	Native	PD0
GPIO81	5V	3VCC	Native	PD1
GPIO82	5V	3VCC	Native	PD2
GPIO83	5V	3VCC	Native	PD3
GPIO84	5V	3VCC	Native	PD4
GPIO85	5V	3VCC	Native	PD5
GPIO86	5V	3VCC	Native	PD6
GPIO87	5V	3VCC	Native	PD7

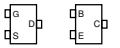
F75111RG GPIO Pins :

Name	Tolerance	Power Well	Default	Function
GPIO10	5V	VSB3V	Native	CH7517_RST#
GPIO11	5V	VSB3V	Native	LVDS_PD#
GPIO12	5V	VSB3V	Native	LVDS_EN
GPIO13	5V	VSB3V	Native	
GPIO14	5V	VSB3V	Native	LVDS2_PD#
GPIO15	5V	VSB3V	Native	LVDS2_EN
GPIO16	5V	VSB3V	Native	LVDS_RBIT0
GPIO17	5V	VSB3V	Native	LVDS_RBIT1
GPIO20	5V	VSB3V	Native	SEL_COM2_MD0
GPIO21	5V	VSB3V	Native	SEL_COM2_MD1
GPIO22	5V	VSB3V	Native	COM2_SLEW
GPIO23	5V	VSB3V	Native	SEL_COM6_MD0
GPIO24	5V	VSB3V	Native	SEL_COM6_MD1
GPIO25	5V	VSB3V	Native	COM6_SLEW
GPIO26	5V	VSB3V	Native	81438_SD
GPIO27	5V	VSB3V	Native	ADM213_EN
GPIO30	5V	VSB3V	GPIO	BoardID_BIT0
GPIO31	5V	VSB3V	GPIO	BoardID_BIT1
GPIO32	5V	VSB3V	GPIO	BoardID_BIT2
GPIO33	5V	VSB3V	GPIO	LVDS_RBIT2

SMBus/I2C Addresses :

Device	Address
SODIMMA	A0h
SODIMMB	A4h
Lewisville	C8h
LCD Backlight Contoller 1	5Ch
LCD Backlight Contoller 2	2Eh
CMOS Backup EEPROM	AEh
GPIO IC	6Eh

PCB Footprints



PCB STACK :

Impedence 55ohm +/-15%.

- Layer 1 : Component
- Layer 2 : GND
- Layer 3 : Signal
- Layer 4 : Signal
- Layer 5 : POWER
- Layer 6 : Signal
- Layer 7 : GND
- Layer 8 : Solder

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Title: System Setting

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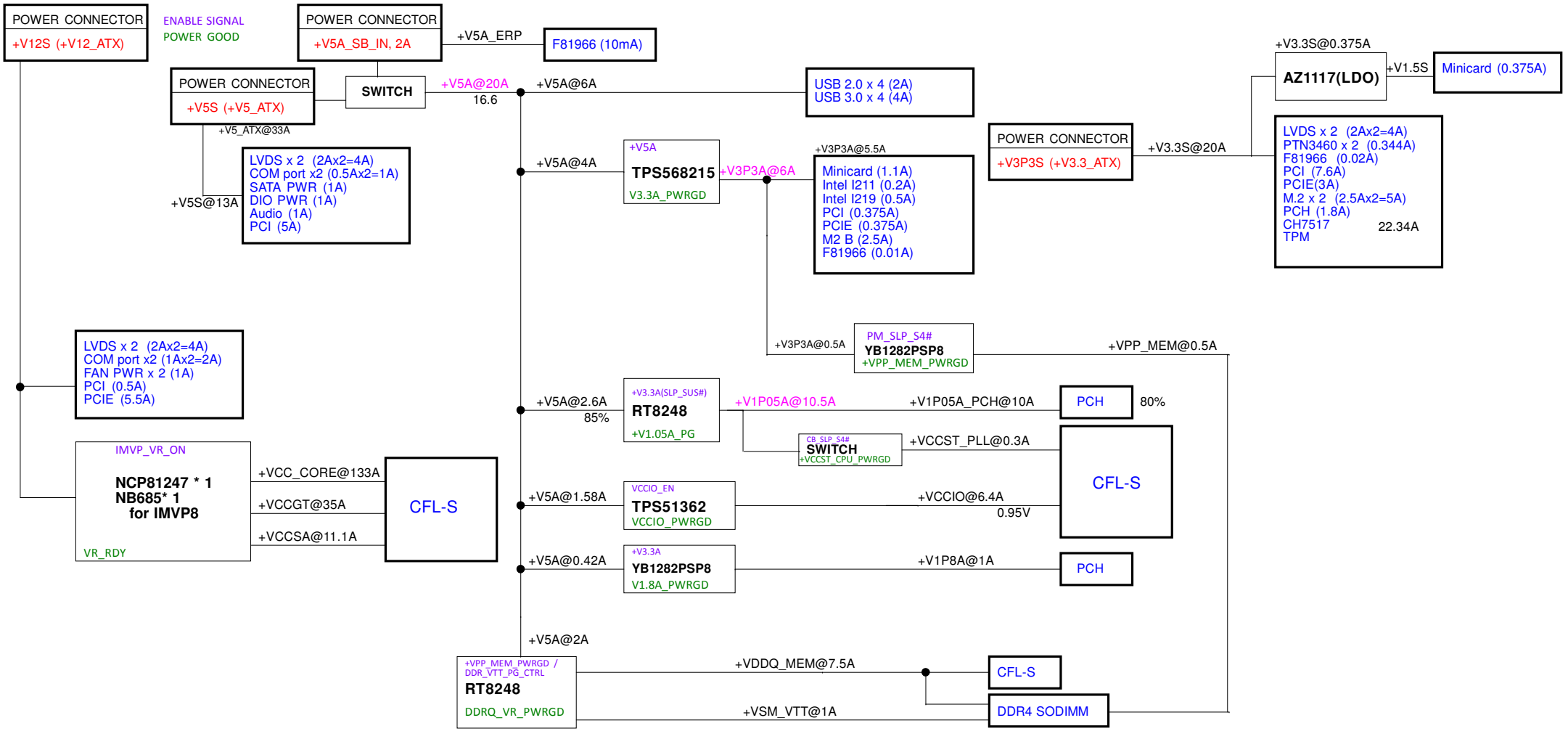

AAEON An ASUS Company	Title: POWER MAP	
	Size: Custom; Document Number: PCM-CFS	Rev: A0.2
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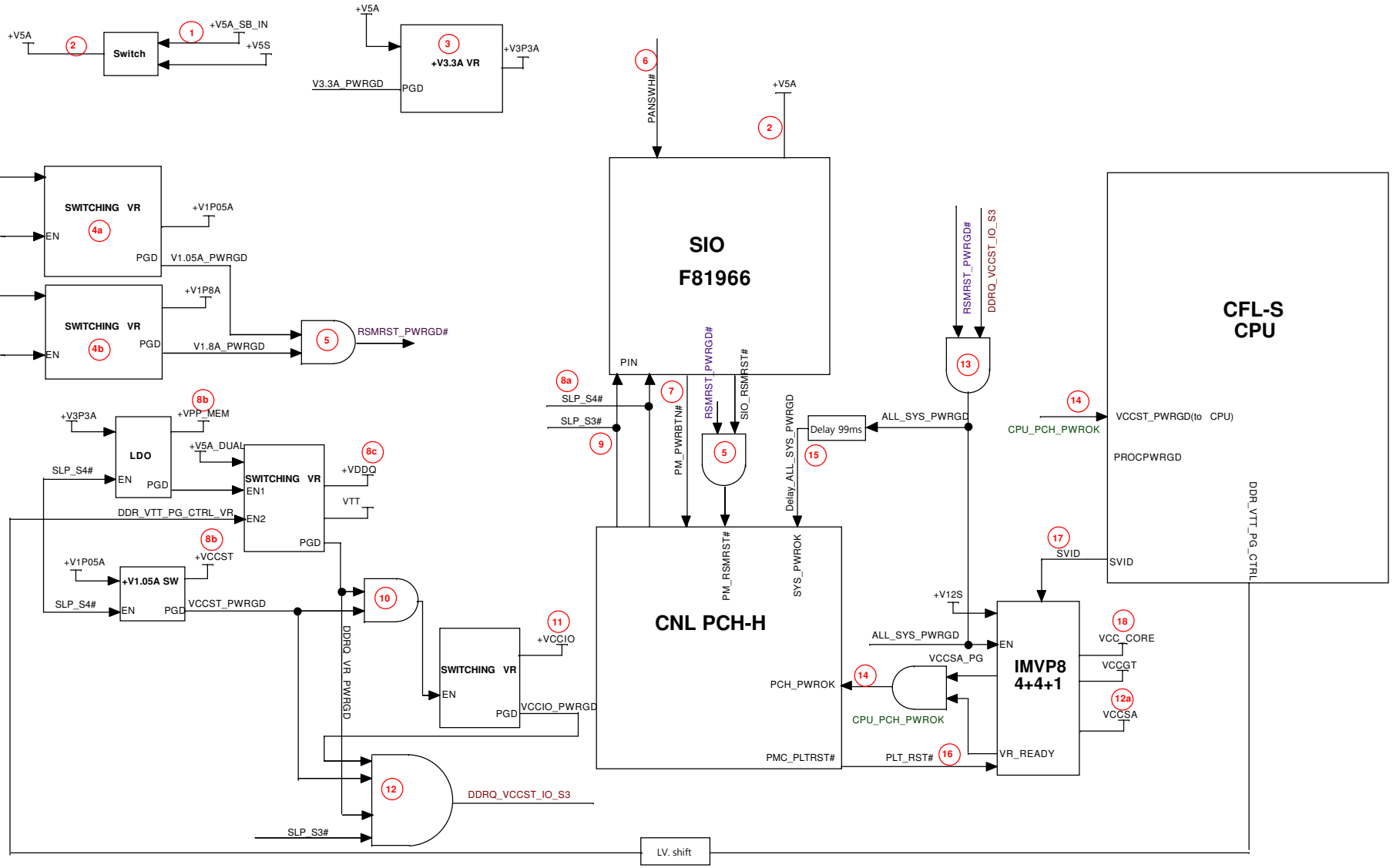

AAEON An ASUS Company	Title: Power Sequence		
	Size: Custom	Document Number: PCM-CFS	Rev: A0.2
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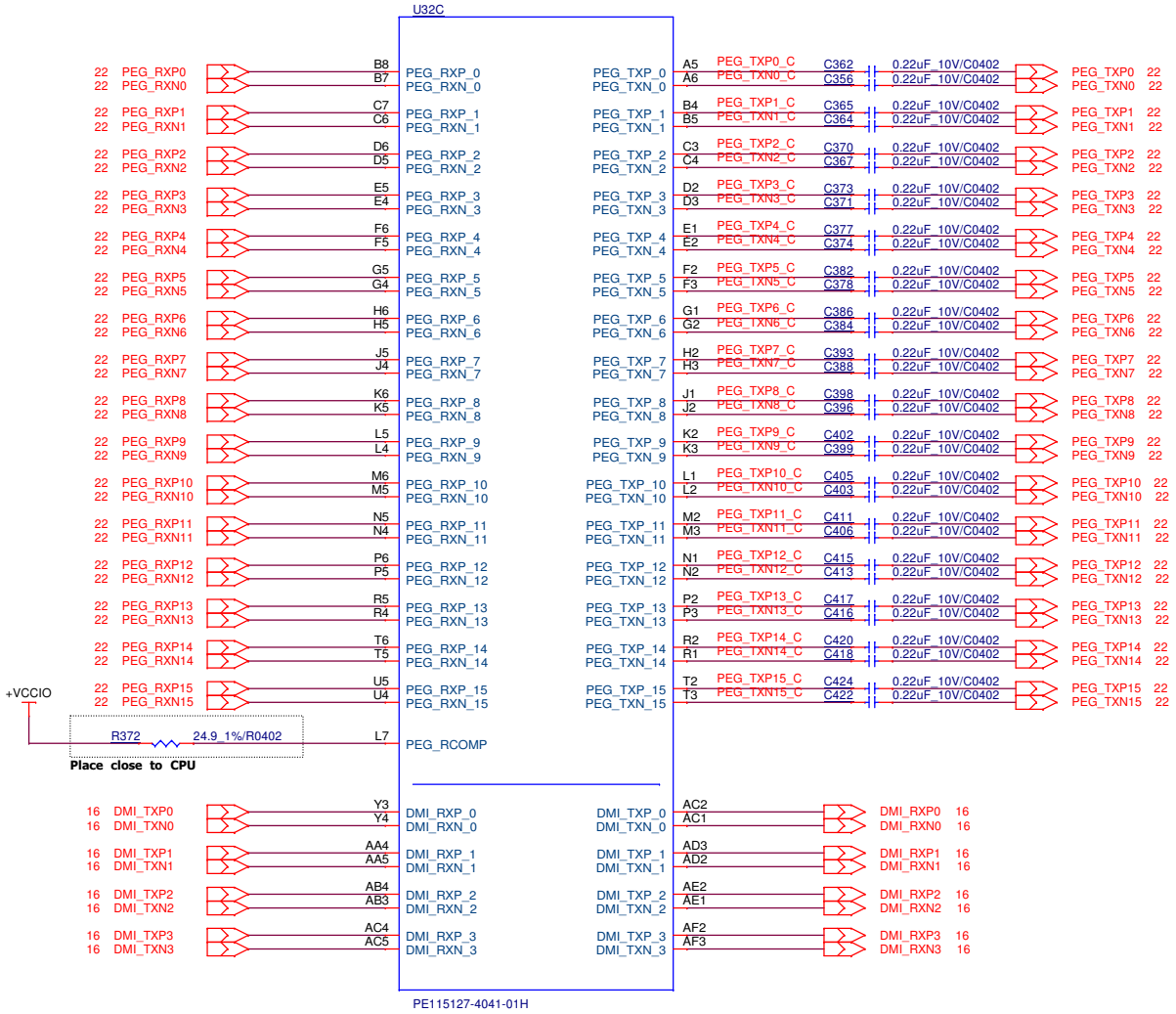

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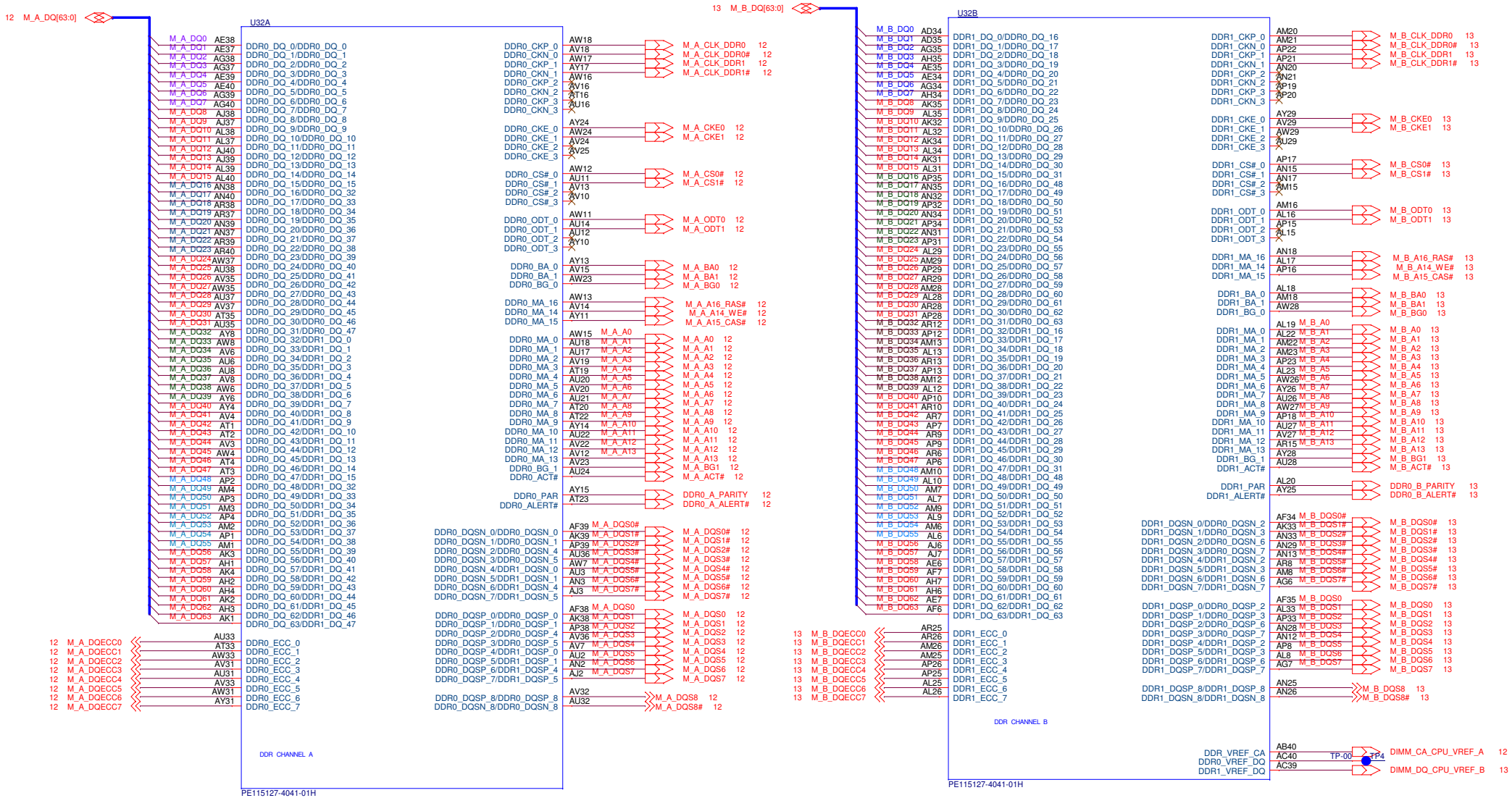
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DDR0_DQ_0/DDR0_DQ_0
DDR0_DQ_1/DDR0_DQ_1
DDR0_DQ_2/DDR0_DQ_2
DDR0_DQ_3/DDR0_DQ_3
DDR0_DQ_4/DDR0_DQ_4
DDR0_DQ_5/DDR0_DQ_5
DDR0_DQ_6/DDR0_DQ_6
DDR0_DQ_7/DDR0_DQ_7
DDR0_DQ_8/DDR0_DQ_8
DDR0_DQ_9/DDR0_DQ_9
DDR0_DQ_10/DDR0_DQ_10
DDR0_DQ_11/DDR0_DQ_11
DDR0_DQ_12/DDR0_DQ_12
DDR0_DQ_13/DDR0_DQ_13
DDR0_DQ_14/DDR0_DQ_14
DDR0_DQ_15/DDR0_DQ_15
DDR0_DQ_16/DDR0_DQ_32
DDR0_DQ_17/DDR0_DQ_33
DDR0_DQ_18/DDR0_DQ_34
DDR0_DQ_19/DDR0_DQ_35
DDR0_DQ_20/DDR0_DQ_36
DDR0_DQ_21/DDR0_DQ_37
DDR0_DQ_22/DDR0_DQ_38
DDR0_DQ_23/DDR0_DQ_39
DDR0_DQ_24/DDR0_DQ_40
DDR0_DQ_25/DDR0_DQ_41
DDR0_DQ_26/DDR0_DQ_42
DDR0_DQ_27/DDR0_DQ_43
DDR0_DQ_28/DDR0_DQ_44
DDR0_DQ_29/DDR0_DQ_45
DDR0_DQ_30/DDR0_DQ_46
DDR0_DQ_31/DDR0_DQ_47
DDR0_DQ_32/DDR1_DQ_0
DDR0_DQ_33/DDR1_DQ_1
DDR0_DQ_34/DDR1_DQ_2
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DDR0_DQ_36/DDR1_DQ_4
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DDR0_DQ_40/DDR1_DQ_8
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DDR0_DQ_55/DDR1_DQ_39
DDR0_DQ_56/DDR1_DQ_40
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DDR0_ECC_2
DDR0_ECC_3
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DDR0_ECC_6
DDR0_ECC_7
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DDR0_CKN_0
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DDR0_CKN_2
DDR0_CKP_3
DDR0_CKN_3
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DDR0_CKE_1
DDR0_CKE_2
DDR0_CKE_3
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DDR0_CS#_1
DDR0_CS#_2
DDR0_CS#_3
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DDR0_ODT_1
DDR0_ODT_2
DDR0_ODT_3
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DDR0_BA_1
DDR0_BG_0
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DDR0_MA_1
DDR0_MA_2
DDR0_MA_3
DDR0_MA_4
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DDR0_PAR
DDR0_ALERT#
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12 M_A_DQECC5
12 M_A_DQECC6
12 M_A_DQECC7
DDR CHANNEL A
PE115127-4041-01H
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DDR1_DQ_1/DDR0_DQ_17
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DDR1_DQ_3/DDR0_DQ_19
DDR1_DQ_4/DDR0_DQ_20
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DDR1_DQ_46/DDR1_DQ_30
DDR1_DQ_47/DDR1_DQ_31
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DDR1_ECC_1
DDR1_ECC_2
DDR1_ECC_3
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DDR1_ECC_7
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DDR1_CKN_0
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DDR1_CKN_1
DDR1_CKP_2
DDR1_CKN_2
DDR1_CKP_3
DDR1_CKN_3
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DDR1_MA_14
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DDR1_BA_1
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DDR1_MA_9
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DDR1_MA_12
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DDR1_PAR
DDR1_ALERT#
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13 M_B_DQECC5
13 M_B_DQECC6
13 M_B_DQECC7
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DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
TP-00
TP4
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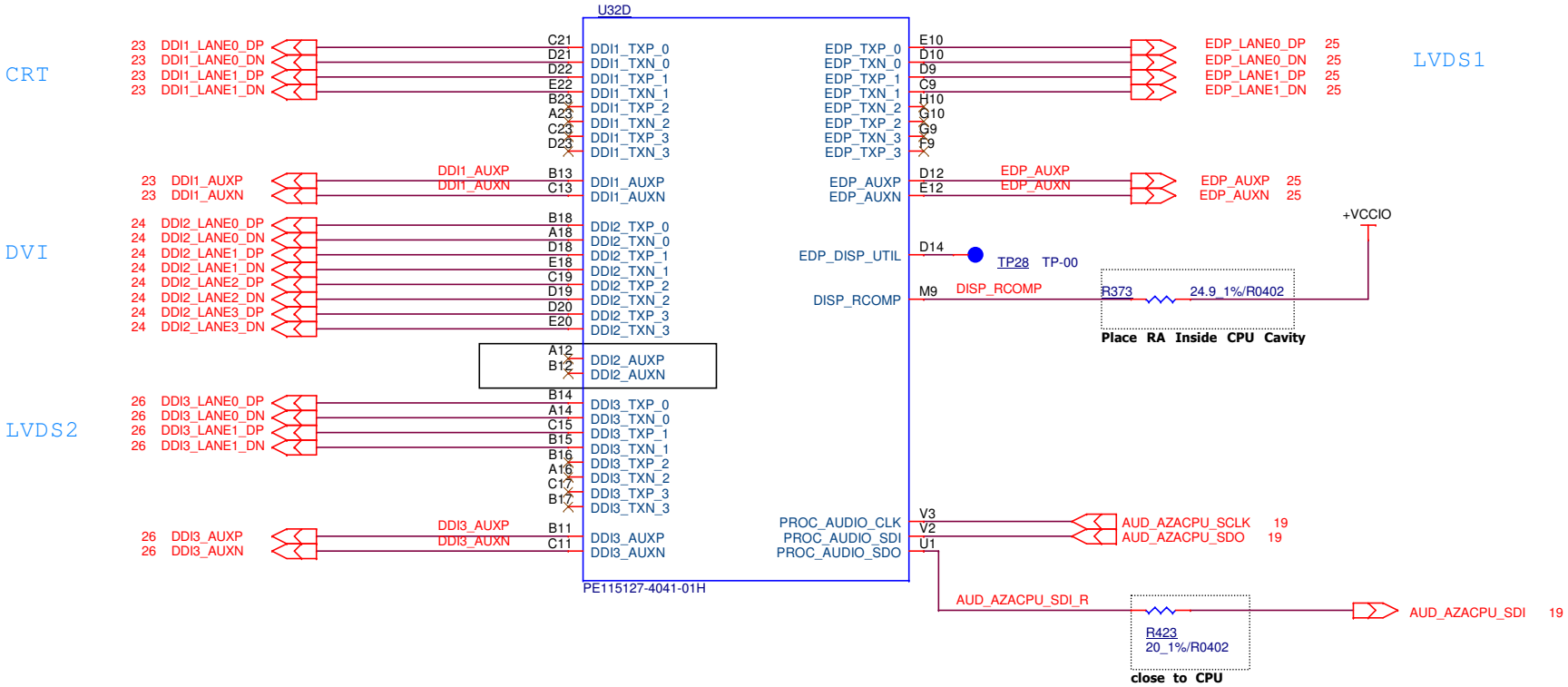

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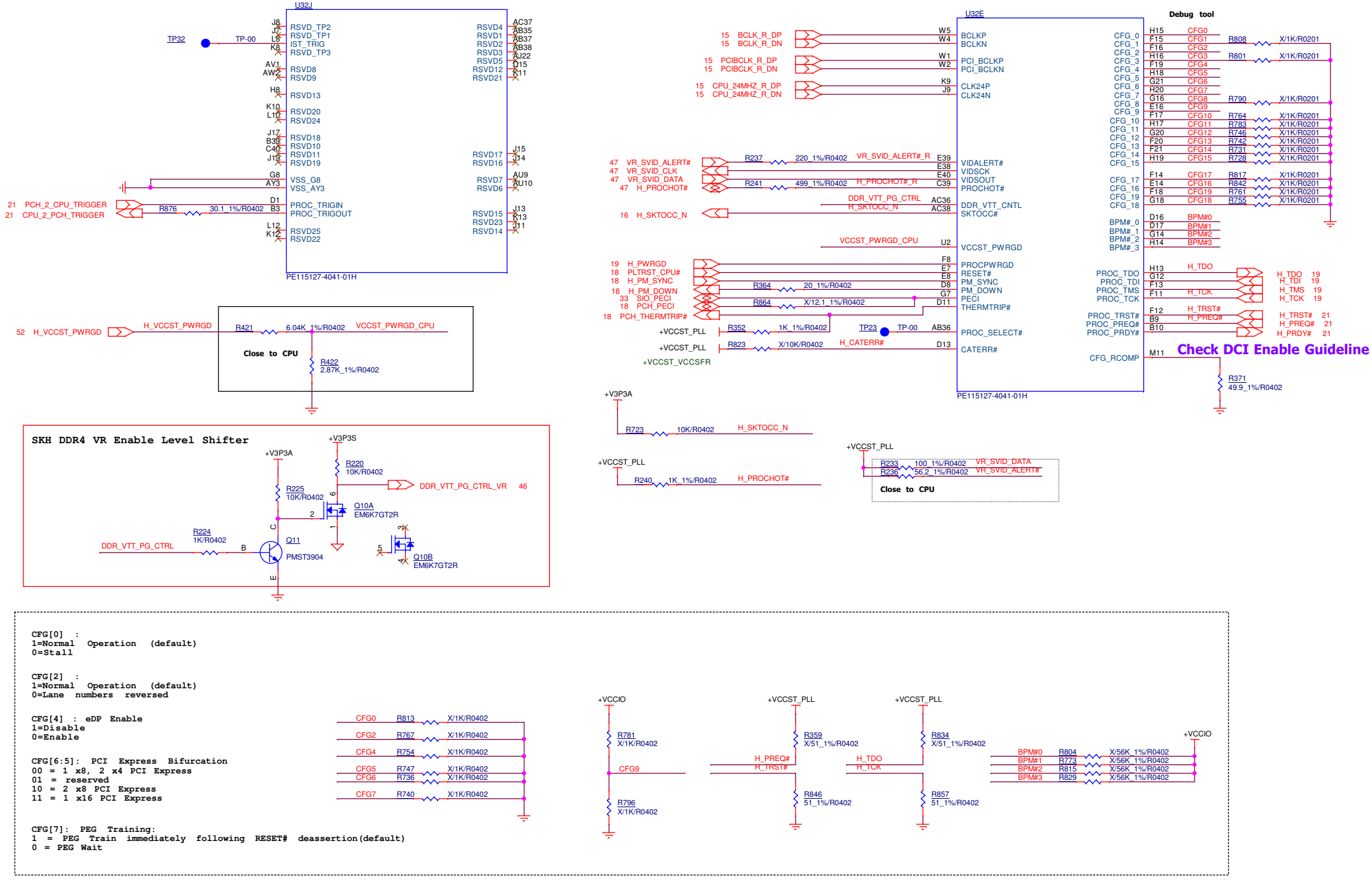

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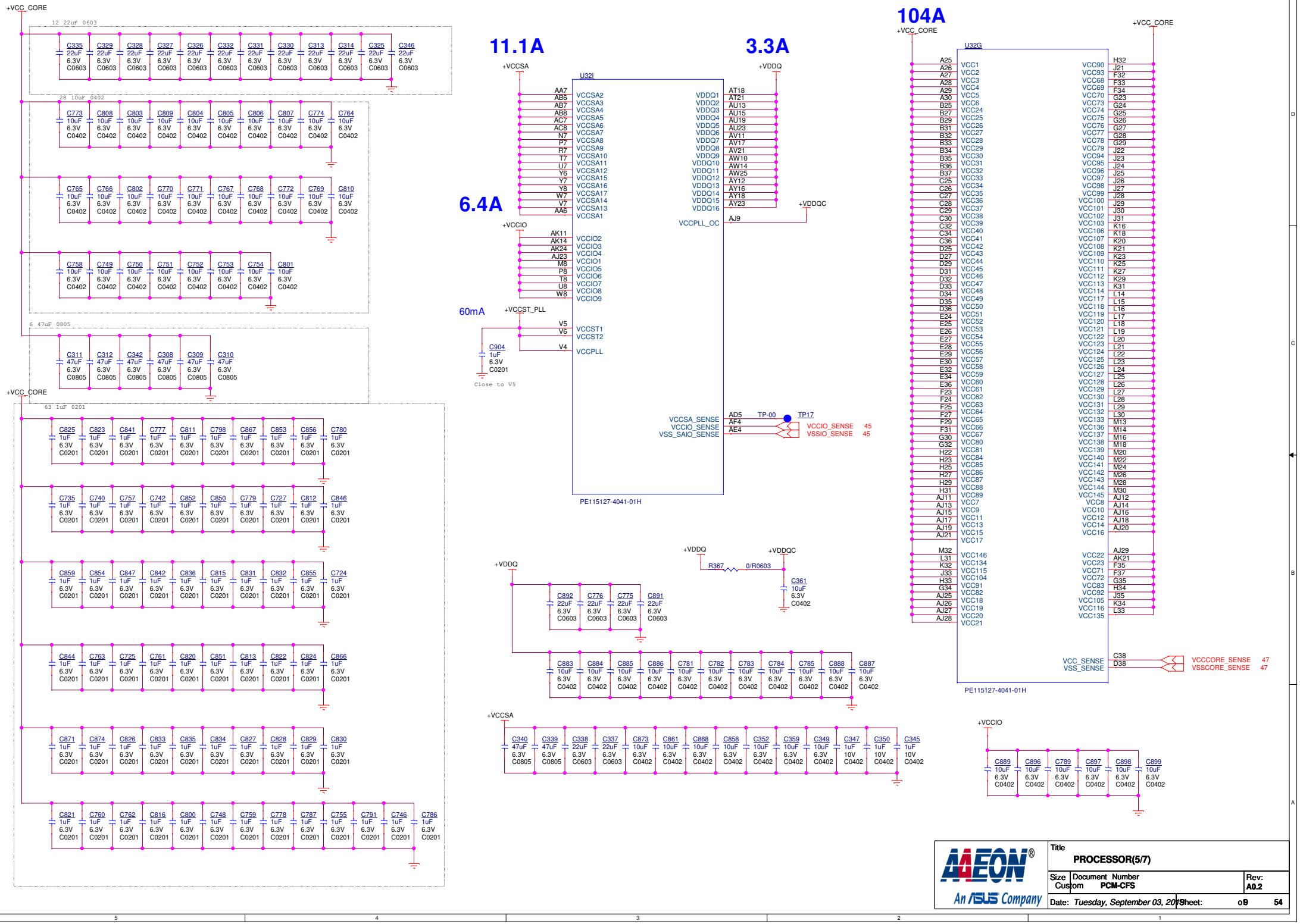
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C335 22uF 6.3V C0603
C329 22uF 6.3V C0603
C328 22uF 6.3V C0603
C327 22uF 6.3V C0603
C326 22uF 6.3V C0603
C332 22uF 6.3V C0603
C331 22uF 6.3V C0603
C330 22uF 6.3V C0603
C313 22uF 6.3V C0603
C314 22uF 6.3V C0603
C325 22uF 6.3V C0603
C346 22uF 6.3V C0603
28 10uF 0402
C773 10uF 6.3V C0402
C808 10uF 6.3V C0402
C803 10uF 6.3V C0402
C809 10uF 6.3V C0402
C804 10uF 6.3V C0402
C805 10uF 6.3V C0402
C806 10uF 6.3V C0402
C807 10uF 6.3V C0402
C774 10uF 6.3V C0402
C764 10uF 6.3V C0402
C765 10uF 6.3V C0402
C766 10uF 6.3V C0402
C802 10uF 6.3V C0402
C770 10uF 6.3V C0402
C771 10uF 6.3V C0402
C767 10uF 6.3V C0402
C768 10uF 6.3V C0402
C772 10uF 6.3V C0402
C769 10uF 6.3V C0402
C810 10uF 6.3V C0402
C758 10uF 6.3V C0402
C749 10uF 6.3V C0402
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C753 10uF 6.3V C0402
C754 10uF 6.3V C0402
C801 10uF 6.3V C0402
6 47uF 0805
C311 47uF 6.3V C0805
C312 47uF 6.3V C0805
C342 47uF 6.3V C0805
C308 47uF 6.3V C0805
C309 47uF 6.3V C0805
C310 47uF 6.3V C0805
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C825 1uF 6.3V C0201
C823 1uF 6.3V C0201
C841 1uF 6.3V C0201
C777 1uF 6.3V C0201
C811 1uF 6.3V C0201
C798 1uF 6.3V C0201
C867 1uF 6.3V C0201
C853 1uF 6.3V C0201
C856 1uF 6.3V C0201
C780 1uF 6.3V C0201
C735 1uF 6.3V C0201
C740 1uF 6.3V C0201
C757 1uF 6.3V C0201
C742 1uF 6.3V C0201
C852 1uF 6.3V C0201
C850 1uF 6.3V C0201
C779 1uF 6.3V C0201
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C854 1uF 6.3V C0201
C847 1uF 6.3V C0201
C842 1uF 6.3V C0201
C836 1uF 6.3V C0201
C815 1uF 6.3V C0201
C831 1uF 6.3V C0201
C832 1uF 6.3V C0201
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C724 1uF 6.3V C0201
C844 1uF 6.3V C0201
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C725 1uF 6.3V C0201
C761 1uF 6.3V C0201
C820 1uF 6.3V C0201
C851 1uF 6.3V C0201
C813 1uF 6.3V C0201
C822 1uF 6.3V C0201
C824 1uF 6.3V C0201
C866 1uF 6.3V C0201
C871 1uF 6.3V C0201
C874 1uF 6.3V C0201
C826 1uF 6.3V C0201
C833 1uF 6.3V C0201
C835 1uF 6.3V C0201
C834 1uF 6.3V C0201
C827 1uF 6.3V C0201
C828 1uF 6.3V C0201
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C830 1uF 6.3V C0201
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C759 1uF 6.3V C0201
C778 1uF 6.3V C0201
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C755 1uF 6.3V C0201
C791 1uF 6.3V C0201
C746 1uF 6.3V C0201
C786 1uF 6.3V C0201
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+VCCSA
U32I
AA7 VCCSA2
AB6 VCCSA3
AB7 VCCSA4
AB8 VCCSA5
AC7 VCCSA6
AC8 VCCSA7
N7 VCCSA8
P7 VCCSA9
R7 VCCSA10
T7 VCCSA11
U7 VCCSA12
Y6 VCCSA15
Y7 VCCSA16
Y8 VCCSA17
W7 VCCSA14
V7 VCCSA13
AA6 VCCSA1
3.3A
+VDDQ
VDDQ1 AT18
VDDQ2 AT21
VDDQ3 AU13
VDDQ4 AU15
VDDQ5 AU19
VDDQ6 AU23
VDDQ7 AV11
VDDQ8 AV17
VDDQ9 AV21
VDDQ10 AW10
VDDQ11 AW14
VDDQ12 AW25
VDDQ13 AY12
VDDQ14 AY16
VDDQ15 AY18
VDDQ16 AY23
VCCPLL_OC AJ9
+VDDQC
6.4A
+VCCIO
AK11 VCCIO2
AK14 VCCIO3
AK24 VCCIO4
AJ23 VCCIO1
M8 VCCIO5
P8 VCCIO6
T8 VCCIO7
U8 VCCIO8
W8 VCCIO9
60mA
+VCCST_PLL
V5 VCCST1
V6 VCCST2
V4 VCCPLL
C904 1uF 6.3V C0201
Close to V5
PE115127-4041-01H
VCCSA_SENSE AD5
VCCIO_SENSE AF4
VSS_SAIO_SENSE AE4
TP-00
TP17
VCCIO_SENSE 45
VSSIO_SENSE 45
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+VDDQC
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C776 22uF 6.3V C0603
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C891 22uF 6.3V C0603
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A27 VCC3
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A29 VCC5
A30 VCC6
B25 VCC24
B27 VCC25
B29 VCC26
B31 VCC27
B32 VCC28
B33 VCC29
B34 VCC30
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B36 VCC32
B37 VCC33
C25 VCC34
C26 VCC35
C27 VCC36
C28 VCC37
C29 VCC38
C30 VCC39
C32 VCC40
C34 VCC41
C36 VCC42
D25 VCC43
D27 VCC44
D29 VCC45
D31 VCC46
D32 VCC47
D33 VCC48
D34 VCC49
D35 VCC50
D36 VCC51
E24 VCC52
E25 VCC53
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E27 VCC55
E28 VCC56
E29 VCC57
E30 VCC58
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E34 VCC60
E36 VCC61
F23 VCC62
F24 VCC63
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F29 VCC66
F31 VCC67
G30 VCC80
G32 VCC81
H22 VCC84
H23 VCC85
H25 VCC86
H27 VCC87
H29 VCC88
H31 VCC89
AJ11 VCC7
AJ13 VCC9
AJ15 VCC11
AJ17 VCC13
AJ19 VCC15
AJ21 VCC17
M32 VCC146
L31 VCC134
K32 VCC115
J33 VCC104
H33 VCC91
G34 VCC82
AJ25 VCC18
AJ26 VCC19
AJ27 VCC20
AJ28 VCC21
H32 VCC90
J21 VCC93
F32 VCC68
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G26 VCC76
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M16 VCC138
M18 VCC139
M20 VCC140
M22 VCC141
M24 VCC142
M26 VCC143
M28 VCC144
M30 VCC145
AJ12 VCC8
AJ14 VCC10
AJ16 VCC12
AJ18 VCC14
AJ20 VCC16
AJ29 VCC22
AK21 VCC23
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H34 VCC92
J35 VCC105
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L33 VCC135
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VSS_SENSE D38
VCCCORE_SENSE 47
VSSCORE_SENSE 47
+VCCIO
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C896 10uF 6.3V C0402
C789 10uF 6.3V C0402
C897 10uF 6.3V C0402
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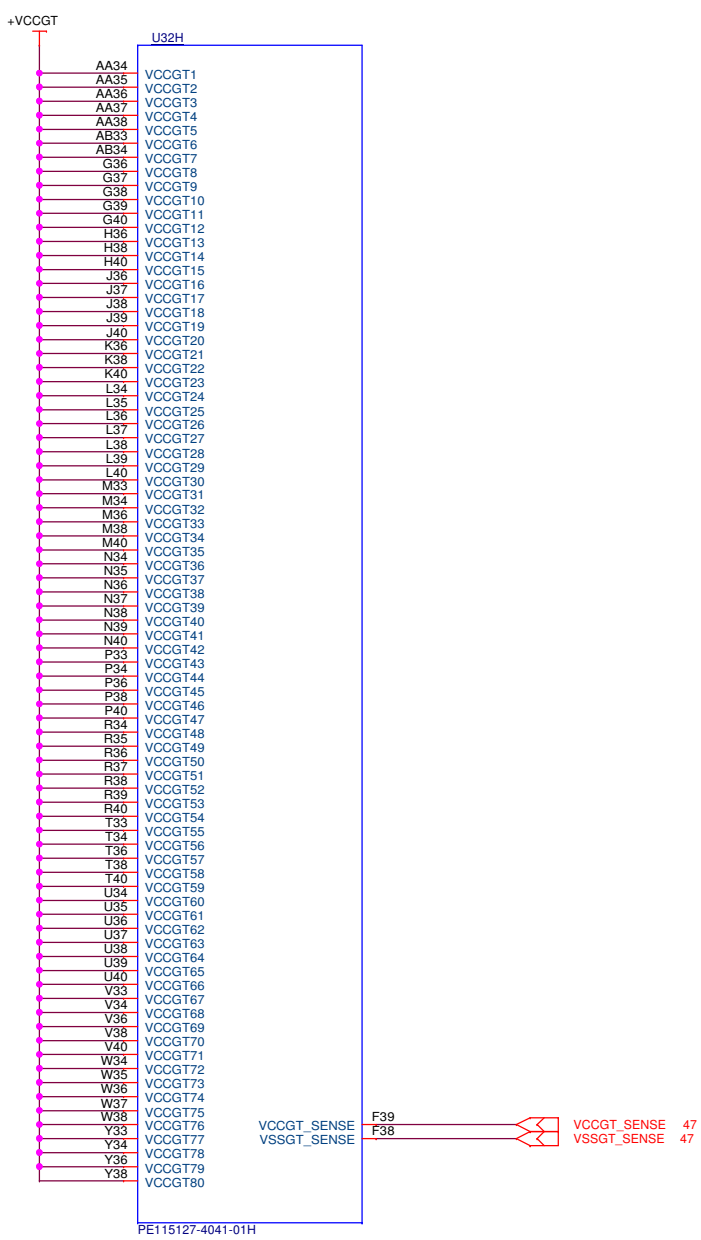

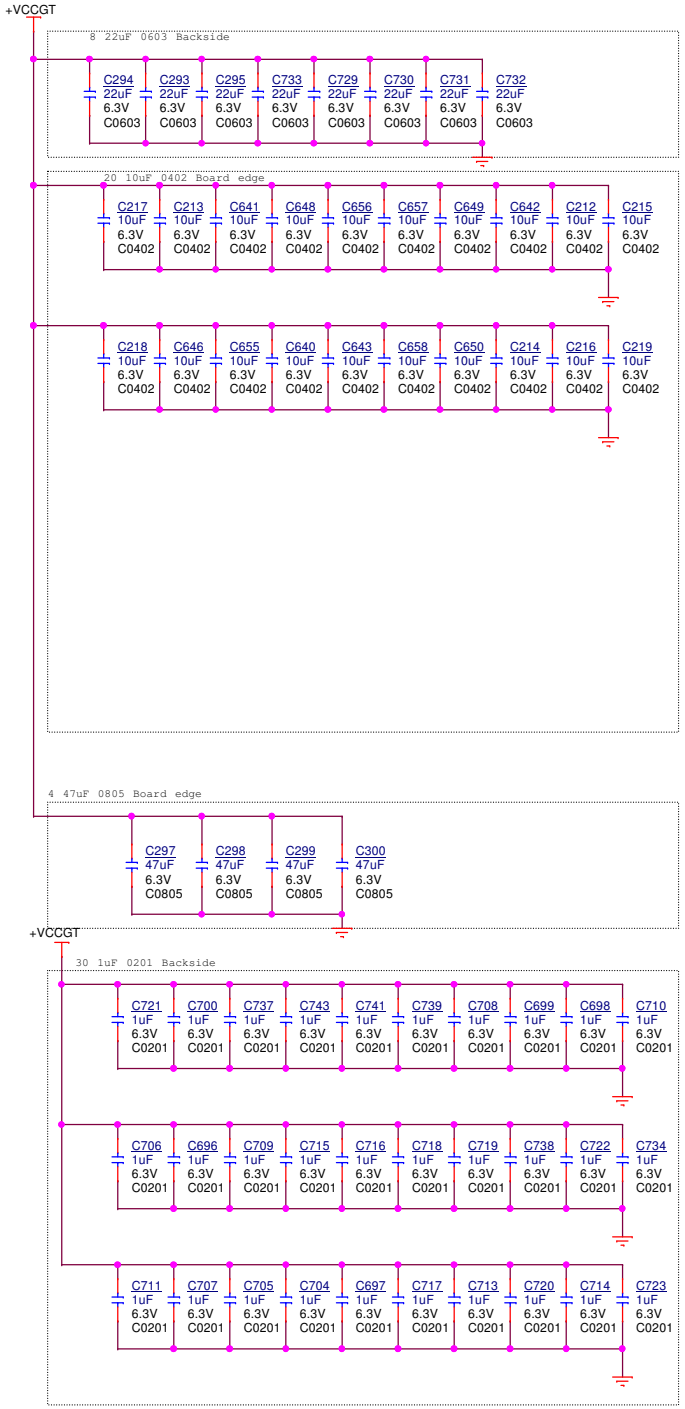

. Decoupling Requirements for CFL H Proce

Domain	Board Edge cap	Backside cap
Vcc	5x 47uF 0805	
		12x 22uF 0603
		21x 10uF 0402
		24x 1uF 0201
		24x 0201 (placeholder)
Vcc_{GT}	3x 47uF 0805	
	7x 22uF 0603	
		10x 10uF 0402
		12x 1uF 0201
Vcc_{SA}	2x 47uF 0805	
	2x 22uF 0603	
		7x 10uF 0402
		1x 1uF 0201

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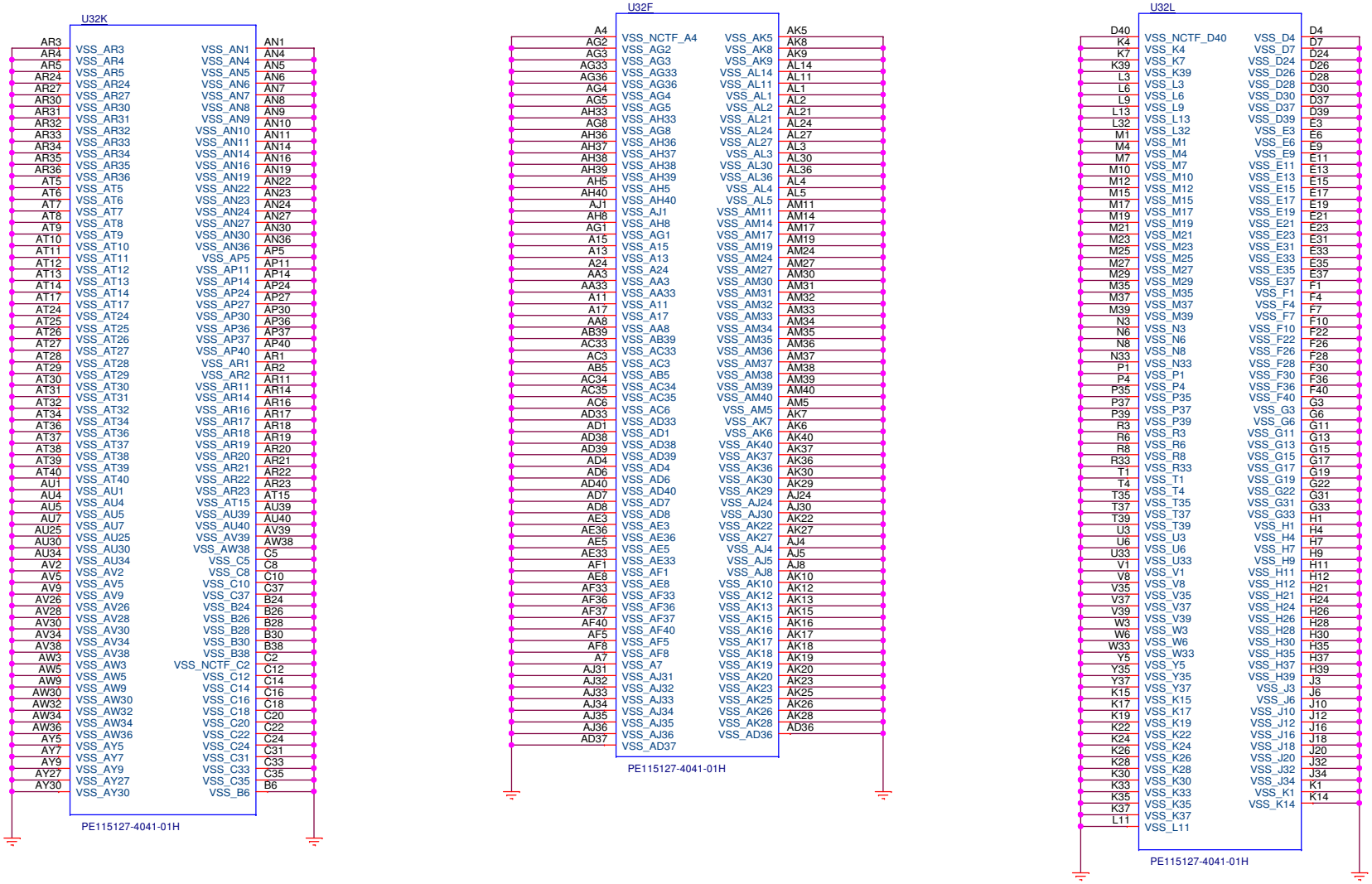

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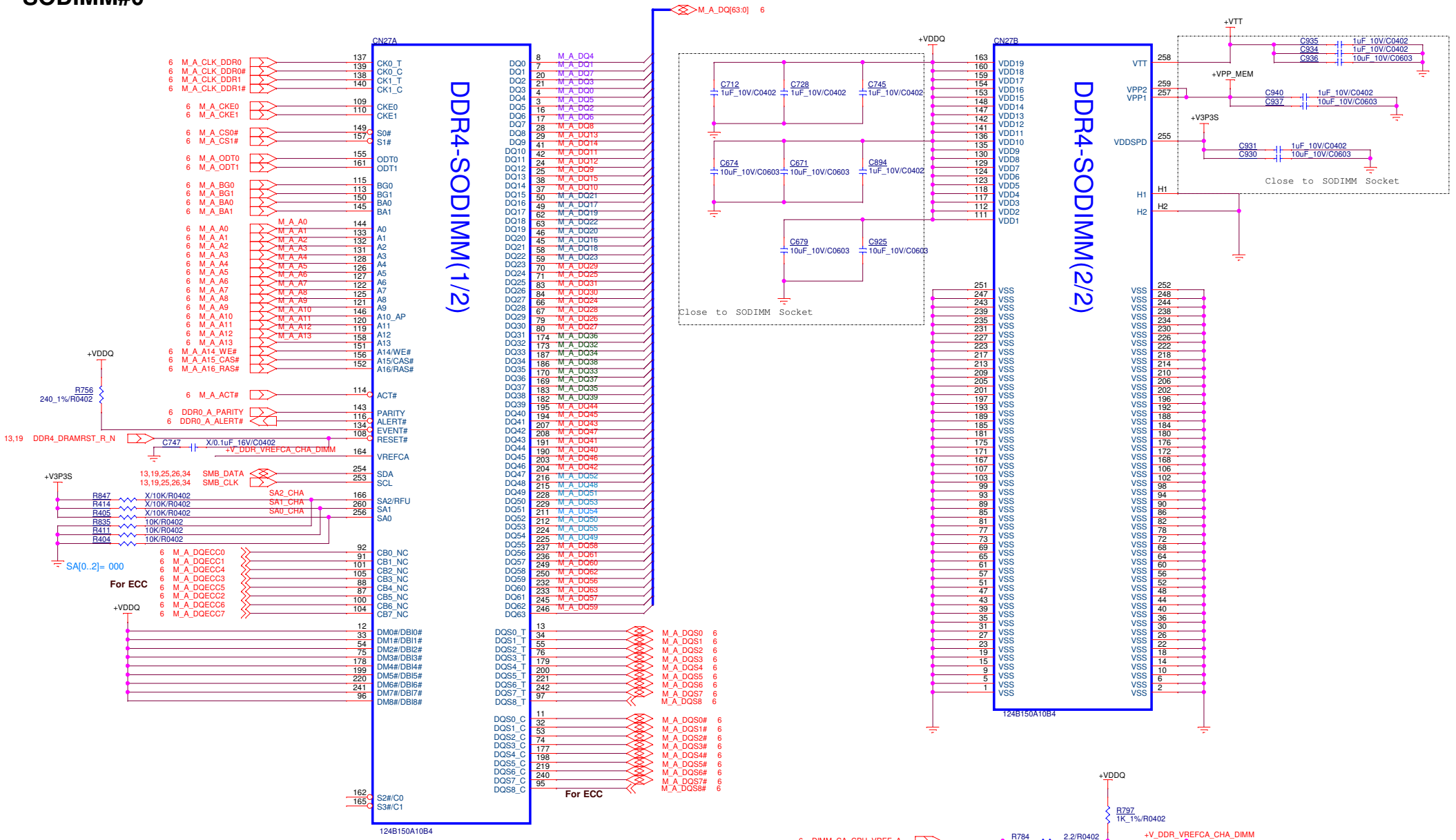

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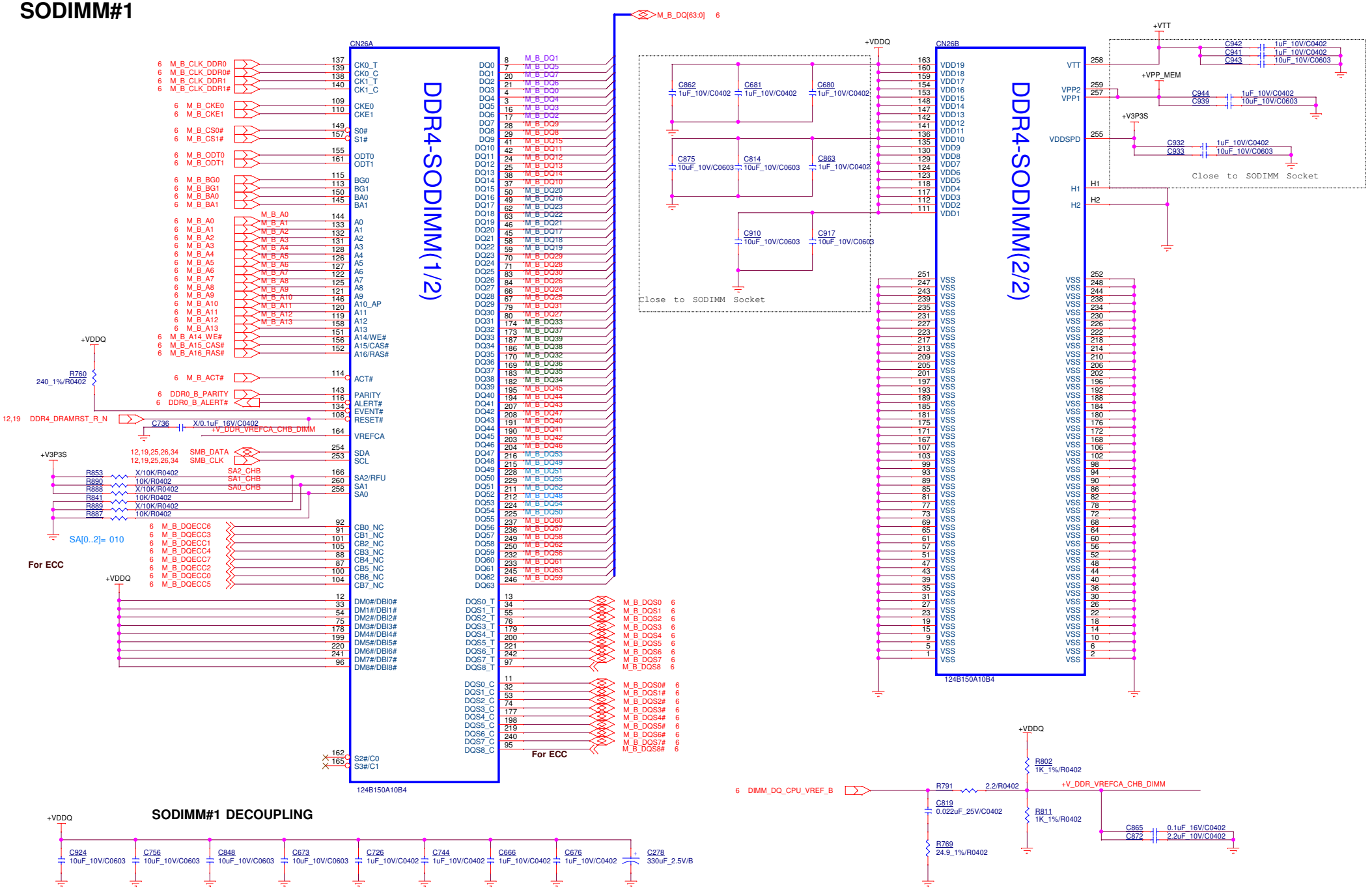

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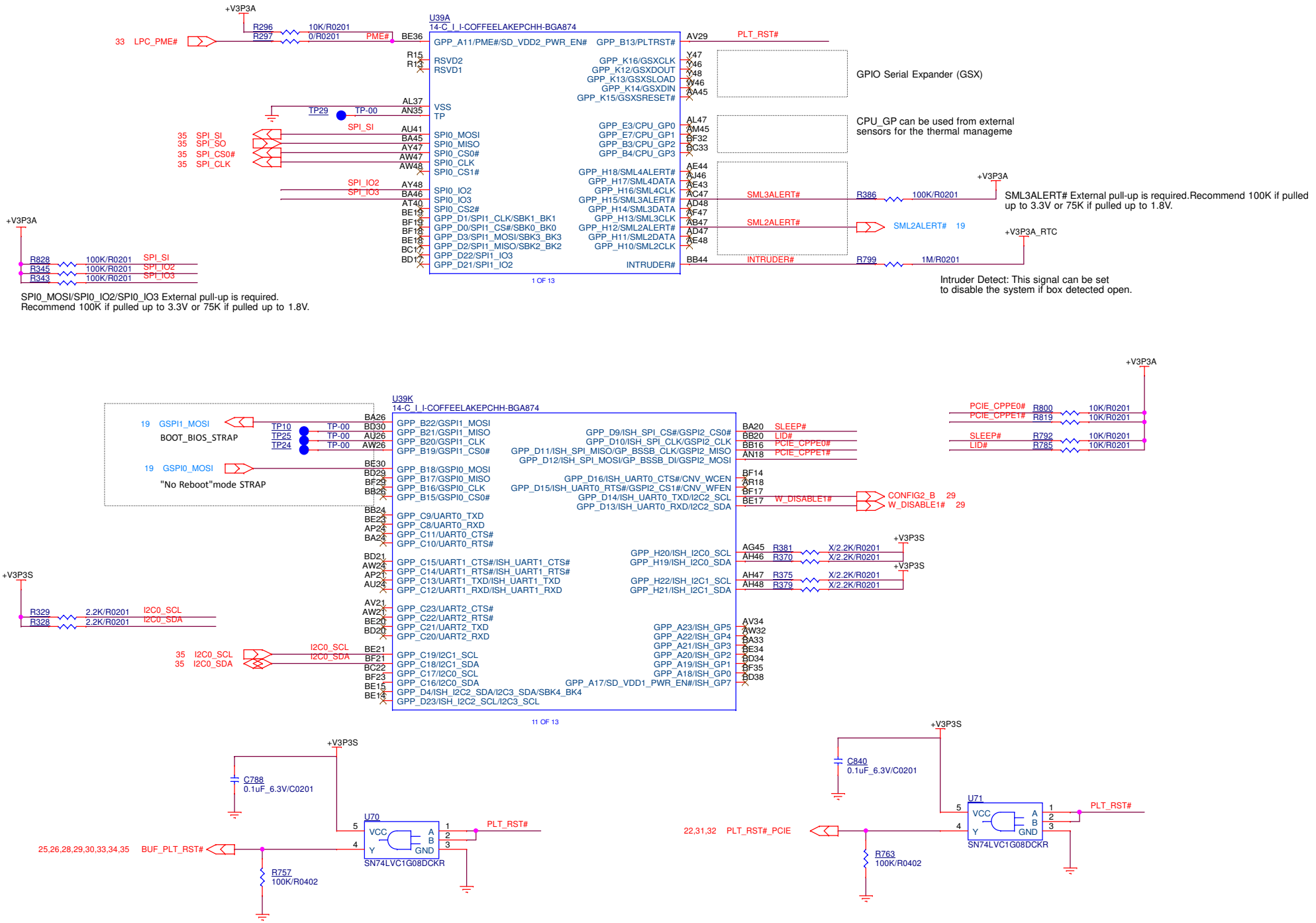

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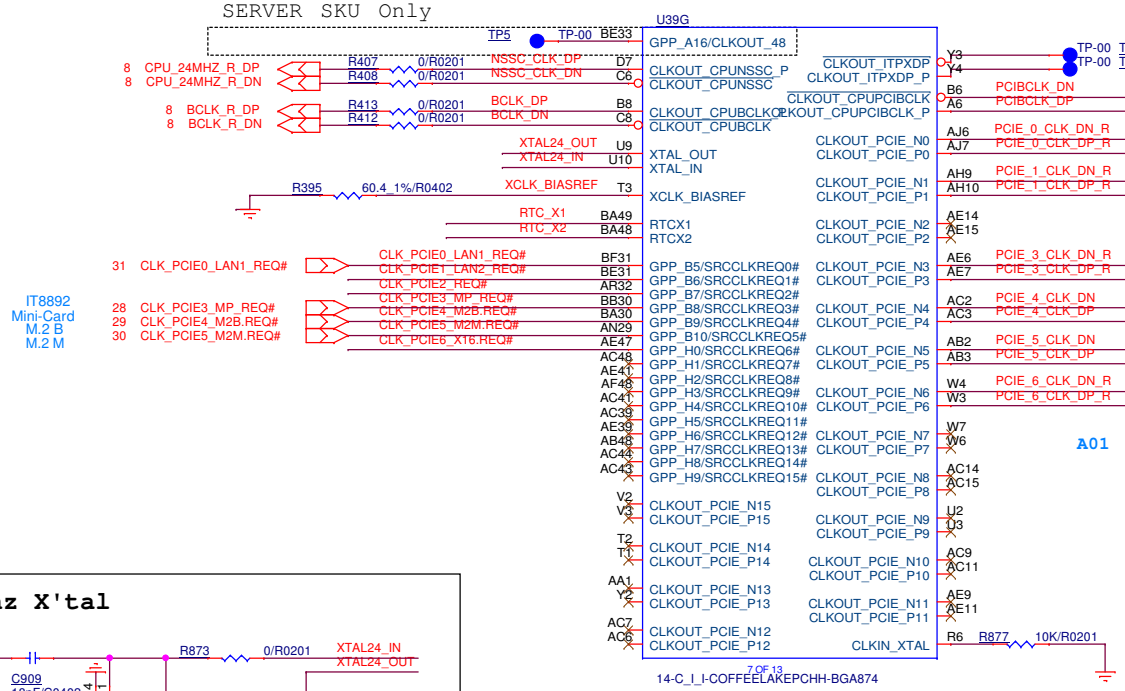


A01 add the R1873~R1876 0ohm (refer CRB REV0.9 reserved)_2017-10-24

Figure 12-1. Clock Integration Distribution Diagram

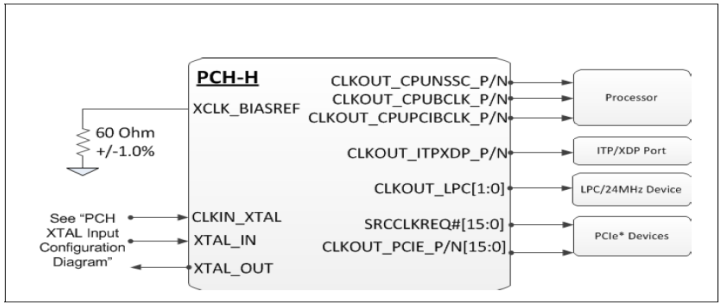
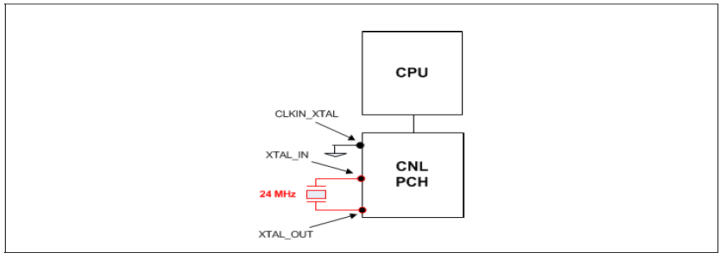
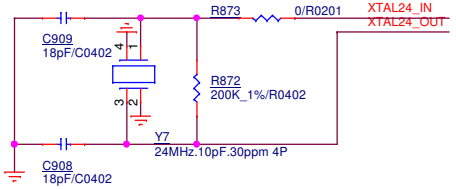
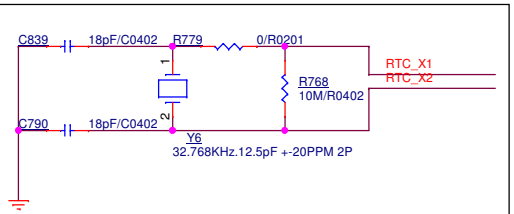


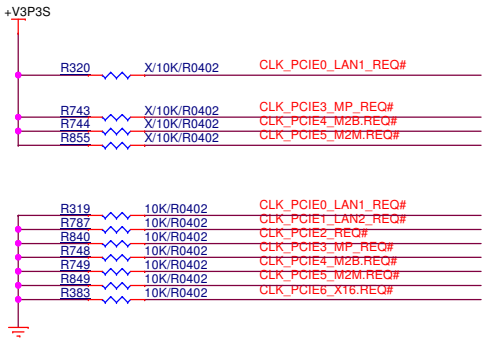
Figure 12-2. PCH XTAL Input Configuration Diagram



24Mhz X'tal







NOTE:

Any differential clock pair not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel ME FW

Any single ended clock signal not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel ME FW.

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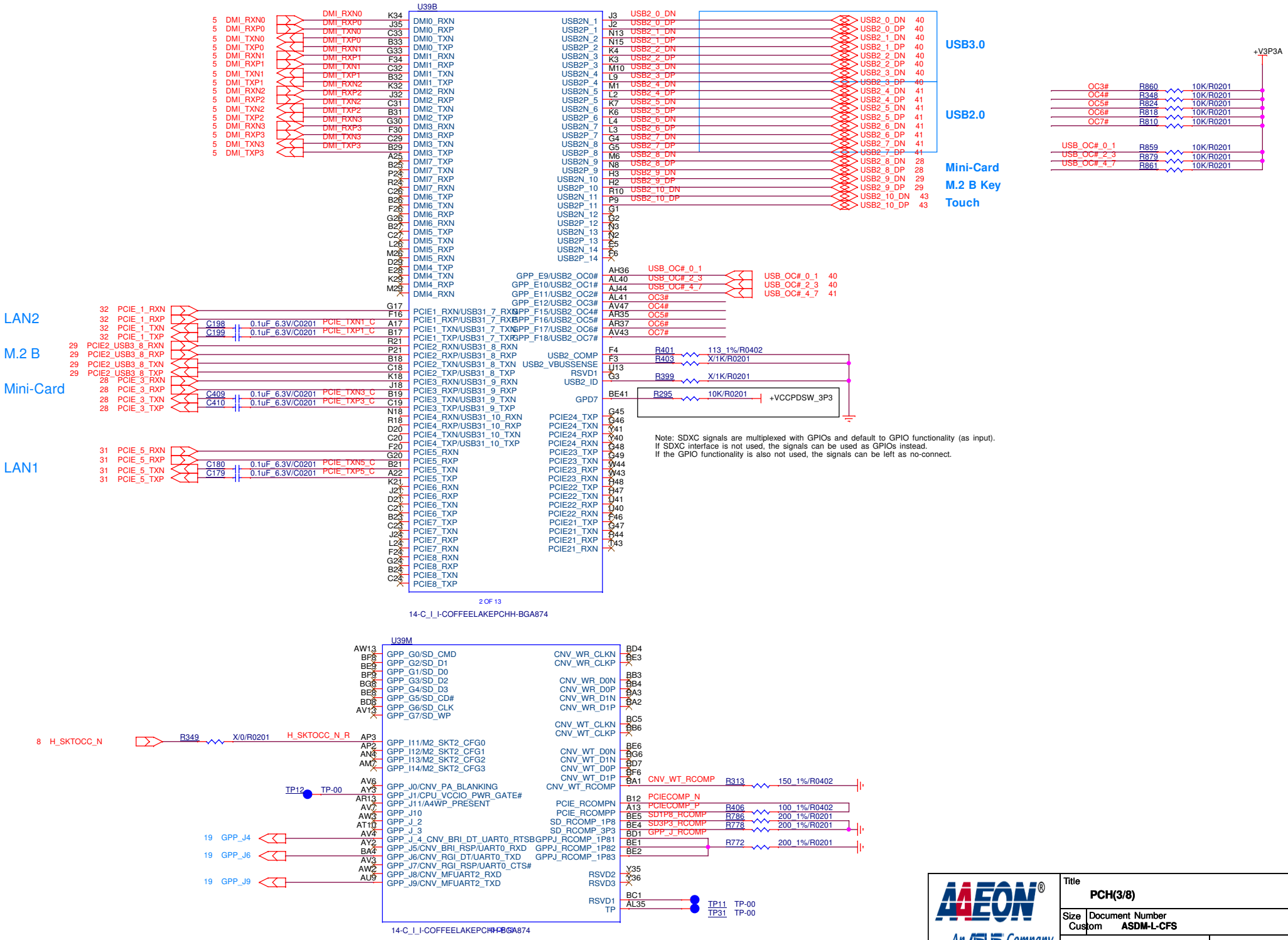

Title	PCH(3/8)	
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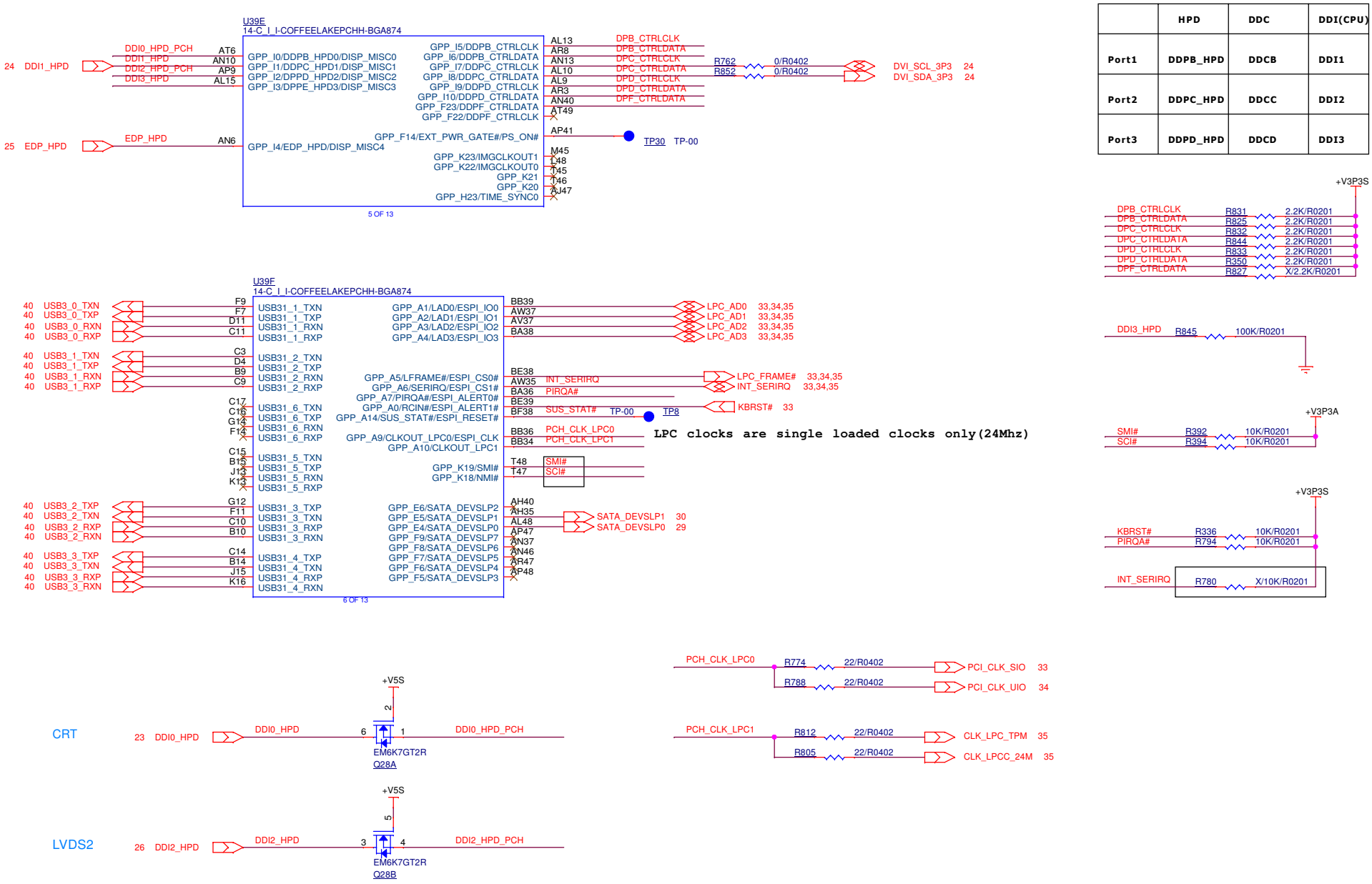

	HPD	DDC	DDI(CPU)
Port1	DDPB_HPD	DDCB	DDI1
Port2	DDPC_HPD	DDCC	DDI2
Port3	DDPD_HPD	DDCD	DDI3

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If an AMT capable Intel WLAN device is not implemented, then this signal can be left as NO CONNECT (NC).

CFL PCH H Flexible I/O

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE	SATA 0a	SATA 1a	GbE	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5						
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

Controller Link
The Controller Link is used to manage the wireless LN device

U39C

TP-00 TP14 AR2 CL_CLK
TP-00 TP26 AT5 CL_DATA
TP-00 TP13 AU4 CL_RST#

TP-00 TP19 P48 GPP_K8
V47 GPP_K9
V48 GPP_K10
W47 GPP_K11

TP-00 TP20 L47 GPP_K0
L46 GPP_K1
U48 GPP_K2
U47 GPP_K3
N48 GPP_K4
N47 GPP_K5
P47 GPP_K6
R46 GPP_K7

C36 PCIE11_TXP/SATA0A_TXP
B36 PCIE11_TXN/SATA0A_TXN
F39 PCIE11_RXP/SATA0A_RXP
G38 PCIE11_RXN/SATA0A_RXN

SGPIO
AR42 GPP_F10/SATA_SCLOCK
AR43 GPP_F11/SATA_SLOAD
AU47 GPP_F13/SATA_SDATAOUT0
AU46 GPP_F12/SATA_SDATAOUT1

28 SATA_1_TXN C39 PCIE14_TXN/SATA1B_TXN
28 SATA_1_TXP D39 PCIE14_TXP/SATA1B_TXP
28 SATA_1_RXN D46 PCIE14_RXN/SATA1B_RXN
28 SATA_1_RXP C47 PCIE14_RXP/SATA1B_RXP

28 SATA_0_TXN B38 PCIE13_TXN/SATA0B_TXN
28 SATA_0_TXP C38 PCIE13_TXP/SATA0B_TXP
28 SATA_0_RXN C45 PCIE13_RXN/SATA0B_RXN
28 SATA_0_RXP C46 PCIE13_RXP/SATA0B_RXP

E37 PCIE12_TXP/SATA1A_TXP
D38 PCIE12_TXN/SATA1A_TXN
J41 PCIE12_RXP/SATA_1A_RXP
H42 PCIE12_RXN/SATA1A_RXN

30 PCIE_20_TXP B44 PCIE20_TXP/SATA7_TXP
30 PCIE_20_TXN A44 PCIE20_TXN/SATA7_TXN
30 PCIE_20_RXP R37 PCIE20_RXP/SATA7_RXP
30 PCIE_20_RXN R35 PCIE20_RXN/SATA7_RXN

30 PCIE_19_TXP D43 PCIE19_TXP/SATA6_TXP
30 PCIE_19_TXN C44 PCIE19_TXN/SATA6_TXN
30 PCIE_19_RXP N42 PCIE19_RXP/SATA6_RXP
30 PCIE_19_RXN M44 PCIE19_RXN/SATA6_RXN

3 OF 13
14-C_I_I-COFFEELAKEPCHH-BGA874

PCIE9_RXN G36
PCIE9_RXP F36
PCIE9_TXN C34
PCIE9_TXP D34

PCIE10_RXN K37
PCIE10_RXP J37
PCIE10_TXN C35
PCIE10_TXP B35

PCIE15_RXN/SATA2_RXN F44 — SATA_2_RXN 28
PCIE15_RXP/SATA2_RXP E45 — SATA_2_RXP 28
PCIE_15_SATA_2_TXN B40 — SATA_2_TXN 28
PCIE15_TXP/SATA2_TXP C40 — SATA_2_TXP 28

PCIE16_RXN/SATA3_RXN L41 — PCIE16_SATA3_RXN 29
PCIE16_RXP/SATA3_RXP M40 — PCIE16_SATA3_RXP 29
PCIE16_TXN/SATA3_TXN B41 — PCIE16_SATA3_TXN 29
PCIE16_TXP/SATA3_TXP C41 — PCIE16_SATA3_TXP 29

M.2 B

PCIE17_RXN/SATA4_RXN K43 — PCIE17_SATA4_RXN 30
PCIE17_RXP/SATA4_RXP K44 — PCIE17_SATA4_RXP 30
PCIE17_TXN/SATA4_TXN A42 — PCIE17_SATA4_TXN 30
PCIE17_TXP/SATA4_TXP B42 — PCIE17_SATA4_TXP 30

M.2 M

PCIE18_RXN/SATA5_RXN P41 — PCIE18_SATA5_RXN 30
PCIE18_RXP/SATA5_RXP R40 — PCIE18_SATA5_RXP 30
PCIE18_TXN/SATA5_TXN C42 — PCIE18_SATA5_TXN 30
PCIE18_TXP/SATA5_TXP D42 — PCIE18_SATA5_TXP 30

M.2 M

GPP_E8/SATA_LED# AK48 — SATA_LED#
GPP_E0/SATAXPCIE0/SATAGP0 AH41 — SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1 AJ43 — SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2 AK47 — SATAGP2
GPP_F0/SATAXPCIE3/SATAGP_3 AN47 — SATAGP3
GPP_F1/SATAXPCIE4/SATAGP4 AM46 — SATAGP4 30
GPP_F2/SATAXPCIE5/SATAGP5 AM43
GPP_F3/SATAXPCIE6/SATAGP6 AM47
GPP_F4/SATAXPCIE7/SATAGP7 AM48

Default SATAXPCIE is set by a soft strap.

GPP_F21/EDP_BKLTCTL AU48 — EDP_BKLT_CTRL
GPP_F20/EDP_BKLTEN AV46 — EDP_BKLT_EN
GPP_F19/EDP_VDDEN AV44 — EDP_VDD_EN

THRMTRIP# AD3 — R390 30_1%/R0201 — PCH_THERMTRIP# 8
PECI AF2 — PCH_PECI 8
PM_SYNC AF3 — H_PM_SYNC_R — R385 30_1%/R0201 — H_PM_SYNC 8
PLTRST_CPU# AG5 — PLTRST_CPU#_R — R382 0/R0201 — PLTRST_CPU# 8
PM_DOWN AE2 — H_PM_DOWN_R — R387 0/R0201 — H_PM_DOWN 8

+V3P3S
R851 10K/R0402
FP_HDLED- — FP_HDLED- 29,30,53
Q29B EM6K7GT2R
+V3P3S
R854 10K/R0402
Q29A EM6K7GT2R
SATA_LED#

+V3P3S
EDP_BKLT_CTRL — R357 X/1K/R0402
EDP_BKLT_EN — R353 X/1K/R0402
EDP_VDD_EN — R820 X/1K/R0402

+V3P3S
SATAGP0 — R862 10K/R0201
SATAGP1 — R848 10K/R0201
SATAGP2 — R365 10K/R0201
SATAGP3 — R362 10K/R0201
SATAGP4 — R8015 10K/R0201

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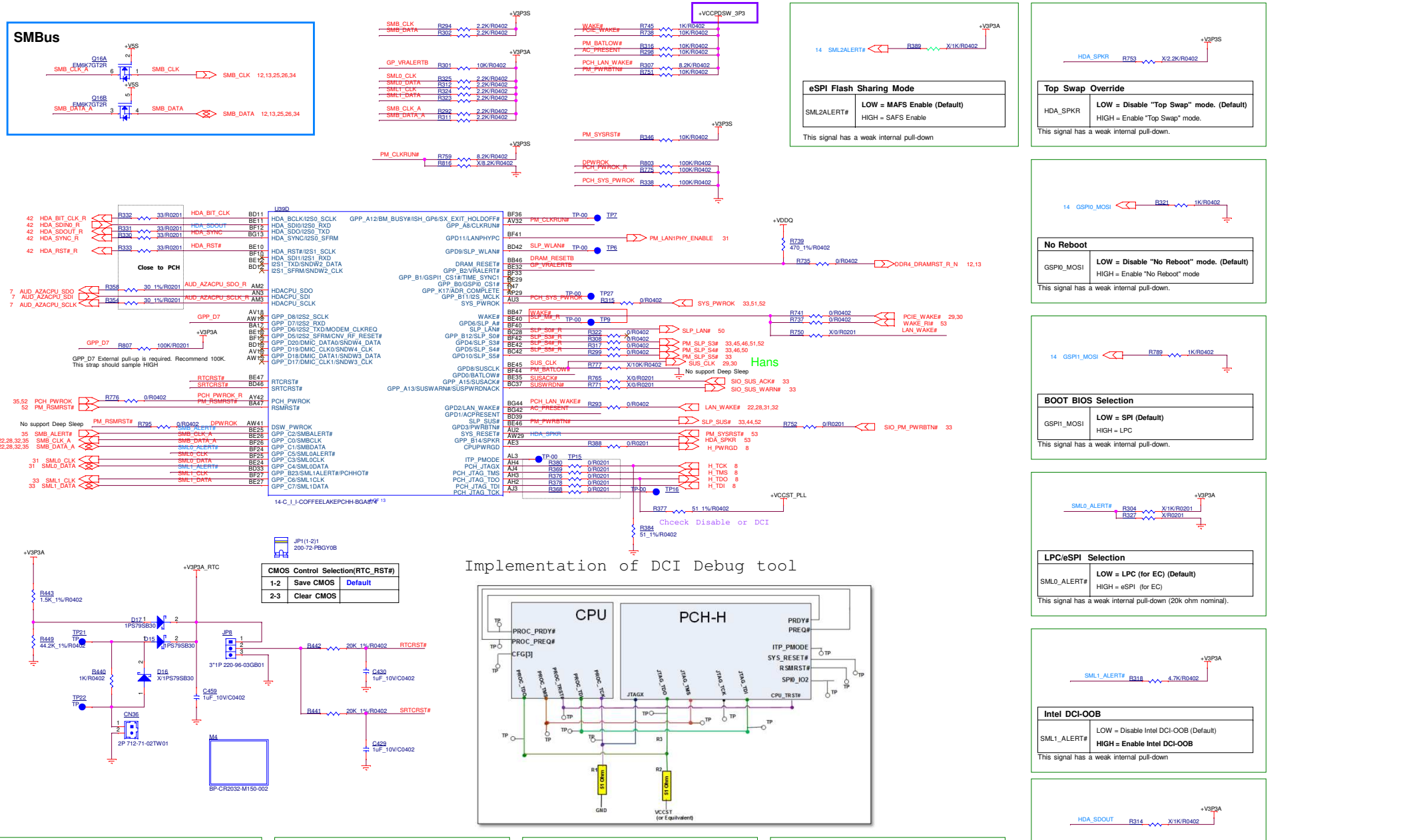
SMBus
Q16A
EM6K7GT2R
Q16B
EM6K7GT2R
SMB_CLK
SMB_DATA
SMB_CLK_A
SMB_DATA_A
+V5S
+V3P3S
+V3P3A
+VCCPDSW_3P3
+VDDQ
+VCCST_PLL
U39D
14-C_I_I-COFFEELAKEPCHH-BGA874
Close to PCH
GPP_D7 External pull-up is required. Recommend 100K.
This strap should sample HIGH
No support Deep Sleep
Hans
Chceck Disable or DCI
JP1(1-2)1
200-72-PBGY0B
CMOS Control Selection(RTC_RST#)
1-2 Save CMOS Default
2-3 Clear CMOS
Implementation of DCI Debug tool
CPU
PCH-H
PROC_PRDY#
PROC_PREQ#
CFG[3]
PRDY#
PREQ#
ITP_PMODE
SYS_RESET#
RSMRST#
SPI0_IO2
JTAGX
CPU_TRST#
3*1P 220-96-03GB01
2P 712-71-02TW01
BP-CR2032-M150-002
eSPI Flash Sharing Mode
SML2ALERT# | LOW = MAFS Enable (Default) / HIGH = SAFS Enable
This signal has a weak internal pull-down
Top Swap Override
HDA_SPKR | LOW = Disable "Top Swap" mode. (Default) / HIGH = Enable "Top Swap" mode.
This signal has a weak internal pull-down.
No Reboot
GSPI0_MOSI | LOW = Disable "No Reboot" mode. (Default) / HIGH = Enable "No Reboot" mode
This signal has a weak internal pull-down.
BOOT BIOS Selection
GSPI1_MOSI | LOW = SPI (Default) / HIGH = LPC
This signal has a weak internal pull-down.
LPC/eSPI Selection
SML0_ALERT# | LOW = LPC (for EC) (Default) / HIGH = eSPI (for EC)
This signal has a weak internal pull-down (20k ohm nominal).
Intel DCI-OOB
SML1_ALERT# | LOW = Disable Intel DCI-OOB (Default) / HIGH = Enable Intel DCI-OOB
This signal has a weak internal pull-down
Flash Descriptor Security Override
HDA_SDOUT | LOW = Enable security measures defined in the Flash Descriptor. (Default) / HIGH = Disable Flash Descriptor Security (override) manufacturing/debug environments ONLY.
This signal has a weak internal pull-down
TLS Confidentiality
SMB_ALERT# | LOW = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) / HIGH = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
This signal has a weak internal pull-down.
M.2 CNV Mode Selection
GPP_J6 | LOW = Integrated CNVi enable. / HIGH = Integrated CNVi disable.
A weak external pull-up is requred.
VCCSPI Selection
SML0_ALERT# | LOW = VCCSPI => 3.3V rail (Default) / HIGH = VCCSPI => 1.8V rail
This signal has a weak internal pull-down.
XTAL Frequecy Selection
GPP_J4 | LOW = 38.4 XTAL frequency selected. (Default) / HIGH = 24MHz XTAL frequency selected.
This signal has a weak internal pull-down.
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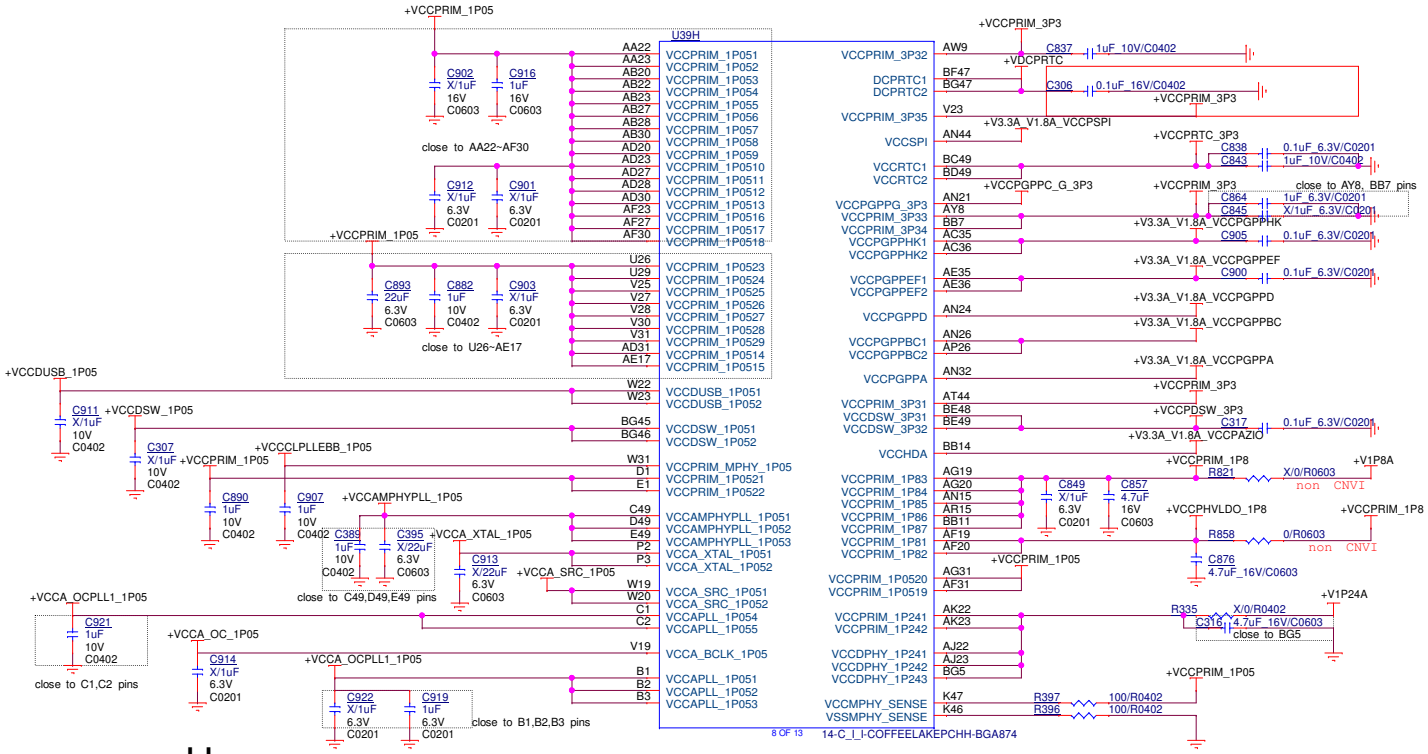
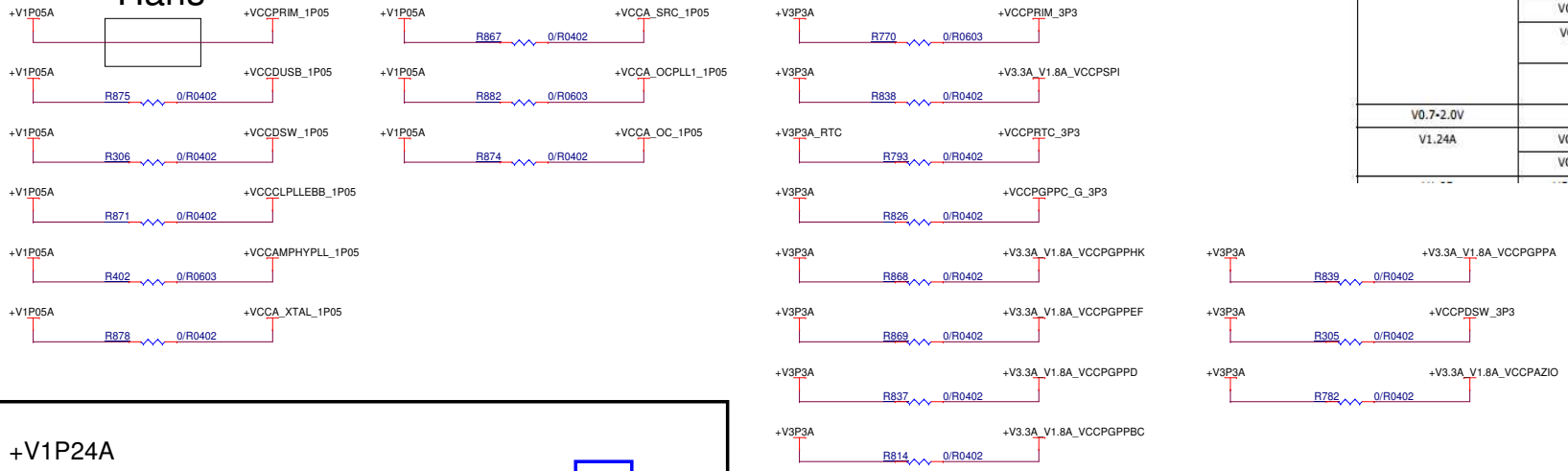
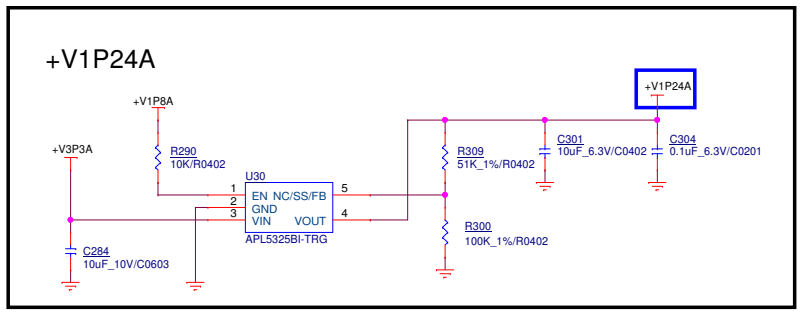


Voltage Supply	External Pin Name	Ball Number	Edge Cap
V1.05A	VCCAPLL_1P05	B1, B2, B3, C1, C2	1x 1uF, 0402, 5mm
	VCCPRIM_1P05	E1, D1	
	VCCA_BCLK_1P05	V19	
	VCCA_SRC_1P05	W19, W20	
	VCCA_XTAL_1P05	P2, P3	
	VCCPRIM_1P05	U26, U29, V25, V27, V28, V30, V31	1x 1uF 0402, 3mm 1x 22uF 0805, 5mm
	VCCAMPHYPLL_1P05	C49, D49, E49	1x 1uF 0402, 3mm
	VCCPRIM_MPHY_1P05	W31	
	VCCDUSB_1P05	W22, W23	
	VCCDSW_1P05	BG45, BG46	
	VCCPRIM_1P05	AF31, AG31, AD31, AA22, AA23, AB20, AB22, AB23, AB27, AB28, AB30, AD20, AD23, AD27, AD28, AD30, AF23, AF27, AF30, AE17	1x 1uF 0402, 3mm
V1.8A	VCCPRIM_1P8	AG19, AG20, AR15, AN15, BB11	1x 4.7uF 0603, 3mm Option 1: Internal LDO 1x 1uF 0402, 3mm Option 2: External VRM
	VCCPHVLDO_1P8	AF19, AF20	
V1.8A/V3.3A	VCCPGPPA	AN32	
	VCCPGPPBC	AN26, AP26	
	VCCPGPPD	AN24	
	VCCPGPPEF	AE35, AE36	1x 0.1uF 0402, 3mm (*placeholder*)
	VCCPGPPHK	AC35, AC36	1x 0.1uF 0402 3mm (*placeholder*)
	VCCPSPI	AN44	
V1.5A/V1.8A/3.3A	VCCHDA	BB14	
V3.3A	VCCPRIM_3P3	AW9, AY8, BB7, V23, AT44	1x 1uF 0603, 3mm Place close to AY8, BB7 pins.
	VCCPGPPG_3P3	AN21	
	VCCPDSW_3P3	BE48, BE49	1x 0.1uF 0402, 3mm (*placeholder*)
	VCCRTC	BC49,BD49	1x 0.1uF 0402, 3mm 1x 1uF 0402, 5mm
V0.7~2.0V	DCPRTC	BG47, BF47	
V1.24A	VCCDPHY_1P24	AJ22, AJ23, AK22, AK23	
	VCCDPHY_1P24	BG5	1x 4.7uF 0603, 5mm

Hans





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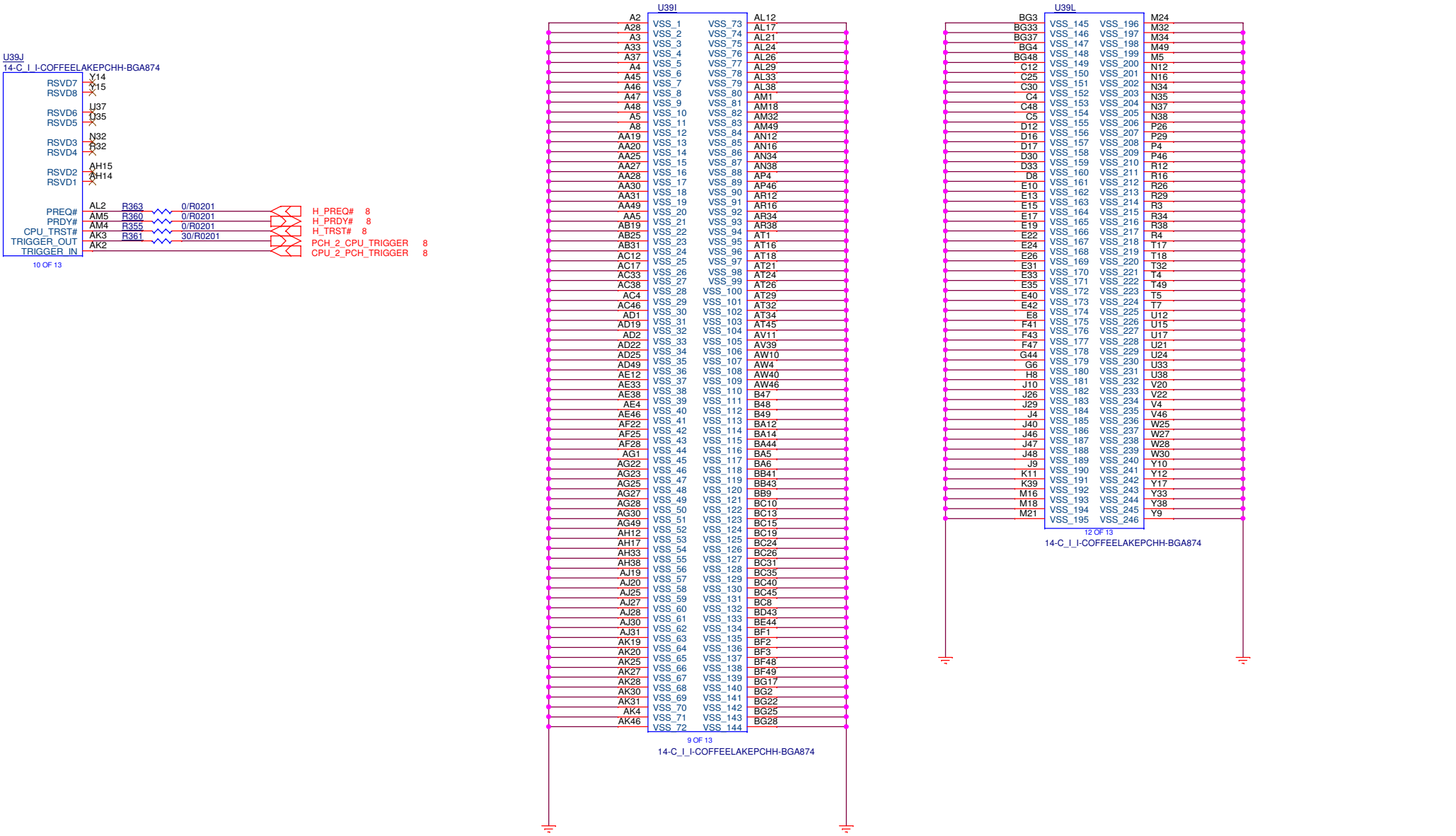

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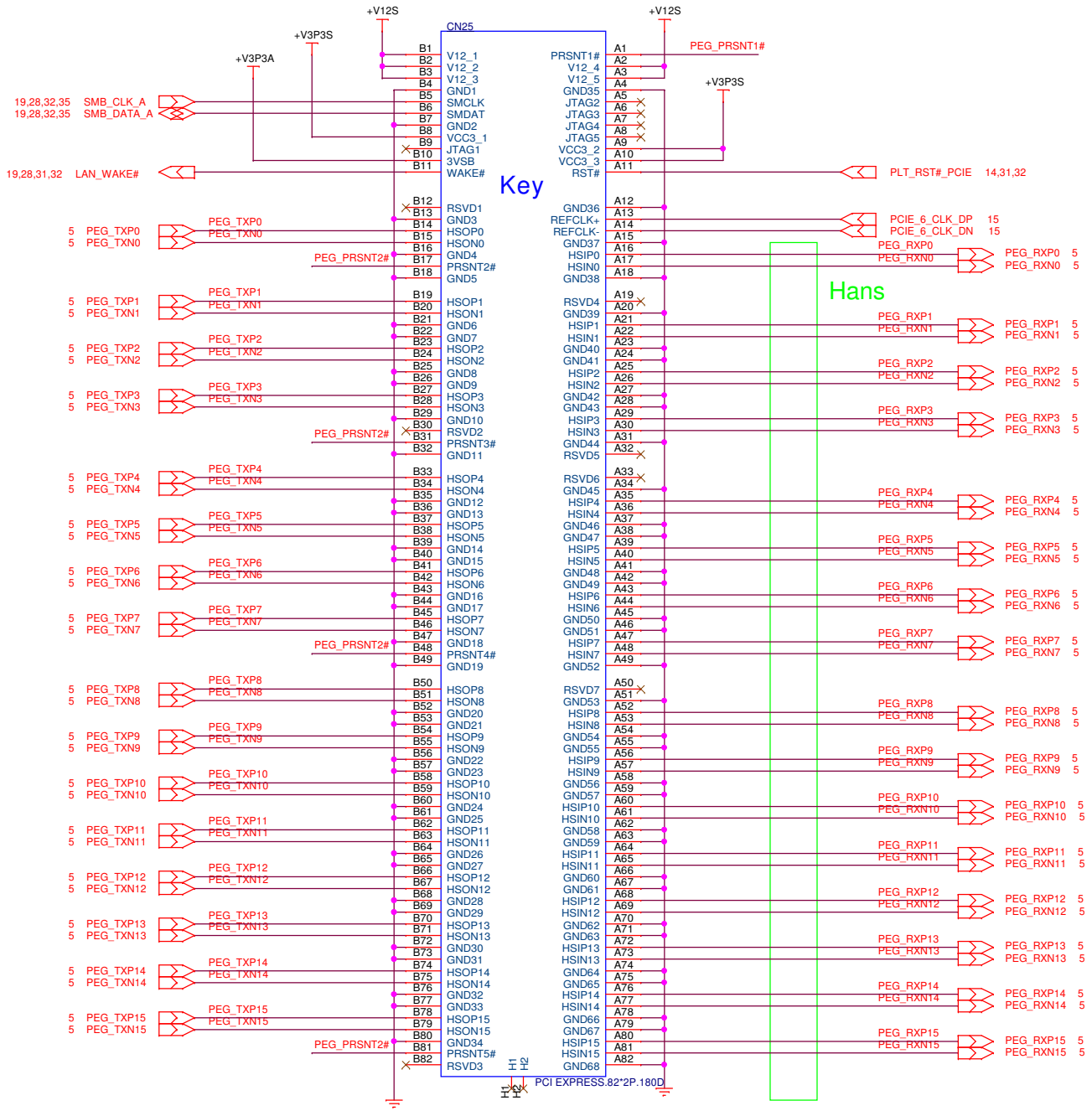

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Title: PCIE GRAPHICS

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CRT

DDI Interface
Differential Pair: 85ohm

7 DDI1_LANE0_DP — C131 0.1uF_6.3V/C0201 — DDI1_LANE0_DP_C
7 DDI1_LANE0_DN — C130 0.1uF_6.3V/C0201 — DDI1_LANE0_DN_C
7 DDI1_LANE1_DP — C129 0.1uF_6.3V/C0201 — DDI1_LANE1_DP_C
7 DDI1_LANE1_DN — C128 0.1uF_6.3V/C0201 — DDI1_LANE1_DN_C
7 DDI1_AUXP — C155 0.1uF_6.3V/C0201 — DDI1_AUXP_C
7 DDI1_AUXN — C164 0.1uF_6.3V/C0201 — DDI1_AUXN_C

+V3P3S — R134 1M/R0402 — R135 X/100K — DDI1_AUXP_C
+V3P3S — R150 X/100K — R151 1M/R0402 — DDI1_AUXN_C

DPB_HPD_R — R568 0/R0402 — DDI0_HPD 17
DPB_HPD_R — R105 100K/R0402

+V3P3S — R570 0/R0402 — 34 CH7517_RST#
+V3P3S — R569 X/1M/R0402
C124 X/0.1uF_16V/C0402 — GND_CH7517A
R104 10K/R0402 — GND_CH7517A

DDI1_LANE0_DP_C
DDI1_LANE0_DN_C
DDI1_LANE1_DP_C
DDI1_LANE1_DN_C
DPB_HPD_R
RESETB
ISEST
+VDVDD
+VAVDD

U18

40	RBIAS	XO	1
39	RSTB	XI	2
38	HPD	AUXP	3
37	DVDD2	AUXN	4
36	DGND2	AVSS2	5
35	D1N	AVCC2	6
34	D1P	RESERVED1	7
33	AVDD	RESERVED2	8
32	D0N	GNDPLL	9
31	D0P	VDDPLL	10
		TPAD	41
		AGND	30
		AVSS3	29
		RDAC	28
		AVCC3	27
		GDAC	26
		AVSS4	25
		BDAC	24
		AVCC4	23
		HSO	22
		VSO	21
	DVDD1	SPC	11
	DGND1	SPD	12
	SPC		13
	SPD		14
	GPIO0		15
	GPIO1		17
	AVSS1		18
	AVCC1		19
	VGA_SCL		20
	VGA_SDA		

CH7517ABF_Yellow

+VCC_3V3 — R117 X/1M_1%/R0402 — 7517_XO — 7517_XI — DDI1_AUXP_C — DDI1_AUXN_C
Y3 27MHz.18PF.20ppm 4P
C133 20pF_50V/C0402 — GND_CH7517A
C143 20pF_50V/C0402 — GND_CH7517A
+VDDPLL — GND_CH7517A

+VCC_DAC — CRT_RED — CRT_GREEN — CRT_BLUE — CRT_HSYNC — CRT_VSYNC — GND_CH7517A

CRT
Single End: 50ohm

+VDVDD — SPC — SPD — GND_CH7517A
+VCC_3V3 — GND_CH7517A
CRT_DDC_DATA — R181 1.8K_1%/R0402 — +V5S_DISP_R
CRT_DDC_CLK — R180 1.8K_1%/R0402
R615 0/R0603 — GND_CH7517A

Optional for firmware update

+V3P3S — R179 6.8K/R0402 — TP3 TP-00_SPD
+V3P3S — R178 6.8K/R0402 — TP2 TP-00_SPC

+V3P3S — FB33 120ohm(100MHz) — 100mA — C605 10uF_10V/C0603 — C617 10uF_10V/C0603 — C615 0.1uF_6.3V/C0201 — C607 0.1uF_6.3V/C0201 — +VCC_DAC
FB34 120ohm(100MHz) — +VCC_3V3 — C621 10uF_6.3V/C0402 — C613 0.1uF_6.3V/C0201

+V1P2S_VGA — FB32 120ohm(100MHz) — 150mA — C583 10uF_10V/C0603 — C183 10uF_10V/C0603 — C176 0.1uF_6.3V/C0201 — C582 0.1uF_6.3V/C0201 — +VDVDD
FB19 120ohm(100MHz) — +VDDPLL — C171 10uF_6.3V/C0402 — C169 0.1uF_6.3V/C0201 — GND_CH7517A
FB31 120ohm(100MHz) — +VAVDD — C577 10uF_6.3V/C0402 — C581 0.1uF_6.3V/C0201 — GND_CH7517A

+V3P3S — U62 EN NC/SS/FB GND VIN VOUT — APL5325BI-TRG — C557 10uF_6.3V/C0402
150mA — R559 5.1k_1%/R0402 — C570 10uF_6.3V/C0402 — +V1P2S_VGA — C569 0.1uF_6.3V/C0201
R560 10K/R0402

CRT_RED — R106 75_1%/R0402 — L2 27nH.DCR=0.9ohm IDC=200mA — C134 10pF/C0402 — C126 10pF/C0402 — CRT_RED_CON
CRT_GREEN — R116 75_1%/R0402 — L3 27nH.DCR=0.9ohm IDC=200mA — C142 10pF/C0402 — C138 10pF/C0402 — CRT_GREEN_CON
CRT_BLUE — R132 75_1%/R0402 — L4 27nH.DCR=0.9ohm IDC=200mA — C150 10pF/C0402 — C152 10pF/C0402 — CRT_BLUE_CON

U12

CRT_DDC_DATA	10	DDC_IN1	DDC_OUT1	9	CRT_DDCDAT_CON
CRT_DDC_CLK	11	DDC_IN2	DDC_OUT2	12	CRT_DDCCLK_CON
CRT_HSYNC	13	SYNC_IN1	SYNC_OUT1	14	HSYNC_R
CRT_VSYNC	15	SYNC_IN2	SYNC_OUT2	16	VSYNC_R
			VCC_VIDEO	2	
			VCC_SYNC	1	
CRT_RED	3	VIDEO_1	VCC_DDC	7	
CRT_GREEN	4	VIDEO_2	BYP	8	
CRT_BLUE	5	VIDEO_3	GNDD	6	

TPD7S019-15DBQR

+V5S_DISP — R142 1.8K_1%/R0402 — R136 1.8K_1%/R0402
R126 33/R0402 — CRT_HSYNC_CON
R113 33/R0402 — CRT_VSYNC_CON
+V5S_DISP — C579 0.22uF_10V/C0402
+V5S — C606 0.22uF_10V/C0402
C611 0.22uF_10V/C0402
C139 33pF/C0402
C125 33pF/C0402

+V5S — D21 B130LAW-7-F — +V5S_DISP_F — FS4 1206L110THYR 8V;1.1A — +V5S_DISP_R — FB24 30ohm(100MHz).1A L0603 — +V5S_DISP_CON
C514 10uF_10V/C0603
C515 0.1uF_10V/C0201

CN10

CRT_RED_CON	1	6	16
CRT_GREEN_CON	2	11	
CRT_BLUE_CON	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
CRT_DDCDAT_CON	11		
CRT_HSYNC_CON	12		
CRT_VSYNC_CON	13		
CRT_DDCCLK_CON	14		
	15	5	17

15P A17201SBG0611

+V5S_DISP_CON

CRT_RED_CON — CRT_RED_CON 24
CRT_GREEN_CON — CRT_GREEN_CON 24
CRT_BLUE_CON — CRT_BLUE_CON 24
CRT_HSYNC_CON — CRT_HSYNC_CON 24
CRT_VSYNC_CON — CRT_VSYNC_CON 24

<Variant Name>

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Title: CRT CH7517		
Size: Custom	Document Number: PCM-CFS	Rev: A0.2
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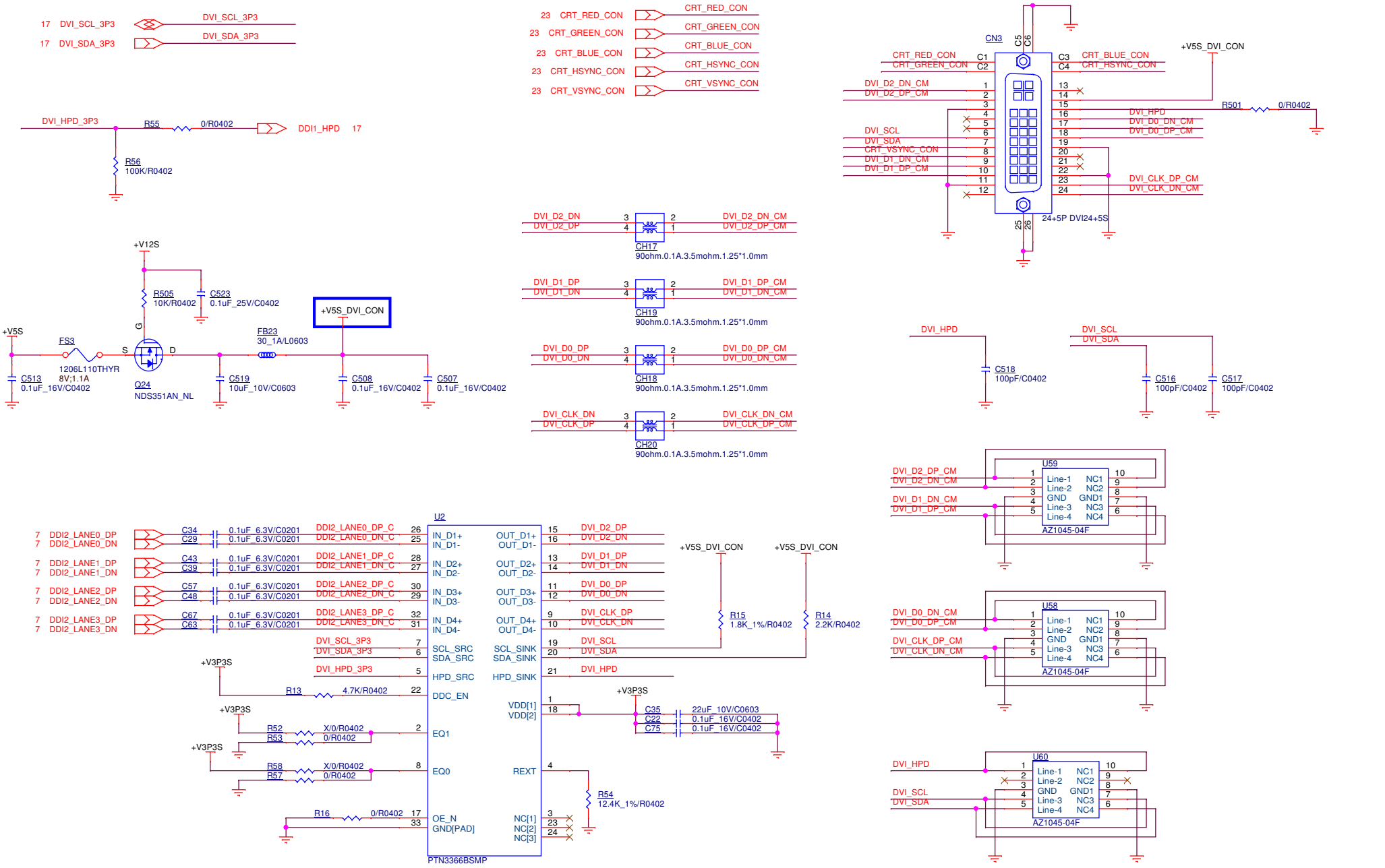
DVI



Title: DVI			
Size: Custom	Document Number: PCM-CFS		Rev: A0.2
Date: Tuesday, September 03, 2015	Sheet: 54	of 124	

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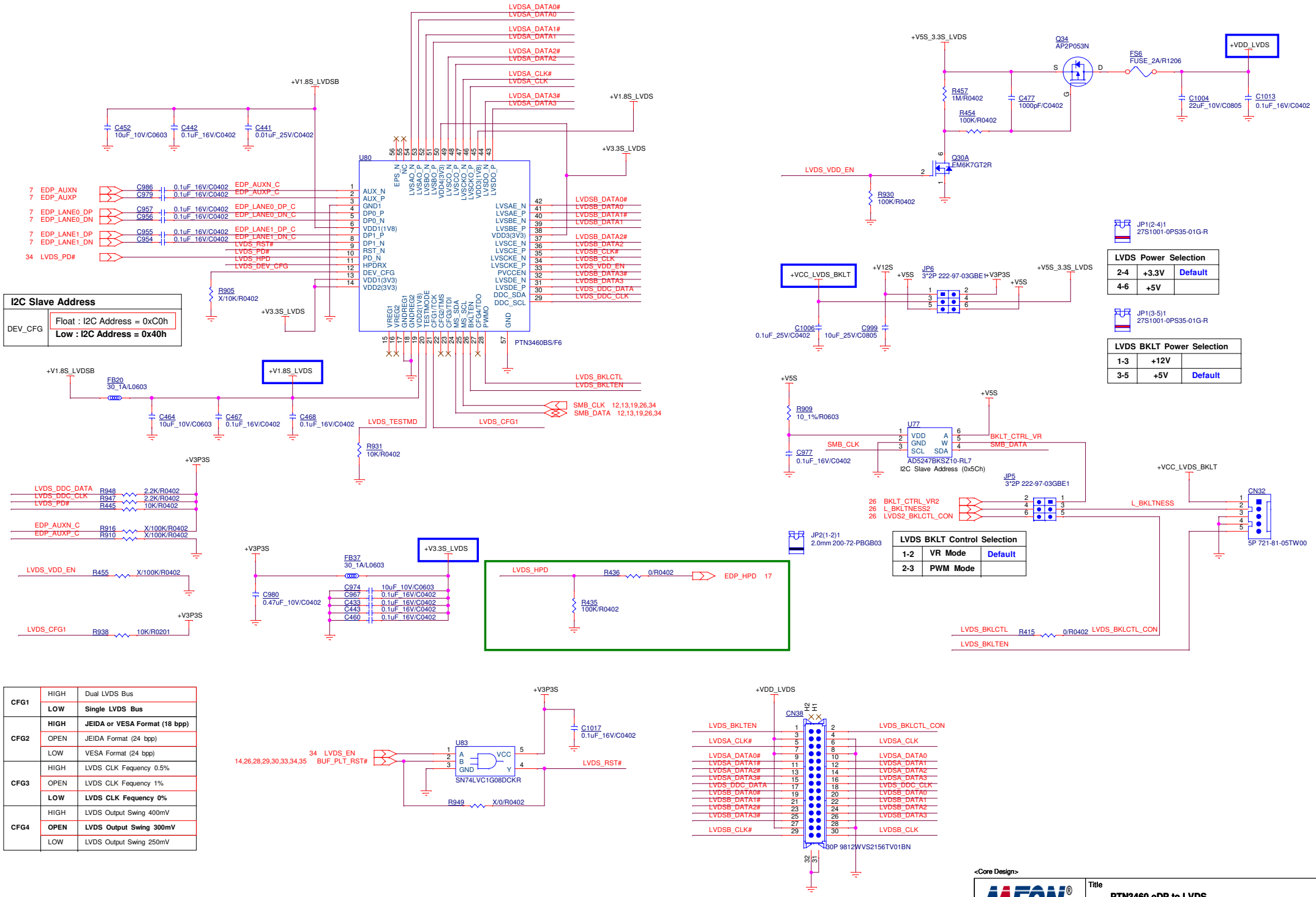


I2C Slave Address	
DEV_CFG	Float : I2C Address = 0xC0h **Low : I2C Address = 0x40h**

LVDS Power Selection		
2-4	+3.3V	Default
4-6	+5V	

LVDS BKLT Power Selection		
1-3	+12V	
3-5	+5V	Default

LVDS BKLT Control Selection		
1-2	VR Mode	Default
2-3	PWM Mode	

CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

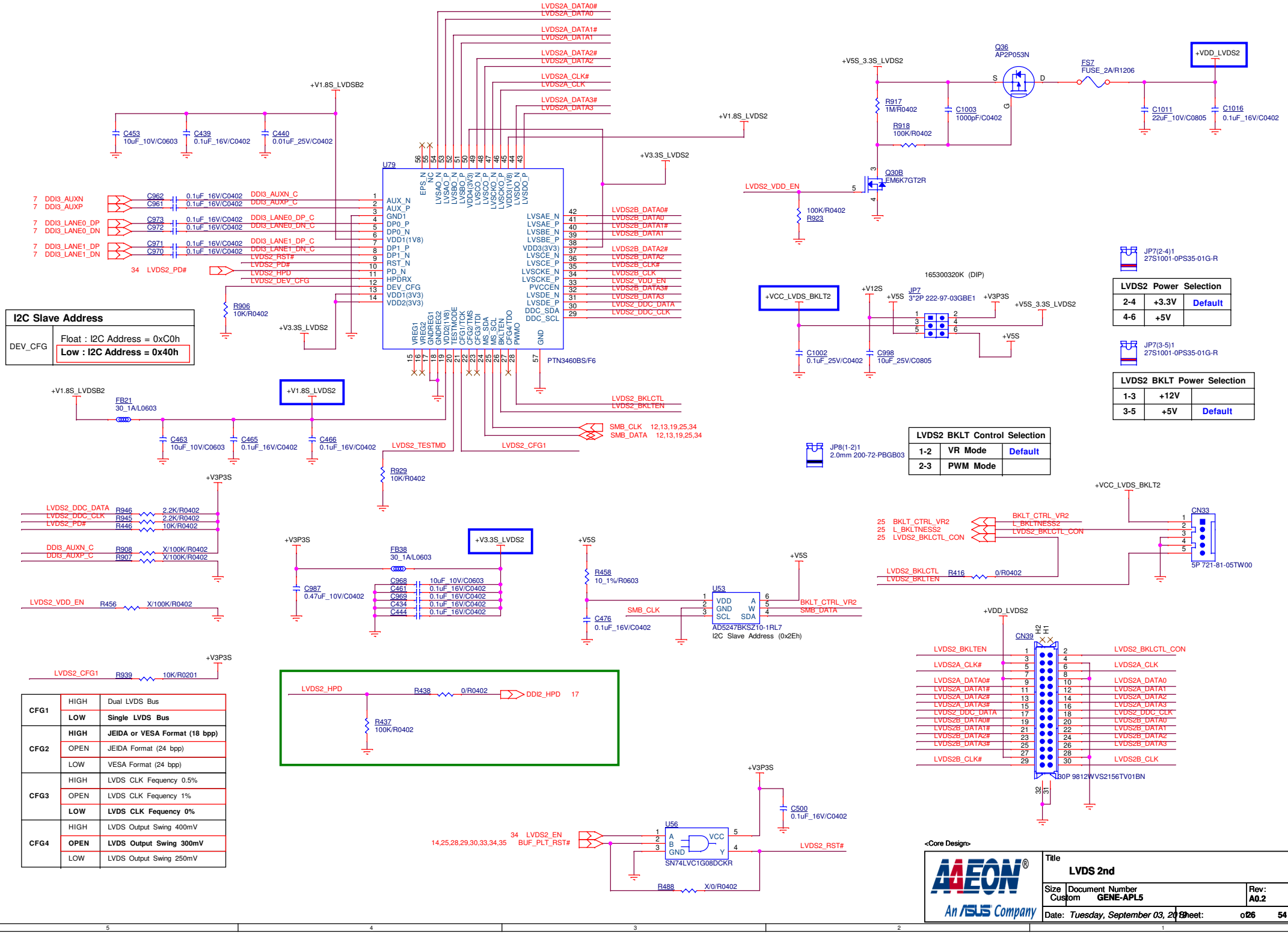
<Core Design>

AAEON An ASUS Company

Title: PTN3460 eDP to LVDS

Size: Custom | Document Number: GENE-APL5 | Rev: A0.2

Date: Tuesday, September 03, 2019 | Sheet: 25 of 54



I2C Slave Address	
DEV_CFG	Float : I2C Address = 0xC0h
	Low : I2C Address = 0x40h

LVDS2 Power Selection		
2-4	+3.3V	Default
4-6	+5V	

LVDS2 BKLT Power Selection		
1-3	+12V	
3-5	+5V	Default

LVDS2 BKLT Control Selection		
1-2	VR Mode	Default
2-3	PWM Mode	

CFG1	HIGH	Dual LVDS Bus
	LOW	**Single LVDS Bus**
CFG2	**HIGH**	**JEIDA or VESA Format (18 bpp)**
	OPEN	JEIDA Format (24 bpp)
	LOW	VESA Format (24 bpp)
CFG3	HIGH	LVDS CLK Fequency 0.5%
	OPEN	LVDS CLK Fequency 1%
	LOW	**LVDS CLK Fequency 0%**
CFG4	HIGH	LVDS Output Swing 400mV
	OPEN	**LVDS Output Swing 300mV**
	LOW	LVDS Output Swing 250mV

<Core Design>

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Title: LVDS 2nd

Size: Custom | Document Number: GENE-APL5 | Rev: A0.2

Date: Tuesday, September 03, 2018 | Sheet: 26 of 54

Remove

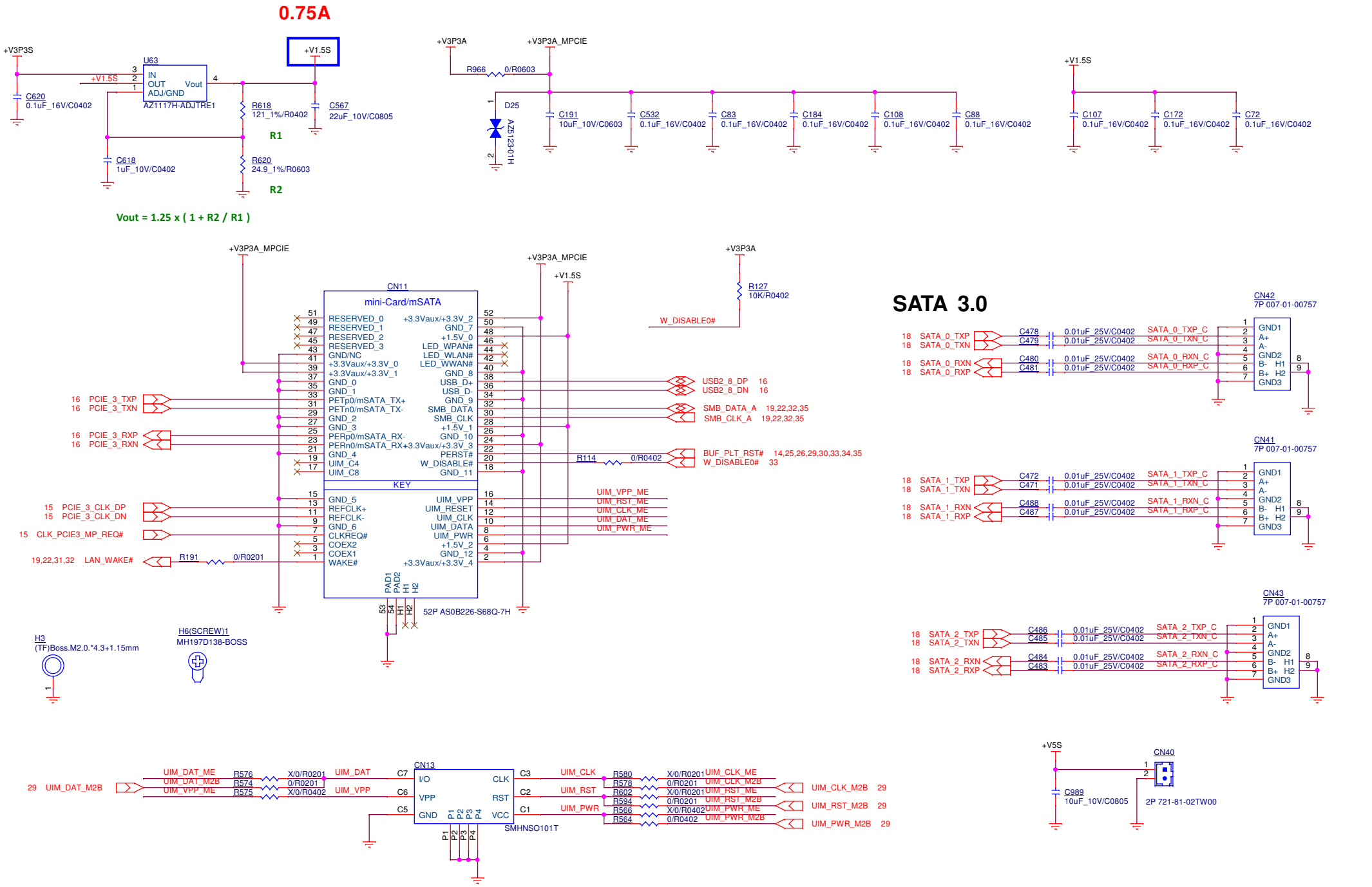
<Variant Name>

AAEON® An ASUS Company

Title: PCIE to PCI - IT8892

Size: Custom | Document Number: PCM-QM77 | Rev: A0.2

Date: Tuesday, September 03, 2013 | Sheet: 27 of 54


0.75A
+V3P3S
U63
IN
OUT
ADJ/GND
Vout
AZ1117H-ADJTRE1
+V1.5S
C620
0.1uF_16V/C0402
C618
1uF_10V/C0402
R618
121_1%/R0402
R1
R620
24.9_1%/R0603
R2
C567
22uF_10V/C0805
Vout = 1.25 x (1 + R2 / R1)
+V3P3A
+V3P3A_MPCIE
R966
0/R0603
D25
AZ5123-01H
C191
10uF_10V/C0603
C532
0.1uF_16V/C0402
C83
C184
C108
C88
C107
C172
C72
CN11
mini-Card/mSATA
RESERVED_0
RESERVED_1
RESERVED_2
RESERVED_3
GND/NC
+3.3Vaux/+3.3V_0
+3.3Vaux/+3.3V_1
GND_0
GND_1
PETp0/mSATA_TX+
PETn0/mSATA_TX-
GND_2
GND_3
PERp0/mSATA_RX-
PERn0/mSATA_RX+
GND_4
UIM_C4
UIM_C8
+3.3Vaux/+3.3V_2
GND_7
+1.5V_0
LED_WPAN#
LED_WLAN#
LED_WWAN#
GND_8
USB_D+
USB_D-
GND_9
SMB_DATA
SMB_CLK
+1.5V_1
GND_10
+3.3Vaux/+3.3V_3
PERST#
W_DISABLE#
GND_11
KEY
GND_5
REFCLK+
REFCLK-
GND_6
CLKREQ#
COEX2
COEX1
WAKE#
UIM_VPP
UIM_RESET
UIM_CLK
UIM_DATA
UIM_PWR
+1.5V_2
GND_12
+3.3Vaux/+3.3V_4
PAD1
PAD2
H1
H2
52P AS0B226-S68Q-7H
R127
10K/R0402
W_DISABLE0#
USB2_8_DP 16
USB2_8_DN 16
SMB_DATA_A 19,22,32,35
SMB_CLK_A 19,22,32,35
BUF_PLT_RST# 14,25,26,29,30,33,34,35
W_DISABLE0# 33
R114
0/R0402
UIM_VPP_ME
UIM_RST_ME
UIM_CLK_ME
UIM_DAT_ME
UIM_PWR_ME
16 PCIE_3_TXP
16 PCIE_3_TXN
16 PCIE_3_RXP
16 PCIE_3_RXN
15 PCIE_3_CLK_DP
15 PCIE_3_CLK_DN
15 CLK_PCIE3_MP_REQ#
19,22,31,32 LAN_WAKE#
R191
0/R0201
H3
(TF)Boss.M2.0.*4.3+1.15mm
H6(SCREW)1
MH197D138-BOSS
SATA 3.0
CN42
7P 007-01-00757
CN41
7P 007-01-00757
CN43
7P 007-01-00757
18 SATA_0_TXP
18 SATA_0_TXN
18 SATA_0_RXN
18 SATA_0_RXP
C478
C479
C480
C481
0.01uF_25V/C0402
SATA_0_TXP_C
SATA_0_TXN_C
SATA_0_RXN_C
SATA_0_RXP_C
18 SATA_1_TXP
18 SATA_1_TXN
18 SATA_1_RXN
18 SATA_1_RXP
C472
C471
C488
C487
SATA_1_TXP_C
SATA_1_TXN_C
SATA_1_RXN_C
SATA_1_RXP_C
18 SATA_2_TXP
18 SATA_2_TXN
18 SATA_2_RXN
18 SATA_2_RXP
C486
C485
C484
C483
SATA_2_TXP_C
SATA_2_TXN_C
SATA_2_RXN_C
SATA_2_RXP_C
GND1
A+
A-
GND2
B- H1
B+ H2
GND3
29 UIM_DAT_M2B
UIM_DAT_ME
UIM_DAT_M2B
UIM_VPP_ME
R576
R574
R575
X/0/R0201
0/R0201
X/0/R0402
UIM_DAT
UIM_VPP
CN13
I/O
VPP
GND
CLK
RST
VCC
C7
C6
C5
C3
C2
C1
UIM_CLK
UIM_RST
UIM_PWR
SMHNSO101T
R580
R578
R602
R594
R566
R564
UIM_CLK_ME
UIM_CLK_M2B
UIM_RST_ME
UIM_RST_M2B
UIM_PWR_ME
UIM_PWR_M2B
UIM_CLK_M2B 29
UIM_RST_M2B 29
UIM_PWR_M2B 29
+V5S
CN40
C989
10uF_10V/C0805
2P 721-81-02TW00
AAEON
An ASUS Company
Title
Mini-Card/SATA
Size
Custom
Document Number
PCM-CFS
Rev:
A0.2
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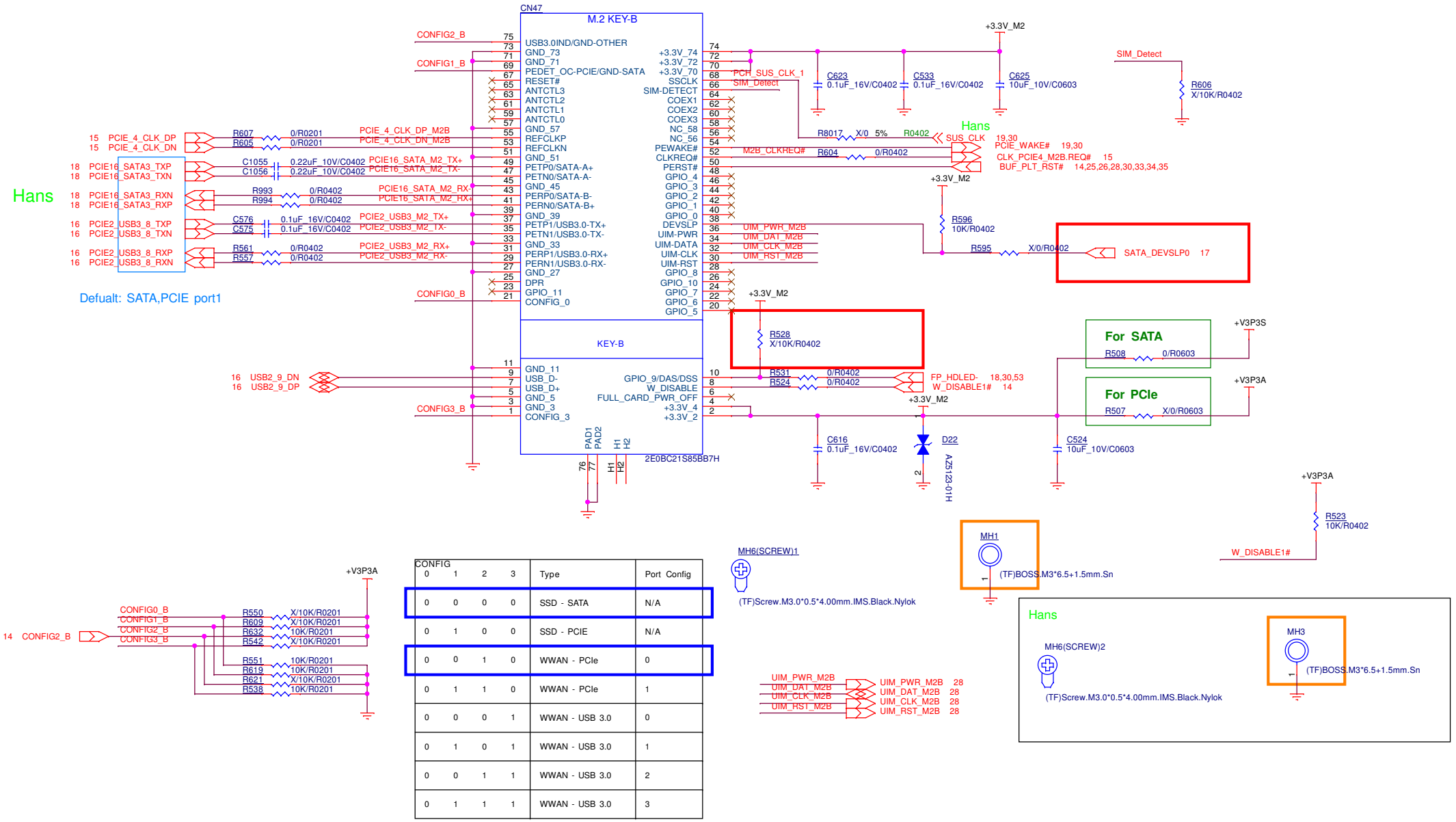
M.2 Key B



CONFIG 0	1	2	3	Type	Port Config
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIE	N/A
0	0	1	0	WWAN - PCIe	0
0	1	1	0	WWAN - PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3

<Variant Name>

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Title: M.2 B Key		
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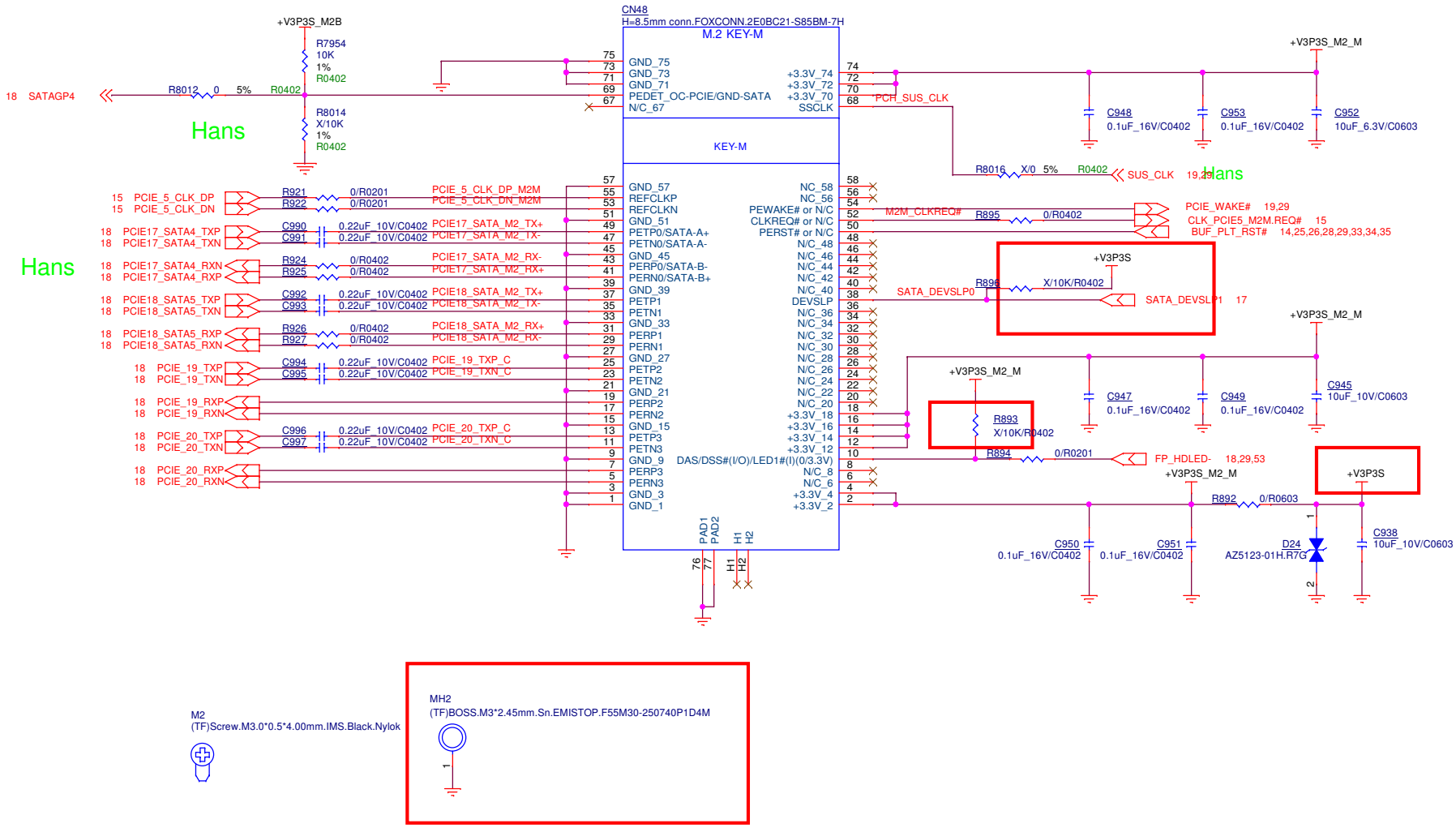
M.2 Key M



<Variant Name>

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Title: M.2 M Key		
Size: Custom	Document Number: PCM-CFS	Rev: A0.2
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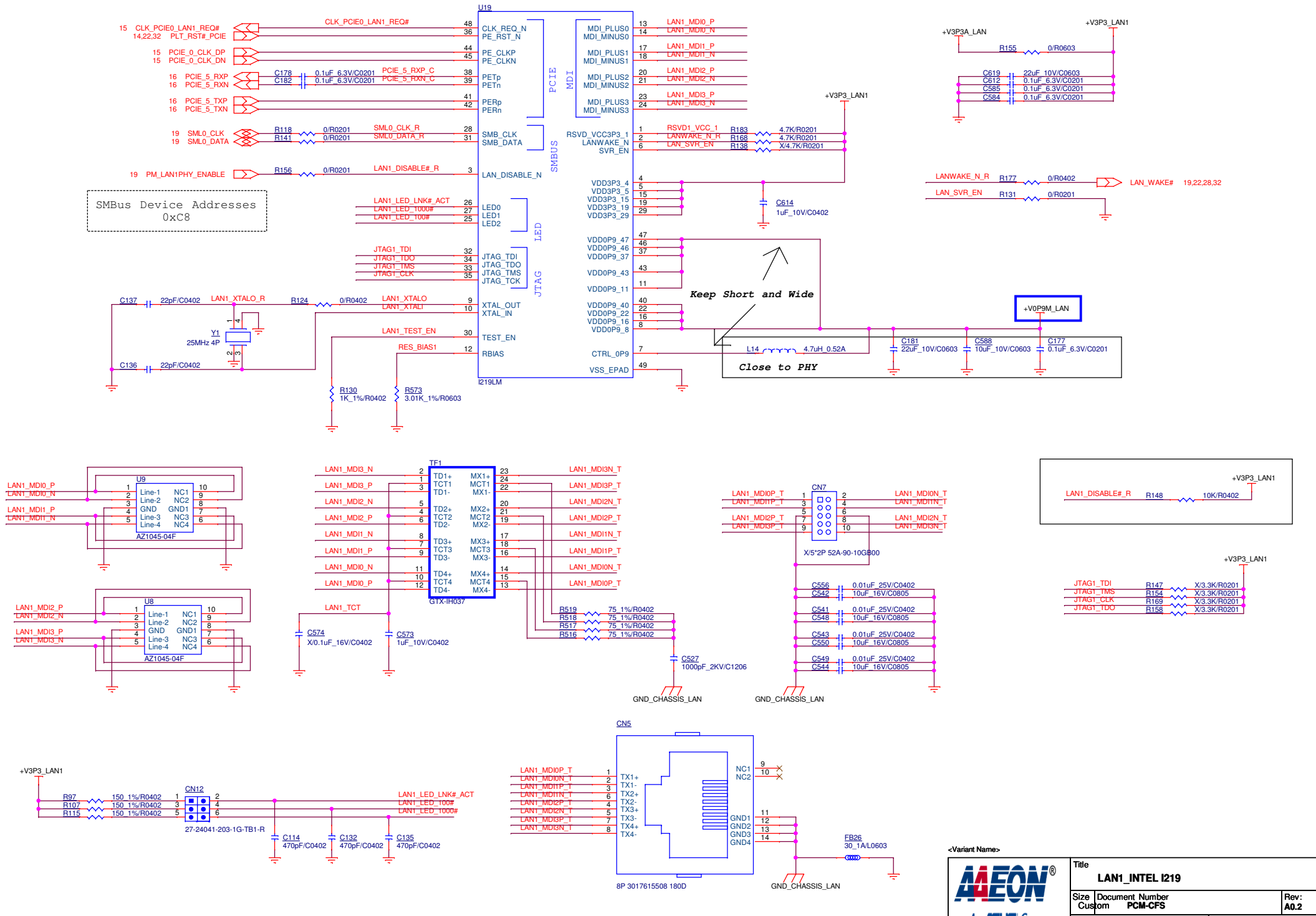
U19
I219LM
PCIE
MDI
SMBUS
LED
JTAG
CLK_PCIE0_LAN1_REQ#
PLT_RST#_PCIE
PCIE_0_CLK_DP
PCIE_0_CLK_DN
PCIE_5_RXP
PCIE_5_RXN
PCIE_5_TXP
PCIE_5_TXN
SML0_CLK
SML0_DATA
PM_LAN1PHY_ENABLE
SMBus Device Addresses
0xC8
LAN1_LED_LNK#_ACT
LAN1_LED_1000#
LAN1_LED_100#
JTAG1_TDI
JTAG1_TDO
JTAG1_TMS
JTAG1_CLK
C137 22pF/C0402
C136 22pF/C0402
LAN1_XTALO_R
LAN1_XTALO
LAN1_XTALI
R124 0/R0402
Y1
25MHz 4P
LAN1_TEST_EN
RES_BIAS1
R130
1K_1%/R0402
R573
3.01K_1%/R0603
LAN1_MDI0_P
LAN1_MDI0_N
LAN1_MDI1_P
LAN1_MDI1_N
LAN1_MDI2_P
LAN1_MDI2_N
LAN1_MDI3_P
LAN1_MDI3_N
RSVD_VCC3P3_1
LANWAKE_N_R
SVR_EN
R183 4.7K/R0201
R168 4.7K/R0201
R138 X/4.7K/R0201
LAN_SVR_EN
+V3P3_LAN1
C614
1uF_10V/C0402
VDD3P3_4
VDD3P3_5
VDD3P3_15
VDD3P3_19
VDD3P3_29
VDD0P9_47
VDD0P9_46
VDD0P9_37
VDD0P9_43
VDD0P9_11
VDD0P9_40
VDD0P9_22
VDD0P9_16
VDD0P9_8
CTRL_0P9
VSS_EPAD
Keep Short and Wide
Close to PHY
L14 4.7uH_0.52A
C181 22uF_10V/C0603
C588 10uF_10V/C0603
C177 0.1uF_6.3V/C0201
+V0P9M_LAN
+V3P3A_LAN
R155 0/R0603
C619 22uF_10V/C0603
C612 0.1uF_6.3V/C0201
C585 0.1uF_6.3V/C0201
C584 0.1uF_6.3V/C0201
LANWAKE_N_R
R177 0/R0402
LAN_WAKE# 19,22,28,32
LAN_SVR_EN
R131 0/R0201
U9
AZ1045-04F
U8
AZ1045-04F
TF1
GTX-IH037
C574 X/0.1uF_16V/C0402
C573 1uF_10V/C0402
R519 75_1%/R0402
R518 75_1%/R0402
R517 75_1%/R0402
R516 75_1%/R0402
C527 1000pF_2KV/C1206
GND_CHASSIS_LAN
CN7
X/5*2P 52A-90-10GB00
C556 0.01uF_25V/C0402
C542 10uF_16V/C0805
C541 0.01uF_25V/C0402
C548 10uF_16V/C0805
C543 0.01uF_25V/C0402
C550 10uF_16V/C0805
C549 0.01uF_25V/C0402
C544 10uF_16V/C0805
LAN1_DISABLE#_R
R148 10K/R0402
JTAG1_TDI R147 X/3.3K/R0201
JTAG1_TMS R154 X/3.3K/R0201
JTAG1_CLK R169 X/3.3K/R0201
JTAG1_TDO R158 X/3.3K/R0201
CN12
R97 150_1%/R0402
R107 150_1%/R0402
R115 150_1%/R0402
27-24041-203-1G-TB1-R
C114 470pF/C0402
C132 470pF/C0402
C135 470pF/C0402
CN5
8P 3017615508 180D
FB26
30_1A/L0603
<Variant Name>
AAEON
An ASUS Company
Title
LAN1_INTEL I219
Size Custom
Document Number PCM-CFS
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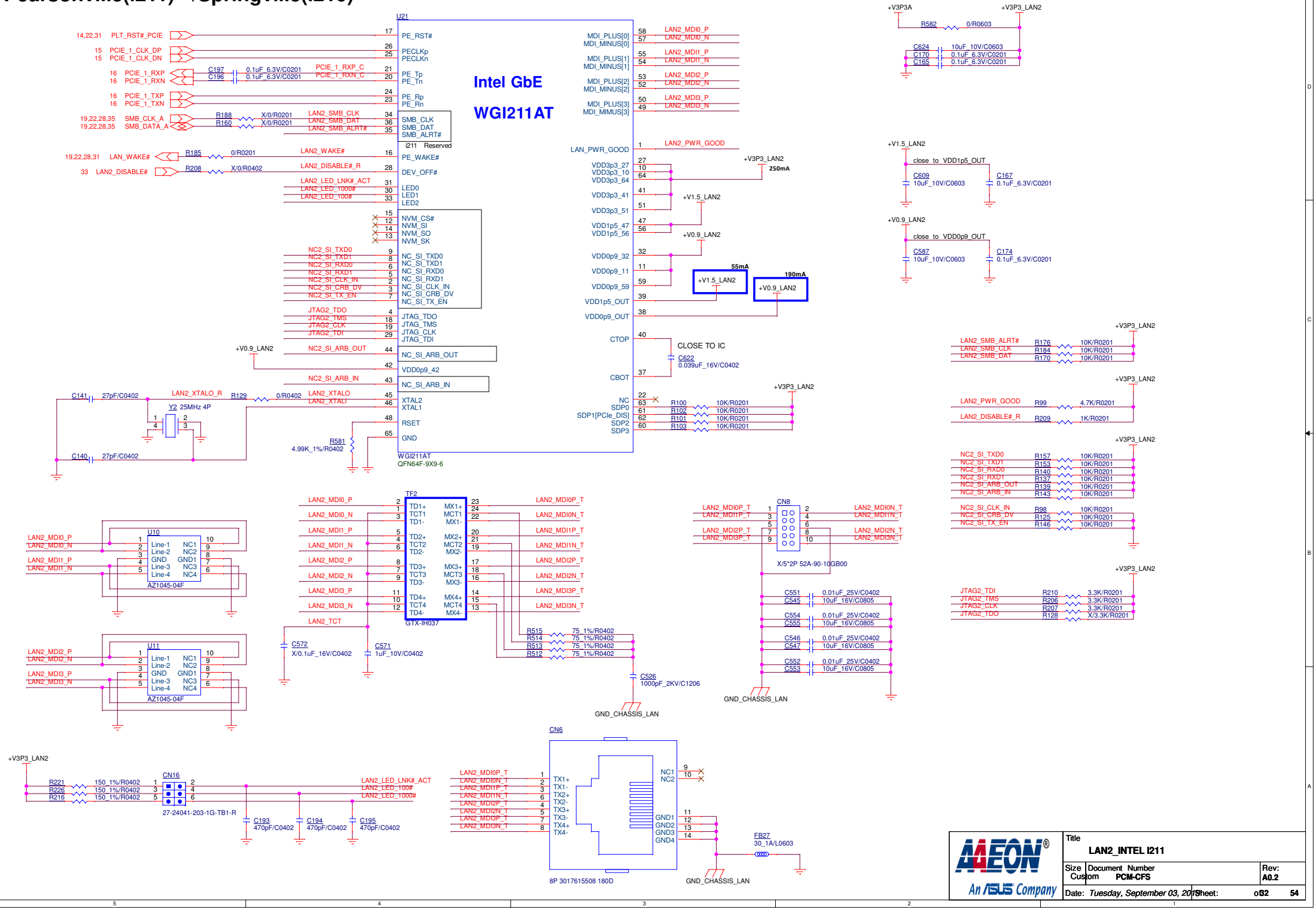
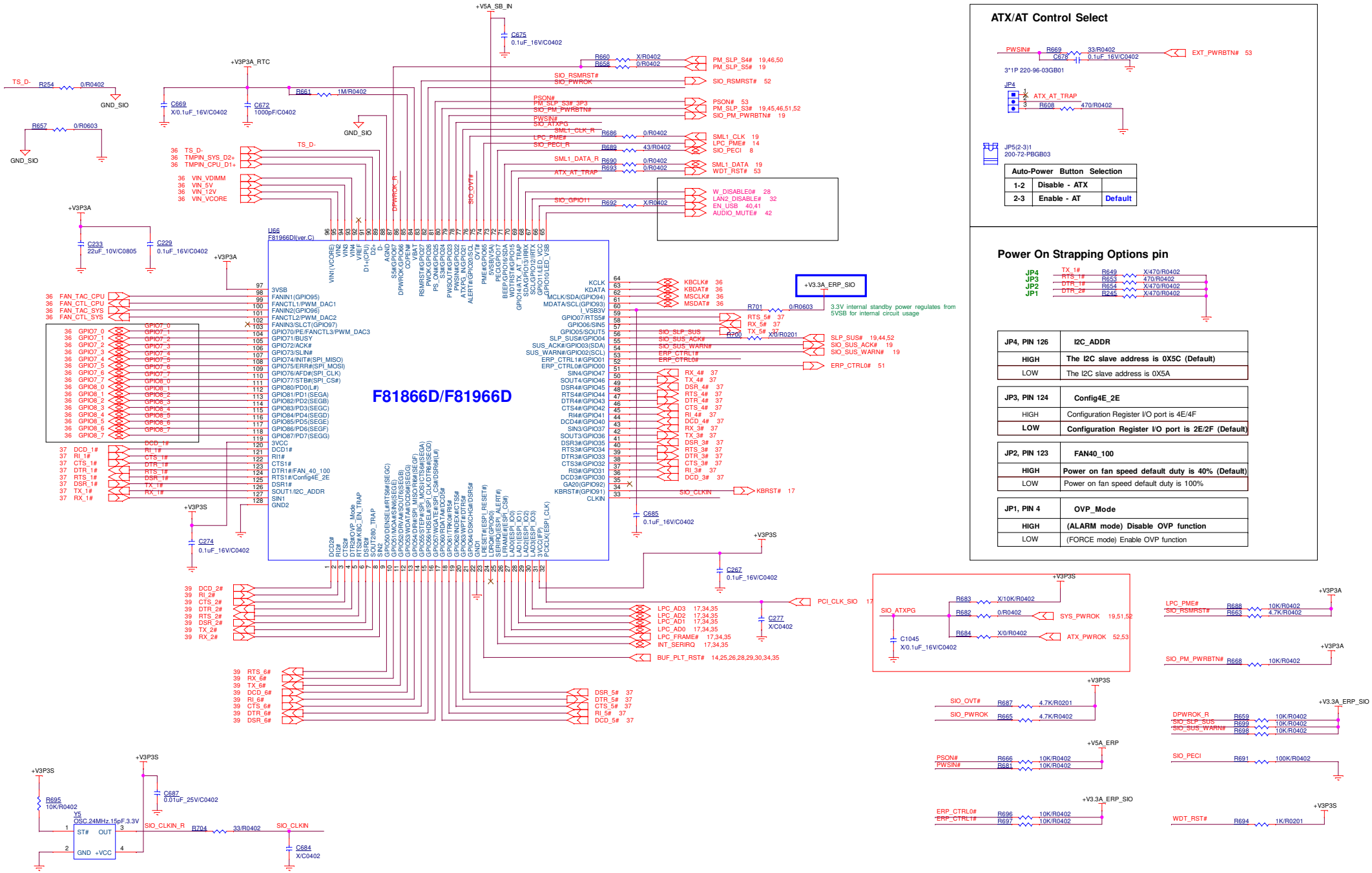
Pearsonville(i211) /Springville(i210)



AAEON An ASUS Company	Title: LAN2_INTEL I211		
	Size: Custom	Document Number: PCM-CFS	Rev: A0.2
	Date: Tuesday, September 03, 2013	Sheet: 32 of 54	

Hans



Title	Super I/O - FINTEK F81966
Size: Custom	Document Number: PCM-CFS
Rev:	A0.2
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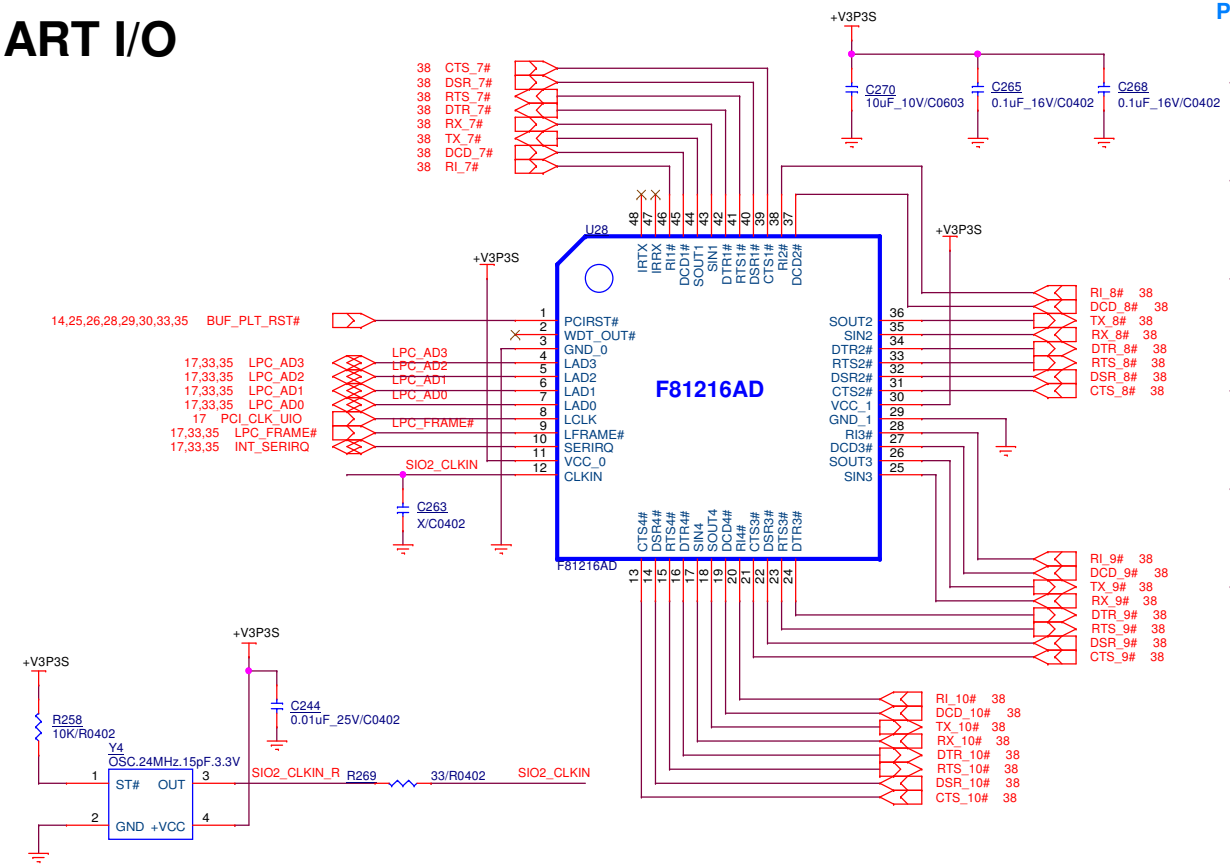
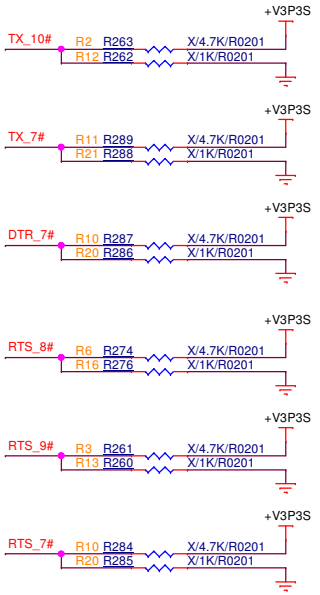
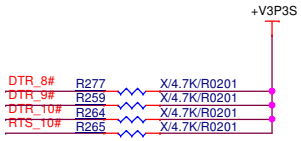
UART I/O



Power On Setting

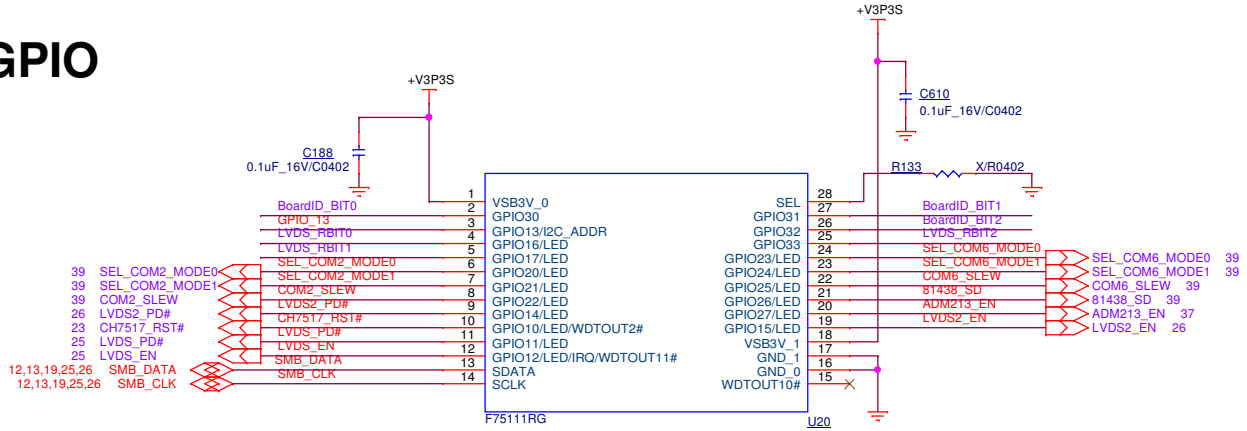




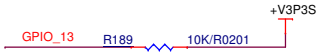
R6	R3	R9	Address	Entry Key
0	0	0	0x4e/0x4f	0x77
0	0	1	0x2e/0x2f	0x77
0	1	0	0x4e/0x4f	0xa0
0	1	1	0x2e/0x2f	0xa0
1	0	0	0x4e/0x4f	0x87
1	0	1	0x2e/0x2f	0x87
1	1	0	0x4e/0x4f	0x67
1	1	1	0x2e/0x2f	0x67

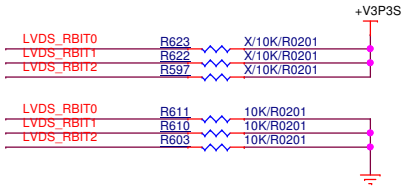
R16 is 0 when R6=1, R16 is 1 when R6=0.
R13 is 0 when R3=1, R13 is 1 when R3=0.
R19 is 0 when R9=1, R19 is 1 when R9=0.

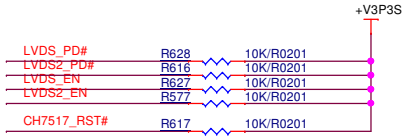
GPIO

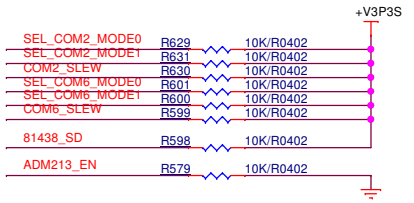


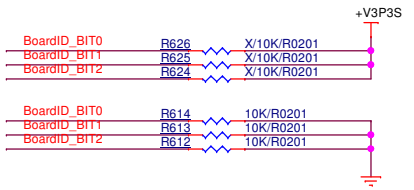
I2C Address	
GPIO13	Float : I2C Address = 0x9Ch
	High : I2C Address = 0x6Eh











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Title: UART I/O - FINTEK F81216

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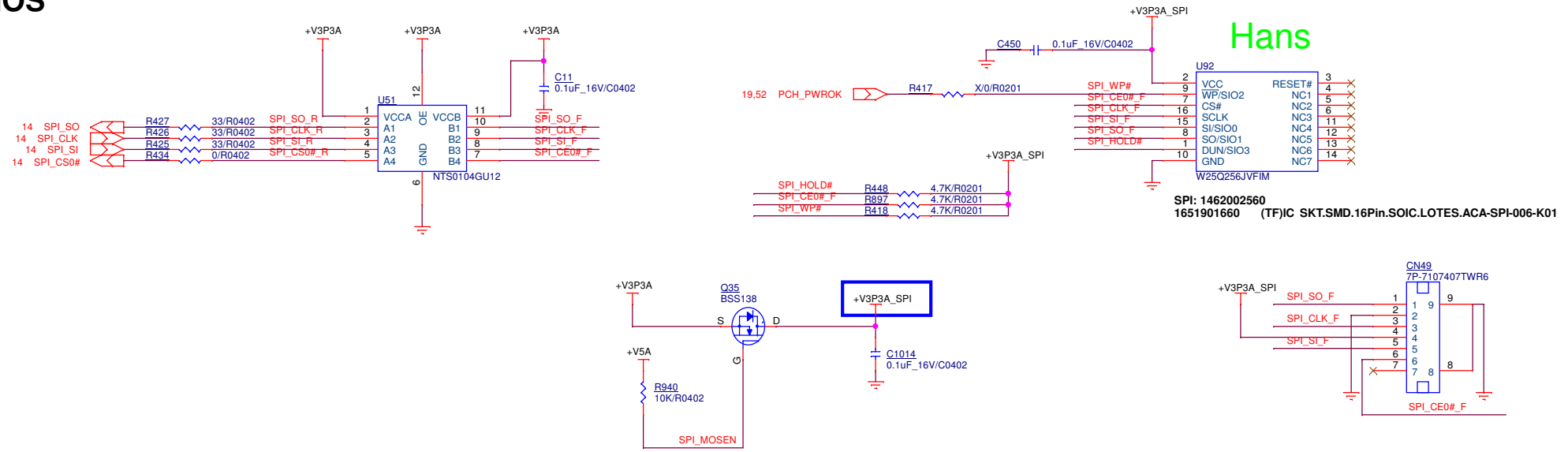
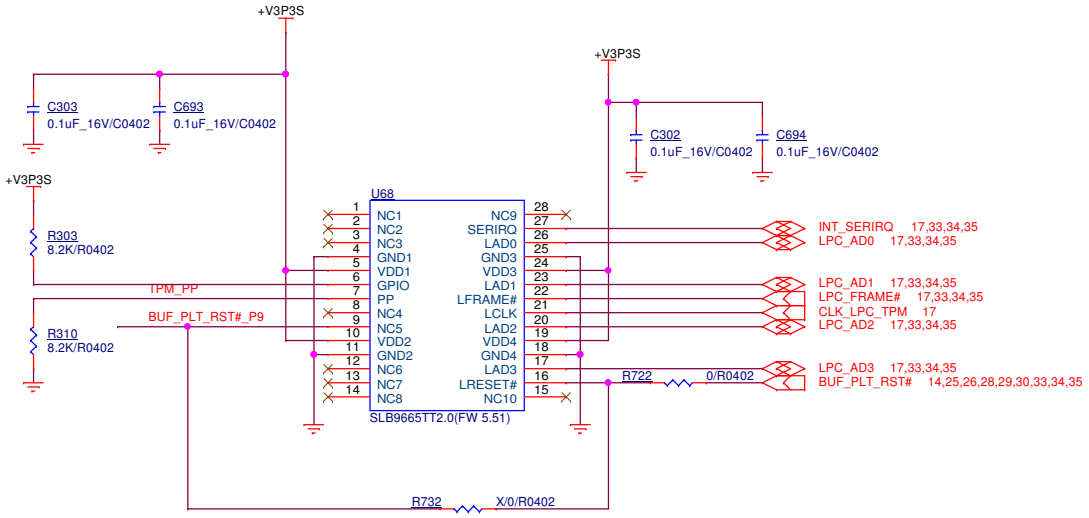
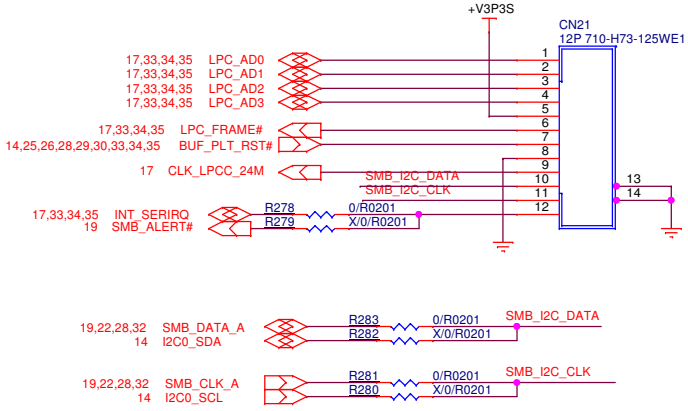
SPI BIOS



TPM



LPC Connector



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Title: SPI BIOS,LPC,TPM		
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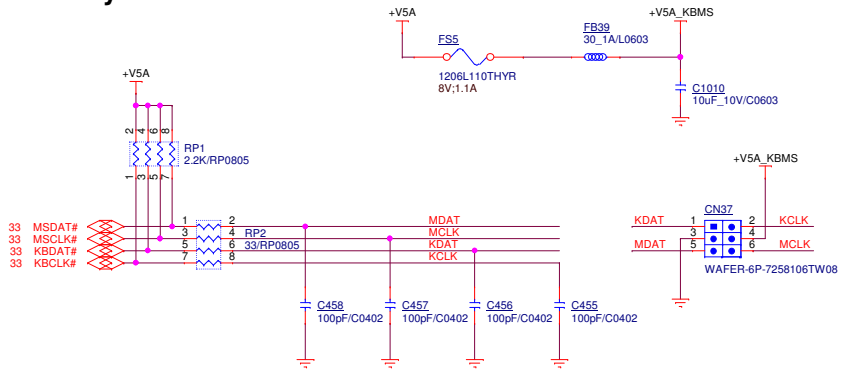
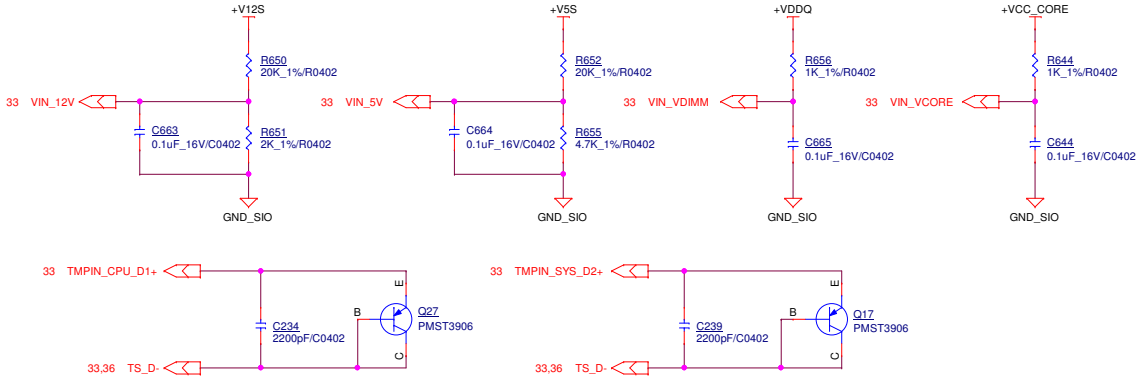
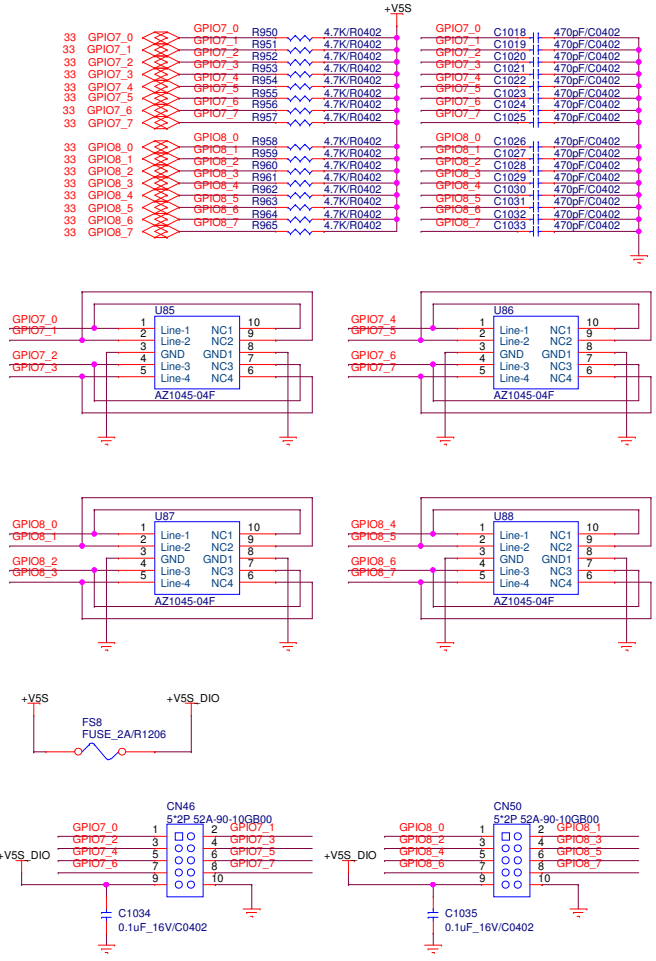
PS/2 Keyboard/Mouse



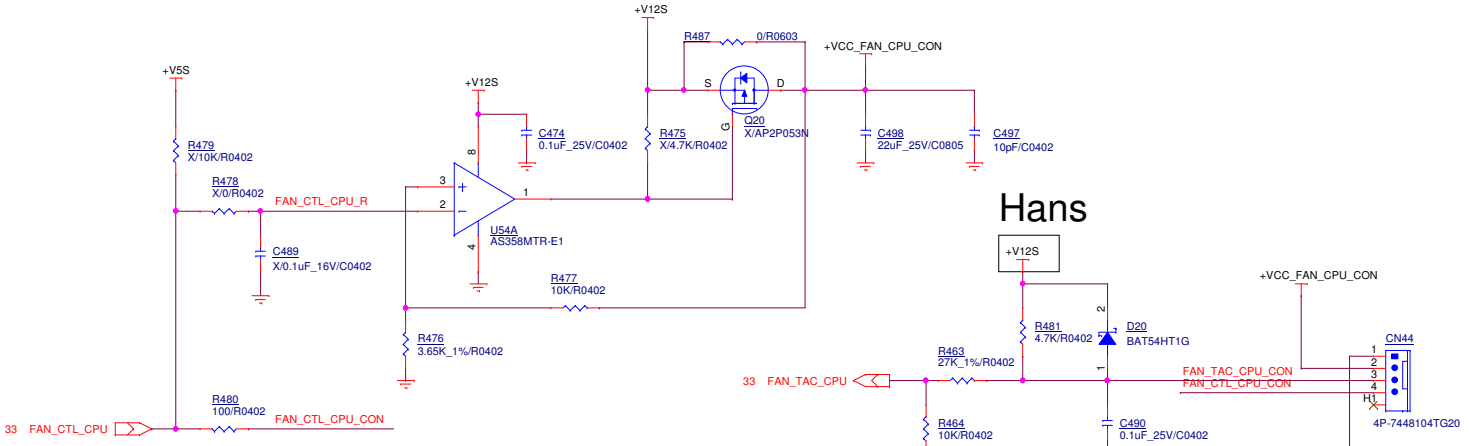
Voltage Monitor



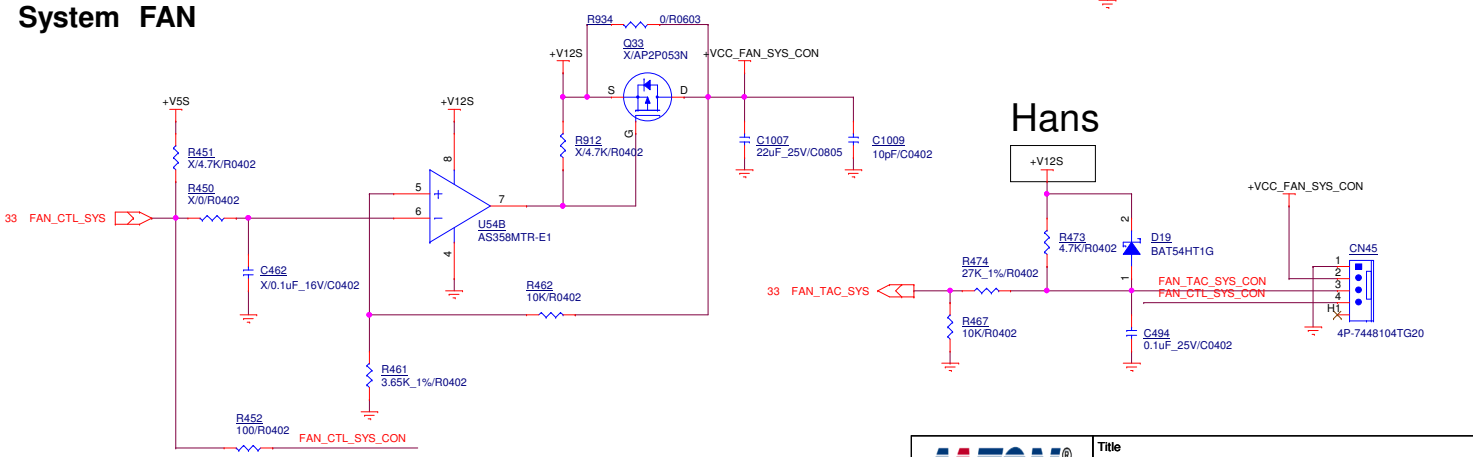
DIO



CPU FAN



System FAN



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Title: KB,MS,DIO,H/W Monitor,FAN

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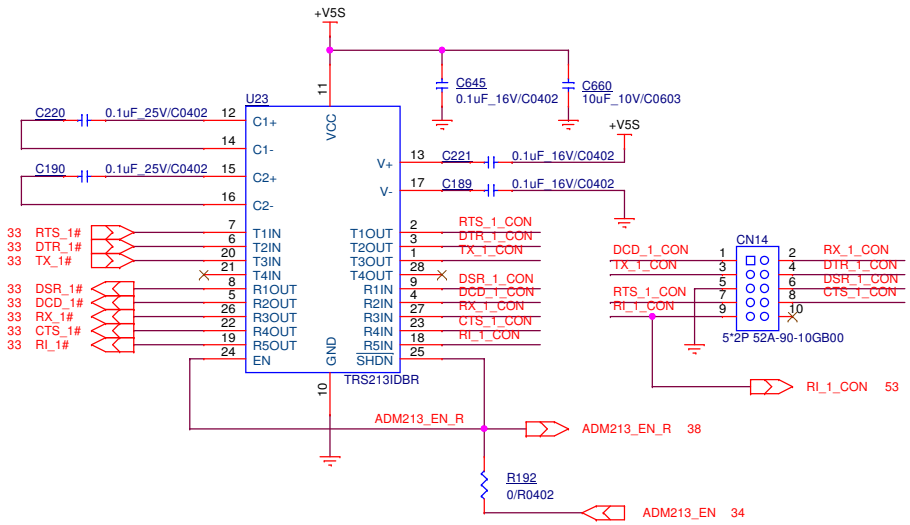
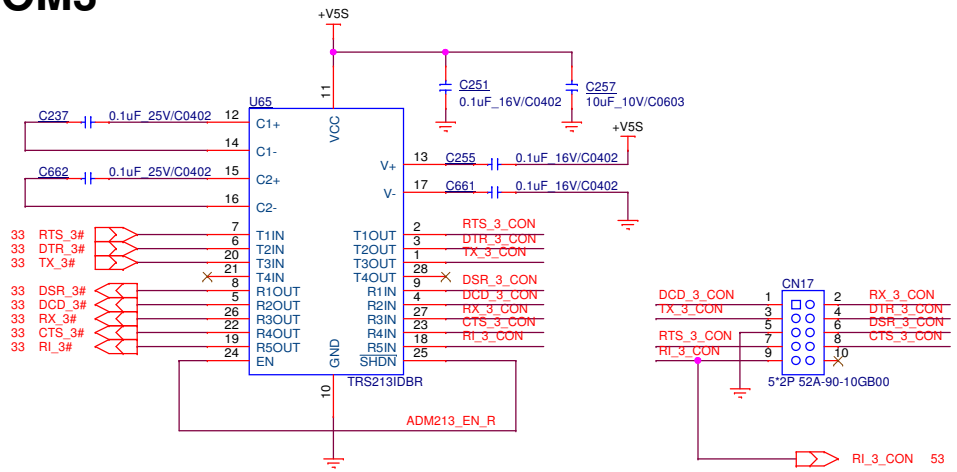
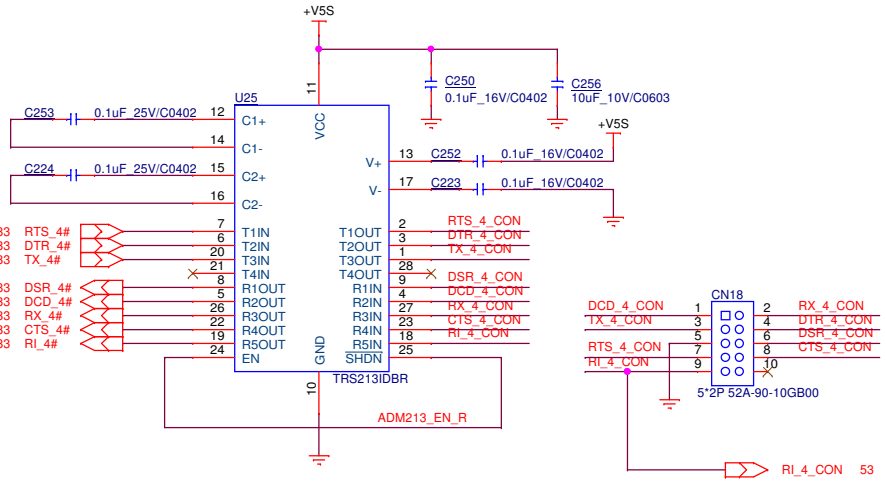
COM1



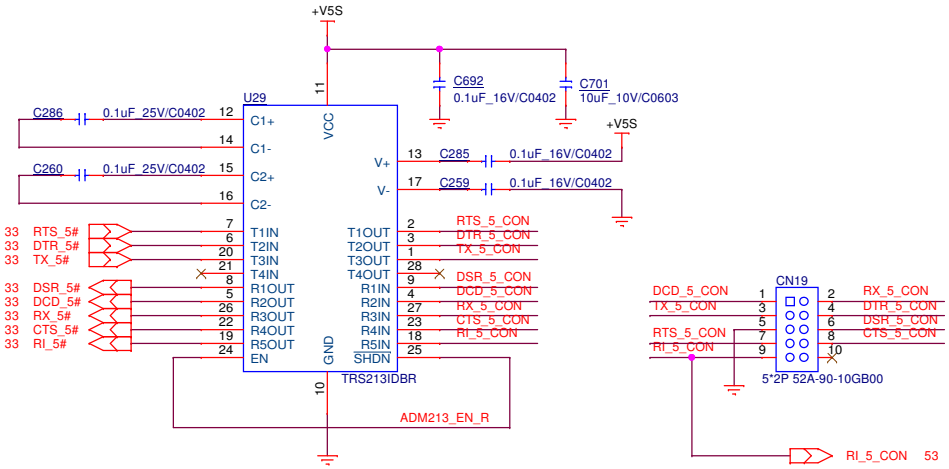
COM3



COM4



COM5



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Title: COM1,COM3,COM4,COM5		
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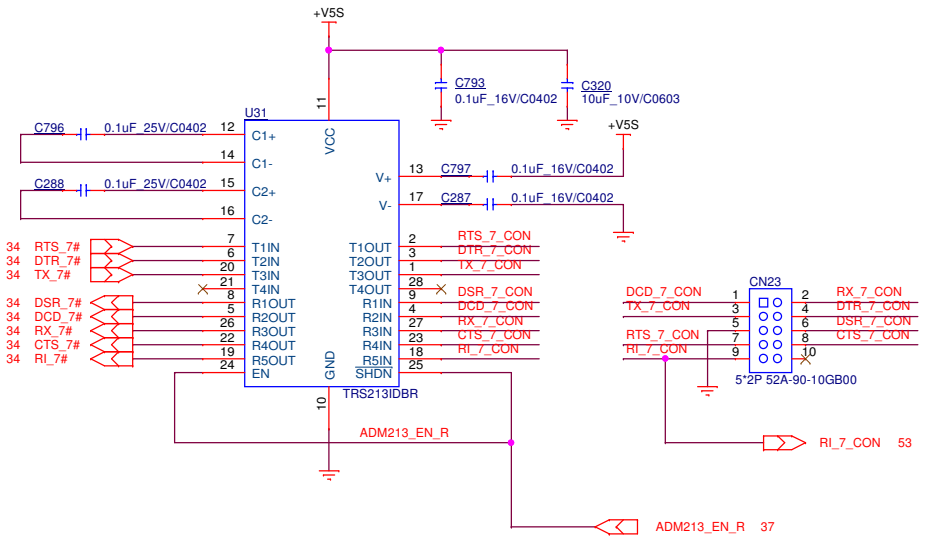
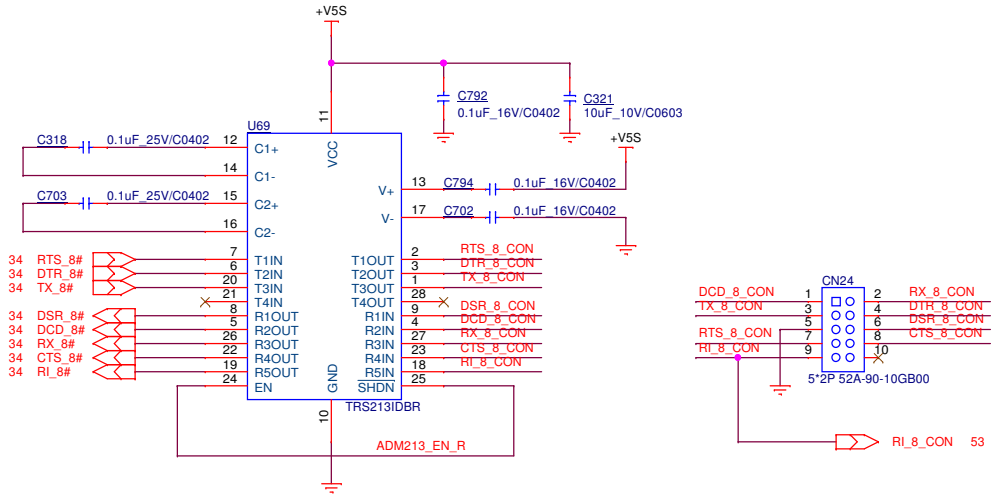
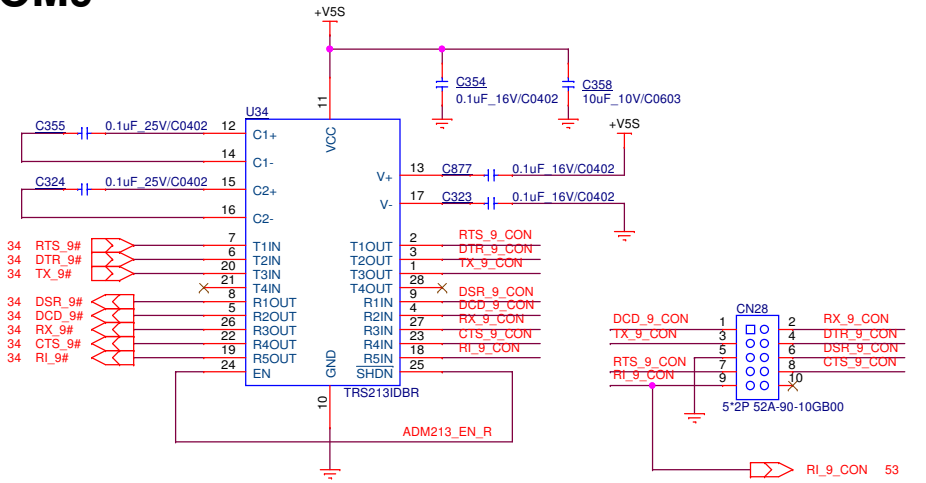
COM7



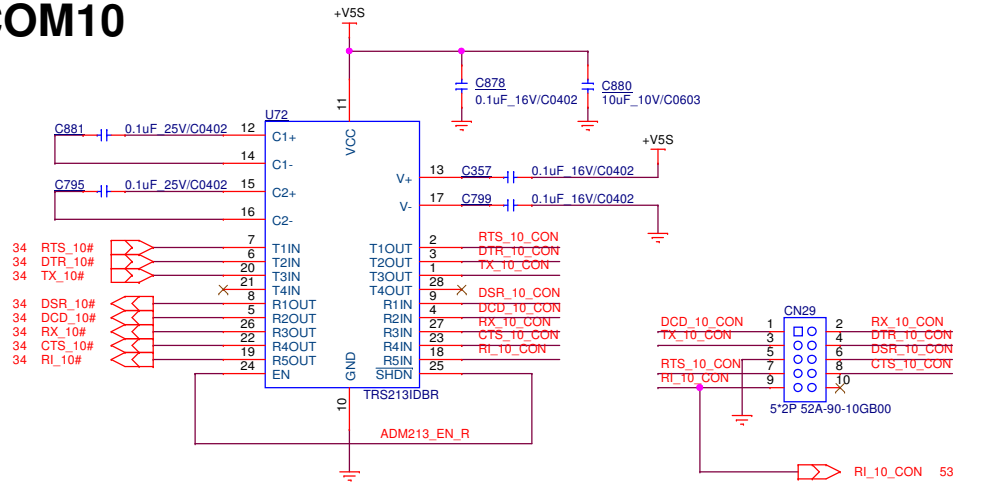
COM8



COM9



COM10



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Title: COM7,COM8,COM9,COM10		
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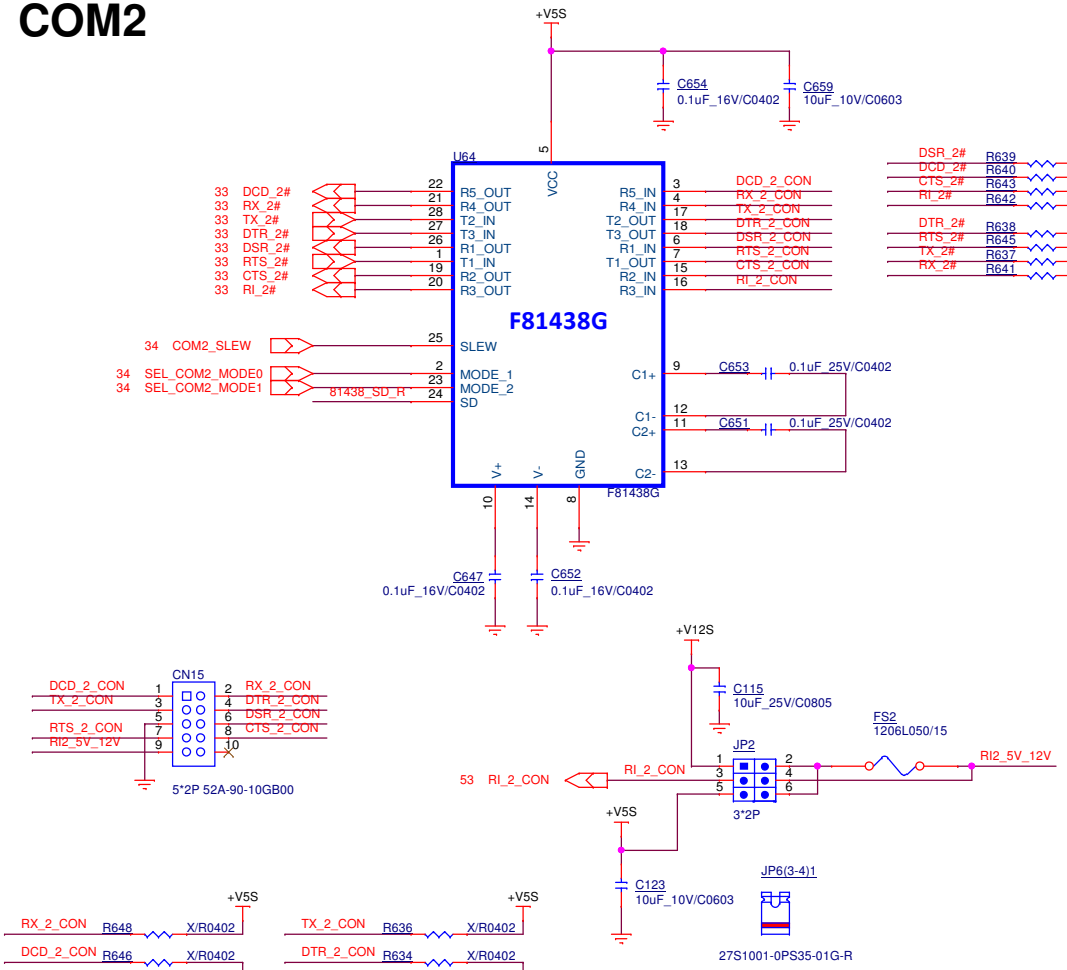
COM2



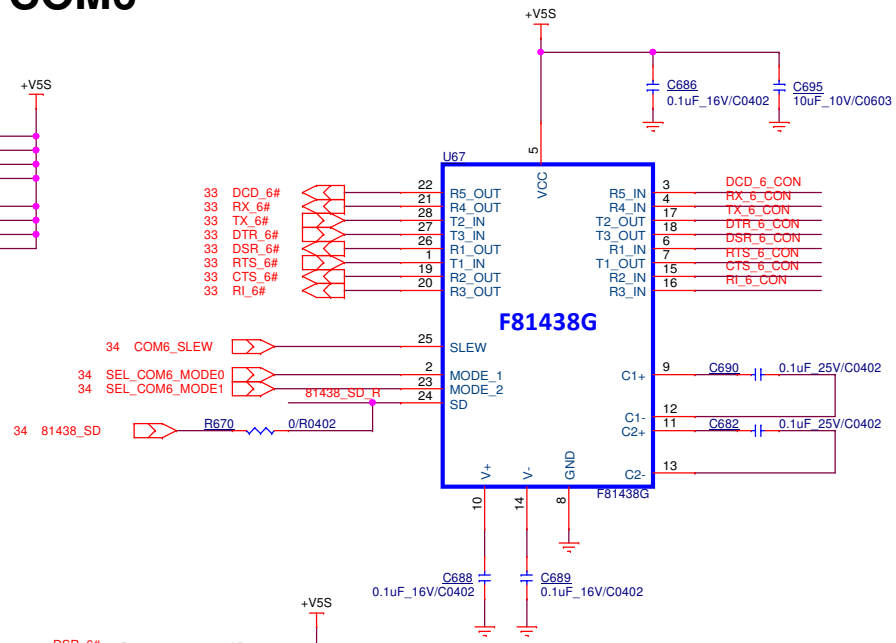
COM2 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

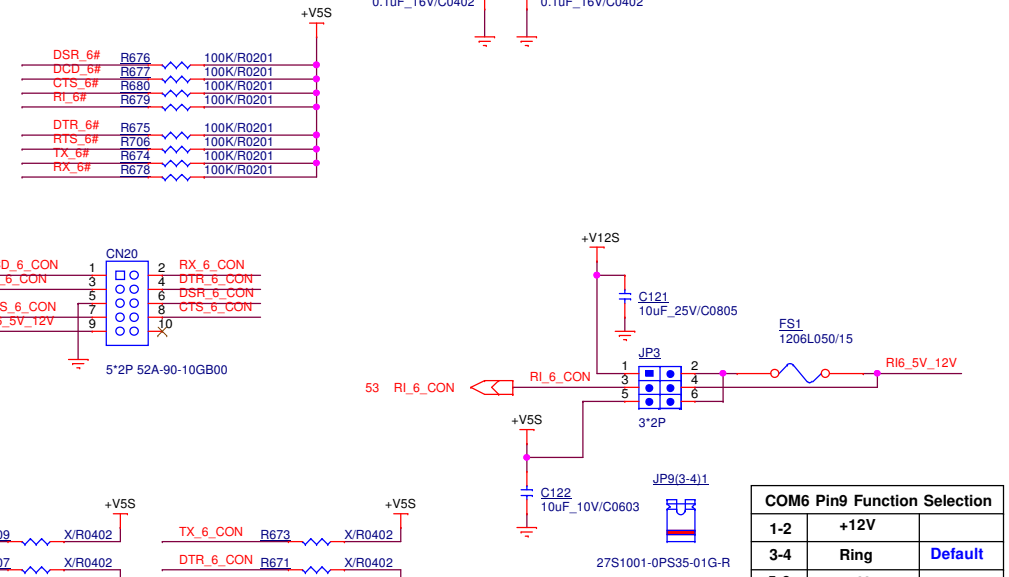
Serial Port 2 Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

Pin Mapping			
	RS-232	RS-485	RS-422
R1_IN	DSR		
T1_OUT	RTS		
T2_OUT	TX		RS422_RX+ (A)
T3_OUT	DTR		RS422_RX- (B)
R2_IN	CTS		
R3_IN	RI		
R4_IN	RX	RS485_D+ (A)	RS422_TX+ (A)
R5_IN	DCD	RS485_D- (B)	RS422_TX- (B)

COM6





COM6 Pin9 Function Selection		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

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Title: RS232/485/422: COM2,COM6

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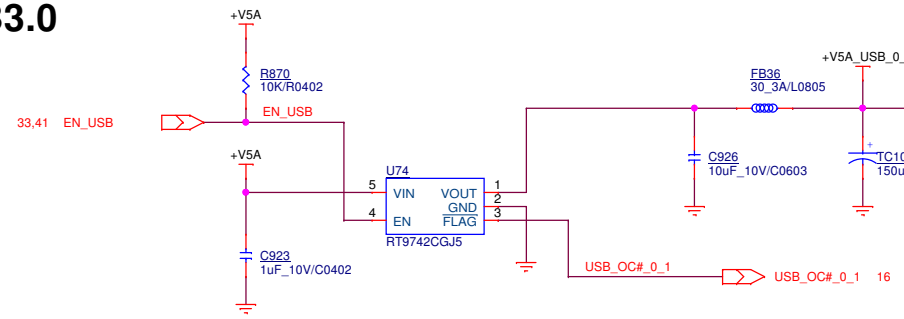
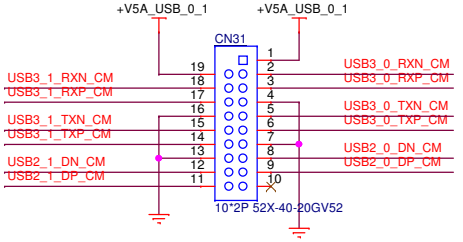
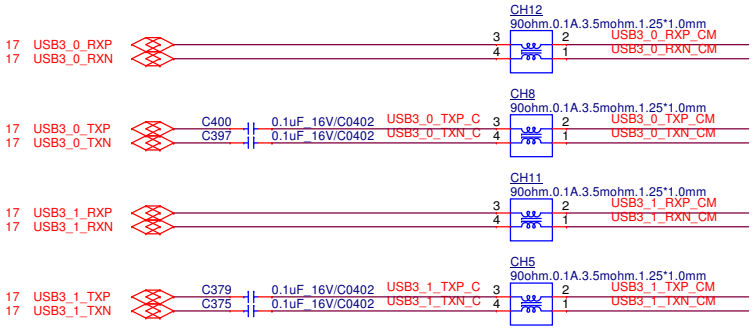
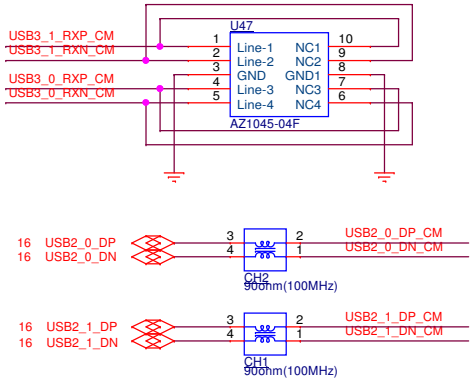
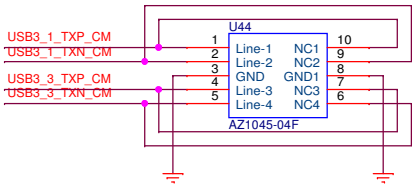
USB3.0

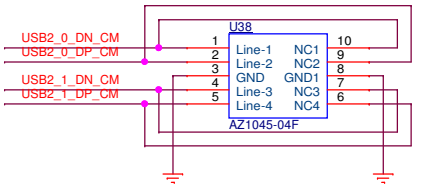


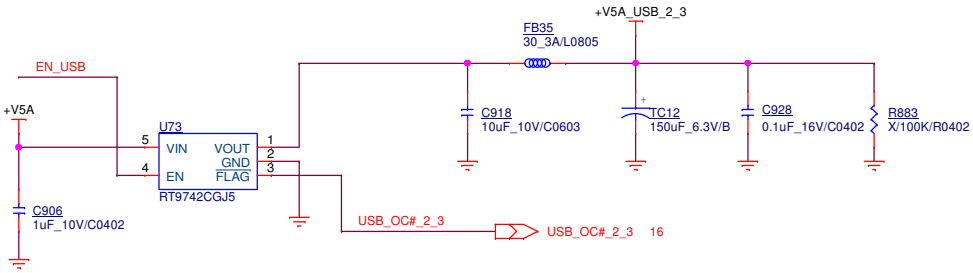


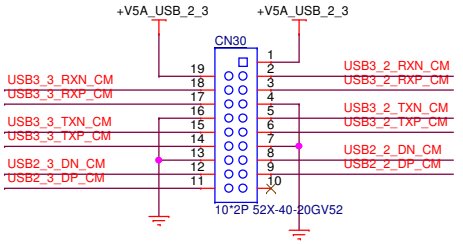


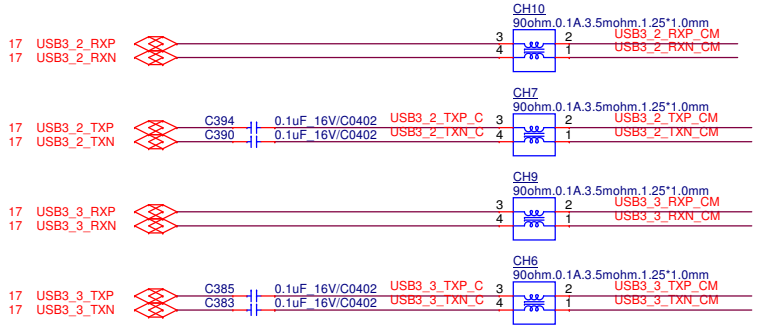


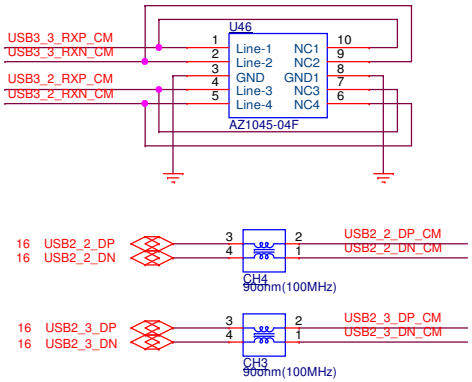


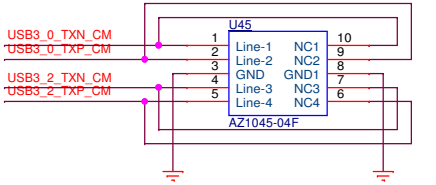


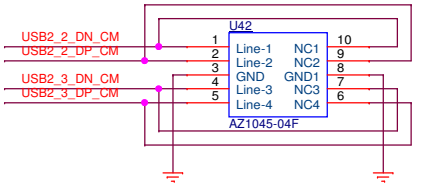












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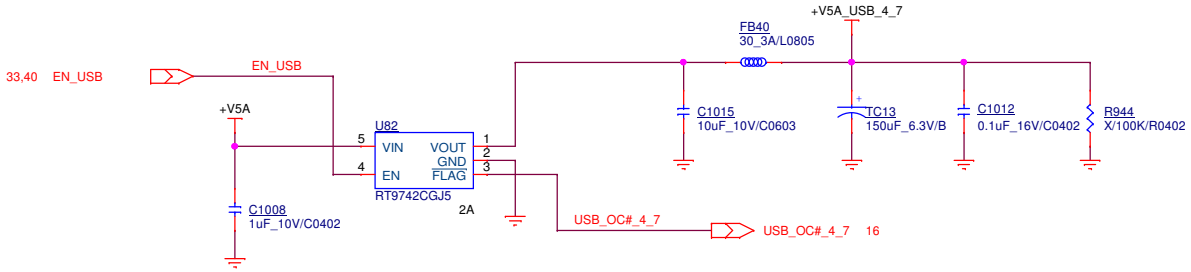

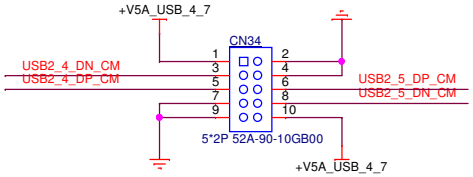

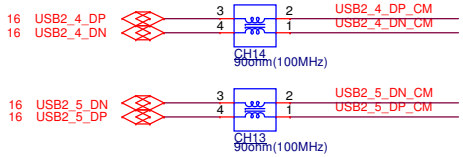

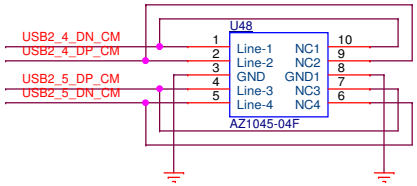

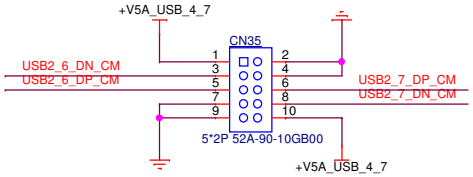

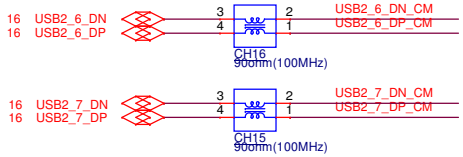

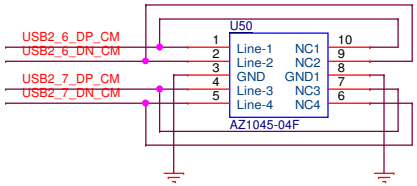

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Title
USB2.0 Port

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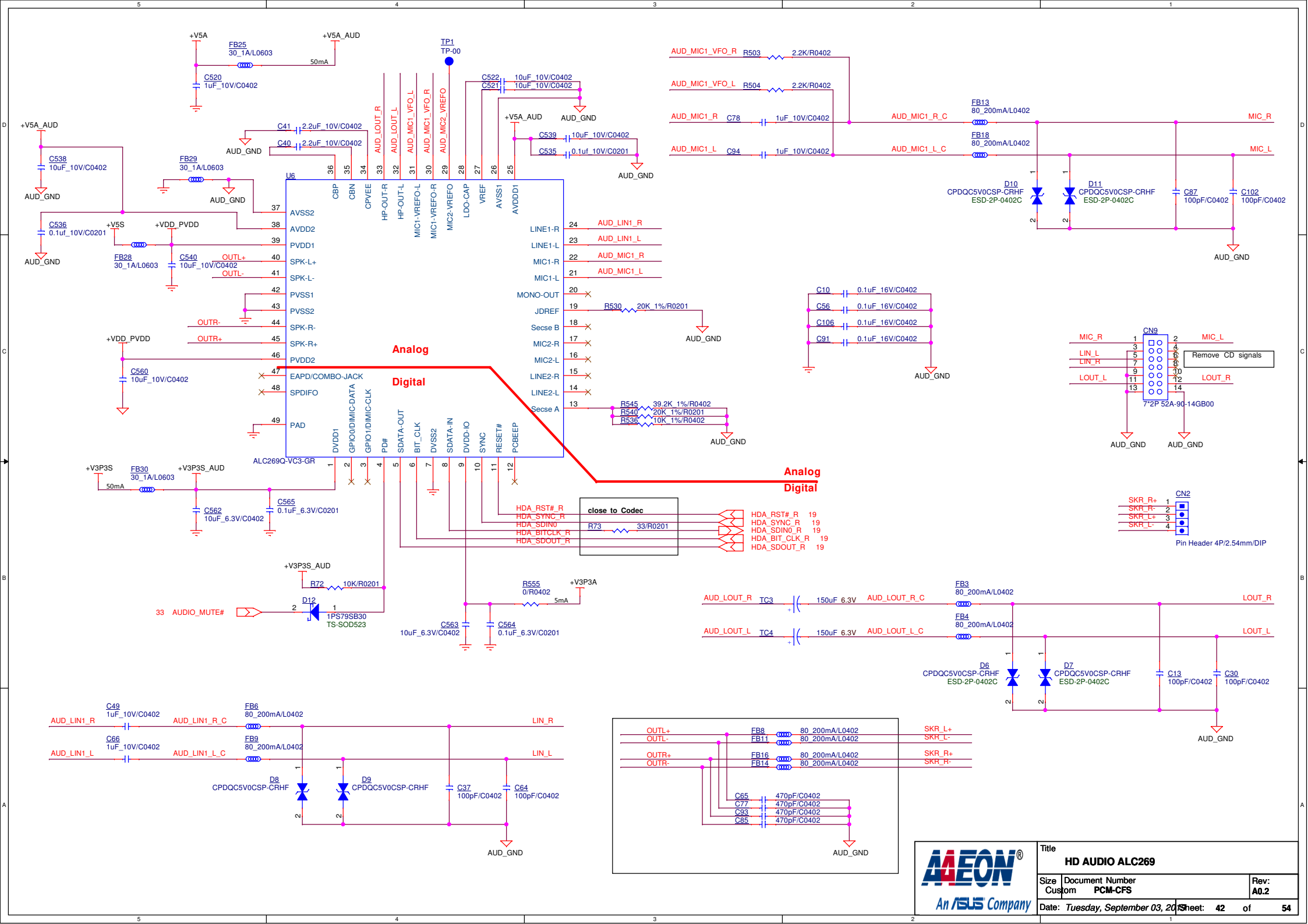
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FB25
30_1A/L0603
+V5A_AUD
50mA
C520
1uF_10V/C0402
TP1
TP-00
C522
10uF_10V/C0402
C521
10uF_10V/C0402
AUD_GND
+V5A_AUD
C539
10uF_10V/C0402
C535
0.1uf_10V/C0201
AUD_GND
C41
2.2uF_10V/C0402
C40
2.2uF_10V/C0402
AUD_GND
AUD_LOUT_R
AUD_LOUT_L
AUD_MIC1_VFO_L
AUD_MIC1_VFO_R
AUD_MIC2_VREFO
+V5A_AUD
C538
10uF_10V/C0402
AUD_GND
FB29
30_1A/L0603
AUD_GND
U6
CBP
CBN
CPVEE
HP-OUT-R
HP-OUT-L
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDDD1
AVSS2
AVDD2
PVDD1
SPK-L+
SPK-L-
PVSS1
PVSS2
SPK-R-
SPK-R+
PVDD2
EAPD/COMBO-JACK
SPDIFO
PAD
LINE1-R
LINE1-L
MIC1-R
MIC1-L
MONO-OUT
JDREF
Secse B
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Secse A
AUD_LIN1_R
AUD_LIN1_L
AUD_MIC1_R
AUD_MIC1_L
R530
20K_1%/R0201
AUD_GND
R545
39.2K_1%/R0402
R540
20K_1%/R0201
R536
10K_1%/R0402
AUD_GND
C536
0.1uf_10V/C0201
AUD_GND
+V5S
FB28
30_1A/L0603
+VDD_PVDD
C540
10uF_10V/C0402
OUTL+
OUTL-
OUTR-
OUTR+
+VDD_PVDD
C560
10uF_10V/C0402
DVDD1
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BIT_CLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
ALC269Q-VC3-GR
Analog
Digital
Analog
Digital
+V3P3S
50mA
FB30
30_1A/L0603
+V3P3S_AUD
C562
10uF_6.3V/C0402
C565
0.1uF_6.3V/C0201
HDA_RST#_R
HDA_SYNC_R
HDA_SDIN0
HDA_BITCLK_R
HDA_SDOUT_R
close to Codec
R73
33/R0201
HDA_RST#_R 19
HDA_SYNC_R 19
HDA_SDIN0_R 19
HDA_BIT_CLK_R 19
HDA_SDOUT_R 19
+V3P3S_AUD
R72
10K/R0201
33 AUDIO_MUTE#
D12
1PS79SB30
TS-SOD523
R555
0/R0402
+V3P3A
5mA
C563
10uF_6.3V/C0402
C564
0.1uF_6.3V/C0201
AUD_MIC1_VFO_R
R503
2.2K/R0402
AUD_MIC1_VFO_L
R504
2.2K/R0402
AUD_MIC1_R
C78
1uF_10V/C0402
AUD_MIC1_L
C94
1uF_10V/C0402
AUD_MIC1_R_C
AUD_MIC1_L_C
FB13
80_200mA/L0402
FB18
80_200mA/L0402
MIC_R
MIC_L
D10
CPDQC5V0CSP-CRHF
ESD-2P-0402C
D11
CPDQC5V0CSP-CRHF
ESD-2P-0402C
C87
100pF/C0402
C102
100pF/C0402
AUD_GND
C10
0.1uF_16V/C0402
C56
0.1uF_16V/C0402
C106
0.1uF_16V/C0402
C91
0.1uF_16V/C0402
AUD_GND
CN9
MIC_R
LIN_L
LIN_R
LOUT_L
MIC_L
LOUT_R
Remove CD signals
7*2P 52A-90-14GB00
AUD_GND
AUD_GND
CN2
SKR_R+
SKR_R-
SKR_L+
SKR_L-
Pin Header 4P/2.54mm/DIP
AUD_LOUT_R
AUD_LOUT_L
TC3
TC4
150uF 6.3V
AUD_LOUT_R_C
AUD_LOUT_L_C
FB3
80_200mA/L0402
FB4
80_200mA/L0402
LOUT_R
LOUT_L
D6
CPDQC5V0CSP-CRHF
ESD-2P-0402C
D7
CPDQC5V0CSP-CRHF
ESD-2P-0402C
C13
100pF/C0402
C30
100pF/C0402
AUD_GND
AUD_LIN1_R
AUD_LIN1_L
C49
1uF_10V/C0402
C66
1uF_10V/C0402
AUD_LIN1_R_C
AUD_LIN1_L_C
FB6
80_200mA/L0402
FB9
80_200mA/L0402
LIN_R
LIN_L
D8
CPDQC5V0CSP-CRHF
D9
CPDQC5V0CSP-CRHF
C37
100pF/C0402
C64
100pF/C0402
AUD_GND
OUTL+
OUTL-
OUTR+
OUTR-
FB8
FB11
FB16
FB14
80_200mA/L0402
SKR_L+
SKR_L-
SKR_R+
SKR_R-
C65
C77
C93
C85
470pF/C0402
AUD_GND
AAEON
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HD AUDIO ALC269
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Custom
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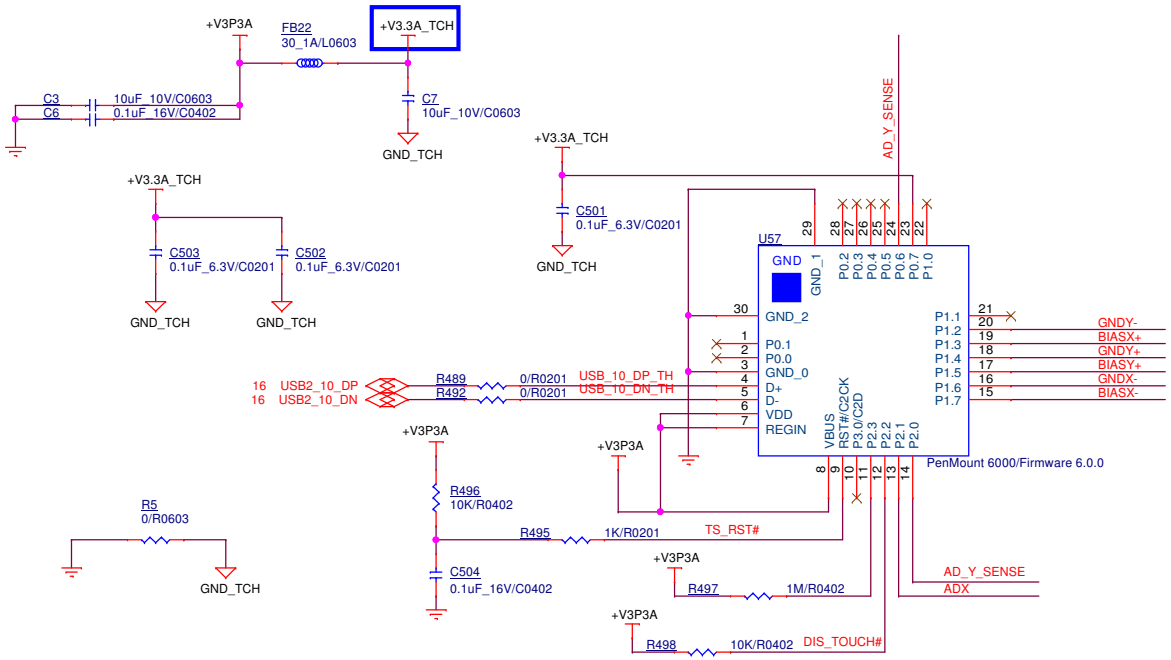
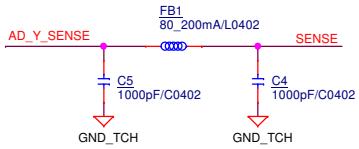
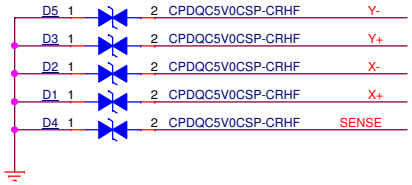
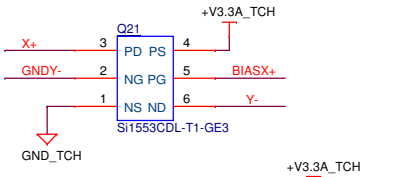
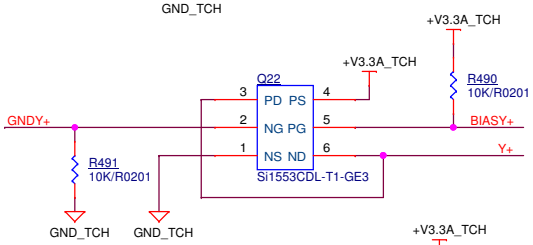
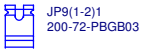




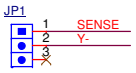


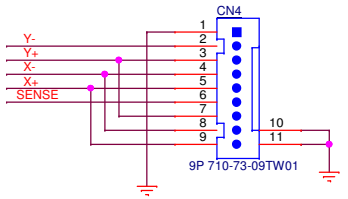






4,5,8 Wire Selection		
1-2	4,8 wire	Default
2-3	5 wire	





CN	Touch Screen Lines		
	8-Wire	4-Wire	5-Wire
PIN9	Right Sense	N/A	N/A
PIN8	Left Sense	N/A	N/A
PIN7	Bottom Sense	N/A	N/A
PIN6	TOP Sense	N/A	Sense(S)
PIN5	Right Excite	Right	LR(X)
PIN4	Left Excite	Left	LL(L)
PIN3	Bottom Excite	Bottom	UR(H)
PIN2	Top Excite	Top	UL(Y)
PIN1	GND	GND	GND

<Core Design>

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Title: TOUCH PANEL

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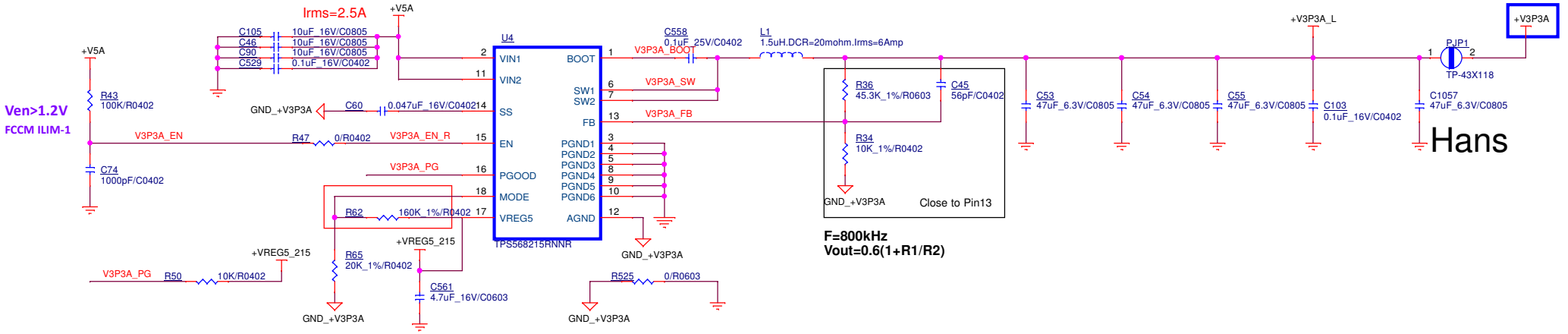
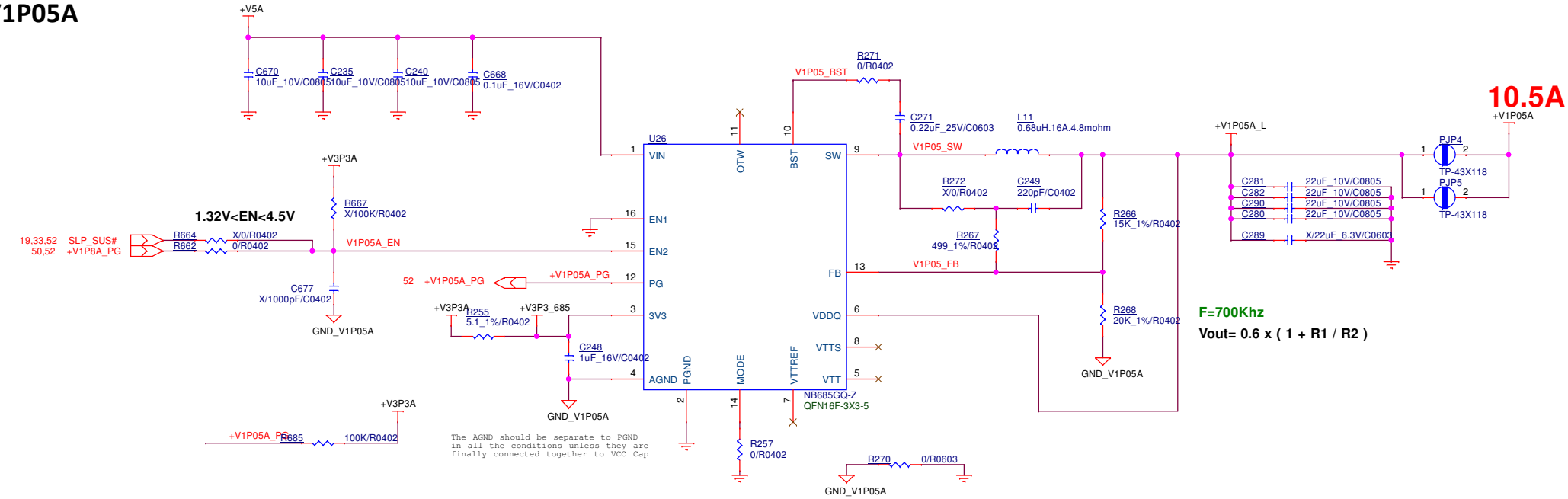
+V3P3A



+V1P05A



<Variant Name>

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Title: Power VR : +V3P3A, +V1P05A		
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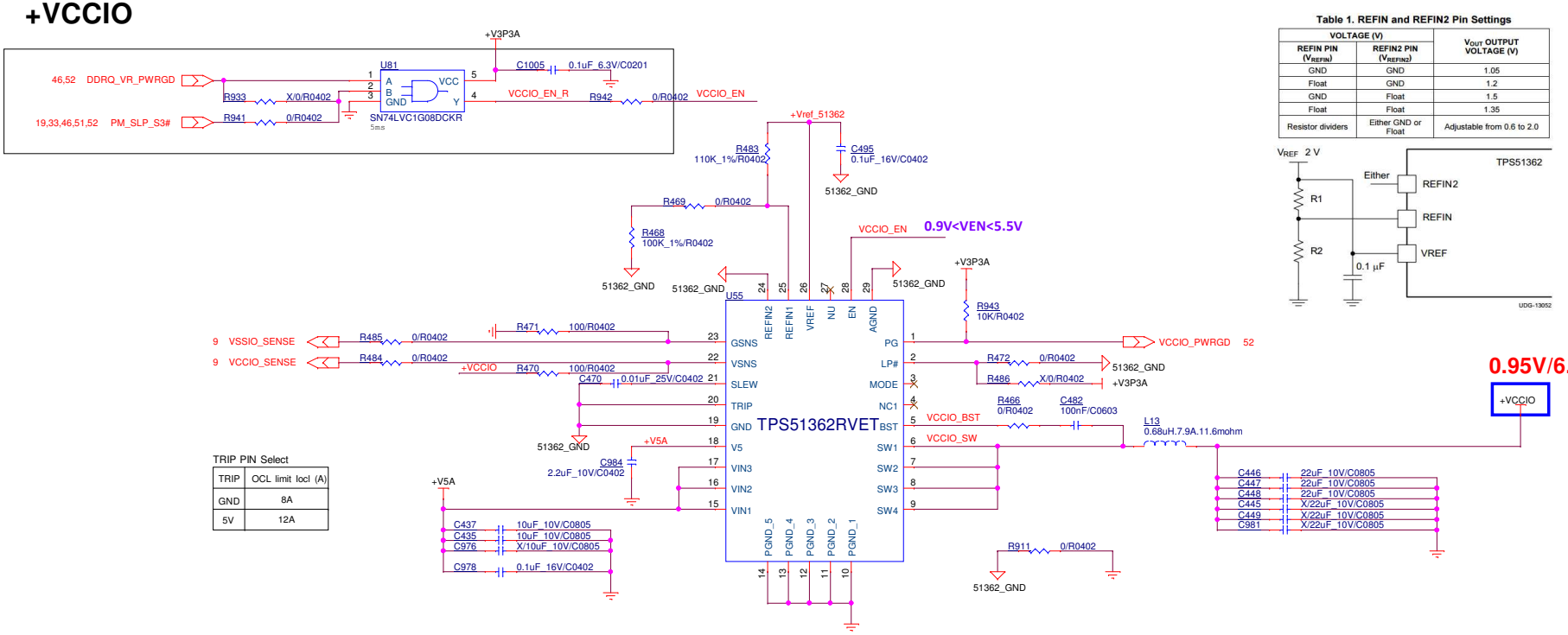
+VCCIO



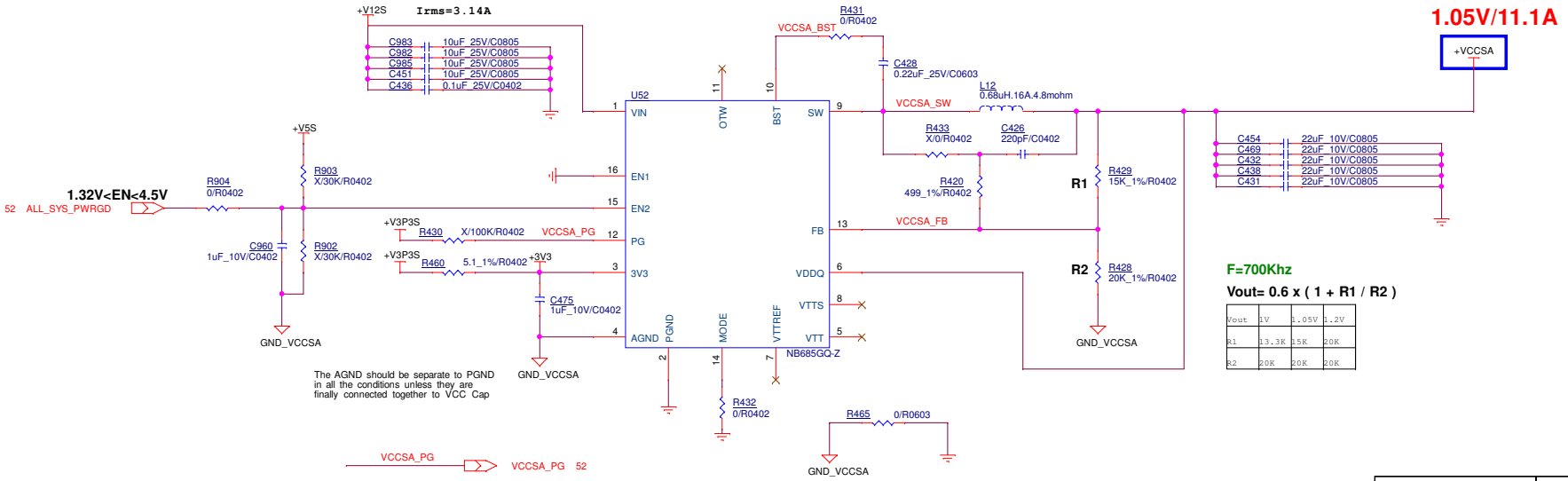
TRIP PIN Select

TRIP	OCL limit Iocl (A)
GND	8A
5V	12A

Table 1. REFIN and REFIN2 Pin Settings

VOLTAGE (V)		V_{OUT} OUTPUT VOLTAGE (V)
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

+VCCSA



Vout	1V	1.05V	1.2V
R1	13.3K	15K	20K
R2	20K	20K	20K

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Title: +VCCIO/+VCCSA

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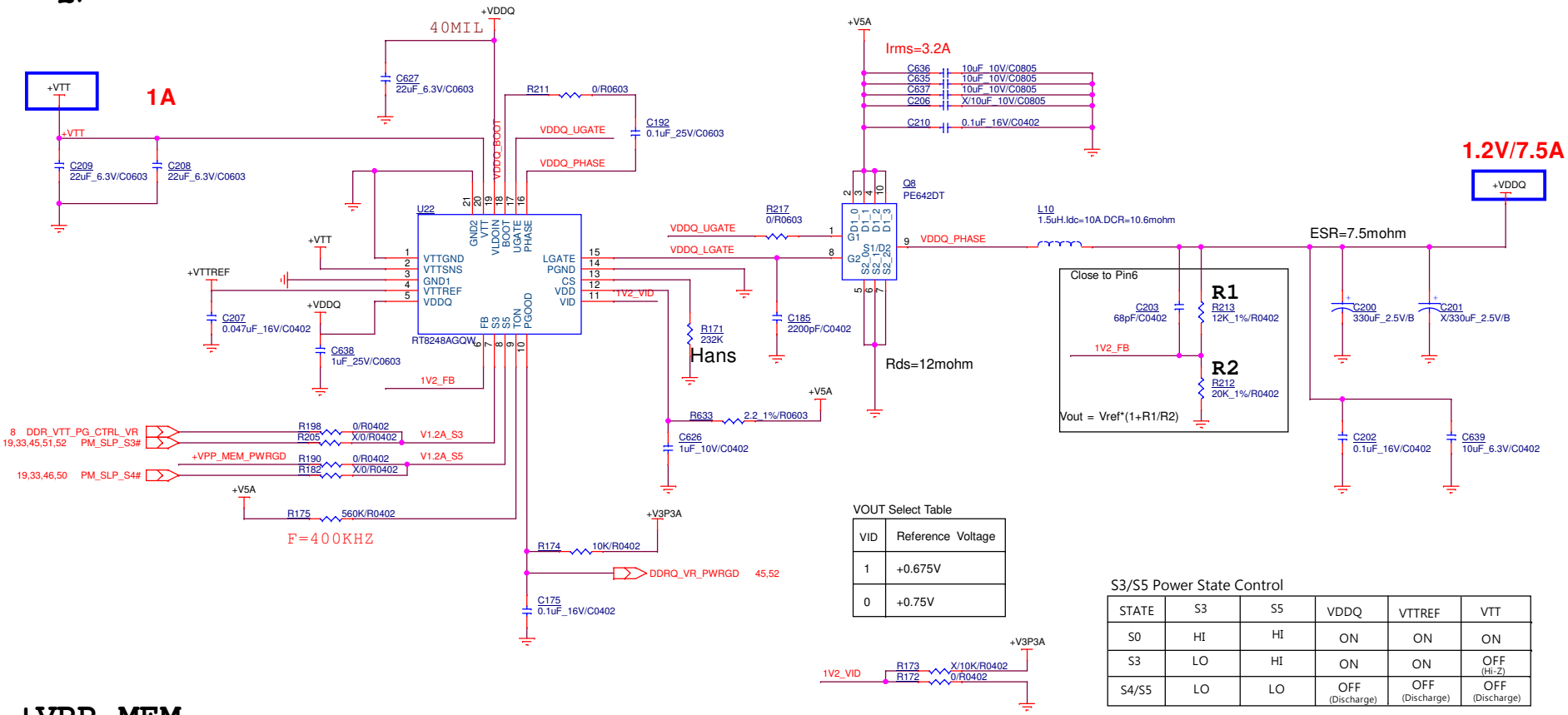
+VDDQ/+VTT



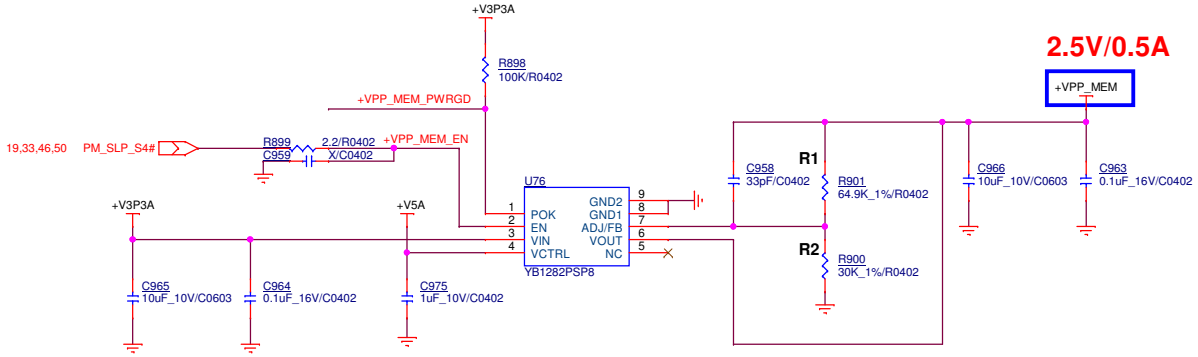
VOUT Select Table

VID	Reference Voltage
1	+0.675V
0	+0.75V

S3/S5 Power State Control

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF (Hi-Z)
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+VPP_MEM



Vout= 0.8 x (1 + R1 / R2)

Vout	1V	1.05V	1.15V	1.2V	1.24V	1.35V	1.5V	1.8V	2.5V
R1	11K	16K	13.3K	15.4K	15K	13.7K	27K	25.5K	64.9K
R2	40.2K	51K	30.1K	30K	27K	19.6K	30K	20K	30K

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Title: +VDDQ/+VTT/+VPP_MEM

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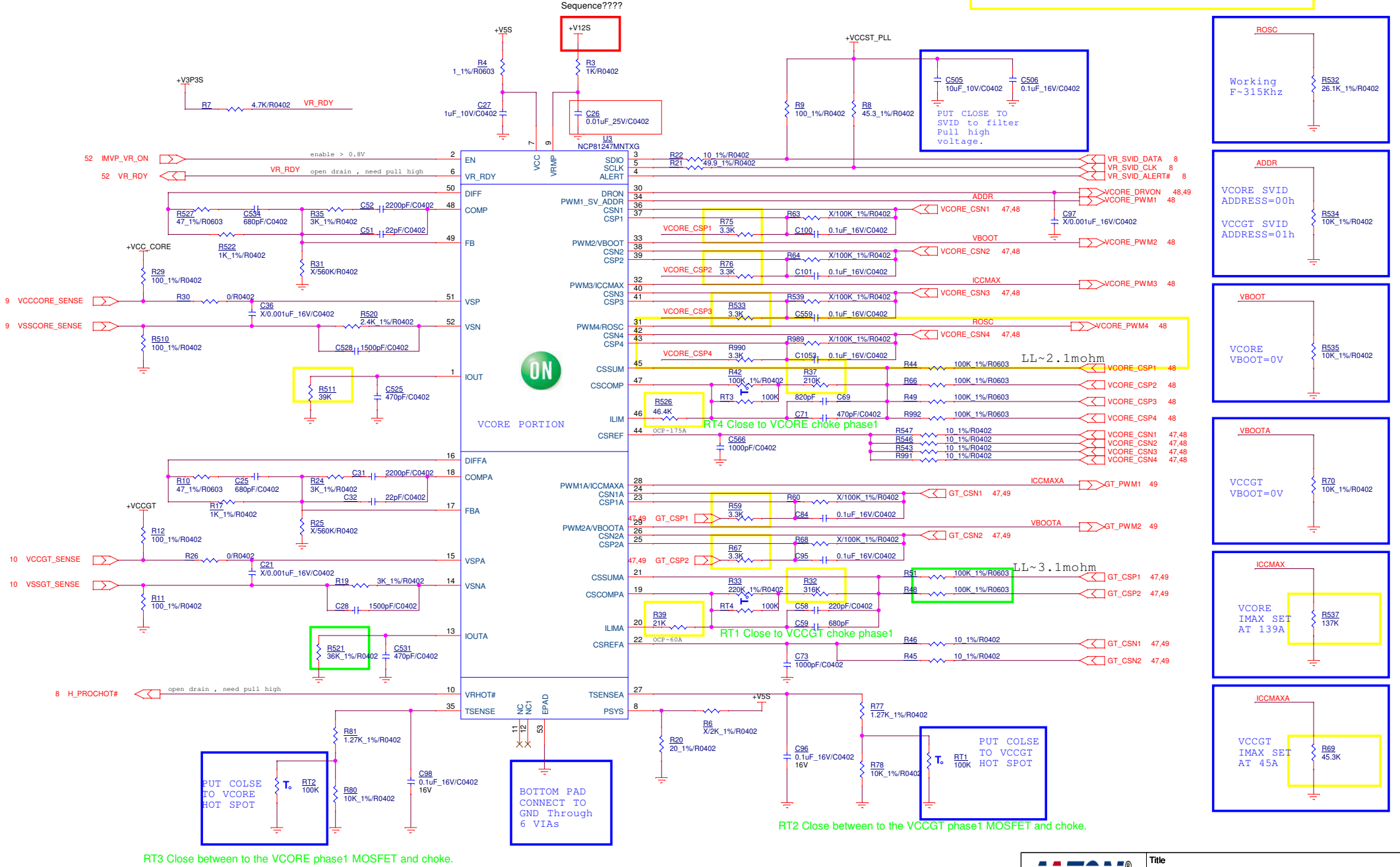
+VCC_CORE/+VCC_GT

S-Line 62 35W CPU power spec
Vcore ICCMAX=138A , TDC=100A , Loadline=2.1m ohm
VCCGT ICCMAX=45A , TDC=30A , Loadline=3.1m ohm

Sequence????



Title	ON-SEMI +VCC_CORE/+VCC_GT		
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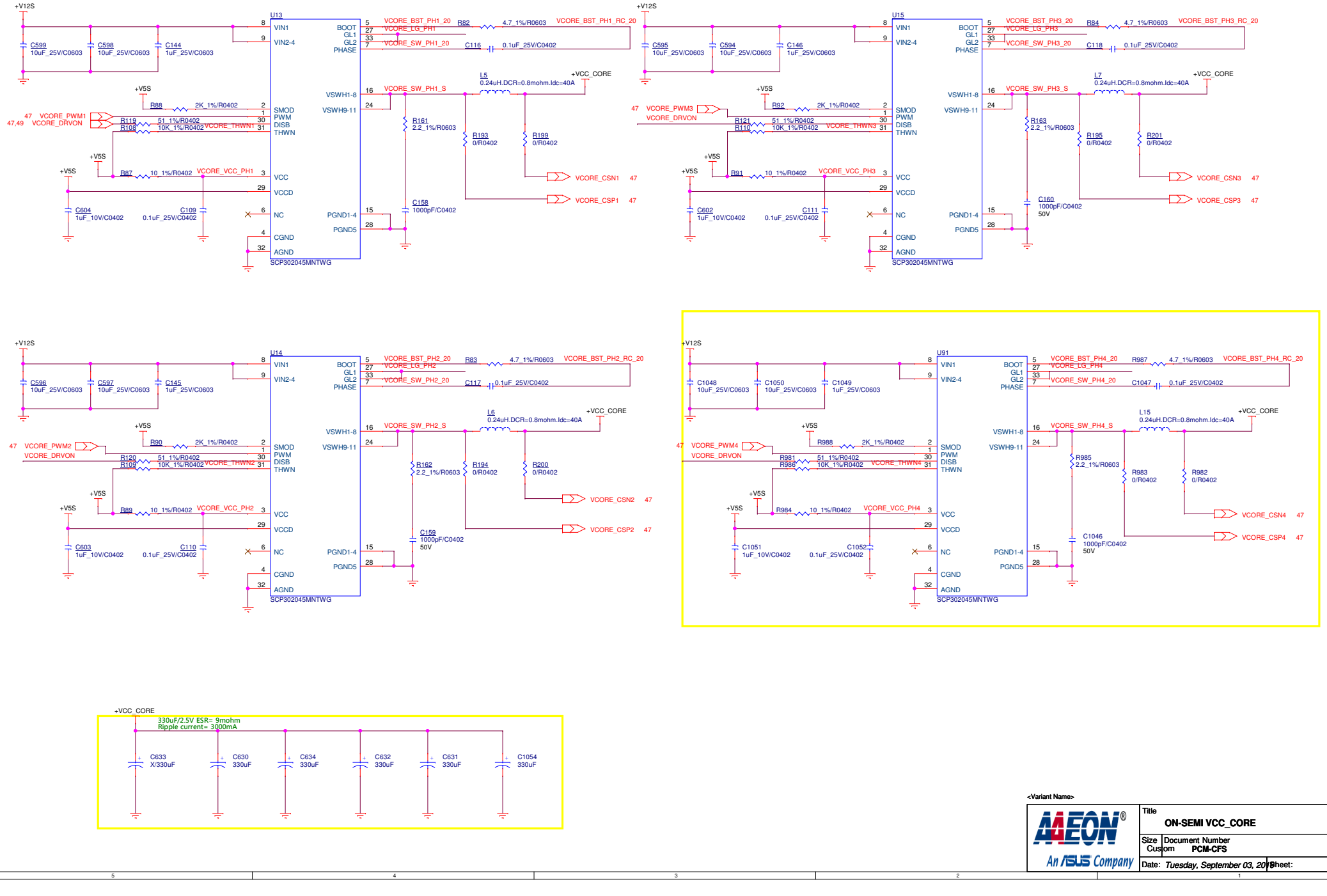
0 ~ 1.52V , ICCMAX = 138A



<Variant Name>

AAEON An ASUS Company

Title: ON-SEMI VCC_CORE		
Size: Custom	Document Number: PCM-CFS	Rev: A0.2
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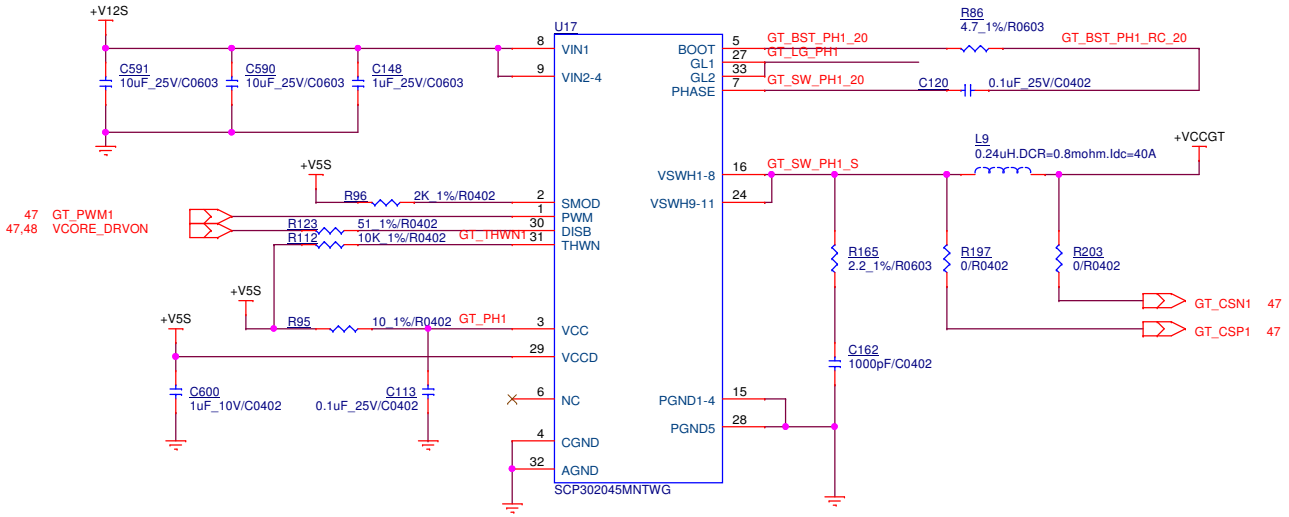
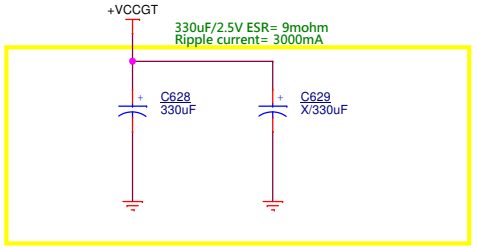
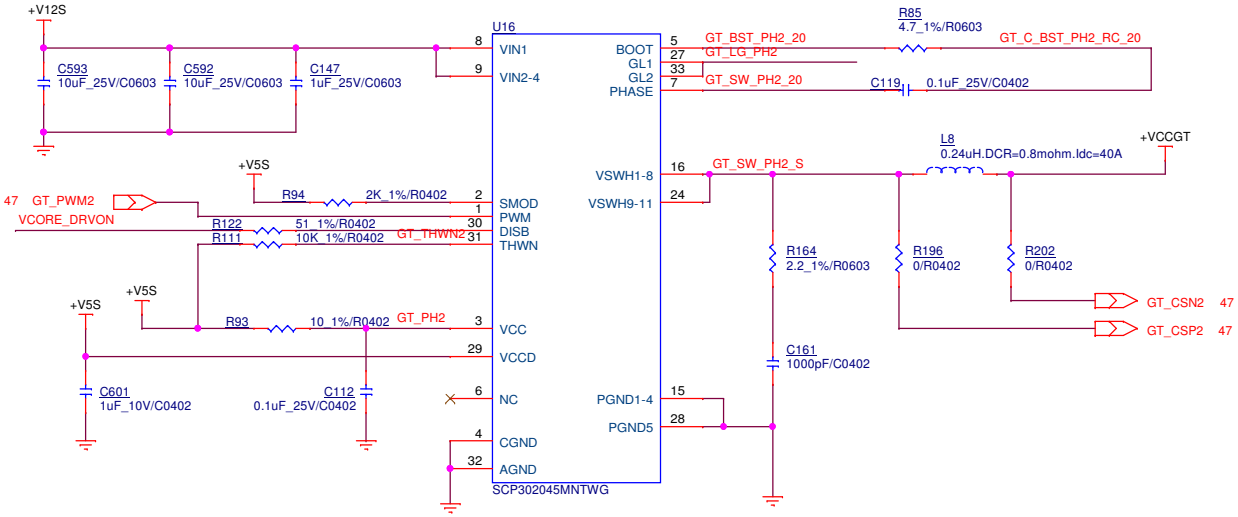
0 ~ 1.52V , ICCMAX = 45A







<Variant Name>

AAEON An ASUS Company

Title: ON-SEMI VCC_GT

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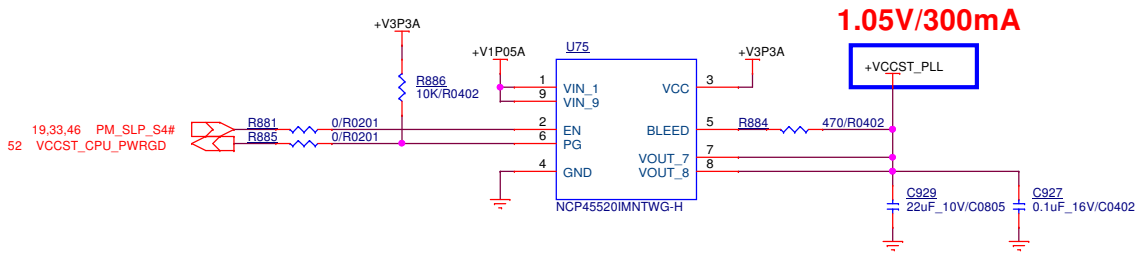
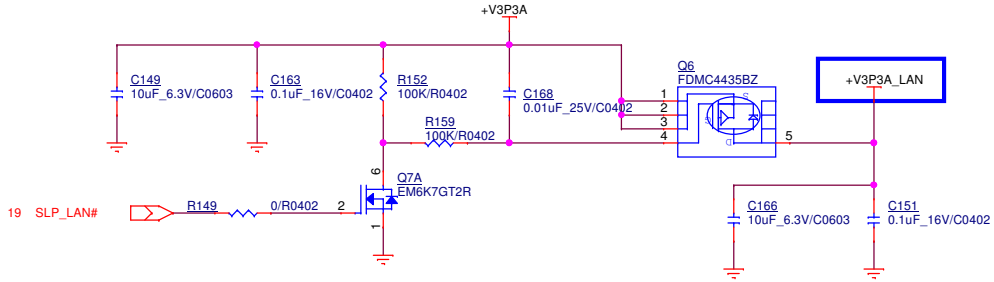
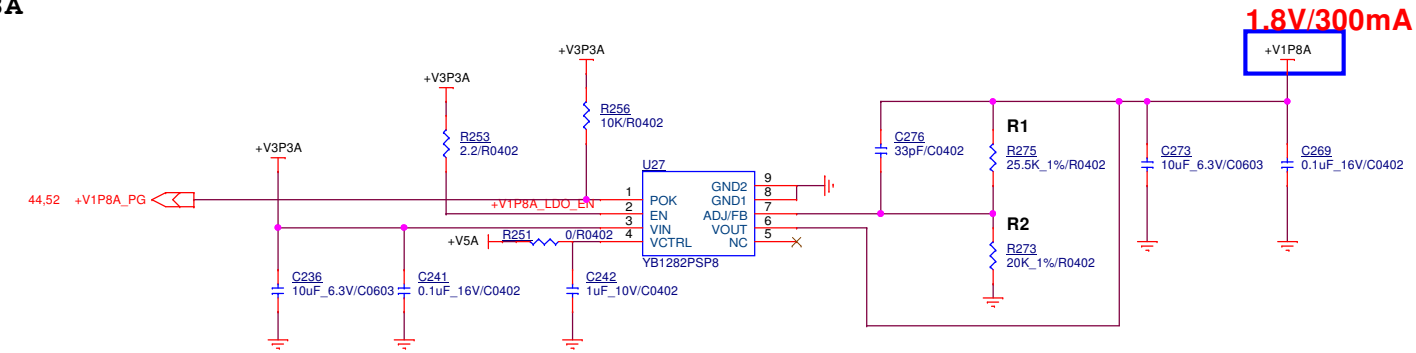
+VCCST_PLL (To CPU)



+V3P3A_LAN



+V1P8A



Vout= 0.8 x (1 + R1 / R2)

Vout	1V	1.05V	1.15V	1.2V	1.24V	1.35V	1.5V	1.8V	2.5V
R1	11K	16K	13.3K	15.4K	15K	13.7K	27K	25.5K	64.9K
R2	40.2K	51K	30.1K	30K	27K	19.6K	30K	20K	30K

AAEON An ASUS Company

Title: PPWER SWITCH +VCCST_PLL,+V3P3A_LAN,+V1P

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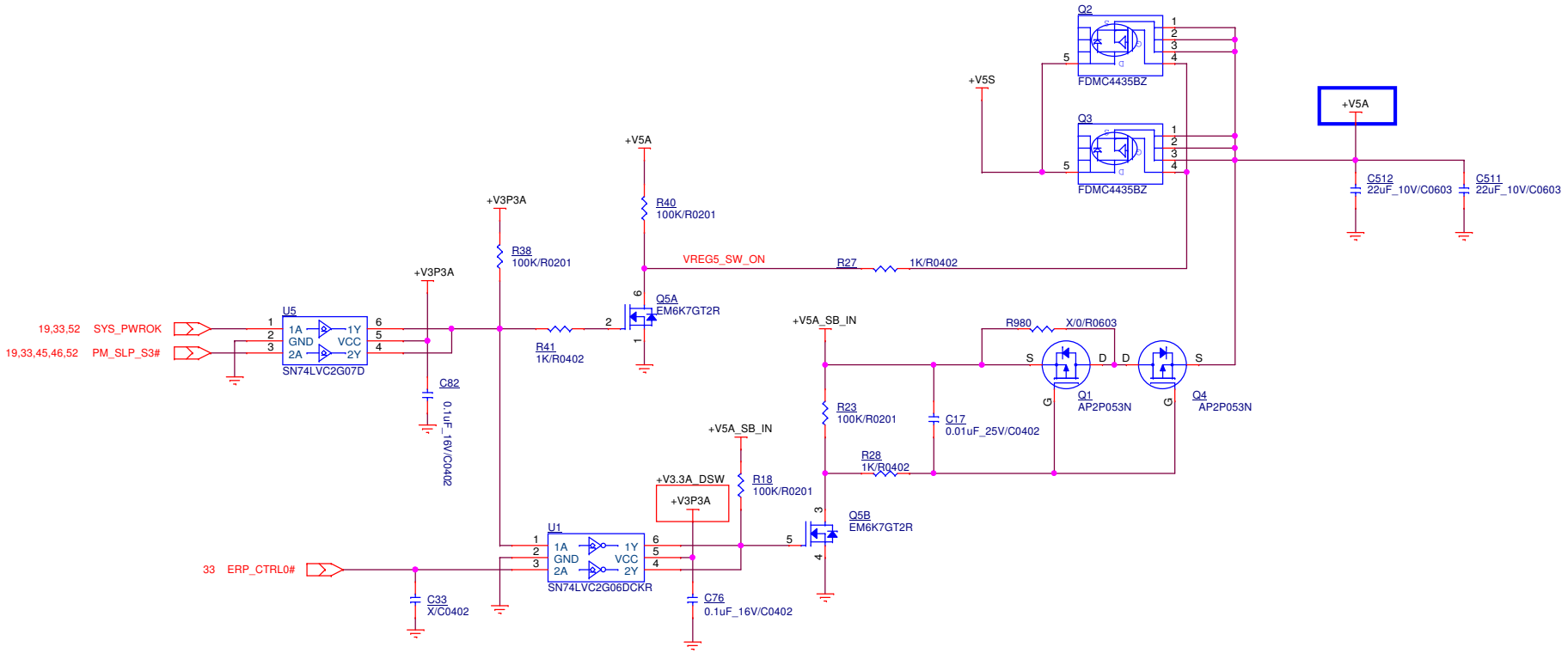

<Variant Name>

AAEON An ASUS Company

Title: Power Standby switch

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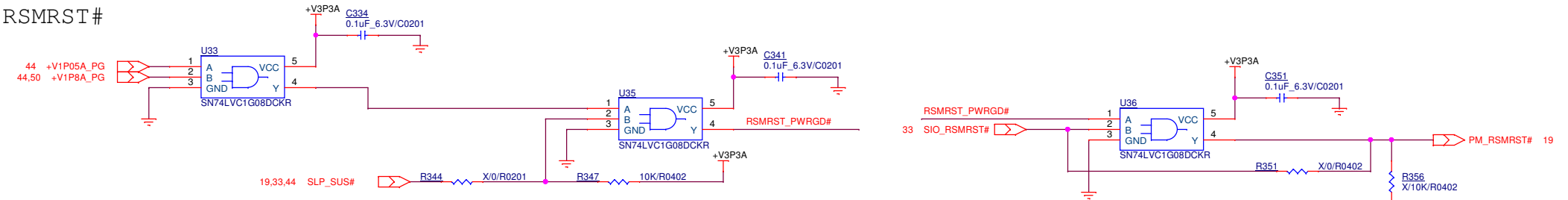
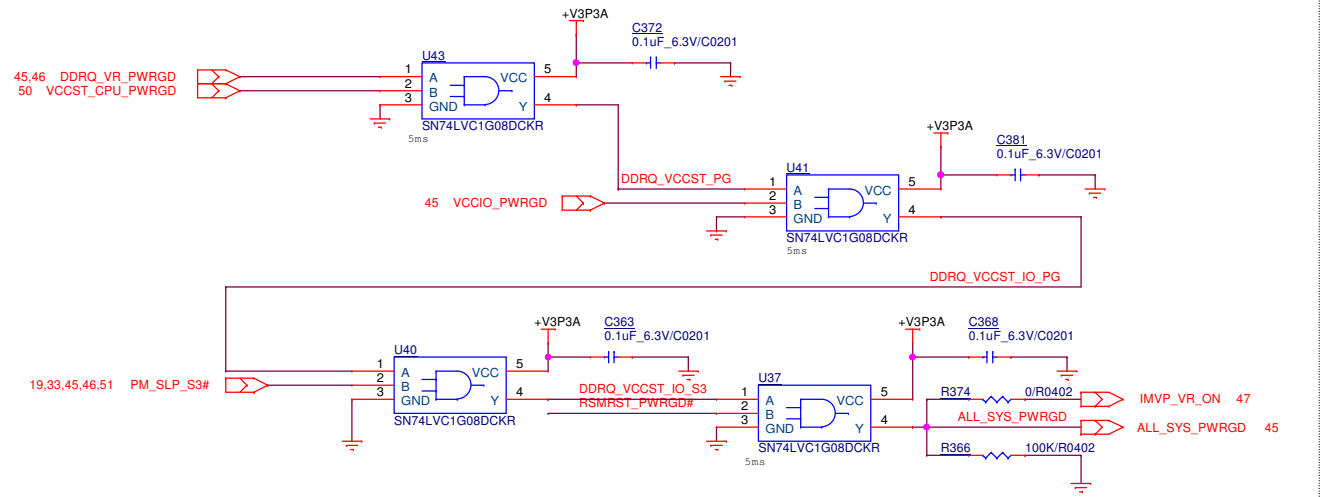
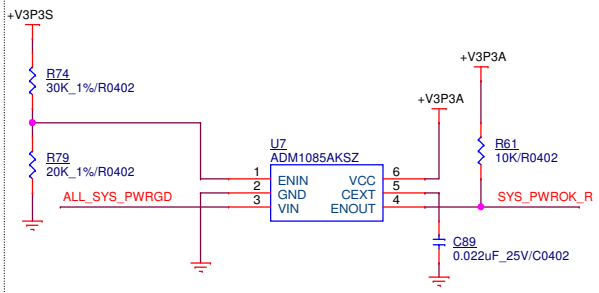
RSMRST#

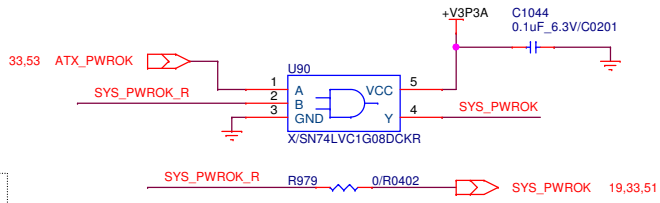


ALL_SYS_PWRGD

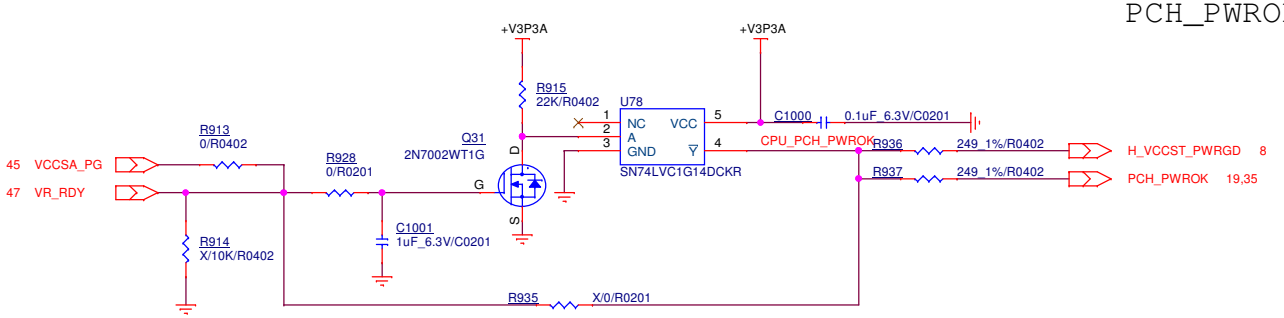


SYS_PWROK





PCH_PWROK



PCH_PWRGD & VCCST_PWRGD & SYS_PWROK

AAEON An ASUS Company

Title: **Boot Sequence**

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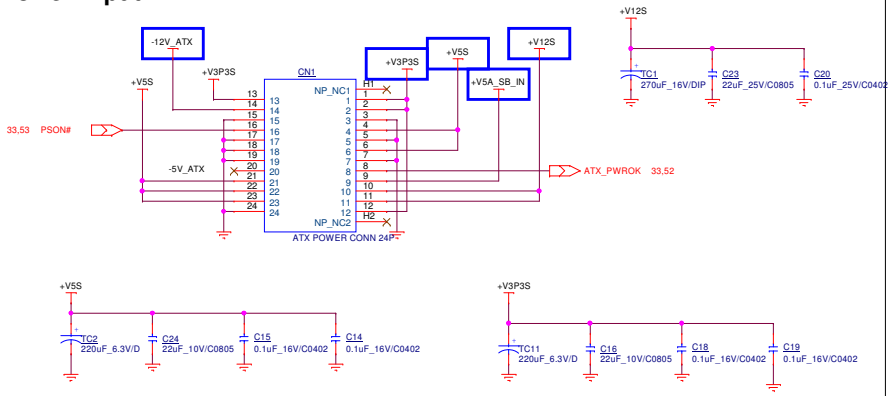
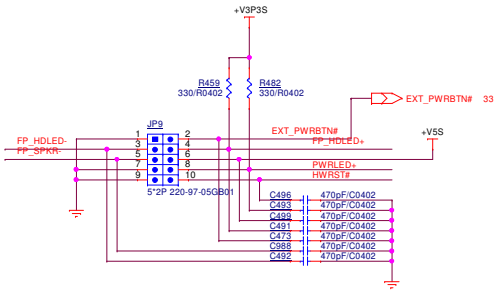
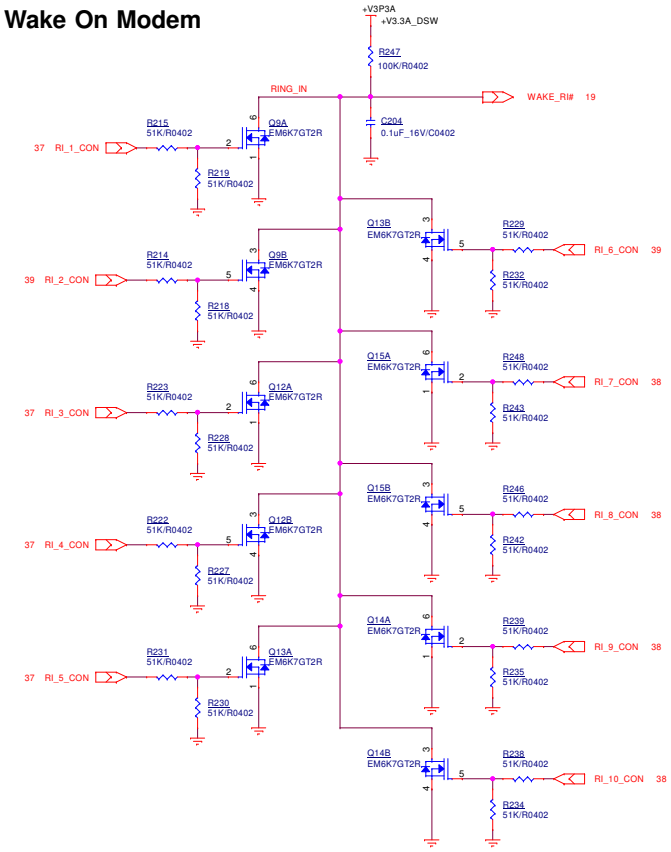
Power Input



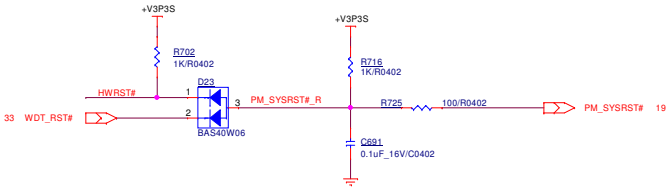
Front Panel



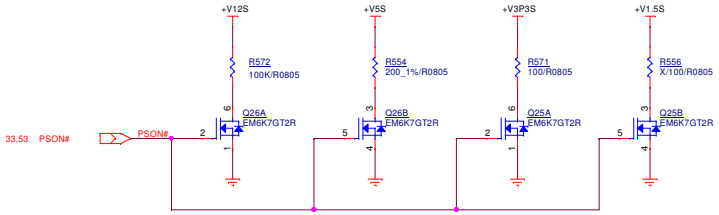
Wake On Modem



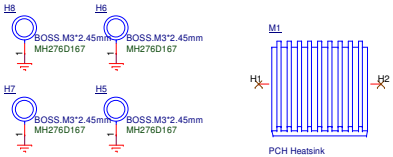
Reset Circuit



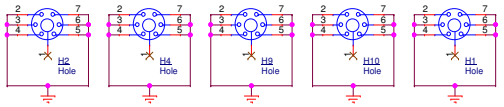
Discharge Circuit



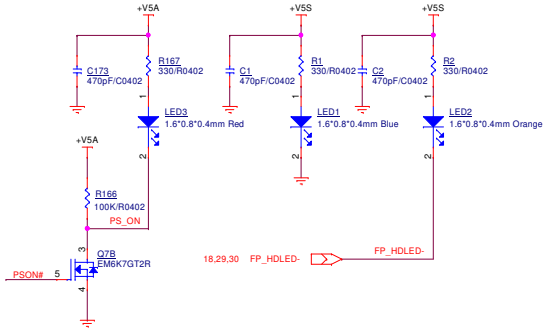
Heat Sink



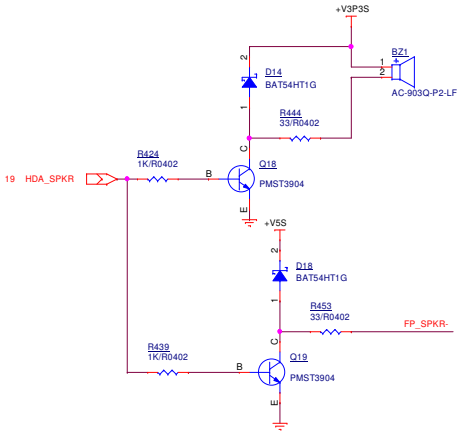
Mounting Holes



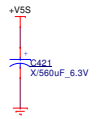
LED



Speaker



Decoupling for power



<Variant Name>

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HISTORY

Item	Date	Revision	Description	Page	Design By	Approve By
1	2019/01/10	A0.1	First Release		Lena	Edwin
2	2019/09/03	A0.2	1. Add 47uF(11EA647010) parallel to C55 for Transient adjust by power team 2.Change R171 from 287kohm to 232kohm(105A523239) for OCP adjust. by power team 3.Vcore power 4 phase by power team 4.BIOS SKT Remove 5.SIO pin73 +V5A_ERP change to +V5A_SB_IN 6. FAN +VCC_FAN_SYS and +VCC_FAN_CPU change to 12V 7. m.2 colay SATA PCIE 8. +VCCPRIM_1P05 resistor remove 9.PCI function remove PCIE Connector move to left side 10.memory support ECC 11.two Dimm Too close.the CPU and two dimm modify location by ME 12. m.2 B key colay 3042	1-53	Hans	Edwin

<Variant Name>

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