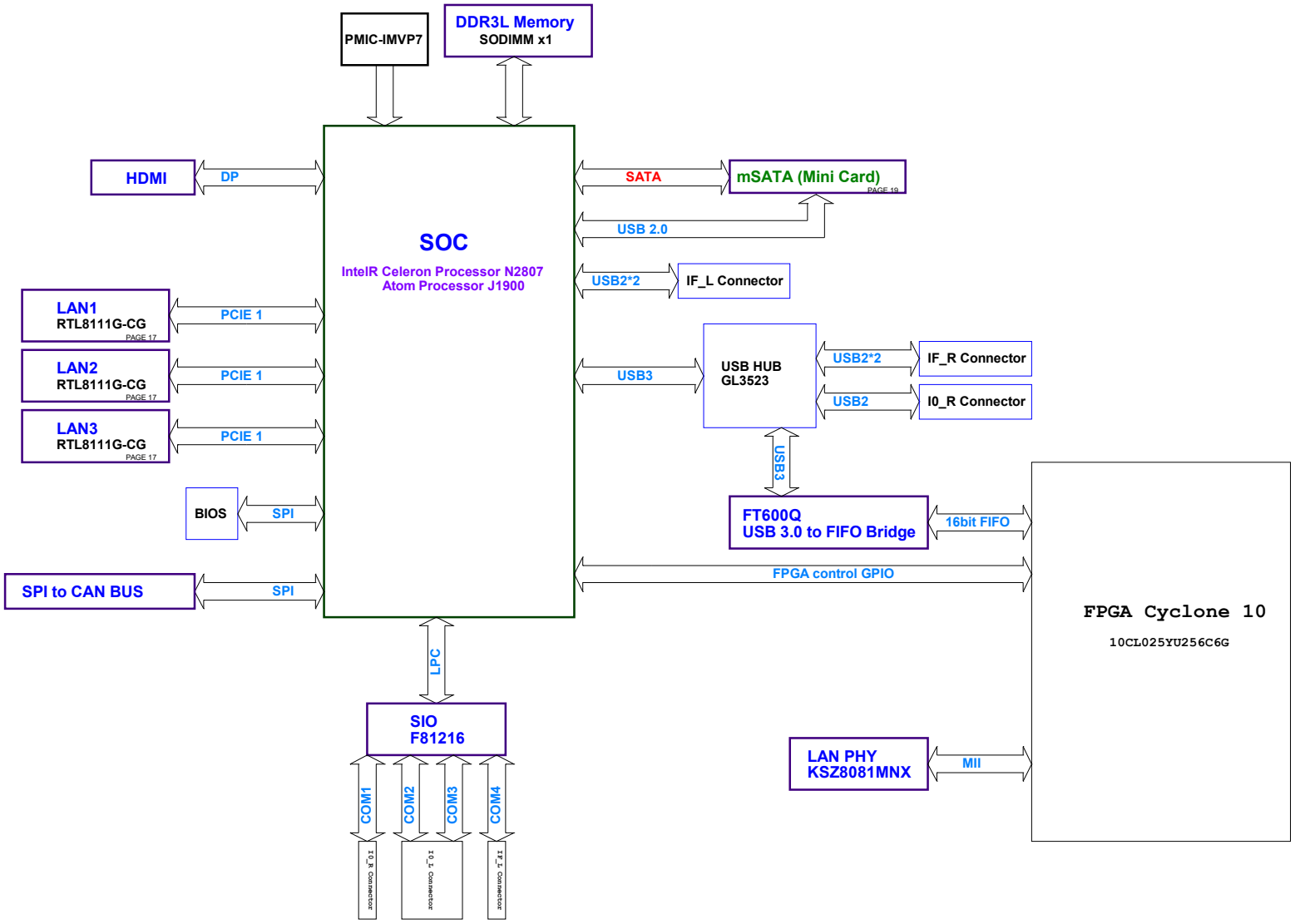
HF-MPLC01



HF-MPLC01

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Title: Cover Sheet

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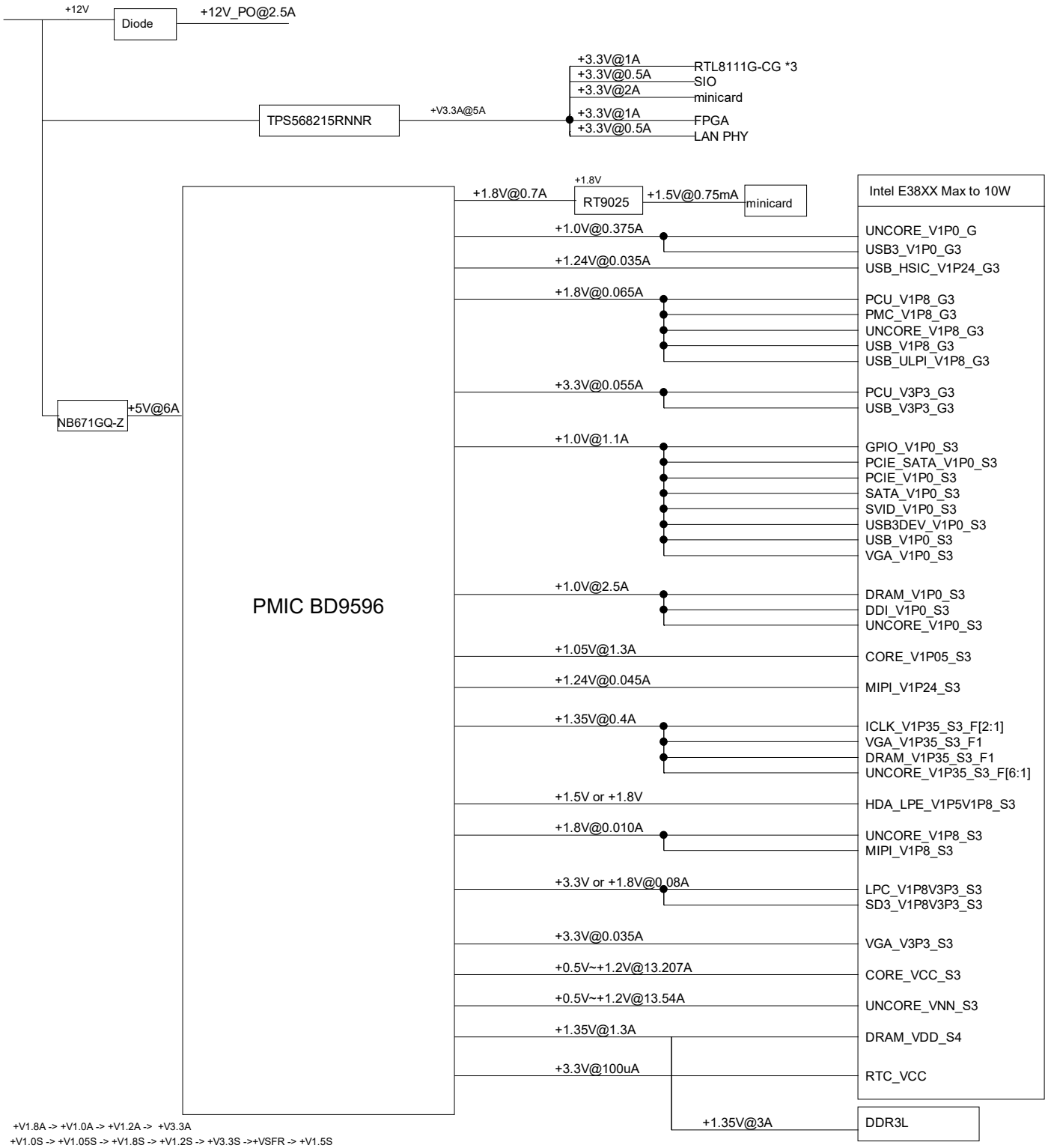
SOC GPIO Pins :

Name	Power Well	Default	GPIO Function
GPIO_S0_SC[00]	1.8V Core	GPI	
GPIO_S0_SC[01]	1.8V Core	GPI	
GPIO_S0_SC[07]	1.8V Core	GPI	
GPIO_S0_SC[55]	1.8V Core		
GPIO_S0_SC[56]	1.8V Core		
GPIO_S0_SC[57]	1.8V Core		DDR_ID0
GPIO_S0_SC[58]	1.8V Core		DDR_ID1
GPIO_S0_SC[59]	1.8V Core		BOARD_ID0
GPIO_S0_SC[60]	1.8V Core		BOARD_ID1
GPIO_S0_SC[61]	1.8V Core		BOARD_ID2
GPIO_S0_SC[92]	1.8V Core		DDR_ID2
GPIO_S0_SC[93]	1.8V Core		
GPIO_S0_SC[94]	1.8V Core		
GPIO_S0_SC[95]	1.8V Core		
GPIO_S5[00]	1.8V Suspend		
GPIO_S5[01]	1.8V Suspend		PME#
GPIO_S5[02]	1.8V Suspend		
GPIO_S5[03]	1.8V Suspend		EN_FPGA_PM
GPIO_S5[04]	1.8V Suspend		LAN1_DISABLE#
GPIO_S5[05]	1.8V Suspend		
GPIO_S5[06]	1.8V Suspend		
GPIO_S5[07]	1.8V Suspend		
GPIO_S5[08]	1.8V Suspend		RUN_STOP
GPIO_S5[09]	1.8V Suspend		FN-KEY
GPIO_S5[10]	1.8V Suspend		24V_DEC_INT
GPIO_S5[17]	1.8V Suspend		5V_DEC_INT
GPIO_S5[22]	1.8V Suspend		USB1_PORT1_EN
GPIO_S5[23]	1.8V Suspend		FPGA_GPIO0
GPIO_S5[24]	1.8V Suspend		FPGA_GPIO1
GPIO_S5[25]	1.8V Suspend		FPGA_GPIO2
GPIO_S5[26]	1.8V Suspend		FPGA_GPIO3
GPIO_S5[27]	1.8V Suspend		FPGA_GPIO4
GPIO_S5[28]	1.8V Suspend		SPI_CAN_INT#
GPIO_S5[29]	1.8V Suspend		SPI_CAN_INT0#
GPIO_S5[30]	1.8V Suspend		SPI_CAN_INT1#



Platform Rail	Voltage Tolerances	Max Icc Premium
V1P0A - UNCORE_V1P0_G3 - USB3_V1P0_G3	1.0 V DC: ±2% AC: ±3%	375 mA
V1P24A - USB_HSIC_V1P24_G3 (Can connect to V1P0A when USB HSIC isn't used)	1.24 V DC: ±3% AC: ±2%	35 mA
V1P8A - PCU_V1P8_G3 - PMC_V1P8_G3 - UNCORE_V1P8_G3 - USB_V1P8_G3 - USB_ULPI_V1P8_G3	1.8 V DC: ±3% AC: ±2%	65 mA
V3P3A - PCU_V3P3_G3 - USB_V3P3_G3	3.3 V DC: ±2% AC: ±3%	55 mA
V1P0S - GPIO_V1P0_S3 - PCIE_SATA_V1P0_S3 - PCIE_V1P0_S3 - SATA_V1P0_S3 - SVID_V1P0_S3 - USB3DEV_V1P0_S3 - USB_V1P0_S3 - VGA_V1P0_S3	1.0 V DC: ±2% AC: ±3%	1.1 A

Platform Rail	Voltage Tolerances	Max Icc Premium
V1P0S - DRAM_V1P0_S3 - DDI_V1P0_S3 - UNCORE_V1P0_S3	1.0 V DC: ±2% AC: ±3%	2.5 A
V1P05S - CORE_V1P05_S3	1.05 V DC: ±2% AC: ±3%	1.3 A
V1P24S - MIPI_V1P24_S3 (can be grounded if MIPI CSI not used)	1.24 V DC: ±2% AC: ±3%	45 mA
V1P35S (VSFR) - ICLK_V1P35_S3_F[2:1] - VGA_V1P35_S3_F1 - DRAM_V1P35_S3_F1 - UNCORE_V1P35_S3_F[6:1]	1.35 V DC: ±3% AC: ±2%	400 mA
V1P5V1P8S (VAUD) - HDA_LPE_V1P5V1P8_S3	1.5 V (LV HDA) 1.8 V (LPE)	In V1P8S
V1P8S - UNCORE_V1P8_S3 - MIPI_V1P8_S3	1.8 V DC: ±3% AC: ±2%	10 mA
V1P8V3P3S (VSDIO,VLPC) - LPC_V1P8V3P3_S3 - SD3_V1P8V3P3_S3	1.8 V 3.3 V (V3P3A) DC: ±2% AC: ±3%	8 mA
V3P3S - VGA_V3P3_S3	3.3 V DC: ±2% AC: ±3%	35 mA
VCC - CORE_VCC_S3	See Table 78	11 A
VNN - UNCORE_VNN_S3	See Table 78	14 A
VDD - DRAM_VDD_S4	1.35 V DC: ±2% AC: ±3%	1.3 A
VRTC - RTC_VCC	G3: 2-3 V at battery* Otherwise: V3P3A (pre diode drop)	100 uA (6 uA Avg.) (see note)

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Title: POWER TREE

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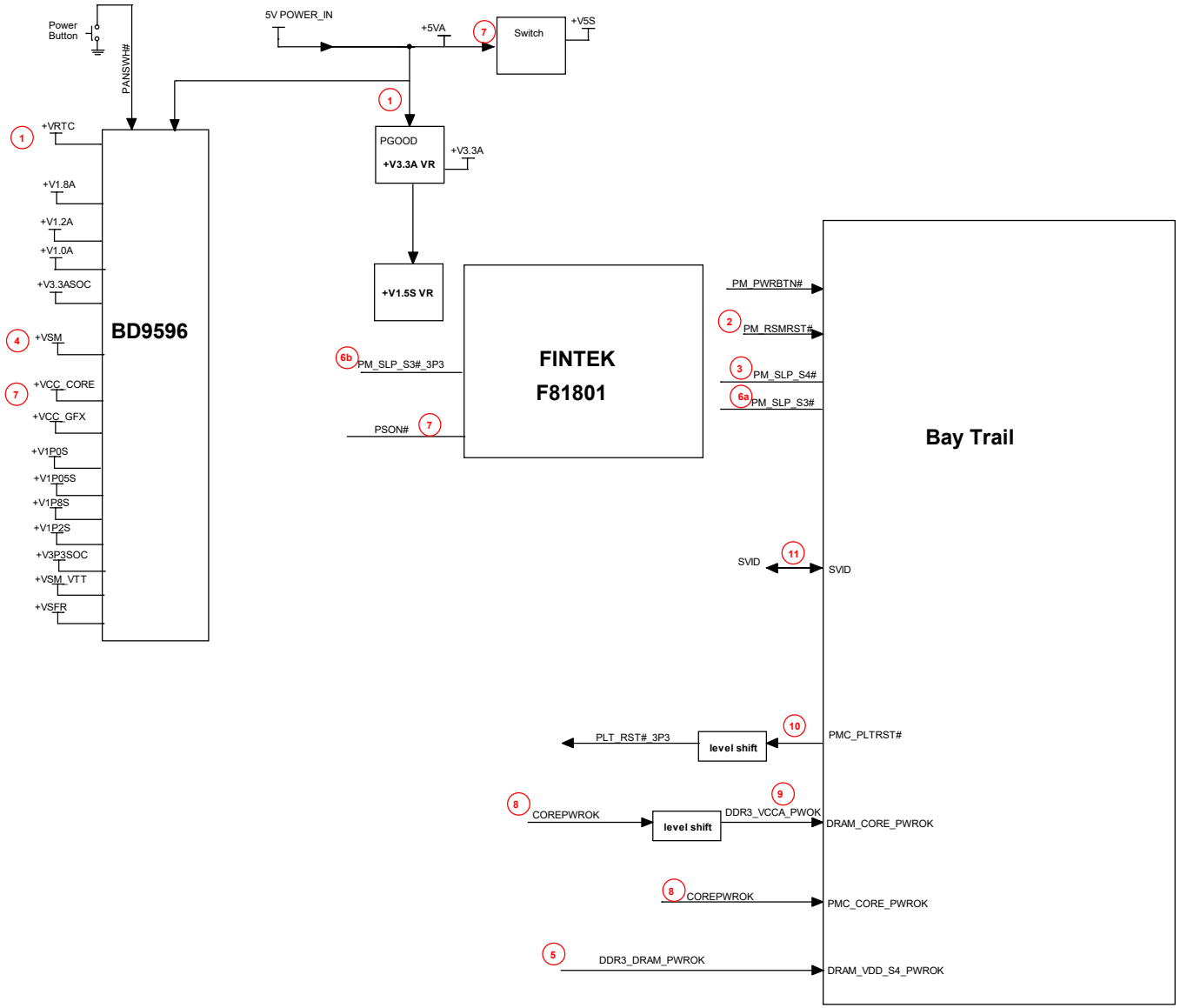

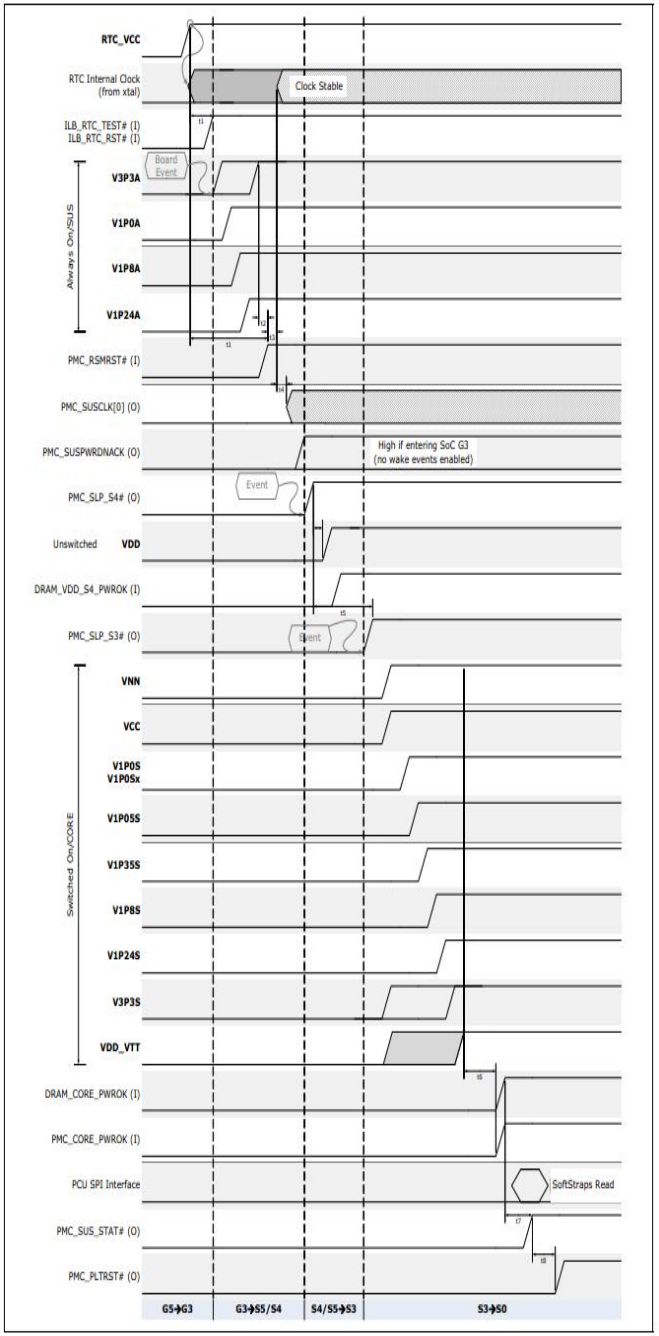

AAEON an ASUS assoc. co.	Title: Power Sequence		
	Size: Custom	Document Number	Rev: A0.2
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AAEON an ASUS assoc. co.	Title: SoC DDR Memory		
	Size: C	Document Number	Rev: A0.2
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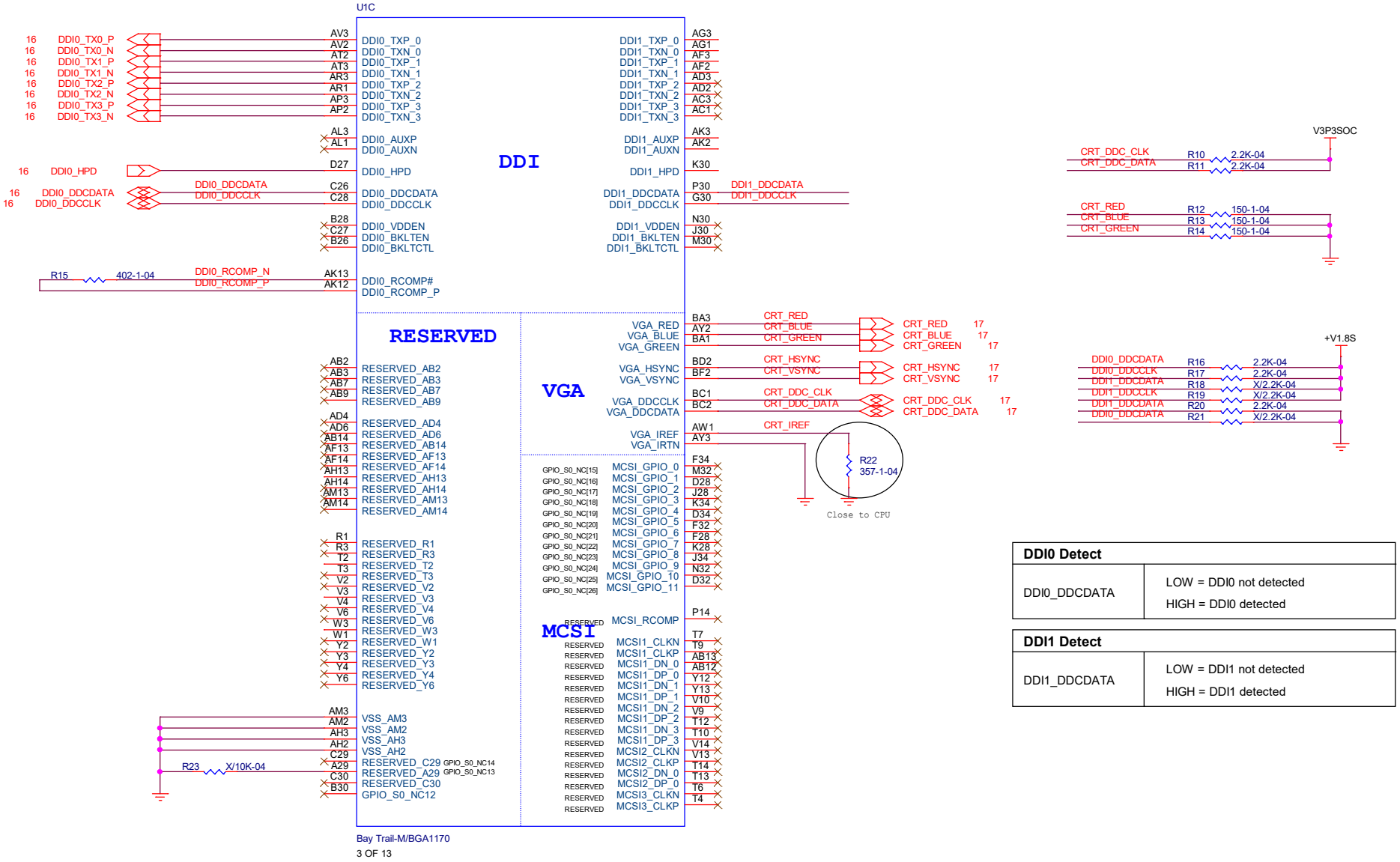

DDI0 Detect	
DDI0_DDCDATA	LOW = DDI0 not detected HIGH = DDI0 detected

DDI1 Detect	
DDI1_DDCDATA	LOW = DDI1 not detected HIGH = DDI1 detected

AAEON an ASUS assoc. co.	Title: SoC Display		
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U1D

SATA
PCIE
eMMC
AUDIO
SDIO
RESERVED
SD

Bay Trail-M/BGA1170

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To mini PCIe

PCIe X1
LAN1
LAN2
LAN3

When LPE is active, the High Definition Audio functionality is disabled.

Boot BIOS Strap	
LPE_I2S2_FRM/GPIO_S0_SC[63]	Boot BIOS
0	LPC
1 (default)	SPI

Flash Descriptor Security Overide	
HDA_SDOUT	LOW = Overide **HIGH = Normal Operation**

AAEON an ASUS assoc. co.	Title: SoC SATA,PCIE,HDA,eMMC,SD		
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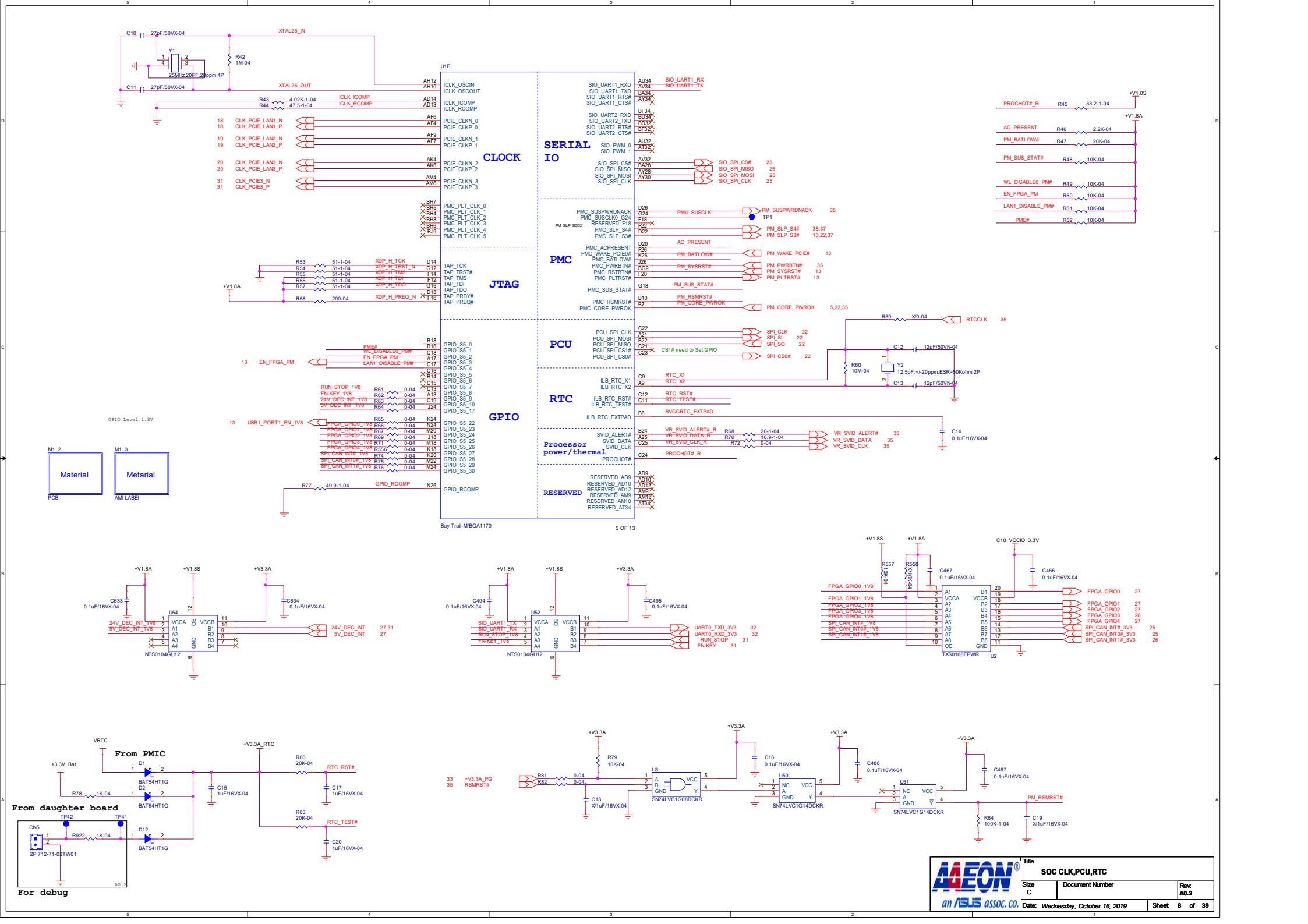
U1E
CLOCK
SERIAL IO
JTAG
PMC
PCU
RTC
GPIO
Processor power/thermal
RESERVED
Bay Trail-M/BGA1170
5 OF 13
XTAL25_IN
XTAL25_OUT
25MHz 20PF 20ppm 4P
ICLK_ICOMP
ICLK_RCOMP
GPIO_RCOMP
PM_SUSPWRDNACK
PM_SUSCLK
PM_SLP_S4#
PM_SLP_S3#
AC_PRESENT
PM_BATLOW#
PM_WAKE_PCIE#
PM_SYSRST#
PM_PWRBTN#
PM_PLTRST#
PM_SUS_STAT#
PM_RSMRST#
PM_CORE_PWROK
RTCCLK
SPI_CLK
SPI_SI
SPI_SO
SPI_CS0#
RTC_X1
RTC_X2
RTC_RST#
RTC_TEST#
BVCCRTC_EXTPAD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
PROCHOT#
SIO_UART1_RX
SIO_UART1_TX
SIO_SPI_CS#
SIO_SPI_MISO
SIO_SPI_MOSI
SIO_SPI_CLK
PROCHOT#_R
AC_PRESENT
PM_BATLOW#
PM_SUS_STAT#
WL_DISABLE0_PM#
EN_FPGA_PM
LAN1_DISABLE_PM#
PME#
GPIO Level 1.8V
Material
PCB
Metarial
AMI LABEl
From PMIC
From daughter board
For debug
SOC CLK,PCU,RTC
Size C
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Rev. A0.2
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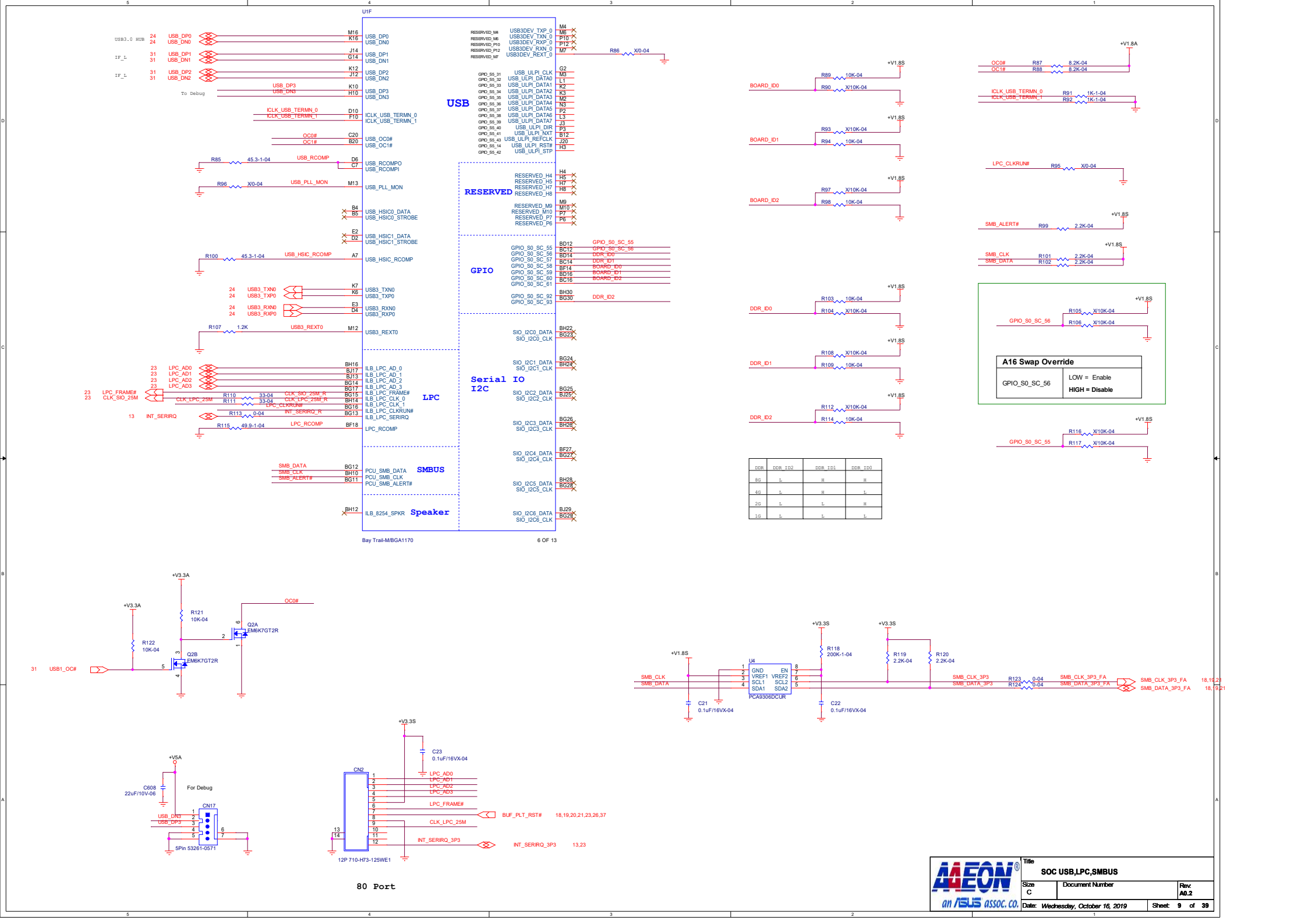
U1F
USB
RESERVED
GPIO
Serial IO I2C
LPC
SMBUS
Speaker
Bay Trail-M/BGA1170
6 OF 13
A16 Swap Override
GPIO_S0_SC_56
LOW = Enable
HIGH = Disable
80 Port
SOC USB,LPC,SMBUS
Size C
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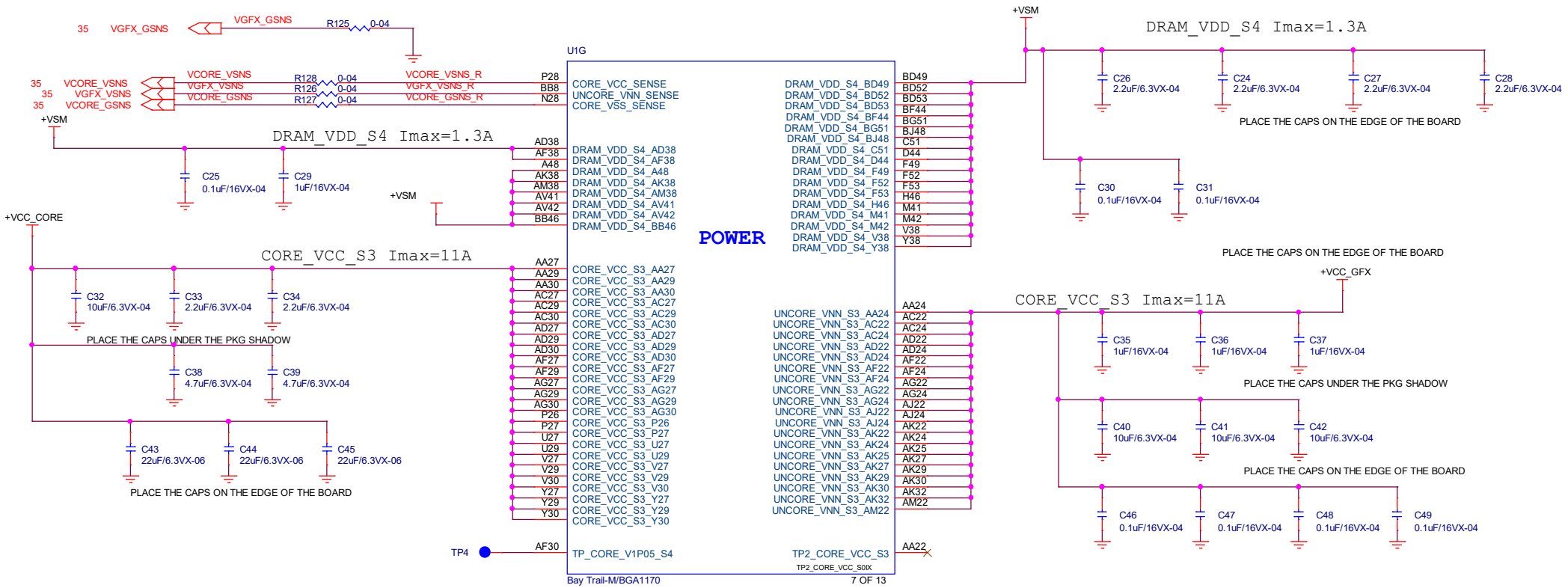

AAEON an ASUS assoc. co.	Title: SOC POWER I	
Size: B	Document Number: HF-MPLC01	Rev: A0.2
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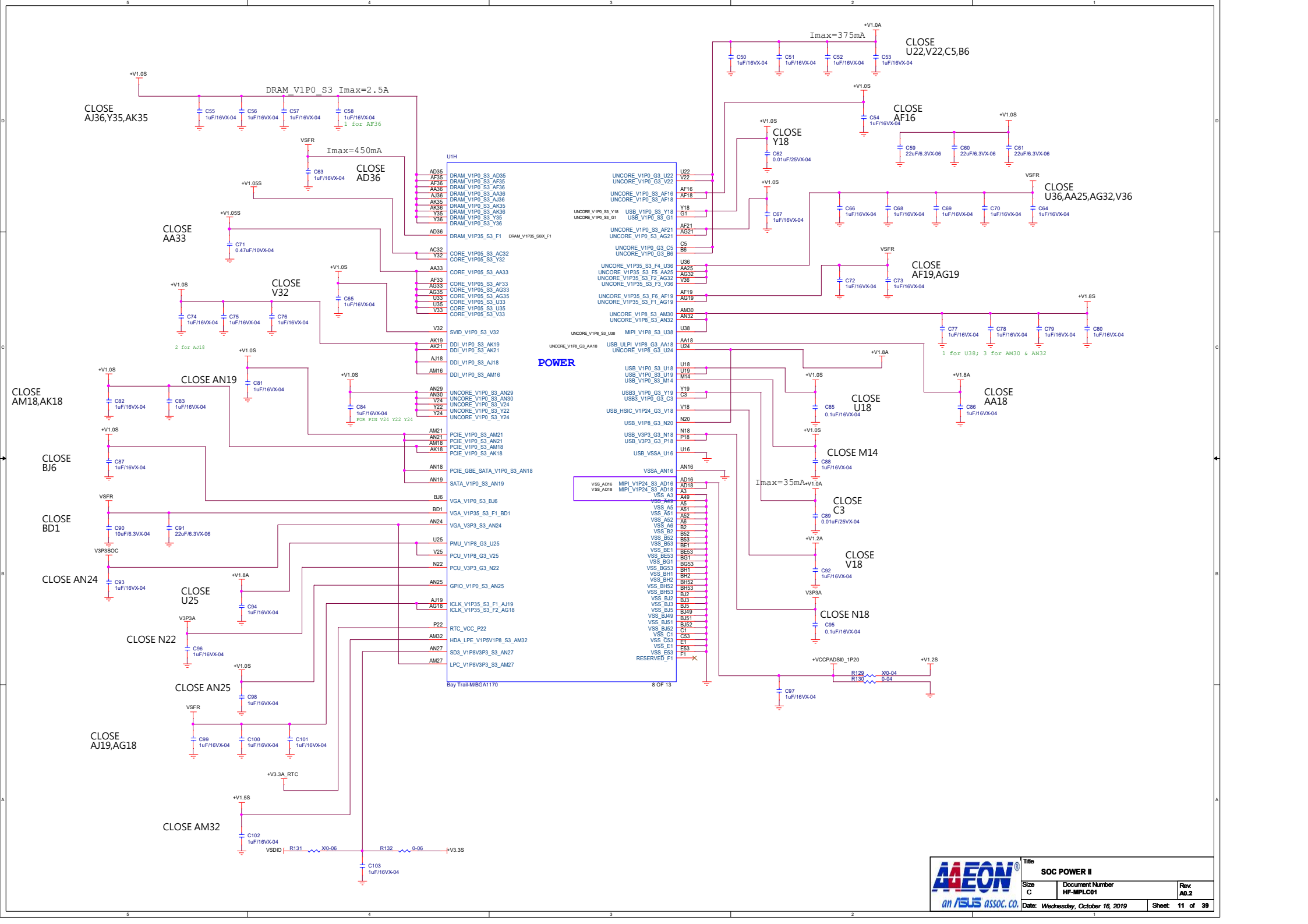
DRAM_V1P0_S3 Imax=2.5A
CLOSE AJ36,Y35,AK35
Imax=450mA
CLOSE AD36
CLOSE AA33
CLOSE V32
CLOSE AN19
CLOSE AM18,AK18
CLOSE BJ6
CLOSE BD1
CLOSE AN24
CLOSE U25
CLOSE N22
CLOSE AN25
CLOSE AJ19,AG18
CLOSE AM32
U1H
POWER
Bay Trail-M/BGA1170
8 OF 13
Imax=375mA
CLOSE U22,V22,C5,B6
CLOSE AF16
CLOSE Y18
CLOSE U36,AA25,AG32,V36
CLOSE AF19,AG19
CLOSE AA18
CLOSE U18
CLOSE M14
Imax=35mA
CLOSE C3
CLOSE V18
CLOSE N18
1 for AF36
2 for AJ18
FOR PIN V24 Y22 Y24
1 for U38; 3 for AM30 & AN32
R129 X/0-04
R130 0-04
R131 X/0-06
R132 0-06
AAEON
an ASUS assoc. co.
SOC POWER II
Size C
Document Number HF-MPLC01
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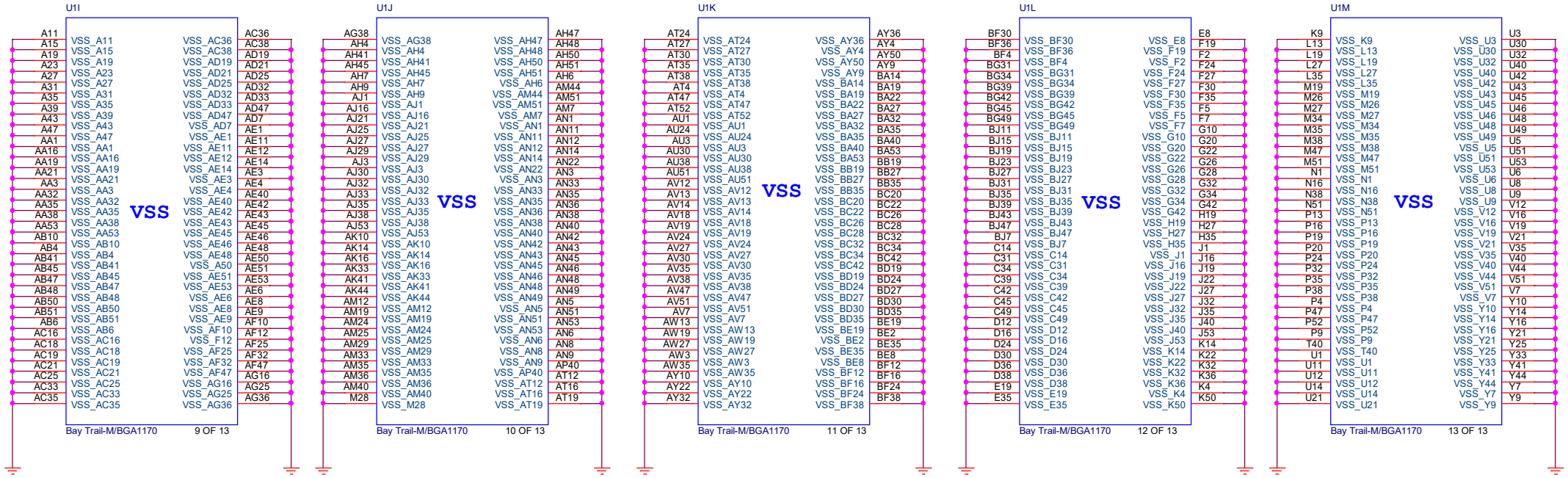

AEON an ASUS assoc. co.	Title: SOC POWER II		
	Size: B	Document Number: HF-MPLC01	Rev: A0.2
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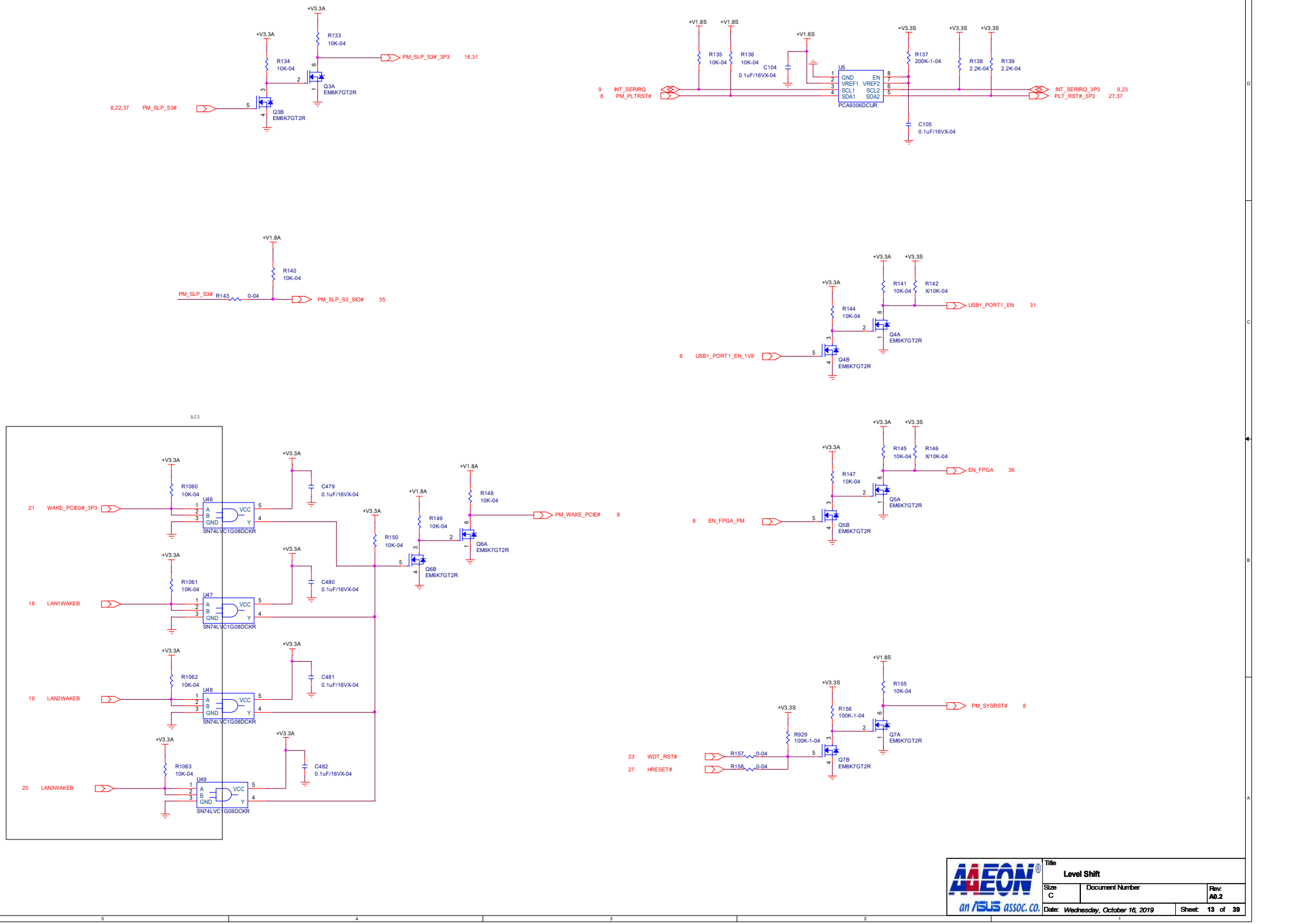

AAEON an ASUS assoc. co.	Title: Level Shift	
	Size: C	Document Number:
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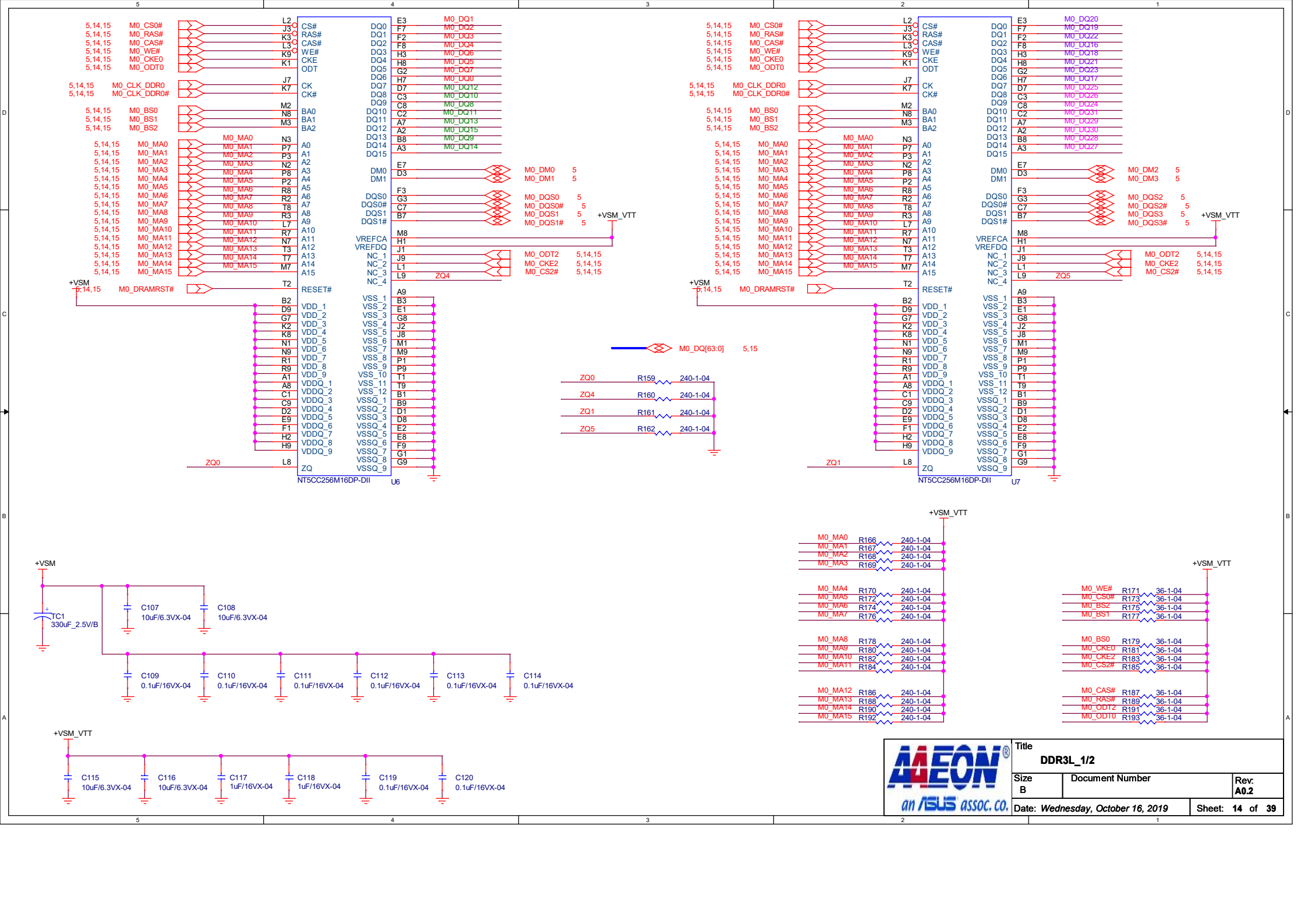

Title	DDR3L_1/2	
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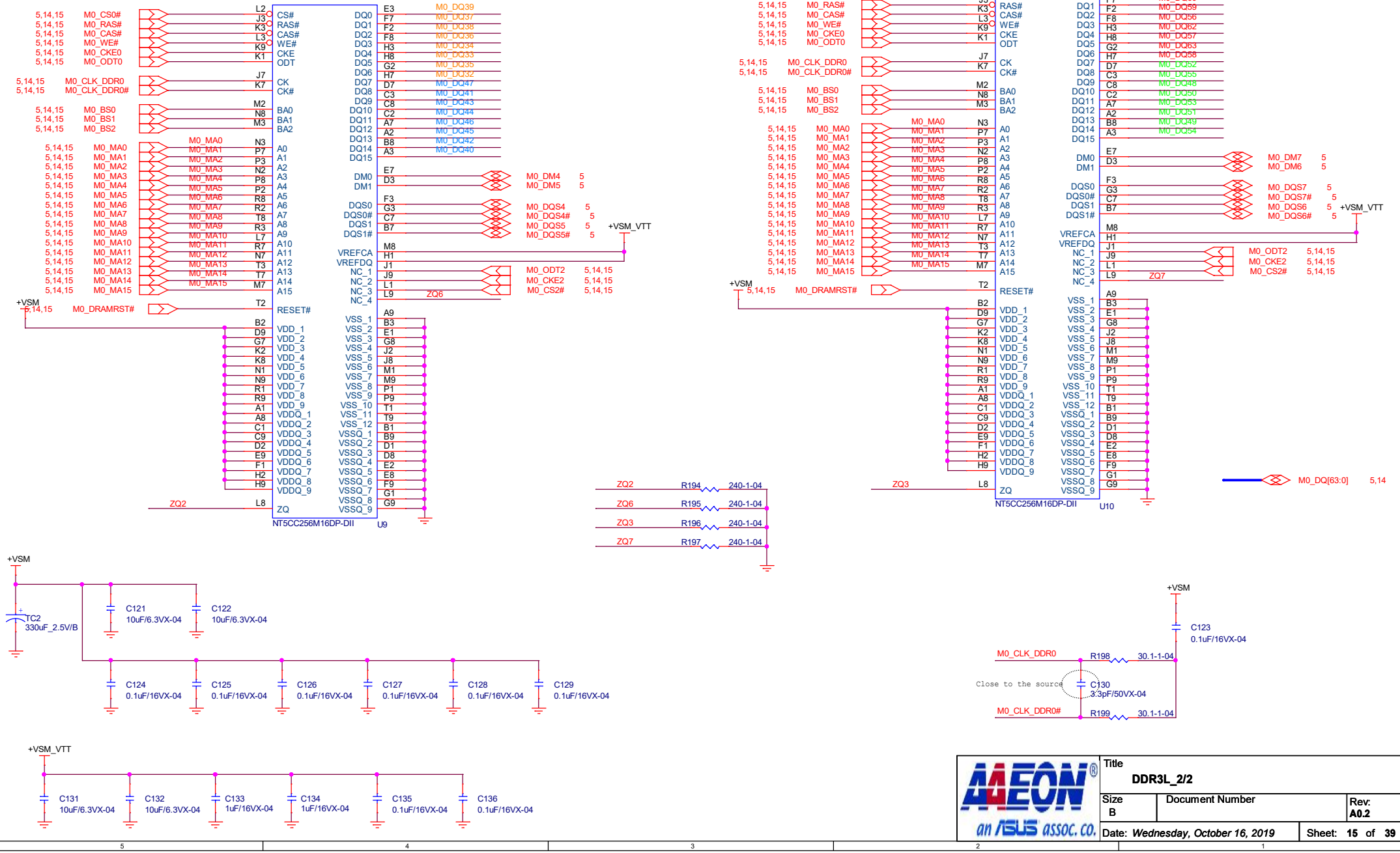

Title: DDR3L_2/2			
Size: B	Document Number		Rev: A0.2
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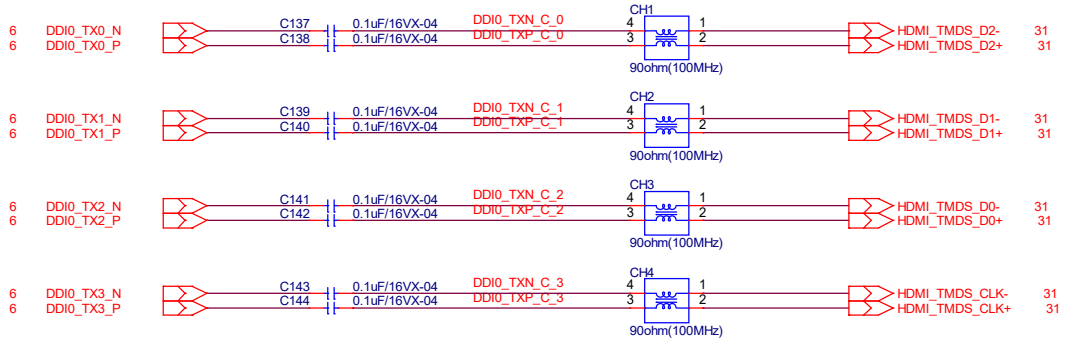
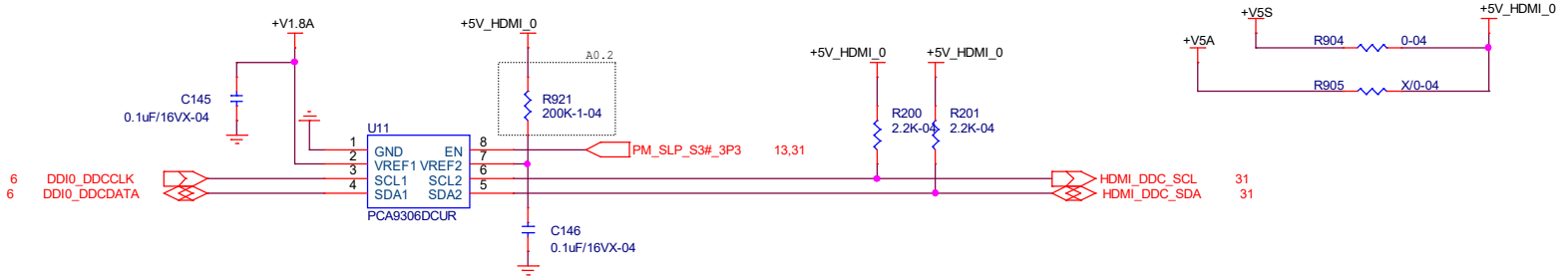
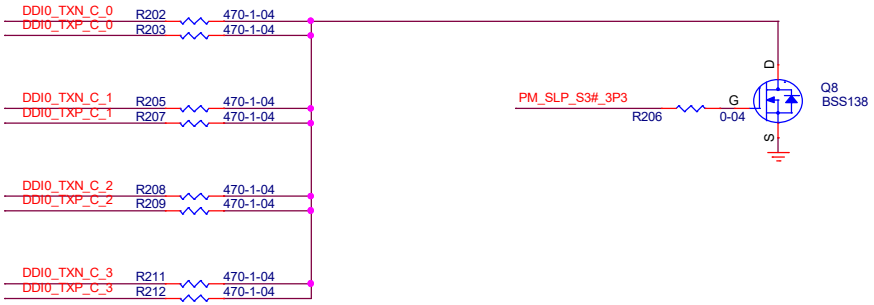
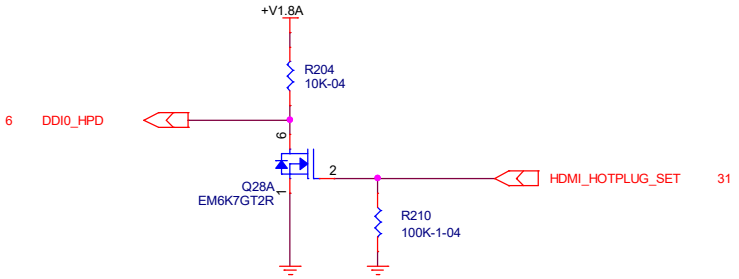
HDMI LEVEL SHIFT









AAEON an ASUS assoc. co.	Title: HDMI	
Size: B	Document Number: HF-MPLC01	Rev: A0.2
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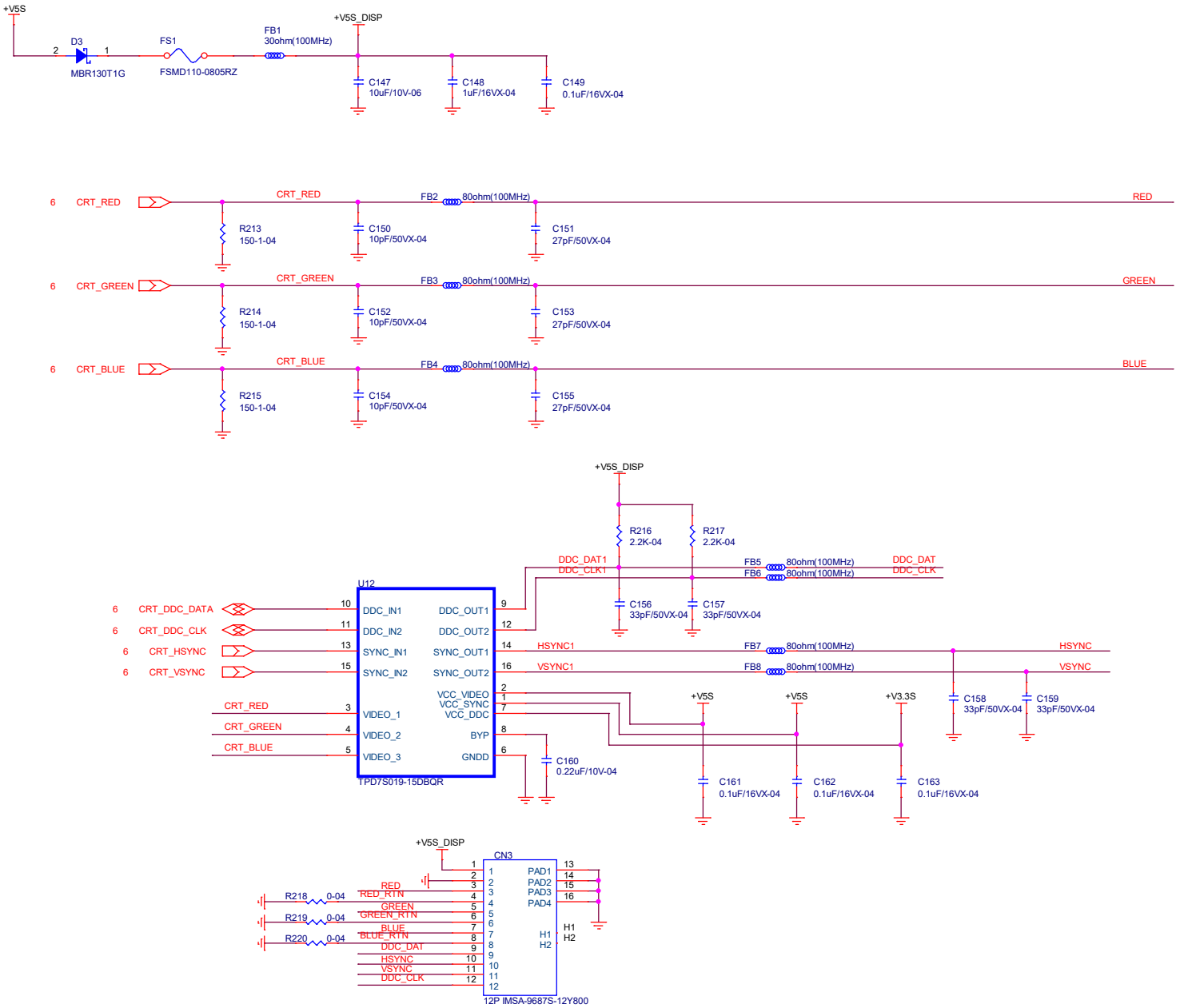

AAEON an ASUS assoc. co.	Title: VGA		
	Size: Custom	Document Number: HF-MPLC01	Rev: A0.2
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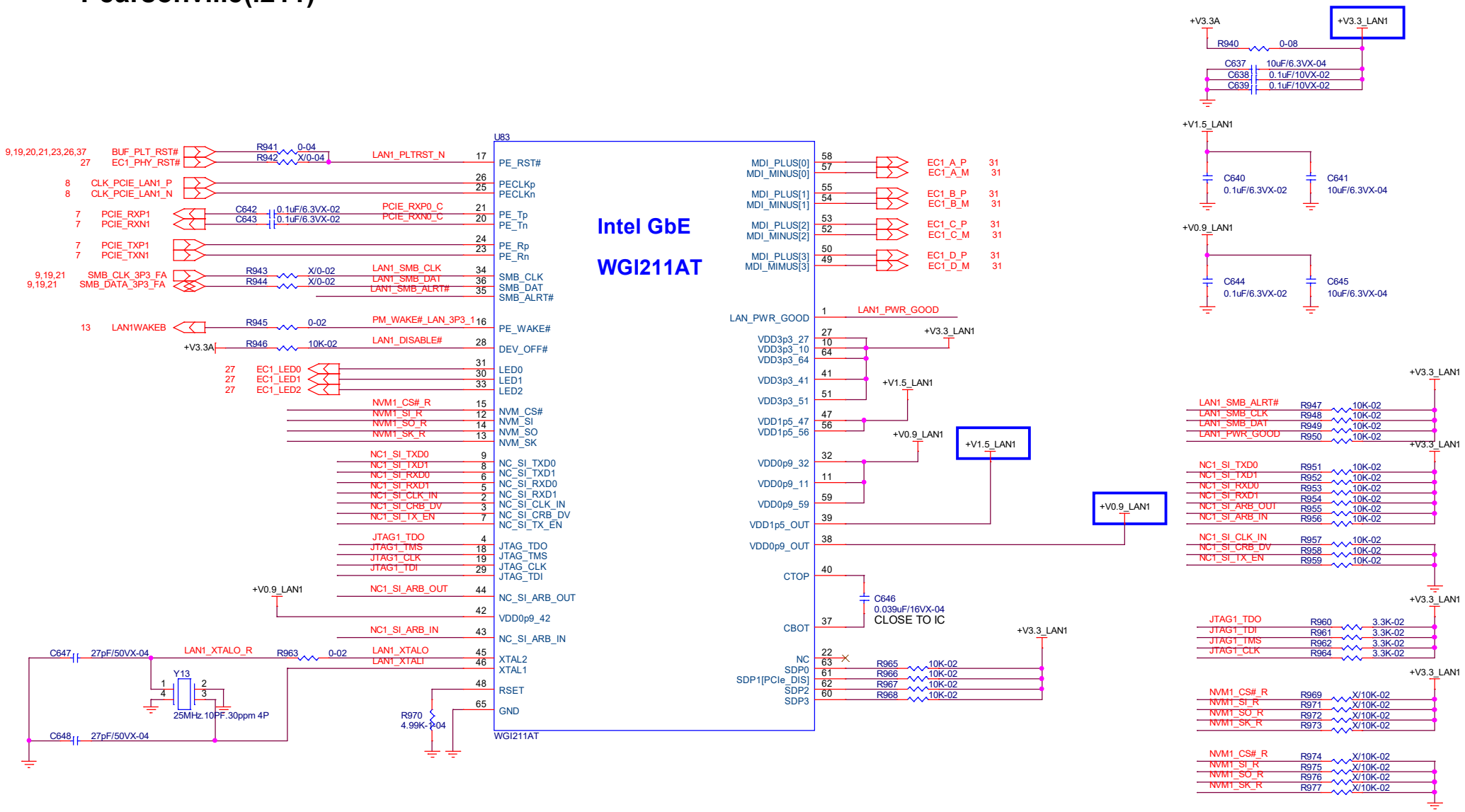
Pearsonville(i211)



AAEON an ASUS assoc. co.	Title: I211 ETHERNET1	
Size: B	Document Number: NET-PLUS	Rev: A0.3
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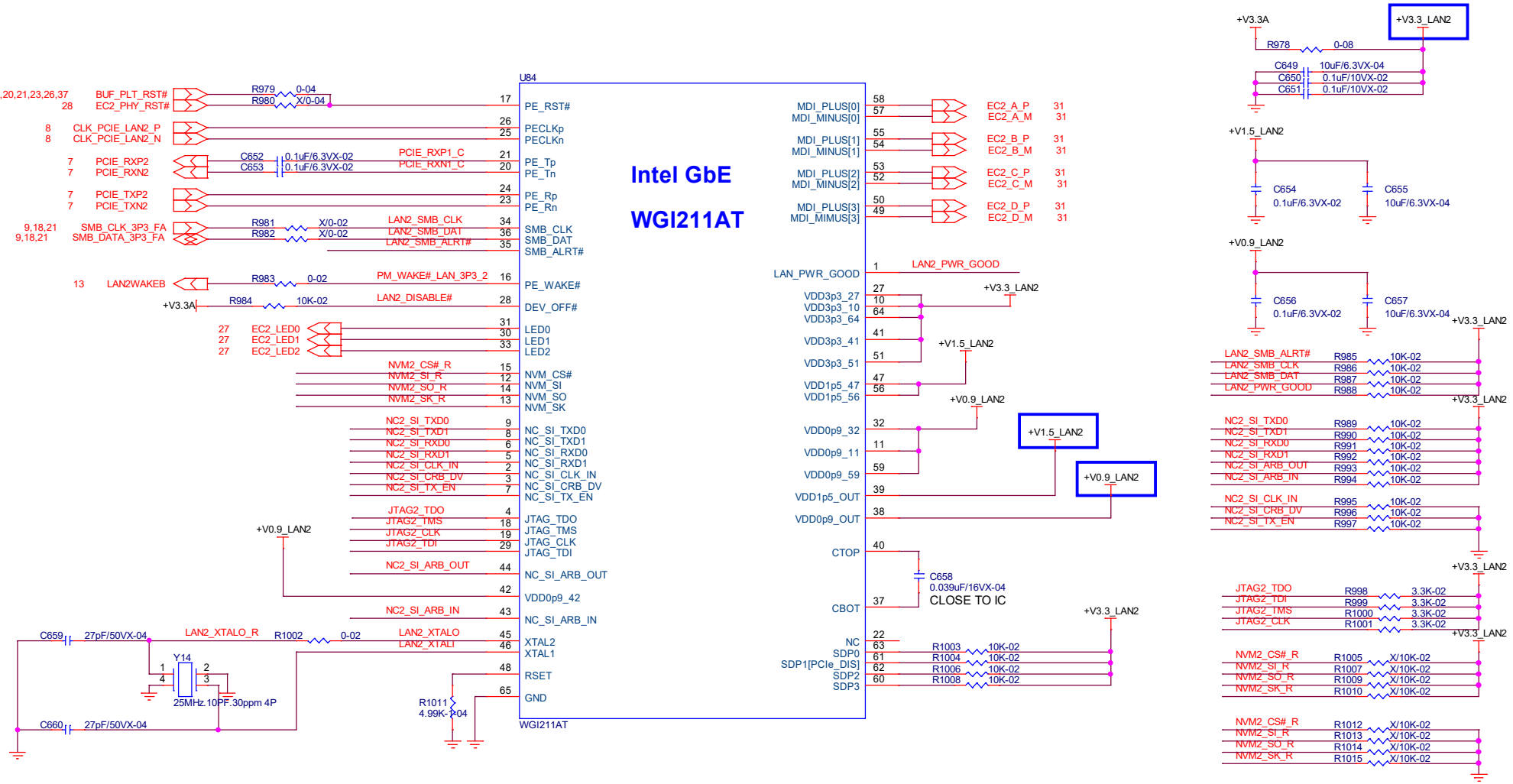
Pearsonville(i211)



Title: I211 ETHERNET2		
Size: B	Document Number: NET-PLUS	Rev: A0.3
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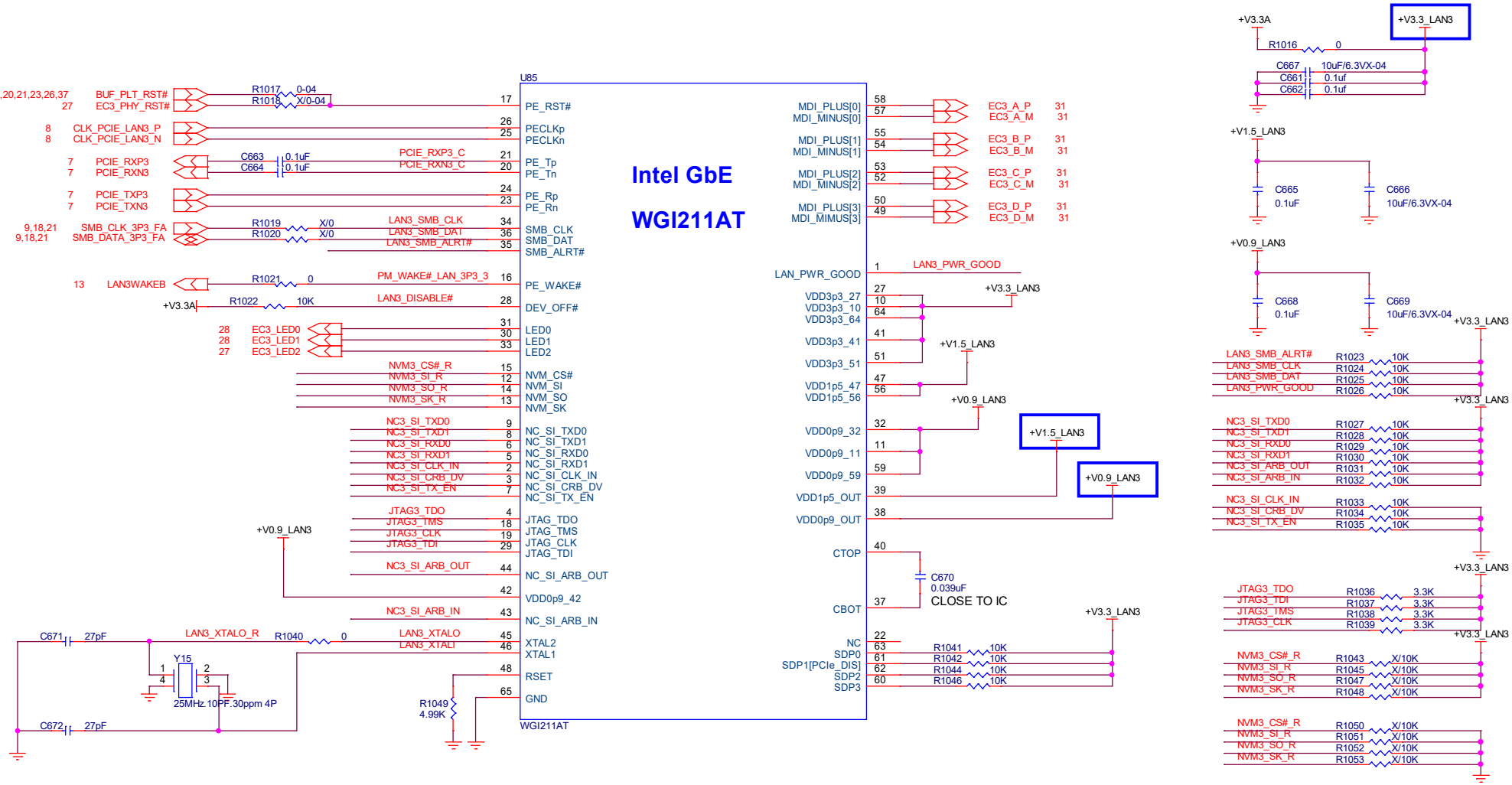
Pearsonville(i211)



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Size: B	Document Number: HF_MBPLC	Rev: A0.3
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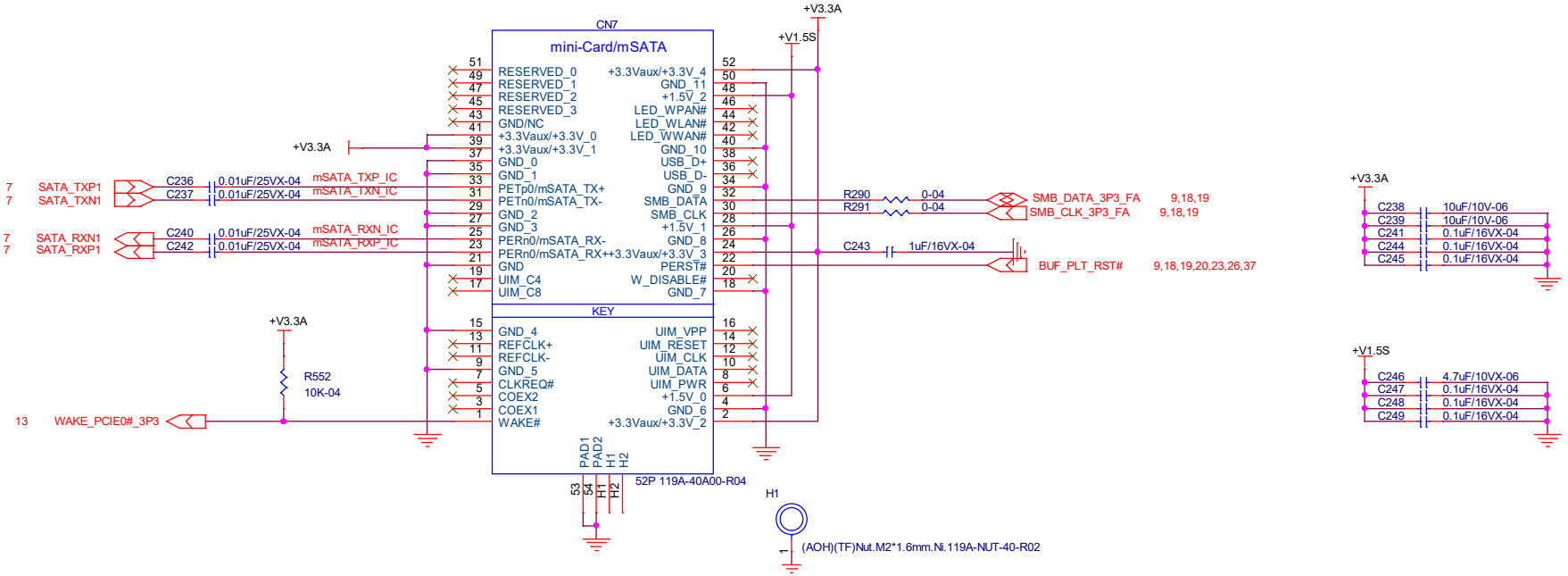

AAEON an ASUS assoc. co.	Title: **Mini-card**	
Size: B	Document Number	Rev: **A0.2**
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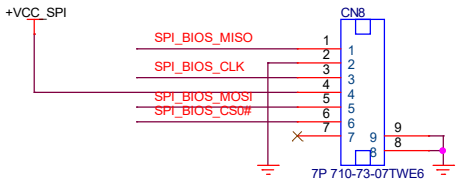
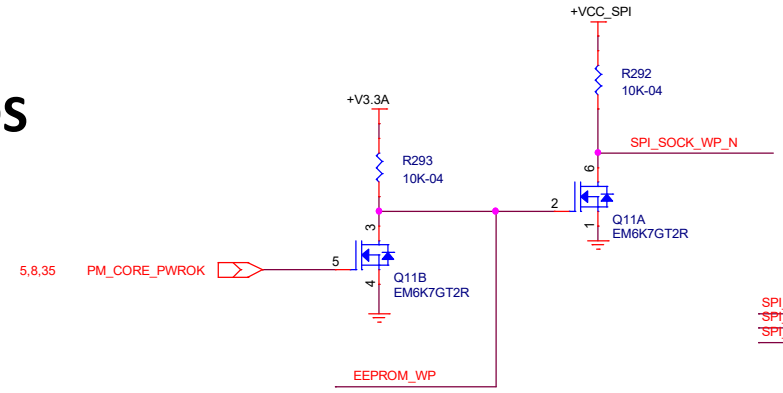
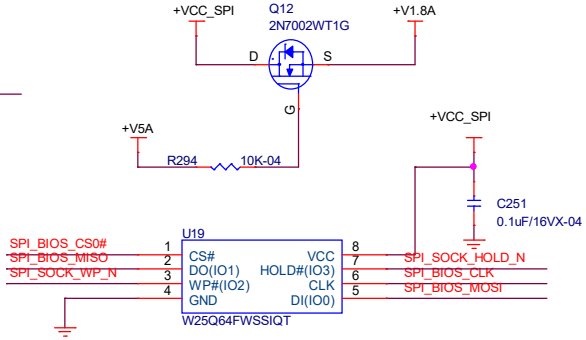
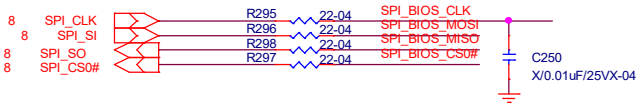
SPIBIOS

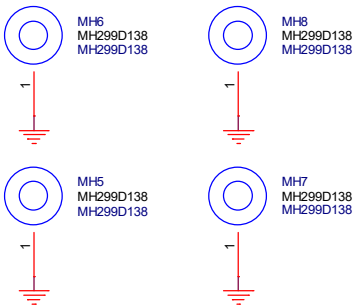




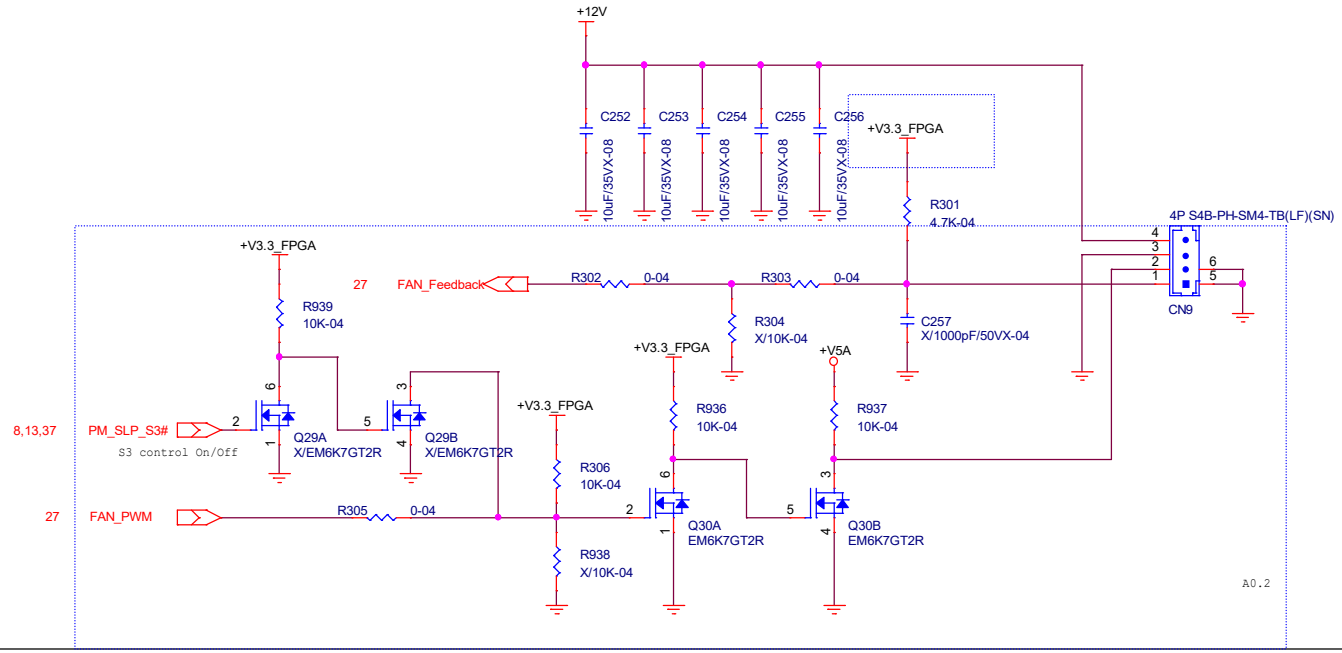




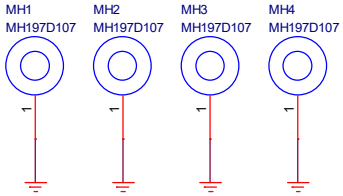
Mounting Holes / PTH



FAN Control



SINK Hold



AAEON an ASUS assoc. co.	Title: H/W Mon/ Debug /CMOS		
	Size: B	Document Number	Rev: A0.2
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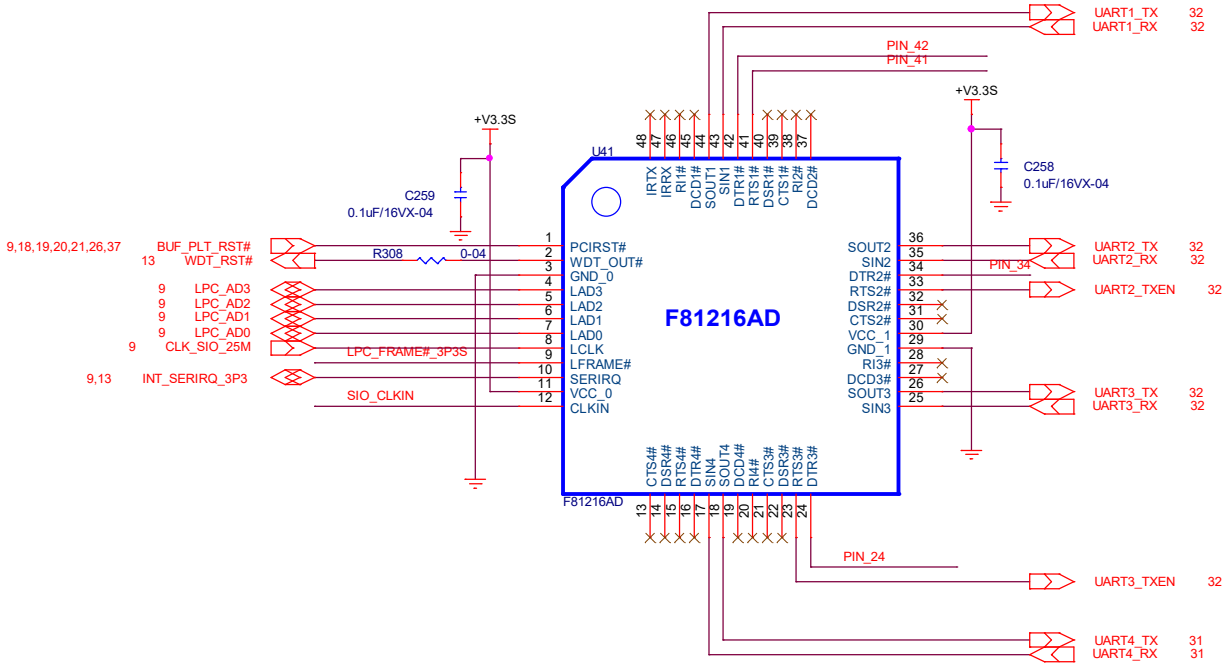
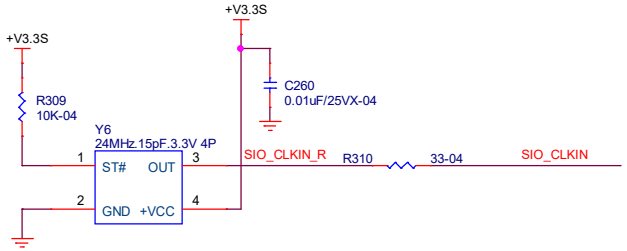
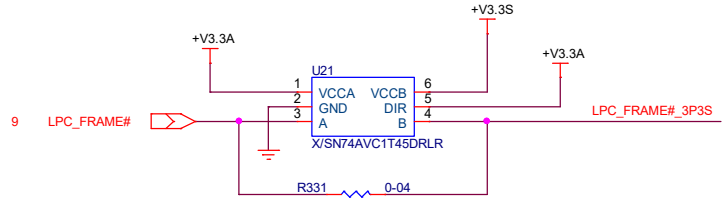
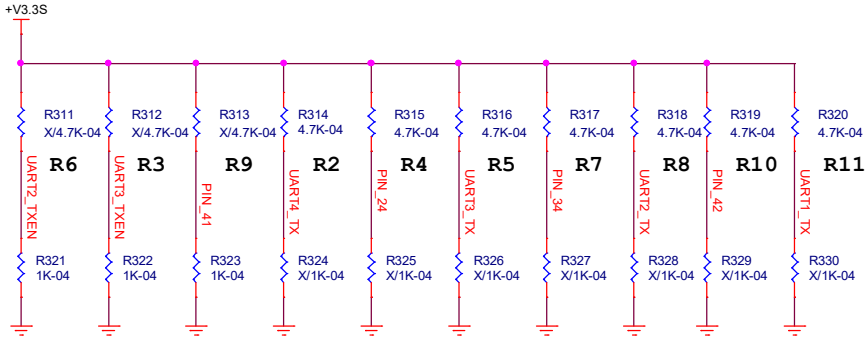


R2 on and R12 off: UART 4 addr:0x2e8 IRQ9; off:UART 4 disabled.
R5 on and R15 off: UART 3 addr:0x3e8 IRQ5; off:UART 3 disabled.
R8 on and R18 off: UART 2 addr:0x2f8 irq4; R7 on, R17 off and R8 off, R18
R6 R3 R9 Entry Key
on : UART 2 addr:0x2e0 IRQ4; R7 off, R17 on and R8 off, R18 on:UART 2
disabled.
R11 on and R21 off: UART 1 addr:0x3f8 irq3; R10 on, R20 off and R11 off, R21
on: UART 1 addr:0x3e0 IRQ3; R10 off, R20 on and R11 off, R21 on:UART 1
disabled.
R4 on and R14 off: Watch Dog Timer enabled and setting to 10 second when the
clock input is 24Mhz. If the clock input is 48Mhz , the timer is setting to
5 second. off :disabled.
R13 is 0 when R3=1, R13 is 1 when R3=0.
R16 is 0 when R6=1, R16 is 1 when R6=0.
R19 is 0 when R9=1, R19 is 1 when R9=0.

UART2_TXEN	UART3_TXEN	PIN_41	Address	Entry Key	On:1
R6	R3	R9			
0	0	0	0x4e/0x4f	0x77	Off:0
0	0	1	0x2e/0x2f	0x77	
0	1	0	0x4e/0x4f	0xa0	
0	1	1	0x2e/0x2f	0xa0	
1	0	0	0x4e/0x4f	0x87	
1	0	1	0x2e/0x2f	0x87	
1	1	0	0x4e/0x4f	0x67	
1	1	1	0x2e/0x2f	0x67	







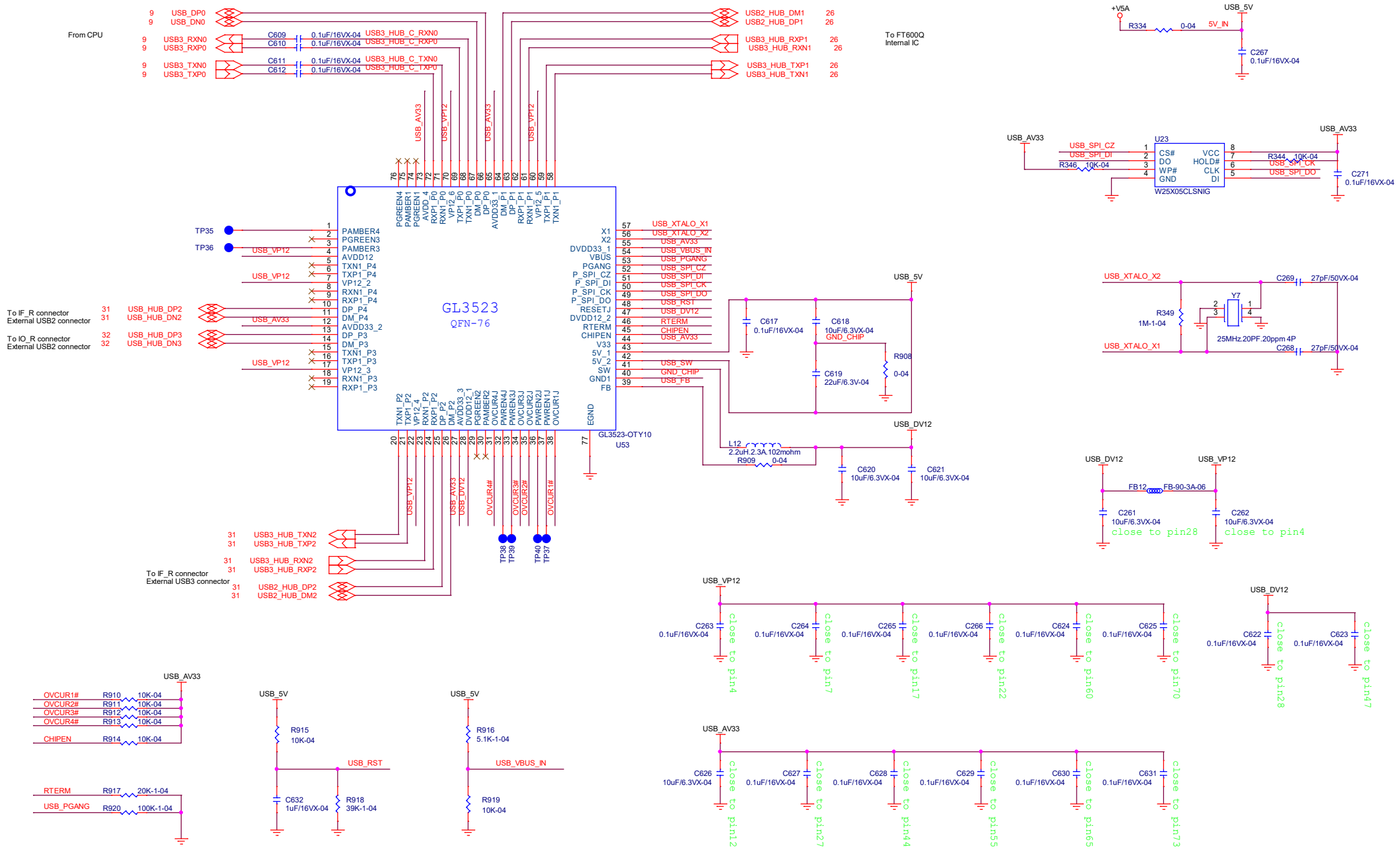
<Core Design>

AAEON an ASUS assoc. co.

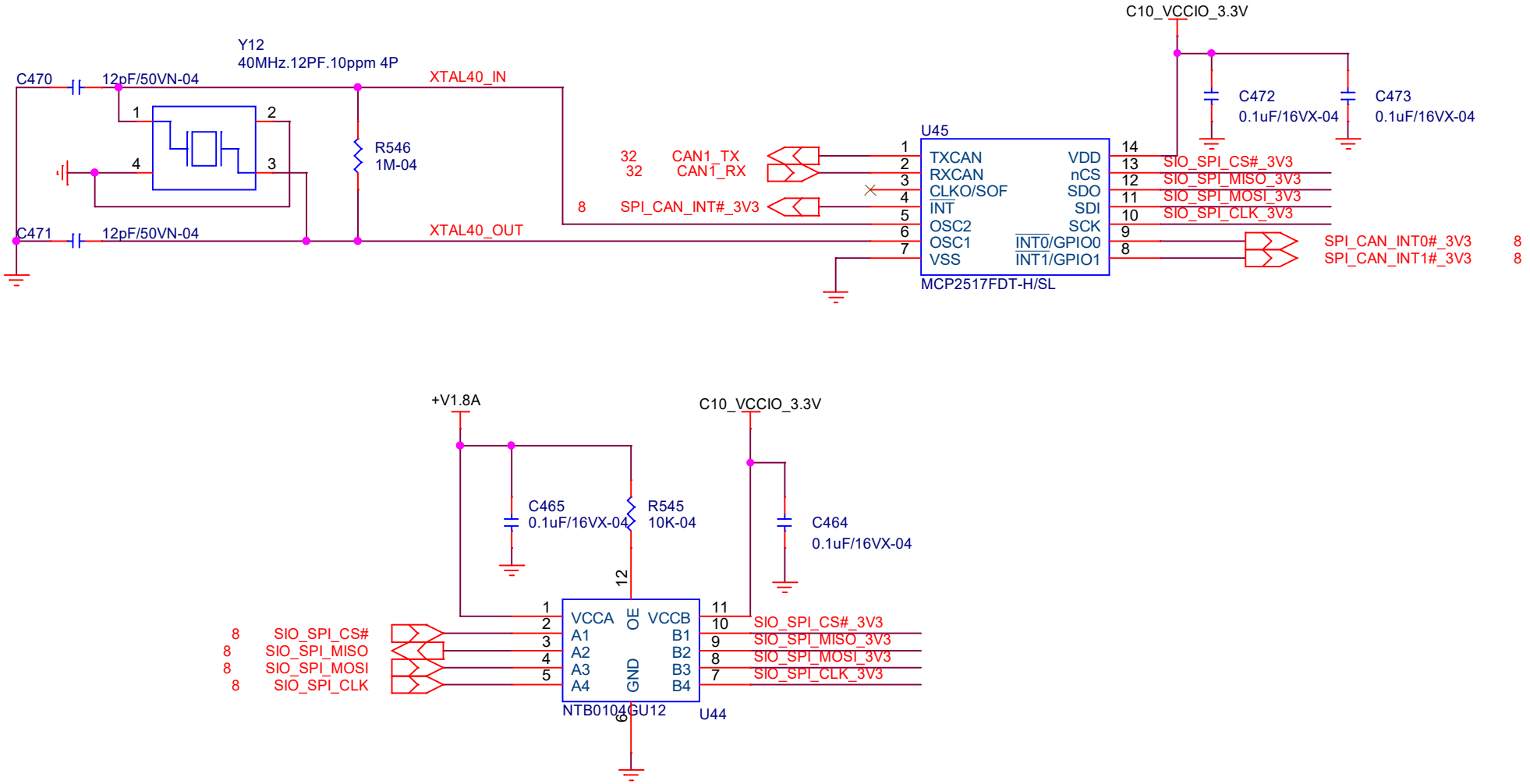
Title: SUPERIO_FINTEK 81966

Size: B | Document Number: HF-MPLC01 | Rev: A0.2

Date: Wednesday, October 16, 2019 | Sheet: 23 of 39

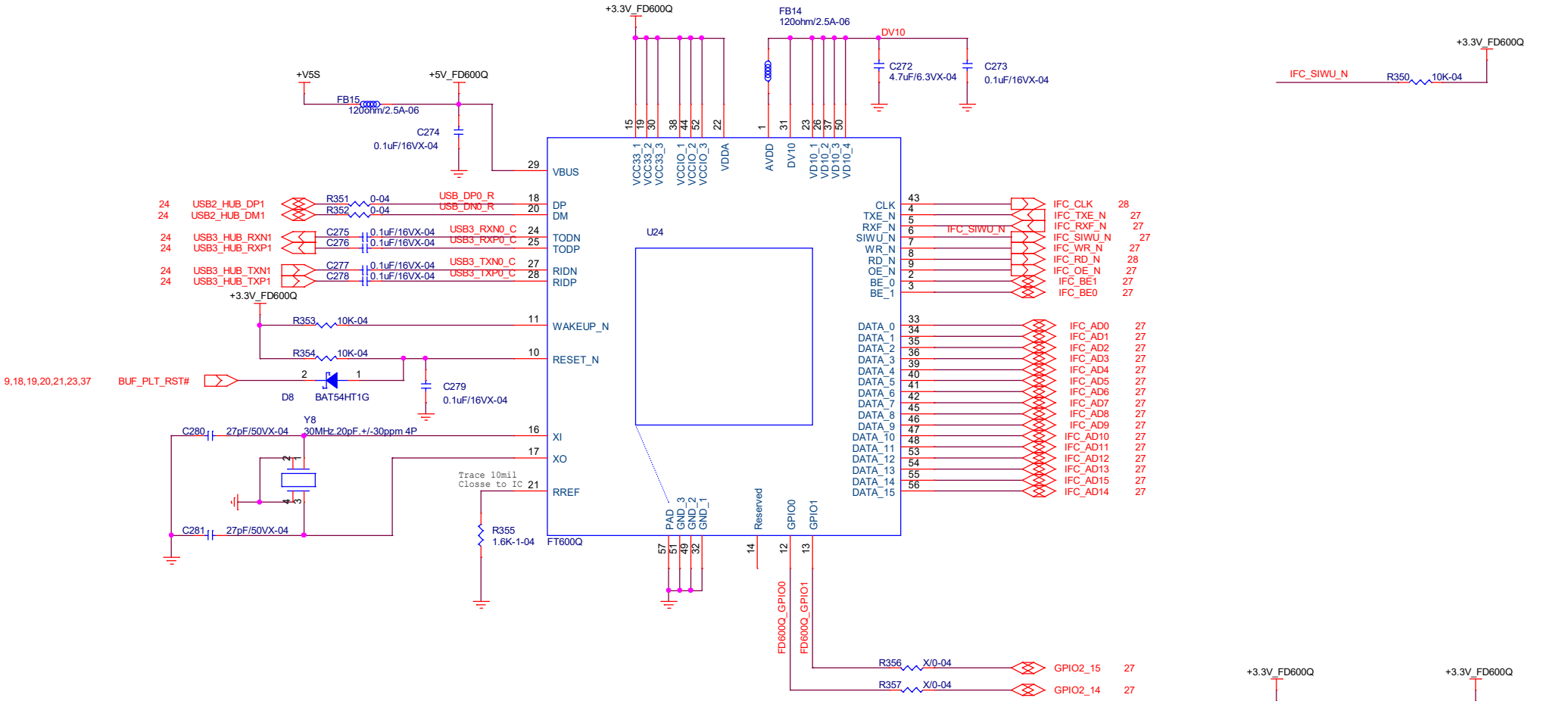


Title: USB3_HUB			
Size: A3	Document Number: HF-MPLC01	Rev: A0.1	
Date: Friday, October 18, 2019	Sheet: 24 of 39		

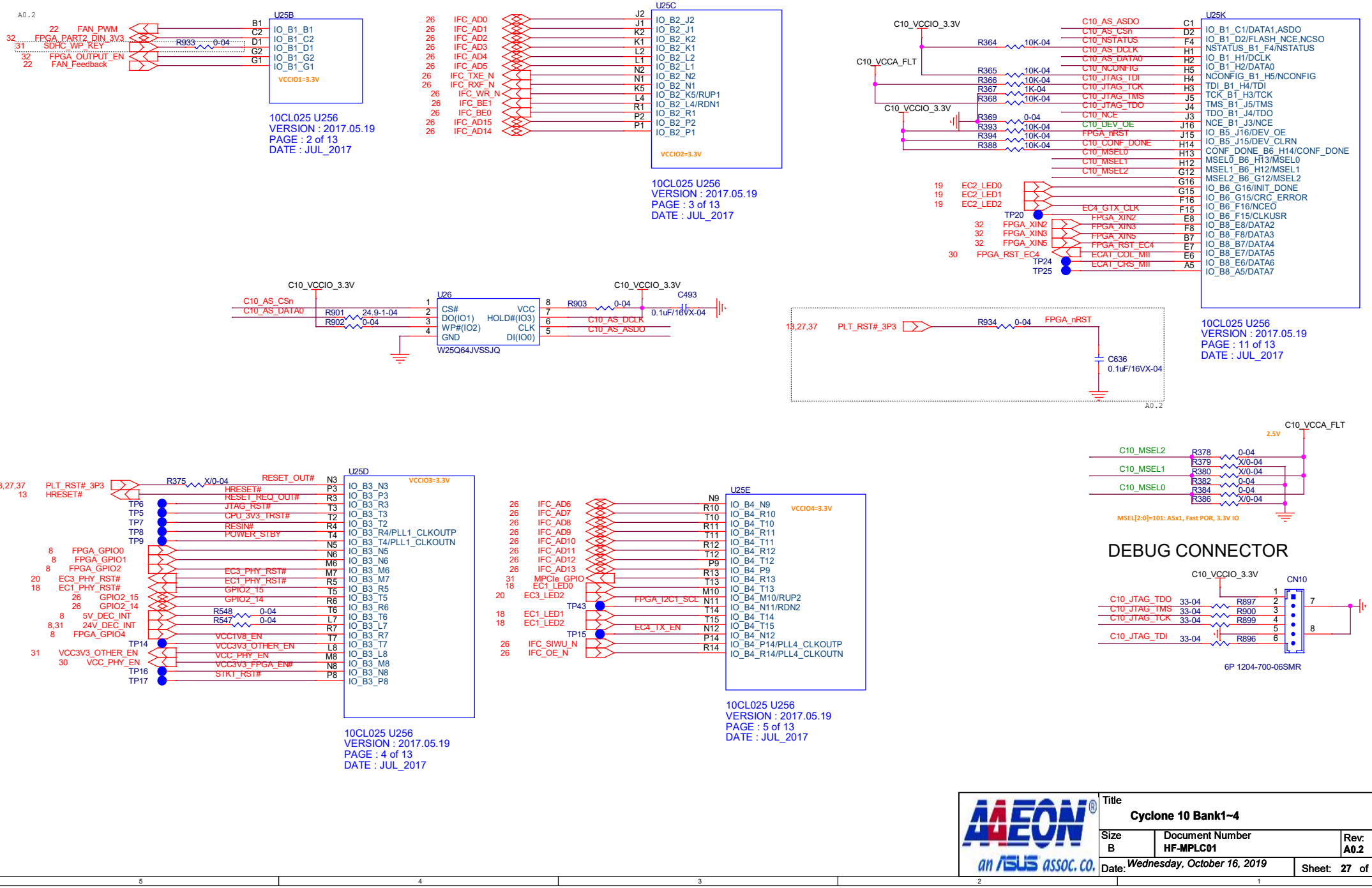


<Core Design>

AAEON an ASUS assoc. co.	Title: **MCP2517FDT SPI to CAN**	
Size: A	Document Number: **HF-MPLC01**	Rev: **A0.2**
Date: *Wednesday, October 16, 2019*	Sheet: **25** of **39**	



Title: FT600Q		
Size: B	Document Number: HF-MPLC01	Rev: A0.2
Date: Wednesday, October 16, 2019		Sheet: 26 of 39


U25B
FAN_PWM
FPGA_PART2_DIN_3V3
SDHC_WP_KEY
FPGA_OUTPUT_EN
FAN_Feedback
R933 0-04
IO_B1_B1
IO_B1_C2
IO_B1_D1
IO_B1_G2
IO_B1_G1
VCCIO1=3.3V
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U25C
IFC_AD0
IFC_AD1
IFC_AD2
IFC_AD3
IFC_AD4
IFC_AD5
IFC_TXE_N
IFC_RXF_N
IFC_WR_N
IFC_BE1
IFC_BE0
IFC_AD15
IFC_AD14
IO_B2_J2
IO_B2_J1
IO_B2_K2
IO_B2_K1
IO_B2_L2
IO_B2_L1
IO_B2_N2
IO_B2_N1
IO_B2_K5/RUP1
IO_B2_L4/RDN1
IO_B2_R1
IO_B2_P2
IO_B2_P1
VCCIO2=3.3V
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DATE : JUL_2017
C10_VCCIO_3.3V
C10_VCCA_FLT
R364 10K-04
R365 10K-04
R366 10K-04
R367 1K-04
R368 10K-04
R369 0-04
R393 10K-04
R394 10K-04
R388 10K-04
U25K
C10_AS_ASDO
C10_AS_CSn
C10_NSTATUS
C10_AS_DCLK
C10_AS_DATA0
C10_NCONFIG
C10_JTAG_TDI
C10_JTAG_TCK
C10_JTAG_TMS
C10_JTAG_TDO
C10_NCE
C10_DEV_OE
FPGA_nRST
C10_CONF_DONE
C10_MSEL0
C10_MSEL1
C10_MSEL2
IO_B1_C1/DATA1,ASDO
IO_B1_D2/FLASH_NCE,NCSO
NSTATUS_B1_F4/NSTATUS
IO_B1_H1/DCLK
IO_B1_H2/DATA0
NCONFIG_B1_H5/NCONFIG
TDI_B1_H4/TDI
TCK_B1_H3/TCK
TMS_B1_J5/TMS
TDO_B1_J4/TDO
NCE_B1_J3/NCE
IO_B5_J16/DEV_OE
IO_B5_J15/DEV_CLRN
CONF_DONE_B6_H14/CONF_DONE
MSEL0_B6_H13/MSEL0
MSEL1_B6_H12/MSEL1
MSEL2_B6_G12/MSEL2
IO_B6_G16/INIT_DONE
IO_B6_G15/CRC_ERROR
IO_B6_F16/NCEO
IO_B6_F15/CLKUSR
IO_B8_E8/DATA2
IO_B8_F8/DATA3
IO_B8_B7/DATA4
IO_B8_E7/DATA5
IO_B8_E6/DATA6
IO_B8_A5/DATA7
EC2_LED0
EC2_LED1
EC2_LED2
TP20
EC4_GTX_CLK
FPGA_XIN2
FPGA_XIN3
FPGA_XIN5
FPGA_RST_EC4
ECAT_COL_MII
ECAT_CRS_MII
TP24
TP25
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DATE : JUL_2017
C10_VCCIO_3.3V
C10_AS_CSn
C10_AS_DATA0
R901 24.9-1-04
R902 0-04
U26
CS#
DO(IO1)
WP#(IO2)
GND
VCC
HOLD#(IO3)
CLK
DI(IO0)
W25Q64JVSSJQ
R903 0-04
C10_AS_DCLK
C10_AS_ASDO
C493
0.1uF/16VX-04
13,27,37
PLT_RST#_3P3
R934 0-04
FPGA_nRST
C636
0.1uF/16VX-04
C10_VCCA_FLT
2.5V
C10_MSEL2
C10_MSEL1
C10_MSEL0
R378 0-04
R379 X/0-04
R380 X/0-04
R382 0-04
R384 0-04
R386 X/0-04
MSEL[2:0]=101: ASx1, Fast POR, 3.3V IO
DEBUG CONNECTOR
C10_VCCIO_3.3V
CN10
C10_JTAG_TDO
C10_JTAG_TMS
C10_JTAG_TCK
C10_JTAG_TDI
R897 33-04
R900 33-04
R899 33-04
R896 33-04
6P 1204-700-06SMR
U25D
VCCIO3=3.3V
PLT_RST#_3P3
HRESET#
R375 X/0-04
RESET_OUT#
HRESET#
RESET_REQ_OUT#
JTAG_RST#
CPU_3V3_TRST#
RESIN#
POWER_STBY
FPGA_GPIO0
FPGA_GPIO1
FPGA_GPIO2
EC3_PHY_RST#
EC1_PHY_RST#
GPIO2_15
GPIO2_14
5V_DEC_INT
24V_DEC_INT
FPGA_GPIO4
VCC1V8_EN
VCC3V3_OTHER_EN
VCC_PHY_EN
VCC3V3_FPGA_EN#
STKI_RST#
R548 0-04
R547 0-04
IO_B3_N3
IO_B3_P3
IO_B3_R3
IO_B3_T3
IO_B3_T2
IO_B3_R4/PLL1_CLKOUTP
IO_B3_T4/PLL1_CLKOUTN
IO_B3_N5
IO_B3_N6
IO_B3_M6
IO_B3_M7
IO_B3_R5
IO_B3_T5
IO_B3_R6
IO_B3_T6
IO_B3_L7
IO_B3_R7
IO_B3_T7
IO_B3_L8
IO_B3_M8
IO_B3_N8
IO_B3_P8
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U25E
VCCIO4=3.3V
IFC_AD6
IFC_AD7
IFC_AD8
IFC_AD9
IFC_AD10
IFC_AD11
IFC_AD12
IFC_AD13
MPCIe_GPIO
EC1_LED0
EC3_LED2
FPGA_I2C1_SCL
EC1_LED1
EC1_LED2
EC4_IX_EN
IFC_SIWU_N
IFC_OE_N
IO_B4_N9
IO_B4_R10
IO_B4_T10
IO_B4_R11
IO_B4_T11
IO_B4_R12
IO_B4_T12
IO_B4_P9
IO_B4_R13
IO_B4_T13
IO_B4_M10/RUP2
IO_B4_N11/RDN2
IO_B4_T14
IO_B4_T15
IO_B4_N12
IO_B4_P14/PLL4_CLKOUTP
IO_B4_R14/PLL4_CLKOUTN
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AAEON
an ASUS assoc. co.
Title
Cyclone 10 Bank1~4
Size B
Document Number HF-MPLC01
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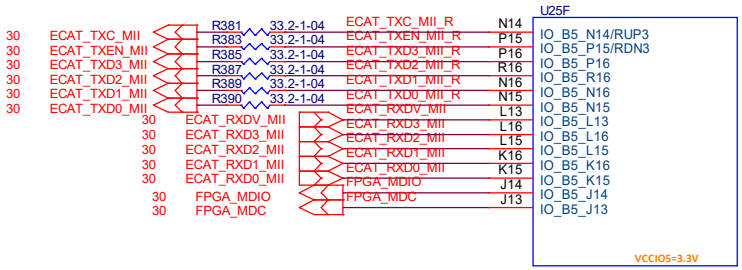

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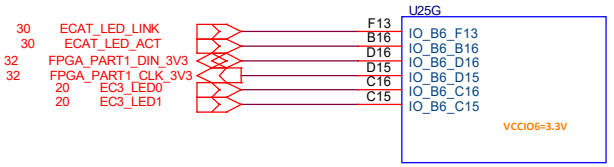
DATE : JUL_2017



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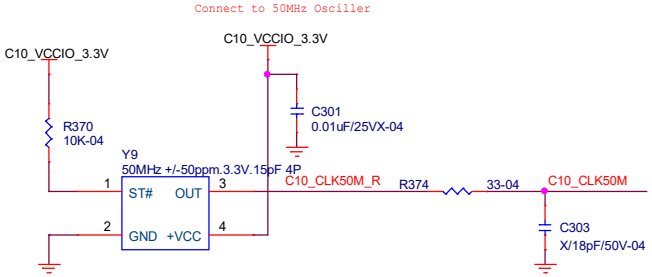

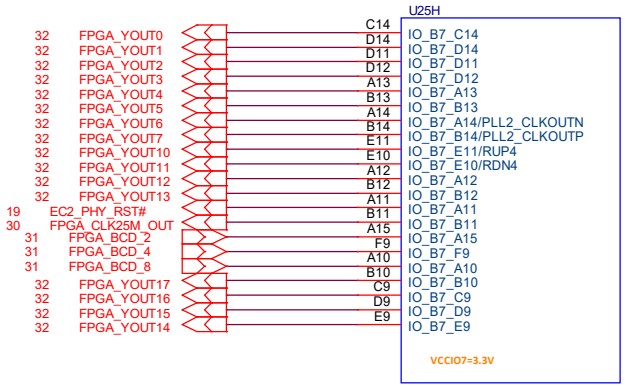

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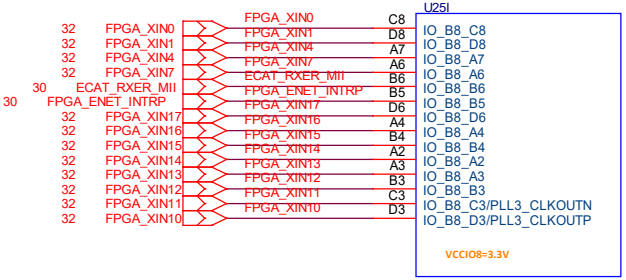
DATE : JUL_2017



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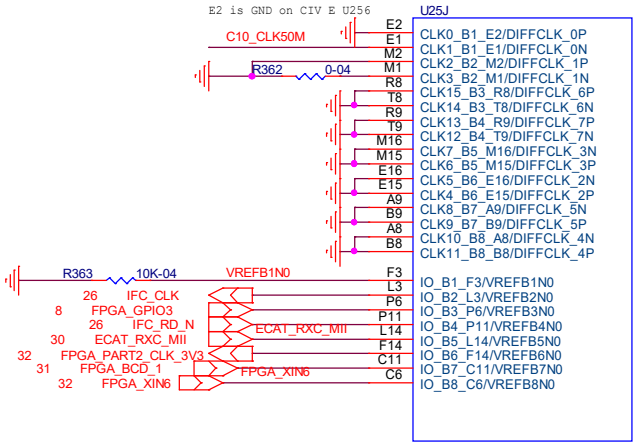

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AAEON an ASUS assoc. co.

Title: **Cyclone 10 Bank5~8**

Size	Document Number	Rev:
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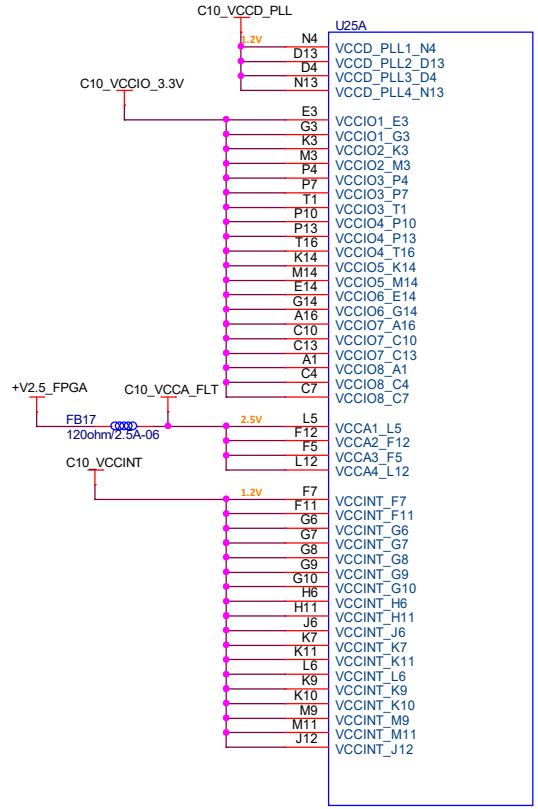

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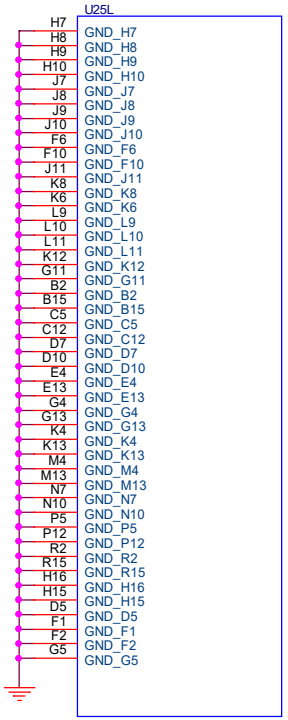

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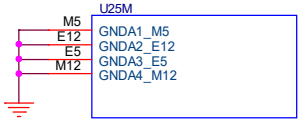
D5, F1, F2, G5 are IO on CIV E U256



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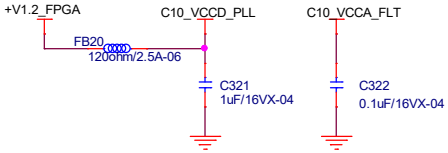
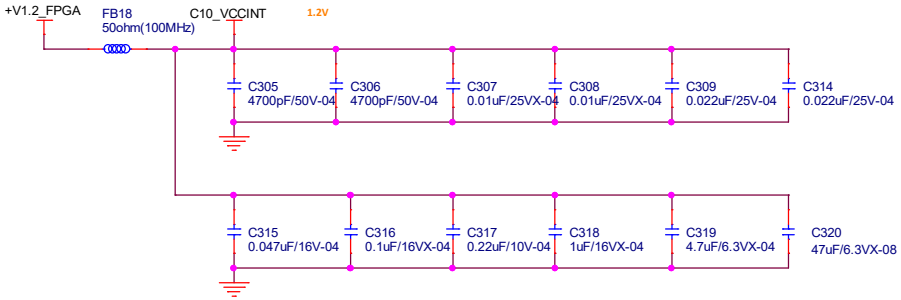
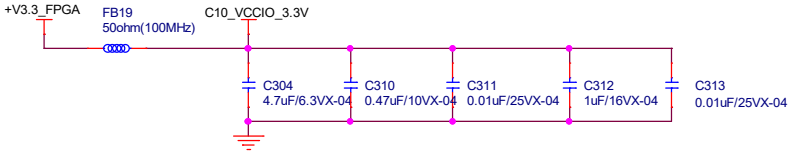
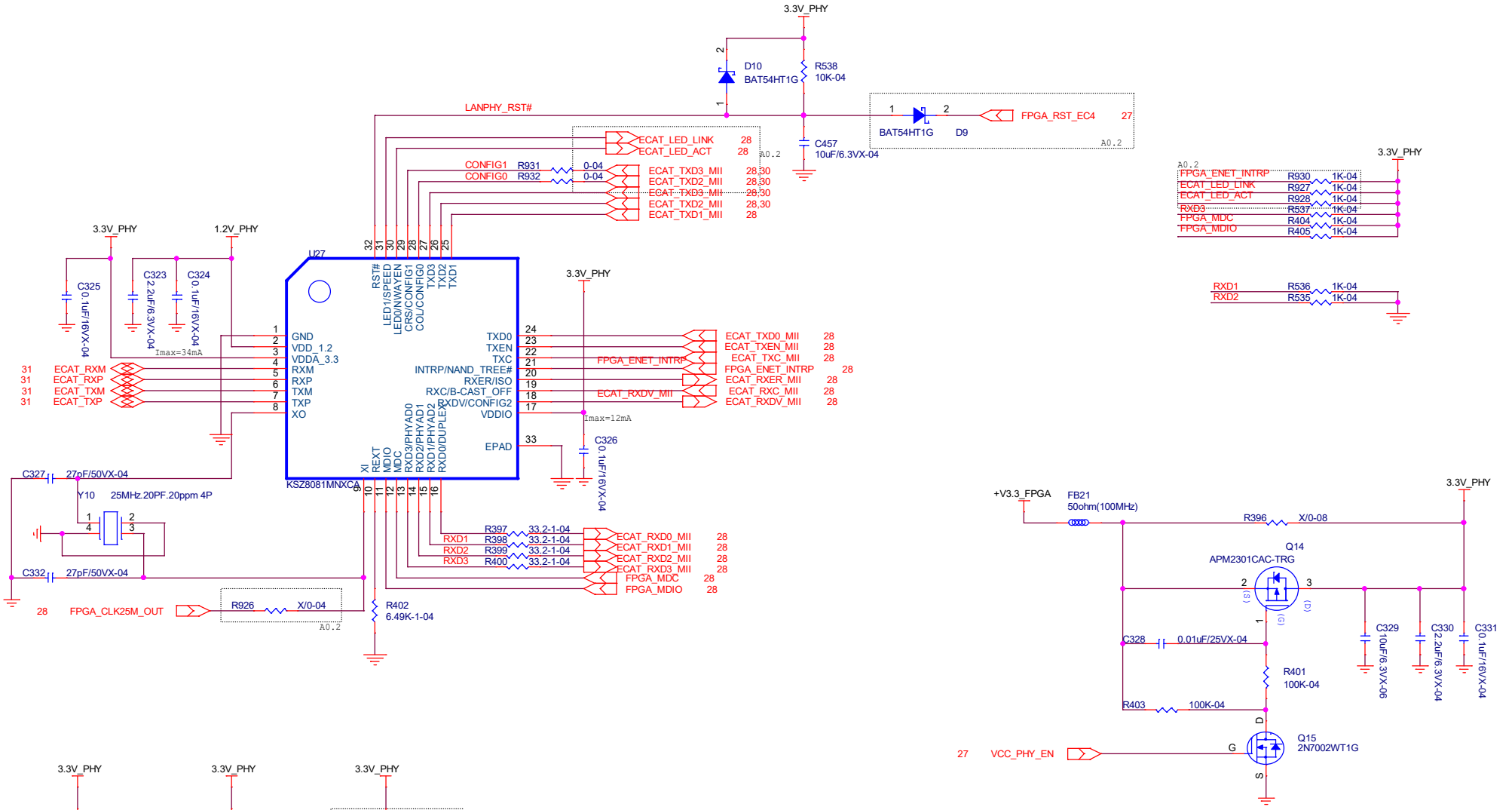






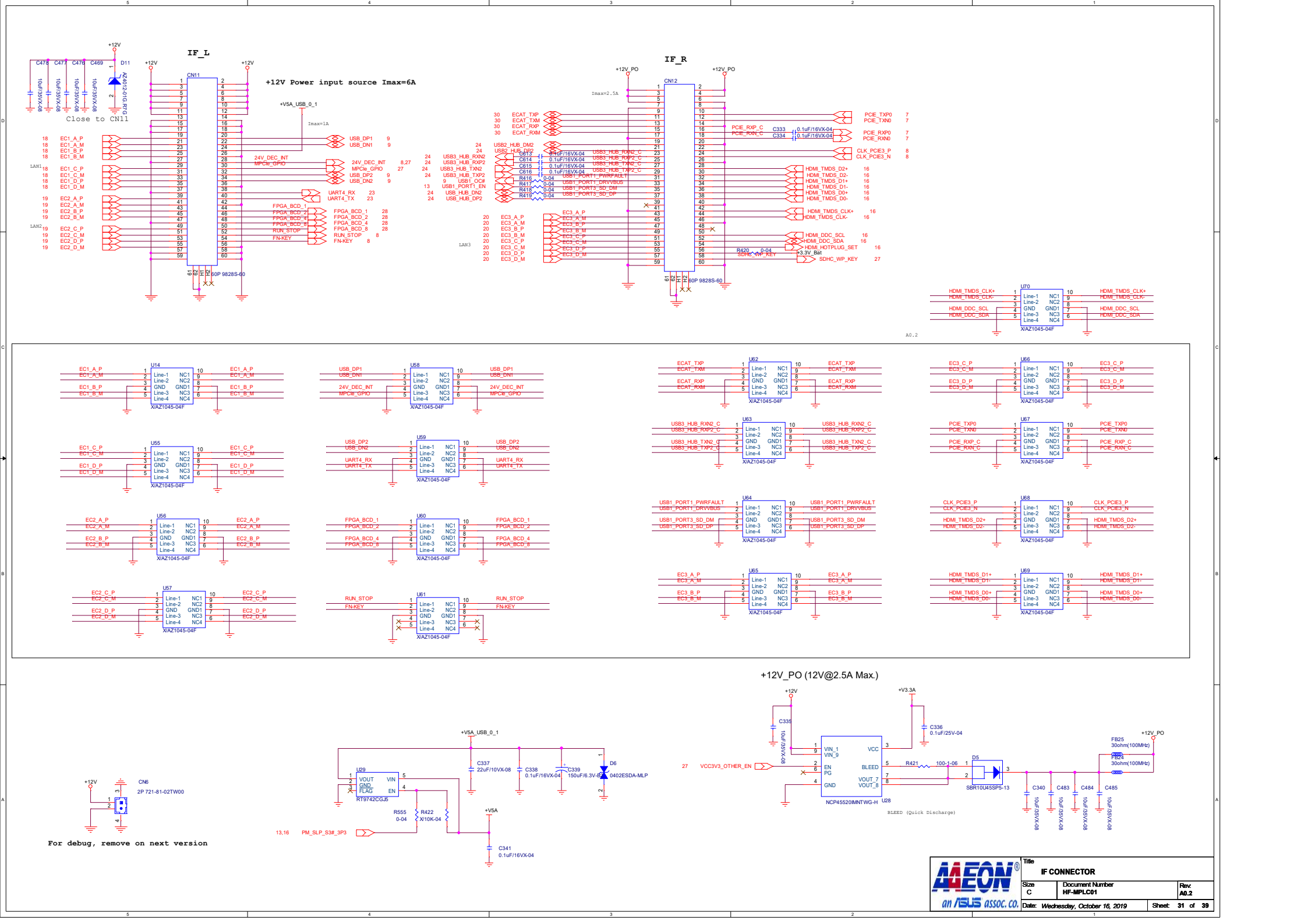
AAEON an ASUS assoc. co.

Title: Cyclone 10 Power		
Size: B	Document Number: HF-MPLC01	Rev: A0.2
Date: *Wednesday, October 16, 2019*	Sheet: 29 of 39	



CONFIG[2:0]	Mode
001	RMII
101	RMII back-to-back
000, 010 ~ 100, 110, 111	Reserved - not used

AAEON an ASUS assoc. co.	Title: LAN PHY		
	Size: B	Document Number: HF-MPLC01	Rev: A0.2
	Date: Wednesday, October 16, 2019		Sheet: 30 of 39



Title	IF CONNECTOR		
Size C	Document Number HF-MPLC01		Rev. A0.2
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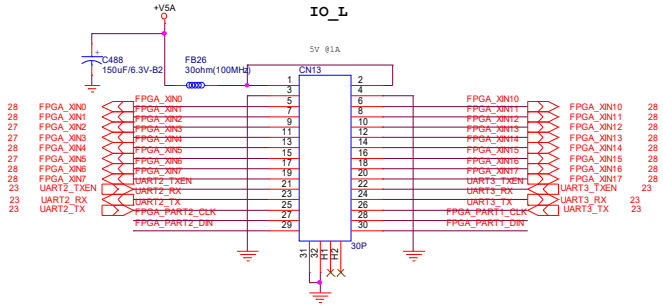

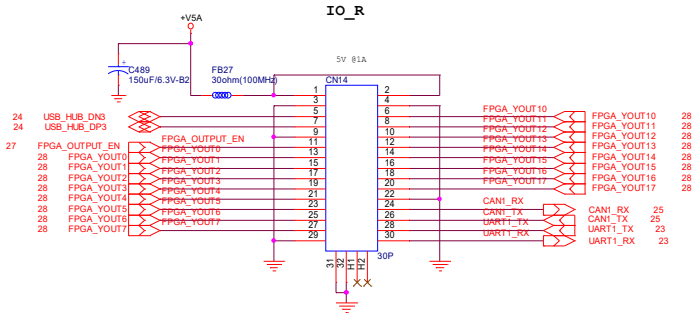

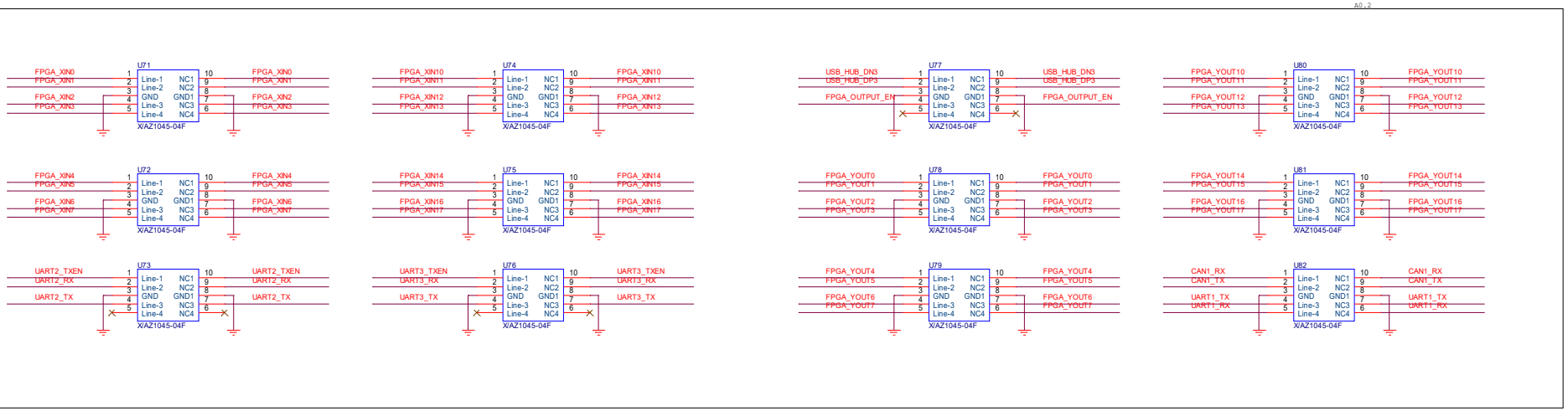

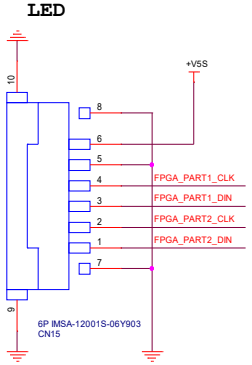

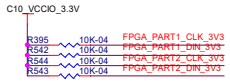

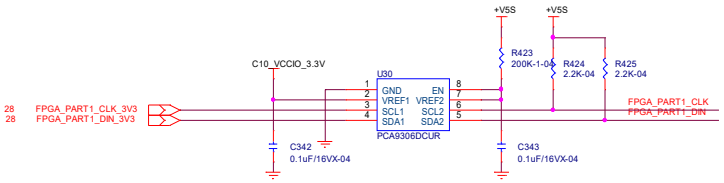

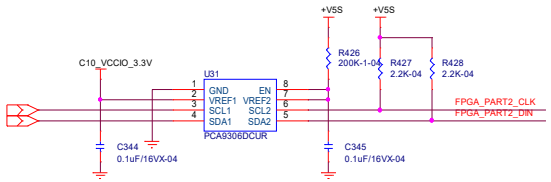

AAEON an ASUS assoc. co.	Title: IO CONNECTOR		
	Size: C	Document Number: HF-MPLC01	Rev: A0.2
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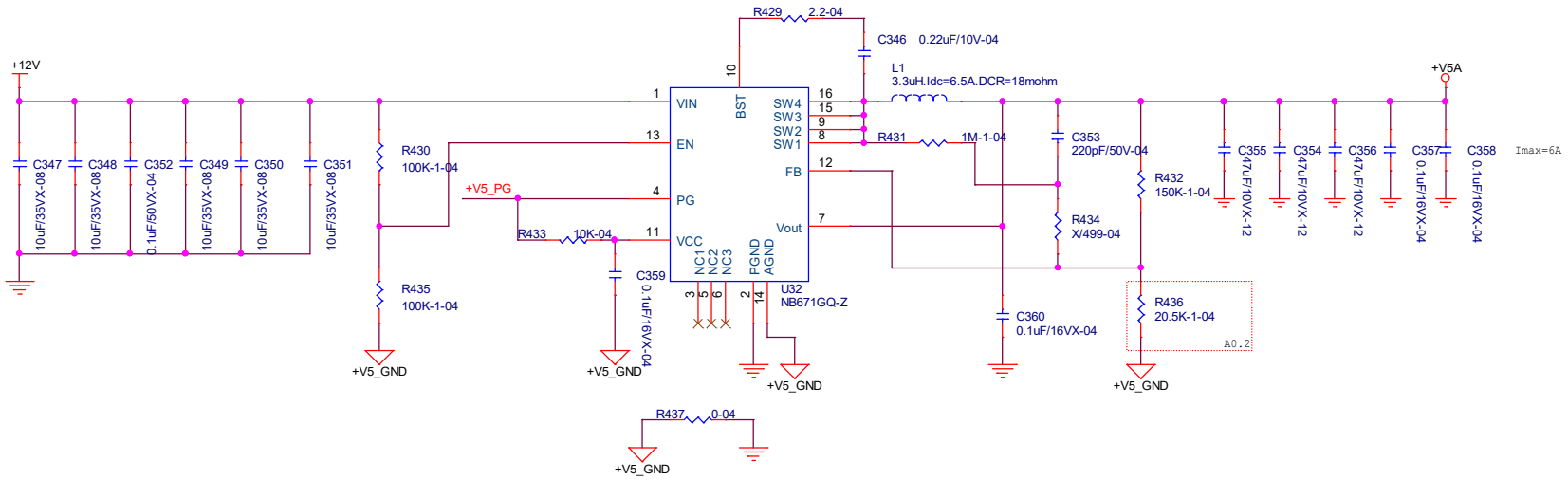
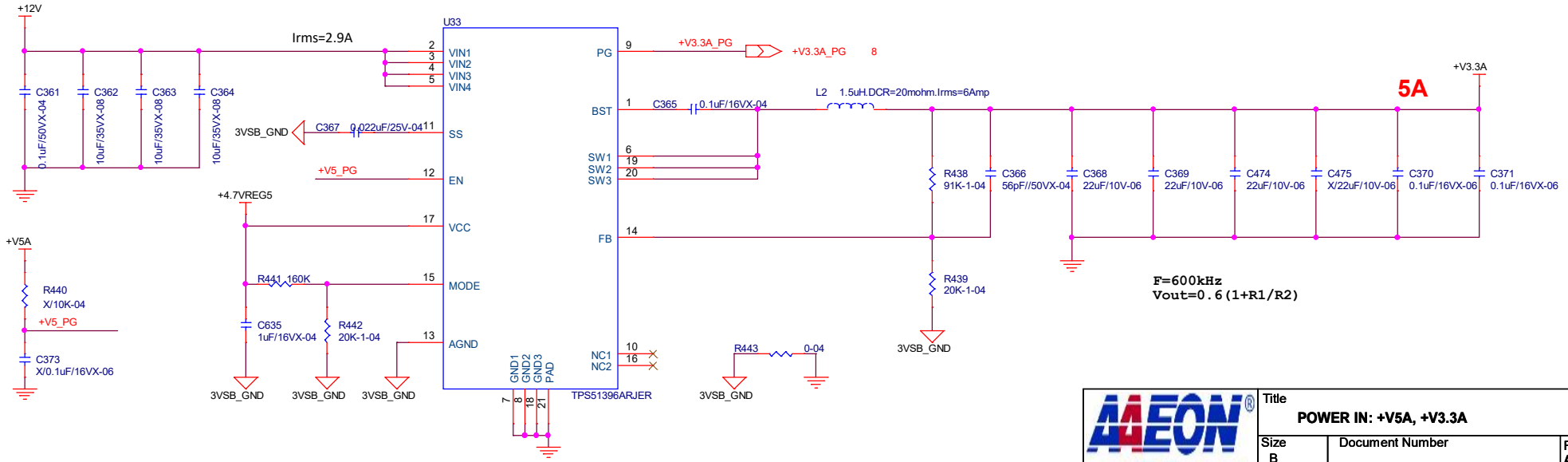
+12V Power Input

Power From IF_L connector



+V3.3A

A0.2



AAEON an ASUS assoc. co.	Title: POWER IN: +V5A, +V3.3A	
	Size: B	Document Number	Rev: A0.2
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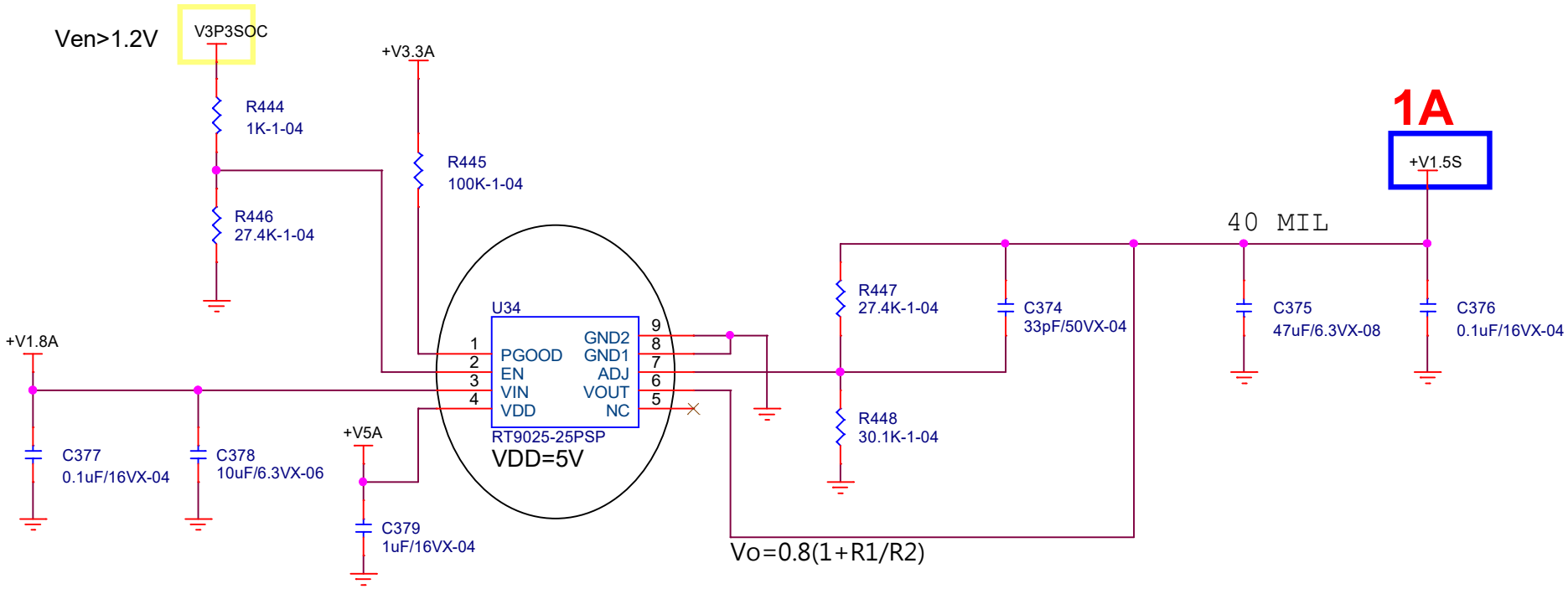
+V1.5S



AAEON an ASUS assoc. co.	Title: **POWER VR_LDO**	
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Q34,R671 colay

V5PMIC: 6A

VRTC: 0.12A
V3P3A: 0.1A
V3P3S: 0.5A
V1P2A: 0.05A
VSDIO: 0.02A

V5PMIC: 1A
V1P0S: 2.667A

V5PMIC: 3.5A
VCC: 13.541A

V5PMIC: 3.5A
VNN: 13.207A

V5PMIC: 1.5A
VDDQ: 4.35A

V1P8S: 0.8A
V1P2S: 0.05A
VSFR: 0.5A

VTT: 0.53A

A0.2 Add R762,R763,R764 for workaround

CPU	
Input Voltage Range	5.5V to 20V
Max Current	12A
Thermal Design Current	7.5A
Dynamic Current	7.5A
Over Current Level	18A
Switching Frequency	400K
DC Load-line	5.9mohm

AAEON an ASUS assoc. co.

Title: POWER VR_PMIC

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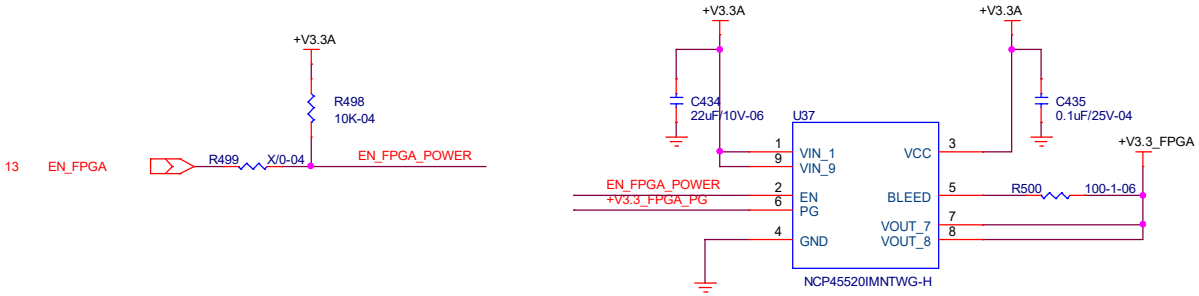
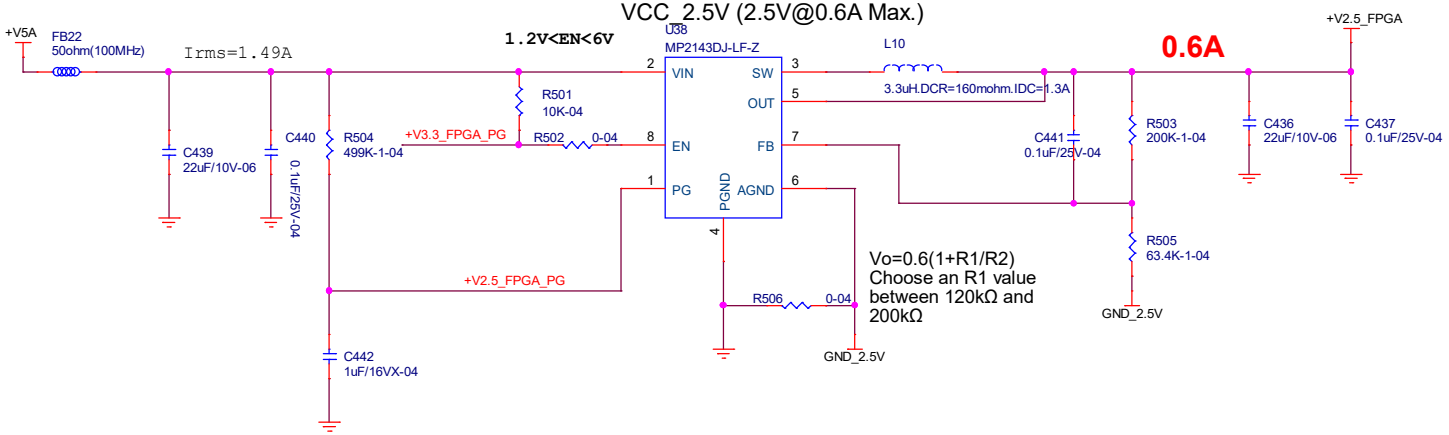
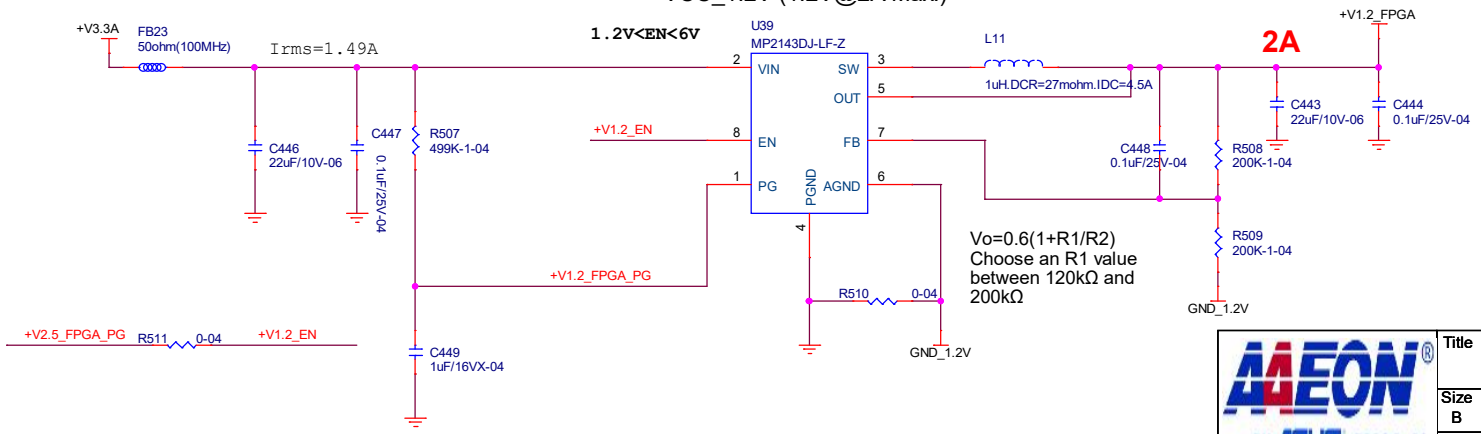
VCC_3.3V (3.3V@3A Max.)



VCC_2.5V (2.5V@0.6A Max.)



VCC_1.2V (1.2V@2A Max.)



AAEON an ASUS assoc. co.	Title: **FPGA Power-I**		
	Size: **B**	Document Number: **HF-MPLC01**	Rev: **A0.2**
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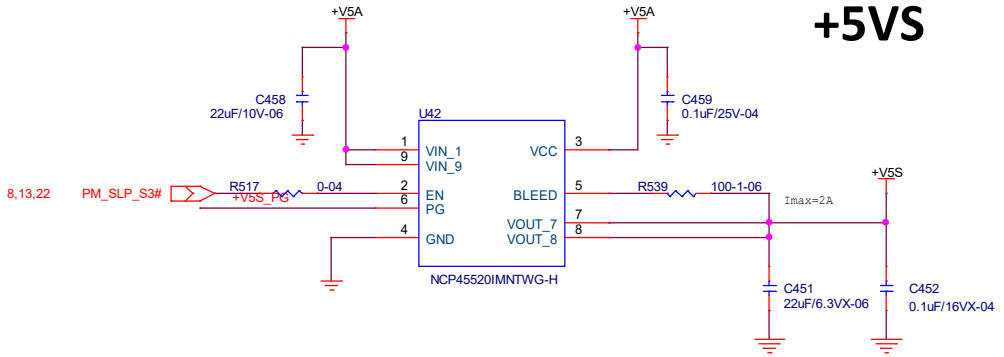
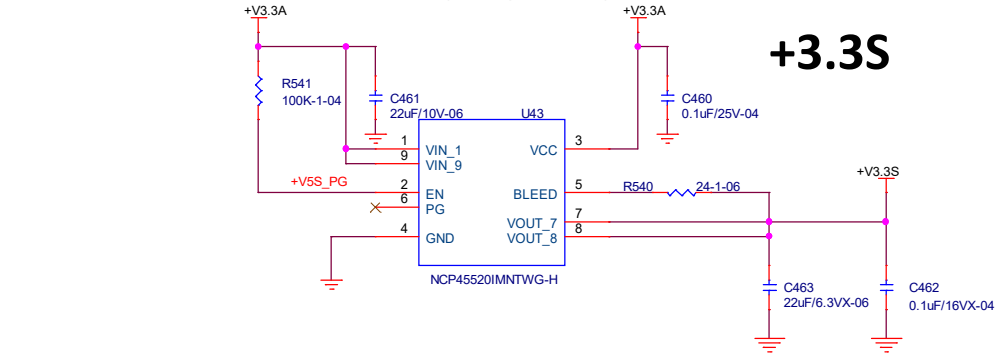
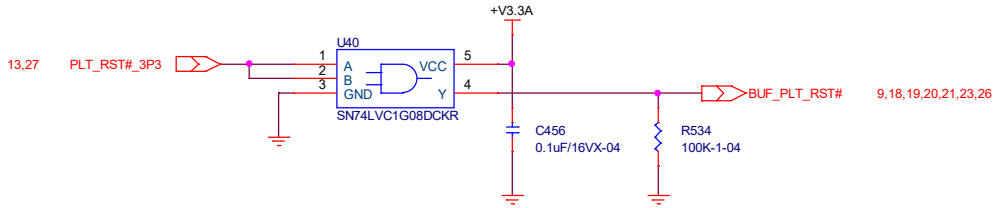
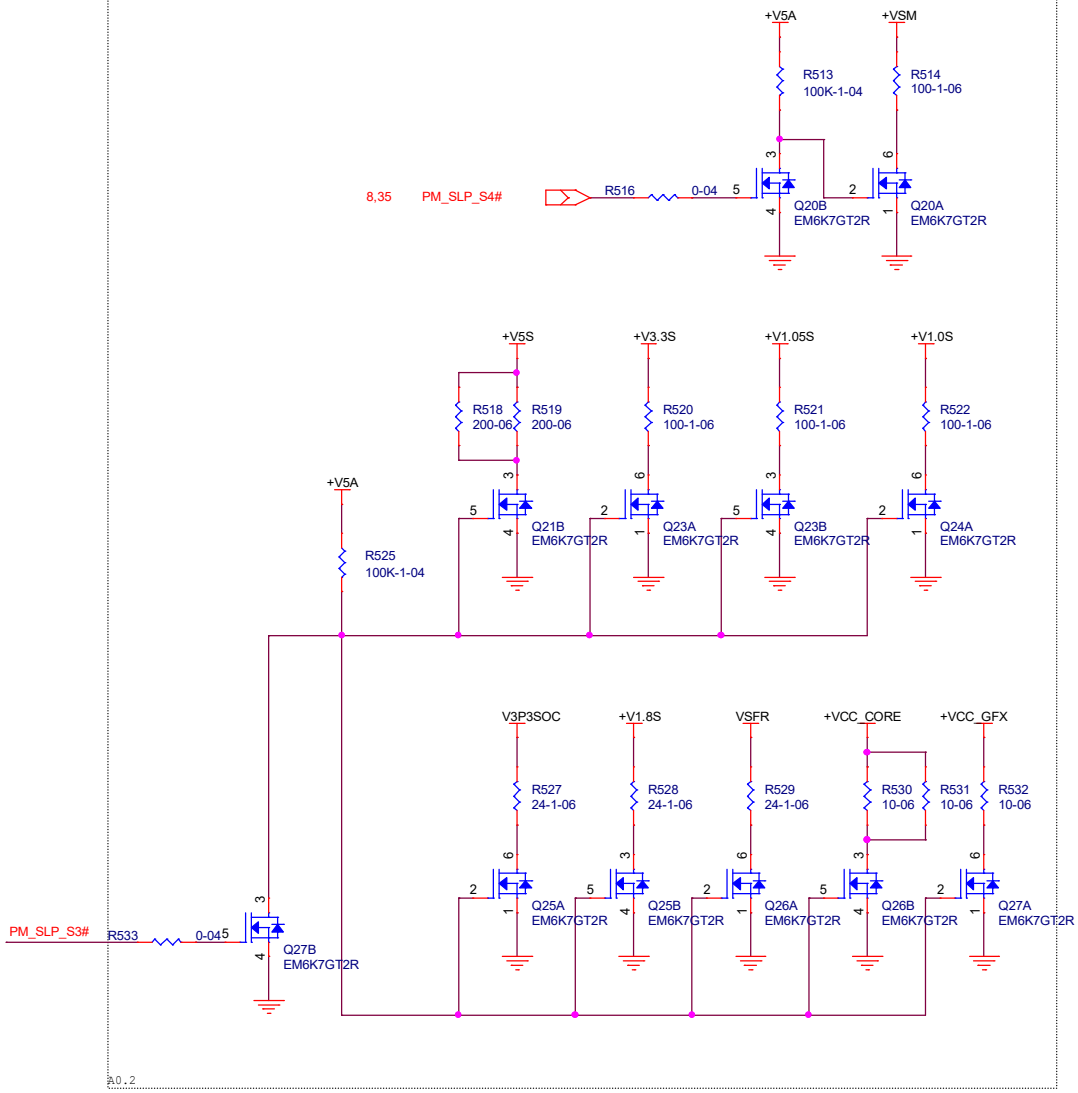
+5VS (5V@5A Max.)



+3.3S (3.3V@5A Max.)







<Variant Name>

AAEON an ASUS assoc. co.	Title: Power Sequence Logic	
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A0.2

1.Change CN1 CN2 CN3 CN4 Footpint.
2.3.3V power solution phase out change to TPS51396ARJER.
3. Add ESD protect IC on IF IO connector
4. Change RTC crystal to ESR 50Kohm.
5. Modify pin define of FAN connector.
6. Add pull up resistor on HRESET#.
7. Add Pull up resistor on FPGA_ENET_INTRP.
8. Add ECAT_COL_MII to CONFIG0 of LAN PHY.
9. Add ECAT_CRS_MII to CONFIG1 of LAN PHY.
10.Revers D9.
11.Change C257 to 1000pF.
12.Add Cap on FPGA_nRST.
13.Modify FPGA pin out as below.

Net name	FPGA
EC1_LED0	T13
EC1_LED1	T14
EC1_LED2	T15
EC2_LED0	G16
EC2_LED1	G15
EC2_LED2	F16
ECAT_LED_LINK	F13
ECAT_LED_ACT	B16
EC3_LED0	C16
EC3_LED1	C15
EC3_LED2	M10

14.Change VGA connector type to FPC.
15.Modify FAN control circuit.

<Variant Name>

AAEON an ASUS assoc. co.

Title: History

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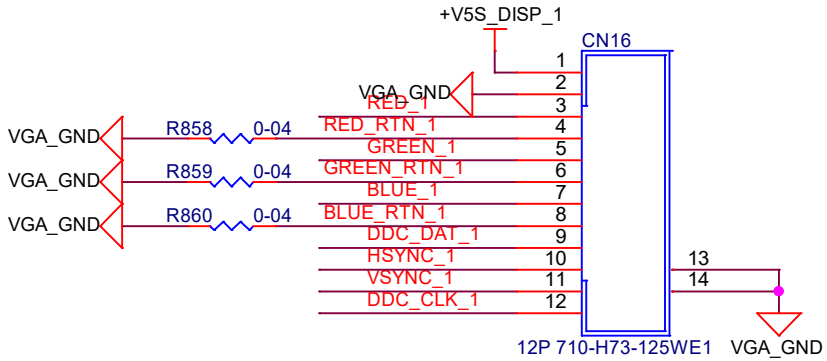

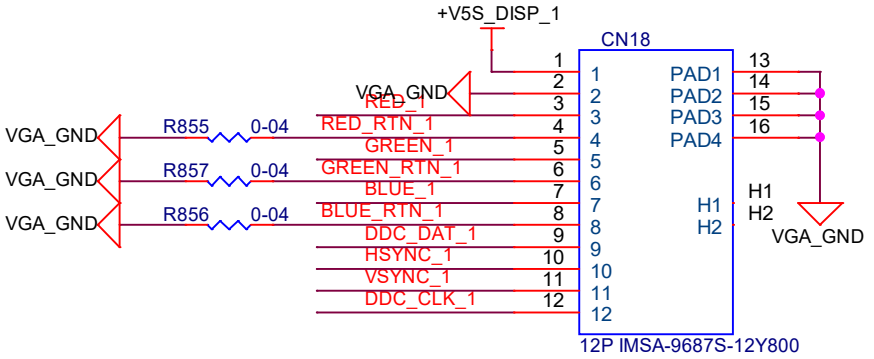

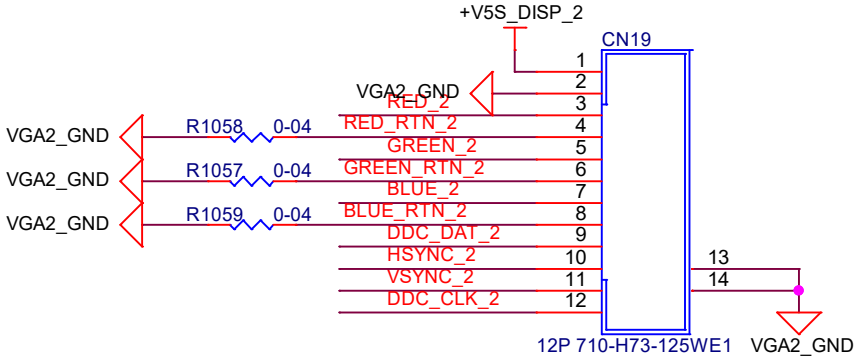

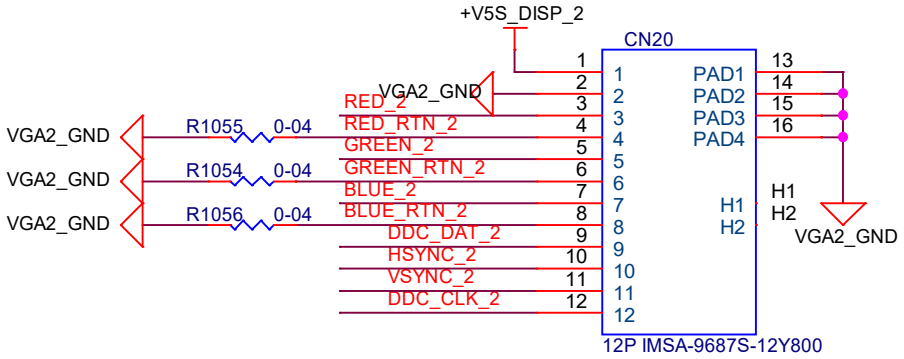

<Variant Name>

AAEON an ASUS assoc. co.	Title: **Test Board**	
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