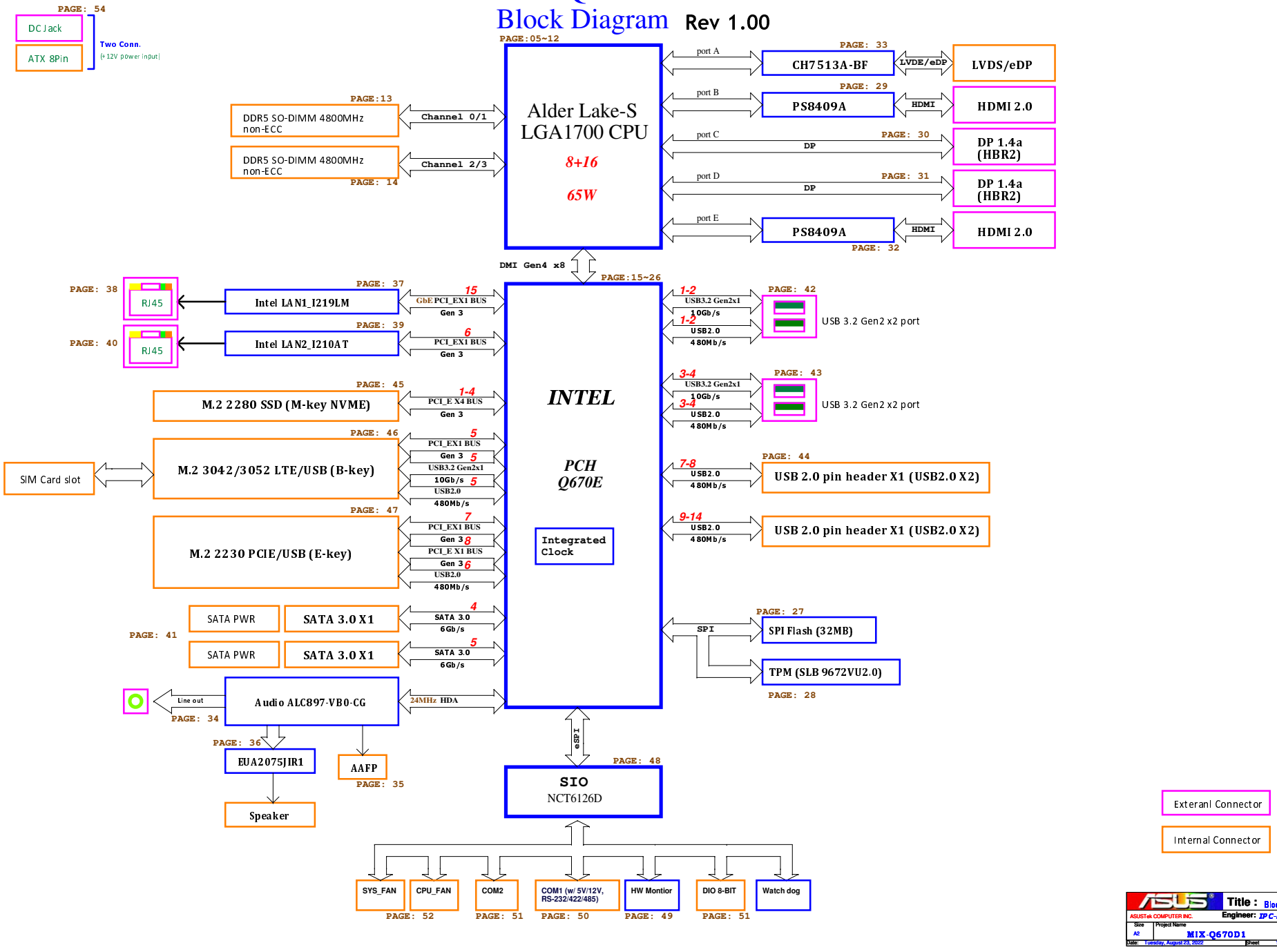
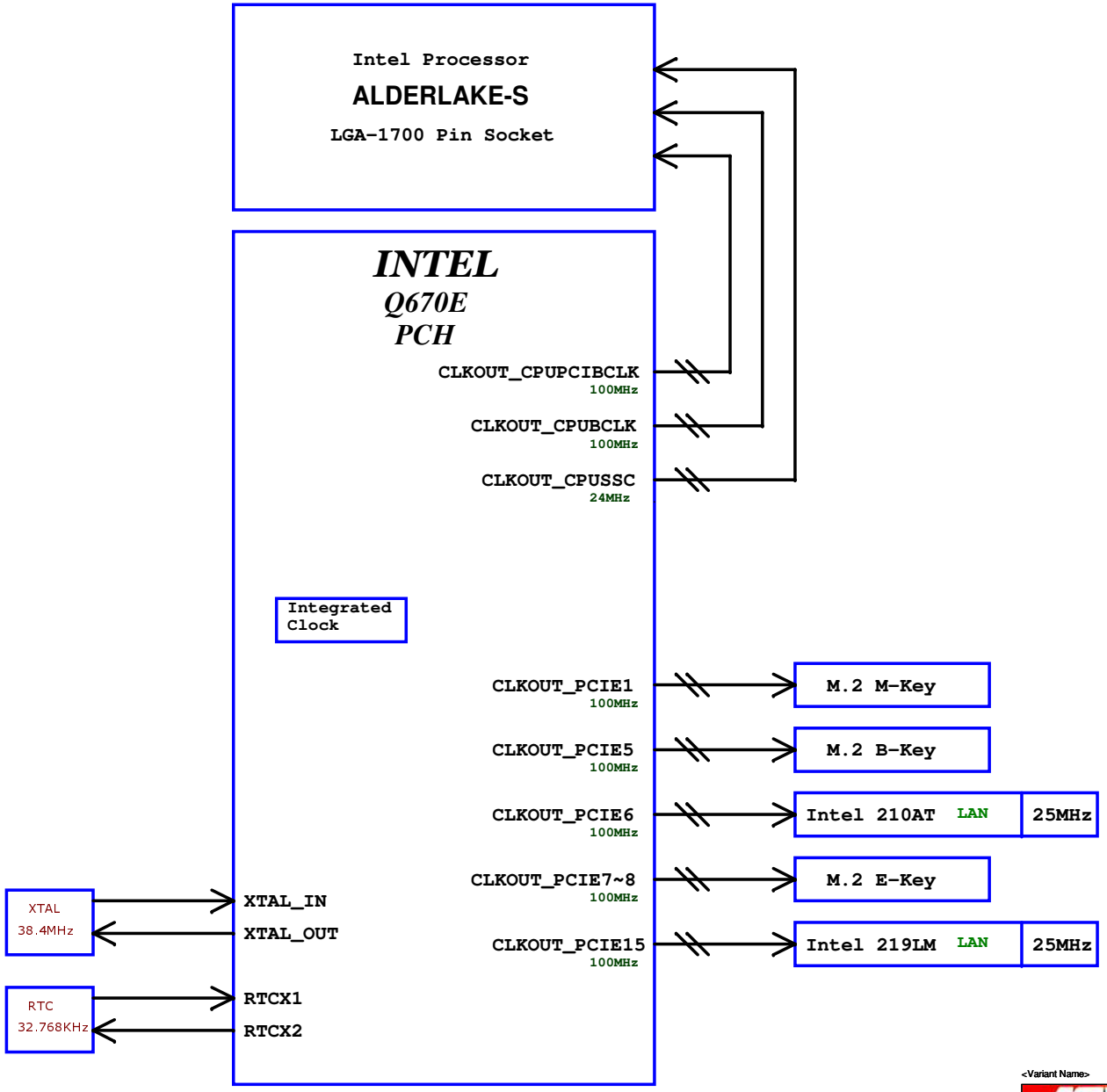
MIX-Q670D1
Block Diagram Rev 1.00



ASUSTeK COMPUTER INC.	Title : Block Diagram		
	Engineer: IPC-EE2		
Size: A2	Project Name: MIX-Q670D1		Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 1 of 70		



<Variant Name>

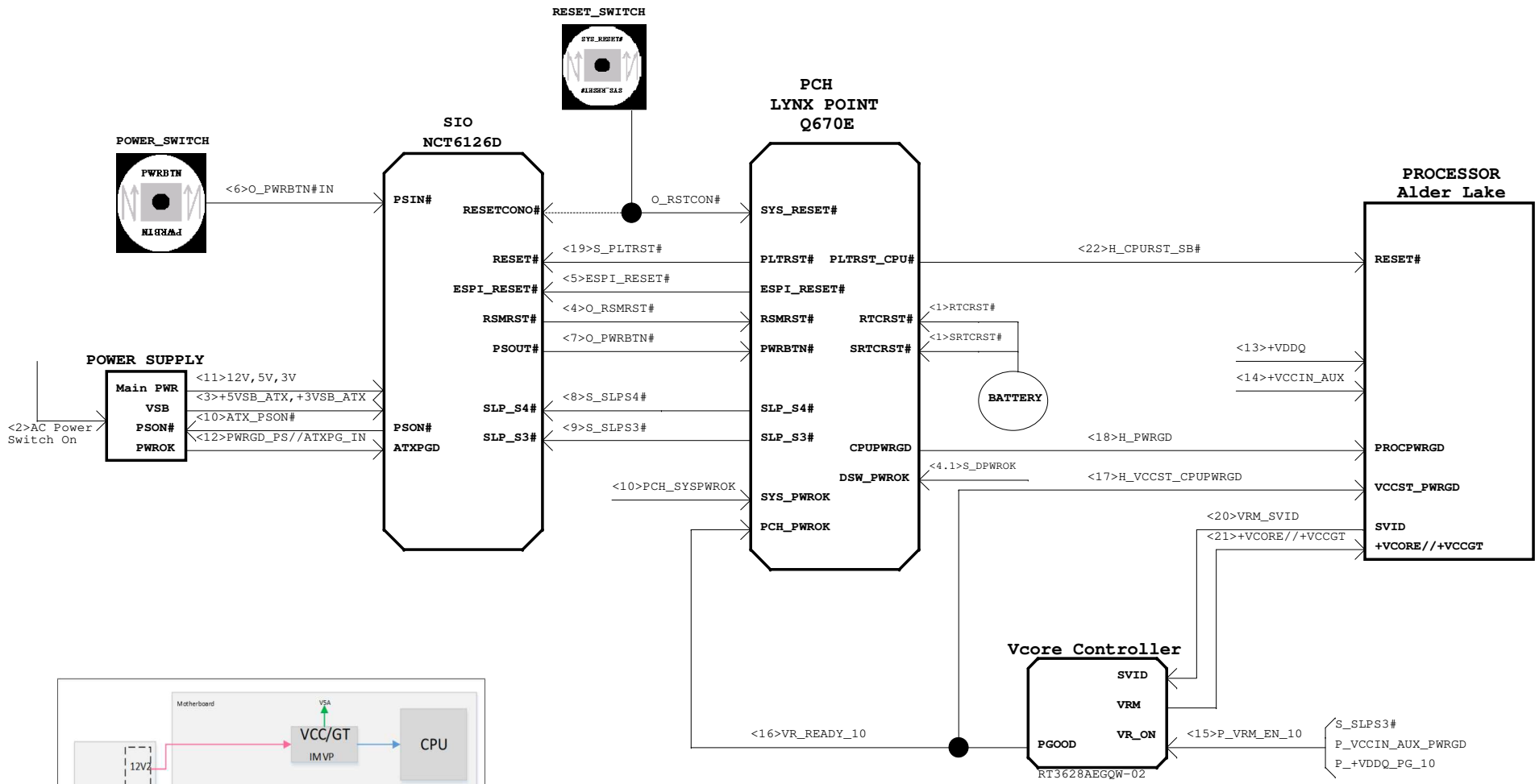
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: IPC-EE2

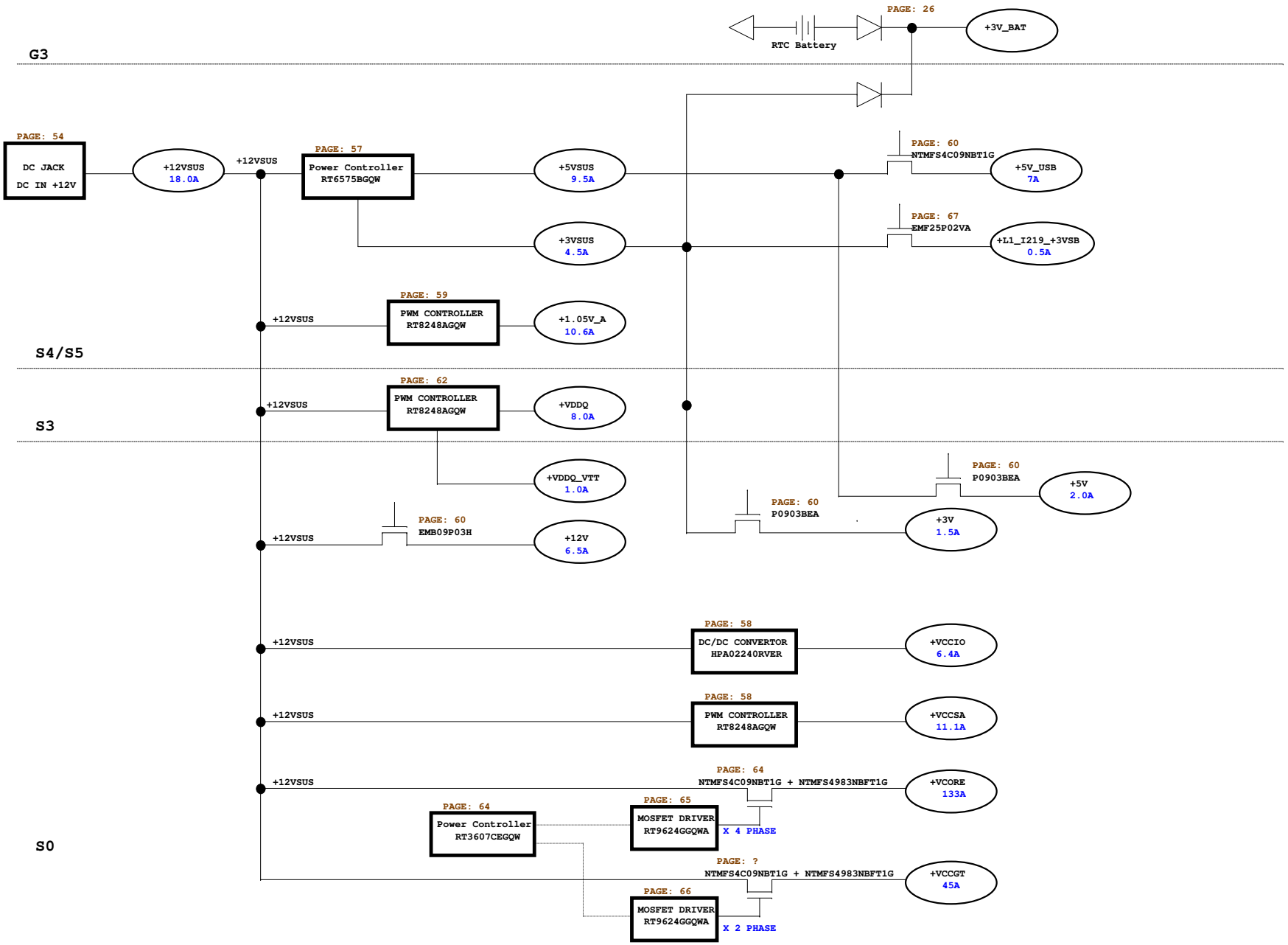
Size	Project Name	Rev
A3	MIX-Q670D1	R1.00

Date: Tuesday, August 23, 2022 Sheet 2 of 70



<Variant Name>

ASUSTek COMPUTER INC.	Title : Signal & Reset map	
	Engineer: IPC-EE2	
Size A3	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 3 of 70	



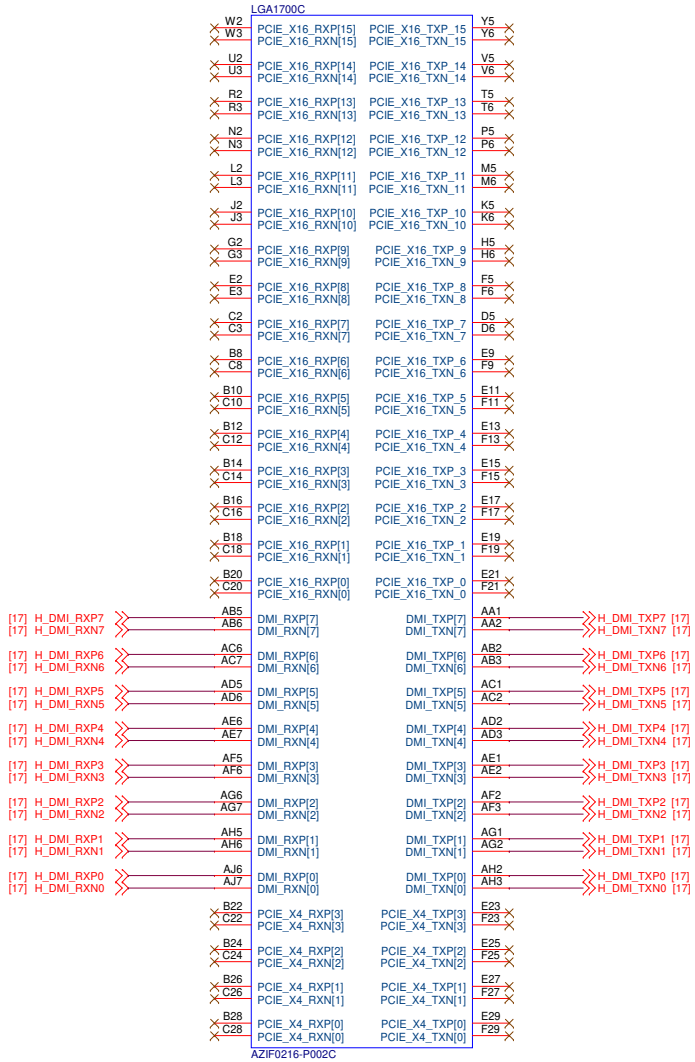
ASUSTeK COMPUTER INC.

Title : Power Flow

Engineer: IPC-EE2

Size	Project Name	Rev
Custom	MIX-Q670D1	R1.00

Date: Tuesday, August 23, 2022 Sheet 4 of 70



LOTES/AZIF0216-P002C

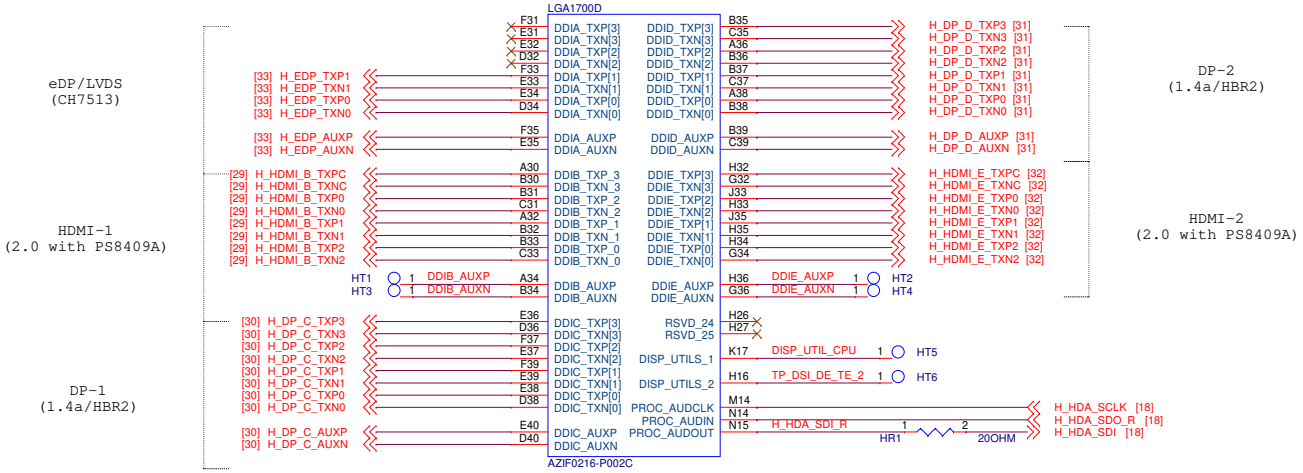
12001-00300200

LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ASUS	Title : LGA1700 (DMI/PCIE)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size A3	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 5 of 70		



12001-00300200

LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ASUS	Title: LGA1700 (DISPLAY)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size: A3	Project Name: MIX-Q670D1		Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 6 of 70		

Channel 0/1
6 Layer routing

DDR4 (IL) / DDR4 (NIL) / DDR5 DDR4 / DDR5

LGA1700A

[13] D5_DDR1_DQ3[0:7]	D5_DDR1_DQ34	AM2	DDR0_DQ7[7]/DDR1_DQ5[7]	/DDR1_DQ3[7]	
	D5_DDR1_DQ35	AL2	DDR0_DQ7[6]/DDR1_DQ5[6]	/DDR1_DQ3[6]	
	D5_DDR1_DQ36	AL3	DDR0_DQ7[5]/DDR1_DQ5[5]	/DDR1_DQ3[5]	
	D5_DDR1_DQ37	AL4	DDR0_DQ7[4]/DDR1_DQ5[4]	/DDR1_DQ3[4]	
	D5_DDR1_DQ32	AP2	DDR0_DQ7[3]/DDR1_DQ5[3]	/DDR1_DQ3[3]	
	D5_DDR1_DQ31	AN2	DDR0_DQ7[2]/DDR1_DQ5[2]	/DDR1_DQ3[2]	
	D5_DDR1_DQ33	AP4	DDR0_DQ7[1]/DDR1_DQ5[1]	/DDR1_DQ3[1]	
[13] D5_DDR1_DQ2[0:7]	D5_DDR1_DQ30	AP3	DDR0_DQ7[0]/DDR1_DQ5[0]	/DDR1_DQ3[0]	
	D5_DDR1_DQ24	AU2	DDR0_DQ6[7]/DDR1_DQ4[7]	/DDR1_DQ2[7]	
	D5_DDR1_DQ26	AT2	DDR0_DQ6[6]/DDR1_DQ4[6]	/DDR1_DQ2[6]	
	D5_DDR1_DQ25	AT4	DDR0_DQ6[5]/DDR1_DQ4[5]	/DDR1_DQ2[5]	
	D5_DDR1_DQ27	AT3	DDR0_DQ6[4]/DDR1_DQ4[4]	/DDR1_DQ2[4]	
	D5_DDR1_DQ23	AW2	DDR0_DQ6[3]/DDR1_DQ4[3]	/DDR1_DQ2[3]	
	D5_DDR1_DQ21	AV2	DDR0_DQ6[2]/DDR1_DQ4[2]	/DDR1_DQ2[2]	
	D5_DDR1_DQ20	AW4	DDR0_DQ6[1]/DDR1_DQ4[1]	/DDR1_DQ2[1]	
	D5_DDR1_DQ22	AW3	DDR0_DQ6[0]/DDR1_DQ4[0]	/DDR1_DQ2[0]	
[13] D5_DDR1_DQ1[0:7]	D5_DDR1_DQ14	BA2	DDR0_DQ5[7]/DDR1_DQ1[7]	/DDR1_DQ1[7]	
	D5_DDR1_DQ16	BA1	DDR0_DQ5[6]/DDR1_DQ1[6]	/DDR1_DQ1[6]	
	D5_DDR1_DQ17	BA3	DDR0_DQ5[5]/DDR1_DQ1[5]	/DDR1_DQ1[5]	
	D5_DDR1_DQ15	BB2	DDR0_DQ5[4]/DDR1_DQ1[4]	/DDR1_DQ1[4]	
	D5_DDR1_DQ13	BC4	DDR0_DQ5[3]/DDR1_DQ1[3]	/DDR1_DQ1[3]	
	D5_DDR1_DQ11	BB5	DDR0_DQ5[2]/DDR1_DQ1[2]	/DDR1_DQ1[2]	
	D5_DDR1_DQ12	BD4	DDR0_DQ5[1]/DDR1_DQ1[1]	/DDR1_DQ1[1]	
	D5_DDR1_DQ10	BC5	DDR0_DQ5[0]/DDR1_DQ1[0]	/DDR1_DQ1[0]	
[13] D5_DDR1_DQ0[0:7]	D5_DDR1_DQ05	BA7	DDR0_DQ4[7]/DDR1_DQ0[7]	/DDR1_DQ0[7]	
	D5_DDR1_DQ06	BC7	DDR0_DQ4[6]/DDR1_DQ0[6]	/DDR1_DQ0[6]	
	D5_DDR1_DQ04	BC8	DDR0_DQ4[5]/DDR1_DQ0[5]	/DDR1_DQ0[5]	
	D5_DDR1_DQ07	BB7	DDR0_DQ4[4]/DDR1_DQ0[4]	/DDR1_DQ0[4]	
	D5_DDR1_DQ02	BB10	DDR0_DQ4[3]/DDR1_DQ0[3]	/DDR1_DQ0[3]	
	D5_DDR1_DQ00	BA10	DDR0_DQ4[2]/DDR1_DQ0[2]	/DDR1_DQ0[2]	
	D5_DDR1_DQ03	BC10	DDR0_DQ4[1]/DDR1_DQ0[1]	/DDR1_DQ0[1]	
	D5_DDR1_DQ01	BC9	DDR0_DQ4[0]/DDR1_DQ0[0]	/DDR1_DQ0[0]	
[13] D5_DDR0_DQ3[0:7]	D5_DDR0_DQ37	BC45	DDR0_DQ3[7]/DDR0_DQ5[7]	/DDR0_DQ3[7]	
	D5_DDR0_DQ35	BC44	DDR0_DQ3[6]/DDR0_DQ5[6]	/DDR0_DQ3[6]	
	D5_DDR0_DQ36	BA44	DDR0_DQ3[5]/DDR0_DQ5[5]	/DDR0_DQ3[5]	
	D5_DDR0_DQ34	BB44	DDR0_DQ3[4]/DDR0_DQ5[4]	/DDR0_DQ3[4]	
	D5_DDR0_DQ32	BC47	DDR0_DQ3[3]/DDR0_DQ5[3]	/DDR0_DQ3[3]	
	D5_DDR0_DQ31	BC46	DDR0_DQ3[2]/DDR0_DQ5[2]	/DDR0_DQ3[2]	
	D5_DDR0_DQ33	BB47	DDR0_DQ3[1]/DDR0_DQ5[1]	/DDR0_DQ3[1]	
	D5_DDR0_DQ30	BA47	DDR0_DQ3[0]/DDR0_DQ5[0]	/DDR0_DQ3[0]	
[13] D5_DDR0_DQ2[0:7]	D5_DDR0_DQ25	BC49	DDR0_DQ2[7]/DDR0_DQ4[7]	/DDR0_DQ2[7]	
	D5_DDR0_DQ27	BD49	DDR0_DQ2[6]/DDR0_DQ4[6]	/DDR0_DQ2[6]	
	D5_DDR0_DQ24	BC50	DDR0_DQ2[5]/DDR0_DQ4[5]	/DDR0_DQ2[5]	
	D5_DDR0_DQ26	BB49	DDR0_DQ2[4]/DDR0_DQ4[4]	/DDR0_DQ2[4]	
	D5_DDR0_DQ22	BA52	DDR0_DQ2[3]/DDR0_DQ4[3]	/DDR0_DQ2[3]	
	D5_DDR0_DQ21	BA51	DDR0_DQ2[2]/DDR0_DQ4[2]	/DDR0_DQ2[2]	
	D5_DDR0_DQ20	AY51	DDR0_DQ2[1]/DDR0_DQ4[1]	/DDR0_DQ2[1]	
	D5_DDR0_DQ23	AY50	DDR0_DQ2[0]/DDR0_DQ4[0]	/DDR0_DQ2[0]	
[13] D5_DDR0_DQ1[0:7]	D5_DDR0_DQ15	AV50	DDR0_DQ1[7]/DDR0_DQ1[7]	/DDR0_DQ1[7]	
	D5_DDR0_DQ17	AV49	DDR0_DQ1[6]/DDR0_DQ1[6]	/DDR0_DQ1[6]	
	D5_DDR0_DQ14	AU51	DDR0_DQ1[5]/DDR0_DQ1[5]	/DDR0_DQ1[5]	
	D5_DDR0_DQ16	AV51	DDR0_DQ1[4]/DDR0_DQ1[4]	/DDR0_DQ1[4]	
	D5_DDR0_DQ12	AR50	DDR0_DQ1[3]/DDR0_DQ1[3]	/DDR0_DQ1[3]	
	D5_DDR0_DQ13	AR49	DDR0_DQ1[2]/DDR0_DQ1[2]	/DDR0_DQ1[2]	
	D5_DDR0_DQ10	AR51	DDR0_DQ1[1]/DDR0_DQ1[1]	/DDR0_DQ1[1]	
	D5_DDR0_DQ11	AT51	DDR0_DQ1[0]/DDR0_DQ1[0]	/DDR0_DQ1[0]	
[13] D5_DDR0_DQ0[0:7]	D5_DDR0_DQ06	AN50	DDR0_DQ0[7]/DDR0_DQ0[7]	/DDR0_DQ0[7]	
	D5_DDR0_DQ04	AN49	DDR0_DQ0[6]/DDR0_DQ0[6]	/DDR0_DQ0[6]	
	D5_DDR0_DQ05	AM51	DDR0_DQ0[5]/DDR0_DQ0[5]	/DDR0_DQ0[5]	
	D5_DDR0_DQ07	AN51	DDR0_DQ0[4]/DDR0_DQ0[4]	/DDR0_DQ0[4]	
	D5_DDR0_DQ00	AK50	DDR0_DQ0[3]/DDR0_DQ0[3]	/DDR0_DQ0[3]	
	D5_DDR0_DQ02	AK49	DDR0_DQ0[2]/DDR0_DQ0[2]	/DDR0_DQ0[2]	
	D5_DDR0_DQ01	AK51	DDR0_DQ0[1]/DDR0_DQ0[1]	/DDR0_DQ0[1]	
	D5_DDR0_DQ03	AL51	DDR0_DQ0[0]/DDR0_DQ0[0]	/DDR0_DQ0[0]	

BC40	DDR0_DQ8[7]/DDR0_DQ8[7]/NC		
BC39	DDR0_DQ8[6]/DDR0_DQ8[6]/NC		
BA39	DDR0_DQ8[5]/DDR0_DQ8[5]/NC		
BB39	DDR0_DQ8[4]/DDR0_DQ8[4]/NC		
BC42	DDR0_DQ8[3]/DDR0_DQ8[3]	/DDR0_DQ4[3]	DDR0_DQSP8/ DDR0_DQSP4
BC41	DDR0_DQ8[2]/DDR0_DQ8[2]	/DDR0_DQ4[2]	DDR0_DQSN8/ DDR0_DQSN4
BA42	DDR0_DQ8[1]/DDR0_DQ8[1]	/DDR0_DQ4[1]	
BB42	DDR0_DQ8[0]/DDR0_DQ8[0]	/DDR0_DQ4[0]	
BA13	NC/NC/DDR1_DQ4[3]		
BA12	NC/NC/DDR1_DQ4[2]		
BC12	NC/NC/DDR1_DQ4[1]		
BB12	NC/NC/DDR1_DQ4[0]		
AH50	DDR_VREF_CA1		
AH52	DDR_VREF_CA0		

	DDR0_CLKP3/DDR1_CLKP0	BC22	D5_DDR1_CLK0 [13]
	DDR0_CLKN3/DDR1_CLKN0	BB22	D5_DDR1_CLK#0 [13]
	DDR0_CLKP2/DDR1_CLKP1	BD23	D5_DDR1_CLK1 [13]
	DDR0_CLKN2/DDR1_CLKN1	BC23	D5_DDR1_CLK#1 [13]
	DDR0_CLKP1/DDR0_CLKP1	BC28	D5_DDR0_CLK1 [13]
	DDR0_CLKN1/DDR0_CLKN1	BB28	D5_DDR0_CLK#1 [13]
	DDR0_CLKP0/DDR0_CLKP0	BD29	D5_DDR0_CLK0 [13]
	DDR0_CLKN0/DDR0_CLKN0	BC29	D5_DDR0_CLK#0 [13]
	DDR0_CKE3/NC	BD37	
	DDR0_CKE2/DDR0_CS1	BB36	D5_DDR0_CS#1 [13]
	DDR0_CKE1/DDR0_CS3	BA37	
	DDR0_CKE0/DDR0_CS0	BC36	D5_DDR0_CS#0 [13]
	DDR0_CS3/DDR1_CS0	BD15	D5_DDR1_CS#0 [13]
	DDR0_CS2/DDR1_CA5	BB18	D5_DDR1_CA5 [13]
	DDR0_CS1/DDR1_CA0	BB16	D5_DDR1_CA0 [13]
	DDR0_CS0/DDR1_CA6	BC18	D5_DDR1_CA6 [13]
	DDR0_ODT3/NC	BB14	
	DDR0_ODT2/DDR1_CA1	BC16	D5_DDR1_CA1 [13]
	DDR0_ODT1/DDR1_CS1	BA16	D5_DDR1_CS#1 [13]
	DDR0_ODT0/DDR1_CA3	BD17	D5_DDR1_CA3 [13]
	DDR0_BA1/DDR1_CA11	BC20	D5_DDR1_CA11 [13]
	DDR0_BA0/DDR1_CA9	BA20	D5_DDR1_CA9 [13]
	DDR0_BG1/DDR0_CA2	BC35	D5_DDR0_CA2 [13]
	DDR0_BG0/DDR0_CA1	BD35	D5_DDR0_CA1 [13]
	DDR0_MA16/DDR1_CA8	BD19	D5_DDR1_CA8 [13]
	DDR0_MA15/DDR1_CA4	BA18	D5_DDR1_CA4 [13]
	DDR0_MA14/DDR1_CA7	BC19	D5_DDR1_CA7 [13]
	DDR0_MA13/DDR1_CA2	BC17	D5_DDR1_CA2 [13]
	DDR0_MA12/DDR0_CA3	BC34	D5_DDR0_CA3 [13]
	DDR0_MA11/DDR0_CA5	BA33	D5_DDR0_CA5 [13]
	DDR0_MA10/DDR1_CA10	BB20	D5_DDR1_CA10 [13]
	DDR0_MA9/DDR0_CA4	BB34	D5_DDR0_CA4 [13]
	DDR0_MA8/DDR0_CA7	BC33	D5_DDR0_CA7 [13]
	DDR0_MA7/DDR0_CA6	BD33	D5_DDR0_CA6 [13]
	DDR0_MA6/DDR0_CA8	BC32	D5_DDR0_CA8 [13]
	DDR0_MA5/DDR0_CA9	BB32	D5_DDR0_CA9 [13]
	DDR0_MA4/DDR0_CA10	BA31	D5_DDR0_CA10 [13]
	DDR0_MA3/DDR0_CA11	BD31	D5_DDR0_CA11 [13]
	DDR0_MA2/NC	BC30	
	DDR0_MA1/DDR0_CA12	BC31	D5_DDR0_CA12 [13]
	DDR0_MA0/DDR1_CA12	BC21	D5_DDR1_CA12 [13]
	DDR0_ACT#/DDR0_CA0	BA35	
	DDR0_PAR/NC	BD21	D5_DDR0_CA0 [13]
	DDR0_ALERT#	AP25	DDR0_ALERT# [13]
	DDR4 (IL) / DDR4 (NIL) / DDR5	AM4	
DDR0_DQSP7/	DDR1_DQSP5/DDR1_DQSP3	AN4	D5_DDR1_DQS3 [13]
DDR0_DQSN7/	DDR1_DQSN5/DDR1_DQSN3	AU4	D5_DDR1_DQS#3 [13]
DDR0_DQSP6/	DDR1_DQSP4/DDR1_DQSP2	AV4	D5_DDR1_DQS2 [13]
DDR0_DQSN6/	DDR1_DQSN4/DDR1_DQSN2	BA4	D5_DDR1_DQS#2 [13]
DDR0_DQSP5/	DDR1_DQSP1/DDR1_DQSP1	BA5	D5_DDR1_DQS1 [13]
DDR0_DQSN5/	DDR1_DQSN1/DDR1_DQSN1	BA8	D5_DDR1_DQS#1 [13]
DDR0_DQSP4/	DDR1_DQSP0/DDR1_DQSP0	BA9	D5_DDR1_DQS0 [13]
DDR0_DQSN4/	DDR1_DQSN0/DDR1_DQSN0	BA45	D5_DDR1_DQS#0 [13]
DDR0_DQSP3/	DDR0_DQSP5/DDR0_DQSP3	BA46	D5_DDR0_DQS3 [13]
DDR0_DQSN3/	DDR0_DQSN5/DDR0_DQSN3	BA49	D5_DDR0_DQS#3 [13]
DDR0_DQSP2/	DDR0_DQSP4/DDR0_DQSP2	AY49	D5_DDR0_DQS2 [13]
DDR0_DQSN2/	DDR0_DQSN4/DDR0_DQSN2	AU49	D5_DDR0_DQS#2 [13]
DDR0_DQSP1/	DDR0_DQSP1/DDR0_DQSP1	AT49	D5_DDR0_DQS1 [13]
DDR0_DQSN1/	DDR0_DQSN1/DDR0_DQSN1	AM49	D5_DDR0_DQS#1 [13]
DDR0_DQSP0/	DDR0_DQSP0/DDR0_DQSP0	AL49	D5_DDR0_DQS0 [13]
DDR0_DQSN0/	DDR0_DQSN0/DDR0_DQSN0		D5_DDR0_DQS#0 [13]
		BA40	
DDR0_DQSP8/	DDR0_DQSP8/DDR0_DQSP4	BA41	
DDR0_DQSN8/	DDR0_DQSN8/DDR0_DQSN4		
	NC/NC/DDR1_DQSP4	BC13	
	NC/NC/DDR1_DQSN4	BD13	
	NC/DDR3_CS3	AU20	
	NC/DDR3_CS2	AV20	
	NC/DDR2_CS2	AW33	
	NC/DDR1_CS3	BA15	
	NC/DDR1_CS2	BC15	
	NC/DDR0_CS2	BC37	

NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8
1 2 3 4 5 6 7 8

AZIF0216-P002C
LOTES/AZIF0216-P002C
12001-00300200

LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300200 LOTES/AZIF0216-P002C
2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ASUS	Title: LGA1700 (DDR5_CH 0/1)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE2	
Size: A3	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 7 of 70	

Channel 2/3
6 Layer routing

DDR4(IL) / DDR4(NIL) / DDR5 DDR4 / DDR5

LGA1700B

[14] D5_DDR3_DQ3[0:7]	D5_DDR3_DQ36	AL7	DDR1_DQ7[7]/DDR1_DQ7[7]	/DDR3_DQ3[7]			
	D5_DDR3_DQ34	AM6	DDR1_DQ7[6]/DDR1_DQ7[6]	/DDR3_DQ3[6]			
	D5_DDR3_DQ37	AL6	DDR1_DQ7[5]/DDR1_DQ7[5]	/DDR3_DQ3[5]			
	D5_DDR3_DQ35	AL8	DDR1_DQ7[4]/DDR1_DQ7[4]	/DDR3_DQ3[4]			
	D5_DDR3_DQ32	AP6	DDR1_DQ7[3]/DDR1_DQ7[3]	/DDR3_DQ3[3]			
	D5_DDR3_DQ30	AN6	DDR1_DQ7[2]/DDR1_DQ7[2]	/DDR3_DQ3[2]			
	D5_DDR3_DQ33	AP7	DDR1_DQ7[1]/DDR1_DQ7[1]	/DDR3_DQ3[1]			
	D5_DDR3_DQ31	AP8	DDR1_DQ7[0]/DDR1_DQ7[0]	/DDR3_DQ3[0]			
[14] D5_DDR3_DQ2[0:7]	D5_DDR3_DQ24	AT7	DDR1_DQ6[7]/DDR1_DQ6[7]	/DDR3_DQ2[7]			
	D5_DDR3_DQ25	AT6	DDR1_DQ6[6]/DDR1_DQ6[6]	/DDR3_DQ2[6]			
	D5_DDR3_DQ26	AV6	DDR1_DQ6[5]/DDR1_DQ6[5]	/DDR3_DQ2[5]			
	D5_DDR3_DQ27	AU6	DDR1_DQ6[4]/DDR1_DQ6[4]	/DDR3_DQ2[4]			
	D5_DDR3_DQ20	AW6	DDR1_DQ6[3]/DDR1_DQ6[3]	/DDR3_DQ2[3]			
	D5_DDR3_DQ23	AV8	DDR1_DQ6[2]/DDR1_DQ6[2]	/DDR3_DQ2[2]			
	D5_DDR3_DQ21	AW8	DDR1_DQ6[1]/DDR1_DQ6[1]	/DDR3_DQ2[1]			
	D5_DDR3_DQ22	AW7	DDR1_DQ6[0]/DDR1_DQ6[0]	/DDR3_DQ2[0]			
[14] D5_DDR3_DQ1[0:7]	D5_DDR3_DQ14	AW10	DDR1_DQ5[7]/DDR1_DQ3[7]	/DDR3_DQ1[7]			
	D5_DDR3_DQ17	AV10	DDR1_DQ5[6]/DDR1_DQ3[6]	/DDR3_DQ1[6]			
	D5_DDR3_DQ16	AW11	DDR1_DQ5[5]/DDR1_DQ3[5]	/DDR3_DQ1[5]			
	D5_DDR3_DQ15	AU10	DDR1_DQ5[4]/DDR1_DQ3[4]	/DDR3_DQ1[4]			
	D5_DDR3_DQ13	AT12	DDR1_DQ5[3]/DDR1_DQ3[3]	/DDR3_DQ1[3]			
	D5_DDR3_DQ11	AU12	DDR1_DQ5[2]/DDR1_DQ3[2]	/DDR3_DQ1[2]			
	D5_DDR3_DQ10	AW12	DDR1_DQ5[1]/DDR1_DQ3[1]	/DDR3_DQ1[1]			
	D5_DDR3_DQ12	AV12	DDR1_DQ5[0]/DDR1_DQ3[0]	/DDR3_DQ1[0]			
[14] D5_DDR3_DQ0[0:7]	D5_DDR3_DQ05	AT14	DDR1_DQ4[7]/DDR1_DQ2[7]	/DDR3_DQ0[7]			
	D5_DDR3_DQ06	AU14	DDR1_DQ4[6]/DDR1_DQ2[6]	/DDR3_DQ0[6]			
	D5_DDR3_DQ04	AW14	DDR1_DQ4[5]/DDR1_DQ2[5]	/DDR3_DQ0[5]			
	D5_DDR3_DQ07	AV14	DDR1_DQ4[4]/DDR1_DQ2[4]	/DDR3_DQ0[4]			
	D5_DDR3_DQ00	AW15	DDR1_DQ4[3]/DDR1_DQ2[3]	/DDR3_DQ0[3]			
	D5_DDR3_DQ01	AU16	DDR1_DQ4[2]/DDR1_DQ2[2]	/DDR3_DQ0[2]			
	D5_DDR3_DQ03	AW16	DDR1_DQ4[1]/DDR1_DQ2[1]	/DDR3_DQ0[1]			
	D5_DDR3_DQ02	AV16	DDR1_DQ4[0]/DDR1_DQ2[0]	/DDR3_DQ0[0]			
[14] D5_DDR2_DQ3[0:7]	D5_DDR2_DQ34	AW40	DDR1_DQ3[7]/DDR0_DQ7[7]	/DDR2_DQ3[7]			
	D5_DDR2_DQ35	AW39	DDR1_DQ3[6]/DDR0_DQ7[6]	/DDR2_DQ3[6]			
	D5_DDR2_DQ37	AU39	DDR1_DQ3[5]/DDR0_DQ7[5]	/DDR2_DQ3[5]			
	D5_DDR2_DQ36	AV39	DDR1_DQ3[4]/DDR0_DQ7[4]	/DDR2_DQ3[4]			
	D5_DDR2_DQ30	AW42	DDR1_DQ3[3]/DDR0_DQ7[3]	/DDR2_DQ3[3]			
	D5_DDR2_DQ33	AW41	DDR1_DQ3[2]/DDR0_DQ7[2]	/DDR2_DQ3[2]			
	D5_DDR2_DQ31	AV42	DDR1_DQ3[1]/DDR0_DQ7[1]	/DDR2_DQ3[1]			
	D5_DDR2_DQ32	AU42	DDR1_DQ3[0]/DDR0_DQ7[0]	/DDR2_DQ3[0]			
[14] D5_DDR2_DQ2[0:7]	D5_DDR2_DQ24	AW45	DDR1_DQ2[7]/DDR0_DQ6[7]	/DDR2_DQ2[7]			
	D5_DDR2_DQ27	AW44	DDR1_DQ2[6]/DDR0_DQ6[6]	/DDR2_DQ2[6]			
	D5_DDR2_DQ26	AV44	DDR1_DQ2[5]/DDR0_DQ6[5]	/DDR2_DQ2[5]			
	D5_DDR2_DQ22	AW46	DDR1_DQ2[4]/DDR0_DQ6[4]	/DDR2_DQ2[4]			
	D5_DDR2_DQ20	AW47	DDR1_DQ2[3]/DDR0_DQ6[3]	/DDR2_DQ2[3]			
	D5_DDR2_DQ25	AU44	DDR1_DQ2[2]/DDR0_DQ6[2]	/DDR2_DQ2[2]			
	D5_DDR2_DQ21	AU47	DDR1_DQ2[1]/DDR0_DQ6[1]	/DDR2_DQ2[1]			
	D5_DDR2_DQ23	AV47	DDR1_DQ2[0]/DDR0_DQ6[0]	/DDR2_DQ2[0]			
[14] D5_DDR2_DQ1[0:7]	D5_DDR2_DQ15	AR45	DDR1_DQ1[7]/DDR0_DQ3[7]	/DDR2_DQ1[7]			
	D5_DDR2_DQ17	AR44	DDR1_DQ1[6]/DDR0_DQ3[6]	/DDR2_DQ1[6]			
	D5_DDR2_DQ16	AR47	DDR1_DQ1[5]/DDR0_DQ3[5]	/DDR2_DQ1[5]			
	D5_DDR2_DQ14	AR46	DDR1_DQ1[4]/DDR0_DQ3[4]	/DDR2_DQ1[4]			
	D5_DDR2_DQ10	AN46	DDR1_DQ1[3]/DDR0_DQ3[3]	/DDR2_DQ1[3]			
	D5_DDR2_DQ11	AN45	DDR1_DQ1[2]/DDR0_DQ3[2]	/DDR2_DQ1[2]			
	D5_DDR2_DQ12	AN47	DDR1_DQ1[1]/DDR0_DQ3[1]	/DDR2_DQ1[1]			
	D5_DDR2_DQ13	AP47	DDR1_DQ1[0]/DDR0_DQ3[0]	/DDR2_DQ1[0]			
[14] D5_DDR2_DQ0[0:7]	D5_DDR2_DQ05	AL45	DDR1_DQ0[7]/DDR0_DQ2[7]	/DDR2_DQ0[7]			
	D5_DDR2_DQ07	AL46	DDR1_DQ0[6]/DDR0_DQ2[6]	/DDR2_DQ0[6]			
	D5_DDR2_DQ04	AK47	DDR1_DQ0[5]/DDR0_DQ2[5]	/DDR2_DQ0[5]			
	D5_DDR2_DQ06	AL47	DDR1_DQ0[4]/DDR0_DQ2[4]	/DDR2_DQ0[4]			
	D5_DDR2_DQ01	AH47	DDR1_DQ0[3]/DDR0_DQ2[3]	/DDR2_DQ0[3]			
	D5_DDR2_DQ00	AJ47	DDR1_DQ0[2]/DDR0_DQ2[2]	/DDR2_DQ0[2]			
	D5_DDR2_DQ03	AH45	DDR1_DQ0[1]/DDR0_DQ2[1]	/DDR2_DQ0[1]			
	D5_DDR2_DQ02	AH46	DDR1_DQ0[0]/DDR0_DQ2[0]	/DDR2_DQ0[0]			
		AU35					
		AV35	DDR1_DQ8[7]/DDR1_DQ8[7]/NC				
		AW36	DDR1_DQ8[6]/DDR1_DQ8[6]/NC				
		AW35	DDR1_DQ8[5]/DDR1_DQ8[5]/NC				
		AV37	DDR1_DQ8[4]/DDR1_DQ8[4]/NC				
		AW37	DDR1_DQ8[3]/DDR1_DQ8[3]	/DDR2_DQ4[3]	DDR1_DQSP8/	DDR1_DQSP8/DDR2_DQSP4	
		AU37	DDR1_DQ8[2]/DDR1_DQ8[2]	/DDR2_DQ4[2]	DDR1_DQSN8/	DDR1_DQSN8/DDR2_DQSN4	
		AT37	DDR1_DQ8[1]/DDR1_DQ8[1]	/DDR2_DQ4[1]			
			DDR1_DQ8[0]/DDR1_DQ8[0]	/DDR2_DQ4[0]		NC/NC/DDR3_DQSP4	AR18
						NC/NC/DDR3_DQSN4	AR19
		AV18					
		AU18	NC/NC/DDR3_DQ4[3]				
		AW18	NC/NC/DDR3_DQ4[2]			NC/DDR3_CLKP3	AP22
		AT18	NC/NC/DDR3_DQ4[1]			NC/DDR3_CLKN3	AP21
			NC/NC/DDR3_DQ4[0]			NC/DDR3_CLKP2	AR21
						NC/DDR3_CLKN2	AT21
		AH49				NC/DDR2_CLKP3	AP32
		AH51	DDR_VREF_CA3			NC/DDR2_CLKN3	AP33
			DDR_VREF_CA2			NC/DDR2_CLKP2	AR33
						NC/DDR2_CLKN2	AT33
						NC/DDR1_CLKP3	AP24
						NC/DDR1_CLKN3	AR24
						NC/DDR1_CLKP2	AR23
						NC/DDR1_CLKN2	AT23
						NC/DDR0_CLKP3	AP30
						NC/DDR0_CLKN3	AR30
						NC/DDR0_CLKP2	AR31
						NC/DDR0_CLKN2	AT31

DDR1_CLKP3/DDR3_CLKP1	BD25	D5_DDR3_CLK1	[14]
DDR1_CLKN3/DDR3_CLKN1	BC25	D5_DDR3_CLK#1	[14]
DDR1_CLKP2/DDR3_CLKP0	BC24	D5_DDR3_CLK0	[14]
DDR1_CLKN2/DDR3_CLKN0	BB24	D5_DDR3_CLK#0	[14]
DDR1_CLKP1/DDR2_CLKP1	BC26	D5_DDR2_CLK1	[14]
DDR1_CLKN1/DDR2_CLKN1	BB26	D5_DDR2_CLK#1	[14]
DDR1_CLKP0/DDR2_CLKP0	BD27	D5_DDR2_CLK0	[14]
DDR1_CLKN0/DDR2_CLKN0	BC27	D5_DDR2_CLK#0	[14]
DDR1_CKE3/NC	AV33		
	AT29		
DDR1_CKE2/DDR2_CS1	AU32	D5_DDR2_CS#1	[14]
DDR1_CKE1/DDR2_CS3	AV32		
DDR1_CKE0/DDR2_CS0		D5_DDR2_CS#0	[14]
	AW22		
DDR1_CS3/DDR3_CS0	AU24	D5_DDR3_CS#0	[14]
DDR1_CS2/DDR3_CA5	AU22	D5_DDR3_CA5	[14]
DDR1_CS1/DDR3_CA0	AV24	D5_DDR3_CA0	[14]
DDR1_CS0/DDR3_CA6		D5_DDR3_CA6	[14]
DDR1_ODT3/NC	AW20		
	AR26		
DDR1_ODT2/DDR3_CA1	AW21	D5_DDR3_CA1	[14]
DDR1_ODT1/DDR3_CS1	AW24	D5_DDR3_CS#1	[14]
DDR1_ODT0/DDR3_CA3		D5_DDR3_CA3	[14]
	AV26		
DDR1_BA1/DDR3_CA11	AW25	D5_DDR3_CA11	[14]
DDR1_BA0/DDR3_CA9		D5_DDR3_CA9	[14]
	AW31		
DDR1_BG1/DDR2_CA2	AW32	D5_DDR2_CA2	[14]
DDR1_BG0/DDR2_CA1		D5_DDR2_CA1	[14]
	AW26		
DDR1_MA16/DDR3_CA8	AW23	D5_DDR3_CA8	[14]
DDR1_MA15/DDR3_CA4	AT25	D5_DDR3_CA4	[14]
DDR1_MA14/DDR3_CA7	AU23	D5_DDR3_CA7	[14]
DDR1_MA13/DDR3_CA2	AU30	D5_DDR3_CA2	[14]
DDR1_MA12/DDR2_CA3	AU29	D5_DDR2_CA3	[14]
DDR1_MA11/DDR2_CA5	AU25	D5_DDR2_CA5	[14]
DDR1_MA10/DDR3_CA10	AV30	D5_DDR3_CA10	[14]
DDR1_MA9/DDR2_CA4	AW29	D5_DDR2_CA4	[14]
DDR1_MA8/DDR2_CA7	AW30	D5_DDR2_CA7	[14]
DDR1_MA7/DDR2_CA6	AV28	D5_DDR2_CA6	[14]
DDR1_MA6/DDR2_CA8	AU26	D5_DDR2_CA8	[14]
DDR1_MA5/DDR2_CA9	AU27	D5_DDR2_CA9	[14]
DDR1_MA4/DDR2_CA10	AW28	D5_DDR2_CA10	[14]
DDR1_MA3/DDR2_CA11	AT27	D5_DDR2_CA11	[14]
DDR1_MA2/NC	AW27		
DDR1_MA1/DDR2_CA12	AU26	D5_DDR2_CA12	[14]
DDR1_MA0/DDR3_CA12		D5_DDR3_CA12	[14]
	AU31		
DDR1_ACT#/DDR2_CA0	AR27	D5_DDR2_CA0	[14]
DDR1_PAR/NC	AP26		
DDR1_ALERT#		DDR1_ALERT#	[14]
DDR4(IL)/ DDR4(NIL)/ DDR5	AM8		
DDR1_DQSP7/ DDR1_DQSP7/DDR3_DQSP3	AN8	D5_DDR3_DQS3	[14]
DDR1_DQSN7/ DDR1_DQSN7/DDR3_DQSN3	AT8	D5_DDR3_DQS#3	[14]
DDR1_DQSP6/ DDR1_DQSP6/DDR3_DQSP2	AU8	D5_DDR3_DQS2	[14]
DDR1_DQSN6/ DDR1_DQSN6/DDR3_DQSN2	AT10	D5_DDR3_DQS#2	[14]
DDR1_DQSP5/ DDR1_DQSP3/DDR3_DQSP1	AT11	D5_DDR3_DQS1	[14]
DDR1_DQSN5/ DDR1_DQSN3/DDR3_DQSN1	AT15	D5_DDR3_DQS#1	[14]
DDR1_DQSP4/ DDR1_DQSP2/DDR3_DQSP0	AT16	D5_DDR3_DQS0	[14]
DDR1_DQSN4/ DDR1_DQSN2/DDR3_DQSN0	AU40	D5_DDR3_DQS#0	[14]
DDR1_DQSP3/ DDR0_DQSP7/DDR2_DQSP3	AU41	D5_DDR2_DQS3	[14]
DDR1_DQSN3/ DDR0_DQSN7/DDR2_DQSN3	AU45	D5_DDR2_DQS#3	[14]
DDR1_DQSP2/ DDR0_DQSP6/DDR2_DQSP2	AU46	D5_DDR2_DQS2	[14]
DDR1_DQSN2/ DDR0_DQSN6/DDR2_DQSN2	AP44	D5_DDR2_DQS#2	[14]
DDR1_DQSP1/ DDR0_DQSP3/DDR2_DQSP1	AN44	D5_DDR2_DQS1	[14]
DDR1_DQSN1/ DDR0_DQSN3/DDR2_DQSN1	AK45	D5_DDR2_DQS#1	[14]
DDR1_DQSP0/ DDR0_DQSP2/DDR2_DQSP0	AJ45	D5_DDR2_DQS0	[14]
DDR1_DQSN0/ DDR0_DQSN2/DDR2_DQSN0		D5_DDR2_DQS#0	[14]
	AT35		
	AT36		
	AR18		
	AR19		
	AP22		
NC/DDR3_CLKP3	AP21		
NC/DDR3_CLKN3	AR21		
NC/DDR3_CLKP2	AT21		
NC/DDR3_CLKN2	AP32		
NC/DDR2_CLKP3	AP33		
NC/DDR2_CLKN3	AR33		
NC/DDR2_CLKP2	AT33		
NC/DDR2_CLKN2	AP24		
NC/DDR1_CLKP3	AR24		
NC/DDR1_CLKN3	AR23		
NC/DDR1_CLKP2	AT23		
NC/DDR1_CLKN2	AP30		
NC/DDR0_CLKP3	AR30		
NC/DDR0_CLKN3	AR31		
NC/DDR0_CLKP2	AT31		
NC/DDR0_CLKN2			

AZIF0216-P002C
LOTES/AZIF0216-P002C
12001-00300200

LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300200 LOTES/AZIF0216-P002C
2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ASUS	Title: LGA1700 (DDR5_CH 2/3)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size A3	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 8 of 70		

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value (KΩ)
BPM#[3:0]	Pull Up/Pull Down	VCC_CFG_PU_OUT	1
PROC_PREQ#	Pull Up	VCC1p05_PROC	1
PROC_TDI	Pull Up	VCC1p05_PROC	1
PROC_TMS	Pull Up	VCC1p05_PROC	1
PROC_TRST#	Pull Down	VCC1p05_PROC	1
PROC_TCK	Pull Down	VCC1p05_PROC	1
CFG[17:0]	Pull Up	VCC_CFG_PU_OUT	1

CFG Straps for Processor (Use VCC_CFG_PU_OUT)

CFG[1:0] : Reserved Configuration Lanes
Reserved Configuration Lanes

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : Normal Operation
- 0 : Lane Numbers Reversed

CFG[4:3] : Reserved Configuration Lanes
Reserved Configuration Lane

CFG[5] : PCI Express* Bifurcation
- 0 : 2 x8 PCI Express*
- 1 : 1 x16 PCI Express* (default)

CFG[6] : Reserved Configuration Lanes
Pull -Up to VCC_CFG_PU_OUT
To ensure reliable boot across HVM.

CFG[8:7] : Reserved Configuration Lane
Reserved Configuration Lane

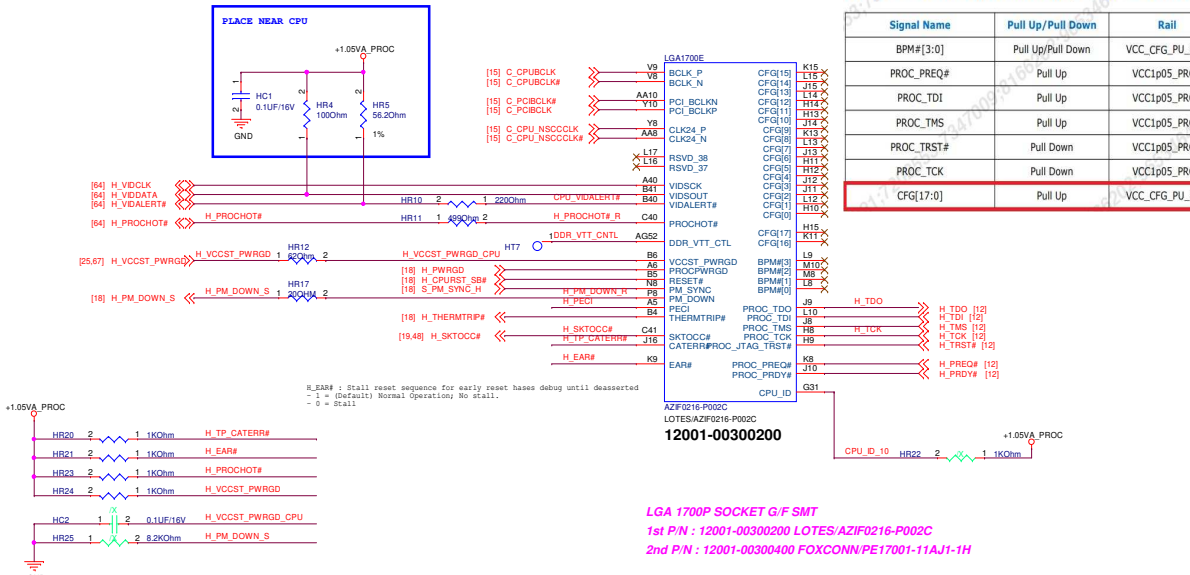
CFG[10:9] : Reserved Configuration Lanes
Pull -Up to VCC_CFG_PU_OUT
To ensure reliable boot across HVM.

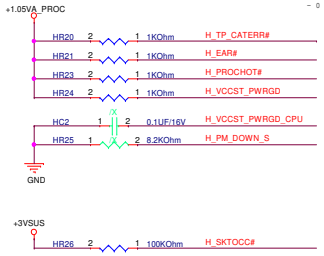
CFG[13:11] : Reserved Configuration Lanes
Reserved Configuration Lanes

CFG[14] : PCI Express* Static x4 Lane Numbering Reversal (PEG60)
- 1 : (Default) Normal
- 0 : Reversed

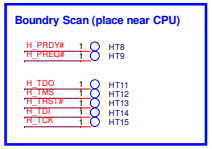
CFG[17:15] : Reserved Configuration Lanes

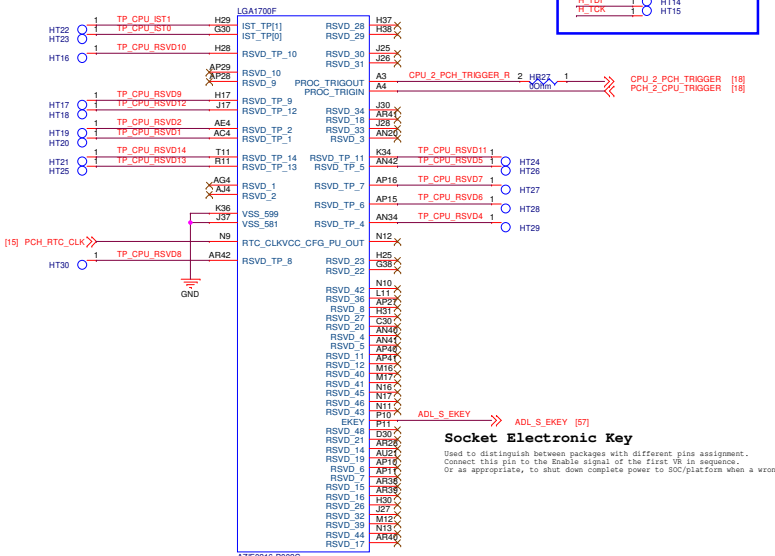
Refer : 619501-adl-processor-eds-vol1-rev2p3.pdf, P.171-172
619508_ADL_S_PDG_Rev2p2, p.319-320





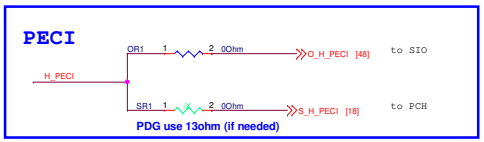
LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300200 LOTES/AZIF0216-P002C
2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H



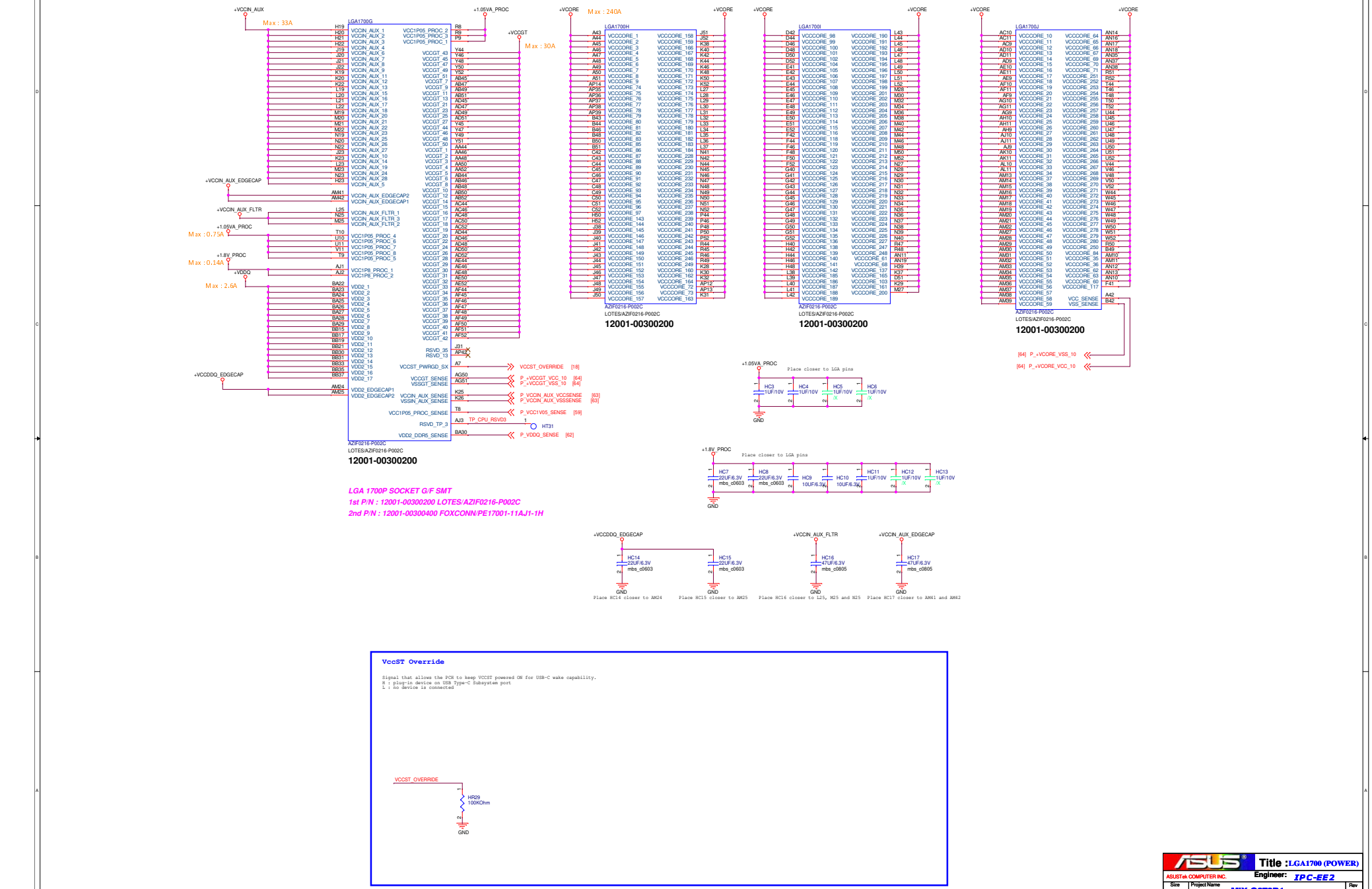


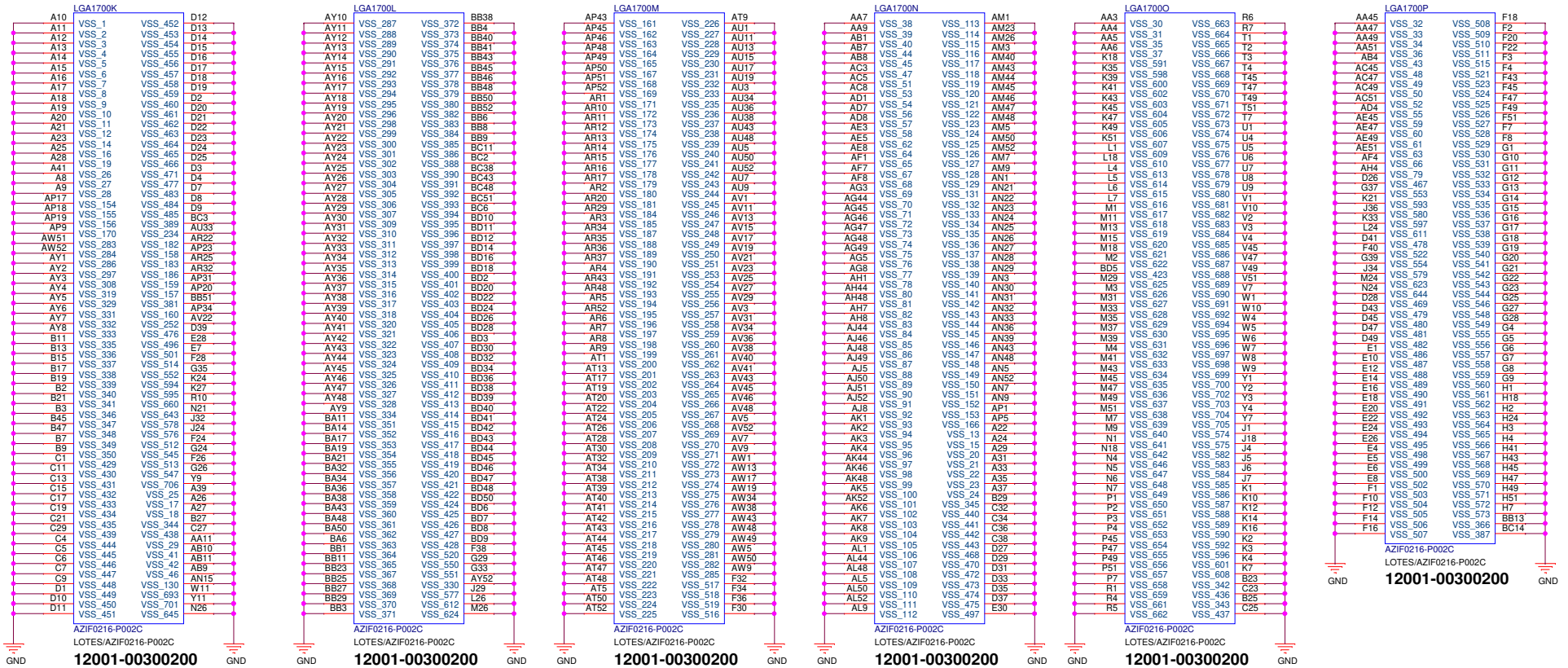
Socket Electronic Key

Used to distinguish between packages with different pins assignment.
Connect this pin to the Enable signal of the first VR in sequence.
Or as appropriate, to shut down complete power to SOC/platform when a wrong package is being used.



ASUSTek COMPUTER INC.	Title : LGA1700 (Control)	Engineer: IPC-EE2	
Size: C	Project Name: MIX-Q670D1		Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 9 of 70		


LGA1700G
LGA1700H
LGA1700I
LGA1700J
AZIF0216-P002C
LOTES/AZIF0216-P002C
12001-00300200
+VCCIN_AUX
Max : 33A
+1.05VA_PROC
+VCCGT
Max : 30A
+VCORE
Max : 240A
+VCCIN_AUX_EDGECAP
+VCCIN_AUX_FLTR
Max : 0.75A
+1.8V_PROC
Max : 0.14A
+VDDQ
Max : 2.6A
+VCCDDQ_EDGECAP
VCCST_OVERRIDE [18]
P_+VCCGT_VCC_10 [64]
P_+VCCGT_VSS_10 [64]
P_VCCIN_AUX_VCCSENSE [63]
P_VCCIN_AUX_VSSSENSE [63]
P_VCC1V05_SENSE [59]
TP_CPU_RSVD3
HT31
P_VDDQ_SENSE [62]
[64] P_+VCORE_VSS_10
[64] P_+VCORE_VCC_10
Place closer to LGA pins
HC3 1UF/10V
HC4 1UF/10V
HC5 1UF/10V
HC6 1UF/10V
HC7 22UF/6.3V mbs_c0603
HC8 22UF/6.3V mbs_c0603
HC9 10UF/6.3V
HC10 10UF/6.3V
HC11 1UF/10V
HC12 1UF/10V
HC13 1UF/10V
HC14 22UF/6.3V mbs_c0603
HC15 22UF/6.3V mbs_c0603
HC16 47UF/6.3V mbs_c0805
HC17 47UF/6.3V mbs_c0805
GND
Place HC14 closer to AM24
Place HC15 closer to AM25
Place HC16 closer to L25, M25 and N25
Place HC17 closer to AM41 and AM42
LGA 1700P SOCKET G/F SMT
1st P/N : 12001-00300200 LOTES/AZIF0216-P002C
2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H
VccST Override
Signal that allows the PCH to keep VCCST powered ON for USB-C wake capability.
H : plug-in device on USB Type-C Subsystem port
L : no device is connected
VCCST_OVERRIDE
HR29 100KOhm
GND
Title : LGA1700 (POWER)
ASUSTek COMPUTER INC.
Engineer: IPC-EE2
Size A2
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 10 of 70

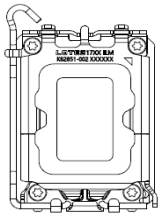


LGA 1700P SOCKET G/F SMT

1st P/N : 12001-00300200 LOTES/AZIF0216-P002C

2nd P/N : 12001-00300400 FOXCONN/PE17001-11AJ1-1H

ILM1



LGA1700_ILM_BP_COVER

[HF]LOTES/AZIF0239-P001C

13021-00020100

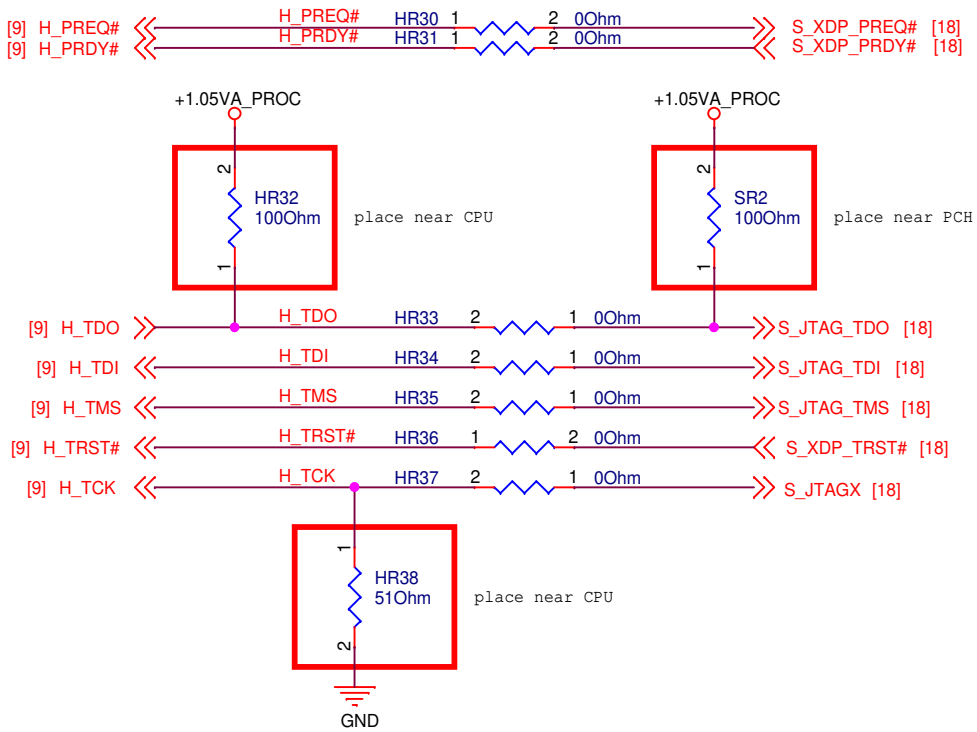
ILM+COVER+BACKPLATE Module-LGA1700

1st P/N : 13021-00020100 LOTES/AZIF0049-P001CC

2nd P/N : 13021-00020000 FOXCONN/PMVA161-11AJ1-4H

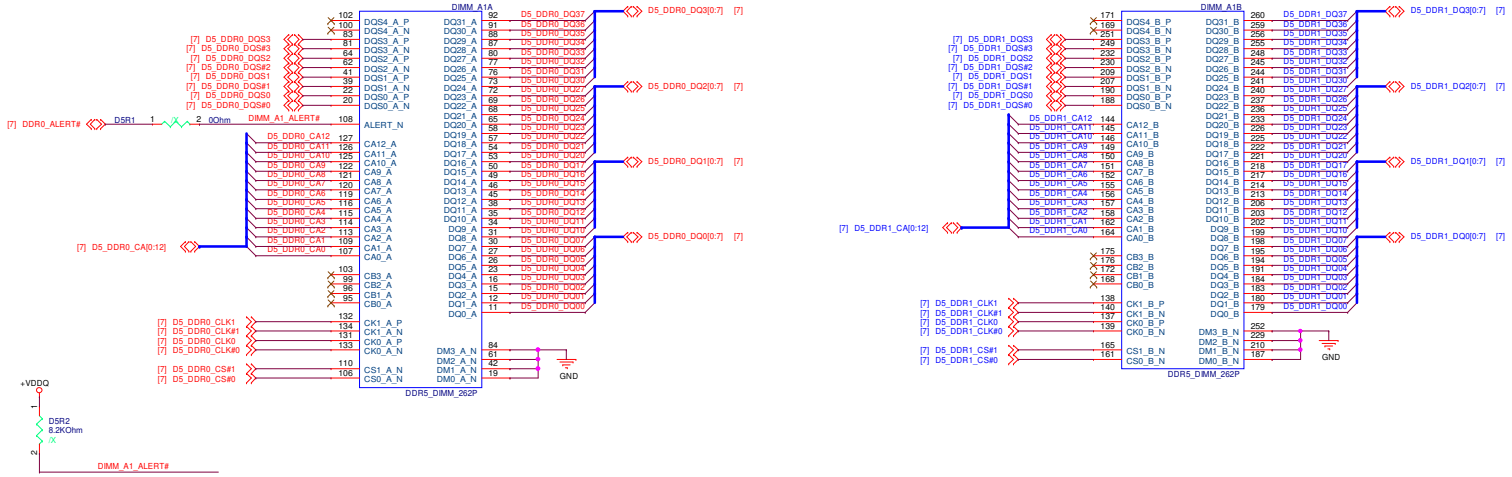
ASUSTek COMPUTER INC.	Title : LGA1700 (GND)	
	Engineer: IPC-EE2	
Size: A3	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 11 of 70	

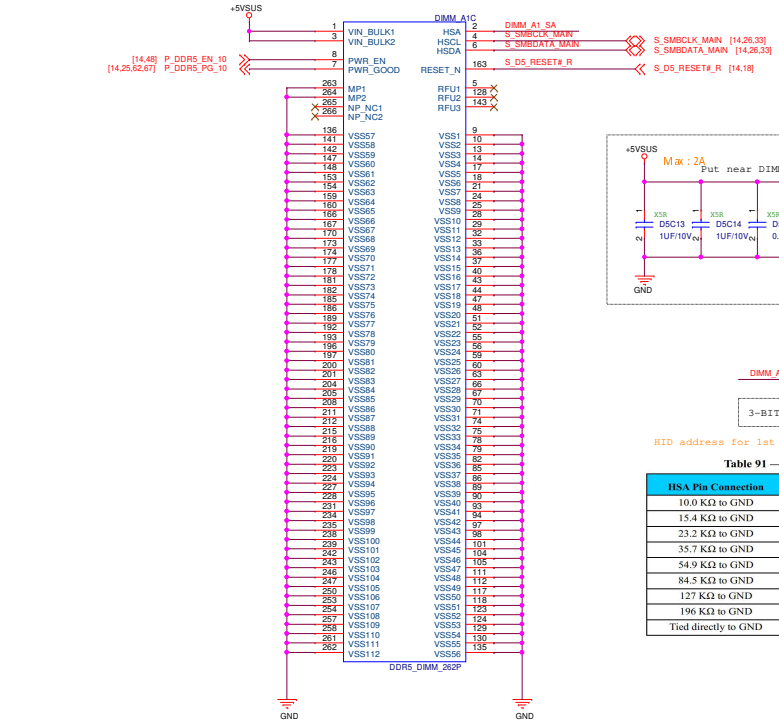
To PCH

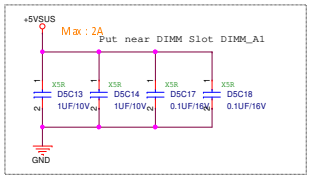


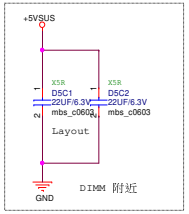
ASUS	Title : LGA1700 (XDP)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size A	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 12 of 70		

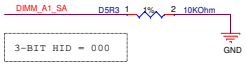
DDR5 SODIMM CHANNEL -A









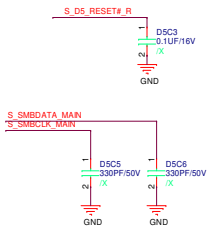


HID address for 1st DIMM is 000 and resistor value is 10K

Table 91 — HSA Pin Resistor Value and ID - SPD5 Family

HSA Pin Connection	3-bit HID	Comment
10.0 KΩ to GND	HID = 000	1% Resistor
15.4 KΩ to GND	HID = 001	
23.2 KΩ to GND	HID = 010	
35.7 KΩ to GND	HID = 011	
54.9 KΩ to GND	HID = 100	
84.5 KΩ to GND	HID = 101	
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

Put One Caps Per DIMM Slot



<Variant Name>

ASUSTeK COMPUTER INC.

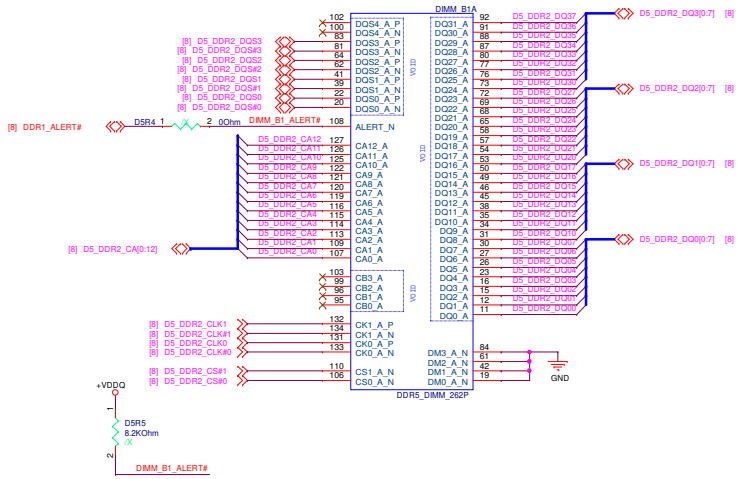
Title : DDR5 DIMM A1

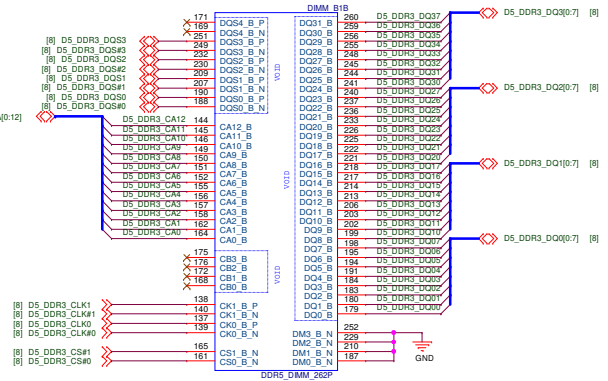
Engineer: IPC-EE2

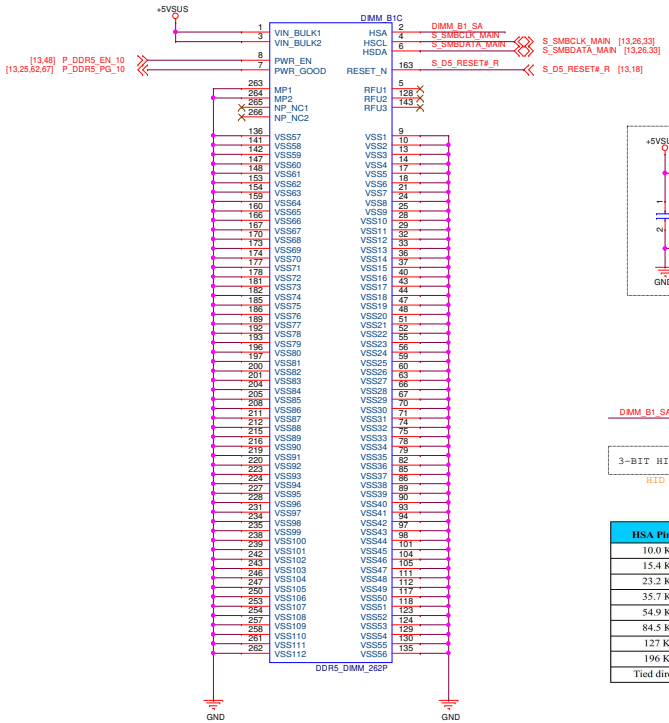
Size	Project Name	Rev
Custom	MIX-Q670D1	R1.00

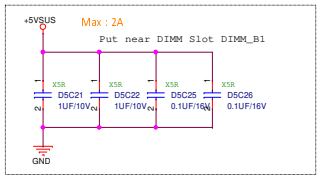
Date: Tuesday, August 23, 2022 Sheet 13 of 70

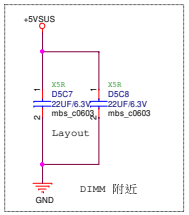
DDR5 SODIMM CHANNEL -B











3-BIT HID = 010

HID address for 2nd DIMM is 010 and resistor value is 23.2K

Put One Caps Per DIMM Slot

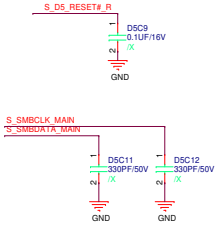
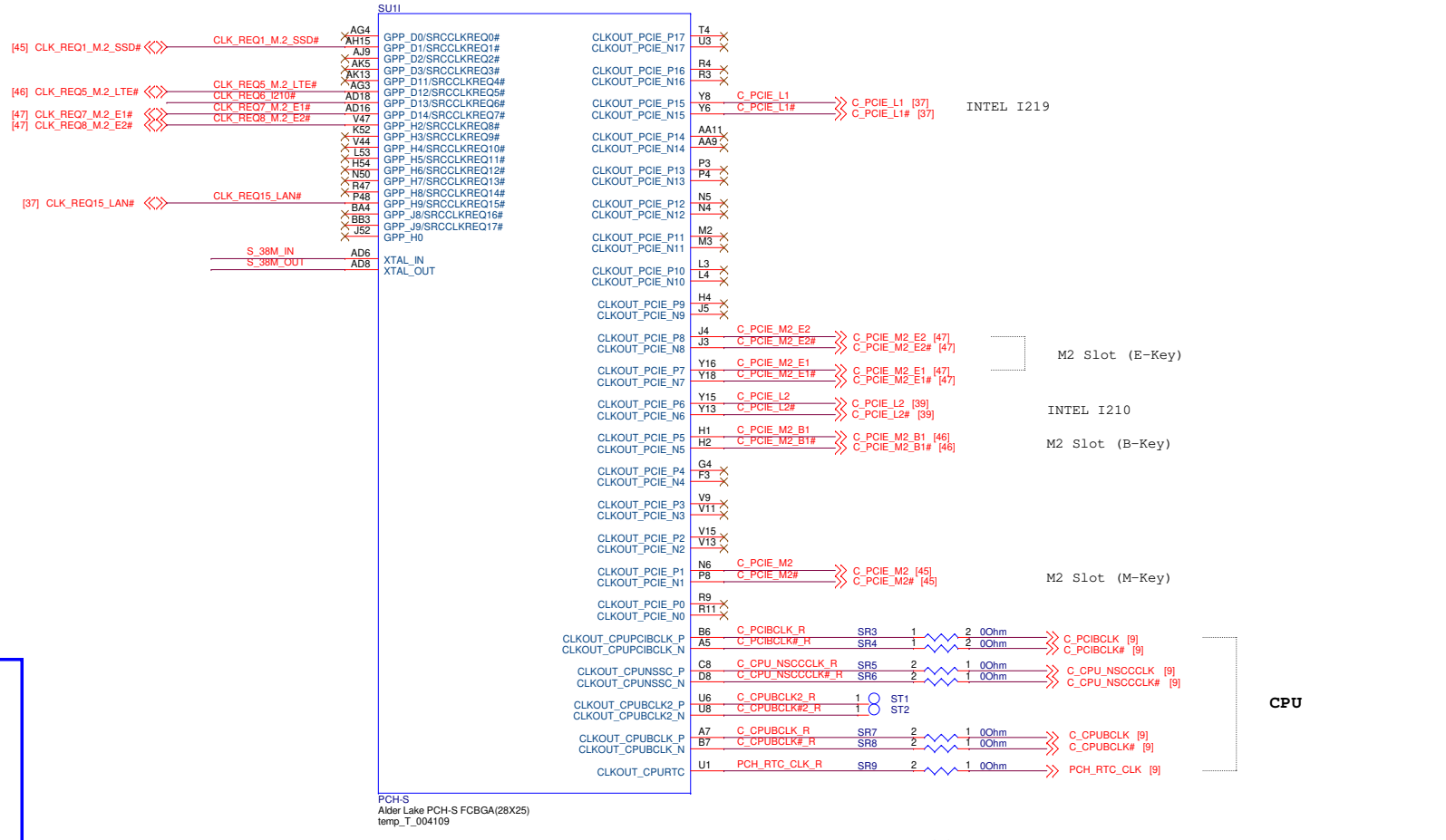
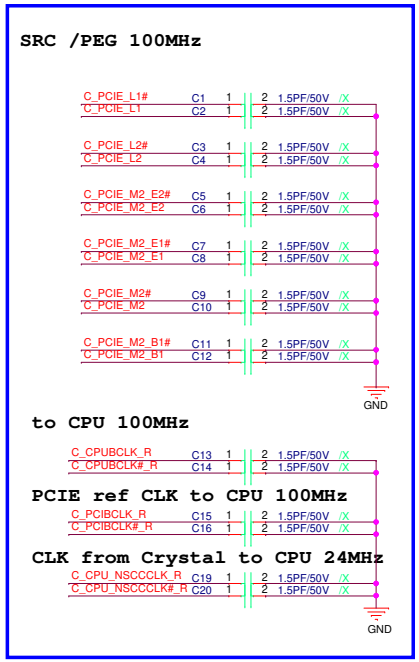
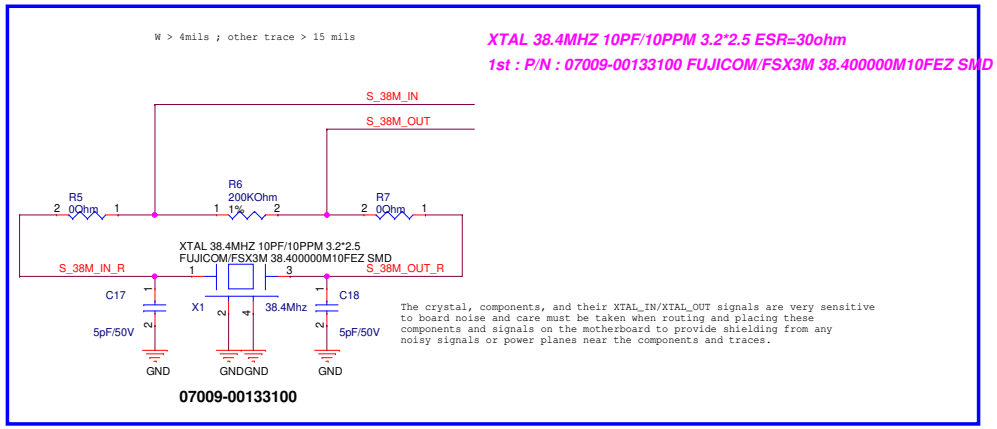


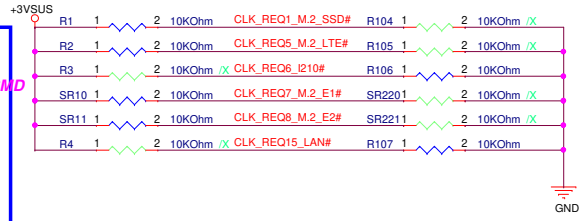
Table 91 — HSA Pin Resistor Value and ID - SPD5 Family

HSA Pin Connection	3-bit HID	Comment
10.0 KΩ to GND	HID = 000	1% Resistor
15.4 KΩ to GND	HID = 001	
23.2 KΩ to GND	HID = 010	
35.7 KΩ to GND	HID = 011	
54.9 KΩ to GND	HID = 100	
84.5 KΩ to GND	HID = 101	
127 KΩ to GND	HID = 110	
196 KΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline Mode; Write protect override enabled

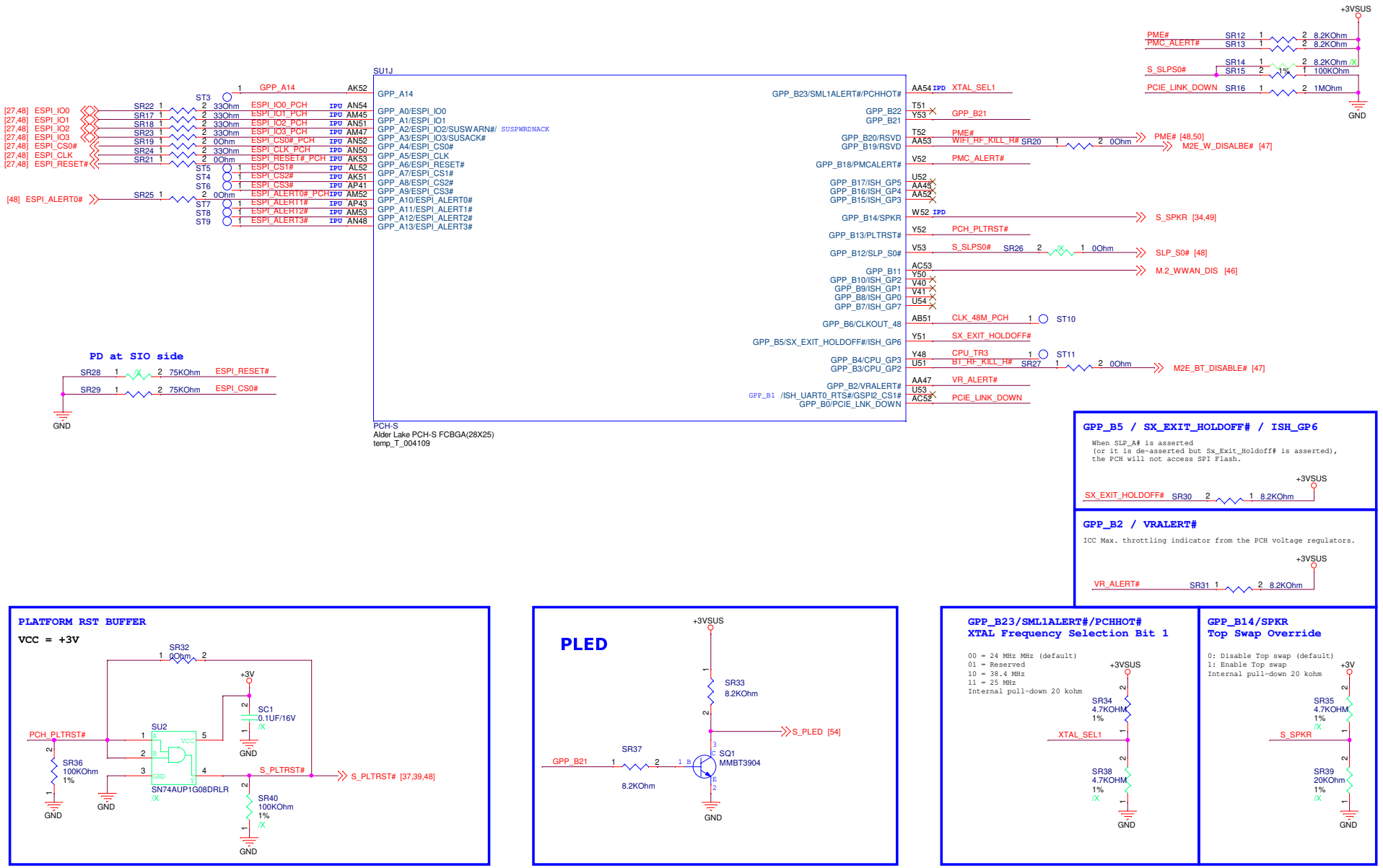








ASUS	Title : CPTH (CLOCK)		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size A3	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 15 of 70		



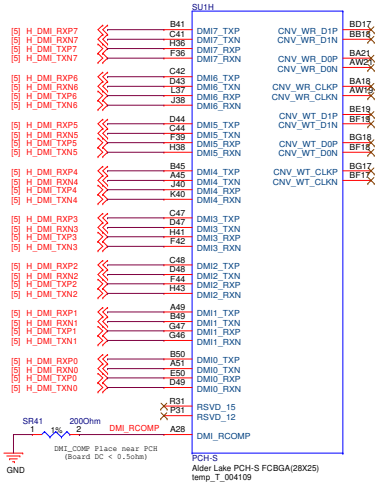
ASUSTek COMPUTER INC.

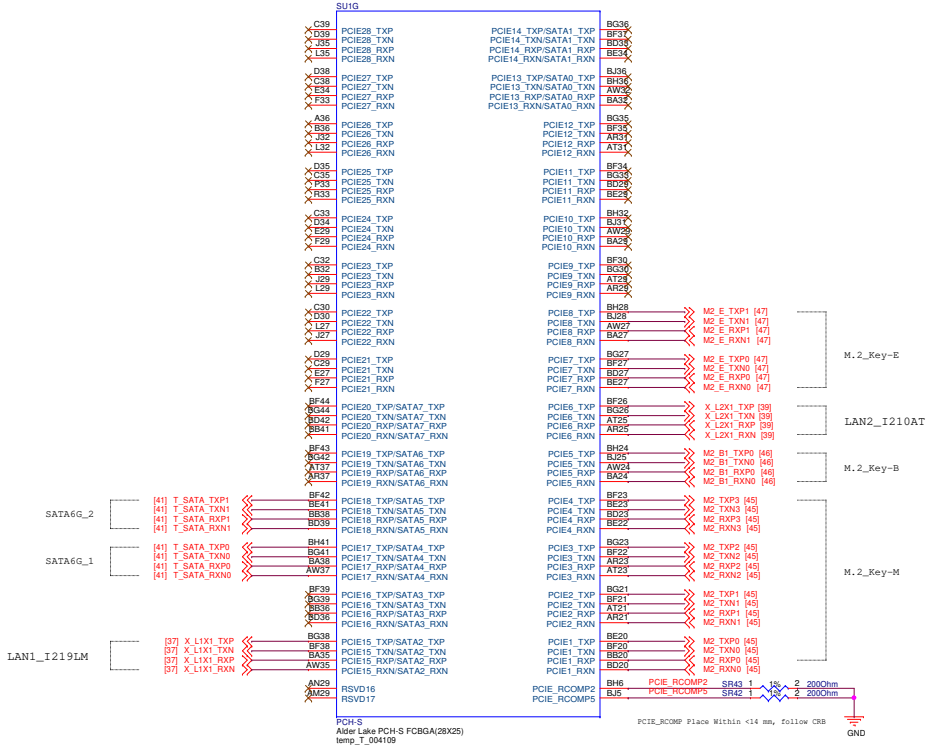
Title : CPTH (eSPI/ISH)

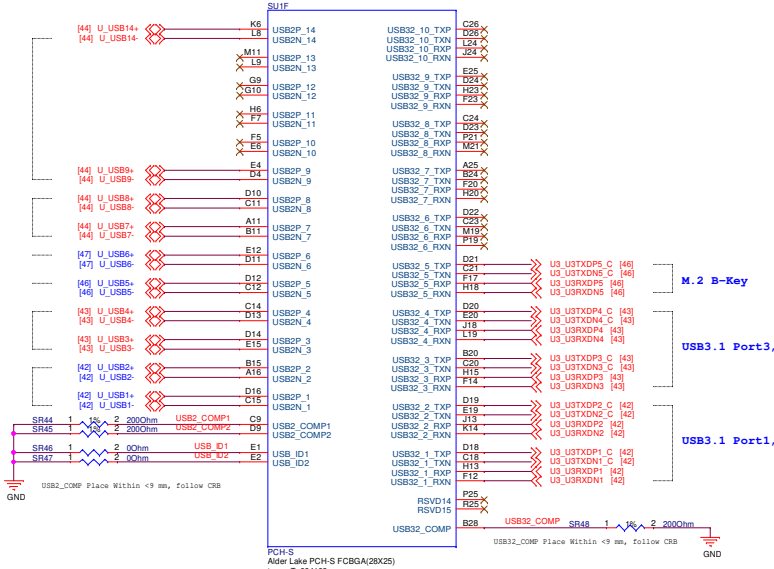
Engineer: IPC-EE2

Size	Project Name	Rev
A3	MIX-Q670D1	R1.00

Date: Tuesday, August 23, 2022 Sheet 16 of 70



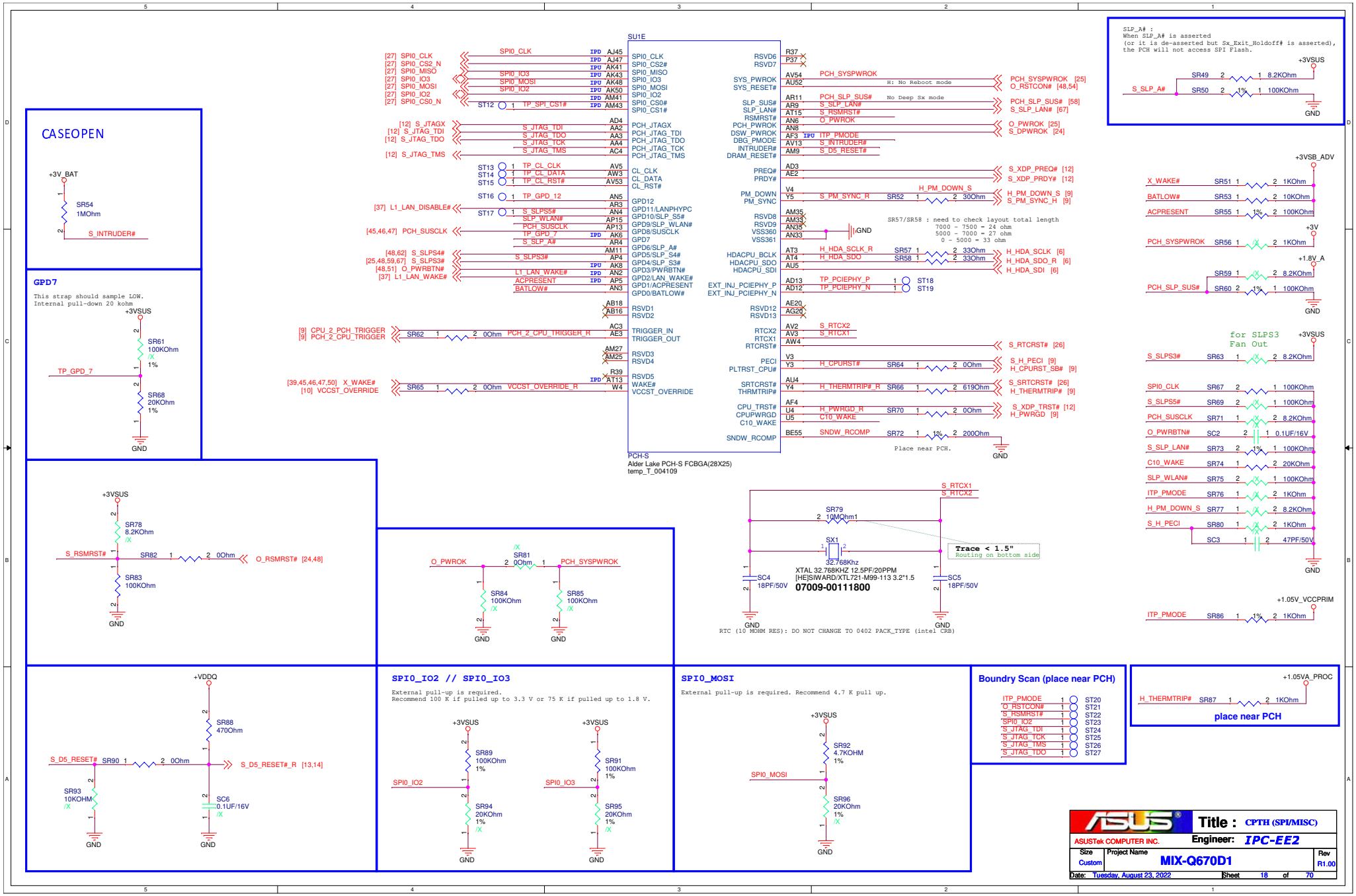


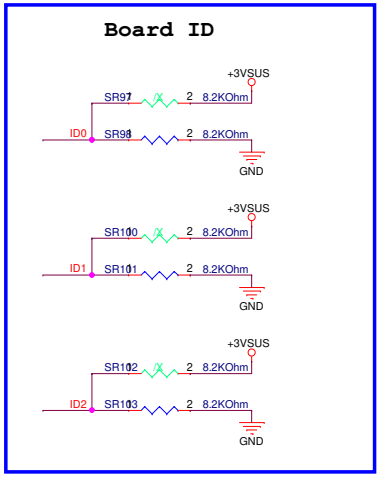


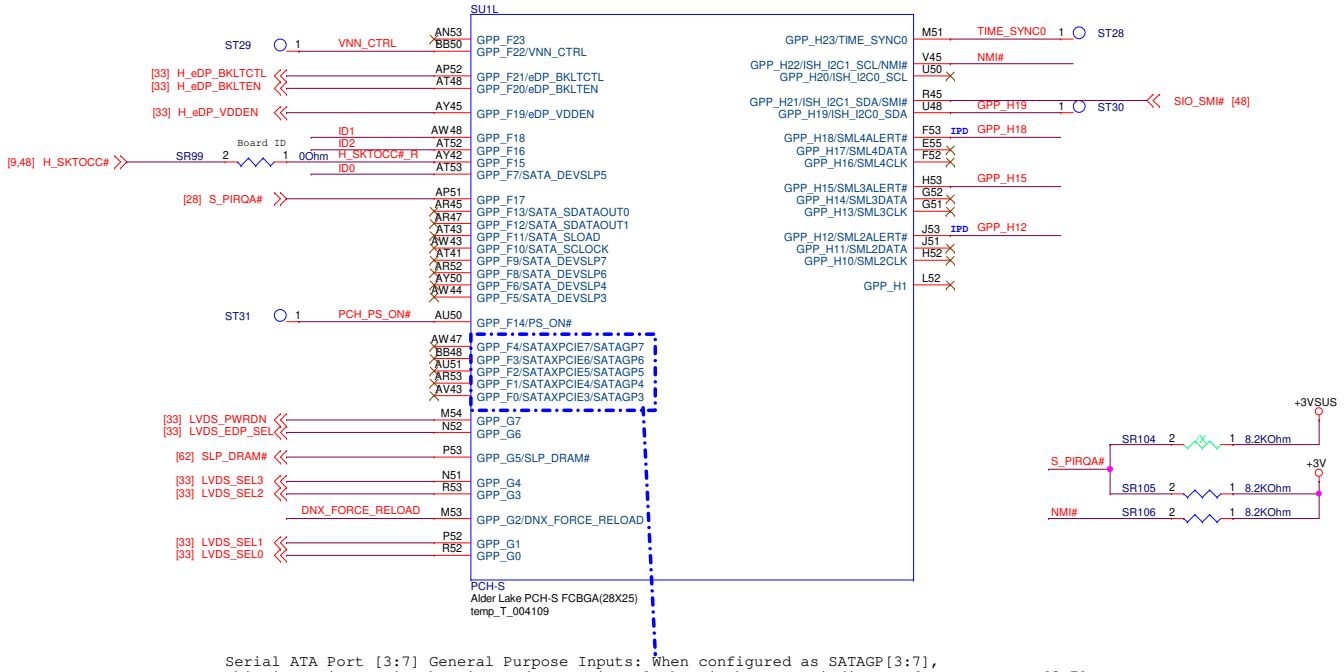
ADL PCH-S Supported PCI Express* Link Configurations

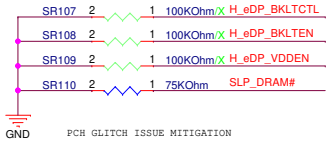
PCH-S	North PGS - Flex HSIO Lanes																				South PD - Flex HSIO Lanes							
Flex I/O Lanes	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
PCIe Controllers	1				2				3				4				5				6				7			
PCIe Max Rate	Gen3				Gen3				Gen3				Gen4				Gen3				Gen4				Gen4			
PCIe Lanes	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Logical Link Lanes: 1x4	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Logical Link Lanes: 1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Logical Link Lanes: 2x2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Logical Link Lanes: 2x2 LR	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Logical Link Lanes: 1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
Logical Link Lanes: 4x1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Assigned Root Ports: 1x4	RP1				RP5				RP9				RP13				RP17				RP21				RP25			
Assigned Root Ports: 1x4 LR	RP1				RP5				RP9				RP13				RP17				RP21				RP25			
Assigned Root Ports: 2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15		RP17		RP19		RP21		RP23		RP25		RP27	
Assigned Root Ports: 2x2 LR	RP3		RP1		RP7		RP5		RP11		RP9		RP15		RP13		RP19		RP17		RP23		RP21		RP27		RP25	
Assigned Root Ports: 1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16	RP17		RP19	RP20	RP21		RP23	RP24	RP25		RP27	RP28
Assigned Root Ports: 4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18	RP19	RP20	RP21	RP22	RP23	RP24	RP25	RP26	RP27	RP28

ASUSTeK COMPUTER INC.	Title : CPTH (PCIE/DMI/USB/SATA)		
	Engineer: IPC-EE2		
Size: C	Project Name: MIX-Q670D1		Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 17 of 70		


CASEOPEN
+3V_BAT
SR54
1MOhm
S_INTRUDER#
GPD7
This strap should sample LOW.
Internal pull-down 20 kohm
+3VSUS
SR61
100KOhm
/X
1%
TP_GPD_7
SR68
20KOhm
1%
GND
SU1E
PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109
SLP_A# :
When SLP_A# is asserted
(or it is de-asserted but Sx_Exit_Holdoff# is asserted),
the PCH will not access SPI Flash.
+3VSUS
SR49 2 1 8.2KOhm
S_SLP_A#
SR50 2 1% 1 100KOhm
GND
+3VSB_ADV
X_WAKE# SR51 1 2 1KOhm
BATLOW# SR53 1 2 10KOhm
ACPRESENT SR55 1 1% 2 100KOhm
+3V
PCH_SYSPWROK SR56 1 /X 2 1KOhm
+1.8V_A
SR59 1 /X 2 8.2KOhm
PCH_SLP_SUS# SR60 2 1% 1 100KOhm
GND
for SLPS3
Fan Out
+3VSUS
S_SLPS3# SR63 1 /X 2 8.2KOhm
SPI0_CLK SR67 2 1 100KOhm
S_SLPS5# SR69 2 /X 1 100KOhm
PCH_SUSCLK SR71 1 /X 2 8.2KOhm
O_PWRBTN# SC2 2 1 0.1UF/16V
S_SLP_LAN# SR73 2 1% 1 100KOhm
C10_WAKE SR74 1 2 20KOhm
SLP_WLAN# SR75 2 /X 1 100KOhm
ITP_PMODE SR76 1 /X 2 1KOhm
H_PM_DOWN_S SR77 1 /X 2 8.2KOhm
S_H_PECI SR80 1 /X 2 1KOhm
SC3 1 2 47PF/50V
GND
+1.05V_VCCPRIM
ITP_PMODE SR86 1 1% 2 1KOhm
+3VSUS
SR78
8.2KOhm
/X
S_RSMRST# SR82 1 2 0Ohm O_RSMRST# [24,48]
SR83
100KOhm
GND
O_PWROK
/X
SR81
0Ohm
PCH_SYSPWROK
SR84
100KOhm
/X
SR85
100KOhm
/X
GND
S_RTCX1
S_RTCX2
SR79
10MOhm1
SX1
32.768Khz
Trace < 1.5"
Routing on bottom side
XTAL 32.768KHZ 12.5PF/20PPM
[HE]SIWARD/XTL721-M99-113 3.2*1.5
07009-00111800
SC4
18PF/50V
SC5
18PF/50V
GND
RTC (10 MOHM RES): DO NOT CHANGE TO 0402 PACK_TYPE (intel CRB)
+VDDQ
SR88
470Ohm
S_D5_RESET# SR90 1 2 0Ohm S_D5_RESET#_R [13,14]
SR93
10KOHM
/X
SC6
0.1UF/16V
/X
GND
SPI0_IO2 // SPI0_IO3
External pull-up is required.
Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V.
+3VSUS
SR89
100KOhm
1%
SPI0_IO2
SR94
20KOhm
1%
/X
SR91
100KOhm
1%
SPI0_IO3
SR95
20KOhm
1%
/X
GND
SPI0_MOSI
External pull-up is required. Recommend 4.7 K pull up.
+3VSUS
SR92
4.7KOHM
1%
SPI0_MOSI
SR96
20KOhm
1%
/X
GND
Boundry Scan (place near PCH)
ITP_PMODE ST20
O_RSTCON# ST21
S_RSMRST# ST22
SPI0_IO2 ST23
S_JTAG_TDI ST24
S_JTAG_TCK ST25
S_JTAG_TMS ST26
S_JTAG_TDO ST27
+1.05VA_PROC
H_THERMTRIP# SR87 1 2 1KOhm
place near PCH
ASUS
Title : CPTH (SPI/MISC)
ASUSTek COMPUTER INC.
Engineer: IPC-EE2
Size Custom
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 18 of 70







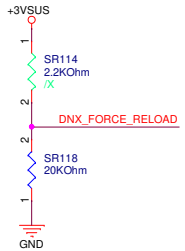
Serial ATA Port [3:7] General Purpose Inputs: When configured as SATAGP[3:7],
this is an input pin that is used as an interlock switch status indicator for SATA Port [3:7].
Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPP_F[0:4]. Pin defaults to Native mode as SATAXPCIE[3:7] depends on soft-strap.

GPP_G2 / DNX_FORCE_RELOAD

Download and Execute (DnX):IntelR CSME ROM samples this pin any time ROM begins execution.
This includes the following conditions:

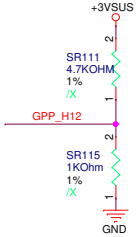
- G3 Exit.
- Sx, Moff Exit.
- Cold Reset(Host Reset with Power Cycle) Exit.
- Warm Reset(Host Reset without Power Cycle) Exit if IntelR CSME was shutdown in Warm Reset.

L => No DnX
H => Enter DnX mode
Note : This pin must not be sampled high at the sampling time for normal operation .



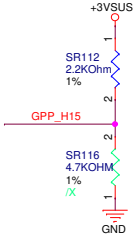
GPP_H12 / SML2ALERT# eSPI Flash Sharing Mode

0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Internal pull-down 20 kohm



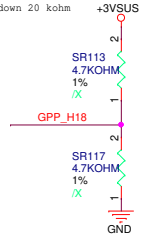
GPP_H15 / SML3ALERT# JTAG ODT Disable

0 = JTAG ODT is disabled (default)
1 = JTAG ODT is enabled
Internal pull-down 20 kohm



GPP_H18 / SML4ALERT# VCCSPI Voltage Configuration

0 = VCCSPI at 3.3 V (Default)
1 = VCCSPI at 1.8 V
Internal pull-down 20 kohm

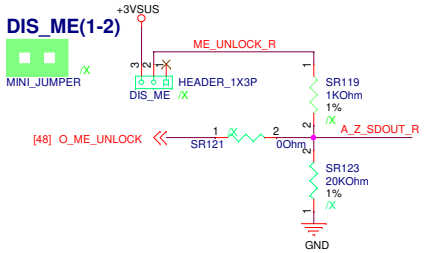


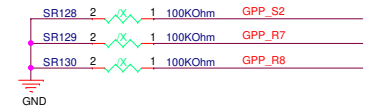
ASUSTek COMPUTER INC.	Title : CPTH (GPIO_F/G/H)	Engineer: IPC-EE2
Size: Custom	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 19 of 70	

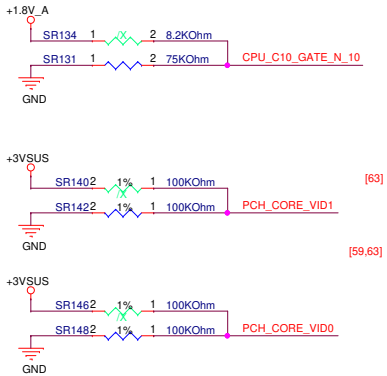
GPP_R2 / HDA_SDO / HDACPU_SDO
Flash Descriptor Security Override

0: Enable security measures defined in the Flash Descriptor. (Default)
1: Disable Flash Descriptor Security (override).

This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
Internal pull-down 20 kohm



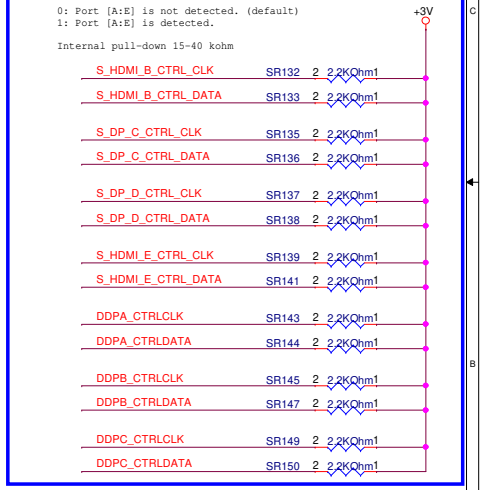




GPP_R[12:21]_I[5:8] / DDP[1:4,A:C] _CTRLDATA

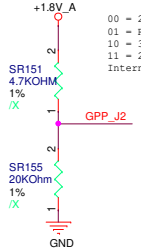
0: Port [A:E] is not detected. (default)
1: Port [A:E] is detected.

Internal pull-down 15-40 kohm



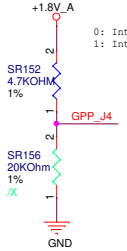
GPP_J2 / CNV_BRI_DT / UART0_RTS#
XTAL Frequency Selection Bit 0

00 = 24 MHz MHz (default)
01 = Reserved
10 = 38.4 MHz
11 = 25 MHz
Internal pull-down 20 kohm



GPP_J4 / CNV_RGI_DT / UART0_TXD
M.2 CNVi Mode Select

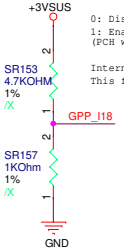
0: Integrated CNVi enable
1: Integrated CNVi disable



GPP_I18 / GSPI0_MOSI
No Reboot

0: Disable "No Reboot" mode. (Default)
1: Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

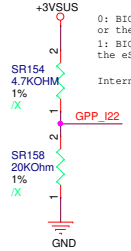
Internal pull-down 20 kohm
This function is useful when running ITP/ XDP.



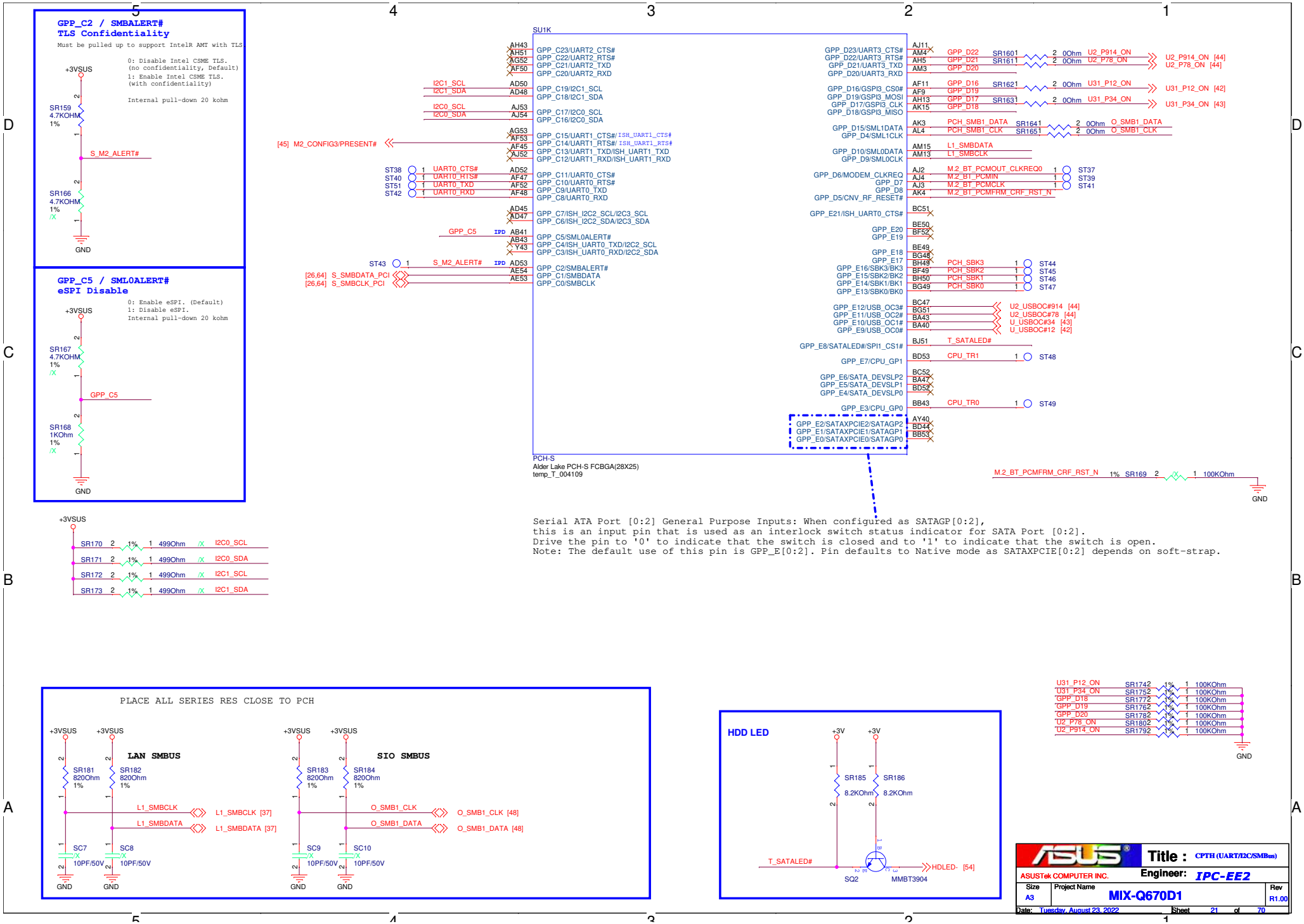
GPP_I22 / GSPI1_MOSI
Boot BIOS Strap (BBS)

0: BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF)
1: BIOS fetches are routed to the eSPI Peripheral Channel

Internal pull-down 20 kohm

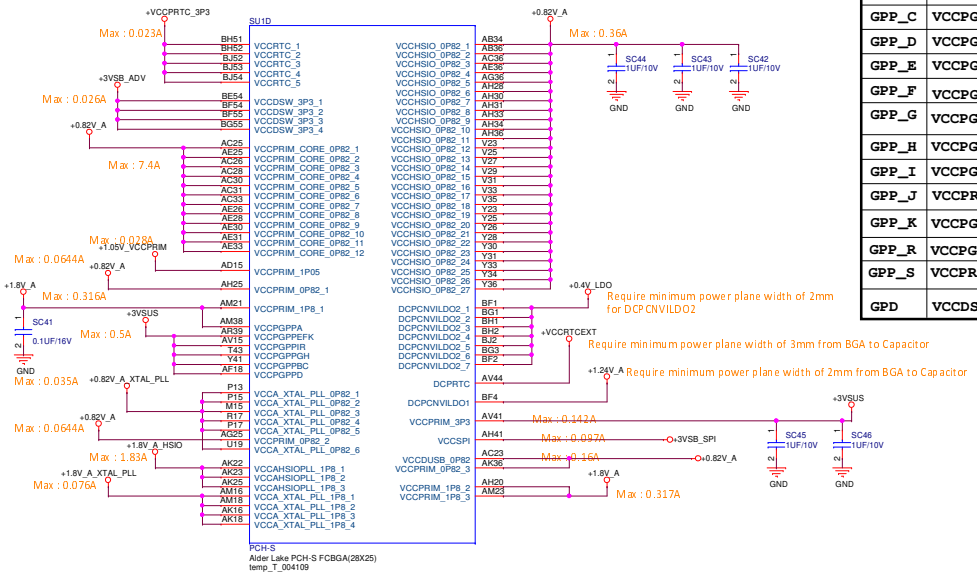


ASUSTek COMPUTER INC.	Title : CPTH (AUDIO/DISPLAY/CNVi)		
	Engineer: IPC-EE2		
Size A3	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 20 of 70		


GPP_C2 / SMBALERT#
TLS Confidentiality
Must be pulled up to support IntelR AMT with TLS
0: Disable Intel CSME TLS. (no confidentiality, Default)
1: Enable Intel CSME TLS. (with confidentiality)
Internal pull-down 20 kohm
+3VSUS
SR159 4.7KOHM 1%
S_M2_ALERT#
SR166 4.7KOHM 1% /X
GND
GPP_C5 / SML0ALERT#
eSPI Disable
0: Enable eSPI. (Default)
1: Disable eSPI.
Internal pull-down 20 kohm
SR167 4.7KOHM 1% /X
GPP_C5
SR168 1KOhm 1% /X
SU1K
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C7/ISH_I2C2_SCL/I2C3_SCL
GPP_C6/ISH_I2C2_SDA/I2C3_SDA
GPP_C5/SML0ALERT#
GPP_C4/ISH_UART0_TXD/I2C2_SCL
GPP_C3/ISH_UART0_RXD/I2C2_SDA
GPP_C2/SMBALERT#
GPP_C1/SMBDATA
GPP_C0/SMBCLK
GPP_D23/UART3_CTS#
GPP_D22/UART3_RTS#
GPP_D21/UART3_TXD
GPP_D20/UART3_RXD
GPP_D16/GSPI3_CS0#
GPP_D19/GSPI3_MOSI
GPP_D17/GSPI3_CLK
GPP_D18/GSPI3_MISO
GPP_D15/SML1DATA
GPP_D4/SML1CLK
GPP_D10/SML0DATA
GPP_D9/SML0CLK
GPP_D6/MODEM_CLKREQ
GPP_D7
GPP_D8
GPP_D5/CNV_RF_RESET#
GPP_E21/ISH_UART0_CTS#
GPP_E20
GPP_E19
GPP_E18
GPP_E17
GPP_E16/SBK3/BK3
GPP_E15/SBK2/BK2
GPP_E14/SBK1/BK1
GPP_E13/SBK0/BK0
GPP_E12/USB_OC3#
GPP_E11/USB_OC2#
GPP_E10/USB_OC1#
GPP_E9/USB_OC0#
GPP_E8/SATALED#/SPI1_CS1#
GPP_E7/CPU_GP1
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_E3/CPU_GP0
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E0/SATAXPCIE0/SATAGP0
PCH-S
Alder Lake PCH-S FCBGA(28X25)
temp_T_004109
[45] M2_CONFIG3/PRESENT#
[26,64] S_SMBDATA_PCI
[26,64] S_SMBCLK_PCI
U2_P914_ON [44]
U2_P78_ON [44]
U31_P12_ON [42]
U31_P34_ON [43]
U2_USBOC#914 [44]
U2_USBOC#78 [44]
U_USBOC#34 [43]
U_USBOC#12 [42]
M.2_BT_PCMFRM_CRF_RST_N
SR169 100KOhm
Serial ATA Port [0:2] General Purpose Inputs: When configured as SATAGP[0:2],
this is an input pin that is used as an interlock switch status indicator for SATA Port [0:2].
Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
Note: The default use of this pin is GPP_E[0:2]. Pin defaults to Native mode as SATAXPCIE[0:2] depends on soft-strap.
SR170 499Ohm I2C0_SCL
SR171 499Ohm I2C0_SDA
SR172 499Ohm I2C1_SCL
SR173 499Ohm I2C1_SDA
PLACE ALL SERIES RES CLOSE TO PCH
LAN SMBUS
SR181 820Ohm 1%
SR182 820Ohm 1%
L1_SMBCLK
L1_SMBDATA
L1_SMBCLK [37]
L1_SMBDATA [37]
SC7 10PF/50V
SC8 10PF/50V
SIO SMBUS
SR183 820Ohm 1%
SR184 820Ohm 1%
O_SMB1_CLK
O_SMB1_DATA
O_SMB1_CLK [48]
O_SMB1_DATA [48]
SC9 10PF/50V
SC10 10PF/50V
HDD LED
SR185 8.2KOhm
SR186 8.2KOhm
T_SATALED#
HDLED- [54]
SQ2 MMBT3904
U31_P12_ON SR1742 100KOhm
U31_P34_ON SR1752 100KOhm
GPP_D18 SR1772 100KOhm
GPP_D19 SR1762 100KOhm
GPP_D20 SR1782 100KOhm
U2_P78_ON SR1802 100KOhm
U2_P914_ON SR1792 100KOhm
ASUSTek COMPUTER INC.
Title : CPTH (UART/I2C/SMBus)
Engineer: IPC-EE2
Size A3
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 21 of 70

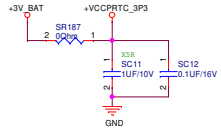
GPIO Voltage Level

Group	Power pin	Power option	Power plane
GPP_A	VCCPGPPA	1.8V or 3.3V	+1.8V_A
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_D	VCCPGPPD	1.8V or 3.3V	+3VSUS
GPP_E	VCCPGPPEFK	1.8V or 3.3V	+3VSUS
GPP_F	VCCPGPPEFK	1.8V or 3.3V	+3VSUS
GPP_G	VCCPGPPGH	1.8V or 3.3V	+3VSUS
GPP_H	VCCPGPPGH	1.8V or 3.3V	+3VSUS
GPP_I	VCCPGPPIR	1.8V or 3.3V	+3VSUS
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPP_K	VCCPGPPEFK	1.8V or 3.3V	+3VSUS
GPP_R	VCCPGPPIR	1.8V or 3.3V	+3VSUS
GPP_S	VCCPRIM_1P8	1.8V Only	+1.8V_A
GPD	VCCDSW_3P3	3.3V Only	+3VSUS



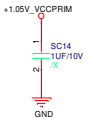
Other Power

SC11, SC12 Place close to the PCH package edge, <10mm



SC13 Place close to the PCH package edge, <5mm
Plan width need >3mm

SC14 Place close to the PCH package edge, <5mm

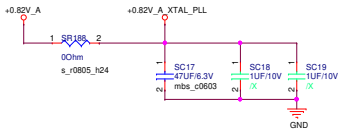


SC21 Place close to the PCH package edge, <5mm
Plan width need >2mm

SC28 Place close to the PCH package edge, <5mm
Plan width need >2mm

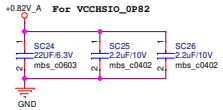
+0.82A

SC17 Place close to the PCH package edge, <10mm
Plan width need >4mm
Need GND shielding.



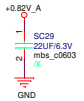
SC18, SC19 Place close to the PCH package edge, <5mm

SC24 Place close to the PCH package edge, <10mm



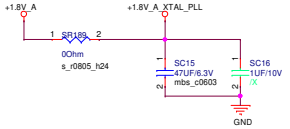
SC25, SC26 Place close to the PCH package edge, <5mm

SC29 Place close to the PCH package edge, <10mm
Plan width need >8mm



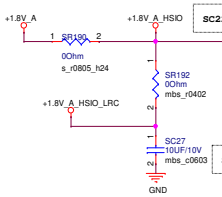
+1.8V_A

SC15 Place close to the PCH package edge, <10mm
Plan width need >3mm
Need GND shielding.



SC16 Place close to the PCH package edge, <5mm

SC22 Place close to the PCH package edge, <5mm



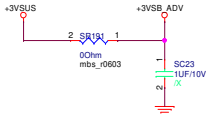
SC27 Place close to the PCH package edge, <10mm

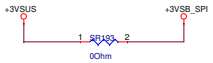
SC30 Place close to the PCH package edge, <5mm
Plan width in package need >3mm, outside need >8mm

+3VSUS

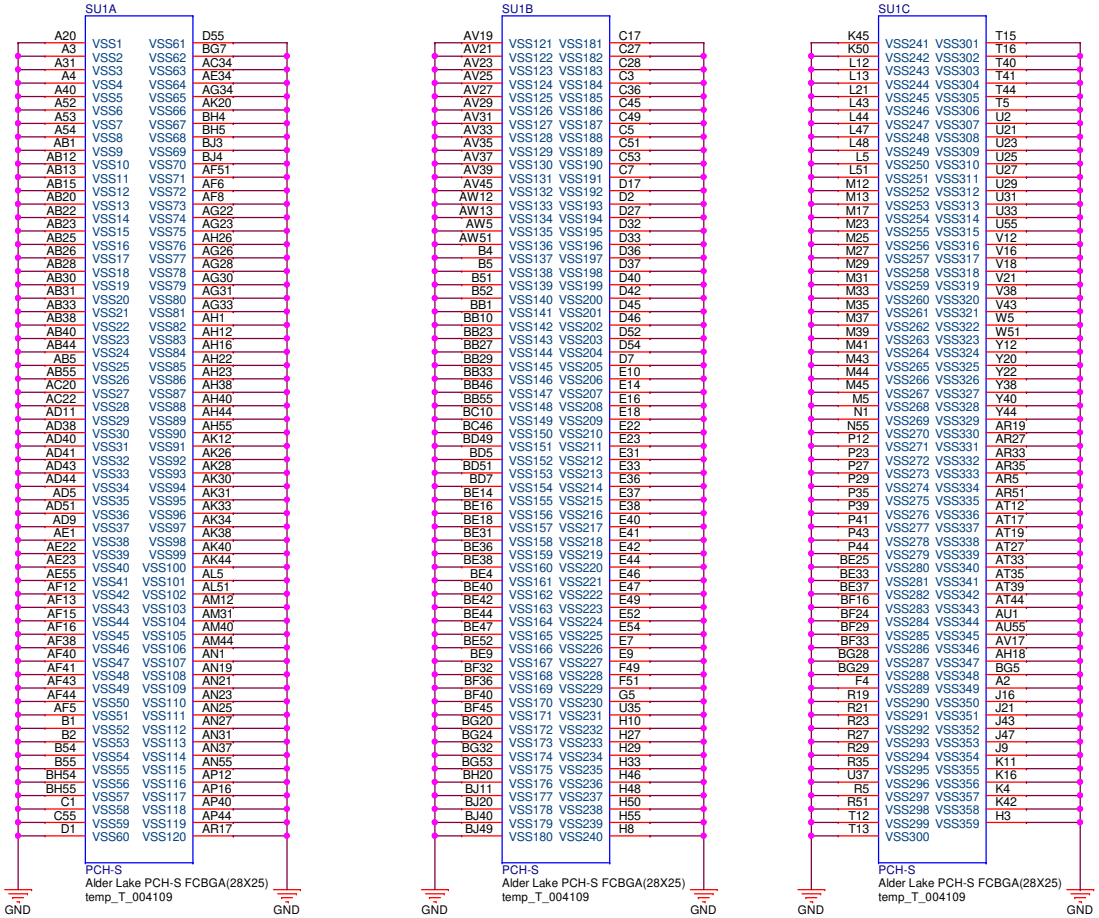
SC20 Place close to the PCH package edge, <5mm
Plan width need >5mm

SC23 Place close to the PCH package edge, <10mm

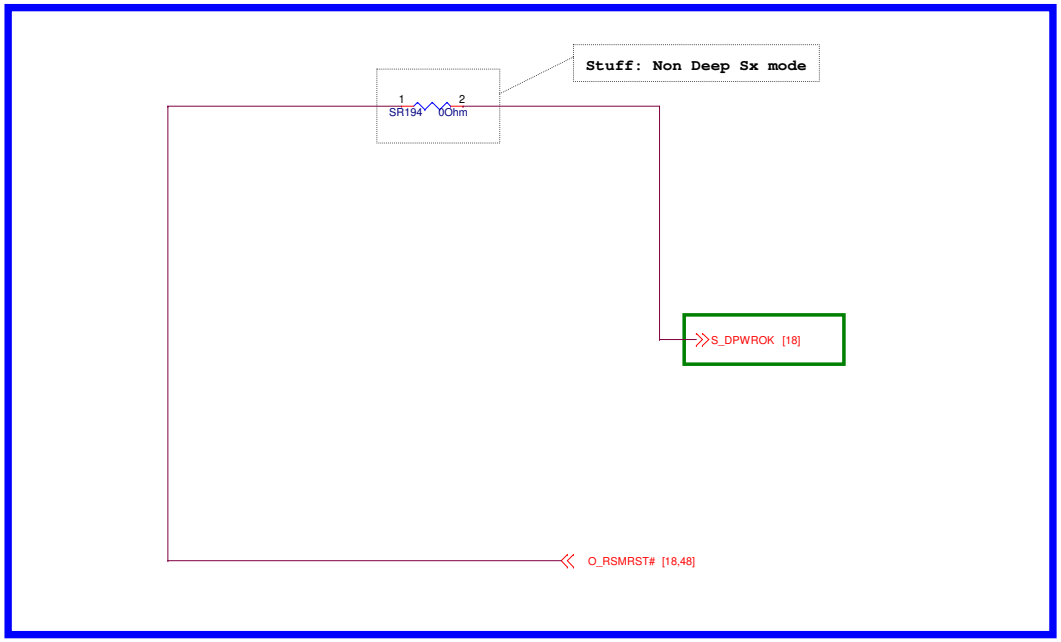


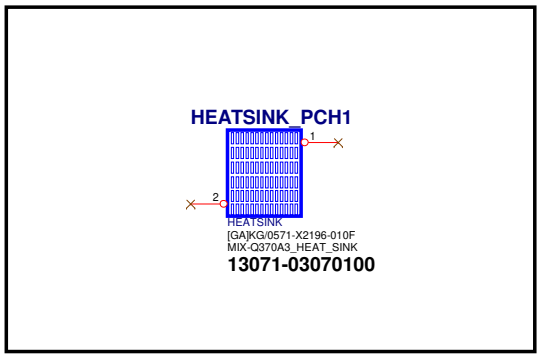


ASUS	Title : KPTH (POWER)	
ASUSTeK COMPUTER INC.	Engineer: IPC-EE2	
Size: C	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 22 of 70	



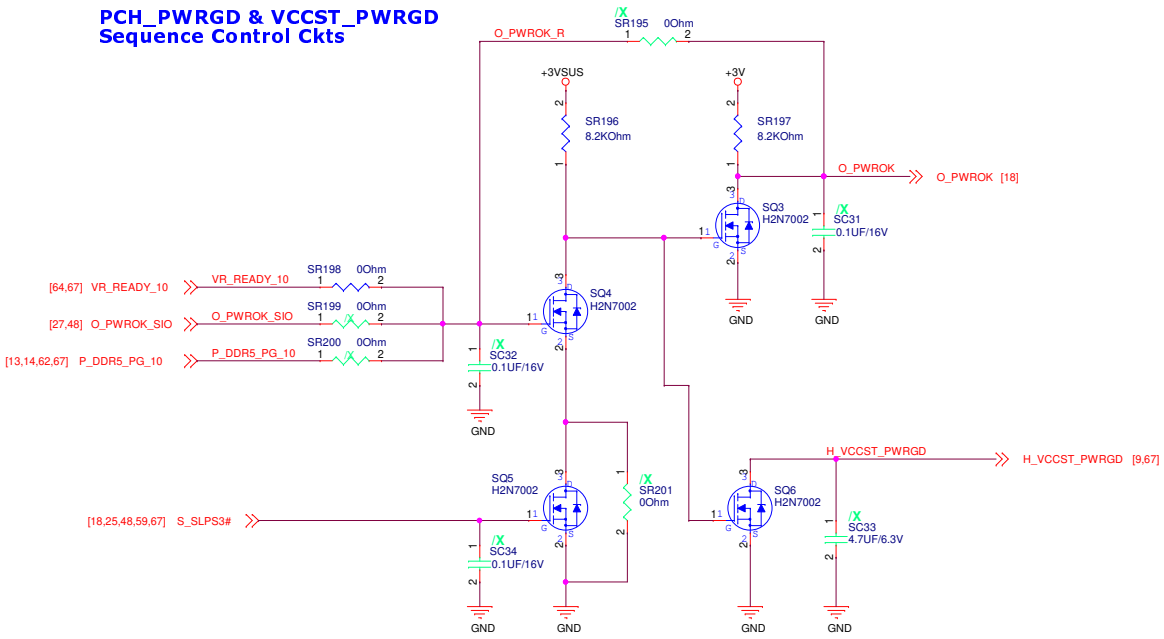
ASUSTek COMPUTER INC.	Title : CPTH (GND)		
	Engineer: IPC-EE2		
Size B	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 23 of 70		



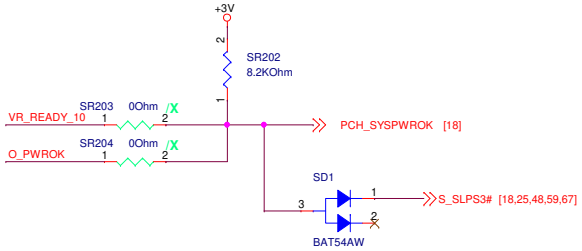


ASUS	Title : CPTH (DSW SEQUENCE)	
ASUSTek COMPUTER INC.	Engineer: IPC-EE2	
Size A3	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 24 of 70	

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



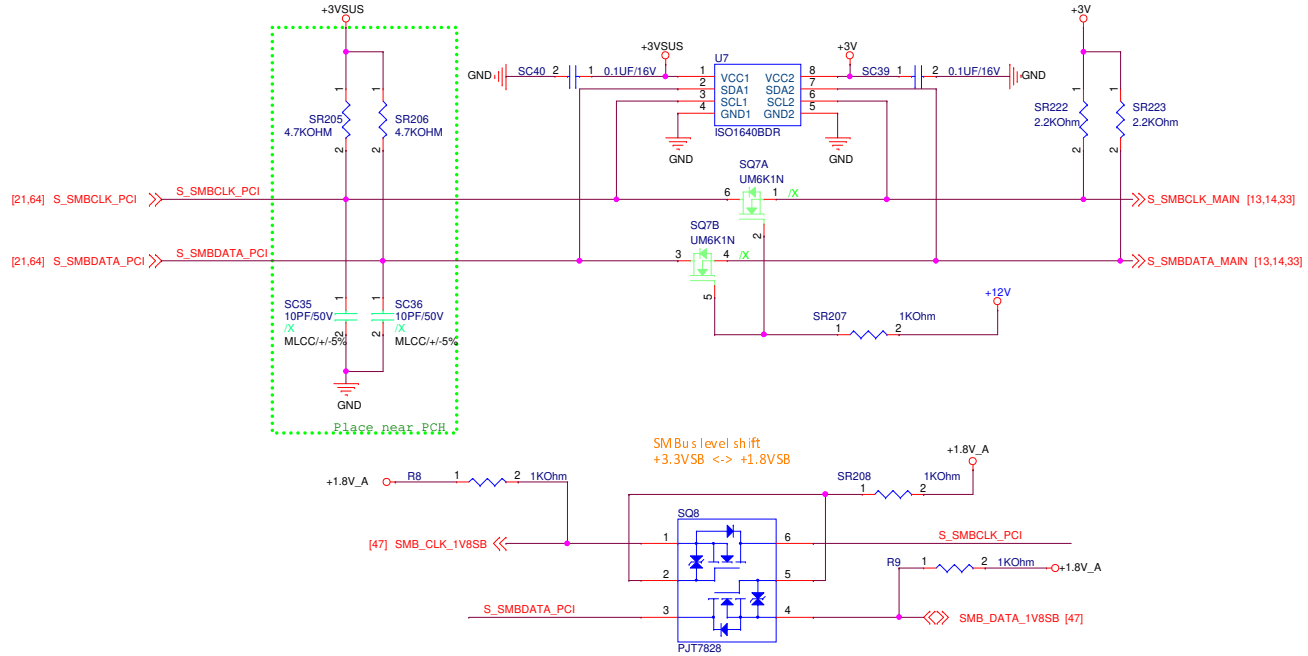
1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

ASUSTek COMPUTER INC.	Title : CETH (PCH/SYS/PROC_PWROK)	
	Engineer: IPC-EE2	
Size A3	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 25 of 70	

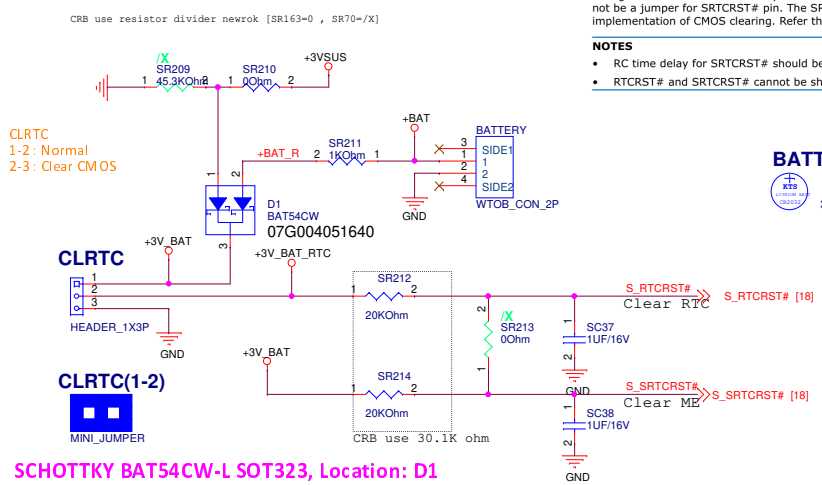


RTC External SRTCRST# Circuit

The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18~25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer the figure above external circuit for PCH RTC.

NOTES

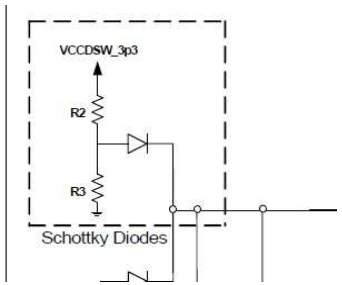
- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.



SCHOTTKY BAT54CW-L SOT323, Location: D1
1st : 07G004203013 PANJIT
2nd : 07G004069020 PANJIT
3rd : 07G004145011 PHILIPS

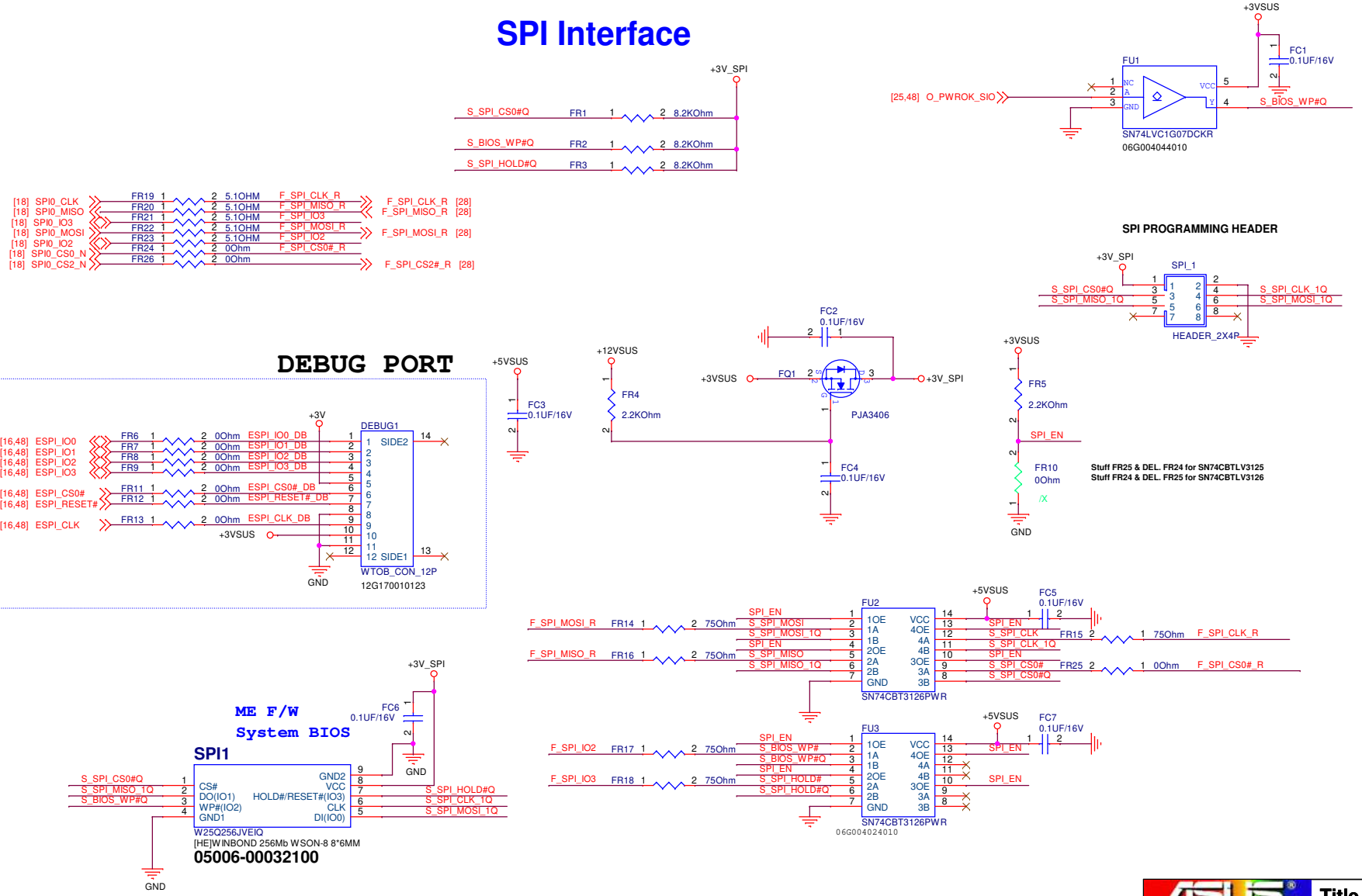
BATTERY1

3V/220mAh



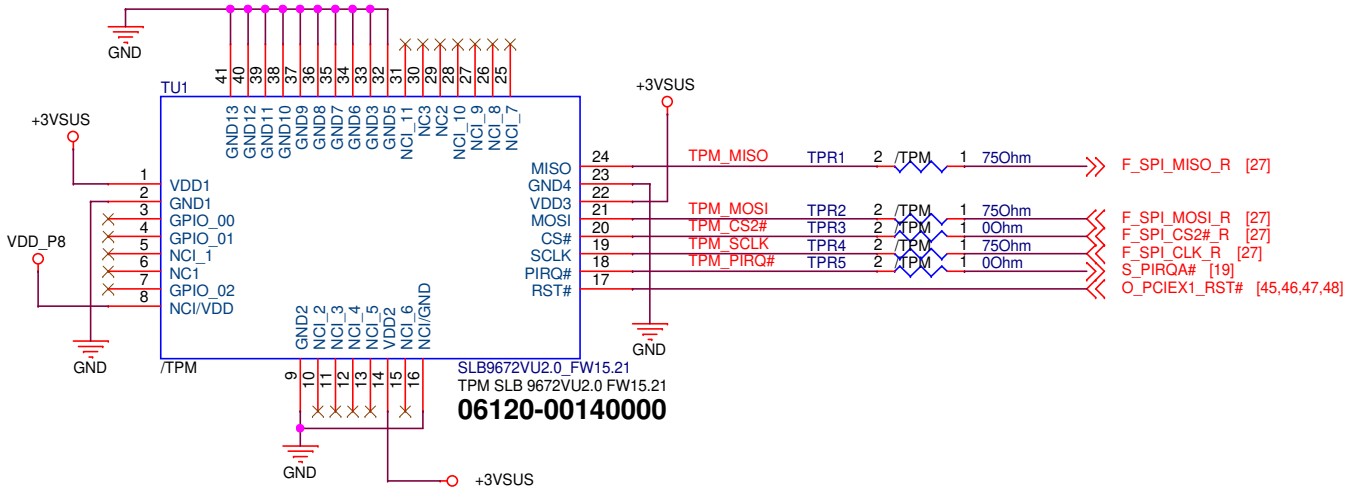
ASUSTek COMPUTER INC.	Title : CPTH (SMBUS/CLRTC)		
	Engineer: IPC-EE2		
Size A3	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 26 of 70		

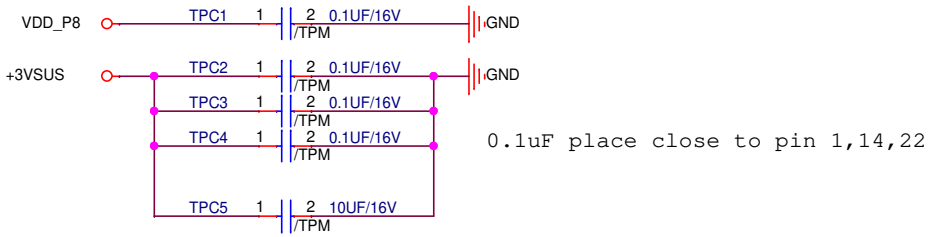
SPI Interface



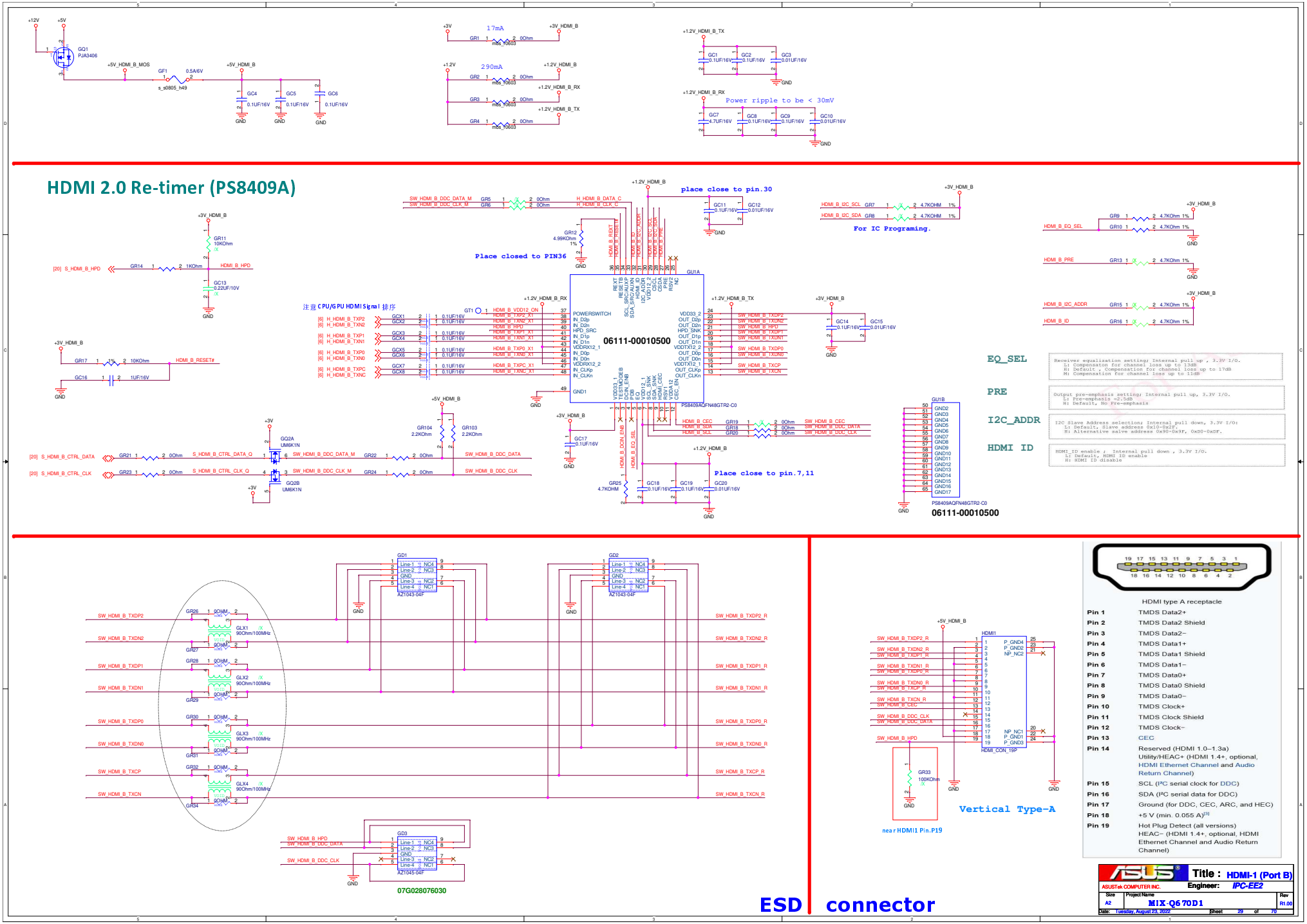
ASUSTek COMPUTER INC.	Title : BIOS/DEBUG	Engineer: IPC-EE2
Size B	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 27 of 70	

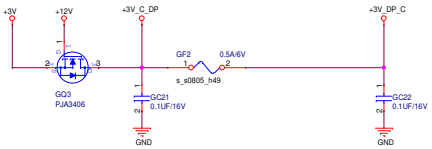
TPM

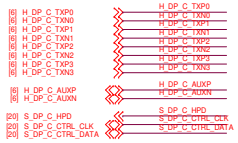


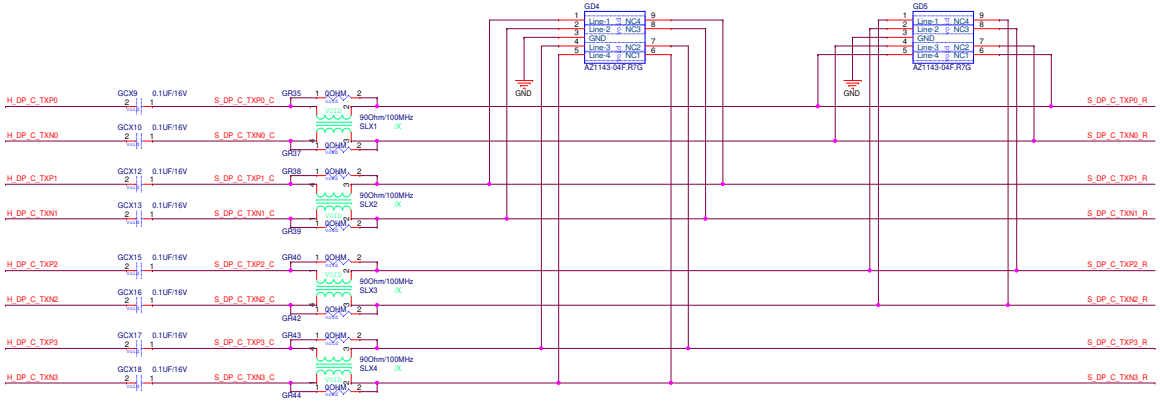


ASUS	Title : TPM SLB 9672VU2.0	
ASUSTek COMPUTER INC.	Engineer: IPC-EE2	
Size A4	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 28 of 70	

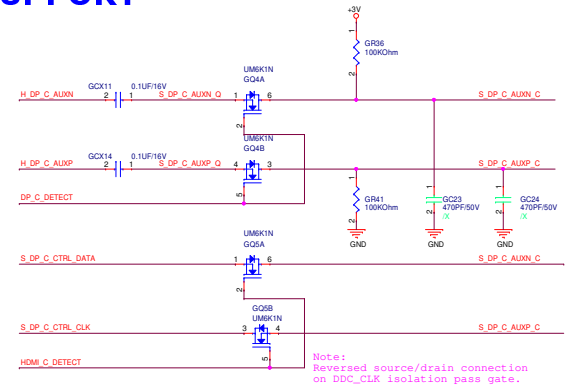

HDMI 2.0 Re-timer (PS8409A)
17mA
290mA
Power ripple to be < 30mV
place close to pin.30
Place closed to PIN36
For IC Programing.
Place close to pin.7,11
06111-00010500
PS8409AQFN48GTR2-C0
EQ_SEL
PRE
I2C_ADDR
HDMI ID
ESD connector
Vertical Type-A
near HDMI1 Pin.P19
07G028076030
HDMI type A receptacle
Pin 1 TMDS Data2+
Pin 2 TMDS Data2 Shield
Pin 3 TMDS Data2−
Pin 4 TMDS Data1+
Pin 5 TMDS Data1 Shield
Pin 6 TMDS Data1−
Pin 7 TMDS Data0+
Pin 8 TMDS Data0 Shield
Pin 9 TMDS Data0−
Pin 10 TMDS Clock+
Pin 11 TMDS Clock Shield
Pin 12 TMDS Clock−
Pin 13 CEC
Pin 14 Reserved (HDMI 1.0–1.3a) Utility/HEAC+ (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)
Pin 15 SCL (I²C serial clock for DDC)
Pin 16 SDA (I²C serial data for DDC)
Pin 17 Ground (for DDC, CEC, ARC, and HEC)
Pin 18 +5 V (min. 0.055 A)[3]
Pin 19 Hot Plug Detect (all versions) HEAC− (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)
Title : HDMI-1 (Port B)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE2
Size A2
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 29 of 70





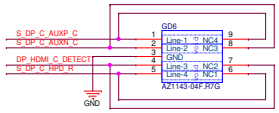


DP/HDMI INTEROPERABILITY SUPPORT

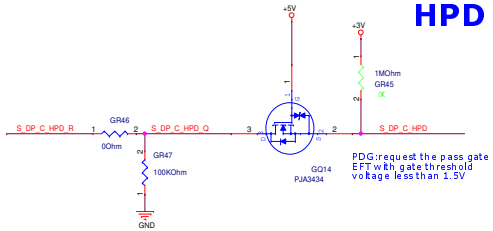


For DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit

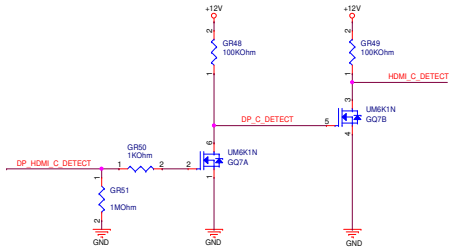
ESD



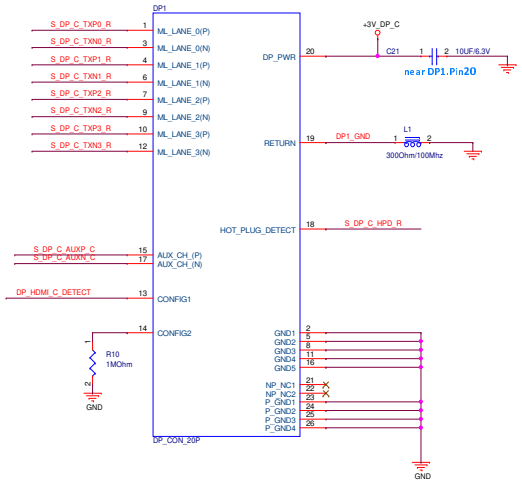
HPD



For HDMI/DP detect

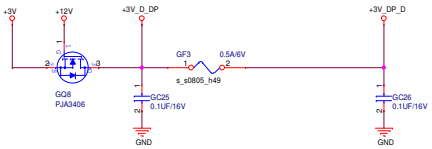


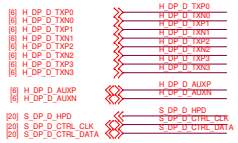
DP-1 (Port C)

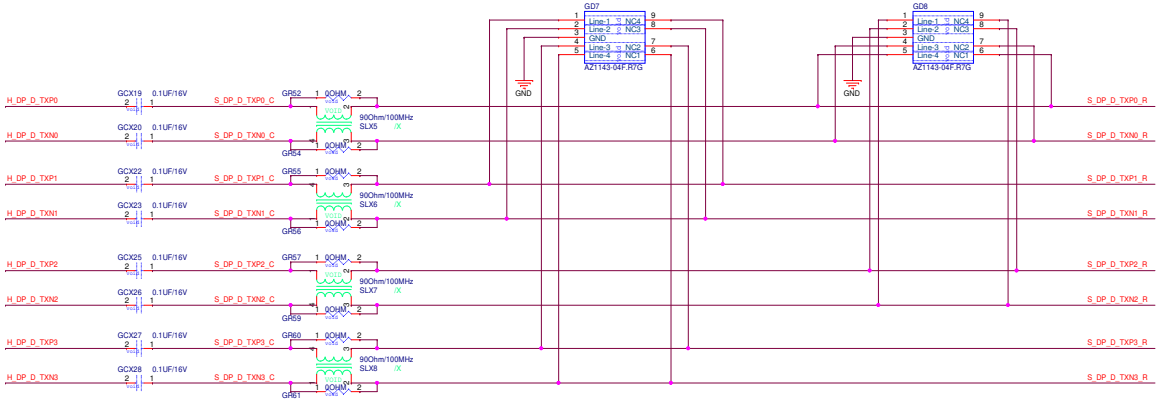


connector

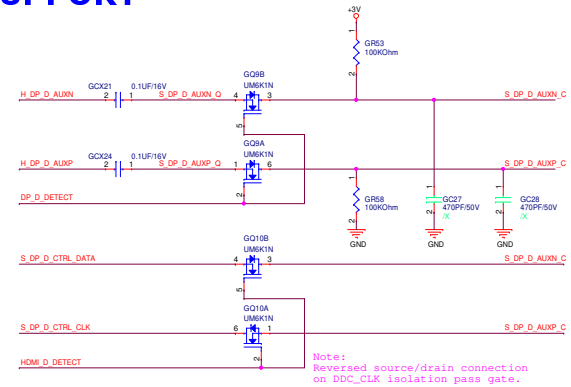
ASUS / ASUSTek COMPUTER INC.	Title : DP-1 (Port C)	
	Engineer: IPC-EE2	
Size: A2	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 30 of 70	



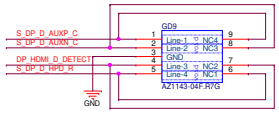




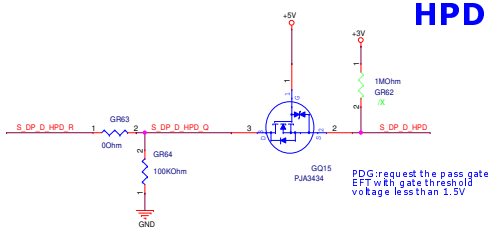
DP/HDMI INTEROPERABILITY SUPPORT



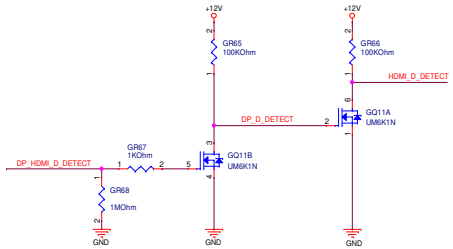
ESD



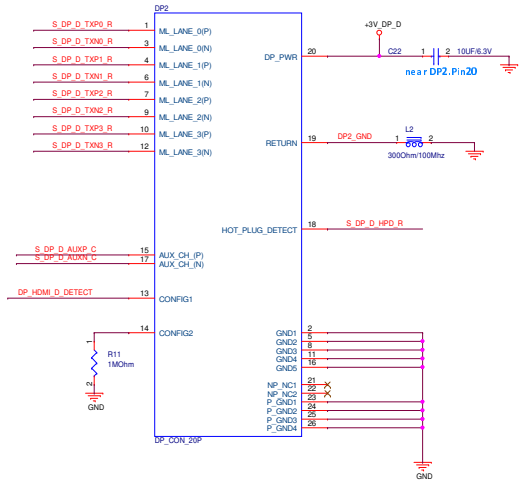
HPD



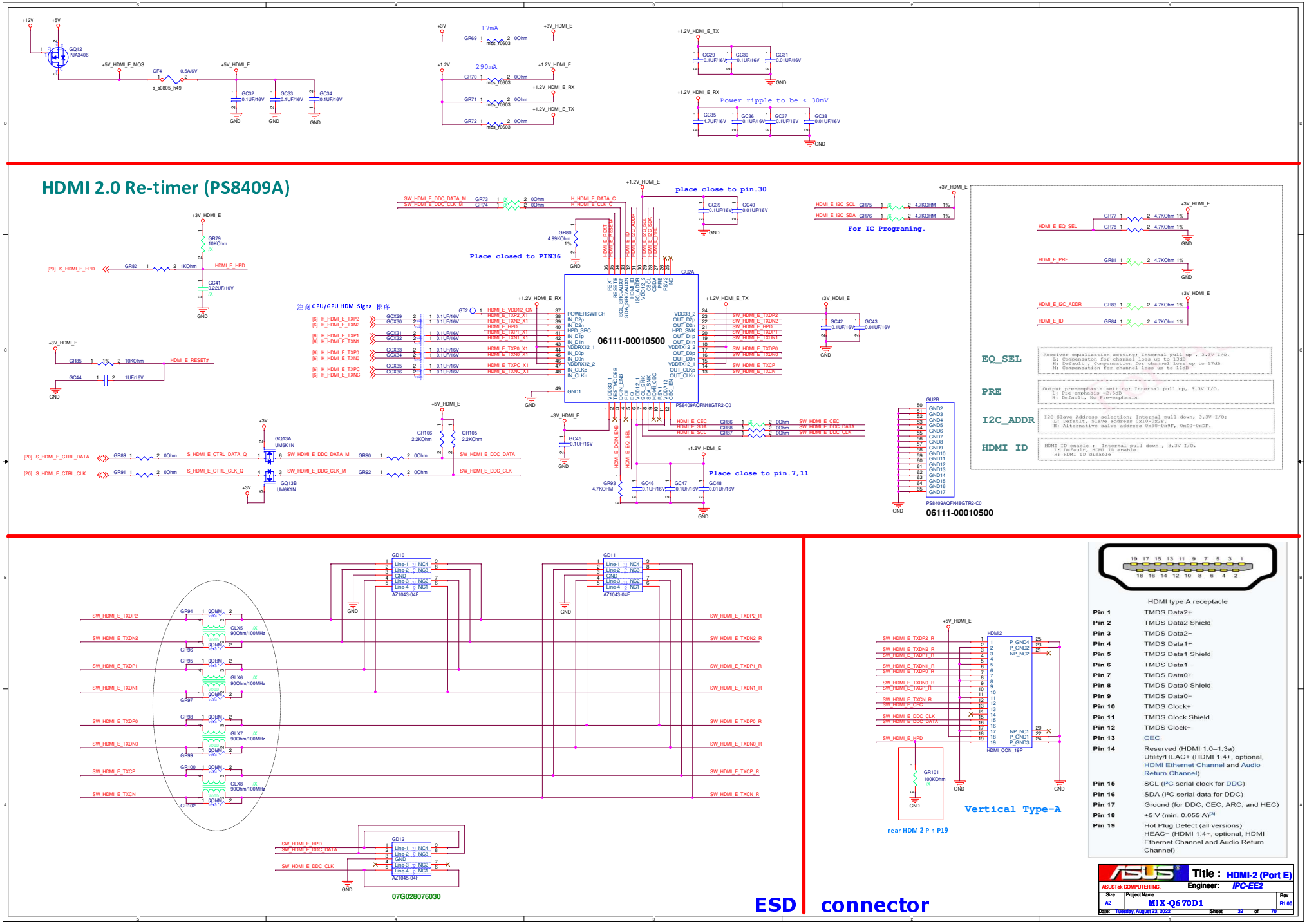
For HDMI/DP detect

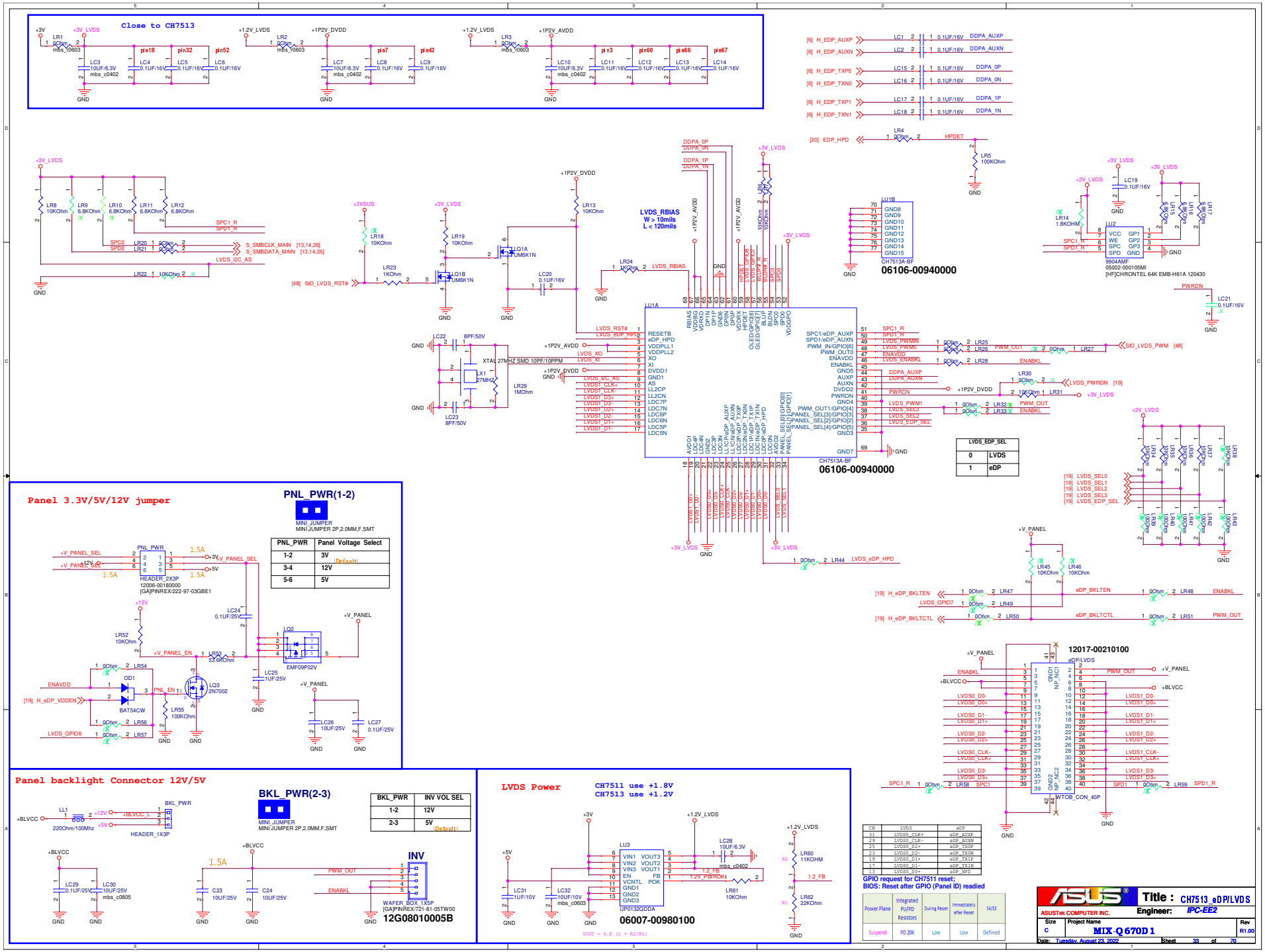


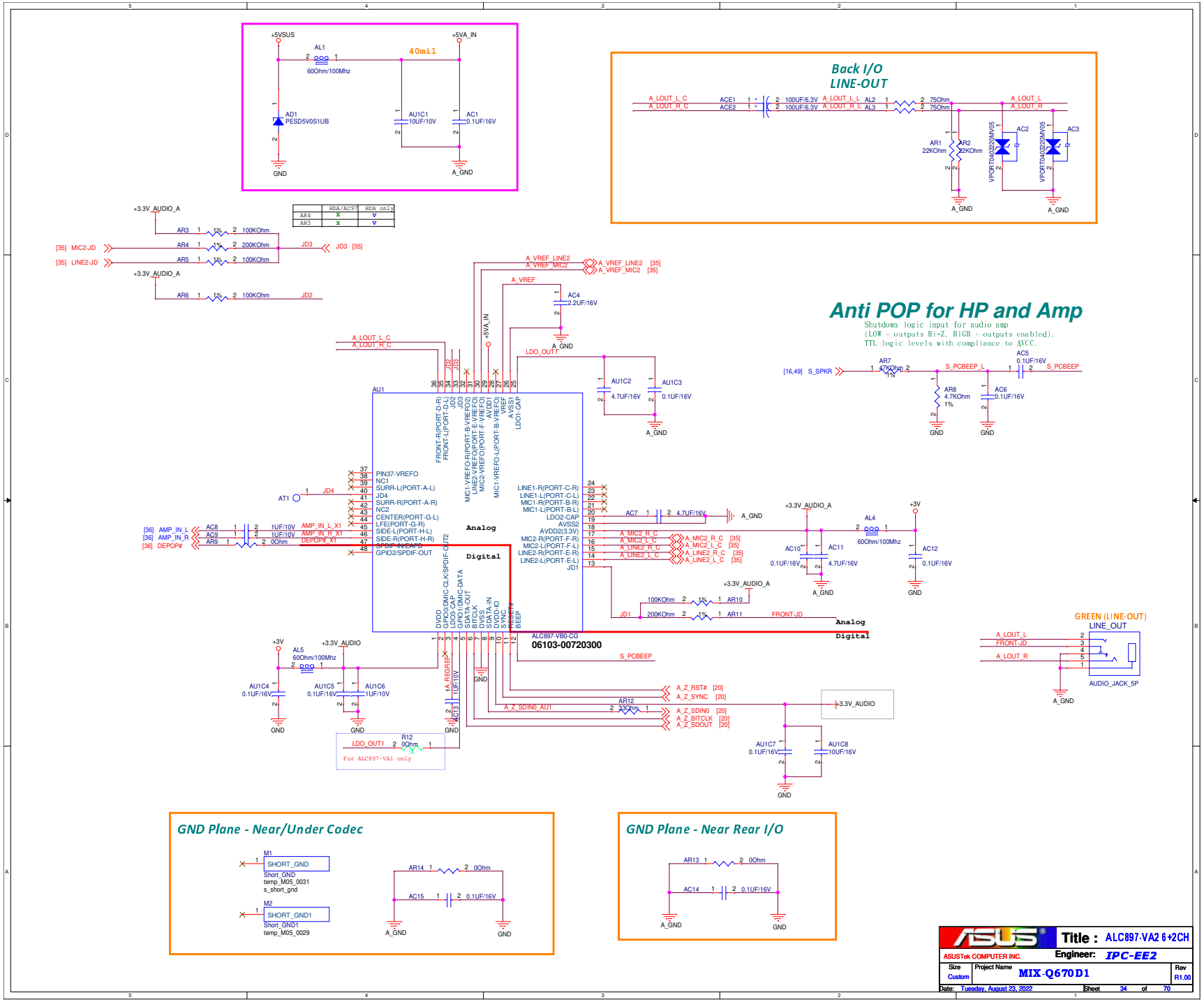
DP-2 (Port D)

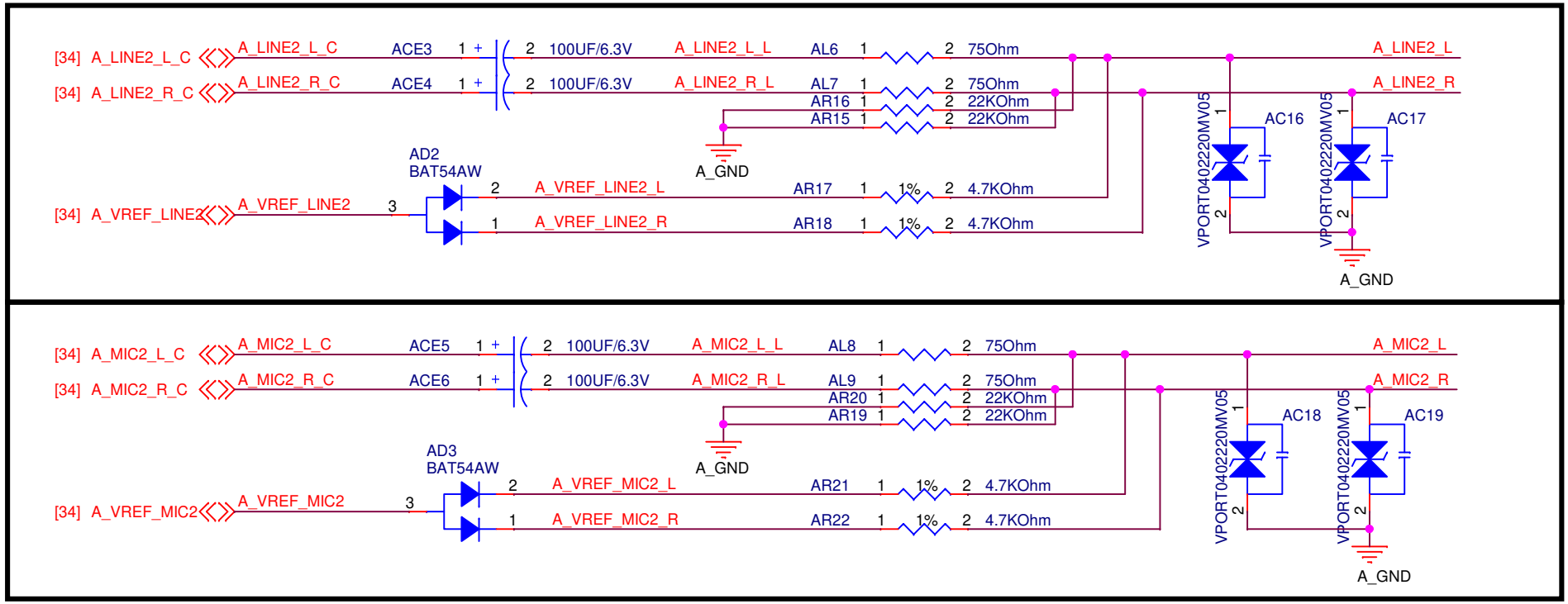


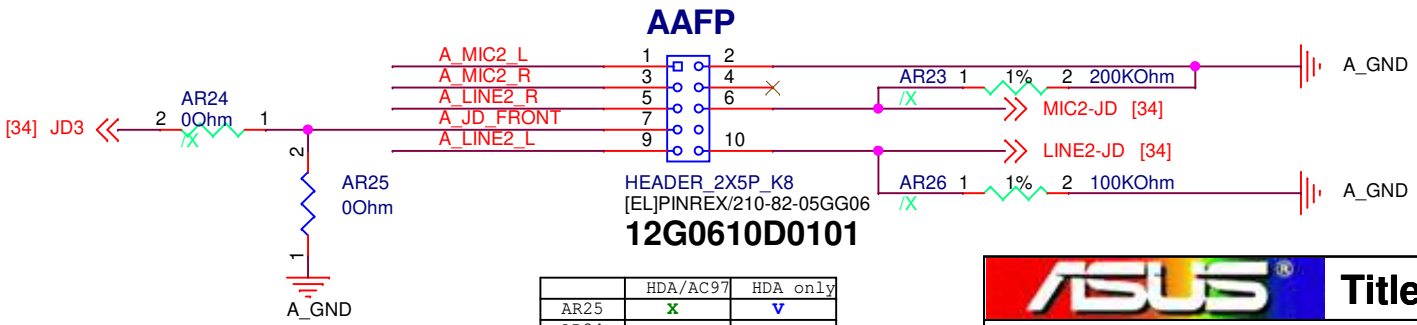
ASUSTeK COMPUTER INC.	Title : DP-2 (Port D)		
	Engineer: IPC-EE2		
Size A2	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 31 of 70		


HDMI 2.0 Re-timer (PS8409A)
17mA
290mA
Power ripple to be < 30mV
place close to pin.30
Place closed to PIN36
For IC Programing.
Place close to pin.7,11
06111-00010500
PS8409AQFN48GTR2-C0
注意CPU/GPU HDMI Signal 排序
EQ_SEL
PRE
I2C_ADDR
HDMI ID
07G028076030
ESD connector
Vertical Type-A
near HDMI2 Pin.P19
HDMI type A receptacle
Pin 1 TMDS Data2+
Pin 2 TMDS Data2 Shield
Pin 3 TMDS Data2−
Pin 4 TMDS Data1+
Pin 5 TMDS Data1 Shield
Pin 6 TMDS Data1−
Pin 7 TMDS Data0+
Pin 8 TMDS Data0 Shield
Pin 9 TMDS Data0−
Pin 10 TMDS Clock+
Pin 11 TMDS Clock Shield
Pin 12 TMDS Clock−
Pin 13 CEC
Pin 14 Reserved (HDMI 1.0–1.3a) Utility/HEAC+ (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)
Pin 15 SCL (I²C serial clock for DDC)
Pin 16 SDA (I²C serial data for DDC)
Pin 17 Ground (for DDC, CEC, ARC, and HEC)
Pin 18 +5 V (min. 0.055 A)[3]
Pin 19 Hot Plug Detect (all versions) HEAC− (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)
Title : HDMI-2 (Port E)
ASUSTeK COMPUTER INC.
Engineer: IPC-EE2
Size A2
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 32 of 70


Close to CH7513
Panel 3.3V/5V/12V jumper
PNL_PWR(1-2)
MINI_JUMPER
MINI JUMPER 2P,2.0MM,F,SMT
PNL_PWR | Panel Voltage Select
1-2 | 3V (Default)
3-4 | 12V
5-6 | 5V
HEADER_2X3P
12006-00180000
[GA]PINREX/222-97-03GBE1
Panel backlight Connector 12V/5V
BKL_PWR(2-3)
MINI_JUMPER
MINI JUMPER 2P,2.0MM,F,SMT
BKL_PWR | INV VOL SEL
1-2 | 12V
2-3 | 5V (Default)
HEADER_1X3P
INV
WAFER_BOX_1X5P
[GA]PINREX/721-81-05TW00
12G08010005B
LVDS Power
CH7511 use +1.8V
CH7513 use +1.2V
LU3
UP0132QDDA
06007-00980100
VOUT = 0.8 (1 + R2/R1)
LVDS_RBIAS
W > 10mils
L < 120mils
LU1A
CH7513A-BF
06106-00940000
LU1B
CH7513A-BF
06106-00940000
LU2
9904AMF
05002-000105MI
[HF]CHRONTEL 64K EMB-H61A 120430
LVDS_EDP_SEL
0 | LVDS
1 | eDP
12017-00210100
eDP/LVDS
WTOB_CON_40P
CN | LVDS | eDP
11 | LVDS0_CLK+ | eDP_AUXP
29 | LVDS0_CLK- | eDP_AUXN
25 | LVDS0_D2+ | eDP_TXOP
23 | LVDS0_D2- | eDP_TXON
19 | LVDS0_D1+ | eDP_TX1P
17 | LVDS0_D1- | eDP_TX1N
13 | LVDS0_D0+ | eDP_TX0P
GPIO request for CH7511 reset;
BIOS: Reset after GPIO (Panel ID) readied
Power Plane | Integrated PU/PD Resistors | During Reset | Immediately after Reset | S4/S5
Suspend | PD 20K | Low | Low | Defined
ASUSTeK COMPUTER INC.
Title : CH7513_eDP/LVDS
Engineer: IPC-EE2
Size C
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 33 of 70


Back I/O
LINE-OUT
Anti POP for HP and Amp
Shutdown logic input for audio amp
(LOW - outputs Hi-Z, HIGH - outputs enabled).
TTL logic levels with compliance to AVCC.
ALC897-VB0-CG
06103-00720300
GREEN (LINE-OUT)
LINE_OUT
AUDIO_JACK_5P
GND Plane - Near/Under Codec
GND Plane - Near Rear I/O
Title : ALC897-VA2 6+2CH
ASUSTek COMPUTER INC.
Engineer: IPC-EE2
Size Custom
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 34 of 70





	HDA/AC97	HDA only
AR25	x	v
AR24	v	x
AR23	v	x
AR26	v	x

ASUSTek COMPUTER INC.

Title : ALC897-VA2 6+2CH

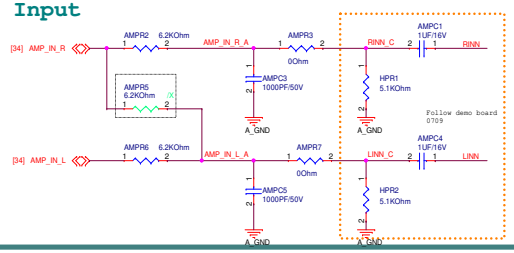
Engineer: IPC-EE2

Size	Project Name	Rev
Custom	MIX-Q670D1	R1.00

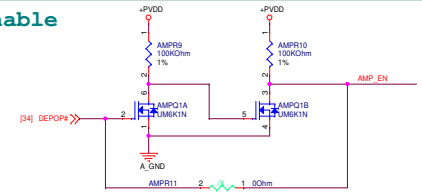
Date: Tuesday, August 23, 2022 Sheet 35 of 70

AMP - EUA2075JIR1 (Only Speaker)

Analog Input

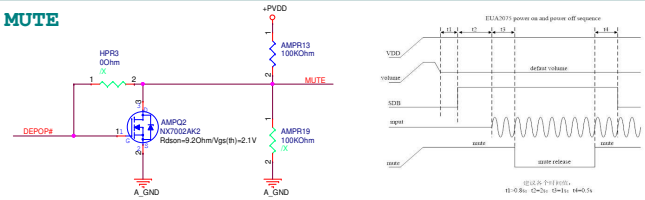


Amp. Enable

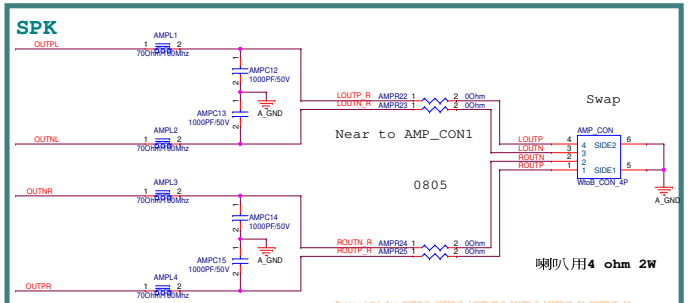


EUA2075 SD PIN 為 High有聲音輸出 , Mute pin 為 Low有聲音輸出

MUTE



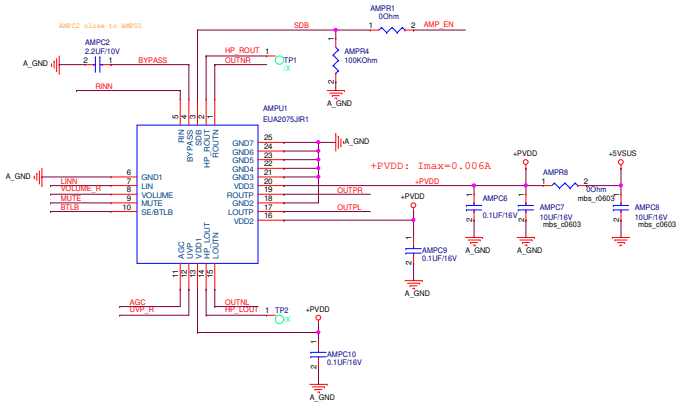
SPK



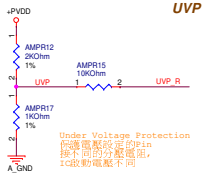
AMPC30, AMPC43, AMPC44, AMPC47, use 1uF is good to EUA2113

Trace width for OUTNR/L,OUTPR/L,LOUTP/N_R,ROUTP_R,LOUTP/N_40,ROUTP/N_40
Speaker
4 ohm : 40mil
8 ohm : 20mil

啲叭用4 ohm 2W



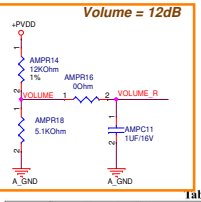
UVP



Under Voltage Protection
低壓電壓啟正的Pin
接不同的分壓電阻,
IC啟動電壓不同

The thresholds can be determined as below:
With the condition: R3 >> R1//R2
V UVP =[1.2-(5.7μA×R3)]×(R1+R2)/R2
Hysteresis=(4.6μA×R3)×(R1+R2)/R2

Volume = 12dB



AGC

Speaker
4 ohm 2W

0.45VDD~0.27VDD: 1.93W

Table 2. AGC Function

AGC Voltage	Output Power
VDD ~ 0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$8\times(VDD\times0.5-VAGC)^2\times0.95/R_L$
0.27VDD ~ GND	P_{OMAX}=2.45W @ 4Ω P_{OMAX}=1.225W @ 8Ω

Auto Gain Control
最大功率的限制對喇叭進行保護
若輸出超過最大功率值
AGC會 自動降低到設定值

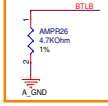
Table 1. DC Volume Control

Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)
1	0.0 - 3.4	2.4 - 0.0	20.0
2	3.4 - 4.8	3.8 - 2.4	19.6
3	4.8 - 6.2	5.2 - 3.8	19.2
4	6.2 - 7.6	6.6 - 5.2	18.8
5	7.6 - 9.0	8.0 - 6.6	18.4
6	9.0 - 10.4	9.4 - 8.0	18.0
7	10.4 - 11.8	10.8 - 9.4	17.6
8	11.8 - 13.2	12.2 - 10.8	17.2
9	13.2 - 14.6	13.6 - 12.2	16.8
10	14.6 - 16.0	15.0 - 13.6	16.4
11	16.0 - 17.4	16.4 - 15.0	16.0
12	17.4 - 18.8	17.8 - 16.4	15.6
13	18.8 - 20.2	19.2 - 17.8	15.2
14	20.2 - 21.6	20.6 - 19.2	14.8
15	21.6 - 23.0	22.0 - 20.6	14.4
16	23.0 - 24.4	23.4 - 22.0	14.0
17	24.4 - 25.8	24.8 - 23.4	13.6
18	25.8 - 27.2	26.2 - 24.8	13.2
19	27.2 - 28.6	27.6 - 26.2	12.8
20	[illegible]	[illegible]	[illegible]
21	30.0 - 31.4	30.4 - 29.0	12.0

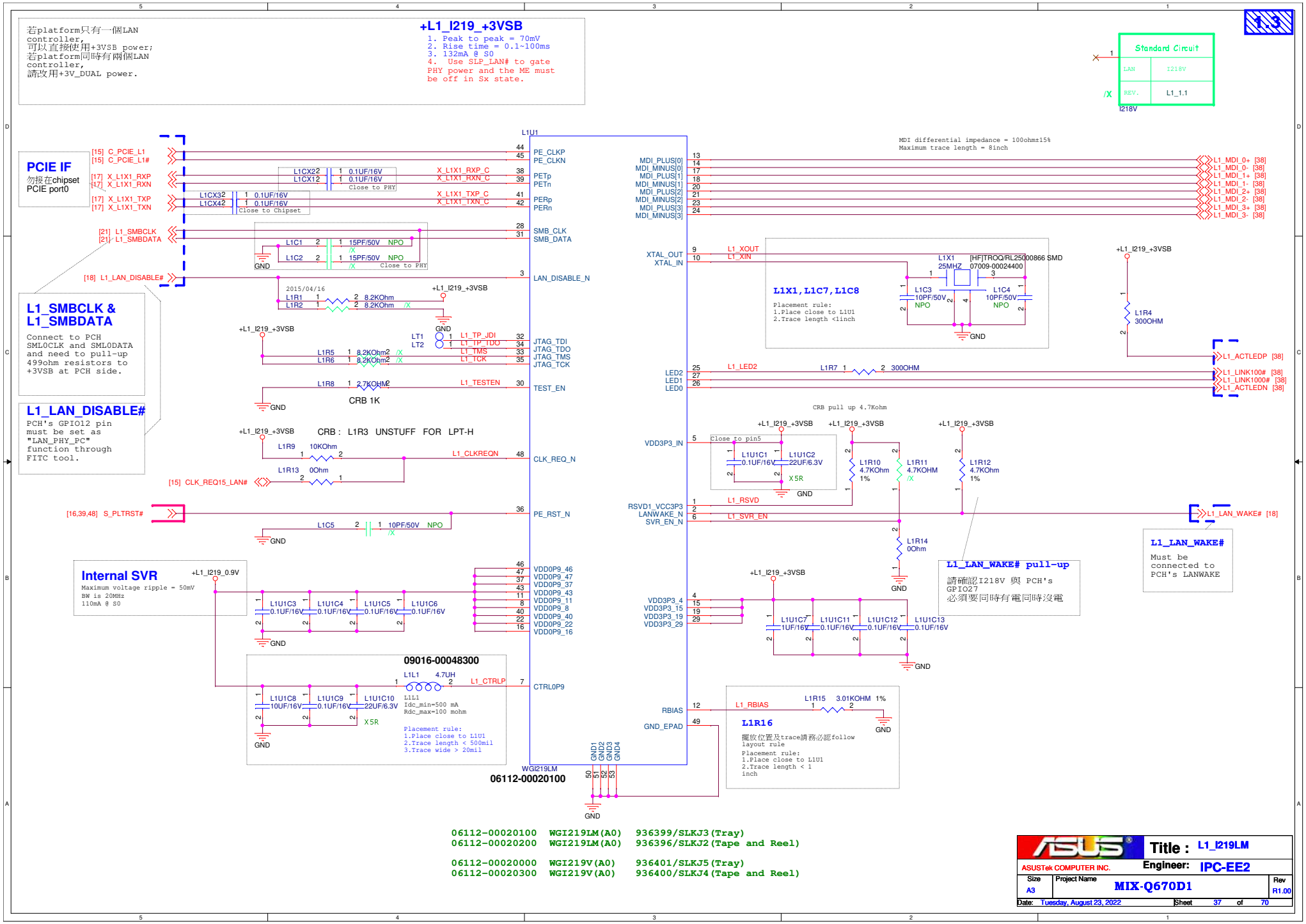
GND Plane - All A_GND

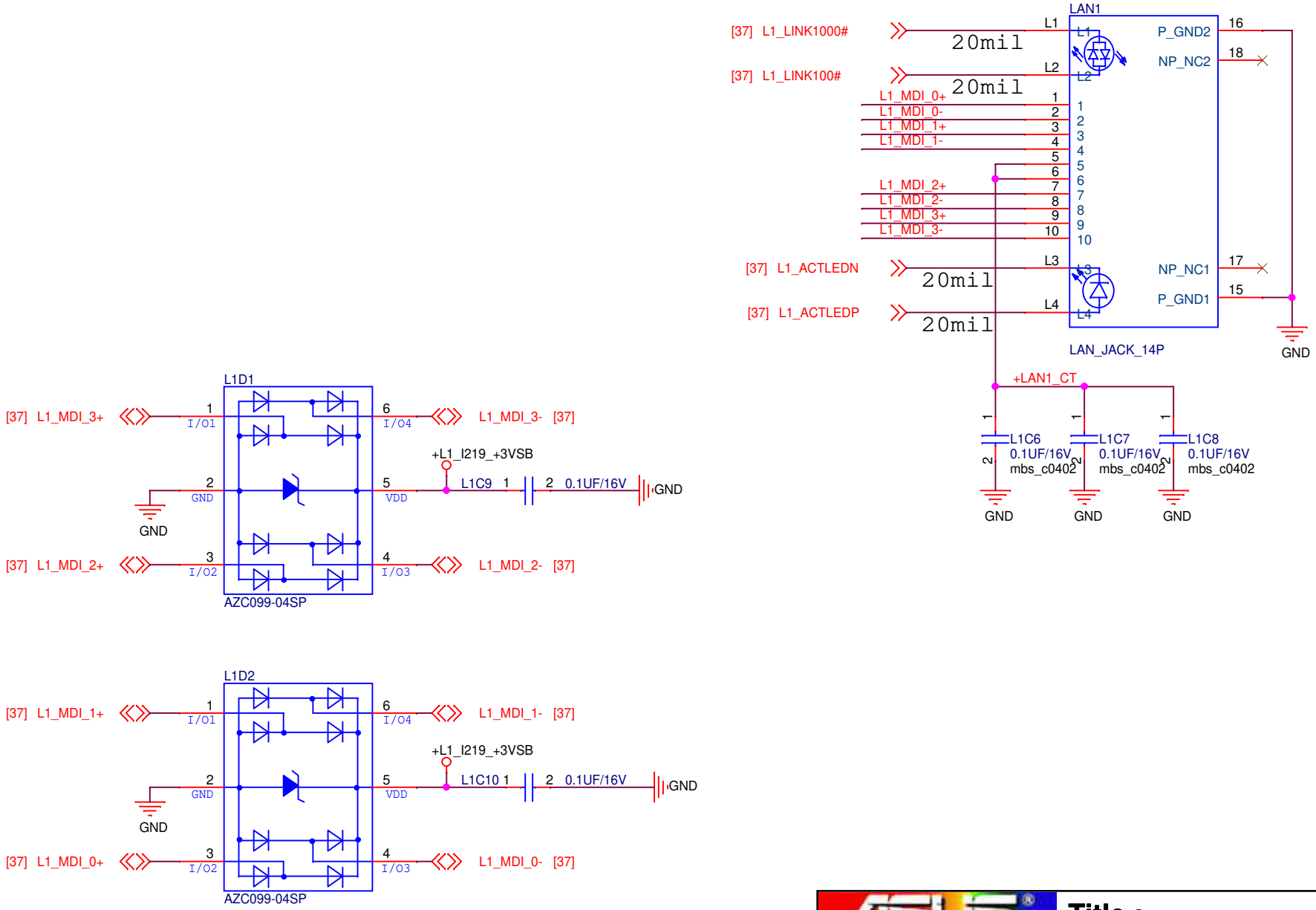
BTLB Only

喇叭與耳機功能切換
SE MODEL :耳機模式 (Hi)
BTL MODEL : 喇叭模式(Low)

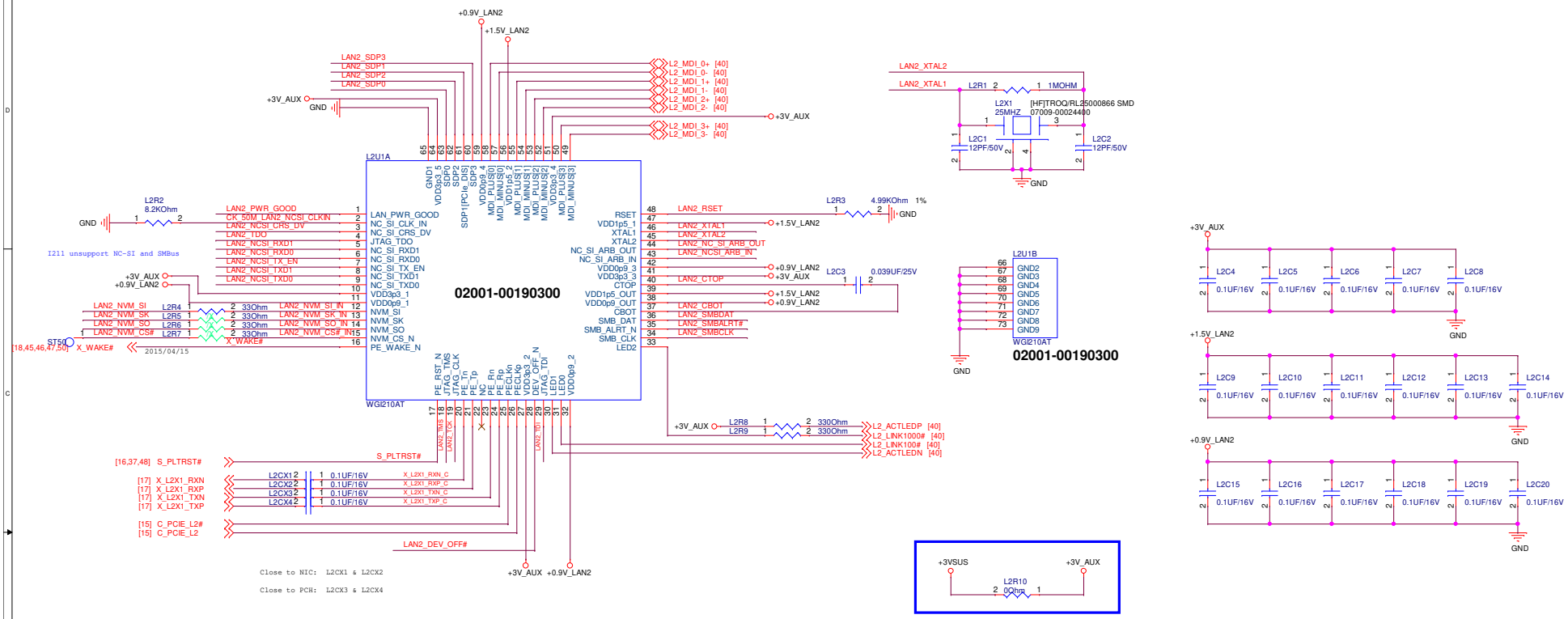


ASUS	Title : AUDIO_EUA2075JIR1	
ASUSTeK COMPUTER INC.	Engineer: IPC-EE2	
Size A2	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 36 of 70	

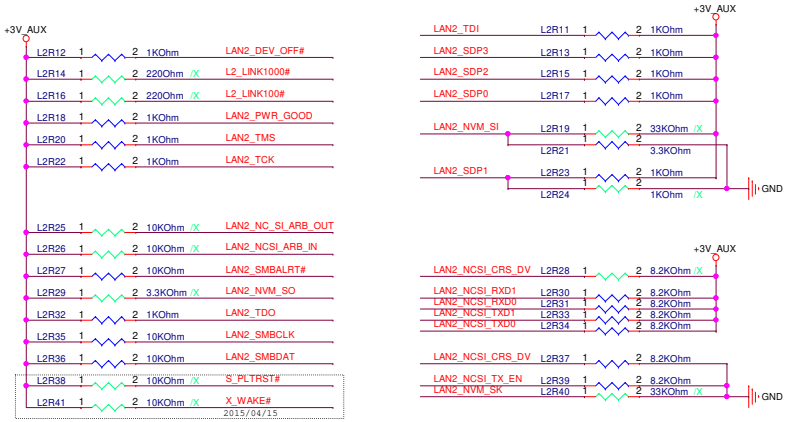

若platform只有一個LAN controller,
可以直接使用+3VSB power;
若platform同時有兩個LAN controller,
請改用+3V_DUAL power.
+L1_I219_+3VSB
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.
Standard Circuit
LAN I218V
REV. L1_1.1
I218V
PCIE IF
勿接在chipset PCIE port0
L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.
L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.
Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0
09016-00048300
L1U1
WGI219LM
06112-00020100
MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch
L1X1,L1C7,L1C8
Placement rule:
1.Place close to L1U1
2.Trace length <1inch
CRB pull up 4.7Kohm
CRB : L1R3 UNSTUFF FOR LPT-H
L1_LAN_WAKE# pull-up
請確認I218V 與 PCH's GPIO27
必須要同時有電同時沒電
L1_LAN_WAKE#
Must be connected to PCH's LANWAKE
L1R16
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch
06112-00020100 WGI219LM(A0) 936399/SLKJ3(Tray)
06112-00020200 WGI219LM(A0) 936396/SLKJ2(Tape and Reel)
06112-00020000 WGI219V(A0) 936401/SLKJ5(Tray)
06112-00020300 WGI219V(A0) 936400/SLKJ4(Tape and Reel)
ASUSTek COMPUTER INC.
Title : L1_I219LM
Engineer: IPC-EE2
Size A3
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 37 of 70



ASUSTek COMPUTER INC.	Title : LAN1_RJ45	
	Engineer: IPC-EE2	
Size A	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 38 of 70	



Follow CRB A.B.



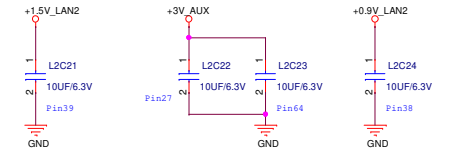
Strapping Options

```
DEV_OFF_N
 I210.28 (DEV_OFF_N)
   1: Exit Device off mode (Default)
   0: Enter Device off mode


AUX_PWR
 I210.28 (DEV_OFF_N)
 I210.60 (SDP3)
   11: Enable AUX power mode (Default)


Security_EN
 I210.12 (NVM_SI)
   1: Enable Flash security
   0: Disable Flash security (Default)


PCIE_DIS_N
 I210.61 (SDP1[PCIe_DIS])
   1: Enable PCIe function (Default)
   0: Disable PCIe function
```

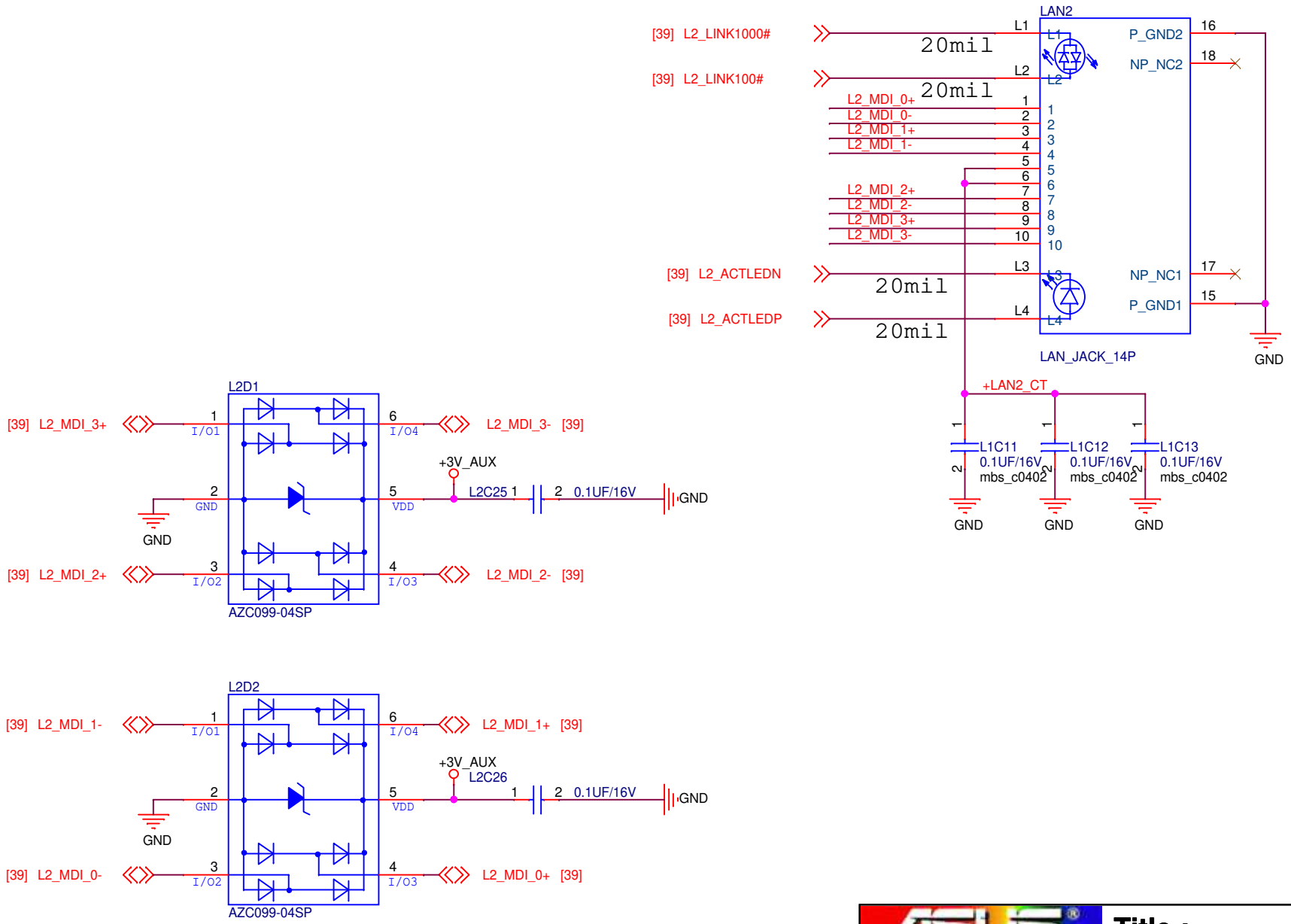


3.4 Voltage Regulator

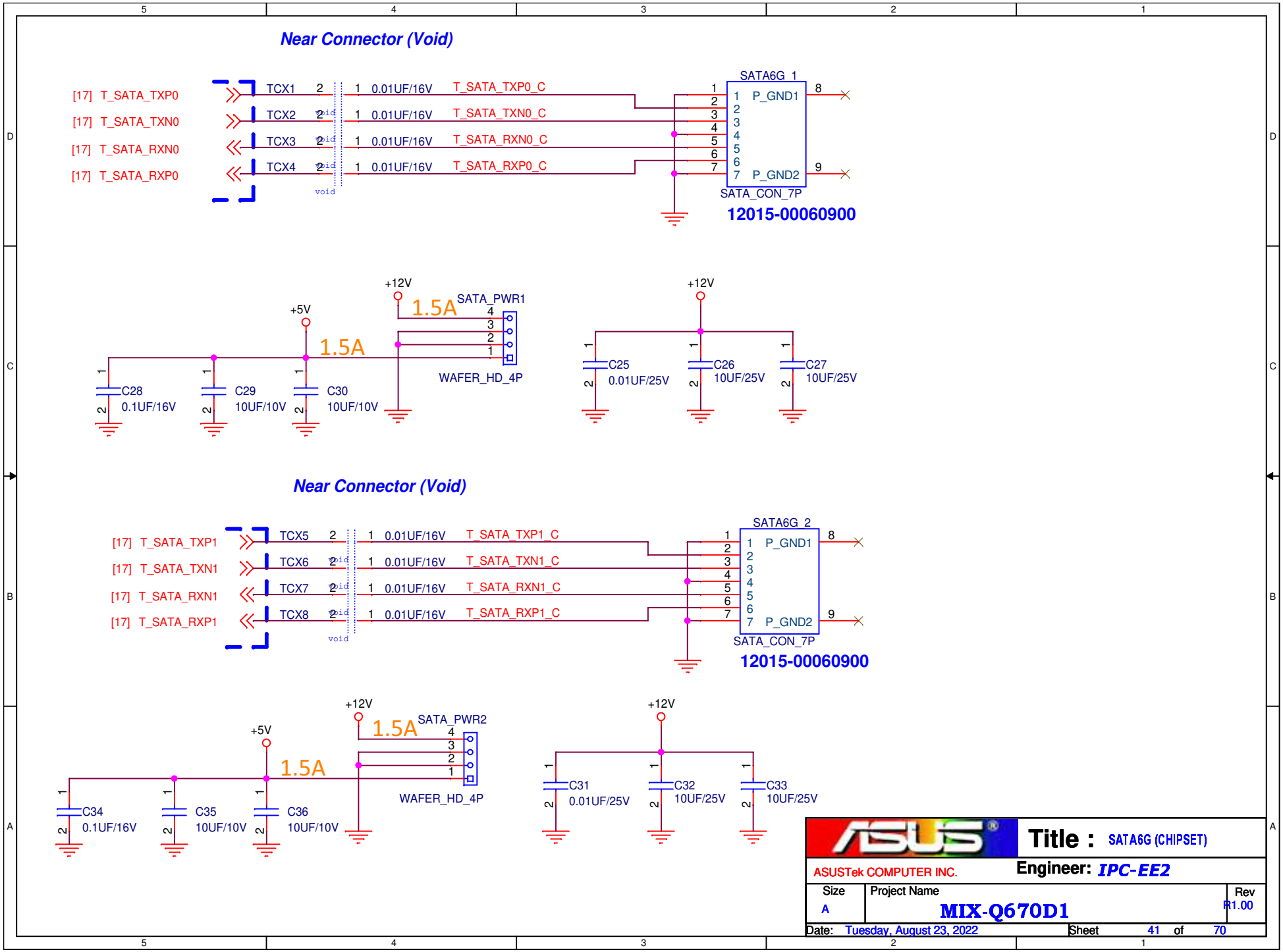
To reduce Bill of Material (BOM) cost, the I211 supports generating the 1.5V and 0.9V power supplies from the 3.3V supply using an on-chip Switching Capacitor Voltage Regulator (SVR) control circuit, which requires only an external capacitor component.

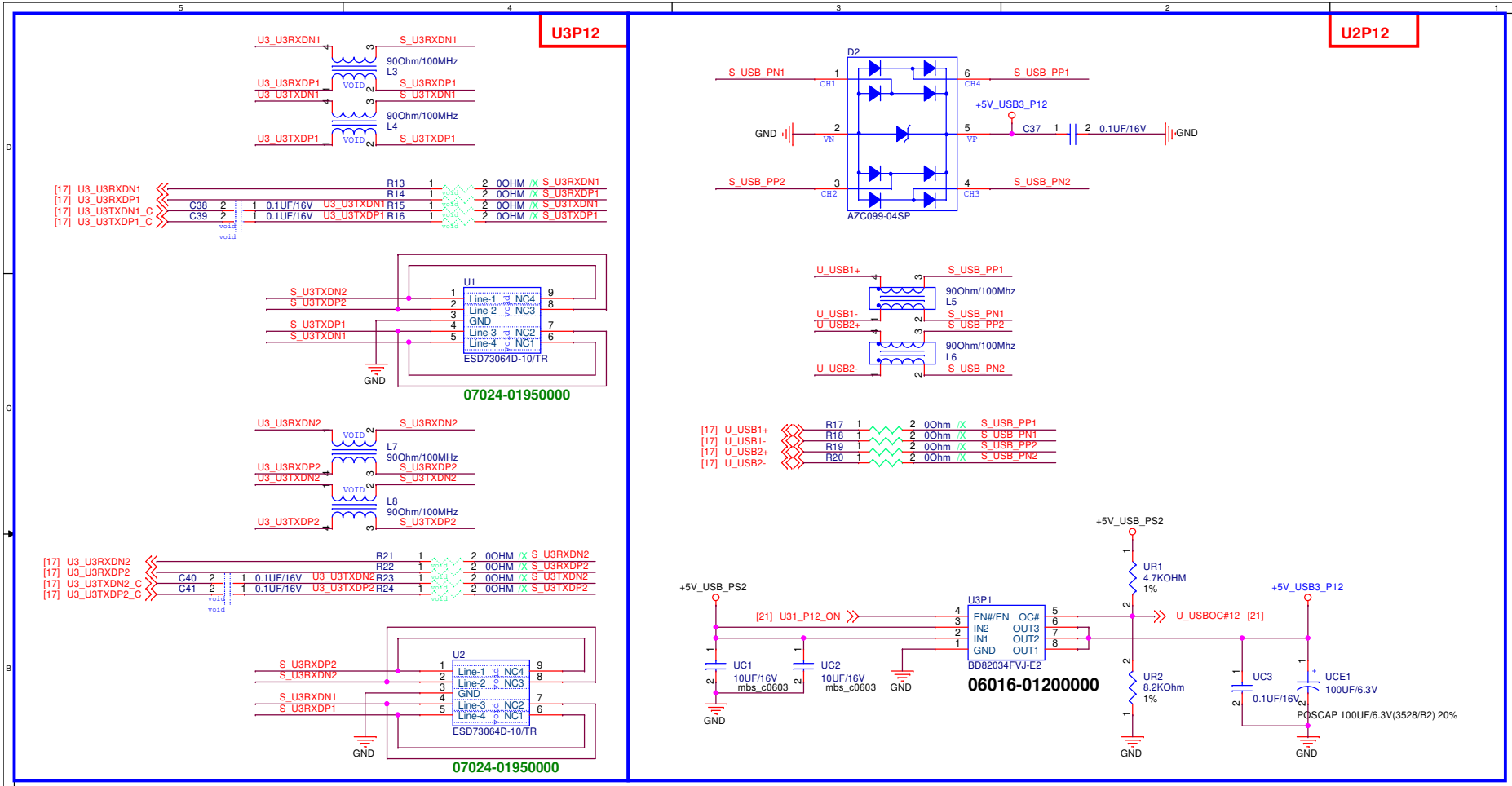
Refer to Section 10.6.4 for more details.

ASUS	Title : LAN2_I210-AT	
ASUSTek COMPUTER INC.	Engineer: IPC-EE2	
Size: Custom	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 39 of 70	



ASUSTek COMPUTER INC.	Title : LAN2_RJ45	
	Engineer: IPC-EE2	
Size A	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 40 of 70	


Near Connector (Void)
[17] T_SATA_TXP0
[17] T_SATA_TXN0
[17] T_SATA_RXN0
[17] T_SATA_RXP0
TCX1
TCX2
TCX3
TCX4
0.01UF/16V
T_SATA_TXP0_C
T_SATA_TXN0_C
T_SATA_RXN0_C
T_SATA_RXP0_C
void
SATA6G_1
P_GND1
P_GND2
SATA_CON_7P
12015-00060900
+12V
+5V
1.5A
SATA_PWR1
WAFER_HD_4P
C28
0.1UF/16V
C29
10UF/10V
C30
10UF/10V
C25
0.01UF/25V
C26
10UF/25V
C27
10UF/25V
Near Connector (Void)
[17] T_SATA_TXP1
[17] T_SATA_TXN1
[17] T_SATA_RXN1
[17] T_SATA_RXP1
TCX5
TCX6
TCX7
TCX8
T_SATA_TXP1_C
T_SATA_TXN1_C
T_SATA_RXN1_C
T_SATA_RXP1_C
SATA6G_2
SATA_PWR2
C34
0.1UF/16V
C35
10UF/10V
C36
10UF/10V
C31
0.01UF/25V
C32
10UF/25V
C33
10UF/25V
ASUSTek COMPUTER INC.
Title : SATA6G (CHIPSET)
Engineer: IPC-EE2
Size A
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 41 of 70



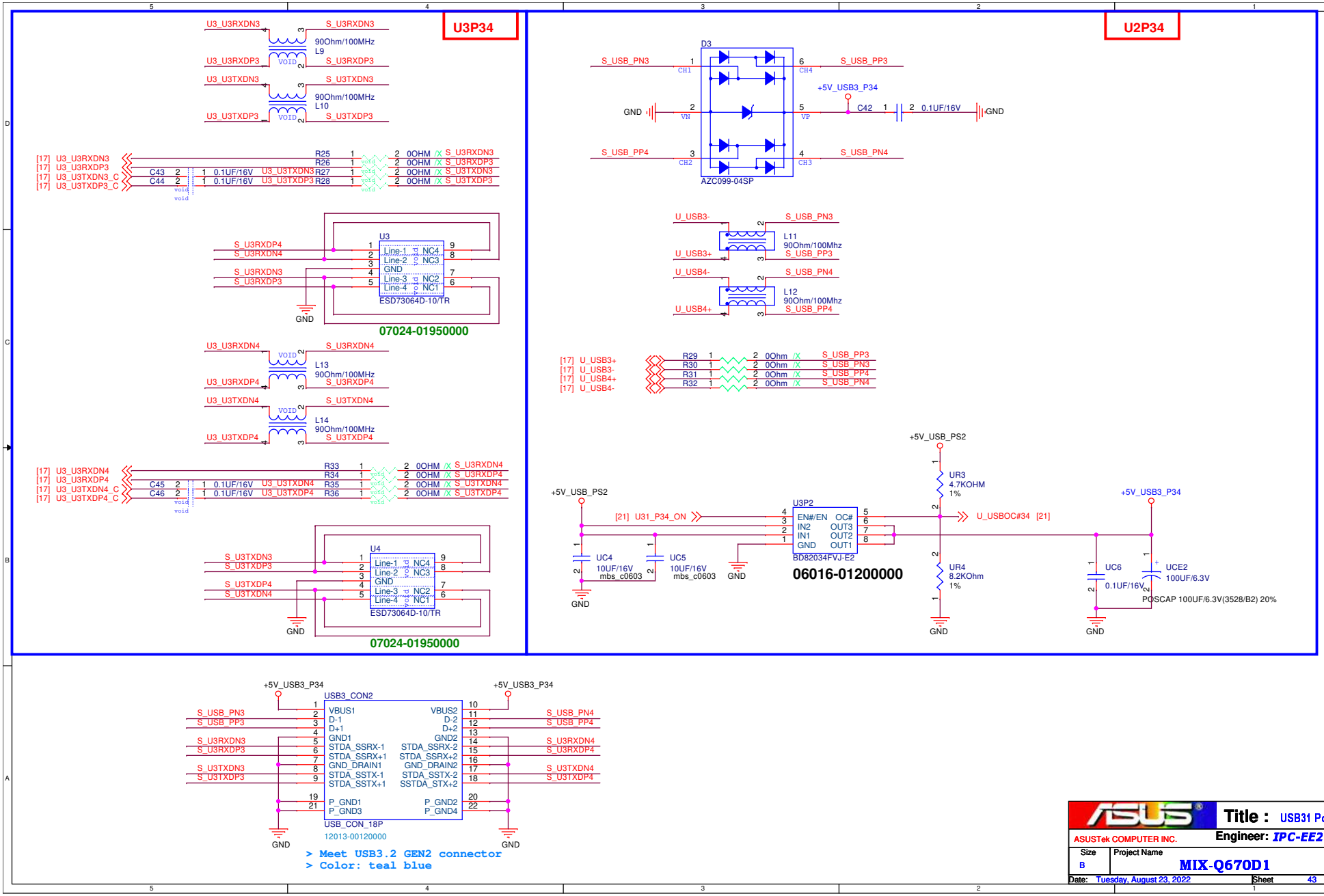
ASUSTek COMPUTER INC.

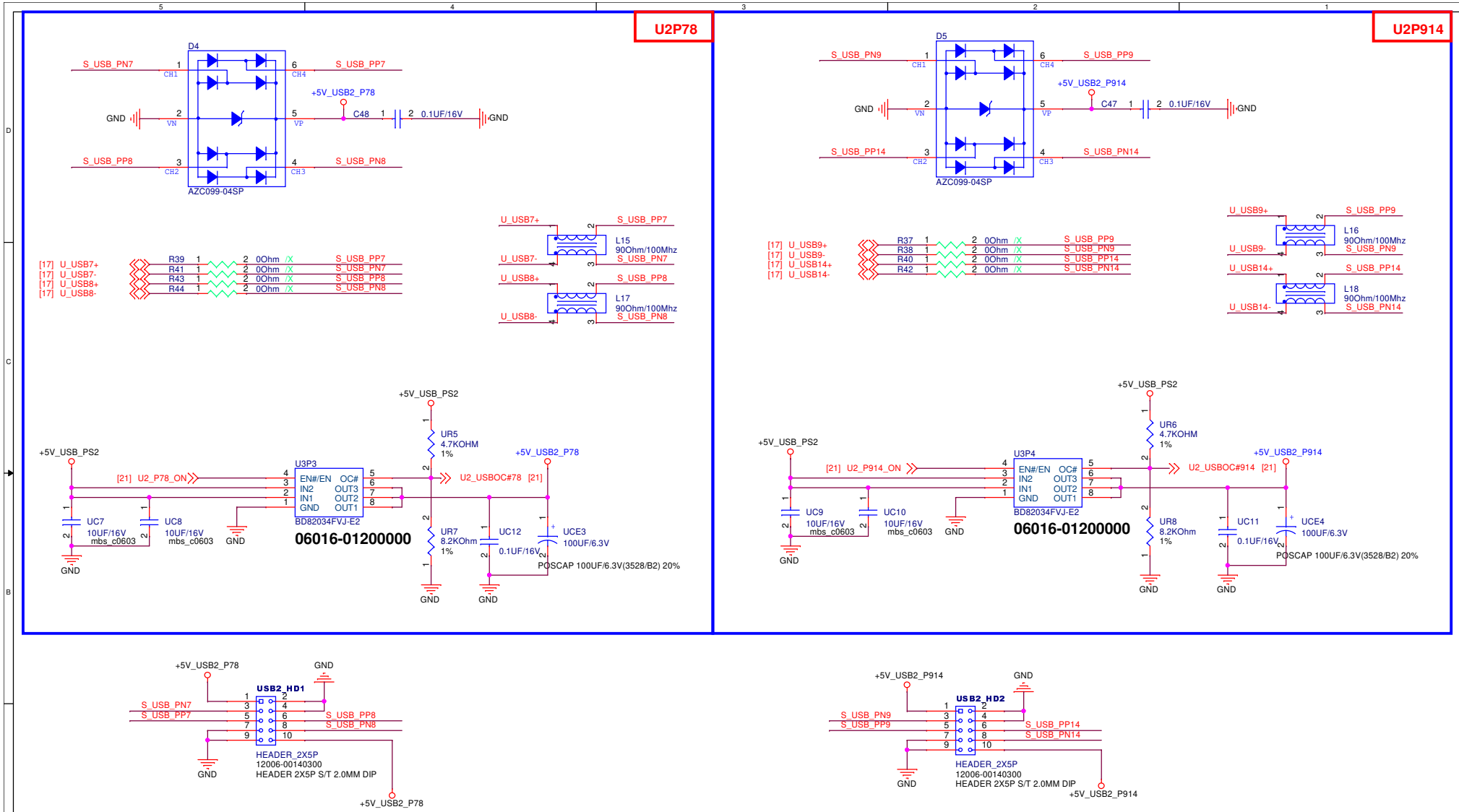
Title : USB31 Port 1,2

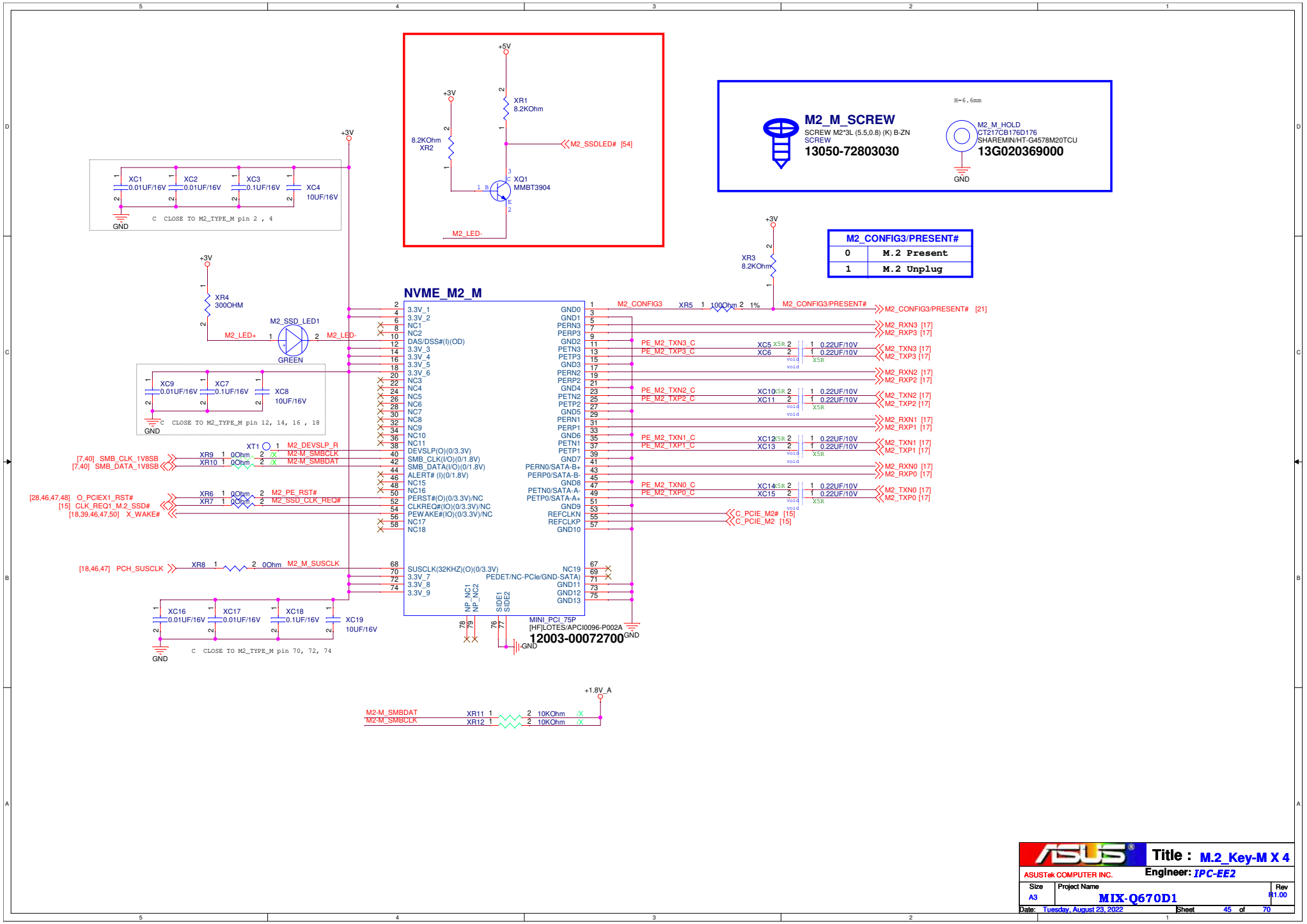
Engineer: IPC-EE2

Size	Project Name	Rev
B	MIX-Q670D1	R1.00

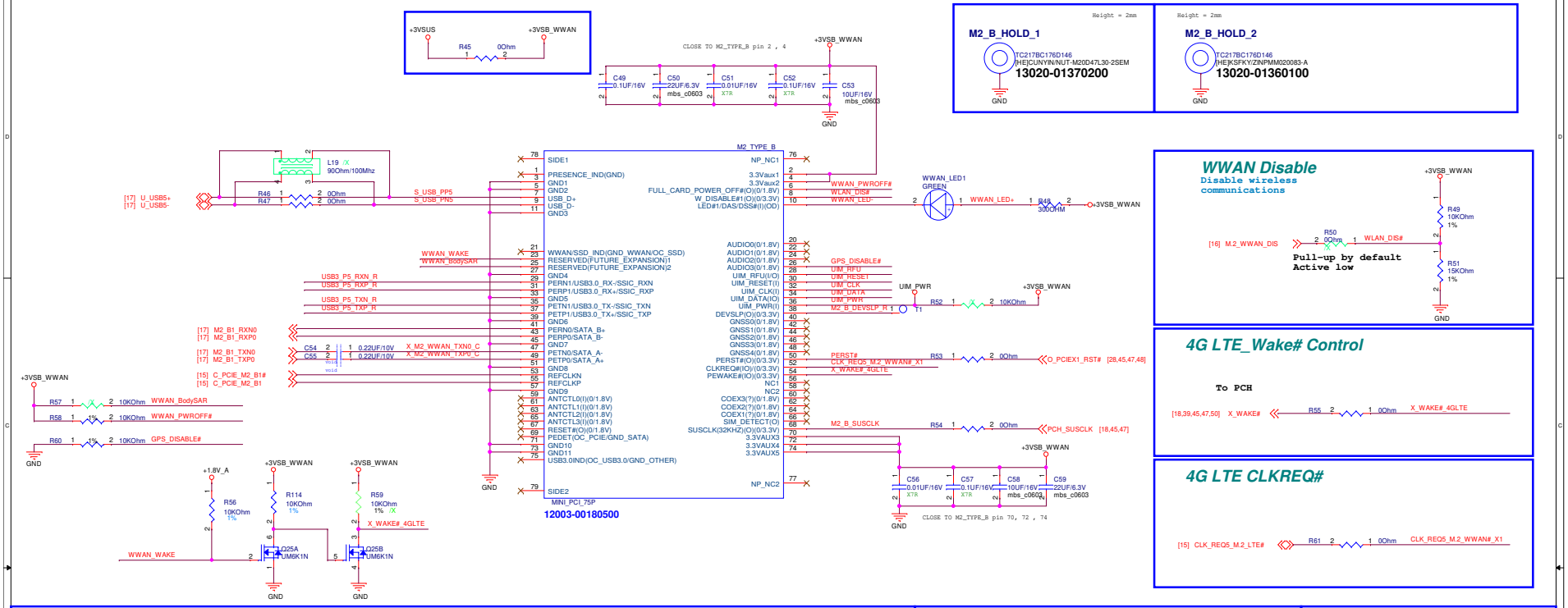
Date: Tuesday, August 23, 2022 Sheet 42 of 70


U3P34
U3_U3RXDN3
S_U3RXDN3
90Ohm/100MHz
L9
U3_U3RXDP3
S_U3RXDP3
U3_U3TXDN3
S_U3TXDN3
90Ohm/100MHz
L10
U3_U3TXDP3
S_U3TXDP3
[17] U3_U3RXDN3
[17] U3_U3RXDP3
[17] U3_U3TXDN3_C
[17] U3_U3TXDP3_C
C43 0.1UF/16V U3_U3TXDN3
C44 0.1UF/16V U3_U3TXDP3
R25 0OHM S_U3RXDN3
R26 0OHM S_U3RXDP3
R27 0OHM S_U3TXDN3
R28 0OHM S_U3TXDP3
U3
S_U3RXDP4
S_U3RXDN4
S_U3RXDN3
S_U3RXDP3
GND
ESD73064D-10/TR
07024-01950000
U3_U3RXDN4
S_U3RXDN4
L13
90Ohm/100MHz
U3_U3RXDP4
S_U3RXDP4
U3_U3TXDN4
S_U3TXDN4
L14
90Ohm/100MHz
U3_U3TXDP4
S_U3TXDP4
[17] U3_U3RXDN4
[17] U3_U3RXDP4
[17] U3_U3TXDN4_C
[17] U3_U3TXDP4_C
C45 0.1UF/16V U3_U3TXDN4
C46 0.1UF/16V U3_U3TXDP4
R33 0OHM S_U3RXDN4
R34 0OHM S_U3RXDP4
R35 0OHM S_U3TXDN4
R36 0OHM S_U3TXDP4
U4
S_U3TXDN3
S_U3TXDP3
S_U3TXDP4
S_U3TXDN4
GND
ESD73064D-10/TR
07024-01950000
U2P34
D3
S_USB_PN3
S_USB_PP3
GND
S_USB_PP4
S_USB_PN4
+5V_USB3_P34
C42 0.1UF/16V
AZC099-04SP
U_USB3-
U_USB3+
L11
90Ohm/100Mhz
S_USB_PP3
U_USB4-
U_USB4+
L12
90Ohm/100Mhz
S_USB_PP4
[17] U_USB3+
[17] U_USB3-
[17] U_USB4+
[17] U_USB4-
R29 0Ohm S_USB_PP3
R30 0Ohm S_USB_PN3
R31 0Ohm S_USB_PP4
R32 0Ohm S_USB_PN4
+5V_USB_PS2
UR3
4.7KOHM
1%
[21] U31_P34_ON
U3P2
EN#/EN
IN2
IN1
GND
OC#
OUT3
OUT2
OUT1
BD82034FVJ-E2
06016-01200000
U_USBOC#34 [21]
+5V_USB3_P34
UC4
10UF/16V
mbs_c0603
UC5
10UF/16V
mbs_c0603
UR4
8.2KOhm
1%
UC6
0.1UF/16V
UCE2
100UF/6.3V
POSCAP 100UF/6.3V(3528/B2) 20%
+5V_USB3_P34
USB3_CON2
VBUS1
D-1
D+1
GND1
STDA_SSRX-1
STDA_SSRX+1
GND_DRAIN1
STDA_SSTX-1
STDA_SSTX+1
P_GND1
P_GND3
VBUS2
D-2
D+2
GND2
STDA_SSRX-2
STDA_SSRX+2
GND_DRAIN2
STDA_SSTX-2
SSTDA_STX+2
P_GND2
P_GND4
USB_CON_18P
12013-00120000
S_USB_PN3
S_USB_PP3
S_U3RXDN3
S_U3RXDP3
S_U3TXDN3
S_U3TXDP3
S_USB_PN4
S_USB_PP4
S_U3RXDN4
S_U3RXDP4
S_U3TXDN4
S_U3TXDP4
GND
> Meet USB3.2 GEN2 connector
> Color: teal blue
ASUS
ASUSTek COMPUTER INC.
Title : USB31 Port 3,4
Engineer: IPC-EE2
Size B
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 43 of 70


U2P78
D4
S_USB_PN7
S_USB_PP7
GND
+5V_USB2_P78
C48
0.1UF/16V
S_USB_PP8
S_USB_PN8
AZC099-04SP
[17] U_USB7+
[17] U_USB7-
[17] U_USB8+
[17] U_USB8-
R39 0Ohm
R41 0Ohm
R43 0Ohm
R44 0Ohm
U_USB7+
U_USB7-
U_USB8+
U_USB8-
L15
90Ohm/100Mhz
L17
90Ohm/100Mhz
+5V_USB_PS2
UR5
4.7KOHM
1%
U3P3
EN#/EN
IN2
IN1
GND
OC#
OUT3
OUT2
OUT1
BD82034FVJ-E2
06016-01200000
[21] U2_P78_ON
U2_USBOC#78 [21]
UC7
10UF/16V
mbs_c0603
UC8
10UF/16V
mbs_c0603
UR7
8.2KOhm
1%
UC12
0.1UF/16V
UCE3
100UF/6.3V
POSCAP 100UF/6.3V(3528/B2) 20%
U2P914
D5
S_USB_PN9
S_USB_PP9
+5V_USB2_P914
C47
0.1UF/16V
S_USB_PP14
S_USB_PN14
AZC099-04SP
[17] U_USB9+
[17] U_USB9-
[17] U_USB14+
[17] U_USB14-
R37 0Ohm
R38 0Ohm
R40 0Ohm
R42 0Ohm
L16
90Ohm/100Mhz
L18
90Ohm/100Mhz
U3P4
06016-01200000
[21] U2_P914_ON
U2_USBOC#914 [21]
UR6
4.7KOHM
1%
UR8
8.2Ohm
1%
UC11
0.1UF/16V
UCE4
100UF/6.3V
USB2_HD1
HEADER_2X5P
12006-00140300
HEADER 2X5P S/T 2.0MM DIP
USB2_HD2
ASUSTek COMPUTER INC.
Title : USB2 Port 7-9,14
Engineer: IPC-EE2
Size B
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
Sheet 44 of 70



ASUSTek COMPUTER INC.	Title : M.2_Key-M X 4
	Engineer: IPC-EE2
Size A3	Project Name MIX-Q670D1
	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 45 of 70



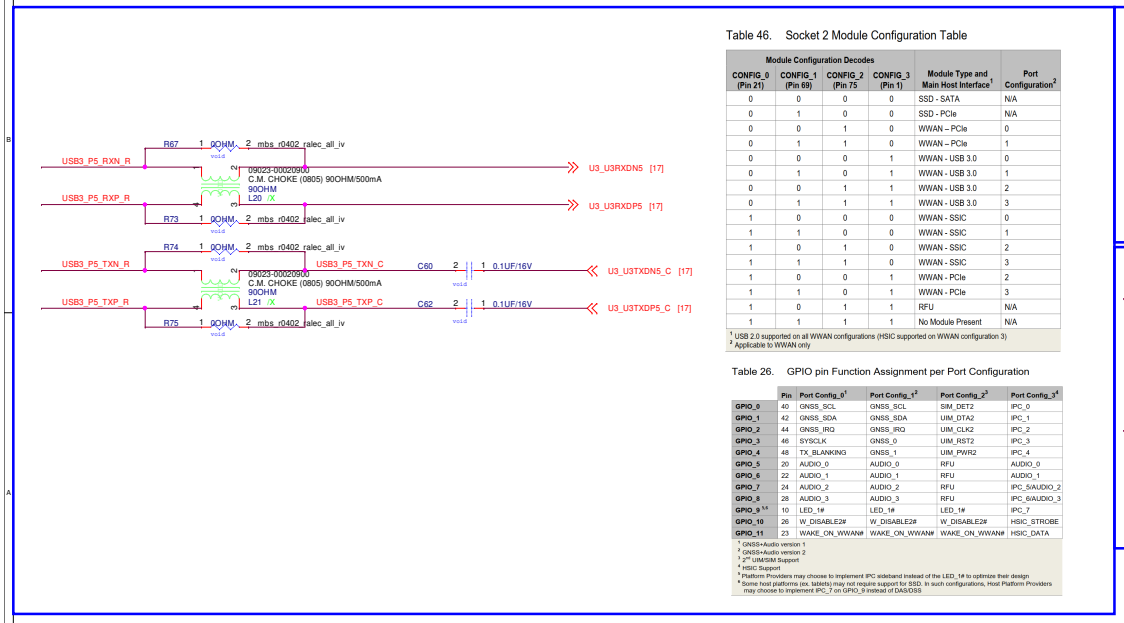


Table 46. Socket 2 Module Configuration Table

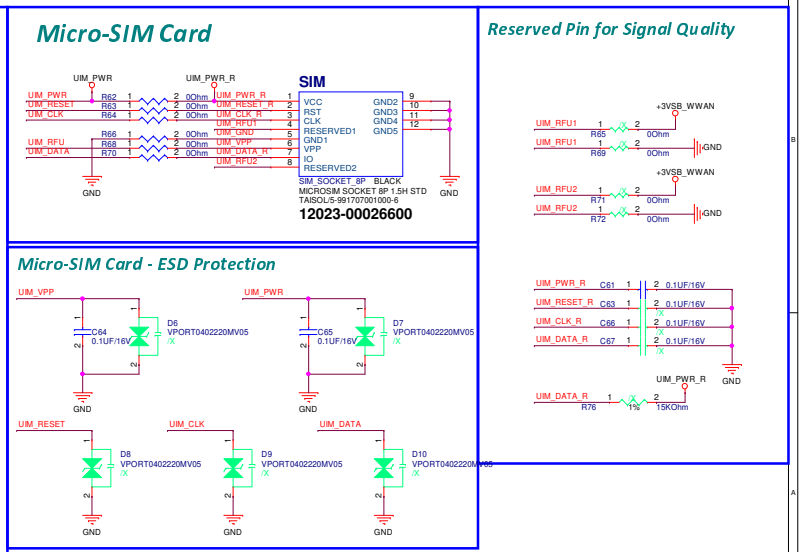
Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
1	0	1	1	RFU	N/A
1	1	1	1	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
[2] Applicable to WWAN only

Table 26. GPIO pin Function Assignment per Port Configuration

	Pin	Port Config_0[1]	Port Config_1[2]	Port Config_2[3]	Port Config_3[4]
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2	IPC_1
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3
GPIO_9 [5,6]	10	LED_1#	LED_1#	LED_1#	IPC_7
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA

[1] GNSS+Audio version 1
[2] GNSS+Audio version 2
[3] 2nd UIM/SIM Support
[4] HSIC Support
[5] Platform Providers may choose to implement IPC sideband instead of the LED_1# to optimize their design
[6] Some host platforms (ex. tablets) may not require support for SSD. In such configurations, Host Platform Providers may choose to implement IPC_7 on GPIO_9 instead of DAS/DSS



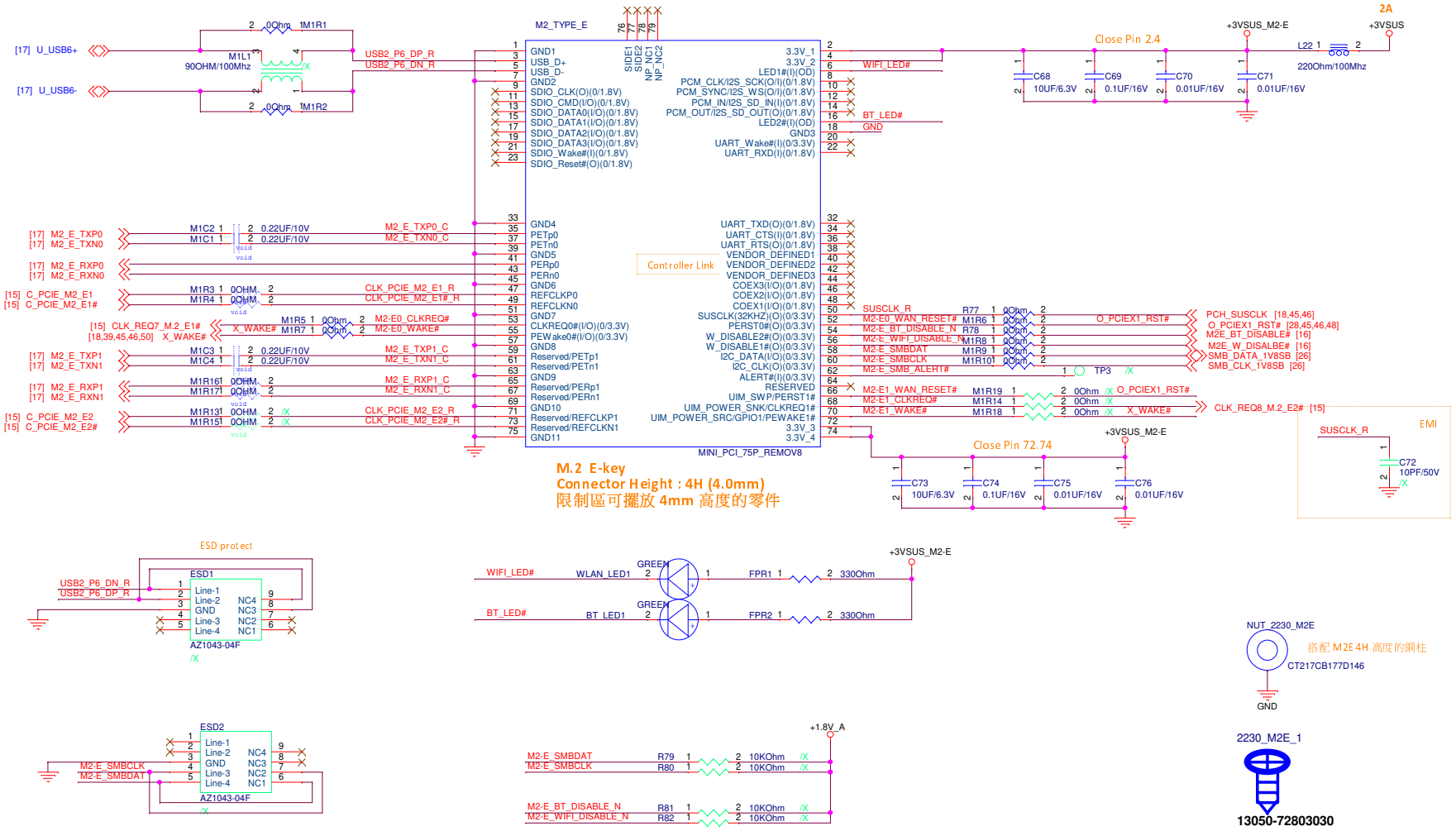
ASUSTeK COMPUTER INC.

Title : M.2_Key-B_LTE

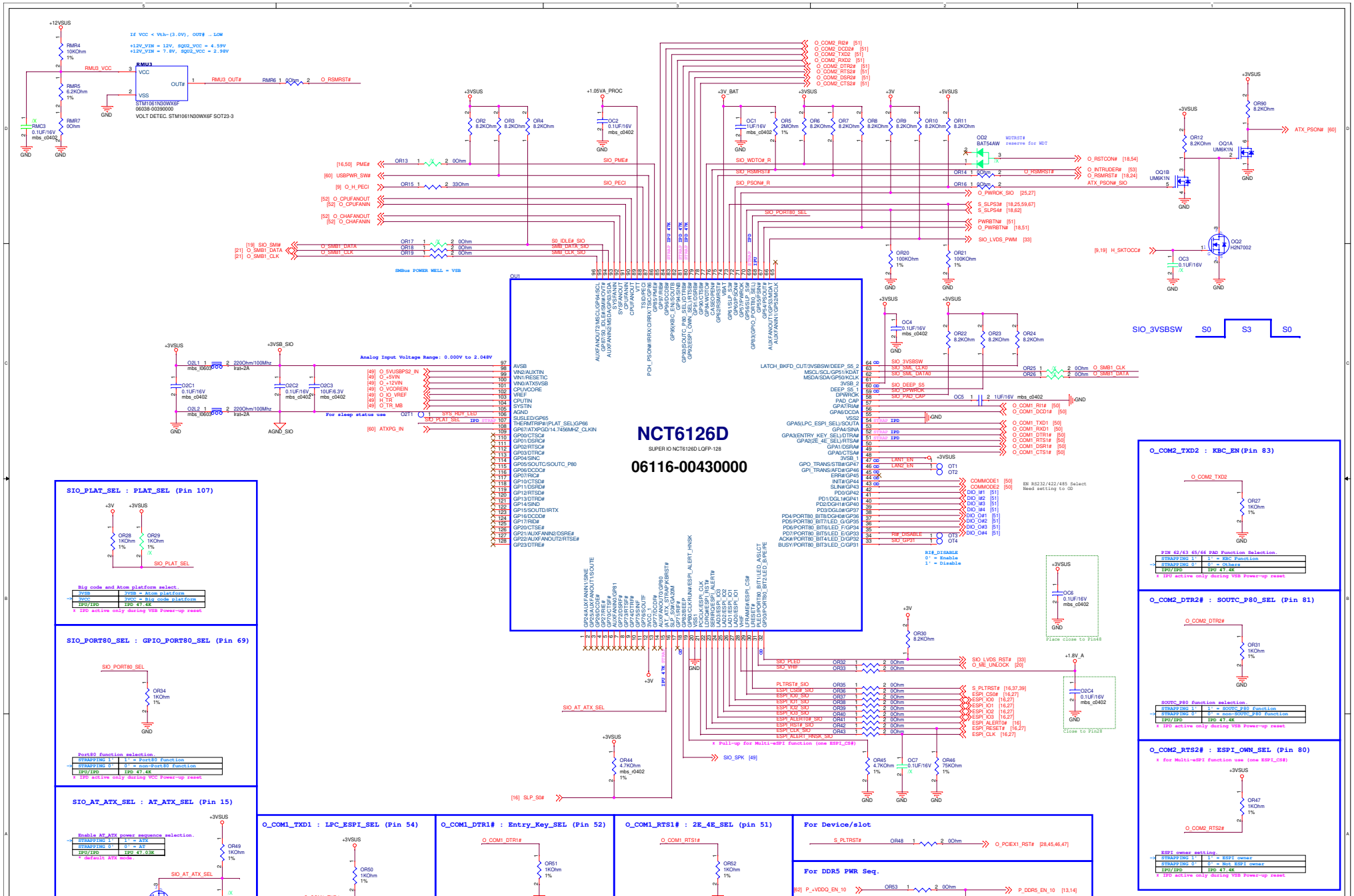
Engineer: IPC-EE2

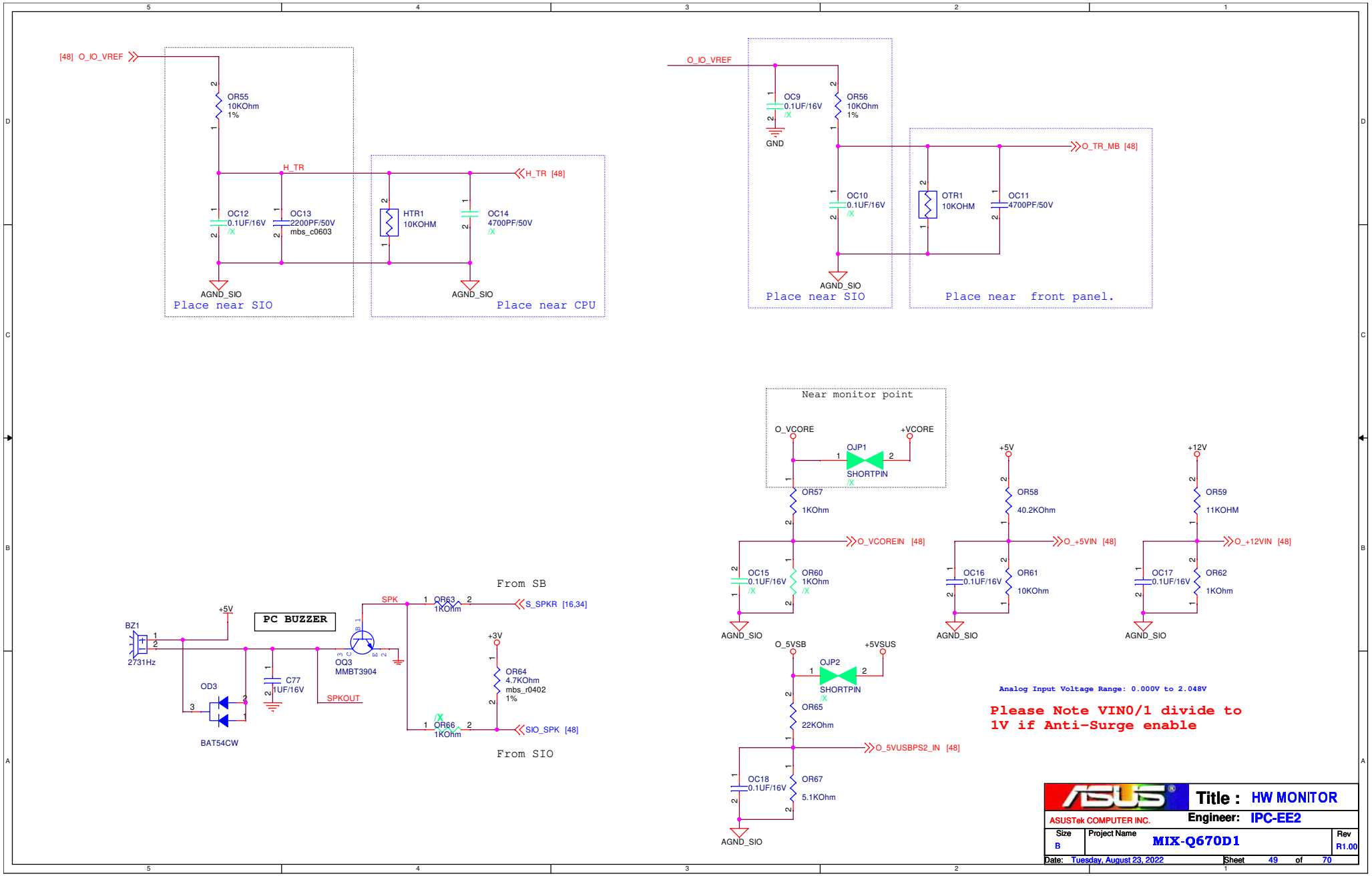
Size	Project Name	Rev
C	MIX-Q670D1	R1.00

Date: Tuesday, August 23, 2022 Sheet 46 of 70



ASUSTek COMPUTER INC.	Title : M.2 E KEY	Engineer: IPC-EE2
Size A3	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 47 of 70	


NCT6126D
SUPER IO NCT6126D LQFP-128
06116-00430000
SIO_PLAT_SEL : PLAT_SEL (Pin 107)
SIO_PORT80_SEL : GPIO_PORT80_SEL (Pin 69)
SIO_AT_ATX_SEL : AT_ATX_SEL (Pin 15)
O_COM1_TXD1 : LPC_ESPI_SEL (Pin 54)
O_COM1_DTR1# : Entry_Key_SEL (Pin 52)
O_COM1_RTS1# : 2E_4E_SEL (pin 51)
For Device/slot
For DDR5 PWR Seq.
O_COM2_TXD2 : KBC_EN(Pin 83)
O_COM2_DTR2# : SOUTC_P80_SEL (Pin 81)
O_COM2_RTS2# : ESPI_OWN_SEL (Pin 80)
Title : SIO NCT6126D
Engineer: IPC-EE2
ASUSTeK COMPUTER INC.
M/X-Q670D1
Date: Tuesday, August 23, 2022
Sheet 48 of 70


[48] O_IO_VREF
OR55
10KOhm
1%
H_TR
H_TR [48]
OC12
0.1UF/16V
/X
OC13
2200PF/50V
mbs_c0603
HTR1
10KOHM
OC14
4700PF/50V
/X
AGND_SIO
Place near SIO
Place near CPU
O_IO_VREF
OC9
0.1UF/16V
/X
GND
OR56
10KOhm
1%
O_TR_MB [48]
OC10
0.1UF/16V
/X
OTR1
10KOHM
OC11
4700PF/50V
Place near SIO
Place near front panel.
Near monitor point
O_VCORE
+VCORE
OJP1
SHORTPIN
/X
OR57
1KOhm
O_VCOREIN [48]
OC15
0.1UF/16V
/X
OR60
1KOhm
/X
+5V
OR58
40.2KOhm
O_+5VIN [48]
OC16
0.1UF/16V
OR61
10KOhm
+12V
OR59
11KOHM
O_+12VIN [48]
OC17
0.1UF/16V
OR62
1KOhm
O_5VSB
+5VSUS
OJP2
SHORTPIN
/X
OR65
22KOhm
O_5VUSBPS2_IN [48]
OC18
0.1UF/16V
OR67
5.1KOhm
Analog Input Voltage Range: 0.000V to 2.048V
Please Note VIN0/1 divide to
1V if Anti-Surge enable
PC BUZZER
BZ1
2731Hz
+5V
OD3
BAT54CW
C77
1UF/16V
SPKOUT
SPK
OQ3
MMBT3904
From SB
OR63
1KOhm
S_SPKR [16,34]
+3V
OR64
4.7KOhm
mbs_r0402
1%
/X
OR66
1KOhm
SIO_SPK [48]
From SIO
ASUS
Title : HW MONITOR
ASUSTek COMPUTER INC.
Engineer: IPC-EE2
Size
B
Project Name
MIX-Q670D1
Rev
R1.00
Date: Tuesday, August 23, 2022
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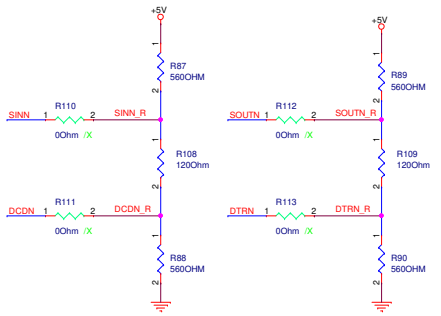
RS422/RS485 Terminator

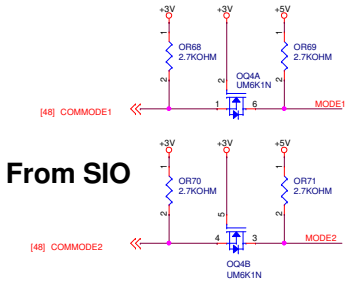


R110,R111,R112,R113 all off -->RS232
R110,R111,R112,R113 all on -->RS485/RS422 with terminator

Mode Selection			
SD	MODE_1	MODE_2	MODE
0	0	0	RS-422
0	0	1	RS-232
0	1	0	RS-485 (Driver Half Duplex)
0	1	1	RS-485 (Receiver Half Duplex)
1	X	X	Shutdown MODE

Note:

Mode_1 and Mode_2 pin. Internal pull high≒ 625KΩ.
As the current is very small (≒15μA), please use the hardware strapping or GPIO (BIOS) to select the modes.



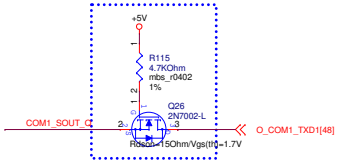
(VDD = +5.0V ± 5%)

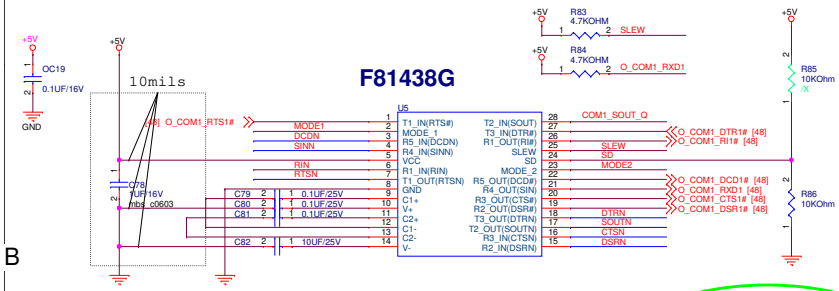
Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Current (RS-232)	No Load, MODE = 01.		2	30	mA
Supply Current (RS-485)	No Load, MODE = 10, 11.		2		mA
Supply Current (RS-422)	MODE = 00.		2		mA
Operating Temperature *	Symbol: T	-40		85	◦ C

(VDD = +5.0V ± 5%)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (MODE, SLEW) 1, 2, 23, 24, 25, 27, 28						
Logic Input Voltage HIGH	V_{IL}	2.4			V	VDD = 5.0 V
Logic Input Voltage LOW	-			0.8	V	
Logic Input Pull-up Current	-			±15	μA	
Driver Input Pull High Current	I_{IT}			±15	μA	

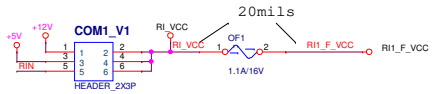
Isolation for H/W Strapping

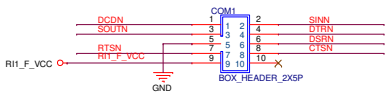


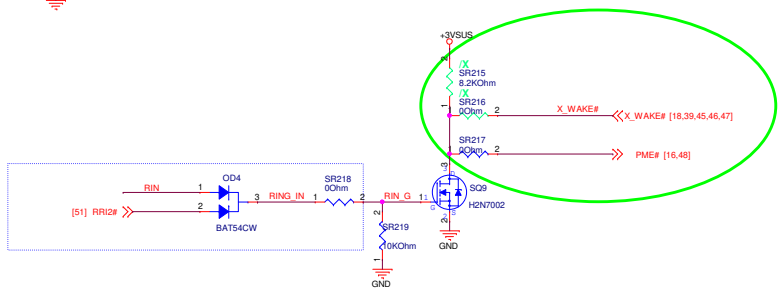


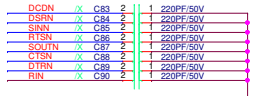
COM1_V1(5-6)	RI & Voltage SEL
1-2	12V
3-4	5V
5-6	RI (Default)

COM1_V1(5-6)

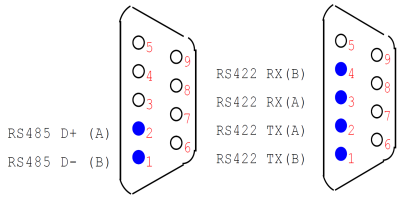








Close to COM port connector



Maximum Slew rate control		
SLEW	RS-232	RS-485/RS-422
0	1Mbps	10Mbps
1	250Kbps	250Kbps

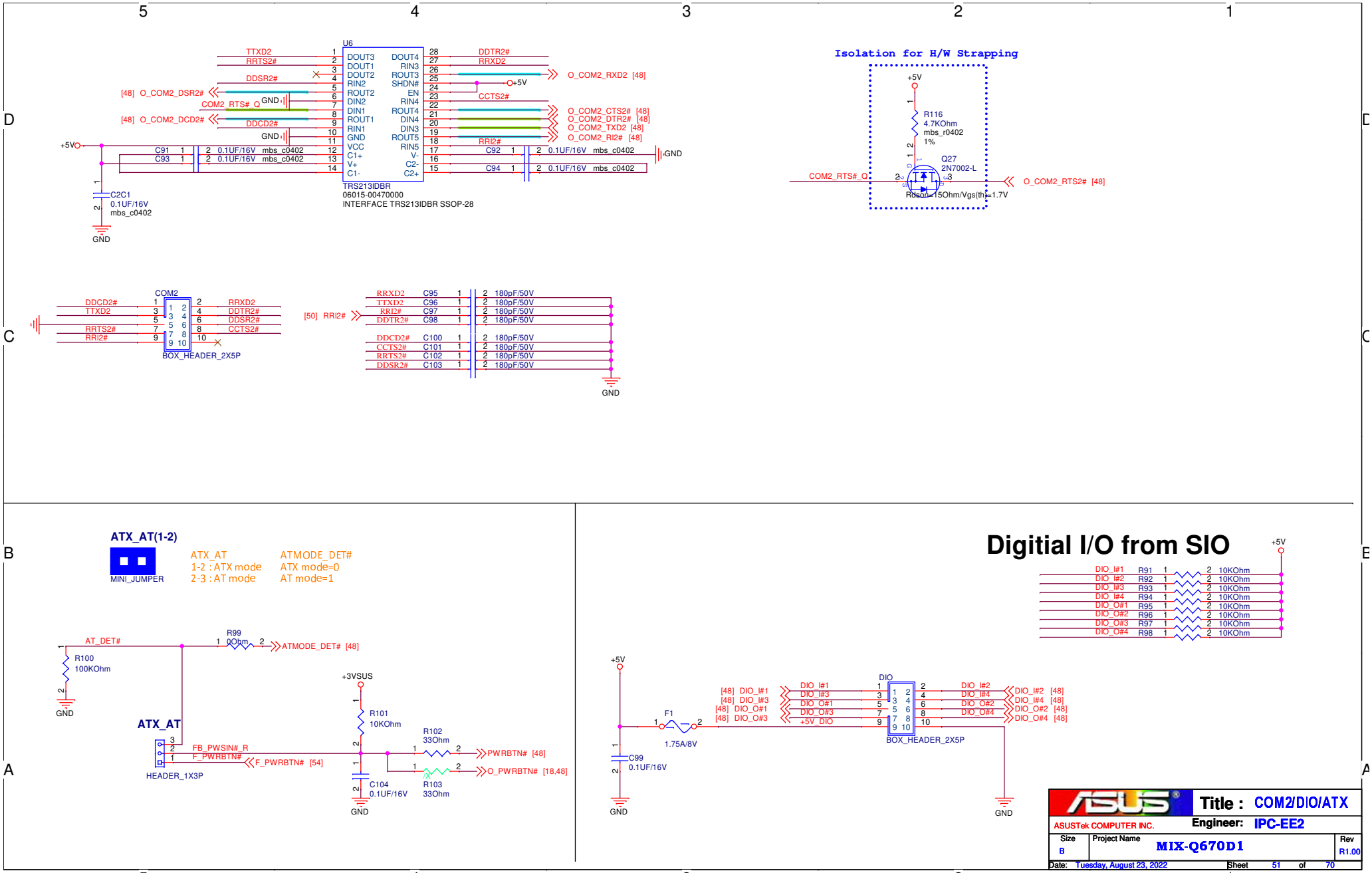
ASUSTek COMPUTER INC.

Title : COM1_RS232/422/485

Engineer: IPC-EE2

Size: Custom | Project Name: MIX-Q670D1 | Rev: R1.00

Date: Tuesday, August 23, 2022 | Sheet 50 of 70


U6
TRS213IDBR
06015-00470000
INTERFACE TRS213IDBR SSOP-28
Isolation for H/W Strapping
R116
4.7KOhm
mbs_r0402
1%
Q27
2N7002-L
Rdson=15Ohm/Vgs(th)=1.7V
COM2
BOX_HEADER_2X5P
ATX_AT(1-2)
MINI_JUMPER
ATX_AT
1-2 : ATX mode
2-3 : AT mode
ATMODE_DET#
ATX mode=0
AT mode=1
HEADER_1X3P
Digitial I/O from SIO
DIO
BOX_HEADER_2X5P
ASUSTek COMPUTER INC.
Title : COM2/DIO/ATX
Engineer: IPC-EE2
Size B
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
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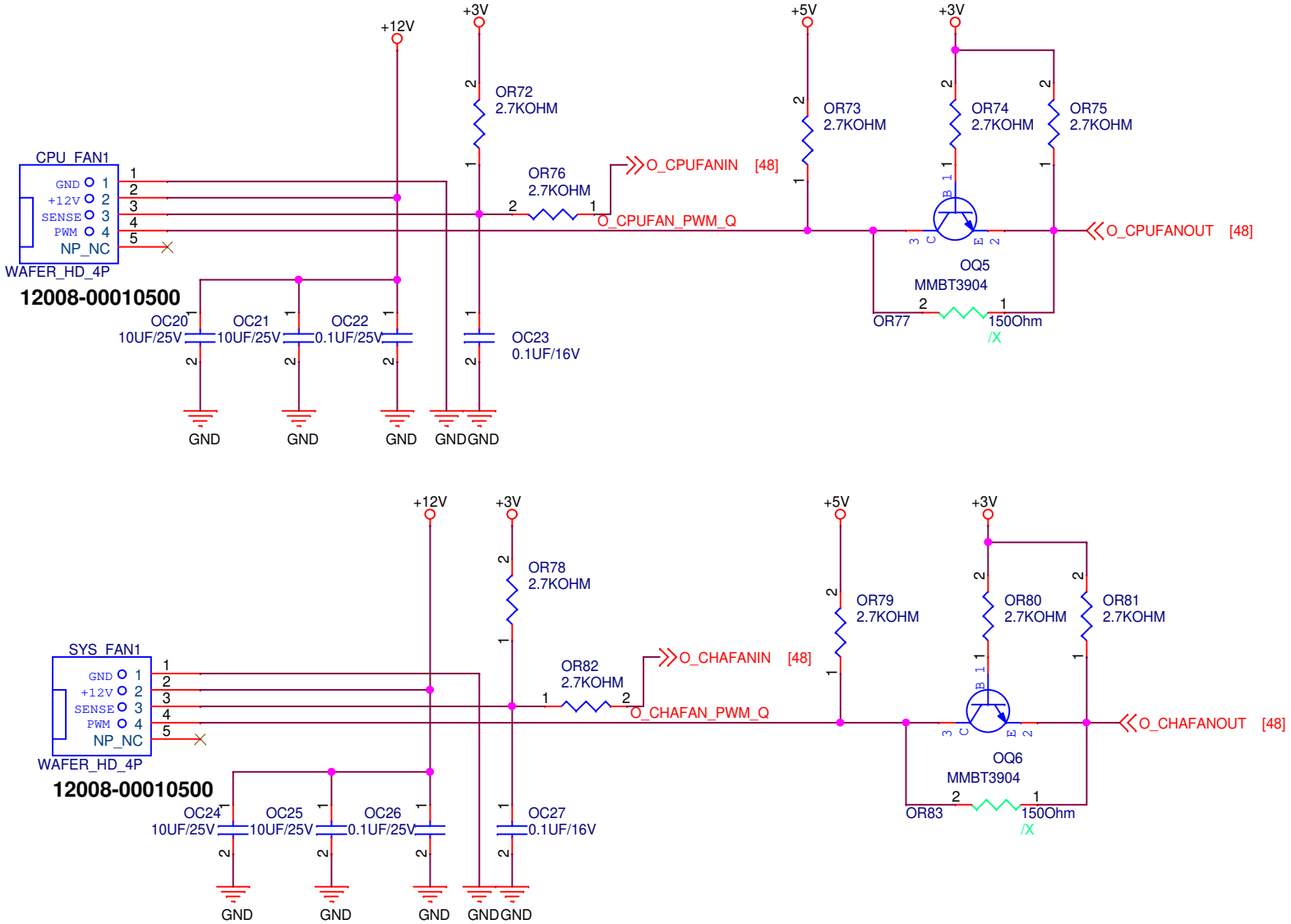
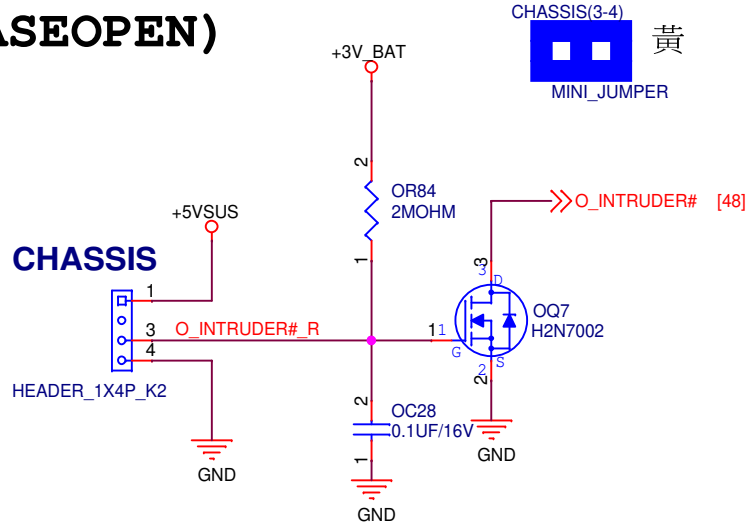


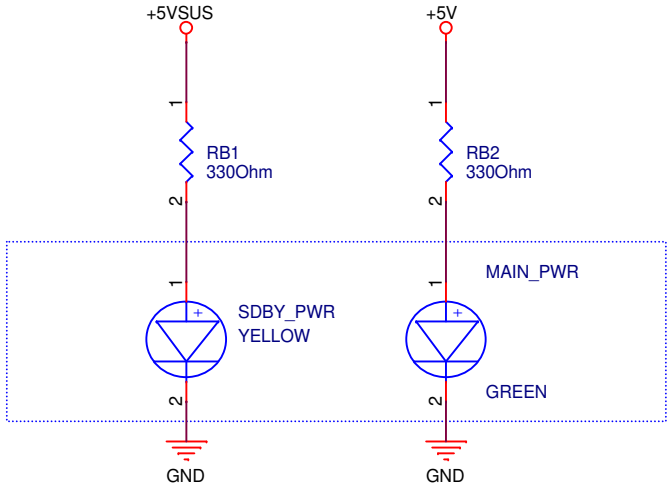
ASUS	Title : CPUFAN_SYSFAN1	
ASUSTek COMPUTER INC.	Engineer: IPC-EE2	
Size A	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 52 of 70	

Intrudor (CASEOPEN)



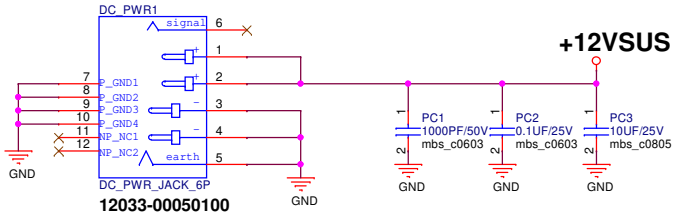
To SIO

POWER_PWR

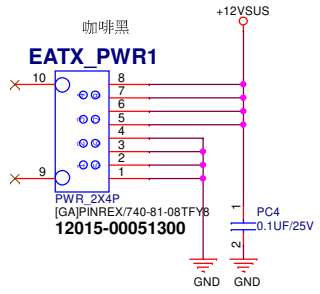


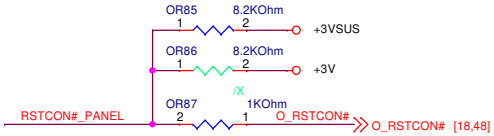
ASUSTek COMPUTER INC.	Title : Intrudor(CASEOPEN)		
	Engineer: IPC-EE2		
Size A	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 53 of 70		

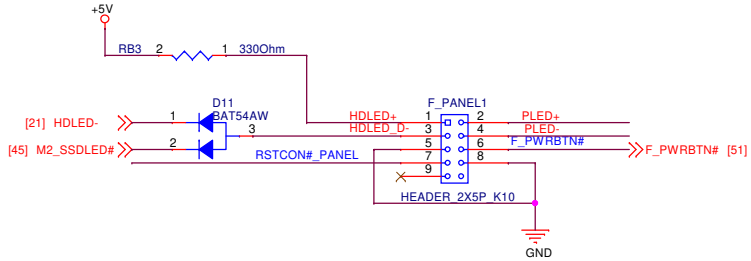
DC INPUT Connector

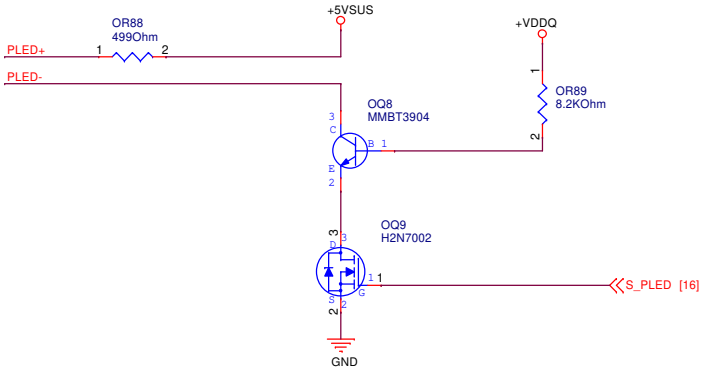


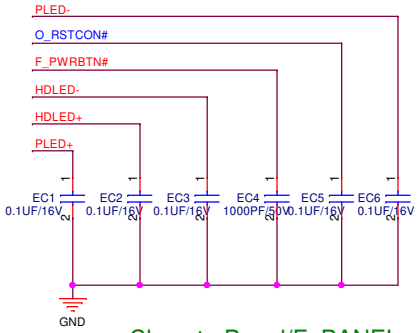
POWER CONNECTOR 12V8P







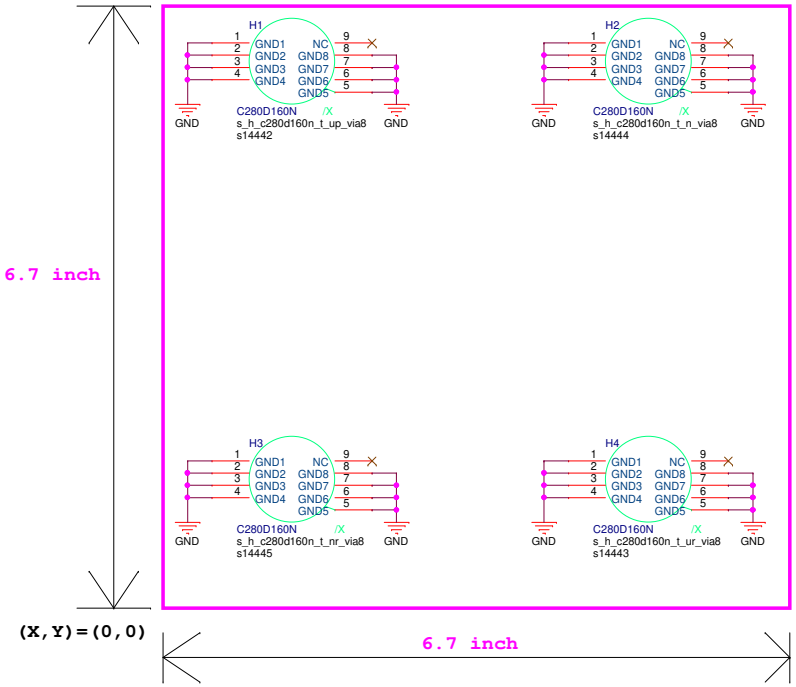




Close to Panel/F_PANEL

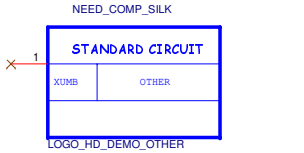
ASUS	Title : FRONT PANEL		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size B	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 54 of 70		

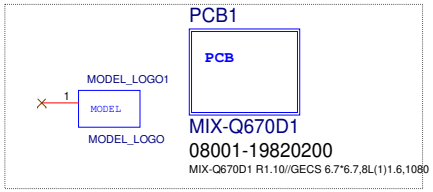
mini-ITX Screw Hole



ASUSTek COMPUTER INC.	Title : Screw Hole	
	Engineer: IPC-EE2	
Size A3	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 55 of 70	

Selling Point





MIX-Q670D1 R1.00 PCB-10 :

R1.00 PCB_GECS : 08001-19820200

R1.00 PCB_TRUSTECH : 08001-19820000

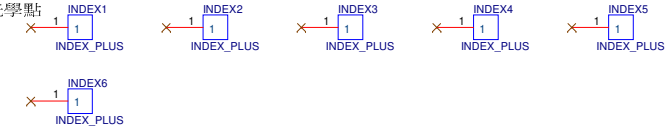
R1.00 PCB_VICTORY : 08001-19820100

Fiducial Mask (光學點)

光學點需要 6 ~ 10 顆,
LayoutRD會依空間大小及版本需求
擺放所需的光學點
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆十字光學點

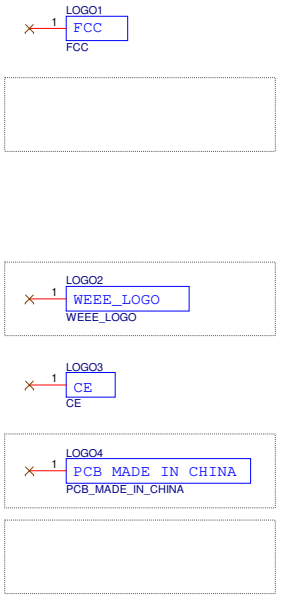
小顆十字光學點



2012/09/11

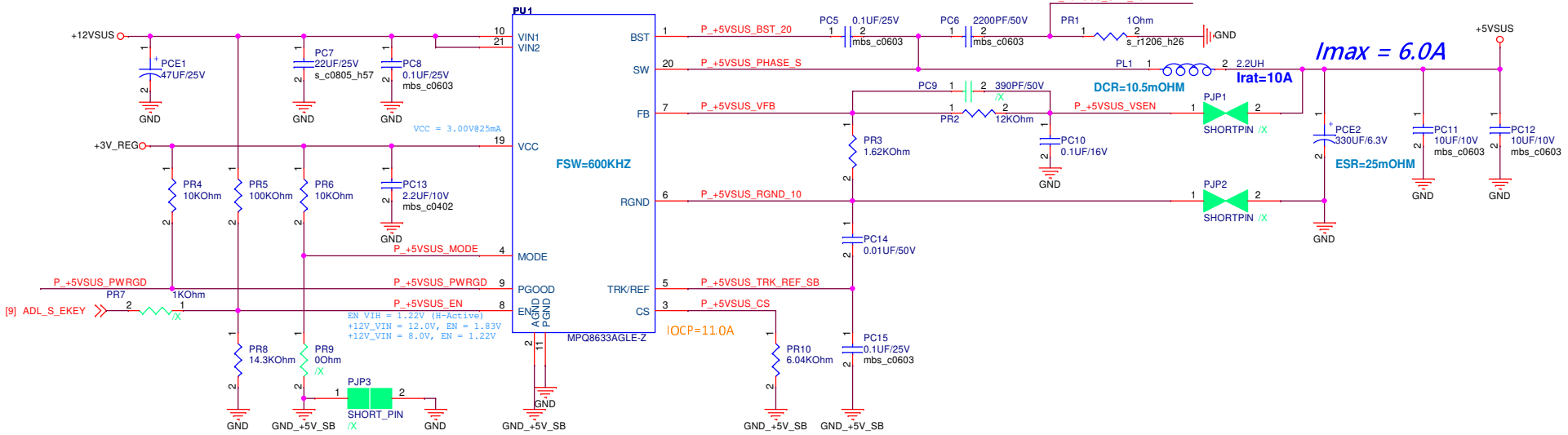
Logo

common Logo for all projects

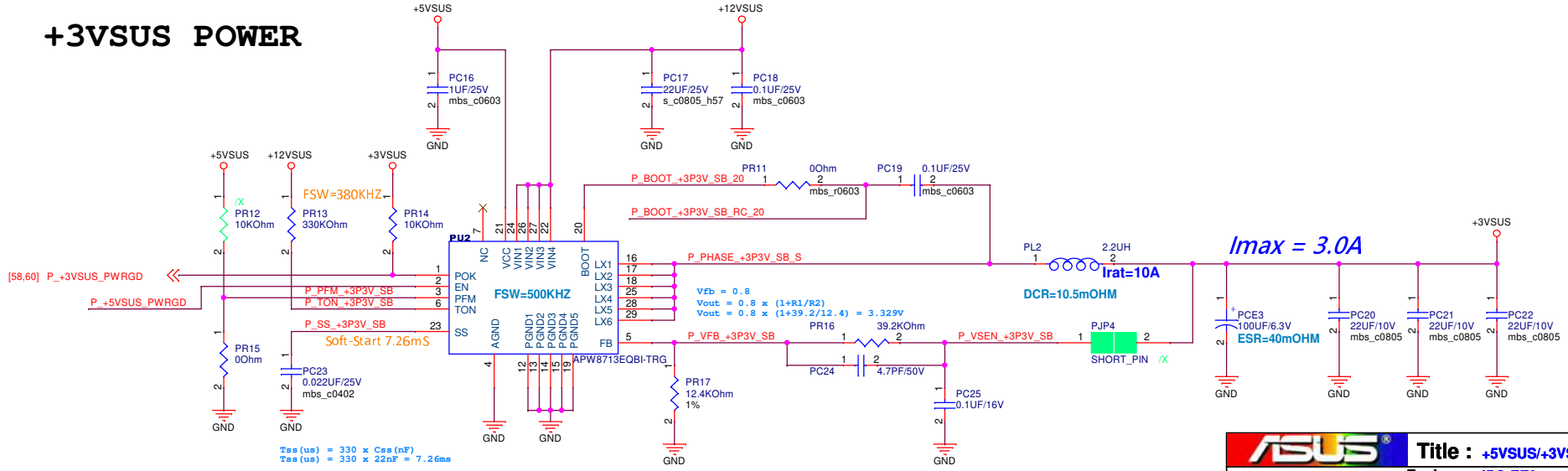


ASUS	Title : Selling Point_Logo		
ASUSTek COMPUTER INC.	Engineer: IPC-EE2		
Size A3	Project Name MIX-Q670D1		Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 56 of 70		

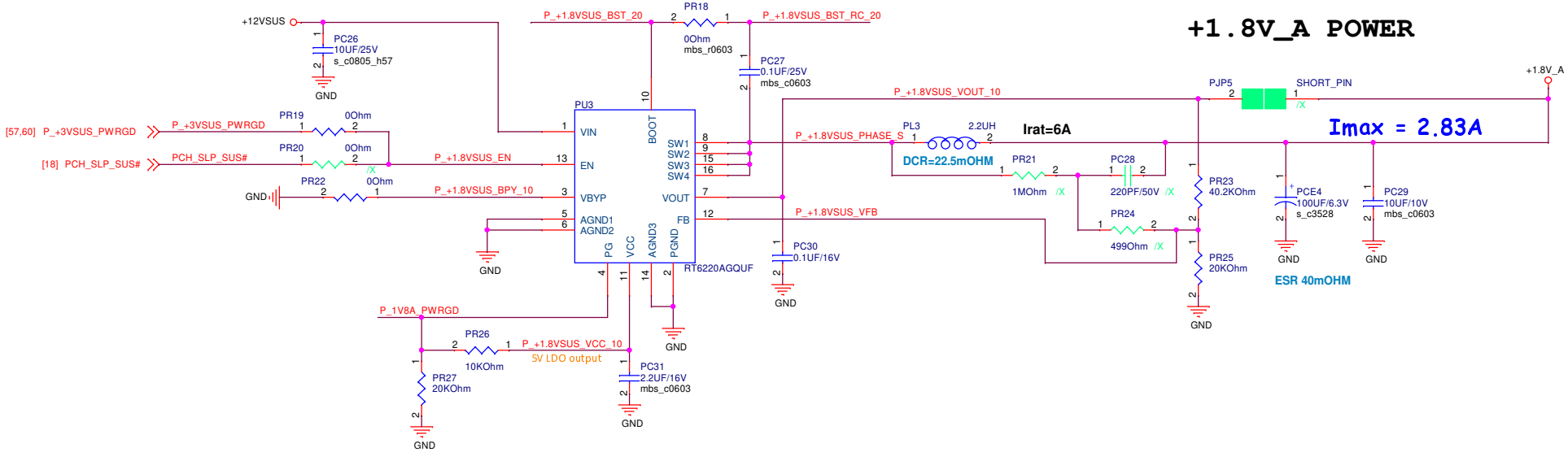
+5VSUS POWER

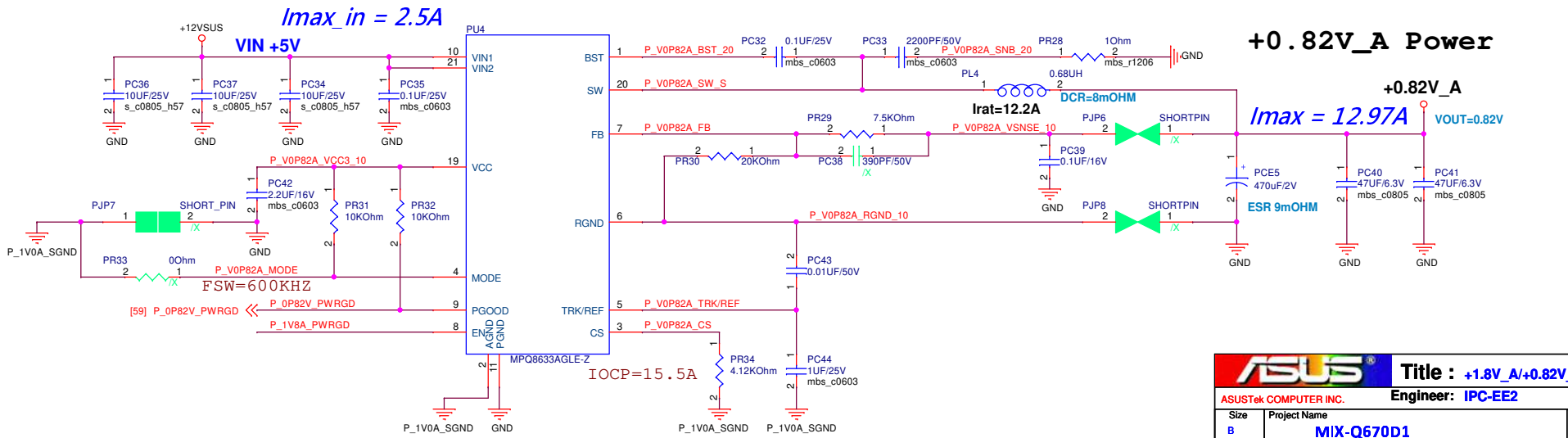


+3VSUS POWER



ASUSTek COMPUTER INC.	Title : +5VSUS/+3VSUS	Engineer: IPC-EE2
Size B	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 57 of 70	





ASUS

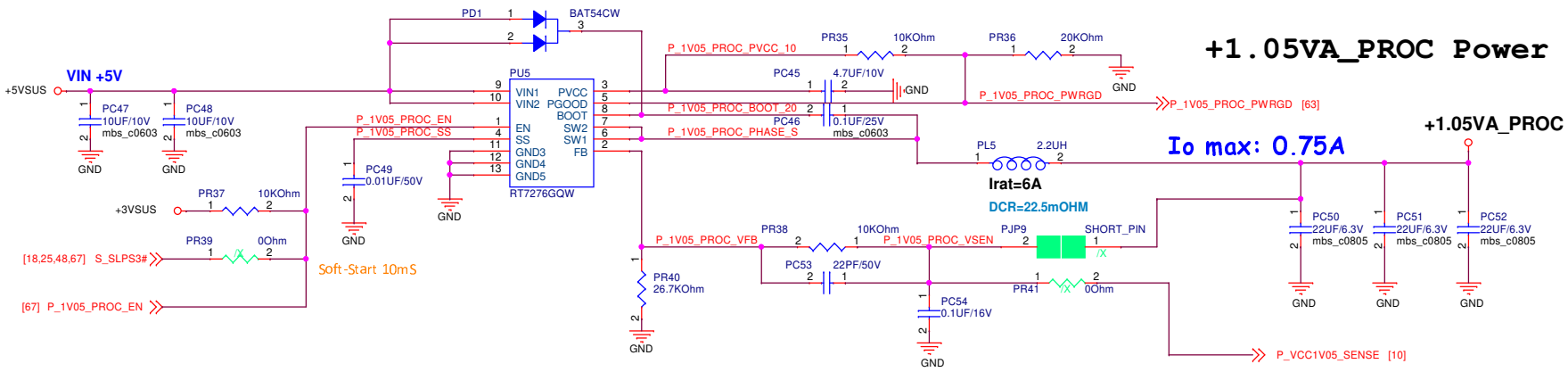
ASUSTek COMPUTER INC.

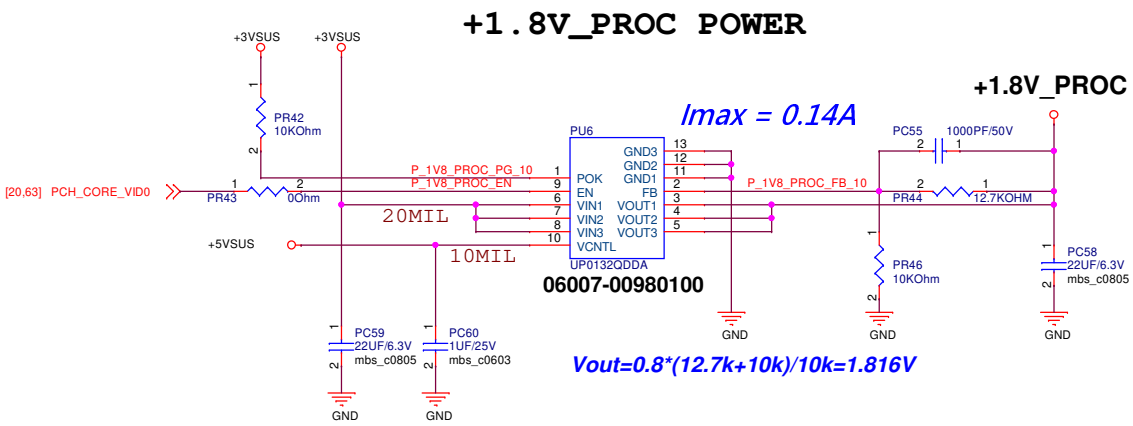
Title : +1.8V_A/+0.82V_A

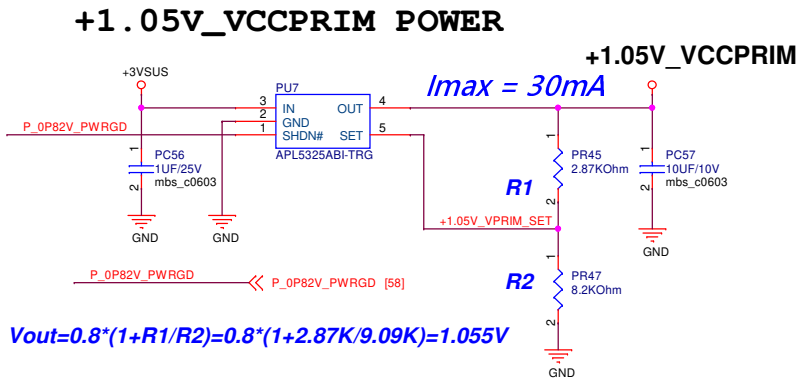
Engineer: IPC-EE2

Size	Project Name	Rev
B	MIX-Q670D1	R1.00

Date: Tuesday, August 23, 2022 Sheet 58 of 70

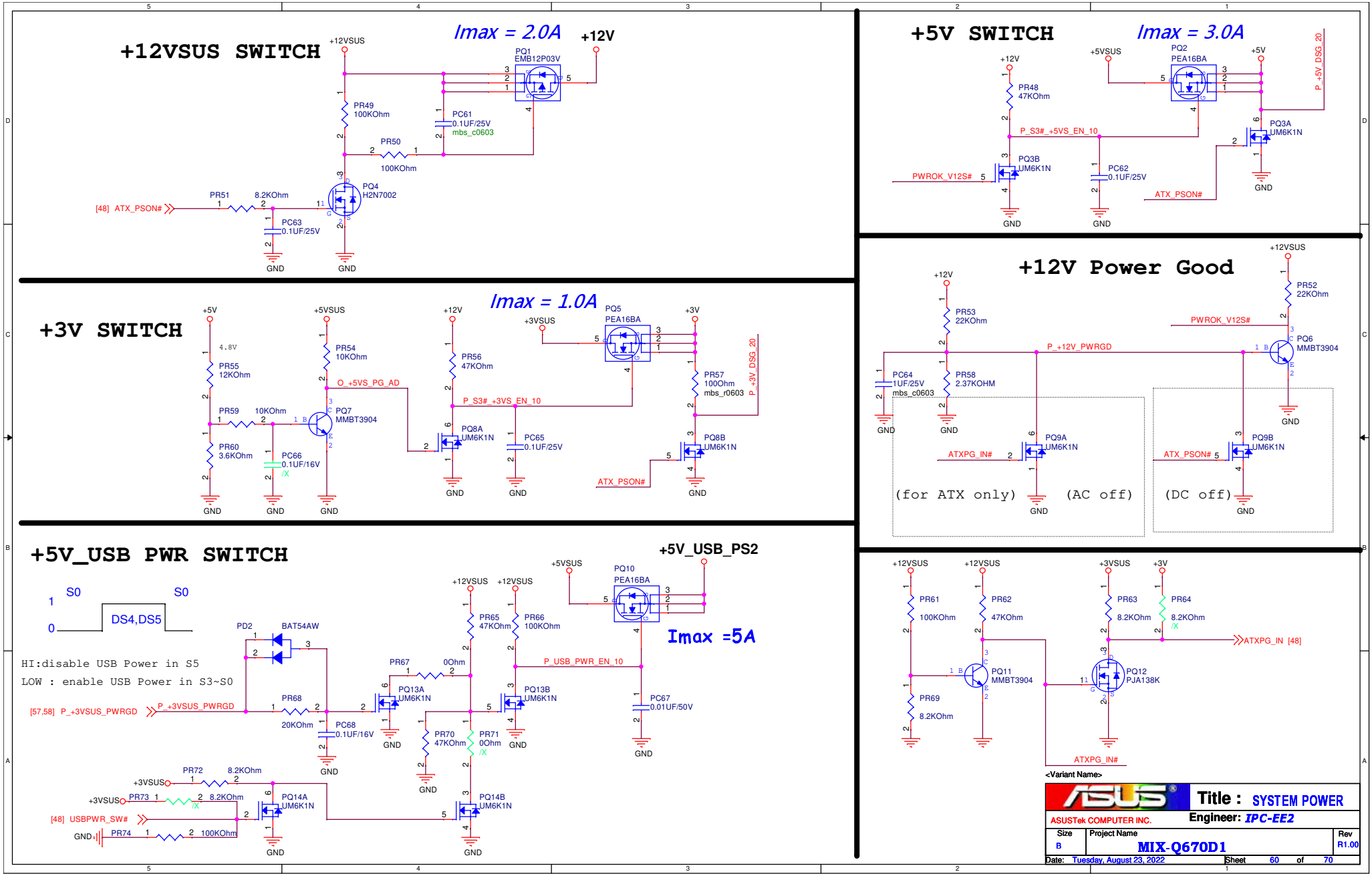






+1.05VA_VCCPRIM&+1.8V_PROC&+1.05V_PROC

ASUSTek COMPUTER INC.	Title :	Engineer: IPC-EE2
Size B	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 59 of 70	


+12VSUS SWITCH
Imax = 2.0A
+12V
PQ1 EMB12P03V
PR49 100KOhm
PC61 0.1UF/25V mbs_c0603
PR50 100KOhm
PR51 8.2KOhm
[48] ATX_PSON#
PQ4 H2N7002
PC63 0.1UF/25V
GND
+3V SWITCH
Imax = 1.0A
PQ5 PEA16BA
PR55 12KOhm
PR54 10KOhm
PR56 47KOhm
PR57 100Ohm mbs_r0603
P_+3V_DSG_20
O_+5VS_PG_AD
P_S3#_+3VS_EN_10
PR59 10KOhm
PQ7 MMBT3904
PR60 3.6KOhm
PC66 0.1UF/16V
PQ8A UM6K1N
PC65 0.1UF/25V
PQ8B UM6K1N
ATX_PSON#
+5V_USB PWR SWITCH
+5V_USB_PS2
Imax =5A
S0
DS4,DS5
HI:disable USB Power in S5
LOW : enable USB Power in S3~S0
PD2 BAT54AW
PR65 47KOhm
PR66 100KOhm
PQ10 PEA16BA
PR67 0Ohm
P_USB_PWR_EN_10
PQ13A UM6K1N
PQ13B UM6K1N
PC67 0.01UF/50V
[57,58] P_+3VSUS_PWRGD
PR68 20KOhm
PC68 0.1UF/16V
PR70 47KOhm
PR71 0Ohm
PR72 8.2KOhm
PR73 8.2KOhm
[48] USBPWR_SW#
PR74 100KOhm
PQ14A UM6K1N
PQ14B UM6K1N
+5V SWITCH
Imax = 3.0A
PQ2 PEA16BA
PR48 47KOhm
P_S3#_+5VS_EN_10
PQ3B UM6K1N
PQ3A UM6K1N
PWROK_V12S#
PC62 0.1UF/25V
ATX_PSON#
+12V Power Good
PR53 22KOhm
PR52 22KOhm
PWROK_V12S#
P_+12V_PWRGD
PQ6 MMBT3904
PC64 1UF/25V mbs_c0603
PR58 2.37KOHM
ATXPG_IN#
PQ9A UM6K1N
PQ9B UM6K1N
(for ATX only)
(AC off)
(DC off)
PR61 100KOhm
PR62 47KOhm
PR63 8.2KOhm
PR64 8.2KOhm
ATXPG_IN [48]
PQ11 MMBT3904
PQ12 PJA138K
PR69 8.2KOhm
ATXPG_IN#
<Variant Name>
Title : SYSTEM POWER
ASUSTek COMPUTER INC.
Engineer: IPC-EE2
Size B
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
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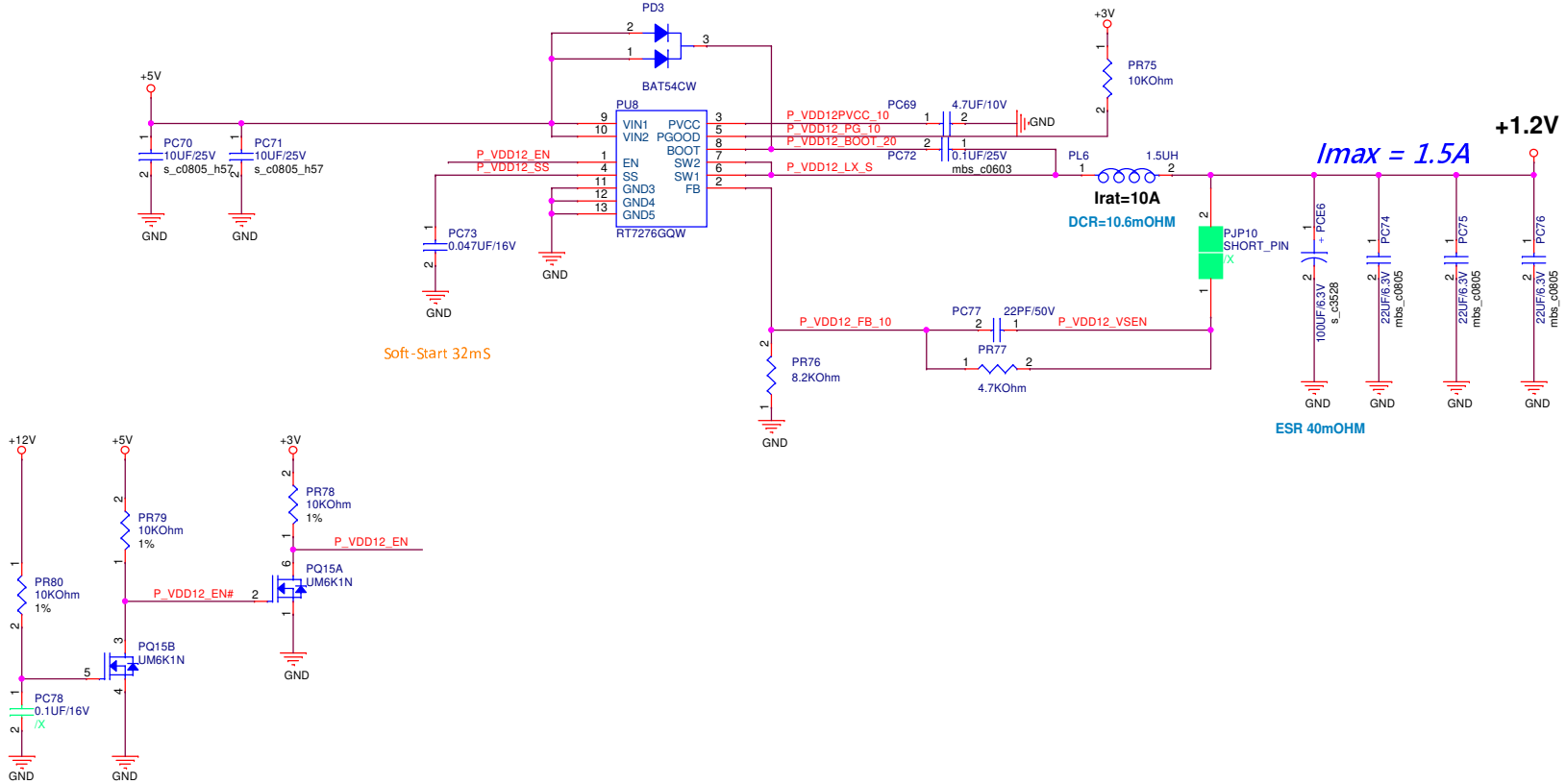
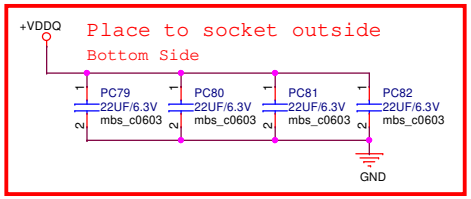
+1.2V POWER

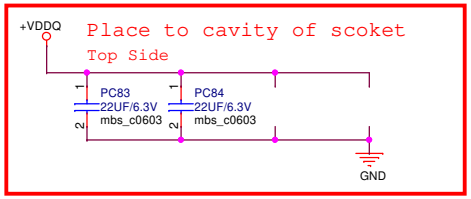


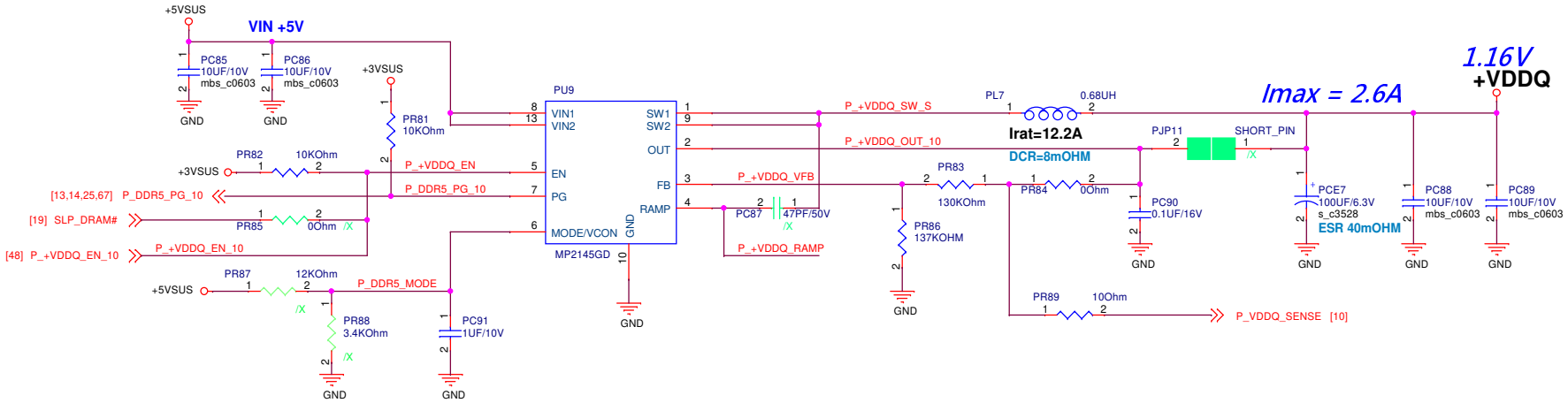
ASUS	Title : +1.2V	
ASUSTek COMPUTER INC.	Engineer: IPC-EE3	
Size B	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 61 of 70	

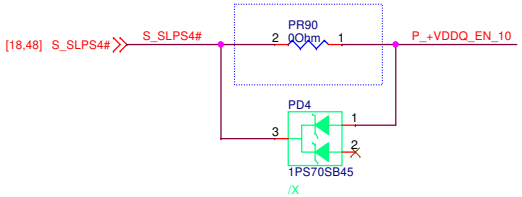
+VPPDDR POWER

Delete +VPPDDR Power, It is directly powered by DDR5 DIMM.



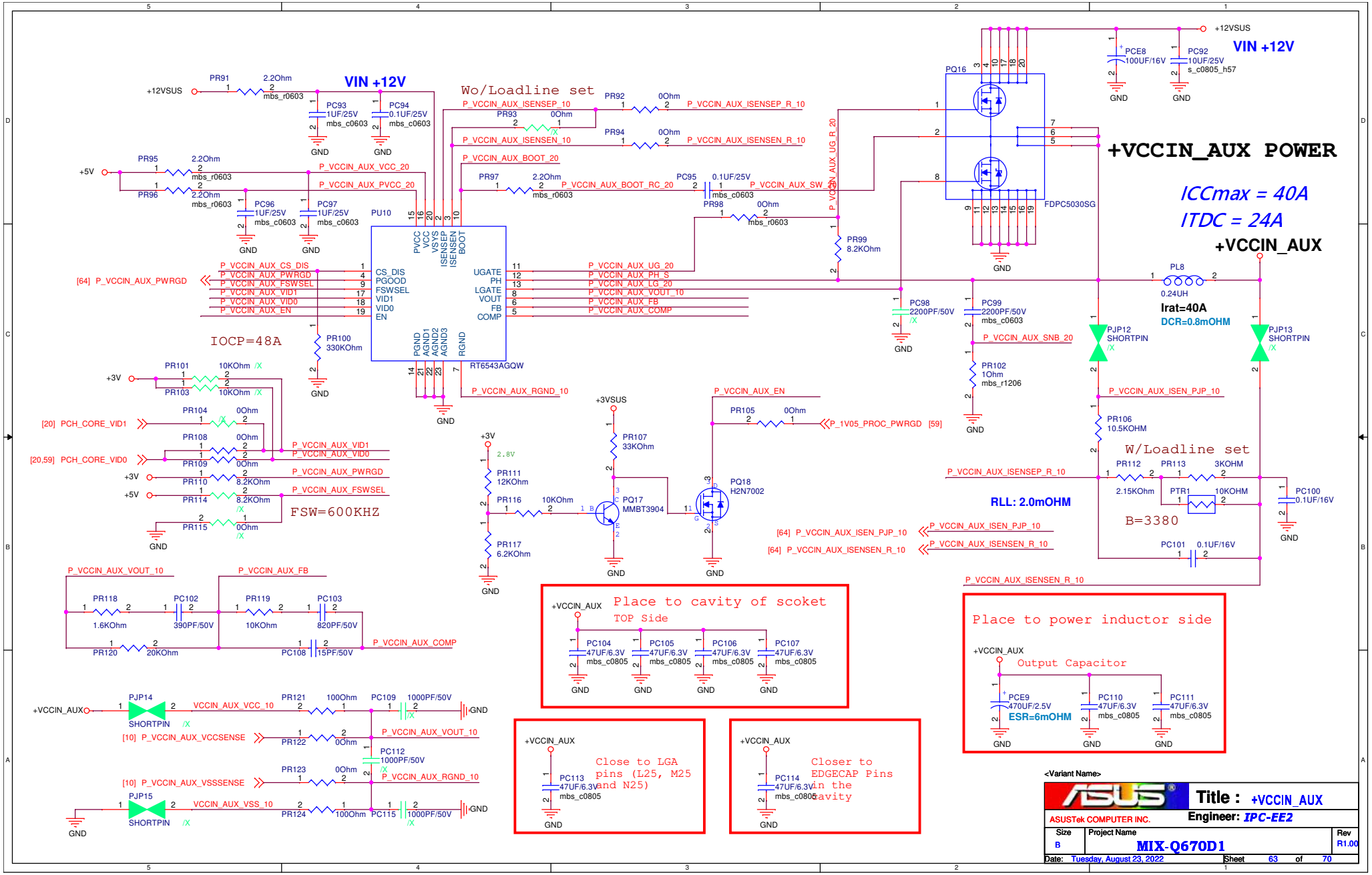






20220103 modify PR49 to 0Ohm for DDR5 Sequ. control

ASUSTek COMPUTER INC.	Title : +VDDQ	Engineer: IPC-EE2
Size B	Project Name MIX-Q670D1	Rev R1.00
Date: Tuesday, August 23, 2022	Sheet 62 of 70	


+VCCIN_AUX POWER
ICCmax = 40A
ITDC = 24A
+VCCIN_AUX
VIN +12V
Wo/Loadline set
W/Loadline set
IOCP=48A
FSW=600KHZ
RLL: 2.0mOHM
B=3380
Irat=40A
DCR=0.8mOHM
PU10
RT6543AGQW
PQ16
FDPC5030SG
PL8
0.24UH
PJP12 SHORTPIN
PJP13 SHORTPIN
PQ17 MMBT3904
PQ18 H2N7002
PJP14 SHORTPIN
PJP15 SHORTPIN
Place to cavity of scoket
TOP Side
Place to power inductor side
Output Capacitor
ESR=6mOHM
Close to LGA pins (L25, M25 and N25)
Closer to EDGECAP Pins in the cavity
Title : +VCCIN_AUX
ASUSTek COMPUTER INC.
Engineer: IPC-EE2
Size B
Project Name MIX-Q670D1
Rev R1.00
Date: Tuesday, August 23, 2022
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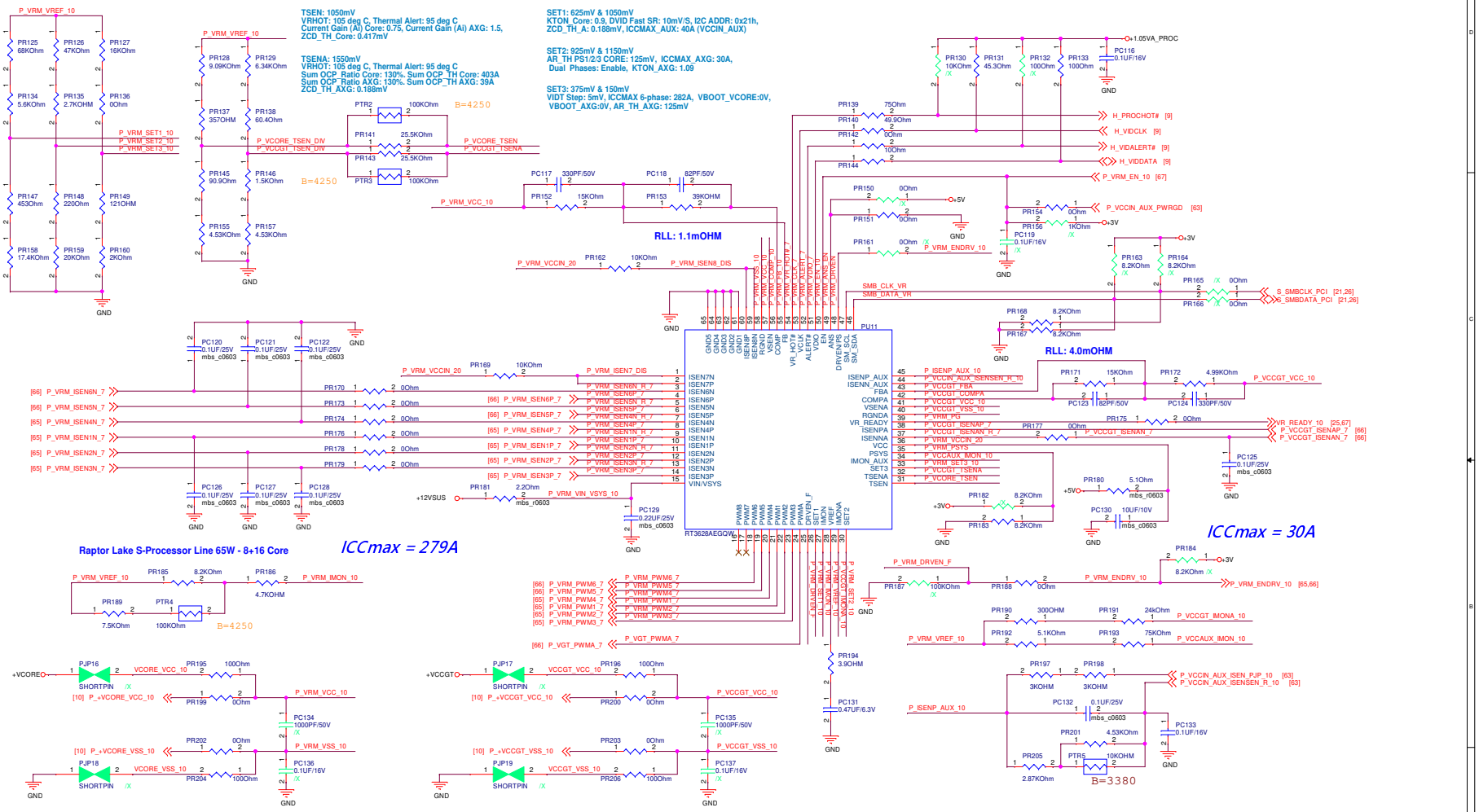
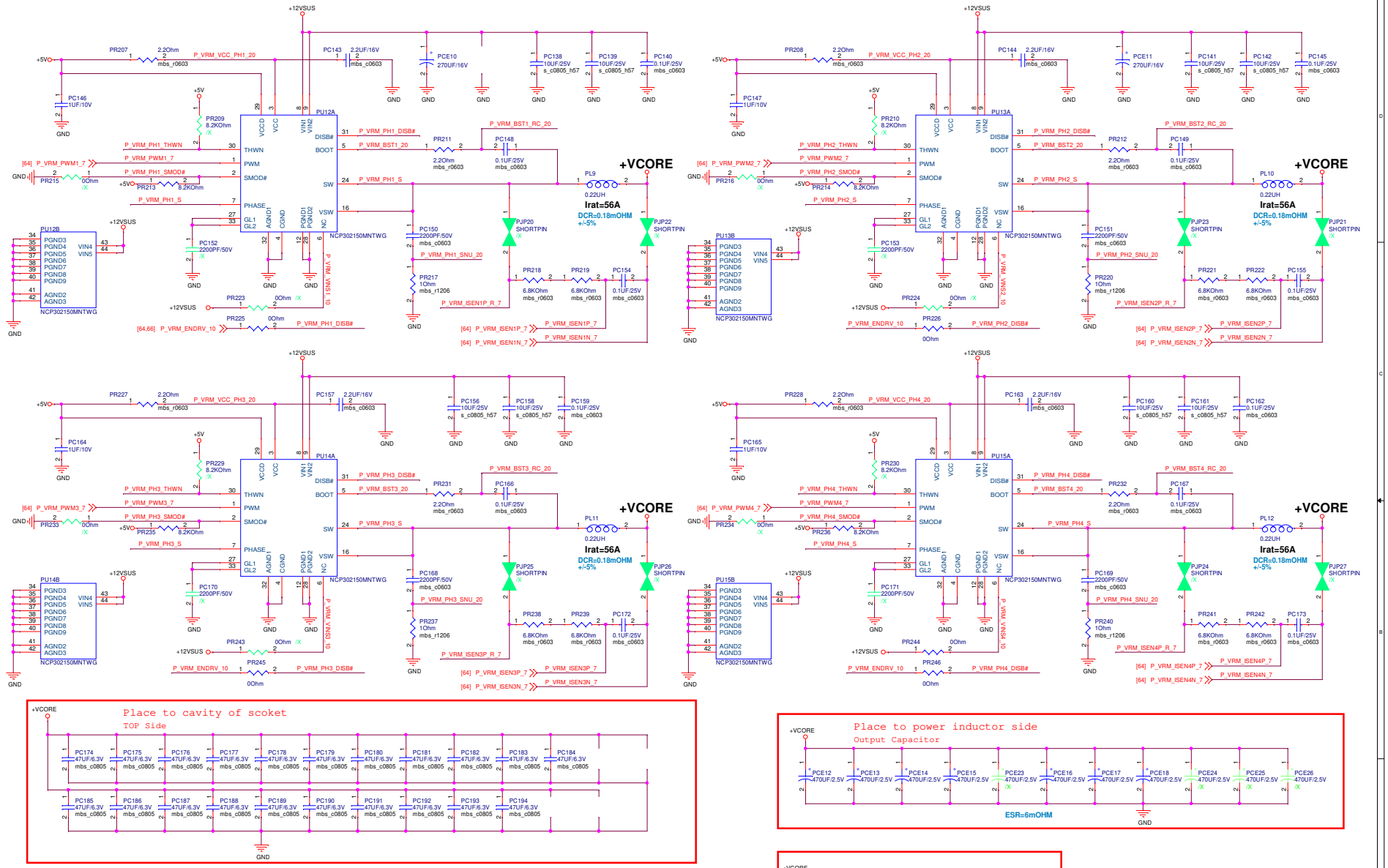
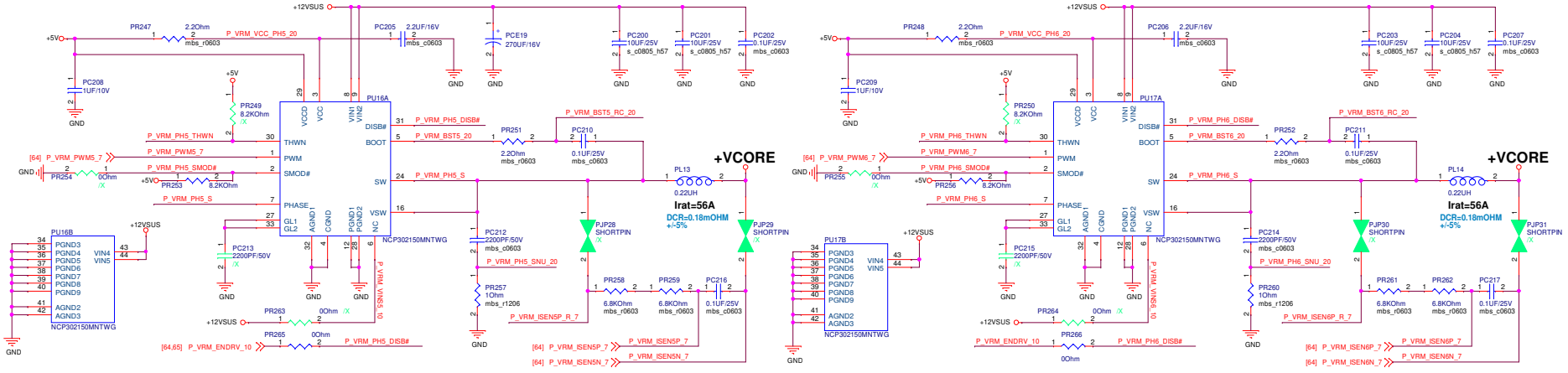
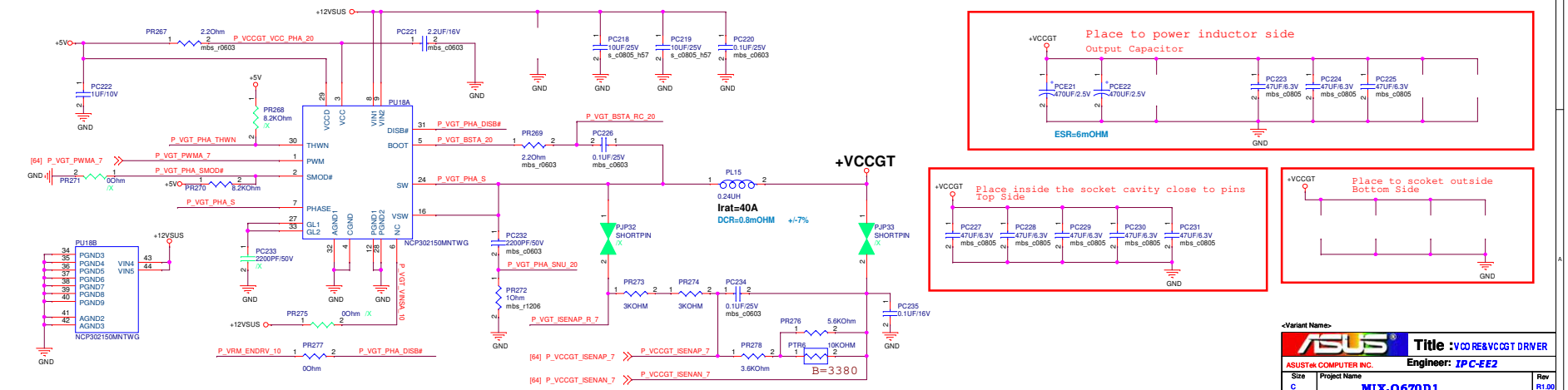

TSEN: 1050mV
VRHOT: 105 deg C, Thermal Alert: 95 deg C
Current Gain (AI) Core: 0.75, Current Gain (AI) AXG: 1.5,
ZCD_TH_Core: 0.417mV
TSENA: 1550mV
VRHOT: 105 deg C, Thermal Alert: 95 deg C
Sum OCP_Ratio Core: 130%. Sum OCP_TH Core: 403A
Sum OCP_Ratio AXG: 130%. Sum OCP_TH AXG: 39A
ZCD_TH_AXG: 0.188mV
SET1: 625mV & 1050mV
KTON_Core: 0.9, DVID Fast SR: 10mV/S, I2C ADDR: 0x21h,
ZCD_TH_A: 0.188mV, ICCMAX_AUX: 40A (VCCIN_AUX)
SET2: 925mV & 1150mV
AR_TH PS1/2/3 CORE: 125mV, ICCMAX_AXG: 30A,
Dual Phases: Enable, KTON_AXG: 1.09
SET3: 375mV & 150mV
VIDT Step: 5mV, ICCMAX 6-phase: 282A, VBOOT_VCORE:0V,
VBOOT_AXG:0V, AR_TH_AXG: 125mV
RLL: 1.1mOHM
RLL: 4.0mOHM
ICCmax = 279A
ICCmax = 30A
Raptor Lake S-Processor Line 65W - 8+16 Core
RT3628AEGQW
PU11
B=4250
B=3380
GND


+VCORE
Irat=56A
DCR=0.18mOHM
+/-5%
PU12A
PU13A
PU14A
PU15A
NCP302150MNTWG
PU12B
PU13B
PU14B
PU15B
NCP302150MNTWG
Place to cavity of scoket
TOP Side
Place to power inductor side
Output Capacitor
ESR=6mOHM
Place to VRM output capacitor side





<Variant Name>

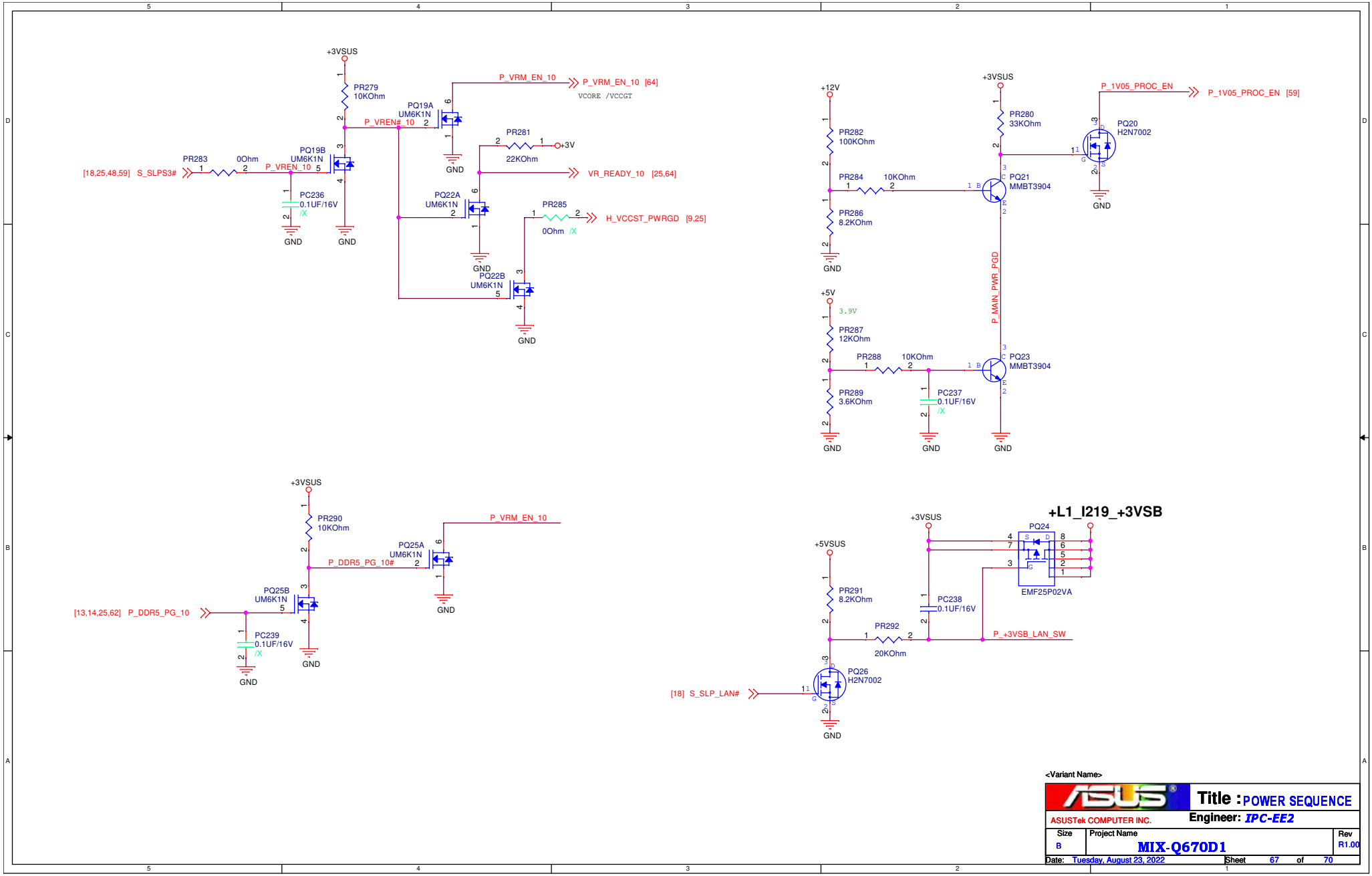
ASUSTeK COMPUTER INC.

Title : VCORE&VCCGT DRIVER

Engineer: IPC-EE2

Size	Project Name	Rev
C	MIX-Q670D1	R1.00

Date: Tuesday, August 23, 2022 Sheet 66 of 70



<Variant Name>

ASUSTek COMPUTER INC.

Title : POWER SEQUENCE

Engineer: IPC-EE2

Size	Project Name	Rev
B	MIX-Q670D1	R1.00

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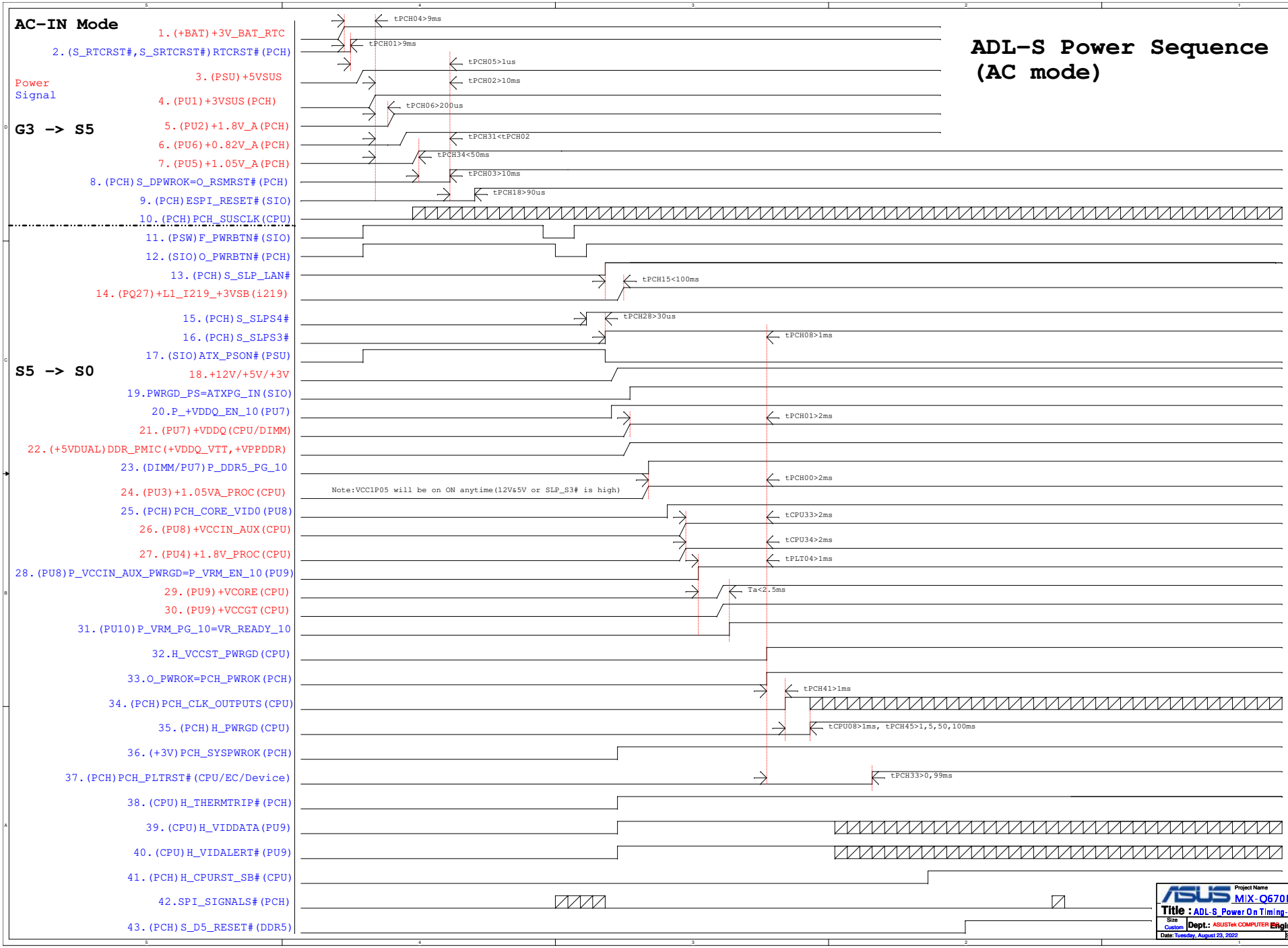
ADL-S Power Sequence (AC mode)



ASUS	Project Name: MIX-Q670D1	Rev: R1.00
Title : ADL-S_Power On Timing--AC mode_R0.1		
Size: Custom	Dept.: ASUSTek COMPUTER INC.	Engineer: IPC-EE2
Date: Tuesday, August 23, 2022	Sheet 68 of 70	

MIX-Q670D1 Power Budget

MIX-Q670D1 ADL-S Power ConsumptionVer0.1	System Power																	
EATX_Power Source_Original	+12VSUS																	
EATX_Power1 Source	12V																	
Power Plane 1	+VCORE	+VCCGT	+1.8V_A	+0.82V_A	+12V	+VCCIN_AUX	+5VSUS					+3VSUS						
Power Voltage	0V~1.72V	0.55V~1.52V	1.8V	0.82V	12V	1.8V	5V					3.3V						
Enable pin	P_VRM_EN_10		+3VSB_PG_10	1V8A_PWRGD		VCCIN_AUX_EN	P_+5VSUS_EN					P_+5VSUS_PWRGD						
Power Good	VR_READY_10		1V8A_PWRGD	0P82V_PWRGD		VCCIN_AUX_PWRGD	P_+5VSUS_PWRGD					P_+3VSUS_PWRGD						
Power Plane 2								+5V		+VDDQ	+5V_USB_PS2		+1.8V_PROC	+L1_I219_+3VSB	+3V_BAT	+3V	+1.2V_LVDS	+1.05V_VCCPRIM
Power Voltage								5V		1.16V (DDR5)	5V		1.8V	3V	3V	3.3V	1.2V	1.05V
Enable pin										+VDDQ_EN_10			PCH_CORE_VID0	S_SLP_LAN#			+3V	0P82V_PWRGD
Power Good										DDR5_PG_10			1V8_PROC_PG_10				1.2V_PWROK	
Power Plane 3									+1.05VA_PROC	+1.2V								
Power Voltage									1.05V	1.2V								
Enable pin									1V05_PROC_EN	+1.2V								
Power Good									1V05_PROC_PWRGD	VDD12_PG_10								
CPU Alder Lake Processor-S (8+8) Cores vPro 32EU, 65W compatible with CPU RPL-S (8+16)	160.000	22.000				36.000			0.767		2.600			0.140					
Chipset Alder Lake PCH-H (600 series)_Q670E			2.314	13.488									0.661			0.023			0.029
DDR5 4800MHz SO-DIMM*2pcs (Max 32GB per DIMM)							4.000												
SIO NCT6126D // Nuvoton LQFP-128									0.001				0.008				0.000		
SPI ROM (System-WINBOND 256M SOIC-16)													0.025						
SPI ROM LOGIC SN74CBT3126PWR *2PCS							0.050												
DP Source Port*2																	3.000		
HDMI Source Port*2								3.000											
HDMI2.0 re-timer_PS8409A * 2pcs										0.580							0.034		
eDP/LVDS Source Port*1					3.500			3.500									1.500		
eDP to LVDS_CH7513A * 1pcs																	0.064	0.138	
M.2 2230 PCIE M.2 E-key *1 pcs (PCIe Gen3)													2.000				1.760		
GLAN-1 I219LM*1															0.399				
GLAN-2 I210AT*1													0.209						
M.2 2242/2280 PCIE M.2 M-key SSD*1 pcs (PCIe Gen3)																	5.000		
M.2 3042/3052 PCIE M.2 B-key SSD/LTE*1 pcs (PCIe																	1.760		
Audio Codec (Realtek_ALC897-VB0)							0.008										0.019		
Audio Amp (EUA2075JIR1)							0.002												
USB3.2 Gen2x1 Type A *4 ports												6.000							
SATA POWER*2					3.000			3.000											
USB 2.0 pin header x 1 (support additional USB2.0												2.000							
FB1438G Transceiver_RS232/RS422/RS485								0.030											
COM1 Port_Support RS232/RS422/RS485					0.500			0.500											
COM2 Ports_Support RS232*1pcs					0.500			0.500											
TPM2.0_SLB 9672													0.035						
CPU FAN_PWM*1pcs					0.750														
Chassis-SYS FAN_PWM*1pcs					0.750														
Front Panel Header, LED & PWR Button							1.000	1.000			0.5						0.500		
Sub_Current(A)	160.000	22.000	2.314	13.488	9.000	36.000	5.059	11.530	0.768	0.580	2.600	8.000	2.914	0.140	0.399	0.023	13.637	0.138	0.029
Toatal_Current(A)	160.000	22.000	2.314	13.488	9.000	36.000	5.059	11.530	0.768	0.580	2.600	8.000	2.914	0.140	0.399	0.023	13.637	0.138	0.029
Voltage(V)	1.720	1.520	1.800	0.820	12.000	1.800	5.000	5.000	1.050	5.000	1.160	5.000	3.000	1.800	3.000	3.000	3.300	1.200	1.050
Total PWR (W)	275.200	33.440	4.166	11.061	108.000	64.800	25.296	57.650	0.806	2.900	3.016	40.000	8.741	0.252	1.197	0.069	45.001	0.166	0.030
Source Current(A)	22.933	2.787	0.347	0.922	9.000	5.400	2.108	4.804	0.067	0.242	0.251	3.333	0.728	0.021	0.100	0.006	3.750	0.014	0.003
Total Source Current(A)	56.816																		

8+8 65W Performance		
IPL2 [A]	160	22
IccMax current 10 ms max	240	30
IccMax_App current	85% of IccMax	NA
IccMax di (IccMax transient) [A]	185	21
IccMax_App di (IccMax_App transient)	IccMax_App di = IccMax_App - (IccMax - IccMax di)	NA
dt (ns) (Slew time for the di step) (Note 3)	200	250
8+8 65W Baseline		
IPL2 [A]	116	22
IccMax current 10 ms max	172	30
IccMax_App current	85% of IccMax	NA
IccMax di (IccMax transient) [A]	134	21
IccMax_App di (IccMax_App transient)	IccMax_App di = IccMax_App - (IccMax - IccMax di)	NA
dt (ns) (Slew time for the di step) (Note 3)	200	250

<Variant Name>

ASUSTeK COMPUTER INC.

Title : Power Budget

Engineer:

Size	Project Name	Rev
C	MIX-Q670D1	R1.00

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History 2022/02/25 R1.00

01) First release

History 2022/03/18

01) update Power schematic at p.4, 65-72
02) correct Clock Distribution at p.2
03) correct TPM symbol and circuit at p.1, 29
04) correct Power net referece at p.76

History 2022/03/28

01) change Cap size to 0201 for USB3.1 Gen2 at p.44, 45, 47
02) change L1L1 to 09016-00048300 for main part EOL at p.39
03) correct resistor of SPI to 75ohm, follow intel PDG at p.28-29
04) modify SKTOCC circuit at p.9, 20, 52-53.
05) PH 1kohm at H_TP_CATERR# for debug use at p.9

History 2022/03/30

01) delete SATA_PWR con. at p.43

History 2022/05/05

01) correct DDC net name at p.21
02) modify +5V_USB_PS2 power cap. at p.44-48, 73
03) delete L1/L2_GND adn modify to GND at p.40, 42
04) default unmount ESD at LAN, p.40, 42
05) modify LVDS PWR at p.35, 76
06) change FAN con. to 12G08000504M and SYS_FAN to PWM mode at p.52, 56
07) unmount HR94, follow CRB. at p.9
08) combine +VCCDDQ_EDGECAP1/2 for better PWR width. at p.10
09) remove +VCCSFR for unused at p.10
10) change S_SLPS0# default PH for EDS required external PH at p.17
11) remove SR129 for double PH at CPU, p.26
12) modfiy +5V PWR cap. at p.64
13) change USB Power to switch IC control for SPEC cahgneat p.21-22, 44-48
14) change B-key to PCIex1 at p.1, 18, 50
15) swap LAN2 PCIe port 8 to port 6 at p.1, 16, 18
16) cahgne CLKREQ# PH location at PCH, p.16, 50
17) cahgne Audio BEEP A_GND to GND at p.36
18) add BOM option for H610 at p.33-34, 46-47

History 2022/06/01

01) modify AGND to A_GND at p.51
02) modify PCIe CLKREQ# default unmount PH for CLK free run at p.16
03) modify M2, H1-H4 and add M4 for layout request at p.36
04) change RSTCON#_PANEL default PH to +3VSB_ATX at p.60
05) change +1.8V_A PWR solution for source shotage at p.67
06) default mount OR24 for RSMRST# OD in SIO at p.52
07) add PD 100kohm to prvent ATXPG_IN at G3, p.60
08) add PH 4.7kohm at SIO_SPK for OD, p.54
09) reserve 0ohm for AT/ATX mode test at p.52
10) remove OR189 for PWM FAN design at p.52
11) change OR37 to 10Kohm at p.54 (follow datasheet)
12) change P_VRM_L+12V_S to +12V for +VCCIN_AUX at p.69
13) default PD 100kohm for eDP control signal at p.20
14) modify LG1700 and ILM P/N at p.5-11
15) modify B-key to H=4mm at p.50
16) delete 42 Hold and change 80 Hold for M-key at p.49
17) use SIO instead of Auto PWR on (AT mode) at p.52, 57
18) delete CPU unused CFG & BPM signal at p.9
19) remove SD4, SMBus and other reserve circuit at p.19, 22, 27, 49-50, 57

History 2022/06/02

01) change 2*HDMI to 2*DP for layout placement at 1, 21, 32-34, 76
02) change eDP/LVDS con. to follow PMC-H610 at p.35
03) remove DC backlight control for spec change at p.35
04) remove BOM option Q670

History 2022/06/07

01) change OC89 to POSCAP 7343 type for layout placement at p.60

History 2022/06/08

01) correct M.2 B-key footprint with place bound at p.50
02) change XCE2 to POSCAP 7343 type for layout placement at p.30

History 2022/06/08 v2

01) chagne PCIex16 to iv part at p.30
02) delete M-key and B-key un-used TP at p.49, 50

History 2022/06/10

01) chagne M.2 B-key default mount 52 and unmount 42 for low profile at p.50
02) modify eDP/LVDS pin description at p.35

History 2022/06/13

01) swap DDI Port B/C and change display con. at p. 1, 6, 21, 31-32, 75
02) modify H1-H4 for standard hole at p.62
03) swap DDR signal for layout request at p.7-8

ASUS	Title : History	
ASUSTek COMPUTER INC.	Engineer:	
Size: A2	Project Name: MIX-Q670D1	Rev: R1.00
Date: Tuesday, August 23, 2022	Sheet 70 of 70	