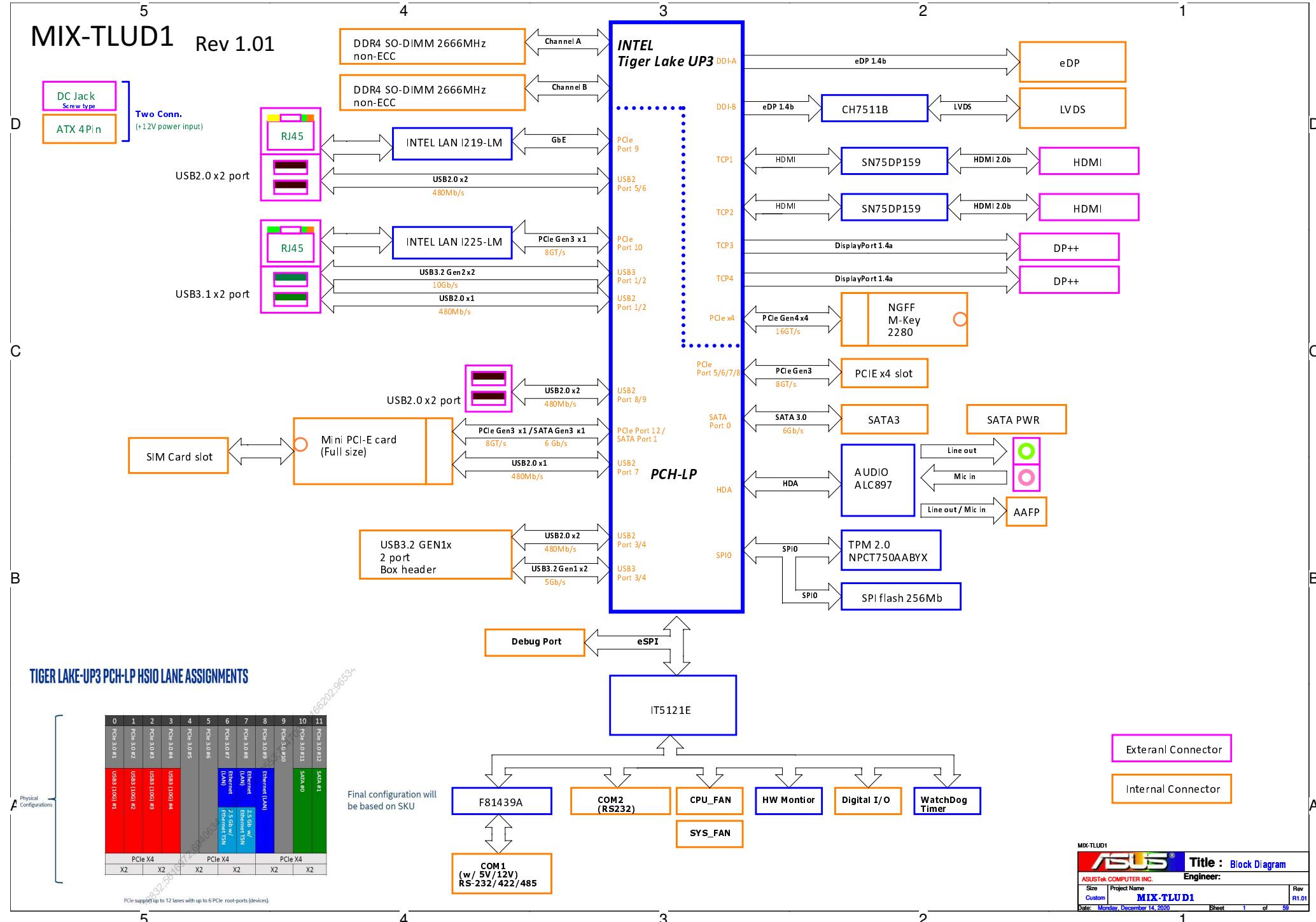
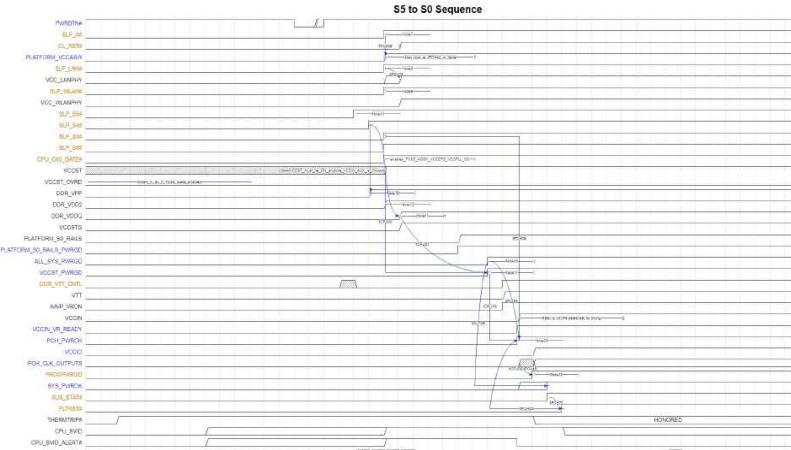
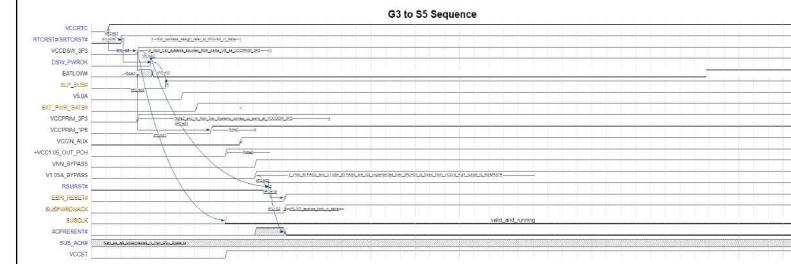
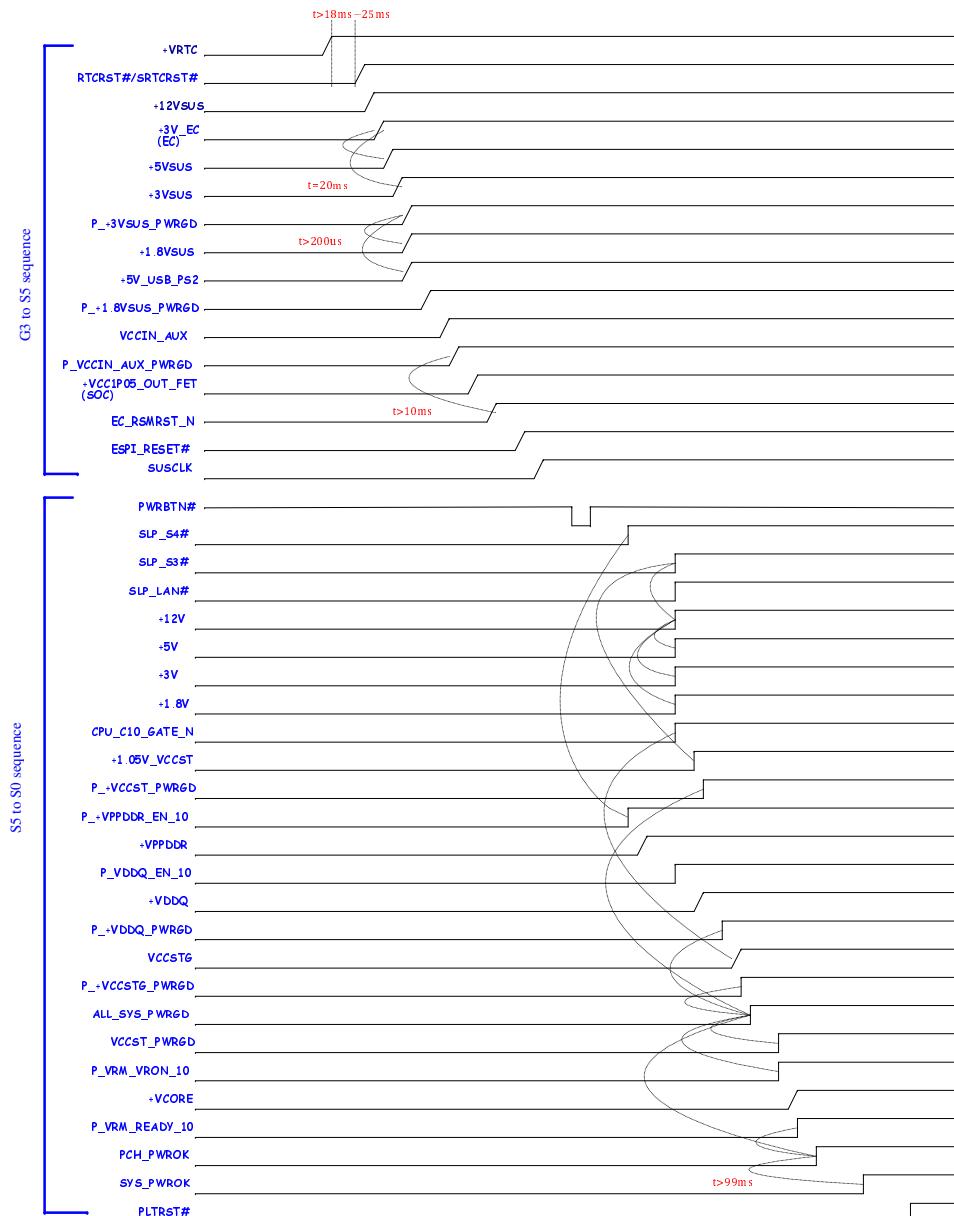
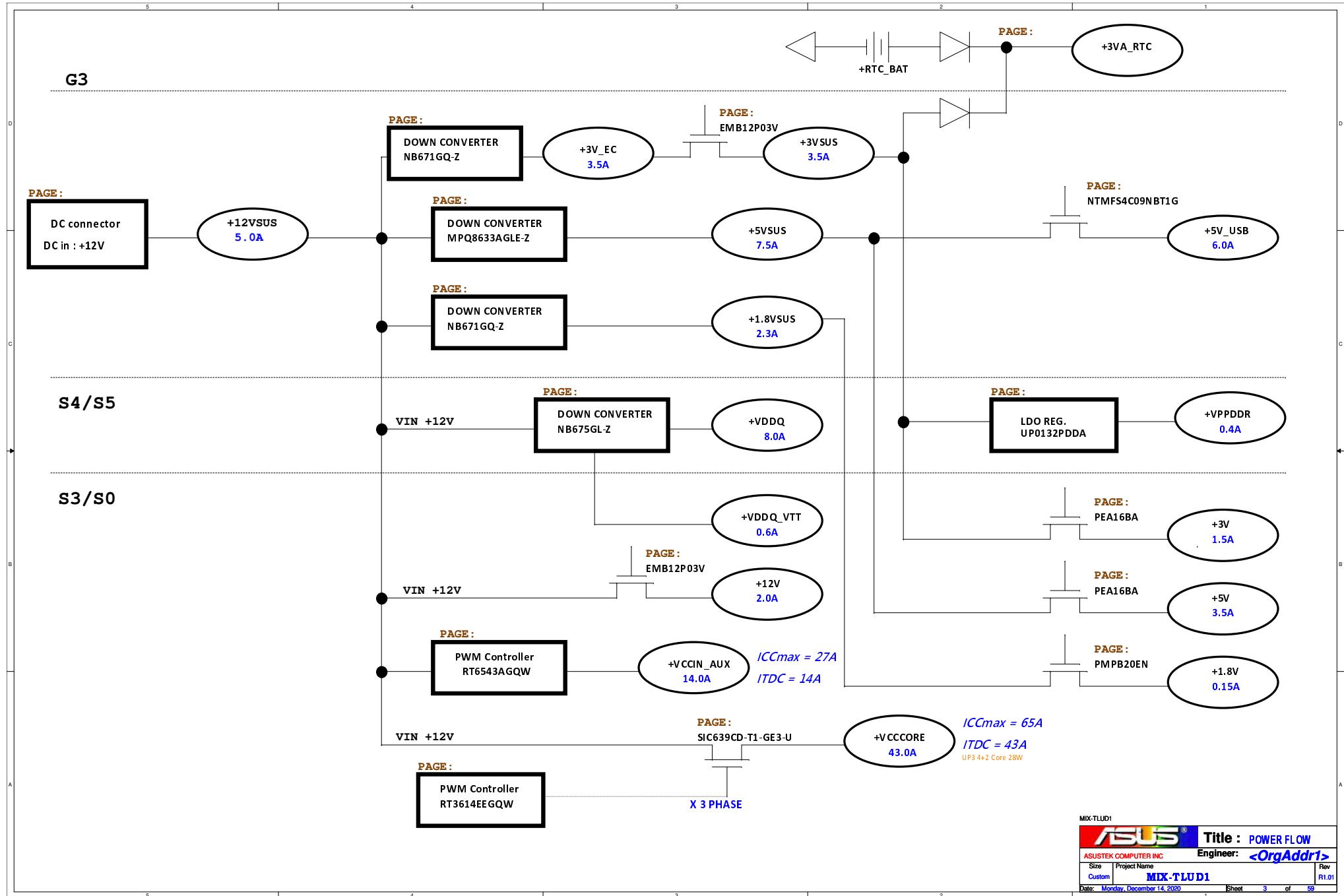


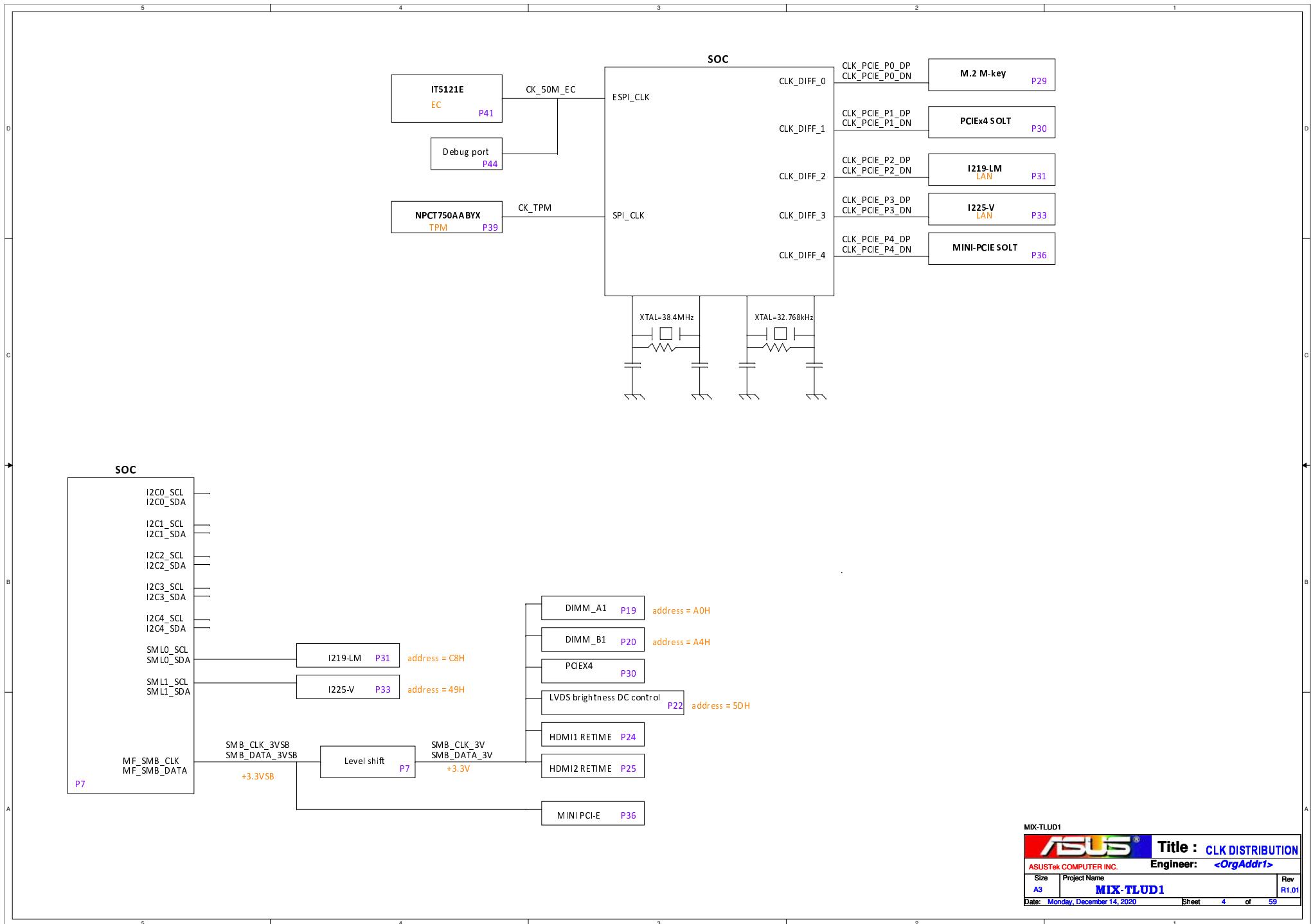
MIX-TLUD1 Rev 1.01

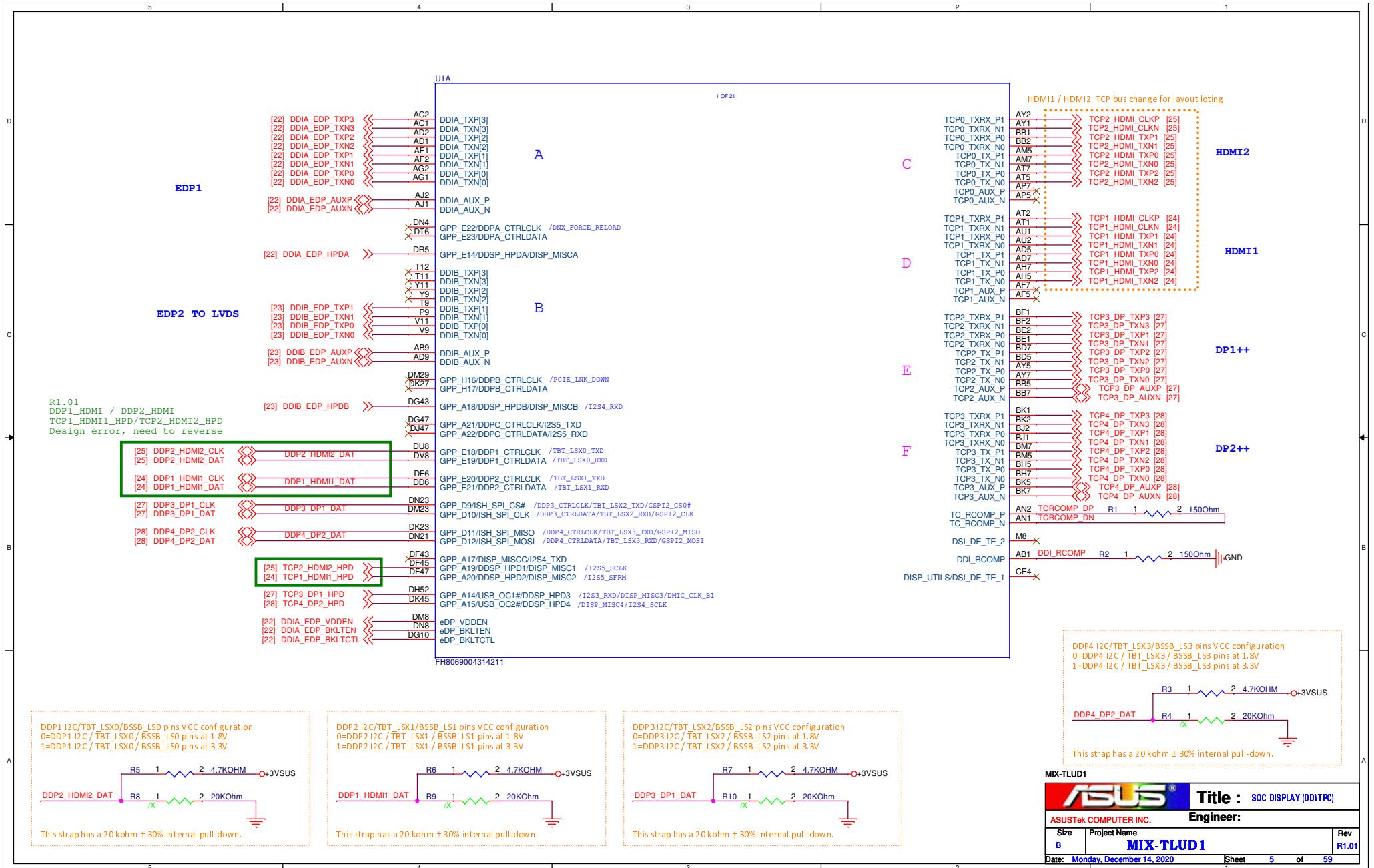


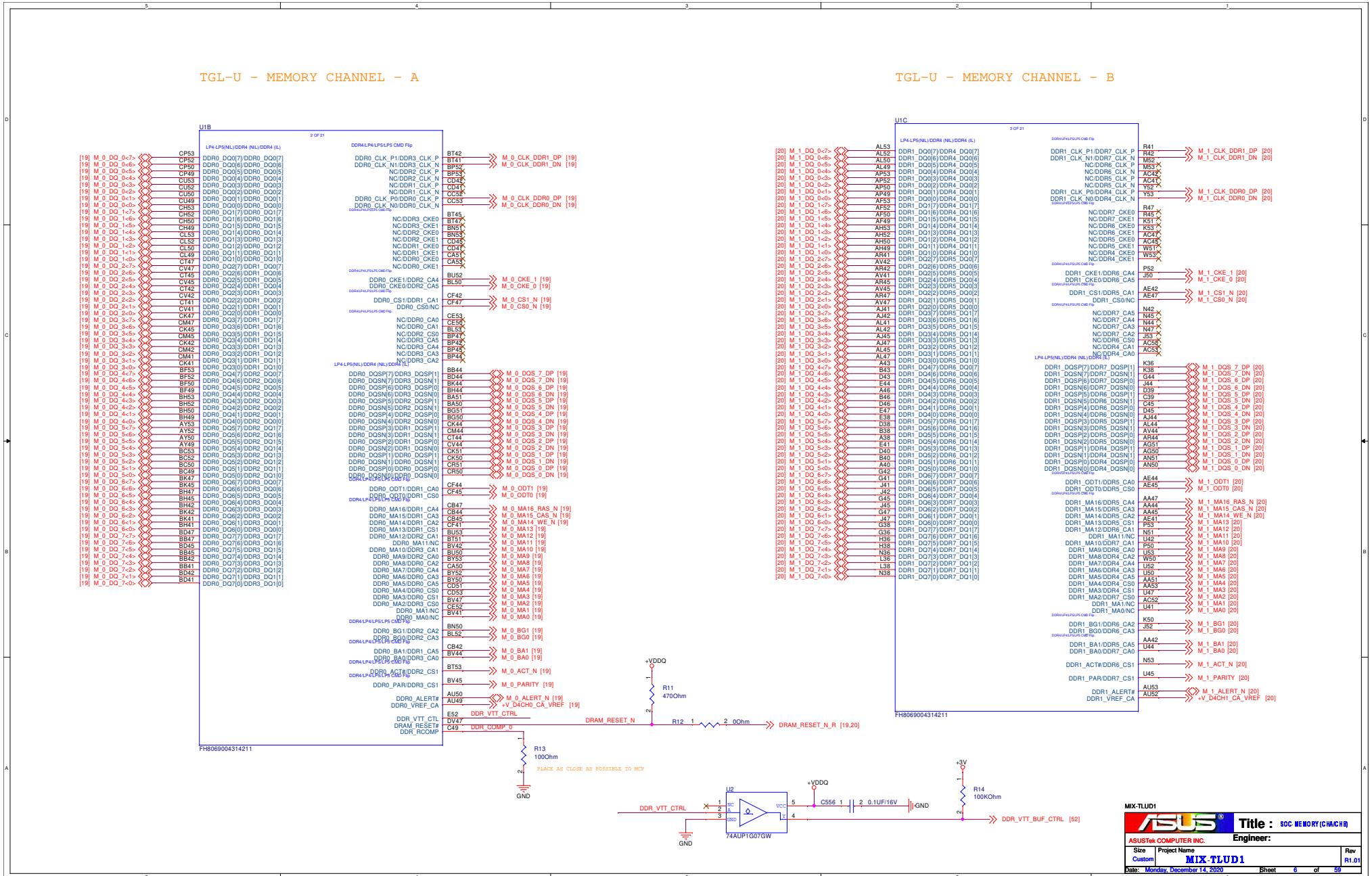
Tiger Lake G3 to S0 power on sequence (Non-Deep Sx Platform)

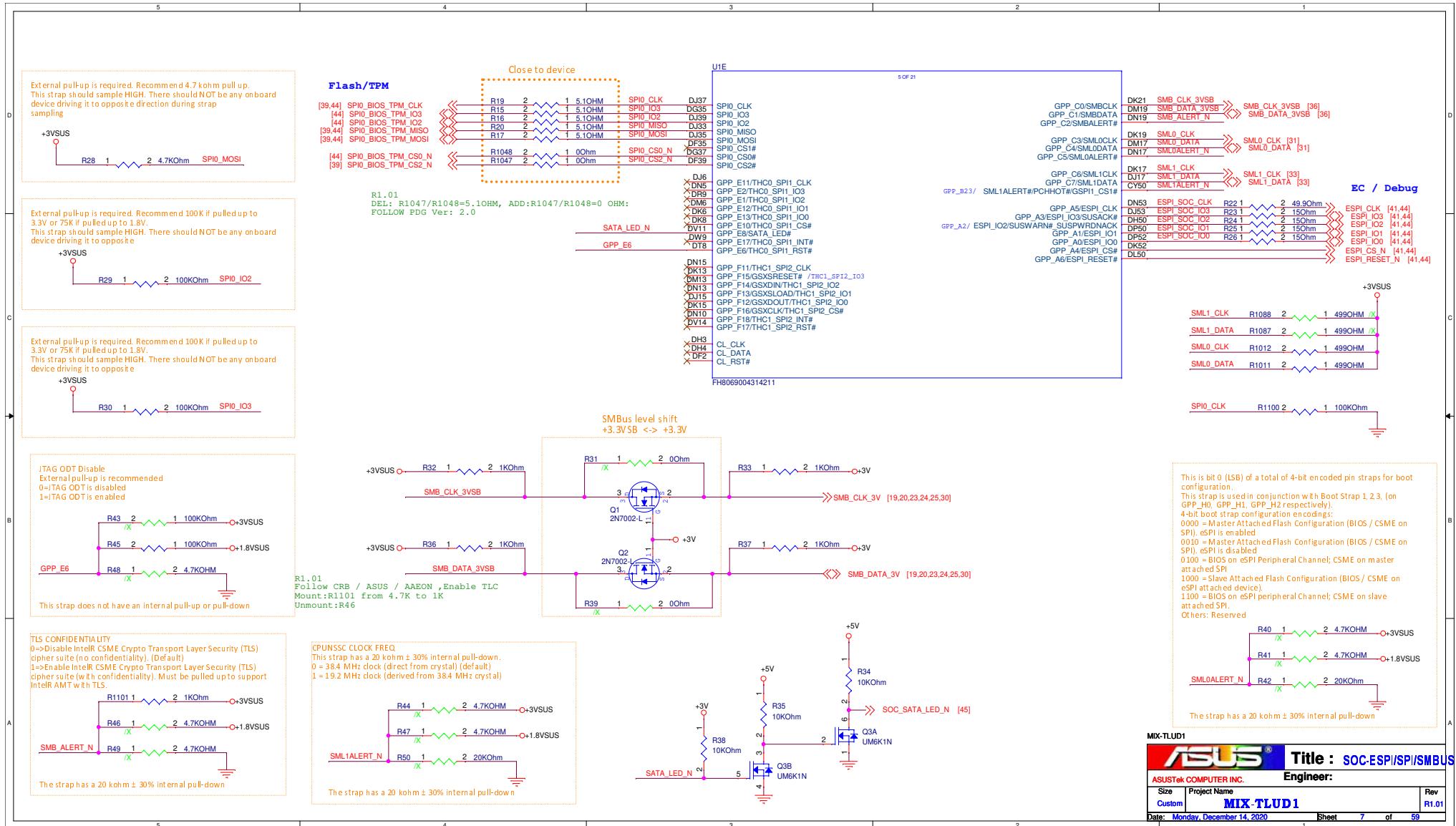


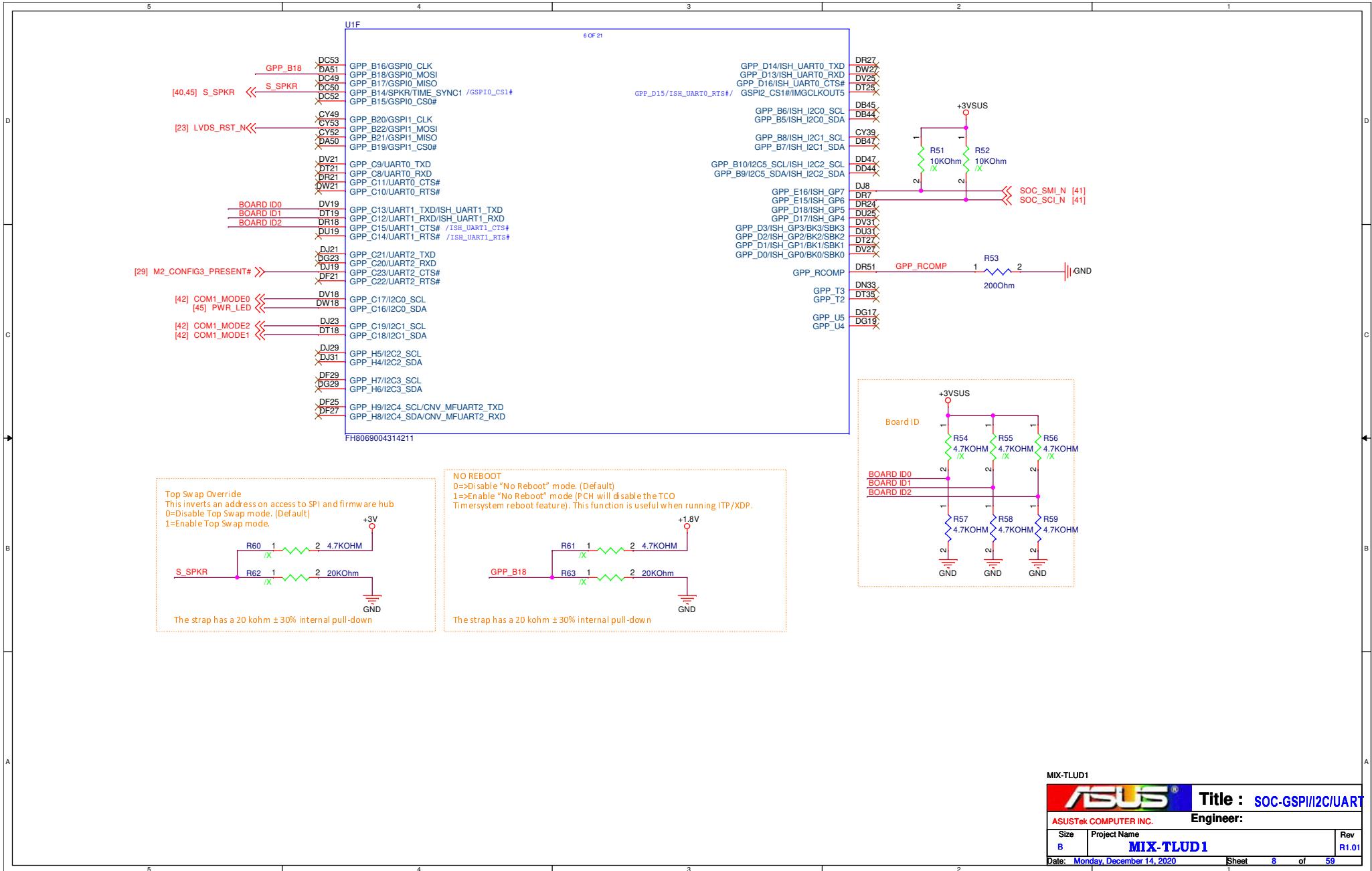


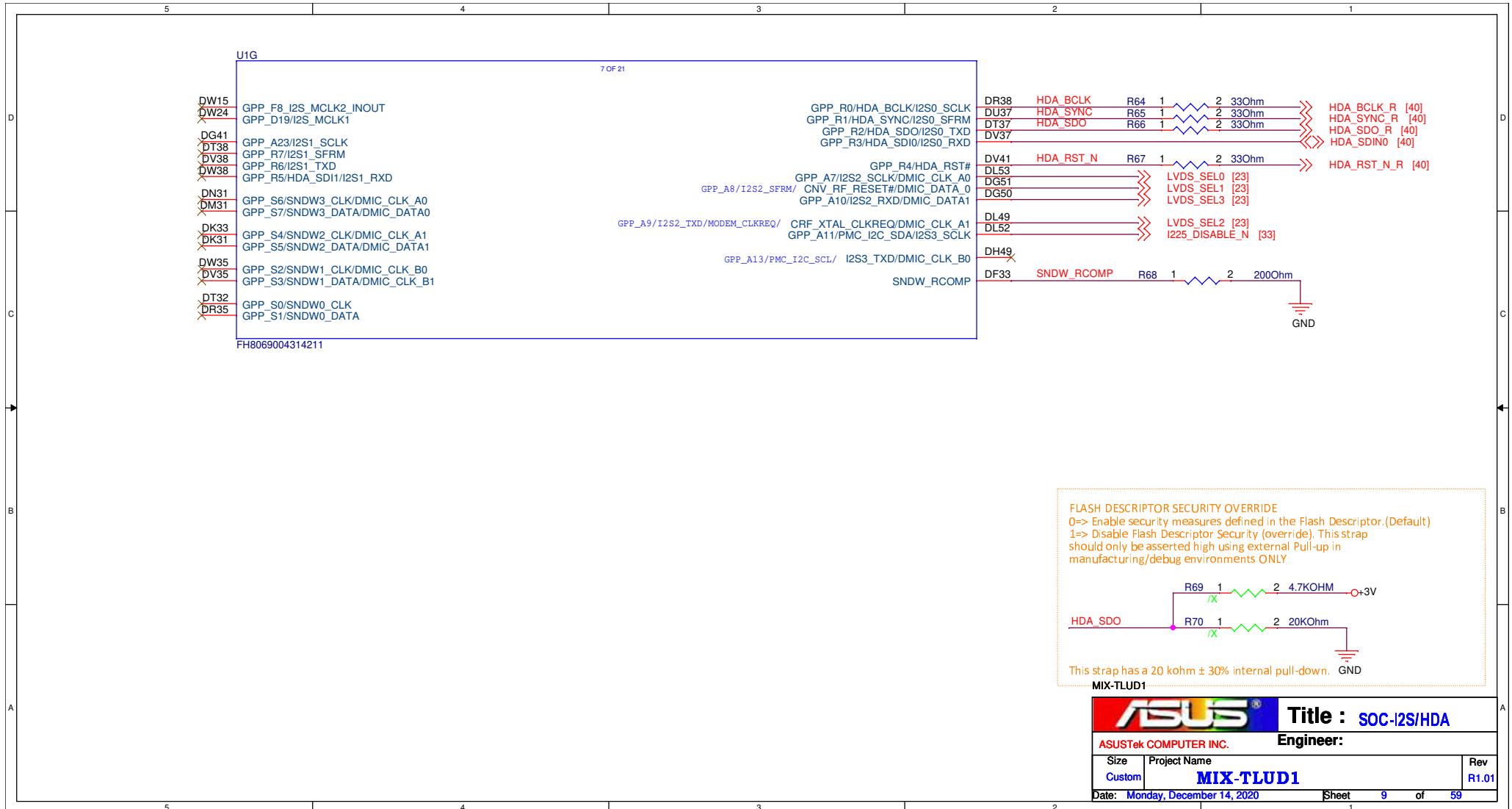


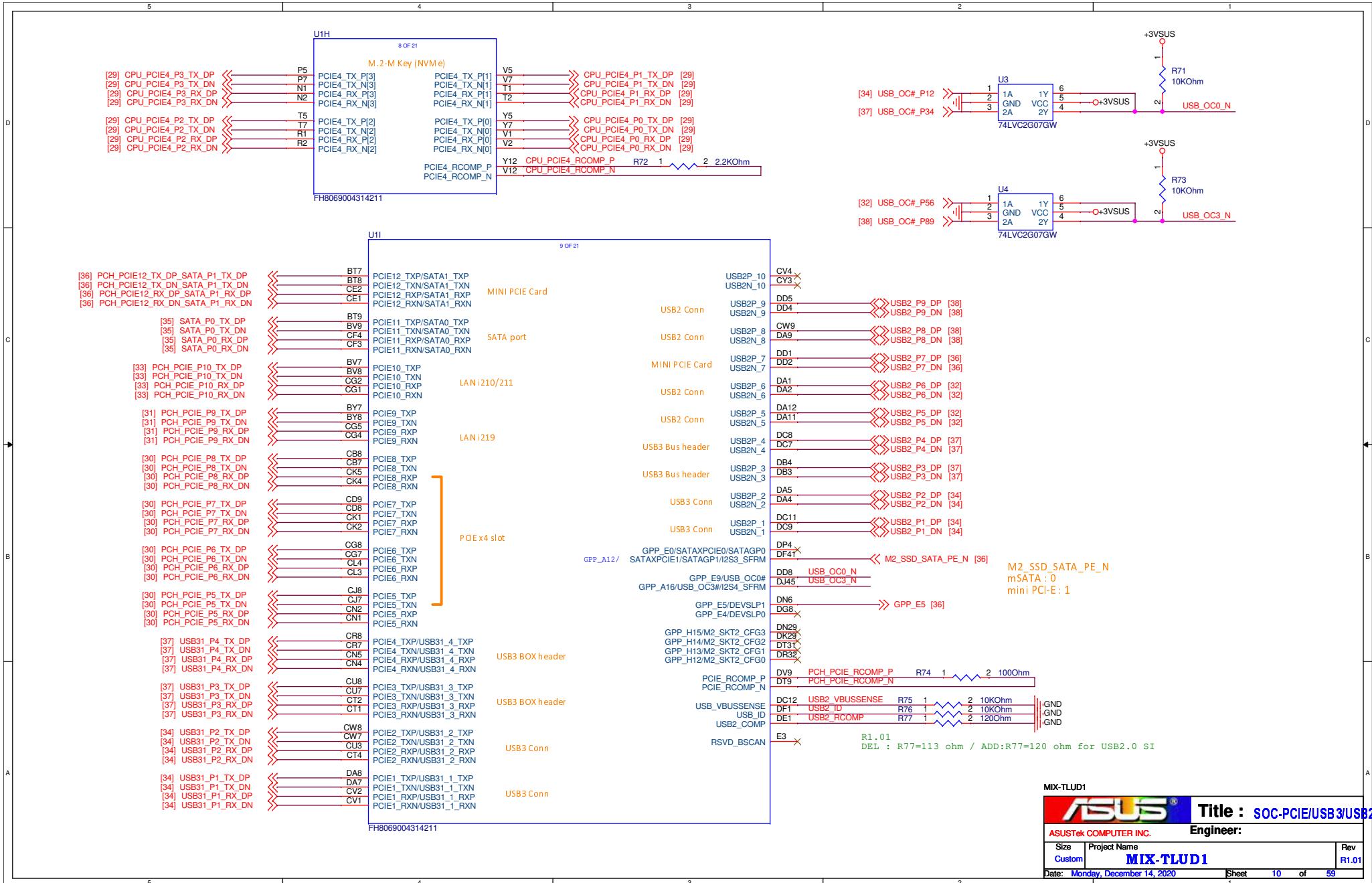


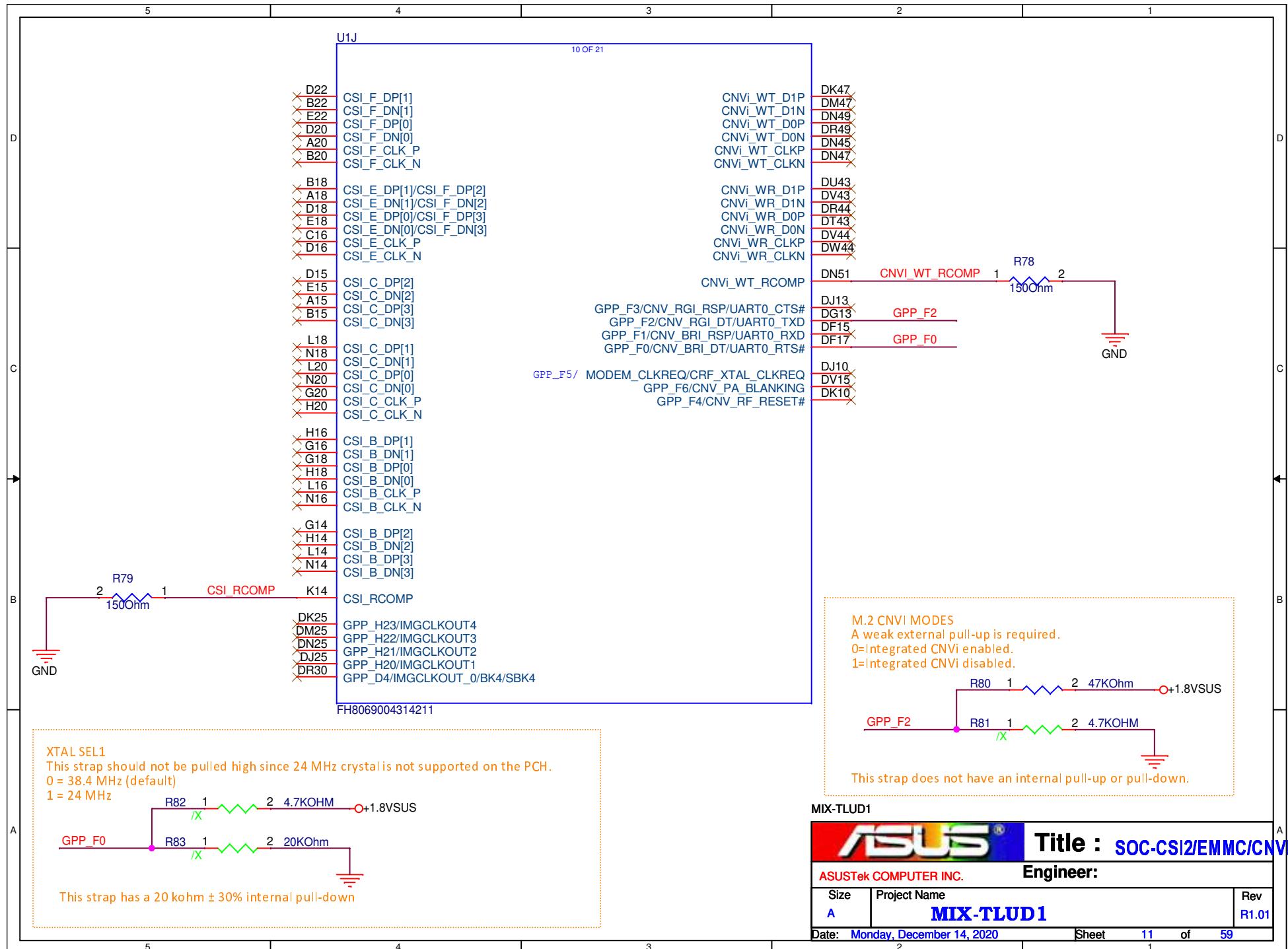


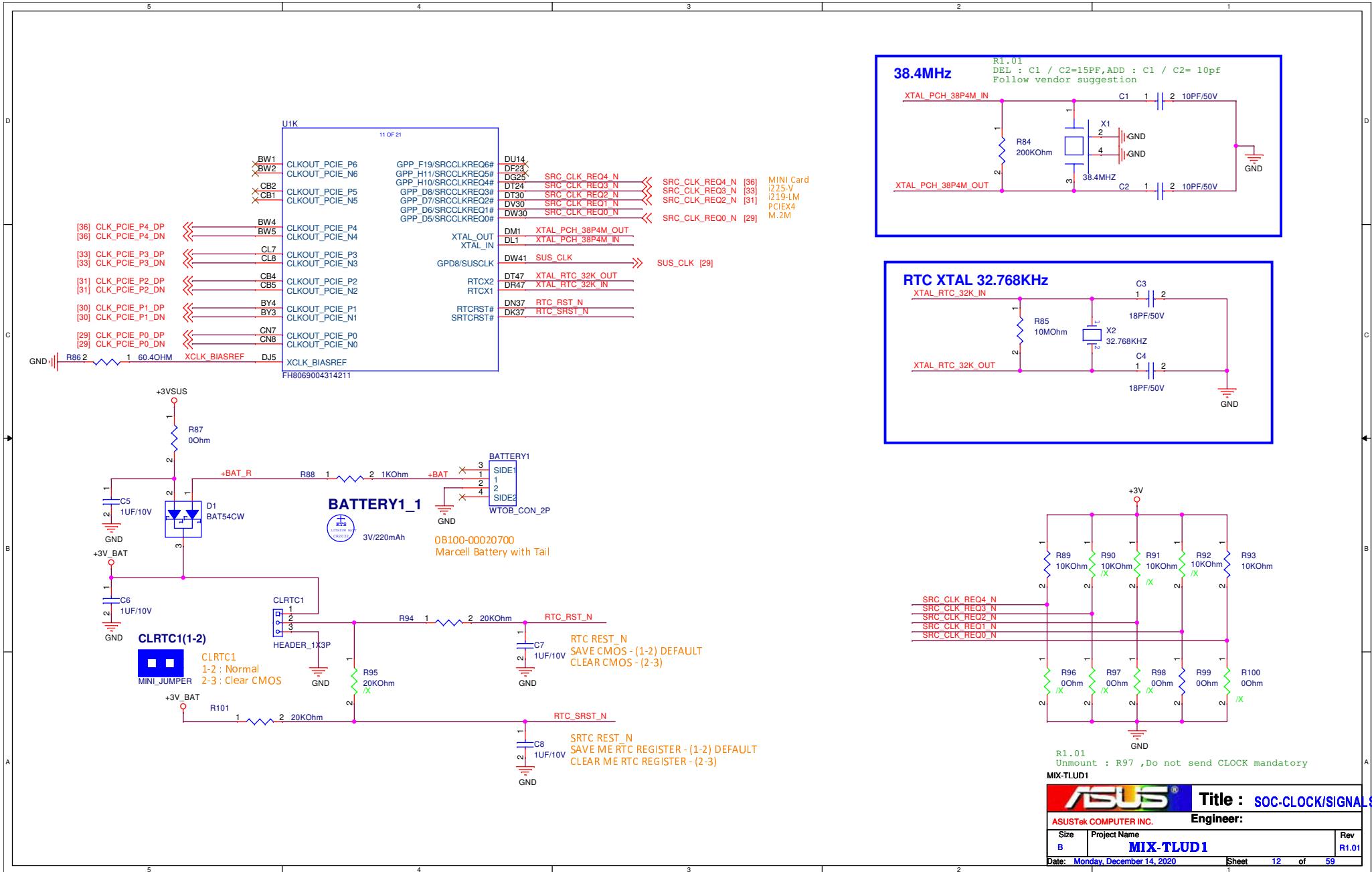


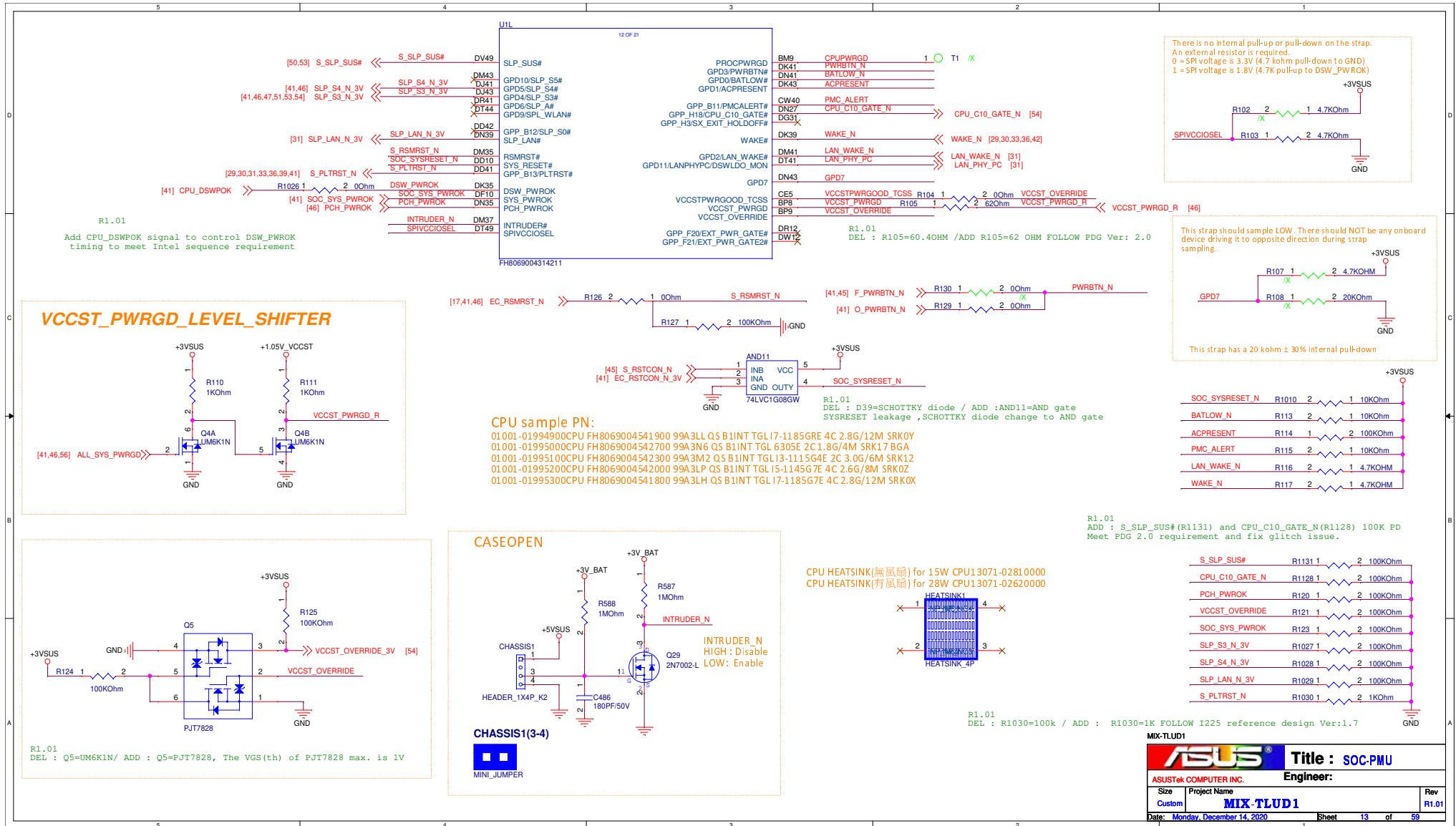


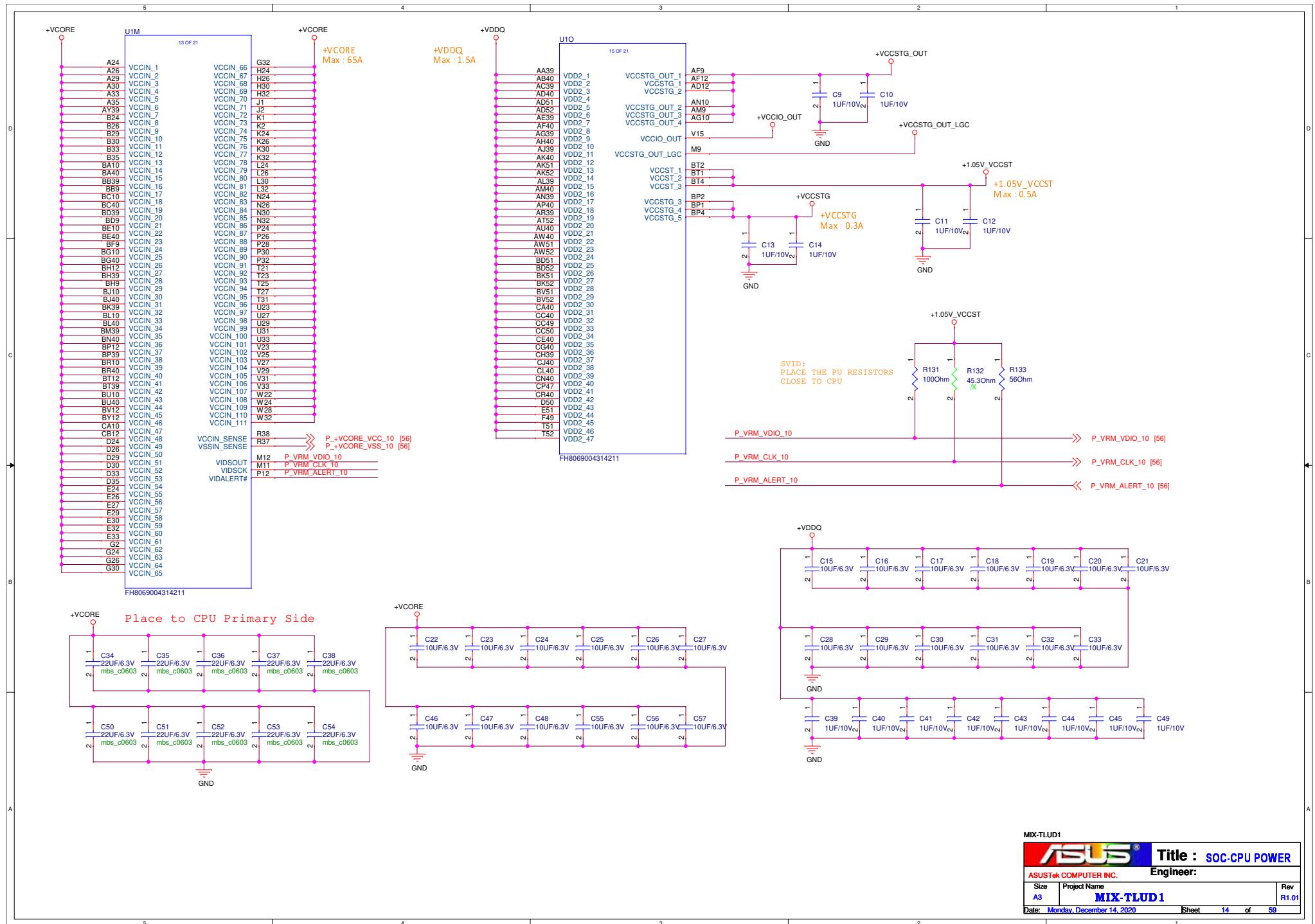


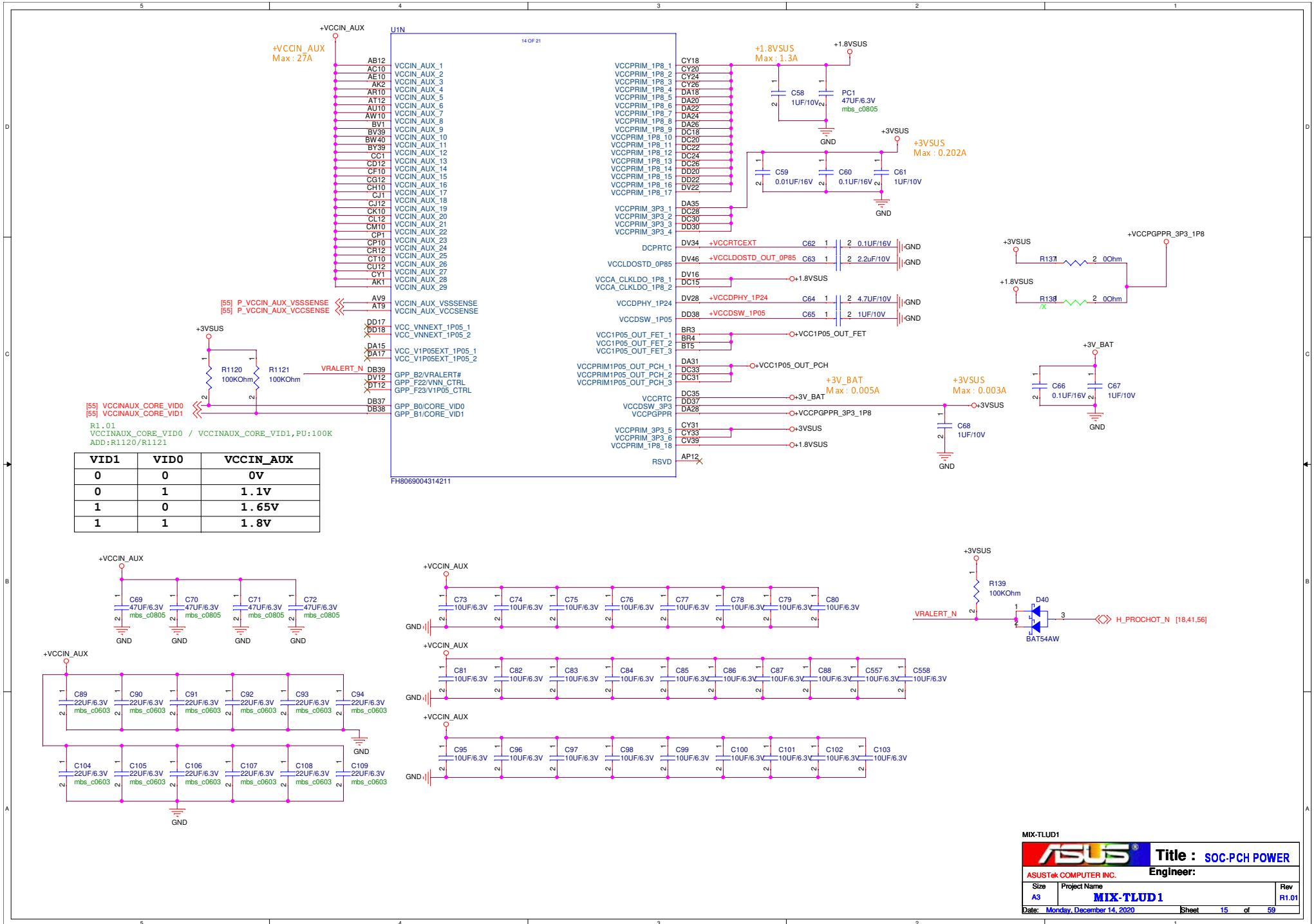


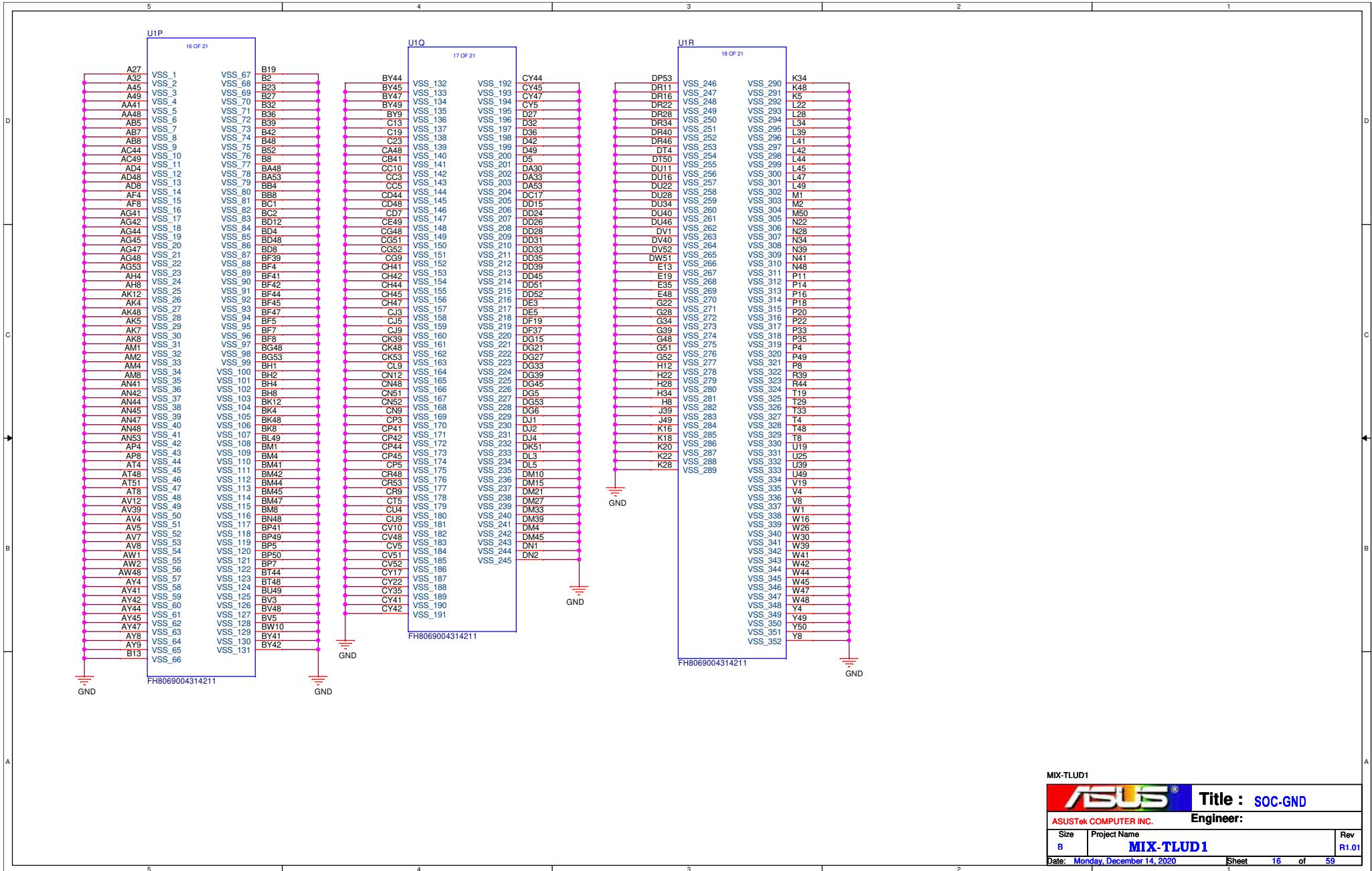


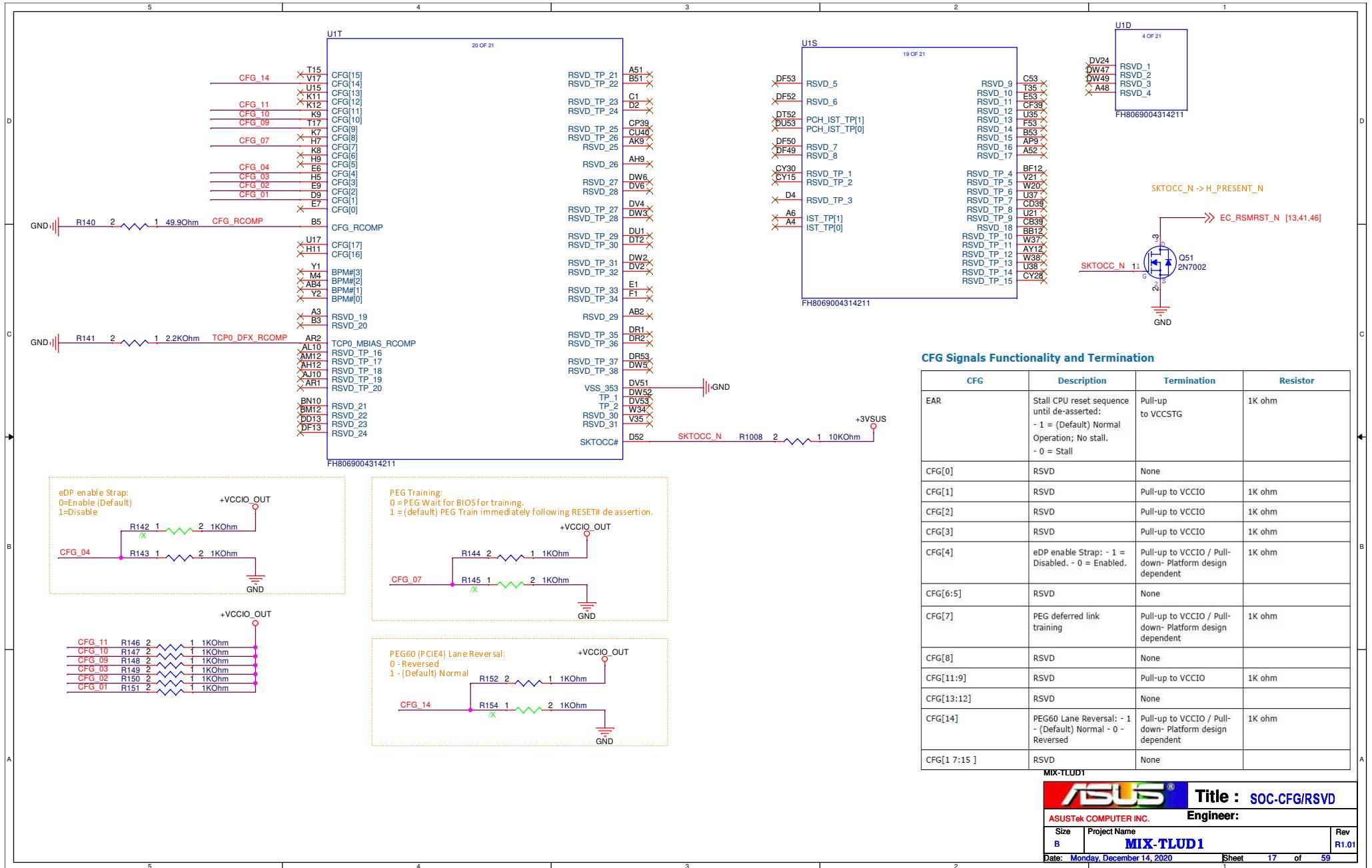


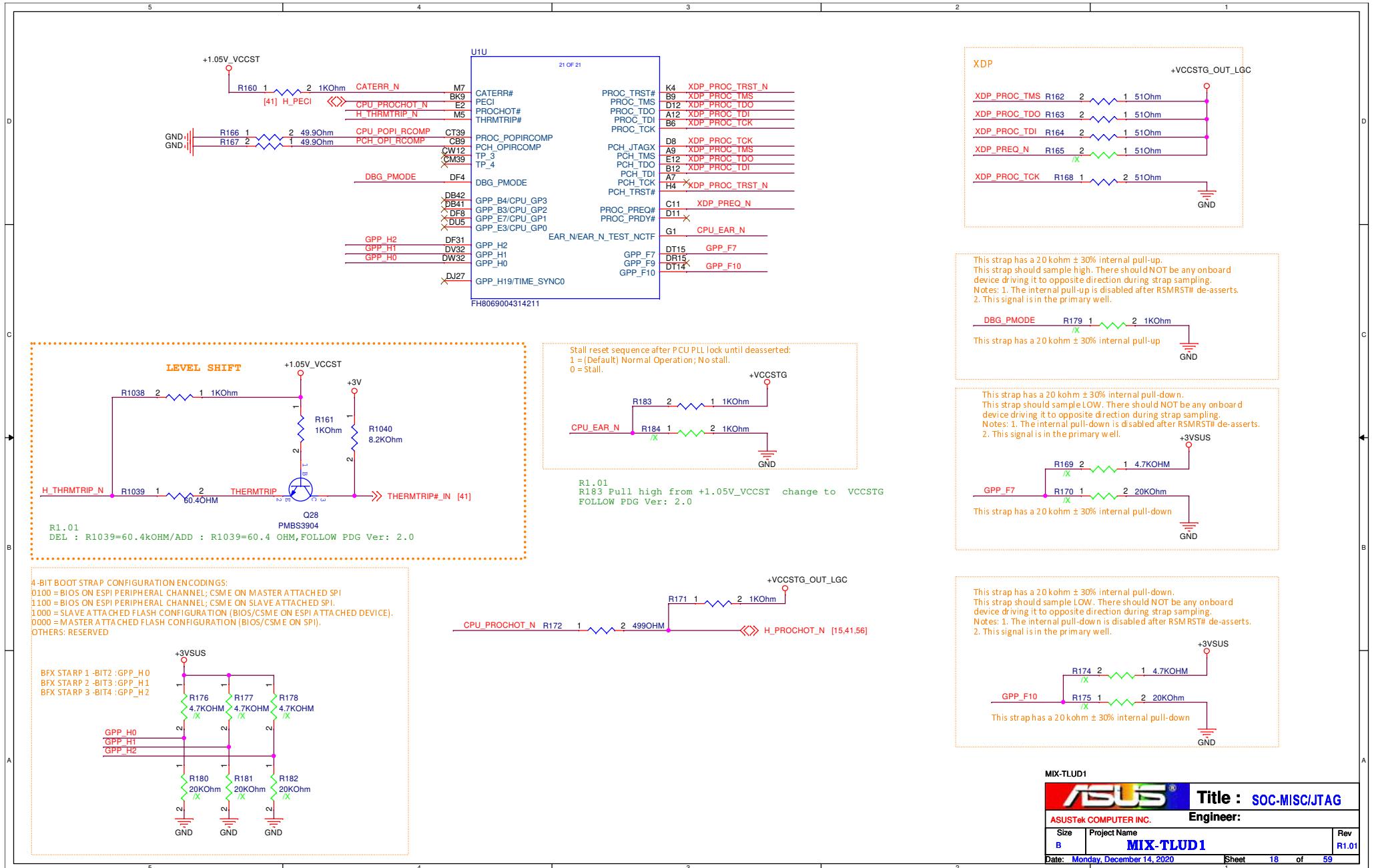




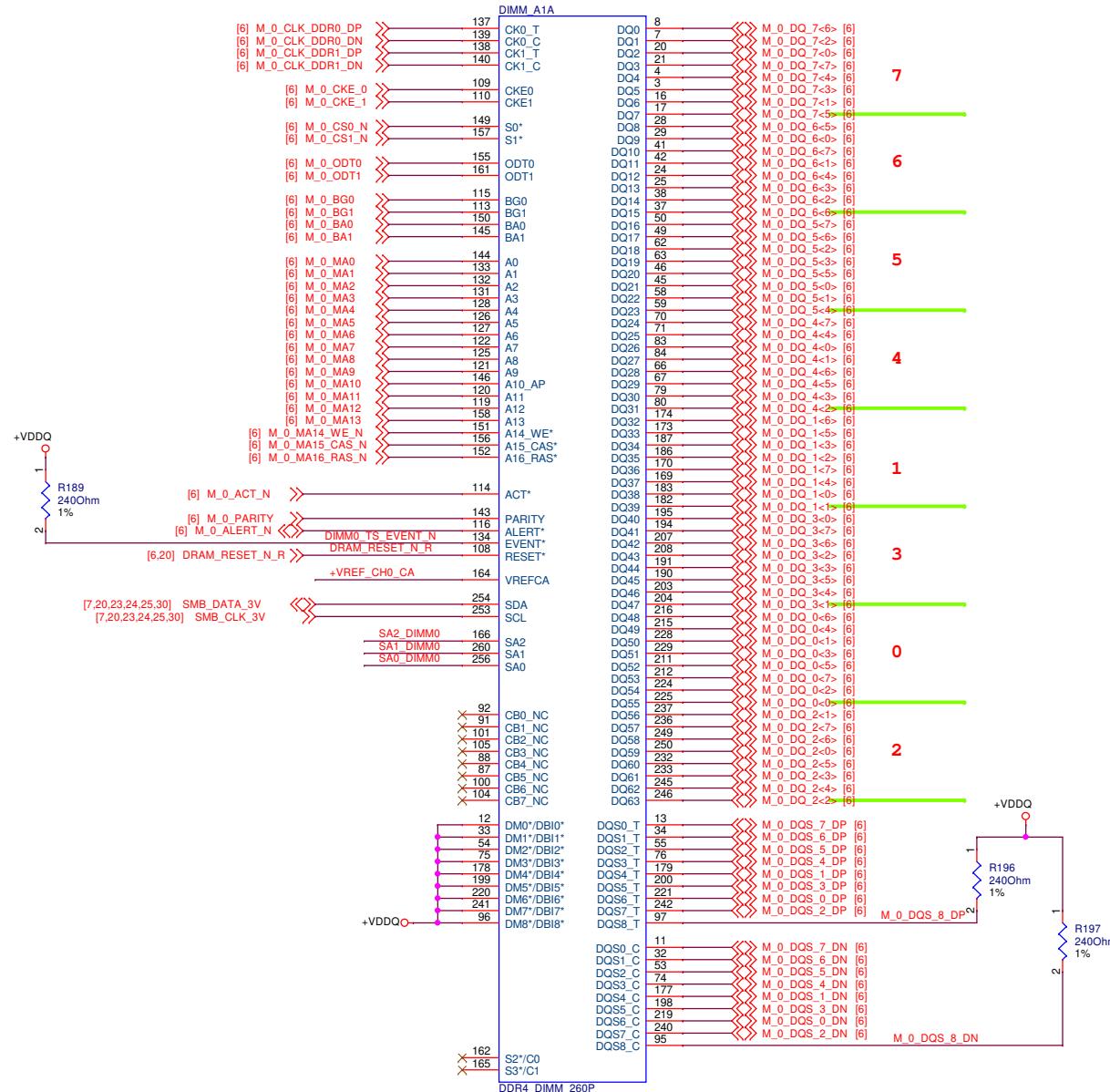




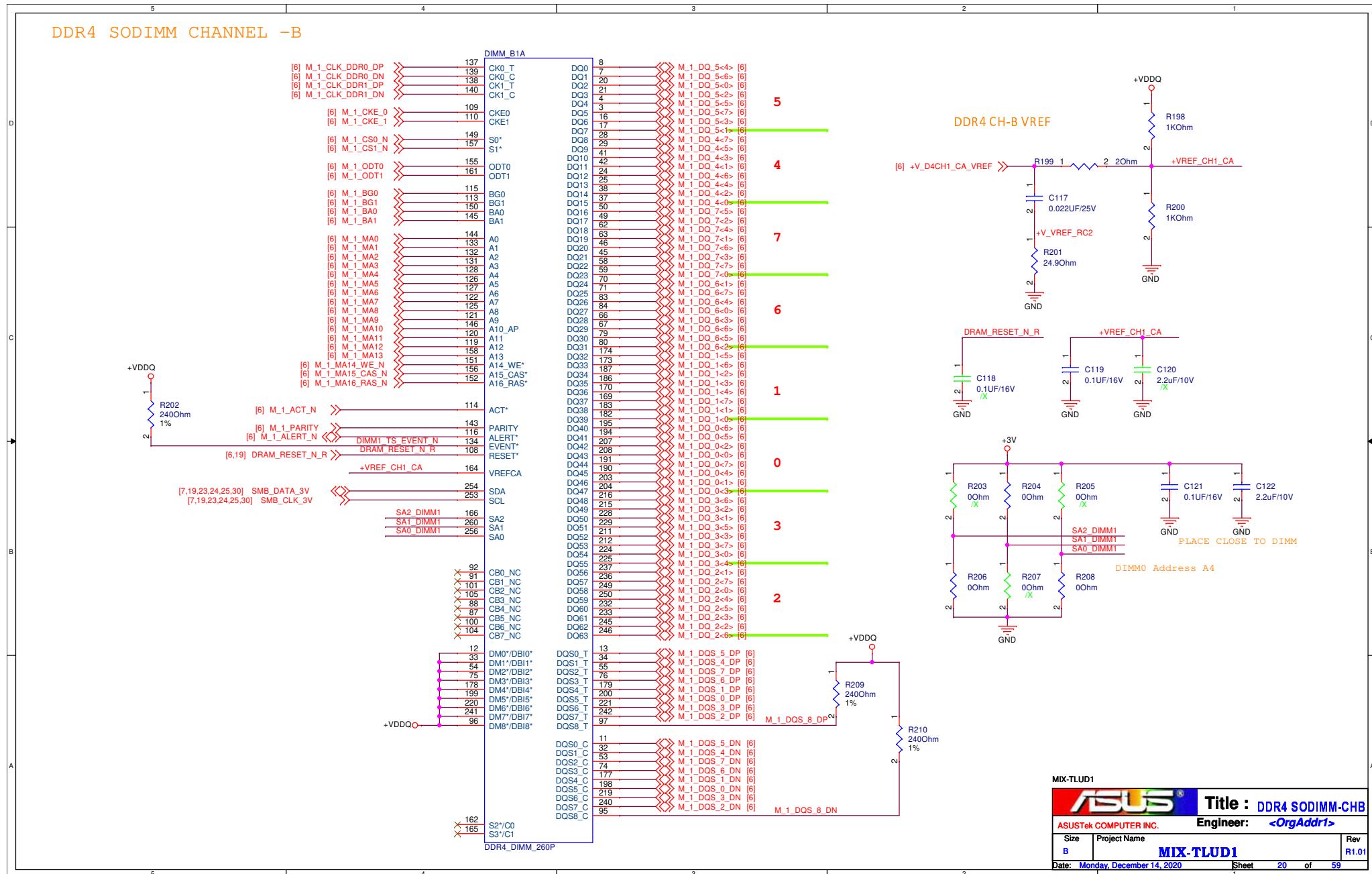


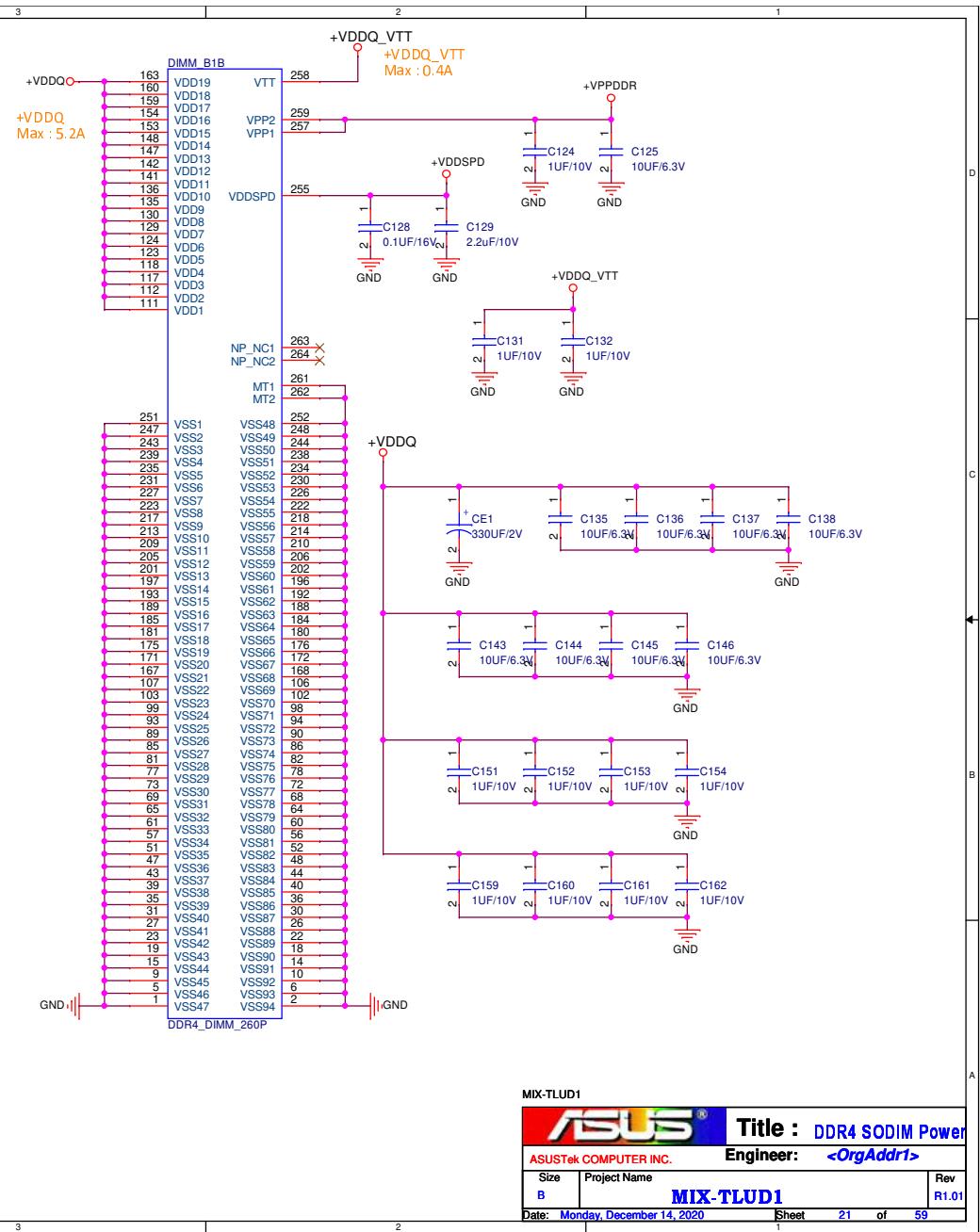
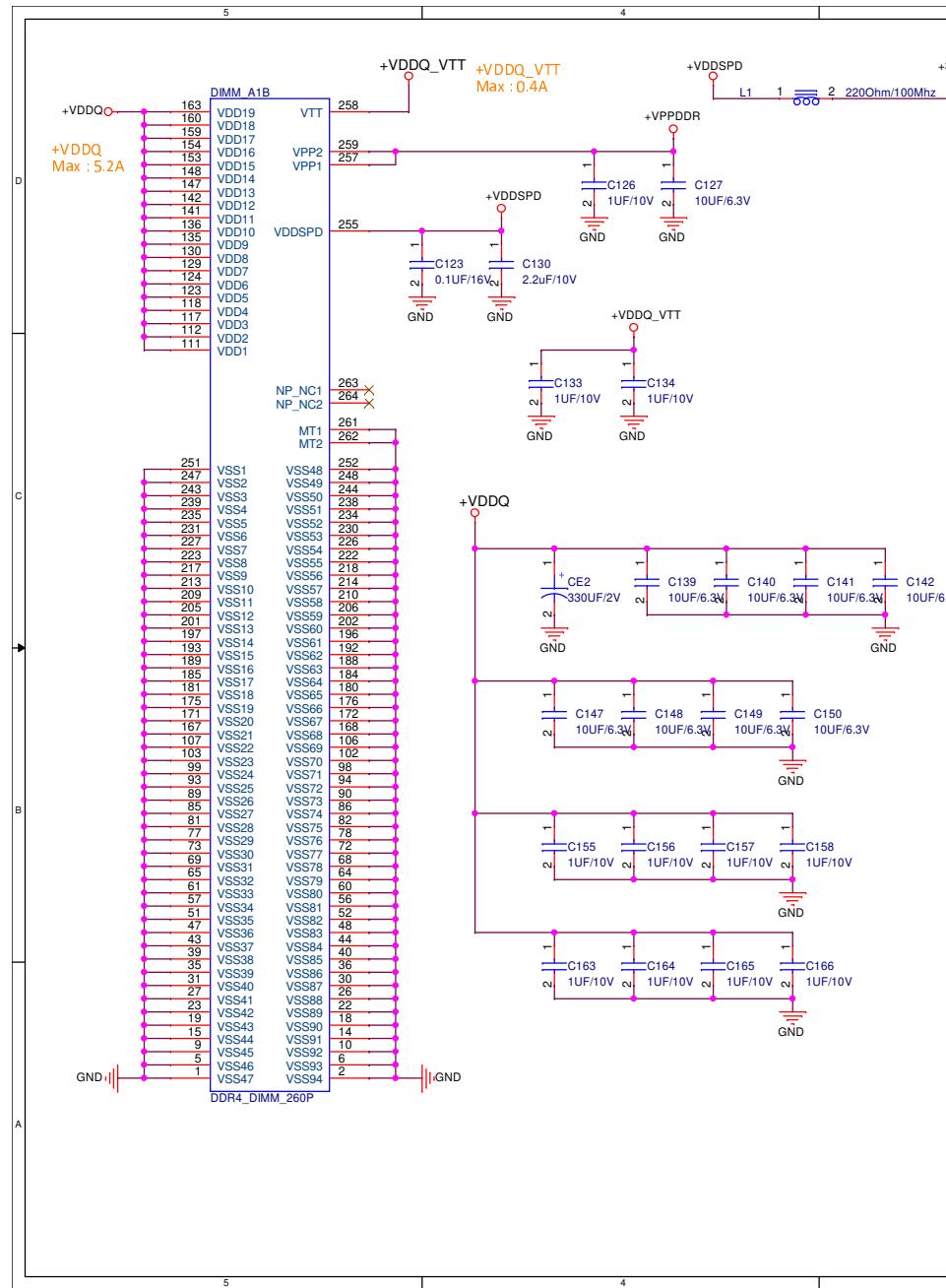


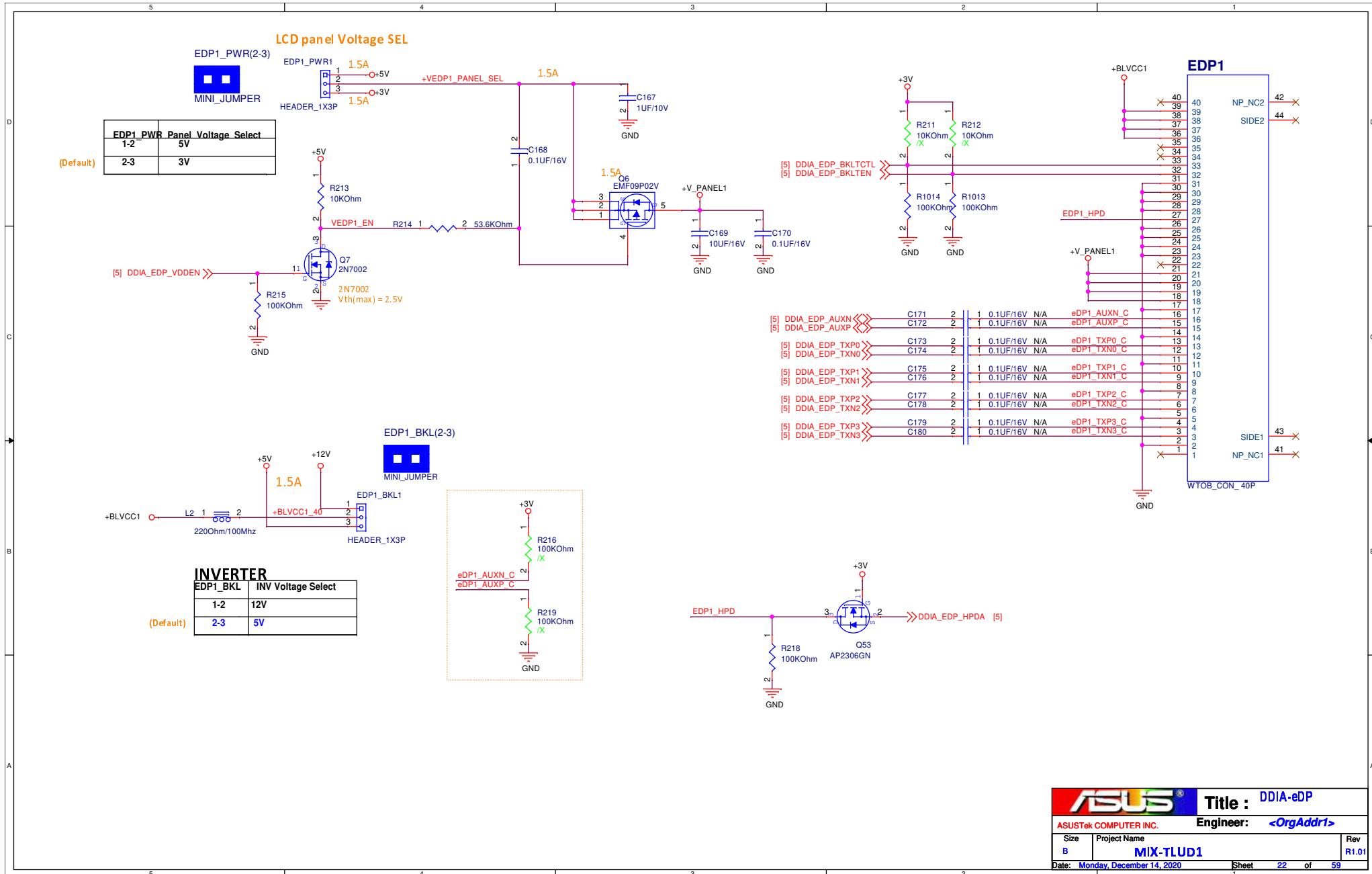
DDR4 SODIMM CHANNEL -A

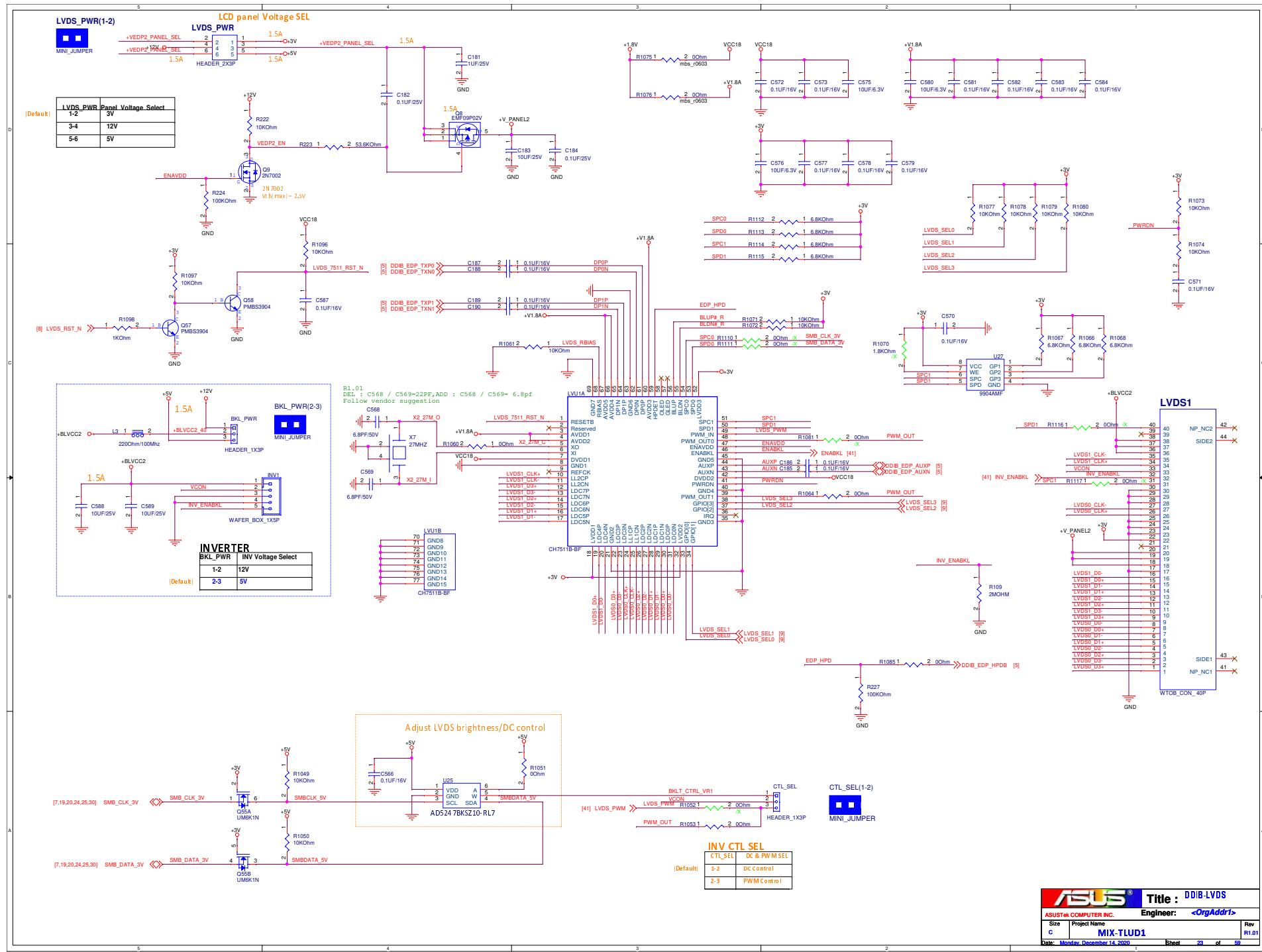


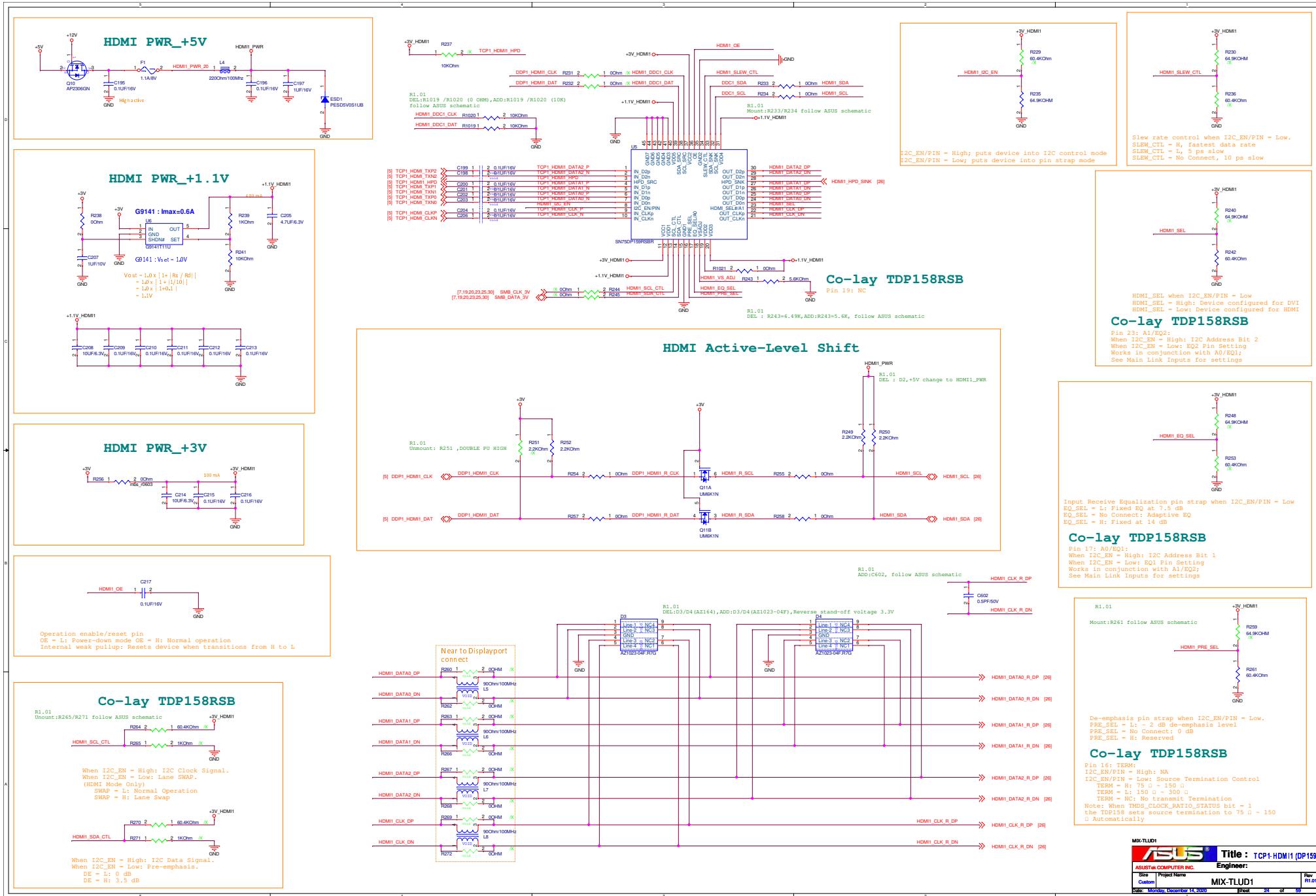
Title : DDR4 SODIMM-CHA	
ASUSTek COMPUTER INC.	Engineer: <OrgAddr1>
Size B	Project Name MIX-TLUD1
Date: Monday, December 14, 2020	Sheet 1 of 59
Rev R1.01	

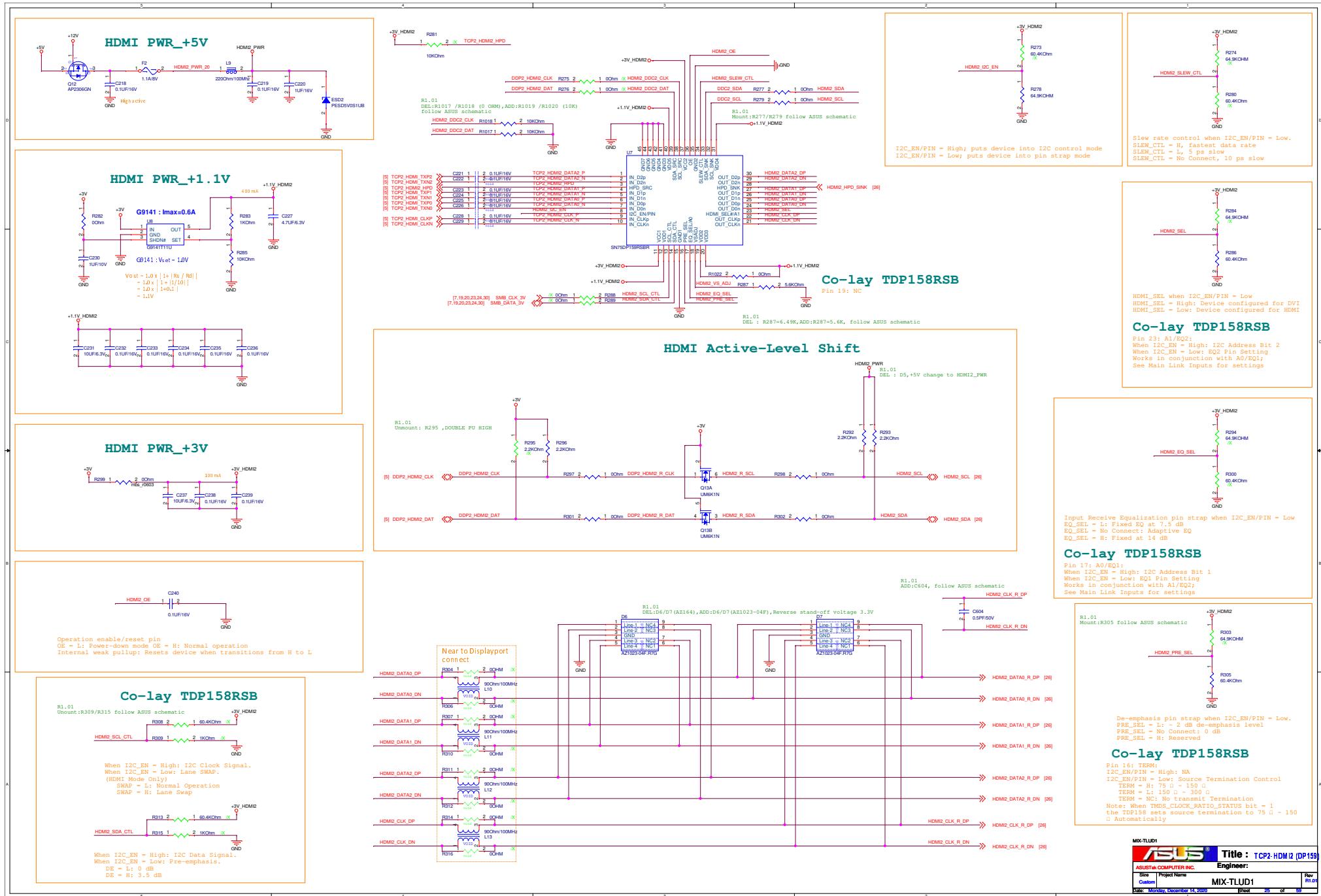


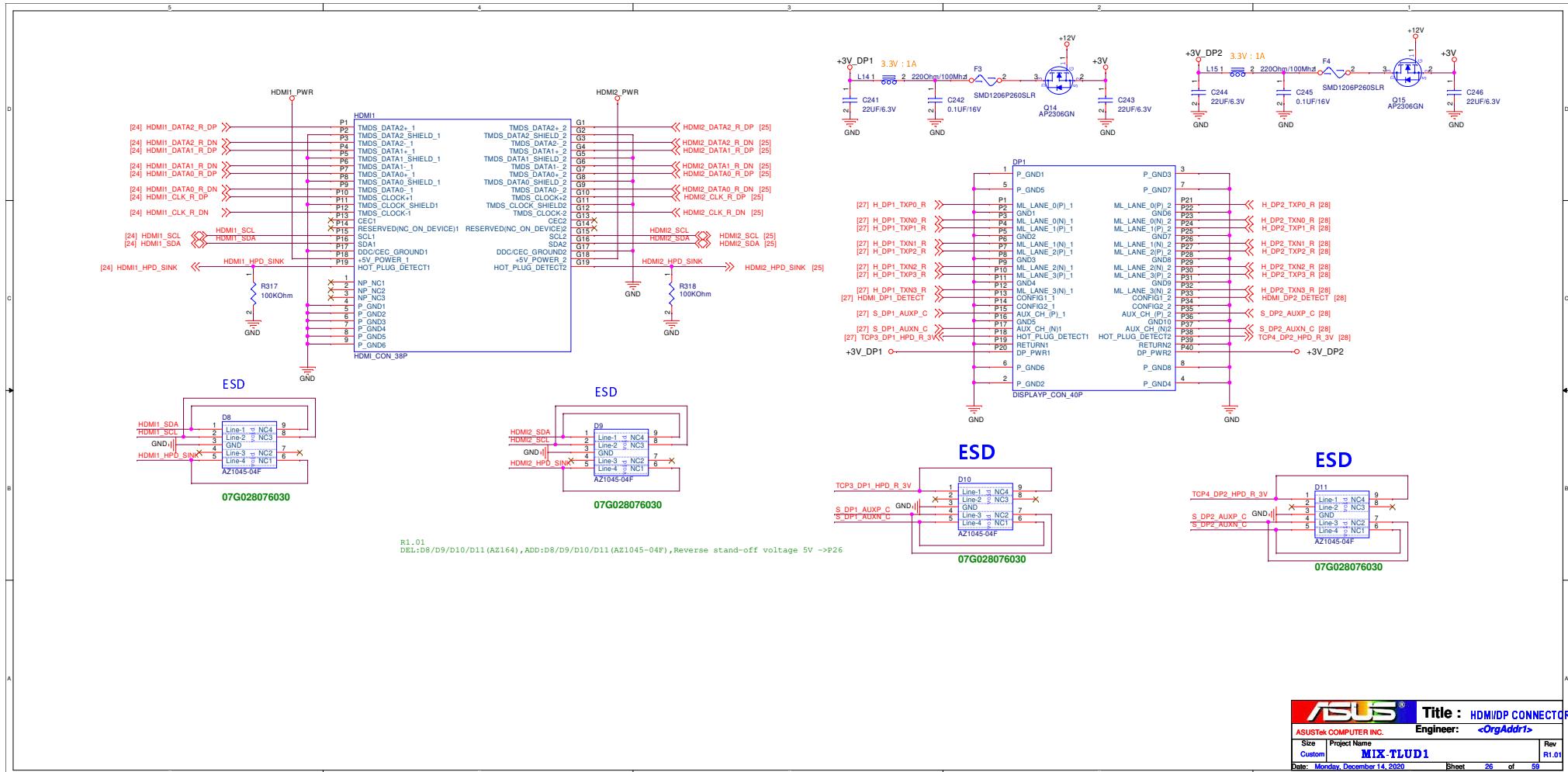




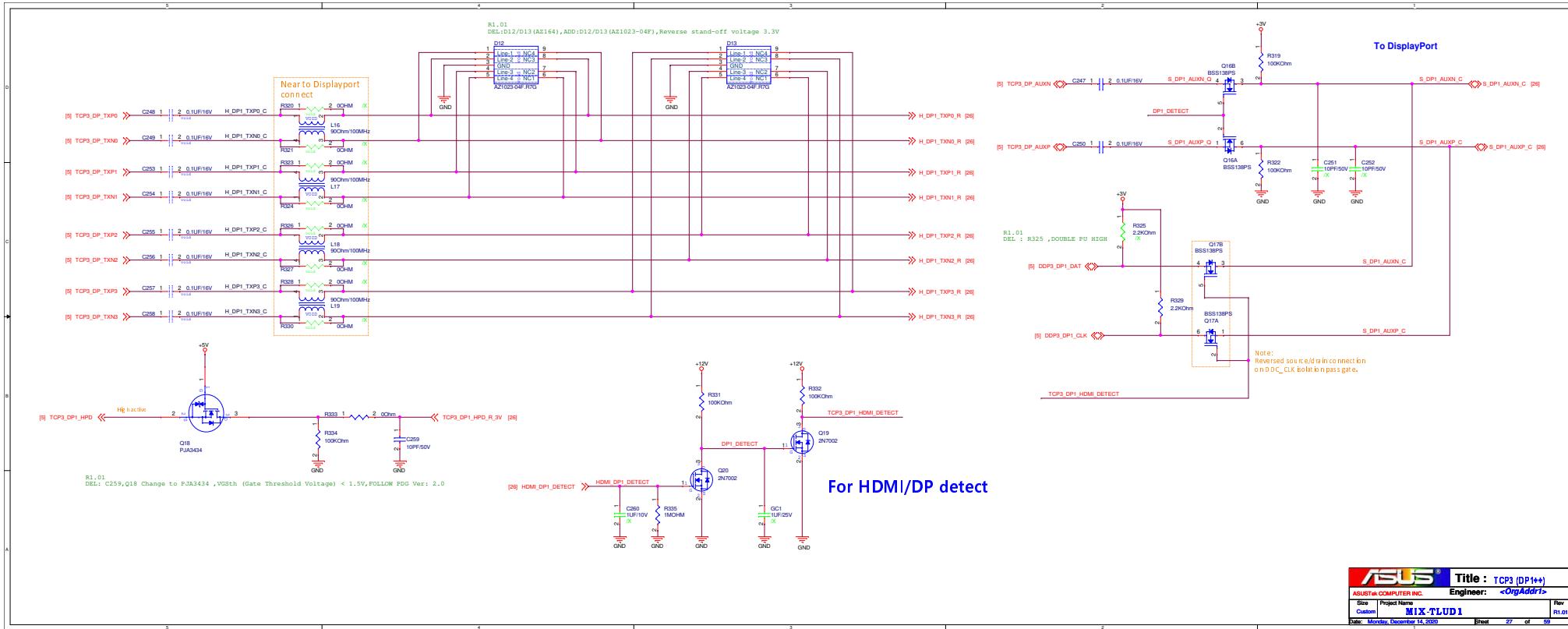


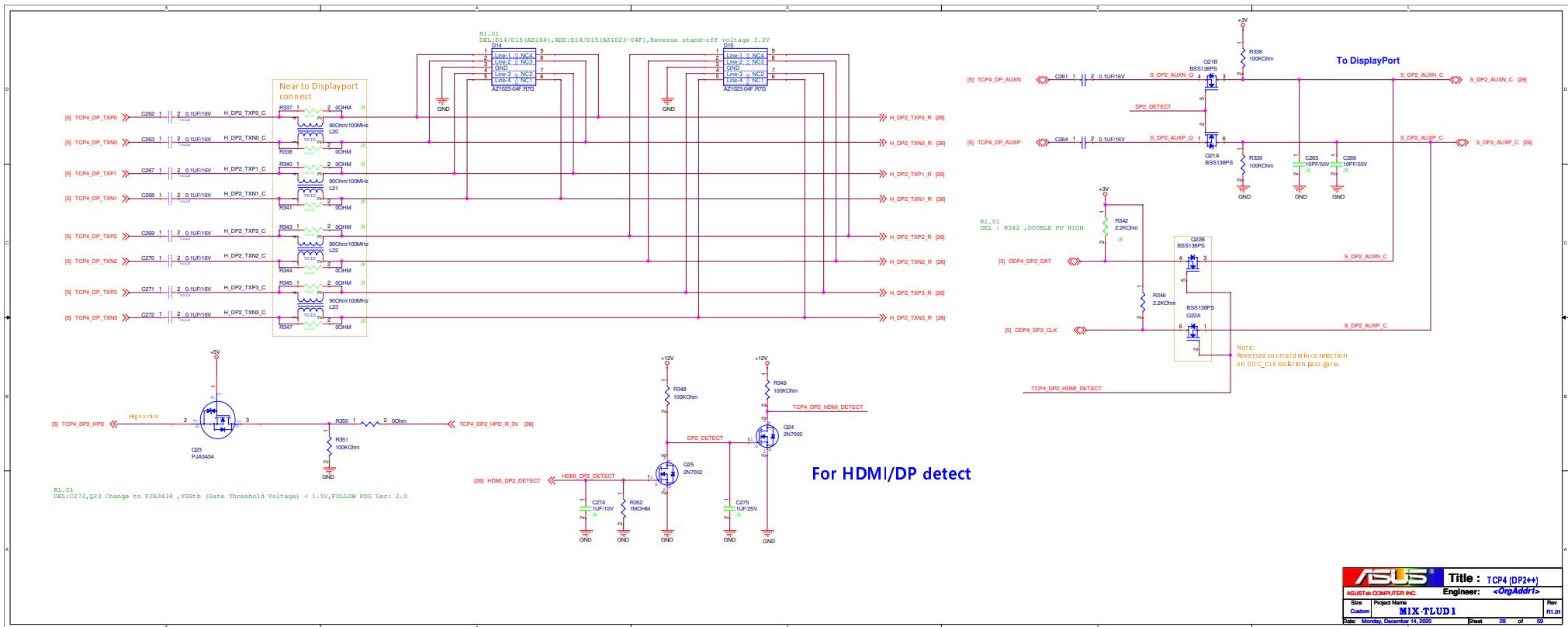


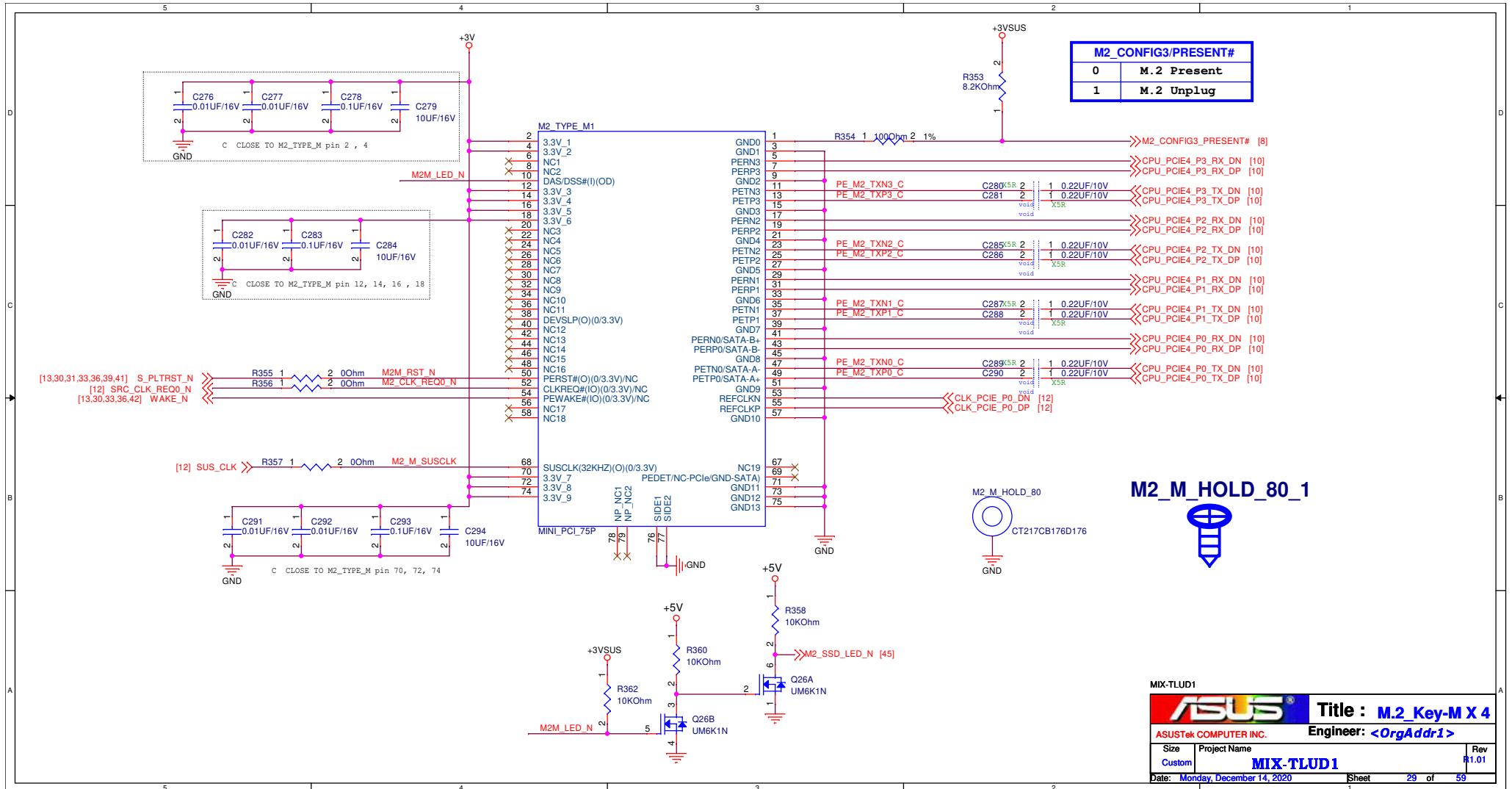


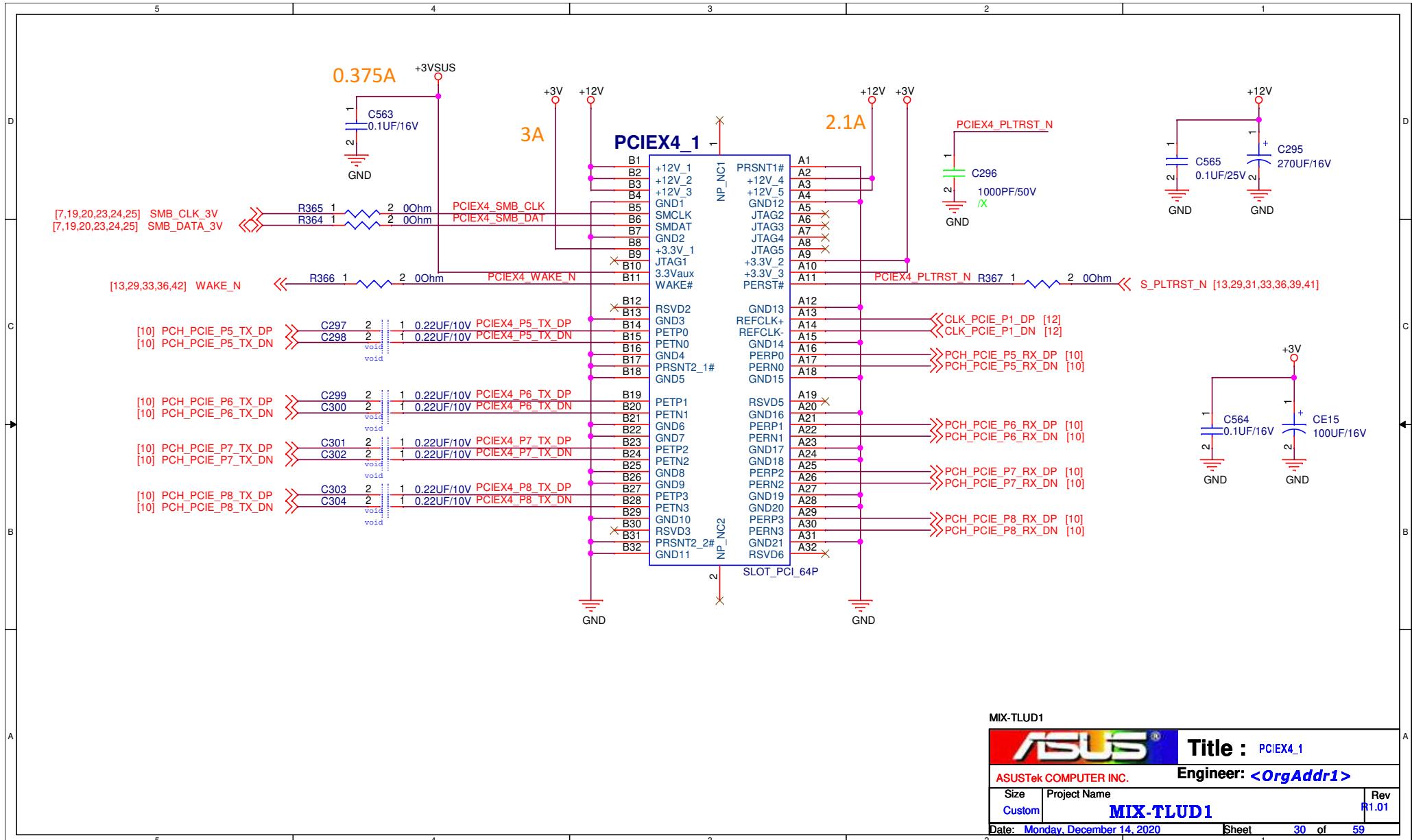


ASUS® Title : HDMI/DP CONNECTOR
ASUSTek COMPUTER INC. Engineer: <OrgAddr>
Size Custom Project Name MIX_TLUD1 Rev R1.01
Date: Monday, December 14, 2020 Sheet 26 of 59



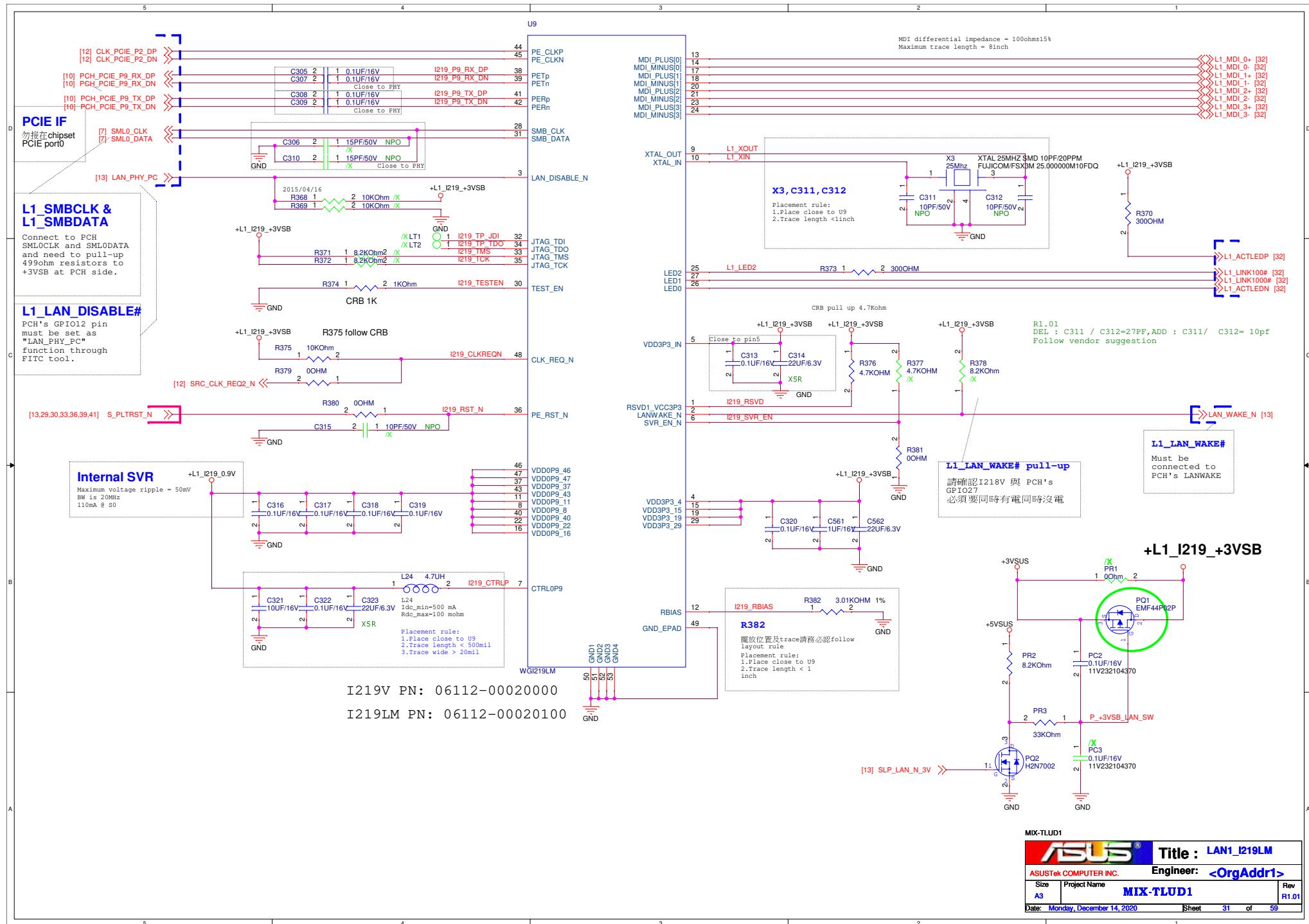


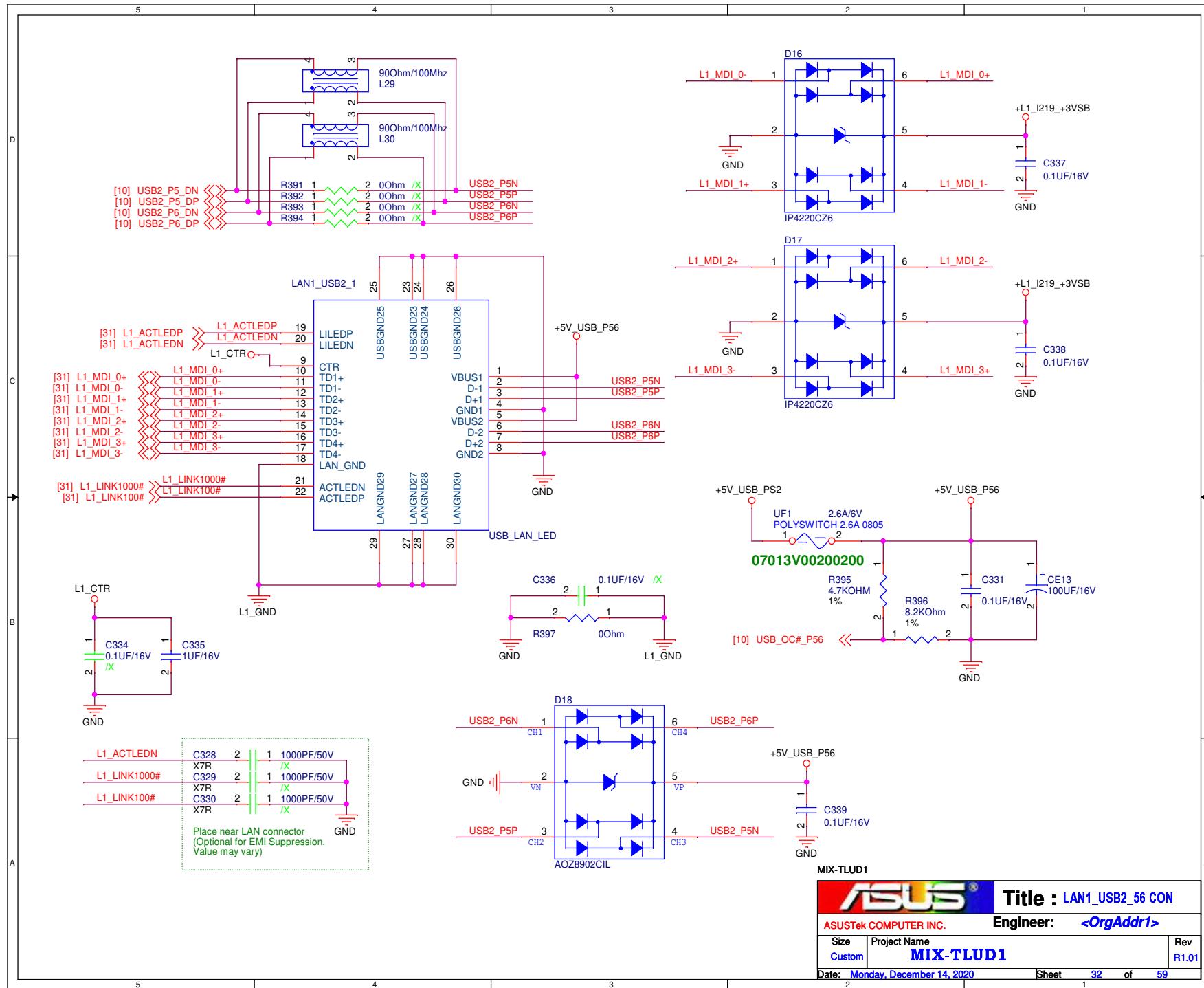


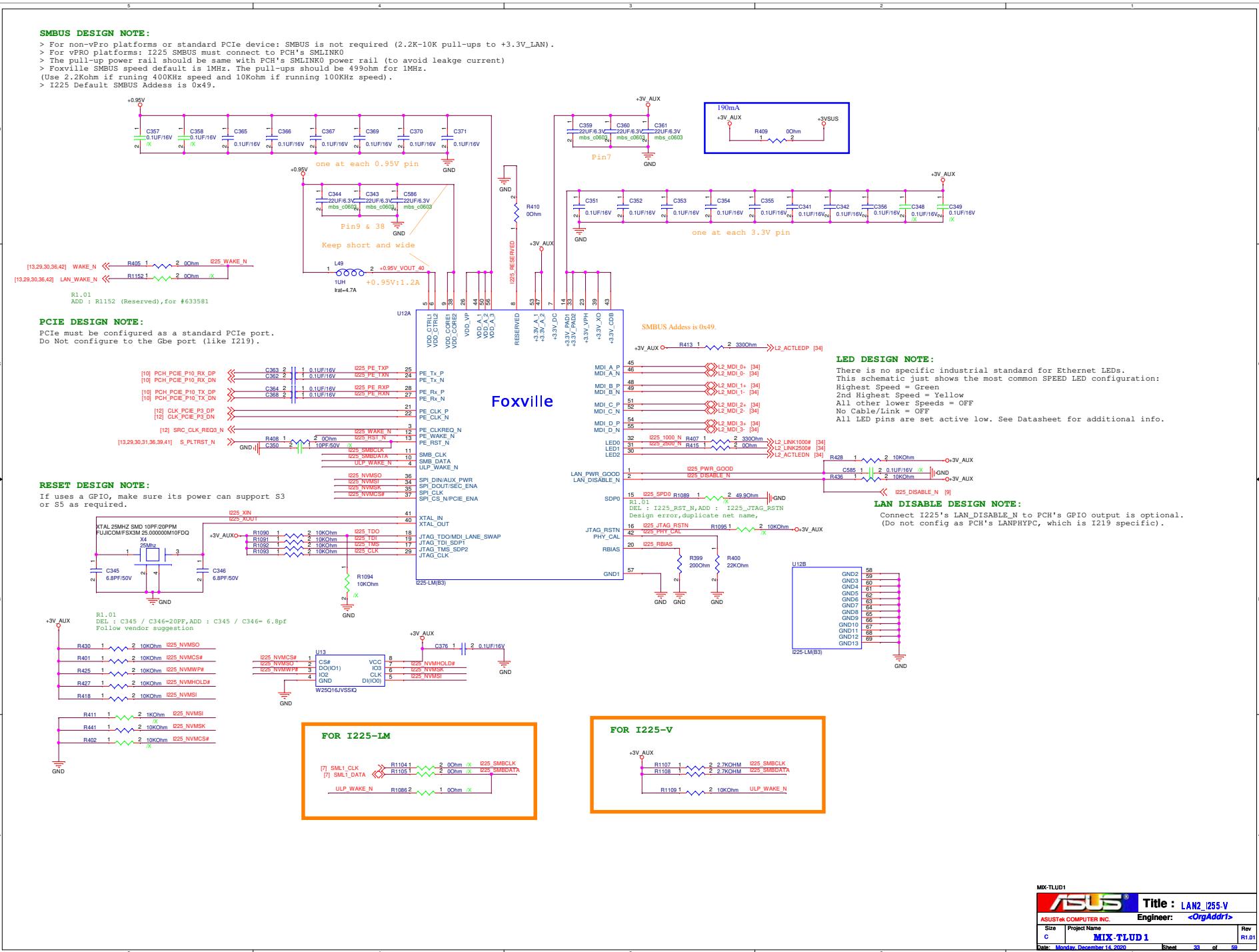


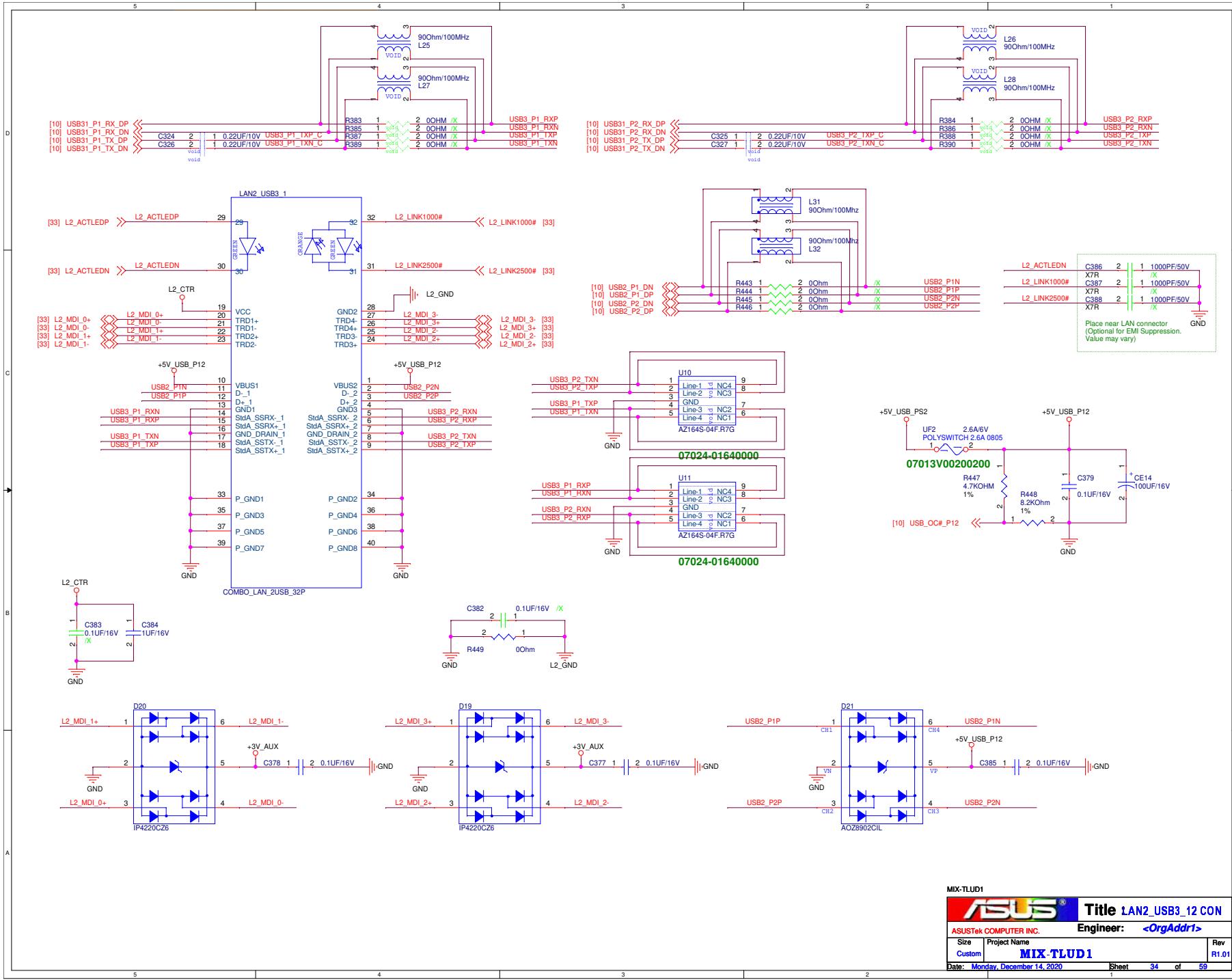
MIX-TLUD1

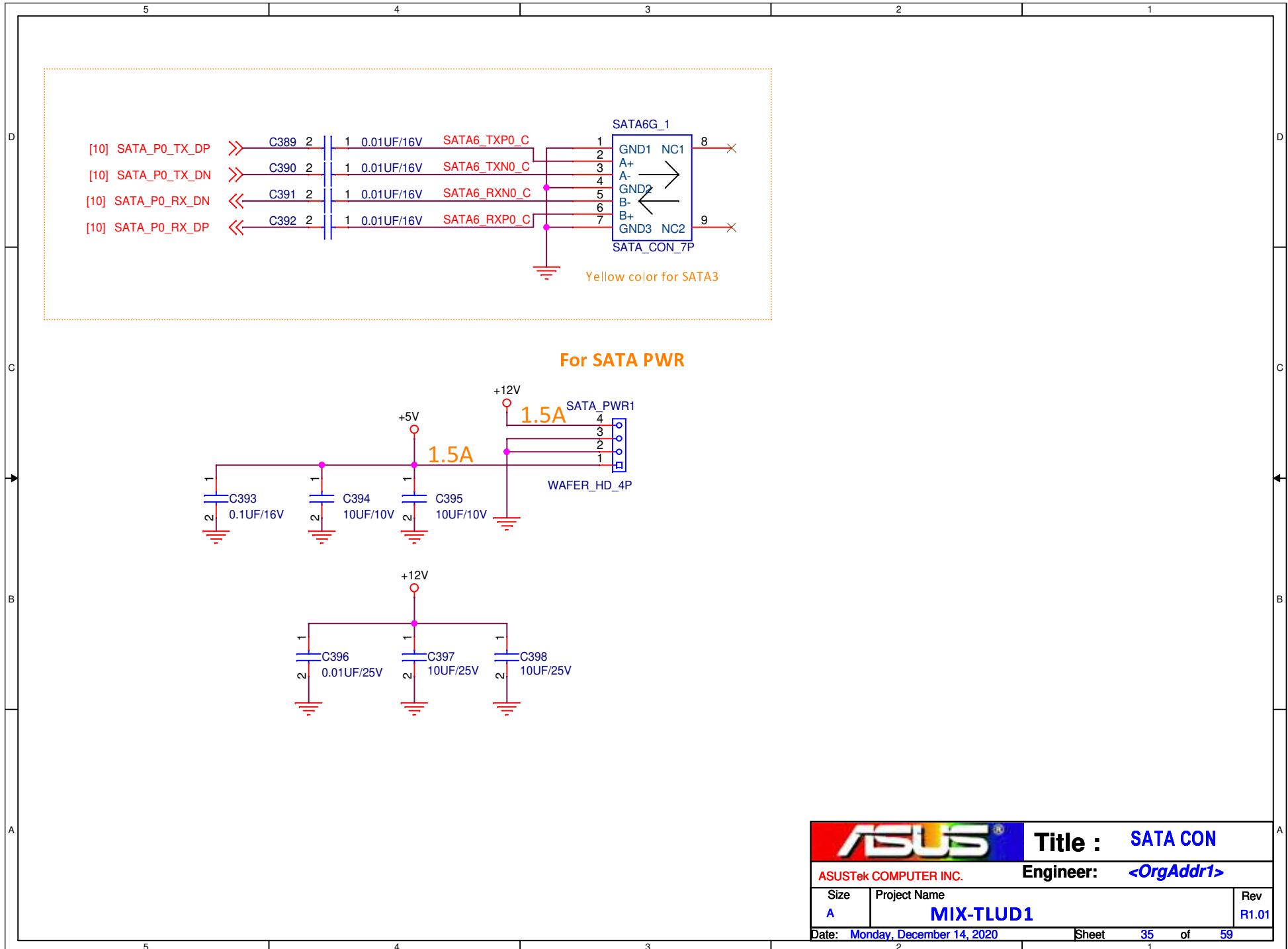
ASUS®		Title : PCIEX4_1
ASUSTek COMPUTER INC.		Engineer: <OrgAddr1>
Size	Project Name	Rev
Custom	MIX-TLUD1	R1.01
Date: Monday, December 14, 2020		Sheet 30 of 59



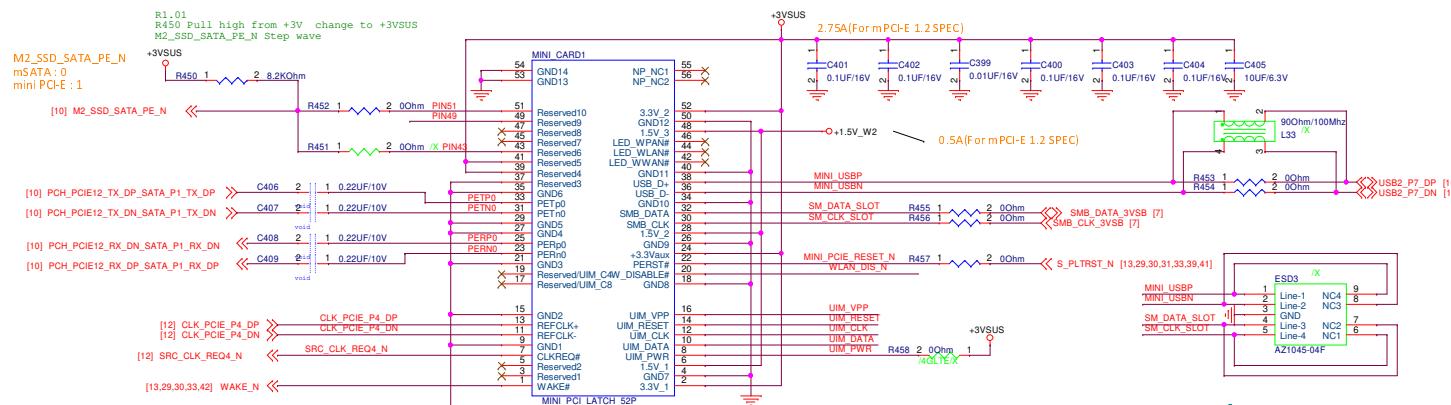




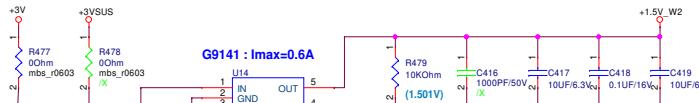
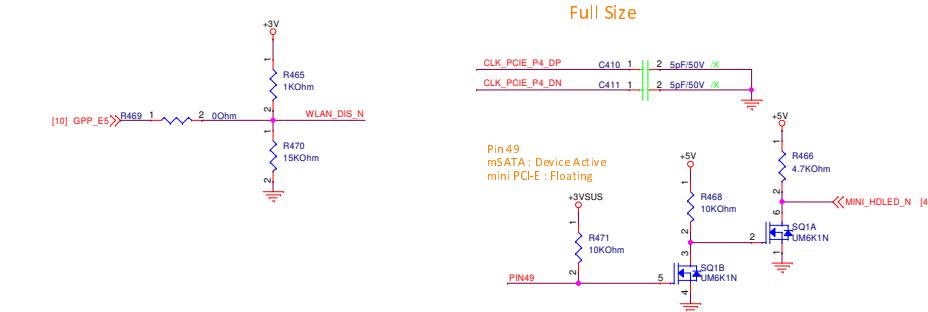




Mini PCI-E Card (Full size)



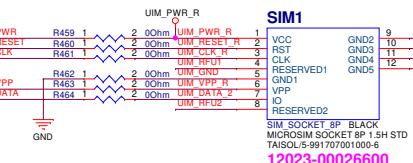
Full Size



NUT_MINI2_27_1

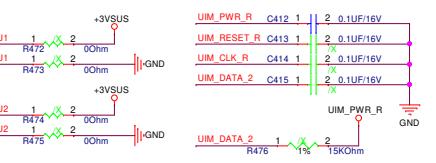
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Micro-SIM Card

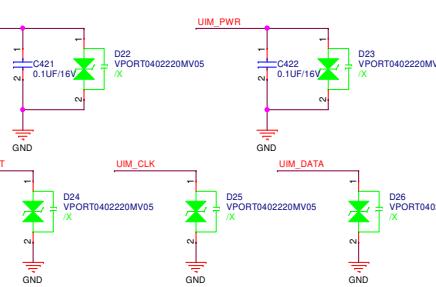


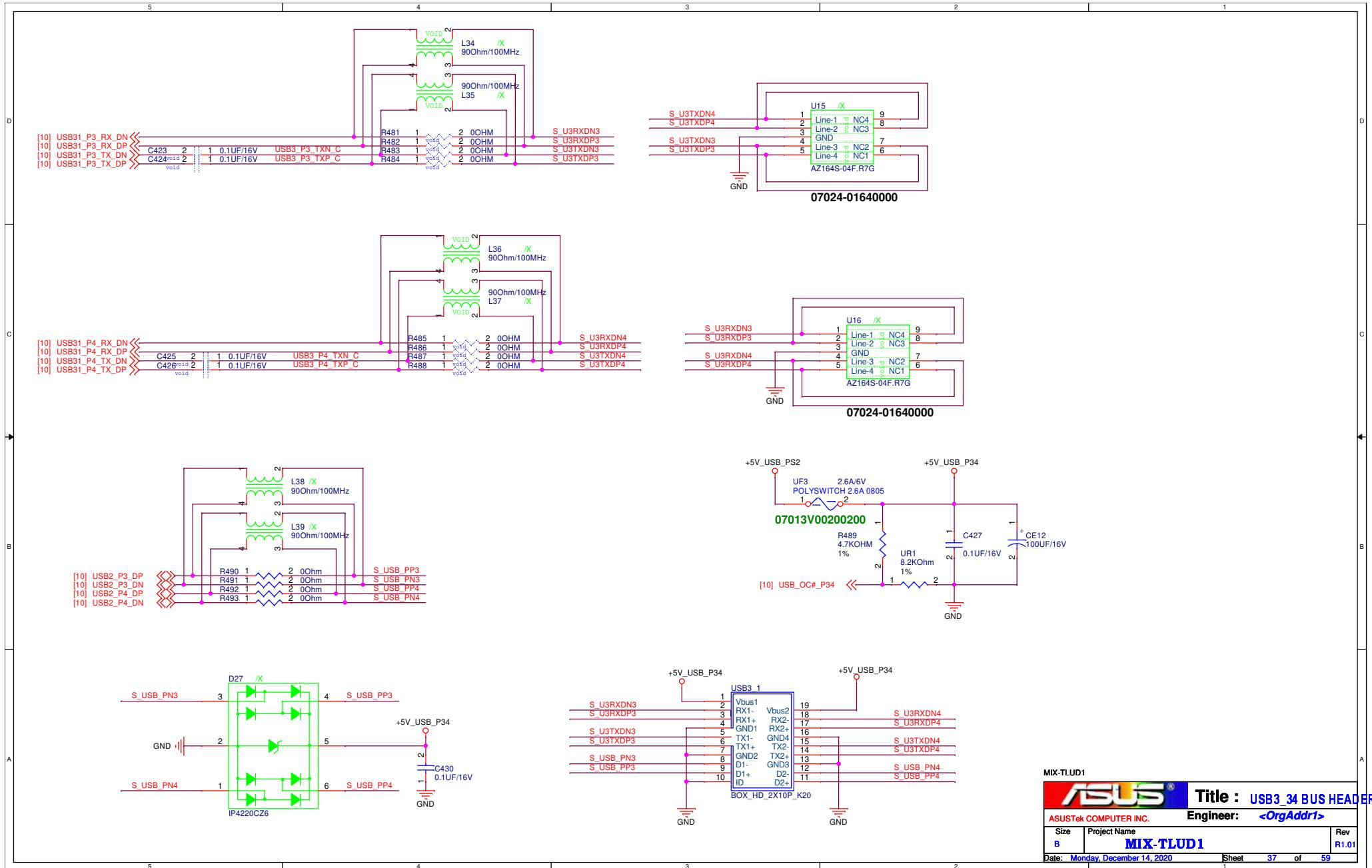
12023-00026600

Micro-SIM Card - Reserved Pin for Signal Quality



Micro-SIM Card - ESD Protection





MIX-TLUD1



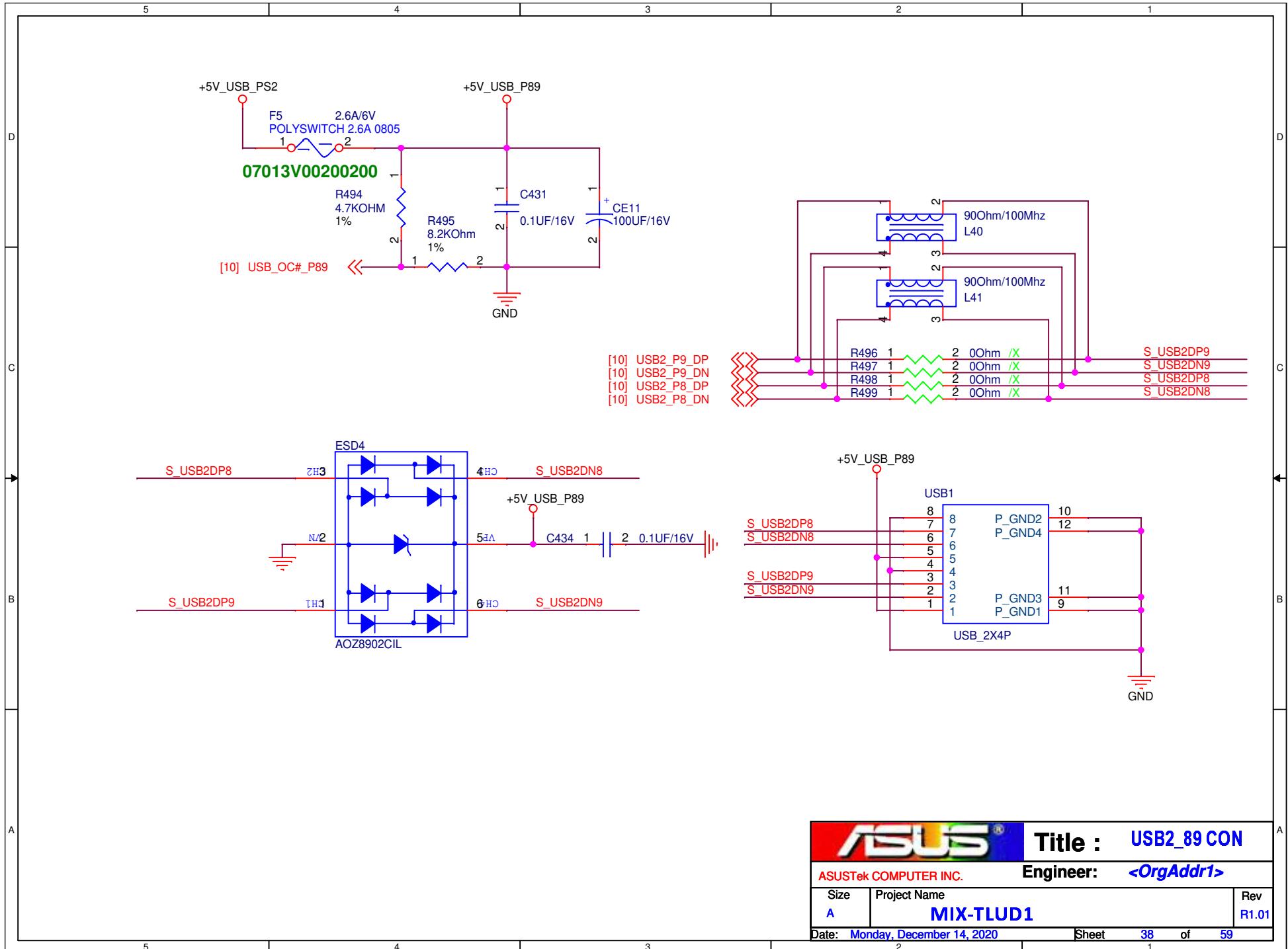
Title : USB3_34 BUS HEADER

Engineer: <OrgAddr1>

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B	MIX-TLUD1	R1.01

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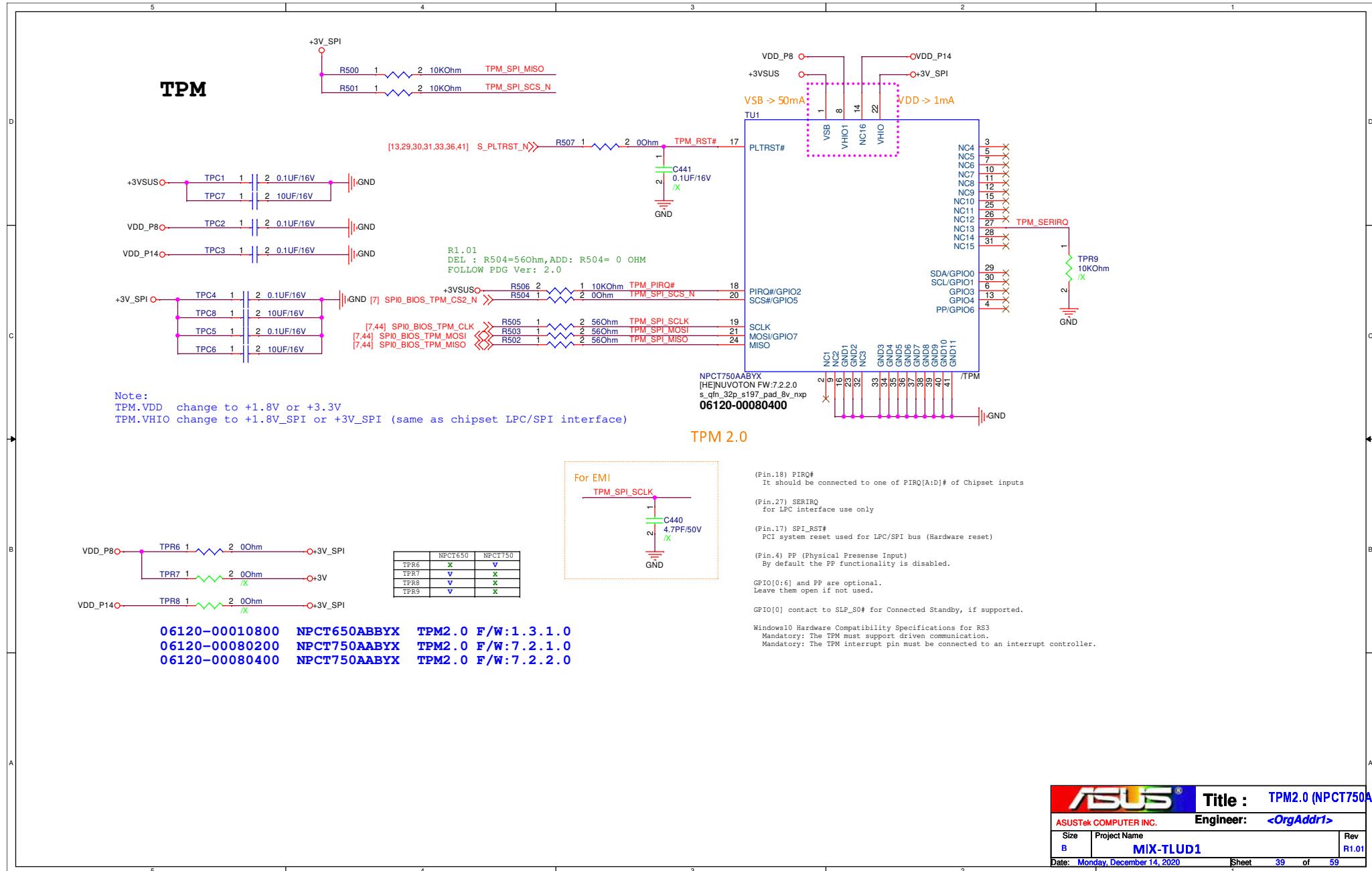


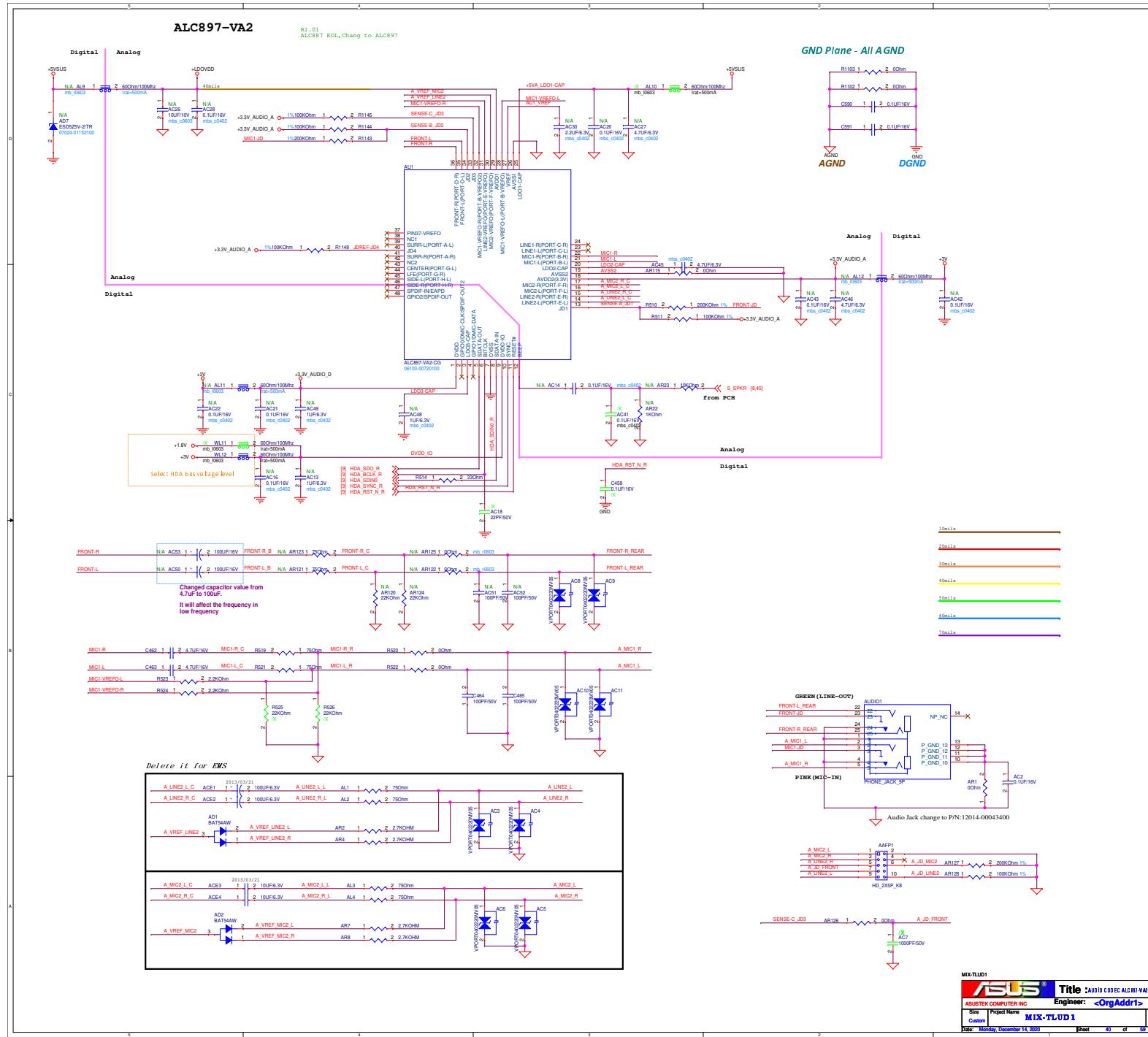
ASUS®

Title : USB2_89 CON

Engineer: <OrgAddr1>

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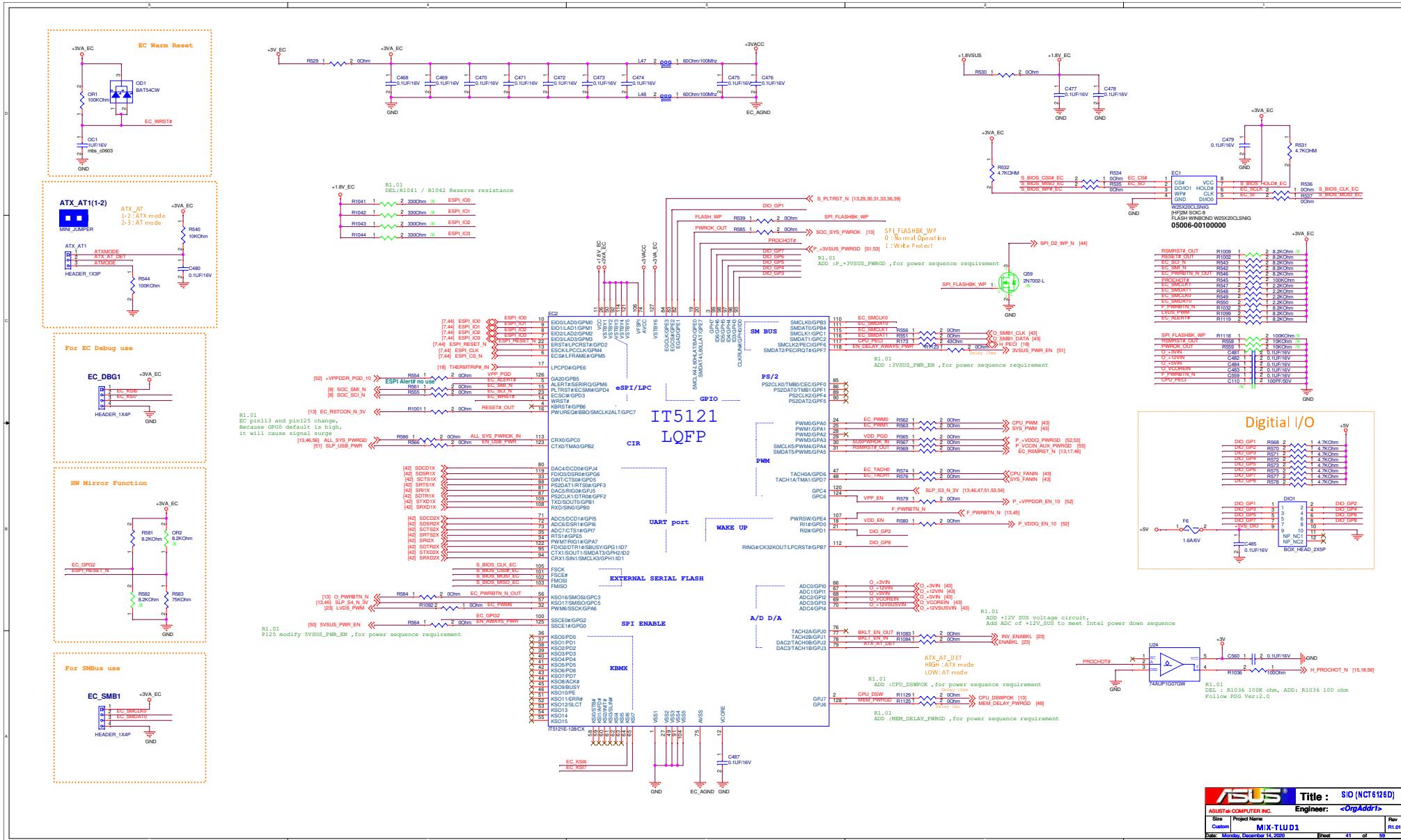
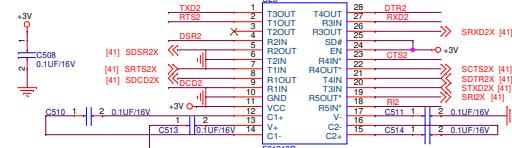
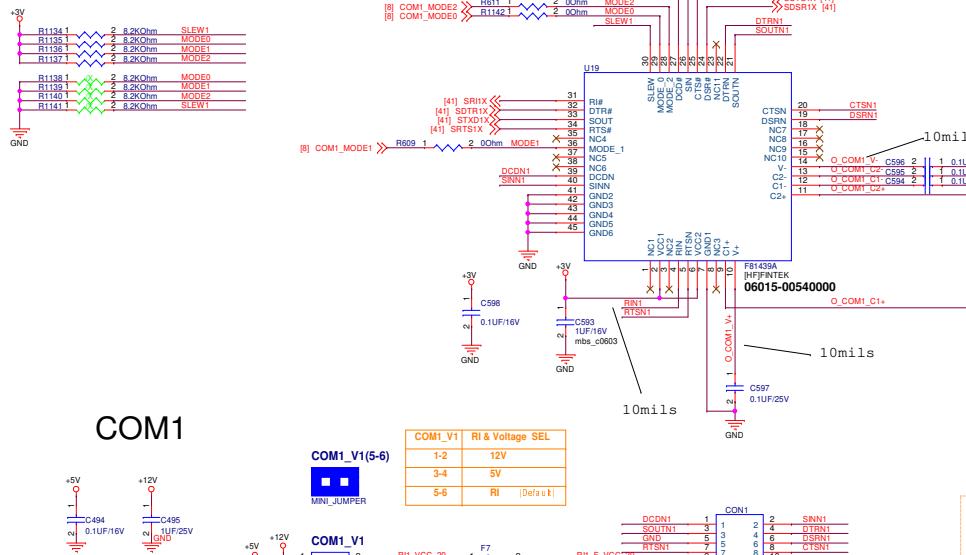


TABLE 1: Mode Select Configuration for F81439

Pin 29 Mode_0	Pin 36 Mode_1	Pin 28 Mode_2	Mode	Status
0	0	0	RS-422 Full Duplex	1T/1R RS-422
0	0	1	Pure RS-232	3T/5R RS-232
0	1	0	RS-485 Half Duplex	1T/R RS-485, TX ENABLE Low Active
0	1	1	RS-485 Half Duplex	1T/R RS-485, TX ENABLE High Active
1	0	0	RS-422 Full Duplex	1T/R RS-422 with termination resistor and bias resistor.
1	0	1	Pure RS-232	1T/R RS-232 co-exists with RS485 application without the need for the bus switch IC (for special usage).
1	1	0	RS-485 Half Duplex	1T/R RS-485 with termination resistor and bias resistor. TX ENABLE Low Active
1	1	1	Low Power Shutdown	All I/O pins are High Impedance

Note

1. COMMODE[0:2] pin. Internal pull high = 625KΩ. As the current is very small ($\approx 8\mu A$), please use the hardware strapping or GPIO (BIOS) to select the modes.
 2. Slew rate control pin. Internal pull high = 625KΩ.
SLEW = GND, RS-232/422/485 data rate = 250 Kbps
SLEW = Vcc, RS-232 data rate = 1.5Mbps, RS-422/485 data rate = 10Mbps



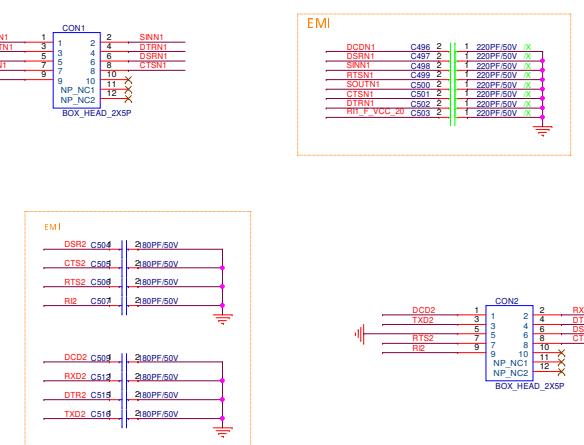
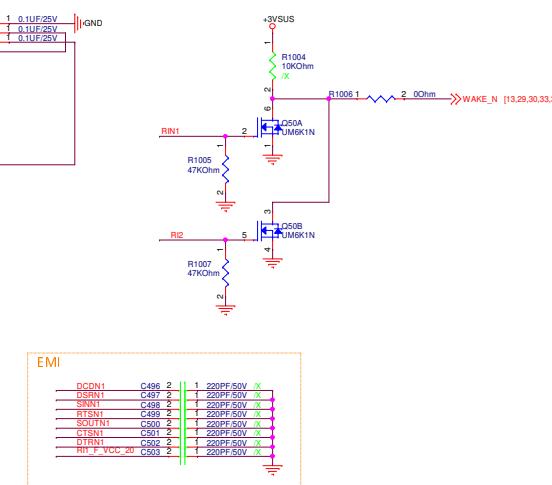
(VCC = +5.0V ± 10%)

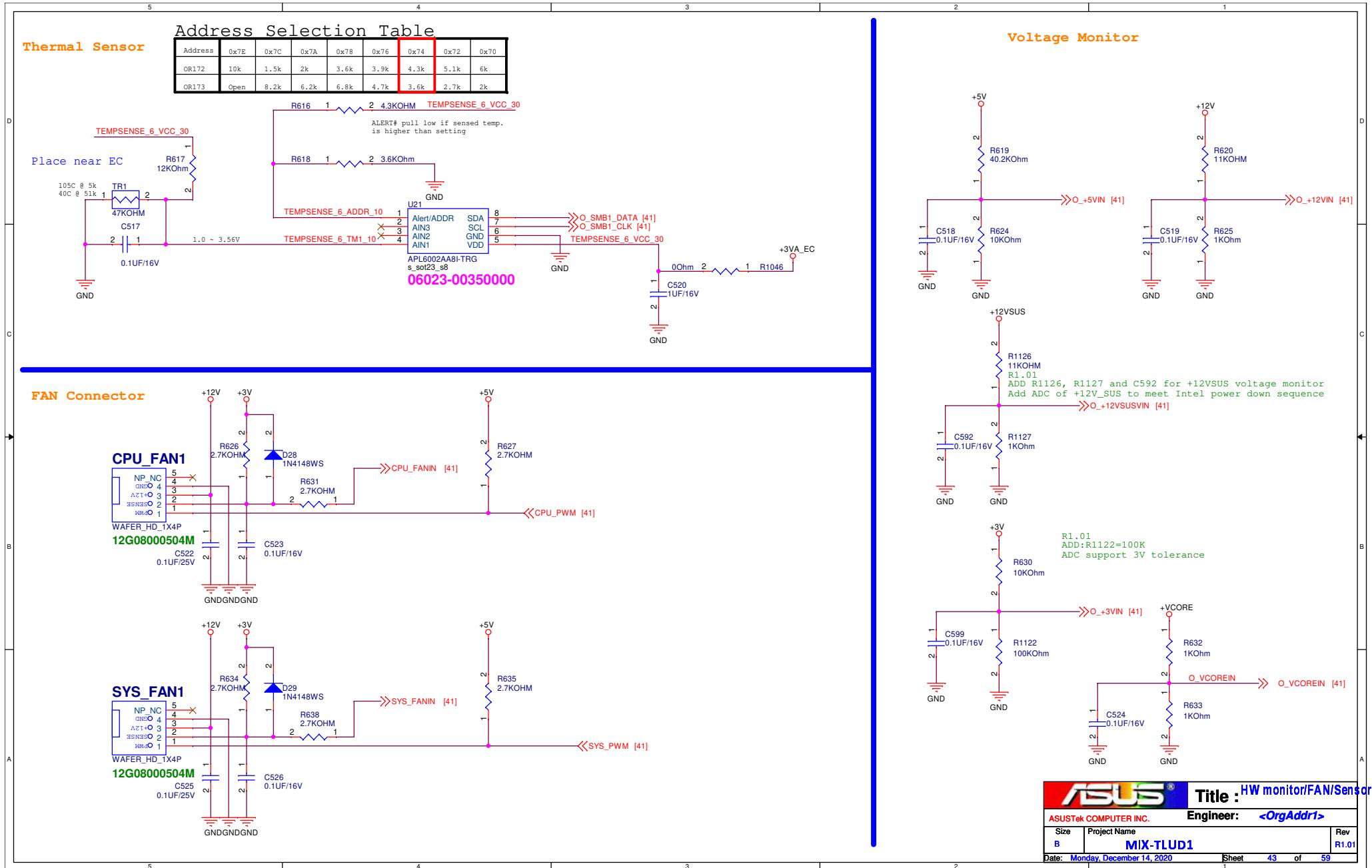
Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Voltage(Vcc=3.3V)		3.2	3.3	3.6	V
Supply Voltage(Vcc=5.0V)		4.5	5.0	5.5	V
Supply Current (RS-232)	No Load		2	30	mA
Supply Current (RS-485)	No Load		2		mA
Supply Current (RS-422)			2		mA

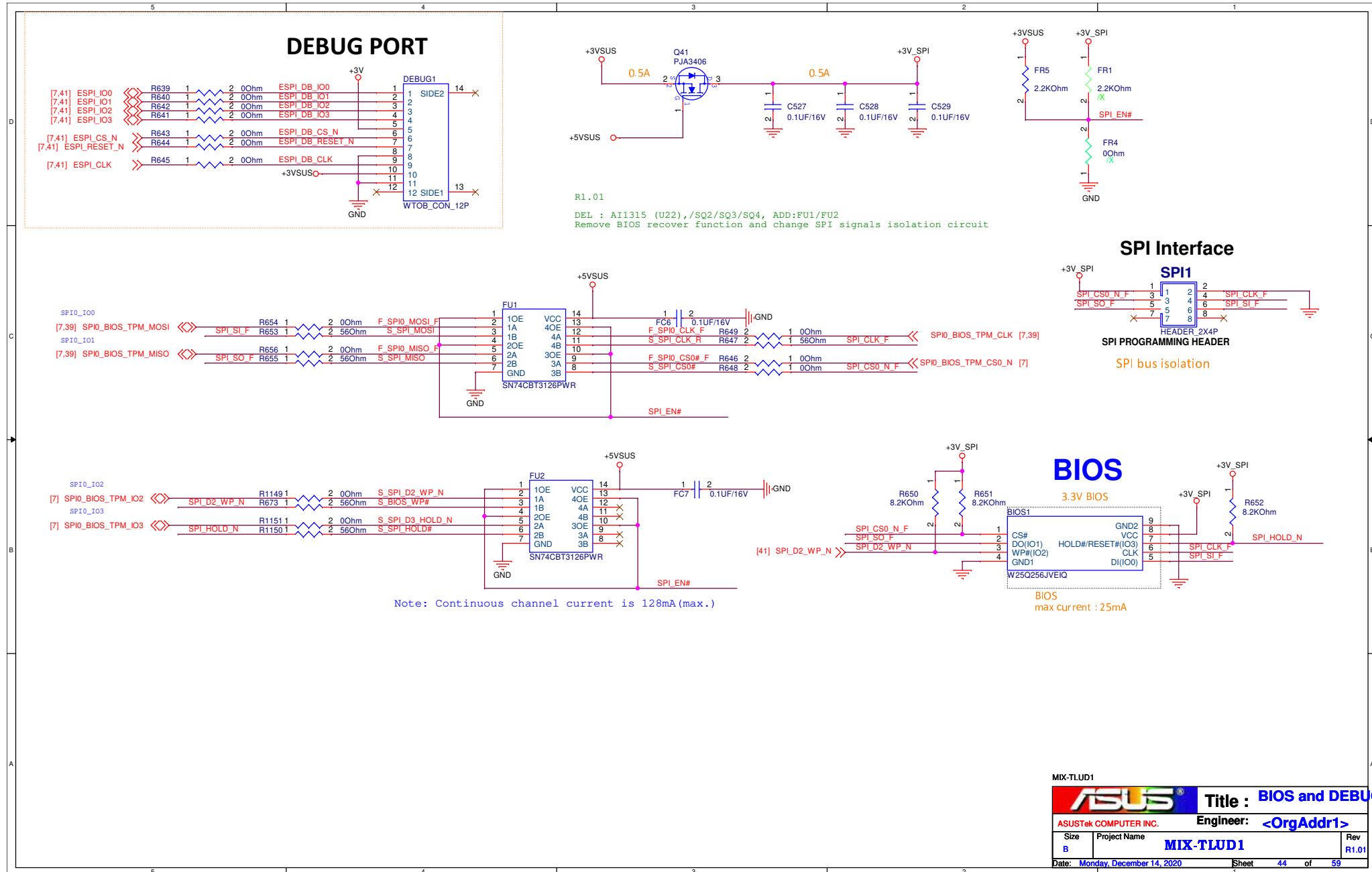
(TA = 0 °C to 70 °C, VCC = 3.3V ±10%, or +5.0V ± 10%)

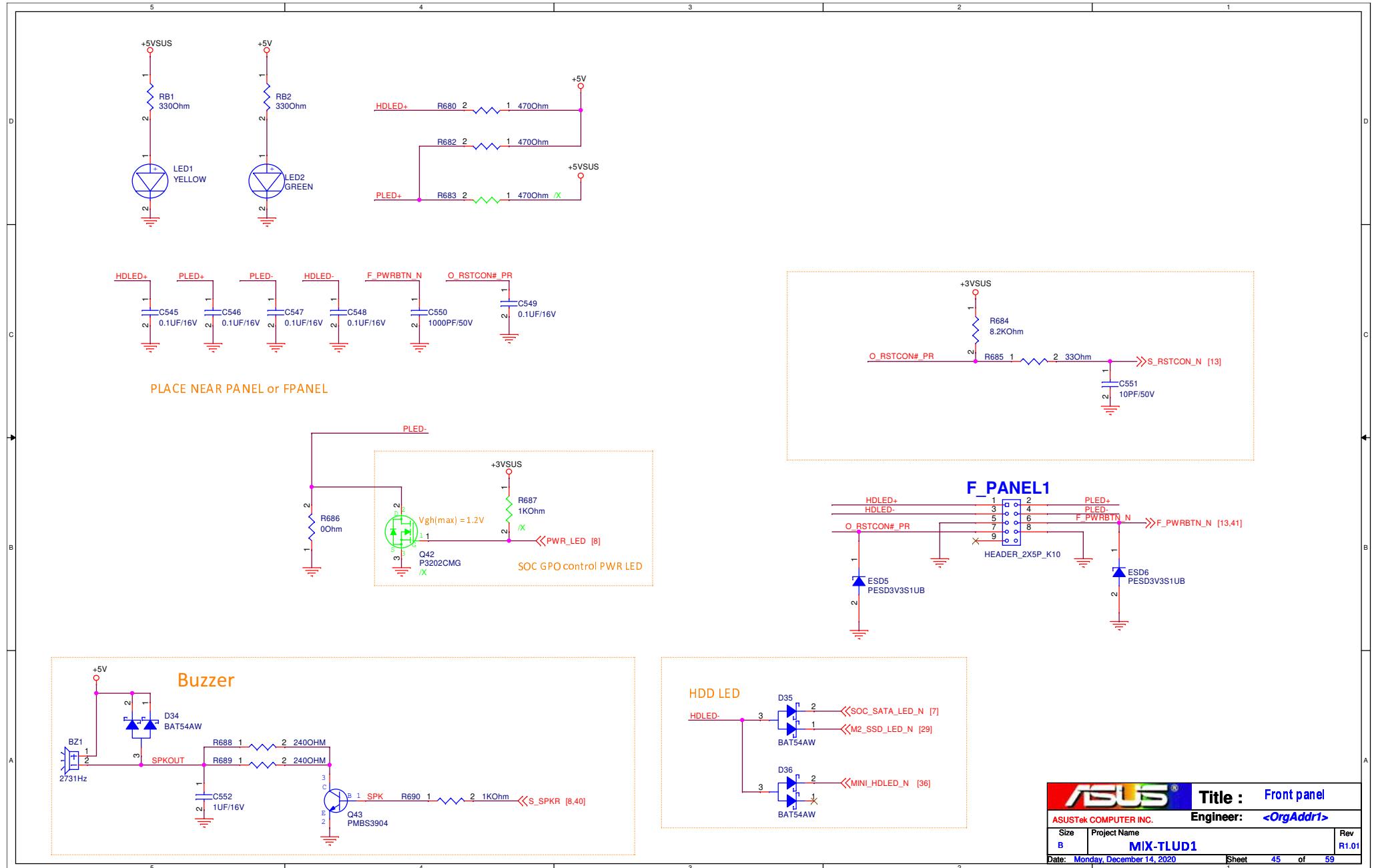
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Transmitter and Logic Input Pins (DRIVING, MODE, SLEW: pin 28, 29, 32, 33, 34, 36)						
Logic Input Voltage HIGH	V _{IH}	2.4			V	
Logic Input Voltage LOW	V _{IL}			0.8	V	VCC = 5.0 V
Logic Input Voltage HIGH	V _{IH}	2.0			V	
Logic Input Voltage LOW	V _{IL}			0.8	V	VCC = 3.3 V
Logic Input Pull-up Current	-			±15	µA	
Driver Input Pull High Current	I _{IT}			±15	µA	
Logic Input Hysteresis	-		0.5		V	

R1.01
Change to 3.3V COM port solut
F81438G change to F81439A
TPC212PPB change to F81212P

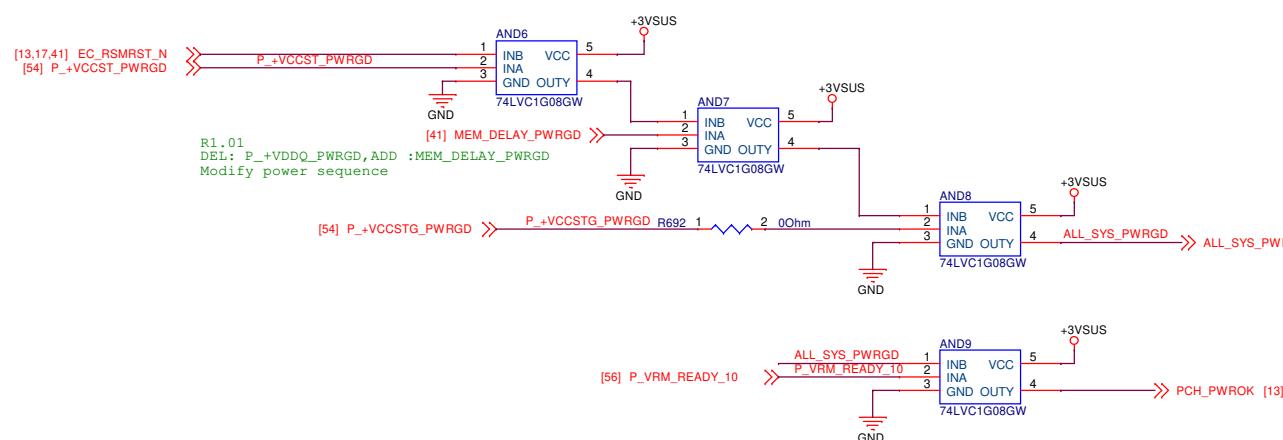




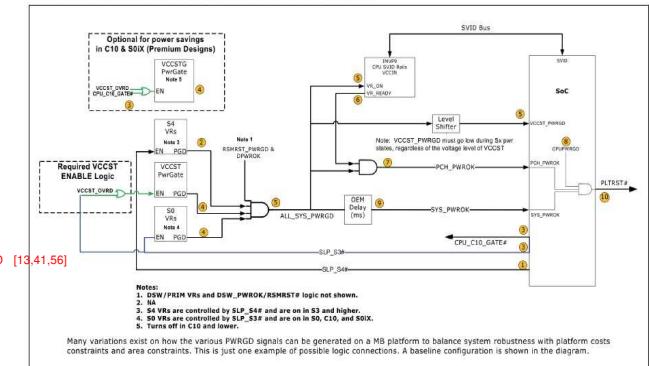




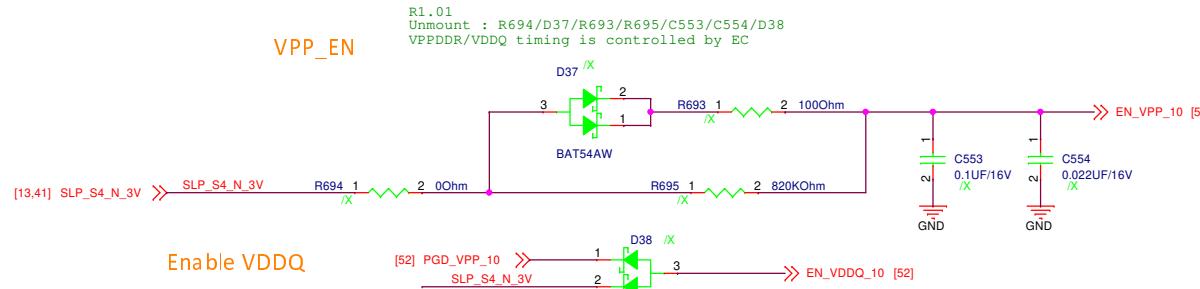
Tiger Lake PWROK Sequence



Premium PWROK Generation Flow Diagram



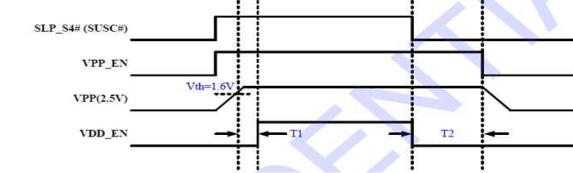
PWR DDR4 Power Sequence



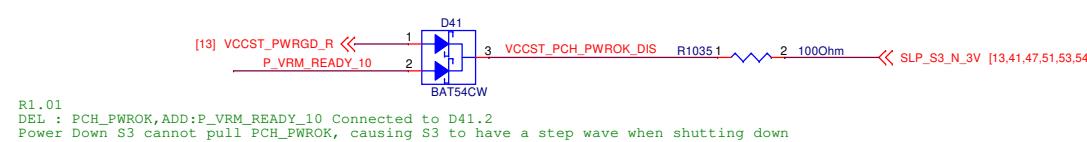
11.21 DDR4 Power Control Specification

Symbol	Typ.	Description
T ₁	5ms	The rising edge of VPP(2.5V) to rising edge of VDD_EN
T ₂	50ms	The falling edge of VDD_EN to rising edge of VPP(2.5V)

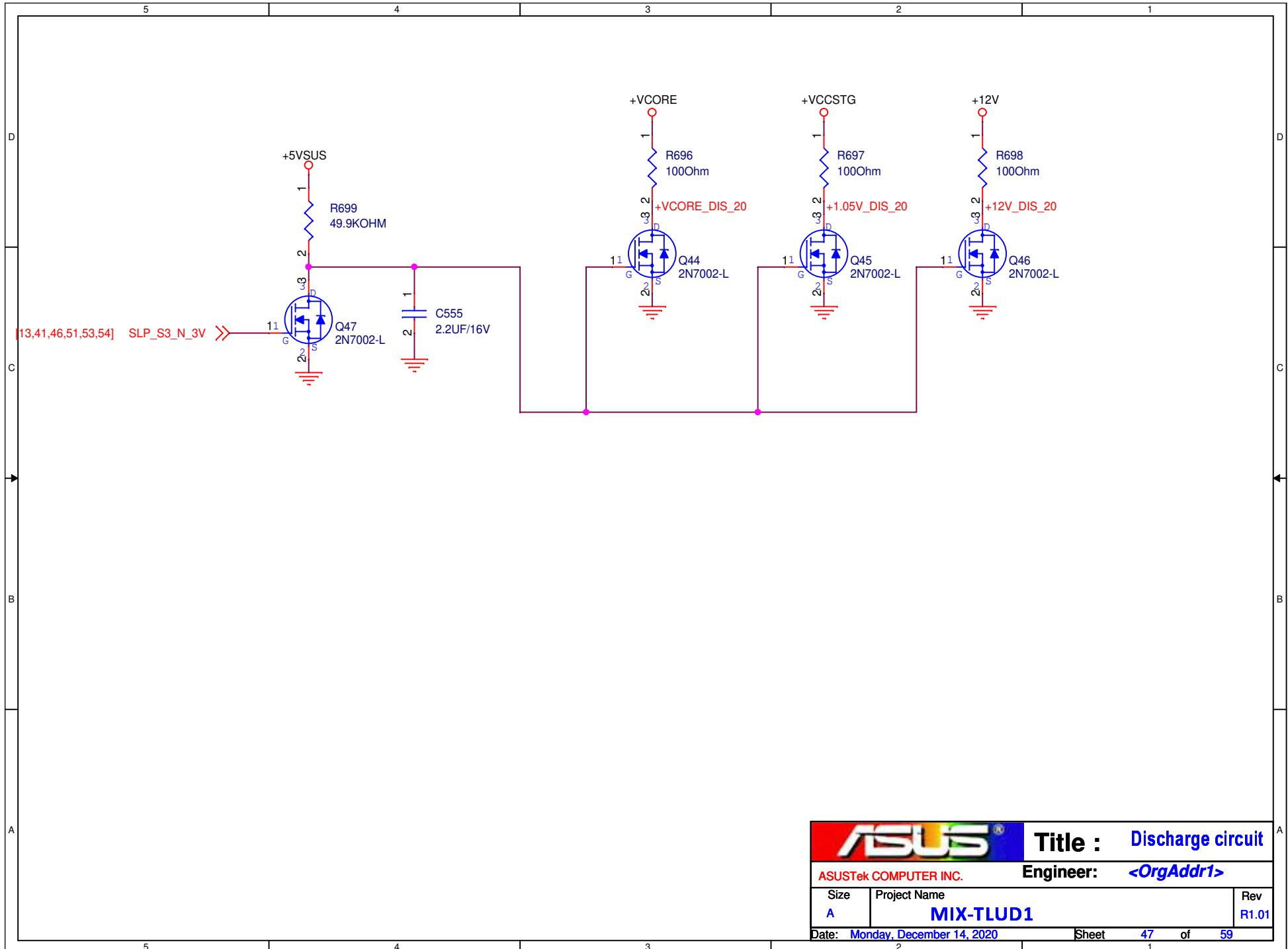
Table 11-5. DDR4 Timings Parameter



Power Down Sequence



MIX-TLUD1

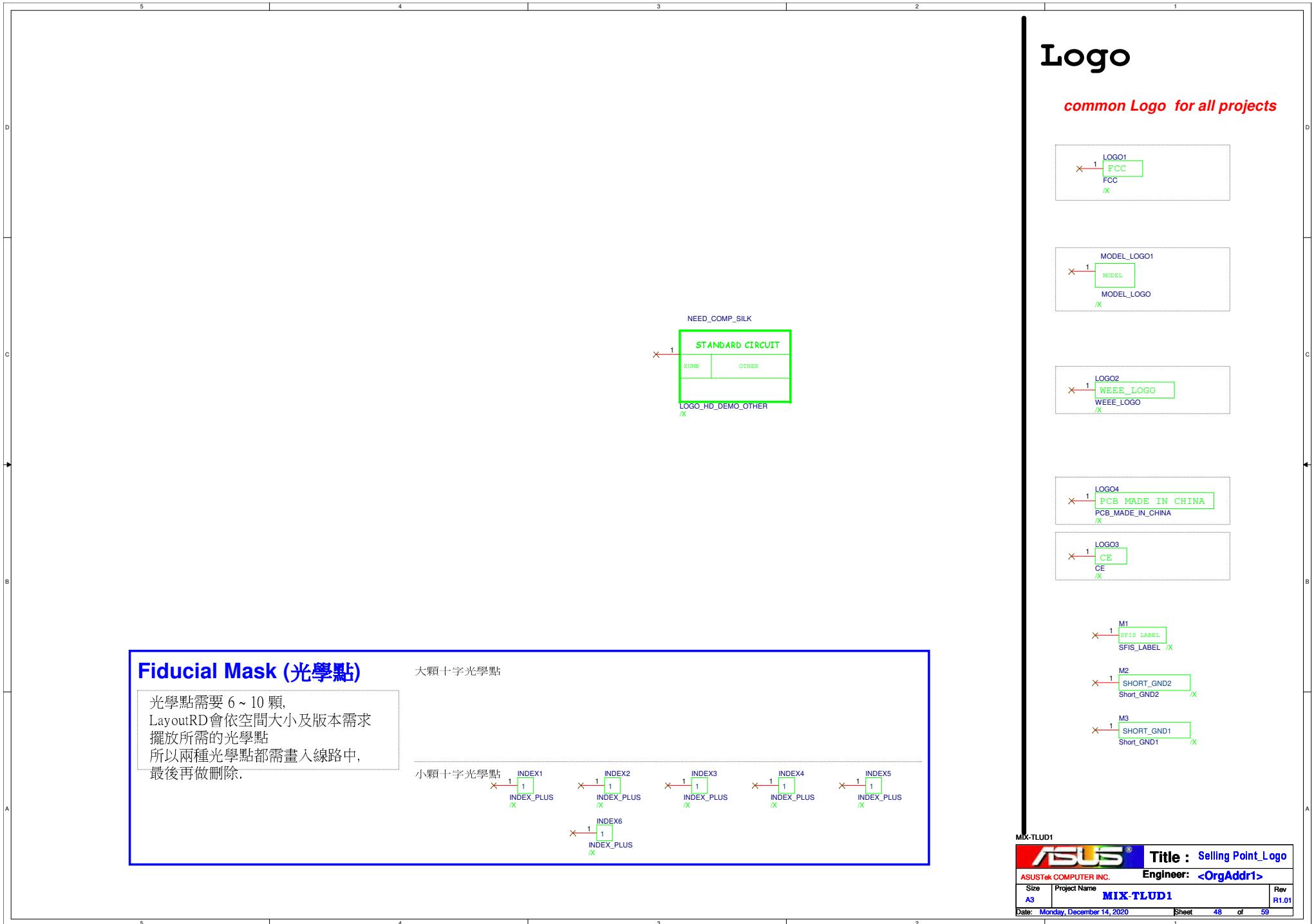


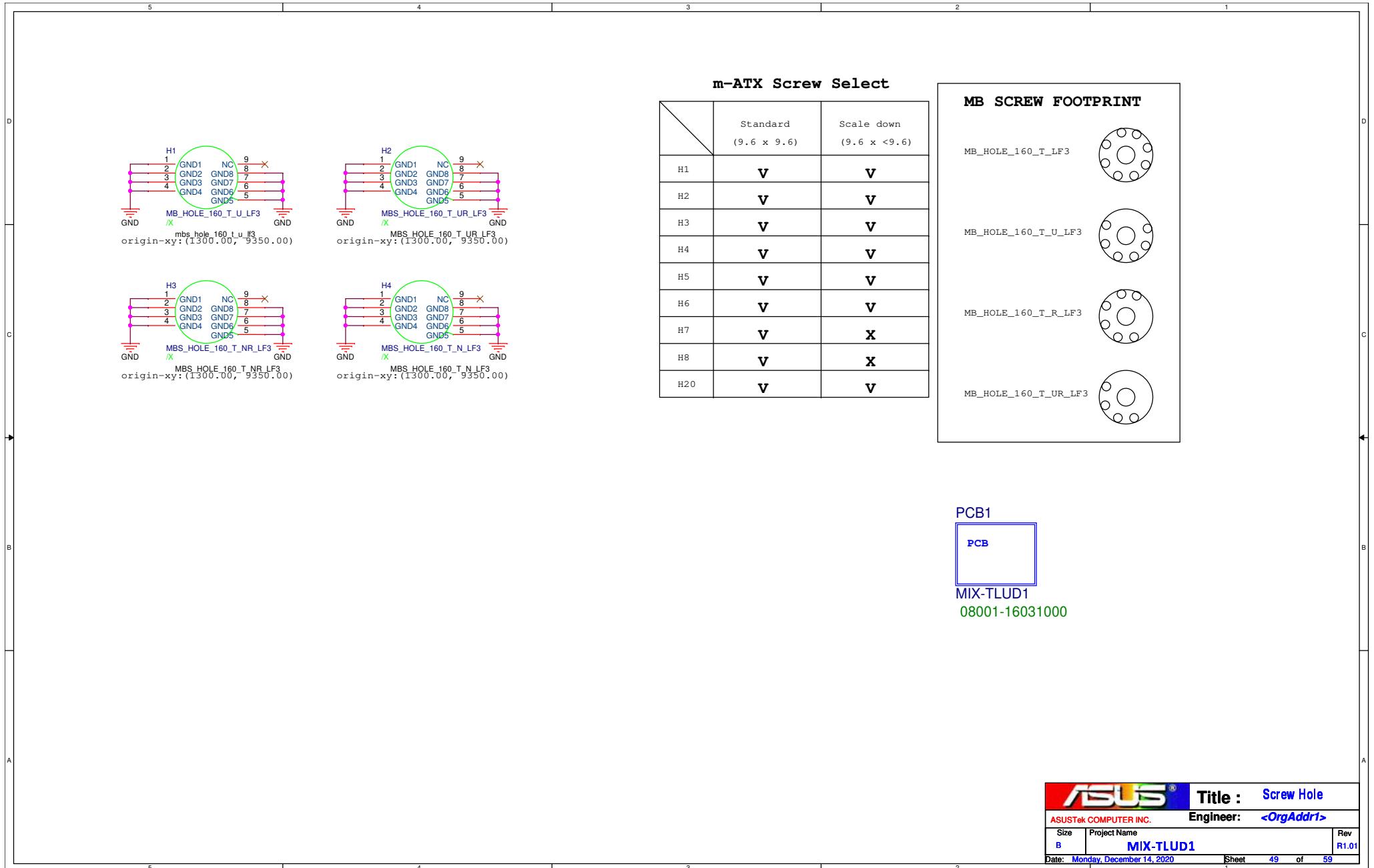
Title : Discharge circuit

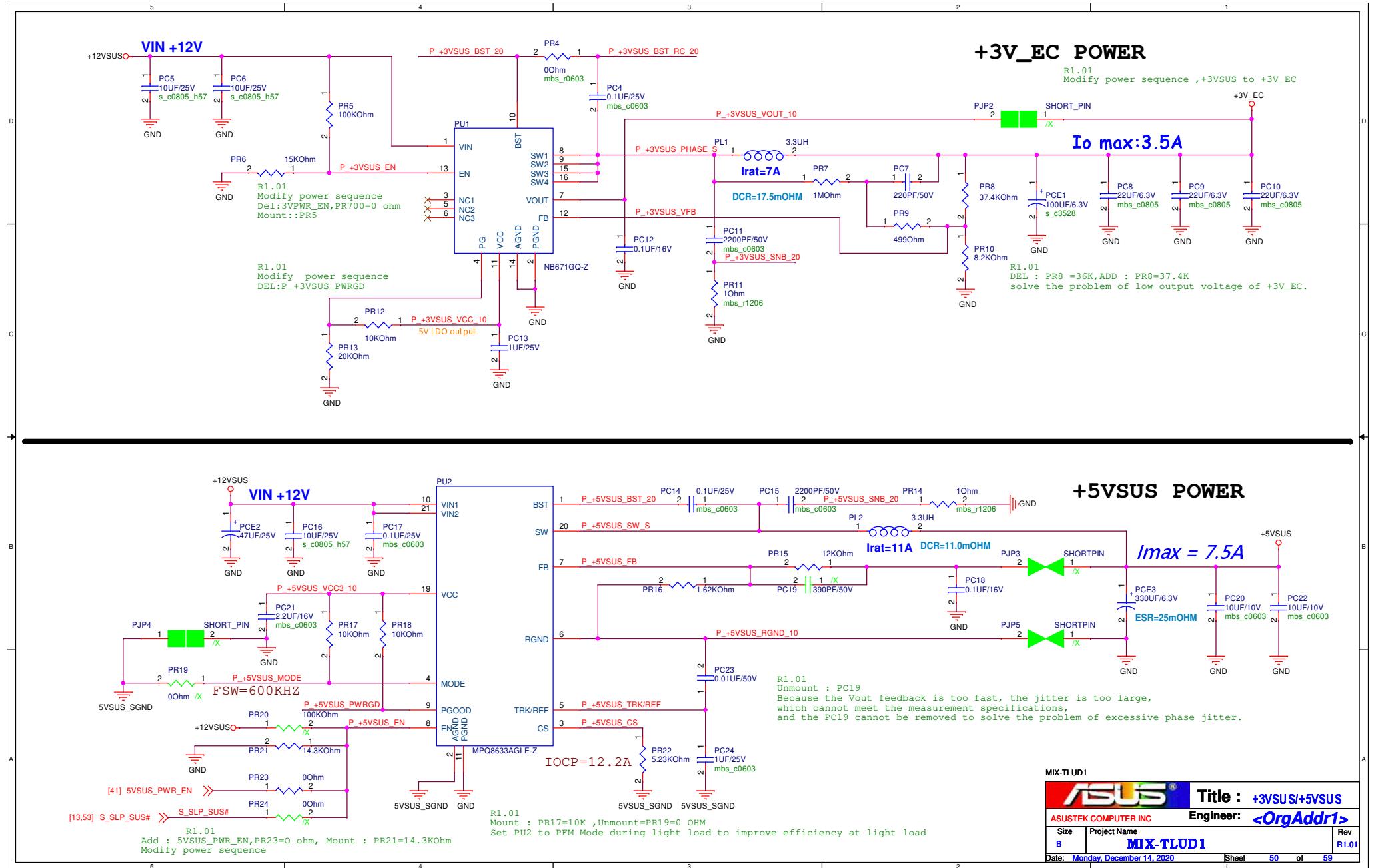
ASUSTek COMPUTER INC.

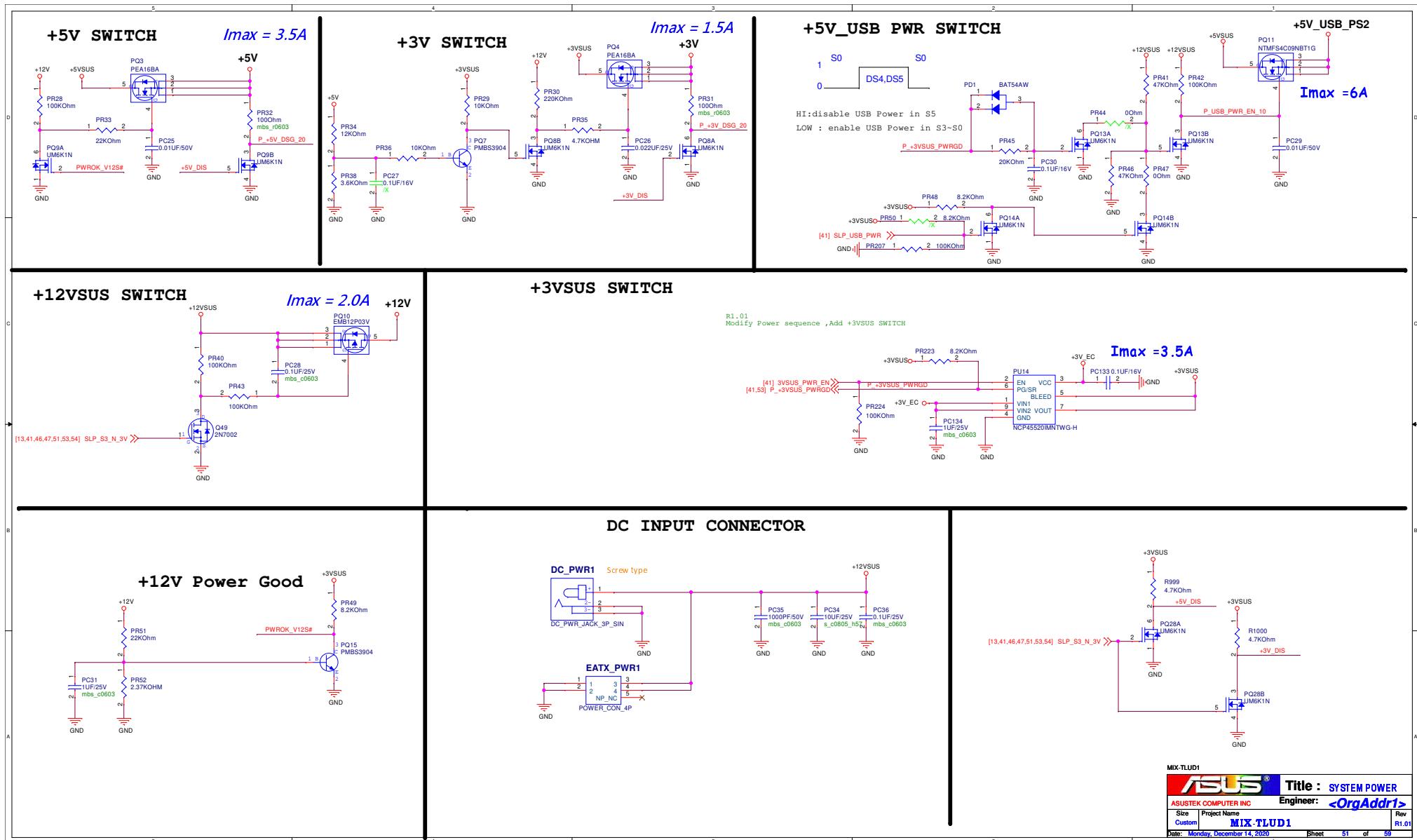
Engineer: <OrgAddr1>

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A	MIX-TLUD1	R1.01
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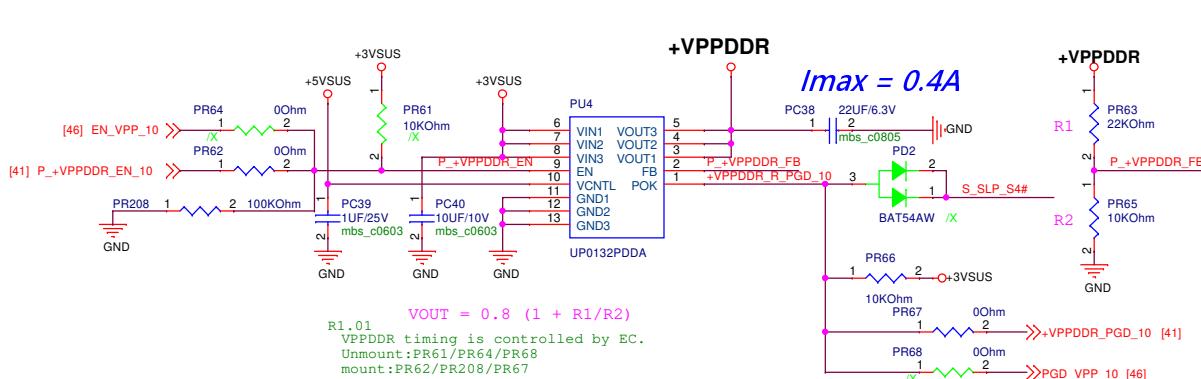
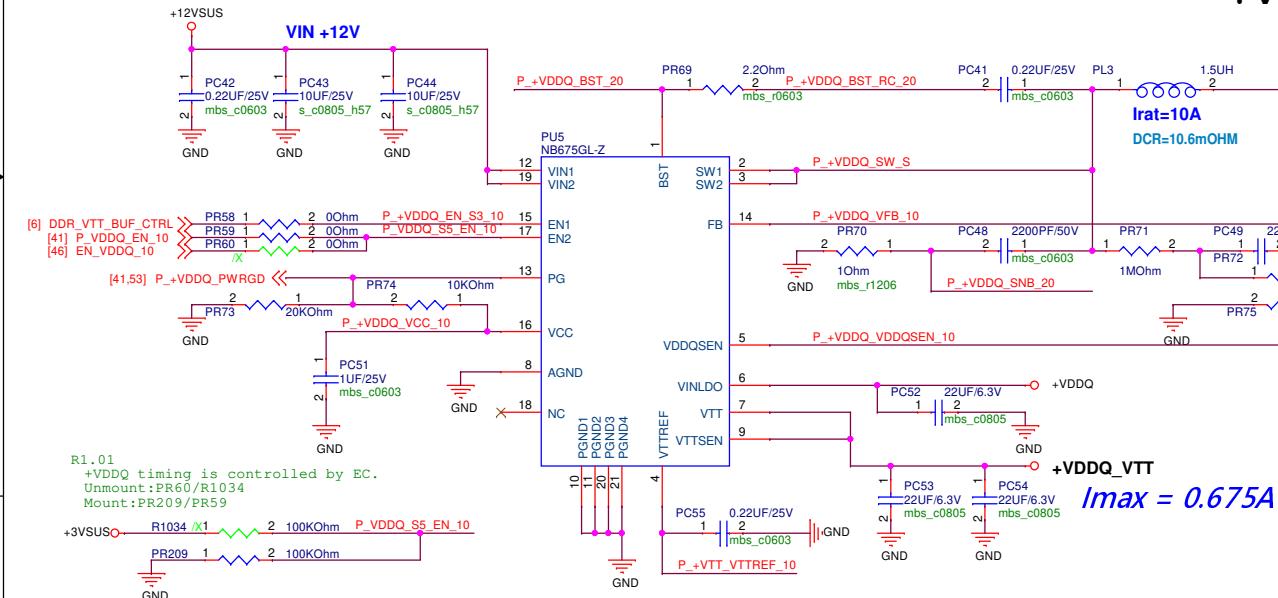




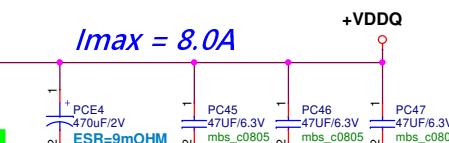
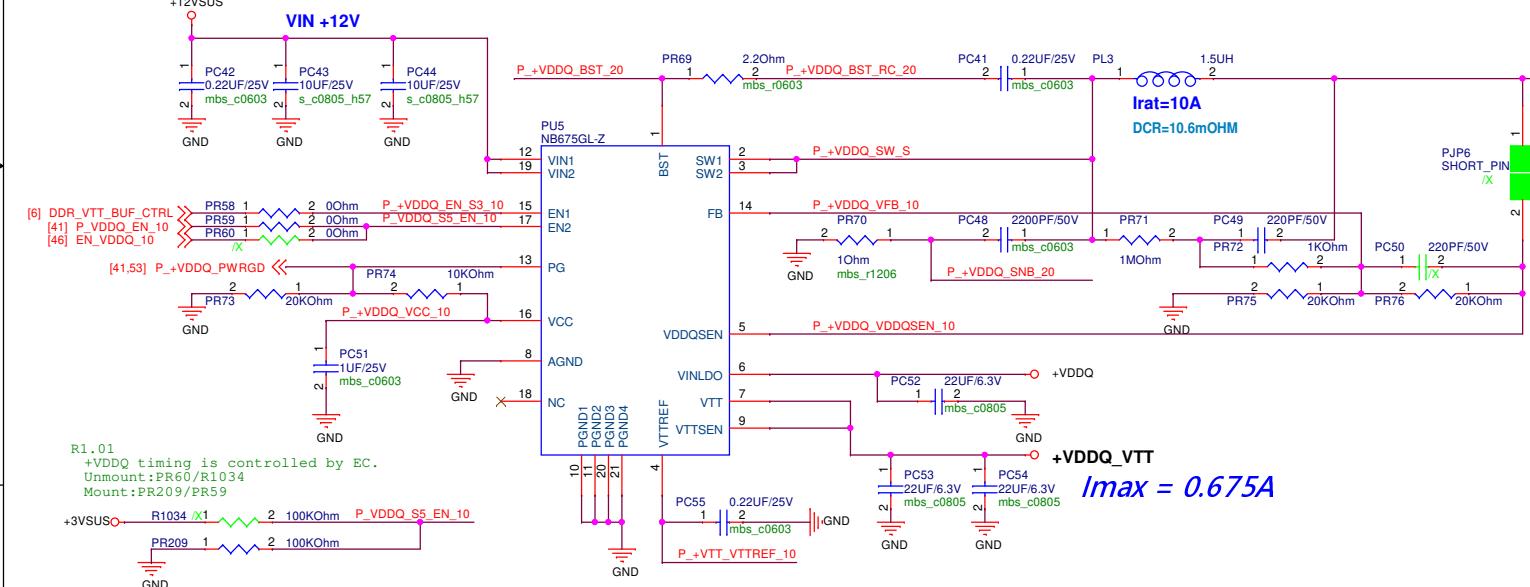




S3 And S5 Truth Table					
State	EN1	EN2	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off
OTHERS	Hi	Low	Off	Off	Off



+VDDQ POWER



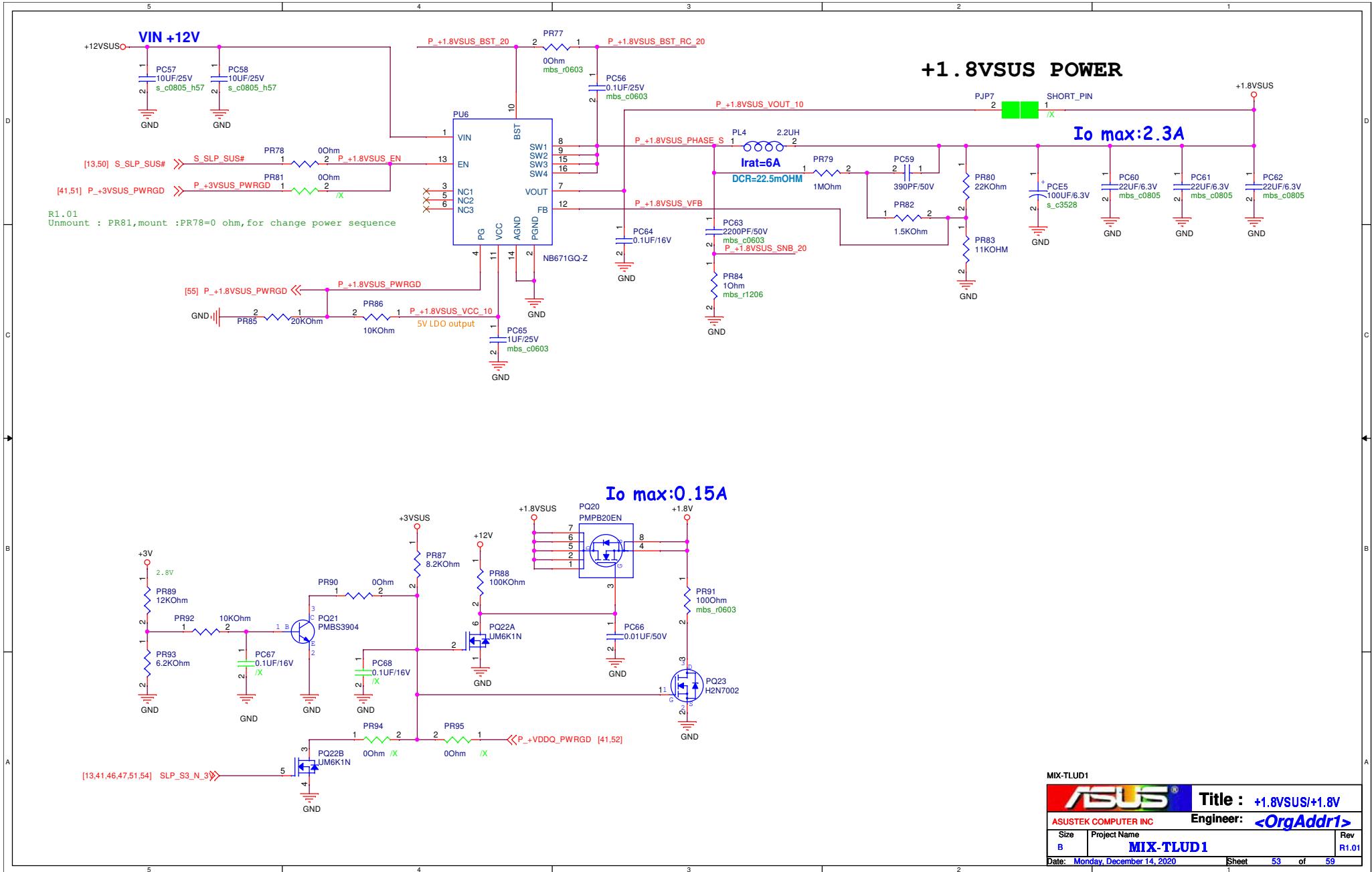
MIX-TLUD

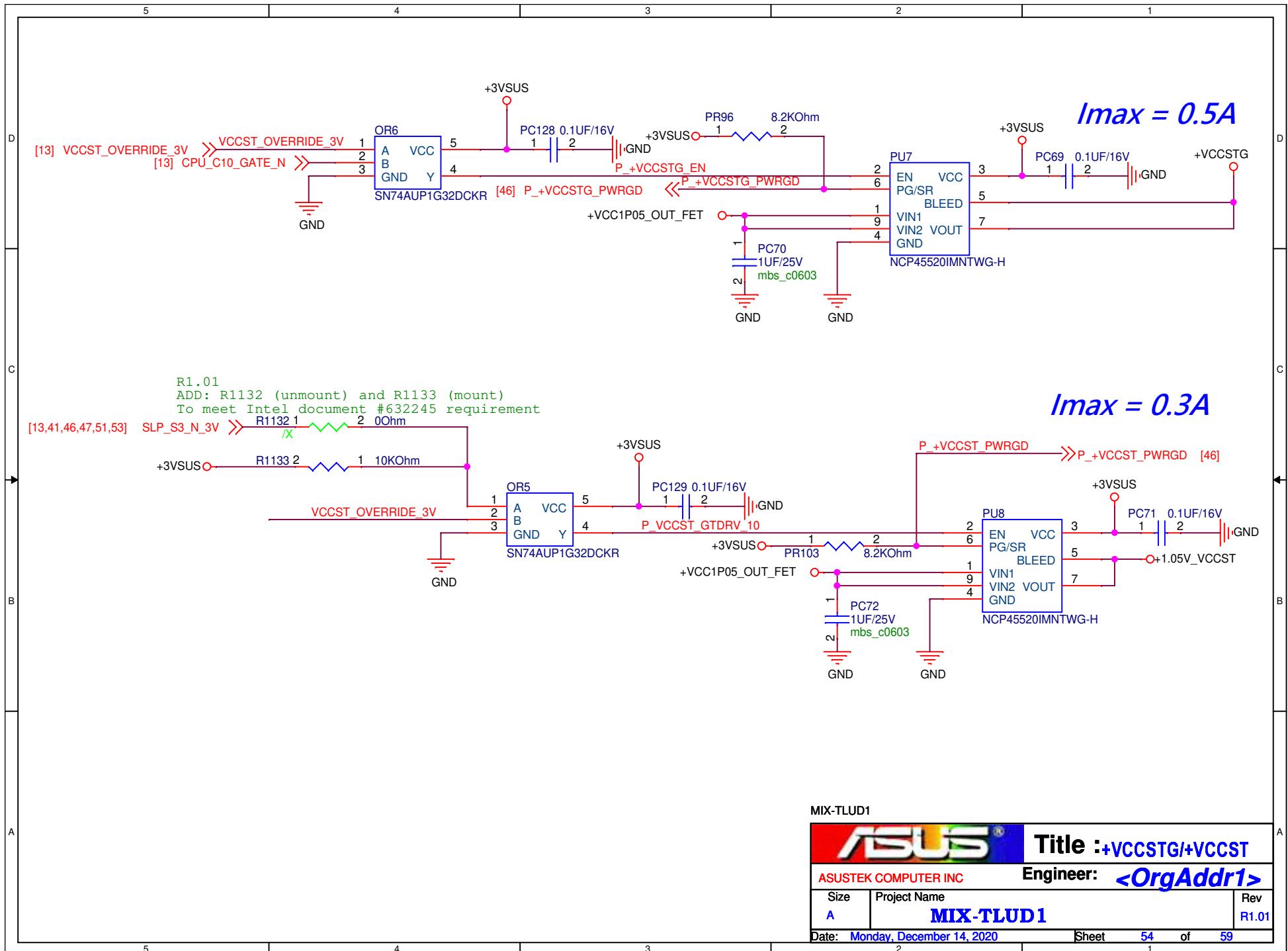


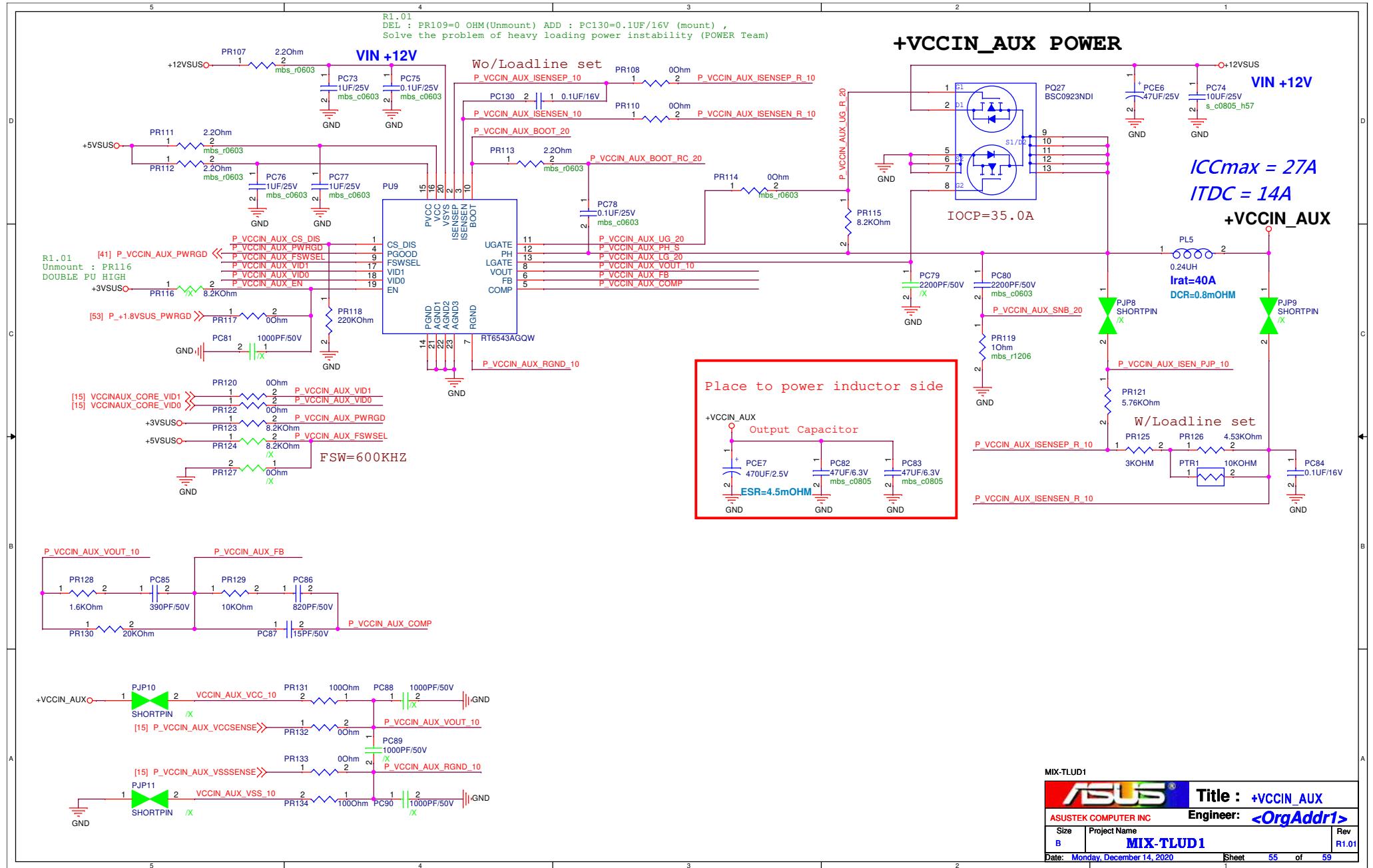
Title : +VDD0/+VBBDD

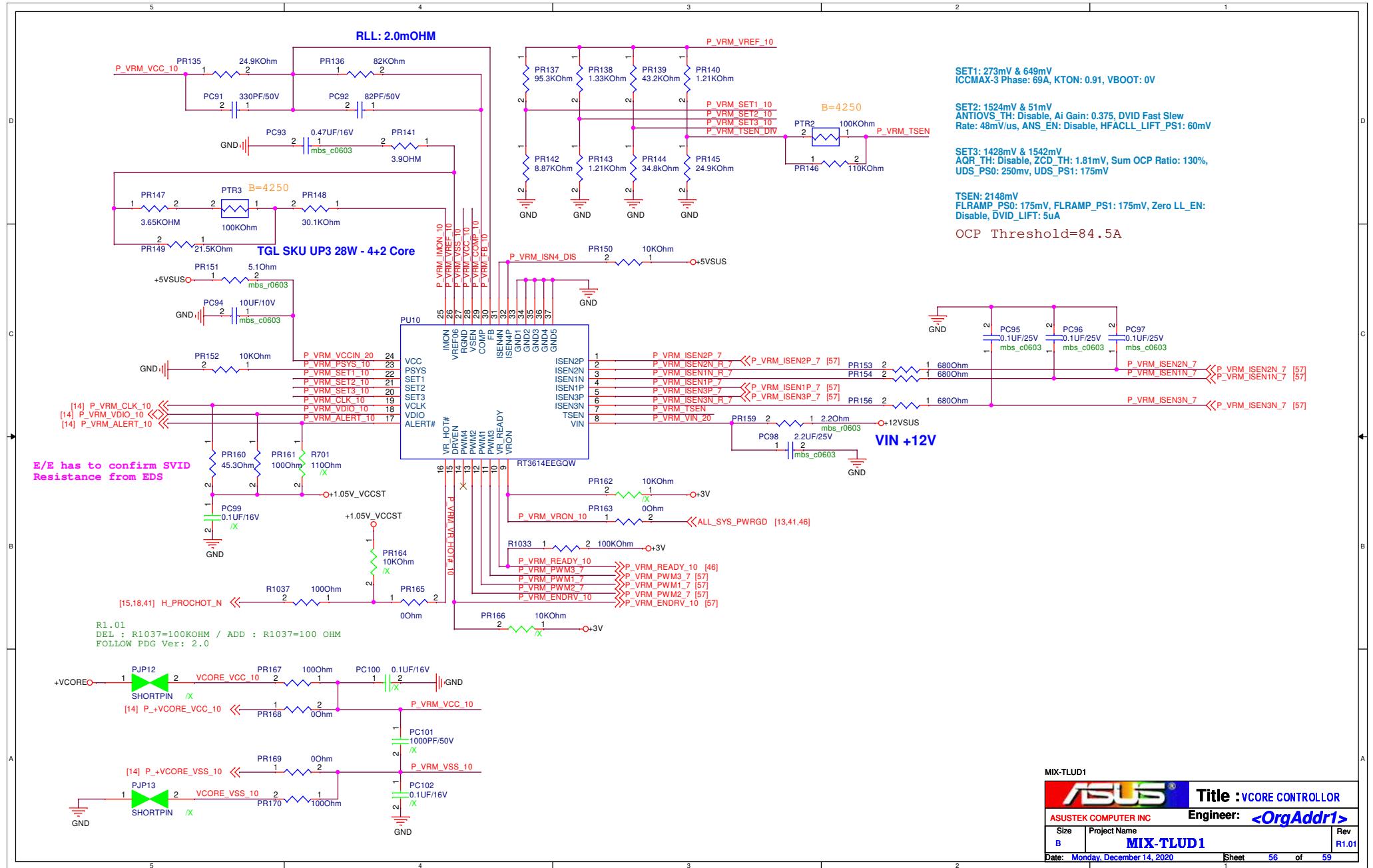
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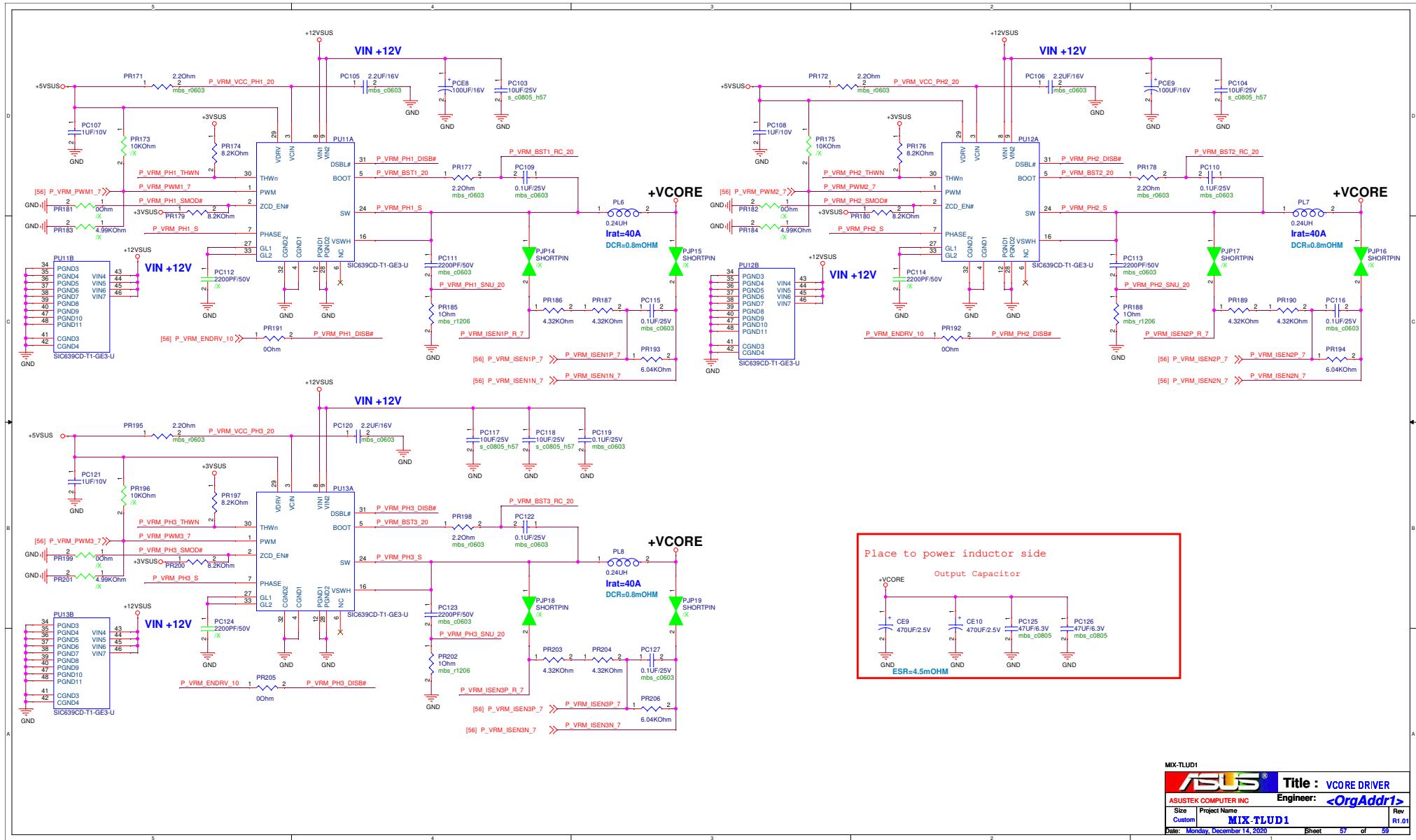
ASUSTOR COMPUTER INC.     











MIX-TGLD1 Power Budget

D

D

C

C

B

B

A

A

Name	VccIN	VccIN_AUX	VDD2	VTT	VccST	VccTGT	VCCPRIM_1P8	VCCPRIM_3P3	VCCDSW_3P3	5V_USB_PS2	3VSUS	12V	5V	3V	+1.1V_HDMI1	1.5V
Power Voltage	2V	1.8V	1.2V	0.6V	1.05V	1.05V	1.8V	3.3V	3.3V	5V	3V	12V	5V	3V	1.1V	1.5V
TGL_PU3+PCB	65	27	15		0.3	0.5	13	0.202	0.008							
DDR4 (SO-DIMM0)				5.2	0.4											
DIMM_A1																
DDR3 (SO-DIMM0)				5.2	0.4											
DIMM_B1																
LAN I219											0.3					
LAN I210/I211											1.3					
USB2.0 x9											4.5					
USB3.0 x4											6					
HDMI (N75DP159) x2														0.034	0.46	
FAN x2												2				
PCIe x4 slot												0.375	2.1		3	
M.2 M-Key (2x20)														0.4		
Mini PCIe Card											2.75					0.5
STAT Power												1.5	1.5			
AUDIO ALC887														0.012		
SPI (AI1315)											0.036					
EC (TS121E)																
TPM 2.0 (NPCT738AAAYX)											0.05					
Voltage (UNIT: V)	2	18	1.2	0.6	1.05	1.05	1.8	3.3	3.3	5	3	12	5	3	1.1	1.5
TOTAL CURRENT (UNIT: A)	65	27	11.9	0.8	0.3	0.5	13	0.202	0.008	10.5	4.811	3.6	1.5	3.446	0.46	0.5
TOTAL WATT (UNIT: W)	130	48.6	14.28	0.48	0.315	0.525	234	0.6666	0.0099	52.5	14.433	67.2	7.5	10.338	0.506	0.75
TRANSFER VOLTAGE	+12VSUS	+12VSUS	+12VSUS	+12VSUS	SOC	SOC	+1.8VSUS	+3VSUS	+3VSUS	+5VSUS	+12VSUS	+12VSUS	+5VSUS	+3VSUS	+3VSUS	+3VSUS
	12VSUS	5VSUS	3VSUS	1.8VSUS												
	27 W	60 W	12.27 W	2.34 W												
Power supply must consumed watts and currents																
Power Type	DC IN (12V)															
Consumed watts (Item: W)	349.61 W															
Consumed currents (Item A)	29.13 A															
Actually required currents (Item A/0.8)	36.4 A															

MD-TLUD1

ASUS		Title : Power Budget
ASUSTek COMPUTER INC.	Engineer:	
Size	Project Name	
C	MIX-TLUD1	Rev R1.0
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1. Bug :DDP1_HDMI / DDP2_HDMI ,TCP1_HDMI1_HPD/TCP2_HDMI2_HPD,Design error need to reverse -->P05
 2. (1)Unmount : PR116 ,DOUBLE PU HIGH. (2) DEL : PR109=0 OHM(Unmount) ADD : PC130=0.1UF/16V (mount) ,Solve the problem of heavy loading power instability (POWER Team Suggest) -->P55
 3. Bug :VCCINUX_CORE_VIDO / VCCINUX_CORE_VID1,Design error,need to PU:100K -->P15
 4. DEL:CS21<0.1UF,ADD:R1122=100K ADC can only input up to 3V, -->P43
 5. Add : SVSUS_PWR_EN,ohm, Mount : PR21 Change power sequence-->P50
 6. DEL : PR8 >3EKA,ADD : PR8=37.4K, solve the problem of low output voltage of +3VSUS, and Modify Power sequence +3VSUS to +3V_EC. -->P50
 7. Add : 5VSUS_PWR_EN,PR23=0 ohm, Mount : PR21=14.3Kohm,Modify power sequence . -->P50
 D
 8. Unmount power sequence , ADD : P_+VSUS_PWRGD/3VSUS_PWR_EN/CP0_DSWF0K / MEM_DELAY_PWRGDand modify 5VSUS_PWR_EN . -->P41
 9. Mount : PR17=10K ,Unmount=PR19=0 OHM,Set PU2 to PFM Mode during light load to improve efficiency at light load -->P50
 10. Unmount : PC19,Because the Vout feedback is too fast, the jitter is too large, which cannot meet the measurement specifications, and the PC19 cannot be removed to solve the problem of excessive phase jitter. -->P50
 11. +VPDDR / +VDDQ timing is controlled by EC. -->P46/P52
 12. Follow CRB / ASUS / AAEON ,Enable TLC,ADD:R1101 to 1K,DEL:R46. -->P07
 13. Unmount : R295 / R251 / R325 / R342,DOUBLE PU HIGH. -->P24/P25/P27/P28
 14. Bug : S_PLT_RST_N connected to I225 signal will have a pulse,DEL : R1030=100k / ADD : R1030=1K FOLLOW I225CRB Ver:1.7 FOLLOW I225 CRB Ver:1.7 -->P13
 15. DEL : I225_RST_N,ADD : I225_JTAG_RSTN,Design error,duplicate net name,-->P33
 16. DEL : R105=60.4OHM / ADD R105=62 OHM FOLLOW PDG Ver: 2.0 -->P13
 17. Modify Power sequence ,Add +3VSUS SWITCH -->P51
 18. DEL: P_+VDDQ_PWRGD,ADD :MEM_DELAY_PWRGD ,Modify power sequence -->P41/P46
 19. EC pin13 and pin125 change, Because GFG0 default is high, it will cause signal surge -->P41
 20. ADD +12V SUS voltage circuit, Add ADC of +12V_SUS to meet Intel power down sequence-->P41/P43
 21. DEL : R1039=60.4KOHM/ADD : R1039=60.4 OHM,FOLLOW PDG Ver: 2.0 -->P18
 22. DEL : Q5=UM6K1N/ ADD : Q5=PJT7828,Because Vgs<IV -->P13
 23. ADD : S_SLP_SUS# /CPU_C10_GATE_N 100K PD,Meet PDG 2.0 requirement and fix glitch issue. -->P13
 C
 24. R183 Pull high from +1.05V_VCCST change to VCCSTG,FOLLOW PDG Ver: 2.0 -->P18
 25. DEL : R1036/R1037=100KOHM / ADD : R1036/R1037=100 OHM FOLLOW PDG Ver: 2.0 -->P41/P56
 26. Unmount : R97 ,Do not send CLOCK mandatory -->P12
 27. DEL : R504=560hm,R1047/R1048=5.1OHM,ADD : R504/R1047/R1048=0 OHM FOLLOW PDG Ver: 2.0 -->P07/P39
 28. DEL:C259/C273,Q18/Q23 Change to PJA3434 ,VGsth (Gate Threshold Voltage) < 1.5V,FOLLOW PDG Ver: 2.0-->P27/P28
 29. DEL : PCH_PWROK,ADD:P_VRM_READY_10,Power Down S3 cannot pull PCH_PWROK, causing S3 to have a step wave when shutting down-->P46
 30. ADD: OR5.1 to R1133=10K pull up +3VSUS for #632245 -->P54
 31. Add CPU_DSWF0K signal to control DSW_PWROK timing to meet Intel sequence requirement . -->P13
 32. DEL : C345 / C346=20PF,ADD : C345 / C346= 6.8pf The manufacturer recommends -->P33
 33. DEL : C311 / C312=27PF,ADD : C311/ C312= 10pf The manufacturer recommends -->P31
 34. DEL : C1 / C2=15PF,ADD : C1 / C2= 10pf The manufacturer recommends -->P12
 35. DEL : C568 / C569=22PF,ADD : C568 / C569= 6.8pf The manufacturer recommends-->P23
 36. Change to 3.3V COM port solution -->P42
 37. Follow PM SPEC I225-V change to I225-LM -->P33
 38. M2_SSD_SATA_PE_N Step wave,R450 Pull high from +3V change to +3VSUS -->P36
 39. DEL:R1041 / R1042 Reserve resistance -->P41
 40. DEL :D31, ADD:AND10,RSMSRT leakage ,SCHOTTKY diode change to AND gate -->P44
 B
 41. DEL : D39=SCHOTTKY diode / ADD :AND11=AND gate ,SYSRESET leakage ,SCHOTTKY diode change to AND gate-->P13
 42. DEL : R77=113 ohm / ADD:R77=120 ohm for USB2.0 SI-->P10
 43. Mount:R233/R234 follow ASUS schematic,and DEL : D2,+5V change to HDMI1_PWR -->P24
 44. Mount:R277/R279 follow ASUS schematic, and DEL : D5,+5V change to HDMI2_PWR -->P25
 45. DEL : S02/S03 ,Remove unnecessary parts, U22 can be replaced. -->P44
 46. ALC887 EOL,Chang to ALC897. -->P40
 47. Unmount : PR81,mount : P:R78=0 ohm,for change power sequence. -->P53
 48. DEL : A11315 (U22),/S02/S03/S04, ADD:FU1/FU2,Modify SPI circuit. -->P44
 49. DEL:R1019 / R1020 (0 OHM),ADD:R1019 / R1020 (10K) follow ASUS schematic -->P24/P25
 50. Mount:R233/R234/R277/R279/R261/R305 follow ASUS schematic -->P24/P25
 51. Unount:R265/R271/R309/R315 follow ASUS schematic -->P24/P25
 52. DEL:D3/D4/D6/D7/D12/D13/D14/D15(AZ164),ADD:D3/D4/D6/D7/D12/D13/D14/D15(AZ1023-04F),Reverse stand-off voltage 3.3V -->P24/P25/P27/P28
 53. ADD:6002/C604, follow ASUS schematic -->P24/P25
 54. ADD : R1152 (Reserved),for #633581 -->P33
 55. DEL : R243/R287=6.49K,ADD:R243/R287=5.6K, follow ASUS schematic -->P24/P25
 56. DEL:D8:09/D10/D11(AZ164),ADD:D8/D9/D10/D11(AZ1045-04F),Reverse stand-off voltage 5V -->P26