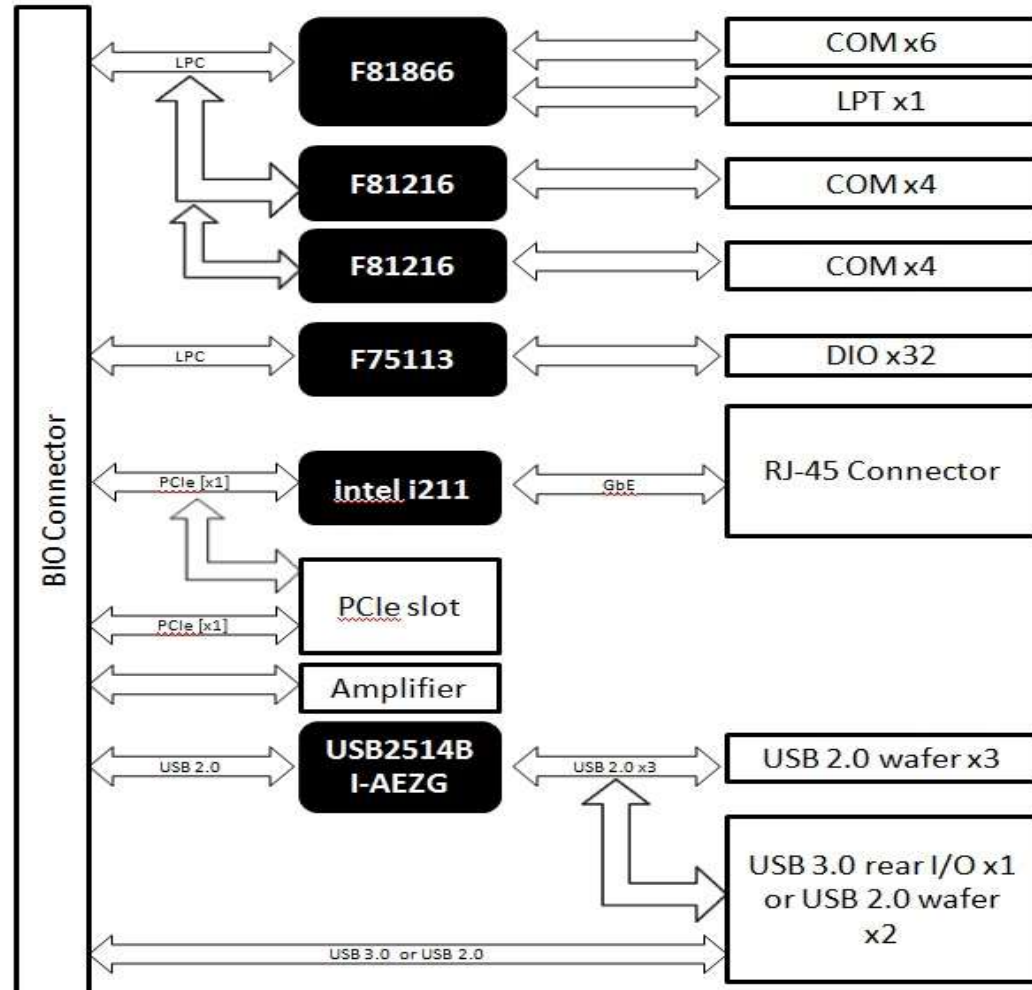


## Sub Compact Board

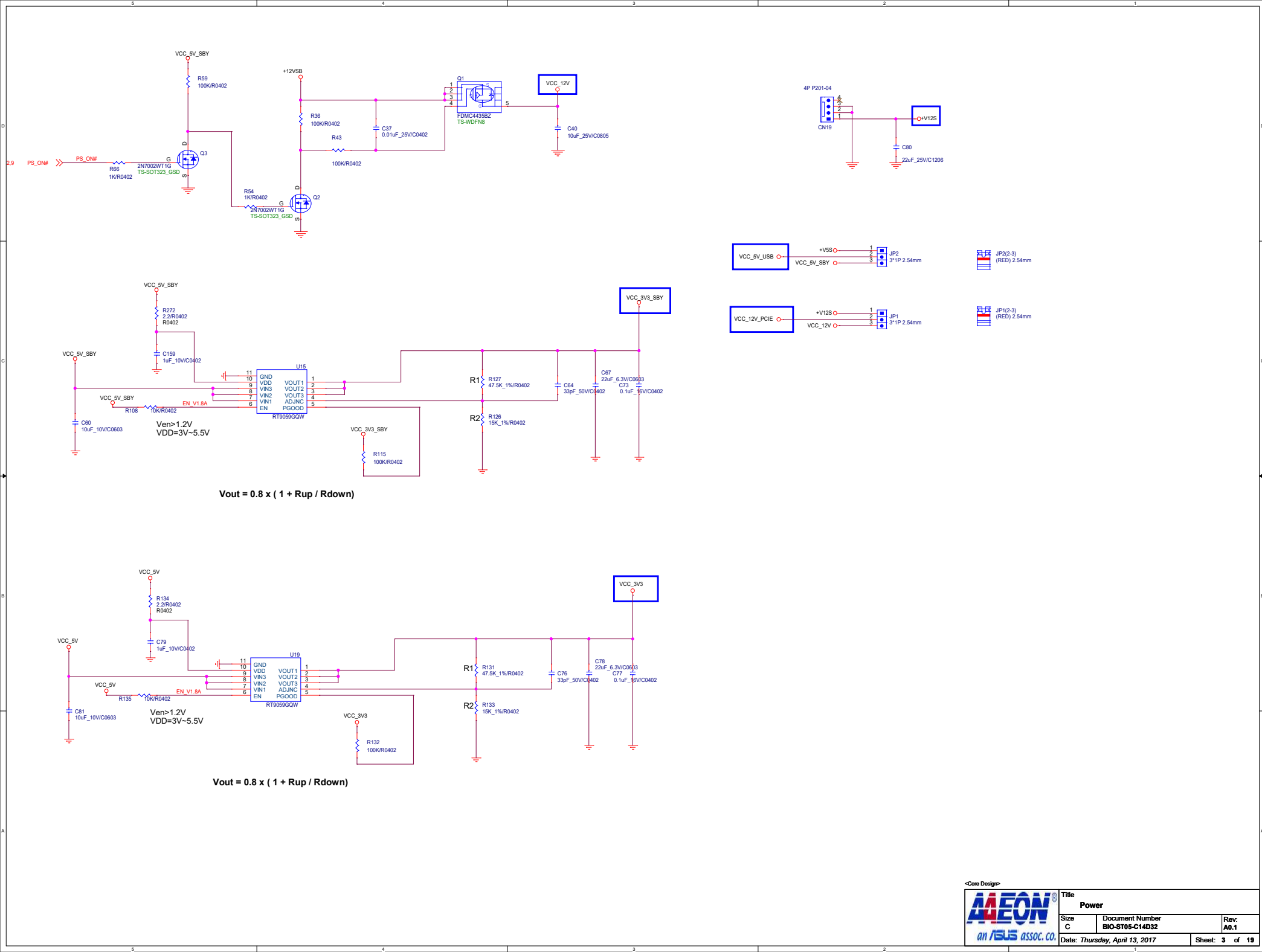


### Page Index

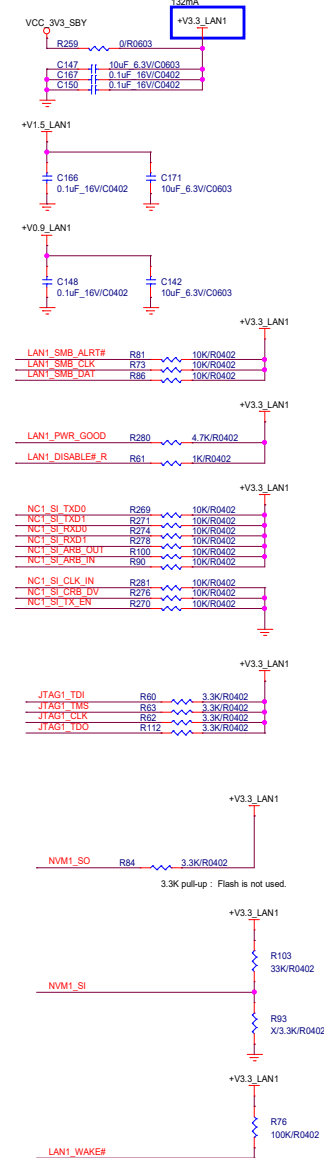
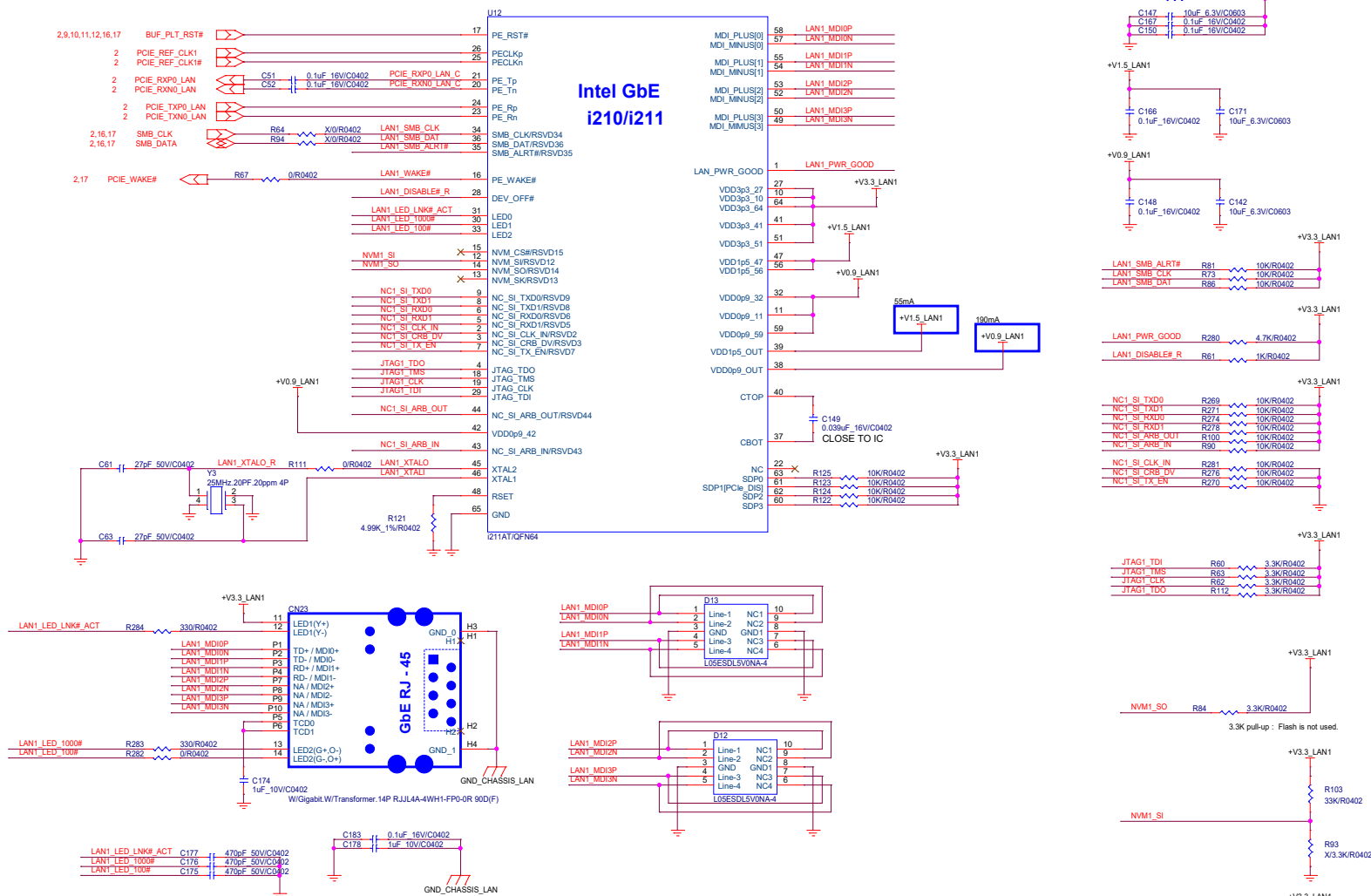
1	Cover Sheet
2	BIO
3	Power
4	i211
5	USB 3.0/USB 2.0
6	USB 2.0 Hub
7	Amplifier
8	12V to 5V
9	F81866
10	F81216-1
11	F81216-2
12	COM1~6
13	COM7~10
14	COM11~14
15	Ring/LPT
16	DIO x32
17	PCIe slot
18	Revision History 1
19	Revision History 2

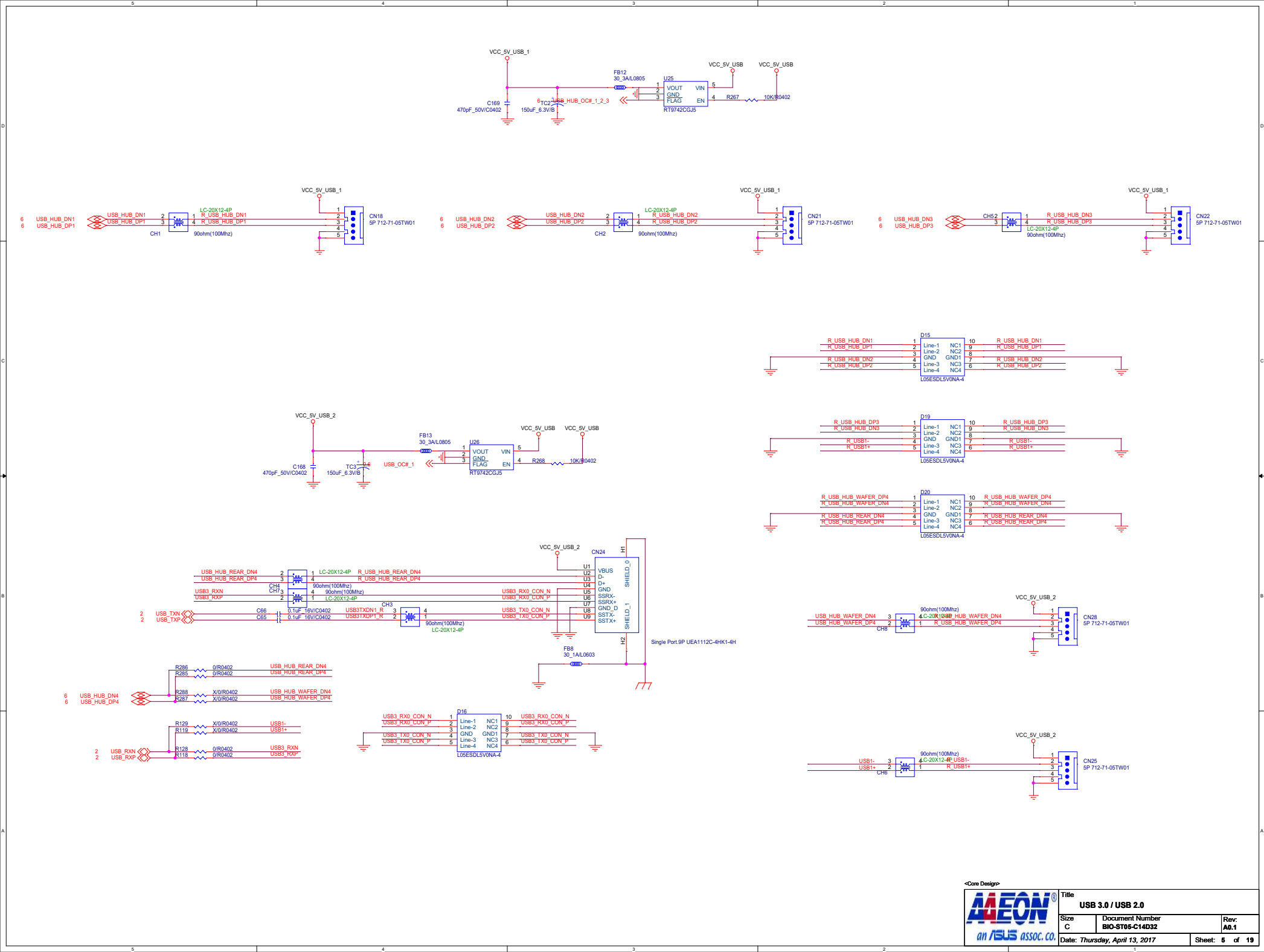
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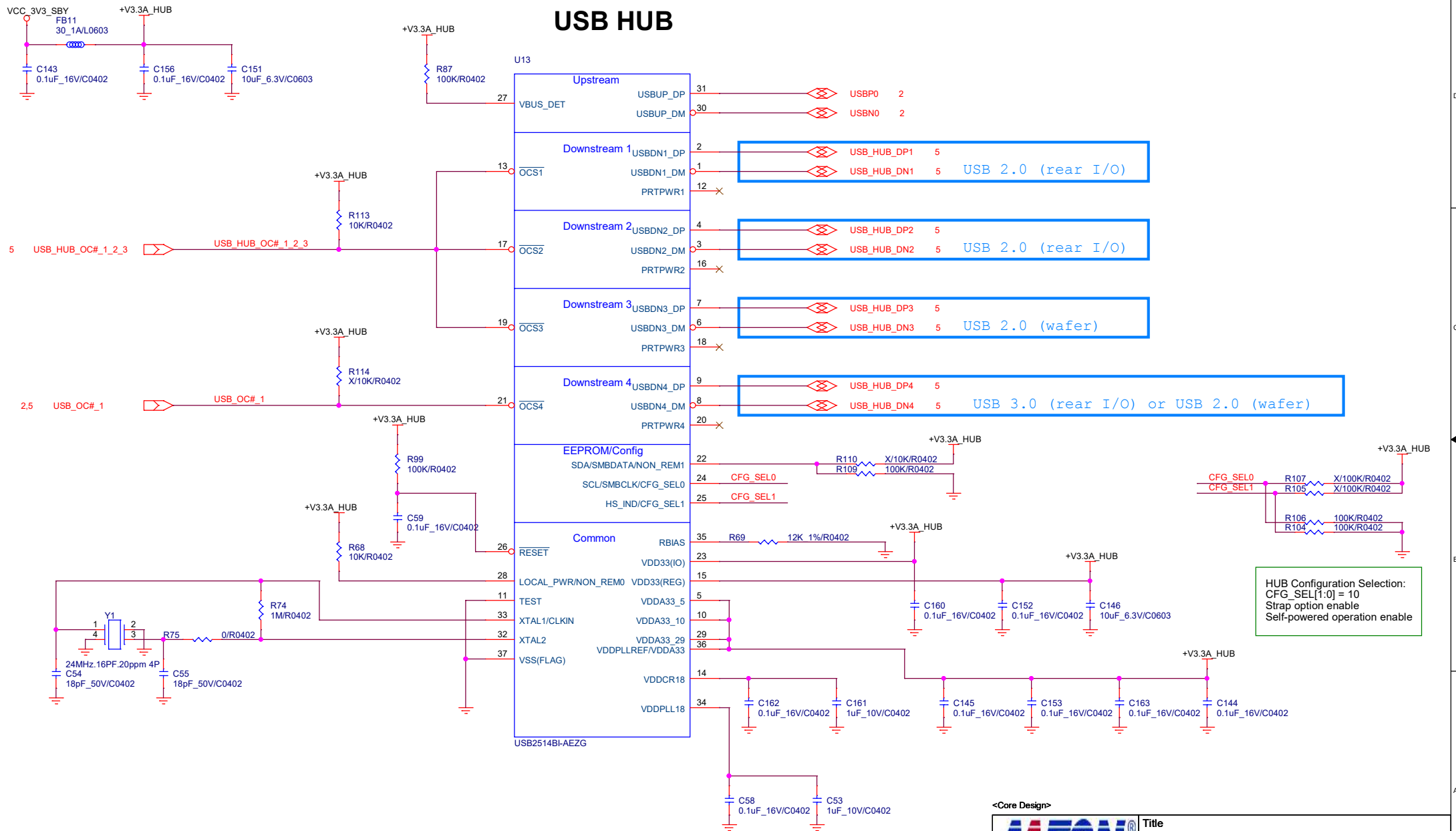




## Pearsonville(i211) /Springville(i210)



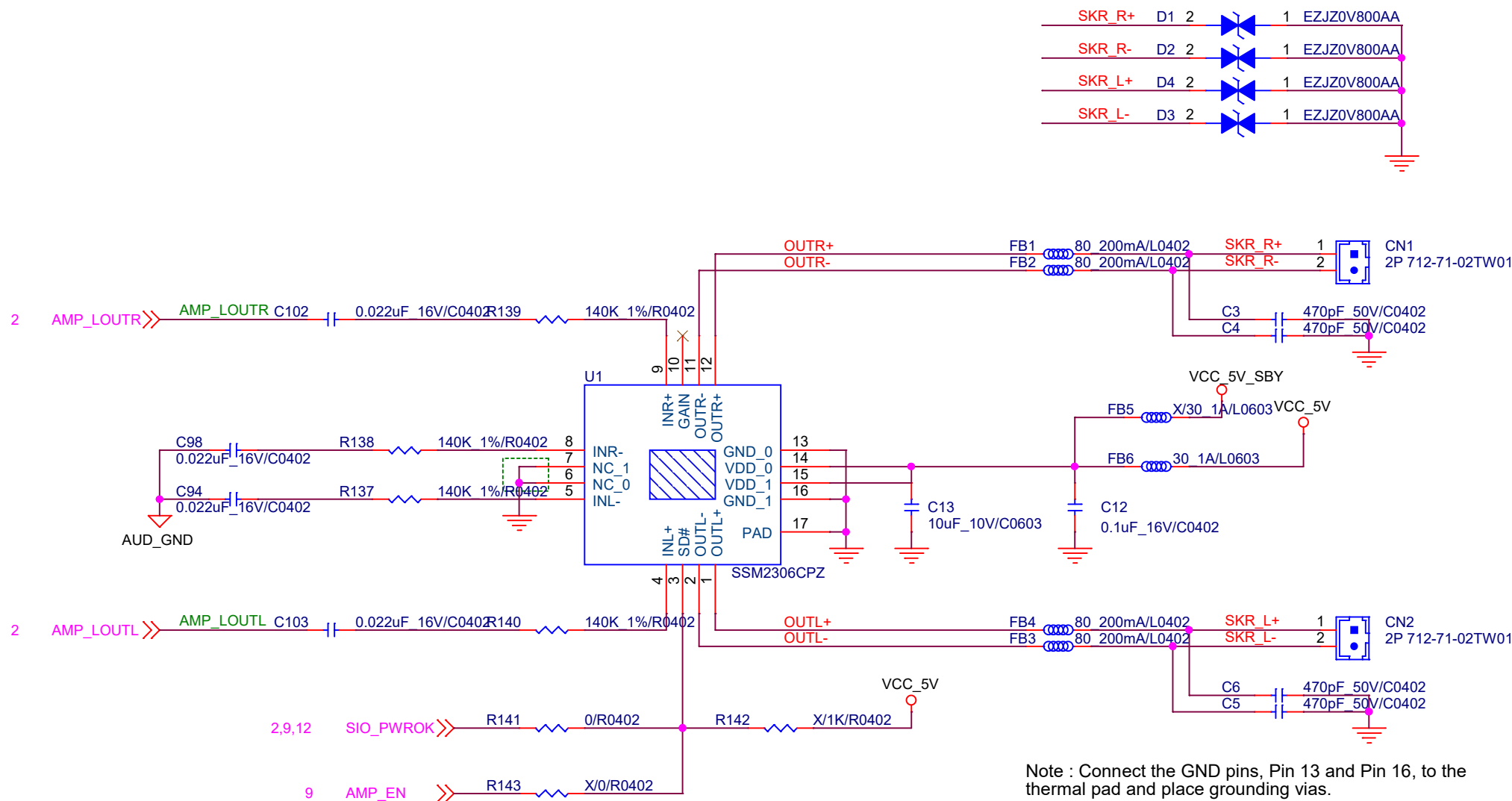




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Size B	Document Number <b>BIO-ST05-C14D32</b>	Rev: <b>A0.1</b>
Date: <b>Thursday, April 13, 2017</b>		Sheet: <b>6</b> of <b>19</b>



<Core Design>



Title <b>Amplifier</b>		
Size A	Document Number <b>BIO-ST05-C14D32</b>	Rev: <b>A0.1</b>
Date: <i>Thursday, April 13, 2017</i>		Sheet: <b>7</b> of <b>19</b>

[illegible]

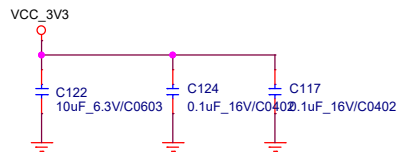
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Sheet: 8 of 19







13 CTS7#  
13 DSR7#  
13 RTS7#  
13 DTR7#  
13 RX7#  
13 TX7#  
13 DCD7#  
13 RI7#

CTS7#  
DSR7#  
RTS7#  
DTR7#  
RX7#  
TX7#  
DCD7#  
RI7#

RI8#  
DCD8#

RI8# 13  
DCD8# 13

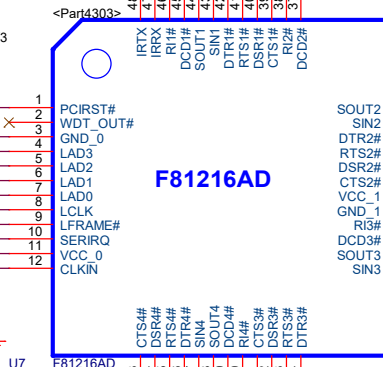
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0	0	1	0x2e/0x2f	0x77
0	1	0	0x4e/0x4f	0xa0
0	1	1	0x2e/0x2f	0xa0
1	0	0	0x4e/0x4f	0x87
1	0	1	0x2e/0x2f	0x87
1	1	0	0x4e/0x4f	0x67
1	1	1	0x2e/0x2f	0x67

2,4,9,11,12,16,17 BUF\_PLT\_RST#

2,9,11,16 LPC\_AD3  
2,9,11,16 LPC\_AD2  
2,9,11,16 LPC\_AD1  
2,9,11,16 LPC\_AD0  
2 LPC\_CLK\_2  
2,9,11,16 LPC\_FRAME#  
2,9,11 INT\_SERIRQ

9 F81216\_CLKIN\_1

LPC\_AD3  
LPC\_AD2  
LPC\_AD1  
LPC\_AD0  
LPC\_FRAME#

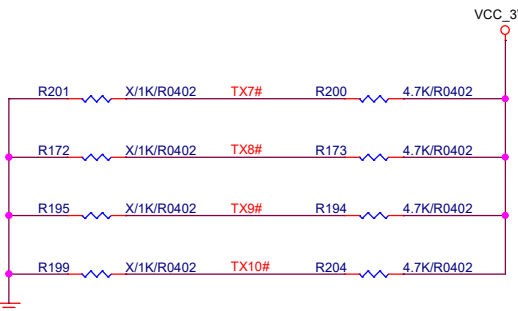
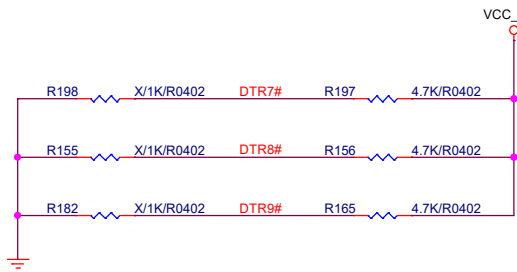
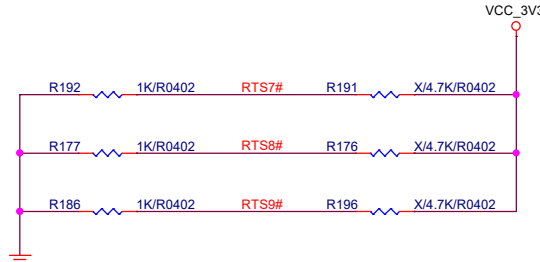


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13 RTS10#  
13 DTR10#  
13 RX10#  
13 TX10#  
13 DCD10#  
13 RI10#

CTS10#  
DSR10#  
RTS10#  
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DCD10#  
RI10#

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RTS9#  
DSR9#  
CTS9#

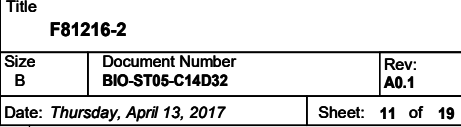
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CTS9# 13



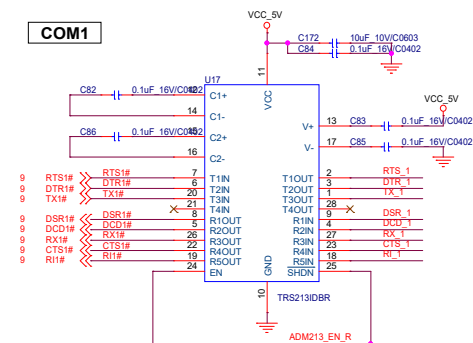
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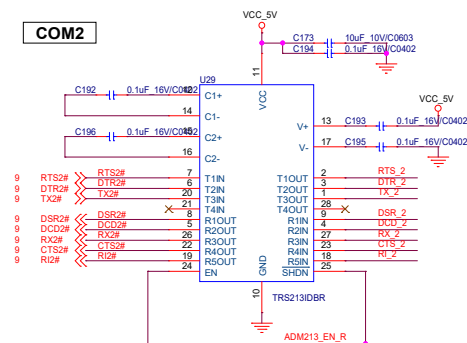
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Size B	Document Number <b>BIO-ST05-C14D32</b>	Rev: <b>A0.1</b>
Date: Thursday, April 13, 2017		Sheet: 10 of 19



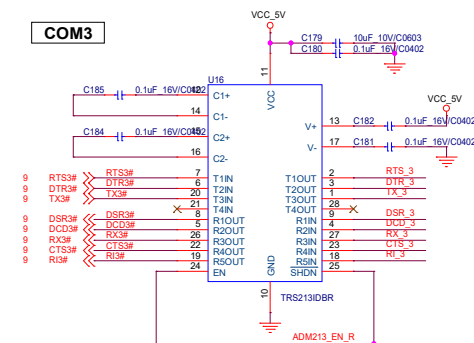
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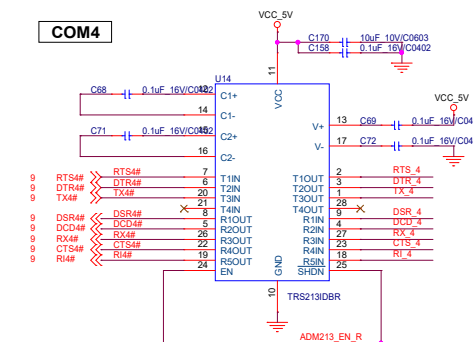
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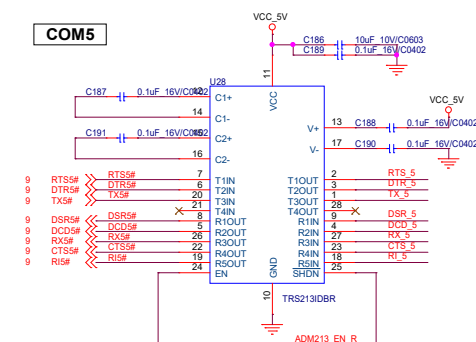
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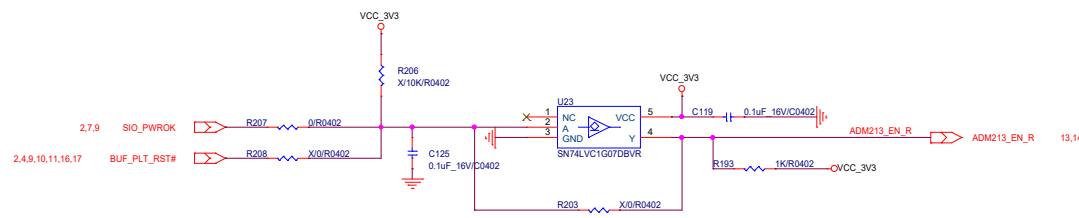
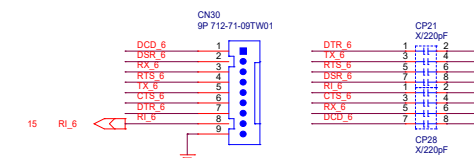
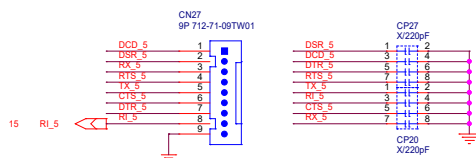
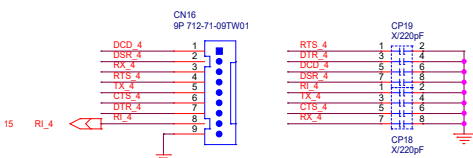
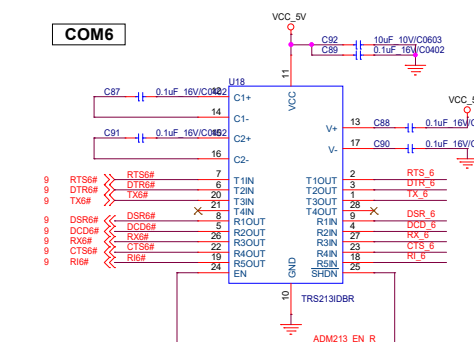
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COM5



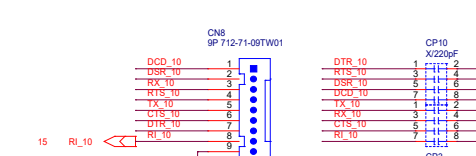
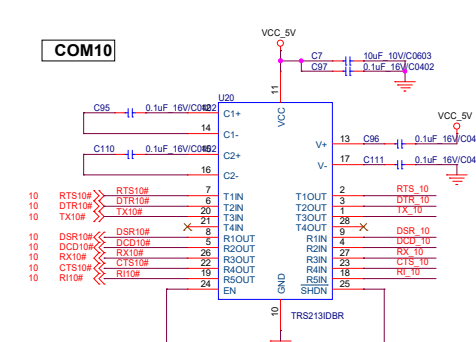
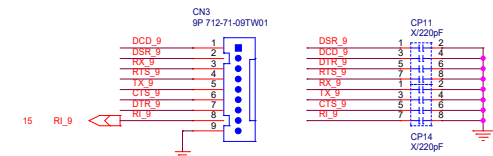
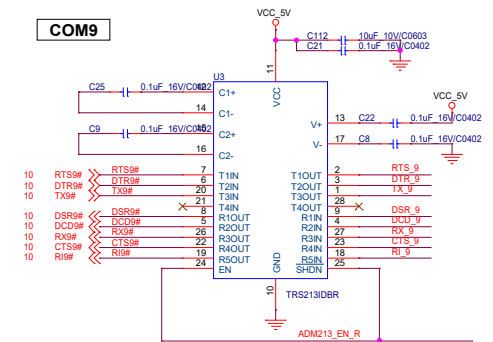
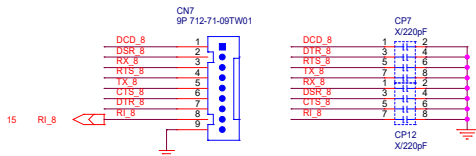
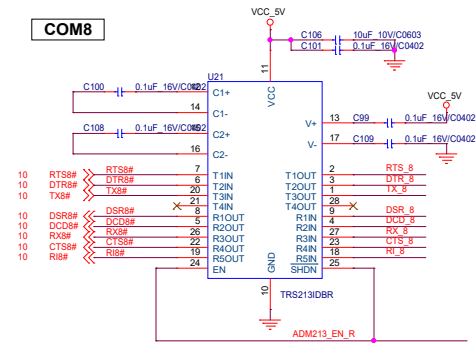
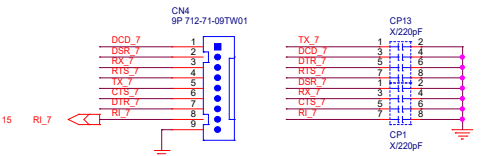
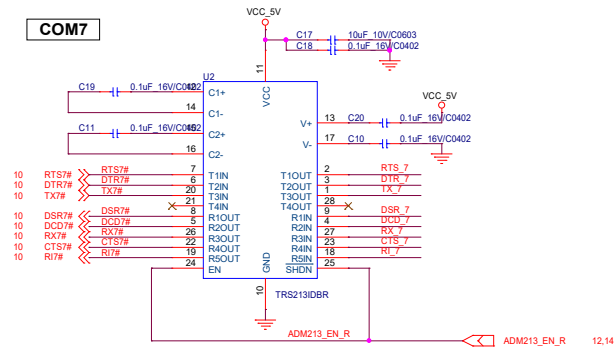
COM6



&lt;Core Design&gt;

**AEON**  
an /SUS ASSOC. CO.

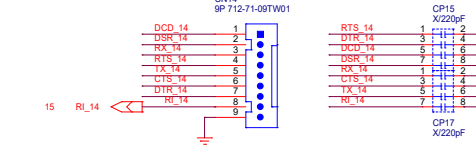
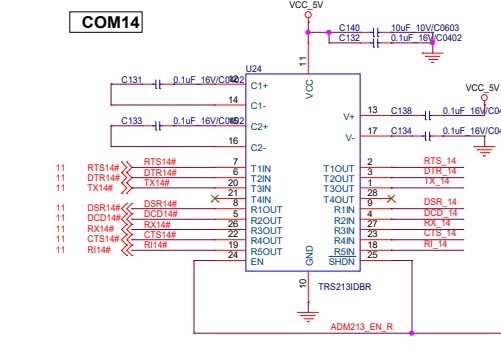
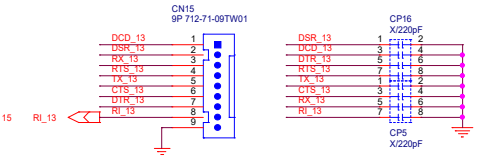
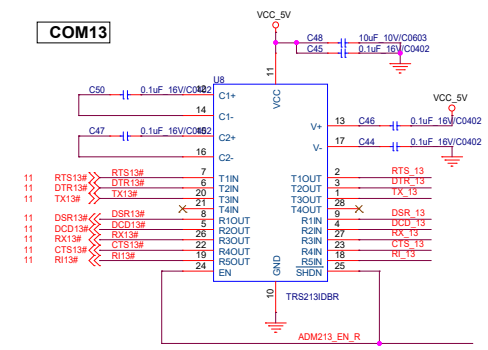
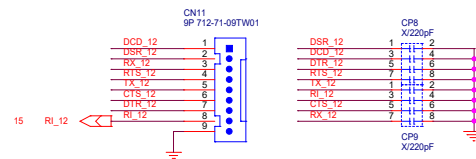
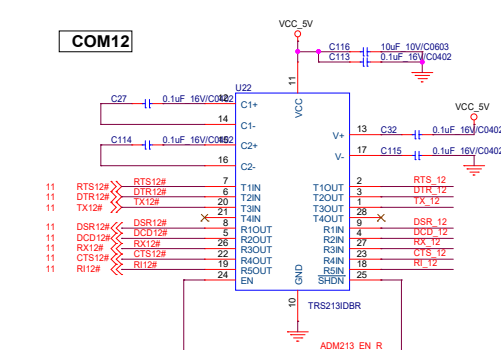
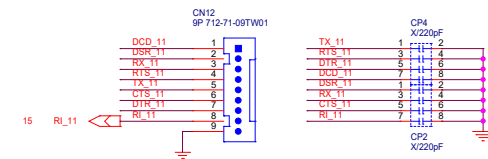
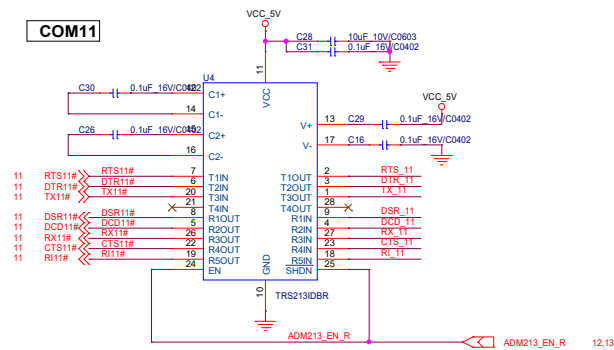
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Document Number: BIO-ST05-C14D32  
Date: Thursday, April 13, 2017  
Rev: A0.1  
Sheet: 12 of 19



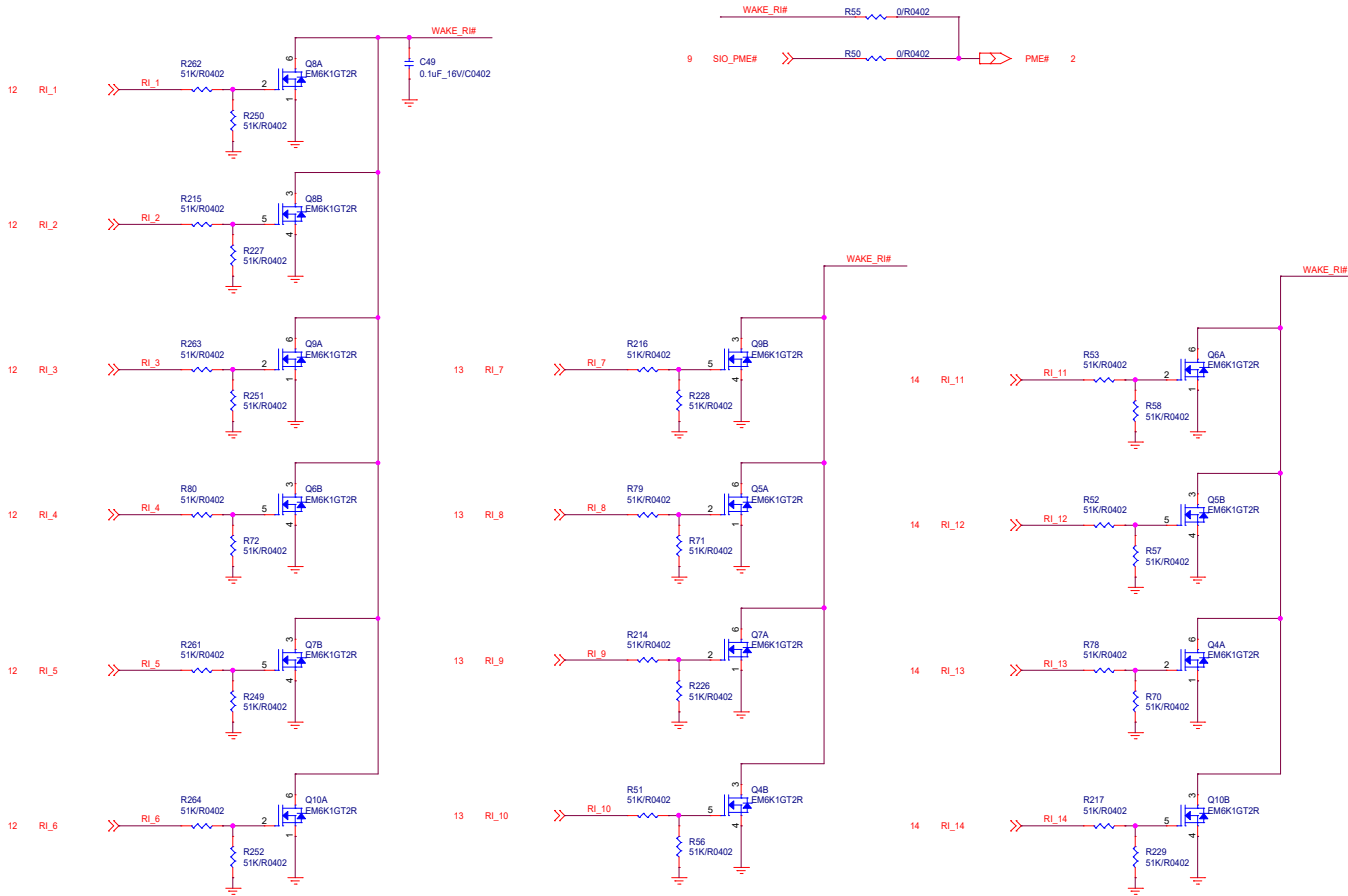
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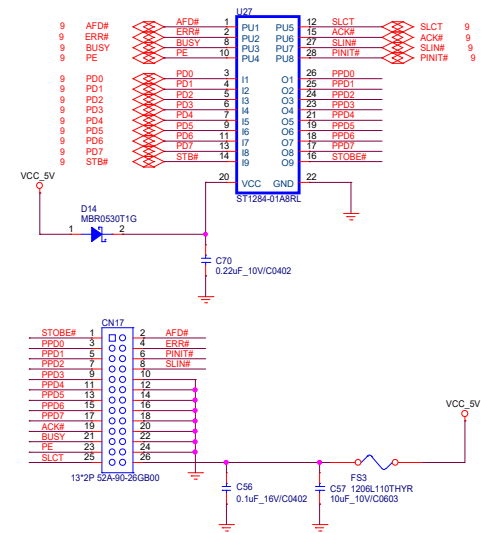
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C	Rev	A0.1
Date: Thursday, April 13, 2017		Sheet: 13 of 19

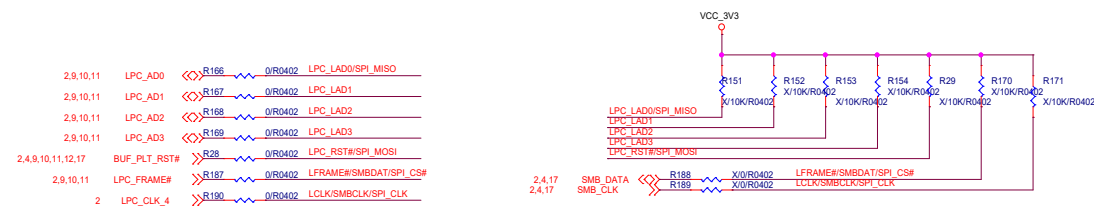
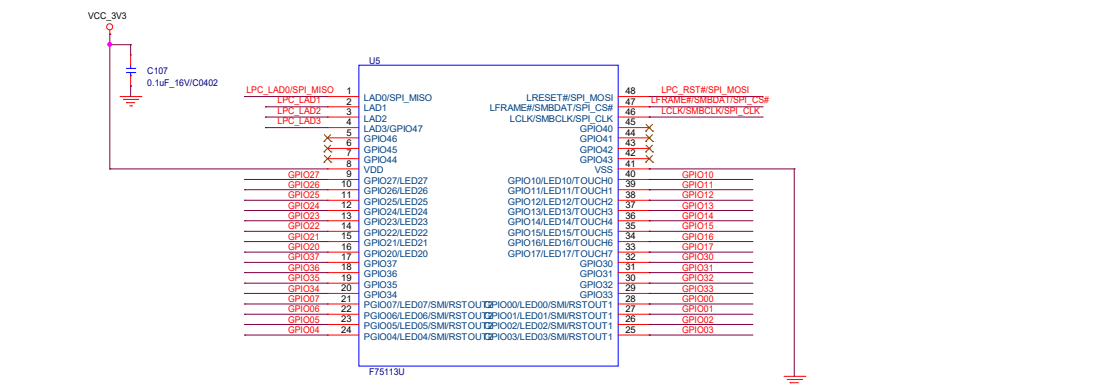


## Wake On Modem



**LPT**

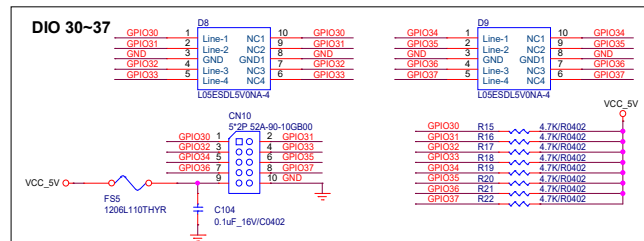
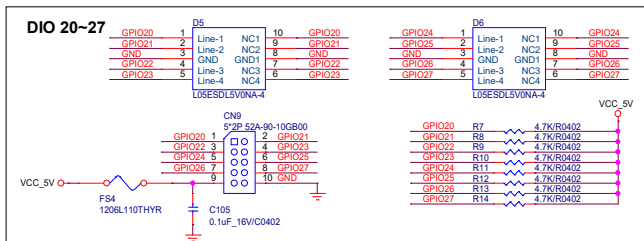
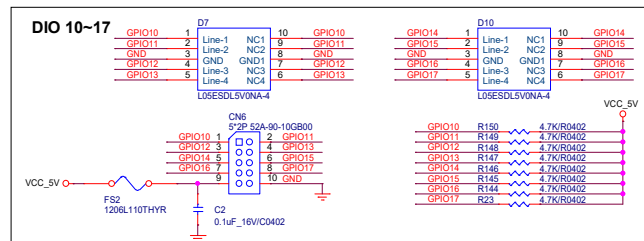
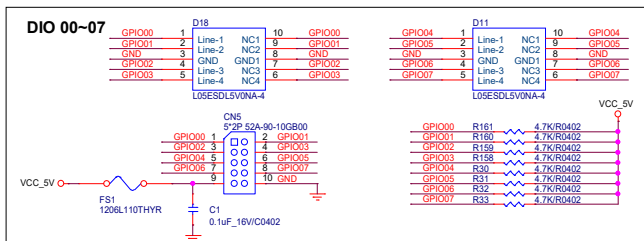




LPC Interface

When using SMBUS interface:  
1.LPC interface pins must be pull high.  
2.LPC signals are not allowed to connected to F75113

SMBUS Interface

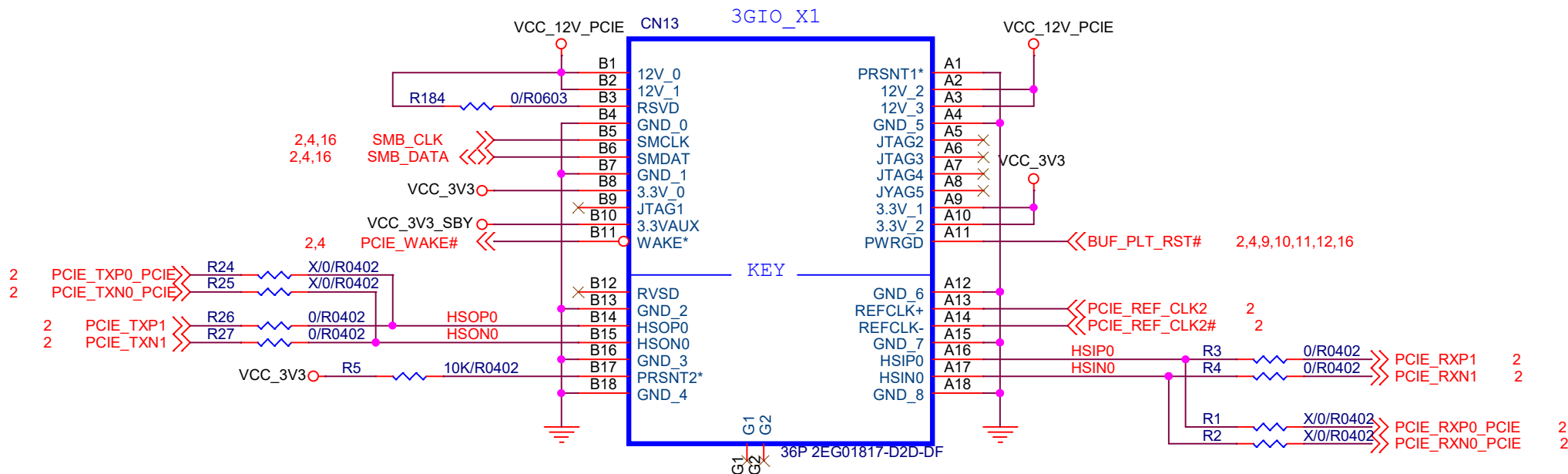


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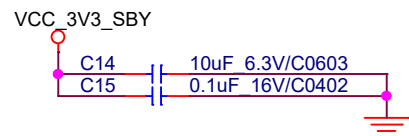
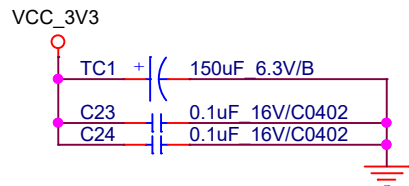
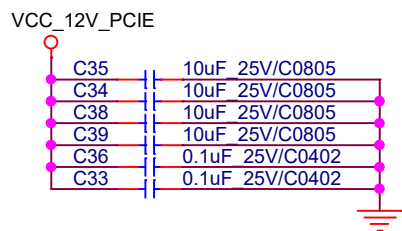


Title		
DIO x32		
Size	Document Number	Rev
C	BIO-ST05-C14D32	A0.1
Date: Thursday, April 13, 2017		Sheet: 16 of 19





+12V==>0.5A  
+3V3==>3A  
+3V3\_DUAL==>375mA



<Core Design>



Title		
PCIe slot		
Size A	Document Number BIO-ST05-C14D32	Rev: A0.1
Date: Thursday, April 13, 2017		Sheet: 17 of 19

Change History

Item	Date	Revision	Description	Page	Design By	Approve By

Change History

Item	Date	Revision	Description	Page	Design By	Approve By