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ITE Tech. Inc.

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Embedded Controller

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(For C Version)

ITE TECH. INC.

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ITE Tech. Inc.
Marketing Department
9F, No. 233-2, Baoqiao Rd., Xindian Dist,
New Taipei City, 23145, Taiwan, R.O.C.

Phone: (02) 29126889
Fax: (02) 2910-2551, 2910-2552

If you have any marketing or sales questions, please contact:
P.Y. Chang, at ITE Taiwan:
E-mail: p.y.chang@ite.com.tw, Tel: 886-2-29126889 X6052, Fax: 886-2-29102551

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Revision History

Section	Revision	Page No.
-	• "I" added to part no., indicating its industrial application • Operating Temperature (Ta) changed into "-40°C to +85°C" for industrial application	-

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1. Features

- **32-bit Andes® N801 Micro-controller**
  - 3-stage pipeline
  - AndeStar™ V3m instruction set
  - 16/32-bit mixed instructions with 16 GPRs
  - Variable frequency range to gain maximum performance, up to 96MHz core clock
  - Hardware Multiplier/Divider
  - 12KB data-local-memory (DLM)

- **eSPI Interface**
  - Compatible with the eSPI specification v1.0
  - Supports Peripheral Channel
  - Supports VW IRQ/System Event
  - Supports Master Attached Flash Sharing
  - Supports 20MHz to 66MHz

- **LPC Bus Interface**
  - Compatible with LPC specification v1.1
  - Supports I/O read/write
  - Supports Memory read/write
  - Supports FWH read/write
  - Serial IRQ
  - Supports LPC 19.2MHz to 33MHz
  - Supports 3.3V/1.8V level

- **Flash Interface**
  - 128K-byte embedded flash (IT5121E/VG-128)
  - 192K-byte embedded flash (IT5121E/VG-192)
  - 256K-byte embedded flash (IT5121E/VG-256)
  - Over 100,000 erase/program cycles
  - Over 10-year data retention
  - 3.3V/1.8V level supported by FSPI

- **Crystal-Free**
  - Built-in 32.768 kHz clock generator
  - External crystal oscillator not required

- **SMBus Controller**
  - SMBus spec. 2.0
  - 6 SMBus masters + 3 slaves
  - 6 SMBus channels
  - Compatible with I2C cycles

- **System Wake-Up Control**
  - Modem RI# wake-up
  - IRQ/SMI# routing

- **EC Wake-up Control**
  - External/internal wake-up events
  - WUI pins

- **Interrupt Controller**
  - interrupt events to EC
  - Fixed priority

- **Timer / Watch Dog Timer**
  - 2 external 8-bit timers and 2 external 24-bit timers in ETWD module, based on 32.768 k clock source
  - 1 external 16-bit WDT in ETWD module, based on 32.768 k clock source

- **UART**
  - 2 standard serial ports (legacy 16C550 COM1/COM2)
    Baud rate up to 460800
  - Receiver/Transmitter can be enabled separately

- **ACPI Power Management Channel**
  - 5 Power management channels
  - Compatible and enhanced mode

- **BRAM**
  - EC registers shared with RTCT SRAM

- **GPIO**
  - Supports 83-port GPIO
  - Programmable pull up/pull down
  - Schmitt trigger for input
  - Supports 28-port 1.8V input level

- **External GPIO Controller (EGPC)**
  - Communicates with four IT8301 or one IT8302 chip
  - Each IT8301 supporting 38 GPIO ports
  - One IT8302 supporting 16 GPIO ports

- **KBC Interface**
  - 8042 style KBC interface
  - Legacy IRQ1 and IRQ12
  - Fast A20G and KB reset

- **ADC**
  - 11 ADC channels (8 external)
  - 10-bit resolution (+/- 6LSB)
  - 3 voltage comparators

- **DAC**
  - 4 DAC channels
  - 8-bit DAC

- **PWM**
  - 8 PWM channels
  - 32.768 kHz of base clock frequency
  - 8 duty cycles of resolution
  - 8/16-bit common input clock prescaler
  - 4 prescalers for 8 PWM output used for devices with different frequencies
  - Supports PWM open-drain output
  - Supports two sets of tachometers; each can be switched from two external pins.

- **PECI Host**
  - PECI spec. 2.0/3.1
  - Supports 16-byte write/read length
  - Supports FCS checking mechanism
  - Supports AW_FCS hardwired mechanism
  - Supports adjustable V_{TT} level

- **PS/2 Interface**
  - 3 PS/2 interface
  - Hardware/Software mode selection

- **KB Matrix Scan**
  - Hardware keyboard scan
  - 18x8 keyboard matrix scan

- **SPI Slave Interface (SSPI)**
  - 2-channel SPI Master, Freq between 575 kHz and 4.6MHz
  - 4-wire or 3-wire (bi-directional data) I/F
  - Supports n-bit transmission (n = 1 ~ 8)
  - SPI Mode 0, 1, 2, 3

- **In-System Programming**
  - ISP via parallel port interface on existing KBS connector
  - Fast flash programming with software provided by ITE

- **Consumer IR**
  - Supports 27-58 KHz, 400-500 KHz device
  - Supports remote power-on switch

- **Power Consumption**
  - Standby with Sleep mode current if Crystal-Free: 50 μA

- **CEC**
  - Suitable for HDMI 1.4a standard

- **TMR**
  - Supports four channels
  - Supports 8-bit/16-bit pulse mode, and toggle mode

- **RTCT**
  - Supports 2 alarms

- **Package**
  - LQFP 128 / VFBGA 128

2. General Description

The IT5121 is a highly integrated embedded controller with system functions suitable for mobile system applications. The IT5121 directly interfaces to the LPC bus and provides ACPI embedded controller function, keyboard controller (KBC) and matrix scan, PWM and ADC for hardware monitor, PS/2 interface for external keyboard/mouse devices, BRAM, CIR and system wake-up functions for system power management.

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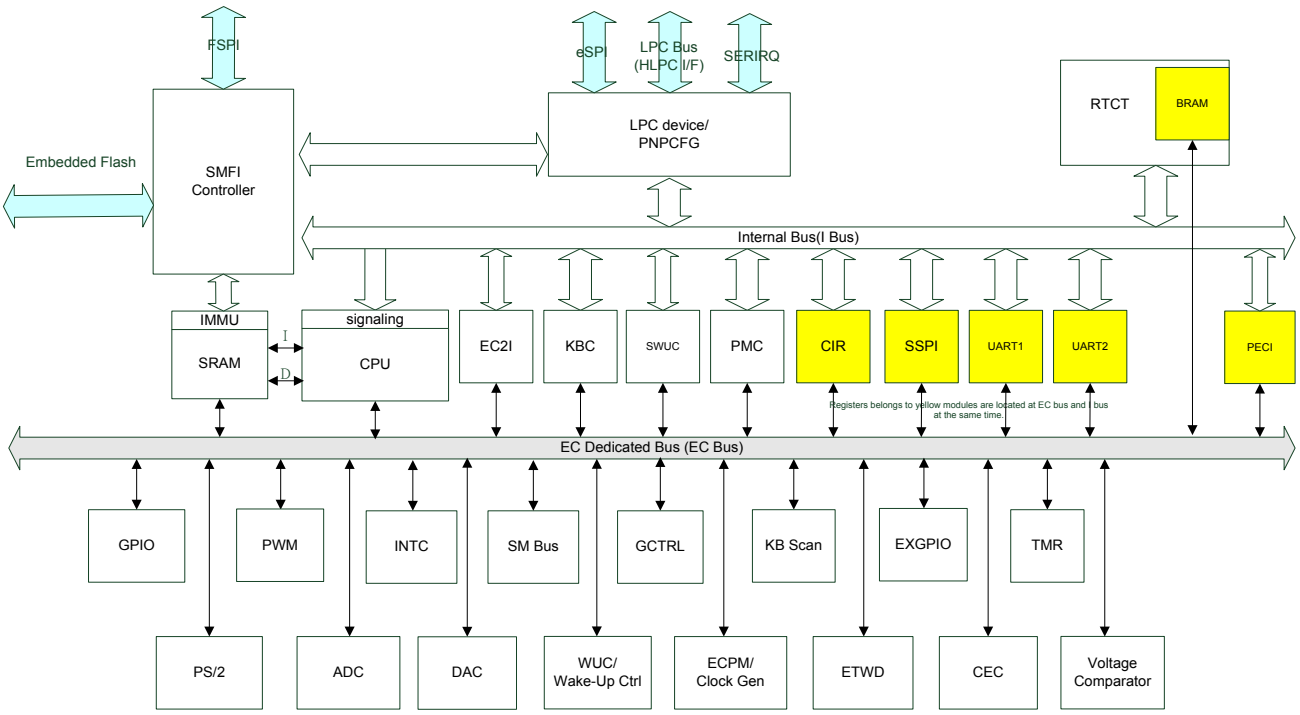
3. System Block Diagram

3.1 Block Diagram

- **IT5121:**



- **Host Domain:**
  LPC, eSPI, PNPCFG, RTCT logic device, host parts of SMFI/SWUC/KBC/PMC logical devices and host parts of EC2I.

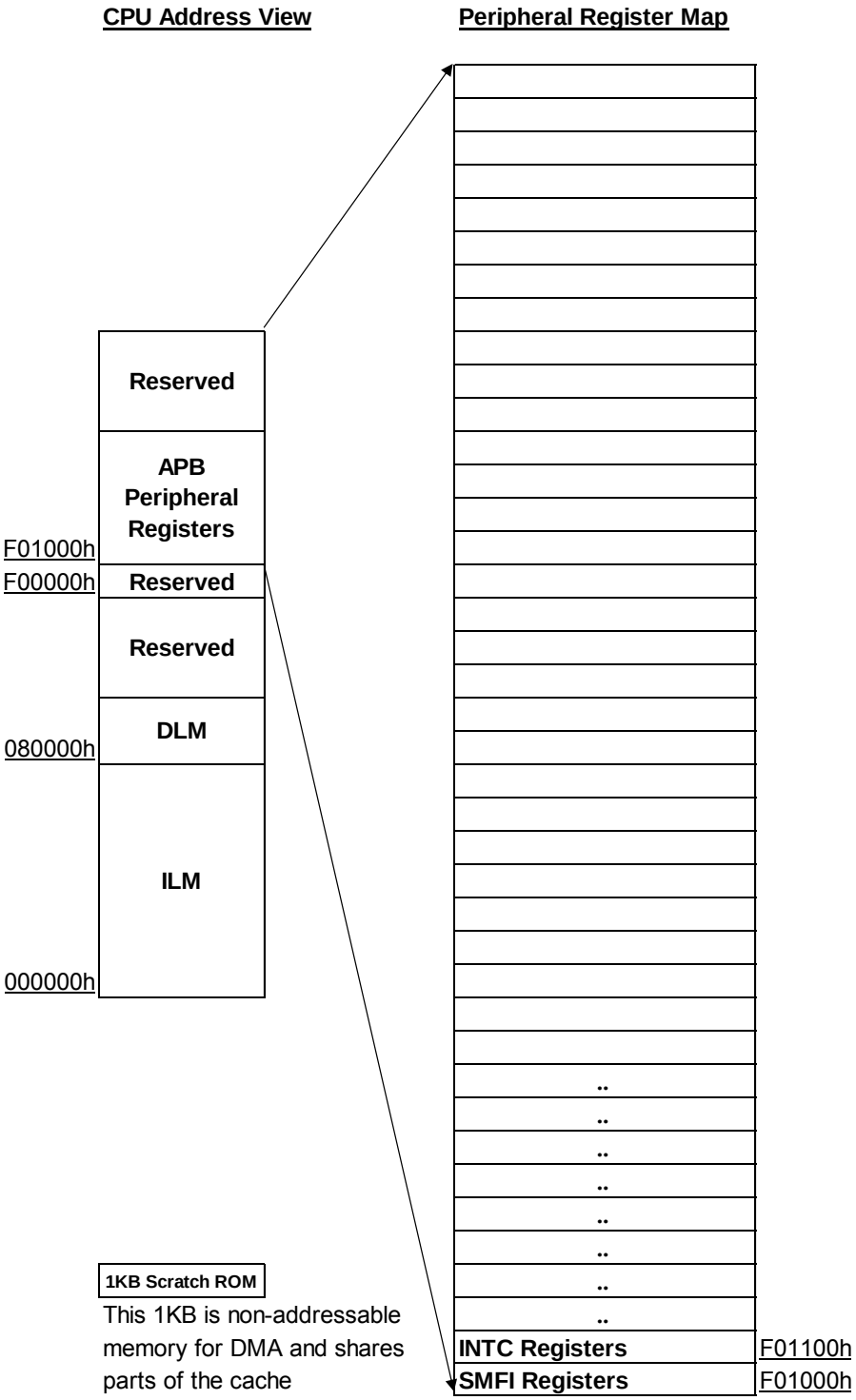
- **EC Domain:**
  INTC, WUC KB Scan, GPIO, ECPM, SMB, PS/2, DAC, ADC, PWM, ETWD, EC2I, GCTRL, BRAM, EGPC, DBGR, CEC , EC parts of SMFI/SWUC/KBC/PMC and EC parts of EC2I.

- **Double-mapping Module:**
  CIR, BRAM, SSPI, PECI, UART1 and UART2.

Note: The SPI master (abbreviated as SSPI) is connected to the slow (contrast to SPI flash) SPI slave(s).

3.2 EC Mapped Memory Space

Figure 3-1. EC Memory Map



3.3 Register Abbreviation

The register abbreviations and access rules are listed below:

R	**READ ONLY**. If a register is read only, writing to this register has no effect.
W	**WRITE ONLY**. If a register is write only, reading to this register returns all zero.
R/W	**READ/WRITE**. A register with this attribute can be read and written.
RC	**READ CLEAR**. If a register is read clear, reading to this register clears the register to ‘0’.
R/WC	**READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, writing 1 clears the corresponding bit and writing 0 has no effect.

BFNAME@REGNAME	This abbreviation may be shown in figures to represent one bit in a register or one field in a register.

The used radix indicator suffixes in this specification are listed below:
Decimal number: "d" suffix or no suffix
Binary number: "b" suffix
Hexadecimal number: "h" suffix

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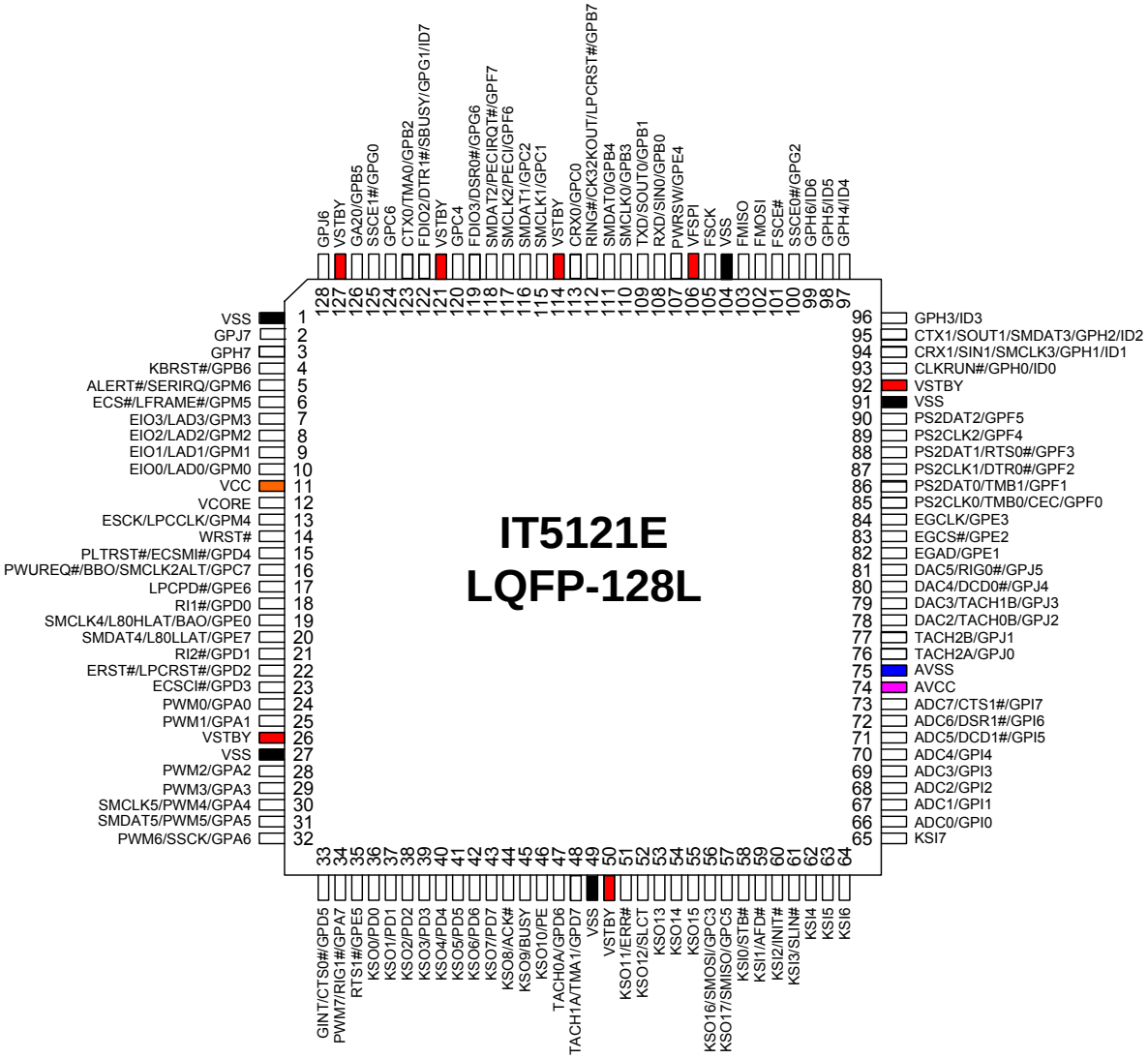
4. Pin Configuration

4.1 Top View

IT5121E Top View



IT5121VG Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	RING#/CK32KOUT/LPCRST#/GPB7	SMDAT0/GPB4	TXD/SOUT0/GPB1	RXD/SIN0/GPB0	PWRSW/GPE4	FMISO	FSCE#	GPH5/ID5	GPH3/ID3	PS2CLK1/DTR0#/GPF2	PS2CLK0/TMB0/CEC/GPF0	EGCS#/GPE2	EGAD/GPE1	A
B	SMCLK2/PECI/GPF6	SMDAT1/GPC2	SMCLK1/GPC1	SMCLK0/GPB3	FSCK	FMOSI	GPH6/ID6	GPH4/ID4	PS2DAT2/GPF5	PS2DAT1/RTS0#/GPF3	PS2DAT0/TMB1/GPF1	EGCLK/GPE3	DAC4/DCD0#/GPJ4	B
C	SMDAT2/PECIRQT#/GPF7	GPC4										DAC5/RIG0#/GPJ5	DAC3/TACH1B/GPJ3	C
D	FDIO3/DSR0#/GPG6	CTX0/TMA0/GPB2		VSTBY	VSTBY	VSS	CTX1/SOUT1/SMDAT3/GPH2/ID2	CLKRUN#/GPH0/ID0	PS2CLK2/GPF4	VSTBY		DAC2/TACH0B/GPJ2	TACH2B/GPJ1	D
E	GPC6	SSCE1#/GPG0		VSTBY	CRX0/GPC0	VFSPI	SSCE0#/GPG2	CRX1/SIN1/SMCLK3/GPH1/ID1	AVCC	AVSS		TACH2A/GPJ0	ADC7/CTS1#/GPI7	E
F	GA20/GPB5	GPJ6		FDIO2/DTR1#/SBUSY/GPG1/ID7	VSS				ADC3/GPI3	ADC5/DCD1#/GPI5		ADC6/DSR1#/GPI6	ADC4/GPI4	F
G	GPJ7	ALERT#/SERIRQ/GPM6		VSS	VSS				KSI7	ADC0/GPI0		ADC2/GPI2	ADC1/GPI1	G
H	ECS#/LFRAME#/GPM5	EIO3/LAD3/GPM3		KBRST#/GPB6	VSS				KSI4	KSI5		KSI3/SLIN#	KSI6	H
J	EIO2/LAD2/GPM2	EIO1/LAD1/GPM1		GPH7	VCC	SMDAT5/PWM5/GPA5	KSO1/PD1	KSO5/PD5	KSI2/INIT#	KSO17/SMISO/GPC5		KSI0/STB#	KSI1/AFD#	J
K	EIO0/LAD0/GPM0	ESCK/LPCCLK/GPM4		VSTBY	VCORE	SMCLK5/PWM4/GPA4	PWM7/RIG1#/GPA7	KSO4/PD4	KSO9/BUSY	VSTBY		KSO15	KSO16/SMOSI/GPC3	K
L	WRST#	PLTRST#/ECSMI#/GPD4										KSO13	KSO14	L
M	LPCPD#/GPE6	PWUREQ#/BBO/SMCLK2ALT/GPC7	SMDAT4/L80LLAT/GPE7	ERST#/LPCRST#/GPD2	PWM0/GPA0	PWM2/GPA2	PWM6/SSCK/GPA6	KSO0/PD0	KSO3/PD3	KSO7/PD7	TACH0A/GPD6	TACH1A/TMA1/GPD7	KSO12/SLCT	M
N	RI1#/GPD0	SMCLK4/L80HLAT/BAO/GPE0	RI2#/GPD1	ECSCI#/GPD3	PWM1/GPA1	PWM3/GPA3	GINT/CTS0#/GPD5	RTS1#/GPE5	KSO2/PD2	KSO6/PD6	KSO8/ACK#	KSO10/PE	KSO11/ERR#	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Table 4-1. Pins Listed in Numeric Order (128-pin LQFP)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	33	GINT/CTS0#/GPD5	65	KSI7	97	GPH4/ID4
2	GPJ7	34	PWM7/RIG1#/GPA7	66	ADC0/GPI0	98	GPH5/ID5
3	GPH7	35	RTS1#/GPE5	67	ADC1/GPI1	99	GPH6/ID6
4	KBRST#/GPB6	36	KSO0/PD0	68	ADC2/GPI2	100	SSCE0#/GPG2
5	ALERT#/SERIRQ/GPM6	37	KSO1/PD1	69	ADC3/GPI3	101	FSCE#
6	ECS#/LFRAME#/GPM5	38	KSO2/PD2	70	ADC4/GPI4	102	FMOSI
7	EIO3/LAD3/GPM3	39	KSO3/PD3	71	ADC5/DCD1#/GPI5	103	FMISO
8	EIO2/LAD2/GPM2	40	KSO4/PD4	72	ADC6/DSR1#/GPI6	104	VSS
9	EIO1/LAD1/GPM1	41	KSO5/PD5	73	ADC7/CTS1#/GPI7	105	FSCK
10	EIO0/LAD0/GPM0	42	KSO6/PD6	74	AVCC	106	VFSPI
11	VCC	43	KSO7/PD7	75	AVSS	107	PWRSW/GPE4
12	VCORE	44	KSO8/ACK#	76	TACH2A/GPJ0	108	RXD/SIN0/GPB0
13	ESCK/LPCCLK/GPM4	45	KSO9/BUSY	77	TACH2B/GPJ1	109	TXD/SOUT0/GPB1
14	WRST#	46	KSO10/PE	78	DAC2/TACH0B/GPJ2	110	SMCLK0/GPB3
15	PLTRST#/ECSMI#/GPD4	47	TACH0A/GPD6	79	DAC3/TACH1B/GPJ3	111	SMDAT0/GPB4
16	PWUREQ#/BBO/SMCLK2ALT/GPC7	48	TACH1A/TMA1/GPD7	80	DAC4/DCD0#/GPJ4	112	RING#/CK32KOUT/LPCRST#/GPB7
17	LPCPD#/GPE6	49	VSS	81	DAC5/RIG0#/GPJ5	113	CRX0/GPC0
18	RI1#/GPD0	50	VSTBY	82	EGAD/GPE1	114	VSTBY
19	SMCLK4/L80HLAT/BAO/GPE0	51	KSO11/ERR#	83	EGCS#/GPE2	115	SMCLK1/GPC1
20	SMDAT4/L80LLAT/GPE7	52	KSO12/SLCT	84	EGCLK/GPE3	116	SMDAT1/GPC2
21	RI2#/GPD1	53	KSO13	85	PS2CLK0/TMB0/CEC/GPF0	117	SMCLK2/PECI/GPF6
22	ERST#/LPCRST#/GPD2	54	KSO14	86	PS2DAT0/TMB1/GPF1	118	SMDAT2/PECIRQT#/GPF7
23	ECSCI#/GPD3	55	KSO15	87	PS2CLK1/DTR0#/GPF2	119	FDIO3/DSR0#/GPG6
24	PWM0/GPA0	56	KSO16/SMOSI/GPC3	88	PS2DAT1/RTS0#/GPF3	120	GPC4
25	PWM1/GPA1	57	KSO17/SMISO/GPC5	89	PS2CLK2/GPF4	121	VSTBY
26	VSTBY	58	KSI0/STB#	90	PS2DAT2/GPF5	122	FDIO2/DTR1#/SBUSY/GPG1/ID7
27	VSS	59	KSI1/AFD#	91	VSS	123	CTX0/TMA0/GPB2
28	PWM2/GPA2	60	KSI2/INIT#	92	VSTBY	124	GPC6
29	PWM3/GPA3	61	KSI3/SLIN#	93	CLKRUN#/GPH0/ID0	125	SSCE1#/GPG0
30	SMCLK5/PWM4/GPA4	62	KSI4	94	CRX1/SIN1/SMCLK3/GPH1/ID1	126	GA20/GPB5
31	SMDAT5/PWM5/GPA5	63	KSI5	95	CTX1/SOUT1/SMDAT3/GPH2/ID2	127	VSTBY
32	PWM6/SSCK/GPA6	64	KSI6	96	GPH3/ID3	128	GPJ6

Table 4-2. Pins Listed in Numeric Order (128-pin VFBGA)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	RING#/CK32KOUT/LPCRST#/GPB7	D4	VSTBY	G9	KSI7	K12	KSO15
A2	SMDAT0/GPB4	D5	VSTBY	G10	ADC0/GPI0	K13	KSO16/SMOSI/GPC3
A3	TXD/SOUT0/GPB1	D6	VSS	G12	ADC2/GPI2	L1	WRST#
A4	RXD/SIN0/GPB0	D7	CTX1/SOUT1/SMDAT3/GPH2/ID2	G13	ADC1/GPI1	L2	PLTRST#/ECSMI#/GPD4
A5	PWRSW/GPE4	D8	CLKRUN#/GPH0/ID0	H1	ECS#/LFRAME#/GPM5	L12	KSO13
A6	FMISO	D9	PS2CLK2/GPF4	H2	EIO3/LAD3/GPM3	L13	KSO14
A7	FSCE#	D10	VSTBY	H4	KBRST#/GPB6	M1	LPCPD#/GPE6
A8	GPH5/ID5	D12	DAC2/TACH0B/GPJ2	H5	VSS	M2	PWUREQ#/BBO/SMCLK2ALT/GPC7
A9	GPH3/ID3	D13	TACH2B/GPJ1	H9	KSI4	M3	SMDAT4/L80LLAT/GPE7
A10	PS2CLK1/DTR0#/GPF2	E1	GPC6	H10	KSI5	M4	ERST#/LPCRST#/GPD2
A11	PS2CLK0/TMB0/CEC/GPF0	E2	SSCE1#/GPG0	H12	KSI3/SLIN#	M5	PWM0/GPA0
A12	EGCS#/GPE2	E4	VSTBY	H13	KSI6	M6	PWM2/GPA2
A13	EGAD/GPE1	E5	CRX0/GPC0	J1	EIO2/LAD2/GPM2	M7	PWM6/SSCK/GPA6
B1	SMCLK2/PECI/GPF6	E6	VFSPI	J2	EIO1/LAD1/GPM1	M8	KSO0/PD0
B2	SMDAT1/GPC2	E7	SSCE0#/GPG2	J4	GPH7	M9	KSO3/PD3
B3	SMCLK1/GPC1	E8	CRX1/SIN1/SMCLK3/GPH1/ID1	J5	VCC	M10	KSO7/PD7
B4	SMCLK0/GPB3	E9	AVCC	J6	SMDAT5/PWM5/GPA5	M11	TACH0A/GPD6
B5	FSCK	E10	AVSS	J7	KSO1/PD1	M12	TACH1A/TMA1/GPD7
B6	FMOSI	E12	TACH2A/GPJ0	J8	KSO5/PD5	M13	KSO12/SLCT
B7	GPH6/ID6	E13	ADC7/CTS1#/GPI7	J9	KSI2/INIT#	N1	RI1#/GPD0
B8	GPH4/ID4	F1	GA20/GPB5	J10	KSO17/SMISO/GPC5	N2	SMCLK4/L80HLAT/BAO/GPE0
B9	PS2DAT2/GPF5	F2	GPJ6	J12	KSI0/STB#	N3	RI2#/GPD1
B10	PS2DAT1/RTS0#/GPF3	F4	FDIO2/DTR1#/SBUSY/GPG1/ID7	J13	KSI1/AFD#	N4	ECSCI#/GPD3
B11	PS2DAT0/TMB1/GPF1	F5	VSS	K1	EIO0/LAD0/GPM0	N5	PWM1/GPA1
B12	EGCLK/GPE3	F9	ADC3/GPI3	K2	ESCK/LPCCLK/GPM4	N6	PWM3/GPA3
B13	DAC4/DCD0#/GPJ4	F10	ADC5/DCD1#/GPI5	K4	VSTBY	N7	GINT/CTS0#/GPD5
C1	SMDAT2/PECIRQT#/GPF7	F12	ADC6/DSR1#/GPI6	K5	VCORE	N8	RTS1#/GPE5
C2	GPC4	F13	ADC4/GPI4	K6	SMCLK5/PWM4/GPA4	N9	KSO2/PD2
C12	DAC5/RIG0#/GPJ5	G1	GPJ7	K7	PWM7/RIG1#/GPA7	N10	KSO6/PD6
C13	DAC3/TACH1B/GPJ3	G2	ALERT#/SERIRQ/GPM6	K8	KSO4/PD4	N11	KSO8/ACK#
D1	FDIO3/DSR0#/GPG6	G4	VSS	K9	KSO9/BUSY	N12	KSO10/PE
D2	CTX0/TMA0/GPB2	G5	VSS	K10	VSTBY	N13	KSO11/ERR#

.

5. Pin Descriptions

5.1 Pin Descriptions

Table 5-1. Pin Descriptions of 3.3V/1.8V LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V/1.8V CMOS I/F) (Supplied by VCC)			
13	**LPCCLK**	PI	***LPC Clock*** 19.2MHz to 33MHz clock for LPC domain functions.
7-10	**LAD[3:0]**	PIO	***LPC Address Data***
6	**LFRAME#**	PI	***LPC LFRAME# Signal***
5	**SERIRQ**	PIO	***SERIRQ Signal*** This pin is supplied by VFSPI or VCC. VFSPI must be supplied as well if VCC is supplied.

Table 5-2. Pin Descriptions of eSPI Bus Interface

Pin(s) No.	Signal	Attribute	Description
eSPI Bus Interface (1.8V CMOS I/F) (Supplied by VCC)			
13	**ESCK**	IK	***eSPI Clock*** 20MHz to 66MHz for eSPI domain functions.
7-10	**EIO[3:0]**	EIO	***eSPI Bi-directional Data***
6	**ECS#**	IK	***eSPI Chip Select***
5	**ALERT#**	EIO	***Alert***

Table 5-3. Pin Descriptions of eSPI Bus Interface

Pin(s) No.	Signal	Attribute	Description
eSPI Bus Interface (1.8V CMOS I/F)			
22	**ERST#**	IK	***eSPI Reset*** Note this pin takes effect after setting 'Input Voltage Selection' to 1.8V.

Table 5-4. Pin Descriptions of LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V CMOS I/F)			
22	**LPCRST#**	IK	***LPC Hardware Reset*** LPC hardware reset will reset LPC interface and host side modules. The source is determined by EC side register bit LPCRSTEN. This pin can be omitted if external LPC reset is not required.
17	**LPCPD#**	IO2	***LPC LPCPD# Signal***
93	**CLKRUN#**	IO16	***LPC CLKRUN# Signal***
15	**ECSMI#**	O8	***EC SMI# Signal*** This is SMI# signal driven by SWUC module.
23	**ECSCI#**	O8	***EC SCI# Signal*** This is SCI# signal driven by PMC module.
126	**GA20**	IO2	***Gate A20 Signal*** This is GA20 signal driven by SWUC module.
4	**KBRST#**	IO2	***KB Reset Signal*** This is KBRST# signal driven by SWUC module.
14	**WRST#**	IK	***Warm Reset*** For EC domain function, reset after power up.
16	**PWUREQ#**	O16	***System Power On Request*** This is PWUREQ# signal driven by SWUC module.
19	**L80HLAT**	O16	***LPC I/O Port 80, High-nibble LAD Latch*** An active high signal to latch Port 80 high-nibble for the debug purpose.
20	**L80LLAT**	O16	***LPC I/O Port 80, Low-nibble LAD Latch*** An active high signal to latch Port 80 low-nibble for the debug purpose.

Table 5-5. Pin Descriptions of 3.3V/1.8V External Serial Flash Interface (FSPI)

Pin(s) No.	Signal	Attribute	Description
External Serial Flash Interface (3.3V/1.8V CMOS I/F) (Supplied by VFSPI)			
105	**FSCK**	O4	***Serial Flash Clock*** Clock (frequency = FreqPLL) to external serial flash. (FreqPLL is listed in Table 10-2 on page 530)
101	**FSCE#**	O4	***Serial Flash Chip Enable*** Connected to CE# of serial flash.
102	**FMOSI**	IOK4	***Serial Flash In*** Connected to SI of serial flash.
103	**FMISO**	IOK4	***Serial Flash Out*** Connected to SO of serial flash.
122	**FDIO2**	IOK8	***Serial Flash In/Out 2*** Connected to IO2 of serial flash.
119	**FDIO3**	IOK8	***Serial Flash In/Out 3*** Connected to IO3 of serial flash.

Note: Please do not place any pull-up resistor on these FSPI pins to reduce power consumption.

Table 5-6. Pin Descriptions of Serial Peripheral Interface (SSPI)

Pin(s) No.	Signal	Attribute	Description
Serial Peripheral Interface (3.3V CMOS I/F)			
32	**SSCK**	O8	***SSPI Clock*** Clock to external device.
125,100	**SSCE1#,** **SSCE0#**	O8, O4	***SSPI Chip Enable*** Connected to SSCE# of SPI device.
57	**SMISO**	IOK8	***SSPI Master In/Slave Out*** Connected to SO of 4-wire SPI device, or connected to SIO of 3-wire SPI device.
56	**SMOSI**	O8	***SSPI Master Out/Slave In*** Connected to SI of 4-wire SPI device.
122	**SBUSY**	IOK16	***SSPI Busy In*** Connected to BUSY of SPI device

Table 5-7. Pin Descriptions of Keyboard Matrix Scan Interface

Pin(s) No.	Signal	Attribute	Description
KB Matrix Interface (3.3V CMOS I/F)			
57-51, 46-36	**KSO[17:0]**	O8	***Keyboard Scan Output*** Keyboard matrix scan output.
65-58	**KSI[7:0]**	IK	***Keyboard*** Scan Input Keyboard matrix scan input for switch based keyboard.

Table 5-8. Pin Descriptions of SMBus Interface

Pin(s) No.	Signal	Attribute	Description
SMBus Interface (3.3V CMOS I/F)			
110, 115, 117, 16, 94, 19, 30	**SMCLK0,** **SMCLK1,** **SMCLK2,** **SMCLK2ALT** **SMCLK3,** **SMCLK4,** **SMCLK5,**	IOK4, IOK4, IOK4, IOK16, IOK16, IOK16, IOK8	***SMBus CLK*** 6 SMBus interface provided.
111, 116, 118, 95 20, 31	**SMDAT0,** **SMDAT1,** **SMDAT2,** **SMDAT3,** **SMDAT4,** **SMDAT5**	IOK4, IOK4, IOK4, IOK16, IOK16, IOK8	***SMBus Data*** 6 SMBus interface provided.

Table 5-9. Pin Descriptions of PS/2 Interface

Pin(s) No.	Signal	Attribute	Description
PS/2 Interface (3.3V CMOS I/F)			
89, 87, 85	**PS2CLK[2:0]**	IOK8	***PS/2 CLK*** 3 sets of PS/2 interface, alternate function of GPIO. PS2CLK0 - 2 correspond to channel 1 - 3 respectively.
90, 88, 86	**PS2DAT[2:0]**	IOK8	***PS/2 Data*** 3 sets of PS/2 interface, alternate function of GPIO. PS2DAT0 - 2 correspond to channel 1 - 3 respectively.

Table 5-10. Pin Descriptions of PWM Interface

Signal	Pin(s) No.	Attribute	Description
PWM Interface (3.3V CMOS I/F)			
34, 32-28, 25-24	**PWM[7:4], PWM[3:0]**	O8, O16	***Pulse Width Modulation Output*** These are general-purpose PWM signals. PWM0-7 correspond to channel 0-7 respectively.
76, 77, 48, 79, 47, 78	**TACH2A** **TACH2B** **TACH1A** **TACH1B** **TACH0A** **TACH0B**	IK	***Tachometer Input*** These are tachometer inputs from external fans. They are used for measuring the external fan speed.

Table 5-11. Pin Descriptions of TMR Interface

Pin(s) No.	Signal	Attribute	Description
TMR Interface (3.3V CMOS I/F)			
123, 48, 85, 86	**TMA0** **TMA1** **TMB0** **TMB1**	O8, O2, O8, O8	***TMR Output***

Table 5-12. Pin Descriptions of Wake-Up Control Interface

Pin(s) No.	Signal	Attribute	Description
Wake-Up Control Interface (3.3V CMOS I/F)			
Refer to Pins List Table 7-9. GPIO Alternate Function	**WUI[86:79]** **WUI[74:32]** **WUI[31:16]** **WUI[7:0]**	IK	***EC Wake-Up Input*** Supplied by VSTBY, used for EC wake-up.
110	**PWRSW**	IK	***Power Switch Input*** Supplied by VSTBY, used to indicate the status of power switch.
112	**RING#**	IK	***Telephone Line Ring Input*** Supplied by VSTBY, used for system wake-up.
21,18	**RI[2:1]#**	IK	***Ring Indicator Input*** Supplied by VSTBY, used for system wake-up.

Table 5-13. Pin Descriptions of Serial Port Interface

Pin(s) No.	Signal	Attribute	Description
Serial Port Interface (3.3V CMOS I/F)			
94,108	**SIN[1:0]**	IOK16	***Serial Data Input*** This input receives serial data from the communications link.

Pin(s) No.	Signal	Attribute	Description
95,109	**SOUT[1:0]**	IOK16	***Serial Data Output*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
72,119	**DSR[1:0]#**	AI / IK	***Data Set Ready*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
35,88	**RTS[1:0]#**	O2 / O8	***Request to Send*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
122,87	**DTR[1:0]#**	O16 / O8	***Data Terminal Ready*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.
73,33	**CTS[1:0]#**	AI / IK	***Clear to Send*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
34,81	**RIG[1:0]#**	IK	***Ring Indicator*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
71,80	**DCD[1:0]#**	AI / IK	***Data Carrier Detect*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-14. Pin Descriptions of Debug UART Interface

Pin(s) No.	Signal	Attribute	Description
Debug UART Interface (3.3V CMOS I/F)			
109	**TXD**	O	***UART TX Output*** UART TX Output
108	**RXD**	IK	***UART RX Input*** UART RX Input

Table 5-15. Pin Descriptions of CIR Interface

Pin(s) No.	Signal	Attribute	Description
CIR Interface (3.3V CMOS I/F)			
123 95	**CTX0** **CTX1**	IOK8, IOK16	***CIR TX Output*** Transmission data for CIR interface.
113 94	**CRX0** **CRX1**	IOK2, IOK16	***CIR RX Input*** Receive data for CIR interface.

Note: There are two channels on interface muxed with GPIO. The alternative function of CTX0/CRX0 and CTX1/CRX1 cannot be enabled at the same time.

Table 5-16. Pin Descriptions of External GPIO Bus (EGPC) Interface

Pin(s) No.	Signal	Attribute	Description
External GPIO Bus (EGPC) Interface (3.3V CMOS I/F)			
82	**EGAD**	IO8	***Address/Data*** The signal is used for the address or data of ITE specify Bus. Connected to IT8301/IT8302 GPIO_DATA pin.

Pin(s) No.	Signal	Attribute	Description
83	**EGCS#**	O8	***Address Chip Select*** The signal is used to identify the chip-select signal. Connected to IT8301/IT8302 CYCLE_START pin.
84	**EGCLK**	O16	***Clock*** The clock frequency is EC clock frequency (listed in Table 10-2 on page 530). The signal only is running when the cycle is active. Connected to IT8301/IT8302 GPIO_CLK pin.

Table 5-17. Pin Descriptions of Platform Environment Control Interface (PECI)

Pin(s) No.	Signal	Attribute	Description
Platform Environment Control Interface Interface (3.3V CMOS I/F)			
117	**PECI**	PECI	***PECI*** This bi-directional pin provides data communication between the PECI host and devices.
118	**PECIRQT#**	O4	***PECI Request*** The PECI request is output to PECI devices. When this pin goes low, it requests the system to make the PECI bus available.

Table 5-18. Pin Descriptions of Hardware Bypass (HWBP)

Pin(s) No.	Signal	Attribute	Description
Hardware Bypass Interface (3.3V CMOS I/F)			
19	**BAO**	O16	***Buffer A Output*** Hardware bypass path from GPI6 to BAO.
16	**BBO**	O16	***Buffer B Output*** Hardware bypass path from GPI7 to BBO.

Table 5-19. Pin Descriptions of Parallel Port Interface

Pin(s) No.	Signal	Attribute	Description
Parallel Port Interface (3.3V CMOS I/F)			
52	**SLCT**	O8	***Printer Select***
46	**PE**	O8	***Printer Paper End***
45	**BUSY**	O8	***Printer Busy***
44	**ACK#**	O8	***Printer Acknowledge***
61	**SLIN#**	IK	***Printer Select Input***
60	**INIT#**	IK	***Printer Initialize***
51	**ERR#**	O8	***Printer Error***
59	**AFD#**	IK	***Printer Auto Line Feed***
58	**STB#**	IK	***Printer Strobe***
43-36	**PD[7:0]**	O8	***Parallel Port Data[7:0]***

*: The interface can be connected to parallel port of computer through ITE-specified cable. The programmer can directly read/write flash through this interface.

Table 5-20. Pin Descriptions of GPIO Interface

Pin(s) No.	Signal	Attribute	Description
GPIO Interface (3.3V CMOS I/F)			
Refer to Pins List Table 7-9. GPIO Alternate Function	**GPA[7:0], GPB[7:0], GPC[7:0], GPD[7:0], GPE[7:0], GPF[7:0], GPG[6,2:0], GPH[7:0], GPI[7:0], GPJ[7:0], GPM[6:0]**	IOK	***GPIO Signals*** The GPIO pins are divided into groups. Some GPIO pins have alternative function. **PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG6 (Reserved hardware strapping)**. GPG2 is pulled up if FSPI I/F is used, and pulled down if otherwise.
33	**GINT**	IK	***General Purpose Interrupt*** General Purpose Interrupt directly input to INT28 of INTC.

Table 5-21. Pin Descriptions of Hardware Strap

Pin(s) No.	Signal	Attribute	Description
Hardware Strap (3.3V CMOS I/F)			
122, 99-93	**ID[7:0]**	IK	***Identify Input*** These hardware straps are used to identify the version for firmware usage. These input signals will be latched when the VSTBY power up. Note that these hardware straps are only available if these pins are not driven by other components on PCB. Disabled if no pull-up or pull-down resistor.
63, 62, 60, 59	**KSI[5,4,2,1]**	IK	The value of 0011b is the entry of DBGR/EPP.
105, 119, 103, 102, 101, 100	**FSCK, GPG6, FMISO, FMOSI, FSCE#, GPG2**	IK	These pins are the entry of the test mode.
125	**GPG0**	IK	***Voltage Comparator Enable*** This hardware strap is enabled if there is an external pull-up resistor, while disabled if pull-down resistor. Note: Only for voltage comparator 0

*: The strapped pin will be strapped 1b if it is pulled up. The strapped pin will be strapped 0b if it is pulled down or not pulled. The strapped pin will be strapped an unknown value if it is driven.

Table 5-22. Pin Descriptions of ADC Input Interface

Pin(s) No.	Signal	Attribute	Description
ADC Interface (3.3V CMOS I/F)			
73-66	**ADC[7:0]**	AI	***ADC Input/Alternate GPIO*** These 8 ADC inputs can be used as GPIO ports depending on the ADC channels required.

Table 5-23. Pin Descriptions of DAC Output Interface

Pin(s) No.	Signal	Attribute	Description
DAC Interface (3.3V CMOS I/F)			
81-78	**DAC[5:2]**	AO	***DAC Output***

Table 5-24. Pin Descriptions of CEC Interface

Pin(s) No.	Signal	Attribute	Description
CEC Interface (3.3V CMOS I/F)			
85	**CEC**	IOK8	***CEC*** This bi-directional pin provides data communication between the CEC host and devices.

Table 5-25. Pin Descriptions of Clock

Pin(s) No.	Signal	Attribute	Description
Clock Interface (3.3V CMOS I/F)			
112	**CK32KOUT**	O16	**32.768 kHz Oscillator Output** 32.768 kHz clock output.

Table 5-26. Pin Descriptions of Power/Ground Signals

Pin(s) No.	Signal	Attribute	Description
Power Ground Signals			
1, 27, 49, 91,104	**VSS**	I	***Ground*** Digital ground.
11	**VCC**	I	***System Power Supply of 3.3V/1.8V*** The power supply of LPC and related functions, which is the main power of system.
26, 50, 92, 114, 121, 127	**VSTBY**	I	***Standby Power Supply of 3.3V*** The power supply of EC domain functions, which is standby power of system.
106	**VFSPI**	I	***Standby Power Supply of 3.3V/1.8V*** This pin supplies the I/O power of FSCK, FSCE#, FMOSI, FMISO, FDIO2, FDIO3 and SERIRQ. If the external SPI flash is used, the power level of the flash must be the same as that of the VFSPI pin. The power pin must be supplied as well if VCC is supplied. It's allowed to let {VSTBY,VFSPI}={on,off} and the FSPI I/F must be disabled by the setting in 16B-signature if the EC power-on configuration is {VSTBY,VFSPI}={on,off},.
12	**VCORE**	I/O	***Core Power Bypass*** Internal core power output. External capacitor is required to be connected between this pin and VSS and physically close to this pin. The capacitor type must be low-ESR and MLCC is required.
75	**AVSS**	I	***Analog Ground for Analog Component***
74	**AVCC**	I	***Analog VCC for Analog Component***

Notes: I/O cell types are described below:

I: Input PAD.
AI: Analog Input PAD.
IK: Schmitt Trigger Input PAD.
IKD: Schmitt Trigger Input PAD (integrated one pull-down resistor).
PI: PCI Bus Specified Input PAD.
PIO: PCI Bus Specified Input/Output PAD.
EIO: eSPI Bus Specified Input/Output PAD.
OSCI: Oscillator Input PAD.
AO: Analog Output PAD.
O2: 2 mA Output PAD.
O4: 4 mA Output PAD.
O6: 6 mA Output PAD.
O8: 8 mA Output PAD.
AIO2: 2 mA Bidirectional PAD with Analog Input PAD.
IOK2: 2 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK4: 4 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK6: 6 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK8: 8 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK16: 16 mA Bidirectional PAD with Schmitt Trigger Input PAD.
PECI: Special design for PECI interface.
All input pins aren't 5V tolerant, except those with the "5VT" field checked in Table 7-9 on page 263.

5.2 Chip Power Planes and Power States

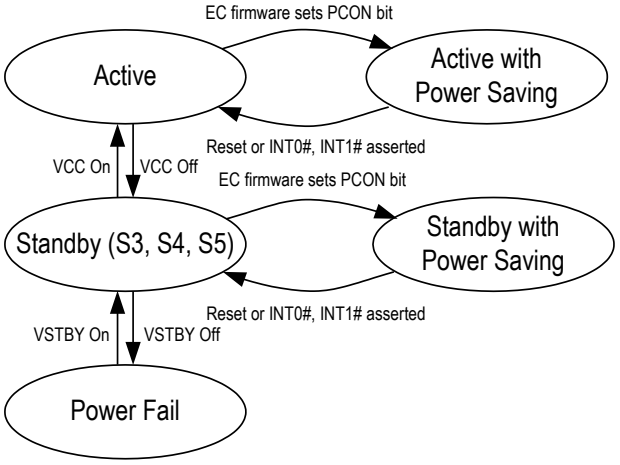
Table 5-27. Power States

Power State	VCC pin	VSTBY/AVCC pin
Active	Supplied	Supplied
Active with Power Saving	Supplied	Supplied EC is in Doze or Sleep Mode
Standby	Not Supplied	Supplied
Standby with Power Saving	Not Supplied	Supplied EC is in Doze or Sleep Mode
Power Fail	Not Supplied	Not Supplied

Note:

(1) The AVCC should be derived from VSTBY.
(2) All other combinations of VCC / VSTBY are invalid.
(3) In Power Saving mode, CPU program counter is stopped and no instruction will be executed no matter whether EC Clock is running or not.

Figure 5-1. Power State Transitions



5.3 Pin Power Planes and States

In the following tables of this section, Standby means that the VCC is not valid but VSTBY is supplied (S3, S4 or S5) and EC is in normal operation. Standby with Sleep means that CPU and most of its functions are out of work due to PLL power-down while VSTBY is still supplied.

The abbreviations used in the following tables are described below:
H means EC drives high or driven high.
L means EC drives low or driven to low or output pin power off.
Z means EC tri-states the I/O pin or output pin with enable.
RUN means that Output or I/O pins are in normal operation.
Driven means that the input pin is driven by connected chip or logic.
STOP means that the output pin keeps its logical level before the clock is stopped.
OFF means I/O pin power off.

Note that reset sources of 'Reset Finish' columns depend on Reset Types and Applied Module Table and it means the reset is finished when its corresponding power plane is supplied.
Note that GPIO pins listed in different functional tables except GPIO table indicate their pin status of the corresponding alternative function.

Table 5-28. Pin States of LPC Bus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
LPCRST# (Y)	VSTBY	Driven	L	L	L
LPCCLK	VCC	Driven	L	L	L
LAD[3:0]	VCC	RUN	OFF	OFF	OFF
LFRAME#	VCC	Driven	L	L	L
SERIRQ	VCC	Z	OFF	OFF	OFF
LPCPD# (Y)	VSTBY	Table 7-9	L	L	L
CLKRUN# (Y)	VSTBY	Table 7-9	OFF	L	OFF
ECSMI#	VSTBY	Table 7-9	RUN	Z	OFF
ECSCI# (Y)	VSTBY	Table 7-9	RUN	Z	OFF
GA20 (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
KBRST# (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
WRST#	VSTBY	Driven	Driven	Driven	L
PWUREQ#	VSTBY	Table 7-9	RUN	STOP	OFF
L80HLAT (Y)	VSTBY	Table 7-9	L	L	OFF
L80LLAT (Y)	VSTBY	Table 7-9	L	L	OFF

Table 5-29. Pin States of Keyboard Matrix Scan Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
KSO	VSTBY	L	RUN	STOP	OFF
KSI	VSTBY	Driven	Driven	Driven	L

Table 5-30. Pin States of SMBus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SMCLK (Y)	VSTBY	Table 7-9	RUN	Z	OFF
SMDAT (Y)	VSTBY	Table 7-9	RUN	Z	OFF

Table 5-31. Pin States of PS/2 Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PS2CLK (Y)	VSTBY	Table 7-9	RUN	Z	OFF
PS2DAT (Y)	VSTBY	Table 7-9	RUN	Z	OFF

Table 5-32. Pin States of PWM Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PWM (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
TACH (Y)	VSTBY	Table 7-9	Driven	Driven	OFF

Table 5-33. Pin States of Wake-Up Control Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
WUI (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
PWRSW (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
RI (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
RING# (Y)	VSTBY	Table 7-9	Driven	Driven	OFF

Table 5-34. Pin States of UART Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
RXD (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
TXD (Y)	VSTBY	Table 7-9	RUN	STOP	OFF

Table 5-35. Pin States of CIR Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
CRX0/CRX1 (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
CTX0/CTX1 (Y)	VSTBY	Table 7-9	RUN	STOP	OFF

Table 5-36. Pin States of EGPC Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
EGAD (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
EGCS# (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
EGCLK (Y)	VSTBY	Table 7-9	RUN	STOP	OFF

Table 5-37. Pin States of SSPI Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SSCE# (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
SSCK (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
SMOSI (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
SMISO (Y)	VSTBY	Table 7-9	Driven	Driven	OFF

Table 5-38. Pin States of Serial Port Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SIN (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
SOUT (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
CTS # (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
DSR # (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
DCD # (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
RIG # (Y)	VSTBY	Table 7-9	Driven	Driven	OFF
DTR # (Y)	VSTBY	Table 7-9	RUN	STOP	OFF
RTS # (Y)	VSTBY	Table 7-9	RUN	STOP	OFF

Table 5-39. Pin States of GPIO Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
GPA0…	VSTBY	Table 7-9	Depends on its mode	STOP	OFF

Table 5-40. Pin States of ADC Input Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
ADC (Y)	AVCC	Driven	Driven	Driven	L

Table 5-41. Pin States of DAC Output Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
DAC (Y)	AVCC	Table 7-9	RUN	RUN	OFF

5.4 Reset Sources and Types

Table 5-42. Reset Sources

Reset Sources	Description
VSTBY Power-Up Reset	Activated after VSTBY is power up and PLL is stable It takes t_{PLLS} for PLL stabling, and the external flash has to be ready before VSTBY Power-Up Reset finish
VCC Power-Up Reset	Activated after VCC is power up
Warm Reset	Activated if WRST# is asserted
LPC Hardware Reset	Activated if LPCRST# is asserted
Super I/O Software Reset	Activated if SIOSWRST of PNPCFG is writing 1
Watch Dog Reset	Activated if CPU WDT or External WDT time-out

Table 5-43. Reset Types and Applied Module

Reset Types	Sources	Applied Module
Host Domain Hardware Reset	Warm Reset, VCC Power-Up Reset or LPC Hardware Reset LPC Hardware Reset may be unused See also LPCRSTEN in GCR register.	LPC, PNPCFG, Logical Devices and EC2I
Host Domain Software Reset	Super I/O Software Reset	PNPCFG, Logical Devices and EC2I
EC Domain Reset	Warm Reset, VSTBY Power-Up Reset or Watch Dog Reset	EC Domain

The WRST# should be driven low for at least t_{WRSTW} before going high (Refer to Table 10-3. Warm Reset AC Table on page 530)

.

If the firmware wants to assert an EC Domain Reset, start an internal of external watchdog without clearing its counter or write invalid data to EWDKEYR register (refer to EWDKEYEN and EWDKEYR registers).
If the firmware wants to determine the source of the last EC Domain Reset, use LRS field in RSTS register.

5.4.1 Related Interrupts to INTC

- Interrupt to INTC
  LPCRST# may come from pin ERST#/LPCRST#/GPD2 or RING#/CK32KOUT/LPCRST#/GPB7. Both pins have another interrupt related alternative function. LPCRST# can be treated as an orthogonal input and LPCRST# event can be handled in the same interrupt routine of another alternative function.

5.5 Chip Power Mode and Clock Domain

Table 5-44. Clock Types

Types	Description
32.768 k Clock	32.768 kHz generated by internal clock generator.
PLL Clock	Clock (frequency = FreqPLL) generated by internal PLL which feds 32.768 k PLL Clock is also the base clock of flash interface. (FreqPLL is listed in Table 10-2 on page 530
EC Clock	It's from internal PLL and its frequency is listed in Table 10-2 on page 530
CPU Clock	The clock of WDT is from EC clock. Core clock: The frequency is FreqPLL. (FreqPLL is listed in Table 10-2 on page 530)
Host LPC Clock	19.2MHz to 33MHz from LPCCLK pin and applied on Host Domain.

The CPU can enter Doze/Deep Doze/Sleep mode to reduce some power consumption. After entering Doze/Deep Doze/Sleep mode, clock of CPU is stopped but the external timer still works. Also see Table 5-46 on page 29 for the details.

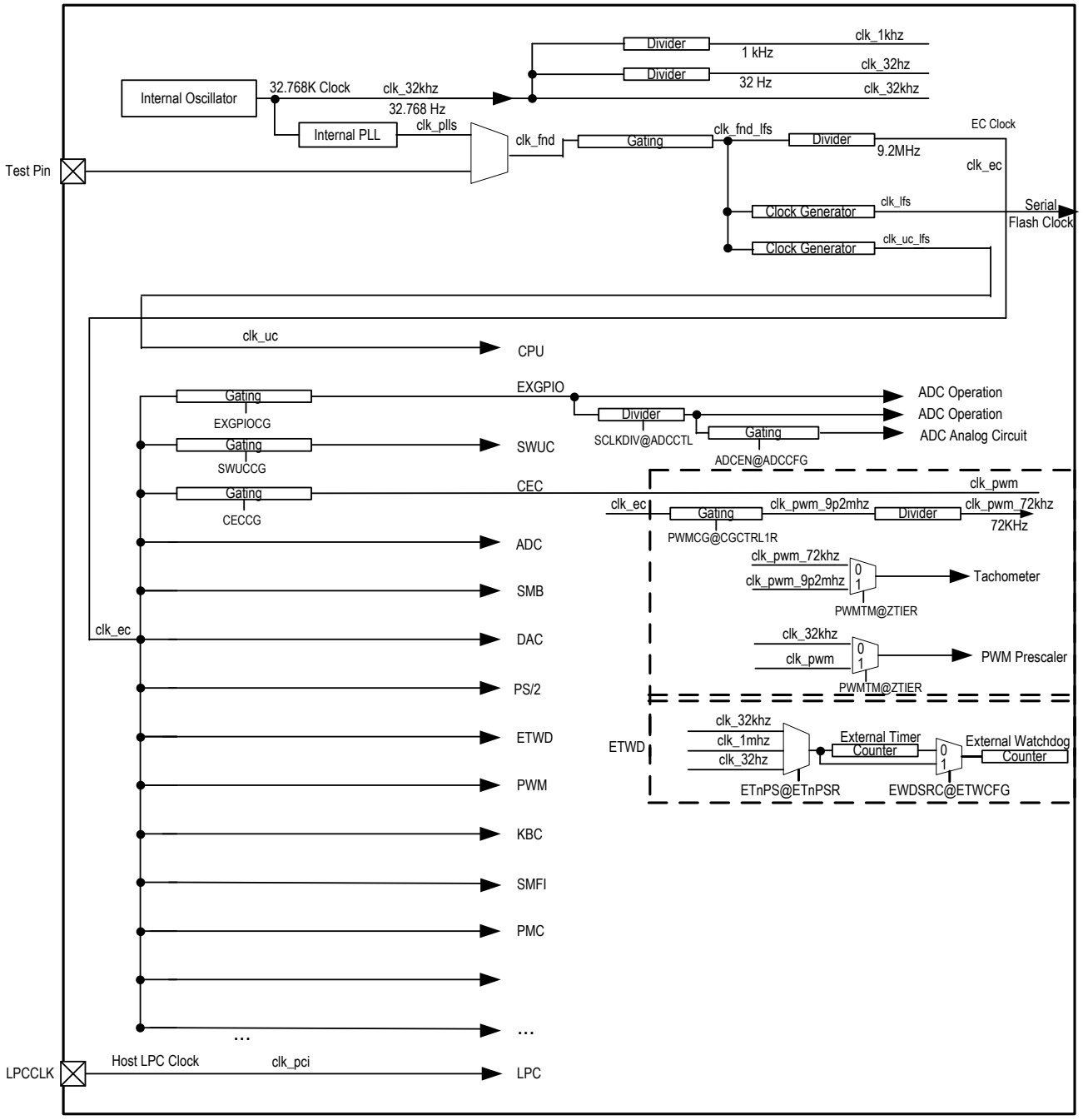
The way to wake up CPU from Doze/Deep Doze/Sleep mode is to enable external interrupts or hardware reset. Firmware may set PLLCTRL bit before setting PD bit to enter the Sleep mode, since stopping PLL can reduce more power consumption, but it takes more time to wake up from Sleep mode due to waiting for PLL being stable. The steps to enter and exit Doze/Deep Doze/Sleep are listed below:

(a) Set related bits of IE register if they are cleared.
(b) Set channels of WUC which wants to wake up CPU and disable unwanted channels.
(c) Set channels of INTC which wants to wake up CPU and disable unwanted channels.
(d) Set PLLCTRL bit for Sleep mode, or clear it for Doze mode.
(e) Execute STANDBY instruction to enter the Doze/Deep Doze/Sleep mode.
(f) CPU waits for an interrupt to wake up.
(g) After an interrupt is asserted, CPU executes the corresponding interrupt routine and returns the next instruction after excuting STANDBY instruction.

The following figure describes the drivers and branches of the three clocks.
In this figure, clk_32kHz represents 32.768 k Clock; clk_fnd and its branches represent EC Clock; clk_pci represents LPC Clock.

IT5121 has a built-in clock generator, which can generates 32.768kHz clock without an external crystal oscillator. This feature is called "Crytal-Free".

Figure 5-2. Clock Tree



FreqPLL/FreqEC are listed in Table 10-2 on page 530.

Table 5-45. Power Saving by EC Clock Operation Mode

Mode	Item	Description
Normal	Enter	VSTBY is supplied and hardware reset done
	Exit	Enter other modes
	32.768 k Clock	On
	PLL	On
	EC Domain Clock	Driven by PLL
	CPU Clock	The same as EC Domain Clock
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Doze	Enter	Execute STANDBY instruction
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	On, clearing PLLCTRL of ECPM module is required
	EC Domain Clock	Driven by PLL
	CPU Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Deep Doze	Enter	Execute STANDBY instruction
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	D2EC disabled: On but gated D2EC enabled: On
	EC Domain Clock	Off
	CPU Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Sleep	Enter	Execute STANDBY instruction
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	D2EC disabled: Off, setting PLLCTRL of ECPM module is required D2EC enabled: On
	EC Domain Clock	Driven by PLL
	CPU Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)

Table 5-46. Module Status in Each Power State/Clock Operation

Power State and/or Clock Operation	Running Module	Stopped Module	Off Module	Note
Active *Active with Power Saving*	LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC / BRAM/RTCT			List host related modules only
Standby *Standby with Power Saving*			LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC	List host related modules only
Active with Doze Mode *Standby with Doze Mode*	All other EC modules	CPU		List EC modules only
Active with Deep Doze/Sleep Mode *Standby with Deep Doze/Sleep Mode*	GPIO, WUC and its sources, INTC and its sources from running modules, SWUC wakeup logic, PWM channel outputs, KBS, ETWD, BRAM	All other EC modules		List all
Power Fail			All others	List all

Note: Running module means this module works well.
Stopped module means this module is frozen because its clock is stopped.
Off module means this module is turned off due to power lost.

5.6 Pins with Pull, Schmitt-Trigger or Open-Drain Function

Table 5-47. Pins with Pull Function

Pin	Pull Function	Note
KSI[7:0]	Programmable 75k pull-up resistor	Default off
KSO[17:0]	Programmable 75k pull-up resistor	Default off
GPIO with pull capability and their alternative functions	Programmable 75k pull-up/down resistor	Detail pull capability refer and default on/off refer to Table 7-9 on page 263
ID7-0	Operational 75k pull-down resister	Default off No pull up or down during VSTBY power on to process the hardware strap function

Note: 75k ohm is typical value. Refer to section 9 DC Characteristics on page 527 for details

Table 5-48. Pins with Schmitt-Trigger Function

Pin	Pull Function	Note
All GPIO pins except GPIO group I/J and their alternative functions	Fixed Schmitt-Trigger Input	
KSI[7:0]	Fixed Schmitt-Trigger Input	
WRST#	Fixed Schmitt-Trigger Input	

Table 5-49. Signals with Open-Drain Function

Signal	Open-Drain Function	Note
CLKRUN#	Open-drain output signal	
KSO	Programmable open-drain output signal	Default is push-pull
PS2CLK, PS2DAT	Open-drain bi-directional signal	
SMCLK, SMDAT	Open-drain bi-directional signal	
ECSCI#, ECSMI#, PWUREQ#	Open-drain output signal	
GPIO with open-drain capability and their alternative functions (Other GPIO pin(s) can support open-drain by setting its(their) GPDR register(s) as 0 and switch GPMD field in GPCR register between input and output mode.)	Programmable open-drain output signal	Default is push-pull

5.7 Pins with 1.8V Input/Output

IT5121 supports 3.3V/1.8V LPC and FSPI interface. It also supports 1.8V input for some GPIOs, suitable for 1.8V open-drain applications like I2C. The setting of these voltage switches are shown below.

Table 5-50. Pins with 1.8V Input/Output

Function	Pin	1.8V		3.3V	
		I/O	Conditions	I/O	Conditions
LPC	LPCCLK, LAD[3:0], LFRAME#	1.8V Input 1.8V Output	VCC=1.8V	3.3V Input 3.3V Output	VCC=3.3V
FSPI SERIRQ	FSCK, FSCE#, FMOSI, FMISO, SERIRQ	1.8V Input 1.8V Output	VFSPI= 1.8V Refer to GCR23	3.3V Input 3.3V Output	VFSPI= 3.3V Refer to GCR23
SMB	SMCLK[5:0], SMDAT[5:0]	1.8V Open-drain Internal pull-up must be disabled	Refer to GCR19 - GCR22	3.3V Open-drain	Refer to GCR19 - GCR22
GPIO	Refer to Table 7-9. GPIO Alternate Function on page 263.	1.8V Input Only Internal pull-up must be disabled	Refer to GCR19 - GCR22	3.3V Input 3.3V Output	Refer to GCR19 - GCR22

5.8 Power Consumption Consideration

- Each input pin should be driven or pulled

Input floating causes leakage current and should be prevented.
Pins can be pulled by an external pull resistor or internal pull for a pin with programmable pull.

- Each output-drain output pin should be pulled

If an output-drain output pin is not used and is not pulled by an external pull resistor or internal pull for a pin with programmable pull, make it drive low by the firmware.

- Each input pin which belongs to VSTBY power plane is connected or pulled up to VCC power plane

Such cases may cause leakage current when VCC is not supplied and a diode may be used to isolate leakage current from VSTBY to VCC. For example, use diodes for KBRST# and GA20 if they are connected to VCC logic of South-Bridge.

- Any pin which belongs to VSTBY power plane should not be pulled to VCC in most cases.

It may cause a leakage current path when VCC is shut down. Refer to the above consideration.

- Program GPIO ports as output mode as soon as possible

Any GPIO port used in output mode should be programmed as soon as possible since this pin may not be driven (be floating) if its default value of pull is off.

- Disable unnecessary pull in power saving mode

Prevent from driving a pin low or letting a pin be driven low but its pull high function is enabled in power saving mode.
Prevent from driving a pin high or letting a pin be driven high but its pull low function is enabled in power saving mode.

- Handle the connector if no cable is plugged into it

The firmware or the hardware should prevent the wire connected to the connector from no driving if no cable is plugged into the connector such as PS/2 mouse and so on.

- Disable unnecessary pull for a programmable pull pin

Pull control may be enabled for an input pin or an open-drain output pin and should be disabled for a push-pull output pin.
Pull control should be disabled if an external pull resistor exists.
External pull resistor can control the pull current precisely since the register value of the internal pull has large tolerance. Refer to section 9 DC Characteristics on page 527 for details.

- Flash standby mode

Make flash enter standby mode to reduce power consumption if it is not used.
It's controlled by AFSTBY bit in FPCFG register.

- Prevent accessing Scratch RAM before entering power-saving mode

There is unnecessary power consumption after Scratch RAM is accessed in data space. Read any other registers of external data memory once to prevent this condition.

- Use Doze mode

Doze mode has huge power consumption reduction due to the CPU clock is gated (stopped) in this mode.

- Use Sleep mode rather than Doze mode

Sleep mode has less power consumption than Doze mode because PLL is power-down and EC clock is stopped in Sleep mode, although most EC modules are not available.
Refer to Table 5-46 on page 29 for the details.

- Gate clock by module in EC domain

All modules in EC domain are not clock gated in default but can be gated by module to get less power consumption.
It's controlled by CGCTRL1R, CGCTRL2R and CGCTRL3R registers.

- Power-down ADC/DAC analog circuit if it is unnecessary.

ADC/DAC analog circuits are power-down in default and should be activated only if necessary.
ADC analog circuit power-down is controlled by ADCEN bit in ADCCFG register.

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6. Host Domain Functions

6.1 The Enhanced Serial Peripheral Interface (eSPI)

6.1.1 Overview

The Enhanced Serial Peripheral Interface (eSPI) is basically a LPC replacement, and it has more benefits such as low voltage level, low power, higher bandwidth, pin-count saving, etc.

The MAFS (Master Attached Flash Sharing) lets the EC runtime code-fetch from the chipset.

Additionally, SAFS (Slave Attached Flash Sharing) is supported. This implies that the physical flash component is attached to the EC, and the eSPI master can access this flash over the eSPI bus by PUT_FLASH_NP and GET_FLASH_C commands.

6.1.2 Features

- Compatible with eSPI specification v1.0
- Supports Peripheral Channel
- Supports OOB Message Channel
- Supports Virtual Wires Channel
- Supports Flash Access Channel, MAFS/SAFS both supported
- Supports eSPI 20MHz to 66MHz

6.1.3 Function Description

It's required to switch the PLL frequency to 32.3MHz or higher.
To read the flash attached to the eSPI master, it can be done by the EC-Indirect Memory cycle or eSPI upstream cycle.
To erase/program the flash attached to the eSPI master, it can be done by the eSPI upstream cycle.

6.1.3.1 Peripheral Channel

EC supports legacy LPC transactions over the Peripheral Channel. Short I/O transactions (PUT_IORD_SHORT and PUT_IOWR_SHORT) are used to access PNPCFG and Logical Devices. The length of short I/O transactions is 1, 2 or 4 bytes, and it is recommended to use the short I/O commands with 1-byte data only. Short Memory transactions (PUT_MEMRD32_SHORT and PUT_MEMWR32_SHORT) or transactions with memory access cycle types (Memory Read 32 and Memory Write 32) are used to access the flash content through SMFI module. Host-Indirect memory cycles based on short I/O transactions can access the flash as well.

- Supports HLPC
- Supports H2RAM
- Supports I2EC
- Supports Host-Indirect memory cycles
- Supports port 80h read via parallel port with the software provided by ITE

The PUT_PC, PUT_NP, GET_PC, PUT_IORD_SHORT, PUT_IOWR_SHORT, PUT_MEMRD32_SHORT and PUT_MEMWR32_SHORT commands are supported.

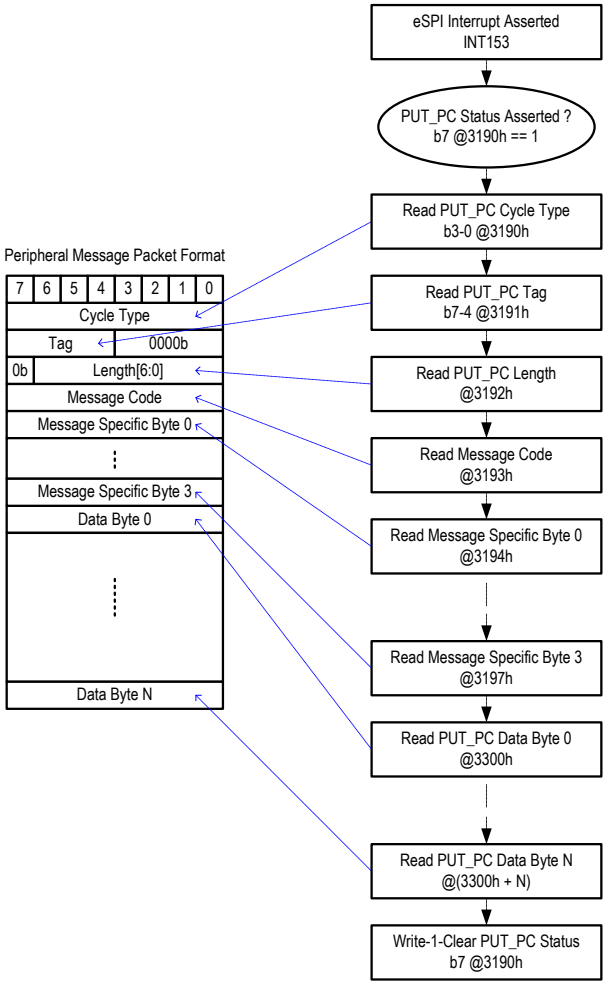
The GET_NP command is reserved and upstream memory access transactions are not supported.

- **Receive A Message through eSPI Peripheral Channel**

After receiving a message transaction initiated by the eSPI master, EC clears its eSPI PC_FREE status (refer to

eSPI specification) to 0, which indicates EC is not free to accept another peripheral posted or completion transaction. The software needs to follow the sequence listed below to release the PC_FREE status.

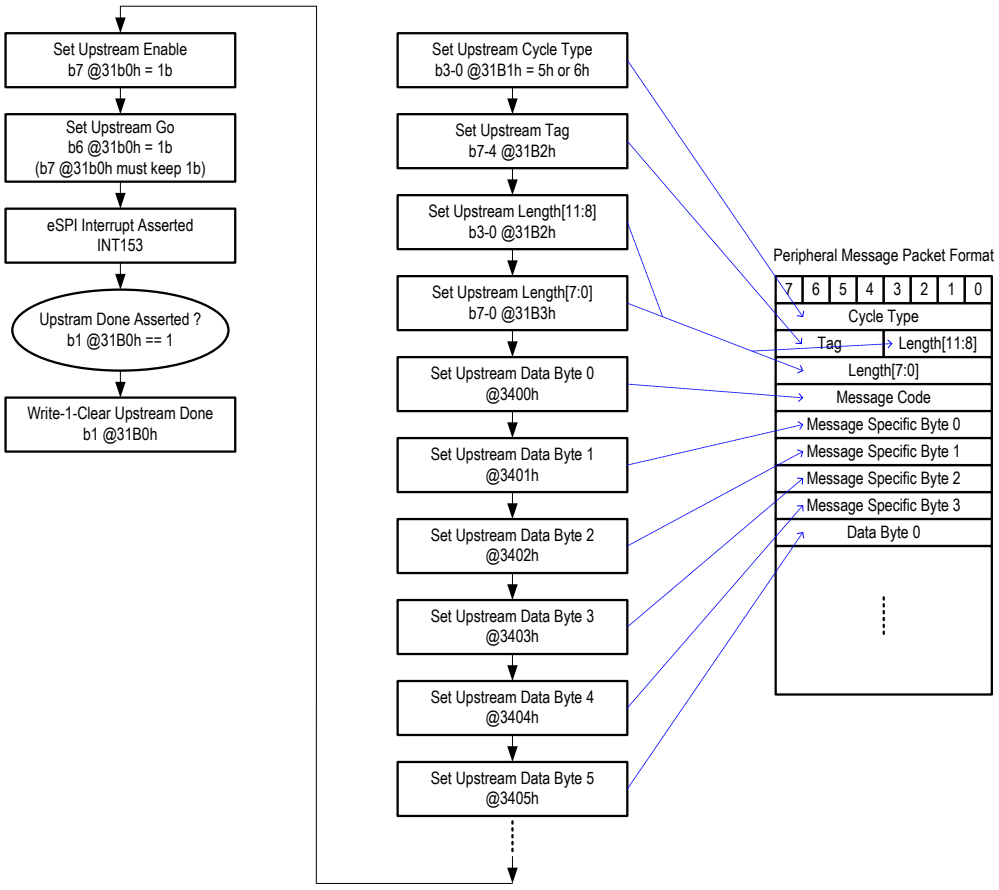
Figure 6-1 Flow of Receiving a Peripheral Message Transcation over eSPI Bus



- **Initiate A Message through eSPI Peripheral Channel**

EC also can initiate a peripheral message transaction over the eSPI bus. The software sequence is listed below.

Figure 6-2 Flow of Initiating a Peripheral Message Transcation over eSPI Bus



6.1.3.2 Flash Access Channel (MAFS)

The flash access channel provides a path allowing the flash components to be shared run-time between chipset and EC. For the master attached to the flash sharing, refers to the scheme where flash components are attached to the eSPI master such as the chipset. EC is allowed to access the shared flash component through the flash access channel.

If MAFS configuration is enabled for a platform, only GET_FLASH_NP and PUT_FLASH_C flash commands, which are required for Master-Attached Flash access, are supported. Under this configuration, the PUT_FLASH_NP and GET_FLASH_C commands are not supported.

- **Code-fetch Switched from Flash to eSPI Flash Sharing**

  - EC power-on (PLL=18.4MHz)
  - Copy flash data to Scratch SRAM
  - The program counter jumps to Scratch ROM
  - Switch PLL=18.4MHz to 32.3MHz or higher
  - Let RSMRST# low-to-high
  - Endless loop to wait for FCEAF@ESGCTRL0 = 1 and Write 1b Clear.
  - Write 1b to FTHS@FLHCTRL5R to make code-fetch from eSPI flash sharing later
  - Endless loop to wait for FTHS@FLHCTRL5R = 1
  - VW SLAVE_BOOT_LOAD_DONE = 1
  - Leave Scratch ROM
  - Fetch through eSPI flash sharing

- **Code-fetch Switched from eSPI Flash Sharing to Flash**

  - Copy flash data to Scratch SRAM
  - The program counter jumps to Scratch ROM
  - Write 0b to FTHS@FLHCTRL5R to make code-fetch from SPI flash later
  - Endless loop to wait for FTHS@FLHCTRL5R = 0
  - Write 0b to FFSPITRI@FLHCTRL3R to re-drive FSPI I/F
  - Switch PLL to 18.4MHz
  - Let RSMRST# high-to-low
  - Leave Scratch ROM
  - Fetch from SPI flash

- **Initiate a Non-Posted Transaction through eSPI Flash Access Channel**

EC also can access the shared flash component through EC bus.

- Maximum read request size: 64 bytes
- Maximum payload size: 64 bytes
- Tag field in Flash Access Request Packet Format must be set 1h
- Flash Read, Flash Write and Flash Erase supported

The software sequence of initiating a Flash Read transaction is listed below.

Figure 6-3 Flow of Initiating a Flash Read Transcation over eSPI Bus

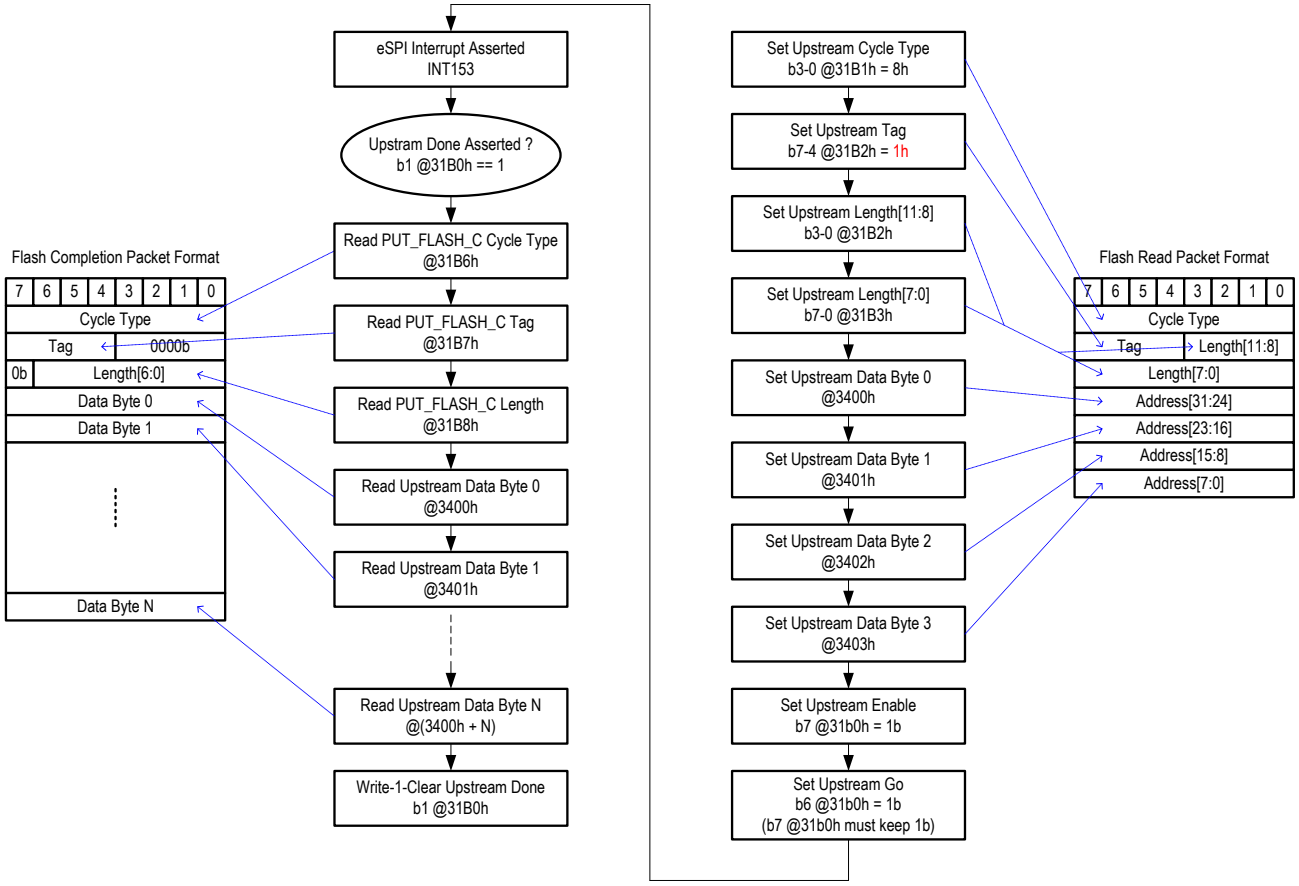
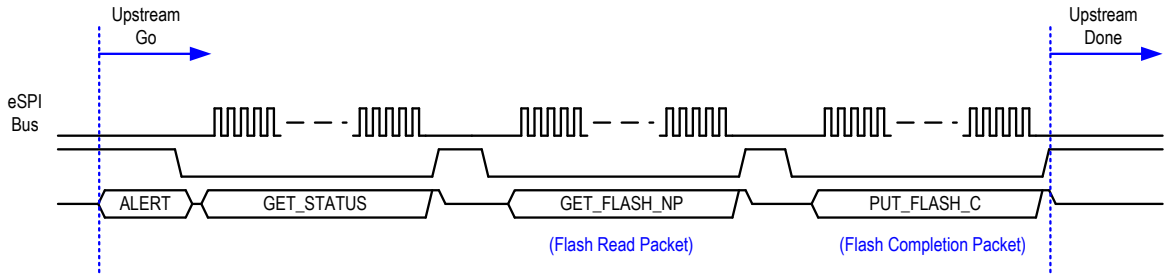
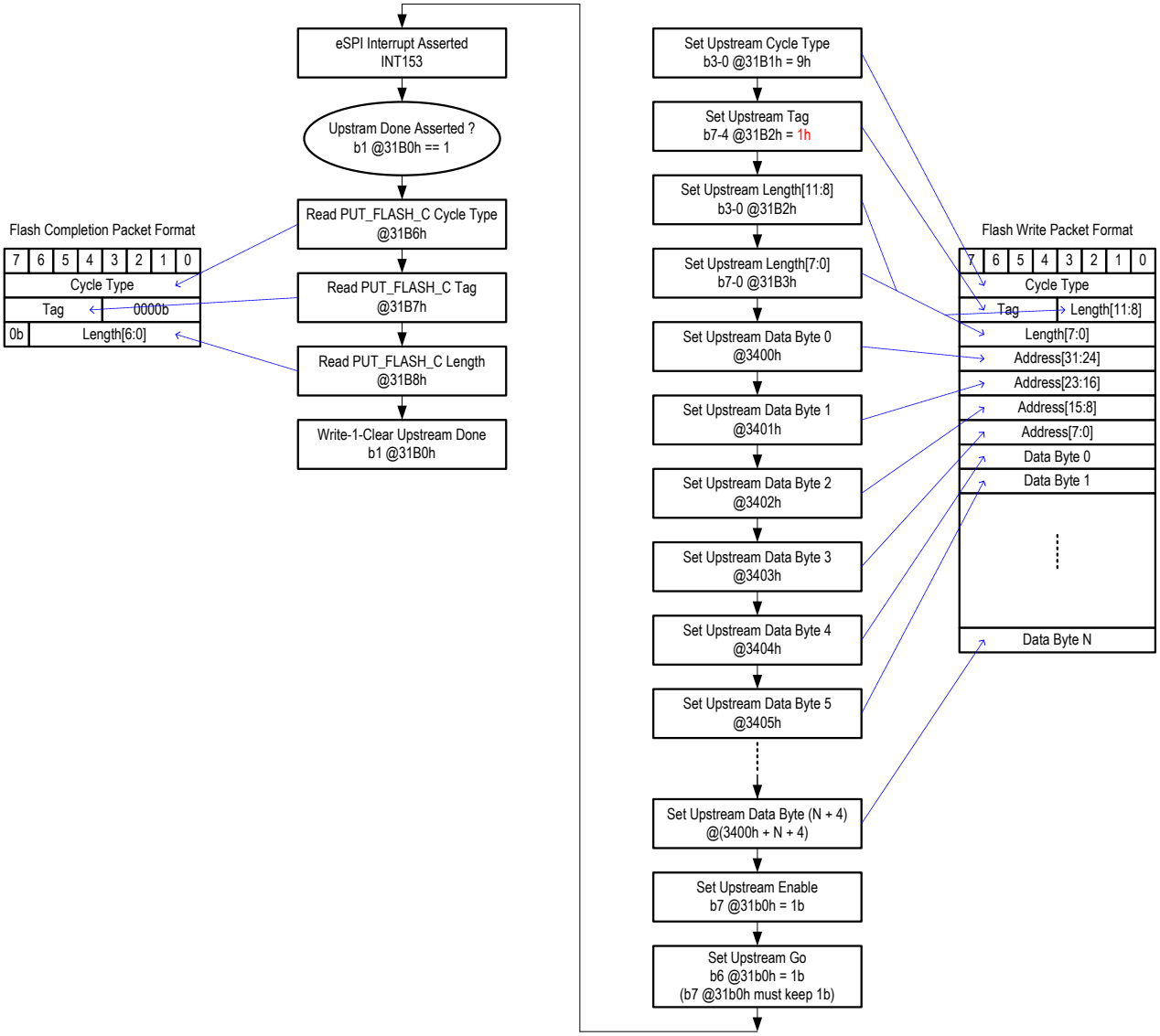


Figure 6-4 Transations of Initiating a Flash Read Transcation over eSPI Bus



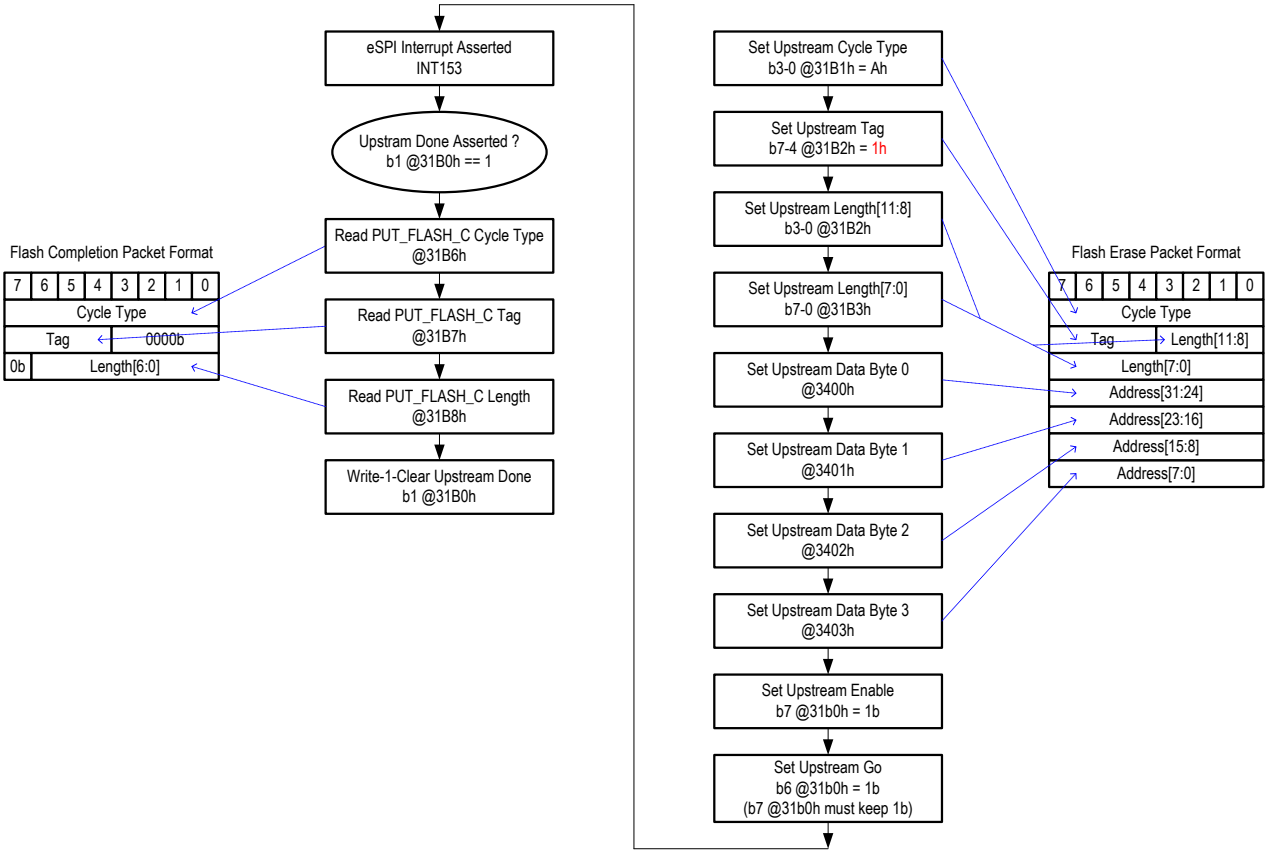
The software sequence of initiating a Flash Write transaction is listed below.

Figure 6-5 Flow of Initiating a Flash Write Transcation over eSPI Bus



The software sequence of initiating a Flash Erase transaction is listed below.

Figure 6-6 Flow of Initiating a Flash Erase Transcation over eSPI Bus



EC uses tag 0 to label the flash access request is initiated for code-fetch and tag 1 for other applications. Different tags allow non-posted requests to be outstanding at any time and there are no requirements for order between each other.

6.1.3.3 Flash Access Channel (SAFS)

If SAFS configuration is enabled for a platform, only PUT_FLASH_NP and GET_FLASH_C flash commands are supported. The eSPI master can access the flash attached to EC over the eSPI bus by PUT_FLASH_NP and GET_FLASH_C flash commands.

- **Receive a Flash Read through eSPI Flash Channel**

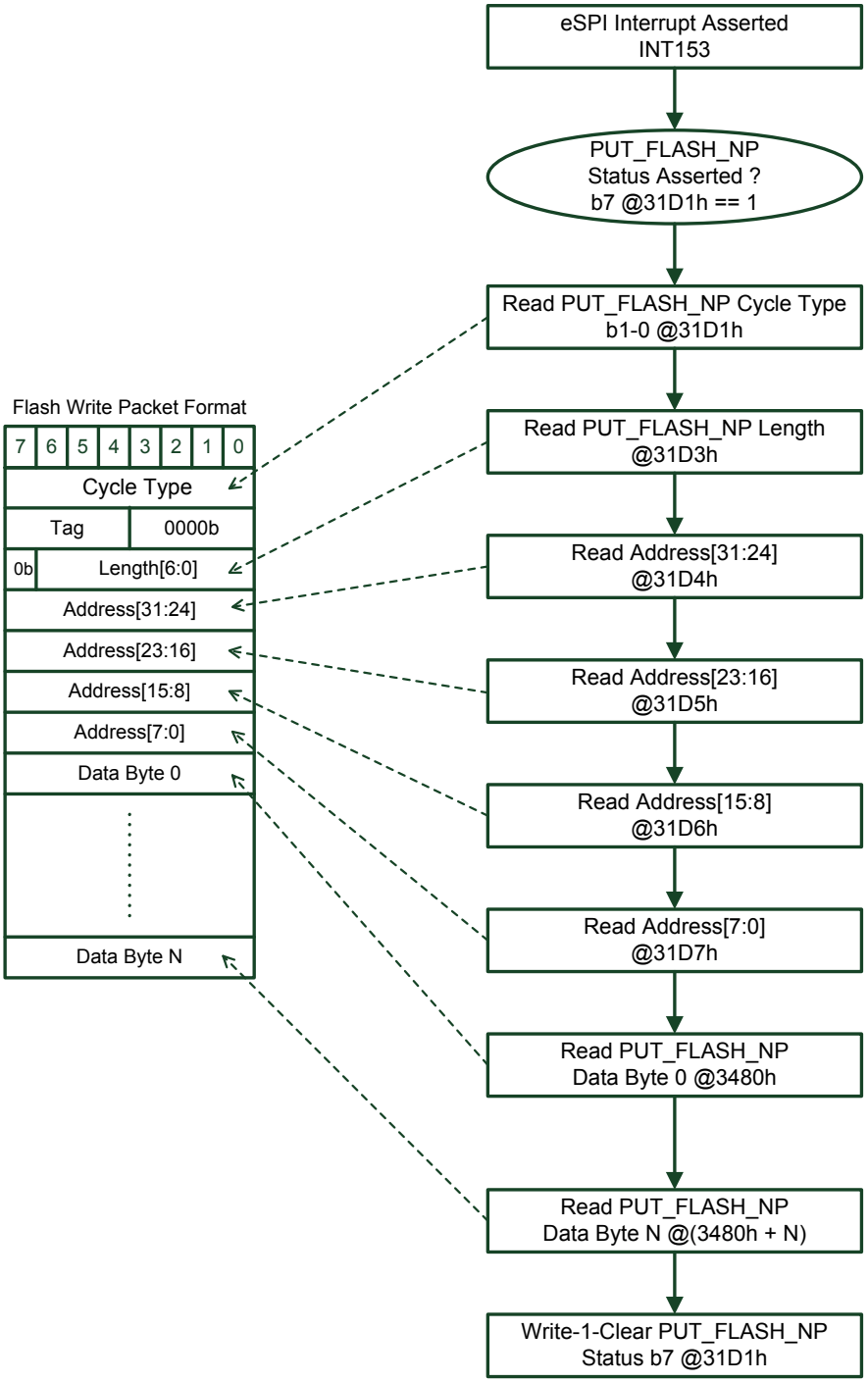
EC issues read cycles with the specified address to the flash, and returns the content of the flash to the eSPI master automatically.

- **Receive a Flash Write through eSPI Flash Channel**

EC issues program sequences with the specified address to the flash, and returns “Successful Completion” to the eSPI master automatically.

For some purpose, it also allows for processing the flash write with software’s intervention. The software sequence is listed below.

Figure 6-7 Flow of Receiving a Flash Write Transcation over eSPI Bus

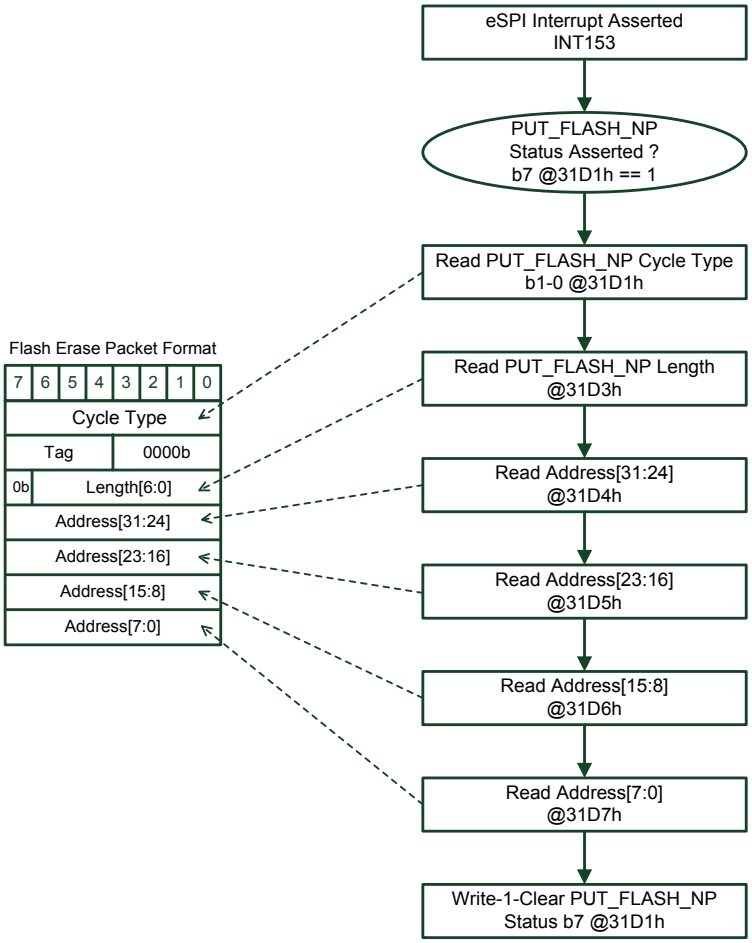


- **Receive A Flash Erase through eSPI Flash Channel**

EC issues erase sequences with the specified address to the flash, and returns “Successful Completion” to the eSPI master automatically. The software sequence is listed below.

For some purpose, it also allows for processing the flash erase with software’s intervention. The software sequence is listed below.

Figure 6-8 Flow of Receiving a Flash Erase Transcation over eSPI Bus



6.1.3.4 OOB Message Channel

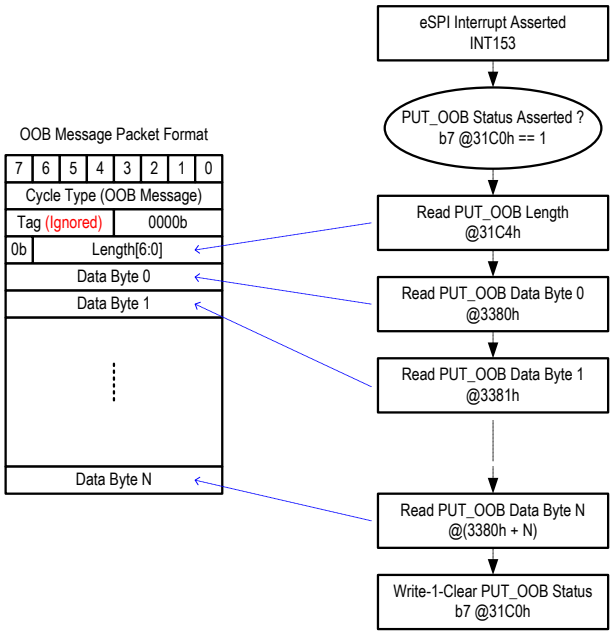
The OOB channel is used to handle transactions between the OOB processor and EC. EC is able to initiate an upstream OOB message transaction for reading of SKL-PCH HW information, including temperature and RTC time/date, using messages with predefined slave address and command codes.

The GET_OOB and PUT_OOB commands are supported.

- **Receive A Posted Transaction through eSPI OOB Message Channel**

EC is able to receive a posted OOB message transaction over the eSPI bus. The software sequence is listed below.

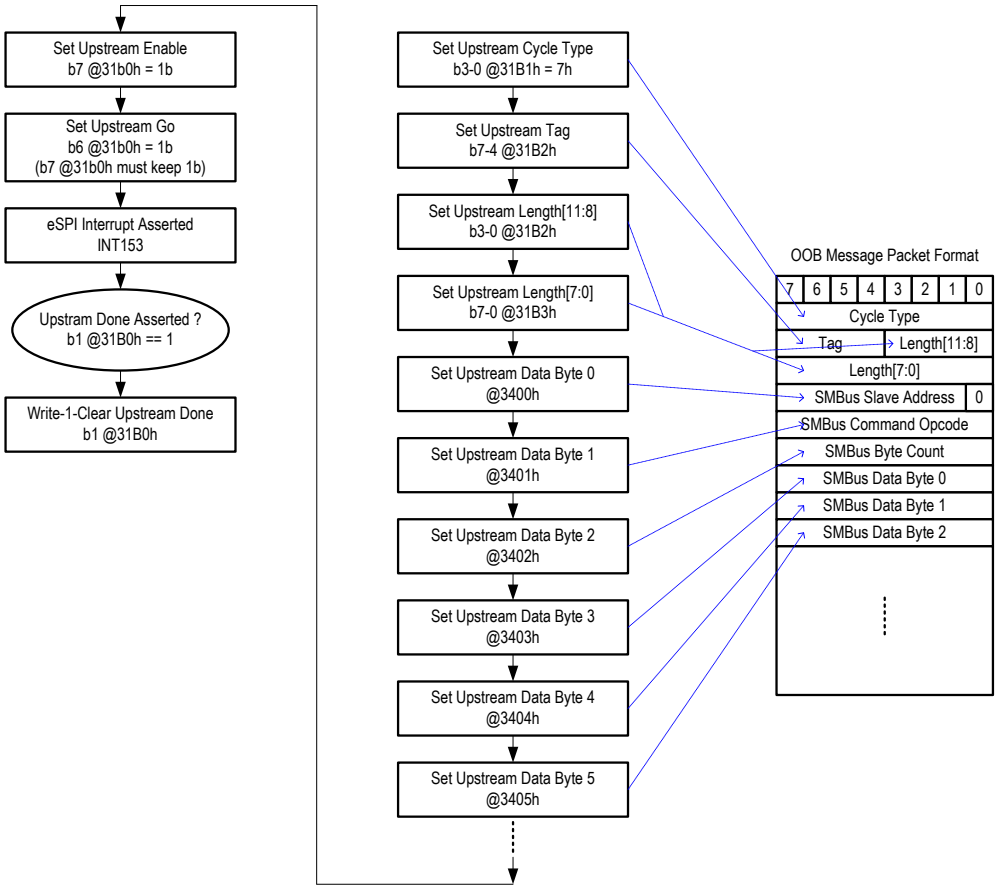
Figure 6-9 Flow of Receiving a OOB Message Transcation over eSPI Bus



- **Initiate A Posted Transaction through eSPI OOB Message Channel**

EC is able to initiate a posted OOB message transaction over the eSPI bus. The software sequence is listed below.

Figure 6-10 Flow of Initiating a OOB Message Transcation over eSPI Bus



6.1.3.5 Virtual Wires Channel

The Virtual Wires channel is used to communicate the state of sideband pins tunneled through eSPI as in-band messages. Serial IRQ interrupts are also communicated through this channel as in-band messages.

.

- Maximum virtual wire count supported: 7
- Supports interrupt event: IRQ0 – IRQ15
- Supports system event

- **Receive An In-band Message through eSPI Virtual Wires Channel**

EC is able to receive an in-band message through the eSPI Virtual Wires channel. The software sequence of handling an updated VW Index 2 event is listed below.

- eSPI VW Interrupt asserted (INT154)
- VWIDX2 Updated Flag asserted? (b0 @3291h)
- Read VW Index 2 @3202h to get the state of VW Index 2
- Write-1-clear VWIDX2 Updated Flag (b0 @3291h)
- Read VW Index2 @3202h again to prevent event losing during "Write-1-clear VWIDX2 Updated Flag"

- **Initiate an In-band Message through eSPI Virtual Wires Channel**

EC is able to initiate an in-band message through eSPI Virtual Wires channel. The software sequence of initiating an in-band message for VW Index 4 is listed below.

Method 1: Write VW Index 4 @3204h to change the state of VW Index 4

If the state of VW Index 4 is different from that sent during the previous transaction, EC initiates an in-band message over the eSPI bus for updating VW Index 4. If not, EC does not initiate an in-band message.

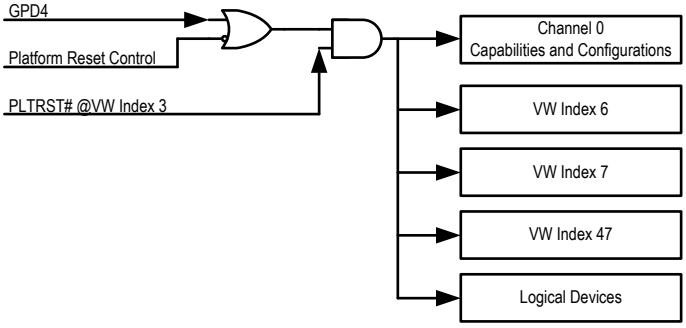
Method 2: Write 1 to VW Index 4 Resend @3293h

Writing 1 to VW Index 4 Resend forces EC to resend the state of VW Index 4 regardless of that sent during the previous transaction. VW Index 4 Resend is automatically cleared after the in-band message is sent through the eSPI Virtual Wires channel.

- **Platform Reset**

Platform Reset event is communicated through the PLTRST# virtual wire. It also can be asserted from GPD4 if Platform Reset Control is set. The Platform Reset event is used in resetting the circuits listed below.

Figure 6-11 Scheme of Platform Reset



6.1.3.6 Expression of eSPI Interrupt Events

eSPI Interrupt Events	Interrupt Register	Description
eSPI Interrupt	b7@3190h & b7@31A1h	PUT_PC Status
	b7@31A0h & b7@31A1h	Flash Access Channel Enable Deasserted Flag
	b6@31A0h & b7@31A1h	OOB Message Channel Enable Deasserted Flag
	b5@31A0h & b7@31A1h	VW Channel Enable Deasserted Flag
	b4@31A0h & b7@31A1h	Peripheral Channel Enable Deasserted Flag
	b3@31A0h & b7@31A1h	Flash Access Channel Enable Asserted Flag
	b2@31A0h & b7@31A1h	OOB Message Channel Enable Asserted Flag
	b1@31A0h & b7@31A1h	VW Channel Enable Asserted Flag
	b0@31A0h & b7@31A1h	Peripheral Channel Enable Asserted Flag
	b2@31B0h & b5@31B0h	Upstream Channel Disable
	b1@31B0h & b5@31B0h	Upstream Done
	b7@31C0h & b7@31C1h	PUT_OOB Status
eSPI VW Interrupt	b7@3291h & b7@3290h	VWIDX47 Updated Flag
	b6@3291h & b7@3290h	VWIDX44 Updated Flag
	b5@3291h & b7@3290h	VWIDX43 Updated Flag
	b4@3291h & b7@3290h	VWIDX42 Updated Flag
	b3@3291h & b7@3290h	VWIDX41 Updated Flag
	b2@3291h & b7@3290h	VWIDX7 Updated Flag
	b1@3291h & b7@3290h	VWIDX3 Updated Flag
	b0@3291h & b7@3290h	VWIDX2 Updated Flag

6.1.4 EC Interface Registers, eSPI slave

The EC interface registers are listed below. The base address for eSPI slave is 3100h.
The address 00h-17h are DWord registers defined in eSPI specification and stored in Big Endian order.

Table 6-1. EC View Register Map, eSPI slave

7 0	Offset
Device Identification	00h-03h
General Capabilities and Configurations	04h-07h
Channel 0 Capabilities and Configurations	08h-0Bh
Channel 1 Capabilities and Configurations	0Ch-0Fh
Channel 2 Capabilities and Configurations	10h-13h
Channel 3 Capabilities and Configurations	14h-17h
Channel 3 Capabilities and Configurations 2	18h-1Bh
eSPI PC Control 0 (ESPCTRL0)	90h
eSPI PC Control 1 (ESPCTRL1)	91h
eSPI PC Control 2 (ESPCTRL2)	92h
eSPI PC Control 3 (ESPCTRL3)	93h
eSPI PC Control 4 (ESPCTRL4)	94h
eSPI PC Control 5 (ESPCTRL5)	95h
eSPI PC Control 6 (ESPCTRL6)	96h
eSPI PC Control 7 (ESPCTRL7)	97h
eSPI General Control 0 (ESGCTRL0)	A0h
eSPI General Control 1 (ESGCTRL1)	A1h
eSPI General Control 2 (ESGCTRL2)	A2h

7	0	Offset
eSPI General Control 3 (ESGCTRL3)		A3h
eSPI Upstream Control 0 (ESUCTRL0)		B0h
eSPI Upstream Control 1 (ESUCTRL1)		B1h
eSPI Upstream Control 2 (ESUCTRL2)		B2h
eSPI Upstream Control 3 (ESUCTRL3)		B3h
eSPI Upstream Control 6 (ESUCTRL6)		B6h
eSPI Upstream Control 7 (ESUCTRL7)		B7h
eSPI Upstream Control 8 (ESUCTRL8)		B8h
eSPI OOB Control 0 (ESOCTRL0)		C0h
eSPI OOB Control 1 (ESOCTRL1)		C1h
eSPI OOB Control 4 (ESOCTRL4)		C4h
eSPI SAFS Control 0 (ESPISAFSC0)		D0h
eSPI SAFS Control 1 (ESPISAFSC1)		D1h
eSPI SAFS Control 2 (ESPISAFSC2)		D2h
eSPI SAFS Control 3 (ESPISAFSC3)		D3h
eSPI SAFS Control 4 (ESPISAFSC4)		D4h
eSPI SAFS Control 5 (ESPISAFSC5)		D5h
eSPI SAFS Control 6 (ESPISAFSC6)		D6h
eSPI SAFS Control 7 (ESPISAFSC7)		D7h

6.1.4.1 Device Identification

Address Offset: 00h-02h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R	-	**Version ID** Read returns 01h.

6.1.4.2 General Capabilities and Configurations

Address Offset: 04h

Bit	R/W	Default	Description
7	R	0b	**CRC Checking Enable** This bit is set to ‘1’ by the eSPI master to enable the CRC’s checking on the eSPI bus. 0b: CRC checking is disabled. 1b: CRC checking is enabled.
6	R	0b	**Response Modifier Enable** This bit is set to ‘1’ to enable the use of Response Modifier by eSPI slave to append either a peripheral (channel 0) completion, a virtual wire (channel 1) packet or a flash access (channel 3) completion to the GET_STATUS response phase. When this bit is a ‘0’, the eSPI slave must only use the Response Modifier of “00”, i.e. no append.
5	-	-	**Reserved**

Bit	R/W	Default	Description
4	R	0b	**Alert Mode** This bit serves to configure the Alert mechanism used by the slave to initiate a transaction on the eSPI interface. 0b: EIO1 (I/O[1]) pin is used to signal the Alert event. 1b: A dedicated ALERT# pin is used to signal the Alert event. Note: This bit can only be '0' in a single master-single slave topology. For single master-multiple slave topology, this bit must be programmed to '1'.
3-2	R	0b	**I/O Mode Select** The eSPI master programs this field to enable the appropriate mode of operation, which will take effect at the deassertion edge of the Chip Select#. The I/O mode configured in this field must be supported by both the master and slave. 00b: Single I/O 01b: Dual I/O 10b: Quad I/O 11b: Reserved
1-0	R	11b	**I/O Mode Support** Read returns 11b. 00b: Single I/O 01b: Single and Dual I/O 10b: Single and Quad I/O 11b: Single, Dual and Quad I/O

Address Offset: 05h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	000b	**Operating Frequency** This field identifies the frequency of operation. 000b: 20 MHz 001b: 25 MHz 010b: 33 MHz 011b: 50 MHz 100b: 66 MHz Otherwise: Reserved
3	-	0h	**Reserved**
2-0	R/W	010b	**Maximum Frequency Supported** This field identifies the maximum frequency of operation supported by the slave. 000b: 20 MHz 001b: 25 MHz 010b: 33 MHz 011b: 50 MHz 100b: 66 MHz Otherwise: Reserved The slave that indicates support for the maximum frequency of operation through this field will support all the lower frequencies on the list as well.

Address Offset: 06h

Bit	R/W	Default	Description
7-4	R	0h	**Maximum WAIT STATE Allowed** The eSPI master sets the maximum WAIT STATE allowed to be responded by the slave before it must respond with an ACCEPT, DEFER, NON-FATAL ERROR or FATAL ERROR response code. This is a 1-based field in the granularity of byte time. When “0”, it indicates a value of 16 byte time. A byte time corresponds to 8 serial clocks in the Single I/O mode, 4 serial clocks in the Dual I/O mode or 2 serial clocks in the Quad I/O mode.
3	-	0h	**Reserved**

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	1111b	**Channel Supported** When any of the four bits is set, it indicates its corresponding channel is supported by the slave. Bit-0: Peripheral Channel Bit-1: Virtual Wire Channel Bit-2: OOB Message Channel Bit-3: Flash Access Channel Otherwise: Reserved for platform specific channels

6.1.4.3 Channel 0 Capabilities and Configurations

Address Offset: 08h-09h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 0Ah

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	001b	**Peripheral Channel Maximum Read Request Size** The eSPI master sets the maximum size of the read request for the Peripheral channel. The length must not cross the naturally aligned address boundary of the corresponding Maximum Read Request Size. 001b: 64 bytes address aligned max read request size. Otherwise: Reserved.
3	-	-	**Reserved**
2-0	R	001b	**Peripheral Channel Maximum Payload Size Selected** The eSPI master sets the maximum payload size for the Peripheral channel. The value set by the eSPI master must never be more than that advertised in the Max Payload Size Supported field. The payload of the transaction must not cross the naturally aligned address boundary of the corresponding Maximum Payload Size. 001b: 64 bytes address aligned max payload size. Otherwise: Reserved.

Address Offset: 0Bh

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	000b	**Peripheral Channel Maximum Payload Size Supported** This field advertises the Maximum Payload Size supported by the slave. 001b: 64 bytes address aligned max payload size. Otherwise: Reserved
3	-	-	**Reserved**
2	R	0b	**Bus Master Enable** Not supported.
1	R	0b	**Peripheral Channel Ready** When this bit is a '1', it indicates that the slave is ready to accept transactions on the Peripheral channel. The eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	1b	**Peripheral Channel Enable** The channel is by default enabled after the ERST# (eSPI Reset#). This bit is cleared to '0' by the eSPI master to disable the Peripheral channel. Besides, clearing this bit from '1' to '0' triggers a reset to the Peripheral channel. The channel remains disabled until this bit is set to '1' again. Prior to disabling the Peripheral channel, the Bus Master Enable bit should be cleared to '0' to disable the bus mastering cycles.

6.1.4.4 Channel 1 Capabilities and Configurations

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	0h	**Operating Maximum Virtual Wire Count** This is the maximum number of Virtual Wire groups that can be sent in a single Virtual Wire packet. This is a 0-based count. The default value of 0 indicates count of 1. The value configured in this field must never be more than that advertised in the Maximum Virtual Wire Count Supported field.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	111b	**Maximum Virtual Wire Count Supported** This field advertises the Maximum Virtual Wire Count supported by the slave. If the slave supports different count values as initiators and as receivers of the Virtual Wires, this field indicates the lower of the two. The Virtual Wire Count specifies the maximum number of Virtual Wire groups being communicated in a single Virtual Wire packet. The eSPI slave must advertise a value of "000111b" or more in this field to indicate the support of at least 8 Virtual Wire groups being communicated in a single Virtual Wire packet. This is a 0-based count.

Address Offset: 0Fh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R	0b	**Virtual Wire Channel Ready** When this bit is a '1', it indicates that the slave is ready to accept transactions on the Virtual Wire channel. The eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	0b	**Virtual Wire Channel Enable** This bit is set to '1' by the eSPI master to enable the Virtual Wire channel. Clearing this bit from '1' to '0' will not reset the Virtual Wire channel. The channel is by default disabled after the ERST# (eSPI Reset#).

6.1.4.5 Channel 2 Capabilities and Configurations

Address Offset: 10h-11h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 12h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R	001b	**OOB Message Channel Maximum Payload Size Selected** The eSPI master sets the maximum payload size for the OOB Message channel. The value set by the eSPI master must never be more than the value advertised in the Max Payload Size Supported field. 001b: 64 bytes max payload size. Otherwise: Reserved

Address Offset: 13h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	001b	**OOB Message Channel Maximum Payload Size Supported** This field advertises the Maximum Payload Size supported by the slave. 001b: 64 bytes max payload size. Otherwise: Reserved
3-2	-	-	**Reserved**
1	R	0b	**OOB Message Channel Ready** When this bit is a '1', it indicates that the slave is ready to accept transactions on the OOB Message channel. The eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	0b	**OOB Message Channel Enable** This bit is set to '1' by the eSPI master to enable the OOB Message channel. Clearing this bit from '1' to '0' triggers a reset to the OOB Message channel such as during error handling. The channel remains disabled until this bit is set to '1' again. The channel is by default disabled after the ERST# (eSPI Reset#).

6.1.4.6 Channel 3 Capabilities and Configurations

Address Offset: 14h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 15h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Flash Sharing Capability Supported** This field indicates the flash sharing capability supported by the slave. 00b: MAFS supported. 01b: MAFS supported. 10b: SAFS supported. 11b: MAFS/SAFS supported.

Address Offset: 16h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R	001b	**Flash Access Channel Maximum Read Request Size** The eSPI master sets the maximum read request size for the Flash Access channel. The length of the read request must not cross the naturally aligned address boundary of the corresponding Maximum Read Request Size. 001b: 64 bytes max payload size. Otherwise: Reserved
3	R	0b	**Flash Sharing Mode** When Flash Access channel is supported, this bit advertises the flash sharing scheme intended by the slave. 0b: Master attached flash sharing. 1b: Slave attached flash sharing. This bit is read-only and the readout value is always ‘0’ in the base specification as it is defined as the master attached flash sharing.
2-0	R	001b	**Flash Access Channel Maximum Payload Size Selected** The eSPI master sets the maximum payload size for the Flash Access channel. The value set by the eSPI master must never be more than that advertised in the Max Payload Size Supported field. 001b: 64 bytes max payload size. Otherwise: Reserved

Address Offset: 17h

Bit	R/W	Default	Description
7-5	R	001b	**Flash Access Channel Maximum Payload Size Supported** This field advertises the Maximum Payload Size supported by the slave. 001b: 64 bytes max payload size. Otherwise: Reserved
4-2	R	001b	**Flash Block Erase Size** The eSPI master sets this field to communicate the block erase size to the slave. This field is applicable only to the master attached flash sharing scheme. 000b: Reserved 001b: 4 Kbytes 010b: 64 Kbytes 011b: Both 4 Kbytes and 64 Kbytes are supported 100b: 128 Kbytes 101b: 256 Kbytes 110b – 111b: Reserved
1	R	0b	**Flash Access Channel Ready** When this bit is a '1', it indicates that the slave is ready to accept transactions on the Flash Access channel. eSPI master should poll this bit after the channel is enabled before running any transaction on this channel to the slave. 0b: Channel is not ready. 1b: Channel is ready.
0	R	0b	**Flash Access Channel Enable** This bit is set to '1' by eSPI master to enable the Flash Access channel. Clearing this bit from '1' to '0' triggers a reset to the Flash Access channel such as during error handling. The channel remains disabled until this bit is set to '1' again. The channel is by default disabled after the ERST# (eSPI Reset#).

6.1.4.7 Channel 3 Capabilities and Configurations 2

Address Offset: 18h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

Address Offset: 19h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	00000b	**Target RPMC Supported** This field indicates the total number of Replay Protected Monotonic Counters (RPMC) supported by the Slave. It is a 1-based field. 0h: Slave does not support RPMC 1h: Slave supports up to 1 RPMC 2h: Slave supports up to 2 RPMC ... 3Fh: Slave supports up to 63 RPMC

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	00000100b	**Target Flash Erase Block Size for Master's Regions** This field indicates the sizes of the erase commands the master may issue. If multiple bits are set, the master may issue an erase using any of the indicated sizes. If multiple regions are accessible by the master, this field advertises the common erase block sizes for these regions. This field is only applicable when slave attached flash sharing scheme is selected. Bit 0: 1 Kbytes EBS supported Bit 1: 2 Kbytes EBS supported Bit 2: 4 Kbytes EBS supported Bit 3: 8 Kbytes EBS supported Bit 4: 16 Kbytes EBS supported Bit 5: 32 Kbytes EBS supported Bit 6: 64 Kbytes EBS supported Bit 7: 128 Kbytes EBS supported

Address Offset: 1Bh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R	001b	**Target Maximum Read Request Size Supported** This field indicates the maximum read request size supported by the slave as the Target on the Flash Access channel. This field is only applicable when slave attached flash sharing scheme is selected. 000b, 001b: 64 bytes max read request size 010b: 128 bytes max read request size 011b: 256 bytes max read request size 100b: 512 bytes max read request size 101b: 1024 bytes max read request size 110b: 2048 bytes max read request size 111b: 4096 bytes max read request size

6.1.4.8 eSPI PC Control 0 (ESPCTRL0)

Address Offset: 90h

Bit	R/W	Default	Description
7	R/WC	0b	**PUT_PC Status** It indicates that the eSPI slave has received a peripheral posted/completion. Write-1-clear to release PC_FREE.
6-4	-	-	**Reserved**
3-0	R	-	**PUT_PC Cycle Type** It stores the decoded cycle type in a received posted/completion cycle. 3h: Message 4h: Message with Data 5h: Successful Completion Without Data 6h: Successful Completion With Data / the first completion 7h: Successful Completion With Data / the middle completion 8h: Successful Completion With Data / the last completion 9h: Successful Completion With Data / the only completion Ah: Unsuccessful Completion Without Data / the last completion Bh: Unsuccessful Completion Without Data / the only completion Ch: Reserved Dh: Reserved Eh: Reserved Fh: Invalid Cycle Type

6.1.4.9 eSPI PC Control 1 (ESPCTRL1)

Address Offset: 91h

Bit	R/W	Default	Description
7-4	R	-	**PUT_PC Tag** It stores the Tag field in a received posted/completion cycle.
3-0	-	-	**Reserved**

6.1.4.10 eSPI PC Control 2 (ESPCTRL2)

Address Offset: 92h

Bit	R/W	Default	Description
1	-	-	**Reserved**
6-0	R	-	**PUT_PC Length** It stores the Length field in a received posted/completion cycle.

6.1.4.11 eSPI PC Control 3 (ESPCTRL3)

Address Offset: 93h

Bit	R/W	Default	Description
7-0	R	-	**Message Code** It stores the Message Code field in a message packet.

6.1.4.12 eSPI PC Control 4 (ESPCTRL4)

Address Offset: 94h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 0** It stores the Message Specific Byte 0 field in a message packet.

6.1.4.13 eSPI PC Control 5 (ESPCTRL5)

Address Offset: 95h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 1** It stores the Message Specific Byte 1 field in a message packet.

6.1.4.14 eSPI PC Control 6 (ESPCTRL6)

Address Offset: 96h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 2** It stores the Message Specific Byte 2 field in a message packet.

6.1.4.15 eSPI PC Control 7 (ESPCTRL7)

Address Offset: 97h

Bit	R/W	Default	Description
7-0	R	-	**Message Specific Byte 3** It stores the Message Specific Byte 3 field in a message packet.

6.1.4.16 eSPI General Control 0 (ESGCTRL0)

Address Offset: A0h

Bit	R/W	Default	Description
7	R/WC	0b	**Flash Access Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'Flash Access Channel Enable' bit after eSPI issues SET_CONFIGURATION.
6	R/WC	0b	**OOB Message Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'OOB Message Channel Enable' bit after eSPI issues SET_CONFIGURATION.
5	R/WC	0b	**VW Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'Virtual Wire Channel Enable' bit after eSPI issues SET_CONFIGURATION.
4	R/WC	0b	**Peripheral Channel Enable Deasserted Flag** It indicates a 1-to-0 transition of 'Peripheral Channel Enable' bit after eSPI issues SET_CONFIGURATION.
3	R/WC	0b	**Flash Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'Flash Access Channel Enable' bit after eSPI issues SET_CONFIGURATION.
2	R/WC	0b	**OOB Message Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'OOB Message Channel Enable' bit after eSPI issues SET_CONFIGURATION.
1	R/WC	0b	**VW Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'Virtual Wire Channel Enable' bit after eSPI issues SET_CONFIGURATION.
0	R/WC	0b	**Peripheral Channel Enable Asserted Flag** It indicates a 0-to-1 transition of 'Peripheral Channel Enable' bit after eSPI issues SET_CONFIGURATION.

6.1.4.17 eSPI General Control 1 (ESGCTRL1)

Address Offset: A1h

Bit	R/W	Default	Description
7	R/W	0b	**eSPI Interrupt Enable**
6	-	-	**Reserved**
5	R/W	0b	**Ignore eSPI Unsupported Memory Read Address (IESPIUMRA)** 0b: Return "Unsuccessful Completion" for unsupported memory addresses (only for read cycle). 1b: Return "Successful Completion" for all memory addresses (only for read cycle).
4	R/W	0b	**Ignore eSPI Unsupported IO Address (IESPIUIOA)** 0b: Return "Unsuccessful Completion" for unsupported IO addresses. 1b: Return "Successful Completion" for all IO addresses.
3-0	-	-	**Reserved**

6.1.4.18 eSPI General Control 2 (ESGCTRL2)

Address Offset: A2h

Bit	R/W	Default	Description
7	R/W	0b	**eSPI Queue Clock Switch Enable (ESPIQCSE)** 0b: eSPI TX/RX queues are clocked by the PLL clock and do not work during the sleep mode. 1b: Switch the clock of eSPI TX/RX queues to ESCK while entering the sleep mode, which lets eSPI TX/RX queues work without the PLL clock.
6	R/W	0b	**eSPI Input Pad Gating (ESPIIPG)** 0b: eSPI Pad is not gated. 1b: eSPI Pad is gated.
5	-	-	**Reserved**
4	R/W	0b	**eSPI To WUC Enable** 0b: Disable 1b: If an eSPI transaction is accepted, WU42 interrupt will be asserted.
3-0	-	-	**Reserved**

6.1.4.19 eSPI General Control 3 (ESGCTRL3)

Address Offset: A3h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Suspend eSPI Peripheral Channel (SESPIPC)** 0b: Return peripheral channel ready for the GET_CONFIGURATION cycle. 1b: Return peripheral channel non-ready for the GET_CONFIGURATION cycle.

6.1.4.20 eSPI Upstream Control 0 (ESUCTRL0)

Address Offset: B0h

Bit	R/W	Default	Description
7	R/W	0b	**Upstream Enable** 0b: Disable 1b: Initiating eSPI upstream transactions is allowed.
6	R/W	-	**Upstream Go** Write-1 to initiate an eSPI upstream transaction if not 'Upstream Busy'. Write-0 is ignored.
5	R/W	0b	**Upstream Interrupt Enable** 0b: Disable 1b: Enable
4-3	-	-	**Reserved**
2	R/WC	0b	**Upstream Channel Disable** A flag to indicate the corresponding channel of the eSPI upstream transaction is disabled. Wrtie-1 to clear this bit.
1	R/WC	0b	**Upstream Done** A flag to indicate the eSPI upstream transaction is done. Wrtie-1 to clear this bit.
0	R	0b	**Upstream Busy** The upstream is in progress (busy).

6.1.4.21 eSPI Upstream Control 1 (ESUCTRL1)

Address Offset: B1h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0b	**Upstream Cycle Type** 7h: OOB Message 8h: Flash Read 9h: Flash Write Ah: Flash Erase Otherwise: Reserved

6.1.4.22 eSPI Upstream Control 2 (ESUCTRL2)

Address Offset: B2h

Bit	R/W	Default	Description
7-4	R/W	0h	**Upstream Tag** The written data will be filled in the Tag field of the upstream transaction.
3-0	R/W	0h	**Upstream Length** The written data will be filled in the Length[11:8] field of the upstream transaction.

6.1.4.23 eSPI Upstream Control 3 (ESUCTRL3)

Address Offset: B3h

Bit	R/W	Default	Description
0	R/W	00h	**Upstream Length** The written data will be filled in the Length[7:0] field of the upstream transaction.

6.1.4.24 eSPI Upstream Control 6 (ESUCTRL6)

Address Offset: B6h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R	0b	**PUT_FLASH_C Cycle Type** It stores the decoded cycle type in a received flash completion transaction. 0h: Successful Completion Without Data 4h: Successful Completion With Data / the only completion 5h: Unsuccessful Completion Without Data / the last completion 6h: Unsuccessful Completion Without Data / the only completion Fh: Invalid Cycle Type Otherwise: Reserved

6.1.4.25 eSPI Upstream Control 7 (ESUCTRL7)

Address Offset: B7h

Bit	R/W	Default	Description
7-4	R	0b	**PUT_FLASH_C Tag** It stores the Tag field in a received flash completion transaction.
3-0	-	-	**Reserved**

6.1.4.26 eSPI Upstream Control 8 (ESUCTRL8)

Address Offset: B8h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R	0b	**PUT_FLASH_C Length** It stores the Length field in a received flash completion transaction.

6.1.4.27 eSPI OOB Control 0 (ESOCTRL0)

Address Offset: C0h

Bit	R/W	Default	Description
7	R/WC	0b	**PUT_OOB Status** It indicates that the eSPI slave has received a PUT_OOB message. Write-1 to clear this bit for the next coming posted transaction.
6-0	-	-	**Reserved**

6.1.4.28 eSPI OOB Control 1 (ESOCTRL1)

Address Offset: C1h

Bit	R/W	Default	Description
7	R/W	0b	**PUT_OOB Interrupt Enable** 0b: Interrupt disabled 1b: Interrupt enabled
6-0	-	-	**Reserved**

6.1.4.29 eSPI OOB Control 4 (ESOCTRL4)

Address Offset: C4h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R	00h	**PUT_OOB Length** It stores the Length field in a received PUT_OOB Message packet.

6.1.4.30 eSPI SAFS Control 0 (ESPISAFSC0)

Address Offset: D0h

Bit	R/W	Default	Description
7	R/W	0b	**PUT_FLASH_NP Interrupt Enable** 0b: Interrupt disabled 1b: Interrupt enabled
6-2	-	-	**Reserved**
1	R/W	0b	**PUT_FLASH_NP Flash Erase Software Mode Enable** 0b: Process flash erase sequences by hardware. 1b: Process flash erase sequences with software's intervention.
0	R/W	0b	**PUT_FLASH_NP Flash Write Software Mode Enable** 0b: Process flash program sequences by hardware. 1b: Process flash program sequences with software's intervention.

6.1.4.31 eSPI SAFS Control 1 (ESPISAFSC1)

Address Offset: D1h

Bit	R/W	Default	Description
7	R/WC	0b	**PUT_FLASH_NP Status** It indicates that the eSPI slave has received a PUT_FLASH_NP packet. Write 1 to clear this bit for the next coming transaction.
6-2	-	-	**Reserved**
1-0	R	00h	**PUT_FLASH_NP Cycle Type** It stores the decoded cycle type in a received PUT_FLASH_NP packet. 1h: Flash write 2h: Flash erase Otherwise: Reserved

6.1.4.32 eSPI SAFS Control 2 (ESPISAFSC2)

Address Offset: D2h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

6.1.4.33 eSPI SAFS Control 3 (ESPISAFSC3)

Address Offset: D3h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R	00h	**PUT_FLASH_NP Length** It stores the length field in a received PUT_FLASH_NP packet.

6.1.4.34 eSPI SAFS Control 4 (ESPISAFSC4)

Address Offset: D4h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[31:24]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.4.35 eSPI SAFS Control 5 (ESPISAFSC5)

Address Offset: D5h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[23:16]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.4.36 eSPI SAFS Control 6 (ESPISAFSC6)

Address Offset: D6h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[15:8]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.4.37 eSPI SAFS Control 7 (ESPISAFSC7)

Address Offset: D7h

Bit	R/W	Default	Description
7-0	R	00h	**PUT_FLASH_NP Address[7:0]** It stores the address field in a received PUT_FLASH_NP packet.

6.1.5 EC Interface Registers, eSPI VW

The EC interface registers are listed below. The base address for eSPI VW is 3200h.

Table 6-2. EC View Register Map, eSPI VW

7 0	Offset
VW Index 0 (VWIDX0)	00h
VW Index 2-7 (VWIDX2-7)	02h-07h
VW Index 40-47 (VWIDX40-47)	40h-47h
VW Contrl 0 (VWCTRL0)	90h
VW Contrl 1 (VWCTRL1)	91h
VW Contrl 2 (VWCTRL2)	92h
VW Contrl 3 (VWCTRL3)	93h
VW Contrl 5 (VWCTRL5)	95h
VW Contrl 6 (VWCTRL6)	96h
VW Contrl 7 (VWCTRL7)	97h

6.1.5.1 VW Index 0 (VWIDX0)

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	0b	**Interrupt Level** 0b: Low 1b: High
6-4	-	-	**Reserved**
3-0	R/W	11b	**Interrupt Line** IRQ0-15

6.1.5.2 VW Index 2-7 (VWIDX2-7)

Address Offset: 02h-07h

Bit	R/W	Default	Description
7-4	R/W	0b	**Valid** 0b: Low 1b: High
3-0	R/W	11b	**Level** 0b: Low 1b: High These registers correspond to the eSPI specification.

6.1.5.3 VW Index 40-47 (VWIDX40-47)

Address Offset: 40h-47h

Bit	R/W	Default	Description
7-4	R/W	0b	**Valid** 0b: Low 1b: High
3-0	R/W	11b	**Level** 0b: Low 1b: High These registers correspond to the Skylake specification.

6.1.5.4 VW Contrl 0 (VWCTRL0)

Address Offset: 90h

Bit	R/W	Default	Description
7	R/W	0b	**VW Interrupt Enable** 0b: Disable 1b: Enable
6-2	-	-	**Reserved**
1	R/W	0b	**Auto Send VW SUS_ACK# Interrupt Enable (ASVWSIE)** 0b: Disable 1b: Issue an interrupt if ASVWSF is set.
0	R/W	0b	**Auto Send VW Boot_Load_Done/Status Interrupt Enable (ASVWBIE)** 0b: Disable 1b: Issue an interrupt if ASVWBF is set.

6.1.5.5 VW Contrl 1 (VWCTRL1)

Address Offset: 91h

Bit	R/W	Default	Description
7	R/WC	0b	**VWIDX47 Updated Flag** Write-1 to clear this bit.
6	R/WC	0b	**VWIDX44 Updated Flag** Write-1 to clear this bit.
5	R/WC	0b	**VWIDX43 Updated Flag** Write-1 to clear this bit.
4	R/WC	0b	**VWIDX42 Updated Flag** Write-1 to clear this bit.
3	R/WC	0b	**VWIDX41 Updated Flag** Write-1 to clear this bit.
2	R/WC	0b	**VWIDX7 Updated Flag** Write-1 to clear this bit.
1	R/WC	0b	**VWIDX3 Updated Flag** Write-1 to clear this bit.
0	R/WC	0b	**VWIDX2 Updated Flag** Write-1 to clear this bit.

6.1.5.6 VW Contrl 2 (VWCTRL2)

Address Offset: 92h

Bit	R/W	Default	Description
7	R/W	0b	**DSW_PWROK Source** 0b: Refers to SW_DSW_PWROK for DSW_PWROK. 1b: Refers to eSPI Reset# for DSW_PWROK.
6	R/W	0b	**SW_DSW_PWROK** Scratch bit and read returns the written data.
5	R/W	0b	**Platform Reset Control** 0b: Refers to PLTRST# virtual wire for Platform Reset. 1b: Refers to GPD4 for Platform Reset.
5-0	-	-	**Reserved**

6.1.5.7 VW Contrl 3 (VWCTRL3)

Address Offset: 93h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**VW Index 46 Resend** Write-1 to resend VW Index 46 over eSPI bus. This bit is automatically cleared after the transaction.
4	R/W	0b	**VW Index 45 Resend** Write-1 to resend VW Index 45 over eSPI bus. This bit is automatically cleared after the transaction.
3	R/W	0b	**VW Index 40 Resend** Write-1 to resend VW Index 40 over eSPI bus. This bit is automatically cleared after the transaction.
2	R/W	0b	**VW Index 6 Resend** Write-1 to resend VW Index 6 over eSPI bus. This bit is automatically cleared after the transaction.
1	R/W	0b	**VW Index 5 Resend** Write-1 to resend VW Index 5 over eSPI bus. This bit is automatically cleared after the transaction.
0	R/W	0b	**VW Index 4 Resend** Write-1 to resend VW Index 4 over eSPI bus. This bit is automatically cleared after the transaction.

6.1.5.8 VW Contrl 5 (VWCTRL5)

Address Offset: 95h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**VW SUS_WARN# Select (VWSS)** 0b: If ASVWSE is set to 1, EC sends SUS_ACK# after SUS_WARN# is deasserted. 1b: If ASVWSE is set to 1, EC sends SUS_ACK# after SUS_WARN# is asserted.
3-2	-	-	**Reserved**
1	R/W	0b	**Auto Send VW SUS_ACK# Enable (ASVWSE)** eSPI_Reset# is the fundamental reset to the eSPI interface. While MAFS configuration is enabled for a platform, EC may not fetch the codes through MAFS if an unexpected eSPI_Reset# event occurs. Set this bit to allow EC to send VW SUS_ACK# automatically after the eSPI master deasserts/asserts SUS_WARN#. 0b: Disable 1b: Enable
0	R/W	0b	**Auto Send VW Boot_Load_Done/Status Enable (ASVWBE)** eSPI_Reset# is the fundamental reset to the eSPI interface. While MAFS configuration is enabled for a platform, EC may not fetch the codes through MAFS if an unexpected eSPI_Reset# event occurs. Set this bit to allow EC to send VW Boot_Load_Done/Status automatically after an unexpected eSPI_Reset# event is deasserted. 0b: Disable 1b: Enable

6.1.5.9 VW Contrl 6 (VWCTRL6)

Address Offset: 96h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/WC	0b	**Auto Send VW SUS_ACK# Flag (ASVWSF)** Write 1 to clear this bit. 0b: Otherwise. 1b: VW SUS_ACK# has been sent automatically.
0	R/WC	0b	**Auto Send VW Boot_Load_Done/Status Flag (ASVWBF)** Write 1 to clear this bit. 0b: Otherwise. 1b: VW Boot_Load_Done/Status has been sent automatically.

6.1.5.10 VW Contrl 7 (VWCTRL7)

Address Offset: 97h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Auto Send VW SUS_ACK# Select (ASVWSS)** 0b: If ASVWSE is 1, EC sends SUS_ACK# =0. 1b: If ASVWSE is 1, EC sends SUS_ACK# =1.

6.1.6 EC Interface Registers, eSPI Queue 0

The EC interface registers are listed below. The base address for eSPI Queue 0 is 3300h.

Table 6-3. EC View Register Map, eSPI Queue 0

7	0	Offset
PUT_PC Data Byte 0-63		00h-3Fh
PUT_OOB Data Byte 0-79		80h-CFh

6.1.6.1 PUT_PC Data Byte 0-63 (PUTPCDB0-63)

Address Offset: 00h-3Fh

Bit	R/W	Default	Description
7-0	R	-	**PUT_PC Data Byte 0-63**

6.1.6.2 PUT_OOB Data Byte 0-79 (PUTOOBDB0-79)

Address Offset: 80h-CFh

Bit	R/W	Default	Description
7-0	R	-	**PUT_OOB Data Byte 0-79**

6.1.7 EC Interface Registers, eSPI Queue 1

The EC interface registers are listed below. The base address for eSPI Queue 1 is 3400h.

Table 6-4. EC View Register Map, eSPI Queue 1

7	0	Offset
Upstream Data Byte 0-79		00h-4Fh
PUT_FLASH_NP Data Byte 0-63		80h-BFh

6.1.7.1 Upstream Data Byte 0-79 (UDB0-79)

Address Offset: 00h-4Fh

Bit	R/W	Default	Description
7-0	R	-	**Upstream Data Byte 0-79**

6.1.7.2 PUT_FLASH_NP Data Byte 0-63 (PUTFLASHNPDB0-63)

Address Offset: 80h-BFh

Bit	R/W	Default	Description
7-0	R	-	**PUT_FLASH_NP Data Byte 0-63**

6.2 Low Pin Count Interface

6.2.1 Overview

The Low Pin Count (LPC) is an interface for modern ISA-free system. It is defined in Intel's LPC Interface Specification, Revision 1.1. There are seven host-controlled modules that can be accessed by the host via the LPC interface. These host-controlled modules are "Logical Devices" defined in Plug and Play ISA Specification, Version 1.0a.

6.2.2 Features

- Complies with Intel's LPC Interface Specification, Revision 1.1
- Supports SERIRQ and complies with Serialized IRQ Support for PCI Systems, Revision 6.0
- Supports LPCPD#/CLKRUN#
- Supports Plug and Play ISA registers
- Supports LPC 19.2MHz to 33MHz

6.2.3 Accepted LPC Cycle Type

The supported LPC cycle types are listed below:
* LPC I/O Read (16-bit address, 8-bit data)
* LPC I/O Write (16-bit address, 8-bit data)
* LPC Memory Read (32-bit address, 8-bit data)
* LPC Memory Write (32-bit address, 8-bit data)
* FWH Read (32-bit address, 8-bit data)
* FWH Write (32-bit address, 8-bit data)

I/O cycles are used to access PNPCFG and Logical Devices. Memory or FWH is used to access Flash content through SMFI module Host-Indirect memory cycles based on I/O cycles can also access Flash. Refer to SMFI Module for details about Host-Indirect memory access.

The following table describes how LPC module responds the I/O, Memory and FWH cycles from Host side in different conditions.

Table 6-5. LPC/FWH Response

Cycle Type/Condition		Read Response	Write Response
All Cycles before PLL Stable NOTE 4		Long-Wait	Long-Wait
I/O Cycle to PNPCFG or Logical Devices		Ready	Ready
I/O Cycle but Address Out Of Range		Cycle Ignored	Cycle Ignored
I/O Cycle to Locked PNPCFG by EC2I		Returns 00h	Cycle Ignored
Host-Indirect Memory Address NOTE 3		Ready	Ready
Memory Cycle, FWH Cycle or Host-Indirect Memory Data		Long-Waits until Ready	Long-Waits until Ready NOTE 1
Memory Cycle, FWH Cycle or Host-Indirect Memory Data but Address Protected by SMFI	*HERES=01*	Returns 00h	Cycle Ignored
Memory Cycle or Host-Indirect Memory Data but Address Out of Range		Cycle Ignored	Cycle Ignored
FWH Cycle but Address Out of Range		Ready	Ready
FWH Cycle but FWH ID is unmatched NOTE 2		Cycle Ignored	Cycle Ignored
FWH Cycle but HBREN bit in HCTRL2R register cleared		Cycle Ignored	Cycle Ignored

Note 1:
After reset, IT5121 responds Long-Waits before Ready for FWH Write Cycle.

If LPC host (South-Bridge) fails to recognize Long-Wait SYNC during FWH Write Cycle, it is recommended to use Host-Indirect Memory.

Note 2:
FWH ID is defined in FWHID field in SHMC register.

Note 3:
Host-Indirect Memory Cycles access the flash via LPC I/O Cycle. Host-Indirect Memory Address is combined with SMIMAR0, SMIMAR1, SMIMAR2 and SMIMAR3 registers. Host-Indirect Memory Data is SMIMDR register.

Note 4:
The host LPC interface is disabled in sleep mode.

6.2.4 Debug Port Function

LPC module implements two latch signals for Main-Board debug purpose. LPC I/O write cycles with address equal to 80h will cause the LPC module to assert L80HLAT and L80LLAT signals which provide a simple external logic to latch it in order to display on LED, even though I/O port 80h is not recognized by PNPCFG or any Logical Device. L80HLAT goes high when it is time to latch the high-nibble of the data written to port 80h, and L80LLAT means the low-nibble.

Port 80h data can be read via parallel port with the software provided by ITE.

6.2.5 Serialized IRQ (SERIRQ)

IT5121 has programmable IRQ number for each logical device. Available IRQ numbers are 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, and 15.

Different logical devices inside IT5121 can share the same IRQ number if they have the same IRQPS bit in IRQTP register and are configured as the same triggered mode (all level-triggered or all edge triggered) in their EC side registers.

But it is not allowed to share an IRQ number with a logical device outside IT5121. Note that edge-triggered interrupts are not suitable for sharing in most cases.

6.2.6 Related Interrupts to WUC

- Interrupt to WUC
  If the LPC address of an I/O, LPC Memory or FWH Cycle on LPC bus is accepted, WU42 interrupt will be asserted.

6.2.7 LPCPD# and CLKRUN#

- LPCPD#
  LPCPD# is used as internal “power good” signal to indicate the status of VCC. It is recommended to be implemented. See also VCCDO bit in RSTS register in 7.17.4.5 on page 441.

- CLKRUN#
  When SERIRQ is in the continuous/quiet mode and LPCCLK is active, CLKRUN# is used for maintaining LPCCLK to make sure that the SERIRQ status is entirely transferred to the host side.

  When SERIRQ is in the quiet mode and LPCCLK is stopped, CLKRUN# is used for restoring LPCCLK if there is any interrupt status transition required to be transferred to the host side.

6.2.8 Check Items

If EC fails in LPC memory or I/O cycles at boot, check the following recommended items first.

- LPC/FWH memory cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether HBREN bit is enabled in HCTRL2R register.
  Check whether the firmware doesn't change the read protection control.

- LPC I/O cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether BADDR1-0 field in BADRSEL register are in correct setting.
  Check whether EC2I is not locking PNPCFG access from the host side.

6.3 Plug and Play Configuration (PNPCFG)

The host interface registers of PNPCFG (Plug and Play Configuration) are listed below. The base address can be configured via BADDR1-0 field in BADRSEL register. Note that bit 0 of SWCBALR has to be zero.
To access a register of PNPCFG, write target index to address port and access this PNPCFG register via data port. If accessing the data port without writing index to address port, the latest value written to address port is used as the index. Reading the address port register returns the last value written to it.

Table 6-6. Host View Register Map, PNPCFG

7 0	BADDR1-0 =00b	BADDR1-0 =01b	BADDR1-0 =10b	BADDR1-0 =11b
	I/O Port Address			
Address Port	2Eh	4Eh	(SWCBAHR, SWCBALR)	Reserved
Data Port	2Fh	4Fh	(SWCBAHR, SWCBALR+1)	Reserved

Note 1: SWCBALR should be on boundary = 2, which means bit 0 has to be 0.
Note 2: Only use BADDR1-0=10b if the port pair is not 2Eh/2Fh or 4Eh/4Fh.

The host interface registers for Logic Device Control are listed below. The base address can be configured via the following Plug and Play Configuration Registers. Note that if a logical device is activated but with base address equal to 0000h, the host side cannot access this logical device since 0000h means I/O address range is disabled.

Table 6-7. Host View Register Map, Logical Devices

7 0	I/O Port Address
Serial Port 1 (UART1)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 16 Legacy Address = 03F8h
Serial Port 2 (UART2)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 16 Legacy Address = 02F8h
System Wake-Up Control (SWUC)	Depend on PnP SW Used Addr: (IOBAD0+00h,+02h,+06h,+07h,13h,15h) Base address boundary = 32
KBC / Mouse Interface	Unused
KBC / Keyboard Interface	Depend on PnP SW Used Addr: (IOBAD0+00h), (IOBAD1+00h) Base address boundary = none, none Legacy Address = 60h,64h
Consumer IR (CIR)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 8
Shared Memory/Flash Interface (SMFI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+8h,+0Ch) Base address boundary = 16
RTC-like Timer (RTCT)	Depend on PnP SW Used Addr: (IOBAD0+0h,+1h), (IOBAD1+0h,+1h) Used Addr: (IOBAD2+0h,+1h), (IOBAD3+0h,+1h) Used Addr: (IOBAD4+0h,+1h) Base address boundary = 2,2 Legacy Address = 70h-71h,272h-273h

7 0	I/O Port Address
Power Management I/F Channel 1 (PMC1)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 62h,66h
Power Management I/F Channel 2 (PMC2)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 68h,6Ch
Power Management I/F Channel 3 (PMC3)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 6Ah,6Eh
Power Management I/F Channel 4 (PMC4)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 74h,78h
Power Management I/F Channel 5 (PMC5)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 7Ah,7Ch
Serial Peripheral Interface (SSPI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+03h) Base address boundary = 4
Platform Environment Control Interface (PECI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 8

Note: The boundary number means the address has to be the multiple of this number.

The host interface registers for Standard Plug and Play Configuration of PNPCFG are listed below. These registers are accessed via the Index-Data I/O ports defined in Table 6-7 on page 72. They are divided into two parts, Super I/O Configuration Registers and Logical Device Registers.

Table 6-8. Host View Register Map via Index-Data I/O Pair, Standard Plug and Play Configuration Registers

	7 — Register Name — 0	Index
Super I/O Configuration Registers	Logical Device Number (LDN)	07h
	Chip ID Byte 1(CHIPID1)	20h
	Chip ID Byte 2(CHIPID2)	21h
	Chip Version (CHIPVER)	22h
	Super I/O Control (SIOCTRL)	23h
	Reserved	24h
	Super I/O IRQ Configuration (SIOIRQ)	25h
	Super I/O General Purpose (SIOGP)	26h
	Reserved	27h
	Reserved	28h
	Reserved	29h
	Reserved	2Ah
	Reserved	2Bh
	Super I/O Power Mode (SIOPWR)	2Dh
	Depth 2 I/O Address (D2ADR)	2Eh
	Depth 2 I/O Data (D2DAT)	2Fh
Logical Device Configuration Registers Selected by LDN Register	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	DMA Channel Select 0 (DMAS0)	74h
	DMA Channel Select 1 (DMAS1)	75h
	Device Specific Logical Device Configuration 1 to 10	F0h-F9h

The IRQ numbers for Logic Device IRQ via LPC/SERIRQ are listed below. The IRQ numbers can be configured via the above Plug and Play Configuration Registers.

Table 6-9. Interrupt Request (IRQ) Number Assignment, Logical Device IRQ via SERIRQ

Logical Device	IRQ number
Serial Port 1 (UART1)	Depend on PnP SW, Legacy IRQ Num=04
Serial Port 2 (UART2)	Depend on PnP SW, Legacy IRQ Num=03
System Wake-Up Control (SWUC)	Depend on PnP SW
KBC / Mouse Interface	Depend on PnP SW, Legacy IRQ Num=12
KBC / Keyboard Interface	Depend on PnP SW, Legacy IRQ Num=01
Consumer IR (CIR)	Depend on PnP SW
Shared Memory/Flash Interface (SMFI)	Unused
RTC-like Timer (RTCT)	Depend on PnP SW, Legacy IRQ Num=08
Power Management I/F Channel 1 (PMC1)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 2 (PMC2)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 3 (PMC3)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 4 (PMC4)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 5 (PMC5)	Depend on PnP SW, Legacy IRQ Num=01
Serial Peripheral Interface (SSPI)	Depend on PnP SW
Platform Environment Control Interface (PECI)	Unused

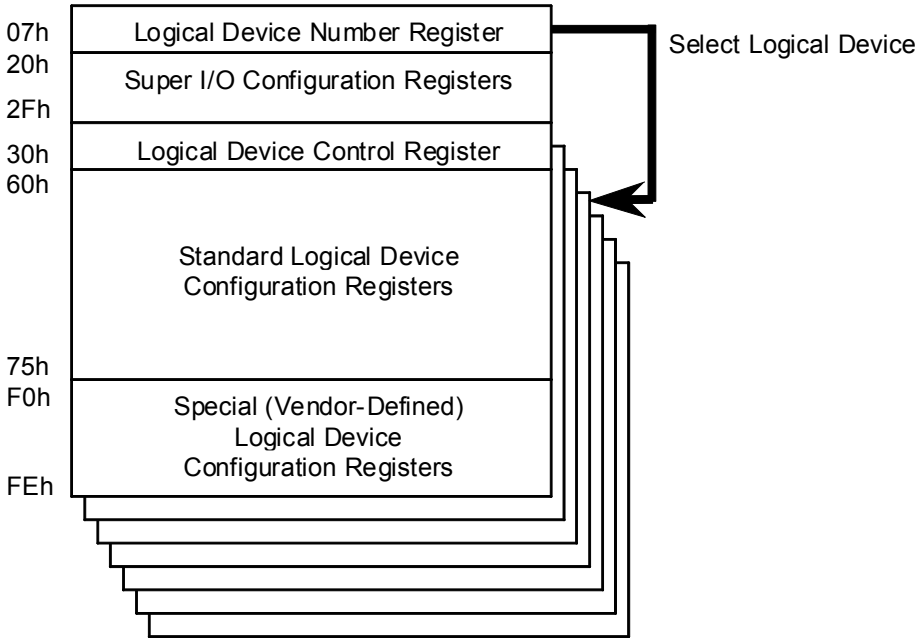
6.3.1 Logical Device Assignment

Table 6-10. Logical Device Number (LDN) Assignments

LDN	Functional Block
01h	Serial Port 1 (UART1)
02h	Serial Port 2 (UART2)
04h	System Wake-Up Control (SWUC)
05h	KBC/Mouse Interface
06h	KBC/Keyboard Interface
0Ah	Consumer IR (CIR)
0Fh	Shared Memory/Flash Interface (SMFI)
10h	RTC-like Timer (RTCT)
11h	Power Management I/F Channel 1 (PMC1)
12h	Power Management I/F Channel 2 (PMC2)
13h	Serial Peripheral Interface (SSPI)
14h	Platform Environment Control Interface (PECI)
17h	Power Management I/F Channel 3 (PMC3)
18h	Power Management I/F Channel 4 (PMC4)
19h	Power Management I/F Channel 5 (PMC5)

The following figure indicates the PNPCFG registers are combined with Super I/O Configuration Registers and Logical Device Configuration Registers. Logical Device Configuration Registers of a specified Logical Device is accessible only when Logical Device Number Register is filled with corresponding Logical Device Number listed in Table 6-10 on page 75 .

Figure 6-12. Host View Register Map via Index-Data Pair



6.3.2 Super I/O Configuration Registers

Registers with index from 07h to 2Eh contain Super I/O configuration settings.

6.3.2.1 Logical Device Number (LDN)

This register contains general Super I/O configurations.

Index: 07h

Bit	R/W	Default	Description
7-0	R/W	04h	**Logical Device Number (LDN)** This register selects the current logical device. All other values are reserved.

6.3.2.2 Chip ID Byte 1 (CHIPID1)

Index: 20h

Bit	R/W	Default	Description
7-0	R	51h	**Chip ID Byte 1 (CHIPID1)** This register contains the Chip ID byte 1.

6.3.2.3 Chip ID Byte 2 (CHIPID2)

Index: 21h

Bit	R/W	Default	Description
7-0	R	21h	**Chip ID Byte 2 (CHIPID2)** This register contains the Chip ID byte 2.

6.3.2.4 Chip Version (CHIPVER)

This register contains revision ID of this chip

Index: 22h

Bit	R/W	Default	Description
7-0	R	02h	**Chip Version (CHIPVER)**

6.3.2.5 Super I/O Control Register (SIOCTRL)

This register contains general Super I/O configurations.

Index: 23h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	W	0b	**Software Reset (SIOSWRST)** Read always returns 0. 0: No action. 1: Software Reset the logical devices.
0	R/W	1b	**Super I/O Enable (SIOEN)** 0: All Super I/O logical devices are disabled except SWUC and SMFI. 1: Each Super I/O logical device is enabled according to its Activate register. (Index 30h)

6.3.2.6 Super I/O IRQ Configuration Register (SIOIRQ)

This register contains general Super I/O configurations.

Index: 25h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0b	**SMI# to IRQ2 Enable (SMI2IRQ2)** This bit enables using IRQ number 2 in the SERIRQ protocol as a SMI# interrupt. This bit is similar to LDACT bit in LDA register. 0: Disable 1: Enable
3-0	-	0h	**Reserved**

6.3.2.7 Super I/O General Purpose Register (SIOGP)

This register contains general Super I/O configurations.

Index: 26h

Bit	R/W	Default	Description
7	R/W	0b	**SIOGP Software Lock (SC6SLK)** 0: GPSCR can be cleared by both Hardware and Software reset. (SIOSWRST). 1: GPSCR can only be cleared by Hardware reset.
6-5	R/W	00b	**General-Purpose Scratch (GPSCR)** Reading returns the value that was previously written. Note that the EC side can access whole PNPCFG registers via EC2I.
4	R/W	0h	**RTCT Disabled (RTCTDE)** 0: RTCT is enabled according to its Activate register and SIOEN bit in SIOCTRL register. 1: Disabled
3-0	-	0h	**Reserved**

6.3.2.8 Super I/O Power Mode Register (SIOPWR)

See also 6.5.5.2.

Index: 2Dh

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	0b	**Power Supply Off (PWRSLY)** It indicates the EC side that the host requests to shut down the power in legacy mode. Refer to SCRDPSO bit in SWCTL2 register on page 155 0: No action 1: It indicates power shut down if PWRSLY is Legacy mode. **Note:** It always returns 0 when read.
0	R/W	0h	**Power Button Mode (PWRBTN)** This bit controls the power button mode in the SWUC. Refer to SCRDPBM bit in SWCTL2 register on page 155 0: Legacy 1: ACPI

6.3.2.9 Depth 2 I/O Address (D2ADR)

For the address/data pair (a.k.a. index/data pair) listed in Table 6-6. Host View Register Map, PNPCFG on page 72, there are two registers to create a sub address space containing 256 addresses, and its depth is 1.

In addition, there are two registers (D2ADR and D2DAT) to create a further sub address, and its depth is 2.

In the depth 2 address space, there are following three registers.
Offset 10h: I2EC_ADDR_L
Offset 11h: I2EC_ADDR_H
Offset 12h: I2EC_DATA

Index: 2Eh

Bit	R/W	Default	Description
7-0	R/W	-	**D2ADR**

6.3.2.10 Depth 2 I/O Data (D2DAT)

Index: 2Fh

Bit	R/W	Default	Description
7-0	R/W	-	**D2DAT**

6.3.3 Standard Logical Device Configuration Registers

Registers with index from 30h to F9h contain Logical Device configuration settings. LDN of the wanted logical device should be written to LDN register before accessing these registers.
This section lists a standard description of these registers. Some default values for each register and more detailed information for each logical device should be referred in each section.

6.3.3.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-1	-	0h	**Reserved**
0	R/W	0b	**Logical Device Activation Control (LDACT)** 0: Disable The registers (Index 60h-FEh) are not accessible. Refer to SIOEN bit in SIOCTRL 1: Enable

6.3.3.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 0.

6.3.3.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 0.

6.3.3.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 1.

6.3.3.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 1.

6.3.3.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register will be read-only if it is unused by a logical device.

Index: 70h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0	**Wake-Up IRQ Enable (WKIRQEN)** Allow this logical device to trigger a wake-up event to SWUC. This bit should not be set in SWUC Logical Device since it is used to collect IRQ sources for SWUC. 0: Disable 1: Enable
3-0	R/W	Depend on Logical Device	**IRQ Number (IRQNUM)** Select the IRQ number (level) asserted by this logical device via SERIRQ. 00d: This logical device doesn't use IRQ. 01d-012d: IRQ1-12 are selected correspondingly. 14d-15d: IRQ14-15 are selected correspondingly. Otherwise: Invalid IRQ routing configuration.

6.3.3.7 Interrupt Request Type Select (IRQTP)

This register will be read-only if it is unused by a logical device.

Index: 71h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	Depend on Logical Device	**Interrupt Request Polarity Select (IRQPS)** This bit indicates the polarity of the interrupt request. 0: IRQ request is buffered and applied on SERIRQ. 1: IRQ request is inverted before being applied on SERIRQ. This bit should be configured before the logical device is activated.
0	R/W	Depend on Logical Device	**Interrupt Request Triggered Mode Select (IRQTMS)** This bit indicates that edge or level triggered mode is used by this logical device and should be updated by EC firmware via EC2I since the triggered mode is configured in EC side registers. This bit is just read as previously written (scratch register bit) and doesn't affect SERIRQ operation. 0: edge triggered mode 1: level triggered mode

6.3.3.8 DMA Channel Select 0 (DMAS0)

Index: 74h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 0** A value of 4 indicates that no DMA channel is active.

6.3.3.9 DMA Channel Select 1 (DMAS1)

Index: 75h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 1** A value of 4 indicates that no DMA channel is active.

6.3.4 Serial Port 1 (UART1) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-11. Host View Register Map via Index-Data I/O Pair, UART1 Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	High Speed Baud Rate Select (HHS)	F0h

6.3.4.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.4.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.3.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.3.4.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	F8h	**Refer to section 6.3.3.3 on page 79.** Bit 3-0 (IOBAD0[3:0]) are forced to 8h and can't be written. It means the base address is on the 16-byte boundary.

6.3.4.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.4.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.4.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	04h	**Refer to section 6.3.3.6 on page 80.**

6.3.4.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.3.7 on page 81.**

6.3.4.8 High Speed Baud Rate Select (HHS)

Index: F0h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**High Speed Baud Rate Select (HHS)** This bit indicates that the baud rate of UART1 can be up to 230.4K/460.8K baud, which are determined by the divisor of the baud rate generator. (From Host Side) 0: Not selected 1: Selected
0	-	0b	**Reserved**

6.3.5 Serial Port 2 (UART2) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-12. Host View Register Map via Index-Data I/O Pair, UART2 Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	High Speed Baud Rate Select (HHS)	F0h

6.3.5.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.5.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.3.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.3.5.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	F8h	**Refer to section 6.3.3.3 on page 79.** Bit 3-0 (IOBAD0[3:0]) are forced to 8h and can't be written. It means the base address is on the 16-byte boundary.

6.3.5.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.5.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.5.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.3.6 on page 80.**

6.3.5.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.3.7 on page 81.**

6.3.5.8 High Speed Baud Rate Select (HHS)

Index: F0h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**High Speed Baud Rate Select (HHS)** This bit indicates that the baud rate of UART2 can be up to 230.4K/460.8K baud, which are determined by the divisor of the baud rate generator. (From Host Side) 0: Not selected 1: Selected
0	-	0b	**Reserved**

6.3.6 System Wake-Up Control (SWUC) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-13. Host View Register Map via Index-Data I/O Pair, SWUC Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.6.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.6.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.**

6.3.6.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.3 on page 79.** Bits 4-0 (IOBAD0[4:0]) are forced to 00000b and can't be written. It means the base address is on the 32-byte boundary.

6.3.6.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.6.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.6.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.6 on page 80.**

6.3.6.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.7 KBC / Mouse Interface Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-14. Host View Register Map via Index-Data I/O Pair, KBC / Mouse Interface Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8]) – Unused	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0]) –Unused	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8]) – Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) –Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.7.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.7.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register is unused and read-only.

Index: 60h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.2 on page 79.**

6.3.7.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register is unused and read-only.

Index: 61h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.3 on page 79.**

6.3.7.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.7.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.7.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	0Ch	**Refer to section 6.3.3.6 on page 80.**

6.3.7.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.8 KBC / Keyboard Interface Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-15. Host View Register Map via Index-Data I/O Pair, KBC / Keyboard Interface Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.8.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.8.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.8.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	60h	**Refer to section 6.3.3.3 on page 79.**

6.3.8.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.8.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	64h	**Refer to section 6.3.3.5 on page 80.**

6.3.8.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.6 on page 80.**

6.3.8.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.9 Consumer IR Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-16. Host View Register Map via Index-Data I/O Pair, Consumer IR Interface Logical Device

7 0 Index

	Register Name	
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.9.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.9.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.3.2 on page 79.**

6.3.9.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	10h	**Refer to section 6.3.3.3 on page 79.** Bit 2-0 (IOBAD0[2:0]) are forced to 000b and can't be written.

6.3.9.4 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.6 on page 80.**

6.3.9.5 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R	02h	**Refer to section 6.3.3.7 on page 81.**

6.3.10 Shared Memory/Flash Interface (SMFI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-17. Host View Register Map via Index-Data I/O Pair, SMFI Interface Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])-Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	LPC Memory Window Base Address [31:24] (LPCMWBA)	F0h
	LPC Memory Window Base Address [23:16] (LPCMWBA)	F1h
	LPC Memory Window Mapping Region Select (LPCMWMRS)	F2h
	LPC Memory Window Control Register (LPCMWCR)	F3h
	Shared Memory Configuration Register (SHMC)	F4h
	H2RAM-HLPC Base Address [15:12] (HLPCRAMBA[15:12])	F5h
	H2RAM-HLPC Base Address [23:16] (HLPCRAMBA[23:16])	F6h
	H2RAM Host Semaphore Interrupt Enable (H2RAMHSIE)	F9h
	H2RAM Host Semaphore Address (H2RAMHSA)	FAh
	H2RAM EC Semaphore Status (H2RAMECSS)	FBh
	H2RAM-HLPC Base Address [24] (HLPCRAMBA[24])	FCh

6.3.10.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.10.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.**

6.3.10.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.3 on page 79.** Bits 3-0 (IOBAD0[3:0]) are forced to 0000b and can't be written. It means the base address is on the 16-byte boundary.

6.3.10.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.10.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.10.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.6 on page 80.**

6.3.10.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.3.7 on page 81.**

6.3.10.8 LPC Memory Window Base Address [31:24] (LPCMWBA[31:24])

The base address of LPC memory window should not overlap with legacy BIOS range, extended legacy BIOS range and HLPCRAMBA.

Index: F0h

Bit	R/W	Default	Description
7-0	R/W	00h	**LPC Memory Window Base Address [31:24] (LPCMWBA[31:24])** Specify the base address of the user-defined 64K window on LPC memory space for PCH LGMR application.

6.3.10.9 LPC Memory Window Base Address [23:16] (LPCMWBA[23:16])

Index: F1h

Bit	R/W	Default	Description
7-0	R/W	00h	**LPC Memory Window Base Address [23:16] (LPCMWBA[23:16])** Specify the base address of the user-defined 64K window on LPC memory space for PCH LGMR application.

6.3.10.10 LPC Memory Window Mapping Region Select (LPCMWMRS)

Index: F2h

Bit	R/W	Default	Description
7-0	R/W	00h	**LPC Memory Window Mapping Region Select (LPCMWMRS)** The LPC memory window is mapped into the region that ranges from (10000_0000h – flash size + 64K*LPCMWMRS) to (FFFF_FFFFh – flash size + 64K*(LPCMWMRS + 1)) on LPC memory space. The flash size is specified by FMSS.

6.3.10.11 LPC Memory Window Control Register (LPCMWCR)

Index: F3h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**LPC Memory Window Enable (LPCMWE)** 0b: Disable 1b: The address located in the user-defined LPC memory window of LPC memory space is mapped into the region of flash address space, which is defined by LPCMWMRS.

6.3.10.12 Shared Memory Configuration Register (SHMC)

Index: F4h

Bit	R/W	Default	Description
7-4	R/W	0h	**BIOS FWH ID (FWHID)** These bits correspond to the 4-bit ID which is part of a FWH transaction.
3	-	-	**Reserved**
2	-	-	**Reserved**
1	R/W	0b	**BIOS Extended Space Enable (BIOSEXTS)** This bit expands the BIOS address space to make this chip respond the Extended BIOS address range.
0	-	-	**Reserved**

6.3.10.13 H2RAM-HLPC Base Address [15:12] (HLPCRAMBA[15:12])

The H2RAM-HLPC base address is only within the range: FXXX_X000h. (X denotes it's programmable by registers).
Use H2RAM-HLPC Base Address [24] to decide the decode Range FEXX_X000h or FFXX_X000h.

The H2RAM-HLPC function will be disabled if SPI follow mode is enabled.

Index: F5h

Bit	R/W	Default	Description
7-4	R/W	0h	**H2RAM-HLPC Base Address Bits [15:12] (HLPCRAMBA[15:12])** If H2RAMPS is set to 0, this field defines EC internal RAM base address on LPC memory space. If H2RAMPS is set to 1, this field defines EC internal RAM base address on LPC IO space.
3-0	-	-	**Reserved**

6.3.10.14 H2RAM-HLPC Base Address [23:16] (HLPCRAMBA[23:16])

Index: F6h

Bit	R/W	Default	Description
7-0	R/W	00h	**H2RAM-HLPC Base Address Bits [23:16] (HLPCRAMBA[23:16])** If H2RAMPS is set to 0, this field defines EC internal RAM base address on LPC memory space. If H2RAMPS is set to 1, write 1b to HLPCRAMBA[16] to enable H2RAM LPC IO-path.

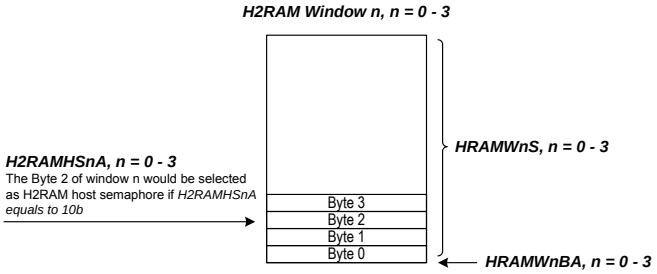
6.3.10.15 H2RAM Host Semaphore Interrupt Enable (H2RAMHSIE)

Address Offset: F9h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**H2RAM Host Semaphore 3 Interrupt Enable (H2RAMHS3IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 3 will produce an interrupt (INT83) to EC.
2	R/W	0b	**H2RAM Host Semaphore 2 Interrupt Enable (H2RAMHS2IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 2 will produce an interrupt (INT83) to EC.
1	R/W	0b	**H2RAM Host Semaphore 1 Interrupt Enable (H2RAMHS1IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 1 will produce an interrupt (INT83) to EC.
0	R/W	0b	**H2RAM Host Semaphore 0 Interrupt Enable (H2RAMHS0IE)** 0b: Disable 1b: A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore 0 will produce an interrupt (INT83) to EC.

6.3.10.16 H2RAM Host Semaphore Address (H2RAMHSA)

Figure 6-13. Location of H2RAM Host Semaphore



Address Offset: FAh

Bit	R/W	Default	Description
7-6	R/W	00b	**H2RAM Host Semaphore 3 Address (H2RAMHS3A)** 00b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 0) 01b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 1) 10b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 2) 11b: H2RAM host semaphore 3 locates at (HRAMW3BA[11:0] + 3) This field is available only when H2RAM window 3 is enabled.
5-4	R/W	00b	**H2RAM Host Semaphore 2 Address (H2RAMHS2A)** 00b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 0) 01b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 1) 10b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 2) 11b: H2RAM host semaphore 2 locates at (HRAMW2BA[11:0] + 3) This field is available only when H2RAM window 2 is enabled.
3-2	R/W	00b	**H2RAM Host Semaphore 1 Address (H2RAMHS1A)** 00b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 0) 01b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 1) 10b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 2) 11b: H2RAM host semaphore 1 locates at (HRAMW1BA[11:0] + 3) This field is available only when H2RAM window 1 is enabled.
1-0	R/W	00b	**H2RAM Host Semaphore 0 Address (H2RAMHS0A)** 00b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 0) 01b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 1) 10b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 2) 11b: H2RAM host semaphore 0 locates at (HRAMW0BA[11:0] + 3) This field is available only when H2RAM window 0 is enabled.

6.3.10.17 H2RAM EC Semaphore Status (H2RAMECSS)

The host can know H2RAM EC semaphore status by reading this register.

Address Offset: FBh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	0b	**H2RAM EC Semaphore 3 Status (H2RAMECS3S)** This bit is automatically set to 1b while H2RAM EC semaphore 3 is written. 0b: H2RAM EC semaphore 3 is not written. 1b: H2RAM EC semaphore 3 is written. Writing 1 to clear this bit.
2	R/WC	0b	**H2RAM EC Semaphore 2 Status (H2RAMECS2S)** This bit is automatically set to 1b while H2RAM EC semaphore 2 is written. 0b: H2RAM EC semaphore 2 is not written. 1b: H2RAM EC semaphore 2 is written. Writing 1 to clear this bit.
1	R/WC	0b	**H2RAM EC Semaphore 1 Status (H2RAMECS1S)** This bit is automatically set to 1b while H2RAM EC semaphore 1 is written. 0b: H2RAM EC semaphore 1 is not written. 1b: H2RAM EC semaphore 1 is written. Writing 1 to clear this bit.
0	R/WC	0b	**H2RAM EC Semaphore 0 Status (H2RAMECS0S)** This bit is automatically set to 1b while H2RAM EC semaphore 0 is written. 0b: H2RAM EC semaphore 0 is not written. 1b: H2RAM EC semaphore 0 is written. Writing 1 to clear this bit.

6.3.10.18 H2RAM-HLPC Base Address [24] (HLPCRAMBA[24])

Index: FCh

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	1b	**H2RAM-HLPC Base Address Bits [24] (HLPCRAMBA[24])** 0b: This field only defines EC decode Range FEXX_X000h on LPC memory space. 1b: This field only defines EC decode Range FFXX_X000h on LPC memory space.

6.3.11 RTC-like Timer Configuration Registers

This section lists the default value for each register and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-18. Host View Register Map via Index-Data I/O Pair, RTCT Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD1[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])	64h
	I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])	65h
	I/O Port Base Address Bits [15:8] for Descriptor 3 (IOBAD3[15:8])	66h
	I/O Port Base Address Bits [7:0] for Descriptor 3 (IOBAD3[7:0])	67h
	I/O Port Base Address Bits [15:8] for Descriptor 4 (IOBAD4[15:8])	68h
	I/O Port Base Address Bits [7:0] for Descriptor 4 (IOBAD4[7:0])	69h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX) –Unused	70h
	Interrupt Request Type Select (IRQTP) –Unused	71h
	RAM Lock Register (RLR)	F0h
	Data of Month Alarm Register Offset (DOMAO)	F1h
	Month Alarm Register Offset (MONAO)	F2h
	P80L Begin Index (P80LB)	F3h
	P80L End Index (P80LE)	F4h
	P80L Current Index (P80LC)	F5h

6.3.11.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.** Refer to SIOEN bit in SIOCTRL and SIOEN bit in SIOCTRL Register.

6.3.11.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.**

6.3.11.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	70h	**Refer to section 6.3.3.3 on page 79.** Bit 0 (IOBAD0[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.3.11.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.3.4 on page 80.**

6.3.11.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	72h	**Refer to section 6.3.3.5 on page 80.** Bit 0 (IOBAD1[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.3.11.6 I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])

Index: 64h

Bit	R/W	Default	Description
7-0	R/W	0h	**Refer to section 6.3.3.4 on page 80.**

6.3.11.7 I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])

Index: 65h

Bit	R/W	Default	Description
7-0	R/W	0h	**Refer to section 6.3.3.5 on page 80.** Bit 0 (IOBAD2[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.3.11.8 I/O Port Base Address Bits [15:8] for Descriptor 3 (IOBAD3[15:8])

Index: 66h

Bit	R/W	Default	Description
7-0	R/W	0h	**Refer to section 6.3.3.4 on page 80.**

6.3.11.9 I/O Port Base Address Bits [7:0] for Descriptor 3 (IOBAD3[7:0])

Index: 67h

Bit	R/W	Default	Description
7-0	R/W	0h	**Refer to section 6.3.3.5 on page 80.** Bit 0 (IOBAD3[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.3.11.10 I/O Port Base Address Bits [15:8] for Descriptor 4 (IOBAD4[15:8])

Index: 68h

Bit	R/W	Default	Description
7-0	R/W	0h	**Refer to section 6.3.3.4 on page 80.**

6.3.11.11 I/O Port Base Address Bits [7:0] for Descriptor 4 (IOBAD4[7:0])

Index: 69h

Bit	R/W	Default	Description
7-0	R/W	0h	**Refer to section 6.3.3.5 on page 80.** Bit 0 (IOBAD4[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.3.11.12 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R	08h	**Refer to section 6.3.3.6 on page 80.**

6.3.11.13 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.11.14 RAM Lock Register (RLR)

Index: F0h

Bit	R/W	Default	Description
7	R/W	0b	**Block Standard RAM R/W (BSRW)** 0: R/W to 38h-3Fh of the Standard RAM is allowed. 1: Not allowed. Writes are ignored and reads return FFh.
6	R/W	0b	**Block RAM Write (BW)** 0: Write to Standard and Extended RAM is allowed. 1: Not allowed. Writes are ignored.
5	R/W	0b	**Block Extended RAM Write (BEW)** 0: Write to bytes 00h-1Fh of the Extended RAM is allowed. 1: Not allowed. Writes are ignored.
4	R/W	0b	**Block Extended RAM Read (BER)** 0: Read from bytes 00h-1Fh of the Extended RAM is allowed. 1: Not allowed. Reads return FFh.
3	R/W	0b	**Block Extended RAM R/W (BERW)** 0: R/W to the Extended RAM 128 bytes is allowed. 1: Not allowed. Writes are ignored and reads return FFh
2-0	-	0h	**Reserved**

6.3.11.15 Date of Month Alarm Register Offset (DOMAO)

Index: F1h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	49h	**Date of Month Alarm Register Offset (DOMAO)** It contains the index offset of "date of month alarm".

6.3.11.16 Month Alarm Register Offset (MONAO)

Index: F2h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	4Ah	**Month Alarm Register Offset (MONAO)** It contains the index offset of “month alarm”.

6.3.11.17 P80L Begin Index (P80LB)

Index: F3h

Bit	R/W	Default	Description
7	R/W	0b	**Host RTCT RAM Only (HRTCRAM)** If HRTCRAM or ECRTCRAM is one, Index 80h-FFh in RTCT Bank 0/1 is RAM bytes. Otherwise, Bit 7 of index in RTCT Bank 0/1 is not decoded.
6	-	-	**Reserved**
5-0	R/W	-	**P80L Begin Index (P80LBI)** It indicates the P80L queue begins in BRAM Bank 1. Refer to section 7.19.3.1 P80L on page 460

6.3.11.18 P80L End Index (P80LE)

Index: F4h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R/W	-	**P80L End Index (P80LEI)** It indicates the P80L queue ends in BRAM Bank 1. Refer to section 7.19.3.1 P80L on page 460

6.3.11.19 P80L Current Index (P80LC)

Index: F5h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R	-	**P80L Current Index (P80LC)** It indicates the P80L queue current in BRAM Bank 1. Refer to section 7.19.3.1 P80L on page 460

6.3.12 Power Management I/F Channel 1 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-19. Host View Register Map via Index-Data I/O, PMC1 Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.12.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.12.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.12.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	62h	**Refer to section 6.3.3.3 on page 79.**

6.3.12.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.12.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	66h	**Refer to section 6.3.3.5 on page 80.**

6.3.12.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
3-0	R/W	01h	**Refer to section 6.3.3.6 on page 80.**

6.3.12.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-2	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.13 Power Management I/F Channel 2 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-20. Host View Register Map via Index-Data I/O, PMC2 Logical Device

7 0

	Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])	64h
	I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])	65h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	General Purpose Interrupt (GPINTR)	F0h

6.3.13.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.13.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.13.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	68h	**Refer to section 6.3.3.3 on page 79.**

6.3.13.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.13.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Ch	**Refer to section 6.3.3.5 on page 80.**

6.3.13.6 I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])

It contains Command/Status Register Base Address Register.

Index: 64h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.13.7 I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])

It contains Command/Status Register Base Address Register.

Index: 65h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.5 on page 80.** Bits 3-0 (IOBAD2[3:0]) are forced to 0000b and can't be written.

6.3.13.8 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.6 on page 80.**

6.3.13.9 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.13.10 General Purpose Interrupt (GPINTR)

Index: F0h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	W	-	**General Purpose Interrupt 3 (GPINT3)** Writing 1 to this bit will issue an interrupt to INT35.
2	W	-	**General Purpose Interrupt 2 (GPINT2)** Writing 1 to this bit will issue an interrupt to INT34.
1	W	-	**General Purpose Interrupt 1 (GPINT1)** Writing 1 to this bit will issue an interrupt to INT33.
0	W	-	**General Purpose Interrupt 0 (GPINT0)** Writing 1 to this bit will issue an interrupt to INT32.

6.3.14 Power Management I/F Channel 3 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-21. Host View Register Map via Index-Data I/O, PMC3 Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.14.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.14.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.** Bit 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.14.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	6Ah	**Refer to section 6.3.3.3 on page 79.**

6.3.14.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.14.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Eh	**Refer to section 6.3.3.5 on page 80.**

6.3.14.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.6 on page 80.**

6.3.14.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.15 Power Management I/F Channel 4 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-22. Host View Register Map via Index-Data I/O, PMC4 Logical Device

	7 … 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.15.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.15.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.** Bit 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.3.15.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	74h	**Refer to section 6.3.3.3 on page 79.**

6.3.15.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.3.15.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	78h	**Refer to section 6.3.3.5 on page 80.**

6.3.15.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.6 on page 80.**

6.3.15.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.16 Power Management I/F Channel 5 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-23. Host View Register Map via Index-Data I/O, PMC5 Logical Device

	7 Register Name 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.16.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.16.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.3.16.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	7Ah	**Refer to section 6.3.3.3 on page 79.**

6.3.16.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.4 on page 80.** Bits 7-4 (IOBAD1[15:12]) are forced to 0000b and can't be written.

6.3.16.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	7Ch	**Refer to section 6.3.3.5 on page 80.**

6.3.16.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.6 on page 80.**

6.3.16.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.3.3.7 on page 81.**

6.3.17 Serial Peripheral Interface (SSPI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-24. Host View Register Map via Index-Data I/O Pair, SSPI Logical Device

	7 — Register Name — 0	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.3.17.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.17.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.3.3.2 on page 79.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't written.

6.3.17.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.3 on page 79.** Bit 1-0 (IOBAD0[1:0]) are forced to 00b and can't be written. It means the base address is on the 4-byte boundary.

6.3.17.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.17.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.17.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.6 on page 80.**

6.3.17.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.3.3.7 on page 81.**

6.3.18 Platform Environment Control Interface (PECI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-25. Host View Register Map via Index-Data I/O Pair, PECI Interface Logical Device

	7 … 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])-Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX) – Unused	70h
	Interrupt Request Type Select (IRQTP) -Unused	71h

6.3.18.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.1 on page 79.**

6.3.18.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.2 on page 79.**

6.3.18.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.3.3.3 on page 79.** Bits 2-0 (IOBAD0[2:0]) are forced to 000b and can't be written. It means the base address is on the 8-byte boundary.

6.3.18.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.4 on page 80.**

6.3.18.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.5 on page 80.**

6.3.18.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register is unused and read-only.

Index: 70h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.6 on page 80.**

6.3.18.7 Interrupt Request Type Select (IRQTP)

This register is unused and read-only.

Index: 71h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.3.3.7 on page 81.**

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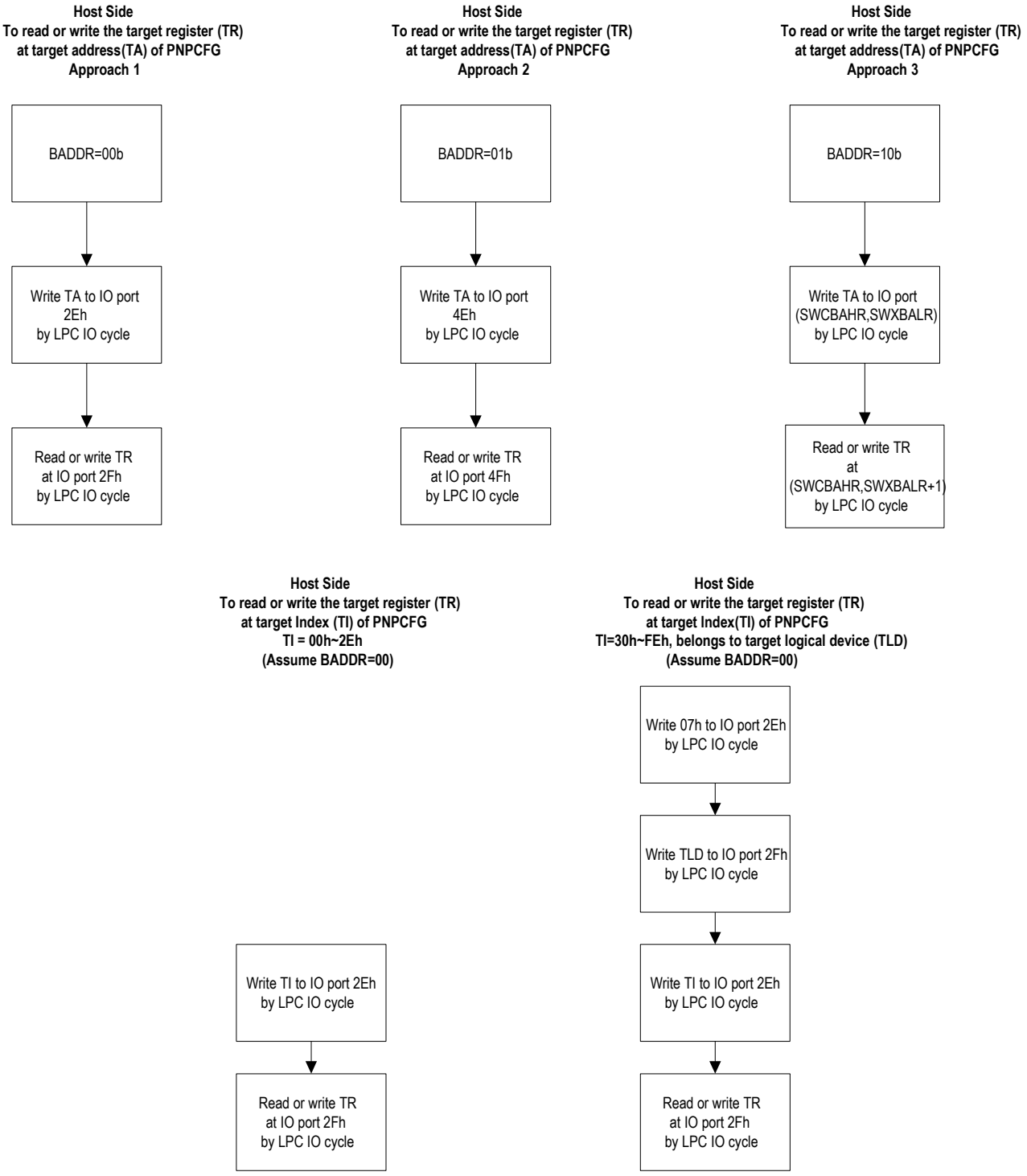
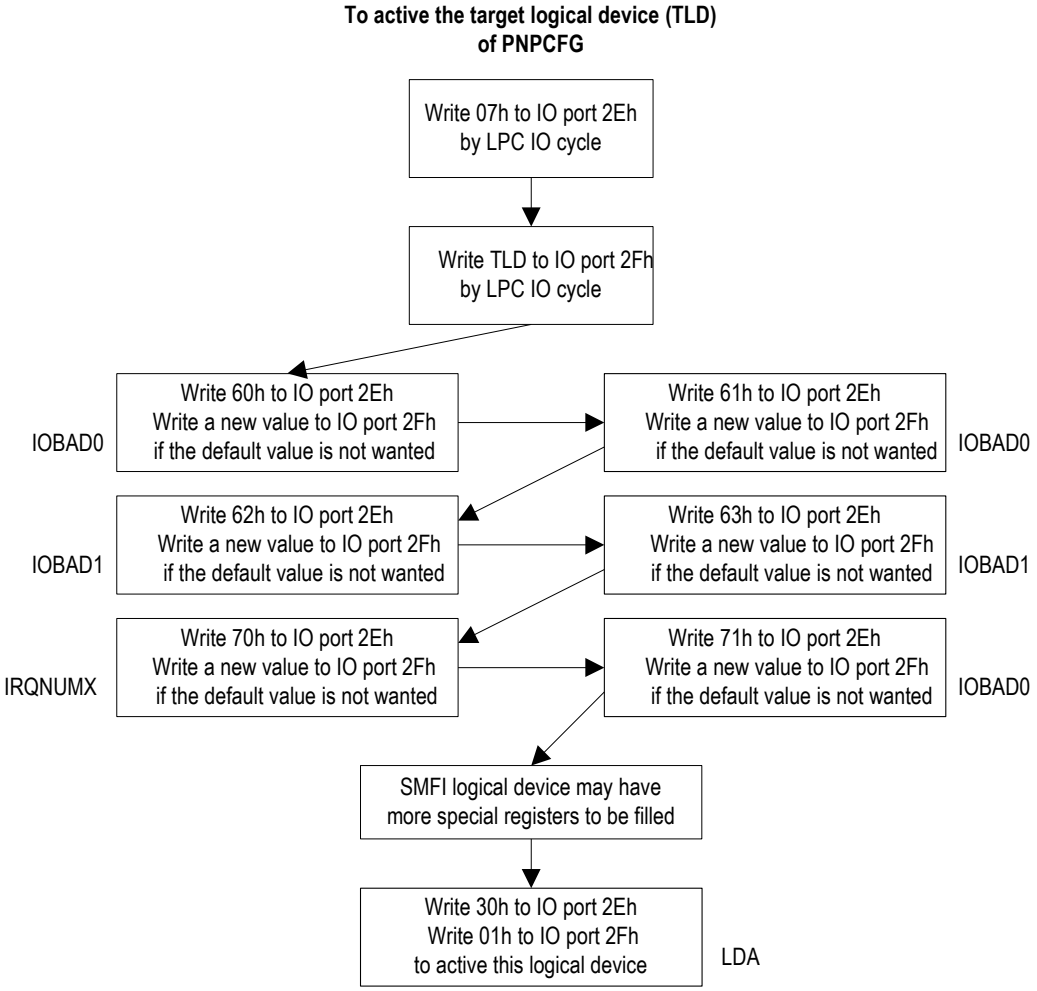


Figure 6-14. Program Flow Chart for PNPCFG



Note: To enable an interrupt to host side through SERIRQ, the firmware enables it in registers at PNPCFG and relative registers in EC side.

See also section 7.15.5 on page 429 for accessing PNPCFG through EC2I.

6.4 Shared Memory Flash Interface Bridge (SMFI)

6.4.1 Overview

The bridge provides the host to access the shared memory. It also provides EC code address space mapped into the host domain address space, and locking mechanism for read/write protection.

6.4.2 Features

- Behaves as a LPC/FWH memory device (HLPC)
- Supports memory mapping between host domain and EC domain
- Supports read/write(program/erase) flash operations and protection mechanism
- Supports two shared memory access paths: host and EC
- Supports 128KB/196KB/256KB e-flash

6.4.3 Function Description

6.4.3.1 Supported Interface

IT5121/SMFI can behave as a LPC/FWH memory device on LPC bus connected to the host Southbridge and this function is abbreviated as HLPC.

6.4.3.2 Supported Flash

- 128KB/196KB/256KB e-flash

6.4.3.3 HLPC: Host Translation

The SMFI provides an HLPC interface between the host bus and the M bus. The flash is mapped into the host memory address space for host accesses. The flash is also mapped into the EC memory address space for EC accesses.
An M bus transaction is generated by the host bus translations and has the following three types:

- 8-bit LPC Memory Read/Write
- 8-bit FWH Read/Write
- 8-bit Host-Indirect Memory Read/Write

After the LPC address translation is done, the host memory transaction is forwarded to M-bus (flash interface) if it is accessing an unprotected region. The host side can't issue a write transaction until the firmware write 1 to HOSTWA bit SMECCS register.

6.4.3.4 EC-Indirect Memory Read/Write Transaction

The firmware code to issue EC-Indirect Memory cycle should be executed within Scratch ROM.
This kind of access is useful to

1. Read flash ID for EC BIOS.
2. Customize user-defined flash programming interface.
3. Put extra BIOS data outside EC 64K.

- **EC-Indirect Memory Address Registers (ECINDAR3-0)**

Stand for flash address bit 31 to 0.

- **EC-Indirect Memory Data Register (ECINDDR)**

Stand for read or write data bit 7 to 0.

- **EC-Indirect Read Mode**

The EC firmware can read the flash byte located at the flash address combined by ECINDAR2-0 from

ECINDDR when ECINDAR3 is 00h.

- **EC-Indirect Follow Mode**

For serial flash, another mode to access whole flash is performed by EC-Indirect Follow Mode.

EC-Indirect Follow Mode is enabled after
1. Writing 0Fh to ECINDAR3 register.

EC-Indirect Follow Mode is disabled after
1. Writing 00h to ECINDAR3 register.

In EC-Indirect Follow Mode, for access serial flash
1. Writing 00h to EC-Indirect Memory Address FFFF_FExxh generates FSCE# with high level.
2. Writing data to EC-Indirect Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. Reading data from EC-Indirect Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. All of the above actions are clocked by 8 FSCK clock-ticks and FSCK is stopped in other cases.

In EC-Indirect Follow Mode, use the EC-Indirect Memory Address(7FFF_FExxh and 7FFF_FDxxh) to access e-flash.

6.4.3.5 Flash Shared between Host and EC Domains

A hardware arbiter handles flash read/write translation between the host and EC side.

- **HLPC**

IT5121 bridges the memory cycles on LPC bus and bridges them to the attached SPI flash.
The SMFI internal flash controller performs interleave mechanism control to let the flash fetch for the host and EC side.

It may responde to Long-Waits on LPC bus or freeze CPU code-fetch due to interleave mechanism.
There is no internal hard-wired mechanism to monitor whether the attached SPI flash is in the WIP (busy) state caused by the WIP instruction from the host. Before the host accesses the e-flash, it is necessary to set the LPC Memory Cycle Target Select bit (LMCTS) or Host Indirect Cycle Target Select (HICTS) at HINSTC2.

When the host wants to erase or program the flash via Follow Mode 0, the signaling interface (Semaphore Write or KBC/PMC extended command such as 62h/66h command) notifies the firmware to write 1 to HOSTWA bit in SMECCS register. EC CPU will fail to code fetch due to the WIP (busy) state caused by erasing/programming so Scratch ROM must be applied. Once the host accessing to the flash is completed, the host should indicate this to the EC, allowing EC to clear HOSTWA bit and resume normal operation. The EC can clear HOSTWA bit at any time, and prevent the host from issuing any erase or program operations.

When the host wants to erase or program the flash via Follow Mode 1, it is not necessary for the firmware to shadow code to the SRAM if the EC code is not modified since there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash. Refer to section 6.4.3.9 HLPC: Serial Flash Programming on page 116 for its description and limitation.

6.4.3.6 Response to a Forbidden Access

A forbidden access is generated by a translated host address which is protected.
HLPC:
The response to the host bus is according to HERES field in SMECCS register.

6.4.3.7 DMA for Scratch SRAM

DMA (Direct Memory Access) is used to shadow flash content of a specified address range inside code space to Scratch SRAM.

To enable DMA operation to Scratch SRAM No. 0, please follow the steps below:
1. Write data to SCAR0H register with wanted SC0A18-16 field and 1 to NSDMA bit.
2. Write data to SCAR0L register with wanted SC0A7-0 field.
3. Write data to SCAR0M register with wanted SC0A15-8 field.
4. Write data to SCAR0H register with wanted SC0A18-16 field and 0 to NSDMA bit.
   DMA operation is started and code space mapping is enabled after DMA operation is finished.

6.4.3.8 HLPC: Flash Programming via Host LPC Interface with Scratch SRAM

When programming flash via HLPC Follow Mode 0 is processing, the flash will be busy and code fetch from flash by CPU and will be invalid and cause CPU fail to execute instructions. It means the firmware must copy necessary instructions from code space to Scratch SRAM, enable mapping Scratch SRAM to Scratch ROM, and jump to Scratch ROM before programming flash.

Flash Programming Steps:
(a) The host side communicates with the EC side via KBC/PMC extended or semaphore registers
(b) EC side: Write 1 to HOSTWA bit in SMECCS register
(c) EC side: Copy necessary code to Scratch RAM
(d) EC side: Enable code space mapping of Scratch SRAM
(e) EC side: Make the host processor enter SMM mode if necessary
(f) EC side: Jump instruction to Scratch ROM
(g) Host side: Set related memory-write registers in South-Bridge
(h) Host side: Start flash programming
(i) End flash programming and reset EC domain if necessary.
    (Refer to section 5.4 on page 25)

Note: Do not let EC enter Doze/Deep Doze/Sleep mode while processing flash programming flow.

6.4.3.9 HLPC: Serial Flash Programming

There is Follow Mode dedicated for serial flash programming through host LPC interface.

There are mode 0 and 1 for Follow Mode and they can not be enabled at the same time.

In mode 0, there is no internal hard-wired mechanism to monitor the WIP (busy) state of the flash.
In mode 1, there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash; however, the utility in the host side is still required to poll the flash status via RDSR instruction.

In mode 0, it's necessay for the firmware to shadow code to the SRAM and stop all flash access to let the HLPC occupies the flash arbiter.
In mode 1, it's not necessay for the firmware to shadow code to the SRAM and HLPC interleaves with other flash access issued by the firmware.

In mode 0, if the hardware protection is disabled, the program in the host side can construct any SPI cycle.
In mode 0, if the hardware protection is enabled, the WIP instructions listed in Table 6-26 are monitored by protection logic.

Table 6-26. SPI Instruction List Monitored by HLPC Follow Mode 0, Protection Enabled

Instruction	Hex Code	Note
Program Data (PROG)	02h	Monitored by protection logic.
AAI Program Byte (AAIB/AAI)	AFh	Monitored by protection logic.
AAI Program Word (AAIW/AAI)	ADh	Monitored by protection logic.
Chip/Bulk Erase (ERASE)	60h,C7h	Inhibited by protection logic.
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h	Monitored by protection logic.
Otherwise	-	Not monitored by protection logic.

In mode 1, only some specified instructions are supported.
If the leading two bytes of JEDEC ID of flash is "BFh 25h","50h 01h" will be sent to the flash before bridging a WIP instruction.

Table 6-27. SPI Instruction List Supported by HLPC Follow Mode 1

Instruction	Hex Code	Note
Program Data (PROG)	02h	Monitored by protection logic. Programming single byte supported. Programming multiple bytes isn't supported.
Read Status (RDSR)	05h	Monitored by protection logic. Reading single status byte supported. Reading multiple status bytes isn't supported.
Chip/Bulk Erase (ERASE)	60h,C7h	Not supported
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h	Monitored by protection logic. Supported
Otherwise	-	Not supported

Follow Mode 0 is enabled after
1. Writing 1 to HOSTWA bit in SMECCS register in the EC side.
2. Writing 00h to LPC/FWH Address FFFF_FExxh in the host side

Follow Mode 0 is disabled after
1. Writing 0 to HOSTWA bit in SMECCS register in the EC side.

Follow Mode 1 is enabled after
1. Writing 1 to HFW1EN bit in HCTRL2R register in the EC side.
2. Writing 00h to LPC/FWH Address FFFF_FExxh in the host side

3. Write 1 to ACP80 bit in SPCTRL1 register to enable LPC_IO-to-FSPI function.

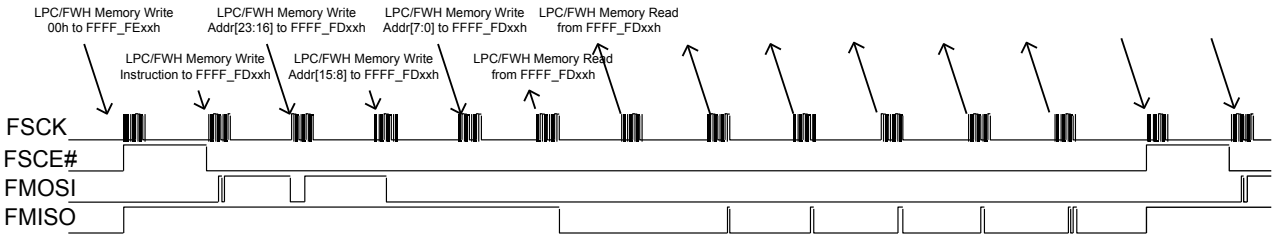
Follow Mode 1 is disabled after

1. Writing 0 to HFW1EN bit in HCTRL2R register in the EC side.

In HLPC Follow Mode,

1. Writing 00h to LPC/FWH Memory Address FFFF_FExxh generates FSCE# with high level.
2. Writing data to LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. Reading data from LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. All the above actions are clocked by 8 FSCK clock ticks and FSCK is stopped in other cases.

Figure 6-15. HLPC Follow Mode for Serial Flash (e.g. Fast Read Instruction)



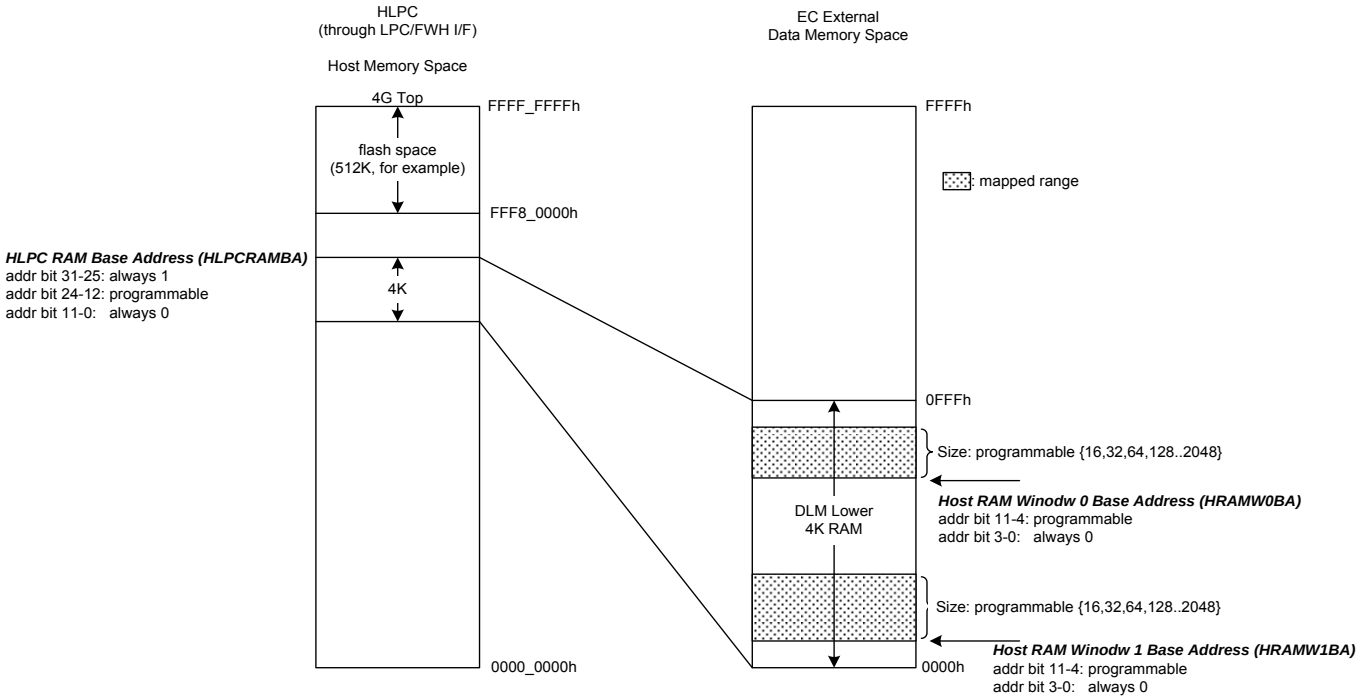
6.4.3.10 Host Side to EC DLM Lower 4K RAM (H2RAM)

6.4.3.10.1 HLPC to EC DLM Lower 4K RAM (H2RAM-HLPC) through LPC Memory/FWH Cycles

- H2RAM can be used by the host side software to access DLM lower 4K RAM through LPC Memory/FWH cycles.
- The read/write protection mechanism is also supported by this function.
- H2RAM isn't available through Host-Indirect Memory path.

Figure 6-16. H2RAM-HLPC Mapping through LPC Memory/FWH Cycles

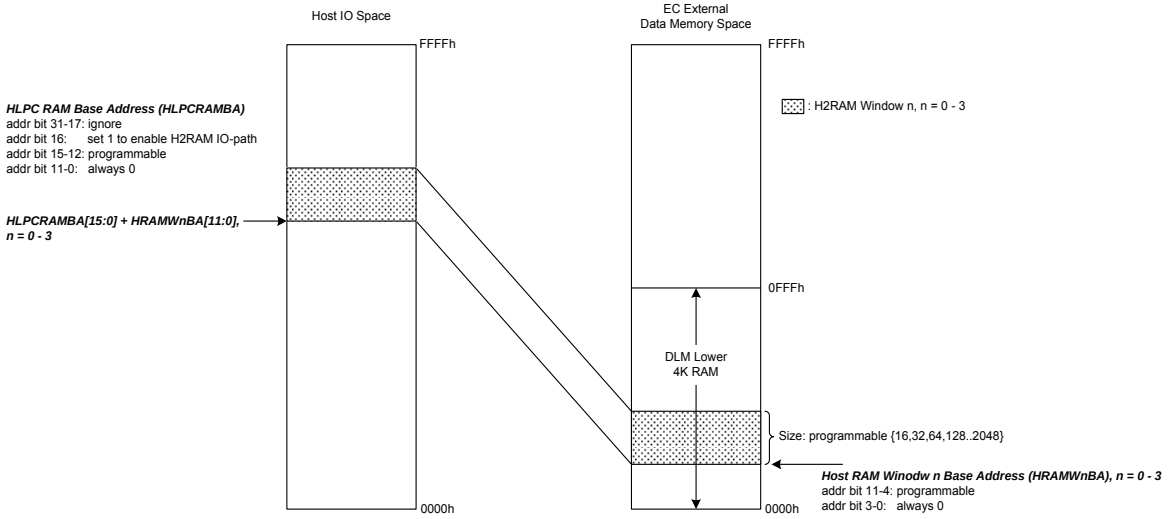
HLPC to DLM Lower 4K RAM



6.4.3.10.2 HLPC to EC DLM Lower 4K RAM (H2RAM-HLPC) through LPC IO Cycles

- H2RAM also can be used in translating some addresses from the host IO space to Scratch RAM space.
- The read/write protection mechanism is also supported by this function.

Figure 6-17. H2RAM-HLPC Mapping through LPC IO Cycles



6.4.3.10.3 H2RAM EC/Host Semaphore

A LPC Memory/FWH/IO Write cycle targeted on H2RAM host semaphore will produce an interrupt (INT83) to inform EC and a Data-Write instruction executed on H2RAM EC semaphore also generates an IRQ to the host. Through these semaphores, the host and EC can communicate with each other during H2RAM data transfer.

Figure 6-18. H2RAM EC/Host Semaphore Interrupt through LPC Memory/FWH Cycles

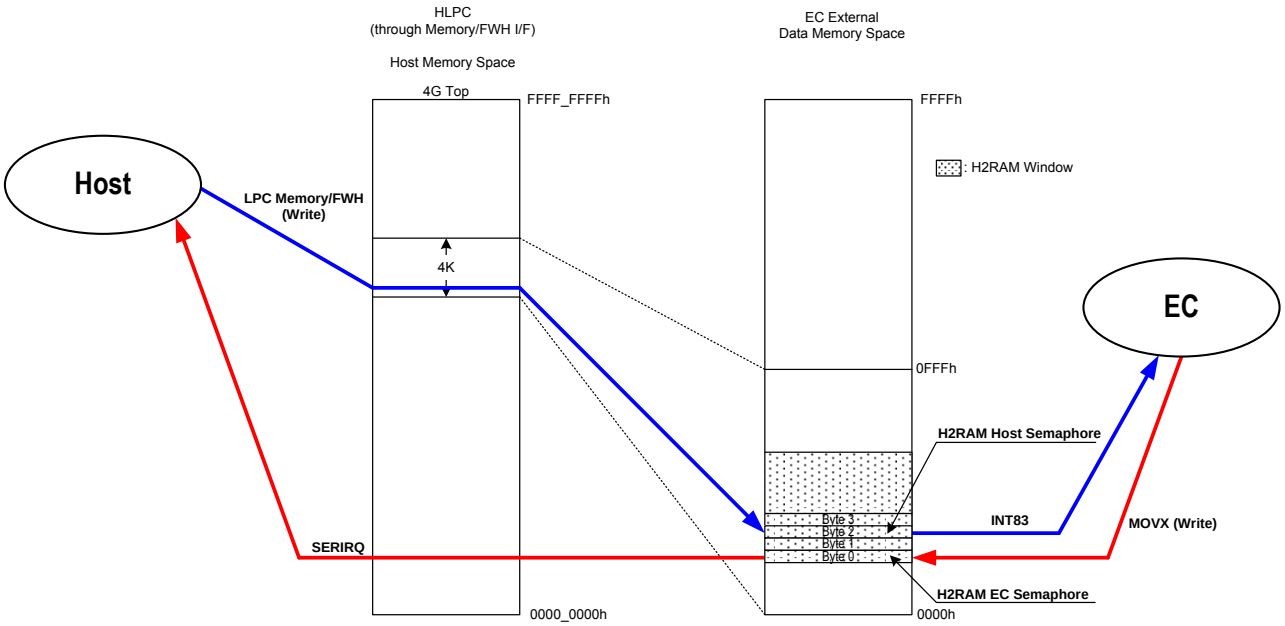
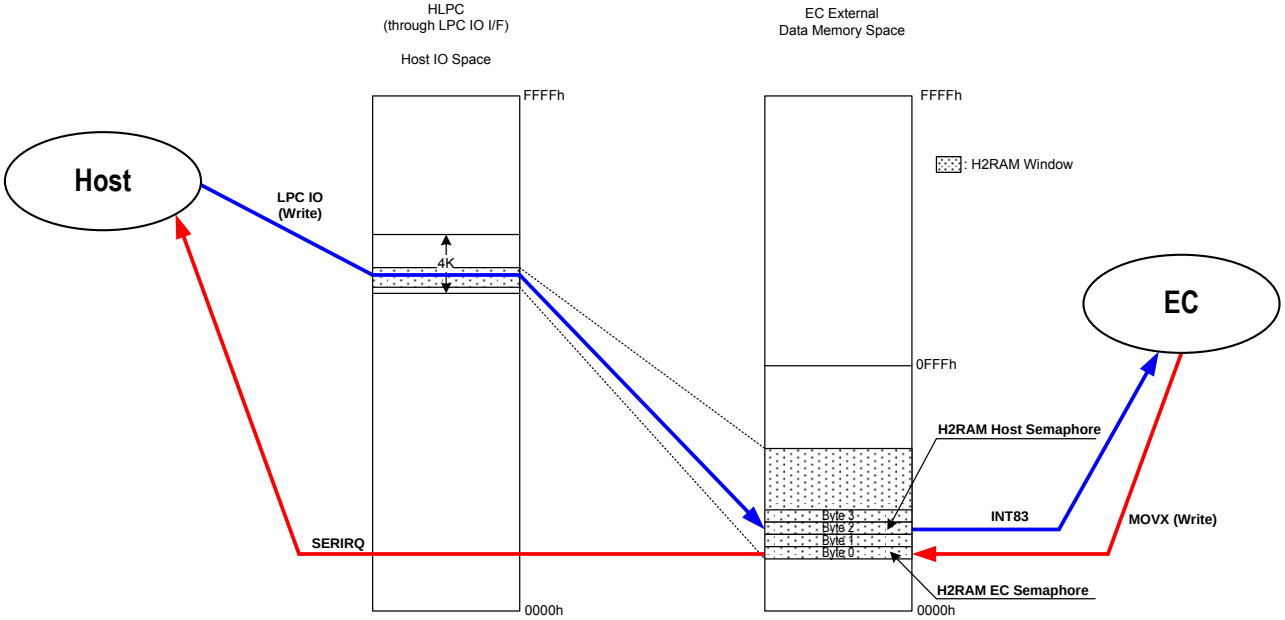


Figure 6-19. H2RAM EC/Host Semaphore Interrupt through LPC IO Cycles



6.4.3.11 E-flash Power-on Detection

6.4.3.11.1 16B-signature and Implicit/Explicit EC Code Base Address

A specific 16B-signature is used to locate the EC code base address.

1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th
A5h	A5h	A5h	A5h	A5h	A5h	A5h	flag	85h	12h	5Ah	5Ah	AAh	AAh	55h	55h

All content of the 16 bytes must match the content in the table.
Note: Add 16-bytes signature in F/W (strongly recommented)

8th byte's bit 7:
It must be 1b.
8th byte's bit 6:
It must be 0b.
8th byte's bit 5:
It must be 0b.
8th byte's bit 4:
It must be 1b.
8th byte's bit 3:
It must be 0b.
8th byte's bit 2:
It must be 1b.
8th byte's bit 1:
It must be 0b.
8th byte's bit 0:
It must be 1b and this option is removed.

1st byte must be located at 16-byte boundary.
For example, let the address of 1st byte be ADDR1[23:0], then ADDR1[3:0] must be 0000b.

14st byte indicates the compared range ADDR [17:10] between e-flash and SPI flash. The compared range is up to 128K-byte and is multiple of 1K-byte. ADDR[17] must be 0b.

The 1st byte must be located at the address 40h, 50h, 60h, …F0h offset to the EC code base. For example, let the address of 1st byte be ADDR1[23:0], then ADDR1[7:0] must be 40h, 50h, 60h…F0h (interval 10h) and the EC code base is loated at (ADDR1[23:12] * 2^12).

6.4.3.11.2 Detection Sequence

Table 6-28. Corresponding Table of SPI Flash Power-on Detection

	Scanned Address or Scanned Range	Contents	If content is matched, EC code base address wil be at	Note
(a)	[addr 0040h], [addr 0050h], [addr 0060h], … [addr 00F0h]	16B-signature with implicit format.	000000h	Use implicit format.

6.4.4 EC Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal CPU processor. The base address for SMFI is 1000h.

These registers are listed below.

Table 6-29. EC View Register Map, SMFI

7 0	Offset
FBIU Configuration (FBCFG)	00h
Flash Programming Configuration Register (FPCFG)	01h
Shared Memory EC Control and Status Register (SMECCS)	20h
Shared Memory Host Semaphore (SMHSR)	22h
Flash Control 1 Register (FLHCTRL1R)	31h
Flash Control 2 Register (FLHCTRL2R)	32h
uC Control Register (UCCTRLR)	34h
Host Control 2 Register (HCTRL2R)	36h
EC-Indirect Memory Address Register 0 (ECINDAR0)	3Bh
EC-Indirect Memory Address Register 1 (ECINDAR1)	3Ch
EC-Indirect Memory Address Register 2 (ECINDAR2)	3Dh
EC-Indirect Memory Address Register 3 (ECINDAR3)	3Eh
EC-Indirect Memory Data Register (ECINDDR)	3Fh
Scratch SRAM 0 Address Low Byte Register (SCAR0L)	40h
Scratch SRAM 0 Address Middle Byte Register (SCAR0M)	41h
Scratch SRAM 0 Address High Byte Register (SCAR0H)	42h
Protect 0 Base Addr Register 0 (P0BA0R)	4Fh
Protect 0 Base Addr Register 1 (P0BA1R)	50h
Protect 0 Size Register (P0ZR)	51h
Protect 1 Base Addr Register 0 (P1BA0R)	52h
Protect 1 Base Addr Register 1 (P1BA1R)	53h
Protect 1 Size Register (P1ZR)	54h
Protect 2 Base Addr Register 0 (P2BA0R)	70h
Protect 2 Base Addr Register 1 (P2BA1R)	71h
Protect 2 Size Register (P2ZR)	72h
Protect 3 Base Addr Register 0 (P3BA0R)	73h
Protect 3 Base Addr Register 1 (P3BA1R)	74h
Protect 3 Size Register (P3ZR)	75h
Deferred SPI Instruction (DSINST)	55h
Deferred SPI Address 15-12 (DSADR1)	56h
Deferred SPI Address 23-16 (DSADR2)	57h
Host Instruction Control 1 (HINSTC1)	58h
Host Instruction Control 2 (HINSTC2)	59h
Flash Control Register 3 (FLHCTRL3R)	63h
Flash Control Register 4 (FLHCTRL4R)	64h
Security Host View Block Mode Select [15:8] (SHVBMS[15:8])	6Bh
Security Host View Block Mode Select [7:0] (SHVBMS[7:0])	6Ch
Host RAM Window Control (HRAMWC)	5Ah
Host RAM Window 0 Base Address (HRAMW0BA[11:4])	5Bh
Host RAM Window 1 Base Address (HRAMW1BA[11:4])	5Ch
Host RAM Window 0 Access Allow Size (HRAMW0AAS)	5Dh
Host RAM Window 1 Access Allow Size (HRAMW1AAS)	5Eh
Host RAM Window 2 Base Address (HRAMW2BA[11:4])	76h
Host RAM Window 3 Base Address (HRAMW3BA[11:4])	77h

7 0	Offset
Host RAM Window 2 Access Allow Size (HRAMW2AAS)	78h
Host RAM Window 3 Access Allow Size (HRAMW3AAS)	79h
H2RAM EC Semaphore Interrupt Enable (H2RAMECSIE)	7Ah
H2RAM EC Semaphore Address (H2RAMECSA)	7Bh
H2RAM Host Semaphore Status (H2RAMHSS)	7Ch
Host Protect Authentication Data Register (HPADR)	7Eh
Flash Control 5 Register (FLHCTRL5R)	80h
Flash Control 6 Register (FLHCTRL6R)	81h
Scratch SRAM SMBus Address Low Byte Register (SCARSL)	9Fh
Scratch SRAM SMBus Address Middle Byte Register (SCARSM)	A0h
Scratch SRAM SMBus Address High Byte Register (SCARSH)	A1h

6.4.4.1 FBIU Configuration Register (FBCFG)

The FBIU (Flash Bus Interface Unit) directly interfaces with the flash device. The FBIU also defines the access time to the flash base address from 00_0000h to 3F_FFFFh (4M bytes).

Address Offset: 00h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

6.4.4.2 Flash Programming Configuration Register (FPCFG)

This register provides general control on banking and flash standby.

Address Offset: 01h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	Serial flash: 0b	**Auto Flash Standby (AFSTBY)** Serial flash: 1: Stop flash access in Doze/Deep Doze/Sleep mode and issue “Deep Power Down (B9h)” instruction before entering Sleep mode and issue “Release Deep Power Down (ABh)” instruction after waking up from Sleep mode. 0: Prevent the flash from entering the standby mode
5-0	-	-	**Reserved**

6.4.4.3 Shared Memory EC Control and Status Register (SMECCS)

The following set of registers is accessible only by the EC. The registers are applied to VSTBY.
This register provides the flash control and status of a restricted access.

Address Offset: 20h

Bit	R/W	Default	Description
7	R/W	0b	**Host Semaphore Interrupt Enable (HSEMIE)** It enables interrupt to CPU via INT22 of INTC. 0: Disable the host semaphore (write) interrupt to the EC. 1: The interrupt is set (level high) if HSEMW bit is set.
6	R/WC	0b	**Host Semaphore Write (HSEMW)** 0: Host has not written to HSEM3-0 field in SMHSR register. 1: Host has written to HSEM3-0 field in SMHSR register. Writing 1 to this bit to clear itself and clear internal detect logic. Writing 0 has no effect.
5	R/W	0b	**Host Write Allow (HOSTWA)** This bit is for HLPC only. If host I/F is LPC command, its default value is 0. If host I/F is I2C pre-defined command, its default value is 1. 0: The SMFI does not generate write transactions on M-bus. 1: The SMFI can generate write transactions on M-bus. The read performance on M-bus will be very poor for Host LPC if write transaction is allowed.
4-3	R	01b	**Host Error Response (HERES)** These bits control response types on read/write translation from/to a protected address. 01b: Read back FFh; ignoring write Otherwise: Reserved
2-0	-	-	**Reserved**

6.4.4.4 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register is reset on host domain hardware reset.
This is the register the same as the one in section 6.4.5.8 but they are in different views.

Address Offset: 22h

Bit	R/W	Default	Description
7-4	R/W	0h	**EC Semaphore (CSEM3-0)** These four bits may be written by the EC and read by both the host and the EC
3-0	R	0h	**Host Semaphore (HSEM3-0)** These four bits may be written by the host and read by both the host and the EC.

6.4.4.5 Flash Control 1 Register (FLHCTRL1R)

Address Offset: 31h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	001b	**SPI Flash Read Mode (SPIFR)** For serial flash: 100b: Uses instruction = EBh 011b: Uses instruction = BBh 010b: Uses instruction = 3Bh 001b: Uses instruction = 0Bh 000b: Uses instruction = 03h The performance of “Read” cycle is better than “Fast Read” cycle in the same frequency since “Fast Read” cycle request 8 dummy clock ticks in each cycle. The attached must support “Fast Read” cycle since it’s the default read instruction to serial flash. Instruction A3h of SPI flash isn’t supported. A few flash types can not achieve their documented frequencies without issuing this instruction.
3	R/W	1b	**Serial Wait 1T (LFSW1T)** For serial flash: Always write 1 to it.
2-0	-	-	**Reserved**

6.4.4.6 Flash Control 2 Register (FLHCTRL2R)

For serial flash only.

Address Offset: 32h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	00b	**FSCE# Min Read High Width (SCEMINRHW)** 00b: Disable 01b: Reserved 10b: 1.5T 11b: Reserved It is similar to SCEMINHW; however, it only applies to the width after all read instructions and overrides SCEMINHW.
3	-	-	**Reserved**
2-0	R/W	011b	**FSCE# Min High Width (SCEMINHW)** 000b: Reserved 001b: 1.5T 010b: 2.5T 011b: 3.5T 100b: 4.5T 101b: 5.5T 110b: 6.5T It depends on the “FSCE# High Time” on flash specification. Small value gets better performance. This register may needs to be modified before the PLL frequency is changed.

6.4.4.7 uC Control Register (UCCTRLR)

Address Offset: 34h

Bit	R/W	Default	Description
7	R/W	0b	**uC Burst Mode (UCBST)** 0: Default 1: for chipset that issues LPC Abort if LPC Long-wait count during a LPC Memory cycle is greater than 255. This bit can be modified only before VCC power is supplied.
6	-	-	**Reserved**
5-3	-	-	**Reserved**
2-0	R/W	5h	**uC Burst Threshold (UCTH)** 5h: default 3h: for chipset that issues LPC Abort if LPC Long-wait count during a LPC Memory cycle is greater than 255. Otherwise: reserved. This field can be modified only before VCC power is supplied.

6.4.4.8 Host Control 2 Register (HCTRL2R)

Address Offset: 36h

Bit	R/W	Default	Description
7	R/W	1b	**Host Bridge Enable (HBREN)** 1: The host memory cycle is decoded 0: Otherwise This bit can be modified only before VCC power is supplied.
6	-	-	Reserved
5	R/W	0b	**HLPC Follow Mode 1 Enable (HFW1EN)** 1: Enable HLPC Follow Mode 1 if HOSTWA bit in SMECCS register isn't set. 0: Otherwise This bit can be modified only before VCC power is supplied.
4-0	-	-	**Reserved**

6.4.4.9 EC-Indirect Memory Address Register 0 (ECINDAR0)

Address Offset: 3Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA7-0)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.10 EC-Indirect Memory Address Register 1 (ECINDAR1)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA15-8)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.11 EC-Indirect Memory Address Register 2 (ECINDAR2)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA23-16)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.12 EC-Indirect Memory Address Register 3 (ECINDAR3)

Address Offset: 3Eh

Bit	R/W	Default	Description
7-6	W	-	**EC-Indirect Memory Address (ECINDA31-30)** 00b/11b: Select SPI 01b: Select e-flash 10b: Reserved
5-4	R	00b	**EC-Indirect Memory Address (ECINDA29-28)** Read only.
3-0	R/W	0h	**EC-Indirect Memory Address (ECINDA27-24)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.4.4.13 EC-Indirect Memory Data Register (ECINDDR)

Address Offset: 3Fh

Bit	R/W	Default	Description
7-0	R/W	-	**EC-Indirect Memory Data (ECINDD7-0)** Read/Write to this register will access one byte on the flash with the 32-bit flash address defined in ECINDAR3-0.

6.4.4.14 Scratch SRAM 0 Address Low Byte Register (SCAR0L)

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 0 Address (SC0A7-0)** The bit 1-0 is constant 0, that is, 4-byte boundary.

6.4.4.15 Scratch SRAM 0 Address Middle Byte Register (SCAR0M)

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 0 Address (SC0A15-8)**

6.4.4.16 Scratch SRAM 0 Address High Byte Register (SCAR0H)

Address Offset: 42h

Bit	R/W	Default	Description
7	W	-	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing.
6-3	-	-	**Reserved**
2-0	R/W	111b	**Scratch SRAM 0 Address (SC0A18-16)** The default value makes this scratch SRAM not be a scratch ROM. **Note:** Write cycle to this register will clear cache. **Note:** Enable mapping Scratch SRAM to Scratch ROM will occupy parts of the cache and regress the cache performance.

6.4.4.17 Protect 0 Base Addr Register 0 (P0BA0R)

For SPI flash only.

Address Offset: 4Fh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	-	**Protect 0 Address (P0BA23-20)** The default value is uncertain.

6.4.4.18 Protect 0 Base Addr Register 1 (P0BA1R)

For SPI flash only.

Address Offset: 50h

Bit	R/W	Default	Description
7-0	R/W	-	**Protect 0 Address (P0BA19-12)** The default value is uncertain.

6.4.4.19 Protect 0 Size Register (P0ZR)

For SPI flash only.

Address Offset: 51h

Bit	R/W	Default	Description
7-6	R/W	00b	**Protect 0 Mode (P0M)** It controls the protection mode of set 0. 00b: Read protection 01b: Write protection 10b: Read protection plus write protection 11b: Reserved This field returns to the default after warm set, and VSTBY power-up reset.
5	R/W	0b	**Release 4K Proteted Part (R4PP)** 0b: Disable 1b: The upper 4K part of the range that is specified by P0Z will be released from protection function. This bit is valid only when P0Z is 5h, 6h, Eh, 7h, 8h, 9h, Ah or Bh.
4	-	-	**Reserved**
3-0	R/W	0	**Protect 0 Size (P0Z)**

Bit	R/W	Default	Description
			If this field is zero, there is no memory block on SPI flash locked by “Protect 0” configuration. If this field is not zero, it means that read or write cycles from the host side to the specified SPI memory block are locked. The address defined by P0BA0R and P0BA1R is SPI physical address, not host LPC address. If write protection is enabled in P0M field, this size field must be equal to or greater than the allowed sector/block size of ERASE instruction. See also HINSTC2 register. This field returns to the default after warm set, and VSTBY power-up reset. The protected size cannot cross the boundary of the base address. 0h: Disable 1h: The range is from (P0BA[23..12] << 12) to (P0BA[23..12] << 12) + ((1 << 12) - 1) and totally 2^12 (4K) bytes are locked. 2h: The range is from (P0BA[23..13] << 13) to (P0BA[23..13] << 13) + ((1 << 13) - 1) and totally 2^13 (8K) bytes are locked. 3h: The range is from (P0BA[23..14] << 14) to (P0BA[23..14] << 14) + ((1 << 14) - 1) and totally 2^14 (16K) bytes are locked. 4h: The range is from (P0BA[23..15] << 15) to (P0BA[23..15] << 15) + ((1 << 15) - 1) and totally 2^15 (32K) bytes are locked. 5h: The range is from (P0BA[23..16] << 16) to (P0BA[23..16] << 16) + ((1 << 16) - 1) and totally 2^16 (64K) bytes are locked. 6h: The range is from (P0BA[23.. 17] << 17) to (P0BA[23.. 17] << 17) + ((1 << 17) - 1) and totally 2^17 (128K) bytes are locked. Eh: The range is from (P0BA[23.. 18] <<18) to (P0BA[23.. 18] << 18) + ((1 << 18) - 1) and totally 2^18 (256K) bytes are locked. 7h: The range is from (P0BA[23.. 19] <<19) to (P0BA[23.. 19] << 19) + ((1 <<19) - 1) and totally 2^19 (512K) bytes are locked. 8h: The range is from (P0BA[23.. 19] <<20) to (P0BA[23.. 19] << 20) + ((1 <<20) - 1) and totally 2^20 (1M) bytes are locked.

Bit	R/W	Default	Description
			9h: The range is from (P0BA[23.. 19] <<21) to (P0BA[23.. 19] << 21) + ((1 <<21) - 1) and totally 2^21 (2M) bytes are locked. Ah: The range is from (P0BA[23.. 19] <<22) to (P0BA[23.. 19] << 22) + ((1 <<22) - 1) and totally 2^22 (4M) bytes are locked. Bh: The range is from (P0BA[23.. 19] <<23) to (P0BA[23.. 19] << 23) + ((1 <<23) - 1) and totally 2^23 (8M) bytes are locked. Otherwise: Reserved

6.4.4.20 Protect 1 Base Addr Register 0 (P1BA0R)

For SPI flash only.

Address Offset: 52h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	-	**Protect 1 Address (P1BA23-20)** The default value is uncertain.

6.4.4.21 Protect 1 Base Addr Register 1 (P1BA1R)

For SPI flash only.

Address Offset: 53h

Bit	R/W	Default	Description
7-0	R/W	-	**Protect 1 Address (P1BA19-12)** The default value is uncertain.

6.4.4.22 Protect 1 Size Register (P1ZR)

For SPI flash only.

Address Offset: 54h

Bit	R/W	Default	Description
7-6	R/W	00b	**Protect 1 Mode (P1)** “Protect 1” configuration is the same as “Protect 0”.
5-4	-	-	**Reserved**
3-0	R/W	0	**Protect 1 Size (P1Z)** “Protect 1” configuration is the same as “Protect 0”.

6.4.4.23 Protect 2 Base Addr Register 0 (P2BA0R)

For SPI flash only.

Address Offset: 70h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	-	**Protect 2 Address (P2BA23-20)** The default value is uncertain.

6.4.4.24 Protect 2 Base Addr Register 1 (P2BA1R)

For SPI flash only.

Address Offset: 71h

Bit	R/W	Default	Description
7-0	R/W	-	**Protect 2 Address (P2BA19-12)** The default value is uncertain.

6.4.4.25 Protect 2 Size Register (P2ZR)

For SPI flash only.

Address Offset: 72h

Bit	R/W	Default	Description
7-6	R/W	00b	**Protect 2 Mode (P2)** “Protect 2” configuration is the same as “Protect 0”.
5-4	-	-	**Reserved**
3-0	R/W	0	**Protect 2 Size (P2Z)** “Protect 2” configuration is the same as “Protect 0”.

6.4.4.26 Protect 3 Base Addr Register 0 (P3BA0R)

For SPI flash only.

Address Offset: 73h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	-	**Protect 3 Address (P3BA23-20)** The default value is uncertain.

6.4.4.27 Protect 3 Base Addr Register 1 (P3BA1R)

For SPI flash only.

Address Offset: 74h

Bit	R/W	Default	Description
7-0	R/W	-	**Protect 3 Address (P3BA19-12)** The default value is uncertain.

6.4.4.28 Protect 3 Size Register (P3ZR)

For SPI flash only.

Address Offset: 75h

Bit	R/W	Default	Description
7-6	R/W	00b	**Protect 3 Mode (P3)** "Protect 3" configuration is the same as "Protect 0".
5-4	-	-	**Reserved**
3-0	R/W	0	**Protect 3 Size (P3Z)** "Protect 3" configuration is the same as "Protect 0".

6.4.4.29 Deferred SPI Instruction (DSINST)

For SPI flash only.

Address Offset: 55h

Bit	R/W	Default	Description
7-0	R	-	**Deferred SPI Instruction (DSINST)** The 8-bit instruction code of deferred SPI WIP instruction.

6.4.4.30 Deferred SPI Address 15-12 (DSADR1)

For SPI flash only.

Address Offset: 56h

Bit	R/W	Default	Description
7-4	R	-	**Deferred SPI Address 15-12 (DSA15-12)** The SPI address of deferred SPI WIP instruction.
3-0	-	-	**Reserved**

6.4.4.31 Deferred SPI Address 23-16 (DSADR2)

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R	-	**Deferred SPI Address 23-16 (DSA23-16)** The SPI address of deferred SPI WIP instruction.

6.4.4.32 Host Instruction Control 1 (HINSTC1)

For HSPI only.

Address Offset: 58h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	-	**Scan EC Base (SCECB)** (For e-flash) See also section 6.4.3.11 E-flash Power-on Detection on page 120. Write 1: Scan e-flash control byte and 16 byte Signature. Write 0: Ignored. Read always returns 0. The firmware may write 1 to this bit after the flash is programmed.
5-4	-	-	**Reserved**
3	W	-	**DISS Valid (DISSV)** (For SPI flash only) Write 1: Writing DISS bit in this register is valid. Write 0: Writing DISS bit in this register is ignored. Only write 1 to this bit while INT59 is active.
2	R/W	-	**Deferred Instruction's Succeeding Step (DISS)** (For SPI flash only) Always write 1 to this bit. Writing data to this bit and writing 1 to DISSV bit must be in the same write cycle, or this writing action to DISS bit is ignored.
1-0	R/W	00b	**Enable Deferring WIP Instruction (ENDI)** (For SPI flash only) HLPC: 11b:Enable deferring an ERASE/PROG instruction in the Follow mode by returning Long-Waits and issuing INT59. 00b: Disable Otherwise: Reserved.

6.4.4.33 Host Instruction Control 2 (HINSTC2)

This register is only valid when LPC hardware protection is enabled by setting P0ZR and P1ZR register.

Some SPI flashes provide two or more sector/block ERASE instructions, e.g. 4K and 64K ERASE instruction. If one specified 4K block is set as hardware protection, it may be erased by 64K ERASE instruction.

To accomplish the hardware protectin on the SPI flash, the size defined in P0Z/P1Z field in P0ZR/P1ZR register must be equal to or greater than the allowed sector/block size of ERASE instruction.

For the above example, if an SPI flash provides the 4K ERASE instruction (code 20h) and 64K ERASE instruction (code D8h), the write protection can work well if the size defined in P0Z/P1Z field is equal to or greater than 64K; otherwise, the 64K ERASE instruction should be inhibited by setting DISEID8 bit.

Address Offset: 59h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Host Indirect Cycle Target Select (HICTS)** 0b: SPI flash 1b: e-flash
4	R/W	0b	**LPC Memory Cycle Target Select (LMCTS)** 0b: SPI flash 1b: e-flash
3	R/W	0b	**Disable Erase Instruction D8h (DISEID8)** (For SPI flash only) Erasing sector/block instruction D8h will be inhibited.
2	R/W	0b	**Disable Erase Instruction D7h (DISEID7)** (For SPI flash only) Erasing sector/block instruction D7h will be inhibited.
1	R/W	0b	**Disable Erase Instruction 52h (DISEI52)** (For SPI flash only) Erasing sector/block instruction 52h will be inhibited.
0	R/W	0b	**Disable Erase Instruction 20h (DISEI20)** (For SPI flash only) Erasing sector/block instruction 20h will be inhibited.

6.4.4.34 Flash Control Register 3 (FLHCTRL3R)

Address Offset: 63h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**SPI flash I/F Enable (SIFE)** 0b: Disable 1b: Enable SPI flash
2-1	-	-	**Reserved**
0	R/W	0b	**Force FSPI I/F Tri-state (FFSPITRI)** 1: FSCK/FSCE#/FMISO/FMOSI are tri-state. 0: FSCK/FSCE#/FMISO/FMOSI are normal operation.

6.4.4.35 Flash Control Register 4 (FLHCTRL4R)

Address Offset: 64h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	W	0b	**Scan SPI 16 Byte Signature (SS16BS)** 1b: Scan 16 byte signature on SPI flash. This bit is available only if FTHS@ FLHCTRL5R = 0. 0b: Ignored
4-0	-	-	**Reserved**

6.4.4.36 Security Host View Block Mode Select [15:8] (SHVBMS[15:8])

HVBMS[15:0] will be replaced by SHVBMS[15:0] if SECKEY[63:0] matches with HAK[63:0].

Address Offset: 6Bh

Bit	R/W	Default	Description
7-6	R/W	11b	**Security Host View Block Mode Select [7:6] (SHVBMS[7:6])** It controls the e-flash protection mode for host view. 11b: Block 4 of e-flash is read/write allowed. 10b: Block 4 of e-flash is read allowed, but write protected. 01b: Block 4 of e-flash is read protected, but write allowed. 00b: Block 4 of e-flash is read/write protected. This field is available only when SECKEY[63:0] matches with HAK[63:0] and RHVPC is set.
5-4	R/W	11b	**Security Host View Block Mode Select [5:4] (SHVBMS[5:4]** Similar to bit 7-6 but it acts on block 5 of e-flash.
3-2	R/W	11b	**Security Host View Block Mode Select [3:2] (SHVBMS[3:2]** Similar to bit 7-6 but it acts on block 6 of e-flash.
1-0	R/W	11b	**Security Host View Block Mode Select [1:0] (SHVBMS[1:0]** Similar to bit 7-6 but it acts on block 7 of e-flash.

6.4.4.37 Security Host View Block Mode Select [7:0] (SHVBMS[7:0])

HVBMS[15:0] will be replaced by SHVBMS[15:0] if SECKEY[63:0] matches with HAK[63:0].

Address Offset: 6Ch

Bit	R/W	Default	Description
7-6	R/W	11b	**Security Host View Block Mode Select [15:14] (SHVBMS[15:14])** It controls the e-flash protection mode for host view. 11b: Block 0 of e-flash is read/write allowed. 10b: Block 0 of e-flash is read allowed, but write protected. 01b: Block 0 of e-flash is read protected, but write allowed. 00b: Block 0 of e-flash is read/write protected. This field is available only when SECKEY[63:0] matches with HAK[63:0] and RHVPC is set.
5-4	R/W	11b	**Security Host View Block Mode Select [13:12] (SHVBMS[13:12]** Similar to bit 7-6 but it acts on block 1 of e-flash.
3-2	R/W	11b	**Security Host View Block Mode Select [11:10] (SHVBMS[11:10]** Similar to bit 7-6 but it acts on block 2 of e-flash.
1-0	R/W	11b	**Security Host View Block Mode Select [9:8] (SHVBMS[9:8]** Similar to bit 7-6 but it acts on block 3 of e-flash.

6.4.4.38 Host RAM Window Control (HRAMWC)

Address Offset: 5Ah

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**H2RAM Path Select (H2RAMPS)** 0b: H2RAM through LPC Memory/FWH cycle. 1b: H2RAM through LPC IO cycle.
3	R/W	0b	**H2RAM Window 3 Enable (H2RAMW3E)** 0b: Disable 1b: H2RAM window 3 enabled.
2	R/W	0b	**H2RAM Window 2 Enable (H2RAMW2E)** 0b: Disable 1b: H2RAM window 2 enabled.
1	R/W	0b	**H2RAM Window 1 Enable (H2RAMW1E)** 0b: Disable 1b: H2RAM window 1 enabled.
0	R/W	0b	**H2RAM Window 0 Enable (H2RAMW0E)** 0b: Disable 1b: H2RAM window 0 enabled.

6.4.4.39 Host RAM Window 0 Base Address (HRAMW0BA[11:4])

Address Offset: 5Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 0 Base Address Bits [11:4] (HRAMW0BA[11:4])** Define RAM window 0 base address.

6.4.4.40 Host RAM Window 1 Base Address (HRAMW1BA[11:4])

Address Offset: 5Ch

Bit	R/W	Default	Description
0	R/W	00h	**Host RAM Window 1 Base Address Bits [11:4] (HRAMW1BA[11:4])** Define RAM window 1 base address.

6.4.4.41 Host RAM Window 0 Access Allow Size (HRAMW0AAS)

Address Offset: 5Dh

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 0 Read Protect Enable (HRAMW0RPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 0 Write Protect Enable (HRAMW0WPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 0 Size (HRAMW0S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.42 Host RAM Window 1 Access Allow Size (HRAMW1AAS)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 1 Read Protect Enable (HRAMW1RPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 1 Write Protect Enable (HRAMW1WPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 1 Size (HRAMW1S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.43 Host RAM Window 2 Base Address (HRAMW2BA[11:4])

Address Offset: 76h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 2 Base Address Bits [11:4] (HRAMW2BA[11:4])** Define RAM window 2 base address.

6.4.4.44 Host RAM Window 3 Base Address (HRAMW3BA[11:4])

Address Offset: 77h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 3 Base Address Bits [11:4] (HRAMW3BA[11:4])** Define RAM window 3 base address.

6.4.4.45 Host RAM Window 2 Access Allow Size (HRAMW2AAS)

Address Offset: 78h

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 2 Read Protect Enable (HRAMW2RPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 2 Write Protect Enable (HRAMW2WPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 2 Size (HRAMW2S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.4.4.46 Host RAM Window 3 Access Allow Size (HRAMW3AAS)

Address Offset: 79h

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 3 Read Protect Enable (HRAMW3RPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 3 Write Protect Enable (HRAMW3WPE)** 00b: Disable 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 3 Size (HRAMW3S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

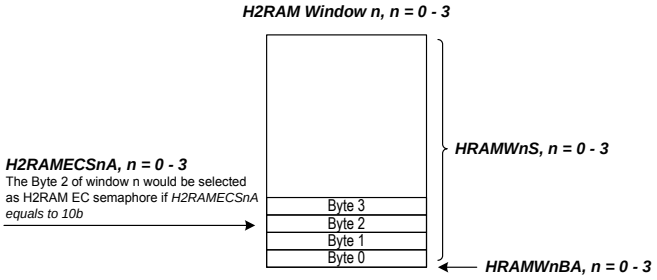
6.4.4.47 H2RAM EC Semaphore Interrupt Enable (H2RAMECSIE)

Address Offset: 7Ah

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**H2RAM EC Semaphore 3 Interrupt Enable (H2RAMECS3IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 3 will produce an IRQ to the host.
2	R/W	0b	**H2RAM EC Semaphore 2 Interrupt Enable (H2RAMECS2IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 2 will produce an IRQ to the host.
1	R/W	0b	**H2RAM EC Semaphore 1 Interrupt Enable (H2RAMECS1IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 1 will produce an IRQ to the host.
0	R/W	0b	**H2RAM EC Semaphore 0 Interrupt Enable (H2RAMECS0IE)** 0b: Disable 1b: A Data-Write instruction executed on H2RAM EC semaphore 0 will produce an IRQ to the host.

6.4.4.48 H2RAM EC Semaphore Address (H2RAMECSA)

Figure 6-20. Location of H2RAM EC Semaphore



Address Offset: 7Bh

Bit	R/W	Default	Description
7-6	R/W	00b	**H2RAM EC Semaphore 3 Address (H2RAMECS3A)** 00b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 0). 01b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 1). 10b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 2). 11b: H2RAM EC semaphore 3 locates at (HRAMW3BA[11:0] + 3). This field is available only when H2RAM window 3 is enabled.
5-4	R/W	00b	**H2RAM EC Semaphore 2 Address (H2RAMECS2A)** 00b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 0). 01b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 1). 10b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 2). 11b: H2RAM EC semaphore 2 locates at (HRAMW2BA[11:0] + 3). This field is available only when H2RAM window 2 is enabled.

Bit	R/W	Default	Description
3-2	R/W	00b	**H2RAM EC Semaphore 1 Address (H2RAMECS1A)** 00b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 0). 01b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 1). 10b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 2). 11b: H2RAM EC semaphore 1 locates at (HRAMW1BA[11:0] + 3). This field is available only when H2RAM window 1 is enabled.
1-0	R/W	00b	**H2RAM EC Semaphore 0 Address (H2RAMECS0A)** 00b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 0). 01b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 1). 10b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 2). 11b: H2RAM EC semaphore 0 locates at (HRAMW0BA[11:0] + 3). This field is available only when H2RAM window 0 is enabled.

6.4.4.49 H2RAM Host Semaphore Status (H2RAMHSS)

EC can know H2RAM host semaphore status by reading this register.

Address Offset: 7Ch

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	0b	**H2RAM Host Semaphore 3 Status (H2RAMHS3S)** This bit is automatically set to 1b while H2RAM host semaphore 3 is written. 0b: H2RAM host semaphore 3 is not written. 1b: H2RAM host semaphore 3 is written. Writing 1 to clear this bit.
2	R/WC	0b	**H2RAM Host Semaphore 2 Status (H2RAMHS2S)** This bit is automatically set to 1b while H2RAM host semaphore 2 is written. 0b: H2RAM host semaphore 2 is not written. 1b: H2RAM host semaphore 2 is written. Writing 1 to clear this bit.
1	R/WC	0b	**H2RAM Host Semaphore 1 Status (H2RAMHS1S)** This bit is automatically set to 1b while H2RAM host semaphore 1 is written. 0b: H2RAM host semaphore 1 is not written. 1b: H2RAM host semaphore 1 is written. Writing 1 to clear this bit.
0	R/WC	0b	**H2RAM Host Semaphore 0 Status (H2RAMHS0S)** This bit is automatically set to 1b while H2RAM host semaphore 0 is written. 0b: H2RAM host semaphore 0 is not written. 1b: H2RAM host semaphore 0 is written. Writing 1 to clear this bit.

6.4.4.50 Host Protect Authentication Data Register (HPADR)

Address Offset: 7Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Protect Lock Authentication Data (GLAD)** The lock state is default off. Write: If the lock state is off, write Auth. Data will enable the lock state. If the lock state is on,write the same Auth. Data will disable the lock state. Read: 00h: The lock state is off. 01h: The lock state is on. If the lock state is on, P0BA0R ~ P1ZR , and P2BA0R ~ P3ZR aren't writable.

6.4.4.51 Flash Control 5 Register (FLHCTRL5R)

Address Offset: 80h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**Fetch Source (FTHS)** This bit can be revised only while code-fetch from the Scratch ROM. Write 0b: uC code-fetch from the e-flash or SPI flash (see also FTHS@FLHCTRL5R) Write 1b: uC code-fetch through eSPI flash sharing Read 0b: The controller has switched fetch source from e-flash or SPI flash. Read 1b: The controller has switched fetch source from eSPI flash sharing.
2-0	R	-	**e-flash size (FS)** 001b: 128K-byte 010b: 256K-byte 011b: 192K-byte Otherwise: Reserved

6.4.4.52 Flash Control 6 Register (FLHCTRL6R)

Address Offset: 81h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	01b	**Limit e-flash size (LFS)** 00b: No e-flash available; Always fetch from the SPI flash. 01b: Treat e-flash size as 2K-byte; uC address 0-7FFh will be fetched from the e-flash, otherwise will be fetched from the SPI flash. 10b: Treat e-flash size as 4K-byte; uC address 0-FFFh will be fetched from the e-flash, otherwise will be fetched from the SPI flash. 11b: Treat e-flash size as 128K-byte

6.4.4.53 Scratch SRAM SMBus Address Low Byte Register (SCARSL)

Address Offset: 9Fh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM SMBus Address (SCARS[7-0])** Notice: The LSB 4 bits of SCARS[7-0] must be 0 for 16-boundary if DFTSDFS is selected to SMBus Slave dedicated FIFO**.** The LSB 5 bits of SCARS[7-0] must be 0 for 32-boundary if DFTSDFS is selected to SMBus Master dedicated FIFO**.**

6.4.4.54 Scratch SRAM SMBus Address Middle Byte Register (SCARSM)

Address Offset: A0h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM SMBus Address (SCARS[15-8])**

6.4.4.55 Scratch SRAM SMBus Address High Byte Register (SCARSH)

Address Offset: A1h

Bit	R/W	Default	Description
7	R/W	0b	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing. DMA path is from Scratch SRAM SMBus address of flash to SMBus Slave or Master dedicated FIFO. For Slave dedicated FIFO, the transmission unit of DMA is 16 bytes at a time, and will align 16-byte boundary. The source inside flash must be located on 16-boundary. For Master dedicated FIFO, the transmission unit of DMA is 32 bytes at a time, and the source inside flash must be located on 32-boundary
6-0	-	-	**Reserved**

6.4.5 Host Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The SMFI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below

Table 6-30. Host View Register Map, SMFI

7 0	Offset
Shared Memory Indirect Memory Address (SMIMAR0-3)	00h-03H
Shared Memory Indirect Memory Data (SMIMDR)	04h
Security Key Index Register (SECKIR)	05h
Security Key Data Register (SECKDR)	06h
Shared Memory Host Semaphore (SMHSR)	0Ch

6.4.5.1 Shared Memory Indirect Memory Address Register 0 (SMIMAR0)

The following set of registers is accessible only by the host. The registers are applied to VCC.
This register defines the addresses 7-0 for a read or write transaction to the memory.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR7-0)**

6.4.5.2 Shared Memory Indirect Memory Address Register 1 (SMIMAR1)

This register defines the addresses 15-8 for a read or write transaction to the memory.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR15-8)**

6.4.5.3 Shared Memory Indirect Memory Address Register 2 (SMIMAR2)

This register defines the addresses 23-16 for a read or write transaction to the memory.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR23-16)**

6.4.5.4 Shared Memory Indirect Memory Address Register 3 (SMIMAR3)

This register defines the addresses 31-24 for a read or write transaction to the memory.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR31-24)**

6.4.5.5 Shared Memory Indirect Memory Data Register (SMIMDR)

This register defines the Data bits 7-0 for a read or write transaction to the memory.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Data (IMDA7-0)**

6.4.5.6 Security Key Index Register (SECKIR)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**
2-0	R/W	111b	**Security Key Index Register (SECKIR)** This field is used in specifying the index of SECKEY[63:0]. It is paired with SECKDR.

6.4.5.7 Security Key Data Register (SECKDR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	W	-	**Security Key Data Register (SECKDR)** This field is used in modifying the corresponding bits of SECKEY[63:0]. It is paired with SECKIR.

6.4.5.8 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register reset on host domain hardware reset.
This is the register the same as the one in section 6.4.4.7 on page 126 but they are in different views.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-4	R	0h	**EC Semaphore (CSEM3-0)** Four bits that may be updated by the EC and read by both the host and the EC.
3-0	R/W	0b	**Host Semaphore (HSEM3-0)** Four bits that may be updated by the host and read by both the host and the EC.

6.5 System Wake-Up Control (SWUC)

6.5.1 Overview

SWUC detects wake-up events and generate SCI#, SMI# and PWUREQ# signals to the host side, or alert EC by interrupts to WUC.

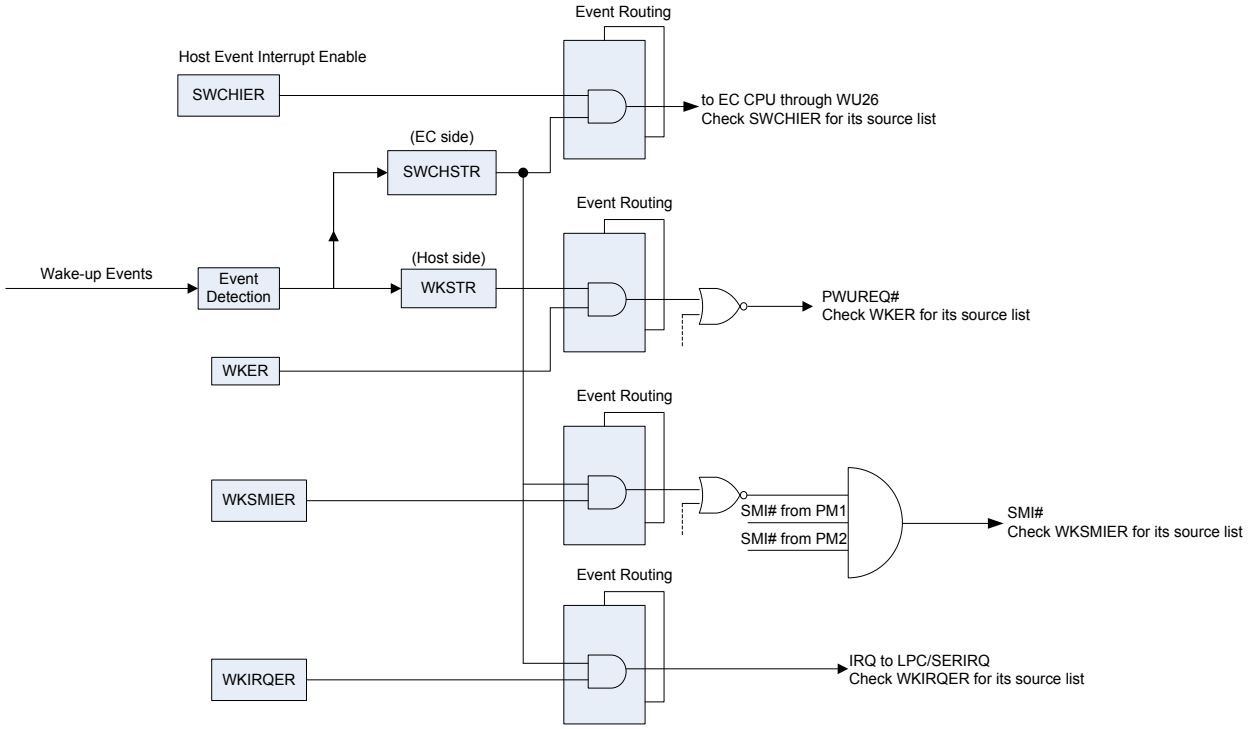
6.5.2 Features

- Supports programmable wake-up events source from the host controlled modules.
- Generates SMI# or PWUREQ# interrupt to the host to wake-up system.

6.5.3 Functional Description

The wake-up event and gathering scheme is shown in Figure 6-21. Wake-up Event and Gathering Scheme on page 146.

Figure 6-21. Wake-up Event and Gathering Scheme



6.5.3.1 Wake-Up Status

When the wake-up event is detected, the related status bit is set to 1 in both host and EC status registers, no matter whether any event enable bits are set or not. A status bit is cleared by writing 1 to it. Writing 0 to a status bit does not change its value. Clearing the event enable bit does not affect the status bit, but prevents it from issuing an event to output. The host uses a mask register (WKSMIER) to decide what the status bits will respond to.

6.5.3.2 Wake-Up Events

When a wake-up event is detected, it is recorded on a status bit in WKSTR (host view) register and SWCHSTR register (EC view), regardless of the enabled bit. Each event behavior is determined by a wake-up control logic controlled by a set of dedicated registers.

Input events are detected by the SWUC shown as the following:

- Module IRQ Wake-up event
- Modem Ring (RI1 and RI2)
- Telephone ring (RING input)
- RTCT alarm
- Software event
- Legacy off event
- ACPI state change event

Module IRQ Wake-Up Event
A module IRQ wake-up event from each logical device is asserted when the leading edge of the module IRQ is detected.
The related enable bit (WKIRQEN) has to be set to 1 to enable and trigger a wake-up event. Refer to the IRQNUM and WKIRQEN fields in IRQNUMX register. When the event is detected, MIRQS bit in WKSTR register is set to 1. If MIRQE in WKER register is also set to 1, the PWUREQ# output is still asserted and until the status bit is cleared.

Modem Ring
If transitions form high to low on RI1# (or RI2#) is detected on the Serial Port 1 (or Serial Port 2) connected to a modem, and then when the signal goes high on RI1#(or RI2#), it will cause a ring wake-up event asserted if the RI1#(or RI2#) event enable bit is set to 1 in the WKER register (bit0 for RI1#, and bit1 for RI2#).

Telephone Ring
If a transition from high to low is detected on the Ring input pin, and then when the signal goes high on Ring input pin. It will cause a ring wake-up event asserted when the ring event enable bit is set to 1 in the WKER register (BIT3).

RTCT Alarm
An alarm signal can be generated by RTCT module and used as a wake-up event. After an alarm event is detected in the RTCT, the RTCT alarm status bit will be set and RTCAL bit in SWCTL3 register will be set as well to respond it. To enable RTCT alarm as a wake-up event to EC, the software needs to follow the sequence listed below:
1. Set the Alarm condition in the RTCT module.
2. Set EIRTCA bit in SWCIER register to enable Alarm status interrupt masking.
3. Make sure that the RTCAL bit in SWCTL3 register is cleared.
4. Enable the Wake-Up on SWUC event in the WUC and INTC modules.

Software Event
This bit may trigger a wake event by software control. When the SIRQS (Software IRQ Event Status bit) in WKSTR register is set, a software event to the host is active. When the SIRQS bit in SWCHSTR register is set, a software event to the EC is active. The software event may be activated by the EC via access to the Host Controlled Module bridge regardless of the VCC status.
The SIRQS bit in SWCHSTR may be set when the respective bit toggles in WKSTR from 0 to 1 and when HSECM=0 is in SWCTL1 register. When HSECM =1 t, the SIRQS bit in SWCHSTR is set on a write of a 1 to the respective bit in WKSTR. The SIRQS bit in SWCHSTR is cleared by writing 1 to it.

Legacy Off Events
The host supports either legacy or ACPI mode. The operation mode is assigned on PWRBTN bit in the Super I/O Power Mode Register (SIOPWR). When EISCRDPBM bit in SWCIER register is set, any change in this bit will generate an interrupt to the EC. The EC may read this bit, using SCRDPBM bit in SWCTL2 register, to

determine the other power state. In the legacy mode, the PWRSLY bit in SIOPWR register represents a turn power off request. When this bit is set and SCRDPSO bit in SWCTL2 register is set, an interrupt is generated to EC if EISCRDPSO bit in SWCIER register is also set.

ACPI State Change Events
The bits (S1-S5) in WKACPIR register are used to provide a set of 'system power state change request'. The host uses these bits to issue an ACPI state change request. A write of 1 to any of these bits represents a state change request to the EC, the request may be also read out in SWCTL2 register even ACPIRS0 is represented when all bits in WKACPIR is cleared to 0. When any of ACPIRS0 -S5 bits in SWCTL2 is set and the respective mask bit in SWCIER register is set, an interrupt is generated to EC. All interrupt outputs may be cleared either writing 1 to the status bit or clearing the masking interrupt enable register.

6.5.3.3 Wake-Up Output Events

The SWUC output four types of wake-up events:
IRQ Interrupt through SERIRQ to the host side, which is activated by SWUC logical device of PNPCFG.
PWUREQ# Routing as an SCI# event.
SMI# Routing as an SMI# event.
WU26 An interrupt to the WUC module in the EC domain which is handled by EC firmware.

Output events are generated to the host when their status bit is set (1 in WKSTR). Output event to the EC through the WUC is generated when their EC status bit is set (1 in SWCHSTR). The host can program three Event Routing Control registers (WKSTR, WKSMIER and WKIRQER) to handle each of the host events to be asserted. This allows selective routing of these events output to PWUREQ#, SMI# and/or SWUC interrupt request (IRQ). After an output event is asserted, it can be cleared either by clearing its status bit or being masked. The current status of the event may be read out at the Wake-Up Event Status Register(WKSTR), and Wake-Up Signals Monitor Register (WKSMR). The SWUC also handles the wake-up event coming from the PMC 1 and 2 for SMI# event. In the EC domain, Wake-Up Event Interrupt Enable register (SWCHIER) holds an enable bit to allow selective routing of the event to output the EC wake-up interrupt (WU26) to the WUC.

6.5.3.4 Other SWUC Controlled Options

Additionally, the SWUC handles the following system control signals:
Host Keyboard Reset (KBRST#)
GA20 Signal
Host Configuration Address Option

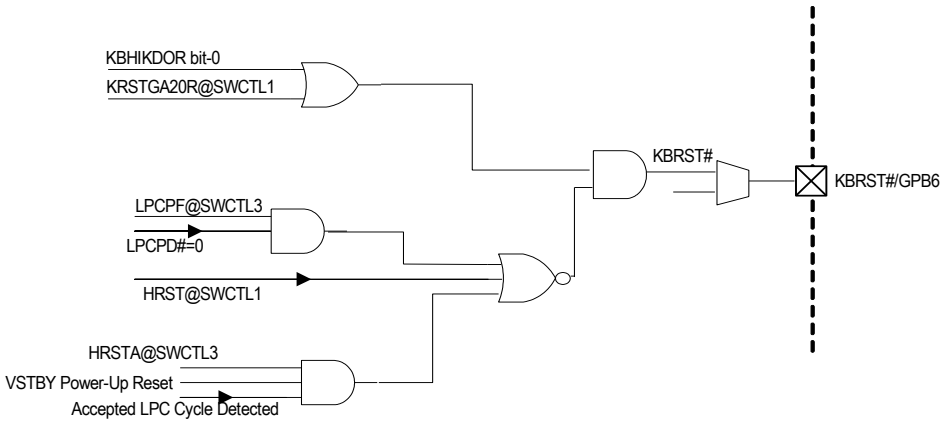
- **Host Keyboard Reset (KBRST#)**

The Host Keyboard Reset output (KBRST#) can be asserted either by software or hardware:
Software: KBRST# will be asserted when the EC firmware issues a reset command by writing 1 to HRST in SWCTL1 register. Clear this bit to de-assert the KBRST#.
Hardware: KBRST# will be asserted during VSTBY Power-Up reset if HRSTA bit in SWCTL3 register is set and a LPC transaction is started.

The KBRST# signal will be active in the following conditions:
(1) HRSTA bit in the SWUC is enabled and LPC cycle is active when the VSTBY is power-on.
(2) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(3) HRST bit in the SWUC is enabled.
(4) Bit 0 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The KBRST# output scheme is shown in Figure 6-22 on page 149.
Note it is another way to use GPIO output function to send KBRST# signal.

Figure 6-22. KBRST# Output Scheme



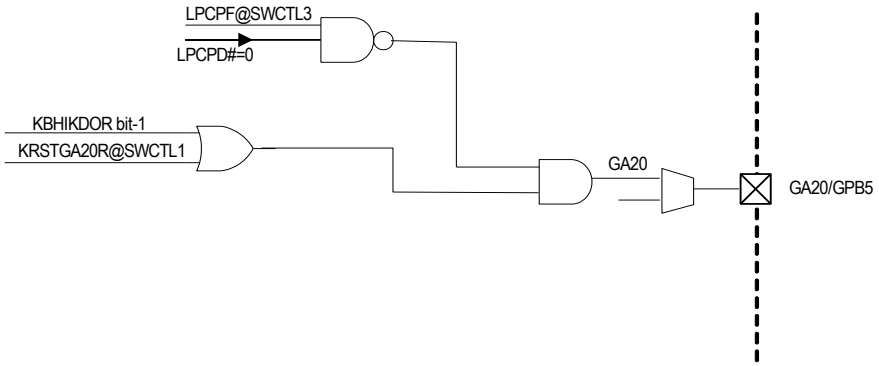
- **GA20 Signal**

In the chip, the GA20 is connected to a GPIO signal that is configured as output. Port GPB5 is recommended to be used as GA20 since its initial state is output driving high.
EC can assert the GA20 signal state by
1. Modifying GPB5 in GPIO register
2. Writing 1 to LPCPF in SWCTL3 register and GA20 signal will be asserted while LPCPD# signal is active.

The GA20 signal will be active in the following conditions:
(1) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(2) Bit-1 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The GA20 output scheme is shown in Figure 6-23 on page 149.
Note it is another way to use GPIO output function to send GA20 signal.

Figure 6-23. GA20 Output Scheme



- **Host Configuration Address Option**

The contents of SWCBAHR and SWCBALR change only during VSTBY Power -Up reset. To update the base address of the PNPCFG registers, refer to the followings:
1. Clear HCAV bit in SWCTL1 register by writing 1 to it.
2. Write the lower byte of the address to SWCBALR (LSB has to be cleared).
3. Write the higher byte of the address to SWCBAHR.
4. Set HCAL bit to prevent the unintended change in the SWCBALR and SWCBAHR register.

6.5.4 Host Interface Registers

The registers of SWUC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. SWUC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below.

Table 6-31. Host View Register Map, SWUC

7 0	Offset
Wake-Up Event Status Register (WKSTR)	00h
Wake-Up Enable Register (WKER)	02h
Wake-Up Signals Monitor Register (WKSMR)	06h
Wake-Up ACPI Status Register (WKACPIR)	07h
Wake-Up SMI# Enable Register (WKSMIER)	13h
Wake-Up Interrupt Enable Register (WKIRQER)	15h

6.5.4.1 Wake-Up Event Status Register (WKSTR)

The register is used to monitor the status of wake-up events. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/WC	0b	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0b	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming the HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0 and writing 1 to this bit, the value of this bit will be inverted. When HSECM=1 and writing 1 to this bit, the bit is set to 1. The bit will be cleared when the SIRQS bit in SWUC Host Event Status Register (SWCHSTR) is written to 1. 0: Event is not active. 1: Event is active.
5-4	R	00b	**Reserved**
3	R/WC	0b	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	0b	**Reserved**
1	R/WC	0b	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0b	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.5.4.2 Wake-Up Event Enable Register (WKER)

The register is used to enable the individual wake-up events to generate PWUREQ# interrupt. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Module IRQ Event Enable (MIRQE)** 0: Disable 1: Enable
6	R/W	0b	**Software IRQ Event Enable (SIRQE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event Enable (RINGE)** 0: Disable 1: Enable
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event Enable (RI2E)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event Enable (RI1E)** 0: Disable 1: Enable

6.5.4.3 Wake-Up Signals Monitor Register (WKSMR)

The register is used to monitor the value of the SMI# and PWUREQ# signals and identify the generated source. This register is a read-only register.

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5	R	0b	**PWUREQ# Output from SWUC (PWUREQOS)** 0: PWUREQ# output from SWUC is low. 1: PWUREQ# output from SWUC is high.
4	R	0b	**PWUREQ# Signal Status (PWUREQS)** 0: PWUREQ# signal is low. 1: PWUREQ# signal is high.
3	R	0b	**SMI# Output from PMC2 (PM2SMI)** 0: SMI# output from PM channel 2 is low. 1: SMI# output from PM channel 2 is high.
2	R	0b	**SMI# Output from PMC1 (PM1SMI)** 0: SMI# output from PM channel 1 is low. 1: SMI# output from PM channel 1 is high.
1	R	0b	**SMI# Output from SWUC (SWCSMI)** 0: SMI# output from SWUC is low. 1: SMI# output from SWUC is high.
0	R	0	**SMI# Signal Status (SMIS)** 0: SMI# signal is low. 1: SMI# signal is high.

6.5.4.4 Wake-Up ACPI Status Register (WKACPIR)

The register is used to monitor the status of ACPI. When this register is read, its value always returns 00h.

Address Offset: 07h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5	R/W	0b	**Change to S5 State (S5)** The host uses this bit to request the EC to change the ACPI S5 state. 0: Not request to change S5 state. 1: Request to change S5 state.
4	R/W	0b	**Change to S4 State (S4)** The host uses this bit to request the EC to change the ACPI S4 state. 0: Not request to change S4 state. 1: Request to change S4 state.
3	R/W	0b	**Change to S3 State (S3)** The host uses this bit to request the EC to change the ACPI S3 state. 0: Not request to change S3 state. 1: Request to change S3 state.
2	R/W	0b	**Change to S2 State (S2)** The host uses this bit to request the EC to change the ACPI S2 state. 0: Not request to change S2 state. 1: Request to change S2 state.
1	R/W	0b	**Change to S1 State (S1)** The host uses this bit to request the EC to change the ACPI S1 state. 0: Not request to change S1 state. 1: Request to change S1 state.
0	R	0b	**Reserved**

6.5.4.5 Wake-Up SMI# Enable Register (WKSMIER)

The register is used to enable the individual wake-up events to generate SMI# interrupt. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 13h

Bit	R/W	Default	Description
7	R/W	0b	**Reserved**
6	R/W	0b	**Software IRQ Event to SMI# Enable (SSMIE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event to SMI# Enable (RINGSMIE)** 0: Disable 1: Enable
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event to SMI# Enable (RI2SMIE)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event to SMI# Enable (RI1SMIE)** 0: Disable 1: Enable

6.5.4.6 Wake-Up IRQ Enable Register (WKIRQER)

The register is used to enable the individual wake-up events to generate the interrupt signal that is assigned by SWUC. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 15h

Bit	R/W	Default	Description
7	R/W	0b	**Reserved**
6	R/W	0b	**Software IRQ Event to IRQ Enable (SIRQE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event to IRQ Enable (RINGIRQE)** 0: Disable 1: Enable
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event to IRQ Enable (RI2IRQE)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event to IRQ Enable (RI1IRQE)** 0: Disable 1: Enable

6.5.5 EC Interface Registers

The registers of SWUC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal CPU processor. The base address for SWUC is 1400h.
These registers are listed below.

Table 6-32. EC View Register Map, SWUC

7 0	Offset
SWUC Control Status 1 Register (SWCTL1)	00h
SWUC Control Status 2 Register (SWCTL2)	02h
SWUC Control Status 3 Register (SWCTL3)	04h
SWUC Host Configuration Base Address Low Byte Register (SWCBALR)	08h
SWUC Host Configuration Base Address High Byte Register (SWCBAHR)	0Ah
SWUC Interrupt Enable Register (SWCIER)	0Ch
SWUC Host Event Status Register (SWCHSTR)	0Eh
SWUC Host Event Interrupt Enable Register (SWCHIER)	10h

6.5.5.1 SWUC Control Status 1 Register (SWCTL1)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is power-up. Bit 0 is only cleared when the warm reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1b	**KB Reset/GA20 Routing (KRSTGA20R)** 0: Enable routing bit-0 of KBHIKDOR as KBRST# source Enable routing bit-1 of KBHIKDOR as GA20 source 1: Disable above
6	R/W	0b	**Reserved**
5	R/W	0b	**Host Software Event Clear Mode (HSECM)** This bit is used to control the clear mode of SIRQS bit at the Wake-Up Event Status Register (WKSTR).
4	R/W	0b	**Host Configuration Address Lock (HCAL)** When the bit is written to 1, the Host Configuration Address and the bit will be locked. The bit is only cleared at the following condition: VSTBY power-up or watchdog reset.
3	R/WC	0b	**Host Configuration Address Valid (HCAV)** This bit is set after writing SWCBAHR register. 1: Indicate Host Configuration Base Address stored in SWCBALR and SWCBAHR registers are valid. 0: SWCBALR and SWCBAHR registers are not valid. The bit can be cleared by writing to 1.
2	R	0b	**LPC Reset Active (LPCRST)** 0: LPCRST# is inactive. 1: LPCRST# is active.
1	R	-	**VCC Power On (VCCPO)** 0: VCC is power-off. 1: VCC is power-on. See also VCCDO bit in RSTS register in 7.17.4.5 on page 441.
0	R/W	-	**Host Reset Active (HRST)** When this bit is 1, the KBRST# is active to generate one host software reset.

6.5.5.2 SWUC Control Status 2 Register (SWCTL2)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is power-up and LPCRST# is active.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/WC	0b	**Super I/O Configuration SIOPWR Power Supply Off (SCRDPSO)** The bit is used to monitor the Power Supply Off (PWRSLY) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the bit and the interrupt signal caused by the value change in this bit. A write of 0 to this bit is ignored.
6	R/WC	0b	**Super I/O Configuration SIOPWR Power Button Mode (SCRDPBM)** The bit is used to monitor the Power Button Mode (PWRBTN) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the interrupt signal caused by the value change in this bit. A write of 0 to this bit is ignored.
5-1	R/WC	00000b	**ACPI request S5-1 (ACPIRS5-1)** These bits are used to monitor the S5-1 bit at the Wake-Up ACPI Status Register (WKACPIR). When the bit is written to 1, clear the bit and the interrupt signal caused by ACPI. A write of 0 to this bit is ignored.
0	R/WC	0b	**ACPI request S0 (ACPIRS0)** If all S5-1 bits at the WKACPIR are written to 0, the bit will be set to 1. The bit will be cleared if the bit is written to 1.

6.5.5.3 SWUC Control Status 3 Register (SWCTL3)

The register is used to control the individual wake-up action on SWUC. The register will only be cleared when the VSTBY power is power-up.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	R	00h	**Reserved**
2	R/WC	0b	**RTCT Alarm Active (RTCTAL)** When the RTCT alarm is active, the bit will be set to 1. The bit can be cleared by writing 1 to it.
1	R/W	0b	**LPC Power Fail Turn Off KBRST# and GA20 (LPCPF)** If the bit is set to 1, the KBRST# and GA20 will be forced to low when the LPCPD# signal is active.
0	R/W	1b	**Host Reset Active During VSTBY Power-Up (HRSTA)** If the bit is set to 1, the KBRST# signal will be active when the LPC cycle is active until VSTBY Power-Up Reset is finished. Writing data to this bit is ignored if HCAL bit is set.

6.5.5.4 SWUC Host Configuration Base Address Low Byte Register (SWCBALR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-6 on page 72 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address Low Byte (BALB)**

6.5.5.5 SWUC Host Configuration Base Address High Byte Register (SWCBAHR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-6 on page 72 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address High Byte (BAHB)**

6.5.5.6 SWUC Interrupt Enable Register (SWCIER)

The register is used to enable the individual interrupt source on SWUC. The interrupt can be cleared by clearing the status bit or masking the source. On the other hand, the register will be cleared when the warm reset is active.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0b	**Enable Interrupt from Super I/O Configuration SIOPWR Power Supply Off (EISCRDPSO)** 1: Generate high-level interrupt when the SCRDPSO bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
6	R/W	0b	**Enable Interrupt from Super I/O Configuration SIOPWR Power Button Mode (EISCRDPBM)** 1: Generate high-level interrupt when the SCRDPBM bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
5-1	R/W	00000b	**Enable Interrupt from ACPI Request S5-1 (EIACPIRS5-1)** 1: Generate high-level interrupt when the ACPIRS5-1 bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
0	R/W	0b	**Enable Interrupt from RTCT Alarm Active (EIRTCTA)** 1: Generate high-level interrupt when the RTCAL bit in SWUC Control Status 3 Register (SWCTL3) is changed to 1. 0: Disable the interrupt source.

6.5.5.7 SWUC Host Event Status Register (SWCHSTR)

The information of this register is mirror as the Wake-Up Event Status Register (WKSTR). The status bits can be cleared by writing to the corresponding bit in the two registers. The register will be cleared when the VSTBY power is power-up, or the host software reset occurs.

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R/WC	0b	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0b	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0, this bit is set to 1 when SIRQS toggles to 1 in WKSTR register. When HSECM=1 and this bit is set to 1 while writing 1 to SIRQS in WKSTR register. This bit will be cleared by writing 1 to it. 0: Event is not active. 1: Event is active.
5-4	R	00b	**Reserved**
3	R/WC	0b	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	0b	**Reserved**
1	R/WC	0b	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0b	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.5.5.8 SWUC Host Event Interrupt Enable Register (SWCHIER)

The register is used to enable the individual wake-up events to generate one interrupt to the EC CPU via WU26 of WUC. The register will be cleared when the warm reset occurs.

Address Offset: 10h

Bit	R/W	Default	Description
7	R/W	0b	**Module IRQ Event Enable (MIRQEE)** 0: Disable 1: Enable
6	R/W	0b	**Software IRQ Event Enable (SIRQEE)** 0: Disable 1: Enable
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event Enable (RINGEE)** 0: Disable 1: Enable
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event Enable (RI2EE)** 0: Disable 1: Enable
0	R/W	0b	**RI1# Event Enable (RI1EE)** 0: Disable 1: Enable

6.6 Keyboard Controller (KBC)

6.6.1 Overview

This Keyboard Controller supports a standard keyboard and mouse controller interface.

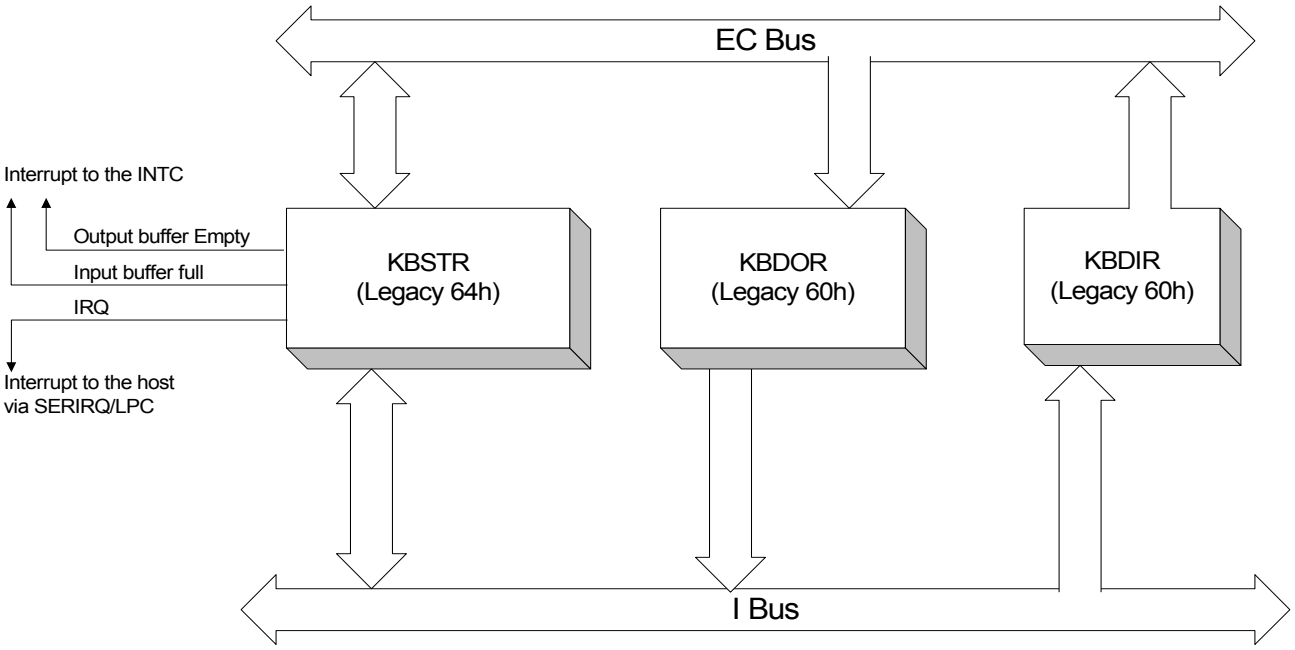
6.6.2 Features

- Compatible with the legacy 8042 interface keyboard controller.
- Supports two standard registers for programming: Command/Data Register and Status Register.
- Automatically generates interrupts to the host side and EC side when the KBC status is changed.

6.6.3 Functional Description

This Keyboard Controller is compatible with the legacy 8042 interface keyboard controller.

Figure 6-24. KBC Host Interface Block Diagram



Status
The host processor can read the status of KBC from the KBC Status Register. The internal CPU can read the status of KBC from the KBC Host Interface Keyboard/Mouse Status Register.

Host Write Data to KBC Interface
When writing to address 60h or 64h (programmable), the IBF bit in the KBC Status Register is set and A2 bit in the KBC Status Register indicates CPU whose address was written. When writing to address 60h, A2 bit is 0. When writing to address 64h, A2 bit is 1.
EC CPU can identify that the input buffer is full by either polling IBF bit in the Status register or detecting an interrupt (INT24) if the interrupt is enabled. EC CPU can read the data from the KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR), and the IBF bit in the Status Register is cleared.

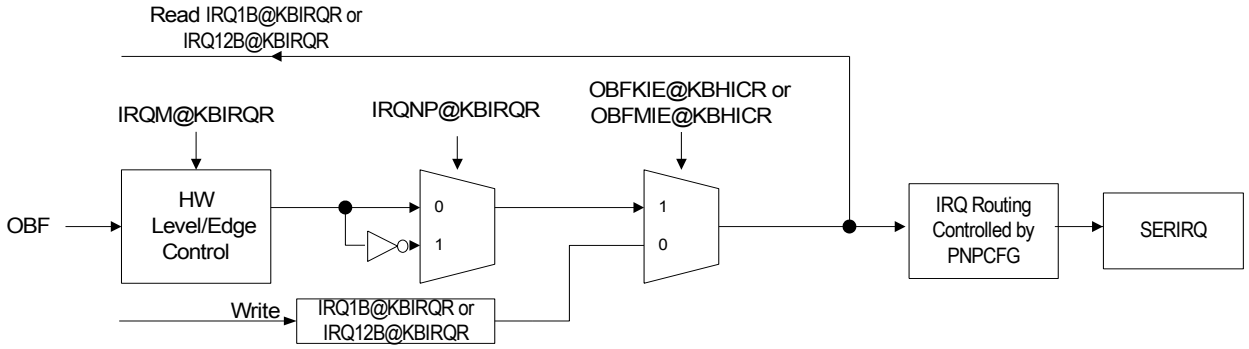
EC CPU Write Data to KBC Interface
EC CPU can write data to the KBC when it needs to send data to the host. When EC CPU writes data to the KBC Host Interface Keyboard Data Output Register (KBHIKDOR), the OBF bit in the Status Register is set. If the IRQ1 interrupt is enabled, the IRQ1 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When EC CPU writes data to the KBC Host Interface Mouse

Data Output Register (KBHIMDOR), the OBF bit in the Status Register is set. If the IRQ12 interrupt is enabled, the IRQ12 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When the Output Buffer Empty interrupt to INTC (INT2) is enabled, the interrupt signal is set high if the output buffer is empty.

Interrupts

There are two interrupts (Input Buffer Full Interrupt and Output Buffer Empty) connected to the INTC.
There are two interrupts (IRQ1 and IRQ12) connected to the host side (SERIRQ).
The IRQ numbers of KBC are programmable and use IRQ1 and IRQ12 as abbreviations in this section.

Figure 6-25. IRQ Control in KBC Module



GA20 and KBRST#

Refer to section 6.5.3.4 on page 148.

6.6.4 Host Interface Registers

The registers of KBC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor.
The KBC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. For compatibility issue, the two I/O Port Base Addresses of KBC/Keyboard are suggested to configure at 60h and 64h.

These registers are listed below.

Table 6-33. Host View Register Map, KBC

7 — 0	Offset
KBC Data Input Register (KBDIR)	Legacy 60h
KBC Data Output Register (KBDOR)	Legacy 60h
KBC Command Register (KBCMDR)	Legacy 64h
KBC Status Register (KBSTR)	Legacy 64h

Legacy 60h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 64h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-7 on page 72.

6.6.4.1 KBC Data Input Register (KBDIR)

When the host processor is writing this register, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be cleared. If the IBFCIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the write action will cause one interrupt to CPU processor via INT24 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	W	-	**KBC Data Input (KBDI)** The data is used to output for Keyboard/Mouse.

6.6.4.2 KBC Data Output Register (KBDOR)

When the host processor is reading this register, The OBF bit in KBC Status Register (KBSTR) will be cleared. The reading access will also clear the interrupt for host processor when the IRQM bits of KBC Interrupt Control Register (KBIRQR) are programmed to be at level mode. If the OBECIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the read action will cause one interrupt to CPU processor via INT2 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	R	-	**KBC Data Output (KBDO)** The data comes from the Keyboard/Mouse source.

6.6.4.3 KBC Command Register (KBCMDR)

When the register is written, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be set.

Address Offset: 00h for I/O Port Base Address 1, Legacy 64h

Bit	R/W	Default	Description
7-0	W	-	**KBC Command (KBCMD)** The command data is used to output for Keyboard/Mouse.

6.6.4.4 KBC Status Register (KBSTR)

The host processor uses the register to monitor the status of KBC. The same information is similar to the KBC Host Interface Keyboard/Mouse Status Register (KBHISR). It is used by the internal CPU.

Address Offset: 01h for I/O Port Base Address 0, Legacy 64h

Bit	R/W	Default	Description
7-4	R	0h	**Programming Data 3-0 (PD3-0)** The data is used by the CPU firmware to be the general-purpose setting.
3	R	0b	**A2 Address (A2)** The bit is used to keep the A2 address information of the last write operation that the host processor accessed the KBC.
2	R	0b	**Programming Data II (PDII)** The function is the same as the PD3-0.
1	R	0b	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when the KBDIR or KBCMDR is read by the CPU firmware.
0	R	0b	**Output Buffer Full (OBF)** When the EC CPU is writing data to KBDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host processor.

6.6.5 EC Interface Registers

The registers of KBC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal CPU processor. The base address for KBC is 1300h.

These registers are listed below

Table 6-34. EC View Register Map, KBC

7	0	Offset
KBC Host Interface Control Register (KBHICR)		00h
KBC Interrupt Control Register (KBIRQR)		02h
KBC Host Interface Keyboard/Mouse Status Register (KBHISR)		04h
KBC Host Interface Keyboard Data Output Register (KBHIKDOR)		06h
KBC Host Interface Mouse Data Output Register (KBHIMDOR)		08h
KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)		0Ah

.

6.6.5.1 KBC Host Interface Control Register (KBHICR)

Address Offset: 00h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear KBC IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear KBC OBF.
5	R/W	0b	**IBF/OBF Clear Mode Enable (IBFOBFCME)** 0b: IBF of KBC/PMC is cleared if EC reads its corresponding data register. OBF of KBC/PMC is cleared if the host reads its corresponding data register. 1b: IBF of KBC/PMC is cleared if write-1 to its corresponding CIBF bit. OBF of KBC/PMC is cleared if the host reads its corresponding data or write-1 to its corresponding CIBF bit.
4	R/W	0b	**PM Channel 1 Host Interface Interrupt Enable (PM1HIE)** 0: The IRQ11 is controlled by the IRQ11B bit in KBC Interrupt Control Register (KBIRQR). 1: Enables the interrupt to the host side via SERIRQ for PM channel 1 when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
3	R/W	0b	**Input Buffer Full CPU Interrupt Enable (IBFCIE)** The bit is used to enable the interrupt to CPU for Keyboard/Mouse when the input buffer is full via INT24 of INTC.
2	R/W	0b	**Output Buffer Empty CPU Interrupt Enable (OBECIE)** The bit is used to enable the interrupt to CPU for Keyboard/Mouse when the output buffer is empty via INT2 of INTC.
1	R/W	0b	**Output Buffer Full Mouse Interrupt Enable (OBFMIE)** 0: The IRQ12 is controlled by the IRQ12B bit in KBIRQR. 1: Enables the interrupt to mouse driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
0	R/W	0b	**Output Buffer Full Keyboard Interrupt Enable (OBFKIE)** 0: The IRQ1 is controlled by the IRQ1B bit in KBIRQR. 1: Enables the interrupt to keyboard driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.

6.6.5.2 KBC Interrupt Control Register (KBIRQR)

Address Offset: 02h

Bit	R/W	Default	Description
7	R	0b	**Reserved**
6	R/W	0b	**Interrupt Negative Polarity (IRQNP)** The bit is enabled, and then the interrupt level is inverted.
5-3	R/W	0b	**Interrupt Mode (IRQM)** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is high and a negative pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from SCIPM field in PMCTL register and SMIPM field in PMIC register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	1b	**IRQ11 Control Bit (IRQ11B)** When the PM1HIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ11 signal. The bit can be used to monitor the status of IRQ11 signal. Reading this bit returns the status of IRQ11 signal, so the read value is not equal to the written value directly.
1	R/W	1b	**IRQ12 Control Bit (IRQ12B)** When the OBFMIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ12 signal. The bit can be used to monitor the status of IRQ12 signal. Reading this bit returns the status of IRQ12 signal, so the read value is not equal to the written value directly.
0	R/W	1b	**IRQ1 Control Bit (IRQ1B)** When the OBFKIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ1 signal. The bit can be used to monitor the status of IRQ1 signal. Reading this bit returns the status of IRQ1 signal, so the read value is not equal to the written value directly.

6.6.5.3 KBC Host Interface Keyboard/Mouse Status Register (KBHISR)

The CPU firmware uses the register to monitor the status of KBC. It can use bit 7-4 and bit 2 to send the information to the host processor. The data of this register is the same as the data of KBC Status Register (KBSTR).

Address Offset: 04h

Bit	R/W	Default	Description
7-4	R/W	0h	**Programming Data 3-0 (PD3-0)** The data is used by the CPU firmware to be the general-purpose setting.
3	R	0b	**A2 Address (A2)** The bit is used to keep the A2 address information of the write operation while the host processor accesses the KBC.
2	R/W	0b	**Programming Data II (PDII)** The function is the same as PD3-0.
1	R	0b	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when KBHIDIR is read by the CPU firmware.
0	R	0b	**Output Buffer Full (OBF)** When CPU is writing data to KBHIKDOR and KBHIMDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host.

6.6.5.4 KBC Host Interface Keyboard Data Output Register (KBHIKDOR)

The CPU firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	W	-	**KBC Keyboard Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.6.5.5 KBC Host Interface Mouse Data Output Register (KBHIMDOR)

The CPU firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	W	-	**KBC Mouse Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.6.5.6 KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)

The CPU firmware can read the register to get the data of the KBC Data Input Register (KBDIR). Besides, the action will clear the IBF bit in the KBC Status Register (KBSTR). If the IBFCIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**KBC Keyboard/Mouse Data Input (KBKMDI)** The data is the same as the data of KBC Data Input Register (KBDIR).

6.7 Power Management Channel (PMC)

6.7.1 Overview

The power management channel is defined in ACPI specification and used as a communication channel between the host processor and embedded controller.

6.7.2 Features

- Supports five PM channels
- Supports compatible mode for channel 1
- Supports enhanced mode for all channels
- Supports shared and private interface
- Supports Command/Status and Data ports
- Supports IRQ/SMI#/SCI# generation

6.7.3 Functional Description

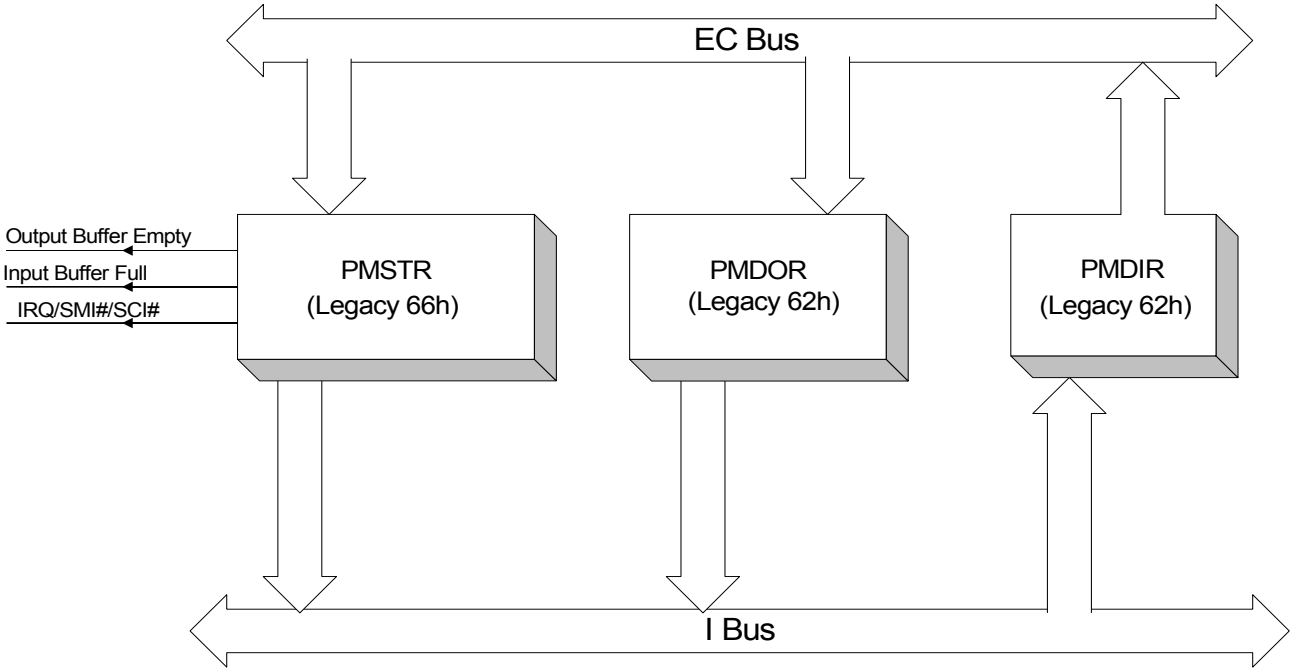
To generate the SCI# and SMI# interrupts to the host

6.7.3.1 General Description

The PM channel supports two operation modes: one is called Compatible mode that is available for channel 1 only. The other is called Enhanced mode. PMC is available for all channels. The PM channel provides four registers: PMDIR, PMDOR, PMCMDR and PMSTR for communication between the EC and host side. The PMDIR register can be written to by the host and read by the EC. The PMDOR register can be written to by the EC and read by the host. The PMCMDR/PMSTR register can be read by both the EC and Host side.

The PMC host interface block diagram is shown below.

Figure 6-26. PMC Host Interface Block Diagram

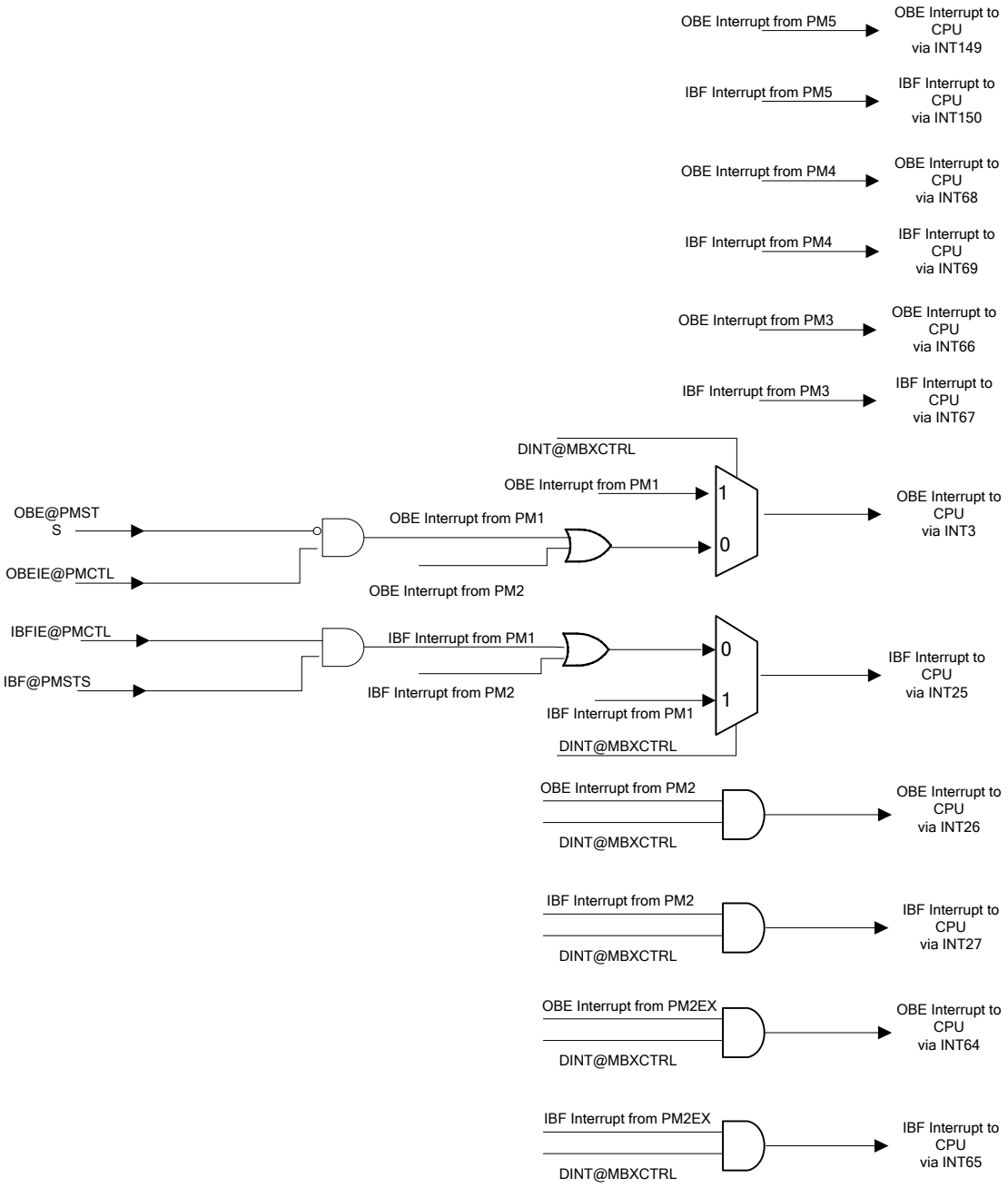


EC Interrupts

Two interrupts (IBF and OBF) are connected to INTC. These interrupts are enabled by OBEIE and IBFIE in PMnCTL register respectively.

The diagram of PMC interrupt to EC CPU via INT3/INT25/INT26/INT27/INT64-INT69/INT149/INT150 of INTC is show below.

Figure 6-27. EC Interrupt Request for PMC



Host Interrupt
The EC can select to access to different address space to generate IRQ, SMI# or SCI# interrupt when either IBF or OBF is set.

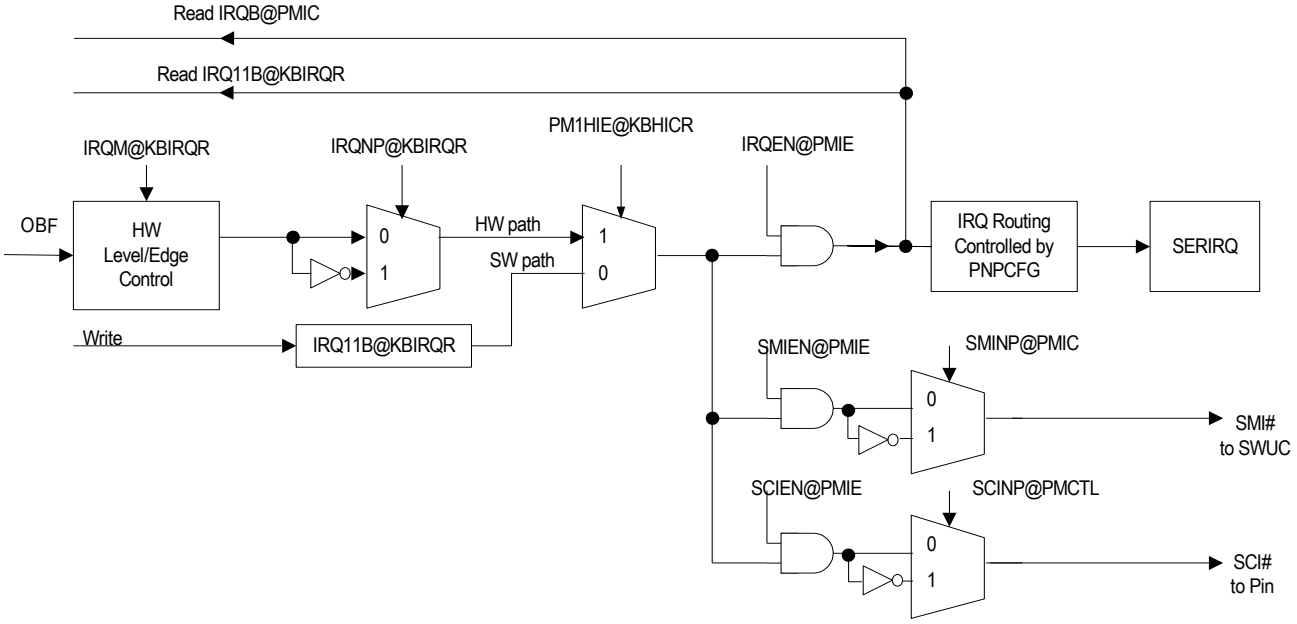
The IRQ numbers of PMC are programmable and use IRQ11 as the abbreviation in the following section. The abbreviation, n, represents channel 1 and/or channel 2 of this register.

6.7.3.2 Compatible Mode

When IRQ numbers in host configuration register are assigned by host software, and the interrupt can be generated either by hardware via PM1HIE in KBHICR register or by programming KBIRQR register. In Normal Polarity mode (IRQNP in KBIRQR register is cleared), IT5121 supports legacy level for PM compatible mode interrupt. When a level interrupt is selected (IRQM in KBIRQR register is cleared), the interrupt signal is asserted when the OBF flag has been set, which is still asserted until the output buffer is read (i.e.,OBF flag is cleared). The EC can control the interrupts generated by the PM channel to the one as follows:
IRQ signal to LPC/SERIRQ, when IRQEN bit in PMnIE register is set.
SMI# output to SWUC, when SMIEN bit in PMnIE register is set.
SCI# signal, using the SCI# output, when SCIEN bit in PMnIE register is set.

The IRQ/SCI#/SMI# control diagram in PMC compatible mode is shown below.

Figure 6-28. IRQ/SCI#/SMI# Control in PMC Compatible Mode

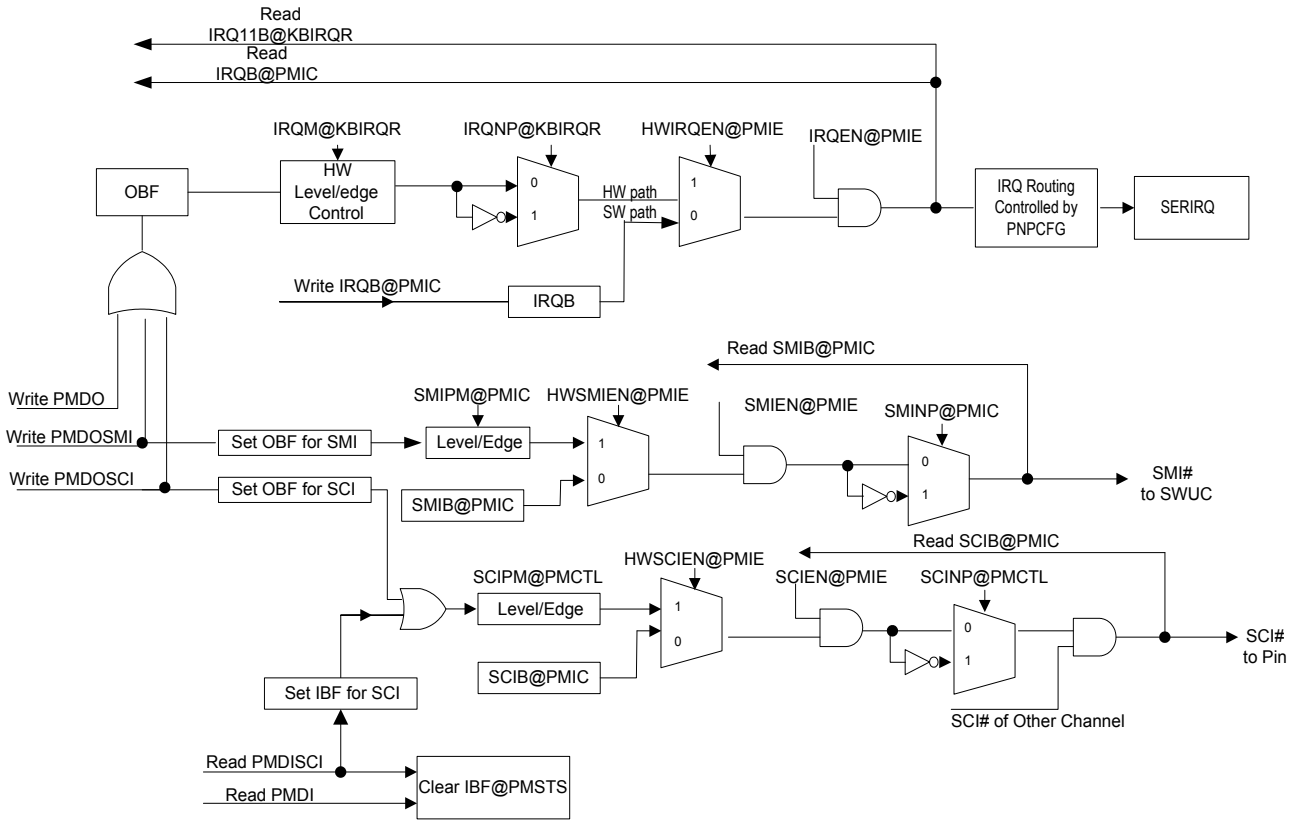


6.7.3.3 Enhanced PM mode

Enhanced PM mode is activated when APM is set to 1 in PMnCTL register. The generated IRQ, SMI# or SCI# interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PMnIE register. SCI# and SMI# are generated when EC writes to the Data output buffer. SCI# is generated when EC reads the Data Input buffer. Different data register generates different interrupt. The OBF flag in PMnSTS register is set and both SMI# and SCI# interrupts are deasserted when data is written to PMnDO register. The OBF interrupt of SMI# is generated when PMnDOSMI register is written into data. The internal OBF flag of SMI# is cleared when OBF flag is cleared. The OBF interrupt of SCI# is generated When PMnDOSCI register is written into data.OBF_SCI# which is cleared when OBF is cleared.
The IBF flag is cleared and SCI# interrupt is generated when PMnDISCI register is read out data. The IBF flag is cleared and SCI# interrupt is not asserted when PMnDI register is read out data.

The IRQ/SCI#/SMI# control diagram in PMC enhanced mode is shown below.

Figure 6-29. IRQ/SCI#/SMI# Control in PMC Enhanced Mode



6.7.3.4 PMC2EX

There is a channel 2 extended (PMC2EX) mailbox (MBX) function based on PMC channel 2, which is constructed by a 16-byte mailbox shared with BRAM. See also Figure 7-33 on page 460.

This 16-byte mailbox can be accessed from both the EC side (named MBXEC0-15) and host side (MBXH0-15). In the EC side, MBXEC0-15 is always located in PMC module offset F0h-FFh and shared with the topmost 16-byte in BRAM.
In the host side, MBXH0-15 address is based on the descriptor 2 of Power Management I/F Channel 2 logic device inside LPC I/O space. (Refer to section 6.3.13.6 and 6.3.13.7 on page 102)

The PMC2EX (channel 2 extended) shares the same interrupt generation resource and registers (offset 10h-18h).

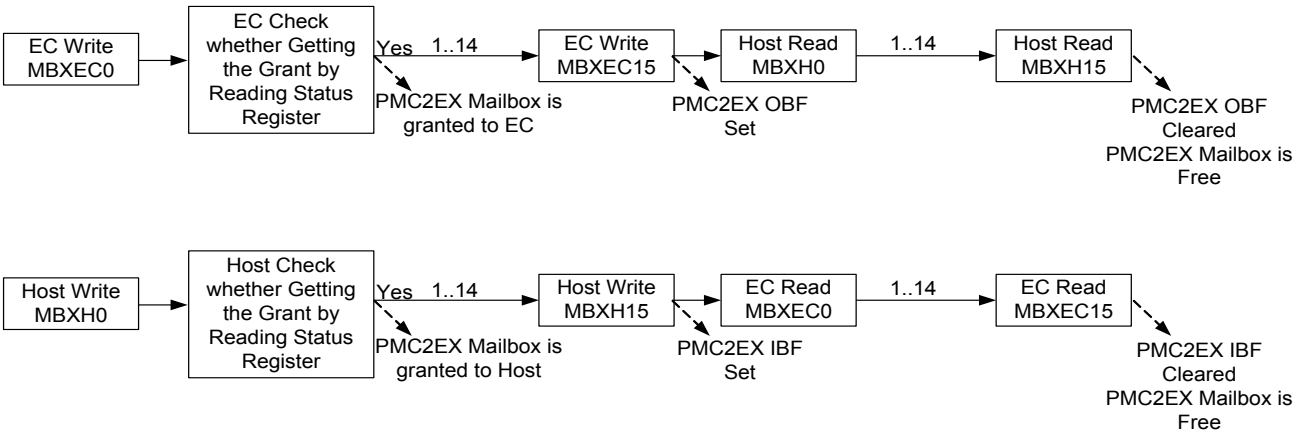
For registers, PMC2EX shares the same registers (offset 10h-18h) and has its dedicated MBXCTRL register (offset 19h).

For interrupt generation, PMC2EX shares the same interrupt logic with channel 2. If MBXEN is set, IBF/OBF interrupt source of PMC2EX is ORed with channel 2.

The EC/host side should check whether to get the grant from the internal arbiter after writing to MBXEC0/MBXH0 (respectively).

The typical PMC2EX mailbox operation is described below.

Figure 6-30. Typical PMC2EX Mailbox Operation

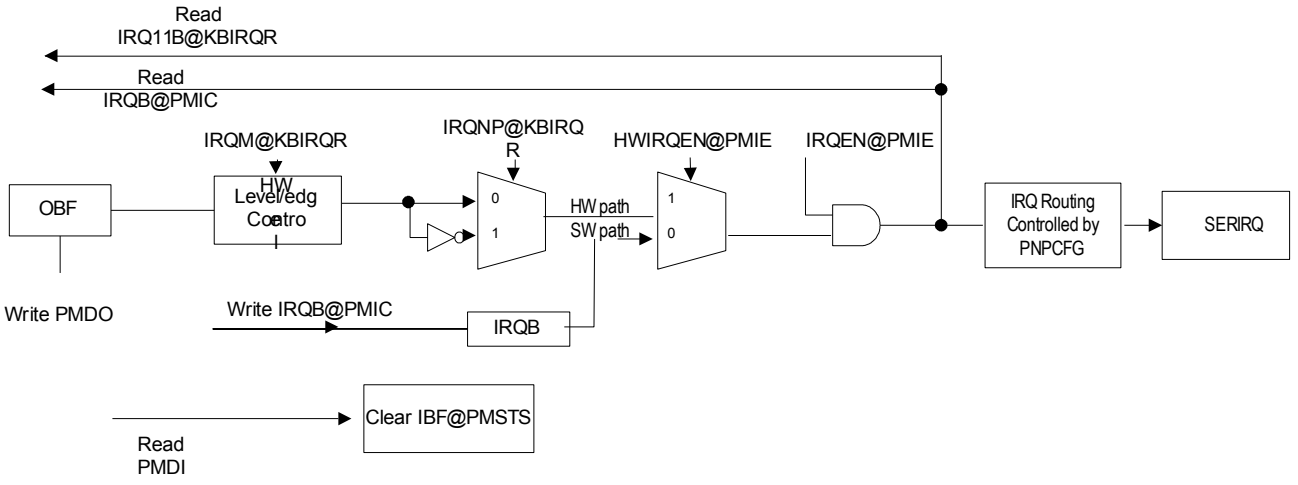


6.7.3.5 PMC3/4/5

Only Enhanced PM mode is activated in PM channel 3/4/5 and only IRQ interrupt is generated. The generated IRQ interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PM3IE/PM4IE/PM5IE register.The OBF flag in PM3STS/PM4STS/PM5STS register is set when data is written to PM3DO/PM4DO/PM5DO register. The IBF flag is cleared when PMnDI register is read out data.

The IRQ control diagram in PMC3/PMC4/PMC5 is shown below.

Figure 6-31. IRQ Control in PM Channel 3/4/5



6.7.4 Host Interface Registers

The registers of PMC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The PMC Channel 1 and 2 reside at LPC I/O space and the base address can be configured through LPC PNPCFG registers. For compatibility issue, the two I/O Port Base Addresses of channel 1 are suggested to configure at 62h and 66h.

These registers are listed below.

Table 6-35. Host View Register Map, PMC

7 — 0	Offset
PMC Data Input Register (PMDIR)	Legacy 62h
PMC Data Output Register (PMDOR)	Legacy 62h
PMC Command Register (PMCMDR)	Legacy 66h
PMC Status Register (PMSTR)	Legacy 66h

Legacy 62h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 66h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-7 on page 72.

6.7.4.1 PMC Data Input Register (PMDIR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	**Data Input Register Bit [7:0] (DIRB)** This is the data input register for power management channel data communication between the host and EC side. When the host writes this port, data is written to PMDIR register and EC CPU can read it. Notice that when the Command/Status register is written, the data is also stored into PMDIR register. Users must read A2 to decide whether the PMDIR data is data or command.

6.7.4.2 PMC Data Output Register (PMDOR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	R	00h	**Data Output Register Bit [7:0] (DORB)** This is the data output register for power management channel data communication between the host and EC. When the host reads this port, data is read from PMDOR register and EC CPU can write it.

6.7.4.3 PMC Command Register (PMCMDR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	**Command Register Bit [7:0] (CRB)** The port is written by the host when A2 = 1 in PMSTR register.

6.7.4.4 Status Register (PMSTR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 1 and channel 2 with MBXEN cleared: This is a general purpose flag used for signaling between the host and EC side. When used as ACPI PM channel, the predefined meaning is burst, SCI# event and SMI# event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents that what is written by the host is data. If this bit is 1, it represents that what is written by the host is command.
2	R/W	0b	**General Purpose flag (GPF)** This bit is used as a general-purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data input register or command register and is cleared when the EC CPU reads the data input register. Notice that the write to data input register or command register by the host all trigger this flag and EC must use A2 to distinguish whether the write is a command or data.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data output port and is cleared when the host reads the data out buffer.

6.7.5 EC Interface Registers

The registers of PMC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal CPU processor. The base address is 1500h.

These registers are listed below.

Table 6-36. EC View Register Map, PMC

7 0	Offset
Host Interface PM Channel 1 Status (PM1STS)	00h
Host Interface PM Channel 1 Data Out Port (PM1DO)	01h
Host Interface PM Channel 1 Data Out Port with SCI# (PM1DOSCI)	02h
Host Interface PM Channel 1 Data Out Port with SMI# (PM1DOSMI)	03h
Host Interface PM Channel 1 Data In Port (PM1DI)	04h
Host Interface PM Channel 1 Data In Port with SCI# (PM1DISCI)	05h
Host Interface PM Channel 1 Control (PM1CTL)	06h
Host Interface PM Channel 1 Interrupt Control (PM1IC)	07h
Host Interface PM Channel 1 Interrupt Enable (PM1IE)	08h
Host Interface PM Channel 2 Status (PM2STS)	10h
Host Interface PM Channel 2 Data Out Port (PM2DO)	11h
Host Interface PM Channel 2 Data Out Port with SCI# (PM2DOSCI)	12h
Host Interface PM Channel 2 Data Out Port with SMI# (PM2DOSMI)	13h
Host Interface PM Channel 2 Data In Port (PM2DI)	14h
Host Interface PM Channel 2 Data In Port with SCI# (PM2DISCI)	15h
Host Interface PM Channel 2 Control (PM2CTL)	16h
Host Interface PM Channel 2 Interrupt Control (PM2IC)	17h
Host Interface PM Channel 2 Interrupt Enable (PM2IE)	18h
Mailbox Control (MBXCTRL)	19h
Host Interface PM Channel 3 Status (PM3STS)	20h
Host Interface PM Channel 3 Data Out Port (PM3DO)	21h
Host Interface PM Channel 3 Data In Port (PM3DI)	22h
Host Interface PM Channel 3 Control (PM3CTL)	23h
Host Interface PM Channel 3 Interrupt Control (PM3IC)	24h
Host Interface PM Channel 3 Interrupt Enable (PM3IE)	25h
Host Interface PM Channel 4 Status (PM4STS)	30h
Host Interface PM Channel 4 Data Out Port (PM4DO)	31h
Host Interface PM Channel 4 Data In Port (PM4DI)	32h
Host Interface PM Channel 4 Control (PM4CTL)	33h
Host Interface PM Channel 4 Interrupt Control (PM4IC)	34h
Host Interface PM Channel 4 Interrupt Enable (PM4IE)	35h
Host Interface PM Channel 5 Status (PM5STS)	40h
Host Interface PM Channel 5 Data Out Port (PM5DO)	41h
Host Interface PM Channel 5 Data In Port (PM5DI)	42h
Host Interface PM Channel 5 Control (PM5CTL)	43h
Host Interface PM Channel 5 Interrupt Control (PM5IC)	44h
Host Interface PM Channel 5 Interrupt Enable (PM5IE)	45h
16-byte PMC2EX Mailbox 0 (MBXEC0)	F0h
…	…
16-byte PMC2EX Mailbox 15 (MBXEC15)	FFh

6.7.5.1 PM Status Register (PMSTS)

This register is the same as the Status register in host side but reside in the EC side.

Address Offset: 00h/10h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 1 and channel 2 with MBXEN cleared: This is a general-purpose flag used for signaling between the host and EC. When used as ACPI PM channel, the predefined meaning is burst, SCI# event and SMI# event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents that what is written to the data port is data. If this bit is 1, it represents that what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general-purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereascleared when the host reads the data output buffer.

6.7.5.2 PM Data Out Port (PMDO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 01h/11h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out (PMDO[7:0])** This is the data output buffer.

6.7.5.3 PM Data Out Port with SCI# (PMDOSCI)

This register is the PMDOR buffer with SCI#. The data written to this register is stored in PMDOR. SCI# is generated upon write.

Address Offset: 02h/12h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out with SCI# (PMDOSCI[7:0])** This is the data output buffer with SCI#. Writing to this port will generate hardware SCI# if enabled.

6.7.5.4 PM Data Out Port with SMI# (PMDOSMI)

This register is the PMDOR buffer with SMI#. The data written to this register is stored in PMDOR. SMI# is generated upon write.

Address Offset: 03h/13h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out with SMI# (PMDOSMI[7:0])** This is the data output buffer with SMI#. Writing to this port will generate hardware SMI# if enabled.

6.7.5.5 PM Data In Port (PMDI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 04h/14h

Bit	R/W	Default	Description
7-0	R	00h	**PM Data In (PMDI[7:0])** This is the data input buffer.

6.7.5.6 PM Data In Port with SCI# (PMDISCI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer. Reading this register (EC) generates SCI#.

Address Offset: 05h/15h

Bit	R/W	Default	Description
7-0	R	00h	**PM Data In with SCI# (PMDISCI[7:0])** This is the data input buffer with SCI#. Reading this port will generate SCI# when enabled.

6.7.5.7 PM Control (PMCTL)

Address Offset: 06h/16h

Bit	R/W	Default	Description
7	R/W	0b	**Enhance PM Mode (APM)** Setting this bit to '1' enables the enhance PM mode. The interrupts (IRQ, SCI# or SMI#) are automatically generated by hardware operations if enabled.
6	R/W	1b	**SCI# Negative Polarity (SCINP)** Setting this bit to '1' causes the SCI# polarity inversed (low active).
5-3	R/W	0h	**SCI# Pulse Mode (SCIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.7.5.8 PM Interrupt Control (PMIC)

Address Offset: 07h/17h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	1b	**SMI# Negative Polarity (SMINP)** Setting this bit to '1' causes the SMI# polarity inversed.
5-3	R/W	000b	**SMI# Pulse Mode (SMIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000b: Level-triggered mode. 001b: Edge-triggered mode with 1-cycle pulse width. 010b: Edge-triggered mode with 2-cycle pulse width. 011b: Edge-triggered mode with 4-cycle pulse width. 100b: Edge-triggered mode with 8-cycle pulse width. 101b: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	0b	**Host SCI# Control Bit (SCIB)** This bit is the SCI# generation bit when hardware SCI# is disabled. Read always returns the current value of SCI#.
1	R/W	0b	**Host SMI# Control Bit (SMIB)** This bit is the SMI# generation bit when hardware SMI# is disabled. Read always returns the current value of SMI#.
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.9 PM Interrupt Enable (PMIE)

Address Offset: 08h/18h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC1/2 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC1/2 OBF.
5	R/W	0b	**Hardware SMI# Enable (HWSMIEN)** Setting this bit to '1' enables the SMI# generated by hardware control. Writing to the SMIB bit generates the SMI# if this bit is set to '0'.
4	R/W	0b	**Hardware SCI# Enable (HWSCIEN)** Setting this bit to '1' enables the SCI# generated by hardware control. Writing to the SCIB bit generates the SCI# if this bit is set to '0'.
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing to the IRQB bit generates the IRQ if this bit is set to '0'.
2	R/W	0b	**SMI# Enable (SMIEN)** Setting this bit to '1' enables the SMI# generated by this module.
1	R/W	0b	**SCI# Enable (SCIEN)** Setting this bit to '1' enables the SCI# generated by this module.
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7.5.10 Mailbox Control (MBXCTRL)

Address Offset: 19h

Bit	R/W	Default	Description
7	R/W	0b	**Mailbox Enable (MBXEN)** 1b: Enable 16-byte PMC2EX mailbox 0b: Otherwise
6	-	-	**Reserved**
5	R/W	0b	**Dedicated Interrupt (DINT)** 0b: INT3: PMC Output Buffer Empty Int INT25: PMC Input Buffer Full Int 1b: INT3: PMC1 Output Buffer Empty Int INT25: PMC1 Input Buffer Full Int INT26: PMC2 Output Buffer Empty Int INT27: PMC2 Input Buffer Full Int (All are High Level Trig)
4-0	-	-	**Reserved**

6.7.5.11 PMC3 Status Register (PM3STS)

This register is the same as the Status register in host side but resides in the EC side.

Address Offset: 20h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 3: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents what is written to the data port is data. If this bit is 1, it represents what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereas cleared when the host reads the data output buffer.

6.7.5.12 PMC3 Data Out Port (PM3DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	W	00h	**PM 3 Data Out (PM3DO[7:0])** This is the data output buffer.

6.7.5.13 PMC3 Data In Port (PM3DI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R	00h	**PMC3 Data In (PM3DI[7:0])** This is the data input buffer.

6.7.5.14 PMC3 Control (PM3CTL)

Address Offset: 23h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to ‘1’ enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.7.5.15 PMC3 Interrupt Control (PM3IC)

Address Offset: 24h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.16 PMC3 Interrupt Enable (PM3IE)

Address Offset: 25h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC3 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC3 OBF.
5-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to '0'.
2-1	-	0b	**Reserved**
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7.5.17 PMC4 Status Register (PM4STS)

This register is the same as the Status register in the host side but resides in the EC side.

Address Offset: 30h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 4: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents what is written to the data port is data. If this bit is 1, it represents what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes the data port or command port whereas cleared when the EC reads the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data port whereas cleared when the host reads the data output buffer.

6.7.5.18 PMC4 Data Out Port (PM4DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 31h

Bit	R/W	Default	Description
7-0	W	00h	**PM 4 Data Out (PM4DO[7:0])** This is the data output buffer.

6.7.5.19 PMC4 Data In Port (PM4DI)

This register is the PMDIR buffer. The written data or command by Host is stored in this buffer.

Address Offset: 32h

Bit	R/W	Default	Description
7-0	R	00h	**PMC4 Data In (PM4DI[7:0])** This is the data input buffer.

6.7.5.20 PMC4 Control (PM4CTL)

Address Offset: 33h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host's reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host's writing the data port or command port).

6.7.5.21 PMC4 Interrupt Control (PM4IC)

Address Offset: 34h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.22 PMC4 Interrupt Enable (PM4IE)

Address Offset: 35h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC4 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC4 OBF.
5-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to '0'.
2-1	-	0b	**Reserved**

Bit	R/W	Default	Description
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7.5.23 PMC5 Status Register (PM5STS)

This register is the same as the Status register in the host side but resides in the EC side.

Address Offset: 40h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 4: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last written (by host) address bit A2. If the bit is 0, it represents what is written to the data port is data. If this bit is 1, it represents what is written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes the data port or command port whereas cleared when the EC reads the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data port whereas cleared when the host reads the data output buffer.

6.7.5.24 PMC5 Data Out Port (PM5DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 41h

Bit	R/W	Default	Description
7-0	W	00h	**PM 5 Data Out (PM5DO[7:0])** This is the data output buffer.

6.7.5.25 PMC5 Data In Port (PM5DI)

This register is the PMDIR buffer. The written data or command by Host is stored in this buffer.

Address Offset: 42h

Bit	R/W	Default	Description
7-0	R	00h	**PMC5 Data In (PM5DI[7:0])** This is the data input buffer.

6.7.5.26 PMC5 Control (PM5CTL)

Address Offset: 43h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host's reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host's writing the data port or command port).

6.7.5.27 PMC5 Interrupt Control (PM5IC)

Address Offset: 44h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.7.5.28 PMC5 Interrupt Enable (PM5IE)

Address Offset: 45h

Bit	R/W	Default	Description
7	W	-	**Clear Input Buffer Full (CIBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC5 IBF.
6	W	-	**Clear Output Buffer Full (COBF)** When IBFOBFCME is enabled, write 1 to this bit to clear PMC5 OBF.
5-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to '0'.
2-1	-	0b	**Reserved**
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7.5.29 16-byte PMC2EX Mailbox 0-15 (MBXEC0-15)

Address Offset: F0h-FFh

Bit	R/W	Default	Description
7-0	R/W	-	**Mailbox Byte Content** This byte is the 16-byte PMC2EX mailbox in the EC side.

6.8 RTC-like Timer (RTCT)

6.8.1 Overview

The RTCT module provides timekeeping and calendar management capabilities until VSTBY is off. The alarm function is available ranging from once a second to once a month.

6.8.2 Features

- Timekeeping and calendar management until VSTBY off.
- Supports two-bank SRAM.
- Time of day alarm ranging from once a second to once a month.
- Four interrupt features available: periodic interrupt, alarm 1 interrupt, alarm 2 interrupt, and update ended interrupt.
- Supports BCD or Binary format to represent the time.
- Supports Daylight Saving Compensation function.
- Supports automatic leap year compensation function.
- Latches LPC I/O port 80h written data into SRAM of RTCT bank 1 (P80L function)

6.8.3 Functional Description

6.8.3.1 Timekeeping

The RTCT includes SRAM for each bank (128B for bank 0; 64B for bank 1; totally 192B SRAM), and provides the function of timekeeping and calendar until VSTBY is off. It uses a 32.768 kHz clock signal for timekeeping. The 32.768 kHz clock can be supplied by the internal RTCT oscillator circuit.

The RTCT update cycle occurs once a second if the SET MODE bit in the RTCT Control Register B is programmed to 0 and the Divider Chain Control field in the RTCT Control Register A is programmed to 010. Time is kept in BCD or binary format, as determined by Data Mode field in the RTCT Control Register B, and in either 12 or 24-hour format, as determined by Hour Mode field in the RTCT Control Register B. The Daylight Saving Time function is enabled by settling the Daylight Savings (DS) bit in the RTCT Control Register B.

6.8.3.2 Update Cycles

Because the time and calendar registers are updated serially, unpredictable results may occur if they are accessed during the update. Therefore, we need to ensure that reading data from or writing data to the time registers does not coincide with a system update of these locations. There are two methods to avoid this contention. One is to use the update-ended interrupt to avoid the update cycle period. When the update-ended interrupt is enabled, the interrupt will be generated immediately following the end of the update cycle. When the interrupt is received, it implies that an update has just been completed, and 999 ms remain until the next update. The other is to use the “Update In Progress” (UIP) bit in the RTCT Control Register A to determine whether the update cycle is in progress or not. If the UIP bit is 0, it is committed that the update cycle will not start for at least 244 μs.

6.8.3.3 Interrupts

The RTCT has three interrupt lines, one (IRQ) is connected to SERIRQ and handles three interrupt conditions, Periodic Interrupt, Alarm 1 Interrupt, and Update End Interrupt. The others are alarm1 interrupt and alarm2 interrupt which are connected to SWUC and INTC (INT29) respectively. The interrupts are generated if the respective enable bits in RTCT Control Register B are set prior to an interrupt event’s occurrence. The Periodic Interrupt Rate Select (PIRSEL) field in RTCT Control Register A controls the rate of the periodic interrupt. The Alarm 1 Interrupt and Alarm 2 Interrupt will be generated when the current time reaches a stored alarm time. Any alarm registers may be set to “Unconditional Match” by setting bits 7 and 6 in the alarm register. The Update Ended Interrupt is generated in the end of the update cycle.

6.8.4 Host Interface Registers

The RTCT resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The RTCT logical device number is 10h (LDN=10h). For compatibility issue, the two I/O Port Base Addresses of channel are suggested to configure at 70h and 72h and it makes two Index/Data pairs mapped into 70h-73h.

These registers are listed below.

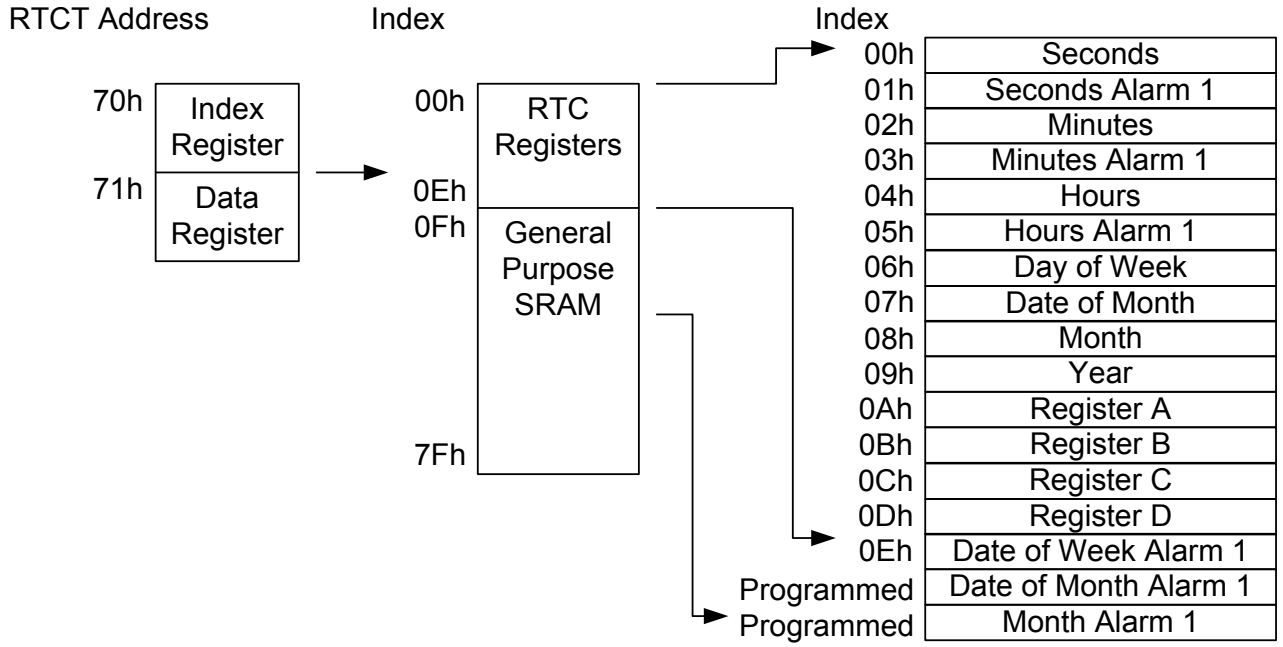
Table 6-37. Host View Register Map, RTCT

7	0	Offset
RTCT Index Register of Bank 0 (RIRB0)		Legacy 70h
RTCT Data Register of Bank 0 (RDRB0)		Legacy 71h
RTCT Index Register of Bank 1 (RIRB1)		Legacy 272h
RTCT Data Register of Bank 1 (RDRB1)		Legacy 273h

Legacy 70h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 71h represents (I/O Port Base Address 0) + (Offset 1h)
Legacy 272h represents (I/O Port Base Address 1) + (Offset 0h)
Legacy 273h represents (I/O Port Base Address 1) + (Offset 1h)
See also Table 6-7 on page 72.

The RTCT has two banks of SRAM, which are Bank 0 SRAM and Bank 1 SRAM.
All RTCT time, alarm data, and control registers are accessed by the RTCT Index and Data Registers. The Index Register points to the register location being accessed, and the Data Register contains the data to be transferred to or from the location. The Bank 0 SRAM is accessed via the first pair of the Index and Data Registers (Legacy Index 70h, 71h). The Bank 1 SRAM is accessed via the second pair of the Index and Data Registers (Legacy Index 272h, 273h). The first 14 bytes and two programmable bytes of the Bank 0 SRAM are RTCT time, alarm 1 data and control registers. The first 5 bytes of the Bank 1 SRAM are RTCT alarm 2 data registers. Access to the RTCT SRAM may be locked.

Figure 6-32. Register Map of RTCT



Bank 0 Register

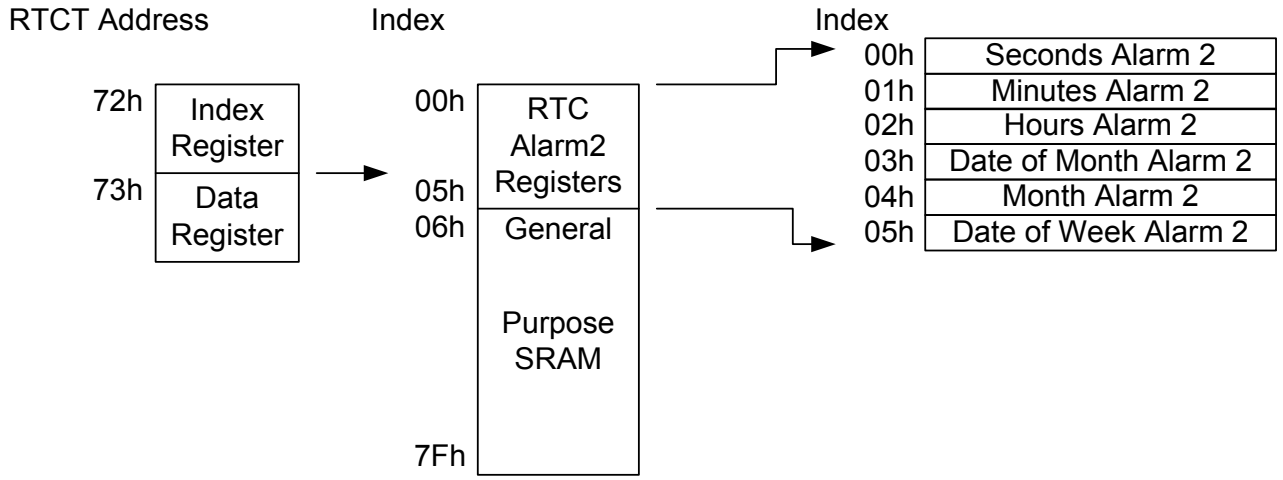


Table 6-38. Host View Register Map via Index-Data I/O Pair, RTCT Bank 0

	Index
Seconds Register (SECREG)	00h
Seconds Alarm 1 Register (SECA1REG)	01h
Minutes Register (MINREG)	02h
Minutes Alarm 1 Register (MINA1REG)	03h
Hours Register (HRREG)	04h
Hours Alarm 1 Register (HRA1REG)	05h
Day Of Week Register (DOWREG)	06h
Date Of Month Register (DOMREG)	07h
Month Register (MONREG)	08h
Year Register (YRREG)	09h
RTCT Control Register A (CTLREGA)	0Ah
RTCT Control Register B (CTLREGB)	0Bh
RTCT Control Register C (CTLREGC)	0Ch
RTCT Control Register D (CTLREGD)	0Dh
Date of Week Alarm 1 Register (DOWA1REG)	0Eh
Date of Month Alarm 1 Register (DOMA1REG)	Programmed
Month Alarm 1 Register (MONA1REG)	Programmed

Table 6-39. Host View Register Map via Index-Data I/O Pair, RTCT Bank 1

	Index
Seconds Alarm 2 Register (SECA2REG)	00h
Minutes Alarm 2 Register (MINA2REG)	01h
Hours Alarm 2 Register (HRA2REG)	02h
Date of Month Alarm 2 Register (DOMA2REG)	03h
Month Alarm 2 Register (MONA2REG)	04h
Date of Week Alarm 2 Register (DOWA2REG)	05h

6.8.4.1 RTCT Bank 0 Register

6.8.4.1.1 Seconds Register (SECREG)

Index: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Seconds Data (SECDAT)** 00 to 59 in BCD format. 00 to 3B in binary format.

6.8.4.1.2 Seconds Alarm 1 Register (SECA1REG)

Index: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Seconds Alarm 1 Data (SECA1DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.1.3 Minutes Register (MINREG)

Index: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Minutes Data (MINDAT)** 00 to 59 in BCD format. 00 to 3B in binary format.

6.8.4.1.4 Minutes Alarm 1 Register (MINA1REG)

Index: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Minutes Alarm 1 Data (MINA1DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.1.5 Hours Register (HRREG)

Index: 04h

Bit	R/W	Default	Description
7-0	R/W	00h	**Hours Data (HRDAT)** In 12-hour mode: 01 to 12 (AM) and 81 to 92 (PM) in BCD format. 01 to 0C (AM) and 81 to 8C (PM) in binary format. In 24-hour mode: 00 to 23 in BCD format. 00 to 17 in binary format.

6.8.4.1.6 Hours Alarm 1 Register (HRA1REG)

Index: 05h

Bit	R/W	Default	Description
7-0	R/W	00h	**Hours Alarm 1 Data (HRA1DAT)** **1**. In 12-hour mode: 01 to 12 (AM) and 81 to 92 (PM) in BCD format. 01 to 0C (AM) and 81 to 8C (PM) in binary format. **2**. In 24-hour mode: 00 to 23 in BCD format. 00 to 17 in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.1.7 Day Of Week Register (DOWREG)

Index: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**Day Of Week Data (DOWDAT)** 01 to 07 in BCD format. 01 to 07 in binary format. 01 is Sunday.

6.8.4.1.8 Date Of Month Register (DOMREG)

Index: 07h

Bit	R/W	Default	Description
7-0	R/W	00h	**Date Of Month Data (DOMDAT)** 01 to 31 in BCD format. 01 to 1F in binary format.

6.8.4.1.9 Month Register (MONREG)

Index: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Month Data (MONDAT)** 01 to 12 in BCD format. 01 to 0C in binary format.

6.8.4.1.10 Year Register (YRREG)

Index: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**Year Data (YRDAT)** 00 to 99 in BCD format. 00 to 63 in binary format.

6.8.4.1.11 RTCT Control Register A (CTLREGA)

Index: 0Ah

Bit	R/W	Default	Description
7	R	-	**Update in Progress (UIP)** It is 0 when bit 7 of CTLREGB register is 1. 0: Timing registers will not be updated within 244 μs. 1: Timing registers will be updated within 244 μs.
6-4	R/W	010b	**Divider Chain Control (DICCTL)** Control the divider chain for timing generation. The following is the table of the divider chain control and test selection: **CTLREGA[6:4] Configuration** 000 Reserved 010 Normal Operation 11x Divider Chain Reset others Test Mode
3-0	R/W	0000b	**Periodic Interrupt Rate Select (PIRSEL)** Control the rate of the periodic interrupt. The following is the table of the periodic interrupt rate encoding: **Rate Select Periodic Interrupt Rate (ms) Divider Chain Output** 0000 No interrupts --- 0001 3.906250 7 0010 7.812500 8 0011 0.122070 2 0100 0.244141 3 0101 0.488281 4 0110 0.976562 5 0111 1.953125 6 1000 3.906250 7 1001 7.812500 8 1010 15.625000 9 1011 31.250000 10 1100 62.500000 11 1101 125.000000 12 1110 250.000000 13 1111 500.000000 14

6.8.4.1.12 RTCT Control Register B (CTLREGB)

Index: 0Bh

Bit	R/W	Default	Description
7	R/W	0b	**Set Mode (SM)** 0: Timing updates occur normally. 1: Update cycles will not occur until this bit is 0.
6	R/W	0b	**Periodic Interrupt Enable (PIE)** Enable the periodic interrupt. The rate is determined by CTLREGA[3:0]. It is cleared to 0 on RTCT reset or at the time when RTCT is disabled. 0: Disable 1: Enable
5	R/W	0b	**Alarm 1 Interrupt Enable (A1IE)** This interrupt is generated when the alarm1 condition matches the current data time. It is cleared to 0 when bit7 of CTLREGD register is 0. 0: Disable 1: Enable
4	R/W	0b	**Update Ended Interrupt Enable (UEIE)** This interrupt is generated when an update occurs. It is cleared to 0 on RTCT reset or at the time when the RTCT is disabled. 0: Disable 1: Enable
3	R/W	0b	**Alarm 2 Interrupt Enable (A2IE)** This interrupt is generated when the alarm 2 condition matches the current data time. It is cleared to 0 when bit7 of CTLREGD register is 0. 0: Disable 1: Enable
2	R/W	0b	**Data Mode (DAM)** 0: Enable BCD format 1: Enable binary format
1	R/W	1b	**Hour Mode (HRM)** 0: Enable 12-hour format 1: Enable 24-hour format
0	R/W	0b	**Daylight Savings (DS)** In spring, time advances from 1:59:59 AM to 3:00:00 AM on the first Sunday in April. In fall, time returns from 1:59:59 AM to 1:00:00 AM on the last Sunday in October. 0: Disable 1: Enable

6.8.4.1.13 RTCT Control Register C (CTLREGC)

Index: 0Ch

Bit	R/W	Default	Description
7	R	0b	**IRQ Flag (IRQF)** This flag will be set and an interrupt will be generated when one of the following conditions occurs: PIF=1 and PIE=1 A1IF=1 and A1IE=1 UEIF=1 and UEIE=1 This bit is cleared to 0 on RTCT reset or at the time when the RTCT is disabled. This bit is also cleared to 0 when this register is read.
6	R	0b	**Periodic Interrupt Flag (PIF)** This bit is cleared to 0 on RTCT reset or at the time when the RTCT is disabled. This bit is also cleared to 0 when this register is read. When the CTLREGA [3:0] bits are not 0000b, the interrupt will be generated and this bit is set to 1 once the period is specified.
5	R	0b	**Alarm 1 Interrupt Flag (A1IF)** This bit is cleared to 0 when bit 7 of CTLREGD register is 0. This bit is also cleared to 0 when this register is read. 0: No alarm condition occurs. 1: Alarm 1 condition occurs.
4	R	0b	**Update Ended Interrupt Flag (UEIF)** This bit is cleared to 0 on RTCT reset or at the time when the RTCT is disabled. This bit is also cleared to 0 when this register is read. 0: No update occurs. 1: The updated cycle is ended
3	R	0b	**Alarm 2 Interrupt Flag (A2IF)** This bit is cleared to 0 when bit 7 of CTLREGD register is 0. This bit is also cleared to 0 when this register is read. 0: No alarm condition occurs. 1: Alarm 2 condition occurs.
2-0	-	000b	**Reserved**

6.8.4.1.14 RTCT Control Register D (CTLREGD)

Index: 0Dh

Bit	R/W	Default	Description
7	R	0b	**Valid RAM and Time (VRAT)** This bit responds whether the voltage that feeds the RTCT is too low or not. 0: RTCT contents are not valid. 1: RTCT contents are valid.
6-0	-	00h	**Reserved**

6.8.4.1.15 Date of Week Alarm 1 Register (DOWA1REG)

Index: 0Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Date of Week Alarm 1 Data (DOWA1DAT)** 01 to 07 in BCD format. 01 to 07 in binary format. 01 is Sunday.

6.8.4.1.16 Date of Month Alarm 1 Register (DOMA1REG)

The index of this register is programmable. Please see the “RTCT Logical Device” for details.

Index: Programmed (Refer to Section 6.3.11.15 , Page 98)

Bit	R/W	Default	Description
7-0	R/W	C0h	**Date of Month Alarm 1 Data (DOMA1DAT)** 01 to 31 in BCD format. 01 to 1F in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.1.17 Month Alarm 1 Register (MONA1REG)

The index of this register is programmable. Please see the “RTCT Logical Device” for details.

Index: Programmed (Refer to Section 6.3.11.16 , Page 99)

Bit	R/W	Default	Description
7-0	R/W	C0h	**Month Alarm 1 Data (MONA1DAT)** 01 to 12 in BCD format. 01 to 0C in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.2 RTCT Bank 1 Register

6.8.4.2.1 Seconds Alarm 2 Register (SECA2REG)

Index: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Seconds Alarm 2 Data (SECA2DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.2.2 Minutes Alarm 2 Register (MINA2REG)

Index: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Minutes Alarm 2 Data (MINA2DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.2.3 Hours Alarm 2 Register (HRA2REG)

Index: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Hours Alarm 2 Data (HRA2DAT)** 1. In 12-hour mode: 01 to 12 (AM) and 81 to 92 (PM) in BCD format. 01 to 0C (AM) and 81 to 8C (PM) in binary format. 2. In 24-hour mode: 00 to 23 in BCD format. 00 to 17 in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.2.4 Date of Month Alarm 2 Register (DOMA2REG)

Index: 03h

Bit	R/W	Default	Description
7-0	R/W	C0h	**Date of Month Alarm 2 Data (DOMA2DAT)** 01 to 31 in BCD format. 01 to 1F in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.2.5 Month Alarm 2 Register (MONA2REG)

Index: 04h

Bit	R/W	Default	Description
7-0	R/W	C0h	**Month Alarm 2 Data (MONA2DAT)** 01 to 12 in BCD format. 01 to 0C in binary format. The unconditional match is selected when bit 7 and 6 are “11”.

6.8.4.2.6 Date of Week Alarm 2 Register (DOWA2REG)

Index: 05h

Bit	R/W	Default	Description
7-0	R/W	00h	**Date of Week Alarm 2 Data (DOWA1DAT)** 01 to 07 in BCD format. 01 to 07 in binary format. 01 is Sunday.

6.8.4.3 RTCT I/O Register

6.8.4.3.1 RTCT Index Register of Bank 0 (RIRB0)

Address offset: 70h

Bit	R/W	Default	Description
7-0	R/W	-	**RTCT Index Register of Bank 0(RIRB0)** This register is used to locate the data on bank 0, and is a read/write access register. It must be paired with RTC Data Register of Bank 0 to program or read the indexed registers.

6.8.4.3.2 RTCT Data Register of Bank 0 (RDRB0)

Address offset: 71h

Bit	R/W	Default	Description
7-0	R/W	-	**RTCT Data Register of Bank 0 (RDRB0)** This register is used to preserve the data to be programmed or read from the bank 0, and is a read/write access register. It must be paired with RTC Index Register of Bank 0 to program or read the indexed registers.

6.8.4.3.3 RTCT Index Register of Bank 1 (RIRB1)

Address offset: 272h

Bit	R/W	Default	Description
7-0	R/W	-	**RTCT Index Register of Bank 1(RIRB1)** This register is used to locate the data on bank 1, and is a read/write access register. It must be paired with RTC Data Register of Bank 1 to program or read the indexed registers.

6.8.4.3.4 RTCT Data Register of Bank 1 (RDRB1)

Address offset: 273h

Bit	R/W	Default	Description
7-0	R/W	-	**RTC Data Register of Bank 1 (RDRB1)** This register is used to preserve the data to be programmed or read from the bank 1, and is a read/write access register. It must be paired with RTC Index Register of Bank 1 to program or read the indexed registers.

6.9 Consumer IR (CIR) in Host Domain

6.9.1 Overview

CIR module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.20 Consumer IR (CIR) for the EC domain function description on page 463.

CIR can be accessed by the software in the host or EC side, however, the CIR function should be controlled by a side only. See also section 7.17.4.10 Reset Control DMM (RSTDMMC) on page 443 and section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273.

6.10 Serial Peripheral Interface (SSPI) in Host Domain

6.10.1 Overview

SSPI module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.21 Serial Peripheral Interface (SSPI) for the EC domain function description on page 480.

SSPI can be accessed by the software in the host or EC side, however, the SSPI function should be controlled by a side only. See also section 7.17.4.10 Reset Control DMM (RSTDMMC) on page 443 and section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273.

6.11 Platform Environment Control Interface (PECI) in Host Domain

6.11.1 Overview

PECI module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.8 Platform Environment Control Interface (PECI) for the EC domain function description on 347.

PECI can be accessed by the software in the host or EC side; however, the PECI function should be controlled by a side only. See also section 7.17.4.10 Reset Control DMM (RSTDMMC) on page 443.

6.12 Serial Port 1/2 (UART1/UART2) in Host Domain

6.12.1 Overview

UART1 module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.22 Serial Port (UART) for the EC domain function description on page 488.

UART1 can be accessed by the software in the host or EC side, however, the UART1 function should be controlled by a side only. See also section 7.17.4.10 Reset Control DMM (RSTDMMC) on page 443 and section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273.

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7. EC Domain Functions

7.1 32-bit Embedded Controller (EC)

7.1.1 Overview

The embedded 32-bit controller is a low-power and small-sized micro processor named N801.

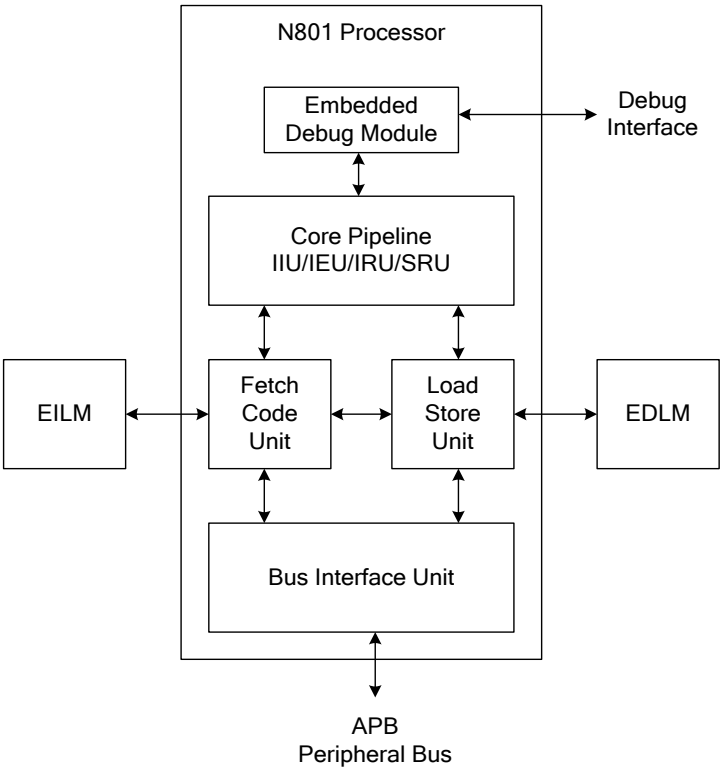
7.1.2 Features

- AndeStar V3m architecture
- 3-stage pipeline
- 16 general-purpose 32-bit registers
- Built-in hardware fast multiplier
- Built-in hardware divider
- Supports STANDBY (a.k.a. power-down) mode
- Supports 16 external interrupts and one power fail interrupt
- Supports 16MB code/data address space

7.1.3 General Description

The N801 is a low-power and small-sized AndeStar V3m architecture micro-processor based on RISC architecture & Pipeline design. With instruction-local-memory(ILM) and data-local-memory(DLM) interface, the processor can access to the code/data directly in one cycle without any bus latency and achieve the optimal performance againsts to the core clock frequency.

Figure 7-1. N801 Processor Block Diagram



7.1.4 Functional Description

Memory
Local memory is for storing instructions and/or data that might be accessed frequently in a system such as interrupt service routine, system call, sensor fusion data, etc. N801 supports load memories through its external local memory interfaces. Both instruction local memory and data
local memory are supported.

I/O ports
N801 has three types of bus interfaces, ILM, DLM and APB. For instruaction access, the code is read from the ILM (Instruction Local Memory) controlled by the IMMU (Instruction Memory Management Unit). For data access, the variables or DMA data are read/written from/to the DLM (Data Local Memory). All the EC side peripheral I/Os are accessed through the APB bus. All these 3 types of interfaces have 24-bit addressing ability.

Interrupts
In AndeStar™ architecture, an interruption is a control flow change of normal instruction execution generated by an Interrupt or an Exception. When an interruption happens, the processor stops processing current flow of instructions, saves enough states for later resuming of the interrupted current flow, disables interrupts, enters Superuser Mode, and starts executing a software interruption handler.

In IT5121, there are 16 interrupt inputs to N801. The entry points for all the exceptions and interrupts are listed as below.

Table 7-1. N801 Interrupt Entry Point

Offset	0	1	2	3	4	5	6	7	8
Entry Point	Reset/ NMI	TLB fill	PTR not present	TLB misc	TLB VLPT miss	Machine error	Debug related	General exception	Syscall

Offset	9	10	11	12	13	14	15	16
Entry Point	HW0	HW1	HW2	HW3	HW4	HW5	HW6	HW7

Offset	17	18	19	20	21	22	23	24
Entry Point	HW8	HW9	HW10	HW11	HW12	HW13	HW14	HW15

Power Management
AndeStar™ ISA provides a STANDBY instruction for Andes cores to enter a reduced power mode. Once entering the reduced power mode, the CPU clock is fully gated-off. Only external interrupt events can wake the CPU up and restore the process routing.

7.2 Interrupt Controller (INTC)

7.2.1 Overview

INTC mainly collects several interrupts from modules. The performance of the interrupt-driven design is better than that of the polling-driven design.

External interrupts can wakeup CPU from Doze/Deep Doze/Sleep mode.

7.2.2 Features

- Configurable level-triggered and edge-triggered mode
- Configurable interrupt polarity of triggered mode
- Clears registers for edge-triggered interrupts
- Each interrupt source able to enabled/masked individually

7.2.3 Functional Description

7.2.3.1 Programmable Interrupts

INTC also collects all maskable interrupt sources and make a request on INT1 # of CPU if triggered. Each channel can be individually enabled or masked by IERx. If an interrupt channel is masked and one interrupt request is triggered, the request is masked (inhibited, not canceled), and will be asserted on INT1# if it is enabled.

The ISRx indicates the status of interrupt regardless of IERx. In the level-triggered mode, ISRx is affected by corresponding interrupt sources, and firmware should clear the interrupt status on interrupt sources after its request is handled. In the edge-triggered mode, ISRx is set by selected edge transition (determined by IELMRx) of corresponding interrupts sources, and firmware should write 1 to clear ISRx after this request is handled.

Firmware may use the IVECT to determine which channel is to be serviced first or have its priority rule by reading ISRx and IERx. IVECT reflects all the internal and external interrupt events. For all IVECT the larger numeric interrupt source has the higher priority and INT1 is in the lowest priority.

The CPU always wakes up from Doze/Deep Doze/Sleep mode when it detects an enabled external interrupt. Firmware should disable unwanted interrupt sources to prevent them from waking up unexpectedly.

Normally interrupts from WUC are high level-triggered. Note that interrupts from WUC are not always level-triggered interrupts since they may be just throughout WUC if the corresponding channels at WUC are disabled (bypassed). If an edge-triggered interrupt passes through WUC and INTC with WUC corresponding channel is disabled and INTC corresponding channel is level-triggered mode, it may cause CPU interrupt routine to be called but finds no interrupt source to service, or it may cause CPU to wake up from Doze/Deep Doze/Sleep mode and enters interrupt routine but finds no interrupt source to service.

7.2.4 EC Interface Registers

The EC interface registers are listed below. The base address for INTC is 1100h.

Table 7-2. EC View Register Map, INTC

7	0	Offset
Interrupt Status Register 0 (ISR0)		00h
Interrupt Status Register 1 (ISR1)		01h
Interrupt Status Register 2 (ISR2)		02h
Interrupt Status Register 3 (ISR3)		03h
Interrupt Status Register 4 (ISR4)		14h
Interrupt Status Register 5 (ISR5)		18h

7	0	Offset
Interrupt Status Register 6 (ISR6)		1Ch
Interrupt Status Register 7 (ISR7)		20h
Interrupt Status Register 8 (ISR8)		24h
Interrupt Status Register 9 (ISR9)		28h
Interrupt Status Register 10 (ISR10)		2Ch
Interrupt Status Register 11 (ISR11)		30h
Interrupt Status Register 12 (ISR12)		34h
Interrupt Status Register 13 (ISR13)		38h
Interrupt Status Register 14 (ISR14)		3Ch
Interrupt Status Register 15 (ISR15)		40h
Interrupt Status Register 16 (ISR16)		44h
Interrupt Status Register 17 (ISR17)		48h
Interrupt Status Register 18 (ISR18)		4Ch
Interrupt Status Register 19 (ISR19)		50h
Interrupt Status Register 20 (ISR20)		54h
Interrupt Status Register 21 (ISR21)		58h
Interrupt Enable Register 0 (IER0)		04h
Interrupt Enable Register 1 (IER1)		05h
Interrupt Enable Register 2 (IER2)		06h
Interrupt Enable Register 3 (IER3)		07h
Interrupt Enable Register 4 (IER4)		15h
Interrupt Enable Register 5 (IER5)		19h
Interrupt Enable Register 6 (IER6)		1Dh
Interrupt Enable Register 7 (IER7)		21h
Interrupt Enable Register 8 (IER8)		25h
Interrupt Enable Register 9 (IER9)		29h
Interrupt Enable Register 10 (IER10)		2Dh
Interrupt Enable Register 11 (IER11)		31h
Interrupt Enable Register 12 (IER12)		35h
Interrupt Enable Register 13 (IER13)		39h
Interrupt Enable Register 14 (IER14)		3Dh
Interrupt Enable Register 15 (IER15)		41h
Interrupt Enable Register 16 (IER16)		45h
Interrupt Enable Register 17 (IER17)		49h
Interrupt Enable Register 18 (IER18)		4Dh
Interrupt Enable Register 19 (IER19)		51h
Interrupt Enable Register 20 (IER20)		55h
Interrupt Enable Register 21 (IER21)		59h
Interrupt Edge/Level-Triggered Mode Register 0 (IELMR0)		08h
Interrupt Edge/Level-Triggered Mode Register 1 (IELMR1)		09h
Interrupt Edge/Level-Triggered Mode Register 2 (IELMR2)		0Ah
Interrupt Edge/Level-Triggered Mode Register 3 (IELMR3)		0Bh
Interrupt Edge/Level-Triggered Mode Register 4 (IELMR4)		16h
Interrupt Edge/Level-Triggered Mode Register 5 (IELMR5)		1Ah
Interrupt Edge/Level-Triggered Mode Register 6 (IELMR6)		1Eh
Interrupt Edge/Level-Triggered Mode Register 7 (IELMR7)		22h
Interrupt Edge/Level-Triggered Mode Register 8 (IELMR8)		26h
Interrupt Edge/Level-Triggered Mode Register 9 (IELMR9)		2Ah
Interrupt Edge/Level-Triggered Mode Register 10 (IELMR10)		2Eh
Interrupt Edge/Level-Triggered Mode Register 11 (IELMR11)		32h
Interrupt Edge/Level-Triggered Mode Register 12 (IELMR12)		36h
Interrupt Edge/Level-Triggered Mode Register 13 (IELMR13)		3Ah
Interrupt Edge/Level-Triggered Mode Register 14 (IELMR14)		3Eh

7 0	Offset
Interrupt Edge/Level-Triggered Mode Register 15 (IELMR15)	42h
Interrupt Edge/Level-Triggered Mode Register 16 (IELMR16)	46h
Interrupt Edge/Level-Triggered Mode Register 17 (IELMR17)	4Ah
Interrupt Edge/Level-Triggered Mode Register 18 (IELMR18)	4Eh
Interrupt Edge/Level-Triggered Mode Register 19 (IELMR19)	52h
Interrupt Edge/Level-Triggered Mode Register 20 (IELMR20)	56h
Interrupt Edge/Level-Triggered Mode Register 21 (IELMR21)	5Ah
Interrupt Polarity Register 0 (IPOLR0)	0Ch
Interrupt Polarity Register 1 (IPOLR1)	0Dh
Interrupt Polarity Register 2 (IPOLR2)	0Eh
Interrupt Polarity Register 3 (IPOLR3)	0Fh
Interrupt Polarity Register 4 (IPOLR4)	17h
Interrupt Polarity Register 5 (IPOLR5)	1Bh
Interrupt Polarity Register 6 (IPOLR6)	1Fh
Interrupt Polarity Register 7 (IPOLR7)	23h
Interrupt Polarity Register 8 (IPOLR8)	27h
Interrupt Polarity Register 9 (IPOLR9)	2Bh
Interrupt Polarity Register 10 (IPOLR10)	2Fh
Interrupt Polarity Register 11 (IPOLR11)	33h
Interrupt Polarity Register 12 (IPOLR12)	37h
Interrupt Polarity Register 13 (IPOLR13)	3Bh
Interrupt Polarity Register 14 (IPOLR14)	3Fh
Interrupt Polarity Register 15 (IPOLR15)	43h
Interrupt Polarity Register 16 (IPOLR16)	47h
Interrupt Polarity Register 17 (IPOLR17)	4Bh
Interrupt Polarity Register 18 (IPOLR18)	4Fh
Interrupt Polarity Register 19 (IPOLR19)	53h
Interrupt Polarity Register 20 (IPOLR20)	57h
Interrupt Polarity Register 21 (IPOLR21)	5Bh
Interrupt Vector Register (IVECT)	10h

7.2.4.1 Interrupt Status Register 0-21 (ISR0 – ISR21)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

ISR0 defined in Group 0
ISR1 defined in Group 1
ISR2 defined in Group 2
ISR3 defined in Group 3
ISR4 defined in Group 4
ISR5 defined in Group 5 (Reserved)
ISR6 defined in Group 6
ISR7 defined in Group 7
ISR8 defined in Group 8
ISR9 defined in Group 9
ISR10 defined in Group 10
ISR11 defined in Group 11
ISR12 defined in Group 12
ISR13 defined in Group 13
ISR14 defined in Group 14
ISR15 defined in Group 15
ISR16 defined in Group 16
ISR17 defined in Group 17 (Reserved)
ISR18 defined in Group 18
ISR19 defined in Group 19
ISR20 defined in Group 20
ISR21 defined in Group 21

Note: Where Group 0-21 (Refer to Table 7-3 on page 211).

Address Offset: 00h

Bit	R/W	Default	Description
7-1	R/WC Or R	-	**Interrupt Status Group 0 (ISGR0 7:1)** It indicates the interrupt input status of INTx. INTST7 to INTST1 correspond to INT7 to INT1 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, while R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending. Read 1: Interrupt input to INTC is pending. For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.
0	R	0b	**Reserved**

Address Offset:
01h,02h,03h,14h,18h,1Ch,20h,24h,28h,2Ch,30h,34h,38h,3Ch,40h,44h,48h,4Ch,50h,54h,58h

Bit	R/W	Default	Description
7-0	R/WC or R	-	**Interrupt Status Group x (ISGRx 7:0)** It indicates the interrupt input status of (INTn).(where n means 0 - 7 whether its corresponding Group x) The same as ISGR0 Note: Where x means (1-21)

7.2.4.2 Interrupt Enable Register 0-21 (IER0 – IER21)

IER0 defined in Group 0
IER1 defined in Group 1
IER2 defined in Group 2
IER3 defined in Group 3
IER4 defined in Group 4
IER5 defined in Group 5 (Reserved)
IER6 defined in Group 6
IER7 defined in Group 7
IER8 defined in Group 8
IER9 defined in Group 9
IER10 defined in Group 10
IER11 defined in Group 11
IER12 defined in Group 12
IER13 defined in Group 13
IER14 defined in Group 14
IER15 defined in Group 15
IER16 defined in Group 16
IER17 defined in Group 17 (Reserved)
IER18 defined in Group 18
IER19 defined in Group 19
IER20 defined in Group 20
IER21 defined in Group 21

Note: Where Group 0-21 (Refer to Table 7-3 on page 211)

Address Offset: 04h

Bit	R/W	Default	Description
7-1	R/W	0h	**Interrupt Enable Group 0 (IEGR0 7:1)** Each bit determines whether its corresponding interrupt channel (INT7-0) is masked or enabled. Note that it has no effect on INT0 0: Mask 1: Enable
0	-	0b	**Reserved**

Address Offset:
05h,06h,07h,15h,19h,1Dh,21h,25h,29h,2Dh,31h,35h,39h,3Dh,41h,45h,49h,4Dh,51h,55h,59h

Bit	R/W	Default	Description
7-0	R/W	00h	**Interrupt Enable Group x (IEGRx 7:0)** Each bit determines whether its corresponding interrupt channel (INTn) is masked or enabled. (where n means 0 - 7 whether its corresponding Group x) 0: Mask 1: Enabled Note: Where x means (1-21)

7.2.4.3 Interrupt Edge/Level-Triggered Mode Register 0-21 (IELMR0 – IELMR21)

It determines whether its corresponding interrupt channel is level-triggered or edge-triggered.

IELMR0 defined in Group 0
IELMR1 defined in Group 1
IELMR2 defined in Group 2
IELMR3 defined in Group 3
IELMR4 defined in Group 4
IELMR5 defined in Group 5 (Reserved)
IELMR6 defined in Group 6
IELMR7 defined in Group 7
IELMR8 defined in Group 8
IELMR9 defined in Group 9
IELMR10 defined in Group 10
IELMR11 defined in Group 11
IELMR12 defined in Group 12
IELMR13 defined in Group 13
IELMR14 defined in Group 14
IELMR15 defined in Group 15
IELMR16 defined in Group 16
IELMR17 defined in Group 17 (Reserved)
IELMR18 defined in Group 18
IELMR19 defined in Group 19
IELMR20 defined in Group 20
IELMR21 defined in Group 21

Note: Where Group 0-21 (Refer to Table 7-3 on page 211)

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00000000b	**Interrupt Edge/Level-Triggered Mode Group 0 (IELMGR0 7:0)** Each bit determines the triggered mode of the corresponding interrupt channel (INT7-0). 0: Level-triggered 1: Edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

Address Offset:
09h,0Ah,0Bh,16h,1Ah,1Eh,22h,26h,2Ah,2Eh,32h,36h,3Ah,3Eh,42h,46h,4Ah,4Eh,52h,56h,5Ah

Bit	R/W	Default	Description
7-0	R/W (only for IELMR 1-3) R (only for IELMR 4-21)	Refer to Table 7-3 on page 211	**Interrupt Edge/Level-Triggered Mode Group x (IELMGRx 7:0)** Each bit determines the triggered mode of the corresponding interrupt channel (INTn). (where n means 0 - 7 whether its corresponding Group x) The same as IELMGR0 Note: Where x means (1-21)

7.2.4.4 Interrupt Polarity Register 0-21 (IPOLR0 – IPOLR21)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

IPOLR0 defined in Group 0
IPOLR1 defined in Group 1
IPOLR2 defined in Group 2
IPOLR3 defined in Group 3
IPOLR4 defined in Group 4
IPOLR5 defined in Group 5 (Reserved)
IPOLR6 defined in Group 6
IPOLR7 defined in Group 7
IPOLR8 defined in Group 8
IPOLR9 defined in Group 9
IPOLR10 defined in Group 10
IPOLR11 defined in Group 11
IPOLR12 defined in Group 12
IPOLR13 defined in Group 13
IPOLR14 defined in Group 14
IPOLR15 defined in Group 15
IPOLR16 defined in Group 16
IPOLR17 defined in Group 17 (Reserved)
IPOLR18 defined in Group 18
IPOLR19 defined in Group 19
IPOLR20 defined in Group 20
IPOLR21 defined in Group 21

Note: Where Group 0-21 (Refer to Table 7-3 on page 211)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity Group 0 (IPOLGR0 7:0)** Each bit determines the active high/low of the corresponding interrupt channel (INT7-0). 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

Address Offset:
0Dh,0Eh,0Fh,17h,1Bh,1Fh,23h,27h,2Bh,2Fh,33h,37h,3Bh,3Fh,43h,47h,4Bh,4Fh,53h,57h,5Bh

Bit	R/W	Default	Description
7-0	R/W (only for IPOLR 1-3) R (only for IPOLR 4-21)	0h	**Interrupt Polarity Group x (IPOLGRx 7:0)** Each bit determines the active high/low of the corresponding interrupt channel (INTn). (where n means 0 - 7 whether its corresponding Group x) The same as IPOLGR0 Note: Where x means (1-21)

7.2.4.5 Interrupt Vector Register (IVCT)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R	00010000b	**Interrupt Vector (IVECT)** It contains the interrupt number, which is the highest priority, enabled and pending interrupt. The valid values range from 10h. Note that INT1 has the lowest priority. If no enabled interrupt is pending, it returns 10h.

7.2.5 INTC Interrupt Assignments

Table 7-3. INTC Interrupt Assignments

Group	Interrupt	Source	Default Type(Adjustable)	Description	Reference
0	INT0	-	-	Reserved	-
	INT1	External/WUC	High-Level Trig	WKO[20]	Figure 7-4, p225
	INT2	Internal	High-Level Trig	KBC Output Buffer Empty Interrupt	Section 6.6.3, p159
	INT3	Internal	High-Level Trig	PMC Output Buffer Empty Intr. PMC1 Output Buffer Empty Intr.	Section 6.7.3.1, p166 Section 6.7.3.1, p166
	INT4	Internal	High-Level Trig	SMBus D Interrupt	Table 7-12 , p310
	INT5	External/WUC	High-Level Trig	WKINTAD (WKINTA or WKINTD)	Figure 7-4, p225
	INT6	External/WUC	High-Level Trig	WKO[23]	Figure 7-4, p225
	INT7	Internal	High-Level Trig	PWM Interrupt	Section 7.12.4.20, p398
1	INT8	Internal	High-Level Trig	ADC Interrupt	Section 7.11.3.1, p363
	INT9	Internal	High-Level Trig	SMBus A Interrupt	Table 7-12 , p310
	INT10	Internal	High-Level Trig	SMBus B Interrupt	Table 7-12 , p310
	INT11	Internal	High-Level Trig	KB Matrix Scan Interrupt	Section 7.4.2, p227
	INT12	External/WUC	High-Level Trig	WKO[26]	Figure 7-4, p225
	INT13	External/WUC	High-Level Trig	WKINTC	Figure 7-4, p225
	INT14	External/WUC	High-Level Trig	WKO[25]	Figure 7-4, p225
	INT15	Internal	High-Level Trig	CIR Interrupt	Section 7.20.5.3, p468
2	INT16	Internal	High-Level Trig	SMBus C Interrupt	Table 7-12 , p310
	INT17	External/WUC	High-Level Trig	WKO[24]	Figure 7-4, p225
	INT18	Internal	Rising-Edge Trig	PS/2 Interrupt 2	Section 7.9.2, p356
	INT19	Internal	Rising-Edge Trig	PS/2 Interrupt 1	Section 7.9.2, p356
	INT20	Internal	Rising-Edge Trig	PS/2 Interrupt 0	Section 7.9.2, p356
	INT21	External/WUC	High-Level Trig	WKO[22]	Figure 7-4, p225
	INT22	Internal	High-Level Trig	SMFI Semaphore Interrupt	Section 6.4.4.4, p124
	INT23	-	-	Reserved	-

Group	Interrupt	Source	Default Type(Adjustable)	Description	Reference
3	INT24	Internal	High-Level Trig	KBC Input Buffer Full Interrupt	Section 6.6.3, p159
	INT25	Internal	High-Level Trig	PMC Input Buffer Full Interrupt PMC1 Input Buffer Full Interrupt	Section 6.7.3.1, p166 Section 6.7.3.1, p166
	INT26	Internal	High-Level Trig	PMC2 Output Buffer Empty Intr.	Section 6.7.3.1, p166
	INT27	Internal	High-Level Trig	PMC2 Input Buffer Full Intr.	Section 6.7.3.1, p166
	INT28	External	High-Level Trig	GINT from function 1 of GPD5	Table 5-20, p18
	INT29	Internal	Rising-Edge Trig	EGPC Interrupt	Section 7.18.3, p450
	INT30	Internal	Rising-Edge Trig	External Timer 1 Interrupt	Section 7.16.3, p432
	INT31	External/WUC	High-Level Trig	WKO[21]	Figure 7-4, p225
4	INT32	Internal	Rising-Edge Trig (Not Adjustable)	GPINT0	Section 6.3.13.10, p103
	INT33	Internal		GPINT1	Section 6.3.13.10, p103
	INT34	Internal		GPINT2	Section 6.3.13.10, p103
	INT35	Internal		GPINT3	Section 6.3.13.10, p103
	INT36	Internal		CIR GPINT	Section 7.20.5.18, p479
	INT37	Internal		SSPI Interrupt	Section 7.21.5.2, p483
	INT38	Internal		UART1 Interrupt	Section 7.22.5.3, p489
	INT39	Internal		UART2 Interrupt	Section 7.22.5.3, p489
5	-	-	-	Reserved	-
6	INT48	External/WUC	High-Level Trig (Not Adjustable)	WKO[60]	Figure 7-4, p225
	INT49	External/WUC		WKO[61]	
	INT50	External/WUC		WKO[62]	
	INT51	External/WUC		WKO[63]	
	INT52	External/WUC		WKO[64]	
	INT53	External/WUC		WKO[65]	
	INT54	External/WUC		WKO[66]	
	INT55	External/WUC		WKO[67]	

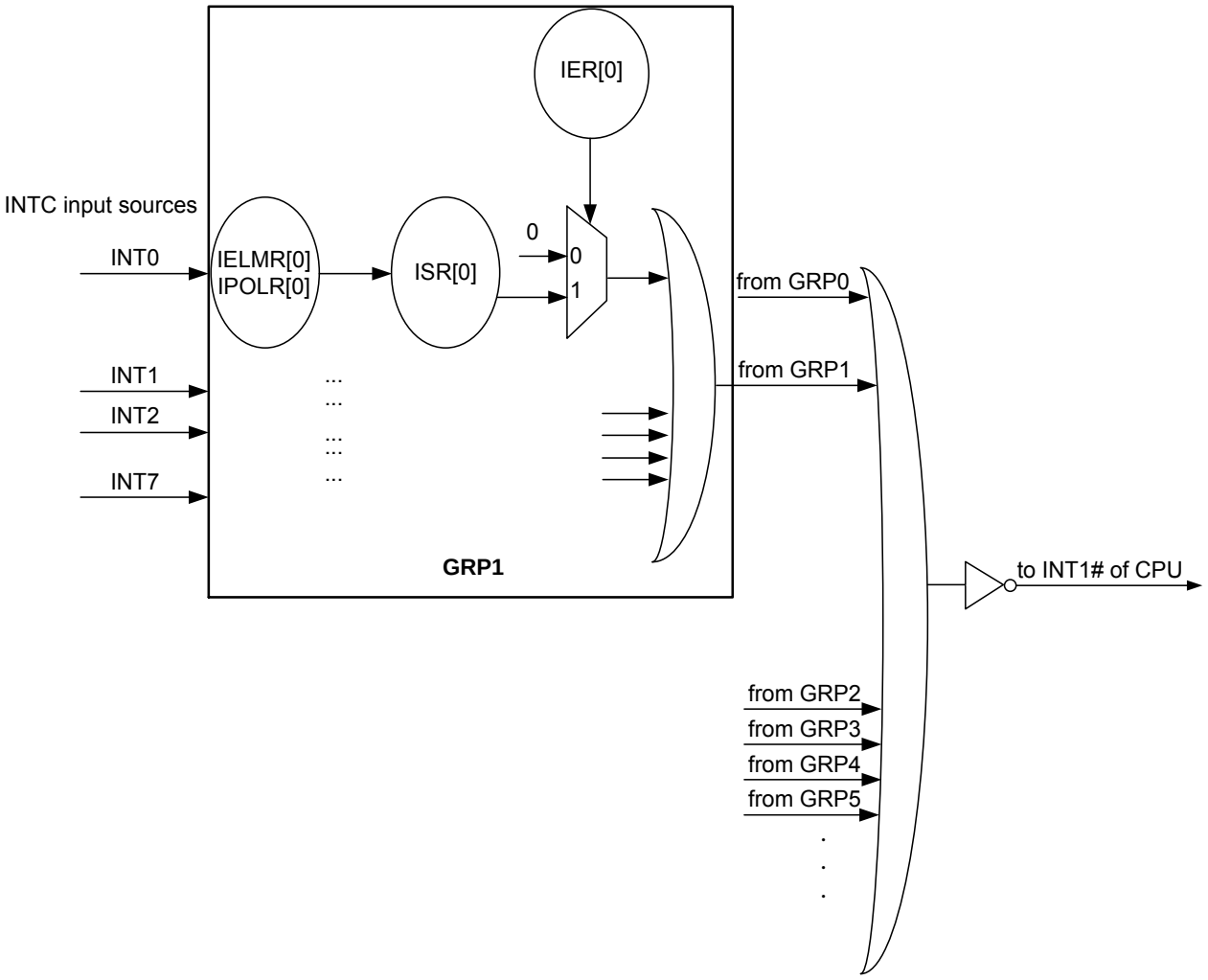
Group	Interrupt	Source	Default Type(Adjustable)	Description	Reference
7	INT56	Internal	Rising-Edge Trig (Not Adjustable)	RTCT Alarm 1	Section 6.8.3.3 p184
	INT57	Internal		RTCT Alarm 2	Section 6.8.3.3 p184
	INT58	Internal		External Timer 2 Interrupt	Section 7.16.3, p432
	INT59	-	-	Reserved	-
	INT60	Internal	Rising-Edge Trig (Not Adjustable)	TMRINTA0	Section 7.13.3.6 , p414
	INT61	Internal		TMRINTA1	Section 7.13.3.6 , p414
	INT62	Internal		TMRINTB0	Section 7.13.3.6 , p414
	INT63	Internal		TMRINTB1	Section 7.13.3.6 , p414
8	INT64	Internal	High-Level Trig (Not Adjustable)	PMC2EX Output Buffer Empty Intr.	Section 6.7.3.1, p166
	INT65	Internal		PMC2EX Input Buffer Full Intr.	Section 6.7.3.1, p166
	INT66	Internal		PMC3 Output Buffer Empty Intr.	Section 6.7.3.1, p166
	INT67	Internal		PMC3 Input Buffer Full Intr.	Section 6.7.3.1, p166
	INT68	Internal		PMC4 Output Buffer Empty Intr.	Section 6.7.3.1, p166
	INT69	Internal		PMC4 Input Buffer Full Intr.	Section 6.7.3.1, p166
	INT70	-	-	Reserved	-
	INT71	Internal	High-Level Trig (Not Adjustable)	I2BRAM Interrupt	Section 7.17.4.23, p447
9	INT72	External/WUC	High-Level Trig (Not Adjustable)	WKO[70]	Figure 7-4, p225
	INT73	External/WUC		WKO[71]	
	INT74	External/WUC		WKO[72]	
	INT75	External/WUC		WKO[73]	
	INT76	External/WUC		WKO[74]	
	INT77	External/WUC		WKO[75]	
	INT78	External/WUC		WKO[76]	
	INT79	External/WUC		WKO[77]	
10	INT80	-	-	Reserved	-
	INT81	Internal	High-Level Trig (Not Adjustable)	SMbus Clock Held intr.	Section 7.7.3.2 , p280
	INT82	Internal		CEC Interrupt	Section 7.14.1.1 , p422
	INT83	Internal		H2RAM LPC Trigger	Section 6.3.10.15 , p93
	INT84	Internal		KB Scan Data Valid Interrupt	Section 7.4.4.35 , p240
	INT85	External/WUC		WKO[88]	Figure 7-4 p225
	INT86	External/WUC		WKO[89]	Figure 7-4 p225
	INT87	External/WUC		WKO[90]	Figure 7-4 p225

Group	Interrupt	Source	Default Type(Adjustable)	Description	Reference
11	INT88	External/WUC	High-Level Trig (Not Adjustable)	WKO[80]	Figure 7-4 p225
	INT89			WKO[81]	
	INT90			WKO[82]	
	INT91			WKO[83]	
	INT92			WKO[84]	
	INT93			WKO[85]	
	INT94			WKO[86]	
	INT95			WKO[87]	
12	INT96	External/WUC	High-Level Trig (Not Adjustable)	WKO[91]	Figure 7-4 p225
	INT97			WKO[92]	
	INT98			WKO[93]	
	INT99			WKO[94]	
	INT100			WKO[95]	
	INT101			WKO[96]	
	INT102			WKO[97]	
	INT103			WKO[98]	
13	INT104	External/WUC	High-Level Trig (Not Adjustable)	WKO[99]	Figure 7-4 p225
	INT105			WKO[100]	
	INT106			WKO[101]	
	INT107			WKO[102]	
	INT108			WKO[103]	
	INT109			WKO[104]	
	INT110			WKO[105]	
	INT111			WKO[106]	
14	INT112	External/WUC	High-Level Trig (Not Adjustable)	WKO[107]	Figure 7-4 p225
	INT113			WKO[108]	
	INT114			WKO[109]	
	INT115			WKO[110]	
	INT116			WKO[111]	
	INT117			WKO[112]	
	INT118			WKO[113]	
	INT119			WKO[114]	
15	INT120	External/WUC	High-Level Trig (Not Adjustable)	WKO[115]	Figure 7-4 p225
	INT121			WKO[116]	
	INT122			WKO[117]	
	INT123			WKO[118]	
	INT124			WKO[119]	
	INT125			WKO[120]	
	INT126			WKO[121]	
	INT127			WKO[122]	

Group	Interrupt	Source	Default Type(Adjustable)	Description	Reference
16	INT128	External/WUC	High-Level Trig (Not Adjustable)	WKO[128]	Figure 7-4 p225
	INT129			WKO[129]	
	INT130			WKO[130]	
	INT131			WKO[131]	
	INT132			WKO[132]	
	INT133			WKO[133]	
	INT134			WKO[134]	
	INT135			WKO[135]	
17	-	-	-	Reserved	-
18	INT144	-	-	Reserved	-
	INT145	-	-	Reserved	-
	INT146	-	-	Reserved	-
	INT147	-	-	Reserved	-
	INT148	External/WUC	High-Level Trig (Not Adjustable)	WKO[127]	Figure 7-4 p225
	INT149	Internal	High-Level Trig (Not Adjustable)	PMC5 Output Buffer Empty Intr.	Section 6.7.3.1, p166
	INT150	Internal	High-Level Trig (Not Adjustable)	PMC5 Input Buffer Full Intr.	Section 6.7.3.1, p166
	INT151	Internal	High-Level Trig (Not Adjustable)	Voltage Comparator Interrupt	Section 7.11.3.1, p363
19	INT152	Internal	High-Level Trig (Not Adjustable)	PECI Interrupt	Section 7.8, p347
	INT153	Internal	High-Level Trig (Not Adjustable)	eSPI Interrupt	Section 1, p47
	INT154	Internal	High-Level Trig (Not Adjustable)	eSPI VW Interrupt	Section 1, p47
	INT155	Internal	High-Level Trig (Not Adjustable)	Port 80h/81h Interrupt	Section 7.17.4.26, p1
	INT156	-	-	Reserved	-
	INT157	Internal	Rising-Edge Trig (Not Adjustable)	External Timer 3 Interrupt	Section 7.16.3, p432
	INT158	Internal	High-Level Trig	Software Interrupt	-
	INT159	Internal	Edge Trig (Always Enabled)	PLL Frequency Change Event Interrupt	-

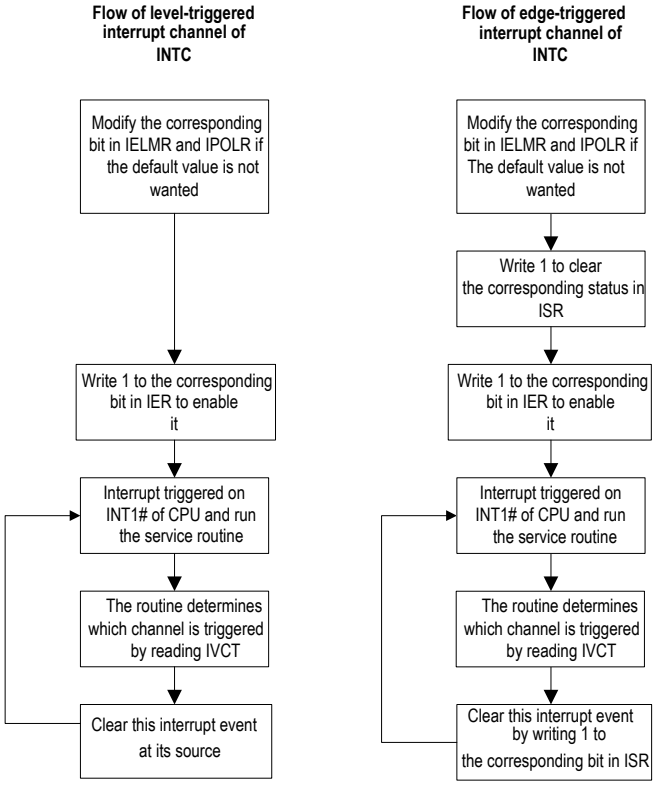
Group	Interrupt	Source	Default Type(Adjustable)	Description	Reference
20	INT160	Internal	High-Level Trig (Not Adjustable)	SMBus E Interrupt	Table 7-12 , p310
	INT161	Internal	High-Level Trig (Not Adjustable)	SMBus F Interrupt	Table 7-12 , p310
	INT162	-	-	Reserved	-
	INT163	-	-	Reserved	-
	INT164	-	-	Reserved	-
	INT165	-	-	Reserved	-
	INT166	-	-	Reserved	-
	INT167	-	-	Reserved	-
21	INT168	-	-	Reserved	-
	INT169	-	-	Reserved	-
	INT170	-	-	Reserved	-
	INT171	-	-	Reserved	-
	INT172	-	-	Reserved	-
	INT173	-	-	Reserved	-
	INT174	Internal	High-Level Trig (Not Adjustable)	Debug UART Interrupt	Section 7.23.4.1, p500
	INT175	Internal	Rising-Edge Trig (Not Adjustable)	External Timer 4 Interrupt	Section 7.16.3, p432

Figure 7-2. INTC Simplified Diagram



7.2.6 Programming Guide

Figure 7-3. Program Flow Chart for INTC



Note: The routine may has its own interrupt priority by reading ISR register.
Note: If this channel source comes from WUC, the corresponding bit in WUESR needs to be cleared, too

7.3 Wake-Up Control (WUC)

7.3.1 Overview

WUC groups internal and external inputs, and asserts wake-up signals to INTC that allows CPU to exit an Doze/Deep Doze/Sleep mode.

7.3.2 Features

- Supports internal and external interrupt inputs.
- Supports both the rising-edge and falling-edge triggered mode.
- Input can be connected to INTC directly.

7.3.3 Functional Description

Input sources of WUC are external inputs such as pins about PS/2, GPIO and KB Matrix Scan, or inputs from internal module such as SWUC, LPC and SMBus that handle external inputs.

Each channel can be selected to be rising or falling edge triggered mode. If one channel is disabled, the input bypasses WUC pending logic and is connected directly to INTC.

7.3.4 EC Interface Registers

The EC interface registers are listed below. The base address for WUC is 1B00h.

Table 7-4. EC View Register Map, WUC

7 — 0	Offset
Wake-Up Edge Mode Register 1 (WUEMR1)	00h
Wake-Up Edge Mode Register 2 (WUEMR2)	01h
Wake-Up Edge Mode Register 3 (WUEMR3)	02h
Wake-Up Edge Mode Register 4 (WUEMR4)	03h
Wake-Up Edge Mode Register 6 (WUEMR6)	10h
Wake-Up Edge Mode Register 7 (WUEMR7)	14h
Wake-Up Edge Mode Register 8 (WUEMR8)	18h
Wake-Up Edge Mode Register 9 (WUEMR9)	1Ch
Wake-Up Edge Mode Register 10 (WUEMR10)	20h
Wake-Up Edge Mode Register 11 (WUEMR11)	24h
Wake-Up Edge Mode Register 12 (WUEMR12)	28h
Wake-Up Edge Mode Register 13 (WUEMR13)	2Ch
Wake-Up Edge Mode Register 14 (WUEMR14)	30h
Wake-Up Edge Sense Register 1 (WUESR1)	04h
Wake-Up Edge Sense Register 2 (WUESR2)	05h
Wake-Up Edge Sense Register 3 (WUESR3)	06h
Wake-Up Edge Sense Register 4 (WUESR4)	07h
Wake-Up Edge Sense Register 6 (WUESR6)	11h
Wake-Up Edge Sense Register 7 (WUESR7)	15h
Wake-Up Edge Sense Register 8 (WUESR8)	19h
Wake-Up Edge Sense Register 9 (WUESR9)	1Dh
Wake-Up Edge Sense Register 10 (WUESR10)	21h
Wake-Up Edge Sense Register 11 (WUESR11)	25h
Wake-Up Edge Sense Register 12 (WUESR12)	29h
Wake-Up Edge Sense Register 13 (WUESR13)	2Dh
Wake-Up Edge Sense Register 14 (WUESR14)	31h
Wake-Up Enable Register 1 (WUENR1)	08h
Wake-Up Enable Register 3 (WUENR3)	0Ah

7	0	Offset
Wake-Up Enable Register 4 (WUENR4)		0Bh

7.3.4.1 Wake-Up Edge Mode Register 1-14 (WUEMR1-WUEMR14)

This register configures the trigger mode of input signals Group x. (Refer to Table 7-5 on page 222)

WUEMR1 defined in Group 1
WUEMR2 defined in Group 2
WUEMR3 defined in Group 3
WUEMR4 defined in Group 4
WUEMR6 defined in Group 6
WUEMR7 defined in Group 7
WUEMR8 defined in Group 8
WUEMR9 defined in Group 9
WUEMR10 defined in Group 10
WUEMR11 defined in Group 11
WUEMR12 defined in Group 12
WUEMR13 defined in Group 13
WUEMR14 defined in Group 14

Address Offset: 00h-03h,10h,14h,18h,1Ch,20h,24h,28h,2Ch,30h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode Group x (WUEMGRx 7:0)** 0: Rising-edge triggered is selected.(for Group 1-14) 1: Falling-edge triggered is selected.(for all Group,except Group 7,10,12) or Either-edge (rising-edge or falling-edge) triggered is selected. (only for Group 7,10,12) Always write-1-clear to the corresponding bit in WUESR register after modifying these bits. Note: Where x means (1 – 14)

7.3.4.2 Wake-Up Edge Sense Register 1-14 (WUESR1-WUESR14)

This register indicates the occurrence of a selected trigger condition and is associated with input signals Group x. (Refer to Table 7-5 on page 222).

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

WUESR1 defined in Group 1
WUESR2 defined in Group 2
WUESR3 defined in Group 3
WUESR4 defined in Group 4
WUESR6 defined in Group 6
WUESR7 defined in Group 7
WUESR8 defined in Group 8
WUESR9 defined in Group 9
WUESR10 defined in Group 10
WUESR11 defined in Group 11
WUESR12 defined in Group 12
WUESR13 defined in Group 13
WUESR14 defined in Group 14

Address Offset: 04h-07h,11h,15h,19h,1Dh,21h,25h,29h,2Dh,31h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense Group x (WUSGRx 7:0)** For each bit: Read 1: It indicates a trigger condition occurs on the corresponding input. Read 0: Otherwise For each bit: Write 1: Clear this bit Write 0: No action Note: Where x means (1 - 14)

7.3.4.3 Wake-Up Enable Register 1/3/4 (WUENR1, WUENR3, WUENR4)

This register enables a wake-up function of the corresponding input signal Group x. (Refer to Table 7-5 on page 222).

Note: Only for Group 1/3/4

WUENR1 defined in Group 1
WUENR3 defined in Group 3
WUENR4 defined in Group 4

Address Offset: 08h,0Ah,0Bh

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable Group x (WUENGRx 7:0)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled but not pending. Note: Where x means (1 / 3 / 4)

7.3.5 WUC Input Assignments

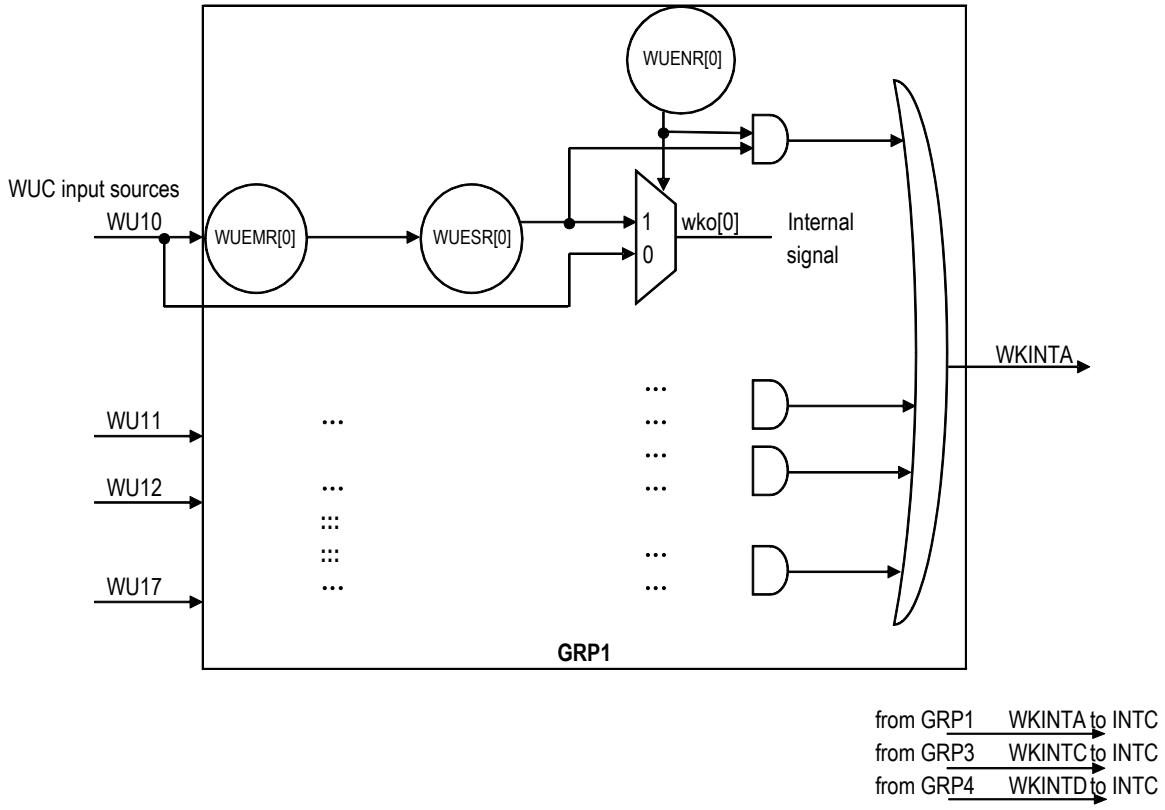
Table 7-5. WUC Input Assignments

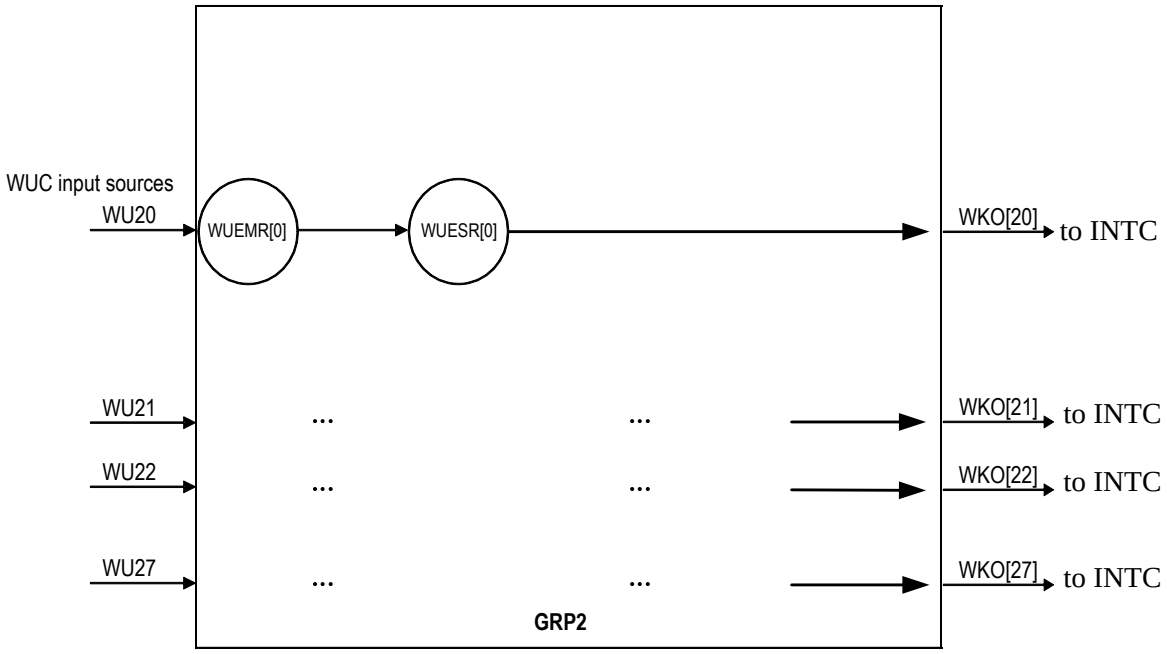
Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
1	WU10	PS2CLK0	External Source from Pin	WKINTA, to INT5	Rising Edge Trig
	WU11	PS2DAT0	External Source from Pin		Rising Edge Trig
	WU12	PS2CLK1	External Source from Pin		Rising Edge Trig
	WU13	PS2DAT1	External Source from Pin		Rising Edge Trig
	WU14	PS2CLK2	External Source from Pin		Rising Edge Trig
	WU15	PS2DAT2	External Source from Pin		Rising Edge Trig
	WU16	Reserved	-		-
	WU17	Reserved	-		-
2	WU20	WUI0	External Source from GPD0	WKO[20], to INT1	Rising Edge Trig
	WU21	WUI1	External Source from GPD1	WKO[21], to INT31	Rising Edge Trig
	WU22	WUI2	External Source from GPC4	WKO[22], to INT21	Rising Edge Trig
	WU23	WUI3	External Source from GPC6	WKO[23], to INT6	Rising Edge Trig
	WU24	WUI4	External Source from GPD2	WKO[24], to INT17	Rising Edge Trig
	WU25	PWRSW	External Source from GPE4	WKO[25], to INT14	Rising Edge Trig
	WU26	SWUC Wake Up	From SWUC Module	WKO[26], to INT12	Rising Edge Trig
	WU27	Reserved	-	-	-
3	WU30	KSI[0]	External Source from Pin	WKINTC, to INT13	Rising Edge Trig
	WU31	KSI[1]	External Source from Pin		Rising Edge Trig
	WU32	KSI[2]	External Source from Pin		Rising Edge Trig
	WU33	KSI[3]	External Source from Pin		Rising Edge Trig
	WU34	KSI[4]	External Source from Pin		Rising Edge Trig
	WU35	KSI[5]	External Source from Pin		Rising Edge Trig
	WU36	KSI[6]	External Source from Pin		Rising Edge Trig
	WU37	KSI[7]	External Source from Pin		Rising Edge Trig
4	WU40	WUI5	External Source from GPE5	WKINTD, to INT5	Rising Edge Trig
	WU41	CRX0/CRX1	External Source from Pin		Rising Edge Trig
	WU42	LPC Access	LPC Cycle with Address Recognized See also Section 6.2.6, p70		Rising Edge Trig
	WU43	SMDAT0	External Source from Pin		Rising Edge Trig
	WU44	SMDAT1	External Source from Pin		Rising Edge Trig
	WU45	WUI6	External Source from GPE6		Rising Edge Trig
	WU46	WUI7	External Source from GPE7		Rising Edge Trig
	WU47	SMDAT2	External Source from Pin		Rising Edge Trig
	-	-	-	-	-

Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
6	WU60	WUI16	External Source from GPH0	WKO[60], to INT48	Rising Edge Trig
	WU61	WUI17	External Source from GPH1	WKO[61], to INT49	Rising Edge Trig
	WU62	WUI18	External Source from GPH2	WKO[62], to INT50	Rising Edge Trig
	WU63	WUI19	External Source from GPH3	WKO[63], to INT51	Rising Edge Trig
	WU64	WUI20	External Source from GPF4	WKO[64], to INT52	Rising Edge Trig
	WU65	WUI21	External Source from GPF5	WKO[65], to INT53	Rising Edge Trig
	WU66	WUI22	External Source from GPF6	WKO[66], to INT54	Rising Edge Trig
	WU67	WUI23	External Source from GPF7	WKO[67], to INT55	Rising Edge Trig
7	WU70	WUI24	External Source from GPE0	WKO[70], to INT72	Rising Edge Trig
	WU71	WUI25	External Source from GPE1	WKO[71], to INT73	Rising Edge Trig
	WU72	WUI26	External Source from GPE2	WKO[72], to INT74	Rising Edge Trig
	WU73	WUI27	External Source from GPE3	WKO[73], to INT75	Rising Edge Trig
	WU74	WUI28	External Source from GPI4	WKO[74], to INT76	Rising Edge Trig
	WU75	WUI29	External Source from GPI5	WKO[75], to INT77	Rising Edge Trig
	WU76	WUI30	External Source from GPI6	WKO[76], to INT78	Rising Edge Trig
	WU77	WUI31	External Source from GPI7	WKO[77], to INT79	Rising Edge Trig
8	WU80	WUI32	External Source from GPA3	WKO[80], to INT88	Rising Edge Trig
	WU81	WUI33	External Source from GPA4	WKO[81], to INT89	Rising Edge Trig
	WU82	WUI34	External Source from GPA5	WKO[82], to INT90	Rising Edge Trig
	WU83	WUI35	External Source from GPA6	WKO[83], to INT91	Rising Edge Trig
	WU84	WUI36	External Source from GPB2	WKO[84], to INT92	Rising Edge Trig
	WU85	WUI37	External Source from GPC0	WKO[85], to INT93	Rising Edge Trig
	WU86	WUI38	External Source from GPC7	WKO[86], to INT94	Rising Edge Trig
	WU87	WUI39	External Source from GPD7	WKO[87], to INT95	Rising Edge Trig
9	WU88	WUI40	External Source from GPH4	WKO[88], to INT85	Rising Edge Trig
	WU89	WUI41	External Source from GPH5	WKO[89], to INT86	Rising Edge Trig
	WU90	WUI42	External Source from GPH6	WKO[90], to INT87	Rising Edge Trig
	WU91	WUI43	External Source from GPA0	WKO[91], to INT96	Rising Edge Trig
	WU92	WUI44	External Source from GPA1	WKO[92], to INT97	Rising Edge Trig
	WU93	WUI45	External Source from GPA2	WKO[93], to INT98	Rising Edge Trig
	WU94	WUI46	External Source from GPB4	WKO[94], to INT99	Rising Edge Trig
	WU95	WUI47	External Source from GPC2	WKO[95], to INT100	Rising Edge Trig
10	WU96	WUI48	External Source from GPF0	WKO[96], to INT101	Rising Edge Trig
	WU97	WUI49	External Source from GPF1	WKO[97], to INT102	Rising Edge Trig
	WU98	WUI50	External Source from GPF2	WKO[98], to INT103	Rising Edge Trig
	WU99	WUI51	External Source from GPF3	WKO[99], to INT104	Rising Edge Trig
	WU100	WUI52	External Source from GPA7	WKO[100], to INT105	Rising Edge Trig
	WU101	WUI53	External Source from GPB0	WKO[101], to INT106	Rising Edge Trig
	WU102	WUI54	External Source from GPB1	WKO[102], to INT107	Rising Edge Trig
	WU103	WUI55	External Source from GPB3	WKO[103], to INT108	Rising Edge Trig

Group	WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
11	WU104	WUI56	External Source from GPB5	WKO[104], to INT109	Rising Edge Trig
	WU105	WUI57	External Source from GPB6	WKO[105], to INT110	Rising Edge Trig
	WU106	WUI58	External Source from GPB7	WKO[106], to INT111	Rising Edge Trig
	WU107	WUI59	External Source from GPC1	WKO[107], to INT112	Rising Edge Trig
	WU108	WUI60	External Source from GPC3	WKO[108], to INT113	Rising Edge Trig
	WU109	WUI61	External Source from GPC5	WKO[109], to INT114	Rising Edge Trig
	WU110	WUI62	External Source from GPD3	WKO[110], to INT115	Rising Edge Trig
	WU111	WUI63	External Source from GPD4	WKO[111], to INT116	Rising Edge Trig
12	WU112	WUI64	External Source from GPD5	WKO[112], to INT117	Rising Edge Trig
	WU113	WUI65	External Source from GPD6	WKO[113], to INT118	Rising Edge Trig
	WU114	WUI66	External Source from GPE4	WKO[114], to INT119	Rising Edge Trig
	WU115	WUI67	External Source from GPG0	WKO[115], to INT120	Rising Edge Trig
	WU116	WUI68	External Source from GPG1	WKO[116], to INT121	Rising Edge Trig
	WU117	WUI69	External Source from GPG2	WKO[117], to INT122	Rising Edge Trig
	WU118	WUI70	External Source from GPG6	WKO[118], to INT123	Rising Edge Trig
	WU119	WUI71	External Source from GPI0	WKO[119], to INT124	Rising Edge Trig
13	WU120	WUI72	External Source from GPI1	WKO[120], to INT125	Rising Edge Trig
	WU121	WUI73	External Source from GPI2	WKO[121], to INT126	Rising Edge Trig
	WU122	WUI74	External Source from GPI3	WKO[122], to INT127	Rising Edge Trig
	WU123	-	Reserved	-	-
	WU124	-	Reserved	-	-
	WU125	-	Reserved	-	-
	WU126	-	Reserved	-	-
	WU127	WUI79	External Source from GPH7	WKO[127], to INT148	Rising Edge Trig
14	WU128	WUI80	External Source from GPJ0	WKO[128], to INT128	Rising Edge Trig
	WU129	WUI81	External Source from GPJ1	WKO[129], to INT129	Rising Edge Trig
	WU130	WUI82	External Source from GPJ2	WKO[130], to INT130	Rising Edge Trig
	WU131	WUI83	External Source from GPJ3	WKO[131], to INT131	Rising Edge Trig
	WU132	WUI84	External Source from GPJ4	WKO[132], to INT132	Rising Edge Trig
	WU133	WUI85	External Source from GPJ5	WKO[133], to INT133	Rising Edge Trig
	WU134	WUI86	External Source from GPJ6	WKO[134], to INT134	Rising Edge Trig
	WU135	WUI87	External Source from GPJ7	WKO[135], to INT135	Rising Edge Trig

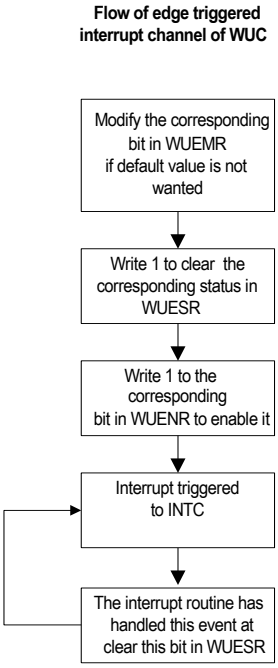
Figure 7-4. WUC Simplified Diagram





7.3.6 Programming Guide

Figure 7-5. Program Flow Chart for WUC



7.4 Keyboard Matrix Scan Controller

7.4.1 Overview

The module provides control for keyboard matrix scan.

7.4.2 Features

- Supports 18 x scan output
- Supports 8 x scan input
- Supports Schmitt trigger input pin
- Supports programmable pull-up on all output/input pins
- Supports one interrupt (connected to INT11 of INTC) for any KSI inputs to go low to wake up the system
- Supports GPIO mode for all KBS pins (GPIO mode overrides EPP mode)

7.4.3 Functional Description

- **KSI/KSO Used as Keyboard Matrix**

Normal usage.

- **KSI/KSO Used as GPIO**

If the EC is applied to a platform without keyboard matrix, KSI/KSO pins can be used as GPIO. See also Figure 7-43. Parallel Port Female 25-Pin Connector on page 505.

Table 7-6. KSI/KSO as GPIO List

KSI0/STB#	—	EPP Signal	Could be used as GPIO
KSI1/AFD#	Hardware strap	EPP Signal	Could be used as GPIO
KSI2/INIT#	Hardware strap	EPP Constant Signal	Could be used as GPIO
KSI3/SLIN#	—	EPP Signal	Could be used as GPIO
KSI4	Hardware strap	—	Could be used as GPIO
KSI5	Hardware strap	—	Could be used as GPIO
KSI6	—	—	Could be used as GPIO
KSI7	—	—	Could be used as GPIO
KSO0/PD0	—	EPP Signal	Could be used as GPIO
KSO1/PD1	—	EPP Signal	Could be used as GPIO
KSO2/PD2	—	EPP Signal	Could be used as GPIO
KSO3/PD3	—	EPP Signal	Could be used as GPIO
KSO4/PD4	—	EPP Signal	Could be used as GPIO
KSO5/PD5	—	EPP Signal	Could be used as GPIO
KSO6/PD6	—	EPP Signal	Could be used as GPIO
KSO7/PD7	—	EPP Signal	Could be used as GPIO
KSO8/ACK#	—	EPP Constant Signal	Could be used as GPIO
KSO9/BUSY	—	EPP Signal	Could be used as GPIO
KSO10/PE	—	EPP Constant Signal	Could be used as GPIO
KSO11/ERR#	—	EPP Constant Signal	Could be used as GPIO
KSO12/SLCT	—	EPP Constant Signal	Could be used as GPIO
KSO13	—	—	Could be used as GPIO
KSO14	—	—	Could be used as GPIO
KSO15	—	—	Could be used as GPIO

7.4.4 EC Interface Registers

The keyboard matrix scan registers are listed below. The base address is 1D00h.

Table 7-7. EC View Register Map, KB Scan

7 0	Offset
Keyboard Scan Out [7:0] (KSOL)	00h
Keyboard Scan Out [15:8] (KSOH1)	01h
Keyboard Scan Out Control (KSOCTRL)	02h
Keyboard Scan Out [17:16] (KSOH2)	03h
Keyboard Scan In [7:0] (KSI)	04h
Keyboard Scan In Control (KSICTRLR)	05h
Keyboard Scan In [7:0] GPIO Control Register (KSIGCTRL)	06h
Keyboard Scan In [7:0] GPIO Output Enable Register (KSIGOEN)	07h
Keyboard Scan In [7:0] GPIO Data Register (KSIGDAT)	08h
Keyboard Scan In [7:0] GPIO Data Mirror Register (KSIGDMRR)	09h
Keyboard Scan Out [15:8] GPIO Control Register (KSOHGCTRL)	0Ah
Keyboard Scan Out [15:8] GPIO Output Enable Register (KSOHGOEN)	0Bh
Keyboard Scan Out [15:8] GPIO Data Mirror Register (KSOHGDMRR)	0Ch
Keyboard Scan Out [7:0] GPIO Control Register (KSOLGCTRL)	0Dh
Keyboard Scan Out [7:0] GPIO Output Enable Register (KSOLGOEN)	0Eh
Keyboard Scan Out [7:0] GPIO Data Mirror Register (KSOLGDMRR)	0Fh
KSO0 Low Scan Data Register (KSO0LSDR)	10h
KSO1 Low Scan Data Register (KSO1LSDR)	11h
KSO2 Low Scan Data Register (KSO2LSDR)	12h
KSO3 Low Scan Data Register (KSO3LSDR)	13h
KSO4 Low Scan Data Register (KSO4LSDR)	14h
KSO5 Low Scan Data Register (KSO5LSDR)	15h
KSO6 Low Scan Data Register (KSO6LSDR)	16h
KSO7 Low Scan Data Register (KSO7LSDR)	17h
KSO8 Low Scan Data Register (KSO8LSDR)	18h
KSO9 Low Scan Data Register (KSO9LSDR)	19h
KSO10 Low Scan Data Register (KSO10LSDR)	1Ah
KSO11 Low Scan Data Register (KSO11LSDR)	1Bh
KSO12 Low Scan Data Register (KSO12LSDR)	1Ch
KSO13 Low Scan Data Register (KSO13LSDR)	1Dh
KSO14 Low Scan Data Register (KSO14LSDR)	1Eh
KSO15 Low Scan Data Register (KSO15LSDR)	1Fh
KSO16 Low Scan Data Register (KSO16LSDR)	20h
KSO17 Low Scan Data Register (KSO17LSDR)	21h
Scan Data Control1 Register (SDC1R)	22h
Scan Data Control2 Register (SDC2R)	23h
Scan Data Control3 Register (SDC3R)	24h
Scan Data Status Register (SDSR)	25h
Keyboard Scan In [7:0] GPIO Open-Drain Register (KSIGPODR)	26h
Keyboard Scan Out [15:8] GPIO Open-Drain Register (KSOHGPODR)	27h
Keyboard Scan Out [7:0] GPIO Open-Drain Register (KSOLGPODR)	28h

7.4.4.1 Keyboard Scan Out Low Byte Data Register (KSOL)

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Keyboard Scan Out Low Data [7:0] (KSOL)** This is the 8-bit keyboard scan output register which controls the KSO[7:0] pins. In GPIO mode, this register is used as KSO[7:0] Data Register (refer to the related KSO GPIO registers).

7.4.4.2 Keyboard Scan Out High Byte Data 1 Register (KSOH1)

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Keyboard Scan Out High Data 1 [7:0] (KSOH1)** This is the 8-bit keyboard scan output register which controls the KSO[15:8] pins. In GPIO mode, this register is used as KSO[15:8] Data Register (Refer to the related KSO GPIO registers).

7.4.4.3 Keyboard Scan Out Control Register (KSOCTRL)

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-3	-	-	**Reserved**
2	R/W	0b	**KSO Pull Up (KSOPU)** Setting 1 enables the internal pull-up of the KSO[15:0] pins. To pull up KSO[17:16], set the GPCR registers of their corresponding GPIO ports. In GPIO mode, the internal pull-up of the pins KSO[15:0] is always disabled even if this bit is set.
1	-	-	**Reserved**
0	R/W	0b	**KSO Open Drain (KSOOD)** Setting 1 enables the open-drain mode of the KSO[17:0] pins. Setting 0 selects the push-pull mode. In GPIO mode, the open-drain mode of the pins KSO[15:0] is always disabled even if this bit is set.

7.4.4.4 Keyboard Scan Out High Byte Data 2 Register (KSOH2)

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Keyboard Scan Out High Data 2 [1:0] (KSOH2)** This is the 2-bit keyboard scan output register which controls the KSO[17:16] pins.

7.4.4.5 Keyboard Scan In Data Register (KSIR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	00h	**Keyboard Scan In High Data [7:0] (KSI)** This is the 8-bit keyboard scan input register which shows the value of the KSI[7:0] pins.

7.4.4.6 Keyboard Scan In Control Register (KSICTRLR)

Address Offset: 05h

Bit	R/W	Default	Description
7-5	-	000b	**Reserved**
4	R/W	0b	**Override PP from KBS (OVRPPK)** This bit overrides PP function which is enabled by hardware strap in KBS interface and disables it.
3	-	-	**Reserved**
2	R/W	0b	**KSI Pull Up (KSIPU)** Setting 1 enables the internal pull-up of the KSI[7:0] pins. In GPIO mode, the internal pull-up of the pins KSI[7:0] is always disabled even if this bit is set.
1	-	-	**Reserved**
0	-	-	**Reserved**

7.4.4.7 Keyboard Scan In [7:0] GPIO Control Register (KSIGCTRLR)

Address Offset: 06h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Control (KSI7GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSI6 GPIO Control (KSI6GCTRL)** 0: KBS mde 1: GPIO mode
5	R/W	0b	**KSI5 GPIO Control (KSI5GCTRL)** 0: KBS mode 1: GPIO mode
4	R/W	0b	**KSI4 GPIO Control (KSI4GCTRL)** 0: KBS mode 1: GPIO mode
3	R/W	0b	**KSI3 GPIO Control (KSI3GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSI2 GPIO Control (KSI2GCTRL)** 0: KBS mode 1: GPIO mode
1	R/W	0b	**KSI1 GPIO Control (KSI1GCTRL)** 0: KBS mode 1: GPIO mode
0	R/W	0b	**KSI0 GPIO Control (KSI0GCTRL)** 0: KBS mode 1: GPIO mode

7.4.4.8 Keyboard Scan In [7:0] GPIO Output Enable Register (KSIGOENR)

Address Offset: 07h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Output Enable (KSI7GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSI6 GPIO Output Enable (KSI6GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSI5 GPIO Output Enable (KSI5GOEN)** 0: Disable GPIO output 1: Enblae GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSI4 GPIO Output Enable (KSI4GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSI3 GPIO Output Enable (KSI3GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
2	R/W	0b	**KSI2 GPIO Output Enable (KSI2GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	R/W	0b	**KSI1 GPIO Output Enable (KSI1GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
0	R/W	0b	**KSI0 GPIO Output Enable (KSI0GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.4.4.9 Keyboard Scan In [7:0] GPIO Data Register (KSIGDATR)

Address Offset: 08h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Data (KSI7GDAT)** In GPIO mode, KSI7 will output this bit if the corresponding Output Enable bit is enabled.
6	R/W	0b	**KSI6 GPIO Data (KSI6GDAT)** In GPIO mode, KSI6 will output this bit if the corresponding Output Enable bit is enabled.
5	R/W	0b	**KSI5 GPIO Data (KSI5GDAT)** In GPIO mode, KSI5 will output this bit if the corresponding Output Enable bit is enabled.

Bit	R/W	Default	Description
4	R/W	0b	**KSI4 GPIO Data (KSI4GDAT)** In GPIO mode, KSI4 will output this bit if the corresponding Output Enable bit is enabled.
3	R/W	0b	**KSI3 GPIO Data (KSI3GDAT)** In GPIO mode, KSI3 will output this bit if the corresponding Output Enable bit is enabled.
2	R/W	0b	**KSI2 GPIO Data (KSI2GDAT)** In GPIO mode, KSI2 will output this bit if the corresponding Output Enable bit is enabled.
1	R/W	0b	**KSI1 GPIO Data (KSI1GDAT)** In GPIO mode, KSI1 will output this bit if the corresponding Output Enable bit is enabled.
0	R/W	0b	**KSI0 GPIO Data (KSI0GDAT)** In GPIO mode, KSI0 will output this bit if the corresponding Output Enable bit is enabled.

7.4.4.10 Keyboard Scan In [7:0] GPIO Data Mirror Register (KSIGDMRRR)

Address Offset: 09h

Bit	R/W	Default	Description
7	R	0b	**KSI7 GPIO Data Mirror (KSI7GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI7 status on reads.
6	R	0b	**KSI6 GPIO Data Mirror (KSI6GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI6 status on reads.
5	R	0b	**KSI5 GPIO Data Mirror (KSI5GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI5 status on reads.
4	R	0b	**KSI4 GPIO Data Mirror (KSI4GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI4 status on reads.
3	R	0b	**KSI3 GPIO Data Mirror (KSI3GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI3 status on reads.
2	R	0b	**KSI2 GPIO Data Mirror (KSI2GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI2 status on reads.
1	R	0b	**KSI1 GPIO Data Mirror (KSI1GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI1 status on reads.
0	R	0b	**KSI0 GPIO Data Mirror (KSI0GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI0 status on reads.

7.4.4.11 Keyboard Scan Out [15:8] GPIO Control Register (KSOHGCTRLR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 GPIO Control (KSO15GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSO14 GPIO Control (KSO14GCTRL)** 0: KBS mode 1: GPIO mode
5	R/W	0b	**KSO13 GPIO Control (KSO13GCTRL)** 0: KBS mode 1: GPIO mode
4	R/W	0b	**KSO12 GPIO Control (KSO12GCTRL)** 0: KBS mode 1: GPIO mode
3	R/W	0b	**KSO11 GPIO Control (KSO11GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSO10 GPIO Control (KSO10GCTRL)** 0: KBS mode 1: GPIO mode
1	R/W	0b	**KSO9 GPIO Control (KSO9GCTRL)** 0: KBS mode 1: GPIO mode
0	R/W	0b	**KSO8 GPIO Control (KSO8GCTRL)** 0: KBS mode 1: GPIO mode

7.4.4.12 Keyboard Scan Out [15:8] GPIO Output Enable Register (KSOHGOENR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 GPIO Output Enable (KSO15GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSO14 GPIO Output Enable (KSO14GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSO13 GPIO Output Enable (KSO13GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSO12 GPIO Output Enable (KSO12GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSO11 GPIO Output Enable (KSO11GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

Bit	R/W	Default	Description
2	R/W	0b	**KSO10 GPIO Output Enable (KSO10GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	R/W	0b	**KSO9 GPIO Output Enable (KSO9GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
0	R/W	0b	**KSO8 GPIO Output Enable (KSO8GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.4.4.13 Keyboard Scan Out [15:8] GPIO Data Mirror Register (KSOHGDMRRR)

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R	0b	**KSO15 GPIO Data Mirror (KSO15GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO15 status on reads.
6	R	0b	**KSO14 GPIO Data Mirror (KSO14GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO14 status on reads.
5	R	0b	**KSO13 GPIO Data Mirror (KSO13GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO13 status on reads.
4	R	0b	**KSO12 GPIO Data Mirror (KSO12GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO12 status on reads.
3	R	0b	**KSO11 GPIO Data Mirror (KSO11GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO11 status on reads.
2	R	0b	**KSO10 GPIO Data Mirror (KSO10GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO10 status on reads.
1	R	0b	**KSO9 GPIO Data Mirror (KSO9GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO9 status on reads.
0	R	0b	**KSO8 GPIO Data Mirror (KSO8GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO8 status on reads.

7.4.4.14 Keyboard Scan Out [7:0] GPIO Control Register (KSOLGCTRLR)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/W	0b	**KSO7 GPIO Control (KSO7GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSO6 GPIO Control (KSO6GCTRL)** 0: KBS mode 1: GPIO mode
5	R/W	0b	**KSO5 GPIO Control (KSO5GCTRL)** 0: KBS mode 1: GPIO mode
4	R/W	0b	**KSO4 GPIO Control (KSO4GCTRL)** 0: KBS mode 1: GPIO mode
3	R/W	0b	**KSO3 GPIO Control (KSO3GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSO2 GPIO Control (KSO2GCTRL)** 0: KBS mode 1: GPIO mode
1	R/W	0b	**KSO1 GPIO Control (KSO1GCTRL)** 0: KBS mode 1: GPIO mode
0	R/W	0b	**KSO0 GPIO Control (KSO0GCTRL)** 0: KBS mode 1: GPIO mode

7.4.4.15 Keyboard Scan Out [7:0] GPIO Output Enable Register (KSOLGOENR)

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R/W	0b	**KSO7 GPIO Output Enable (KSO7GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSO6 GPIO Output Enable (KSO6GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSO5 GPIO Output Enable (KSO5GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSO4 GPIO Output Enable (KSO4GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSO3 GPIO Output Enable (KSO3GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

Bit	R/W	Default	Description
2	R/W	0b	**KSO2 GPIO Output Enable (KSO2GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	R/W	0b	**KSO1 GPIO Output Enable (KSO1GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
0	R/W	0b	**KSO0 GPIO Output Enable (KSO0GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.4.4.16 Keyboard Scan Out [7:0] GPIO Data Mirror Register (KSOLGDMRRR)

Address Offset: 0Fh

Bit	R/W	Default	Description
7	R	0b	**KSO7 GPIO Data Mirror (KSO7GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO7 status on reads.
6	R	0b	**KSO6 GPIO Data Mirror (KSO6GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO6 status on reads.
5	R	0b	**KSO5 GPIO Data Mirror (KSO5GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO5 status on reads.
4	R	0b	**KSO4 GPIO Data Mirror (KSO4GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO4 status on reads.
3	R	0b	**KSO3 GPIO Data Mirror (KSO3GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO3 status on reads.
2	R	0b	**KSO2 GPIO Data Mirror (KSO2GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO2 status on reads.
1	R	0b	**KSO1 GPIO Data Mirror (KSO1GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO1 status on reads.
0	R	0b	**KSO0 GPIO Data Mirror (KSO0GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO0 status on reads.

7.4.4.17 KSO0 Low Scan Data Register (KSO0LSDR)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R	0b	**KSO0 Low Scan Data Register (KSO0LSDR)** This is the 8-bit keyboard scan data at the KSO0 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.18 KSO1 Low Scan Data Register (KSO1LSDR)

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R	0b	**KSO1 Low Scan Data Register (KSO1LSDR)** This is the 8-bit keyboard scan data at the KSO1 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.19 KSO2 Low Scan Data Register (KSO2LSDR)

Address Offset: 12h

Bit	R/W	Default	Description
7-0	R	0b	**KSO2 Low Scan Data Register (KSO2LSDR)** This is the 8-bit keyboard scan data at the KSO2 pin low.The Data Register is available for reading when Scan Data Valid is set.

7.4.4.20 KSO3 Low Scan Data Register (KSO3LSDR)

Address Offset: 13h

Bit	R/W	Default	Description
7-0	R	0b	**KSO3 Low Scan Data Register (KSO3LSDR)** This is the 8-bit keyboard scan data at the KSO3 pin low.The Data Register is available for reading when Scan Data Valid is set.

7.4.4.21 KSO4 Low Scan Data Register (KSO4LSDR)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R	0b	**KSO4 Low Scan Data Register (KSO4LSDR)** This is the 8-bit keyboard scan data at the KSO4 pin low.The Data Register is available for reading when Scan Data Valid is set.

7.4.4.22 KSO5 Low Scan Data Register (KSO5LSDR)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R	0b	**KSO5 Low Scan Data Register (KSO5LSDR)** This is the 8-bit keyboard scan data at the KSO5 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.23 KSO6 Low Scan Data Register (KSO6LSDR)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R	0b	**KSO6 Low Scan Data Register (KSO6LSDR)** This is the 8-bit keyboard scan data at the KSO6 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.24 KSO7 Low Scan Data Register (KSO7LSDR)

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R	0b	**KSO7 Low Scan Data Register (KSO7LSDR)** This is the 8-bit keyboard scan data at the KSO7 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.25 KSO8 Low Scan Data Register (KSO8LSDR)

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R	0b	**KSO8 Low Scan Data Register (KSO8LSDR)** This is the 8-bit keyboard scan data at the KSO8 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.26 KSO9 Low Scan Data Register (KSO9LSDR)

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R	0b	**KSO9 Low Scan Data Register (KSO9LSDR)** This is the 8-bit keyboard scan data at the KSO9 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.27 KSO10 Low Scan Data Register (KSO10LSDR)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R	0b	**KSO10 Low Scan Data Register (KSO10LSDR)** This is the 8-bit keyboard scan data at the KSO10 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.28 KSO11 Low Scan Data Register (KSO11LSDR)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-0	R	0b	**KSO11 Low Scan Data Register (KSO11LSDR)** This is the 8-bit keyboard scan data at the KSO11 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.29 KSO12 Low Scan Data Register (KSO12LSDR)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R	0b	**KSO12 Low Scan Data Register (KSO12LSDR)** This is the 8-bit keyboard scan data at the KSO12 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.30 KSO13 Low Scan Data Register (KSO13LSDR)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-0	R	0b	**KSO13 Low Scan Data Register (KSO13LSDR)** This is the 8-bit keyboard scan data at the KSO13 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.31 KSO14 Low Scan Data Register (KSO14LSDR)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	0b	**KSO14 Low Scan Data Register (KSO14LSDR)** This is the 8-bit keyboard scan data at the KSO14 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.32 KSO15 Low Scan Data Register (KSO15LSDR)

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	0b	**KSO15 Low Scan Data Register (KSO15LSDR)** This is the 8-bit keyboard scan data at the KSO15 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.33 KSO16 Low Scan Data Register (KSO16LSDR)

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	0b	**KSO16 Low Scan Data Register (KSO16LSDR)** This is the 8-bit keyboard scan data at the KSO16 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.34 KSO17 Low Scan Data Register (KSO17LSDR)

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	0b	**KSO17 Low Scan Data Register (KSO17LSDR)** This is the 8-bit keyboard scan data at the KSO17 pin low. The Data Register is available for reading when Scan Data Valid is set.

7.4.4.35 Scan Data Control1 Register (SDC1R)

Address Offset: 22h

Bit	R/W	Default	Description
7	R/W	0b	**Scan Data Enable (SDEN)** 0: Disable 1: Enable
6	-	-	**Reserved**
5	R/W	0b	**Interrupt from Scan Data Valid Enable (INTSDVEN)** 0: Disable valid interrupt to INT84 1: Enable valid interrupt to INT84
4-3	-	-	**Reserved**
2-0	R/W	001b	**Scan Loop Select (SLS)** 000b: Reserved 001b: 2 round 010b: 3 round 011b: 4 round 100b: 5 round 101b: 6 round 110b: 7 round 111b: 8 round

7.4.4.36 Scan Data Control2 Register (SDC2R)

Address Offset: 23h

Bit	R/W	Default	Description
7-6	R/W	00b	**KSO Pin Count Select (KSOPCS)** 00: 8x16 01: 8x17 10: 8x18 11: Reserved
5-4	-	-	**Reserved**
3-0	R/W	0h	**Wait KSO High Delay (WKSOHDLY)** 0h: 23 us 1h: 31 us 2h: 39 us 3h: 47 us 4h: 55 us 5h: 63 us 6h: 71 us 7h: 79 us 8h: 87 us 9h: 95 us Other: Reserved

7.4.4.37 Scan Data Control3 Register (SDC3R)

Address Offset: 24h

Bit	R/W	Default	Description
7-4	R/W	0h	**Wait KSO Low Delay (WKSOLDLY)** 0h: 11 us 1h: 13 us 2h: 15 us 3h: 17 us 4h: 19 us 5h: 21 us 6h: 23 us 7h: 25 us 8h: 27 us 9h: 29 us Other: Reserved
3-0	R/W	0h	**Spacing Delay Between Rounds (SDLYBR)** 0h: 0 ms 1h: 1 ms 2h: 2 ms 3h: 3 ms 4h: 4 ms 5h: 5 ms 6h: 6 ms 7h: 7 ms 8h: 8 ms 9h: 9 ms Ah: 10 ms Bh: 11 ms Ch: 12 ms Dh: 13 ms Eh: 14 ms Fh: 15 ms

7.4.4.38 Scan Data Status Register (SDSR)

Address Offset: 25h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/WC	0b	**Scan Data Valid (SDV)** This bit is write cleared. 0: Data not available 1: Data valid

7.4.4.39 Keyboard Scan In [7:0] GPIO Open-Drain Register (KSIGPODR)

Address Offset: 26h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 Output Open-Drain Enable (KSI7ODEN)** 0b: Configure KSI7 as push-pull if this pin is set GPO. 1b: Configure KSI7 as open-drain if this pin is set GPO.
6	R/W	0b	**KSI6 Output Open-Drain Enable (KSI6ODEN)** 0b: Configure KSI6 as push-pull if this pin is set GPO. 1b: Configure KSI6 as open-drain if this pin is set GPO.
5	R/W	0b	**KSI5 Output Open-Drain Enable (KSI5ODEN)** 0b: Configure KSI5 as push-pull if this pin is set GPO. 1b: Configure KSI5 as open-drain if this pin is set GPO.
4	R/W	0b	**KSI4 Output Open-Drain Enable (KSI4ODEN)** 0b: Configure KSI4 as push-pull if this pin is set GPO. 1b: Configure KSI4 as open-drain if this pin is set GPO.
3	R/W	0b	**KSI3 Output Open-Drain Enable (KSI3ODEN)** 0b: Configure KSI3 as push-pull if this pin is set GPO. 1b: Configure KSI3 as open-drain if this pin is set GPO.
2	R/W	0b	**KSI2 Output Open-Drain Enable (KSI2ODEN)** 0b: Configure KSI2 as push-pull if this pin is set GPO. 1b: Configure KSI2 as open-drain if this pin is set GPO.
1	R/W	0b	**KSI1 Output Open-Drain Enable (KSI1ODEN)** 0b: Configure KSI1 as push-pull if this pin is set GPO. 1b: Configure KSI1 as open-drain if this pin is set GPO.
0	R/W	0b	**KSI0 Output Open-Drain Enable (KSI0ODEN)** 0b: Configure KSI0 as push-pull if this pin is set GPO. 1b: Configure KSI0 as open-drain if this pin is set GPO.

7.4.4.40 Keyboard Scan Out [15:8] GPIO Open-Drain Register (KSOHGPODR)

Address Offset: 27h

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 Output Open-Drain Enable (KSO15ODEN)** 0b: Configure KSO15 as push-pull if this pin is set GPO. 1b: Configure KSO15 as open-drain if this pin is set GPO.
6	R/W	0b	**KSO14 Output Open-Drain Enable (KSO14ODEN)** 0b: Configure KSO14 as push-pull if this pin is set GPO. 1b: Configure KSO14 as open-drain if this pin is set GPO.
5	R/W	0b	**KSO13 Output Open-Drain Enable (KSO13ODEN)** 0b: Configure KSO13 as push-pull if this pin is set GPO. 1b: Configure KSO13 as open-drain if this pin is set GPO.
4	R/W	0b	**KSO12 Output Open-Drain Enable (KSO12ODEN)** 0b: Configure KSO12 as push-pull if this pin is set GPO. 1b: Configure KSO12 as open-drain if this pin is set GPO.
3	R/W	0b	**KSO11 Output Open-Drain Enable (KSO11ODEN)** 0b: Configure KSO11 as push-pull if this pin is set GPO. 1b: Configure KSO11 as open-drain if this pin is set GPO.
2	R/W	0b	**KSO10 Output Open-Drain Enable (KSO10ODEN)** 0b: Configure KSO10 as push-pull if this pin is set GPO. 1b: Configure KSO10 as open-drain if this pin is set GPO.

Bit	R/W	Default	Description
1	R/W	0b	**KSO9 Output Open-Drain Enable (KSO9ODEN)** 0b: Configure KSO9 as push-pull if this pin is set GPO. 1b: Configure KSO9 as open-drain if this pin is set GPO.
0	R/W	0b	**KSO8 Output Open-Drain Enable (KSO8ODEN)** 0b: Configure KSO8 as push-pull if this pin is set GPO. 1b: Configure KSO8 as open-drain if this pin is set GPO.

7.4.4.41 Keyboard Scan Out [7:0] GPIO Open-Drain Register (KSOLGPODR)

Address Offset: 28h

Bit	R/W	Default	Description
7	R/W	0b	**KSO7 Output Open-Drain Enable (KSO7ODEN)** 0b: Configure KSO7 as push-pull if this pin is set GPO. 1b: Configure KSO7 as open-drain if this pin is set GPO.
6	R/W	0b	**KSO6 Output Open-Drain Enable (KSO6ODEN)** 0b: Configure KSO6 as push-pull if this pin is set GPO. 1b: Configure KSO6 as open-drain if this pin is set GPO.
5	R/W	0b	**KSO5 Output Open-Drain Enable (KSO5ODEN)** 0b: Configure KSO5 as push-pull if this pin is set GPO. 1b: Configure KSO5 as open-drain if this pin is set GPO.
4	R/W	0b	**KSO4 Output Open-Drain Enable (KSO4ODEN)** 0b: Configure KSO4 as push-pull if this pin is set GPO. 1b: Configure KSO4 as open-drain if this pin is set GPO.
3	R/W	0b	**KSO3 Output Open-Drain Enable (KSO3ODEN)** 0b: Configure KSO3 as push-pull if this pin is set GPO. 1b: Configure KSO3 as open-drain if this pin is set GPO.
2	R/W	0b	**KSO2 Output Open-Drain Enable (KSO2ODEN)** 0b: Configure KSO2 as push-pull if this pin is set GPO. 1b: Configure KSO2 as open-drain if this pin is set GPO.
1	R/W	0b	**KSO1 Output Open-Drain Enable (KSO1ODEN)** 0b: Configure KSO1 as push-pull if this pin is set GPO. 1b: Configure KSO1 as open-drain if this pin is set GPO.
0	R/W	0b	**KSO0 Output Open-Drain Enable (KSO0ODEN)** 0b: Configure KSO0 as push-pull if this pin is set GPO. 1b: Configure KSO0 as open-drain if this pin is set GPO.

7.5 General Purpose I/O Port (GPIO)

7.5.1 Overview

The General Purpose I/O Port is composed of independent I/O pins controlled by registers.

There are also other available general purpose I/O such as External GPIO Control (EGPC) and hardware strap ID7-0

7.5.2 Features

- I/O pins individually configured as input, output or alternate function
- Supports 83-port GPIO with serial flash
- Configurable internal pull-up resistors
- Configurable internal pull-down resistors
- Supports Schmitt-Trigger input on all ports except group I and group J

7.5.3 EC Interface Registers

The EC interface registers are listed below. The base address for GPIO is 1600h.

Table 7-8. EC View Register Map, GPIO

7 0	Offset
General Control Register (GCR)	00h
General Control 1 Register (GCR1)	F0h
General Control 2 Register (GCR2)	F1h
General Control 3 Register (GCR3)	F2h
General Control 4 Register (GCR4)	F3h
General Control 5 Register (GCR5)	F4h
General Control 6 Register (GCR6)	F5h
General Control 7 Register (GCR7)	F6h
General Control 8 Register (GCR8)	F7h
General Control 9 Register (GCR9)	F8h
General Control 10 Register (GCR10)	F9h
General Control 11 Register (GCR11)	FAh
General Control 12 Register (GCR12)	FBh
General Control 13 Register (GCR13)	FCh
General Control 14 Register (GCR14)	FDh
General Control 15 Register (GCR15)	FEh
General Control 16 Register (GCR16)	E0h
General Control 17 Register (GCR17)	E1h
General Control 18 Register (GCR18)	E2h
General Control 19 Register (GCR19)	E4h
General Control 20 Register (GCR20)	E5h
General Control 21 Register (GCR21)	E6h
General Control 22 Register (GCR22)	E7h
General Control 23 Register (GCR23)	E8h
Power Good Watch Control Register (PGWCR)	FFh
Port Data Register (GPDRA)	01h
Port Data Register (GPDRB)	02h
…	…
Port Data Register (GPDRJ)	0Ah
Port Data Register (GPDRM)	0Dh
Port Control n Registers (GPCRA0)	10h
Port Control n Registers (GPCRA1)	11h

7 … 0	Offset
…	…
Port Control n Registers (GPCRJ5)	5Dh
Port Control n Registers (GPCRM0)	A0h
...	...
Port Control n Registers (GPCRM6)	A6h
Port Data Mirror Register (GPDMRA)	61h
Port Data Mirror Register (GPDMRB)	62h
…	…
Port Data Mirror Register (GPDMRJ)	6Ah
Port Data Mirror Register (GPDMRM)	6Dh
Output Type Register (GPOTA)	71h
Output Type Register (GPOTB)	72h
Output Type Register (GPOTD)	74h
Output Type Register (GPOTE)	75h
Output Type Register (GPOTF)	76h
Output Type Register (GPOTH)	78h
Output Type Register (GPOTJ)	7Ah

7.5.3.1 General Control Register (GCR)

This register individually controls the bus state of each port. The input gating and output floating control signals can be used to reduce power consumption in various system conditions.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	0h	**GPB5 Follow LPCRST# Enable (GFLE)** 1: Refer to GFLES0 bit in this register 0: Otherwise Note that GA20 is function 1 of GPB5, LPCRST# is function 1 of GPD2 and WUI4 is function 2 of GPD2.
6	R/W	0b	**Reserved**
5	R/W	0b	**Reserved**
4-3	-	00b	**Reserved**
2-1	R/W	10b	**LPC Reset Enable (LPCRSTEN)** 00: Reserved 01: LPC Reset is enabled on GPB7. 10: LPC Reset is enabled on GPD2. 11: LPC Reset is disabled.
0	R/W	0b	**GFLE Set (GFLES0)** 1: GPDRB bit 5 will be set if WUI4 is level-low. 0: GPDRB bit 5 will be set immediately if there is a high-to-low transition on WUI4. If this “set” action occurs between a “reading from GPDRB” and “writing to GPDRB”, the GPDRB bit 5 is not writable in the “writing to GPDRB” action.

7.5.3.2 General Control 1 Register (GCR1)

Address Offset: F0h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Support SSPI BUSY Pin (SSSPIBP)** 0b: SSPI does not support BUSY pin 1b: SSPI supports BUSY pin
5-4	R/W	00b	**SPI Control (SPICTRL)** If this field is zero, the corresponding function 3 of SPI is disabled. Otherwise, partial of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: SPI channel 0 and channel 1 are disabled. 10b: SSCK/SMOSI/SMISO/SSCE1# are enabled. 01b: SSCK/SMOSI/SMISO/SSCE0# are enabled. 11b: SSCK/SMOSI/SMISO/SSCE1#/SSCE0# are enabled.
3-2	R/W	00b	**UART2 Control (U2CTRL)** If this field is zero, the corresponding function 3 of UART2 is disabled. Otherwise, partial or all of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: UART2 is disabled. 01b: SIN1/SOUT1 are enabled. 10b: SIN1/SOUT1/DSR1#/RTS1#/DTR1#/CTS1#/DCD1# are enabled. 11b: SIN1/SOUT1/DSR1#/RTS1#/DTR1#/CTS1#/DCD1#/RIG1# are enabled.
1-0	R/W	00b	**UART1 Control (U1CTRL)** If this field is zero, the corresponding function 3 of UART1 is disabled. Otherwise, partial or all of them are set as function 3 if their corresponding GPCRn is 00b. 00b: UART1 is disabled. 01b: SIN0/SOUT0 are enabled. 10b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0#/DCD0# are enabled. 11b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0#/DCD0#/RIG0# are enabled.

7.5.3.3 General Control 2 Register (GCR2)

Address Offset: F1h

Bit	R/W	Default	Description
7	R/W	0b	**TACH2A Enable (TACH2AEN)** 0b: Disable 1b: GPJ0 will select TACH2A as its alternative function. Refer to Table 7-9. GPIO Alternate Function on page 263.
6	R/W	0b	**CK32K Out Enable (CK32OE)** Refer to Table 7-9. GPIO Alternate Function on page 263.
5	R/W	0b	**SMBus Channel 3 Enable (SMB3EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.
4	R/W	0b	**PECI Enable (PECIE)** Refer to Table 7-9. GPIO Alternate Function on page 263.
3	R/W	0b	**TMB1 Enabled (TMB1EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.

Bit	R/W	Default	Description
2	R/W	0b	**TMB0 Enabled (TMB0EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.
1	R/W	0b	**TMA1 Enabled (TMA1EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.
0	R/W	0b	**TMA0 Enabled (TMA0EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.

7.5.3.4 General Control 3 Register (GCR3)

If VCC power-down and I/O port pins have been configured as their respective alternative function mode, enabling these bits will turn off corresponding I/O port pins.

Address Offset: F2h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	1b	**PECI VCC Power-down Gating (PECIPDG)** 0b: Disable 1b: Turn off PECI related pins if VCC power-down.
5	R/W	0b	**UART2 VCC Power-down Gating (UART2PDG)** 0b: Disable 1b: Turn off UART2 related pins if VCC power-down.
4	R/W	0b	**UART1 VCC Power-down Gating (UART1PDG)** 0b: Disable 1b: Turn off UART1 related pins if VCC power-down.
3	R/W	0b	**SSPI VCC Power-down Gating (SSPIPDG)** 0b: Disable 1b: Turn off SSPI related pins if VCC power-down.
2	-	-	**Reserved**
1	R/W	0b	**ECSMI#/ECSCI# VCC Power-down Gating (EEPDG)** 0b: Disable 1b: Turn off ECSMI#/ECSCI# related pins if VCC power-down. Please note that this feature is regardless of the GPMD field in GPCR register for EEPDG bit.
0	R/W	0b	**CLKRUN#/GA20/KBRST# VCC Power-down Gating (CGKPDG)** 0b: Disable 1b: Turn off CLKRUN#/GA20/KBRST# related pins if VCC power-down. Please note that this feature is regardless of the GPMD field in GPCR register for CGKPDG bit.

7.5.3.5 General Control 4 Register (GCR4)

Address Offset: F3h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/W	000b	**Hardware Bypass Enable (HWBPE)** 000b: Disable 001b: GPI6 input will be directly bypassed to BAO. 010b: GPI7 input willl be directly bypassed to BBO. 011b: GPI6/GPI7 input will be directly bypassed to BAO/BBO. 101b: GPI6 input will be directly bypassed to BAO and BBO. Others: Reserved.

7.5.3.6 General Control 5 Register (GCR5)

Address Offset: F4h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	000b	**Power Good Watch Delay Time (PLR2DLY)** These bits control the delay time of Power Good Watch function. 000b: About 100 ms. 001b: About 500 ms. 010b: About 1000 ms. 011b: About 1500 ms. 100b: About 2000 ms. 101b: About 2500 ms. 110b: About 3000 ms. 111b: About 4000 ms.
3	R/W	0b	**Power Good Drop Pin Select (PGDRPSEL)** This bit controls the selection of the drop pins while power good watch condition occurs. 0b: GPB5-7, GPJ1, GPH0-7, GPE0-7 and GPG1/2/6 will be reset. 1b: GPB5-7, GPJ1 and GPH0-7 will be reset.
2	R/W	0b	**Power Good Watch Enable (PGOODEN)** 0b: Power Good Watch function is disabled. 1b: Power Good Watch function is enabled. This bit will be cleared when power good watch condition is detected. Please note that whether GPH0-6 will be reset or not is controlled by the PGDRPSEL bit.
1	R/W	0b	**TACH1B Enable (TACH1BEN)** 0b: Disable 1b: GPJ3 will select TACH1B as its alternative function. Refer to Table 7-9. GPIO Alternate Function on page 263.
0	R/W	0b	**TACH0B Enable (TACH0BEN)** 0b: Disable 1b: GPJ2 will select TACH0B as its alternative function. Refer to Table 7-9. GPIO Alternate Function on page 263.

7.5.3.7 General Control 6 Register (GCR6)

Address Offset: F5h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5	R/W	0b	**Power Good Watch Pin Select (PGWPSEL)** This bit controls the selection of the watch pin in power good watch function. 0b: GPIOH4 is selected. 1b: GPIOE0 is selected.
4	-	-	**Reserved**
3	R/W	1b	**UART SOUT1 Enable (SOUT1EN)** This bit enables the transmitter of UART2 separately. 0b: SOUT1 is disabled. 1b: SOUT1 is enabled.

Bit	R/W	Default	Description
2	R/W	1b	**UART SIN1 Enable (SIN1EN)** This bit enables the receiver of UART2 separately. 0b: SIN1 is disabled. 1b: SIN1 is enabled.
1	R/W	1b	**UART SOUT0 Enable (SOUT0EN)** This bit enables the transmitter of UART1 separately. 0b: SOUT0 is disabled. 1b: SOUT0 is enabled.
0	R/W	1b	**UART SIN0 Enable (SIN0EN)** This bit enables the receiver of UART1 separately. 0b: SIN0 is disabled. 1b: SIN0 is enabled.

7.5.3.8 General Control 7 Register (GCR7)

Address Offset: F6h

Bit	R/W	Default	Description
7	R/W	0b	**SMCLK2 Pin Switch (SMCLK2PS)** 0b: SMCLK2 is located on GPF6. 1b: SMCLK2 is located on GPC7. Refer to Table 7-9. GPIO Alternate Function on page 263.
6-0	-	-	**Reserved**

7.5.3.9 General Control 8 Register (GCR8)

Address Offset: F7h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**CEC Enable (CECEN)** Refer to Table 7-9. GPIO Alternate Function on page 263.
4	R/W	0b	**PWRSW WDT 2 Enable 1 (PWSW2EN1)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT2CNTR on page 251. Write 1b: Set bit and enable WDT 2. Write 0b: Ignored Read returns the last written data. Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
3-2	R/W	00b	**UART2 Control 2 (U2CTRL2)** If this field is zero, the corresponding function 3 of UART2 is disabled when U2CTRL is set to 00b. Otherwise, partial or all of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: UART2 is disabled when U2CTRL is set to 00b. 01b: SIN1/SOUT1/RTS1# are enabled. 10b: SIN1/SOUT1/RTS1#/CTS1# are enabled. 11b: SIN1/SOUT1/DSR1#/RTS1#/DTR1#/CTS1# are enabled.

Bit	R/W	Default	Description
1-0	R/W	00b	**UART1 Control 2 (U1CTRL2)** If this field is zero, the corresponding function 3 of UART1 is disabled when U1CTRL is set to 00b. Otherwise, partial or all of them are set as function 3 if their corresponding GPCRn is 00b. 00b: UART1 is disabled when U1CTRL is set to 00b. 01b: SIN0/SOUT0/RTS0# are enabled. 10b: SIN0/SOUT0/RTS0#/CTS0# are enabled. 11b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0# are enabled.

7.5.3.10 General Control 9 Register (GCR9)

Address Offset: F8h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**PWRSW WDT 2 Output Reset Pulse Polarity (PWSW2RPP)** A timeout reset event will be asserted to generate an active high or low pulse on GPI5 after PWRSW has been pulled low for more than a determined period. 1: Active high 0: Active low
5	R/W	0b	**PWRSW WDT 2 Enable 2 (PWSW2EN2)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT2CNTR on page 251. 0b: Disable 1b: Dedicate PWRSW to timeout reset function. Write 1b: Set bit and enable WDT 2. Write 0b: Clear bit. The WDT 2 is enabled by (PWSW2EN1 | PWSW2EN2) Read returns the last written data.
4	-	-	**Reserved**
3	R/W	0b	**PWRSW WDT 2 GPO Output Enable (PWSWDT2GPEN)** A timeout reset event will be asserted to generate an active high or low pulse (decided by PWSW2RPP) on GPI5 after PWRSW has been pulled low for more than a determined period. 0b: Disable 1b: Enable Note: GPI5 should be alternate function.
2	R/W	0b	**PWRSW WDT 1 Enable 2 (PWSW1EN2)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT1CNTR on page 252. Write 1b: Set bit, enable WDT 1, and touch (re-start) WDT 1. Write 0b: Clear bit. The WDT 1 is enabled by (PWSW1EN1 | PWSW1EN2) Read returns the last written data.

Bit	R/W	Default	Description
1	R/W	0b	**PWRSW WDT 1 Enable 1 (PWSW1EN1)** A timeout reset event will be asserted to reset EC after PWRSW has been pulled low for more than a determined period indicated by PWDT1CNTR on page 252. Write 1b: Set bit and enable WDT 1. Write 0b: Ignored Read returns the last written data. Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
0	R/W	0b	**Check PWRSW (CHKPWRSW)** 0: WDT1/2 counts only if PWRSW low, otherwise cleared. 1: WDT1/2 counts only if PWRSW low and GPE6 high, otherwise cleared.

7.5.3.11 General Control 10 Register (GCR10)

Address Offset: F9h

Bit	R/W	Default	Description
7-5	R/W	000b	**PWRSW WDT 2 Output Reset Pulse Width (PWSW2RPW)** This is the generated pulse width on GPI5 after PWRSW has been pulled low for more than a determined period. 000b: 30 us 001b: 200 ms 010b: 3 sec Others: Reserved Note: It also means delay 30 us/200 ms/3 sec to reset EC.
4-3	-	-	**Reserved**
2-0	R/W	000b	**PWRSW WDT 2 Counter Byte (PWDT2CNTR)** Selective WDT 2 timeout periods. 000b: 10 sec 001b: 8 sec 010b: 12 sec 100b: 7.5 sec 111b: 15 sec Others: Reserved The register content is not writable if PWSW2EN1 is set. The register content is reloaded when counter state is from “clear” to “count”.

7.5.3.12 General Control 11 Register (GCR11)

Address Offset: FAh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0000b	**PWRSW WDT 1 Counter Byte (PWDT1CNTR)** Selective WDT 1 timeout periods. 0000b: 4 sec 0001b: 5 sec 0010b: 6 sec 0011b: 7 sec 0100b: 8 sec 0101b: 9 sec 0110b: 10 sec 0111b: 11 sec 1000b: 12 sec Others: Reserved The register content is reloaded when counter state is from “clear” to “count”.

7.5.3.13 General Control 12 Register (GCR12)

Address Offset: FBh

Bit	R/W	Default	Description
7-0	R/W	00h	**GPIO Lock Authentication Data (GLAD)** The lock state is default off. Write: If the lock state is off, write Auth. Data will enable lock state. If the lock state is on, write the same Auth. Data will disable lock state. Read : 00h: The lock state is off. 01h: The lock state is on.

7.5.3.14 General Control 13 Register (GCR13)

Address Offset: FCh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**GPIOJ0 Lock Enable (GPJ0LE)** Enabling this bit will lock the output state of GPIOJ0. Note: This bit can be changed only when the lock state is off.
1	R/W	0b	**GPIOD7 Lock Enable (GPD7LE)** Enabling this bit will lock the output state of GPIOD7. Note: This bit can be changed only when the lock state is off.
0	R/W	0b	**GPIOD6 Lock Enable (GPD6LE)** Enabling this bit will lock the output state of GPIOD6. Note: This bit can be changed only when the lock state is off.

7.5.3.15 General Control 14 Register (GCR14)

Address Offset: FDh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**WUI Debounce Independent Enable (WUIDIE)** Debounce Independent for WUI0, WUI1, WUI2, WUI3, WUI5, and PWRSW 0b: Disable 1b: Enable
2-0	R/W	0h	**WUI Debounce Select (WUIDS)** Debounce WUI inputs from WUI0,WUI1,WUI2,WUI3,WUI5, and PWRSW. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.5.3.16 General Control 15 Register (GCR15)

Address Offset: FEh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**SMBus Channel 5 Enable (SMB5EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.
4	R/W	0b	**SMBus Channel 4 Enable (SMB4EN)** Refer to Table 7-9. GPIO Alternate Function on page 263.
3	R/W	0b	**TACH2B Enable (TACH2BEN)** 0b: Disable 1b: GPJ1 will select TACH2B as its alternative function. Refer to Table 7-9. GPIO Alternate Function on page 263.
2	R/W	0b	**Comparator 2 GPIO Enable (CMP2GPEN)** Comparator 2 output to GPJ5 0b: Disable 1b: Enable
1	R/W	0b	**Comparator 1 GPIO Enable (CMP1GPEN)** Comparator 1 output to GPJ4 0b: Disable 1b: Enable
0	R/W	0b	**Comparator 0 GPIO Enable (CMP0GPEN)** Comparator 0 output to GPJ3 0b: Disable 1b: Enable

7.5.3.17 General Control 16 Register (GCR16)

Address Offset: E0h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**WUI1 Debounce Select (WUI1DS)** Debounce WUI inputs from WUI1. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec
3	-	-	**Reserved**
2-0	R/W	0h	**WUI0 Debounce Select (WUI0DS)** Debounce WUI inputs from WUI0. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.5.3.18 General Control 17 Register (GCR17)

Address Offset: E1h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**WUI3 Debounce Select (WUI3DS)** Debounce WUI inputs from WUI3. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec
3	-	-	**Reserved**
2-0	R/W	0h	**WUI2 Debounce Select (WUI2DS)** Debounce WUI inputs from WUI2. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.5.3.19 General Control 18 Register (GCR18)

Address Offset: E2h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**WUI5 Debounce Select (WUI5DS)** Debounce WUI inputs from WUI5. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec
3	-	-	**Reserved**
2-0	R/W	0h	**PWRSW Debounce Select (PWRSWDS)** Debounce WUI inputs from PWRSW. Only WUIDIE is enabled within GCR14. 0h: Disable 1h: 16ms 2h: 64ms 3h: 1sec 4h: 2sec

7.5.3.20 General Control 19 Register (GCR19)

Address Offset: E4h

Bit	R/W	Default	Description
7	R/W	0b	**GPB5 Input Voltage Selection (GPB5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPB6 Input Voltage Selection (GPB6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	0b	**GPC1 Input Voltage Selection (GPC1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	0b	**GPC2 Input Voltage Selection (GPC2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPC7 Input Voltage Selection (GPC7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPD0 Input Voltage Selection (GPD0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	0b	**GPD1 Input Voltage Selection (GPD1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	0b	**GPD2 Input Voltage Selection (GPD2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.5.3.21 General Control 20 Register (GCR20)

Address Offset: E5h

Bit	R/W	Default	Description
7	R/W	0b	**GPD3 Input Voltage Selection (GPD3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPD4 Input Voltage Selection (GPD4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	0b	**GPE0 Input Voltage Selection (GPE0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	0b	**GPE6 Input Voltage Selection (GPE6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPE7 Input Voltage Selection (GPE7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPF2 Input Voltage Selection (GPF2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	0b	**GPF3 Input Voltage Selection (GPF3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	0b	**GPF4 Input Voltage Selection (GPF4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.5.3.22 General Control 21 Register (GCR21)

Address Offset: E6h

Bit	R/W	Default	Description
7	R/W	0b	**GPF5 Input Voltage Selection (GPF5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
6	R/W	0b	**GPF6 Input Voltage Selection (GPF6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
5	R/W	0b	**GPF7 Input Voltage Selection (GPF7VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
4	R/W	0b	**GPG1 Input Voltage Selection (GPG1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
3	R/W	0b	**GPG6 Input Voltage Selection (GPG6VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPH0 Input Voltage Selection (GPH0VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
1	R/W	0b	**GPH1 Input Voltage Selection (GPH1VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
0	R/W	0b	**GPH2 Input Voltage Selection (GPH2VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

7.5.3.23 General Control 22 Register (GCR22)

Address Offset: E7h

Bit	R/W	Default	Description
7	W	0b	**VCC Power Domain Select (VCCPDS)** 0b: VCC is supplied by 3.3V. 1b: VCC is supplied by 1.8V.
6-4	-	-	**Reserved**
3	R/W	0b	**GPA4 Input Voltage Selection (GPA4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.
2	R/W	0b	**GPA5 Input Voltage Selection (GPA5VS)** 0b: 3.3V. 1b: 1.8V. Do not enable the internal pull-up if this bit is set to one.

Bit	R/W	Default	Description
1	R/W	1b	**GPB3 Input Voltage Selection (GPB3VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.
0	R/W	1b	**GPB4 Input Voltage Selection (GPB4VS)** 0b: 3.3V. 1b: 1.8V. Do not enable internal pull-up if this bit is set to one.

7.5.3.24 General Control 23 Register (GCR23)

Address Offset: E8h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**GPM6 Power Domain Select (GPM6PDS)** 0b: ALERT#/SERIRQ/GPM6 is supplied by VFSPI. 1b: ALERT#/SERIRQ/GPM6 is supplied by VCC.

7.5.3.25 Power Good Watch Control Register (PGWCR)

Address Offset: FFh

Bit	R/W	Default	Description
7	R/W	0b	**Power Good Watch Mode 1 Enable (PGWM1EN)** 1b: Enable Power good watch mode 1. PGWFS is to determine whether to go back or not. 0b: Otherwise.
6	R/WC	0b	**Power Good Watch Flag Status (PGWFS)** This bit will be cleared when a timeout reset event of power good watch occurs. This bit will be cleared when PGWM1EN is cleared.
5-4	-	-	**Reserved**
3	R/W	0b	**PWRSW WDT 2 to Drop Low Enable (PWSW2DLEN)** 1b: A timeout reset event from PWRSW WDT 2 occurs, it will drop power good watch pin to low and delay 1 second before reset EC. 0b: A timeout reset event from PWRSW WDT 2 occurs. it reset EC immediately.
2	R/WC	0b	**PWRSW WDT 2 to Drop Low Flag (PWDT2TDLF)** 0b: Otherwise 1b: This flash indicates a timeout reset event from PWRSW WDT 2 triggers power good watch reset. Write 1 to clear this flag.
1-0	-	-	**Reserved**

7.5.3.26 Port Data Registers A-J,M (GPDRA-J,M)

The Port Data register (GPDR) is an 8-bit register. The pin function is controlled by Port Control Register (GPCRn). When the pin function is set to be a general output pin, the value of the GPDRx bit is directly output to its corresponding pin. When the pin function is set to be a general input pin, the pin level status can be detected by reading the corresponding register bit. Each register contains one group which has eight ports at most.

Address Offset: 01h-0Ah, 0Dh

Bit	R/W	Default	Description
7-0	R/W	GPDRG[0] : 1b Otherwise: 0b	**Port Data Register (GPDRn[7:0])** When the pin function is set to be a general output pin, the value of this bit is directly output to its corresponding pin. In the output mode, reading returns the last written data to GPDRn. In other modes, reading this register returns the pin level status. For group I/J, the return data may have no meaningful in the function 1 mode.

7.5.3.27 Port Data Mirror Registers A-J,M (GPDMRA-J,M)

Address Offset: 61h-6Ah, 6Dh

Bit	R/W	Default	Description
7-0	R	-	**Port Data Mirror Register (GPDMRn[7:0])** Reading this register returns the pin level status. For group I/J, the return data may have no meaningful in the function 1 mode.

7.5.3.28 Port Control n Registers (GPCRn, n = A0-M6)

These registers are used to control the functions of each I/O port pin. Each register is responsible for the settings of one pin in the port.
If Operation Mode is "Alternate Function", Function 1 and/or Function 2/3 will be enabled. Refer to Table 7-9. GPIO Alternate Function on page 263 for details.

Address Offset: Refer to Table 7-9. GPIO Alternate Function

Bit	R/W	Default	Description
7-6	R/W	Refer to Table 7-9 on page 263	**Port Pin Mode (GPMD[1:0])** These bits are used to select the GPIO operation Mode. **GPMD[1:0]** / **Pin Status** / **READ GPDRn** / **WRITE GPDRn** 00b / Alternate Function / Pin Status / GPDR is writable but it has no effects on the pin status. 01b / Output / Pin Status / The value written to GPDR is output to pin. 10b / Input / Pin Status / GPDR is writable but it has no effects on the pin status. 11b / Reserved / - / -
5-3	-	-	**Reserved**
2	R/W	Refer to Table 7-9 on page 263	**Port Pin Pull Up (GPPU)** This bit is used to pull the port. It is always valid regardless of GPMD, input or output. Enable this bit will increase power consumption. Note that if one port is operated in output mode, it should not enable this bit unless its output type is open-drain. For example, clear this bit when DAC0/GPJ0 is switched to alternative function. If GPPU and GPPD are set both 1b, the corresponding port would be configured as tri-state. However, ports GPB0, GPI0-GPI7 and GPJ0-GPJ7 cannot be configured as tri-state.
1	R/W	Refer to Table 7-9 on page 263	**Port Pin Pull Down (GPPD)** This bit is used to pull the port. This bit is always valid regardless of GPMD, input or output. If GPPU and GPPD are both set 1b, the corresponding port would be configured as tri-state. However, ports GPB0, GPI0-GPI7 and GPJ0-GPJ7 cannot be configured as tri-state.
0	R/W	0	**Reserved**

7.5.3.29 Output Type Registers A/B/D/E/F/H/J (GPOT A/B/D/E/F/H/J)

The Output Type register (GPOT) is an 8-bit register. These registers control the output type of GPIO. Each register contains one group which has eight ports at most. Note that these bits are valid only when corresponding GPMD equals to 01 (Output mode).

Other GPIO pin(s) can support open-drain by setting its(their) GPDR register(s) as 0 and switch GPMD field in GPCR register between input and output mode.

Address Offset: 71h, 72h, 74h, 75h, 76h, 78h, 7Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Output Type Register (GPOTn[7:0])** The adjustable output types are only available on port GPA0-3, GPB0-B7, GPD0-D7, GPE0-E7, GPF0-F7, GPH0-H6 and GPJ0-J5. For each bit: 0: Push-pull output 1: Open-drain output

7.5.4 Alternate Function Selection

The following lists function 1 and function 2 of each GPIO port. Notice that the GA20 function can be implemented by GPO or function 1 which is implemented at KBC module. Function 1 of GPB6 is KBRST# from KBC module through SWUC mode. LPCRST# is recommended to input from GPD2 port.

Table 7-9. GPIO Alternate Function

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output (Drive or source/ sink mA)	Sch Trig	Pull Cap	Def Pull	5VT	1.8V in	Def Mode
GPIOA	0	1610h	24	PWM0	GPCRA0[7:6]=00	WUI43	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI
	1	1611h	25	PWM1	GPCRA1[7:6]=00	WUI44	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI
	2	1612h	28	PWM2	GPCRA2[7:6]=00	WUI45	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI
	3	1613h	29	PWM3	GPCRA3[7:6]=00	WUI32	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI
	4	1614h	30	PWM4	GPCRA4[7:6]=00	WUI33	Always	SMCLK5	GPCRA4[7:6]=00 / SMB5EN=1	8	Y	Up/Dn	-	Y	Y	GPI
	5	1615h	31	PWM5	GPCRA5[7:6]=00	WUI34	Always	SMDAT5	GPCRA5[7:6]=00 / SMB5EN=1	8	Y	Up/Dn	-	Y	Y	GPI
	6	1616h	32	PWM6	GPCRA6[7:6]=00	WUI35	Always	SSCK	GPCRA6[7:6]=00 / SPICTRL>0	8	Y	Up/Dn	-	Y	-	GPI
	7	1617h	34	PWM7	GPCRA7[7:6]=00	WUI52	Always	RIG1#	GPCRA7[7:6]=00 / U2CTRL=3	8	Y	Up/Dn	-	Y	-	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output (Drive or source/ sink mA)	Sch Trig	Pull Cap	Def Pull	5VT	1.8V in	Def Mode
GPIOB	0	1618h	108	-	-	WUI53	Always	RXD SIN0	GPCRB0[7:6]=00 GPCRB0[7:6]=00 / U1CTRL>0 / SIN0EN=1	8/16	Y	Up/Dn	-	Y	-	GPI
	1	1619h	109	-	-	WUI54	Always	TXD SOUT0	GPCRB1[7:6]=00 GPCRB1[7:6]=00 / U1CTRL>0 / SOUT0EN=1	8/16	Y	Up/Dn	-	Y	-	GPI
	2	161Ah	123	CTX0	GPCRB2[7:6]=00	WUI36	Always	TMA0	GPCRB2[7:6]=00 TMA0EN = 1	8	Y	Up/Dn	-	-	-	GPI
	3	161Bh	110	SMCLK0	GPCRB3[7:6]=00	WUI55	Always	-	-	4	Y	Up/Dn	-	Y	Y	Func1 1.8V in
	4	161Ch	111	SMDAT0	GPCRB4[7:6]=00	WUI46	Always	-	-	2	Y	Up/Dn	-	Y	Y	Func1 1.8V in
	5	161Dh	126	GA20	GPCRB5[7:6]=00	WUI56	Always	-	-	2	Y	Up/Dn	-	-	Y	GPI
	6	161Eh	4	KBRST#	GPCRB6[7:6]=00	WUI57	Always	-	-	2	Y	Up/Dn	-	-	Y	GPI
	7	161Fh	112	RING# LPCRST#	GPCRB7[7:6]=00 GPCRB7[7:6]=00 /LPCRSTEN=01	WUI58	Always	CK32KOUT	GPCRB7[7:6]=00 / CK32OE=1	8/16	Y	Up/Dn	-	Y	-	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output (Drive or source/ sink mA)	Sch Trig	Pull Cap	Def Pull	5VT	1.8V in	Def Mode
GPIOC	0	1620h	113	CRX0	GPCRC0[7:6]=00	WUI37	Always	-	-	2	Y	Up/Dn	-	Y	-	GPI
	1	1621h	115	SMCLK1	GPCRC1[7:6]=00	WUI59	Always	-	-	4	Y	Up/Dn	-	Y	Y	GPI
	2	1622h	116	SMDAT1	GPCRC2[7:6]=00	WUI47	Always	-	-	4	Y	Up/Dn	-	Y	Y	GPI
	3	1623h	56	KSO16	GPCRC3[7:6]=00	WUI60	Always	SMOSI	GPCRC3[7:6]=00 / SPICTRL>0	8	Y	Up/Dn	-	-	-	GPI
	4	1624h	120	-	-	WUI2	Always	-	-	2	Y	Up/Dn	-	-	-	GPI
	5	1625h	57	KSO17	GPCRC5[7:6]=00	WUI61	Always	SMISO	GPCRC5[7:6]=00 / SPICTRL>0	8	Y	Up/Dn	-	-	-	GPI
	6	1626h	124	-	-	WUI3	Always	-	-	2	Y	Up/Dn	-	-	-	GPI
	7	1627h	16	PWUREQ#	GPCRC7[7:6]=00	WUI38	Always	BBO SMCLK2ALT	GPCRC7[7:6]=00 / HWBPE[2:1]>0 GPCRC7[7:6]=00 / SMCLK2PS=1	8/16	Y	Up/Dn	-	-	Y	GPI
GPIOD	0	1628h	18	RI1#	GPCRD0[7:6]=00	WUI0	Always	-	-	4	Y	Up/Dn	-	-	Y	GPI
	1	1629h	21	RI2#	GPCRD1[7:6]=00	WUI1	Always	-	-	4	Y	Up/Dn	-	Y	Y	GPI
	2	162Ah	22	LPCRST#	LPCRSTEN=10	WUI4	Always	-	-	8	Y	Up/Dn	-	Y	Y	Func1
	3	162Bh	23	ECSCI#	GPCRD3[7:6]=00	WUI62	Always	-	-	8	Y	Up/Dn	-	Y	Y	GPI
	4	162Ch	15	ECSMI#	GPCRD4[7:6]=00	WUI63	Always	PLTRST#	b5@VWCTRL2 = 1	8	Y	Up/Dn	-	-	Y	GPI
	5	162Dh	33	GINT	GPCRD5[7:6]=00	WUI64	Always	CTS0#	GPCRD5[7:6]=00 / U1CTRL>1	8	Y	Up/Dn	-	Y	-	GPI
	6	162Eh	47	TACH0A	GPCRD6[7:6]=00	WUI65	Always	-	-	2	Y	Up/Dn	-	-	-	GPI
	7	162Fh	48	TACH1A	GPCRD7[7:6]=00	WUI39	Always	TMA1	GPCRD7[7:6]=00 TMA1EN = 1	2	Y	Up/Dn	-	-	-	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output (Drive or source/ sink mA)	Sch Trig	Pull Cap	Def Pull	5VT	1.8V in	Def Mode
GPIOE	0	1630h	19	L80HLAT	GPCRE0[7:6]=00	WUI24	Always	BAO SMCLK4	GPCRE0[7:6]=00 / HWBPE[0]=1 GPCRE0[7:6]=00 / SMB4EN=1	8/16	Y	Up/Dn	-	Y	Y	GPI
	1	1631h	82	EGAD	GPCRE1[7:6]=00	WUI25	Always	-	-	8	Y	Up/Dn	-	Y	-	GPI
	2	1632h	83	EGCS#	GPCRE2[7:6]=00	WUI26	Always	-	-	8	Y	Up/Dn	-	Y	-	GPI
	3	1633h	84	EGCLK	GPCRE3[7:6]=00	WUI27	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI
	4	1634h	107	PWRSW	GPCRE4[7:6]=00	WUI66	Always	-	-	2	Y	Up/Dn	-	-	-	GPI
	5	1635h	35	-	-	WUI5	Always	RTS1#	GPCRE5[7:6]=00 / U2CTRL>1	2	Y	Up/Dn	-	Y	-	GPI
	6	1636h	17	LPCPD#	GPCRE6[7:6]=00	WUI6	Always	-	-	2	Y	Up/Dn	-	Y	Y	GPI
	7	1637h	20	L80LLAT	GPCRE7[7:6]=00	WUI7	Always	SMDAT4	GPCRE7[7:6]=00 / SMB4EN=1	8/16	Y	Up/Dn	-	Y	Y	GPI
GPIOF	0	1638h	85	PS2CLK0	GPCRF0[7:6]=00	WUI48	Always	TMB0 CEC	GPCRF0[7:6]=00 / TMB0EN = 1 GPCRF0[7:6]=00 / CECEN = 1	8	Y	Up/Dn	-	Y	-	GPI
	1	1639h	86	PS2DAT0	GPCRF1[7:6]=00	WUI49	Always	TMB1	GPCRF1[7:6]=00 / TMB1EN = 1	8	Y	Up/Dn	-	Y	-	GPI
	2	163Ah	87	PS2CLK1	GPCRF2[7:6]=00	WUI50	Always	DTR0#	GPCRF2[7:6]=00 / U1CTRL>1	8	Y	Up/Dn	-	Y	Y	GPI
	3	163Bh	88	PS2DAT1	GPCRF3[7:6]=00	WUI51	Always	RTS0#	GPCRF3[7:6]=00 / U1CTRL>1	8	Y	Up/Dn	-	Y	Y	GPI
	4	163Ch	89	PS2CLK2	GPCRF4[7:6]=00	WUI20	Always	-	-	8	Y	Up/Dn	-	Y	Y	GPI
	5	163Dh	90	PS2DAT2	GPCRF5[7:6]=00	WUI21	Always	-	-	8	Y	Up/Dn	-	Y	Y	GPI
	6	163Eh	117	SMCLK2	GPCRF6[7:6]=00 / SMCLK2PS=0	WUI22	Always	PECI	GPCRF6[7:6]=00 / PECIE=1	4	Y	Up/Dn	-	-	Y	GPI
	7	163Fh	118	SMDAT2	GPCRF7[7:6]=00	WUI23	Always	PECIRQT#	GPCRF7[7:6]=00 / PECIE=1 / SMCLK2PS=0	4	Y	Up/Dn	-	-	Y	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output (Drive or source/ sink mA)	Sch Trig	Pull Cap	Def Pull	5VT	1.8V in	Def Mode
GPIOG	0	1640h	125	-	-	WUI67	Always	SSCE1#	GPCRG0[7:6]=00 / SPICTRL[0]>0	8	Y	Up/Dn	-	-	-	GPO,H
	1	1641h	122	FDIO2	GPCRG1[7:6]=00 / SPIFR=100b	WUI68	Always	DTR1# SBUSY	GPCRG1[7:6]=00 / U2CTRL>1 GPCRG1[7:6]=00 / SSSPIBP=1	8/16	Y	Up/Dn	Dn	-	Y	GPO,L /ID7
	2	1642h	100	-	-	WUI69	Always	SSCE0#	GPCRG2[7:6]=00 / SPICTRL[0]>0	4	Y	Up/Dn	-	Y	-	GPI
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	6	1646h	119	FDIO3	GPCRG6[7:6]=00 / SPIFR=100b	WUI70	Always	DSR0#	GPCRG6[7:6]=00 / U1CTRL>1	4	Y	Up/Dn	-	-	Y	GPI Don't pull up this.
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
GPIOH	0	1648h	93	CLKRUN#	GPCRH0[7:6]=00	WUI16	Always	-	-	8	Y	Up/Dn	-	Y	Y	GPI/ID0
	1	1649h	94	CRX1	GPCRH1[7:6]=00	WUI17	Always	SIN1 SMCLK3	GPCRH1[7:6]=00 / U2CTRL>0 / SIN1EN=1 GPCRH1[7:6]=00 / SMB3EN=1	8	Y	Up/Dn	-	Y	Y	GPI/ID1
	2	164Ah	95	CTX1	GPCRH2[7:6]=00	WUI18	Always	SOUT1 SMDAT3	GPCRH2[7:6]=00 / U2CTRL>0 / SOUT1EN=1 GPCRH2[7:6]=00 / SMB3EN=1	8	Y	Up/Dn	-	Y	Y	GPI/ID2
	3	164Bh	96	-	-	WUI19	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI/ID3
	4	164Ch	97	-	-	WUI40	Always	-	-	8/16	Y	Up/Dn	-	Y	-	GPI/ID4
	5	164Dh	98	-	-	WUI41	Always	-	-	8	Y	Up/Dn	-	Y	-	GPI/ID5
	6	164Eh	99	-	-	WUI42	Always	-	-	8	Y	Up/Dn	-	Y	-	GPI/ID6
	7	164Fh	3	-	-	WUI79	Always	-	-	2	Y	Up/Dn	-	-	-	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output (Drive or source/ sink mA)	Sch Trig	Pull Cap	Def Pull	5VT	1.8V in	Def Mode
GPIOI	0	1650h	66	ADC0	GPCRI0[7:6]=00	WUI71	Always	-	-	2	Y	-	-	-	-	GPI
	1	1651h	67	ADC1	GPCRI1[7:6]=00	WUI72	Always	-	-	2	Y	-	-	-	-	GPI
	2	1652h	68	ADC2	GPCRI2[7:6]=00	WUI73	Always	-	-	2	Y	-	-	-	-	GPI
	3	1653h	69	ADC3	GPCRI3[7:6]=00	WUI74	Always	-	-	2	Y	-	-	-	-	GPI
	4	1654h	70	ADC4	GPCRI4[7:6]=00	WUI28	Always	-	-	2	Y	-	-	-	-	GPI
	5	1655h	71	ADC5	GPCRI5[7:6]=00	WUI29	Always	DCD1#	GPCRI5[7:6]=00 / U2CTRL>1	2	Y	-	-	-	-	GPI
	6	1656h	72	ADC6	GPCRI6[7:6]=00	WUI30	Always	DSR1#	GPCRI6[7:6]=00 / U2CTRL>1	2	Y	-	-	-	-	GPI
	7	1657h	73	ADC7	GPCRI7[7:6]=00	WUI31	Always	CTS1#	GPCRI7[7:6]=00 / U2CTRL>1	2	Y	-	-	-	-	GPI
GPIOJ	0	1658h	76	-	-	WUI80	Always	TACH2A	GPCRJ0[7:6]=00 / TACH2AEN=1	4	Y	Up/Dn	-	-	-	GPI
	1	1659h	77	-	-	WUI81	Always	TACH2B	GPCRJ1[7:6]=00 / TACH2BEN=1	4	Y	Up/Dn	-	-	-	GPI
	2	165Ah	78	DAC2	GPCRJ2[7:6]=00	WUI82	Always	TACH0B	GPCRJ2[7:6]=00 / TACH0BEN=1	4	Y	Up/Dn	-	-	-	GPI
	3	165Bh	79	DAC3	GPCRJ3[7:6]=00	WUI83	Always	TACH1B	GPCRJ3[7:6]==00 / TACH1BEN=1	4	Y	Up/Dn	-	-	-	GPI
	4	165Ch	80	DAC4	GPCRJ4[7:6]=00	WUI84	Always	DCD0#	GPCRJ4[7:6]=00 / U1CTRL>1	4	Y	Up/Dn	-	-	-	GPI
	5	165Dh	81	DAC5	GPCRJ5[7:6]=00	WUI85	Always	RIG0#	GPCRJ5[7:6]=00 / U1CTRL=3	4	Y	Up/Dn	-	-	-	GPI
	6	165Eh	128	-	-	WUI86	Always	-	-	2	Y	Up/Dn	-	-	-	GPI
	7	165Fh	2	-	-	WUI87	Always	-	-	2	Y	Up/Dn	-	-	-	GPI
GPIOM	0	16A0h	10	LAD0/EIO0	GPCRM0[7:6]=00	-	-	-	-	8	Y	Up/Dn	-	-	-	Func1
	1	16A1h	9	LAD1/EIO1	GPCRM1[7:6]=00	-	-	-	-	8	Y	Up/Dn	-	-	-	Func1
	2	16A2h	8	LAD2/EIO2	GPCRM2[7:6]=00	-	-	-	-	8	Y	Up/Dn	-	-	-	Func1
	3	16A3h	7	LAD3/EIO3	GPCRM3[7:6]=00	-	-	-	-	8	Y	Up/Dn	-	-	-	Func1
	4	16A4h	13	LPCCLK/ESCK	GPCRM4[7:6]=00	-	-	-	-	2	Y	Up/Dn	-	-	-	Func1
	5	16A5h	6	LFRAME#/ECS#	GPCRM5[7:6]=00	-	-	-	-	2	Y	Up/Dn	-	-	-	Func1
	6	16A6h	5	SERIRQ/ALERT#	GPCRM6[7:6]=00	-	-	-	-	8	Y	Up/Dn	-	-	-	Func1
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

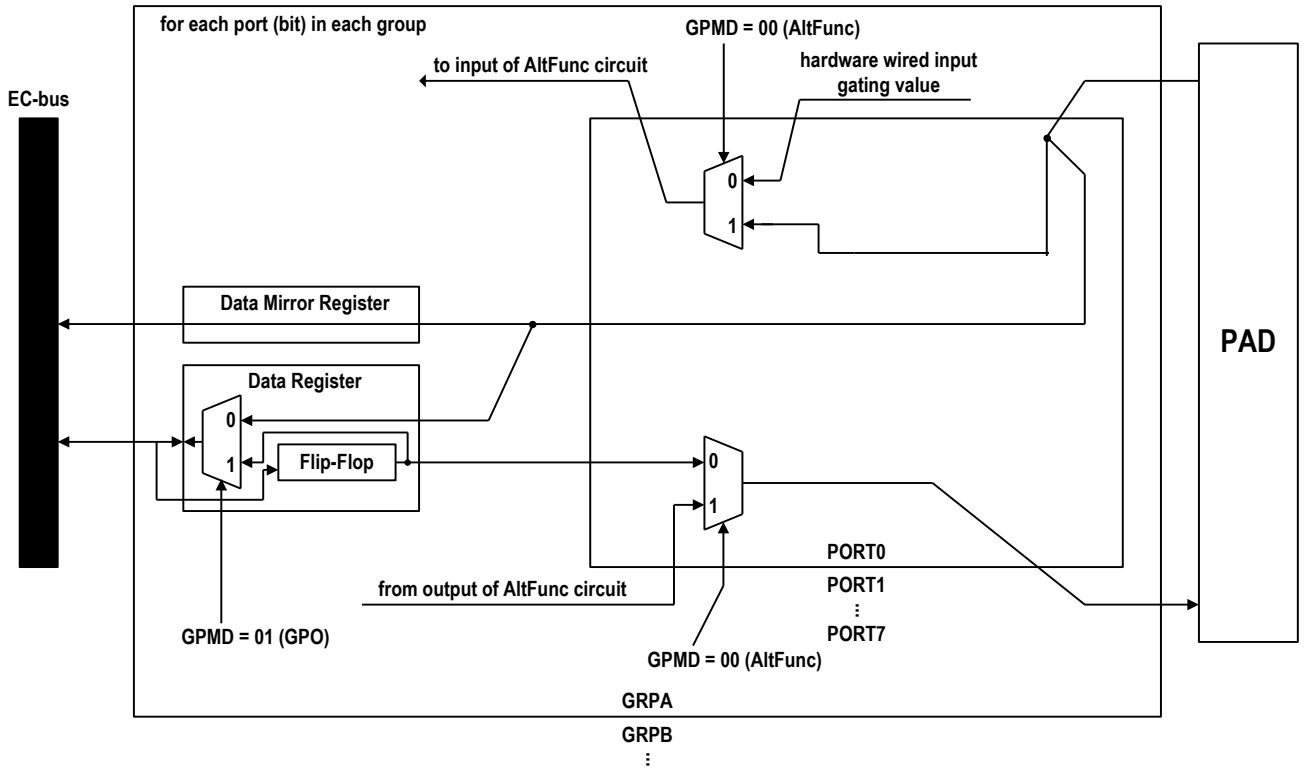
Note: Since all GPIO belong to VSTBY power plane, and there are some special considerations below:

(1) If it is output to external VCC derived power plane circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power plane circuit, this external circuit must consider not floating the GPIO input.
(3) Dash “-“ means this function is not included.

Table 7-10. GPIO with Some Other Function

Pin	Description	Note
GPC7(=BBO)	Hardware bypass: one of the following: GPI6 bypass to GPC7. GPI7 bypass to GPC7.	Refer to Section 7.5.3.5 General Control 4 Register (GCR4), page 247.
GPE0(=BAO)	Hardware bypass: GPI6 bypass to GPE0.	
GPE4	A timeout reset event will be asserted to reset EC after GPE4 has been pulled low for more than 10 seconds. Reset also will output to GPI5.	Refer to Section 7.5.3.10 General Control 9 Register (GCR9), page 250.
In: GPH4, GPI2, GPI3 Out: GPB5-7, GPJ1 GPH0-7, GPE0-7 and GPG1/2/6	Power Good Watch: Basically, it's an extention of the above.	Refer to Section 7.5.3.6 General Control 5 Register (GCR5) , page 248. Refer to Section 7.5.3.7 General Control 6 Register (GCR6) , page 248 . Refer to Section 7.5.3.25 Power Good Watch Control Register (PGWCR), page 259.
In: GPE0, GPI2, GPI3 Out: The same as above	Power Good Watch: It's alternative input of the above.	Refer to Section 7.5.3.6 General Control 5 Register (GCR5) , page 248. Refer to Section 7.5.3.7 General Control 6 Register (GCR6) , page 248. Refer to Section 7.5.3.25 Power Good Watch Control Register (PGWCR), page 259.
GPD0 GPD1 GPC4 GPC6 GPE5 GPE4	Input Debounce circuit Debounce WUI inputs from WUI0, WUI1, WUI2, WUI3, WUI5 and PWRSW.	to Section 7.5.3.15 General Control 14 Register (GCR14) , page 253. Refer to Section 7.5.3.17 General Control 16 Register (GCR16), page 254. Refer to Section 7.5.3.18 General Control 17 Register (GCR17), page 254. Refer to Section 7.5.3.19 General Control 18 Register (GCR18), page 255.

Figure 7-6. GPIO Simplified Diagram



7.5.5 Programming Guide

The firmware should modify LPCRSTEN when it boots up if necessary.

7.6 EC Clock and Power Management Controller (ECPM)

7.6.1 Overview

The EC Clock and Power Management module provide the EC clock control and power management.

7.6.2 Features

- Supports programmable EC clock frequency
- Supported by module power-down mode control
- Supports PLL power-down when CPU enters a Sleep mode

7.6.3 EC Interface Registers

The clock generation and power management registers are listed below. The base address is 1E00h.

Table 7-11. EC View Register Map, ECPM

7 0	Offset
Reserved	00h
Clock Gating Control 1 Register (CGCTRL1R)	01h
Clock Gating Control 2 Register (CGCTRL2R)	02h
Clock Gating Control 3 Register (CGCTRL3R)	05h
PLL Control (PLLCTRL)	03h
Auto Clock Gating (AUTOCG)	04h
PLL Frequency (PLLFREQR)	06h
PLL SSC Control (PLLSSCR)	07h
Clock Gating Control 4 Register (CGCTRL4R)	09h

7.6.3.1 Clock Gating Control 1 Register (CGCTRL1R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	-	-	**Reserved**

7.6.3.2 Clock Gating Control 2 Register (CGCTRL2R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 02h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**EGPC Clock Gating (EXGCG)** 0: Operation 1: Clock to this module is gated
5	R/W	0b	**CIR Clock Gating (CIRCG)** 0: Operation 1: Clock to this module is gated
4	R/W	0b	**SWUC Clock Gating (SWUCCG)** 0: Operation 1: Clock to this module is gated
3-0	-	-	**Reserved**

7.6.3.3 Clock Gating Control 3 Register (CGCTRL3R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 05h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	1b	**Reserved** Always write 1 to this bit.
5-4	-	-	**Reserved**
3	R/W	0b	**PECI Clock Gating (PECICG)** 0: Operation 1: Clocks to PECI module is gated.
2	R/W	0b	**UART Clock Gating (UART12CG)** 0: Operation 1: Clocks to UART1/UART2 modules are gated.
1	R/W	0b	**SSPI Clock Gating (SSPICG)** 0: Operation 1: Clock to this module is gated.
0	R/W	1b	**DBGR Clock Gating (DBGRCG)** 0: Operation 1: Clock to this module is gated.

7.6.3.4 PLL Control (PLLCTRL)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**Deep Doze Mode Control (DDMC)** 0 : PLL will be disabled 1 : PLL will not be disabled (Deep Doze Mode)
0	R/W	1b	**PLL Power Down Control (PPDC)** 0: PLL will not be powered down by software until VSTBY is not supplied. Excuting STANDBY instruction will enter the EC Doze mode. 1: PLL will be powered down after excuting STANDBY instruction and entering an EC power-down mode.

7.6.3.5 Auto Clock Gating (AUTOCG)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 04h

Bit	R/W	Default	Description
7	-	-	**Reserved**

Bit	R/W	Default	Description
6	R/W	1b	**Auto UART1 Clock Gating (AUART1CG)** 1: The UART1 clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides UART12CG bit in CGCTRL3R register. If UART1SD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Doze/Deep Doze/Sleep mode. If UART1SD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The UART1 clock is gated by UART12CG bit in CGCTRL3R register.
5	R/W	1b	**Auto UART2 Clock Gating (AUART2CG)** 1: The UART2 clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides UART12CG bit in CGCTRL3R register. If UART2SD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Doze/Deep Doze/Sleep mode. If UART2SD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The UART2 clock is gated by UART12CG bit in CGCTRL3R register.
4	R/W	1	**Auto SSPI Clock Gating (ASSPICG)** 1: The SSPI clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides SSPICG bit in CGCTRL3R register. If SSPISD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Doze/Deep Doze/Sleep mode. If SSPISD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The SSPI clock is gated by SSPICG bit in CGCTRL3R register.
3	-	-	**Reserved**
2	R/W	0b	**Auto CIR Clock Gating (ACIRCG)** 1: The CIR clock will be automatically gated by channel if the chip is in the Doze/Deep Doze/Sleep mode. It also overrides CIRCG bit in CGCTRL2R register. 0: The CIR clock is gated by CIRCG bit in CGCTRL2R register.
1-0	-	-	**Reserved**

7.6.3.6 PLL Frequency (PLLFREQR)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 06h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0001b	**PLL Frequency (PLLFREQ)** 0001b: Select 18.4MHz as PLL frequency. 0011b: Select 32.3MHz as PLL frequency. 0111b: Select 64.5MHz as PLL frequency. Otherwise: Reserved Read returns the current PLL frequency setting. Writing to this register doesn't change PLL frequency immediately until wakeup from the Sleep mode. SCEMINHW field in FLHCTRL2R register may be required before the PLL frequency is changed.

7.6.3.7 PLL SSC Control (PLLSSCR)

Address Offset: 07h

Bit	R/W	Default	Description
7	W	0b	**Deep-Doze Gating Mode Enable (DDGME)** 0: Disable 1: Enable
6-0	-	-	**Reserved**

7.6.3.8 Clock Gating Control 4 Register (CGCTRL4R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 09h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
0	R/W	1b	**CEC Clock Gating (CECCG)** 0: Operation 1: Clock to this module is gated.

7.7 SMBus Interface (SMB)

7.7.1 Overview

The SMBus interface includes six SMBus designs. The module can maintain bi-directional communication with the external devices through the interface SMCLKn/SMDATn (n denotes 0 to 5) pins. It is compatible with ACCESS BUS and I2C BUS.

7.7.2 Features

- Supports SMBus 2.0
- Supports six SMBus designs
- Performs SMBus messages with packet error checking (PIO PEC) either enabled or disabled; besides, hardwired PEC function supported by masters and slaves as well
- Compatible with I2C cycles
- Supports six masters and three slaves and each one able to be located at SMBus interface 0~5
- Shared FIFO mode or two 32-byte dedicated FIFOs mode for read/write also supported by SMBus master and threshold function supported by master dedicated FIFO mode as well
- Three SMBus slaves on design A, B and C; shared FIFO mode or 16-byte dedicated FIFO mode for read/write supported by slave and threshold function supported by slave dedicated FIFO mode
- Two user-defined Slave addresses for each slave
- Supports Flash DMA to SMB Slave or Master dedicated FIFO
- Supports pre-defined command (dedicated pre-defined slave address) for Slave A and B
- Supports two bridge functions; SMBus module able to bridge signal from Slave A to Master C or from Slave B to Master D
- Independently select SMCLK frequency for each design

7.7.3 Functional Description

The SMBus design A contains one SMBus master and one SMBus slave.
The SMBus design B contains one SMBus master and one SMBus slave.
The SMBus design C contains one SMBus master and one SMBus slave.
The SMBus design D contains one SMBus master.
The SMBus design E contains one SMBus master.
The SMBus design F contains one SMBus master.

The interface of the SMBus master and SMBus slave can be switched to SMCLKn/SMDATn by setting SMBus Design Switch Interface Control Register.

The master supports seven command protocols of the SMBus (see System Management Bus Specification): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, and Block Read/Write. The master also supports the I2C-compatible cycles (see The I2C-Bus Specification). Furthermore, the SMBus master supports the shared FIFO mode or dedicated FIFO mode (32-byte) for the following commands, Block Write, Block Read, I2C-compatible Write, I2C-compatible Read and I2C-compatible Write to Read. For Crystal-Free case, SMBus master hardware will continue to complete the transmission of FIFO data to the slave device after EC enters the sleep mode.

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.
Furthermore, the SMBus slave supports the shared FIFO mode or dedicated FIFO mode (16-byte) for the following commands, Block Write, Block Read, I2C-compatible Write and I2C-compatible Read.

Slave design A and B also support pre-defined command. They support protocols such as I2EC Read/Write, Flash Read and Follow mode command for each SPI instruction.

The SMBus module also supports two bridge functions. The bridge function will bypass Slave design A signal to Master design C or Slave design B signal to Master design D. The data in the bridge mode will be bridged by

byte if it is the slave address; otherwise it will be bridged by bit.

7.7.3.1 SMBus Master Interface

When an interrupt to INTC (INT9, INT10, INT16, INT4, INT160, and INT161 for design A, B, C, D, E, and F respectively) is detected, software can read the Host Status Register to know the interrupt source. There are 5 interrupt conditions: Byte Done, Failed, Bus Error, Device Error, and Finish.

Quick Command:
In the Quick Command, the Transmit Slave Address Register is sent. Software should force the PEC_EN bit in Host Control Register and I2C_EN bit in Host Control 2 Register to 0 when this command is run.

Send Byte/ Receive Byte:
In the Send Byte command, the Transmit Slave Address and Host Command Registers are sent.
In the Receive Byte command, the Transmit Slave Address Register is sent. The received data is stored in the Host DATA 0 register. Software must force the I2C_EN bit in Host control 2 Register to 0 when this command is run.

Write Byte/ Write Word
In the Write Byte command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Registers are sent.
In the Write Word command, the Transmit Slave Address Register, Host Command Register, Host Data 0, and Host Data 1 Registers are sent.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Read Byte/ Read Word
In the Read Byte command, the Transmit Slave Address Register and Host Command Register are sent. Data is received into the Host Data 0 Register.
In the Read Word command, the Transmit Slave Address Register and Host Command Register are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Process Call
In the Process Call command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data1 registers are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register. When the I2C_EN bit in Host Control 2 Register is set to 1, the Host Command Register will not be sent.
Note: The Process Call command with I2C_EN bit set and the PEC_EN bit set produce undefined results.

Block Write/ Block Read
In the Block Write command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 (byte count) register are sent. Data is then sent from the Host Block Data Byte register.
In the Block Read commands, the Transmit Slave Address Register, and Host Command Register are sent. The first byte (byte count) received is stored in the Host Data 0 register, and the remaining bytes are stored in the Host Block Data Byte register.
The Byte Done Status bit in the Host Status Register will be set 1 when the master has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands).
Note: On the block read command, software shall write 1 to LAST BYTE bit in Host Control Register when the next byte will be the last byte to be received.

I2C Block Read
This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent. Bit 0 of the Transmit Slave Address Register has to be 0. The received data is stored in the Host Block Data Byte register.

I2C-compatible Write Command
In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent and the transmitted data is set in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has completed transmission of a byte.

Note: Software shall write 0 to I2C_EN bit in Host Control Register 2 when the cycle is decided to be finished.

I2C-compatible Read Command
In I2C-compatible Read Command, the Transmit Slave Address Register is sent and the received data is stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has received a byte.

Note: Software shall write 1 to LABY bit in the Host Control Register when the next byte to be received is the last one.

I2C-compatible Combined Command
This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in I2C-compatible cycles.
In I2C-compatible Combined Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent. Bit 0 of the Transmit Slave Address Register is set to decide the direction of the cycle and the received data is also stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set 1 when the host has completed transmission of a byte or received a byte.

Note: Software shall control the I2C_SW_EN bit and I2C_SW_WAIT bit in Host Control Register 2 when the direction switch is decided to be performed.

Description of SMBus Master FIFO Mode
SMBus master supports shared FIFO mode, dedicated FIFO mode (32-byte) or dedicated FIFO threshold mode for read/write. For the shared FIFO mode, shared FIFO is mapped into EC external data memory space, whose size is 4k. It includes the following registers, Shared FIFO Function Enable, Master Shared FIFO Size Select, Shared FIFO Base Address and Master FIFO Control. For the dedicated FIFO, it has two 32-byte dedicated FIFOs. It includes the following registers, Master FIFO Control and Master FIFO Status. Besides, the master dedicated FIFO mode supports threshold function as well. It includes Master FIFO Control, Master FIFO Status, Master Dedicated FIFO Threshold, Master Dedicated FIFO Threshold Enable, and Master Dedicated FIFO Threshold Interrupt Status.

Block Write Command (Dedicated FIFO and Shared FIFO Mode)
In the Block Write command, for the dedicated FIFO mode, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers and set Enable SMB design in FIFO Mode bit of Master FIFO Control register). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from FIFO. (Software shall write data to the Host Block Data Byte Register depending on byte count set in Data 0 Register). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

For the shared FIFO mode, it is necessary to set Master FIFO Control and shared FIFO related registers. The Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from the shared FIFO. (Software shall write data to the shared FIFO depending on the byte count set in Data 0 Register). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

Block Read Command (Dedicated FIFO and Shared FIFO Mode)
In the Block Read commands, for the dedicated FIFO mode, the Transmit Slave Address Register and Host

Command Register are sent (Software shall write data to these registers and set Enable SMB design in FIFO Mode bit of Master FIFO Control register). Bit 0 of the Transmit Slave Address Register has to be 1. When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt. Software read the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the received data bytes.

For the shared FIFO mode, it is necessary to set Master FIFO Control and shared FIFO related registers. The Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1. When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt. Software read the data from the Host Data 0 Register to obtain the byte count, and read the data from the shared FIFO to obtain the received data bytes.

If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Master PIO Packet Error Check Register.

I2C-compatible Write Command (Dedicated FIFO, Dedicated FIFO Threshold, Shared FIFO Mode and Non-FIFO To Shared FIFO Mode)

In I2C-compatible Write Command, for the dedicated FIFO mode, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers and set Enable SMB design in FIFO Mode bit of Master FIFO Control register). Bit 0 of the Transmit Slave Address Register has to be 0. When the data in the FIFO have been transmitted, an interrupt will be generated. If byte count is less than 32, Software can read the Host Status Register to know the source of the interrupt(Finish interrupt is 1) or check FIFO Block Done status when this transmission is over 32 data bytes(byte count > 32). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW would transmit the successive bytes from FIFO. When the cycle is completed, a finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

For the dedicated FIFO threshold mode, it is necessary to set Master FIFO Control, MSTDFTH, MDFTHEN registers. The Transmit Slave Address register and Host Block Data Byte register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. When the FIFO byte count is less than the set threshold value, data (length is 32-threshold) in the FIFO have been transmitted, and an dedicated FIFO threshold Tx data available interrupt will be generated. Software writes the data to the Host Block Data Byte register, and writes one to clear the master TX interrupt detected bit in the MDFTISTA register, then HW will transmit the successive bytes from the FIFO. When the cycle is completed, a finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

For the shared FIFO mode, it is necessary to set Master FIFO Control and shared FIFO related registers. The Transmit Slave Address register and shared FIFO data are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. When data in the share FIFO have been transmitted, a finish interrupt will be generated. Software can read the Host Status register to know the source of the interrupt.

To change the non-FIFO mode to the shared FIFO mode, it is necessary to set the shared FIFO related registers first but the Master FIFO control should be disabled. The Transmit Slave Address register and Host Block Data Byte register are sent (Software shall write data to these registers) and the transmitted data are set in the Host Block Data Byte register. The Byte Done Status bit in the Host Status register will be set to 1 when the host has completed transmission of a byte.

Once software wants to enable the FIFO mode when Byte Done Status bit in the Host Status register is set to 1, write one to the FIFO enable bit in the Master FIFO Control register, write one to the SFDFSF bit in the Master FIFO Control register (to start fetch data from Shared FIFO) and write byte count to D0REG and ISFBCH then HW will transmit the successive bytes from the shared FIFO. When all data in the shared FIFO have been transmitted, a finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

I2C-compatible Read Command (Dedicated FIFO, Dedicated FIFO Threshold, Shared FIFO Mode and Non-FIFO To Shared FIFO Mode)

In I2C-compatible Read Command, for the dedicated FIFO mode, the Transmit Slave Address Register is sent (Software shall write data to this register and set Enable SMB design in FIFO Mode bit of Master FIFO Control register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register. When the data have been received to FIFO, an interrupt will be generated. If byte count is less than 32, Software can read the Host Status Register to know the source of the interrupt(finish interrupt is 1). Software can get FIFO data through Host Block Data Byte Register or check FIFO Block Done status when this transmission is over 32 data bytes(byte count > 32). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW would receive the successive bytes into FIFO. When the cycle is completed, a finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

For the dedicated FIFO threshold mode, it is necessary to set Master FIFO Control, MSTDFTH, MDFTHEN registers. The Transmit Slave Address register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address register has to be 1 and the received data byte is stored in the Dedicated FIFO.

When the FIFO byte count is more than the set threshold value, data (length is threshold) in the FIFO have been received, and an dedicated FIFO threshold Rx data available interrupt will be generated. Software read the successive data from the Host Block Data Byte register, and write one to clear the master RX interrupt detected bit in the MDFTISTA register. When the cycle is completed, a finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

For the shared FIFO mode, it is necesasry to set Master FIFO Control and shared FIFO related registers.The Transmit Slave Address Register and Host Command Register are sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1. When the data receive is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt. Software read data from the shared FIFO to get the received data bytes.

To change the non-FIFO mode to the shared FIFO mode, it is necessary to set the shared FIFO related registers first but the Master FIFO control should be disabled. The Transmit Slave Address register is sent and the received data is stored in the Host Block Data Byte register. The Byte Done Status bit in the Host Statusr register will be set to 1 when the host has received a byte .Once software wants to enable the FIFO mode when Byte Done Status bit in the Host Status Register is set to 1, write one to the FIFO enable bit in the Master FIFO Control register, write the byte count to D0REG and ISFBCH then HW will receive the successive bytes to the shared FIFO. When all data have been received in the shared FIFO, a finish interrupt will be generated. Software can read the Host Status register to know the source of the interrupt. Software read data from the shared FIFO to get the received data bytes.

7.7.3.2 SMBus Slave Interface

The slave supports the following three types of messages: Byte Write, Byte Read, and Host Notify.
When an interrupt to INTC (INT9, INT10 and INT16 for design A, B and C respectively) is detected, software can read the Slave Status Register to know the interrupt source. There are 4 interrupt conditions: STOP Condition Detect Status, Slave Timeout Status, Slave Data Status, and Host Notify Status. In the Byte Write/Byte Read command, software must write/read data in the Slave Data Register twice to release the SMCLK line. For the first time, software would set/get data in the Slave Data Register, but the SMCLK line would not be released. The SMCLK line would be held low until software writes/reads data in the Slave Data Register for the second time, after which the SMCLK line would be reelased.

SMBus slave will issue INT81 for the occurrance of Clock Held event.
Here are the steps Software shall follow:

1. Enable the slave stretch clock low bit of HOCTL2 register. SMBus Slave will hold Smbus clock to low after the start bit is received. If the control bit is set, this register required to be set before entering the sleep mode.

2. When INT81 is generated, the software shall check SSSLS bit of SLSTA Register to know which slave side is stretching SMBCLK low.
3. Software can disable slave stretch clock low function to release clock by writing the slave stretch clock low bit to zero.
4. After the above steps, SMBus master side will get bus control and continually send data bit to slave side.

Byte Write
In the byte write command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the Slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time). After the data is read, the third byte (Data) is received and stored in the Slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time).

Byte Read
In the byte read command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the Slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time). After the Repeated Start and Slave Address cycle, the software shall write the data to the Slave Data Register (for the first time) and this register will be sent during the Data Byte Cycle. The SMCLK line will be held low until the data is set in the Slave Data Register for the second time, after which the SMCLK line would be reelased.

Host Notify Command
In the host notify command, the first received byte must be 0001000b. The second received byte is stored in the Notify Device Address Register. The next two bytes are stored in the Notify Data Low Byte Register and Notify Data High Byte Register.

Furthermore, the SMBus slave supports the shared FIFO mode or dedicated FIFO mode (16byte) for the following commands, Block Write, Block Read, I2C-compatible Write and I2C-compatible Read.

7.7.3.3 SMBus Porting Guide

(1).SMBus Master Interface:

The SMBus controller requires that various data and command registers be setup for the message to be sent. When the START bit in the Host Control Register is set, the SMBus controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing of a new command.

The “Timing Registers” (22h~28h, 33h) should be programmed before the transaction starts. In addition, the SMCLK frequency of design A~D can be switched independently to 50 kHz, 100 kHz, or 400 kHz by setting the registers 40h~43h, which means SMCLK timing doesn’t relate to “Timing Register (22h~28h, 33h).” Besides the 25ms Register, all of the other count numbers are based on EC clock. For example, write the 1Bh (37 / FreqEC ~= 4.0us) into the 4.0us register.
(FreqEC is listed in Table 10-2 on page 530 and this example assumes FreqEC = 9.2 MHz.)

The IT5121 SMBus Interface can perform SMBus messages with either packet error checking (PEC) enabled or disabled (PEC_EN bit = 1 or 0 in the Host Control Register). The actual PEC calculation and checking is performed in software.
Here is the steps the software shall follow to program the registers for various command.

1. Quick Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.

(2). In Quick Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register).
(3). Start the transaction (Write 41h to the Host Control Register, which will select the "Quick Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt is generated. Software can read the Host Status Register to know the source of the interrupt.

Note: After reading the Status Register, the software must write 1 to clear it.

2. Send Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Send Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to the Transmit Slave Address Register and Host Command Register) (Host Command Register is used for transmitting data here). Bit 0 of the Transmit Slave Address Register has to be 0.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

3. Receive Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Receive Byte Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Receive Byte Command, the received data is stored in the Host Data 0 Register. Software can read this register to get the data.

4. Write Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Write Byte Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Master PIO Packet Error Check Register and this register will be sent, too.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

5. Write Word Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Write Word Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Master PIO

Packet Error Check Register. And this register will be sent, too.

(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).

(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

6. Read Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.

(2). In Read Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.

(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).

(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

(5). In Read Byte Command, the data received is stored in the Host Data 0 Register. Software can read this register to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Master PIO Packet Error Check Register.

7. Read Word Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.

(2). In Read Word Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.

(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).

(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

(5). In Read Word Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Master PIO Packet Error Check Register.

8. Process Call Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).

(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Process Call Command will skip the command code.

(3). In Process Call Command, the Transmit Slave Address Register, Host Command Register (if I2C_EN = 0), Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.

(4). Start the transaction (Write 51h to the Host Control Register, which will select the "Process Call Command", enable the interrupts, and start the transaction).

(5). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

(6). In Process Call Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Master PIO Packet Error Check Register.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

9. Block Write Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
(3). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from the Host Block Data Byte Register (Software shall write data to this register).
(4). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(5). When the data in Host Block Data Byte Register is sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software writes the data to the Host Block Data Byte Register, then the data is sent from this register by SMBus logic.
(7). Repeat step (5) and (6) for the other data byte until all of the data were sent.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Master PIO Packet Error Check Register and this register will be sent, too.
(8). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

10. Block Read Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(4). When the byte count and the first byte data are received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software read the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the first data byte.
(6). When the next data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software read the data from the Host Block Data Byte Register to get the data.
(8). Repeat step (6) and (7) until the last byte.
(9). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(10). Get an interrupt and receive the last byte.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Master PIO Packet Error Check Register.

11. I2C Block Read Command

This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(3). Start the transaction (Write 59h to the Host Control Register, which will select the "I2C Block Read Command", enable the interrupts, and start the transaction).

(4). When the data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software can read the data from the Host Block Data Byte Register to get the data.
(6). Repeat step (4) and (5) until the last byte.
(7). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(8). Get an interrupt and receive the last byte.

12. I2C-compatible Write Command

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(4). Start the transaction (Write 5Dh to the Host Control Register, which will select the “Extend Command”, enable the interrupts, and start the transaction).
(5). When the data in the Host Block Data Byte Register has been transmitted, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is transmitted from this register by the SMBus logic.
(7). Repeat step (5) and (6) for the other data bytes until software wants to finish the cycle.
(8). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
(9). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

13. I2C-compatible Read Command

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). In I2C-compatible Read Command, the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register.
(4). Start the transaction (Write 5Dh to the Host Control Register, which will select the “Extend Command”, enable the interrupts, and start the transaction).
(5). When the data has been received from the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
(7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
(8). Set the LABY bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
(9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

14. I2C-compatible Combined Command

This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in the I2C-compatible cycles.

From I2C Write Command to I2C Read Command:

(1). In the I2C Write Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Read Command.
(2). After the last transmitted data byte has been sent in the I2C Write Command, the Byte Done interrupt will be generated. Then, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Read Command.
(3). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(4). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Read Command.
(5). When the data has been received and stored in the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
(7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
(8). Set the LABY bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
(9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

From I2C Read Command to I2C Write Command:
(1). In the I2C Read Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Write Command.
(2). In the I2C Read Command, after setting the LABY bit in the Host Control Register, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Write Command.
(3). Get the Byte Done interrupt of the last byte, and receive the last byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(4). Software writes the transmitted data byte in the Host Block Data Byte Register.
(5). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Write Command.
(6). When the data in the Host Block Data Byte Register has been sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is sent from this register by the SMBus logic.
(8). Repeat step (6) and (7) for the other data bytes until software wants to finish the cycle.
(9). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
(10). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

15. Block Write Command (Dedicated FIFO Mode)

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Enable SMBus Dedicated FIFO Mode.
(3). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
(4). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from FIFO. (Software shall write data to the Host Block Data Byte Register depending on byte count set in Data 0 Register).
(5). Start the transaction (Write 55h to the Host Control Register, which will select the “Block Read/Block Write Command”, enable the interrupts, and start the transaction).
(6). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

16. Block Read Command (Dedicated FIFO Mode)

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). Enable SMBus Dedicated FIFO Mode
(3). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(4). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(5). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(6). Software reads the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the received data bytes. If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Master PIO Packet Error Check Register.

17. I2C-compatible Write Command (Dedicated FIFO Mode)

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). Enable SMBus Dedicated FIFO Mode.
(4). Write byte count value to Data 0 register to indicate HW how many bytes will (should) be transmitted.
(5). In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(6). Write data bytes to FIFO through Host Block Data Byte Register.
(7). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(8). When the data in the FIFO have been transmitted, an interrupt will be generated. If the byte count is less than 32, Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).
(9). Or check FIFO Block Done status when this transmission is over 32 data bytes (byte count > 32).
(10). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Block Done Status bit in the FIFO Control Register, then HW will transmit the successive bytes from FIFO.
(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1). If this cycle is not completed yet, go to step (9) again.

18. I2C-compatible Read Command (Dedicated FIFO Mode)

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). Enable SMBus Dedicated FIFO Mode.
(4). Write byte count value to Data 0 register to indicate HW how many bytes will (should) be received.
(5). In I2C-compatible Read Command, the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register.
(6). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(7). When the data have been received to FIFO, an interrupt will be generated. If byte count is less than 32, Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).
(8). Software can get FIFO data through Host Block Data Byte Register.
(9). Or check FIFO Block Done status when this transmission is over 32 data bytes (byte count > 32).
(10). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Block Done

Status bit in the FIFO Control Register, then HW will receive the successive bytes into FIFO.

(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1). If this cycle is not completed yet, go to step (9) again.

(2).SMBus Slave Interface:

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.
Here are the steps the software shall follow to program the registers for various commands.

1. Byte Write

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.
(4). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
(5). Software can read the data from the Slave Data Register for the first time. (This data byte is the command code.) The SMCLK line would be held low until software reads the data for the second time.
(6). When the next interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
(7). Software can read the data from the Slave Data Register for the first time. (This data byte is the Data Byte in SMBus Protocol.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be reelased.

2. Byte Read

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.
(4). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Read Command).
(5). Software can read the data from the Slave Data Register for the first time. (This data byte is the command code.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be reelased.
(6). When the next interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 0Ah for Byte Read Command).
(7). Software can write the data to the Slave Data Register for the first time. (This data will be sent to the external device.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be reelased.

3. Host Notify Command

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 01h for Host Notify Command).
(4). Software can read the data from the Notify Device Address Register, Notify Data Low Byte Register, and Notify Data High Byte Register.

Furthermore, Slave design A,B,C also support the shared FIFO or dedicaed FIFO mode (16-byte) for the following commands, Block Write, Block Read, I2C-compatible Write and I2C-compatible Read. The slave dedicated FIFO also supports threshold function. Threshold function lets software process part of FIFO data

before FIFO becomes empty and it can improve the transmission performance of the bus.

For the dedicated FIFO mode, software needs to enable the slave dedicated FIFO mode (Write 01h to Slave Dedicated FIFO pre-defined Control Register (SADFPCTL, SBDFPCTL or SCDFFCTL Register). If the master wants to write any data to the slave, once the data have been received to the slave dedicated FIFO, an interrupt will be generated and the software can read the Slave Status register to know the source of the interrupt as well as read the Slave FIFO status register to know the length of the FIFO byte count. Software can read data from the Slave Data register continuously according to the byte count. When the cycle is completed, a stop interrupt will be generated. Software can read the Slave Status Register to know the source of the interrupt and clear it.If the master wants to read any data from the slave, the slave side interrupt is generated and the software can read the Slave Status Register to know the source of the interrupt as well as write data to the Slave Data Register continuously. When the cycle is completed, a stop interrupt will be generated. Software can read the Slave Status Register to know the source of the interrupt and clear it.

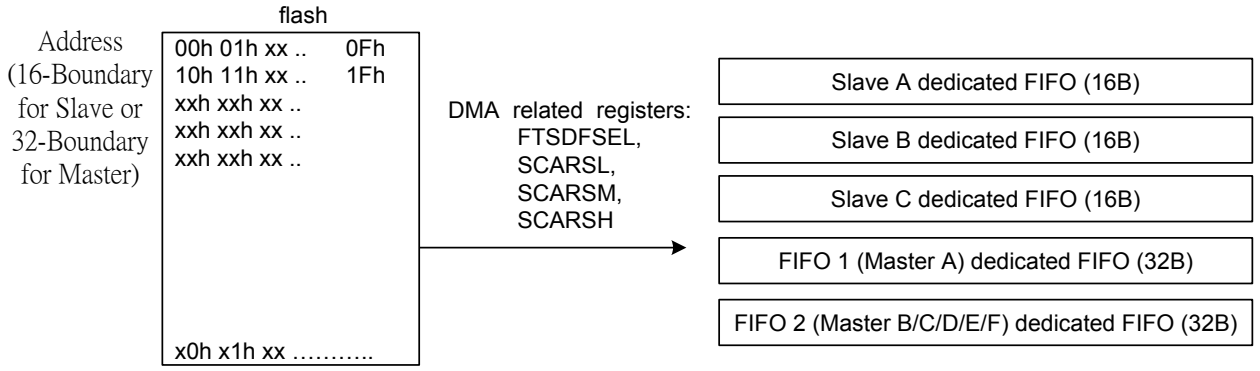
For the dedicated FIFO threshold mode, software needs to set SLVDFTH and SDFTHEN registers. If the master wants to write any data to the slave when the slave FIFO byte count is more than the set threshold value, data (length is threshold) in the slave FIFO have been received, and an slave dedicated FIFO threshold Rx data available interrupt will be generated. If the master wants to read any data from the slave when the slave FIFO byte count is less than the set threshold value, data (length is 16-threshold) in the slave FIFO have been transmitted, and an slave dedicated FIFO threshold Tx data available interrupt will be generated.
Note: For the dedicated FIFO mode and dedicated FIFO threshold mode, the Slave Data register stores the data received from the external master. When this register is served, software must write/read data stored in this register once to release the SCL line.

For the shared FIFO mode, software needs to set the Shared FIFO Base Address For Slave and Slave Shared FIFO Size Select registers and enable the shared FIFO bit of SFFE register. If the master wants to write any data to the slave, once the data have been received to the slave shared FIFO, a stop interrupt will be generated. Software can read data from the slave shared FIFO to get the received data bytes and clear this interrupt.
If the master wants to read any data from the slave, software needs to write data to the slave shared FIFO first. Once the data have been transmitted from the slave shared FIFO, a stop interrupt will be generated. Software can read the Slave Status register to know the source of the interrupt and clear it.

(3).DMA From Flash To SMB Slave Dedicated FIFO

DMA is used as shadow flash content of the Scratch SRAM SMBus address to SMBus Slave or Master dedicated FIFO. For Slave dedicated FIFO, the transmission unit of DMA is 16 bytes at a time, and will align 16-byte boundary. The source inside the flash must be located on 16-boundary. For Master dedicated FIFO, the transmission unit of DMA is 32 bytes at a time, and the source inside the flash must be located on 32-boundary. DMA related registers are DFTSDFSEL, SCARSL, SCARSM, and SCARSH.

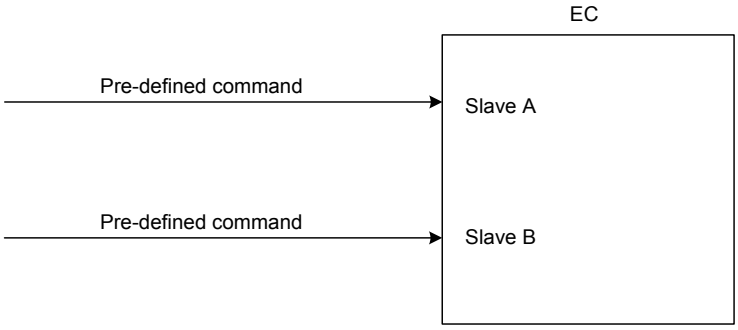
Figure 7-7. DMA from Flash to SMB Dedicated FIFO



(4). Pre-defined Command:

The slave design A, B also support the pre-defined command. Whether function is enabled or not is controlled by writing 1 to the HSAPE bit and HSAPFME bit of the SADFPCTL register as well as the HSBPE and HSBPFME bit of the SBDFPCTL register. The dedicated pre-defined slave address is 5Bh. Here are supported protocols.

Figure 7-8. Pre-defined command



1. Reset through I2C:

Reset

S	5bh	W	A	5ah	A	a5h	A	P

Assert reset to EC.

2. I2EC through I2C:

I2EC Address Write

S	5bh	W	A	10h	A	EC Address[15:8]	A	EC Address[7:0]	A	P

I2EC Address Read

S	5bh	W	A	10h	A	S	5bh	R	A	EC Address[15:8]	A	EC Address[7:0]	A	P

I2EC Data Write

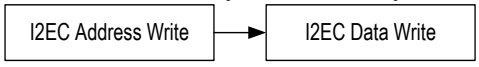
S	5bh	W	A	11h	A	EC Data[7:0]	A	P

I2EC Data Read

S	5bh	W	A	11h	A	S	5bh	R	A	EC Data[7:0]	A	P

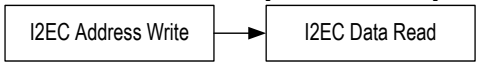
(1). I2EC Write:

- Specify the targeted address of EC memory through “I2EC Address Write”.
- Write EC memory addressed by the targeted address through “I2EC Data Write”.



(2). I2EC Read:

- Specify the targeted address of EC memory through “I2EC Address Write”.
- Read EC memory addressed by the targeted address through “I2EC Data Read”.



3. IO Read through I2C:

IO Address Write

S	5bh	W	A	12h	A	IO Address[15:8]	A	IO Address[7:0]	A	P

IO Address Read

S	5bh	W	A	12h	A	S	5bh	R	A	IO Address[15:8]	A	IO Address[7:0]	A	P

IO Data Write

S	5bh	W	A	13h	A	IO Data[7:0]	A	P

IO Data Read

S	5bh	W	A	13h	A	S	5bh	R	A	IO Data[7:0]	A	P

(1). IO Write:

IO Address Write → IO Data Write

(2). IO Read:

IO Address Write → IO Data Read

4. Flash Read through I2C:

Flash Address Write

S	5bh	W	A	14h	A	Flash Address[23:16]	A	Flash Address[15:8]	A	Flash Address[7:0]	A	P

Flash Address Read

S	5bh	W	A	14h	A	S	5bh	R	A	Flash Address[23:16]	A	Flash Address[15:8]	A	Flash Address[7:0]	A	P

Flash Data Read

S	5bh	W	A	15h	A	S	5bh	R	A	Flash Data[7:0]	A	P

Flash Data Read (auto increase address)

S	5bh	W	A	16h	A	S	5bh	R	A	Flash Data[7:0]	A	Flash Data[7:0]	A	.....	P
										(Flash Address)		(Flash Address + 1)			

(1). Flash Read:

- Specify the targeted address of Flash memory through “Flash Address Write”.
- Read Flash memory addressed by the targeted address through “Flash Data Read”.

Flash Address Write → Flash Data Read

5. Follow Mode for SPI Bus through I2C:

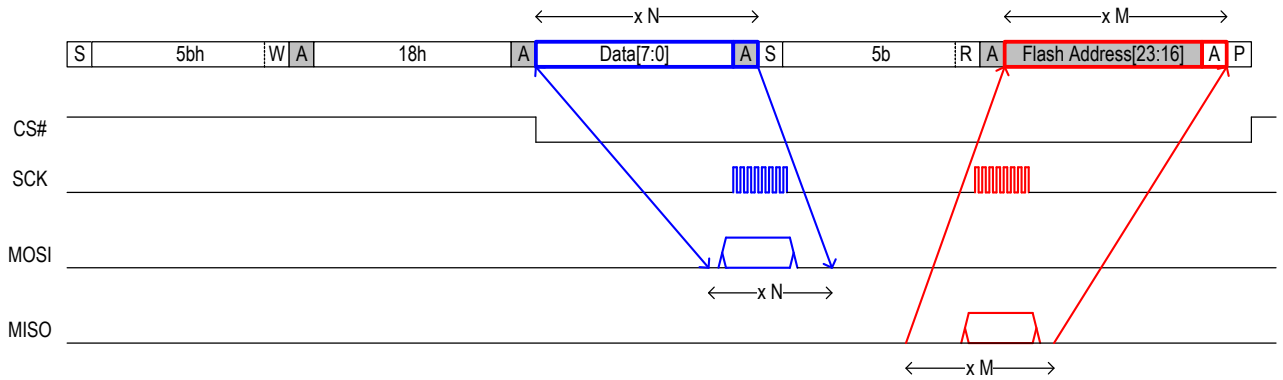
Set CS# of SPI Bus High

S	5bh	W	A	17h	P

Transfer Write/Read Cycle to SPI Bus

S	5bh	W	A	18h	A	Data[7:0]	A	S	5b	R	A	Flash Address[23:16]	A	P
						←x N→						←x M→		

(1). Always execute “Set CS# of SPI Bus high” first.
(2). Use “Transfer Write/Read Cycle to SPI Bus” to generate the SPI cycle.



6. Fast AAIW:

(1). Use "Follow Mode for SPI Bus through I2C" to construct the AAIW cycle with addresses. That is

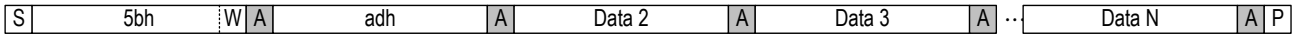
a. Let CS# of SPI Bus high
b. Write adh
c. Write address[23:16]
d. Write address[15:8]
e. Write address[7:0]
f. Write Data 0
g. Write Data 1
h. Let CS# of SPI Bus high

(2). Use "Follow Mode for SPI Bus through I2C" to construct the RDSR cycle. That is

a. Let CS# of SPI Bus high
b. Write 05h
c. Polling status until flash returns non-busy
d. Let CS# of SPI Bus high

(3). Use "Fast data-insertion for AAIW" to write the remaining data.

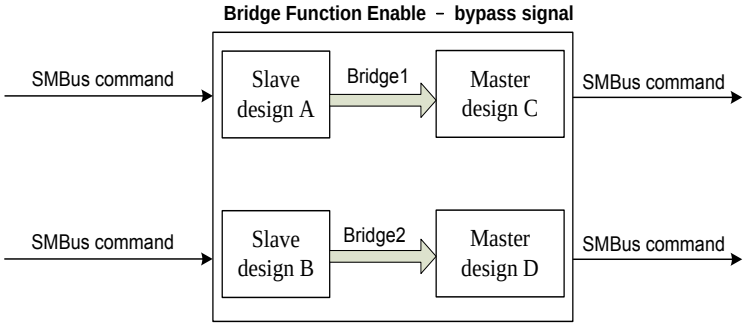
Fast data-insertion for AAIW



(5).Bridge Function

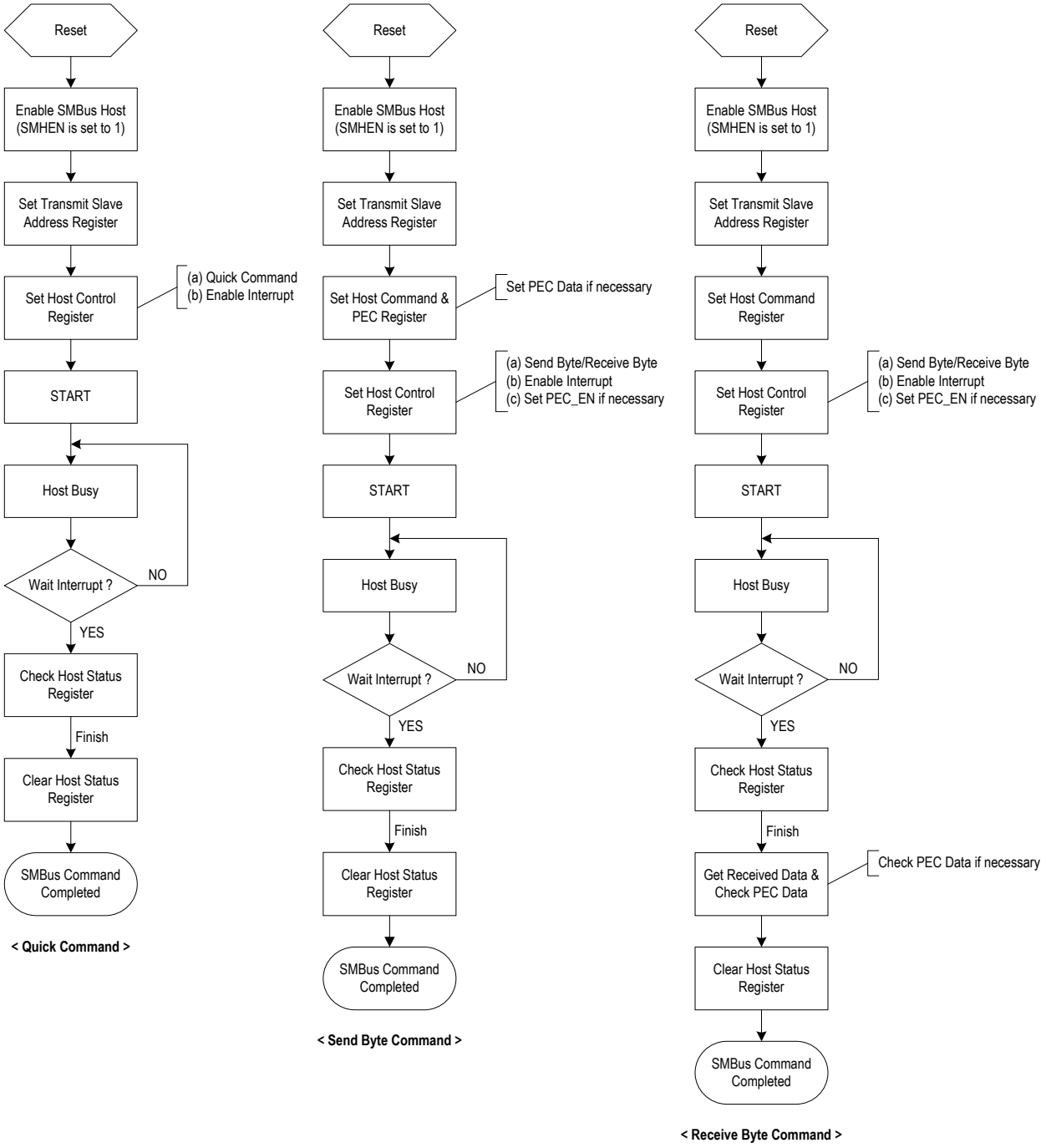
The SMBus module also supports two bridge functions. Whether function is enabled or not is controlled by writing 1 to SABF bit or SBBF bit of SLVBCR register. Write 1 to SMHEN bit of HOCTL2_C to enable Master design C and write 1 to SLVEN bit of HOCTL2_A to enable Slave design A or write 1 to SMHEN bit of HOCTL2_D to enable Master design D and write 1 to SLVEN bit of HOCTL2_B to enable Slave design B. Besides, set SCLKS of SCLKTS_C or SCLKTS_D to select the SMCLK rate for design C or design D. The bridge function will bypass Slave design A signal to Master design C or Slave design B signal to Master design D. The data in the bridge mode will be bridged by byte if it is the slave address; otherwise it will be bridged by bit.

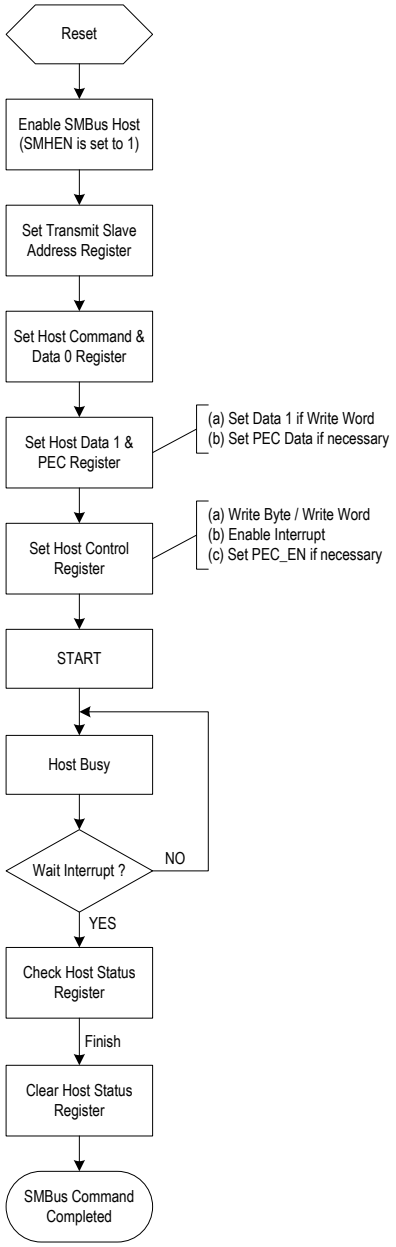
Figure 7-9 Diagram of SMBus Bridge Bypass Function



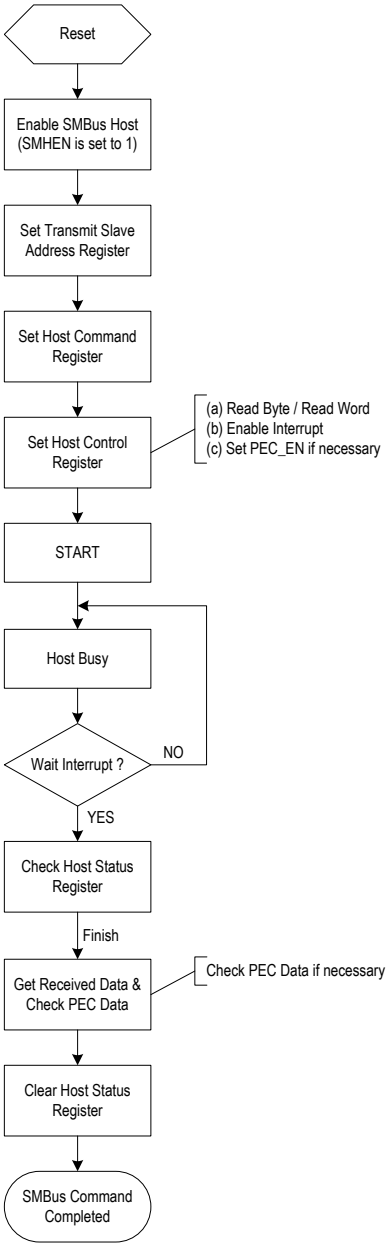
7.7.3.4 SMBus Master Programming Guide

Figure 7-10. Program Flow Chart of SMBus Master Interface

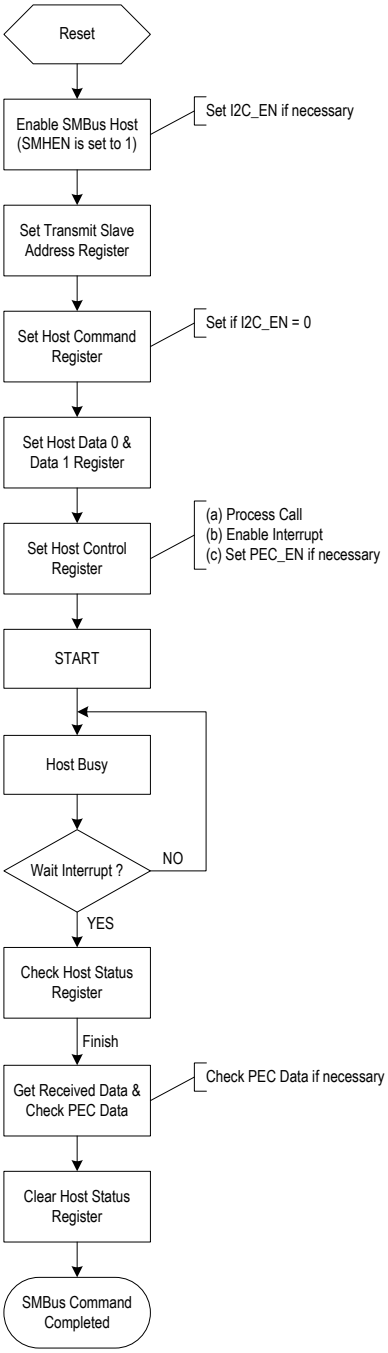




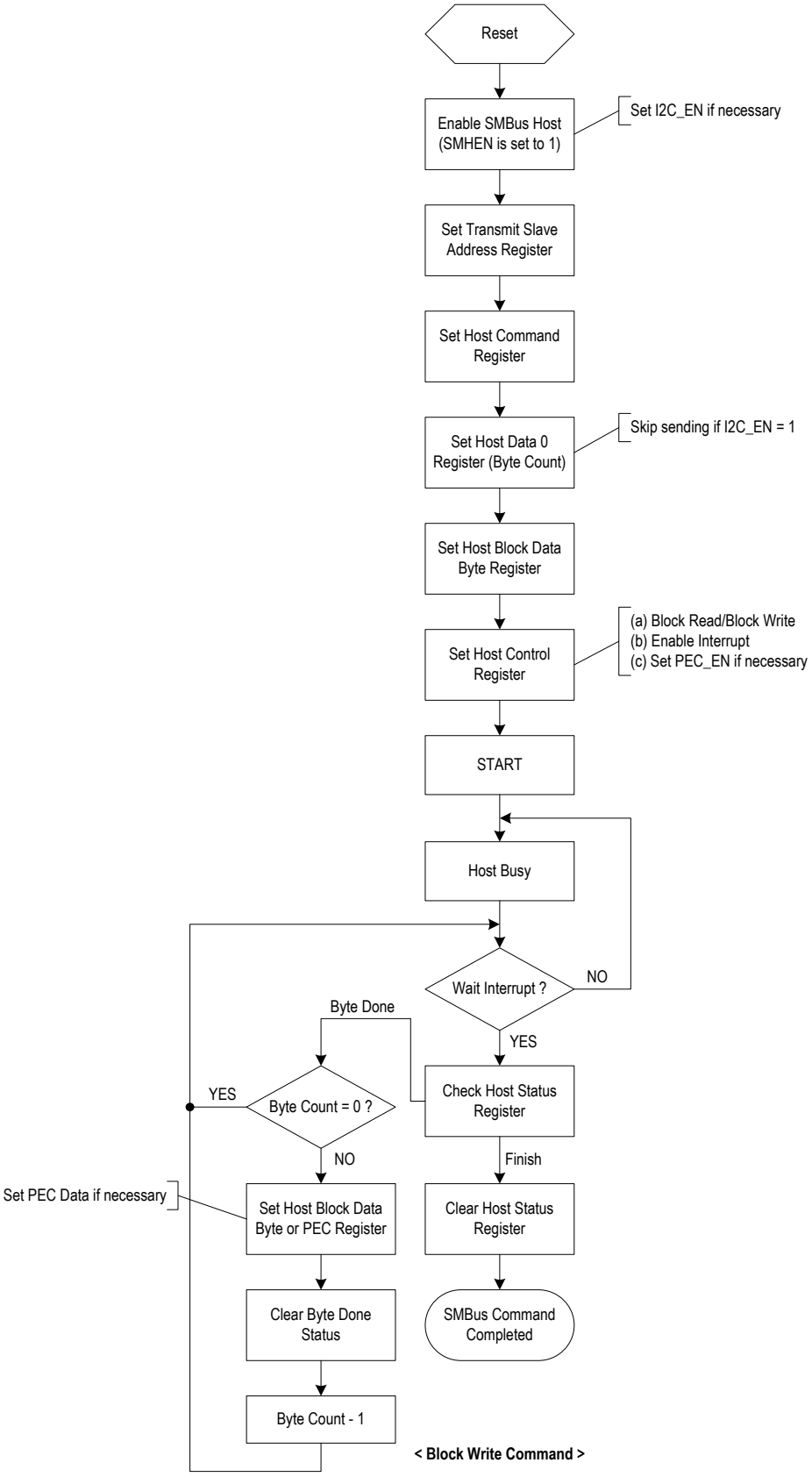
< Write Byte / Word Command >



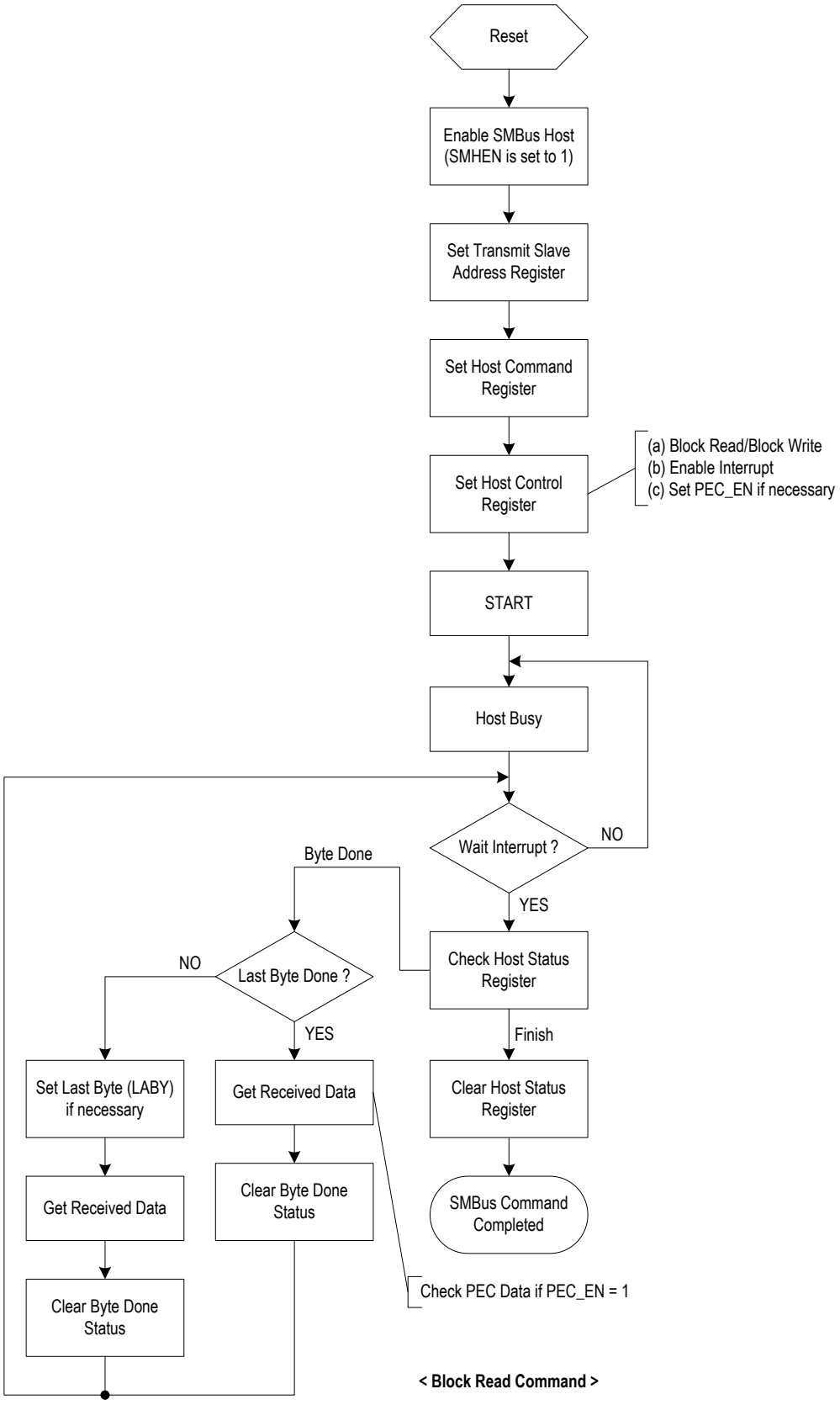
< Read Byte / Word Command >



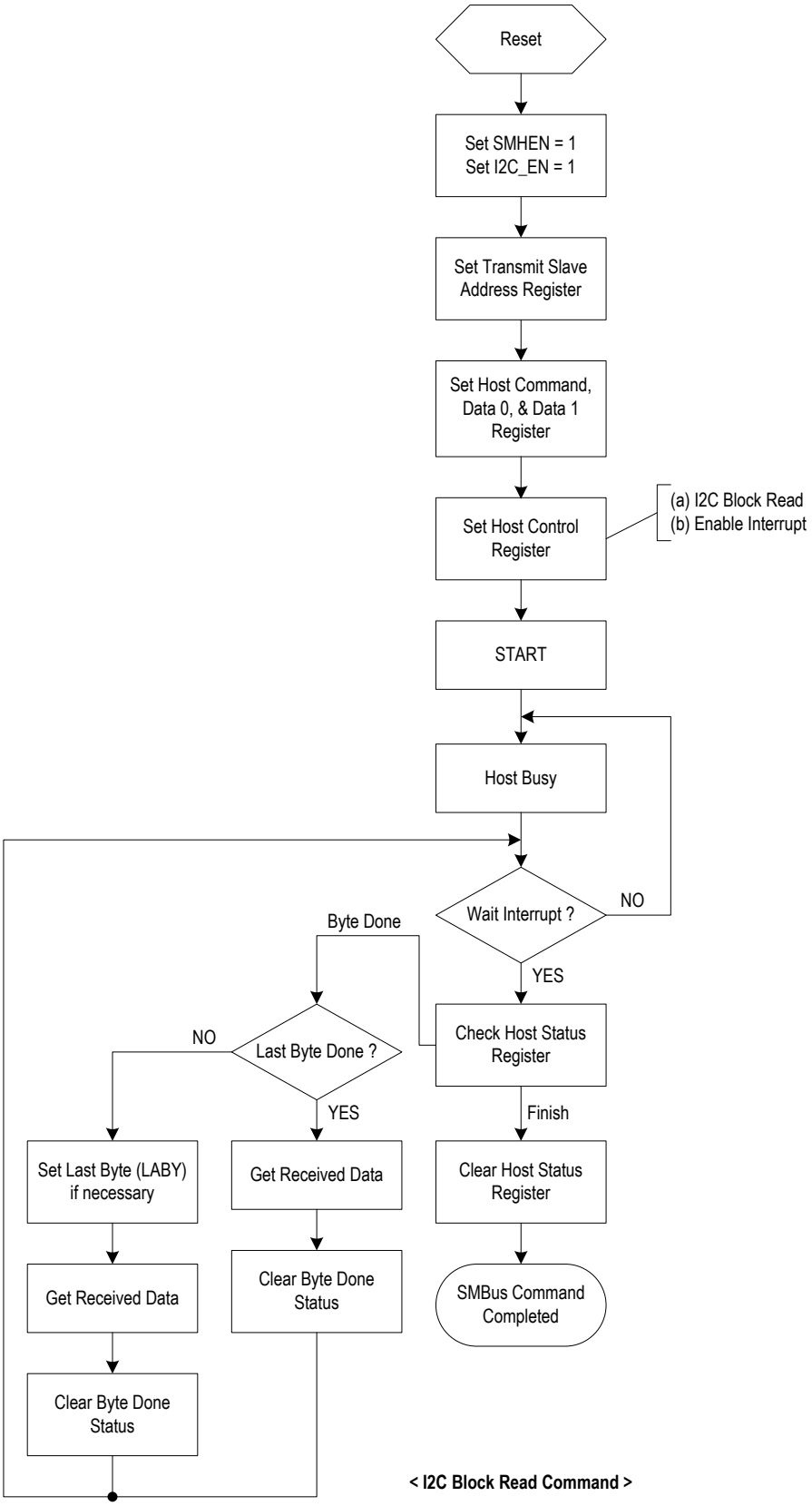
< Process Call Command >



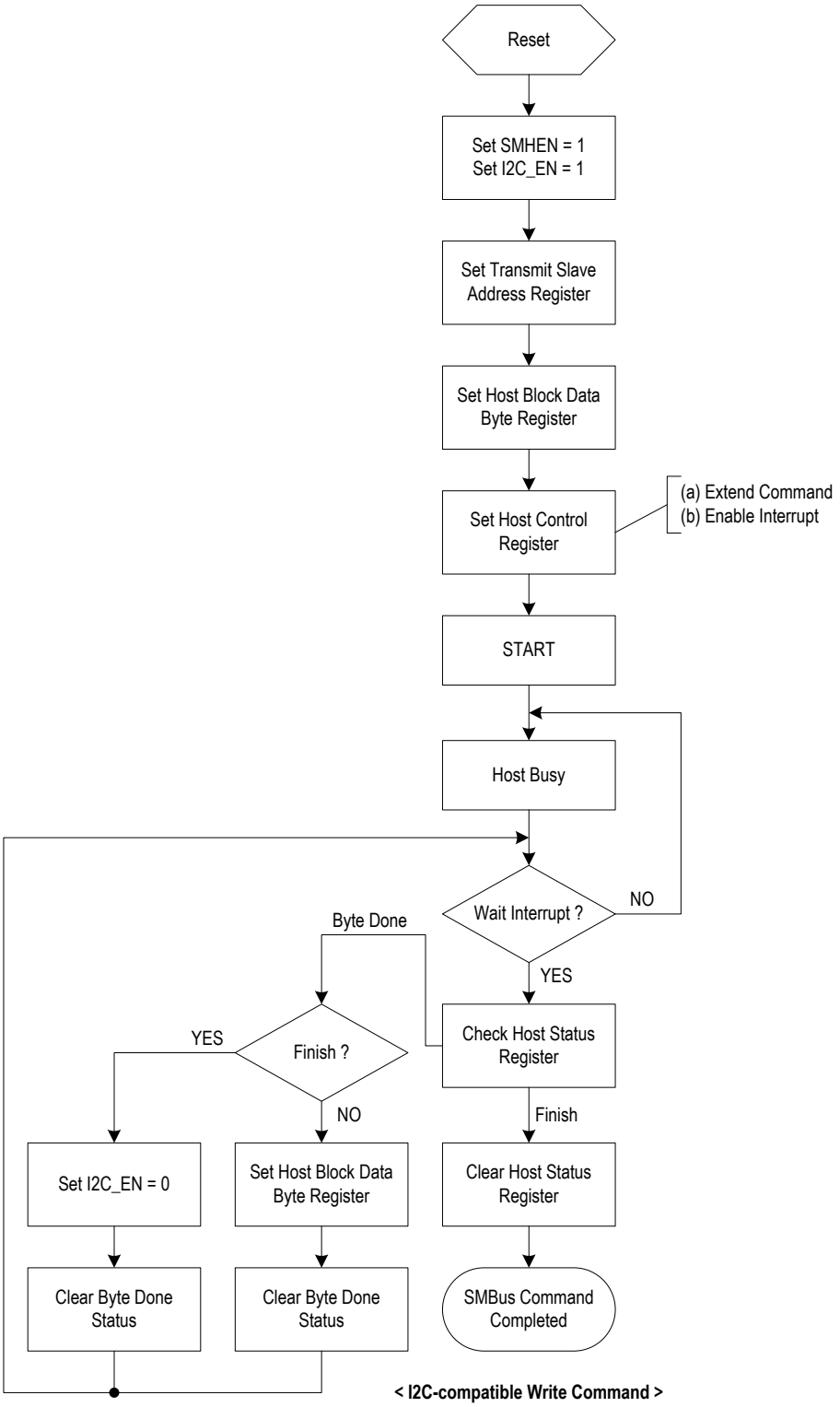
< Block Write Command >



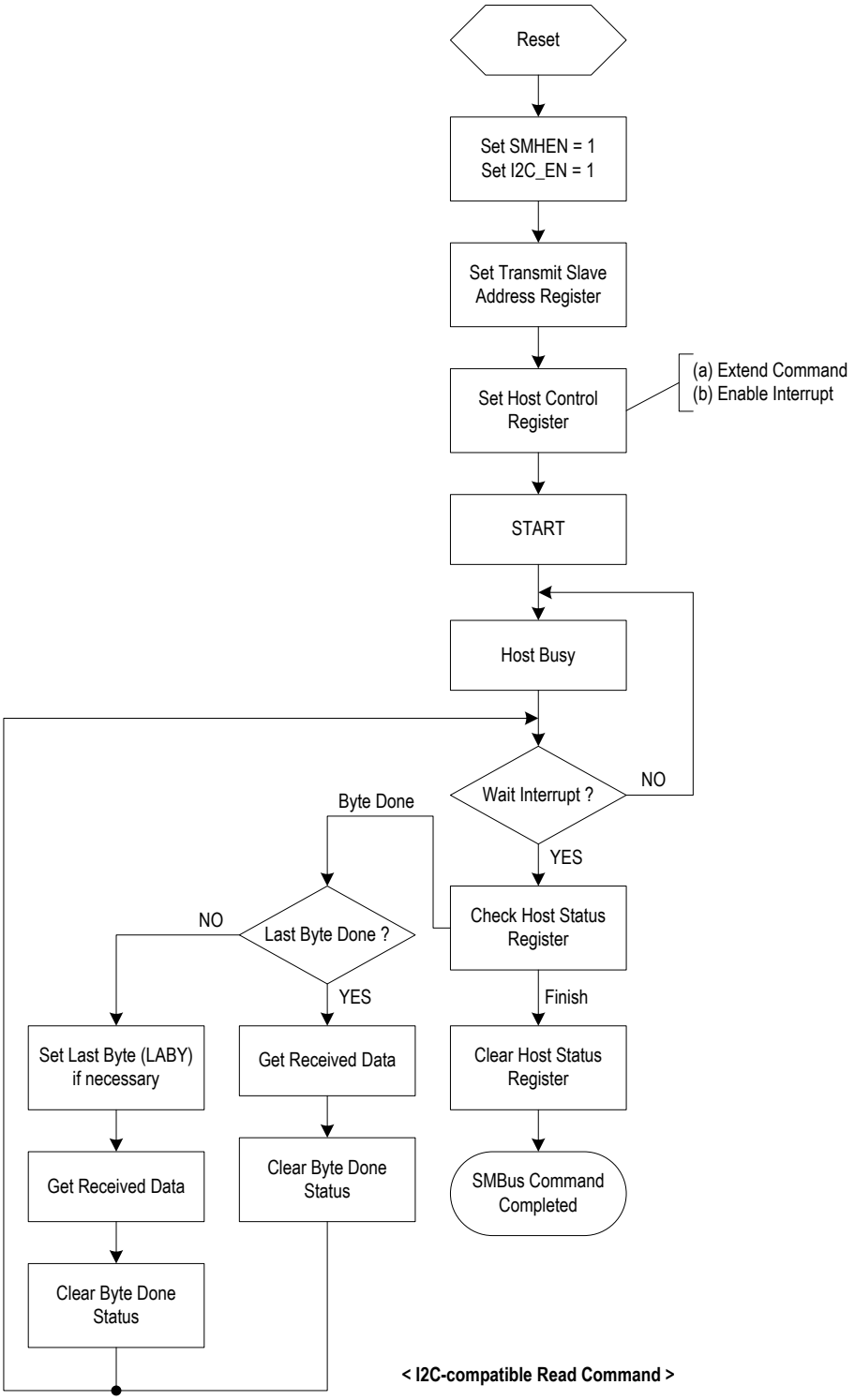
< Block Read Command >



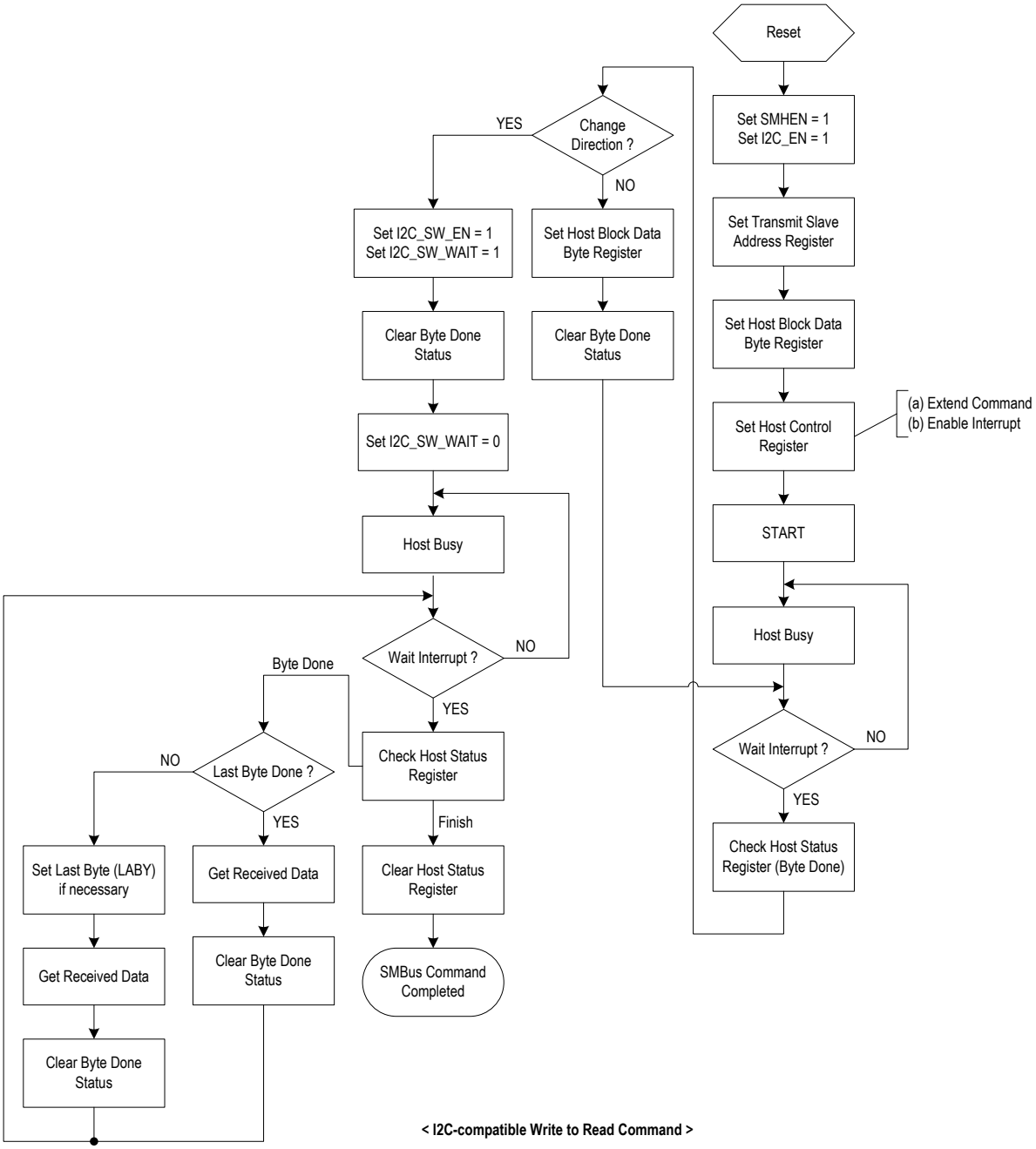
< I2C Block Read Command >



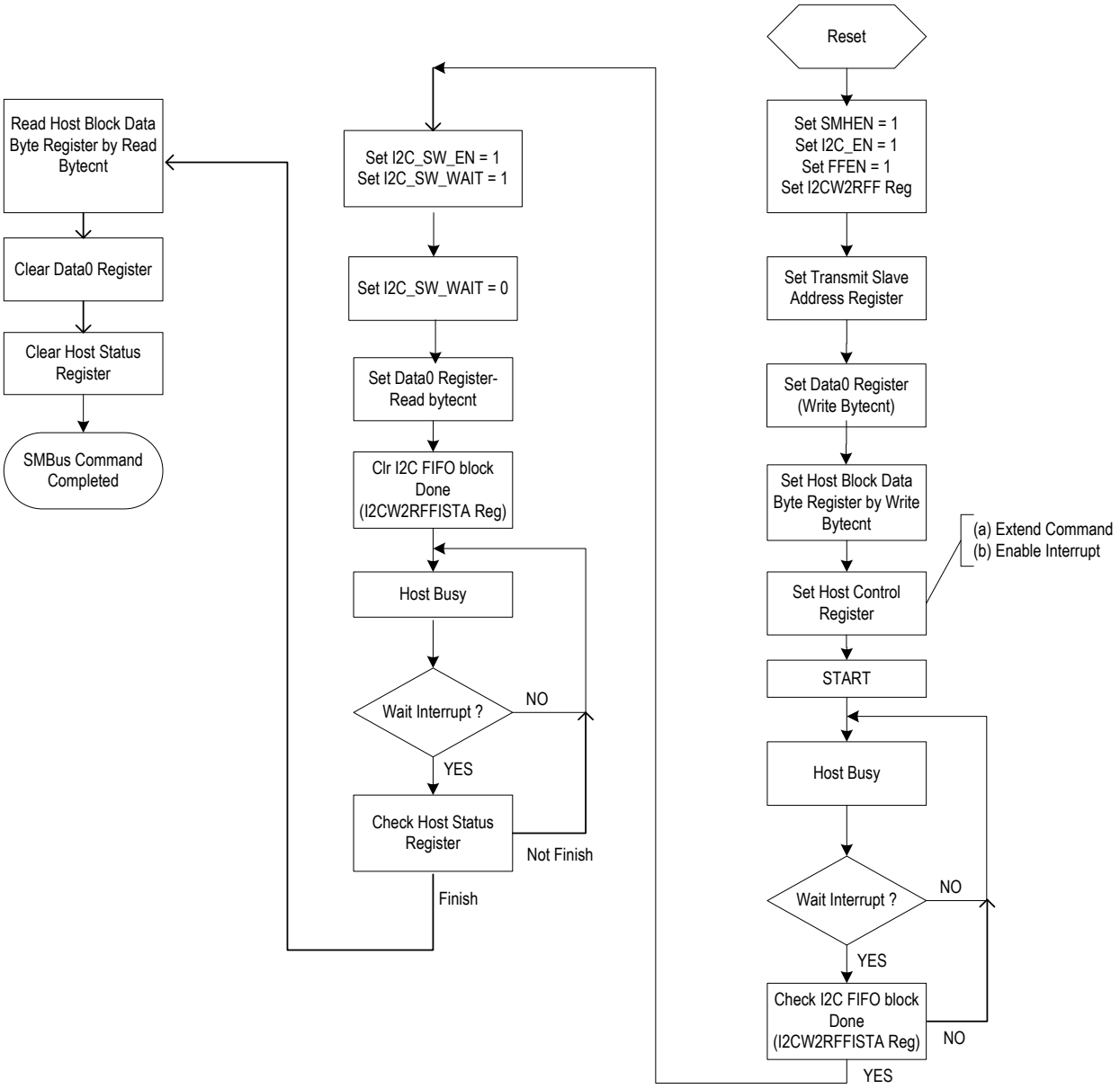
< I2C-compatible Write Command >



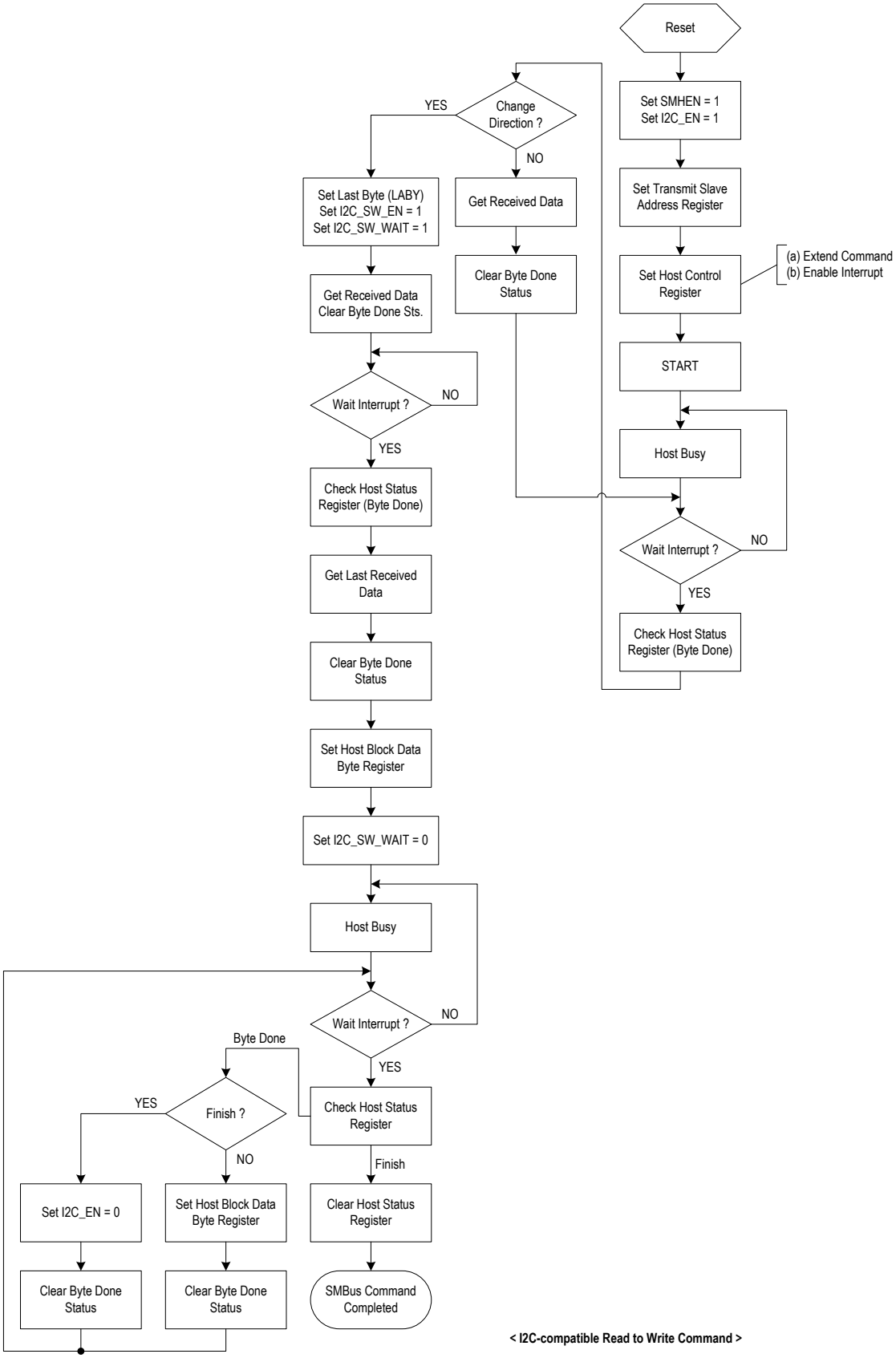
< I2C-compatible Read Command >



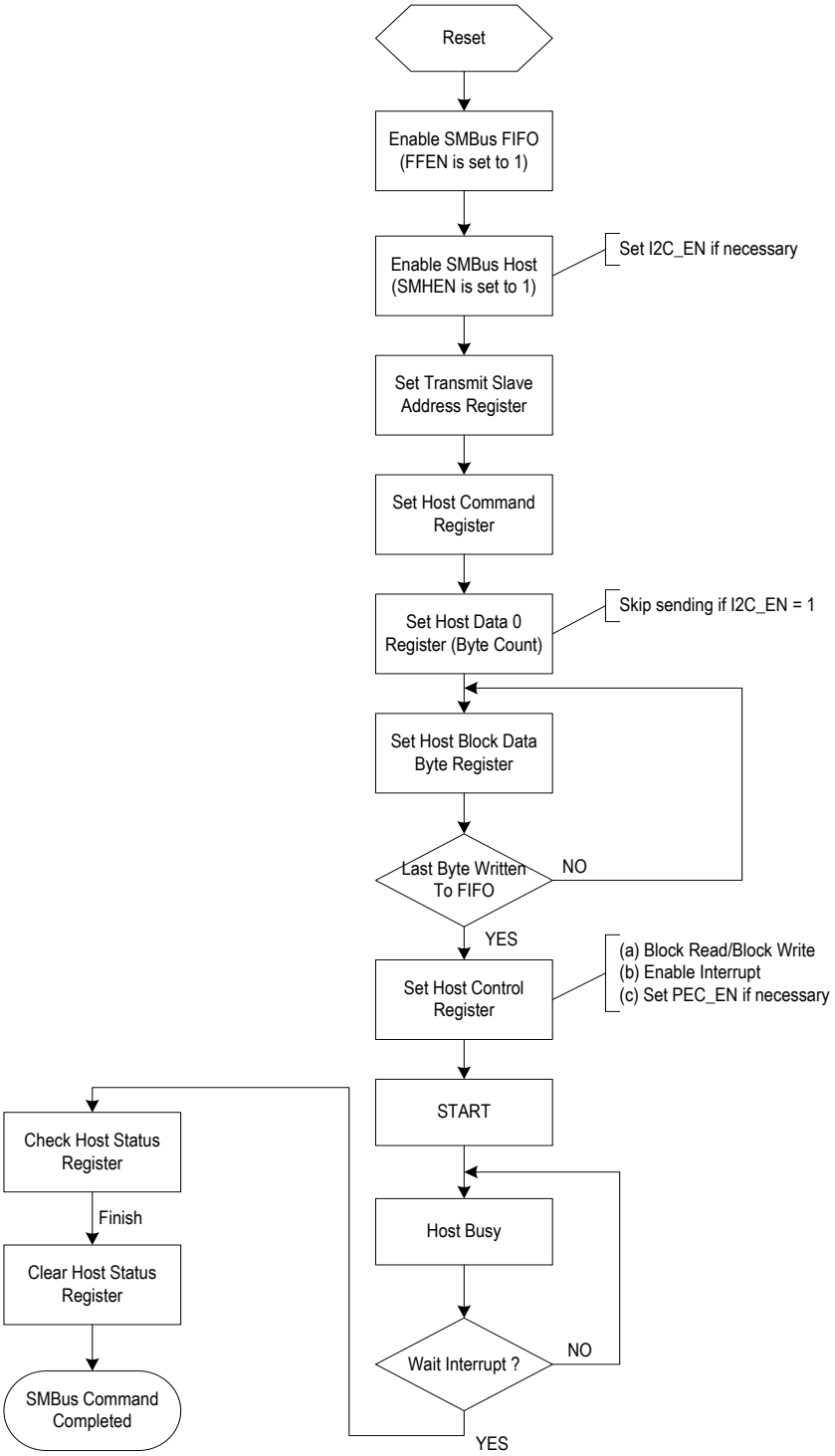
< I2C-compatible Write to Read Command >



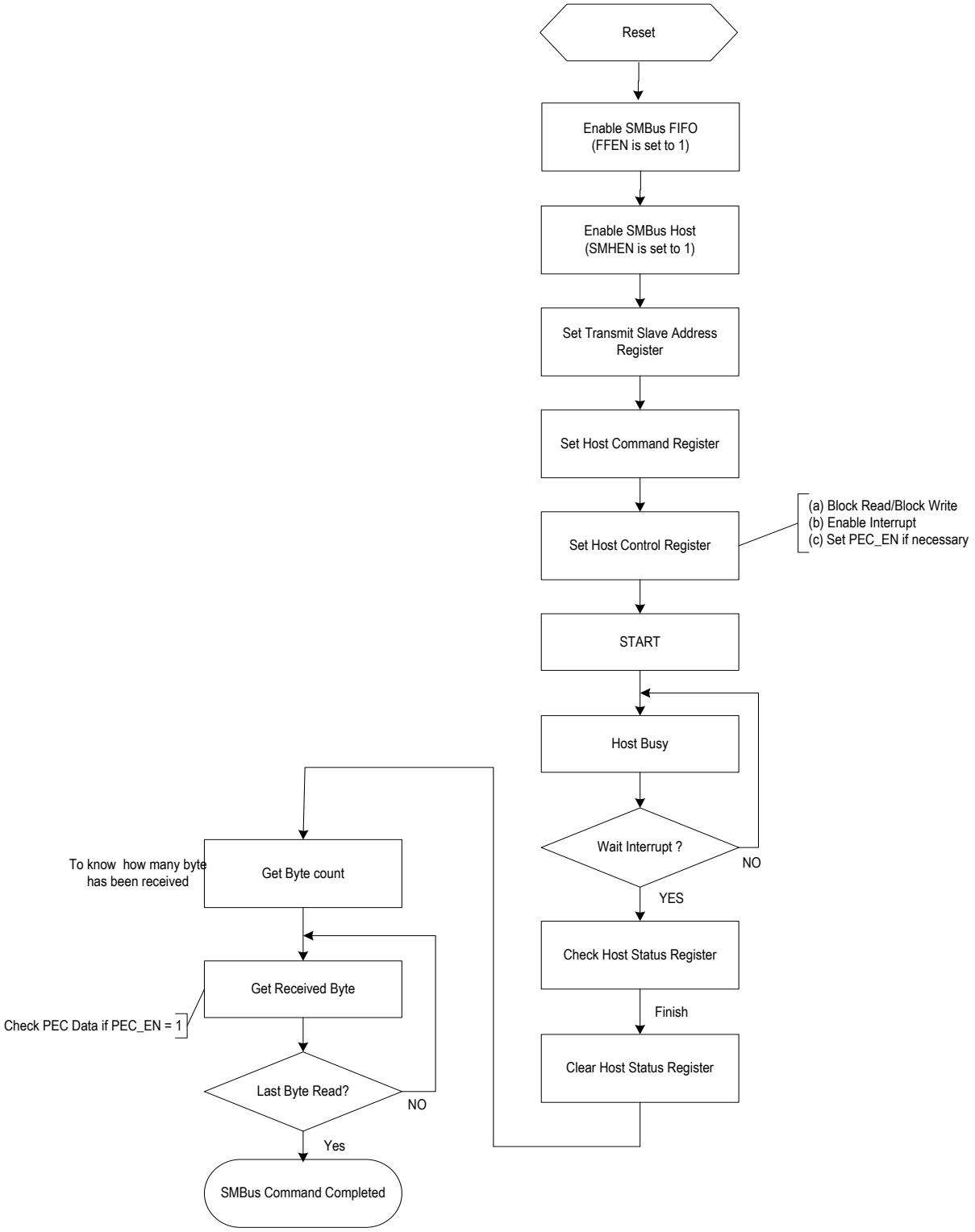
< I2C-compatible Write to Read Command (Dedicated FIFO Mode) >



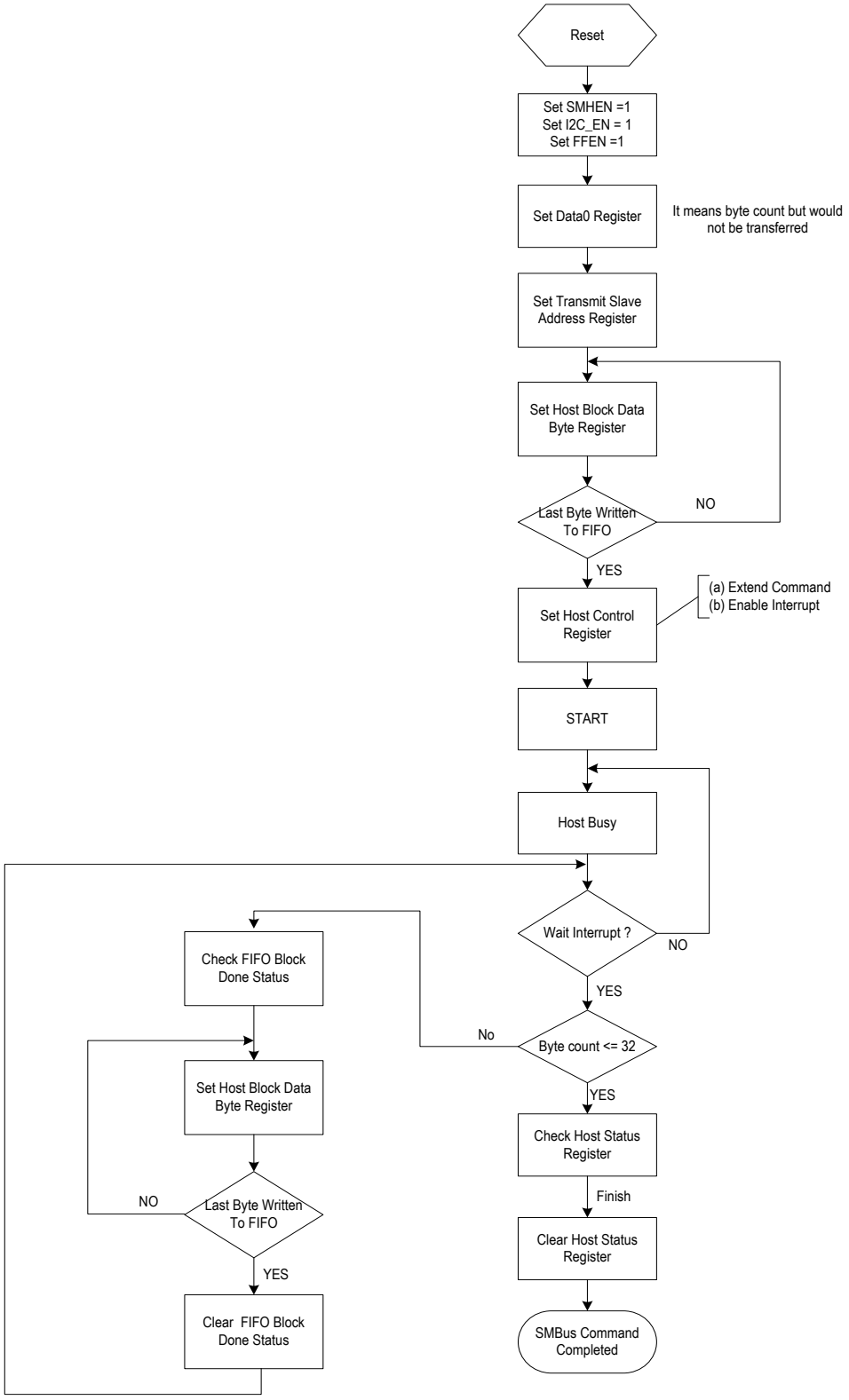
< I2C-compatible Read to Write Command >



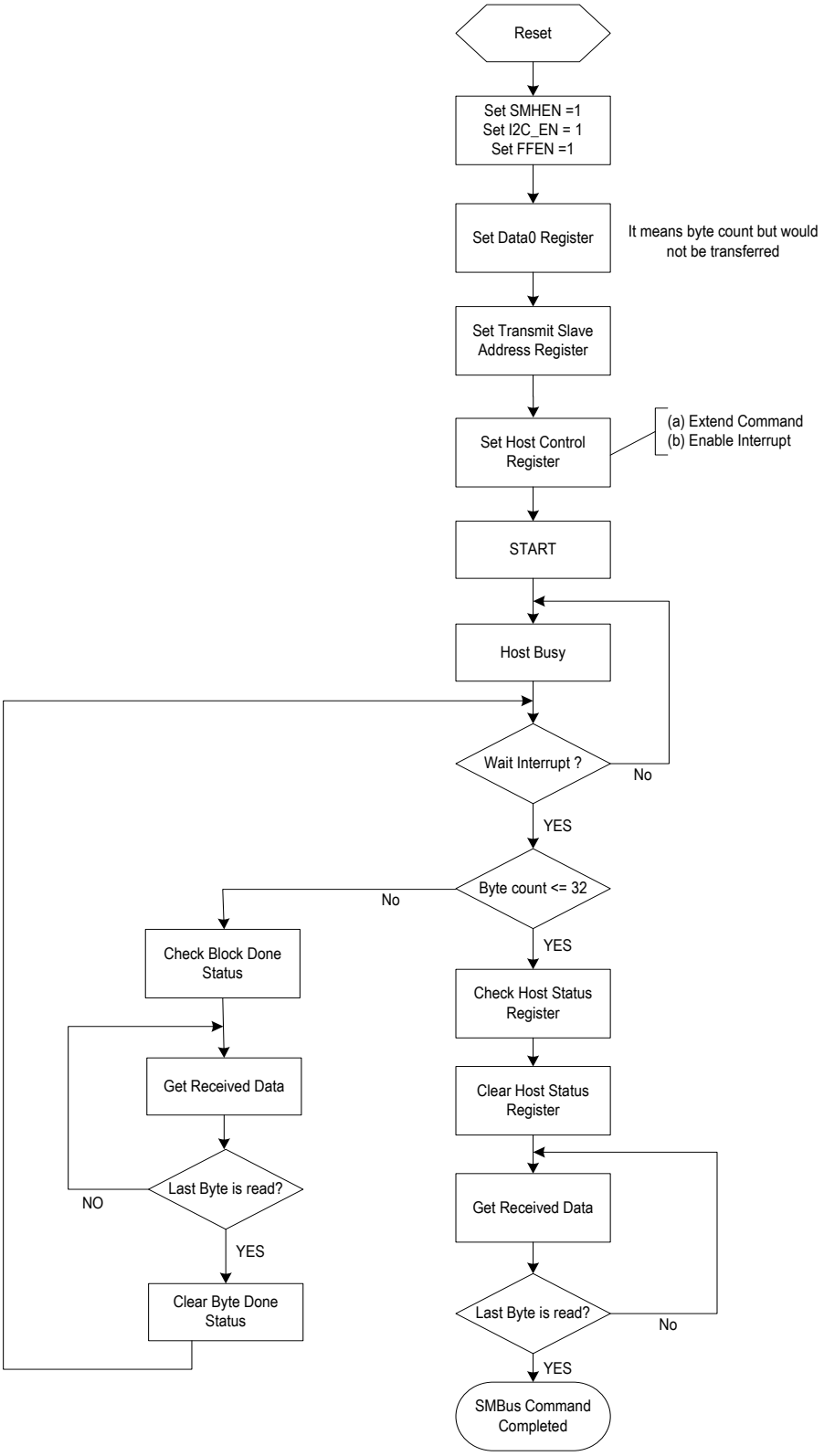
< Block Write Command (Dedicated FIFO Mode)>



< Block Read Command (Dedicated FIFO Mode)>



< I2C-compatible Write Command (Dedicated FIFO Mode)>



< I2C-compatible Read Command (Dedicated FIFO Mode)>

7.7.3.5 Description of SMCLK and SMDAT Line Control in Software Mode

(1) Control the SMCLK and SMDAT line by setting SCLCTL bit, SDACTLE bit, and SDACTL bit in SMBus Pin Control register (a.k.a., in software mode).
(2) When the SMCLK and SMDAT line are controlled in software mode, the hardware's SMBus logic will be reset, so the hardware will release the SMCLK and SMDAT line.
(3) The hardware's mechanism of 25 ms time-out will not work in software mode.

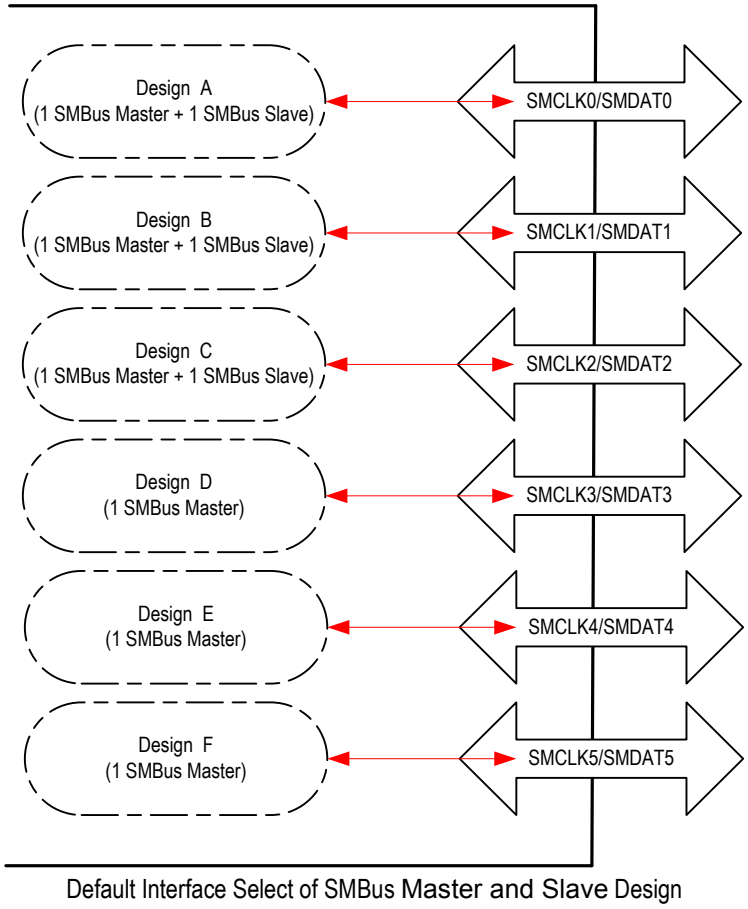
Note: It is recommended that SMCLK and SMDAT line should not be controlled in software mode and hardware mode simultaneously.

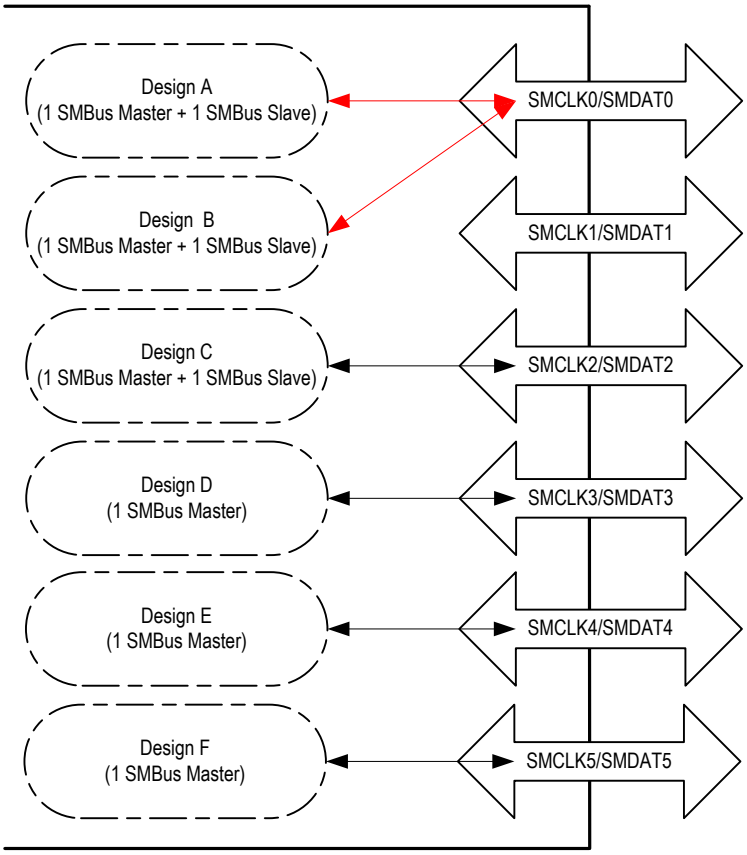
7.7.3.6 Description of SMBus Master and Slave Interface Select

The interface of the SMBus master and slave can be switched from SMCLK0/SMDAT0 to SMCLK5/SMDAT5 by setting the SDSIC, SDSIC2 and SDSIC3 registers.

Note: Switching the interfaces of the six designs (six master designs or three slave designs) to the same interface is invalid.

Figure 7-11. Schematic Diagram of SMBus Design Interface Select

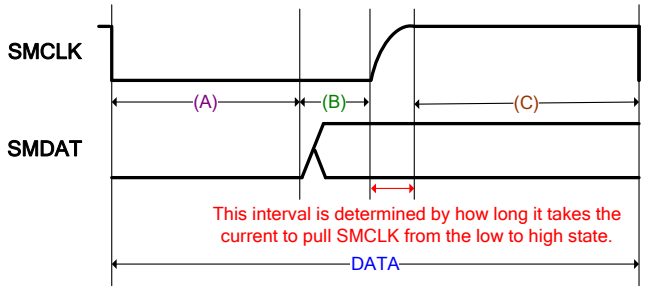




Invalid Interface Select of SMBus Master and Slave Design

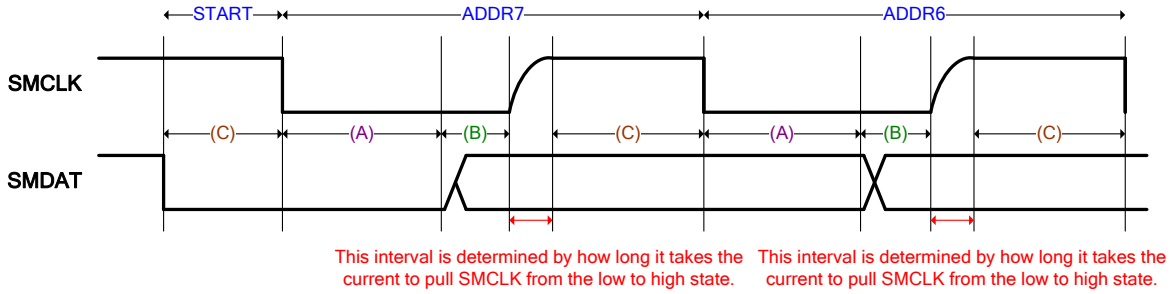
7.7.3.7 SMBus Waveform

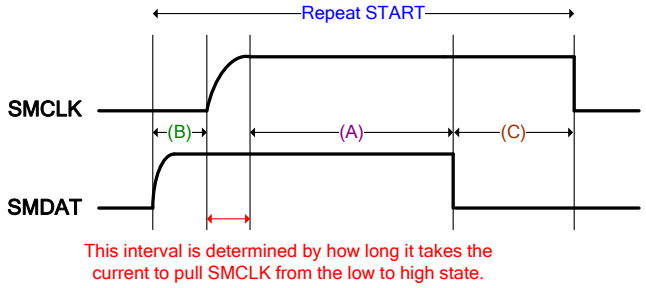
Figure 7-12. SMBus Waveform versus SMBus Timing Registers

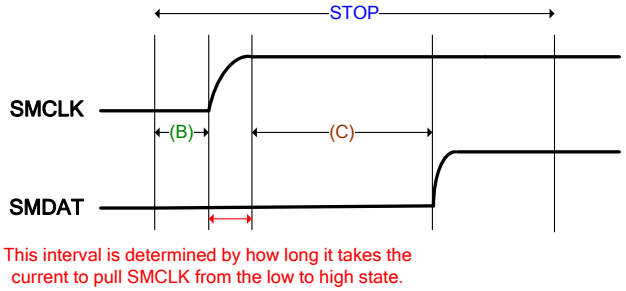


(A): ~=(VALUE_OF_4P7USREG / Freq_EC)
(B): ~=(VALUE_OF_250NSREG / Freq_EC)
(C): ~=(VALUE_OF_4P0USREG / Freq_EC)

where VALUE_OF_4P7USREG consists of 4P7USH and 4P7USL.
VALUE_OF_4P0USREG consists of 4P0USH and 4P0USL.







7.7.3.8 Expression of SMBus Interrupt Events

Table 7-12. SMBus Interrupt Events Expression

SMBus Interrupt Events	Interrupt Register	Description	
SMBus A Interrupt (Master)	b4@1C45h[MSTFCTRL1] & b0@1C01h[HOCTL]	Block Done Status 1	
	b7@1C00h[HOSTA] & b0@1C01h[HOCTL]	Byte Done Status	
	b6@1C00h[HOSTA] & b0@1C01h[HOCTL]	Time-out Error	
	b5@1C00h[HOSTA] & b0@1C01h[HOCTL]	Not Response ACK	
	b4@1C00h[HOSTA] & b0@1C01h[HOCTL]	Fail	
	b3@1C00h[HOSTA] & b0@1C01h[HOCTL]	Bus Error	

SMBus Interrupt Events	Interrupt Register	Description	
	b2@1C00h[HOSTA] & b0@1C01h[HOCTL]	Device Error	
	b1@1C00h[HOSTA] & b0@1C01h[HOCTL]	Finish Interrupt	
	b0@1C89h[HWPES] & b0@1C01h[HOCTL]	Master A Hardware PEC Check Error	
	b0@1C0Bh[SLSTA] & b0@1C0Ch[SICR]	Host Notify Status	
	b7@1C51h[MFTISTA]	Master A RX Interrupt Detected (for Dedicated FIFO threshold)	
	b3@1C51h[MFTISTA]	Master A TX Interrupt Detected (for Dedicated FIFO threshold)	
	b0@1C6Ah[IWRFISTA] & b0@1C69h[I2CW2RF]	Master A I2C Wr->Rd FIFO Interrupt Detected	
SMBus A Interrupt (Slave)	b1@1C0Bh[SLSTA] & b5@1C10h[HOCTL2] & b1@1C0Ch[SICR]	Slave Data Status	
	b2@1C0Bh[SLSTA] & b5@1C10h[HOCTL2] & b1@1C0Ch[SICR]	Slave Timeout Status	
	b5@1C0Bh[SLSTA] & b3@1C0Ch[SICR] & b5@1C10h[HOCTL2] & b1@1C0Ch[SICR]	Stop Condition Detect Status	
	b1@1C59h[SFTISTA] & b1@1C58h[SFTHEN] & b5@1C10h[HOCTL2] & b1@1C0Ch[SICR]	RX Interrupt Detected for Slave A (for Dedicated FIFO threshold)	
	b0@1C59h[SFTISTA] & b0@1C58h[SFTHEN] & b5@1C10h[HOCTL2] & b1@1C0Ch[SICR]	TX Interrupt Detected for Slave A (for Dedicated FIFO threshold)	
	b4@1C89h[HWPES] & b5@1C10h[HOCTL2] & b1@1C0Ch[SICR]	Slave A PEC Check Error	
SMBus B Interrupt (Master)	b4@1C47h[MSTFCTRL2] & b0@1C12h[HOCTL] & (b2-0@1C47h[MSTFCTRL2] = 000b)	Block Done Status 2	
	b7@1C11h[HOSTA] & b0@1C12h[HOCTL]	Byte Done Status	
	b6@1C11h[HOSTA] & b0@1C12h[HOCTL]	Time-out Error	
	b5@1C11h[HOSTA] & b0@1C12h[HOCTL]	Not Response ACK	
	b4@1C11h[HOSTA] & b0@1C12h[HOCTL]	Fail	
	b3@1C11h[HOSTA] & b0@1C12h[HOCTL]	Bus Error	
	b2@1C11h[HOSTA] & b0@1C12h[HOCTL]	Device Error	
	b1@1C11h[HOSTA] & b0@1C12h[HOCTL]	Finish Interrupt	
	b1@1C89h[HWPES] & b0@1C12h[HOCTL]	Master B Hardware PEC Check Error	
	b0@1C1Ch[SLSTA] & b0@1C1Dh[SICR]	Host Notify Status	
	b6@1C51h[MFTISTA]	Master B RX Interrupt Detected (for Dedicated FIFO threshold)	
	b2@1C51h[MFTISTA]	Master B TX Interrupt Detected (for Dedicated FIFO threshold)	
	b1@1C6Ah[IWRFISTA] & b1@1C69h[I2CW2RF]	Master B I2C Wr->Rd FIFO Interrupt Detected	
SMBus B Interrupt (Slave)	b1@1C1Ch[SLSTA] & b5@1C21h[HOCTL2] & b1@1C1Dh[SICR]	Slave Data Status	
	b2@1C1Ch[SLSTA] & b5@1C21h[HOCTL2] & b1@1C1Dh[SICR]	Slave Timeout Status	
	b5@1C1Ch[SLSTA] & b3@1C1Dh[SICR] & b5@1C21h[HOCTL2] & b1@1C1Dh[SICR]	Stop Condition Detect Status	

SMBus Interrupt Events	Interrupt Register	Description	
	b3@1C59h[SFTISTA] & b3@1C58h[SFTHEN] & b5@1C21h[HOCTL2] & b1@1C1Dh[SICR]	RX Interrupt Detected for Slave B (for Dedicated FIFO threshold)	
	b2@1C59h[SFTISTA] & b2@1C58h[SFTHEN] & b5@1C21h[HOCTL2] & b1@1C1Dh[SICR]	TX Interrupt Detected for Slave B (for Dedicated FIFO threshold)	
	b5@1C89h[HWPES] & b5@1C21h[HOCTL2] & b1@1C1Dh[SICR]	Slave B PEC Check Error	
SMBus C Interrupt (Master)	b4@1C47h[MSTFCTRL2] & b0@1C2Ah[HOCTL] & (b2-0@1C47h[MSTFCTRL2] = 001b)	Block Done Status 2	
	b7@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Byte Done Status	
	b6@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Time-out Error	
	b5@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Not Response ACK	
	b4@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Fail	
	b3@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Bus Error	
	b2@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Device Error	
	b1@1C29h[HOSTA] & b0@1C2Ah[HOCTL]	Finish Interrupt	
	b2@1C89h[HWPES] & b0@1C2Ah[HOCTL]	Master C Hardware PEC Check Error	
	b0@1C52h[SLSTA] & b0@1C53h[SICR]	Host Notify Status	
	b5@1C51h[MFTISTA]	Master C RX Interrupt Detected (for Dedicated FIFO threshold)	
	b1@1C51h[MFTISTA]	Master C TX Interrupt Detected (for Dedicated FIFO threshold)	
	b2@1C6Ah[IWRFISTA] & b2@1C69h[I2CW2RF]	Master C I2C Wr->Rd FIFO Interrupt Detected	
SMBus C Interrupt (Slave)	b1@1C52h[SLSTA] & b5@1C32h[HOCTL2] & b1@1C53h[SICR]	Slave Data Status	
	b2@1C52h[SLSTA] & b5@1C32h[HOCTL2] & b1@1C53h[SICR]	Slave Timeout Status	
	b5@1C52h[SLSTA] & b3@1C53h[SICR] & b5@1C32h[HOCTL2] & b1@1C53h[SICR]	Stop Condition Detect Status	
	b5@1C59h[SFTISTA] & b5@1C58h[SFTHEN] & b5@1C32h[HOCTL2] & b1@1C53h[SICR]	RX Interrupt Detected for Slave C (for Dedicated FIFO threshold)	
	b4@1C59h[SFTISTA] & b4@1C58h[SFTHEN] & b5@1C32h[HOCTL2] & b1@1C53h[SICR]	TX Interrupt Detected for Slave C (for Dedicated FIFO threshold)	
	b6@1C89h[HWPES] & b5@1C32h[HOCTL2] & b1@1C53h[SICR]	Slave C PEC Check Error	
SMBus D Interrupt (Master)	b4@1C47h[MSTFCTRL2] & b0@1C36h[HOCTL] & (b2-0@1C47h[MSTFCTRL2] = 010b)	Block Done Status 2	
	b7@1C35h[HOSTA] & b0@1C36h[HOCTL]	Byte Done Status	
	b6@1C35h[HOSTA] & b0@1C36h[HOCTL]	Time-out Error	
	b5@1C35h[HOSTA] & b0@1C36h[HOCTL]	Not Response ACK	
	b4@1C35h[HOSTA] & b0@1C36h[HOCTL]	Fail	
	b3@1C35h[HOSTA] & b0@1C36h[HOCTL]	Bus Error	
	b2@1C35h[HOSTA] & b0@1C36h[HOCTL]	Device Error	
	b1@1C35h[HOSTA] & b0@1C36h[HOCTL]	Finish Interrupt	
	b3@1C89h[HWPES] & b0@1C36h[HOCTL]	Master D Hardware PEC Check Error	

SMBus Interrupt Events	Interrupt Register	Description	
	b4@1C51h[MFTISTA]	Master D RX Interrupt Detected (for Dedicated FIFO threshold)	
	b0@1C51h[MFTISTA]	Master D TX Interrupt Detected (for Dedicated FIFO threshold)	
	b3@1C6Ah[IWRFISTA] & b3@1C69h[I2CW2RF]	Master D I2C Wr->Rd FIFO Interrupt Detected	
SMBus E Interrupt (Master)	b4@1C47h[MSTFCTRL2] & b0@1CA1h[HOCTL] & (b2-0@1C47h[MSTFCTRL2] = 011b)	Block Done Status 2	
	b7@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Byte Done Status	
	b6@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Time-out Error	
	b5@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Not Response ACK	
	b4@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Fail	
	b3@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Bus Error	
	b2@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Device Error	
	b1@1CA0h[HOSTA] & b0@1CA1h[HOCTL]	Finish Interrupt	
	b0@1C9Fh[HWPES2] & b0@1CA1h[HOCTL]	Master E Hardware PEC Check Error	
	b7@1C9Dh[MFTISTA2]	Master E RX Interrupt Detected (for Dedicated FIFO threshold)	
	b3@1C9Dh[MFTISTA2]	Master E TX Interrupt Detected (for Dedicated FIFO threshold)	
	b4@1C6Ah[IWRFISTA] & b6@1C6Ah[IWRFISTA]	Master E I2C Wr->Rd FIFO Interrupt Detected	
SMBus F Interrupt (Master)	b4@1C47h[MSTFCTRL2] & b0@1CB1h[HOCTL] & (b2-0@1C47h[MSTFCTRL2] = 100b)	Block Done Status 2	
	b7@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Byte Done Status	
	b6@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Time-out Error	
	b5@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Not Response ACK	
	b4@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Fail	
	b3@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Bus Error	
	b2@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Device Error	
	b1@1CB0h[HOSTA] & b0@1CB1h[HOCTL]	Finish Interrupt	
	b1@1C9Fh[HWPES2] & b0@1CB1h[HOCTL]	Master F Hardware PEC Check Error	
	b6@1C9Dh[MFTISTA2]	Master F RX Interrupt Detected (for Dedicated FIFO threshold)	
	b2@1C9Dh[MFTISTA2]	Master F TX Interrupt Detected (for Dedicated FIFO threshold)	
	b5@1C6Ah[IWRFISTA] & b7@1C6Ah[IWRFISTA]	Master F I2C Wr->Rd FIFO Interrupt Detected	

7.7.4 EC Interface Registers

The SMBus I/O registers are listed below. The base address for SMBus is 1C00h.
A, B, C, D, E and F are for design A, B, C, D, E and F respectively.

Table 7-13. EC View Register Map, SMBus

7 0	Offset
Host Status Register (HOSTA)	00h,11h,29h,35h, A0h,B0h
Host Control Register (HOCTL)	01h,12h,2Ah,36h, A1h,B1h
Host Command Register (HOCMD)	02h,13h,2Bh,37h, A2h,B2h
Transmit Slave Address Register (TRASLA)	03h,14h,2Ch,38h, A3h,B3h
Data 0 Register (D0REG)	04h,15h,2Dh,39h, A4h,B4h
Data 1 Register (D1REG)	05h,16h,2Eh,3Ah ,A6h,B6h
Host Block Data Byte Register (HOBDB)	06h,17h,2Fh,3Bh, A7h,B7h
Master PIO Packet Error Check Register (PECERC)	07h,18h,30h,3Ch, A8h,B8h
Receive Slave Address Register (RESLADR)	08h,19h,5Ah
Receive Slave Address Register 2 (RESLADR2)	3Fh,44h,54h
Slave Data Register (SLDA)	09h,1Ah,5Bh
SMBus Pin Control Register (SMBPCTL)	0Ah,1Bh,31h,3Dh ,A9h,B9h
Slave Status Register (SLSTA)	0Bh,1Ch,52h
Slave Interrupt Control Register (SICR)	0Ch,1Dh,53h
Notify Device Address Register (NDADR)	0Dh,1Eh,55h
Notify Data Low Byte Register (NDLB)	0Eh,1Fh,56h
Notify Data High Byte Register (NDHB)	0Fh,20h,57h
Host Control Register 2 (HOCTL2)	10h,21h,32h,3Eh, AAh,BAh
4.7 μs Low Register (4P7USL)	22h
4.0 μs Low Register (4P0USL)	23h
250 ns Register (250NSREG)	25h
25 ms Register (25MSREG)	26h
45.3 μs Low Register (45P3USLREG)	27h
45.3 μs High Register (45P3USHREG)	28h
4.7 μs And 4.0 μs High Register (4p7A4P0H)	33h
Slave Bridge Control Register (SLVISELR)	34h
SMCLK Timing Setting Register A (SCLKTS_A)	40h
SMCLK Timing Setting Register B (SCLKTS_B)	41h
SMCLK Timing Setting Register C (SCLKTS_C)	42h
SMCLK Timing Setting Register D (SCLKTS_D)	43h
Master FIFO Control 1 Register (MSTFCTRL1)	45h
Master FIFO Status 1 Register (MSTFSTS1)	46h
Master FIFO Control 2 Register (MSTFCTRL2)	47h
Master FIFO Status 2 Register (MSTFSTS2)	48h
Host Nack Source (HONACKSRC)	49h,4Ah,4Bh,4Ch ,ACh,BCh
Slave Dedicated FIFO Threshold (SLVFTH)	4Dh
DMA from Flash to SMB Dedicated FIFO Selection (DFTSDFSEL)	4Eh

7 0	Offset
Master Dedicated FIFO Threshold (MSTFTH)	4Fh
Master Dedicated FIFO Threshold Enable (MFTHEN)	50h
Master Dedicated FIFO Threshold Interrupt Status (MFTISTA)	51h
Slave Dedicated FIFO Threshold Enable (SFTHEN)	58h
Slave Dedicated FIFO Threshold Interrupt Status (SFTISTA)	59h
Slave A Dedicated FIFO Pre-defined Control Register (SADFPCTL)	5Eh
Slave A Dedicated FIFO Status (SFFSTA)	5Fh
SMBus Design Switch Interface Control (SDSIC)	60h
SMBus Design Switch Interface Control 2 (SDSIC2)	61h
Slave B Dedicated FIFO Pre-defined Control Register (SBDFPCTL)	62h
Slave B Dedicated FIFO Status (SBDFFSTA)	63h
Slave C Dedicated FIFO Control Register (SCDFFCTL)	64h
Slave C Dedicated FIFO Status (SCDFFSTA)	65h
I2C Wr to Rd FIFO Register (I2CW2RF)	69h
I2C Wr to Rd FIFO Interrupt Status (IWRFISTA)	6Ah
Shared FIFO Function Enable (SFFE)	6Fh
Master Shared FIFO Size Select (MSFSS)	76h
Slave Shared FIFO Size Select1 (SSFSS1)	77h
Shared FIFO Base Address For Master A (SFBAMA)	78h
Shared FIFO Base Address For Master BCD (SFBAMBCD)	7Eh
Shared FIFO Base Address For Slave A (SFBASA)	80h
Shared FIFO Base Address For Slave B (SFBASB)	82h
Shared FIFO Base Address For Slave B (SFBASC)	84h
Slave Shared FIFO Size Select2 (SSFSS2)	87h
Hardwired PEC Register (HWPEC)	88h
Hardwired PEC Error Status (HWPES)	89h
Slave Transaction PEC Control Register (SLVTPECC)	8Ah
Slave Hardwired PEC VALUE (SHWPECV)	8Bh,8Ch,8Dh
Bridge Timeout Interrupt Enable Register (BTOIER)	8Eh
I2C Shared FIFO Byte Count H (ISFBCH)	90h,91h,92h,93h ,A5h,B5h
SMBus Interface Switch Pin Control (SISPC)	73h
SMBus Design Switch Interface Control 3 (SDSIC3)	99h
Master Dedicated FIFO Threshold Enable 2 (MFTHEN2)	9Ch
Master Dedicated FIFO Threshold Interrupt Status 2 (MFTISTA2)	9Dh
Hardwired PEC Register 2 (HWPEC2)	9Eh
Hardwired PEC Error Status 2 (HWPES2)	9Fh
SMCLK Timing Setting Register E (SCLKTS_E)	ABh
SMCLK Timing Setting Register F (SCLKTS_F)	BBh

7.7.4.1 Host Status Register (HOSTA)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the source of the interrupt (Master Interface).

Address Offset: 00h/11h/29h/35h/A0h/B0h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7	R/WC	0b	**Byte Done Status (BDS)** This bit will be set to 1 when the host controller has received a byte (for Block Read commands and I2C-compatible cycles) or if it has completed the transmission of a byte (for Block Write commands and I2C-compatible cycles).
6	R/WC	0b	**Time-out Error (TMOE)** 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when 25ms time-out error occurs.
5	R/WC	0b	**Not Response ACK (NACK)** 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when the device does not respond ACK.
4	R/WC	0b	**Fail (FAIL)** 0: This bit is cleared by writing a 1 to the bit position. 1: Reading this bit will return 1 if KILL is set and a processing transmission is successfully killed.
3	R/WC	0b	**Bus Error (BSER)** 0: This bit is cleared by writing a 1 to the bit position. 1: The source of the interrupt is that the SMBus has lost arbitration.
2	R/WC	0b	**Device Error (DVER)** 0: This bit is cleared by writing a 1 to this bit's position. 1: This bit is set in one of the following conditions: (1) 25ms Time-out Error. (2) Not response ACK.
1	R/WC	0b	**Finish Interrupt (FINTR)** This bit will be set by termination of a command. 0: This bit is cleared by writing 1 to this position. 1: The source of the interrupt is the stop condition detected.
0	R	0b	**Host Busy (HOBY)** 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

7.7.4.2 Host Control Register (HOCTL)

Address Offset: 01h/12h/2Ah/36h/A1h/B1h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7	R/W	0b	**PEC Enable (PEC_EN)** 0: The transaction without the PEC (Packet Error Checking) phase0 appended 1: The transaction with the PEC phase appended.
6	W	0b	**Start (SRT)** 0: This bit will always return 0 on reads. 1: When this bit is set, the SMBus host controller will perform the requested transaction.
5	W	0b	**Last Byte (LABY)** This bit is used for Block Read command and I2C-compatible read cycle. Read returns 1 if the next byte is the last byte to be received for the block read command and I2C-compatible read cycle. The firmware shall write 1 to this bit when the next byte will be the last byte to be received for the block read command and I2C-compatible cycle.
4-2	R/W	000b	**SMBus Command (SMCD)** These bits indicate which command will be performed. Bit 0 of the Transmit Slave Address Register determines if this is a read or write command. 000:Quick Command 001:Send Byte/ Receive Byte 010:Write Byte/ Read Byte 011:Write Word/ Read Word 100:Process Call 101:Block Read/ Block Write 110:I2C Block Read 111:Extend Command
1	R/W	0b	**Kill (KILL)** 0: Normal SMBus Host controller functionality. 1: When this bit is set, kill the current host transaction. This bit, once set, has to be cleared by software to allow the SMBus Host controller to function normally.
0	R/W	0b	**Host Interrupt Enable (INTREN)** 0: Disable 1: Enable the generation of an interrupt for the master interface

7.7.4.3 Host Command Register (HOCMD)

Address Offset: 02h/13h/2Bh/37h/A2h/B2h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-0	R/W	00h	**Host Command Register (HCREG)** These bits are transmitted in the command field of the SMBus protocol.

7.7.4.4 Transmit Slave Address Register (TRASLA)

Address Offset: 03h/14h/2Ch/38h/A3h/B3h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-1	R/W	00h	**Address (ADR)** Address of the targeted slave.
0	R/W	0b	**Direction (DIR)** Direction of the host transfer. 0: Write 1: Read

7.7.4.5 Data 0 Register (D0REG)

Address Offset: 04h/15h/2Dh/39h/A4h/B4h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-0	R/W	00h	**Data 0 (D0)** These bits contain the data sent in the DATA0 (The first transaction date byte) field of the SMBus protocol. For block write commands, this register reflects the number (from 1 to 32) of bytes to transfer.

7.7.4.6 Data 1 Register (D1REG)

Address Offset: 05h/16h/2Eh/3Ah/A6h/B6h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-0	R/W	00h	**Data 1 (D1)** These bits contain the data sent in the DATA1 (Data Byte High) field of the SMBus protocol.

7.7.4.7 Host Block Data Byte Register (HOBDB)

Address Offset: 06h/17h/2Fh/3Bh/A7h/B7h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-0	R/W	00h	**Block Data (BLDT)** For a block write command, data is sent from this register. On block read command, the received data is stored in this register.

7.7.4.8 Master PIO Packet Error Check Register (PECERC)

Address Offset: 07h/18h/30h/3Ch/A8h/B8h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-0	R/W	00h	**Master PIO PEC Data (PECD)** These bits are written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software.

7.7.4.9 Receive Slave Address Register (RESLADR)

Address Offset: 08h/19h/5Ah for Design A/B/C respectively

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	00h	**Slave Address (SADR)** These bits are the slave address decoded for read and write cycles.

7.7.4.10 Receive Slave Address Register 2 (RESLADR2)

Address Offset: 3Fh/44h/54h for Design A/B/C respectively

Bit	R/W	Default	Description
7	R/W	0b	**Slave Address 2 Enable** 0: SADR2 field is ignored. 1: SADR2 field holds a valid address and enables the function to decode SADR2 for comparison with the received address.
6-0	R/W	00h	**Slave Address 2 (SADR2)** These bits are the slave address 2 decoded for read and write cycles.

7.7.4.11 Slave Data Register (SLDA)

Address Offset: 09h/1Ah/5Bh for Design A/B/C respectively

Bit	R/W	Default	Description
7-0	R/W	00h	**Slave Data Byte0 (SDB0)** For the non-FIFO mode, this register stores the data received from the external master. When this register is served, software must write/read data stored in this register twice to release the SCL line. (See also section 7.7.3.3 SMBus Porting Guide on page 281) For the dedicated FIFO mode, this register stores the data received from the external master.When this register is served, software must write/read data stored in this register once to release the SCL line.

7.7.4.12 SMBus Pin Control Register (SMBPCTL)

Address Offset: 0Ah/1Bh/31h/3Dh/A9h/B9h for Design A/B/C/D/E/F respectively

	R/W	Default	Description
7-5	-	0h	**Reserved**
4	W	0b	**SMDAT Control Enable (SDACTLE)** This bit is used to enable the SMDAT Control (SDACTL) bit setting. It is write-only, and always returns 0 on reads.
3	R/W	1b	**SMDAT Control (SDACTL)** Only when the SMDAT Control Enable (SDACTLE) bit is set to 1 to 1 at the same time, this bit can be written as the following: 0: The Master ch A/B/C/E/F pin will be driven low regardless of the other SMBus logic. 1: The Master ch A/B/C/E/F pin will not be driven low. The other SMBus logic controls this pin.
2	R/W	1b	**SMCLK Control (SCLCTL)** 0: The Master ch A/B/C pin will be driven low regardless of the other SMBus logic. 1: The Master ch A/B/C pin will not be driven low. The other SMBus logic controls this pin.
1	R	-	**SMDAT Current State (SMBDCS)** This bit returns the value of the Master ch A/B/C/E/F pin. 0: Low 1: High
0	R	-	**SMCLK Current State (SMBCS)** This bit returns the value of the Master ch A/B/C/E/F pin. 0: Low 1: High

7.7.4.13 Slave Status Register (SLSTA)

Software can read this register to know the source of the interrupt (Slave Interface).

Address Offset: 0Bh/1Ch/52h for Design A/B/C respectively

Bit	R/W	Default	Description
7	R/WC	0b	**Slave Stretch SMBCLK Low Status (SSSLS)** 1: SMB Slave A is stretching SMBCLK low. 0: This bit will be auto-cleared if SSCL bit is disabled.
6	-	1b	**Reserved**
5	R/WC	0b	**Stop Condition Detect Status (SPDS)** 0: Cleared by writing a 1 to this bit. 1: Indicate Stop Condition detected.
4	R	0b	**Match Slave Address 2 (MSLA2)** 0: The received address is matched with SADR. 1: The received address is matched with SADR2. Don't care when Host notify command.
3	R	0b	**Read Cycle Status (RCS)** Direction of the slave transfer. 0: Write. 1: Read.
2	R/WC	0b	**Slave Timeout Status (STS)** 0: Cleared by writing a 1 to this bit. 1: Timeout status occurs.

Bit	R/W	Default	Description
1	R/WC	0b	**Slave Data Status (SDS)** 0: Cleared by writing a 1 to this bit. 1: Slave Data Register is waiting for read or write. When this bit is set and the Read Cycle Status (RCS) bit is low, the software shall read the data from the Slave Data Register. When this bit is set and the Read Cycle Status (RCS) bit is high, the software shall write the data to the Slave Data Register.
0	R/WC	0b	**Host Notify Status (HONOST)** This bit will be set to 1 when a Host Notify command has been completely received. Software can read this bit to determine that the source of the interrupt is the reception of the Host Notify Command.

Note: The firmware is required to check **SCIS** before enable bit **SSCL** and after "CLR EA".

7.7.4.14 Slave Interrupt Control Register (SICR)

Address Offset: 0Ch/1Dh/53h for Design A/B/C respectively

Bit	R/W	Default	Description
7-4	-	00h	**Reserved**
3	R/W	0b	**Slave Detect STOP Condition Interrupt Enable (SDSEN)** 0: Disable 1: Enable the generation of an interrupt for STOP detected by slave.
2	R/W	0b	**Slave SMDAT Low Timeout Enable (SDLTOEN)** This bit controls the reset mechanism of SMBus Slave to handle the SMDAT line low if 25ms timeout. 0: SMCLK will be released if timeout. 1: SMCLK/SMDAT will be released if timeout.
1	R/W	0b	**Slave Interrupt Enable (SITEN)** 0: Disable 1: Enable the generation of an interrupt for the slave interface.
0	R/W	0b	**Host Notify Interrupt Enable (HONOIN)** 0: Disable 1: Enable the generation of an interrupt when Host Notify Status is set and it dose not affect the setting of the Host Notify Status bit.

7.7.4.15 Notify Device Address Register (NDADR)

Address Offset: 0Dh/1Eh/55h for Design A/B/C respectively

Bit	R/W	Default	Description
7-1	R	00h	**Device Address (DVADR)** These bits contain the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification.
0	-	0b	**Reserved**

7.7.4.16 Notify Data Low Byte Register (NDLB)

Address Offset: 0Eh/1Fh/56h for Design A/B/C respectively

Bit	R/W	Default	Description
7-0	R	00h	**Data Low Byte (DALB)** These bits contain the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

7.7.4.17 Notify Data High Byte Register (NDHB)

Address Offset: 0Fh/20h/57h for Design A/B/C respectively

Bit	R/W	Default	Description
7-0	R	00h	**Data High Byte (DAHB)** These bits contain the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

7.7.4.18 Host Control Register 2 (HOCTL2)

Address Offset: 10h/21h/32h/3Eh/AAh/BAh for Design A/B/C/D/E/F respectively

Bit	R/W	Default	Description
7	R/W	0b	**Slave Stretch Clock Low (SSCL)** 1: Enable "SMBus slave hold clock after the start bit received". 0: Disable "SMBus slave hold clock after the start bit received". Only for slave A/B/C.
6	-	0b	**Reserved**
5	R/W	1b (Design A) 1b (Design B) 0b (Design C)	**SMBus Slave Enable (SLVEN)** 0: Disable the SMBus Slave Device. 1: Enable the SMBus Slave Device. The SMBus Host Controller is disabled when this bit is set. Only for slave A/B/C.
4	R/W	0b	**SMDAT Timeout Enable (SMD_TO_EN)** This bit controls the reset mechanism of SMBus Master to handle the SMDAT line low if 25ms timeout. 0: SMCLK will be released if timeout. 1: SMCLK/SMDAT will be released if timeout.
3	R/W	0b	**I2C Switch Direction Enable (I2C_SW_EN)** 0: Disable I2C Switch Direction. 1: Enable I2C Switch Direction.
2	R/W	0b	**I2C Switch Direction Wait (I2C_SW_WAIT)** 0: Disable I2C Switch Direction Wait. 1: Enable I2C Switch Direction Wait.
1	R/W	0b	**I2C Enable (I2C_EN)** 0: SMBus behavior. 1: Enable to communicate with I2C device and support I2C-compatible cycles. When this bit is set, the SMBus logic will instead be set to communicate with I2C devices and support I2C-compatible cycles. This forces the following changes: (1) The Process Call command will skip the Command code. (2) The Block Write command will skip sending the Byte Count. (3) The Extend command can be used to support I2C-compatible cycles.
0	R/W	0b	**SMBus Host Enable (SMHEN)** 0: Disable the SMBus Host Controller. 1: The SMBus Host interface is enabled to execute commands.

7.7.4.19 4.7 μs Low Register (4P7USL)

The following registers (22h-28h, 33h) define the SMCLK0/1/2/3/4/5 and SMDAT0/1/2/3/4/5 timing.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.7 μs Low Register (4P7USL)** This 4.7 μs Low Register and 4.7 μs high bit (in the 4.7 μs and 4.0 μs High Register) define the count number for the 4.7 μs counter. The 4.7 μs is (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 530)

7.7.4.20 4.0 μs Low Register (4P0USL)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.0 μs Low Register (4P0USL)** This 4.0 μs Low Register and 4.0 μs high bit (in the 4.7 μs and 4.0 μs High Register) define the count number for the 4.0 μs counter. The 4.0 μs is (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 530)

7.7.4.21 250 ns Register (250NSREG)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	00h	**250ns Register (250NS)** This field defines the SMDAT0/1/2/3/4/5 setup time. This byte is the count number of the counter for 250 ns. The 250 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 530)

7.7.4.22 25 ms Register (25MSREG)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	19h	**25 ms Register (25MS)** This field defines the SMCLK0/1/2/3/4/5 clock low timeout. This byte is the count number of the counter for 25 ms. The 25 ms is calculated by (count number *1.024 kHz).

7.7.4.23 45.3 μs Low Register (45P3USLREG)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 μs Low Register (45P3USLOW)** This 45.3 μs Low Register, 45.3 μs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7μs And 4.0 μs High Register) define the SMCLK0/1/2/3/4/5 high periodic (maximal). (45.3μs + 4.7μs=50μs) This byte is the count number bits [7:0] of the counter for 45.3 μs. The 45.3 μs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 10-2 on page 530)

7.7.4.24 45.3 μs High Register (45P3USHREG)

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 μs High Register (45P3USHGH)** This 45.3 μs Low Register, 45.3 μs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7μs And 4.0 μs High Register) define the SMCLK0/1/2/3/4/5 high periodic (maximal). (45.3 μs + 4.7μs=50μs). This byte is the count number bits [15:8] of the counter for 45.3 μs. The 45.3 μs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 10-2 on page 530)

7.7.4.25 4.7 μs And 4.0 μs High Register (4p7A4P0H)

Address Offset: 33h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**4.0 μs High Bit (4P0USH)** This bit is bit 8 of the count number for the 4.0 μs counter. This 4.0 μs Low Register and 4.0μs High Bit define the count number for the 4.0 μs counter.
0	R/W	0b	**4.7 μs High Bit (4P7USH)** This bit is bit 8 of the count number for the 4.7 μs counter. This 4.7 μs Low Register and 4.7μs High Bit define the count number for the 4.7 μs counter.

7.7.4.26 Slave Bridge Control Register (SLVISELR)

Address Offset: 34h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	0b	**Slave B Bridge Function (SBBF)** 0b: Disable 1b: Enable
5	R/W	0b	**Slave A Bridge Function (SABF)** 0b: Disable 1b: Enable
4	R/W	0b	**Override Debug Mode through SMBus (OVRSMDBG)** This bit overrides Debug Mode function enabled by hardware strap in SMBus interface and disables it.
3-2	-	01b	**Reserved**
1-0	-	00b	**Reserved**

7.7.4.27 SMCLK Timing Setting Register A (SCLKTS_A)

Address Offset: 40h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 7-12 on page 310 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	1b	**SMCLK 1MHz Setting (SCLKA1M)** 0b: Disable 1b: 1MHz for Design A.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to determine which SMCLK rate is for design A. If Disable, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.7.4.28 SMCLK Timing Setting Register B (SCLKTS_B)

Address Offset: 41h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 7-12 on page 310 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	1b	**SMCLK 1MHz Setting (SCLKB1M)** 0b: Disable 1b: 1MHz Design B.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to determine which SMCLK rate is for design B. If Disable, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.7.4.29 SMCLK Timing Setting Register C (SCLKTS_C)

Address Offset: 42h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 7-12 on page 310 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	0b	**SMCLK 1MHz Setting (SCLKC1M)** 0b: Disable 1b: 1MHz Design C.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to decide which SMCLK rate for the design C. If Disable, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.7.4.30 SMCLK Timing Setting Register D (SCLKTS_D)

Address Offset: 43h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 7-12 on page 310 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	0b	**SMCLK 1MHz Setting (SCLKD1M)** 0b: Disable 1b: 1MHz Design D.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to decide which SMCLK rate for the design D. If Disable, the SMCLK rate depends on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.7.4.31 Master FIFO Control 1 Register (MSTFCTRL1)

Address Offset: 45h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/WC	0b	**Block Done Status 1 (BLKDS1)** This bit will be set to 1 when the host controller has received or transmitted one block of 32 bytes while the byte count is set larger than 32 for I2C-compatible FIFO Mode cycles. Write to clear, then HW automatically do the successive read/write cycle. (This is for design A FIFO) **Start Fetch Data From Shared FIFO (SFDFSF)** For the I2C non-FIFO to shared FIFO write command, once software wants to enable the FIFO mode, it is required to write this bit to start fetch data from the shared FIFO. (This is for design A)
3	R/W	0b	**FIFO 1 Enable (FF1EN)** 0: Disable SMB design A in FIFO Mode. 1: Enable SMB design A in FIFO Mode. (This is for design A dedicated FIFO)
2-0	R/W	000b	**Reserved**

7.7.4.32 Master FIFO Status 1 Register (MSTFSTS1)

Address Offset: 46h

Bit	R/W	Default	Description
7	R	-	**FIFO 1 Empty** (This is for design A dedicated FIFO)
6	R	-	**FIFO 1 Full** (This is for design A dedicated FIFO)
5-0	R	-	**FIFO 1 Byte Count** (This is for design A dedicated FIFO)

7.7.4.33 Master FIFO Control 2 Register (MSTFCTRL2)

Address Offset: 47h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/WC	0b	**Block Done Status 2 (BLKDS2)** This bit will be set to 1 when the host controller has received or transmitted one block of 32 bytes while the byte count is set larger than 32 for I2C-compatible FIFO Mode cycles. Write to clear, then HW automatically do the successive read/write cycle. (This is for the second FIFO, which can be used by design B, design C or design D.) **Start Fetch Data From Shared FIFO (SFDFSF)** For the I2C non-FIFO to the shared FIFO write command, once software wants to enable the FIFO mode, it is required to write this bit to start fetch data from the shared FIFO. (This is for design B, C, and D)
3	R/W	0b	**FIFO 2 Enable (FFEN2)** 0: Disable FIFO 2. 1: Enable FIFO 2. (This is for the second FIFO, which can be used by design B, design C or design D.)
2-0	R/W	000b	**FIFO 2 Design Select (FFCHSEL2)** 000b: Switch FIFO to Design B. 001b: Switch FIFO to Design C. 010b: Switch FIFO to Design D. 011b: Switch FIFO to Design E. 100b: Switch FIFO to Design F. Otherwise: Reserved

7.7.4.34 Master FIFO Status 2 Register (MSTFSTS2)

Address Offset: 48h

Bit	R/W	Default	Description
7	R	-	**FIFO 2 Empty** (This is for the second FIFO, which can be used by design B, design C or design D.)
6	R	-	**FIFO 2 Full** (This is for the second FIFO, which can be used by design B, design C or design D.)
5-0	R	-	**FIFO 2 Byte Count** (This is for the second FIFO, which can be used by design B, design C or design D.)

7.7.4.35 Host Nack Source (HONACKSRC)

Address Offset: 49h/4Ah/4Bh/4Ch/ACh/BCh for Design A/B/C/D/E/F respectively

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**SMCLK & SMDAT Timeout Disable (SMCDTD)** 0: Enable 1: Disable timeout function
3	-	-	**Reserved**
2-0	R/WC	000b	**Host Nack Source (HNACKS)** 000: No nack_error 001: Slave address nack error 010: Command nack error 011: Slave address read nack error 100: Data low byte nack error (DL) 101: Data high byte nack error (DH) 110: Data nack error (for block write) 111: PEC nack error (Writing 111b can be cleared.)

7.7.4.36 Slave Dedicated FIFO Threshold (SLVFTH)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	01b	**Slave Dedicated FIFO Threshold (SFTH)** 00: The threshold is 4 bytes. 01: The threshold is 8 bytes. 10: The threshold is 12 bytes.

7.7.4.37 DMA from Flash to SMB Dedicated FIFO Selection (DFTSDFSEL)

Address Offset: 4Eh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
2-0	R/W	000b	**DMA from Flash to SMB Dedicated FIFO Selection (DFTSDFS)** 000: Slave A dedicated FIFO. 001: Slave B dedicated FIFO. 010: Slave C dedicated FIFO. 100: FIFO 1 dedicated FIFO. (Master A) 101: FIFO 2 dedicated FIFO. (Master B or Master C or Master D) Others: Reserved.

Note: (1) DMA related registers are SCARSL, SCARSM, and SCARSH.

(2) DMA is used as shadow flash content of the Scratch SRAM SMBus address to SMBus Slave or Master dedicated FIFO. For Slave dedicated FIFO, the transmission unit of DMA is 16 bytes at a time, and will align 16-byte boundary. The source inside the flash must be located on 16-boundary. For Master dedicated FIFO, the transmission unit of DMA is 32 bytes at a time, and the source inside the flash must be located on 32-boundary.

7.7.4.38 Master Dedicated FIFO Threshold (MSTFTH)

Address Offset: 4Fh

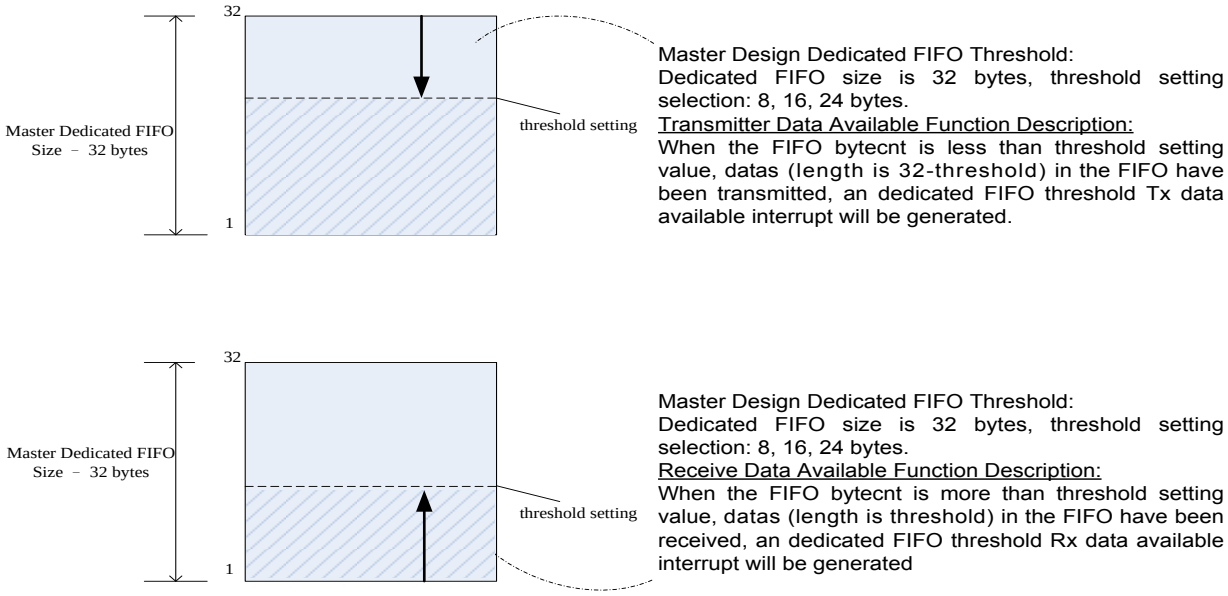
Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	01b	**Master Dedicated FIFO Threshold (MFTH)** 00: The threshold is 8 bytes. 01: The threshold is 16 bytes. 10: The threshold is 24 bytes.

7.7.4.39 Master Dedicated FIFO Threshold Enable (MFTHEN)

Address Offset: 50h

Bit	R/W	Default	Description
7	R/W	0b	**Master A Receive Data Available Function (MARDA)** 0: Disable 1: Enable
6	R/W	0b	**Master B Receive Data Available Function (MBRDA)** 0: Disable 1: Enable
5	R/W	0b	**Master C Receive Data Available Function (MCRDA)** 0: Disable 1: Enable
4	R/W	0b	**Master D Receive Data Available Function (MDRDA)** 0: Disable 1: Enable
3	R/W	0b	**Master A Transmitter Data Available Function (MATDA)** 0: Disable 1: Enable
2	R/W	0b	**Master B Transmitter Data Available Function (MBTDA)** 0: Disable 1: Enable
1	R/W	0b	**Master C Transmitter Data Available Function (MCTDA)** 0: Disable 1: Enable
0	R/W	0b	**Master D Transmitter Data Available Function (MDTDA)** 0: Disable 1: Enable

Figure 7-13. Master Design Dedicated FIFO Threshold Description



7.7.4.40 Master Dedicated FIFO Threshold Interrupt Status (MFTISTA)

Address Offset: 51h

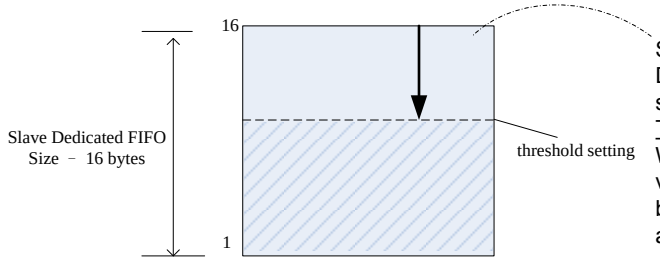
Bit	R/W	Default	Description
7	R/WC	0b	**Master A RX Interrupt Detected (MARID)** 0: Cleared by writing a 1 to this bit. 1: Master A Receive Data Available Interrupt is detected.
6	R/WC	0b	**Master B RX Interrupt Detected (MBRID)** 0: Cleared by writing a 1 to this bit. 1: Master B Receive Data Available Interrupt is detected.
5	R/WC	0b	**Master C RX Interrupt Detected (MCRID)** 0: Cleared by writing a 1 to this bit. 1: Master C Receive Data Available Interrupt is detected.
4	R/WC	0b	**Master D RX Interrupt Detected (MDRID)** 0: Cleared by writing a 1 to this bit. 1: Master D Receive Data Available Interrupt is detected.
3	R/WC	0b	**Master A TX Interrupt Detected (MATID)** 0: Cleared by writing a 1 to this bit. 1: Master A Transmitter Data Available Interrupt is detected.
2	R/WC	0b	**Master B TX Interrupt Detected (MBTID)** 0: Cleared by writing a 1 to this bit. 1: Master B Transmitter Data Available Interrupt is detected.
1	R/WC	0b	**Master C TX Interrupt Detected (MCTID)** 0: Cleared by writing a 1 to this bit. 1: Master C Transmitter Data Available Interrupt is detected.
0	R/WC	0b	**Master D TX Interrupt Detected (MDTID)** 0: Cleared by writing a 1 to this bit. 1: Master D Transmitter Data Available Interrupt is detected.

7.7.4.41 Slave Dedicated FIFO Threshold Enable (SFTHEN)

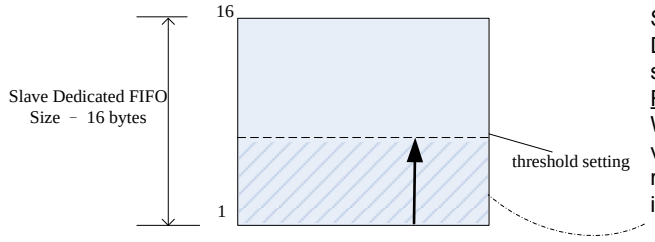
Address Offset: 58h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**Slave C Receive Data Available Function (SCRDAF)** 0: Disable 1: Enable
4	R/W	0b	**Slave C Transmitter Data Available Function (SCTDAF)** 0: Disable 1: Enable
3	R/W	0b	**Slave B Receive Data Available Function (SBRDAF)** 0: Disable 1: Enable
2	R/W	0b	**Slave B Transmitter Data Available Function (SBTDAF)** 0: Disable 1: Enable
1	R/W	0b	**Slave A Receive Data Available Function (SARDAF)** 0: Disable 1: Enable
0	R/W	0b	**Slave A Transmitter Data Available Function (SATDAF)** 0: Disable 1: Enable

Figure 7-14. Slave Design Dedicated FIFO Threshold Description



Slave Design Dedicated FIFO Threshold:
Dedicated FIFO size is 1 6 bytes, threshold setting selection: 4, 8, 12 bytes.
Transmitter Data Available Function Description:
When the FIFO bytecnt is less than threshold setting value, datas (length is 16-threshold) in the FIFO have been transmitted, an dedicated FIFO threshold Tx data available interrupt will be generated.



Slave Design Dedicated FIFO Threshold:
Dedicated FIFO size is 1 6 bytes, threshold setting selection: 4, 8, 12 bytes.
Receive Data Available Function Description:
When the FIFO bytecnt is more than threshold setting value, datas (length is threshold) in the FIFO have been received, an dedicated FIFO threshold Rx data available interrupt will be generated

7.7.4.42 Slave Dedicated FIFO Threshold Interrupt Status (SFTISTA)

Address Offset: 59h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/WC	0b	**Slave C RX Interrupt Detected for Slave C (SCRIDSC)** 0: Cleared by writing a 1 to this bit. 1: Receive data available interrupt is detected for Slave C.
4	R/WC	0b	**Slave C TX Interrupt Detected for Slave C (SCTXIDSC)** 0: Cleared by writing a 1 to this bit. 1: Transmitter data available interrupt is detected for Slave C.
3	R/WC	0b	**Slave B RX Interrupt Detected for Slave B (SBRIDSB)** 0: Cleared by writing a 1 to this bit. 1: Receive data available interrupt is detected for Slave B.
2	R/WC	0b	**Slave B TX Interrupt Detected for Slave B (SBTXIDSB)** 0: Cleared by writing a 1 to this bit. 1: Transmitter data available interrupt is detected for Slave B.
1	R/WC	0b	**Slave A RX Interrupt Detected for Slave A (RIDSA)** 0: Cleared by writing a 1 to this bit. 1: Receive data available interrupt is detected for Slave A.
0	R/WC	0b	**Slave A TX Interrupt Detected for Slave A (TXIDSA)** 0: Cleared by writing a 1 to this bit. 1: Transmitter data available interrupt is detected for Slave A.

7.7.4.43 Slave A Dedicated FIFO Pre-defined Control Register (SADFPCTL)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	1b	**Hardware Slave A (For Pre-defined) Follow Mode Enable (HSAPFME)** 1: Enable 0: Disable
2	R	0b	**Slave A Bridge Busy Status (SABBS)** 0: Not Busy. 1: Busy.
1	R/W	1b	**Hardware Slave A (for Pre-defined) Enable (HSAPE)** 1: Enable 0: Disable
0	R/W	0b	**Slave A Dedicated FIFO Enable (SADFE)** 1: Enable 0: Disable

7.7.4.44 Slave A Dedicated FIFO Status (SFFSTA)

Address Offset: 5Fh

Bit	R/W	Default	Description
7	R	-	**FIFO Empty**
6	R	-	**FIFO Full**
5	-	-	**Reserved**
4-0	R	-	**FIFO Byte Count**

7.7.4.45 SMBus Design Switch Interface Control (SDSIC)

Address Offset: 60h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-4	R/W	000b	**Design B (Master B and Slave B) Switch to Interface (DBSTI)** 000: Interface 1 (SMCLK1/SMDAT1) 001: Interface 0 (SMCLK0/SMDAT0) 010: Interface 1 (SMCLK1/SMDAT1) 011: Interface 2 (SMCLK2/SMDAT2) 100: Interface 3 (SMCLK3/SMDAT3) 101: Interface 4 (SMCLK4/SMDAT4) 110: Interface 5 (SMCLK4/SMDAT5) Others: Reserved
3	-	0b	**Reserved**
2-0	R/W	000b	**Design A (Master A and Slave A) Switch to Interface (DASTI)** 000: Interface 0 (SMCLK0/SMDAT0) 001: Interface 0 (SMCLK0/SMDAT0) 010: Interface 1 (SMCLK1/SMDAT1) 011: Interface 2 (SMCLK2/SMDAT2) 100: Interface 3 (SMCLK3/SMDAT3) 101: Interface 4 (SMCLK4/SMDAT4) 110: Interface 5 (SMCLK4/SMDAT5) Others: Reserved

7.7.4.46 SMBus Design Switch Interface Control 2 (SDSIC2)

Address Offset: 61h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-4	R/W	000b	**Design D (Master D) Switch to Interface (DDSTI)** 000: Interface 3 (SMCLK3/SMDAT3) 001: Interface 0 (SMCLK0/SMDAT0) 010: Interface 1 (SMCLK1/SMDAT1) 011: Interface 2 (SMCLK2/SMDAT2) 100: Interface 3 (SMCLK3/SMDAT3) 101: Interface 4 (SMCLK4/SMDAT4) 110: Interface 5 (SMCLK4/SMDAT5) Others: Reserved
3	-	0b	**Reserved**
2-0	R/W	000b	**Design C (Master C and Slave C) Switch to Interface (DCSTI)** 000: Interface 2 (SMCLK2/SMDAT2) 001: Interface 0 (SMCLK0/SMDAT0) 010: Interface 1 (SMCLK1/SMDAT1) 011: Interface 2 (SMCLK2/SMDAT2) 100: Interface 3 (SMCLK3/SMDAT3) 101: Interface 4 (SMCLK4/SMDAT4) 110: Interface 5 (SMCLK4/SMDAT5) Others: Reserved

7.7.4.47 Slave B Dedicated FIFO Pre-defined Control Register (SBDFPCTL)

Address Offset: 62h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	1b	**Hardware Slave B (For Pre-defined) Follow Mode Enable (HSBPFME)** 1: Enable 0: Disable
2	R	0b	**Slave B Bridge Busy Status (SBBBS)** 0: Not busy. 1: Busy.
1	R/W	1b	**Hardware Slave B (For Pre-defined) Enable (HSBPE)** 1: Enable 0: Disable
0	R/W	0b	**Slave B Dedicated FIFO Enable (SBDFE)** 1: Enable 0: Disable

7.7.4.48 Slave B Dedicated FIFO Status (SBDFFSTA)

Address Offset: 63h

Bit	R/W	Default	Description
7	R	1b	**FIFO Empty**
6	R	0b	**FIFO Full**
5	-	-	**Reserved**
4-0	R	0h	**Dedicated FIFO Byte Count**

7.7.4.49 Slave C Dedicated FIFO Control Register (SCDFFCTL)

Address Offset: 64h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Slave C Dedicated FIFO Enable (SCDFE)** 1: Enable 0: Disable

7.7.4.50 Slave C Dedicated FIFO Status (SCDFFSTA)

Address Offset: 65h

Bit	R/W	Default	Description
7	R	1b	**FIFO Empty**
6	R	0b	**FIFO Full**
5	-	-	**Reserved**
4-0	R	0h	**Dedicated FIFO Byte Count**

7.7.4.51 I2C Wr to Rd FIFO Register (I2CW2RF)

Address Offset: 69h

Bit	R/W	Default	Description
7	R/W	0b	**Master A I2C Wr->Rd FIFO Function (MAIF)** 1: Enable 0: Disable
6	R/W	0b	**Master BCDEF I2C Wr->Rd FIFO Function (MBCDEFIF)** 1: Enable 0: Disable
5-4	-	-	**Reserved**
3	R/W	0b	**Master D I2C Wr->Rd FIFO Interrupt (MDIFI)** 1: Enable 0: Disable
2	R/W	0b	**Master C I2C Wr->Rd FIFO Interrupt (MCIFI)** 1: Enable 0: Disable
1	R/W	0b	**Master B I2C Wr->Rd FIFO Interrupt (MBIFI)** 1: Enable 0: Disable
0	R/W	0b	**Master A I2C Wr->Rd FIFO Interrupt (MAIFI)** 1: Enable 0: Disable

7.7.4.52 I2C Wr to Rd FIFO Interrupt Status (IWRFISTA)

Address Offset: 6Ah

Bit	R/W	Default	Description
7	R/W	0b	**Master F I2C Wr->Rd FIFO Interrupt (MFIFI)** 1: Enable 0: Disable
6	R/W	0b	**Master E I2C Wr->Rd FIFO Interrupt (MEIFI)** 1: Enable 0: Disable
5	R/WC	0b	**Master F I2C Wr->Rd FIFO Interrupt Detected (MFIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt detected for Master F
4	R/WC	0b	**Master E I2C Wr->Rd FIFO Interrupt Detected (MEIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt detected for Master E
3	R/WC	0b	**Master D I2C Wr->Rd FIFO Interrupt Detected (MDIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt detected for Master D
2	R/WC	0b	**Master C I2C Wr->Rd FIFO Interrupt Detected (MCIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt detected for Master C
1	R/WC	0b	**Master B I2C Wr->Rd FIFO Interrupt Detected (MBIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt detected for Master B
0	R/WC	0b	**Master A I2C Wr->Rd FIFO Interrupt Detected (MAIFID)** 0: Cleared by writing a 1 to this bit. 1: I2C Wr->Rd FIFO Interrupt detected for Master A

7.7.4.53 Shared FIFO Function Enable (SFFE)

Address Offset: 6Fh

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Shared FIFO For Slave C Enable (SFSCE)** 1: Enable 0: Disable
5	R/W	0b	**Shared FIFO For Slave B Enable (SFSBE)** 1: Enable 0: Disable
4	R/W	0b	**Shared FIFO For Slave A Enable (SFSAE)** 1: Enable 0: Disable
3-2	-	-	**Reserved**
1	R/W	0b	**Shared FIFO For Master B, C, D, E, F Enable (SFMBCDEFE)** 1: Enable 0: Disable
0	R/W	0b	**Shared FIFO For Master A Enable (SFMAE)** 1: Enable 0: Disable

Note: The set size value of the shared FIFO needs to be larger than the size of the transferred data.

Figure 7-15. Shared FIFO Control

Shared FIFO is mapping to EC external data memory space (4k)
Shared FIFO Related Control Registers includes:
SFFE : Shared FIFO Enable Control
MSFSS : Master Shared FIFO Size Select
SSFSS1,SSFSS2 : Slave Shared FIFO Size
SFBAMA, SFBAMBCD : Master Shared FIFO Base Address
SFBASA,SFBASB,SFBASC : Slave Shared FIFO Base Address

User can using above registers to control each one shared fifo base address and size.

4k SRAM

7.7.4.54 Master Shared FIFO Size Select (MSFSS)

Address Offset: 76h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	000b	**Shared FIFO Size For Master B, C, D, E, F (SFSFMBCDEF)** 000: 32 bytes. 010: 32 bytes. 011: 64 bytes. 100: 128 bytes. 101: 256 bytes.
3	-	-	**Reserved**
2-0	R/W	000b	**Shared FIFO Size For Master A (SFSFMA)** 000: 32 bytes. 010: 32 bytes. 011: 64 bytes. 100: 128 bytes. 101: 256 bytes

7.7.4.55 Slave Shared FIFO Size Select1 (SSFSS1)

Address Offset: 77h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	000b	**Shared FIFO Size For Slave B (SFSFSB)** 000: 16 bytes. 001: 16 bytes. 010: 32 bytes. 011: 64 bytes. 100: 128 bytes. 101: 256 bytes.
3	-	-	**Reserved**
2-0	R/W	000b	**Shared FIFO Size For Slave A (SFSFSA)** 000: 16 bytes. 001: 16 bytes. 010: 32 bytes. 011: 64 bytes. 100: 128 bytes. 101: 256 bytes.

7.7.4.56 Shared FIFO Base Address for Master A (SFBAMA)

Address Offset: 78h

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared FIFO Base Address Bits[11:4] For Master A (SFBABMA[11:4])** Define Shared FIFO Base address Bits[11:4].

7.7.4.57 Shared FIFO Base Address for Master BCD (SFBAMBCD)

Address Offset: 7Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared FIFO Base Address Bits[11:4] For Master BCDEF (SFBABMBCDEF[11:4])** Define Shared FIFO Base address Bits[11:4].

7.7.4.58 Shared FIFO Base Address for Slave A (SFBASA)

Address Offset: 80h

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared FIFO Base Address Bits[11:4] For Slave A (SFBABSA[11:4])** Define Shared FIFO Base address Bits[11:4].

7.7.4.59 Shared FIFO Base Address for Slave B (SFBASB)

Address Offset: 82h

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared FIFO Base Address Bits[11:4] For Slave B (SFBABSB[11:4])** Define Sharde FIFO Base address Bits[11:4].

7.7.4.60 Shared FIFO Base Address for Slave C (SFBASC)

Address Offset: 84h

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared FIFO Base Address Bits[11:4] For Slave C (SFBABSC[11:4])** Define Shared FIFO Base address Bits[11:4].

7.7.4.61 Slave Shared FIFO Size Select2 (SSFSS2)

Address Offset: 87h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/W	000b	**Shared FIFO Size For Slave C (SFSFSC)** 000: 16 bytes. 001: 16 bytes. 010: 32 bytes. 011: 64 bytes. 100: 128 bytes. 101: 256 bytes.

7.7.4.62 Hardwired PEC Register (HWPEC)

Address Offset: 88h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Slave C Hardwired PEC Function (SCHPF)** 1: Enable 0: Disable
5	R/W	0b	**Slave B Hardwired PEC Function (SBHPF)** 1: Enable 0: Disable
4	R/W	0b	**Slave A Hardwired PEC Function (SAHPF)** 1: Enable 0: Disable
3	R/W	0b	**Master D Hardwired PEC Function (MDHPF)** 1: Enable 0: Disable
2	R/W	0b	**Master C Hardwired PEC Function (MCHPF)** 1: Enable 0: Disable
1	R/W	0b	**Master B Hardwired PEC Function (MBHPF)** 1: Enable 0: Disable
0	R/W	0b	**Master A Hardwired PEC Function (MAHPF)** 1: Enable 0: Disable

Note: PEC function is not supported if FIFO mode is used.

7.7.4.63 Hardwired PEC Error Status (HWPES)

Address Offset: 89h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/WC	0b	**Slave C Hardwired PEC Check Error (SCHPCE)** 1: PEC Check Error 0: PEC Check Normal
5	R/WC	0b	**Slave B Hardwired PEC Check Error (SBHPCE)** 1: PEC Check Error 0: PEC Check Normal
4	R/WC	0b	**Slave A Hardwired PEC Check Error (SAHPCE)** 1: PEC Check Error 0: PEC Check Normal
3	R/WC	0b	**Master D Hardwired PEC Check Error (MDHPCE)** 1: PEC Check Error 0: PEC Check Normal
2	R/WC	0b	**Master C Hardwired PEC Check Error (MCHPCE)** 1: PEC Check Error 0: PEC Check Normal
1	R/WC	0b	**Master B Hardwired PEC Check Error (MBHPCE)** 1: PEC Check Error 0: PEC Check Normal

Bit	R/W	Default	Description
0	R/WC	0b	**Master A Hardwired PEC Check Error (MAHPCE)** 1: PEC Check Error 0: PEC Check Normal

Note 1:
After the master transmits a cycle, the PEC field will be automatically filled.
After the master receives a cycle, hardware will notify whether the PEC field is corrupted or not by the HWPES register.
Note 2:
The slave transmitting a cycle should judge which field is the PEC field and read data from the SHWPECV register while write data to the SLDA register to transmit it. Ths slave receiving a cycle should judge which field is the PEC field and read data from the SHWPECV register and SLDA register to compare them.

7.7.4.64 Slave Transaction PEC Control Register (SLVTPECC)

Address Offset: 8Ah

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Slave C Transaction Contains PEC (SLVCTCP)** 1: Enable 0: Disable
1	R/W	0b	**Slave B Transaction Contains PEC (SLVBTCP)** 1: Enable 0: Disable
0	R/W	0b	**Slave A Transaction Contains PEC (SLVATCP)** 1: Enable 0: Disable

7.7.4.65 Slave Hardwired PEC VALUE (SHWPECV)

Address Offset: 8Bh/8Ch/8Dh for Design A/B/C respectively

Bit	R/W	Default	Description
7-0	R	0h	**Slave Hardware PEC Value (SHPV)** Display Slave Hardware PEC Value

7.7.4.66 Bridge Timeout Interrupt Enable Register (BTOIER)

Address Offset: 8Eh

Bit	R/W	Default	Description
7	R/W	0b	**Master D Bridge Timeout Interrupt Enable (MDBTOIE)** 1: Enable 0: Disable
6	R/W	0b	**Slave B Bridge Timeout Interrupt Enable (SBBTOIE)** 1: Enable 0: Disable
5	R/W	0b	**Master C Bridge Timeout Interrupt Enable (MCBTOIE)** 1: Enable 0: Disable
4	R/W	0b	**Slave A Bridge Timeout Interrupt Enable (SABTOIE)** 1: Enable 0: Disable

Bit	R/W	Default	Description
3	R/WC	0b	**Master D Bridge Timeout Status (MDBTOS)** 1: The bridge timeout status occurs. 0: Cleared by writing a 1 to this bit.
2	R/WC	0b	**Slave B Bridge Timeout Status (SBBTOS)** 1: The bridge timeout status occurs. 0: Cleared by writing a 1 to this bit.
1	R/WC	0b	**Master C Bridge Timeout Status (MCBTOS)** 1: The bridge timeout status occurs. 0: Cleared by writing a 1 to this bit.
0	R/WC	0b	**Slave A Bridge Timeout Status (SABTOS)** 1: The bridge timeout status occurs. 0: Cleared by writing a 1 to this bit.

7.7.4.67 I2C Shared FIFO Byte Count H (ISFBCH)

Address Offset: 90h/91h/92h/93h/A5h/B5h for Design A/B/C/D/E/F respectively

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-0	R/W	00h	**I2C FIFO Byte Count Bit[14:8] (IFBCB)** I2C FIFO byte count value [14:8]. The IFBCH and D0REG define the I2C FIFO byte count value [14:0]. Note: the I2C FIFO byte count value is 100h for share FIFO and up to 4000h for dedicated FIFO.

7.7.4.68 SMBus Interface Switch Pin Control (SISPC)

Address Offset: 73h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	W	0b	**SMBus Interface 5 Switch Control (SMBIF5SC)** Enabling this bit will swap the clock and data pin of SMBus interface 5. 1b: Enable 0b: Disable
4	W	0b	**SMBus Interface 4 Switch Control (SMBIF4SC)** Enabling this bit will swap the clock and data pin of SMBus interface 4. 1b: Enable 0b: Disable
3	W	0b	**SMBus Interface 3 Switch Control (SMBIF3SC)** Enabling this bit will swap the clock and data pin of SMBus interface 3. 1b: Enable 0b: Disable
2	W	0b	**SMBus Interface 2 Switch Control (SMBIF2SC)** Enabling this bit will swap the clock and data pin of SMBus interface 2. 1b: Enable 0b: Disable
1	W	0b	**SMBus Interface 1 Switch Control (SMBIF1SC)** Enabling this bit will swap the clock and data pin of SMBus interface 1. 1b: Enable 0b: Disable
0	W	0b	**SMBus Interface 0 Switch Control (SMBIF0SC)** Enabling this bit will swap the clock and data pin of SMBus interface 0. 1b: Enable 0b: Disable

7.7.4.69 SMBus Design Switch Interface Control 3(SDSIC3)

Address Offset: 99h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	000b	**Design F Switch to Interface (DFSTI)** 000b: Interface 5 (Default) 001b: Interface 0 010b: Interface 1 011b: Interface 2 100b: Interface 3 101b: Interface 4 110b: Interface 5 Others: Reserved
3	-	-	**Reserved**
2-0	R/W	000b	**Design E Switch to Interface (DESTI)** 000b: Interface 4 (Default) 001b: Interface 0 010b: Interface 1 011b: Interface 2 100b: Interface 3 101b: Interface 4 110b: Interface 5 Others: Reserved

7.7.4.70 Master Dedicated FIFO Threshold Enable 2 (MFTHEN2)

Address Offset: 9Ch

Bit	R/W	Default	Description
7	R/W	0b	**Master E Receive Data Available Function (MERDA)** 0: Disable 1: Enable
6	R/W	0b	**Master F Receive Data Available Function (MFRDA)** 0: Disable 1: Enable
5-4	-	-	**Reserved**
3	R/W	0b	**Master E Transmitter Data Available Function (METDA)** 0: Disable 1: Enable
2	R/W	0b	**Master F Transmitter Data Available Function (MFTDA)** 0: Disable 1: Enable
1-0	-	-	**Reserved**

7.7.4.71 Master Dedicated FIFO Threshold Interrupt Status 2 (MFTISTA2)

Address Offset: 9Dh

Bit	R/W	Default	Description
7	W/RC	0b	**Master E RX Interrupt Detected (MERID)** 0: Cleared by writing a 1 to this bit. 1: Master E Receive Data Available Interrupt is detected.
6	W/RC	0b	**Master F RX Interrupt Detected (MFRID)** 0: Cleared by writing a 1 to this bit. 1: Master F Receive Data Available Interrupt is detected.
5-4	-	-	**Reserved**
3	W/RC	0b	**Master E TX Interrupt Detected (METID)** 0: Cleared by writing a 1 to this bit. 1: Master E Transmitter Data Available Interrupt is detected.
2	W/RC	0b	**Master F TX Interrupt Detected (MFTID)** 0: Cleared by writing a 1 to this bit. 1: Master F Transmitter Data Available Interrupt is detected.
1-0	-	-	**Reserved**

7.7.4.72 Hardwired PEC Register 2 (HWPEC2)

Address Offset: 9Eh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	-	-	**Master F Hardwired PEC Function (MFHPF)** 1: Enable 0: Disable
0	-	-	**Master E Hardwired PEC Function (MEHPF)** 1: Enable 0: Disable

Note: PEC Function is not supported when using FIFO mode.

7.7.4.73 Hardwired PEC Error Status 2 (HWPES2)

Address Offset: 9Fh

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
1	-	-	**Master F Hardwired PEC Check Error (MFHPCE)** 1: PEC check error 0: PEC check normal
0	-	-	**Master E Hardwired PEC Check Error (MEHPCE)** 1: PEC check error 0: PEC check normal

7.7.4.74 SMCLK Timing Setting Register E (SCLKTS_E)

Address Offset: ABh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 7-12 on page 310 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	0b	**SMCLK 1MHz Setting (SCLKE1M)** 0b: Disable 1b: 1MHz Design E.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to decide which SMCLK rate is for the design E. If they are disabled, the SMCLK rate will depend on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.7.4.75 SMCLK Timing Setting Register F (SCLKTS_F)

Address Offset: BBh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Fix Repeat Start Setup Time (FRSST)** 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 7-12 on page 310 for Repeat Start period (A).
3	-	-	**Reserved**
2	R/W	0b	**SMCLK 1MHz Setting (SCLKF1M)** 0b: Disable 1b: 1MHz Design F.
1-0	R/W	00b	**SMCLK Setting (SCLKS)** These bits are to decide which SMCLK rate is for the design F. If they are disabled, the SMCLK rate will depend on the setting of original timing registers. 00b: Disable 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

7.8 Platform Environment Control Interface (PECI)

7.8.1 Overview

The Platform Environment Control Interface (PECI) can maintain bi-directional communication with external devices through the PECI pin. It is compatible with the PECI 2.0/3.0/3.1 specification.

7.8.2 Features

- Supports both Host and EC side.
- Supports PECI 2.0/3.0/3.1
- Supports 16-byte write/read length
- Supports FCS checking mechanism
- Supports AW_FCS hardwired mechanism
- Supports adjustable V_{TT} level

7.8.3 Functional Description

The PECI module can maintain bi-directional communication with PECI devices (e.g. Intel processor). The PECI host controller supports all command protocols as listed in the PECI 2.0/3.0/3.1 specification, including Ping(), GetDIB(), GetTemp() and so on. In addition, it supports FCS checking mechanism and PECI Assured Write Message as well.

7.8.3.1 PECI Porting Guide

The PECI host controller requires that target address, write length, read length, command, and write data be setup for various commands to be sent out. Based on the PECI 2.0/3.0/3.1 specification, software must setup data and command (as mentioned above) before START. When the START bit in the Host Control Register is set, the PECI host controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing a new command.

Here are the steps the software shall follow to program the registers for various commands.

(1). After system resets, switch the related GPIO to the PECI function mode, and then enable the PECI Host Controller (the PECIHEN bit in Host Control Register is set to 1).
(2). Depending on the desired command, software shall write data to the Host Target Address Register, Host Write Length Register, Host Read Length Register, Host Command Register, and Host Write Data Register.
(3). Start the transaction (Write 09h to the Host Control Register, which will enable the PECI Host, and start the transaction).
(4). During the transaction, software shall read the Host Status Register to check whether the transaction is being performed or not (the Host Busy bit in the Host Status Register will be set during the transaction).
(5). For the polling mode, software continues reading the Host Status Register to check whether the transaction is completed or not (the Finish bit in the Host Status Register will be set when the transaction is completed). For the interrupt mode, the Host Status Register will be available after data-valid event occurs resulting from PECI interrupt.
(6). When the transaction is completed, software can read the Host Read Data Register to get the received data if necessary.
(7). If the programmer requires that hardware support the AW_FCS calculation in the commands supporting the Assured Write Message during the transaction, the AWFCS_EN or AWFCS_FRC_CTRL bit in the Host Control Register shall be set before START.

7.8.3.2 PECI Programming Guide

Figure 7-16. Program Flow Chart for Polling Mode

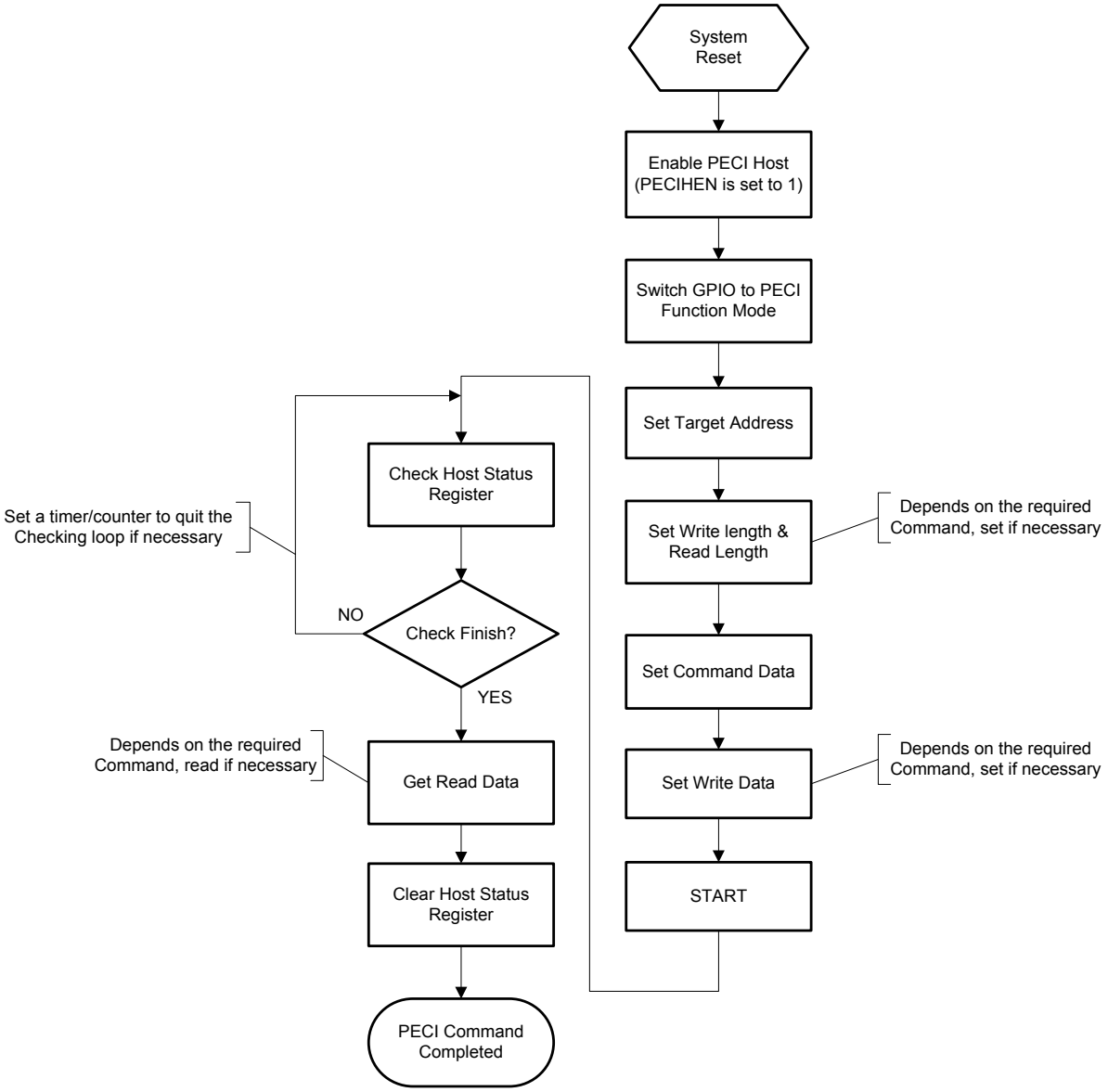
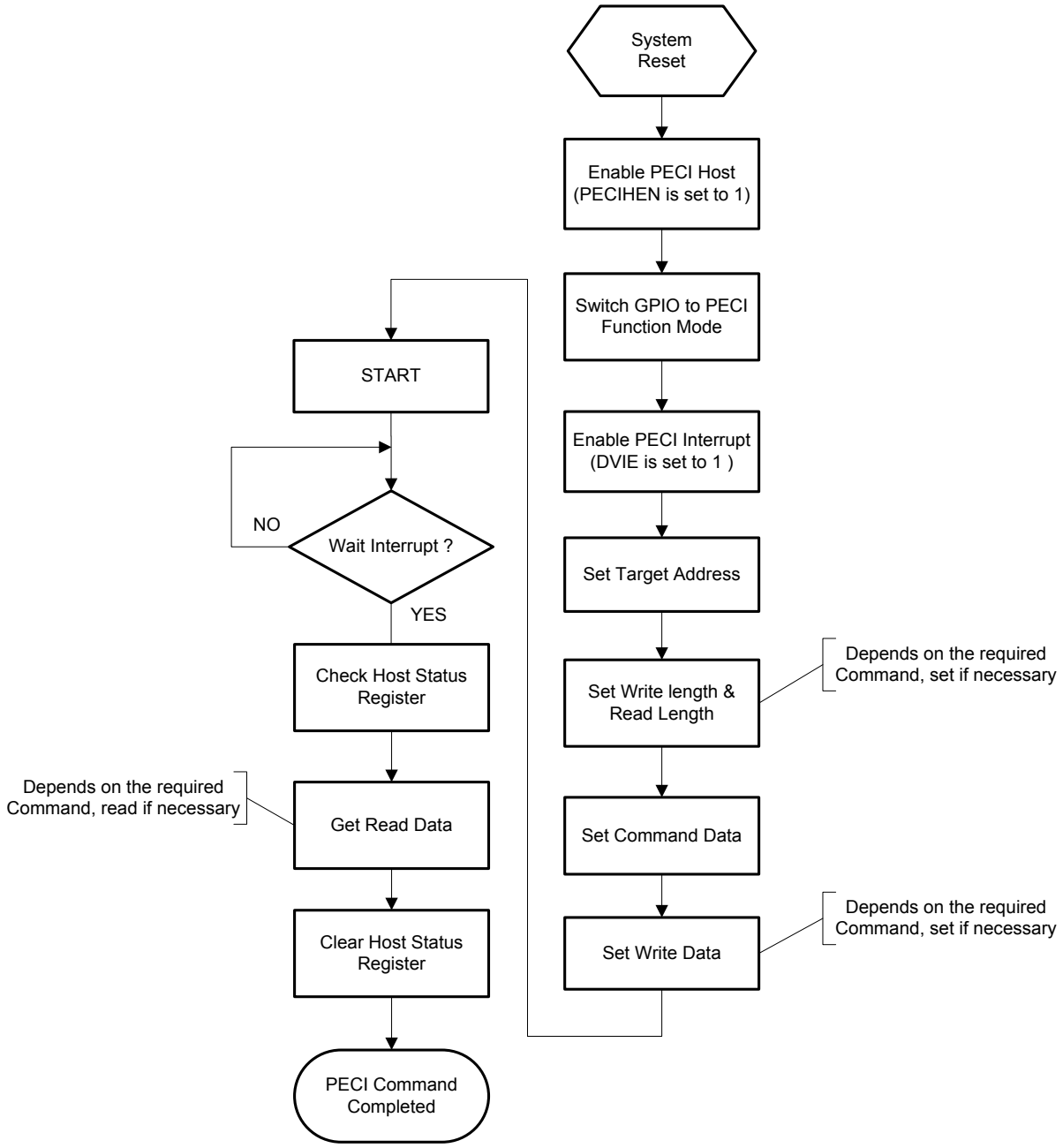


Figure 7-17. Program Flow Chart for Interrupt Mode



7.8.4 Host Interface Registers

The registers of PECI can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The PECI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-14. Host View Register Map, PECI

7 0		Offset
Host Status Register (HOSTAR)		00h
Host Control Register (HOCTLR)	HHRAE = 0	01h
Host Command Register (HOCMDR)		02h
Host Target Address Register (HOTRADDR)		03h
Host Write Length Register (HOWRLR)		04h
Host Read Length Register (HORDLR)		05h
Host Write Data Register (HOWRDR)		06h
Host Read Data Register (HORDDR)		07h
Host Control 2 Register (HOCTL2R)	HHRAE = 1	01h
Pad Control Register (PADCTLR)	HHRAE = 1	07h
Received Write FCS Value (RWFCSV)	HHRAE = 1	02h
Received Read FCS Value (RRFCSV)	HHRAE = 1	03h
Write FCS Value (WFCSV)	HHRAE = 1	04h
Read FCS Value (RFCSV)	HHRAE = 1	05h
Assured Write FCS Value (AWFCSV)	HHRAE = 1	06h

All registers are double mapped into the host and EC side; however, the PECI function should be controlled by a side only.

The definition of all registers are the same as their identical register names in the EC side except HHRAE (Host Side High Range Address Enable) bit. HHRAE bit is located in bit 7 in the registers with offset 01h (HOCTLR or HOCTL2R). HHRAE bit is used to select different registers if they have the same offset number.

7.8.5 EC Interface Registers

The register map of EC interface is listed below. The base address for PECI is 3000h.

Table 7-15. EC View Register Map, PECI

7 0	Offset
Host Status Register (HOSTAR)	00h
Host Control Register (HOCTLR)	01h
Host Command Register (HOCMDR)	02h
Host Target Address Register (HOTRADDR)	03h
Host Write Length Register (HOWRLR)	04h
Host Read Length Register (HORDLR)	05h
Host Write Data Register (HOWRDR)	06h
Host Read Data Register (HORDDR)	07h
Host Control 2 Register (HOCTL2R)	08h
Pad Control Register (PADCTLR)	0Eh
Received Write FCS Value (RWFCSV)	09h
Received Read FCS Value (RRFCSV)	0Ah
Write FCS Value (WFCSV)	0Bh
Read FCS Value (RFCSV)	0Ch
Assured Write FCS Value (AWFCSV)	0Dh

Other related register(s):
- General Control 2 Register (GCR2), PECIE bit
-
- General Control 3 Register (GCR3), PECIPDG bit

7.8.5.1 Host Status Register (HOSTAR)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the status of the command.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/WC	0b	**PECI GetTemp() Command Receive Error Code (RCV_ERRCODE)** This bit reports the status of receiving the error code (8000h ~ 81FFh). 0: No error. 1: The error code in the GetTemp() command is received.
6	R/WC	0b	**PECI Bus Abnormal/Contention Error (BUSERR)** This bit reports the PECI line status. 0: No error. 1: Abnormal/Contention error occurs.
5	R/WC	0b	**PECI Slave Message Phase t-bit Extend over Error (EXTERR)** This bit reports the PECI line status. 0: No error 1: T-bit extend over error occurs.
4	-	0b	**Reserved**
3	R/WC	0b	**Write_FCS Error (WR_FCS_ERR)** This bit reports if the write FCS error occurs in the communication or not. 0: No error. 1: Write_FCS error occurs.
2	R/WC	0b	**Read_FCS Error (RD_FCS_ERR)** This bit reports if the read FCS error occurs in the communication or not. 0: No error. 1: Read_FCS error occurs.
1	R/WC	0b	**Finish (FINISH)** 0: This bit is cleared by writing 1 to this position. 1: The bit is set by termination of a command.
0	R	0b	**Host Busy (HOBY)** 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

7.8.5.2 Host Control Register (HOCTLR)

Address Offset: Host: 01h (HHRAE = 0) / EC: 01h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side High Range Address Enable (HHRAE)** This bit is only available in host side. 0: Host Side High Range Address is disabled. 1: Host Side High Range Address is enabled.
6	R/W	0b	**AW_FCS Force Control (AWFCS_FRC_CTRL)** This bit forces the AW_FCS hardwired mechanism no matter what PECI command (except the Ping() command) is issued. When this bit is set, the hardware will handle the calculation of AW_FCS. The programmer should set this bit based on the command to be issued. This bit will be cleared when the command is finished or aborted. 0: Disable 1: Enable
5	W	0b	**Data FIFO Pointer Clear (FIFOCLR)** Writing a 1 to this bit clears the Write/Read Data FIFO pointers. 0: No action; it always returns 0 when reading it. 1: Both Write and Read Data FIFO pointers will be cleared. Write Data pointer will point to Write Data 2, and Read Data pointer will point to Read Data 1.
4	R/W	0b	**PECI Host Auto-abort at FCS_Error (FCSERR_ABT)** This bit enables the PECI host to abort the transaction when FCS error occurs. 0: Disable 1: Enable
3	R/W	0b	**PECI Host Enable (PECIHEN)** This bit enables the PECI host controller. 0: Disable 1: Enable
2	R/W	0b	**PECI Contention Control (CONCTRL)** This bit enables the contention mechanism of the PECI bus. When this bit is set, the host will abort the transaction if the PECI bus is contentious. 0: Disable 1: Enable
1	R/W	0b	**Assured Write FCS Enable (AWFCS_EN)** This bit enables the AW_FCS hardwired mechanism based on the PECI command. This bit is functional only when the AW_FCS supported command of PECI 2.0/3.0/3.1 is issued. When this bit is set, the hardware will handle the calculation of AW_FCS. 0: Disable 1: Enable
0	W	0b	**Start (START)** This bit is write-only. Writing a 1 to it during the NOT Host Busy state will start a transaction. Writing a 1 to it during the Host Busy state will not issue any transaction. So, the programmer should check the Host Busy state before issuing a transaction. 0: This bit always returns 0 on reads. 1: When this bit is set, the PECI host controller will perform the desired transaction.

7.8.5.3 Host Command (Write Data 1) Register (HOCMDR)

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Command Register (HCMD[7:0])** This register is the command field of the PECI protocol. In the PECI protocol, it is the command (Write Data 1) byte. If the host controller is busy, the programmer should not change the value of this register, or the PECI host controller will send the wrong command. If the value of the register is out of definition, the host will transfer it as the normal value and no error will be detected by the PECI host controller.

7.8.5.4 Host Target Address Register (HOTRADDR)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Target Address (HAddr[7:0])** This register is the Target Address field of the PECI protocol.

7.8.5.5 Host Write Length Register (HOWRLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Write Length Register (HW_Length[7:0])** This register is the Write Length field of the PECI protocol.

7.8.5.6 Host Read Length Register (HORDLR)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Read Length Register (HR_Length[7:0])** This register is the Read Length field of the PECI protocol.

7.8.5.7 Host Write Data (2-16) Register (HOWRDR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**Write Data (2-16) (WR_DAT[7:0])** These are 15-byte FIFO registers, which are the Write Data field of the PECI protocol.

7.8.5.8 Host Read Data (1-16) Register (HORDDR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	00h	**Read Data (1-16) (RD_DAT[7:0])** These are 16-byte FIFO registers, which are the Read Data field of the PECI protocol.

7.8.5.9 Host Control 2 Register (HOCTL2R)

Address Offset: Host: 01h (HHRAE = 1) / EC: 08h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side High Range Address Enable (HHRAE)** This bit is only available in host side. 0: Host Side High Range Address is disabled. 1: Host Side High Range Address is enabled.
6-3	-	-	**Reserved**
2-0	R/W	000b	**Host Optimal Transfer Rate Setting (HOPTTRS)** These bits are used to set PECI host's optimal transfer rate. 000b: 1.8MHz. 001b: 1MHz. 100b: 1.5MHz. Otherwise: Reserved.

7.8.5.10 Pad Control Register (PADCTLR)

Address Offset: Host: 07h (HHRAE = 1) / EC: 0Eh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Data Valid Interrupt Enable (DVIE)** This register is to enable the PECI interrupt generated by the Data Valid event from PECI. This bit is only available in EC side. 0: Disable (default). 1: Enable
1-0	R/W	00b	**Host V_{TT} Setting (HOVTTS)** These bits are used to set PECI V_{TT} level. 00b: 1.10V. 01b: 1.05V. 10b: 1.00V. 11b: 0.90V.

7.8.5.11 Received Write FCS Value (RWFCSV)

Address Offset: Host: 02h (HHRAE = 1) / EC: 09h

Bit	R/W	Default	Description
7-0	R	00b	**Received Write FCS Value (RWFCSV)** RWFCSV is used in storing the Write FCS generated by the PECI client. A new received Write FSC will automatically update this field.

7.8.5.12 Received Read FCS Value (RRFCSV)

Address Offset: Host: 03h (HHRAE = 1) / EC: 0Ah

Bit	R/W	Default	Description
7-0	R	00b	**Received Read FCS Value (RRFCSV)** RRFCSV is used in storing the Read FCS generated by the PECI client. A new received Read FSC will automatically update this field.

7.8.5.13 Write FCS Value (WFCSV)

Address Offset: Host: 04h (HHRAE = 1) / EC: 0Bh

Bit	R/W	Default	Description
7-0	R	00b	**Write FCS Value (WFCSV)** WFCSV is used in storing the Write FCS generated by EC. This field will be automatically updated while WRFCSV is updated.

7.8.5.14 Read FCS Value (RFCSV)

Address Offset: Host: 05h (HHRAE = 1) / EC: 0Ch

Bit	R/W	Default	Description
7-0	R	00b	**Read FCS Value (RFCSV)** RFCSV is used in storing the Read FCS generated by EC. This field will be automatically updated while RRFCSV is updated.

7.8.5.15 Assured Write FCS Value (AWFCSV)

Address Offset: Host: 06h (HHRAE = 1) / EC: 0Dh

Bit	R/W	Default	Description
7-0	R	00b	**Assured Write FCS Value (AWFCSV)** AWFCSV is used in storing the Assured Write FCS generated by EC. This field will be automatically updated while WRFCSV is updated.

7.9 PS/2 Interface

7.9.1 Overview

The PS/2 device uses a two-wire bi-directional interface for data transmission. The device consists of three identical channels. Each of the three channels provides two signals (CLK and DATA line) to communicate with the auxiliary device. The PS/2 interface also connects the CLK line and DATA line to the WUC (WU10-WU17) to wake-up the CPU when these lines are toggled.

CLK line and DATA line are the same as PS2CLKn and PS2DATn (n=0, 1 or 2) pins. Refer to Table 5-9 on page 15 for the details.

7.9.2 Features

- Supports three PS/2 channels.
- Supports hardware/software mode selection.
- Three interrupt features are available: Start Interrupt, Transaction Done Interrupt, and Software Mode Interrupt (INT18, INT19 and INT20).

7.9.3 Functional Description

The PS/2 Interface has two operation methods: Hardware mode and software mode. When the hardware mode is enabled, the PS/2 interface can perform automatic reception or transmission depending on the TRMS bit in the PSCTLn register. When the hardware mode is disabled (software mode is enabled), the PS/2 CLK line and DATA line are controlled by the firmware via the CCLK bit and CDAT bit in the PSCTLn register. The following sections will describe how to use the PS/2 interface.

7.9.3.1 Hardware Mode Selected

Receive Mode
Here are the steps the host shall follow to receive data from a PS/2 device.

1. Enable the hardware mode, select the receive mode, and release the CLK line and DATA line (Write 07h to the PS/2 Control Register).
2. Enable the interrupts. (TDIE bit in PS/2 Interrupt Control Register has to be set to 1 because when the data transmission is completed, the data in PS/2 Data Register needs to be read.)

After these steps, the PS/2 interface is ready to receive data. When the data transmission is completed, an interrupt signal is set high (Transaction Done interrupt). The status (Transaction Done Status) can be read from PS/2 Status Register and the received data can be read from the PS/2 Data Register. The PS/2 CLK line will be held low until the PS/2 Data Register is read.

Transmit Mode
Here are the steps the host shall follow to send data to a PS/2 device.
1. Enable the hardware mode, select the transmit mode, and pull the CLK line low and DATA line high (Write 0Dh to the PS/2 Control Register).
2. Enable the interrupts. (TDIE bit in PS/2 Interrupt Control Register has to be set to 1 because when the data transmission is completed, the data in PS/2 Status Register needs to be read.)
3. Write the data to be transmitted to the PS/2 Data Register.
4. Pull the DATA line low (Write 0Ch to the PS/2 Control Register).
5. Pull the CLK line high (Write 0Eh to the PS/2 Control Register).

After these steps, the PS/2 interface is ready to transmit data. When the data transmission is completed, an interrupt signal is set high (Transaction Done interrupt). The status (Transaction Done Status) can be read from PS/2 Status Register. The CLK line will be held low until the PS/2 Status Register is read.

Input Signal Debounce
This PS/2 Interface performs a debounce operation on the CLK input signal before determining its logical value. When this operation is enabled (DCEN bit in the PS/2 Control Register is set to 1), the CLK input signal has to be stable for at least 4 clock cycles.

7.9.3.2 Software Mode Selected

Software Control PS/2 CLK line and DATA line
When the Software Mode is selected (PSHE=0 in PS/2 Control Register), the software can control the PS/2 CLK line and DATA line. The CCLK bit and CDAT bit in the PS/2 Control Register control the CLK line and DATA line. When one of these bits is cleared, the relevant pin is held low. When one of these bits is set, the relevant pin is pulled high.

Software Control the Interrupt
When the PS/2 Hardware Enable bit is cleared (PSHE=0 in PS/2 Control Register) and the Software Mode Interrupt Enable bit is set (SMIE=1 in PS/2 Interrupt Control Register), the software can control the PS/2 interrupt. The interrupt is set high when the CCLK bit in PS/2 Control Register is set high. If such an interrupt is not desired, clear the Software Mode Interrupt Enable bit (SMIE=0 in PS/2 Interrupt Control Register).

7.9.4 EC Interface Registers

The PS/2 interface registers are listed below. The base address for PS/2 is 1700h.

Table 7-16. EC View Register Map, PS/2

7 — 0	Offset
PS/2 Control Register 1 (PSCTL1)	00h
PS/2 Control Register 2 (PSCTL2)	01h
PS/2 Control Register 3 (PSCTL3)	02h
PS/2 Interrupt Control Register 1 (PSINT1)	04h
PS/2 Interrupt Control Register 2(PSINT2)	05h
PS/2 Interrupt Control Register 3 (PSINT3)	06h
PS/2 Status Register 1 (PSSTS1)	08h
PS/2 Status Register 2 (PSSTS2)	09h
PS/2 Status Register 3 (PSSTS3)	0Ah
PS/2 Data Register 1 (PSDAT1)	0Ch
PS/2 Data Register 2 (PSDAT2)	0Dh
PS/2 Data Register 3 (PSDAT3)	0Eh

7.9.4.1 PS/2 Control Register 1-3 (PSCTL1-3)

This register controls the operation of the PS/2 interface. PS/2 Control Register 1-3 are for channel 1-3 respectively.

Address Offset: 00h, 01h, 02h

Bit	R/W	Default	Description
7-5	-	000b	**Reserved**
4	R/W	0b	**Debounce Circuit Enable (DCEN)** 0: The debounce circuit is disabled. 1: The debounce circuit is enabled.
3	R/W	0b	**Transmit / Receive Mode Selection (TRMS)** 0: Receive mode is selected. 1: Transmit mode is selected.
2	R/W	0b	**PS/2 Hardware Enable (PSHE)** When this bit is set to 1, the PS/2 channel can perform automatic reception or transmission. When this bit is 0, the channel's CLK and DATA lines are controlled by the CCLK and CDAT bits in this register. 0: PS/2 hardware mode is disabled (Software mode is enabled). 1: PS/2 hardware mode is enabled.
1	R/W	0b	**Control CLK Line (CCLK)** This bit can control the CLK line. 0: The CLK line is held low. 1: The CLK line is pulled high.
0	R/W	1b	**Control DATA Line (CDAT)** This bit can control the DATA line. 0: The DATA line is held low. 1: The DATA line is pulled high.

7.9.4.2 PS/2 Interrupt Control Register 1-3 (PSINT1-3)

This register enables or disables various interrupts sources. PS/2 Interrupt Control Register 1-3 are for channel 1-3 respectively.

Address Offset: 04h, 05h, 06h

Bit	R/W	Default	Description
7-4	-	00000b	**Reserved**
3	R/W	0b	**Timeout Interrupt Enable (TOIE)** Enable Timeout timer and the generation of an interrupt for timeout events to activate. Timeout events: (a) Request to send and wait over 15ms during transmission (b) Data transfer over 2ms during transmission and reception 0: Disable 1: Enable
2	R/W	0b	**Transaction Done Interrupt Enable (TDIE)** Enable or disable the interrupt generation when the Transaction Done status occurs. 0: Disable the interrupt. 1: Enable the interrupt.

Bit	R/W	Default	Description
1	R/W	0b	**Start Interrupt Enable (SIE)** Enable or disable the interrupt generation when the Start status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
0	R/W	0b	**Software Mode Interrupt Enable (SMIE)** Enable or disable the interrupt generation when the PS/2 hardware is disabled. The CCLK bit in PSCTLn register can control the interrupt output when this bit is set to 1 and PS/2 hardware is disabled. 0: Disable the interrupt. 1: Enable the interrupt.

7.9.4.3 PS/2 Status Register 1-3 (PSSTS1-3)

This register contains the status information on the data transfer on the PS/2. Status Register 1-3 are for channel 1-3 respectively.

Address Offset: 08h, 09h, 0Ah

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
6	R/WC	0b	**Timeout Error(TOER)** This bit is 1 when the timeout event occurs and cleared by write 1 to this bit.
5	R	0b	**Frame Error (FER)** This bit is 1 when the stop bit in a received frame was detected low.
4	R	0b	**Parity Error (PER)** This bit is 1 when a parity error condition occurs.
3	R	0b	**Transaction Done Status (TDS)** This bit is 1 when a PS/2 data transfer is done.
2	R	0b	**Start Status (SS)** This bit is 1 when a start bit is detected.
1	R	-	**CLK Line Status (CLS)** Reading this bit returns the current status of the PS/2 CLK line.
0	R	-	**DATA Line Status (DLS)** Reading this bit returns the current status of the PS/2 DATA line.

7.9.4.4 PS/2 Data Register 1-3 (PSDAT1-3)

In receive mode, this register holds the data received from the PS/2 device. In transmit mode, the data in this register is transmitted to the PS/2 device. Data Register 1-3 are for channel 1-3 respectively.

Address Offset: 0Ch, 0Dh, 0Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Data (DAT)** Holds the data received from the PS/2 device in the receive mode or the data which will be transmitted in the transmit mode.

7.10 Digital to Analog Converter (DAC)

7.10.1 Overview

The DAC interface is used as a communication interface between the embedded controller and DAC.

7.10.2 Feature

- Supports 4-channel D/A converter
- 8-bit resolution
- Independent enable signals for each channel
- Power-down function

7.10.3 Functional Description

The DAC interface has four channels. Each channel generates an output in the range of 0V to AVCC with eight-bit resolution. When a DAC channel is enabled, its output is defined by the value written to its DACDAT register. DACDAT 2-5 control channel 2-5 respectively. The 0V output is obtained for a value of 00h in the DACDAT register. The AVCC output is obtained for a value of FFh in the DACDAT register. In power-down mode (POWDNx=1 in DAC Power Down Register), the DAC output is 0V.

DAC analog circuit has less power consumption if it is power-down. POWDNx bit in DAC Power Down Register controls this and it's cleared during EC domain reset.

7.10.4 EC Interface Registers

The DAC interface registers are listed below. The base address for DAC is 1A00h.

Table 7-17. EC View Register Map, DAC

7	0	Offset
DAC Power Down Register (DACPDREG)		01h
DAC Data Channel 2 (DACDAT2)		04h
DAC Data Channel 3 (DACDAT3)		05h
DAC Data Channel 4 (DACDAT4)		06h
DAC Data Channel 5 (DACDAT5)		07h

7.10.4.1 DAC Power Down Register (DACPDREG)

When the bit in this register is set, the respective DAC channels will be power-down.

Address Offset: 01h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	1b	**DAC Channel 5 Power Down (POWDN5)** 0: The DAC channel 5 is not power-down. 1: The DAC channel 5 is power-down.
4	R/W	1b	**DAC Channel 4 Power Down (POWDN4)** 0: The DAC channel 4 is not power-down. 1: The DAC channel 4 is power-down.
3	R/W	1b	**DAC Channel 3 Power Down (POWDN3)** 0: The DAC channel 3 is not power-down. 1: The DAC channel 3 is power-down.
2	R/W	1b	**DAC Channel 2 Power Down (POWDN2)** 0: The DAC channel 2 is not power-down. 1: The DAC channel 2 is power-down.
1-0	-	-	**Reserved**

7.10.4.2 DAC Data Channel 2~5 Register (DACDAT2~5)

The data in these registers will be loaded into channel 2~5.

Address Offset: **Channel 2: 04h**
Channel 3: 05h
Channel 4: 06h
Channel 5: 07h

Bit	R/W	Default	Description
7-0	R/W	-	**DAC Data Register (DACDAT)** 8 bit data will be loaded to the DAC for D/A operation.

7.11 Analog to Digital Converter (ADC)

7.11.1 Overview

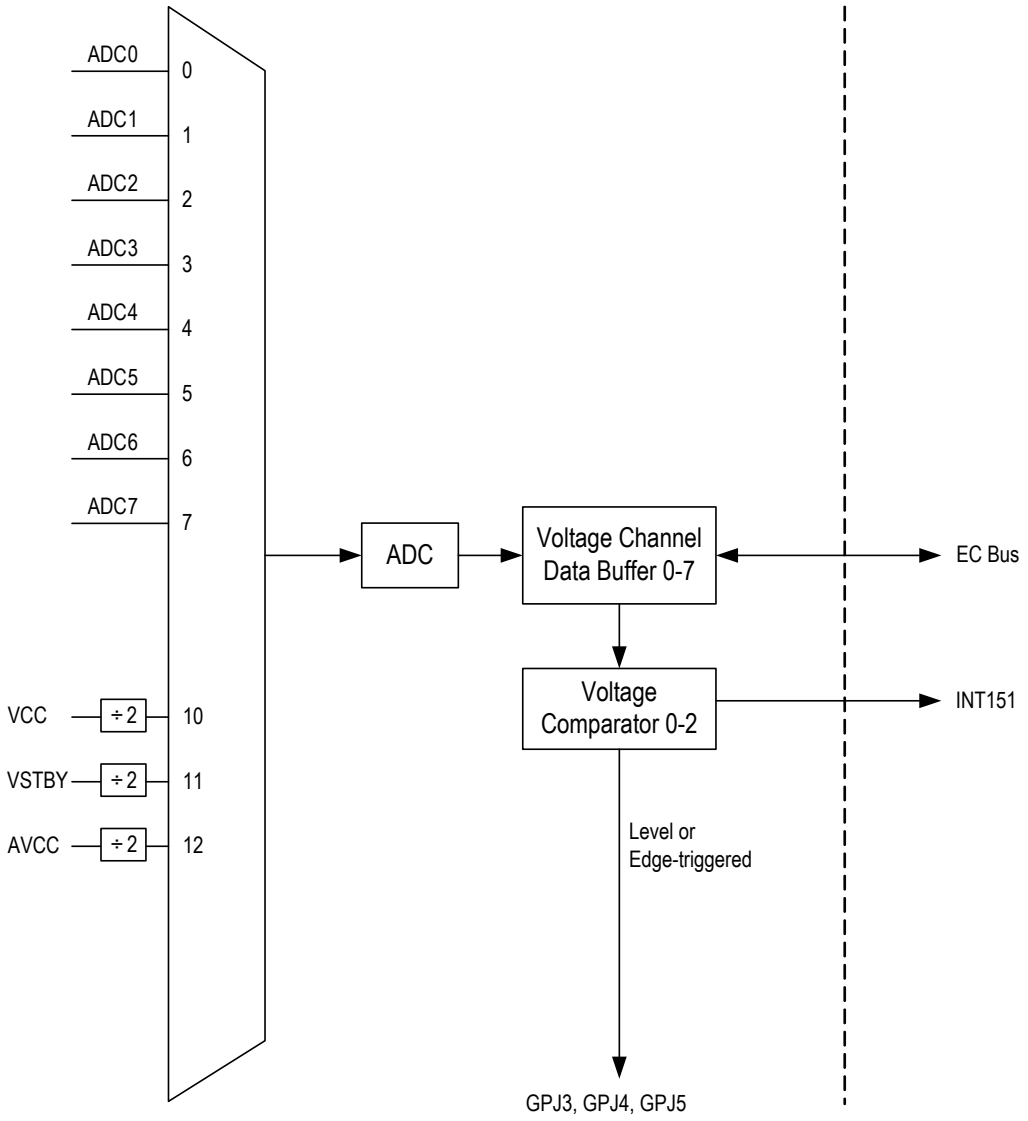
The ADC (analog to digital converter) provides an accurate method for measuring slow changing voltages. The module can measure the channel up to eleven-voltage with 10-bit resolution.

7.11.2 Features

- Supports 10-bit resolution and 0 to AVCC/1.1 or AVCC input voltage range
- Supports 8 voltage buffers
- Supports fast AD conversion of 11 channels
- Supports 3 voltage comparators, even EC in sleep mode.
- Polling or interrupt-driven interface

7.11.3 Functional Description

Figure 7-18. ADC Channels Control Diagram



7.11.3.1 ADC General Description

Inputs
The ADC has 11 inputs (ADC0-7, ADC10-12) divided into two groups described as the following:
• External Voltage (ADC0-7):
These are for DC voltage sources.

• Internal Voltage (ADC10-12):
These are connected to the internal supply voltages of the device (VCC, VSTBY and AVCC).
The input voltages of ADC10-12 are divided by 2 before being input to analog multiplexer.

A/D Converter
The high-resolution A/D converter receives the selected input with a 16 to 1 analog multiplier and converts it. The result of the conversion is a 10-bit unsigned integer.

ADC Cycle
The ADC has 8 output buffers, which are for the voltage channel. The buffer for voltage measurement channels holds the current data until the next same volt channel measurement is completed after one ADC cycle is finished. An ADC cycle includes measurements of all active channels. If all 8 channels are enabled, the first measurement is a voltage channel 0 and followed by voltage channel 1, 2, 3, … 7. After an A/D conversion is completed for a certain active channel, its related bit in the Data Valid (DATVAL bit in VCH0CTL - VCH7CTL) flag is set, which represents the channel of data is available and EC can read out.

Channel Conversion Time
The channel conversion time of ADC is listed bellow.

Table 7-18. ADC Channel Conversion Time

{ADCCTS1, ADCCTS0}	= 11b	= 01b	= 00b or 10b
Conversion Time (μs)	200*(SCLKDIV + 1)	103.2*(SCLKDIV + 1)	30.8*(SCLKDIV + 1)

Interrupt to INTC
ADC interrupt (INT8) will be active if end-of-cycle or voltage channel 0-7 data valid is true. See also INTECEN and INTDVEN.

The voltage comparator interrupt (INT151) will be active if the value stored in the selected voltage channel data buffer reaches the threshold level of the comparator.

7.11.3.2 Voltage Measurement and Automatic Hardware Calibration

The ADC converts the input voltage signal ranging from 0V to AVCC/1.1 or AVCC into a 10-bit unsigned integer. This 10-bit integer then will be stored in data buffer VCHiDATL and VCHiDATM.

Changing the input selection for a new measurement channel (voltage), the software needs to set a delay time to prevent the result of an unintended ADC operation. The ADC waits for a programmable delay time between the selection of the input to be measured and the beginning of the A/D conversion.

7.11.3.3 ADC Operation

Reset
The ADC is disabled, and all interrupt is masked and all event status bits reset. The selected input for all four-voltage channels is disabled (Bit4-0 of the VCHiCTL register is set to 0Fh).

Initializing the ADC
The ADC has to be initialized before ADC is enabled (ADCEN in the ADCCFG register is set to 1). The followings need to be done before the ADC is enabled.

1. Set AINITB@ADCSTS = 1 then clear it (only once after VSTBY power on)
2. Channel Select in VCHiCTL register
3. ADCEN bit in ADCCFG register is cleared.

Enabling the ADC
After the ADC is enabled, the voltage channel is measured as long as the ADCEN is set to 1 and when the voltage channel is selected. The measurement operations may be enabled or disabled individually.

Disabling the ADC
ADC analog circuit has less power consumption if it is disabled. ADCEN bit in ADCCFG register controls this and it's cleared at EC Domain Reset.

The firmware should clear ADCEN bit before entering Doze/Deep Doze/Sleep mode.

7.11.4 EC Interface Registers

The ADC control/status and data out registers set interfaces with the EC through the EC Dedicated bus. These registers are mapped in the address space of the EC. The registers are listed below and the base address is 1900h.

Table 7-19. EC View Register Map, ADC

7 0	Offset
ADC Status Register (ADCSTS)	00h
ADC Configuration Register (ADCCFG)	01h
ADC Clock Control Register (ADCCTL)	02h
ADC General Control Register (ADCGCR)	03h
Voltage Channel 0 Control Register (VCH0CTL)	04h
Calibration Data Control Register (KDCTL)	05h
Voltage Channel 1 Control Register (VCH1CTL)	06h
Voltage Channel 1 Data Buffer LSB (VCH1DATL)	07h
Voltage Channel 1 Data Buffer MSB (VCH1DATM)	08h
Voltage Channel 2 Control Register (VCH2CTL)	09h
Voltage Channel 2 Data Buffer LSB (VCH2DATL)	0Ah
Voltage Channel 2 Data Buffer MSB (VCH2DATM)	0Bh
Voltage Channel 3 Control Register (VCH3CTL)	0Ch
Voltage Channel 3 Data Buffer LSB (VCH3DATL)	0Dh
Voltage Channel 3 Data Buffer MSB (VCH3DATM)	0Eh
Voltage Channel 0 Data Buffer LSB (VCH0DATL)	18h
Voltage Channel 0 Data Buffer MSB (VCH0DATM)	19h
Voltage Comparator Scan Period (VCMPSCP)	37h
Voltage Channel 4 Control Register (VCH4CTL)	38h
Voltage Channel 4 Data Buffer MSB (VCH4DATM)	39h
Voltage Channel 4 Data Buffer LSB (VCH4DATL)	3Ah
Voltage Channel 5 Control Register (VCH5CTL)	3Bh
Voltage Channel 5 Data Buffer MSB (VCH5DATM)	3Ch
Voltage Channel 5 Data Buffer LSB (VCH5DATL)	3Dh
Voltage Channel 6 Control Register (VCH6CTL)	3Eh
Voltage Channel 6 Data Buffer MSB (VCH6DATM)	3Fh
Voltage Channel 6 Data Buffer LSB (VCH6DATL)	40h
Voltage Channel 7 Control Register (VCH7CTL)	41h
Voltage Channel 7 Data Buffer MSB (VCH7DATM)	42h
Voltage Channel 7 Data Buffer LSB (VCH7DATL)	43h
ADC Data Valid Status (ADCDVSTS)	44h
Voltage Comparator Status (VCMPSTS)	45h
Voltage Comparator 0 Control Register (VCMP0CTL)	46h
Voltage Comparator 0 Threshold Data Buffer MSB (VCMP0THRDATM)	47h
Voltage Comparator 0 Threshold Data Buffer LSB (VCMP0THRDATL)	48h
Voltage Comparator 1 Control Register (VCMP1CTL)	49h
Voltage Comparator 1 Threshold Data Buffer MSB (VCMP1THRDATM)	4Ah
Voltage Comparator 1 Threshold Data Buffer LSB (VCMP1THRDATL)	4Bh
Voltage Comparator 2 Control Register (VCMP2CTL)	4Ch
Voltage Comparator 2 Threshold Data Buffer MSB (VCMP2THRDATM)	4Dh
Voltage Comparator 2 Threshold Data Buffer LSB (VCMP2THRDATL)	4Eh
Voltage Comparator Output Type Register (VCMPOTR)	4Fh
Voltage Comparator 0 Hysteresis Data Buffer MSB (VCMP0HYDATM)	50h
Voltage Comparator 0 Hysteresis Data Buffer LSB (VCMP0HYDATL)	51h
Voltage Comparator Lock Register (VCMPLR)	52h
ADC Input Voltage Mapping Full-Scale Code Selection 1 (ADCIVMFSCS1)	55h
ADC Input Voltage Mapping Full-Scale Code Selection 2 (ADCIVMFSCS2)	56h

For a summary of the abbreviations used for register type, see “Register Abbreviations and Access Rules”

7.11.4.1 ADC Status Register (ADCSTS)

This register indicates the global status of the ADC module. ADCSTS is cleared (00h) on VSTBY Power-Up reset; on other resets, bit 2 is unchanged and other bits are cleared.

Address Offset: 00h

Bit	R/W	Default	Description
7	-	1b	**ADC Conversion Time Select 1 (ADCCTS1)** Change this bit to increase or decrease the ADC conversion time.
6	-	0b	**Reserved**
5	R/W	0b	**Clock Source Select (SDIVSRC)** This bit provides selection of the clock source of ADC clock. See also SCLKDIV field in ADCCTL register. 0: Select EC Clock (frequency = FreqEC) 1: Select PLL Clock (frequency = FreqPLL) FreqPLL/FreqEC is listed in Table 10-2 on page 530.
4	-	0b	**Reserved**
3	R/W	0b	**Analog Accuracy Initialization Bit (AINITB)** Write 1 to this bit and write 0 to this bit immediately once and only once during the firmware initialization and do not write 1 again after initialization since IT5121 takes much power consumption if this bit is set as 1. Writing steps about this bit should be done before ADCEN bit is set in ADCCFG register. 1: Start ADC accuracy initialization. 0: Stop ADC accuracy initialization.
2	R/W	0b	**ADC Power Statement (ADCPS)** This bit remains zero when ADC power is in a normal state. When ADC power shuts down or failure occurs, the software must program this bit to one. The program has to be waited at least 200usec for ADC internal initialization after power on. 0: Indicate the ADC power in a normal state. 1: Indicate the ADC power in a shut-down or failure state.
1	R/WC	0b	**Data Overflow Event (DOVE)** Measurement data from the previous cycle was overwritten with data From the current cycle before being read. In the event of a data overflow, the DATVAL bit remains set and new data is placed in Channel Data Buffer register. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No overflow (default) 1: Overflow
0	R/WC	0b	**End-of-Cycle Event (EOCE)** End of ADC cycle; all enabled measurements (up to four) are completed. For each of the enabled channels, the DATVAL bit is set to 1 and the data stored in Channel Data Buffer register respectively. 0: Cycle in progress (default) 1: End of ADC cycle

7.11.4.2 ADC Configuration Register (ADCCFG)

This register controls the operation and global configuration of the ADC module.

Address Offset: 01h

Bit	R/W	Default	Description
7-6		10b	**Reserved**
5	-	0b	**ADC Conversion Time Select 0 (ADCCTS0)** Change this bit to increase or decrease the ADC conversion time.
4-3	-	-	**Reserved**
2	R/W	0b	**Interrupt from End-of-Cycle Event Enable (INTECEN)** Enables an ADC interrupt generated by End-of ADC-cycle event (EOCE in ADCSTS register). 0: Disable (default) 1: Enabled interrupt by EOCE event
1	R/W	0b	**Reserved**
0	R/W	0b	**ADC Module Enable (ADCEN)** Controls ADC operation or not 0: ADC disabled (default), power-down 1: ADC enabled

7.11.4.3 ADC Clock Control Register (ADCCTL)

This register controls the EC clock to ADC clock division.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-0	R/W	15h	**Select Clock Division Factor (SCLKDIV)** This field is used in selecting the divisor for the ADC clock divider. Note: SCLKDIV has to be equal to or greater then 1h.

7.11.4.4 ADC General Control Register (ADCGCR)

This register controls the ADC Data kept in VCHxDATL/VCHxDATM.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W	0b	**ADC Data Buffer Keep Enable (ADCDBKEN)** Enable this bit, and VCHxDATL/VCHxDATM will be kept until DATVAL is cleared (write 1 clear) especially for that conversion time is short. 0: Disable (default) 1: Enable
6-3	-	-	**Reserved**
2-0	R/W	2h	**Reserved** Note: Do not modify this default value.

7.11.4.5 Voltage Channel 0 Control Register (VCH0CTL)

This register both controls the operation and indicates the status of the Voltage channel.

Address Offset: 04h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The VCH0DATL/VCH0DATM is available for reading when DATVAL is set. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. 0: No valid data in VCH0DATL/VCH0DATM register (default) 1: End of conversion – new data is available in VCH0DATL/VCH0DATM
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt generated by Data valid event of voltage channel 0. 0: Disable (default) 1: Enable – ADC Interrupt from local DATVAL
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input is selected for measurement. The channel selection has to be programmed before the channel is measured. **Bits** 43210 Description 00000: Channel 0 00001: Channel 1 .... 01010: Channel 10 .... 01100: Channel 12 Others: Reserved 11111: Channel Disabled (default)

7.11.4.6 Calibration Data Control Register (KDCTL)

This register both controls the operation and indicates the status of the Calibration channel.

Address Offset: 05h

B it	R/W	Default	Description
7	R/W	0b	**Automatic Hardware Calibration Enable(AHCE)** 0: Disable automatic hardware calibration. 1: Enable automatic hardware calibration.
6-0	-	0000000b	**Reserved**

7.11.4.7 Voltage Channel 1 Control Register (VCH1CTL)

This register both controls the operation and indicates the status of Voltage Channel 1.

Address Offset: 06h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH1DATL/VCH1DATM register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 1. 0: Disable (default) 1: Enable – ADC Interrupt from local DATVAL
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input is selected for measurement. The channel selection has to be programmed before the channel is measured. **Bits** 43210 Description 00000: Channel 0 00001: Channel 1 .... 01010: Channel 10 .... 01100: Channel 12 Others: Reserved 11111: Channel Disabled (default)

7.11.4.8 Voltage Channel 1 Data Buffer LSB (VCH1DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 1.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 1. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.9 Voltage Channel 1 Data Buffer MSB (VCH1DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 1.

Address Offset: 08h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 1. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.10 Voltage Channel 2 Control Register (VCH2CTL)

This register both controls the operation and indicates the status of Voltage Channel 2.

Address Offset: 09h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.11.4.11 Voltage Channel 2 Data Buffer LSB (VCH2DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 2.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 2. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.12 Voltage Channel 2 Data Buffer MSB (VCH2DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 2.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 2. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.13 Voltage Channel 3 Control Register (VCH3CTL)

This register both controls the operation and indicates the status of Voltage Channel 3.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.11.4.14 Voltage Channel 3 Data Buffer LSB (VCH3DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 3.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 3. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.15 Voltage Channel 3 Data Buffer MSB (VCH3DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 3.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-2		-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 3. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.16 Voltage Channel 0 Data Buffer LSB (VCH0DATL)

This register (buffer) holds the data (LSB 7-0) measured by the Voltage Channel 0.

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R	-	**Voltage Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 0. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.17 Voltage Channel 0 Data Buffer MSB (VCH0DATM)

This register (buffer) holds the data (MSB 6 bits) measured by the Voltage Channel 0.

Address Offset: 19h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R	-	**Voltage Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 0. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.11.4.18 Voltage Comparator Scan Period (VCMPSCP)

This register defines the scan period of Voltage Comparator 0 ~ 2.

Address Offset: 37h

Bit	R/W	Default	Description
7-4	R/W	0110b	**Comparator 0/1/2 Scan Period (CMPSNP)** 0001b : 100 uS 0010b : 200 uS 0011b : 400 uS 0100b : 600 uS 0101b : 800 uS 0110b : 1mS 0111b : 1.5 mS 1000b : 2 mS 1001b : 2.5 mS 1010b : 3 mS 1011b : 4 mS 1100b : 5 mS
3-0	-	-	**Reserved**

7.11.4.19 Voltage Channel 4 Control Register (VCH4CTL)

This register both controls the operation and indicates the status of Voltage Channel 4.

Address Offset: 38h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH4DATL/VCH4DATM register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 4. 0: Disable (default) 1: Enable – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** Note: Only for ADC Input Channel 4 0 : Disable (Default) 1 : Enable
3-0	R/W	0000b	**Reserved**

7.11.4.20 Voltage Channel 4 Data Buffer MSB (VCH4DATM)

This register (buffer) holds the data(MSB 2bits) measured by the Volt Channel 4.

Address Offset: 39h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 4. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.21 Voltage Channel 4 Data Buffer LSB (VCH4DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 4.

Address Offset: 3Ah

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 4. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.22 Voltage Channel 5 Control Register (VCH5CTL)

This register both controls the operation and indicates the status of Voltage Channel 5.

Address Offset: 3Bh

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH5DATL/VCH5DATM register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 5. 0: Disable (default) 1: Enable – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** Note: Only for ADC Input Channel 5 0 : Disable (Default) 1 : Enable
3-0	R/W	0000b	**Reserved**

7.11.4.23 Voltage Channel 5 Data Buffer MSB (VCH5DATM)

This register (buffer) holds the data(MSB 2bits) measured by the Volt Channel 5.

Address Offset: 3Ch

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 5. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.24 Voltage Channel 5 Data Buffer LSB (VCH5DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 5.

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 5. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.25 Voltage Channel 6 Control Register (VCH6CTL)

This register both controls the operation and indicates the status of Voltage Channel 6.

Address Offset: 3Eh

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH6DATL/VCH6DATM register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 6. 0: Disable (default) 1: Enable – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** Note: Only for ADC Input Channel 6 0 : Disable (Default) 1 : Enable
3-0	R/W	0000b	**Reserved**

7.11.4.26 Voltage Channel 6 Data Buffer MSB (VCH6DATM)

This register (buffer) holds the data(MSB 2bits) measured by the Volt Channel 6.

Address Offset: 3Fh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 6. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.27 Voltage Channel 6 Data Buffer LSB (VCH6DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 6.

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 6. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.28 Voltage Channel 7 Control Register (VCH7CTL)

This register both controls the operation and indicates the status of Voltage Channel 7.

Address Offset: 41h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH7DATL/VCH7DATM register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 7. 0: Disable (default) 1: Enable – ADC Interrupt from local DATVAL
4	R/W	0b	**Voltage Channel Enable (VCHEN)** Note: Only for ADC Input Channel 7 0 : Disable (Default) 1 : Enable
3-0	R/W	0000b	**Reserved**

7.11.4.29 Voltage Channel 7 Data Buffer MSB (VCH7DATM)

This register (buffer) holds the data(MSB 2bits) measured by the Volt Channel 7.

Address Offset: 42h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R	-	**Volt Channel Data (VCHDAT9-8)** Volt channel data is measured by the volt channel 7. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.30 Voltage Channel 7 Data Buffer LSB (VCH7DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 7.

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 7. The data may be available only when DATVAL is set. DATVAL has to be cleared after data is read.

7.11.4.31 ADC Data Valid Status (ADCDVSTS)

This register indicates the data valid status of Voltage Channel 0 ~ 7.

Address Offset: 44h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid of Channel 7 (DAT7VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH7DATL/VCH7DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH7CTL
6	R/WC	0b	**Data Valid of Channel 6 (DAT6VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH6DATL/VCH6DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH6CTL
5	R/WC	0b	**Data Valid of Channel 5 (DAT5VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH5DATL/VCH5DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH5CTL
4	R/WC	0b	**Data Valid of Channel 4 (DAT4VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH4DATL/VCH4DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH4CTL

Bit	R/W	Default	Description
3	R/WC	0b	**Data Valid of Channel 3 (DAT3VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH3DATL/VCH3DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH3CTL
2	R/WC	0b	**Data Valid of Channel 2 (DAT2VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH2DATL/VCH2DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH2CTL
1	R/WC	0b	**Data Valid of Channel 1 (DAT1VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH1DATL/VCH1DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH1CTL
0	R/WC	0b	**Data Valid of Channel 0 (DAT0VAL)** The data may be read immediately when this bit is set to 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH0DATL/VCH0DATM register (default) 1: End of conversion – New data is available. Note: The same as DATVAL in VCH0CTL

7.11.4.32 Voltage Comparator Status (VCMPSTS)

This register indicates the status of Voltage Comparator 0 - 2.

Address Offset: 45h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/WC	0b	**Comparator 2 Reach Threshold Status (CMP2RTS)** This bit indicates the GPIO(GPJ5) status of comparator 2 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP2GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP2GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold

Bit	R/W	Default	Description
5	R/WC	0b	**Comparator 1 Reach Threshold Status (CMP1RTS)** This bit indicates the GPIO(GPJ4) status of comparator 1 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP1GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP1GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
4	R/WC	0b	**Comparator 0 Reach Threshold Status (CMP0RTS)** This bit indicates the GPIO(GPJ3) status of comparator 0 reach voltage threshold. This bit is cleared when writing 1 to it. If CMP0GPOL is set to 0b (active-high), 0: Not reach the voltage threshold 1: Reach the voltage threshold. If CMP0GPOL is set to 1b (active-low), 0: Reach the voltage threshold 1: Not reach the voltage threshold
3	-	-	**Reserved**
2	R/WC	0b	**Comparator 2 Reach Threshold Interrupt Status(CMP2RTIS)** This bit indicates the interrupt status of comparator 2 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.
1	R/WC	0b	**Comparator 1 Reach Threshold Interrupt Status (CMP1RTIS)** This bit indicates the interrupt status of comparator 1 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.
0	R/WC	0b	**Comparator 0 Reach Threshold Interrupt Status (CMP0RTIS)** This bit indicates the interrupt status of comparator 0 reach voltage threshold. This bit is cleared when writing 1 to it. 0: Not reach the voltage threshold 1: Reach the voltage threshold.

7.11.4.33 Voltage Comparator 0 Control Register (VCMP0CTL)

This register controls the operation of Voltage Comparator 0.

Address Offset: 46h

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 0 enable (CMP0EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 0 interrupt enable (CMP0INTEN)** 0: Disable 1: Enable

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 0 Trigger Mode (CMP0TMOD)** Select the trigger condition. 0: Less then or equal to CMP0THRDAT [9:0] 1: Greater then CMP0THRDAT [9:0]
4	R/W	0b	**Comparator 0 Edge/Level Sense Mode (CMP0ELSM)** Determines the sensed mode of the comparator 0. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 0 GPIO Polarity (CMP0GPOL)** Determines the GPIO(GPJ3) active high/low of the comparator 0. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 0 Channel Select (CMP0CSEL)** Select ADC channel for comparator 0. 000b : ADC0 001b : ADC1 010b : ADC2 011b : ADC3 100b : ADC4 101b : ADC5 110b : ADC6 111b : ADC7

7.11.4.34 Voltage Comparator 0 Threshold Data Buffer MSB (VCMP0THRDATM)

Address Offset: 47h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 0 Threshold Data (CMP0THRDAT9-8)** The MSB (2 Bits) of CMP0THRDAT.

7.11.4.35 Voltage Comparator 0 Threshold Data Buffer LSB (VCMP0THRDATL)

Address Offset: 48h

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 0 Threshold Data (CMP0THRDAT7-0)** The LSB (8 Bits) of CMP0THRDAT.

7.11.4.36 Voltage Comparator 1 Control Register (VCMP1CTL)

This register controls the operation of Voltage Comparator 1.

Address Offset: 49h

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 1 Enable (CMP1EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 1 Interrupt Enable (CMP1INTEN)** 0: Disable 1: Enable

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 1 Trigger Mode (CMP1TMOD)** Select the trigger condition. 0: Less then or equal to CMP1THRDAT [9:0] 1: Greater then CMP1THRDAT [9:0]
4	R/W	0b	**Comparator 1 Edge/Level Sense Mode (CMP1ELSM)** Determines the sensed mode of the comparator 1. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 1 GPIO Polarity (CMP1GPOL)** Determines the GPIO(GPJ4) active high/low of the comparator 1. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 1 channel select (CMP1CSEL)** Select ADC channel for comparator 1. 000b : ADC0 001b : ADC1 010b : ADC2 011b : ADC3 100b : ADC4 101b : ADC5 110b : ADC6 111b : ADC7

7.11.4.37 Voltage Comparator 1 Threshold Data Buffer MSB (VCMP1THRDATM)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 1 Threshold Data (CMP1THRDAT9-8)** The MSB (2 Bits) of CMP1THRDAT.

7.11.4.38 Voltage Comparator 1 Threshold Data Buffer LSB (VCMP1THRDATL)

Address Offset: 4Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Comparator 1 Threshold Data (CMP1THRDAT7-0)** The LSB (8 Bits) of CMP1THRDAT.

7.11.4.39 Voltage Comparator 2 Control Register (VCMP2CTL)

This register controls the operation of Voltage Comparator 2.

Address Offset: 4Ch

Bit	R/W	Default	Description
7	R/W	0b	**Comparator 2 enable (CMP2EN)** 0: Disable 1: Enable
6	R/W	0b	**Comparator 2 interrupt enable (CMP2INTEN)** 0: Disable 1: Enable

Bit	R/W	Default	Description
5	R/W	0b	**Comparator 2 Trigger Mode (CMP2TMOD)** Select the trigger condition. 0: Less then or equal to CMP2THRDAT [9:0] 1: Greater than CMP2THRDAT [9:0]
4	R/W	0b	**Comparator 2 Edge/Level Sense Mode (CMP2ELSM)** Determines the sensed mode of the comparator 1. 0: Level-sensed 1: Edge-sensed
3	R/W	0b	**Comparator 2 GPIO Polarity (CMP2GPOL)** Determines the GPIO(GPJ5) active high/low of the comparator 2. 0: Active-high 1: Active-low
2-0	R/W	000b	**Comparator 2 Channel Select (CMP2CSEL)** Select ADC channel for comparator 2. 000b : ADC0 001b : ADC1 010b : ADC2 011b : ADC3 100b : ADC4 101b : ADC5 110b : ADC6 111b : ADC7

7.11.4.40 Voltage Comparator 2 Threshold Data Buffer MSB (VCMP2THRDATM)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 2 Threshold Data (CMP2THRDAT9-8)** The MSB (2 Bits) of CMP2THRDAT.

7.11.4.41 Voltage Comparator 2 Threshold Data Buffer LSB (VCMP2THRDATL)

Address Offset: 4Eh

Bit	R/W	Default	Description
7-0	R/W	00b	**Comparator 2 Threshold Data (CMP2THRDAT7-0)** The LSB (8 Bits) of CMP2THRDAT.

7.11.4.42 Voltage Comparator Output Type Register (VCMPOTR)

This register controls the output type of voltage comparator .

Address Offset: 4Fh

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Comparator 0 Hysteresis Enable (CMP0HYSEN)** Hysteresis enable of the comparator 0. 0: Disable 1: Enable
3	R/W	0b	**Reserved**

Bit	R/W	Default	Description
2	R/W	0b	**Comparator 2 Output Type (CMP2OT)** Determines the output type of the comparator 2. 0: Push-pull 1: Open-drain
1	R/W	0b	**Comparator 1 Output Type (CMP1OT)** Determines the output type of the comparator 1. 0: Push-pull 1: Open-drain
0	R/W	0b	**Comparator 0 Output Type (CMP0OT)** Determines the output type of the comparator 0. 0: Push-pull 1: Open-drain

7.11.4.43 Voltage Comparator 0 Hysteresis Data Buffer MSB (VCMP0HYDATM)

Address Offset: 50h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Comparator 0 Hysteresis Data (CMP0HYDAT9-8)** The MSB (2 Bits) of CMP0HYDAT.

7.11.4.44 Voltage Comparator 0 Hysteresis Data Buffer LSB (VCMP0HYDATL)

Address Offset: 51h

Bit	R/W	Default	Description
7-0	R/W	00b	**Comparator 0 Hysteresis Data (CMP0HYDAT7-0)** The LSB (8 Bits) of CMP0HYDAT.

7.11.4.45 Voltage Comparator Lock Register (VCMPLR)

This register locks the control register of the voltage comparator.

Address Offset: 52h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Comparator 2 Lock Enable (CMP2LE)** Lock the control register of the comparator 2 (except CMP2INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.
1	R/W	0b	**Comparator 1 Lock Enable (CMP1LE)** Lock the control register of the comparator 1 (except CMP1INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.

Bit	R/W	Default	Description
0	R/W	0b	**Comparator 0 Lock Enable (CMP0LE)** Lock the control register of the comparator 0 (except CMP0INTEN). 0: Disable 1: Enable Once the bit is set, it cannot be disabled until VSTBY Power-Up Reset or Warm Reset.

7.11.4.46 ADC Input Voltage Mapping Full-Scale Code Selection 1 (ADCIVMFSCS1)

This register controls ADC Full-Scale code.

Address Offset: 55h

Bit	R/W	Default	Description
7	R/W	0b	**Channel7 Select Full-Scale Code (C7SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
6	R/W	0b	**Channel6 Select Full-Scale Code (C6SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
5	R/W	0b	**Channel5 Select Full-Scale Code (C5SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
4	R/W	0b	**Channel4 Select Full-Scale Code (C4SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
3	R/W	0b	**Channel3 Select Full-Scale Code (C3SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
2	R/W	0b	**Channel2 Select Full-Scale Code (C2SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
1	R/W	0b	**Channel1 Select Full-Scale Code (C1SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
0	R/W	0b	**Channel0 Select Full-Scale Code (C0SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.

7.11.4.47 ADC Input Voltage Mapping Full-Scale Code Selection 2 (ADCIVMFSCS2)

This register control ADC Full-Scale code.

Address Offset: 56h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**Channel10 Select Full-Scale Code (C10SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
1	R/W	0b	**Channel9 Select Full-Scale Code (C9SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.
0	R/W	0b	**Channel8 Select Full-Scale Code (C8SFSC)** 0: ADC input voltage 0V ~ AVCC/1.1 is mapped to 0h-3FFh while AVCC is 3.3V. 1: ADC input voltage 0V ~ AVCC is mapped to 0h-3FFh.

7.11.5 ADC Programming Guide

Table 7-20. Detail Step of ADC Channel Conversion

Step	Description
1	Set AINITB@ADCSTS = 1 (only once after VSTBY power-on)
2	Automatic hardware calibration enable (only once after VSTBY power-on) AHCE@KDCTL = 1
3	Set AINITB@ADCSTS = 0 (only once after VSTBY power-on)
4	Enable VCHiCTL for measuring desired channels; n = 0,1, 2, or 3
5	For example, to measure ADC0 voltage on voltage buffer 1, set SELIN@VCH1CTL = 0
6	Start ADC channel conversion by setting ADCEN@ADCCFG =1
7	Wait for DATVAL@VCH1CTL = 1 IGet ADC0 output data **D**[9:0] by reading VCH1DATM and VCH1DATL **D**[9:0] = {VCH1DATM [1:0], VCH1DATL[7:0]}
8	Disable ADC to reduce power consumption by setting ADCEN@ADCCFG = 0

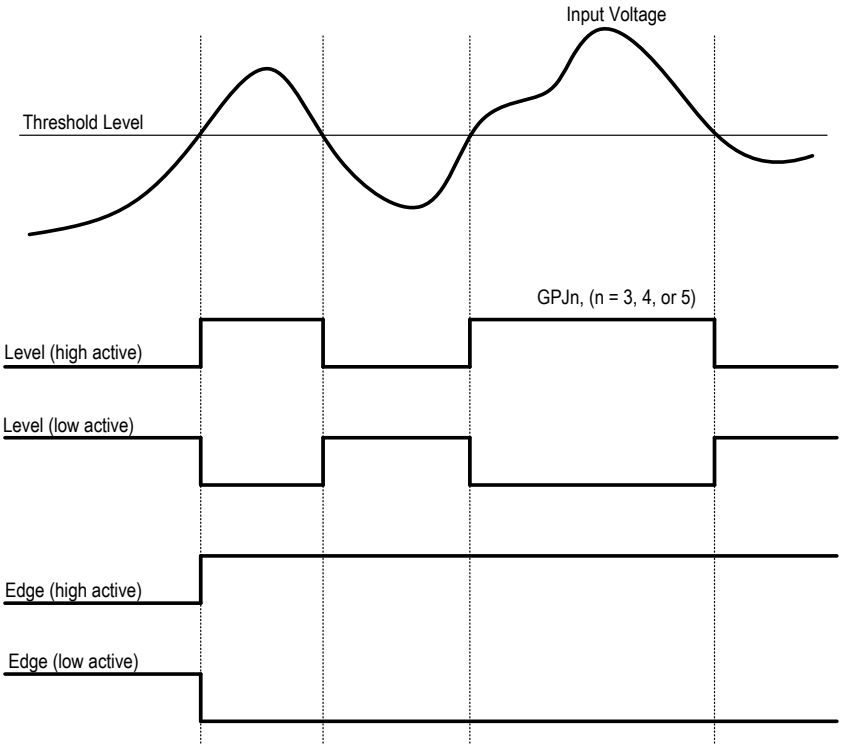
7.11.6 Voltage Comparator Programming Guide

Table 7-21. Detail Step of Voltage Comparator Programming

Step	Description
1	**Set voltage comparator threshold level buffer:** Program CMP0THRDAT[9:0] to select the threshold level for voltage comparator 0. The equivalent threshold voltage is (3V * CMP0THRDAT/1023).
2	**Select the voltage input channel:** Program CMP0CSEL to select one of the voltage input channels AD0-AD7. This sets voltage comparator 0 to monitor the selected voltage input channel. Notice, that the selected channel must be set to its alternate function for ADC application.

Step	Description
3	**Set voltage comparator trigger mode:** If CMP0TMOD is set 0, a event is produced while the voltage of the selected channel is lower than or equal to the threshold level. If CMP0TMOD is set to 1, a event is produced while the voltage of the selected channel is higher than the threshold level.
4	**Set the scan period of voltage comparator:** Set CMPSNP @ VCMPSCP to determine the interval per comparing operation for voltage comparator.
5	**Set event response:** Set CMP0INTEN = 1, the event in Step 3 would be propagated to INT151. or Set CMP0GPEN @ GCR15 and GPCRJ3 = 00h , the event in Step 3 would be propagated to GPJ3
6	**Start voltage comparator conversion** CMP0EN @ VCMP0CTL = 1
7	**Wait for input voltage's reaching threshold level** If the input voltage reaches the threshold level, CMP0RTS @VCMPSTS will be set to 1 , and corresponding GPJ3 will change the output status if this function is enabled in Step 5. In Level-sensed mode, the input voltage far away from the threshold level, CMP0RTS / GPJ3 willl be reset immediately. In Edge-sensed mode, the input voltage is far away from the threshold level, CMP0RTS / GPJ3 only be reset when write 1 to CMP0RTS. If CMP0INTEN = 1, the input voltage reaches the threshold level, then generates INT151, and CMP0RTIS @VCMPSTS will be set to 1. Write 1 to clear this bit and only the input voltage is far away from the threshold level. (Refer to Figure 7-19 , on page 386)

Figure 7-19. Voltage Comparator Operation Time



7.12 PWM

7.12.1 Overview

The PWM module generates eight 8-bit PWM outputs; each PWM output may have a different duty cycle. The fan speed is controlled by software.

7.12.2 Features

- Supports eight PWM outputs.
- Supports two sets tachometers; each set tachometer can be switched from two external pins.
- Supports PWM open-drain output.
- Supports two channels to control LEDs in dimming mode.

7.12.3 Functional Description

7.12.3.1 General Description

Figure 7-20. PWM Diagram

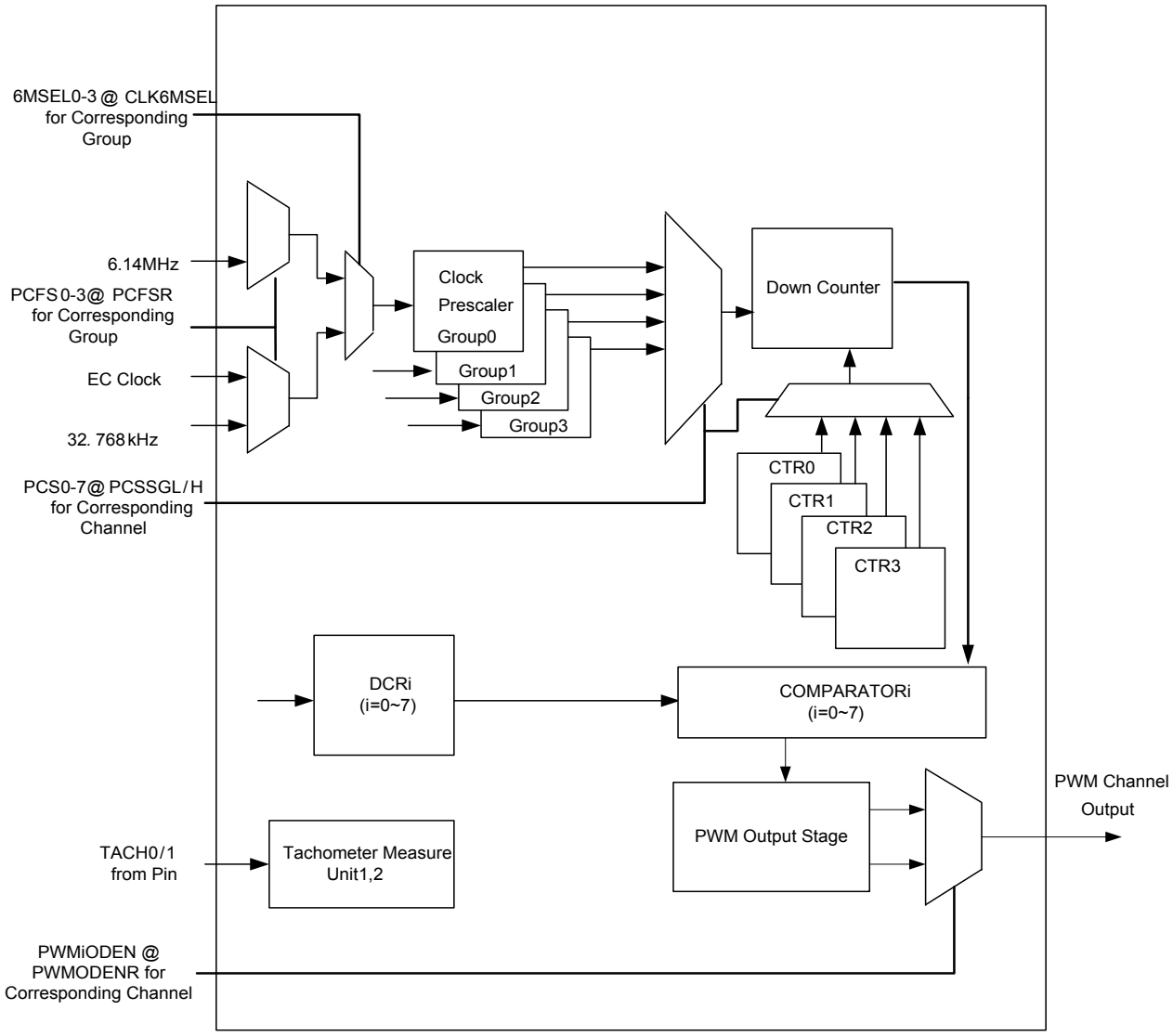
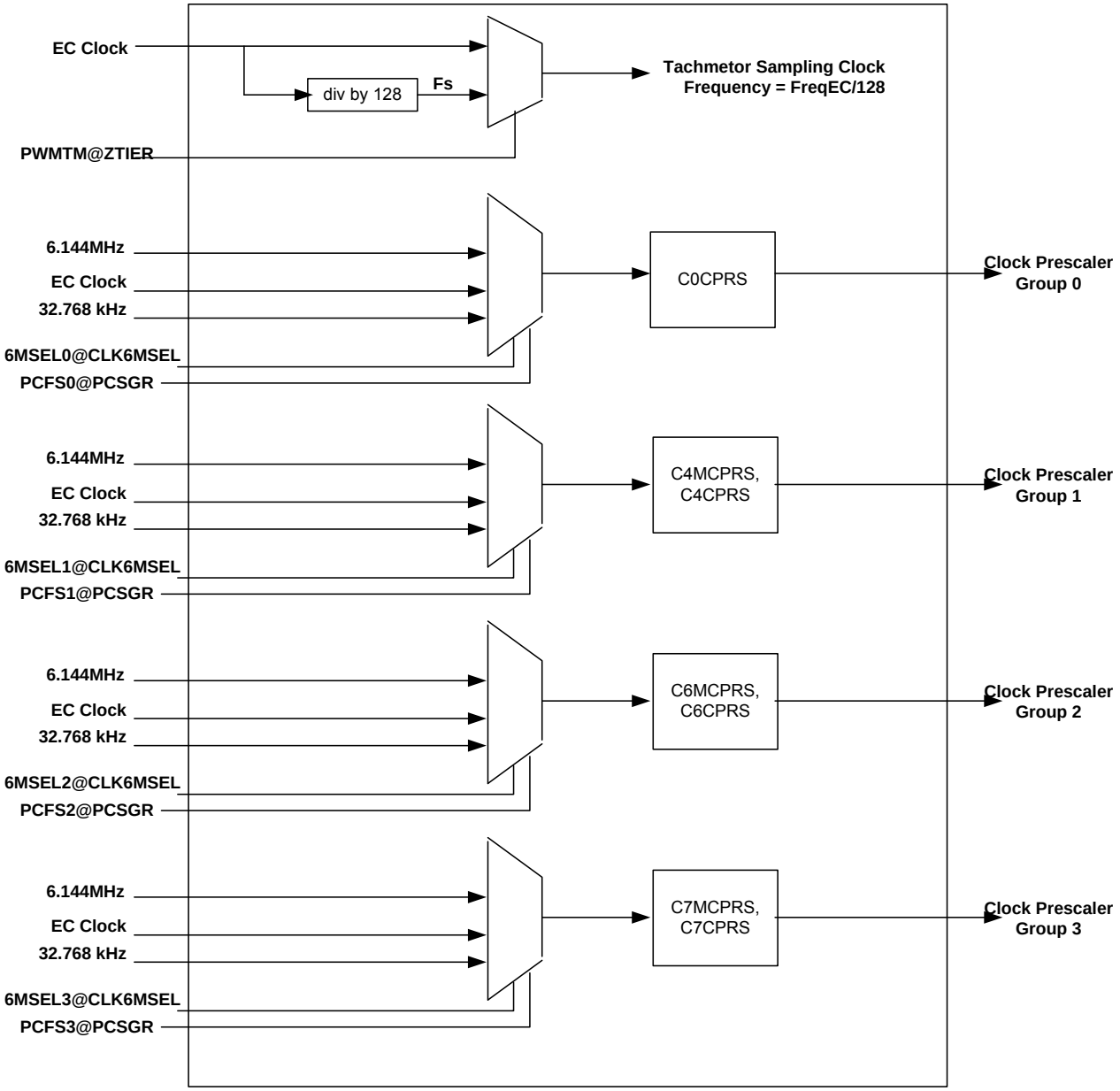


Figure 7-21. PWM Clock Tree



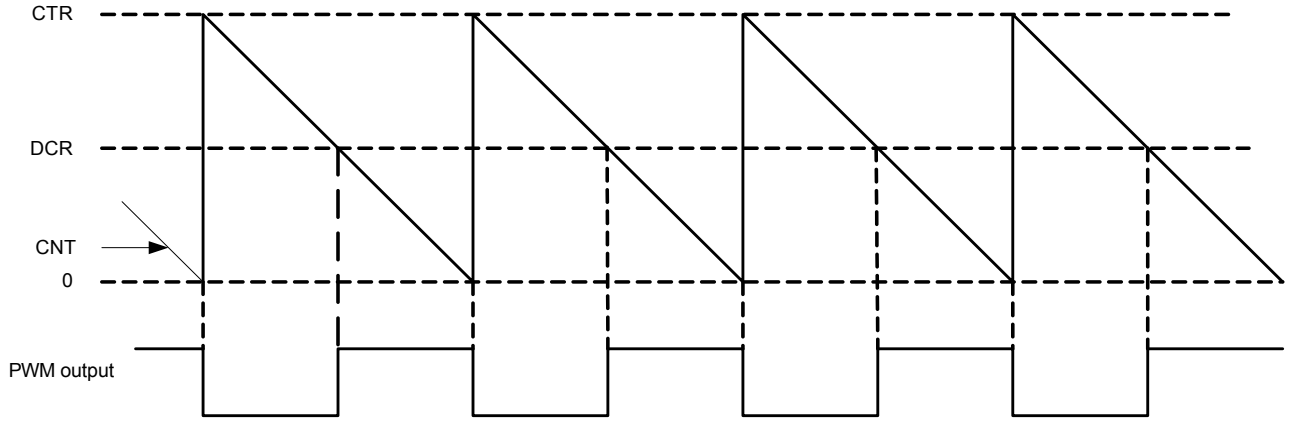
The PWM uses the 32.768 kHz Clock, EC Clock or 6.14 MHz Clock as a reference for its PWM output. The prescaler divider values in CiCRPS register which divides the PWM input clock into its working clock respectively. Each channel can select their prescaler divider by {PCSSGH, PCSSGL} register. The prescaler divider C0CPRS register has 8-bit counter value; and the {CiMCRPS, CiCRPS}(i=4,6,7) has 16-bit counter value. The PWM provides eight 8-bit PWM outputs, which are PWM0 to PWM7. Each PWM output is controlled by its Duty Cycle registers (DCRi, i =0 to 7). All PWM output is controlled by a Cycle Time registers (CTRi, i =0 to 3).

When PWM working clock is enabled, the PWM cycle output is high when the value in the DCRi register is greater than the value in CTR down-counter. When the value of DCRi register is not greater than the value in CTR down-counter, the PWMi cycle output is on LOW and PWMi cycle output polarity can be inversed by INVPi register.

When the value in CTR counter down-counter reaches 0, the value in CTR counter will be reloaded then start down-counter until the PWM working clock is disabled.

Cycle Time and Duty Cycle

Figure 7-22. PWM Output Waveform



The PWM module supports duty cycles ranging from 0% to 100%.
The PWMi output signal cycle time is:

n(CiCPRS + 1) x (CTR + 1) x T_{clk}

Where:

- T_{clk} is the period of PWM input clock = (1 / 32.768 kHz) or (1 / FreqEC), which is selected by PCFS3-0 in PCFSR regiser. (FreqEC is listed in Table 10-2 on page 530)
- The PWMi output signal duty cycle (in %, when INVPi is 0) is:
  (DCRi) / (CTR + 1) x 100.

In the following cases, the PWMi output is hold at a state(low or high):

- PWMi output is still low when the content of DCRi is greater than the CTR value.
- PWMi output is still high when the content of DCRi is equal to the CTR value.
- PWMi output is still low when the content of DCRi =0 & INVPi = 0 is in PWMPOL register.

PWM Inhibit Mode

The PWM is in an inhibit mode when PCCE in ZTIER Register is 0. In this mode, the PWM input clock is disabled (stopped). The PWMi signal is 0 when INVPi bit is 0; it is 1 when INVPi bit is 1. It is recommended the PRSC and CTR registers should be updated in a PWM inhibit mode.

7.12.3.2 Manual Fan Control Mode

The content of the Tachometer Reading Register is still updated according to the sampling counter that samples the tachometer input (TACH0A/B pin for FAN1 of the local sensor zone and TACH1A/B pin for FAN2 of the remote sensor zone). The sampling rate (fs) is FreqEC / 128. (FreqEC is listed in Table 10-2 on page 530)

Fan Speed (R.P.M.) = 60 / (1/fs sec * {FnTMRR, FnTLRR} * P)

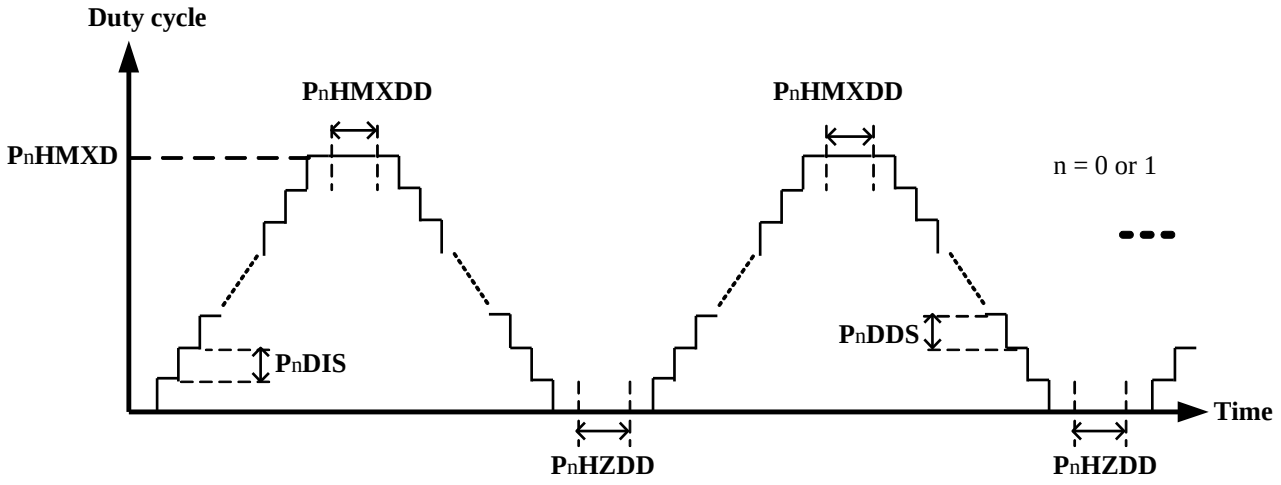
n denotes 1 or 2
P denotes the numbers of square pulses per revolution.
And {FnTMRR, FnTLRR} = 0000h denotes Fan Speed is zero.

7.12.3.3 PWM Dimming Mode

Two PWM channels can operate in dimming mode to control LED light. In this mode, PWM generates a modulation signal with its duty cycle gradually increasing and decreasing which depends on the setting of the related PWMn {n = 0 or 1} LED control registers. With LED light connecting to such PWM signal, it shows a dimming-like light.

PWM Dimming Mode should be used with 32K clock input. Before dimming mode starts, user should decide LED dimming behavior first by setting LED control registers, otherwise LED would show a unpredicatable behavior. Once heatbeat mode is enabled by register 50h or 53h, PWM cycle time will be auto set FFh. Due to 32K clock and FFh cycle time, each PWM cycle take 8ms. {1/32K * (FFh+1) }.
Figure 7-30. shows the behavior of the PWM duty cycle controlled by the related LED control registers.

Figure 7-23. PWM LED Dimming Mode Waveform



As the illustrated waveform above, in PWM dimming mode, duty cycle increases or decreases step by step with each PWM cycle. The increasing or decreasing track are linear and can be decided individually by PnDIS and PnDDS.The maximum duty cycle is also selective by PnHMXD. When duty cycle increase to the maximum value, PWM can keep the maximum duty cycle a priod of time decided by PnHMXDD. On the contrary, PWM can keep the zero duty cycle a priod of time decided by PnHZDD. Note that n = 0 or 1 represents PWM0 or PWM1.

7.12.4 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 1800h.

Table 7-22. EC View Register Map, PWM

7 0	Offset
Channel 0 Clock Prescaler Register (C0CPRS)	00h
Cycle Time 0 (CTR0)	01h
Cycle Time 1 (CTR1)	41h
Cycle Time 1 MSB (CTR1M)	5Bh
Cycle Time 2 (CTR2)	42h
Cycle Time 3 (CTR3)	43h
PWM Duty Cycle (DCR0-7)	02h-09h
PWM Duty Cycle 2 MSB (DCR2M)	5Ch
PWM Duty Cycle 3 MSB (DCR3M)	5Dh
PWM Polarity (PWMPOL)	0Ah
Prescaler Clock Frequency Select Register (PCFSR)	0Bh
Prescaler Clock Source Select Group Low (PCSSGL)	0Ch
Prescaler Clock Source Select Group High (PCSSGH)	0Dh
Prescaler Clock Source Gating Register (PCSGR)	0Fh
Fan 1 Tachometer LSB Reading (F1TLRR)	1Eh
Fan 1 Tachometer MSB Reading (F1TMRR)	1Fh
Fan 2 Tachometer LSB Reading (F2TLRR)	20h
Fan 2 Tachometer MSB Reading (F2TMRR)	21h
Zone Interrupt Status Control Register (ZINTSCR)	22h
PWM Clock Control Register (ZTIER)	23h
Channel 4 Clock Prescaler Register (C4CPRS)	27h
Channel 4 Clock Prescaler MSB Register (C4MCPRS)	28h
Channel 6 Clock Prescaler Register (C6CPRS)	2Bh
Channel 6 Clock Prescaler MSB Register (C6MCPRS)	2Ch
Channel 7 Clock Prescaler Register (C7CPRS)	2Dh
Channel 7 Clock Prescaler MSB Register (C7MCPRS)	2Eh
PWM Clock 6MHz Select Register (CLK6MSEL)	40h
PWM5 Timeout Control Register (PWM5TOCTRL)	44h
Fan 3 Tachometer LSB Reading (F3TLRR)	45h
Fan 3 Tachometer MSB Reading (F3TMRR)	46h
Zone Interrupt Status Control Register 2 (ZINTSCR2)	47h
Tachometer Switch Control Register 2 (TSWCTLR2)	4Fh
Tachometer Switch Control Register (TSWCTLR)	48h
PWM Output Open-Drain Enable Register (PWMODENR)	49h
Backlight Duty Register (BLDR)	4Ch
PWM0 LED Dimming Enable Register (PWM0LHE)	50h
PWM0 LED Dimming Control Register 1 (PWM0LCR1)	51h
PWM0 LED Dimming Control Register 2 (PWM0LCR2)	52h
PWM1 LED Dimming Enable Register (PWM1LHE)	53h
PWM1 LED Dimming Control Register 1 (PWM1LCR1)	54h
PWM1 LED Dimming Control Register 2 (PWM1LCR2)	55h
PWM Load Counter Control Register (PWMLCCR)	5Ah

Other related register(s):
- General Control 2 Register (GCR2), TACH2AEN and TACH2BEN bit
- General Control 5 Register (GCR5), TACH0BEN bit
- General Control 5 Register (GCR5), TACH1BEN bit

For a summary of the abbreviations used for register types, see “Register Abbreviations and Access Rules”

7.12.4.1 Channel 0 Clock Prescaler Register (C0CPRS)

This register controls the cycle time and the minimal pulse width of channel 0~3.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV)** PWM input clock is divided by the number of (C0CPRS+ 1). For example, the value of 01h results in a divide by 2. The value of FFh results in a divide by 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.2 Cycle Time Register 0 (CTR0)

This register controls the cycle time 0 and duty cycle steps.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 0 (CTV0)** The Prescaler output clock is divided by the number of (CTR0 + 1). For example, the value of 00h results in a divide by 1. The value of FFh results in a divide by 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.3 Cycle Time Register 1 (CTR1)

This register controls the cycle time 1 and duty cycle steps.

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 1 (CTV1)** The Prescaler output clock is divided by the number of (CTR1M*100h + CTR1). For example, the value of 00h results in a divide by 1. The value of 3FFh results in a divide by 1024. After writing data to the register, system will be changed to the 4-CTR mode. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.12.4.4 Cycle Time Register 1 MSB (CTR1M)

This register controls the MSB of cycle time 1 and duty cycle steps.

Address Offset: 5Bh

Bit	R/W	Default	Description
1-0	R/W	3h	**Cycle Time Value 1 MSB (CTV1M)** Refer to the description of CTR1. The CTR1M and CTR1 register must be written successively in order. That is, write MSB first.

7.12.4.5 Cycle Time Register 2 (CTR2)

This register controls the cycle time 2 and duty cycle steps.

Address Offset: 42h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 2 (CTV2)** The function of this register is the same as that of CTR1.

7.12.4.6 Cycle Time Register 3 (CTR3)

This register controls the cycle time 2 and duty cycle steps.

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 3 (CTV3)** The function of this register is the same as that of CTR1.

7.12.4.7 PWM Duty Cycle Register 0 to 7(DCRi)

This register (DCRi; i=0 to 7) controls the duty cycle of PWMi output signal.

Address Offset: 02h(ch0), 03h(ch1), 04h(ch2), 05h(ch3), 06h(ch4), 07h(ch5), 08h(ch6), 09h(ch7);

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value (DCV)** DCRi register decides the number of clocks for which PWMi is high when INVPi bit is 0 in PWMPOL register. The PWMi Duty Cycle output = (DCRi)/(CTR+1) If the DCRi value > CTR value, PWMi signal is still low. If DCRi value = CTR value, PWMi signal is still high. When Inverse PWMi bit is 1, the value of PWMi is inversed.

7.12.4.8 PWM Duty Cycle Register 2 MSB (DCR2M)

This register controls the duty cycle MSB of PWM2 output signal.

Address Offset: 5Ch

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00h	**Duty Cycle Value 2 MSB (DCV2M)** DCR2M register decides the number of clocks for which PWM2 is high when INVP2 bit is 0 in PWMPOL register. The PWM2 Duty Cycle output = (DCR2M * 100h + DCR2)/(CTR1M * 100h + CTR1) If the (DCR2M * 100h + DCR2) value > (CTR1M * 100h + CTR1) value, PWM2 signal is still low. If (DCR2M * 100h + DCR2) value = (CTR1M * 100h + CTR1) value, PWM2 signal is still high. When Inverse PWM2 bit is 1, the value of PWM2 is inversed. This register will value when the next time write DCV2.

7.12.4.9 PWM Duty Cycle Register 3 MSB (DCR3M)

This register controls the duty cycle MSB of PWM3 output signal.

Address Offset: 5Dh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00h	**Duty Cycle Value 3 MSB (DCV3M)** DCR3M register decides the number of clocks for which PWM3 is high when INVP3 bit is 0 in PWMPOL register. The PWM3 Duty Cycle output = (DCR3M * 100h + DCR3)/(CTR1M * 100h + CTR1) If the (DCR3M * 100h + DCR3) value > (CTR1M * 100h + CTR1) value, PWM3 signal is still low. If (DCR3M * 100h + DCR3) value = (CTR1M * 100h + CTR1) value, PWM3 signal is still high. When Inverse PWM3 bit is 1, the value of PWM3 is inversed. This register will value when the next time write DCV3.

7.12.4.10 PWM Polarity Register (PWMPOL)

This register controls the polarity of PWM0 to PWM7.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Inverse PWM Outputs (INVP7-0)** Bit 7 to 0 control the polarity of PWM7 to PWM0 respectively. 0: Non-inverting. 1: Inverting.

7.12.4.11 Prescaler Clock Frequency Select Register (PCFSR)

This register Bit 3~0 is used to select prescaler clock frequency for four channel group 3~0. Each of them includes 1 set prescaler registers. See the following table.

Channel Group	Prescaler Channels
0	C0CPRS
1	C4MCPRS,C4CPRS
2	C6MCPRS,C6CPRS
3	C7MCPRS,C7CPRS

Address Offset: 0Bh

Bit	R/W	Default	Description
5-4	-	-	**Reserved**
3-0	R/W	0000b	**Prescaler Clock Frequency Select (PCFS3-0)** The clock source of the prescaler of group 0 consists of G6MSEL0 and PCFS0 bit. G6MSEL0 bit is in CLK6MSEL register. PCFS0 bit is in this register. {G6MSEL0, PCFS0}: 00b: Select 32.768 kHz. 01b: Select FreqEC (EC Clock). 10b: Select FreqEC*2/3 (6.14 MHz) 11b: Reserved (FreqEC and FreqPLL are listed in Table 10-2 on page 530) So are group 1, 2 and 3.

7.12.4.12 Prescaler Clock Source Select Group Low (PCSSGL)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock sources.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-6	R/W	00b	**Prescaler Clock Select 3 (PCS3)** The bits select prescaler clock for channel 3. The bits 7-6 are the same as bit 1-0.
5-4	R/W	00b	**Prescaler Clock Select 2 (PCS2)** The bits select prescaler clock for channel 2. The bits 5-4 are the same as bit 1-0.
3-2	R/W	00b	**Prescaler Clock Select 1 (PCS1)** The bits select prescaler clock for channel 1. The bits 3-2 are the same as bit 1-0.

Bit	R/W	Default	Description
1-0	R/W	00b	**Prescaler Clock Select 0 (PCS0)** Default as below： 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR0 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR0 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR0 After writing data to CTR1,CTR2 or CTR3 register 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR1 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR2 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR3

7.12.4.13 Prescaler Clock Source Select Group High (PCSSGH)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock sources.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	R/W	01b	**Prescaler Clock Select 7 (PCS7)** The bits select prescaler clock for channel 7. The bits 7-6 are the same as bit 1-0.
5-4	R/W	01b	**Prescaler Clock Select 6 (PCS6)** The bits select prescaler clock for channel 6. The bits 5-4 are the same as bit 1-0.
3-2	R/W	01b	**Prescaler Clock Select 5 (PCS5)** The bits select prescaler clock for channel 5. The bits 3-2 are the same as bit 1-0.
1-0	R/W	01b	**Prescaler Clock Select 4 (PCS4)** The bits select prescaler clock for channel 4. Default as below： 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR0 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR0 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR0 After writing data to CTR1,CTR2 or CTR3 register 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR1 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR2 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR3

7.12.4.14 Prescaler Clock Source Gating Register (PCSGR)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Clock Source Gating (PCSG)** Bits 7-0 are used to gate prescaler clock source for PWM channels 7-0 respectively. 0: no gating clock source 1: gating clock source; PWM channel output is 0 when INVP bit is set to 0 respectively

7.12.4.15 Fan 1 Tachometer LSB Reading Register (F1TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. The tachometer input of Fan 1 corresponds to TACH0A/TACH0B, and it can be switched by controlling the T0CHSEL bit.
Reading F1TLRR and F1TMRR registers should be in pairs to get the correct 16-bit tachometer value.
Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.
After switching the input TACH0A/TACH0B, these two registers should be read in pairs after the data-valid status (T0DIS or T0DVS bit) is set.

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer 1 LSB Value (CT1ACHLV)** The value of bit 7-0 denotes the LSB tachometer speed.

7.12.4.16 Fan 1 Tachometer MSB Reading Register (F1TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. The tachometer input of Fan 1 corresponds to TACH0A/TACH0B, and it can be switched by controlling the T0CHSEL bit.

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer 1 MSB Value (CT1ACHMV)** The value of bits 7-0 denotes MSB Tachometer speed.

7.12.4.17 Fan 2 Tachometer LSB Reading Register (F2TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. The tachometer input of Fan 2 corresponds to TACH1A/TACH1B, and it can be switched by controlling the T1CHSEL bit.
Reading F2TLRR and F2TMRR registers should be in pairs to get the correct 16-bit tachometer value.
Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.
After switching the input TACH1A/TACH1B, these two registers should be read in pairs after the data-valid status (T1DIS or T1DVS bit) is set.

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer 2 LSB Value (CT2ACHLV)** The value of bits 7-0 denotes the LSB tachometer speed.

7.12.4.18 Fan 2 Tachometer MSB Reading Register (F2TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16-bit binary digits. The tachometer input of Fan 2 corresponds to TACH1A/TACH1B, and it can be switched by controlling the T1CHSEL bit.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer 2 MSB Value (CT2ACHMV)** The value of bits 7-0 denotes the MSB tachometer speed.

7.12.4.19 Zone Interrupt Status Control Register (ZINTSCR)

Address Offset: 22h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5	R/W	0b	**TACH0A/TACH0B Data-valid Interrupt Enable (T0DIE)** 1: Enable interrupt to CPU when fan 1 tachometer data is valid. 0: Disable interrupt to CPU when fan 1 tachometer data is valid.
4	R/WC	0b	**TACH0A/TACH0B Data-valid Interrupt Clear (T0DIC)** Write one to clear the Interrupt status, which is caused when fan 1 tachometer data is valid; writing zero is ignored.
3	R	0b	**TACH0A/TACH0B Data-valid Interrupt Status (T0DIS)** 1: Fan 1 tachometer data-valid event occurs. 0: No fan 1 tachometer data-valid event occurs.
2	R/W	0b	**TACH1A/TACH1B Data-valid Interrupt Enable (T1DIE)** 1: Enable interrupt to CPU when fan 2 tachometer data is valid. 0: Disable interrupt to CPU when fan 2 tachometer data is valid.
1	R/WC	0b	**TACH1A/TACH1B Data-valid Interrupt Clear (T1DIC)** Write one to clear the Interrupt status, which is caused when fan 2 tachometer data is valid; writing zero is ignored.
0	R	0b	**TACH1A/TACH1B Data-valid Interrupt Status (T1DIS)** 1: Fan 2 tachometer data-valid event occurs. 0: No fan 2 tachometer data-valid event occurs.

7.12.4.20 PWM Clock Control Register (ZTIER)

Address Offset: 23h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5-2	-	0b	**Reserved**
1	R/W	0b	**PWM Clock Counter Enable (PCCE)** 1: Enable PWMs clock counter. Set this bit to 1 after all other registers have been set. 0: Disable PWMs clock counter
0	R/W	0b	**PWM Test Mode (PWMTM)** 1: PWM switches to a test mode 0: PWM works on a normal mode

7.12.4.21 Channel 4 Clock Prescaler Register (C4CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C4MCPRS defines the high byte.

7.12.4.22 Channel 4 Clock Prescaler MSB Register (C4MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the details.

7.12.4.23 Channel 6 Clock Prescaler Register (C6CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Bh

	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C6MCPRS defines the high byte.

7.12.4.24 Channel 6 Clock Prescaler MSB Register (C6MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the details.

7.12.4.25 Channel 7 Clock Prescaler Register (C7CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C7MCPRS defines the high byte.

7.12.4.26 Channel 7 Clock Prescaler MSB Register (C7MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the details.

7.12.4.27 PWM Clock 6MHz Select Register (CLK6MSEL)

This register controls the group clock.

Address Offset: 40h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R	0b	**Cycle Time Register Mode (CTRMODE)** 0: 1 cycle time mode. 1: 4 cycle time mode. After writing data to CTR1, CTR2, or CTR3, the bit will be set to 1 and system will be changed to the 4-CTR mode.
3-0	R/W	0000b	**Clock Group 6MHz Selection (G6MSEL3-0)** Refer to PCFS3-0 field in PCFSR register.

7.12.4.28 PWM5 Timeout Control Register (PWM5TOCTRL)

This register controls the PWM5 Timeout Period.
Backlight mode control is enabled.

Address Offset: 44h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Backlight Mode Enable (BME)** 0: Tachometer 2 choice r.p.m. mode. 1: Tachometer 2 choice backlight mode.
3	-	-	**Reserved**
2-0	R/W	000b	**PWM5 Timeout Period Selection (PWM5TOSEL3-0)** If PWM5 Timeout is enabled, PWM5 output would be held 100% duty when the DCR of PWM5 is not updated during the specified time selected in Timeout Control Register. 000h: Disable 001h: 1 sec 010h: 1.5 sec 011h: 2 sec 100h: 2.5 sec 101h: 3 sec 110h: 3.5 sec 111h: 4 sec

7.12.4.29 Fan 3 Tachometer LSB Reading (F3TLRR)

When BME is 1, this register reflects the LSB value of the current Frequency of the Backlight from TACH2. The value is shown in 16-bit format.
Reading CFLRR and CFMRR registers should be in pairs to get the correct 16-bit frequnecy value.Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.

Address Offset: 45h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer 3 LSB Value (CT3ACHLV)** The value of bit 7-0 denotes the LSB tachometer speed.

7.12.4.30 Fan 3 Tachometer MSB Reading (F3TMRR)

When BME is 1, this register reflects the MSB value of the current Frequency of the Backlight from TACH2. The value is shown in 16-bit format.

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer 3 MSB Value (CT3ACHMV)** The value of bit 7-0 denotes the LSB tachometer speed.

7.12.4.31 Zone Interrupt Status Control Register 2 (ZINTSCR2)

Address Offset: 47h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0b	**TACH2 Data-valid Interrupt Enable (T2DIE)** 1: Enable interrupt to CPU when fan 3 tachometer data is valid. 0: Disable interrupt to CPU when fan 3 tachometer data is valid.
1	R/WC	0b	**TACH2 Data-valid Interrupt Clear (T2DIC)** Write one to clear the Interrupt status, which is caused when fan 3 tachometer data is valid; writing zero is ignored.
0	R	0b	**TACH2 Data-valid Interrupt Status (T2DIS)** 1: Fan 3 tachometer data-valid event occurs. 0: Fan 3 tachometer data-valid event does not occur.

7.12.4.32 Tachometer Switch Control Register 2 (TSWCTLR2)

Address Offset: 4Fh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	-	**TACH2 Data-valid Status (T2DVS)** Write one to clear the status, which is caused when TACH2 data is valid; writing zero is ignored. 0: TACH2 data is not valid. 1: TACH2 data is valid.
0	R/W	0b	**TACH2A/TACH2B Channel Selection (T2CHSEL)** This bit controls the channel switch of TACH2A and TACH2B. Notice that the related GPIO ports should be set to the function mode. 0b: Fan 3 tachometer input is set to select TACH2A. 1b: Fan 3 tachometer input is set to select TACH2B.

7.12.4.33 Tachometer Switch Control Register (TSWCTLR)

Address Offset: 48h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	0b	**TACH0A/TACH0B Data-valid Status (T0DVS)** Write one to clear the status, which is caused when TACH0A/TACH0B data is valid; writing zero is ignored. This bit will be cleared when the input is switched by controlling the T0CHSEL bit. 0: TACH0A/TACH0B data is not valid. 1: TACH0A/TACH0B data is valid.
2	R/W	0b	**TACH0A/TACH0B Channel Selection (T0CHSEL)** This bit controls the channel switch of TACH0A and TACH0B. Notice that the related GPIO ports should be set to the function mode. 0b: Fan 1 tachometer input is set to select TACH0A. 1b: Fan 1 tachometer input is set to select TACH0B.
1	R/WC	0b	**TACH1A/TACH1B Data-valid Status (T1DVS)** Write one to clear the status, which is caused when TACH1A/TACH1B data is valid; writing zero is ignored. This bit will be cleared when the input is switched by controlling the T1CHSEL bit. 0: TACH1A/TACH1B data is not valid. 1: TACH1A/TACH1B data is valid.
0	R/W	0b	**TACH1A/TACH1B Channel Selection (T1CHSEL)** This bit controls the channel switch of TACH1A and TACH1B. Notice that the related GPIO ports should be set to the function mode. 0b: Fan 2 tachometer input is set to select TACH1A. 1b: Fan 2 tachometer input is set to select TACH1B.

7.12.4.34 PWM Output Open-Drain Enable Register (PWMODENR)

Address Offset: 49h

Bit	R/W	Default	Description
7	R/W	0b	**PWM7 Output Open-Drain Enable (PWM7ODEN)** This bit controls the output open-drain function of PWM7. Notice that the related GPIO ports should be set to the function mode. 0b: PWM7 output is set to push-pull mode. 1b: PWM7 output is set to open-drain mode.
6	R/W	0b	**PWM6 Output Open-Drain Enable (PWM6ODEN)** This bit controls the output open-drain function of PWM6. Notice that the related GPIO ports should be set to the function mode. 0b: PWM6 output is set to push-pull mode. 1b: PWM6 output is set to open-drain mode.
5	R/W	0b	**PWM5 Output Open-Drain Enable (PWM5ODEN)** This bit controls the output open-drain function of PWM5. Notice that the related GPIO ports should be set to the function mode. 0b: PWM5 output is set to push-pull mode. 1b: PWM5 output is set to open-drain mode.
4	R/W	0b	**PWM4 Output Open-Drain Enable (PWM4ODEN)** This bit controls the output open-drain function of PWM4. Notice that the related GPIO ports should be set to the function mode. 0b: PWM4 output is set to push-pull mode. 1b: PWM4 output is set to open-drain mode.
3	R/W	0b	**PWM3 Output Open-Drain Enable (PWM3ODEN)** This bit controls the output open-drain function of PWM3. Notice that the related GPIO ports should be set to the function mode. 0b: PWM3 output is set to push-pull mode. 1b: PWM3 output is set to open-drain mode.
2	R/W	0b	**PWM2 Output Open-Drain Enable (PWM2ODEN)** This bit controls the output open-drain function of PWM2. Notice that the related GPIO ports should be set to the function mode. 0b: PWM2 output is set to push-pull mode. 1b: PWM2 output is set to open-drain mode.
1	R/W	0b	**PWM1 Output Open-Drain Enable (PWM1ODEN)** This bit controls the output open-drain function of PWM1. Notice that the related GPIO ports should be set to the function mode. 0b: PWM1 output is set to push-pull mode. 1b: PWM1 output is set to open-drain mode.
0	R/W	0b	**PWM0 Output Open-Drain Enable (PWM0ODEN)** This bit controls the output open-drain function of PWM0. Notice that the related GPIO ports should be set to the function mode. 0b: PWM0 output is set to push-pull mode. 1b: PWM0 output is set to open-drain mode.

7.12.4.35 Backlight Duty Register (BLDR)

This register reflects the current duty of the backlight sensor from TACH2.

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R	-	**Current Backlight Duty Value (CBLDV)** The value of bit 7-0 denotes the duty of backlight. Duty cycle = (CBLDV) / 256 X 100% e.g. 00h means the duty range is 0/256~1/256. 01h means the duty range is 1/256~2/256. 02h means the duty range is 2/256~3/256. … FFh means the duty range is 255/256~256/256.

7.12.4.36 PWM0 LED Dimming Enable (PWM0LHE)

Address Offset: 50h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**PWM0 Dimming Enable (PWM0HE)** 0: Disable 1: Enable It is recommended that set PWM0LCR1 and PWM0LCR2 first before enable dimming mode

7.12.4.37 PWM0 LED Dimming Control Register 1 (PWM0LCR1)

Address Offset: 51h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	00b	**PWM0 Dimming Maximum Duty Cycle Select (P0HMXD)** 00b: 40h 01b: 80h 10b: C0h 11b: FFh
3-2	R/W	00b	**PWM0 Duty Decreasing Step (P0DDS)** 00b: 1h 01b: 2h 10b: 4h 11b: 8h
1-0	R/W	00b	**PWM0 Duty Increasing Step (P0DIS)** 00b: 1h 01b: 2h 10b: 4h 11b: 8h

7.12.4.38 PWM0 LED Dimming Control Register 2 (PWM0LCR2)

Address Offset: 52h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**PWM0 Dimming Maximum Duty Cycle Delay Period (P0HMXDD)** 0h: 1/64 s 1h: 1/8 s 2h: 1/4 s 3h: 1/2 s 4h: 1 s 5h: 2 s 6h: 4 s The above time period is calculated by selecting 32.768K clock and no prescaler.
3	-	-	**Reserved**
2-0	R/W	0h	**PWM0 Dimming Zero Duty Cycle Delay Period (P0HZDD)** 0h: 1/64 s 1h: 1/8 s 2h: 1/4 s 3h: 1/2 s 4h: 1 s 5h: 2 s 6h: 4 s The above time period is calculated by selecting 32.768K clock and no prescaler.

7.12.4.39 PWM1 LED Dimming Enable (PWM1LHE)

Address Offset: 53h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**PWM1 Dimming Enable (PWM0HE)** 0: Disable 1: Enable It is recommended that set PWM1LCR1 and PWM1LCR2 first before enable dimming mode

7.12.4.40 PWM1 LED Dimming Control Register 1 (PWM1LCR1)

Address Offset: 54h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	00b	**PWM1 Dimming Maximum Duty Cycle Select (P1HMXD)** 00b: 40h 01b: 80h 10b: C0h 11b: FFh
3-2	R/W	00b	**PWM1 Duty Decreasing Step (P1DDS)** 00b: 1h 01b: 2h 10b: 4h 11b: 8h
1-0	R/W	00b	**PWM1 Duty Increasing Step (P1DIS)** 00b: 1h 01b: 2h 10b: 4h 11b: 8h

7.12.4.41 PWM1 LED Dimming Control Register 2 (PWM1LCR2)

Address Offset: 55h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-4	R/W	0h	**PWM1 Dimming Maximum Duty Cycle Delay Period (P1HMXDD)** 0h: 15.6 ms 1h: 125 ms 2h: 250 ms 3h: 0.5 s 4h: 1 s 5h: 2 s 6h: 4 s The above time period is derived from selecting 32.768K clock and no prescaler.
3	-	-	**Reserved**
2-0	R/W	0h	**PWM1 Dimming Zero Duty Cycle Delay Period (P1HZDD)** 0h: 15.6 ms 1h: 125 ms 2h: 250 ms 3h: 0.5 s 4h: 1 s 5h: 2 s 6h: 4 s The above time period is derived from selecting 32.768K clock and no prescaler.

7.12.4.42 PWM Load Counter Control Register (PWMLCCR)

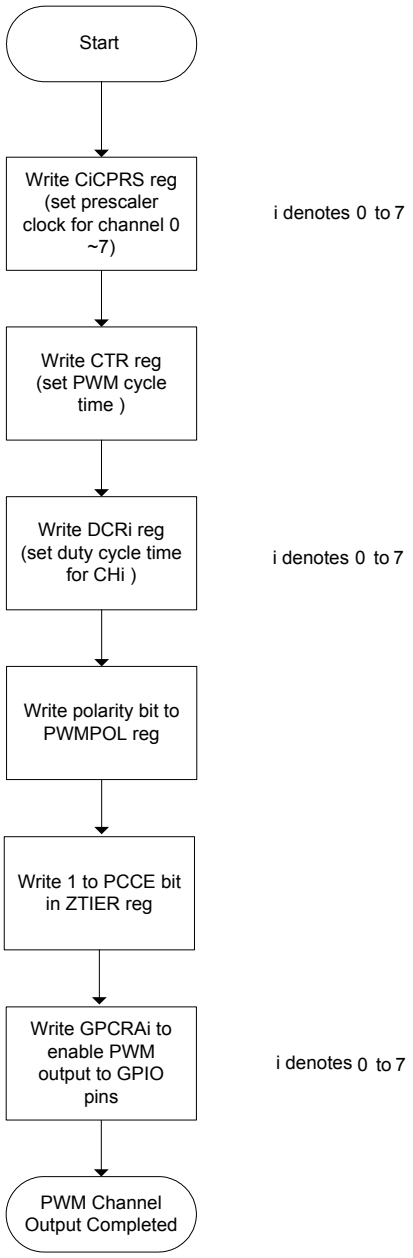
This register controls the way to load the DCR/CTR into the down counter.

Address Offset: 5Ah

Bit	R/W	Default	Description
7	R/W	0b	**PWM7 Load Control (PWM7LC)** 0b: Load DCR7/CTRi into down counter7 when writing data to the register of DCR7/CTRi. 1b: Load CTRi into down counter7 when the down counter counts to zero.
6	R/W	0b	**PWM6 Load Control (PWM6LC)** 0b: Load DCR6/CTRi into down counter6 when writing data to the register of DCR6/CTRi. 1b: Load CTRi into down counter6 when the down counter counts to zero.
5	R/W	0b	**PWM5 Load Control (PWM5LC)** 0b: Load DCR7/CTRi into down counter5 when writing data to the register of DCR5/CTRi. 1b: Load CTRi into down counter5 when the down counter counts to zero.
4	R/W	0b	**PWM4 Load Control (PWM4LC)** 0b: Load DCR4/CTRi into down counter4 when writing data to the register of DCR4/CTRi. 1b: Load CTRi into down counter4 when the down counter counts to zero.
3	R/W	0b	**PWM3 Load Control (PWM3LC)** 0b: Load DCR3/CTRi into down counter3 when writing data to the register of DCR3/CTRi. 1b: Load CTRi into down counter3 when the down counter counts to zero.
2	R/W	0b	**PWM2 Load Control (PWM2LC)** 0b: Load DCR2/CTRi into down counter2 when writing data to the register of DCR2/CTRi. 1b: Load CTRi into down counter2 when the down counter counts to zero.
1	R/W	0b	**PWM1 Load Control (PWM1LC)** 0b: Load DCR1/CTRi into down counter1 when writing data to the register of DCR1/CTRi. 1b: Load CTRi into down counter1 when the down counter counts to zero.
0	R/W	0b	**PWM0 Load Control (PWM0LC)** 0b: Load DCR0/CTRi into down counter0 when writing data to the register of DCR0/CTRi. 1b: Load CTRi into down counter0 when the down counter counts to zero.

7.12.5 PWM Programming Guide

Figure 7-24. Program Flow Chart for PWM Channel Output



7.13 8-bit Timer (TMR)

7.13.1 Overview

This module is an on-chip 8-bit timer (TMA0, TMA1, TMB0, and TMB1) with four channels operating on the basis of an 8-bit counter. The 8-bit timer module can be used as a multi-function timer in a variety of applications, such as generation of counter reset, interrupt requests, and pulse output with an arbitrary duty cycle using a compare-match signal with registers.

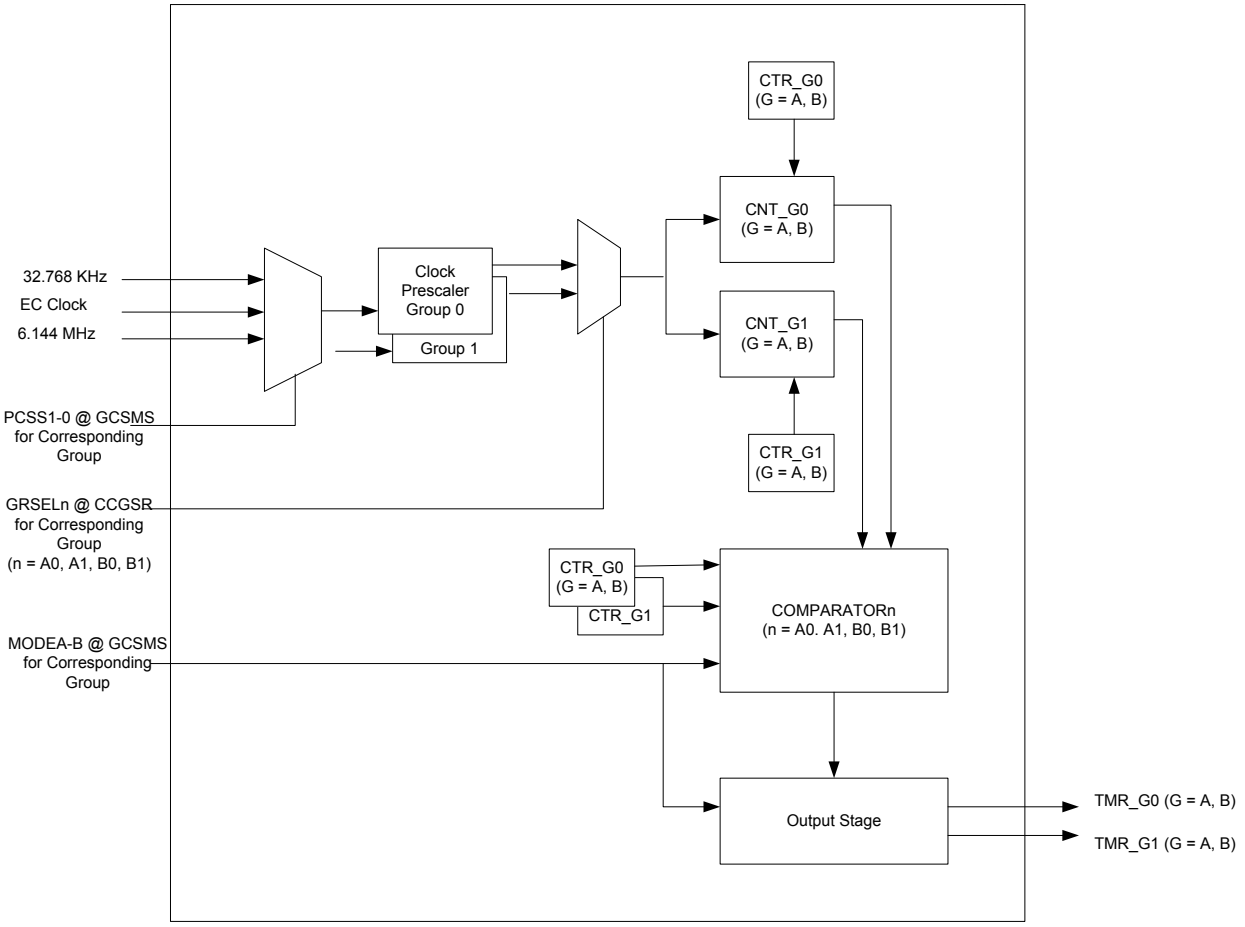
7.13.2 Features

- Supports four channels.
- Supports four Counters, Cycle Time registers and Duty Cycle registers for each channel.
- Supports four clock sources and two clock prescalers.
- Supports 8-bit pulse mode, 16-bit pulse mode, and toggle mode.
- Supports interrupt enable and interrupt disable for cycle time match and duty cycle match respectively.

7.13.3 Functional Description

7.13.3.1 General Description

Figure 7-25. TMR Block Diagram



The TMR uses the 32.768 kHz Clock, EC Clock, or 6.14 MHz Clock as a reference for its TMR output. The prescaler divider values in PRSC register divides the TMR intput clock into its working clock respectively. Each

channel can select their prescaler divider by CCGSR register. The TMR provides four TMR outputs, TMA0 , TMA1, TMB0, and TMB1. Each TMR output is controlled by its Duty Cycle registers and Cycle Time register.

TMR module consists of three modes, 8-bit mode, 16-bit mode, and toggle mode.

7.13.3.2 TMR Counter (CNT)

Each CNT is an 8-bit up-counter. CNT_A0 and CNT_A1 (or CNT_B0 and CNT_B1) comprise a single 16-bit counter in toggle mode or 16-bit pulse mode. CNT can be cleared by writing data to Duty Cycle register or by compare-match Cycle Time signal. Note that CNT is disabled when DCR is 00h and CNT is initialized to 00h.

7.13.3.3 TMR Duty Cycle (DCR)

DCR is an 8-bit readable/writable register. DCR_A0 and DCR_A1 (or DCR_B0 and DCR_B1) comprise a single 16-bit register in toggle mode or 16-bit pulse mode. DCR is continually compared with the value in CNT. When a match is detected, the corresponding TMR output polarity will be changed and the corresponding interrupt will be set if the interrupt is enabled. DCR is initialized to 00h.

7.13.3.4 TMR Cycle Time (CTR)

CTR is an 8-bit readable/writable register. CTR_A0 and CTR_A1 (or CTR_B0 and CTR_B1) comprise a single 16-bit register in toggle mode or 16-bit pulse mode. CTR is continually compared with the value in CNT. When a match is detected, the corresponding TMR output polarity will be changed and the corresponding interrupt will be set if the interrupt is enabled and the value in CNT will be changed to 00h. CTR is initialized to H'FF.

7.13.3.5 TMR Mode

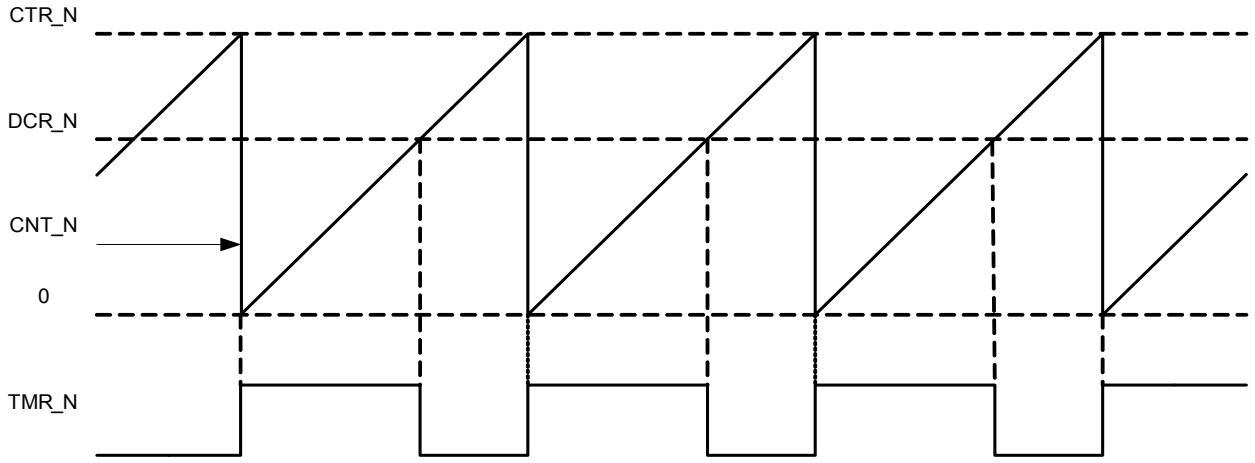
8-bit Pulse Mode
In 8-bit pulse mode, each TMR_N output is controlled by its Duty Cycle register and Cycle Time register.(N = A0, A1, B0, and B1)

When the TMR working clock is enabled, the TMR_N output is high when the value in the DCR_N register is greater than the value in the counter. When the value of DCR_N register is not greater than the value in the counter, the TMR_N cycle output is low. When the value in the counter reaches the value in the CTR_N register, the counter will be reset then start counting until the TMR working clock is disabled.

The TMR_N output signal cycle time is:
Tclk × PRSC0/PRSC1 × (CTR_N + 1)
Where Tclk is the period of TMR intput clock = (1/ 32.768 kHz), (1/ FreqEC) or (1/ 6.14 MHz), which is selected by PCSS1-0 in GCSMS register.

The TMR_N output signal duty cycle (in %) is:
(DCR_N) / (CTR_N + 1) × 100

Figure 7-26. 8-bit Mode Waveform of Channel N



16-bit pulse mode

In 16-bit pulse mode, TMR output is controlled by the cascading of two Duty Cycle registers and two Cycle Time registers.

Operation of a 16-bit counter can be performed by using CNT_G1 as the upper half and CNT_G0 as the lower half, and operation of 16-bit Duty Cycle register (DCR_G) and 16-bit Cycle Time register (CTR_G) is performed in the same way as that of 16-bit counter (CNT_G). (G = A, B)

When the TMR working clock is enabled, the TMR_G1 output is high when the value in the DCR_G register is greater than the value in the CNT_G register. When the value of the DCR_G register is not greater than the value in the CNT_G register, the TMR_G1 output is low. When the value in the CNT_G register reaches the value in the CTR_G register, the CNT_G counter will be reset then start counting until the TMR working clock is disabled. But TMR_G0 output is always low in 16-bit pulse mode.

The TMR_G1 output signal cycle time is:

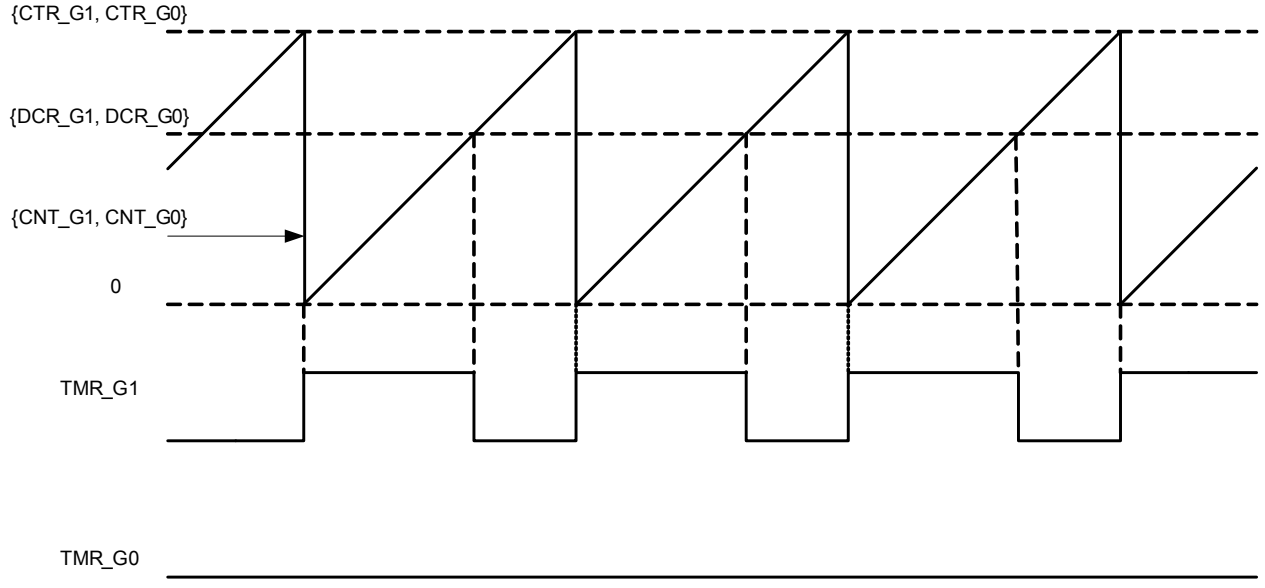
Tclk × PRSC0/PRSC1 × (CTR_G + 1)

Where Tclk is the period of TMR intput clock = (1/ 32.768 kHz), (1/ FreqEC) or (1/ 6.14 MHz), which is selected by PCSS1-0 in GCSMS register.

The TMR_G1 output signal duty cycle (in %) is:

(DCR_G) / (CTR_G + 1) × 100

Figure 7-27. 16-bit Mode Waveform of Group G



Toggle mode

The Counter, Duty Cycle register, and Cycle Time register are cascaded in the same way as that in 16-bit pulse mode.

When TMR working clock is enabled, the TMR_G1 output polarity will be changed at the moment that the value in the CNT_G counter reaches the value in the DCR_G register and the TMR_G0 output polarity will be changed at the moment that the value in the CNT_G counter reaches the value in the CTR_G register. When the value in the CNT_G register reaches the value in the CTR_G register, the CNT_G counter will be reset then start counting until the TMR working clock is disabled.

The TMR_G1 and TMR_G0 output signal cycle time is:

Tclk × PRSC0/PRSC1 × (CTR_G + 1)

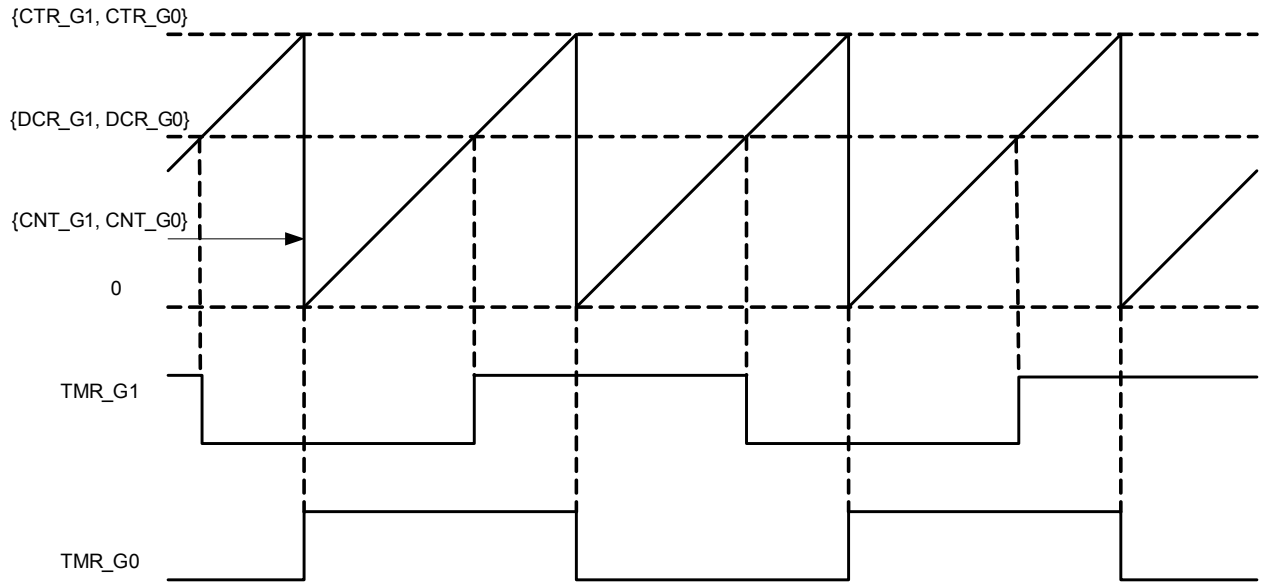
Where Tclk is the period of TMR intput clock = (1/ 32.768 kHz), (1/ FreqEC) or (1/ 6.14 MHz), which is selected by PCSS1-0 in GCSMS register.

The TMR_G1 and TMR_G0 output signal duty cycle (in %) is 50 %.

The phase differential of TMR_G1 and TMR_G0 (in %) is:

(DCR_G) / (CTR_G + 1) × 100

Figure 7-28. 16-bit Mode Waveform of Group N



7.13.3.6 TMR Interrupt

Each TMR output can generate two types of interrupts, Cycle Time compare-match interrupt and Duty Cycle compare-match interrupt. Each interrupt source can be enabled or disabled independently by interrupt enable bits in TMRIE register. Independent signals are sent to the interrupt controller for each interrupt.

For the following three TMR modes, each of the four interrupts, TMRINTA0, TMRINTA1, TMRINTB0, TMRINTB1, has its own specific interrupt sources.

CTR_A = CTR_A1 * 100h + CTR_A0
DCR_A = DCR_A1 * 100h + DCR_A0
CTR_B = CTR_B1 * 100h + CTR_B0
DCR_B = DCR_B1 * 100h + DCR_B0

8-bit Pulse Mode

TMRINTA0: CTR_A0 compare-match and DCR_A0 compare-match sources.
TMRINTA1: CTR_A1 compare-match and DCR_A1 compare-match sources.
TMRINTB0: CTR_B0 compare-match and DCR_B0 compare-match sources.
TMRINTB1: CTR_B1 compare-match and DCR_B1 compare-match sources.

16-bit Pulse Mode

TMRINTA0: No interrupt.
TMRINTA1: CTR_A compare-match and DCR_A compare-match sources.
TMRINTB0: No interrupt.
TMRINTB1: CTR_B compare-match and DCR_B compare-match sources.

Toggle mode

TMRINTA0: CTR_A compare-match source.
TMRINTA1: DCR_A compare match source.
TMRINTB0: CTR_B compare-match source.
TMRINTB1: DCR_B compare match source.

7.13.4 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 2900h.

Table 7-23. EC View Register Map, TMR

7 0	Offset
TMR Prescaler Register (PRSC)	00h
Group Clock Source and Mode Select Register (GCSMS)	01h
A0 Cycle Time Register (CTR_A0)	02h
A1 Cycle Time Register (CTR_A1)	03h
B0 Cycle Time Register (CTR_B0)	04h
B1 Cycle Time Register (CTR_B1)	05h
A0 Duty Cycle Register (DCR_A0)	06h
A1 Duty Cycle Register (DCR_A1)	07h
B0 Duty Cycle Register (DCR_B0)	08h
B1 Duty Cycle Register (DCR_B1)	09h
Channel Clock Group Select Register (CCGSR)	0Ah
TMR Clock Enable Register (TMRCE)	0Bh
TMR Interrupt Enable Register (TMRIE)	0Ch

Other related register(s):
- General Control 2 Register (GCR2), TMB1EN bit
- General Control 2 Register (GCR2), TMB0EN bit
- General Control 2 Register (GCR2), TMA1EN bit
- General Control 2 Register (GCR2), TMA0EN bit

For a summary of the abbreviations of register types, refer to “Register Abbreviations and Access Rules”

7.13.4.1 TMR Prescaler Register (PRSC)

This register controls the cycle time and the minimal pulse width of TMR channel.

Address Offset: 00h

Bit	R/W	Default	Description
7-4	R/W	0000b	**TMR Prescaler Divider Value 1 (PRSC1)** PWM input clock is divided by the number of PRSC1. 0000: clk disabled. 1000: clk/128. 0001: clk. 1001: clk/256. 0010: clk/2. 1010: clk/512. 0011: clk/4. 1011: clk/1024. 0100: clk/8. 1100: clk/2048. 0101: clk/16. 1101: clk/4096. 0110: clk/32. 1110: clk/8192. 0111: clk/64. 1111: clk/16384. Where clk is the clock source selected by PCSS1 field in GCSMS register.
3-0	R/W	0000b	**TMR Prescaler Divider Value 0 (PRSC0)** Bit 3-0 are the same as bit 7-4

7.13.4.2 Group Clock Source and Mode Select Register (GCSMS)

This register selects the clock source and mode.

Address Offset: 01h

Bit	R/W	Default	Description
7-6	R/W	00b	**Group B Mode (MODEB)** Select the mode of TMB0 and TMB1. 00: 8-bit pulse mode. 01: 16-bit pulse mode. 10: Toggle mode. 11: The same as 10.
5-4	R/W	00b	**Group A Mode (MODEA)** Select the mode of TMA0 and TMA1. Bit 5-4 are the same as bit 7-6.
3-2	R/W	00b	**Prescaler 1 Clock Source Select (PCSS1)** 00b: Select 32.768 kHz. 01b: Select FreqEC (EC Clock). 10b: Select FreqEC*2/3 (6.14 MHz) 11b: Reserved (FreqEC and FreqPLL are listed in Table 10-2 on page 530)
1-0	R/W	00b	**Prescaler 0 Clock Source Select (PCSS0)** Bit 1-0 are the same as bit 3-2

7.13.4.3 A0 Cycle Time Register (CTR_A0)

This register controls the cycle time of channel A0.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value A0 (CTVA0)** The Prescaler output clock is divided by the number of (CTR_A0 +1). For example, the value of 00h results in a divide by 1. The value of FFh results in a divided by 256.

7.13.4.4 A1 Cycle Time Register (CTR_A1)

This register controls the cycle time of channel A1.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value A1 (CTVA1)** The function of this register is the same as that of CTR_A0.

7.13.4.5 B0 Cycle Time Register (CTR_B0)

This register controls the cycle time of channel B0.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value B0 (CTVB0)** The function of this register is the same as that of CTR_A0.

7.13.4.6 B1 Cycle Time Register (CTR_B1)

This register controls the cycle time of channel B1.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value B1 (CTVB1)** The function of this register is the same as that of CTR_A0.

7.13.4.7 A0 Duty Cycle Register (DCR_A0)

This register controls the duty cycle of channel A0.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value A0 (DCVA0)** DCR_A0 register decides the number of clocks for the waveform of the corresponding TMR output.

7.13.4.8 A1 Duty Cycle Register (DCR_A1)

This register controls the duty cycle of channel A1.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value A1 (DCVA1)** The function of this register is the same as that of DCR_A0.

7.13.4.9 B0 Duty Cycle Register (DCR_B0)

This register controls the duty cycle of channel B0.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value B0 (DCVB0)** The function of this register is the same as that of DCR_A0.

7.13.4.10 B1 Duty Cycle Register (DCR_B1)

This register controls the duty cycle of channel B1.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value B1 (DCVB1)** The function of this register is the same as that of DCR_A0.

7.13.4.11 Channel Clock Group Select Register (CCGSR)

This register selects the clock group of TMR output.

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R	0b	**TMR B1 Reading Register (RDB1)** Read Channel B1 if TMR output pins are used by other modules.
6	R	0b	**TMR B0 Reading Register (RDB0)** Bit 6 is the same as bit 7.
5	R	0b	**TMR A1 Reading Register (RDA1)** Bit 5 is the same as bit 7.
4	R	0b	**TMR A0 Reading Register (RDA0)** Bit 4 is the same as bit 7.
3	R/W	0b	**TMR B1 Clock Group Select Register (GRSELB1)** Select the clock group of channel B1. 0: Select Clock PRSC0. 1: Select Clock PRSC1.
2	R/W	0b	**TMR B0 Clock Group Select Register (GRSELB0)** Bit 2 is the same as bit 3 In the 16-bit pulse mode or toggle mode, this bit is of no use and the clock group of TMR B0 will be the same as TMR B1.
1	R/W	0b	**TMR A1 Clock Group Select Register (GRSELA1)** Bit 1 is the same as bit 3.
0	R/W	0b	**TMR A0 Clock Group Select Register (GRSELA0)** Bit 0 is the same as bit 3. In the 16-bit pulse mode or toggle mode, this bit is of no use and the clock group of TMR A0 will be the same as TMR A1.

7.13.4.12 TMR Clock Enable Register (TMRCE)

This register selects the clock group of TMR output.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**TMR Clock Enable Register (CLKEN)** 1: Enable TMR clock counter. Set this bit to 1 after all other registers have been set. 0: Disable TMR clock counter.
0	R/W	0b	**TMR Test Mode (TMRTM)** 1: The mode of TMR is switched to a test mode. 0: TMR works in a normal mode.

7.13.4.13 TMR Interrupt Enable Register (TMRIE)

This register controls the interrupt enable of all TMR channels.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0b	**TMR B1 Duty Cycle Interrupt Enable Register (B1DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable **In toggle mode:** This bit controls the duty cycle compare-match interrupt enable.
6	R/W	0b	**TMR B1 Cycle Time Interrupt Enable Register (B1CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In toggle mode:** This bit is of no use.
5	R/W	0b	**TMR B0 Duty Cycle Interrupt Enable Register (B0DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit is of no use. **In toggle mode:** This bit is of no use.
4	R/W	0b	**TMR B0 Cycle Time Interrupt enable Register (B0CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** The bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** The bit is of no use. **In toggle mode:** The bit controls the cycle time compare-match interrupt enable.
3	R/W	0b	**TMR A1 Duty Cycle Interrupt enable Register (A1DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable **In toggle mode:** This bit controls the duty cycle compare-match interrupt enable.

Bit	R/W	Default	Description
2	R/W	0b	**TMR A1 Cycle Time Interrupt enable Register (A1CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In toggle mode:** This bit is of no use.
1	R/W	0b	**TMR A0 Duty Cycle Interrupt enable Register (A0DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit is of no use **In toggle mode:** This bit is of no use.
0	R/W	0b	**TMR A0 Cycle Time Interrupt enable Register (A0CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** This bit is of no use. **In toggle mode:** This bit controls the cycle time compare-match interrupt enable.

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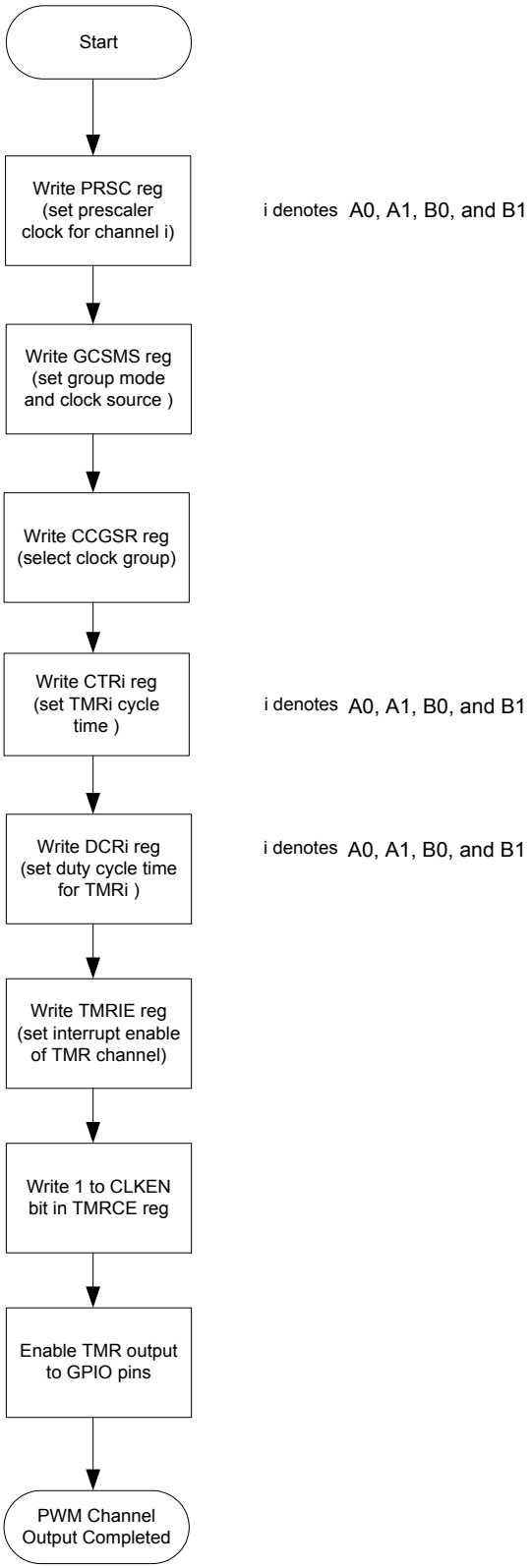
Figure 7-29. Program Flow Chart for TMR Channel Output



7.14 Consumer Electronics Control (CEC)

7.14.1 Overview

CEC provides a number of high-level control functions within a HDMI system. Several CEC features are designed to enhance interoperability between the varios audiovisual products in a user's environment.

7.14.1.1 General Description

CEC bus is a single wire and bi-direction signal. All the related transmission protocol and bit timing specfication follow the HDMI 1.4a standard. F/W can use the frame-based data transmission to construct any CEC protocol which CEC device really supports. A CEC frame consists of a "Start bit", a "Header Block" and successive "Data Block". The "Data Block" and "Header Block" are the same structure which has 8-bit information bits plus two control bits "EOM" and "ACK".

There is a FFIO provided for continuity of successive bit transmitting. F/W can monitor FIFO status to control the flow of frame transmission. If device operates in the initiator mode, F/W should define Header Information in first byte of FIFO then the bytes afterward are Data. And switch device to intiator mode by register DMS, then writing 1 to register ICC to fire CEC frame.

Initial setting for CEC function: INT82 Enable, GPIOF0 set alternate function mode, CECEN, Enable CEC clock , CEC Interrup Enable Register(CECIE).

Set logical device address (CECDLA) to decide Device Type when operating in followr mode.

7.14.1.2 CEC TX Flow

If CEC operates in initiator mode and want to transimit 2 byte, include header.(1 header + 1 data)
1. Write header information into FIFO
2. Write data byte into FIFO
3. Switch Device to Initiator mode
4. Issue CEC frame by writing 1 to bit ICC.
5. Wait Interrupt. If transmitting normally, status DBD will be set high
6. Set EOM high to terminate this transfer.
7. Wait Interrupt. If transmitting normally, status DBD will be set high
8. When last byte is transmitted. CEC will auto switch to follower mode.

7.14.1.3 CEC RX Flow

1. Wait interrupt. If header receives normally, status HDRCV will be set high
2. F/W read CECRH to get header information which is sent from initiator device.
3. Wait interrupt. If the following data receives normally
4. F/W could check FFCNT to monitor how many data bytes are received.
5. Read CECDR to get data byte which is sent from initiator device.
6. F/W also monitor EB@CECOPSTS to know when the initiator want to terminate this transfer.
7. Follower can response nack during ACK bit by setting NKEN, however default response is ack.

7.14.2 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 2E00h.

Table 7-24. EC View Register Map, CEC

7 — 0	Offset
CEC Data Register (CECDR)	00h
CEC FIFO Status Register (CECFSTS)	01h
CEC Device Logical Address Register (CECDLA)	02h
CEC Control Register (CECCTRL)	03h
CEC Status Register (CECSTS)	04h
CEC Interrupt Enable Register (CECIE)	05h
CEC Operation Status Register (CECOPSTS)	06h
CEC Received Header Register (CECRH)	07h

7.14.2.1 CEC Data Register (CECDR)

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**CEC Data Buffer (CECDB)** TX/RX Data Byte

7.14.2.2 CEC FIFO Status Register (CECFSTS)

Address Offset: 01h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	-	**FIFO Clear (FCLR)** 0: no action 1: Clear FIFO content.
5	R	-	**FIFO Empty (FE)** 0: FIFO is not empty 1: FIFO is empty
4	R	-	**FIFO Full (FF)** 0: FIFO is not full 1: FIFO is full
3	-	-	**Reserved**
2-0	R	-	**FIFO Count (FCNT)** 0h: FIFO is empty 1h: FIFO has 1 byte 2h: FIFO has 2 bytes 3h: FIFO has 3 bytes 4h: FIFO has 4 bytes (FIFO is full) 5h,6h,7h: Reserved

7.14.2.3 CEC Device Logical Address Register (CECDLA)

Address Offset: 02h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0h	**Device Logical Address (DLA)** Use CEC logical address to define Device Type. Default is TV device.

7.14.2.4 CEC Control Register (CECCTRL)

Address Offset: 03h

Bit	R/W	Default	Description
7-6	R/W	-	**Reserved**
5	R/W	0b	**NACK Enable (NKEN)** 0: response ACK 1: response NACK When device is in Follower mode, setting this bit to ACK or NACK the current receiving byte.
4	R/W	0b	**EOM Bit Enable(EOM)** 0: one block follows 1: final block When device is in Initiator mode, setting this bit to indicate whether the current transmitting byte is final or not
3	R/W	1b	**Normal Bit Timing (NBT)** 0: increase 0.1ms 1:normal Increase bit timing period by around 01ms
2	-	-	**Reserved**
1	-	-	**Reserved**
0	W	0b	**Issue CEC Cycle (ICC)** Write 1 to transmit the Data Bytes that have been written into FIFO. Ignore write 0

7.14.2.5 CEC Status Register (CECSTS)

Address Offset: 04h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5	R/WC	0b	**Header Received (HDRCV)** 0: no event occur 1: even occurs Event occurs upon a “Start bit” plus “Header block” are received and CEC is in Follower mode.
4	R/WC	0b	**Data Block Done (DBD)** 0: no event occur 1: even occurs Event occurs when a “Data block” are transmitted or received.

Bit	R/W	Default	Description
3	R/WC	0b	**CEC Line Error (CLE)** 0: no event occur 1: even occurs Event occurs upon detecting that the period between falling edges of a bit is less than the minimum bit period and CEC is in Follower mode.
2	R/WC	0b	**CEC Error Notified (CEN)** 0: no event occur 1: even occurs Even occurs upon a low bit period on CEC line of 1.4 - 1.6 times the nominal data bit period is generating from follower device. (while CEC is in Initiator mode)
1	R/WC	0b	**BUS Low Error (BLE)** 0: no event occur 1: even occurs Event occurs upon detecting a low status on CEC line while it is transmitting a high status on bus and CEC is in Initiator mode.
0	R/WC	0b	**Bit Timing Error (BTE)** 0: no event occur 1: even occurs Event occurs upon receiving an invalid bit timing while CEC is in Follower mode.

7.14.2.6 CEC Interrupt Enable Register (CECIE)

Address Offset: 05h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6			**Reserved**
5	R/W	0b	**Header Received Interrupt Enable (HDRCVIE)** 0: Disable 1: Enable
4	R/W	0b	**Data Block Done Interrupt Enable (DBDIE)** 0: Disable 1: Enable
3	R/W	0b	**CEC Line Error Interrupt Enable (CLEIE)** 0: Disable 1: Enable
2	R/W	0b	**CEC Error Notified Interrupr Enable (CENIE)** 0: Disable 1: Enable
1	R/W	0b	**BUS Low Error Interrupt Enable (BLEIE)** 0: Disable 1: Enable
0	R/W	0b	**Bit Timing Error Interrup Enable (BTEIE)** 0: Disable 1: Enable

7.14.2.7 CEC Operation Status Register (CECOPSTS)

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R/W	00h	**Reserved**
5	R/W	0b	**CEC Follower Line Control (CFLCTL)** 0: release bus 1: drive bus low When device is in Follower mode, write one to this bit can make CEC lind drive to low state. Write zero would release CEC line.
4	R/W	0b	**Initiator Broadcast Enable (IBE)** When device is in initiator mode, write 1 to this bit before issuing a broadcast message.
3	R/W	0b	**Device Mode Select (DMS)** 0: Follower mode 1: Initiator mode
2	R	0b	**EOM Bit (EB)** EOM status from initiator while device is in Follower mode
1	R	1b	**ACK Bit (AB)** ACK status from follower while device is in Initiator mode
0	R	0b	**CEC In Process (CIP)** 0: CEC write cycle is not in process. 1: After “Issue CEC Cycle”, CEC write cycle is in process

7.14.2.8 CEC Received Header Register (CECRH)

Address Offset: 07h

Bit	R/W	Default	Description
7-4	R/W	0h	**Initiator address (IADDR)** Received Header[7:4] from initiator while CEC is in Follower mode
3-0	R/W	0h	**Destination address (DADDR)** Received Header[3:0] from initiator while CEC is in Follower mode

7.15 EC Access to the Host Controlled Modules (EC2I Bridge)

7.15.1 Overview

The module enables EC access to PNPCFG and SWUC modules. It can access the host domain modules with host on alternate usage.

7.15.2 Features

- Supports Super I/O I-Bus arbitration

7.15.3 Functional Description

The EC2I bridge enables the EC to access the Host Controlled module registers (e.g., host configuration module(PNPCFG) and SWUC).

For EC Read Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write 1 to CRIB bit in IBCTL register.
6. Read the CRIB bit in IBCTL until it returns 0.
7. Read the data from IHD register.

For EC Write Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write the data to IHD register, which begins a write transaction.
6. Read the CWIB bit in IBCTL until it returns 0, which represents that a write transaction has been finished.

For minimal conflict between host and EC in the use of Host Controlled modules, refer to the followings.

7.15.4 EC Interface Registers

The following set of registers is accessible only by the EC. The registers are maintained by VSTBY.
The registers are listed below and the base address is 1200h.

Table 7-25. EC View Register Map, EC2I

7	0	Offset
Indirect Host I/O Address Register (IHIOA)		00h
Indirect Host Data Register (IHD)		01h
EC to I-Bus Modules Access Enable Register (IBMAE)		04h
I-Bus Control Register (IBCTL)		05h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”.

7.15.4.1 Indirect Host I/O Address Register (IHIOA)

This register defines the host I/O address for read or write transactions initiated by EC from/to the Host Controlled modules. The I/O address is an offset from the LSB bits of the address of the host controlled module. The accessed module is selected using EC to I-Bus Modules Access Enable Register (IBMAE).

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Indirect Host I/O Offset (IHIOO)** These bits indicate the offsets within the device range are allowed.

7.15.4.2 Indirect Host Data Register (IHD)

This register holds host data for read or write transactions initiated by EC from/to the Host Controlled modules.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Indirect Host Data (IHDA)**

7.15.4.3 EC to I-Bus Modules Access Enable Register (IBMAE)

This register enables EC access to the Host Controlled modules. Only one of the bits in this register may be set at a time.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	0b	**Mobile System Wake-Up Control (SWUC) Access Enable (SWUCAE)** 0: EC access to the SWUC Registers is disabled. 1: EC access to the SWUC Registers is enabled.
1	R/W	0b	**Real-time Clock (RTC) EC Access Enable (RTCAE)** 0: EC access to the RTC Registers is disabled. 1: EC access to the RTC Registers is enabled.
0	R/W	0b	**PNPCFG Register EC Access Enable (CFGAE)** 0: EC access to the PNPCFG Registers is disabled. 1: EC access to the PNPCFG Registers is enabled.

7.15.4.4 I-Bus Control Register (IBCTL)

This register allows EC to the I-Bus Bridge operation.

Address Offset: 05h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	-	-	**Reserved**
2	R	0b	**EC Write to I-Bus (CWIB)** Read: 1: EC write-access is still processing with IHD register. 0: It's completed.
1	R/W	0b	**EC Read from I-Bus (CRIB)** Write: See also CSAE bit definition. Read: 1: EC read-access is still processing. 0: It's completed and IHD register is available.
0	R/W	0b	**EC to I-Bus Access Enabled (CSAE)** 0: EC access to the I-Bus is disabled (default). 1: EC access to the I-Bus is enabled. The module to be accessed is selected in the IBMAE register. If 1 is written to both CSAE and CRIB, this access is a read-action. If 1 is written to CSAE and 0 to CRIB, this access is a write-action. If 0 is written to CSAE, the internal state machine of accessing is stopped.

7.15.5 EC2I Programming Guide

The read/write cycles PNPCFG and SWUC modules via EC2I are only valid when VCC is supplied. It means that such cycles may be executed after every VCC power-on.

Figure 7-30. Program Flow Chart for EC2I Read

Program flow chart for EC2I Read

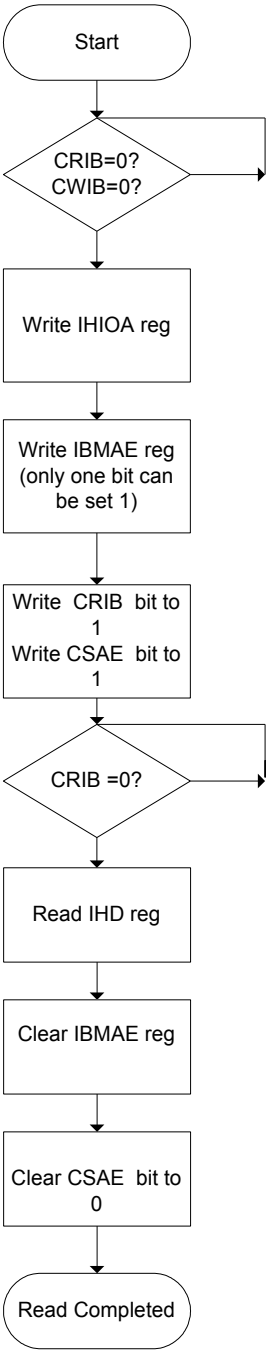
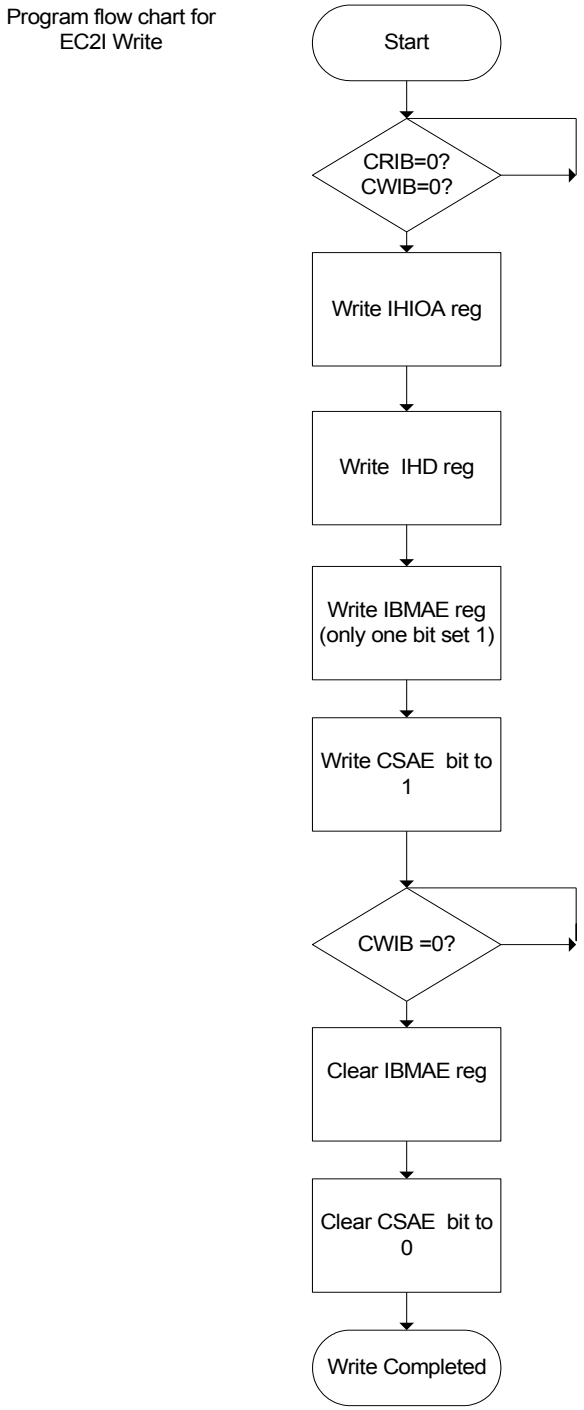


Figure 7-31. Program Flow Chart for EC2I Write



7.16 External Timer and External Watchdog (ETWD)

7.16.1 Overview

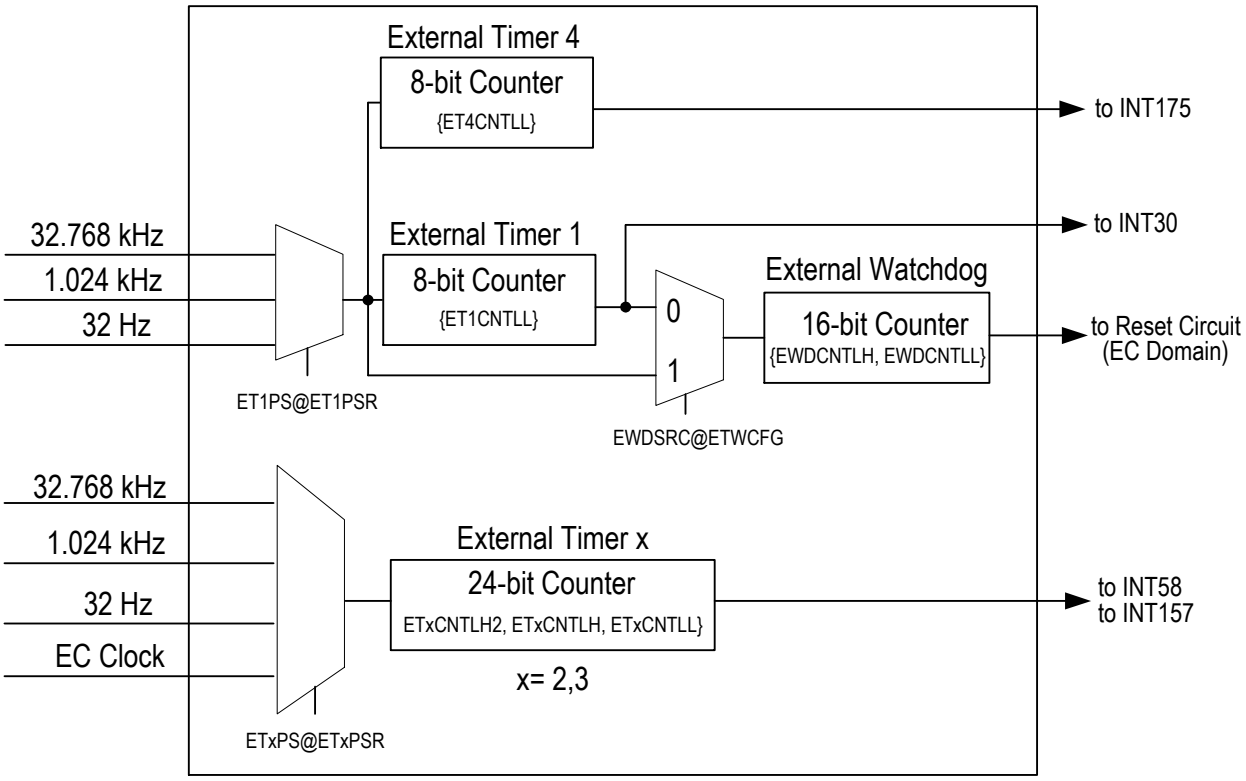
IT5121 implements 4 external timers outside CPU. External timer 1, 4 can function as a watchdog timer (WDT) as well and the other 2 timers are without WDT function. All 4 timers are based on 32.768 k clock and still work when EC is in the Doze/Deep Doze/Sleep mode.

ETWD module cannot count external signal sources from pins. If the firmware wants to count external signal sources from pins, refer to TACH0A/B and TACH1A/B. TACH0/1 are tachometer inputs of PWM.

7.16.2 Features

- 32.768 kHz, 1.024 kHz and 32 Hz prescaler for External Timer 1, 4
- 32.768 kHz, 1.024 kHz, 32 Hz, and 9.2 MHz prescaler for External Timer 2, 3
- 8-bit count-down External Timer 1, 4
- 24-bit count-down External Timer 2, 3
- 16-bit count-down External WDT

Figure 7-32. ETWD Simplified Diagram



7.16.3 Functional Description

7.16.3.1 External Timer Operation

External Timer 1, 4 are 8-bit counter down timers, while External Timer 2, 3 are 24-bit count-down timers. Its clock source is based on 32.768 k Clock and can be selected by a prescaler defined at ETxPS/ETxPS field in ETxPSR/ETxPSR register.

The count number of External Timer 1, 4 is defined in ET1CNTLL and ET4CNTLL registers, and that of External

Timer 2/3 is defined in ETxCNTLH2, ETxCNTLH, and ETxCNTLL registers. External Timer 1, 2, 3, 4 are stopped after reset and started after writing data to ET1CNTLL/ET2CNTLL/ET3CNTLL register and never stops until reset. It asserts an interrupt to INTC (INT30 for External Timer 1; INT58 for External Timer 2; INT157 for External Timer 3; INT175 for External Timer 4) when it counts to zero every time.

External Timer 1/2/3/4 re-starts when
- it counts to zero periodically.
- data is written to ET1CNTLL/ET2CNTLL/ET3CNTLL/ET4CNTLL register.
- 1 is written to ET1RST/ET2RST/ET3RST/ET4RST bit in ETWCTRL register.

External Timer 1/2/3/4 asserts periodical interrupt to EC CPU via INT30/INT58/INT157/INT175 of INTC.

7.16.3.2 External WDT Operation

External WDT is a 16-bit counter down timer. Its clock source is either External Timer 1 output or the same clock source of External Timer 1, and it is controlled by EWDSRC bit in ETWCFG register.
The count number is defined in EWDCNTLH and EWDCNTLL registers. External WDT is stopped after reset and started after writing data to EWDCNTLL register and can be stopped by setting EWDSCEN bit and EWDSCMS bit in ETWCTRL register. It asserts an External Watchdog Reset to EC domain when it counts to zero. External WDT requires starting External Timer 1 regardless of EWDSRC field in ETWCFG register. External WDT cannot be started until External Timer 1 is started.

The External WDT re-starts when it is touched by the firmware.
There are two following ways to touch (re-start) External WDT:
- Writing data to EWDCNTLL register (if LEWDCNTL bit in ETWCFG register is not set)
- Writing 5Ch to EWDKEYR register, called key-match

External WDT asserts an External Watchdog Reset to EC domain when
- it counts to zero.
- data except 5Ch is written to EWDKEYR register.

7.16.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 1F00h.

Table 7-26. EC View Register Map, ETWD

7 — 0	Offset
External Timer 1/WDT Configuration Register (ETWCFG)	01h
External Timer 1 Prescaler Register (ET1PSR)	02h
Reserved	03h
External Timer 1 Counter High Byte (ET1CNTLHR)	03h
External Timer 1 Counter Low Byte (ET1CNTLLR)	04h
External Timer 2 Prescaler Register (ET2PSR)	0Ah
External Timer 2 Counter High Byte (ET2CNTLHR)	0Bh
External Timer 2 Counter Low Byte (ET2CNTLLR)	0Ch
External Timer 2 Counter High Byte 2 (ET2CNTLH2R)	0Eh
External Timer 3 Prescaler Register (ET3PSR)	10h
External Timer 3 Counter High Byte (ET3CNTLHR)	11h
External Timer 3 Counter Low Byte (ET3CNTLLR)	12h
External Timer 3 Counter High Byte 2 (ET3CNTLH2R)	13h
External Timer 4 Counter Low Byte (ET4CNTLLR)	16h
External Timer / WDT Control Register (ETWCTRL)	05h
External WDT Counter High Byte (EWDCNTLHR)	09h
External WDT Counter Low Byte (EWDCNTLLR)	06h

7	0	Offset
External WDT Key Register (EWDKEYR)		07h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

7.16.4.1 External Timer 1/WDT Configuration Register (ETWCFG)

Address Offset: 01h

Bit	R/W	Default	Description
7-6	-	0b	**Reserved**
5	R/W	0b	**External WDT Key Enabled (EWDKEYEN)** 1: Enable the key match function to touch the WDT. 0: Otherwise.
4	R/W	0b	**External WDT Clock Source (EWDSRC)** 1: Select clock after prescaler of External Timer 1. 0: Select clock from the output of External Timer 1.
3	R/W	0b	**Lock EWDCNTLx Register (LEWDCNTL)** 1: Writing to EWDCNTL is ignored. 0: Writing to EWDCNTL is allowed.
2	R/W	0b	**Lock ET1CNTLx Registers (LET1CNTL)** 1: Writing to ET1CNTLL is ignored. 0: Writing to ET1CNTLL is allowed.
1	R/W	0b	**Lock ET1PS Register (LET1PS)** 1: Writing to ET1PS is ignored. 0: Writing to ET1PS is allowed.
0	R/W	0b	**Lock ETWCFG Register (LETWCFG)** 1: Writing to ETWCFG itself is ignored, and this bit can’t be cleared until reset. 0: Writing to ETWCFG itself is allowed.

7.16.4.2 External Timer 1 Prescaler Register (ET1PSR)

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1-0	R/W	00b	**External Timer 1 Prescaler Select (ET1PS)** These bits control the clock input source to External Timer 1 and 4. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: Reserved Note the prescaler will not output clock until data is written to ET1CNTLLR register.

7.16.4.3 External Timer 1 Counter Low Byte (ET1CNTLLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 1 Counter Low Byte (ET1CNTLL)** Define the count number of the 8-bit count-down timer. External Timer 1 starts or re-starts after writing this register.

7.16.4.4 External Timer 2 Prescaler Register (ET2PSR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 2 Prescaler Select (ET2PS)** These bits control the clock input source to the external timer 2. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: 9.2 MHz Note the prescaler will not output clock until data is written to ET2CNTLLR register.

7.16.4.5 External Timer 2 Counter High Byte (ET2CNTLHR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter High Byte (ET2CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.16.4.6 External Timer 2 Counter Low Byte (ET2CNTLLR)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter Low Byte (ET2CNTLL)** Define the count number of low byte of the 24-bit count-down timer. External Timer 2 starts or re-starts after writing this register.

7.16.4.7 External Timer 2 Counter High Byte 2 (ET2CNTLH2R)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter High Byte 2 (ET2CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.16.4.8 External Timer 3 Prescaler Register (ET3PSR)

Address Offset: 10h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 3 Prescaler Select (ET3PS)** These bits control the clock input source to External Timer 3. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: 9.2 MHz Note the prescaler will not output the clock until data is written to ET3CNTLLR register.

7.16.4.9 External Timer 3 Counter High Byte (ET3CNTLHR)

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter High Byte (ET3CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.16.4.10 External Timer 3 Counter Low Byte (ET3CNTLLR)

Address Offset: 12h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter Low Byte (ET3CNTLL)** Define the count number of low byte of the 24-bit count-down timer. External Timer 3 starts or re-starts after data is written to this register.

7.16.4.11 External Timer 3 Counter High Byte 2 (ET3CNTLH2R)

Address Offset: 13h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 3 Counter High Byte 2 (ET3CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.16.4.12 External Timer 4 Counter Low Byte (ET4CNTLLR)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 4 Counter Low Byte (ET4CNTLL)** Define the count number of the 8-bit count-down timer. External Timer 4 starts after writing data to ET1CNTLLR. External Timer 4 re-starts after writing data to this register.

7.16.4.13 External Timer / WDT Control Register (ETWCTRL)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	-	**External Timer 3 Terminal Count (ET3TC)** Read only. 1: Indicates External Timer 3 has counted down to zero, and it is cleared after reading it. 0: Otherwise. **External Timer 3 Reset (ET3RST)** Write only. Writing 1 forces External Timer 3 to re-start. Writing 0 is ignored.
6	R/W	-	**External Timer 4 Terminal Count (ET4TC)** Read only. 1: Indicates External Timer 4 has counted down to zero, and it is cleared after reading it. 0: Otherwise. **External Timer 4 Reset (ET4RST)** Write only. Writing 1 forces External Timer 4 to re-start. Writing 0 is ignored.
5	R/W	0b	**External WDT Stop Count Enable (EWDSCEN)** 1: External WDT is stopped counting. 0: Otherwise. This bit cannot be set until EWDSCMS bit is set to 1.
4	R/W	0b	**External WDT Stop Count Mode Select (EWDSCMS)** 1: External WDT can be stopped by setting EWDSCEN bit. 0: External WDT cannot be stopped. Writing data to this bit is ignored after writing data to EWDCNTLL register, and this bit cannot be cleared until being reset.
3	R	0b	**External Timer 2 Terminal Count (ET2TC)** 1: Indicates the External Timer 2 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing data to this bit is ignored.
2	W	-	**External Timer 2 Reset (ET2RST)** Writing 1 forces the External Timer 2 to re-start. Writing 0 is ignored. Read always returns zero.
1	R	0b	**External Timer 1 Terminal Count (ET1TC)** 1: Indicates External Timer 1 has counted down to zero, and it is cleared after reading it. 0: Otherwise Writing data to this bit is ignored.
0	W	-	**External Timer 1 Reset (ET1RST)** Writing 1 forces External Timer 1 to re-start. Writing 0 is ignored. Read always returns zero.

7.16.4.14 External WDT Counter High Byte (EWDCNTLHR)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**External WDT Counter High Byte (EWDCNTL)** Define the count number of high byte of the 16-bit count-down WDT.

7.16.4.15 External WDT Counter Low Byte (EWDCNTLLR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0Fh	**External WDT Counter Low Byte (EWDCNTLL)** Define the count number of 16-bit count-down WDT.

7.16.4.16 External WDT Key Register (EWDKEYR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	W	-	**External WDT Key (EWDKEY)** External WDT is re-started (touched) if 5Ch is written to this register. Writing with other values causes an External Watchdog Reset. This function is enabled by EWDKEYEN bit. Read returns unpredictable value.

7.17 General Control (GCTRL)

7.17.1 Overview

This module controls EC function that doesn't belong to the specified module.

7.17.2 Features

- By module reset

7.17.3 Functional Description

Wait Next Clock Rising:
When writing 0 WNCKR register, the CPU will be paused and wait for a low to high transition of the internal 65.536 kHz clock. This may be useful to get a delay.

For a loop that writing 0 to WNCKR register for N times, the delay value will be
((N-1) / 65.536 kHz) to (N / 65.536 kHz)

e.g.
Consecutively writing 0 to WNCKR register for 33 times get 0.5ms delay with –2.3% ~ +0.7% tolerance.
Consecutively writing 0 to WNCKR register for 66 times get 1ms delay with –0.8% ~ +0.7% tolerance.
Consecutively writing 0 to WNCKR register for 132 times get 2ms delay with –0.05% ~ +0.7% tolerance.

7.17.4 EC Interface Registers

The following set of the registers is accessible only by EC. They are listed below and the base address is 2000h.

Table 7-27. EC View Register Map, GCTRL

7 0	Offset
Chip ID Byte 1 (ECHIPID1)	00h
Chip ID Byte 2 (ECHIPID2)	01h
Chip Version (ECHIPVER)	02h
Reserved	03h
Identify Input Register (IDR)	04h
Reserved	05h
Reset Status (RSTS)	06h
Reset Control 1 (RSTC1)	07h
Reset Control 2 (RSTC2)	08h
Reset Control 3 (RSTC3)	09h
Reset Control 4 (RSTC4)	11h
Reset Control DMM (RSTDMMC)	10h
Reset Control 6 (RSTC6)	29h
Base Address Select (BADRSEL)	0Ah
Wait Next Clock Rising (WNCKR)	0Bh
Special Control 5 (SPCTRL5)	0Ch
Special Control 1 (SPCTRL1)	0Dh
Reset Control Host Side (RSTCH)	0Eh
Generate IRQ (GENIRQ)	0Fh
Special Control 2 (SPCTRL2)	12h
Special Control 3 (SPCTRL3)	16h
Port I2EC High-Byte Register (PI2ECH)	14h
Port I2EC Low-Byte Register (PI2ECL)	15h
BRAM Interrupt Address 0 Register (BINTADDR0R)	19h
BRAM Interrupt Address 1 Register (BINTADDR1R)	1Ah

7	0	Offset
BRAM Interrupt Control Register (BINTCTRLR)		1Bh
Special Control 4 (SPCTRL4)		1Ch
Port 80h/81h Status Register (P80H81HSR)		30h
Port 80h Data Register (P80HDR)		31h
Port 81h Data Register (P81HDR)		32h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”.

7.17.4.1 Chip ID Byte 1 (ECHIPID1)

The content of this EC side register is the same as that of the CHIPID1 register in the host side.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	51h	**Chip ID Byte 1 (ECHIPID1)** This register contains the Chip ID byte 1.

7.17.4.2 Chip ID Byte 2 (ECHIPID2)

The content of this EC side register is the same as that of the CHIPID2 register in the host side.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R	21h	**Chip ID Byte 2 (ECHIPID2)** This register contains the Chip ID byte 2.

7.17.4.3 Chip Version (ECHIPVER)

This register contains revision ID of this chip.
The content of this EC side register is the same as that of the CHIPVER register in the host side.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R	02h	**Chip Version (ECHIPVER)**

7.17.4.4 Identify Input Register (IDR)

Address Offset: 04h

Bit	R/W	Default	Description
7	R	-	**Identify Input 7 (ID7)**
6	R	-	**Identify Input 6 (ID6)**
5	R	-	**Identify Input 5 (ID5)**
4	R	-	**Identify Input 4 (ID4)**
3	R	-	**Identify Input 3 (ID3)**
2	R	-	**Identify Input 2 (ID2)**
1	R	-	**Identify Input 1 (ID1)**
0	R	-	**Identify Input 0 (ID0)**

7.17.4.5 Reset Status (RSTS)

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R/W	01b	**VCC Detector Option (VCCDO)** 00b: The VCC power status is treated as power-off. 01b: The VCC power status is treated as power-on. Otherwise: Reserved No matter which option is selected, the VCC power status is always recognized as power off if LPCPD# input is level low. The VCC power status is used as internal “power good” signal to prevent current leakage while VCC is off. The current VCC power status can be read from VCCPO bit in SWCTL1 register in section 6.5.5.1 on page 154. Intentionally toggling this field when VCC is supplied can reset logic VCC domain in EC.
5	R/W	-	**VFSPI Power Good (VFSPIPG)** The written data of this bit is used as an internal "power good" signal to avoid current leakage while VFSPI is off. 0b: The power status of VFSPI is treated as power-on 1b: The power status of VFSPI is treated as power-off
4	-	-	**Reserved**
3	R/W	1b	**Host Global Reset (HGRST)** 0: The reset source of PNPCFG is RSTPNP bit in RSTCH register and WRST#. 1: The reset source of PNPCFG are RSTPNP bit in RSTCH register, internal VCC status controlled by VCCDO bit in RSTS register, LPCPD#, LPCRST# and WRST#.
2	R/W	1b	**Global Reset (GRST)** This bit controls whether to reset EC domain globally during Internal/External Watchdog Reset. 0: Only reset CPU, and each module can be reset by RSTCn register 1: Reset all the EC domain
1-0	R/WC	-	**Last Reset Source (LRS)** These bits indicate the last reset source. To clear them, write a one to bit 0. If this register field is used, it is required to write 11b to this field once and only one time after reset. 00b, 01b: VSTBY Power-Up Reset or Warm Reset 10b: Internal Watchdog Reset 11b: External Watchdog Reset

7.17.4.6 Reset Control 1 (RSTC1)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).
Refer to VCCDO field in RSTS register to reset logic in VCC domain in EC.

Address Offset: 07h

Bit	R/W	Default	Description
7	W	-	**Reset SMFI (RSMFI)**
6	W	-	**Reset INTC (RINTC)**
5	W	-	**Reset EC2I (REC2I)**
4	W	-	**Reset KBC (RKBC)**
3	W	-	**Reset SWUC (RSWUC)**
2	W	-	**Reset PMC (RPMC)**
1	W	-	**Reset GPIO (RGPIO)**
0	W	-	**Reset PWM (RPWM)**

7.17.4.7 Reset Control 2 (RSTC2)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 08h

Bit	R/W	Default	Description
7	W	-	**Reset ADC (RADC)**
6	W	-	**Reset DAC (RDAC)**
5	W	-	**Reset WUC (RWUC)**
4	W	-	**Reset KBS (RKBS)**
3	-	-	**Reserved**
2	W	-	**Reset EGPC (REXGPIO)**
1	W	-	**Reset CIR (RCIR)**
0	-	-	**Reserved**

7.17.4.8 Reset Control 3 (RSTC3)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 09h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	-	**Reset PS/2 Channel 3 (RPS23)**
5	W	-	**Reset PS/2 Channel 2 (RPS22)**
4	W	-	**Reset PS/2 Channel 1 (RPS21)**
3	W	-	**Reset SMBus Channel D (RSMBD)**
2	W	-	**Reset SMBus Channel C (RSMBC)**
1	W	-	**Reset SMBus Channel B (RSMBB)**
0	W	-	**Reset SMBus Channel A (RSMBA)**

7.17.4.9 Reset Control 4 (RSTC4)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 11h

Bit	R/W	Default	Description
7	W	-	**Reset CEC (RCEC)**
6-5	-	-	**Reserved**
4	W	-	**Reset PECI (RPECI)**
3	W	-	**Reset TMR (RTMR)**
2	W	-	**Reset UART2 (RUART2)**
1	W	-	**Reset UART1 (RUART1)**
0	W	-	**Reset SSPI (RSSPI)**

7.17.4.10 Reset Control DMM (RSTDMMC)

Determine whether a double-mapping module belongs to the host or EC side.

Address Offset: 10h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	-	-	**Reserved**
3	R/W	0b	**UART1 SIDE (UART1SD)** 1: UART1 belongs to the EC side. For its clock, refer to section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273. 0: UART1 belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.
2	R/W	0b	**UART2 SIDE (UART2SD)** 1: UART2 belongs to the EC side. For its clock, refers to section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273. 0: UART2 belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.
1	R/W	1b	**SSPI SIDE (SSPISD)** 1: SSPI belongs to the EC side. For its clock, refer to section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273. 0: SSPI belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.
0	R/W	1b	**CIR SIDE (CIRSD)** 1: CIR belongs to the EC side. For its clock, refer to section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 273. 0: CIR belongs to the host side and it will be reset during Host Domain Hardware/Software reset. Its clock is off if VCC is off.

7.17.4.11 Reset Control 6 (RSTC6)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 29h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	W	-	**Reset SMBus Channel F (RSMBF)**
0	W	-	**Reset SMBus Channel E (RSMBE)**

7.17.4.12 Base Address Select (BADRSEL)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Base Address (BADDR1-0)** 00b: The register pair to access PNPCFG is 002Eh and 002Fh. 01b: The register pair to access PNPCFG is 004Eh and 004Fh. 10b: The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR. 11b: Reserved.

7.17.4.13 Wait Next Clock Rising (WNCKR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	W	-	**Wait Next 65K Rising (WN65K)** Writing 00h to this register and the CPU program counter will be paused until the next low to high transition of 65.536 kHz clock. Writing other values is reserved.

7.17.4.14 Special Control 5 (SPCTRL5)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	W	0b	**ECRTCT RAM Only (ECRTCRAM)** If HRTCRAM or ECRTCRAM is one, Index 80h-FFh in RTCT Bank 0/1 is RAM bytes. Otherwise, Bit 7 of index in RTCT Bank 0/1 is not decoded.
3-0	-	-	**Reserved**

7.17.4.15 Special Control 1 (SPCTRL1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/W	0b	**P80L Enable (P80LEN)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VSTBY power. Refer to section 7.19.3.1 P80L on page 460. 1b: Enable P80L function. 0b: Otherwise
6	R/W	0b	**Accept Port 80h Cycle (ACP80)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VSTBY power. Refer to section 7.19.3.1 P80L on page 460. 1b: The host LPC I/O cycle with address 80h will be accepted by EC. If P80LEN is set, enabling this bit to guarantee LPC I/O port 80h data can be latched even though there is a transaction cycle to BRAM. 0b: Otherwise
5-4	-	-	**Reserved**
3	R/W	0b	**Accept Port 81h Cycle (ACP81)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VSTBY power. Refer to section 7.19.3.1 P80L on page 460. 1b: The host LPC I/O cycle with address 81h will be accepted by EC. If P80LEN is set, enabling this bit to guarantee LPC I/O port 81h data can be latched even though there is a transaction cycle to BRAM. 0b: Otherwise
2	-	-	**Reserved**
1-0	R/W	00b	**I2EC Control (I2ECCTRL)** 00b: I2EC is disabled. 10b: I2EC is read-only. 11b: I2EC is read-write. 01b: Reserved Refer to section 7.24.3.5 EC Memory Snoop (ECMS) on page 503.

7.17.4.16 Reset Control Host Side (RSTCH)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	W	-	**Reset PNPCFG (RSTPNP)**
1-0	-	-	**Reserved**

7.17.4.17 Generate IRQ (GENIRQ)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	W	-	**Generate IRQ Number (GENIRQNUM)** Writing to this field will generate SERIRQ with a specified number. This field is valid only when it is between 1-12 or 14-15.

7.17.4.18 Special Control 2 (SPCTRL2)

Address Offset: 12h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Port I2EC Enable (PI2ECEN)** 1b: Decode I2EC cycles via address I2EC_XADDR. 0b: Otherwise Refer to section 7.24.3.5 EC Memory Snoop (ECMS) on page 503.

7.17.4.19 Special Control 3 (SPCTRL3)

Address Offset: 16h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**eSPI Port80 Catch Mode (ESPIP80CM)** 0b: Disable 1b: The eSPI slave is configured to monitor the eSPI bus only and is capable of catching the data of eSPI IO write cycle with address 80h.
4-0	-	-	**Reserved**

7.17.4.20 Special Control 4 (SPCTRL4)

Address Offset: 1Ch

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/WC	-	**Last Reset Source Is Pre-defined Reset (LRSIPDR)** If this bit is used, it is required to write 1 to this bit once and only one time after reset. 0b: The last reset source is not generated from the Pre-defined reset command. 1b: The last reset source is from the Pre-defined reset command. Write 1: Clear this bit Write 0: No action
2	R/WC	-	**Last Reset Source Is Warm Reset (LRSIWR)** To clear this bit, write a one to it. 0b: Last reset is not generated from Warm reset function. 1b: Last reset source is Warm reset.

Bit	R/W	Default	Description
1	R/WC	-	**Last Reset Source Is PWRSW Timeout Reset (LRSIPWRSWTR)** If this bit is used, it is required to write 1 to this bit once and only one time after reset. 0b: Last reset is not generated from PWRSW timeout reset function. 1b: Last reset source is PWRSW timeout reset. Write 1: Clear this bit Write 0: No action
0	R/WC	-	**Last Reset Source Is Power Good Watch Reset (LRSIPGWR)** If this bit is used, it is required to write 1 to this bit once and only one time after reset. 0b: Last reset is not generated from power good watch reset function. 1b: Last reset source is power good watch reset. Write 1: Clear this bit Write 0: No action

7.17.4.21 Port I2EC High-Byte Register (PI2ECH)

LPC I/O port with address equal to PORT_I2EC[15:0] + 1: I2EC_XADDR_H
LPC I/O port with address equal to PORT_I2EC[15:0] + 2: I2EC_XADDR_L
LPC I/O port with address equal to PORT_I2EC[15:0] + 3: I2EC_XDATA
EC only accepts the LPC I/O cycle with PORT_I2EC address if PI2ECEN bit in SPCTRL2 register is set.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	03h	**Port I2EC[15:8] (PORT_I2EC[15:8])** High-byte address of I/O port for I2EC purpose. Bit 7-4 (PORT_I2EC[15:12]) are forced to 0000b and can't be written.

7.17.4.22 Port I2EC Low-Byte Register (PI2ECL)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	80h	**Port I2EC[7:0] (PORT_I2EC[7:0])** Low-byte address of I/O port for I2EC purpose. Bit 1-0 (PORT_I2EC[1:0]) are forced to 00b and can't be written.

7.17.4.23 BRAM Interrupt Address 0 Register (BINTADDR0R)

BINTADDR0R, BINTADDR1R and BINTCTRLR are used for I2BRAM function.

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R/W	00h	**BRAM Interrupt Address 0 (BINTADDR0)** When the host side writes data to BRAM and the address offset equals to the value of BINTADDR0, the interrupt source, INT71, will be issued. In addition, this function will be activated only when BINTA0EN bit is set. Notice that BRAM interrupt address range must be set from 2280h to 22BFh.

7.17.4.24 BRAM Interrupt Address 1 Register (BINTADDR1R)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**BRAM Interrupt Address 1 (BINTADDR1)** When the host side writes data to BRAM and the address offset equals to the value of BINTADDR1, the interrupt source, INT71, will be issued. In addition, this function will be activated only when BINTA1EN bit is set. Notice that BRAM interrupt address range must be set from 2280h to 22BFh.

7.17.4.25 BRAM Interrupt Control Register (BINTCTRLR)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/WC	0b	**BRAM Interrupt Address 1 Match Status (BINTA1MSTS)** This bit will be set when the host side writes data to BRAM address offset, BINTADDR1 and it will be write-one-cleared.
4	R/WC	0b	**BRAM Interrupt Address 0 Match Status (BINTA0MSTS)** This bit will be set when host side writes data to BRAM address offset, BINTADDR0 and it will be write-one-cleared.
3-2	-	-	**Reserved**
1	R/W	0b	**BRAM Interrupt Address 1 Enable (BINTA1EN)** 0b: BRAM interrupt address 1 function is disabled. 1b: BRAM interrupt address 1 function is enabled.
0	R/W	0b	**BRAM Interrupt Address 0 Enable (BINTA0EN)** 0b: BRAM interrupt address 0 function is disabled. 1b: BRAM interrupt address 0 function is enabled.

7.17.4.26 Port 80h/81h Status Register (P80H81HSR)

Address Offset: 30h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/WC	0b	**Port 80h/81h Receive Status (P80H81HRS)** 0b: No cycle is received. 1b: The LPC I/O cycle with address 80h (or 81h) is received. Write 1 to clear this bit.

7.17.4.27 Port 80h Data Register (P80HDR)

Address Offset: 31h

Bit	R/W	Default	Description
7-0	R	-	**Port 80h Data (P80HD)** Read returns the received data of the LPC I/O cycle with address 80h.

7.17.4.28 Port 81h Data Register (P81HDR)

Address Offset: 32h

Bit	R/W	Default	Description
7-0	R	-	**Port 81h Data (P81HD)** Read returns the received data of the LPC I/O cycle with address 81h.

7.18 External GPIO Controller (EGPC)

7.18.1 Overview

This module controls the external GPIO (General Purpose I/O Port) chip. It can maintain bi-directional communication with the 4 external IT8301/IT8302.

7.18.2 Features

- Communicates with 4 IT8301/IT8302 chip
  (IT8301 is a 48-pin GPIO chip)
  (IT8302 is a 24-pin GPIO chip)
- Each IT8301 supports 38 GPIO ports
- Each IT8302 supports 16 GPIO ports
- Supports interrupt to indicate change in external GPIO pin status

7.18.3 Functional Description

This module uses a three-wire bidirectional interface for data transmission. When writing the data to the External GPIO Data Register, this module will start to transmit the data (the contents of the External GPIO Data Register) to the targeted register of the external GPIO chip (the targeted register can be assigned in the External GPIO Address Register). When reading the External GPIO Data Register, the contents of the targeted register of the external GPIO chip can be read.

Because of the serial nature of the interface, the time of accessing the external GPIO chip may be longer than the time that the CPU CPU read/write the External GPIO Controller registers. We have two methods to handle this condition.

(1). A dedicated channel ready signal (internal signal) for the CPU CPU

The channel ready signal (internal signal) is used to inform the CPU CPU whether the data transfer process is ended or not. When the Channel Ready Enable bit in the External GPIO Control Register is set, the channel ready signal will not be asserted until the data transfer process is ended. When the Channel Ready Enable bit is cleared, the channel ready signal is always set high no matter the data transfer process is ended or not.

(2). Enable the cycle done interrupt

If the Channel Ready Enable bit in the External GPIO Control Register is cleared, the firmware must enable the Cycle Done Interrupt Enable bit in the External GPIO Control Register to know that the data transfer process is ended or not. When writing the data to the External GPIO Data Register, this module will start to transmit the data to the targeted register of the external GPIO chip. When the transfer process is ended, the Cycle Done Status bit in the External GPIO Status Register is set and the Cycle Done Interrupt is asserted. When firmware first reads the External GPIO Data Register, this module will start to receive data from the targeted register of the external GPIO chip. When the transfer process is ended, the Cycle Done Status bit in the External GPIO Status Register is set and the Cycle Done Interrupt is asserted. Then the firmware can read again the External GPIO Data Register to get the updated data.

7.18.4 EC Interface Registers

The EGPC registers are listed below. The base address is 2100h.

Table 7-28. EC View Register Map, EGPC

7 — 0	Offset
External GPIO Address Register (EADDR)	00h
External GPIO Data Register (EDAT)	01h
External GPIO Control Register (ECNT)	02h
External GPIO Status Register (ESTS)	03h
External GPIO Auto Read Control Register (EARCR)	04h
External GPIO Read Enable 1 Register (ERE1R)	05h
External GPIO Read Enable 2 Register (ERE2R)	06h
External GPIO Read Enable 3 Register (ERE3R)	07h
External GPIO Read Enable 4 Register (ERE4R)	08h
External GPIO Read Enable 5 Register (ERE5R)	09h
External GPIO Status Vector Register (ESVR)	0Ah
External GPIO Status Change Flag 1 Register (ESCF1R)	10h
External GPIO Status Change Flag 2 Register (ESCF2R)	11h
External GPIO Status Change Flag 3 Register (ESCF3R)	12h
External GPIO Status Change Flag 4 Register (ESCF4R)	13h
External GPIO Status Change Flag 5 Register (ESCF5R)	14h

7.18.4.1 External GPIO Address Register (EADDR)

Address Offset: 00h

Bit	R/W	Default	Description
7-2	R/W	00h	**Address (AD)** The 6-bit address of the targeted register of the external GPIO chip.
1-0	R/W	00h	**Chip Selection (CS)** These bits will be transmitted as external chip selection

7.18.4.2 External GPIO Data Register (EDAT)

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data (DATA)** When writing to this register, the contents of this register are sent to the targeted register of the external GPIO chip. When reading this register, the contents of the targeted register of the external GPIO chip can be read.

7.18.4.3 External GPIO Control Register (ECNT)

Address Offset: 02h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-2	R/W	100b	**Transmitted Data Bits (TMB)** Define the number of the data bits that will be transmitted to (or received from) the data register of the external GPIO chip. 000: 1 bit 001: 2 bits 010: 3 bits 011: 4 bits 100: 5 bits 101: 6 bits 110: 7 bits 111: 8 bits
1	R/W	0b	**Cycle Done Interrupt Enable (CDIE)** Enable or disable the interrupt generation when the Cycle Done status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
0	R/W	1b	**Channel Ready Enable (CREN)** The channel ready signal (internal signal) is used to inform the CPU CPU that the data transfer process is ended or not. When this bit is set, the channel ready signal will not be asserted until the data transfer process is ended. When this bit is cleared, the channel ready signal is always set high no matter the data transfer process is ended or not. 0: Disable 1: Enable

7.18.4.4 External GPIO Status Register (ESTS)

Address Offset: 03h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R	-	**Cycle Done Status (CDS)** This bit is set when the data transfer was done.

7.18.4.5 External GPIO Auto Read Control Register (EARCR)

Address Offset: 04h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Auto Read Enable (ARE)** 1: Enable Auto Read function. 0: Disable Auto Read function.
3	R/W	0b	**Auto Read Interrupt Enable (ARIE)** 1: Enable interrupt to CPU when the status of the external GPIO pin changes. 0: Disable interrupt to CPU when the status of the external GPIO pin changes.
2	R/W	0b	**Scan All Pad Mode (SAPM)** 1: Scan all of external GPIO pins' statuses. 0: Scan the status of the external GPIO pin which is enabled by the corresponding register ERE1R ~ ERE5R.
1-0	R/W	00b	**Auto Scan Period Select (ASPS)** The former time is in normal mode, another one is in sleep Mode. 00: 200 us / 55 ms 01: 400 us / 110 ms 10: 800 us / 220 ms 11: 1600 us / 440 ms

7.18.4.6 External GPIO Read Enable 1 Register (ERE1R)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	0b	**External GPIO 7 Read Enable (EG7RE)** When the auto read mode is enabled, it will check external GPIO 7 pin's status if this bit is 1.
6	R/W	0b	**External GPIO 6 Read Enable (EG6RE)** When the auto read mode is enabled, it will check external GPIO 6 pin's status if this bit is 1.
5	R/W	0b	**External GPIO 5 Read Enable (EG5RE)** When the auto read mode is enabled, it will check external GPIO 5 pin's status if this bit is 1.
4	R/W	0b	**External GPIO 4 Read Enable (EG4RE)** When the auto read mode is enabled, it will check external GPIO 4 pin's status if this bit is 1.
3	R/W	0b	**External GPIO 3 Read Enable (EG3RE)** When the auto read mode is enabled, it will check external GPIO 3 pin's status if this bit is 1.
2	R/W	0b	**External GPIO 2 Read Enable (EG2RE)** When the auto read mode is enabled, it will check external GPIO 2 pin's status if this bit is 1.
1	R/W	0b	**External GPIO 1 Read Enable (EG1RE)** When the auto read mode is enabled, it will check external GPIO 1 pin's status if this bit is 1.

Bit	R/W	Default	Description
0	R/W	0b	**External GPIO 0 Read Enable (EG0RE)** When the auto read mode is enabled, it will check external GPIO 0 pin's status if this bit is 1.

7.18.4.7 External GPIO Read Enable 2 Register (ERE2R)

Address Offset: 06h

Bit	R/W	Default	Description
7	R/W	0b	**External GPIO 15 Read Enable (EG15RE)** When the auto read mode is enabled, it will check external GPIO 15 pin's status if this bit is 1.
6	R/W	0b	**External GPIO 14 Read Enable (EG14RE)** When the auto read mode is enabled, it will check external GPIO 14 pin's status if this bit is 1.
5	R/W	0b	**External GPIO 13 Read Enable (EG13RE)** When the auto read mode is enabled, it will check external GPIO 13 pin's status if this bit is 1.
4	R/W	0b	**External GPIO 12 Read Enable (EG12RE)** When the auto read mode is enabled, it will check external GPIO 12 pin's status if this bit is 1.
3	R/W	0b	**External GPIO 11 Read Enable (EG11RE)** When the auto read mode is enabled, it will check external GPIO 11 pin's status if this bit is 1.
2	R/W	0b	**External GPIO 10 Read Enable (EG10RE)** When the auto read mode is enabled, it will check external GPIO 10 pin's status if this bit is 1.
1	R/W	0b	**External GPIO 9 Read Enable (EG9RE)** When the auto read mode is enabled, it will check external GPIO 9 pin's status if this bit is 1.
0	R/W	0b	**External GPIO 8 Read Enable (EG8RE)** When the auto read mode is enabled, it will check external GPIO 8 pin's status if this bit is 1.

7.18.4.8 External GPIO Read Enable 3 Register (ERE3R)

Address Offset: 07h

Bit	R/W	Default	Description
7	R/W	0b	**External GPIO 23 Read Enable (EG23RE)** When the auto read mode is enabled, it will check external GPIO 23 pin's status if this bit is 1.
6	R/W	0b	**External GPIO 22 Read Enable (EG22RE)** When the auto read mode is enabled, it will check external GPIO 22 pin's status if this bit is 1.
5	R/W	0b	**External GPIO 21 Read Enable (EG21RE)** When the auto read mode is enabled, it will check external GPIO 21 pin's status if this bit is 1.
4	R/W	0b	**External GPIO 20 Read Enable (EG20RE)** When the auto read mode is enabled, it will check external GPIO 20 pin's status if this bit is 1.

Bit	R/W	Default	Description
3	R/W	0b	**External GPIO 19 Read Enable (EG19RE)** When the auto read mode is enabled, it will check external GPIO 19 pin's status if this bit is 1.
2	R/W	0b	**External GPIO 18 Read Enable (EG18RE)** When the auto read mode is enabled, it will check external GPIO 18 pin's status if this bit is 1.
1	R/W	0b	**External GPIO 17 Read Enable (EG17RE)** When the auto read mode is enabled, it will check external GPIO 17 pin's status if this bit is 1.
0	R/W	0b	**External GPIO 16 Read Enable (EG16RE)** When the auto read mode is enabled, it will check external GPIO 16 pin's status if this bit is 1.

7.18.4.9 External GPIO Read Enable 4 Register (ERE4R)

Address Offset: 08h

Bit	R/W	Default	Description
7	R/W	0b	**External GPIO 31 Read Enable (EG31RE)** When the auto read mode is enabled, it will check external GPIO 31 pin's status if this bit is 1.
6	R/W	0b	**External GPIO 30 Read Enable (EG30RE)** When the auto read mode is enabled, it will check external GPIO 30 pin's status if this bit is 1.
5	R/W	0b	**External GPIO 29 Read Enable (EG29RE)** When the auto read mode is enabled, it will check external GPIO 29 pin's status if this bit is 1.
4	R/W	0b	**External GPIO 28 Read Enable (EG28RE)** When the auto read mode is enabled, it will check external GPIO 28 pin's status if this bit is 1.
3	R/W	0b	**External GPIO 27 Read Enable (EG27RE)** When the auto read mode is enabled, it will check external GPIO 27 pin's status if this bit is 1.
2	R/W	0b	**External GPIO 26 Read Enable (EG26RE)** When the auto read mode is enabled, it will check external GPIO 26 pin's status if this bit is 1.
1	R/W	0b	**External GPIO 25 Read Enable (EG25RE)** When the auto read mode is enabled, it will check external GPIO 25 pin's status if this bit is 1.
0	R/W	0b	**External GPIO 24 Read Enable (EG24RE)** When the auto read mode is enabled, it will check external GPIO 24 pin's status if this bit is 1.

7.18.4.10 External GPIO Read Enable 5 Register (ERE5R)

Address Offset: 09h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**External GPIO 37 Read Enable (EG37RE)** When the auto read mode is enabled, it will check external GPIO 37 pin's status if this bit is 1.

Bit	R/W	Default	Description
4	R/W	0b	**External GPIO 36 Read Enable (EG36RE)** When the auto read mode is enabled, it will check external GPIO 36 pin's status if this bit is 1.
3	R/W	0b	**External GPIO 35 Read Enable (EG35RE)** When the auto read mode is enabled, it will check external GPIO 35 pin's status if this bit is 1.
2	R/W	0b	**External GPIO 34 Read Enable (EG34RE)** When the auto read mode is enabled, it will check external GPIO 34 pin's status if this bit is 1.
1	R/W	0b	**External GPIO 33 Read Enable (EG33RE)** When the auto read mode is enabled, it will check external GPIO 33 pin's status if this bit is 1.
0	R/W	0b	**External GPIO 32 Read Enable (EG32RE)** When the auto read mode is enabled, it will check external GPIO 32 pin's status if this bit is 1.

7.18.4.11 External GPIO Status Vector Register (ESVR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	FFh	**External GPIO Status Vector (ESV)** It contains the interrupt number, which is the highest priority, enabled and pending interrupt. The valid values range from 00h to 25h. Note that 00h has the lowest priority. If no enabled interrupt is pending, it returns FFh. Example: ESV data value is 1Dh means the status of the external GPIO pin 29 has changed.

7.18.4.12 External GPIO Status Change Flag 1 Register (ESCF1R)

Address Offset: 10h

Bit	R/W	Default	Description
7	R/WC	0b	**External GPIO 7 Status Change Flag (E7SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 7 changes. Write zero is ignored.
6	R/WC	0b	**External GPIO 6 Status Change Flag (E6SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 6 changes. Write zero is ignored.
5	R/WC	0b	**External GPIO 5 Status Change Flag (E5SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 5 changes. Write zero is ignored.
4	R/WC	0b	**External GPIO 4 Status Change Flag (E4SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 4 changes. Write zero is ignored.
3	R/WC	0b	**External GPIO 3 Status Change Flag (E3SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 3 changes. Write zero is ignored.
2	R/WC	0b	**External GPIO 2 Status Change Flag (E2SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 2 changes. Write zero is ignored.

Bit	R/W	Default	Description
1	R/WC	0b	**External GPIO 1 Status Change Flag (E1SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 1 changes. Write zero is ignored.
0	R/WC	0b	**External GPIO 0 Status Change Flag (E0SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 0 changes. Write zero is ignored.

7.18.4.13 External GPIO Status Change Flag 2 Register (ESCF2R)

Address Offset: 11h

Bit	R/W	Default	Description
7	R/WC	0b	**External GPIO 15 Status Change Flag (E15SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 15 changes. Write zero is ignored.
6	R/WC	0b	**External GPIO 14 Status Change Flag (E14SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 14 changes. Write zero is ignored.
5	R/WC	0b	**External GPIO 13 Status Change Flag (E13SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 13 changes. Write zero is ignored.
4	R/WC	0b	**External GPIO 12 Status Change Flag (E12SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 12 changes. Write zero is ignored.
3	R/WC	0b	**External GPIO 11 Status Change Flag (E11SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 11 changes. Write zero is ignored.
2	R/WC	0b	**External GPIO 10 Status Change Flag (E10SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 10 changes. Write zero is ignored.
1	R/WC	0b	**External GPIO 9 Status Change Flag (E9SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 9 changes. Write zero is ignored.
0	R/WC	0b	**External GPIO 8 Status Change Flag (E8SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 8 changes. Write zero is ignored.

7.18.4.14 External GPIO Status Change Flag 3 Register (ESCF3R)

Address Offset: 12h

Bit	R/W	Default	Description
7	R/WC	0b	**External GPIO 23 Status Change Flag (E23SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 23 changes. Write zero is ignored.
6	R/WC	0b	**External GPIO 22 Status Change Flag (E22SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 22 changes. Write zero is ignored.
5	R/WC	0b	**External GPIO 21 Status Change Flag (E21SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 21 changes. Write zero is ignored.

Bit	R/W	Default	Description
4	R/WC	0b	**External GPIO 20 Status Change Flag (E20SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 20 changes. Write zero is ignored.
3	R/WC	0b	**External GPIO 19 Status Change Flag (E19SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 19 changes. Write zero is ignored.
2	R/WC	0b	**External GPIO 18 Status Change Flag (E18SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 18 changes. Write zero is ignored.
1	R/WC	0b	**External GPIO 17 Status Change Flag (E17SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 17 changes. Write zero is ignored.
0	R/WC	0b	**External GPIO 16 Status Change Flag (E16SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 16 changes. Write zero is ignored.

7.18.4.15 External GPIO Status Change Flag 4 Register (ESCF4R)

Address Offset: 13h

Bit	R/W	Default	Description
7	R/WC	0b	**External GPIO 31 Status Change Flag (E31SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 31 changes. Write zero is ignored.
6	R/WC	0b	**External GPIO 30 Status Change Flag (E30SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 30 changes. Write zero is ignored.
5	R/WC	0b	**External GPIO 29 Status Change Flag (E29SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 29 changes. Write zero is ignored.
4	R/WC	0b	**External GPIO 28 Status Change Flag (E28SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 28 changes. Write zero is ignored.
3	R/WC	0b	**External GPIO 27 Status Change Flag (E27SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 3 changes. Write zero is ignored.
2	R/WC	0b	**External GPIO 26 Status Change Flag (E26SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 26 changes. Write zero is ignored.
1	R/WC	0b	**External GPIO 25 Status Change Flag (E25SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 25 changes. Write zero is ignored.
0	R/WC	0b	**External GPIO 24 Status Change Flag (E24SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 24 changes. Write zero is ignored.

7.18.4.16 External GPIO Status Change Flag 5 Register (ESCF5R)

Address Offset: 14h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/WC	0b	**External GPIO 37 Status Change Flag (E37SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 37 changes. Write zero is ignored.
4	R/WC	0b	**External GPIO 36 Status Change Flag (E36SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 36 changes. Write zero is ignored.
3	R/WC	0b	**External GPIO 35 Status Change Flag (E35SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 35 changes. Write zero is ignored.
2	R/WC	0b	**External GPIO 34 Status Change Flag (E34SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 34 changes. Write zero is ignored.
1	R/WC	0b	**External GPIO 33 Status Change Flag (E33SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 33 changes. Write zero is ignored.
0	R/WC	0b	**External GPIO 32 Status Change Flag (E32SC)** Write one to clear the Interrupt status, which is caused when the status of the external GPIO pin 32 changes. Write zero is ignored.

7.19 BRAM .

7.19.1 Overview

This module provides 192 bytes of memory area.

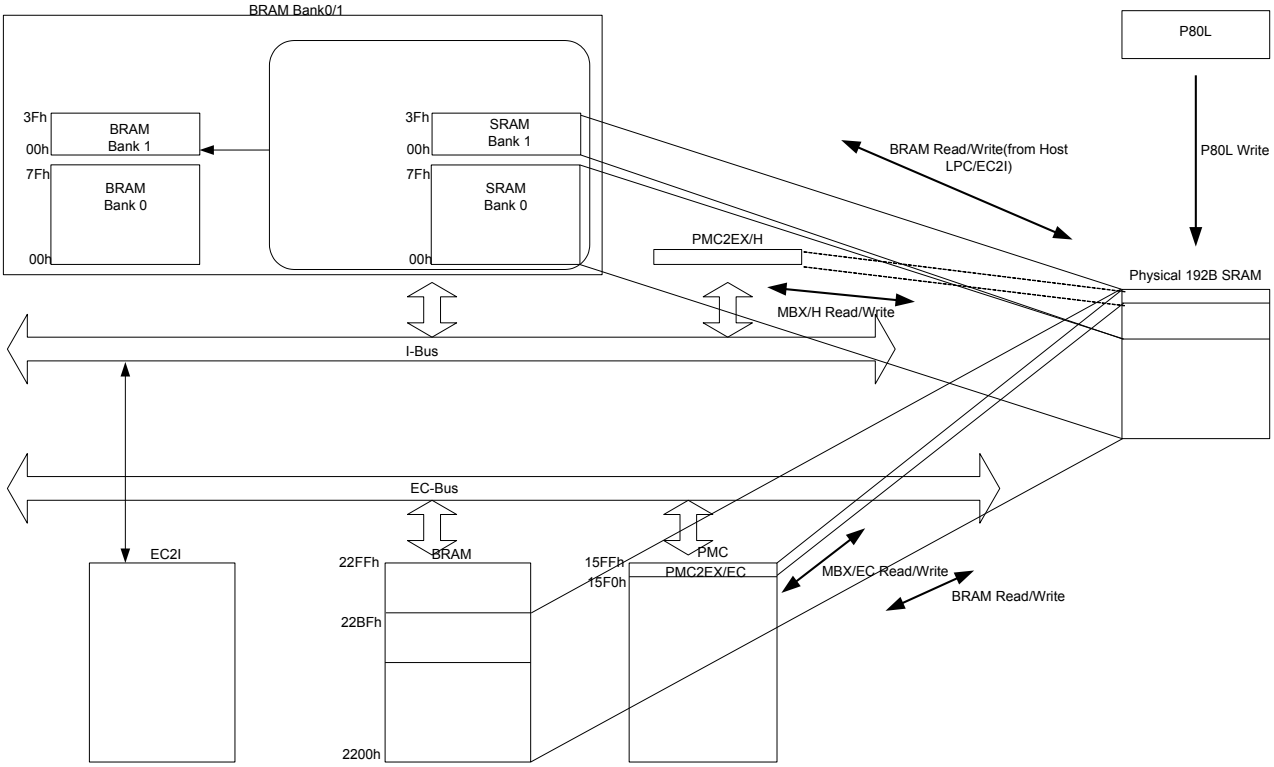
7.19.2 Features

- 192 bytes of SRAM mapped into the host and EC side

7.19.3 Functional Description

This module provides 192 bytes of SRAM for data-saving function shared with the host side.

Figure 7-33. BRAM Mapping Diagram



7.19.3.1 P80L

If this function is enabled by P80LEN bit in SPCTRL1 register, LPC I/O port 80h written data will be latched into SRAM of BRAM bank 1.

The data may fail to latch data if there is a transaction cycle to BRAM at the same time unless ACP80 bit in SPCTRL1 register is set, which guarantees written data is latched into SRAM by issuing Long Wait Sync on host LPC bus.

The destination address range in BRAM Bank 1 is determined by P80LB, P80LE register in the host side, which constructs a queue.
P80LB: It indicates the start index of the queue. Readable/Writable.
P80LE: It indicates the end index of the queue. Readable/Writable.
P80LC: It indicates the current index of the queue. Read-only.

These three registers are supplied by VSTBY power and not affected by VCC status.

Whenever written data is latched, P80LC increases one. If it reaches P80LE (queue end), it will wrap back to P80LB (queue begin).

7.19.4 Host Interface Registers

The registers of BRAM can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.

The BRAM resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below. In addition to the I/O Port Base Addresses of channel, there are three I/O Port Base Addresses of channel for accessing BRAM of Bank1.

Table 7-29. Host View Register Map, BRAM

7 … 0	Offset
BRAM Index Register of Bank 0 (RIRB0)	Legacy 70h
BRAM Data Register of Bank 0 (RDRB0)	Legacy 71h
BRAM Index Register of Bank 1 (RIRB1)	Legacy 272h
BRAM Data Register of Bank 1 (RDRB1)	Legacy 273h

Legacy 70h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 71h represents (I/O Port Base Address 0) + (Offset 1h)
Legacy 272h represents (I/O Port Base Address 1) + (Offset 0h)
Legacy 273h represents (I/O Port Base Address 1) + (Offset 1h)
See also Table 6-7 on page 72.

Table 7-30. Host View Register Map via Index-Data I/O Pair, BRAM Bank 0

7 … 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT127)	7Fh

Table 7-31. Host View Register Map via Index-Data I/O Pair, BRAM Bank 1

7 … 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT63)	3Fh

7.19.5 EC Interface Registers

The registers of the SRAM are listed below. The base address is 2200h.

Table 7-32. EC View Register Map, BRAM

7 … 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT191)	BFh

7.19.5.1 SRAM Byte n Registers (SBTn, n= 0-191)

Address Offset: 00h – BFh for byte 0 – byte 191

Bit	R/W	Default	Description
7-0	R/W	-	**SRAM Data (SD)** When data is written to this register, it will be saved in the corresponding memory space. When this register is read, the contents of the corresponding memory space can be read.

7.20 Consumer IR (CIR)

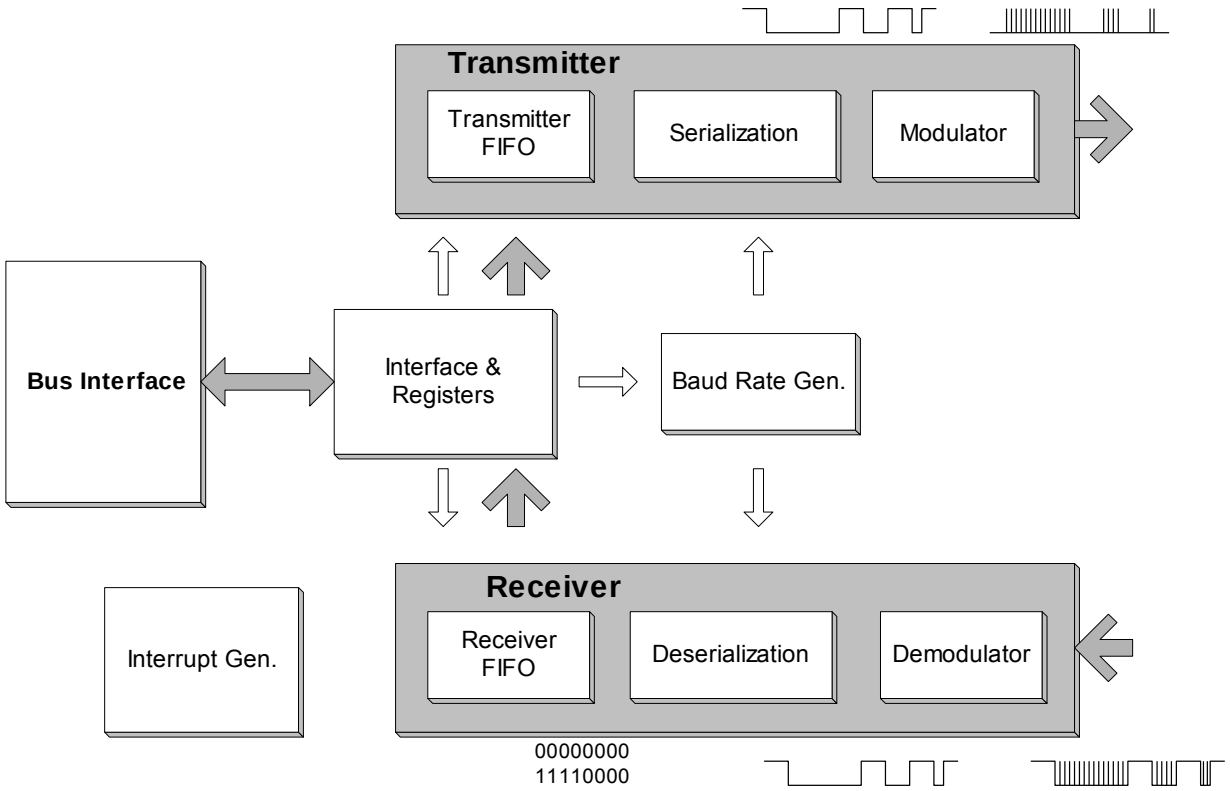
7.20.1 Overview

The CIR module is used in the Consumer Remote Control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisor values and sensitivity ranges, CIR registers are able to support the major protocols such as RC-5, NEC, and RECS-80. New protocols can be supported by programming the software driver.

7.20.2 Features

- Supports 1 CIR channels
- Supports 28 kHz ~ 57 kHz (low frequency) or 400 kHz ~ 500 kHz (high frequency) carrier transmission
- The baud rate up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral functions
- Supports two dedicated 32-byte FIFO, one for data transmission and the other for data reception

Figure 7-34. CIR Simplified Diagram



7.20.3 Functional Description

The CIR channel consists of two main elements, Transmitter and Receiver. The Transmitter transmits data to the FIFO, processes the FIFO data by serialization, modulation and sends out the data through the LED device. The Receiver is responsible for receiving the FIFO data, processing data by demodulation and deserialization, and storing data into the Receiver FIFO.

7.20.3.1 Transmit Operation

The Transmit data formats written to the Transmitter FIFO differ from one another with respect to different communication protocols. Only physical layer functions are provided in this module. The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with the carrier frequency and sent to the pad output. The communication commands are decoded by software.

Before the data transmission can be started, code byte write operations has to be performed to the Transmitter FIFO C0DR. The bit TXRLE in the C0TCR should be set to “1” before the run-length decode data can be written into the Transmitter FIFO. The bit width of the serialized bit string is determined by programming the baud rate divisor registers, C0BDLR and C0BDHR. When bits HCFS and CFQ[4:0] in the C0CFR are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bits TXMPM[1:0] and TXMPW[2:0] in the C0TCR specify the pulse numbers in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic 0 can activate the Transmitter LED in the format of a series of modulating pulses.

7.20.3.2 Receive Operation

The Receiver function is enabled if bit RXEN in the C0RCR is set to “1”. Either demodulated or modulated RX# signal is loaded into the Receiver FIFO, and bit RXEND in the C0RCR determines how the demodulation logic should be used. When bits HCFS and CFQ[4:0] in the C0CFR are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bit RXACT in the C0RCR is set to “1” if the serial data or the selected carrier is incoming, and the sampled data will then be kept in the Receiver FIFO. Write “1” to clear bit RXACT and then stop operation of Receiver FIFO; write “0” to bit RXEN to disable all the Receiver functions. It is strongly suggested that software clear RXACT every time when you will change the expected carrier frequency.

7.20.3.3 Wakeup (Power On) Controller Programming Sequence

Software power-off is performed by setting the resetting bits of RCRST and WCRST to “1”, and the CIRPOIS bit to “0” at the initial state in the C0WPS register. When the system is on, users can reset the read/write counter to 0 at any time. However, if users need to save codes into 20 bytes in the power-switch-code area, the best way is to reset the write counter first since users may not know the value in the counter. Therefore, it is possible that users will make a mistake when saving the codes. Users can also reset the read counter before reading the code in the power-switch-code area. Before users perform the power-off function, it is necessary to save the correct length into the C0WCL register and the coded into the power-switch-code area or the power-on function will not function normally. The CIRPOIS bit is set to one when the data received by CIR for first time matches the code data on the power-switch-code area. The CIRPOIS bit is toggled when the data received again by CIR matches the code data on the power-switch-code area.

Note: If the system designer needs to use the remote power-on function, the designer should program the related receive registers to some proper values via software before shutdown.

7.20.4 Host Interface Registers

The registers of CIR can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The CIR resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-33. Host View Register Map, CIR

7 0		Offset
CIR Data Register (C0DR)	Page 0	00h
CIR Master Control Register (C0MSTCR)	Page 0	01h
CIR Interrupt Enable Register (C0IER)	Page 0	02h
CIR Interrupt Identification Register (C0IIR)	Page 0	03h
CIR Carrier Frequency Register (C0CFR)	Page 1	04h
CIR Receiver Control Register (C0RCR)	Page 0	05h
CIR Transmitter Control Register (C0TCR)	Page 0	07h
CIR Slow Clock Control Register (C0SCK)	Page 1	03h
CIR Wake-Code Set Select Register (C0WCSSR)	Page 1	00h
CIR Baud Rate Divisor Low Byte Register (C0BDLR)	Page 1	01h
CIR Baud Rate Divisor High Byte Register (C0BDHR)	Page 1	02h
CIR Transmitter FIFO Status Register (C0TFSR)	Page 0	06h
CIR Receiver FIFO Status Register (C0RFSR)	Page 0	04h
CIR Wakeup Code Length Register (C0WCL)	Page 1	05h
CIR Wakeup Code Read/Write Register (C0WCR)	Page 1	06h
CIR Wakeup Power Control/Status Register (C0WPS)	Page 1	07h
CIR Scratch Register (CSCRR)	Page 2	00h
CIR General Purpose Interrupt (CGPINTR)	Page 2	01h

All registers are double mapped into the host and EC side, however, the CIR function should be controlled by a side only.

The definitions of all registers are the same as their identical register names in the EC side except HRAE (High Range Address Enable) bit. HRAE bit is a write-only bit, which is located in bit 7 in the registers with offset 07h (C0TCR or C0WPS). HRAE bit is used to select different registers if they have the same offset number.

7.20.5 EC Interface Registers

The EC interface registers are listed below. The base address for CIR is 2300h.

Table 7-34. EC View Register Map, CIR

7 0	Offset
CIR Data Register (C0DR)	00h
CIR Master Control Register (C0MSTCR)	01h
CIR Interrupt Enable Register (C0IER)	02h
CIR Interrupt Identification Register (C0IIR)	03h
CIR Carrier Frequency Register (C0CFR)	04h
CIR Receiver Control Register (C0RCR)	05h
CIR Transmitter Control Register (C0TCR)	06h
CIR Slow Clock Control Register (C0SCK)	07h
CIR Baud Rate Divisor Low Byte Register (C0BDLR)	08h
CIR Baud Rate Divisor High Byte Register (C0BDHR)	09h
CIR Transmitter FIFO Status Register (C0TFSR)	0Ah
CIR Receiver FIFO Status Register (C0RFSR)	0Bh
CIR Wake-Code Set Select Register (C0WCSSR)	0Ch
CIR Wakeup Code Length Register (C0WCL)	0Dh
CIR Wakeup Code Read/Write Register (C0WCR)	0Eh
CIR Wakeup Power Control/Status Register (C0WPS)	0Fh
CIR Scratch Register (CSCRR)	10h

7.20.5.1 CIR Data Register (C0DR)

The C0DR, an 8-bit register, is the data port for CIR. Data is transmitted and received through this register.
Note: Reading an empty FIFO will return a default value, ″FF″.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**CIR FIFO Data (CFD[7:0])** Writing data to this register causes data to be written to the Transmitter FIFO. Reading data from this register causes data to be received from the Receiver FIFO.

7.20.5.2 CIR Master Control Register (C0MSTCR)

The C0MSTCR, an 8-bit register, is used to control CIR functions.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	0b	**CTX Channel Select (CTXSEL)** 0: CTX0 selected 1: CTX1 selected This bit is valid only if both CTX0/CTX1 are set as func 1 mode in GPIO module.
6	R/W	0b	**CRX Channel Select (CRXSEL)** 0: CRX0 selected 1: CRX1 selected This bit is valid only if both CRX0/CRX1 are set as func 1 mode in GPIO module.
5	R/W	0b	**Internal Loopback Select (ILSEL)** This bit is used to determine the internal loopback source. When this bit is set to “0”, the Serial data is the internal loopback source. When this bit is set to “1”, the Modulated data is the internal loopback source.
4	R/W	0b	**Internal Loopback Enable (ILE)** This bit is used to execute internal loopback for test and has to be “0” in normal operation. When this bit is set to “0”, the internal Loopback mode is disabled. When this bit is set to “1”, the internal Loopback mode is enabled.
3-2	R/W	00b	**FIFO Threshold Level (FIFOTL)** These two bits are used to set the FIFO Threshold Level. The FIFO length is 32 bytes for TX/RX function. **00** 1 **01** 7 **10** 17 **11** 25
1	R/W	0b	**FIFO Clear (FIFOCLR)** Writing a “1” to this bit clears both TX and RX FIFO. This bit is then cleared to “0” automatically.
0	R/W	0b	**RESET (RESET)** The function of this bit is software reset. Writing a “1” to this bit resets the registers of C0DR, C0MSTCR, C0IER, C0IIR, C0CFR, C0TCR, C0TFSR and C0RFSR. This bit is then cleared to “0” automatically.

7.20.5.3 CIR Interrupt Enable Register (C0IER)

The C0IER, an 8-bit register, is used to enable the CIR interrupt request.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Interrupt Enable Function Control (IEC)** This bit is used to control the interrupt enabled function. Set this bit to “1” to enable the interrupt request for CIR. Set this bit to “0” to disable the interrupt request for CIR.
6	R/W	0b	**Wakeup-Code Interrupt Type (WCIT)** Set this bit to “1” to deliver the level interrupt request to EC(INT15) of Wakeup-code. The level interrupt request may be cleared by clearing their CIRPOII respectively. Set this bit to “0” to deliver the edge interrupt request to EC(INT15) of Wakeup-code.
5 – 3	-	-	**Reserved**
2	R/W	0b	**Receiver FIFO Overrun Interrupt Enable (RFOIE)** This bit is used to control Receiver FIFO Overrun Interrupt request. Set this bit to “1” to enable Receiver FIFO Overrun Interrupt request. Set this bit to “0” to disable Receiver FIFO Overrun Interrupt request.
1	R/W	0b	**Receiver Data Available Interrupt Enable (RDAIE)** This bit is used to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in FIFO exceeds FIFO Threshold Level. Under carrier period learning mode, the Receiver also geneates this interrupt after receiving three carreirs. Set this bit to “1” to enable Receiver Data Available Interrupt request. Set this bit to “0” to disable Receiver Data Available Interrupt request.
0	R/W	0b	**Transmitter Low Data Level Interrupt Enable (TLDLIE)** This bit is used to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in FIFO is less than the FIFO threshold Level. Set this bit to “1” to enable Transmitter Low Data Level Interrupt request. Set this bit to “0” to disable Transmitter Low Data Level Interrupt request.

7.20.5.4 CIR Interrupt Identification Register (C0IIR)

The C0IIR, an 8-bit register, is used to identify the pending interrupt.

Address Offset: 03h

Bit	R/W	Default	Description
7	R	1b	**No Interrupt Pending (NIP)** This bit will be set to "1" if no interrupt is pending.
6 - 4	-	-	**Reserved**
3	R	0b	**Receiver Carreir Period Learning Error Interrupt (RXCPLEI)** This bit is available only when RXCPLE is 1, and will be set to "1" if the period of the received carrier is greater than 488us.
2	R	0b	**Receiver FIFO Overrun Interrupt (RFOI)** This bit will be set to "1" if receiver FIFO overruns.
1	R	0b	**Receiver Data Available Interrupt (RDAI)** This bit will be set to "1" when the data available in the receiver FIFO exceeds the FIFO Threshold Level.
0	R	0b	**Transmitter Low Data Level Interrupt (TLDLI)** This bit will be set to "1" when the data available in the transmitter FIFO is less than the FIFO threshold Level.

7.20.5.5 CIR Carrier Frequency Register (C0CFR)

The CxCFR, an 8-bit register, is used to determine the carrier frequency.

Address Offset: 04h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	0b	**High-Speed Carrier Frequency Select (HCFS)** This bit is used to select whether the Carrier Frequency is at a high speed or low speed. 0: 30-58 kHz (Default) 1: 400-500 kHz
4-0	R/W	01011b	**Carrier Frequency (CFQ[4:0])** These five bits are used to determine the modulation carrier frequency. See Table 7-35.

Table 7-35. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00001	28 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38 kHz (default)**	**480 kHz (default)**
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

7.20.5.6 CIR Receiver Control Register (C0RCR)

The C0RCR, an 8-bit register, is used to control the CIR Receiver.

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	0b	**Receiver Enable (RXEN)** This bit is used to enable the Receiver function. Set this bit to “1” to enable the Receiver function. Set this bit to “0” to disable the Receiver function. When the Receiver function is enabled, RXACT will be active if the selected carrier frequency is received.
6	R/W	0b	**Receiver Carrier Period Learning Enable (RXCPLE)** 0b: Disable 1b: Enable Set this bit to “1” to enable the carrier learning mode. The Receiver then starts to measure the period of the received carrier, and takes down the result into RX FIFO. The carrier’s period can be calculated by 217ns * CFD[7:0].
5	R/W	0b	**Receiver Data Without Sync. (RDWOS)** This bit is used to control the sync. logic for Receiving data. Set this bit to “1” to obtain the receiving data without sync. logic. Set this bit to “0” to obtain the receiving data in sync. logic.
4	R/W	0b	**Receiver Demodulation Enable (RXEND)** This bit is used to control the Receiver Demodulation logic. Set this bit to “1” to enable the Receiver Demodulation logic. Set this bit to “0” to disable the Receiver Demodulation logic. Set this bit to “1” to the Receiver device to demodulate the correct carrier.
3	R/WC	0b	**Receiver Active (RXACT)** This bit is used to control the Receiver operation. This bit is set to “0” when the Receiver is inactive. This bit is set to “1” when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with the correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Writing a “1” to this bit to clear the Receiver Active condition and make the Receiver enter an inactive mode.
2-0	R/W	001b	**Receiver Demodulation Carrier Range (RXDCR[2:0])** These three bits are used to set the tolerance of the Receiver Demodulation carrier frequency. See Table 7-36 and Table 7-37.

Table 7-36. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		
CFQ	min.	max.	min.	max.	Min.	max.	min.	Max.	min.	max.	min.	max.	(Hz)
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28K
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29K
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30K
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31K
00101	30	34	28	36	26	38	24	40	22	42	20	44	32K
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33K
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34K
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35K
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36K
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37K
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	**28.5**	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38K**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39K
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40K
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41K
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42K
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43K
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44K
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45K
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46K
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47K
10101	45	51	42	54	39	57	36	60	33	63	30	66	48K
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49K
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50K
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51K
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52K
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53K
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54K
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55K
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56K
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57K

Table 7-37. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**(kHz)**
00011	375	425	350	450	325	475	300	500	275	525	250	550	400K
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450K
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480K**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500K

7.20.5.7 CIR Transmitter Control Register (C0TCR)

The C0TCR, an 8-bit register, is used to control the Transmitter.

Address Offset: 06h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Transmitter Run Length Enable (TXRLE)** This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte according to the value stored in bit 7 and the value stored in bits 6-0 minus 1. If this bit is set to "1", the Transmitter Run Length mode is enabled. If this bit is set to "0", the Transmitter Run Length mode is disabled.
5	R/W	0b	**Transmitter Deferral (TXENDF)** This bit is used to avoid the Transmitter underrun condition. When this bit is set to "1", the Transmitter FIFO data will be kept until the transmitter time-out condition occurs or when FIFO is full.
4 - 3	R/W	00b	**Transmitter Modulation Pulse Mode (TXMPM[1:0])** These two bits are used to define the Transmitter modulation pulse mode.

TXMPM[1:0]	Modulation Pulse Mode
00	C_pls mode (Default) Pulses are generated continuously for the entire logic 0 bit time.
01	8_pls mode 8 pulses are generated for each logic 0 bit.
10	6_pls mode 6 pulses are generated for each logic 0 bit.
11	Reserved

Bit	R/W	Default	Description
2-0	R/W	100b	**Transmitter Modulation Pulse Width (TXMPW[2:0])** These three bits are used to set Transmitter Modulation Pulse Width. The duty cycle of the carrier will be determined according to the settings of Carrier Frequency and the selection of Transmitter Modulation Pulse Width.

TXMPW[2:0]	HCFS= 0	HCFS= 1	
000	Reserved	Reserved	
001	Reserved	Reserved	
010	6 μs	0.7 μs	
011	7 μs	0.8 μs	
100	**8.7 μs**	**0.9 μs (Default)**	
101	10.6 μs	1.0 μs	
110	13.3 μs	1.16 μs	
111	Reserved	Reserved	

7.20.5.8 CIR Slow Clock Control Register (C0SCK)

The C0SCK, an 8-bit register, is used to select the slow clock source of 32.768k or DLL output for operating with low power and can wake up EC from the Sleep mode.

In the Sleep mode, CIR only can receive serial data up to 2 kHz when
1. C0BDLR = 01h (max baud rate = 32.768k/16)
2. C0BDHR = 00h
3. SCKS = 1b
4. Demodulation has to be disabled.

Note: prior to set up Wakeup code and receive enable before enter Sleep mode (set SCKS bit in C0SCK register). If firmware needs to compare received data stored in the C0DR register with Wakeup code(written into C0WCR previously), SCKS has to be set to zero beforehand after Wakeup code has received completely.

Address Offset: 07h

Bit	R/W	Default	Description
7	R	1b	**DLL Lock (DLLOCK)** This bit is available when DLLE = 1. 1: DLL in the locked state 0: DLL in the unlocked state
6-4	R/W	0b	**Baud Rate Count Mode (BRCM)** These three bits are used to select the baud rate counter number. They only need to be set when demodulation is disabled and SCKS = 1, DLL1P8E =0. Bits 6-4 baud counter 000 16 (488us) 001 14 (427us) 010 15 (457us) 011 18 (549us)
3	R/W	0b	**DLL Test Enable (DLLTE)** 1: Set DLL to the test mode. 0: DLL in the normal mode
2	R/W	0b	**DLL Enable (DLLE)** 1: DLL Enabled 0: DLL Disabled The slow clock selects 32.768 kHz when this bit is set to 0 and SCKS =1. The slow clock selects DLL when this bit is set to 1 and SCKS =1.
1	R/WC	0b	**TXD Clock Gating (TXDCKG)** 1: CIR transmitter clock source gating 0: CIR transmitter clock source not gating
0	R/W	0b	**Slow Clock Select (SCKS)** 1: Select the slow clock source (32.768k or DLL) for cir receiver to receive serial data which is input to CRX0/CRX1 when RXEND = 0, RDWOS =1, and RXEN = 1. 0: unselect slow clock as the receiver clock source.

7.20.5.9 CIR Baud Rate Divisor Low Byte Register (C0BDLR)

The C0BDLR, an 8-bit register, is used to program the CIR Baud Rate clock.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor Low Byte (BRDL[7:0])** These bits are the low byte of the register and used to divide the Baud Rate clock.

7.20.5.10 CIR Baud Rate Divisor High Byte Register (C0BDHR)

The C0BDHR, an 8-bit register, is used to program the CIR Baud Rate clock.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor High Byte (BRDH[7:0])** These bits are the high byte of the register and used to divide the Baud Rate clock.

Baud rate divisor = 115200/baud rate when SCKS =0.
Ex1: 2400bps ➔ 115200 /2400 = 48 ➔ 48(d) = 0030 (h)
C0BDHR = 00(h), C0BDLR = 30(h)
Ex2: bit width = 0.565 ms ➔ 1770 bps ➔ 115200/1770 = 65 (d) = 0041 (h)
C0BDHR = 00(h), C0BDLR = 0041(h)
The baud rate will be set to 20K bps when C0BDHR = 00h and C0BDLR = 00h. This is a special case.

Baud rate divisor = 116500/baud rate when SCKS =1, and DLLE is enabled.
Ex1: 2540bps ➔ 116500 / 2540 = 46 ➔ 46(d) = 002E (h)
C0BDHR = 00(h), C0BDLR = 2E(h)
Ex2: bit width = 0.565 ms ➔ 1770 bps ➔ 116500/1770 = 66 (d) = 0042 (h)
C0BDHR = 00(h), C0BDLR = 0042(h)

7.20.5.11 CIR Transmitter FIFO Status Register (C0TFSR)

The C0TFSR, an 8-bit register, provides the status information of Transmitter FIFO.

Address Offset: 0Ah

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Transmitter FIFO Clear (TXFIFOCLR)** Writing 1 to this bit to clear TX FIFO. This bit is then cleared to 0 automatically.
5 - 0	R	00h	**Transmitter FIFO Byte Count (TXFBC[5:0])** Return the number of bytes left in Transmitter FIFO.

7.20.5.12 CIR Receiver FIFO Status Register (C0RFSR)

The C0RFSR, an 8-bit register, provides the status information of Receiver FIFO.

Address Offset: 0Bh

Bit	R/W	Default	Description
7	R	0b	**Receiver FIFO Time-out Monitor (RXFTO)** This bit will be set to "1" when the Receiver FIFO time-out condition occurs. The conditions required for the occurrence of Receiver FIFO time-out include the followings: When at least one byte data are queued in Received FIFO for more than 64 ms, and the receiver has been inactive (RXACT=0) for over 64ms. If RXFTO = 1 and both IEC and RDAIE are set one, RDAI(receive data available interrupt) will be asserted at least 16msec to notify the firmware that FIFO still retains data and the firmware needs to read it.
6	R/W	0b	**Receiver FIFO Clear (RXFIFOCLR)** Writing 1 to this bit to clear RX FIFO. This bit is then cleared to 0 automatically.
5-0	R	00h	**Receiver FIFO Byte Count (RXFBC[5:0])** Return the number of bytes left in Receiver FIFO.

7.20.5.13 CIR Wake-Code Set Select Register (C0WCSSR)

The C0WCSSR, an 8-bit register for index, is used to select one programming set from 5 sets of wake-up code which can be accessed in C0WCR. Its length can be accessed in C0WCL and its wakeup status can be accessed in C0WPS.

Address Offset : 0Ch

Bit	R/W	Default	Description
7-5	R/W	000b	**Wake-Up Code Select Index(WUCSI)** 000: Select the 1st wakeup-code set and length to be programmed from C0WCR, C0WCL, and C0WPS. Hardware use this set to do wakeup-code comparison feature (original one set wakeup-code feature) 001: Select the 2nd wakeup-code set and length to be programmed from C0WCR, C0WCL, and C0WPS. 010: Select the 3rd wakeup-code set and length to be programmed from C0WCR, C0WCL, and C0WPS. 011: Select the 4th wakeup-code set and length to be programmed from C0WCR, C0WCL, and C0WPS. 100: Select the 5th wakeup-code set and length to be programmed from C0WCR, C0WCL, and C0WPS. Others: CIR in test mode of manufacture
4-0	R/W	00h	**Reserved**

7.20.5.14 CIR Wakeup Code Length Register (C0WCL)

The C0WCL, an 8-bit register, keeps the value of the valid code length minus 1 in the power-switch-code area. The wakeup controller in CIR module compares the received code with the code saved in the power-switch-code area of wakeup controller C0WCL - 1 bytes.

Address Offset : 0Dh

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5-0	R/W	111111b	**CIR Wakeup Code Length (WCL[5:0])** The value in this register is the valid code length minus 1. For instance, when C0WCL is equal to 0, the valid code length is 1.

7.20.5.15 CIR Wakeup Code Read/Write Register (C0WCR)

The C0WCR, an 8-bit register, is the read/write port for accessing 20 wakeup code bytes. These bytes are accessed sequentially according to the read counter or write counter.

Address Offset : 0Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**CIR Wakeup Code Read/Write Register (WCR[7:0])** A port is for accessing 20 wakeup code bytes.

7.20.5.16 CIR Wakeup Power Control/Status Register (C0WPS)

The C0WPS, an 8-bit register, is used to record the power-on source, and two control bits are used to reset the read or write counter for accessing 20 code bytes through C0WCR.

Address Offset : 0Fh

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5	R/W	0b	**CIR Wakeup Code Writing Counter Resetting Bit (WCRST)** This bit is used to reset the writing counter to 1, and it is where the first byte saved in the power-switch-code area. After the counter is reset, this bit will be reset to 0.
4	R/W	0b	**CIR Wakeup Code Reading Counter Resetting Bit (RCRST)** This bit is used to reset the reading counter to 1, and it is where the first byte is saved in the power-switch-code area.
3	-	-	**Reserved**
2	R/W	0b	**CIR Power On/Off Interrupt Identification (CIRPOII)** This bit is set to denote that the CIR Power On/Off interrupt(INT15) event has occurs . Writing 0 clears this identification bit.
1	R	0b	**CIR Power On/Off Interrupt Status (CIRPOIS)** This bit is set to denote that the CIR Power On request event has been generated by the CIR Remote-Controller-pressed power on/off key. Setting 0 denotes that the CIR Power Off request event has been generated by the CIR Remote-Controller-pressed power on/off key.
0	R/W	0b	**CIR Power On/Off Status Interrupt Enable (CIRPOSIE)** This bit is set to enable the CIR Power On/Off interrupt event(INT15), which is generated by the CIR Remote-Controller-pressed power on/off key. Setting 0 to disable interrupt by the Power on/off event.

7.20.5.17 CIR Scratch Register (CSCRR)

Address Offset: 10h

Bit	R/W	Default	Description
7	EC side: R/W Host side: R	0b	**Page mode** 0: 2-page selected, to be compatible with old version firmware 1: 3-page selected, two consecutive writing cycles to HRAE to switch page
6	-	-	**Reserved**
5-0	R/W	00h	**Scratch Bit (SCRB5-0)** Reading returns the value that was previously written.

7.20.5.18 CIR General Purpose Interrupt (CGPINTR)

Address Offset: 01h on Page 2 (Host View Only)

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	W	-	**CIR General Purpose Interrupt (CGPINT)** Writing 1 to this bit will issue an interrupt to INT36.

7.21 Serial Peripheral Interface (SSPI)

7.21.1 Overview

The SPI device uses 3-wire bi-directional or 4-wire interface for data transmission. The 4-wire device consists four signals, SSCE#, SSCK, SMOSI, and SMISO, for data transmission, and the 3-wire device consists three signals, SSCE#, SSCK, SMISO, for data transmission. The SPI interface consists of two identical channels which can be selected to connect to the 3-wire or 4-wire device.

7.21.2 Features

- Supports both Host and EC side.
- Supports eight frequency dividers of SSCK. (2, 4, 6, 8, 10, 12, 14, 16)
- Supports n-bit transmission (n = 1 ~ 8).
- Supports blocking and non-blocking selection.
- Supports Interrupt enable and Interrupt disable in the non-blocking selection.
- Supports 3-wire SPI device and 4-wire SPI device.
- Supports four clock modes.
- Supports BUSY pin.

7.21.3 Functional Description

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. The interfacne supplies the synchronous clock (SSCK) for the serial interface and initiates the data transfer.

The device responds by sending (or receiving) the requested data. The device uses the interface clock to serially shift data out (or in) while the interface shifts the data in (or out).

7.21.3.1 Data Transmissions

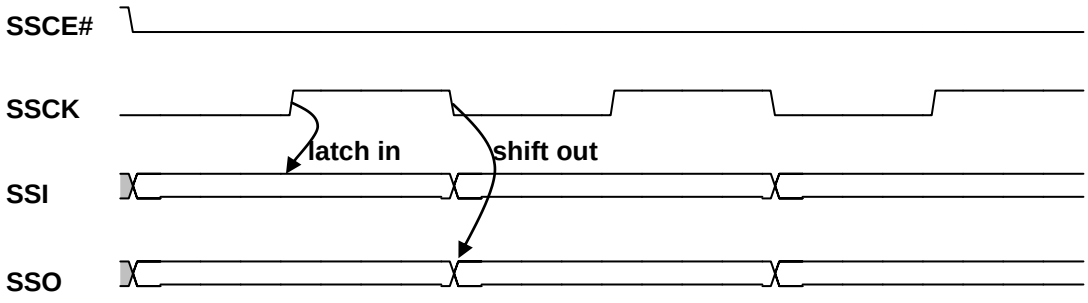
8-bit Transmission
The interface supports 8-cycle SSCK for data transmission. It is available for 1-byte transaction devices. (default)

N-bit Transmission (N = 1 ~ 7)
The interface supports N-cycle SSCK for data transmission. It is available for non-1-byte transaction devices.

7.21.3.2 SPI Mode

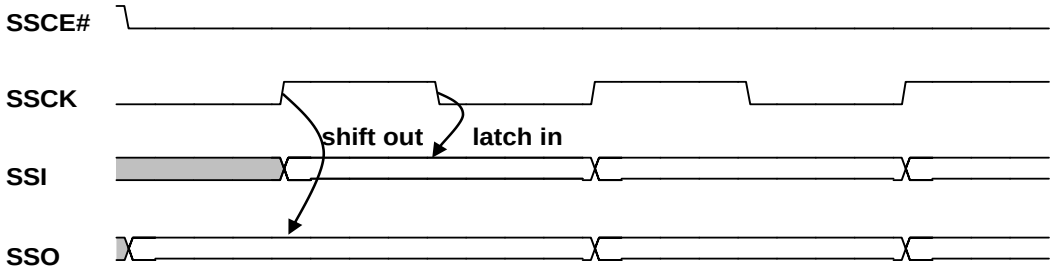
Mode 0
SSCK is low in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Figure 7-35. SPI Mode 0 Waveform



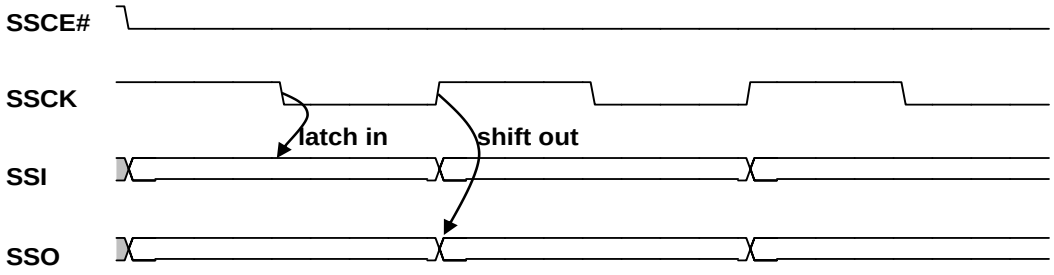
Mode 1
SSCK is low in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge.

Figure 7-36. SPI Mode 1 Waveform



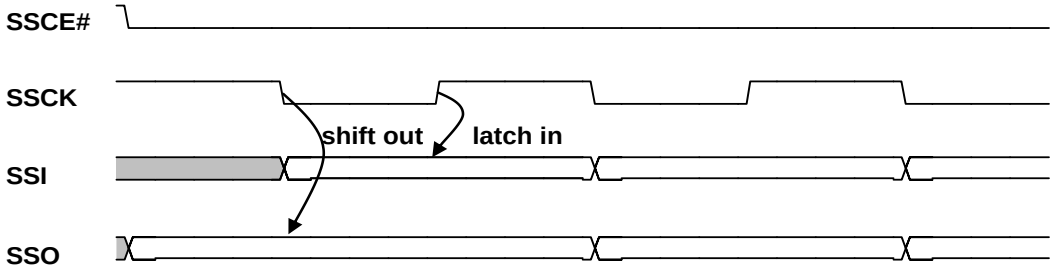
Mode 2
SSCK is high in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge.

Figure 7-37. SPI Mode 2 Waveform



Mode 3
SSCK is high in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Figure 7-38. SPI Mode 3 Waveform



7.21.3.3 Blocking and Non-blocking mode

- Blocking mode:

After starting the read cycle or write cycle to the SPI module (writing 1 to CH0START or CH1START bit in SPISTS register), the bus will be blocked until this read/write command is finished.

If the SPI function is controlled by the EC side, CPU instruction will be halted until this read/write command is finished.

If the SPI function is controlled by the host side, the LPC bus will return the long-wait sync pattern until this read/write command is finished.

It means that the interrupt and the polling are not needed.

- Non-blocking mode

After starting the read cycle or write cycle to the SSPI module (writing 1 to CH0START or CH1START bit in SPISTS register), the processor receives an interrupt signal or polls bit 2 of SPISTS register to determine if this read/write command will be terminated .

7.21.4 Host Interface Registers

The registers of SSPI can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The SSPI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-38. Host View Register Map, SSPI

7 — 0		Offset
SPI Data Register (SPIDATA)		00h
SPI Control Register 1 (SPICTRL1)	Bank 0	01h
SPI Control Register 2 (SPICTRL2)		02h
SPI Control Register 3 (SPICTRL3)	Bank 1	01h
SPI Start and End Status Register (SPISTS)		03h

All registers are double mapped into the host and EC side, however, the SSPI function should be controlled by a side only.

7.21.5 EC Interface Registers

The register map of EC interface is listed below. The base address for SSPI is 2600h.

Table 7-39. EC View Register Map, SSPI

7 — 0	Offset
SPI Data Register (SPIDATA)	00h
SPI Control Register 1 (SPICTRL1)	01h
SPI Control Register 2 (SPICTRL2)	02h
SPI Control Register 3 (SPICTRL3)	04h
SPI Start and End Status Register (SPISTS)	03h

Other related register(s):
- General Control 1 Register (GCR1), SPICTRL bit
- General Control 1 Register (GCR1), SSSPIBP bit
- General Control 3 Register (GCR3), SSPIPDG bit

7.21.5.1 SPI Data Register (SPIDATA)

In the read mode, the register holds the shift data from the SPI device. In the write mode, the interface shift the data out to the SPI device.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**SPI Data (DATA)** Receive Data from the SPI device or Transmit Data to the SPI device.

7.21.5.2 SPI Control Register 1 (SPICTRL1)

This register controls the SPI operation mode.

Address Offset: Host: 01h (Bank 0) / EC: 01h

Bit	R/W	Default	Description
7	R/W	0b	**Chip Select Polarity (CHPOL)** If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 0. Otherwise, the bit indicates both the chip select polarity of device 0 and device 1 0: Active low 1: Active high
6-5	R/W	00b	**Bit 6:Clock Polarity (CLPOL)** 0: SSCK is low in the idle mode. 1: SSCK is high in the idle mode. **Bit 5:Clock Phase (CLPHS)** 0: Latch data on the first SSCK edge. 1: Latch data on the second SSCK edge. **Mode 0:** SSCK is low in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge. **Mode 1:** SSCK is low in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge. **Mode 2:** SSCK is high in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge. **Mode 3:** SSCK is high in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.
4-2	R/W	000b	**SSCK Frequency (SCKFREQ)** **000b:** 1/2 FreqEC **001b:** 1/4 FreqEC **010b:** 1/6 FreqEC **011b:** 1/8 FreqEC **100b:** 1/10 FreqEC **101b:** 1/12 FreqEC **110b:** 1/14 FreqEC **111b:** 1/16 FreqEC (FreqEC is listed in Table 10-2 on page 530)

Bit	R/W	Default	Description
1	R/W	0b	**Interrupt Enable (INTREN)** 0: Disable 1: Enable
0	R/W	0b	**Device0 3-Wire Mode (3WIRECH0)** 0: Disable (4-wire) 1: Enable (3-wire)

7.21.5.3 SPI Control Register 2 (SPICTRL2)

This register controls the SPI operation mode.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side Bank (HBANK)** The bit is only available in host side. 0: bank 0 1: bank 1
6	R/W	0b	**Device Busy Polarity (DEVBUSYPOL)** The bit indicates the state of the device busy signal when the device is not busy.
5-3	R/W	000b	**Byte Width (BYTEWIDTH)** 000b: 8-bit transmission 001b: 1-bit transmission 010b: 2-bit transmission 011b: 3-bit transmission 100b: 4-bit transmission 101b: 5-bit transmission 110b: 6-bit transmission 111b: 7-bit transmission
2	R/W	0b	**Channel Read/Write Cycle (CHRW)** 0: Write cycle 1: Read cycle
1	R/W	0b	**Block Select (BLKSEL)** 0: Non-blocking selection 1: Blocking selection
0	R/W	0b	**Device1 3-Wire Mode (3WIRECH1)** 0: Disable (4-wire) 1: Enable (3-wire)

7.21.5.4 SPI Start and End Status Register (SPISTS)

This register reports the status of the SPI and controls the start and end signal.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/WC	0b	**Wait Busy Start Signal (WAITBUSYSTART)** Write 1 to start the Wait Busy function after a write command or a read command. Read 0b.
6	R	-	**Device Busy Signal (DEVBUSY)** The bit indicates the device busy signal.
5	R/WC	0b	**SPI Transmission End (TRANEND)** Write 1 to end the SPI transmission. Read 0b.
4	R/WC	0b	**Channel 0 Start Signal (CH0START)** Write 1 to start the data transmission of device 0. Read 0b.
3	R/WC	0b	**Channel 1 Start Signal (CH1START)** Write 1 to start the data transmission of device 1. Read 0b.
2	R	0b	**Transfer In Progress (TRANIP)** This bit indicates the SPI is in the transmission state. 0: Data transfer is not in progress. 1: Data transfer is in progress.
1	R/WC	0b	**Transfer End Flag(TRANENDIF)** This bit indicates SPI transmission ends. The bit will be 1 when writing 1 to TRANEND bit. Write 1 to clear this bit and terminate data transmission.
0	R	0b	**SPI Busy (SPIBUSY)** This bit indicates whether the SPI interface is busy or not. 0: SPI idle 1: SPI busy

7.21.5.5 SPI Control Register 3 (SPICTRL3)

This register controls the SPI operation mode.

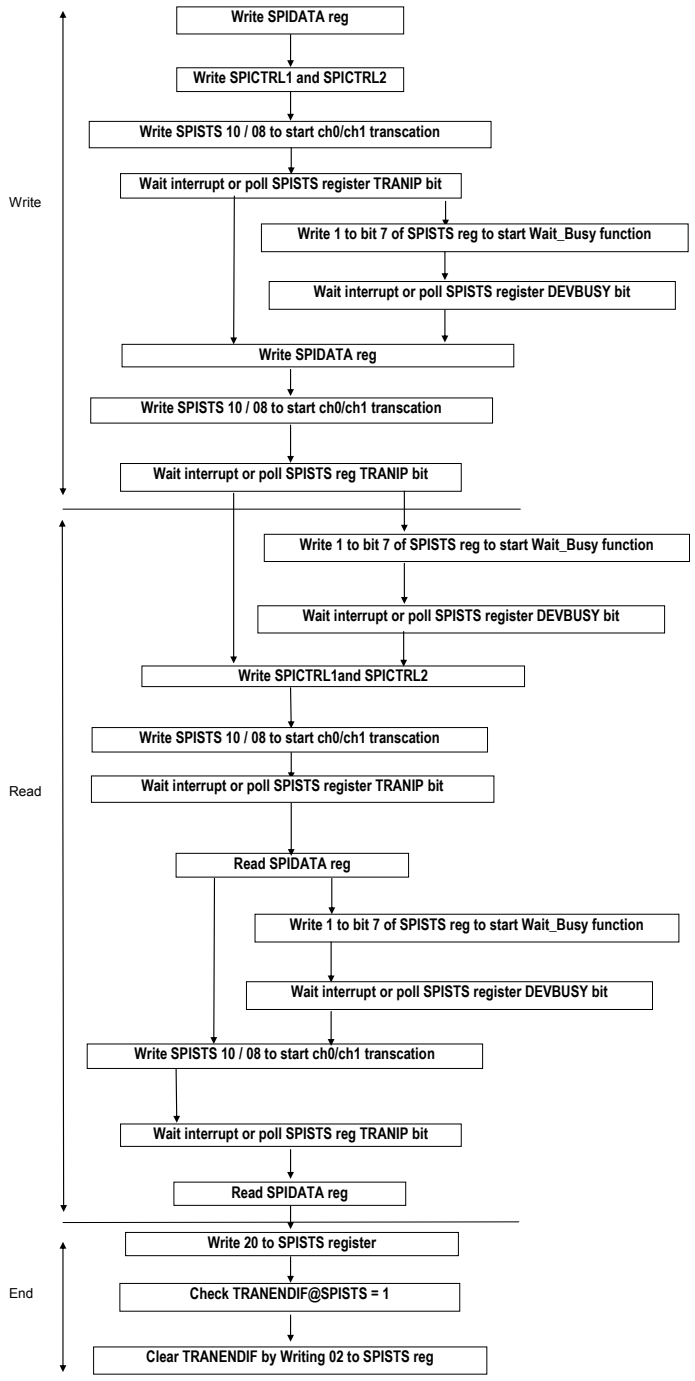
Address Offset: Host: 01h (Bank 1) / EC: 04h

Bit	R/W	Default	Description
7-3	R	-	**Reserved**
2	R/W	0b	**Chip Select Polarity Select (CSPOLSEL)** 0: The chip select polarity of device 1 and device 0 is the same. 1: The chip select polarity of device 1 and device 0 is different.
1	R/W	0b	**Chip Select Polarity 1 (CHPOL1)** If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 1. 0: Active low 1: Active high
0	R/W	0b	**No BUSY Clock (BUSYNOCLK)** 0: Generate SSPI clock when waiting for the device busy signal. 1: Do not generate SSPI clock when waiting for the device busy signal.

7.21.6 Programming Guide

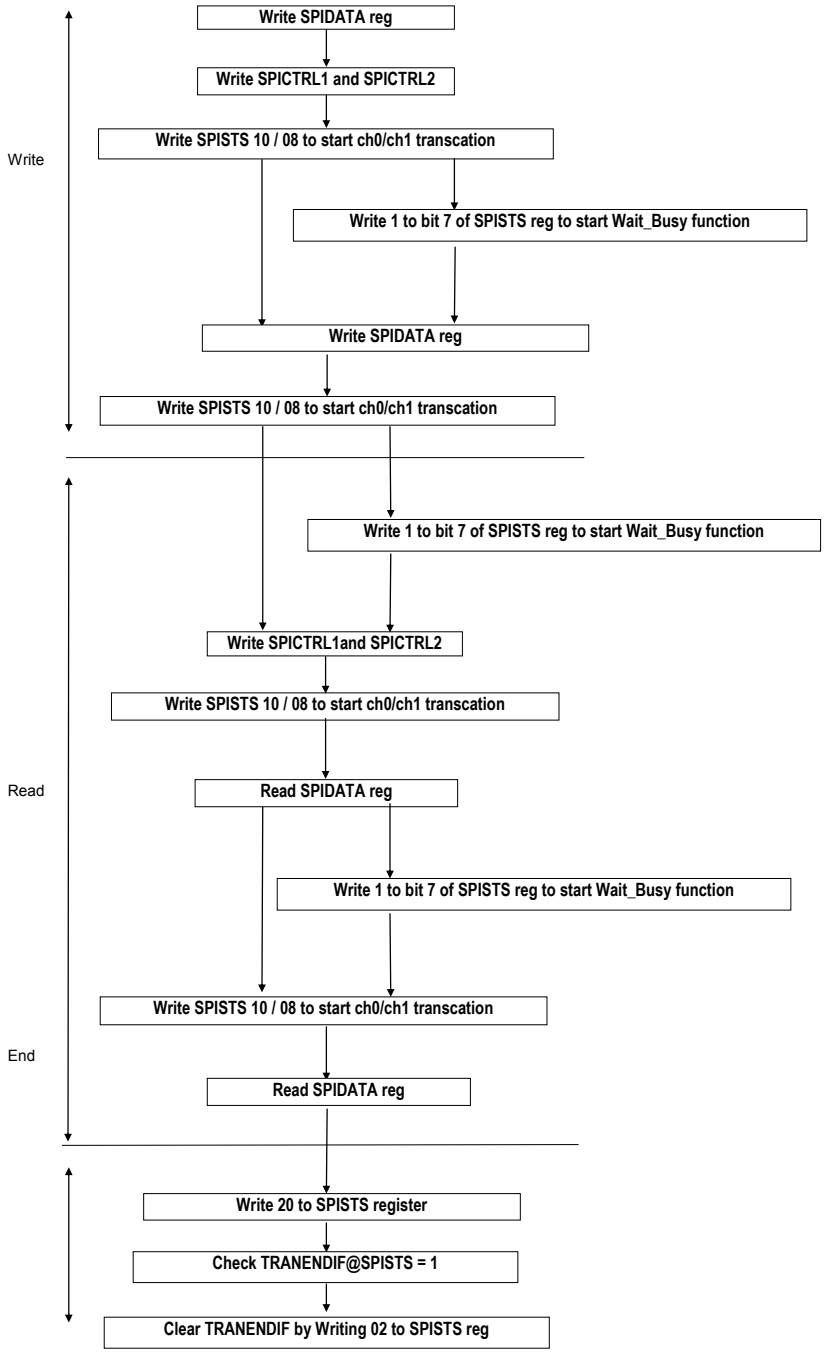
Write 16-bit data to SPI device and read 16-bit data from SPI device.

Figure 7-39. Program Flow Chart for SSPI Non-blocking



Write 16-bit data to SPI device and read 16-bit data from SPI device.

Figure 7-40. Program Flow Chart for SSPI Blocking



7.22 Serial Port (UART)

7.22.1 Overview

UART1 can be accessed by software in the host or EC side, however, the UART1 function should be controlled by a side only.
So is UART2.

The UART1/UART2 module is 16550 compatible. This module performs the serial to parallel conversion for the received data, and parallel to serial conversion for the transmitted data.

7.22.2 Features

- Programmable FIFO or character mode
- The 16-byte FIFO buffer is on the transmitter and receiver in the FIFO mode
- Add or delete standard asynchronous communication bits (start, stop and parity) to or from serial data.
- The programmable baud rate generator allows the division of input clock by 1 to 2^16-1 and generates the internal 16X clock.
- Modem control function (CTS#, RTS#, DTR#, DSR#, RI#, DCD#)
- Fully programmable serial-interface characteristics: 5, 6, 7 or 8-bit character
- Even, odd, forced 0/1 or no parity bit generation and detection
- 1, 1½, or 2 stop bits generation
- Baud rate up to 115.2K
- Baud rate up to 230.4K/460.8K if high speed mode enabled
- False start bit detection
- Receiver/Transmitter can be enabled separately.

7.22.3 Functional Description

UART contains a programmable baud rate generator that is capable of dividing the input clock by a number from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts. Besides, if the High Speed Baud Rate Select (HHS) or EC High Speed Select (ECHS) is activated, the highest baud rate can be up to 230.4K and 460.8K, which are determined by the divisor of the baud rate generator.

7.22.4 Host Interface Registers

The registers of UART1/UART2 can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The UART resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. These registers are listed below:

Table 7-40. Host/EC View Register Map, UART

			Index
Receiver Buffer Register (RBR)	if DLAB=0	R	00h
Interrupt Enable Register (IER)	if DLAB=0	R/W	01h
Interrupt Identification Register (IIR)		R	02h
Line Control Register (LCR)		R/W	03h
Modem Control Register (MCR)		R/W	04h
Divisor Latch LSB Register (DLL)	if DLAB=1	R/W	00h
Divisor Latch MSB Register (DLM)	if DLAB=1	R/W	01h
Line Status Register (LSR)		R/W	05h
Modem Status Register (MSR)		R/W	06h
Scratch Pad Register (SCR)		R/W	07h
Transmitter Holding Register (THR)		W	00h
FIFO Control Register (FCR)		W	02h
EC Serial Port Mode Register (ECSPMR)	EC View	R/W	08h

All registers are double mapped into the host and EC side except that ECSPMR is only for EC side; however, the UART function should be controlled by a side only.

7.22.5 EC Interface Registers

The register map of EC interface is the the same as Host interface registers. The base address for UART1 is 2700h and the base address for UART2 is 2800h.

Other related register(s):
- General Control 1 Register (GCR1), U1CTRL bit
- General Control 1 Register (GCR1), U2CTRL bit
- General Control 3 Register (GCR3), UART1PDG bit
- General Control 3 Register (GCR3), UART2PDG bit

7.22.5.1 Receiver Buffer Register (RBR)

This register receives and holds the entering data. It contains a non-accessible shift register that converts the incoming serial data stream to a parallel 8-bit word.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	00h	**Receiver Buffer Register (URBR)** This register receives and holds the entering data.

7.22.5.2 Transmitter Holding Register (THR)

This register holds and transmits the data via a non-accessible shift register. It converts the outgoing parallel data to a serial stream before transmission.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	W	-	**Transmitter Holding Register (THR)** This register holds and transmits the data via a non-accessible shift register.

7.22.5.3 Interrupt Enable Register (IER)

IER is used to enable (or disable) four active high interrupts that activate the interrupt outputs with its lower four

bits, bit 0-bit 3.

Address Offset: 01h

Bit	R/W	Default	Description
7-4	R	0h	**Reserved** These bits are always “0”.
3	R/W	-	**Enable Modem Status Interrupt (EMSI)** Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit state.
2	R/W	-	**Enable Receiver Line Status Interrupt (ERLSI)** Set this bit high to enable the receiver line status interrupt, which is caused when overrun, parity, framing or break occurs.
1	R/W	-	**Enable Transmitter Holding Register Empty Interrupt (ETHREI)** Set this bit high to enable the transmitter holding register empty interrupt.
0	R/W	-	**Enable Received Data Available Interrupt (ERDVI)** Set this bit high to enable the received data available interrupt (and time-out interrupt in the FIFO mode).

7.22.5.4 Interrupt Identification Register (IIR)

Address Offset: 02h

Bit	R/W	Default	Description
7-6	R	00b	**Interrupt Identification Register Bit 7, Bit 6 (IIR7, IIR6)** These bits are set when FCR[0] is equal to 1.
5-4	R	00b	**Reserved** Always logic 0.
3	R	0b	**Interrupt Identification Register Bit 3 (IIR3)** In the non-FIFO mode, this bit is logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
2-1	R	00b	**Interrupt Identification Register Bit 2, Bit 1 (IIR2, IIR1)** These bits are used to identify the highest priority pending interrupt.
0	R	1b	**Interrupt Identification Register Bit 0 (IIR0)** This bit is used to indicate a pending interrupt in either a hard-wired prioritized or a polled environment with a logic 0 state. When the condition takes place, IIR contents may be used as a pointer to the appropriate interrupt service routine.

Table 7-41. Interrupt Control Functions

IIR				Interrupt Set and Reset Functions			
Bit3	**Bit2**	**Bit1**	**Bit0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	-	None	None	-
0	1	1	0	1st	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	2nd	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or FIFO drops below the Trigger Level
1	1	0	0	2nd	Character Timeout Identification	There is at least one character in the FIFO but no character has been input to the FIFO or read from it for the last four Char times.	Reading the Receiver Buffer Register
0	0	1	0	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if the source of interrupt is THRE) or Writing into the THR
0	0	0	0	4th	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

7.22.5.5 FIFO Control Register (FCR)

This register is used to enable, and clear the FIFO, and set the RCVR FIFO trigger level.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	W	00b	**FIFO Control Register Bit 7, Bit 6 (FCR7,FCR6)** These bits set the trigger level for the RCVR FIFO interrupt. **FCR7 FCR6 RCVR FIFO Trigger Level** 0 0 1 byte 0 1 4 bytes 1 0 8 bytes 1 1 14 bytes
5-4	W	00b	**Reserved**
3	W	0b	**Reserved** This bit does not affect the serial channel operation. RXRDY and TXRDY functions are not available on this controller.
2	W	0b	**XMIT FIFO Reset (XFRST)** This self-clearing bit clears all contents of XMIT FIFO and resets its related counter to 0.
1	W	0b	**RCVR FIFO Reset (RFRST)** Set this self-clearing bit to logic “1” to clear all contents of RCVR FIFO and resets its related counter to 0 (except the shift register).
0	W	0b	**FIFO Enable (FEN)** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs will be disabled and cleared when this bit is cleared to low. This bit has to be a logic “1” if the other bits of the FCR are written or they will not be properly programmed. When this register is changed to the non-FIFO mode, all contents will be cleared.

7.22.5.6 Divisor Latch LSB (DLL)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Divisor Latch LSB (DLL)** This register stores the low byte of the divisor.

7.22.5.7 Divisor Latch MSB (DLM)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Divisor Latch LSB (DLM)** This register stores the high byte of the divisor.

Table 7-42. Baud Rate Using 1.8432MHz Clock

Desired Baud Rate	Divisor Used	Percent Error Difference[1]	High Speed Bit[2]
50	2304	-	X
75	1536	-	X
110	1047	0.1247	X
134.5	857	0.0409	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.5916	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	-	X
57600	2	-	X
115200	1	-	X
230400	32770	-	1
460800	32769	-	1

Note[1]: The percent error difference, which is between the desired and the actual value, for all baud rates is 0.0986% except where the baud rates are indicated otherwise.
Note[2]: The high speed bit indicates whether the HHS bit or ECHS bit is set to high or not.

7.22.5.8 Scratch Pad Register (SCR)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	-	**Scratch Pad Register (SCR)** This 8-bit register does not control the operation of UART in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general-purpose data.

7.22.5.9 Line Control Register (LCR)

LCR controls the format of the data character and provides the information of the serial line.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W	-	**Divisor Latch Access Bit (DLAB)** This bit has to be set high to access the Divisor Latches of the baud rate generator during read or write operation and set low to access the Data Register (RBR and THR) or the Interrupt Enable Register.
6	R/W	-	**Break Control (BREAK)** This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will remain until a low level resets this bit, enabling the serial port to alert the terminal in a communication system.
5	R/W	-	**Stick Parity Bit (SP)** When this bit and Parity Enable (PEN) bit are high at the same time, the parity bit is transmitted and then detected by the receiver. On the contrary, the parity bit is detected by Even Parity Select (EPS) bit to force the parity to a known state and to check the parity bit in a known state.
4	R/W	-	**Even Parity Select (EPS)** When the parity is enabled (Parity Enable=1), EPS=0 selects odd parity, and EPS=1 selects even parity.
3	R/W	-	**Parity Enable (PEN)** A parity bit, between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when this bit is high.
2	R/W	-	**Stop Bit Select (STB)** Specify the number of stop bits in each serial character, which is summarized below: **STB** **Word Length** **No. of Stop Bit** 0 - 1 bit 1 5 1.5 bits 1 6 2 bits 1 7 2 bits 1 8 2 bits **Note:** The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.
1-0	R/W	-	**Word Length Select Bit 1, Bit 0 (WLS1, WLS0)** Specify the number of bits in each serial character, which is encoded below: **WLS1** **WLS0** **Word Length** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits

7.22.5.10 Modem Control Register (MCR)

Address Offset: 04h

Bit	R/W	Default	Description
7-5	R	000b	**Reserved** Bit 7-5 are always low.
4	R/W	0b	**Loop** This bit provides a loopback feature for the diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State. Shift Register output Loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected, and the four are forced to inactive high. The transmitted data are immediately received, allowing the processor to verify the data paths of transmitting and receiving of the serial channel.
3	R/W	0b	**OUT2** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	-	0b	**OUT1** This bit does not have an output pin and can only be read or written by the processor.
1	R/W	0b	**Request To Send (RTS)** This bit controls the Request to Send (RTS#), which is in an inverse logic state with it.
0	R/W	0b	**Data Terminal Ready (DTR)** This bit controls the Data Terminal Ready (DTR#), which is in an inverse logic state with it.

7.22.5.11 Line Status Register (LSR)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	0b	**Error In RCVR FIFO (ERF)** In the 16550 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads LSR if there are no subsequent errors in the FIFO.
6	R	1b	**Transmitter Empty (TEMT)** This read-only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty; otherwise, this bit is “0”. It has the same function in the FIFO mode.
5	R	1b	**Transmitter Holding Register Empty (THRE)** This read-only bit indicates that the THR is empty, and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to XMIT FIFO.
4	R/W	0b	**Break Interrupt (BI)** This bit indicates that the last received character is a break character. The break interrupt status bit will be asserted only when the last received character, parity bits and stop bits are all break bits. When any of these error conditions is detected (LSR[1] to LSR[4]), a Receiver Line Status interrupt (priority 1) will be produced in IIR with IER[2] previously enabled.

Bit	R/W	Default	Description
3	RC	0b	**Framing Error (FE)** When this bit is a logic 1, it indicates that the stop bit in the received character is not valid. It is reset low when the CPU reads the contents of LSR.
2	RC	0b	**Parity Error (PE)** This bit Indicates the parity error (PE) with a logic "1", representing that the received data character does not have the correct even or odd parity as bit 3 of LCR (Parity Enable) is set to "1". It will be reset to "0" whenever LSR is read by CPU.
1	RC	0b	**Overrun Error (OE)** Overrun Error (OE) bit is set as a logic "1" after RBR has been overwritten by the next character before it is read by CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when CPU reads LSR.
0	R/W	0b	**Data Ready (DR)** A logic "1" indicates a character has been received by RBR. A logic "0" indicates all data in the RBR or RCVR FIFO have been read.

7.22.5.12 Modem Status Register (MSR)

This 8-bit register provides the current state of the control lines from modems or peripheral devices. In addition to this current state information, bit 7-4 can provide the change information when a modem control input changes the state. It will be reset to low when the processor reads MSR.

Address Offset: 06h

Bit	R/W	Default	Description
7	R	0b	**Data Carrier Detect (DCD#)** This bit indicates the complement status of Data Carrier Detect input. If bit 4 of MCR is 1, this bit is equivalent to OUT2 of MCR.
6	R	0b	**Ring Indicator (RI#)** This bit indicates the complement to the RI# input. If bit 4 of MCR is 1, this bit is equivalent to OUT1 in MCR.
5	R	0b	**Data Set Ready (DSR#)** This bit indicates the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (bit 5 of MCR is 1), this bit is equivalent to DTR# in the MCR.
4	R	0b	**Clear to Send (CTS#)** This bit indicates the complement of CTS# input. If the serial channel is in the loop mode (bit 4 of MCR is 1), this bit is equivalent to RTS# in MCR.
3	R/W	0b	**Delta Data Carrier Detect (DDCD)** This bit indicates that the DCD# input state has been changed since the last time it is read by the processor.
2	R/W	0b	**Trailing Edge of Ring Indicator (TERI)** This bit indicates that RI input state to the serial channel has been changed from a low to high state since the last time it is read by the processor. The change of logic 1 doesn't activate TERI.
1	R/W	0b	**Delta Data Set Ready (DDSR)** A logic "1" indicates that DSR# input state to the serial channel has been changed since the last time it is read by the processor.
0	R/W	0b	**Delta Clear to Send (DCTS)** This bit indicates the CTS# input state to the serial channel has been changed since the last time it is read by the processor.

7.22.5.13 EC Serial Port Mode Register (ECSPMR)

Address Offset: 08h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved** Bit 7-2 are always low.
1	R/W	0b	**EC High Speed Select (ECHS)** This bit indicates that the supported baud rate of UART1/UART2 can be up to 230.4K and 460.8K, which are determined by the divisor of the baud rate generator. (From EC Side) 0: Not selected 1: Selected
0	-	0b	**Reserved** This bit is always low.

7.22.6 Programming Guide

Each serial channel is programmed by control registers whose contents define the character length, number of stop bits, parity, baud and modem interface. Although the control registers can be written in any order, IER should be the last because it controls whether the interrupt is enabled. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

7.22.6.1 Programming Sequence

UART module in Intelligent Peripheral Controller is compatible with standard 16550. The following is the programming sequence for standard 16550 compatible component register.

For access RBR/THR:
1. Set bit 7 of the LCR register to “0”.
2. Access RBR/THR.

For Access IER:
1. Set bit 7 of the LCR register to “0”.
2. Access IER.

For Access DLL/DLM:
1. Set bit 7 of the LCR register to “1”.
2. Access DLL/DLM.

7.22.7 Software Reset

This method allows returning to a completely known state without a system reset. It consists of writing the required data to LCR, DLL, DLM and MCR. LSR and RBR has to be read before enabling interrupts in order to clear any residual data or status bits that may be invalid for the subsequent operations.

If UART function is controlled by the EC side, it can be done by writing 1 to the corresponding bit in RSTC4 register, too.

7.22.8 Clock Input Operation

The input frequency of the Serial Channel is FreqEC/5, not exactly 1.8432 MHz.
FreqEC is listed in Table 10-2 on page 530.

7.22.9 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When bit 0 of FCR and bit 0 of IER are set to 1, RCVR FIFO and receiver interrupts are enabled. RCVR interrupt occurs under the following conditions:

A. The received data available interrupt and the IIR receive data available indication will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.

B. The receiver line status interrupt has higher priority than the received data available interrupt.

C. The time-out timer will be reset after receiving a new character or after the processor reads RCVR FIFO whenever a time-out interrupt occurs.

RCVR FIFO time-out Interrupt: By enabling RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

A. It will occur only if there is at least one character in FIFO whenever the period between the most recent received serial character and the most recent processor read from the FIFO is longer than the period of four consecutive character-time.
B. The time-out timer will be reset after receiving a new character or after the processor reads RCVR FIFO whenever any time-out interrupts occur. The timer will be reset when the processor reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting bit 0 of FCR and bit 1 of IER to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt will occur as follows:

A. The transmitter interrupt will occur when XMIT FIFO is empty, and it will be reset if THR is written or IIR is read.
B. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following conditions occurs:
THRE=1 and there are not at least two bytes in the transmitter FIFO at the same time since the last THRE=1. The transmitter interrupt will be issued immediately after the bit 0 of FCR is changed. Once it is enabled, the THRE indication is delayed for 1 character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation (Bit 0 of FCR is 1, and bit 0, 1, 2, 3 of IER or all are 0.)
Either one or both XMIT and RCVR can be in this operation mode in which the program will check RCVR and XMIT status via the LSR as described below:

LSR[7]: RCVR FIFO error indication.
LSR[6]: XMIT FIFO and Shift register empty.
LSR[5]: The XMIT FIFO empty indication.
LSR[4] – LSR[1]: Specify that errors have occurs, and the character error status is handled in the same way as in the interrupt mode. IIR is not affected since IER(2)=0.
LSR[0]: This bit is high whenever RCVR FIFO contains at least one byte. There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode.

7.22.10 High Speed Baud Rate Activation

When the high speed baud rate select bit is set to 1 from host side (High Speed Baud Rate Select ; HHS) or EC side (EC High Speed Select ; ECHS), the highest baud rate of UART1/UART2 can be up to 230.4K or 460.8K, which are determined by the divisor of the baud rate generator.

If HHS or ECHS is set to 1 and the divisor is 32770, the baud rate is 230.4K.
If HHS or ECHS is set to 1 and the divisor is 32769, the baud rate is 460.8K.

7.23 Debug UART

7.23.1 Overview

The Debug UART module is likely IT8051 UART. This module performs the serial to parallel conversion for the received data, and parallel to serial conversion for the transmitted data.

7.23.2 Features

- Supports full duplex UART

7.23.3 Functional Description

7.23.4 EC Interface Registers

The register map of EC interface is listed below. The base address for Debug UART is 3700h.

Table 7-43. EC View Register Map, Debug UART

7	0	Offset
Serial Port Control Register (SCON)		01h
Timer 1 High Byte Register (TH1R)		02h
Timer 1 Low Byte Register (TL1R)		03h
Serial Port Buffer Register (SBUFR)		04h
Serial Port Control Register (SCTRL)		05h
Timer Mode Register (TMOD)		06h
Timer Control Register (TCON)		07h
Clock Control Register (CKCON)		08h

7.23.4.1 Serial Port Control Register (SCON)

Address Offset: 01h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Receive Enable (REN)** Receiver enable bit. Setting ‘1’ enables the serial data reception. Setting ‘0’ disables the serial data reception.
3	R/W	0b	**Transmit Bit 8 (TB8)** Transmit bit 8, set/cleared by hardware to determine the state of the ninth data bit transmitted in 9-bit UART mode.
2	R/W	0b	**Receive Bit 8 (RB8)** Receive bit 8, set/cleared by hardware to determine the state of the ninth data bit received in 9-bit UART mode.
1	R/W	0b	**Transmit Interrupt (TI)** Transmit interrupt, set by hardware when the byte is transmitted and cleared by software after serving.
0	R/W	0b	**Receive Interrupt (RI)** Receive interrupt, set by hardware when the byte is received and cleared by software when data is processed.

7.23.4.2 Timer 1 High Byte Register (TH1R)

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 1 High Byte Bit [7:0] (TH1)** Timer 1 high byte register.

7.23.4.3 Timer 1 Low Byte Register (TL1R)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 1 Low Byte Bit [7:0] (TL1)** Timer 1 low byte register.

7.23.4.4 Serial Port Buffer Register (SBUFR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	00h	**Serial Port Buffer Bit [7:0] (SBUF)** This is the 8-bit serial port data buffer. Writing to **SBUF** loads the transmit buffer to the serial I/O port. Reading **SBUF** reads the receive buffer of the serial port.

7.23.4.5 Serial Port Control Register (SCTRL)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	1b	Always write 1 to this bit.
6-0	-	-	**Reserved**

7.23.4.6 Timer Mode Register (TMOD)

Address Offset: 06h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	10b	Always write 10b to this bit.
3-0	-	-	**Reserved**

7.23.4.7 Timer Control Register (TCON)

Address Offset: 07h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Timer 1 Run Control (TR1)** Setting ‘1’ enables timer 1 operation and setting ‘0’ disables timer 1.
5-0	-	000000b	**Reserved**

7.23.4.8 Clock Control Register (CKCON)

Address Offset: 08h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	1b	Always write 1 to this bit. Timer 1 clock is EC clock / 5 for easy setting baud rate 115200.
1-0	-	-	**Reserved**

7.23.5 Programming Guide

```
//Register Write
        SCON = 0x52;            // Mode1, RX Enable, TI=1, RI=0
        TMOD = 0x20;            // Using Timer1 mode1 to execute 8 bits auto reload UART
        SCTRL = 0x80;           // Set Double Baud Rate
        CKCON = 0x04;           // Timer1 clock is EC clock/5
        TH1 = 0xFF;             // Baud rate = 115200
        TCON = 0x40;            // Timer1 Enable
```

7.24 Debugger (DBGR)

7.24.1 Overview

This DBGR module provides the ability to access the instruction SRAM, data SRAM and EC side peripheral modules. Besides, it also provides a path to download or program the embedded flash, called In-system Programming (ISP).

DBGR can be performed by one of the two interfaces.
- DBGR/EPP
- DBGR/SMB

Both ISP and ISD can be performed by either DBGR/EPP or DBGR/SMB.

7.24.2 Features

- ISP and ISD
- EC Memory Snoop (ECMS = I2EC + D2EC)

7.24.3 Functional Description

7.24.3.1 DBGR/EPP

Refer to section 7.25 Parallel Port (PP).
It can be disabled by OVRPPK bit in the KSICTRLR register.
Hot-plug is available.

7.24.3.2 DBGR/SMB

Refer to section 7.7.3.2 SMBus Slave Interface.
There is another dedicated SMBus slave for this function.
It can be disabled by OVRSMDBG bit in SLVISELR register.
Hot-plug is available, but can not exit DBGR mode after being detected.

7.24.3.3 In-system Programming Operation

It provides flash read and program function.

7.24.3.4 In-system Debugging Operation

It's performed by the utility provided by ITE and contains two features below.
1. D2EC described in section 7.24.3.5 EC Memory Snoop (ECMS).
2. Breakpoints, stepping, etc. and reset functions supported.

7.24.3.5 EC Memory Snoop (ECMS)

ECMS is available through one of the two ways:

1. I2EC (I-bus to EC Memory)
Local machine snoops EC memory through the LPC I/O cycle.

Here are two registers to provide the way to perform the I2EC access.
- I2EC_ADDR_H/I2EC_ADDR_L/I2EC_DATA register, defined in section 6.3.2.9 Depth 2 I/O Address (D2ADR) on page 78.
- I2EC_XADDR_H/ I2EC_XADDR_L/I2EC_XDATA register, with programmable address and defined in section 7.17.4.21 Port I2EC High-Byte Register (PI2ECH) on page 447.

Figure 7-41. I2EC through 2Eh/2Fh I/O Port Operation Flow

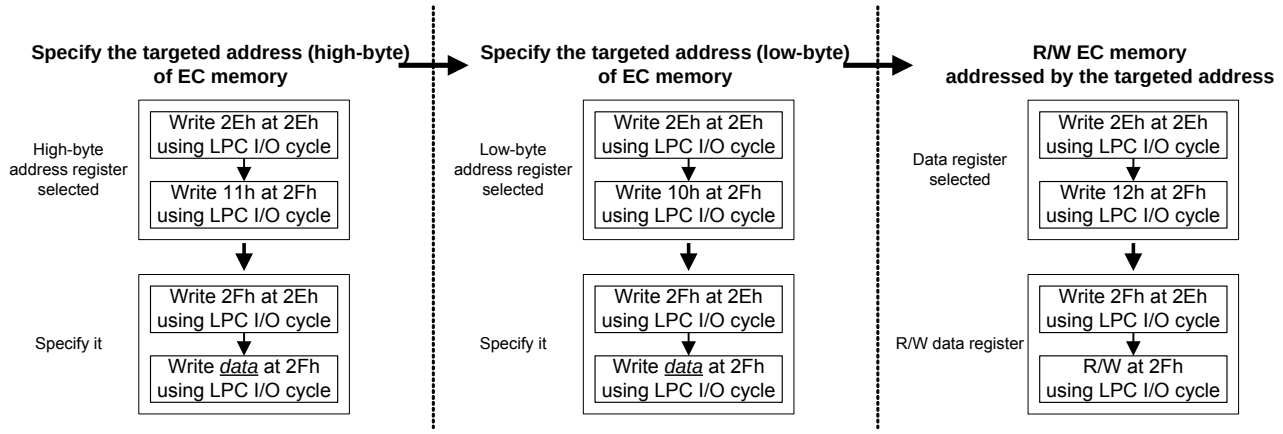
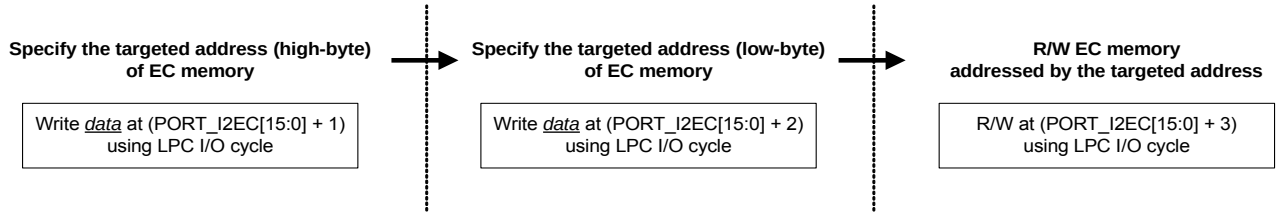


Figure 7-42. I2EC through Dedicated I/O Port Operation Flow



2. D2EC (DBGR to EC Memory)
Remote machine snoops EC memory through EPP cycle.

I2EC/D2EC utility is provided by ITE.
I2EC is not enabled until its controlled register in the EC side register is written.
I2EC can be configured as read-only for all targets.
I2EC and D2EC can work at the same time.
I2EC/D2EC will not affect any register content of read-clear registers.
The writing action of I2EC/D2EC to F/F based register is okay, however, the result of writing to non-F/F based register is not expected. Such registers may be write-clear, or writing to start internal state-machine, etc.
If D2EC is enabled, PLL will not be power-down in the Sleep mode.

7.24.3.6 Other Debug Topics

Here some debug features not covered in this DBGR section but may be useful for users.
1. Section 6.2.4 Debug Port Function on page 70.
2. Section 6.2.4 Debug Port Function on page 70. Hardware output signals to latch port 80h data on LAD[3:0].
3. Section 7.19.3.1 P80L on page 460.

7.25 Parallel Port (PP)

7.25.1 Overview

IT5121 supports IEEE 1284 parallel port interface to allow in-system programming (ISP) or in-system debugging (ISD) regardless of running firmware code.

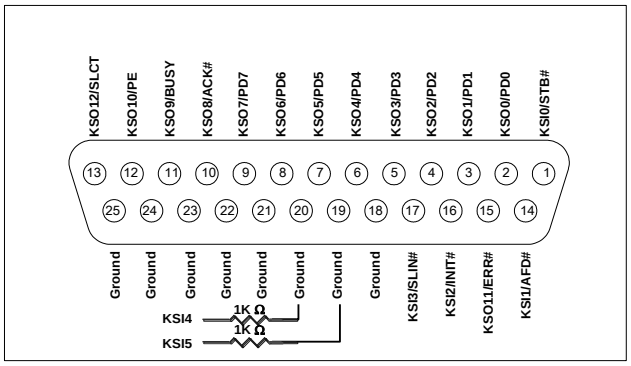
7.25.2 Features

- ISP/ISD via parallel port interface on existed KBS connector
- Fast flash programming with software provided by ITE
- Programming software supports EPP/SPP mode

7.25.3 Functional Description

7.25.3.1 KBS Connection with Parallel Port Connector

Figure 7-43. Parallel Port Female 25-Pin Connector



If Parallel Port cable is detected by internal hardware strap, the following functions will be disabled.

1. ROM Address Match Interrupt
2. Internal/External Watchdog

The DBGR/EPP debug mode takes place when VSTBY is supplied (other types of power are don't-care) and both EC chip and the flash are soldered on PCB. Parallel port interface occupies pins with the same interface as that of KBS to use the existing KBS connector.

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8. Register List

Section	Register Name	Pg	Addr
6.1.4	**EC Interface Registers, eSPI slave**	**47**	
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6.1.4.2	General Capabilities and Configurations	48	3104h-3107h
6.1.4.3	Channel 0 Capabilities and Configurations	50	3108h-310Bh
6.1.4.4	Channel 1 Capabilities and Configurations	51	310Ch-310Fh
6.1.4.5	Channel 2 Capabilities and Configurations	52	3110h-3113h
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6.1.4.8	eSPI PC Control 0 (ESPCTRL0)	57	3190h
6.1.4.9	eSPI PC Control 1 (ESPCTRL1)	57	3191h
6.1.4.10	eSPI PC Control 2 (ESPCTRL2)	57	3192h
6.1.4.11	eSPI PC Control 3 (ESPCTRL3)	57	3193h
6.1.4.12	eSPI PC Control 4 (ESPCTRL4)	58	3194h
6.1.4.13	eSPI PC Control 5 (ESPCTRL5)	58	3195h
6.1.4.14	eSPI PC Control 6 (ESPCTRL6)	58	3196h
6.1.4.15	eSPI PC Control 7 (ESPCTRL7)	58	3197h
6.1.4.16	eSPI General Control 0 (ESGCTRL0)	59	31A0h
6.1.4.17	eSPI General Control 1 (ESGCTRL1)	59	31A1h
6.1.4.18	eSPI General Control 2 (ESGCTRL2)	60	31A2h
6.1.4.19	eSPI General Control 3 (ESGCTRL3)	60	31A3h
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6.1.4.21	eSPI Upstream Control 1 (ESUCTRL1)	61	31B1h
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6.1.4.23	eSPI Upstream Control 3 (ESUCTRL3)	61	31B3h
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6.1.4.25	eSPI Upstream Control 7 (ESUCTRL7)	61	31B7h
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6.1.6	**EC Interface Registers, eSPI Queue 0**	**68**	
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6.1.6.2	PUT_OOB Data Byte 0-79 (PUTOOBDB0-79)	68	3380h-33CFh
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6.3.5.3	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	84	61h
6.3.5.4	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	84	62h
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6.3.6.5	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	86	63h
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6.3.7.4	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	87	62h
6.3.7.5	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	87	63h
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6.3.10.3	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	91	61h
6.3.10.4	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	91	62h
6.3.10.5	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	91	63h
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7.17.4.7	Reset Control 2 (RSTC2)	442	2008h
7.17.4.8	Reset Control 3 (RSTC3)	442	2009h
7.17.4.12	Base Address Select (BADRSEL)	444	200Ah
7.17.4.13	Wait Next Clock Rising (WNCKR)	444	200Bh
7.17.4.14	Special Control 5 (SPCTRL5)	444	200Ch
7.17.4.15	Special Control 1 (SPCTRL1)	445	200Dh
7.17.4.16	Reset Control Host Side (RSTCH)	445	200Eh
7.17.4.17	Generate IRQ (GENIRQ)	446	200Fh
7.17.4.10	Reset Control DMM (RSTDMMC)	443	2010h
7.17.4.9	Reset Control 4 (RSTC4)	443	2011h
7.17.4.18	Special Control 2 (SPCTRL2)	446	2012h
7.17.4.21	Port I2EC High-Byte Register (PI2ECH)	447	2014h
7.17.4.22	Port I2EC Low-Byte Register (PI2ECL)	447	2015h
7.17.4.19	Special Control 3 (SPCTRL3)	446	2016h
7.17.4.23	BRAM Interrupt Address 0 Register (BINTADDR0R)	447	2019h
7.17.4.24	BRAM Interrupt Address 1 Register (BINTADDR1R)	448	201Ah
7.17.4.25	BRAM Interrupt Control Register (BINTCTRLR)	448	201Bh
7.17.4.20	Special Control 4 (SPCTRL4)	446	201Ch
7.17.4.11	Reset Control 6 (RSTC6)	443	2029h
7.17.4.26	Port 80h/81h Status Register (P80H81HSR)	448	2030h
7.17.4.27	Port 80h Data Register (P80HDR)	448	2031h
7.17.4.28	Port 81h Data Register (P81HDR)	448	2032h
7.18	**External GPIO Controller (EGPC)**	**450**	
7.18.4	EC Interface Registers	451	
7.18.4.1	External GPIO Address Register (EADDR)	451	2100h
7.18.4.2	External GPIO Data Register (EDAT)	451	2101h
7.18.4.3	External GPIO Control Register (ECNT)	452	2102h
7.18.4.4	External GPIO Status Register (ESTS)	452	2103h
7.18.4.5	External GPIO Auto Read Control Register (EARCR)	453	2104h
7.18.4.6	External GPIO Read Enable 1 Register (ERE1R)	453	2105h
7.18.4.7	External GPIO Read Enable 2 Register (ERE2R)	454	2106h
7.18.4.8	External GPIO Read Enable 3 Register (ERE3R)	454	2107h
7.18.4.9	External GPIO Read Enable 4 Register (ERE4R)	455	2108h
7.18.4.10	External GPIO Read Enable 5 Register (ERE5R)	455	2109h
7.18.4.11	External GPIO Status Vector Register (ESVR)	456	210Ah
7.18.4.12	External GPIO Status Change Flag 1 Register (ESCF1R)	456	2110h
7.18.4.13	External GPIO Status Change Flag 2 Register (ESCF2R)	457	2111h
7.18.4.14	External GPIO Status Change Flag 3 Register (ESCF3R)	457	2112h
7.18.4.15	External GPIO Status Change Flag 4 Register (ESCF4R)	458	2113h
7.18.4.16	External GPIO Status Change Flag 5 Register (ESCF5R)	459	2114h

7.19	**BRAM**	**460**	
7.19.5	EC Interface Registers	461	
7.19.5.1	SRAM Byte n Registers (SBTn, n= 0-191)	462	22xxh
6.8	**RTC-like Timer (RTCT)**	**184**	
6.8.4	Host Interface Registers	185	
6.8.4.1	RTCT Bank 0 Register	187	
6.8.4.1.1	Seconds Register (SECREG)	187	00h
6.8.4.1.2	Seconds Alarm 1 Register (SECA1REG)	187	01h
6.8.4.1.3	Minutes Register (MINREG)	188	02h
6.8.4.1.4	Minutes Alarm 1 Register (MINA1REG)	188	03h
6.8.4.1.5	Hours Register (HRREG)	188	04h
6.8.4.1.6	Hours Alarm 1 Register (HRA1REG)	188	05h
6.8.4.1.7	Day Of Week Register (DOWREG)	188	06h
6.8.4.1.8	Date Of Month Register (DOMREG)	189	07h
6.8.4.1.9	Month Register (MONREG)	189	08h
6.8.4.1.10	Year Register (YRREG)	189	09h
6.8.4.1.11	RTCT Control Register A (CTLREGA)	190	0Ah
6.8.4.1.12	RTCT Control Register B (CTLREGB)	191	0Bh
6.8.4.1.13	RTCT Control Register C (CTLREGC)	192	0Ch
6.8.4.1.14	RTCT Control Register D (CTLREGD)	193	0Dh
6.8.4.1.15	Date of Week Alarm 1 Register (DOWA1REG)	193	0Eh
6.8.4.1.16	Date of Month Alarm 1 Register (DOMA1REG)	193	Programmed
6.8.4.1.17	Month Alarm 1 Register (MONA1REG)	193	Programmed
6.8.4.2	RTCT Bank 1 Register	193	
6.8.4.2.1	Seconds Alarm 2 Register (SECA2REG)	193	00h
6.8.4.2.2	Minutes Alarm 2 Register (MINA2REG)	194	01h
6.8.4.2.3	Hours Alarm 2 Register (HRA2REG)	194	02h
6.8.4.2.4	Date of Month Alarm 2 Register (DOMA2REG)	194	03h
6.8.4.2.5	Month Alarm 2 Register (MONA2REG)	194	04h
6.8.4.2.6	Date of Week Alarm 2 Register (DOWA2REG)	194	05h
6.8.4.3	RTCT I/O Register	195	
6.8.4.3.1	RTCT Index Register of Bank 0 (RIRB0)	195	70h
6.8.4.3.2	RTCT Data Register of Bank 0 (RDRB0)	195	71h
6.8.4.3.3	RTCT Index Register of Bank 1 (RIRB1)	195	272h
6.8.4.3.4	RTCT Data Register of Bank 1 (RDRB1)	195	273h
7.20	**Consumer IR (CIR)**	**463**	
7.20.4	Host Interface Registers	465	
7.20.5	EC Interface Registers	466	
7.20.5.1	CIR Data Register (C0DR)	466	2300h
7.20.5.2	CIR Master Control Register (C0MSTCR)	467	2301h
7.20.5.3	CIR Interrupt Enable Register (C0IER)	468	2302h
7.20.5.4	CIR Interrupt Identification Register (C0IIR)	469	2303h
7.20.5.5	CIR Carrier Frequency Register (C0CFR)	469	2304h
7.20.5.6	CIR Receiver Control Register (C0RCR)	471	2305h
7.20.5.7	CIR Transmitter Control Register (C0TCR)	474	2306h
7.20.5.8	CIR Slow Clock Control Register (C0SCK)	475	2307h
7.20.5.9	CIR Baud Rate Divisor Low Byte Register (C0BDLR)	476	2308h
7.20.5.10	CIR Baud Rate Divisor High Byte Register (C0BDHR)	476	2309h
7.20.5.11	CIR Transmitter FIFO Status Register (C0TFSR)	476	230Ah
7.20.5.12	CIR Receiver FIFO Status Register (C0RFSR)	477	230Bh

7.20.5.13	CIR Wake-Code Set Select Register (C0WCSSR)	477	230Ch
7.20.5.14	CIR Wakeup Code Length Register (C0WCL)	478	230Dh
7.20.5.15	CIR Wakeup Code Read/Write Register (C0WCR)	478	230Eh
7.20.5.16	CIR Wakeup Power Control/Status Register (C0WPS)	478	230Fh
7.20.5.17	CIR Scratch Register (CSCRR)	479	2310h
7.20.5.18	CIR General Purpose Interrupt (CGPINTR)	479	-
7.21	**Serial Peripheral Interface (SSPI)**	**480**	
7.21.5	EC Interface Registers	482	
7.21.5.1	SPI Data Register (SPIDATA)	483	2600h
7.21.5.2	SPI Control Register 1 (SPICTRL1)	483	2601h
7.21.5.3	SPI Control Register 2 (SPICTRL2)	484	2602h
7.21.5.4	SPI Start and End Status Register (SPISTS)	485	2603h
7.21.5.5	SPI Control Register 3 (SPICTRL3)	485	2604h
7.22	**Serial Port (UART)**	**488**	
7.22.4	Host Interface Registers	488	
7.22.5	EC Interface Registers	489	
7.22.5.1	Receiver Buffer Register (RBR)	489	2700h
7.22.5.2	Transmitter Holding Register (THR)	489	2700h
7.22.5.6	Divisor Latch LSB (DLL)	492	2700h
7.22.5.3	Interrupt Enable Register (IER)	489	2701h
7.22.5.4	Interrupt Identification Register (IIR)	490	2701h
7.22.5.7	Divisor Latch MSB (DLM)	492	2701h
7.22.5.5	FIFO Control Register (FCR)	492	2702h
7.22.5.9	Line Control Register (LCR)	494	2703h
7.22.5.10	Modem Control Register (MCR)	495	2704h
7.22.5.11	Line Status Register (LSR)	495	2705h
7.22.5.12	Modem Status Register (MSR)	496	2706h
7.22.5.8	Scratch Pad Register (SCR)	493	2707h
7.22.5.13	EC Serial Port Mode Register (ECSPMR)	497	2708h
7.22	**Serial Port (UART)**	**488**	
7.22.4	Host Interface Registers	488	
7.22.5	EC Interface Registers	489	
7.22.5.1	Receiver Buffer Register (RBR)	489	2800h
7.22.5.2	Transmitter Holding Register (THR)	489	2800h
7.22.5.6	Divisor Latch LSB (DLL)	492	2800h
7.22.5.3	Interrupt Enable Register (IER)	489	2801h
7.22.5.4	Interrupt Identification Register (IIR)	490	2801h
7.22.5.7	Divisor Latch MSB (DLM)	492	2801h
7.22.5.5	FIFO Control Register (FCR)	492	2802h
7.22.5.9	Line Control Register (LCR)	494	2803h
7.22.5.10	Modem Control Register (MCR)	495	2804h
7.22.5.11	Line Status Register (LSR)	495	2805h
7.22.5.12	Modem Status Register (MSR)	496	2806h
7.22.5.8	Scratch Pad Register (SCR)	493	2807h
7.22.5.13	EC Serial Port Mode Register (ECSPMR)	497	2808h
7.13	**8-bit Timer (TMR)**	**410**	
7.13.4	EC Interface Registers	415	
7.13.4.1	TMR Prescaler Register (PRSC)	415	2900h

7.13.4.2	Group Clock Source and Mode Select Register (GCSMS)	416	2901h
7.13.4.3	A0 Cycle Time Register (CTR_A0)	416	2902h
7.13.4.4	A1 Cycle Time Register (CTR_A1)	416	2903h
7.13.4.5	B0 Cycle Time Register (CTR_B0)	416	2904h
7.13.4.6	B1 Cycle Time Register (CTR_B1)	417	2905h
7.13.4.7	A0 Duty Cycle Register (DCR_A0)	417	2906h
7.13.4.8	A1 Duty Cycle Register (DCR_A1)	417	2907h
7.13.4.9	B0 Duty Cycle Register (DCR_B0)	417	2908h
7.13.4.10	B1 Duty Cycle Register (DCR_B1)	417	2909h
7.13.4.11	Channel Clock Group Select Register (CCGSR)	418	290Ah
7.13.4.12	TMR Clock Enable Register (TMRCE)	418	290Bh
7.13.4.13	TMR Interrupt Enable Register (TMRIE)	419	290Ch

7.14	**Consumer Electronics Control (CEC)**	**422**	
7.14.2	EC Interface Registers	423	
7.14.2.1	CEC Data Register (CECDR)	423	2E00h
7.14.2.2	CEC FIFO Status Register (CECFSTS)	423	2E01h
7.14.2.3	CEC Device Logical Address Register (CECDLA)	424	2E02h
7.14.2.4	CEC Control Register (CECCTRL)	424	2E03h
7.14.2.5	CEC Status Register (CECSTS)	424	2E04h
7.14.2.6	CEC Interrupt Enable Register (CECIE)	425	2E05h
7.14.2.7	CEC Operation Status Register (CECOPSTS)	426	2E06h
7.14.2.8	CEC Received Header Register (CECRH)	426	2E07h

7.8	**Platform Environment Control Interface (PECI)**	**347**	
7.8.5	EC Interface Registers	350	
7.8.5.1	Host Status Register (HOSTAR)	351	3000h
7.8.5.2	Host Control Register (HOCTLR)	352	3001h
7.8.5.3	Host Command (Write Data 1) Register (HOCMDR)	353	3002h
7.8.5.4	Host Target Address Register (HOTRADDR)	353	3003h
7.8.5.5	Host Write Length Register (HOWRLR)	353	3004h
7.8.5.6	Host Read Length Register (HORDLR)	353	3005h
7.8.5.7	Host Write Data (2-16) Register (HOWRDR)	353	3006h
7.8.5.8	Host Read Data (1-16) Register (HORDDR)	353	3007h
7.8.5.9	Host Control 2 Register (HOCTL2R)	354	3008h
7.8.5.10	Pad Control Register (PADCTLR)	354	300Eh
7.8.5.11	Received Write FCS Value (RWFCSV)	354	3009h
7.8.5.12	Received Read FCS Value (RRFCSV)	354	300Ah
7.8.5.13	Write FCS Value (WFCSV)	355	300Bh
7.8.5.14	Read FCS Value (RFCSV)	355	300Ch
7.8.5.15	Assured Write FCS Value (AWFCSV)	355	300Dh

7.23	**Debug UART**	**500**	
7.23.4	EC Interface Registers	500	
7.23.4.1	Serial Port Control Register (SCON)	500	3701h
7.23.4.2	Timer 1 High Byte Register (TH1R)	501	3702h
7.23.4.3	Timer 1 Low Byte Register (TL1R)	501	3703h
7.23.4.4	Serial Port Buffer Register (SBUFR)	501	3704h
7.23.4.5	Serial Port Control Register (SCTRL)	501	3705h
7.23.4.6	Timer Mode Register (TMOD)	501	3706h
7.23.4.7	Timer Control Register (TCON)	501	3707h
7.23.4.8	Clock Control Register (CKCON)	502	3708h

9. DC Characteristics

Operating Conditions

VSTBY ……..... 3.3V±0.15V
VFSPI (3.3V) …….. ..... 3.3V±0.15V
VFSPI (1.8V) …….. ..... 1.8V±0.09V
VCC (3.3V)……..... 3.3V±0.15V
VCC (1.8V)……..... 1.8V±0.09V
AVCC…….. ..... 3.3V±0.15V
Operating Temperature (Ta) .....-40°C to +85°C

Absolute Maximum Ratings

Applied Voltage of VFSPI(1.8V), VCC(1.8V) …….. ..... -0.3V to +2.1V
Applied Voltage of VSTBY, VFSPI(3.3V), VCC(3.3V), AVCC …….. ..... -0.3V to +3.6V
Input Voltage of 1.8V Interface.... -0.3V to VSUP+0.3V
Input Voltage of 3.3V Interface.... -0.3V to VSUP+0.3V
Input Voltage of 5.0V Interface..... -0.3V to +5.8V
Input Voltage of 1.8V/3.3V ..... Optional Interface ..... -0.3V to +3.6V
Storage Temperature .....-40°C to +125°C

Note: VSUP is VCC, VSTBY, VFSPI or AVCC.

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
V_{IL}	Input low voltage	—	—	0.8V	—
V_{IH}	Input high voltage	2.0V	—	—	—
V_{IH}	Input high voltage (5V tolerant pad)	2.0V	—	—	—
V_{OL}	Output low voltage	—	—	0.4V	I_{OL}= -2 - -16mA
V_{OH}	Output high voltage	2.4V	—	—	I_{OH}= 2 - 16mA
V_{T-}	Schmitt trigger negative going threshold voltage	0.8V	—	—	—
V_{T+}	Schmitt trigger positive going threshold voltage	—	—	2.0V	—
I_{IL}	Input leakage current	-10μA	±1μA	10μA	No pull-up or pull-down
I_{OZ}	Tri-state leakage current	-10μA	±1μA	10μA	No pull-up or pull-down
R_{pu}	Input pull-up resistance	40KΩ	75KΩ	190KΩ	V_I= 0V
R_{pd}	Input pull-down resistance	40KΩ	75KΩ	190KΩ	V_I= VSUP
Cin	Input capacitance	—	2.8pF	—	—
C_L	Load capacitance	—	—	10pF	Only for FSPI signals
Cout	Output capacitance	2.7pF	—	4.9pF	—
Cbld	Bi-directional buffer	2.7pF	—	4.9pF	—

Note: VSUP is VCC (3.3V), VSTBY, VFSPI (3.3V) or AVCC.

1.8V CMOS Interface					
V_{IL}	Input low voltage	—	—	0.25*VSUP	—
V_{IH}	Input high voltage	0.75*VSUP	—	—	—
V_{IH}	Input high voltage (3.3V tolerant pad)	0.75*VSUP	—	—	—
V_{OL}	Output low voltage	—	—	0.4V	I_{OL}= -2 - -16mA
V_{OH}	Output high voltage	0.75*VSUP	—	—	I_{OH}= 2 - 16mA
V_{T-}	Schmitt trigger negative going threshold voltage	0.25*VSUP	—	—	—
V_{T+}	Schmitt trigger positive going threshold voltage	—	—	0.75*VSUP	—
I_{IL}	Input leakage current	-10μA	±1μA	10μA	No pull-up or pull-down
I_{OZ}	Tri-state leakage current	-10μA	±1μA	10μA	No pull-up or pull-down
R_{pu}	Input pull-up resistance	80KΩ	200KΩ	510KΩ	V_I= 0V
R_{pd}	Input pull-down resistance	80KΩ	200KΩ	510KΩ	V_I= VSUP
Cin	Input capacitance	—	2.8pF	—	—
C_L	Load capacitance	—	—	10pF	Only for FSPI signals
Cout	Output capacitance	2.7pF	—	4.9pF	—
Cbld	Bi-directional buffer	2.7pF	—	4.9pF	—

Note: VSUP is VCC (1.8V), VFSPI (1.8V).

Table 9-1. Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
I_{SLEEP}	VSTBY supply current if Crystal-Free	—	50μA	—	Internal pull is disabled VIL = GND VIH = VSTBY No load

10. AC Characteristics

Figure 10-1. VSTBY Power-on Reset Timing

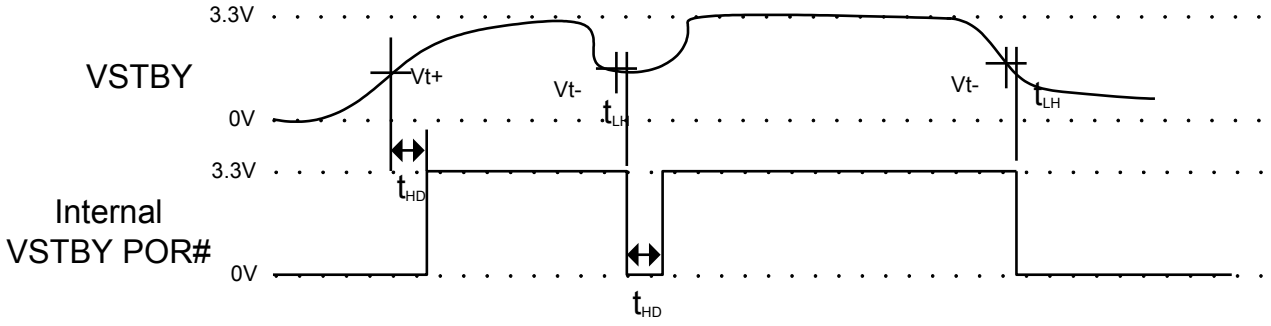


Table 10-1. VSTBY Power-on Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vt+	Level detection positive going threshold voltage	—	2.6	—	V
Vt-	Level detection negative going threshold voltage	—	Vt+ - 0.2	—	V
t_{HD}	Internal VSTBY POR going high delay	—	500	—	μs
t_{LH}	Minimum hold time after VSTBY < Vt- and before internal VSTBY POR going low	—	10	—	μs

Figure 10-2. Reset Timing

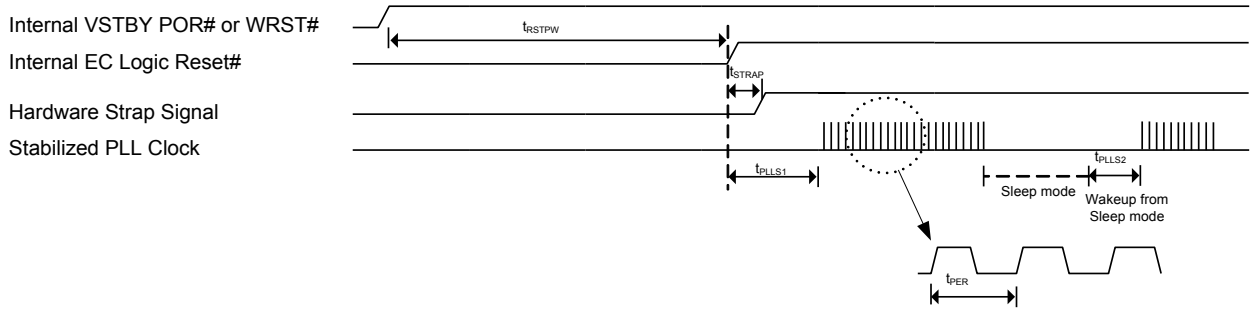


Table 10-2. Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RSTPW}	Internal EC logic reset after VSTBY POR or WRST#	—	1650	—	Tick (by 32.768 kHz)
t_{STRAP}	Strap sampling time	0	—	—	ns
t_{PLLS1}	PLL stabilization time hardware	—	5	—	ms
t_{PLLS2}	PLL stabilization time after waking up from Sleep mode	—	5	—	ms
t_{PER}	PLL clock period	—	$1/_{FreqPLL}$	—	ns
FreqPLL	PLL clock frequency if PLLFREQ = 0001b	—	18.4	—	MHz
	PLL clock frequency if PLLFREQ = 0011b	—	32.3	—	MHz
	PLL clock frequency if PLLFREQ = 0111b	—	64.5	—	MHz
FreqEC	EC clock frequency	—	9.2	—	MHz
E_{cf1}	“Crystal-Free”: Center frequency of FreqPLL/FreqEC Temperature: 0 ~ 70℃	—	—	±1.7	%
E_{cf2}	“Crystal-Free”: Center frequency of FreqPLL/FreqEC Temperature: -25 ~ 85℃	—	—	±2.3	%
E_{cf3}	“Crystal-Free”: Center frequency of FreqPLL/FreqEC Temperature: -40 ~ 85℃	—	—	±3.1	%

Figure 10-3. Warm Reset Timing

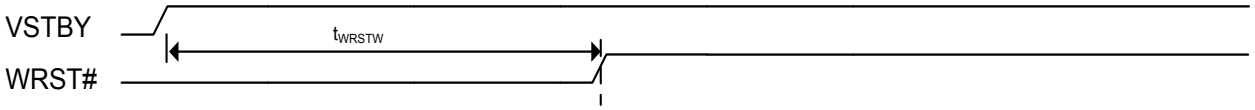


Table 10-3. Warm Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	μs

Figure 10-4. Wake-up from Doze Mode Timing

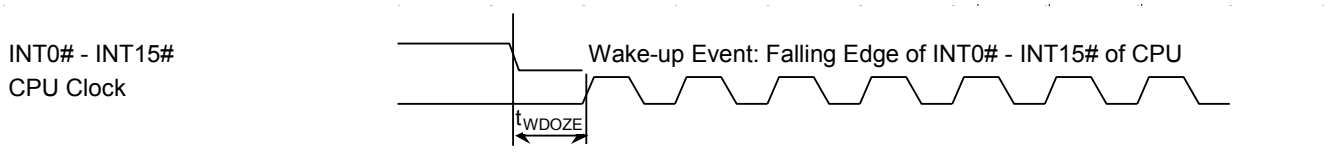


Table 10-4. Wake-up from Doze Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDOZE}	Doze wake-up time from falling edge of INT0# - INT15# to rising edge of first CPU clock	—	—	2 / (EC Clock Freq)	—

Figure 10-5. Wake-up from Sleep Mode Timing

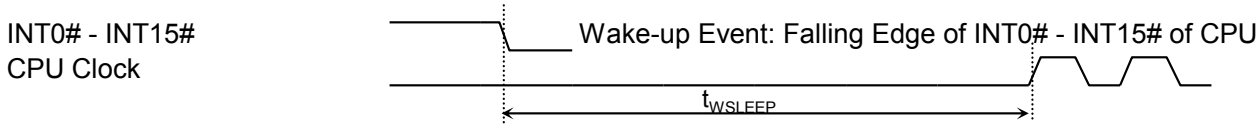


Table 10-5. Wake-up from Sleep Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WSLEEP}	Sleep wake-up time from falling edge of INT0# - INT15# to rising edge of first CPU clock	—	5	—	ms

Figure 10-6. Asynchronous External Wakeup/Interrupt Source Edge Detected Timing

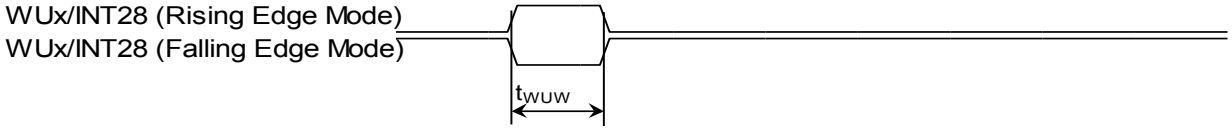


Table 10-6. Asynchronous External Wake-up/Interrupt Source Edge Detected AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{wuw}	Wake-up source pulse width	—	1	—	ns

Figure 10-7. LPC and SERIRQ Timing

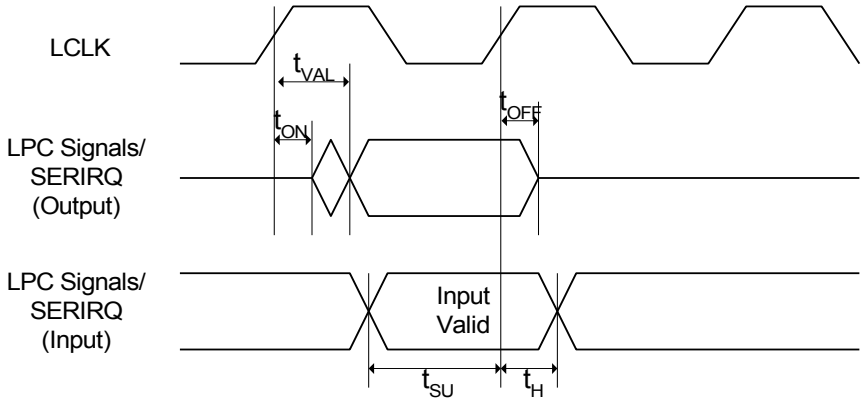


Table 10-7. LPC and SERIRQ AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ON}	Float to active delay	3	—	—	ns
t_{VAL}	Output valid delay	—	—	12	ns
t_{OFF}	Active to float delay	—	—	20	ns
t_{SU}	Input setup time	7	—	—	ns
t_H	Input hold time	0	—	—	ns

Figure 10-8. SWUC Wake-up Timing

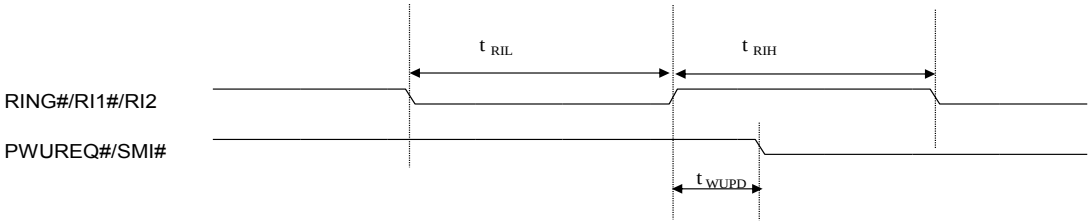


Table 10-8. SWUC Wake-up AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RIL}	RING#, RI1# , RI2# low time	10	—	—	ns
t_{RIh}	RING#, RI1# , RI2# high time	10	—	—	ns
t_{WUPD}	Wake-up propagation delay time	—	20	—	ns

Figure 10-9. Serial Flash (FSPI) Cycle Timing

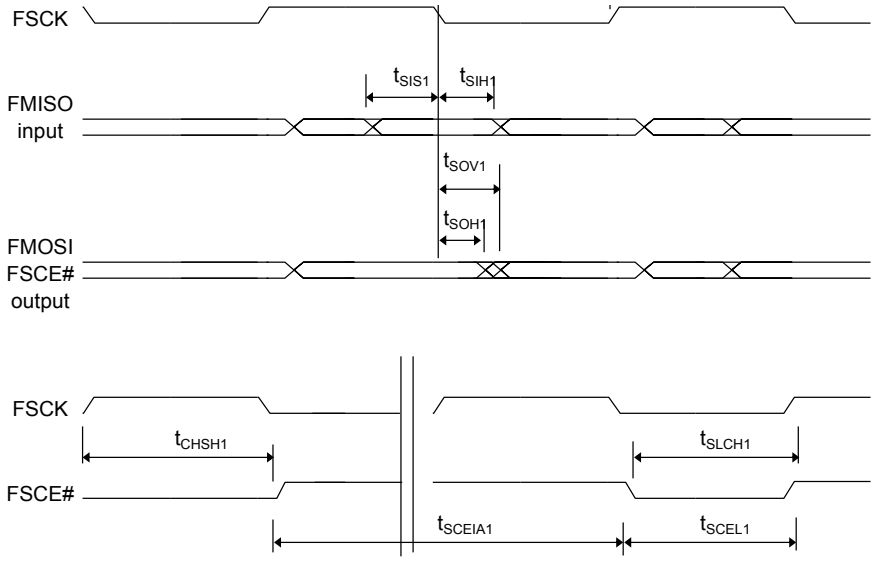


Table 10-9. Serial Flash (FSPI) Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCK}	FSCK period	—	1/FreqPLL	—	ns
t_{CLH} t_{CLL}	FSCK high time NOTE1 FSCK low time NOTE1	6 Note2	—	—	ns
t_{SIS1}	Input setup time	3	—	—	ns
t_{SIH1}	Input hold time	0	—	—	ns
t_{SOV1}	Clock low to output valid	—	—	5	ns
t_{SOH1}	Output hold time	0	—	—	ns
t_{SCEL1}	FSCE# Active time	(0.5/ FreqPLL)-2.5	—	—	ns
t_{SCEIA1}	FSCE# high time	(SCEMINHW + 1) * t_{SCK}	—	—	ns
t_{SLCH1}	FSCE# Active Setup Time relative to FSCK rising edge	(0.5/ FreqPLL)-2.5	—	—	ns
t_{CHSH1}	FSCE# Active Hold Time relative to FSCK rising	(0.5/ FreqPLL)-2.5	—	—	ns

Note 1: Measurement point for low time and high time is taken at VSTBY*0.5.
Note 2: Characterized only.

Figure 10-10. PWM Output Timing

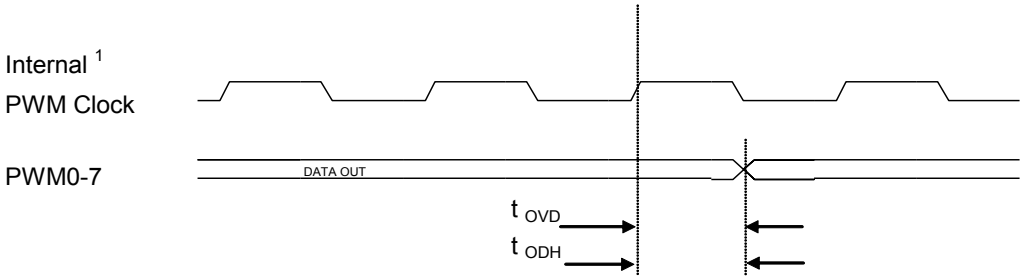


Table 10-10. PWM Output AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{OVD}	PWM output valid delay time	—	—	0.5	T NOTE1
t_{ODH}	PWM output hold time	0	—	—	ns

Note 1: T is one time unit and its length is equal to the EC clock period X C0CPRS +1 (ns) for CH0~3, or X C4CPRS +1 (ns) for CH4~7.

Figure 10-11. PMC SMI#/SCI# Timing

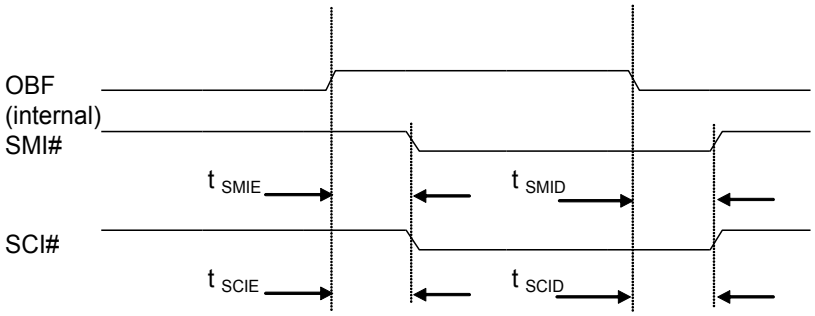


Table 10-11. PMC SMI#/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SMIE}	OBF asserted to SMI# asserted time	—	10	—	ns
t_{SMID}	OBF de-asserted to SMI# de-asserted time	—	5	—	ns
t_{SCIE}	OBF asserted to SCI# asserted time	—	10	—	ns
t_{SCID}	OBF de-asserted to SCI# de-asserted time	—	5	—	ns

Figure 10-12. PMC IBF/SCI# Timing

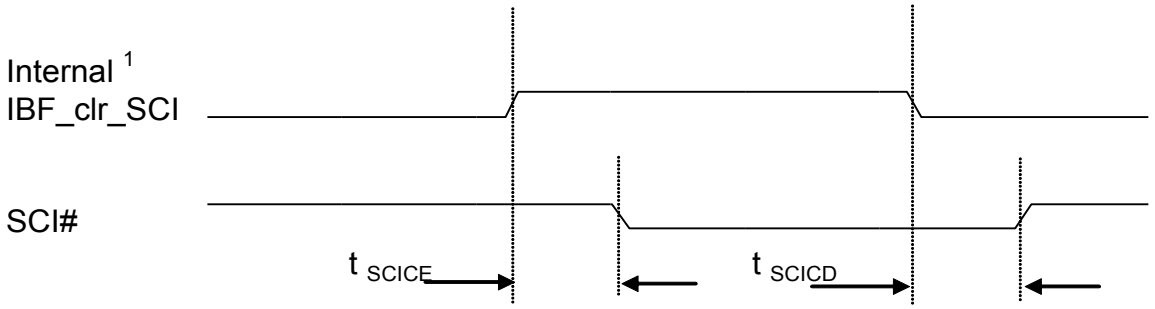


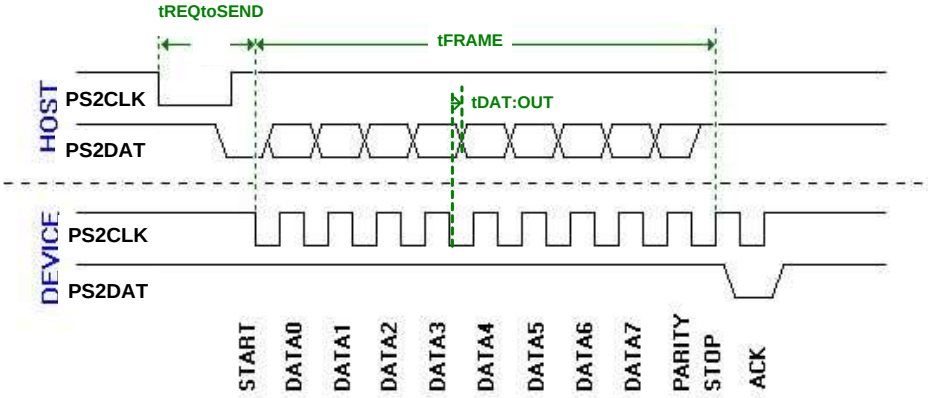
Table 10-12. PMC IBF/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCICE}	IBF_clr_SCI# asserted to SCI# asserted time	—	70	—	ns
t_{SCICD}	IBF_clr_SCI# de-asserted to SCI# de-asserted time	—	40	—	ns

Note 1: IBF_clr_SCI# means the invert signal of IBF, IBF_clr_SCI# set to one when EC read PMDI or PMDISCI.

Figure 10-13. PS/2 Receive/Transmit Timing

Receive:



Transmit:

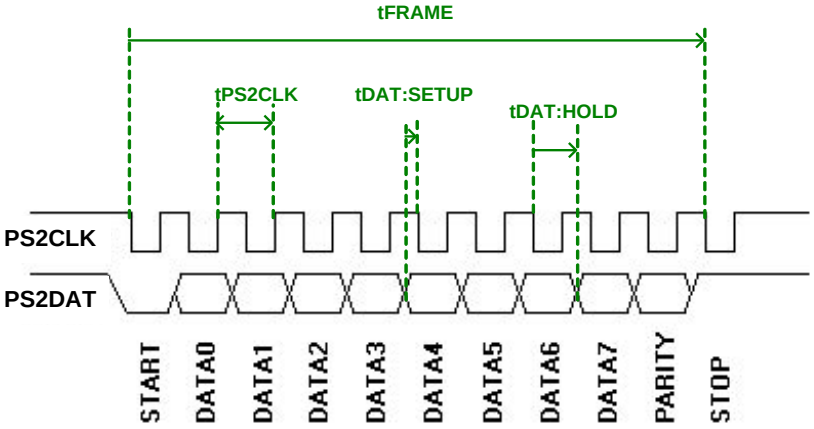
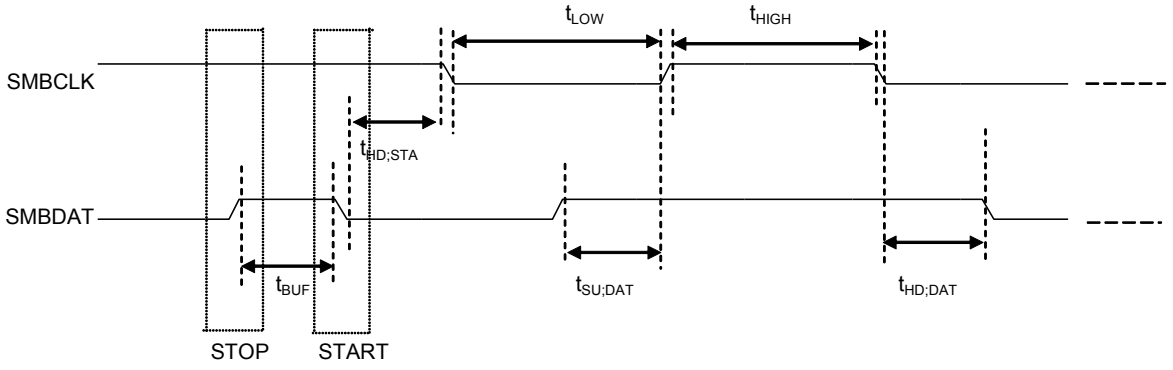


Table 10-13. PS/2 Receive/Transmit AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{REQtoSEND}$	PS/2 host Request to send and wait for PS/2 device responding by driving PS2CLK low	—	—	15	ms
t_{FRAME}	Duration of frame	—	—	2	Ms
$t_{DAT:OUT}$	Date output by PS/2 host following the falling edge of PS2CLK	400[Note1] ns 700[Note2] ns	—	1[Note1] µs 2[Note2] µs	—
$t_{DAT:SETUP}$	Date setup time to falling edge of PS2CLK	1	—	—	µs
$t_{DAT:HOLD}$	Date hold time from falling edge of PS2CLK	1	—	—	µs
t_{PS2CLK}	PS/2 clock line period	60	—	100	µs

Note 1: DCEN@PSCTL1-3 = 0b
Note 2: DCEN@PSCTL1-3 = 1b

Figure 10-14. SMBus Timing



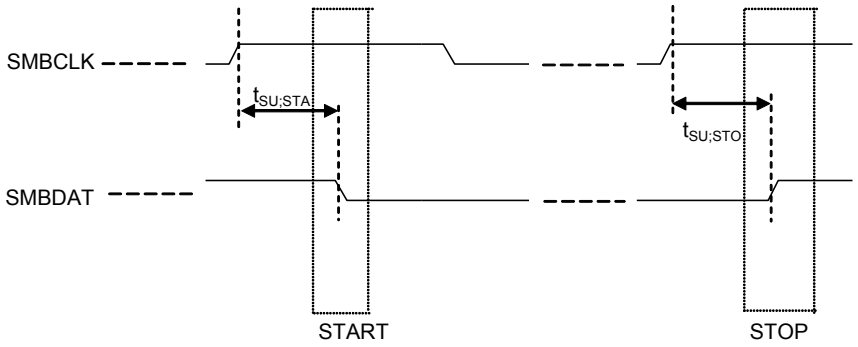


Table 10-14. SMBus AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUF}	Bus free time between Stop and Start condition	4.7	—	—	μs
$t_{HD;STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	4.0	—	—	μs
t_{LOW}	Clock low period	4.7	—	—	μs
t_{HIGH}	Clock high period	4.0	—	50	μs
$t_{SU;DAT}$	Data setup time	250	—	—	ns
$t_{HD;DAT}$	Data hold time	300	—	—	ns
$t_{SU;STA}$	Repeated Start condition setup time	4.7	—	—	μs
$t_{SU;STO}$	Stop condition setup time	4.0	—	—	μs

Figure 10-15. Consumer IR (CIR) Timing

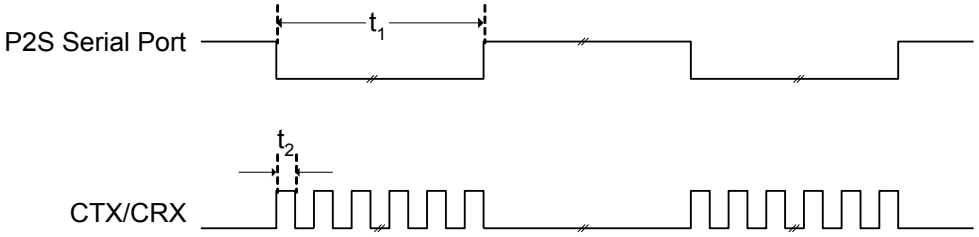


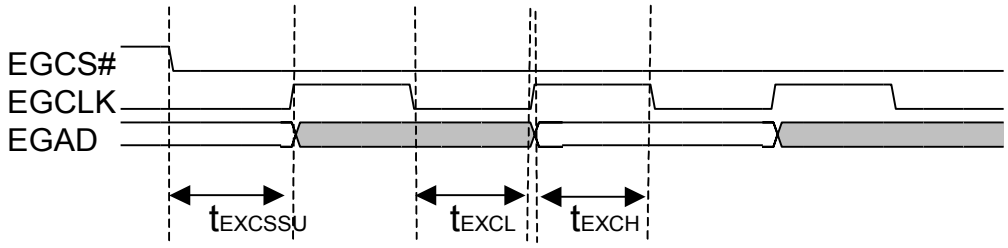
Table 10-15. Consumer IR (CIR) AC Table

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single bit time in P2S of CIR	Transmitter	t_{BTN} – Tclk Note1	t_{BTN} + Tclk Note1	ns
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	ns
t_2	Modulation signal pulse width in CTX0/CRX0 and CTX1/CRX1	Transmitter	Tpwd – Tclk Note2	Tpwd +Tclk Note2	ns
		Receiver	Tpwd –2%	Tpwd +2%	ns

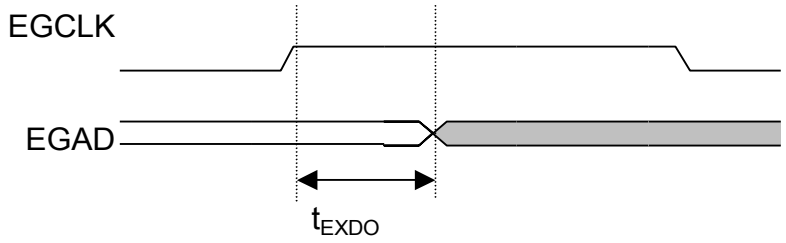
Note 1: t_{BTN} is the nominal bit time in Serial Port of P2S block of CIR. It is determined by the setting on the Baud Rate Divisor registers (C0BDHR/C0BDLR). Tclk equals to 1/ FreqEC.

Note 2: Tpwd is normal modulated pulse width on CTX0/CRX0 and CTX1/CRX1pin. It is determined by C0TCR registers.

Figure 10-16. External GPIO Controller Data Timing



Transmit:



Receive:

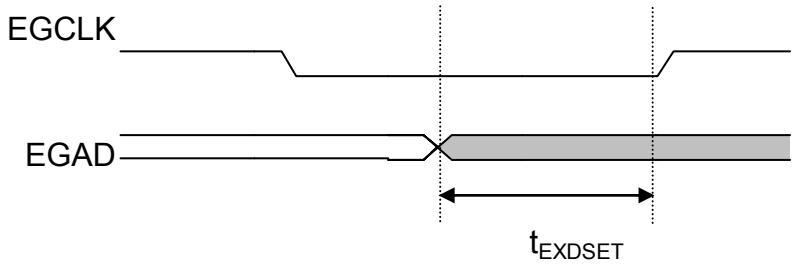


Table 10-16. External GPIO Controller Interface AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{EXCSSU}	EGCS# line input set up time	30	—	—	ns
t_{EXCL+} t_{EXCH}	EGCLK line period time	—	1/FreqEC	—	ns
t_{EXDO}	EGAD line output data time	—	—	50	ns
t_{EXDSET}	EGAD line input set up time	1	—	—	ns

Figure 10-17. Serial Peripheral Interface (SSPI) Timing

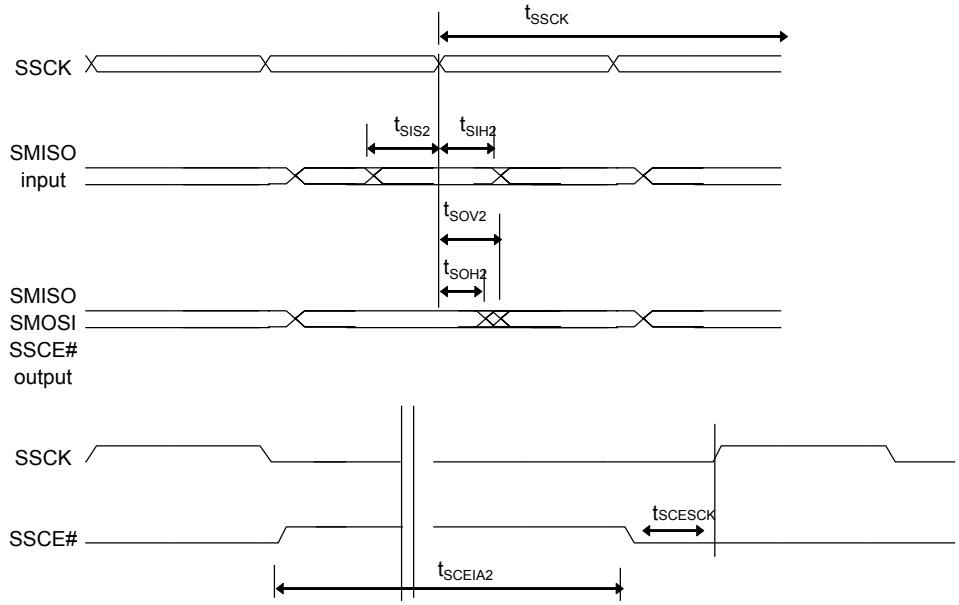


Table 10-17. Serial Peripheral Interface (SSPI) AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SSCK}	SSCK period	2/ FreqEC	—	16/ FreqEC	ns
t_{SIS2}	Input setup time	5	—	—	ns
t_{SIH2}	Input hold time	5	—	—	ns
t_{SOV2}	Clock edge to output valid	—	—	5	ns
t_{SOH2}	Output hold time	0	—	—	ns
t_{SCEIA2}	SSCE# inactive time	1/ FreqEC	—	—	ns
$t_{SCESSCK}$	From SSCE# active edge to first SSCK active edge	—	2/ FreqEC	—	ns

Figure 10-18. Serial Port (UART) Timing

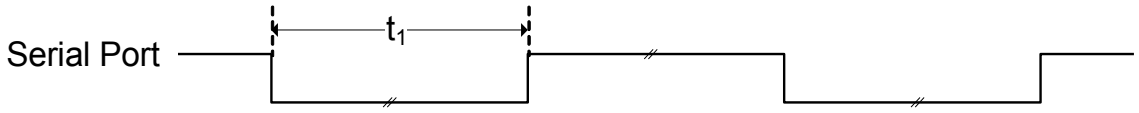


Table 10-18. Serial Port (UART) AC Table

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single bit time in UART	Transmitter	t_{BTN} – Tclk Note1	t_{BTN} + Tclk Note1	ns
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	ns

Note 1: tBTN is the nominal bit time in Serial Port (UART). It is determined by setting the Baud Rate Divisor registers. Tclk equals to 1/ FreqEC.Tclk equals to 1/ FreqEC.

11. Analog Device Characteristics

Table 11-1. ADC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution	—	—	10	—	Bit
Integral Non-linearity Error (INL)	—	—	—	±6	LSB
Differential Non-linearity Error (DNL)	—	—	—	±6	LSB
ADC Input Voltage Range	—	0	—	AVCC/1.1 or AVCC	V
ADC Input Leakage Current	ADC0-x: 0 ≦ Vin ≦ AVCC	—	±1	—	μA
ADC Input Resistance	—	4	—	—	MΩ
ADC Input Capacitance	—	—	—	8	pF
ADC Clock Frequency	—	—	0.5	—	MHz
Voltage Conversion Time	—	—	—	100	us

Note 1: The voltage reference is AVCC/1.1 or AVCC.
Note 2: All calculated above are only within 0.25V ~ (AVCC - 0.15V) if the corresponding bit in ADCIVMFSCS1 or ADCIVMFSCS2 is set to 1b.
Note 3: All calculated above are only within 0.25V ~ 2.85V if the corresponding bit in ADCIVMFSCS1 or ADCIVMFSCS2 is set to 0b.
Note 4: After calibration is performed, INL is the difference between the actual transition curve and the end-point line.

Table 11-2. DAC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution	—	—	8	—	Bit
Integral Non-linearity Error (INL)	AVCC = 3.3V	—	—	±1	LSB
Differential Non-linearity Error (DNL)	AVCC = 3.3V	—	—	±1	LSB
DAC Output Voltage Range	—	0	—	AVCC	V
DAC Settling Time	C_{load} = 50pF	—	—	1	μs
DAC Output Resistance	0 ≦ Vout ≦ AVCC	3	—	800	Ω
DAC Output Capacitance	—	—	6.5	—	pF

Note: C_{load} = (DAC Output Capacitance) + (External Load Capacitance)

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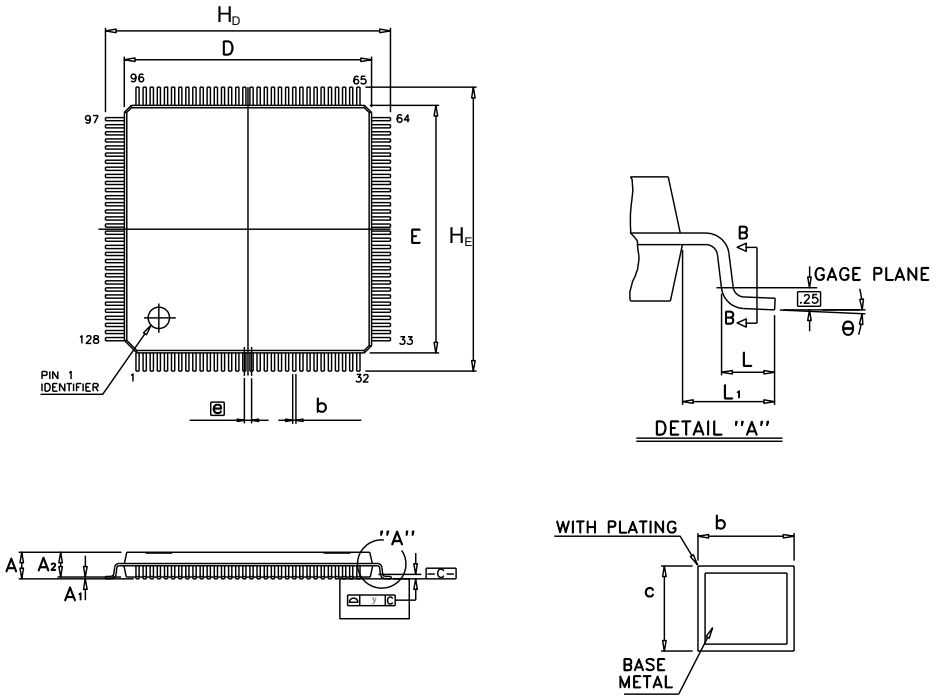
12. Package Information

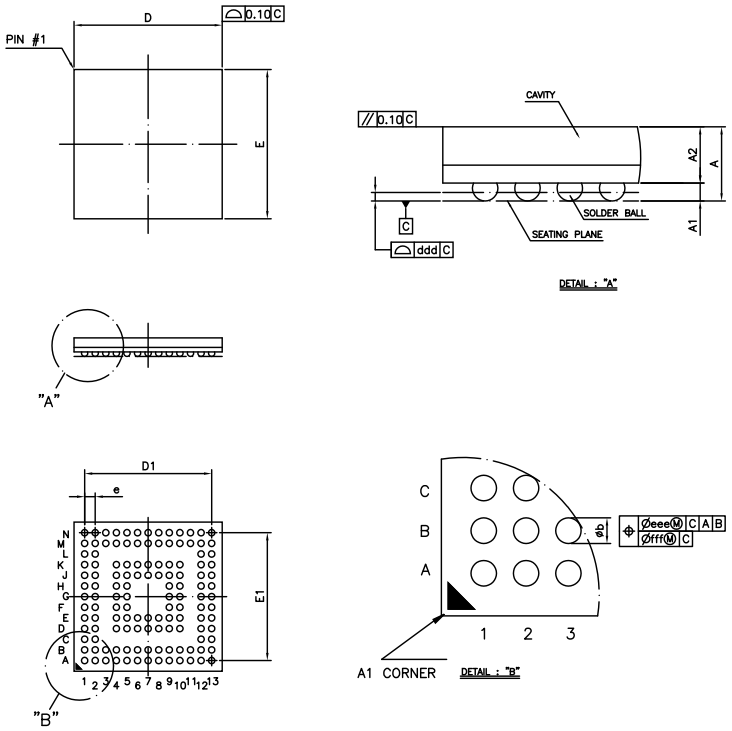
LQFP 128(14*14) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	-	0.05	-	-
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H_D	0.624	0.630	0.636	15.85	16.00	16.15
H_E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
3. Total in excess of the b dimension at maximum material condition.
4. Dambar cannot be located on the lower radius of the foot.
5. Controlling dimensions: Millimeter
6. Reference document: JEDEC MS-026

VFBGA 128(7*7) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.038	---	---	0.97
A1	0.006	0.008	0.010	0.16	0.21	0.26
A2	0.024	0.026	0.028	0.61	0.66	0.71
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
D1	0.236 BSC			6 BSC		
E1	0.236 BSC			6 BSC		
e	0.02 BSC			0.5 BSC		
b	0.010	0.012	0.014	0.25	0.30	0.35
ddd	0.003			0.08		
eee	0.006			0.15		
fff	0.003			0.08		
MD/ME	13/13			13/13		

Notes:
1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-225

DI-VFBGA128(7*7)v3

13. Ordering Information

Part No.	Package	e-Flash Size
IT5121E-I-128/CX	LQFP 128	128KB
IT5121VG-I-128/CX	VFBGA 128	128KB
IT5121E-I-192/CX	LQFP 128	192KB
IT5121VG-I-192/CX	VFBGA 128	192KB
IT5121E-I-256/CX	LQFP 128	256KB
IT5121VG-I-256/CX	VFBGA 128	256KB

All green components provided are in compliance with RoHS, and Halogen-Free.

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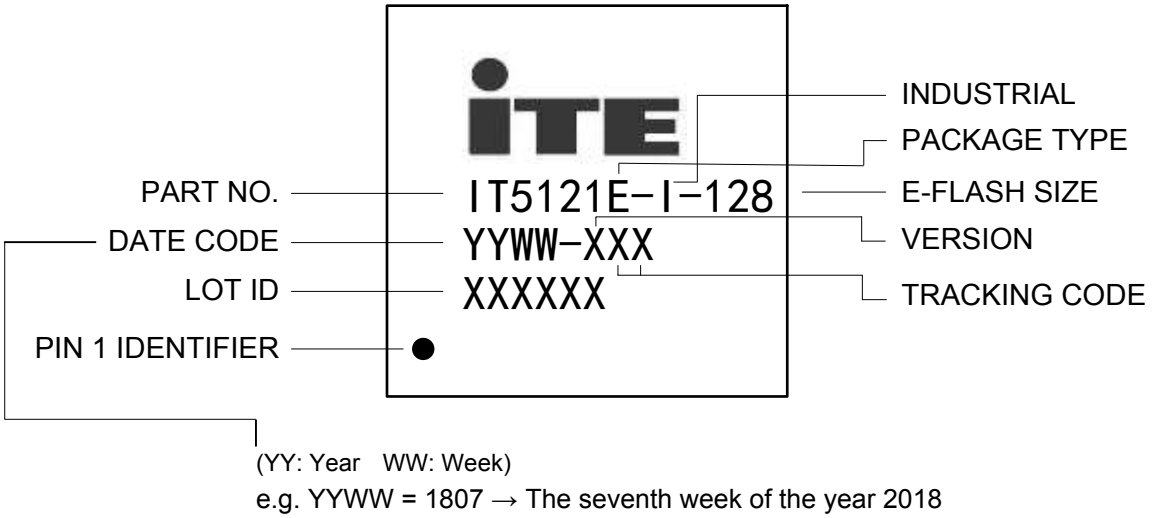
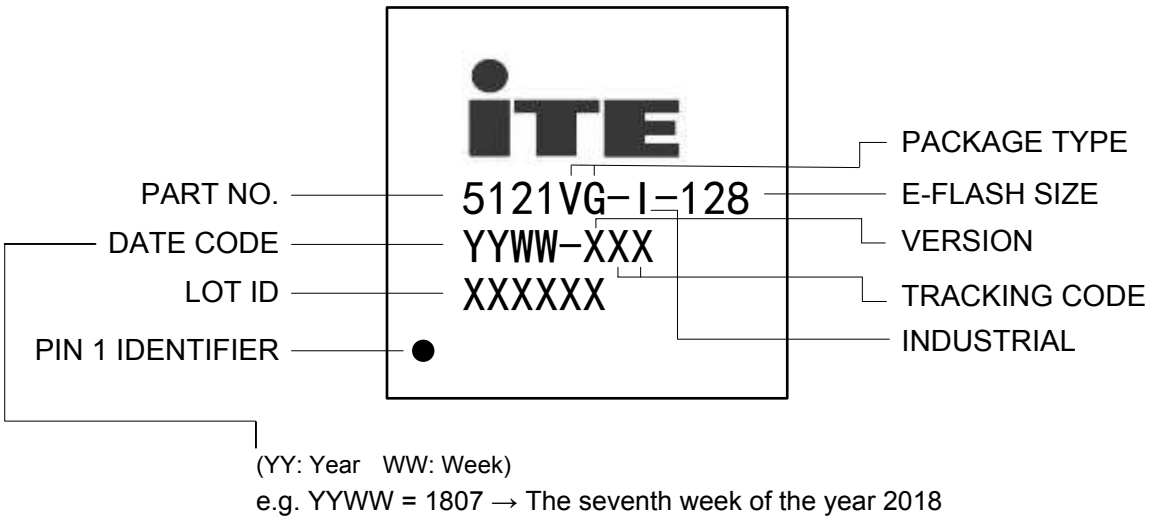
14. Top Marking Information

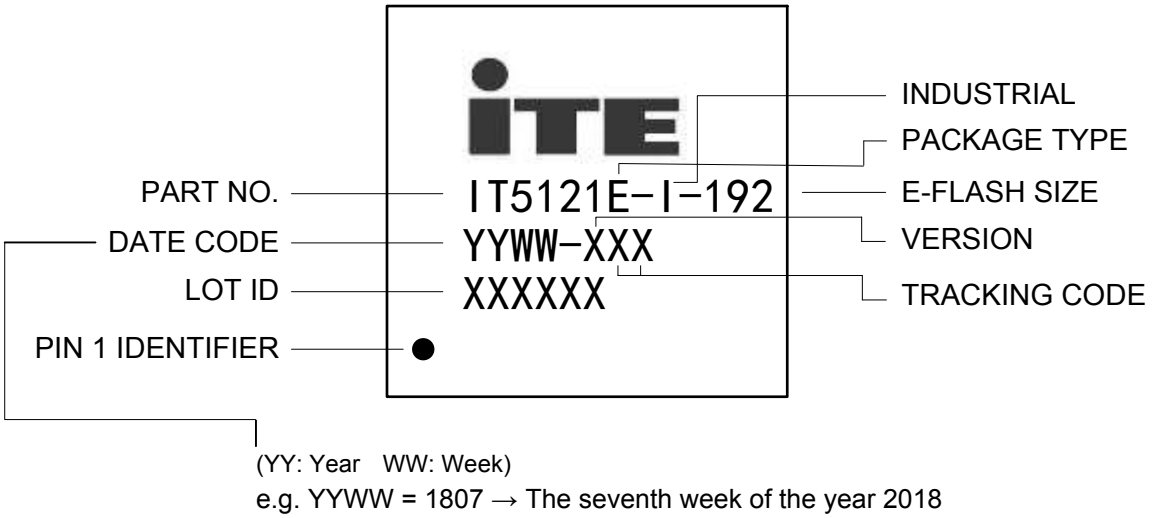
IT5121E-I-128



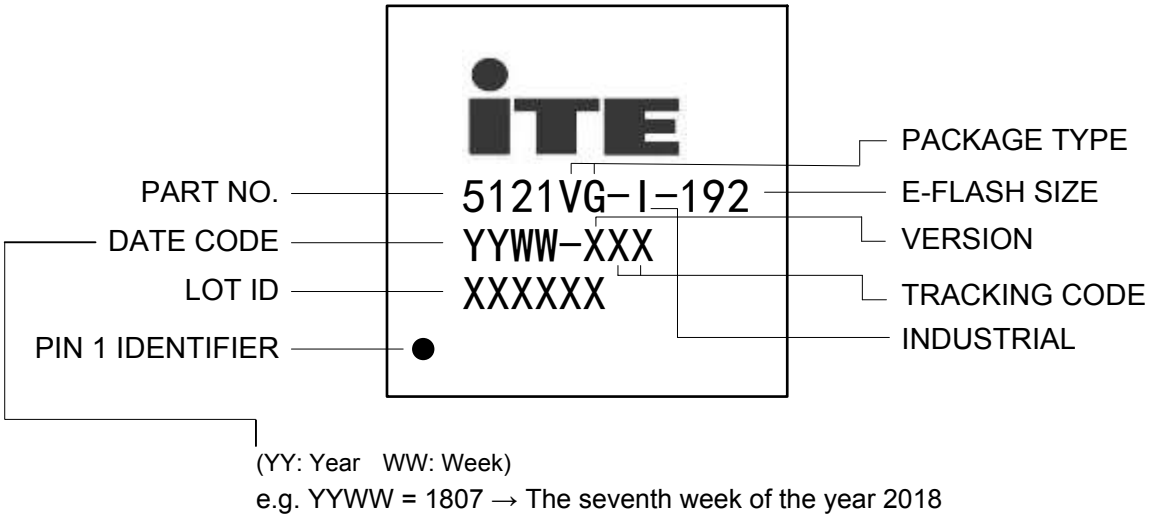
IT5121VG-I-128



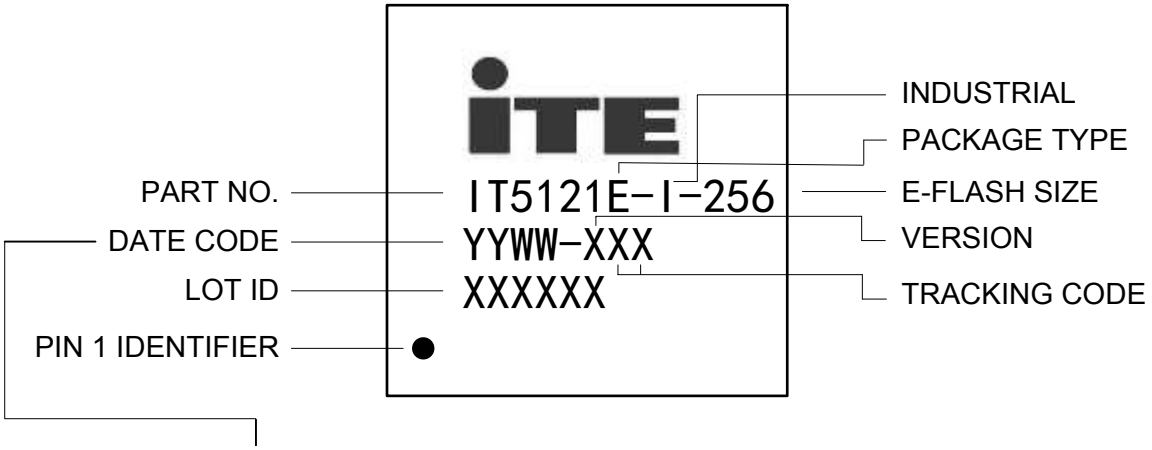
IT5121E-I-192



IT5121VG-I-192

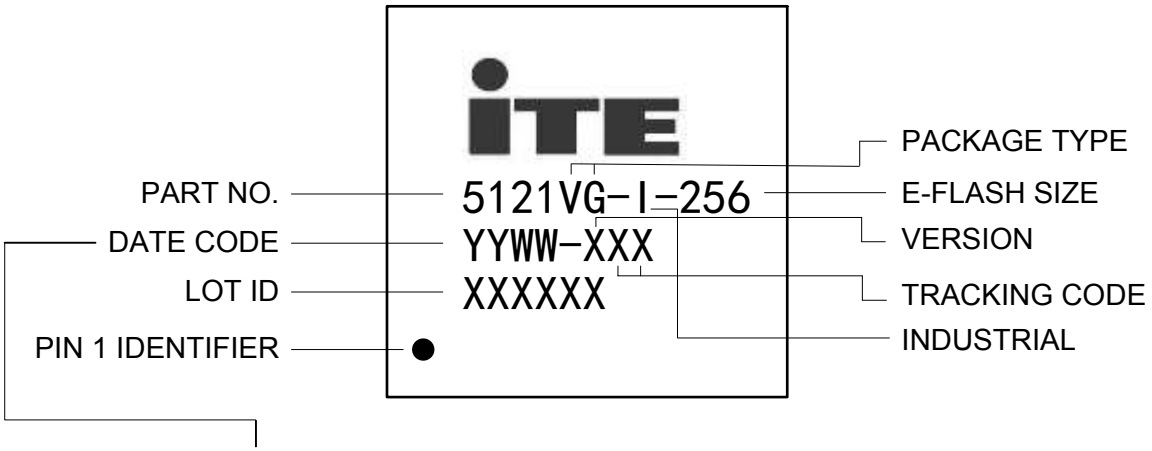


IT5121E-I-256



(YY: Year WW: Week)
e.g. YYWW = 1807 → The seventh week of the year 2018

IT5121VG-I-256



(YY: Year WW: Week)
e.g. YYWW = 1807 → The seventh week of the year 2018

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.