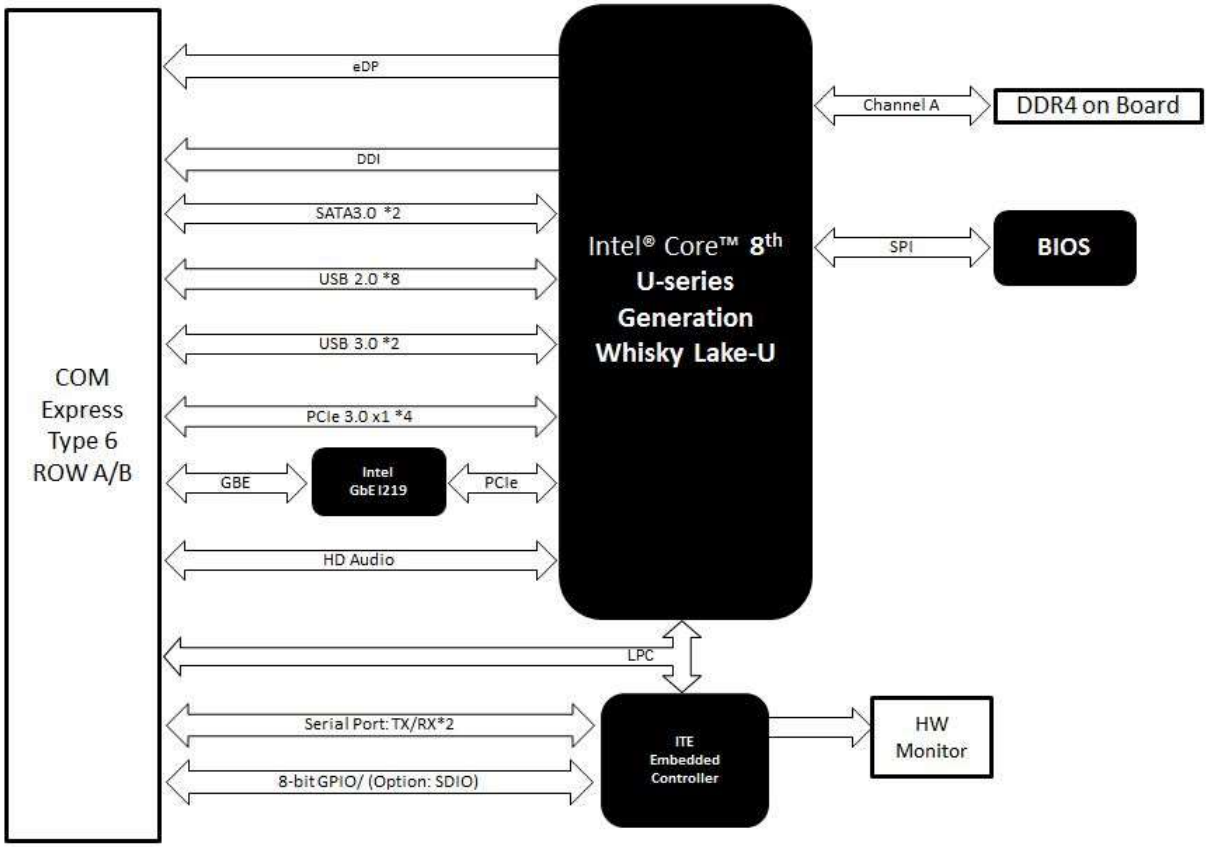
Project Name: NANOCOM-WHU
Project Number:
Version: A0.3_0_0

System block diagram



WHU

AAEON Technology INC.

Title: Cover Sheet

Size: Custom | Document Number: NANOCOM-WHU | Rev: A0.3_0_0

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SoC GPIO Pins :

Name	Power Well	Default	GPIO Function	Location
GPP_G0/SD_CMD	+V3P3A		GPI0	
GPP_G1/SD_DATA0	+V3P3A		GPI1	
GPP_G2/SD_DATA1	+V3P3A		GPI2	
GPP_G3/SD_DATA2	+V3P3A		GPI3	
GPP_G4/SD_DATA3	+V3P3A		GPO0	
GPP_G5/SD_CD#	+V3P3A		GPO1	
GPP_G6/SD_CLK	+V3P3A		GPO2	
GPP_G7/SD_WP	+V3P3A		GPO3	
GPP_C22	+V3P3A		SMI#	
GPP_C23	+V3P3A		SCI#	

EC GPIO Pins :

SMBus/I2C Addresses :

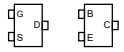
Device	address
I219	0XC8

Board ID

ID0	ID1	Description
0	0	Micron DDR4 8G
0	1	Samsung DDR4 4G
1	0	N/A
1	1	N/A

PCB Footprints

MOSFET BJT



BOM	Description
9697NAWU06-D	Celeron 4305UE.DDR4 4GB(Samsung).eMMC 32G
9697NAWU07-D	I3-8145UE.DDR4 8GB(Micron).eMMC 64G
9697NAWU08-D	I5-8365UE.DDR4 8GB.(Micron).eMMC 64G
9697NAWU09-D	I7-8665UE.DDR4 8GB(Micron).eMMC 64G

PCB STACK :

Board: FR4
Impedence: 50ohm +/-10%
Thickness: 2.0mm +-10%

- Layer 1 : Component (Top)
- Layer 2 : GND (GND1)
- Layer 3 : Signal (IN1)
- Layer 4 : GND (GND2)
- Layer 5 : Signal (IN2)
- Layer 6 : POWER (VCC)
- Layer 7 : POWER (VCC)
- Layer 8 : Signal (IN3)
- Layer 9 : GND (GND3)
- Layer 10 : Signal (IN4)
- Layer 11 : GND (GND4)
- Layer 12 : Signal (IN5)
- Layer 13 : GND (GND5)
- Layer 14 : Solder (Bottom)

WHU

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AAEON Technology INC.

Title: System Setting

Size: Custom | Document Number: NANOCOM-WHU | Rev: A0.3_0_0

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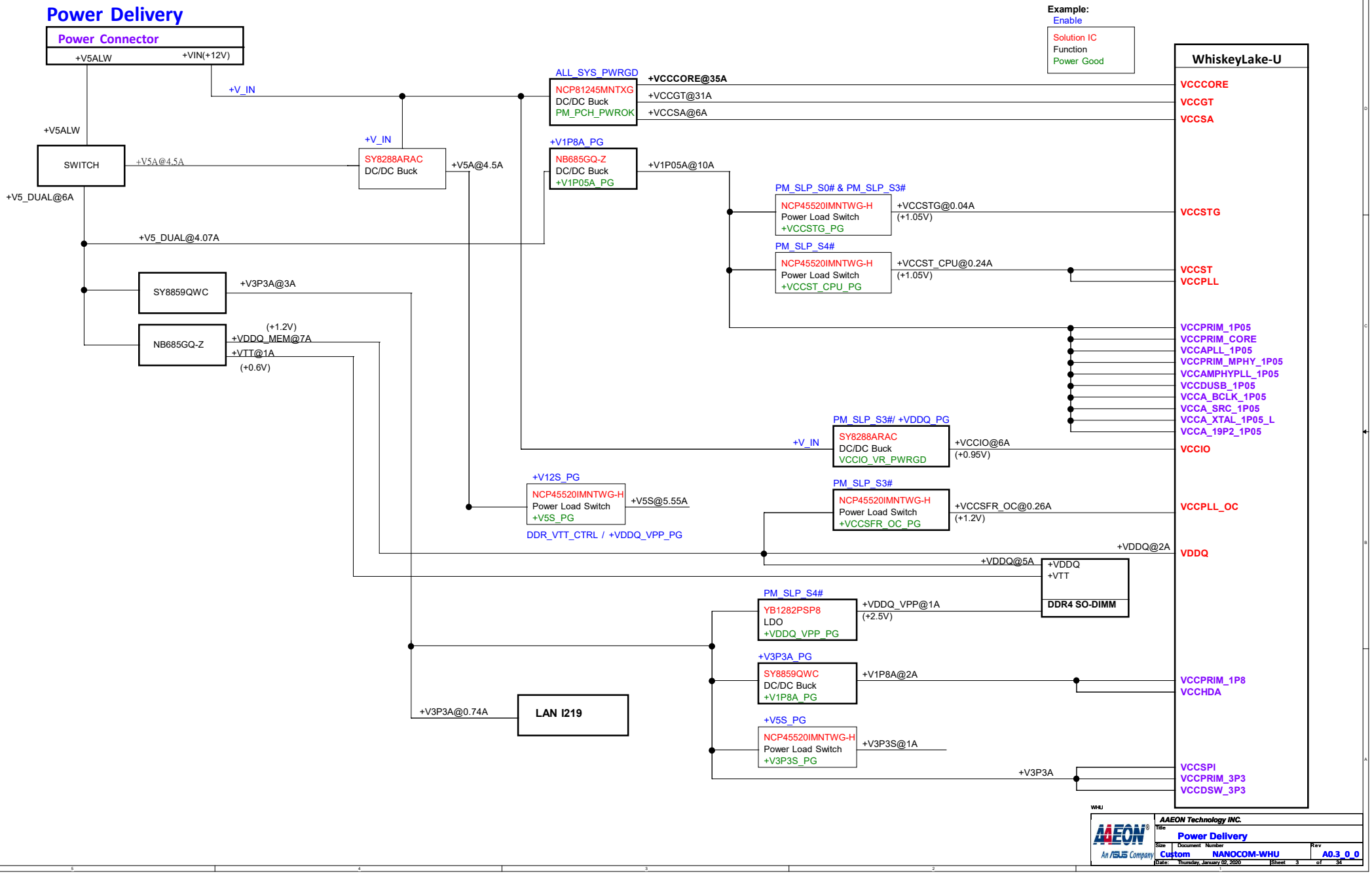
Power Delivery



WHU

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Title: Power Delivery

Size: Custom | Document Number: NANOCOM-WHU | Rev: A0.3_0_0

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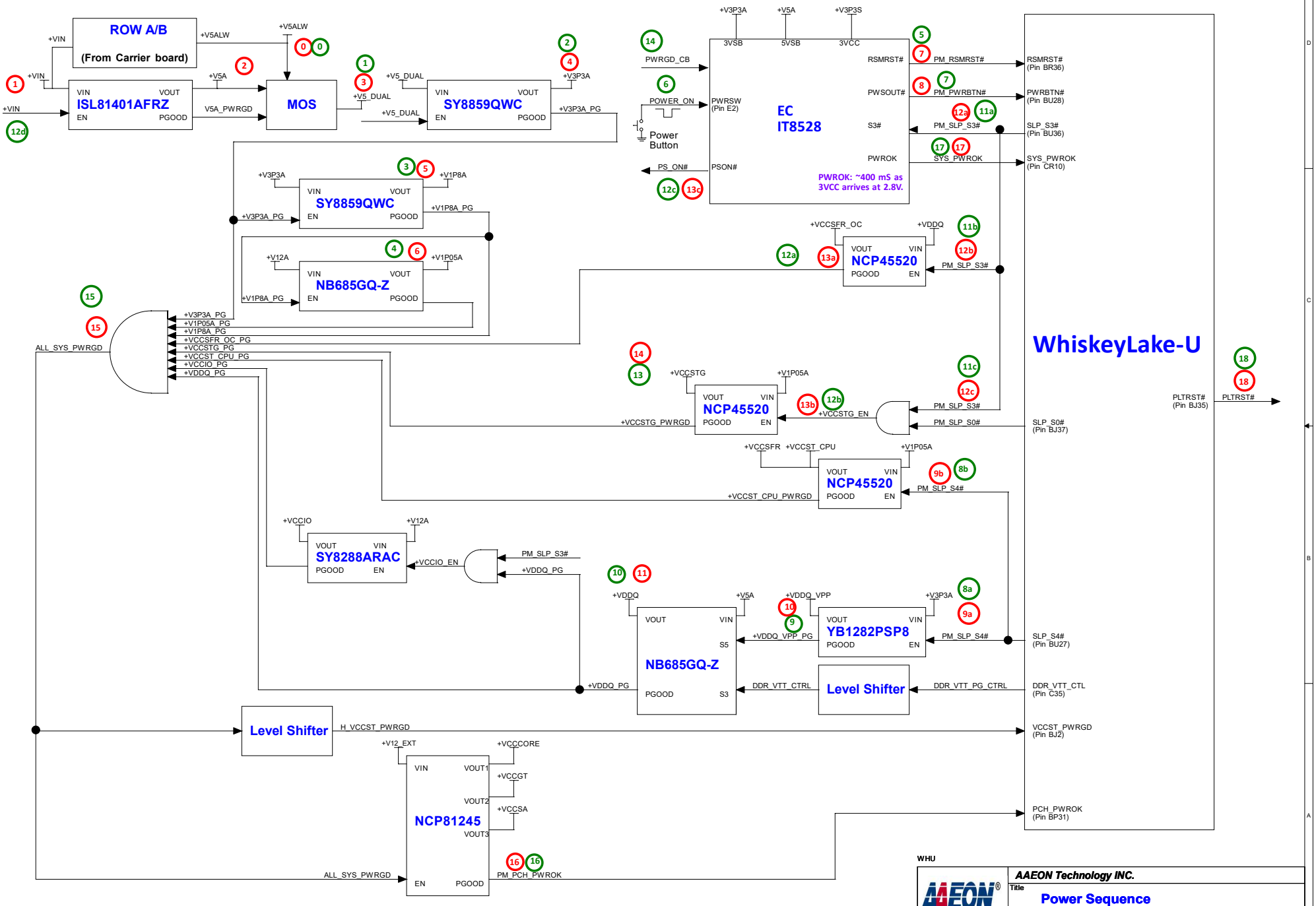
Power Sequence

ATX AT



WHU

AAEON Technology INC.		
Title: Power Sequence		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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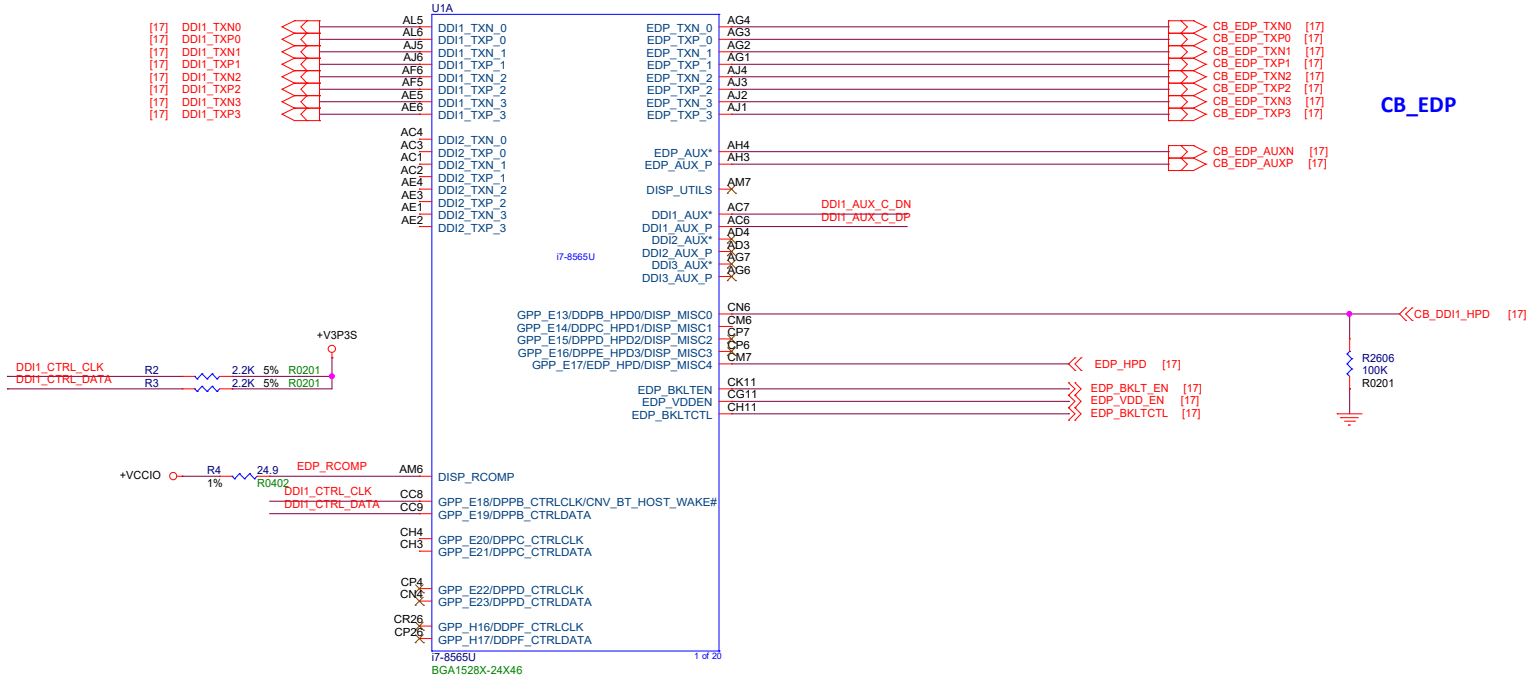
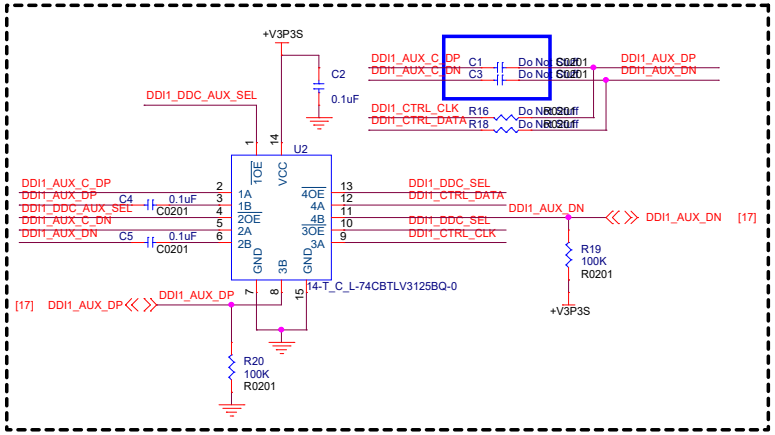
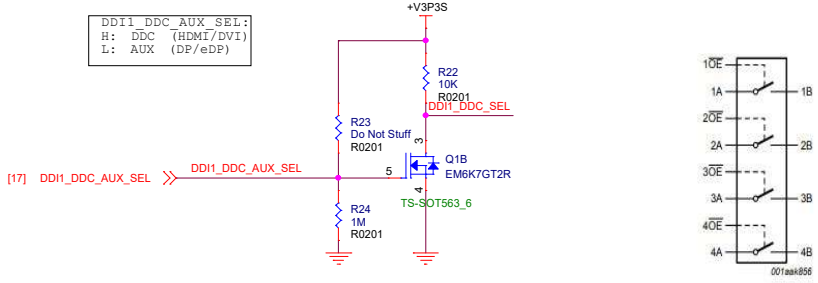
SoC DDI







WHU

AAEON Technology INC.		
Title: SoC DDI		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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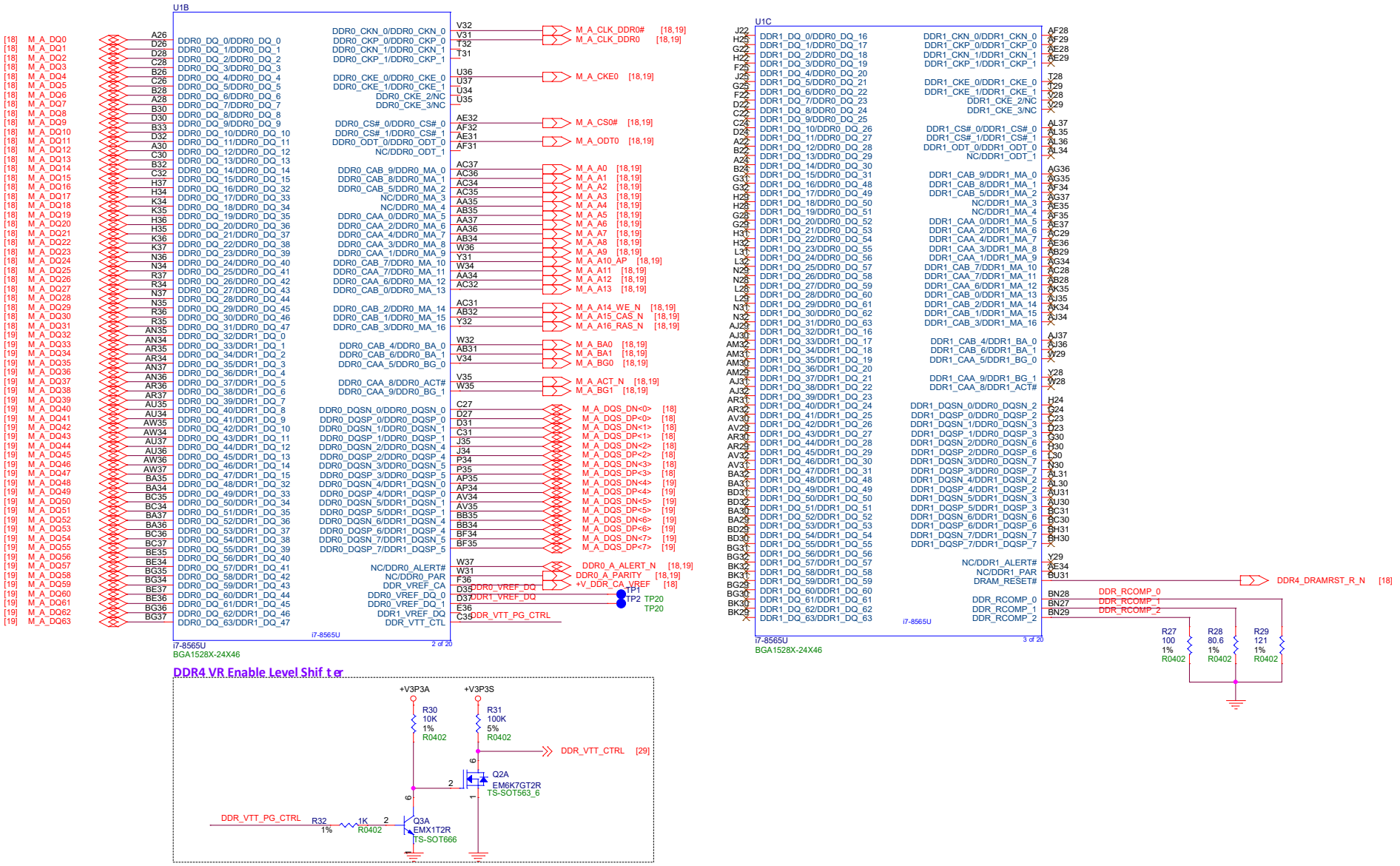
SoC DDR4



DDR4 VR Enable Level Shift

WHU

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Title: SoC DDR4		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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SoC SPI/LPC/SMBus

CONSENT STRAP

+V3.3A_1.8A_PCH_SPI

SPI0_IO2_R — R35 100K 5% R0402 — R38 Do Not Stuff R0402

High - Disabled
Low - Enabled
Weak Internal PU

ESPI or LPC

+V3P3A

SML0ALERT# — R33 Do Not Stuff R0201 — R36 20K 1% R0201

High - ESPI Is Selected For EC
Low - LPC Selected
Weak Internal PD

TLS CONFIDENTIALITY

+V3P3A

SMBALERT# — R34 4.7K 5% R0201 — R37 Do Not Stuff R0201

High - TLS Confidentiality Disable
Low - TLS Confidentiality Enable
Weak Internal PD

A0 PERSONALITY STRAP

+V3.3A_1.8A_PCH_SPI

SPI0_IO3_R — R40 100K 5% R0402 — R43 Do Not Stuff R0402

High - Disabled
Low - Enabled
Weak Internal PU

BOOT HALT

+V3.3A_1.8A_PCH_SPI

SPI0_SI_R — R41 100K 5% R0402 — R44 Do Not Stuff R0402

High - Disabled
Low - Enabled
Weak Internal PU

EXI BOOT STALL BYPASS

+V3P3A

SML1ALERT# — R39 Do Not Stuff R0402 — R42 Do Not Stuff R0402

High - Enable (BSSB 2+2)
Low - Disable (BSSB 4 Wire)
Weak Internal PD

U1E — i7-8565U — BGA1528X-24X46 — 5 of 20

[23] SPI0_CLK — CH37 SPI0_CLK
[23] SPI0_SO — CF37 SPI0_MISO
[23] SPI0_SI — CF36 SPI0_MOSI
[23] SPI0_DQ2_WP# — R48 Do Not Stuff R0201 — SPI0_IO2_R — CF34 SPI0_IO2
[23] SPI0_DQ3_HOLD# — R49 Do Not Stuff R0201 — SPI0_IO3_R — CG34 SPI0_IO3
[23] SPI0_CS0# — CG36 SPI0_CS0#
CG35 SPI0_CS1#
CH34 SPI0_CS2#

CF20 GPP_D1/SPI1_CLK/BK1/SBK1
CG22 GPP_D2/SPI1_MISO_IO1/BK2/SBK2
CF22 GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
CG23 GPP_D21/SPI1_IO2
CH23 GPP_D22/SPI1_IO3
CG20 GPP_D0/SPI1_CS0#/BK0/SBK0

CH7 CL_CLK
CH8 CL_DATA
CH9 CL_RST#

BV29 GPP_A0/RCIN#/TIME_SYNC1
BV28 GPP_A6/SERIRQ

GPP_C0/SMBCLK — CK14 SMB_CLK
GPP_C1/SMBDATA — CH15 SMB_DATA
GPP_C2/SMBALERT# — CJ15 SMBALERT#

GPP_C3/SML0CLK — CH14 LAN_SM_CLK — LAN_SM_CLK [20]
GPP_C4/SML0DATA — CF15 LAN_SM_DATA — LAN_SM_DATA [20]
GPP_C5/SML0ALERT# — CG15 SML0ALERT#

GPP_C6/SML1CLK — CN15 SML1_CLK — SML1_CLK [21]
GPP_C7/SML1DATA — CM15 SML1_DATA — SML1_DATA [21]
GPP_B23/SML1ALERT#/PCHHOT# — CC34 SML1ALERT#

GPP_A1/LAD0/ESPI_IO0 — CA29 LPC_AD0_R — R2612 22 5% R0201 — LPC_AD0 [17,21]
GPP_A2/LAD1/ESPI_IO1 — BY29 LPC_AD1_R — R2613 22 5% R0201 — LPC_AD1 [17,21]
GPP_A3/LAD2/ESPI_IO2 — BY27 LPC_AD2_R — R2614 22 5% R0201 — LPC_AD2 [17,21]
GPP_A4/LAD3/ESPI_IO3 — BV27 LPC_AD3_R — R2615 22 5% R0201 — LPC_AD3 [17,21]
GPP_A5/LFRAME#/ESPI_CS# — CA28 LPC_FRAME# — LPC_FRAME# [17,21]
GPP_A14/SUS_STAT#/ESPI_RESET# — CA27 — PM_SUS_STAT#_R [17,21]

GPP_A9/CLKOUT_LPC0/ESPI_CLK — BV32 ESPI_CLK_SoC — R60 33 5% R0201 — PCI_CLK_LPC [17]
GPP_A10/CLKOUT_LPC1 — BV30 LPC_CLK_SOC — R61 22 5% R0201 — LPC_CLK_EC [21]
GPP_A8/CLKRUN# — BV30 — PM_CLKRUN#

R63 8.2K 1% R0402 +V3P3S

Carrier board

I219

EC

+V3P3A

SMB_CLK — R51 1K 1% R0402
SMB_DATA — R52 1K 1% R0402
LAN_SM_CLK — R53 499 1% R0402
LAN_SM_DATA — R54 499 1% R0402
PM_SUS_STAT#_R — R55 Do Not Stuff R0402
SML1_CLK — R56 1K 1% R0402
SML1_DATA — R57 1K 1% R0402

+V3P3S

R59 10K 1% R0402
[21] KBRST#
[17,21] INT_SERIRQ
R64 10K 1% R0402
+V3P3S

XDP

+VCCST_CPU
+VCCSTG

R71 1K 1% R0402
R72 1K 1% R0402
R73 49.9 1% R0402

[21] PECI_EC — R79 43 5% — PECI
[31] H_PROCHOT_N — R80 499 1% — PROCHOT# — CATERR# — PROCHOT_N — THRMTRIP#
H_THRMTRIP_# — R81 60.4 1% — THRMTRIP#

R0402 R0402 R0402

U1D — i7-8565U — BGA1528X-24X46 — 4 of 20

CATERR# AA4
PECI AR1
PROCHOT# Y4
THRMTRIP# BJ1

BPM#_0 U1
BPM#_1 U2
BPM#_2 U3
BPM#_3 U4

PROC_TCK — T6 XDP_CPU_JTAG_TCLK
PROC_TDI — U6 XDP_CPU_JTAG_TDI
PROC_TDO — Y5 XDP_CPU_JTAG_TDO
PROC_TMS — T5 XDP_CPU_JTAG_TMS
PROC_TRST# — AB6 XDP_CPU_JTAG_TRST_N

PCH_TCK — W6 XDP_PCH_JTAG_TCLK
PCH_TDI — U5 XDP_CPU_JTAG_TDI
PCH_TDO — W5 XDP_CPU_JTAG_TDO
PCH_TMS — P5 XDP_CPU_JTAG_TMS
PCH_TRST# — Y6 XDP_CPU_JTAG_TRST_N
PCH_JTAGX — P6 XDP_CPU_JTAG_TCLK

GPP_E3/CPU_GP0 — CE9
GPP_E7/CPU_GP1 — CN3
GPP_B3/CPU_GP2 — CB34
GPP_B4/CPU_GP3 — CC35

PROC_PREQ# — W2
PROC_PRDY# — W1

PROC_POPIRCOMP — BP27
PCH_OPIRCOMP — BW25

R90 49.9 1% R0402
R91 49.9 1% R0402

+V3P3A — R68 0 5% R0402 — +V3.3A_1.8A_PCH_SPI

a0.2 remove

+V3P3A
Q15A — SMBALERT# — EM6K7GT2R TS-SOT563_6 — R75 2.2K 5% R0201 — SMB_ALERT#_M [17]
Q4A — SMB_DATA — EM6K7GT2R TS-SOT563_6 — R83 2.2K 5% R0201 — SMB_DATA_M [17]
Q4B — SMB_CLK — EM6K7GT2R TS-SOT563_6 — R89 2.2K 5% R0201 — SMB_CLK_M [17]

+VCCSTG

XDP_CPU_JTAG_TDO — R74 100 R0201
XDP_CPU_JTAG_TDI — R76 Do Not Stuff R0402
XDP_CPU_JTAG_TMS — R77 Do Not Stuff R0402
XDP_CPU_JTAG_TCLK — R78 51 1% R0402
XDP_CPU_JTAG_TRST_N — R82 Do Not Stuff R0402

XDP_PCH_JTAG_TCLK — R88 Do Not Stuff R0402

WHU

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Title: SoC SPI/LPC/SMBus

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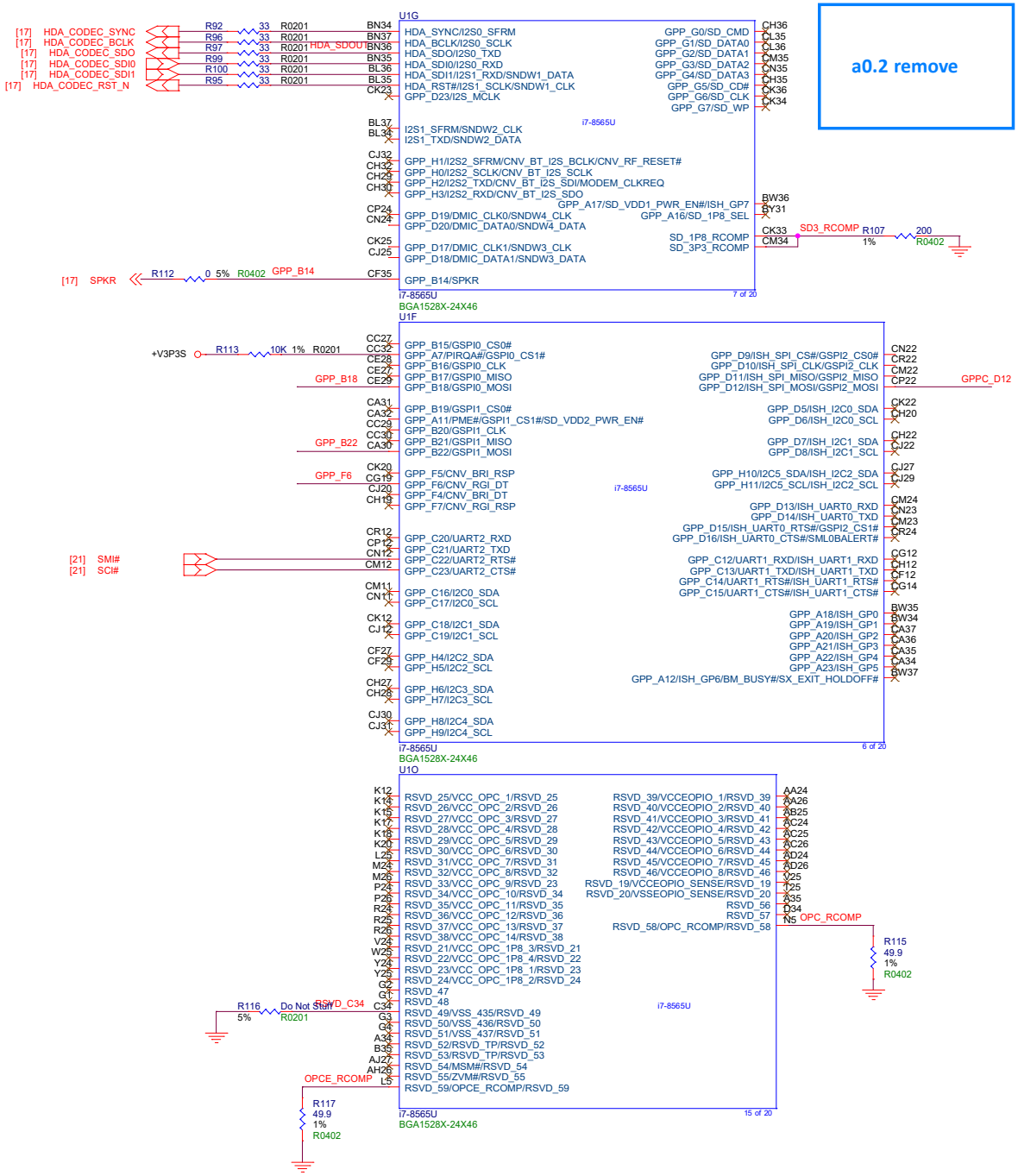
SoC HDA/SD



TOP SWAP OVERRIDE

GPP_B14 R93 Do Not Stuff 5% R0402

High - Top Swap Enable
Low - Disable
Weak Internal PD

NO REBOOT +V3P3S

GPP_B18 R94 Do Not Stuff R0402 R98 Do Not Stuff R0402

High - No Reboot
Low - Rebbot Enable
Weak Internal PD

BOOT BIOS STRAP +V3P3S

GPP_B22 R101 Do Not Stuff R0402 R103 Do Not Stuff R0402

High - LPC Selected For System Flash
Low - SPI Selected (Default)
Weak Internal PD

JTAG ODT DISABLE +V3P3A

GPPC_D12 R102 20K 5% R0402 R104 Do Not Stuff R0402

High - JTAG ODT Enabled
Low - JTAG ODT Disabled
Weak Internal PU

Integrated CNVi Set ti +V1P8A a0.2

GPP_F6 R110 20K 1% R0201 R111 Do Not Stuff R0201

High - Integrated CNVi disable
Low - Integrated CNVi enable
Weak Internal PU

FLASH DESCRIPTOR SECURITY OVERRIDE

+VCCPAZIO_3P3_1P8_1P5

HDA_SDOUT R114 Do Not Stuff R0402

High - Overriden
Low - Security Measures Not Overriden
Weak Internal PD

WHU

AAEON Technology INC.

Title: SoC HDA/ SD			
Size: Custom	Document Number: NANOCOM-WHU		Rev: A0.3_0_0
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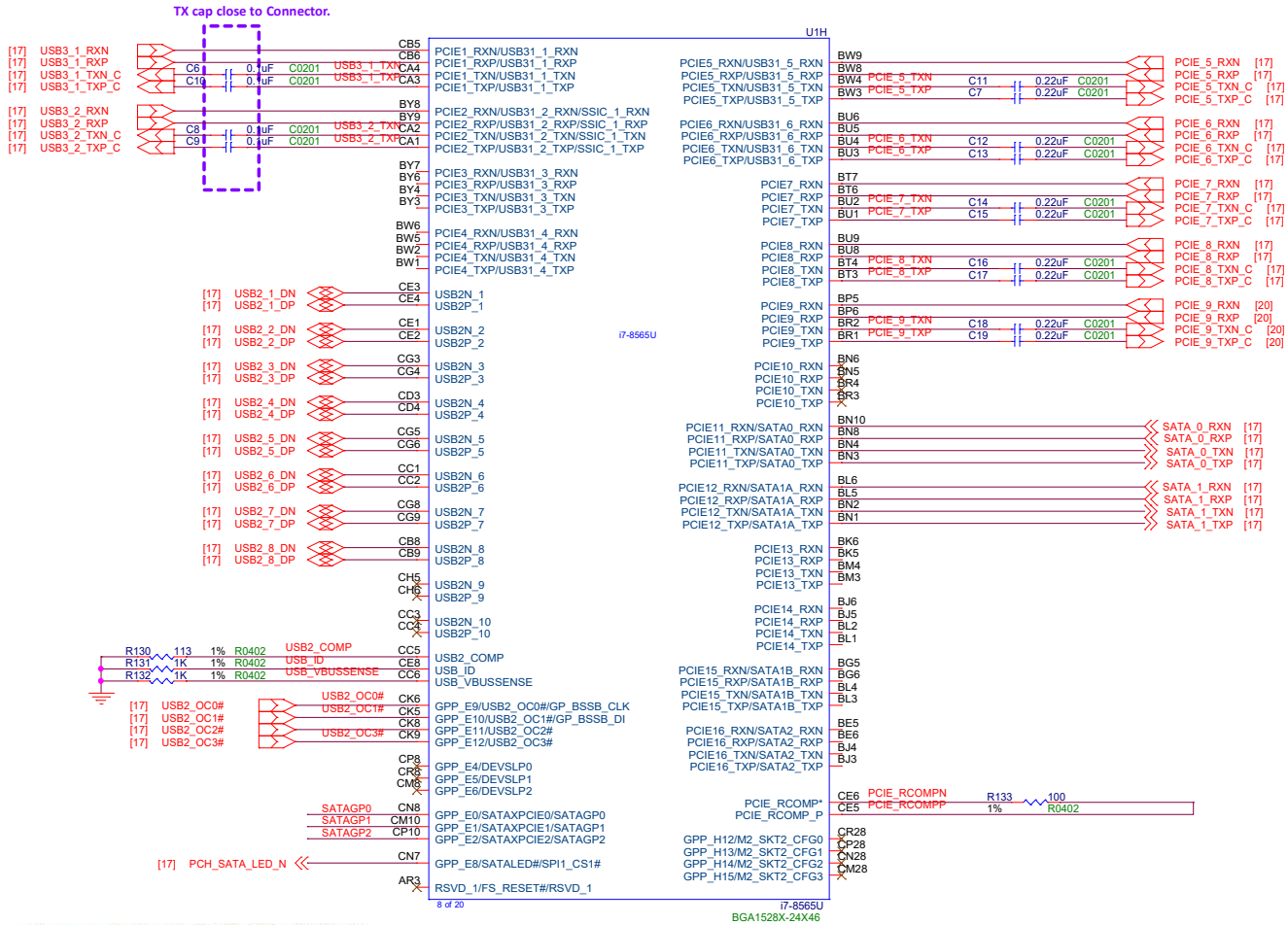
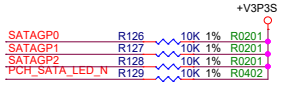
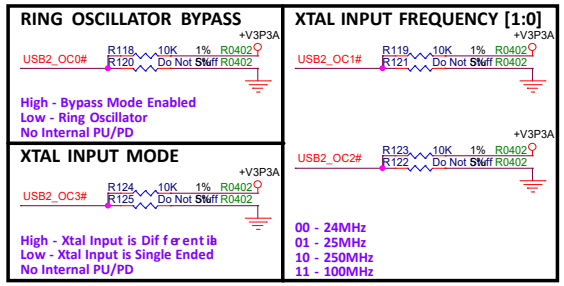
SoC PCIe/SATA/USB

USB 3.0



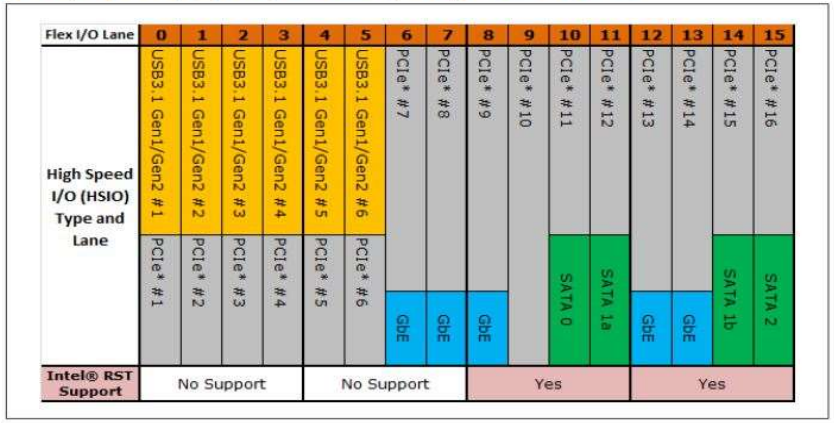
PCIe for LAN





6.1.2.1 Cannon Lake U (CNL U) PCH-LP

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP



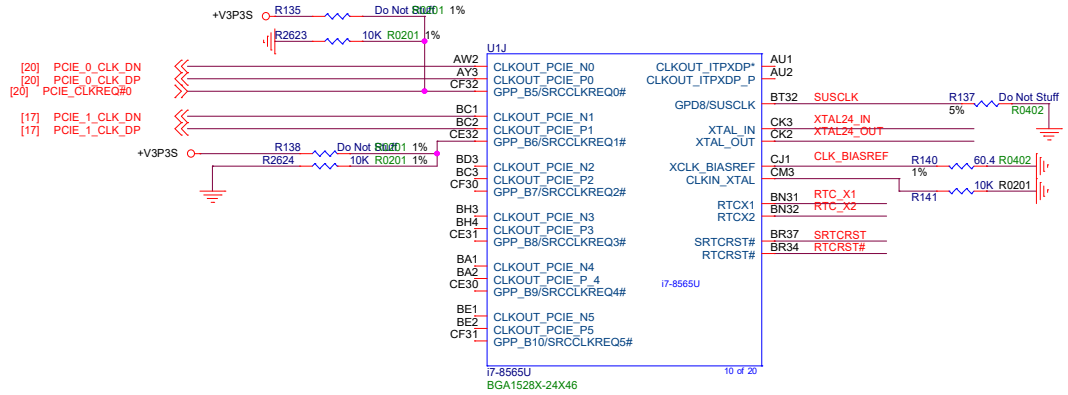
WHU

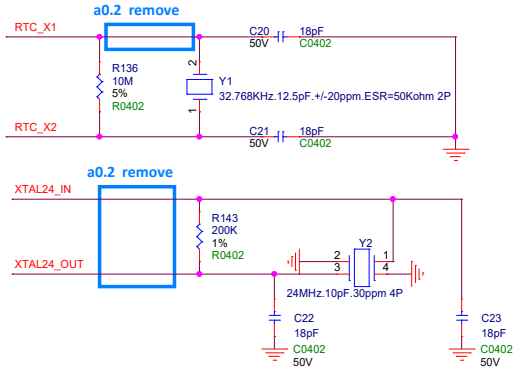
AAEON Technology INC.		
Title: SoC PCIe/SATA/USB		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
Date: Thursday, January 02, 2020	Sheet 9 of 34	

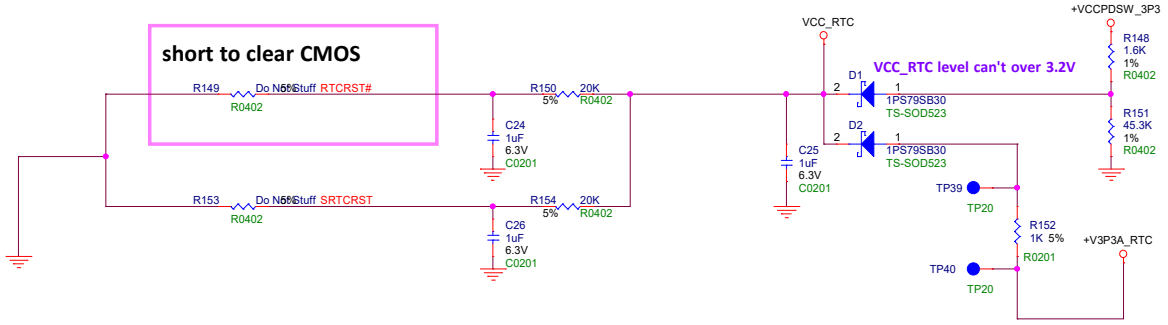
SoC PCIE_CLK/ RTC

LAN I219

Carrier board







Whiskey Lake U					NANOCOM-WHU	Whiskey Lake U	NANOCOM-WHU
1	USB3 #1	PCIE #1			USB3.0 to CB	USB2 #1	USB2 to CB
2	USB3 #2	PCIE #2			USB3.0 to CB	USB2 #2	USB2 to CB
3	USB3 #3	PCIE #3				USB2 #3	USB2 to CB
4	USB3 #4	PCIE #4				USB2 #4	USB2 to CB
5	USB3 #5	PCIE #5			PCIE [X4]	USB2 #5	USB2 to CB
6	USB3 #6	PCIE #6			PCIE [X4]	USB2 #6	USB2 to CB
7		PCIE #7	GbE		PCIE [X4]	USB2 #7	USB2 to CB
8		PCIE #8	GbE		PCIE [X4]	USB2 #8	USB2 to CB
9		PCIE #9	GbE		PCIE for LAN i219	USB2 #9	
10		PCIE #10		Intel RST		USB2 #10	
11		PCIE #11	SATA 0	Support			
12		PCIE #12	SATA 1A				
13		PCIE #13	GbE				
14		PCIE #14	GbE	Intel RST			
15		PCIE #15	SATA 1b	Support			
16		PCIE #16	SATA 2				

WHU

AAEON Technology INC.

Title: SoC PCIE_CLK/ RTC

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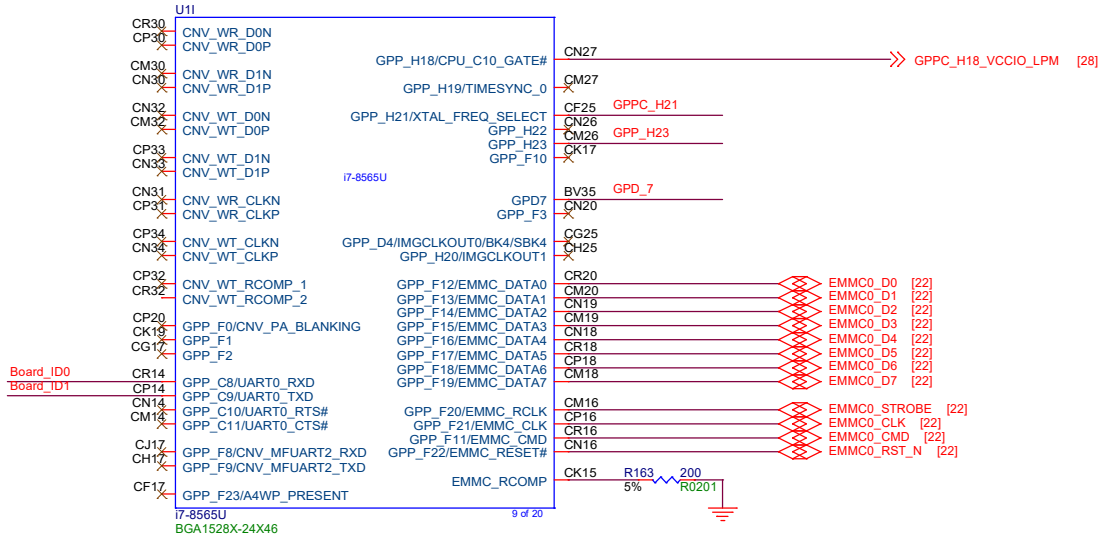
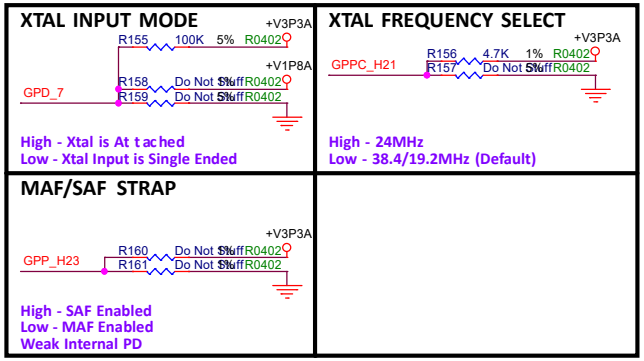
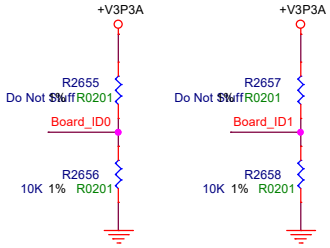
SoC eMMC





A0.3



Board ID

ID0	ID1	Description
0	0	Micron DDR4 8G
0	1	Samsung DDR4 4G
1	0	N/A
1	1	N/A

WHU

AAEON Technology INC.

Title: SoC eMMC		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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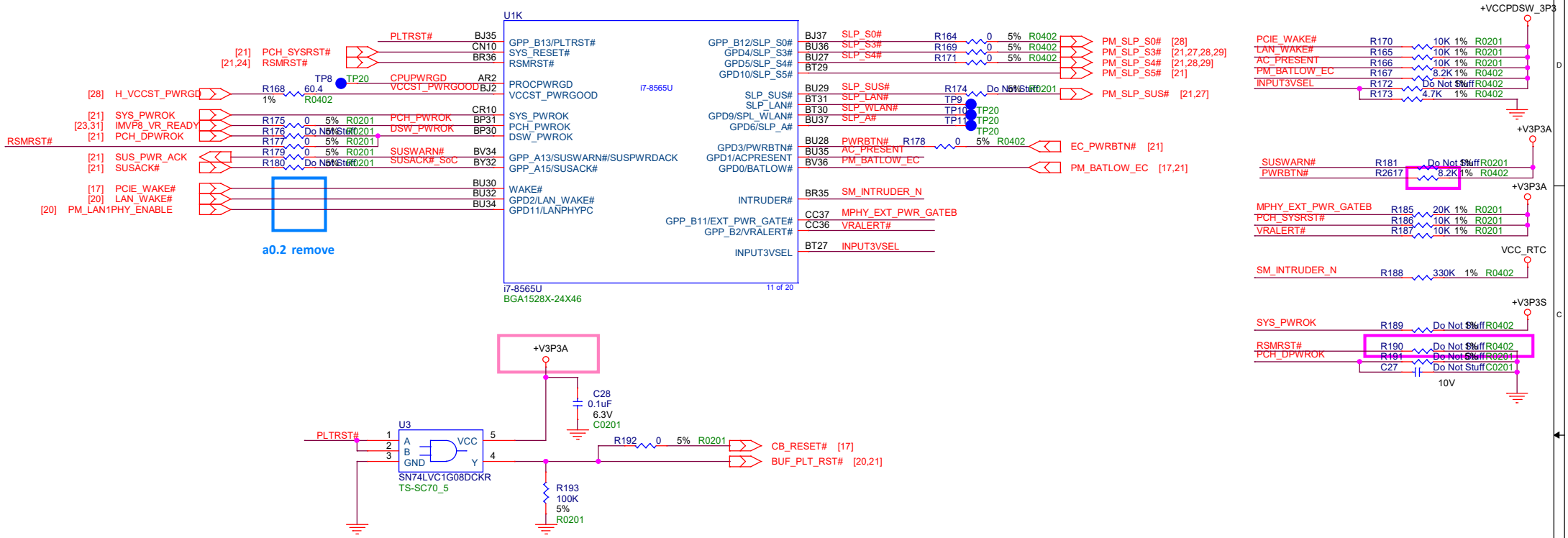
SoC System



WHU

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	Title: SoC System	
Size: B	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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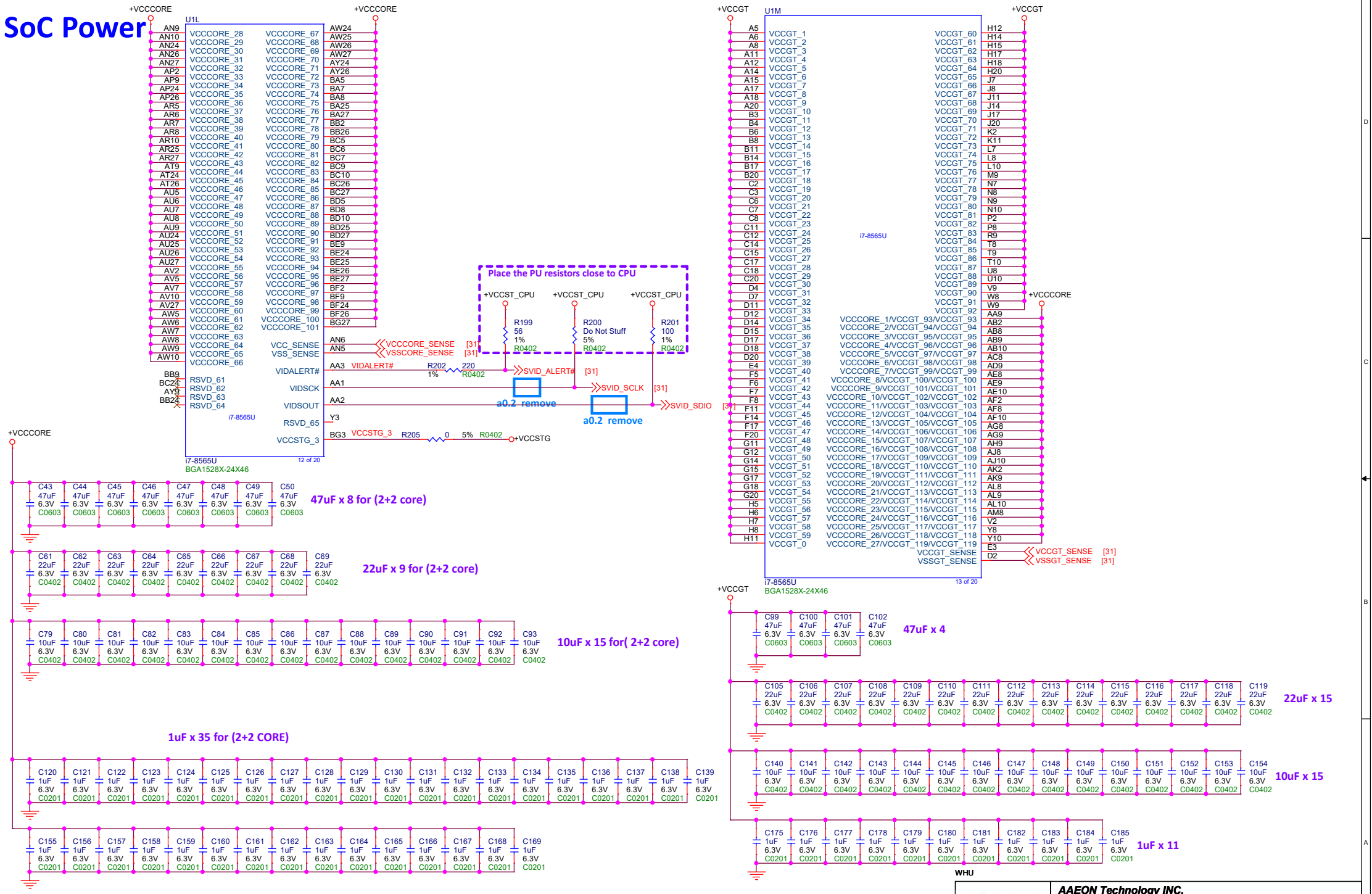
SoC Power



Title	SoC Power1		
Size	Document Number		Rev
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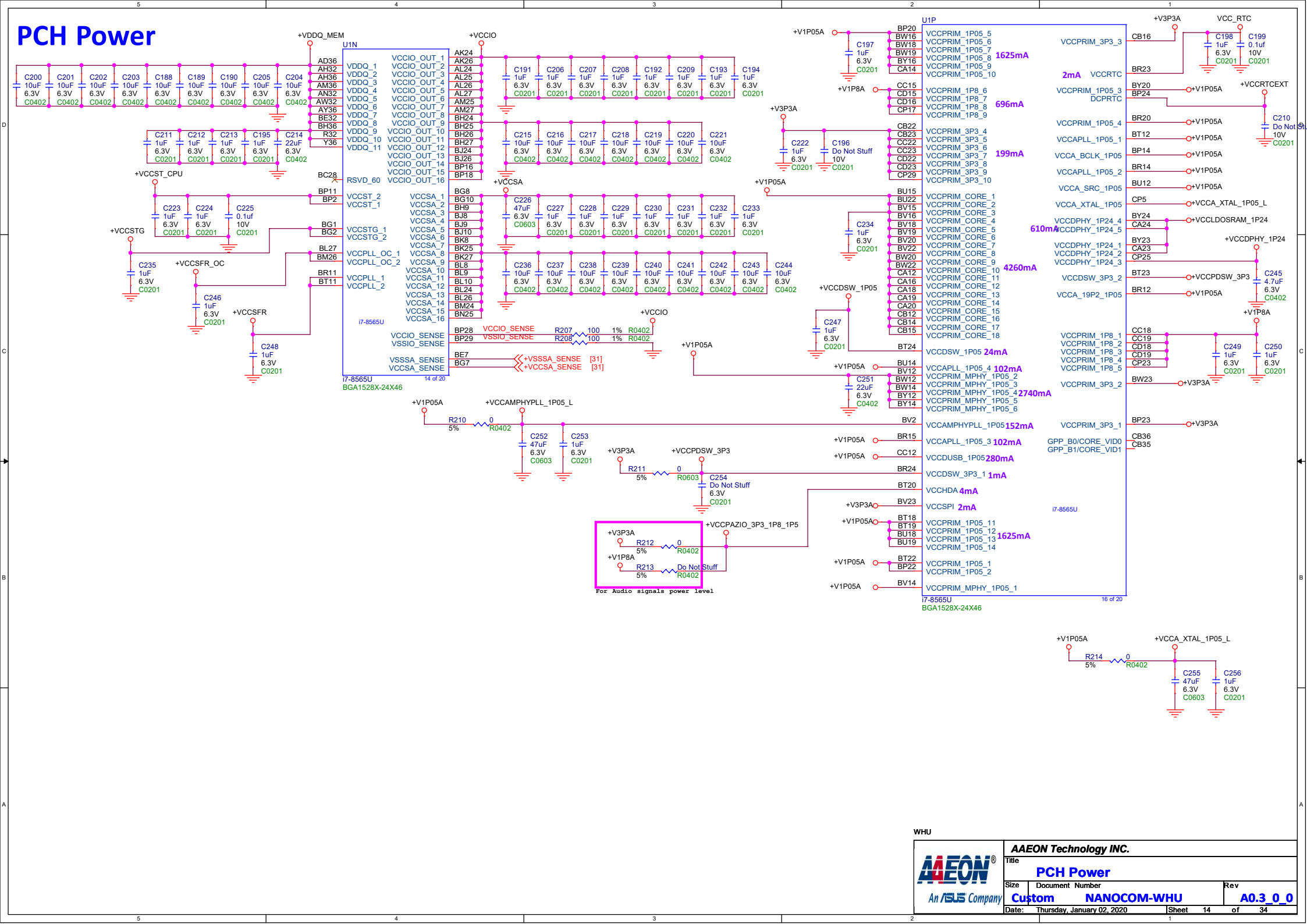
AAEON Technology INC.

An ASUS Company

WHU

PCH Power



WHU	
AAEON Technology INC.	
Title	PCH Power
Size: Custom	Document Number: NANOCOM-WHU
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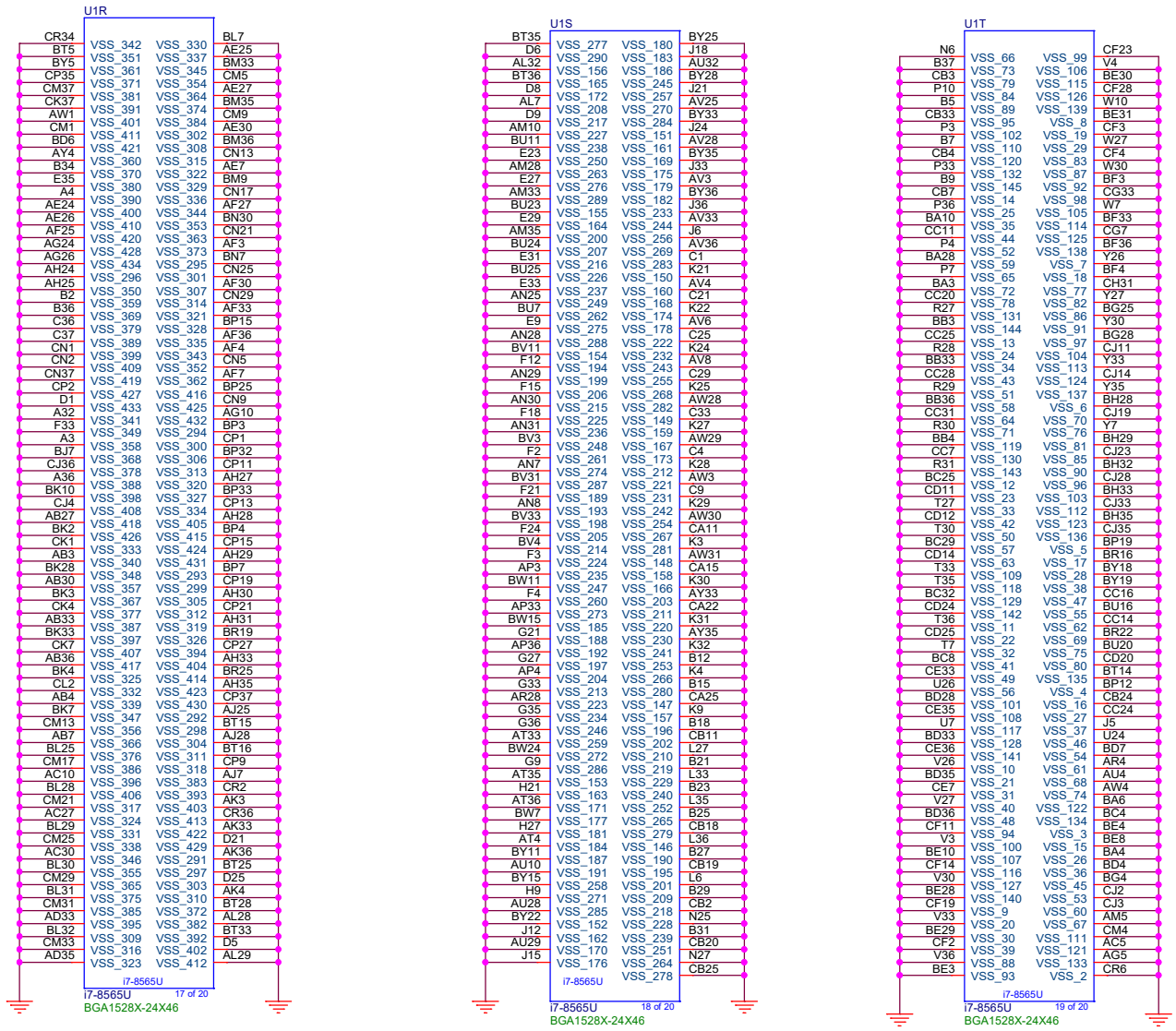
SoC GND



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AAEON Technology INC.

Title: SoC GND		
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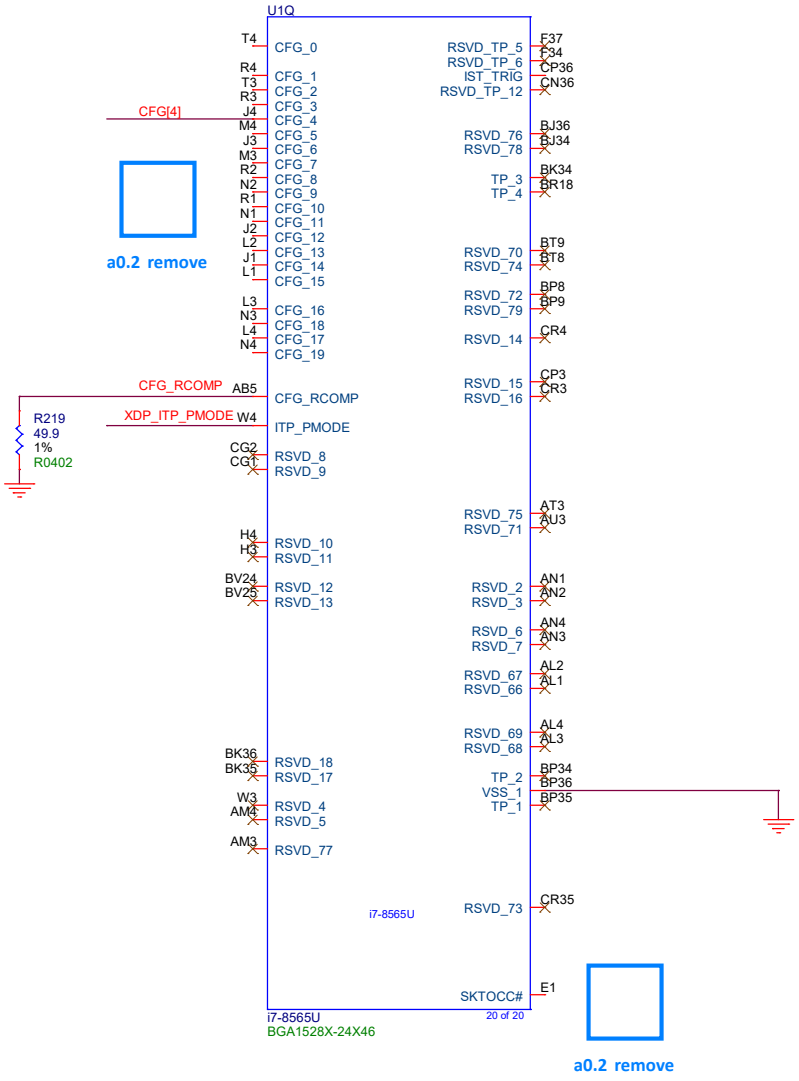
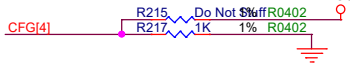
SoC Strap



DFXTESTMODE

High - DFXTESTMODE Disabled (Default)
Low - DFXTESTMODE Enabled
Weak Internal PU

DISPLAY PORT PRESENCE STRAP



High - Disabled: No Physical Display Port At t ached To eDP
Low - Enabled: An External Display Port Device Is Connected To The eDP

WHU

AAEON An ASUS Company	AAEON Technology INC.		
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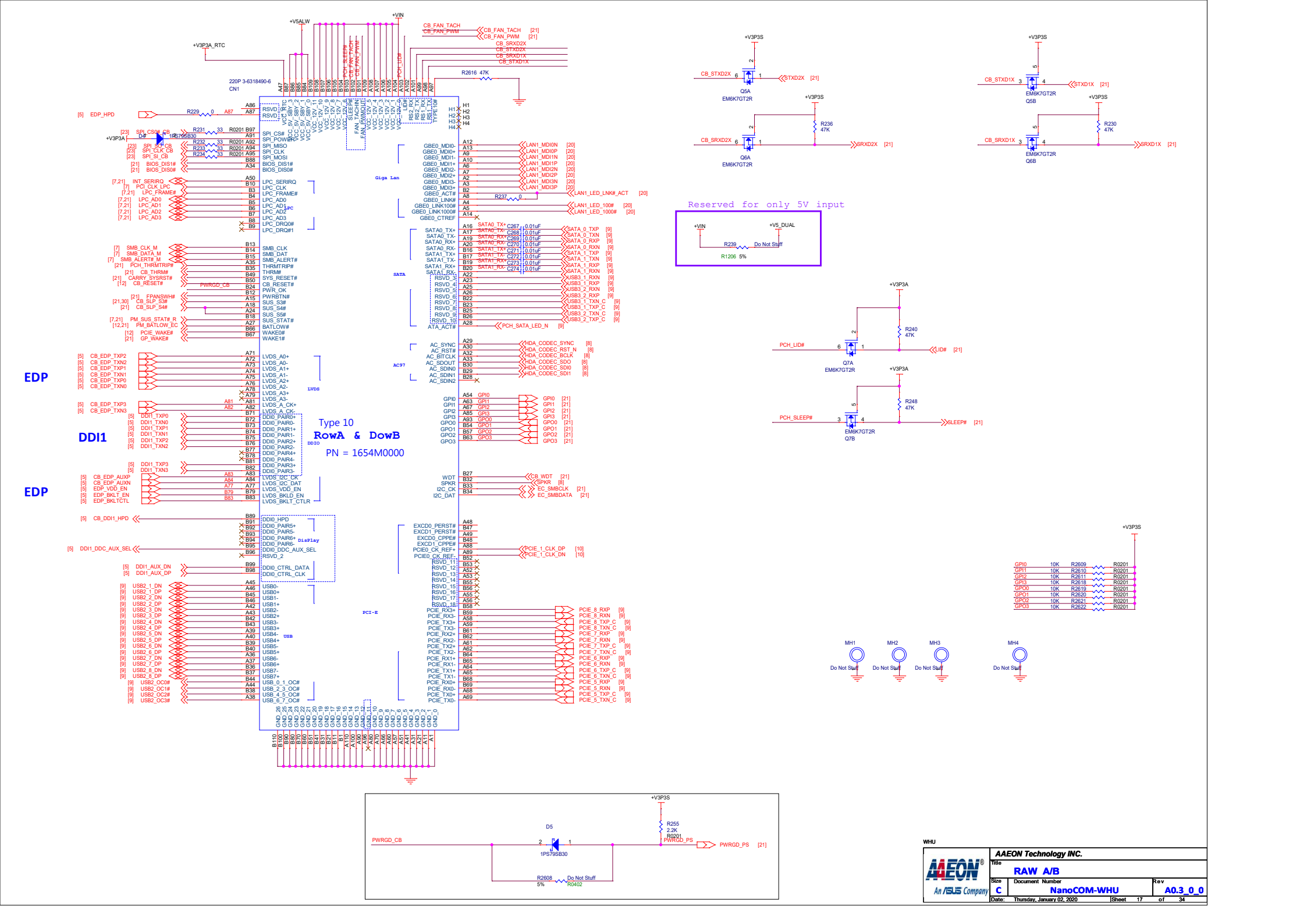
EDP
DDI1
EDP
Type 10
RowA & DowB
PN = 1654M0000
Reserved for only 5V input
Do Not Stuff
Giga Lan
SATA
AC97
LVDS
DDIO
PCI-E
USB
DisPlay
+V5ALW
+VIN
+V3P3A_RTC
+V3P3A
+V3P3S
+V5_DUAL
CN1
220P 3-6318490-6
R2616 47K
R231 33
R232 33
R233 33
R234 33
R237 0
R239 Do Not Stuff
R1206 5%
R240 47K
R248 47K
R236 47K
R230 47K
R255 2.2K
R2608 Do Not Stuff
R0402
Q5A
Q5B
Q6A
Q6B
Q7A
Q7B
EM6K7GT2R
1PS79SB30
D5
MH1
MH2
MH3
MH4
AAEON Technology INC.
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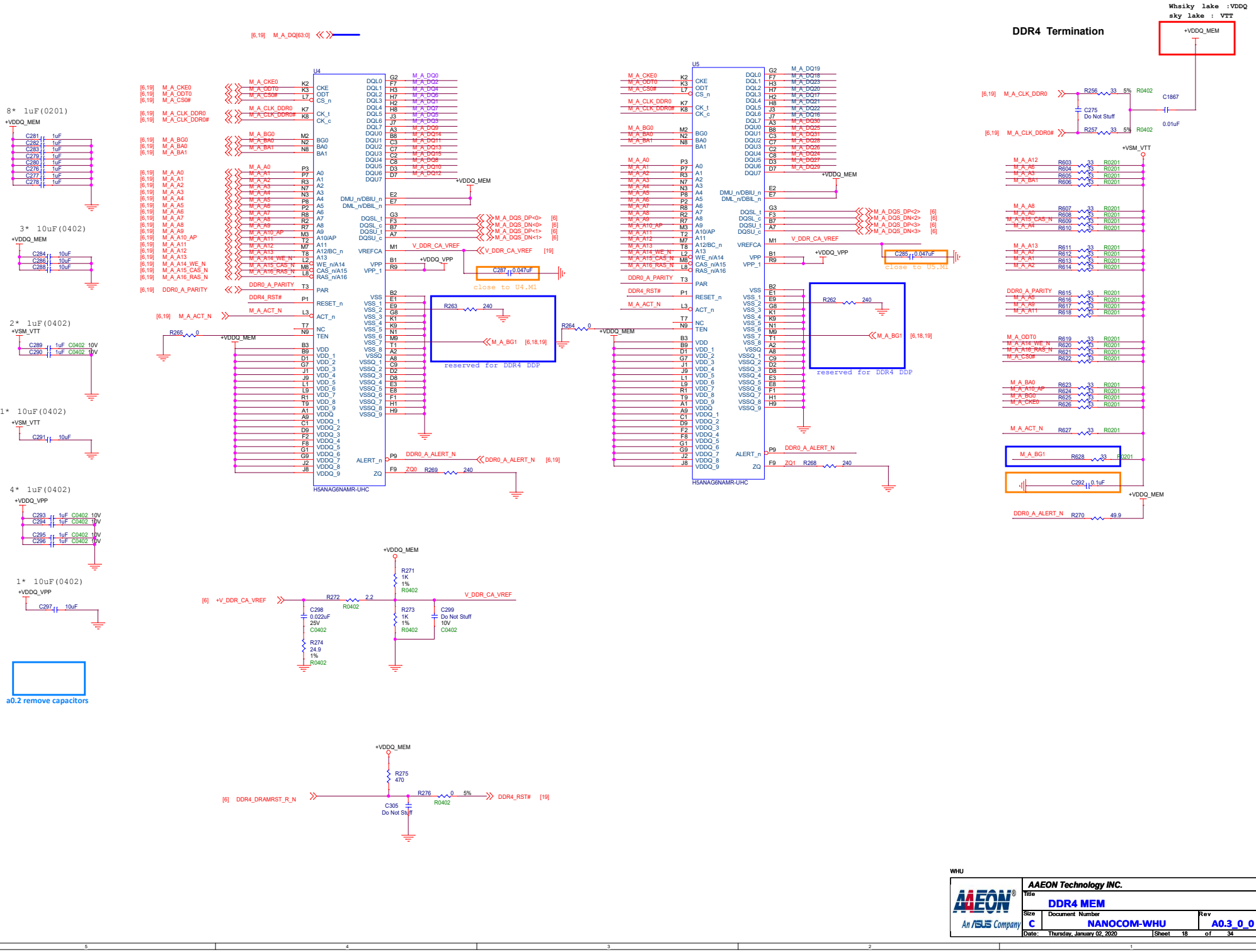
DDR4 Memory Down



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AAEON® An ASUS Company	AAEON Technology INC.	
	Title: DDR4 MEM	
	Size: C	Document Number: NANOCOM-WHU
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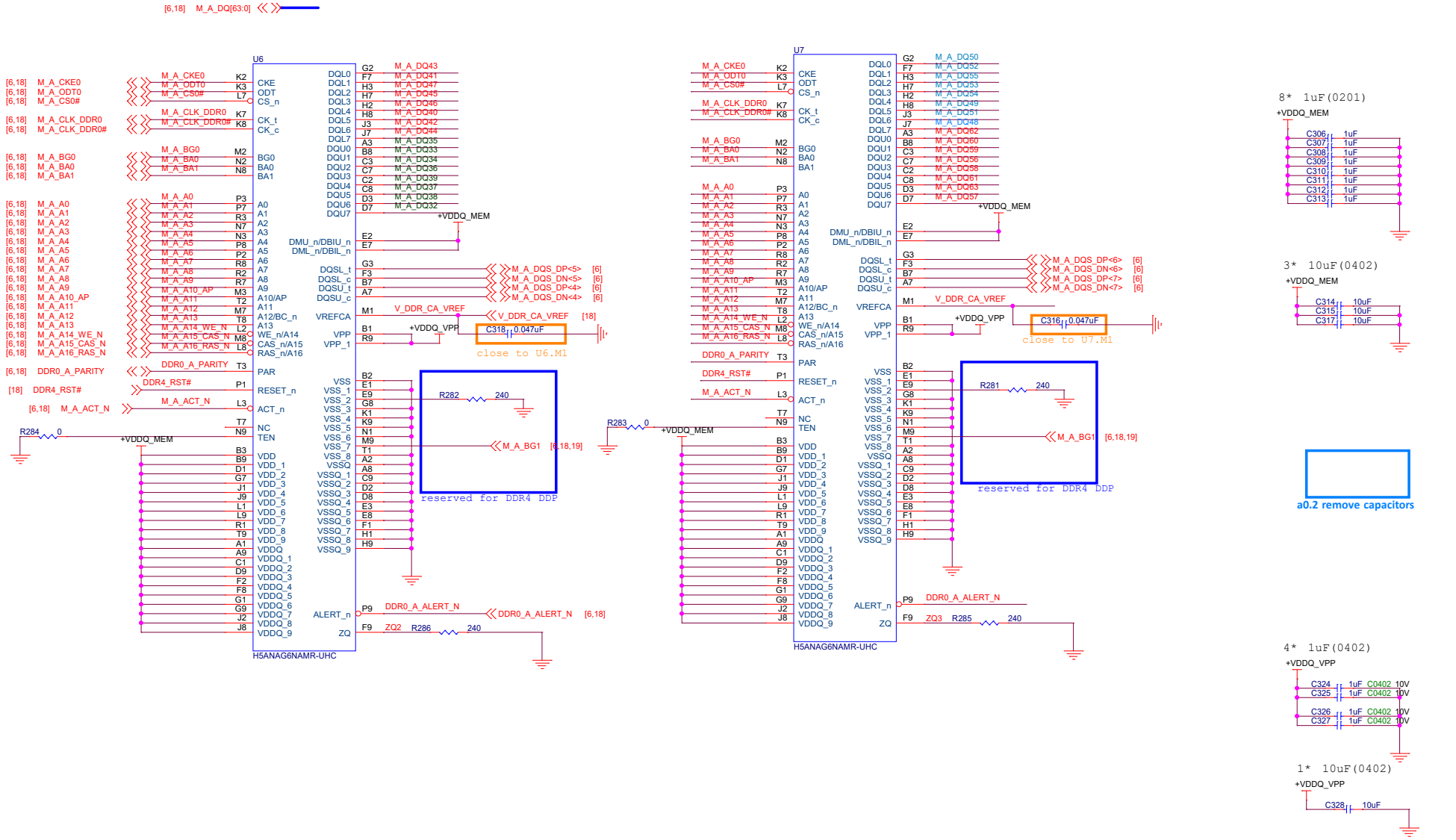

WHU

AAEON Technology INC.

Title	DDR4 MEM		
Size	Document Number		Rev
Custom	NANOCOM-WHU		A0.3_0_0
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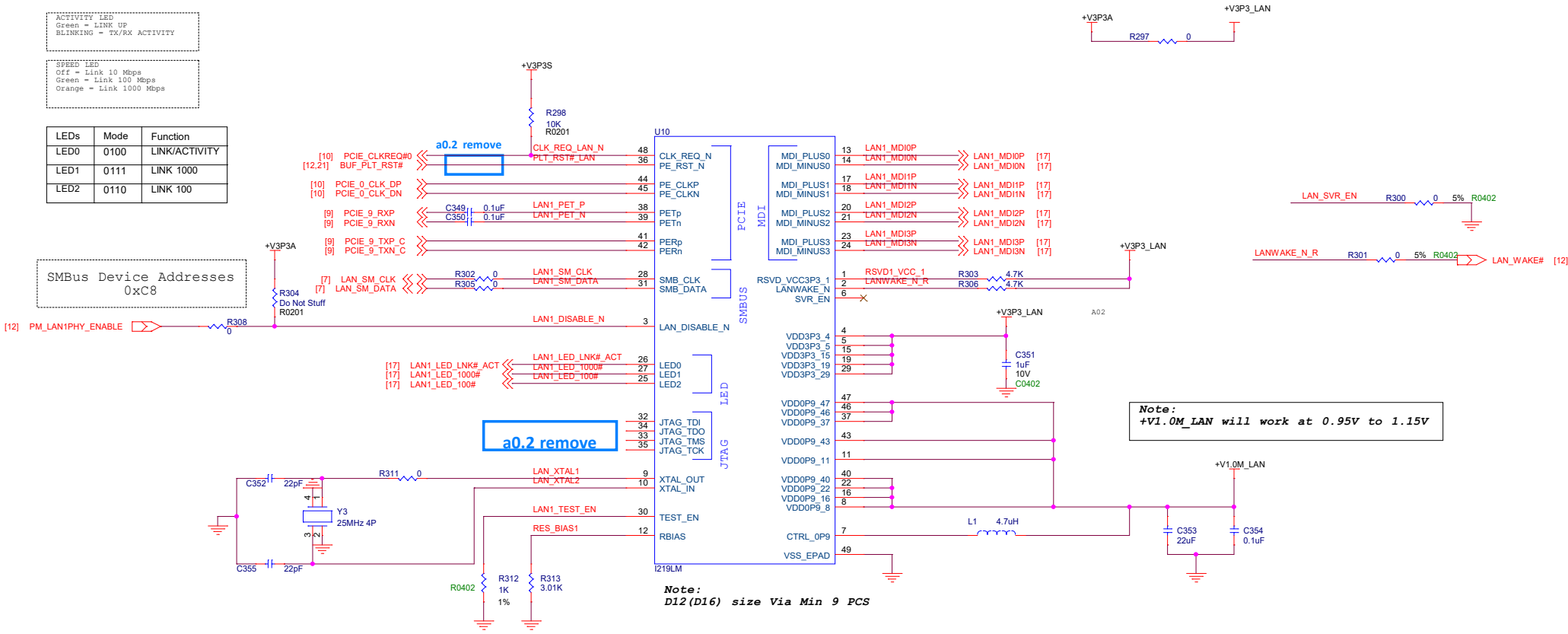

WHU

AAEON Technology INC.		
Title: LAN-I219		
Size	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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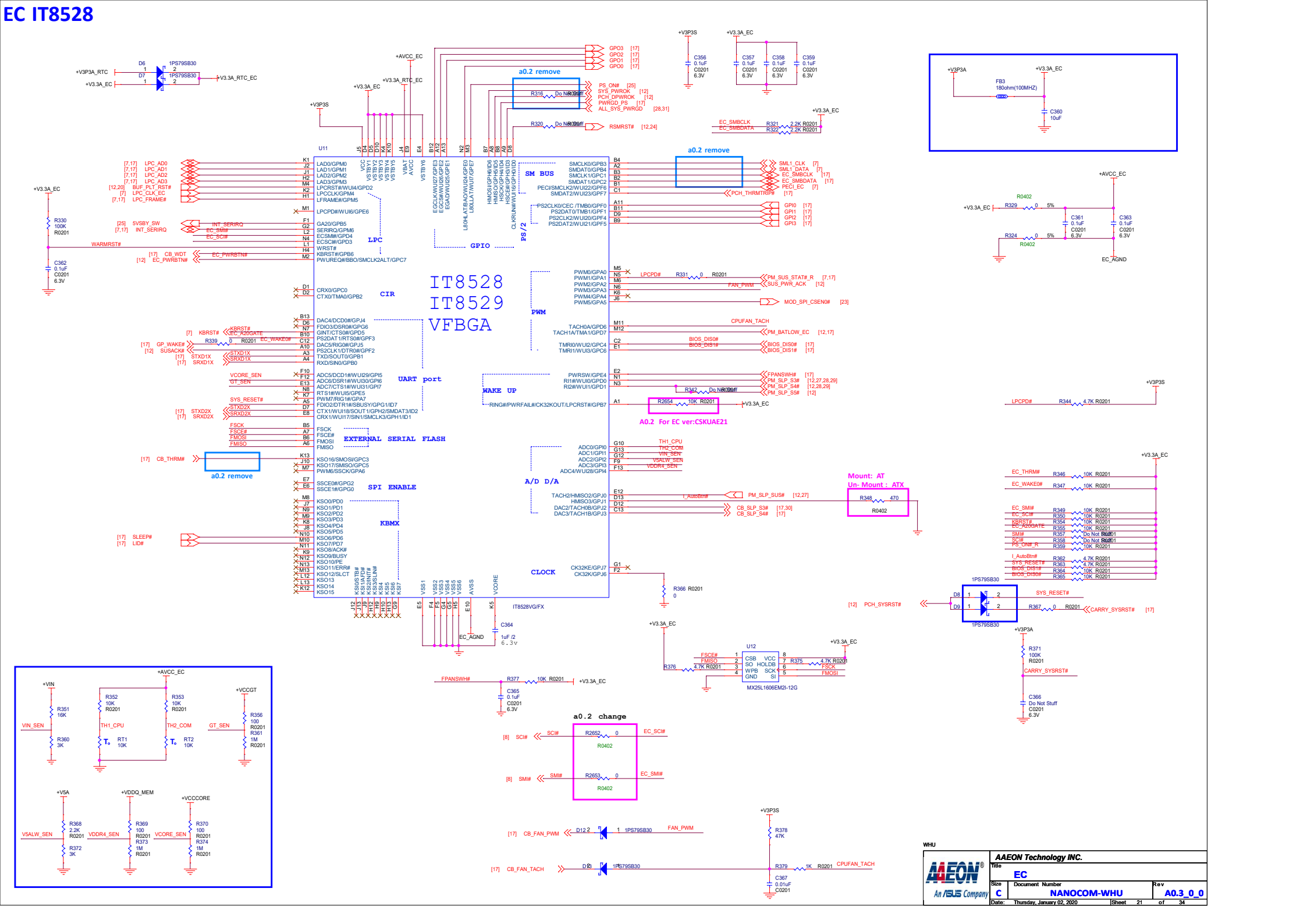
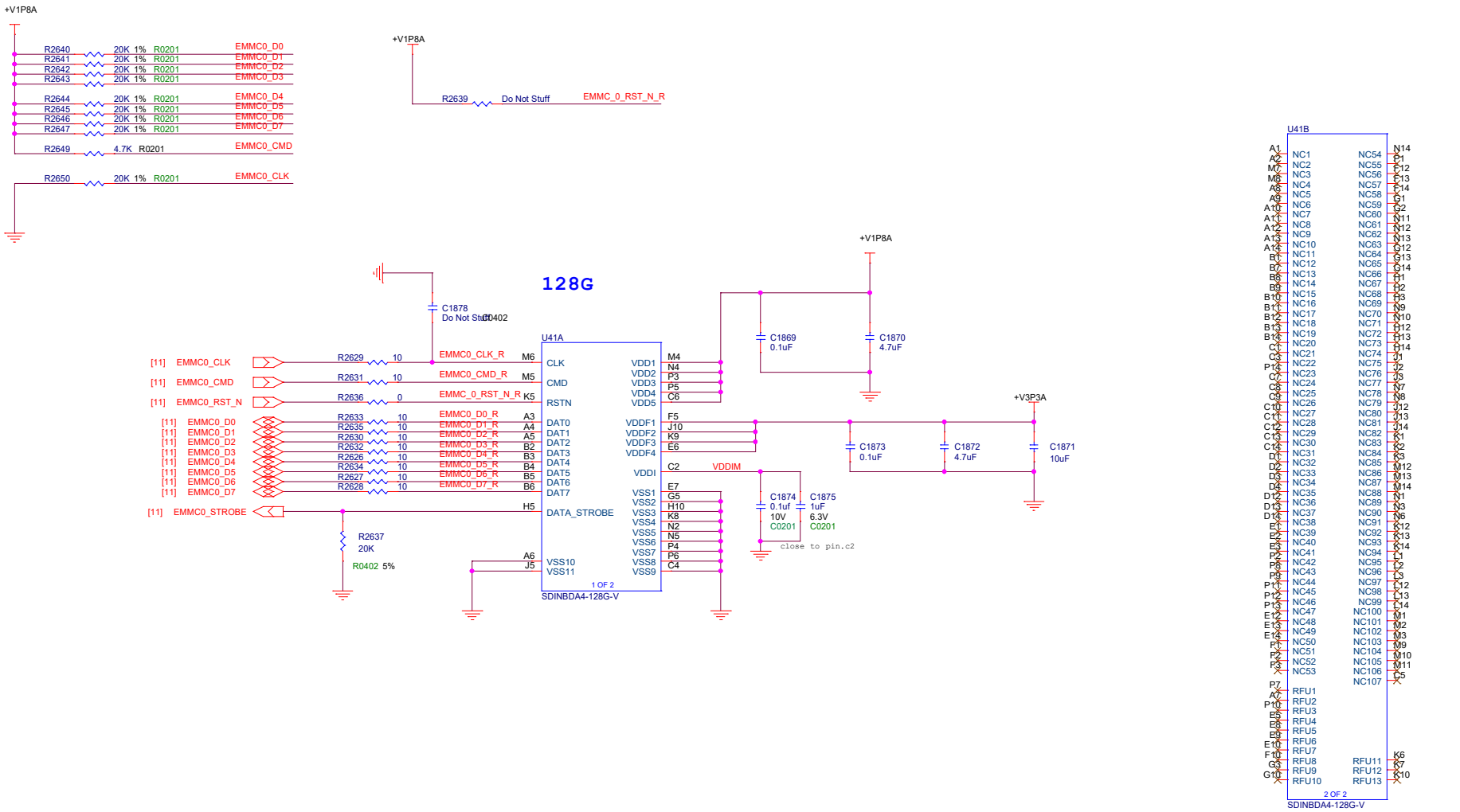
EC IT8528


U11
IT8528
IT8529
VFBGA
IT8528VG/FX
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
A/D D/A
SPI ENABLE
KBMX
CLOCK
a0.2 remove
a0.2 change
A0.2 For EC ver:CSKUAE21
Mount: AT
Un- Mount : ATX
MX25L1606EM2I-12G
EC_AGND



WHU

AAEON an ASUS assoc. co.

Title: EMMC		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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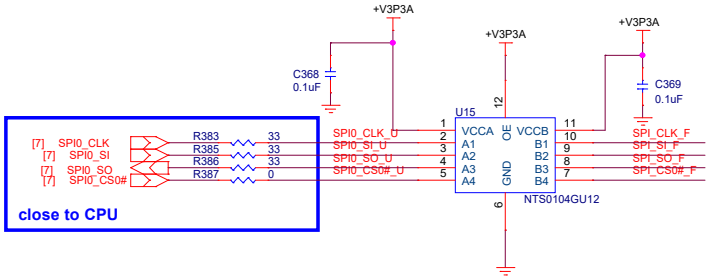
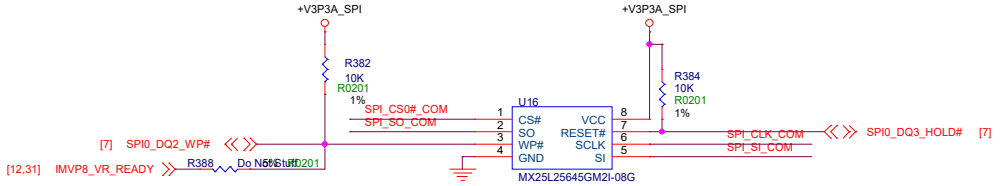
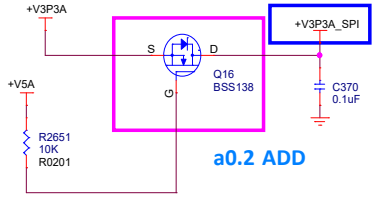
BIOS





1462002564 (TF)IC.Flash Memory.256M Bit serial.SOP-8(209mil).w/ Dual & Quad SPI.SMD.MACRONIX.MX25L25645GM2I-08G

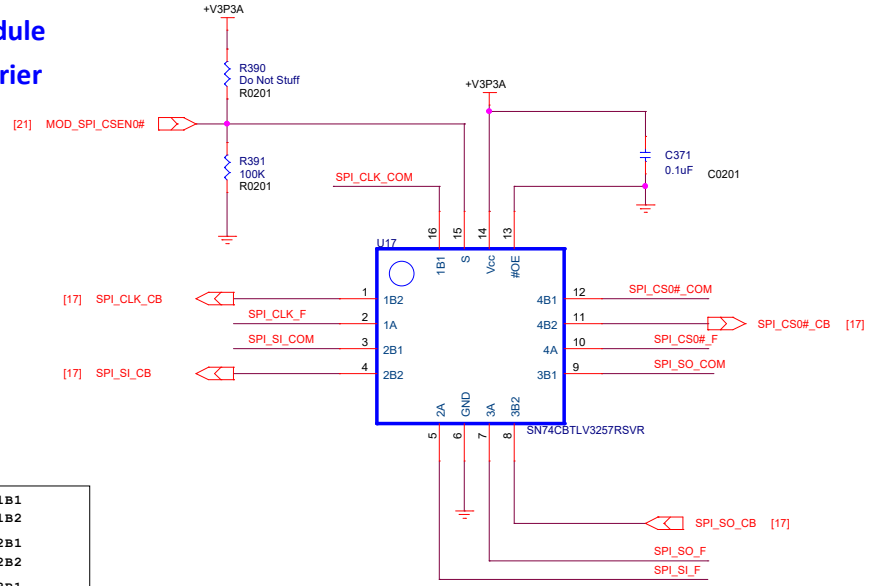
A0.2 Change to 32M

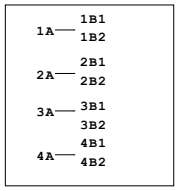


a0.2 ADD

L: Module

H: Carrier





INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

WHU

AAEON Technology INC.

Title	FAN/BIOS/ LPC/ HW Monitor		
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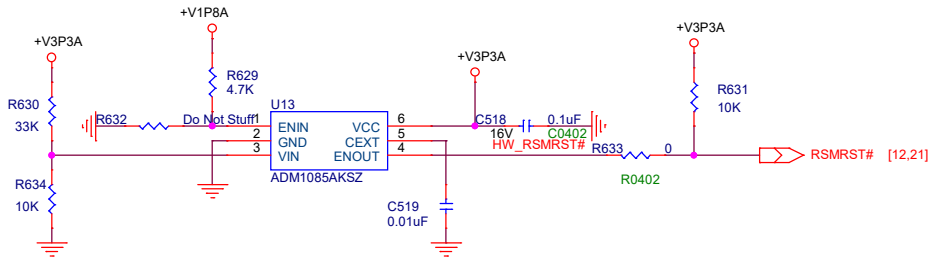
RSMRST# Control



3.3V x 10 / (10+33) = 0.767

ENIN VIH = 0.3*VCC+0.2 =1.19V
ENIN VIL = 0.3*VCC- 0.2 = 0.79V

ENOUT/ENOUT# Voltage Low (MAX =0.4V),When Vin < Vth_falling (ENOUT) / Vin > Vth_rising (ENOUT#)

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	2.25		3.6	V	
V_{IN} Operating Voltage Range	0		22	V	
Supply Current		10	15	µA	
V_{IN} Rising Threshold, V_{TH_RISING}	0.56	0.6	0.64	V	V_{CC} = 3.3 V
V_{IN} Falling Threshold, $V_{TH\_FALLING}$	0.545	0.585	0.625	V	V_{CC} = 3.3 V
V_{IN} Hysteresis		15		mV	

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AAEON Technology INC.

Title: RSMEST# Control		
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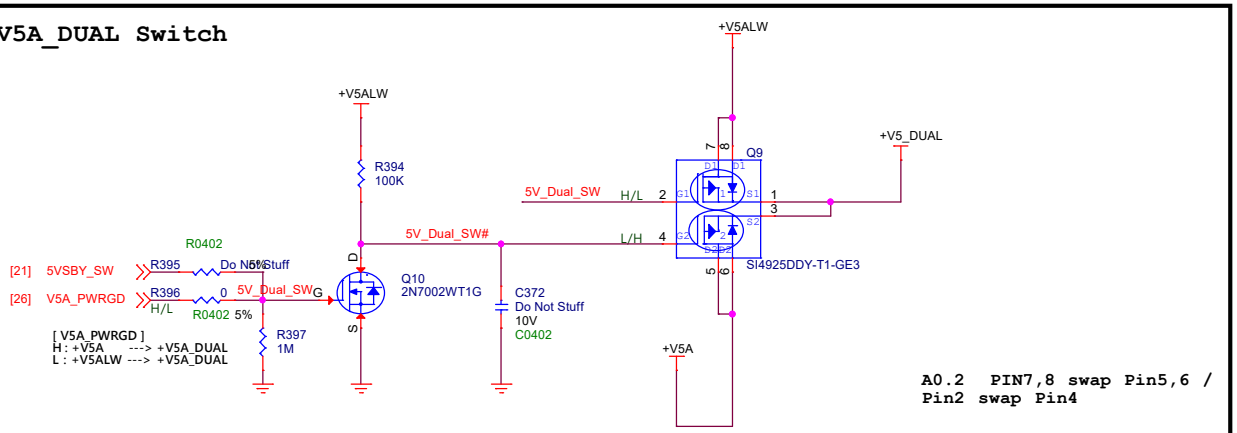
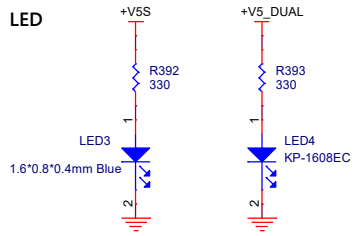
V5A_DUAL Switch

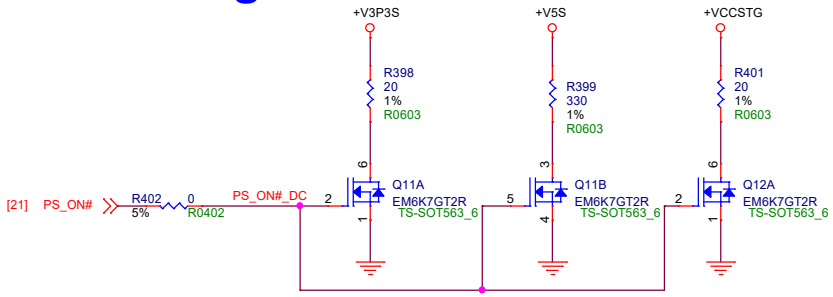


A0.2 PIN7,8 swap Pin5,6 / Pin2 swap Pin4

LED



Discharge Circuit



M1
material
Do Not Stuff

WHU

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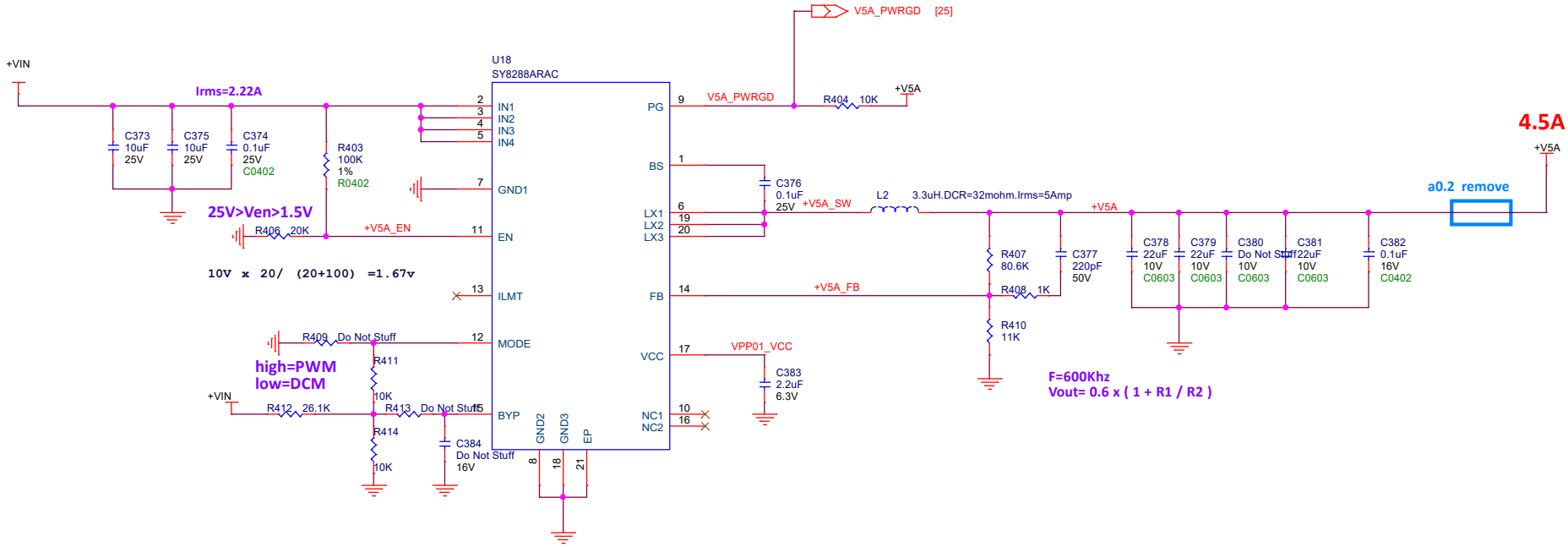
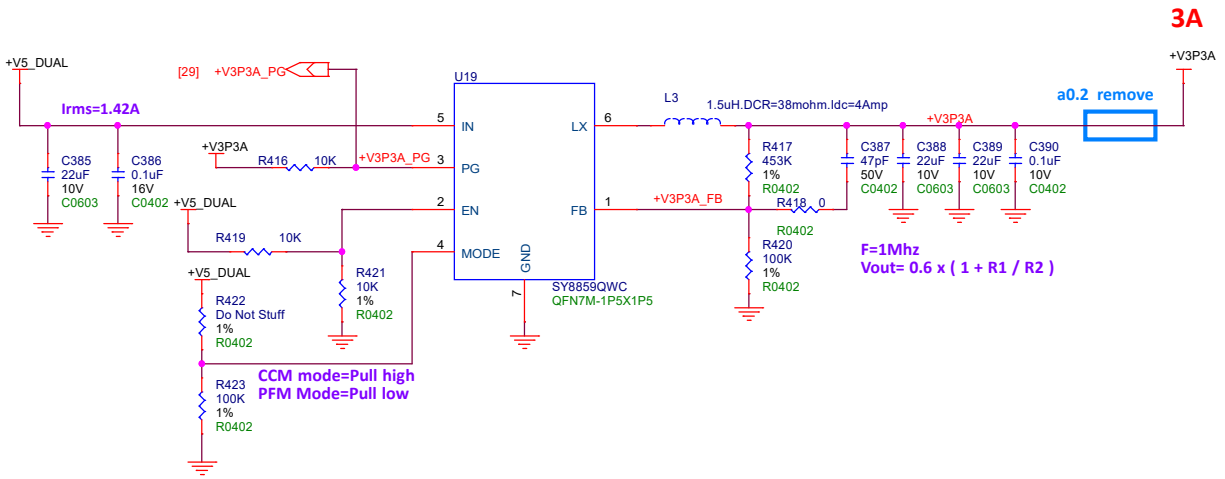
+V5A



+V3P3A



WHU

AAEON Technology INC.

Title: PWR_+V5A/ +V3P3A		
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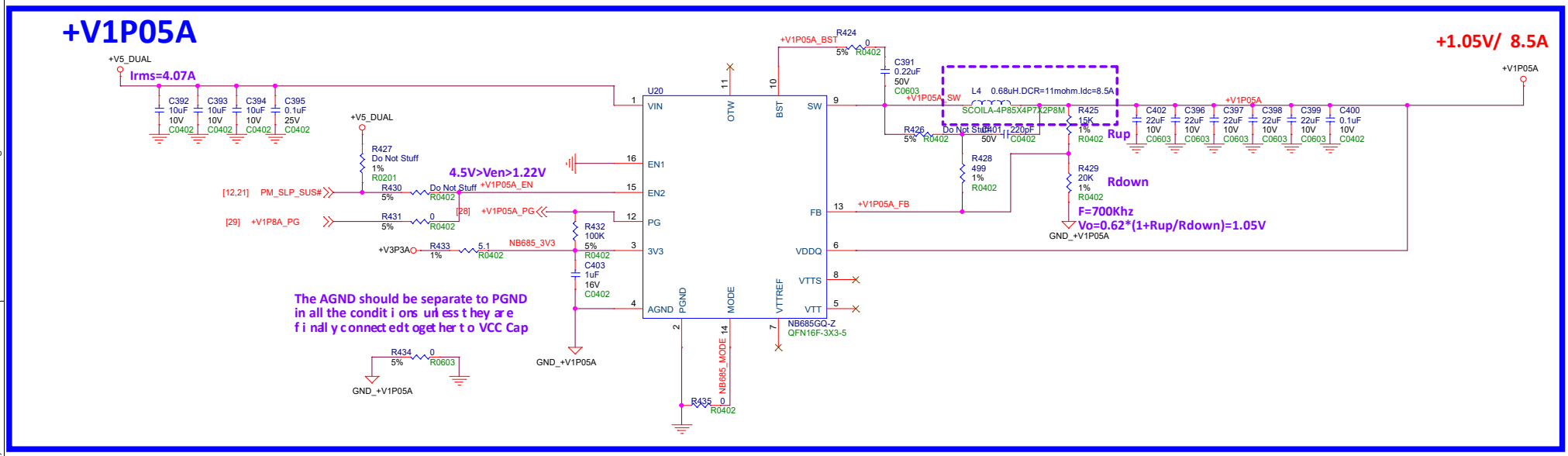

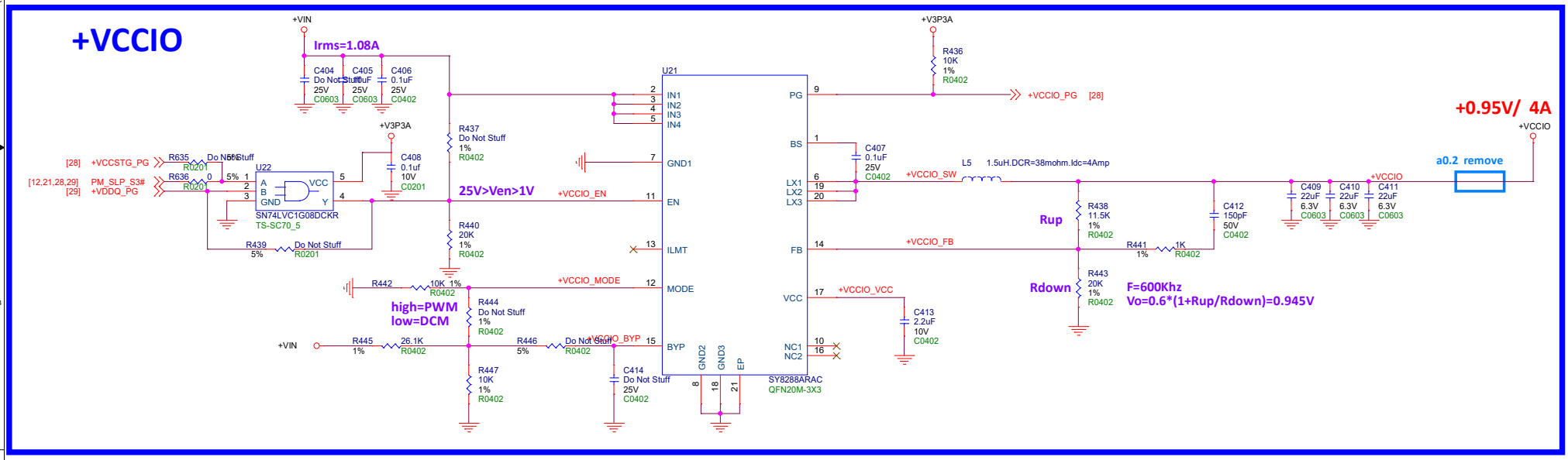

*Spec: It is strongly recommended that the SLP_S3# be a qualifying input signal to ALL_SYS_PWRGD logic, which drives IMVP VR_ON inputs. Additionally, it is recommended that SLP_S3# also qualify the EN control to the VCCIO power supply

WHU

AAEON Technology INC.

Title	PWR_+V1P05A/ +VCCIO	
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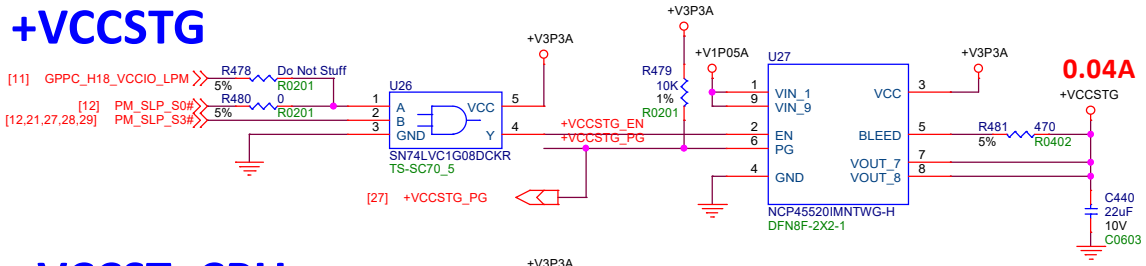
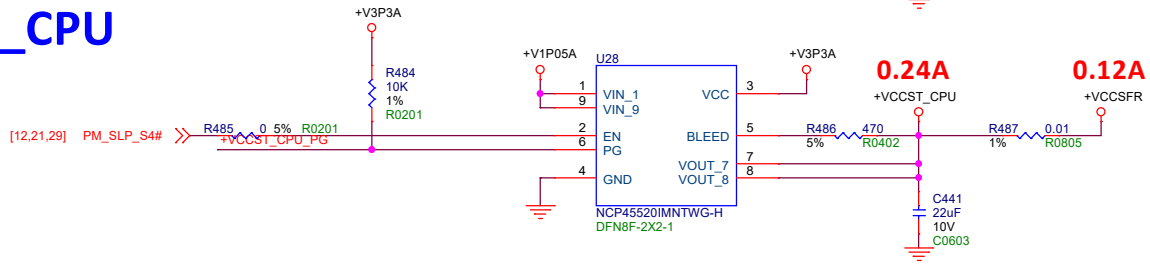
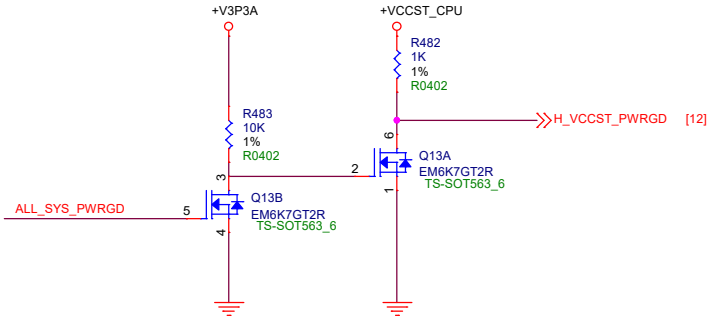
+VCCSTG

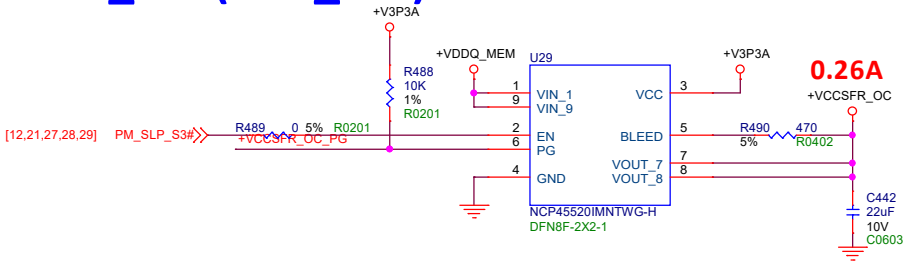


+VCCST_CPU

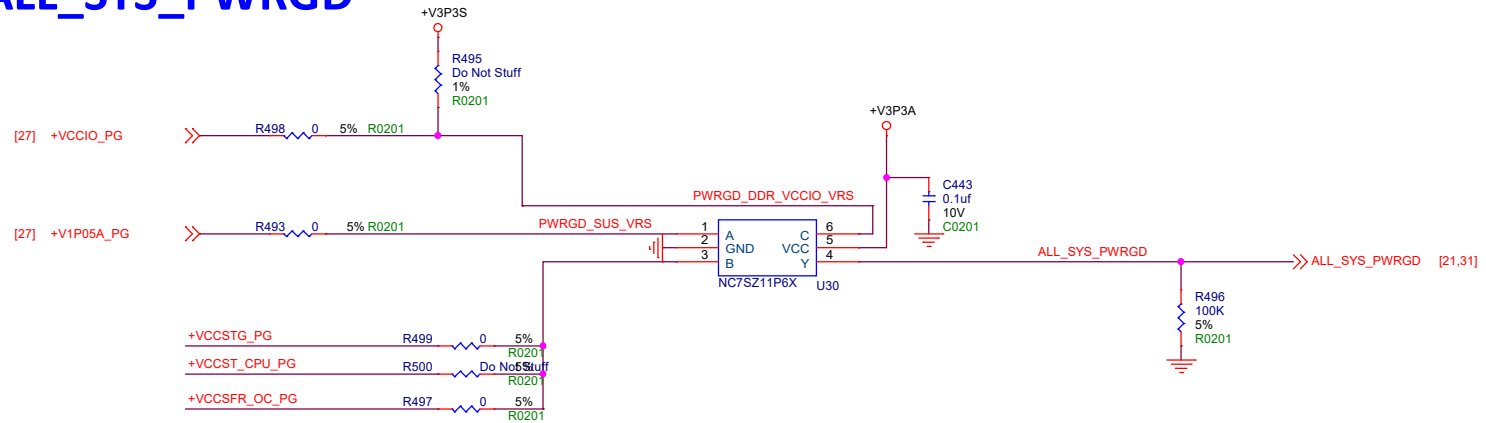




+VCCSFR_OC (VCC_PLL)



ALL_SYS_PWRGD



WHU

AAEON Technology INC.

Title: PWR_+VCCSTG/+VCCSFR_OC		
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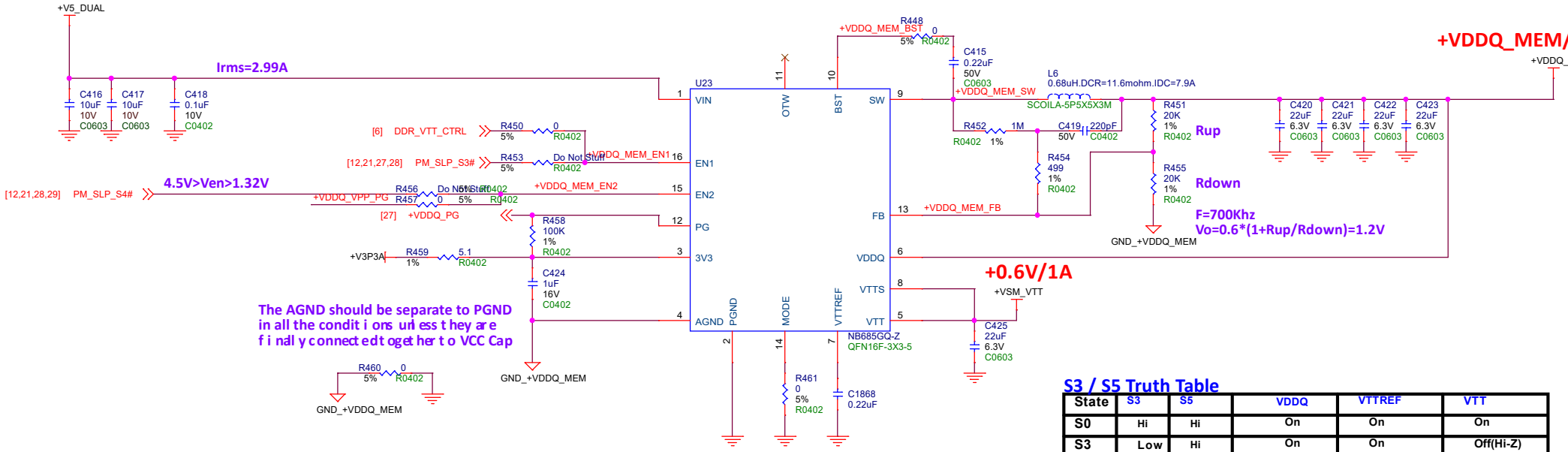
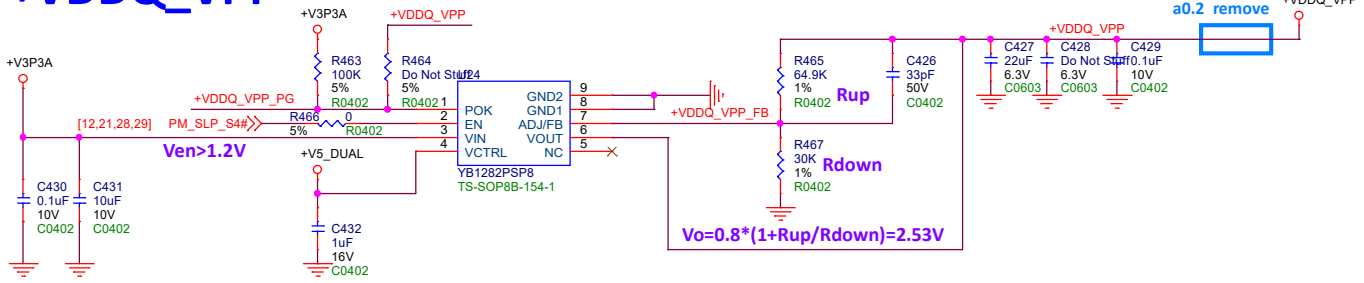
+VDDQ_MEM



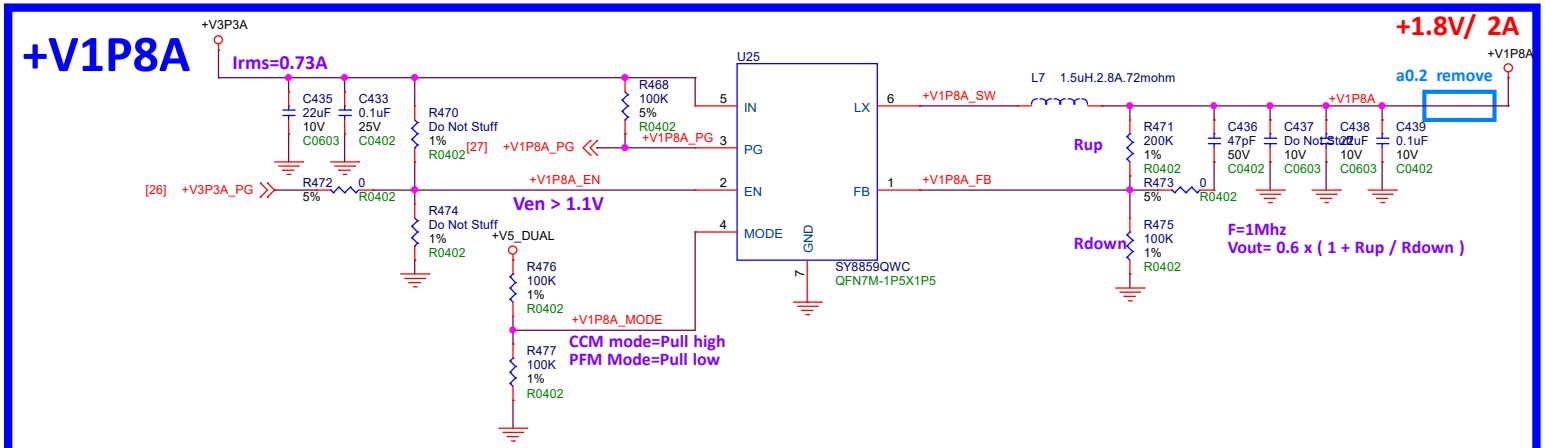
S3 / S5 Truth Table

State	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Low	Hi	On	On	Off(Hi-Z)
S4/S5	Low	Low	Off(Discharge)	Off(Discharge)	Off(Discharge)

+VDDQ_VPP



+V1P8A



WHU

AAEON Technology INC.

Title	PWR_+VDDQ/ +VDDQ_VPP/ +V1P8A		
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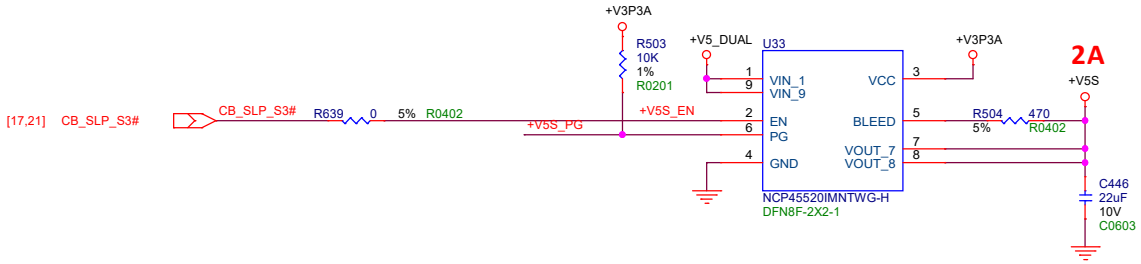
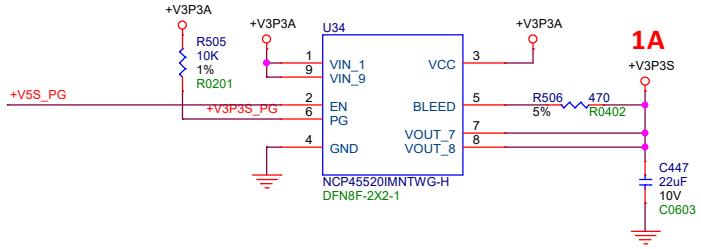
+V5S



+V3P3S



WHU

AAEON Technology INC.

Title: PWR_+V12S/ +V5S/ +V3P3S		
Size: Custom	Document Number: NANOCOM-WHU	Rev: A0.3_0_0
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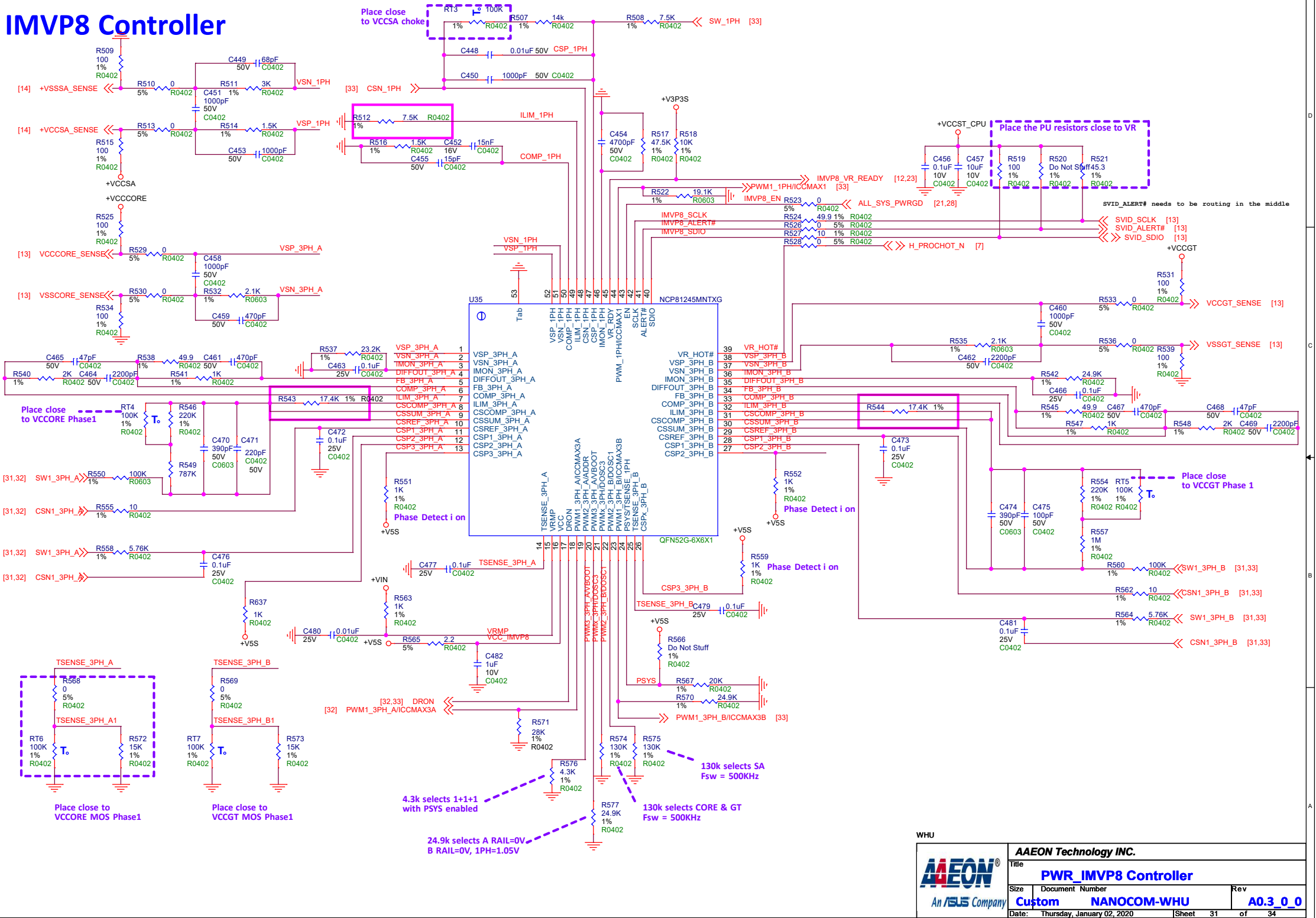
IMVP8 Controller



WHU

AAEON Technology INC.

Title	PWR_IMVP8 Controller	
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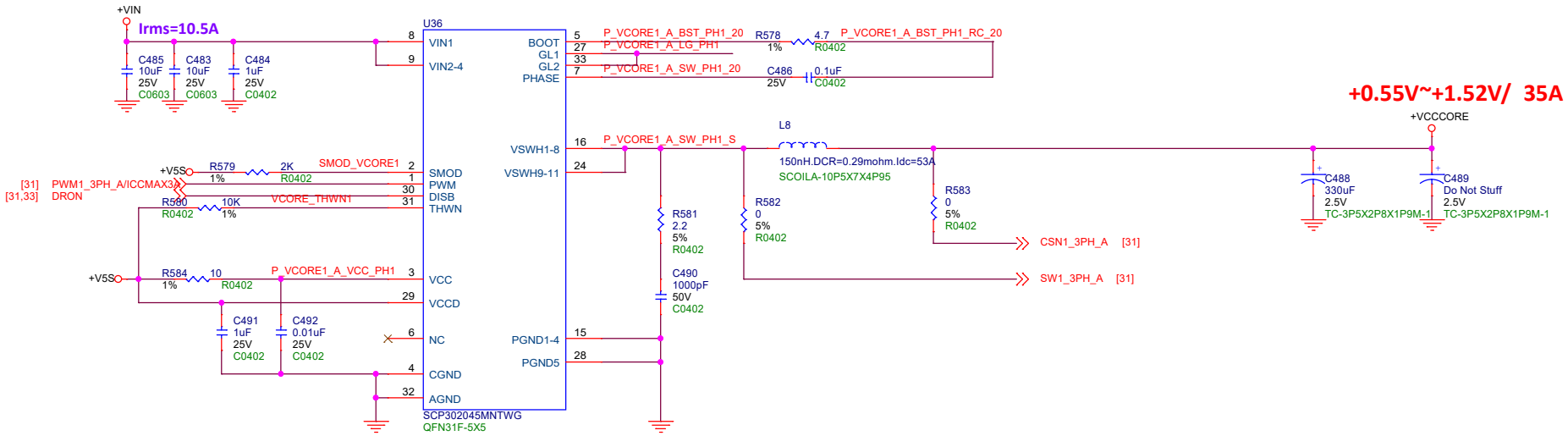
+VCCCORE



WHU

AAEON Technology INC.

Title: PWR_+VCCCORE		
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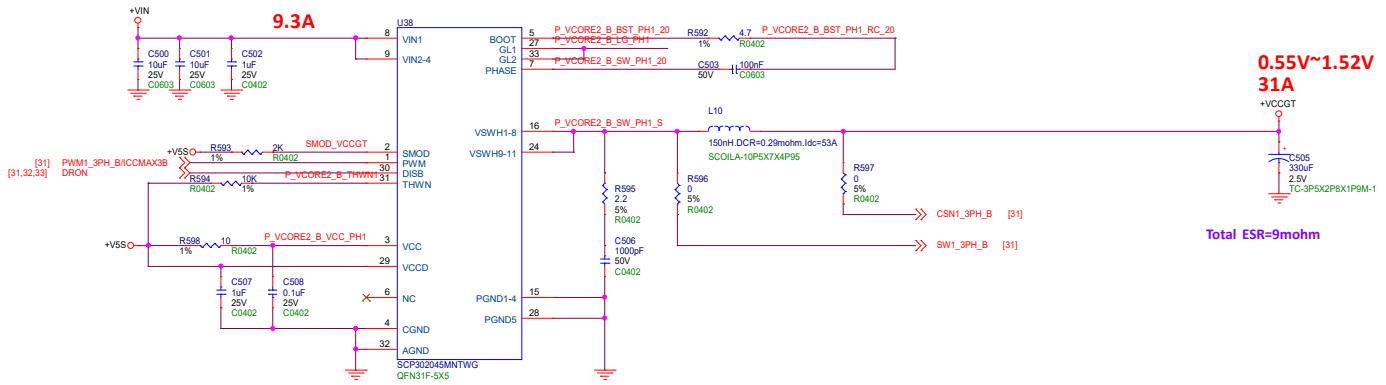
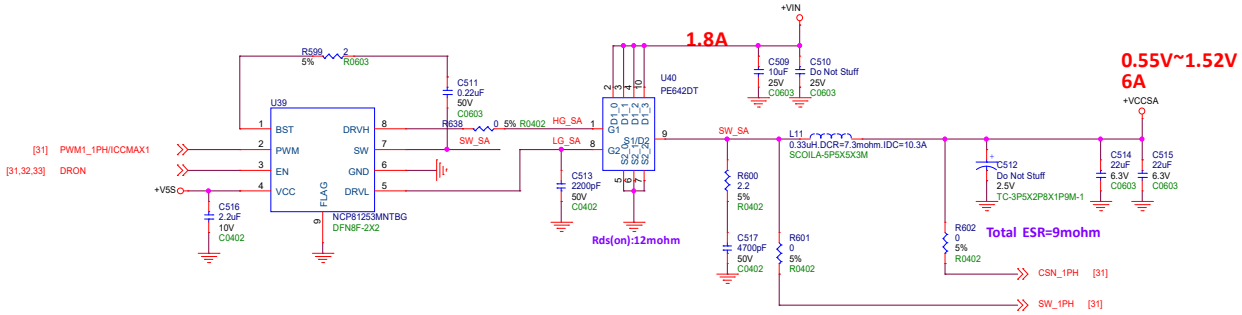
+VCCGT



+VCCSA



WHU

AAEON Technology INC.

Title	+VCCCORE/+VCCGT/+VCCSA	
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HISTORY

Date	Revision	Page	Modification list	Reason
2019/4/XX	A0.1_0_0	1-32	First Release	First Release
2019/6/18	A0.2_0_0	25-32	Unmount C437 for cost down. Unmount R422 for Frequency adjust. Unmount C380 for cost down. Unmount C404 for cost down. Unmount R444 for Frequency adjust.Mount R442 for Frequency adjust. Monut C500 for Vin adjust Change R544 from 12kohm to 17.4kohm(1050517424) for OCP adjust. Monut C483 for Vin adjust. Unmount C489 for cost down. Change R543 from 10kohm to 17.4kohm(1050517424) for OCP adjust. Change R512 from 16kohm to 7.5kohm(1050507524) for OCP adjust. ADD R2617 8.2K for PWRBTN# sequence	For power test and request
2019/7/23 2019/8/6 2019/9/24	A0.2_0_0		Mount R212, un-mount R213 Change DIO signal to EC from chipset ADD EMMC U41 schematice ADD R2654 For EC ver:CSKUAE21 SCI#,SMI# remove diode and change to 0 ohm(R2652,R2653) Add Q16 for BIOS	
2019/12/25	A0.3_0_0		Add Board ID circuit	

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