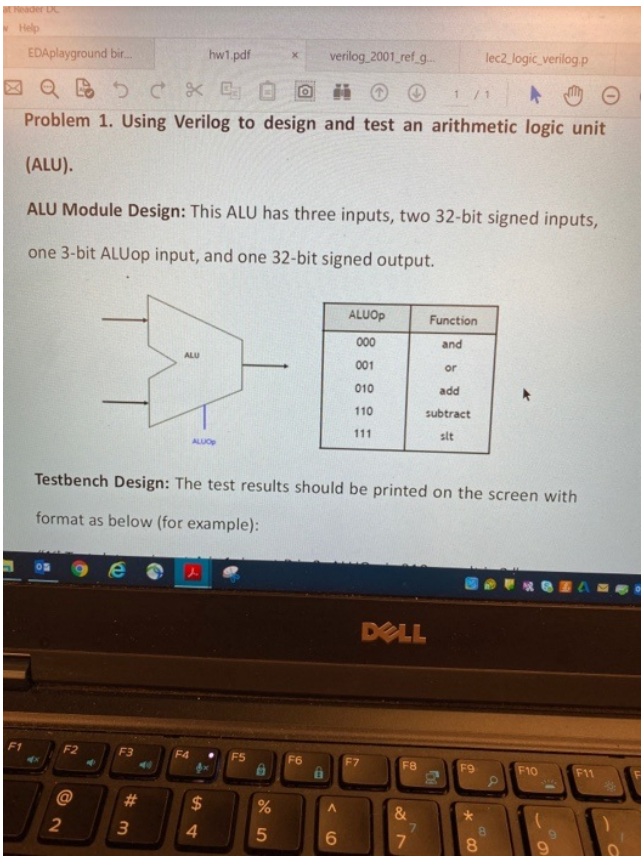
Question: At Reader DC Help verilog 2001 ref g.. lec2 logic verilog.p hw



Show transcribed image text

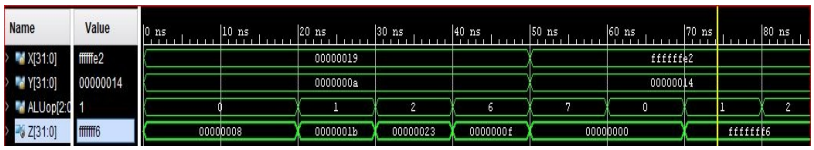
Expert Answer

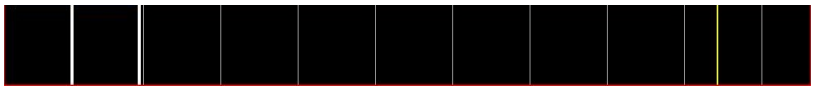
Anonymous answered this
341 answers

Was this answer helpful?

```
//ALU  module design code
module ALU(
    input [31:0] X,Y,
    input [2:0] ALUop,
    output reg [31:0] Z
    );
    always@(X,Y,ALUop)
    begin
    case(ALUop)
    3'b000:Z=X&Y;
    3'b001:Z=X|Y;
    3'b010:Z=X+Y;
    3'b110:Z=X-Y;
    3'b111: begin
    if(X<Y)
    Z=32'hffffffff;
    else
    Z=32'h00000000;
    end
    default:Z=Z;//no operation performed
    endcase
    end
endmodule
```

```
//testbench design code
module ALU_test();
reg signed [31:0] X,Y;
reg [2:0] ALUop;
wire signed [31:0] Z;
ALU p1(X,Y,ALUop,Z);
initial
begin
X=25;Y=10;ALUop=3'b000;
#10 ALUop=3'b000;
#10 ALUop=3'b001;
#10 ALUop=3'b010;
#10 ALUop=3'b110;
#10 ALUop=3'b111;
 X=-30;Y=20;
#10 ALUop=3'b000;
 #10 ALUop=3'b001;
 #10 ALUop=3'b010;
 #10 ALUop=3'b110;
 #10 ALUop=3'b111;
X=10;Y=20;
#10 ALUop=3'b000;
#10 ALUop=3'b001;
#10 ALUop=3'b010;
#10 ALUop=3'b010;
end   endmodule
```





Comment

Your answer

Add your answer

ABOUT CHEGG

LEGAL & POLICIES

CHEGG PRODUCTS AND SERVICES

CHEGG NETWORK

CUSTOMER SERVICE