Pack

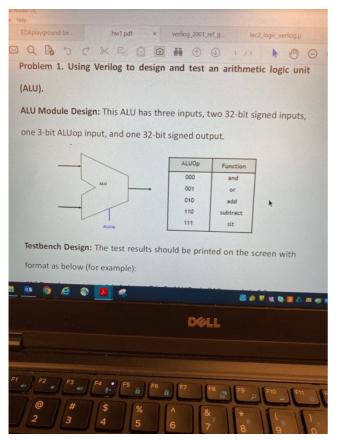
Find solutions for your homework or get textbooks



 $home \ / \ study \ / \ engineering \ / \ electrical \ engineering \ / \ electrical \ engineering \ questions \ and \ answers \ / \ at \ reader \ dc \ help \ verilog \ 2001 \ ref \ g... \ lec \ 2 \ l... \ lec \ 3 \ l... \ lec \ 4 \ l... \ lec$ 

## Question: At Reader DC Help verilog 2001 ref g.. lec2 logic verilog.p hw





Show transcribed image text

## **Expert Answer**

Anonymous answered this

Was this answer helpful?

```
//testbench design code
                                               module ALU test();
                                               reg signed [31:0] X,Y;
                                               reg [2:0] ALUop;
module ALU(
                                               wire signed [31:0] Z;
   input [31:0] X,Y,
                                               ALU pl(X,Y,ALUop,Z);
   input [2:0] ALUop,
                                               initial
   output reg [31:0] Z
                                               begin
                                               X=25;Y=10;ALUop=3'b000;
   always@(X,Y,ALUop)
                                               #10 ALUop=3'b000;
   begin
                                               #10 ALUop=3'b001;
   case (ALUop)
                                               #10 ALUop=3'b010;
   3'b000: Z=X&Y:
                                               #10 ALUop=3'b110;
   3'b001:Z=X|Y;
                                               #10 ALUop=3'b111;
   3'b010:Z=X+Y;
                                                X=-30;Y=20;
   3'b110:Z=X-Y;
                                               #10 ALUop=3'b000;
   3'blll: begin
                                                #10 ALUop=3'b001;
   if (X<Y)
                                                #10 ALUop=3'b010;
   Z=32'hffffffff;
                                                #10 ALUop=3'b110;
                                                #10 ALUop=3'b111;
   Z=32'h000000000;
                                               X=10;Y=20;
                                               #10 ALUop=3'b000;
   end
                                               #10 ALUop=3'b001;
   default: Z=Z; //no operation performed
   endcase
                                               #10 ALUop=3'b010;
   end
                                               #10 ALUop=3'b010;
endmodule
                                                    endmodule
```

Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns	60 ns	70 ns	liii	80 ns
> 🛂 X[31:0]	fffffe2			00000019				ffffff	e2		
¥ Y[31:0]	00000014			0000000a				000000	14		
ALUop[2:0	1		0	1	2	6	7	0		1	2
₹ Z[31:0]	ffffff6	0000	0008	0000001Р	00000023	0000000f	0000	0000		ffffff	£6



Comment >

## Your answer

Add your answer

ABOUT CHEGG	~
LEGAL & POLICIES	~
CHEGG PRODUCTS AND SERVICES	~
CHEGG NETWORK	~
CUSTOMER SERVICE	~

© 2003-2020 Chegg Inc. All rights reserved.