Technical Document

28/02/2016

Title: LOKA SOM MCU connectivity

Table 1 – MCU pins connections in the LOKA board.

MCU pin	Schematics signal	MCU direction	Polarity	Connected chipset	Connected chipset pin	Description
PJ.2	3V3_EN	OUT	HIGH	TPS63021	EN (pin 12)	3.3 V power supply enable. Active high.
P4.1	SPI_MOSI	OUT	HIGH	LIS3DE CC1125 ESP8266	SDI (pin 6) SI (pin 7) MTCK (pin 12)	Shared SPI bus Master Out, Slave In. Serial data from the MCU to the connected chipsets. Active high.
P4.2	SPI_MISO	IN	HIGH	LIS3DE CC1125 ESP8266	SDO (pin 7) SO (pin 9) MTDI (pin 10)	Shared SPI bus Master In, Slave Out. Serial data from the MCU to the connected chipsets. Active high.
P4.3	SPI_SCLK	OUT	HIGH	LIS3DE CC1125 ESP8266	SCL (pin 4) SCLK (pin 8) MTMS (pin 9)	Shared SPI bus clock. Sampling clock from the MCU to the connected chipsets. Active high.
P1.1	BUTTON	IN	HIGH			Tactile button output, connected to interrupt capable MCU pin. Active high.
P1.2	HALL	IN	HIGH	SM353LT	OUT (pin 3)	Hall effect sensor output, connected to interrupt capable MCU pin. Active high.
P4.0	LED	OUT	HIGH			LED indicator. Active high.
P6.5	ACC_CSN [(1)]	OUT	LOW	LIS3DE	CS (pin 8)	Accelerometer shared SPI bus chip enable. Active low.
P1.3	ACC	IN	HIGH	LIS3DE	INT1 (pin 11)	Accelerometer interrupt output, connected to interrupt capable MCU pin
P6.0	RADIO_EN	OUT	LOW			Radio power switch enable. Active low.
P6.4	RADIO_RSTN	OUT	LOW	CC1125	RESET_N (pin 2)	Radio transceiver reset. Active low.
P6.1	RADIO_CSN [(1)]	OUT	LOW	CC1125	CSN (pin 11)	Radio transceiver shared SPI bus chip enable. Active low.
P6.2	RADIO_GPIO00	IN	HIGH	CC1125	GPIO0 (pin 10)	Radio transceiver GPIO0. Active high.
P1.0	RADIO_GPIO2	IN	HIGH	CC1125	GPIO2 (pin 4)	Radio transceiver GPIO2. Active high.
P6.3	RADIO_GPIO3	IN	HIGH	CC1125	GPIO3 (pin 3)	Radio transceiver GPIO3. Active high.
P4.5	RADIO_LNA_EN	OUT	HIGH	CC1190	LNA_EN (pin7)	Radio front-end LNA enable. Active high.
P4.6	RADIO_PA_EN	OUT	HIGH	CC1190	PA_EN (pin 8)	Radio front-end PA enable. Active high.
P4.4	WIFI_EN	OUT	LOW			WIFI power switch enable. Active low.

P3.0	WIFI_RSTN	OUT	LOW	ESP8266	EXT_RSTB (pin 32)	WIFI transceiver reset. Active low.
P3.1	WIFI_CSN (1)	OUT	LOW	ESP8266	MTDO (pin 13)	WIFI transceiver shared SPI bus chip enable. Active low.
P1.4	WIFI_INT0	IN	HIGH	ESP8266	GPIO0 (pin 15)	WIFI transceiver status flag 0. Active high.
P1.5	WIFI_INT2	IN	HIGH	ESP8266	GPIO2 (pin 14)	WIFI transceiver status flag 2. Active high.
P5.0	IO0_A0	IN/OUT				
P5.1	IO1_A1	IN/OUT				
P1.6	IO2	IN/OUT				
P1.7	IO3	IN/OUT				
P3.2	IO4_CSN	IN/OUT				
P3.3	IO6_MOSI_TX	IN/OUT				
P3.4	IO5_MISO_RX	IN/OUT				
P2.7	IO7_SCLK	IN/OUT				

(1) CAUTION: Ensure those pins are never simultaneously asserted.