2EL6020 – Computer Architecture

Instructors: Ruben Salvador Perea
Department: CAMPUS DE RENNES
Language of instruction: ANGLAIS
Campus: CAMPUS DE RENNES
Workload (HEE): 60
On-site hours (HPE): 35,00
Elective Category : Fundamental Sciences
Advanced level : Yes

Description

This elective course is open to any interested student while it is also mandatory for the InfoSec track.

Microprocessors are omnipresent in today's society. However, their design, implementation and construction remain a challenge that have a major impact on the performance and overall security of computing systems.

The main objective of this course is to give students all necessary basic knowledge to understand how modern processors work. We will lay out the fundamental concepts and techniques in computer architecture, with a focus on the hardware/software interface and a bottom-up approach to understand how computers work and how they can actually be designed.

This course is largely inspired by Patterson and Hennessy's book "Computer Organization and Design, The Hardware/Software interface, RISC-V Edition, Morgan Kaufmann, 2018", and it will be used as the main book for the course. Both did pioneering work on computer architecture, specifically in "Reduced Instruction Set Computer" (RISC) architectures. David Patterson coined the term RISC, while John L. Hennessy was the inventor of the MIPS microprocessor. Both won the 2017 Turing Award for their work in RISC architectures.

Quarter number

SG6

Prerequisites (in terms of CS courses)

This course builds on fundamental concepts from:
- 1CC1000 – Information systems and programming
- 1EL8000 – Electronic Systems (particularly important is the "digital electronics" part)

Certain notions on algorithms & complexity fundamentals are also interesting.

Syllabus

Digital circuit design using a Hardware Description Language (HDL) (4.5h lectures + 6h tutorials)

- Combinational logic circuits design
- Sequential logic circuits design, Finite State Machines (FSM), análisis temporal
- Reconfigurable circuits: the Field-Programmable Gate Array (FPGA)
- HDL design flow for FPGAs (HDL description, simulation, synthesis)

Computer architecture and RISC-V (10.5h lectures + 12h labs)

- The Von Neumann model of computer architectures
- RISC/CISC architecture paradigms
- RISC-V instruction set architecture (ISA), addressing modes
- Processor components: datapath, register file, arithmetic logic unit (ALU), control unit, memory, peripherals
- Interrupts and exceptions
- Performance: pipeline, memory hierarchy and caches, branch prediction, out-of-order execution
- Notions on processor architecture security

Tutorials and Labs

- VHDL design flow for FPGAs
- RISC-V assembly programming
- VHDL design of (a subpart of) a RISC-V processor

Class components (lecture, labs, etc.)

Lectures : 15h
Tutorials : 6h
Labs : 12h

Grading

Final exam (written or oral): 40%
Lab exam (project technical realization, demonstration and oral defense): 40%
Course assignments (exercises, readings ...): 20%

Course support, bibliography

- **Slides** provided to students

- **Main books for the course**: The are some copies of these books at the library and they are also available from the school ebook platform at: https://www-vlebooks-com.ezproxy.universite-paris-saclay.fr/
    - D. A. Paterson, J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, RISC-V Edition, Morgan Kaufmann, 2018. [CA]
    - S. L. Harris, D. M. Harris, Digital Design and Computer Architecture (MIPS or ARM Edition), Morgan Kaufmann. [DDCA]

- **Other books**
    - W. J. Dally, R. C. Harting, T. M. Aamodt, Digital Design Using VHDL: A Systems Approach, First Edition, Cambridge University Press, 2016 [DD]
    - B. J. LaMeres, Introduction to Logic Circuits & Logic Design with VHDL, Second Edition, Springer, 2019 [DD]
    - M. M. Mano, C. R. Kime, T. Martin, Logic and Computer Design Fundamentals, Fifth edition, Pearson, 2015 [DDCA]
    - P. J. Ashenden, J. Lewis, The Designer's Guide to VHDL, Third Edition, Morgan Kaufmann, 2008 [DD]
- **Freely available PDFs**
    - B. Mealy, F. Tappero, Free Range VHDL : http://www.freerangefactory.org [DD]
    - P. J. Ashenden, The VHDL Cookbook : https://tams.informatik.uni-hamburg.de/vhdl/doc/cookbook/VHDL-Cookbook.pdf [DD]

Legend:
[CA] : Computer Architecture
[DD] : Digital Design
[DDCA] : Digital design and computer architecture

Resources
Teaching staff: Rubén Salvador, Guillaume Hiet, Amor Nafkha

- Maximum enrollment: 25
- Software, number of licenses required: Xilinx Vivado (25 licences)
- Board Xilinx Pynq-Z1
- Equipment-specific classrooms : Rennes Campus Level 5 lab rooms, 25 students

Learning outcomes covered on the course
At the completion of the course, students will be able to :

- explain the fundamental design principles of modern microprocessors architectures
- design some blocs of a simple microprocessor corresponding to the RISC-V instruction set architecture
- simulate and synthesize this microprocessor on an FPGA
- develop programs in assembly language using RISC-V instruction set

Description of the skills acquired at the end of the course

C1.4 - Design, detail and corroborate a whole or part of a complex system.