FAIRCHILD SEMICONDUCTOR®

January 2008

# 74F245
# Octal Bidirectional Transceiver with 3-STATE Outputs

## Features

- Non-inverting buffers
- Bidirectional data path
- A outputs sink 24mA
- B outputs sink 64mA

## General Description

The 74F245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24mA at the A Ports and 64mA at the B Ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A Ports to B Ports; Receive (active LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a High Z condition.

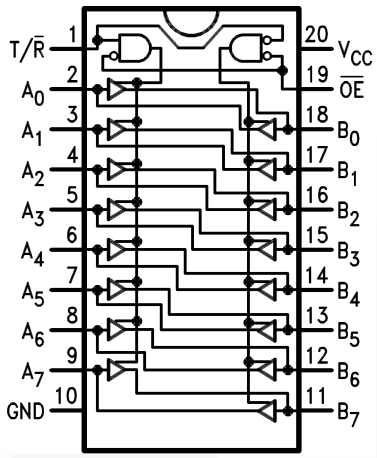
## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74F245SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74F245SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F245MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74F245MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74F245PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

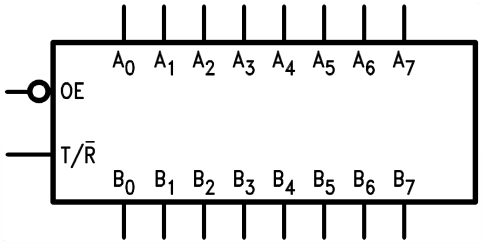
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

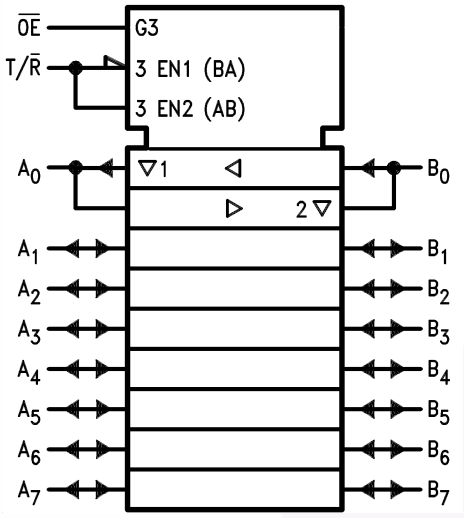
## Connection Diagram




## Logic Symbols




IEEE/IEC




## Truth Table

| Inputs | | Output |
|---|---|---|
| $\overline{OE}$ | T/$\overline{R}$ | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
|---|---|---|---|
| $\overline{OE}$ | Output Enable Input (Active LOW) | 1.0/2.0 | 20µA/–1.2mA |
| T/$\overline{R}$ | Transmit/Receive Input | 1.0/2.0 | 20µA/–1.2mA |
| $A_0$–$A_7$ | Side A Inputs or<br>3-STATE Outputs | 3.5/1.083<br>150/40 (38.3) | 70 µA/–0.65mA<br>–3 mA/24mA (20mA) |
| $B_0$–$B_7$ | Side B Inputs or<br>3-STATE Outputs | 3.5/1.083<br>600/106.6 (80) | 70µA/–0.65mA<br>–12mA/64mA (48mA) |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_{STG}$ | Storage Temperature | –65°C to +150°C |
| $T_A$ | Ambient Temperature Under Bias | –55°C to +125°C |
| $T_J$ | Junction Temperature Under Bias | –55°C to +150°C |
| $V_{CC}$ | $V_{CC}$ Pin Potential to Ground Pin | –0.5V to +7.0V |
| $V_I$ | Input Voltage(1) | –0.5V to +7.0V |
| $I_I$ | Input Current(1) | –30mA to +5.0mA |
| | Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | |
| | Standard Output | –0.5V to $V_{CC}$ |
| | 3-STATE Output | –0.5V to +5.5V |
| | Current Applied to Output in LOW State (Max.) | twice the rated $I_{OL}$ (mA) |
| | ESD Last Passing Voltage (Min.) | 4000V |

**Note:**

1. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_A$ | Free Air Ambient Temperature | 0°C to +70°C |
| $V_{CC}$ | Supply Voltage | +4.5V to +5.5V |

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CC}$ | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | | Recognized as a HIGH Signal | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | Recognized as a LOW Signal | | | 0.8 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | | Min. | $I_{IN}$ = –18mA | | | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | 10% $V_{CC}$ | Min. | $I_{OH}$ = –3mA ($A_n$) | 2.4 | | | V |
| | | 10% $V_{CC}$ | | $I_{OH}$ = –15mA ($B_n$) | 2.0 | | | |
| | | 5% $V_{CC}$ | | $I_{OH}$ = –3mA ($A_n$) | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | 10% $V_{CC}$ | Min. | $I_{OL}$ = 24mA ($A_n$) | | | 0.5 | V |
| | | 10% $V_{CC}$ | | $I_{OL}$ = 64mA ($B_n$) | | | 0.55 | |
| $I_{IH}$ | Input HIGH Current | | Max. | $V_{IN}$ = 2.7V | | | 5.0 | µA |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | Max. | $V_{IN}$ = 7.0V ($\overline{OE}$, T/$\overline{R}$) | | | 7.0 | µA |
| $I_{BVIT}$ | Input HIGH Current Breakdown (I/O) | | Max. | $V_{IN}$ = 5.5V ($A_n$, $B_n$) | | | 0.5 | mA |
| $I_{CEX}$ | Output HIGH Leakage Current | | Max. | $V_{OUT}$ = $V_{CC}$ ($A_n$, $B_n$) | | | 50 | µA |
| $V_{ID}$ | Input Leakage Test | | 0.0 | $I_{ID}$ = 1.9µA, All Other Pins Grounded | 4.75 | | | V |
| $I_{OD}$ | Output Leakage Circuit Current | | 0.0 | $V_{IOD}$ = 150mV, All Other Pins Grounded | | | 3.75 | µA |
| $I_{IL}$ | Input LOW Current | | Max. | $V_{IN}$ = 0.5V (T/$\overline{R}$, $\overline{OE}$) | | | –1.2 | mA |
| $I_{IH}$ + $I_{OZH}$ | Output Leakage Current | | Max. | $V_{OUT}$ = 2.7V ($A_n$, $B_n$) | | | 70 | µA |
| $I_{IL}$ + $I_{OZL}$ | Output Leakage Current | | Max. | $V_{OUT}$ = 0.5V ($A_n$, $B_n$) | | | –650 | µA |
| $I_{OS}$ | Output Short-Circuit Current | | Max. | $V_{OUT}$ = 0V ($A_n$) | –60 | | –150 | mA |
| | | | | $V_{OUT}$ = 0V ($B_n$) | –100 | | –225 | |
| $I_{ZZ}$ | Bus Drainage Test | | 0.0V | $V_{OUT}$ = 5.25V($A_n$, $B_n$) | | | 500 | µA |
| $I_{CCH}$ | Power Supply Current | | Max. | $V_O$ = HIGH | | 70 | 90 | mA |
| $I_{CCL}$ | Power Supply Current | | Max. | $V_O$ = LOW | | 95 | 120 | mA |
| $I_{CCZ}$ | Power Supply Current | | Max. | $V_O$ = HIGH Z | | 85 | 110 | mA |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$ | | | $T_A = -55°C$ to $+125°C$, $C_L = 50pF$ | | $T_A = 0°C$ to $+70°C$, $C_L = 50pF$ | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, | 2.5 | 4.2 | 6.0 | 2.0 | 7.5 | 2.0 | 7.0 | ns |
| | $A_n$ to $B_n$ or $B_n$ to $A_n$ | 2.5 | 4.2 | 6.0 | 2.0 | 7.5 | 2.0 | 7.0 | |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time | 3.0 | 5.3 | 7.0 | 2.5 | 9.0 | 2.5 | 8.0 | ns |
| | | 3.5 | 6.0 | 8.0 | 3.0 | 10.0 | 3.0 | 9.0 | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time | 2.0 | 5.0 | 6.5 | 2.0 | 9.0 | 2.0 | 7.5 | ns |
| | | 2.0 | 5.0 | 6.5 | 2.0 | 10.0 | 2.0 | 7.5 | |

## Physical Dimensions

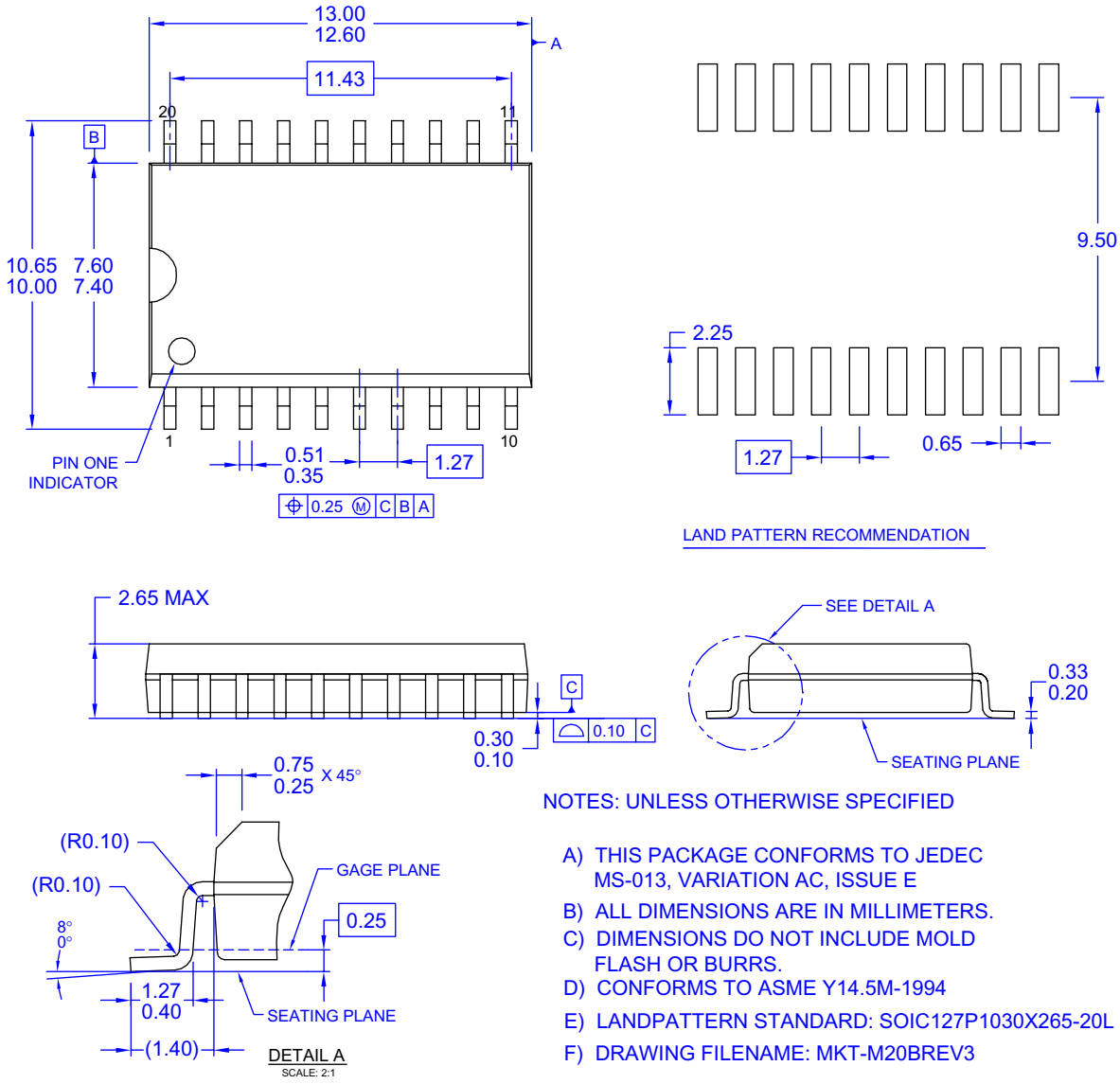



**Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

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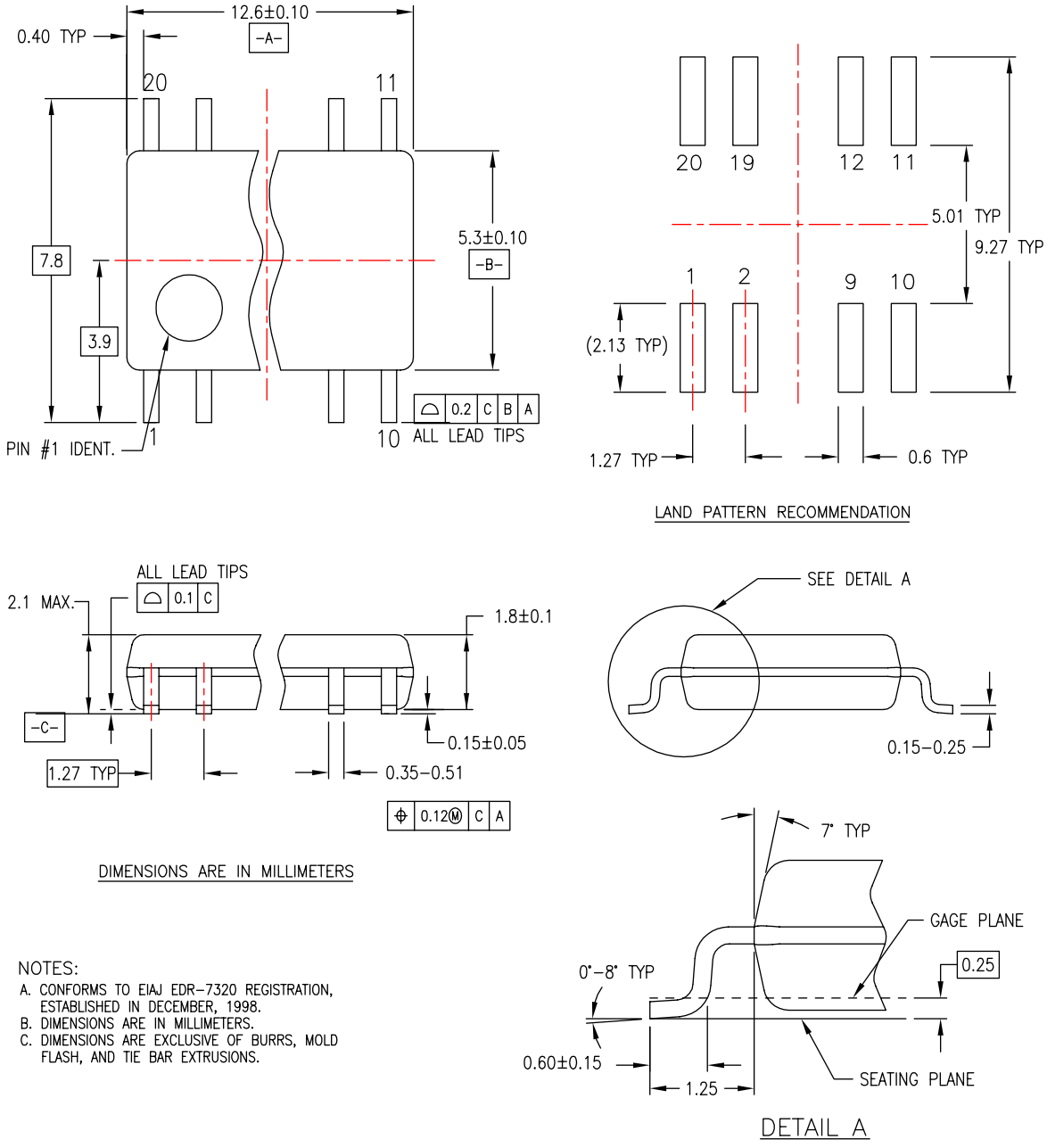
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

**Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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## Physical Dimensions (Continued)

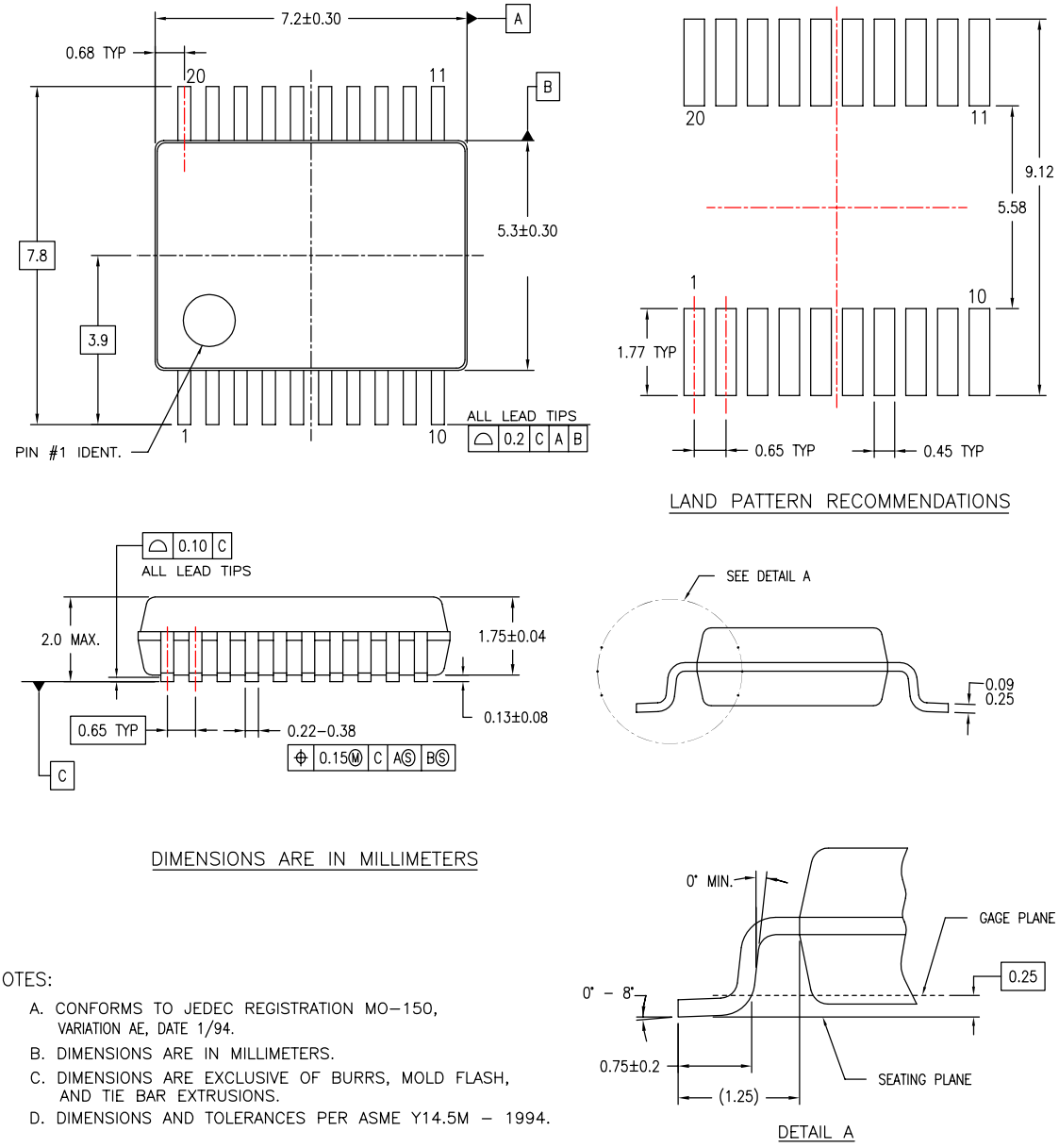


**Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**

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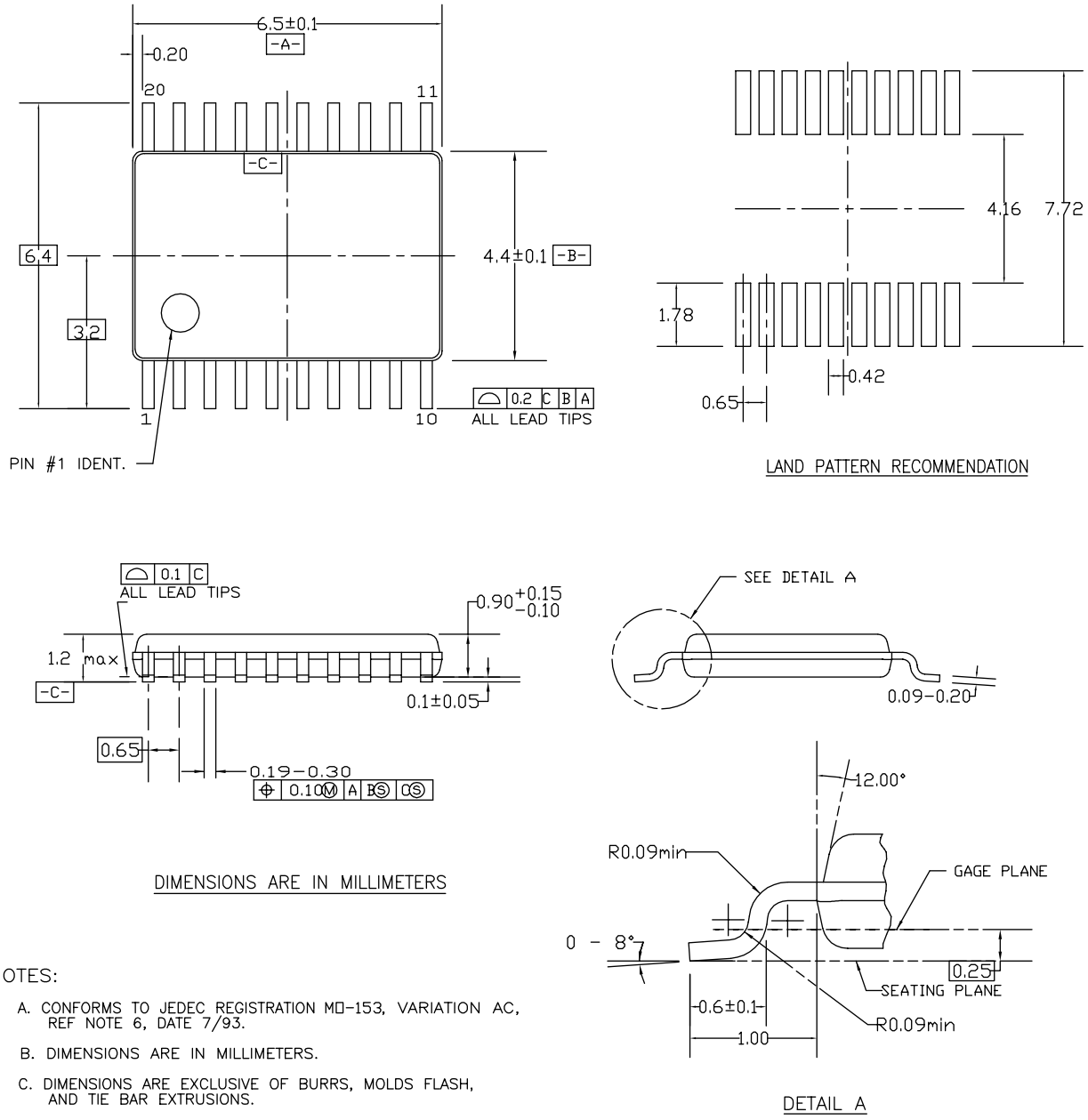
## Physical Dimensions (Continued)




DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

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D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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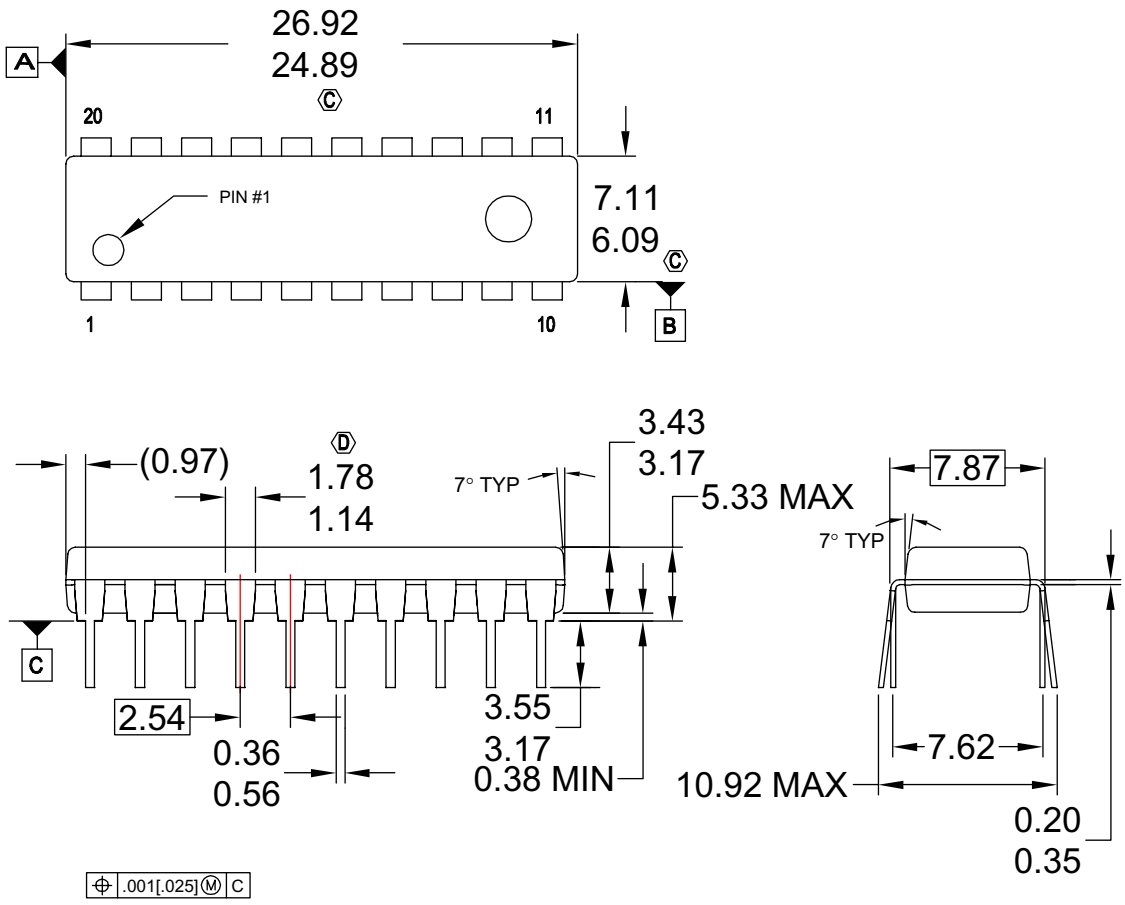
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.

B. ALL DIMENSIONS ARE IN MILLIMETERS

C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.

D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.

E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

F. DRAWING FILE NAME: N20AREV8

**Figure 5. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

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