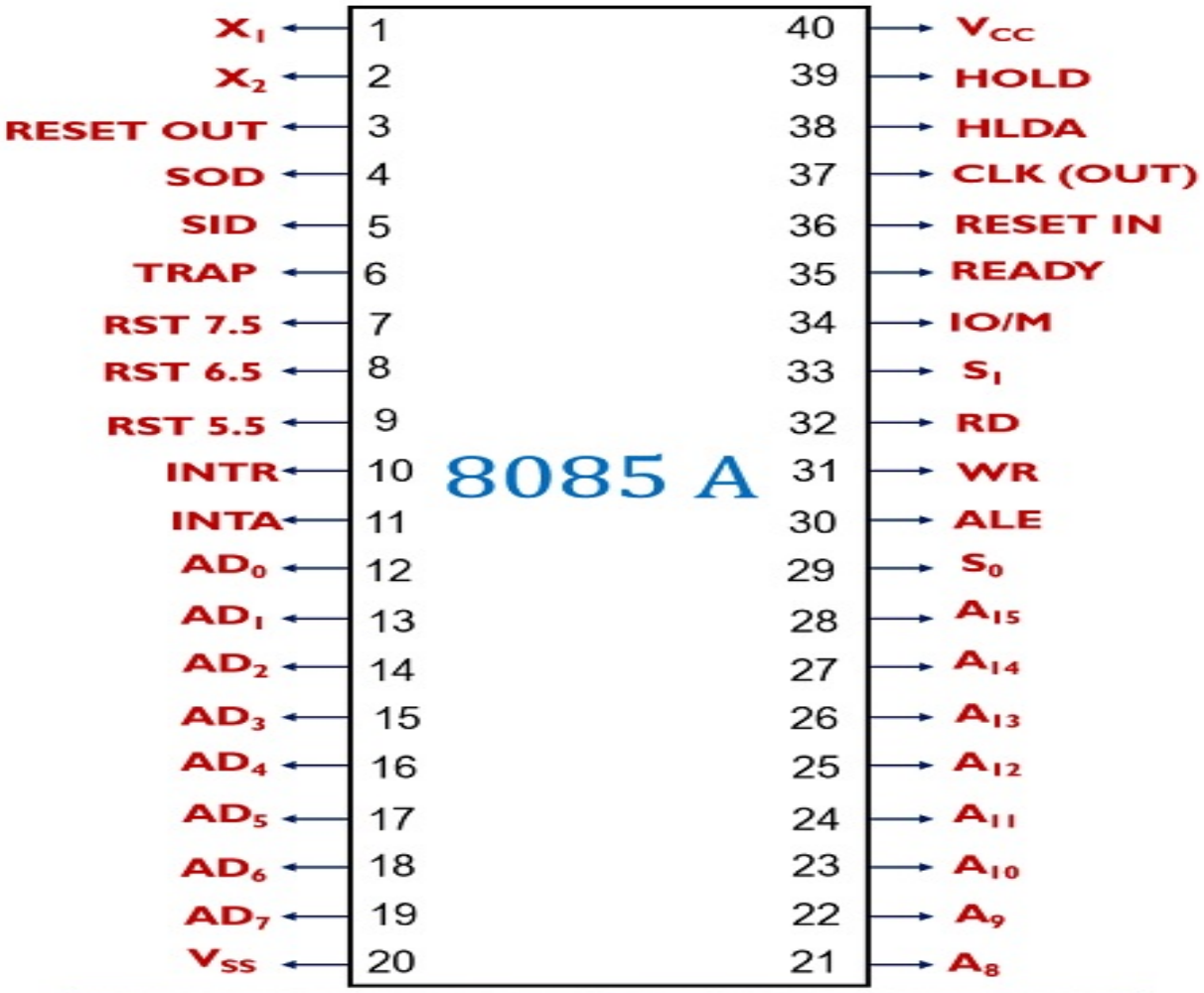
Microprocessor Lecture 3

8085 Microprocessor

Presented by: Robinhood Khadka

Pin Configuration of 8085



Pin diagram of 8085 Microprocessor

Electronics Desk

Pin Configuration of 8085

1. Address bus (A15-AD0)

   - 16 signal lines are used as address bus
   - However these lines are split into two segments: A15-A8 and AD7-AD0
   - A15-A8 are unidirectional and carries higher order address
   - AD7-AD0 are used for dual purpose

Pin Configuration of 8085

- Data Bus(AD7-AD0)

- They are bidirectional
- They are used as lower order address bus as well as data bus

- Control and Status signal

- The processor contains two control signals ($\overline{RD}$ and $\overline{WR}$) and three status signal(IO/$\overline{M}$, S1, S2)

- ALE: Address Latch Enable is a +ve signal that is generated every time when operation begins

- $\overline{RD}$(Read): when it is low, it indicates that selected I/O or memory device is to be read and data are available on data bus. It is active Low signal

Pin Configuration of 8085

- $\overline{WR}$(Write): When it is low, it indicates that the selected data on the data bus are ready to be written into the memory or I/O location

- IO/$\overline{M}$: When it is high it indicates the Input/output operation and when it is low it indicates memory related operation

- S0 & S1: Status 0 and Status 1 signals are used to identify various operation

S1	S0	Mode
0	0	HLT
0	1	WRITE
1	0	READ
1	1	OPCODE FETCH

Pin Configuration of 8085

- SOD & SID:

  Serial input data comes bit by bit into the microprocessor and goes out through the Serial Out data pin bit by bit

- Interrupts:
  a. TRAP : Highest priority interrupt. Non-Maskable
  b. RST 7.5,6.5,5.5: Maskable restart Interrupt
  c. INTR(Interrupt Request): General purpose interrupt
  d. $\overline{\text{INTA}}$(Int Ack):Active low signal used to acknowledge the interrupt

Pin Configuration of 8085

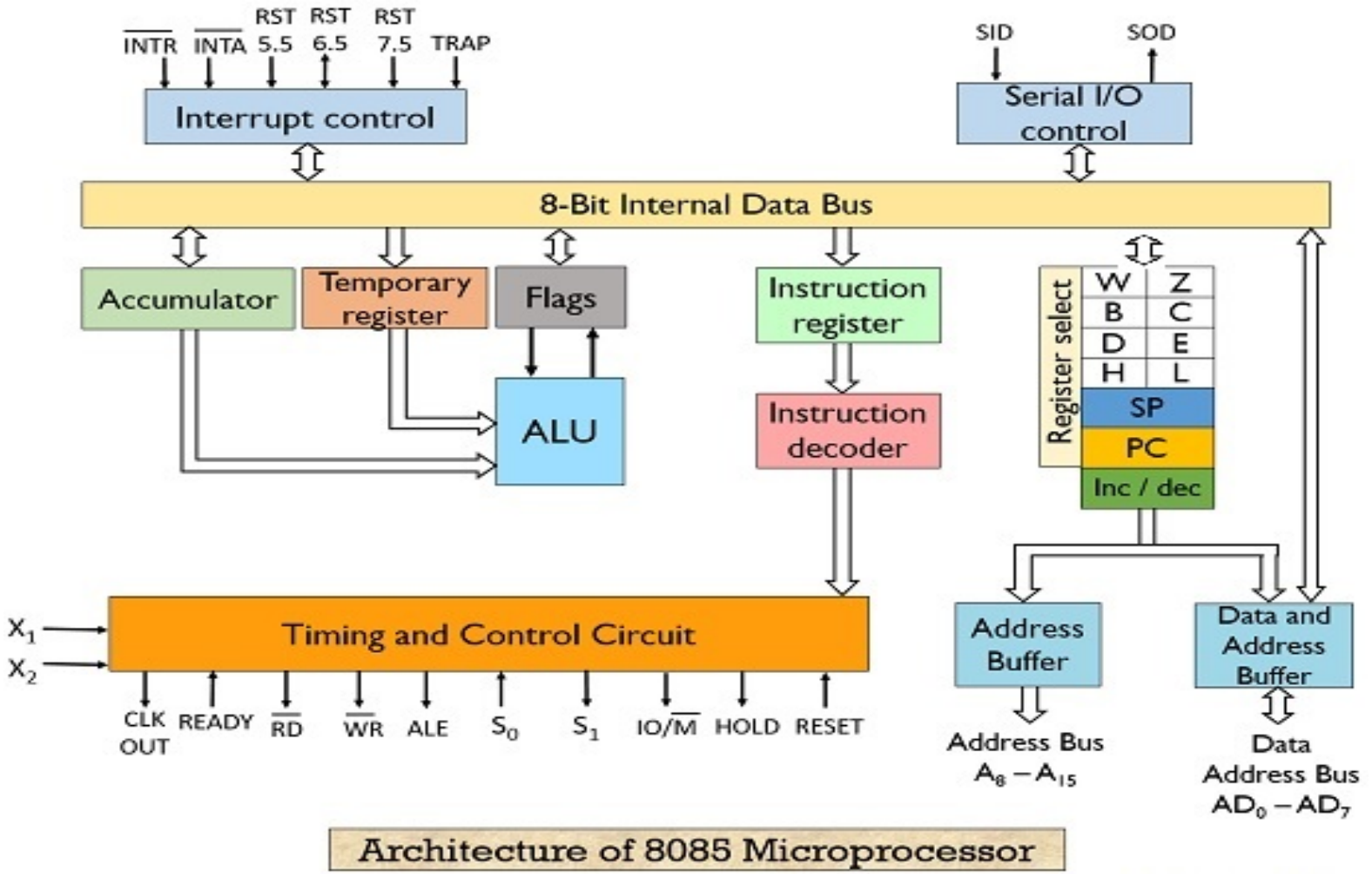
- Hold: This signal indicates that a peripheral device such as DMA is requesting the use of address and data bus

- HLDA(Hold ACK): It acknowledges the HOLD request
- READY: This signal is used to delay the µp Read or Write cycle until a slow responding peripheral is ready to send or accept data. When it goes low, µp waits until it goes high

- X1,X2: They are crystal oscillators that provides the frequency which are internally divided into two
- RESET OUT: It is a active high signal that resets the devices which are connected to the microprocessor

- $\overline{\text{RESET IN}}$: When the signal on this pin goes low, the program counter is set to zero and MPU is reset

8085 Architecture



8085 Architecture

1. Program Counter(16)
   - PC register is used to sequence the execution of instruction.
   - PC points to the memory address of next instruction
   - After fetching the instruction the PC is incremented by 1
2. Instruction Register(8)
   - Opcode (instruction) fetched is stored in this register before it is decoded and encoded.
   - It is not accessible to the programmer
3. Accumulator(8)
   - All arithmetic and logical operation make use of this register
   - The first data as well as the result of the last operation is stored in accumulator before being sent to different memory address
4. General Purpose Registers(8)
   - used to store the 8 bit data
   - It has 6 general purpose registers made available to the user. B,C,D,E,H,L which are all 8-bit in size but can be made in pairs to make room for 16-bit data as well.
   - The pairs are BC, DE, HL

8085 Architecture

5. Temporary Registers(8)

- Also used to store the data for brief amount of time
- They are not accessible to the user but are used internally
- W and Z are such registers

6. Stack Pointer(16)

- Holds the address in the memory when the registers are full
- It user PUSH and POP operation
- Follows LIFO order
- It always points to the address of the top of the stack

8085 Architecture

7. Flags and Flip-flops

- There are 5 flip-flops which are SET/RESET according to the result of the operation and are called FLAGS

I. Carry Flag: It is set (equals 1) when the accumulator contains larger than 8-bit

II. Zero Flag: It is set when the result of the last operation is zero

III. Sign Flag: It is set when the MSB of the result is 1 . If D7 is 1 the number is viewed as –ve number else if it is 0 it is considered +ve number

IV. Parity Flag: It is set when the number of 1's in the last operation is even

V. Auxiliary Carry(AC): It is set if a carry is generated from half word. That is from bit D3 to bit D5

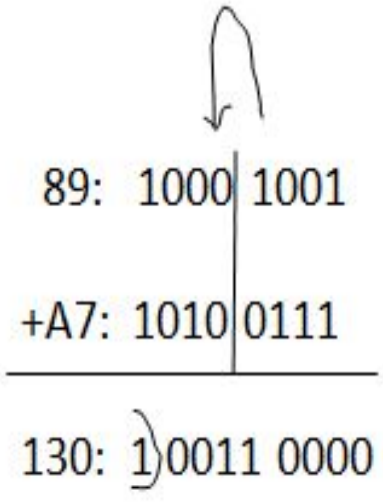
D7	D6	D5	D4	D3	D2	D1	D0
S	Z		AC		P		CY

Exercise

- Perform the following operation and show the status of the flag
  a. 89H + A7H
  b. B4H + 3AH
  c. ADH + 53H
  d. 33H + A6H

Question no 1.

Question 1. 89H+A7H



Therefore the Flag status are

AC: 1(Set)

Parity: 1 (Set)

Sign: 0 (Reset)

Zero: 0(Reset)

Carry: 1(Set)

Thank you