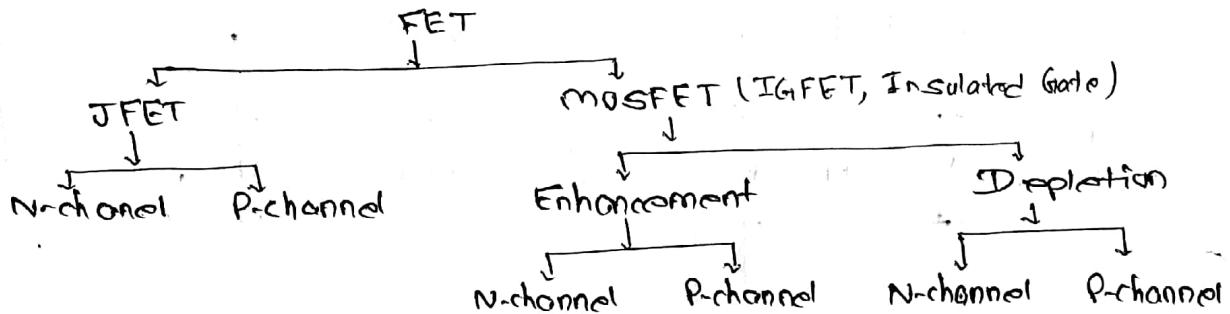


Junction Field Effect Transistor (JFET)

Field effect transistor (FET) is a 3-terminal voltage controlled electronic device. Like BJT, FET can also be used as amplifier & a switch. FET is unipolar device since the current flows due to either electrons (in N-channel) or holes (in P-channel).

Classification of FET



Comparison between BJT & FET

Similarities:

- Both are SiC devices.
- Both are 3-terminal device.
- Both can be used as a switch or an amplifier.

Differences:

- BJT is bipolar while FET is unipolar transistor.
- As the ip ckt (i.e. Gate to Source) of FET is reverse-biased, it has high ip impedance while ip ckt of ordinary transistor is forward biased so that it has low ip impedance.
- BJT has fast switching property than FET.
- FET occupies less chip area than BJT.
- BJT is current controlled while FET is voltage controlled device.
- It has less voltage gain than BJT.
- In BJT current flows through a junction, but in FET current flows through a surface of SiC material (channel) i.e. parallel to junction so that noise level in FET is very small.

JFET

It is a three terminal SiC device. Current conduction is done either by electrons or holes & controlled by electric field b/w Gate electrode & conduction channel.

A JFET consists of a P-type or N-type channel (Silicon Bar) containing two PN junction on each side. The Bar forms the

conducting channel for charge carriers. If bar is of N-type, it is called N-channel JFET & if the bar is of P-type, it is called P-channel JFET. The two PN junction forming diode are connected internally & the common terminal is called Gate. & two ends of a channel are called source & drain.

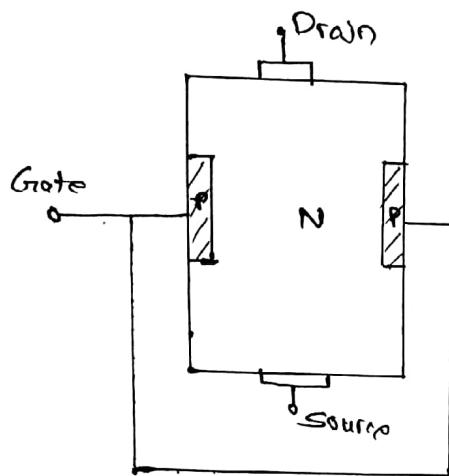


Fig: N-channel JFET

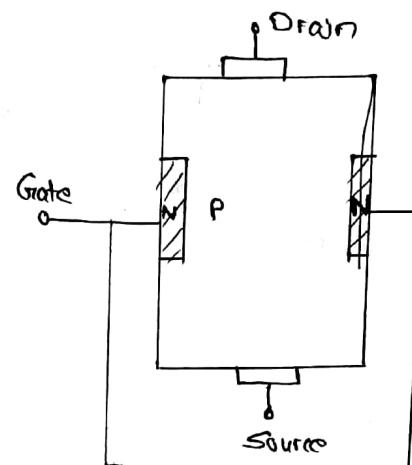


Fig: P-channel JFET

Top of N or P-channel is called Drain & bottom end is called Source. S & D are interchangeable i.e. JFET is symmetrical device.

The schematic symbols of NJFET & PJFET are as shown:

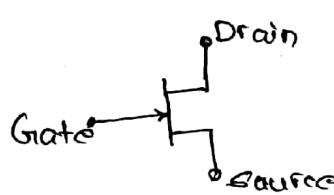


Fig: NJFET
(symbols of JFET)

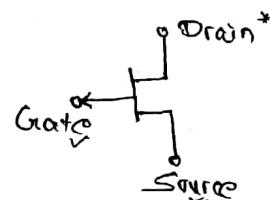


Fig: PJFET



Operation of N-channel JFET (NJFET)
In the NJFET, the N-channel silicon bar has two P-type silicon material diffused on the opposite sides of its middle part. The two PN junctions forming the diodes are internally connected & the common terminal is called Gate, & the two ends of the channel are Drain & Source.

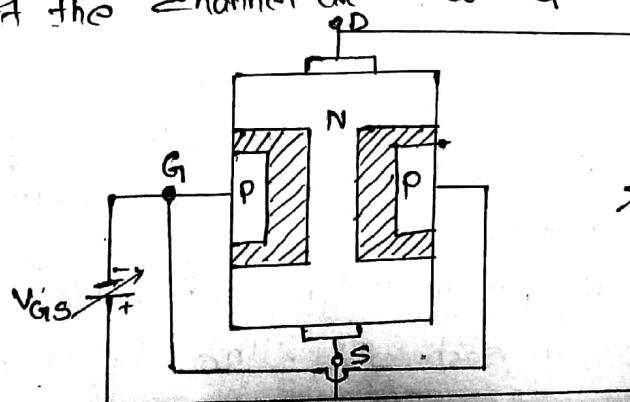


Fig: JFET with
 $V_{GS} = 0V$ & $V_{DS} \geq 0V$

* When $V_{GS} = 0V$ & $V_{DS} = 0V$, i.e. no voltage is applied at a Gate as well as Drain with respect to source, then there will be small depletion region of equal thickness & symmetrical as shown in above figure.

* When $V_{GS} = 0V$ & V_{DS} is slightly increased, current I_D also increases proportionally.

As V_{DS} is increased, depletion region is changed - near the top of the channel (voltage is nearly equal to V_{DS}). So there is large reverse-bias voltage betn N-channel & P-Gate.

At the lower end, reverse-bias voltage becomes smaller so depletion layer becomes wider & hence channel will be narrower at the Drain. The overall channel will be tapered as shown in fig below.

When V_{DS} is sufficiently increased, depletion region meet at point near to Drain end. This condition is known as pinch off & V_{DS} at that condition with $V_{GS} = 0$ is called Pinched off voltage (V_p).

As V_{DS} is increased beyond V_p , I_D will not change and remains constant. The region where I_D increases linearly with V_{DS} is called Ohmic region.

Also the region where I_D remain constant even though the V_{DS} is increased is called Pinch-off or Saturation region. This saturation value of I_D for $V_{GS} = 0$ is called saturation current I_{DSs} . I_{DSs} is maxm possible Drain current for JFET & is defined

by the condition,

$$V_{GS} = 0V \quad \text{&} \quad V_{DS} > |V_{pI}|$$

* Now, if V_{GS} = some -ve value & $V_{DS} > 0V$.

If Gate to source reverse bias voltage is applied, depletion region further penetrates deep into the channel & will be narrower & resistance increases. Now, Pinch off will occur

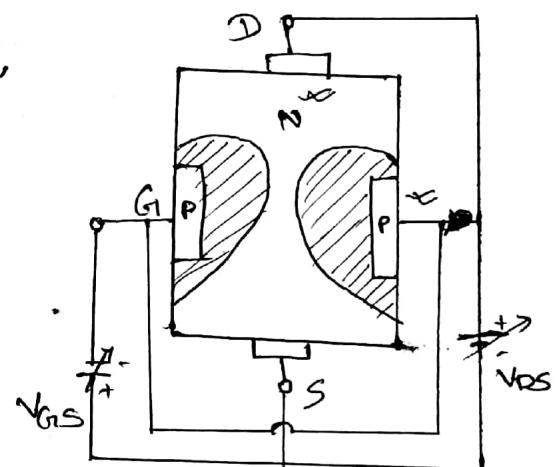


fig: JFET with $V_{GS} = 0V$
& $V_{DS} > 0V$

at lower value of V_{GS} , because there is already another reverse bias voltage V_{GS} .

$$\therefore V_{DS} = V_{GS} - V_p$$

When reverse bias voltage V_{GS} is equal to V_p , depletion layer will meet along the entire path length of channel and drain current I_D is at cutoff region.

$$\text{Cutoff} \Rightarrow V_{GS} = V_p \quad \& \quad I_D = 0$$

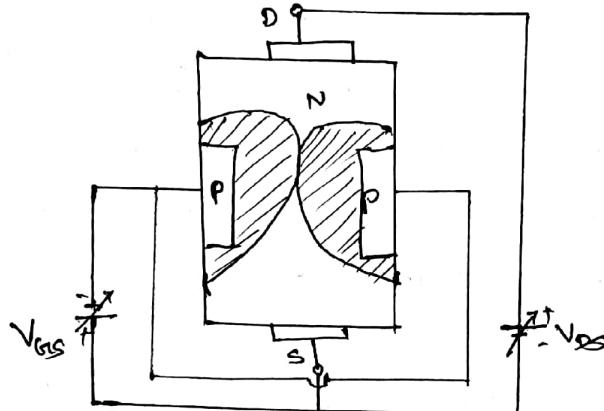


Fig: JFET with $V_{GS} = 0V$ & $V_{DS} > 0V$.

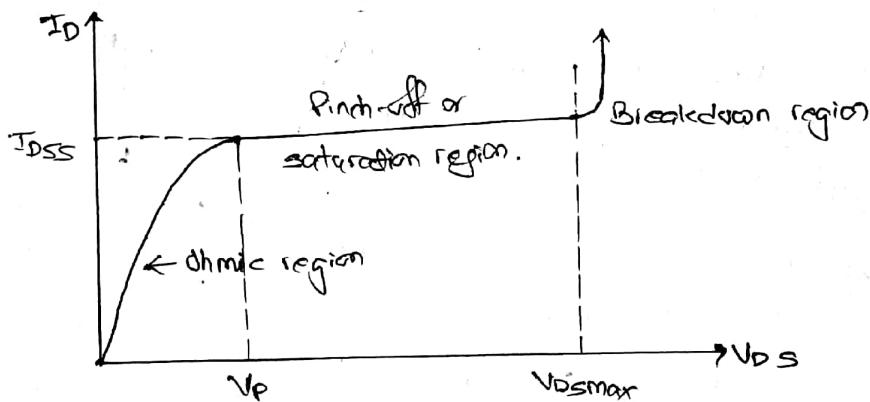


Fig: Drain characteristic with $V_{GS} = 0V$

Drain(I_D) & Transfer Characteristic Curves

The drain characteristic curves are the plots of the drain current (I_D) & drain-to-source voltage (V_{DS}) with constant V_{GS} .

The transfer characteristics for a JFET can be determined experimentally keeping V_{DS} constant & determining I_D for various V_{GS} .

It is observed that:

- I_D decreases with increase in V_{GS} .

ii) $I_D = I_{DSS}$ when $V_{GS} = 0$

iii) $I_D = 0$ when $V_{GS} = V_p$

The drain current in pinch-off or saturation region is given by,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS,off}} \right)^2$$

If reverse-bias voltage V_{DS} (at $V_{GS}=0$) is increased beyond $V_{DS\max}$, an avalanche breakdown occurs & current flows sharply. Although, the breakdown occurs at lesser value of V_{DS} for $V_{GS} = -V_0$ as shown in figure below.

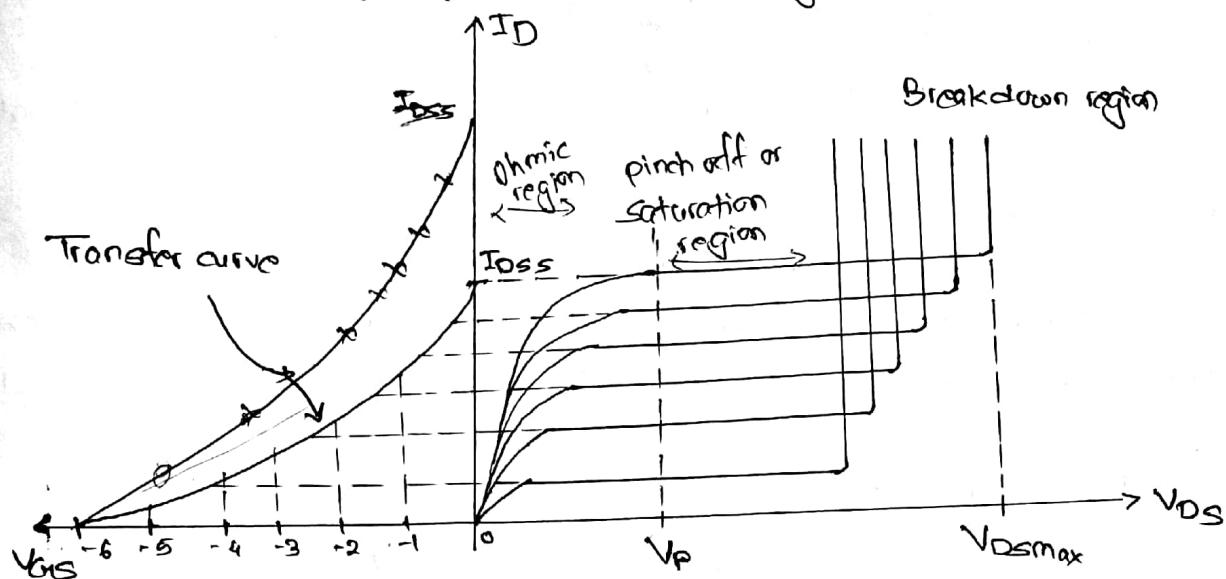


Fig: Drain & transfer characteristics for $V_{GS} > 0$ & $V_{GS} < 0$

General Expression for current in JFET

Current in JFET is,

$$I_D = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_P} \right) \left\{ -\frac{V_{DS}}{V_P} + \left(\frac{V_{DS}}{V_P} \right)^2 \right\} \right]$$

Ohmin region:

$$\frac{V_{DS}}{V_P} \ll 1 \quad \text{or} \quad \frac{V_{DS}}{V_P} < 1$$

$$\text{So, } \left| \frac{V_{DS}}{V_P} \right|^2 \ll 1$$

$$\therefore I_D = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_P} \right) \left(-\frac{V_{DS}}{V_P} \right) \right]$$

$$\frac{I_D}{V_{DS}} = -2 \frac{I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P} \right) = \frac{1}{R_{DS}}$$

i.e. JFET behave as voltage controlled resistance

in ohmic region.

Saturation/Pinch off region:

$$\frac{V_{DS}}{V_P} \geq \frac{V_{GS} - V_P}{V_P}$$

At pinch off region, $V_{DS} = V_{GS} - V_P$ & further increase in V_{DS} doesn't increase I_D .

$$I_D = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_P} \right) \left\{ -\frac{V_{GS} - V_P}{V_P} \right\} - \left(\frac{V_{GS} - V_P}{V_P} \right)^2 \right]$$

$$\Rightarrow I_{D, \text{sat}} = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_P} \right) \left(1 - \frac{V_{GS}}{V_P} \right) - \left(1 - \frac{V_{GS}}{V_P} \right)^2 \right]$$

$$= I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_P} \right)^2 - \left(1 - \frac{V_{GS}}{V_P} \right)^2 \right]$$

$$\therefore I_{D, \text{sat}} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

JFET is operated as an amplifier in pinch-off or saturation region.

JFET Parameters

i) AC Drain resistance (r_d)

It is defined as the ratio of change in Drain-Source voltage (V_{DS}) to change in Drain current (I_D) at constant Gate-Source voltage (V_{GS}).

$$\text{AC drain resistance } (r_d) = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS} = \text{constant}}$$

From the drain characteristics curve, it is observed that the curve is flat in saturation or pinch-off region. i.e. there is only small change in I_D for large change in V_{DS} . It means AC drain resistance of JFET is very large ranging from $10\text{k}\Omega$ to $1\text{M}\Omega$.

ii) Transconductance (g_m)

It is defined as the ratio of change in Drain current ΔI_D to change in Gate-Source voltage (V_{GS}) at constant Drain-Source voltage (V_{DS}).

$$\text{i.e. transconductance } (g_m) = \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{V_{DS} = \text{constant}} \quad (1)$$

$$\text{We have, } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad [\Delta I_D = g_m \Delta V_{GS}]$$

On differentiating w.r.t V_{GS} ,

$$\frac{dI_D}{dV_{GS}} = I_{DSS} * 2 * \left(1 - \frac{V_{GS}}{V_P} \right)^2 * \left(-\frac{1}{V_P} \right)$$

$$\therefore g_m = -\frac{2 I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad (2)$$

$$\text{or } g_m = \frac{2 I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}} = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

When, $V_{GS} = 0$, $g_m = g_{m0}$

$$\text{where, } g_{m0} = \frac{2 I_{DSS}}{V_P} \quad (3)$$

(iii) Amplification factor (μ)
It is defined as the ratio of change of Drain-source voltage (V_{DS}) to Gate-source voltage (V_{GS}) at constant Drain-current (I_D)

i.e. amplification factor (μ) = $\frac{\Delta V_{DS}}{\Delta V_{GS}} \mid I_D = \text{constant}$

or, $\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d * g_m$

$\therefore \mu = r_d * g_m$

JFET Biasing Methods:

1) Fixed Bias

2) Self-bias

3) Voltage divider bias

1) Fixed Bias

A fixed bias N-channel JFET in common source configuration is as shown below.

Here, $V_G = V_{GSE}$

$$V_S = 0$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = -V_{GSE} - 0 = -V_{GG}$$

Applying KVL in O/P loop

$$V_{DD} = I_D R_D + V_{DS}$$

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D \quad (1)$$

For JFET, characteristics eqn is given by,

$$I_D = I_{DSS} \left(1 - \frac{V_{DS}}{V_P} \right)^2 \quad (2)$$

Solving eqn (1) & (2), we can find the value of I_D & V_{DS} which is called operating point for JFET.

2) Self-Bias

Here, $V_G = I_G \cdot R_G$ ($\because I_G = 0$ for JFET)
 $= 0 \cdot R_G = 0$

$$\& V_S = I_D \cdot R_S$$

$$\text{Thus, } V_{GS} = V_G - V_S \quad (V_G = V_{GS} + I_D R_S) \\ = 0 - I_D R_S$$

$$\therefore V_{GS} = -I_D R_S$$

For JFET, we have,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad (1)$$

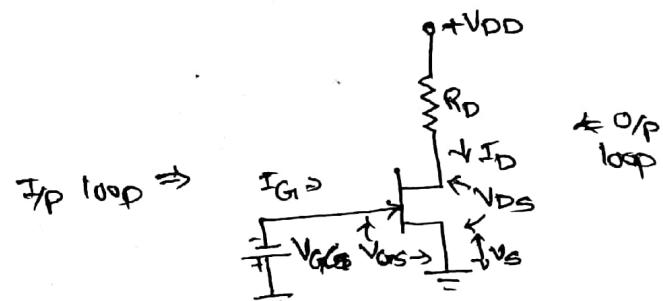


Fig: fixed bias NJFET

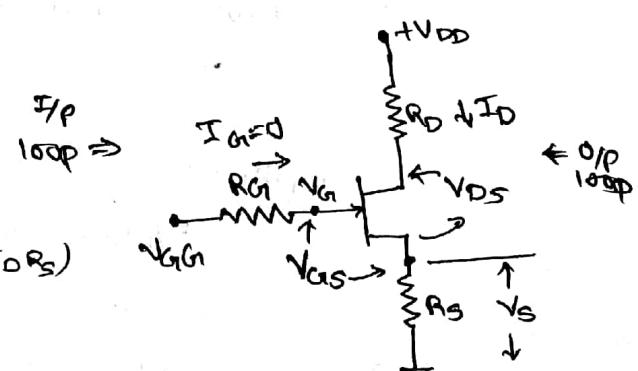


Fig: self Bias NJFET

Applying KVL in O/P loop,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$\therefore V_{DS} = V_{DD} - I_D (R_D + R_S) \quad (1)$$

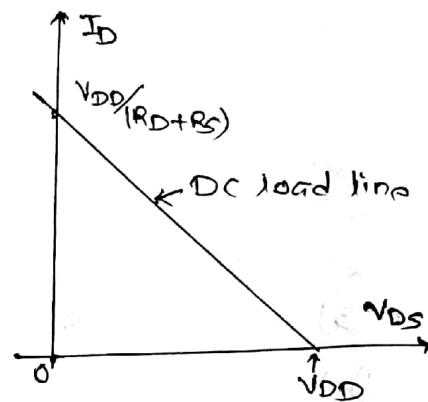
Solving eqn(1) & (2), we can get the values of I_D & V_{DS} , which is operating point.

To draw a DC load line,

From eqn(2), $V_{DS} = V_{DD} - I_D (R_D + R_S)$

$$\text{When, } I_D = 0, \quad V_{DS} = V_{DD}$$

$$\text{When, } V_{DS} = 0, \quad I_D = \frac{V_{DD}}{R_D + R_S}$$



③ Voltage Divider Bias

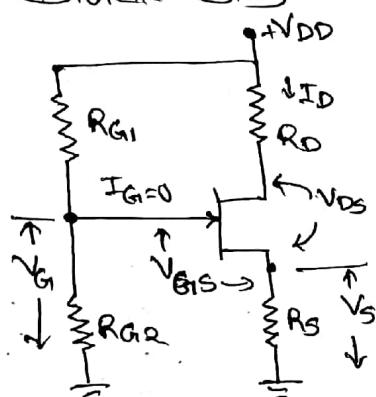


Fig: Voltage divider bias of NJFET

Here, $V_G = V_{RG2}$, voltage drop across R_{G2}

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} \times V_{DD}$$

$$\& \quad V_s = I_D \cdot R_S$$

$$\therefore V_{GS} = V_G - V_s = \frac{R_{G2}}{R_{G1} + R_{G2}} \times V_{DD} - I_D R_S$$

We have, characteristic eqn for JFET is,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad (1)$$

Applying KVL on O/P loop,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$\Rightarrow V_{DS} = V_{DD} - I_D (R_D + R_S) \quad (2)$$

Solving eqn(1) & (2), the values of I_D & V_{DS} can be calculated, & gives operating point.

To draw DC load line,

From eqn(2), $V_{DS} = V_{DD} - I_D (R_S + R_D)$

When $I_D = 0$, $V_{DS} = V_{DD}$

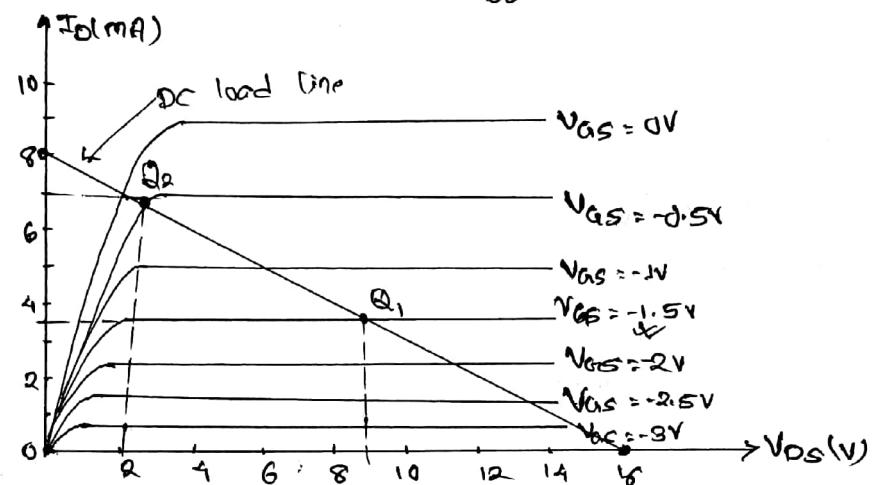
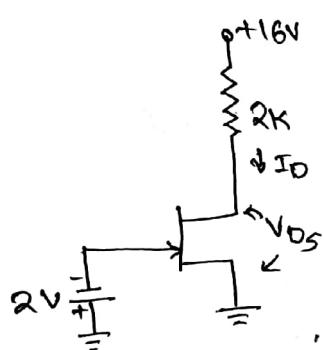
& when $V_{DS} = 0$, $I_D = \frac{V_{DD}}{R_D + R_S}$

By joining these two points $(V_{DD}, 0)$ & $(0, \frac{V_{DD}}{R_D + R_S})$ gives a straight line & is called DC load line.

The drain characteristics of NJFET is shown. Find the quiescent values of I_D & V_{DS} when,

(i) $V_{GS} = -1.5V$, (ii) $V_{GS} = -0.5V$ &

(iii) find I_{DS} if $I_{DSS} = 10mA$ & $N_p = -3.5V$



Soln:

We have $V_{DD} = I_D R_D + V_{DS}$

when $I_D = 0$, $V_{DS} = V_{DD} = 16V$

& when $V_{DS} = 0$, $I_D = \frac{V_{DD}}{R_D} = \frac{16}{2} = 8mA$

Now join these two points $(16, 0)$ & $(0, 8)$ in given characteristic curve.

The DC load line intersects $V_{GS} = -1.5V$, curve at Q_1 & $V_{GS} = -0.5V$ at Q_2 .

At Q_1 , $I_{DQ_1} = 3.5mA$ & $V_{DSQ_1} = 8V$
Here Q-point is in saturation or pinch-off region.

At Q_2 , $I_{DQ_2} = 7mA$ & $V_{DSQ_2} = 2V$

Here, Q_2 is in Ohmic region. The Q-point must be located in the pinch-off region for normal amplifier operation. To operate JFET in pinch-off region, following condition must be satisfied.

$$|V_{DS}| > |V_p| - |V_{GS}|$$

For Q_1 : $|8| > |3.5| - |1.5|$, is valid.

So $I_D = 3.5mA$ is in pinch-off region & is valid.

For Q₂,

$|2I| > |3.5| - |0.5|$, is not valid. So Q₂ is not in pinch-off region.

Again, we have for JFET,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 10 \times 10^{-3} \left(1 - \frac{-1.5}{-3}\right)^2$$
$$= 3.26 \text{ mA}$$

$$\& V_{DS} = V_{DD} - I_D R_D = 16 - 3.26 \times 2$$
$$= 9.46 \text{ V}$$

For the common source NJFET biasing ckt shown,
find I_D & V_{DS} . Given $I_{DSS} = 10 \text{ mA}$ & $V_P = -4 \text{ V}$.

Soln: Given,

$$V_{DD} = 15 \text{ V}$$

$$I_{DSS} = 10 \text{ mA}$$

$$V_P = -4 \text{ V}$$

$$R_D = 1.5 \text{ k}\Omega$$

$$R_S = 600 \Omega$$

We have, for JFET,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{where, } V_{GS} = V_G - V_S = I_G R_G + I_D R_S = 0 \Rightarrow 600 I_D = -600 I_D$$

$$\text{So, } I_D = 10 \times 10^{-3} \left(1 - \frac{-600 I_D}{-4}\right)^2 = \frac{10 \times 10^{-3}}{16} (4 - 600 I_D)^2$$

$$\text{or, } 16 I_D = 10 \times 10^{-3} (16 - 4800 I_D + 360000 I_D^2)$$

$$\text{or, } 16 I_D = 0.16 - 48 I_D + 3600 I_D^2$$

$$\text{or, } 3600 I_D^2 - 64 I_D + 0.16 = 0$$

On solving above eqn,

$$I_D = 3 \text{ mA or } 14.8 \text{ mA}$$

As, Drain current can't be greater than I_{DSS} .

So $I_D = 14.8 \text{ mA}$ is not valid. Thus,

$$I_D = 3 \text{ mA.}$$

$$\text{Now, } V_{DS} = V_{DD} - I_D(R_D + R_S) \\ = 15 - 3 \times 10^{-3} (1.5 \times 10^3 + 0.6 \times 10^3) = 8.7V$$

$$\& V_{GDS} = -I_D R_S = -3 \times 0.6 = -1.8V$$

$$\text{Here, } |V_{DS}| > |V_p| - |V_{GS}|$$

$$\text{or, } |8.7| > |-4| - |-1.8|$$

or, $8.7 > 2.2$, is True.

Thus operating point is in the pinch-off region.

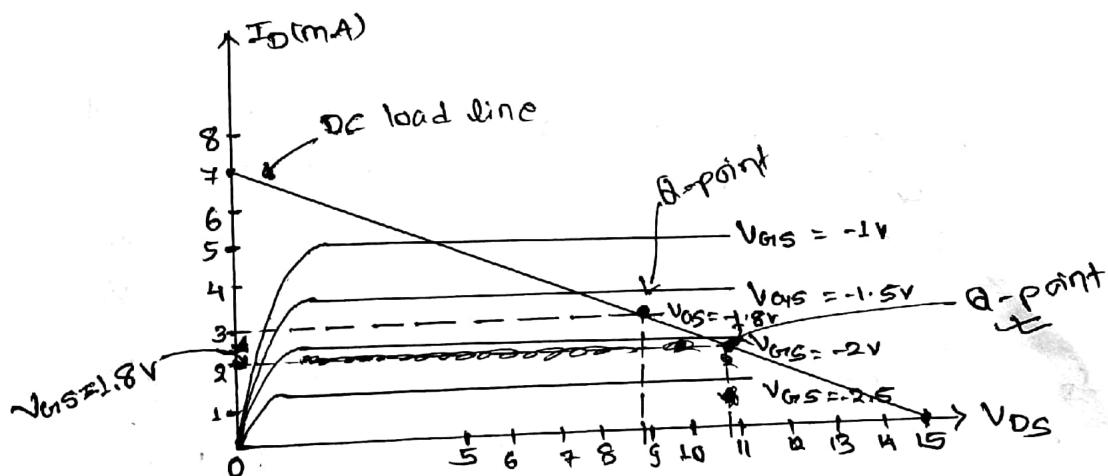
For DC load line,

$$\text{we have, } V_{DS} = V_{DD} - I_D(R_D + R_S) = V_{DD} - I_D(1.5 + 0.6)$$

$$\text{or, } V_{DS} = 15 - 2.1 I_D$$

$$\text{when } I_D = 0, V_{DS} = V_{DD} = 15V$$

$$\& \text{when } V_{DS} = 0, I_D = \frac{V_{DD}}{R_D + R_S} = \frac{15}{2.1} = 7.143 \text{ mA}$$



Here, DC load line intersects $V_{GDS} = -1.8V$ at Q,

$$\text{where } I_{DQ} = 3 \text{ mA} \& V_{DSQ} = \cancel{10.8} \cancel{V} = 8.7V$$

This is Q-point & is in the pinch-off region.

An NJFET has $I_{DSS} = 10 \text{ mA}$ & $V_p = -4 \text{ V}$. Find minimum value of V_{DS} for pinch-off region & drain current for $V_{GS} = -2 \text{ V}$ in pinch-off region.

$$\text{Soln: Drain current, } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 = 10 \times 10^{-3} \left(1 - \frac{-2}{-4}\right)^2 \\ = 10 \times 10^{-3} (1 - 0.5)^2 = 2.5 \times 10^{-3} = 2.5 \text{ mA}$$

$$\text{And, } V_{DS\min} = |V_p| = 4 \text{ V.}$$

For the NJFET biasing ckt given find: V_{AS} , V_{DS} & I_D .
 Given $I_{DSS} = 12 \text{ mA}$ & $V_p = -6 \text{ V}$

Sol:

We have, for JFET

$$I_D = I_{DSS} \left(1 - \frac{V_{AS}}{V_p} \right)^2$$

Here, at I/P loop,

$$-3 = I_{G1} R_{G1} + G_S$$

$$\Rightarrow G_S = -3 \text{ V} \quad (\because I_{G1} = 0)$$

$$\text{So, } I_D = 12 \times 10^{-3} \left(1 - \frac{-3}{-6} \right)^2 = 12 \times 10^{-3} (1 - 0.5)^2 = 2.5 \text{ mA}$$

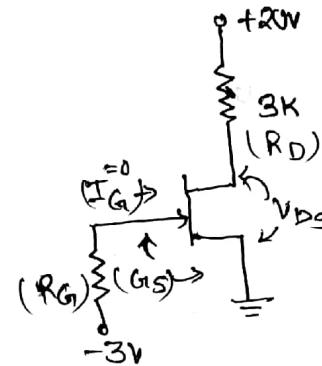
$$\therefore I_D = 2.5 \text{ mA}$$

Also, applying KVL in O/P loop

$$V_{DD} = I_D R_D + V_{DS}$$

$$\Rightarrow V_{DS} = 20 - 2.5 \times 3 = 12.5 \text{ V}$$

$$\therefore V_{DS} = 12.5 \text{ V}$$



Design a voltage divider NJFET ckt operating at 15mA.
 drain current & 10V drain-to-source voltage.

Given, $I_{DSS} = 25 \text{ mA}$ & $V_p = -4 \text{ V}$.

Sol:

Given, $I_{DSS} = 25 \text{ mA}$

$$V_p = -4 \text{ V}$$

$$I_D = 15 \text{ mA}$$

$$V_{DS} = 10 \text{ V}$$

We know that,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$\text{or, } 15 = 25 \left(1 - \frac{V_{GS}}{-4} \right)^2$$

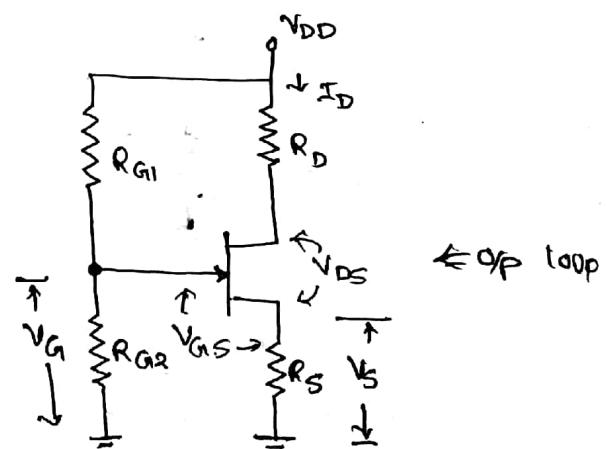
$$\text{or, } 1 + \frac{V_{GS}}{4} = \sqrt{\frac{15}{25}} = \sqrt{0.6}$$

$$\therefore V_{GS} = -0.9 \text{ V}$$

$$\text{Also, from figure, } V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} * V_{DD} = \frac{20 R_{G2}}{R_{G1} + R_{G2}}$$

$$\text{and } V_S = I_D R_S = 15 R_S$$

$$\text{Also, } V_{GS} = V_G - V_S \Rightarrow -0.9 = \frac{20 R_{G2}}{R_{G1} + R_{G2}} - 15 R_S \quad \text{--- (i)}$$



Applying KVL in O/P loop.

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S = V_{DS} + I_D (R_D + R_S)$$

$$\text{or, } 20 = 10 + 15 (R_D + R_S)$$

$$\Rightarrow R_D + R_S = \frac{10}{15} = 0.66 \text{ k}\Omega$$

$$\text{Let } R_D = 0.5 \text{ k}\Omega$$

$$\text{Then, } R_S = 0.66 - 0.5 = 0.16 \text{ k}\Omega$$

Now, from eqn (i)

$$-0.9 = \frac{20 R_{G2}}{R_{G1} + R_{G2}} - 15 \times 0.16$$

$$\boxed{R_D > R_S \\ \& R_{G1} > R_{G2}}$$

$$\text{or, } \frac{20 R_{G2}}{R_{G1} + R_{G2}} = 2.4 - 0.9 = 1.5$$

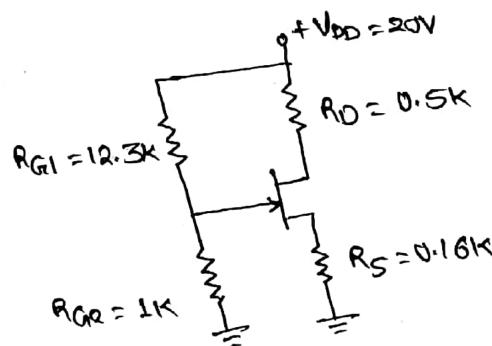
$$\text{or, } 20 R_{G2} = 1.5 R_{G1} + 1.5 R_{G2}$$

$$\text{or, } 18.5 R_{G2} = 1.5 R_{G1}$$

$$\text{Let } R_{G2} = 1 \text{ k}\Omega$$

$$\text{Then, } R_{G1} = \frac{18.5}{1.5} \times 1 = 12.3 \text{ k}\Omega$$

Now, the voltage divider NJFET circuit operating at $I_D = 15 \text{ mA}$
& $V_{DS} = 10 \text{ V}$ is,



Design a self-bias NJFET circuit operating at 15mA drain current & 10V drain-to-source voltage. Given $I_{DSS} = 25 \text{ mA}$, $V_p = -4 \text{ V}$ & $V_{DD} = 25 \text{ V}$. Also find transconductance.

Sol:

Given, $I_{DSS} = 25 \text{ mA}$

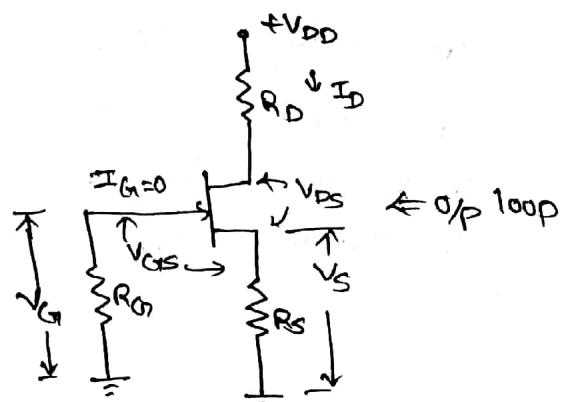
$$V_p = -4 \text{ V}$$

$$V_{DD} = 25 \text{ V}$$

$$I_D = 15 \text{ mA}$$

$$V_{DS} = 10 \text{ V}$$

$$\text{we have, } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$



$$\text{or, } I_S = 25 \left(1 - \frac{V_{GS}}{-4} \right)^2 = 25 \left(1 + \frac{V_{GS}}{4} \right)^2$$

$$\text{or, } 1 + \frac{V_{GS}}{4} = \sqrt{\frac{15}{25}}$$

$$\Rightarrow V_{GS} = -0.9V$$

$$\text{Also, } V_G = I_G R_G = 0$$

$$\text{and, } V_S = I_D R_S = 15 R_S$$

$$\text{Thus, } V_{DS} = V_G - V_S \quad \left[\Rightarrow V_{GS} = -V_S = -0.9V \right]$$

$$\text{or, } -0.9 = 0 - 15 R_S$$

$$\Rightarrow R_S = \frac{0.9}{15} = 0.06K$$

Applying KVL in O/P loop,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$\text{or, } 20 = 15 R_D + 10 + 0.9$$

$$\Rightarrow R_D = \frac{14.1}{15} = 0.9K\Omega$$

$$\text{Let } R_O = 100\Omega$$

$$\text{Then, transconductance, } g_m = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P} \right)$$

$$\text{or, } g_m = -\frac{2 \times 25 \times 10^{-3}}{-4} \left(1 - \frac{-0.9}{-4} \right)$$

$$= 12.5 \times 10^{-3} (1 - 0.225)$$

$$= 12.5 \times 10^{-3} \times 0.775$$

$$\therefore g_m = 9.687 \times 10^{-3} = 9.687 \text{ mS}$$

JFET Configurations

1. Common Source JFET

2. Common Drain JFET

3. Common Gate JFET

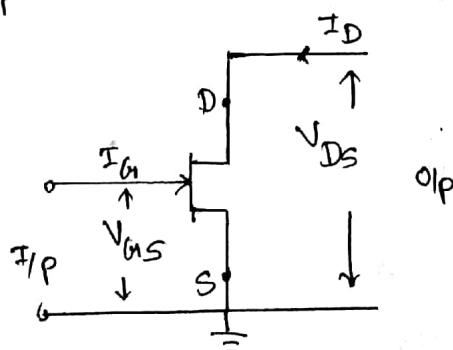
↳ Common Source NJFET

I/P voltage = V_{GS}

I/P current = $I_G = 0$

O/P voltage = V_{DS}

O/P current = I_D



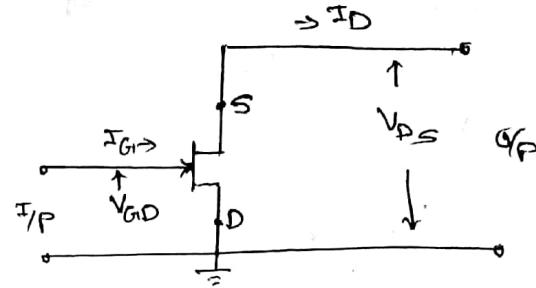
2) Common Drain JFET

Here, I/P voltage = V_{GD}

I/P current = $I_{G1} = 0$

O/P voltage = V_{DS}

O/P current = I_D



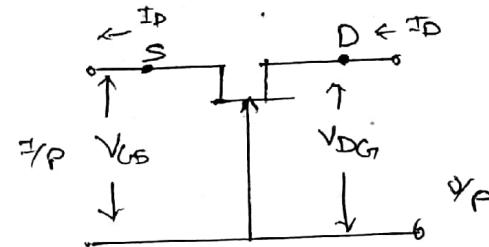
3) Common Gate JFET

Here, I/P voltage = V_{GS}

I/P current = I_D

O/P voltage = V_{DG}

O/P current = I_D



Small Signal Low Frequency Model of JFET

1) Common Source NJFET [Common Emitter]

Common Source NJFET is the mostly used configuration because it provides high-I/P impedance, good voltage gain & moderately low-O/P impedance.

The circuit diagram for a common source NJFET and its small signal model are as shown in fig. below:

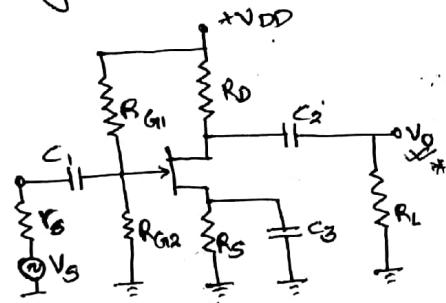


Fig: Common source NJFET

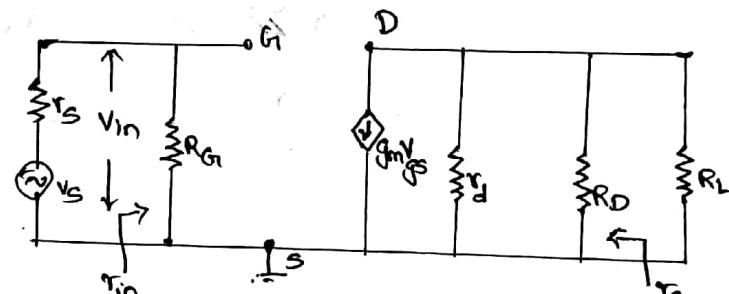


Fig: small signal model

Here, $R_{G1} = R_{G1} // R_{G2}$

i) Input Impedance, $Z_{in} = R_{G1}$

ii) O/P impedance (resistance), $Z_o = r_d // R_D$

iii) Voltage gain (A_v) = $\frac{V_o}{V_{in}}$

From small signal model,

$$V_o = j_0 (r_d // R_D) = -g_m V_{GS} (r_d // R_D)$$

$$\& V_{in} = V_{GS}$$

$$\therefore A_v = -\frac{g_m V_{GS} (r_d // R_D)}{V_{in}} = -g_m (r_d // R_D)$$

In Common Source
Source \Rightarrow common
O/P from \Rightarrow Drain

$r_{in} \Rightarrow R_{G1}$
 $r_o \Rightarrow R_D$
 $V_o \Rightarrow R_D$
(R_L not included)

Also, Overall voltage gain (V_o/V_s)

$$\frac{V_o}{V_s} = A_v \left(\frac{r_{in}}{r_s + r_{in}} \right) \left(\frac{R_L}{r_o + R_L} \right)$$

2) Common Drain NJFET

Figure below shows the common drain NJFET & its small signal model

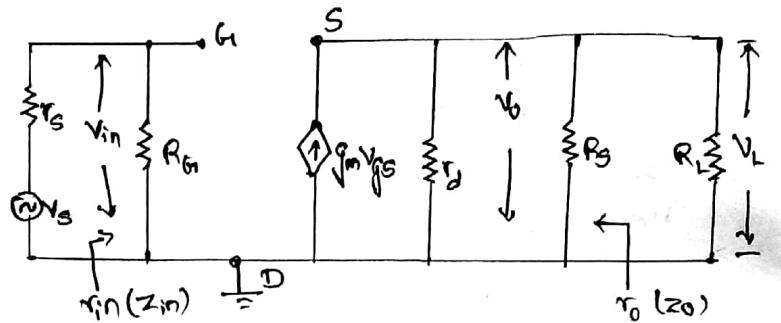
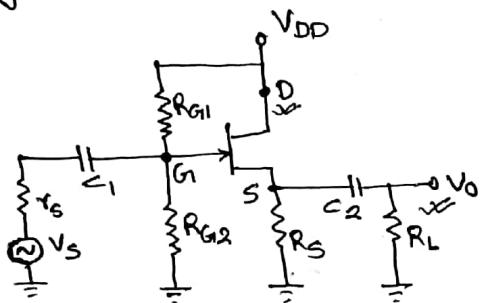


Fig: Common Drain NJFET

$$\text{Here, } R_G = R_{G1} // R_{G2}$$

Resistance looking into the source terminal is given by

$$Z_S = \frac{V_{GS}}{I_D} = \frac{V_{GS}}{g_m V_{GS}} = \frac{1}{g_m}$$

i) Input Impedance

$$r_{in} \text{ or } Z_{in} = R_{G1}$$

ii) Output Impedance

$$Z_O = R_S // r_d // Z_S = R_S // r_d // \frac{1}{g_m}$$

$$\text{But, } r_d \gg \frac{1}{g_m} \quad (r_d \gg \frac{1}{g_m})$$

$$\text{So, } Z_O = R_S // \frac{1}{g_m}$$

iii) Voltage Gain

$$A_V = \frac{V_o}{V_{in}}$$

From small signal model,

$$V_o = g_m V_{GS} \cdot (r_d // R_S)$$

$$\& V_{in} = V_{GS} + V_{SD} = V_{GS} + V_o \quad (\because V_o = V_{SD})$$

$$= V_{GS} + g_m V_{GS} (r_d // R_S)$$

$$= V_{GS} [1 + g_m (r_d // R_S)]$$

$$\text{Thus, } A_V = \frac{g_m V_{GS} (r_d // R_S)}{V_{GS} [1 + g_m (r_d // R_S)]}$$

$$= \frac{g_m (r_d // R_S)}{1 + g_m (r_d // R_S)}$$

$$\left[\& \text{ Overall gain} = \frac{V_o}{V_S} = A_V \left(\frac{r_s}{r_{eff,in}} \right) \left(\frac{R_L}{r_o + R_L} \right) \right]$$

$r_o \Rightarrow \text{Load}$
 $V_S \Rightarrow \text{Source}$

3) Common Gate JFET

The common Gate JFET & its small signal model is as shown in figure below:

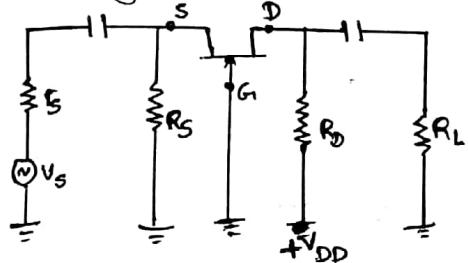


Fig: Common Gate JFET

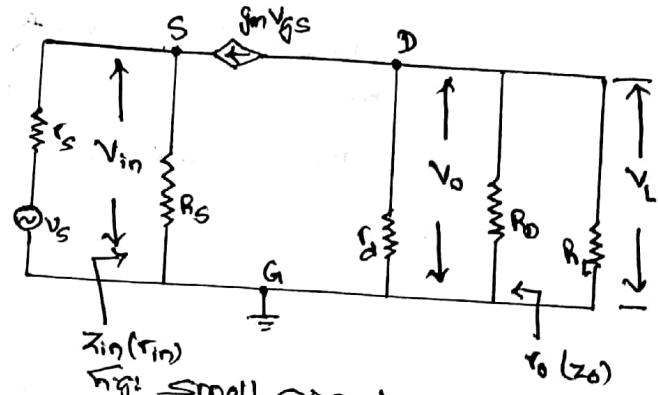


Fig: Small signal model

Here,

Resistance looking into source terminal is

$$Z_S = \frac{V_{GS}}{I_D} = \frac{V_{GS}}{g_m V_{GS}} = \frac{1}{g_m}$$

i) Input Impedance or resistance (Z_{in} or r_{in})

$$Z_{in} = R_S \parallel Z_S = R_S \parallel \frac{1}{g_m}$$

(Since i_p is across source terminal, so Z_S must be included)

ii) Output Impedance or resistance (Z_o or r_o)

$$Z_o = r_d \parallel R_D$$

iii) Voltage gain (A_v)

$$A_v = \frac{V_o}{V_{in}} = \frac{-g_m V_{GS} (r_d \parallel R_D)}{V_{GS}} = \frac{-g_m V_{GS} (r_d \parallel R_D)}{-V_{GS}}$$

$$\therefore A_v = g_m (r_d \parallel R_D)$$

$$\& \text{overall gain} = \frac{V_o}{V_S} = A_v \left(\frac{r_{in}}{r_{in} + r_s} \right) \left(\frac{R_L}{r_o + R_L} \right)$$

The JFET shown in figure has transconductance 4mS at its bias point. Its drain resistance is 100kΩ. Assuming small signal model, find the overall voltage gain.

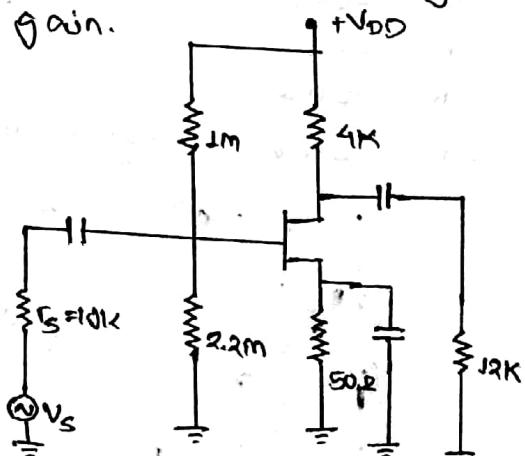
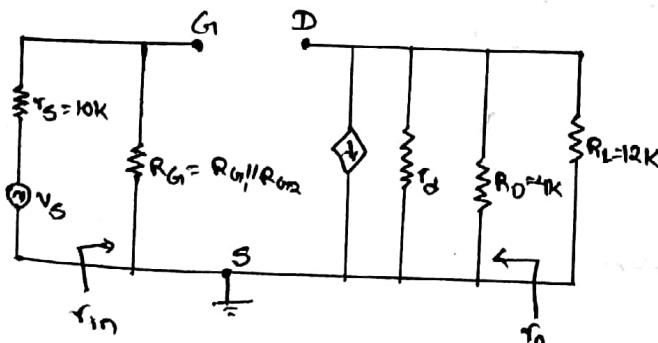
Soln:

Given,

$$g_m = 4000 \mu S = 4000 \times 10^{-6} S$$

$$r_d = 100 k\Omega$$

Its small signal model is,



$$\text{Now, } R_{G1} = R_{G11} // R_{G12}$$

$$= 1 // 2$$

$$= \frac{1 \times 2}{1+2} \text{ M}\Omega = 687.5 \text{ k}\Omega$$

Then, we know,

$$r_{in} = R_{G1} = 687.5 \text{ k}\Omega$$

$$\text{and, } r_o = r_d // R_D = 100 // 4 = \frac{100 \times 4}{104} = 3.846 \text{ k}\Omega$$

$$\text{Given, } A_v = -g_m (r_d // R_D)$$

$$= -4000 \times 10^{-6} \times 3.846 \times 10^3 \\ = -15.44$$

Then,

Overall voltage gain is given by,

$$\frac{V_L}{V_S} = A_v \left(\frac{r_{in}}{r_{in} + r_o} \right) \left(\frac{R_L}{R_L + r_o} \right) \\ = -15.44 \left(\frac{687.5}{10 + 687.5} \right) \left(\frac{12}{3.846 + 12} \right)$$

$$\therefore \frac{V_L}{V_S} = -11 //$$

* Calculate r_{in} , r_o , A_v for the common drain JFET shown in figure. Given $I_{DSS} = 10 \text{ mA}$, $V_P = -5 \text{ V}$, $r_d = 100 \text{ k}\Omega$.

Soln:

Given,

$$I_{DSS} = 10 \text{ mA}$$

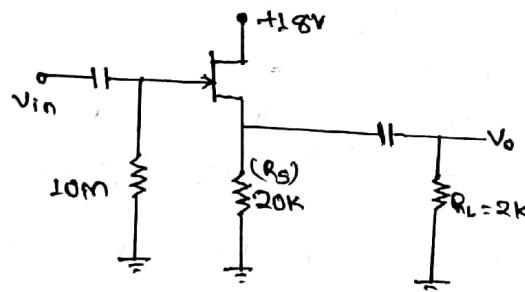
$$V_P = -5 \text{ V}$$

$$r_d = 100 \text{ k}\Omega$$

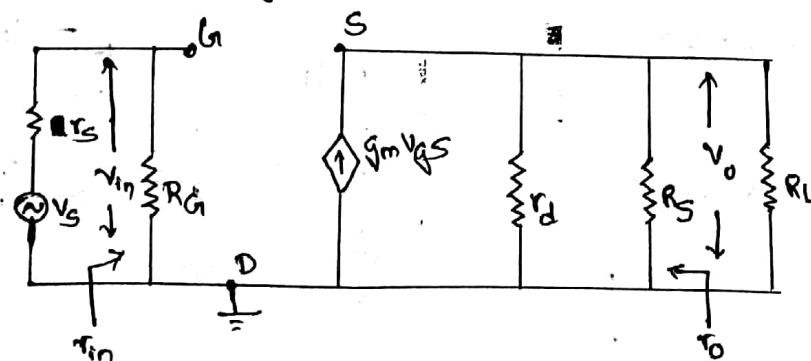
$$R_S = 20 \text{ k}\Omega$$

$$R_L = 2 \text{ k}\Omega$$

$$R_{G1} = 10 \text{ M}\Omega$$



This small signal model is,



$$\text{Here, } r_{in} = R_G = 10 \text{ M}\Omega$$

$$r_o = R_S // r_d // 1/g_m = 20 // 100 //$$

$$\text{where, } g_m = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GDS}}{V_P} \right) = -\frac{2 \times 10 \times 10^{-3}}{-5} \left(1 - \frac{4.3}{5} \right)$$

* As we have, $|V_{GDS}| = |V_P| - \frac{V_{GDS}}{5} = 5 - 0$
 $\therefore V_{GDS} = -4.3 \text{ V}$

$$\text{So, } g_m = \frac{2 \times 10 \times 10^{-3}}{5} \left(1 - \frac{4.3}{5} \right) = 0.5 \text{ mS}$$

Now,

$$r_o = R_S \parallel r_d \approx \frac{1}{g_m}$$

$$= 20 \parallel 100 \parallel 2.98$$

$$= 1.76 \text{ k}\Omega$$

Then, voltage gain,

$$A_V = \frac{V_o}{V_{in}} = \frac{g_m V_{GS} (R_S \parallel r_d)}{V_{GS} + g_m V_{GS} (R_S \parallel r_d)} = \frac{g_m (R_S \parallel r_d)}{1 + g_m (R_S \parallel r_d)}$$

$$= \frac{0.5 \times (20 \parallel 100)}{1 + 0.5 \times (20 \parallel 100)}$$

$$= 0.4$$

Uni Junction Transistor (UJT)

The Uni-Junction Transistor (UJT) consists of a lightly-doped N-type silicon bar with a small piece of heavily doped P-type material alloyed to its one side. Since there exists only one junction, it is called a uni-junction transistor. The silicon bar has two ohmic contacts which are called Base 1 and Base 2, as shown in figure below, where P-type region is called emitter (E), which is located closer to B₂.

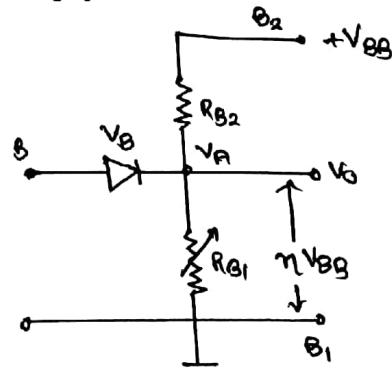
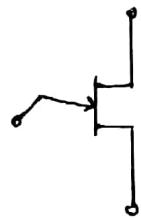
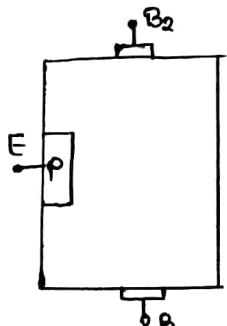


Fig: Construction, Symbol & equivalent circuits.

Operation

* Here, $V_A = \frac{R_B}{R_B + R_E} \times V_{BB}$

Case 1:
 Let $V_E = 0$. The diode is reverse-biased with $V_B + \eta V_{BB}$.

Then only leakage saturation current flows.

Case II:

Let V_E is increased slowly. If $V_E = \eta V_{BB}$, then the leakage saturation current (I_{E0}) is reduced to zero.

Case III:

If $V_E > (\eta_0 V_{BB} + V_B)$, then the diode is forward-biased & I_E flows through R_{B1} & the resistance R_{B1} is reduced. This causes the diode to be in a more forward-biased mode & results in large forward current.

Since, V_A decreases with the increase in emitter current, VJT is said to have a -ve resistance characteristics.

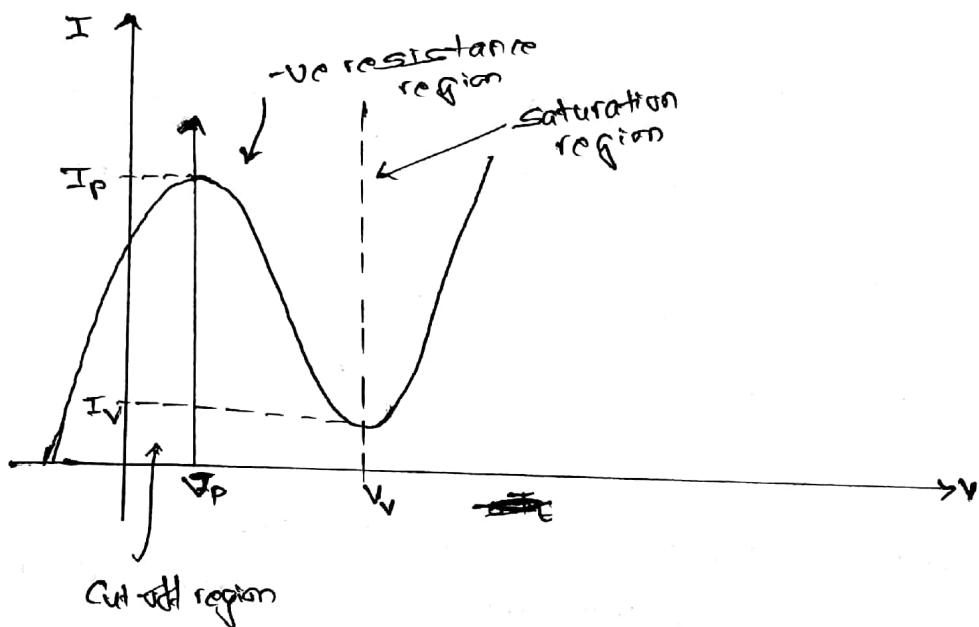


Fig: Characteristics curve of VJT