ELX 212.3 Logic Circuits (3-1-3)

	Theory	Practical	Total
Sessional	30	20	50
Final	50	-	50
Total	80	20	100

Course Objectives:

1. To provide basics of logic systems.
2. To design, construct and test logic circuits.
3. To design a basic digital computer.

Course Contents:

1. Introduction (3 hrs)

Numerical representation, Digital number system, Digital and analog system, representing binary quantities.

2. Number System and Codes (6 hrs)

Binary to decimal and decimal to binary conversions, Octal, hexadecimal number system and conversions, Binary arithmetic, 1's complement and 9's complements, gray code, instruction codes, alphanumeric characters, Modulo 2 system and 2's complement, Binary coded decimal (BCD) and hexadecimal codes, Parity method for error detection.

3. Boolean Algebra and Logic Gates (4 hrs)

Basic definition, Basic properties and theorem of Boolean algebra, DeMorgan's theorem, Logic gates and truth tables, Universality of NAND and NOR gates, Trio-stage logic.

4. Simplification of Boolean Functions (4 hrs)

Venn diagrams and test vectors, Karnaugh maps up to five variables, Minimum relizatio, don't care conditions, Logic gates implementation, Practical design steps.

5. Combinational Logic (3 hrs)

Design procedure, Adders and subtractors, Code conversion, analysis procedure, Multilevel NAND and NOR circuits, Parity generation and checking.

6. MSI and LSI components in Combinational Logic Design (4 hrs)

Binary adder and substractor, decimal adder, Magnitude comparator, decoder and encoder, Multiplexer and demultiplexer, Read-only memory (ROM), programmable, Logic Array (PLA), Programmable Array Logic (PAL).

7. Sequential Logic (6 hrs)

Event driven model and state diagram, Flip-flops and their types, Analysis of clocked sequential circuits, Multiplexer as memory device, State reduction and assignment, Synchronous and asynchronous logic, Two-phase asynchronous logic, Edge triggered device, Master-slave flip-flops, JK and T flip flops.

8. Registers, Counters and Memory Unit (6 hrs)

Registers, shift registers, superposition of registers, generation of codes using register, Ripple, Synchronous and Johnson counters, Design of multiple input circuits, Random Access Memory (RAM), Memory decoding, error-correction code, Output hazards races.

9. Arithmetic Logic units (9 hrs)

Nibble adder, Adder/substrata unit, Design of arithmetic logic unit, Status register, Design of shifter. Processor unit Design of accumulator, System configuration, Memory, Program counters, Accumulator and instruction register, Flags.

Laboratory:

1. Familiarization with logic gates.
2. Encodes and decodes.
3. Multiplexer and demultiplexer.
4. Design of simple combinational circuits.
5. Design of adder/ substrator.
6. Design of flip-flop.
7. Design of counter.
8. Clock driven sequential circuits.
9. Conversion of parallel data into serial formal.
10. Generation of timing signal for sequential system.\

Reference Books:

1. M. Mano, *Digital Logic and Computer Design*, Prentice Hall of India, 1998.
2. M. Mano, *Computer System Architecture*, Prentice Hall of India, 1998.
3. M. Mano, *Digital Design*, Prentice Hall of India, 1988.