

microprocessor

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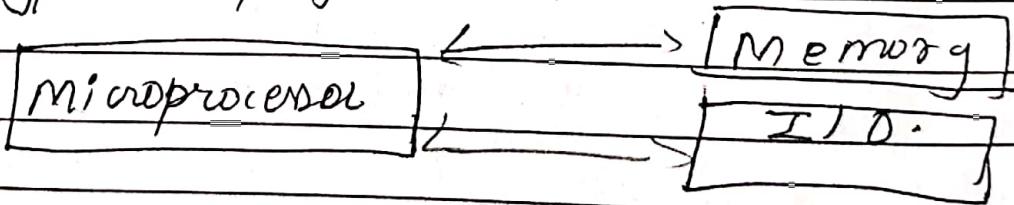
-> IT IS A PROGRAMMABLE DEVICE.

A microprocessor is a multipurpose, programmable, clock driven, register based electronic device that reads binary input as instructions from storage device called memory, processes the data acc. to instructions & provides results as output.

3 basic characteristics that differentiate the microprocessors:

1. Instruction set : no. of instruction
2. Bandwidth : no. of bits processed in a single instruction.
3. Clock speed : how many instruction per sec.

A typical programmable machine.



It consists of.

1. Microprocessor
2. Memory
3. Input device
4. Output device

MP Based system

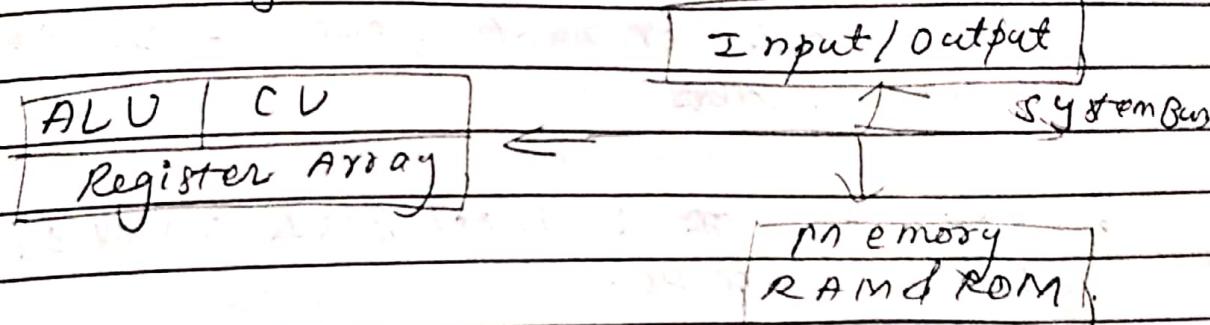


Fig MP based system with Bus Architecture.

1. CPU
 └> ALU
 └> CU
 └> Register

2. Data is fed through input device & collected via output devices.
3. RAM and ROM helps to store the data as memory.
4. The system bus carries the information (data and address) to and from the memory devices to the CPU.

Microcomputer:

- As the name implies, microcomputers are small computers.
- They range from small controllers that work directly with 4-bit words to larger units that work directly with 32-bit words.

- Some of the more powerful microcomputers have all or most features of earlier minicomputers.
- Examples of : Intel 8085 controller - a single board , IBM PC.

II Microcontroller

- Single - chip microcomputers .
- They are used primarily to perform dedicated functions .
- They are used as slaves in distributed processing .

Diff betw. microprocessor & microcontroller .

- # Fixed Program concept
- # Stored Program concept
- 1. von Neumann Architecture
- 2. Harvard Architecture .

8085 Microprocessor

- 8 bit microprocessor .
- capable of addressing 64K memory .
- 8 bit data bus (Bi-directional)
- Has 40 pin DIP (Dual In-line Package)
- Requires +5V power supply .
- Min clock of 500kHz to maximum of 3MHz
- Has 246 instructions sets .

- Data and address are in Hexadecimal notation as
 - Data (from 00H to FFH)
 - Address (from 0000H to FFFFH)
 i.e. if we convert to binary we get 9 bits for each hex as "0000 0000" which is 8 bit width

Pin configuration of 8085 microprocessor

1. Address bus (A15-A00)

- 16 signal lines are used as address bus.
- However these lines are split into 2 A15-A8 and A07-A00.
- A15-A8 are unidirectional and carries higher order address.
- A07-A00 are used for dual purpose.

2. Data Bus (A07-A00)

Bidirectional

Lower order address bus as well as data bus.

3. Control and status signal.

The processor contains 2 control signals (RD & WR) and 3 status signals (IO/M, S1, S2).

4. ALE: Address Latch Enable is a signal that is generated every time when operation begins.

- \overline{RQ} (Read): When it is low, it indicates that selected I/O or memory device is to be read and data are available on databus. It is active low signal.
- \overline{WK} : When it is low, indicates the selected data on the data bus are ready to be written into memory (or I/O location).
- $I0/I1$: When it is high, indicates the I/O operation and when it is low it indicates memory related operation.
- $S0$ & $S1$: Status 0 and status 1 signals are used to identify various operations.

$S1$	$S0$	Mode
0	0	HLT
0	1	WRITE
1	0	READ
1	1	OPCODE FETCH

- $S0D$ & $S1D$: Serial input data comes bit by bit into the MP4 and goes out through the serial out data pin bit by bit.

• Interrupts:

- a) TRAP: Highest priority interrupt. Non-maskable
- b) RST 7.5, 8.5, 5.5: Maskable restart interrupt.
- c) I

- HOLD: This signal indicates that a peripheral device such as DMA is requesting the use of address and data bus.

- HLDC(HOLD ACK): It acknowledges the HOLD request.

- READY: This signal is used to delay the up Read or write cycle until a slow responding peripheral is ready to send or accept data. When it goes low, it waits until it goes high.

- X1, X2: They are crystal oscillators that provides the frequency which are internally divided into two.

- RESET OUT: It is a active high signal that resets the devices which are connected to it.

- RESET IN: When the signal on this pin goes low, the program counter is set to zero and MPO is reset.

8085 Architecture.

- 1) Program Counter (16)
- 2) Instruction Register (8)
- 3) Accumulator (8)
- 4) General Purpose Registers (8)
- 5) Temporary Registers (8)
- 6) Stack Pointer (16)

7 flags and flip flops.

5 flip flops.

- i. Carry flag.
- ii. zero flag.
- iii. sign flag.
- iv. parity flag.
- v. auxiliary carry (AC)

Exercise.

Perform the following operation & show flag.

a) $89H + A7H$

b) $B4H + 3AH$

c) $A0H + 53H$

d) $33H + A6H$

Timing Diagram

- > Timing Diagram is a graphical representation of instructions executed with respect to clock.
- > The execution time is represented in T-states.
- > The following control signals, status signals and buses must be shown in the timing diagram:
 - 1) Higher Order Address Bus, Lower Order Address Bus.
- > ALE, WR, RD, IO1, M1, S1, S0.
- * T-state is defined as the subdivision of operation performed in 1 clock period.
1 T-state is precisely equal to 1 clock period.
- * Machine cycle: The time taken by the processor to access memory location, I/O ports or to acknowledge the interrupt is called machine cycle.
- * Instruction cycle: The time taken to complete the execution of an instruction is called instruction cycle - It is the combination of machine cycle.

Instr.: STA
 STAX
 OUT

Memory write.

✓ C67 state.
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opcode operand.

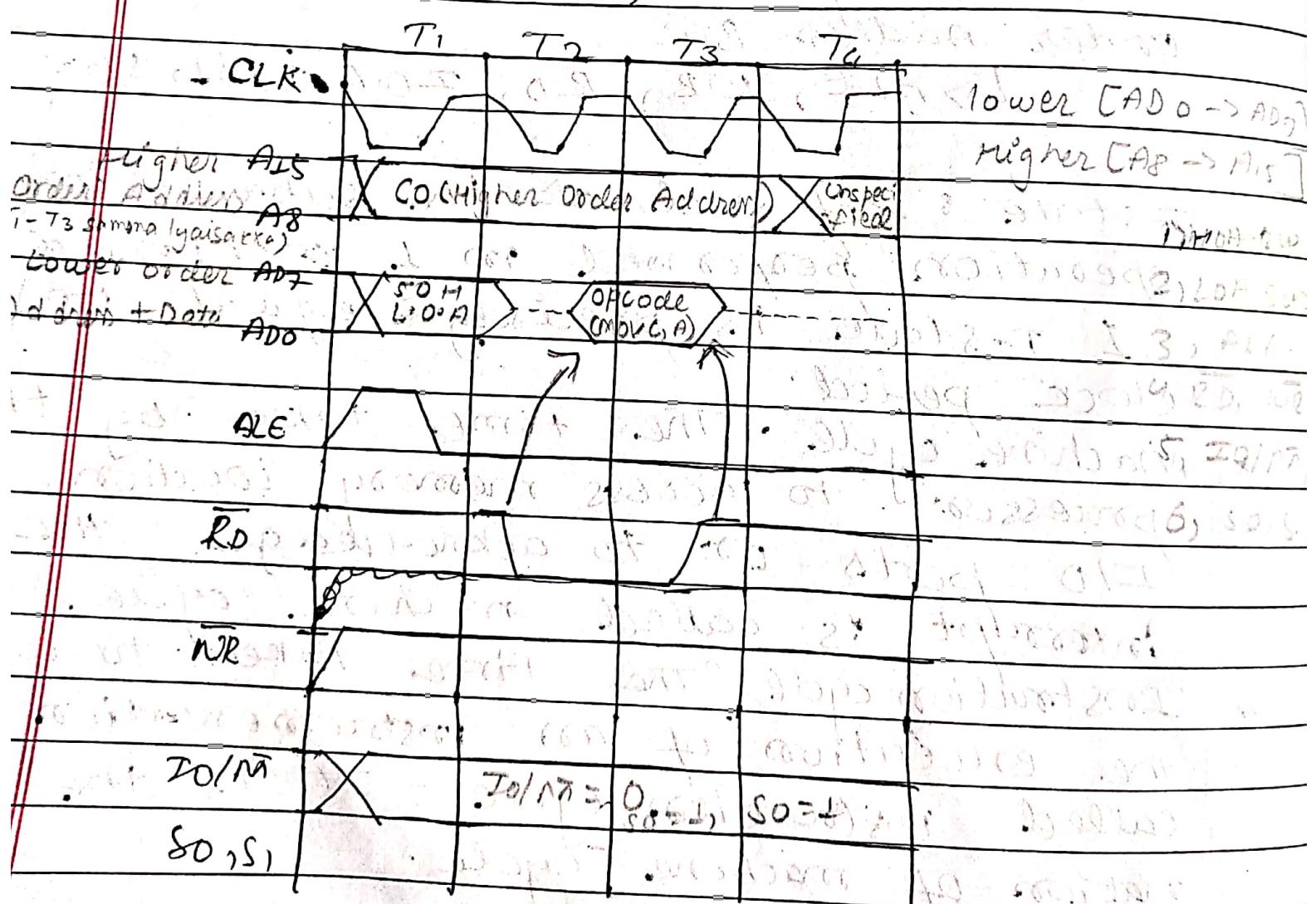
4-T

Machine cycle: MOVA,B

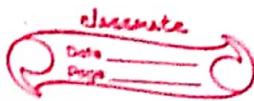
MVI A, 32

STA COSO

Timing diagram of MOVCS A. 1-byte instruction
 → let us assume the address of the instruction is C050: MOVC, A



Timing diagram description.



- The instruction `Mov C, A` is a 1-byte instruction. Therefore the 8085 CPU needs to read this from memory and thus requires 1 machine cycle. At the instruction is just an opcode fetch instruction it requires 4T-states.
- The higher order Address Bus (A8-A15) will carry the MSB of the address which is (C0H) and the cycle or the no of T-states needed to complete the fetching is $T_1 - T_3$. The rest is unspecified.
- The lower order address & data (AD0-AD7) will fetch the LSB of the address which is (50H). Similarly the opcode `Mov C, A` will be fetched during time interval of $T_2 \& T_3$.
- The ALE (Address Latch Enable) goes high during the time period T_1 which indicates the Address has been latched to address & data bus.
- As the opcode is a memory Read signal, the RD goes low when it reads the opcode.
- The CPU identifies that it is an opcode fetch cycle by placing 0, 1, 1 on the IOM & SO, SI status signals.

LDA COSD

STA DOSD

L3-T states

ACC: rajeeko data addresser base main

I/O OUT

memory relative

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Timing diagram for MVI A, 32 H

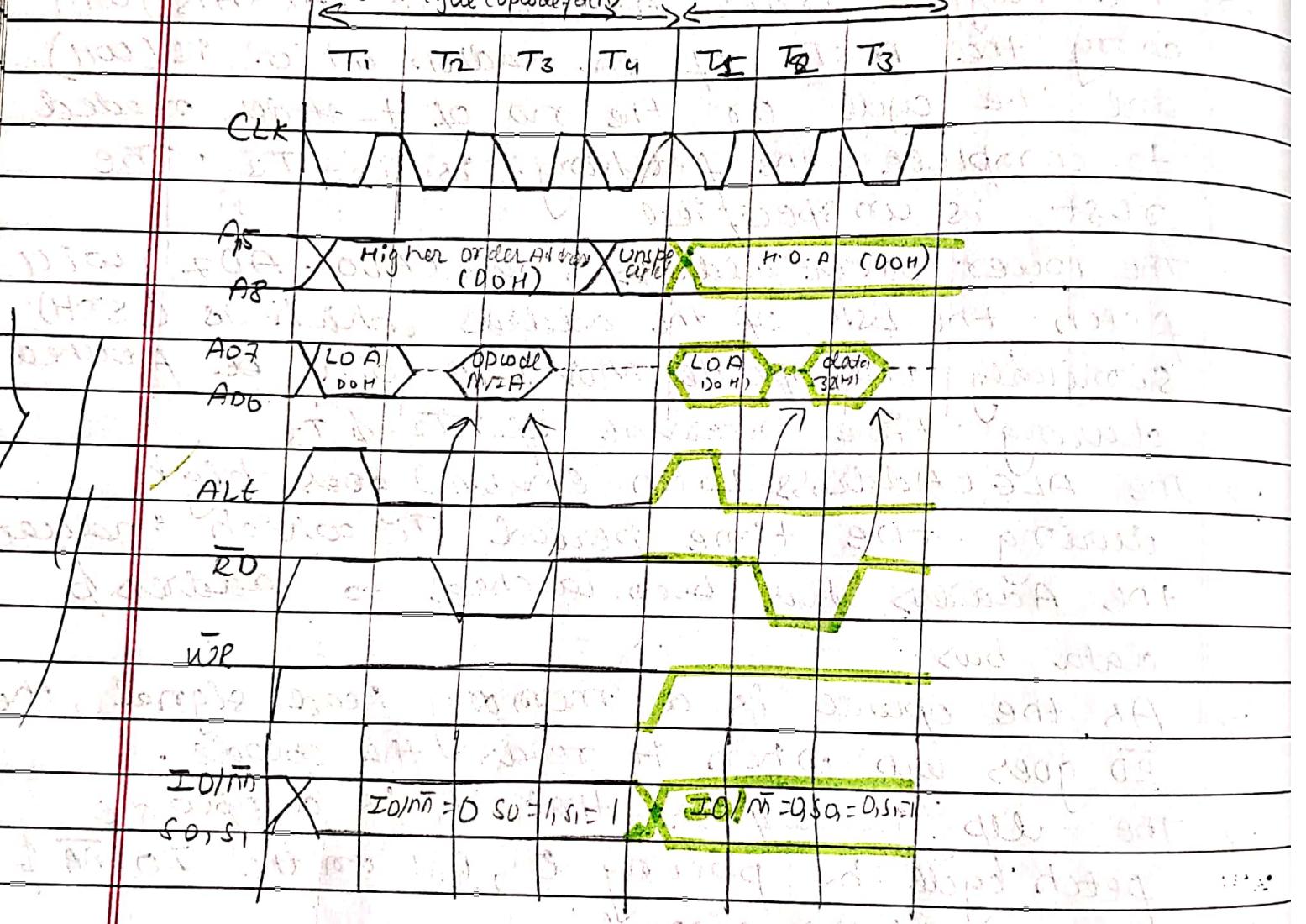
- Let us assume the address of instruction is 0020 : MVI A + op code fetch (4T)

0021 (32) → memory Read (3T)

Instruction cycle

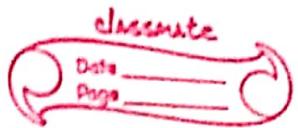
Machine cycle (op code fetch)

Machine cycle (memory read)



Combination of status signal.

Machine cycle	SO	SI	IOM
Op code cycle	1	1	0
Memory Read	0	1	0
Memory write	1	0	0
I/O Read	0	1	→ I/O read IN
I/O write	1	0	→ I/O write OUT



$E050; LDA(4T)$

$E051; S0C3T$

$E052; C0C3T$

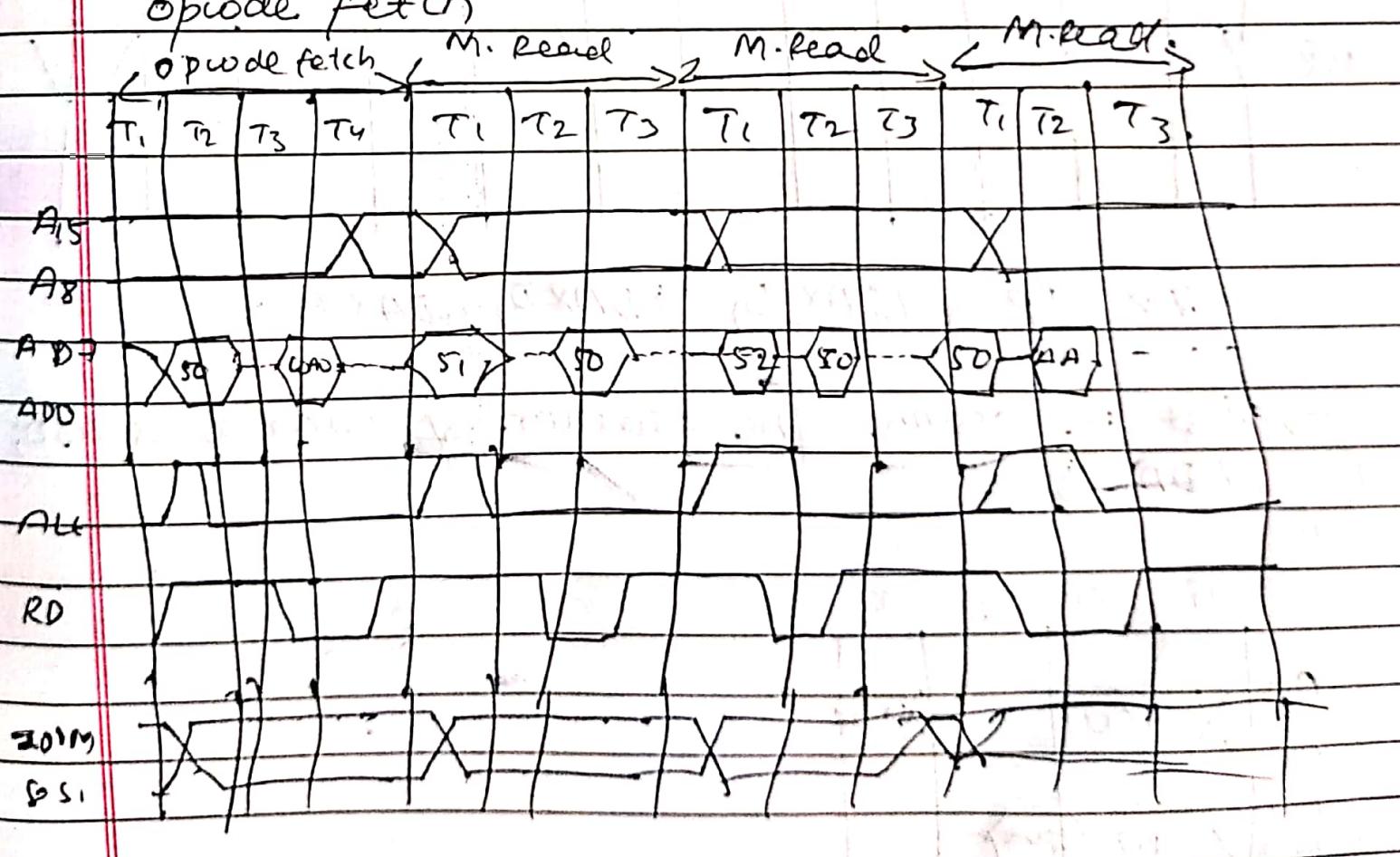
$10T + 3T$

= 13 T-states.

LDA COS0 , let us assume $E050; LAA$

$E051, S0 \quad } 3\text{-byte in}$
 $E052, C0 \quad }$

opcode fetch



Q. Calculate the total execution time for MVI A, 0H.
if the clock frequency is 3MHz.

Soln

Length of instruction \rightarrow 2 Byte.

No. of machine cycles \rightarrow 2 Machine cycle

(Opcode fetch + Memory
Read)

Total no. of T-states \rightarrow 4 T (Opcode fetch) +
3 T (Memory Read)
 \rightarrow 7 T states.

Now, total execution time; Clock period *
no. of T states.

$$\rightarrow 3\text{MHz} * 7$$

$$\rightarrow \frac{1}{3 \times 10^6} * 7$$

$$\rightarrow 0.53333 * 7$$

$$\rightarrow 2.31 \mu\text{s}$$

Individual execution of machine cycle.

Execution time for opcode fetch = $4T$, $T = \frac{1}{f}$
 $4 \times 0.33 = 1.32 \mu\text{s}$.

Execution time memory Read = $3T$
 $= 3 \times 0.33 = 0.99 \mu\text{s}$.