Signal Conversion :-

General considerations of A/D and D/A Conversion :-

A/D and D/A converters relate analog quantities to digital quantities and vice versa through an appropriate code called the Binary code in which a number is represented by

$$N = d_{n-1} \times 2^{n-1} + d_{n-2} \times 2^{n-2} + \cdots + d_2 \times 2^2 + d_1 \times 2^1 + d_0 \times 2^0 \quad \text{—(1)}$$

Where, the coefficients $d_{n-1}, d_{n-2}, \cdots, d_2, d_1, d_0$ assume the values of either 0 or 1.

In a four bit system converter, it permits a number from 0-15. Hence, the maximum count for a four bit converter is $2^4 - 1$. Therefore, for n-bit system, maximum count $= 2^n - 1$.

$$\text{Resolution} = \frac{\text{Weight of LSB}}{\text{Maximum count}} = \frac{2^0}{2^n - 1} = \frac{1}{2^n - 1} \simeq \frac{1}{2^n}$$

If ER be the full range of the converter (reference voltage) then the weight (range) of MSB $= \frac{1}{2} \times$ range of converter

$$= \frac{ER}{2} \text{ and}$$

the weight (range) of the LSB $= \frac{1}{2^n} \times$ range of converter

$$= \frac{ER}{2^n}$$

For a four bit converter having ER as refirance or full range voltage, the analog output for different digital inputs are given as follows:

Digital inputs	Analog outputs
1000	$ER/2$
0100	$ER/2^2$
0010	$ER/2^3$
0001	$ER/2^4$

If all bits are high i.e. input is 1111, then the analog output can be obtained by superposition theorem i.e.

$$E_0 = \frac{E_R}{2} + \frac{E_R}{2^2} + \frac{E_R}{2^3} + \frac{E_R}{2^4}$$

$$= E_R\left(1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}\right)$$

$$= E_R\left(d_3 2^{-1} + d_2 2^{-2} + d_1 2^{-3} + d_0 2^{-4}\right)$$

$$= \frac{E_R}{2^4}\left[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0\right]$$

Hence, for n-bit system, output voltage (analog) is given by

$$E_0 = \frac{E_R}{2^n}\left[d_{n-1} 2^{n-1} + d_{n-2} 2^{n-2} + \cdots + d_0 2^0\right]$$

Example:- Find out the analog output for a digital input of 1010 if the reference voltage is 8 volt.

Soln: we know,

$$E_0 = \frac{E_R}{2^4}\left[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0\right]$$

$$= \frac{8}{16}\left[1\times2^3 + 0\times2^2 + 1\times2^1 + 0\times2^0\right]$$

$$= \frac{1}{2}(8+2) = \frac{10}{2} = 5 \text{ volts.}$$

Analog to Digital converters (ADC):-

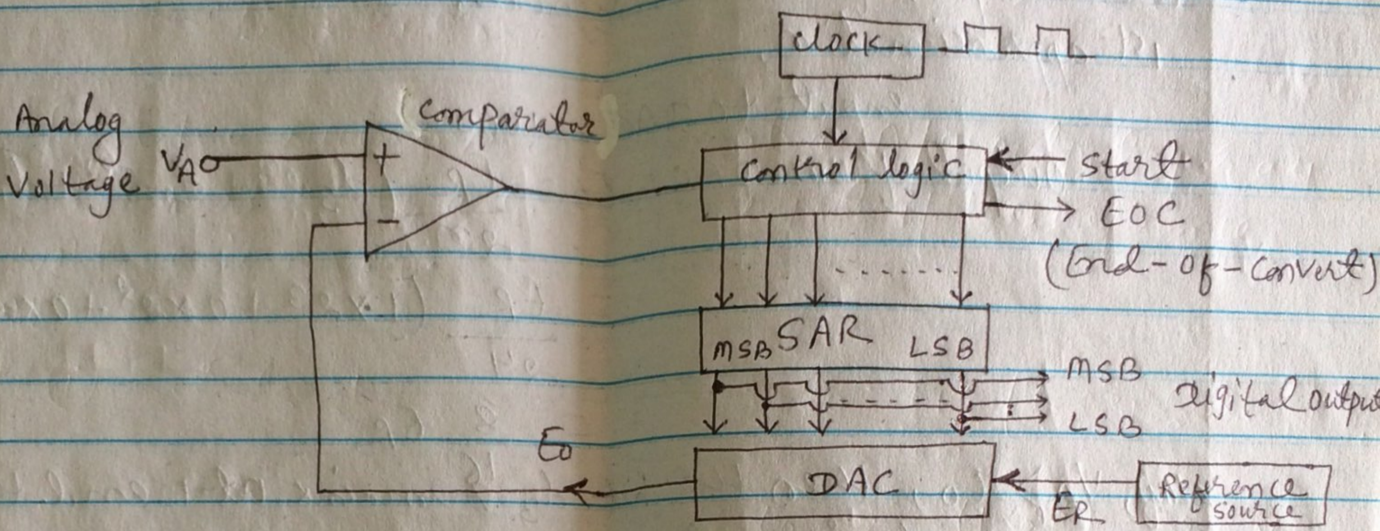
Why analog signal is converted to digital form?

(i) most of the real world physical quantities such as voltage, current, temperature, time etc. are available in analog form. But it is difficult to process, store or transmit them without introducing considerable error. So, for processing, transmission and storage purposes, it is often convenient to express these variables into digital form.

(ii) Digital form gives better accuracy and reduces noise.

Bhattarai

(i) Successive Approximation ADC (potentiometric type):-



Successive approximation ADC consists of comparator, control logic, SAR (Successive Approximation Resistor), DAC and Reference source.

V_A represents the analog input voltage. When START button is pressed, SAR sets the MSB high i.e. 1 with all other bits to zero so that the trial code becomes 1000 (for 4 bit). DAC converts the trial code into analog equivalent. The analog equivalent output of DAC is given as

$$E_0 = \frac{E_R}{2^n}\left[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + \cdots + d_0 2^0\right]$$

for n-bits

E_0 is compared with V_A by comparator.

If $V_A > E_0$, then SAR lefts MSB at 1 and makes the next lower significant bit 1 and further compares.

If $V_A < E_0$, then SAR resets MSB at 0 and makes the next lower significant bit 1. This procedure is continued for all subsequent bits one at a time until all bit positions have been tested.

When $V_A = E_0$, the comparator changes the state and this can be taken as the End-of-Conversion (EoC).

For example, for 4-bits signal,

1st approximation,

input to DAC = 1000

$$\text{output from DAC} = E_0 = \frac{E_R}{2^n}\left[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0\right]$$

$$= \frac{E_R}{2^4}\left[1\times2^3 + 0\times2^2 + 0\times2^1 + 0\times2^0\right]$$

$$= \frac{8}{16} E_R$$

Now, $V_A > E_0$, then the bit d_3 remains at 1 and the next bit i.e. d_2 is set to 1.

2nd approximation,

input to DAC = 1100

$$\text{output from DAC} = E_0 = \frac{E_R}{2^4}\left(1\times2^3 + 1\times2^2\right) = \frac{12}{16} E_R$$

Now, $V_A < E_0$, then the bit d_2 is reset to 0 and the next bit i.e. d_1 is set to 1.

3rd approximation,

input to DAC = 1010

$$\text{output from DAC} = E_0 = \frac{E_R}{16}\left(1\times2^3 + 1\times2^1\right) = \frac{10}{16} E_R$$

Now, $V_A > E_0$, then the bit d_1 remains at 1 and the next bit d_0 is set to 1.

4th approximation,

input to DAC = 1011

$$\text{output from DAC} = E_0 = \frac{E_R}{16}\left(1\times2^3 + 1\times2^1 + 1\times2^0\right) = \frac{11}{16} E_R$$

Now, $V_A < E_0$, then the bit d_0 is reset to 0 and digital equivalent of the analog input voltage will be

$$d_3 d_2 d_1 d_0 = 1010$$

Q: Find the successive approximation A/D output for a 4 bit converter to a 3.217 volt input if the reference voltage is 5 volt.

Soln:

(i) set $d_3 = 1$ $\quad \therefore$ output $= E_0 = \frac{E_R}{2^n}\left[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0\right]$

$$\Rightarrow E_0 = \frac{5}{2^4}(1\times 2^3) = 2.5\text{V}$$

Now, $3.217 > 2.5$ and $\therefore$ set $d_3 = 1$

(ii) set $d_2 = 1$ $\quad \therefore$ output $(E_0) = \frac{5}{16}(1\times 2^3 + 1\times 2^2) = \frac{5}{16}\times 12 = 3.75\text{V}$

Now, $3.217 < 3.75$ and $\therefore$ set $d_2 = 0$

(iii) set $d_1 = 1$ $\quad \therefore$ output $(E_0) = \frac{5}{16}(1\times 2^3 + 1\times 2^1) = \frac{5}{16}\times 10$

$$= 3.125\text{ V}$$

Now, $3.217 > 3.125$ and $\therefore$ set $d_1 = 1$

(iv) set $d_0 = 1$ $\quad \therefore$ output $(E_0) = \frac{5}{16}(1\times 2^3 + 1\times 2^1 + 1\times 2^0)$

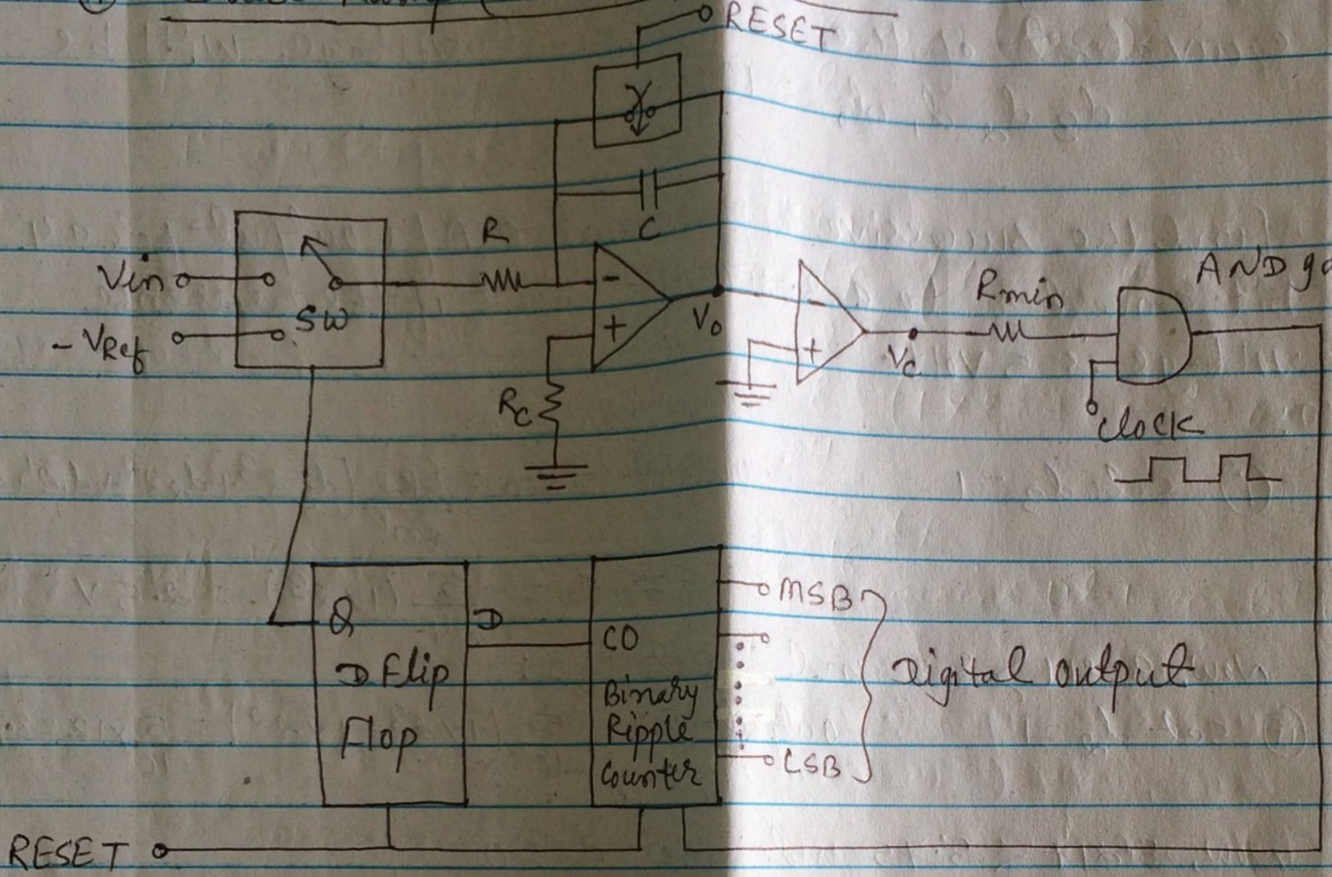
$$= \frac{5}{16}\times 11 = 3.4375\text{ V}$$

Now, $3.217 < 3.4375$ and $\therefore$ set $d_0 = 0$

Thus, the output of A/D converter is: 1010.

Successive Approximation Type ADC are widely applied because of their combination of high resolution and speed. They can perform conversions within 1 to 50 micro seconds rather than the miliseconds required by stair case Ramp, Dual slope and Voltage to frequency converter types. However, they are more expensive than ... slower types.

(ii) Dual Ramp (Dual slope) ADC :-



The circuit diagram shows the integrating type Dual Ramp (Dual slope) ADC. It performs conversion in an indirect manner by first changing analog input to a linear function of time or frequency and then to a digital code. Dual slope ADC is the most widely used Integrating type ADC.

Binary counter is RESET and it results 0000 digital output (4 bits). Switch (SW) moves to 0 position and Vin is fed to an Integrator which produces a Ramp output waveform ($V_0 = -\frac{V_{in}}{T} \times t$). The capacitor charges. The Ramp signal starts at zero and increases for a fixed interval of time T_1, equal to the maximum count of the counter multiplied by the clock frequency. The slope of the ramp signal is proportional to Vin. It results V_C (comparator output) high. AND gate enables and the counting starts (0000 ...... 1111) where $2^n - 1$ pulses are applied.

For pulse 2^n i.e. at the end of the interval T_1, counter resets. Carry Bit (CO) of the ripple counter causes the switch to move to $-V_{Ref}$ position. In this position, a constant current $-V_{Ref}/R$ begins to discharge the capacitor. The count continues until capacitor C being discharged completely i.e. $V_0 < 0$. As V_0 becomes positive, V_C becomes low which disables AND gate and counting stops. The resultant count is proportional to the input voltage V_{in}.

Advantages:-

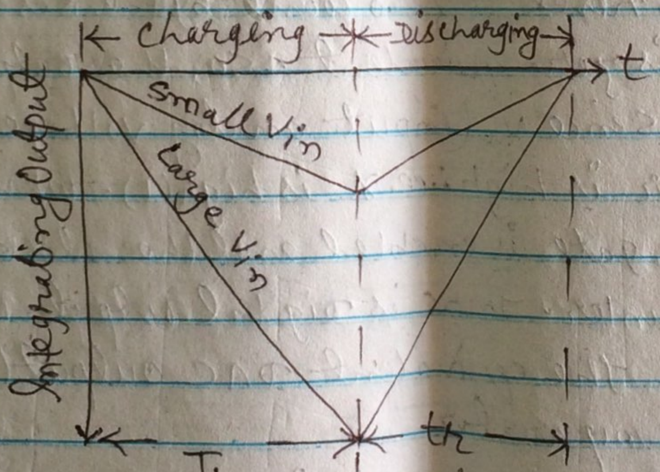
The main advantages are:

→ Good accuracy of conversion and

→ Low cost.

Disadvantages:-

→ Slow speed of operation.



Fixed no. of clock pulses

No. of pulses proportional to V_{in}

Now, $Q_{charging} = Q_{discharging}$

$$\frac{iT_1}{C} = \frac{it_2}{C} \quad \text{or,} \quad \frac{V_{in}}{R} T_1 = \frac{V_{Ref}}{R} t_2$$

$$\text{or,} \quad V_{in} = V_{Ref}\left(\frac{t_2}{T_1}\right) \quad \therefore \boxed{V_{in} \propto t_2} \text{ i.e.}$$

the count recorded is proportional to the input voltage.