

Chapter: Semiconductor Material Procession

Reasons why the Silicon has wide spread use, dominating Germanium:

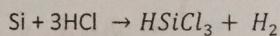
1. The structure of Germanium crystals would be destroyed at higher temperature. However, Silicon crystals are not easily damaged by excess heat.
2. Silicon is less expensive due to the greater abundance of element. The major raw material for Silicon wafer fabrication is sand and there is lots of sand available in nature.
3. The forbidden energy band of Silicon is 1.1eV which is higher than that of germanium (0.66eV) which makes silicon more stable.
4. It is easy for doping by impurities.
5. Si has quick response to solar radiation and light.
6. While high power applications are taken into account, Si based devices can tolerate high power (more than 50W), while Ge can survive applications under 10W only.
7. Germanium has a reverse breakdown voltage of 50-70V while Si can withstand up to 100V. While requiring the necessity to block reverse voltage, it is advantageous to have one that can withstand more voltage.

Crystal Growing:

Pure Silicon is required for many applications. However, nature does not provide a pure form of it, rather compound Silicon is abundant. So, to obtain pure Silicon crystal, following processes are adapted.

Firstly, SiO_2 is heated to high temperature in an appropriate environment to produce almost pure Silicon in powder form.

Secondly, the silicon powder is reacted with HCl gas that gives Trichlorosilane (HSiCl_3) gas.



It is then distilled and reduced with hydrogen to form polycrystalline Silicon.

Finally, the Polycrystalline silicon is melted and cast into ingots, from which the single crystal is obtained.

The basic two methods to obtain pure silicon crystal from polycrystalline silicon are:

1. Float zone refining and crystal growth.
2. Czochralski growth.

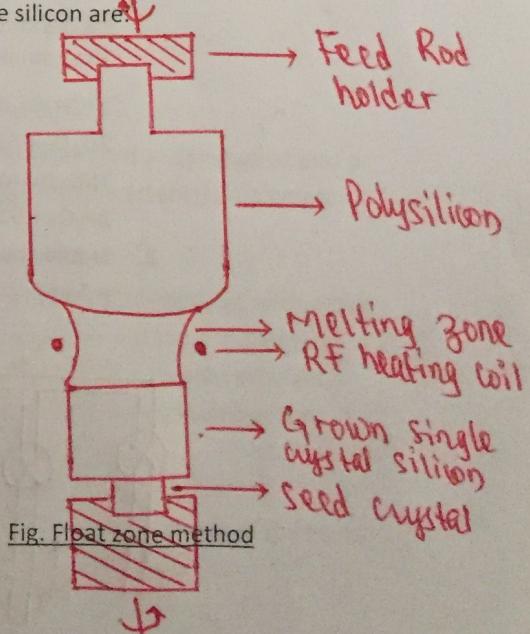
- **Floating zone method of crystal growth:**

This method produces not only a single crystal, but also removes impurities.

It consists basically

of a seed crystal, polycrystalline silicon and radio frequency (RF) heating coil.

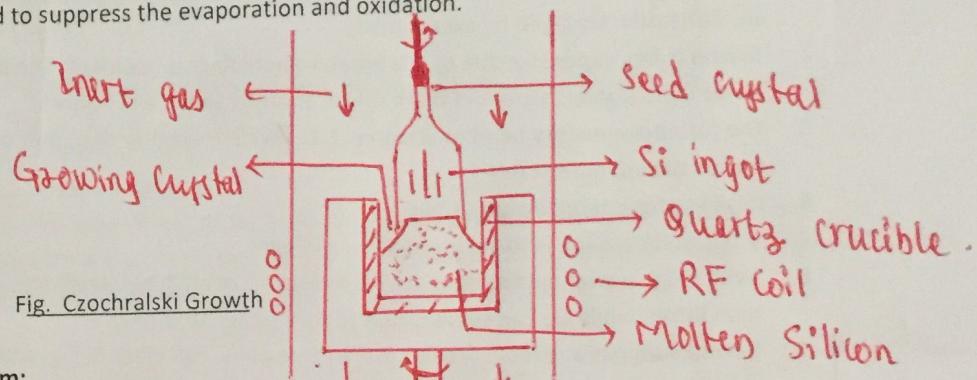
The RF coil heats the crucible inside which the polycrystalline silicon is melted. Then, it is moved slowly towards the seed crystal to produce a wafer of single bigger silicon crystal. It is then cooled by pulling outside the crucible.



- **Czochralski growth:**

In this method, the polycrystalline Si is melted inside the Quartz crucible by RF coil. The seed crystal is lowered to touch the melt, which grows larger single crystal. Then, it is slowly pulled out of the melt by rotating and finally solidified.

Inert gas is used to suppress the evaporation and oxidation.



- **Methods of doping:**

Diffusion system:

This system consists of an open furnace tube, inside which quartz boat is situated. The silicon wafer is located vertically in the boat. The dopant (impurity like Arsenic, Phosphorus etc) is carried towards the highly heated silicon wafer in vaporized form. The dopant may be in solid, liquid or in gaseous form.

1. **Solid source:** The carrier gases N₂ or O₂ pick up the vapor of dopant from the solid source and transport it to the furnace tube. Those vapors are deposited on the surface of the Silicon wafer.

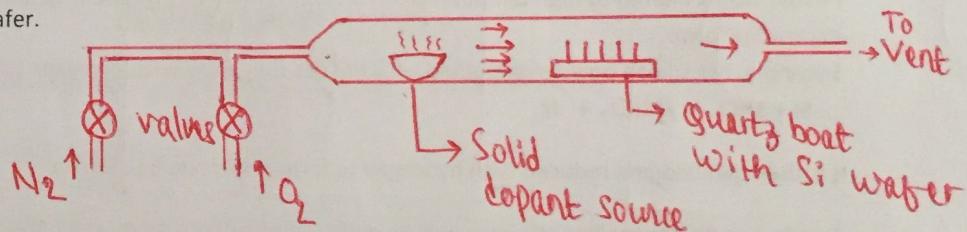
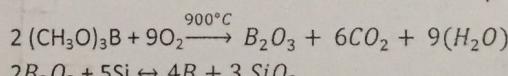
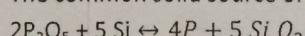


Fig. Open furnace tube diffusion for solid impurity source

The common solid source of Boron is Trimethyl Borate.



The common solid source of Phosphorus is Phosphorus Pentoxide.



2. **Liquid source:** The carrier gas passing through the liquid dopant source, picks up the source in vapour form into the furnace tube where it reacts with the surface of the silicon wafer.

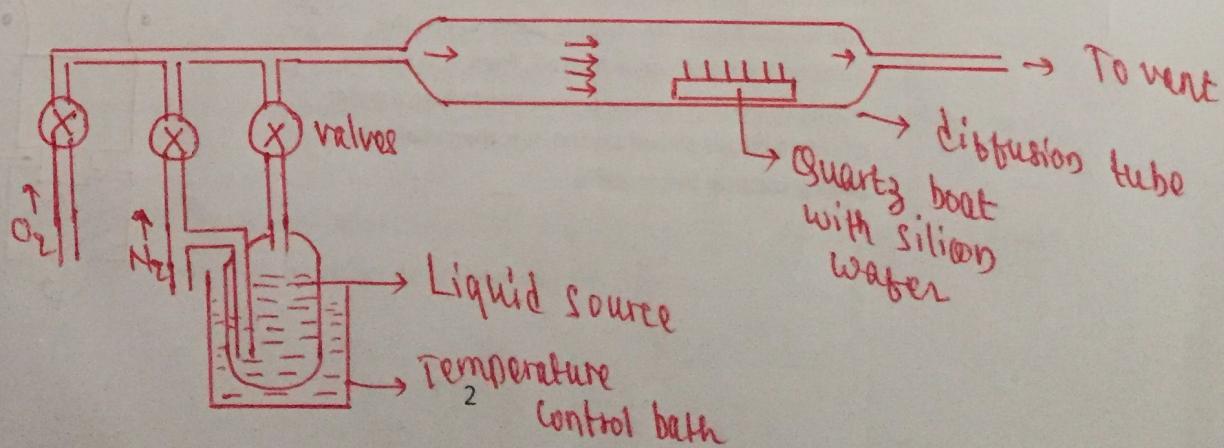
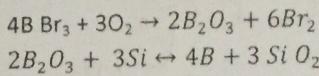
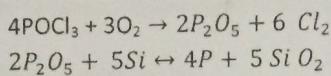


Fig. Diffusion of liquid dopant in open furnace tube
 The most common liquid source of Boron is Boron Tribromide.

The reaction is



The Common liquid source of Phosphorus is Phosphorus Oxichloride.



3. **Gas source:** The dopant source are directly supplied to the furnace tube. Since the gas source is extremely toxic, an additional system is required to ensure that all the source gas is removed before and after the wafer is entered or removed from the furnace.

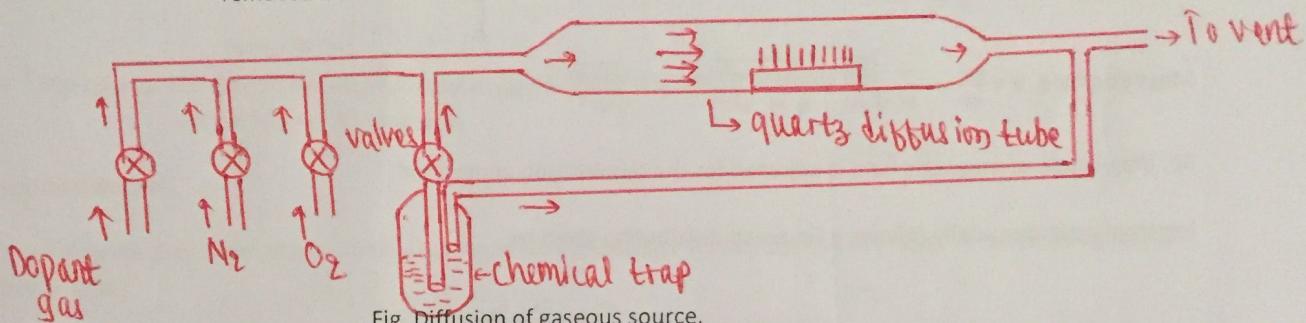
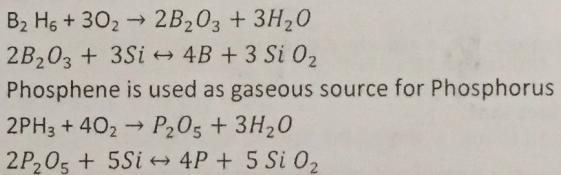


Fig. Diffusion of gaseous source.

The common gaseous source of Boron is Diborane. The reaction is,

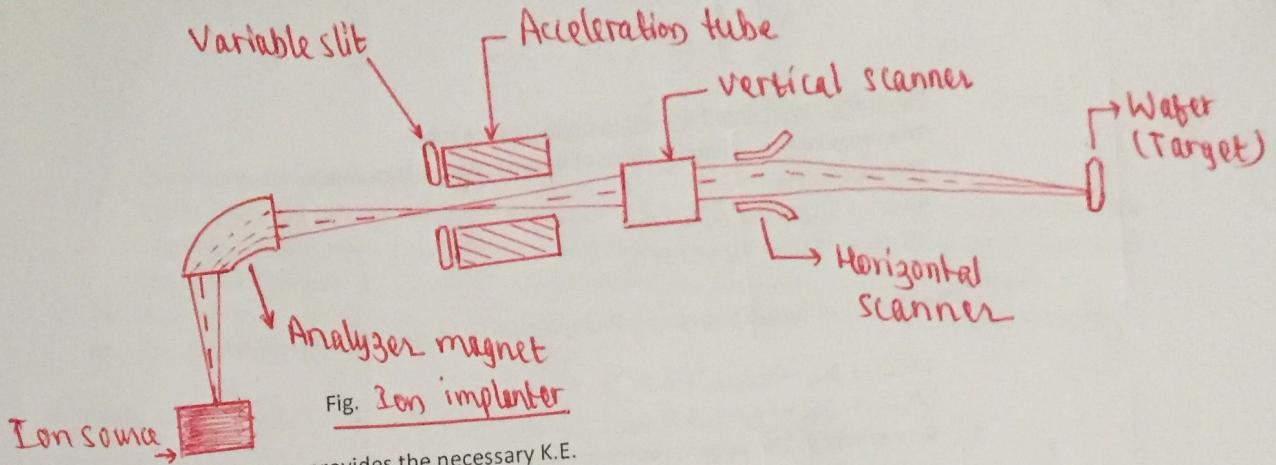


Ion Implantation:

It is the engineering process in which the ions of a material are accelerated in an electric field and impacted into a solid to change the properties of a solid. Semiconductor doping with boron, phosphorus, or arsenic is a common application of ion implantation.

The equipment consists of desired impurity as an ion source in plasma form. These ions are accelerated with a high voltage (20 KV to 250KV) accelerator. The highly accelerated ions impinge on a target material to be implanted with the impurity ions. An analyzer magnet bends the selected ion beam into right angle. The scanner provides necessary deflection to give a uniform implantation and to build up the desired dose. The target chamber has silicon wafer.

The centrifugal force is balanced by magnetic force. ie. $Bqv = \frac{mv^2}{r} \Rightarrow B = \frac{mv}{qr} \Rightarrow r = \frac{mv}{Bq}$ (i) i.e. radius of the beam depends upon the mass. So, selected ion beam can be allowed to pass.



And, the electrostatic energy provides the necessary K.E.

$$\text{i.e. } qV = \frac{1}{2}mv^2 \Rightarrow v = \sqrt{\frac{2qV}{m}}$$

$$\text{Magnetic field, } B = \frac{mv}{qr} = \frac{m}{qr} \sqrt{\frac{2qV}{m}} = \sqrt{\frac{2qV}{m} \frac{m^2}{q^2r^2}} \Rightarrow B = \sqrt{\frac{2mV}{qr^2}} \dots \text{(ii)}$$

So, magnitude of magnetic field is adjusted for the required ion of mass 'm'.

Ion implantation usually follows a Gaussian distribution given by,

$$N(x) = N_p e^{-\frac{(x - R_p)^2}{2\Delta R_p^2}}$$

Where, $N(x)$ = impurity concentration.

N_p = Peak concentration. R_p = projected range. ΔR_p = standard deviation called straggle.

Wide use of this process is due to the fact that:

- a. The target chamber is maintained at relatively low temperature during implantation that prevents undesired spreading of impurities by diffusion.
- b. This process is useful for very large scale fabrication.
- c. A wide range of impurities can be implanted.
- d. The dose and depth of implantation can be precisely controlled.

Lattice damage and annealing in Ion implantation:

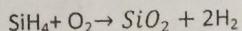
There may be so many defects and damaging in the target crystal on impact during ion implantation, such as vacancies and interstitials. It is called lattice damaging.

The recovery of lattice damaging is done by heating the wafer to about 900°C for few minutes and cooled slowly. This recovery is called annealing.

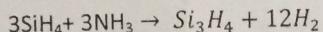
Chemical vapor deposition (CVD):

CVD is a technique of depositing thin films of materials on a wafer or substrates. In this process, the substrate is placed inside a reactor where thermal decomposition and chemical reaction takes place between source gases. The product is a solid which condenses on the surface of the wafer.

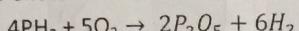
- For silicon, the CVD process is the synthesis of polycrystalline silicon from Silane (SiH_4) gas, using the reaction, $\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$
- Silicon dioxide can be deposited by using Silane and Oxygen. The reaction is,



- Silicon nitride is often used as insulator and chemical barrier in manufacturing integrated circuits.



- Phosphorus Pentaoxide can be deposited by using Phosphine and oxygen gas as,



Epitaxial Growth:

It refers to the deposition of a crystalline overlayer on a crystalline substance. The overlayer is called an epitaxial film or layer.

- The vapor phase epitaxy (VPE) is a modification of chemical vapor deposition, commonly used to deposit Silicon.
$$\text{SiCl}_4 \text{(gas)} + 2\text{H}_2 \leftrightarrow \text{Si(solid)} + 4\text{HCl(gas)}$$
This reversible reaction takes place in 1200 to 2500°C.
- In liquid phase epitaxy (LPE), into the melt of material to be deposited. The substrate acts as a seed for material crystallizing directly from the melt.
- Solid phase epitaxy (SPE) is usually done by first depositing a film of amorphous material on a crystalline substrate. This substrate is then heated to crystallize the film.
- Molecular beam Epitaxy (MBE) is done by heating source material to produce an evaporated beam of particles. These particles travel through a very high vacuum to the substrate where they condense. Substrate temperature ranges from 400 to 900°C.

Photolithography:

Lithography refers to the term "writing on stones". It is the process which involves photographic transfer of a pattern to the surface of wafer to make diffusion window by etching. A geometrical pattern is transferred from a mask to the surface of Silicon wafer.

Step 1: Coat Si with oxide then with photo resist.

For this, the silicon single crystal is oxidized in an oxidation furnace to form a thin layer of SiO_2 . Then, the wafer is coated with a radiation sensitive polymer film called the photo resist. Finally, the silicon wafer is spun rapidly for the uniform coating.

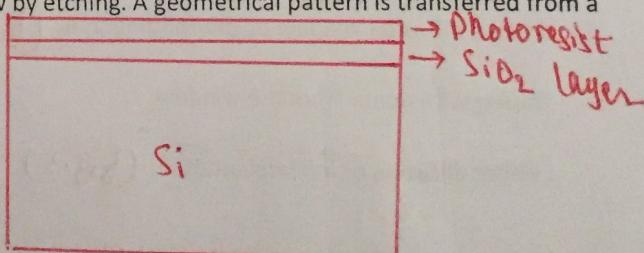
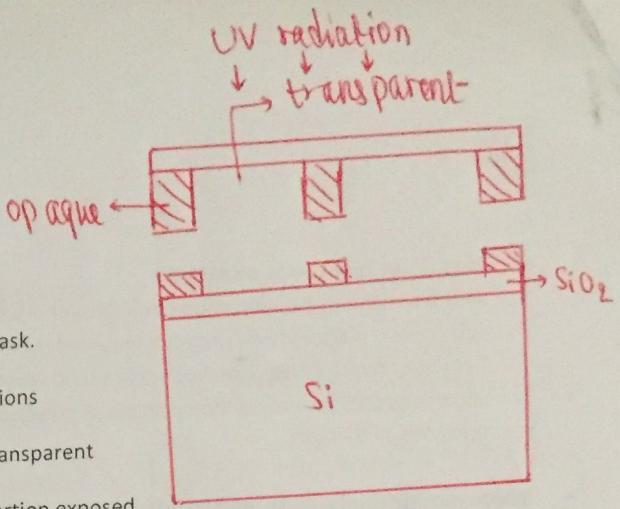


Fig.(1)

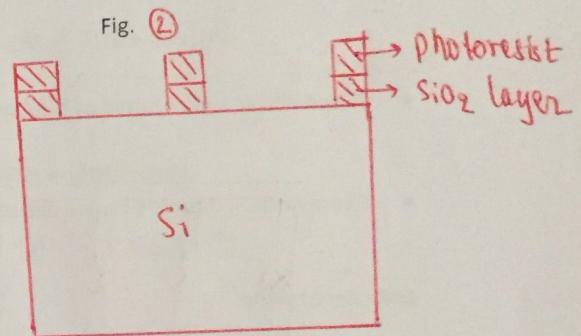


Step 2: Expose to radiation and develop the pattern.

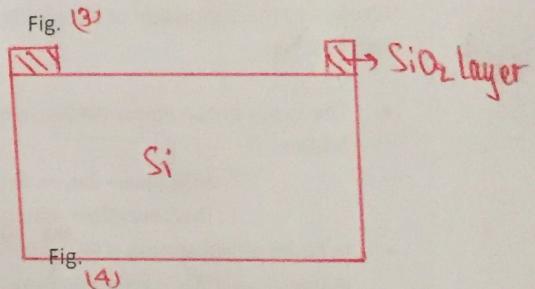
Allow the UV radiation to fall on photo resist through mask.

A mask is a glass plate with transparent and opaque regions made on it. Only those regions of the mask which are transparent allow radiation to fall on the semiconductor. And the portion exposed to radiation change their properties.

Step 3: The substance is kept in diluted etching solution, the SiO_2 from the Si regions corresponding to transparency of mask is removed.



Step 4: All the photo resist is removed by keeping it on photo resist remover solution.

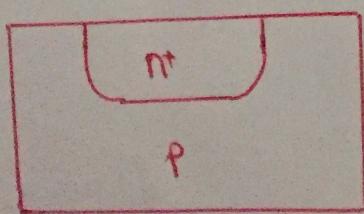
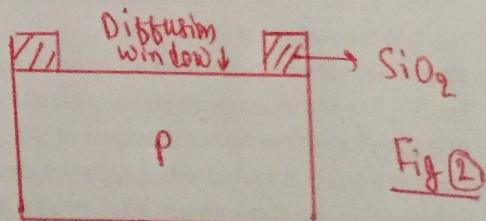
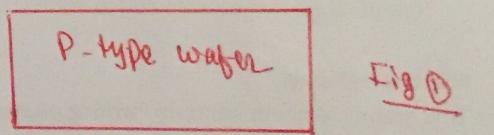


SiO_2 is an excellent insulating material. It has good masking properties. The region which is not to be doped is masked with SiO_2 . It does not allow dopant to pass through it.

- Monolithic IC Fabrication:**

The fabrication of IC is done plane by plane at the wafer. We consider fabrication of a npn junction transistor.

1. First, take a P-type single crystal (substrate). (Fig. 1)
2. Make a diffusion window by photolithography. (Fig. 2)
3. Doping with donor from the window (either diffusion or ion implantation) (Fig. 3)
4. Removing the oxide layer by etching. (Fig. 4)



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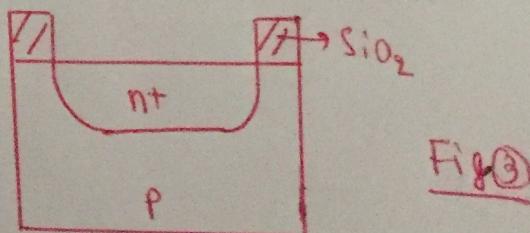
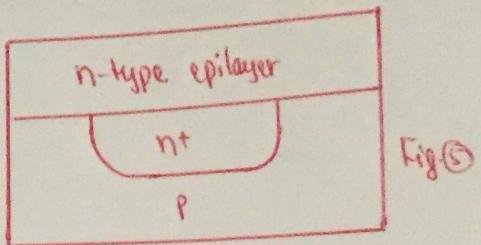


Fig. ④

5. Growing a n-type epilayer on the top by etching. (Fig. 5)
6. Grow SiO₂ layer and then etching window on either sides. (Fig. 6)
7. Diffuse acceptor dopants heavily through the windows. (Fig. 7)
8. Removing SiO₂ layer by etching, doping acceptors over n-region to form P-region for base diffusion. (Fig. 8)



9. Again, dope donors to form emitter. (Fig. 9)
10. Metallization: It involves deposition of metal for external electrical connections. The E, B, C, are metal connectors for emitter, base and collector of npn transistor so formed. (Fig. 10)

