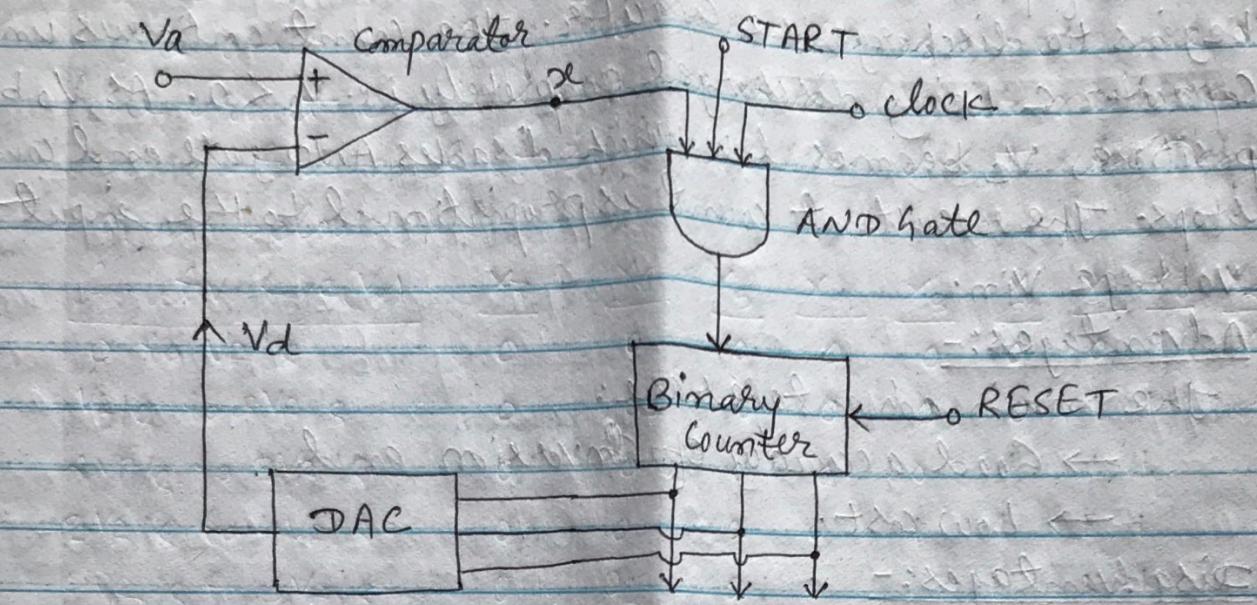


(iii) Staircase Ramp type (Counting type) ADC:-



Binary Counter is reset to zero count by the Reset Pulse. The digital output is zero equivalent. So, the output of DAC is zero i.e. $V_d = 0$. Since V_a (input analog voltage) $> V_d$, output of the comparator is high i.e. π is high(1). When START button is pressed, AND gate is enabled and the clock pulse is counted by the Binary Counter. There is digital output. But the counting does not stop here. The equivalent DAC output (V_d) is compared with V_a by the comparator.

If $V_a > V_d$, π is high. AND gate is enabled. The clock pulses are passed through the AND gate and counted by the Binary Counter. Digital output is obtained which are fed to the computer or any other digital signal processing.

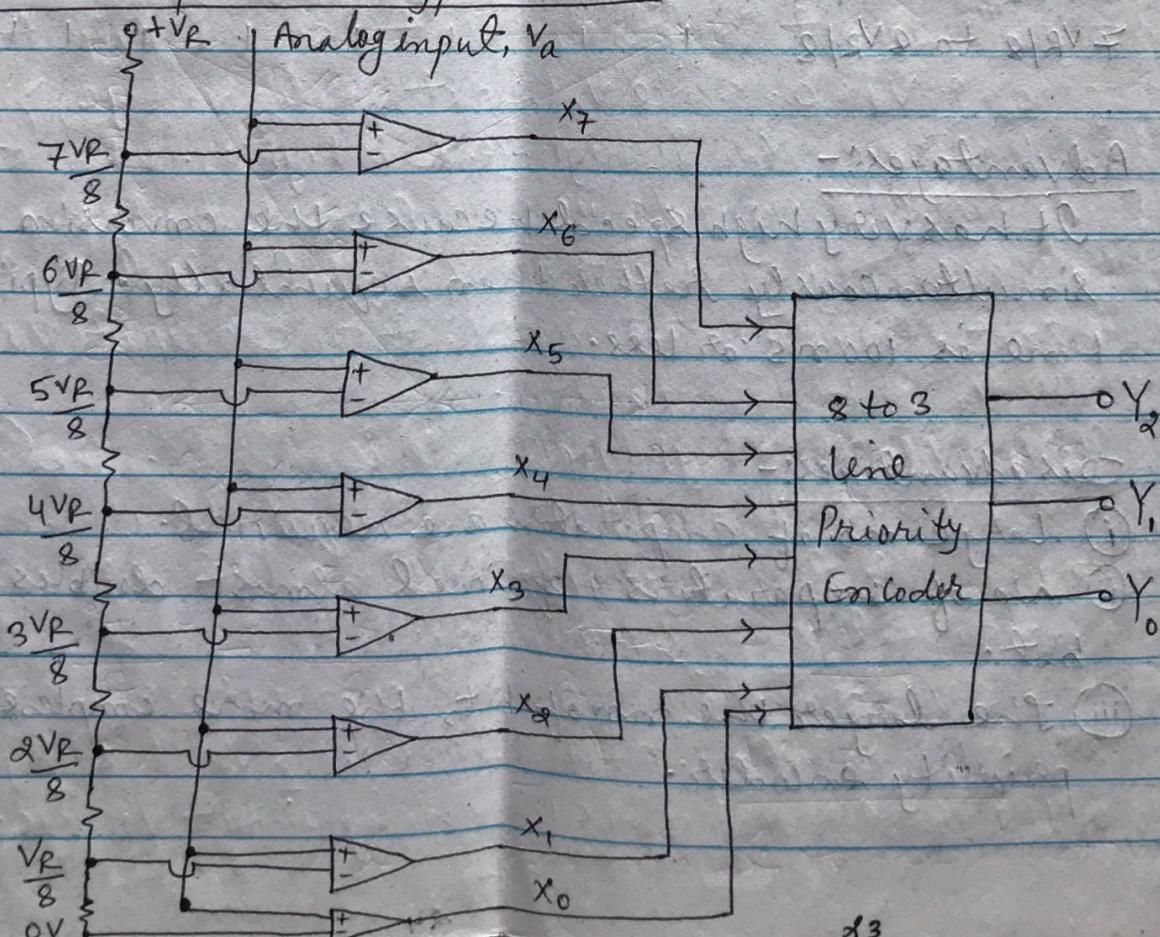
If $V_a < V_d$, π is low i.e. 0 and AND gate is disabled. This stops the counting. At the time $V_d > V_a$, the digital output of the counter represents the analog input voltage.

For a new value of analog input V_a , a second RESET pulse is applied to clear the counter. Upon the end of the RESET and with START button on, the counting begins again.

Serious Drawbacks:-

- (i) The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond.
- (ii) When $V_a > V_d$, x is high and AND gate is enabled and counter counts and digital output is one bit more than the exact value. To remove this problem, we can use Up/Down counter. In this process, when DAC output is more than V_a , the counter reverses the direction and count down by one count and it decreases the count by 1 LSB.

(iv) Flash or parallel Type ADC :-



The circuit diagram of the 3 bit parallel Type (Flash Type) ADC is shown above. In this technique, the input voltage is fed simultaneously to one input of each comparator. The other input of the comparator is a reference voltage. The circuit consists of a resistive divider network, 8 opamp comparators and 8 to 3 line encoder. Its Truth Table is given below:

<u>Input Voltage (V_A)</u>	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	y_2	y_1	y_0
0 to $VR/8$	0	0	0	0	0	0	0	1	0	0	0
$VR/8$ to $2VR/8$	0	0	0	0	0	0	1	1	0	0	1
$2VR/8$ to $3VR/8$	0	0	0	0	0	0	1	1	0	1	0
$3VR/8$ to $4VR/8$	0	0	0	0	1	0	1	1	0	1	1
$4VR/8$ to $5VR/8$	0	0	0	1	1	1	1	1	1	0	0
$5VR/8$ to $6VR/8$	0	0	1	1	1	1	1	1	1	0	1
$6VR/8$ to $7VR/8$	0	1	1	1	1	1	1	1	1	1	0
$7VR/8$ to $8VR/8$	1	1	1	1	1	1	1	1	1	1	1

Advantages:-

It has very high speed because the conversion takes place simultaneously rather than sequentially. Typical conversion time is 100ns or less.

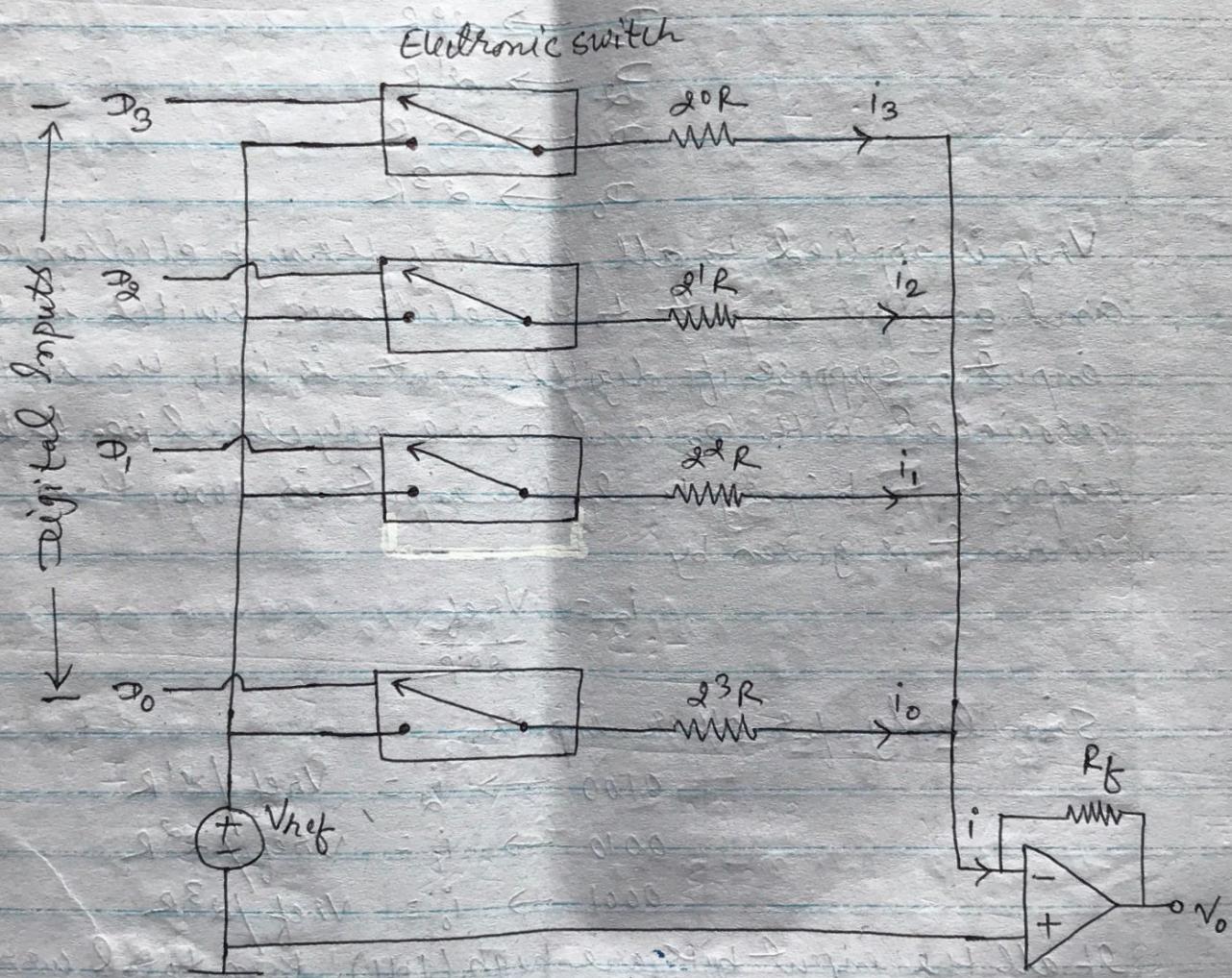
Disadvantages:-

- (i) Large no of comparators are required.
- (ii) No. of comparators required almost doubles for each added bit.
- (iii) The larger the no. of bit, the more complex is the priority encoder.

Digital to Analog converters (DAC) :-

Typical applications of DAC include microcomputer interfacing, CRT graphics generation, Programmable power supplies, digitally controlled gain circuits, digital filters etc.

(i) Weighted Resistor Network (WRN) DAC :-



In the WRN DAC, the resistance are weighted reverse eight binary system i.e. the resistance associated with the MSB has the least value and as we move from MSB to LSB, the resistance value increases by a factor of 2 as shown.

Let resistance associated with MSB for n-bit is R i.e.

$$D_{n-1} \rightarrow 2^0 R$$

$$D_{n-2} \rightarrow 2^1 R$$

$$D_{n-3} \rightarrow 2^2 R$$

$$D_0 \rightarrow 2^{n-1} R$$

Hence, for n -bit system, we have

$$D_3 \rightarrow 2^0 R$$

$$D_2 \rightarrow 2^1 R$$

$$D_1 \rightarrow 2^2 R$$

$$D_0 \rightarrow 2^3 R$$

V_{ref} is applied to all resistors through electronic switches and another input to the electronic switch is the digital input. Suppose if digital input is 1001, the switches associated with D_3 and D_0 are only closed i.e. these switches respond to binary 1. If the input is 1000, then the current is given by

$$i_3 = \frac{V_{ref}}{2^0 R}$$

Similarly for other inputs,

$$0100 \rightarrow i_2 = \frac{V_{ref}}{2^1 R}$$

$$0010 \rightarrow i_1 = \frac{V_{ref}}{2^2 R}$$

$$0001 \rightarrow i_0 = \frac{V_{ref}}{2^3 R}$$

If all the input bits are high (1111), then total current i can be obtained by superposition theorem.

$$i = i_3 + i_2 + i_1 + i_0 \\ = \frac{V_{ref}}{R} (1 + 1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3})$$

$$= \frac{V_{ref}}{2^3 R} (1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$$

$$= \frac{V_{ref}}{2^3 R} (D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0)$$

Advantages:-

- Easy principle / construction.
- Fast conversion.

$$V_o = -iR_f = \frac{-V_{ref} \times R_f}{2^3 R} (D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0)$$

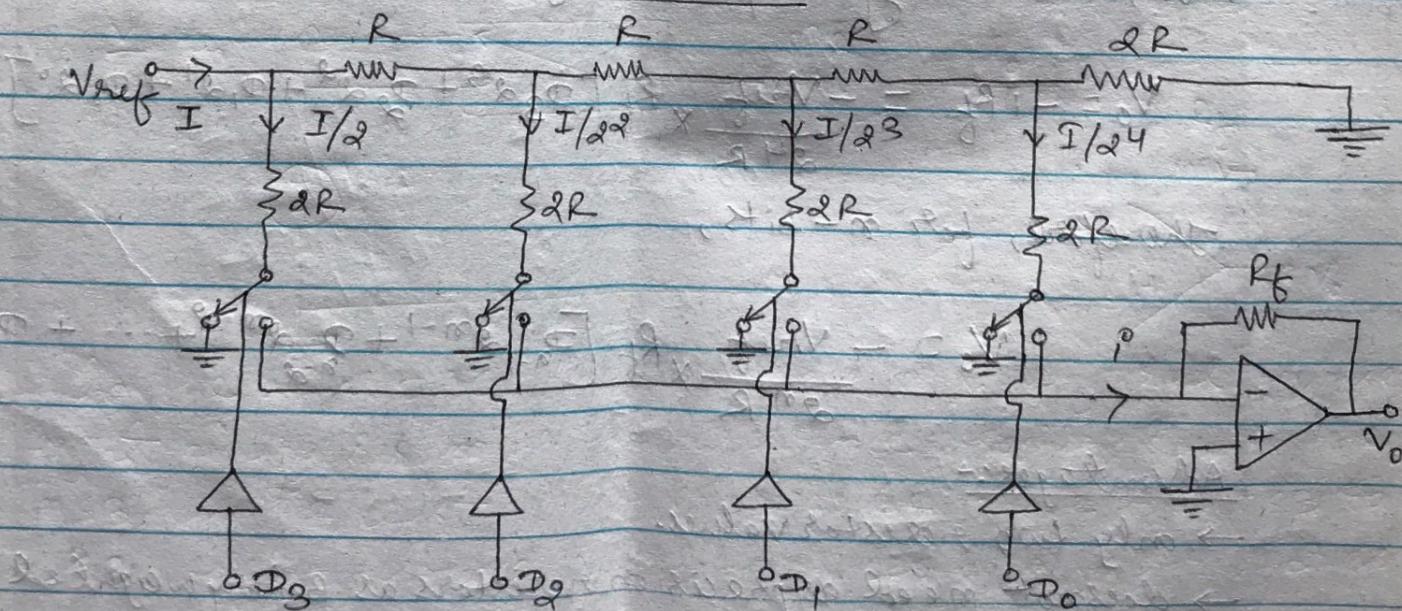
Hence, for n -bits system,

$$V_o = -\frac{V_{ref} \times R_f}{2^{n-1} R} (D_{n-1} 2^{n-1} + \dots + D_0 2^0)$$

Disadvantages:-

- As the number of bit goes on increasing, the resistance values as well as the complexity of the circuit increases. So, cost will be high.
- As the no. of bit increases, the tolerance of the resistance associated with LSB may exceed the value of resistance in MSB.
- As the no. of bit increases, the variation in the value of the resistance will be large and so the power rating. This is not required in the process of IC manufacturing.

(ii) R- ΔR Ladder Network DAC :-



In a ladder n/w right of each node, there are two equal resistors, and each having the value $2R$ and placed across. Hence, the current entering to the node is divided as $I/2^n$ where n is the no. of node starting from MSB to LSB i.e. it generates a current given by $I/2^0, I/2^1, \dots, I/2^n$. So, the ladder network generates a binary sequence of current. If all bits of digital inputs are high i.e. for a 4-bit converter, digital input is 1111, then the total current i is obtained by superposition.

Theorem.

$$\begin{aligned} i &= I/2^0 + I/2^1 + I/2^2 + I/2^3 + I/2^4 \\ &= I(1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4}) \\ &= \frac{V_{ref}}{R} (D_3 2^{-1} + D_2 2^{-2} + D_1 2^{-3} + D_0 2^{-4}) \\ &= \frac{V_{ref}}{2^4 R} (D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0) \end{aligned}$$

Now, the analog output voltage V_o is given by

$$V_o = -i R_f = -\frac{V_{ref}}{2^4 R} \times R_f [D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0]$$

Therefore, for n -bits,

$$V_o = -\frac{V_{ref}}{2^n R} \times R_f [D_{n-1} 2^{n-1} + D_{n-2} 2^{n-2} + \dots + D_0 2^0]$$

Advantages:-

- only two resistor values.
- does not need as precision resistors as Binary Weighted DAC.
- cheap and easy to manufacture.

Disadvantages:-

- slower conversion rate.

Interference Signals and their elimination:-

Interference is contamination by extraneous signals. This may be signals from other transmitters, power cables, machineries, switching circuits, human sources and many more.

Appropriate filtering can remove interference to the extent that the interfering signals occupy different frequency bands than the desired signal.

Interference maybe the coherent signals from other systems (and sometimes the circuit itself) that enters into the desired system.

Interference is external signals in opposition to noise. For this reason, the best way to minimize its effects is to identify the interference paths to our circuits / systems. Its major limitation is in precision measurements and the detectability (resolution).

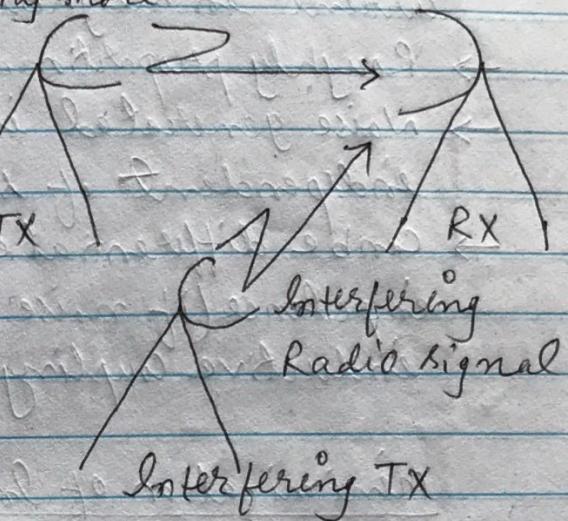
The major paths for interference are:

- ① Signals coupled in inputs and outputs.
- ② Capacitive Coupling
- ③ Inductive Coupling
- ④ Magnetic Coupling
- ⑤ RF Coupling.

Capacitive coupling :-

conductors in the close proximity interfere with each other.

- Implements highpass RC filter across the noise source and the signal.
- Noise appearing on the signal is proportional to the noise source level.



→ Problem with high frequency and high impedance signals.

Inductive Coupling :-

magnetic flux generated due to noise circuit will induce current in neighboring circuits.

→ Roughly proportional to the areas of the two circuits.

→ Noise generated is an added voltage in parallel, therefore, independent of signal level.

→ Can't be differentiated from capacitance by changing the load impedance (if noise level stays the same, then we have inductive coupling).

Minimization of Interference Effects :-

→ Avoid direct capacitive coupling between signals tracks using ground planes and guard rings.

→ Avoid magnetic coupling avoiding loops (use of twisted pair).

→ Protecting power supply inputs with feedthroughs to avoid interference signal paths through supply voltages.

→ use shielding to avoid RF coupling when necessary.

→ use separate grounds for digital / analog signals.

→ use only one point to 'ground' the circuit.

→ use separate power supply when possible.