

## Unit 1 Introduction of microprocessor

### 1.1 Evolution of microprocessor

Basic Components	4-Bit microprocessor	8-Bit	16-bit	32 bit	C4 bit
Date:	1971	(1972 - 1976)	1976	(1985 - 1995)	(1997 - 2000)
No. of data lines	4-bit	8-bit	16-bit	32 bit	64-bit
Name of CPU	Intel 4004	(i) 8008 (1972) (ii) 8080 (1974) (iii) 8085 (1978)	Intel 8086	80386 80486 Pentium Pentium Pro	Pentium-II Pentium-III Pentium-IV
Technology used	p-MOS	p-MOS			
Access memory provide	640 Bytes	8 KB 64 KB	1 MB	4 GB 4 GB 4 GB 64 GB	640 GB
Speed	6000 operation/sec				
No. of transistors	2300	6500	24000	> 1 million	4.5 million
Clock freq.	750 KHz	5 MHz	5 MHz	2 GHz (16 - 150) MHz	6 GHz > 200 MHz
Advance Version	4004				
Other Companies	PPS-4, T 3438	MC6800, Zilog, Z80 8 Z800			

Note: 2005 → ~~i3~~ Pentium D after this i3, i5  
 To i7 → 2008  
 i9 → in 2017 → 64 bit processor

### 1.2) Von Neumann

- (i) C4 bus microprocessor (1997 - 2000)
- (ii) Data & Code lie in same memory block
- (iii) 232 data bus used for instruction and data
- (iv) CPU perform only one operation at time

### Harvard architecture

- (i) 64 data & code lie in different memory block
- (ii) 2 separate buses used for instruction and data
- (iii) CPU perform many operations at time.

Pentium-II  
Pentium-III  
Pentium-IV

C407B

### 1.3 Microprocessor

- (i) 8 bit, 16 bit, 32 bit Video, Audio and image processing
- (ii) microprocessor use general purpose
- (iii) Eg: TV, mobile, laptop, Camera, etc

### MicroController

- (i) 8 bit, 16 bit, 32 bit Audio, Video processing
- (ii) Pre programmed
- (iii) Eg: washing machine, traffic light, timer, car microdrive.

- (i) Large Heavy size use
- (ii) Size Heavy use

- (i) Small size low cost

## (1.4) Internal architecture of 8085 CPU

## ① Registers

Special purpose register  
(B, C, D, F, H, L, A)General purpose register  
(PC, SC, SP, BP)

(ii) Instruction register (Instruction store)

(iii) Instruction Decoder (Decode instruction)

(iv) Timing Diagrams & Circuit (It realizes Control signals)  
जिन डायग्राम के द्वारा हमने बताते हैं)  $\Rightarrow$  human brain

(v) Arithmetic &amp; logic unit

(vi) Temporary register

(vii) Flags.

1.5

Concept of fetch

Fetch: CPU को Instruction / data देखते from memory.

Decode: CPU को ~~सही~~ सही Instruction को pattern करता है और मानते

Execute: program execute हो।

## (Unit II) Assembly language programming

Page 110

Date: \_\_\_\_\_

it II). Assembly language program. opcodes. It is indicate the type of operation. A lso performed on the given data.

$\Rightarrow$  opCode at given data ~~of~~ for type operation performed on reg C21 AT&T 36,  
eg ~~+ - \* /~~ Add, Sub:

Operand  $\rightarrow$  କୁଣିତ କାର୍ଡ ମେହିନେ ପାଇଁ କୁଣିତ

The diagram illustrates the MOV instruction with the following components:

- OpCode:** The label for the first part of the instruction.
- Operands:** The label for the second part of the instruction.
- Source:** The variable A is shown as the source operand.
- Destination:** The variable B is shown as the destination operand.

Arrows indicate the flow of data: one arrow points from the Source (A) to the Destination (B), and another arrow points from the Destination (B) back to the Source (A). The word "OpCode" is positioned below the first arrow, and "Operands" is positioned below the second arrow.

May A, B

## Opcode

Mnemonics :- ~~g~~ <sup>21st</sup> <sup>Q</sup> Symbol Suitable Symbols  
Page 1

Eg: R used for Register, A used for Accumulator.

2.2.

## 8085 Instruction Set

- (i) Data transfer instruction (MOV A, B, P/M A, 4FH)
  - (ii) Arithmetic " (Sub B, Add B)
  - (iii) Logic and Bit manipulation (AND B, ANI 02)
  - (iv) Branch instruction (JNZ, Jmp)
  - (v) Machine Control instruction (HLT, NOP)

## (2.4) Addressing modes of 8085

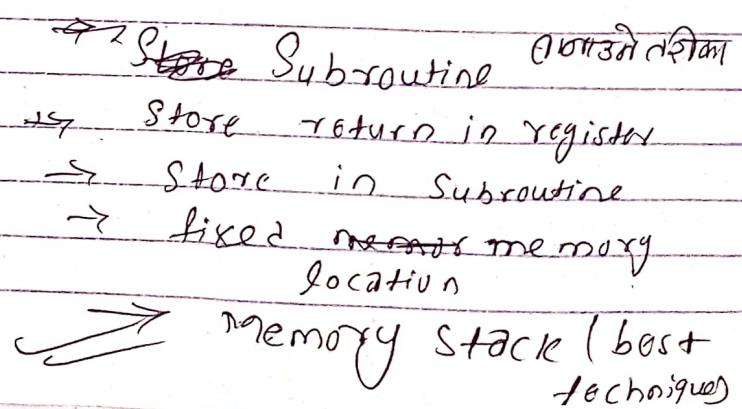
- (i) Immediate Addressing mode: Eg: MVI A, 33H  
LYI B, 2050H
- (ii) Direct Addressing mode: LDA 2050H, STA 2070H and  
IN 20H, OUT 30H
- (iii) Register Addressing mode: MOV A, B, ADD D
- (iv) Register Indirect addressing mode: LDAX B, STAX D
- (v) Implied Addressing mode: CMA, RRC, RLC

program Control: ~~MP~~ <sup>MP</sup> ~~Sequence~~ <sup>Sequence</sup> Sequence  
 program execute ~~seq~~ but program control  
 is used for randomly execute the  
 program.

## Jump Instruction

- (i) Unconditional Eg JMP 16 bit address
- (ii) Conditional : Eg JZ 16 bit address

Subroutine call ~~return~~ Just like function.



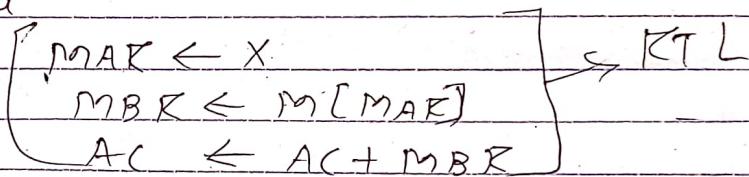
### Timing Diagram (Involved terms)

- Higher order Address ( $A_8 - A_{15}$ )
- Lower order .. ( $A_{D0} - A_{D7}$ )  $\Rightarrow$  (Address + Data)
- Address latch Enable (ALE)
- RD, WR, IO/M, SO, S1.

### 2.7 RTL Instruction descriptions

प्रति microoperation performed by symbolic  
उपर्युक्त.

Eg. ADDX



### (2.8) Assembly language program,

जो low-level programming language है  
 जो आप hardware को direct communicate  
नहीं।

ADD B.  
MOV B.

## Unit 3

(3.1) Bus Structure H1 प्र० ०८८१ Part ३६४

(i) Address bus :- यह पास Unidirectional है।  
 अन्तरा  $2^{16} = 64\text{ KB}$  Capacity है।  
 यह bus पर IP को memory में  
 पहुंचने की data fetch होती है ताकि यह प्राप्त कर सके।

(ii) Data bus :- यह पास bidirectional है।  
 अन्तरा 28 - 256 instruction होती है।  
 यह bus पर CPU को data exchange करती है।  
 data memory से प्राप्ति की जाती है। Read & Write  
 प्रक्रिया का समान रूप से data bus पर होती है।

(iii) Control bus :- यहले सबसे Signal है।  
 It controls the flow rate of peripheral device buses जैसे  
 Hard disk, etc.

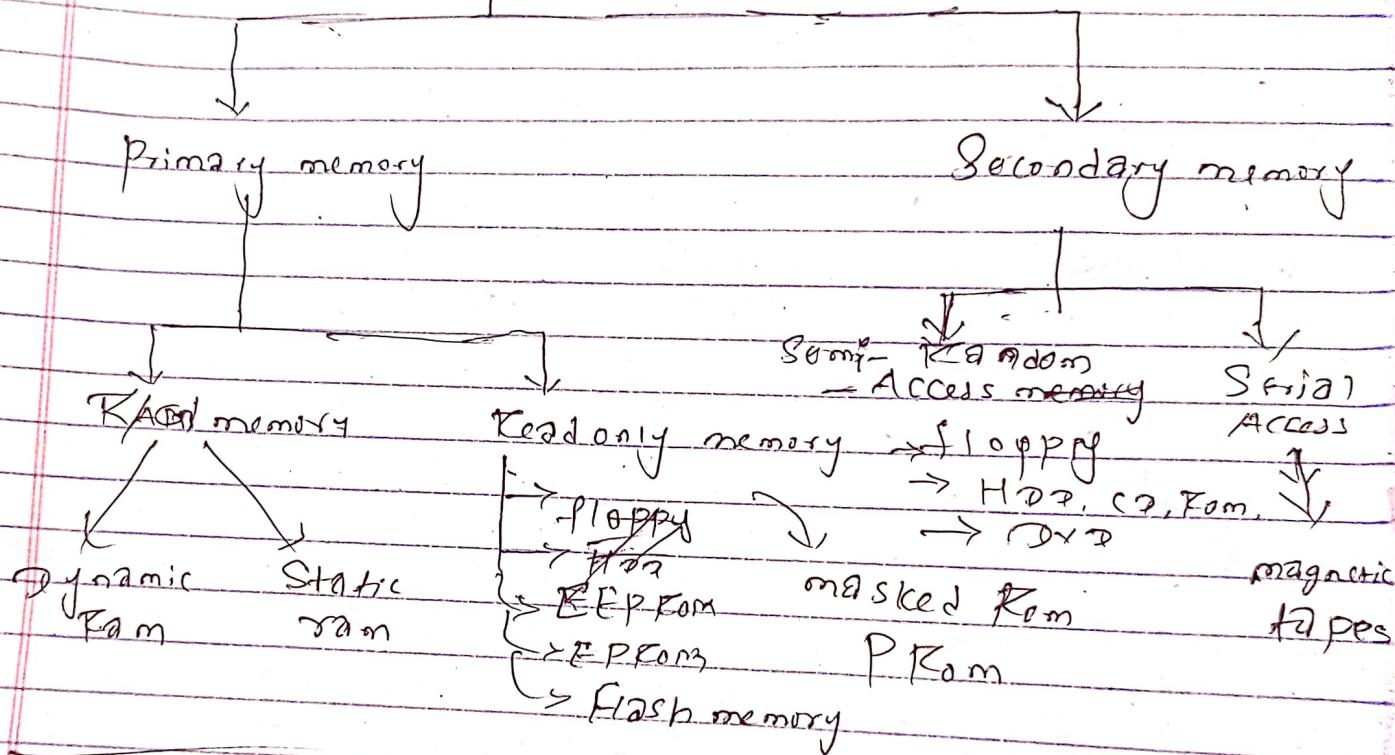
### \* Classified data bus

(i) Synchronous data bus :- यहले फॉर्म  
 Data ताकि वह दोहरी clock लियो।

(ii) Asynchronous data bus :- यहले फॉर्म  
 इकली दोहरी clock लिये जाते हैं जो previous  
 data की तरफ आते हैं।

(3.2) Memory interfacing :- डिजिटली memory  
 AP II समीक्षा र मिशन interrupt  
 (24/3/201)

### Types of memory



#### Static Ram

- 2141H Six OR 12 Transistor
- 1 bit Store OR 1

- 2141H 2<sup>32</sup> Capacitor

- कोई अवधि नहीं flip flop

- Eg: Cache memory, SDRAM

#### Dynamic Ram

- 2121H 1 Transistor

- 1 bit Store OR 1

- 2121H 2<sup>32</sup> Capacitor

- Eg: Hard disk, magnetic tape,

- 2121H Cost ~~ann~~ ₹ 564

I/O mapped

→ 21 पाले I/O device + 0  
Accumulator विषयी data  
transfer से ।

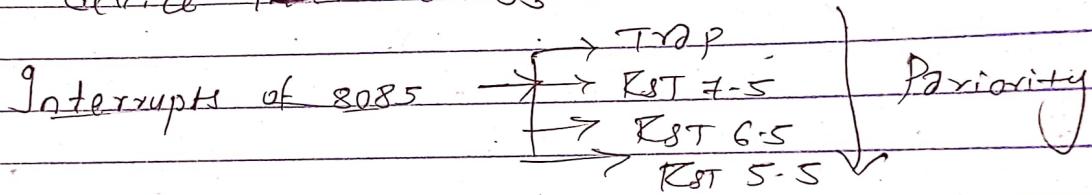
→ 21 पाले I/O device + 0  
I/O R operation  
S64

memory mapped I/O

21 पाले memory, Register  
to Accumulator परिवहन data  
transfer S64, ।

21 पाले MFMDR & MERO  
Operation की ।

(3.3) I/O interfacing :- 21 पाले up H1 peripheral  
device interface की है ।



(i) DMA Controller (8237) (Direct memory Access) 21 पाले  
memory & I/O device की direct access की  
होती है । 21 पाले क्रूप्ति mode S64, ।

(i) master mode: 21 पाले की busy S64, वे  
DMA की hold परिवहन करते हुए H1 DA  
Signal up की release करते हुए ।

(ii) slave mode: 21 पाले DMA की काम सके थे  
21 पाले buses का प्रियंका S64, वे आप द्वारा  
as peripheral devices की 21 पाले की S64, ।

(ii) PIC (Programmable Interrupt Controller) (8259):-

यह एक प्रोग्रामेबल इन्टरफ़ेस है जो इन्टरफ़ेस के लिए  
प्रोग्रामिंग करता है। यह 16 बिट इन्टरफ़ेस है और 64 पिन  
में से 8 पिन SPI के रूप में उपलब्ध हैं।

(iii) USART (8251) (Universal Synchronous Asynchronous  
Receiver And Transmitter):-

यह एक परिपर्वक डिवाइस है जो कम्युनिकेशन के लिए  
उपलब्ध है।

Transmitter के पारलल ऑट्सी लोजिक कोडर के लिए  
& receiver के लोजिक कोडर के पारलल लोजिक के लिए

(iv) PPI (8255) (Programmable Peripheral Interface):-

(v) PPI (8255A) (Programmable Peripheral Interface)

यह एक परिपर्वक डिवाइस है।

यह CPU के इन्टरफ़ेस के लिए उपलब्ध है जैसे कि ADC, DAC, I/O

Unit: 04

(4.1) 8086

→ 21st H1

Segmentation &amp; Pipeline 8

→ 21st H1 Six 021 instruction

Fetch

866

8085

21st H1

Pipeline &amp; Segmentation

Fetch 866

→ 21st H1 Six 021 instruction

Fetch

866

→ 21st H1 data bus - 16 bit

Address bus - 20 bit

Capacity  $2^{20} = 1\text{MB}$ 

21st H1 data bus - 8 bit

Address bus - 16 bit

Capacity  $= 2^{16} = 64\text{KB}$ 

4.2 Bus interface unit :- 21st H1 Instruction queues,

:- 1 pointer register IP, And Segmentation (CS, SS, DS, ES, BP)  
Contain stackExecution unit :- 21st H1 4P 866 instruction 015  
fetch 866 decode 866 execute 866 control 866

4.3 Pin-diagram :- 21st H1 40 pins 866 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 30 40

21st H1 Address bus, 16 021 data bus, 1 supply  
1 reset, 2 Ground pins 866