Presentación trabajo final
circuitos lógicos programables

Controlador VGA

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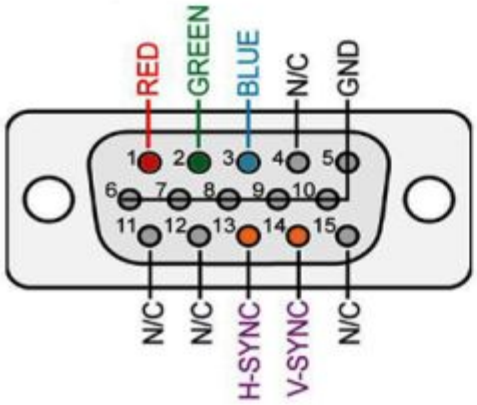
Características

Video Graphics Array (**VGA**) o **Matriz de gráficos de vídeo** se utiliza para denominar a:

- Una pantalla estándar analógica de computadora.
- La resolución 640 × 480 píxeles.
- El conector de 15 contactos D subminiatura.
- La tarjeta gráfica que comercializó IBM por primera vez en 1988.
- La señal que se emite a través de estos cables es analógica, por lo que tiene ciertos inconvenientes frente a las señales digitales.

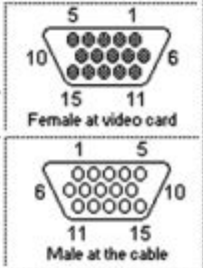


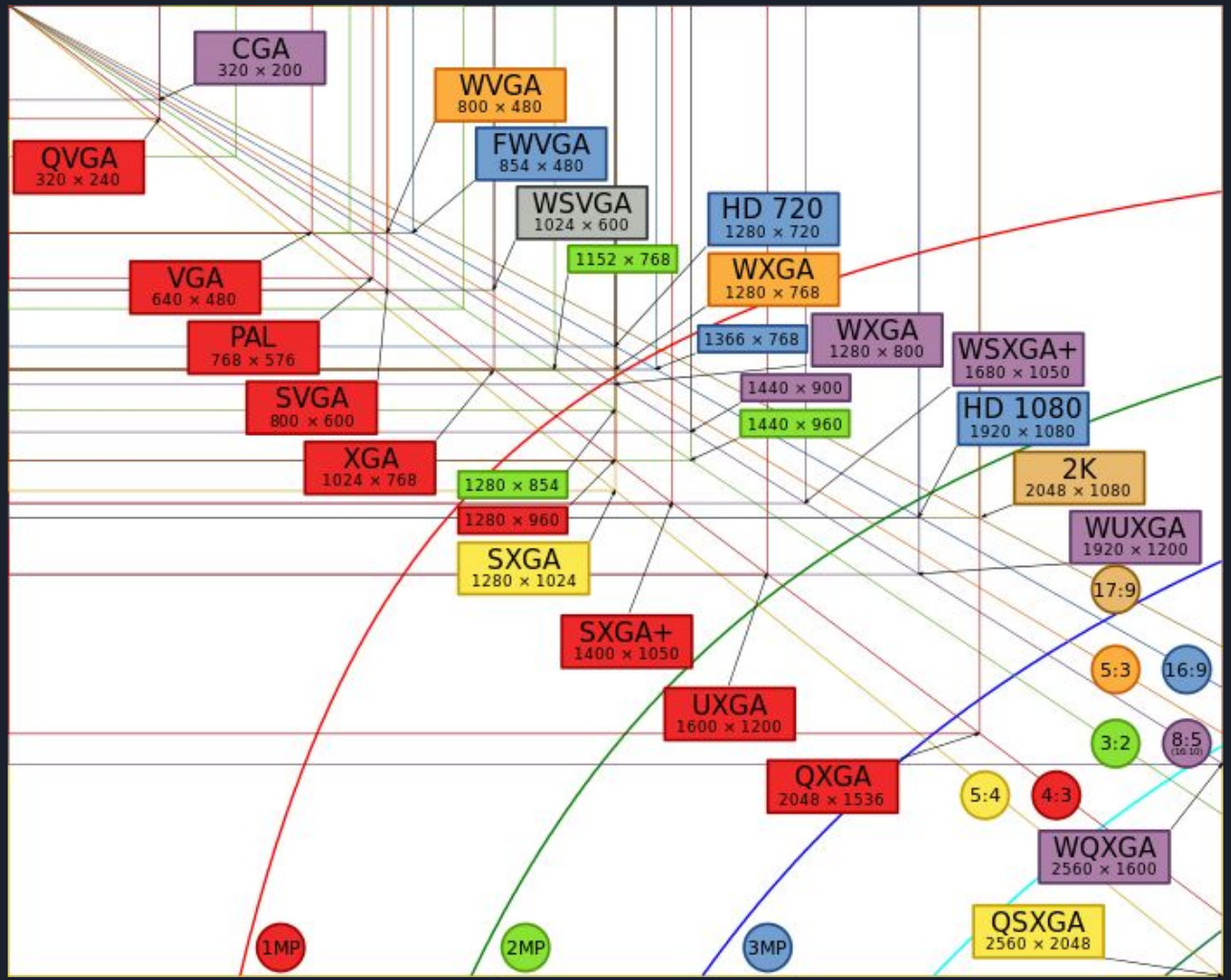
DETAIL FUNGSI DARI MASING-MASING PIN

1 - Red Video	6 - Red GND	11 - Monitor ID
2 - Green Video	7 - Green GND	12 - DDC SDA
3 - Blue Video	8 - Blue GND	13 - H_{sync}
4 - Reserved	9 - +5 V DC	14 - V_{sync}
5 - GND	10 - Sync GND	15 - DDC SCL

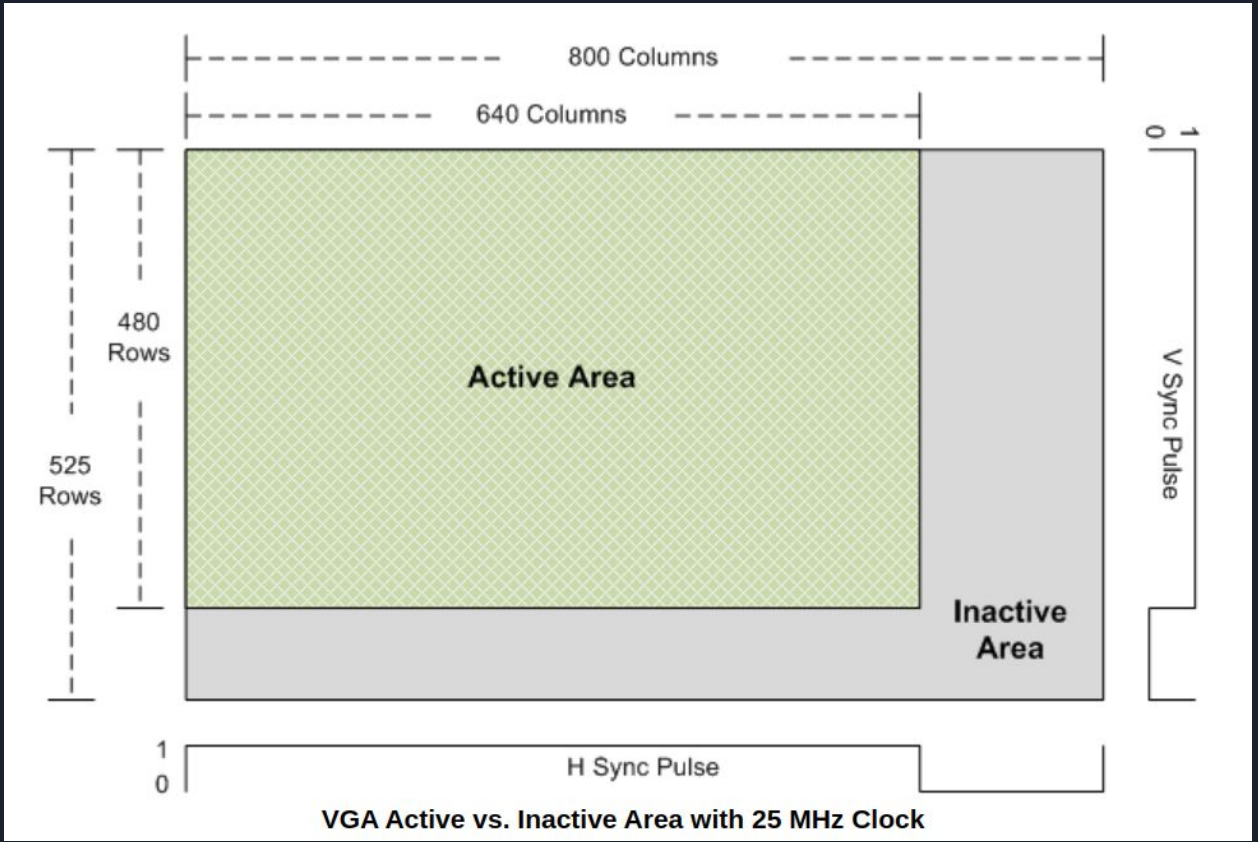
VGA PINOUT

Pin	Name	Dir	Description
1	RED	OUT	Red Video (75 ohm, 0.7 V p-p)
2	GREEN	OUT	Green Video (75 ohm, 0.7 V p-p)
3	BLUE	OUT	Blue Video (75 ohm, 0.7 V p-p)
4	ID2	IN	Monitor ID Bit 2
5	GND	------	Ground
6	RGND	------	Red Ground
7	GGND	------	Green Ground
8	BGND	------	Blue Ground
9	KEY	-	Key (No pin)
10	SGND	------	Sync Ground
11	ID0	IN	Monitor ID Bit 0 GND=Color; NC=Mono
12	ID1 or SDA	IN	Monitor ID Bit 1 NC=Color; GND=Mono Some systems only uses ID0 for monitor ID
13	HSYNC or CSYNC	OUT	Horizontal Sync (or Composite Sync)
14	VSYNC	OUT	Vertical Sync
15	ID3 or SCL	IN	Monitor ID Bit 3




CGA
320 × 200
QVGA
320 × 240
WVGA
800 × 480
FWVGA
854 × 480
WSVGA
1024 × 600
1152 × 768
HD 720
1280 × 720
WXGA
1280 × 768
VGA
640 × 480
PAL
768 × 576
1366 × 768
WXGA
1280 × 800
WSXGA+
1680 × 1050
1440 × 900
HD 1080
1920 × 1080
1440 × 960
SVGA
800 × 600
XGA
1024 × 768
1280 × 854
2K
2048 × 1080
1280 × 960
WUXGA
1920 × 1200
SXGA
1280 × 1024
17:9
SXGA+
1400 × 1050
5:3
16:9
UXGA
1600 × 1200
3:2
8:5
QXGA
2048 × 1536
5:4
4:3
WQXGA
2560 × 1600
QSXGA
2560 × 2048
1MP
2MP
3MP

Información que se visualiza en pantalla



VGA Active vs. Inactive Area with 25 MHz Clock

https://www.nandland.com/goboard/vga-introduction-test-patterns.html

Sincronismo vertical y horizontal

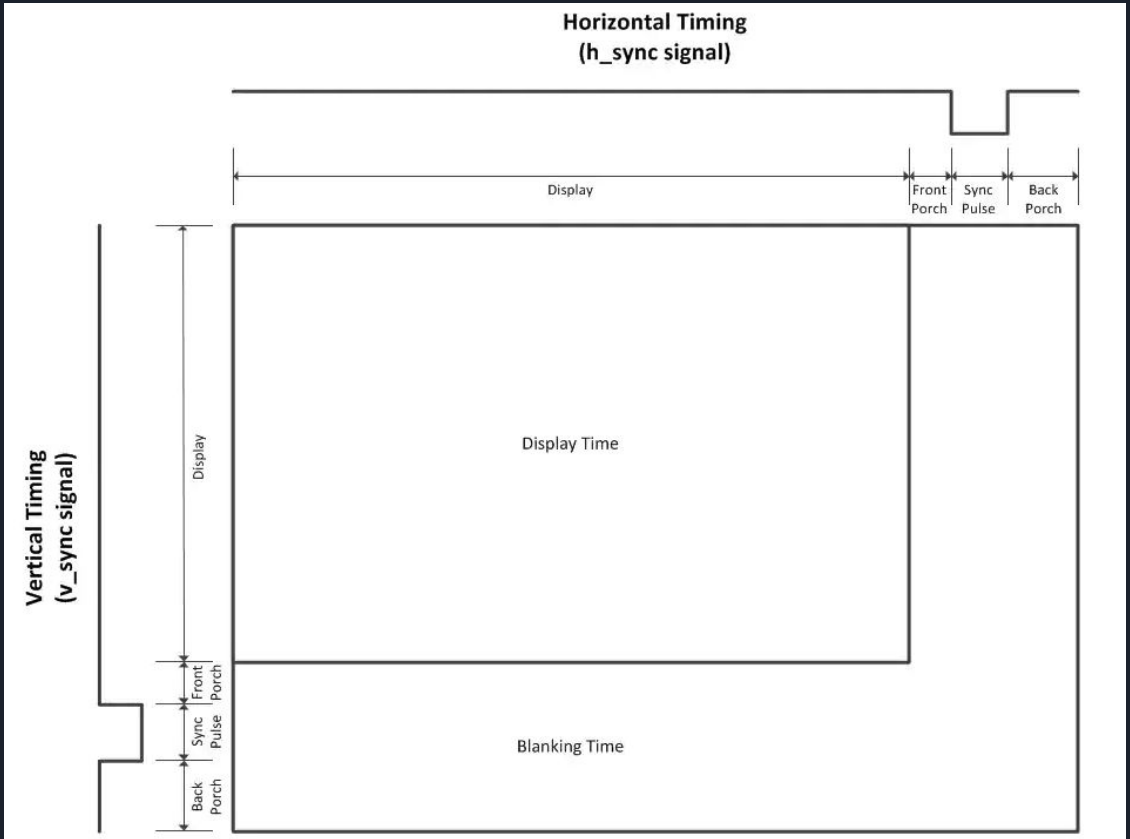


Figure 3. Signal Timing Diagram

https://www.digikey.com/eewiki/pages/viewpage.action?pageId=15925278

VGA Signal 640 x 480 @ 60 Hz Industry standard timing

General timing

Screen refresh rate	60 Hz
Vertical refresh	31.46875 kHz
Pixel freq.	25.175 MHz

Horizontal timing (line)

Polarity of horizontal sync pulse is negative.

Scanline part	Pixels	Time [µs]
Visible area	640	25.422045680238
Front porch	16	0.63555114200596
Sync pulse	96	3.8133068520357
Back porch	48	1.9066534260179
Whole line	800	31.777557100298

Vertical timing (frame)

Polarity of vertical sync pulse is negative.

Frame part	Lines	Time [ms]
Visible area	480	15.253227408143
Front porch	10	0.31777557100298
Sync pulse	2	0.063555114200596
Back porch	33	1.0486593843098
Whole frame	525	16.683217477656

http://tinyvga.com/vga-timing

Modos VGA - Ejemplos

Pixel Clock (MHz)	Horizontal (pixel clocks)				Vertical (rows)				Polarity	
	Display	Front Porch	Sync Pulse	Back Porch	Display	Front Porch	Sync Pulse	Back Porch	h_sync	v_sync
25.175	640	16	96	48	480	10	2	33	n	n
44.9	1024	8	176	56	768	0	8	41	p	p
65	1024	24	136	160	768	3	6	29	n	n
234	1920	128	208	344	1440	1	3	56	n	p
297	1920	144	224	352	1440	1	3	56	n	p

https://www.digikey.com/eewiki/pages/viewpage.action?pageId=15925278

Entidades: VGA_Sync

```
entity VGA_Sync is
    generic(
        COLUMNS         : natural := 800;
        ROWS            : natural := 525;
        H_display       : natural := 640;    -- pixels
        H_font_porch    : natural := 16;     -- pixels
        H_sync_pulse    : natural := 96;     -- pixels
        H_back_porch    : natural := 48;     -- pixels
        V_display       : natural := 480;    -- lines
        V_font_porch    : natural := 10;     -- lines
        V_sync_pulse    : natural := 2;      -- lines
        V_back_porch    : natural := 33      -- lines
    );
    port(
        clk_i           : in    std_logic;
        rst_i           : in    std_logic;
        H_sync          : out   std_logic;
        V_sync          : out   std_logic;
        display_enable  : out   std_logic;
        column          : out   natural range 0 to COLUMNS;
        row             : out   natural range 0 to ROWS
    );
end VGA_Sync;
```

Entidades: VGA_Sync_MMCM

```
entity VGA_Sync_MMCM is
    generic(
        COLUMNS         : natural := 800;
        ROWS            : natural := 525;
        H_display       : natural := 640;   -- pixels
        H_font_porch    : natural := 16;    -- pixels
        H_sync_pulse    : natural := 96;    -- pixels
        H_back_porch    : natural := 48;    -- pixels
        V_display       : natural := 480;   -- lines
        V_font_porch    : natural := 10;    -- lines
        V_sync_pulse    : natural := 2;     -- lines
        V_back_porch    : natural := 33     -- lines
    );
    port(
        clk_i           : in    std_logic;
        rst_i           : in    std_logic;
        H_sync          : out   std_logic;
        V_sync          : out   std_logic;
        display_enable  : out   std_logic;
        column          : out   natural range 0 to COLUMNS;
        row             : out   natural range 0 to ROWS
    );
end VGA_Sync_MMCM;
```

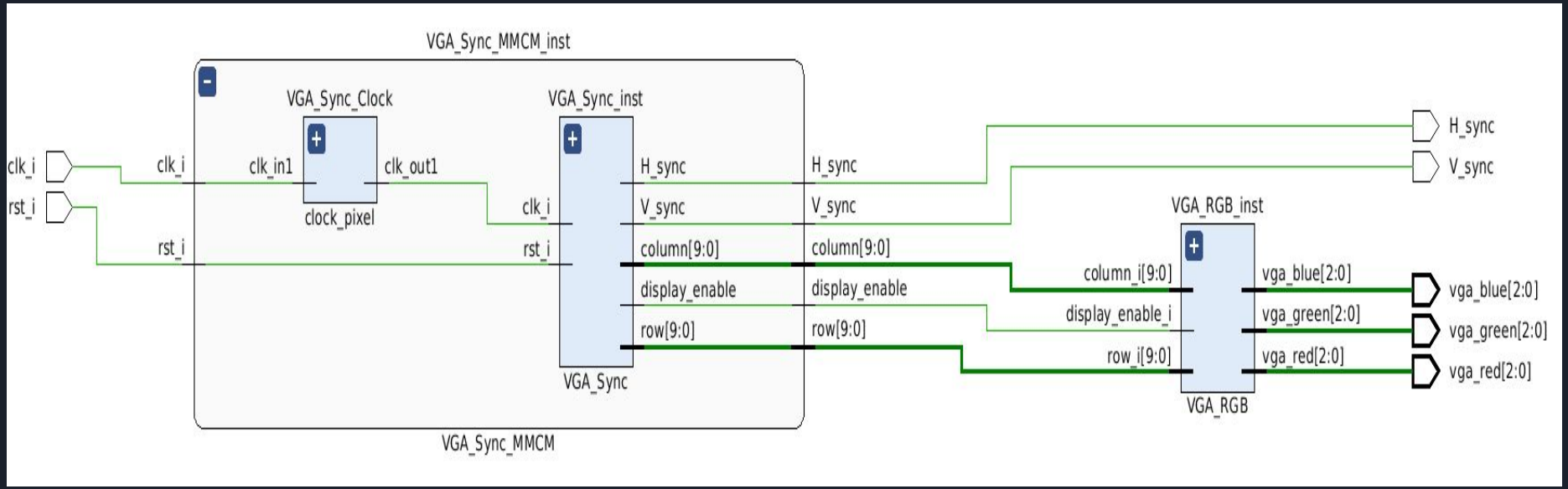
Entidades: VGA_RGB

```
entity VGA_RGB is
    generic(
        COLOR_BITS      : natural := 3;
        COLUMNS         : natural := 800;
        ROWS            : natural := 525;
        H_display       : natural := 640;    -- pixels
        V_display       : natural := 480     -- lines
    );
    port(
        column_i            : in    natural range 0 to COLUMNS;
        row_i               : in    natural range 0 to ROWS;
        display_enable_i    : in    std_logic;
        vga_red             : out   std_logic_vector(COLOR_BITS-1 downto 0) := (others => '0');
        vga_green           : out   std_logic_vector(COLOR_BITS-1 downto 0) := (others => '0');
        vga_blue            : out   std_logic_vector(COLOR_BITS-1 downto 0) := (others => '0')
    );
end VGA_RGB;
```

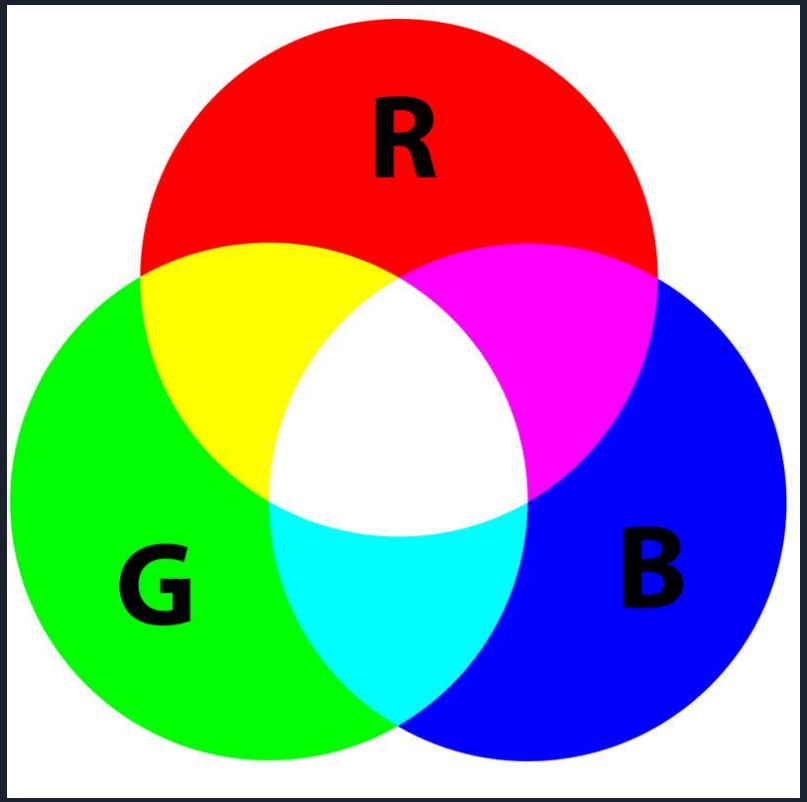
Entidades: VGA_background

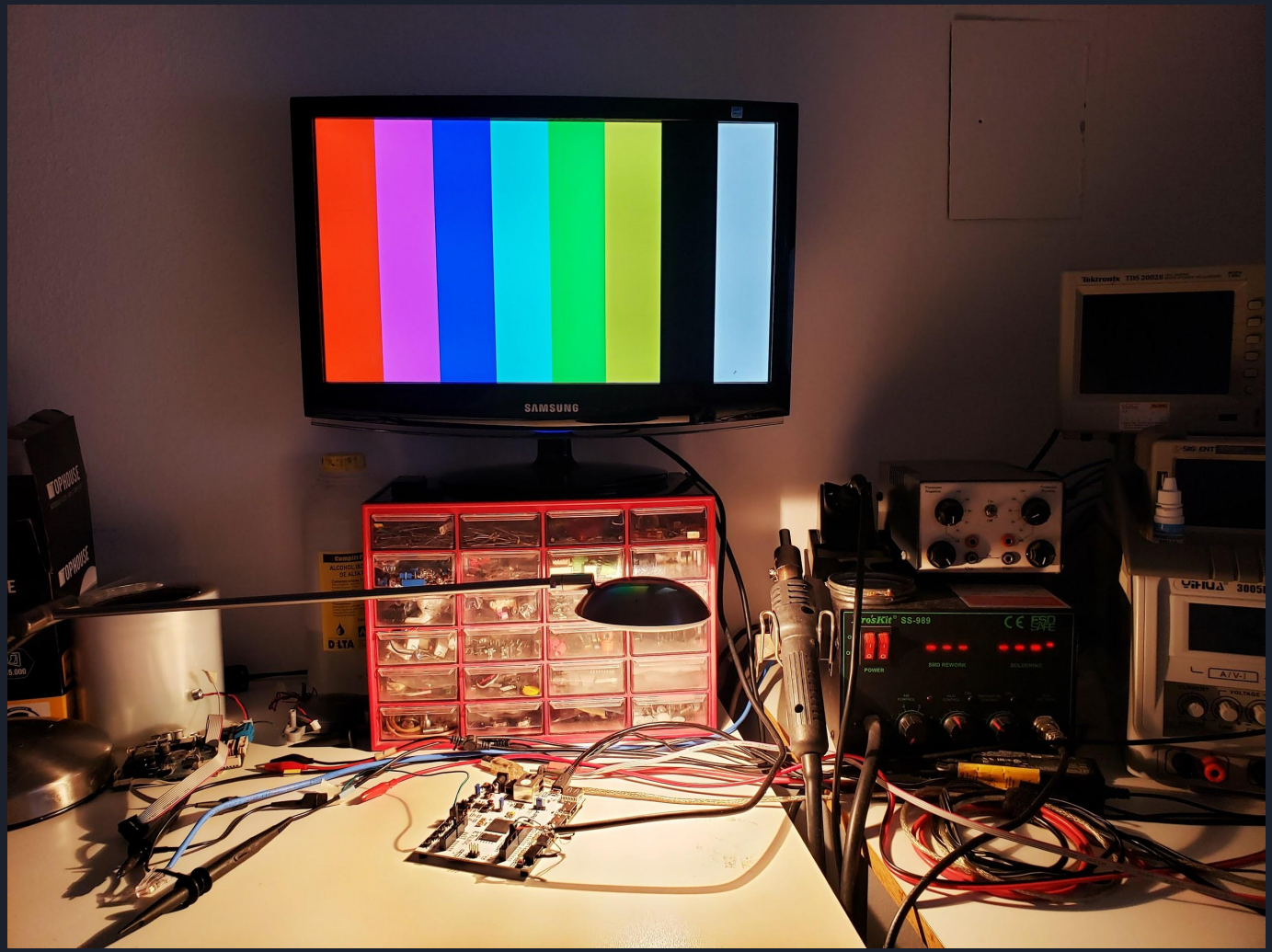
```
entity VGA_background is
    generic(
        COLOR_BITS      : natural := 3;
        COLUMNS         : natural := 800;
        ROWS            : natural := 525;
        H_display       : natural := 640;   -- pixels
        H_font_porch    : natural := 16;    -- pixels
        H_sync_pulse    : natural := 96;    -- pixels
        H_back_porch    : natural := 48;    -- pixels
        V_display       : natural := 480;   -- lines
        V_font_porch    : natural := 10;    -- lines
        V_sync_pulse    : natural := 2;     -- lines
        V_back_porch    : natural := 33     -- lines
    );
    port(
        clk_i           : in    std_logic;
        rst_i           : in    std_logic;
        H_sync          : out   std_logic;
        V_sync          : out   std_logic;
        vga_red         : out   std_logic_vector(COLOR_BITS-1 downto 0) := (others => '0');
        vga_green       : out   std_logic_vector(COLOR_BITS-1 downto 0) := (others => '0');
        vga_blue        : out   std_logic_vector(COLOR_BITS-1 downto 0) := (others => '0')
    );
end VGA_background;
```

Esquemático realizado en FPGA



Colores que podemos formar con 1 bit en RGB

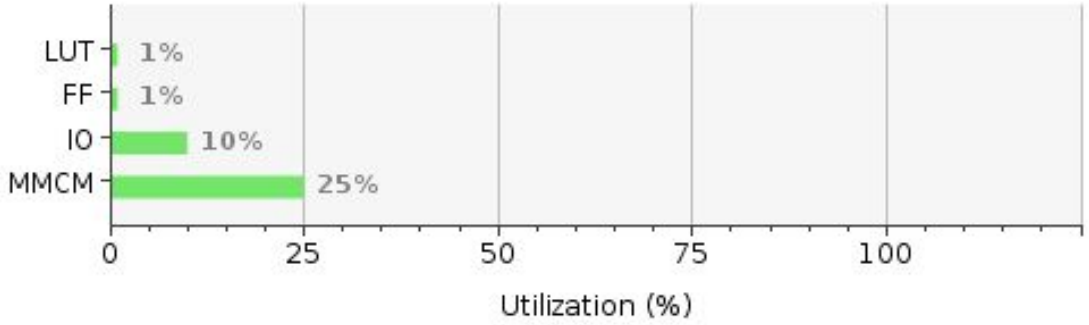



SAMSUNG
Tektronix TDS 2002B
SS-989
POWER
SMD REWORK
SOLDERING

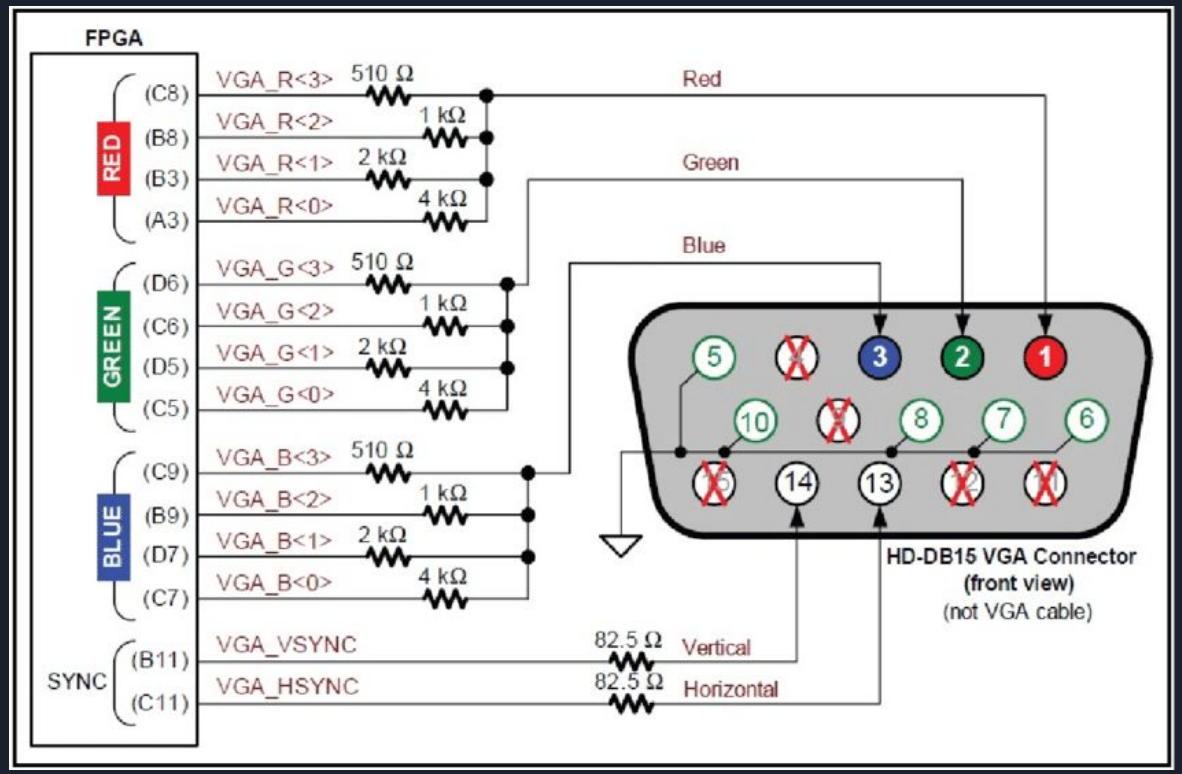
Reporte de utilización herramienta Vivado

Summary

Resource	Utilization	Available	Utilization %
LUT	49	53200	0.09
FF	37	106400	0.03
IO	13	125	10.40
MMCM	1	4	25.00



Opciones para utilizar varios bits de video



https://www.researchgate.net/publication/312984160_FPGA_Based_Real_Time_Iris_Recognition_Signature

Opciones para utilizar varios bits de video

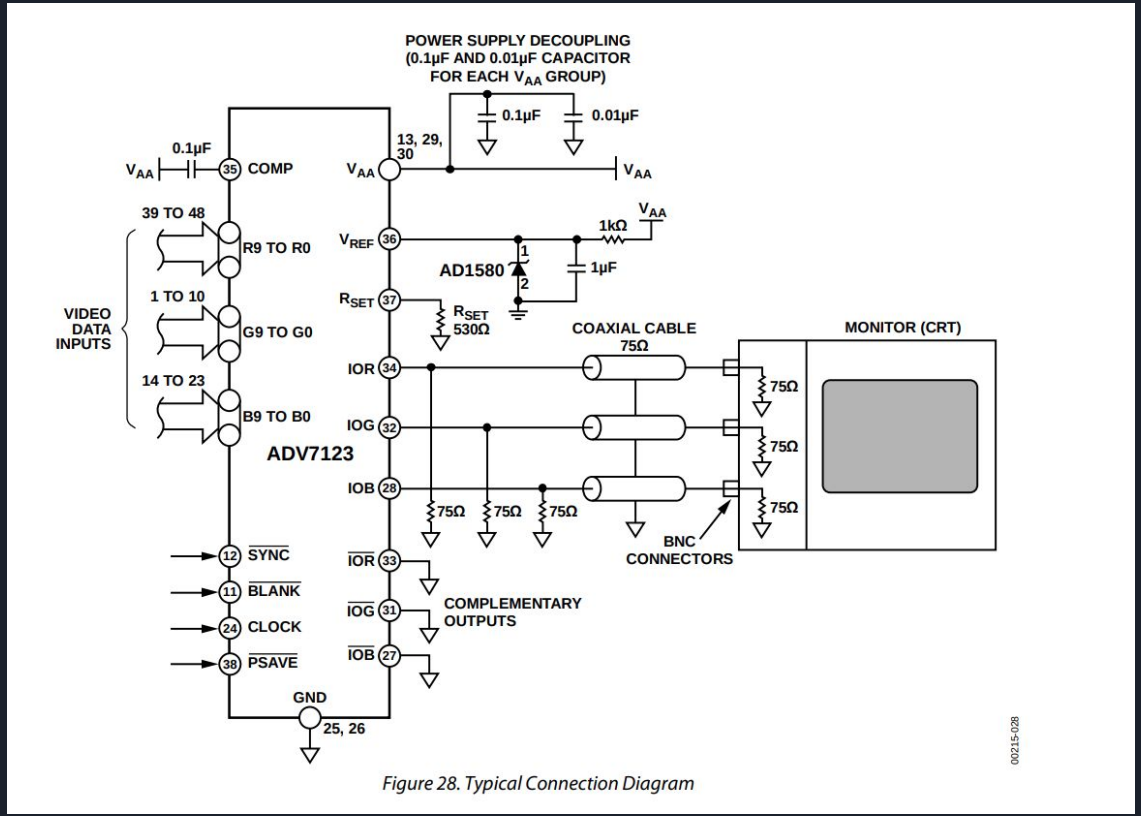


Figure 28. Typical Connection Diagram

https://www.analog.com/media/en/technical-documentation/data-sheets/ADV7123.pdf

Muchas gracias.

Ing. Luciano Francisco Vittori