Marshall T. Versteeg

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EDUCATION

University of Michigan - Ann Arbor, MI **GPA: 3.79/4.00**

- M.S.E. Electrical Engineering — April 2017
- B.S.E. Electrical Engineering — April 2016
- Relevant Courses: Computer Architecture, Digital Logic Design, Embedded Systems, Data Structures & Algorithms

EXPERIENCE

Computer Architecture Graduate Student Instructor, *U of M* — Aug 2016 – Present

- Hold weekly lab section for students designing out-of-order, superscalar processor
- Assist students with questions about Verilog, EDA tools, and lecture material

FPGA Engineer Intern, *Harris Corporation* — Summer 2016

- Designed and implemented synthesizable test platform on Zynq FPGA which will allow researchers to easily run tests for DDR3 memory
- Implemented and tested SelectMap Interface between two FPGAs utilizing standard debug cores

Instructional Aide, *College of Engineering* — Jan 2015 – Dec 2015

- Taught first-year engineering students about wireless technology and photovoltaic cells
- Created new laboratory project to give students hands-on experience using microcontrollers and power electronic systems

Undergraduate Researcher, *U of M Energy Institute* — May 2015 – Aug 2015

- Researched new method of doping silicon carbide to reduce processing costs
- Fabricated and tested samples in cleanroom of Lurie Nanofabrication Facility

Research Assistant, *U of M Electronics Shop* — May 2014 – Dec 2014

- Added debug capability to large Verilog design by implementing Gigabit transciever, ILA, and VIO cores
- Gained experience using Xilinx Vivado tool and common lab equipment including oscilloscope, function generator, and soldering tools

PROJECTS

RISC Processor Design, Senior Design Project — Jan 2016 – Apr 2016

- Designed a fully synthesizable superscalar out-of-order execution processor as part of a five person team
- Individually designed and tested early branch resolution feature which improved performance by an estimated 9%
- Created visual debugger, automatic testing script, and automatic performance result script using SystemVerilog and Bash to greatly reduce time spent debugging and analyzing

SKILLS

Programming Languages: (System)Verilog, VHDL, C++, C
Scripting Languages: Bash, Python, Tcl
Software/Tools: Xilinx Vivado IDE, Cadence IES, Synopsys VCS, Matlab

ACTIVITIES

Eta Kappa Nu (HKN), *EECS Honor Society* — Jan 2014 – Present

- Activities Officer — Aug 2014 – Dec 2014