Shenzhen Hansheng Industrial Co., Ltd.

SHENZHEN HANSHENG INDUSTRAIL CO.LTD.,

HS12864TG10B

Specifications

DA TASHEET

Han Sheng **HS**	Production	Audit	approve

Version:VER 1.0	
Version:VER 1.1	Cable29mm,Change the serial number of port silk screen 1~12

Shenzhen Hansheng Industrial Co., Ltd.

Address: Niucheng Road, Xili Town, Nanshan District, Shenzhen208Yilion Industrial Building5Floor Phone:0755-86114312/86114313/86114313 business: 13662619413technology:13418624768 fax:0755-86114314

Website:www.hslcm.com

one,LCDBasic parameters

1.Product Introduction:

The HS12864TG10B LCD module produced by our company is small and light, easy to use and has clear display, so it is widely used in various human-computer communication panels. This model can display 128 columns * 64 rows

Dot matrix monochrome pictures, or display 8/row*4 rows 16*16 dot matrix Chinese characters, or display 16/row*8 rows 8*8 dot matrix English, numbers, symbols. Strong input command, can be combined into various input, display, displacement methods to meet different requirements

It can be widely used in various instruments, PM2.5 detectors, POS card machines, attendance systems, access control systems, etc.

2.Features of the module:

2.1. The product is thin, light, solid in structure, and has FPC and plug-in technology.

2.2. COG process, IC adopts ST7567, which has powerful functions and good stability.

2.3. Display content:

● 128*64 dot matrix monochrome picture;

● You can choose to use 16*16 dot matrix or other dot matrix pictures to edit Chinese characters. According to the calculation of 16*16 dot matrix Chinese characters, 8 characters/line*4 lines can be displayed.

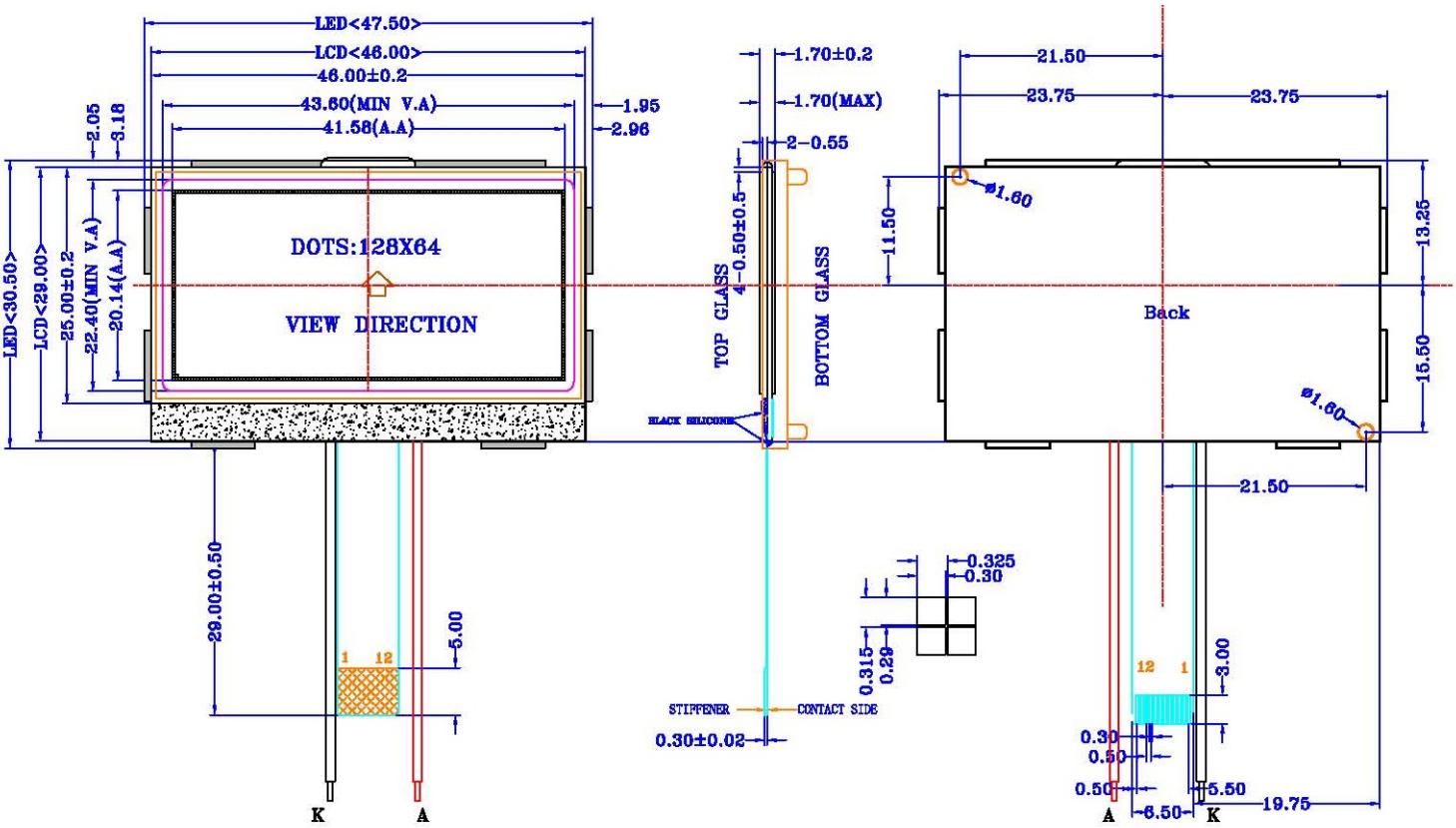
2.4. Strong command function: can be combined into various input, display and shift modes to meet different requirements;

2.5. Simple and convenient interface: serial interface.

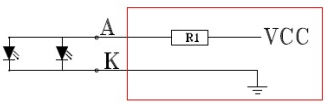
3.Basic parameters of display screen:

project	Specifications	unit
Display Mode	DFSTN/Black background with white text------FSTN/Black text on white background	
LCDBias ratio	1/64 duty, 1/9 bias	- - -
Logic Power (VDD)	3.3	V
Viewing angle	6	o'clock
Dimensions	47.5×30.5×5	mm
VAarea	43.6×22.4	mm
AAarea	41.7×20.36	mm
Number of driving dots	128 × 64	dots
Operating temperature	-10 ~ +60	℃
Storage temperature	-20 ~ +70	℃

4.Display screen size diagram:



LED电路图 CIRCUIT DIAGRAM (LED 1*3=3 dies)



限流电阻：

VCC=5.0V R1=51R~68R
VCC=3.3V R1=10R~15R

客户电路板限流设置

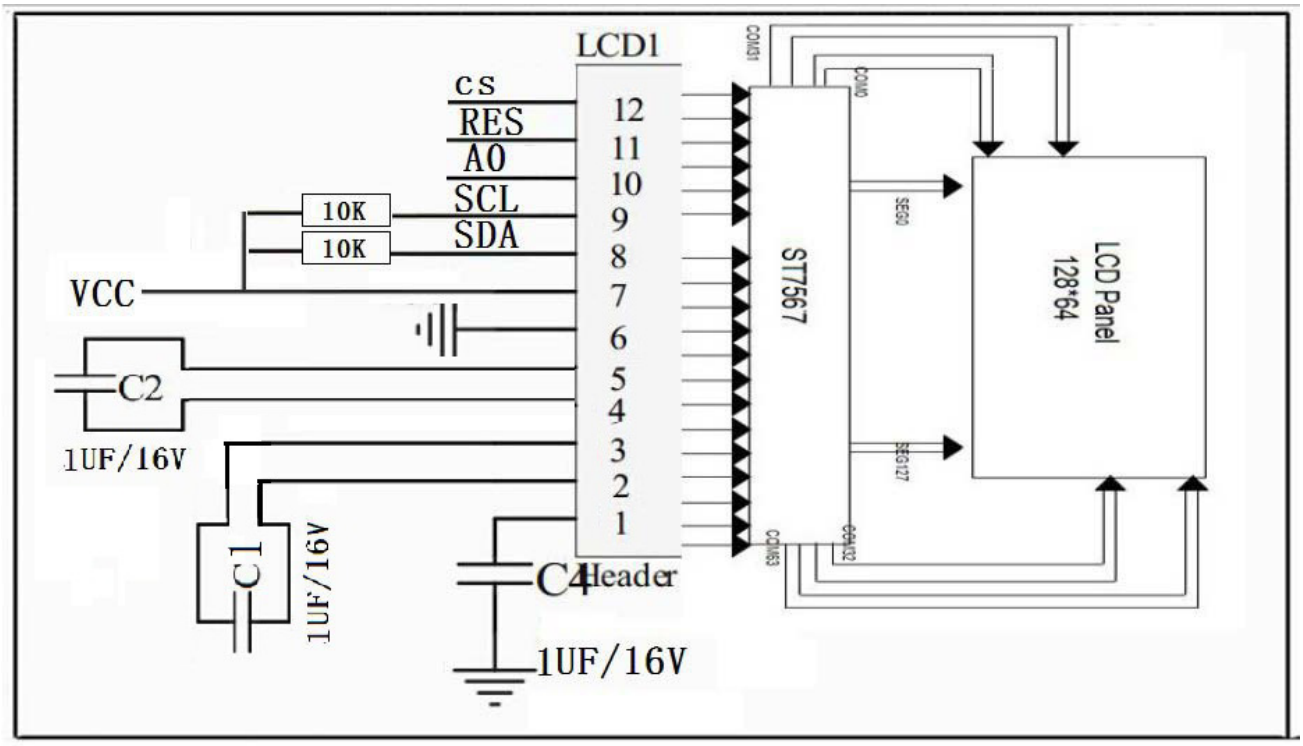
5.Display interface definition:

5.1

Serial number	name		Function
1	VG	- - -	LCDVoltage doubler output, withVSSThis is a capacitor
2	XVO	- - -	Voltage doubler circuit, capacitor connected between two wires.
3	VO	- - -	Voltage doubler circuit, capacitor connected between two wires.
4	VO	- - -	Voltage doubler circuit, capacitor connected between two wires.
5	XVO	- - -	Voltage doubler circuit, capacitor connected between two wires.
6	VSS	- - -	Grounding
7	VDD	H	3.3V
8	D7（SDA）	H/L	Serial data input

9	D6（SCL	H/L	Serial clock input
10	A0	H/L	Instruction and data selection portsA0=H：To display the numberA0=L：For control instructions
11	RES	H/L	Hardware reset input pin, when it is low level, the circuit is reset
12	CS	H/L	Chip select input pin, low level enables

5.2Peripheral connection diagram:



6.Technical Parameters

6.1Limit parameters

Unless otherwise specified,T_{amb}=25℃,VSS=0V

Parameter name	symbol	Rating	unit
Digital supply voltage	VDD	- 0.3～ +3.6	V
Analog supply voltage	VDD2	- 0.3～ +3.6	V
LCDSupply voltage	VOUT,V0	- 0.3～ +13.5	V
LCDBias voltage	V1,V2,V3,V4	- 0.3~V0	V
Logic input voltage	VIN	- 0.3~V_{DD}+ 0.3	V
Operating temperature	T_{amb}	- 10～+60	℃
Storage temperature	T_{stg}	- 20～+70	℃

Note:1,V0, VDD2, VG, VM, VSSandXV0The matching relationship:V0 ≥ VDD2 > VG > VM > VSS ≥ XV0

6.2**DC parameters1**

Unless otherwise specified,T_a=-30℃～+80℃,VSS_C=0V

Parameter name	symbol	Test conditions		Standard value			unit	correspond port
				Minimum	typical	maximum		
Operating voltage (1)	VDD1			1.7	-	3.3	V	VDD1
Operating voltage (2)	VDD2			2.4	-	3.3	V	VDD2
Operating voltage (3)	VDD3			2.4	-	3.3	V	VDD3
Input high level voltage	V_{IHC}			0.7VDD1	-	VDD1	V	MPUcatch mouth
Input low level voltage	V_{ILC}			VSS1	-	0.3VDD1	V	MPUcatch mouth
Output high level voltage	V_{OHC}	I_{OUT}=1mA,VDD1=1.8V		0.8VDD1	-	VDD1	V	D[7:0]
Output low level voltage	V_{OLC}	I_{OUT}=-1mA,VDD1=1.8V		VSS1	-	0.2VDD1	V	D[7:0]
Input leakage current	I_{LI}			- 1.0	-	1.0	μA	MPUcatch mouth
Output leakage current	I_{LO}			- 3.0	-	3.0	μA	MPUcatch mouth
LCD driver on-resistance	R_{ON}	T_a=25℃	VOP=8.5V, ΔV = 0.85 V	-	0.6	0.8	KΩ	COMX
			VG=1.9V, ΔV = 0.19 V	-	1.3	1.5	KΩ	SEGX
Frame rate	FR	Duty=1/65, OP=8.5V, T_a=25℃		70	75	80	Hz	

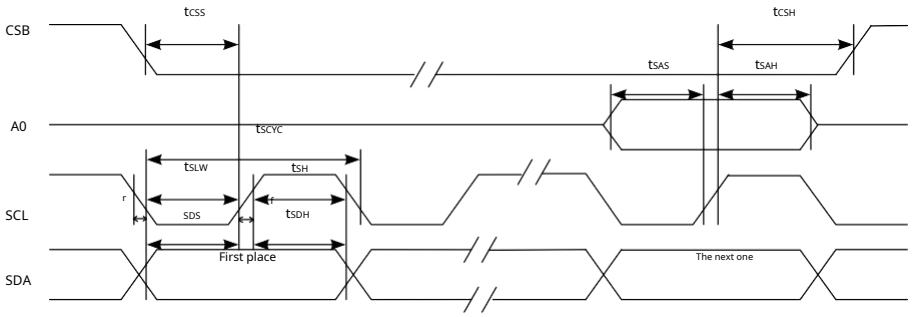
6.2.1DC parameters2

Current consumption: output display, internal power supply working, current consumption of the entire bare chip

Working status	symbol	Test conditions	Standard value			unit
			Minimum	typical	maximum	
show: SNOW(static)	ISS	VDD1=VDD2=VDD3=3.0V, double pressureX5, VOP=8.5 V, Bias=1/9,Ta=25℃	-	150	300	μA
Display Off	ISS	VDD1=VDD2=VDD3=3.0V, double pressureX5 , VOP=8.5 V, Bias=1/9,Ta=25℃	-	95	190	μA
Power off	ISS	VDD1=VDD2=VDD3=3.0V,Ta=25℃	-	8	16	μA

7.Read and write timing characteristics

Serial4Line interface timing parameters



picture6, AC parameters3

(VDD1 = 3.3V, Ta = 25℃)

Parameter name	correspond port	symbol	Test conditions	Standard value		unit
				Minimum	maximum	
Serial clock cycle	SCLK	tQC		50	—	ns
SCLK HPulse Width		wxya		25	—	
SCLK LPulse Width		tW		25	—	
Address creation time	A0	tSAS		20	—	
Address hold time		tH		10	—	
Data creation time	SDA	tD		20	—	
Data retention time		oeLh		10	—	
CSBarriveSCLKhour between	CSB	tCSS		20	—	
CSBarriveSCLKtime		tC		40	—	

(VDD1 = 2.8V, Ta = 25℃)

Parameter name	correspond port	symbol	Test conditions	Standard value		unit
				Minimum	maximum	
Serial clock cycle	SCLK	tQC		100	—	ns
SCLK HPulse Width		wxya		50	—	
SCLK LPulse Width		tW		50	—	
Address creation time	A0	tSAS		30	—	
Address hold time		tH		20	—	
Data creation time	SDA	tD		30	—	
Data retention time		oeLh		20	—	
CSBarriveSCLKhour between	CSB	tCSS		30	—	
CSBarriveSCLKtime		tC		60	—	

(VDD1 = 1.8V, Ta = 25℃)

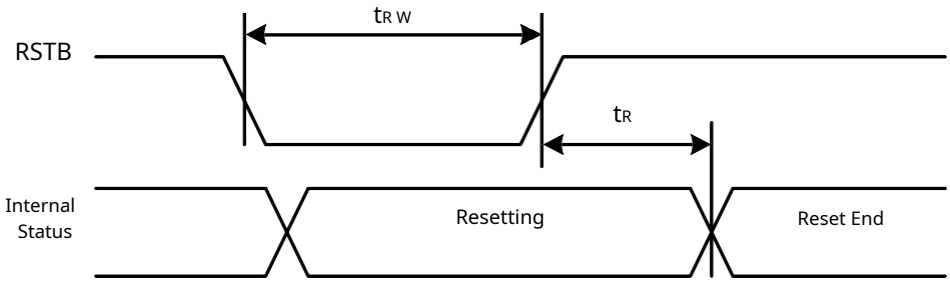
Parameter name	correspond port	symbol	Test conditions	Standard value		unit
				Minimum	maximum	
Serial clock cycle	SCLK	tQC		200	—	ns
SCLK HPulse Width		wxya		80	—	
SCLK LPulse Width		tW		80	—	
Address creation time	A0	tSAS		60	—	
Address hold time		tH		30	—	
Data creation time	SDA	tD		60	—	
Data retention time		oeLh		30	—	
CSBarriveSCLKhour between	CSB	tCSS		40	—	
CSBarriveSCLKtime		tC		100	—	

Note:1、Rise and fall time of input signal (tr, tf)want≤15 ns.

2, the reference voltage for all timing tests is20% VDD1arrive80% VDD1.

7.1 Hardware Reset Timing

parameter



picture7, AC parameters4

Parameter name	symbol	Test conditions	Standard value		unit
			Minimum	maximum	
Reset time	R		—	1.0	us
RESET LPulse Width	tW		1.0	—	

(VDD1 = 3.3V, Ta = 25℃)

(VDD1 = 2.8V, Ta = 25℃)

Parameter name	symbol	Test conditions	Standard value		unit
			Minimum	maximum	
Reset time	R		—	2.0	us
RESET LPulse Width	tW		2.0	—	

(VDD1 = 1.8V, Ta = 25℃)

Parameter name	symbol	Test conditions	Standard value		unit
			Minimum	maximum	
Reset time	R		—	3.0	us
RESET LPulse Width	tW		3.0	—	

7.2

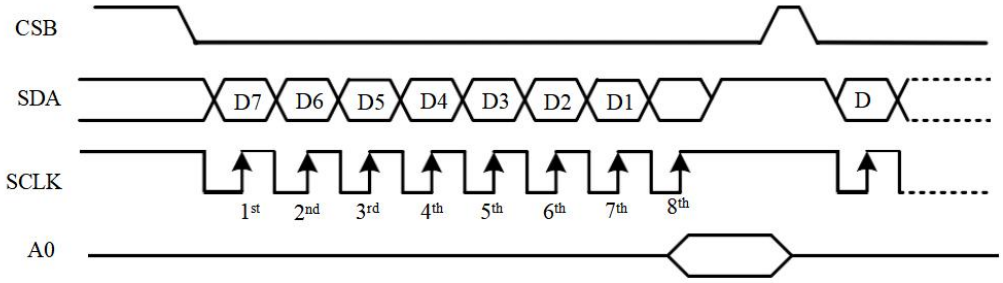
SPI4Line serial communication (PSBis high level,C86Set the serial interface to high or low

Communication Mode	PSB	C86	CSB	A0	ERD	RWR	D[7:0]
SPI 4Line serial communication	L	X	CSB	A0	- -	- -	SDA,SCLK,--,--,--,--,--,--

Note:1, the pins marked with "--" must be shorted to a high potential,VDD1,

VDDH 2,C86Marked as "×", can be connected to high potential or low potential

whenCSBWhen it is low, the chip can communicate, serial data (SDA) and the serial clock (SCLK) to start working.CSBWhen it is high level,ST7567Unable to communicate, internal8Shift registers and3When the circuit is in serial mode, the bit counter is reset. SDAThe above data isSCLKThe rising edge of the eighth clock is stored in the shift register.A0The signal storage of the port generates a pulse signal at the same time, converting the serial data into parallel data, and the subsequent data processing is exactly the same as the parallel signal.DDRAMAfter accessing each byte,DDRAM columnThe address pointer will automatically increase by one.SCLKThe anti-interference ability is very important, and external noise will cause abnormal data or commands to appear.



picture8,4WireSPIaccess

Note:1, when in power saving mode or after hardware reset, some microprocessors tend to be in a high impedance state. VDD1This is not allowed because it will cause an abnormal state at the floating input terminal of the circuit.

7.3, data transmission

ST7567The interface data transfer is performed using the bus latch and the internal data bus.MPUTowardsDDRAMWhen writing data, the data is automatically transferred from the bus latch to theDDRAM, as shown in the figure4When from the filmDDRAMRead data toMPUWhen the first read cycle reads the contents of the bus latch (empty read), the next read cycle will outputMPUThe data that should be read is as shown in the figure5This means that after setting the target address, an idle read cycle is required before the next read operation. Therefore, some data that requires precision cannot be read in the first read cycle after setting the target address, but can be read in the second read cycle.

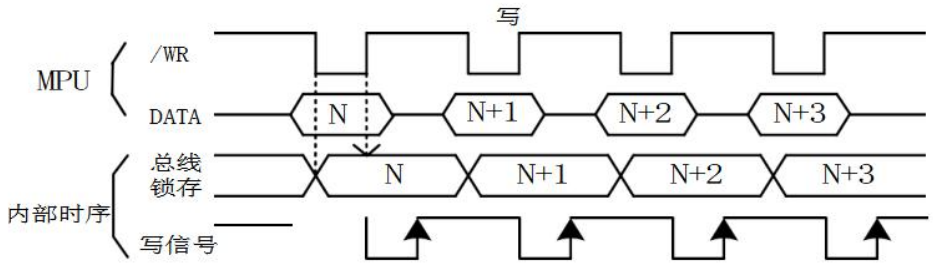


图 9 、数据传输：写

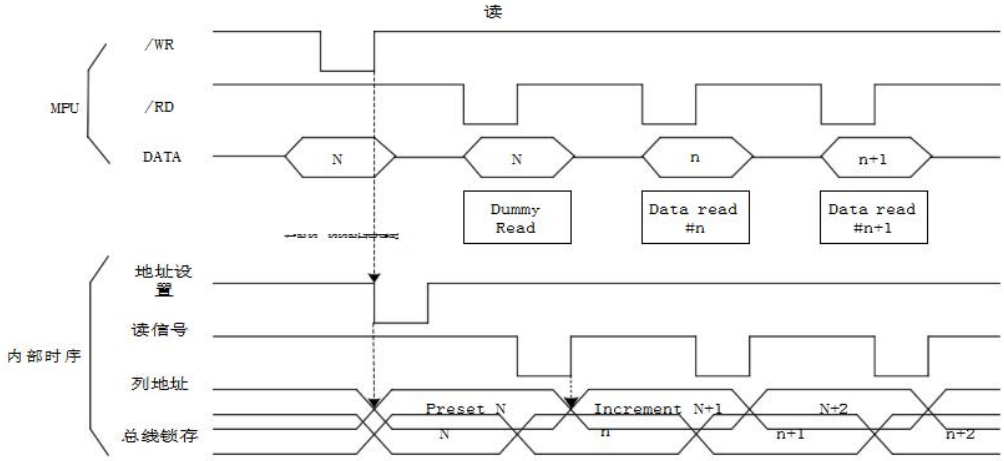


图 10、数据传输：读

7.4, Display data

ST7567Built-in circuit65*132bitofDDRAMUsed to store display data, display dataRAM （DDRAM) storedLCDThe point data can be set by132Column and65line to control the display.DDRAMand LCDThe corresponding relationship between the screen and the communication address is shown in the figure6When inMPUIn communication mode,DDRAMquiltX,Y Address split into9OK,132Columns, each column8bitData, when inLCDIn display mode,DDRAMDivided into65Line, each line 132bitData, where rows are divided into pages,Page0~Page7Each page has8OK (correspondCOM0~63),Page8only There is a line (corresponding toCOMMS, used for image display). Display data (D7 ~D0)correspondLCDofCOMrow direction,D0 ~D0 In the first place. All pages except image pages can beD7 Direct access. ImageRAMJust use the number According to the busD0This one. See picture7.MPUCan beI/OThe bus performs read and write operations.LCDThe drives can be operated independently, and data can be written synchronously while being displayed, without causingLCDFlickering or data conflict.

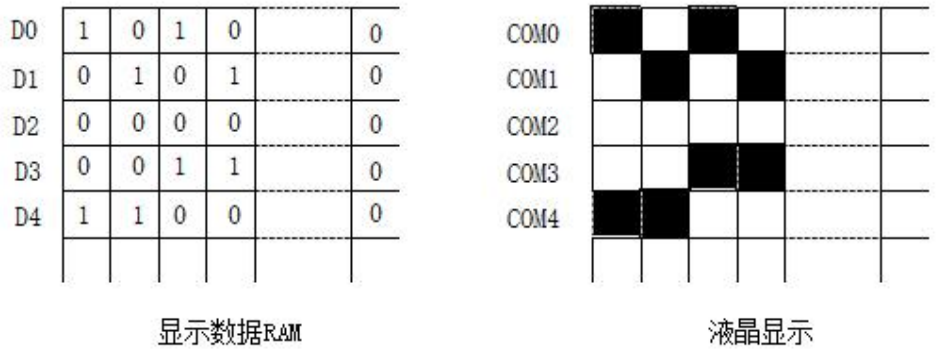


图 11、 DDRAM 的数据与显示屏的对应关系

图 12、 读写地址与 DDRAM 的对应关系

Note: In serial mode, you can only write but not read

7.5, Addressing

ST7567Display dataRAMfor132bit*65, the address range is:X=0~131(column address),Y=0~8(page address). Data outside this range is invalid.

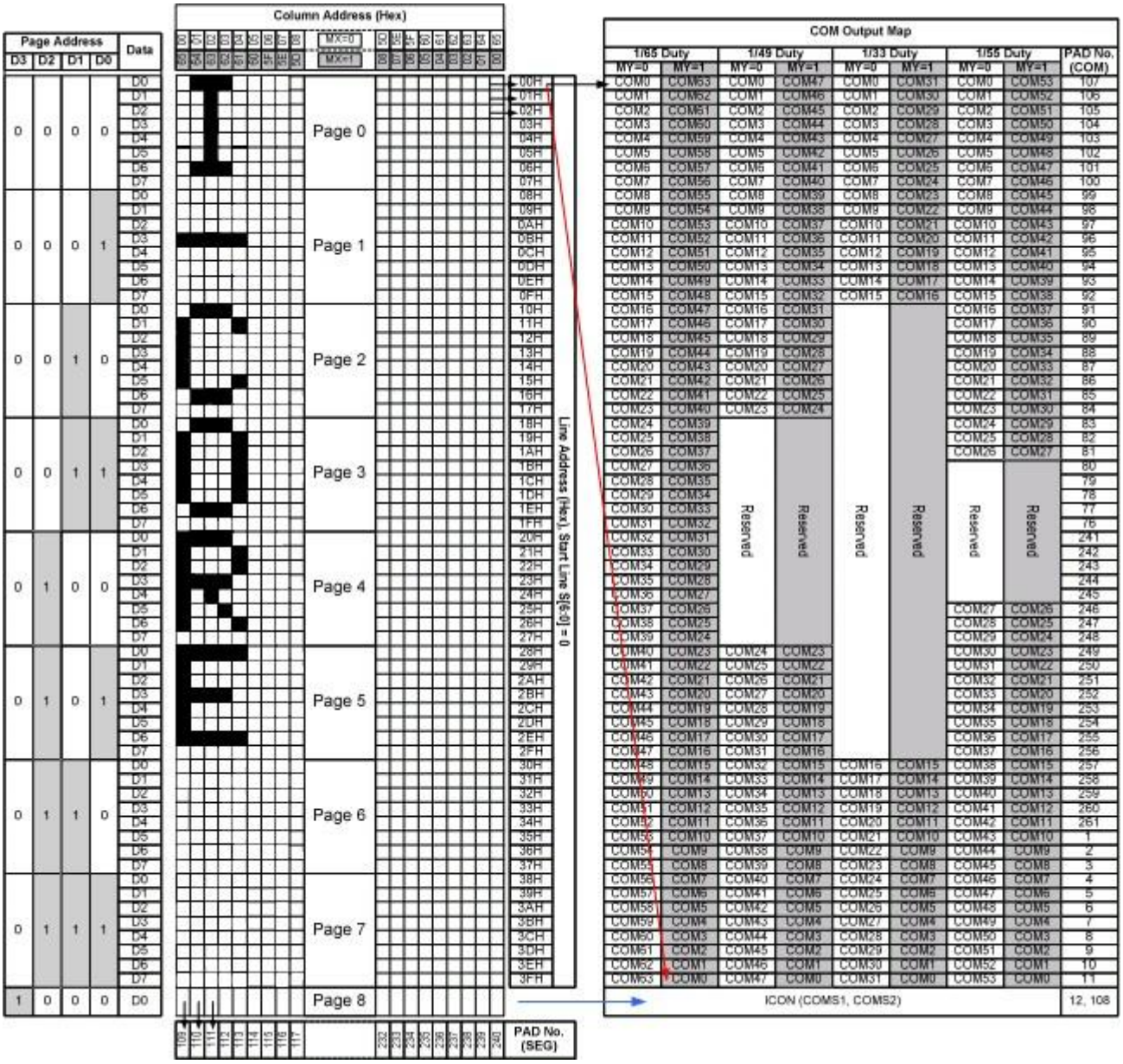
7.6, Page address circuit

This circuit consists of a4bit page address register, can only bePAGEADDRESSSET"Instructions can be modified to provideDDRAMThe page address must be in the accessDDRAMSet before the content, page address8It is a special one for image display.RAMThere is only one legal operation bit:D0.

7.7, column address circuit

DDRAMThe column address is determined by theCOLUMN ADDRESS SET"The column address is set by the command. The column address is incremented after each display data access (read/write).1,thereforeMPUContinuous accessDDRAMHowever, since the page address circuit and column address circuit are independent, this feature can only be executed until the end of each page (column address "83H") For example, from (page - 0,List -83H) to (page -1,List -0) , both the page address and the column address need to be reassigned to changeDDRAMpointer.

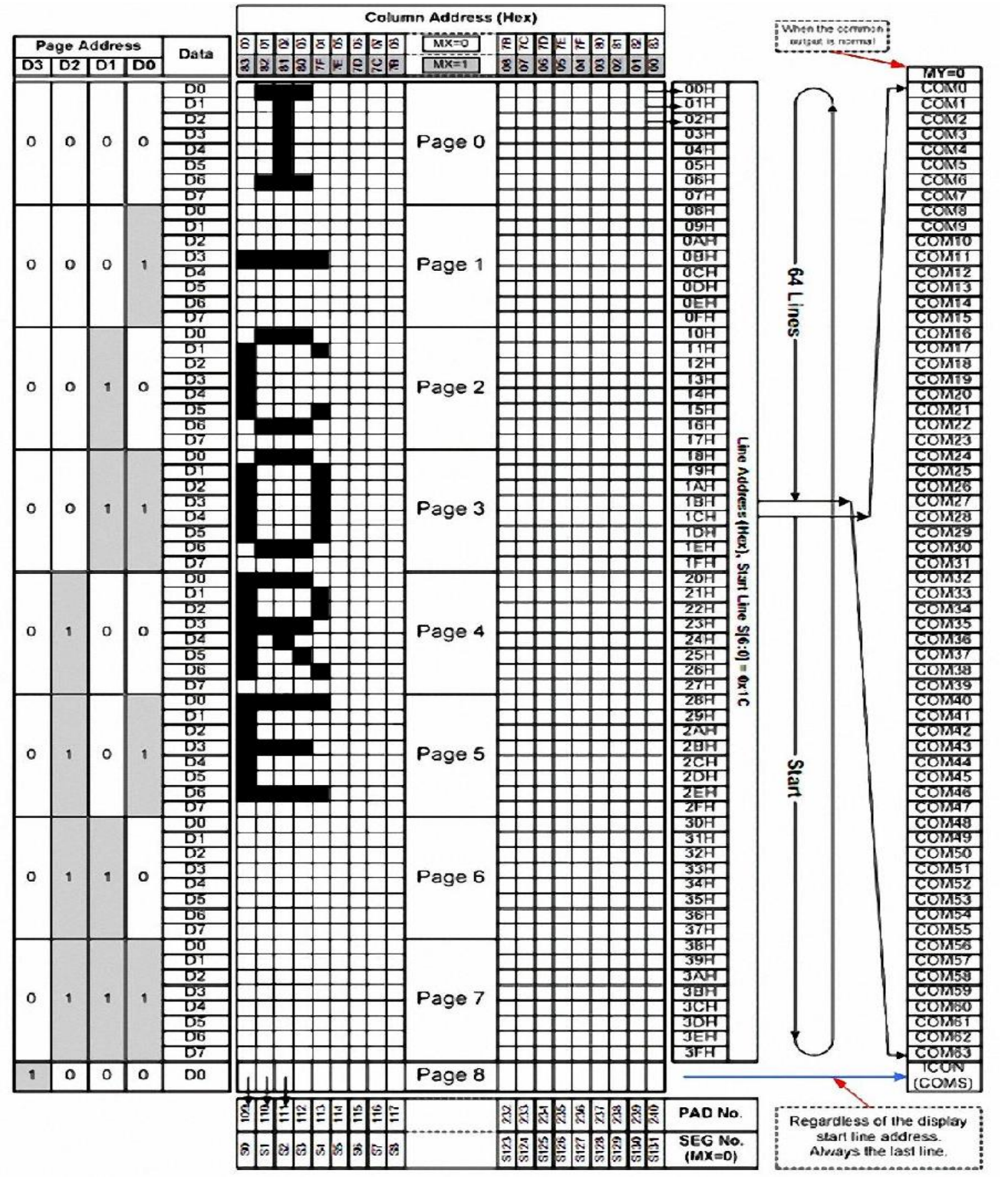
In addition, the registerMXandMYCan be reversedDDRAMWith output (COM/SEG) is changingMX After the setting, the display data must be rewritten toDDRAMinside.



picture13,DDRAMData andSEG,COMThe corresponding relationship

7.8, row address circuit

The row address circuit consists of a counter and a row address register. The row address register consists of a DISPLAY STARTLINESET"This circuit is assigned toDDRAMA row address, to be used as the first row of the display (COM0） Therefore, by repeatedly setting the row address,ST7567Can not changeDDRAMContent to achieve screen scrolling.9The last line is alwaysCOMMS(Used as line output for images) , that is, the image will not be displayed as usual The data rolls together.



picture14,DDRAMCorrespondence between data and starting row

relation

8.0, Oscillation circuit

ST7567The built-in oscillator circuit generates the system clock required by the LCD driver circuit.ST7567After initialization, the oscillation circuit is activated. To reduce power consumption, the clock is not output.

8.1, LCD drive power circuit

ST7567Built-in power circuit to generate voltage to drive the liquid crystal. The circuit uses minimal peripheral components to reduce power loss. The built-in power circuit includes a voltage doubler, a voltage regulator, and a voltage follower circuit.ST7567A power off procedure is required before power off (refer to the operation flow section) .

8.2, peripheral components of power supply circuit

The recommended power peripheral components are only two capacitors. The specific values of these two capacitors are determined by the size of the screen and the load.

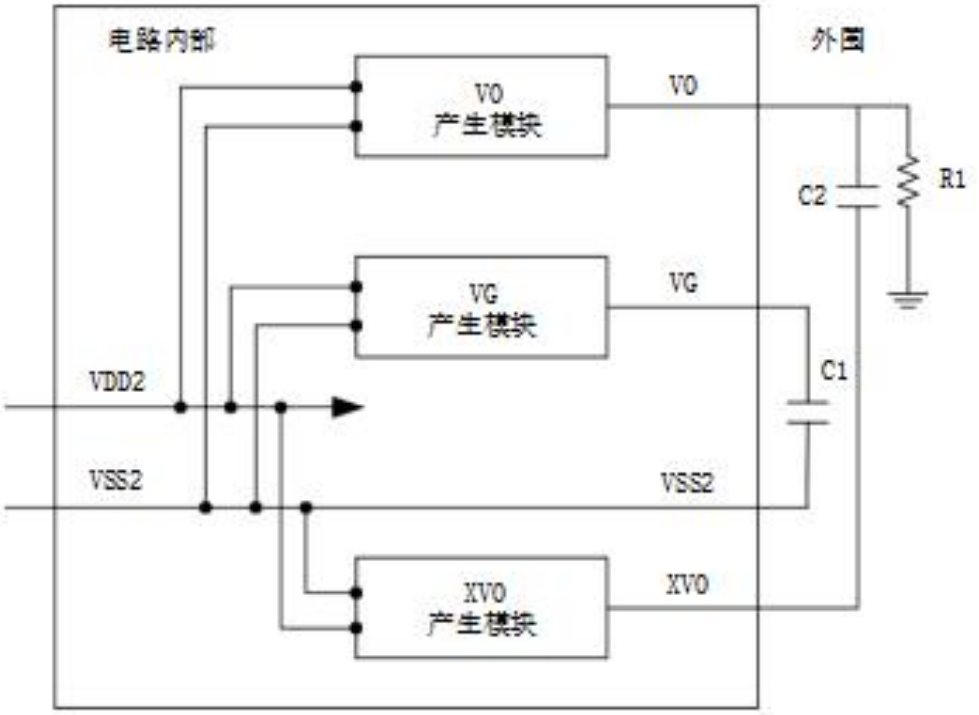


图 15、电源电路

8.3, Regulator Circuit

ST7567Built-in high-precision regulator circuit, total8Adjustment ratio (Regulation ratio—RR), eachRRhave64indivual EV No additional external components are required, and the output voltage can be adjusted byRegulation Ratio”and"Set EV” The instruction description section has detailed setting methods.

8.4, reset circuit

ST7567Depend onRSTBThe port is set low to initialize the internal circuit.RSTBWhen set low, except for the read status instruction, all other instructions are invalid.RSTBThe hardware reset is different from the software reset. RSTBbecomes low, the hardware reset procedure will start; when executingRESETAfter the command is given, the software reset procedure will be started.

register	RSTBHardware reset value	RESETSoftware reset value
Display Off:D=0,allSEGandCOMOutputs are low	V	X
Normal display:INV=0,AP=0	V	X
SEGNormal display	V	X
Serial counter and shift register cleared (if serial interface is used)	V	X
Bias selection:BS=0	V	X
Voltage doubling range:BL=0	V	X
Exit power saving mode	V	X
Power off control:VB=0,VR=0,VF=0	V	X
Exit read-write correction mode	V	V
Starting line:S[5]=0	V	V
Line Address:X[7:0]=0	V	V
Page address:Y[3:0]=0	V	V
COMNormal display mode:MY=0	V	V
V0Adjustment rate:RR[2:0]=(1,0,0)	V	V
EV[5:0]=(1,0,0,0,0,0)	V	V
Exit test mode	V	V

After power on,RAMData is undefined, and the display status is "display off". It is best to initialize the entireDDRAM (For example: fill in the full00hor write display pattern)In addition, the power is unstable when it is just turned on, and it needs to be repaired after the power is stable. Perform a hardware reset to initialize the internal registers.

9.Instruction Description

9.1. General Instruction List

sequence Number	instruction	A0	R/W (RW R)	Instruction bit								describe
				D7	D6	D5	D4	D3	D2	D1	D0	
1	Display on/off (display on/off)	0	0	1	0	1	0	1	1	1	D	D=1, display on D=0, display off
2	Set the starting line (set start line)	0	0	0	1	S5	S4	S3	S2	S1	S0	Set the starting line of the display
3	Set the page address (set pageaddress)	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
4	Set the column address (setcolumn address)	0	0	0	0	0	1	X7	X6	X5	X4	Set the column address high bit (MSB)
		0	0	0	0	0	0	X3	X2	X1	X0	Set column address position (LSB)

5	Read Status (read status)	0	1	0	MX	D	RST	0	0	0	0	ReadICStatus
6	Writing Data (write data)	1	0	D7	D6	D5	D4	D3	D2	D1	D0	rightDDRAMWriting Data
7	Read Data (read data)	1	1	D7	D6	D5	D4	D3	D2	D1	D0	ReadDDRAMData
8	SEGDisplay Mode (segdirection)	0	0	1	0	1	0	0	0	0	MX	set upSEGScan direction MX=1, showing left and right reversed MX=0, normal display
9	Reverse (inverse display)	0	0	1	0	1	0	0	1	1	INV	INV=1, reverse display INV=0, normal display
10	Full screen (all pixels on)	0	0	1	0	1	0	0	1	0	AP	AP=1, the screen lights up completely AP=0, normal display
11	Bias selection (biasselect)	0	0	1	0	1	0	0	0	1	BS	Bias selection 0=1/9;1=1/7(1/65 Duty Cycle)
12	read-modify-write	0	0	1	1	1	0	0	0	0	0	Row address increment: Read:+0, write: +1
13	END	0	0	1	1	1	0	1	1	1	0	quit

												read-modify-write model
14	Reset(RESET	0	0	1	1	1	0	0	0	1	0	Software reset
15	COMScanning method (comdirection)	0	0	1	1	0	0	MY	-	-	-	set upCOMScan direction MY=1, upside down MY=0, normal display
16	Power Control (power control)	0	0	0	0	1	0	1	VB	VR	VF	Setting the internal power supply Managing the circuit work
17	RRset up (regulation ratio)	0	0	0	0	1	0	0	RR2	RR1	RR0	chooseRRResistance Range
18	EVset up(set EV)	0	0	1	0	0	0	0	0	0	1	Double line command setting PlaceEVgrade
		0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
19	Setting the voltage doubler (setbooster)	0	0	1	1	1	1	1	0	0	0	Two-line instructions Set the voltage multiplier level: BL=0:4times BL=1:5times
		0	0	0	0	0	0	0	0	0	BL	
20	Power saving mode (power save)	0	0	Reuse Instructions								display off + all pixel on
twenty one	No operation (nop)	0	0	1	1	1	0	0	0	1	1	No Action
twenty two	test(test)	0	0	1	1	1	1	1	1	1	-	Test Instructions

Note: "-" can be connected to "H"or"L"

9.2, Display on/off (display on/off)

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	D

D=1, display on

D=0, display off, allSEG,COMThe port is set to0Level

9.3, set the starting row (set start line)

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S5	S4	S3	S2	S1	S0

The role of setting the starting line is to selectDDRAMMiddleS[5:0]The specified display data is inCOM0The above is displayed, and the rest of the data is looped according to the address increment to set the scrolling effect of the screen.

S5	S4	S3	S2	S1	S0	Display Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	.
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

9.4, set the page address (set page address)

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	Page address	Valid bits of data
0	0	0	0	page0	D7~D0
0	0	0	1	page1	D7~D0
0	0	1	0	page2	D7~D0
.	.	.	.	.	.
0	1	1	0	page6	D7~D0
0	1	1	1	page7	D7~D0
1	0	0	0	page8（Icon page）	D0

9.5. Set column address

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4
0	0	0	0	0	0	X3	X2	X1	X0

The row address can be selected in the range of0~131, two instructions are required to complete the complete setting.

X7	X6	X5	X4	X3	X2	X1	X0	Row Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

9.6, write data (write data）

A0	R/W(RWR)	D6	D5	D4	D3	D2	D1	D0
1	0	D6	D5	D4	D3	D2	D1	D0

After the address setting is completed,MPUCan be continuouslyDDRAMWrite data, but after a row is written, it must be resetX,YThe next row of data can be written only after the address isXAfter the address overflows, the original input data will be overwritten.

9.7,SEGDisplay mode (seg direction）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

MX=0: Normal display mode (SEG0->SEG131

） MX=1: Left-right inverted display mode (

SEG131~SEG0）

9.8、Reverse display（inverse display）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

INV=0: Normal display mode

INV=1: Invert display mode

9.9, full screen (all pixel on）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

AP=0: Normal display mode

AP=1: Full screen display mode

Mode

10, bias selection (bias selection）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	BS

10.1, Reset (RESET）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

After executing this instruction, the circuit enters the software reset state. The register values are detailed in the reset state register table.

10.2,COMScan mode (com direction）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	-	-	-

MY=0: Normal scanning display mode (COM0~COM63）

MY=1: Upside-down scanning display mode (COM63~COM0）

10.3, Power saving mode (power save）

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	0
0	0	1	0	1	0	0	1	0	1

ST7567The power saving mode of the circuit is realized by using two instructions together. The first instruction is to set the display off. （D=0），

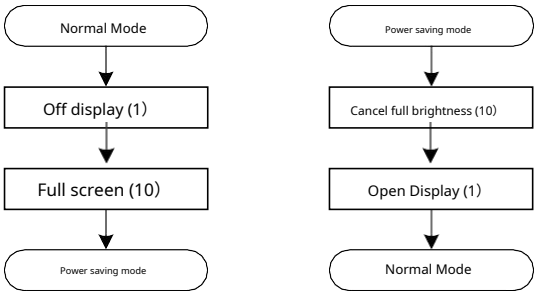
The second instruction is to set the screen to full brightness (AP=1），then the circuit enters power saving mode, the circuit works when entering power saving mode

state:

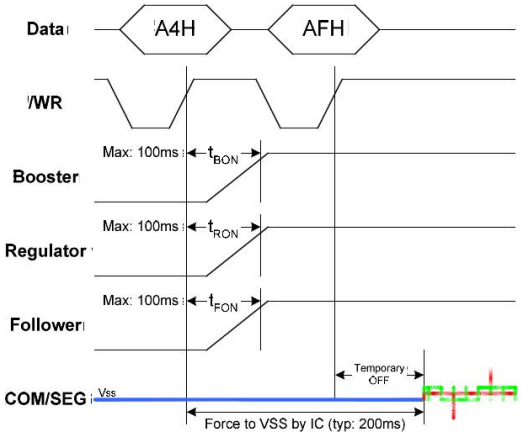
1,RCClock Off

2, the built-in power management circuit shuts down

3,LCDThe timing of the shutdown occurs, allCOM,SEGThe port is set to0Potential



whenFD=0When the circuit works according to the following timing sequence



picture19, Working sequence

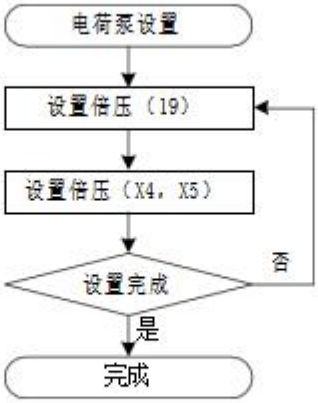
When exiting the power saving mode, the above two instructions are executed. After exiting the power saving mode, the circuit returns to the configuration state before the power saving mode.

10.4, set the voltage multiplier (set booster)

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	0	BL

BL=0：4 倍压

BL=1：5 倍压



11. 、NOP

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

当设置为这条指令时，电路不执行任何操作

11.1、工作时序

11.2、电路上电

工作流程：

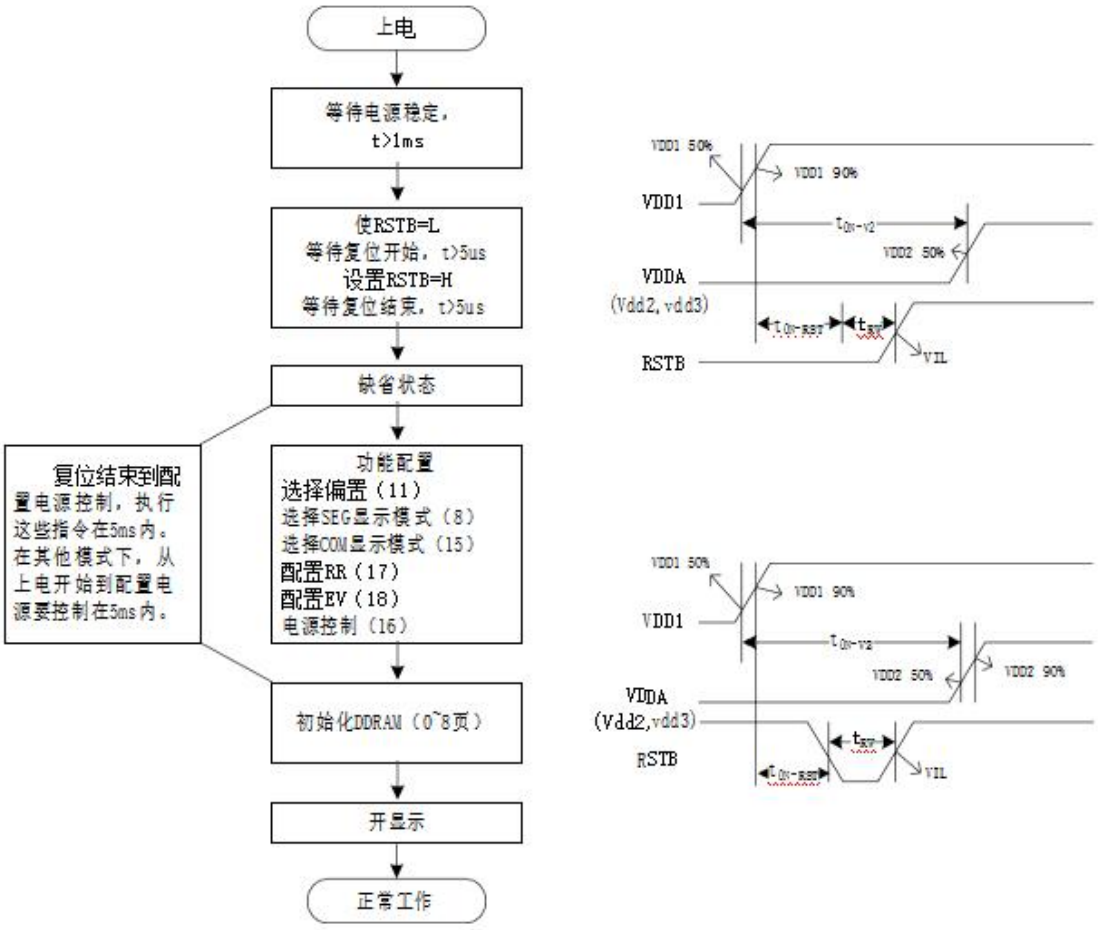


图 21、上电时序

注：下面表格有参数的详细描述

1、 tRW 和 tR 请参考时序参数指标

2、 RESET 请参考4.11.6节说明

3、 5ms 是为了符合LCD屏的规格和电源部分外接器件的要求。可根据实际使用的器件来检测

4、 INSTRUCTION 功能的详细描述见4.11节说明

5、 VDDI 或者 VDDA电压上升到预定值的90%时，被视为电源的稳定态。

11.3、时序要求：

参 数	符号	条件	备注
VDDA 电源延时	tON-V2	0 ≤ tON-V2	VDDI 和 VDDA 在任何情况下都不会损坏电路。
RSTB 输入时间	tON-RST	没有限制	● 在上电期间，如果RSTB 为低电平、高电平或者补丁态，RSTB有效的外部复位应该是在VDDI 电压稳定后。 ● 电源电压稳定后，在任何时候都可以使RSTB置为低电平。 ● tRW 和 tR 必须符合RSTB的时序要求。 ● 防止损坏显示，推荐的时序是： 0 ≤ tON-RST ≤ 30 ms.

注：表中给出的时序要求是为了防止损坏LCD模组

11.4、显示数据

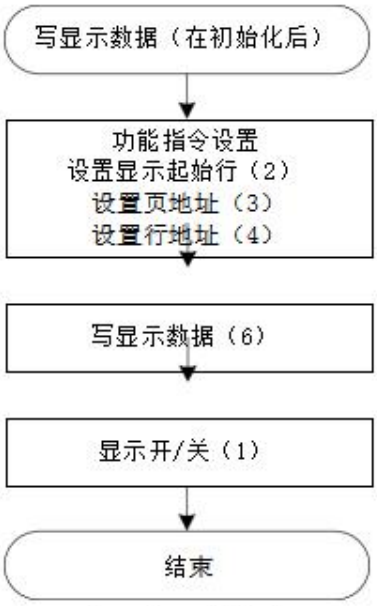


图 22、显示数据流程

注：参考项目

1、 INSTRUCTION 功能的详细描述见4.11节分说明

2、 在显示打开之前，推荐要写入显示数据，即初始化DDRAM

11.5、刷新

推荐在固定的间隔时间刷新时序

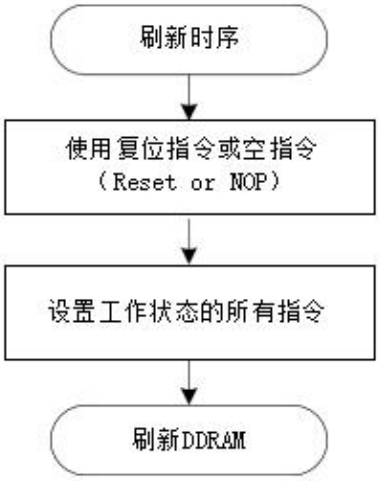


图23、刷新流程

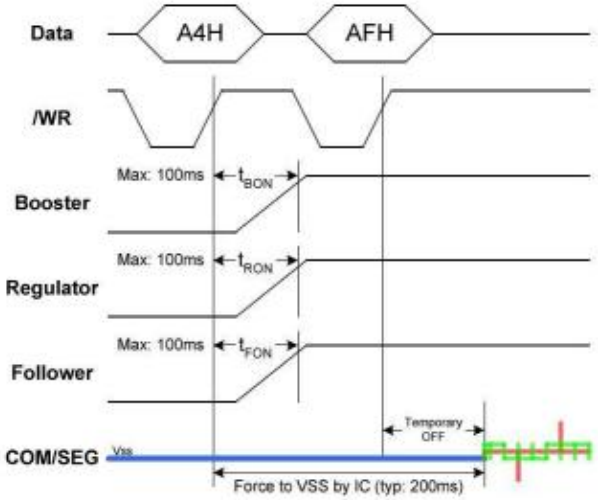


图24、刷新时序

注：

1、 电源稳定时间取决于加载的LCD屏。

2、 上图中给出的电源稳定时间的条件是：LCD屏尺寸=1.4”， C1=1uF，C2=1uF，VDD=2.7V，Vop=9V。

11.6 、电路掉电时序及流程

电路在省电模式时，LCD输出端拉到VSS，模拟输出端处于放电状态，电源电压关断。下面给出的两种方式可以触发电路进入省电模式。

使用省电模式

掉电流程：

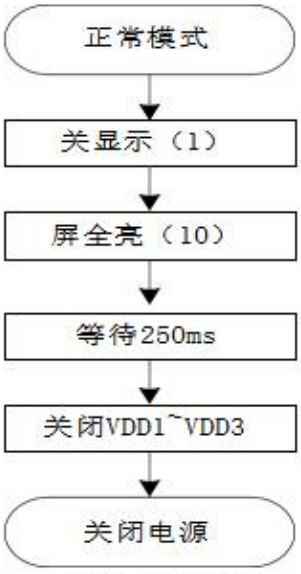


图25、掉电流程

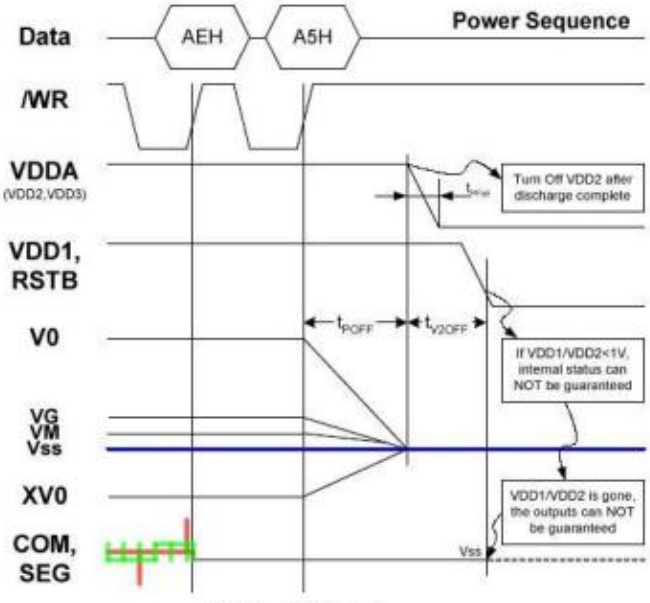


图26、工作时序：

在内置电源电路关断和完全放电之后，VDD1和VDDA电压被移掉。

11.7、硬件复位功能：掉
电流程：

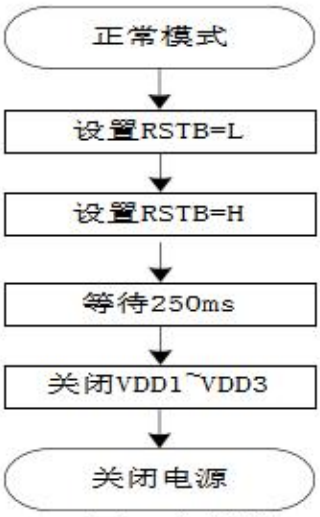


图27、掉电流程

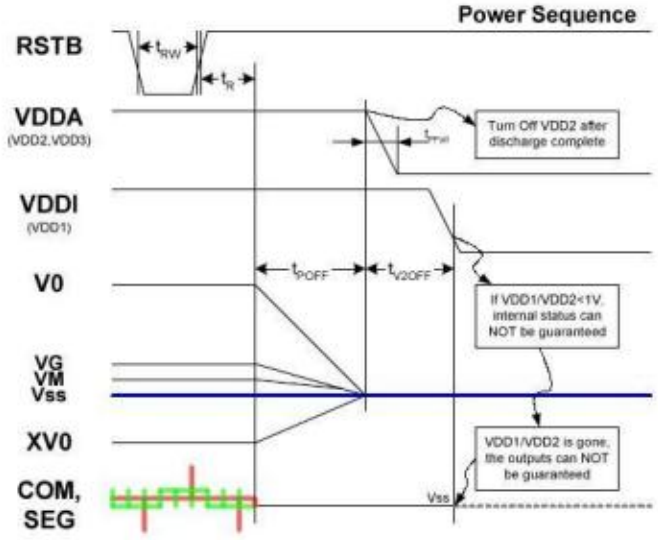


图28、工作时序

在内置电源电路关断和完全放电之后，VDD1和VDDA电压被移掉。
注：
1、 tPOFF：内部电源放电时间≥250ms(最大)
2、 tV2OFF ：VDDI 和 VDDA关断时间≥0ms(最小)
3、 不建议在VDDA关断前，先关断VDDI。关断了VDDI，电路内部状态不稳定，可能会停止放电。未被放掉的电压可能会流入COM/SEG输出端，及极化LCD屏。
4、 VDDI 和 VDDA 不同时供电，不会损坏电路
5、 时序与负载屏和外接电容有关
6、 上图中的时序测试条件：LCD P屏尺寸 = 1.4” ， C1=1uF, C2=1uF
7、 VDDA关断时，下降时间要满足如下要求：20ms ≤ tPFall ≤ 0.2s

12. Sample reference program:

```
/********************************************** ************/ //
driver IC       :    st7567
// LCD             :       1/65 duty, 1/9 bias, 8.8V vop
// interface    :    SPI
//ver             :  00
// date           :   - 07
//other          :  VDD 3.1v
/********************************************** *************/
#include "reg51.h"
/*

   sbit RS = P3^7;      AO
   sbit RES = P3^3;     Reset
   sbit CS = P3^4;      Partial Selection
   sbit SCL = P1^1;
   sbit SDI = P1^0;
* /

   sbit CS = P1^0;
   sbit RES = P1^1;
   sbit RS = P1^2;
   sbit SCL = P1^3;
   sbit SDI = P1^4;




//   sbit SCL = P1^6;
//   sbit SDI = P1^7;
     sbit    key1=P2^1;
   sbit      key2=P2^2;
```

```
   sbit      pause=P2^0;
void writec(uchar);
void stop(void);
void writed(uchar);

#define    uchar     unsigned char
#define    uint     unsigned int
  uchar vop=0x29;

uchar code chara1[]= { /
*--     An image was loaded:C:\Users\02.bmp    --*/
/*--    widthxHeight =128x64 --*/
};ucharcodechara2[]=
{/*Imagesize:128x64pixels*//*--.....C:\Users\1.bmp--*/ /
```

```
 void delay1(unsigned int t)
{
   while(t>0)
   {
      t--;                    //TT-                                    `
      pause=1;
      if(pause==0)stop();
   }
}


 void flash(unsigned int t)
{
   while(t>0)
   {
      t--;                    //TT-                                    `


   }
}
//-----------------------------
            void stop()
            {
```

```
    flash(100);
    while(pause==0)
    {
      pause=1;
      key1=1;
      key2=1;
      if(key1==0)
      {
      flash(200);
      if(key1==0)
      {

      while(key1==0);
      flash(100);
         if(vop<63)
         {
         vop++;
      writec(0x81);
         writec(vop);}
         }
}
      else if(key2==0)
      {
        flash(100);
    if(key2==0)
      {

        while(key2==0);
        flash(100);
        if(vop>0)
        {
          vop--;
      writec(0x81);
         writec(vop);
      }
        }
```

```
            }
          }
       }

void writec(uchar com)
{ unsigned char i ;
  CS=0;
  RS=0;

    for(i=0;i<8;i++)
     { com=com<<1;
     SDI=CY;
     SCL=1;
     SCL=0;
     }

      CS=1;
  RS=1;
 }

void writed(uchar dat)
{ unsigned char i;
  CS=0;
      RS=1;

   for(i=0;i<8;i++)
      {

      dat=dat<<1;
     SDI=CY;
     SCL=1;
     SCL=0;
     }

      CS=1;
  RS=1;
```

```
}

  void init ( )
{
       uchar col;
     RES=1;
     flash(1000);
     RES=0;
     flash(2000);
     RES=1;
     flash(1000);

  writec(0xe3);      // reset signal
  writec(0xa3);      //(0xa2 1/9 bias,1/65
  writec(0xa0);      duty) // ADC select
  writec(0xc8);      // command output select //
  writec(0x2f);      power control
  writec(0x24);      // select resistor ratio Rb/
  writec(0x81);      Ra // select volume
  writec(20);        // vop
  writec(0xf8);      // x4
  writec(0x08);      // x4
    writec(0xb0);//set page address
          writec(0x10);//set column address
          writec(0x00);
          for(col=0;col<128;col++) {

               written(0x00);

          }
  writec(0xaf); //display on
}
void display(uchar dat1,uchar dat2) {

     uchar row,col;
```

```
    for (row=0xb0; row<0xb8; row++) {        //0XB0        0XB8

        writec(row);//set page address
        writec(0x10);//set column address
        writec(0x00);
        for(col=0;col<128;col++) {

            written(dat1);
            written(dat2);
        }
    }

    delay1(50000);

}

void displaychar(uchar *p) {

    uchar row,col;

    for (row=0xb0; row<0xb8; row++) {

        writec(row);//set page address
        writec(0x10);//set column address
        writec(0x00);
        for(col=0;col<128;col++)
        written(*p++);
    }

    delay1(50000);

}
void main(void)
{
    delay1(1000);
```

```
    vop=0x29;      //vop=9.1V
//vop=0x15;        //vop=7.1V
  init();
 while (1)
 {
        display(0xff,0xff);
        display(0x00,0x00);
        display(0x55,0xaa);
        display(0xaa,0x55);
        displaychar(chara1);
        displaychar(chara2);//vop_test();
 }
```