

- Design Consideration

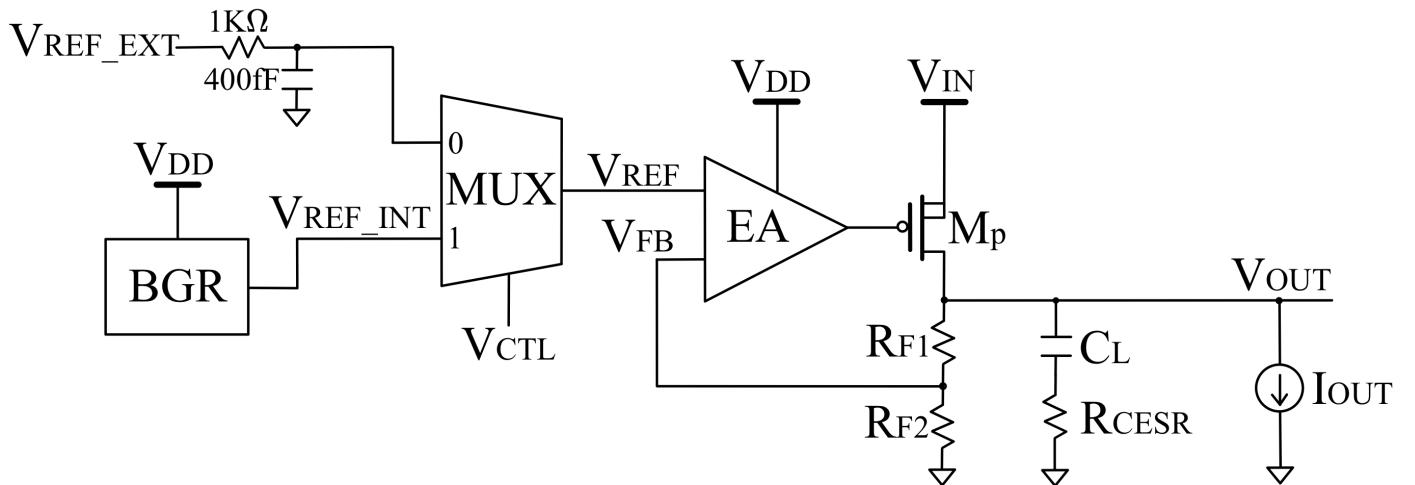
Initially, I needed to determine the size of Power MOS which could endure max current (200mA). In my opinion, I assumed the worst case that it's in region 1, according to triode current equation: $I_{in} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left[(V_{SG} - |V_{th}|)V_{SD} - \frac{1}{2}V_{SD}^2 \right]$ (set $L=0.18\mu m$ and $V_{th} = 484mV$ acquired by sweeping MOS I-V curve), so I could get width = 7.52mm. After adjusting my Phase Margin, I finally got my $\left(\frac{W}{L}\right)_p = \frac{100\mu}{0.18\mu}$, multiple = 55.

Besides, I could obtain R_{F1} and R_{F2} based on $V_{out} = 1.5V$ and $V_{FB} = 1.2V$. Therefore, I set my $R_{F1} \approx 30 k\Omega$ to avoid recovery time increasing $\rightarrow R_{F2} \approx 127 k\Omega$. When it comes to R_{CESR} , I gave it a variable and swept to get the best value of Phase Margin. Eventually, I got the value = $170m\Omega$.

To slightly reduce the circuit area, the RC compensation of EA was removed. Although this reduced the phase margin to approximately 40° , making the loop marginally stable, the issue can be mitigated by downsizing the power MOSFET to reduce excessive parasitic capacitance. This adjustment also increases the unity-gain bandwidth, which helps improve overshoot and undershoot performance.

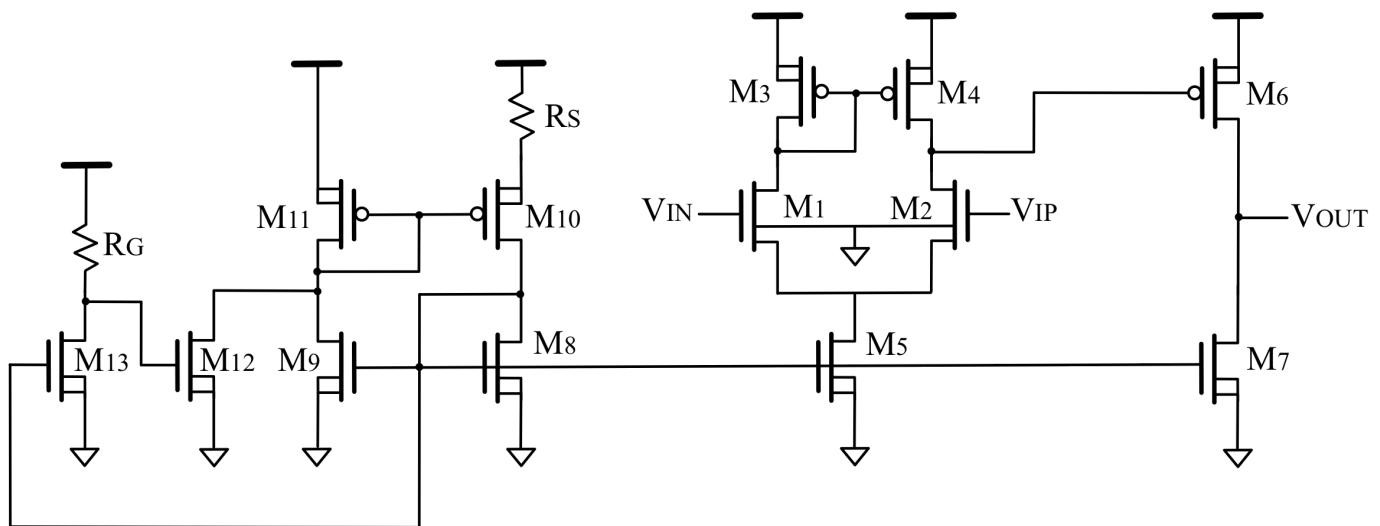
- Circuit Diagram

■ LDO



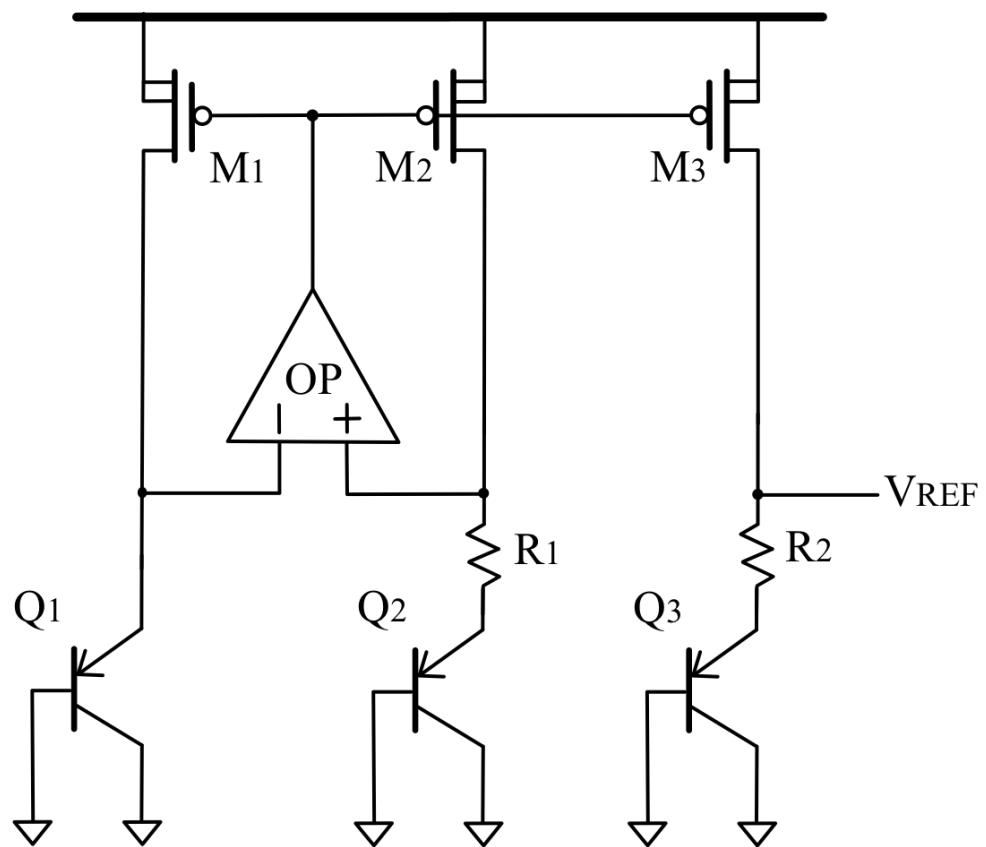
Device	Parameter	Device	Parameter
R_{F1}	$30.0327k\Omega$	R_{CESR}	$50m\Omega$
R_{F2}	$127.358k\Omega$	M_p	$100\mu/0.18\mu$ mul: 44
C_L	$4.7\mu F$	MUX	PMOS:2u/1u NMOS:1u/1u

EA



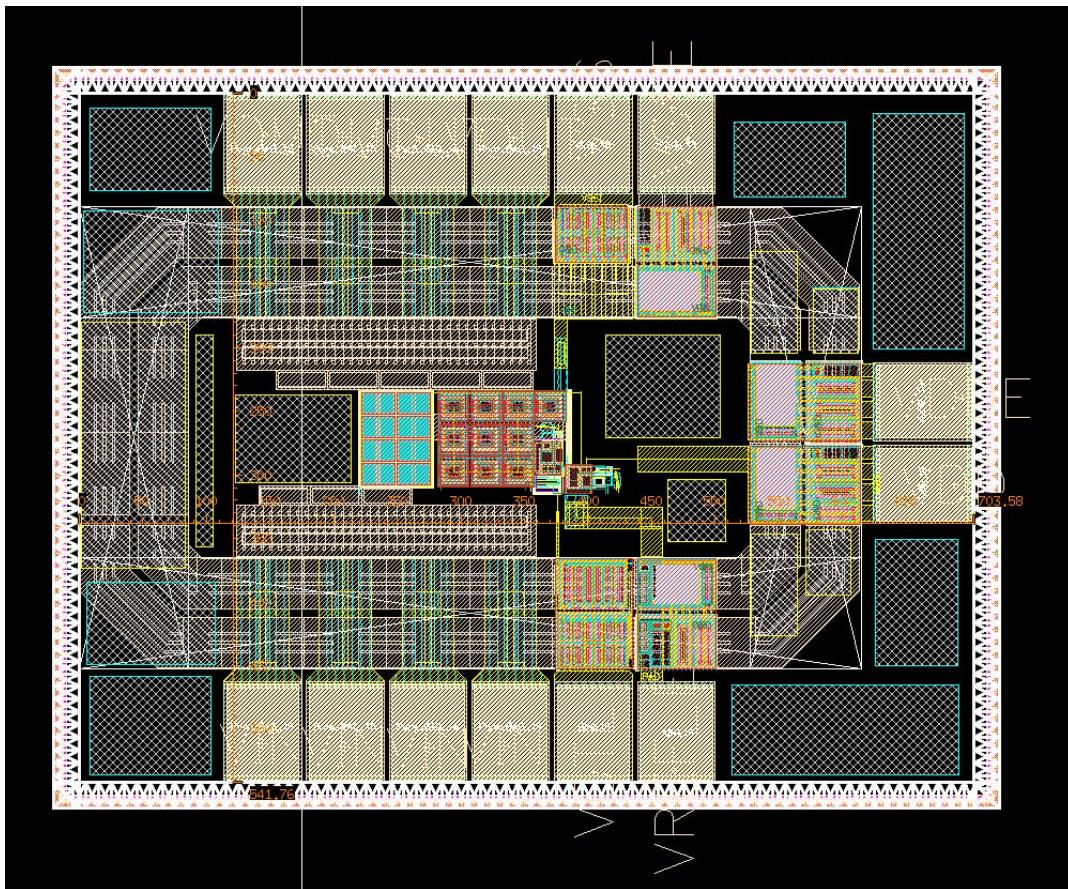
M_1	3u/1u	M_7	10u/0.5u	M_{13}	7u/1u
M_2	3u/1u	M_8	2u/1u	R_S	85.0235k Ω
M_3	4u/1u	M_9	2u/1u	R_G	93.5325k Ω
M_4	4u/1u	M_{10}	8u/1u		
M_5	4u/1u	M_{11}	2u/1u		
M_6	31.92u/0.5u	M_{12}	1u/1u		

BGR

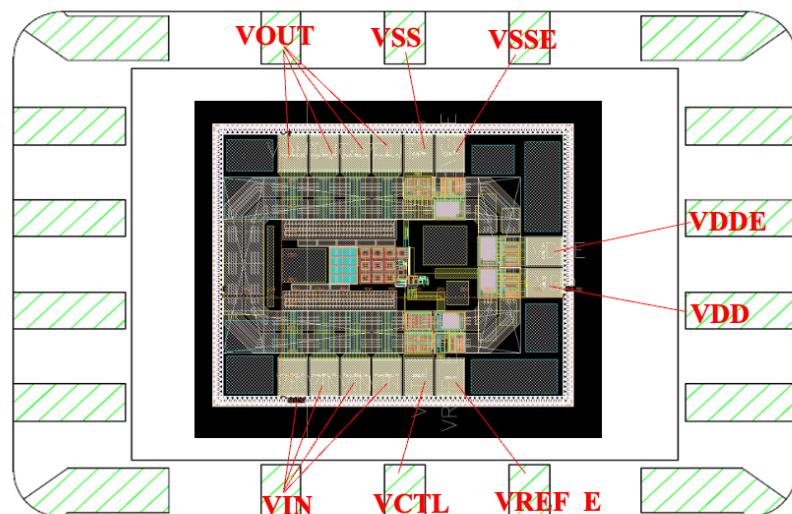


M_1	8u/1u
M_2	8u/1u
M_3	8u/1u
$Q_1: Q_2: Q_3$	1:8:1
R_1	20k
R_2	190k

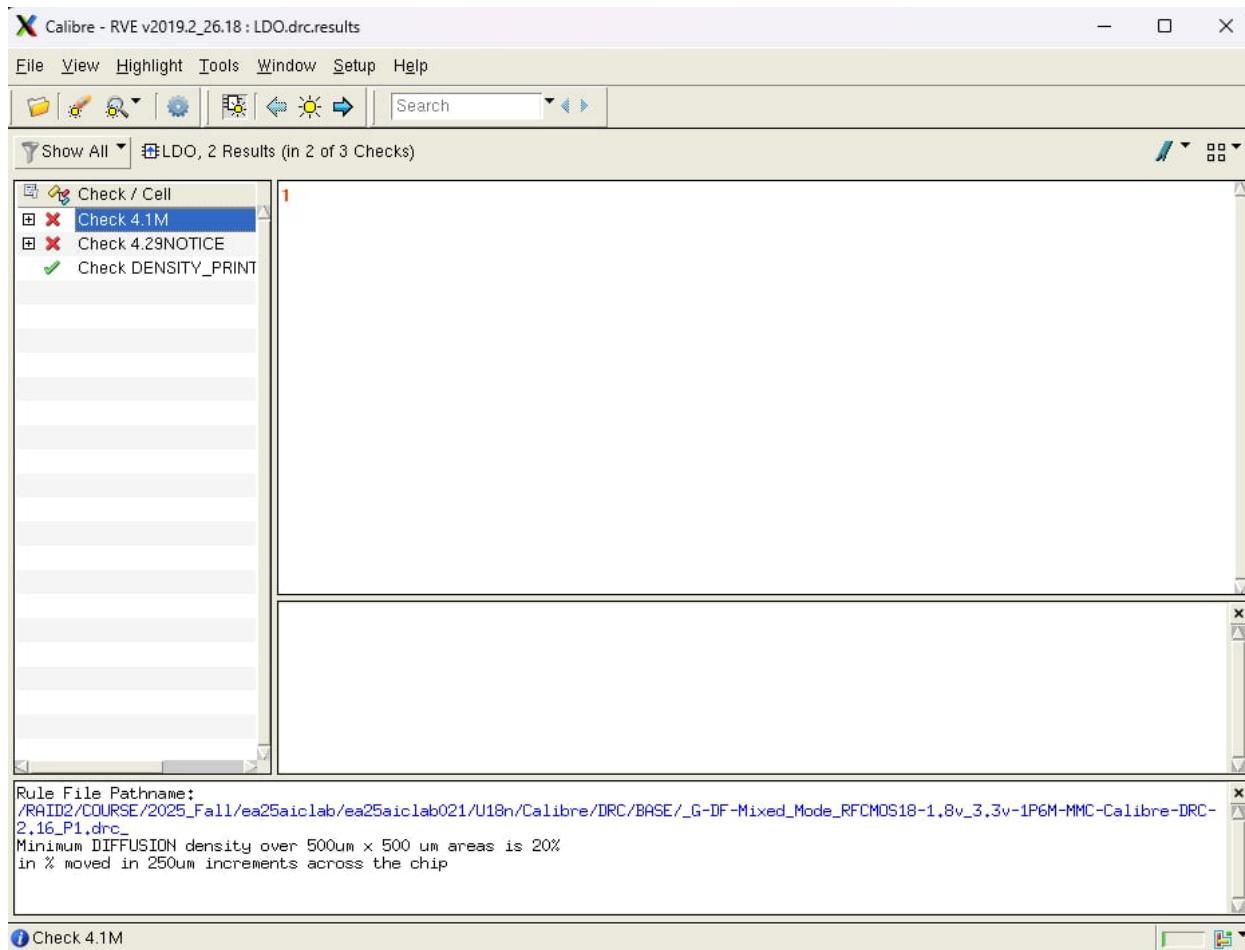
- Chip Layout and Bonding Diagram



$$\text{Area: } 703.58 \times 541.76 = 3.8117 \times 10^5 (\mu\text{m}^2)$$



- DRC Result



- LVS

