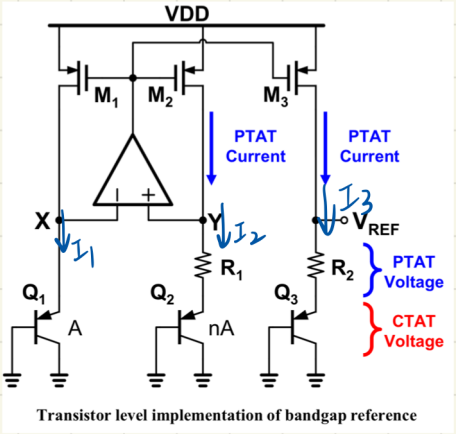
- Design consideration
  - Find the equation of V_{REF}



Transistor level implementation of bandgap reference

Assume $V_X = V_Y$,

$V_X = V_{EB1} = V_T \ln \frac{I_1}{I_S}$

$V_Y = V_{EB2} + I_2 \cdot R_1 = V_T \ln \frac{I_2}{nI_S} + I_2 \cdot R_1$

$\because M_1 = M_2 = M_3 \Rightarrow I_1 = I_2 = I_3$

$\Rightarrow V_T \ln \frac{I_1}{I_S} = V_T \ln \frac{I_2}{nI_S} + I_2 \cdot R_1 = V_T \ln \frac{I_1}{nI_S} + I_2 \cdot R_1$

$\Rightarrow V_T \ln n = I_2 R_1$

$\Rightarrow I_2 = \frac{V_T \ln n}{R_1} = I_3$

$V_{REF} = I_3 R_2 + V_{EB3} = \frac{R_2}{R_1} V_T \ln n + V_{EB3}$

  - How to determine the circuit parameter

The design process began by differentiating the previously derived expression for V_{REF}, which yielded the required resistor ratio $R_2/R_1 \approx 9.39$. To establish the PTAT–CTAT balance, I assumed equal branch currents $I_1 = I_2 = I_3 = 3\,\mu$A. Under this condition, the differential node voltage satisfies

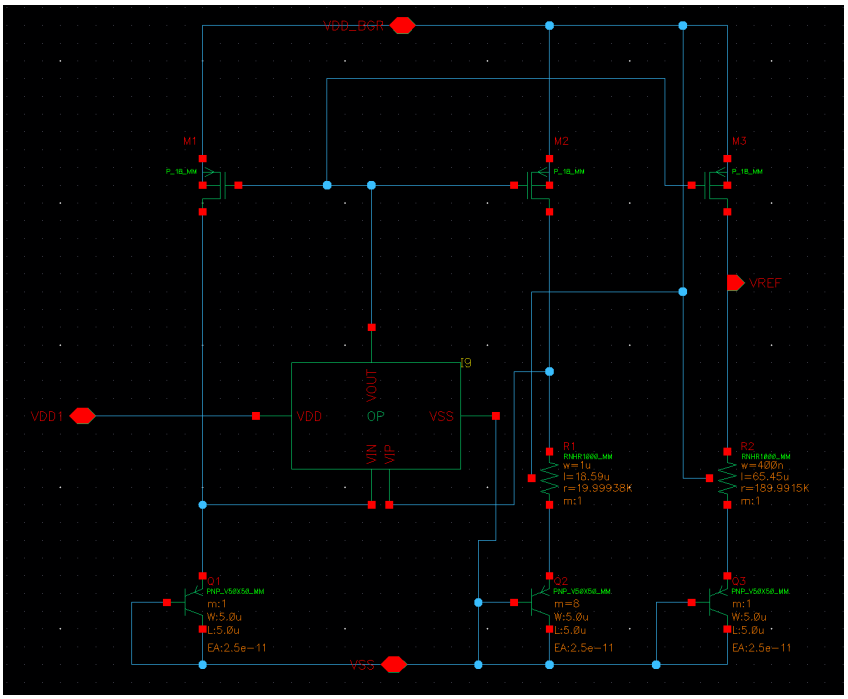
$$V_y - V_x = I_2 R_1 = V_T \ln(n).$$

To maintain perfect layout symmetry between Q_1 and Q_2, the emitter area ratio was chosen as $n = 8$. Substituting this value gives $R_1 \approx 20\text{k}\,\Omega$, and together with the required ratio, R_2 was initially set to approximately $170\text{k}\,\Omega$. For the MOS devices, I initially selected a channel length of $L = 1\,\mu$m to mitigate short-channel effects and used $W = 2\,\mu$m as the starting point. These parameters were then refined using simulation waveforms to achieve a stable V_{REF} under the TT corner.

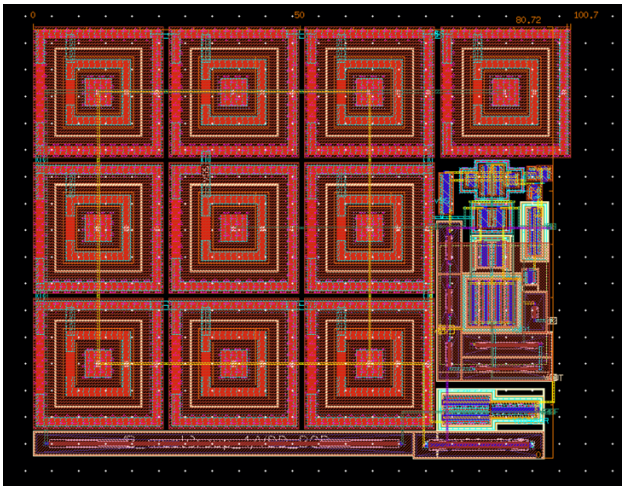
However, ensuring correct behavior across all process corners required additional modification of the operational amplifier. In FF and SS corners, the input differential pair and bias current sources tended to enter the triode region, degrading loop accuracy and generating large drifting V_{REF}. To address this, I resized the OP-amp devices to guarantee region2 operation for all MOS transistors across extreme temperatures and all corners.

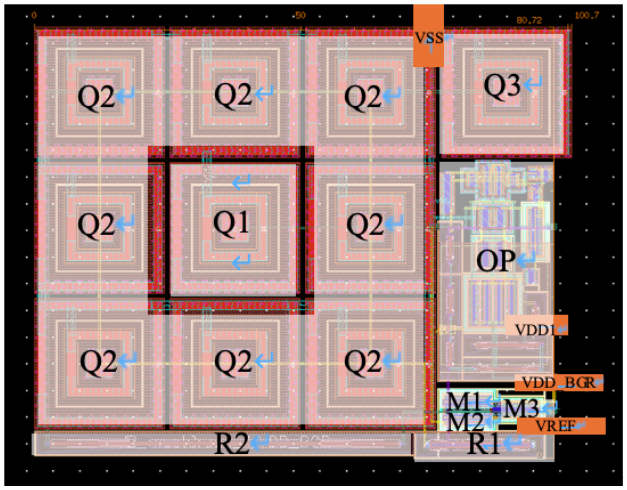
Finally, minor adjustments were applied to the bandgap resistors. Very short resistor lengths were found to cause significant drift under the FF corner, so I increased their lengths while maintaining the same resistance values. A final sweep on MOSFET widths was then performed to minimize the temperature coefficient and achieve the most stable overall bandgap behavior.

- Schematic



- Layout and Floorplan





Layout area = 80.72 * 100.7 ≈ **8128.5(um^2)**

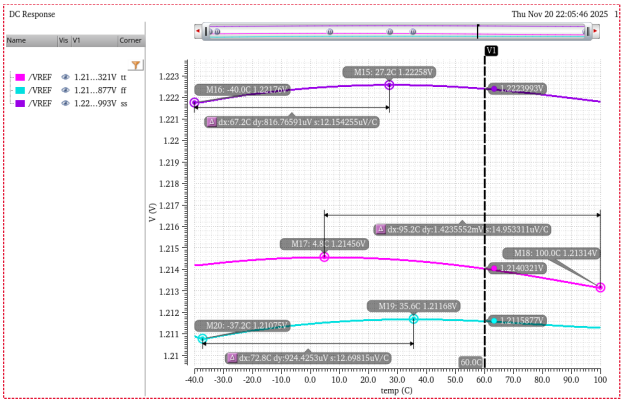
- Final Table
  - Pre-simulation

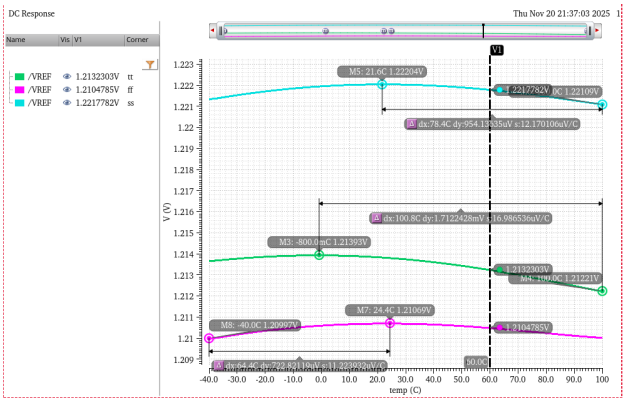
parameter	spec	Case 1	Case 2	Case 3	Case 4	Case 5
Corner		TT	FF	SS	TT	TT
Supply voltage		1.8	1.8	1.8	1.9	2.0
V_{REF} @ 60°C		**1.214V**	**1.212V**	**1.222V**	**1.215V**	**1.216V**
Static current(exclude OP)	<50uA	**9.34u**	**12.73u**	**7.34u**	**9.36u**	**9.36u**
Static current(OP)		**55.9u**	**90.08u**	**36.52u**	**61.38u**	**67.04u**
OP consumption(uW)		**100.62**	**162.14**	**65.74**	**116.62**	**134.08**
TC(ppm)	<15ppm/°C	**8.37**	**5.45**	**4.73**	**5.82**	**3.95**

  - Post-simulation

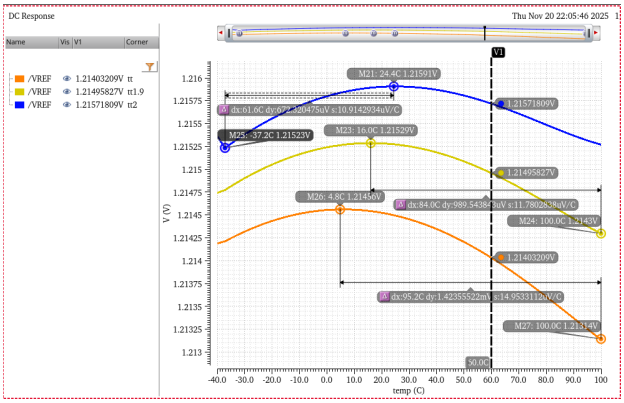
parameter	spec	Case 1	Case 2	Case 3	Case 4	Case 5
Corner		TT	FF	SS	TT	TT
Supply voltage		1.8	1.8	1.8	1.9	2.0
V_{REF} @ 60°C		**1.213V**	**1.21V**	**1.222V**	**1.214V**	**1.215V**
Static current(exclude OP)	<50uA	**9.32u**	**12.7u**	**7.33u**	**9.33u**	**9.33u**
Static current(OP)		**55.69u**	**89.59u**	**36.42u**	**61.15u**	**66.78u**
OP consumption(uW)		**100.24**	**161.26**	**65.56**	**116.19**	**133.56**
TC(ppm)	<15ppm/°C	**10.08**	**4.26**	**5.57**	**7.37**	**5.15**

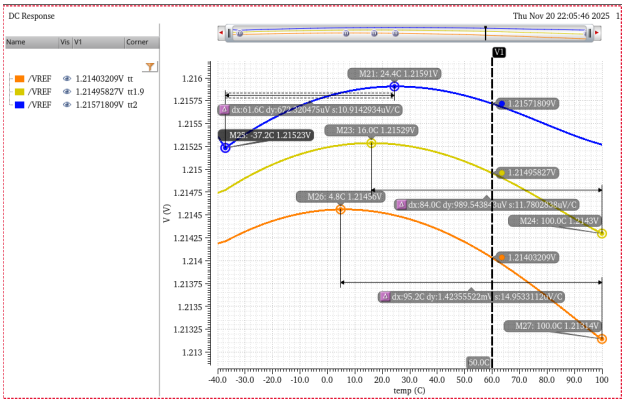
- Simulation waveform (left: pre-sim / right: post-sim)
  - Temperature ($-40°C \sim 100°C$) vs. V_{REF} @ TT, FF, and SS corners when $V_{DD} = 1.8V$





- Temperature ($-40°C \sim 100°C$) vs. V_{REF} @ TT corner when $V_{DD} = 1.8V, 1.9V, 2V$





- Time ($0 \sim 200$ ms) vs. V_{REF} @ TT corner when V_{DD} *is a ramp signal* ($1.8V \sim 2V$) with rising time 100 ms