

CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Acceso a Hardware

PINSEL0 to PINSEL9 Values	Function	Register	Controls
00	Primary (default) function, typically GPIO port	PINSEL0	P0[15:0]
01	First alternate function	PINSEL1	P0 [31:16]
10	Second alternate function	PINSEL2	P1 [15:0] (Ethernet)
11	Third alternate function	PINSEL3	P1 [31:16]
PINMODE_0D0 to PINMODE_0D4 Values	Function	PINSEL4	P2 [15:0]
0	Pin is in the normal (not open drain) mode.	PINSEL5	P2 [31:16] not used
1	Pin is in the open drain mode.	PINSEL6	P3 [15:0] not used
PINMODE0 to PINMODE9 Values	Function	PINSEL7	P3 [31:16]
00	Pin has an on-chip pull-up resistor enabled.	PINSEL8	P4 [15:0] not used
01	Repeater mode	PINSEL9	P4 [31:16]
10	Pin has neither pull-up nor pull-down resistor enabled.	PINSEL10	Trace port enable
11	Pin has an on-chip pull-down resistor enabled.		

- `void SetPINSEL(uint8_t puerto, uint8_t pin, uint8_t modo)`
- `void SetPINMODE(uint8_t port, uint8_t pin, uint8_t modo)`
- `void SetDIR(uint32_t* puerto, uint8_t pin, uint8_t dirección)`
- `void SetPIN(uint32_t* puerto, uint8_t pin, uint8_t estado)`
- `uint8_t GetPIN(uint8_t puerto, uint8_t pin, uint8_t actividad)`

Name	Description	Access	Reset Value ^[1]	Address
PINSEL0	Pin function select register 0.	R/W	0	0x4002 C000
PINSEL1	Pin function select register 1.	R/W	0	0x4002 C004
PINSEL2	Pin function select register 2.	R/W	0	0x4002 C008
PINSEL3	Pin function select register 3.	R/W	0	0x4002 C00C
PINSEL4	Pin function select register 4	R/W	0	0x4002 C010
PINSEL7	Pin function select register 7	R/W	0	0x4002 C01C
PINSEL8	Pin function select register 8	R/W	0	0x4002 C020
PINSEL9	Pin function select register 9	R/W	0	0x4002 C024
PINSEL10	Pin function select register 10	R/W	0	0x4002 C028
PINMODE0	Pin mode select register 0	R/W	0	0x4002 C040
PINMODE1	Pin mode select register 1	R/W	0	0x4002 C044
PINMODE2	Pin mode select register 2	R/W	0	0x4002 C048
PINMODE3	Pin mode select register 3.	R/W	0	0x4002 C04C
PINMODE4	Pin mode select register 4	R/W	0	0x4002 C050
PINMODE5	Pin mode select register 5	R/W	0	0x4002 C054
PINMODE6	Pin mode select register 6	R/W	0	0x4002 C058
PINMODE7	Pin mode select register 7	R/W	0	0x4002 C05C
PINMODE9	Pin mode select register 9	R/W	0	0x4002 C064
PINMODE_OD0	Open drain mode control register 0	R/W	0	0x4002 C068
PINMODE_OD1	Open drain mode control register 1	R/W	0	0x4002 C06C
PINMODE_OD2	Open drain mode control register 2	R/W	0	0x4002 C070
PINMODE_OD3	Open drain mode control register 3	R/W	0	0x4002 C074
PINMODE_OD4	Open drain mode control register 4	R/W	0	0x4002 C078
I2CPADCFG	I ² C Pin Configuration register	R/W	0	0x4002 C07C

Mapa de las G PIO del LPC1769

Table 101. GPIO register map (local bus accessible registers - enhanced GPIO features)				
Generic Name	Description	Access	Reset value ^[1]	PORTn Register Name & Address
FIODIR	Fast GPIO Port Direction control register. This register individually controls the direction of each port pin.	R/W	0	FIO0DIR - 0x2009 C000 FIO1DIR - 0x2009 C020 FIO2DIR - 0x2009 C040 FIO3DIR - 0x2009 C060 FIO4DIR - 0x2009 C080
FIOMASK	Fast Mask register for port. Writes, sets, clears, and reads to port (done via writes to FIOPIN, FIOSET, and FIOCLR, and reads of FIOPIN) alter or return only the bits enabled by zeros in this register.	R/W	0	FIO0MASK - 0x2009 C010 FIO1MASK - 0x2009 C030 FIO2MASK - 0x2009 C050 FIO3MASK - 0x2009 C070 FIO4MASK - 0x2009 C090
FIOPIN	Fast Port Pin value register using FIOMASK. The current state of digital port pins can be read from this register, regardless of pin direction or alternate function selection (as long as pins are not configured as an input to ADC). The value read is masked by ANDing with inverted FIOMASK. Writing to this register places corresponding values in all bits enabled by zeros in FIOMASK. Important: if an FIOPIN register is read, its bit(s) masked with 1 in the FIOMASK register will be read as 0 regardless of the physical pin state.	R/W	0	FIO0PIN - 0x2009 C014 FIO1PIN - 0x2009 C034 FIO2PIN - 0x2009 C054 FIO3PIN - 0x2009 C074 FIO4PIN - 0x2009 C094
FIOSET	Fast Port Output Set register using FIOMASK. This register controls the state of output pins. Writing 1s produces highs at the corresponding port pins. Writing 0s has no effect. Reading this register returns the current contents of the port output register. Only bits enabled by 0 in FIOMASK can be altered.	R/W	0	FIO0SET - 0x2009 C018 FIO1SET - 0x2009 C038 FIO2SET - 0x2009 C058 FIO3SET - 0x2009 C078 FIO4SET - 0x2009 C098
FIOCLR	Fast Port Output Clear register using FIOMASK. This register controls the state of output pins. Writing 1s produce lows at the corresponding port pins. Writing 0s has no effect. Only bits enabled by 0 in FIOMASK can be altered.	WO	0	FIO0CLR - 0x2009 C01C FIO1CLR - 0x2009 C03C FIO2CLR - 0x2009 C05C FIO3CLR - 0x2009 C07C FIO4CLR - 0x2009 C09C

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

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Registros PINSEL

Table 79. Pin function select register 0 (PINSEL0 - address 0x4002 C000) bit description

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.0	GPIO Port 0.0	RD1	TXD3	SDA1	00
3:2	P0.1	GPIO Port 0.1	TD1	RXD3	SCL1	00
5:4	P0.2	GPIO Port 0.2	TXD0	AD0.7	Reserved	00
7:6	P0.3	GPIO Port 0.3	RXD0	AD0.6	Reserved	00
9:8	P0.4 ^[1]	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5 ^[1]	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00
29:24	-	Reserved	Reserved	Reserved	Reserved	0
31:30	P0.15	GPIO Port 0.15	TXD1	SCK0	SCK	00

Table 80. Pin function select register 1 (PINSEL1 - address 0x4002 C004) bit description

PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.16	GPIO Port 0.16	RXD1	SSEL0	SSEL	00
3:2	P0.17	GPIO Port 0.17	CTS1	MISO0	MISO	00
5:4	P0.18	GPIO Port 0.18	DCD1	MOSI0	MOSI	00
7:6	P0.19 ^[1]	GPIO Port 0.19	DSR1	Reserved	SDA1	00
9:8	P0.20 ^[1]	GPIO Port 0.20	DTR1	Reserved	SCL1	00
11:10	P0.21 ^[1]	GPIO Port 0.21	RI1	Reserved	RD1	00
13:12	P0.22	GPIO Port 0.22	RTS1	Reserved	TD1	00
15:14	P0.23 ^[1]	GPIO Port 0.23	AD0.0	I2SRX_CLK	CAP3.0	00
17:16	P0.24 ^[1]	GPIO Port 0.24	AD0.1	I2SRX_WS	CAP3.1	00
19:18	P0.25	GPIO Port 0.25	AD0.2	I2SRX_SDA	TXD3	00
21:20	P0.26	GPIO Port 0.26	AD0.3	AOUT	RXD3	00
23:22	P0.27 ^{[1][2]}	GPIO Port 0.27	SDA0	USB_SDA	Reserved	00
25:24	P0.28 ^{[1][2]}	GPIO Port 0.28	SCL0	USB_SCL	Reserved	00
27:26	P0.29	GPIO Port 0.29	USB_D+	Reserved	Reserved	00
29:28	P0.30	GPIO Port 0.30	USB_D-	Reserved	Reserved	00
31:30	-	Reserved	Reserved	Reserved	Reserved	00

Table 81. Pin function select register 2 (PINSEL2 - address 0x4002 C008) bit description

PINSEL2	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.0	GPIO Port 1.0	ENET_TXD0	Reserved	Reserved	00
3:2	P1.1	GPIO Port 1.1	ENET_TXD1	Reserved	Reserved	00
7:4	-	Reserved	Reserved	Reserved	Reserved	0
9:8	P1.4	GPIO Port 1.4	ENET_TX_EN	Reserved	Reserved	00
15:10	-	Reserved	Reserved	Reserved	Reserved	0
17:16	P1.8	GPIO Port 1.8	ENET_CRS	Reserved	Reserved	00
19:18	P1.9	GPIO Port 1.9	ENET_RXD0	Reserved	Reserved	00
21:20	P1.10	GPIO Port 1.10	ENET_RXD1	Reserved	Reserved	00
27:22	-	Reserved	Reserved	Reserved	Reserved	0
29:28	P1.14	GPIO Port 1.14	ENET_RX_ER	Reserved	Reserved	00
31:30	P1.15	GPIO Port 1.15	ENET_REF_CLK	Reserved	Reserved	00

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Table 82. Pin function select register 3 (PINSEL3 - address 0x4002 C00C) bit description

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.16 ^[1]	GPIO Port 1.16	ENET_MDC	Reserved	Reserved	00
3:2	P1.17 ^[1]	GPIO Port 1.17	ENET_MDIO	Reserved	Reserved	00
5:4	P1.18	GPIO Port 1.18	USB_UP_LED	PWM1.1	CAP1.0	00
7:6	P1.19	GPIO Port 1.19	MCOA0	USB_PPWR	CAP1.1	00
9:8	P1.20	GPIO Port 1.20	MCI0	PWM1.2	SCK0	00
11:10	P1.21 ^[1]	GPIO Port 1.21	MCABORT	PWM1.3	SSEL0	00
13:12	P1.22	GPIO Port 1.22	MCOB0	USB_PWRD	MAT1.0	00
15:14	P1.23	GPIO Port 1.23	MCI1	PWM1.4	MISO0	00
17:16	P1.24	GPIO Port 1.24	MCI2	PWM1.5	MOSI0	00
19:18	P1.25	GPIO Port 1.25	MCOA1	Reserved	MAT1.1	00
21:20	P1.26	GPIO Port 1.26	MCOB1	PWM1.6	CAP0.0	00
23:22	P1.27 ^[1]	GPIO Port 1.27	CLKOUT	USB_OVRCR	CAP0.1	00
25:24	P1.28	GPIO Port 1.28	MCOA2	PCAP1.0	MAT0.0	00
27:26	P1.29	GPIO Port 1.29	MCOB2	PCAP1.1	MAT0.1	00
29:28	P1.30	GPIO Port 1.30	Reserved	V _{BUS}	AD0.4	00
31:30	P1.31	GPIO Port 1.31	Reserved	SCK1	AD0.5	00

Table 83. Pin function select register 4 (PINSEL4 - address 0x4002 C010) bit description

PINSEL4	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P2.0	GPIO Port 2.0	PWM1.1	TXD1	Reserved	00
3:2	P2.1	GPIO Port 2.1	PWM1.2	RXD1	Reserved	00
5:4	P2.2	GPIO Port 2.2	PWM1.3	CTS1	Reserved ^[2]	00
7:6	P2.3	GPIO Port 2.3	PWM1.4	DCD1	Reserved ^[2]	00
9:8	P2.4	GPIO Port 2.4	PWM1.5	DSR1	Reserved ^[2]	00
11:10	P2.5	GPIO Port 2.5	PWM1.6	DTR1	Reserved ^[2]	00
13:12	P2.6	GPIO Port 2.6	PCAP1.0	RI1	Reserved ^[2]	00
15:14	P2.7	GPIO Port 2.7	RD2	RTS1	Reserved	00
17:16	P2.8	GPIO Port 2.8	TD2	TXD2	ENET_MDC	00
19:18	P2.9	GPIO Port 2.9	USB_CONNECT	RXD2	ENET_MDIO	00
21:20	P2.10	GPIO Port 2.10	EINT0	NMI	Reserved	00
23:22	P2.11 ^[1]	GPIO Port 2.11	EINT1	Reserved	I2STX_CLK	00
25:24	P2.12 ^[1]	GPIO Port 2.12	EINT2	Reserved	I2STX_WS	00
27:26	P2.13 ^[1]	GPIO Port 2.13	EINT3	Reserved	I2STX_SDA	00
31:28	-	Reserved	Reserved	Reserved	Reserved	0

Table 84. Pin function select register 7 (PINSEL7 - address 0x4002 C01C) bit description

PINSEL7	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
17:0	-	Reserved	Reserved	Reserved	Reserved	0
19:18	P3.25 ^[1]	GPIO Port 3.25	Reserved	MAT0.0	PWM1.2	00
21:20	P3.26 ^[1]	GPIO Port 3.26	STCLK	MAT0.1	PWM1.3	00

Table 85. Pin function select register 9 (PINSEL9 - address 0x4002 C024) bit description

PINSEL9	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
23:0	-	Reserved	Reserved	Reserved	Reserved	00
25:24	P4.28	GPIO Port 4.28	RX_MCLK	MAT2.0	TXD3	00
27:26	P4.29	GPIO Port 4.29	TX_MCLK	MAT2.1	RXD3	00

Interrupciones: NVIC

Table 51. NVIC register map

Name	Description	Access	Reset value	Address
ISER0 to ISER1	Interrupt Set-Enable Registers. These 2 registers allow enabling interrupts and reading back the interrupt enables for specific peripheral functions.	RW	0	ISER0 - 0xE000 E100 ISER1 - 0xE000 E104
ICER0 to ICER1	Interrupt Clear-Enable Registers. These 2 registers allow disabling interrupts and reading back the interrupt enables for specific peripheral functions.	RW	0	ICER0 - 0xE000 E180 ICER1 - 0xE000 E184
ISPR0 to ISPR1	Interrupt Set-Pending Registers. These 2 registers allow changing the interrupt state to pending and reading back the interrupt pending state for specific peripheral functions.	RW	0	ISPR0 - 0xE000 E200 ISPR1 - 0xE000 E204
ICPR0 to ICPR1	Interrupt Clear-Pending Registers. These 2 registers allow changing the interrupt state to not pending and reading back the interrupt pending state for specific peripheral functions.	RW	0	ICPR0 - 0xE000 E280 ICPR1 - 0xE000 E284
IABR0 to IABR1	Interrupt Active Bit Registers. These 2 registers allow reading the current interrupt active state for specific peripheral functions.	RO	0	IABR0 - 0xE000 E300 IABR1 - 0xE000 E304

Table 52. Interrupt Set-Enable Register 0 register (ISER0 - 0xE000 E100)

Bit	Name	Function
0	ISE_WDT	Watchdog Timer Interrupt Enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.
1	ISE_TIMER0	Timer 0 interrupt Enable. See functional description for bit 0.
2	ISE_TIMER1	Timer 1. interrupt Enable. See functional description for bit 0.
3	ISE_TIMER2	Timer 2 interrupt Enable. See functional description for bit 0.
4	ISE_TIMER3	Timer 3 interrupt Enable. See functional description for bit 0.
5	ISE_UART0	UART0 interrupt Enable. See functional description for bit 0.
6	ISE_UART1	UART1 interrupt Enable. See functional description for bit 0.
7	ISE_UART2	UART2 interrupt Enable. See functional description for bit 0.
8	ISE_UART3	UART3 interrupt Enable. See functional description for bit 0.
9	ISE_PWM	PWM1 interrupt Enable. See functional description for bit 0.
10	ISE_I2C0	I ² C0 interrupt Enable. See functional description for bit 0.
11	ISE_I2C1	I ² C1 interrupt Enable. See functional description for bit 0.
12	ISE_I2C2	I ² C2 interrupt Enable. See functional description for bit 0.
13	ISE_SPI	SPI interrupt Enable. See functional description for bit 0.
14	ISE_SSP0	SSP0 interrupt Enable. See functional description for bit 0.
15	ISE_SSP1	SSP1 interrupt Enable. See functional description for bit 0.
16	ISE_PLL0	PLL0 (Main PLL) interrupt Enable. See functional description for bit 0.
17	ISE_RTC	Real Time Clock (RTC) interrupt Enable. See functional description for bit 0.
18	ISE_EINT0	External Interrupt 0 interrupt Enable. See functional description for bit 0.
19	ISE_EINT1	External Interrupt 1 interrupt Enable. See functional description for bit 0.
20	ISE_EINT2	External Interrupt 2 interrupt Enable. See functional description for bit 0.
21	ISE_EINT3	External Interrupt 3 interrupt Enable. See functional description for bit 0.
22	ISE_ADC	ADC interrupt Enable. See functional description for bit 0.
23	ISE_BOD	BOD interrupt Enable. See functional description for bit 0.
24	ISE_USB	USB interrupt Enable. See functional description for bit 0.
25	ISE_CAN	CAN interrupt Enable. See functional description for bit 0.
26	ISE_DMA	GPDMA interrupt Enable. See functional description for bit 0.
27	ISE_I2S	I ² S interrupt Enable. See functional description for bit 0.
28	ISE_ENET	Ethernet interrupt Enable. See functional description for bit 0.
29	ISE_RIT	Repetitive Interrupt Timer interrupt Enable. See functional description for bit 0.
30	ISE_MCPWM	Motor Control PWM interrupt Enable. See functional description for bit 0.
31	ISE_QEI	Quadrature Encoder Interface interrupt Enable. See functional description for bit 0.

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void ResetISR(void);
WEAK void NMI_Handler(void);
WEAK void HardFault_Handler(void);
WEAK void MemManage_Handler(void);
WEAK void BusFault_Handler(void);
WEAK void UsageFault_Handler(void);
WEAK void SVCall_Handler(void);
WEAK void DebugMon_Handler(void);
WEAK void PendSV_Handler(void);
WEAK void SysTick_Handler(void);
WEAK void IntDefaultHandler(void);

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void TIMER0_IRQHandler(void) ALIAS(IntDefaultHandler);
void TIMER1_IRQHandler(void) ALIAS(IntDefaultHandler);
void TIMER2_IRQHandler(void) ALIAS(IntDefaultHandler);
void TIMER3_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART0_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART1_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART2_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART3_IRQHandler(void) ALIAS(IntDefaultHandler);
void PWM1_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2C0_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2C1_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2C2_IRQHandler(void) ALIAS(IntDefaultHandler);
void SPI_IRQHandler(void) ALIAS(IntDefaultHandler);
void SSP0_IRQHandler(void) ALIAS(IntDefaultHandler);
void SSP1_IRQHandler(void) ALIAS(IntDefaultHandler);
void PLL0_IRQHandler(void) ALIAS(IntDefaultHandler);
void RTC_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT0_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT1_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT2_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT3_IRQHandler(void) ALIAS(IntDefaultHandler);
void ADC_IRQHandler(void) ALIAS(IntDefaultHandler);
void BOD_IRQHandler(void) ALIAS(IntDefaultHandler);
void USB_IRQHandler(void) ALIAS(IntDefaultHandler);
void CAN_IRQHandler(void) ALIAS(IntDefaultHandler);
void DMA_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2S_IRQHandler(void) ALIAS(IntDefaultHandler);
void ENET_IRQHandler(void) ALIAS(IntDefaultHandler);
void RIT_IRQHandler(void) ALIAS(IntDefaultHandler);
void MCPWM_IRQHandler(void) ALIAS(IntDefaultHandler);
void QEI_IRQHandler(void) ALIAS(IntDefaultHandler);
void PLL1_IRQHandler(void) ALIAS(IntDefaultHandler);
void USARTActivity_IRQHandler(void) ALIAS(IntDefaultHand

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Interrupciones. Externas

Table 9. External Interrupt registers

Name	Description	Access	Reset value ^[1]
EXTINT	The External Interrupt Flag Register contains interrupt flags for EINT0, EINT1, EINT2 and EINT3. See Table 10 .	R/W	0x00
EXTMODE	The External Interrupt Mode Register controls whether each pin is edge- or level-sensitive. See Table 11 .	R/W	0x00
EXTPOLAR	The External Interrupt Polarity Register controls which level or edge on each pin will cause an interrupt. See Table 12 .	R/W	0x00

Table 11. External Interrupt Mode register (EXTMODE - address description)

Bit	Symbol	Value	Description
0	EXTMODE0	0	Level-sensitivity is selected for EINT0.
		1	EINT0 is edge sensitive.
1	EXTMODE1	0	Level-sensitivity is selected for EINT1.
		1	EINT1 is edge sensitive.
2	EXTMODE2	0	Level-sensitivity is selected for EINT2.
		1	EINT2 is edge sensitive.
3	EXTMODE3	0	Level-sensitivity is selected for EINT3.
		1	EINT3 is edge sensitive.
31:4	-	-	Reserved, user software should not write bits. The value read from a reserved bit is

Table 10. External Interrupt Flag register (EXTINT - address 0x400F C140) bit description

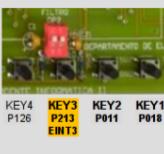
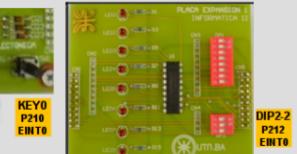
Bit	Symbol	Description	Reset value
0	EINT0	In level-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state. ^[1]	0
1	EINT1	In level-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state. ^[1]	0
2	EINT2	In level-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state. ^[1]	0
3	EINT3	In level-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state. ^[1]	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 12. External Interrupt Polarity register (EXTPOLAR - address 0x400F C14C) bit description

Bit	Symbol	Value	Description	Reset value
0	EXTPOLAR0	0	EINT0 is low-active or falling-edge sensitive (depending on EXTMODE0).	0
		1	EINT0 is high-active or rising-edge sensitive (depending on EXTMODE0).	
1	EXTPOLAR1	0	EINT1 is low-active or falling-edge sensitive (depending on EXTMODE1).	0
		1	EINT1 is high-active or rising-edge sensitive (depending on EXTMODE1).	
2	EXTPOLAR2	0	EINT2 is low-active or falling-edge sensitive (depending on EXTMODE2).	0
		1	EINT2 is high-active or rising-edge sensitive (depending on EXTMODE2).	
3	EXTPOLAR3	0	EINT3 is low-active or falling-edge sensitive (depending on EXTMODE3).	0
		1	EINT3 is high-active or rising-edge sensitive (depending on EXTMODE3).	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA



Interrupciones Externas en Infotronic Implementación

Interrupción EXTERNA	Puerto	Infotronic	Función
EINT0	P210	SW1	KEY0
EINT1	P211	ENT.DIG2	BORNERA
EINT2	P212	EXPANSION17	DIP2_2
EINT3	P213	SW4	KEY3
  			
KEY4 P126 KEY3 P213 EINT3 KEY2 P011 KEY1 P018 KEY0 P210 EINT0 DIP2-2 P212 EINT0			

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Systick

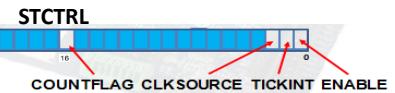
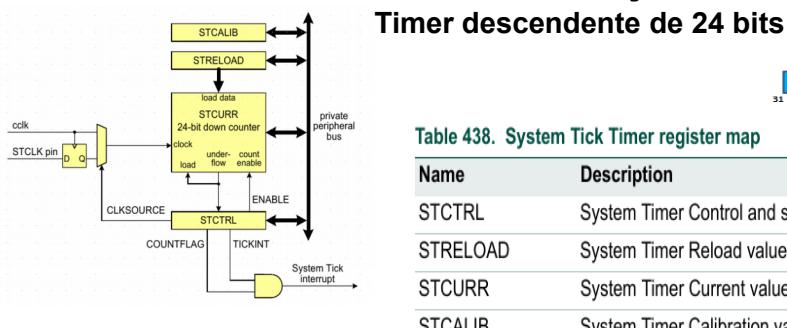


Table 438. System Tick Timer register map

Name	Description	Access	Reset value ^[1]	Address
STCTRL	System Timer Control and status register	R/W	0x4	0xE000 E010
STRELOAD	System Timer Reload value register	R/W	0	0xE000 E014
STCURRE	System Timer Current value register	R/W	0	0xE000 E018
STCALIB	System Timer Calibration value register	R/W	0x000F 423F	0xE000 E01C

Clock por defecto: Interno (CCLK)

Si se elige clock externo: STCLK (P3.26) => Seleccionar al pin STCLK en el registro pinMode

STRELOAD = (STCALIB / N) - 1 ➔ Si N=1 ➔ tick cada 10ms. (si clock=100MHz)

Power Control for Peripherals

Table 46. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

Bit	Symbol	Description	Reset value
0	-	Reserved.	NA
1	PCTIMO	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	-	Reserved.	NA
6	PCPWM1	PWM1 power/clock control bit.	1
7	PCI2C0	The I ² C0 interface power/clock control bit.	1
8	PCSPI	The SPI interface power/clock control bit.	1
9	PCRTC	The RTC power/clock control bit.	1
10	PCSSP1	The SSP 1 interface power/clock control bit.	1
11	-	Reserved.	NA
12	PCADC	A/D converter (ADC) power/clock control bit.	0
Note: Clear the PDN bit in the ADDCR before clearing this bit, and set this bit before setting PDN.			
13	PCCAN1	CAN Controller 1 power/clock control bit.	0
14	PCCAN2	CAN Controller 2 power/clock control bit.	0
15	PCGPIO	Power/clock control bit for IOCON, GPIO, and GPIO interrupts.	1
16	PCRIT	Repetitive Interrupt Timer power/clock control bit.	0

Table 46. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

Bit	Symbol	Description	Reset value
17	PCMPCPWM	Motor Control PWM	0
18	PCQEI	Quadrature Encoder Interface power/clock control bit.	0
19	PCI2C1	The I ² C1 interface power/clock control bit.	1
20	-	Reserved.	NA
21	PCSSP0	The SSP0 interface power/clock control bit.	1
22	PCTIM2	Timer 2 power/clock control bit.	0
23	PCTIM3	Timer 3 power/clock control bit.	0
24	PCUART2	UART 2 power/clock control bit.	0
25	PCUART3	UART 3 power/clock control bit.	0
26	PCI2C2	I ² C interface 2 power/clock control bit.	1
27	PCI2S	I ² S interface power/clock control bit.	0
28	-	Reserved.	NA
29	PCGPDMA	GPDMA function power/clock control bit.	0
30	PCENET	Ethernet block power/clock control bit.	0
31	PCUSB	USB interface power/clock control bit.	0

Peripheral Clock Selection Register

Table 40. Peripheral Clock Selection register 0 (PCLKSEL0) bit description

Bit	Symbol	Description	bit	Reset value
1:0	PCLK_WDT	Peripheral clock selection for WDT.	00	
3:2	PCLK_TIMER0	Peripheral clock selection for TIMER0.	00	
5:4	PCLK_TIMER1	Peripheral clock selection for TIMER1.	00	
7:6	PCLK_UART0	Peripheral clock selection for UART0.	00	
9:8	PCLK_UART1	Peripheral clock selection for UART1.	00	
11:10	-	Reserved.	NA	
13:12	PCLK_PWM1	Peripheral clock selection for PWM1.	00	
15:14	PCLK_I2C0	Peripheral clock selection for I ² C0.	00	
17:16	PCLK_SPI	Peripheral clock selection for SPI.	00	
19:18	-	Reserved.	NA	
21:20	PCLK_SSP1	Peripheral clock selection for SSP1.	00	
23:22	PCLK_DAC	Peripheral clock selection for DAC.	00	
25:24	PCLK_ADC	Peripheral clock selection for ADC.	00	

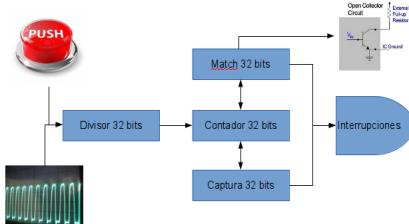
PCLKSEL0

Table 42. Peripheral Clock Selection register bit values

PCLKSEL0 and PCLKSEL1 Function	individual peripheral's clock select options	Reset value
00	PCLK_peripheral = CCLK/4	00
01	PCLK_peripheral = CCLK	
10	PCLK_peripheral = CCLK/2	
11	PCLK_peripheral = CCLK/8, except for CAN1, CAN2, and CAN filtering when '11' selects = CCLK/6.	

CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Timers



- 2 canales de captura, que sacan una foto del timer ante una transición de una entrada. Puede generar, en forma opcional, una interrupción.
- Cuatro registros de match de 32-bit que permiten:
 - Operación continua con generación opcional de interrupción on match.
 - Frena timer on match con interrupción opcional.
 - Reset timer on match interrupción opcional.
- Hasta cuatro salidas externas correspondientes a los registros de match con las siguientes capacidades:
 - Set low on match.
 - Set high on match.
 - Toggle on match.
 - No hace nada on match

Mapa de Registros

//resumen\\

Table 425. TIMER/COUNTER0-3 register map

Generic Name	Description	Access	Reset Value	TIMERn Register/Name & Address
IR	Interrupt Register. The IR can be written to clear interrupts. The IR can be read to identify which of eight possible interrupt sources are pending.	R/W	0	T0IR - 0x4000 4000 T1IR - 0x4000 8000 T2IR - 0x4009 0000 T3IR - 0x4009 4000
TCR	Timer Control Register. The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	R/W	0	T0TCR - 0x4000 4004 T1TCR - 0x4000 8004 T2TCR - 0x4009 0004 T3TCR - 0x4009 4004
TC	Timer Counter. The 32-bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	R/W	0	T0TC - 0x4000 4008 T1TC - 0x4000 8008 T2TC - 0x4009 0008 T3TC - 0x4009 4008
MCR	Match Control Register. The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	R/W	0	T0MCR - 0x4000 4014 T1MCR - 0x4000 8014 T2MCR - 0x4009 0014 T3MCR - 0x4009 4014
MR0	Match Register 0. MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	R/W	0	T0MR0 - 0x4000 4018 T1MR0 - 0x4000 8018 T2MR0 - 0x4009 0018 T3MR0 - 0x4009 4018
MR1	Match Register 1. See MR0 description.	R/W	0	T0MR1 - 0x4000 401C T1MR1 - 0x4000 801C T2MR1 - 0x4009 001C T3MR1 - 0x4009 401C
MR2	Match Register 2. See MR0 description.	R/W	0	T0MR2 - 0x4000 4020 T1MR2 - 0x4000 8020 T2MR2 - 0x4009 0020 T3MR2 - 0x4009 4020
MR3	Match Register 3. See MR0 description.	R/W	0	T0MR3 - 0x4000 4024 T1MR3 - 0x4000 8024 T2MR3 - 0x4009 0024 T3MR3 - 0x4009 4024
CCR	Capture Control Register. The CCR controls which edges of the capture inputs are used to load the Capture Registers and whether or not an interrupt is generated when a capture takes place.	R/W	0	T0CCR - 0x4000 4028 T1CCR - 0x4000 8028 T2CCR - 0x4009 0028 T3CCR - 0x4009 4028
EMR	External Match Register. The EMR controls the external match pins MATn.0-3 (MAT0.0-3 and MAT1.0-3 respectively).	R/W	0	T0EMR - 0x4000 403C T1EMR - 0x4000 803C T2EMR - 0x4009 003C T3EMR - 0x4009 403C
CTCR	Count Control Register. The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	R/W	0	T0CTCR - 0x4000 4070 T1CTCR - 0x4000 8070 T2CTCR - 0x4009 0070 T3CTCR - 0x4009 4070

No contigüo

No contigüo

No contigüo

CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Bit	Symbol	Description
0	MRO Interrupt	Interrupt flag for match channel 0.
1	MR1 Interrupt	Interrupt flag for match channel 1.
2	MR2 Interrupt	Interrupt flag for match channel 2.
3	MR3 Interrupt	Interrupt flag for match channel 3.
4	CR0 Interrupt	Interrupt flag for capture channel 0 event.
5	CR1 Interrupt	Interrupt flag for capture channel 1 event.
31:6	-	Reserved

TxIR (TIMERx[0])

Table

426. Interrupt Register (T[0/1/2/3]IR - addresses 0x4000 4000, 0x4000 8000, 0x4009 0000, 0x4009 4000) bitdescription

Bit	Symbol	Description	TxTCR (TIMERx[1])	Reset Value
0	Counter Enable	When one, the Timer Counter and Prescale Counter are enabled for counting. When 1, the counters are disabled.		0
1	Counter Reset	When one, the Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until TCR[1] is returned to zero.		0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.		NA

Table 427. Timer Control Register (TCR, TIMERN: TnTCR - addresses 0x4000 4004, 0x4000 8004, 0x4009 0004, 0x4009 4004) bit description

Timers como match

Table 429. Match Control Register (T[0/1/2/3]MCR - addresses 0x4000 4014, 0x4000 8014, 0x4009 0014, 0x4009 4014) bit description			
Bit	Symbol	Value	Description
0	MR0I	1	Interrupt on MR0: an interrupt is generated when MR0 matches the value in the TC.
		0	This interrupt is disabled
1	MR0R	1	Reset on MR0: the TC will be reset if MR0 matches it.
		0	Feature disabled.
2	MR0S	1	Stop on MR0: the TC and PC will be stopped and TCR[0] will be set to 0 if MR0 matches the TC.
		0	Feature disabled.
3	MR1I	1	Interrupt on MR1: an interrupt is generated when MR1 matches the value in the TC.
		0	This interrupt is disabled
4	MR1R	1	Reset on MR1: the TC will be reset if MR1 matches it.
		0	Feature disabled.
5	MR1S	1	Stop on MR1: the TC and PC will be stopped and TCR[0] will be set to 0 if MR1 matches the TC.
		0	Feature disabled.

bit 12 a 31: Reserved

Bit	Symbol	Value
0	MR0I	1
		0
1	MR0R	1
		0
2	MR0S	1
		0
3	MR1I	1
		0
4	MR1R	1
		0
5	MR1S	1
		0
6	MR2I	1
		0
7	MR2R	1
		0
8	MR2S	1
		0
9	MR3I	1
		0
10	MR3R	1
		0
11	MR3S	1
		0

CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Table 431. External Match Register (T[0/1/2/3]EMR - addresses 0x4000 403C, 0x4000 803C, 0x4009 003C, 0x4009 403C) bit description

Bit	Symbol	Description	Reset Value
		TxEMR (no está en posiciones contiguas) <code>#define TxEMR (* ((_RWuint32_t *) 0x[ver dirección]UL))</code>	
0	EM0	External Match 0. When a match occurs between the TC and MR0, this bit can either toggle, go low, go high, or do nothing, depending on bits 5:4 of this register. This bit can be driven onto a MATn.0 pin, in a positive-logic manner (0 = low, 1 = high).	0
1	EM1	External Match 1. When a match occurs between the TC and MR1, this bit can either toggle, go low, go high, or do nothing, depending on bits 7:6 of this register. This bit can be driven onto a MATn.1 pin, in a positive-logic manner (0 = low, 1 = high).	0
2	EM2	External Match 2. When a match occurs between the TC and MR2, this bit can either toggle, go low, go high, or do nothing, depending on bits 9:8 of this register. This bit can be driven onto a MATn.2 pin, in a positive-logic manner (0 = low, 1 = high).	0
3	EM3	External Match 3. When a match occurs between the TC and MR3, this bit can either toggle, go low, go high, or do nothing, depending on bits 11:10 of this register. This bit can be driven onto a MATn.3 pin, in a positive-logic manner (0 = low, 1 = high).	0
5:4	EMC0	External Match Control 0. Determines the functionality of External Match 0. Table 432 shows the encoding of these bits.	00
7:6	EMC1	External Match Control 1. Determines the functionality of External Match 1. Table 432 shows the encoding of these bits.	00
9:8	EMC2	External Match Control 2. Determines the functionality of External Match 2. Table 432 shows the encoding of these bits.	00
11:10	EMC3	External Match Control 3. Determines the functionality of External Match 3. Table 432 shows the encoding of these bits.	00
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 432. External Match Control

EMR[11:10], EMR[9:8], Function

EMR[7:6], or EMR[5:4]

00	Do Nothing.
01	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).
10	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).
11	Toggle the corresponding External Match bit/output.

Timers como captura

Table 428. Count Control Register (T[0/1/2/3]CTCR - addresses 0x4000 4070, 0x4000 8070, 0x4009 0070, 0x4009 4070) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	Counter/Timer Mode	00	This field selects which rising PCLK edges can increment the Timer's Prescale Counter (PC), or clear the PC and increment the Timer Counter (TC).	00
		01	Timer Mode: the TC is incremented when the Prescale Counter matches the Prescale Register. The Prescale Counter is incremented on every rising PCLK edge.	
		10	Counter Mode: TC is incremented on rising edges on the CAP input selected by bits 3:2.	
		11	Counter Mode: TC is incremented on falling edges on the CAP input selected by bits 3:2.	
3:2	Count Input Select	00	When bits 1:0 in this register are not 00, these bits select which CAP pin is sampled for clocking.	00
		01	CAPn.0 for TIMERn	
		10	Reserved	
		11	Reserved	
Note: If Counter mode is selected for a particular CAPn input in the TnCTCR, the 3 bits for that input in the Capture Control Register (TnCCR) must be programmed as 000. However, capture and/or interrupt can be selected for the other 3 CAPn inputs in the same timer.				
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 430. Capture Control Register (T[0/1/2/3]CCR - addresses 0x4000 4028, 0x4000 8020, 0x4009 0028, 0x4009 4028) bit description

Bit	Symbol	Value	Description	Reset Value
TxCCR (TIMERx[9])				
0	CAP0RE	1	Capture on CAPn.0 rising edge: a sequence of 0 then 1 on CAPn.0 will cause CR0 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
1	CAP0FE	1	Capture on CAPn.0 falling edge: a sequence of 1 then 0 on CAPn.0 will cause CR0 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
2	CAP0I	1	Interrupt on CAPn.0 event: a CR0 load due to a CAPn.0 event will generate an interrupt.	0
		0	This feature is disabled.	
3	CAP1RE	1	Capture on CAPn.1 rising edge: a sequence of 0 then 1 on CAPn.1 will cause CR1 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
4	CAP1FE	1	Capture on CAPn.1 falling edge: a sequence of 1 then 0 on CAPn.1 will cause CR1 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
5	CAP1I	1	Interrupt on CAPn.1 event: a CR1 load due to a CAPn.1 event will generate an interrupt.	0
		0	This feature is disabled.	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

¿Cuáles pines pueden ser salidas de match?

Table 79. Pin function select register 0 (PINSEL0 - address 0x4002 C000) bit description

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00

Table 82. Pin function select register 3 (PINSEL3 - address 0x4002 C00C) bit description

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
13:12	P1.22	GPIO Port 1.22	MCOB0	USB_PWRD	MAT1.0	00
19:18	P1.25	GPIO Port 1.25	MCOA1	Reserved	MAT1.1	00
25:24	P1.28	GPIO Port 1.28	MCOA2	PCAP1.0	MAT0.0	00
27:26	P1.29	GPIO Port 1.29	MCOB2	PCAP1.1	MAT0.1	00

Table 84. Pin function select register 7 (PINSEL7 - address 0x4002 C01C) bit description

PINSEL7	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
19:18	P3.25 ^[1]	GPIO Port 3.25	Reserved	MAT0.0	PWM1.2	00
21:20	P3.26 ^[1]	GPIO Port 3.26	STCLK	MAT0.1	PWM1.3	00

Table 85. Pin function select register 9 (PINSEL9 - address 0x4002 C024) bit description

PINSEL9	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
25:24	P4.28	GPIO Port 4.28	RX_MCLK	MAT2.0	TXD3	00
27:26	P4.29	GPIO Port 4.29	TX_MCLK	MAT2.1	RXD3	00

¿Cuáles pines pueden ser entrada de captura?

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
9:8	P0.4 ^[1]	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5 ^[1]	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00
PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
15:14	P0.23 ^[1]	GPIO Port 0.23	AD0.0	I2SRX_CLK	CAP3.0	00
17:16	P0.24 ^[1]	GPIO Port 0.24	AD0.1	I2SRX_WS	CAP3.1	00
PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
5:4	P1.18	GPIO Port 1.18	USB_UP_LED	PWM1.1	CAP1.0	00
7:6	P1.19	GPIO Port 1.19	MCOA0	USB_PPWR	CAP1.1	00
21:20	P1.26	GPIO Port 1.26	MCOB1	KEY4_RC	PWM1.6	CAP0.0
23:22	P1.27 ^[1]	GPIO Port 1.27	CLKOUT	USB_OVRCR	CAP0.1	00

CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

ADC/DAC

29.5 Register description

The A/D Converter registers are shown in [Table 530](#).

Table 530. ADC registers

Generic Name	Description	Access	Reset value ^[1]	AD0 Name & Address
ADCR	A/D Control Register. The ADCR register must be written to select the operating mode before A/D conversion can occur.	R/W	1	AD0CR - 0x4003 4000
ADGDR	A/D Global Data Register. This register contains the ADC's DONE bit and the result of the most recent A/D conversion.	R/W	NA	AD0GDR - 0x4003 4004
ADINTEN	A/D Interrupt Enable Register. This register contains enable bits that allow the DONE flag of each A/D channel to be included or excluded from contributing to the generation of an A/D interrupt.	R/W	0x100	AD0INTEN - 0x4003 400C
ADDR0	A/D Channel 0 Data Register. This register contains the result of the most recent conversion completed on channel 0.	RO	NA	AD0DR0 - 0x4003 4010
ADDR1	A/D Channel 1 Data Register. This register contains the result of the most recent conversion completed on channel 1.	RO	NA	AD0DR1 - 0x4003 4014
ADDR2	A/D Channel 2 Data Register. This register contains the result of the most recent conversion completed on channel 2.	RO	NA	AD0DR2 - 0x4003 4018
ADDR3	A/D Channel 3 Data Register. This register contains the result of the most recent conversion completed on channel 3.	RO	NA	AD0DR3 - 0x4003 401C
ADDR4	A/D Channel 4 Data Register. This register contains the result of the most recent conversion completed on channel 4.	RO	NA	AD0DR4 - 0x4003 4020
ADDR5	A/D Channel 5 Data Register. This register contains the result of the most recent conversion completed on channel 5.	RO	NA	AD0DR5 - 0x4003 4024
ADDR6	A/D Channel 6 Data Register. This register contains the result of the most recent conversion completed on channel 6.	RO	NA	AD0DR6 - 0x4003 4028
ADDR7	A/D Channel 7 Data Register. This register contains the result of the most recent conversion completed on channel 7.	RO	NA	AD0DR7 - 0x4003 402C
ADSTAT	A/D Status Register. This register contains DONE and OVERRUN flags for all of the A/D channels, as well as the A/D interrupt/DMA flag.	RO	0	AD0STAT - 0x4003 4030
ADTRIM	ADC trim register.	R/W	0x0000 0F00	AD0TRIM - 0x4003 4034



CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Registro ADCR: Configura el modo de conversión- (R/W)

BURST: Conversiones continuas o controladas por software

"1" : El convertidor AD realiza conversiones de hasta 200 kHz, de barrido (si es necesario) a través de los pinos seleccionados por los bits del campo SEL. La primera conversión de inicio corresponde al menos significativo en 1 del campo SEL, a continuación, el siguiente adc seleccionado

Nota: Los bits de START deben ser 000 para iniciar conversiones continuas (BURST = 1).

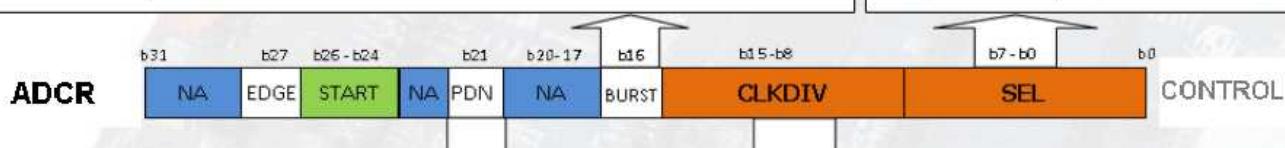
"0" : Controladas por software. Necesitan 65 ciclos de clock

SEL (bit 0 – 7): Reset value=1

Selecciona cuál de los **ADC0..7**: 0 Pins es (son)

objeto de muestreo y conversión. Para ADC0, bit 0 En el modo controlado por software, sólo uno de los estos bits debe ser 1.

En el modo de exploración de hardware, cualquier valor es permitido.



START: Inicio y parada de conversión

"000" Stop (se debe usar cuando se borra PDN)

"001" Inicia la conversión.

Las siguientes combinaciones Inician la conversión cuando se produce el flanco seleccionado por **EDGE** (bit 27) en el pin asociado

"010" en el pin P2.10

"011" en el pin P1.27 CAP0.1 pin.

"100" se produce por match de timer MAT0.1

"101" se produce por match de timer MAT0.3

"110" se produce por match de timer MAT1.0

"111" se produce por match de timer MAT1.1

Si EDGE es

1 Inicia con un flanco descendente en CAP / MAT

0 Inicia con un flanco ascendente en CAP / MAT

El **reloj** (PCLK_ADC0) se divide por (este valor más uno) para producir el reloj para el convertidor A / D, que debe ser menor que o igual a 13 MHz. Típicamente, el software debe programar el valor más pequeño en este campo que produce un reloj < 13 MHz

$$f_{ADC} = f_{CLK_ADC} / (65 * (CLKDIV + 1))$$

$$f_{ADC \ MAX} \leq 200 \text{ kHz}$$

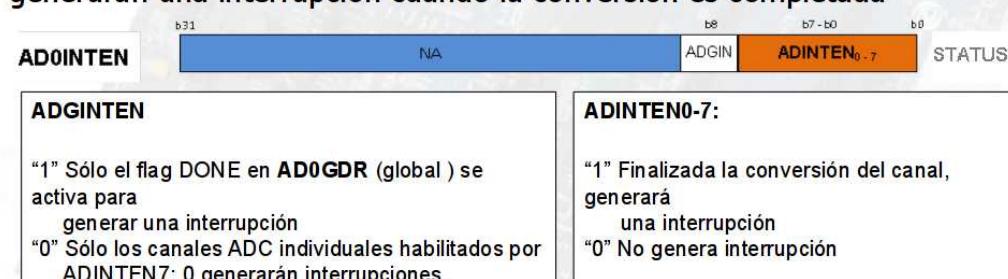
Bit	Symbol	Description
23.22	PCLK_DAC	Peripheral clock selection for DAC.
25.24	PCLK_ADC	Peripheral clock selection for ADC.

PCLKSEL

// si CCLK = 100MHz, y PCLK_ADC = 0 => $f_{clk_adc} = f_{clock} / 4 = 25MHz$
 PCLKSEL0 &= ~(3<<24);
 // CLKDIV = 1 => fADC = 200kHz
 AD0CR |= (1<<8);

AD0INTEN - Interrupt Enable Register (R/W)

Habilitación de canales de interrupción - Habilita qué canales generarán una interrupción cuando la conversión es completada



AD0STAT - Status Register - (R/W)

Estado de conversión de todos los canales

Este registro de Status permite comprobar el estado de todos los canales al mismo tiempo.

Los indicadores DONE y OVERRUN que aparecen en el ADDRn registran para cada canal se reflejan en ADSTAT. El flag de interrupción (operador lógico OR de todos los flags de hecho) también se encuentra en ADSTAT.



DONEx : Este bit refleja el indicador de estado DONE del registro ADDRx de cada canal.

OVERRUNx: Este bit refleja el indicador de estado OVERRUN del registro ADDRx de cada canal.

ADINT : Este bit es el Flag de interrupción del A / D. Es "1" cuando cualquier canal A / D se establece su flag en DONE.

CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Puerto Serie

$$UART1_{baudrate} = \frac{PCLK}{16 \times (256 \times U1DLM + U1DLL) \times \left(1 + \frac{DivAddVal}{MulVal}\right)}$$

```
#define DIR_UART0 (( volatile uint32_t * ) 0x4000C000UL)
#define DIR_UART1 (( volatile uint32_t * ) 0x40010000UL)
```

PUERTO SERIE: La dirección de los puertos serie del sistema, se encuentra a partir de la dirección 0x0400 de memoria																																											
Line Control Register: LCR - BASE + 3 (activo alto)																																											
Word Length (WLS0 – WLS1)				Number of Stop Bits (STB)																																							
<table border="1"> <tr> <th>B1</th><th>B0</th><th colspan="2">Character length</th></tr> <tr> <td>0</td><td>0</td><td colspan="2">5</td></tr> <tr> <td>0</td><td>1</td><td colspan="2">6</td></tr> <tr> <td>1</td><td>0</td><td colspan="2">7</td></tr> <tr> <td>1</td><td>1</td><td colspan="2">8</td></tr> </table>				B1	B0	Character length		0	0	5		0	1	6		1	0	7		1	1	8		<table border="1"> <tr> <th>B2</th><th>Word length</th><th colspan="2">Stop bits</th></tr> <tr> <td>0</td><td>5,6,7 o 8</td><td colspan="2">1</td></tr> <tr> <td>1</td><td>5</td><td colspan="2">1,5</td></tr> <tr> <td>1</td><td>6,7 o 8</td><td colspan="2" rowspan="3">2</td></tr> </table>				B2	Word length	Stop bits		0	5,6,7 o 8	1		1	5	1,5		1	6,7 o 8	2	
B1	B0	Character length																																									
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Parity Enable (PEN)				Even Parity Select (EPS)																																							
<table border="1"> <tr> <th>B3</th><th>Paridad</th></tr> <tr> <td>0</td><td>OFF</td></tr> <tr> <td>1</td><td>ON</td></tr> </table>				B3	Paridad	0	OFF	1	ON	<table border="1"> <tr> <th>B4</th><th>Parity</th></tr> <tr> <td>0</td><td>Odd</td></tr> <tr> <td>1</td><td>Even</td></tr> </table>				B4	Parity	0	Odd	1	Even																								
B3	Paridad																																										
0	OFF																																										
1	ON																																										
B4	Parity																																										
0	Odd																																										
1	Even																																										
Stick Parity				Set Break																																							
<table border="1"> <tr> <th>B5</th><th>B4</th><th>B3</th><th>Logic of parity bit</th></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Logic 0</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>Logic 1</td></tr> <tr> <td>0</td><td>X</td><td>X</td><td>Disable</td></tr> </table>				B5	B4	B3	Logic of parity bit	1	1	1	Logic 0	1	0	1	Logic 1	0	X	X	Disable	<table border="1"> <tr> <th>B6</th><th>Causes break conditions (SOUT)</th></tr> <tr> <td>0</td><td>Disable</td></tr> <tr> <td>1</td><td>Enable</td></tr> </table>				B6	Causes break conditions (SOUT)	0	Disable	1	Enable														
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0	Disable																																										
1	Enable																																										
Divisor Latch Access Bit (DLAB)				<table border="1"> <tr> <th>B7</th><th>Access</th></tr> <tr> <td>0</td><td>Receiver Buffer and Interrupt Enable Register</td></tr> <tr> <td>1</td><td>Divisor Latches of the Baud Generator</td></tr> </table>				B7	Access	0	Receiver Buffer and Interrupt Enable Register	1	Divisor Latches of the Baud Generator																														
B7	Access																																										
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Line Status Register: LSR - BASE + 5 (activo alto)																																											
<table border="1"> <tr> <td>0</td><td>TEMT 6</td><td>THRE 5</td><td>BI 4</td><td>FE 3</td><td>PE 2</td><td>OE 1</td><td>DR 0</td></tr> <tr> <td>Transmitter Empty</td><td>Transmitter Holding Register Empty</td><td>Transmitter Register Empty</td><td></td><td>Framing Error Break Interrupt</td><td>Parity Error</td><td>Overrun Error</td><td>Data Ready</td></tr> </table>								0	TEMT 6	THRE 5	BI 4	FE 3	PE 2	OE 1	DR 0	Transmitter Empty	Transmitter Holding Register Empty	Transmitter Register Empty		Framing Error Break Interrupt	Parity Error	Overrun Error	Data Ready																				
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INICIALIZACION DEL PUERTO TRANSMISION - REGISTROS																																											
				<p>Cuando pasa de (1) a (2) se activa THRE (BASE+5, bit 5) Cuando sale de (2) se activa TEMT (BASE + 5 , bit 6)</p>																																							
INICIALIZACION DEL PUERTO RECEPCION - REGISTROS																																											
				<p>Cuando pasa de (2) a (1) se activa DR (BASE + 5 , bit 0)</p>																																							
Interrupt Enable Register: IER - BASE + 1 (activo alto)																																											
<table border="1"> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>IER(3)</td><td>IER(2)</td><td>IER(1)</td><td>IER(0)</td></tr> </table>								0	0	0	0	IER(3)	IER(2)	IER(1)	IER(0)																												
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<p>IER0: A 1 si habilitar interrupción de dato disponible. IER1: A 1 si habilitar interrupción de registro de retención de transmisión vacío. IER2: A 1 si habilitar interrupción de error de recepción (bits 1 al 4 del LSR). IER3: A 1 si habilitar interrupción ante el cambio del MSR (Registro de estado del modem).</p>																																											
Interrupt Ident Register: IIR - BASE + 2 (activo alto)																																											
<table border="1"> <tr> <td>0</td><td>0</td><td>b2</td><td>b1</td><td>b0</td><td></td><td></td><td></td></tr> </table>								0	0	b2	b1	b0																															
0	0	b2	b1	b0																																							
<p>b0 = 0 => Hay una interrupción pendiente de atención b0 = 1 => No hay una interrupción pendiente</p>																																											
<table border="1"> <tr> <th>b2</th><th>b1</th><th>Descripción</th></tr> <tr> <td>1</td><td>1</td><td>Errores y break (>)</td></tr> <tr> <td>1</td><td>0</td><td>Dato disponible</td></tr> <tr> <td>0</td><td>1</td><td>THR disponible</td></tr> <tr> <td>0</td><td>0</td><td>Estado del MODEM (<)</td></tr> </table>								b2	b1	Descripción	1	1	Errores y break (>)	1	0	Dato disponible	0	1	THR disponible	0	0	Estado del MODEM (<)																					
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