**计算机组成原理 实验报告**

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**一、实验题目：**

实验四 多周期CPU

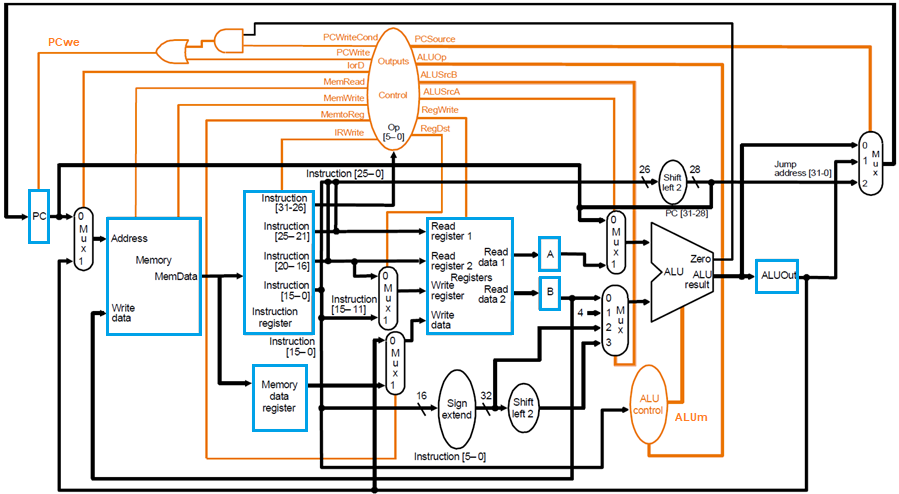
**二、实验目的：**

1. 理解计算机硬件的基本组成、结构和工作原理；
2. 掌握数字系统的设计和调试方法；
3. 熟练掌握数据通路和控制器的设计和描述方法。

**三、实验平台：**

ISE / Vivado（暂不支持其他Verilog HDL开发环境的检查）

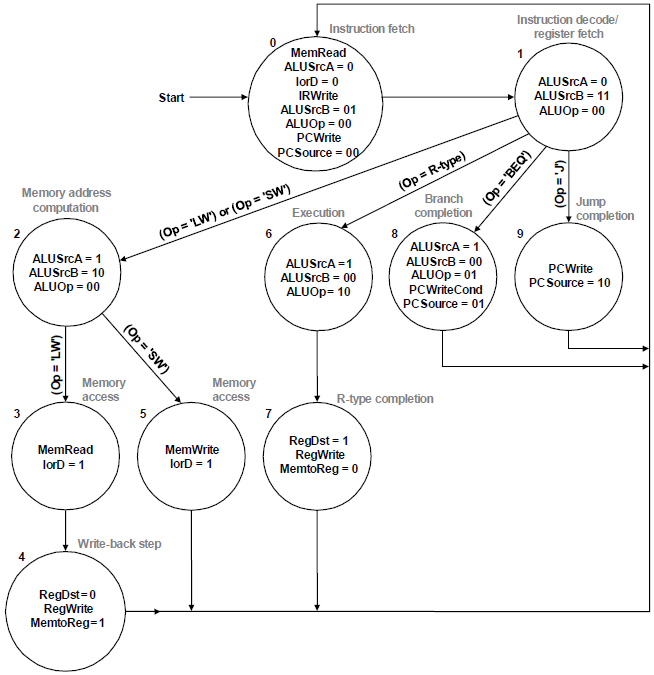
**四、实验过程：**



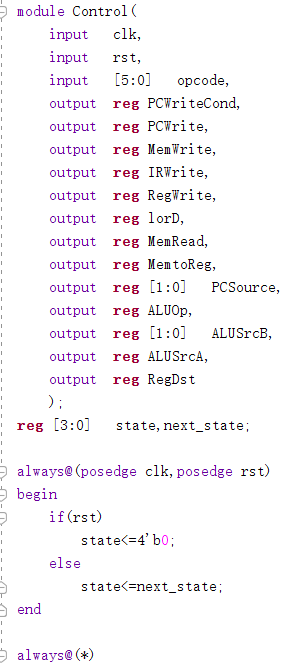
根据上图设计多周期CPU相关部件。

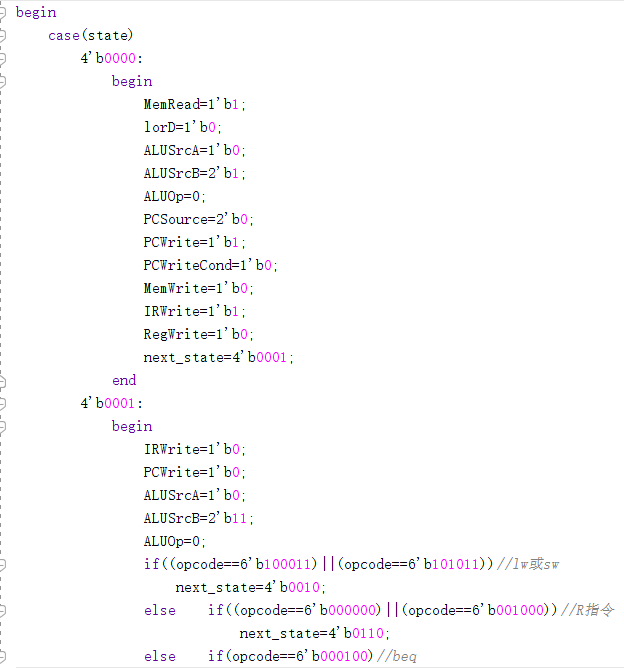
**控制器:**

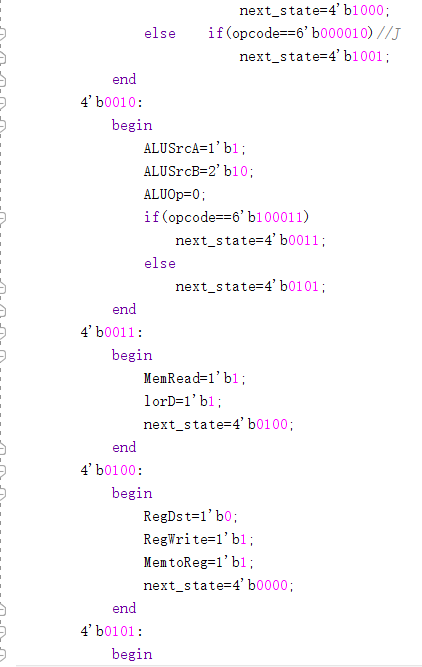


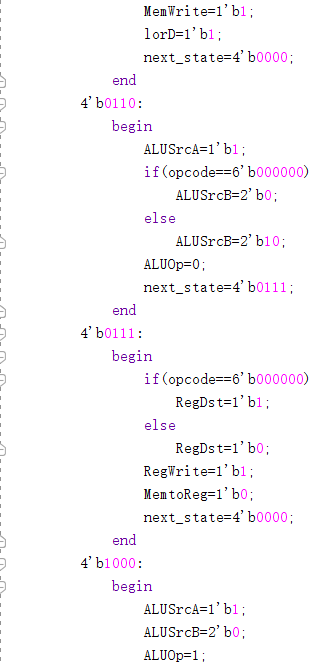


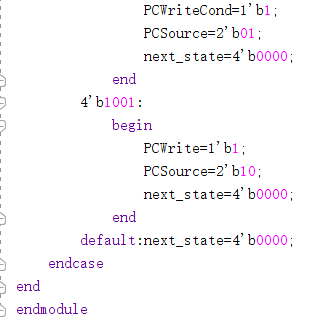
根据状态图及相关信号使能设计控制器：



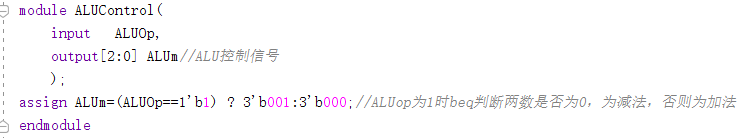




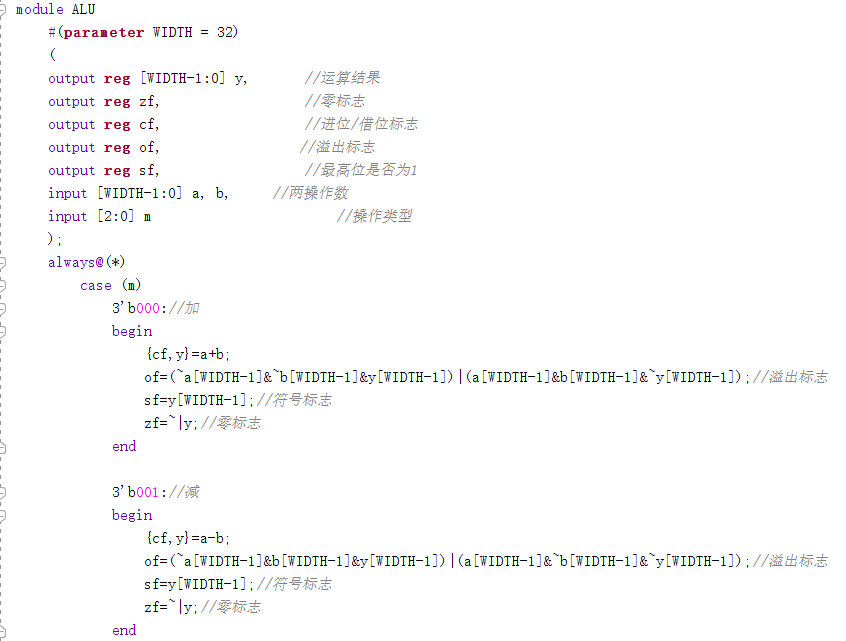


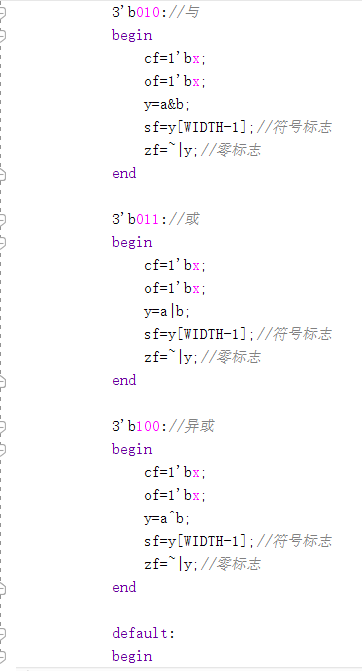


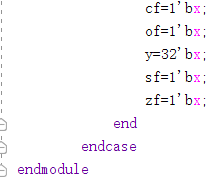
**ALUControl：**



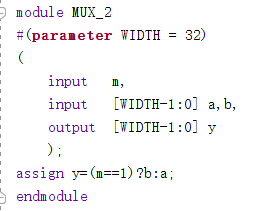
**ALU：**

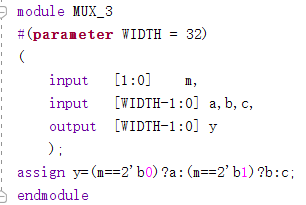


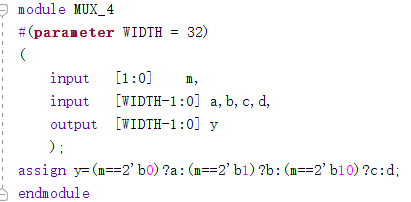




**各种MUX：**



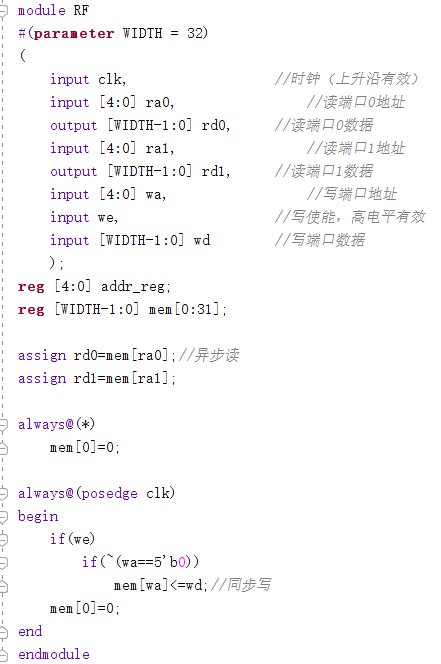




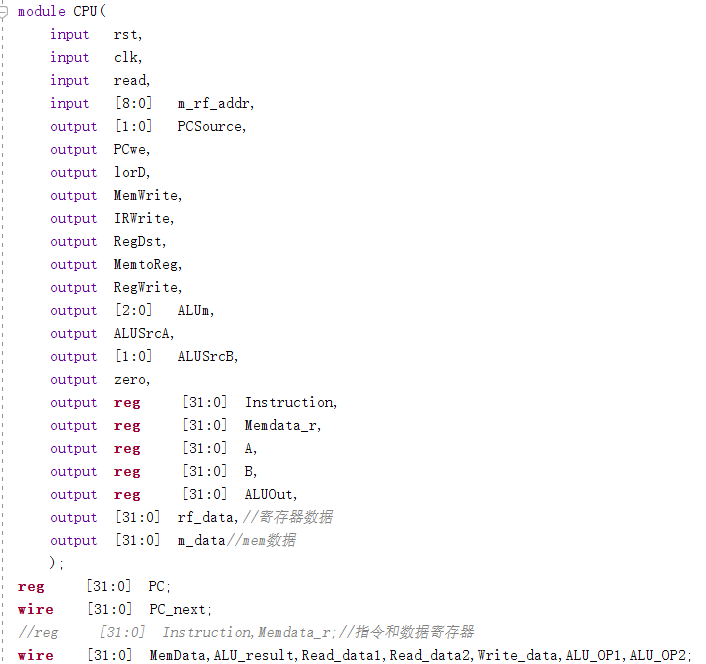
**Mem:**

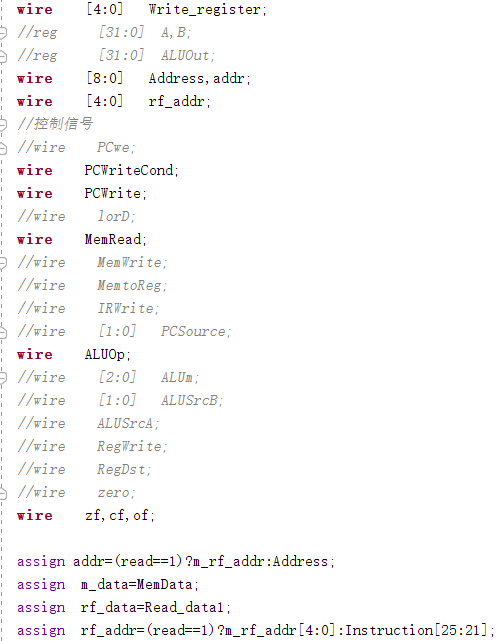
指令和数据存储共用一个RAM存储器，采用IP例化实现，容量为512 x 32位的分布式存储器。

**寄存器堆：**

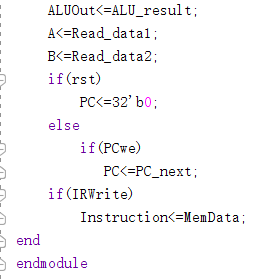


**CPU:**

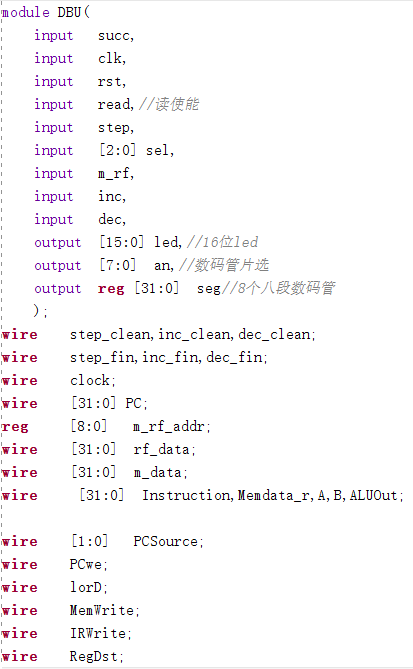


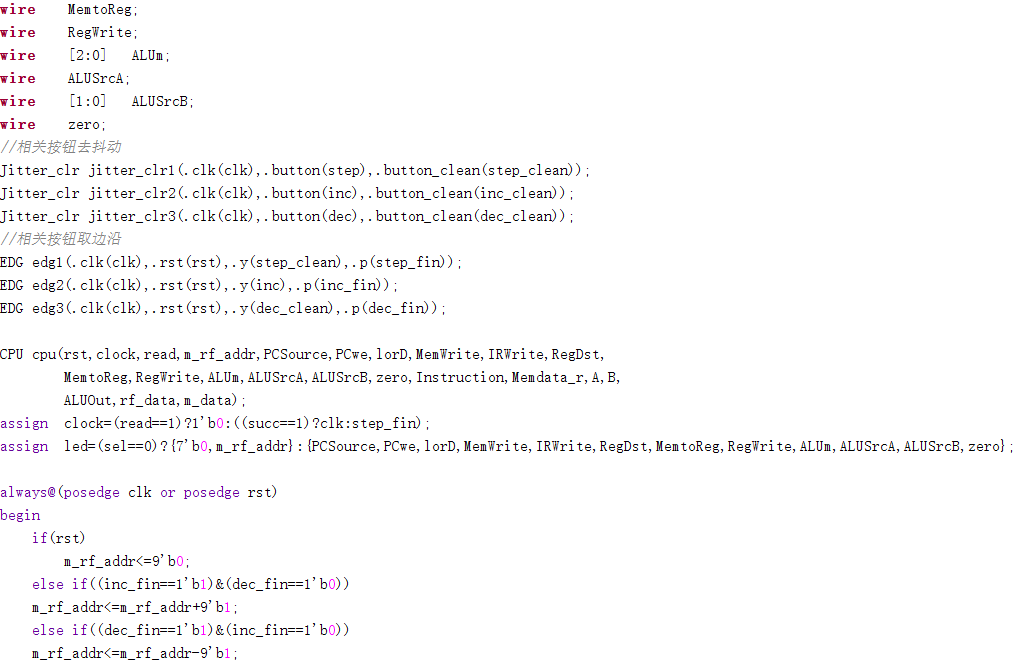


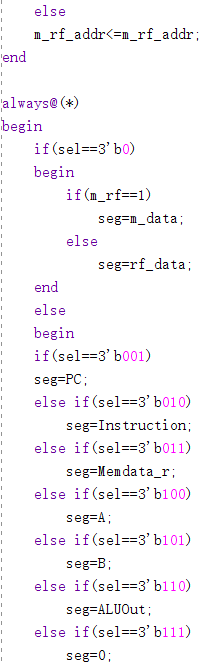


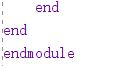


**DBU:**



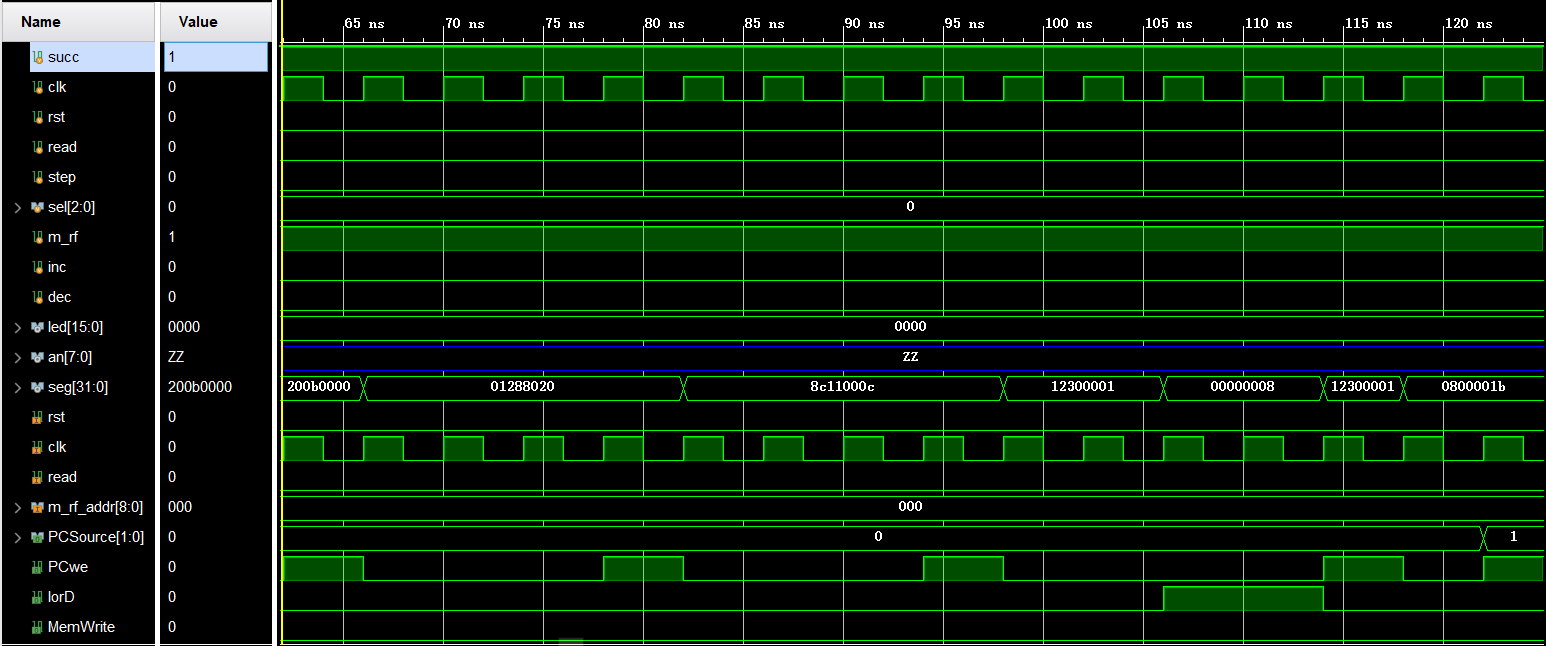


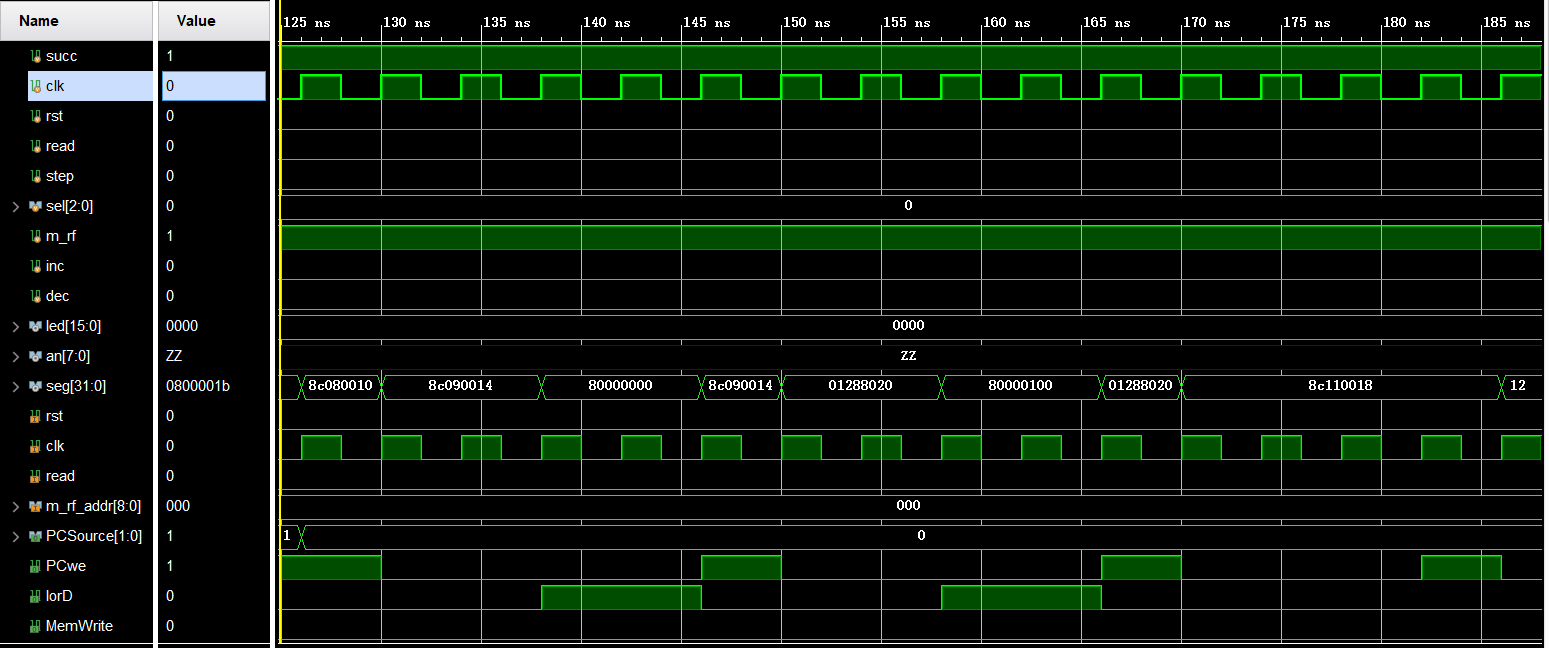




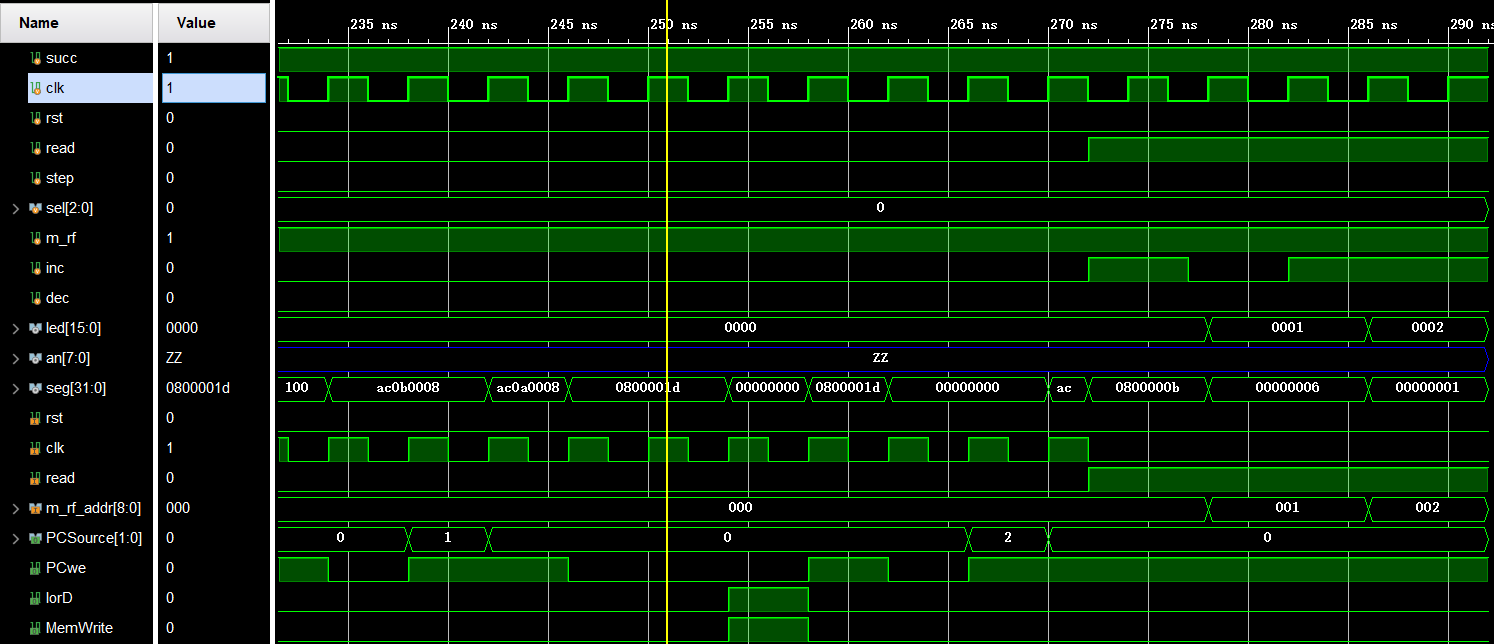
**五、实验结果：**

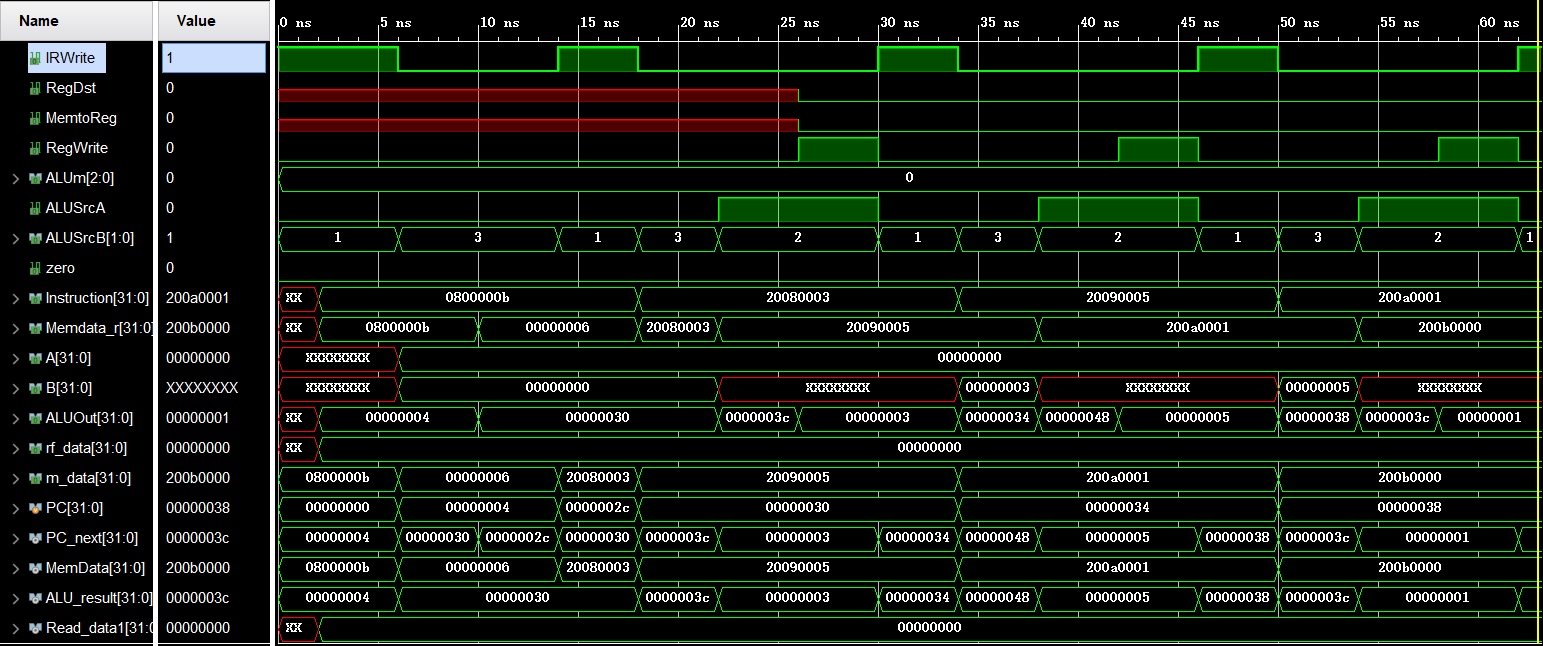


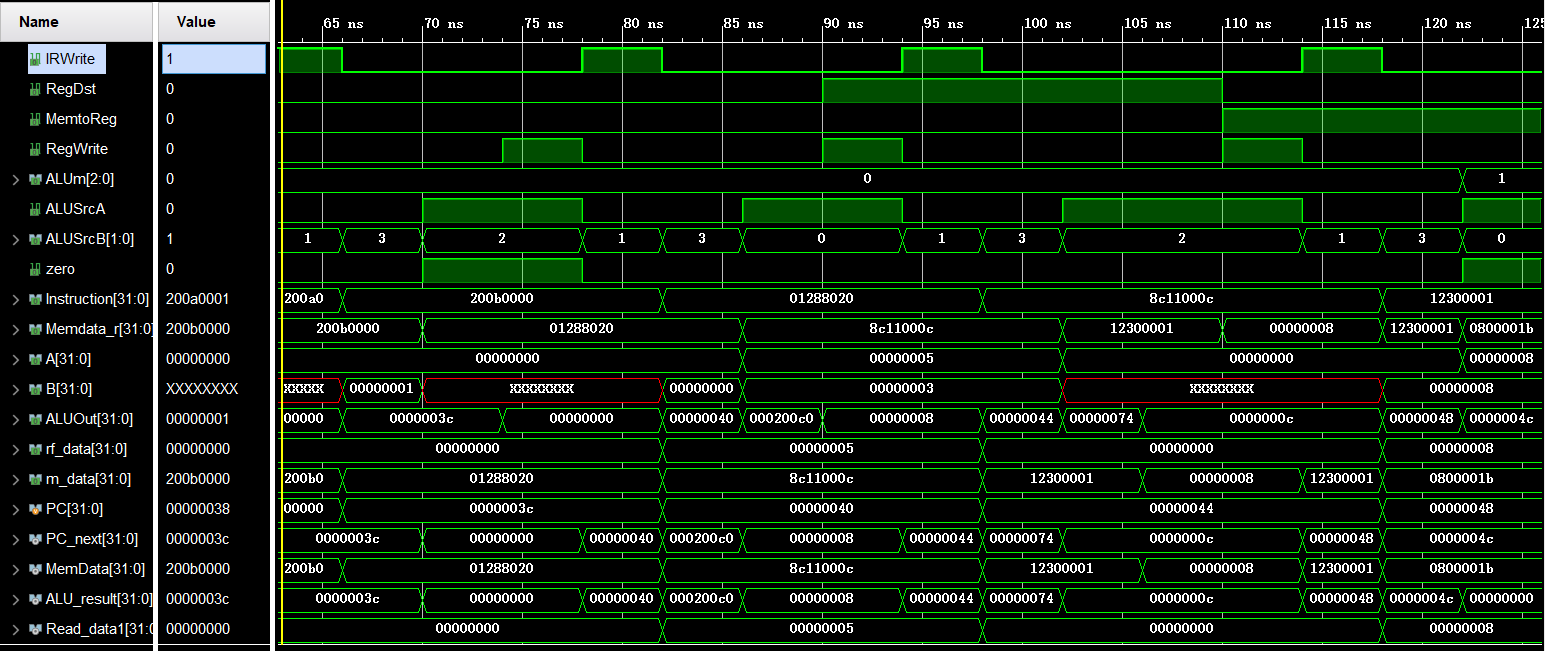


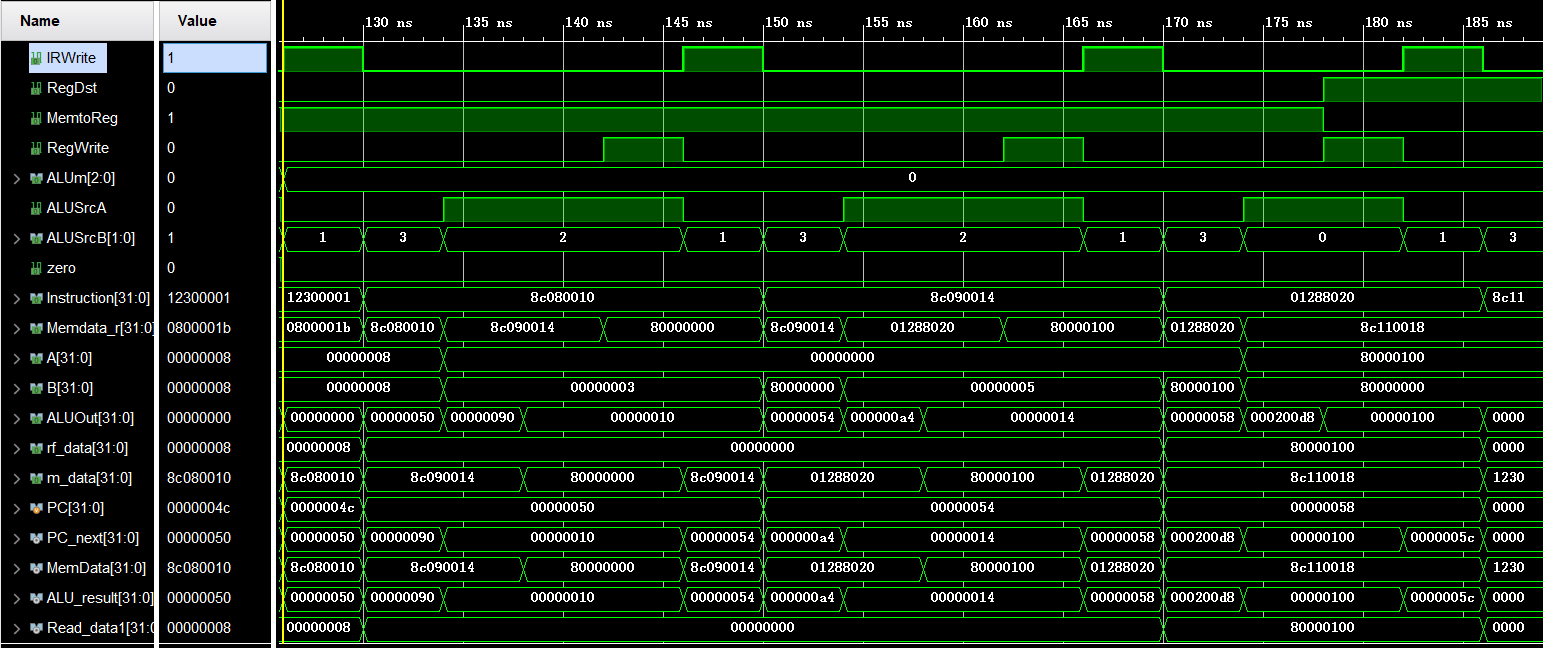


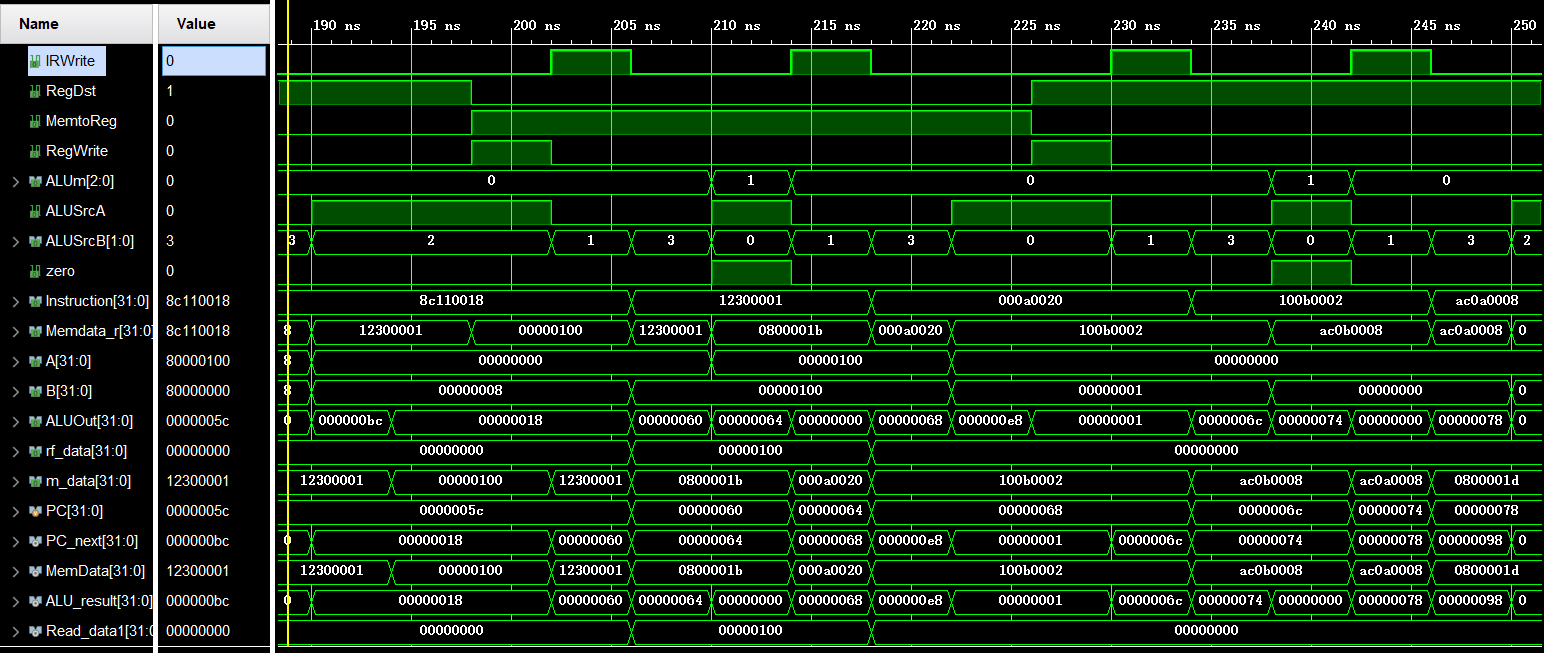


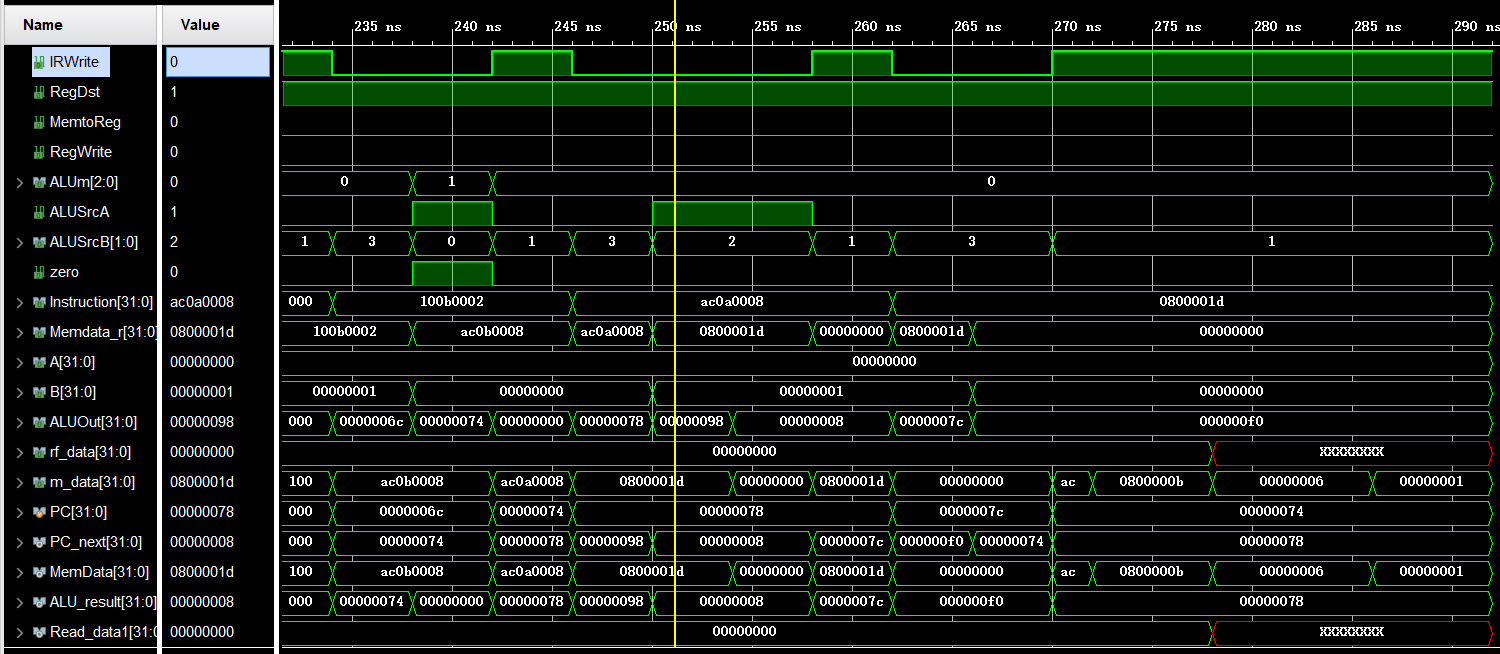


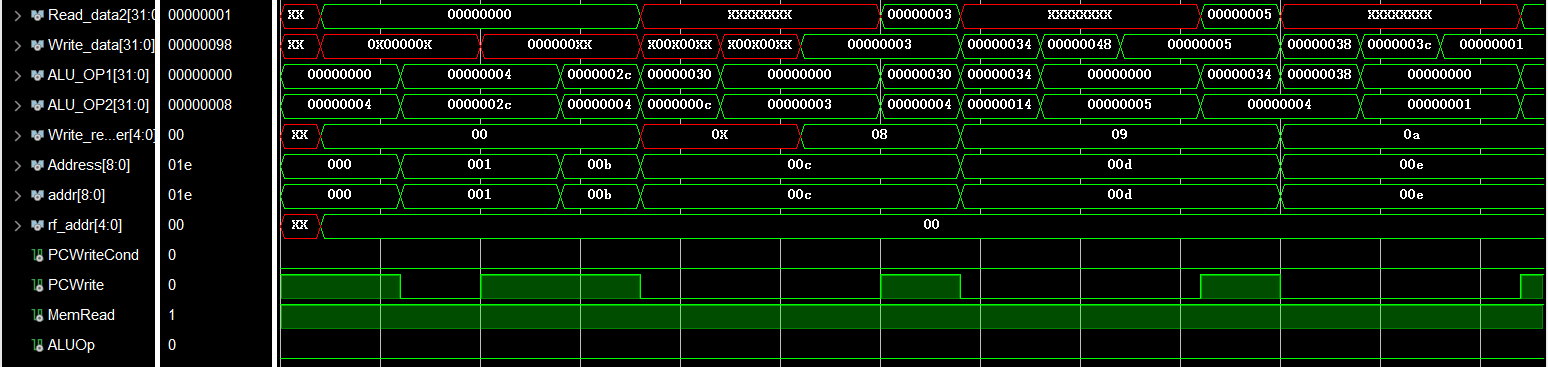


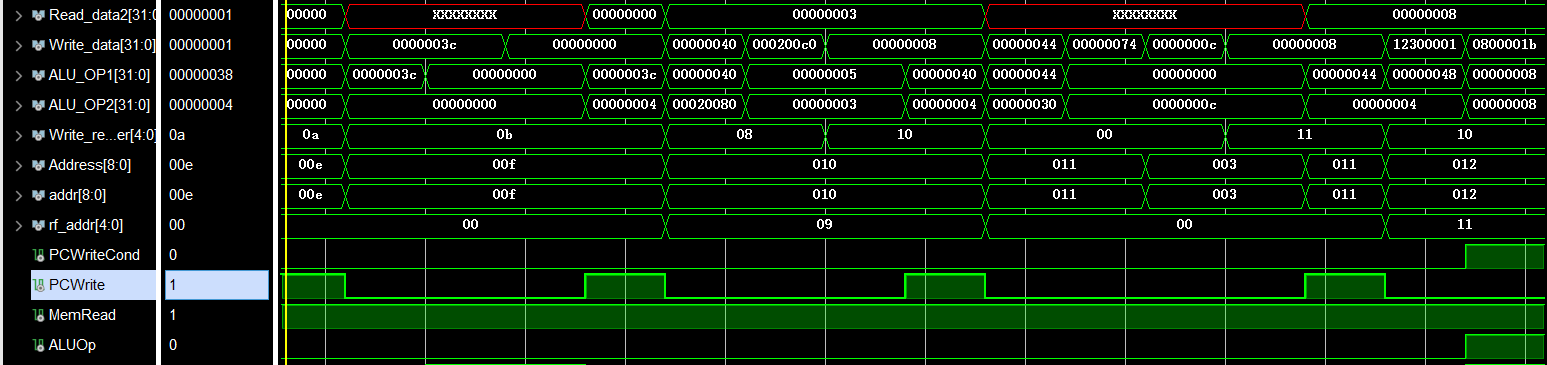


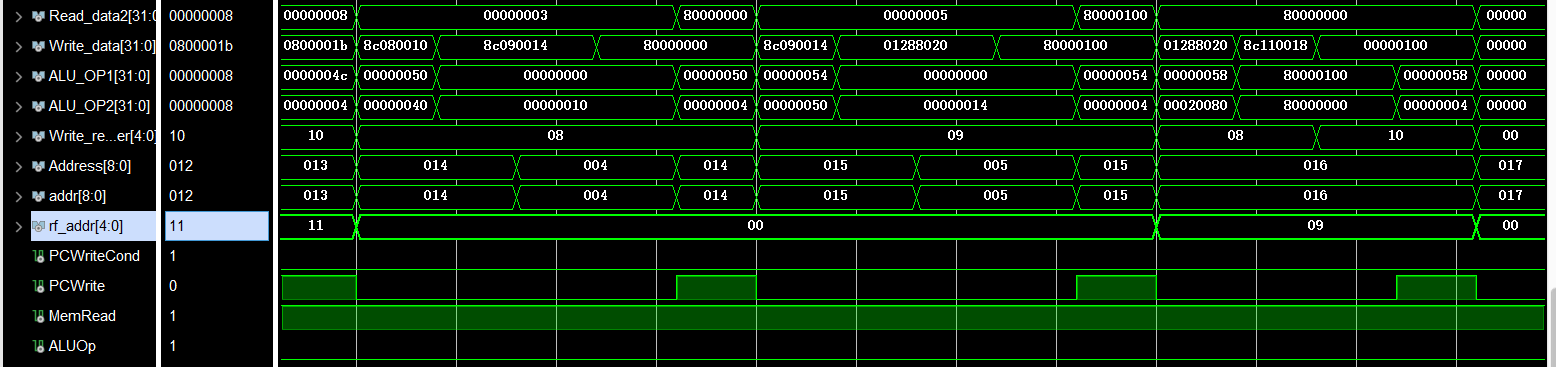


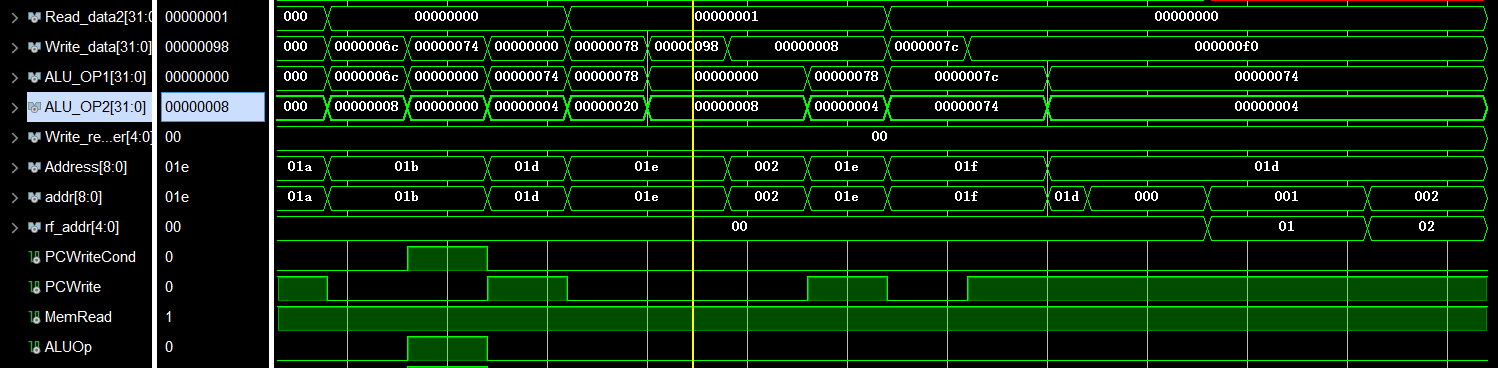
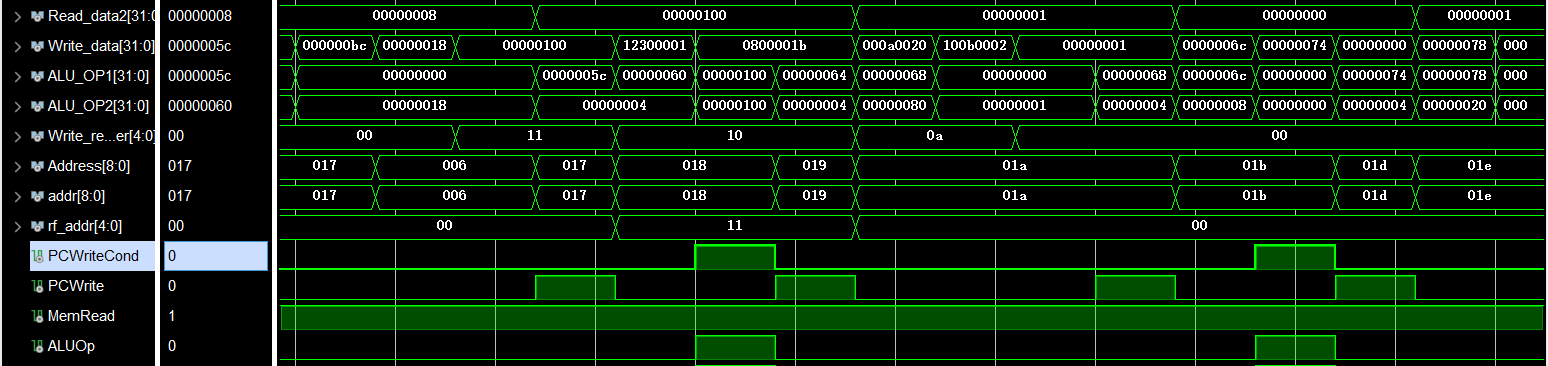












**六、心得体会：**

通过本次实验理解了计算机硬件的基本组成、结构和工作原理；掌握了数字系统的设计和调试方法；熟练掌握了数据通路和控制器的设计和描述方法。