

- I used the HDL programming in the Nand Tetris hardware simulator to implement this 16-bit register.
- This is created by forming arrays of 16 single-bit registers.
- Then connecting them together to form the 16-bit register.
- The 1-bit register has a Mux and DFF components.
- The chip interface consists of an input pin which carries a data bit, a load. bit which enables the cell for writes, and an output pin which emits the current state of the cell.
- This forms a single bit register.
- Then in the 16-bit register HDL file, I had to write 16 arrays of 1-bit registers and connect them with one another to implement the 16-bit register completely.
- The connection between the in [0] and out [0] bits is established using bus syntax, and this connection process is repeated up to the 16th bit. In other words, the input bit in [0] is linked to the output bit out [0] via bus syntax, and this connection is continued sequentially up to the 16th bit
- Then loaded the 16-bit register HDL file and the test file in Hardware simulator and ran it.
- The comparison ended successfully, showing that we created a 16-bit register successfully.

Hardware Simulator (2.5) - D:\Downloads\nand2tetris\nand2tetris\projects\03\Bit\Bit.hdl

File View Run Help

Chip Name: Bit (Clocked) Time: 107

| Input pins |       | Output pins |       |
|------------|-------|-------------|-------|
| Name       | Value | Name        | Value |
| in         | 1     | out         | 0     |
| load       | 0     |             |       |

| Internal pins |       |
|---------------|-------|
| Name          | Value |
| dffOut        | 0     |
| muxOut        | 0     |

```

HDL
/**
 * 1-bit register:
 * If load is asserted, the reg:
 * Otherwise, the register maint
 * out(t+1) = (load(t), in(t), c
 */
CHIP Bit {
  IN in, load;
  OUT out;

  PARTS:
  Mux(a=dffOut, b=in, sel=load;
  DFF(in=muxOut, out=out, out=

```

End of script - Comparison ended successfully

Hardware Simulator (2.5) - D:\Downloads\nand2tetris\nand2tetris\projects\03\Register.hdl

File View Run Help

Chip Name: Register (Clocked) Time: 74

| Input pins |       | Output pins |       |
|------------|-------|-------------|-------|
| Name       | Value | Name        | Value |
| in[16]     | 32767 | out[16]     | 32767 |
| load       | 1     |             |       |

| Internal pins |       |
|---------------|-------|
| Name          | Value |
|               |       |

```

HDL
// This file is part of vnm.nand
// and the book "The Elements of
// by Nisan and Schocken, MIT Pr
// File name: projects/03/a/Regi
/**
 * 16-bit register:
 * If load is asserted, the reg:
 * Otherwise, the register maint
 * out(t+1) = (load(t), in(t), c
 */
CHIP Register {
  IN in[16], load;
  OUT out[16];

```

End of script - Comparison ended successfully