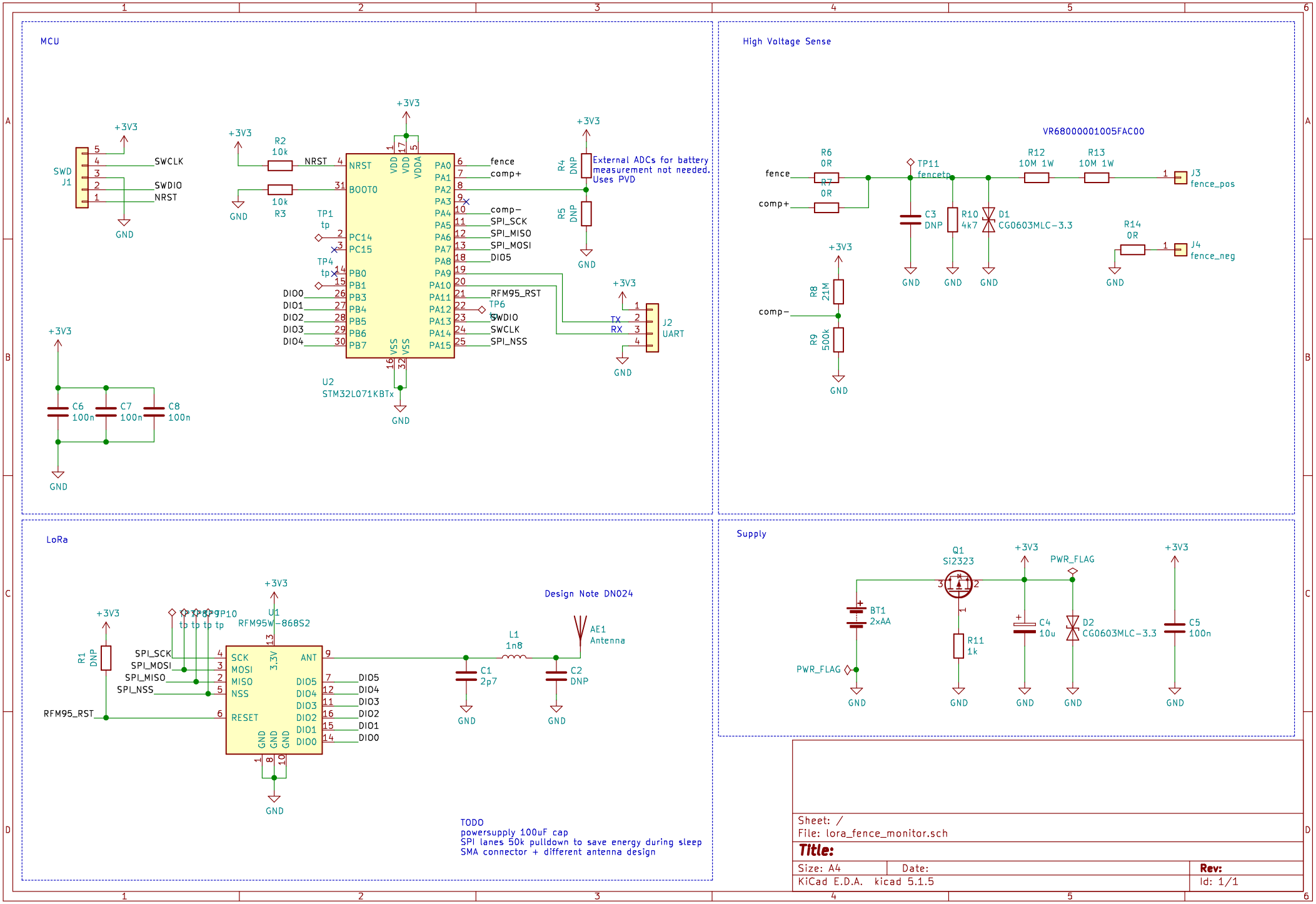
MCU
SWD
J1
SWCLK
SWDIO
NRST
+3V3
GND
R2
10k
R3
10k
NRST
TP1
tp
TP4
tp
DIO0
DIO1
DIO2
DIO3
DIO4
NRST
BOOT0
PC14
PC15
PB0
PB1
PB3
PB4
PB5
PB6
PB7
VDD
VDDA
VSS
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
fence
comp+
comp−
SPI_SCK
SPI_MISO
SPI_MOSI
DIO5
RFM95_RST
TP6
SWDIO
SWCLK
SPI_NSS
U2
STM32L071KBTx
R4
DNP
R5
DNP
External ADCs for battery measurement not needed. Uses PVD
J2
UART
TX
RX
C6
100n
C7
100n
C8
100n
High Voltage Sense
VR68000001005FAC00
R6
0R
R7
0R
TP11
fencetp
R12
10M 1W
R13
10M 1W
J3
fence_pos
C3
DNP
R10
4k7
D1
CG0603MLC-3.3
R14
0R
J4
fence_neg
R8
21M
R9
500k
LoRa
U1
RFM95W-868S2
TP10
tp tp tp tp
R1
DNP
SPI_SCK
SPI_MOSI
SPI_MISO
SPI_NSS
RFM95_RST
SCK
MOSI
MISO
NSS
RESET
3.3V
ANT
DIO5
DIO4
DIO3
DIO2
DIO1
DIO0
GND
L1
1n8
C1
2p7
C2
DNP
AE1
Antenna
Design Note DN024
TODO
powersupply 100uF cap
SPI lanes 50k pulldown to save energy during sleep
SMA connector + different antenna design
Supply
Q1
Si2323
BT1
2xAA
PWR_FLAG
R11
1k
C4
10u
D2
CG0603MLC-3.3
C5
100n
Sheet: /
File: lora_fence_monitor.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.5
Id: 1/1