Blocking-Waived Estimation: Improving the Worst-Case End-To-End Delay Analysis in Switched Ethernet

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Focus on **Time-Sensitive Networks**

Classic Ethernet

~~Best-effort service~~

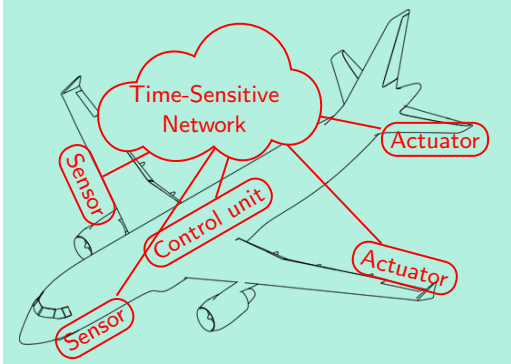
Time-Sensitive Networks

Bounded latency

and zero loss by congestion

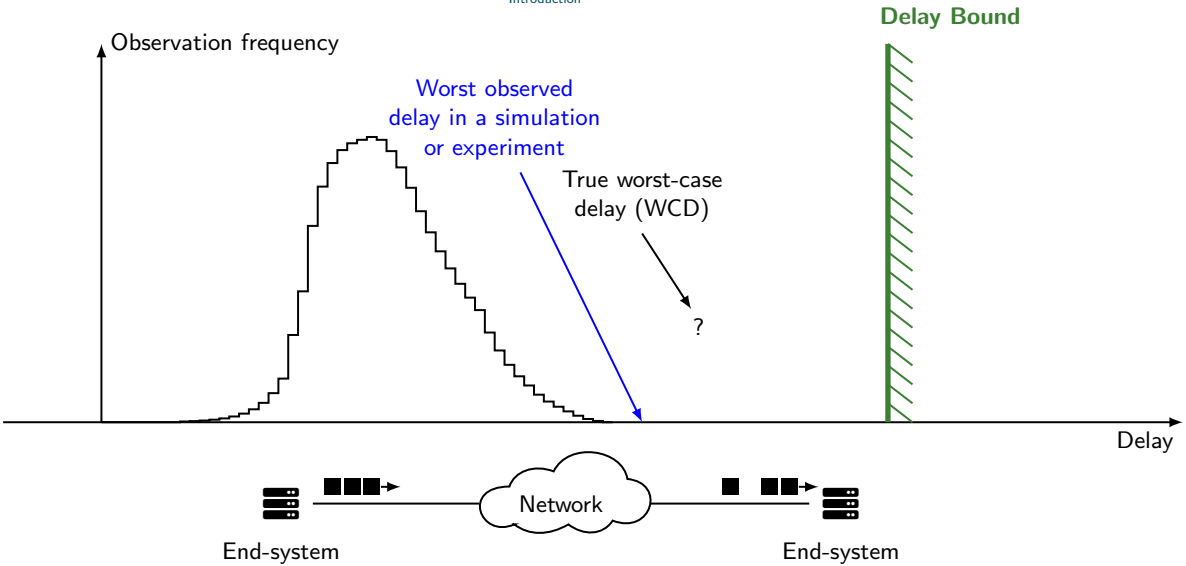
Deterministic service

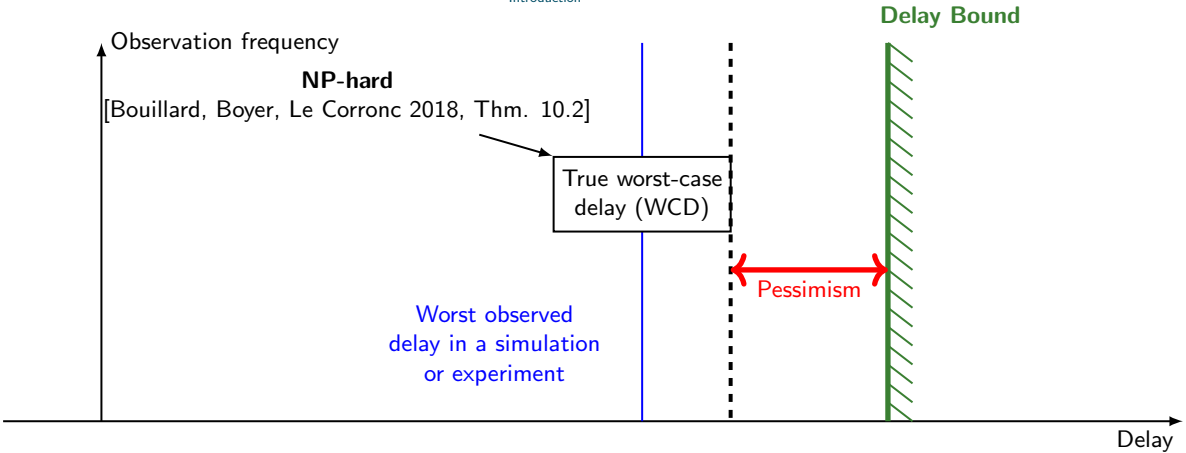
Cyber-Physical Systems



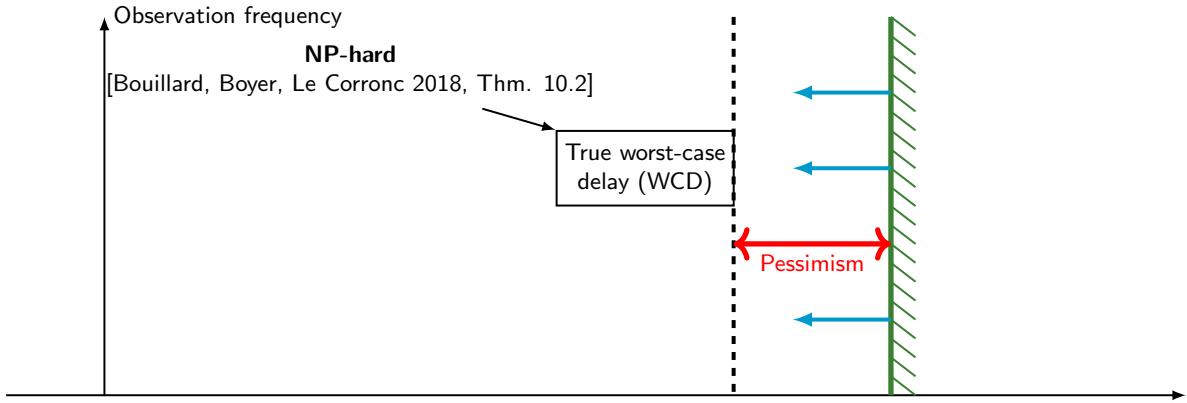
Safety-critical applications

IEEE Time-Sensitive Networking (TSN)
IETF Deterministic Networking (DetNet)


Delay Bound
Observation frequency
Worst observed
delay in a simulation
or experiment
True worst-case
delay (WCD)
?
Delay
Network
End-system
End-system



– [Bouillard, Boyer, Le Corronc 2018] Anne Bouillard, Marc Boyer, and Euriell Le Corronc [Oct. 2018]. *Deterministic Network Calculus*. https://doi.org/10.1002/9781119440284. John Wiley & Sons, Inc. DOI: 10.1002/9781119440284



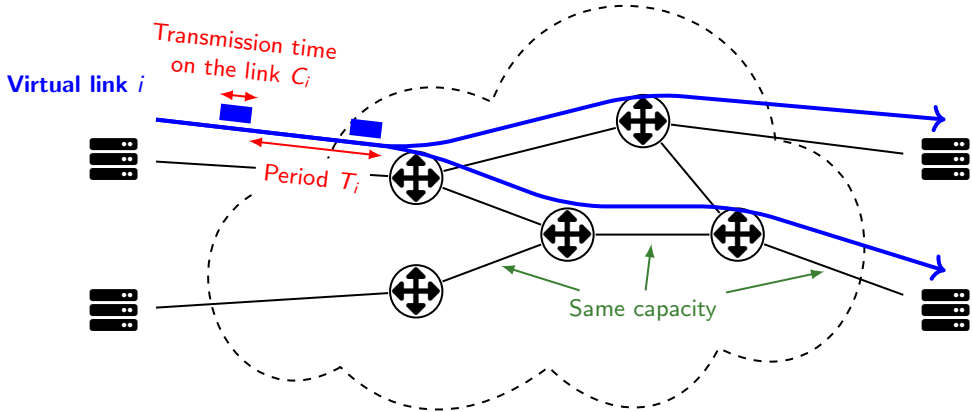
Several approaches:

- Network calculus
- Compositionnal performance Analysis

In our paper Reduce the pessimism of **Response-time analysis**

- ...

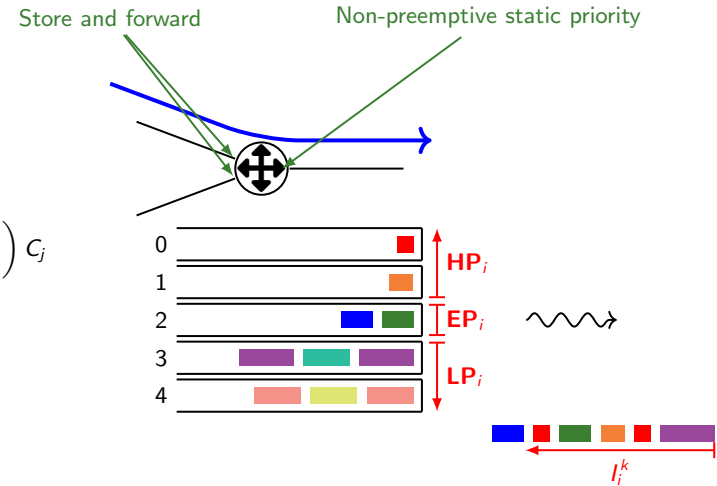
Presentation of **Response-Time Analysis (RTA)** in Switched Networks



Response-Time Analysis (RTA) in Switched Networks

Bound on blocking time with RTA:

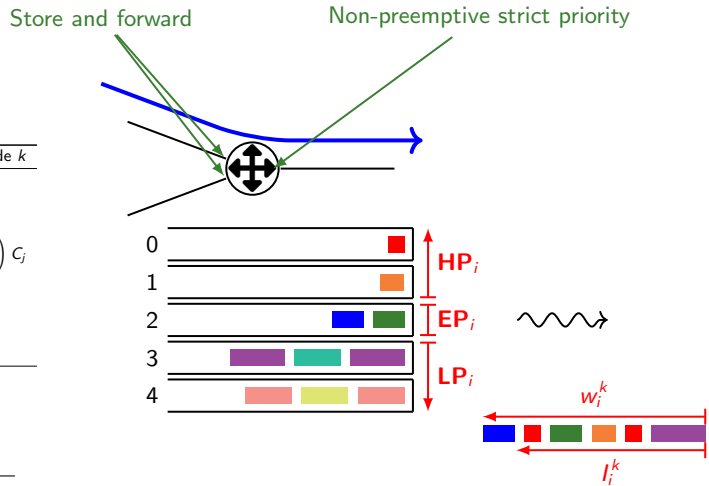
$$I_i^k = \max_{m \in \mathbf{LP}_i} C_m + \sum_{j \in \mathbf{EP}_i \cup \mathbf{HP}_i} \left(\left\lfloor \frac{I_i^k}{T_j} \right\rfloor + 1 \right) C_j$$



Response-Time Analysis (RTA) in Switched Networks

Algorithm RTA induction for the delay bound of VL i at node k

1: **procedure** RTA_DelayBoundAtNode(k, i)
2: $\quad I_i^{k,0} \leftarrow 0$
3: $\quad$ **repeat**
4: $\quad\quad I_i^{k,n+1} \leftarrow \max_{m \in \mathbf{LP}_i} C_m + \sum_{j \in \mathbf{EP}_i \cup \mathbf{HP}_i} \left(\left\lfloor \frac{I_i^{k,n}}{T_j} \right\rfloor + 1 \right) C_j$
5: $\quad$ **until** $I_i^{k,n+1} = I_i^{k,n}$
6: $\quad w_i^k \leftarrow I_i^{k,n} + C_i$
7: $\quad$ **return** w_i^k
8: **end procedure**

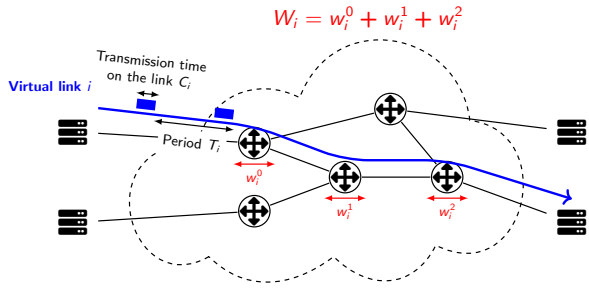


VL : Virtual Link

Response-Time Analysis (RTA) in Switched Networks

Algorithm RTA **end-to-end** delay bound of VL i

1: **procedure** RTA_EndToEndDelayBound(i)
2: $W_i \leftarrow 0$
3: **for** hop k in path of VL i **do**
4: $w_i^k \leftarrow$ RTA_DelayBoundAtNode(k, i)
5: $W_i \leftarrow W_i + w_i^k$
6: **end for**
7: **return** W^i
8: **end procedure**



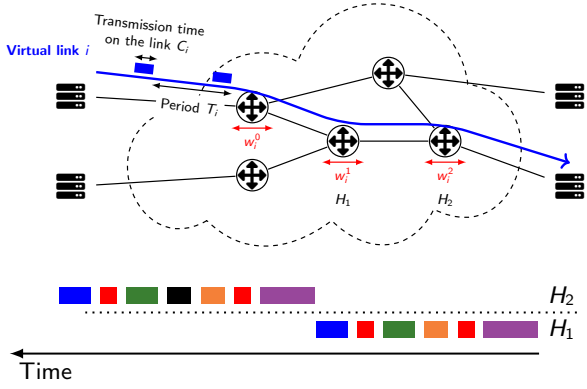
VL : Virtual Link

Pessimism of Response-Time Analysis (RTA)

Source of pessimism

Does not capture the serialisation

$$W_i = w_i^0 + w_i^1 + w_i^2$$



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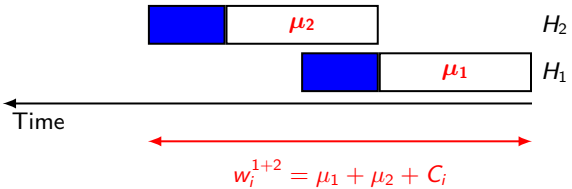
8: **end procedure**

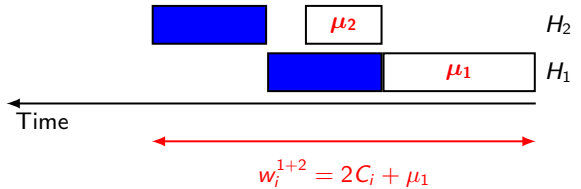
VL : Virtual Link

Blocking-Waived Estimation (BWE): Reduce the Pessimism of RTA

Case $\mu_2 \geq C_i$



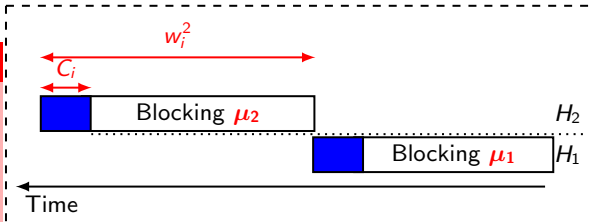
Case $\mu_2 \leq C_i$



Generalisation:
$w_i^{1+2} = \max(\mu_1 + \mu_2, w_i^1) + C_i$

BWE end-to-end delay bound for VL *i*

$$w_i^{1+\cdots+k+1} = \max\left(w_i^{1+\cdots+k}, \sum_{0 \leq m \leq k+1} \mu_m\right) + C_i$$



VL : Virtual link

RTA: Response-time analysis

Blocking-Waived Estimation: Reduce the Pessimism of RTA

Algorithm BWE **end-to-end** delay bound of VL i

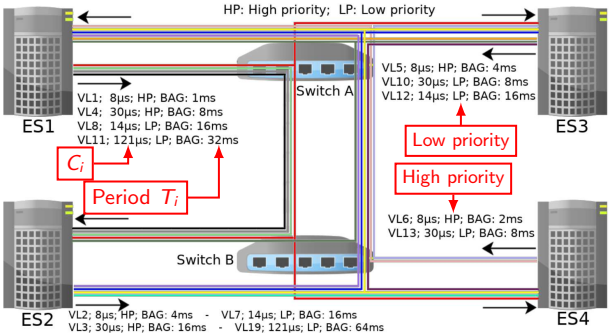
```
1: procedure BWE_EndToEndDelayBound(i)
3:     for hop k in path of VL i do
4:         w_i^k ← RTA_DelayBoundAtNode(k, i)
6:     end for
7:     W_i ← BWE_Blocking_Analysis([w_i^k]_{k∈[0,n]})
8:     return W^i
9: end procedure
```

Algorithm BWE blocking computation for VL i

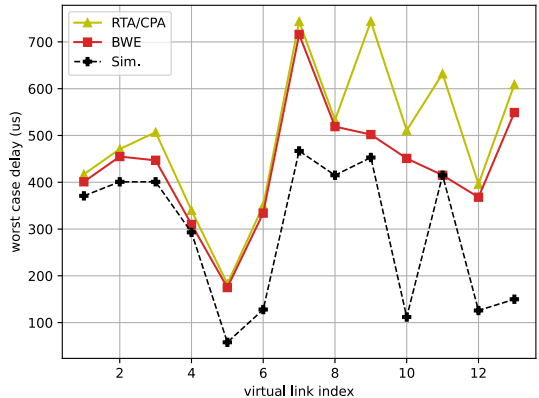
```
1: procedure BWE_Blocking_Analysis([w_i^k]_{k∈[0,n]}, C_i)
2:     β ← [...]_{k∈[1,n]}                ▷ β[k] = Σ_{m≤k} μ_m
3:     current_sum ← 0
4:     for k ∈ [0, n] do
5:         μ_k ← w_i^k − C_i
6:         current_sum = current_sum +μ_k
7:         β[k] ← current_sum
8:     end for
9:     for k ∈ [0, n] do
10:        if k = 0 then
11:            W_i ← C_i + w_i^k
12:        else
13:            W_i ← C_i + max(W_i, β[k])
14:        end if
15:    end for
16:    return W_i
17: end procedure
```

VL : Virtual Link

Comparison of the Approaches on an Industrial Use-Case



AFDX use-case from [Rox, Ernst 2010]
13 virtual links, 2 priority levels, 2 switches

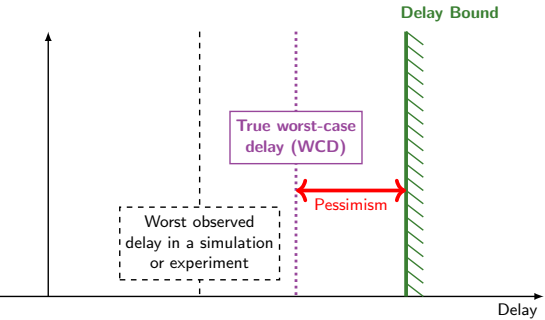


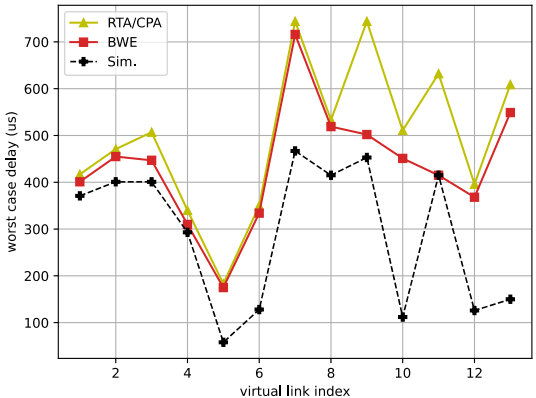
End-to-end delay bound per virtual link

VL: Virtual link (flow) BAG: Bandwidth Allocation Gap (minimum period) ADFX: Avionics Full-duplex Ethernet

– [Rox, Ernst 2010] Jonas Rox and Rolf Ernst [Apr. 2010]. "Formal Timing Analysis of Full Duplex Switched Based Ethernet Network Architectures". In: *SAE Technical Paper Series*. https://doi.org/10.4271/2010-01-0455. SAE International. DOI: 10.4271/2010-01-0455

Comparison of the Approaches on an Industrial Use-Case





End-to-end delay bound per virtual link

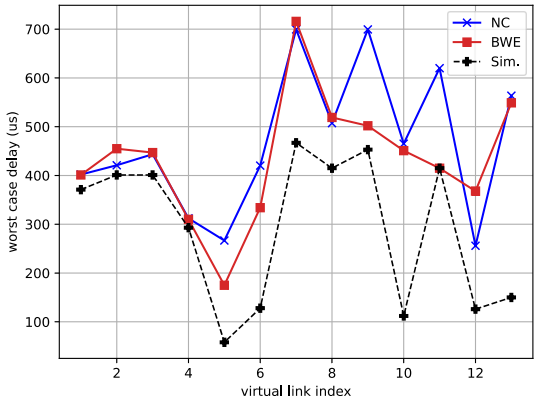
Key takeaway

Significant reduction of the pessimism with respect to RTA (response-time analysis)

Comparison of the Approaches on an Industrial Use-Case

Key takeaway

Comparable, sometimes better performances with respect to network calculus [Tsai, *et al.* 2023]



End-to-end delay bound per virtual link

BWE: Blocking-waived estimation

NC: Network calculus

– [Tsai, *et al.* 2023] Chun-Tso Tsai, Seyed Mohammadhossein Tabatabaee, Stéphan Plassart, and Jean-Yves Le Boudec [2023]. *Saihu: A Common Interface of Worst-Case Delay Analysis Tools for Time-Sensitive Networks.* https://github.com/adfeel220/Saihu-TSN-Analysis-Tool-Integration. arXiv: 2303.14565 [cs.NI]

Conclusion

Blocking-Waived Estimation (BWE) reduces the pessimism of RTA (response-time analysis) by taking into account the **serialisation effect** and by analysing the intrications between **blocking time** of concurrent flows and the **transmission time** of the flow of interest.

Tested on an industrial use-case, BWE reveals:

- A significant reduction of the delay-bound pessimism (estimated by simulation) with respect to RTA.
- Comparable performances with respect to network calculus.

Perspectives include:

- To evaluate the performance of BWE with respect to other approaches on **broader use-cases**.
- To compare the **time complexity** of BWE with respect to other approaches.
- To use BWE on **other scheduling policies**, e.g., the TSN credit-based shaper.

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Bibliography I

[Bouillard, Boyer, Le Corronc 2018] Bouillard, Anne, Marc Boyer, and Euriell Le Corronc (Oct. 2018). *Deterministic Network Calculus*. https://doi.org/10.1002/9781119440284. John Wiley & Sons, Inc. DOI: 10.1002/9781119440284.

[Rox, Ernst 2010] Rox, Jonas and Rolf Ernst (Apr. 2010). "Formal Timing Analysis of Full Duplex Switched Based Ethernet Network Architectures". In: *SAE Technical Paper Series*. https://doi.org/10.4271/2010-01-0455. SAE International. DOI: 10.4271/2010-01-0455.

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