Ludovic Provost

Computer Engineering

Tel.: 418-717-4030
Github: https://github.com/LudoProvost
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Skills

- **Languages**: Python, C++, C, C, Java, SQL, R, VHDL, Verilog, Rust, Bash
- **Tools**: Linux (Ubuntu/Debian/Arch), Quartus, Matlab, Jira, Jenkins, Fusion360, KiCad, Wireshark, Logic2
- **General skills**: teamwork, communication, organization, resourceful

Education

University of Ottawa, BASc. Computer Engineering **September 2020 – May 2025**

- CGPA : **94.4%**
- Part of the Dean's Honor List for 8 semesters
- 8 Merit scholarships

Experiences

I.T. Technician **May 2021 – November 2021**
Élections Québec

- Repair and maintenance of computer equipment (HDD, CPU, etc.)
- Imaging and set up laptops for new employee onboarding
- Customer service using Cisco Finesse, MS Teams
- Frequent use of Azure AD and SCCM

Application Support Intern **May 2022 – August 2022**
Brookfield Renewable Partners L.P.

- Used PL/SQL scripts to recover information in the company's database
- Offered support for company applications

CI/CD Software developer intern **September 2022 – December 2022**
Intact Financial Corporation

- Documented code, processes, and permissions in accordance with company standards
- Implemented automated tasks, automated tests, and a failure alert system
- Maintenance on pipelines, services, the company's website and its tools
- Migrated services from Log4j to Logback

Projects

Embedded & Electronics | C, UART, SPI, I2C

- Writing drivers for EEPROM and sensor ICs using datasheets and register maps
- Debugging and testing using power supply, logic analyzer and port reader
- Design of PCBs and schematics using KiCad and Fusion360

Software & Algorithms| Python, TCP, Rust, C, UEFI

- Real-time signal processing and use of multi-threading for a beat detection algorithm
- Completed many PicoCTF challenges since 2021 using various Linux distros
- Writing a custom bootloader and OS using C and the UEFI specifications

School Projects | FPGA, VHDL, Verilog, ModelSim, Quartus, Vivado

- Design of a single-cycle and a 5-stage pipelined MIPS processor in VHDL
- Design of a UART in structural VHDL for a traffic light controller

Note: More projects are on display on my Github & website.