ELEN 422 Lab #6 – Ripple Carry Adder

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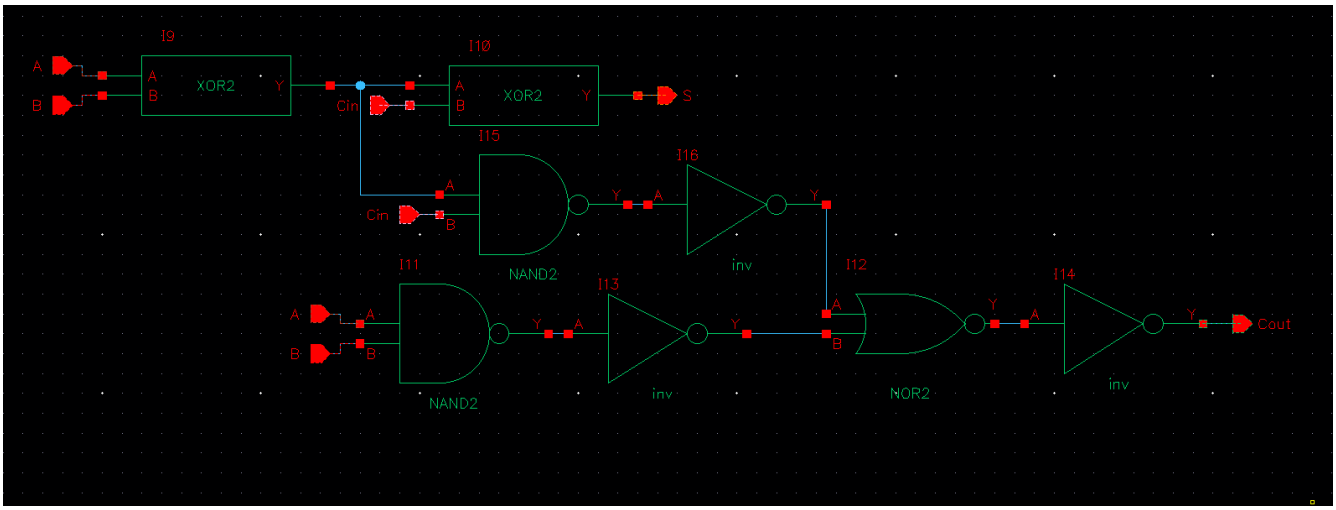
Procedure:

The purpose of this lab was to design a 2-bit CMOS ripple carry adder. The process involved creating a 1-bit full adder circuit as a building block. A schematic, symbol, layout, and simulation results were obtained for both the 1-bit and 2-bit configurations. The 2-bit adder was constructed by connecting the Cout of the first adder to the Cin of the second adder. This design demonstrates the principles of cascading adders to achieve larger bit-width adders.

1-bit Full Adder

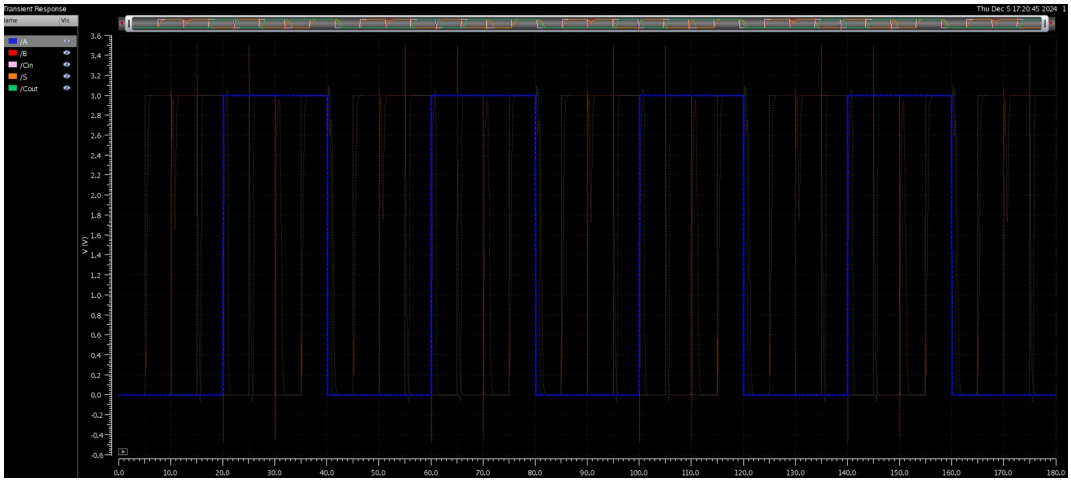
Schematic:



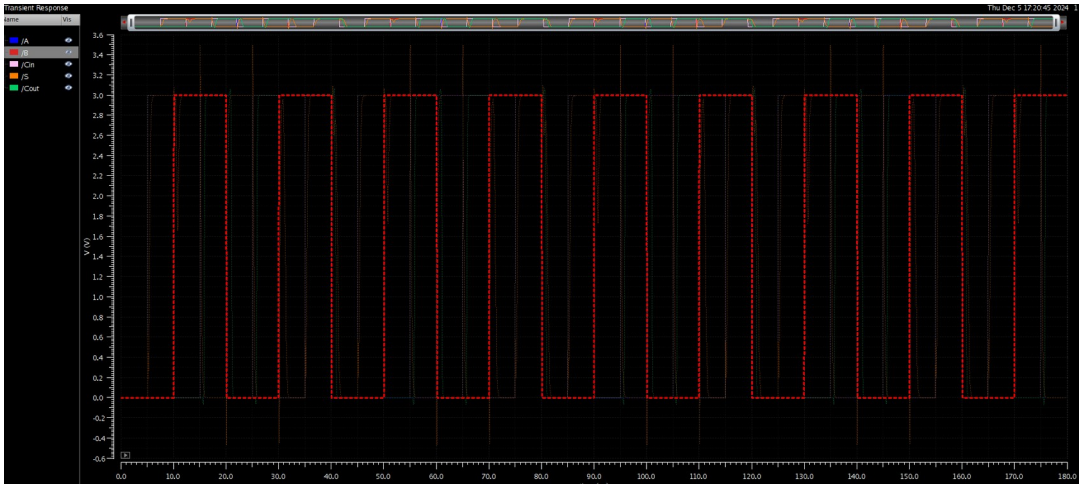
An XOR2 gate was also constructed to aid in the process. Also, instead of creating an AND and OR gate, inverters are used after the NAND and NOR gates. With the schematic created, it can be simulated.

Inputs: The inputs correspond to the 1-bit Full Adder truth table

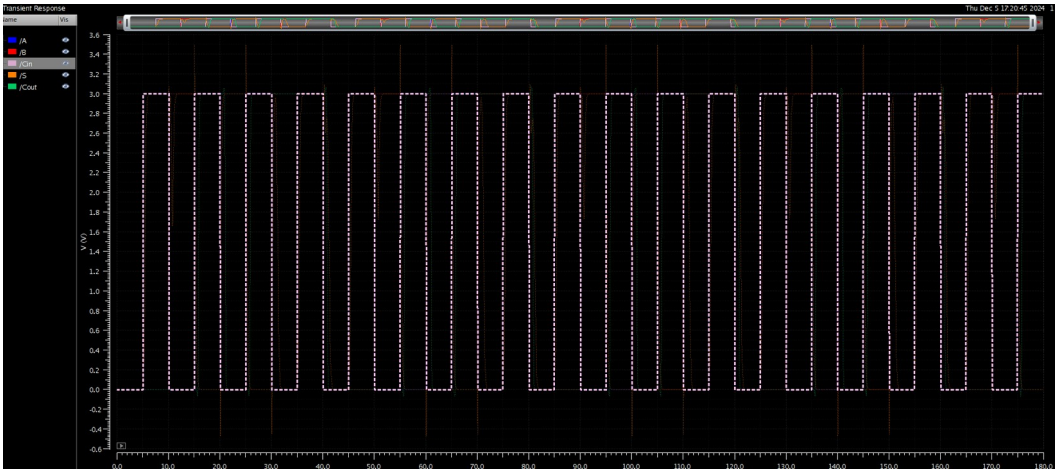
A



B

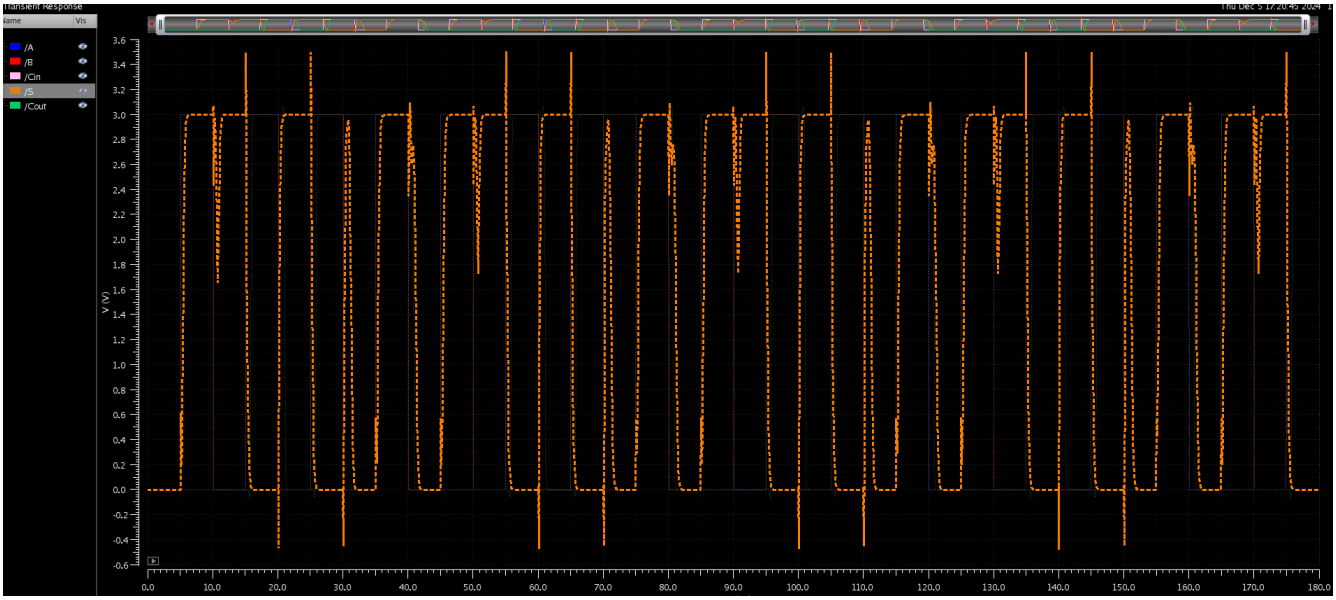


Cin

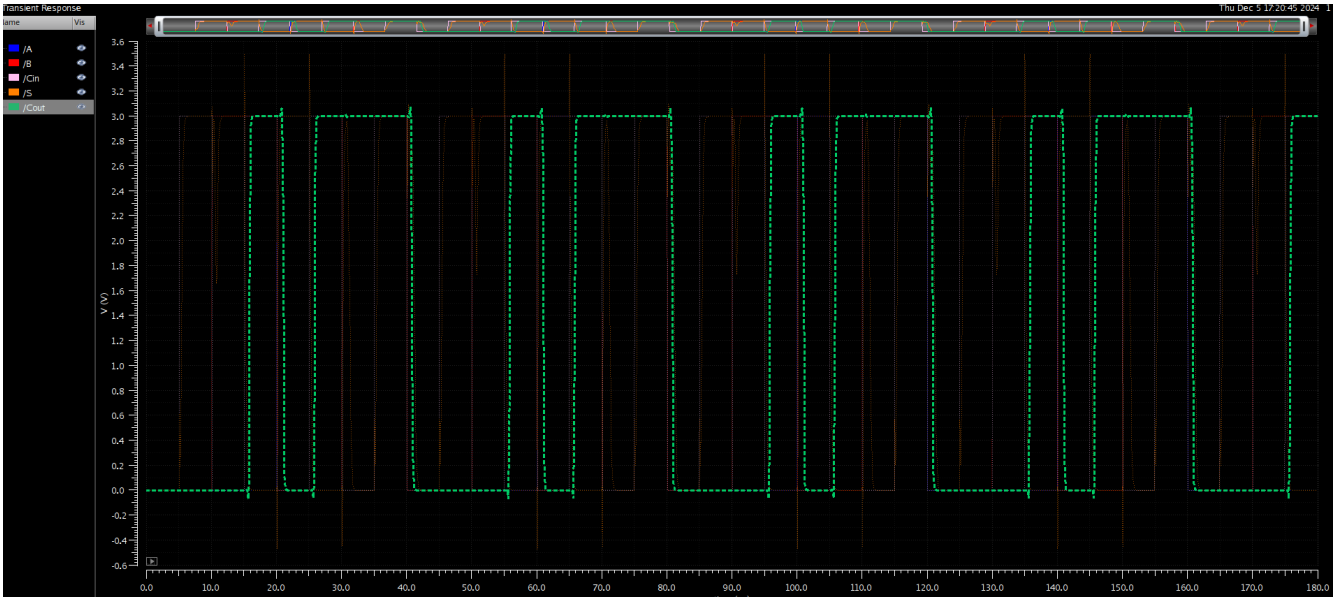


Outputs:

S



Cout

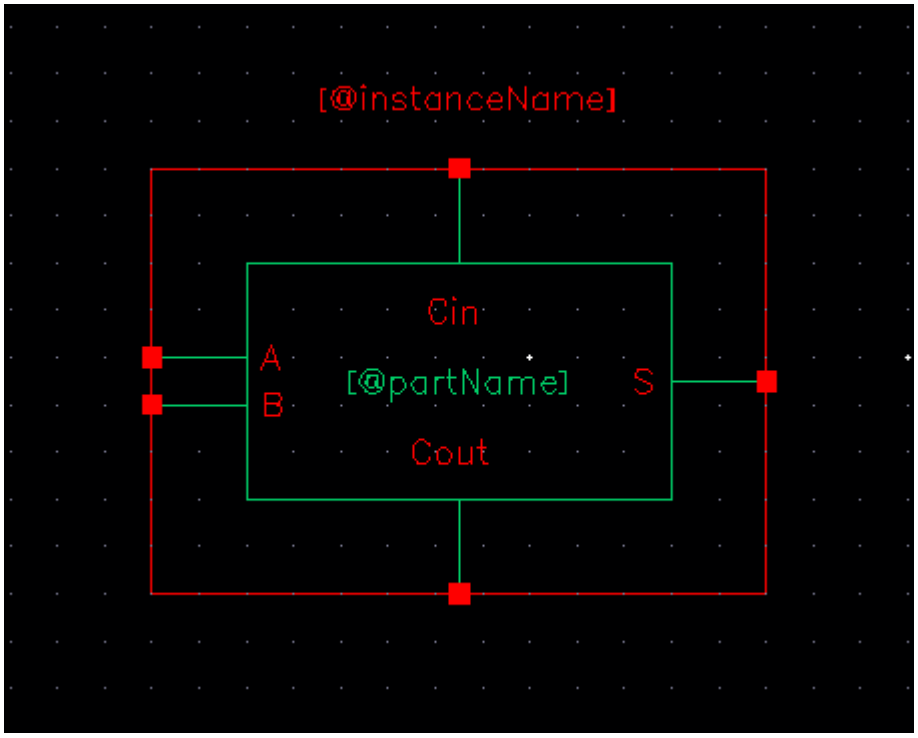


The outputs match the expected truth table.

With the schematic simulated, the symbol and layout can be created.

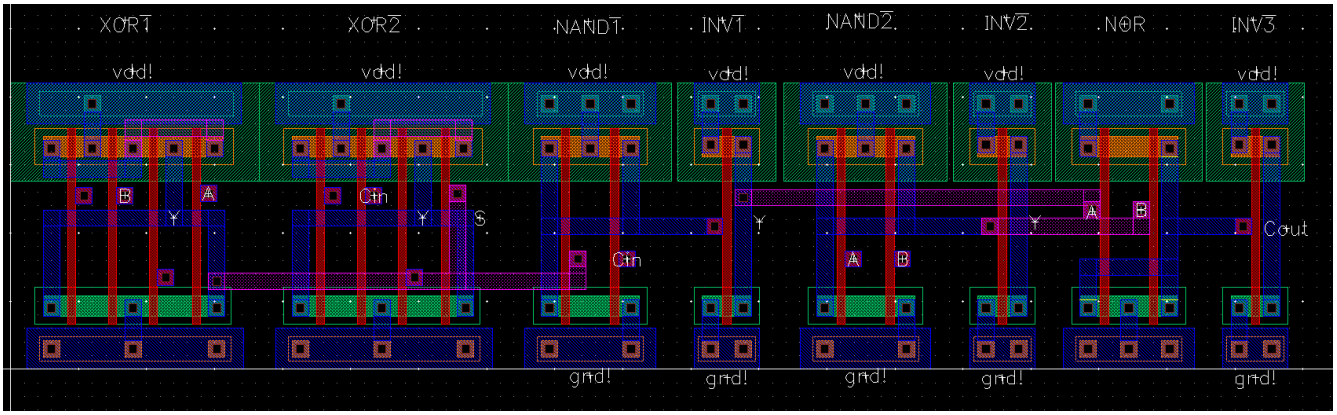
Symbol:

The symbol closely resembles that of a typical 1-bit adder symbol.



The symbol closely resembles that of a typical 1-bit adder symbol.

Layout:

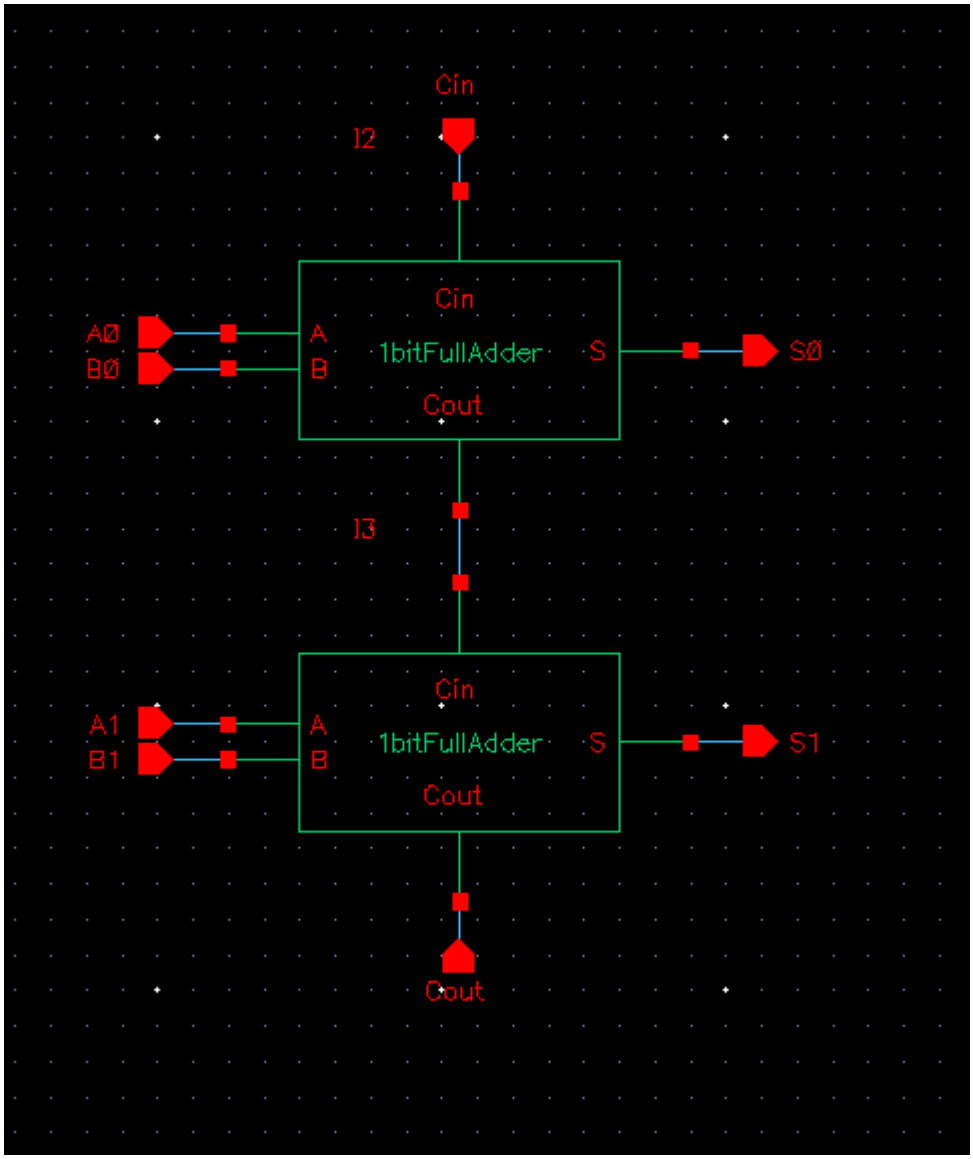


In the layout, each gate is labeled. The connections are exact to the specifications of the schematic.

With the 1-bit Full Adder completed, the 2-bit Full Adder can be created.

2-bit Full Adder

Schematic:

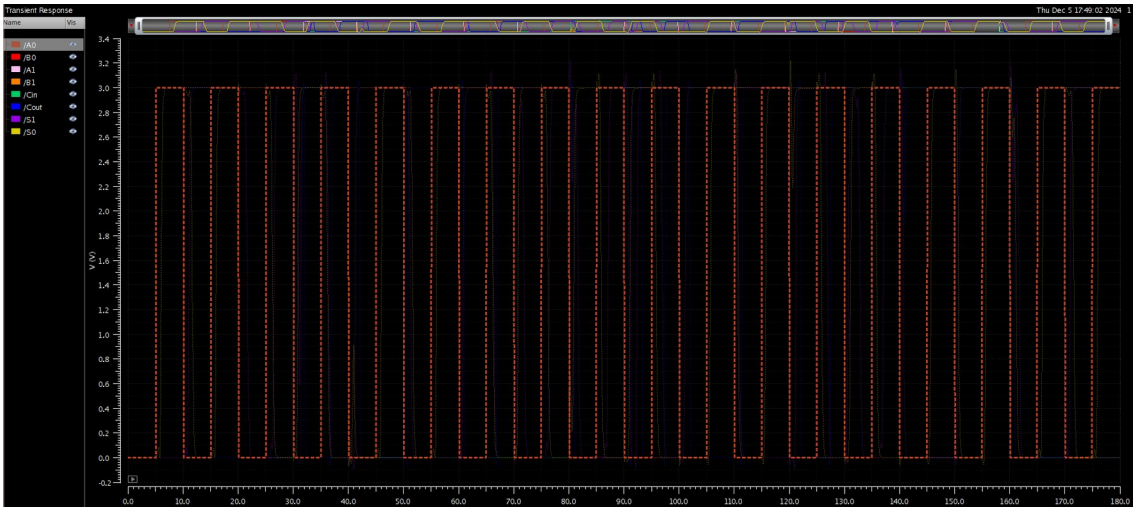


Creating the 2-bit adder is as simple as connecting the Cout of the first adder to Cin of the second adder.

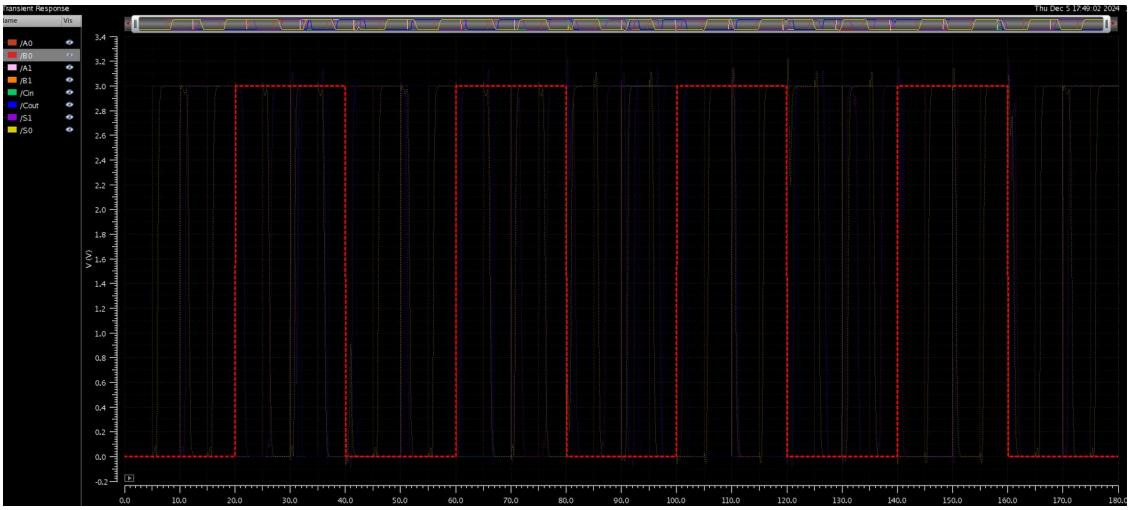
With the schematic created, the simulation can be done.

Inputs:

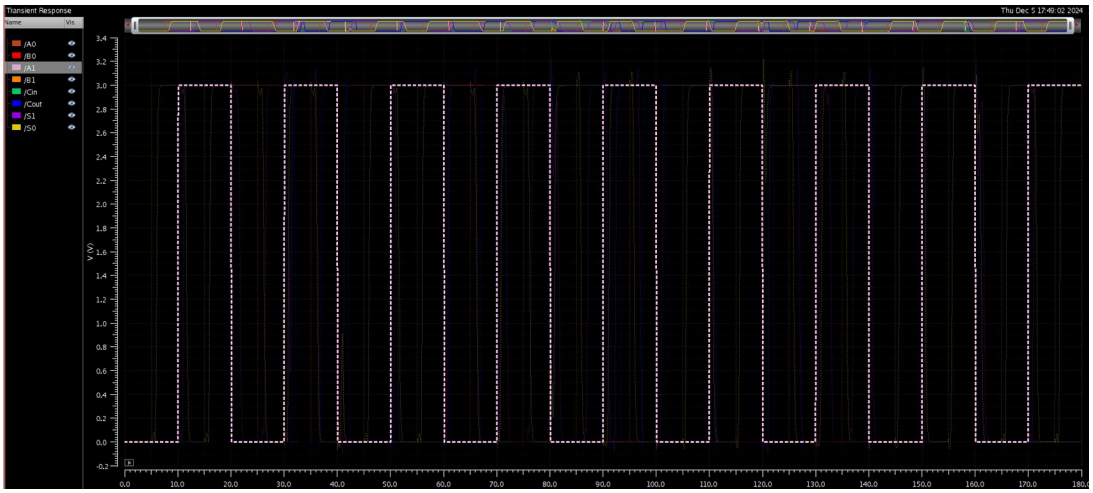
A0



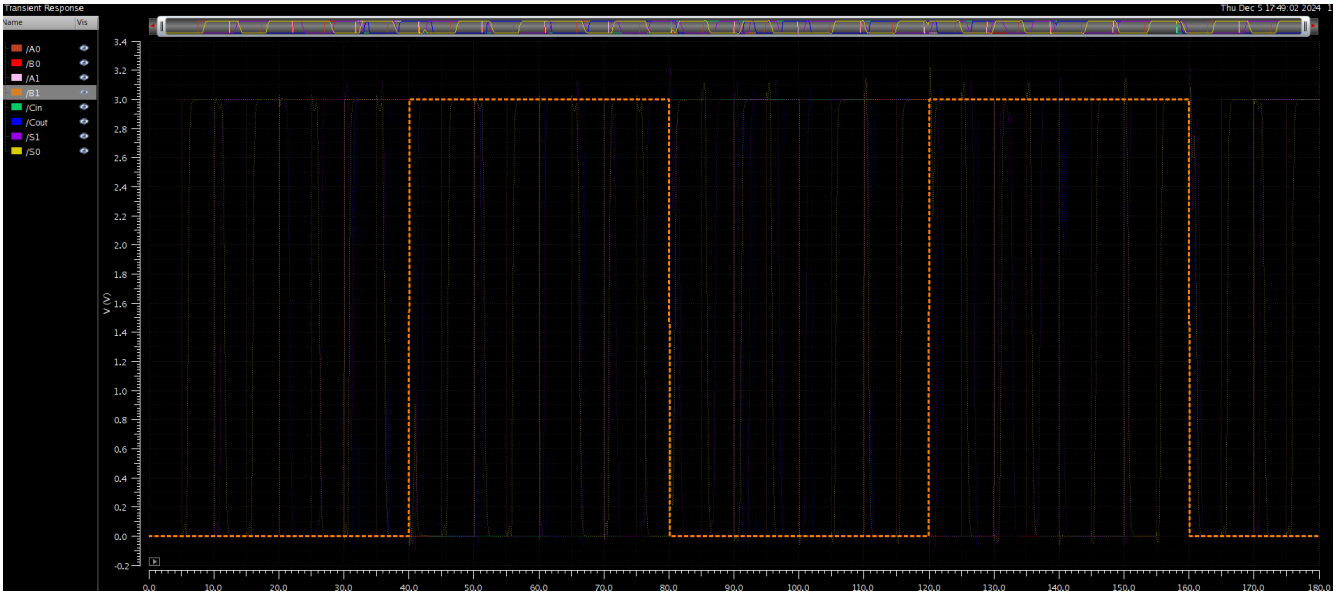
B0



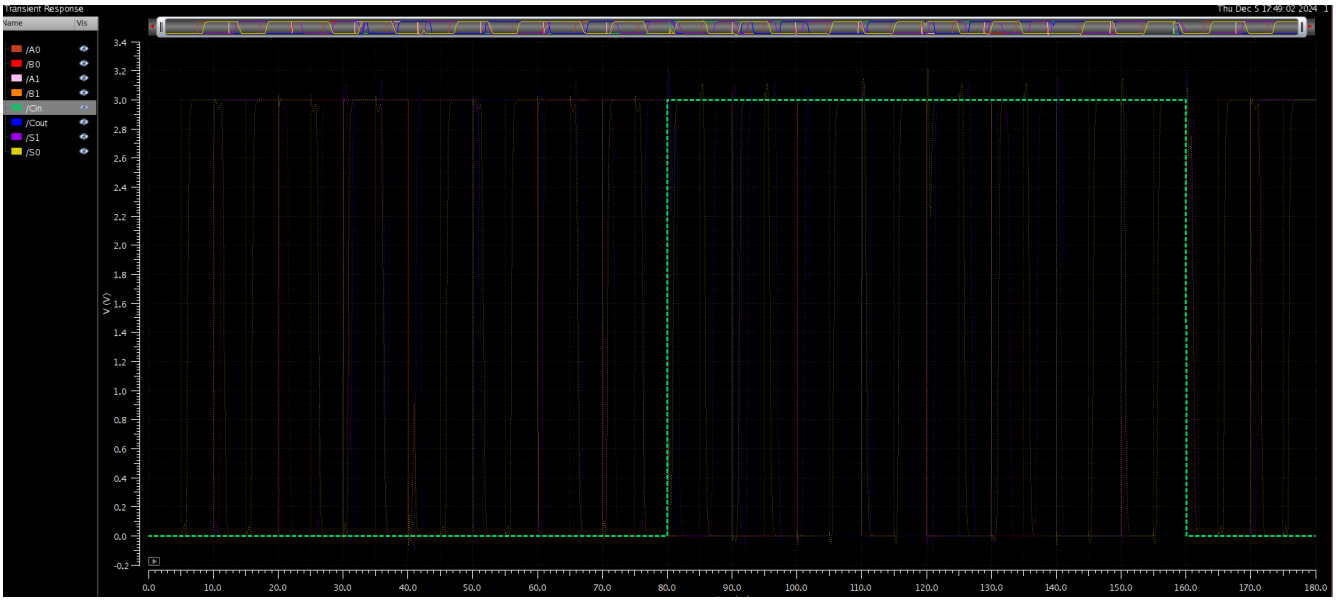
A1



B1

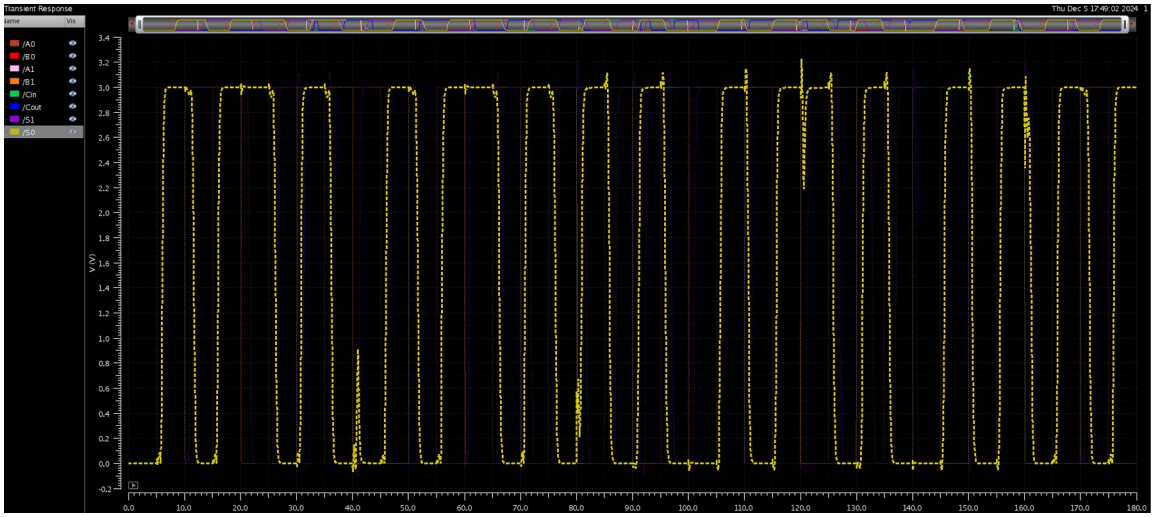

Transient Response
Thu Dec 5 17:49:02 2024
Name
Vis
/A0
/B0
/A1
/B1
/Cin
/Cout
/S1
/S0
V (V)
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0

Cin

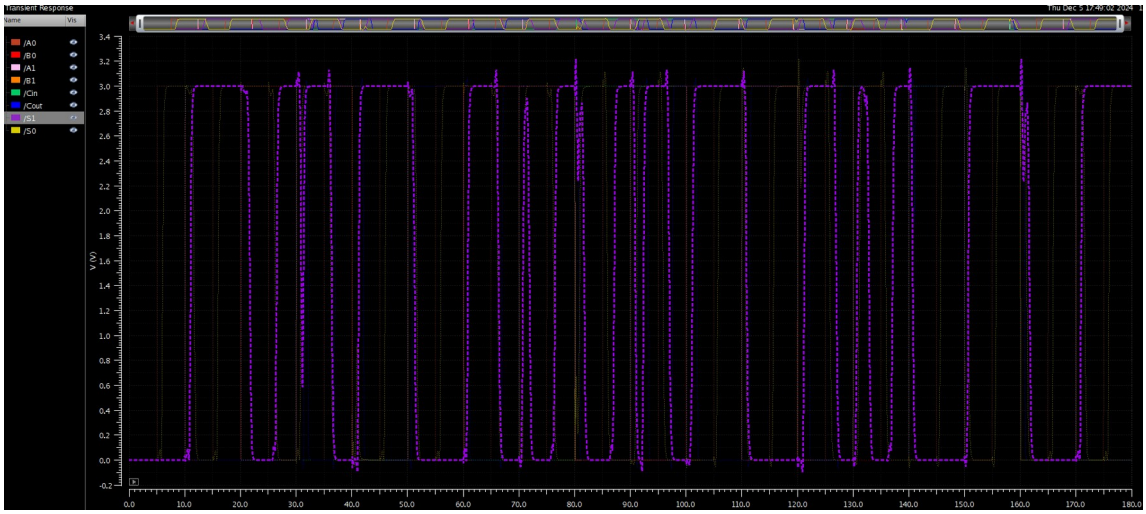

Transient Response
Thu Dec 5 17:49:02 2024
Name
Vis
/A0
/B0
/A1
/B1
/Cin
/Cout
/S1
/S0
V (V)
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0

Outputs:

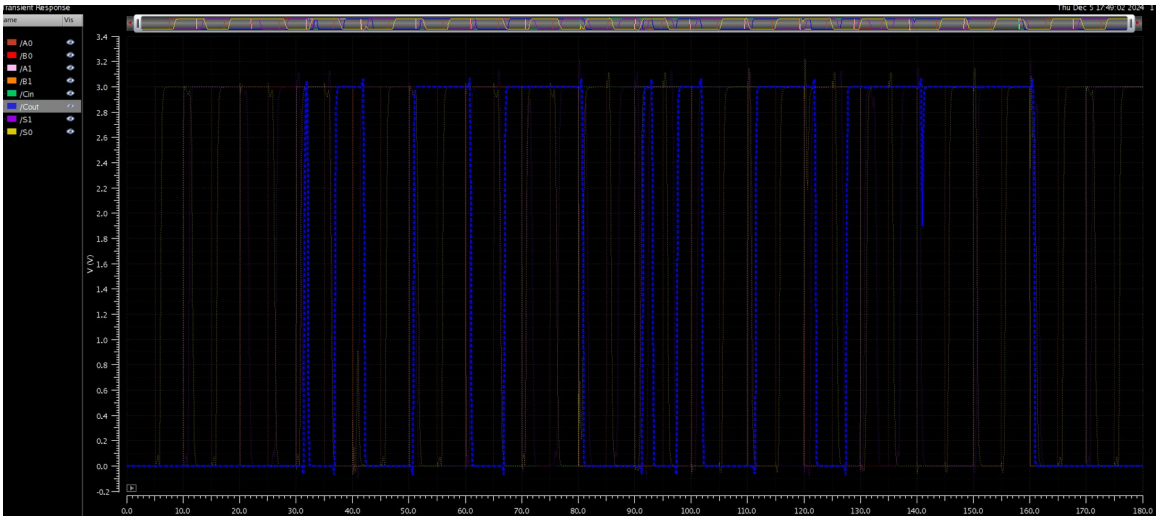
S0



S1

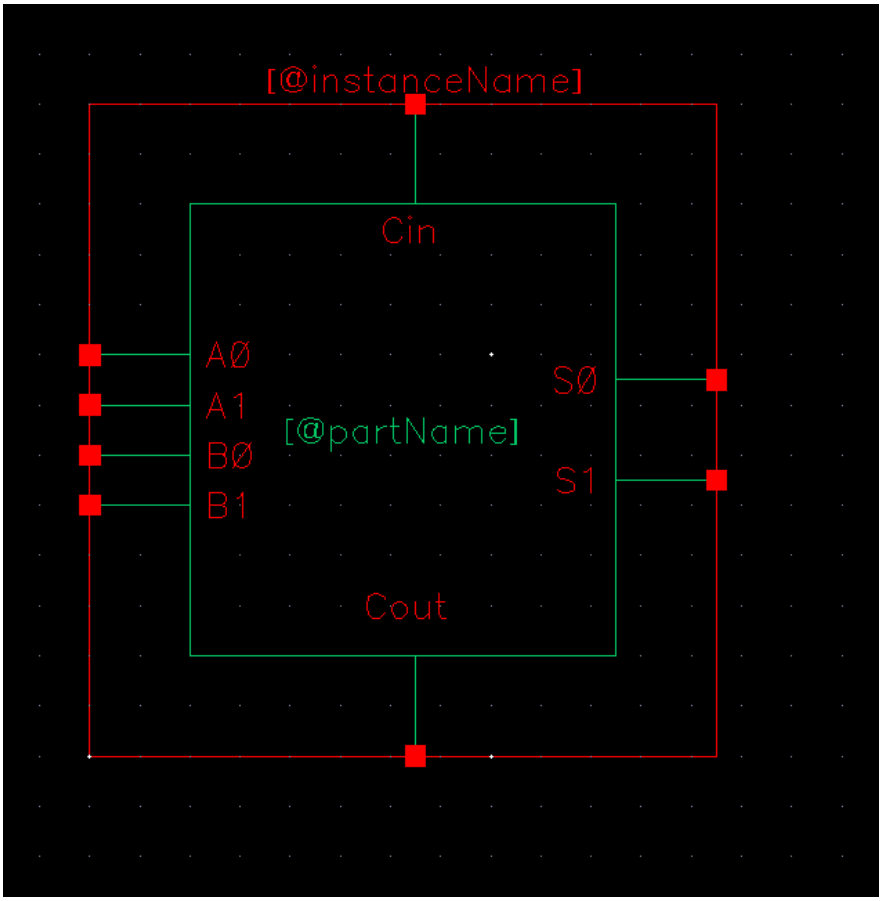


Cout

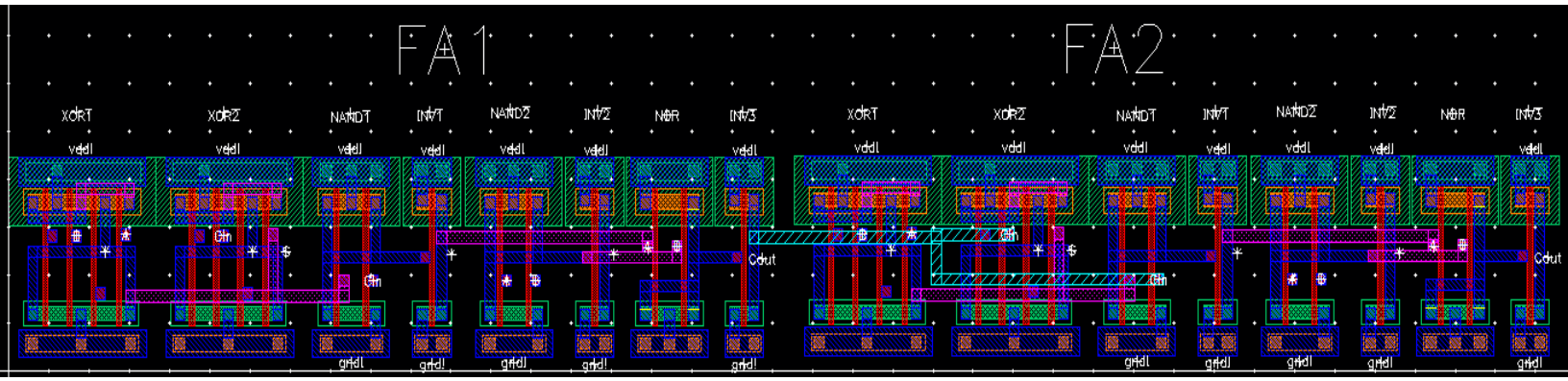


With the schematic simulations returning as expected, the symbol and layout can be drawn.

Symbol:



Layout:



The layout is extremely difficult to see on paper, so all screenshots will also be submitted with the report.

Observation

The 2-bit full adder seems simple from a gate level design, however when designing a CMOS 2-bit ripple carry adder, the layout becomes extremely complicated very quickly.

Conclusion

This lab demonstrated the design, simulation, and layout of a CMOS based 2-bit ripple carry adder. Despite challenges in the layout phase, the process reinforced the importance of modular design and accurate schematic representation. Similar to previous labs, licensing issues prevented verification of the layouts, but careful adherence to design principles suggests the layout is error-free.