DINFOX SYSTEM

TECHNICAL DESCRIPTION

DIN rail modules for power management

Local control and monitoring by HMI or serial link

Remote control and monitoring by long range radio

Revision history

Doc	Date	Author(s) / Reviewer(s)	Description
td1.0	2025/06/07	Ludovic Lesur	*Initial version.*
td1.1	2025/07/20	Ludovic Lesur	*Add RS485-BRIDGE board in nodes list.* *Add `CVF` registers and flag on BPSM and BCM nodes.* *Add shunt resistor field in FLAGS_1 register of BCM node.*
td1.2	2025/10/20	Ludovic Lesur	*Change temperature representation unit to tenth of Celsius degrees.*

Version compatibility table

Doc	una-lib	una-at	una-r4s8cr	lmac-driver	dinfox-registers	dmm	dsm
td1.0	sw2.2	≥ sw5.0	≥ sw1.0	≥ sw3.0	sw2.0	sw6.4 ▶ sw6.5	sw7.3
td1.1	sw3.0 ▶ sw3.1	≥ sw5.0	≥ sw1.0	≥ sw3.0	sw3.1	sw6.6 ▶ sw6.9	sw7.7 ▶ sw7.12
td1.2	≥ sw4.0	≥ sw5.0	≥ sw1.0	≥ sw3.0	≥ sw4.0	≥ sw6.10	≥ sw7.13

Contents

1 Global architecture

1.1 Introduction

The main goal of the DINFox project is to design a scalable power system in order to control and monitor any kind of power supply (AC line, solar panel, backup, regulators, relays, etc.).

This main idea can be split in several objectives:

- Design a **single module for a given function** (1 board for 1 relay for instance) and use a **common physical bus** to perform the communication between boards. Thanks to this modular approach, each DINFox system can be composed of a custom group of nodes according to the required features.
- Provide a mechanical design in such a way that the boards can be fixed to a DIN rail and can be stacked together without additional wiring.
- Define a **unified interface** to access all nodes in order to manage a **single API for local control and monitoring**.
- Achieve the **minimum power consumption** to be able to monitor backup sources such as battery powered systems.

1.2 Functional description

A DINFox system consists of several DIN rail modules, called **nodes**, physically connected through an RS485 bus. The general behavior of the system is controlled by one **master** module which is the master of the RS485 bus. All other nodes are **slaves**, they are continuously listening on the bus to wait for commands.

The DINFox system is a concrete implementation of the **Unified Node Access (UNA)** framework: all nodes of the bus are controlled through a set of registers regardless of the physical interface.

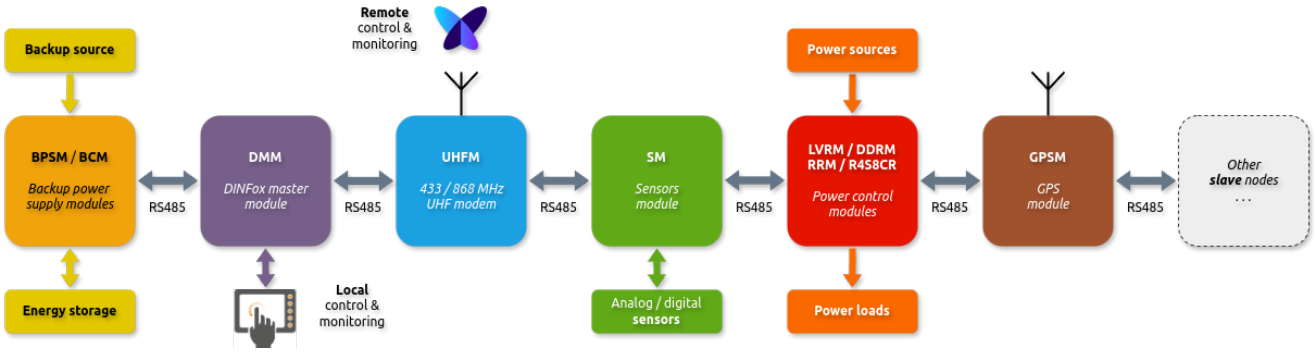

Figure 1: *Functional architecture of a DINFox system.*

2 Node identification

2.1 Node types

There are two categories of nodes:

- **DINFox nodes**: boards that were specifically designed for this project.
- **External nodes**: existing products with RS485 interface which can be managed on the same bus.

2.2 Node address (NODE_ADDR)

Since all the boards of a DINFox system are connected through an RS485 bus, each node must have a unique address.

DINFox nodes are based on the STM32L0 and STM32G4 families from ST-Microelectronics. The LPUART peripheral of these MCUs features a wake-up capability from stop mode where address recognition is performed by hardware. This is very suited to optimize the node power consumption, since the core will be woken-up only if a command was sent to its address. But this feature requires the most significant bit to be set, so that the usable address range is on the 7 lower bits.

As a consequence, each node attached to a DINFox bus has a **unique 7 bits address** (NODE_ADDR). All address values between **0x00** and **0x7E** are allowed, **0x7F** being used by the LMAC protocol (see section **3.4.1**).

By convention, the address **0x00** is reserved for the master node.

2.2.1 DINFox nodes

Even if there is no constraint on the address mapping for the slave nodes, some values and ranges have been assigned to each node type to facilitate address management when flashing the boards (see table **1**).

2.2.2 External nodes

2.2.2.1 KMTronic R4S8CR

The R4S8CR is a relay box manufactured by KMTronic. It is identified by **4 bits ID**, configurable with DIP switches. In order to be compatible with the DINFox system, a 7 bits address has been assigned accordingly: the **0x70 − 0x7E** address range has been reserved for this product, where the 4 lower bits of the address correspond to (relay box ID − 1). For example, the relay box configured with ID 13 has the 0x7C address assigned.

This address is virtual from a physical point of view: it is only known by the high level layers to identify the node in the system, but is not used in the physical layer.

2.3 Board identifier (BOARD_ID)

As part of the UNA framework, each distinct hardware module has a **unique 8 bits board identifier** (BOARD_ID). This value is used by the master to enumerate dynamically the slave nodes attached to the bus and their specific features (function, capabilities, set of registers, input controls, output data, radio messages format, etc.).

On a given DINFox system, each node must have a unique address, but several nodes can have the same BOARD_ID: for example, 3 independent relays will have 3 different addresses but the same board identifier, since this is the same module from an hardware point of view.

The board identifiers have been assigned in chronological order during hardware design. They are defined in the **UNA library** which is available on GitHub: https://github.com/Ludovic-Lesur/una-lib.

2.4 Nodes list

The table below shows the list of nodes which are currently supported by the DINFox system. DINFox nodes are marked in green whereas external nodes are in orange.

BOARD_ID	Node	Description	Width	Input controls	Output data	NODE_ADDR
0x00	LVRM	Low voltage relay module	3U	Relay state	Relay state, V_{COM}, V_{OUT}, I_{OUT}, V_{MCU}, T_{MCU}	0x20 – 0x27
0x01	BPSM	Backup power supply module	3U	Charge enable, backup enable	Charge enabled, Charge status, backup enabled, V_{SRC}, V_{STR}, V_{BKP}, V_{MCU}, T_{MCU}	0x02
0x02	DDRM	DC-DC converter module	3U	DC-DC state	DC-DC state, V_{IN}, V_{OUT}, I_{OUT}, V_{MCU}, T_{MCU}	0x28 – 0x2F
0x03	UHFM	433 / 868 MHz UHF modem	4U	Radio TX / RX commands	Radio RX data, V_{RF}, V_{MCU}, T_{MCU}	0x03
0x04	GPSM	GPS module	3U	Geo-location / time commands	Geo-location, time, V_{ANT}, V_{GPS}, V_{MCU}, T_{MCU}	0x04
0x05	SM	Sensors module	3U	Digital outputs state	Digital and analog inputs state, T_{AMB}, H_{AMB}, V_{MCU}, T_{MCU}, external sensors data	0x05
0x06	RS485 – BRIDGE	RS485 to UART / USB interface	2U	–	–	0x01
0x07	RRM	Rectifier and regulator module	3U	Regulator state	V_{IN}, V_{OUT}, I_{OUT}, V_{MCU}, T_{MCU}	0x30 – 0x37
0x08	DMM	DINFox master module	4U	–	Number of nodes, V_{USB}, V_{HMI}, V_{RS}, V_{MCU}, T_{MCU}	0x00
0x09	MPMCM	Mains power monitoring and controller module	5U	–	V_{MAIN}, P_{MAINx}, V_{MCU}, T_{MCU}	0x06
0x0A	R4S8CR	Relay box from KMTronic	–	Relays state	Relays state	0x70 – 0x7E
0x0B	BCM	Battery charger module	4U	Charge enable, backup enable	Charge enabled, Charge status, backup enabled, V_{SRC}, V_{STR}, I_{STR}, V_{BKP}, V_{MCU}, T_{MCU}	0x07

Table 1: *DINFox system nodes list.*

3 Bus description

3.1 OSI model

The figure below shows the OSI model implementation of the DINFox bus. There are 3 main groups of layers:

- On a hardware point of view, all the nodes are **physically connected on a shared RS485 bus**.
- Then, the data link, network and transport layers are **specific to the board**: DINFox nodes use the UART, LMAC and UNA-AT protocols, whereas external nodes have custom interfaces imposed by the product manufacturer.
- Finally, the application layer **unifies the node access methods** by using 32-bits software registers regardless of the lower layers, as specified in the UNA framework.

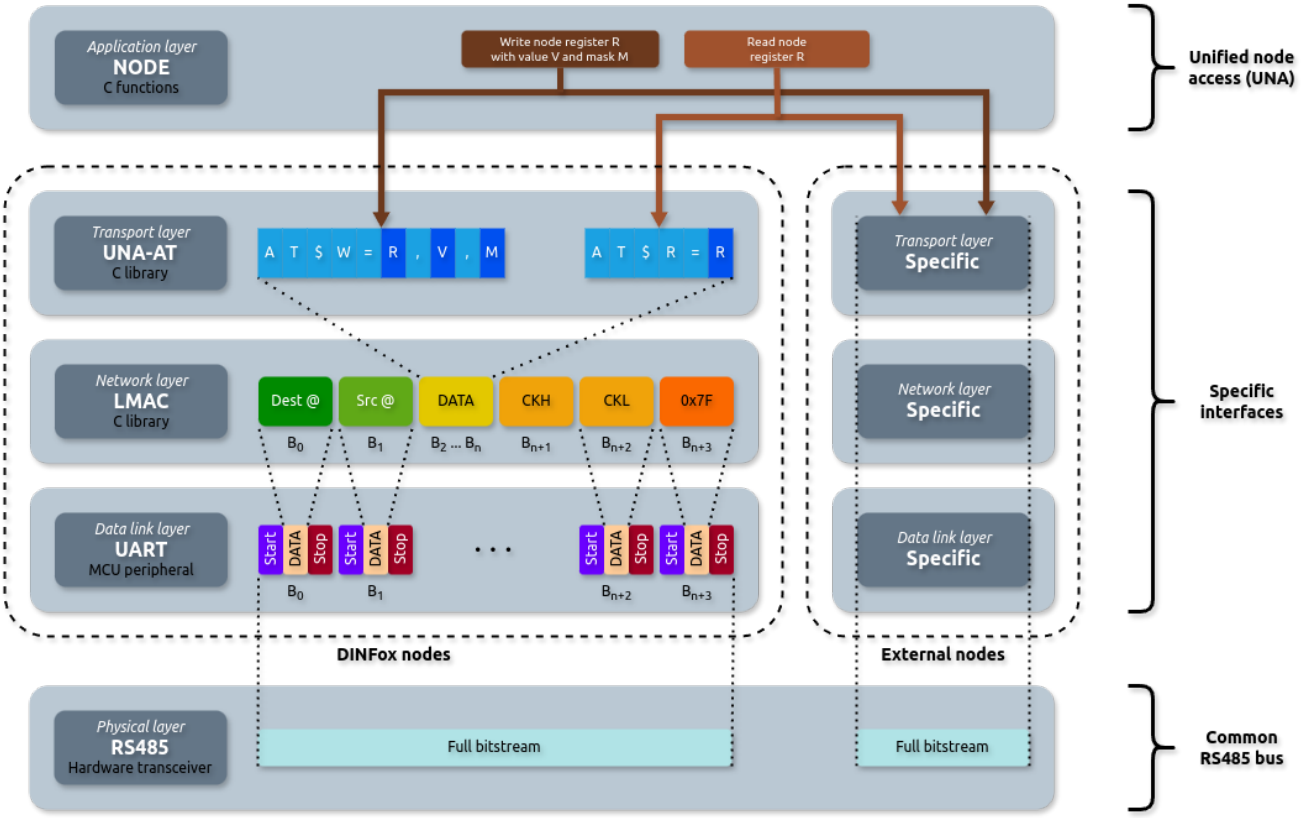

Figure 2: *OSI model of the DINFox bus.*

3.2 Physical layer (RS485)

All the nodes of a DINFox system are **physically connected on a shared RS485 bus** composed of 2 differential signals (named A and B).

Parameter	Value
Differential voltage	$3.0\,V$
Data rate	Node-dependent (see section **3.3**)

Table 2: *RS485 parameters.*

3.2.1 DINFox nodes

To reach a very low power consumption, DINFox nodes are based on the MAX3471 transceiver from Maxim Integrated, which is always powered by a $3.0\,V$ voltage regulator. This is the reason why the differential voltage of the RS485 is fixed to $3.0\,V$ as mentioned before.

Additionally, DINFox nodes use a 4 wires link composed of a common power supply rail (V_{RS}), the ground (GND) and the two signals of the RS485 differential pair (A and B). These signals are grouped on a 4 pins connector on both edges of the PCB, so that multiple nodes can be **stacked on a DIN rail** without any wire.

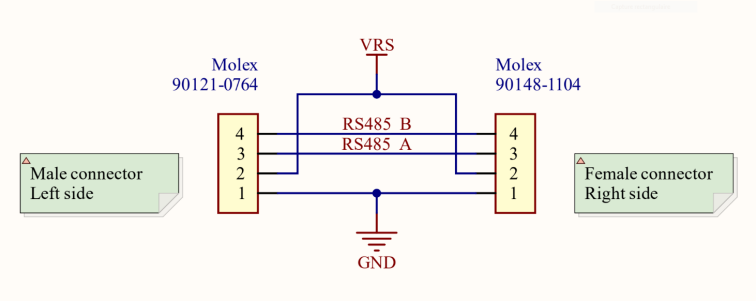

Figure 3: *RS485 connectors pin-out of DINFox nodes.*

3.2.2 External nodes

To be compatible with the DINFox system, the only requirement of an external node is to **support RS485 communication with a differential voltage of** $3.0\,V$, which is imposed by the master node (**DMM** board).

Depending on the power input specifications, external nodes can either be supplied by the V_{RS} rail or by an external source.

3.3 Data link layer

3.3.1 DINFox nodes (UART)

DINFox nodes use the UART standard to transfer data over the RS485 bus, with the following parameters.

Parameter	Value
Number of start bits	1
Number of data bits	8
Number of stop bits	1
Parity	None
Baud rate	1200 bauds

Table 3: *DINFox nodes UART parameters.*

3.3.1.1 Slave nodes

On slave nodes, the LPUART peripheral of the MCU is clocked by an external 32.768 kHz quartz. The internal baud rate generator for TX and RX operations is also deriving from this quartz. Since the input frequency is low, the baud rate value has to be limited to avoid jitter on the signal. At 9600 bauds, there are only 4 clock cycles from the 32.768 kHz: the resulting signal has a very poor duty cycle stability, leading to bit transmission or reception errors on the RS485 bus. To improve transfer robustness, the baud rate for DINFox nodes has thus been reduced to **1200 bauds**.

3.3.1.2 Master node

Since the master node initiates all the transfers and is never in a continuous reception state, there is no need to keep the LPUART active in stop mode, the RS485 transceiver can be switched off when there is no pending operation. Therefore, the master node can use a high speed clock source when transmitting on the RS485 bus, so that it can communicate with external nodes at higher baud rates without any jitter issue.

3.3.2 External nodes

3.3.2.1 KMTronic R4S8CR

R4S8CR protocol is based on the UART standard to transfer data over the RS485 bus, with the following parameters.

Parameter	Value
Number of start bits	1
Number of data bits	8
Number of stop bits	1
Parity	None
Baud rate	9600 bauds

Table 4: *R4S8CR UART parameters.*

3.4 Network layer

3.4.1 DINFox nodes (LMAC)

The nodes specifically designed for the DINFox system use a custom protocol called **LMAC** (Light Media Access Control), which adds the minimum overhead to transfer 7-bits data between two nodes.

The LMAC protocol is provided as a cross-platform C library and is available on GitHub: `https://github.com/Ludovic-Lesur/lmac-driver`. It is embedded as a Git sub-module in the nodes firmware.

An LMAC frame is composed of the following fields:

- The first byte of the frame is the **destination address** of the packet. It must have the **most significant bit set to 1** in order to be recognized as an address (see section **2.2**). All other bytes must have the most significant bit set to 0.
- The second byte is the **source address**, in other words the address of the node which is transmitting the packet. For a slave node, this field is used to know at which address the response has to be sent. For the master node, it is used to check that the response comes from the expected slave.
- Next bytes are the data.
- Then there is a **16-bits checksum** composed of the `CKH` and `CKL` fields. It is computed over all the previous bytes using the **Fletcher algorithm**.
- The frame finally ends with a specific marker **0x7F** which must not be used in any other byte: in particular, the **address 0x7F is forbidden** because the source address would be erroneously read as the end marker.

B0	B1	B2 .. B(n)	B(n+1)	B(n+2)	B(n+3)
Destination @ | **0x80**	Source @	DATA	CKH	CKL	**0x7F**

Table 5: *LMAC frame structure.*

3.4.2 External nodes

3.4.2.1 KMTronic R4S8CR

The R4S8CR relay box uses a custom protocol where the address is not managed by the network layer, but by the transport layer with the commands content. Indeed, each address corresponds to one relay rather than one box, so that multiple boxes can be connected on the same bus. However, all the frames start with a **0xFF** header.

B0	B1 .. Bn
0xFF	DATA

Table 6: *R4S8CR frame structure.*

3.5 Transport layer

3.5.1 DINFox nodes (UNA-AT)

On top of the network protocol, nodes communication is performed through **AT commands** which are transferred in ASCII format in the `DATA` field of the LMAC frame. As part of the UNA framework, the aim of this interface is to read and write 32 bits registers in order to control or monitor the node (see section 4). The commands are sent by the master node and will always be followed by a reply from the queried slave.

All DINFox nodes must support the following commands set. Mandatory fields are marked in orange, optional ones are marked in green. All values, addresses, masks and codes are in **hexadecimal representation** from 2 to 8 characters (1 to 4 bytes value). All AT commands and replies end with a single **CR character** (0x0D ASCII code).

The UNA-AT protocol is provided as a cross-platform C library and is available on GitHub: https://github.com/Ludovic-Lesur/una-at. It is embedded as a Git sub-module in the nodes firmware.

Command	Syntax	Parameters	Reply
Read register	AT$R=<reg_addr><CR>	<reg_addr> : Register address to read.	<reg_value><CR> or ERROR_<code><CR>
Write register	AT$W=<reg_addr>,<reg_value>,<reg_mask><CR>	<reg_addr> : Register address to write. <reg_value> : Value to write in register. <reg_mask> : Optional writing mask.	OK<CR> or ERROR_<code><CR>

Table 7: *UNA-AT commands set.*

When an error occurs during a command execution, the slave replies `ERROR_<code><CR>` on the bus, where `<code>` is always a 16 bits hexadecimal value. This error code is also stored in the slave errors stack, which can be read later on by the master (see section 4.2.1.6). The error will also be notified through dedicated **status bits** or a specific **error value** in the involved register.

3.5.2 External nodes

3.5.2.1 KMTronic R4S8CR

The R4S8CR commands are detailed in the following table, where all syntax is written in **hexadecimal format**. This protocol is implemented in a cross-platform C driver available on GitHub: https://github.com/Ludovic-Lesur/r4s8cr-driver. It is embedded as a Git sub-module in the master node firmware.

Command	Syntax	Parameters	Reply
Read relays	A<relay_box_id>00	<relay_box_id> : 4 bits relay box ID.	A<relay_box_id><r1st><r2st><r3st> <r4st><r5st><r6st><r7st><r8st> <rxst> : 00 if the relay x is off, 01 if the relay x is on.
Write relay	<relay_id><rxst>	<relay_id> : 8 bits relay ID. <rxst> : 00 to turn off, 01 to turn on.	*None.*

Table 8: *R4S8CR commands set.*

Note:

relay_box_id = (NODE_ADDR − 0x70 + 1) & 0x0F

relay_id = ((relay_box_id − 1) × 8) + relay_number (relay_number = 1 to 8)

4 Nodes registers

Nodes input controls and output data are accessed through a **set of registers** (up to 32 bits value), that can be read and/or written by the master module.

4.1 Physical data representation

Custom representations have been defined for physical data, in order to align fields on 8 bits and optimize their size, reducing RS485 frame lengths and power consumption when sending data through radio.

All **conversion functions** between physical values and custom representations are defined in the cross-platform **Unified Node Access library** (UNA-LIB) which is available in a GitHub repository: https://github.com/Ludovic-Lesur/una-lib.

4.1.1 Bit

A single bit is represented by a 2-bits value with the following mapping.

VALUE[1:0]	Meaning
0b00	Bit was successfully read as 0.
0b01	Bit was successfully read as 1.
0b10	Bit is not readable because it is forced by hardware.
0b11	Error occurred during bit reading (error value).

Table 9: *Bit representation.*

4.1.2 Time

7 6	5 4 3 2 1 0
UNIT[1:0]	VALUE[5:0]
0b00 : seconds **0b01** : minutes **0b10** : hours **0b11** : days	Raw value ($0 - 63$ range)

Table 10: *8-bits time representation.*

The available time ranges are the following:

- $\sim [0 - 1\ \text{minute}]$ with 1 second resolution.
- $\sim [0 - 1\ \text{hour}]$ with 1 minute resolution.
- $\sim [0 - 2.5\ \text{days}]$ with 1 hour resolution.
- $\sim [0 - 2\ \text{months}]$ with 1 day resolution.
- **0xFF** is used as **error value**.

4.1.3 Temperature

11	10	9	8	7	6	5	4	3	2	1	0
SIGN	VALUE[10:0]										
0b0 : positive **0b1** : negative	Raw absolute value in $0.1°C$ ($0 - 2047$ range)										

Table 11: *12-bits temperature representation.*

The available temperature range is the following:

- $-204.7\,°C$ to $+204.7\,°C$ with $0.1°C$ resolution.
- **0x7FF** is used as **error value**.

4.1.4 Voltage

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNIT	VALUE[14:0]														
0b0 : mV **0b1** : dV	Raw value ($0 - 32767$ range)														

Table 12: *16 bits voltage representation.*

The available voltage ranges are the following:

- $\sim [\,0 - 32\,V\,]$ with $1\,mV$ resolution.
- $\sim [\,0 - 3.2\,kV\,]$ with $100\,mV$ resolution.
- **0xFFFF** is used as **error value**.

4.1.5 Current

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNIT[1:0]		VALUE[13:0]													
0b00 : μA **0b01** : dmA **0b10** : mA **0b11** : dA		Raw value ($0 - 16383$ range)													

Table 13: *16 bits current representation.*

The available current ranges are the following:

- $\sim [\,0 - 16\,mA\,]$ with $1\,\mu A$ resolution.
- $\sim [\,0 - 1.6\,A\,]$ with $100\,\mu A$ resolution.
- $\sim [\,0 - 16\,A\,]$ with $1\,mA$ resolution.
- $\sim [\,0 - 1.6\,kA\,]$ with $100\,mA$ resolution.
- **0xFFFF** is used as **error value**.

4.1.6 Electrical power

15	14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
SIGN	UNIT[1:0]	VALUE[12:0]
0b0 : positive **0b1** : negative	**0b00** : mW **0b01** : dW **0b10** : W **0b11** : daW	Raw value ($0 - 8191$ range)

Table 14: *16 bits electrical power representation.*

The available power ranges are the following:

- $\sim [-8 - 8\,W]$ with $1\,mW$ resolution.
- $\sim [-800 - 800\,W]$ with $100\,mW$ resolution.
- $\sim [-8 - 8\,kW]$ with $1\,W$ resolution.
- $\sim [-80 - 80\,kW]$ with $10\,W$ resolution.
- **0x7FFF** is used as **error value**.

The same representation applies for VA unit.

4.1.7 Electrical energy

15	14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
SIGN	UNIT[1:0]	VALUE[12:0]
0b0 : positive **0b1** : negative	**0b00** : mWh **0b01** : dWh **0b10** : Wh **0b11** : $daWh$	Raw value ($0 - 8191$ range)

Table 15: *16 bits electrical energy representation.*

The available power ranges are the following:

- $\sim [-8 - 8\,Wh]$ with $1\,mWh$ resolution.
- $\sim [-800 - 800\,Wh]$ with $100\,mWh$ resolution.
- $\sim [-8 - 8\,kWh]$ with $1\,Wh$ resolution.
- $\sim [-80 - 80\,kWh]$ with $10\,Wh$ resolution.
- **0x7FFF** is used as **error value**.

The same representation applies for VAh unit.

4.1.8 Power factor

7	6	5	4	3	2	1	0
SIGN	VALUE[6:0]						
0b0 : positive **0b1** : negative	Floor of absolute value × 100 (0 – 100 range)						

Table 16: *8 bits power factor representation.*

The available power factor range is the following:

- -1 to $+1$ with $0,01$ resolution.
- **0x7F** is used as **error value**.

4.1.9 RF power

7	6	5	4	3	2	1	0
VALUE[7:0]							
Offset (0 – 255 range) defined as $(P[dBm] + 174)$							

Table 17: *8 bits RF power representation.*

The available RF power range is the following:

- $-174\,dBm$ to $+80\,dBm$ with $1\,dB$ resolution.
- **0xFF** is used as **error value**.

4.1.10 Year

7	6	5	4	3	2	1	0
VALUE[7:0]							
Offset (0 – 255 range) defined as $(Y - 2000)$							

Table 18: *8 bits year representation.*

The available year range is the following:

- 2000 to 2254 with 1 year resolution.
- **0xFF** is used as **error value**.

4.2 DINFox nodes

DINFox nodes have a minimum registers set available on all nodes. Following the common registers, all nodes can have specific registers that contain the specific input controls or output data of the node. They are defined in the following GitHub repository: https://github.com/Ludovic-Lesur/dinfox-registers.

4.2.1 Common registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x00	NODE_ID	16	R	Table **20**	Node address and board ID.
0x01	HW_VERSION	16	R	Table **21**	Node hardware version.
0x02	SW_VERSION_0	32	R	Table **22**	Node embedded software version
0x03	SW_VERSION_1	32	R	Table **23**	Node embedded software commit ID.
0x04	FLAGS_0	8	R	Table **24**	Common compilation flags.
0x05	ERROR_STACK	16	R	Table **25**	Error stack.
0x06	STATUS_0	16	R	Table **26**	Common status register.
0x07	CONTROL_0	8	R/W	Table **27**	Common control register.
0x08	ANALOG_DATA_0	32	R	Table **28**	Common analog data.

Table 19: *DINFox common registers set.*

4.2.1.1 Node ID register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BOARD_ID[7:0]									NODE_ADDR[6:0]						

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 8	8	BOARD_ID	–	Node board ID (see table **1**)	**Raw** value.
7	1	–	0b0	Unused.	–
6 – 0	7	NODE_ADDR	–	Node address (see section **2.2**)	**Raw** value.

Table 20: *Node ID register.*

4.2.1.2 Hardware version register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINOR[7:0]								MAJOR[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 8	8	MINOR	–	Minor part of the hardware version.	**Raw** value.
7 – 0	8	MAJOR	–	Major part of the hardware version.	**Raw** value.

Table 21: *Hardware version register.*

4.2.1.3 Software version register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							DTYF	COMMIT_INDEX[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINOR[7:0]								MAJOR[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 25	7	–	0b0000000	Unused.	–
24	1	DTYF	–	Git dirty flag.	**0b0** : clean code. **0b1** : dirty code.
23 – 16	8	COMMIT_INDEX	–	Git commit index.	**Raw** value.
15 – 8	8	MINOR	–	Minor part of the software version.	**Raw** value.
7 – 0	8	MAJOR	–	Major part of the software version.	**Raw** value.

Table 22: *Software version register 0.*

4.2.1.4 Software version register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				COMMIT_ID[27:16]											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMIT_ID[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 28	4	–	0b0000	Unused.	–
27 – 0	28	COMMIT_ID	–	Git commit ID.	**Raw** value.

Table 23: *Software version register 1.*

4.2.1.5 Flags register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
														NFRF	DF

Bits	Size	Field	Reset value	Description	Format
31 – 2	30	–	0b0[30]	Unused.	–
1	1	NFRF	–	NVM factory reset flag.	**0b0** : Factory reset is disabled. **0b1** : Factory reset is enabled.
0	1	DF	–	Debug mode flag.	**0b0** : Debug mode is disabled. **0b1** : Debug mode is enabled.

Table 24: *Flags register 0.*

4.2.1.6 Error stack register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERROR[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	ERROR	–	Last error code stored in stack.	**Raw** value.

Table 25: *Error stack register.*

This register can be read multiple times to unstack all errors, until the returned value is 0.

Errors codes use a **relative base system** where each driver has its own sub-bases. When an error occur, the code is propagated to the upper layers and encapsulated in the sub-base of each calling driver until the application. This way, **all the stack trace is combined in a single 16-bits value** instead of creating multiple codes with absolute bases. This is very useful to monitor the error codes remotely, especially with a radio link which has a limited number of bytes.

Root bases are defined in each embedded software project:

- Master node: https://github.com/Ludovic-Lesur/dmm/blob/master/application/inc/error_base.h
- Slave nodes: https://github.com/Ludovic-Lesur/dsm/blob/master/application/inc/error_base.h

4.2.1.7 Status register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
						ESF	BF	LPWR	WWDG	IWDG	SFT	POR	PIN	OBL	FW

Bits	Size	Field	Reset value	Description	Format
31 – 10	22	–	0b0[22]	Unused.	–
9	1	ESF	0b0	MCU error stack flag.	**0b0** : error stack is empty. **0b1** : error stack is not empty.
8	1	BF	0b1	MCU boot flag.	**0b0** : MCU did not reboot since last flag clearing. **0b1** : MCU rebooted since last flag clearing.
7	1	LPWR	–	Low power reset flag.	**0b0** : no LPWR reset occurred. **0b1** : LPWR reset occurred.
6	1	WWDG	–	Window watchdog reset flag.	**0b0** : no WWDG reset occurred. **0b1** : WWDG reset occurred.
5	1	IWDG	–	Independent watchdog reset flag.	**0b0** : no IWDG reset occurred. **0b1** : IWDG reset occurred.
4	1	SFT	–	Software reset flag.	**0b0** : no SFT reset occurred. **0b1** : SFT reset occurred.
3	1	POR	–	Power on reset flag.	**0b0** : no POR reset occurred. **0b1** : POR reset occurred.
2	1	PIN	–	NRST pin reset flag.	**0b0** : no PIN reset occurred. **0b1** : PIN reset occurred.
1	1	OBL	–	Options bytes loading reset flag.	**0b0** : no OBL reset occurred. **0b1** : OBL reset occurred.
0	1	FW	–	Firewall reset flag.	**0b0** : no FW reset occurred. **0b1** : FW reset occurred.

Table 26: *Status register 0.*

4.2.1.8 Control register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
													BFC	MTRG	RTRG

Bits	Size	Field	Reset value	Description	Format
31 – 3	29	–	0b0[29]	Unused.	–
2	1	BFC	0b0	MCU boot flag clear.	**0b0** : no action. **0b1** : clear boot flag (BF bit) in status register 0.
1	1	MTRG	0b0	Measure trigger flag.	**0b0** : no action (W) or no pending measurement (R). **0b1** : start measurements (W) or measurements pending (R).
0	1	RTRG	0b0	Reset trigger flag.	**0b0** : no action. **0b1** : trigger software reset.

Table 27: *Control register 0.*

4.2.1.9 Analog data register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				TMCU[11:0]											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VMCU[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 28	4	–	0b0000	Unused.	–
27 – 16	12	TMCU	0x7FF	MCU temperature.	Table **11**
15 – 0	16	VMCU	0xFFFF	MCU supply voltage.	Table **12**

Table 28: *Analog data register 0.*

4.2.2 LVRM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	8	R	Table **30**	Compilation flags.
0x0A	CONFIGURATION_0	32	R/W	Table **31**	Battery voltage thresholds for BMS mode.
0x0B	CONFIGURATION_1	16	R/W	Table **32**	I_{OUT} offset calibration value.
0x0C	STATUS_1	8	R	Table **33**	Relay status.
0x0D	CONTROL_1	8	R/W	Table **34**	Relay control.
0x0E	ANALOG_DATA_1	32	R	Table **35**	V_{COM} and V_{OUT} voltages measurements.
0x0F	ANALOG_DATA_2	16	R	Table **36**	I_{OUT} current measurement.

Table 29: *LVRM specific registers set.*

4.2.2.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
														RLFH	BMSF

Bits	Size	Field	Reset value	Description	Format
31 – 2	30	–	0b0[30]	Unused.	–
1	1	RLFH	–	Relay control mode (set at compilation step according to hardware).	**0b0** : Relay controlled by the MCU. **0b1** : Relay controlled by hardware.
0	1	BMSF	–	BMS mode flag (set at compilation step).	**0b0** : BMS mode disabled. **0b1** : BMS mode enabled.

Table 30: *Flags register 1.*

4.2.2.2 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VBATT_THRESHOLD_HIGH															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBATT_THRESHOLD_LOW															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VBATT_THRESHOLD_HIGH	–	High voltage threshold of the BMS hysteresis.	Table **12**
15 – 0	16	VBATT_THRESHOLD_LOW	–	Low voltage threshold of the BMS hysteresis.	Table **12**

Table 31: *Configuration register 0.*

Note: this register is only used when the BMSF bit is set.

4.2.2.3 Configuration register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOUT_OFFSET[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	IOUT_OFFSET	–	Output current offset calibration value.	Table **13**

Table 32: *Configuration register 1.*

4.2.2.4 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
														RLSTST	

Bits	Size	Field	Reset value	Description	Format
31 – 2	30	–	0b0[30]	Unused.	–
1 – 0	2	RLSTST	0b11	Relay state status.	Table **9** **0b00** : NC or R path closed. **0b01** : NO or S path closed.

Table 33: *Status register 1.*

4.2.2.5 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															RLST

Bits	Size	Field	Reset value	Description	Format
31 – 1	31	–	0b0[31]	Unused.	–
0	1	RLST	0b0	Relay state control.	**0b0** : close NC or R path. **0b1** : close NO or S path.

Table 34: *Control register 1.*

4.2.2.6 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VOUT[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCOM[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VOUT	0xFFFF	Relay output voltage.	Table **12**
15 – 0	16	VCOM	0xFFFF	Relay common input voltage.	Table **12**

Table 35: *Analog data register 1.*

4.2.2.7 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOUT[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	IOUT	0xFFFF	Relay output current.	Table **13**

Table 36: *Analog data register 2.*

4.2.3 BPSM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	8	R	Table **38**	Compilation flags.
0x0A	CONFIGURATION_0	32	R/W	Table **39**	CHEN threshold and toggle period.
0x0B	CONFIGURATION_1	32	R/W	Table **40**	Low voltage flag (LVF) thresholds.
0x0C	CONFIGURATION_2	32	R/W	Table **41**	Critical voltage flag (CVF) thresholds.
0x0D	STATUS_1	16	R	Table **42**	Charging and backup status.
0x0E	CONTROL_1	8	R/W	Table **43**	Charging and backup control.
0x0F	ANALOG_DATA_1	32	R	Table **44**	V_{SRC} and V_{STR} voltages measurements.
0x10	ANALOG_DATA_2	16	R	Table **45**	V_{BKP} voltage measurement.

Table 37: *BPSM specific registers set.*

4.2.3.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
												BKFH		CSFH	CEFH

Bits	Size	Field	Reset value	Description	Format
31 – 4	28	–	0x0000000	Unused.	–
3	1	BKFH	–	Backup output control mode (set at compilation step according to hardware).	**0b0** : Backup output controlled by the MCU. **0b1** : Backup output controlled by hardware.
2	1	–	0b0	Unused.	–
1	1	CSFH	–	Charge status mode (set at compilation step according to hardware).	**0b0** : Charge status connected to the MCU. **0b1** : Charge status connected in hardware.
0	1	CEFH	–	Charge control mode (set at compilation step according to hardware).	**0b0** : Charge controlled by the MCU. **0b1** : Charge controlled by hardware.

Table 38: *Flags register 1.*

4.2.3.2 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								CHEN_TOGGLE_PERIOD							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHEN_THRESHOLD															

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	–	0x00	Unused.	–
23 – 16	8	CHEN_TOGGLE_PERIOD	–	Charge toggle period.	Table **10**
15 – 0	16	CHEN_THRESHOLD	–	Voltage threshold to set CHEN bit.	Table **12**

Table 39: *Configuration register 0.*

Note: this register is only used when CHMD = 0b1 and CEFH = 0b0.

4.2.3.3 Configuration register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LVF_HIGH_THRESHOLD															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LVF_LOW_THRESHOLD															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	LVF_HIGH_THRESHOLD	–	High threshold of the LVF voltage hysteresis.	Table **12**
15 – 0	16	LVF_LOW_THRESHOLD	–	Low threshold of the LVF voltage hysteresis.	Table **12**

Table 40: *Configuration register 1.*

4.2.3.4 Configuration register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CVF_HIGH_THRESHOLD															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CVF_LOW_THRESHOLD															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CVF_HIGH_THRESHOLD	–	High threshold of the CVF voltage hysteresis.	Table **12**
15 – 0	16	CVF_LOW_THRESHOLD	–	Low threshold of the CVF voltage hysteresis.	Table **12**

Table 41: *Configuration register 2.*

4.2.3.5 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						CVF	LVF			CHRGST		CHENST		BKENST	

Bits	Size	Field	Reset value	Description	Format
31 – 10	22	–	0b0[22]	Unused.	–
9	1	CVF	0b0	Critical voltage detector flag.	**0b0** : storage element voltage is above the critical threshold. **0b1** : storage element voltage is under the critical threshold.
8	1	LVF	0b0	Low voltage detector flag.	**0b0** : storage element voltage is above the low threshold. **0b1** : storage element voltage is under the low threshold.
7 – 6	2	–	0b00	Unused.	–
5 – 4	2	CHRGST	0b11	Storage element charging status.	Table **9** **0b00** : charge pending. **0b01** : charge complete.
3 – 2	2	CHENST	0b11	Storage element charging enable status.	Table **9** **0b00** : charge disabled. **0b01** : charge enabled.
1 – 0	2	BKENST	0b11	Backup output state.	Table **9** **0b00** : backup output disabled. **0b01** : backup output enabled.

Table 42: *Status register 1.*

4.2.3.6 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
													CHEN	CHMD	BKEN

Bits	Size	Field	Reset value	Description	Format
31 – 3	29	–	0b0[29]	Unused.	–
2	1	CHEN	0b0	Storage element charging control (only if CHMD = 0b1 and CEFH = 0b0).	**0b0** : disable charge. **0b1** : enable charge.
1	1	CHMD	0b0	Storage element charging mode.	**0b0** : charge is automatically controlled by software. **0b1** : charge is controlled by the CHEN bit.
0	1	BKEN	0b0	Backup output control.	**0b0** : disable backup output. **0b1** : enable backup output.

Table 43: *Control register 1.*

4.2.3.7 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VSTR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSRC[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VSTR	0xFFFF	Storage element voltage.	Table **12**
15 – 0	16	VSRC	0xFFFF	Source voltage.	Table **12**

Table 44: *Analog data register 1.*

4.2.3.8 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBKP[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	VBKP	0xFFFF	Backup voltage.	Table **12**

Table 45: *Analog data register 2.*

4.2.4 DDRM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	8	R	Table **47**	Compilation flags.
0x0A	CONFIGURATION_0	16	R/W	Table **48**	I_{OUT} offset calibration value.
0x0B	STATUS_1	8	R	Table **49**	DC–DC converter status.
0x0C	CONTROL_1	8	R/W	Table **50**	DC–DC converter control.
0x0D	ANALOG_DATA_1	32	R	Table **51**	V_{IN} and V_{OUT} voltages measurements.
0x0E	ANALOG_DATA_2	16	R	Table **52**	I_{OUT} current measurement.

Table 46: *DDRM specific registers set.*

4.2.4.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
															DDFH

Bits	Size	Field	Reset value	Description	Format
31 – 1	31	–	0b0[31]	Unused.	–
0	1	DDFH	–	DC–DC control mode (set at compilation step according to hardware).	**0b0** : DC–DC controlled by the MCU. **0b1** : DC–DC controlled by hardware.

Table 47: *Flags register 1.*

4.2.4.2 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOUT_OFFSET[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	IOUT_OFFSET	–	Output current offset calibration value.	Table **13**

Table 48: *Configuration register 0.*

4.2.4.3 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
														DDENST	

Bits	Size	Field	Reset value	Description	Format
31 – 2	30	–	0b0[30]	Unused.	–
1 – 0	2	DDENST	0b11	DC–DC converter state.	Table **9** **0b00** : DC–DC output disabled. **0b01** : DC–DC output enabled.

Table 49: *Status register 1.*

4.2.4.4 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
															DDEN

Bits	Size	Field	Reset value	Description	Format
31 – 1	31	–	0b0[31]	Unused.	–
0	1	DDEN	0b0	DC–DC converter state control.	**0b0** : disable DC–DC output **0b1** : enable DC–DC output.

Table 50: *Control register 1.*

4.2.4.5 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VOUT[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VOUT	0xFFFF	DC–DC converter output voltage.	Table **12**
15 – 0	16	VIN	0xFFFF	DC–DC converter input voltage.	Table **12**

Table 51: *Analog data register 1.*

4.2.4.6 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOUT[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	IOUT	0xFFFF	DC–DC converter output current.	Table **13**

Table 52: *Analog data register 2.*

4.2.5 UHFM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	CONFIGURATION_0	16	R/W	Table **54**	Sigfox radio parameters.
0x0A	CONFIGURATION_1	32	R/W	Table **55**	Sigfox radio parameters.
0x0B	STATUS_1	32	R	Table **56**	Modem status.
0x0C	CONTROL_1	32	R/W	Table **57**	Modem control.
0x0D	ANALOG_DATA_1	32	R	Table **58**	V_{RF} voltage measurement.
0x0E	SIGFOX_EP_ID	32	R	Table **59**	Sigfox end-point ID.
0x0F	SIGFOX_UL_PAYLOAD_0	32	R/W	Table **60**	Sigfox UL payload bytes 0 to 3.
0x10	SIGFOX_UL_PAYLOAD_1	32	R/W	Table **61**	Sigfox UL payload bytes 4 to 7.
0x11	SIGFOX_UL_PAYLOAD_2	32	R/W	Table **62**	Sigfox UL payload bytes 8 to 11.
0x12	SIGFOX_DL_PAYLOAD_0	32	R	Table **63**	Sigfox DL payload bytes 0 to 3.
0x13	SIGFOX_DL_PAYLOAD_1	32	R	Table **64**	Sigfox DL payload bytes 4 to 7.
0x14	RADIO_TEST_0	32	R/W	Table **65**	Radio test modes configuration.
0x15	RADIO_TEST_1	16	R/W	Table **66**	Radio test modes configuration.

Table 53: *UHFM specific registers set.*

4.2.5.1 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		RFP_TEST_MODE[4:0]				UL_PAYLOAD_SIZE[4:0]					BF	MSGT[2:0]			CMSG
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_POWER[7:0]								NFR[1:0]		BR[1:0]		RC[4:0]			

Bits	Size	Field	Reset value	Description	Format
31 – 30	2	–	0b00	Unused.	–
29 – 26	4	RFP_TEST_MODE	0b0000	Sigfox RFP Addon test mode reference.	See sigfox_ep_addon_rfp_api.h file of Sigfox RFP Addon.
25 – 21	5	UL_PAYLOAD_SIZE	0b00000	Uplink payload size.	**Raw** value in bytes (0 to 12 for protocol V1)
20	1	BF	0b0	Bidirectional flag.	**0b0** : uplink only **0b1** : uplink with downlink request
19 – 17	3	MSGT	0b000	Application message type (CMSG = 0) or control message type (CMSG = 1).	See sigfox_types.h file of Sigfox End-Point Library.
16	1	CMSG	0b0	Control message flag. (Disabled at compilation step).	**0b0** : application message **0b1** : control message
15 – 8	8	TX_POWER	0xBC	TX power of Sigfox transmission. (14 dBm fixed at compilation step).	Table **17**
7 – 6	2	NFR	0b11	Number of frames per uplink messages (N).	**0b00** : no frame (uplink disabled) **0b01** : 1 frame (N=1) **0b10** : 2 frames (N=2) **0b11** : 3 frames (N=3)
5 – 4	2	BR	0b00	Signal bit rate.	**0b01** : 100 bps **0b01** : 600 bps **0b10–0b11** : reserved for future use
3 – 0	4	RC	0b0000	Sigfox radio configuration zone. (RC1 fixed at compilation step).	**0b0000** : RC1 **0b0001** : RC2 **0b0010** : RC3C **0b0011** : RC3D **0b0100** : RC4 **0b0101** : RC5 **0b0110** : RC6 **0b0111** : RC7 **0b1000–0b1111** : reserved for future use

Table 54: *Configuration register 0.*

Note: Application message payload is given in the SIGFOX_UL_PAYLOAD_x registers.

4.2.5.2 Configuration register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCONF[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIFU[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	TCONF	0x07D0	Delay between downlink reception and confirmation frame transmission. (2000 *ms* fixed at compilation step).	**Raw** value in *ms* (1400 to 4000)
15 – 0	16	TIFU	0x03E8	Delay between uplink frames. (1000 *ms* fixed at compilation step).	**Raw** value in *ms* (0 to 2000)

Table 55: *Configuration register 1.*

4.2.5.3 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				BIDIRECTIONAL_MC[11:0]											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL_RSSI[7:0]								MESSAGE_STATUS[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 28	4	–	0x0	Unused.	–
27 – 16	12	BIDIRECTIONAL_MC	–	Message counter of the last uplink with bidirectional request.	**Raw** value.
15 – 8	8	DL_RSSI	0x00	RSSI of the last downlink message received.	Table **17**
7 – 0	8	MESSAGE_STATUS	0x00	Sigfox message transmission status.	See sigfox_ep_api.h file of Sigfox End-Point Library.

Table 56: *Status register 1.*

4.2.5.4 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
												RSEN	CWEN	TTRG	STRG

Bits	Size	Field	Reset value	Description	Format
31 – 4	28	–	0b0[28]	Unused.	–
3	1	RSEN	0b0	Continuous RSSI measurement control.	**0b0** : stop RSSI measure (W) or RSSI measure stopped (R). **0b1** : start RSSI measure (W) or RSSI measure running (R).
2	1	CWEN	0b0	Continuous wave control.	**0b0** : Stop continuous wave (W) or continuous wave stopped (R). **0b1** : Start continuous wave (W) or continuous wave running (R).
1	1	TTRG	0b0	Sigfox RFP Addon test mode trigger.	**0b0** : no action (W) or no test mode pending (R). **0b1** : start test mode (W) or test mode pending (R).
0	1	STRG	0b0	Sigfox message trigger.	**0b0** : no action (W) or no transmission pending (R). **0b1** : send message (W) or message transmission pending (R).

Table 57: *Control register 1.*

Note: Continuous RSSI measurement and continuous wave are performed on the RF frequency given by the `RADIO_TEST_0` register. Continuous wave power is given by the `RADIO_TEST_1` register.

4.2.5.5 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VRF_RX[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VRF_TX[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VRF_RX	0xFFFF	Radio front-end voltage in RX.	Table **12**
15 – 0	16	VRF_TX	0xFFFF	Radio front-end voltage in TX.	Table **12**

Table 58: *Analog data register 1.*

4.2.5.6 Sigfox EP ID register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EP_ID_BYTE_3[7:0]								EP_ID_BYTE_2[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EP_ID_BYTE_1[7:0]								EP_ID_BYTE_0[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	EP_ID_BYTE_3	–	Byte 3 of the Sigfox end-point ID.	–
23 – 16	8	EP_ID_BYTE_2	–	Byte 2 of the Sigfox end-point ID.	–
15 – 8	8	EP_ID_BYTE_1	–	Byte 1 of the Sigfox end-point ID.	–
7 – 0	8	EP_ID_BYTE_0	–	Byte 0 of the Sigfox end-point ID.	–

Table 59: *Sigfox EP ID register.*

4.2.5.7 Sigfox UL payload register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UL_PAYLOAD_BYTE_3[7:0]								UL_PAYLOAD_BYTE_2[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UL_PAYLOAD_BYTE_1[7:0]								UL_PAYLOAD_BYTE_0[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	UL_PAYLOAD_BYTE_3	0x00	Byte 3 of the Sigfox uplink payload.	–
23 – 16	8	UL_PAYLOAD_BYTE_2	0x00	Byte 2 of the Sigfox uplink payload.	–
15 – 8	8	UL_PAYLOAD_BYTE_1	0x00	Byte 1 of the Sigfox uplink payload.	–
7 – 0	8	UL_PAYLOAD_BYTE_0	0x00	Byte 0 of the Sigfox uplink payload.	–

Table 60: *Sigfox UL payload register 0.*

4.2.5.8 Sigfox UL payload register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UL_PAYLOAD_BYTE_7[7:0]								UL_PAYLOAD_BYTE_6[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UL_PAYLOAD_BYTE_5[7:0]								UL_PAYLOAD_BYTE_4[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	UL_PAYLOAD_BYTE_7	0x00	Byte 7 of the Sigfox uplink payload.	–
23 – 16	8	UL_PAYLOAD_BYTE_6	0x00	Byte 6 of the Sigfox uplink payload.	–
15 – 8	8	UL_PAYLOAD_BYTE_5	0x00	Byte 5 of the Sigfox uplink payload.	–
7 – 0	8	UL_PAYLOAD_BYTE_4	0x00	Byte 4 of the Sigfox uplink payload.	–

Table 61: *Sigfox UL payload register 1.*

4.2.5.9 Sigfox UL payload register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UL_PAYLOAD_BYTE_11[7:0]								UL_PAYLOAD_BYTE_10[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UL_PAYLOAD_BYTE_9[7:0]								UL_PAYLOAD_BYTE_8[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	UL_PAYLOAD_BYTE_11	0x00	Byte 11 of the Sigfox uplink payload.	–
23 – 16	8	UL_PAYLOAD_BYTE_10	0x00	Byte 10 of the Sigfox uplink payload.	–
15 – 8	8	UL_PAYLOAD_BYTE_9	0x00	Byte 9 of the Sigfox uplink payload.	–
7 – 0	8	UL_PAYLOAD_BYTE_8	0x00	Byte 8 of the Sigfox uplink payload.	–

Table 62: *Sigfox UL payload register 2.*

4.2.5.10 Sigfox DL payload register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DL_PAYLOAD_BYTE_3[7:0]								DL_PAYLOAD_BYTE_2[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL_PAYLOAD_BYTE_1[7:0]								DL_PAYLOAD_BYTE_0[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	DL_PAYLOAD_BYTE_3	0x00	Byte 3 of the Sigfox downlink payload.	–
23 – 16	8	DL_PAYLOAD_BYTE_2	0x00	Byte 2 of the Sigfox downlink payload.	–
15 – 8	8	DL_PAYLOAD_BYTE_1	0x00	Byte 1 of the Sigfox downlink payload.	–
7 – 0	8	DL_PAYLOAD_BYTE_0	0x00	Byte 0 of the Sigfox downlink payload.	–

Table 63: *Sigfox DL payload register 0.*

4.2.5.11 Sigfox DL payload register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DL_PAYLOAD_BYTE_7[7:0]								DL_PAYLOAD_BYTE_6[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL_PAYLOAD_BYTE_5[7:0]								DL_PAYLOAD_BYTE_4[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	DL_PAYLOAD_BYTE_7	0x00	Byte 7 of the Sigfox downlink payload.	–
23 – 16	8	DL_PAYLOAD_BYTE_6	0x00	Byte 6 of the Sigfox downlink payload.	–
15 – 8	8	DL_PAYLOAD_BYTE_5	0x00	Byte 5 of the Sigfox downlink payload.	–
7 – 0	8	DL_PAYLOAD_BYTE_4	0x00	Byte 4 of the Sigfox downlink payload.	–

Table 64: *Sigfox DL payload register 1.*

4.2.5.12 Radio test register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RF_FREQUENCY[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RF_FREQUENCY[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 0	32	RF_FREQUENCY	0x33AD5EC0	RF center frequency used for continuous wave, RSSI and downlink decoder.	**Raw** value in *Hz*. (826000000 to 958000000)

Table 65: *Radio test register 0.*

4.2.5.13 Radio test register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSSI[7:0]								TX_POWER[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 8	8	RSSI	0x00	Radio RSSI read during continuous RSSI measurement.	Table **17**
7 – 0	8	TX_POWER	0xBC	Radio TX power used during continuous wave.	Table **17**

Table 66: *Radio test register 1.*

4.2.6 GPSM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	8	R	Table **68**	Compilation flags.
0x0A	CONFIGURATION_0	32	R/W	Table **69**	Time and geo-location fix timeout.
0x0B	CONFIGURATION_1	32	R/W	Table **70**	GPS timepulse output frequency.
0x0C	CONFIGURATION_2	8	R/W	Table **71**	GPS timepulse output duty cycle.
0x0D	STATUS_1	8	R	Table **72**	GPS status.
0x0E	CONTROL_1	8	R/W	Table **73**	GPS control.
0x0F	ANALOG_DATA_1	32	R	Table **74**	V_{GPS} and V_{ANT} voltages measurements.
0x10	TIME_DATA_0	32	R	Table **75**	UTC date.
0x11	TIME_DATA_1	32	R	Table **76**	UTC time.
0x12	TIME_DATA_2	16	R	Table **77**	Time fix duration.
0x13	GEOLOC_DATA_0	32	R	Table **78**	Latitude.
0x14	GEOLOC_DATA_1	32	R	Table **79**	Longitude.
0x15	GEOLOC_DATA_2	16	R	Table **80**	Altitude.
0x16	GEOLOC_DATA_3	32	R	Table **81**	Geo-location fix duration, number of satellites and HDOP.

Table 67: *GPSM specific registers set.*

4.2.6.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
														BKFH	AAF

Bits	Size	Field	Reset value	Description	Format
31 – 2	30	–	0b0[30]	Unused.	–
1	1	BKFH	–	GPS backup control mode (set at compilation level according to hardware).	**0b0** : GPS backup signal controlled by the MCU. **0b1** : GPS backup signal forced in hardware.
0	1	AAF	–	Active antenna flag (set at compilation level according to hardware).	**0b0** : Active antenna disabled. **0b1** : Active antenna enabled.

Table 68: *Flags register 1.*

4.2.6.2 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GEOLOC_TIMEOUT[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIME_TIMEOUT[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	GEOLOC_TIMEOUT	0x00B4	Geo-location fix timeout.	**Raw** value in *s*.
15 – 0	16	TIME_TIMEOUT	0x0078	Time fix timeout.	**Raw** value in *s*.

Table 69: *Configuration register 0.*

4.2.6.3 Configuration register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREQUENCY[31:16]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FREQUENCY[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 0	32	FREQUENCY	0x00989680	Timepulse signal frequency.	**Raw** value in *Hz*. (1 to 10000000)

Table 70: *Configuration register 1.*

4.2.6.4 Configuration register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
									DUTY_CYCLE[6:0]						

Bits	Size	Field	Reset value	Description	Format
31 – 7	25	–	0b0[25]	Unused.	–
6 – 0	7	DUTY_CYCLE	0x32	Timepulse signal duty cycle.	**Raw** value in % (0 to 100)

Table 71: *Configuration register 2.*

4.2.6.5 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
										BKENST		PWST	TPST	GFS	TFS

Bits	Size	Field	Reset value	Description	Format
31 – 6	26	–	0b0[26]	Unused.	–
5 – 4	2	BKENST	0b11	GPS backup voltage status.	Table **9** **0b00** : GPS backup disabled. **0b01** : GPS backup enabled.
3	1	PWST	0b0	GPS power supply status.	0b0 : GPS power supply is off. **0b1** : GPS power supply is on.
2	1	TPST	0b0	GPS timepulse status.	**0b0** : GPS timepulse stopped. **0b1** : GPS timepulse running.
1	1	GFS	0b0	GPS geo-location fix status.	**0b0** : timeout. **0b1** : success.
0	1	TFS	0b0	GPS time fix status.	**0b0** : timeout. **0b1** : success.

Table 72: *Status register 1.*

4.2.6.6 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										BKEN	PWEN	PWMD	TPEN	GTRG	TTRG

Bits	Size	Field	Reset value	Description	Format
31 – 6	26	–	0b0[26]	Unused.	–
5	1	BKEN	0b0	GPS backup voltage control.	**0b0** : Turn GPS backup off. **0b1** : Turn GPS backup on.
4	1	PWEN	0b0	Direct control of the GPS power supply (only if PWMD = 0b1).	**0b0** : Turn GPS off. **0b1** : Turn GPS on.
3	1	PWMD	0b0	GPS power supply control mode.	**0b0** : GPS power supply is automatically controlled by software. **0b1** : GPS power supply is controlled by the PWEN bit.
2	1	TPEN	0b0	GPS timepulse output control.	**0b0** : Disable GPS timepulse. **0b1** : Enable GPS timepulse.
1	1	GTRG	0b0	GPS geo-location fix trigger.	**0b0** : no action (W) or no geo-location fix pending (R). **0b1** : Perform geo-location fix (W) or geo-location fix pending (R).
0	1	TTRG	0b0	GPS time fix trigger.	**0b0** : no action (W) or no time fix pending (R). **0b1** : Perform time fix (W) or time fix pending (R).

Table 73: *Control register 1.*

Note: Time and geo-location fix timeouts are given by the CONFIGURATION_1 register.

Note: Timepulse signal settings are given by the CONFIGURATION_2 and CONFIGURATION_3 registers.

4.2.6.7 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VANT[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VGPS[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VANT	0xFFFF	Active antenna voltage.	Table **12**
15 – 0	16	VGPS	0xFFFF	GPS module voltage.	Table **12**

Table 74: *Analog data register 1.*

4.2.6.8 Time data register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								YEAR[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
				MONTH[3:0]				DATE[4:0]					DAY[2:0]		

Bits	Size	Field	Reset value	Description	Format
31 – 24	12	–	0x000	Unused.	–
23 – 16	8	YEAR	0x00	UTC year.	Table **18**
15 – 12	4	–	0b0000	Unused.	–
11 – 8	4	MONTH	0b0000	UTC month.	**Raw** value (1 – 12)
7 – 3	5	DATE	0b00000	UTC date.	**Raw** value (1 – 31)
2 – 0	3	DAY	0b000	UTC week day (not supported yet).	**0b000** : Monday. **0b001** : Tuesday. **0b010** : Wednesday. **0b011** : Thursday. **0b100** : Friday. **0b101** : Saturday. **0b110** : Sunday. **0b111** : unused.

Table 75: *Time data register 0.*

4.2.6.9 Time data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
											HOUR[4:0]				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		MINUTE[5:0]								SECOND[5:0]					

Bits	Size	Field	Reset value	Description	Format
31 – 21	11	–	0b0[11]	Unused.	–
20 – 16	5	HOUR	0b00000	UTC hour.	**Raw** value (0 – 23)
15 – 14	2	–	0b00	Unused.	–
13 – 8	6	MINUTE	00b000000	UTC minute.	**Raw** value (0 – 59)
7 – 6	2	–	0b00	Unused.	–
5 – 0	6	SECOND	0b000000	UTC second.	**Raw** value (0 – 59)

Table 76: *Time data register 1.*

4.2.6.10 Time data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIX_DURATION[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	FIX_DURATION	0x0000	Time fix duration.	**Raw** value in *s*.

Table 77: *Time data register 2.*

4.2.6.11 Geo-location data register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NF	SECOND[16:2]														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECOND[1:0]		MINUTE[5:0]						DEGREE[7:0]							

Bits	Size	Field	Reset value	Description	Format
31	1	NF	0b0	Latitude north flag.	**0b0** : south. **0b1** : north.
30 – 14	17	SECOND	0b0[17]	Second of latitude.	Fractional part of minutes ×100000 seconds [”] = (SECOND / 100000) × 60
13 – 8	6	MINUTE	0b000000	Minute of latitude.	**Raw** value in ’
7 – 0	8	DEGREE	0x00	Degree of latitude.	**Raw** value in °

Table 78: *Geo-location data register 0.*

4.2.6.12 Geo-location data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EF	SECOND[16:2]														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECOND[1:0]	MINUTE[5:0]							DEGREE[7:0]							

Bits	Size	Field	Reset value	Description	Format
31	1	EF	0b0	Longitude east flag.	**0b0** : west. **0b1** : east.
30 – 14	17	SECOND	0b0[17]	Second of longitude.	Fractional part of minutes ×100000 seconds [”] = (SECOND / 100000) × 60
13 – 8	6	MINUTE	0b000000	Minute of longitude.	**Raw** value in ’
7 – 0	8	DEGREE	0x00	Degree of longitude.	**Raw** value in °

Table 79: *Geo-location data register 1.*

4.2.6.13 Geo-location data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALTITUDE[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	ALTITUDE	0x0000	Altitude.	**Raw** value in *m*

Table 80: *Geo-location data register 2.*

4.2.6.14 Geo-location data register 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HDOP[11:0]												NSAT[3:0]			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIX_DURATION[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 20	12	HDOP	0x000	Horizontal precision.	**Raw** value × 100
19 – 16	4	NSAT	0b0000	Number of satellites.	**Raw** value
15 – 0	16	FIX_DURATION	0x0000	Position fix duration.	**Raw** value in *s*.

Table 81: *Geo-location data register 3.*

4.2.7 SM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	8	R	Table **83**	Compilation flags.
0x0A	FLAGS_2	32	R	Table **84**	V_{AIN0} and V_{AIN1} front–end configuration.
0x0B	FLAGS_3	32	R	Table **85**	V_{AIN2} and V_{AIN3} front–end configuration.
0x0C	ANALOG_DATA_1	32	R	Table **86**	V_{AIN0} and V_{AIN1} voltages measurements.
0x0D	ANALOG_DATA_2	32	R	Table **87**	V_{AIN2} and V_{AIN3} voltages measurements.
0x0E	ANALOG_DATA_3	16	R	Table **88**	T_{amb} and H_{amb} measurements.
0x0F	DIGITAL_DATA	8	R	Table **89**	Digital inputs measurements.

Table 82: *SM specific registers set.*

4.2.7.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
													DIGF	DIOF	AINF

Bits	Size	Field	Reset value	Description	Format
31 – 3	29	–	0b0[29]	Unused.	–
2	1	DIGF	–	Digital sensors enable flag.	**0b0** : digital sensors disabled. **0b1** : digital sensors enabled.
1	1	DIOF	–	Digital inputs enable flag.	**0b0** : digital inputs disabled. **0b1** : digital inputs enabled.
0	1	AINF	–	Analog inputs enable flag.	**0b0** : analog inputs disabled. **0b1** : analog inputs enabled.

Table 83: *Flags register 1.*

4.2.7.2 Flags register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AI1T	AI1G[15:0]														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AI0T	AI0G[15:0]														

Bits	Size	Field	Reset value	Description	Format
31	1	AI1T	–	V_{AIN1} conversion type (set at compilation step according to hardware).	**0b0** : attenuation. **0b1** : amplification.
30 – 16	15	AI1G	–	V_{AIN1} conversion gain (set at compilation step according to hardware).	**Raw value** expressed as: $\frac{V_{AIN1}}{V_{ADC}}$ for attenuation. $\frac{V_{ADC}}{V_{AIN1}}$ for amplification.
15	1	AI0T	–	V_{AIN0} conversion type (set at compilation step according to hardware).	**0b0** : attenuation. **0b1** : amplification.
14 – 0	15	AI0G	–	V_{AIN0} conversion gain (set at compilation step according to hardware).	**Raw value** expressed as: $\frac{V_{AIN0}}{V_{ADC}}$ for attenuation. $\frac{V_{ADC}}{V_{AIN0}}$ for amplification.

Table 84: *Flags register 2.*

4.2.7.3 Flags register 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AI3T	AI3G[15:0]														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AI2T	AI2G[15:0]														

Bits	Size	Field	Reset value	Description	Format
31	1	AI1T	–	V_{AIN3} conversion type (set at compilation step according to hardware).	**0b0** : attenuation. **0b1** : amplification.
30 – 16	15	AI1G	–	V_{AIN3} conversion gain (set at compilation step according to hardware).	**Raw value** expressed as: $\frac{V_{AIN3}}{V_{ADC}}$ for attenuation. $\frac{V_{ADC}}{V_{AIN3}}$ for amplification.
15	1	AI0T	–	V_{AIN2} conversion type (set at compilation step according to hardware).	**0b0** : attenuation. **0b1** : amplification.
14 – 0	15	AI0G	–	V_{AIN2} conversion gain (set at compilation step according to hardware).	**Raw value** expressed as: $\frac{V_{AIN2}}{V_{ADC}}$ for attenuation. $\frac{V_{ADC}}{V_{AIN2}}$ for amplification.

Table 85: *Configuration register 3.*

4.2.7.4 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAIN1[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAIN0[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VAIN1	0xFFFF	V_{AIN1} voltage.	Table **12**
15 – 0	16	VAIN0	0xFFFF	V_{AIN0} voltage.	Table **12**

Table 86: *Analog data register 1.*

4.2.7.5 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAIN3[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAIN2[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VAIN3	0xFFFF	V_{AIN3} voltage.	Table **12**
15 – 0	16	VAIN2	0xFFFF	V_{AIN2} voltage.	Table **12**

Table 87: *Analog data register 2.*

4.2.7.6 Analog data register 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								HAMB[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TAMB[11:0]											

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	–	0x00	Unused.	–
23 – 16	8	HAMB	0xFF	Ambient humidity.	**Raw** value in %.
15 – 12	4	–	0b0000	Unused.	–
11 – 0	12	TAMB	0x7FF	Ambient temperature.	Table **11**

Table 88: *Analog data register 3.*

4.2.7.7 Digital data register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DIO3		DIO2		DIO1		DIO0	

Bits	Size	Field	Reset value	Description	Format
31 – 8	24	–	0x000000	Unused.	–
7 – 6	2	DIO3	0b11	Digital input 3 state.	Table **9** **0b0** : low level **0b1** : high level
5 – 4	2	DIO2	0b11	Digital input 2 state.	Table **9** **0b0** : low level **0b1** : high level
3 – 2	2	DIO1	0b11	Digital input 1 state.	Table **9** **0b0** : low level **0b1** : high level
1 – 0	2	DIO0	0b11	Digital input 0 state.	Table **9** **0b0** : low level **0b1** : high level

Table 89: *Digital data register.*

4.2.8 RRM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	8	R	Table **91**	Compilation flags.
0x0A	CONFIGURATION_0	16	R/W	Table **92**	I_{OUT} offset calibration value.
0x0B	STATUS_1	8	R	Table **93**	Regulator status.
0x0C	CONTROL_1	8	R/W	Table **94**	Regulator control.
0x0D	ANALOG_DATA_1	32	R	Table **95**	V_{IN} and V_{OUT} voltages measurements.
0x0E	ANALOG_DATA_2	16	R	Table **96**	I_{OUT} current measurement.

Table 90: *RRM specific registers set.*

4.2.8.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
															RFH

Bits	Size	Field	Reset value	Description	Format
31 – 1	31	–	0b0[31]	Unused.	–
0	1	RFH	–	Regulator control mode (set at compilation step according to hardware).	**0b0** : Regulator controlled by the MCU. **0b1** : Regulator controlled by hardware.

Table 91: *Flags register 1.*

4.2.8.2 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOUT_OFFSET[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	IOUT_OFFSET	–	Output current offset calibration value.	Table **13**

Table 92: *Configuration register 0.*

4.2.8.3 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
														RENST	

Bits	Size	Field	Reset value	Description	Format
31 – 2	30	–	0b0[30]	Unused.	–
1 – 0	2	RENST	0b11	Regulator state.	Table **9** **0b00** : Regulator output disabled. **0b01** : Regulator output enabled.

Table 93: *Status register 1.*

4.2.8.4 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
															REN

Bits	Size	Field	Reset value	Description	Format
31 – 1	31	–	0b0[31]	Unused.	–
0	1	REN	0b0	Regulator state control.	**0b0** : disable regulator output. **0b1** : enable regulator output.

Table 94: *Control register 1.*

4.2.8.5 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VOUT[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VOUT	0xFFFF	Regulator output voltage.	Table **12**
15 – 0	16	VIN	0xFFFF	Regulator input voltage.	Table **12**

Table 95: *Analog data register 1.*

4.2.8.6 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOUT[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	IOUT	0xFFFF	Regulator output current.	Table **13**

Table 96: *Analog data register 2.*

4.2.9 DMM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	CONFIGURATION_0	32	R/W	Table **98**	Radio monitoring and nodes scan periods.
0x0A	STATUS_1	8	R	Table **99**	Nodes count.
0x0B	CONTROL_1	8	R/W	Table **100**	Nodes scan trigger flag.
0x0C	ANALOG_DATA_1	32	R	Table **101**	V_{RS} and V_{HMI} voltages measurements.
0x0D	ANALOG_DATA_2	16	R	Table **102**	V_{USB} voltage measurement.

Table 97: *DMM specific registers set.*

4.2.9.1 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								SIGFOX_DL_PERIOD[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIGFOX_UL_PERIOD[7:0]								NODES_SCAN_PERIOD[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	–	0x00	Unused.	–
23 – 16	8	SIGFOX_DL_PERIOD	–	Remote control period.	Table **10**
15 – 8	8	SIGFOX_UL_PERIOD	–	Remote monitoring period.	Table **10**
7 – 0	8	NODES_SCAN_PERIOD	–	Automatic nodes scan period.	Table **10**

Table 98: *Configuration register 0.*

4.2.9.2 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
								NODES_COUNT[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 8	24	–	0x000000	Unused.	–
7 – 0	8	NODES_COUNT	–	Number of nodes connected on the bus.	**Raw** value.

Table 99: *Status register 1.*

4.2.9.3 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															STRG

Bits	Size	Field	Reset value	Description	Format
31 – 1	31	–	0b0[31]	Unused.	–
0	1	STRG	0b0	Nodes scan trigger flag.	**0b0** : no action. **0b1** : start nodes scan. The bit is automatically cleared after the operation.

Table 100: *Control register 1.*

4.2.9.4 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VHMI[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VRS[15:0]															

Bits	Size	Field	Reset value	Description	Format
Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VHMI	0xFFFF	HMI voltage.	Table **12**
15 – 0	16	VRS	0xFFFF	RS485 bus power supply rail.	Table **12**

Table 101: *Analog data register 1.*

4.2.9.5 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VUSB[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	VUSB	0xFFFF	USB voltage.	Table **12**

Table 102: *Analog data register 2.*

4.2.10 MPMCM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	16	R	Table **104**	Transformer attenuation ratio.
0x0A	FLAGS_2	32	R	Table **105**	Current sensors attenuation ratio.
0x0B	CONFIGURATION_0	16	R/W	Table **106**	Transformer gain.
0x0C	CONFIGURATION_1	32	R/W	Table **107**	CH1 and CH2 current sensors gain.
0x0D	CONFIGURATION_2	32	R/W	Table **108**	CH3 and CH4 current sensors gain.
0x0E	CONFIGURATION_3	8	R/W	Table **109**	Linky TIC sampling period.
0x0F	STATUS_1	8	R	Table **110**	AC channels measurements status.
0x10	CONTROL_1	8	R/W	Table **111**	AC channels measurements control.
0x11	MAINS_FREQUENCY_0	32	R	Table **112**	Run and averaged mains frequency.
0x12	MAINS_FREQUENCY_1	32	R	Table **113**	Min and max mains frequency.
0x13	CH1_ACTIVE_POWER_0	32	R	Table **114**	CH1 run and averaged active power.
0x14	CH1_ACTIVE_POWER_1	32	R	Table **115**	CH1 min and max active power.
0x15	CH1_RMS_VOLTAGE_0	32	R	Table **116**	CH1 run and averaged RMS voltage.
0x16	CH1_RMS_VOLTAGE_1	32	R	Table **117**	CH1 min and max RMS voltage;
0x17	CH1_RMS_CURRENT_0	32	R	Table **118**	CH1 run and averaged RMS current.
0x18	CH1_RMS_CURRENT_1	32	R	Table **119**	CH1 min and max RMS current.
0x19	CH1_APPARENT_POWER_0	32	R	Table **120**	CH1 run and averaged apparent power.
0x1A	CH1_APPARENT_POWER_1	32	R	Table **121**	CH1 min and max apparent power.
0x1B	CH1_POWER_FACTOR_0	32	R	Table **122**	CH1 run and averaged power factor.
0x1C	CH1_POWER_FACTOR_1	32	R	Table **123**	CH1 min and max power factor.
0x1D	CH1_ENERGY	32	R	Table **124**	CH1 cumulated active and apparent energy.
0x1E – 0x28	*Same for* CH2				
0x29 – 0x33	*Same for* CH3				
0x34 – 0x3E	*Same for* CH4				
0x3F – 0x49	*Same for* TIC				

Table 103: *MPMCM specific registers set.*

Note: As far as active power, apparent power and power factor are concerned, when the sign changes during the accumulation period (switch between production and consumption modes), the maximum and minimum values correspond to the absolute minimum value and absolute maximum value observed during the accumulation period.

4.2.10.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRANSFORMER_ATTEN[7:0]													LTM	LTE	AME

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 8	8	TRANSFORMER_ATTEN	–	Transformer attenuation ratio (set at compilation step according to hardware).	**Raw** value in V/V.
7 – 3	5	–	0b0[5]	Unused.	–
2	1	LTM	–	Linky TIC mode.	**0b0** : Historic mode. **0b1** : Standard mode.
1	1	LTE	–	Linky TIC interface enable flag.	**0b0** : Linky TIC interface disabled. **0b1** : Linky TIC interface enabled.
0	1	AME	–	Analog measure enable.	**0b0** : Analog measure disabled. **0b1** : Analog measure enabled.

Table 104: *Flags register 1.*

4.2.10.2 Flags register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CH4_CURRENT_SENSOR_ATTEN[7:0]								CH3_CURRENT_SENSOR_ATTEN[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CH2_CURRENT_SENSOR_ATTEN[7:0]								CH1_CURRENT_SENSOR_ATTEN[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	CH4 CURRENT_SENSOR_ATTEN	–	CH4 current sensor attenuation ratio (set at compilation step according to hardware).	**Raw** value in V/V.
23 – 16	8	CH3 CURRENT_SENSOR_ATTEN	–	CH3 current sensor attenuation ratio (set at compilation step according to hardware).	**Raw** value in V/V.
15 – 8	8	CH2 CURRENT_SENSOR_ATTEN	–	CH2 current sensor attenuation ratio (set at compilation step according to hardware).	**Raw** value in V/V.
7 – 0	8	CH1 CURRENT_SENSOR_ATTEN	–	CH1 current sensor attenuation ratio (set at compilation step according to hardware).	**Raw** value in V/V.

Table 105: *Flags register 2.*

4.2.10.3 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRANSFORMER_GAIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 0	16	TRANSFORMER_GAIN	–	Transformer gain (between primary and secondary).	**Raw** value in $10 \times V/V$.

Table 106: *Configuration register 0.*

4.2.10.4 Configuration register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CH2_CURRENT_SENSOR_GAIN[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH1_CURRENT_SENSOR_GAIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CH2 CURRENT_SENSOR_GAIN	–	CH2 current sensor gain.	**Raw** value in $10 \times A/V$.
15 – 0	16	CH1 CURRENT_SENSOR_GAIN	–	CH1 current sensor gain.	**Raw** value in $10 \times A/V$.

Table 107: *Configuration register 1.*

4.2.10.5 Configuration register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CH4_CURRENT_SENSOR_GAIN[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH3_CURRENT_SENSOR_GAIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CH4 CURRENT_SENSOR_GAIN	–	CH4 current sensor gain.	**Raw** value in $10 \times A/V$.
15 – 0	16	CH3 CURRENT_SENSOR_GAIN	–	CH3 current sensor gain.	**Raw** value in $10 \times A/V$.

Table 108: *Configuration register 2.*

4.2.10.6 Configuration register 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								TIC_SAMPLING_PERIOD[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 8	24	–	0x000000	Unused.	–
7 – 0	8	TIC_SAMPLING_PERIOD	–	Linky TIC sampling period.	Table **10**

Table 109: *Configuration register 3.*

4.2.10.7 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
										MVD	TICD	CH4D	CH3D	CH2D	CH1D

Bits	Size	Field	Reset value	Description	Format
31 – 6	26	–	0b0[26]	Unused.	–
5	1	MVD	0b0	Mains voltage detect flag.	**0b0** : mains voltage not detected **0b1** : mains voltage detected
4	1	TICD	0b0	Linky TIC detect flag.	**0b0** : Linky TIC not detected **0b1** : Linky TIC detected
3	1	CH4D	0b0	AC channel 4 current sensor detect flag.	**0b0** : sensor not connected **0b1** : sensor connected
2	1	CH3D	0b0	AC channel 3 current sensor detect flag.	**0b0** : sensor not connected **0b1** : sensor connected
1	1	CH2D	0b0	AC channel 2 current sensor detect flag.	**0b0** : sensor not connected **0b1** : sensor connected
0	1	CH1D	0b0	AC channel 1 current sensor detect flag.	**0b0** : sensor not connected **0b1** : sensor connected

Table 110: *Status register 1.*

4.2.10.8 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
										FRQS	TICS	CH4S	CH3S	CH2S	CH1S

Bits	Size	Field	Reset value	Description	Format
31 – 6	26	–	0b0[26]	Unused.	–
5	1	FRQS	0b0	Mains frequency measurements control.	**0b0** : no action **0b1** : store frequency measurements in registers and reset them
4	1	TICS	0b0	TIC measurements control.	**0b0** : no action **0b1** : store TIC measurements in registers and reset them
3	1	CH4S	0b0	AC channel 4 measurements control.	**0b0** : no action **0b1** : store all CH4 measurements in registers and reset them
2	1	CH3S	0b0	AC channel 3 measurements control.	**0b0** : no action **0b1** : store all CH3 measurements in registers and reset them
1	1	CH2S	0b0	AC channel 2 measurements control.	**0b0** : no action **0b1** : store all CH2 measurements in registers and reset them
0	1	CH1S	0b0	AC channel 1 measurements control.	**0b0** : no action **0b1** : store all CH1 measurements in registers and reset them

Table 111: *Control register 1.*

4.2.10.9 Mains frequency register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAINS_FREQUENCY_MEAN[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAINS_FREQUENCY_RUN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	MAINS_FREQUENCY_MEAN	0xFFFF	Averaged value of mains frequency since last measurements reset.	**Raw** value in cHz.
15 – 0	16	MAINS_FREQUENCY_RUN	0xFFFF	Averaged value of mains frequency during last second.	**Raw** value in cHz.

Table 112: *Mains frequency register 0.*

4.2.10.10 Mains frequency register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAINS_FREQUENCY_MAX[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAINS_FREQUENCY_MIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	MAINS_FREQUENCY_MAX	0xFFFF	Maximum value of mains frequency since last measurements reset.	**Raw** value in cHz.
15 – 0	16	MAINS_FREQUENCY_MIN	0xFFFF	Minimum value of mains frequency since last measurements reset.	**Raw** value in cHz.

Table 113: *Mains frequency register 1.*

4.2.10.11 CHx active power register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_ACTIVE_POWER_MEAN[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_ACTIVE_POWER_RUN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_ACTIVE_POWER_MEAN	0x7FFF	Averaged value of active power since last measurements reset.	Table **14**
15 – 0	16	CHx_ACTIVE_POWER_RUN	0x7FFF	Averaged value of active power during last second.	Table **14**

Table 114: *CHx active power register 0.*

4.2.10.12 CHx active power register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_ACTIVE_POWER_MAX[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_ACTIVE_POWER_MIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_ACTIVE_POWER_MAX	0x7FFF	Maximum value of active power since last measurements reset.	Table **14**
15 – 0	16	CHx_ACTIVE_POWER_MIN	0x7FFF	Minimum value of active power since last measurements reset.	Table **14**

Table 115: *CHx active power register 1.*

4.2.10.13 CHx RMS voltage register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_RMS_VOLTAGE_MEAN[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_RMS_VOLTAGE_RUN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_RMS_VOLTAGE_MEAN	0xFFFF	Averaged value of RMS voltage since last measurements reset.	Table **12**
15 – 0	16	CHx_RMS_VOLTAGE_RUN	0xFFFF	Averaged value of RMS voltage during last second.	Table **12**

Table 116: *CHx RMS voltage register 0.*

4.2.10.14 CHx RMS voltage register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_RMS_VOLTAGE_MAX[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_RMS_VOLTAGE_MIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_RMS_VOLTAGE_MAX	0xFFFF	Maximum value of RMS voltage since last measurements reset.	Table **12**
15 – 0	16	CHx_RMS_VOLTAGE_MIN	0xFFFF	Minimum value of RMS voltage since last measurements reset.	Table **12**

Table 117: *CHx RMS voltage register 1.*

4.2.10.15 CHx RMS current register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_RMS_CURRENT_MEAN[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_RMS_CURRENT_RUN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_RMS_CURRENT_MEAN	0xFFFF	Averaged value of RMS current since last measurements reset.	Table **12**
15 – 0	16	CHx_RMS_CURRENT_RUN	0xFFFF	Averaged value of RMS current during last second.	Table **12**

Table 118: *CHx RMS current register 0.*

4.2.10.16 CHx RMS current register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_RMS_CURRENT_MAX[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_RMS_CURRENT_MIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_RMS_CURRENT_MAX	0xFFFF	Maximum value of RMS current since last measurements reset.	Table **12**
15 – 0	16	CHx_RMS_CURRENT_MIN	0xFFFF	Minimum value of RMS current since last measurements reset.	Table **12**

Table 119: *CHx RMS current register 1.*

4.2.10.17 CHx apparent power register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_APPARENT_POWER_MEAN[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_APPARENT_POWER_RUN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_APPARENT_POWER_MEAN	0x7FFF	Averaged value of apparent power since last measurements reset.	Table **14**
15 – 0	16	CHx_APPARENT_POWER_RUN	0x7FFF	Averaged value of apparent power during last second.	Table **14**

Table 120: *CHx apparent power register 0.*

4.2.10.18 CHx apparent power register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_APPARENT_POWER_MAX[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_APPARENT_POWER_MIN[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_APPARENT_POWER_MAX	0x7FFF	Maximum value of apparent power since last measurements reset.	Table **14**
15 – 0	16	CHx_APPARENT_POWER_MIN	0x7FFF	Minimum value of apparent power since last measurements reset.	Table **14**

Table 121: *CHx apparent power register 1.*

4.2.10.19 CHx power factor register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								CHx_POWER_FACTOR_MEAN[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								CHx_POWER_FACTOR_RUN[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	–	0x00	Unused.	–
24 – 16	8	CHx_POWER_FACTOR_MEAN	0x7F	Averaged value of power factor since last measurements reset.	Table **16**
15 – 8	8	–	0x00	Unused.	–
7 – 0	8	CHx_POWER_FACTOR_RUN	0x7F	Averaged value of power factor during last second.	Table **16**

Table 122: *CHx power factor register 0.*

4.2.10.20 CHx power factor register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								CHx_POWER_FACTOR_MAX[7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								CHx_POWER_FACTOR_MIN[7:0]							

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	–	0x00	Unused.	–
23 – 16	8	CHx_POWER_FACTOR_MAX	0x7F	Maximum value of power factor since last measurements reset.	Table **16**
15 – 8	8	–	0x00	Unused.	–
7 – 0	8	CHx_POWER_FACTOR_MIN	0x7F	Minimum value of power factor since last measurements reset.	Table **16**

Table 123: *CHx power factor register 1.*

4.2.10.21 CHx energy register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHx_APPARENT_ENERGY[15:0]															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHx_ACTIVE_ENERGY[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CHx_APPARENT_ENERGY	0x0000	Accumulated apparent energy since last measurements reset.	Table **15**
15 – 0	16	CHx_ACTIVE_ENERGY	0x0000	Accumulated active energy since last measurements reset.	Table **15**

Table 124: *CHx energy register.*

4.2.11 BCM specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x09	FLAGS_1	16	R	Table **126**	Compilation flags.
0x0A	CONFIGURATION_0	32	R/W	Table **127**	CHEN threshold and toggle period.
0x0B	CONFIGURATION_1	32	R/W	Table **128**	Low voltage flag (LVF) thresholds.
0x0C	CONFIGURATION_2	32	R/W	Table **129**	Critical voltage flag (CVF) thresholds.
0x0D	STATUS_1	16	R	Table **130**	Charging and backup status.
0x0E	CONTROL_1	8	R/W	Table **132**	Charging and backup control.
0x0F	ANALOG_DATA_1	32	R	Table **133**	V_{SRC} and V_{STR} voltages measurements.
0x10	ANALOG_DATA_2	32	R	Table **134**	V_{BKP} voltage and I_{STR} current measurements.

Table 125: *BCM specific registers set.*

4.2.11.1 Flags register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHUNT_RESISTOR												BKFH	CLFH	CSFH	CEFH

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 8	8	SHUNT_RESISTOR	–	LTC4013 shunt resistor value.	**Raw** value in $m\Omega$.
7 – 4	4	–	0x0	Unused.	–
3	1	BKFH	–	Backup output control mode (set at compilation step according to hardware).	**0b0** : Backup output controlled by the MCU. **0b1** : Backup output controlled by hardware.
2	1	CLFH	–	LED control mode (set at compilation step according to hardware).	**0b0** : LED controlled by the MCU. **0b1** : LED controlled by hardware.
1	1	CSFH	–	Charge status mode (set at compilation step according to hardware).	**0b0** : Charge status connected to the MCU. **0b1** : Charge status connected in hardware.
0	1	CEFH	–	Charge control mode (set at compilation step according to hardware).	**0b0** : Charge controlled by the MCU. **0b1** : Charge controlled by hardware.

Table 126: *Flags register 1.*

4.2.11.2 Configuration register 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								CHEN_TOGGLE_PERIOD							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHEN_THRESHOLD															

Bits	Size	Field	Reset value	Description	Format
31 – 24	8	–	0x00	Unused.	–
23 – 16	8	CHEN_TOGGLE_PERIOD	–	Charge toggle period.	Table **10**
15 – 0	16	CHEN_THRESHOLD	–	Voltage threshold to set CHEN bit.	Table **12**

Table 127: *Configuration register 0.*

Note: this register is only used when CHMD = 0b1 and CEFH = 0b0.

4.2.11.3 Configuration register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LVF_HIGH_THRESHOLD															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LVF_LOW_THRESHOLD															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	LVF_HIGH_THRESHOLD	–	High threshold of the LVF voltage hysteresis.	Table **12**
15 – 0	16	LVF_LOW_THRESHOLD	–	Low threshold of the LVF voltage hysteresis.	Table **12**

Table 128: *Configuration register 1.*

4.2.11.4 Configuration register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CVF_HIGH_THRESHOLD															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CVF_LOW_THRESHOLD															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	CVF_HIGH_THRESHOLD	–	High threshold of the CVF voltage hysteresis.	Table **12**
15 – 0	16	CVF_LOW_THRESHOLD	–	Low threshold of the CVF voltage hysteresis.	Table **12**

Table 129: *Configuration register 2.*

4.2.11.5 Status register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
						CVF	LVF	CHRGST1		CHRGST0		CHENST		BKENST	

Bits	Size	Field	Reset value	Description	Format
31 – 10	22	–	0b0[22]	Unused.	–
9	1	CVF	0b0	Critical voltage detector flag.	**0b0** : battery voltage is above the critical threshold. **0b1** : battery voltage is under the critical threshold.
8	1	LVF	0b0	Low voltage detector flag.	**0b0** : battery voltage is above the low threshold. **0b1** : battery voltage is under the low threshold.
7 – 6	2	CHRGST1	0b11	Battery charging status 1.	Table **9** See table **131** for bit meaning.
5 – 4	2	CHRGST0	0b11	Battery charging status 0.	Table **9** See table **131** for bit meaning.
3 – 2	2	CHENST	0b11	Battery charging enable status.	Table **9** **0b00** : charge disabled. **0b01** : charge enabled.
1 – 0	2	BKENST	0b11	Backup output state.	Table **9** **0b00** : backup output disabled. **0b01** : backup output enabled.

Table 130: *Status register 1.*

CHRGST1	CHRGST0	Charge status
0b0	**0b0**	Not charging or terminated
0b0	**0b1**	Constant current charging (CC)
0b1	**0b1**	Constant voltage charging (CV)
0b1	**0b0**	Low battery or thermal shutdown fault

Table 131: *BCM charge status bits.*

4.2.11.6 Control register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
													CHEN	CHMD	BKEN

Bits	Size	Field	Reset value	Description	Format
31 – 3	29	–	0b0[29]	Unused.	–
2	1	CHEN	0b0	Battery charging control (only if CHMD = 0b1 and CEFH = 0b0).	**0b0** : disable charge. **0b1** : enable charge.
1	1	CHMD	0b0	Battery charging mode.	**0b0** : charge is automatically controlled by software. **0b1** : charge is controlled by the CHEN bit.
0	1	BKEN	0b0	Backup output control.	**0b0** : disable backup output. **0b1** : enable backup output.

Table 132: *Control register 1.*

4.2.11.7 Analog data register 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VSTR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSRC[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	VSTR	0xFFFF	Battery voltage.	Table **12**
15 – 0	16	VSRC	0xFFFF	Source voltage.	Table **12**

Table 133: *Analog data register 1.*

4.2.11.8 Analog data register 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ISTR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBKP[15:0]															

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	ISTR	0xFFFF	Battery charge current.	Table **13**
15 – 0	16	VBKP	0xFFFF	Backup voltage.	Table **12**

Table 134: *Analog data register 2.*

4.3 External nodes

4.3.1 R4S8CR specific registers set

REG_ADDR	Register name	Size	Access	Format	Description
0x00	STATUS	16	R	Table **136**	Relays status.
0x01	CONTROL	8	R/W	Table **137**	Relays control.

Table 135: *R4S8CR registers set.*

4.3.1.1 Status register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R8STST		R7STST		R6STST		R5STST		R4STST		R3STST		R2STST		R1STST	

Bits	Size	Field	Reset value	Description	Format
31 – 16	16	–	0x0000	Unused.	–
15 – 14	2	R8STST	0b11	Relay 8 state.	Table **9** **0b0** : NC path closed **0b1** : NO path closed
13 – 12	2	R7STST	0b11	Relay 7 status.	
11 – 10	2	R6STST	0b11	Relay 6 status.	
9 – 8	2	R5STST	0b11	Relay 5 status.	
7 – 6	2	R4STST	0b11	Relay 4 status.	
5 – 4	2	R3STST	0b11	Relay 3 status.	
3 – 2	2	R2STST	0b11	Relay 2 status.	
1 – 0	2	R1STST	0b11	Relay 1 status.	

Table 136: *Status register.*

4.3.1.2 Control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								R8ST	R7ST	R6ST	R5ST	R4ST	R3ST	R2ST	R1ST

Bits	Size	Field	Reset value	Description	Format
31 – 8	24	–	0x000000	Unused.	–
7	1	R8ST	0b0	Relay 8 state.	**0b0** : close NC path **0b1** : close NO path
6	1	R7ST	0b0	Relay 7 state.	
5	1	R6ST	0b0	Relay 6 state.	
4	1	R5ST	0b0	Relay 5 state.	
3	1	R4ST	0b0	Relay 4 state.	
2	1	R3ST	0b0	Relay 3 state.	
1	1	R2ST	0b0	Relay 2 state.	
0	1	R1ST	0b0	Relay 1 state.	

Table 137: *Control register.*

4.4 Bus enumeration

Thanks to the node addressing system and the read commands, the master module is able to enumerate dynamically all the slaves nodes attached to the RS485 bus.

4.4.1 DINFox nodes

For each `NODE_ADDR` between **0x00** and **0x6F**, the master uses the UNA-AT protocol at 1200 bauds and reads the common `NODE_ID` register (see section **4.2.1.1**). If a data is received, the master stores the address and the `BOARD_ID` (directly read in the reply) in its nodes list.

4.4.2 External nodes

4.4.2.1 KMTronic R4S8CR

For each `NODE_ADDR` between **0x70** and **0x7E**, the master uses the KMTronic protocol at 9600 bauds and reads the relays state. If a data is received, the master stores the address in its nodes list.

5 Radio link description

A DINFox system can be remotely monitored or controlled thanks to the **UHFM** node, which features a long-range bidirectional radio interface using **Sigfox** technology.

5.1 RF performances

The **UHFM HW1.0** has an RF front-end composed of a sub-GHz transceiver, a discrete RX LNA, a discrete TX filter, a diode switch and a common antenna connector. The next table recaps its characteristics.

Parameter	Condition	Min	Typ	Max	Unit
RF output power	$V_{RS} = 5\,V$, continuous wave at 868.13 MHz		14		dBm
TX current			32		mA
TX current	$V_{RS} = 5\,V$, Sigfox uplink frame at 868.13 MHz		26		mA
RF sensitivity	$V_{RS} = 5\,V$, Sigfox downlink frame at 869.525 MHz		-128		dBm
RX current			16		mA

Table 138: *UHFM HW1.0 characteristics.*

5.2 Remote monitoring (uplink)

The remote monitoring is performed via the Sigfox uplink mechanism, which is periodically initiated by the DINFox system. One uplink operation sends the data of one node.

The payload starts with a 2 bytes header composed of the address of the node (`NODE_ADDR`) and its board ID (`BOARD_ID`) which uniquely identifies the node within the DINFox system. The remaining bytes (1 to 10) contain the node data, whose format depends on the board ID.

B0	B1	B2 .. Bn (2 to 11)
`NODE_ADDR`	`BOARD_ID`	`DATA` (depends on board ID)

Table 139: *Uplink payload format.*

This format has several advantages:

- By containing the board ID, the frame is self-sufficient: on the server side, the parser can decode any UL payload without knowing the nodes address mapping (which is dynamically enumerated by the DINFox system itself, not the server).
- The UL payload length can be optimized for a given board ID. Indeed, the number of data for a given node is fixed. A more generic format with register address and value would have been less efficient in term of bytes count.
- Frame formats which where already defined from other Sigfox projects can be reused, such as the startup frame or the error stack, improving the code factorization on the server side.

When multiple uplink payload formats have to be defined for a same module (same board ID), the **UL payload size** is used as distinguishing criteria.

The `DATA` field format is described in each node driver, implemented in the master embedded software: https://github.com/Ludovic-Lesur/dmm/tree/master/middleware/radio/src.

5.3 Remote control (downlink)

The remote control is performed via the Sigfox downlink mechanism, which is periodically initiated by the DINFox system. One downlink operation controls one or two nodes. Contrary to the uplink, a more generic interface was defined by accessing the node registers, since the DL payload length is fixed.

The 8 bytes of the payload starts with a 1 byte header containing an operation code (`OP_CODE`) which defines the action to perform on the node(s). The remaining bytes contain optional dynamic data, whose format depends on the operation code.

B0	B1	B2	B3	B4	B5	B6	B7
`OP_CODE`	`DATA` (depends on operation code)						

Table 140: *Downlink payload format.*

Since the `DATA` field is limited to 7 bytes, some operation codes have a limited access range regarding the register size that can be accessed. However most of writable registers are 8 bits long and are fully supported by all operation codes.

`OP_CODE`	Operation	Number of nodes	Number of registers	8 bits registers	16 bits registers	32 bits registers	Format
0x00	No-operation (NOP)	–	–	–	–	–	Table **142**
0x01	Single full read	1	1	✓	✓	✓	Table **143**
0x02	Single full write	1	1	✓	✓	✓	Table **144**
0x03	Single masked write	1	1	✓	✓	✗	Table **145**
0x04	Temporary full write	1	1	✓	✓	✓	Table **146**
0x05	Temporary masked write	1	1	✓	✓	✗	Table **147**
0x06	Successive full write	1	1	✓	✓	✗	Table **148**
0x07	Successive masked write	1	1	✓	✗	✗	Table **149**
0x08	Dual full write	1	2	✓	✓	✗	Table **150**
0x09	Triple full write	1	3	✓	✗	✗	Table **151**
0x0A	Dual node write	2	1	✓	✗	✗	Table **152**

Table 141: *Downlink operation codes.*

5.3.1 No-operation (NOP)

The NOP operation should be used when a downlink is requested by the DINFox system but there is none action to perform. In terms of power consumption, it is better to send a NOP operation instead of sending nothing, because the radio modem will remain in RX state less time.

B0	B1	B2	B3	B4	B5	B6	B7
0x00							

Table 142: *NOP operation DL payload format.*

5.3.2 Single full read

This operation reads one 32 bits register. The register value will be sent in the dedicated uplink action log message of the master board.

B0	B1	B2	B3	B4	B5	B6	B7
0x01	NODE_ADDR	REG_ADDR					

Table 143: *Single full read operation DL payload format.*

5.3.3 Single full write

This operation writes a value in one 32 bits register.

B0	B1	B2	B3	B4	B5	B6	B7
0x02	NODE_ADDR	REG_ADDR	REG_VALUE				

Table 144: *Single full write operation DL payload format.*

5.3.4 Single masked write

This operation writes a value in a subpart of a 16 bits register defined by a mask.

B0	B1	B2	B3	B4	B5	B6	B7
0x03	NODE_ADDR	REG_ADDR	REG_MASK		REG_VALUE		

Table 145: *Single masked write operation DL payload format.*

5.3.5 Temporary full write

This operation writes a value in one 32 bits register during a specified duration, and then comes back to the previous (read before downlink operation). The DURATION field follows the time byte format (see table **10**).

B0	B1	B2	B3	B4	B5	B6	B7
0x04	NODE_ADDR	REG_ADDR	REG_VALUE				DURATION

Table 146: *Temporary full write operation DL payload format.*

5.3.6 Temporary masked write

This operation writes a value in a subpart of a 16 bits register defined by a mask, during a specified duration, and then comes back to the previous (read before downlink operation). The DURATION field follows the time byte format (see table **10**).

B0	B1	B2	B3	B4	B5	B6	B7
0x05	NODE_ADDR	REG_ADDR	REG_MASK		REG_VALUE		DURATION

Table 147: *Temporary masked write operation DL payload format.*

5.3.7 Successive full write

This operation performs two successive full write operations spaced by a given duration. The `DURATION` field follows the time byte format (see table **10**).

B0	B1	B2	B3	B4	B5	B6	B7
0x06	NODE_ADDR	REG_ADDR	REG_VALUE_1		REG_VALUE_2		DURATION

Table 148: *Successive full write DL payload format.*

5.3.8 Successive masked write

This operation performs two successive masked write operations spaced by a given duration. The `DURATION` field follows the time byte format (see table **10**).

B0	B1	B2	B3	B4	B5	B6	B7
0x07	NODE_ADDR	REG_ADDR	REG_MASK	REG_VALUE_1	REG_VALUE_2	DURATION	

Table 149: *Successive masked write DL payload format.*

5.3.9 Dual full write

This operation performs 2 independent full write operation on two 16 bits registers.

B0	B1	B2	B3	B4	B5	B6	B7
0x08	NODE_ADDR	REG_1_ADDR	REG_1_VALUE		REG_2_ADDR	REG_2_VALUE	

Table 150: *Dual full write operation DL payload format.*

5.3.10 Triple full write

This operation performs 3 independent full write operation on three 8 bits registers.

B0	B1	B2	B3	B4	B5	B6	B7
0x09	NODE_ADDR	REG_1_ADDR	REG_1_VALUE	REG_2_ADDR	REG_2_VALUE	REG_3_ADDR	REG_3_VALUE

Table 151: *Triple full write operation DL payload format.*

5.3.11 Dual node write

This operation performs 2 independent full write operation on two 8 bits registers of two different nodes.

B0	B1	B2	B3	B4	B5	B6	B7
0x0A	NODE_1_ADDR	REG_1_ADDR	REG_1_VALUE	NODE_2_ADDR	REG_2_ADDR	REG_2_VALUE	

Table 152: *Dual node write operation DL payload format.*

6 Embedded software

6.1 DINFox master node (DMM)

The master node embedded software is hosted on GitHub: https://github.com/Ludovic-Lesur/dmm. As shown in the diagram below, the code is structured in such a way that all slaves node are accessed through a common interface (`node.h` header file). From low to high layers, the architecture is composed of:

- the **common physical layer** (RS485 bus) handled by the LPUART peripheral.
- the specific **slave nodes drivers**, using the **LMAC** and the **UNA-AT** protocols for the DINFox nodes.
- a **common node interface** to write and read registers of all slave nodes (**UNA framework** implementation).
- the **human machine interface (HMI)** layer which handles the local user interface (screen, buttons and switches) and defines the data printing format for each node.
- the **radio** layer which defines the uplink messages format for each node and implements the downlink operation codes.
- the main **application** which calls the HMI and the radio drivers.

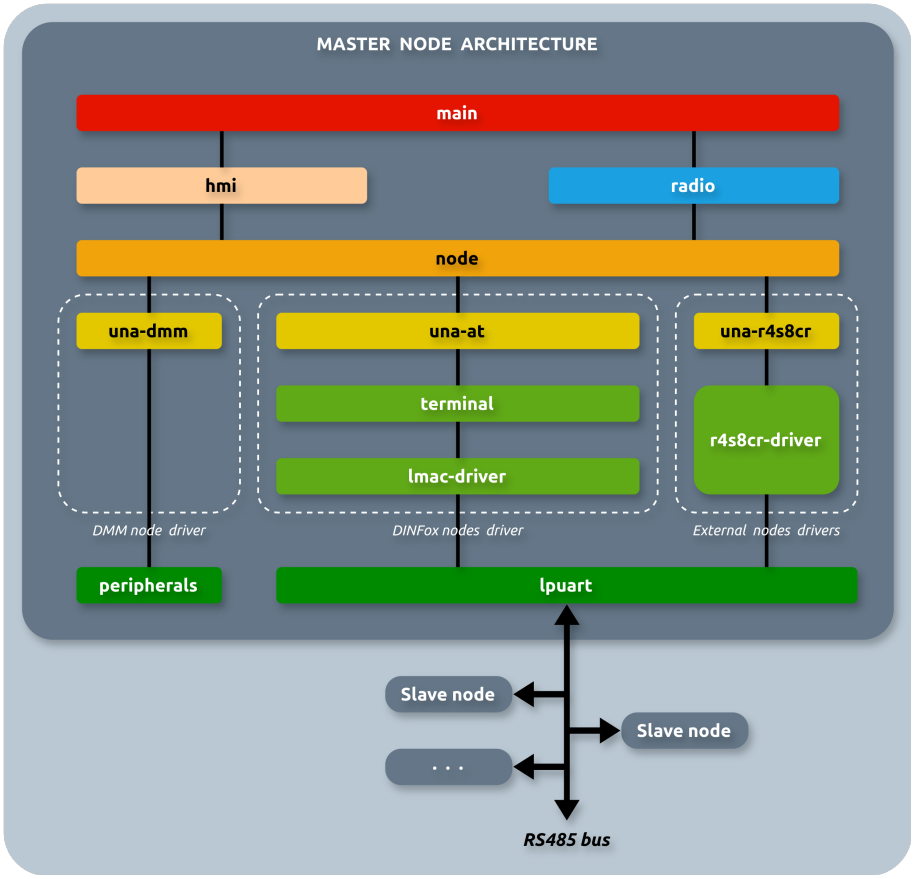

Figure 4: *Simplified architecture of the master embedded software.*

6.2 DINFox slave nodes (DSM)

The slave nodes embedded software is hosted on GitHub: https://github.com/Ludovic-Lesur/dsm. As shown in the diagram below, the code is structured in such a way that all registers are accessed through a common interface (`node.h` header file). From low to high layers, the architecture is composed of:

- the **common physical layer** (RS485 bus) handled by the LPUART peripheral.
- the **LMAC driver** which manages the network layer.
- the **AT** and **UNA-AT** drivers which are responsible for command parsing and execution.
- a **common node interface** to write and read registers of all slave nodes (**UNA framework** implementation). Contrary to the master node where all slaves have to be dynamically supported, the node is here selected at compilation level with macros (build configuration), since the final code will be flashed on 1 defined slave.
- the main **application** which calls the command line task continuously.

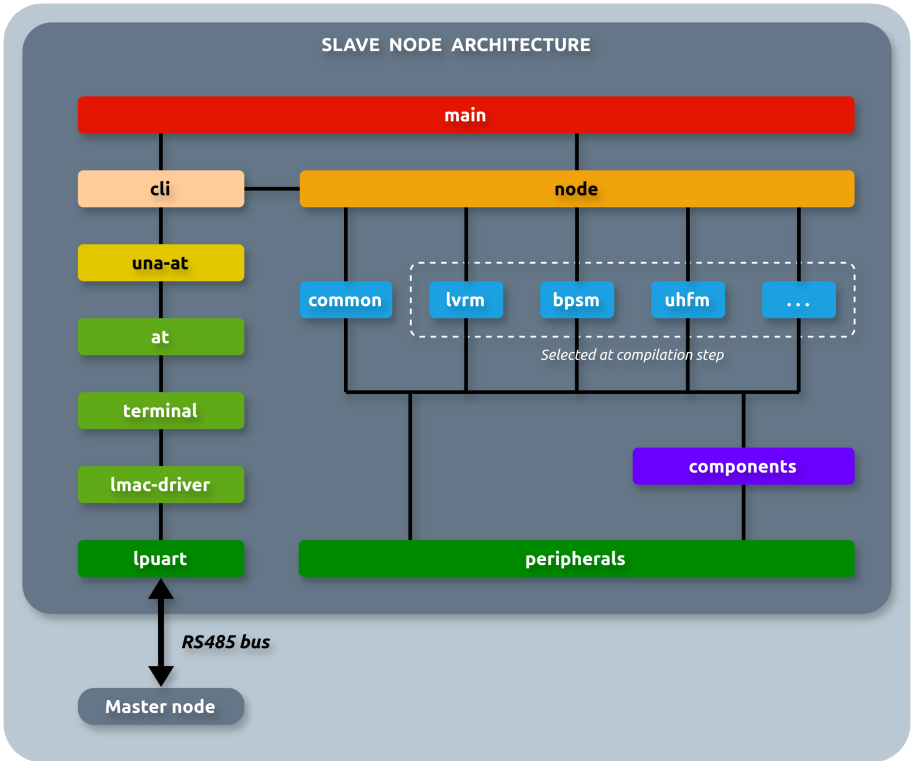

Figure 5: *Simplified architecture of the slave embedded software.*

7 Hardware design

7.1 Power supply

DINFox nodes have been designed to achieve a very low power consumption, in order to be compatible with backup power systems. As shown in the below power tree, DINFox nodes are usually powered by two parallel sources:

- the power input (V_{SRC}, V_{IN}, V_{COM}, etc...), generally a high voltage source but not always present.
- the bus voltage rail V_{RS}, typically provided by a **BPSM** or a **BCM** module connected to an energy storage element, in order to keep a backup voltage for all nodes when the power input is not available.

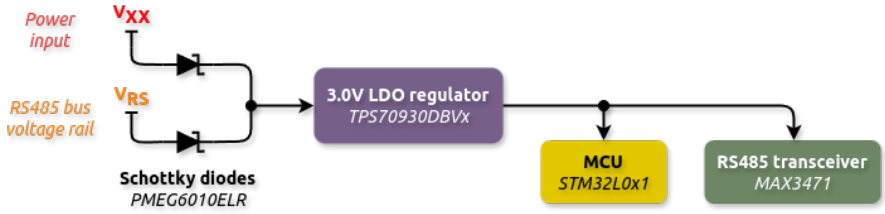

Figure 6: *Simplified power tree of DINFox nodes.*

Powering a node by its power input has two advantages:

- The node does not drain current from the backup source V_{RS} when the high voltage is available.
- Avoid pseudo-powering issues of the MCU via the ADC pins, as there are some direct voltage dividers on the power input and output for monitoring.

Since most of the nodes monitor the power input, they can determine if they are currently powered by the power input or by the backup rail V_{RS}. Therefore, they can adjust their behavior accordingly to reduce the power consumption (ADC conversions period, enable LED blinking, etc...).

7.1.1 LDO regulator

In order to optimize the power consumption, a very low quiescent current LDO regulator has to be chosen to power the MCU and the RS485 transceiver, which is always in reception on slaves nodes. The regulator must also withstand the high voltage input when available (up to $28\,V$). The TPS709 regulator from Texas Instruments is an ideal reference and has been selected for all the boards (**TPS70930DBVx**, $3.0\,V$ output in SOT23-5 package).

Parameter	Condition	Min	Typ	Max	Unit
Input voltage	–	2.7		30.0	V
Output current	–			150	mA
Quiescent current	$I_{OUT} = 0\,mA$		1.4	2.25	μA
	$I_{OUT} = 150\,mA$		350		μA
Dropout voltage	$I_{OUT} = 50\,mA$		295	650	mV
	$I_{OUT} = 150\,mA$		960	1400	mV

Table 153: *TPS70930DBVx LDO regulator characteristics.*

Warning: whereas the regulator supports $30\,V$, the enable input of the TPS709 is limited to $6.5\,V$. As a consequence, when this regulator is not controlled and always on (for the MCU and the RS485 transceiver) the enable input must not be tied to the input but left floating: there is an internal pull-up that will ensure the regulator is on, with the right logic voltage whatever the input voltage.

7.1.2 Schottky diodes

Schottky diodes perform the OR operation between the power input and V_{RS}, by naturally selecting the highest voltage as source. Caution must be taken on the **reverse current**: indeed, when one of the voltage inputs is not available (especially the power input), an extra leakage current is drained by the second diode which is in reverse state. Some Schottky diodes have an excellent low forward voltage (main characteristic of these diodes) but a very poor reverse current (tens of μA) which drastically increase the node power consumption in idle mode. Also, the reverse voltage has to be higher than the power input maximum voltage ($28\,V$).

Taken these parameters into account, the **PMEG6010ELR** reference from Nexperia was chosen for all the boards.

Parameter	Condition	Min	Typ	Max	Unit
Average forward current	–			1.0	A
Reverse voltage	–			60	V
Forward voltage	$I_F = 1\,A$		605	660	mV
Reverse current	$V_R = 60\,V$		90	300	nA

Table 154: *PMEG6010ELR Schottky diode characteristics.*

7.1.3 MCU

Most of slave nodes are based on the **STM32L0x1** MCU. Thanks to the LPUART peripheral clocked on the external $32.768\,kHz$ quartz, the MCU is able to stay in **stop mode** while waiting for commands with address match feature. Since there are only static measures to do, the core is only woken-up when a command is sent to the node address (and periodically to clear the internal watchdog).

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage	–	1.65		3.6	V
MCU current in stop mode	–		1.5		μA

Table 155: *STM32L0x1 characteristics.*

The **MPMCM** is an exception regarding power consumption. This node performs mains voltage measurements which require continuous AC data acquisition and processing. It is based on a **STM32G4x1** MCU which is more powerful than a **STM32L0x1**. The LPUART peripheral has the same wake-up features, but the MCU is not put in stop mode when measuring (only when the mains voltage is not present).
As a consequence, this node continuously drains a high current. But power consumption is not a constraint in this case, because the node is indirectly powered by the mains voltage instead of the backup voltage V_{RS}.

7.1.4 RS485 transceiver

There are lots of RS485 transceiver references, but only few of them are low power. In particular, the **MAX3471** of Maxims Integrated is one of the best part regarding power consumption: it can be powered by a $3.0\,V$ supply and drains less than $2\,\mu A$ in reception mode, whereas other transceivers drain hundreds of μA, even few mA.

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage	–	2.5		5.5	V
RX current	$V_{CC} < 3.6\,V$		1.6	2.0	μA
TX current	$V_{CC} < 3.6\,V$		50	60	μA

Table 156: *MAX3471 characteristics.*

7.1.5 VRS voltage

Due to the drop-out voltages of the LDO regulator ($1400\,mV$ maximum) and the Schottky diodes ($660\,mV$ maximum), the minimum supply voltage of the DINFox node is $V_{RS} = 5\,V$.

Parameter	Condition	Min	Typ	Max	Unit
V_{RS}	–	5.0		28	V

Table 157: V_{RS} *characteristics.*

Note: if powering the nodes with their power inputs is not required, it is possible to remove the diodes, select a lower input voltage LDO regulator which will have a lower drop-out (such as TPS782, TPS7A05, etc...) and thus reduce V_{RS} to 3.6V. But in this case, **caution must be taken with the voltage dividers which are directly connected to the MCU**: either disconnect them or ensure that V_{RS} is always present.

7.1.6 Power consumption

Regarding the overall power consumption of a DINFox system, the most critical parameter is the RX current, because slave nodes are continuously listening on the RS485 bus to wait for commands. Thanks to the previous components selection, a slave node in continuous reception drains less than $5\,\mu A$ (except for **MPMCM** node).

Parameter	Condition	Min	Typ	Max	Unit
Diode reverse current	–		90		nA
LDO quiescent current	–		1.4		μA
MCU current in stop mode	–		1.5		μA
RS485 transceiver RX current	–		1.6		μA
Node overall RX current	–		4.5		μA

Table 158: *DINFox slave node overall RX current.*

7.2 Mechanical specification

As shown in the next drawing, DINFox nodes have been designed to be mounted on a **DIN rail**. They have a common height of 70 mm and a variable width expressed in the standard U unit (multiple of 17.6 mm).

The RS485 interface described in section **3.2.1** is exposed on a male connector on the left edge and a female connector on the right edge, so that the modules can be **stacked side by side** without any wire.

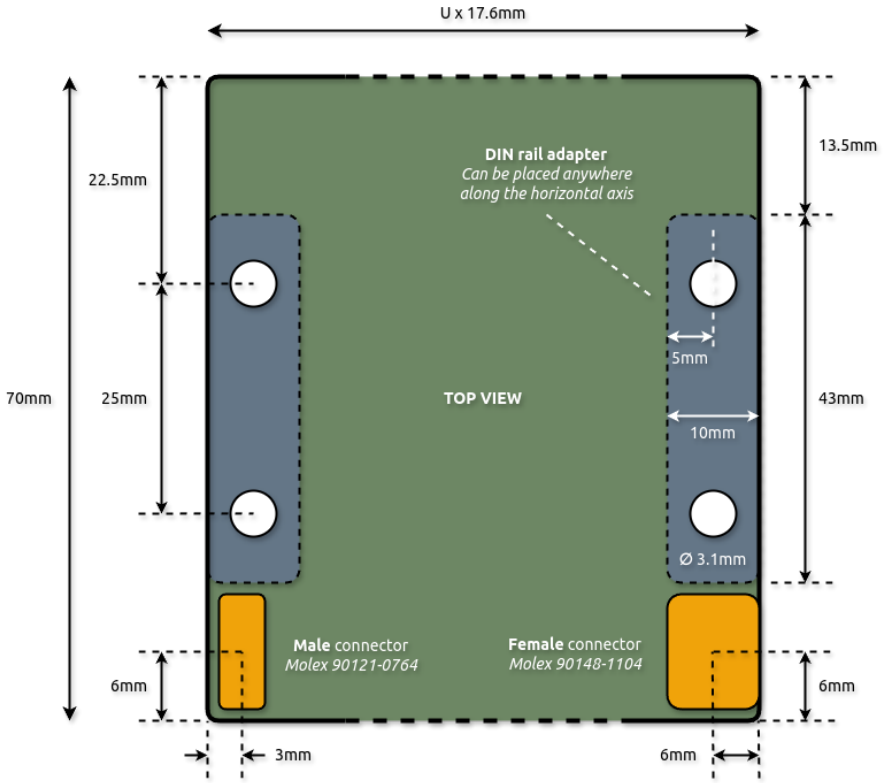

Figure 7: *Mechanical dimensions of a DINFox node.*