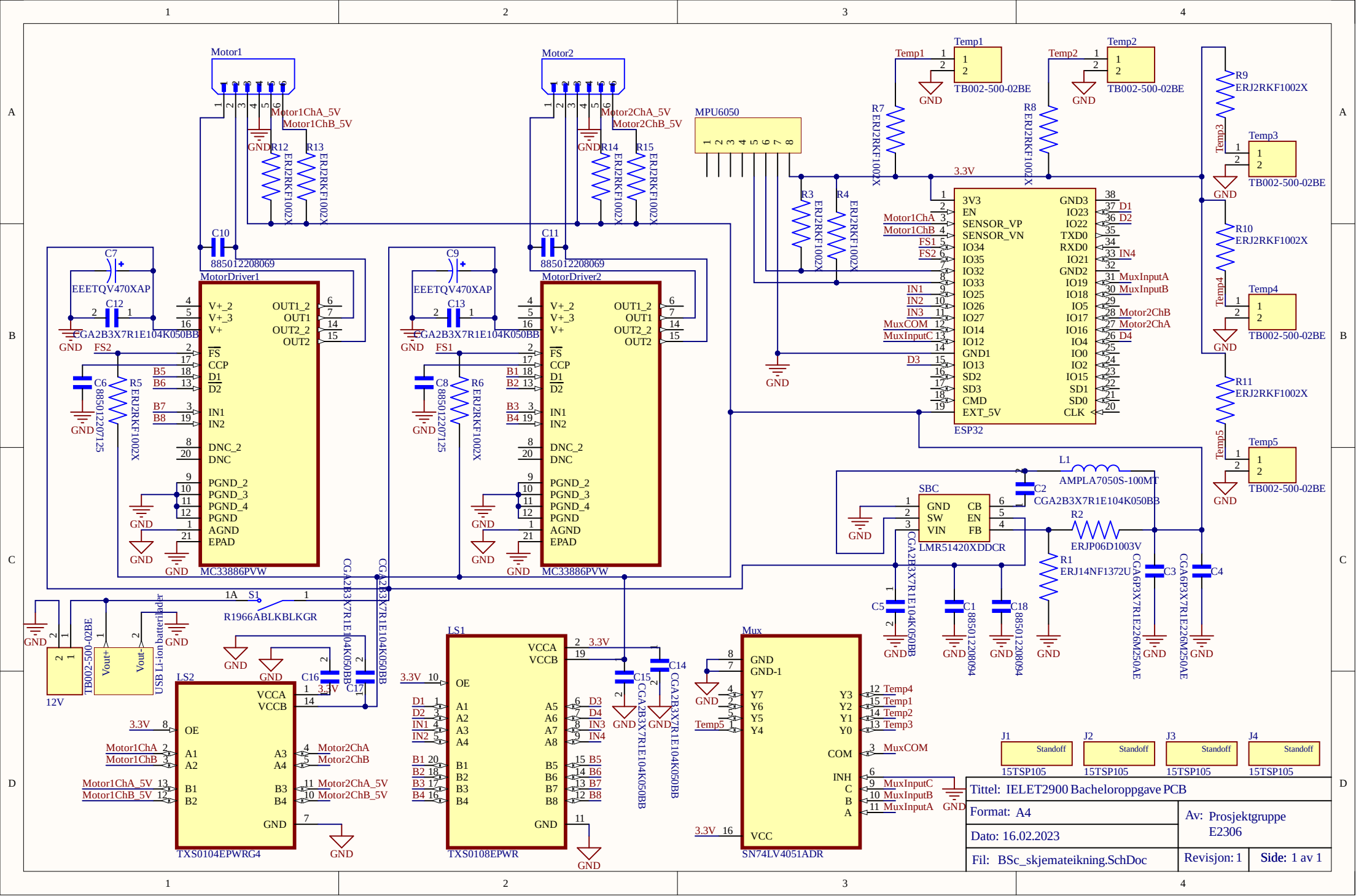
Motor1
Motor2
Motor1ChA_5V
Motor1ChB_5V
Motor2ChA_5V
Motor2ChB_5V
MPU6050
Temp1
Temp2
Temp3
Temp4
Temp5
TB002-500-02BE
R7
R8
R9
R10
R11
R12
R13
R14
R15
R3
R4
ERJ2RKF1002X
3.3V
GND
ESP32
3V3
EN
SENSOR_VP
SENSOR_VN
IO34
IO35
IO32
IO33
IO25
IO26
IO27
IO14
IO12
GND1
IO13
SD2
SD3
CMD
EXT_5V
GND3
IO23
IO22
TXD0
RXD0
IO21
GND2
IO19
IO18
IO5
IO17
IO16
IO4
IO0
IO2
IO15
SD1
SD0
CLK
Motor1ChA
Motor1ChB
FS1
FS2
IN1
IN2
IN3
IN4
MuxCOM
MuxInputA
MuxInputB
MuxInputC
Motor2ChA
Motor2ChB
D1
D2
D3
D4
MotorDriver1
MotorDriver2
MC33886PVW
V+_2
V+_3
V+
OUT1_2
OUT1
OUT2_2
OUT2
FS
CCP
D1
D2
IN1
IN2
DNC_2
DNC
PGND_2
PGND_3
PGND_4
PGND
AGND
EPAD
C7
C9
C10
C11
C12
C13
EEETQV470XAP
885012208069
CGA2B3X7R1E104K050BB
C6
C8
R5
R6
885012207125
SBC
LMR51420XDDCR
GND
CB
EN
FB
SW
VIN
L1
AMPLA7050S-100MT
C2
R2
ERJP06D1003V
R1
ERJ14NF1372U
C1
C3
C4
C5
C18
CGA6P3X7R1E226M250AE
885012208094
S1
R1966ABLKBLKGR
1A
TB002-500-02BE
12V
USB Li-ion batterilader
Vout+
Vout-
LS1
LS2
TXS0108EPWR
TXS0104EPWRG4
VCCA
VCCB
OE
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
C14
C15
C16
C17
Mux
SN74LV4051ADR
GND-1
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
COM
INH
C
B
A
VCC
J1
J2
J3
J4
Standoff
15TSP105
Tittel: IELET2900 Bacheloroppgave PCB
Format: A4
Av: Prosjektgruppe E2306
Dato: 16.02.2023
Fil: BSc_skjemateikning.SchDoc
Revisjon: 1
Side: 1 av 1

12V
S1
E2306
C17
C16
LS2
JLCJLCJLCJLC
C12
C7
C13
C9
C6
C8
iver1
iver2
Motor1
C10
R13R12
Motor2
C11
R14
R15
MotorDriver
MotorDriver
MPU6050
R5
Mux
C18
C1
C5
R6
R1
C2
SBC
R2
C3 C4
Temp5.
LS1
R4
R3
L1
C15
C14
Temp1.
Temp2.
Temp3.
Temp4.
ESP32
R11 R10 R9 R8 R7

Design Rules Verification Report

Filename : C:\Users\bjorn\OneDrive - NTNU\PCB_BSc_backups\BSc_PCB_balanserande_pinne_backup 10.02.2023\BSc_PCB_teikning.PcbD

Warnings 0
Rule Violations 144

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	30
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=500mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	44
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	53
Silk to Silk (Clearance=10mil) (All),(All)	13
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	144

Clearance Constraint (Gap=10mil) (All),(All)
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-1(1964.992mil,2041.842mil) on Top Layer And Pad LS1-2(1964.992mil,2067.433mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-10(1964.992mil,2272.157mil) on Top Layer And Pad LS1-9(1964.992mil,2246.567mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-11(1739.008mil,2272.157mil) on Top Layer And Pad LS1-12(1739.008mil,2246.567mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-12(1739.008mil,2246.567mil) on Top Layer And Pad LS1-13(1739.008mil,2220.976mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-13(1739.008mil,2220.976mil) on Top Layer And Pad LS1-14(1739.008mil,2195.386mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-14(1739.008mil,2195.386mil) on Top Layer And Pad LS1-15(1739.008mil,2169.795mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-15(1739.008mil,2169.795mil) on Top Layer And Pad LS1-16(1739.008mil,2144.205mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-16(1739.008mil,2144.205mil) on Top Layer And Pad LS1-17(1739.008mil,2118.614mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-17(1739.008mil,2118.614mil) on Top Layer And Pad LS1-18(1739.008mil,2093.024mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-18(1739.008mil,2093.024mil) on Top Layer And Pad LS1-19(1739.008mil,2067.433mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-19(1739.008mil,2067.433mil) on Top Layer And Pad LS1-20(1739.008mil,2041.842mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-2(1964.992mil,2067.433mil) on Top Layer And Pad LS1-3(1964.992mil,2093.024mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-3(1964.992mil,2093.024mil) on Top Layer And Pad LS1-4(1964.992mil,2118.614mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-4(1964.992mil,2118.614mil) on Top Layer And Pad LS1-5(1964.992mil,2144.205mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-5(1964.992mil,2144.205mil) on Top Layer And Pad LS1-6(1964.992mil,2169.795mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-6(1964.992mil,2169.795mil) on Top Layer And Pad LS1-7(1964.992mil,2195.386mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-7(1964.992mil,2195.386mil) on Top Layer And Pad LS1-8(1964.992mil,2220.976mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS1-8(1964.992mil,2220.976mil) on Top Layer And Pad LS1-9(1964.992mil,2246.567mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-1(1779.228mil,3658.008mil) on Top Layer And Pad LS2-2(1804.819mil,3658.008mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-10(1881.591mil,3883.992mil) on Top Layer And Pad LS2-11(1856mil,3883.992mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-10(1881.591mil,3883.992mil) on Top Layer And Pad LS2-9(1907.181mil,3883.992mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-11(1856mil,3883.992mil) on Top Layer And Pad LS2-12(1830.409mil,3883.992mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-12(1830.409mil,3883.992mil) on Top Layer And Pad LS2-13(1804.819mil,3883.992mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-13(1804.819mil,3883.992mil) on Top Layer And Pad LS2-14(1779.228mil,3883.992mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-2(1804.819mil,3658.008mil) on Top Layer And Pad LS2-3(1830.409mil,3658.008mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-3(1830.409mil,3658.008mil) on Top Layer And Pad LS2-4(1856mil,3658.008mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-4(1856mil,3658.008mil) on Top Layer And Pad LS2-5(1881.591mil,3658.008mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-5(1881.591mil,3658.008mil) on Top Layer And Pad LS2-6(1907.181mil,3658.008mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-6(1907.181mil,3658.008mil) on Top Layer And Pad LS2-7(1932.772mil,3658.008mil) on Top Layer
Clearance Constraint: (9.449mil < 10mil) Between Pad LS2-8(1932.772mil,3883.992mil) on Top Layer And Pad LS2-9(1907.181mil,3883.992mil) on Top Layer

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (129.921mil > 100mil) Pad -(1340mil,1673mil) on Multi-Layer Actual Hole Size = 129.921mil
Hole Size Constraint: (129.921mil > 100mil) Pad -(1340mil,3910mil) on Multi-Layer Actual Hole Size = 129.921mil
Hole Size Constraint: (129.921mil > 100mil) Pad -(4181.102mil,1669.292mil) on Multi-Layer Actual Hole Size = 129.921mil
Hole Size Constraint: (129.921mil > 100mil) Pad -(4181.102mil,3909.448mil) on Multi-Layer Actual Hole Size = 129.921mil

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (5.544mil < 10mil) Between Pad C12-1(2845.59mil,3840mil) on Top Layer And Pad C12-2(2880mil,3840mil) on Top Layer [Top Solder] Mask Sliver [5.544mil]
Minimum Solder Mask Sliver Constraint: (5.544mil < 10mil) Between Pad C13-1(3634.41mil,3850mil) on Top Layer And Pad C13-2(3600mil,3850mil) on Top Layer [Top Solder] Mask Sliver [5.544mil]
Minimum Solder Mask Sliver Constraint: (5.543mil < 10mil) Between Pad C14-1(2041mil,2067.205mil) on Top Layer And Pad C14-2(2041mil,2032.795mil) on Top Layer [Top Solder] Mask Sliver [5.543mil]
Minimum Solder Mask Sliver Constraint: (5.543mil < 10mil) Between Pad C15-1(1643mil,2063.205mil) on Top Layer And Pad C15-2(1643mil,2028.795mil) on Top Layer [Top Solder] Mask Sliver [5.543mil]
Minimum Solder Mask Sliver Constraint: (5.543mil < 10mil) Between Pad C16-1(1696mil,3657.795mil) on Top Layer And Pad C16-2(1696mil,3692.205mil) on Top Layer [Top Solder] Mask Sliver [5.543mil]
Minimum Solder Mask Sliver Constraint: (5.543mil < 10mil) Between Pad C17-1(1696mil,3883.205mil) on Top Layer And Pad C17-2(1696mil,3848.795mil) on Top Layer [Top Solder] Mask Sliver [5.543mil]
Minimum Solder Mask Sliver Constraint: (5.544mil < 10mil) Between Pad C2-1(3240mil,2454.41mil) on Top Layer And Pad C2-2(3240mil,2420mil) on Top Layer [Top Solder] Mask Sliver [5.544mil]
Minimum Solder Mask Sliver Constraint: (5.544mil < 10mil) Between Pad C5-1(3502.794mil,2590.001mil) on Top Layer And Pad C5-2(3537.204mil,2590.001mil) on Top Layer [Top Solder] Mask Sliver [5.544mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-1(1964.992mil,2041.842mil) on Top Layer And Pad LS1-2(1964.992mil,2067.433mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-10(1964.992mil,2272.157mil) on Top Layer And Pad LS1-9(1964.992mil,2246.567mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-11(1739.008mil,2272.157mil) on Top Layer And Pad LS1-12(1739.008mil,2246.567mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-12(1739.008mil,2246.567mil) on Top Layer And Pad LS1-13(1739.008mil,2220.976mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-13(1739.008mil,2220.976mil) on Top Layer And Pad LS1-14(1739.008mil,2195.386mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-14(1739.008mil,2195.386mil) on Top Layer And Pad LS1-15(1739.008mil,2169.795mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-15(1739.008mil,2169.795mil) on Top Layer And Pad LS1-16(1739.008mil,2144.205mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-16(1739.008mil,2144.205mil) on Top Layer And Pad LS1-17(1739.008mil,2118.614mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-17(1739.008mil,2118.614mil) on Top Layer And Pad LS1-18(1739.008mil,2093.024mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-18(1739.008mil,2093.024mil) on Top Layer And Pad LS1-19(1739.008mil,2067.433mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-19(1739.008mil,2067.433mil) on Top Layer And Pad LS1-20(1739.008mil,2041.842mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-2(1964.992mil,2067.433mil) on Top Layer And Pad LS1-3(1964.992mil,2093.024mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-3(1964.992mil,2093.024mil) on Top Layer And Pad LS1-4(1964.992mil,2118.614mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-4(1964.992mil,2118.614mil) on Top Layer And Pad LS1-5(1964.992mil,2144.205mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-5(1964.992mil,2144.205mil) on Top Layer And Pad LS1-6(1964.992mil,2169.795mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-6(1964.992mil,2169.795mil) on Top Layer And Pad LS1-7(1964.992mil,2195.386mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-7(1964.992mil,2195.386mil) on Top Layer And Pad LS1-8(1964.992mil,2220.976mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS1-8(1964.992mil,2220.976mil) on Top Layer And Pad LS1-9(1964.992mil,2246.567mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-1(1779.228mil,3658.008mil) on Top Layer And Pad LS2-2(1804.819mil,3658.008mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-10(1881.591mil,3883.992mil) on Top Layer And Pad LS2-11(1856mil,3883.992mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-10(1881.591mil,3883.992mil) on Top Layer And Pad LS2-9(1907.181mil,3883.992mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-11(1856mil,3883.992mil) on Top Layer And Pad LS2-12(1830.409mil,3883.992mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-12(1830.409mil,3883.992mil) on Top Layer And Pad LS2-13(1804.819mil,3883.992mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-13(1804.819mil,3883.992mil) on Top Layer And Pad LS2-14(1779.228mil,3883.992mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-2(1804.819mil,3658.008mil) on Top Layer And Pad LS2-3(1830.409mil,3658.008mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-3(1830.409mil,3658.008mil) on Top Layer And Pad LS2-4(1856mil,3658.008mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-4(1856mil,3658.008mil) on Top Layer And Pad LS2-5(1881.591mil,3658.008mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-5(1881.591mil,3658.008mil) on Top Layer And Pad LS2-6(1907.181mil,3658.008mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-6(1907.181mil,3658.008mil) on Top Layer And Pad LS2-7(1932.772mil,3658.008mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad LS2-8(1932.772mil,3883.992mil) on Top Layer And Pad LS2-9(1907.181mil,3883.992mil) on Top Layer [Top Solder] Mask Sliver [1.449mil]
Minimum Solder Mask Sliver Constraint: (5.5mil < 10mil) Between Pad MotorDriver1-12(3230mil,3410mil) on Top Layer And Via (3230mil,3484mil) from Top Layer to Bottom Layer [Top Solder] Mask Sliver [5.5mil]
Minimum Solder Mask Sliver Constraint: (9.22mil < 10mil) Between Pad MotorDriver2-3(3753.254mil,2884mil) on Top Layer And Via (3754.474mil,2806.28mil) from Top Layer to Bottom Layer [Top Solder] Mask Sliver [9.22mil]
Minimum Solder Mask Sliver Constraint: (5.778mil < 10mil) Between Pad SBC-1(3427.674mil,2431.868mil) on Top Layer And Pad SBC-2(3465.074mil,2431.868mil) on Top Layer [Top Solder] Mask Sliver [5.778mil]
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad SBC-2(3465.074mil,2431.868mil) on Top Layer And Pad SBC-3(3502.476mil,2431.868mil) on Top Layer [Top Solder] Mask Sliver [5.78mil]
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad SBC-4(3502.476mil,2530.294mil) on Top Layer And Pad SBC-5(3465.074mil,2530.294mil) on Top Layer [Top Solder] Mask Sliver [5.78mil]
Minimum Solder Mask Sliver Constraint: (5.778mil < 10mil) Between Pad SBC-5(3465.074mil,2530.294mil) on Top Layer And Pad SBC-6(3427.674mil,2530.294mil) on Top Layer [Top Solder] Mask Sliver [5.778mil]

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (4.354mil < 10mil) Between Arc (2016.961mil,2041.842mil) on Top Overlay And Pad C14-2(2041mil,2032.795mil) on Top Layer [Top Overlay] to [Top Solder] clearance [4.354mil]
Silk To Solder Mask Clearance Constraint: (5.373mil < 10mil) Between Pad C10-1(4042.331mil,4619.874mil) on Top Layer And Track (4067.921mil,4651.37mil)(4138.787mil,4651.37mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.309mil < 10mil) Between Pad C10-1(4042.331mil,4619.874mil) on Top Layer And Track (4071.857mil,4588.378mil)(4138.787mil,4588.378mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (8.427mil < 10mil) Between Pad C10-2(4164.377mil,4619.874mil) on Top Layer And Text "C10" (4194.52mil,4612.008mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (5.373mil < 10mil) Between Pad C10-2(4164.377mil,4619.874mil) on Top Layer And Track (4067.921mil,4651.37mil)(4138.787mil,4651.37mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.373mil < 10mil) Between Pad C10-2(4164.377mil,4619.874mil) on Top Layer And Track (4071.857mil,4588.378mil)(4138.787mil,4588.378mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.374mil < 10mil) Between Pad C1-1(3254.976mil,2606mil) on Top Layer And Track (3280.567mil,2637.496mil)(3351.433mil,2637.496mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad C1-1(3254.976mil,2606mil) on Top Layer And Track (3284.504mil,2574.504mil)(3351.433mil,2574.504mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.373mil < 10mil) Between Pad C11-1(4051.635mil,4179.286mil) on Top Layer And Track (4077.225mil,4210.782mil)(4148.091mil,4210.782mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.312mil < 10mil) Between Pad C11-1(4051.635mil,4179.286mil) on Top Layer And Track (4081.163mil,4147.79mil)(4148.091mil,4147.79mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.453mil < 10mil) Between Pad C11-2(4173.681mil,4179.286mil) on Top Layer And Text "C11" (4204.851mil,4168.008mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (5.373mil < 10mil) Between Pad C11-2(4173.681mil,4179.286mil) on Top Layer And Track (4077.225mil,4210.782mil)(4148.091mil,4210.782mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.373mil < 10mil) Between Pad C11-2(4173.681mil,4179.286mil) on Top Layer And Track (4081.163mil,4147.79mil)(4148.091mil,4147.79mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.374mil < 10mil) Between Pad C1-2(3377.024mil,2606mil) on Top Layer And Track (3280.567mil,2637.496mil)(3351.433mil,2637.496mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.374mil < 10mil) Between Pad C1-2(3377.024mil,2606mil) on Top Layer And Track (3284.504mil,2574.504mil)(3351.433mil,2574.504mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.514mil < 10mil) Between Pad C18-1(3253.976mil,2709mil) on Top Layer And Text "C18" (3241.001mil,2752.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (5.374mil < 10mil) Between Pad C18-1(3253.976mil,2709mil) on Top Layer And Track (3279.567mil,2740.496mil)(3350.433mil,2740.496mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad C18-1(3253.976mil,2709mil) on Top Layer And Track (3283.504mil,2677.504mil)(3350.433mil,2677.504mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.514mil < 10mil) Between Pad C18-2(3376.024mil,2709mil) on Top Layer And Text "C18" (3241.001mil,2752.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (5.374mil < 10mil) Between Pad C18-2(3376.024mil,2709mil) on Top Layer And Track (3279.567mil,2740.496mil)(3350.433mil,2740.496mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.374mil < 10mil) Between Pad C18-2(3376.024mil,2709mil) on Top Layer And Track (3283.504mil,2677.504mil)(3350.433mil,2677.504mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (7.198mil < 10mil) Between Pad C5-1(3502.794mil,2590.001mil) on Top Layer And Text "C5" (3498.016mil,2614.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (7.198mil < 10mil) Between Pad C5-2(3537.204mil,2590.001mil) on Top Layer And Text "C5" (3498.016mil,2614.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (6.712mil < 10mil) Between Pad ESP32-1(1355.512mil,3711.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.712mil < 10mil) Between Pad ESP32-1(1355.512mil,3711.26mil) on Multi-Layer And Track (1306.3mil,3760.472mil)(1501.182mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-10(1355.512mil,2811.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-11(1355.512mil,2711.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-12(1355.512mil,2611.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-13(1355.512mil,2511.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-18(1355.512mil,2011.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-19(1355.512mil,1911.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.908mil < 10mil) Between Pad ESP32-19(1355.512mil,1911.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1695.276mil,1862.834mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-2(1355.512mil,3611.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (5.908mil < 10mil) Between Pad ESP32-20(2355.512mil,1911.26mil) on Multi-Layer And Track (2015.354mil,1862.834mil)(2404.724mil,1862.834mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-20(2355.512mil,1911.26mil) on Multi-Layer And Track (2404.724mil,1862.834mil)(2404.724mil,3760.472mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-21(2355.512mil,2011.26mil) on Multi-Layer And Track (2404.724mil,1862.834mil)(2404.724mil,3760.472mil) on Top Overlay [Top Overlay] to

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-22(2355.512mil,2111.26mil) on Multi-Layer And Track (2404.724mil,1862.834mil)(2404.724mil,3760.472mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-23(2355.512mil,2211.26mil) on Multi-Layer And Track (2404.724mil,1862.834mil)(2404.724mil,3760.472mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-27(2355.512mil,2611.26mil) on Multi-Layer And Track (2404.724mil,1862.834mil)(2404.724mil,3760.472mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-6(1355.512mil,3211.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.694mil < 10mil) Between Pad ESP32-7(1355.512mil,3111.26mil) on Multi-Layer And Track (1306.3mil,1862.834mil)(1306.3mil,3760.472mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.734mil < 10mil) Between Pad R1-2(3690mil,2530mil) on Top Layer And Text "R1" (3670.013mil,2590.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.734mil]
Silk To Solder Mask Clearance Constraint: (8.754mil < 10mil) Between Pad R5-1(2920mil,2680mil) on Top Layer And Text "R5" (2877.214mil,2703.597mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [8.754mil]
Silk To Solder Mask Clearance Constraint: (8.754mil < 10mil) Between Pad R5-2(2879.684mil,2680mil) on Top Layer And Text "R5" (2877.214mil,2703.597mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [8.754mil]
Silk To Solder Mask Clearance Constraint: (7.135mil < 10mil) Between Pad R6-1(3703.142mil,2693.033mil) on Top Layer And Text "R6" (3699.016mil,2715.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (7.135mil < 10mil) Between Pad R6-2(3743.458mil,2693.033mil) on Top Layer And Text "R6" (3699.016mil,2715.01mil) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (9.844mil < 10mil) Between Pad SBC-1(3427.674mil,2431.868mil) on Top Layer And Track (3402.082mil,2407.262mil)(3402.082mil,2456.474mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.843mil < 10mil) Between Pad SBC-1(3427.674mil,2431.868mil) on Top Layer And Track (3407.988mil,2470.254mil)(3522.162mil,2470.254mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.843mil < 10mil) Between Pad SBC-2(3465.074mil,2431.868mil) on Top Layer And Track (3407.988mil,2470.254mil)(3522.162mil,2470.254mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.843mil < 10mil) Between Pad SBC-3(3502.476mil,2431.868mil) on Top Layer And Track (3407.988mil,2470.254mil)(3522.162mil,2470.254mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.843mil < 10mil) Between Pad SBC-4(3502.476mil,2530.294mil) on Top Layer And Track (3407.988mil,2491.908mil)(3522.162mil,2491.908mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.843mil < 10mil) Between Pad SBC-5(3465.074mil,2530.294mil) on Top Layer And Track (3407.988mil,2491.908mil)(3522.162mil,2491.908mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.843mil < 10mil) Between Pad SBC-6(3427.674mil,2530.294mil) on Top Layer And Track (3407.988mil,2491.908mil)(3522.162mil,2491.908mil) on Top Overlay [Top Overlay] to [Top

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (4.014mil < 10mil) Between Text "C18" (3241.001mil,2752.01mil) on Top Overlay And Track (3279.567mil,2740.496mil)(3350.433mil,2740.496mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (9.446mil < 10mil) Between Text "C7" (3197.866mil,3899.86mil) on Top Overlay And Track (3141.55mil,3961.346mil)(3180.92mil,3921.976mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (9.446mil < 10mil) Between Text "C7" (3197.866mil,3899.86mil) on Top Overlay And Track (3180.92mil,3701.504mil)(3180.92mil,3921.976mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (9.746mil < 10mil) Between Text "C9" (3198.166mil,3702.584mil) on Top Overlay And Track (3180.92mil,3701.504mil)(3180.92mil,3921.976mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (9.445mil < 10mil) Between Text "C9" (3198.166mil,3702.584mil) on Top Overlay And Track (3315.078mil,3701.079mil)(3315.078mil,3921.551mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (9.344mil < 10mil) Between Text "ESP32" (1359.045mil,1786.01mil) on Top Overlay And Track (1306.3mil,1862.834mil)(1695.276mil,1862.834mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (3.298mil < 10mil) Between Text "R1" (3670.013mil,2590.01mil) on Top Overlay And Track (3727.204mil,2579.212mil)(3788.622mil,2579.212mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.904mil < 10mil) Between Text "R2" (3670.016mil,2370.01mil) on Top Overlay And Track (3725.236mil,2354.606mil)(3747.284mil,2354.606mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (4.717mil < 10mil) Between Text "Temp1" (2600.042mil,1920.006mil) on Top Overlay And Track (2614.724mil,1887.796mil)(3008.426mil,1887.796mil) on Top Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (4.717mil < 10mil) Between Text "Temp2" (3030.045mil,1920.006mil) on Top Overlay And Track (3041.574mil,1887.796mil)(3435.276mil,1887.796mil) on Top Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (4.717mil < 10mil) Between Text "Temp3" (3457.045mil,1920.006mil) on Top Overlay And Track (3468.574mil,1887.796mil)(3862.276mil,1887.796mil) on Top Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (8.062mil < 10mil) Between Text "Temp4" (3972.936mil,1783.694mil) on Top Overlay And Track (4008.492mil,1801.742mil)(4008.492mil,2195.444mil) on Top Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (7.007mil < 10mil) Between Text "Temp5" (3973.994mil,2209.045mil) on Top Overlay And Track (4008.494mil,2228.568mil)(4008.494mil,2622.268mil) on Top Overlay Silk Text to Silk

Name	Designator	Quantity	Manufacturer 1	Manufacturer Part Number 1	Manufacturer Lifecycle 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Subtotal 1	Supplier Order Qty 1
MPU6050	MPU6050 (Vedlagt socket og header 8-pins)	1								
15TSP105	J1, J2, J3, J4 (Standoff hol)	4								
USB Li-ion batterilader	(Vedlagt kretskort. Loddast ved Vout+ og Vout-)	1								
885012207125	C6, C8	2	Wurth Electronics	885012207125	Unknown	Mouser	710-885012207125	0,11	0,22	2
AMPLA7050S-100MT	L1	1	Abracon	AMPLA7050S-100MT	Unknown	Mouser	815-AMPLA7050S-100MT	1,71	1,71	1
CGA6P3X7R1E226M250AE	C3, C4	2	TDK	CGA6P3X7R1E226M250AE	Unknown	Mouser	810-CGA6P3X7R1E226M5	1,71	3,42	2
ESP32-DEVKITC	ESP32 (Vedlagt socket 2 stk. 19-pins)	1	Espressif Systems	ESP32-DEVKITC-32U	Unknown	Mouser	356-ESP32-DEVKITC32U	10	10	1
LMR51420XDDCR	SBC	1	Texas Instruments	LMR51420XDDCR	Unknown	Mouser	595-LMR51420XDDCR	1,56	1,56	1
MC33886PVW	MotorDriver1, MotorDriver2	2	NXP Semiconductors	MC33886PVW	Unknown	Mouser	841-MC33886PVW	12,36	24,72	2
TB002-500-02BE	12V, Temp1, Temp2, Temp3, Temp4, Temp5	6	CUI Devices	TB002-500-02BE	Unknown	Mouser	490-TB002-500-02BE	0,24	2,4	10
B6B-PH-K-S(LF)(SN)	Motor1, Motor2	2	JST	B6B-PH-K-S(LF)(SN)	Volume Production	Digi-Key	455-1708-ND	0,36	0,72	2
885012208069	C10, C11	2	Wurth Electronics	885012208069	Volume Production	Mouser	710-885012208069	0,6	1,2	2
885012208094	C1, C18	2	Wurth Electronics	885012208094	Volume Production	Mouser	710-885012208094	0,95	1,9	2
CGA2B3X7R1E104K050BB	C2, C5, C12, C13, C14, C15, C16, C17	8	TDK	CGA2B3X7R1E104K050BB	Volume Production	Mouser	810-CGA2B3X7R1E104K	0,046	0,46	10
EEETQV470XAP	C7, C9	2	Panasonic	EEE-TQV470XAP	Volume Production	Mouser	667-EEE-TQV470XAP	1,26	2,52	2
ERJ2RKF1002X	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15	13	Panasonic	ERJ-2RKF1002X	Volume Production	Mouser	667-ERJ-2RKF1002X	0,033	0,429	13
ERJ14NF1372U	R1	1	Panasonic	ERJ-14NF1372U	Volume Production	Mouser	667-ERJ-14NF1372U	0,44	0,44	1
ERJP06D1003V	R2	1	Panasonic	ERJ-P06D1003V	Volume Production	Mouser	667-ERJ-P06D1003V	0,33	0,33	1
R1966ABLKBLKGR	S1	1	E-Switch	R1966ABLKBLKGR	Volume Production	Mouser	612-R1966ABKBKGR	1,88	1,88	1
SN74LV4051ADR	Mux	1	Texas Instruments	SN74LV4051ADR	Volume Production	Mouser	595-SN74LV4051ADR	0,56	0,56	1
TXS0104EPWRG4	LS2	1	Texas Instruments	TXS0104EPWRG4	Volume Production	Mouser	595-TXS0104EPWRG4	1,28	1,28	1
TXS0108EPWR	LS1	1	Texas Instruments	TXS0108EPWR	Volume Production	Mouser	595-TXS0108EPWR	1,57	1,57	1