

A New ADC topology for reliable conversion in the automotive environment

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LIST OF SYMBOLS

Symbols

σ_i	standard deviation of i
E_g	Bandgap Energy
F_{snyq}	nyquist frequency
g_m	transistor small signal transconductance
K	degree Kelvin
Si	Silicon
L	transistor gate length
μ_i	mobility based on the phenomenon i or of the particle i
V_{th}	transistor threshold voltage
W	transistor gate width
ξ	electric field
CAD	computer-aided-design
FET	Field-Effect-Transistor
MOS	Metal-Oxide-Semiconductor

Writing Conventions

\bar{X} complementary of signal X

Acronyms and Abbreviations

ADC	Analog-to-Digital Converters
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
GBW	Gain-BandWidth product
IC	Integrated Circuit
LSB	Least Significant Bit

List of Symbols

MDAC Multiplying Digital-to-Analog Converter

MSB Most Significant Bit

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

PSTB Periodic STaBility

PVT Process-Voltage-Temperature

SAR Successive Approximation Register

SNR Signal over Noise Ratio

UGF Unity-Gain-Frequency

CHAPTER 1

INTRODUCTION

The advent of the Internet of Things (IoT) has brought the need for novel studies to conform to its extensive requirements, driven specifically by the Smart Vehicle industry. Smart vehicles must be able to efficiently sense and communicate with other nearby vehicles, including cars, buses and trucks. For obvious reasons, the design and specification of microelectronic circuits, which are used in these applications, are regulated by many strict security and safety standards. Reliability and robustness in the device operation must be ensured for harsh environments [1], including the required operating temperature range from -40 °C to 175 °C. This temperature range is arguably the most difficult environment challenge for electronics in the automotive industry [2]. Hence, to meet the IoT challenge, smart vehicles must integrate high performance electronics over a wide temperature range.

Such electronics are challenged by the high temperature near engine, disc brake systems and abrupt accelerations worsen the difficulty of smart actuator design. Information on automotive environments and electrical component test standards can be found at the Automotive Electronics Council [3, 4]. Figure 1.1 shows the typical temperature environment for such embedded electronics. The operating temperature is a function of the location, the circuit's power dissipation, and the thermal design. Noting that typical junction temperature for integrated circuits are 10°C to 25°C higher than ambient temperature, the on-engine temperature specification is often -40°C to 175°C.

Aiming a Smart Vehicle, the sensor market is arguably the most important one. The vehicle smartness is given by strong processing unit which could not stand the harsh environment in which most of sensors should sustain. To transfer the information of sensors to those processing units, it is mandatory to place the Analog-to-Digital converters (ADC) as close as possible to the sensor with a sampling rate sufficiently high for the future application of autonomous car. For all these reasons, ADC design is a challenge since it should remain reliable even under performance variation [5].

1.1 Motivation

To that extent, a low-cost, fast and accurate ADC operating in those harsh conditions is a good ally for equipment manufacturers. To decrease the cost, the area is a major concern. Considering re-use of the ADC as an IP-bloc, the area should be limited to less than half a square millimeter. In the automotive environment, ADCs are the usual interface with environmental sensors and motor control sensors.

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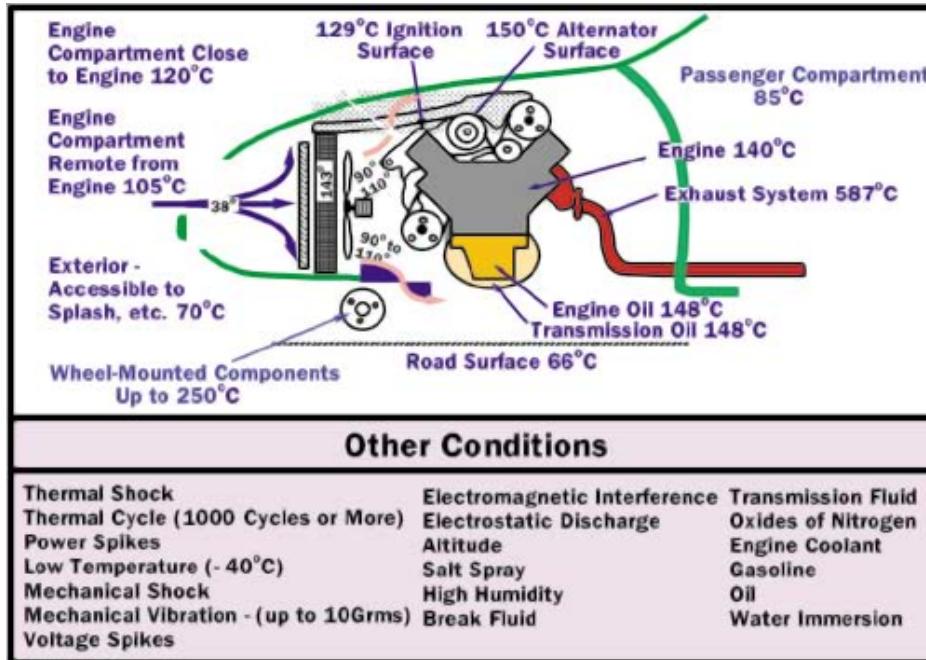


Figure 1.1 Stringent automotive conditions presented by the Automotive Electronics Council [3, 4]

Table 1.1 Specification of target ADC

Criterion	
Operating Temperature	-40 °C – +175 °C
Supply Voltage	1.8 V ± 10 %
Differential Input Voltage Range	± 1V
Area	<0.5 mm ²
Conversion Speed	20 MSamples/s
Maximum Clock Frequency	100 MHz
Clock Duty-Cycle	40 – 60 %
Latency	500 ns
Resolution	≥ 12-bits
SNDR	min 74 dB for $F_s < 5$ MHz min 68 dB for 5 MHz < $F_s < 10$ MHz, min 62 dB for $F_s > 10$ MHz
SFDR (Full-Scale)	min 68 dB
DNL	<LSB/2
INL	<LSB/2 best-fit method
Offset Error	<4 LSB
Gain Error	<4 LSB
Adjacent ADC mismatch Error	<4 LSB
Energy, $E_s = P/F_s$	0.75 nJ/sample

The frequency spectrum of such application being limited, the ADC does not need to tackle for Gigahertz sampling. The accuracy and the linearity is of much importance. Nevertheless, vehicle communicates the sensors information. The bandwidth of the signals communication is few megahertz. To fulfill the need, the minimum requirements for a final product are listed in Table 1.1. The order of importance is the area, the resolution, the power consumption, and the conversion speed. It is important to highlight the temperature range and the ratio between the conversion speed and the maximum clock frequency equal to 5. This ratio also called Oversampling Ratio (OSR) is the number of clock cycle allowed to perform a conversion.

To responds to the future need of the automotive environment, we aim to design an ADC over a wide temperature range from -40°C to 175°C with the following characteristics:

- Maximum oversampling ratio of 5
- SNDR greater than 68 dB
- a consumption less than 0.75 nJ/sample
- and target a silicon area less than 0.5 mm² for cost reason

With a preference sets on the minimization of the silicon area, before the minimization of the power consumption, the resolution and the speed.

The XT018 technology, from the XFAB Silicon Foundries, is ideal for system-on-chip (SoC) applications in the automotive market such as control devices inside combustion engine compartments or electric engine housings with temperature range up to 175°C, as well as robust medical applications which should sustain high voltages [6]. Such technology is a SOI process, which uses a deep-trench buried oxide that leads to a very low junction leakage current even at high temperatures.

1.2 Thesis Organisation

This work focuses on the design of high-precision, high-speed and energy efficient ADC under the harsh environment the automotive one represents. A emphasis is on doing such design in a SOI CMOS processes under stringent Process-Voltage-Temperature (PVT) variations. Our main contribution relies on the development of a new hybrid topology proposal using 3 stages to cope with such constraints based on a top-down approach: a counting stage inherently linear, an algorithmic stage to increase rapidly the precision, and a SAR stage for area and power consumption trade-off.

We review operation of conventional ADC topologies in the Chapter 2. Their advantages and source of errors are discussed to present why some architectures are predominant in high temperature conditions. Namely, few of them such as $\Delta\Sigma$, SAR, and pipelined are able to cope with

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analog imperfections coming from the temperature. The proposed architecture is then presented to benefit from the strength of each one.

The section 2.2 then discusses the challenge of analog design over a large temperature range from -40°C to +175°C. Phenomena tightly linked to the temperature are analysed to highlight the design trade-offs when considering temperature effects. Based on a g_m/I_D methodology, the insight gained from this analysis is then reused during the design phase.

Having the severe degradation, we discuss the enhancement ported to our topology proposal to glean the maximum of performances within the smallest footprint in a 180 nm technology. Alongside the optimization, Chapter 3 considers the reliability and introduces the case of pseudo-asynchronous design to relax timing restrictions in the digital part over temperature. We have defined a methodology for the design and characterization of such converter by using a testbench comparing a high-level model of the converter, defined in VerilogAMS, and a schematic description of the converter, able to use macromodels of the components or their transistor-level description. A MATLAB post-processing can extract the main characteristics such as the precision, the INL, DNL ...

The design of mandatory analog blocks, which are respectively comparators and operational amplifier, is examined to ensure the expected behavior for a rigorous 6σ process variation. To achieve this, a new time delay model have been developed for the Double Tail comparator. This model has been presented during the ECCTD conference held in 2017. Meanwhile, the layout concerns to get the most of the op-amp is also discussed in the Chapter 4.

Despite the fact the ADC testchip is in a finalization stage, experimentation is key in the validation process of IP components. Details in the realization of testchips in temperature which are worth to be discussed are presented in Chapter 5. With a chip dedicated for the assessment of comparators, their offset, the delay, the noise, and the hysteresis measurement circuits are implemented. The delay of high speed clocked comparator has been measured with a new measurement circuits presented during the ECCTD in 2017. After the enhancement of our topology proposal, only the testability of the last stage has seen its complexity increased. A second test chip assesses the effectiveness of pseudo-asynchronous design at high temperature and extracts static metrics of the last stage (DNL, INL, ...). Then, a last section focuses on the ADC testchip. Its design and preliminary results of the ADC are presented. Chapter 6 concludes our research findings and suggests potential future work.

STATE OF THE ART

The performance of an ADC can be defined by the fidelity of signal representation, and the bandwidth of the signal which can be represented. In other term, the key criteria of an ADC are the Signal to Noise and Distortion Ratio (SNDR) and the Nyquist frequency (F_{Nyq}). Figure 2.1 distinguishes ADC families using both criteria. These ADC families are:

1. Flash, having a higher time-efficiency but too expensive for high resolution as power consumption and the area scales with resolution;
2. $\Delta\Sigma$, being the best trade-off between resolution and speed but power consumption and area scales with requirements;
3. Pipelined and Algorithmic, being high-speed and high-resolution but power consumption and area hungry;
4. SAR, performing either high-resolution or high-speed conversions for a very low power consumption.

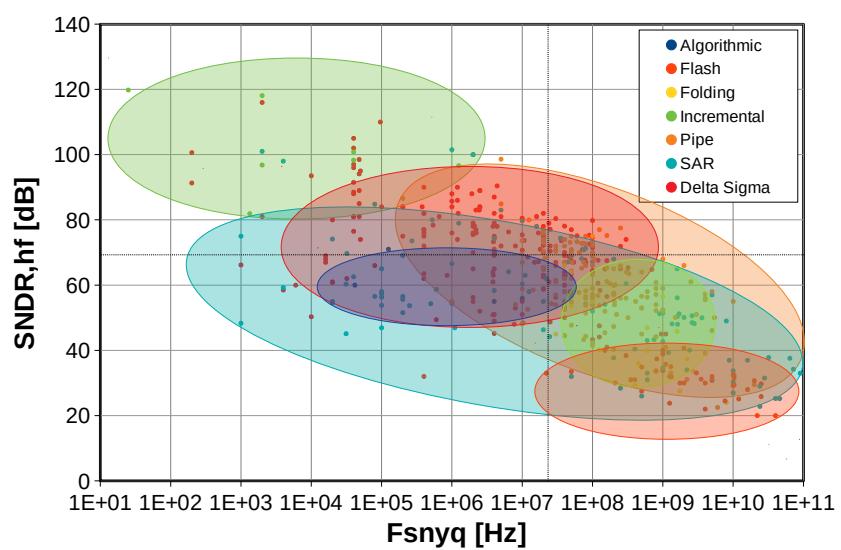


Figure 2.1 Comparison of ADC topology in the SNDR- F_{Nyq} space based on publication in ISSCC and VLSI from 1997 to 2018 [7]

An analysis of the chart allows the designer to proper decide what kind of a converter topology is desired according to the speed and the signal fidelity required. For instance, Flash ADCs achieve rather low SNDR at very high speed while Incremental ADCs achieve high fidelity signal representation for low signal bandwidth.

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It is worth to mention that Folding ADC are close from the ADC specification in this thesis. Besides that, prior art topologies are often requiring more than 5 clock cycles per conversion to reach the resolution expected. In this scenario, there is no immediate solution to propose a topology that meets the specification requirements. That's why, a new topology is proposed in this work. This chapter begins with an analysis of classical ADC architectures. A large emphasis is set on the low-OSR and high-resolution possibility at a medium conversion rate.

Later in this chapter, a brief review of ADC design over extended temperature range is presented. At high temperatures, transistors suffer from several defects that degrade their performances which impacts system performance. The impact of the temperature at the device level and the material dependences are studied using CMOS XT018 technology.

2.1 Analog-to-Digital Converters

2.1.1 Flash

Flash ADCs proceed a conversion by comparing the analog input voltage with several reference voltages. While a resistive divider generates references, the comparators provide in the same clock cycle the comparison results of the input voltage with each reference voltage, as represented in Figure 2.2.

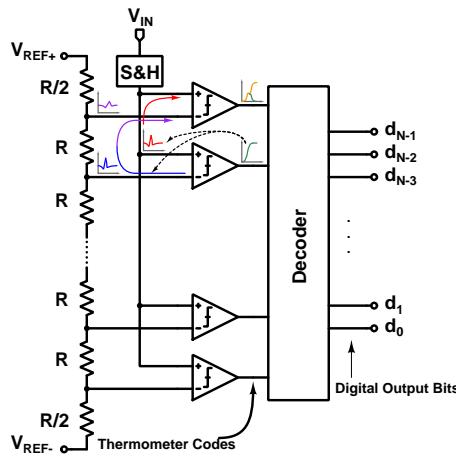


Figure 2.2 Flash ADC architecture: illustration of comparators' kickback noise impacts other comparator though the reference ladder

Thus, an analog input below the i^{th} reference voltage produces an output of $i - 1$ ones followed by zeros. A rising input voltage increasing the number of consecutive ones at the output, this architecture is known as thermometer code encoding. For an N -bit converter, a Flash ADC requires $2^N - 1$ comparators, and a decoder usually follow to bring an N -bit binary word. The time-efficiency of this architecture is too expensive for high resolution ADC, as both the power consumption and

the area scales with the desired resolution. In addition to that, the clock skew has an important impact on the output code. The decision of a comparator could disturb the decision of another who starts to decide later. Usually Flash does not exceed 8-bits.

A different kind of Flash ADC, able to achieve 8-bits or more, is the Folding ADC. In the Folding ADC, a pre-estimation of the performed by a Flash ADC is done as depicted by Figure 2.3. There a folding amplifier generates a sawtooth waveform corresponding to the error of conversion of the "first stage". The folding depends on the conversion results of a the first Flash ADC. Thus, it generates the Most-Significant-Bits (MSB) saving area and power consumption.

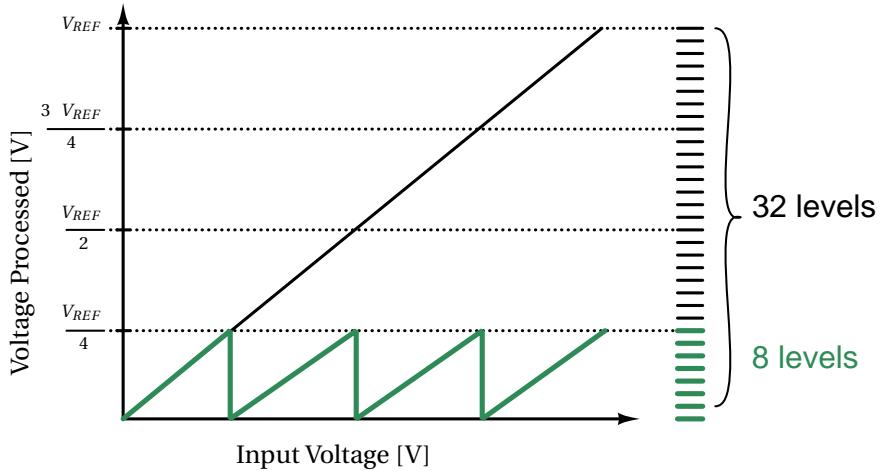


Figure 2.3 Signal folding principle to reduce the number of needed comparators in a 5-bits ADC example

In the same time, a second Flash ADC performs the conversion of the folded signal. This reduces the total number of components relaxing previous constraints of first Flash ADC [8–11]. Unfortunately, the Folding topology should have a linearity greater than the fine Flash ADC. Such linearity issues can be corrected either by a digital calibration or by a resistive interpolation [11]. Such topology of ADC allows the cascade of several stages [12, 13], making it a good candidate to achieve medium resolution at high speed [11, 14]. The biggest flaws of Folding Flash ADC is the area and the power consumption despite works to reduce them [15]. The comparison table 2.1 reveals the resolution of such architectures of Flash ADC. They achieve a very high speed with a small latency. This can be viewed as a trade of time for resolution.

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Table 2.1 Folding ADC in the literature

Ref.	Architecture	Techno. [nm]	F_{snyq} [MHz]	Area [mm ²]	Supply [V]	Power [mW]	Res.
[11]	Folding & Interpolation	1000	60	7	5	300	12
[12]	Cascaded Folding	180	1000	49	1.8	1260	10
[13]	Folding & Interpolation	250	6000	13.3	5.1/3	10200	10
[15]	switched-cap Folding	350	100	NA	3.3	2.5	8
[16]	Folding	500	100	1.68	5	165	8

2.1.2 $\Delta\Sigma$ Converters

2.1.2.1 $\Delta\Sigma$ Modulation

Delta-Sigma ($\Delta\Sigma$) modulation efficiently performs high-resolution data conversion using oversampling. For the sake of clarity, let's us consider first a sine wave converted by an ADC without oversampling. The power spectral density, Figure 2.4a, is made of a tone representing the signal power, an floor corresponding to the quantification noise, and other source of noise. The effective number of bits (ENOB) is related to the gap between the noise floor and the signal level. The bigger the gap is, the higher is the ENOB of the converter.

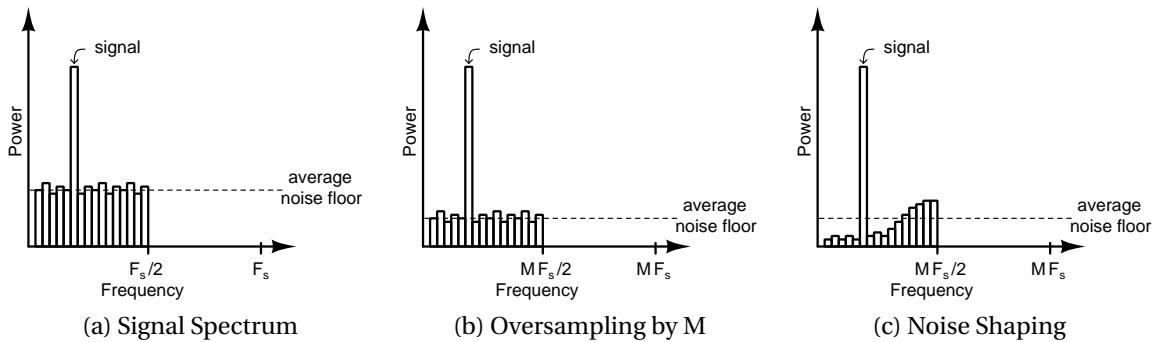
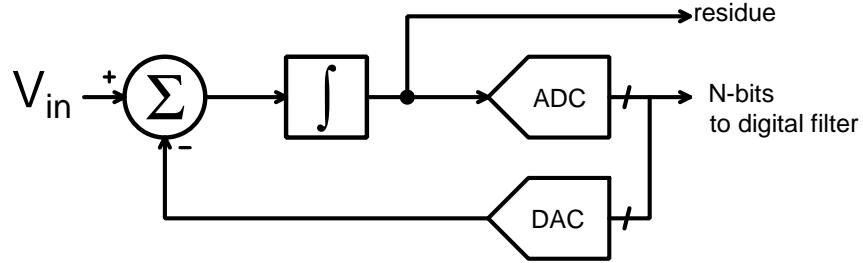


Figure 2.4 Principle of the $\Delta\Sigma$ ADC to perform a high-resolution conversion

By increasing the sampling frequency F_s by a factor M , the noise floor level decreases by M ; it is now spread over a wider frequency range ($F_s \cdot M$). The integral of the noise over the frequency band of interest remains constant as illustrated from Figure 2.4a to Figure 2.4b. By filtering the spectrum with a cut off frequency of $F_s/2$, the noise power reduced in the signal bandwidth. To enhance further performance, the distribution of the noise can be shaped to push the noise at higher frequencies than the cut-off of the digital filter.

To convert the input signal, a $\Delta\Sigma$ modulator is similar to a regulation loop in which the integrator controller monitors the process of conversion as illustrated in Figure 2.7. The integral term


 Figure 2.5 Multi-bits $\Delta\Sigma$ converter

permits the rejection of a step disturbance and ensures that for a stepped input, the static error of the conversion process is nulled. With respect to the input signal, the integrator behaves like a low-pass filter. To the contrary, for the quantification noise coming from the feedback path, the integrator is likewise an high-pass filter. The noise is shaped. In consequence, there is a signal transfer function (STF) and a noise transfer function (NTF). The implementation imperfections, including matching errors and offsets which limit the obtainable resolution of Nyquist rate converters, can thus be surmounted as these are in the feedback path. Furthermore, the oversampling reduces the constraint of the anti-aliasing filter in front of ADC by relaxing the filter order required.

To increase bandwidth, it is necessary to reduce the oversampling ratio (OSR). To preserve the resolution, the noise-shaping filter order should be higher. The improve originates from extra integrator in the forward path. Unfortunately, feedback structure of the modulator is prone to instability for high-order of noise shaping (≥ 3). Besides, high-order modulators suffer from a stability dependency on system parameters such as integrator gains and delays, input amplitude, transients, initial conditions, or even saturation limit cycles [17–19]. For modulator stability, the integrator signal shall be weighted appropriately. Reducing the input amplitude is another way to stabilize the system, as well as reducing the error signal integrated to prevent saturation of the following integrator. In this regard, multi-bit quantization limits the excursion of the integrator. However, the implementation of the multi-level error feedback DACs can significantly reduce the modulator performance if the DAC is not extremely linear [20].

2.1.2.2 Incremental- $\Delta\Sigma$

Unlike conventional $\Delta\Sigma$ ADC, the analog loop filter and digital filter in Incremental- $\Delta\Sigma$ ($I\Delta\Sigma$) ADC are reset after oversampling each input sample. As a result, $I\Delta\Sigma$ ADC can offer sample-by-sample conversion much like Nyquist-rate ADC allowing multiplexing of different inputs to be done without cross talk.

A first order $I\Delta\Sigma$ as represented in Figure 2.6 has a resolution of N-bits is achieved in 2^N clock cycle. Different approaches have been proposed to significantly enhance the conversion speed and/or resolution of $I\Delta\Sigma$ ADC [21–23]. The most popular alternatives are high-order architec-

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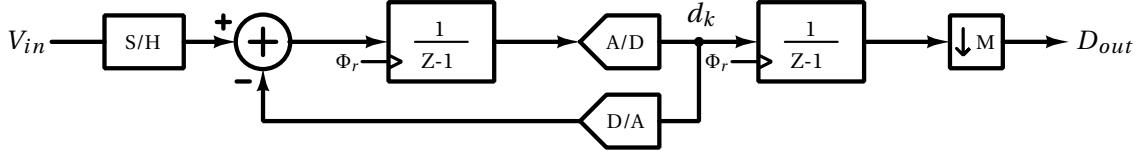


Figure 2.6 First Order Incremental- $\Delta\Sigma$

tures [24–26]. Recent advances in $I\Delta\Sigma$ ADC showcase further improvement in power efficiency by employing inverter-based integrators [27], or comparator based integrators [28].

An added benefit to $I\Delta\Sigma$ is the simplicity of the decimation filter. As the output of the regulation loop is the bits of the conversion process, these represent the input signal. So, the error at the input of integrator is in the best case zero. The output of the controller keeping the error null, the digital reconstruction filter should have the same transfer function of the controller to represent the input. For a first order modulator, the input signal is reconstituted by counting output bits, while for higher order the representation of the input signal is given by a weighted multiple integral. For a third order modulator, V_{in} is thus estimated by the equation (2.1).

$$\frac{V_{in}}{V_{ref}} \approx \frac{3!}{(n-2)(n-1)n} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k \quad (2.1)$$

In other term, the input-referred noise of an Incremental- $\Delta\Sigma$ comes from a weight association of each sample, and for higher order modulators earlier samples have a higher weighting than later samples because the digital filter has non-uniform weighting coefficients for higher order modulators. The equation (2.2) expresses the total input-referred noise power $\overline{v_n^2}$

$$\overline{v_n^2} = \sum_{i=1}^M w_i^2 \overline{v_s^2} = \overline{v_s^2} \sum_{i=1}^M w_i^2 \quad (2.2)$$

where $\overline{v_s^2}$ is the input noise power of each sample, M is the OSR, and w_i is the weight associated with each sample.

In a first-order modulator, and assuming an accumulator as a decimation filter, the output as an average of the M inputs added to the quantization noise error introduced leads to $w_i = 1/M$. The resulting input-referred noise power is $\overline{v_n^2}/M$, as expected for an ADC oversampled by M . Nevertheless, the first clock cycle is dedicated to the reset of the integrator, which limits the resolution in low-OSR architecture.

2.1.2.3 MASH

To the opposite of high-order modulator, first-order modulators are inherently stable without weighting the output of the integrator. A cascade of such modulators results in an increased noise shaping order without the stability issue or sacrificing the input amplitude [29]. Also called Multi-stAge noise-SHaping (MASH), they have the advantage that no individual modulator needs to be designed with a high-order filter; the total filter order can be spread out across many different stages so that each individual $\Delta\Sigma$ stage will only be of low order. The modulator stability will be a function of the individual lower order modulators rather than the total order of the modulator.

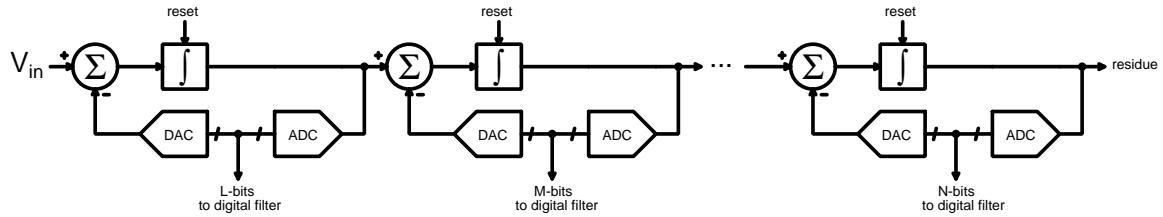


Figure 2.7 1-1-...-1 MASH $\Delta\Sigma$ converter

The digital output of individual $\Delta\Sigma$ modulators is then processed by a digital filter. It is designed to reduce error introduced in first stages by the product of the Noise-Transfer-Function of each stage. This cancellation is dependent on matching between the digital filters and the analog filters within modulators. The latter is one of the major limitations for high-resolution cascaded $\Delta\Sigma$ modulators leveraged by digital calibration [30].

2.1.2.4 Mixed Architecture based on $\Delta\Sigma$

Other alternatives are the extended counting (EC-ADC) [31–33] and the extended range (ER-ADC) [34, 35] architectures, which combine the $I\Delta\Sigma$ ADC with a low-power Nyquist-rate ADC. The main difference between the two is that in an EC-ADC, the $I\Delta\Sigma$ ADC hardware is usually reused and reconfigured as a cyclic ADC, while in an ER-ADC, the residue of the $I\Delta\Sigma$ is processed by another Nyquist-rate ADC.

The table 2.2 compares $I\Delta\Sigma$ to MASH and mixed architecture to highlight the main characteristics of these converters.

2.1.3 Pipelined and Algorithmic

Pipelined and Algorithmic converter are fundamentally similar. They are based on a common build bloc: the analog processor. This bloc is made of an ADC-DAC chain to estimate the input, whose difference with it is then multiplied by an arbitrary factor A. The output of the analog processor is the conversion residue amplified. A is the radix of conversion and it is often set to 2. Represented

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Table 2.2 $I\Delta\Sigma$ -ADC in the literature

Ref.	Architecture	Techno. [nm]	F_{snyq} [kHz]	OSR	Area [mm 2]	Supply [V]	Power [mW]	Res.
[22]	3 rd Order $I\Delta\Sigma$	600	30.72	512	2.08	2.5/5	0.6	22
[27]	3 rd Order $\Delta\Sigma$	180	40	100	0.715	0.7	0.036	14
[31]	EC- $\Delta\Sigma$	180	185	8	0.0069	1.8	0.022	12
[34]	ER- $I\Delta\Sigma$	180	1000	45	3.5	1.8	38.1	14
[36]	1-1-1 MASH CT- $\Delta\Sigma$	40	50000	29.7	0.177	1.2/2.5	19.7	11

in Figure 2.8a, pipelined ADCs are a cascade of these extracting N-bits for each clock cycle. The algorithmic depicted in Figure 2.8b, reuses the analog processor over and over by recycling the residue. After M clock cycle, both architectures extract $N \times M$ bits with the same latency. However, for the same clock frequency and number of bits extracted, a pipelined of M-stages has a sampling frequency M-times higher than an algorithmic with M-clock cycles. In addition to that, pipelined ADCs occupy a bigger area than algorithmic.

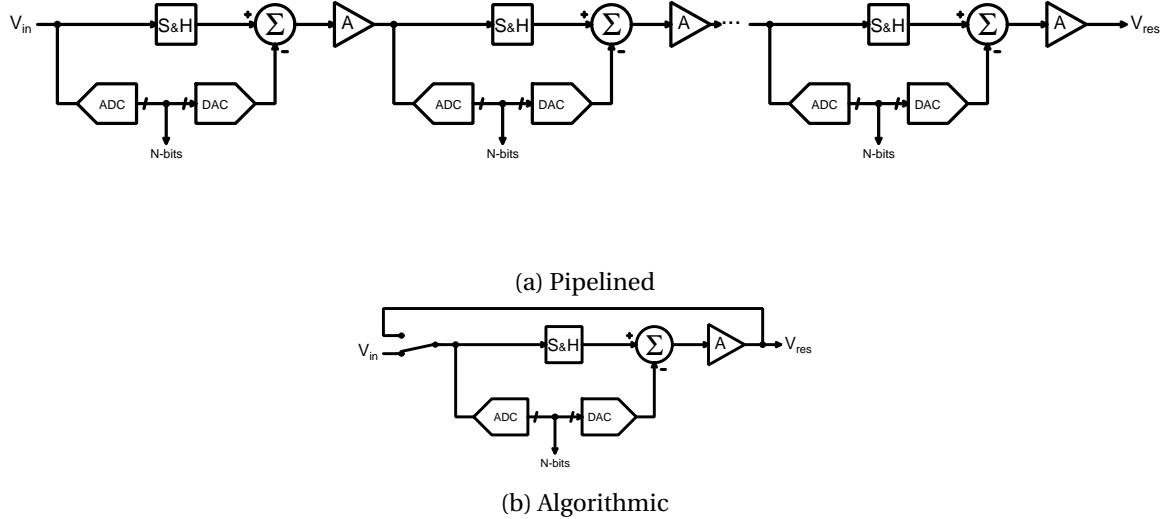


Figure 2.8 Principle of the pipelined and of the algorithmic converter

These architectures have garnered much attention recently due to their low-voltage and higher integration characteristics [37–45]. Systems that inherently require low-voltage operation, such as biomedical and wireless sensor applications, also motivate research in this area and demonstrate their versatility [37–39].

Current mode method offers an ease of implementation of basic functions such as summation and scaling, and they are also appropriate for low voltage application. Some current mode algorithmic have been designed recently [46–49]. Even if current mode design requires lower voltage

swing and increase noise immunity, the accuracy is limited by current mirror matching. This can be improved by increasing transistor sizes and biasing currents. Larger transistor sizes and larger reference current, however, need larger chip area and a higher-power consumption. This trends establishes a trade-off which may turns the proposed Current Mode ADC in a less attractive solution than other ADCs[47].

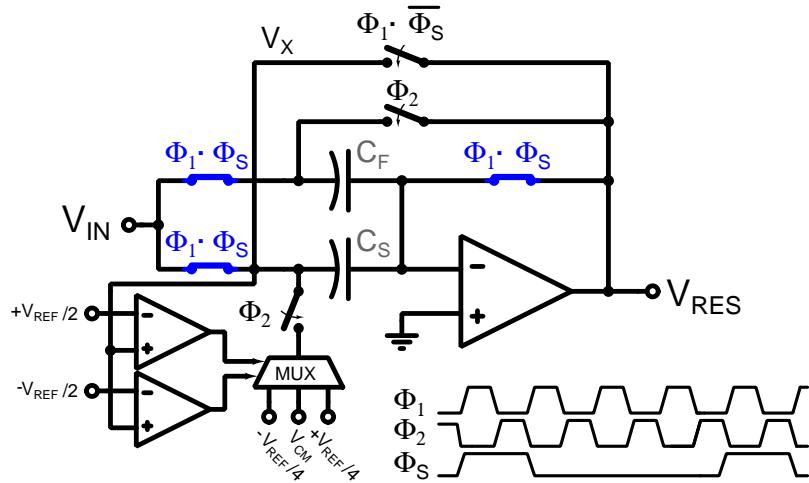


Figure 2.9 Principle of a 3-levels Flip-Around MDAC in the realization of an Algorithmic converter

A common implementation of the algorithmic converter is by building the stage around a Flip-Around Multiplying DAC (FA-MDAC). This way, the closed-loop gain is defined by a ratio of capacitor whose mismatch is well controlled, as represented in Figure 2.9. A simple differential pair is a valid amplifier to operate under low-supply condition. As the resolution increases (recycling of its inner self error), the gain of the amplifier shall drastically increase. By stacking transistors the output swing is thus limited, and non-linearity occurs. Therefore, medium to high resolution algorithmic ADC requires a digital compensation [50] or an adjustment of its residue curve [51, 52].

The amplifier or Operational Transconductance Amplifier (OTA) is power hungry. Few analog circuits exist to emulate them with a reduced power consumption such as the comparator based MDAC and the ring amplifier based MDAC. The table 2.3 highlights the main characteristics of the algorithmic converters.

2.1.4 Successive Approximation Register

The first appearance of SAR ARC was back in early 70s [56]. Using a binary search algorithm, this kind of converter is by far slower than a Flash or Folding ADC. As represented in Figure 2.10, the SAR does not have any active component such an amplifier making it very efficient and targeting low-power application. But they are also able to perform either high-resolution conversions or high-speed conversions.

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Table 2.3 Algorithmic-Pipelined ADC in the literature

Ref.	Architec-ture	Techno-[nm]	F_{snyq} [MHz]	OSR	Area [mm^2]	Supply [V]	Power [mW]	Res.
[43]	pipe.-SAR	65	50		0.054	1.2	1	13
[50]	pipe.	350	75		7.9	3	290	12
[53]	pipe.	65	50		0.36	1	4	12
[54]	pipe.	28	600		0.62	0.9	14.2	12
[55]	pipe.	180	80		1.9	1.8	94	10

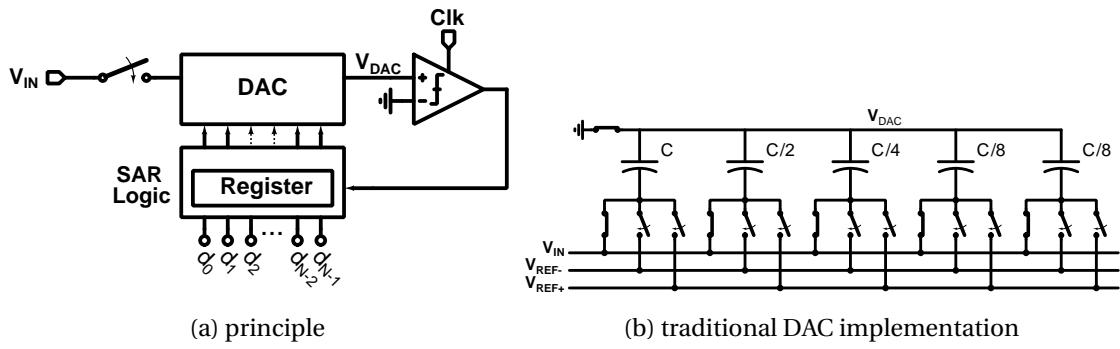


Figure 2.10 Traditional charge redistribution SAR ADC as presented in [56]

The architecture also benefits from using only one comparator to reduce the occupied area. With recent progress, the SAR converter outperforms power consumption and. Besides, its area occupancy have been tremendously shrunk; the speed have been improved. Power dissipation sources are the digital control circuit, the comparator, and capacitive reference DAC network. The advancement in technology also favors the speed of the digital logic while the power consumption of the comparator and the capacitive DAC is limited by mismatch and noise [57–59]. To address both the area occupancy and further reduce the energy consumption, the DAC architecture can be optimized by decreasing the capacitance and still preserving the binary scale.

2.1.4.1 DAC Enhancement

Having high resolution SAR ADC is quite challenging. Using a binary weighted capacitive reference in the DAC network leads to a increasing number of capacitors. Stereotypical capacitive DAC forms a binary scale split into a bunch of unit capacitors, so that the n-th capacitor in the scale is a group of 2^N of them. To increase the resolution from N to N+1, we double the number of unit capacitors. Thus, the occupied area grows exponentially as the resolution increases. And considering a differential structure, the phenomenon is even more pronounced causing lateral effects such as an excessive reference voltage loading.

Conventional techniques to shrink the area and to relax constraints on voltage buffers, designers usually play with serial-parallel configurations of unit components. This results into well-known techniques called split-junction and split-capacitor. The split-capacitor as represented in Figure 2.11a inserts a capacitor which scales down a segment of the DAC. Thus, the biggest capacitors can be sized down to preserve the scale. The diminution of load provides substantial power saving. The implementation obstacle is introduced by the attenuation capacitor not being a multiple integer of the unit capacitor. Moreover, an extra switch per segmented DAC is introduced for the sampling of the input signal. Thus, the thermal noises is increased by both the scale down of capacitance and by the extra noise sources switches represent.

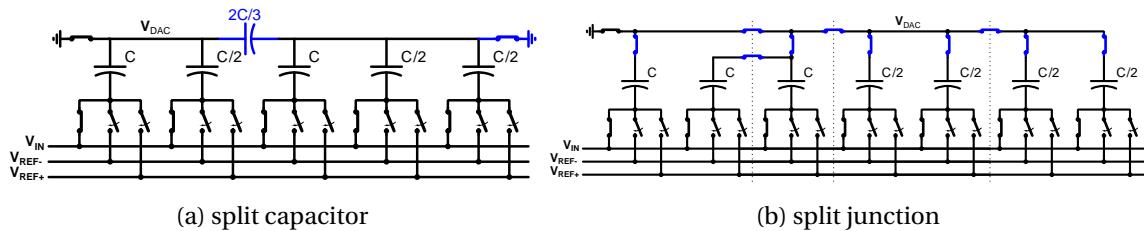


Figure 2.11 DAC optimization by altering capacitors connections

Instead of connecting an attenuation capacitor in series to weight down part of the DAC to reduce the size of the biggest capacitors, small capacitors cunningly connected in parallel to split charges stored by the expected ratio. Introduced in [60] and optimized in [61], the split junction scheme has a superior efficiency by reducing the number of “down” transitions by appending extra sections in parallel to redistribute charges. The two-step junction-splitting capacitor array requires more switches than the conventional and junction-splitting ones as depicted by the Figure 2.11b. Compared to a classical DAC, this technique reduces the total capacitance by a factor $2^{N/2}$ and have almost the same area saving than a Split-capacitor method. From a thermal point of view, this architecture is more sensitive to thermal noise by adding noise source on the floating node V_{DAC} . The floating node connected on the comparator inputs leads to excessive decision error at high temperatures. Such error could be mitigated with the help of redundancy and non binary ratio of the DAC scale [62].

2.1.4.2 Switching Methods

The low-power asset of the SAR ADC can further be improved by a careful attention of switching energy loss. In the conventional charge-redistribution switching, the input voltage is sampled on all capacitors of the DAC during the first clock cycle. Then, we proceed in a voltage inversion and we remove half of charges stored by connecting V_{refp} to one half and V_{refm} on the other half. Since this end of the capacitor is already at V_{inp} (resp. V_{inm}), the energy is dissipated in switches to charge half of the capacitance and discharge the other half. In case the output bit $d_1 = 1$, the next capacitor is tested. As the weight of this capacitor is half of the previous one, there is less

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dissipation. Otherwise, the charge/discharge operation is reverting and the next capacitor is tested. The conventional charge-redistribution method is thus not power efficient owing to the discharge of the capacitor under test and charging-back this capacitor [63]

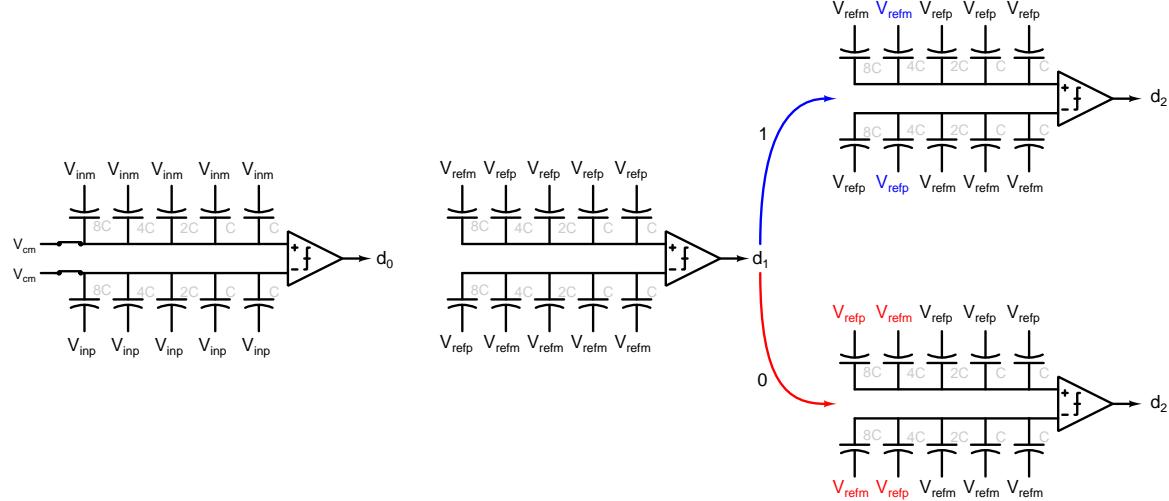


Figure 2.12 Traditional charge-redistribution conversion

Even if lot of progress comes by a load reduction as discussed previously, the switching can strikingly reduce the power consumption; as far as 98% of the conventional switching scheme [64–66]. The first technique which draws attention was the monotonic switching. Since the first clock cycle is the more power hungry, the monotonic switching samples the differential input voltage on the top-plates of capacitors while the common-mode voltage V_{cm} is applied on the bottom-plates. As represented in Figure 2.13, the comparator determines first bit d_0 as polarity of the differential voltage [63]. Compared to the conventional switching method, the reset of the MSB capacitor is saved. Moreover, a N-1 bits DAC is sufficient to output N-bits. According to the comparison results, the logic unit will connect the largest capacitor of bigger voltage side to the ground, and the other side remains the same. Therefore, almost half of the switching energy is saved. However, the common-mode level is decreasing during the monotonic switching, which puts a high demand on the performance of the comparator.

Moreover, the switching loss is voltage dependent. The reduction of the voltage step diminishes the switching loss in the same proportion. Using V_{cm} instead of the ground already halves the switching energy. In the sampling phase, the differential input is sampled as inputs on the top-plates (V_{DAC}) while the bottom-plates is connected to V_{cm} . After the sampling phase, during each conversion cycle of a V_{cm} -based switching, the bottom plates of the capacitors will be switched in descending order, from V_{cm} to V_{refp} in one-side or another depending on each bit decision as depicted by Figure 2.13. The connection to V_{cm} adds one switch per capacitor increasing the thermal noise sources.

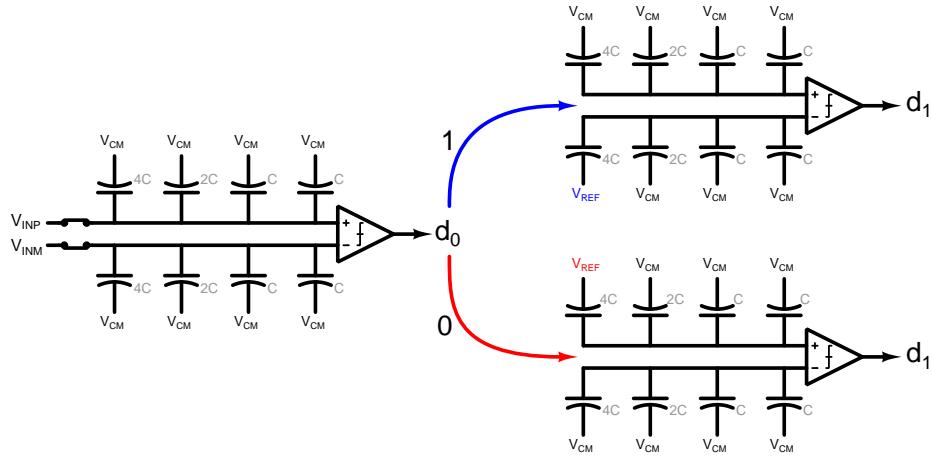


Figure 2.13 V_{cm} -based monotonic digital switching to reduce area and save switching energy

The switching being optimized, a further improvement could come from an assumption on the signal converted. As sensors outputs react slowly and their voltage are usually filtered in front, the input signal of the ADC is of low mean activity over a time window. The conversion can start from an initial guess which is the output of the previous sample [67]. Bit-cycling only last bits, the LSB first conversion performed is power efficient. When the error between the final code and the initial guess overtake few LSBs, a complete conversion shall be performed. Therefore, the power saving is inherent to the nature of the input signal. Without such assumption, the power consumption is higher than previous methods and limit the speed of the conversion.

Compared to the traditional charge-redistribution scheme, these switching methods engender a large common-mode variation. This puts an extra design constraint on the comparator making decision. For instance, the monotonic scheme allows only PMOS differential pairs which limit the maximum speed of comparison.

2.1.4.3 Synchrone and Asynchrone Digital Implementation

To optimize the digital circuitry, the clock rate is deeply linked to the power consumption. However, it enters in conflict with specification for a manufacturable design. Indeed, the internal clock limits the settling time of DAC and the decision time of the comparator. For a robust design, one might base the sampling frequency on the peak delay in the worst corner. By using an asynchronous logic, such constraints could be relaxed on the comparator design. The conversion time T_{conv} shall respect at least the following inequality

$$T_{conv} >= \sum_{i=0}^N t_{cmp,i} + t_{Logic,i} + t_{DAC,i} \quad (2.3)$$

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where $t_{cmp,i}$ is the delay of the comparator, $T_{Logic,i}$ the propagation time of the logic toggling switches, $t_{DAC,i}$ the settling time of the DAC.

In a synchronous SAR, the two clock phases are used such that the first phase is dedicated to the DAC settling and the reset of the comparator whereas the second phase is devoted to the comparator decision and finish the settling. Also, the digital logic should control when the comparator resets and the moment to make a decision. With regard to the logic, a delay larger than the total delay from comparator to the switching signals shall be ensured between a ready signal and the new decision start [68]. By using a single XOR or NAND gate of the comparator outputs, a ready (valid) signal can be asserted [68–71]. In turns, the ready signal triggers the reset of the comparator and the DAC settling. A delayed copy of the ready signal starts a new decision. This solution based on standard cells still requires delay cells. The delay sensitive to PVT variation, an asynchronous control is preferred. As done in Figure 2.14a, two loops can control respectively the reset and the next decision latching [72]. Unfortunately, the double-input T-flip-flop is not among standard cells in many processes. Moreover, the loop of the reset (in blue) should be ensured to be faster than the loop of the set (in red) over PVT variations after place and route. S.S. Wong *et al.* presented switching signals to trigger the asynchronous loop instead of a fixed delay of comparator ready signal or asynchronous loop [73]. The process variation problem caused by the control logic and buffers is thus overcomed without any tunable or worst-case delay cells. Represented in Figure 2.14b, this also has the benefit of more easily ensure that DAC settling is started before triggering the comparator.

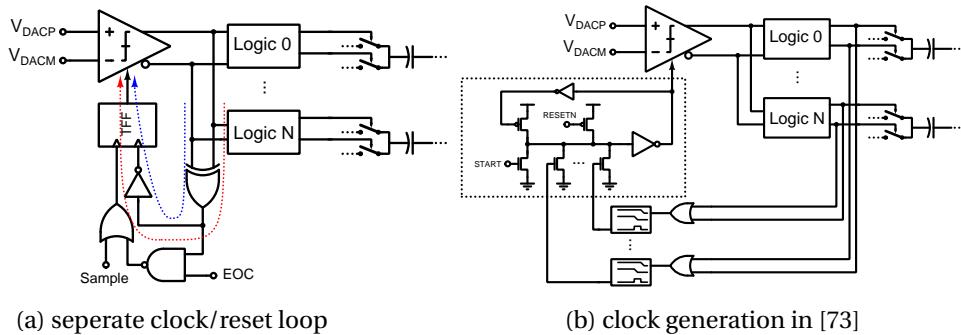


Figure 2.14 Comparator's clock generation

In addition, when the input voltages of the comparator are closer to each other, the comparator decision in either way to zero or one lasts longer. At low-temperature when the noise is not sufficient to force the latch in a state, metastability is inevitable. For unusually too long decision time, the digital code might be incomplete and result in errors. In the work of Tung *et al.*, a timer circuit provides a timing slot which at the end a flag is raised to indicate the metastability and force the execution of subsequent cycles [74]. Moreover, the PVT variations alter the settling of the DAC. Instead of waiting the full settling and sizing accordingly delay cells, [75] suggests that decision

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errors due to a partial settling can be tolerated with redundancy. An erroneous decision in the redundant region, via the non-binary scale of the DAC, is corrected by a latter decision.

For the SAR logic, a shift register cadenced by ready (valid) signal is implemented and generates the end of conversion flag for the asynchronous clock generator [68, 71]. To the contrary, one could waits for the ready (valid) signal of the LSB logic as in [73]. The table 2.4 gives as an abstract the main characteristics of these converters. Most of them achieved high speed and a low/medium resolution with fairly small power consumption.

Table 2.4 SAR ADC in the literature

Ref.	Architecture	Techno. [nm]	F_{snyq} [MHz]	Area [mm ²]	Supply [V]	Power [μW]	Res.
[62]	1.85-radix classic CDAC	65	10	0.01	NA	50	15
[71]	classic CDAC asynchronous	180	20	1.61	1.8	1770	12
[76]	split-cap Vcm-based	90	100	0.18	1.2	3000	10
[77]	classic CDAC Monotonic	130	50	0.05	1.2	826	10
[78]	classic CDAC asynchronous	90	10	0.05	1	26	8

In summary, a full-flash converter is power hungry, and only one kind of ADC is not sufficient to reach high resolution within 5-clock cycles. A cascade of sub-ADCs seems more promising. Architectures which suffer less from the analog deficiencies are $\Delta\Sigma$ -based architectures, and the SAR. In addition to that, SAR ADCs using a charge redistribution are energy efficient. These are less limited by technology and supply voltage scaling compared to others. However, in a $\Delta\Sigma$ -based architecture, the re-use of an integrator outputs imposes important constraints on the amplifier. The latter should thus meet these over the full temperature range.

2.2 Analog design under wide-temperature range

There are many industries such as the automotive that smart sensing and mixed signal electronics capable of operating within an extreme temperature range from -40 °C to 175 °C. At high temperatures, transistors suffer from several defects which degrade their performance which leads to the system performance variation.

Over such a large temperature range, physical phenomena due to temperature variation should be considered in early design stages. The background presented within this section discusses the impact of the temperature at the device- and circuit-level. Moreover, the material dependencies, as well as transistors variation with respect to the temperature, are illustrated with the CMOS XT018 technology results.

2.2.1 Physical limits

2.2.1.1 Energy Band Gap

In solid-state physics, the energy band gap is the energy required to supercharge an electron from the valence band to the conduction band. Any extra energy will change the thermodynamic equilibrium of the solid. Therefore, the electrons' state repartition in the valence and conduction band varies with the temperature according to the Fermi-Dirac distribution. Thus, the band gap energy changes with respect to the temperature. These intrinsic properties are widely used for temperature sensing, voltage and current references, and temperature compensation circuits.

Even if, the fitting equations of low-temperature data have been greatly discussed [79–82], the trends of the bandgap energy required over temperature is modelled easily by the Varshni equation (2.4) in [79]

$$E_g(T) = E_g(T_0) - \alpha \frac{T^2}{T + \beta} \quad (2.4)$$

$E_g(T_0)$ represents the band gap energy required at the temperature of reference T_0 , while α and β are fitting constants. For the Silicon (Si), with $T_0 = 300$ K, α and β are respectively 0.473 meV/K and 636K. $E_g(T_0)$ is given to be 1.166 eV. The change over the temperature range of interest is given by the Figure 2.15 where the derivative with respect to the temperature is about 400 ppm/K.

2.2.1.2 Mobility

Carriers in the doped semiconductor respond to any extra energy: one can accelerate them by the application of an electric field. The momentum gained is $m_c v_c$ where v_c is the drift velocity. The factor of proportionality between the drift velocity and the electric field applied is called the

2.2 Analog design under wide-temperature range

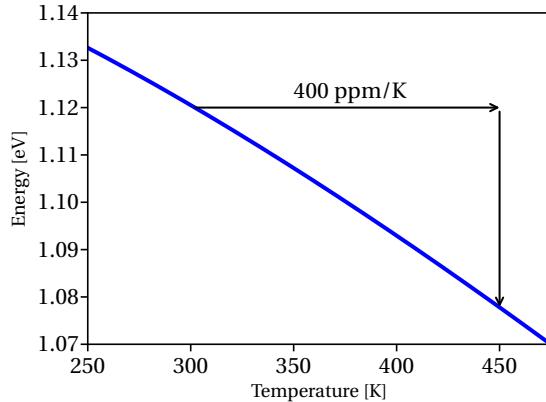


Figure 2.15 Band Gap Energy of the Silicon

mobility μ_c in units of cm^2/V . One should consider that any collision deflecting the carrier is limiting the velocity. Thus, the various scattering mechanisms limit the mobility.

Therefore, the mobility has very complex temperature dependence, defined by the interaction of the following: phonon μ_{ph} , surface roughness μ_{sr} , bulk charge Coulombic μ_{cb} , and interface charge Coulombic μ_{int} scatterings. Each of these depends on the temperature and the electric field ξ_{eff} .

The Berkeley Short-Channel IGFET Model (BSIM), one of the most widely used simulation models and the one of the technology used, combines these four scattering parameters into an effective mobility, μ_{eff} using Matthiessen's rule (2.5) [2].

$$\frac{1}{\mu_{eff}(T, \xi_{eff})} = \frac{1}{\mu_{ph}(T, \xi_{eff})} + \frac{1}{\mu_{sr}(T, \xi_{eff})} + \frac{1}{\mu_{cb}(T, \xi_{eff})} + \frac{1}{\mu_{int}(T, \xi_{eff})} \quad (2.5)$$

The phonon scattering is a vibration of the crystal lattice. The temperature increasing carriers collision are more frequent. The mobility limitation at high temperature is dominated by this scattering mechanism. Theoretical analysis shows that the mobility due to lattice scattering will decrease in proportion to $T^{-\frac{3}{2}}$.

Surface roughness scattering becomes dominant when high electric fields pull electrons closer to the Si/SiO₂ surface ($\mu_{sr} \propto \xi_{eff}^{-2.1}$) [83].

At low temperatures, electrons move more slowly, and lattice vibrations are small. The ion impurity forces which have little impact on high-energy particles become the dominant limit to mobility. In this regime, decreasing temperature extends the amount of time electrons spend passing an impurity ion, causing mobility to decrease as temperature decreases ($\mu_{cb} \propto T$).

At low temperatures, the interface charges have two conflicting dependences. Reducing temperature reduces the carriers' thermal velocity, which increases the impact of interface charges.

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However, the reduced thermal velocity also reduces the screening effect[84], and this reduction in screening dominates the temperature dependence ($\mu_{int} \propto T^{-1}$). For a temperature greater than 200 K, the mobility is decreasing with the temperature increasing.

In the BSIM model of transistor, the mobility change over temperature is modelled as in the equation (2.6).

$$\mu_{eff}(T) \propto \mu_{eff}(T_0) \left(\frac{T}{T_0} \right)^{\alpha_\mu} \quad (2.6)$$

T_0 is the room temperature ($\approx 300K$) and α_μ is a fitting coefficient often set to -1.5 for NMOS transistors in strong inversion.

2.2.1.3 Velocity Saturation

As presented in the Section 2.2.1.2, the mobility and the velocity of carriers are linked to each other as $v \approx \mu\xi$; where v is the velocity, μ the mobility, and ξ the electric field.

One assumption is that the mean free time of carriers between collisions is constant, which holds for low values of ξ . But for high electric fields, the additional velocity component will result in a shorter average time between lattice scatterings, thus the mobility is no longer constant. An increase in energy no longer causes carrier velocity to increase; instead, the additional energy is lost to phonon generation through lattice interactions. The mobility will finally saturate for high electric fields, and it may be approximated by the following empirical expression:

$$v = \frac{v_s}{1 + \left(\frac{\xi}{\xi_{sat}} \right)} \quad (2.7)$$

where v_s is the saturation velocity (10^7 cm/s for Si at 300 K), and ξ_{sat} is a constant equal to 7.10^3 V/cm for electrons and 2.10^4 V/cm for holes.

Although saturation velocity has been found to be a dominant temperature dependent parameter as far back as 1970 [85] using device as longer as $10 \mu m$. In the BSIM4 device model, the impact of temperature on velocity saturation v_{sat} is modelled by [2] as:

$$v_{sat}(T) = v_{sat}(T_0) - \alpha_v \left(\frac{T}{T_0} - 1 \right) \quad (2.8)$$

where $v_{sat}(T_0)$ is the saturation velocity at nominal temperature (T_0) and a α_v is the saturation velocity temperature coefficient. Thus, the temperature degrades the saturation velocity and devices' current.

2.2.1.4 Current Density

The current densities relation related to the temperature is complex and based on two components given by the equation (2.9): the drift and the diffusion.

$$J_N = q\mu_n n\xi + qD_n \nabla n \quad (2.9)$$

$$J_P = q\mu_p p\xi - qD_p \nabla p \quad (2.10)$$

The **diffusion** component corresponds to the displacement of carriers to even their concentration. The gradients of electrons and holes ∇n and ∇p is not dependent from the temperature. But the diffusion rates D_n and D_p are. Increasing the temperature increases particle kinetic energy, in turn, increasing the diffusion component of the total current.

The **drift** component corresponds to the displacement of carriers under a force proportional to the electric field ξ and the mobility μ_n and μ_p . The temperature impacts the mobility as related in Section 2.2.1.2 and the carrier density as well. The carrier density is flat over temperature in the extrinsic region and the mobility is decreasing, one may deduce that drift current density decreases as the temperature increase.

The drift and diffusion currents have opposite temperature dependencies. The global trends of the current density over temperature will depends on the electric field applied.

Transistor's current density ($J_{DS} = I_{DS}/W$) increases as bias increases according to [86]:

$$J_{DS} = \mu \frac{\epsilon_{ox} \cdot \xi_{DS}}{L} (V_{GS} - V_{th}) \quad (2.11)$$

Depending on transistor bias, J_{DS} is drift-dominated under the condition $\xi_{DS} > \xi_{sat}$; but it is diffusion-dominated under the condition $\xi_{DS} < \xi_{sat}$. In contrast to the bias dependency, J_{DS} has opposite temperature dependence while it is drift- and diffusion-dominated due to mobility scattering limitation. In fact, drift-dominated J_{DS} decreases, but diffusion-dominated J_{DS} increases as temperature increases.

To clarify the temperature variation, a simulation experiment is carried out using a n-type (*nel*) low- V_{th} MOSFET of XT018 technology of XFAB. The *nel* transistor is sized with $W = 1\mu\text{m}$ and $L = 180\text{ nm}$ and the current density is represented at the Figure 2.16. Another factor of current change over the temperature is the threshold voltage V_{th} in (2.11).

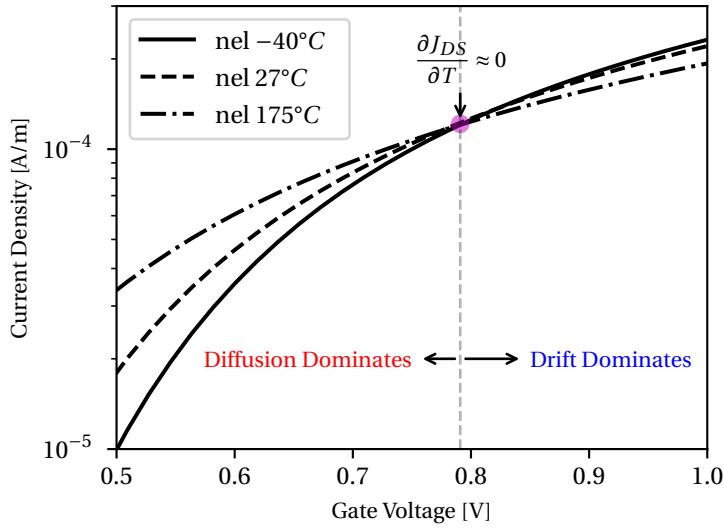


Figure 2.16 Current density of low-VT nMOSFET of $1\mu\text{m}/180\text{nm}$ over temperature

2.2.1.5 Threshold Voltage

The MOSFET threshold voltage is given in the equation (2.12) [87], where V_{FB} is the voltage for which its application yields to a flat energy band in the semiconductor, Φ_F is the Fermi energy, and γ the body effect parameters.

$$V_{th} = V_{FB} + 2\Phi_F + \gamma\sqrt{2\Phi_F} \quad (2.12)$$

Its variation over temperature is found to be defined by (2.13) [88].

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial V_{FB}}{\partial T} + \left(2 + \frac{\gamma}{\sqrt{2\Phi_F}}\right) \frac{\partial \Phi_F}{\partial T} \quad (2.13)$$

The flat band voltage depends on the dopant concentration of the substrate, of the gate, and the intrinsic carrier concentration of the silicon. The fermi energy also changes over temperature as represented in Figure 2.17.

For practical design, the variation over temperature of the threshold voltage is modelled in the BSIM model as:

$$V_{th}(T) = V_{th0} + \alpha(T - T_0) \quad (2.14)$$

where $\alpha = \frac{KT1}{T_0} + \frac{KT1,L}{L_{eff}T_0} + \frac{KT2V_{bseff}}{T_0}$ represents the linearized variation coefficient with respect of the temperature, depicted by Figure 2.18. Figure 2.18a represents both the threshold voltage decreasing with the temperature (solid line) and the thermal behavior for a lot under a 3σ process variation delimited by the shaded area around the average.

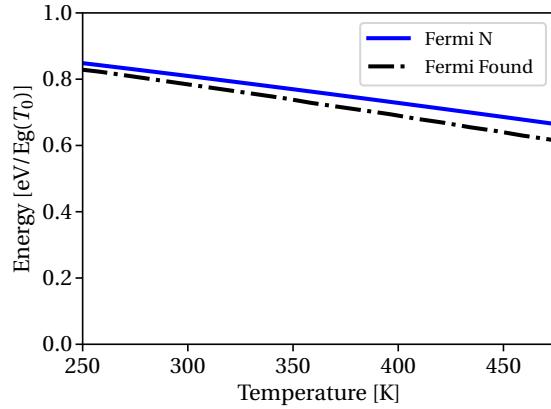


Figure 2.17 Fermi energy normalized over the temperature range of interest without (b-) and with (k-) impurities in the substrate

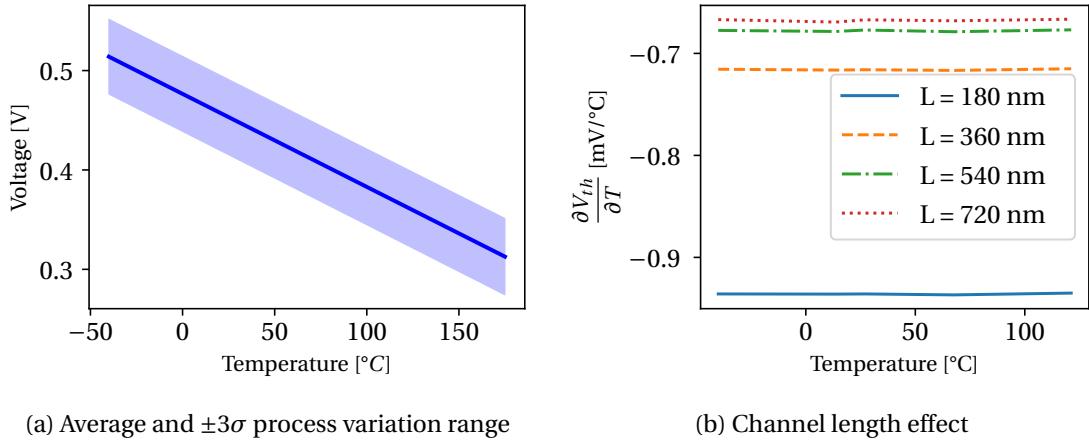


Figure 2.18 Threshold voltage of low-VT nMOSFET of $1\mu\text{m}/180\text{nm}$ over temperature under process and channel length variations

The slope depends on the transistor channel length L and the bulk-source voltage applied. For a voltage $V_{bs} = 0$ as done in the Figure 2.18b, the bigger the channel length is, the less sensitive is the threshold voltage. This offer the possibility to the designer to adjust the sensitivity of the threshold voltage to temperature by either decreasing the transistor channel length or by body biasing [89].

2.2.1.6 Leakage Current

In semiconductor devices, leakage is a quantum phenomenon where mobile charge carriers tunnel through an insulating region. It also comes from the free charges displacement in a region subjected to an electric field. These leakages are represented in Figure 2.19 for a NMOS and PMOS transistor with a partially depleted SOI technology.

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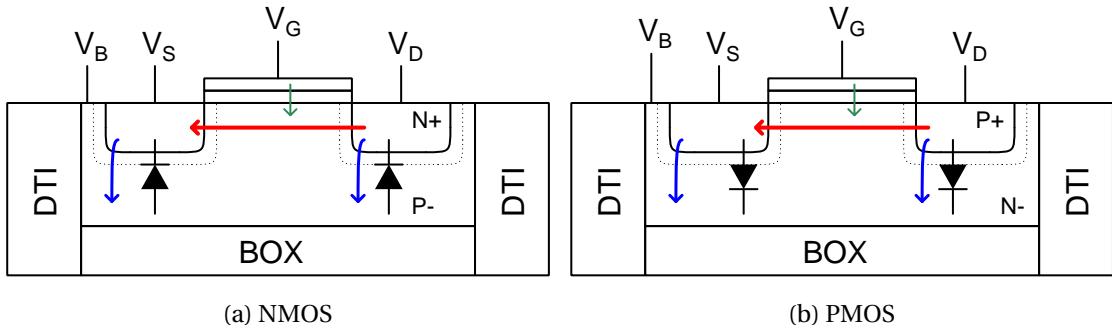


Figure 2.19 Substrate leakage current in SOI transistors

The **off-state current** of a transistor gradually became a limiting factor for down-scaling the threshold voltage since it determines the power consumption of a chip in its idle state. In a CMOS cell at high temperature, these off-state current of NMOS transistor is pump from the useful current of PMOS transistor. It could not be ignored longer and new physical models had to be applied to correctly describe the device behaviour in the so-called sub-threshold or weak-inversion regime [90–92]. This weak-inversion current contributes as:

$$I_{ds}(V_{gs}, V_{bs}, V_{ds}, T) = \mu_{eff} C_{ox} \frac{W}{L} \left(\frac{k_B T}{q} \right)^2 [n(V_{bs}) - 1] e^{q(V_{gs} - V_{th})/nk_B T} \left(1 - e^{-qV_{ds}/k_B T} \right) \quad (2.15)$$

where n is the slope factor, μ_{eff} the mobility of carriers as given in Section 2.2.1.2. The leakage current due to the off state of a transistor is therefore increasing exponentially with the temperature. This is arguably the most challenging constraint on high temperature design.

In addition to that, and without considering contact losses and recombination, charges also diffuse in the substrate. This **substrate-current** depends on the electric field imposed by the MOSFET use case. In the case of a NMOS transistor as in Figure 2.19a, the leakage current flow is either in one of the following configuration:

- $V_B = V_S < V_D$: no charges flows in the intrinsic pn junction at the source but a reverse leakage current exists in the pn-junction at the drain.
- $V_S < V_B < V_D$: the reverse current in the pn-junction at the drain is smaller, and a forward leakage current occurs in the pn-junction at the source.
- $V_S < V_D < V_B$: both pn-junction at the source and at the drain are forward biased. The current flows from the bulk to the each contact.

while for the PMOS transistor,

- $V_B = V_S < V_D$: no charges flows in the intrinsic pn junction at the source but a forward leakage current exists in the pn-junction at the drain.

- $V_S < V_B < V_D$: the reverse current in the pn-junction at the source increases, and a forward leakage current occurs in the pn-junction at the drain decrease.
- $V_S < V_D < V_B$: both pn-junction at the source and at the drain are reverse biased. The current flows from each contact to the bulk.

Based on the Shockley equation, the forward and reverse current of the diode is defined by equation (2.16) where $L_n(L_p)$ represents the equivalent height of the n-block (p-block), while $D_n(D_p)$ is the diffusion coefficients of this block, and n_i is the intrinsic carrier concentration.

$$I_{\text{db/sb}} = q \left(\frac{D_n}{L_n} \frac{n_i^2}{N_a} + \frac{D_p}{L_p} \frac{n_i^2}{N_d} \right) \exp \left(\frac{qV_{\text{db/sb}}}{k_B T} - 1 \right) \quad (2.16)$$

2.2.2 g_m/I_D -based design over temperature

Physical design for analog ICs has not been automated at the same degree as digital IC design. However, computer-aided-design (CAD) can significantly improve the productivity of circuit engineers. As presented in the Section 2.2.1.5, the threshold voltage decreases with the temperature. Thus, a design methodology based on the voltage overdrive ($V_{ov} = V_{GS} - V_{th}$) will be difficult and time consuming. To the contrary, the g_m/I_D methodology employs design charts to accurately size transistors which fits well the purpose of productivity. Moreover, a g_m/I_D -based design methodology links design variables (g_m, f_T, I_d, \dots) to analog macro blocks specification such as the bandwidth, the power consumption, the noise budget, or accuracy.

The analysis of the variations of each circuit's characteristics, as noise figure, gain, bandwidth or power consumption, as function the g_m/I_D parameter over temperature helps us to select the MOS transistor optimum inversion region to have a design cost equilibrated to the temperature related design [93–96].

2.2.2.1 High-Frequency design over temperature

In the design of high-speed integrated circuits, PLL and RF-Amplifiers are few applications among many using transistors at the limit of their speed with an important criterion on the in-band noise. Usually with a low-impedance and at the largest transconductance possible, a transistor acts as a current source or current sink to either charge or discharge the capacitive load. In such circumstances, a very high frequency signal encounters a primary limitation known as slew rate, i.e. a limited speed as long as a transistor is not able to source or sink the maximum current needed by the load; and a second one which is the current-gain-bandwidth of a single transistor, known as the transition frequency f_T . This f_T is the frequency at which the current gain drops to 0 dB.

In a usual common-source configuration, a MOSFET has its transition frequency $f_T \approx g_m/2\pi(C_{gs} + C_{gd})$. In this equation, C_{gs} and C_{gd} are the parasitic capacitance between the gate and the source

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and between the gate and the drain of a MOSFET. The transconductance g_m defined as the derivative of the drain-source current (I_{ds}) with respect to the gate-source voltage (V_{gs}) depends on the transistor size (W/L), the carriers mobility (μ), and the electric field (ξ).

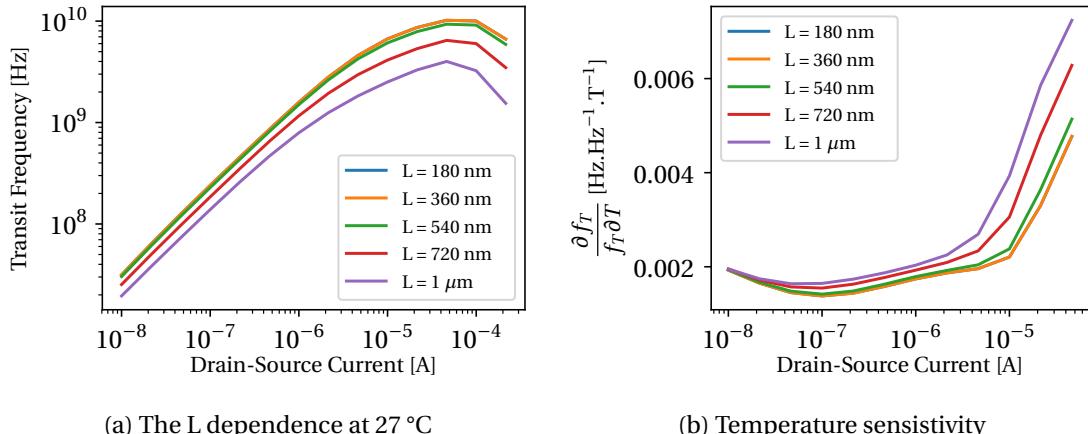


Figure 2.20 Transition frequency f_T at different channel length L and its sensitivity over temperature

From the Figure 2.20, we deduce that:

- increasing bias current increases transition frequency (square root dependence)
- Keeping bias current constant, decreasing length increases transition frequency ($\propto L^{-3/2}$).
- the transition frequency decreases with increasing temperature.
- as smaller the L is, the less sensitive the transition frequency is with respect to the temperature

Therefore, for high speed design, the transistor sizing shall be minimum to decrease the parasitic and to reduce its variation with the temperature. So, technology scaling favors the transition frequency. Regarding the temperature dependence, the current should be minimum to limit the variation of this frequency.

2.2.2.2 Signal amplification over temperature

The design for instrumentation, or the design of a high-resolution ADC, requires very high gain amplifiers. In order to efficiently design such amplifiers, the voltage gain temperature influence should be known in advance to correctly choose the biasing point.

Figure 2.21 represents the intrinsic gain of a single *n*eFET transistor: the product of its transconductance g_m and its output impedance $1/g_{ds}$. For $L = L_{\min}$, the gain falls with the increasing drain-source current, from the weak inversion to the strong inversion. A longer channel length maintains the gain higher over an extended drain-source current range.

2.2 Analog design under wide-temperature range

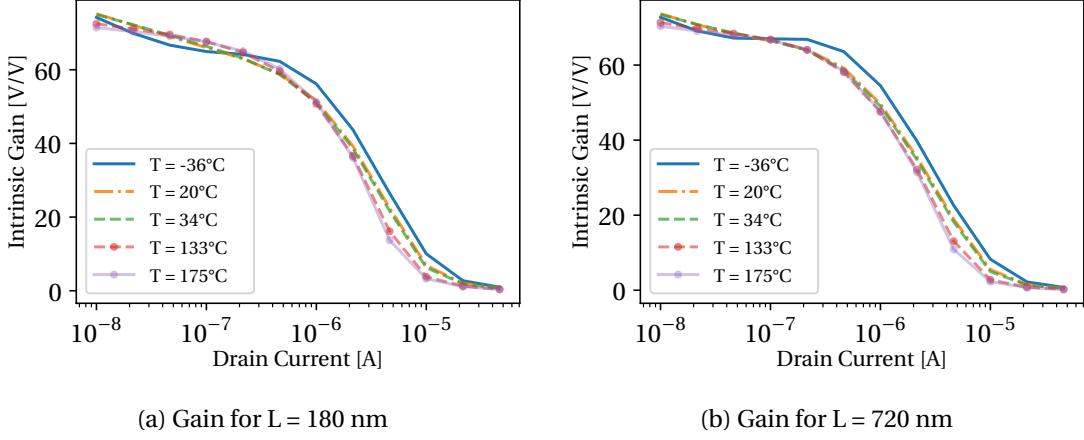


Figure 2.21 Intrinsic gain g_m/g_{ds} at $L = L_{\min}$ on the left and $L = 4L_{\min}$ on the right

The sensitivity of the intrinsic gain to temperature is depicted by Figure 2.22 for different channel length in both weak inversion and in strong inversion. In weak inversion, the gain is increasing with temperature while in strong inversion the gain is decreasing. The channel length only shifts the biasing current at which the derivative of the gain with respect to the temperature changes its sign. This trip point current is higher with small channel length compared to longer ones.

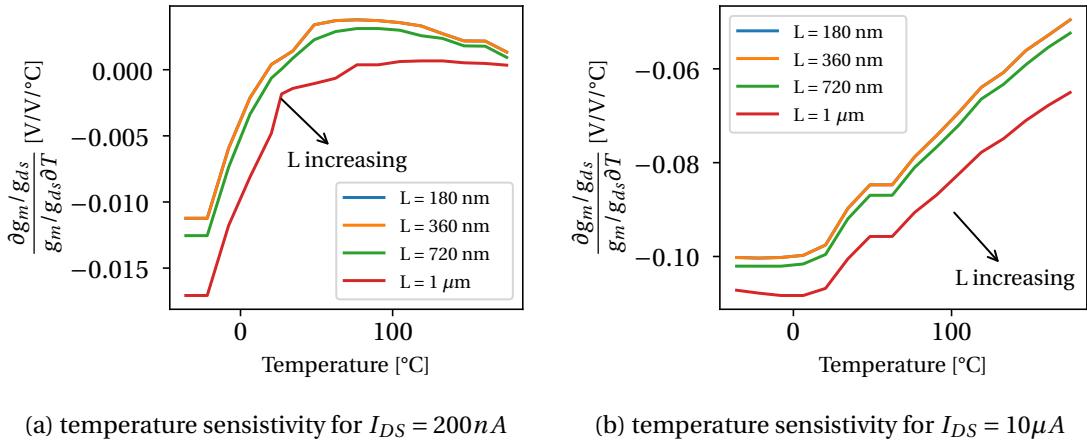


Figure 2.22 Intrinsic gain g_m/g_{ds} temperature sensitivity in different inversion level

The intrinsic gain temperature sensitivity is depicted by Figure 2.22 for different channel length in both weak inversion and in strong inversion. In weak inversion, the gain is increasing with temperature while in strong inversion the gain is decreasing. The channel length only shifts the biasing current at which the derivative of the gain with respect to the temperature change its sign. This trip point current is higher with small channel length compared to longer ones.

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Therefore, a design for high accuracy should be done in weak inversion. The weak inversion gives the maximum of the intrinsic gain and reduces the temperature sensitivity. A first trade-off between the gain and the speed occurs.

2.2.2.3 Low-Power Design Consideration

As the opposite of speed, the design for low-power reduces the current consumption to its maximum. Therefore, the speed is limited. Moreover, a particular attention is paid to the minimize the leakage currents. From the equation (2.15), the designer should decrease the gate-source voltage, the drain-source voltage (power supply voltage), and increase the transistor channel length (L). Therefore, the transistors should be biased in a diffusion dominated region where the transition frequency is low. Besides, the transition frequency degradation with respect to the temperature is limited to approximately 2000 ppm/°C according to Figure 2.20b. Moreover, the increase of the channel length limits the decrease of the threshold voltage as represented by Figure 2.18b.

2.2.2.4 Low-Signal-Distortion over temperature

A single MOSFET transistor is a transconductance amplifier by itself. The linearity can be considered as the input gate voltage range for which the current changes is minimum. Defined that way, the sensitivity of the current with respect to the input gate voltage is related to the g_m/I_D ratio [97, 98].

Figure 2.23 represents the variation of current dependence to the gate voltage, the temperature and the channel length. For the sake of clarity, this is plotted for only $V_{ds} = 0.45V$. Disregarding V_{ds} , increasing V_{gs} is beneficial for linearity. This implies to work in strong inversion where the intrinsic gain is minimum, and the speed is maximum.

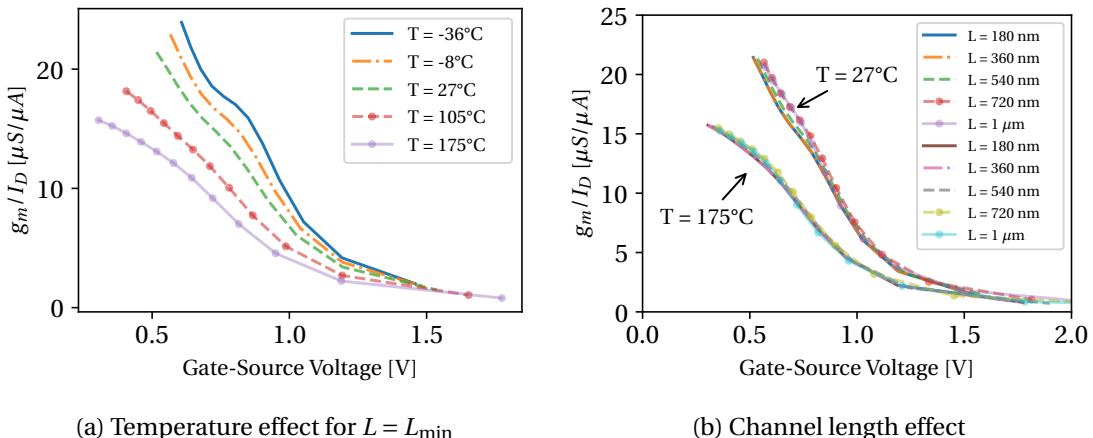


Figure 2.23 Intrinsic gain g_m/g_{dS} temperature sensitivity in different inversion level

2.2 Analog design under wide-temperature range

In Figure 2.23a, the temperature lowers the g_m/I_D ratio and keeps it small over an extended V_{gs} for $L = L_{\min}$. In other term, the temperature is beneficial and improves the linearity range. As represented in Figure 2.23b, the channel length has a reduced impact compared to the temperature. Moreover, the temperature has almost the same impact whatever the channel length is for small V_{ds} .

2.2.2.5 Tradeoffs for a temperature-driven design

Nowadays ADC target ever more high speed and higher resolution. Pushing design constraints in a precise corner in the possible design set. As discussed in Section 2.2.2.1, the speed of a single common-source transistor is severely reduced by the temperature.

Temperature variation in semiconductor physics is widely studied in the literature. Since 1995, C. Park *et al.* have described the trade-off between mobility (μ) and threshold voltage (V_{th}) under temperature variation [99]. The reduction in mobility at high temperatures affect most the speed of the circuit and the reliability. To counterbalance, MOSFETs can be biased near the zero temperature coefficient (ZTC) point that oppose threshold and mobility variations with temperature within MOSFETs [88, 100]. In a stringent area constraint, the ZTC biasing restrict the maximum achievable speed. Another mean is to implement temperature compensation circuit that either adapt the gate voltage [101, 102], or pre-distort the inputs [103], or generate a constant current.

Depending on the system constraints, one solution is preferred over another. For instance, in high-speed switched capacitor circuit (above 100 MHz), a very high DC-gain stable over temperature is a challenge. A constant Gain-Bandwidth Product (GBW) or Unity Gain Frequency (UGF) over temperature is more attractive considering a digital calibration able to correct linearity error due to the Gain and the UGF limitation. The Figure 2.24 represents the MOSFET operating plane and describes the trade-offs as presented by [104]. The temperature analysis and effect are added in blue.

The design of high-resolution and high-speed OTA is the bottleneck of high-performance ADCs: the accuracy in switched capacitor circuits is essentially based on the gain and the speed of the OTA. Based on this analysis, the temperature affect the speeds of transistors, and it cannot be prevented. While the gain could be stable over temperature, this can only be ensured for transistors in weak inversion. In this mode, the a single transistor of the technology cannot exceed 200 MHz. Therefore, biasing circuitry would be in weak-moderate inversion region with large-L. And high-speed differential pairs should be in moderate-strong inversion region with small-L.

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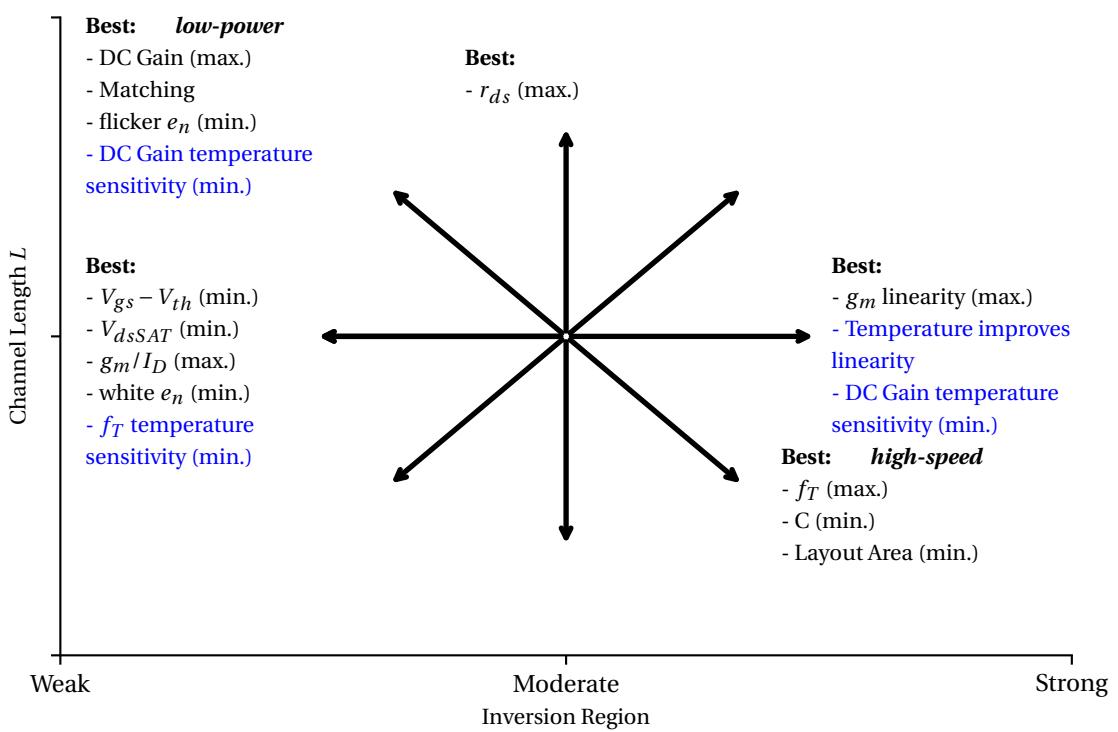


Figure 2.24 Trade-offs in circuit performance as a function of the channel length L and the Inversion level

2.3 High Temperature ADCs

Until now, only standard topologies and recent progress among them have been reported. High-speed and medium to high resolution converters are an extended topic. With the temperature constraints previously explained, this topic is fairly reduced since only few papers address this challenge. This subsection discuss work published to cope with high temperature in ADCs.

From a high-level point of view, solutions with fewer sensitive components over wide temperature range are preferred. As the temperature deeply impacts the analog electronics more than a synchronous digital, SAR without amplifier or $\Delta\Sigma$ ADCs are less demanding on analog accuracy. Thus, they are popular architectures among many for harsh environment applications.

2.3.1 SAR

Even though SAR have a limited number of active components, the resolution of SAR exhibits a limiting factor temperature dependent. Indeed, the temperature increase raises the leakage current exponentially which also discharge capacitors faster. For a DAC based on poly-resistors having the lowest thermal variations, the leakage currents alter the voltage across them. Over a wide temperature range, SAR ADC are only used as a small sub-ADC or as a low-resolution ADC.

In the work of Rahman *et al.* [105], the ADC consists in an 8-bits R-2R poly-resistor DAC driven by a binary search algorithm logic from 25°C to 300°C. Poly-resistors have been chosen for their lowest temperature coefficient in the technology while the comparator and the logic is implemented in a SiC FET transistors. The large-bandgap of SiC reduces the leakage currents. Despite this, the resolution is limited to 8-bits which reveal how important is the leakage currents. Experimental results highlight the fact that ADCs have a better linearity at high temperatures when the dominant factor are switches non-linearity.

Recently, an overview of an analysis of latched-comparators performance, considering process variability and temperature variation from -40°C to 175°C was presented. Fonseca *et al.* [106] have extended such analysis to the metastability and performance metrics variation of SAR ADCs. Besides the known advantages of the Double-Tail comparator, Fonseca's work has demonstrated that such a comparator has a serious drawback under harsh environments. Finally, post-layout results have been presented. Once the SAR ADC is calibrated and operated at a frequency of around 100 MHz, the ADC performance can be maintained in a wide temperature range. Both SA- and DT-SAR ADC achieve an ENOB of 9.8 bits, which is reduced to 9.6 bits in high-temperature operation.

2.3.2 $\Delta\Sigma$

$\Delta\Sigma$ modulator is known to be resilient to analog circuit impairment by transferring the complexity to the digital domain. Nevertheless, the leakage current turns out to be the main contributor to significant voltage drop in switched capacitor circuit. Due to this reason, a fully differential ADC lower the impact on the accuracy to the leakage difference of the positive and negative branch [107]. For low-OSR modulator, experiments have demonstrated that single-stage modulator are more resistant to high-temperature than MASH cascaded one. The latter underwent severe drift of the amplifier output common-mode voltage up to 255°C degrading overall performance of MASH solutions. The $\Delta\Sigma$ modulation reaches high resolution for a large temperature range. Such results were demonstrated either in a bulk technology [107] or in an SOI technology [108].

2.3.3 Pipelined

Keeping aside these architectures, a pipelined based on Flip-Around MDAC has been proved to work under stringent temperature range from -180°C to 120°C in a bulk technology [109]. At negative temperatures, the amplifier is prone to a transconductance reduction and a reduced gain owed to the threshold voltage increased. Large W/L transistors reduce the threshold shift while they improve the matching property. As expected, the pipelined architecture with a 5 MHz sampling frequency in [109] is faster in comparison to $\Delta\Sigma$ ADCs for a resolution of 12-bits.

2.3.4 Mixed Architecture

In the implementation of a CMOS temperature sensor in the -40°C to 125°C range, Souri *et al.* present a second-order Zoom-ADC [110]. A capacitive SAR ADC performs a coarse conversion to determine a rough estimate followed by a fine conversion by a second order Incremental- $\Delta\Sigma$ converter. The SAR first proposal allows one to remove the sample and hold introducing large error as the temperature increase. Using well-known robust sub-ADCs, only single temperature point calibration effectively trims inaccuracy over the wide temperature range. This ADC achieves a resolution of 16-bits, and a power consumption drastically low of 8.6 μW .

The table 2.3 compares performance of converters in prior art.

Despite the heavy work on the temperature to enhance ADCs, the following references achieve valuable results at high temperature but disregards what happen at negative temperature [105, 107, 108]. It is worth to point out that high resolution converter are based on $\Delta\Sigma$ modulation such as in the work of [107, 108, 110]. The ADC performance reliability can be maintained in a wide temperature range according to [106]. Finally, the closest ADC from our expectation is an hybrid architecture presented in [110]. Nevertheless, the latter operates for a reduced temperature range which does not exceed 125°C. A new solution shall be considered.

Table 2.5 High-Temperature ADC in the literature

Ref.	Archi.	Technology [nm]		F_{snyq} [kHz]	Temperature Range	Supply [V]	Power [mW]	Res. [bits]
[106]	SAR	180	SOI CMOS	5000	-40°C–175°C	1.8	0.35	9.8
[105]	SAR	1200	SiC	64	25°C–300°C	5	1.4	8
[107]	$\Delta\Sigma$	1500	Bulk CMOS	1	25°C–225°C	5	NA	14
[108]	$\Delta\Sigma$	500	SOI CMOS	2	25°C–225°C	3.3	NA	16
[109]	pipe.	500	Bulk CMOS	5000	-180°C–120°C	3.3	30.4	12
[110]	SAR+ $\Delta\Sigma$	160	Bulk CMOS	NA	-55°C–125°C	1.8	8.6×10^{-3}	16

A NEW MIXED ADC TOPOLOGY

3.1 Architectural Study

The goal of this research project is to define and to implement a low-OSR ADC for high-speed conversion at 20 MSamples/s with a high-resolution within the smallest silicon area possible. Based on 40 years literature in the ADC domain, only one kind of ADC is not sufficient to match the different desires within 5-clock cycles. A cascade of sub-ADCs seems more promising. Within 5 clock cycles per sample, sub-ADC do not give enough bits as well as the SAR, the algorithmic, the folding, or the counting. And a full-flash converter would exceed the 15 mW budget we fixed for the ADC.

Aware of the large resolution drop at high temperature, and with a high-sensitivity to process variations, a true pipelined ADC cannot be used as is considering the area, and the power consumption. Over an extended temperature range from -40°C to +175°C, an ADC having each stage of a different kind would allow us to mix strength and weakness of each one, to reduce the area overhead and the power consumption.

We propose in this section some candidate topologies for the realization of a high performance ADC. The main functional characteristics of these stages are gathered at the Table 3.1.

Table 3.1 Functional characteristics of mainstream architecture presented in Section 2

	Oversampled	Precision/stage 1-bit converter	Sample & Hold required	Has a residue	multibit conversion possible
Pipelined	No	1	NA	Yes	Yes
Counting	Yes	$\log_2(OSR)$	Yes	Yes	Yes
Algorithmic	Yes	OSR	No	Yes	Yes
Flash	No	1	NA	No	Yes
SAR	Yes	$OSR - 1$	No	No ¹	No

All kinds of stages cannot be connected together due to topological constraints. To list some of them, Flash and SAR stages should always be the last stage as they produce no residue. If the SAR is not the last-stage, an extra amplification with high gain is required at the output of the SAR. When counting stages are cascaded, a sample and hold stage is required between them. And considering the sensitivity to non-idealities and noise filtering, counting stages should be used before algorithmic ones.

¹at the price of extra area and power consumption to sample and hold or to buffer

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As a rule of thumb, to reduce the area, the topology of the ADC should minimize the total amount of components. In consequence, the resources required for each kind of stage are gathered at the next table where N is the number of digital levels produced by the stage.

Table 3.2 Mandatory resources to estimate the area required and the potential intrinsic noise contributor

(For Single-Ended implementation)	Comparators	OTA	Capacitors	Switches
Pipelined	$N - 1$	1	2	$5 + N$
First Order	$N - 1$	1	2	$4 + N$
Counting	$N - 1$	1	$2 / 3$	$5 + N / 4 + 2(N - 1)$
Algorithmic	$N - 1$	0	0	0
Flash	$N - 1$	0	2^{OSR-1}	$3(OSR - 1)$
SAR	1	0		

From all these constraints, we deduce some possible candidates to achieve the resolution of 12-bits with a limited oversampling ratio. A MASH or an Extended-Range followed by a last sub-ADC of any kind benefit from the noise shaping of the $\Delta\Sigma$ modulation with a limited sensitivity to analog defects with few components.

3.1.1 Pipelined of Counting ADCs

The converter is composed with several counting stages, each of them being composed with first-order or second-order sigma delta. The clock frequency of the counting stages is the Nyquist frequency multiplied by the OSR of the converter. In the case of first order counters, The resolution is the ADC resolution multiplied by $\log_2(OSR)$. For example, with a 3-level ADC and OSR=5, the resolution of each counting stage is approximately 3.5 bits.

Among the three configurations of the Figure 3.1, the first one is made of 4 first order Incremental- $\Delta\Sigma$ modulator. The maximum reachable resolution is therefore a 14 bits one. At a clock frequency of 100 MHz, the power hungry element is arguably the OTA. Built around 4 of these this configuration is not the most efficient one and the total area becomes large.

The last stage could also be a Flash or a SAR. Only using 3 OTAs, the power consumption is more reasonable. The second configuration, with a flash at the end, is able to achieve a 13.5-bits resolution with the employ of 13 comparators. The power and area of 1 OTA are now allocated to 5 extra comparators. Willing a fully differential implementation of the design, the choice in favor of this configuration is not justified.

As soon as the OSR is high-enough, the SAR technology will be more efficient than the FLASH in terms of area and consumption. And this last configuration is the most promising out of those three. The power budget of 15 mW at 20 Msamples/s sounds reachable based on an architecture

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quite similar: in [36] a 1-1-1 MASH CT- $\Delta\Sigma$ consumes 19.7 mW at 50 Msamples/s in a 40 nm technology supplied at only 1.2 V for a resolution of 11-bits.

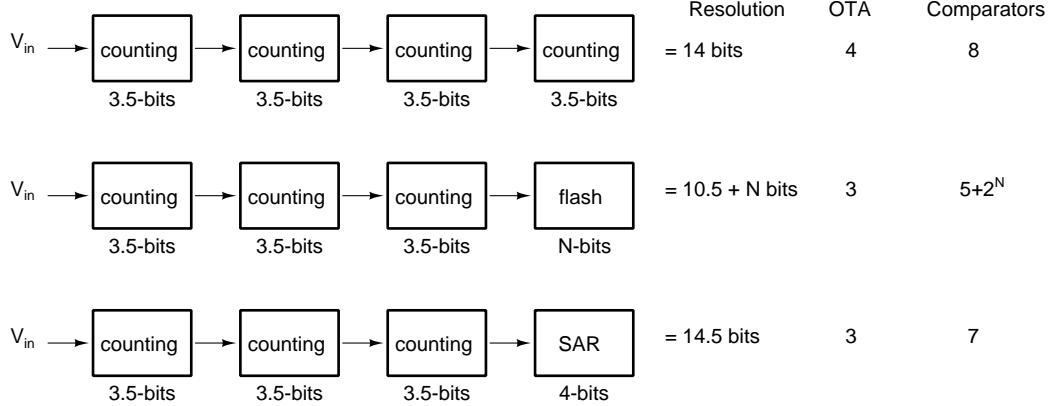


Figure 3.1 Possible candidates leveraging the strength of the $\Delta\Sigma$ modulation to achieve the expected resolution with the resources needed

3.1.2 Extended-Range with extra stage

The topologies in this section are composed with two kinds of stages: counting and algorithmic. A final stage of a third kind such as a SAR is proposed. Algorithmic stages are the most sensitive to non-idealities. This is why they always follow and not precede the counting stages.

The forth configuration of these last three is similar to previous ones. The 1-1 MASH at the input is the least sensitive to non-idealities while the noise shaping is still effective at low-OSR. Despite this, the algorithmic copes clumsily with transistor non-linearity. And a 2-bit flash is sufficient to make a 13.5-bit ADC with in total 9 comparators. Therefore, this solution is expected a larger silicon footprint than the third possible configuration.

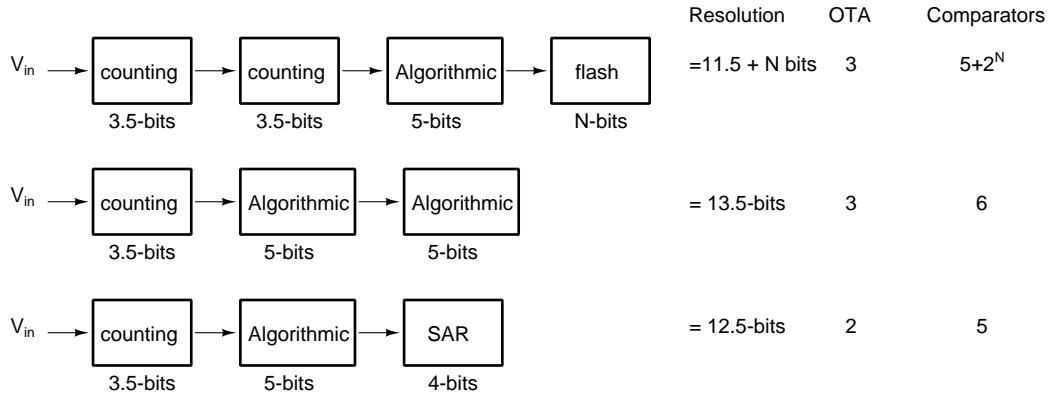


Figure 3.2 Possible candidates leveraging the strength of the $\Delta\Sigma$ modulation and the fast signal information extraction of the algorithmic with the resources required

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The fifth proposal gets rid of a stage and 3 comparators to achieve the same resolution. Unfortunately, the analog defects have a deeper impact due to the presence of two consecutive algorithmic stages. The last proposal replaces the final stage for a SAR having only one comparator. The advantages are three fold: first, the SAR scales well with the technology while it consumes very few. Second, the number of OTA is reduced to only two for the sake of power consumption saving. And third, this architecture is less sensitive to analog non-linearity.

Among the six different configurations which have been proposed, the last configuration uses three different architectures to reduce the footprint, the power consumption while preserving a reachable resolution greater than 12-bits. In consequence, the latter is selected for the design of the new harsh environment ADC.

3.1.3 The selected topology

Previous sections briefly presents the possible candidates and the reasons of the proposed architecture. The current design of the proposal is based for an oversampling ratio of 5, but allows us to perform conversions with an oversampling ratio of 6. In consequence, the SAR is designed in this way while the two first stage design is OSR independent. The selected architecture is represented in Figure 3.3 with more details about the operation and resources involved. While a severe drop of 2 bits can be experienced over 150°C as in [108], Reaching a maximum of 12.5-bits is not sufficient.

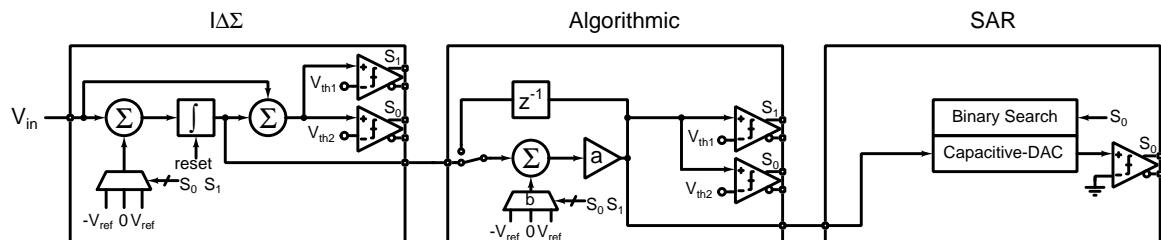


Figure 3.3 Early proposition of the ADC architecture

To provide extra margin, the modification highlighted in Figure 6.2 consists in adding an extra comparator S_2 of the second stage to extract the polarity of the second stage residue. The comparison results corresponds to the first decision made by a binary search algorithm such as the one used in the last stage. By an appropriate threshold voltage for comparators of the 3-levels quantizer previously used (S_0, S_1), leads to the third stage second decision.

The change of the bits distribution into 4-bits from the second stage, and 6-bits for the last stage allows us to extract 1 extra bit. The next section discusses in detail the implementation of the selected architecture depicted in Figure 6.2.

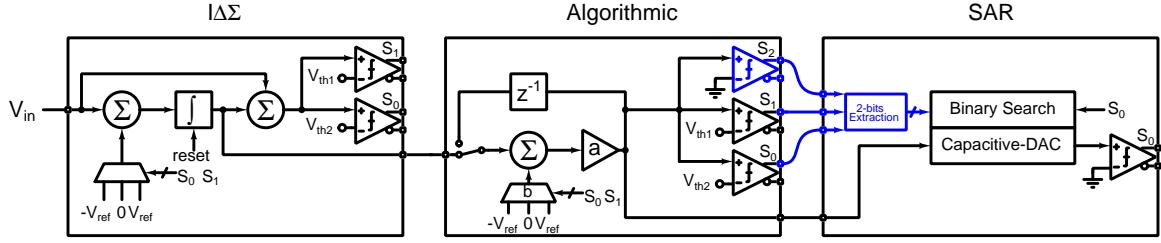


Figure 3.4 Final proposition of the ADC architecture

3.2 Sub-ADC Analysis

3.2.1 Incremental- $\Delta\Sigma$

principle and the basic choice: The first stage is a fully-differential Incremental- $\Delta\Sigma$ modulator based on the principle given in section 2.1.2.2. Compared to a conventional $\Delta\Sigma$ modulator, the integrator is reset at each new sample to mimic a nyquist rate ADC. Therefore, the design of an $I\Delta\Sigma$ requires OSR+1 clock cycles to achieve an oversampling ratio of OSR. The version presented in the State of the Art was a multi-bit quantizer to be generic. However, the 1-bit quantizer is the simplest and is inherently linear. In consequence, a first-order Incremental- $\Delta\Sigma$ with 1-bit quantizer is the most robust solution.

limitations: Kept as a basis for the first stage of our ADC, the 1-bit quantizer in this topology does not limit the excursion of the integrator output. Without this limitation of the output swing, a large constraint is placed on the amplifier inside the integrator, and results in an integrator output deformed and outside of the allowed input swing of the following stage. In order to suppress this eventuality, two key actions have been implemented.

solutions: First, two comparators instead of one detects when the output of integrator, also called the residue, is outside the desired excursion range. Second, the input voltage is summed with the integrator output before the comparison to the excursion range limits. The input has a feed-forward path not to saturate the integrator by summing the residue with the input signal.

solution 1 (3-levels quantizer): Let us assume the output of comparators is either zero or one, and we call the quantification error $e(z)$, the error between the input voltage of the quantizer $x(z)$, and the estimation coming from the comparators' outputs. The estimation performed by the 3-levels quantizer is thus $(S_1(z) + S_0(z) - 1)V_{ref}$, if we consider $S_1(z)$ and $S_0(z)$ the comparators' outputs in the z-domain. The value of the estimation is one among those in the following set $\{-1, 0, 1\}$. The quantification error is thus given to be

$$e(z) = x(z) - (S_1(z) + S_0(z) - 1)V_{ref} \quad (3.1)$$

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To estimate the repercussion on the output of the integrator called Residue, we describe the modulator using the z-transform in the equation (3.2).

$$\frac{V_{in}(z)z^{-1} - (S_1(z) + S_0(z) - 1)V_{ref}z^{-1}}{1 - z^{-1}} + V_{in}(z) + e(z) = (S_1(z) + S_0(z) - 1)V_{ref} \quad (3.2)$$

$$e(z) = \frac{(V_{ref}(S_1(z) + S_0(z) - 1) - V_{in}(z))}{1 - z^{-1}} \quad (3.3)$$

Based on the latter, the output of the integrator is thus defined by

$$\text{Residue}(z) = -\frac{e(z)z^{-1}}{1 + z^{-1}} \quad (3.4)$$

To minimize the Residue, $e(z)$ shall be minimized too.

error minimization: From the definition of quantification error, at the n^{th} -clock cycle, $e[n]$ can be expressed as a function of the threshold voltages and the input swing of the quantizer delimited in the range $[x_{\min}, x_{\max}]$. This is given in equation (3.5).

$$e[n](x) = \begin{cases} \frac{2}{x_{\max}-x_{\min}}(x - x_{\max}), & \text{if } x > V_{\text{th}2} \\ \frac{2}{x_{\max}-x_{\min}}x, & \text{if } x \in [V_{\text{th}1}, V_{\text{th}2}] \\ \frac{2}{x_{\max}-x_{\min}}(x - x_{\min}), & \text{otherwise} \end{cases} \quad (3.5)$$

Graphically, the error function is depicted in Figure 3.5 with the extrema values.

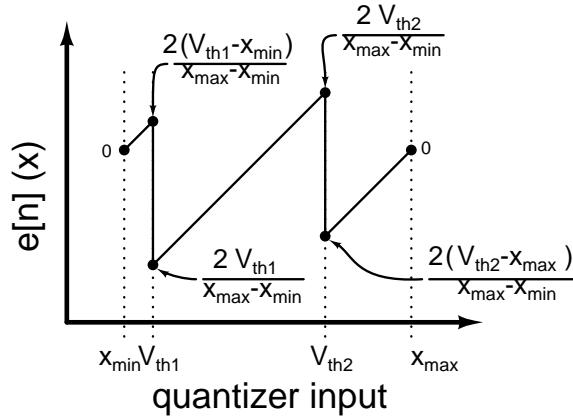


Figure 3.5 3-levels error pattern

error minimization (threshold voltages tuning): As the structure is fully differential a constraint of symmetry on the threshold voltage is equivalent to impose the same output swing for both the positive and negative signal of the integrator around the common-mode voltage. This assumption being reasonable, the error $e[n](x)$ is minimal when $V_{\text{th}2} = -V_{\text{th}1} = \frac{x_{\max}-x_{\min}}{2}$.

solution 2 (input feed-forward): The second solution to control the excursion of the integrator output consists in the addition of a feed-forward input path. For the sake of clarity the modulator is represented as a single-ended topology in Figure 3.6. This figure represents the normal behaviour of the modulator. Being incremental, the integrator is reset at the beginning of each new sample: during the first clock cycle. Without the feed-forward path, the decision of the 3-levels quantizer in this clock cycle is irrelevant. And the integrator will increment by the value of the input at the second clock cycle. With this input path, the input voltage is estimated from the first clock cycle. And a feedback is applied then. The integrator does not have the possibility to exceed the limit fixed as the increment is the error between the input and its pre-estimation.

Besides that, the input feed-forward is beneficial for the modulator in the configuration depicted in Figure 3.6b. Without the input feed-forward, the integrator has to process the quantization noise in addition to the input signal for the regulation of the output. On the other hand, the integrator has to process only the quantization noise. And the removal of the input signal component reduces the swing at the internal nodes of the modulator which relaxes the headroom requirements, and allows for more efficient amplifier architectures to be used. However, the input-feed-forward path presents complications, a timing constraint overhead and the analog adder at the quantizer input.

This given, the adder can be implemented as an active analog bloc or as a passive one. For power saving reason, a bunch of capacitors forms the passive adder.

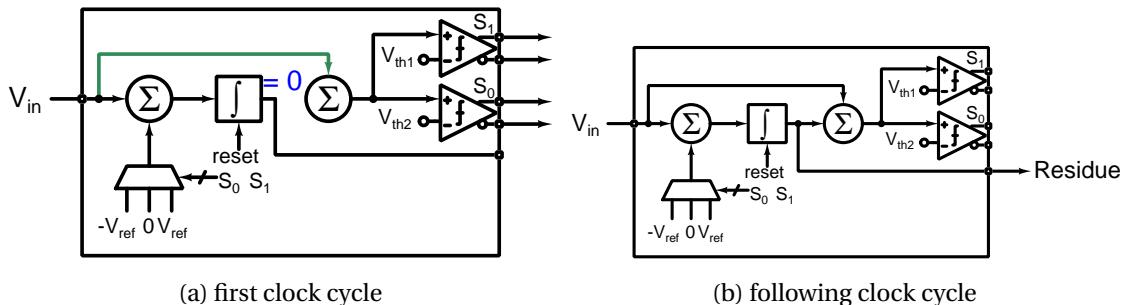


Figure 3.6 3-level $\Delta\Sigma$ modulator architecture in the ADC and the initialization of a new sample while delivering the residue to the next stage

resolution and strategy: Due to the minimization of the quantification error by selecting the threshold voltages of the quantizer, the residue is limited to $\pm V_{\text{ref}}/2$. The resolution of the ADC can be enhanced by an inter-stage gain of two between this stage, and the one following. This transfer analog constraint on the offset to the second stage with a possible input overflow. With an ability to withstand greater offsets, errors from non-perfectly set threshold voltages, and prevents extra noise source decreasing the SNR of internal nodes, no inter-stage gain is introduced within this stage. With 8-levels in the transfer function of this stage, the maximum resolution is 3-bits.

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3.2.1.1 Integrator

principle: The switched capacitor integrator is continuous-time integrator whose resistor is emulated by a switching capacitor. Here in the Figure 3.7, C_S first samples the input voltage during Φ_1 and then delivers its charge to C_I through the virtual ground of the amplifier during Φ_2 . Not being reset, at each clock cycle, C_I integrate charges sampled. At the output, the voltage change after each clock period is equal to $-(C_S/C_I)(V_{in} - V_{FB})$.

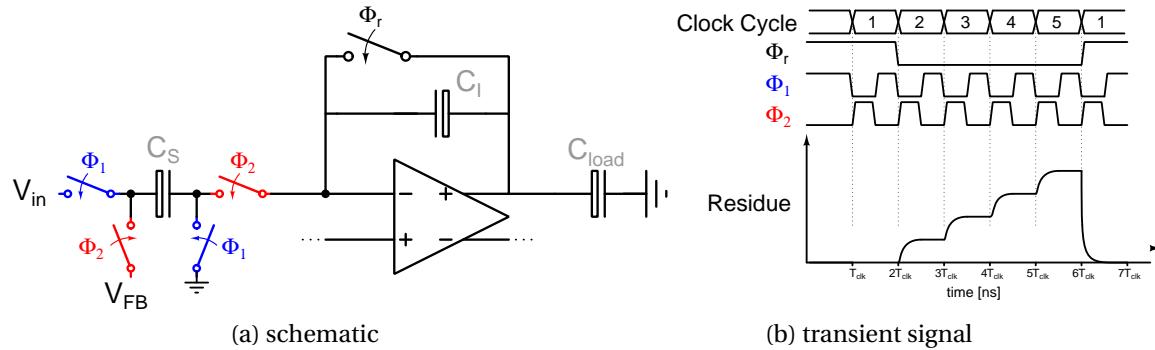


Figure 3.7 Principle of switched capacitor integrator

parasitic insensitive: Suppose C_S has a parasitic capacitance from each plate to ground. While the left plate charges to V_{in} then V_{FB} , the parasitic capacitor of this plate has no contribution in the charge transfer during Φ_2 . Unfortunately, the right plate parasitic will be charged a little due to the finite gain of the amplifier and appears in the charge transfer as a small voltage drop. This point also applies to the nonlinearities arising from these parasitics.

In addition to this, the implementation using parasitic insensitive switched capacitor integrator requires the use of non-overlapping phases. This is necessary for avoiding the simultaneous activation of switches connecting to the V_{cm} or V_{refp}/V_{refm} , which would corrupt the value stored on C_S , and switches connecting the input voltage and the virtual ground, which would allow V_{in} to momentarily charge C_I through C_S , reducing the integrator gain.

integrator existing modes: In a conventional mode, the first clock cycle is lost for the reset of the integrator. In the case of a reset done at the first clock cycle of a new conversion, the output bits of the last clock cycle are not related to the residue transfer at this clock cycle. With two bits at each clock cycle, only 8-bits are necessary out of the ten provided. With a low-OSR conversion, each clock cycle is important. One can enhance by adding a switch in the charge transfer path as depicted in Figure 3.8. This switch opens the signal path to shunt the amplifier at each clock cycle without resetting the charge stored in C_I . As a result, the residue is falling down to zero at each clock cycle. The amplifier has thus an increased speed and slew-rate constraint. For the implementation, Φ_{1mode} is a signal always on to operate in a conventional mode.

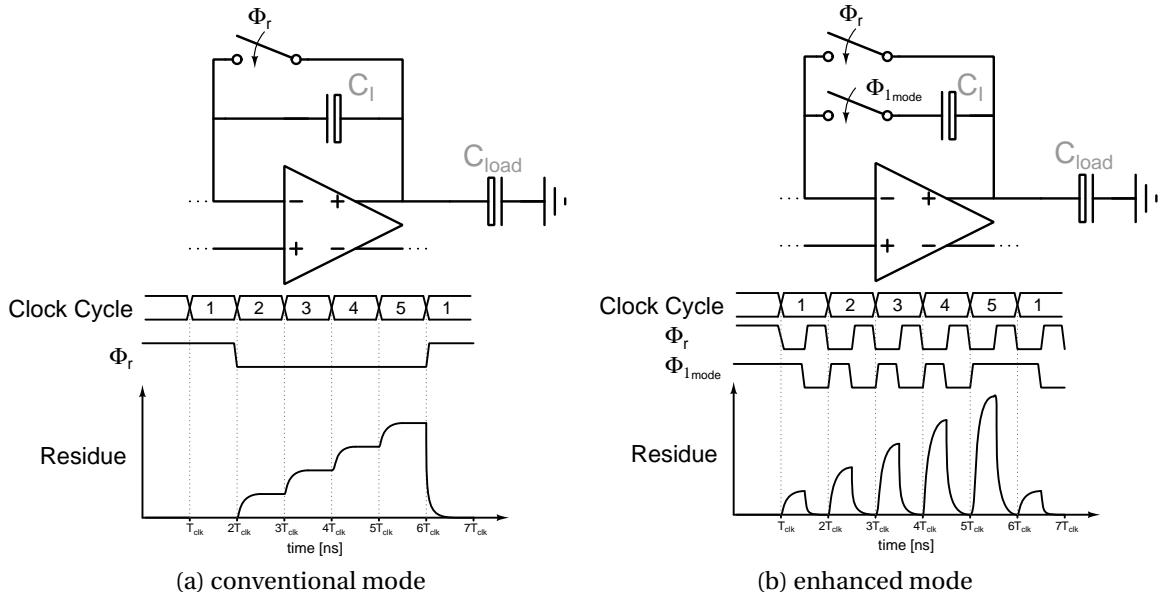


Figure 3.8 Integration without clock cycle loss to enhance performance by amplifier shunt

The final representation of the integrator is represented by the Figure 3.9 where Φ_1 and Φ_2 are non-overlapping phase while Φ_{1d} and Φ_{2d} are respectively their delayed version. Φ_{2d} does not overlap with Φ_1 too.

Reduction of the INL without calibration by the ratio C_S/C_I : In such circumstances the SC-Integrator respects the equation (3.6) where A is the OTA DC Gain, C_S the sampling capacitor, C_I the integration capacitor, and V_{in} , V_{ref} , V_{out} respectively the differential voltage $V_{inp} - V_{inm}$, $V_{refp} - V_{refm}$, and $V_{outp} - V_{outm}$.

$$V_{\text{out}}[n] = V_{\text{out}}[n-1] \left(\frac{1 + \frac{1}{A}}{1 + \frac{1+C_S/C_I}{A}} \right) + (V_{\text{in}} - b[n-1]V_{\text{ref}}) \frac{C_S}{C_I} \left(\frac{1}{1 + \frac{1+C_S/C_I}{A}} \right) \quad (3.6)$$

As demonstrated in Appendix C, the INL is tightly linked with the settling error of the integrator after n-steps. Even if this highly depends on the OTA DC Gain, the ratio C_S/C_I deeply impacts it. The settling error is smaller for small C_S/C_I and the output swing of the integrator is limited by the threshold voltages of the 3-levels quantizer. However, for a ratio $C_S/C_I < 1$, the intrinsic noise of the OTA has more weight. Accordingly a ratio of 1 is preferred leading to a feedback factor $\beta = C_I/(C_S + C_I) = 1/2$ for the design of the OTA.

switches noise: Considering error sources, switches on the signal path are of much importance as they source the signal and induce noise by their finite channel resistance. Therefore, the voltage standard deviation of the thermal noise injected by a switch on a capacitance is given to be $\sqrt{k_B T/C}$ where k_B is the Boltzmann constant, T the temperature, and C the load capacitance of

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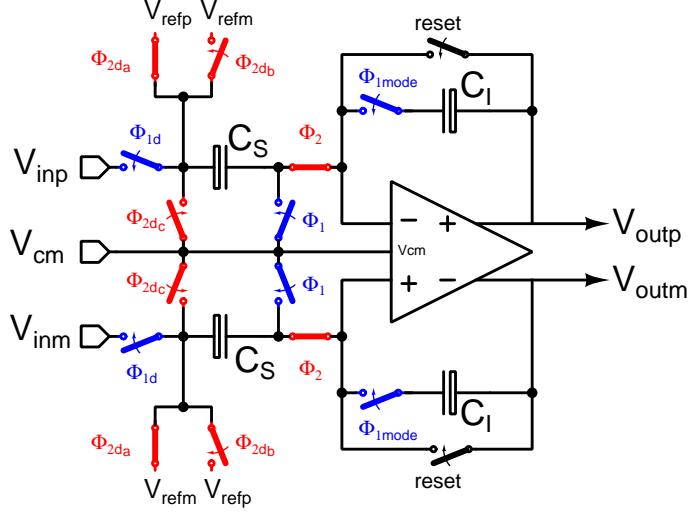


Figure 3.9 Switched-capacitor integrator implementation

a switch. On the sampling capacitor, the number of switches connected is $N_{\text{switches}} = 6$. To bind the noise variation within an LSB of a given resolution, the following criterion shall be respected: $\sqrt{N_{\text{switches}} k_B T / C} < \frac{V_{\text{inmax}} - V_{\text{inmin}}}{2^{\text{resolution}}}$. So, the minimum capacitance to for a desired resolution is $C_{\min} > N_{\text{switches}} k_B T \left(\frac{2^{\text{resolution}}}{V_{\text{inmax}} - V_{\text{inmin}}} \right)^2$. As the $\Delta\Sigma$ is oversampling at least over 5 clock cycles, the noise power is divided by OSR. For a maximum temperature of 175°C, the sampling capacitor should at least be to 110 fF in order to bind the thermal noise within a 11.7-bits LSB.

channel resistance and settling time: The second source of error concerning them is the settling error. This error comes from a first order system settling error whose time constant is defined by the product of the finite channel resistance and the sampling capacitance as $\tau = R_{\text{switches}} C_S$. In this regard, two switches in series samples the input voltage with a settling time of 9 ns and an accuracy of 14-bits. The maximum switch resistance follows as

$$2R_{\text{switches}} = -\frac{T_{\max}}{C_S \times \ln(V_{\text{error}})} = -\frac{9\text{ns}}{110\text{fF} \times \ln(1/2^{14})} \approx 8400\Omega \quad (3.7)$$

This does not consider the voltage dependence of τ coming from the non-linear junction capacitance of switches parasitics and the bulk effect of transistors as depicted by the Figure 3.10. In either case, the designed switches on resistance is far below the limit to not be the bottleneck in the settling speed.

charge injection: By the way, charge injection in analog switches and multiplexers is a level change caused by stray capacitance associated with the NMOS and PMOS transistors that make up the analog switch. In a fully differential architecture this phenomenon is fairly reduced, but not annihilated. Indeed, the voltage commuted in the positive side is the opposite of the one in the

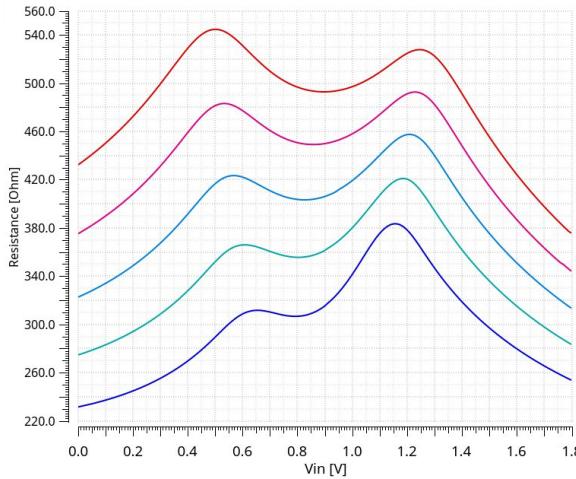


Figure 3.10 CMOS switches for a ratio PMOS/NMOS of 3.5 at 5 different temperatures from -40°C to 175°C as a function of the input voltage

negative side: at least a voltage dependant error is introduced. In the case of switches connecting the input voltages, the error on the transfer function of the ADC is dependant of the input voltage.

As signal switches shall be complementary ones with at least PMOS 3.5 times larger than NMOS to reduce non-linearity dependant on the input voltage. The charge injected by PMOS stray capacitance are thus not fully absorbed by the NMOS stray capacitance as depicted by Figure 3.11a. As we assume that the input voltage of the switch is approximately equal to the one sampled on the capacitor C_S , the charge deposited by the NMOS transistor is $\Delta q = W_n L_n C_{ox} (V_{DD} - V_{in} - V_{thn})$ while the charge from the PMOS transistor is $\Delta q = W_p L_p C_{ox} (V_{in} - V_{thp})$. Hence, size of switches shall be minimal to reduce the charge injection while the increased channel resistance induce distortions.

Finally, the bottom switch connecting the bottom plate of the capacitor to the common mode voltage should turn on/off before the signal switches connect to top plate capacitance. Indeed, in the case of a bottom sampling, switches on the bottom plate inject charge while opening. Injected charge is constant since its gate-source voltage is constant and eliminated when used differentially. Then the bottom plate of C_S is already floating when its top-plate switch is opened, no signal dependant charge is injected on C_S .

clock feedthrough: In addition to the charge injection coming from these signal switches, the clock feed-through is an error that is constant with the input voltage level $\Delta V = V_{gate} \frac{W C_{ov}}{W C_{ov} + C_S}$. For high-speed input signals, it is critical that the NMOS and PMOS switches in Figure 3.11b turn off simultaneously. If, for example, the NMOS device turns off Δt seconds earlier than the PMOS device, then the output voltage tends to track the input for the remaining Δt seconds, but with a large, input-dependent time constant. This effect gives rise to distortion in the sampled value.

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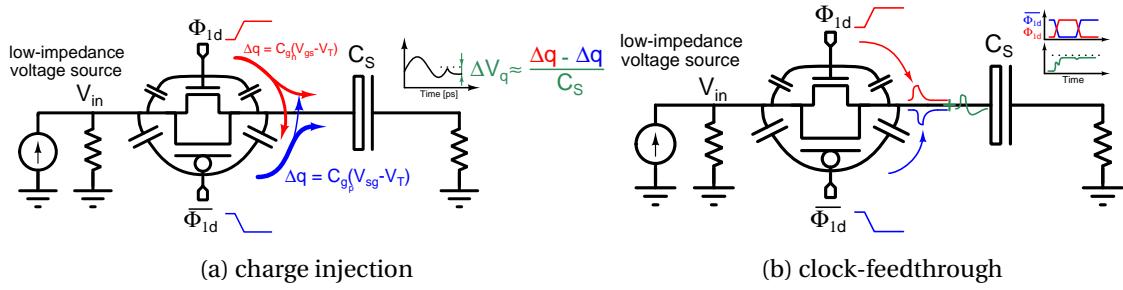


Figure 3.11 Phenomenon of charge injection and clock-feed-through on the sampling switches

To reduce the amount of charges, the switches size is determined by $L = L_{\min}$ to minimize the area, and an optimization of their width to reduce the input voltage dependency of this sub-ADC residue in the range from $1\mu\text{m}$ to $4\mu\text{m}$. A good balance is found for $W/L = 2 \mu\text{m}/180 \text{ nm}$ with a ratio PMOS over NMOS of 3.5.

3.2.1.2 1.5-bit Quantizer

This given, The passive adder circuit is represented in Figure 3.12. The first clock phase is used to reset the passive adder while the subtractor-integrator is sampling. The second clock phase activates the summation by charging capacitors.

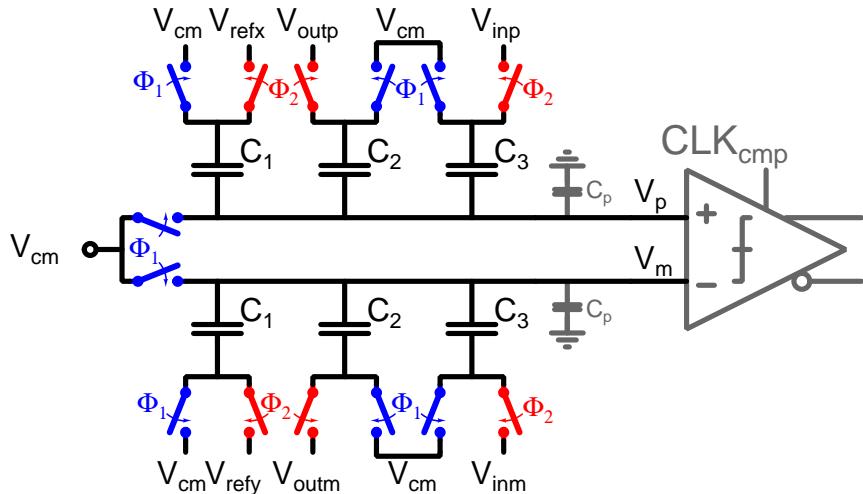


Figure 3.12 Switched capacitor passive adder and comparison to a threshold voltage

The choice of appropriate capacitor ratio results from following equations of the differential voltage seen at the input of comparators.

$$V_p = \frac{C_1 V_{\text{refx}} + C_2 V_{\text{outp}} + C_3 V_{\text{inp}} + 0 \times C_p}{C_1 + C_2 + C_3 + C_p} \quad (3.8)$$

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$$V_m = \frac{C_1 V_{\text{refy}} + C_2 V_{\text{outm}} + C_3 V_{\text{inm}} + 0 \times C_p}{C_1 + C_2 + C_3 + C_p} \quad (3.9)$$

The differential voltage seen by the comparator is proportional to the first differential input plus a weighted second differential voltage. We can notice that when comparing the input voltage to a weighted reference voltage, the gain is not a concern since only the sign of the differential voltage is important. And determining the sign is equivalent to get the result of the following inequalities (3.10).

$$V_p > V_m \equiv C_1 V_{\text{refx}} + C_2 V_{\text{outp}} + C_3 V_{\text{inp}} + 0 \times C_p > C_1 V_{\text{refy}} + C_2 V_{\text{outm}} + C_3 V_{\text{inm}} + 0 \times C_p \quad (3.10)$$

$$\equiv C_2 V_{\text{outd}} + C_3 V_{\text{ind}} > C_1 (V_{\text{refy}} - V_{\text{refx}}) \quad (3.11)$$

where V_{outd} is the differential output of the integrator, V_{ind} the differential input sampled, and V_{refy} and V_{refx} are alternatively V_{refp} or V_{refm} . This solution shows an ability of lessening sensitivity to parasitic. So, a comparison to half the reference voltage is performed for the capacitances $C_2 = C_3$ are twice C_1 . The ratio between the input voltage and the remainder is set to unity to not saturate the integrator.

Due to process mismatch, a difference within the negative side and positive side capacitance induce an offset in the comparison. Indeed, let us suppose that for each positive side capacitance a mismatch is added ΔC_i for each capacitance C_i while on the negative side there is $-\Delta C_i$ for each capacitance C_i .

The inequality (3.10) mutates into (3.12).

$$\frac{C_1 V_1 + C_2 V_2 + C_3 V_3 + \sum_{i=1}^3 \Delta C_i V_i}{C_1 + C_2 + C_3 + C_p + \sum_{i=1}^3 \Delta C_i} - \frac{C_1 V_4 + C_2 V_5 + C_3 V_6 + \sum_{i=1}^3 \Delta C_i V_{i+3}}{C_1 + C_2 + C_3 + C_p - \sum_{i=1}^3 \Delta C_i} > 0 \quad (3.12)$$

By changing for a common denominator and by setting $X = C_1 + C_2 + C_3 + C_p$, this is equivalent to compare

$$\left(C_1 V_1 + C_2 V_2 + C_3 V_3 + \sum_{i=1}^3 \Delta C_i V_i \right) \left(X - \sum_{i=1}^3 \Delta C_i V_i \right) > \left(C_1 V_4 + C_2 V_5 + C_3 V_6 - \sum_{i=1}^3 \Delta C_i V_{i+3} \right) \left(X + \sum_{i=1}^3 \Delta C_i V_i \right) \quad (3.13)$$

$$C_1 (V_1 - V_4) + C_2 (V_2 - V_5) + C_3 (V_3 - V_6) > \left(\sum_{i=1}^6 C_i V_i \right) \frac{\sum_{i=1}^3 \Delta C_i}{X} - \left(\sum_{i=1}^3 C_i V_i \right) \frac{X - \sum_{i=1}^3 \Delta C_i}{X} \quad (3.14)$$

$$- \left(\sum_{i=1}^3 C_i V_{i+3} \right) \frac{X + \sum_{i=1}^3 \Delta C_i}{X}$$

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$$C_1(V_1 - V_4) + C_2(V_2 - V_5) + C_3(V_3 - V_6) > \frac{\sum_{i=1}^3 \Delta C_i}{C_1 + C_2 + C_3 + C_p} \left(\sum_{i=1}^3 \Delta C_i (V_i - V_{i+3}) \right) \quad (3.15)$$

$$- \left(\frac{\sum_{i=1}^3 \Delta C_i}{C_1 + C_2 + C_3 + C_p} - 1 \right) \left(\sum_{i=1}^3 \Delta C_i (V_i + V_{i+3}) \right)$$

$$C_1(V_1 - V_4) + C_2(V_2 - V_5) + C_3(V_3 - V_6) > \frac{\sum_{i=1}^3 \Delta C_i}{C_1 + C_2 + C_3 + C_p} \left(\sum_{i=1}^3 \Delta C_i V_{d_i} \right) \quad (3.16)$$

$$- 2 \left(1 - \frac{\sum_{i=1}^3 \Delta C_i}{C_1 + C_2 + C_3 + C_p} \right) \left(\sum_{i=1}^3 \Delta C_i V_{cm_i} \right)$$

The latter precise the nature of the offset for arbitrary differential voltage on capacitor of such structure: a term which depends on the common mode voltage, and one dependant on the differential voltage applied. Therefore, the comparison offset is voltage dependant. As differential voltages are limited by $V_{ref} = 1$, the common mode is assumed to be $V_{DD}/2$, and capacitance C_i a multiple integer of unit capacitance C_0 as $k_i C_0$, the maximum offset is given by

$$V_{DD} \left(\frac{C_0 \Delta C_0 \sum_{i=1}^3 \sqrt{k_i}}{C_0 (\sum_{i=1}^3 k_i)} \right) + (1 - V_{DD}) \left(\frac{(C_0 \Delta C_0)^2 (\sum_{i=1}^3 \sqrt{k_i})^2}{(C_p + C_0 (\sum_{i=1}^3 k_i)) (C_0 (\sum_{i=1}^3 k_i))} \right) \quad (3.17)$$

Henceforth, from the allowed tolerance on the mismatch from the ideal values, the area of the unit capacitance can be found according to the Pelgrom modelling of capacitance variation in the design kit: $\Delta C_0 \propto A_{c_{MIM}} / \sqrt{WL}$ with $C_0 \propto WL \times C_{MIM} (fF/\mu m^2)$. We consider a large tolerance of 1% mismatch on the unit capacitance for an offset generated to be under 20 mV. For an OSR=6, the reconstruct transfer function is a staircase with 200 mV steps. This value of the offset is a less than a tenth of this sub-ADC transfer function step. In consequence, the unit capacitance is chosen to be 50 fF with a size of $3.2 \mu m \times 3.2 \mu m$.

One should consider the influence of a fast latching output of the comparator. By capacitive coupling to its inputs, a fast transient variation of the outputs “kicks back” the signal V_p/V_m used for the comparison. In this case, only the differential kickback is of interest. As the kickback propagates to the residue via C_2 and introduces an extra error on the final value, this could be reduced by cutting the path for the kickback before the comparator makes a decision.

From this structure, $V_{refy} = V_{refp}$ and $V_{refx} = V_{refm}$ in order to compare $V_{outd} + V_{ind} > -V_{ref}/2$ while a replicate structure is connected as $V_{refy} = V_{refm}$ and $V_{refx} = V_{refp}$ to compare $V_{outd} + V_{ind} > V_{ref}/2$. The combination of the two is the 3-levels quantizer needed to bind the residue.

3.2.1.3 Digital Circuit

3.2.1.3.1 Clock Phase Generator For the ease of design as well as being silicon proven in very high speed two clock phases generation, the clock generator is presented in Figure 3.13. The

cross-coupled NOR gates version is preferred over the cross-coupled version since Φ_2 cannot rise until Φ_{1d} has fallen below the switching point for the NOR gate. Such that even for very fast buffers at very low-temperature in the fastest corner we are confident the non-overlapping time exists.

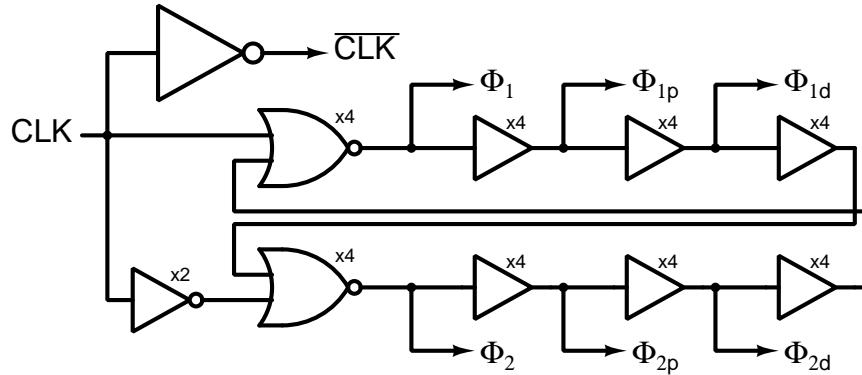


Figure 3.13 Two-phase non overlapping generator circuit

In such topology, buffers define the driving capability of phase generator. In many applications in order to maximize the available settling time for the circuit, the phase's widths are widened by minimizing non-overlapping duration. Hence, the number of logic gates used in the clock generator is normally minimized, also reducing the accumulated jitter.

For the bottom sampling, both Φ_1 and Φ_{1d} drive sampling switches. In this regard, the delay between those two shall be minimal to allow the maximum sampling time with a delay bigger than the commutation time of the bottom switch. By using buffers for medium strength (x4), the delay introduced admits a maximum of 400 ps and a minimum of 200 ps.

3.2.1.3.2 Switches command signal driver As discussed earlier, the simultaneity of turning off switches prevents ambiguity in the sampled value when the settling time is limited and the non-overlapping time is short. In order to make transition crossing the most possible around half the power supply for complementary switches, the driver of the Figure 3.14a is ideally used. As the inverter and the transmission gate exhibit both a small propagation delay, they almost compensate for each other. In fact, process variation generates different trip point for inverters while the equivalent resistance of transmission barely changes in comparison. The mismatch between the RC settling of the transmission gate and the pseudo-RC settling of inverters becomes ever more prominent.

For a minimal size inverter, good results are given without the transmission gate as depicted by Figure 3.14b. In a typical corner over temperature, the variation of the crossing point is 300 ps for a capacitive load that analog switches represent. Crossings between the PMOS and the NMOS command signals are in the 600-725 mV range over the temperature range. Taking into account the process variation, this range enlarges to 490-850 mV. With the transmission gate, the delay

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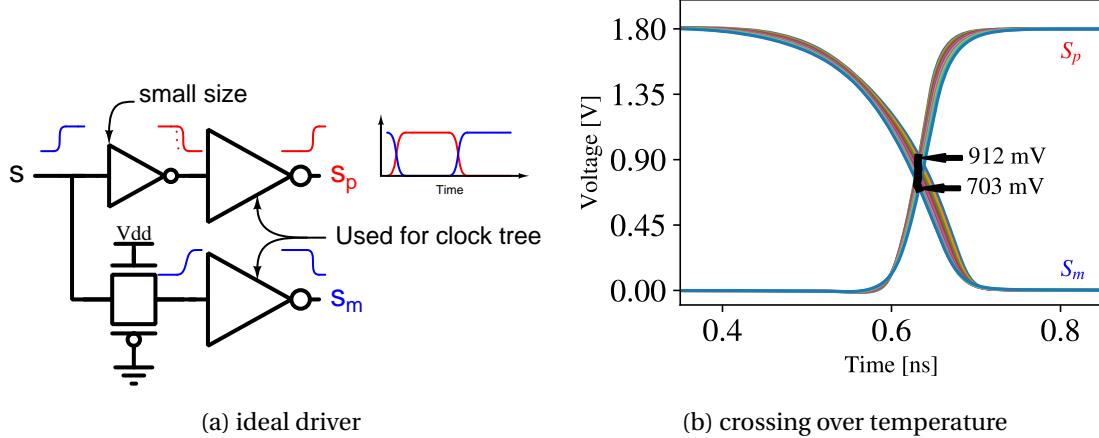


Figure 3.14 Digital driver to ensure PMOS and NMOS command signal S_p/S_m transition crossing around half the power supply voltage

for low-to high variation is compensated. Taking into account the process variation, this range enlarges to 700-1150 mV. In comparison, the range suffers from a greater process variation given by the transmission gate equivalent resistance while the range is centred around half the power supply voltage. Furthermore crossings occurs at almost the same time over temperature. For this last reason, the version using transmission gate is preferred.

3.2.1.3.3 Relaxed comparator constraints Analog constraints undergo large variation with process alteration and increasing temperature. In this regard, the digital should respect these constraints, but can also relieve them. As an example, the transition frequency of a single transistor as a sensitivity of about 2000 ppm/ $^{\circ}\text{C}$. This is equivalent to say from -40°C to 175°C that the speed is reduced by 35 %. For the sake of simplicity, let us assume comparators follows the same trend over temperature. As the differential input is getting closer to zero, the delay increase. While in most of the case the decision is made within the non-overlapping time, this is not the case with this design. This is done in order to reduce the probability of a metastable state, or more generally to prevent latch output transition at the time the digital is applying the feedback voltage.

Figure 3.15 depicts the scheduling of the comparator decision in order to apply the correct voltage feedback. As the second clock phase settles the input voltage of the quantizer, the comparator makes a decision in less than 1 ns after. The decision made toggles the nand-RS-latch to generate the appropriate feedback selector signal. In the case of the critical path, a single gate generates the signal. The following AND gate makes the results only available for the next second phase of the clock. Therefore, between the beginning of the settling of input voltages to compare and the available result signal, there is $T_{clk}/2 - T_{delay} - T_{RSLatch} - T_{nor} - T_{setup}$ for the comparator.

In summary, the first stage Incremental- $\Delta\Sigma$ heavily relies on the performance of the integrator. The design from the top-level down to switches' transistors have been considered to reduce the

3.2 Sub-ADC Analysis

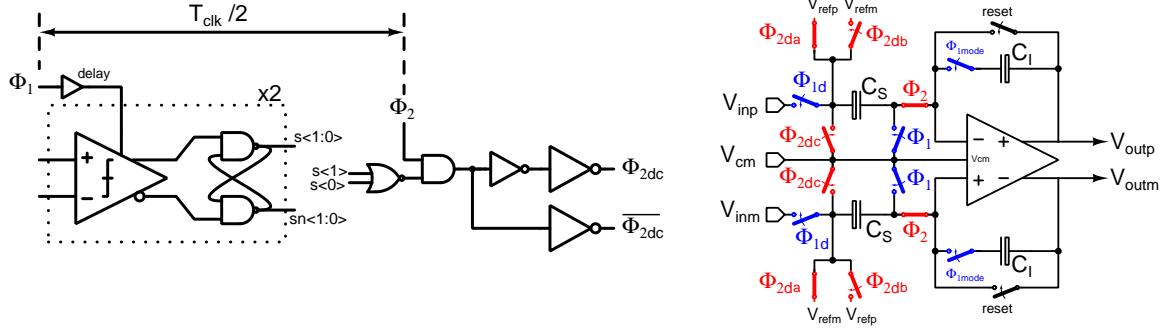


Figure 3.15 Comparator relaxed constraints by appropriate scheduling

INL drop due to parasitics, coupling, charge trapped and mismatches. From a system point of view, the fully differential structure limits the impact of clock coupling, charge injections and mismatches. With a parasitic insensitive topology, the parasitic can be disregarded for the design as the switches command signals are non-overlapping and limits charge injections. However, only partial specification have been given for the OTA not discussed yet. Connected to the integrator, the 3-levels switched capacitor quantizer limits the swing of the residue by making the decision of the feedback to apply. Being the interface between comparators and the integrator, the offset introduced by mismatch in capacitors sums with the offset of comparators. The excursion of the residue takes into account the disturbance to be processed by the following stage: the Algorithmic.

3.2.2 Algorithmic

principle: The principle of the Algorithmic conversion lies in the successive amplification of the estimation error. Made out of an ADC-DAC chain to estimate the input voltage, the error is then amplified by an arbitrary factor a before the recycle of this error as the new input of this converter.

For its first clock cycle, this stage samples the residue of the previous stage. Herein the previous stage residue is named V_{in} for clarity as represented in Figure 3.16. After the comparator makes a decision, either $+bV_{ref}$, or 0, or $-bV_{ref}$ is added to the amplified input signal. The output of the adder is the part of the input that has not yet been quantized and is called the residue. Here a denotes the gain applied to the residue between comparator decisions and is called the residue gain. In later cycles, the input switch is always in the up position, and the residue is sent back to the comparator for further quantization as in Figure 3.16b.

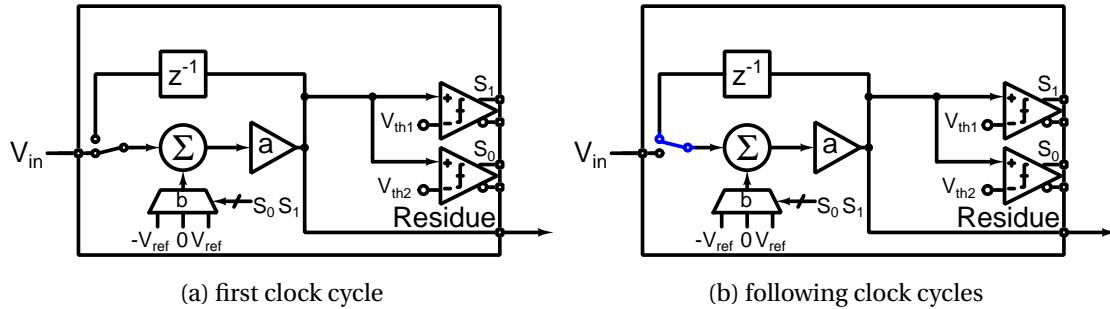


Figure 3.16 3-level algorithmic stage operation

limitations from analog error amplified and on residue: A common implementation of the algorithmic converter is by building the stage around a Flip-Around Multiplying DAC (FA-MDAC) composed of two capacitors and one amplifier. While a simple differential pair is a valid amplifier to operate under low-supply condition, as the resolution increases the gain of the amplifier should drastically increase too. Indeed, at each clock cycle the FA-MDAC recycles its inner self error. To achieve high gain amplifier by stacking transistors the output swing is thus limited and non-linearity occurs. Therefore, medium to high resolution algorithmic ADC require a digital compensation or an adjustment of its residue curve.

resolution enhancement with interstage gain: Besides this, the residue of the first stage is within the $\pm V_{ref}/2$ range. With a SAR following this stage, an increase of this stage residue can be converted. In consequence, the resolution of the ADC can be enhanced by the introduction of an interstage gain to amplify the residue of the first stage. The benefits and limitations of an interstage gain will be discussed later in this section.

resolution enhancement and threshold change: In addition to that, the architecture proposal discussed in section 3.1.3 consists in turning the estimation of the error provided by the last clock cycle into the first bits of the SAR. Depending on the adjustment of the residue curve, threshold

voltages of the quantizer change in the last cycle to $\pm V_{\text{ref}}/2$. Depicted by Figure 3.17, during this last clock cycle, a third comparator is used to give the sign of the residue. The output of the comparison results in the expected first step perform by a SAR. The threshold change to match the threshold of the second step of the SAR, such that the outputs of the three comparators provide the quadrant of the residue. This digital information will be used by the third stage of the converter right after the sampling phase to perform its third comparison.

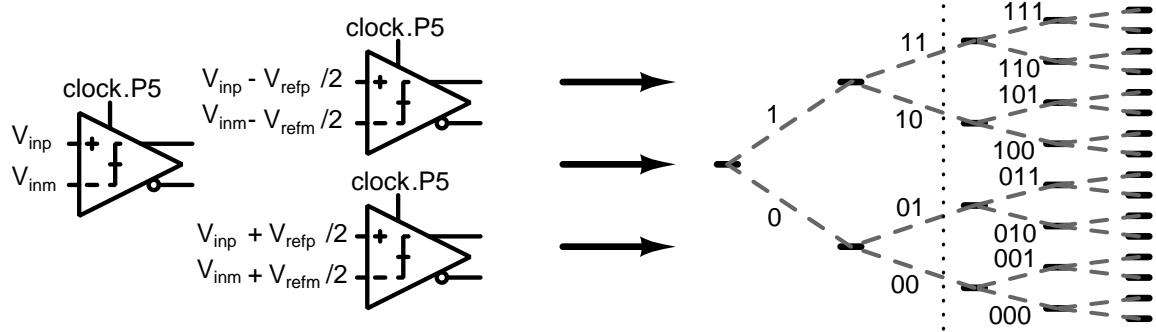


Figure 3.17 Principle to enhance the number of extracted bits by using an extra comparator inside the algorithmic stage to perform the two first steps of a charge-redistribution SAR

solutions (residue constrained with a 1.5-bit quantizer): Expecting a digital calibration of mismatch compensation, the adjustment of the residue curve provides the necessary margin to achieve medium to high resolution with an algorithmic ADC. With a transfer function of the form $V_{\text{residue}}[n+1] = aV_{\text{residue}}[n] \pm bV_{\text{ref}}$, the two parameters a and b can be tuned.

If the residue gain $a = 2$, N-bit conversion requires N clock cycles and the output code is simply raw output bits of the comparator shifted and added. Reducing the residue gain increases the number of required clock cycles, but also introduces redundancy, allowing ADC non-linearity from the SHA charge injection, comparator offset, and OTA offset to be avoided [111]. However, the ADC output cannot be calculated by a simple bit shift and addition. So, we decide to keep the residue gain $a = 2$.

Thus, redundancy is introduced via a 1.5-bit quantizer to relax the requirements on the offset of the comparator and the amplifier. As performed in the design of the first stage, we thus constrain the residue within the desired range by tuning the parameter b .

Classical algorithmic converters use threshold voltages equal to $\pm V_{\text{ref}}/4$ and a feedback gain $b = 1$ such that the residue is depicted in Figure 3.18b [40, 52]. In this case, the sub-ADC is resilient to large comparator and amplifier offset by demonstrating a large margin between the $\pm V_{\text{ref}}$ limits and the maximum of the residue curve. Unfortunately, such error on the first stage increases the input voltage range, which results in a range overflow. Let us suppose that we do not want to exceed $\pm V_{\text{ref}}/2$. For the case represented in Figure 3.18b, an offset on the comparator of the first stage will increase the input voltage to $\pm V_{\text{ref}}/2 + V_{\text{offset}}$. The error committed on the residue range

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is twice V_{offset} . With an interstage gain envisioned, the effect could be catastrophic: the residue could exceed $\pm V_{\text{ref}}$ range leading to missing codes.

By using the general shape of the residue represented in Figure 3.18a, the residue is limited by an appropriate choice of threshold voltages and the feedback gain b . Let us suppose the desired residue is symmetrical around 0 and based on the system study we required a tolerance of l/a for charge injection, comparator offset, OTA offset. Hence, the extrema of the residue curve is $l = aV_{\text{th}2} = aV_{\text{th}1} + bV_{\text{ref}} = -aV_{\text{th}1} = -aV_{\text{th}2} + bV_{\text{ref}}$. From these equations, the threshold voltages are given as

$$V_{\text{th}2} = l/a = -V_{\text{th}1} \quad (3.18)$$

while the feedback gain b is given by

$$b = \frac{2l}{V_{\text{ref}}} \quad (3.19)$$

From a robustness point of view, such design handles input range overflow since the input values which makes the residue crossing $\pm V_{\text{ref}}$ are $\pm \frac{1+b}{a} V_{\text{ref}}$. For the conventional design $a = 2, b = 1, V_{\text{th}} = \pm V_{\text{ref}}/4$, the maximum input range is $\pm V_{\text{ref}}$. For a tolerance of 10% of V_{ref} for offset and charge injection, or $l = 0.8 V_{\text{ref}}$, the input range extends to $\pm 1.3 V_{\text{ref}}$. From the design of the first stage and considering a precise inter-stage gain of 2, the tolerance for the offset on the first stage is 15% of V_{ref} .

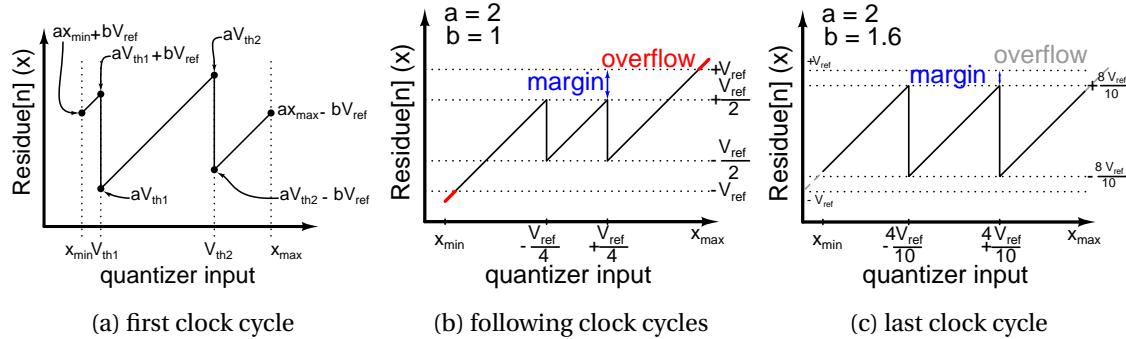


Figure 3.18 3-levels algorithmic stage operation as an optimization for robustness

This slightly novel approach allows to find the best compromise between performance and sensitivity to offset by changing the feedback gain. The threshold voltages required by a 1.5-bit quantizer vary accordingly as a quarter of the feedback gain. With a feedback gain equal to 1, we found back the conventional design. Of course, the residue range changing with b , the possible interstage gain depends on the feedback gain. To keep performance high, with a small area footprint, the optimization of the residue curve should consider the design of the interstage gain.

3.2.2.1 Gain Stage

Based on a common Flip-Around Multiplying DAC (FA-MDAC) represented in Figure 3.19, the input is sampled by $C_S + C_F$ in the first clock phase while in the second clock phase the reference is subtracted only on C_S . This way, the closed-loop gain is defined by a ratio of capacitor 1 + C_S/C_F . The capacitor ratio mismatch is well controlled, both the charge subtraction weighted by C_S/C_F and the gain are well-controlled. By default, this architecture fits the conventional residue gain and feedback gain values of respectively 2 and 1.

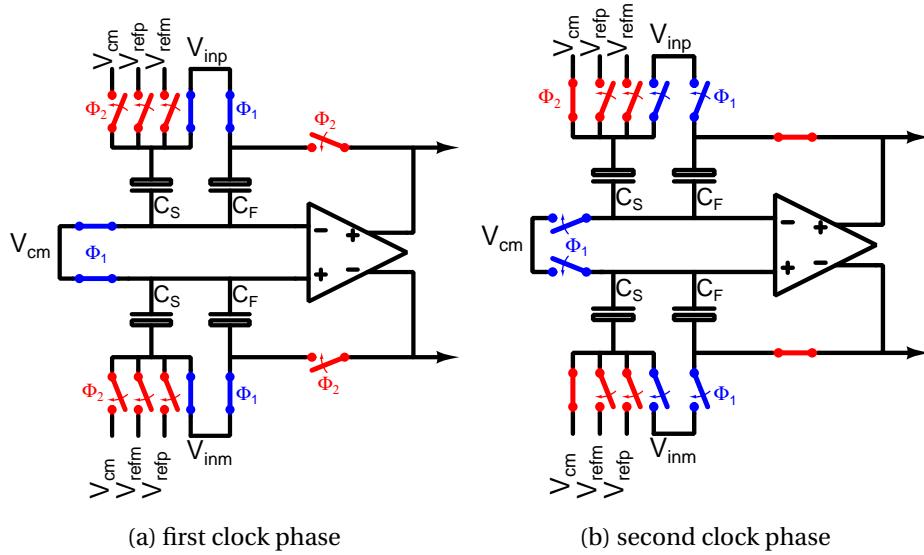


Figure 3.19 Standard Flip-Around MDAC operation for the algorithmic implementation

inter stage gain: The second tuning relates to the inter-stage gain. As only the sampling of the first stage residue shall be multiplied by a factor of two, an extra capacitance C_G is mandatory. As represented in Figure 3.20a, during the sampling phase the capacitor C_G is connected to the inputs of the OTA and the first stage residue for the sampling. Then illustrated by Figure 3.20b, till to the end of the sample conversion the latter is connected to the inputs of the OTA and the common-mode voltage V_{cm} .

Over the first clock cycle, the charges stored in the system for an amplifier gain A are

$$Q_{11p} = (C_G + C_S + C_F)(V_{inp}[n-1] - V_{cm}) \quad (3.20)$$

$$Q_{12p} = (C_S)(V_{ref}b_i[n-1] - V^-[n]) + C_G(V_{cm} - V^-[n]) + C_F(V_{op}[n] - V^-[n]) \quad (3.21)$$

$$Q_{11m} = (C_G + C_S + C_F)(V_{inm}[n-1] - V_{cm}) \quad (3.22)$$

$$Q_{12m} = (C_S)(V_{ref}b_i[n-1] - V^+[n]) + C_G(V_{cm} - V^+[n]) + C_F(V_{om}[n] - V^+[n]) \quad (3.23)$$

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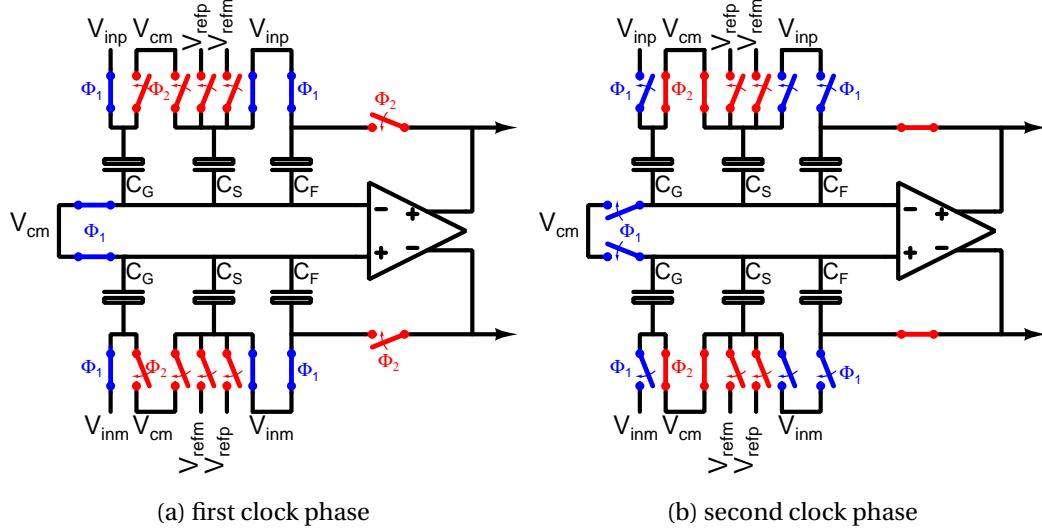


Figure 3.20 Flip-Around MDAC operation during the first clock cycle only for the implementation of interstage gain

which results in a differential output voltage following

$$V_{\text{out}}[n] = \frac{C_G + C_S + C_F}{C_F + \frac{C_G + C_S + C_F}{A}} V_{\text{in}}[n-1] - \frac{C_S}{C_F + \frac{C_G + C_S + C_F}{A}} V_{\text{ref}} b_i[n-1] \quad (3.24)$$

Then, the gain capacitor being always connected to the V_{cm} , the transfer function for the following clock cycles is

$$V_{\text{out}}[n] = \frac{C_S + C_F}{C_F + \frac{C_G + C_S + C_F}{A}} V_{\text{in}}[n-1] - \frac{C_S}{C_F + \frac{C_G + C_S + C_F}{A}} V_{\text{ref}} b_i[n-1] \quad (3.25)$$

We deduce the interstage gain as the ratio of input gain between the first and the following clock cycles, to wit, $1 + \frac{C_G}{C_S + C_F}$. In this configuration, the gain capacitor is not disconnected to prevent a switch injecting thermal noise on the input of the amplifier, and to simplify the digital calibration as the feedback gain is constant.

feedback gain: To optimize the feedback gain b , either new references can be generated for this stage, or an extra capacitor can be charged and connected. The change of reference voltages only for this stage is not recommended as extra circuitry is required which could exhibit a temperature variation in opposition to the first stage references. In this case, the accuracy of the ADC is compromised.

To the contrary, a capacitor ratio based design based on capacitance experiences a reduced alteration and good variation over temperature and process. As the feedback gain of a conventional FA-MDAC has been set to $C_S/C_F = 1$, only an extra fraction of V_{ref} capacitance is required. Consider-

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ering a design with unit capacitors, both the sampling and the feedback capacitance could be Q units. Figure 3.21 highlights the extra capacitance C_B of P units connected between the OTA inputs and the feedback voltage applied to C_S in order to bring charges in the amounts of $C_B/C_F = P/Q$ of V_{ref} . During the sampling phase on C_S and C_F , this C_B capacitor is reset by connecting its plates to the common-mode voltage V_{cm} .

For instance, a feedback gain $b = 1.6$ need an extra 0.6 times V_{ref} . This ratio being equal to 3/5, one set $C_S = C_F = 5C_0$ with $C_B = 3C_0$. And for a feedback gain $b = 1.25$, $C_S = C_F = 4C_0$ and $C_B = C_0$. In general, a feedback gain b in the form 1+P/Q requires 2Q unit capacitors for C_S and C_F and P unit capacitors for C_B . To reduce the area, Q should be the smallest possible.

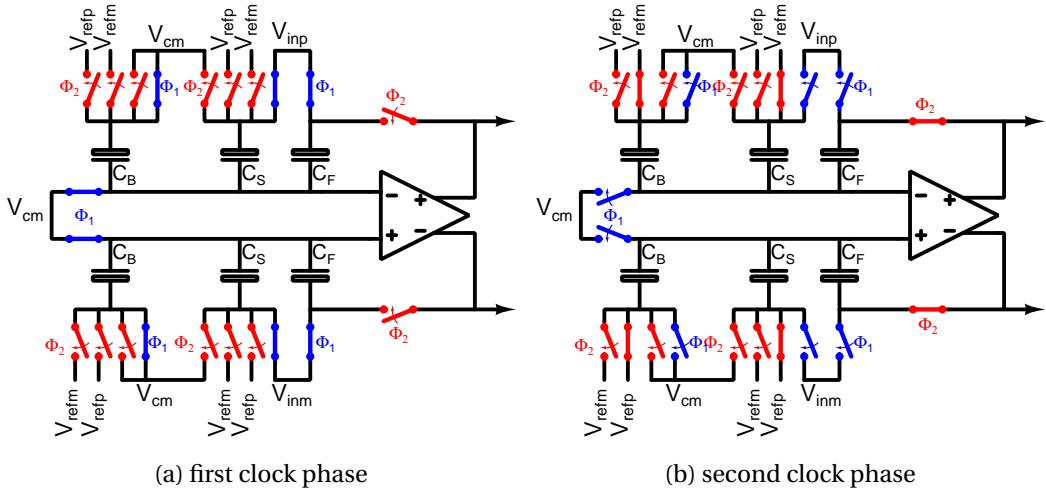


Figure 3.21 Flip-Around MDAC operation for the algorithmic implementation of arbitrary feedback gain

To estimate the error by combining the modification of the interstage gain and the feedback gain, over the first clock cycle, the charges stored in the system are

$$Q_{11p} = (C_G + C_S + C_F)(V_{\text{inp}}[n-1] - V_{\text{cm}}) + C_B(V_{\text{cm}} - V_{\text{cm}}) \quad (3.26)$$

$$Q_{12p} = (C_S + C_B)(V_{\text{ref}}b_i[n-1] - V^-[n]) + C_G(V_{\text{cm}} - V^-[n]) + C_F(V_{\text{op}}[n] - V^-[n]) \quad (3.27)$$

$$Q_{11m} = (C_G + C_S + C_F)(V_{\text{inm}}[n-1] - V_{\text{cm}}) + C_B(V_{\text{cm}} - V_{\text{cm}}) \quad (3.28)$$

$$Q_{12m} = (C_S + C_B)(V_{\text{ref}}b_i[n-1] - V^+[n]) + C_G(V_{\text{cm}} - V^+[n]) + C_F(V_{\text{om}}[n] - V^+[n]) \quad (3.29)$$

which results in a differential output voltage following

$$V_{\text{out}}[n] = \frac{C_G + C_S + C_F}{C_F + \frac{C_B + C_G + C_S + C_F}{A}} V_{\text{in}}[n-1] - \frac{C_S + C_B}{C_F + \frac{C_B + C_G + C_S + C_F}{A}} V_{\text{ref}}b_i[n-1] \quad (3.30)$$

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Then, in the same manner, the differential output voltage for following clock cycles is

$$V_{\text{out}}[n] = \frac{C_S + C_F}{C_F + \frac{C_B + C_G + C_S + C_F}{A}} V_{\text{in}}[n-1] - \frac{C_S + C_B}{C_F + \frac{C_B + C_G + C_S + C_F}{A}} V_{\text{ref}} b_i[n-1] \quad (3.31)$$

optimization of ratio: For the sake of clarity, we define the interstage gain of $g = 1 + C_G/(2C_F)$ and a feedback gain of $b = 1 + C_B/C_F$, after N clock cycle the estimated error for the same output code is

$$\text{error}[N] = g \times 2^N \left(1 - \left(\frac{1}{1 + \frac{2g+b-1}{A}} \right)^N \right) V_{\text{in}} - b \times \sum_{i=0}^{N-1} 2^i \left(1 - \left(\frac{1}{1 + \frac{2g+b-1}{A}} \right)^{i+1} \right) V_{\text{ref}} \quad (3.32)$$

From this equation, the minimum gain of the amplifier can be calculated as we already know the maximum excursion of this sub-ADC input range: $\pm V_{\text{ref}}/2$. It is also worth to note the impact of the feedback and the interstage gain on the error for a given DC Gain of the OTA. Figure 3.22a depicts the error at the end of the sample conversion for different values of the feedback gain b . In order to preserve the symmetry of the residue curve the threshold voltage of the 3-levels quantizer shall be $\pm b/4V_{\text{ref}}$. In turn the output range is delimited by $\pm b/2V_{\text{ref}}$.

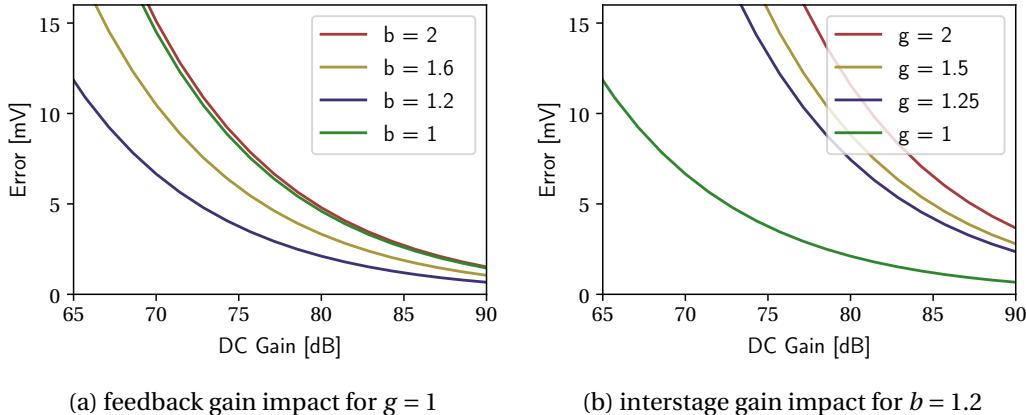


Figure 3.22 Impact of modification introduced on the standard Flip-Around MDAC

As the feedback gain increase, the OTA DC Gain shall also increase to reach the same level of error. Let us suppose the maximum error to target is 7 mV which corresponds to a resolution of 6-bits on the last stage. For an interstage gain $g = 1$, the minimum gain varies from 67 dB to 76 dB, while a variation of g for $b = 1.2$ the minimum gain varies from 67 dB to 84 dB. We deduce a higher sensitivity to the interstage gain rather than to feedback. Moreover, the feedback with less error on the settling is for $b = 1.2$. This can be explained by the fact the residue transfer function does not exceed thresholds of the 3-levels quantizer as often. Therefore, large settling errors occur later in the conversion process for input voltages close to the limits of its excursion. The settling error is thus multiplied by a smaller factor.

Therefore, the optimization leads us to the solution of $b = 1.2, g = 1$ which corresponds to the conventional sizing of the algorithmic. This point is equivalent to an output range of $\pm 0.6V_{ref}$ with threshold of $\pm 0.3V_{ref}$. The system is able to withstand 200 mV of error coming from the analog devices offset and charge injections, enhance the output swing of the sub-ADC, while the constraint on the OTA Gain is reduced. The second option close behind is the conventional sizing $b = 1, g = 1$ with an area smaller than the optimized solution. With a priority set on the area, we let the impact of temperature on each of these two at the transistor level simulation decides which is the final one.

That said, the amplifier drives the capacitor $C_S + C_F$ during first clock phases and $C_F \parallel C_{\text{parasitics}}$ during other phases. The latter capacitance being small, in the phase when the comparators make decisions for the feedback to apply, the amplifier design becomes difficult in order to prevent ringing of the output voltage.

3.2.2.2 Sequencing

In the conventional FA-MDAC, and in the modified version too, the comparator shall make a decision at the end of the settling of the first clock phase and apply the appropriate feedback from the beginning of the second clock phase. In such circumstances, the comparator endures an important timing constraint for an accuracy around 10-bits.

Moreover, the OTA shall reach this accuracy level within half a clock cycle and the output voltage exhibits large variations. In order to overcome this limitation and reduce design pressure upon analog blocks, the digital sequencing can be altered for a small modification of the analog core. This section discusses the modification bestowed.

The first modification introduced concerns the sampling of the input and the residue of this sub-ADC. In a conventional FA-MDAC, the input is sampled on $C_S + C_F$ at the beginning of each clock cycle before C_F is re-connected into a feedback capacitor. In the proposed sequence of operation an extra capacitor of the same amount of C_S is required. Let's call the latter C_{S2} and the previous sampling capacitor C_{S1} rather than C_S .

During the first clock cycle, the behaviour is almost identical with the FA-MDAC at the exception of a capacitor C_{S2} connected on the residue and the local ground as depicted by Figure 3.23a. Meanwhile, the 3-levels quantizer estimates the feedback voltage to apply so that the residue is constrained in the desired output range. In a second clock cycle, Figure 3.23b, C_F is in feedback mode while a feedback is applied to the original sampling capacitor C_{S1} . These two clock cycles are equivalent to the two clock phases of the FA-MDAC first clock cycle. C_{S2} connected on the residue is accurately sampling the next input. The residue at the end of the second clock cycle is given by equation (3.34).

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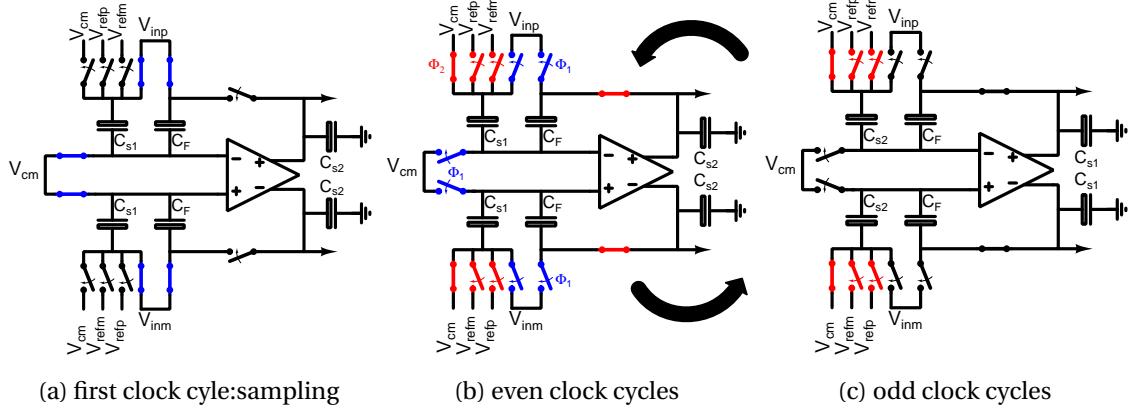


Figure 3.23 Proposed sequencing to relax Flip-Around MDAC timing constraints

$$\Delta Q_{\Phi_{1 \rightarrow 2}} = C_{S1} [(V_{ref}[2] - V[2]^-) - (V_{inp} - V[1]^-)] + C_F [(V_{op}[2] - V[2]^-) - (V_{inp} - V[1]^-)] \quad (3.33)$$

$$+ C_{S2} [V_{op}[2] - V_{op}[1]]$$

$$V_{op}[2] = \frac{C_F + C_{S1}}{C_{S2} + C_F \left(1 + \frac{C_F + C_{S1}}{AC_F}\right)} (V_{inp} - V_{cm}) - \frac{C_{S1}}{C_{S2} + C_F \left(1 + \frac{C_F + C_{S1}}{AC_F}\right)} V_{ref}[2] + \frac{C_{S2}}{C_{S2} + C_F \left(1 + \frac{C_F + C_{S1}}{AC_F}\right)} V_{cm} \quad (3.34)$$

This implementation follows the same equation as the conventional FA-MDAC. A global factor scale down the residue by two in comparison. As the residue is scaled down, large steps occurs less often such that OTA constraints on the gain is relieved.

Then, the sampling capacitors are swapped without breaking the feedback loop made by C_F as in Figure 3.23c. Again, the 3-levels quantizer estimates the feedback voltage to constraint the residue within the desired output range. In the next clock cycle, sampling capacitors are swapped and a new feedback voltage estimation is performed by the 3-levels quantizer. This process repeats over and over, Figure 3.23, till the last clock cycle in which the 3-levels quantizer outputs the two first bits of the following stage.

$$\Delta Q_{\Phi_{2 \rightarrow 3}} = C_{S1} [(V_{op}[3]) - (V_{ref}[2] - V[2]^-)] + C_F [(V_{op}[3] - V[3]^-) - (V_{op}[2] - V[2]^-)] \quad (3.35)$$

$$+ C_{S2} [(V_{ref}[3] - V[3]^-) - V_{op}[2]]$$

$$V_{op}[3] = \frac{C_{S2} + C_F \left(1 + \frac{C_F + C_{S1}}{AC_F}\right)}{C_{S1} + C_F \left(1 + \frac{C_F + C_{S2}}{AC_F}\right)} (V_{inp} - V_{cm}) - \frac{C_{S2}}{C_{S1} + C_F \left(1 + \frac{C_F + C_{S2}}{AC_F}\right)} V_{ref}[3] + \frac{C_{S2}}{C_{S1} + C_F \left(1 + \frac{C_F + C_{S2}}{AC_F}\right)} V_{cm} \quad (3.36)$$

This operation sequence, compared to the conventional sequence, loses one clock cycle: the two phase operation of the first clock cycle spread onto the two first clock cycles. Nevertheless, the timing constraints on the OTA and the comparator stress are relieved. The comparators have $T_{clk} - T_{settling} - T_{setup} - T_{logic}$ to make a decision, while the accuracy of the residue voltage can be reached for a longer settling time $T_{settling}$. Moreover, much OTA architectures have a minimal load criterion to ensure a minimum phase margin and an extra load that C_{S2} represents enhance the settling of marginally stable OTA.

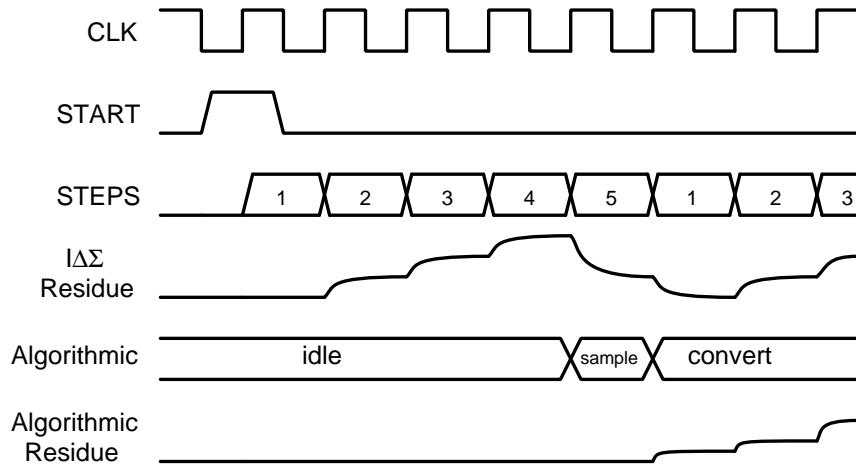


Figure 3.24 Sampling instant of the $\text{I}\Delta\Sigma$ residue

With the proposed sequencing, the sampling instant is twice the time span of the conventional one. As a result, Figure 3.24 represents the initialization of the ADC and when the residue of the first stage is sampled by this algorithmic sub-ADC. As the first stage reset the integrator during the first clock cycle, the algorithmic shall sample during the whole fifth clock cycle rather than half of this clock period. Therefore, the speed constraints on the first stage is relaxed.

3.2.2.3 1.5-bit DAC

In the same fashion done for the first-stage Incremental- $\Delta\Sigma$, the 3-levels quantizer is implemented by the comparison of passive differential voltage summation. With the specificities of this sub-ADC, the 3-levels quantizer shall be able to change its threshold voltages on the last clock cycle to generate the two-firsts bits of the SAR. The design procedures addressed in Section 3.2.1.2, this section will discuss the reference voltage change and its implication on the residue. For the conventional algorithmic sizing ($a = 2, b = 1$), it is noteworthy that there is no reference voltage change mandatory.

Figure 3.25 depicts one possibility to achieve the threshold change. C_1 and C_2 operates as demonstrated in the Section 3.2.1.2. At the last clock cycle denoted P_5 in the figure, the capacitor

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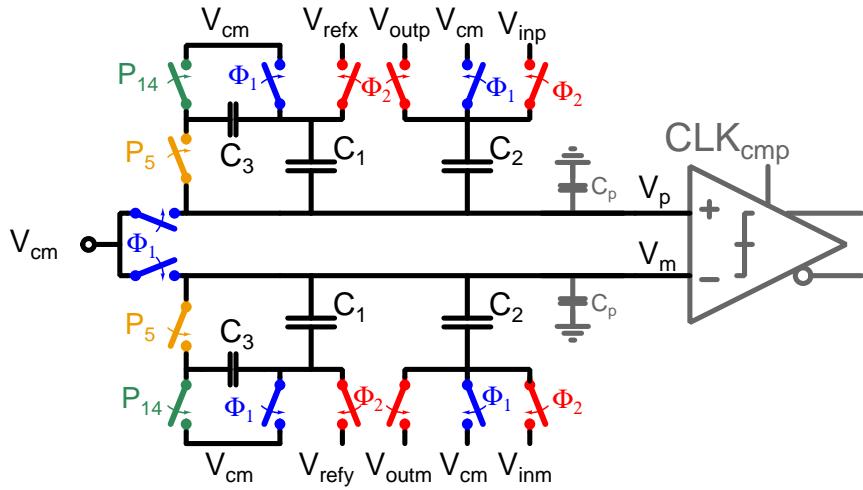


Figure 3.25 Threshold change in the conversion process

C_3 connects to the input voltages of the comparator. This way, the ratio of V_{refx} is defined by $\frac{C_1+C_3}{C_2}$ rather than $\frac{C_1}{C_2}$.

This solution does not let any floating nodes while the behaviour is fully defined by the procedure presented for the first stage. In order to size the capacitor, we consider a unit capacitance $C_0 = 12 fF$ such that $C_1 = 3C_0$, $C_2 = 10C_0$, and $C_3 = 2C_0$.

The impact on the residue is thus coming from the mismatch. The commit error increases the residue range by an amount ϵ_{res} given by equation (3.37) for an assumed ideal gain of 2. This expression is valid from the first to the penultimate clock cycle where V_{d_i} is the differential voltage applied to C_i capacitors.

$$\epsilon_{\text{res}} = 2 \left(\frac{\Delta C_1 + \Delta C_2}{C_1 + C_2 + C_p} \left(\sum_{i=1}^2 \Delta C_i V_{d_i} \right) - 2 \left(1 - \frac{\Delta C_1 + \Delta C_2}{C_1 + C_2 + C_p} \right) \left(\sum_{i=1}^2 \Delta C_i V_{cm_i} \right) \right) \quad (3.37)$$

In the same manner, the error committed on the last clock cycle engender a mismatch on the two first bits of the SAR. This error is likely given by equation (3.38).

$$\epsilon_{\text{res}} = 2 \left(\frac{\Delta C_1 + \Delta C_2 + \Delta C_3}{C_1 + C_2 + C_3 + C_p} \left(\sum_{i=1}^3 \Delta C_i V_{d_i} \right) - 2 \left(1 - \frac{\Delta C_1 + \Delta C_2 + \Delta C_3}{C_1 + C_2 + C_3 + C_p} \right) \left(\sum_{i=1}^3 \Delta C_i V_{cm_i} \right) \right) \quad (3.38)$$

3.2.2.4 Digital Circuit

define what is reused in the digital: To drive the analog core, the digital circuit also needs a clock generator, a sequencer, and driver interfaces. The sequencer and the clock generator available inside the digital circuit of the first stage are re-used while the driver interfaces are instantiated again for the switches command signal of this stage. The new sequencing no more being based

on clock phase for the MDAC, the clock phase generated only serves the purpose of the 3-levels quantizer.

the problematic of non overlapping without using clock phases: As switches in the MDAC connect several analog reference voltages on the same capacitor plates, non overlaps shall be respected to prevent the short circuit of them. In order to improve both the sustainability and the yield, the non-overlap time in the digital circuit shall be fully “synthesizable”. Then, non overlapping time being part of the digital static timing analysis, such cells ensure the operation with an increased reliability on the sub-ADC.

solution 1: A first possible realization could be the one depicted by Figure 3.26a. This solution can be implemented with standard digital tools with a pulse generation based on a clock and a delayed one. Unfortunately, this circuit suffers from possible glitches due to the multiplex of DFF outputs and clocks are used in a data path.

A Double-Edge circuit is able to implement the functionality desired as one clock sets the value to block analog switches till a delayed clock sample the signal to activate the analog switches. A usual realization is built around two pulse generation to trigger a latch at two distinct instant [112–115]. Pulses generation is considered as an analog circuit for which digital tools cope with badly.

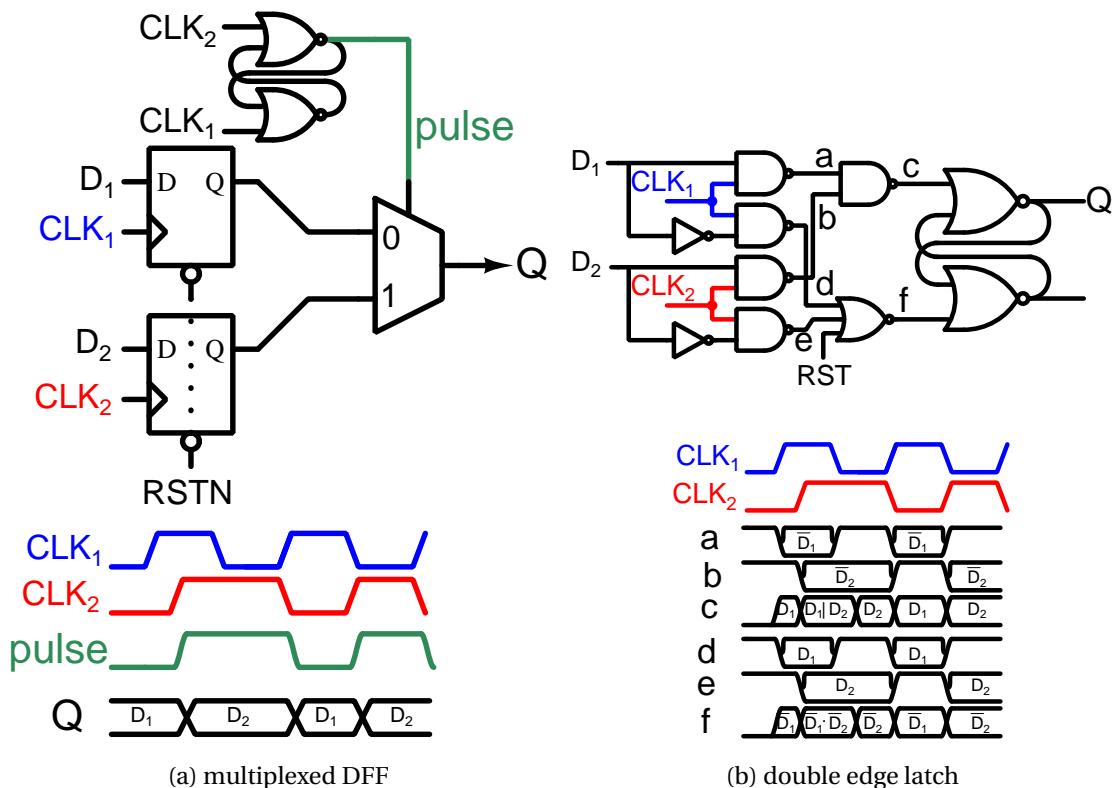


Figure 3.26 Possible realization of the dual-edge trigger D-Flip-Flop

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solution 2: In response, Figure 3.26b represents an alternative based on combinatorial logic. This clocked nor rs-latch with a reset generates a new dual-edge DFF with a distinct data path from the clock path. From a timing point of view, the non overlap between CLK_1 and CLK_2 shall be ideally ensured. Otherwise a glitch can occur for arbitrary D_1 and D_2 . In case of $D_1 = 0$, the overlapping of CLK_1 and CLK_2 is no more a concern. For timing constraints, the cell is sensitive to the placement.

solution 3 (the one kept): Proposed by Ralf Hildebrandt [116], such a block can be described with only two DFFs without mixing of the clock and data path and no possibility for glitches. This proposition is represented in Figure 3.27 after a change of CLK_2 as a delayed CLK_1 . Therefore, there is no hold time issue and the setup time constraint relaxed on the DFF triggered by CLK_1 put under pressure the DFF triggered by the delayed clock. Over temperature the transition time of analog switches increases as the non overlap time defined by the delay between the two clocks does.

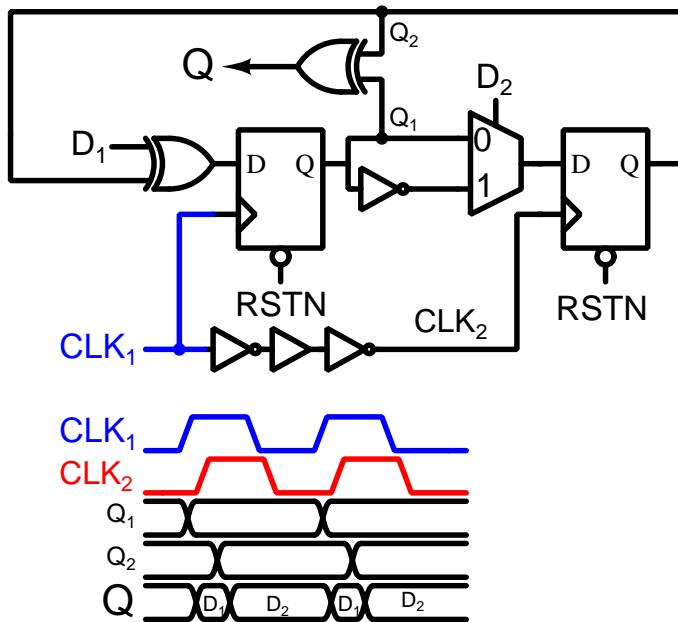


Figure 3.27 Synthetizable non-overlap circuit without failure in the static timing analysis

Then, the latter is followed by digital driver presented in Section 3.2.1.3.2 to prevent ambiguity in the sampled value when the settling time is limited and the non-overlapping time is short.

For switches in the 3-levels quantizer, two non overlapping clock phases are required. The already mentioned clock phase generator circuit of the first stage fits this purpose. A particular caution is paid at the clock phase connection such that the sampling occurs when the settling is almost performed around the instant of the falling edge of the main clock. As the delay between our pseudo dual edge trigger DFF (pseudo-DET-DFF) reduces the maximum settling time of the OTA, and non-overlapping time is limited by a delay cells, the skew of the clock tree gains

3.2 Sub-ADC Analysis

much importance. For accurate results, the clock of the clock phase generator shall be delayed in comparison of the clock provided to the pseudo-DET-DFFs.

The algorithmic ADC is known to be sensitive to analogue imperfections. At a system-level, the architecture and the conversion sequencing have been thought to reduce the error on the settling of the residue. From the equation of the error in the MDAC, we consider the introduction of an interstage gain g , and a tunable feedback gain f . The two candidate pairs of values exhibiting a reduce error are the conventional design implemented ($g=1, f=1$), and ($g=1, f=1.2$). To facilitate the digital implementation of non-overlapping command signal without clock phase, the digital interface has been investigated. The selected circuit allows the introduction of a scan chain, and simplifies the layout phase without introducing failure in the timing analysis.

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3.2.3 SAR

The SAR architecture benefits from using only one comparator to reduce the occupied area. With recent progress, the SAR converter outperformed power consumption, its area occupancy has tremendously shrunk, and the speed has been soaring. Made of a capacitive DAC, a comparator, and a digital control circuit, the primary source of power dissipation are the digital control circuit and capacitive reference DAC network, while the source of large area occupancy is the capacitive DAC.

Since the two first bits of the SAR are given by the previous stage, one clock cycle will be used for pre-charging capacitors, and remaining clock cycles before the next sample extract more information. In consequence with 5 clock cycles, the SAR provides 6 bits. An adaptation of the DAC is necessary.

In addition to the specification, an extra mode exists to increase the resolution of the ADC by sacrificing the sampling rate. This extra mode performs a conversion over 6 clock cycles instead of 5. While this does not impact the structure of the analog in the two preceding stages, several modifications are required in this sub-ADC. Therefore, we discuss in this section of the relevant modification in the capacitive reference DAC network and in the digital circuit.

3.2.3.1 Capacitive DAC Array

To address both the area occupancy and further reduce the energy consumption, the DAC architecture can be optimized by decreasing the capacitance as discussed in section 2.1.4. For thermal noise reason of switches, the split-capacitor structure is preferred over split-junction.

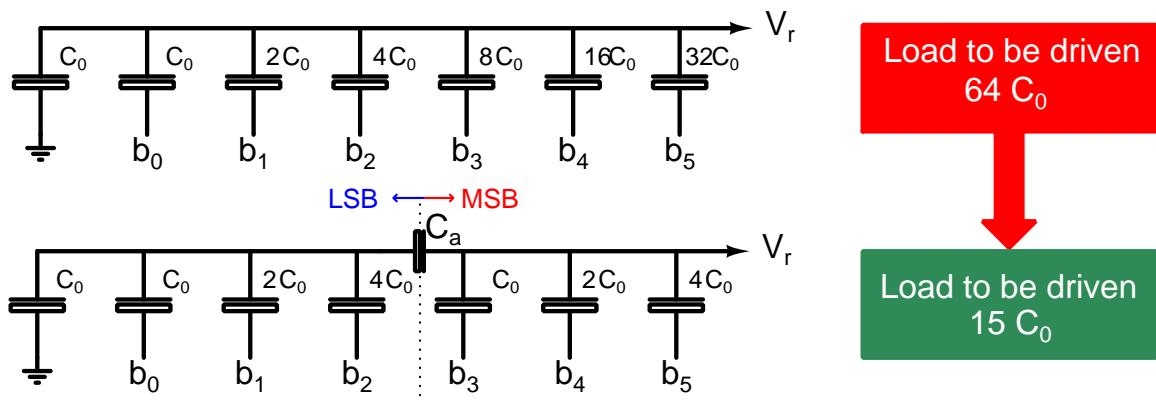


Figure 3.28 Load reduction for both the OTA of the Algorithmic and the voltage references buffers

position of the attenuation capacitor to minimize the load: In Figure 3.28, the position of the attenuation capacitance C_a can be placed between either group of two consecutive capacitors of the DAC, which create a group of **MSB** capacitors and a group of **LSB** capacitors. The attenuation

capacitor is at the position which minimize the load seen by voltage references and the previous stage OTA. In our case, the attenuation capacitor creates one group of four capacitors for LSBs, and one group of three capacitors for MSBs.

parasitic insensitive: Switches connecting either voltage of the following set $\{V_{in}, V_{refp}, V_{refm}\}$ are on the bottom plate (side opposite to the comparator input). It makes the DAC inherently insensitive to switches' parasitic capacitance and still keep the criterion on accurate reference voltages $\varepsilon_{\text{references}} < 1\text{LSB}$.

voltages generated and scale: By application of superposition, the output voltage V_r is given by equation (3.39) where C_i the capacitor connected to the voltage $b_i V_{\text{ref}}$ of the aforementioned figure. A consequence of the attenuation capacitor is the difficult implementation to have both a binary scale and C_a a multiple integer of the unit capacitance C_0 .

$$V_r = \frac{(C_a + \sum_{i \in \text{LSB}} C_i)}{(C_a + \sum_{i \in \text{LSB}} C_i)(C_a + \sum_{i \in \text{MSB}} C_i) - C_a^2} \sum_{i \in \text{MSB}} C_i b_i V_{\text{ref}} \\ + \frac{C_a}{(C_a + \sum_{i \in \text{LSB}} C_i)(C_a + \sum_{i \in \text{MSB}} C_i) - C_a^2} \sum_{i \in \text{LSB}} C_i b_i V_{\text{ref}} \quad (3.39)$$

In the case of ideal value of the attenuation capacitor $C_a = 8/7$ for a configuration as represented in Figure 3.28, the voltage contribution of each capacitor driven by b_5 to b_0 is respectively $\{0.5, 0.25, 0.125, 0.0625, 0.03125, 0.015625\}$.

second stage decision error: The previous stage generating the two first bits of the SAR, an erroneous decision of the algorithmic impacts the overall decisions of the SAR and cannot be fully corrected. Without any redundancy as represented in Figure 3.29a, an error in the decision made by comparators providing a 01 instead of a 10 corresponds a final error of 1 LSB. The redundancy could be introduced by decreasing the two first bits' weight A_{MSB} and $A_{\text{MSB}-1}$: a weight distribution of A_i 's as 3-1.5-1-4-2-1-1 rather than 4-2-1-4-2-1-1 times the unit capacitor. In fact, keeping A_i as an integer multiple of the unit capacitor, the version 6-3-2-4-2-1-1 is implemented with an ideal attenuation capacitor of $8/3$. As depicted by Figure 3.29b, the resulting error is less than 1 LSB. The counterpart is a bigger LSB, which is representative of a trade off between robustness and resolution.

attenuation capacitor rounding for redundancy: The attenuation capacitor scaling down the A_i 's in the LSB part can be an alternative to introduce redundancy. As the ideal attenuation capacitor is most of the time not an integer multiple of the unit capacitor, rounding to the superior integer could be sufficient.

For instance, let us consider two "capacitors" in series of which their equivalent capacitance is the weight the smallest capacitor within the MSB group in Figure 3.28. The size of the attenuation

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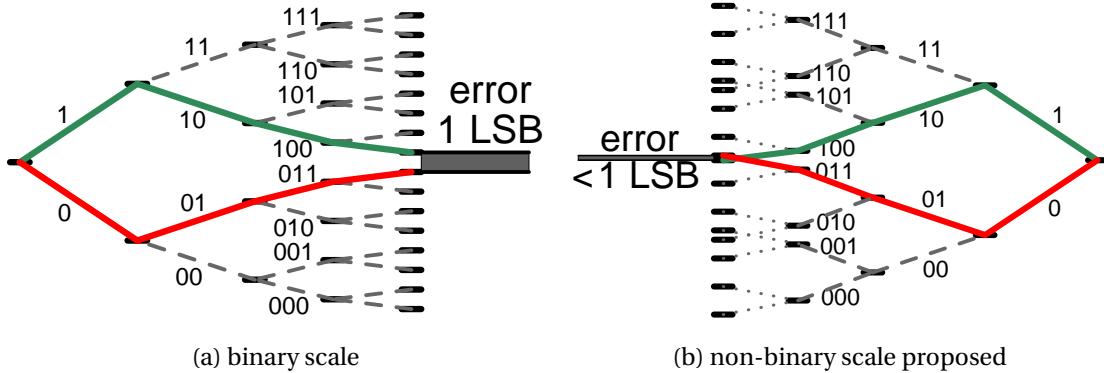


Figure 3.29 Alteration of the search scale to provide robustness with redundancy

capacitor to ensure ideal scale is given by $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$. Similarly, in the case of a split-dac the attenuation capacitor is given by equation (3.40).

$$\frac{1}{C_{eq}} = \frac{1}{C_a} + \frac{1}{\sum_{i \in LSB} C_i} \quad (3.40)$$

For a capacitance $C_{eq} = 2$ and $C_2 = 8$, the expected value of C_1 to ensure the equality is $8/3 \approx 2.667$. Rounding the value of C_1 to 3, changes the equivalent capacitance to $24/11 \approx 2.18$ while a ceiling of C_1 to 2, results into an equivalent capacitance of $8/5 = 1.6$. Therefore, rounding the attenuation capacitor gives more weight to the LSB group to be able to alleviate errors of the previous stage. This solution also results into a resolution/robustness trade-off with an easier realization since each capacitance is made of an integer multiple of the unit capacitor. The finale capacitor distribution is thus 6-3-2—4-2-1-1 with an attenuation capacitor of 3 unit capacitor. The reference voltages generated are $\{0.5, 0.25, 0.167, 0.091, 0.045, 0.023, 0.011\}$.

unit capacitor sizing procedure: Based on the procedure formulated in [57], we estimate the noise contribution and the mismatch impact on the resolution of the DAC with respect to the unit capacitor size. We consider that the maximum tolerable error for an N-bit DAC is $\pm 1/2$ LSB which equals $V_{ref}/2^{N+1}$. We suppose that mismatch variation and noise contribution of each capacitor are uncorrelated so that the standard deviation of the error is given by $\sigma^2 = \sigma_{mismatch}^2 + \sigma_{noise}^2$, and we shall constrain the error to within $\pm 1/2$ LSB.

matching error contribution: For the expectation of the matching to be relevant, the assumption is a common-centroid layout for the implementation of the DAC to get rid of all gradient related source of mismatch (temperature, mechanical stress, ...) to only keep the manufacturing variations. Capacitors split into multiple of unit capacitors with a normal distribution of the unit capacitance $\frac{\Delta C}{C} \approx N(0, \sigma_0^2)$, the mismatch of a single capacitor $C_i = A_i C_0$ is given by $\frac{\Delta C_i}{C_i} \approx N(0, A_i \sigma_0^2)$ if each unit capacitor variation is independent from the other.

3.2 Sub-ADC Analysis

We thus set a limit for the mismatch by the equation (3.41) where N_σ is the number of standard deviations we consider for the confidence interval, and a LSB error contribution as the maximum error defined in [57] weighted by the $C_a/(C_a + \sum_{i \in LSB} C_i)$.

$$\frac{V_{\text{ref}}}{2^{N+1}} = \frac{N_\sigma \sigma_0 V_{\text{ref}}}{\sum_{i \in LSB} A_i - N_\sigma \sigma_0 \sqrt{\sum_{i \in LSB} A_i}} \sum_{i \in LSB} \sqrt{A_i} \times \frac{A_a(1-N_\sigma \sigma_0)}{(A_a + \sum_{i \in LSB} A_i)(1-N_\sigma \sigma_0)} \\ + \frac{N_\sigma \sigma_0 V_{\text{ref}}}{\sum_{i \in MSB} A_i - N_\sigma \sigma_0 \sqrt{\sum_{i \in MSB} A_i}} \sum_{i \in MSB} \sqrt{A_i} \quad (3.41)$$

noise estimation: Let's now consider the noise introduced by switches on the DAC. Assuming switches as a resistance, the voltage standard deviation of the thermal noise ΔV_i on a capacitance $C_i = A_i C_0$ is given by equation (3.42).

$$\Delta V_i = \sqrt{\frac{k_B T}{A_i C_0}} \quad (3.42)$$

From the equation developed, the output noise on the input of the comparator is defined by the equation (3.43)

$$\Delta V_{r\text{noise}} = \frac{\left(\frac{C_a}{C_0} + \sum_{i \in LSB} A_i\right)\left(\sum_{i \in MSB} \sqrt{\frac{k_B T}{A_i}}\right) + \frac{C_a}{C_0} \left(\sum_{i \in LSB} \sqrt{\frac{k_B T}{A_i}}\right)}{\left(\frac{C_a}{C_0} + \sum_{i \in LSB} A_i\right)\left(\frac{C_a}{C_0} + \sum_{i \in MSB} A_i\right) - \left(\frac{C_a}{C_0}\right)^2} \frac{1}{\sqrt{C_0}} \quad (3.43)$$

unit capacitor size: From thence, and the variation σ_0 known as a function of C_0 , the value of the unit capacitance required is given by a Newton-Raphson algorithm. The unit capacitor needed to cope with a $N_\sigma = 6$ is about 48 fF. In comparison a classical DAC would have required a unit capacitance of 42 fF for the same error budget. For the OTA of the second stage, the load to be driven is thus 950 fF saving 1.7 pF. The noise on the voltage to be compared V_r is 847 μV_{rms} at 475°K.

modification for a 6 clock cycle operation: To allow an operation over 6 clock cycles, the DAC

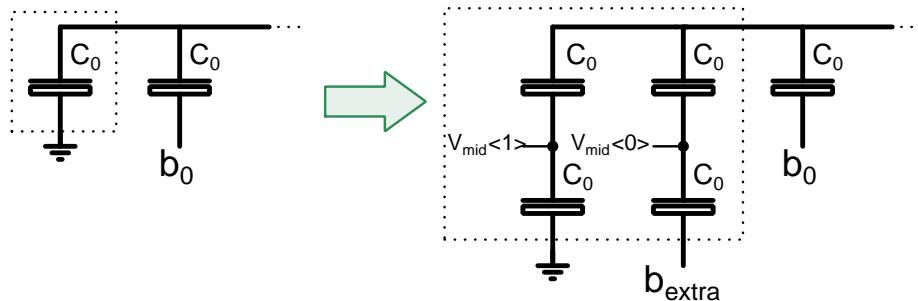


Figure 3.30 DAC modification to perform conversion with an extra clock cycle

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shall be modified in consequence. Usual configuration would implement an extra MSB capacitor doubling the area. Here, the modification consists in splitting the extra unit capacitor not driven into two half the capacitance in parallel. To keep the mismatch low, half the unit capacitance is performed by connecting in series two unit capacitors as represented in Figure 3.30.

In a normal 5 clock operation, b_{extra} is the same potential as the one at its left, such that the block of 4 is equivalent to a unit capacitance C_0 .

Since this modification adds two floating points, voltages $V_{mid} < 1 : 0 >$ are defined when the DAC sample the input voltages. While sampling, in a charge redistribution mode operation, the input voltage is sampled on one end of capacitors. On the other end, capacitors are connected to a virtual ground such as the common mode voltage in a differential circuit. In a differential circuit as ours, $V_{mid} < 1 : 0 > = V_{cm}$ during the sampling. Then, they are disconnected to let the chosen switching scheme drives voltage applied on a half capacitance. The resulting DAC is presented in Figure 3.31.

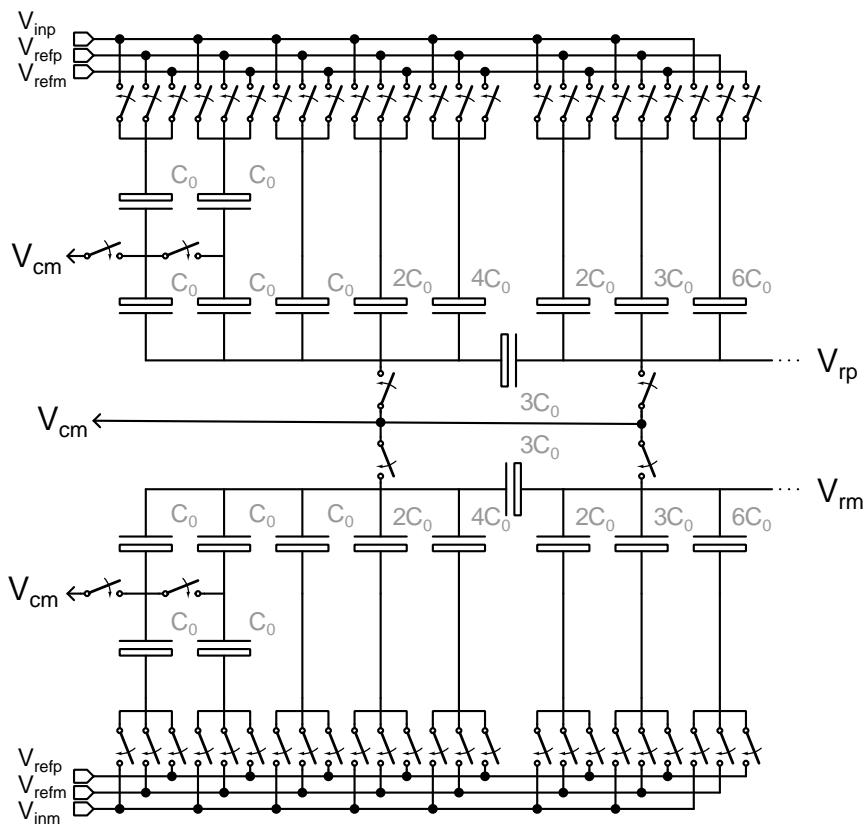


Figure 3.31 Final DAC schematic for the SAR

3.2.3.2 Switching Scheme

Based on the discussion in Section 2.1.4.2, the conventional charge-redistribution method is not power effective [63]. A monotonic switching can divide by almost two the switching loss as the MSB capacitor is no more necessary. However, the common mode voltage undergoes decision dependant large variations. Represented in Figure 3.32 for the sake of comprehension, a monotonic based switching keeps the V_{cm} within the input range. For each decision made, as only one voltage is altered at a time, the common mode voltage inevitably fluctuates from one clock period to another. Let's suppose the final output code is full of ones, the common mode voltage will be ever increasing to reach the maximum input voltages. While for a final output code full of zeros, the common mode voltage will be ever decreasing to reach the minimum input voltages. This is a high-demanding input range on the comparator performance for a switching power consumption relaxed. At least with a V_{cm} -monotonic once the decision is made, the decision is applied on both sides by the application of complementary voltages to keep the common mode voltage around half V_{DD} .

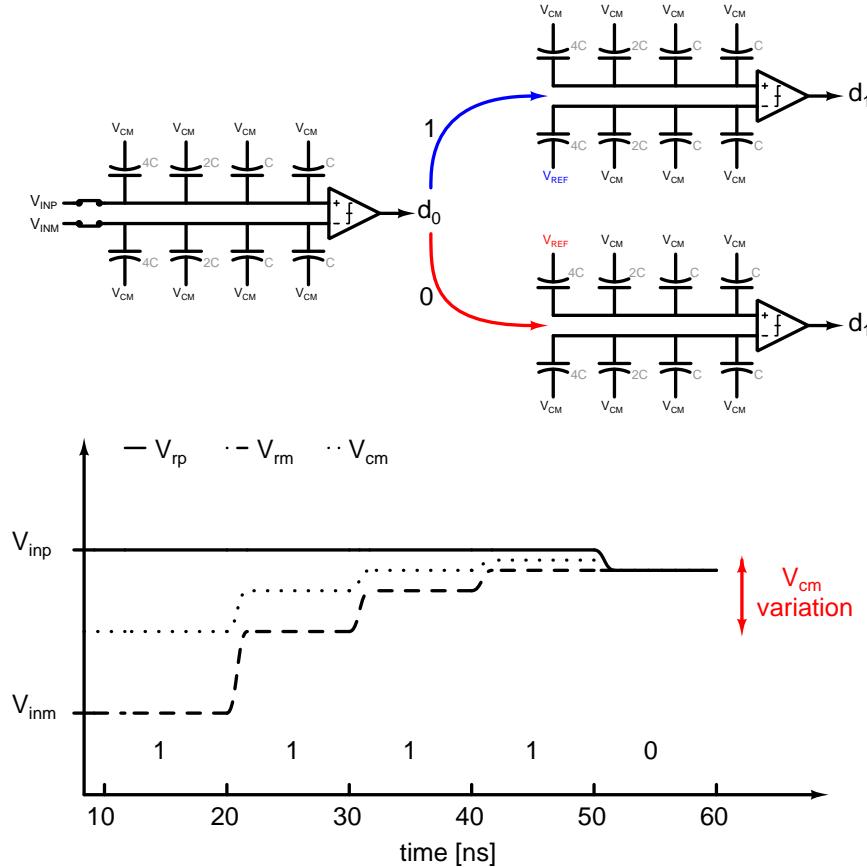


Figure 3.32 Change of the common mode voltage in a monotonic based digital scheme

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Unfortunately, both monotonic switching methods rely on a top sampling technique. To the contrary the bottom plate sampling of the conventional charge-redistribution is related to better linearity and higher resolution: the method reduces the effect of charge injection during switching off and the non-linearity of the junction capacitance of the top plate switch is negligible. As the charge injection of switches is a linear function of the temperature at a rate of $C_{ox}WL\alpha_{V_{th}}$, the conventional switching scheme has been selected.

3.2.3.3 Digital Circuit

As the clock frequency increase, or as the temperature degrades the speed of the analog part, the digital constraints on a SAR become challenging. The timing constraint is defined by the time the DAC requires to settle to the wished accuracy, the delay of the comparator, and the time the logic need to respond.

synchronous: In a synchronous SAR, the high demand is assumed on the comparator to latch as fast as necessary to let the digital toggle switches according to the decision made. The clock period is usually defined on the worst speed corner for the lowest power supply voltage and the higher temperature.

asynchronous: To the contrary an asynchronous SAR waits for the comparator decision and “digital” does not wait for an edge of the clock. For unusually too long decision time, the digital code might be incomplete and result in errors. Forcing the decision in case of metastability did not have the same impact on the digital code representation of the input compared to an erroneous decision. Indeed, the metastability occurs in decisions where the inputs of the comparator are close enough to prevent either the noise or mismatch to set the decision value within the allotted time. A comparator sensing a difference less than an LSB is sufficient.

synchronous versus asynchronous: This first modification in the operation increases the allotted time for the comparator to make a decision: the probability of the metastability is highly reduced for the same comparator while the power consumption can be reduced for the same probability of metastable events.

Figure 3.33 compares the synchronous and the pseudo-asynchronous operation which forces the decision in case of metastability. The instants in delimited by blue boxes represents the domain when the decision shall be made to ensure correct operation based on setup and hold violation in the logic. Although, in a synchronous digital scheme the time window is “constant”, in the proposed version the time window is at least equal or greater. The stringent constraints on the comparator is thus relaxed.

Assuming the clocked comparator delay follows a small signal model of a cross-coupled latch with regeneration time constant τ_{reg} , link the differential input voltage ΔV_{in} pre-amplified in a linear phase, to the decision time as in (3.44).

$$\Delta V_{out}(t) = \Delta V_{out}(0) \exp(\tau_{reg}) \quad (3.44)$$

The probability to generate an erroneous decision depends on the input voltage applied, the temperature, the process and can further generate metastability within the logic as described in Appendix D. Considering a synchronous ADC, failures in digital circuit due to metastability is critical and missing a most significant bit should be prevented.

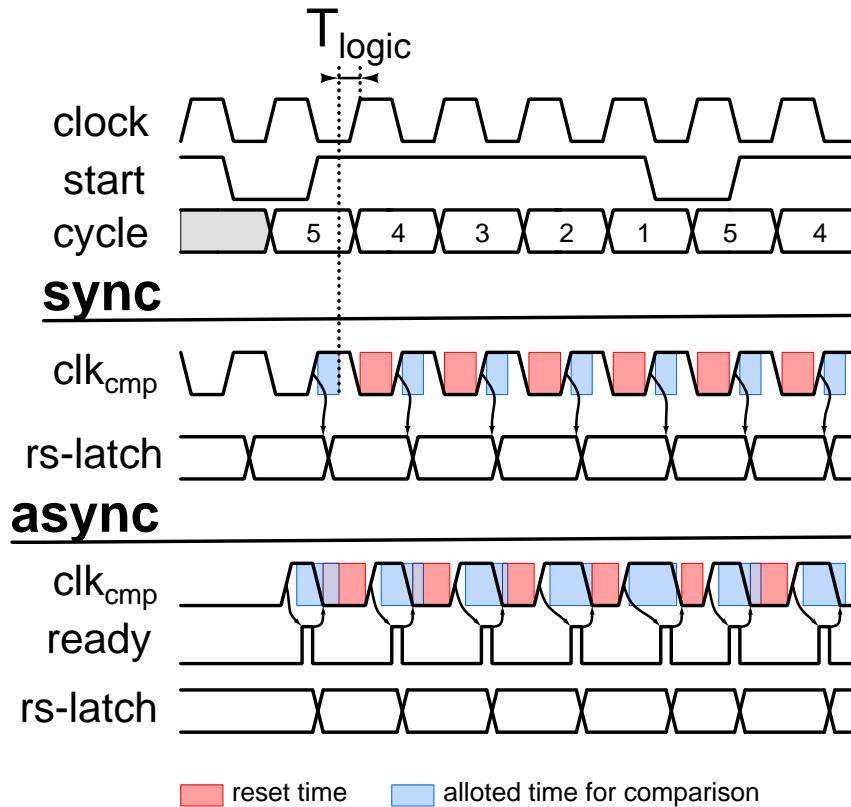


Figure 3.33 Comparator constraint relaxed by the use of pseudo-synchronous digital scheme

Furthermore, a comparator making a decision quickly also benefits from a long time to reset. Otherwise, a reduce reset time engenders a hysteresis owing to a mismatch in the potential of parasitics. The hysteresis introduced is thence state dependant and vary from one clock cycle to the other.

In the design of the latch, the delay shall be less than $T_{clk} - T_{logic} - T_{settlingDAC}$. Without considering the clock skew the comparator delay can be as large as 7 ns. This value does not consider the clock skew. Nevertheless, to reduce the metastability to a maximum without increased tremendously the power consumption the delay have been fixed to 3 ns at maximum with a standard variation of 500 ps.

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In the case of a SAR ADC clocked at 100 MHz with the proposed digital scheme, the probability of a metastable event to occur is estimated to be less than 10^{-18} at 175°C (Appendix D): the typical lifetime of an electronic component is not sufficient to be sure to see a metastable event.

sequencer: Considering PVT variations and the case of the metastability, an asynchronous digital is implemented. To prevent halt in the conversion, the clock provides a time slot in which a flag is raised at the end to indicate the metastability and force the execution of subsequent cycles as in [74]. This ensures at the end of the conversion a digital code of the desired length and easily interfaceable with a synchronous digital.

The sequencer resulting is depicted in Figure 3.34 to generate the phase in one hot encoding. In front of the first DFF, the logic allows continuous conversion for a START signal hold to zero. Therefore, the digital sequencer can be halted and resume the conversion process without a reset.

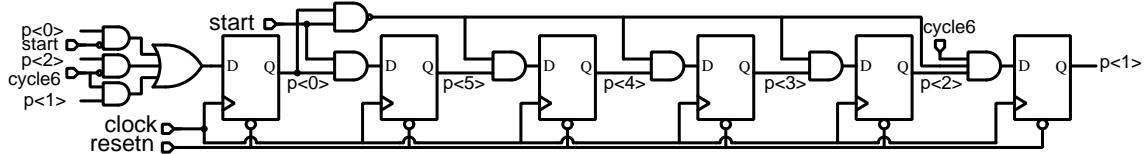


Figure 3.34 Synchronous sequencer to force decision in case of metastability

comparator clock generation: To relax constraints on the comparator, asynchronism is introduced in the clock generation as well as in switches command. Inside the clock generation circuit represented in Figure 3.35, the possibility between a synchronous and a generated clock is allowed with the clock mixer. For the sake of implementation, the delay of the inverter at the data input of the DFF shall be long enough to prevent a hold violation.

In a fully synchronous design, the comparator makes decision on falling edge of the primary clock, whereas in a pseudo-synchronous design the reset of comparators is triggered $T_{nor} + T_{dff} + T_{mux}$ after a decision have been made. This allows a nor-rs-latch to store the result of comparison for the full clock cycle.

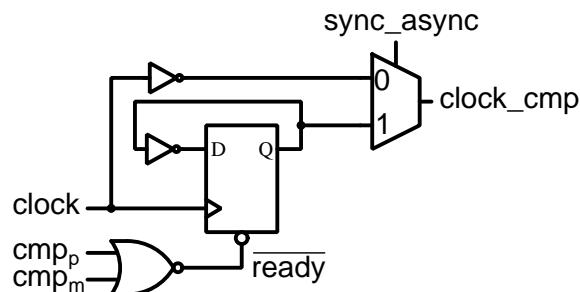


Figure 3.35 Comparator clock generation to select a pseudo-synchronous operation or fully synchronous behaviour

3.2 Sub-ADC Analysis

For cmos cross-coupled inverter based latches, the reset phase can consume as much energy as during the decision-making stage. The modification does not improve the power consumption. Nevertheless the redundancy being an intrinsic property of the DAC, a settling error is corrected by following clock cycles. The redundancy allows to trigger the comparator earlier, while the settling is not complete.

switches design: For the selected digital scheme, switches shall connect the input voltages during the sampling clock cycle. Then each capacitor weight is tested from the most significant weight to the least significant one. This is done by connecting $+V_{ref}$ ($V_{refp} - V_{refm}$) on capacitors whose weight is not being under test and to the others $-V_{ref}$ ($V_{refm} - V_{refp}$).

Not to introduce a settling error the positive reference voltage is connected to capacitors via low-vt pmos transistors, the negative reference voltage by low-vt nmos transistors, and the input via transmission gates whose pmos is 3.5 times bigger than nmos. In addition to that, only one switch is active at a time: the transmission gate only during the sampling clock cycle, and then either the pmos or the nmos.

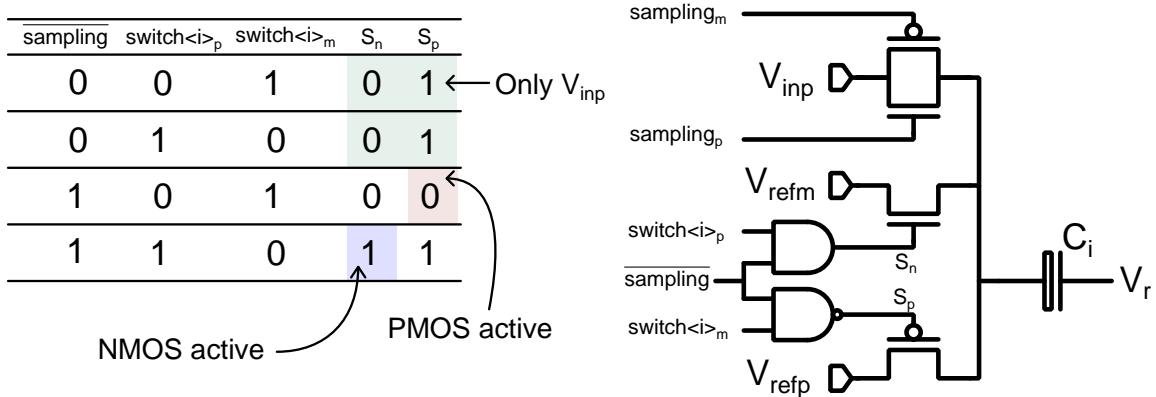


Figure 3.36 The switches signal command to connect only one voltage at a time of the connected capacitor

As represented in Figure 3.36, the 4 wires are present. S_n and S_p are generated from a common signal and the complementary of sampling. The truth table on highlights which switch is active to ensure that only one is active.

The common signal is thus a predefined waveform which is set to one for the sampling clock cycle, reset to zero for the clock cycle to test the capacitor connected to the switch, and then set to the result of the comparison made by the comparator. The generation of each signal follows the same pattern depicted by Figure 3.37.

This SAR has the purpose to extract final bits in the conversion for an insignificant fraction of the ADC power consumption. In the analogue domain, the capacitance of the DAC has been reduced by the employ of a split-DAC technique. The energy consumption can be further scaled

A new mixed ADC topology

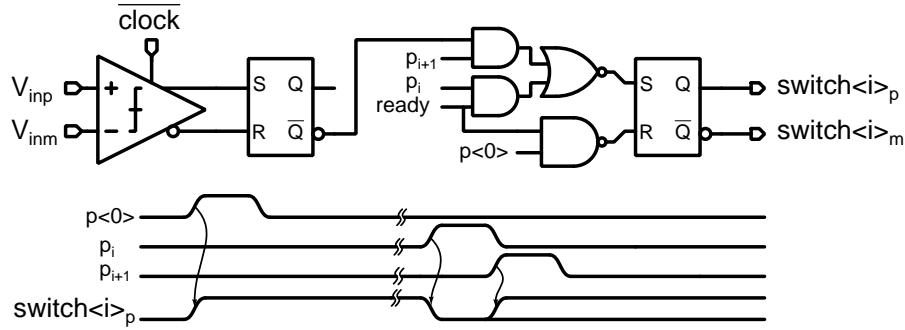


Figure 3.37 Switches signal command based on the decision of the comparator

down by changing the digital switching scheme at a price of a common-mode voltage variation, in turn impacting the comparator.

Considering, the possible error in the decision and variation in the DAC due to manufacturing, a redundancy is introduced. The redundancy is helpful to reach higher sampling rates with a slow comparator. Unfortunately, the redundancy does not reduce the latch metastability and its repercussion on the digital. Henceforth, a pseudo-asynchronous digital gives a margin to reduce the probability of a metastable event.

So far, the design of each stage is independent of each other and assumption on the amplifiers are numerous. Simulations of the ADC thus follow.

3.3 Simulation Results

By design the first stage integrates over 4 clock cycles with a 1.5-bit quantizer. The resulting output code having 8 steps in its sub-ADC transfer function, we expected this stage to behave as a 3-bit sub-ADC. In turn, the second stage performs the conversion of the first stage residue over 5 clock cycles. As the last clock cycle output bits are re-used to be the two first bits of the SAR, the second stage provides only 4 bits while the SAR gives 6 bits. However, the scale of the SAR has been tuned to a non binary ratio to trade accuracy for robustness. All these modifications result in a 3+4+5.3 bits ADC. In theory, the ADC should provide 12.3-bits, and as there is no interstage gain between the algorithmic and the SAR, the true maximum value is 11.3-bits. For a 6-clock cycle mode, the resulting maximum resolution is 13.6-bits.

In a first start, we have simulated the ADC using MATLAB simulations. With the assumption of ideal amplifiers, we confirm the limits given in the previous paragraph. In the MATLAB post-processing, a function has been defined for each stage which returns the output code and the residue. In a first step, we estimate/reconstruct the transfer function from the ideal bit coefficients. By comparing the ideal transfer function ($V_{out} = V_{in}$) with the one obtained by simulation, we de-

duce the total error in the conversion process. This error should be limited to $\pm \text{LSB}/2$, whatsoever the condition is.

Then, we moved to high-level spice simulations. The latter considers switches at the transistor level and use the capacitors of the technology taking into account voltage non-linearity. To a first attempt, the amplifiers are defined in a verilog-a model to take into account the slew-rate, the finite gain and the limited gain-bandwidth-product.

This section discusses the results of the architecture on some particular strategy chosen with respect to the resilience. Then, the Static performance of the ADC is presented.

3.3.1 Algorithmic Feedback

For the design of the FA-MDAC, the feedback coefficient can utterly affect the error made by this switched capacitor structure. The error optimization leads us to the solution of in Section 3.2.2.1 where the feedback factor $f = 1.2$ to generate an output range of $\pm 0.6 V_{\text{ref}}$ with thresholds of $\pm 0.3 V_{\text{ref}}$. Despite this fact, the traditional implementations consider a unit feedback factor with threshold voltages of $\pm 0.25 V_{\text{ref}}$. The question is thus twofold: what is the resolution improvement over the traditional implementation in the ADC? and How does each cope with the temperature?

To evaluate the advantage of one set of parameter to the other we set up the parameters for the OTA model listed in Table 3.3.

Table 3.3 OTA configuration for the test

Verilog-A model ahdllib	value
Dc Gain [dB]	70
Unity Gain Frequency [MHz]	750
$C_{\text{Load}} = 250 fF$	
Input Impedance [Ω]	100 Meg
Input Offset [mV]	0 – 50
Maximum Current [mA]	1
Output Impedance [Ω]	110
Output Voltage Range [V]	0.4 – 1.4

Those parameters are sufficient for a 11.8-bits accuracy over the full input range, and thus neglecting the slewing effect on the capacitive load of 250 fF as the maximum current to charging 1 V in 1 ns on such a load is 250 μA .

Figure 3.38 represents the transfer function and the residue of each stage: from the left to the right, the stages are respectively the $I\Delta\Sigma$, the Algorithmic, and the SAR. The SAR does not give any residue and therefore, in-place, the error between the ideal transfer function and the current transfer function is represented. The error is compared to the closed binary resolution LSB in solid

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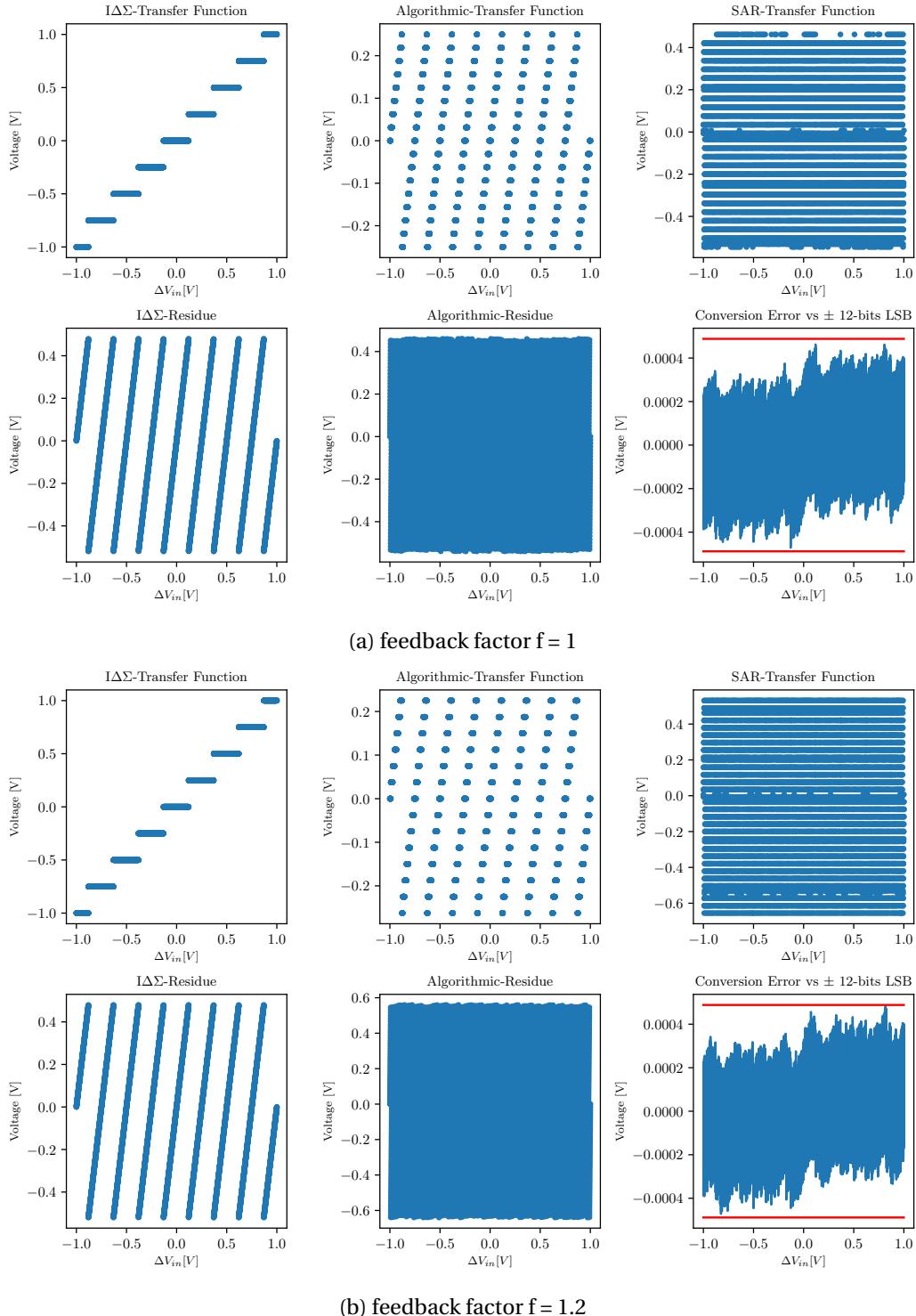


Figure 3.38 Sub-ADCs transfer function and its residue underneath and the ADC transfer function error at 300 K. Plots obtained for 8192 different input voltages from -1 V to +1 V

3.3 Simulation Results

red lines. For the results of a conversion performed in 5 clock cycles, the limits are $\pm \text{LSB}/2$ of a 11-bits ADC. In a nutshell, the error committed by a feedback factor $f=1.2$ is greater than the error for a feedback factor $f=1$ by $20 \mu\text{V}$ at 300 K. The performance is equivalent to respectively 11.06-bits and 11.03-bits ADC while we are expecting 11.3-bits.

Using the real OTA designed in Section 4.3.3 at 475 K, the feedback has a deeper impact. The OTA modelization has an input capacitance, a second pole with a phase margin altered by the temperature, a gain and a speed variation over the temperature range. Figure 3.39 exposes the error in the conversion process at high temperature. To the contrary of expected results, a greater feedback factor has an increased temperature sensitivity. A greater spikes at $\pm 0.8 \text{ V}$ are displayed in part due to a greater voltage dependence of feedback capacitors having more weight and extra parasitics of switches needed. This results in a loss of 122 steps corresponding to a 11.15-bits rather than the 11.07-bits at high temperature.

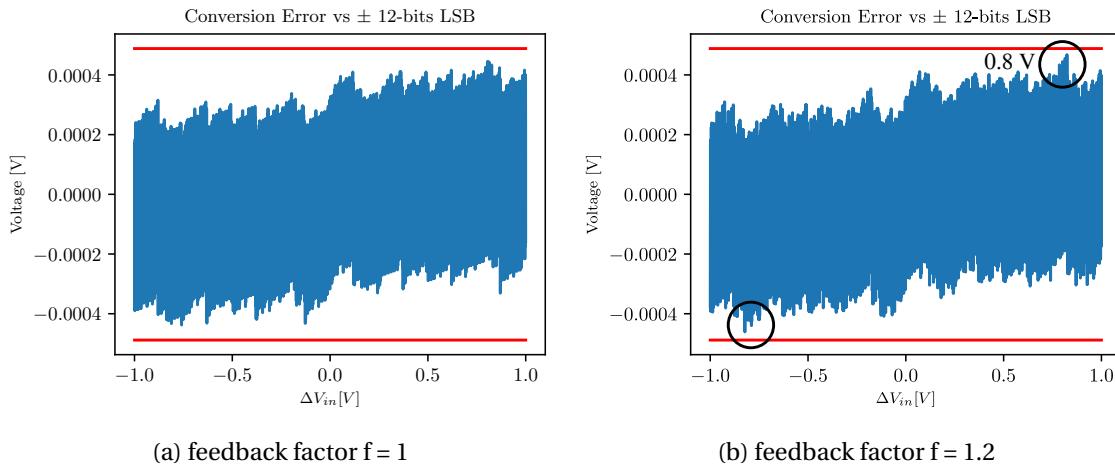


Figure 3.39 ADC transfer function error at 475 K for 8192 different input voltages from -1 V to +1 V

In consequence, the feedback factor selected is 1. Despite having a greater error on the Sub-ADC residue, since this extra error on the residue does not exceed the LSB of the SAR and extra components are removed, the final error is less sensitive to analog defects. Removing extra capacitors and switches for the feedback ratio, the area also shrinks. The estimated area saving is twice $50\mu\text{m} \times 8\mu\text{m}$.

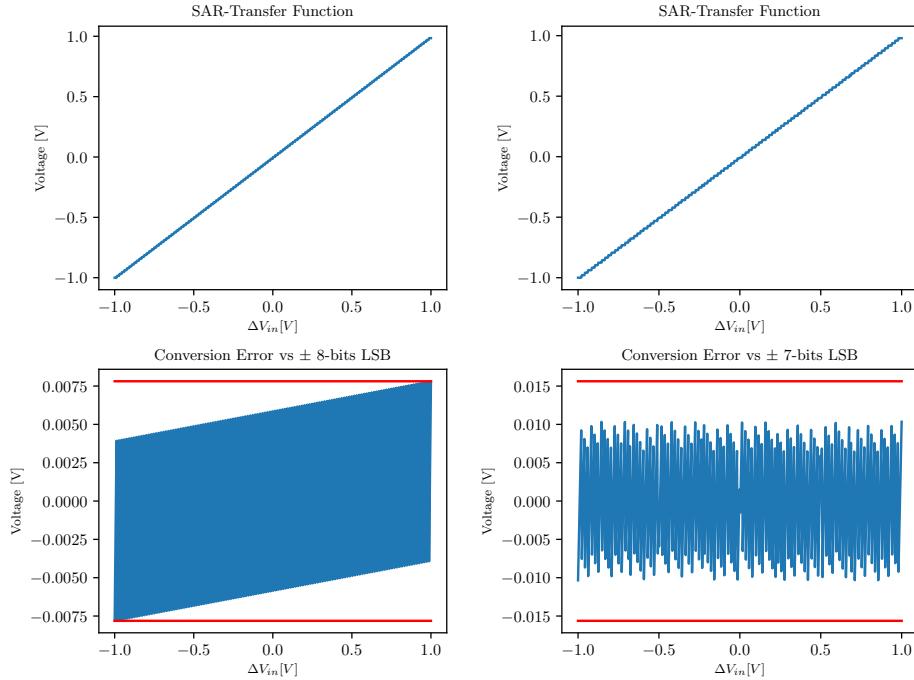
3.3.2 SAR resilience

By design, we have tuned the scale of the capacitive DAC to cope with comparators offset and voltage references alterations. By using a split-capacitor DAC, the adjustment consists of rounding the attenuation capacitor to the closest multiple integer of the unit capacitor. Of course, we decrease the effective number of bits of this stage, but to keep it even under large voltage and

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process variations. As the second stage gives the two first bits of the SAR, threshold errors on the second stage comparators also undermine the conversion of this stage.

In order to compare, Figure 3.41 represents side by side the transfer function and the error for binary scale and the designed one. These are presented in ideal conditions (no threshold voltages error and without comparator offset) and with a 40 mV error on threshold voltages and 10 mV offset.



(a) 421-8/7-4211 ideal references and offset (b) 632-3-4211 ideal references and offset

Figure 3.40 Comparison of ideal binary scale and proposed scale for ideal conditions

As expected, the designed version exhibits an error of 10 mV for an OSR equal to 6 whereas the ideal binary scale has an error not exceeding 7.5 mV. The equivalent resolution is therefore 6.64-bits instead of 7-bits. By adding inaccuracy, the resolution drops from 7 bits in an ideal case to 5.32-bits in the 421-8/7-4211 configuration. However, the 632-3-4211 configuration preserves the resolution, even for 10mV offset and 40mV on threshold voltages: at the exception of the last code the error range is conserved. Otherwise, the resolution is 6-bits.

In consequence, the proposed DAC scale is easier to implement, ensure better process variation, and reduce the resolution drop under possible PVT inaccuracy.

3.3 Simulation Results

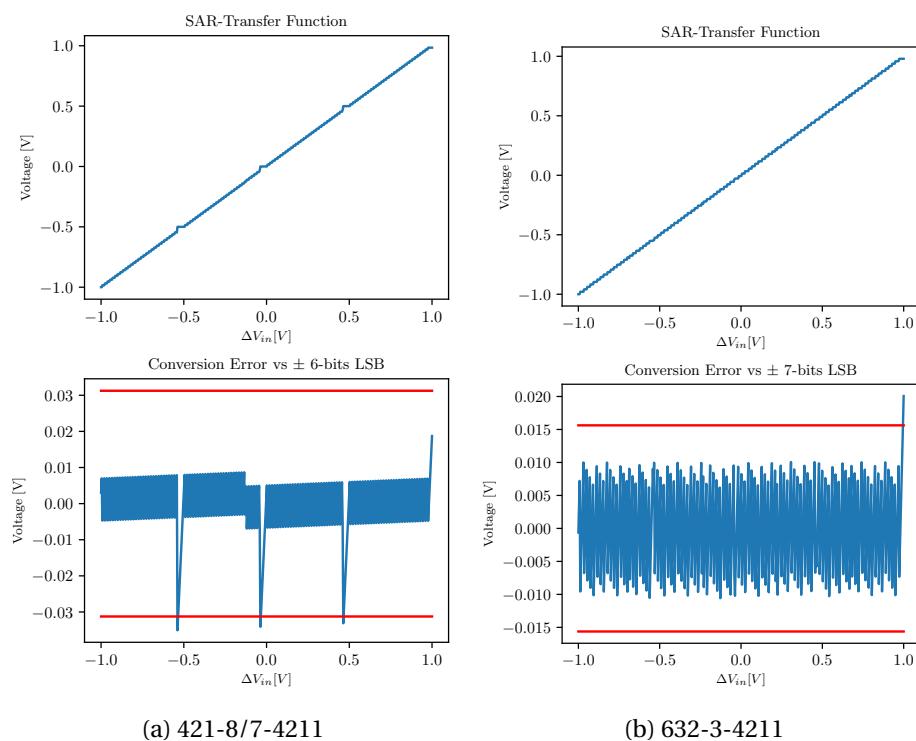


Figure 3.41 Comparison of ideal binary scale and proposed scale for large variations of reference voltage and offset: 40 mV error on references and 10 mV offset

3.3.3 ADC static performance

As aforementioned, this part will collect simulation results about a variation of the amplifier DC gain, and the unity gain frequency variations to deduce the sensitivity of the ADC architecture. To reflect the true performance, we did not apply any calibration coefficients.

Let's first consider the sensitivity of the ADC with an oversampling ratio of 5 clock cycles. As earlier explained, the maximum resolution is calculated to be 11.3-bits.

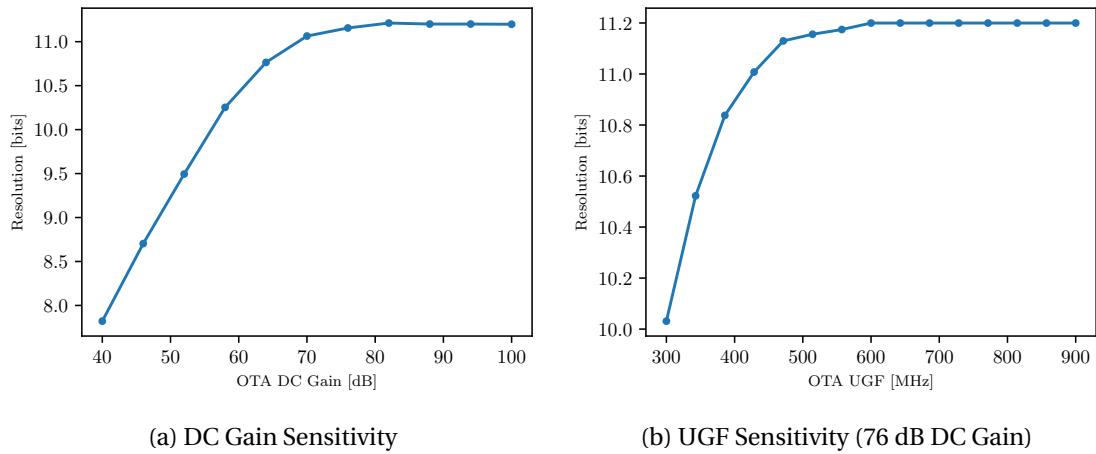


Figure 3.42 DC Gain and Unity Gain Frequency Sensitivity of the ADC for an OSR = 5

The DC Gain sensitivity of the ADC is depicted by the Figure 3.42a for a Unity Gain Frequency of 800 MHz. The resolution admits a limit of 11.2-bits at the transistor level for OTA DC Gain greater than 76 dB. This can be explained by the fact the minimal DC Gain of the OTA shall be 62 dB is not sufficient due to the UGF limitation. Then, the DC Gain error is decreasing to let the UGF limitation the dominating factor. Finally, the Error is dominated UGF and increasing the DC Gain is no more relevant. That said, Figure 3.42b highlights for a DC Gain of 80 dB the minimal Unity Gain Frequency. In our case, the minimum UGF is 6 times the clock frequency.

In the same manner, we replicate the analysis for the ADC with an OSR = 6. The result in Figure 3.43 demonstrates for a UGF 8 times the clock frequency that the gain to reach 13.8-bits is at minimum 100 dB. For a more reasonable improvement compared to its 5-clock cycle counterpart, with a gain of 80 dB and a 600 MHz of Unity Gain Frequency, the reachable resolution is 13.45-bits.

Therefore, based on this high-level spice simulation, we deduce the minimum performances of the OTA without slewing. Keeping these values, we set the Gain to 80 dB and the Unity-Gain-Frequency to 600 MHz. Without offset we get a resolution of 11.25-bits and 13.48-bits for respectively an oversampling ratio of 5 and 6.

Then, we force an offset of 40 mV on the $\text{I}\Delta\Sigma$ and the Algorithmic stage, while on the SAR we introduce an offset on the comparator of 10 mV. Figure 3.44 represents the conversion error once

3.3 Simulation Results

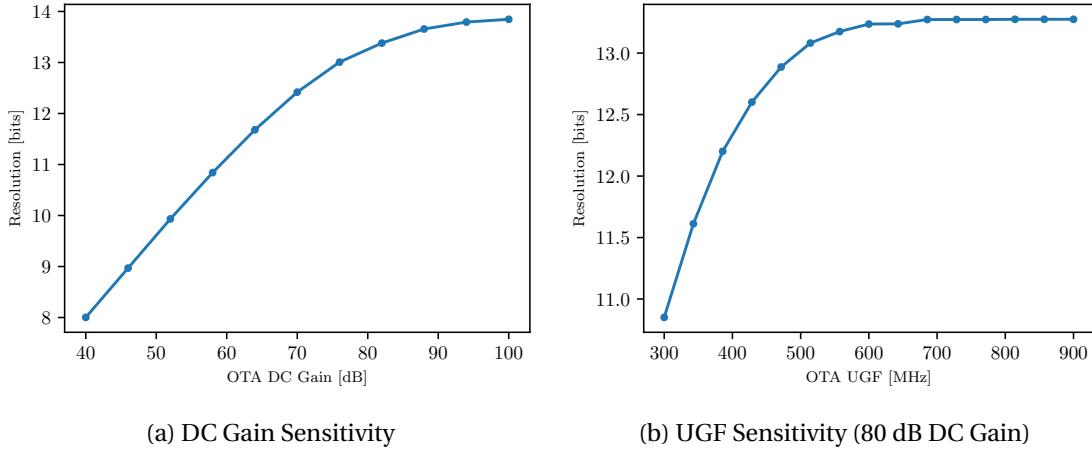


Figure 3.43 DC Gain and Unity Gain Frequency Sensitivity of the ADC for an OSR = 6

the estimation of the offset by averaging output codes is subtracted. Compared errors without offset introduction, the error exhibits a positive slope with respect to the input voltage, but is still in the expected resolution limits.

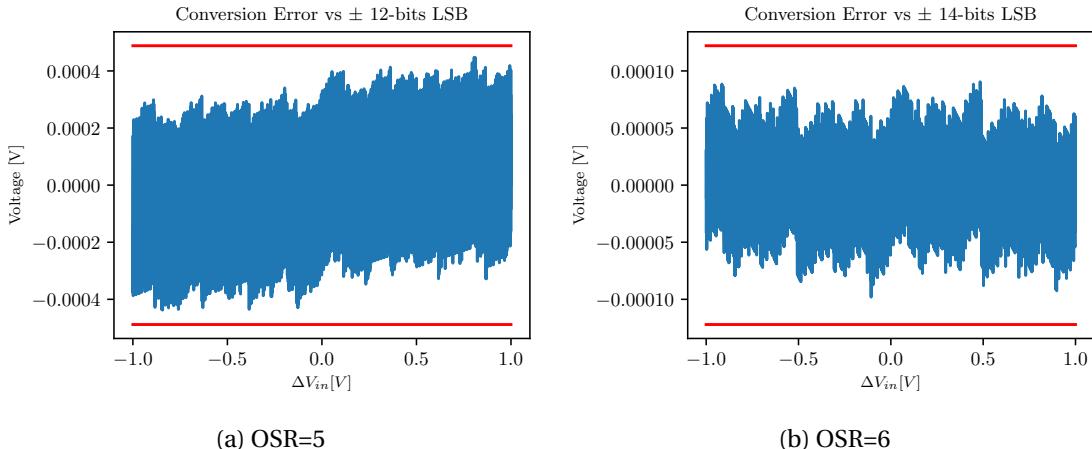


Figure 3.44 Conversion error after offset removing by subtracting the average of codes for an OSR=5 and OSR=6 with 40 mV offset on first stages and 10 mV on the last

For an OSR=5, we also represent the Differential Non-Linearity (DNL) and the Integral-Non-Linearity (INL) of the ADC in Figure 3.45. The expected resolution is 11.3-bits. So far, we were able to extract the error for an ideal reconstruction of the transfer function which is steps of binary words weighted by real values. As the number of bits produced exceed twelve, we can consider the weighted output code to be ideal. In case we quantize the weighted output code to a 12-bits one, the length of the steps and the error are affected. So, we quantize the weighted output code to twelve bits and look at non-linearities of the ADC. Either with offsets or without offset, the

A new mixed ADC topology

non linearity does not exceed a 11-bits LSB. And this with only an offset correction based on the averaging of the output codes.

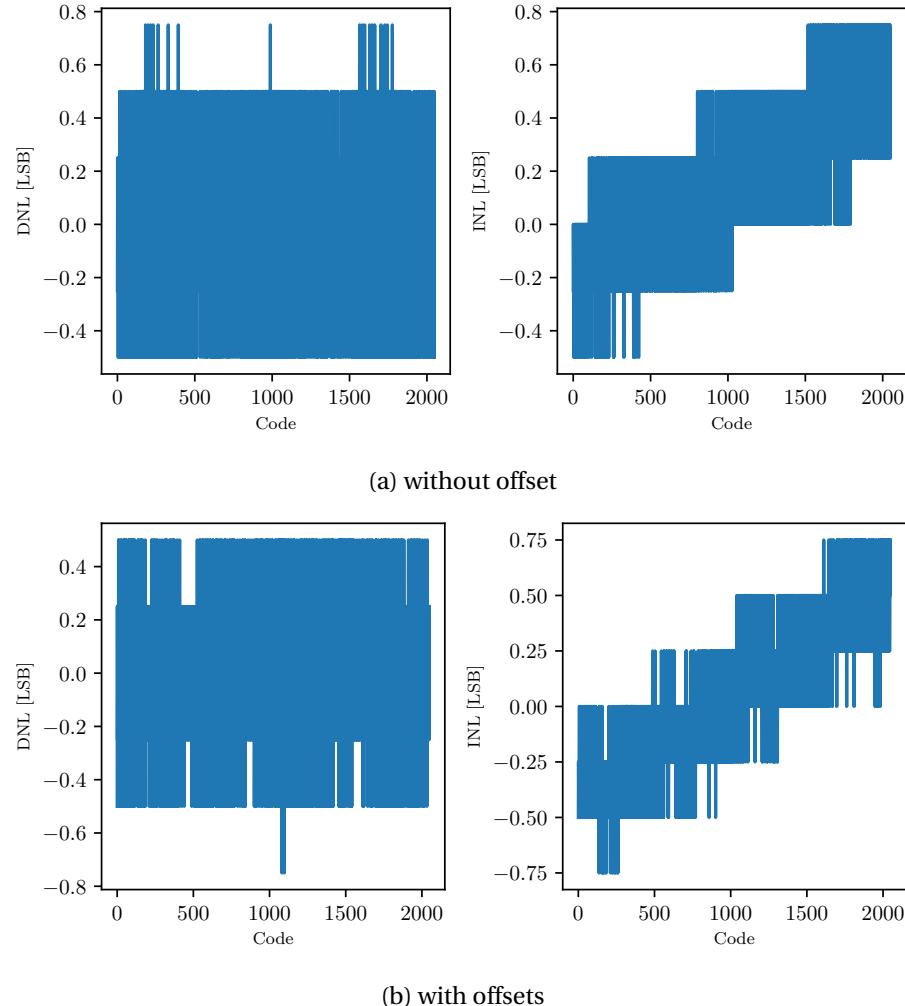


Figure 3.45 DNL and INL of the proposed converter under large offsets of 40 mV on first stages and 10 mV on the last

3.3 Simulation Results

From simulations, we deduce the specifications for key analogue blocks. In the case of the OTA, these are listed in Table 3.4 while for the comparator, they are in Table 3.5.

Table 3.4 OTA specification for a calibration free ADC

OTA	
Temperature [°C]	-40 – 175
DC Gain [dB]	>80
Unity Gain Frequency [MHz]	>600
Input Offset [mV]	<50
Phase Margin [deg]	>50
Output Current [μ A]	<400
Output Voltage Range [V]	0.6 – 1.3
Average Power [mW]	<5

Table 3.5 Comparator specification for a calibration of only the offset ADC

	Comparator ($I\Delta\Sigma$)	Comparator (Algorithmic)	Comparator (SAR)
Temperature [°C]	-40 – 175	-40 – 175	-40 – 175
Resolution [mV]	<25	<50	6
Delay [ns]	<2.5	<2.5	<7
Input Offset [mV]	<50	<50	<10
Hysteresis [mV]	<1	<1	<2
Differential Kickback [mV]	to be minimum	to be minimum	to be minimum
Average Power [μ W]	to be minimum	to be minimum	to be minimum

For the ADC, high-level simulations with verilog-a model of the OTA and comparators estimate static metrics over the temperature range. The resolution variation highly depends on the OTA variation of the settling error. The differential non-linearity depicts no-missing code for respectively 11-bits LSB and 13-bits LSB for an OSR=5 and OSR=6.

Table 3.6 ADC static results with real OTA and only offset calibration

	OSR = 5		OSR = 6	
	min	max	min	max
Temperature [°C]	-40	175	-40	175
Resolution [bits]	11.25	11.4	13.45	13.9
F_{snyq} [MHz]	10	-	8.33	-
DNL [LSB]	-0.5	0.5	-0.5	0.5
INL [LSB]	-0.5	0.78	0.23	1.5

It is important to notice that in OSR=6, a gain error is introduced in the transfer function shifting the INL. With a gain correction the INL is kept in the -LSB/2 – LSB/2 range.

ANALOG BUILDING BLOCS

In this section, we will discuss in detail the key building blocks of most ADC. Among them, comparators and amplifiers are the most common source of performance limitation. A review of existing comparators and amplifiers is followed by a comparison of most common architecture over temperature. Then, the design of the best candidates is discussed.

4.1 Prior Art

4.1.1 Latches and Comparators

In the design of ADC, comparators and latches are usually designed to output a logic level indicating the position of the differential input voltage to a non-zero threshold voltage. Implemented as a fully differential balanced circuit, the sensitivity to mismatch, supply noise, charge injection is utterly diminished. The comparator should thus have four inputs. However, by dividing the comparison operation in two steps, it is possible to transform a comparison to any reference level into a signal polarity detection.

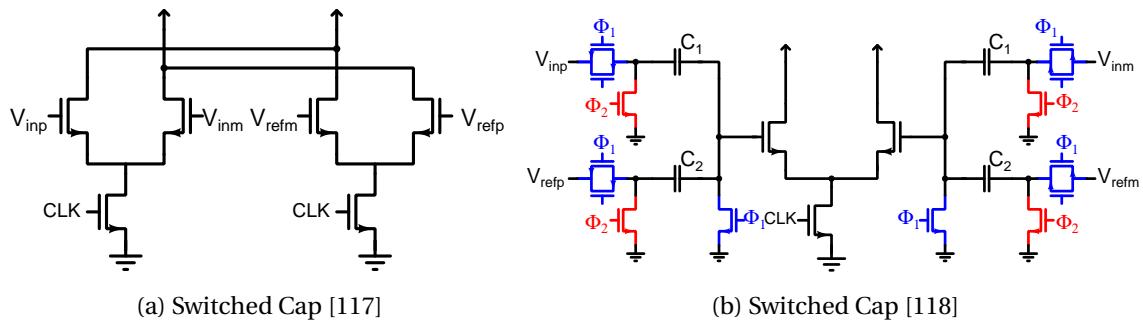


Figure 4.1 Analog subtraction for differential voltage comparison

The analog subtraction can be done using two differential pairs as shown in Figure 4.1a [117]. This one-step solution introduces an offset coming from the mismatches between the two input differential pairs. The threshold level is thus fixed by the ratio of differential pair transistors creating a dependence between the offset and the reference voltage applied.

In a charge domain, the subtraction can be implemented as in Figure 4.1b taken from [118]. The threshold voltage is now fixed by the capacitor ratio C_1/C_2 and improves the reference voltage dependence of the offset. Nevertheless, the gain introduced as $C_1/(C_1 + C_2)$ effectively makes the offset and noise of the comparator greater with respect to the input signal. If the comparator offset

Analog Building Blocs

and noise are limiting constraints, the input signal attenuation caused by the previous architecture may not be tolerable. The circuit shown in Figure 4.2, introduced by Abo and Gray in [119], avoids this problem. One would rather prefer to change to virtual ground between C_2 capacitors to a proper connection to the ground to enhance reliability.

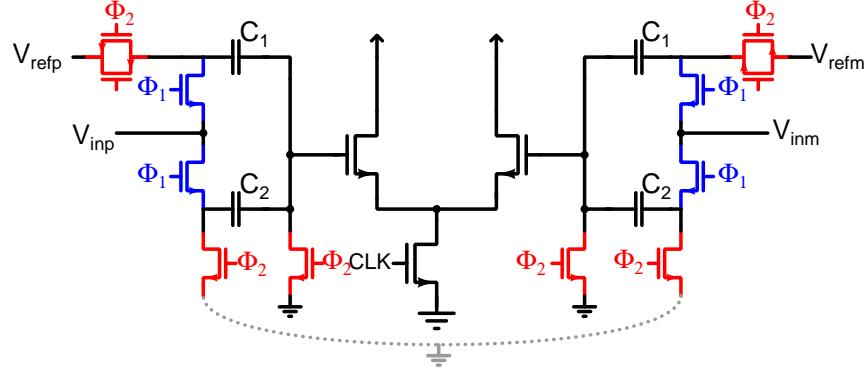


Figure 4.2 Abo implementation of the analog subtraction to prevent voltage compression

The polarity of the analog subtraction output is then reused by digital logic to perform the conversion. Comparators could be evaluated in different ways, depending on the application. The most generally used figures of merit are probably resolution, followed possibly by delay (speed) and offset. The most important ones from our point of view are listed below:

- Resolution
- Delay
- Input Referred Offset
- Noise
- Kickback
- Metastability
- Power consumption
- Hysteresis

The resolution of a comparator is the minimum difference between the input signals that can be detected. Closely related to the gain of the input stage of a comparator, a comparator is conceptually a high-gain differential amplifier that saturates to the supply rails, or to some other levels. Therefore a high gain amplifier is a first candidate. In the case of closed-loop amplifier that use positive feedback, the comparison time is involved. The system has two stable points and will follow a trajectory to either one depending on the initial condition. More time is allotted into latching to either state, more sensitive the comparator will be.

Open-loop wideband amplifiers have the desirable feature of high initial speed, but suffer from limited resolution and potentially troublesome offset voltage. Latches and positive feedback increase the gain and allow faster decisions. Unfortunately, The first inherent flaw is the rising exponential behaviour: the gain is low if the input signal (or the initial condition) is small. The second drawback is related to the practical realization of a latch. Since the objective is to maximize dynamic gain, one should maximize speed by minimizing capacitance. This is done by using small

transistors, which also helps reduce power consumption. However, the mismatch worsens as the devices become smaller, thus fast latches exhibit relatively large input offsets. This drawback hinders the use of latches as comparators for analog to digital conversion. The best solution is to cascade an open-loop amplifier and a latch. In this way, the overall gain can be distributed over two stages. The first stage has the most dynamic gain near the origin, and outputs a voltage that sets the initial condition of the second stage away from its zero gain region, speeding it up.

4.1.1.1 Current Mode Latches

The earliest comparator circuits using the cascading of a pre-amplifier and a latch were used in current-mode logic (CML) circuits. The first current mode latch was presented by Yamashina et al in a current control logic for processors [120]. The principle of CML is to use of a differential pair loaded by resistances to amplify the difference between the inputs. The differential output sets the starting voltage of a regenerative amplifier stage. Both stages are biased by constant current sinks, which are switched on and off to reduce the power dissipation. Some examples of CMOS CML can be found in the work of Usama and Kwasniewski [121]. The power consumption of CML CMOS comparators can be reduced down to about $182 \mu\text{W}$ in a $0.13 \mu\text{m}$ CMOS technology [122]. These comparators can reach the fastest possible speed, at the expense of large power dissipation. They are typically found in GHz-level serial links where Inter Symbol Interference is a key concern. Nonetheless, they are an example of combining two stages, one linear and one regenerative, to obtain the best performance.

4.1.1.2 Single Stage Latches

Cross-coupled CMOS inverters work as a regenerative amplifier with fully restored logic outputs. Another advantage is that it does not draw any static current and scales well with nanometre technology. The major issue is the offset [123]. Several examples can be found in the study released by Stojanovic and Oklobdzija [124]. With a first use in an ADC by Yukawa and Fujita in 1985 [125] whose offset (one standard deviation) is reported to be less than 3 mV without any offset cancelling technique. Nevertheless, it consumes power as long as the input common mode is held in the range where both PMOS and NMOS transistors are conducting. Another impairment is the fact that the memory of the previous state directly influences the comparison threshold as well as both the threshold voltage and the transconductance and the mismatch in the capacitive loads [126].

Based on it, comparators found in [117, 118], and presented earlier for the analog subtraction, are a derivation of a widely used single-stage latched comparator: the Strong-Arm latch.

Introduced by Kobayashi for a memory cell [127], a major reliability issue is floating nodes above the transistors of the differential pair as represented in Figure 4.3. The transistor M10 was introduced in [128] to solve a floating node problem that occurs if the differential input

voltage reverses polarity after the decision has been taken. One can also introduce additional reset transistors to remove any memory of previous decisions in all internal nodes as in [129].

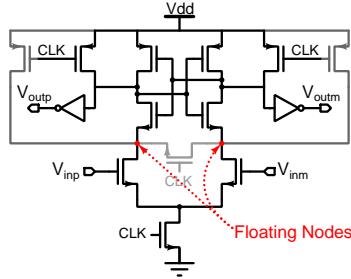


Figure 4.3 Floating Nodes of a conventional Strong-Arm latches and method to circumvent from [128] and [129]

4.1.1.3 Two-Stage Latches

Single stage latched comparators are fast and consume little power. However, they tend to be noisy, to have large offset and kickback noise. To address these problems, a more common practice is to use a pre-amplification stage. Moreover, at low-voltage operation the 4-transistor stack of a StrongArm latch reduces the headroom of the input pair transistors.

In 2006, Chen and Brodersen added reset switches in both the pre-amplifier and latch stage to reduce the comparator recovery time during the reset phase [130]. Reset transistors of the pre-amplifier are also used for input offset cancellation technique. In addition, current mirror between the two stages are useful to reduce charge kickback from the logic level swing of the latch [131]. This technique decreases the offset and the hysteresis. Proposed in a SAR ADC realized in $0.13 \mu\text{m}$, the 6-bit ADC performs at 600MS/s [130] while the analog core consumes 1.2 mW. Yet, the current consumption is more important than CML latch since a large transient current runs through the latch at the beginning of a decision while the pre-amplifier consumes a static current over the full clock period.

To be energy-efficient a comparator can also have a pre-amplifier that is efficient too. Van Elzakker base his comparator on a recent structure introduced by Schinkel [132, 134]. Compared to the previous architecture, the double tail has less stacked transistors in order to operate even at very low voltage. Figure 4.4 represents the different variations around the double tail architecture. The main change noticed is the choice of the second stage. The speed can be further increased by the introduction of a positive feedback inside the pre-amplifier as in [131, 137] at the price of an extra kickback. The dynamic pre-amplification proves to be efficient as in [133] with a supply voltage of 1 V and a clock at 1 GHz, the estimated power consumption is around $17 \mu\text{W}$.

An overall comparison of comparators is presented in Table 4.1.

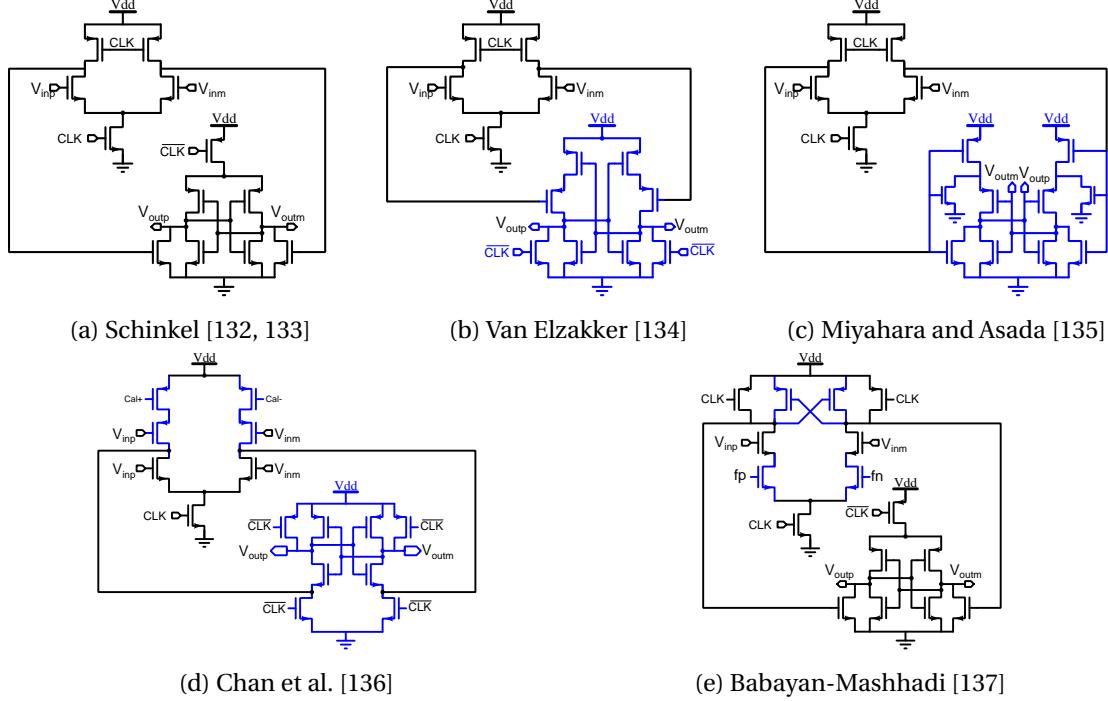


Figure 4.4 Usual variations of the double tail comparator over its original version

Table 4.1 Comparators Performances

Ref.	Architecture	Technology [nm]	Delay [ps]	σ_{Offset} [mV]	Supply [V]	Power [μ W]	Res./Load [mV/pF]	
[117]	Strong Arm	500	Bulk CMOS	<5000	10	3	837	NC/20
[120]	CML	NA	Bulk CMOS	200	NA	1.2	1000	200/NC
[121]	CML	180	Bulk CMOS	112	NA	1.2	275	1200/2
[122]	CML	130	Bulk CMOS	66	NA	1.2	182	1200/NC
[124]	Strong Arm	180	Bulk CMOS	175	NA	1.8	31	1800/0.2
[125]	Two-Stage	1200	Bulk CMOS	7000	2	NA	1300	10/NC
[129]	Strong Arm	90	Bulk CMOS	<570	27	1	32	25/NC
[132]	Double Tail	90	Bulk CMOS	165	9	1.2	225	10/NC
[133]	Double Tail	90	Bulk CMOS	142	NA	1	17	1000/NC
[134]	Double Tail	65	Bulk CMOS	1300	NA	1	0.06	2/NC
[135]	Double Tail	90	Bulk CMOS	122	13	1	40	1/NC
[137]	Double Tail	180	Bulk CMOS	800	8	0.8	576	5/NC

4.1.2 Amplifiers

Switched capacitor analog is proven first-class candidate for critical analog function implementation in mixed-signal systems. Fully compatible with modern digital cmos they required amplifiers, capacitors, and clocked switches.

Amplifiers role in high-accuracy system is twofold: either in delta charge flow or in charge transfer implementation the amplifier preserves the charge stored on a capacitor and maintain the signal, and in a charge transfer implementation they also are responsible for moving charges from one capacitor into another.

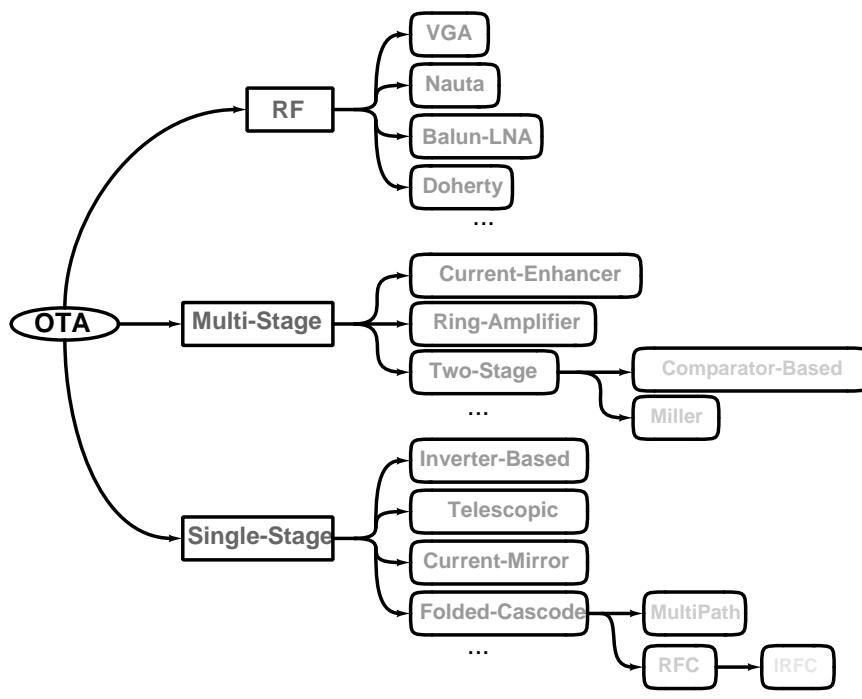


Figure 4.5 Family tree of common amplifiers architecture

Depending on the applications many amplifier topologies have emerged. A non-exhaustive list of common topologies is, in Figure 4.5, grouped under three categories: RF, Single Stage, and MultiStage.

Focused on a high gain and high speed amplifiers, all amplifiers for RF communications are not suited for the conception of an ADC. Indeed, they reach with difficulty 20 dB of DC Gain and are power hungry [138, 139].

The analog design insight over temperature in Section 2.2.2 highlight the difficulty to achieve a stable high-gain over temperature and a high speed amplifier based on a single transistor performance. Therefore, high-gain amplifier usually use either cascode and multi-stage architectures [140]. In a multi-stage amplifier each stage contributes at its simplest form as an extra pole

and an extra zero. In this regard, to ensure the Barkhausen stability criterion, phase compensation schemes are required to obtain a good phase margin. To the contrary high bandwidth amplifiers use a single-stage architecture, high bias current and short channel devices.

Among single stage amplifiers, inverter based amplifier are often used in ADC and well-reputed for their low-power consumption [141, 142]. Nevertheless, limited bandwidth and the biasing of transistors based on the change of the supply voltage are not suited for a high speed ADC in an automotive environment. To reduce the power consumption of amplifiers and reduce analog design constraint, the one could implement a continuous-time comparator with a push-pull stage as a comparator based ADC. This has been discussed in [143], to build a 10 bits pipelined ADC whose power consumption is 2.5 mW at 7.9 MSamples/s in 0.18 μm CMOS technology. Nevertheless, this comes at a cost of an increased complexity in the digital switching more sensitive to jitter.

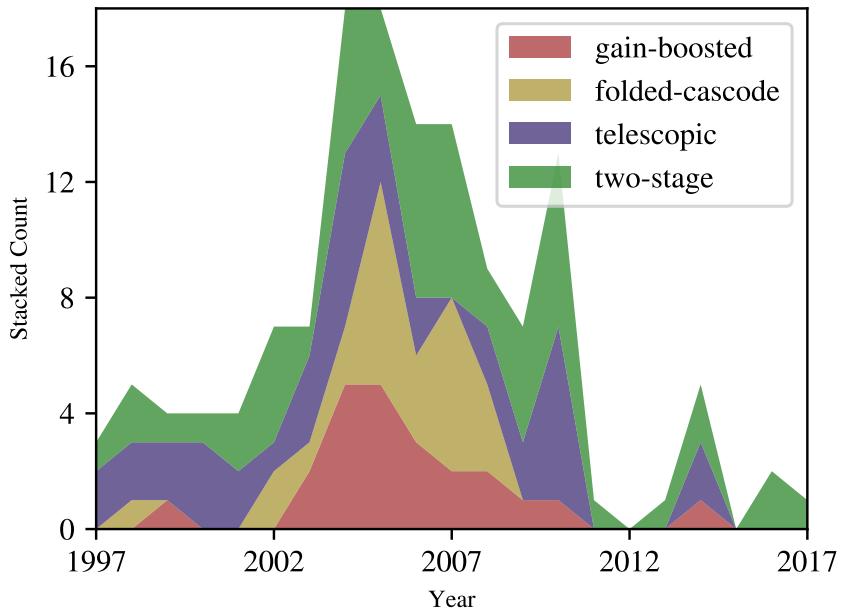


Figure 4.6 Repartition for $\Delta\Sigma$ and Pipelined over Years 1997-2017 of ISSCC and VLSI ADCs in [7]

Figure 4.6 represents the repartition over years of usual topologies for technology over 65 nm. For the sake of clarity, only four topologies have been selected. Furthermore, for a given year, the results are stacked such that the total number of publications and the number of publications using one topology is represented. For the 0.18 μm CMOS process, most of the publications have been published between 2001 and 2008. Over this period, the Folded-Cascode (FC), Two-Stage (TS), and Gain-Boosting (GB) were mainstream with a large preference for folded cascode amplifier either alone or followed by a source follower stage to enlarge the output swing.

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Traditionally, folded-cascode OTA have been preferred for high-speed switched capacitor applications [144, 145] because of their high DC gain and GBW. This architecture candidate is proven to operate under low voltage conditions, even for larger process node size: down to 0.7 V [146, 147]. The Telescopic OTA (Tele.) provides better current efficiency, hence consumes less power, but suffers from limited output swing [148]. Such limitation is circumvent by the use of pseudo-differential architecture as in [149].

The Table 4.2 lists some amplifiers used in ADC between 12-bits and 14-bits of resolution.

Table 4.2 OTA Performances

Ref.	Tech. [μ m]	Topology	Gain [dB]	UGF [MHz]	PM [$^{\circ}$]	Load [pF]	Out Swing [V]	Supply [V]	Power [mW]
[146]	0.18	TS (FC+SF ¹)	50	10	80	4	0.5	0.7	0.055
[149]	0.18	Pseudo-Diff Tele. GB	130	NA	70	NA	2^2	1.8	16
[150]	1.6	FC GB	90	116	64	16	4.2	5	52
[151]	0.18	TS	88	250	NA	NA	2^2	1.6	27.4
[152]	0.35	TS	80	1400	62	2	NA	± 1.25	11.5
[153]	0.13	FC GB	85	4750	50	1.6	1.2	1.5	NA
[154]	0.18	Tele. GB	102	1200	NA	0.48	NA	1.8	1.7
[155]	0.18	Buffered TS	81	1500	68	0.5	NA	1.9	22.8

For a 0.18- μ m technology, the Folded Cascode OTA with Gain Boosting or a Telescopic OTA with gain boosting are the best candidates. In order to cope with 10% power supply variations and a large output swing needed, the Folded Cascode OTA with Gain Boosting is preferred. The advantage of this solution is a reduced area overhead compared to a two stage implementation with a greater bandwidth achievable.

Before diving into the design of a complex OTA over temperature, let us start with simpler circuits: the comparators.

¹folded cascode amplifier followed by a source-follower

²Volt peak-peak

4.2 Latch comparator design

4.2.1 Use case

The hybrid pipelined architecture contains an $\text{I}\Delta\Sigma$ stage followed by an algorithmic stage and a SAR stage. In principle, all stages share the same common-mode and reference voltage levels. In addition, the proposed hybrid converter should operate from -40°C up to $+175^\circ\text{C}$. Each one of these stages imposes different constraints on the amplifier and the comparators within.

As a trade-off between output swing, linearity, and gain at a given speed to realize the ADC, some constraints can be relaxed by implementing at least a 1.5-bit encoder for the first two stages. From the review done in Section 4.1.1, a switched capacitor analog subtraction is preferred in this regard for the reduced temperature variation of the capacitor over the current variation of the double differential pair variation.

The incremental and the algorithmic stages are closed-loop converters. Therefore, the only effect of errors introduced by the comparators is to increase the amplitude of the residue passed on to the following stage. Those two first stages are fault tolerant while the comparator errors do not exceed a rather relaxed level of non-correctable error.

From a design point of view, both the strong arm and the double tail comparator do not keep the result from a clock period to another. Therefore, they are followed by an RS-latch in charge of keeping the decision made for the digital circuits. This RS-latch is thus the load seen by the comparator.

4.2.2 Strong Arm Latch vs Double Tail

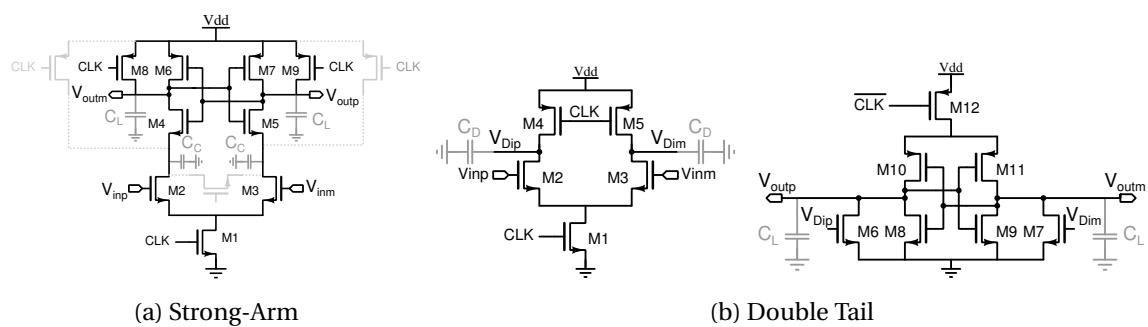


Figure 4.7 Comparators designed for the temperature

The Strong ARM (SA) latch depicted by Figure 4.7a has been chosen for its rail-to-rail output and a quite fast response with small power consumption. The Double-Tail architecture is a promising candidate for low-power, reduced voltage, and scaling.

4.2.2.1 Delay

The detailed operation of the SA latch has been studied thoroughly [156, 157]. In a nutshell, the reset state ($\text{CLK}=0 \text{ V}$) sets the transistors M4-M5 are in deep sub-threshold region, and the outputs are pulled up to V_{DD} by M8-M9. No current flows in the differential pair because M1 is also off. Once the clock is active ($\text{CLK}=V_{DD}$), M1 turns on hard in the linear region, and M2-M3 convert the differential input voltage ΔV_{in} into a current that pull down the voltages at the sources of NMOS devices M4-M5 until they start to conduct. Once V_{outm} or V_{outp} reach $V_{DD} - V_{thp}$, M6-M7 turn on and the cross-coupled inverters regenerates the voltage imbalance $\Delta V_{out}(t_{lin}) = V_{outp}(t_{lin}) - V_{outm}(t_{lin})$. In order to derive t_{lin} , we will assume that the discharge rate is constant as well as C_C and C_L : the total capacitance loads at the sources of M4-M5 and the total capacitance load at the output nodes.

$$t_{lin} = V_{thp} \frac{C_L + C_C}{I_{M2,M3}} \quad (4.1)$$

$$\Delta V_{out}(t_{lin}) = \frac{I_{M3} - I_{M2}}{C_L + C_C} t_{lin} \quad (4.2)$$

The regeneration to fully restored logic values (V_{logic}) denoted by t_{reg} is given by equation (4.3). The total propagation delay of the comparator is then the sum of t_{lin} and t_{reg} .

$$t_{reg} = \frac{C_L}{g_{m4,m5} + g_{m6,m7}} \ln \left(\frac{V_{logic}}{\Delta V_{out}(t_{lin})} \right) \quad (4.3)$$

To reach the maximum speed, transistors in the differential pair and of the current source are biased in strong inversion according to Figure 2.24. With a quadratic model leading to the approximate $g_m/I_d \approx 2/V_{ov}(T)$, the variation of the delay with respect to the temperature can be found to be

$$\frac{1}{t_{lin}} \frac{\partial t_{lin}}{\partial T} = (C_L + C_C) \left[\alpha_{vthp} \left(\frac{g_{m2,m3}}{I_{d2,d3}}(T) - \frac{1}{V_{thp}(T)} \right) + \alpha_\mu \left(\frac{T_0}{T} \right) \right] \quad (4.4)$$

The variation of time spent in the linear phase is thus minimized for a small g_m/I_d and a low- V_{th} transistor. And the delay unconditionally increases in this architecture with the temperature.

Among methods to prevent the floating drain of the differential pair transistor, the solution presented in [128] also affects the speed of the decision as demonstrated in Appendix B.

In comparison, the double tail (DT) comparator [132], shown in Figure 4.7b, is becoming a popular alternative to the SA comparator in the past few years, together with its variations [135, 137, 158]. The key idea is to split the pre-amplification from latch to decouple the constraints, and to increase the voltage headroom. This section develops an original model for the propagation

delay taking into account the current drawn by transistors M6-M7 to improve accuracy of the previous attempted model [137].

Briefly, during the reset phase ($CLK=0V$), the tail transistor M1 is off and transistors M4-M5 are on. The drains of M2-M3 are pulled up to V_{DD} which discharge to the ground the output nodes of the cross-coupled latch thanks to M6-M7. This is possible because M12 is driven by a complementary clock signal. Once the clock toggles to V_{DD} , M4-M5 turn off, M1 turns on and the differential pair M2-M3 discharges the internal nodes V_{Dip} and V_{Dim} to ground, at slightly different rates: $I_{M2,3}/(2C_D)$. Transistor M12 turned on and V_{Dip} and V_{Dim} translated by M6-M7 into a current imbalance at the output nodes, the output voltages are ramping up at a rate of $(I_{M12}/2 - I_{M6,M7})/C_L$. This until the drain voltage of M8-M9 has risen V_{thn} above ground, when one can consider that regeneration takes over and the currents drawn by M6-M7 no longer matter.

t_{lin} is deduced by the equation (4.5)

$$t_{lin} = \frac{C_D}{2C_L} \left(\frac{g_{m6,m7} V_{DD} - I_{M10,M11}}{g_{m6,m7} I_{M2,M3}} + \frac{C_L \sqrt{\xi}}{g_{m6,m7} I_{M2,M3}} \right) \quad (4.5)$$

where

$$\xi = (g_{m6,m7} V_{DD} - I_{M10,M11})^2 + 4V_{thn} \frac{g_{m6,m7} I_{M2,M3} (C_L)}{C_D} \quad (4.6)$$

and $\Delta V_{out}(t_{lin})$ is given by equation (4.7)

$$\Delta V_{out}(t_{lin}) = V_{op} - V_{om} \approx \frac{g_{m6} I_{M2} - g_{m7} I_{M3}}{(C_L) C_D} t_{lin}^2 \quad (4.7)$$

Similarly to the Strong Arm latch, the regeneration time is given by equation (4.8), and the total delay as the sum of (4.5) + (4.8).

$$t_{reg} = \frac{C_L}{g_{m10,m11} + g_{m8,m9}} \ln \left(\frac{V_{logic}}{\Delta V_{out}(t_{lin})} \right) \quad (4.8)$$

The minimization of temperature variation of the delay comes by the minimization of the value $4V_{thn} \frac{C_L^3}{g_{m6,m7} I_{M2,M3} (C_D)}$ and the minimization of the thermal dependence of $\frac{g_{m6,m7} V_{DD} - I_{M10,M11}}{g_{m6,m7} I_{M2,M3}}$. The latter can be minimized for low $\frac{g_m}{I_d}$ of the differential pair transistor and a large voltage overdrive of transistor M6, M7.

4.2.2.2 Input Referred Offset

As explained by Razavi for the Strong-Arm Latch in [157], the dominant contributor to the offset, are the transistors in the differential pair. Exploiting the small-signal model represented in Figure 4.8a, the input referred offset is given by equation (4.9).

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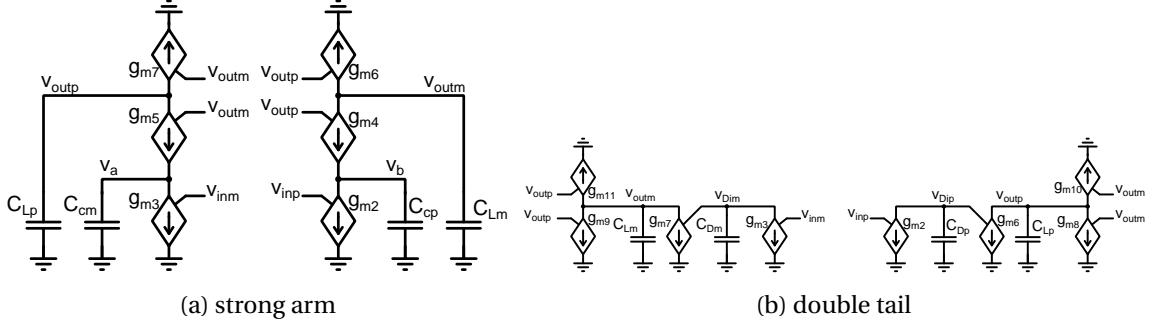


Figure 4.8 Latches Small Signal Models

$$\frac{v_{offset}}{2} \left(\frac{g_{m3}}{1 + s \frac{C_{cm}}{g_{m5}}} + \frac{g_{m2}}{1 + s \frac{C_{cp}}{g_{m4}}} \right) = (g_{m4} + g_{m6} - g_{m5} - g_{m7} - s(C_{Lp} - C_{Lm})) v_{outc} \quad (4.9)$$

$$+ v_{outc} \left(\frac{g_{m5}}{1 + s \frac{C_{cm}}{g_{m5}}} - \frac{g_{m4}}{1 + s \frac{C_{cp}}{g_{m4}}} \right)$$

$$+ v_{inc} \left(\frac{g_{m3}}{1 + s \frac{C_{cm}}{g_{m5}}} - \frac{g_{m2}}{1 + s \frac{C_{cp}}{g_{m4}}} \right)$$

The equation (4.9) fits the explanation given by both [157] and [159]: the output capacitance contributes to the dynamic offset. Both expect a small mismatch for large capacitors due to the proportion of the error committed by a non-ideal manufacturing process over the size of the capacitance. For small capacitance at the output, the offset is greater. In addition, both the input and output common mode voltage have an impact on the offset. The input common mode voltage (V_{inc}) in our converter is already set. And the higher the output common mode voltage (V_{outc}) is, the higher the offset will be.

By the way, the small signal model of the DT latch results in the approximation of (4.10). The offset originates from the mismatch in the same manner it is in the SA latch: a dynamic offset and a static one.

$$-\frac{V_{offset}}{2} \approx V_{outc} \frac{[s(C_{L1} - C_{L2}) + (g_{m1} + g_{m2}) - (g_{m3} + g_{m4})] s(C_{g5} + C_{g6})}{2(g_{m11} + g_{m10})} \quad (4.10)$$

$$+ V_c \frac{[s(C_{g5} - C_{g6}) + (g_{m5} - g_{m6})]}{g_{m11} + g_{m10}}$$

$$+ V_{inc} \frac{g_{m11} - g_{m10}}{g_{m11} + g_{m10}}$$

The DT offset abide the input/output common mode alteration, and with mismatch of parasitics. Thus, both outputs shall be connected to almost similar cells. An RS-latch fits this purpose as it also keep the decision made once the comparator is reset.

4.2.3 Simulation Results

In order to check specific parameters of the comparators designed, a test bench has been set-up to extract the delay, the offset, the hysteresis, the kickback and the power consumption. The test bench represented in Figure 4.9 consists in the generation of a triangle stepped differential input voltage. The output of the RS-latch is thus a window whose edges corresponds to the offsets and their difference is the hysteresis. The time span between the clock rising edge and an edge of this window coincide with the delay of the comparator and of the RS-latch.

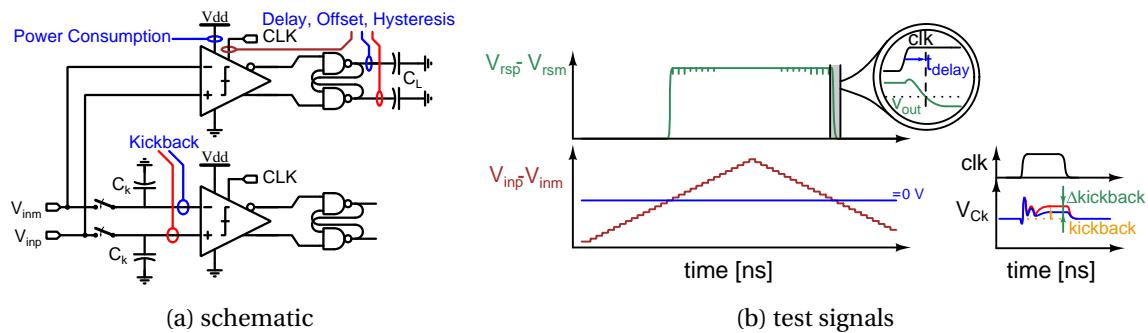


Figure 4.9 Extraction comparators characteristic in spice simulation for fast Monte-Carlo Analysis of simulations

To extract the common mode and the differential kickback, capacitors on the inputs (C_k) are connected to the desired input voltages while the comparator is reset ($CLK=0$ V). When the clock triggers the comparator, switches are already open. The voltage across C_k is sampled before the reset.

Then, the error between the ideal input voltage and the voltages sampled gives us the kickback of the comparator for a capacitive load C_k . As the comparator is used in a fully differential architecture, the common-mode kickback have less importance than the differential kickback has.

A Strong-Arm and a Schinkel-Double-Tail have been designed for the same offset standard deviation. Once laid out as in Figure 4.10, and parasitic extracted, a 100 point Monte-Carlo analysis of their characteristic inside the test bench is performed.

Figure 4.11a represents the offset standard deviation over temperature. As agreed in the design phase, both architectures present a similar offset profile. As explained in [160], the offset variation over temperature is tightly linked with the inverse of g_m/I_D variation.

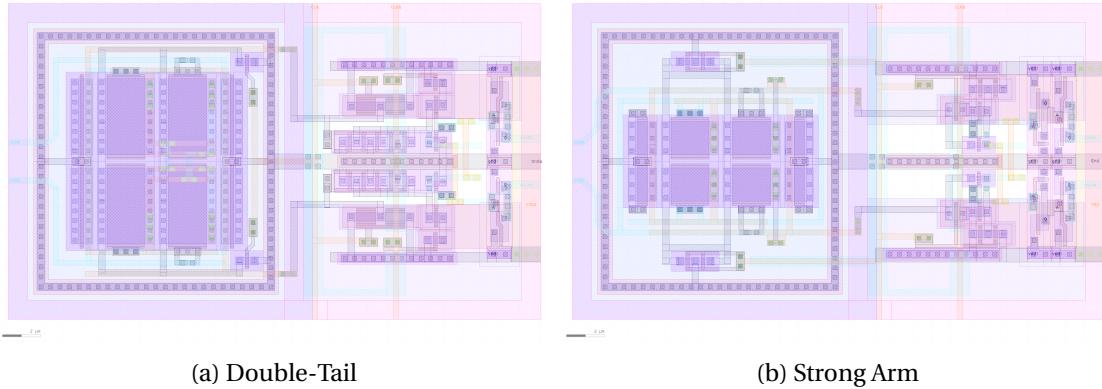


Figure 4.10 Layout of slow version of comparator designed made to respond in maximum 3 ns with a footprint of $28\mu m \times 16\mu m$

Figure 4.11b depicts the $3-\sigma$ delay variation over temperature of both architectures. For a differential input voltage of $800\mu V$, the maximum delay increase with the temperature. The average response time of the SA latch varies from 2.3 ns to 2.53 ns. This represents a variation of 460 ppm/ $^{\circ}C$. While the standard deviation shrinks from 0.22 ns at $-40^{\circ}C$ to 0.15 ns $+175^{\circ}C$, the maximum delay is almost constant over temperature. In the same condition, the DT latch exhibits an average time increase of 3333 ppm/ $^{\circ}C$. The main contributor to this temperature sensitivity is the differential pair transistor of the pre-amplifier as the design for low-offset gives more weight to the first stage. This value matches the results of a low- V_{th} transition frequency temperature sensitivity for the designed current of $20\mu A$ in differential pair transistors. However, the DT latch features a response time process variation increasing with the temperature as 0.15 ns at $-40^{\circ}C$ to 0.2 ns $+175^{\circ}C$, close from the values of the SA latch.

In the Figure 4.11c, the differential kickback is computed at the sample time since its effect will be seen when the decision is taken. While the temperature worsens the differential kickback of the Strong ARM, the one of the double tail is more stable. Moreover, the kickback of the double tail is one order of magnitude lower than the kickback of the Strong ARM. So, the Double Tail is less prone to error. With a $600\mu V$ of differential kickback for the Double Tail, this comparator introduces an error that is equivalent to 11.7 bit LSB for a differential input voltage of 1 V. In comparison the Strong ARM latch introduce an error equivalent to 9.4 bit LSB.

Figure 4.11d presents the electrical simulation of comparator power consumption from $-40^{\circ}C$ to $175^{\circ}C$ at 100 MHz. In both topologies, the power consumption increases as temperature rises. The Strong ARM average power consumption is $34\mu W$ varying 592 ppm/ $^{\circ}C$ over the temperature range while the Double Tail topology exhibits a $74\mu W$ average power and 535 ppm/ $^{\circ}C$ variation over the temperature range. Considering power consumption, one may conclude that Strong ARM has lower power consumption. However, Double Tail depicts a smaller variation $\Delta P/P(T_0)$ with respect to the temperature.

4.2 Latch comparator design

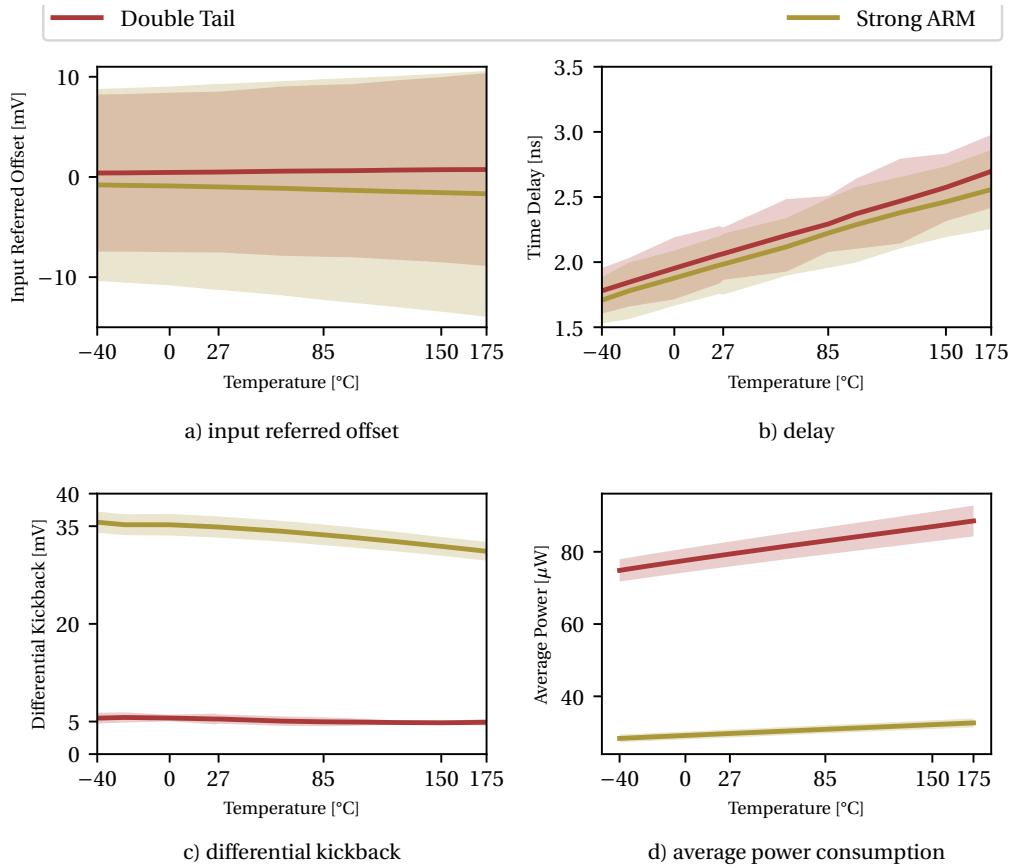


Figure 4.11 Delay, Offset, Kickback and Power consumption of designed comparators over temperature after layout parasitic extraction

Even if a Monte-Carlo analysis of 6σ process and mismatch parameter variations have been performed over temperature for each comparator, in the Table 4.3, only the worst value of the post layout simulations is presented.

According to these results, for low-power systems without calibration on comparators, the Strong ARM latch is more appropriate. With a smaller size than the double tail and low power consumption, the Strong ARM fit well the requirements for a flash converter. The Double Tail is tailored for fast systems with a moderate requirement on the offset. Since the power consumption is inversely related to the squared standard deviation of the offset, a constraint on it makes this comparator consumes more than the Strong ARM. The Double Tail is far more efficient than it is with calibration which relaxes the offset constraint.

Verified by simulation, in both topologies a large transient current is needed. And the faster the latch should be, the more important the current is. While the Strong ARM latch requires a peak voltage of $300 \mu\text{A}$, the Double Tail requires twice this current.

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Table 4.3 Post-layout simulation worst results over temperature and process for design comparators

Criterion	Double Tail		Strong Arm	
	slow	fast	slow	fast
Offset [mV]	$\mu = 0.6, \sigma < 3.5$	$\mu = 0.7, \sigma < 6.5$	$\mu = 0.3, \sigma < 3.9$	$\mu = -0.2, \sigma < 5.3$
Hysteresis [μ V]	<450	<450	<450	<450
Peak KickBack [mV]	Diff.: <4.7	Diff.: <3.34	Diff.: <37	Diff.: <18.8
C_input = 100 fF	Common: <500	Common: <230	Common: <230	Common: <173
Delay $\Delta V_{in} = 1$ mV	<2.8 ns	<1.4 ns	<2.8 ns	<1.4 ns
Delay $\Delta V_{in} = 20$ mV	Not Calculated	<0.8 ns	Not Calculated	<0.8 ns
Average Power [μ W]	<90	<68	<33	<39
Peak Power [μ W]	<640	<820	<625	<496

4.3 OTA

Operational Transconductance Amplifiers (OTA's) are used in microelectronics applications to drive small capacitive loads at high frequencies. An OTA is basically an op-amp without any output buffer, preventing it from driving resistive or large capacitive loads. They are preferred over op-amps mainly because of their smaller size and simplicity. The OTA is based on a differential amplifier at the input. The purpose of an OTA is to generate a current proportional to an input voltage difference. This report is concerned with the design of a fully differential OTA, meaning there are two outputs. The difference in the output currents should be proportional to the difference in the input voltages.

4.3.1 Challenges

The proposed converter topology is composed of an Incremental- $\Delta\Sigma$, an Algorithmic, and a SAR. The first stage giving the residue of the conversion to the following stage, most of the OTA constraints corresponds to the desired expectation of the Incremental- $\Delta\Sigma$ integrator.

With a settling time-based approach, without calibration, the gain and the bandwidth of the OTA should ensure a cumulative settling-time error less than 1/2 LSB. Since the system is clocked at 100 MHz and a DFF responds in less than 1ns over the temperature range, we should account for 9 ns of settling time with the output voltage of the integrator following the equation (4.11) where V_{in} is held constant over the integration.

$$V_{out}[n] = V_{in} \frac{C_s}{C_i} \sum_{i=0}^{N-1} \frac{\left(1 + \frac{1}{A}\right)^i}{\left(1 + \frac{C_s + C_i}{C_i A}\right)^{i+1}} \quad (4.11)$$

The error at the end of the integration is thus given by equation (4.12). This does not consider the bandwidth limitation effect.

$$V_{error}[n] = V_{in} \frac{C_s}{C_i} \left(\sum_{i=0}^{N-1} \frac{\left(1 + \frac{1}{A}\right)^i}{\left(1 + \frac{C_s + C_i}{C_i A}\right)^{i+1}} - N \right) \quad (4.12)$$

This leads to the minimum gain required for this amplifier. This minimum is the flat horizontal found in the Figure 4.12. The vertical parts of curves corresponds to the area for which the speed of the amplifier could not result in an error below the desired error level. An optimum point blending performance is found and highlights by dots in this figure. This figure does not consider slew-rate and phase margin as the amplifier is supposed to be a first-order system with a tolerance to 1 ns of slewing.

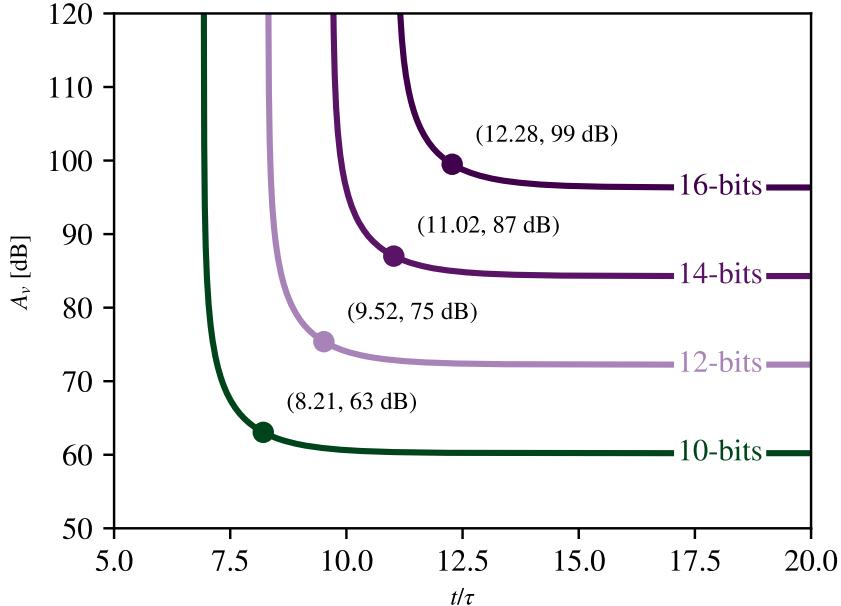


Figure 4.12 Trade-off speed versus gain of the amplifier for the SC-Integrator of the $I\Delta\Sigma$

Therefore, a 12-bits accuracy requires a gain of 75 dB and a gain-bandwidth product of 952 MHz whatever the load is. As discussed in the Section 2.2.2.1, and in Section 2.2.1.2 there is no optimum solution to prevent the speed of the amplifier to fall over the temperature range without an adaptive biasing. Moreover, the bandwidth limitation is general and does consider the feedback factor β of the configuration in which the OTA is. Let's consider the case of the first stage: the $I\Delta\Sigma$ whose integrator output is given to the following sub-ADC.

The feedback factor is given to be $C_I/(C_S + C_I)$ where C_I and C_S are the respectively the integration capacitor and the sampling capacitor. The equivalent gain-bandwidth product of the

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system in such configuration is the product βGBW_{OTA} . As the feedback factor is strictly less than 1, the minimum gain-bandwidth-product of the OTA shall be greater than $952/\beta$ MHz. For the standard design of $C_S = C_I$, this requires a design of an OTA having a $GBW > 1.9$ GHz even at high temperature and a DC Gain greater than 75 dB.

As the load seen by OTA varies from one clock cycle to another, only the worst case is considered for each stage. This corresponds to a 400 fF load on the first stage OTA, and a 1 pF for the second stage amplifier loading the SAR.

These stringent specification implies that a calibration free ADC over the temperature range is not feasible. Nevertheless, both the gain and GBW limitation can be corrected by the use of digital calibration as in [161, 162].

In consequence, the expectation of the OTA is corrected downwards to save power and noise with only a sufficient DC Gain over the temperature. We therefore investigate the possibility to use a low-power, high gain OTA for high speed ADC over temperature. The GBW limitation remaining the only deficiency, a digital calibration shall correct it as well as the process mismatch of surrounding capacitors.

4.3.2 Design

From the review of amplifier topology in Section 4.1.2, the folded cascode amplifier is selected. The variation around this basis is represented in Figure 4.13. To operate even at reduce supply voltage, a standard high swing current mirror for the biasing circuit is preferred. Moreover, the input is a complementary differential pair to enlarge the input swing and increase the slew rate [144]. As the amplifier will also be used in unity gain configuration the input swing is approximately the output swing. The complementary differential pair overcomes limitations arising on a Folded Cascode in this particular situation.

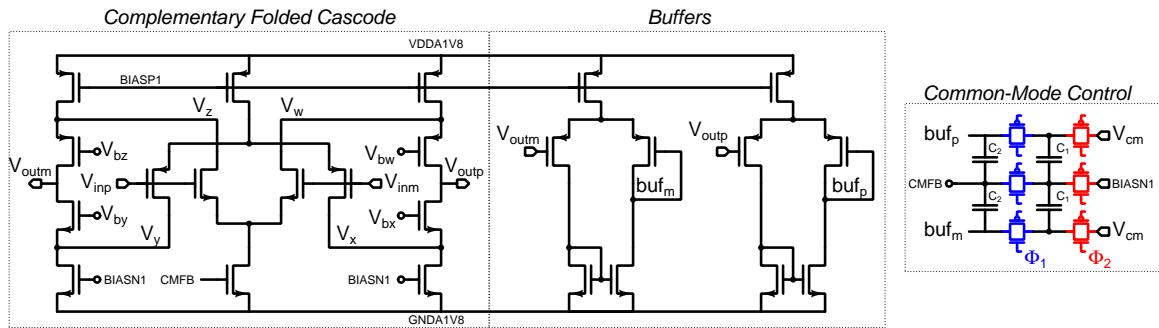


Figure 4.13 Designed OTA with its common-mode feedback

This section decomposes the amplifier design into smaller analog blocks which are: the Complementary-Folded-Cascode (CFC), the Common-Mode Control, Buffers, and Current Mirrors for the Biasing.

The CFC architecture is a modified current steering architecture that incorporates a class AB cascode stage. In this section, the design focus on one of the possible trade-offs over the temperature which lead to reduced settling time error over process and temperature variations.

Among possible trade-offs, constant current, constant g_m , and constant gain are only those achievable. The Section 2.2.1.4 reveals the existence of a zero temperature coefficient point for the current. Nevertheless, this point is found for a non constant g_m/I_D ratio where both gain and transconductance suffer from the temperature variation: the slew-rate is constant over a large temperature range while the gain and speed is severely degraded. As seen in Section 2.2.2.1, the transistor transition frequency admits no zero temperature coefficient which scale down the maximum achievable speed. The constant- g_m candidate is often used in temperature aware design as it conserves the primary pole location. An extra circuit is required for the compensation of the process and voltage variation [163]. Then, the remaining option is a constant gain over temperature. This is feasible for very small current according to Section 2.2.2.2.

In consequence, we propose a design where the input stage and the cascode output experience each a different design choice to blend performances.

4.3.2.1 Input Differential Pairs

While the input stage targets very high speed, the second stage should ensure a sufficient current to limit the slew rate time. As discussed earlier, we tolerate a slewing of 1 ns. This given, the slewing current should be at least $375 \mu\text{A}$ in the first stage and twice as much for the second stage. This current fixes for us, the biasing current.

In Section 2.2.2.1, to achieve the maximum speed with reduced thermal dependence $L = L_{\min}$ and a maximum current of $10\mu\text{A}$ for a transistor with the size of $1\mu\text{m}/180\text{nm}$. For such biasing, the intrinsic gain is given to be decreasing for a temperature rising according to Section 2.2.2.2. We expect then, a gain variation coming from this part of the design. But this is less relevant since most of the gain comes from the gain boosting cascode.

As the current and the transistor's length is now defined, their width is then defined by the g_m/I_D methodology. This structure has been considered in an other research work and can be studied in detail in [164–166]. We keep for the design the Unity-Gain Frequency equation defined as

$$\omega_{ugf} = \frac{g_{m1n,m2n} + g_{m1p,m2p}}{C_L} \quad (4.13)$$

Therefore, the sum of NMOS and PMOS transconductance should be equal to 2.5 mS in typical conditions at 27°C. The sizing adds an extra margin to take into account layout parasitics, process variations, and power supply variations of 10%.

4.3.2.2 Cascode Stage

For the class AB cascode output stage, the gain, the current, and the output swing are key factors. As the current in the branch is already fixed by the slew-rate, the gain is of primary concern here.

Section 2.2.2.2 reveals a lesser sensitivity over temperature for 1 μ A biasing current of a differential transistor sized at 1 μ /180 nm. In order to slightly increase the gain, the cascode transistors are sized for $L = 2L_{\min}$.

For the current sources at the folded node, a high impedance reduces the sensitivity to the power supply variations while the capacitance shall be minimized to improve the overall speed of the OTA. A good trade-off has been found for $L = 3L_{\min}$. As the threshold voltage temperature coefficient depends on the transistor's length, as the bigger L is smaller this coefficient will be, the chosen L offers a reduced temperature sensitivity compared to $L = L_{\min}$.

Considering an output swing from 525 mV to 1.275 V, the transistors of the cascode part cannot be in strong inversion. As their drain-source voltage is increasing with the level of inversion, the maximum output swing will be limited to $V_{DD} - 4V_{DS}$. As the drain-source voltage increases by 100 mV from 27°C to 175°C, a reduced power supply of $V_{DD} - 10\%$ pushes the cascode transistors into deep sub-threshold operating region at high temperature.

$$\begin{aligned} 4V_{ds\max} &= (V_{GSsource,n} - V_{THsource,n}) + (V_{GScascode,n} - V_{THcascode,n}) \quad (4.14) \\ &+ (V_{GSsource,p} - V_{THsource,p}) + (V_{GScascode,p} - V_{THcascode,p}) \\ &= 0.9V_{DD} - (1.275V - 0.525V) = 0.87V \end{aligned}$$

where $V_{GSsource} - V_{THsource}$ represents the voltage overdrive of the transistor playing the current source of the folded cascode, and $V_{GScascode} - V_{THcascode}$ the voltage overdrive of the cascoding transistor. Let's suppose the margin split evenly across PMOS and NMOS transistors, the minimum voltage required is 0.335 V at 27°C for $(V_{GSsource,n} - V_{THsource,n}) + (V_{GScascode,n} - V_{THcascode,n})$.

Therefore, the wide-swing cascode biasing depicted by Figure 4.14 allows correct operation from an output voltage $V_{out\min} > V_{ds3} + V_{ds5}$. $M2$ and $M4$ act like a single-diode connected transistor to create the gate source voltage for $M3$. Including $M4$ helps lower the V_{ds2} so that it matches V_{ds3} . As $V_{gs1} = V_{gs4}$, $M2$ and $M3$ are pushed at the edge of the triode region such that $V_{ds3} = V_{ov3}$. In this operation mode, the transistors $M2$ and $M3$ are closer to the current

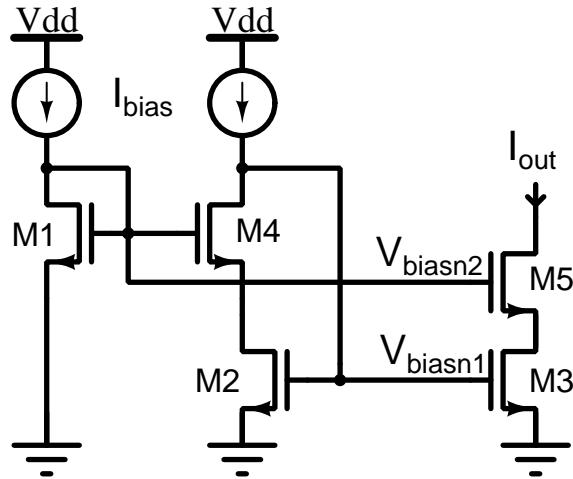


Figure 4.14 Wide-Swing current mirror for the biasing of the proposed OTA

insensitivity point with respect to the temperature defined in Section 2.2.1.4. As the transistor M_5 is no more in saturation for $V_{ds5} = V_{ov5} = V_{ov1} - V_{ov3}$, $V_{out\min}$ shall be greater than the voltage overdrive of transistor M_1 . Thus the output swing is enhanced and the output resistance defined by the transistor M_1 .

For our application, the output swing is known and mainly defined by the voltage overdrive of one transistor for NMOS and one for PMOS. The design constraints are now relaxed and cascode transistors can be minimal to reduce parasitics on the output node which enhance both the speed and the PSRR frequency response [167].

4.3.2.3 Gain Boosting

To boost the DC gain, if appropriate, either a single-ended or a differential auxiliary amplifier can be envisioned. The single-ended boosting architecture uses four auxiliary op amps to regulate the transconductance of cascode transistors and enhances the gain. It is first reported by [140]. However, the single-ended version of the boosters are associated with some undesired effects:

- Signal usually travels a longer path inside the booster and sees an extra pole from an internal current mirror. Therefore, frequency response of the booster suffers, especially when optimizing the pole-zero doublet effect.
- Noises generated by the biasing circuitry inside the boosters are not correlated. This means the noise overhead associated with gain boosting is higher.

The problems are addressed by using a fully differential gain-boosting scheme. This improves the settling behaviour and rejects the common source of noise. But fully differential amplifiers require common-mode feedback increasing the area and injecting thermal noise. A Sackinger

version of the gain boosting could also be used to reduce the length of the signal path inside the booster, and to reduce the noise generated by decreasing the number of transistors needed for the amplification.

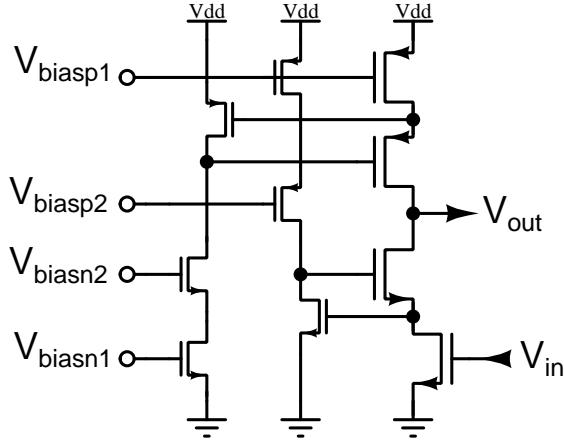


Figure 4.15 Nested-Gain boosting for large gain OTA

In Figure 4.15, the small size of the Sackinger version is exploited to even more enhance the DC Gain by nesting the gain boosting. This nesting requires only small size transistors which does not connect large parasitics on the folding nodes of the core amplifier. For a common source transistor the voltage noise is given by equation (4.15) which combines the thermal noise, the flicker noise, and the output resistance of the current source r_{Id} .

$$\overline{V_n^2} = \left(4k_B T \gamma g_m + \frac{K}{C_{ox}WL} \frac{g_m^2}{f} + \frac{4k_B T \Delta f}{r_{Id}} \right) (r_o || r_{Id})^2 \quad (4.15)$$

The noise reduction implies a large g_m coming from a transistor in strong inversion to reduce the output resistance r_o . As the total noise is proportional to the output impedance of the common source configuration, the output resistance of the current source shall be large. To reduce the flicker noise, the area of the transistor shall be maximized and the transconductance minimized. Therefore an adjustment of the operation mode and the area is performed to reduce the noise spectral power. The decision is made as follows:

- the main gain boosting stage is designed with $L = 2L_{\min}$ and transistors operate in strong inversion to reduce the thermal noise impact.
- nested gain boosting is designed with $L = 4L_{\min}$ and transistors operate in moderate inversion to reduce the flicker noise while giving a larger DC gain.
- the current sources are cascaded, and regulated, to improve both the DC gain and the noise due to its output resistance.

The main gain boosting stage also impacts the settling of the overall OTA. For optimal settling, the speed of the gain boosting stage should respect the following criterion according to [150]

$$\beta\omega_{ugf} < \omega_{add} < \omega_{p2} \quad (4.16)$$

where, $\beta\omega_{ugf}$ is the closed-loop dominant pole frequency, ω_{ugf} is the open-loop unity-gain frequency, ω_{add} is the unity-gain frequency of the boosting amplifier and ω_{p2} is the second pole frequency of the main amplifier (also the second pole of the local gain-boosting loop). In the current design, the second pole frequency of the main amplifier has been overlooked over temperature and process. This procedure has been applied then on a PMOS version of the gain boosting for the Complementary Folded Cascode.

4.3.2.4 Common-Mode Control

To regulate the common mode voltage of differential circuits, one could either use feed-forward compensation (CMFF) or feedback compensation (CMFB). The feedback compensation being more reliable than the feed-forward, the latter is disregarded.

CMFB's stabilize common-mode voltages for differential-mode analog systems by means of adjusting the common-mode output currents. The two differential output voltages are averaged to estimate the common-mode voltage, which is compared with the designated reference of the common-mode. The difference is then amplified and converted into the common-mode output current to adjust the common-mode voltage. Most of the currently used common-mode feedback circuits fall into the following four categories:

- Shunt Inverters CMFB
- Resistor-Averaged CMFB (RA-CMFB)
- Differential Difference Amplifier CMFB (DDA-CMFB)
- Switched-capacitor CMFB (SC-CMFB)

Whatsoever the realisation is, some rules have to be fulfilled when designing a good CMFB circuit:

- First, a unity gain-bandwidth of the common-mode loop should be higher than the one of the input signal to prevent the decrease of the operational speed. Or at least equal.
- Second, common-mode loop compensation is necessary to ensure the common-mode stability.
- Third, a common-mode detector should have a linear characteristic.
- Finally, the performance of the fully differential amplifier needs to be maintained when the CMFB circuit is connected.

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For high speed purpose one could consider a continuous time CMFB (CT-CMFB). CT-CMFB are usually designed based on one bloc for sensing the error on the common-mode voltage and one amplifier it.

Nowadays the trend being to scale down the supply voltage, shunted parallel inverters are more and more used to sense the common-mode voltage. There is shunted CMOS inverters as in Figure 4.16a, but are considered not as a good practice since neither the current is well controlled nor the biasing point despite a very large output range allowed. Nevertheless the inverter can be changed into a transistor in common source to better control the current such as in Figure 4.16b[168–170]. For a power supply voltage of 1.8 V, this solution turns out to be power hungry consuming more than the core itself.

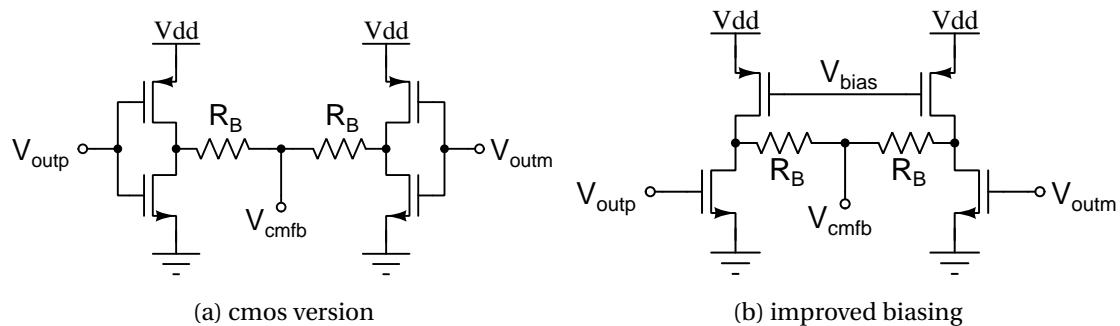


Figure 4.16 Shunt Inverters sensing CMFB

By the way, a CMFB can be decomposed into a sensing bloc estimating the current common mode and an amplifier bloc to apply the correction. Assuming that the gain of the amplifier is defined by the product of an effective transconductance and the output resistance, an output resistance variation also alters the DC Gain of the amplifier, violating the fourth rule. A resistive sensing circuit as in Figure 4.17a thus limits the gain of the OTA and draws a current between the two outputs V_{outp} and V_{outm} through averaging resistor R_A .

In order not to alter the DC Gain of the amplifier over temperature, the resistance of the common-mode sensing is replaced by two transistors in the differential pair resulting in a DDA-CMFB whose possible implementation is depicted by the Figure 4.17b. The impedance seen is therefore near infinite. As a transistor generates a current proportional to the voltage applied at its gate, DDA-CMFB becomes a relevant solution. As the power supply reduces, the DDA variant suffers from the non-linearity of the current drawn. As the temperature increase, the effect is ever more pronounced. The operating range in which the common mode voltage can be corrected is much more limited to the one of a switched capacitor version. In addition, the CMFB circuit shall be faster than the primary amplifier whose common mode voltage is controlled. Therefore, both the current consumption and the area are tremendously increased for high speed high gain OTA.

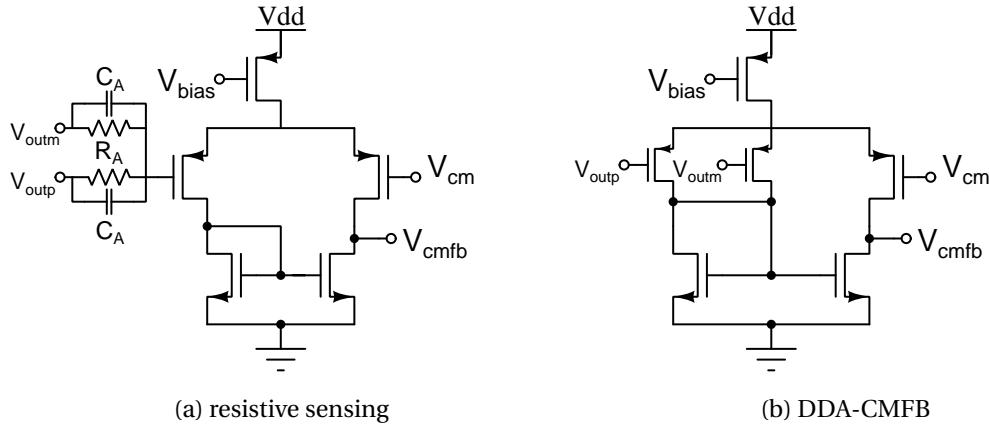


Figure 4.17 Typical continuous time CMFB

Considering a SC-CMFB, it is commonly assumed that the clock used is the same for the switched capacitor circuit surrounding the amplifier. With a standard SC-CMFB circuit as depicted by the Figure 4.18, the size of capacitors and the sizing of switches should be determined.

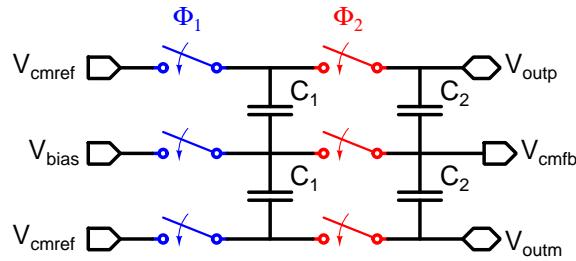


Figure 4.18 Standard SC CMFB circuit implemented

With respect to the DC Gain of the amplifier, the toggling of capacitor C_1 emulates a resistance connecting the output and the common mode voltage of reference. This equivalent resistance is evaluated as $1/(C_1 F_{clk})$ where F_{clk} is the clock frequency and C_1 the capacitor sampling $V_{cm} - V_{BIASN1}$.

Assuming that the gain of the amplifier is defined by the product of an effective transconductance and the output resistance, the required transconductance $G_m = g_m \cdot g_{mb} = g_m = 2.2 \text{ mS}$, a 75 dB gain results into an output resistance of $2.24 \text{ M}\Omega$. With $F_{clk} = 100 \text{ MHz}$, the capacitance C_1 should be around 4.4 fF. A standard SC-CMFB is not feasible considering mismatch and the parasitic of switches.

Therefore, a proposition is made for the design of the CMFB circuit to blend performances. This proposition consists in using a SC-CMFB and using a voltage follower to decouple the amplifier from the switched cap circuit. The benefits are twofold: First, the load seen by the amplifier is reduced and bumps up the unity gain frequency, and the phase margin. Second, the operating

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range of the CMFB circuit is enlarged compared to the DDA-CMFB circuit without reducing the gain of the amplifier.

In order to improve the accuracy of the settling voltage, the transistor's size is 220 nm/360 nm. Concerning the settling time, the ratio capacitor C_2/C_1 is crucial. From the equation (4.17) issued in [171], one can intuit that the bigger the ratio is, the slower the amplifier is, and more accurate will be the settling. Considering charge injections and clock feed-through on C_1 , they will have a reduced impact as the ratio C_2/C_1 is big and C_2 capacitors driven by buffers. By the way, the gain of the cascode approximate to A_{cm} is assumed to be large to reduce the impact of biasing voltage variation. As a trade off between settling speed and accuracy, the ratio is set to 3. This means that 3/4 of the new voltage is coming from its value at the previous clock step while 1/4 from the common-mode mismatch.

$$V_{outc}[n] = \frac{C_2}{C_1 + C_2} V_{outc}[n-1] + \frac{C_1}{C_1 + C_2} \frac{V_{cm_{ref}} - V_{bias}}{1 + \frac{1}{A_{cm}}} \quad (4.17)$$

For the mismatch, the Pelgrom coefficient of cmm4t is 0.4 %/ μm . With a minimal size of 2 μm x 2 μm the mismatch coefficient of C_1 is 0.14 % and on C_2 0.08 %.

In the proposed CMFB circuit of the Figure 4.13, the output buffer has 10 ns to settle accurately. The accuracy is based on the mismatch in capacitor in the SC-CMFB circuit and the precision of the output voltage. To reduce the latter, the differential pair transistors of these buffers are sized at $L = 3L_{\min}$ to have a small gate capacitance and a large gain at a moderate intrinsic speed.

Buffers are not cascoded to allow a wider output swing than the core amplifier without suffering from a DC gain deficiency as they solely replicates their inputs. Then, the biasing current is 140 μA such that the unity gain frequency is set to be around 700 MHz. This corresponds to 7 times the speed of the clock. Therefore, most of the inaccuracy is due to the mismatch in the gain of the voltage follower set in unity gain configuration.

This buffer-sc-cmfb combination allows the design of high-gain amplifier in high frequency clocked system. This experiment is then verified over temperature and process variations.

4.3.2.5 Layout Consideration

The OTA is the core of the ADC analog and the performances of the full ADC heavily relies on the OTA. Therefore, the design blend constraints to reach technological limits. In the scope of the thesis, the reliability is of key concern in the design such that physical phenomenon in the manufacturing process are considered.

A folded cascode amplifier is an architecture sensitive to current mismatch at the folding node. Figure 4.19 represents the current error on the output node due to the mismatch. As the load is fully capacitive in most applications, the error is integrated. To minimize the error, the pmos

transistors shall be matched in that error to the ideal current value is the same. The layout will thus ensure that mechanical stress, and temperature gradient seen are the same in these pmos transistors.

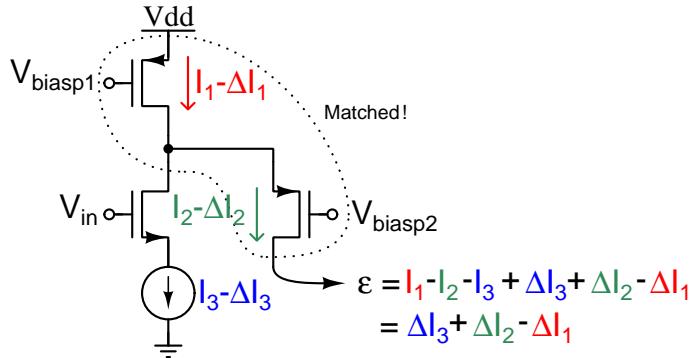


Figure 4.19 The error generated on the output current based on the current mismatch due to the biasing

The remaining source of error are thus the transistors of the differential pair generating an ΔI_3 error. By design, the common mode circuit adjusts I_3 to correct so that it remains only the error coming from ΔI_1 and ΔI_2 cancelling one another. Using a two differential pairs (one in nmos and one in pmos), only the mismatch of nmos transistors in the differential pair is compensated. As the area of pmos differential pair is twice bigger than the area of nmos one, $\Delta I_{3p} < \Delta I_{3n}$.

A requirement is a good matching in current of the pmos differential pair current source, and the nmos-cascode of the CFC-Folded Cascode OTA which suppose a better matching in the biasing circuit.

Since the principle is applicable for both PMOS and NMOS folding nodes, the layout is split into a group of low-vth nmos and low-vth pmos.

To reduce ΔI_3 , the layout is drawn with mechanical stress, the temperature gradient in mind with long term viability to pay a careful attention to the current flow always in the same direction. Unfortunately, usual layout recommendation and matching analysis are typically carried out on simple rectangular transistors which become impractical for large W/L ratios of high-speed amplifiers. To be closer from test cases during matching analysis, the large differential pair is split into parallel smaller ones.

Among layout good matching techniques, a common centroid layout is usually the way of doing it. Suppose the gradient of stress or temperature is a linear function of the distance from the source of the stress or from the hot spot, the average stress/temperature seen by a transistor in a differential pair is equivalent to the average stress concentrated on its centroid. As the respective centroid of differential pair transistors are at the same position, the first order gradient is compensated. In Figure 4.20, the centroids are represented by circles for common-centroid and

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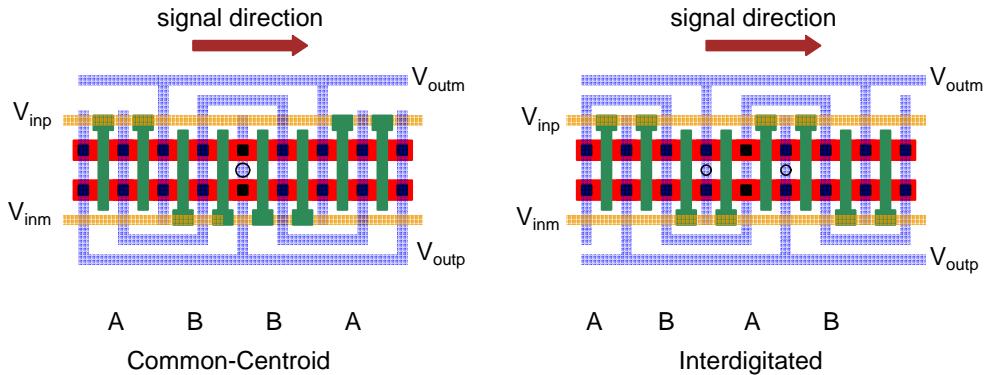


Figure 4.20 Comparison of mismatch for common-centroid and interdigitated layout of a differential pair

interdigitated layout. The figure highlights the mismatch of centroids but also demonstrates the capacitive mismatch on the outputs.

As the transistors of the differential pair have an ever bigger W/L ratio, the differences are more pronounced. Splitting them in parallel chunks of differential pairs, with the following pattern:

```

ABAB
BABA
-----
BABA
ABAB

```

converges the centroids of A transistors and B transistors toward a common-centroid one without the capacitive mismatch on the outputs. Another advantage is a limited dispersion of transistors whose statistical mismatch is improved by a factor $1/\sqrt{N}$ where N is the number of parallel differential pairs as given by [172].

In order to use the OTA inside a medium-to-high resolution ADC, the OTA shall exhibit low-noise characteristic. The traditional method to cope with the noise is at the design stage to have transistors in strong inversion with low-impedance and large parasitic capacitance to limit the bandwidth of the noise. From a layout point of view, the interdigitated transistors of the large differential pair already display such abilities. Nevertheless, an often unconsidered source of noise is the substrate coupling noise.

As power supplies of surrounding elements suffer from large IR drops, the diffusion contact into the NWELL tub (resp. the substrate for the ground) can easily interfere. In a process with a p+ layer substrate the phenomenon is found to be boosted by the higher conductivity of this layer. To limit the effect, the differential pairs are surrounded by a substrate guard ring connected to the potential of the transistor source. Then, either a large space shall be allocated in the layout

to increase the impedance of the coupling path or a deep trench isolation (DTI) can be used as represented in Figure 4.21. As the technology allows DTI and this technique reduces the spacing needed, a ring of DTI surrounds the sensitive differential pair. This way, the noise sensitive part has been isolated from potential noise source.

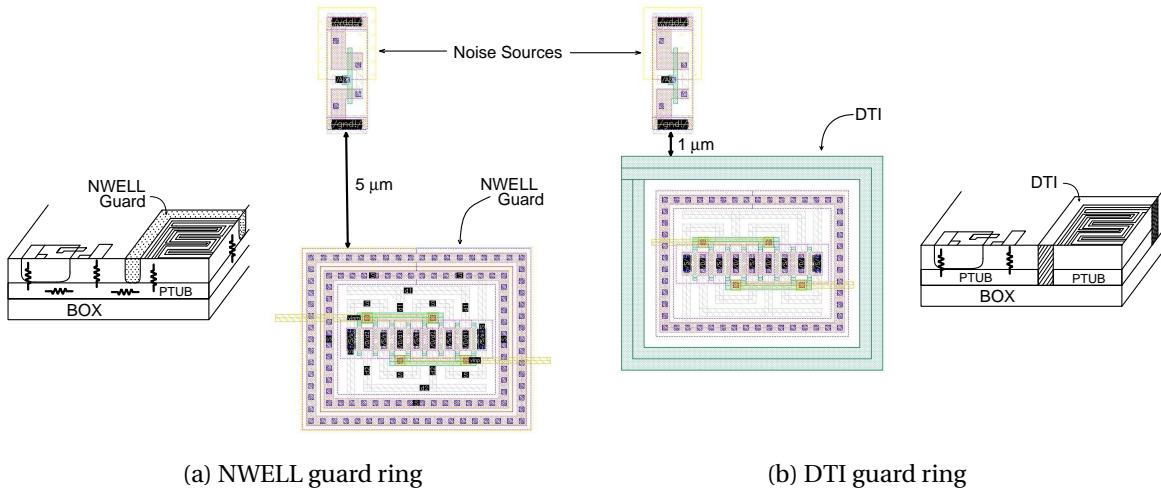


Figure 4.21 Substrate noise coupling with a protection based on a) a NWELL guard ring and on b) a DTI one

Concerning other parts, there is only one ground connection for the positive and negative branch. For a reduced impedance of the coupling path coming from the ground, a single connection point for the two branches conveys the noise in the same manner to the outputs of the OTA. The design being fully symmetrical and being differential, the noise from a ground coupling cancels differentially. This is not the case for the power supply coupling since each branch has a separate power supply rail. Nevertheless, the NWELL tubs increase naturally the impedance of the substrate coupling path.

For the layout of the folding cascode the L is different between the current source (A) and the cascode transistor (B). The current through A transistors is twice as much through B transistors while the current matching even for surrounding variation shall be assured. To cope with these basic requirements the ABABAAAABABA pattern provides a common centroid for A transistors and B transistors with twice as much A than B. Moreover, both A and B are placed inside the same NWELL tub as depicted by Figure 4.22.

Weakness introduced in the current layout are the disunited layout of the biasing circuit and the OTA. Therefore, the matching of transistors in the biasing circuit and the OTA suffers from an extra term proportional to the distance separating them. An improvement would be to join the biasing/OTA transistor forming a current mirror in the OTA. In addition, the biasing voltages

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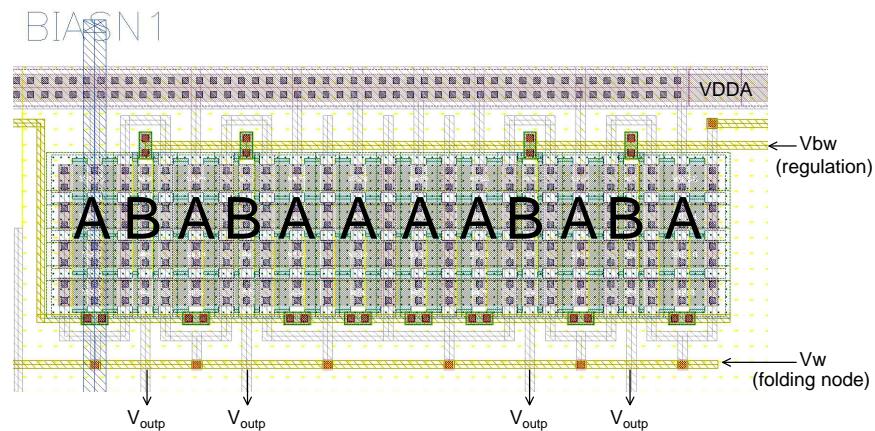


Figure 4.22 Layout pattern used for the regulated cascode layout inside the same NWELL tub

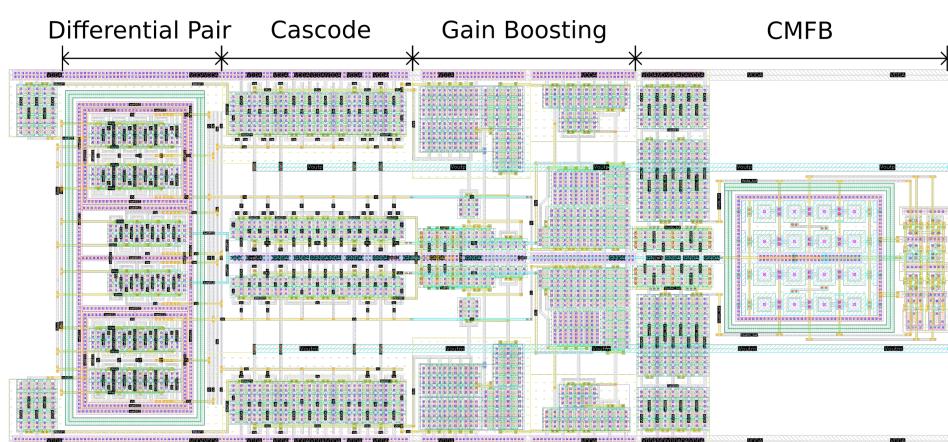


Figure 4.23 Gain Boosted CFC-Folded Cascode OTA layout 52 μ m × 128 μ m

are propagated by METTP over the amplifier. This results into biasing voltages exposed to the surrounding of the chip and require a reconnection for use in projects with more metal layers.

Concerning the biasing voltage of the current pmos current sources, the cascode and the current source of the differential pair are not in common. In consequence, a mismatch is only partially corrected by the CMFB.

4.3.3 Simulation Results

Performance metrics of the OTA depend of its application. In our case, the metrics are the results of both small signal analysis and transient response after layout parasitic extraction:

- DC Gain
- Unity-Gain Frequency
- Phase Margin
- Power Consumption
- Slew Rate
- Settling Error
- Noise

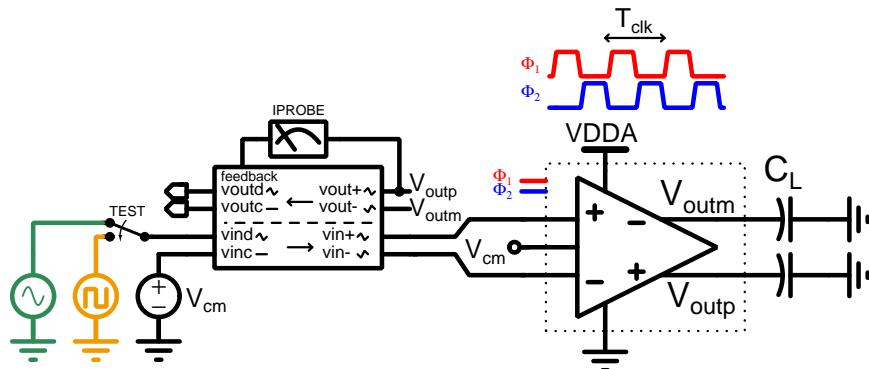


Figure 4.24 Test bench schematic for metrics extraction

For the sake of simplicity the allotted time for the settling is defined by ($T_{clk} - T_{nonoverlap} - T_{digital}$) which approximates 8 ns in worst cases.

The test bench depicted by Figure 4.24 sets up the OTA in a unity gain configuration, driving a capacitors $C_L = 400 fF$ (then 1 pF) wherein the IPROBE allows one to extract the open loop AC response through a PSTB analysis (DC Gain, Unity Gain Frequency, ...).

Then, the differential input voltage is a square wave signal from ± 500 mV around the common mode voltage of 900 mV of period 16 ns. Both the power consumption, the slew rate, and the settling error is extracted from this transient simulation. The power consumption from the current of VDDA represented in Figure 4.25, the slew rate as the derivative of V_{outd} , and the settling error as the difference between V_{ind} and V_{outd} 8 ns after the transition of V_{ind} .

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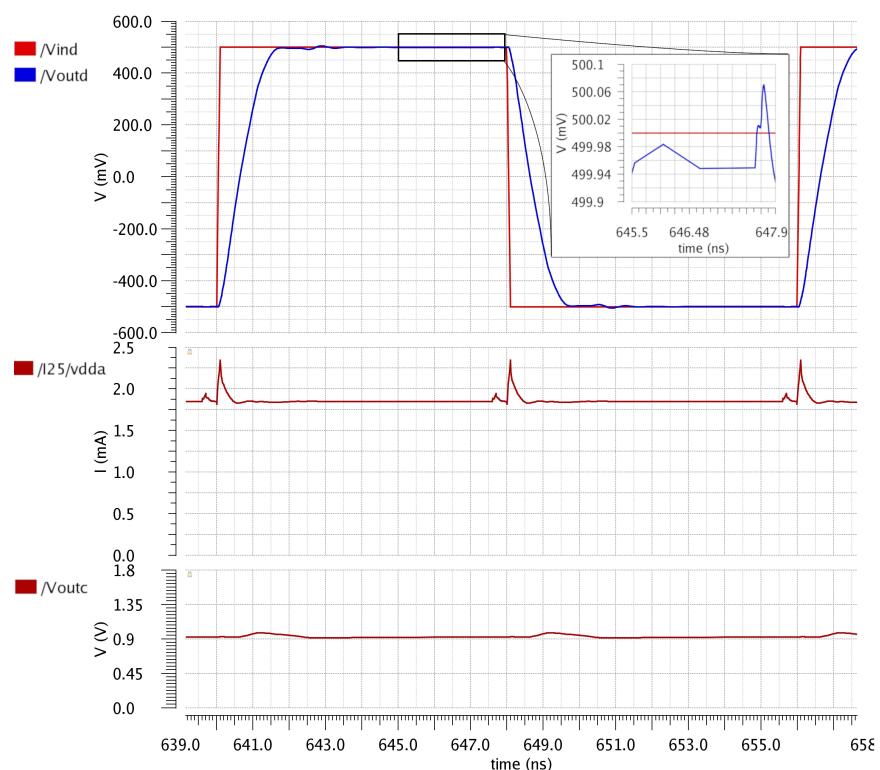


Figure 4.25 Transient waveform of the OTA in typical corner at 27°C for a power supply at 1.8 V and a load of 400 fF

Figure 4.26 represents variation of these metrics over temperature for different process corners. The trades made in the conception highlight a significant DC Gain, and Unity Gain Frequency drop in accordance to a biasing in moderate inversion without any compensation. This effect is more pronounced since by design the input common-mode is by 250-300 mV away from the NMOS and PMOS g_m -zero temperature coefficient (GZTC).

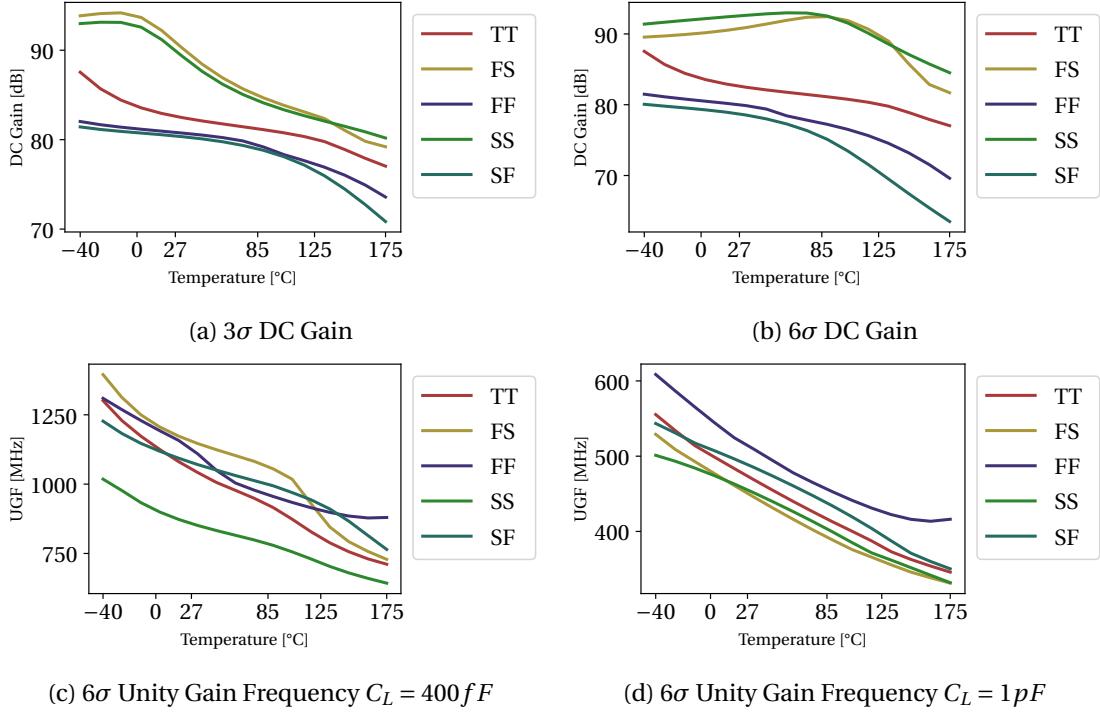


Figure 4.26 Post-layout results of the designed OTA: DC Gain and Unity Gain Frequency across process variations

The designed OTA exhibits a large-gain stable at 3σ over corners while at 6σ the FS corner achieves a limited gain at the limit of the specification. This results from a shrink current in the gain boosting for PMOS excessively slower than NMOS transistors regulating the cascode folding nodes.

Indeed, this correlates with settling error at 8 ns, for which the error at 6σ in this corner corresponds $800 \mu V$ on a $\pm 1 V$ jump while the others are below $400 \mu V$. Moreover, a discrepancy occurs at sub-zero temperature in this corner since the output voltages buffering to estimate the common mode is based on PMOS differential pairs.

Furthermore, Figure 4.27a and 4.27b represent the average settling error and the extrema settling error for the capacitive load variations in the process. The solid lines correspond to the settling error for the typical value of the capacitive load while the translucent areas are for extreme values of the capacitive load of the process. Thus, the FS corner is more sensitive to the capacitive load variation than any other corners as revealed by the largest translucent area. In

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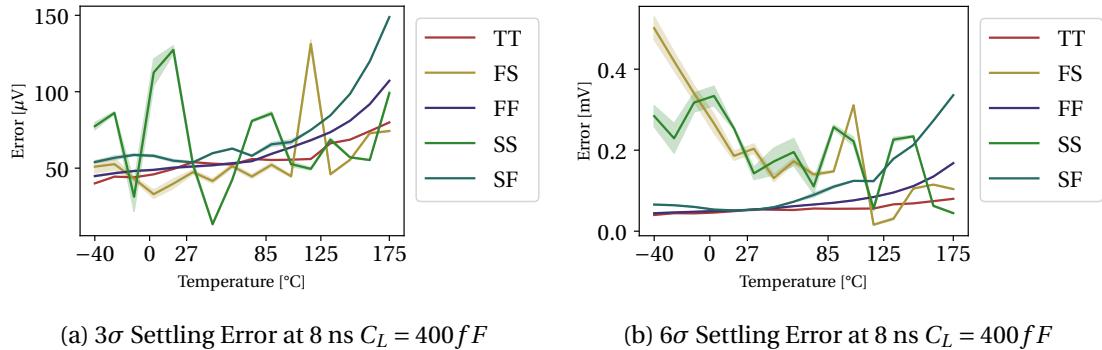


Figure 4.27 Post-layout results of the designed OTA: Settling error in 8 ns across process variations

general the overall values of the OTA reveal that it is possible to fully reset in a clock cycle in unity gain configuration. The settling error is small enough not to introduce a memory effect from sample to sample.

For a 3σ design, such topology ensures a good response for a reduced power consumption of 2.2 mW with its biasing circuit. In the case of a 6σ design, the power consumption is increased by $250\mu\text{W}$ and this OTA architecture evinces a limit in the process control which in turn binds the feasibility of a robust high speed ADC without calibration.

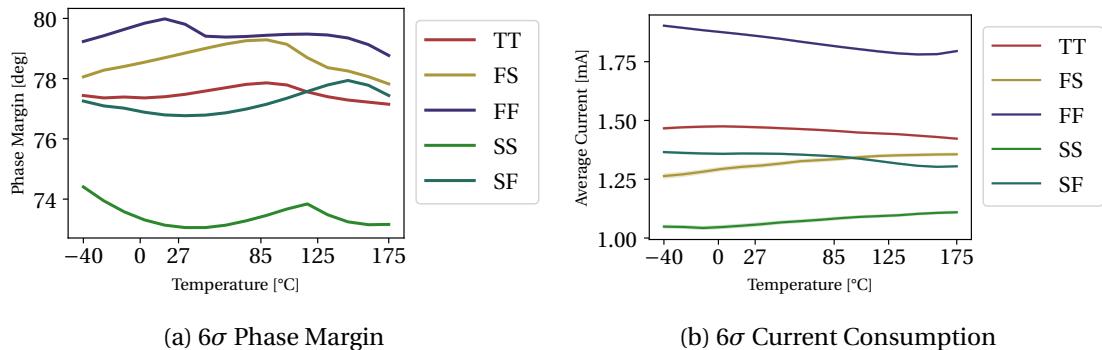


Figure 4.28 Post-layout results of the designed OTA: Phase Margin and Current Consumption

The settling error being strictly positive after an absolute value, a gamma distribution is assumed for which the TT corner is the maximum of probability while the other four corners represent extrema at N times the standard deviation of this distribution. Following this assumption, it is possible to estimate the percentage of ADC requiring a calibration which correct more than gain and offset error. Since the gain is not sufficient for the first stage integrator, the INL is affected as demonstrated in Appendix C.

Figure 4.29a represents the distribution of the error with the limit of the first stage to ensure 12-bits accuracy (red) and the second stage limit (green) without calibration. From this cumulative

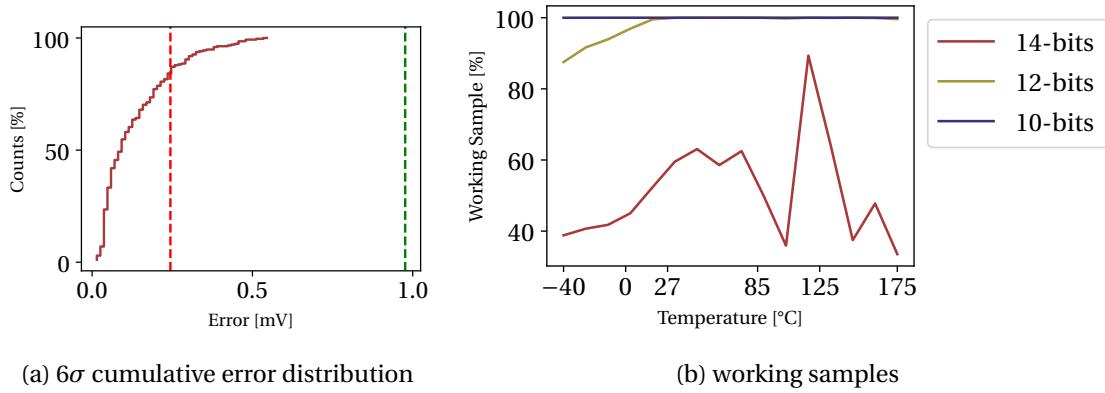


Figure 4.29 Settling error distribution and estimation of working samples

distribution, we estimate the achievable accuracy according to the settling error at 8 ns. The expected working samples are thus 75 %.

Then, a noise analysis is performed at 175°C to estimate the degradation on the signal noise ratio coming from the OTA with the maximum of thermal noise. From the voltage noise density represented in Figure 4.30 up to 2 GHz, we extract rms value of the noise. This noise rms value admits a maximum of $198 \mu V_{rms}$.

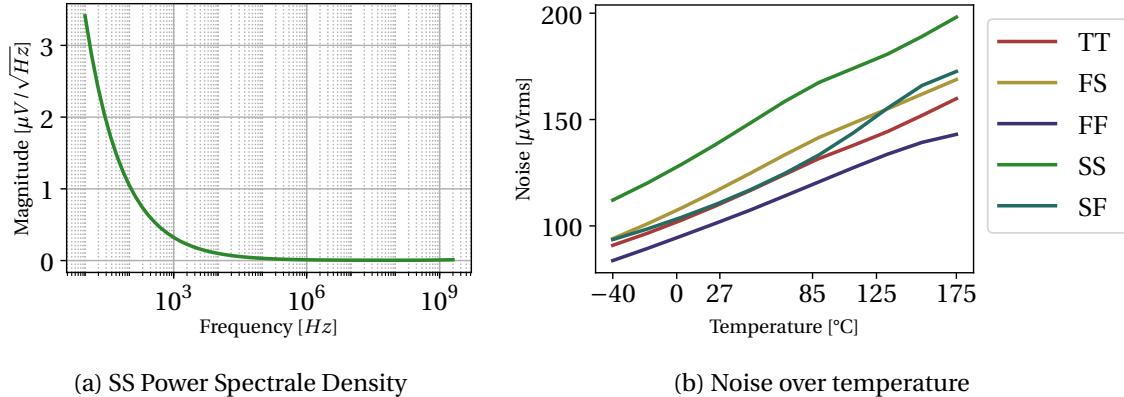
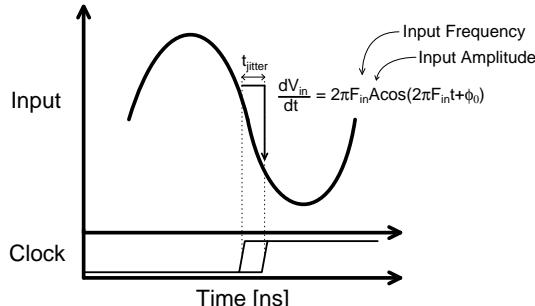


Figure 4.30 Noise power spectral density at 175°C over corners and its distribution over temperature

4.4 LVDS receiver design

High resolution ADCs are sensitive to the sampling clock. Figure 4.31 represents how the clock jitter affects the voltage sampled by the ADC, and the sample and hold circuit required at its input. With a possibility to reach 13.5-bits of resolution for an input frequency as high as 10 MHz, the maximum jitter is thus $t_{jitter} \leq V_{LSB}/4\pi F_{in} = 1.4ps$.



(a) Aperture jitter representation

$$SNR_{rms} = 20 \log_{10} \left(\frac{1}{2\pi F_{in} t_{jitter}} \right) \quad (4.18)$$

$$ENOB_{max} = \frac{SNR - 1.76}{6.02} \quad (4.19)$$

(b) SNR limit

Figure 4.31 Limitation of the SNR and ENOB owing to the variation of the clock period

In recent years low-voltage differential signaling (LVDS) has found broad application in consumer electronics, high-speed computer peripherals, telecom/networking, and wireless base stations. LVDS has distinctive advantages in performance, power, noise, EMI reduction, and cost. At a rate of 100MHz to 800MHz the LVDS signal can reach as far as 10m to 15m in a twisted-pair cable link, or > 1m in a PCB trace pair. In addition, the power consumption is relatively frequency independent, while the power dissipated in 100Ω load at the input is often around 1.2 mW in commercial chip. Usually used in time sensitive applications and possibly long PCB trace, the LVDS is well suited for the transmission of the clock of high-speed or medium-speed and high-resolution ADCs. The power budget for the LVDS receiver is then fixed to 1.4 mW to allow margin for an operation at high temperature.

Based on the IEEE 1596 standard for the LVDS, the input differential voltage is in the range of 100 mV to 350 mV as the current of the H-bridge is supposed to be in the range of 1 mA to 3.5 mA and the termination load is 100Ω . In order to select an accurate 100Ω resistance which does not vary much over temperature, it has been decided to externalize it outside of the chip. In order to decrease the jitter the design considers that the minimization of the intrinsic noise is fundamental as the noise is integrated on the capacitive load of the receiver and the duty cycle shall be preserved.

According to the section 2.2.2, the noise and the temperature frequency sensitivity are minimized for transistors in moderate or in weak inversion region. To the contrary, to reduce transition time variations, transistors should operate in strong inversion. Therefore, a multi-stage topology

4.4 LVDS receiver design

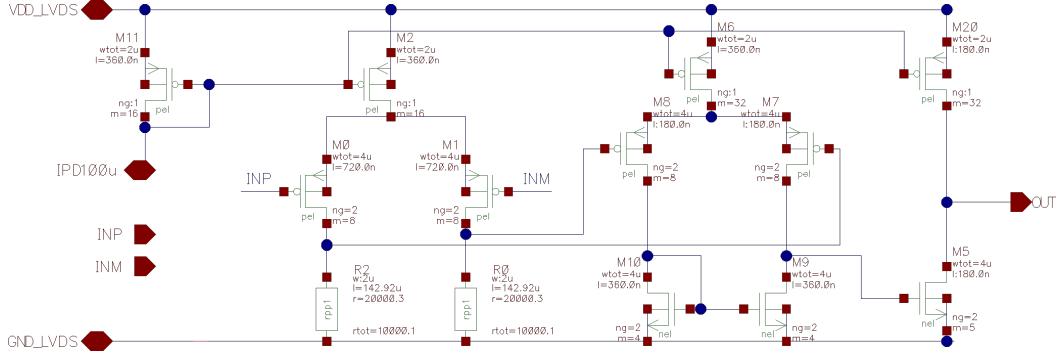


Figure 4.32 LVDS clock receiver to designed for high temperature

has been selected to blend performances, Figure 4.32. The first stage is a medium-gain amplifier to minimize the noise figure with $L = 4L_{min}$ to reduce the temperature sensitivity. The second stage further amplifies the difference with transistors in strong inversion and with a low gain and reduced parasitic capacitance of differential pair transistors to decrease the accumulated noise of the first stage. Then, the last stage is low-impedance and provides a large current to drive a capacitive load of 100 fF with steep transitions of 250 ps. The noise mostly defined by the first stage and the transition can then be adjusted by a single biasing current IPD100U. By default the value of the biasing current is 100 μ A based on the period jitter variation.

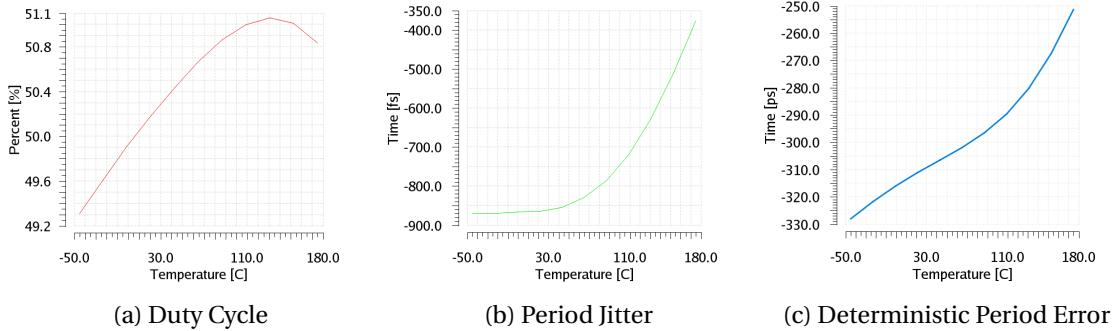


Figure 4.33 LVDS receiver duty cycle and jitter over temperature for $V_{cm} = 400\text{mV}$

Simulation results depicted by Figure 4.33, represents the variation due to the temperature and the process variations. The process variations consider the transistor and the resistance alteration while driving a 100 fF capacitive load for a differential input of 100 mV: the minimum detectable voltage of a LVDS signal for a common mode voltage of 400 mV. The period jitter is degraded at low-temperature due to the output common mode voltage of the first stage increasing. As there is a difficulty in the worst-speed corner as the capacitive load is increased to 110 fF, the resistance is increased by 10%. Nevertheless, this solution is able to drive a large capacitive load over the temperature range if the capacitive load is reduced or if the common mode voltage at the input of the receiver is closer from the ideal range as depicted by Figure 4.34 for $V_{cm} = 1\text{V}$.

Analog Building Blocs

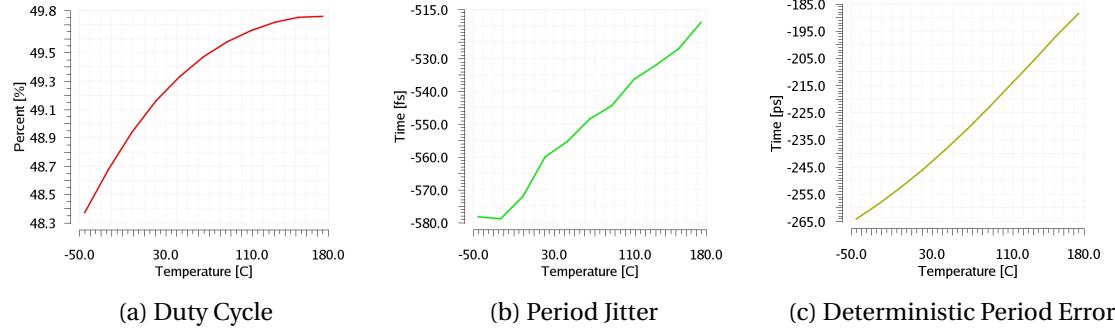


Figure 4.34 LVDS receiver duty cycle and jitter over temperature for $V_{cm} = 1V$

Being sensitive to the input common mode voltage, most LVDS receivers require internal or external fail-safe circuitry so that under a specific link condition or failure the receiver's output will have a known logic condition, usually logic-high. This includes inputs that are either open, floating, or shorted.

In favor of a fully integrated LVDS receiver, the fail-safe circuit is also inside the IC. The easiest realisation of such circuit consists in biasing the 100Ω load by connecting it to supply via resistors. As represented in the Figure 4.35, this fail-safe function is a simple circuit consisting of three resistors connected externally to the receiver input pins such that the current through the 100Ω regenerates a sufficient voltage across it to set the CLK signal to 1. $R_1 + R_2 + R_3$ set the current through R_2 which define the differential voltage while R_3 set the common mode voltage. This approach operates when the inputs are floating. Unfortunately, this circuit introduces an internal offset in normal condition which is unbalanced – degrading the duty cycle and increasing the jitter –. In addition to that, resistors inject power supply noise and thermal noise in the signal path.

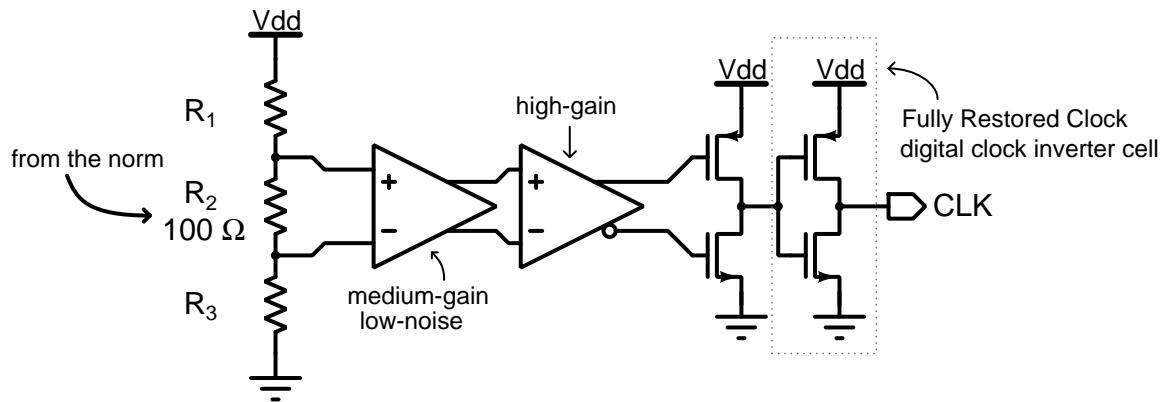


Figure 4.35 In-path fail-safe circuit by the biasing with resistor R1 and R3

The in-path fail-safe design is similar to the external-biasing fail-safe approach, except that here R_1 and R_2 are integrated into LVDS receivers so the offset on VID is now a built-in voltage source. This circuit has been used extensively in some LVDS receivers [173].

To overcome major drawbacks of the prior fail-safe circuit, the failure detection can be in parallel of the signal path. As illustrated in Figure 4.36, this circuit is used in commercial LVDS receivers as in MAX9157 from Maxim Integrated. As shown in this figure, The common mode voltage is compared to a reference voltage V_{ref} usually taken as a $V_{DD} - V_{th}$. In case the inputs are opened or floating, the current injected by the resistor R_1 rises the common mode voltage. The voltage ramps up at rate defined by $(R_1 + R_3)(C_{pad} + C_{parasitic})$.

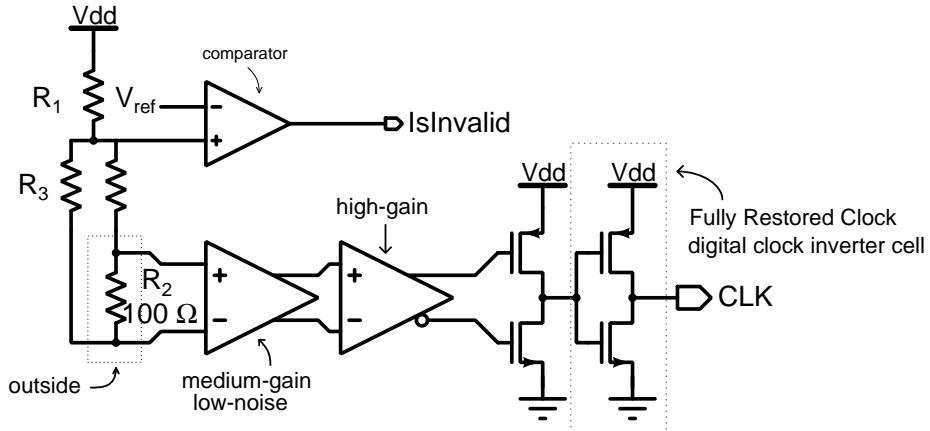


Figure 4.36 Parallel fail-safe circuit implementation

If the link voltage level is higher than the reference, its output goes to logic-high. Then, IsInvalid signal could block the receiver's output through an OR gate and the fail-safe function is activated. This functional design can work properly as long as the common-mode voltage is less than the reference voltage. So, PMOS transistors are preferred to not add an extra common mode voltage limit. Moreover, the parallel-fashion circuit has a much higher noise margin for both the common and differential modes without degradation on the duty cycle and jitter of the input differential signal.

The latter has been designed and sized for a maximum V_{cm} of 1.32 V in typical case, while in the worst speed corner the error is flagged for a common mode voltage of 1.23 V. This process dependence is necessary as the jitter increase as the clock receiver is slower.

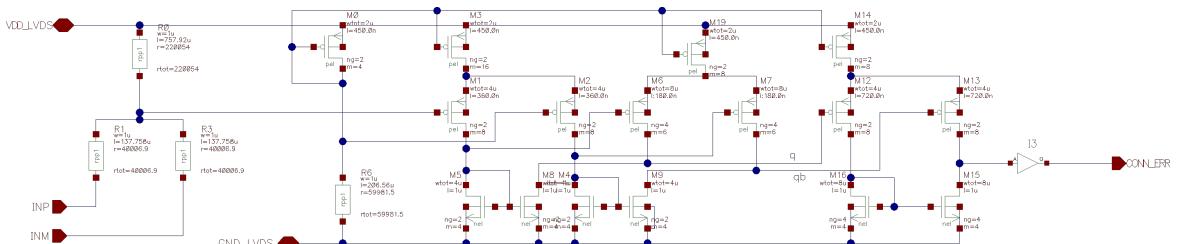


Figure 4.37 Schematic of the parallel fail-safe circuit with its biasing circuit

Analog Building Blocs

With less than 1 ps of period jitter, the proposed LVDS receiver design allows to reach an SNR of 84 dB. This corresponds to an ENOB of 13.6 bits over the full temperature range. In addition to that, the duty cycle at the output of the receiver corresponds to the duty cycle of the input clock with a maximum error of 1.1%. Thus, the LVDS receiver could be used without causing damage in a conversion at 5 clock cycles per sample. At 6 clock cycles per sample, the period jitter is close from the maximum ENOB of the ideal ADC.

In this chapter, we discussed the design of analog building blocks of the ADC: the comparators, the OTA, and the LVDS receiver. After a temperature aware analysis of both a Strong-Arm and a Double-Tail comparator, their design tries to reduce their temperature variation of both the speed and the offset. Post-layout simulation results encourage the use of Strong-Arm comparators for low-power application, and Double-Tail comparators for fully differential application sensitive to the differential kickback. The latter is well suited for charge-redistribution SAR ADCs, while the Strong-Arm comparator found application in the two first stages of the ADC. Concerning the design of the OTA, a gain boosting complementary folded cascode has been selected for its wide-swing, and the slew rate capability of class-AB amplifiers. Its design has been focused on the reduction of the settling error under PVT variations, and the noise reduction afterwards. Despite a large DC Gain variation over temperature, the limiting factor to reach small settling errors is mainly the speed of the OTA. Finally, we designed an LVDS receiver for the specific needs of the ADC. A careful attention is paid to the period jitter limiting the maximum ENOB achievable. However, this chapter only presents simulation and post-layout simulation results. This is not sufficient to reuse them as validated IP blocks.

TESTS AND MEASUREMENT RESULTS

Each block has been considered as an IP so far. In this regard, their performances are cross-checked by measurements over the temperature range of operation: from -40°C to 175°C.

This chapter presents the four different test chips designed during the thesis. These are listed in the table 5.1. The first test chip called DOE_COMP assess comparators. There are two versions of it to characterize the fast comparators needed for the two first stages of our ADC, and for the slow version of them used in the last stage of our ADC. The second test chip evaluates the converter last stage (SAR), and the comparator of in its environment. Called DOE_SAR, its goal is the measurement of the static performances of the SAR ADC. Then, DOE_ADC is the final test chip to evaluate both the static and the dynamic performance of the ADC, all stages combined.

Table 5.1 List of test chips during the thesis and their dates of measurements

Test chip	Test Circuit	Date of manufacture	Date of measurement
DOE_COMP slow/fast		2 February 2017	
	delay oscillator	-	02/06/2018-02/09/2018
	offset feedback	-	not tested yet
	conventional offset	-	not tested yet
DOE_SAR	-	2 February 2017	01/16/2018-02/02/2018
DOE_ADC	-	-	-

The inner chip temperature measurement is therefore crucial for the comparison between simulation results and measures. Being a common component inside every test chips, for the sake of clarity, the chapter begins with its description.

5.1 Internal Temperature Measurement (for all test chips)

Due to the heat dissipation from the silicon to the ambient air, and the self-heating of components, the temperature inside the chip will be greater than the ambient temperature. In order to compare measurement with the simulation results, the temperature inside the chip should be measured.

As presented in section 2.2.1.1 in the Figure 2.15, the band-gap energy of the silicon decreases with the temperature. As the Fermi energy being a fraction of the band-gap energy, the temperature affects the Fermi energy as well with an almost similar variation. Based on the latter, the threshold voltage tracks the variation coming from the band-gap energy due to the temperature.

Tests and Measurement Results

In consequence, the simplest temperature tracker is a diode whose threshold voltage varies in accordance with these explanations.

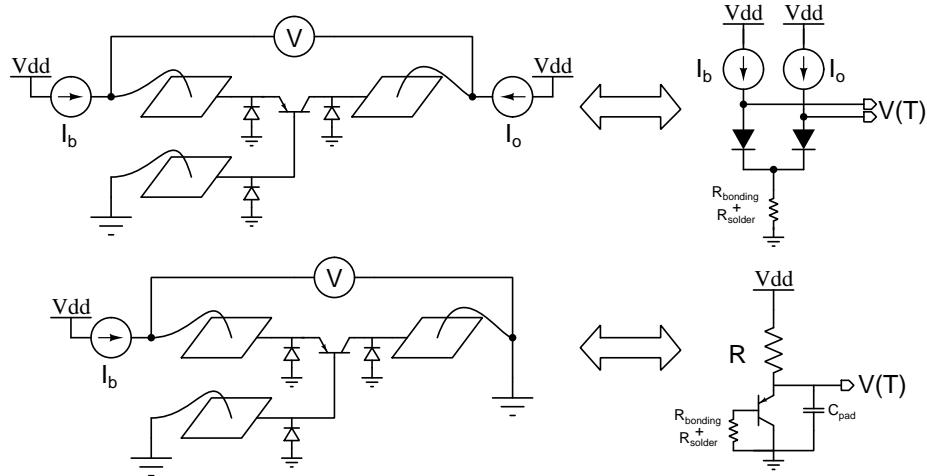


Figure 5.1 Two possible configurations based on a single PNP: Brokaw band-gap or diode mode to sense the internal temperature

The temperature measurement circuit consists in measuring the voltage across a diode with a constant forward current as depicted in Figure 5.1. With a bipolar transistor in diode mode, the voltage across the emitter and the collector follows the Shockley-diode equation and is almost linear with the temperature as in equation (5.1).

$$V(T) = n \frac{k_B T}{q} \ln\left(\frac{I_b}{I_s} + 1\right) \quad (5.1)$$

where n is the number of diodes in parallel, I_b the forward biasing current, and I_s the specific current of the diode.

In practice the biasing current can be either a bench top source meter or a simple resistor. For the sake of simplicity, a resistor has been selected. For a power supply of 1.8 V, simulation performed demonstrates good results for a biasing resistance $R = 33\text{k}\Omega$. Represented in Figure 5.2a, the diode voltage variation is between 220 mV and 350 mV across process corners for a temperature from -40°C to 175°C. The resolution achieved is about less than 1 mK/mV. And Figure 5.2b represents the non linearity of the solution with a resistor. If the differential measurement is preferred one could connect into the Browkaw configuration. Nevertheless, the differential value is highly nonlinear and drops from 16 mV to almost 0 at high temperature. The latter is not selected for our test for its lower resolution.

As the specific current and the current injected to forward bias the diode depend on the process and the temperature, and due to the non-linearity of the bandgap energy, a calibration should be performed before any other test. The voltage would be measured in a controlled temperature

5.1 Internal Temperature Measurement (for all test chips)

environment by steps of 5°C in the temperature range. This operation serves to calibrate the measure and to create a calibration table for the chip tested. For each sample of the chip, a calibration table has to be associated.

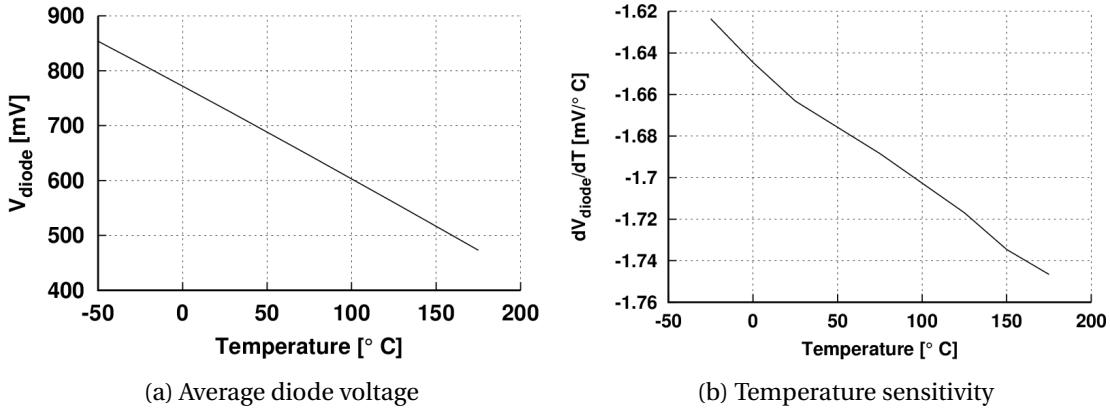


Figure 5.2 Internal temperature voltage sensing results for a best resolution of 0.6°C/mV with a resistor $R = 33k\Omega$ as a current source

A parametric analysis varying the temperature over the range in 15 points gives the results presented in the Figure 5.2. The Figure 5.2a represents the variation of the voltage across the diode with the temperature. The voltage variation is 380 mV with a value of 730 mV instead of 732 mV in theory at 27°C. This confirms the sizing of the design. The plot of the Figure 5.2b represents the sensitivity of the voltage across the temperature range. As expected the sensitivity is about -1.7 mV/°C with a variation that is not linear with the temperature. The choice for a calibration table, instead of an approximate linear transformation to calculate the temperature, is based on the desired accuracy for the application intended. Indeed, with a least square approximation of the linear transform the maximum error would be 2.4 mV or 1.4°C due to the curvature.

5.2 Validation of Comparators in DOE_COMP circuits

Among the available topologies in the literature, the most popular has been investigated in section 4.2: the Strong ARM latch and the Double Tail comparator. With a digital clocking scheme different between the SAR of the last stage and the two first stages of the hybrid ADC, a fast version and a slow version of comparators are targeted. The slow version is well-suited for the SAR for which the offset is the most stringent constraint. While for the two first stages, to wit, the Incremental- $\Delta\Sigma$ and the Algorithmic, require a comparator to make decisions very fast with less constraints on the offset.

For the slow version of comparators, the expected delay should be lower than 3 ns, while the offset does not exceed 10 mV. The hysteresis and differential kickback should be minimized. For the fast version, the delay should be a few hundreds of picoseconds. And the offset is not a big deal since the two first stage combined can be calibrated to cope with up to 50 mV of offset (amplifier offset plus the comparator offset taking into account the capacitive bench).

In consequence, comparators should be tested with respect to the following criteria from -40°C to +175°C:

- The power consumption
- The offset
- The time delay
- The noise

For the comparators test chip, DOE_COMP, there are three test patterns: one to estimate the delay, one to measure only the offset, and a last to estimate the offset, the noise, and the hysteresis. Respectively we called them test pattern A, B, and C. To this, two other measures are required: the power consumption of comparators and the temperature inside the chip.

DOE_COMP evaluates two different comparator topologies by the mean of dedicated test circuits. This test chip counts up to 20 comparators with 16 comparators under the test pattern C, 8 of each topology. Other test patterns can only test one comparator. Therefore, DOE_COMP counts two delay test pattern (Pattern A-SA and Pattern A-DTL) and two Offset Feedback test pattern (Pattern B-SA and Pattern B-DTL) to assess each topology. Due to its novelty, one extra Pattern A circuit is added to the test chip for diagnostic purpose with an external comparator. In consequence, DOE_COMP characterizes 10 Double-Tail latches and 10 Strong-Arm latches with 3 Patterns A, 2 Patterns B, 1 Pattern C and 4 frequency dividers to output high speed signals generated by Pattern A circuits, and to verify the clock connection.

Furthermore, one pad will distribute the clock signal CLK across the offset test circuits and their digital part. The signal of the clock is single-ended and will be generated by using a 100 MHz reshaped sine wave.

5.2 Validation of Comparators in DOE_COMP circuits

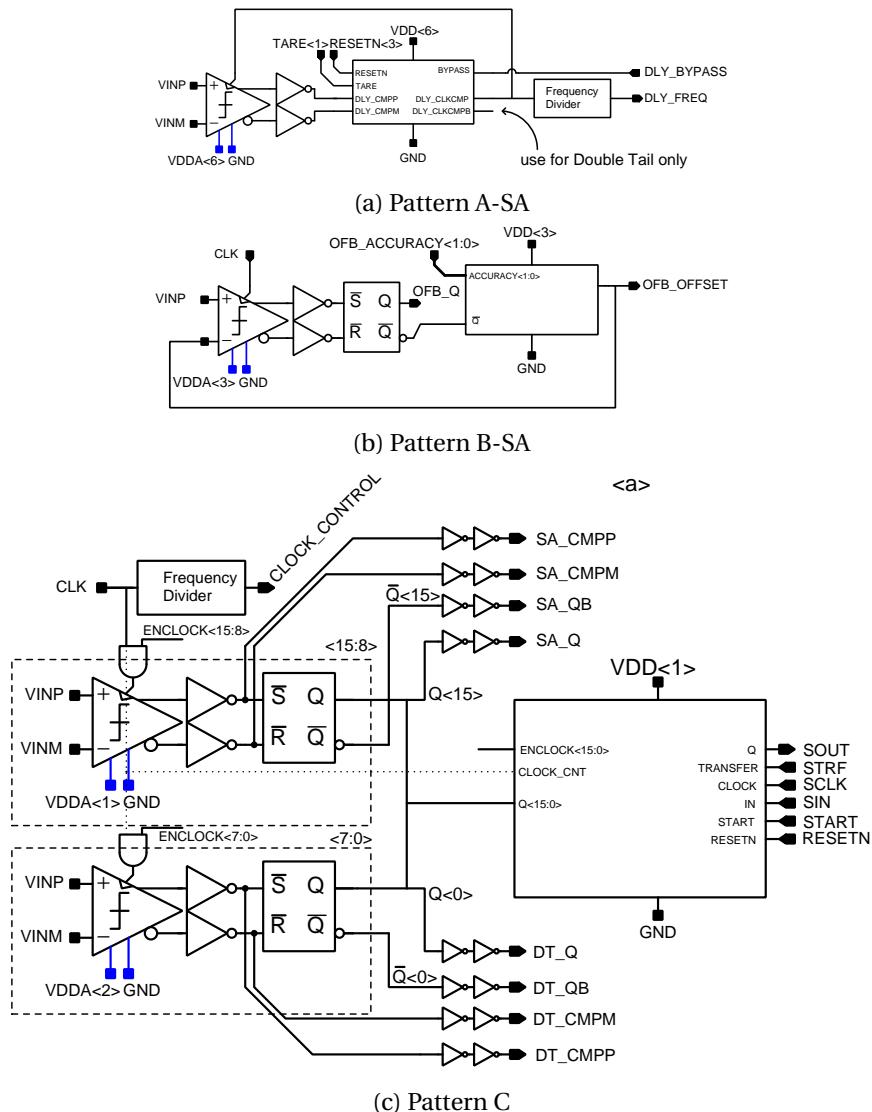


Figure 5.3 Representation of test patterns which will be described in the following sections

Tests and Measurement Results

For signal generation the Tektronic AFG3102C is at our disposal. On the PCB, a clock driver and an impedance adaptation are assumed close to the comparator test chip. Inside the chip, the clock signal reshaped with a Schmitt trigger is distributed differentially across the test chip (CLK and CLKB). A CLOCK_CONTROL signal is output in order to check to good-connexion of the clock signal to test blocks.

The digital signals are generated by an NI-USB 8452 and drive directly pads of the test chip. Inside the IC, those signals are reshaped with a Schmitt trigger. Finally the test chip has 56 pads in total connected to the footprint of a CLCC68 package.

5.2.1 Power Consumption

To supply DOE_COMP, one power supply is connected to the comparators while another is connected to the remaining circuits. As both topologies of comparators are tested, we thus separate the power supplies of comparators of different topology to limit the interference in results. As presented in table 5.2, there are 12 pads for supply connections: VDDA<6:1> and VDD<6:1>. Therefore, we are able to measure both the comparator power consumption and the test circuit consumption without interference of one over another. For the sake of simplicity, there is one ground pad for all comparators, and one ground for the remaining circuits in DOE_COMP. These two forms a star connection to have the same reference between comparators and test circuits.

Table 5.2 Test pattern implemented to assess each comparator topology

Test Pattern	Comparator Topology	Function	Power Supply comparator	Power Supply test circuit
Pattern A	Strong Arm	Measure the delay and the time to reset	VDDA<6>	VDD<6>
	Double-Tail		VDDA<5>	VDD<5>
Pattern B	Strong Arm	Measure the offset by using a feedback loop	VDDA<3>	VDD<3>
	Double-Tail		VDDA<4>	VDD<4>
Pattern C	Strong Arm	Measure the offset by using the output CDF ¹ for a given input voltages	VDDA<1>	VDD<1>
	Double-Tail		VDDA<2>	

To measure the power consumption, the power supply connections to DOE_COMP are cut. In normal operation jumpers connect them. For the consumption measurement, an amp-meter takes the place of a jumper.

To limit the variation on power supply pads from the chip consumption, an external capacitor of at least 1 μF should be connected to each power supply pads. The power supply should be able to provide 20 mA at 1.8 V for digital pads and a peak internal power consumption of 35 mA. For tests, the power consumption of one comparator is in average 20 μW at 1.8 V. This implies to be

¹cumulative density function

able to measure an average current in the order of $11 \mu\text{A}$. A Keithley-2000 series is appropriate with a possible accuracy in the sub micro-amps range. For measures, while only one comparator is connected in the Pattern A and B, the power supply of the Pattern C is connected to 8 comparators.

5.2.2 Test Pattern A: Delay Measurement Circuit

5.2.2.1 Bibliography

From an junction temperature of -40°C to $+175^\circ\text{C}$, the experimental measurements of the propagation delay pose an interesting challenge. Earlier works have used simple as well as complex circuits for delay extraction.

The easiest solution would be to externalize the clock and the outputs of the comparator to extract the delay by a high speed high resolution measurement device. Unfortunately, outputs drivers consumes much chip area, add extra delay, bond-wires inductances would alter the signal and the delay estimation too, and different length of cables between the clock of reference and the output generates unconditional error prone measurement system.

For a simple solution of delay measurement, one can generates a DC voltage proportional to the delay. In the case of a clocked comparator, continuous decisions made are averaged by a low-pass filter to externalize a DC voltage. Difficulties occur as a pulse indicates a “decision made” event whose width is sensitive to the parasitics and PVT variations. While the PVT variations can be alleviated by the employ of mathematical expressions for differential output pulses as in [174], it suffers of mismatch in parasitics seen by XOR cells within the pulse of reference generator and the generator of the “decision made” pulse.

For instance, high precision time interval measurement systems are commonly used in Telecommunications, nuclear science, frequency synthesis, measurement devices such as oscilloscopes and logic analyzers, and time-of-flight cameras are heavily relying on time-to-digital converters (TDC). In a nutshell, a TDC is made with a counter and delay line interpolation [175]. Such converters have a limited achievable accuracy in a technology based on the small delay cell (an inverter), the quantization noise, and the non-linearity in the time interpolation. The latter coming from variation in the delay elements of the smallest delay cell, as the cascade of delay cells increase, the integral non-linearity grows such that accurate measurement of large delay is challenging.

In contrast, measurement circuits based on Vernier delay line can achieve fine delay resolution.

Practical implementations of the delay line and interpolation is depicted by Figure 5.4. J.P. Jansson *et al.* uses the differential implementation represented in this figure. To estimate the delay a synchronous counter performs a coarse estimation of the delay while the recorded state of the

Tests and Measurement Results

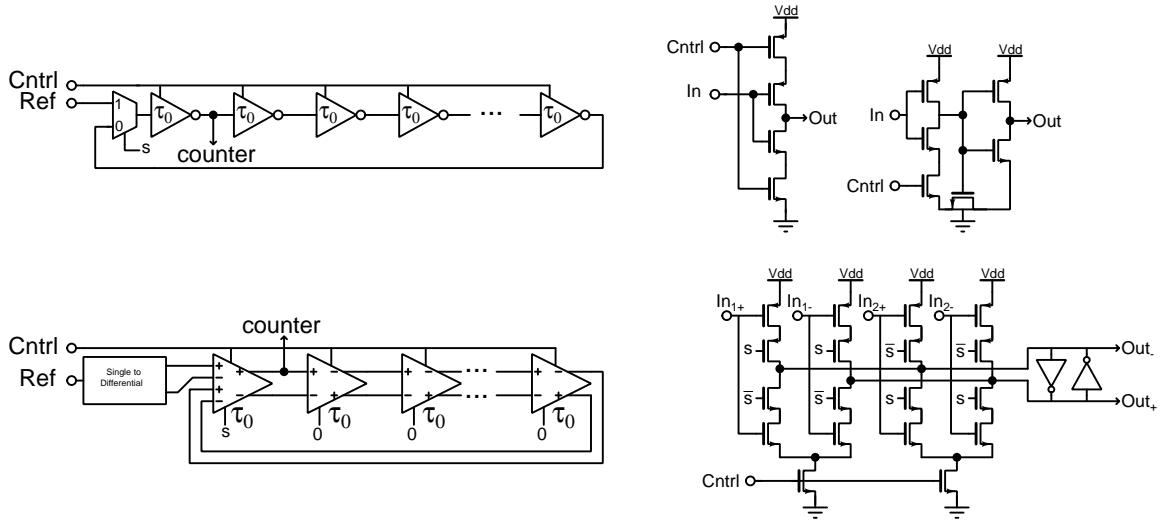


Figure 5.4 Some delay line implementation for the delay estimation and practical implementations of delay cells

delay line divides the clock of the counter into pieces of ΔT [175]. The recorded state of the delay line corresponds to the value stored by DFFs of the positive output of these delay cells.

That said, averaging results either in the time domain or by several TDC running in parallel mitigates the non-linearity: the improvements being inversely proportional to the square root of measurements. However, they are sensitive to PVT variations [176, 177] such that calibration is mandatory. Finally, this method does not timely occupy a silicon footprint for built-in self-test.

Finally, the ring oscillator can also be employed to estimate the delay as in [178] wherein perused different oscillators related to the device under test can accurately calculate the delay of element under test. In the case of [178] the delay of Through-Silicon Via for 3D IC are measured. This solution fit within a small silicon area with a large measurement range. Unfortunately, as the number of oscillators increase, mismatch of their instance is averaged and the calculus of the delay becomes even more tedious. Furthermore, it is difficult from the design phase to estimate the accuracy of measurement.

5.2.2.2 Delay measurement Principle

Therefore, we proposed a circuit to reliably measure the comparator's delay with a differential measure of frequency generated by an auto-oscillator with an estimation of the measurement accuracy early in its design phase. The generated frequency is then divided by an arbitrary ratio N to be measured. We choose $N = 64$ to prevent high speed signal routing consideration.

The auto-oscillator generates a first frequency of reference without the comparator only based on digital cells. Then, with the same digital cells configuration the frequency is generated by fully

5.2 Validation of Comparators in DOE_COMP circuits

restored comparator's outputs in response to the comparators input voltages when the frequency trigger the comparator.

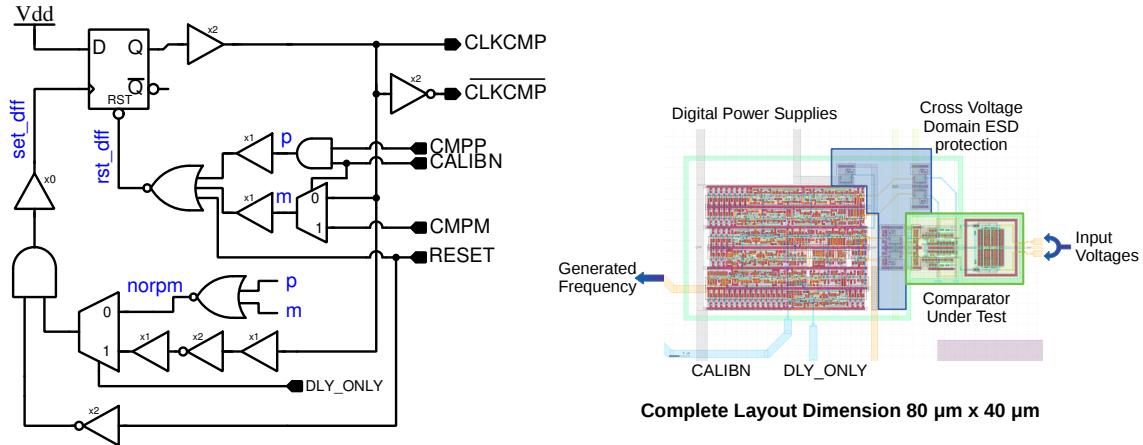


Figure 5.5 Schematic of the proposed measurement circuit and the delay test dimension

Figure 5.5 represents the auto-oscillator circuit connected to the comparator under test. Build around a central D-Flip-Flop generating our frequency CLKCMP, an inverter is used to generate the complementary clock with some delay (≈ 70 ps) to test the Double-Tail comparator.

CALIBN signal allows us to choose the generated frequency: the frequency of reference or the frequency with the comparator to extract the delay. As the comparator requires some time to reset, the required time to reset can also be extracted. To select whether we need to extract only the delay or the delay and the reset time of the comparator DLY_ONLY shall respectively be set to '1' and '0'. And the RESET signal sets the CLKCMP signal to '0' which in turn resets the comparator under test. To change from the generation of one frequency to another, a reset is necessary.

For the sake of clarity, we comply with the following frequency names for each configuration possible:

DLY_ONLY	CALIBN	Frequency Name
1	0	$F_{CLKCMP1}$
1	1	$F_{CLKCMP2}$
0	0	$F_{CLKCMP3}$
0	1	$F_{CLKCMP4}$

When the signal RESET is released, the reset signal of the DFF is disengaged and CLKCMP keep its state. Few picoseconds later, the clock signal of the DFF rises to '1'. This edge triggers the DFF which sets its outputs Q to '1', as depicted by the Figure 5.6 a and b. In consequence, the comparator makes a decision. The DFF is triggered either by the nor of p and m signal if CALIBN is '1' or by the inversion of CLKCMP if CALIBN is '0'. The DFF is reset, and the oscillations begin.

Tests and Measurement Results

For DLY_ONLY set to '1', the clock of the DFF (set_dff) is a delayed \overline{CLKCMP} . Therefore, the time of CLKCMP spend at zero is fixed and PVT dependant. While, for a DLY_ONLY signal set to '0', the signal set_dff depends from the generated pulse of the nor gate. In that case, the time that CLKCMP spent at zero is defined by the speed of the comparator to reset.

The frequency difference between the two modes defined by CALIBN corresponds to the mismatch of the MUX inputs selecting either CMPM or CLKCMP, and the delay of the comparator to make a decision. While, the difference introduced by the two states of DLY_ONLY corresponds to the difference of the delay and the time to reset the comparator. Thus, the proposed circuit is able to extract the delay of the comparator or the delay and the time to reset the comparator.

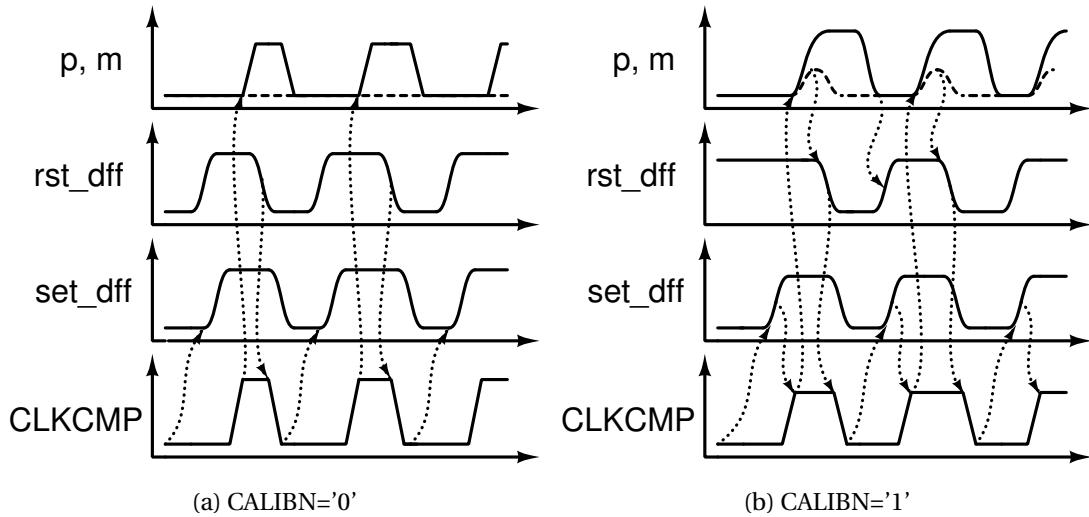


Figure 5.6 Measurement circuit transient behavior

As the same path is used for the generation of the frequency of reference and the frequency with the comparator under test, the PVT dependence of digital cells is the same in either generation case. Therefore, the differential measurement of the frequency cancels the PVT variations.

The calculation of the frequency in the normal operation mode (CALIBN='1' and DLY_ONLY=RESET='0') is given by the equation (5.2).

$$F_{CLKCMP4} = \frac{1}{N} (T_{delay} + T_{set} + T_{rst} + T_{reset})^{-1} \quad (5.2)$$

where T_{delay} is the delay of the comparator, T_{reset} the time the comparator takes to reset, and T_{set}/T_{rst} the time of the digital circuit to react. In detail, $T_{set} = 2T_{MUX} + T_{NOR} + T_{AND2} + T_{DLY2} + T_{DFF} + T_{BUX2}$ and $T_{rst} = T_{MUX} + T_{DLY} + T_{NOR3} + T_{DFF} + T_{BUX2}$.

In the calibration mode (CALIBN='0' and DLY_ONLY=RESET='0') the frequency is given by equation (5.3).

$$F_{CLKCMP3} = \frac{1}{N} (T_{set} + T_{rst})^{-1} \quad (5.3)$$

The sum of the delay and the reset time is thus given by the equation (5.4).

$$T_{delay} + T_{reset} = \frac{1}{N} \left(\frac{1}{F_{CLKCMP4}} - \frac{1}{F_{CLKCMP3}} \right) \quad (5.4)$$

When the DLY_ONLY signal is set to '1', the reset time of the comparator no longer matter, and T_{reset} of the equation (5.2) and (5.4) is 0.

$$T_{delay} = \frac{1}{N} \left(\frac{1}{F_{CLKCMP2}} - \frac{1}{F_{CLKCMP1}} \right) \quad (5.5)$$

$$T_{reset} = \frac{1}{N} \left(\frac{1}{F_{CLKCMP1}} + \frac{1}{F_{CLKCMP4}} - \frac{1}{F_{CLKCMP3}} - \frac{1}{F_{CLKCMP2}} \right) \quad (5.6)$$

5.2.2.3 Design Criteria

In this design, both set_dff and rst_dff are driven by the same signals: p and m . To ensure the stability of the circuit the race condition to respect is defined by the equation (5.7) if DLY_ONLY='0'

$$T_{DLY} + T_{NOR3} + T_{margin} < T_{NOR2} + T_{MUX2} + T_{AND2} + T_{DLY2} \quad (5.7)$$

and by equation (5.8) if DLY_ONLY='1'.

$$T_{MUX} + T_{DLY} + T_{NOR3} + T_{margin} < T_{INV} + 2T_{DLY} + T_{MUX2} + T_{AND2} + T_{DLY2} \quad (5.8)$$

And this over the process and temperature variation which limit the measurement delay range of the circuit.

5.2.2.4 Measures

The basic setup for the test in this section is depicted by the Figure 5.7. This includes four power supplies, a frequency meter, a multimeter, an optional oscilloscope, and an optional current source.

Among power supplies, two are for the power distribution. One a 1.8 V for the core and one at 3.3 V for the level shifting needed of the digital signals connected to NI-USB boxes. The remaining two are dedicated to the input voltages applied at comparator's inputs.

Tests and Measurement Results

The frequency meter should be plugged in the BNC signal of at the top of the motherboard named SA_DLY_FREQ1 and DT_DLY_FREQ1.

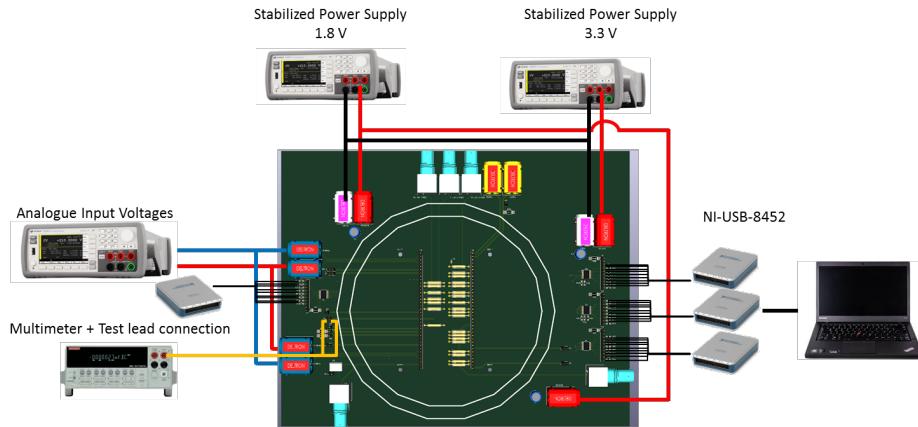


Figure 5.7 Bench-Top installation to measure the delay of comparators

Either a homemade software or LabView is required to drive the NI-USB boxes. In our case, they are driven by the Labview API provided into a C code, allowing us to drive pins of SPI port as DIO.

For all possible configurations of CALIBN and DLY_ONLY signals, we measure the frequencies generated for the following temperatures: -40°C, -25°C, -10°C, 0°C, 27°C, 85°C, 100°C, 125°C, 150°C, and 175°C.

Since by design we fixed the frequency divider to be $N = 64$, the delay is given for DLY_ONLY = '1' by

$$T_{delay} = \frac{1}{64} \left(\frac{1}{F_{CLKCMP2}} - \frac{1}{F_{CLKCMP1}} \right) \quad (5.9)$$

And the sum of the delay and the time to reset is given for DLY_ONLY = '0' by

$$T_{delay} + T_{reset} = \frac{1}{64} \left(\frac{1}{F_{CLKCMP4}} - \frac{1}{F_{CLKCMP3}} \right) \quad (5.10)$$

Figure 5.8 represents the post-layout simulation results of the delay against the measurements results of the delay estimation circuit for three different samples. We notice that first, the delay after extraction of parasitics is superior to measured values for some chips. This can be explained by three main reasons. First, the transistor in the process from which samples are coming from can be more doped than the typical case. Second, the voltage which trigger cells in the circuit is not the same level as the logic level used in the Section 4.2.3. And third, a 5 kHz inaccuracy while measuring the delay generate a systematic error of 13 ps for an output frequency around 2.5 MHz.

From sample to sample, we experiment an error which varies from less than 10 ps to 107 ps in the worst case, at 175°C which correspond to an inaccuracy of 25 kHz. Or in other terms, an error

5.2 Validation of Comparators in DOE_COMP circuits

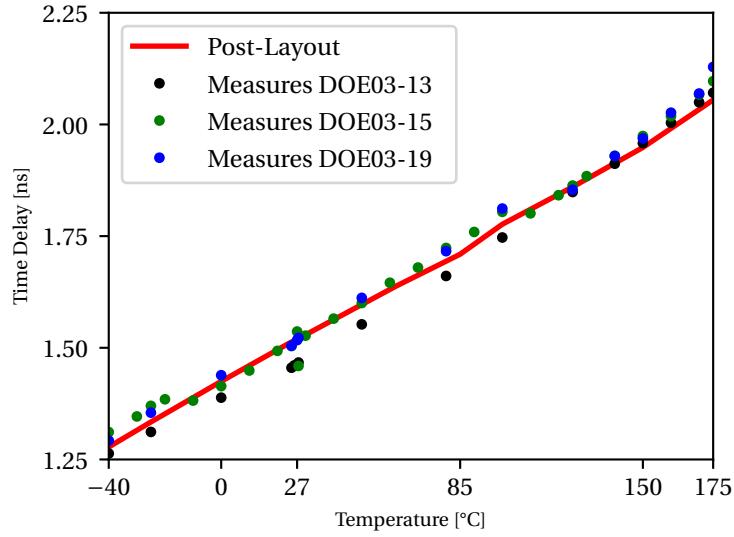


Figure 5.8 Post-layout delay results versus the estimated delay from the new proposed circuit

of 1% on the frequency. Despite that, the circuit provides results with an absolute maximum error of 60 ps without correction.

Then, the proposed delay measurement circuit is compared to existing circuits to measure the delay of analog component. The comparison in Table 5.3 highlights the small footprint of the proposed solution for a resolution in the order of few picoseconds which competes with traditional Time-to-Digital converter (TDC). Moreover, the proposed circuit achieves the best power consumption known. Nevertheless, toggling at very high frequency induces large transient peaks detected up to 1 mA.

Table 5.3 Comparison of delay measurement circuits

	[175]	[176]	[179]	[180]	proposed
technology [nm]	350	40	350	65	180
area [$\mu\text{m} \times \mu\text{m}$]	2500×3000	1000×300	610000	120×130	40×30
resolution [ps]	12.2	100	0.61	2	5^{\dagger}
max error [ps]	13	50	4.5	3.5	60
measurement range [μs]	202	0.003	327	NC	NA
temperature range [°C]	$-40 - +60$	$-40 - +125$	$-30 - +70$	$0 - +100$	$-40 - +175$
power consumption [mW]	40	NC	80	0.78	0.52

Measurements results confirm the operation of the proposed delay measurement circuit. With a reduced power consumption and a small area overhead, this circuit is well suited for advanced on-chip assessment of comparators over a large temperature range. This circuit has the potential

[†]the resolution of the circuit depends on the resolution of the frequency meter. The resolution given corresponds to a frequency divider of 64 and a frequency meter able to differentiate 6.01 MHz and 6 MHz

Tests and Measurement Results

to estimate the offset as the input voltage difference for which the delay measured is the greatest. Furthermore, the measurement is expected to be only limited by the external frequency meter. Besides that, more accurate delay results could only be achieved with a TDC. And this circuit is surely a source of noise and EMC near sensitive components.

5.2.3 Test Pattern B: Offset Measurement Circuit by feedback method

5.2.3.1 Principle

This solution consists in regulating one input voltage of the comparator such that the comparator always has difficulty to make the difference. The differential input voltage applied is the offset. This circuit is an hysteretic control loop based on [181].

The advantage of such a direct control over the output voltage is the speed of the control loop. When the output voltage changes due to a transient, the time it takes for the control loop to begin to react is limited only by the propagation delays in the comparator and gate driver. There is no low-bandwidth error amplifier for an error signal to travel through. Thus, the hysteretic topology is the fastest control topology. This test allows to easily measure the offset for different common-mode voltage.

Nevertheless, the main disadvantages of this method are the slow convergence (few milliseconds) to the actual threshold value considering mismatch and PVT variations according to [182] with the intrinsic noise of the comparator which toggle outputs. Moreover, one circuit is able to test only one comparator at the same time.

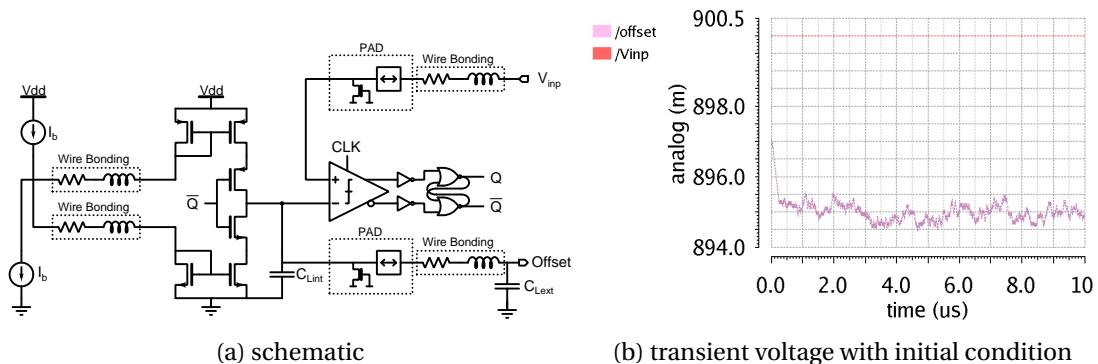


Figure 5.9 Test bench for the offset simulation which including pads and wire bonding with the noisy transient simulation for a comparator of reference

The Figure 5.9 a represents the schematic view of the test while the Figure 5.9 b depicts the signal seen over the simulation of a comparator with 5 mV offset and 1 mV rms noise. This test circuit has only one mode and is always on. By beginning with a reference voltage V_{inp} at 0 V, the offset voltage after few milliseconds will be at zero volt too. Then, the reference voltage steps up to

the desired common-mode voltage. Therefore, the comparator will detect the difference between the two, and its memorized output will be 1. So, the charge pump circuit in the voltage generation bloc raises the OFB_OFFSET voltage. With one transistor in saturation while the other is blocked, the current to load the capacitor is approximately the current defined by the I_b over a full clock period of CLK. This pursues until the offset voltage is greater than the reference voltage. In this case, the current that charges the load capacitor is $-I_b$. Thence, the offset voltage starts to oscillate around the real input referred offset of the comparator.

5.2.3.2 Bloc Description

As represented in Figure 5.9 a, this circuit takes as an input two currents of reference which control the slewing of the feedback voltage OFFSET. In addition to that, a reference voltage called V_{inp} corresponds to the common-mode voltage at which we expect to test. The clock provided to the comparator control makes the comparator start a decision at its rising edge, while the comparator is reset when the clock is low. An SR-latch memorizes the output of the comparator under test before the reset. From the decision, the charge pump charges/or discharges an internal capacitor of 1.8 pF. The voltage generated OFFSET is used as the second input voltage of the comparator, and is connected to an output pad itself connected to an external capacitor to limit oscillations. Concerning the power supply, only one VDD and GND pins are needed. The voltage of the power supply is 1.8 V.

5.2.3.3 source of perturbations

In this circuit the external source of perturbations is the current source. Let us suppose the comparator operates in the same condition it will in the ADC, to wit $V_{DD} = 1.8$ V and $F_{CLK} = 100$ MHz. The comparator makes a decision every 10 ns. Due to the latency in the feedback loop, the variation of the offset voltage ΔV is thus defined by the slewing: $\Delta V = \frac{I_b}{C_L F_{CLK}}$.

In a first approximation, the error committed by the circuit with a $C_L = C_{Lint} = 1.8$ pF, $I_b = 500nA$ is 1.38 mV around the real value. In order to match the requirement of the 500 μ V around the offset, the minimal capacitance should be at least 5.3 pF. This can be easily achieved by connecting an I/O pad directly to the probe of the measurement device and adding an external capacitor out of the chip of 2.2 pF: $C_L = C_{Lint} + C_{probe} + C_{Lextr}$. This limiting the oscillations, but not annihilating them, we are interested in only the average value of the differential input.

Concerning phenomena from the comparator, the hysteresis will impact the desired voltage measurement. Indeed, having a different threshold voltage due to previous state of the comparator, the measured offset voltage will be oscillating between the two thresholds of the hysteresis. If the slope of the generated offset is very slow such that the variation peak-peak between two clock rising edge is less than the hysteresis, this phenomena is detected. If not, the average value still

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provides the information of the offset which is close to the average of the hysteresis threshold value.

Another phenomenon due to the comparator decision occurs: the kickback. The single-ended kickback is important since it will drop the voltage across the load capacitor, even if, the amplifier is always charging the capacitor. Therefore, the size of the capacitor is an important decision. With a single-ended kickback of 500 mV over a 100 fF capacitor, by applying a rule of three, the kickback seen on a 1.8 pF plus an I/O pad will be 16 mV. The amplifier limiting the drop, this results in a 14.7 mV voltage drop on the offset voltage.

5.2.3.4 Post-Layout Results

Since neither the kickback nor the hysteresis is modelled in the comparator of reference, the information of whether the offset feedback circuit is able to cope with these phenomena is not known. Therefore, a post-layout comparator replaced the one of reference. Moreover, the schematic of the comparator and the extracted version of comparators have an adjusted offset around 5 mV to compare with the previous simulation results in Figure 5.9. This allows us to compare only the impact of the phenomena not taken into account by the reference comparator. To wit, parasitic and the intrinsic hysteresis introduced by layout mismatch.

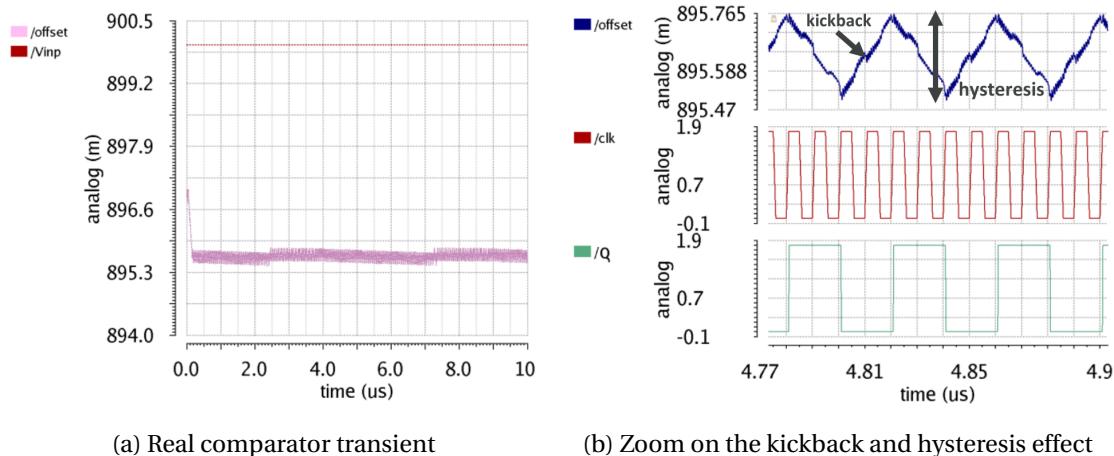


Figure 5.10 Hysteresis and kickback effect on the offset feedback circuit at 27°C

The transient offset voltage with the clock and the decision of the comparator alongside are depicted by the Figure 5.10. The results are for ambient temperature at 27°C. Since the current switching is low the voltage variation is fully delimited by the hysteresis of the comparator under test, to wit 325 µV. With a large capacitive load split inside the chip and outside, the kickback is limited to few microvolts even for a clock at 100 MHz.

Running a Monte-Carlo analysis of comparators designed after parasitic extraction, the offset statistic of a slow double-tail comparator is compared to the traditional method of clocked com-

5.2 Validation of Comparators in DOE_COMP circuits

parator extraction used in Section 4.2.3. The Table 5.4 presents the result under a 6σ process and mismatch parameter variation at three different temperatures with 50 samples each.

Table 5.4 (Gaussian 6σ) Monte-Carlo analysis results of the extracted offset for the double tail comparator with the current offset simulation

Temperature/Offset	Min [mV]	Max [mV]	Mean [μ V]		σ_{offset} [mV]		ΔV [mV]
			Circuit	Ref	Circuit	Ref	
-50°C	-1.89	2.72	269	290	1.27	1.73	1.16
27°C	-2.14	3.47	570	620	1.39	1.84	2.33
175°C	3.33	6.6	1000	1410	2.29	2.44	4.64

The circuit is relevant for low-temperature measurement with an accuracy of 50 μ V. Owing to thermal noise and hysteresis at high temperature the accuracy of the circuit decrease to 400 μ V on the mean. A possibility to enhance results is by the averaging of the offset voltage lasting longer in time than 1 μ s (1000 comparator decision) to mitigate the transient noise in measurement with twice more samples. Unfortunately a lack of time available for the tests did not permit us to collect experimental data. This is scheduled to happen later on.

5.2.4 Test Pattern C: Conventional Offset, Hysteresis, and Noise measurement

At our best knowledge, Test Pattern B has only been used in simulation [181]. In order to compare with the most common methodology to measure the offset, this conventional method has also been implemented in DOE_COMP. In addition to offset measurement, this circuit allows the extraction of the comparator's hysteresis and its intrinsic noise.

From the design of comparators, the target offset is as close as possible from zero with a standard deviation of 3 mV. Based on that, the accuracy needed is less 500 μ V¹ for a maximum error of 5% on the standard deviation.

5.2.4.1 Principle

As represented in Figure 5.11, this solution consists in counting the number of ones and zeros generated by comparators under test, for each differential input voltage distributed evenly around the common mode voltage. Therefore, each differential input voltage is associated with a ratio of ones counted over the maximum possible values in the test time. This corresponds to averaging the comparator output for each differential input voltage. By sweeping the input voltages of the comparator, we get an S-shaped probability distribution.

¹see Appendix F for the details of the calculation

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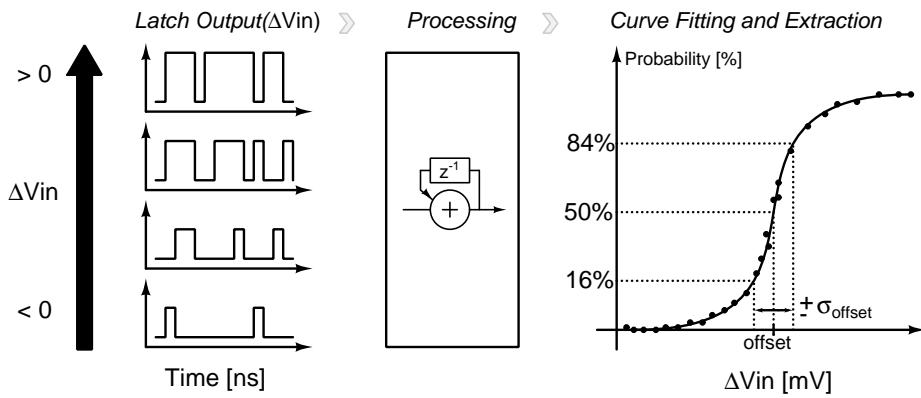


Figure 5.11 Typical principle to measure the offset of comparators based on the variation of the differential input voltage

Without offset, the inflexion point of the curve plotted should be equal to the common-mode voltage: $\Delta V_{in} = 0$. And a small shift corresponds to the offset. This solution is the most common for measurement of the offset [183–185].

The advantage of such circuit is the resilience to cope with the thermal noise. At a given clock frequency, the smallest differential input voltage is set by the one who test. But for a tiny differential input, the noise will trigger the comparator under test, and its outputs are either 1 or 0. An assumed white thermal noise will produce an evenly repartition of 1 and 0, thence only few bits over thousands shift the probability to output one. This makes a smoother transition from quasi-zero to quasi-one probability. This results only in a change of the standard deviation.

From the density function to output a one, we fit the data with the cumulative distribution function of a Normal distribution. The fitting will average the error due the white Gaussian noise while it estimates the average and the standard deviation of the offset. The average, equal to the inflexion point of the curve, corresponds to the offset, and ideally occurs for a probability of 50%. And the standard deviation of the offset corresponds to the noise contribution. There is no preferred algorithm for the fitting, so we used Levenberg-Marquardt to minimize the error committed on the fitting.

Moreover, applying this procedure over several comparators allows us to calculate the average of the offset and its standard deviation with respect to process and mismatch. This time, the probability curve should be the average of each comparator probability curve. The average offset is thus defined by the differential input voltage which corresponds to the 50% of the new probability. And the standard deviation is extracted from the 68.27% probability range around the new inflexion point.

5.2.4.2 Curve Fitting Limitation

For a comparator without hysteresis, the probability to output a one for each ΔV_{in} is similar to what is represented in the Figure 5.11. With an hysteresis, Figure 5.12, the transition of probability will be slightly sharper. In order to highlight the presence of hysteresis, the differential input voltage should be progressively changing from negative values to positive values then from positive values to negative values. The presence of hysteresis will demonstrate two S-shapes shifted from one to the other. The ΔV shift of the offset value corresponds to the hysteresis while ΔV_{in1} and ΔV_{in2} represent the offset voltage. To correctly estimate, the data should be split to have one fitting when the differential input is increasing, and one when the differential input is decreasing.

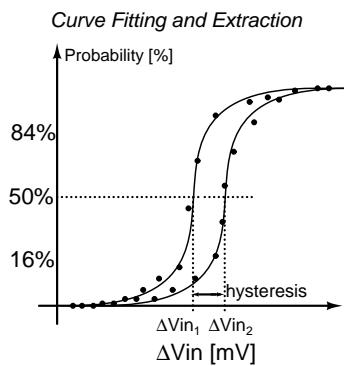


Figure 5.12 Measurement of the hysteresis by sweeping back and forth the input voltages of comparators

About the choice of the input voltage, the input referred offset is in the ± 10 mV range. Therefore, the ΔV shall be from -20 mV to +20 mV to ensure some margin. And to respect the requirement on the accuracy, a step between two consecutive differential input voltages should be less than 500 μ V.

From a fitting point of view, the less noise there is, the fewer the number of points is in the transition. In consequence, the step between two consecutive differential input voltages might not be sufficient to estimate the noise accurately. By simulation, the standard deviation of the noise is 480 μ V rms such that a 3σ transition is expected to have 9 points.

5.2.4.3 Bloc Description

The analogue part of the conventional test circuit is represented in the Figure 5.13. This part is made of 16 comparators with their inverters and SR-latch next to them. Among those comparators, there are 8 Strong Arm and 8 Double Tail comparators taking their decision at the same time. Inverters decouple the comparator output from the SR-latch who memorized the output. The inverter's outputs are considered to be analog, while the output of the SR-latch is assumed to be digital.

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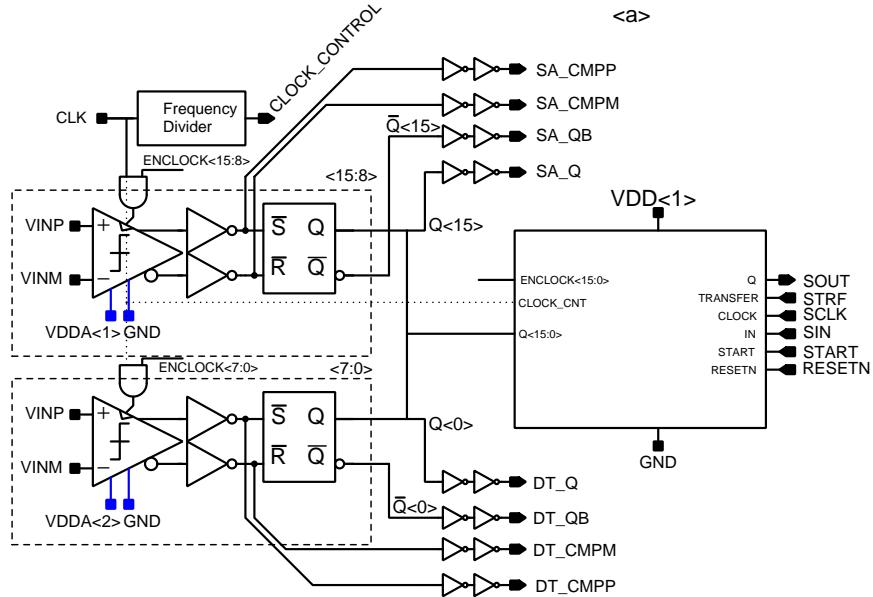


Figure 5.13 Conventional offset measurement circuit to measure the offset, the hysteresis and the noise of 16 comparators (8 Strong-ARM and 8 Double-Tail)

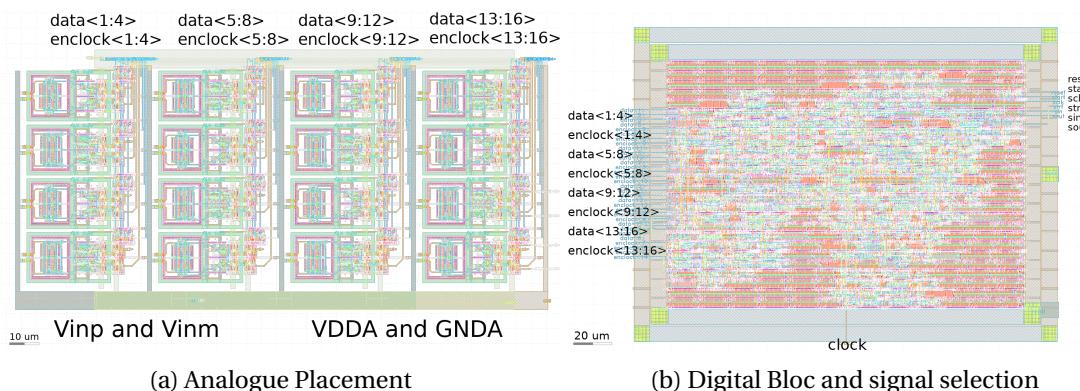


Figure 5.14 Comparator test chip overview with 20 comparators to test the delay, the offset of the both comparator topologies. One extra delay test circuit is for diagnostic purpose

5.2 Validation of Comparators in DOE_COMP circuits

The interleaved repartition into even index for strong arm and odd index for double tail, in Figure 5.14 a, prevents the performance degradation of one comparator in favor of the other by having the same voltage drops for both topologies.

As represented in Figure 5.14 b, the outputs of the 16 comparators enter the digital bloc which selects which one is counted. To configure which comparator is selected, 4 bits are transferred through SIN with respect to its clock SCLK. Then 16 bits are transferred in order to select which comparators are taking decisions which control the ENCLOCK signals. The last bit is validated by a STRF pulse which reply by sending the output of the internal counter of 1s.

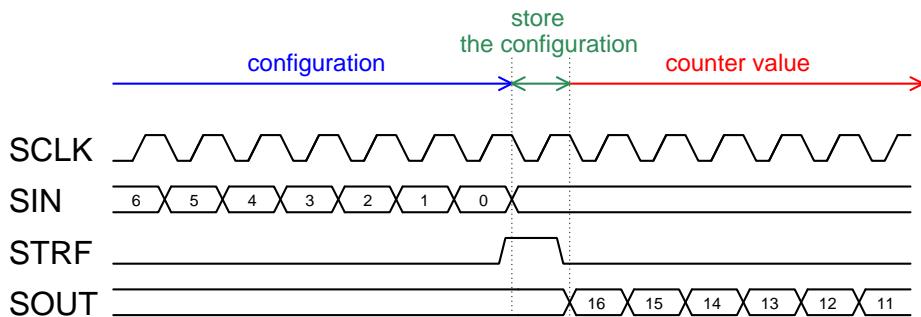


Figure 5.15 Configuration signal to validate the configuration and the counter value reading

5.2.4.4 Simulation Results

In order to verify that the probability model chosen is correct, the input file of the post-processing script is obtained by simulation of the test bench with a comparator of Reference. While one input voltage is set to the common mode voltage, the other is a triangle waveform from $V_{cm} - 20mV$ to $V_{cm} + 20mV$ by step of 0.5 mV. The expected offset and the expected standard deviation of the offset are respectively 5 mV and 1 mV with an hysteresis of 1 mV. The simulation at 27°C, gives the results presented in the Figure 5.16.

In simulation, the average offset is as represented in Figure 5.16 a. The estimation for each comparator gives 5 mV as expected. And since there is only the noise which impact the slope of the rising probability of one, the standard variation should be equal too. In the Figure 5.16 b, the estimation of the standard deviation is around this value. Therefore, the methodology applied extracts correctly the information of the offset for the comparator of reference.

Then, the comparators are changed for a Double-Tail comparator as done in other tests. First, the impact of the temperature is studied for 5 temperatures linearly distributed in the -50°C – +175°C range. Nothing is changed between the simulation of the reference comparator and this test. The results for the temperature variation are presented in the Figure 5.17 which represents the offset variation, its standard deviation, and the hysteresis with respect to the temperature for the

Tests and Measurement Results

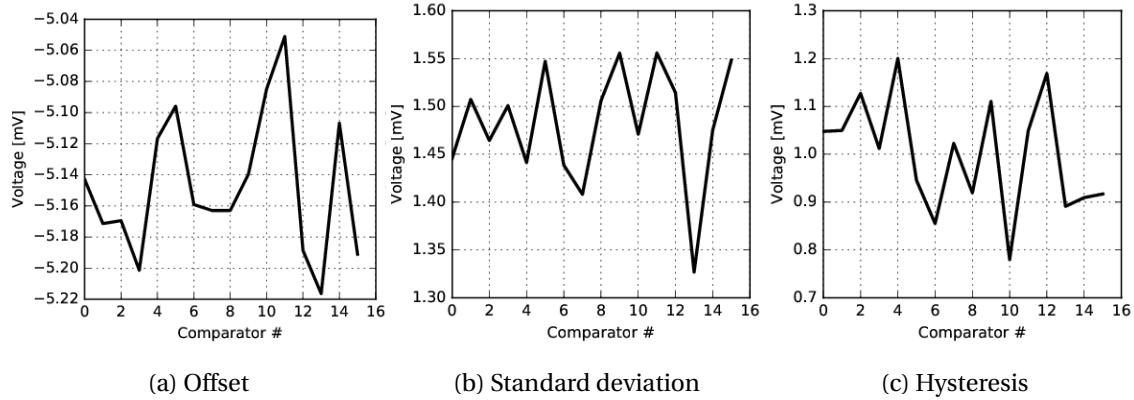


Figure 5.16 Extracted offset and standard variation of the offset for the comparator of reference at all positions

slowest version of the Double Tail. A Gaussian variation of parameters due to mismatch around this corner is performed.

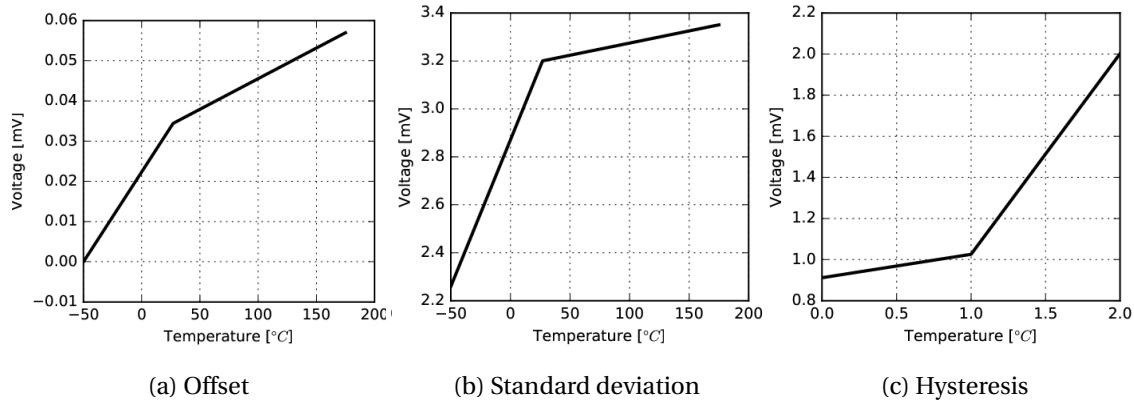


Figure 5.17 Extracted offset and standard variation of the offset for the slowest double tail

The proposed circuit is able to operate even for a comparator which is really slow and over temperature. The variation with respect to the temperature behaves as expected. The standard deviation of the offset corresponds to the results found in section 4.2.3, while the mean of the offset is centred on 0.

For practical reasons related in Appendix E, most of samples taped out does not give relevant results. While most of them does not have a configuration link properly connected, those whose configuration operate as expected has been partially tested.

5.3 Performance measurement of the SAR with DOE_SAR circuits

The SAR is the stage providing most of the complete ADC resolution. As the SAR is only the last stage from the ADC, none of its metric reflects the ADC performance. With a digital scheme being pseudo-synchronous, and the two first bits given by the previous stage, the test of this stage over the large temperature range from -40°C to +175°C poses an interesting challenge.

In addition to that, while the generation of an accurate and linear differential input to test a 6-bit ADC is not difficult to achieve, the timely generation of the two first bits given to the SAR is a struggling point. Yet, static metric contains meaningful information on the thermal dependence of the stage, which can be related to the ADC temperature sensitivity. Despite the gain and offset errors are a good estimator and their dependence to the temperature is a key factor, a more accurate understanding of the temperature dependence come from the analysis of the calibration coefficients' variation over temperature. Their variations allow one to detect which group of capacitors and switches generate the possible failure. That said, the non linearity will indicate error either in the settling or in the comparator decision if no failure is detected.

In order to calculate the metric, the transfer function of the ADC shall be collected at different temperature. The servo loop methodology, finding the input voltage at the transitions between two output codes, has not been selected since no transition exists for extreme input voltage values. The latter making difficult the estimation of small gain error.

To extract the total transfer function of the SAR, a ramp is generated for each quadrant defined by the two bits given as depicted by Figure 5.18.

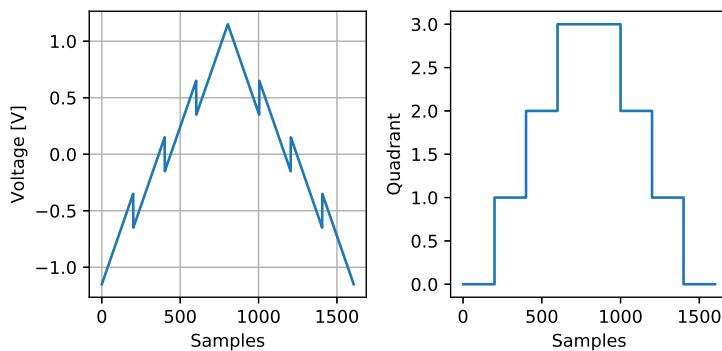


Figure 5.18 Input voltage profile and quadrant sent to the SAR under test

5.3.1 Measures

The basic setup for the test is depicted by the Figure 5.19. This includes five power supplies, a multimeter, an oscilloscope with DSO, and an optional current source. Among power supplies, two

Tests and Measurement Results

are for the power distribution. One at 1.8 V for the core, and one at 3.3 V for the level shifting needs of the digital signals connected to NI-USB boxes. The remaining three are dedicated to reference voltages.

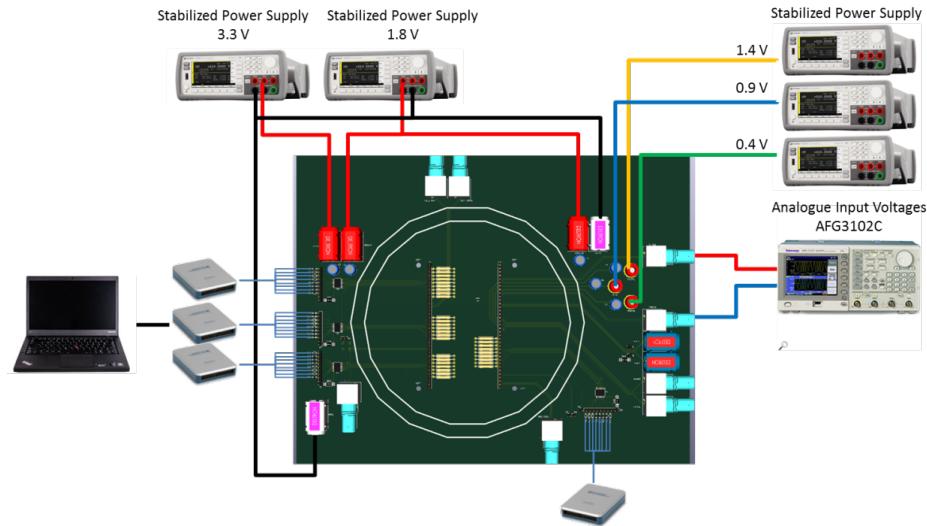


Figure 5.19 Motherboard connections of bench top devices for the test of the Sub-ADC

The differential input voltage has been generated with an Hameg HMP4040 automated through the GPIB bus. The digital signals are generated by an NI-USB 8452 and drive directly pads of the test chip. Inside it, those signals are reshaped with a Schmitt trigger inside the chip. The RESETN signal is asynchronous and resets all digital parts. Due to the different time to respond of each signal generator, the quadrant could be received by the test chip far before or after the input voltage change. To prevent erroneous conversions, overlapping range of the Figure 5.18 are 300 mV large around the quadrant transitions. This allows a change within a range of sample that will be removed to get the transfer function.

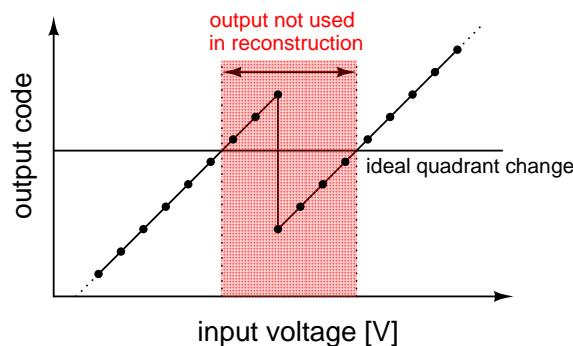


Figure 5.20 Reconstruction of the transfer function of the SAR with overlapping handling

Once the measure under the thermal stream performed, we extracted the transfer function. Due to the overlapping ranges in the test stimulus, we decided to keep the output data only in

5.3 Performance measurement of the SAR with DOE_SAR circuits

accordance with the expected ideal two first bits the algorithmic would have given. Represented in Figure 5.20, the transfer function is given by only one sweep of the triangular input signal given. Based on that, an example of measurements data collected for a SAR at 175°C is given in Figure 5.21. This figure depicts the different steps from the input voltage measures to the estimation of the DNL expressed in LSB of a 6-bit ADC.

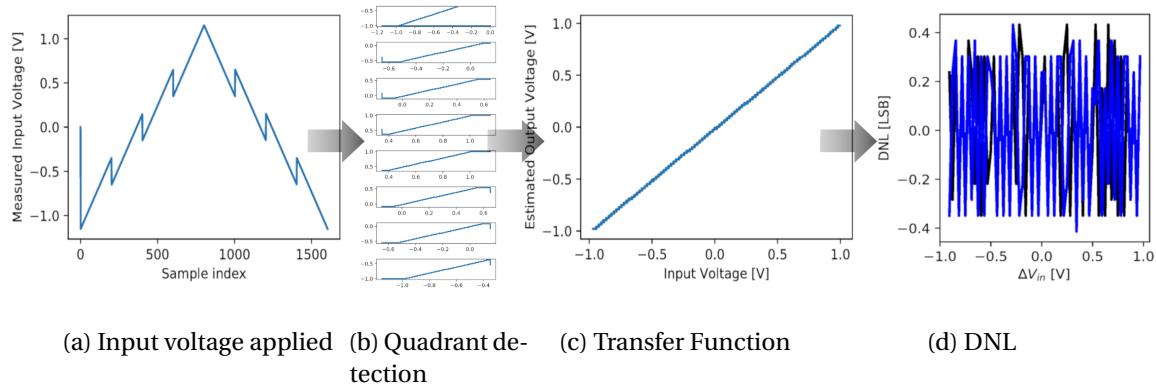


Figure 5.21 Example of data collected and processed for a DOE_SAR test chip at 175°C at 6 clock cycles per sample

Knowing the input voltage given, the results of fitting the output code to input signal gives the calibration coefficients to minimize the error committed. The error between these coefficients and the ones given by the equation (3.39) in section 3.2.3.1 is then divided by the weight given by this equation for the LSB. Repeated for each temperature, this ratio thus represents by how much the calibration coefficients shall change to get the lowest non-linearity. Represented in Figure 5.22 for a typical sample, the error on these coefficients does not exceed $\pm 35\%$. In other terms, the ideal bit weights can be kept to achieve the lowest non-linearity.

On an extreme edge case in the samples, the error could reach up to 68 % of the LSB weight at 200°C. This scenario is represented by the Figure 5.23, in which the limit for 50 % of the LSB is highlighted. The crossing occurs for a temperature of 180°C. The error occurs above the operating range of the design, we consider the last stage as calibration free.

It is important to notice, that the SAR employs the Double Tail comparator. This work demonstrates the good operation of the Double-Tail latch even at high temperature. Second, the increasing error on the LSB above 180°C have been replicated for another sample when the epoxy resin becomes fluid. Due to the different coefficient of thermal expansion between the epoxy and the silicon, the wire bonding of CoB samples underwent a strong shear stress altering the analogue voltage. Nevertheless, we can conclude that the SAR stage operates correctly over the full temperature range.

Tests and Measurement Results

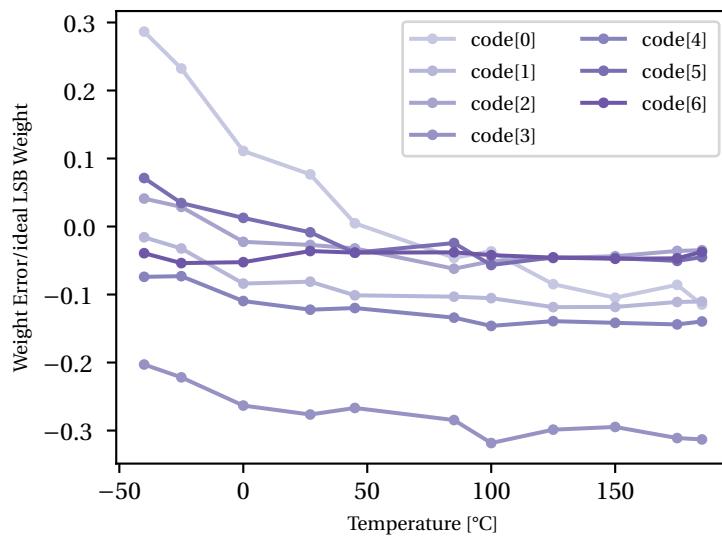


Figure 5.22 Binary weight error in the code of the SAR with respect to the ideal LSB weight versus the temperature for the DOE_SAR11

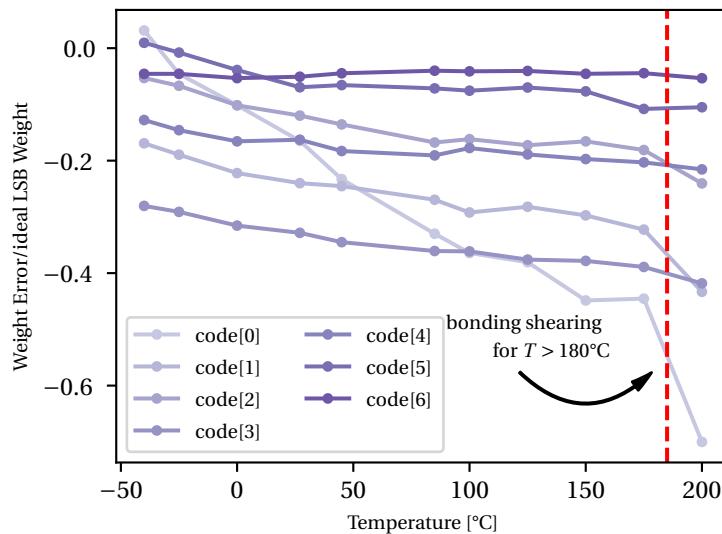


Figure 5.23 Binary weight error in the code of the SAR with respect to the ideal LSB weight versus the temperature for the DOE_SAR13

5.4 Full ADC validation

Towards a future evaluation of the ADC, this test chip is the last in the thesis and has not been tested yet. Nevertheless, this test chip has the ambition to assess each sub-ADC and the complete ADC at full speed. In this regard, the conception and preliminary simulation results are discussed. After the thesis, it is planned I finish the ADC validation.

The on-going chip design is represented in Figure 5.24. There are two ADC analog parts. One is designed for sub-ADC test whereas the second is designed to evaluate the ADC in itself. The one designed for sub-ADC characterization is also designed for evaluation of itself as a complete ADC built of these sub-ADCs. In the analog domain, there are two analog buffers for the inspection of analog signal, to wit, the residue of the each stage. Between the analog cores, the digital drives them and generates non-overlapping clock phases needed to control switches in the analog. Moreover, the digital block contains a configuration link to define what is under evaluation and how the buffers should be interconnected to the ADC. Finally, an ADC is sensitive to clock jitter and duty-cycle. To minimize this, an LVDS clock receiver has been designed for the ADC.

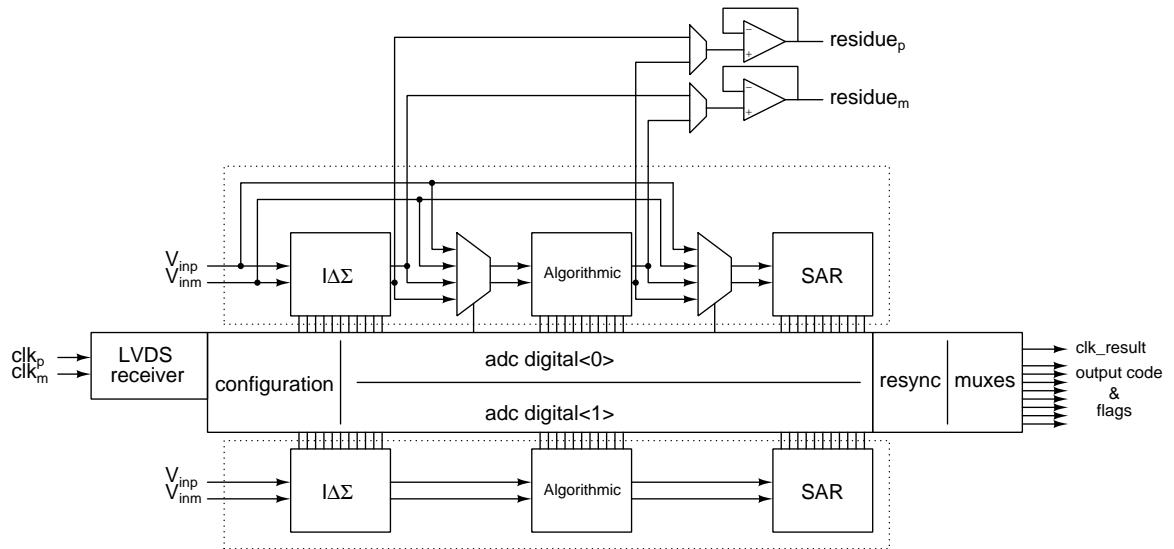


Figure 5.24 On-going test chip schematic of two ADC analog parts within along the common digital block with an LVDS clock recovery and analog buffers

The evaluation is planned to follow the validation plan discussed in Section A.1. In addition to this, the temperature and the power consumption are background measurements to get truth worthy values under experimental conditions to later consider them in the power management of future projects.

5.4.1 Power Consumption

In order to measure the power consumption of each stage, there is a single power supply pad for the analogue and one single power supply pad for the digital for each stage. In total, there are 6 power supplies pads for the ADC. Of course, to each power supply a ground is dedicated on the chip leading to the following supply voltages:

- VDDA1V8<3:1>
- GNDA1V8<3:1>
- VDD1V8<3:1>
- GND1V8<3:1>

The number inside bracket corresponds to a single voltage reference associated with the stage that this number reference: VDDA1V8<1> is connected to the ADC with stage under test selections, while VDDA1V8<2> is connected to the ADC without selections, and VDDA1V8<3> to the LVDS circuit for the clock. The order is kept for the digital power supply voltage VDD1V8 and the ground as well. Even if they are connected together on the PCB, the connection will be on a ground plane for the analogue and another one for the digital. At least, the digital and the analogue can share the same ground plane if there is a slit to reduce the switching noise of the digital on the analogue ground. Concerning the analogue buffer to replicate the residue voltage, they operate at 3.5 V provided by an analogue power supply.

In simulation, the average power consumption of the first stage is 3.7 mW, the second stage is 3.9 mW, and of the last stage is 0.8 mW. The measurement can be realized with a Keithley-2000 series appropriate in the sub micro-amps range accuracy up to 3 A. One should pay a particular attention to the digital pad connected to the digital power supply which increases the power consumption of the digital part. For the analogue part, the maximum power consumption is expected to be less than 16 mW.

5.4.2 Sub-ADC validation

While the ADC validation plan given in Appendix A.1 has the purpose of performance characterization, the Sub-ADC validation does not serve the same purpose. The Sub-ADC validation allows the detection of analogue limitation over temperature. In this regard, each stage shall be tested independently from the other.

According to the validation plan, Sub-ADCs undergo a static and a dynamic evaluation. Unfortunately, the independence does not hold for dynamic evaluation as the error committed between two consecutive stages and the stage under test followed by an external ADC will not exhibit the same transient responses. In consequence, for dynamic characterization the stage under test and the stage following it are always on.

5.4.2.1 Input Voltage Selection

The evaluation of the Sub-ADC consists in injecting the input voltage to be tested (ramp/sinusoid) at the input of the sub-ADC under test. The input selection is controlled by the configuration link which in turn drives an analog muxer. In the design of the analog muxer, we consider two factors: first the settling error of the RC filtering made of the capacitive load after the MUX and the pass resistance of the MUX, and the extra capacitive load it represents on the amplifier of the previous stage. The latter is a criterion to be able to use this analog part as a degraded ADC IP or has an ADC IP prepared for built-in test possibility. As depicted by Figure 5.26, the analog muxers are in the signal path of the input voltage and of the residue.

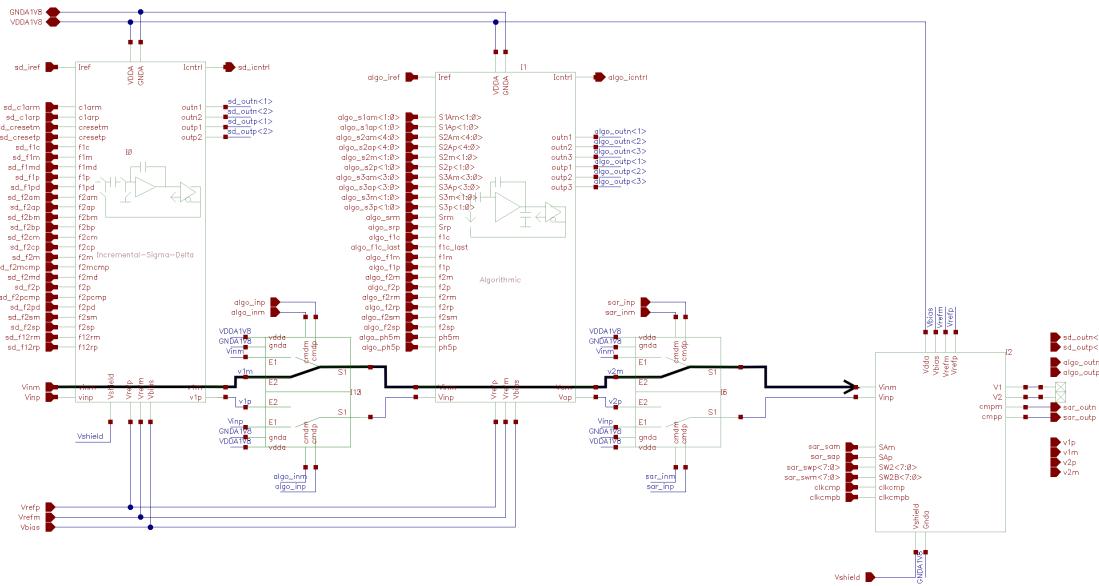


Figure 5.25 Analog core of the ADC IP with input selection for sub-ADC assessment

Even if the analog residue is planned to be between 0.65 V and 1.15 V for a differential $\pm V_{ref}/2$, we should not neglect the mismatch engendering offsets. So, the switches are CMOS to allow an extended input voltage range without adding extra errors due to a limited excursion of transistors.

Concerning the settling time, the maximum capacitive load an analog muxer is the capacitive load the SAR DAC represents. With its 950 fF in typical case and 1 pF as an edge case, we expect a settling not exceeding 40% of the clock period to allow a large duty cycle variation. To reach an accuracy of 14-bits, the time allotted for the settling is assessed to be at minimum 9.5 times the time constant of the approximated first order RC-filter. The allotted settling time being 40% of the clock period, we deduce a time constant of 421 ps. In turn, the maximum on-resistance of the analog muxer is 607Ω whatsoever the PVT condition is. To ensure this, the low-vth nmos transistors have a $W/L = 4\mu m/0.18\mu m$ and pmos transistors are 3 times bigger.

Tests and Measurement Results

In addition to that, the parasitic capacitance of the CMOS switches injects charges on the input capacitance of the sub-ADC under test as well. The minimum input capacitance is the combination of the sampling and feedback capacitors of the algorithmic stage with 200 fF. Based on simulations in the worst corner for the parasitic capacitance of the MOS transistors, the charge injection coming from nmos transistors is estimated to be few nanovolts as there are completely absorbed by the pmos parasitic capacitance. While the charge injection coming from the pmos transistors is estimated to reach 8 mV in the worst case.

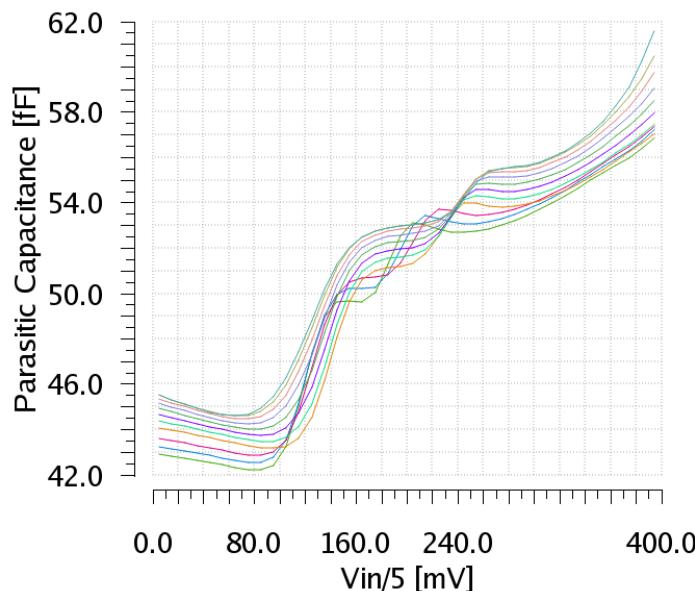


Figure 5.26 The parasitic capacitance of the input of the analog muxer the process corner exhibiting the maximum of the parasitic capacitance for several temperatures from -45°C to 175°C for an input voltage from 0 to 2 V

Henceforth, the input capacitor of sub-ADC should have a long sampling time to recover from the charge injection. That is why, as the configuration is received the analog muxer are connected accordingly and the test is at least 50 ns latter.

5.4.2.2 Static Error Estimation

The goal of this test is to determine the error committed by the ADC stage under test without considering the limitation of the settling time. The input stimulus applied will be a staircase from -0.5 V to + 0.5 V differentially around 0.9 V for a power supply of 1.8 V. A step represents the accuracy with which the code level transition is extracted. In order to measure the worst case the ADC could encounter, the precision should be of the resolution of the ADC at this stage: less than 1.9 mV.

The principle of this test consists in performing a conversion for each step by sending a pulse on the start signal lasting no more than 4 clock cycles, Figure 5.27. For a 100 MHz clock, this

corresponds to a pulse width of 40 ns. As a consequence, at the end of the conversion, the voltage of the residue is kept and the analog 3.5 V buffers connected on the residue voltages replicate them on a bigger load that represents the analogue pad, the parasitic on the PCB and the probe for the measurement. Once the measurement done, another pulse on the start signal will perform another conversion.

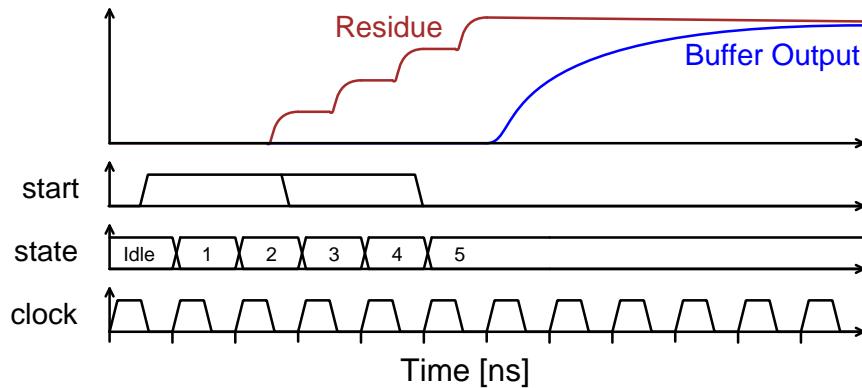


Figure 5.27 Principle of the static error estimation test with a measurement of the analogue residue

Concerning the impact of the input capacitance of the buffer, transmission gates isolate them while a transistor connects their input voltages to the ground. Then, the transistors connecting to the ground are released while the transmission gates connect the residue to the input of buffers, as depicted by the Figure 5.28. From a digital point of view, the digital circuit driving switches in the analog core of the ADC is halted when the new_sample signal is enabled and we are in the static test mode. So then, the buffers replicate the residue voltage stored by either the integration capacitor of the $\Delta\Sigma$, or one of the sampling capacitor of the Algorithmic.

To estimate the static error of the sub-ADC under test, the input voltage estimated is subtracted from the voltage reconstitution done and the added value of the residue. The linearity of the curve would indicate a reduced linearity range of the amplifier. And the maximum error in this linearity range would give the effective gain of the amplifier.

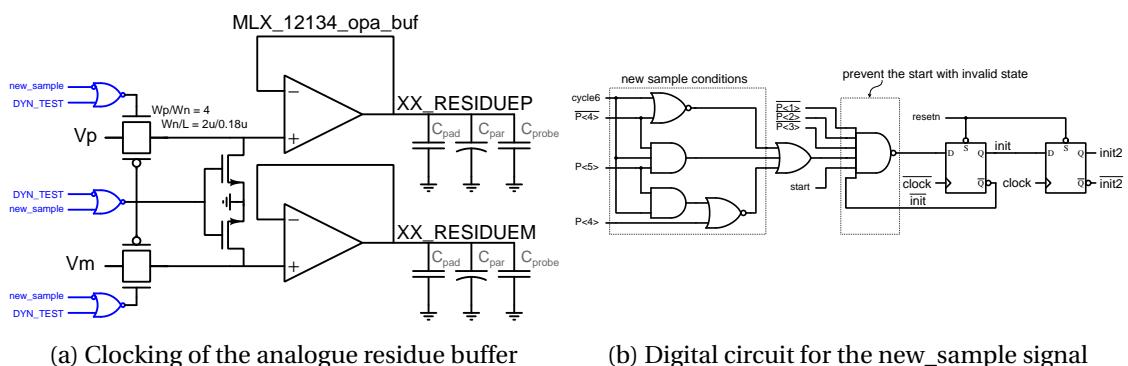


Figure 5.28 Principle of the static error estimation test with a measurement of the analogue residue

Tests and Measurement Results

Concerning the impact of the input capacitance of the buffer, transmission gates isolate them while a transistor connects their input voltages to the ground. Then, the transistors connecting to the ground are released while the transmission gates connect the residue to the input of buffers, as depicted by the Figure 5.28.

To estimate the error, the voltage reconstitution should be done by affecting a weight for each bit of 1/OSR and by adding the value of the residue. By subtracting this voltage to the input voltage applied at the input the static error is given as a function of the input voltage. The linearity of the curve would indicate a reduced linearity range of the amplifier. And the maximum error in this linearity range would give the effective gain of the amplifier.

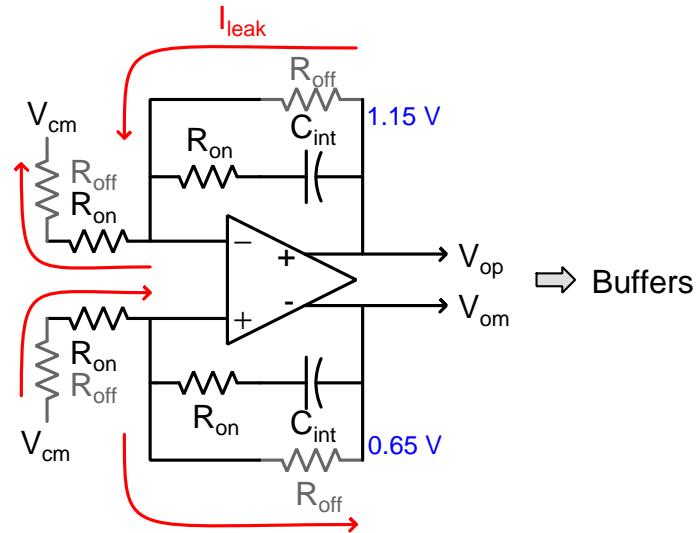


Figure 5.29 Leakage current limiting the holding time of the residue for the measure

One precaution, in this test holds in the design of switches to reset the amplifier and the integrator. As depicted in the Figure 5.29, for a differential residue voltage, a non-ideal off-resistance of the reset switches lead a leakage current discharging the integration capacitor. The load capacitor of the residue being at least 200 fF, the maximum leakage current allowed for 1 LSB drop after 20 μ s is 2.44 pA. This is equivalent to say, that the leakage impedance is 100 G Ω . Over temperature, the criterion cannot be ensured but only limited. Considering the settling time of the reset, the best comprise is $W_n=W_p=2 \mu m$ and $L_n=L_p=0.18 \mu m$ for the switches of the reset. By the way, the analogue residue measure should be done once during the conversion to estimate the offset of the buffers, and once the conversion is done the fastest possible. Either a precise ADC of 14-bits giving the results in less than 5 us or a high-precision voltmeter is necessary.

5.4.2.3 Dynamic Error Estimation

The goal of this test is to give the impact of time slots for the settling and to determine the error caused by a slow amplifier. In order to shrink the test time, The input stimulus applied will be a differential staircase ramp from -1 V to +1V around 0.9 V for a power supply of 1.8 V. A step represents the accuracy with which the code level transition is extracted. In order to measure the worst case the ADC could encounter, the precision should be of the resolution of the ADC: less than 488 μ V in 5 clock cycle mode while the steps are set to 122 μ V in 6 clock cycle mode.

To estimate the residue of the first stage, the $I\Delta\Sigma$ should operate as a standard $\Delta\Sigma$ modulator running over 4101 clock cycle (4102 if $cycle6 = 1$). The signal start shall be kept to 1 for all the duration of the residue estimation: 5 clock cycles to generate the residue, and 4096 clock cycles to reach a 12-bit resolution on the residue. So, the signal start is hold to 1 for 4101 clock cycles. From a digital point of view, the reset switch is disabled and the output bits are still output every 5 clock cycles (6 if $cycle6 = 1$). These output codes are read on the rising edge of the clock CLK_RESULT. These shall be stored either in a FIFO of the test device reading and configuring the test setup of the motherboard, and then in a file for post-processing. For each voltage in the test, 821 output codes are concatenated and bits are summed.

To estimate the residue of the second stage, the Algorithmic re-samples its last clock cycle residue such that it operates as an algorithmic with an oversampling ratio of respectively 10 or 12 clock cycles according to the sign of the $cycle6$ signal. Then, the residue at the end of the tenth/twelves clock cycle is passed to the SAR. The final resolution of the residue estimation is thus 9-bits in 5 clock cycles and 11-bits in the 6 clock cycle mode. In the digital, only one every other sample start with the loading state. And from an estimation point of view, only the second output code of the algorithmic and the related output code of the SAR are of interest.

5.4.3 Test Configuration

This test chip contains two ADCs: one with each stage independently testable and one with internally connected stages to produce a full ADC. The target of this chip is to implement the modification on the ADC only version to test each stage independently. Since performances can be altered, a second ADC without the modification is placed alongside.

The test configuration is sent on CFG_RX with the clock CFG_CLK alongside in the order depicted by Figure 5.30. Built around a shift register, the bits sent on the RX line are also output on the TX line. So, these can be checked for debug purpose. To store the configuration word, a single pulse on the CFG_VALID is sent with the last bit. To ensure the chip has been correctly set-up, we increase the duration of the validation pulse to be at least two clock cycles. In this case, the values stored in the configuration register are copied back into the shift register. To be more precise, the rewrite of the shift register occurs when CFG_VALID fall down. Therefore, the CFG_VALID pulse

Tests and Measurement Results

can be long, the data sent back are correct. Whatever is sent on CFG_TX when CFG_VALID is 1 is disregarded.

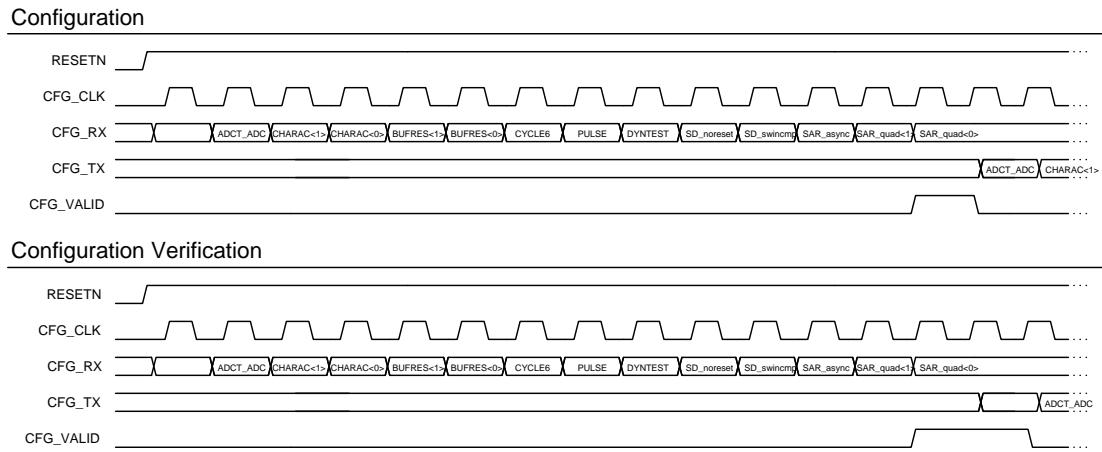


Figure 5.30 Configuration bits order for the selection of the test and configuration of possible existing mode of the ADC

Among the 13-bits configuration register, the first bit ADCT_ADC selects which ADC analog core is under test. Set High, the ADC with sub-ADC input selection is under test while set Low, the ADC without input selection is under test.

Bits called CHARAC<1:0> select which part is under test if ADCT_ADC is Low:

- 00: Sigma-Delta Incremental
- 01: Algorithmic
- 10: SAR
- 11: Full ADC

The bits BUFRES<1:0> select which residue is connected to the buffers for measurements:

- 00: None
- 01: Algorithmic
- 10: $I\Delta\Sigma$
- 11: Shall never be used

Finally, a synchronizer block is in charge of triggering the start of a new sample for the all three stages based on the following bits:

- START: when conversion is expected to be performed/when a conversion should start
- CYCLE6: the ADC performs a conversion in 6 clock cycle or in 5
- DYNTEST: the rising edge of the signal start starts a new conversion. While start is 1 each stage is still processing.

5.5 Preliminary ADC Schematic Simulation Results

In this section we present preliminary simulation results of the analog core of the ADC. The simulations performed are full transistor for the analog core and for the interface between the digital and the analog. Comparators and OTAs are those designed in the chapter 4 at the schematic level.

The DOE_ADC chip is composed of the schematic presented earlier in Figure 5.24 with addition pads from the PDK of the technology. In order to estimate the future behaviour of the ADC, we model the wire bonding by an RL-serie circuit with $R=0.1 \Omega$, and $L=1 \text{ nH}$. This corresponds to a wire whose diameter is $55 \mu\text{m}$ and 1 cm long. As depicted by Figure 5.31, all signals and power supplies are connected by the wire bondings model to the chip. A verilog bloc sends the test configuration to DOE_ADC. For instance, to test only the ADC in 6 clock cycle mode the pattern sent is 1000010010100. While for the ADC with an OSR = 5, we send 1000000010100. In addition to that, a verilog-ams bloc stores in a file the output codes and the voltages $V_{\text{inp}}/V_{\text{inm}}$. These permit the evaluation of the ADC (DNL, INL, SNR, ENOB, ...).

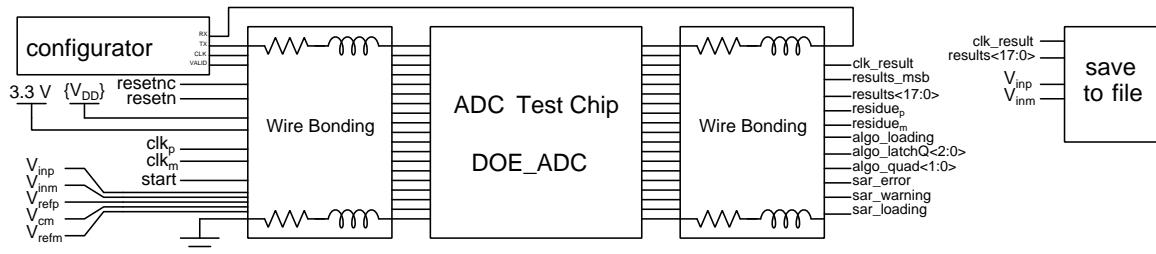


Figure 5.31 Stimuli generation to check the static performance of the ADC

For the analogue voltages, we allow the use of ideal power supplies as display in Figure 5.32. In order to re-use the simulation test bench, the parameters are the following:

- OSR: the oversampling ratio between the sampling frequency, and the ADC clock
- $T_{\text{start-up}}$: the time given for the slow-start of the circuit, to let settle the common-mode
- LSB: the voltage resolution expected of the ADC
- F_s : the sampling frequency
- V_{DD} : the ADC power supply voltage for the test

By default, the input voltage is a linear ramp, changing at a rate of $1/F_s$ by a fifth of the LSB. The differential input voltage ramps up from -1 V to + 1 V.

Concerning the clock generation, the LVDS signal is made from an ideal pulsed source with a transition time of 3 ns between a low-level of 0.7 V to a high-level of 1.1 V. With a differential amplitude of 400 mV around a common-mode of 0.9 V, the LVDS clock signal is a best-case.

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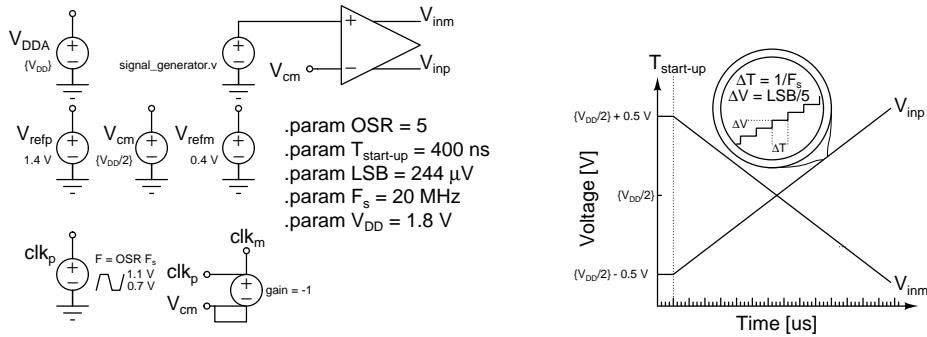


Figure 5.32 Input voltages generation to check static performance of the ADC

To extract the information on the resolution, we reconstruct the input signal from the output bit of the ADC by their ideal weight. In this case the weight is the voltage contribution of each bit. For the first stage, each bit has an ideal weight of $1/\text{OSR}$. For the second stage, the ideal weight is $[0.5 \ 0.25 \ 0.125 \ 0.0625]/\text{OSR}$. And the contribution of the SAR is given by the equation (3.39) scaled by a factor $0.0625/\text{OSR}$. The offset has been estimated by averaging the output code and is removed in the transfer function.

Figure 5.33 presents the resolution based on the maximum error between the resolution input voltage and its reconstruction from the output codes. After an offset estimation based on the average output code, the maximum resolution is represented for an oversampling ratio of 5 and 6 in the typical process corner.

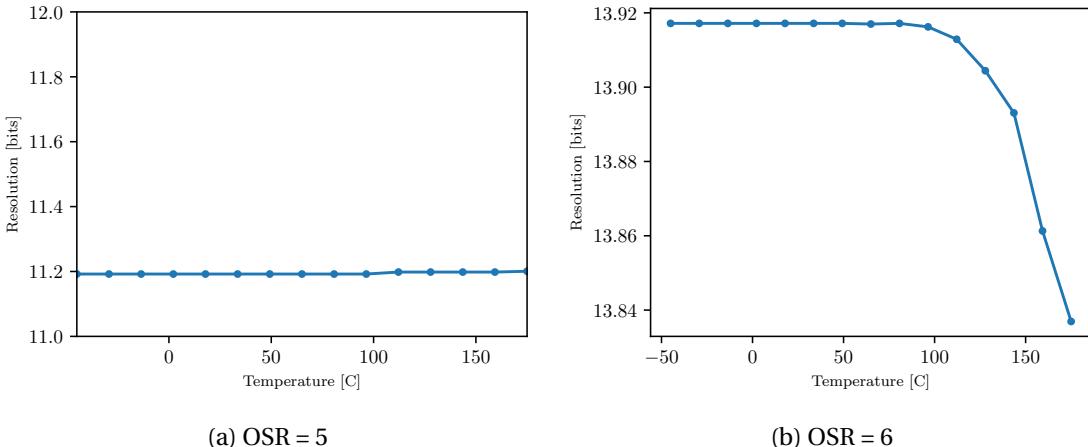


Figure 5.33 Resolution for the typical corner over the temperature at the two oversampling ratios the ADC has been designed for

The ADC exhibits an encouraging stable behavior over temperature. The error committed on the residue of the first stage has the deepest impact on the final resolution. Heavily relying on the performance of the OTA, and a gain higher than the 11.2-bits of resolution, the ADC in 5 clock cycle mode does not suffer from the temperature. To the contrary, in the 6 clock cycle mode, the

5.5 Preliminary ADC Schematic Simulation Results

OTA gain in a typical corner drop from 86 dB to 78 dB. In consequence, the best case error of the OTA on the residue drop from a 14-bits resolution to a 13.3-bits one. Therefore, the resolution also drops from 100°C. The error committed on the first stage residue being less than an LSB of the sub-ADCs remaining, the ADC does experience a more severe degradation of its resolution.

With the process variation, the OTA undergoes a severe degradation of its gain and its settling speed. This OTA degradation has repercussions on the resolution of the ADC. The results of the resolution due to the process variation is depicted by Figure 5.34 for the ADC operating at 6 clock cycles per sample.

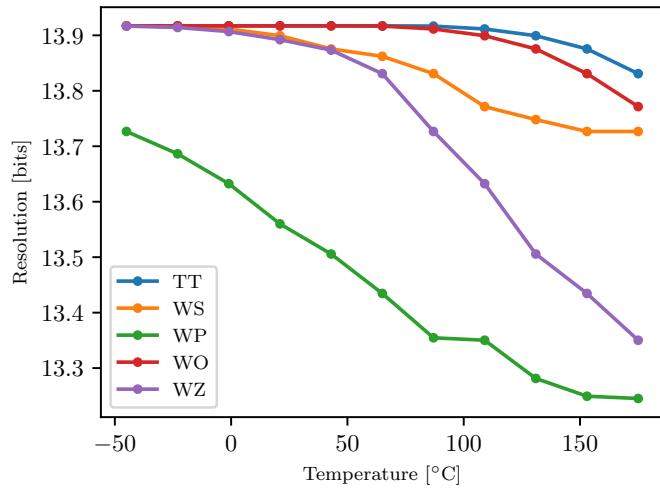


Figure 5.34 Resolution over the temperature for each corner of the process with the ADC operating at 6 clock cycles per sample

The results over the corners of the process display a drop of 0.67-bits. This drop is a third of experimentation in the work of Ericson over the same temperature range with a 0.5 μ m SOS-CMOS technology [108]. It is planned to validate the behaviour in simulation with coming experimental data.

At this stage of the realization, the analogue part of the ADC consumes 9 mW in the worst case. With a Nyquist frequency of 8.33 MHz for a resolution of 13-bits in 6 clock cycle mode, the corresponding Walden Figure of Merit is 131 fJ/conv for an area of 0.12 mm². Similarly, in 5 clock cycle mode, the Walden FoM is given to be 382 fJ/conv for a target of 390 fJ/conv. The design is in the middle of publications in ISSCC and VLSI as depicted by Figure 5.35.

In order to represent the effort of integration, Figure 5.36 represents the FoM versus the area of one channel for ADC realized in 180 nm technology. The proposed converter exhibits a low area footprint, placing it at the front edge of the technology. Considering the FoM, the results can be improved by either reducing the power consumption, or by increasing the resolution.

Tests and Measurement Results

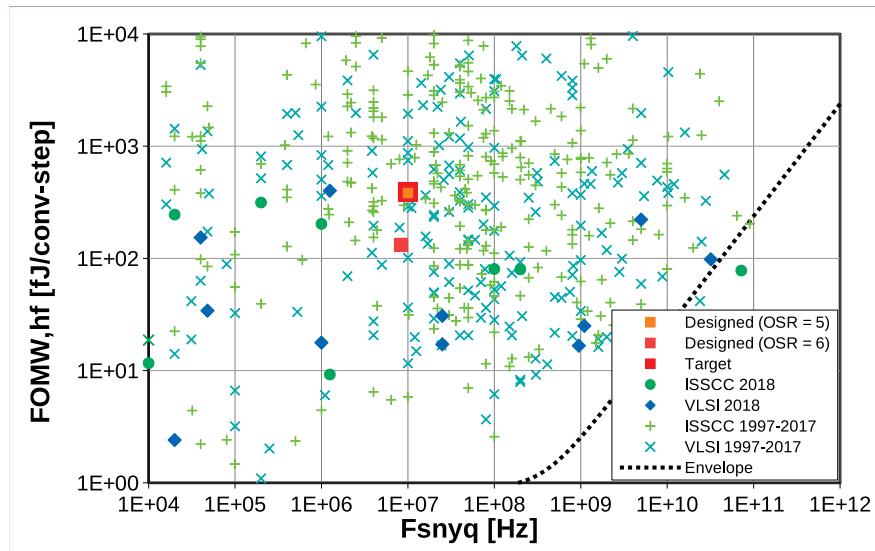


Figure 5.35 Walden FoM versus the nyquist frequency of ADC published in ISSCC and VLSI from 1997 to 2018 in comparison with the proposed one

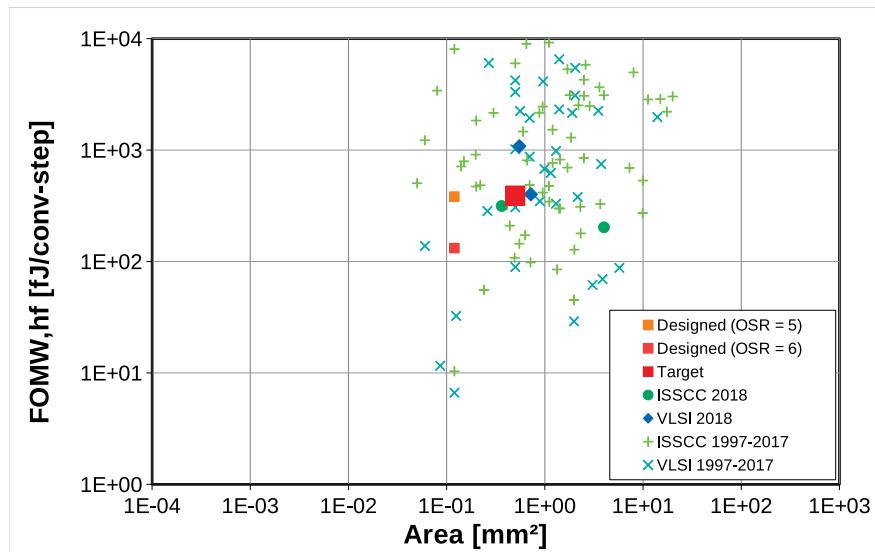


Figure 5.36 Walden FoM versus the area of a single channel ADC published in ISSCC and VLSI from 1997 to 2018 in comparison with the proposed one

5.5 Preliminary ADC Schematic Simulation Results

In this work, a low-OSR 3-stage hybrid ADC is employed to improve the sampling rate, and the resolution without sacrificing the silicon area. This work also proposed a temperature aware design of the building blocks to reduce the performance drop with increasing temperature. After design, the performance achieved are listed in Table 5.5.

Table 5.5 Specification of target ADC

	Criterion	OSR=5	OSR=6
Operating Temperature	-40 °C – +175 °C		
Supply Voltage	1.8 V ± 10 %	1.8 V +10 % - 5 %	
Differential Input Voltage Range	± 1V		
Area	<0.5 mm ²	0.114 mm ²	
Conversion Speed [MSamples/s]	20	16.66	
Maximum Clock Frequency	100 MHz		
Clock Duty-Cycle	40 – 60 %	To Be Defined	
Latency	<500 ns	150 ns	180 ns
Resolution	≥ 12-bits	11-bits	13-bits
SNDR	min 74 dB for $F_s < 5$ MHz min 68 dB for 5 MHz < $F_s < 10$ MHz, min 62 dB for $F_s > 10$ MHz min 68 dB	To Be Defined To Be Defined To Be Defined To Be Defined	
SFDR (Full-Scale)	<LSB/2		
DNL	<LSB/2 best-fit method		
INL	<4 LSB		
Offset Error	<4 LSB		
Gain Error	<4 LSB		
Adjacent ADC mismatch Error	<4 LSB		
Energy, $E_s = P/F_s$ [nJ/sample]	0.75	0.45	0.54

Although this work demonstrates encouraging results, lot of topics has not been addressed yet. For instance, the reference voltage generation, the sample-and-hold, the tolerance to duty-cycle variation, the calibration, etc. These are only few among many.

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The automotive environment is a challenge for the design of resilient and robust electronics. Exposed to high temperatures, abrupt accelerations and large process and voltage variations, many innovations were explored to provide smart sensing for a market driven by the autonomous car. At the interface of the severe environment and the processing power, the trend is to shift the ADC upfront so that more processing can be done in the digital domain to leverage complex algorithms and to conserve energy. The stability is thus the key factor to these interfaces in any circumstance. However, the general lack of progress in applying this technique to high-temperature applications is evident in the state-of-the-art.

To achieve medium speed and high resolution ADCs, $\Delta\Sigma$ modulation and SAR have many times demonstrated their ability to face a harsh environment under the high temperature constraint. While in standard temperature range pipelined ADCs lead the high resolution and high-speed rank, their sensitivity to analog defects put them in default at high temperature: calibration being the only way to minimize the PVT variation effects.

This research reports works from the architecture to the analog design to reduce the sensitivity of the conversion performances. Following a top-down approach, a new hybrid three stages pipelined architecture has been proposed. The pipelined architecture provides an efficient way to achieve high speed conversions with a low oversampling ratio. And low-resolution first order Incremental- $\Delta\Sigma$ modulator and SAR ensure the robustness of the solution by decreasing the in-band noise, at a low-power consumption and small area footprint.

After an analysis of the design space sensitivity of the silicon electronic, major guidelines have been dispatched along the conceptual design of each stage of the new topology proposal. From the capacitor ratio of Incremental- $\Delta\Sigma$ integrator limiting the linearity to the digital interface of the algorithmic stage have been investigated. Even in the case of the differential architecture implemented, charge injections, clock feed-through have been considered as well as the analog requirement of amplifiers early in the design phase to limit the requirement of multi temperature calibration due to temperature dependent phenomena. The SAR building bloc was optimized to cope with imperfections from the Algorithmic, face large comparator offset and relax timing constraints by the employ of a pseudo-synchronous digital scheme.

Using only 6 comparators and 2 OTAs, those are key IP components of the designed proposal. From a selection of the most appropriate architecture based on the most used one in the literature,

Conclusion and Future Work

analytical models have been drawn out to design and select the most appropriate one for the application: Strong-Arm latches for the two first stages, Double-Tail latch for the SAR, and a Gain-Boosted Complementary Folded Cascode Class AB OTA. The latter has been optimized for High-Speed High-Gain and reduce noise power.

Comparators have been tested over temperature to validate models. In this regard a new delay measurement circuit has been developed to minimize the area, the power consumption and the time to design a delay assessment circuit.

The SAR were fabricated with a Double-Tail latch and tested from -40°C to 200°C at the limit of the test setup. The result is first, to our best knowledge, to present a double-tail latch operating at high temperature.

Finally, the design of the ADC test chip to fully characterize the ADC and the OTA performance is detailed. The preliminary results of this work demonstrate the potential high-resolution data-converter in SOI CMOS XT018 technology. The resolution reported represents a significant improvement on the sensitivity over reported high-temperature ADC having a severe drop of 2-bits.

During the thesis, my published contributions are following:

- L. Cron, P. Laugier, P. M. Ferreira, F. Vinci dos Santos and P. Benabes, "Évaluation des convertisseurs analogique-numériques pour le secteur automobile", JNRDM, Toulouse, May 2016
- L. Cron, P. Laugier, P. M. Ferreira, F. Vinci dos Santos and P. Benabes, "Delay estimation and measurement circuit for a high-speed CMOS clocked comparator," 2017 European Conference on Circuit Theory and Design (ECCTD), Catania, Set 2017, pp. 1-4. doi: 10.1109/ECCTD.2017.8093261
- Adriano V. Fonseca, Ludwig Cron, Fernando A. P. Barúqui, Carlos F. T. Soares, Philippe Benabes, Pietro Maris Ferreira, "A Temperature-Aware Analysis of SAR ADCs for Smart Vehicle Applications", Journal of Integrated Circuits and Systems, vol. pp, no. pp, pp. 1–11, 2018.

6.2 Future Work

The ADC test chip not being fabricated yet, a first step is the characterization of the ADC. Being part of my first job, a measurement session of the ADC test chip is planned.

From the results collected in this future session, the main goal is to push the architecture at higher sampling rates to then leverage the digital processing to enhance the sampling rate without changing the analog.

The development of the ADC IP is not complete and the architecture not being sample-and-hold free, its design is the next challenge to address. Although we are not yet at this stage, it is possible to extend the SAR to always be at the limit of the technology by using a fully asynchronous design with DFT capability.

In switched-capacitor applications, comparator-based (comparator output driving current source to charge/discharge a capacitive load) and ring amplifiers (cascade of an odd number of inverters with a dead zone) are two low-power (1-2 mW) and high-speed (Fclk from 100 MHz to 500 MHz) amplification techniques for pipelined/algorithmic and Delta-Sigma modulators. Recently a lot of improvement to cope with the process and temperature variations have been published in 2017 and 2018 (ISSCC and ISCAS). Measurement results demonstrate their efficiency for technology from 180 nm to 65 nm. Therefore, these are the possible steps to move the presented architecture closer from a digital design while shrinking the power consumption and the area.

Another investigation could be the re-use of the auto-oscillating delay measurement circuit. With the comparator as a voltage comparator, the circuit convert a differential voltage into a frequency. Tested at high temperature, the circuit could be a fully digital asynchronous design for a possible asynchronous fully differential ADC.

From another point of view, the top-down approach can be pushed further with the insight on temperature sensitivity. This can be embedded in “A SPICE Circuit Optimizer” (ASCO) to reduce the time to design for 6σ process variations considering voltage and temperature variations to reduce the sensitivity.

ADC CHARACTERIZATION

A.1 Validation of ADC and Sub-ADC

This section has the important role of listing methods for High-Speed ADC evaluation and sub-ADC evaluation. For an ADC, both static and dynamic performances shall be known for the practical use case. In our case, we limit the scope of metric to those listed in the Table A.1.

Classical methods are now mainstream in the industry and can be found in application notes of some manufacturer [186–188]. Several methodologies existing, they are gathered on the criterion of whether they are for static metrics or dynamic ones. For each, the mean to extract the metric listed in the Table A.1 is discussed.

Since the ADC IP bloc is differential others metrics are of interest such as:

- Common mode and differential input impedance
- maximum common-mode signal
- maximum operating common-mode signal
- common-mode rejection ratio
- common-mode out-of-range

These are not discussed in this section.

Table A.1 Metric of interest for the ADC tests

Static Metric	Dynamic Metric
– Gain Error	– Single-Tone Signal to Noise Ratio (SNR)
– Offset Error	– Signal to Noise and Distortion (SINAD)
– Temperature Drift of Gain and Offset Error	– Effective Number of Bits (ENOB)
– Differential Non Linearity (DNL)	– Total Harmonic Distortion (THD)
– Integral Non Linearity (INL)	

A.1.1 IEEE recommendations

A.1.1.1 Static Metric

Among static metrics extraction methods, the histogram based is widely adapted. A histogram is collected by driving the analogue inputs of the ADC with a known signal. Each bin value of the

ADC Characterization

histogram corresponds to how many times the associated code of this bin is counted. The offset of the ADC can be estimated as the average code of all if the input signals applied have a zero mean. The offset error is thus, the difference between the average output code and the ideal output code. The gain error defined as the ratio of the actual transfer function slope over the ideal one can be seen in the histogram as a discrepancy between the first and the last bins weight and their ideal weight. For instance, a slope coefficient lower than the ideal one (negative gain error) will display an histogram close to the ideal one shrink into fewer bins and extreme bin values higher than expected as depicted by the Figure A.1.

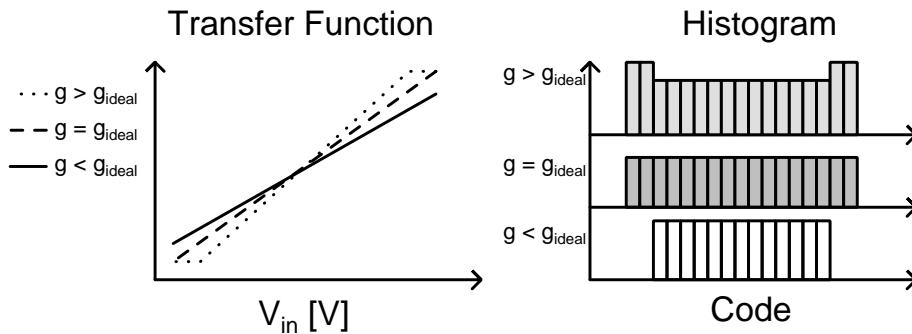


Figure A.1 Gain error detection in an histogram based analysis

The input signal can be a ramp, a sine wave, or small signal variation around an even increasing offset, the DNL and INL can be extracted by subtracting the actual ADC histogram to the ideal ADC histogram. In a practical implementation, the input stimulus might not be perfectly linear and might degrade the DNL estimation. As a common practice, the stimulus linearity is 2 to 3 bits higher than the ADC under test. The INL is usually defined as the cumulative sum of the DNL. To limit the number of records, a ramp is usually preferred. A sine wave can be applied to reduce the test time but the number of records should be selected as described at the page 41 of [189].

A major flaw of this testing method concerns potential missing codes. Since the histogram is a counter of code occurrence, the occurrence of a missing code is attributed to the closest adjacent code. So an incorrect amount of occurrences is detectable but this implies that we are not able to detect a missing code. To avoid these issues, the ADC should also be tested for SINAD performance to confirm that non-monotonic behaviour is not significant.

By applying a signal on the ADC inputs, the output codes should ideally represent the input signal applied. Therefore, a fitting of output codes with the ideally expected results is sufficient to extract the gain and the offset of the ADC under test. The input signal can be either a ramp or a sine wave, and a least mean square algorithm is able to extract errors on the gain and the offset. Unfortunately, this method is input dependant, and does not extract other metrics. A classical post-processing of output codes is necessary to extract dynamic characteristic and non-linearity

(histogram, FFT). Its advantage over the method in the previous clause is that it is less sensitive to noise and more thoroughly eliminates spectral leakage.

However, the transfer function of an ADC can also be estimated by knowing at which input voltages occur a transition. The servo-loop method is a closed loop approached consisting in finding the code transition level of a given reference code. This method is well suited to find transition in the transfer function. An ADC output code different from the one selected will adjust the ADC input voltage until the reference code is met. Once the code transition level has been reached, the input signal is forced to oscillate across this transition. This time the input voltage should be measured with an extra difficulty coming from the final oscillations. Either filtering or averaging is necessary with a bias correction to determine the ideal voltage value. Repeating this process for each code of the ADC, the INL can be estimated from all the ideal voltage value. The input stimulus can be generated by either a DAC at the input. In which all the estimation is digital. Or the input voltage is done by an analogue integrator. This method is limited by the confidence in the linearity and the performances of the DAC used.

A.1.1.2 Dynamic Metric

The dynamic metrics are usually extracted from the FFT of the sine wave reconstructed [189]. Nevertheless, some precautions on the signal have to be respected: the number of records and the frequency of the single-tone sine wave are only two among many. For high speed ADC, the IEEE standard 1241-2010 recommends the use of a memory buffer to acquire data at the ADC sample rate. While the coherent sampling is reached when there is an integer number of waveform cycles in the data record. The following relationship describes it:

$$MF_i = JF_s \quad (\text{A.1})$$

Where F_s is the sampling frequency, J is the integer number of cycles of the waveform in the data record, F_i is the frequency of the input waveform, and M is the number of samples in the data record. The recommendation is to set J to be at least 5 and to be co-prime with M . ($J = 5$, $M = 7 \times 2^{12}$ are co-prime)

Concerning the distortion of the input sine wave, the THD should be far less than the one of the expected ADC. Otherwise, this non-linearity will be found as well in the INL plot as in the dynamic parameters. The purity of the sine wave should be ensured and readily tested with a spectrum analyser. The clear advantage of the sine wave stimulus is the relax constraint on the signal and clock synchronicity. The trigger of conversion does not have to be synchronized. Finally, a great care is considered about the input signal overdrive which should at least be 3 times the rms value of the random noise at the input. If noise is present, it will modify the probabilities of samples falling in various code bins, and the effect will be larger near the peaks where the curvature of the

ADC Characterization

probability density is greatest. Once the setup configured, the metrics are extracted from the FFT of the reconstructed signal. To prevent spectral leakage, a rectangular window is sufficient if the coherent sampling criterion is respected (a single ray at the input frequency shall be present in the spectrum). Otherwise, whatsoever the window is applied the record length should large enough to reduce the spectral leakage.

A.2 ADC Figure of Merit

To compare the specification presented to the specification of other ADC in the literature, it is commonly accepted to represent the results of a calculation based on reached performances, as a value representing the effort put into the design. The calculation of such Figure of Merit (FoM) can vary. A widely adopted Figures of Merit, also called Walden's Figures of Merit incorporates the resolution, the speed and the power consumption in order to provide a simple value to compare with:

$$FoM_{\text{walden}} = \frac{\text{Power}}{2F_{\text{signal}}2^{\text{ENOB}}} \quad (\text{A.2})$$

where the ENOB is defined by

$$\text{ENOB} \approx \frac{\text{SNR} - 1.76}{6.02} \quad (\text{A.3})$$

P is the total power consumption, ENOB is the effective number of bits, and F_{signal} is the input frequency of the signal. SNDR is the signal-to-noise-distortion ratio in dB measured with a sinusoidal input.

This FoM is intended to provide a measure of how much energy is required to perform a conversion step, expressed in picojoules (pJ) per conversion step. This metric is created under the assumption that power tends to scale linearly with the input frequency and SNDR. However, In a high resolution ADC that is 10 bits or more, the resolution is mostly limited by thermal noise. Let us suppose the ADC is a capacitive load C, the noise is in the form of $\sqrt{kT/C}$. In order to increase the resolution by 1 bit, C has to quadruple. If the operating frequency is kept constant, the power consumption has to be increased by a factor of four for an improvement of a factor of two in resolution. This implies that improving the resolution by 1 bit automatically worsens the FoM by a factor of two.

Figure A.2 represents the Walden FoM from the Murmann ADC survey taking into account conferences until 2018. In addition the FoM of the proposed ADC is represented in the middle of these by a large bullet. With 15 mW at 20 Mhz it should be equal to 750 pJ with an SNDR = 68 dB. Even if the ADC is placed in the middle of the graph, the highest temperature of the operating range make the thermal noise the most limiting factor in our design challenging.

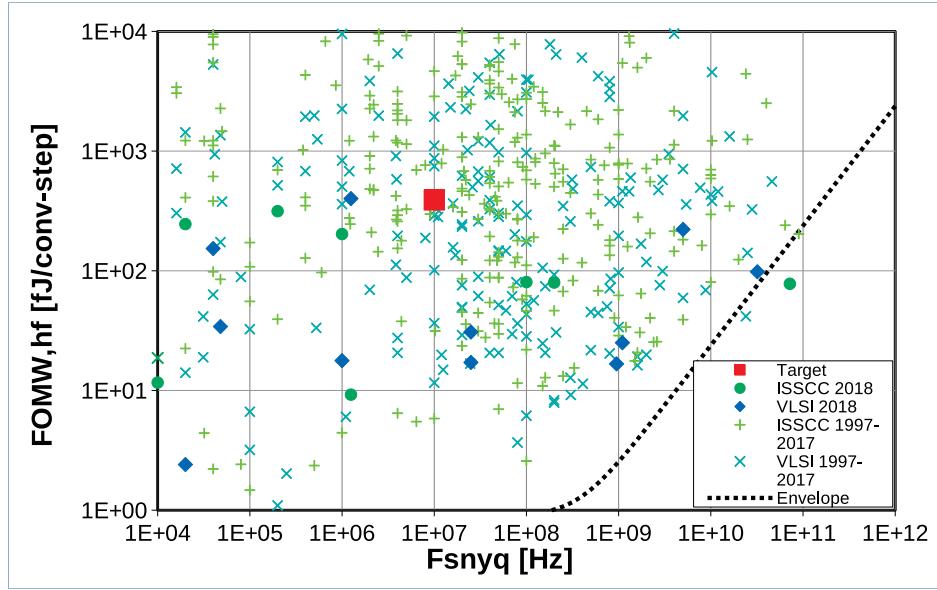


Figure A.2 Walden FoM versus the nyquist frequency of ADC published in ISSCC and VLSI from 1997 to 2018 in comparison with the proposed one

This figure of merit can also be represented in function of the surface per channel to represent the design effort to minimize the cost. Represented in Figure A.3, the ADC are concentrated along a line going from a low FoM with a small area (bottom left corner), to the high FoM with a large area (top right corner). The technology scaling down more and more ADC appear in the bottom left corner. The specification of the target ADC is right in the middle. Our primary goal is first to reduce the area, and then this FoM.

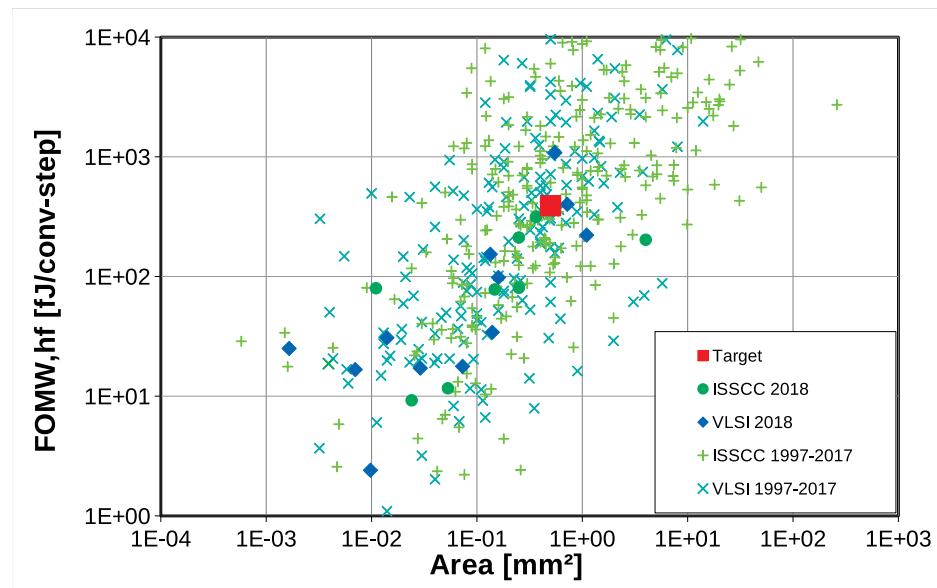


Figure A.3 Walden FoM versus the area of ADC published in ISSCC and VLSI from 1997 to 2018 in comparison with the proposed one

LATCHES SMALL SIGNAL MODELS

B.1 Strong Arm

In order to derive offset and delay equations, the small signal model of the strong arm latch is represented in Figure B.1. The drain-source effect of transistors is neglected for the sake of simplicity. These are considered then in the post-layout simulation results presented in Section 4.2.3

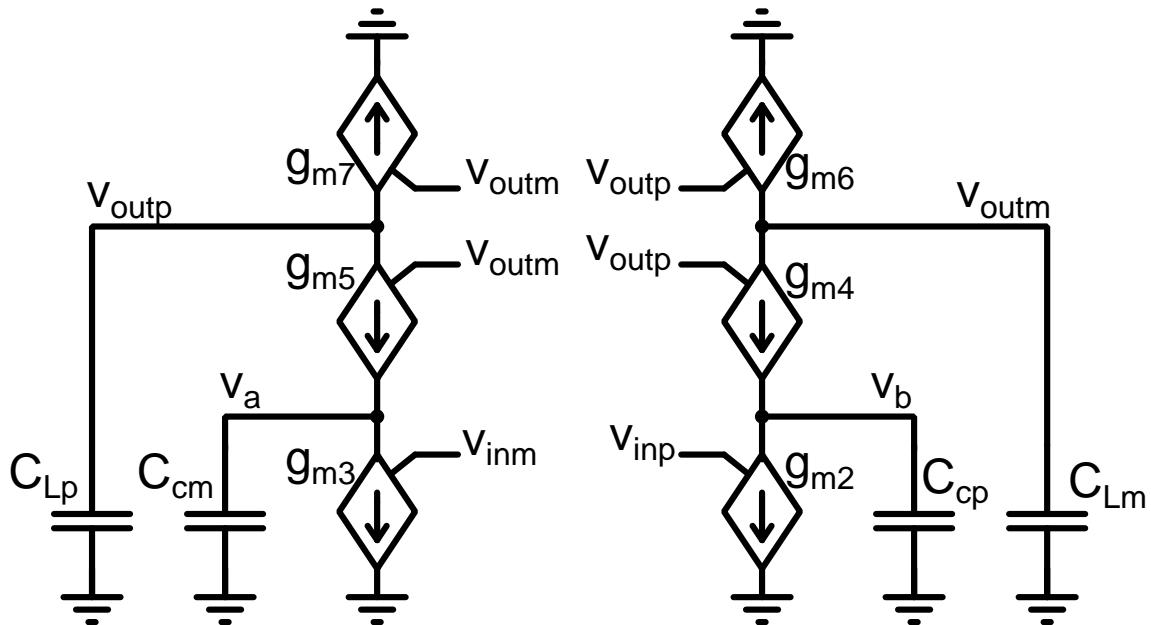


Figure B.1 Strong Arm Small Signal Model

The application of KCL at nodes v_a and v_b gives respectively

$$(sC_{cm} + g_{m5}) v_a = g_{m5} v_{outm} - g_{m3} v_{inm} \quad (B.1)$$

$$(sC_{cp} + g_{m4}) v_b = g_{m4} v_{outp} - g_{m2} v_{inp} \quad (B.2)$$

while KCL on output nodes lead to

$$sC_{Lp} v_{outp} = -(g_{m5} + g_{m7}) v_{outm} + g_{m5} v_a \quad (B.3)$$

$$sC_{Lm} v_{outm} = -(g_{m4} + g_{m6}) v_{outp} + g_{m4} v_b \quad (B.4)$$

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Replacing v_a and v_b in these equation by their expression in B.2 gives us

$$sC_{Lp}v_{outp} = -(g_{m5} + g_{m7})v_{outm} + \frac{g_{m5}}{1 + s\frac{C_{cm}}{g_{m5}}}v_{outm} - \frac{g_{m3}}{1 + s\frac{C_{cm}}{g_{m5}}}v_{inm} \quad (\text{B.5})$$

$$sC_{Lm}v_{outm} = -(g_{m4} + g_{m6})v_{outp} + \frac{g_{m4}}{1 + s\frac{C_{cp}}{g_{m4}}}v_{outp} - \frac{g_{m2}}{1 + s\frac{C_{cp}}{g_{m4}}}v_{inp} \quad (\text{B.6})$$

Then, voltages are defined in term of their common mode voltage and differential voltages such that $v_{inp} = v_{inc} + v_{ind}/2$ and $v_{inm} = v_{inc} - v_{ind}/2$ (resp. for v_{outp} and v_{outm}).

$$\begin{aligned} s(C_{Lp} - C_{Lm})v_{outc} + s(C_{Lp} + C_{Lm})\frac{v_{outd}}{2} &= (g_{m4} + g_{m6} - g_{m5} - g_{m7})v_{outc} \\ &\quad + (g_{m4} + g_{m6} + g_{m5} + g_{m7})v_{outd} \\ &\quad + v_{outc} \left(\frac{g_{m5}}{1 + s\frac{C_{cm}}{g_{m5}}} - \frac{g_{m4}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) \\ &\quad - \frac{v_{outd}}{2} \left(\frac{g_{m5}}{1 + s\frac{C_{cm}}{g_{m5}}} + \frac{g_{m4}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) \\ &\quad + v_{inc} \left(\frac{g_{m3}}{1 + s\frac{C_{cm}}{g_{m5}}} - \frac{g_{m2}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) \\ &\quad - \frac{v_{ind}}{2} \left(\frac{g_{m3}}{1 + s\frac{C_{cm}}{g_{m5}}} + \frac{g_{m2}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) \end{aligned} \quad (\text{B.7})$$

The input referred offset could be defined as the differential input voltage when the differential output voltage is null, the offset is thus defined as

$$\begin{aligned} \frac{v_{offset}}{2} \left(\frac{g_{m3}}{1 + s\frac{C_{cm}}{g_{m5}}} + \frac{g_{m2}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) &= (g_{m4} + g_{m6} - g_{m5} - g_{m7} - s(C_{Lp} - C_{Lm}))v_{outc} \\ &\quad + v_{outc} \left(\frac{g_{m5}}{1 + s\frac{C_{cm}}{g_{m5}}} - \frac{g_{m4}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) \\ &\quad + v_{inc} \left(\frac{g_{m3}}{1 + s\frac{C_{cm}}{g_{m5}}} - \frac{g_{m2}}{1 + s\frac{C_{cp}}{g_{m4}}} \right) \end{aligned} \quad (\text{B.8})$$

B.2 Strong Arm Montanaro Version

The transistor introduced by Montanaro in [128] keep a the voltage defined at drain of differential pair transistors even if the differential input is extremely large. Unfortunately, this extra “resistor” implemented by a mosfet alter the decision in both the offset and the delay required to make a decision.

The small signal model is represented in

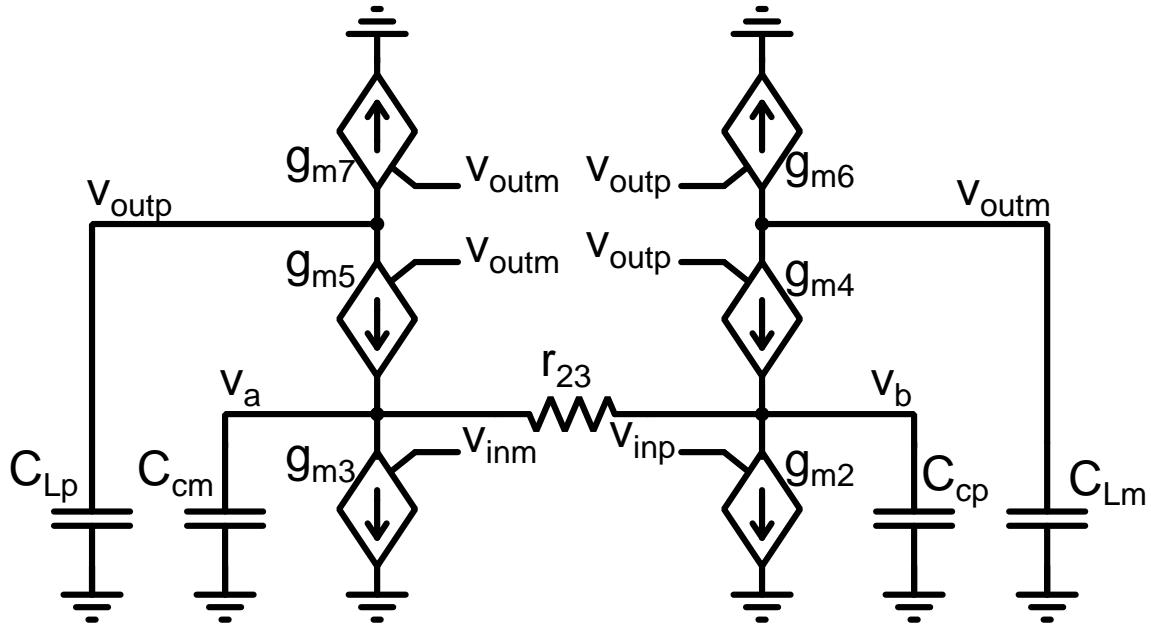


Figure B.2 Strong Arm Small Signal Model

Compared to conventional structure, KCL on output nodes lead to the same equations which are

$$sC_{Lp}v_{outp} = -(g_{m5} + g_{m7})v_{outm} + g_{m5}v_a \quad (B.9)$$

$$sC_{Lm}v_{outm} = -(g_{m4} + g_{m6})v_{outp} + g_{m4}v_b \quad (B.10)$$

while KCL applied on nodes v_a and v_b gives respectively

$$(sC_{cm} + g_{m5})v_a = \frac{v_b - v_a}{r_{23}} + g_{m5}v_{outm} - g_{m3}v_{inm} \quad (B.11)$$

$$(sC_{cp} + g_{m4})v_b = \frac{v_a - v_b}{r_{23}} + g_{m4}v_{outp} - g_{m2}v_{inp} \quad (B.12)$$

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From each of these,

$$\begin{cases} \frac{v_a}{r_{23}} = \frac{v_b}{r_{23}^2(sC_{cm} + g_{m5} + \frac{1}{r_{23}})} + \frac{g_{m5}v_{outm} - g_{m3}v_{inm}}{r_{23}(sC_{cm} + g_{m5} + \frac{1}{r_{23}})} \\ \frac{v_b}{r_{23}} = \frac{v_a}{r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})} + \frac{g_{m4}v_{outp} - g_{m2}v_{inp}}{r_{23}(sC_{cp} + g_{m4} + \frac{1}{r_{23}})} \end{cases}$$

which put in one the other gives us

$$\begin{cases} (sC_{cm} + g_{m5} + \frac{1}{r_{23}})v_a = \frac{v_a}{r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})} + \frac{g_{m4}v_{outp} - g_{m2}v_{inp}}{r_{23}(sC_{cp} + g_{m4} + \frac{1}{r_{23}})} + g_{m5}v_{outm} - g_{m3}v_{inm} \\ (sC_{cp} + g_{m4} + \frac{1}{r_{23}})v_b = \frac{v_b}{r_{23}^2(sC_{cm} + g_{m5} + \frac{1}{r_{23}})} + \frac{g_{m5}v_{outm} - g_{m3}v_{inm}}{r_{23}(sC_{cm} + g_{m5} + \frac{1}{r_{23}})} + g_{m4}v_{outp} - g_{m2}v_{inp} \end{cases}$$

This simplifies as

$$\begin{cases} v_a = \frac{r_{23}(g_{m4}v_{outp} - g_{m2}v_{inp}) + r_{23}^2(g_{m5}v_{outm} - g_{m3}v_{inm})(sC_{cp} + g_{m4} + \frac{1}{r_{23}})}{r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})(sC_{cm} + g_{m5} + \frac{1}{r_{23}}) - 1} \\ v_b = \frac{r_{23}(g_{m5}v_{outm} - g_{m3}v_{inm}) + r_{23}^2(g_{m4}v_{outp} - g_{m2}v_{inp})(sC_{cm} + g_{m5} + \frac{1}{r_{23}})}{r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})(sC_{cm} + g_{m5} + \frac{1}{r_{23}}) - 1} \end{cases}$$

We can already notice that for large r_{23} this acts much alike to the conventional circuit. While for small value of the resistance, the variation of v_a and v_b are slowed down.

Expressed as a function of the common and the differential component, this trends is clearer where $\gamma = r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})(sC_{cm} + g_{m5} + \frac{1}{r_{23}}) - 1$:

$$\begin{cases} v_a = \frac{g_{m4}r_{23} + g_{m5}r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})}{\gamma} v_{outc} - \frac{g_{m2}r_{23} + g_{m3}r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})}{\gamma} v_{inc} \\ \quad + \frac{g_{m4}r_{23} - g_{m5}r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})}{\gamma} \frac{v_{outd}}{2} + \frac{-g_{m2}r_{23} + g_{m3}r_{23}^2(sC_{cp} + g_{m4} + \frac{1}{r_{23}})}{\gamma} \frac{v_{ind}}{2} \\ v_b = \frac{g_{m5}r_{23} + g_{m4}r_{23}^2(sC_{cm} + g_{m5} + \frac{1}{r_{23}})}{\gamma} v_{outc} - \frac{g_{m3}r_{23} + g_{m2}r_{23}^2(sC_{cm} + g_{m5} + \frac{1}{r_{23}})}{\gamma} v_{inc} \\ \quad + \frac{-g_{m5}r_{23} + g_{m4}r_{23}^2(sC_{cm} + g_{m5} + \frac{1}{r_{23}})}{\gamma} \frac{v_{outd}}{2} + \frac{g_{m3}r_{23} - g_{m2}r_{23}^2(sC_{cm} + g_{m5} + \frac{1}{r_{23}})}{\gamma} \frac{v_{ind}}{2} \end{cases}$$

Finally, the offset can be found by setting $v_{outd} = 0$ which gives us

$$\begin{aligned} \frac{v_{offset}}{2} &= \left(g_{m5}g_{m3}r_{23}^2\left(sC_{cp} + g_{m4} + \frac{1}{r_{23}}\right) + g_{m4}g_{m2}r_{23}^2\left(sC_{cm} + g_{m5} + \frac{1}{r_{23}}\right) - r_{23}(g_{m4}g_{m3} + g_{m5}g_{m2}) \right) \quad (\text{B.13}) \\ &= (s(C_{Lp} - C_{Lm}) + g_{m7} + g_{m5} - g_{m6} - g_{m4})v_{outc}\gamma \\ &\quad - \left(g_{m5}^2\left(sC_{cp} + g_{m4} + \frac{1}{r_{23}}\right) - g_{m4}^2\left(sC_{cm} + g_{m5} + \frac{1}{r_{23}}\right) \right)v_{outc}r_{23}^2 \\ &\quad - \left(g_{m4}g_{m2}r_{23}^2\left(sC_{cm} + g_{m5} + \frac{1}{r_{23}}\right) - g_{m5}g_{m3}r_{23}^2\left(sC_{cp} + g_{m4} + \frac{1}{r_{23}}\right) + r_{23}(g_{m4}g_{m3} - g_{m5}g_{m2}) \right)v_{inc} \end{aligned}$$

Despite the extra complexity this engender, the static offset (for $s=0$) is greater than the static offset of the traditional version for large r_{23} . Indeed, the γ factor acts share the same equation than a cascode. This boosting the mismatch error with the output common mode voltage. Others errors are also boosted if

$$\left(g_{m5}g_{m3}r_{23}^2 \left(sC_{cp} + g_{m4} + \frac{1}{r_{23}} \right) + g_{m4}g_{m2}r_{23}^2 \left(sC_{cm} + g_{m5} + \frac{1}{r_{23}} \right) - r_{23} \left(g_{m4}g_{m3} + g_{m5}g_{m2} \right) \right) < g_{m2} + g_{m3}.$$

In term of delay, the differential output is expressed in function of the differential input as

$$v_{outd} \left[s(C_{Lp} + C_{Lm}) - (g_{m4} + g_{m5} + g_{m6} + g_{m7}) + \frac{g_{m4}^2 r_{23}^2 \left(sC_{cm} + g_{m5} + \frac{1}{r_{23}} \right) + g_{m5}^2 r_{23}^2 \left(sC_{cp} + g_{m4} + \frac{1}{r_{23}} \right) - 2g_{m4}g_{m5}r_{23}}{\gamma} \right] = \\ v_{ind} \frac{g_{m5}g_{m3}r_{23}^2 \left(sC_{cp} + g_{m4} + \frac{1}{r_{23}} \right) + g_{m4}g_{m2}r_{23}^2 \left(sC_{cm} + g_{m5} + \frac{1}{r_{23}} \right) - g_{m5}g_{m2}r_{23} - g_{m4}g_{m3}r_{23}}{\gamma}$$
(B.14)

which decompose as a gain factor and a time constant for the generation: the time constant is given to be

$$\tau \approx \frac{(C_{Lp} + C_{Lm})\gamma_0 + g_{m4}^2 r_{23}^2 C_{cm} + g_{m5}^2 r_{23}^2 C_{cp}}{-(g_{m4} + g_{m5} + g_{m6} + g_{m7})\gamma_0 + g_{m4}^2 r_{23}^2 \left(g_{m5} + \frac{1}{r_{23}} \right) + g_{m5}^2 r_{23}^2 \left(g_{m4} + \frac{1}{r_{23}} \right) - 2g_{m4}g_{m5}r_{23}}$$
(B.15)

The time constant expression is very similar to the one of the conventional strong arm. The part depending on r_{23} cannot be negative if the product of $g_{m4}r_{23}$ and $g_{m5}r_{23}$ are both greater than 1. $\gamma_0 = \gamma(s=0)$ being strictly positive, the time constant is reduced.

An interesting observation is for a perfectly matching where $g_m = g_{m4} = g_{m5}$, $C_c = C_{cp} = C_{cm}$, and $C_L = C_{Lp} = C_{Lm}$. The time constant reduces to

$$\tau \approx \frac{C_L\gamma_0 + 2g_m^2 r_{23}^2 C_c}{-(2g_m + g_{m6} + g_{m7})\gamma_0 + g_m^2 r_{23}^2 \left(g_m + \frac{1}{r_{23}} \right) + g_m^2 r_{23}^2 \left(g_m + \frac{1}{r_{23}} \right) - 2g_m^2 r_{23}}$$

for which the limit for large r_{23} gives

$$\lim_{r_{23} \rightarrow +\infty} \tau = \frac{C_L + 2C_c}{-(2g_m + g_{m6} + g_{m7}) + 2g_m}$$

In a way, even a very large resistance almost reach the same performance at the exception of parasitics introduced at nodes which increase C_c capacitance over the conventional circuit. Otherwise, extra $g_m^2 r_{23}$ in the denominator further reduce the time constant. In addition, the pmos transistors in the regeneration are those improving most the speed.

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This indicates a trade-off between the delay and the offset for this architecture which is not the case of the version introduced in [129].

B.3 Double Tail

Similarly to the SA latch, this section presents the details for the offset calculus and the model used to derive the offset and the delay equation. The small signal model of the Schinkel version is represented in

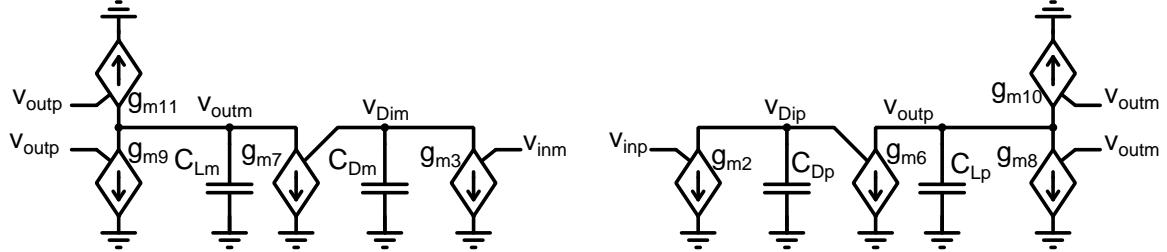


Figure B.3 Double Tail Small Signal Model

The application of KCL on v_{Dix} nodes results in

$$\begin{cases} sC_{Dp}v_{Dip} = -g_{m2}v_{inp} \\ sC_{Dm}v_{Dim} = -g_{m3}v_{inm} \end{cases}$$

while KCL on output nodes gives us

$$\begin{cases} sC_{Lp}v_{outp} = -g_{m6}v_{Dip} - (g_{m8} + g_{m10})v_{outm} \\ sC_{Lm}v_{outm} = -g_{m7}v_{Dim} - (g_{m9} + g_{m11})v_{outp} \end{cases}$$

Thus, the output voltages goes as

$$\begin{aligned} \frac{v_{outd}}{2} (s(C_{Lp} + C_{Lm}) - g_{m8} - g_{m9} - g_{m10} - g_{m11}) &= -\frac{v_{ind}}{2} \left(\frac{g_{m6}g_{m2}}{sC_{Dp}} + \frac{g_{m7}g_{m3}}{sC_{Dm}} \right) \\ &\quad + v_{inc} \left(\frac{g_{m6}g_{m2}}{sC_{Dp}} - \frac{g_{m7}g_{m3}}{sC_{Dm}} \right) \\ &\quad + v_{outc} (s(C_{Lp} - C_{Lm}) + g_{m8} + g_{m10} - g_{m9} - g_{m11}) \end{aligned} \quad (\text{B.16})$$

Assuming $v_{outd} = 0$ for the calculation of the input referred offset, the latter dependent on the input/output common mode and on mismatches as follow:

$$\begin{aligned} \frac{v_{offset}}{2} \left(\frac{g_{m6}g_{m2}}{sC_{Dp}} + \frac{g_{m7}g_{m3}}{sC_{Dm}} \right) &= +v_{inc} \left(\frac{g_{m6}g_{m2}}{sC_{Dp}} - \frac{g_{m7}g_{m3}}{sC_{Dm}} \right) \\ &+ v_{outc} (s(C_{Lp} - C_{Lm}) + g_{m8} + g_{m10} - g_{m9} - g_{m11}) \end{aligned} \quad (\text{B.17})$$

MINIMUM DC GAIN OF AN OTA IN AN INCREMENTAL- $\Delta\Sigma$

This section investigates the impact of the DC Gain of an OTA inside the SC-Integrator on the first stage of the proposed architecture: an Incremental- $\Delta\Sigma$.

The assumption made is a unity gain frequency of the OTA is such wide that the error on the settling of the integrator is only due to the OTA DC Gain.

Moreover, process mismatch is disregarded and the passive-adder with comparators are supposed to be ideal.

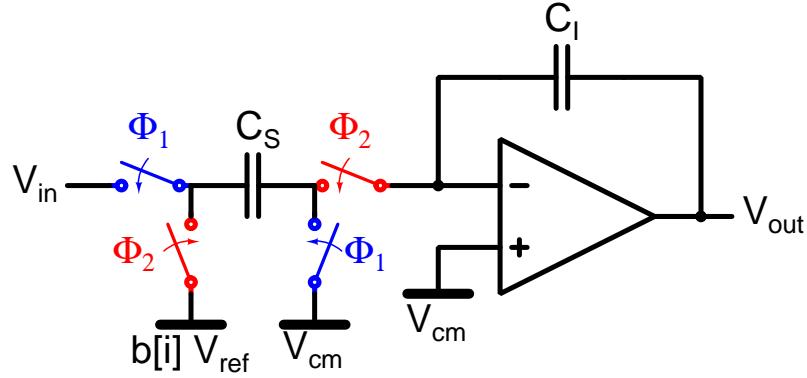


Figure C.1 Two-Phase SC Integrator implemented

In such circumstances the SC-Integrator of the Figure C.1 respects the equation (C.1) where A is the OTA DC Gain, C_S the sampling capacitor, and C_I the integration capacitor.

$$V_{out}[n] = V_{out}[n-1] \left(\frac{1 + \frac{1}{A}}{1 + \frac{1+C_S/C_I}{A}} \right) + (V_{in} - b[n-1]V_{ref}) \frac{C_S}{C_I} \left(\frac{1}{1 + \frac{1+C_S/C_I}{A}} \right) \quad (C.1)$$

One could note the ratio of C_S/C_I deeply impact the error at each integration step. In order to decrease the DC Gain requirement is to reduce this ratio to the maximum. Therefore a ratio of 1 is a good candidate.

By recurrence, the residue of this stage being the output of the integrator, the residue can be expressed as

$$V_{out}[n] = V_{out}[0] \left(\frac{1 + \frac{1}{A}}{1 + \frac{1+C_S/C_I}{A}} \right)^n + \frac{C_S}{C_I} \frac{1}{1 + \frac{1+C_S/C_I}{A}} \sum_{i=1}^n (V_{in} - b[n-1]V_{ref}) \left(\frac{1 + \frac{1}{A}}{1 + \frac{1+C_S/C_I}{A}} \right)^i \quad (C.2)$$

The incremental mode resetting at each new sample, the initial output value is zero. Therefore, the residue only depends on the transfer of charges from the sampling to the integration capacitor. The maximum of error is governed by the threshold voltage of the 1.5-bits quantizer following our architecture.

The error committed by a finite gain is thus

$$V_{error}[n] = \frac{C_S}{C_I} \sum_{i=1}^n (V_{in} - b[n-1]V_{ref}) \left[\left(\frac{(1 + \frac{1}{A})^i}{\left(1 + \frac{1+C_S/C_I}{A}\right)^{i+1}} \right) - 1 \right] \quad (\text{C.3})$$

To consider the ADC does not need calibration, we could assume that the error is below half LSB of the desired accuracy. In this case, the residue displays the maximum of the error at the transition between two adjacent codes. As the input range is $2V_{ref}$, a transition for a 1.5-bit quantizer whose threshold voltage are $\pm V_{ref}/2$ occurs at $V_{ref}/(2 \times OSR)(1 + 2k)$ where k is a signed integer.

$$\frac{V_{error}[n]}{V_{LSB}} = 2^{NBits} \frac{C_S}{C_I} \left(\frac{1}{4OSR} \left[\sum_{i=1}^n \left(\frac{(1 + \frac{1}{A})^i}{\left(1 + \frac{1+C_S/C_I}{A}\right)^{i+1}} \right) \right] - N \right) \quad (\text{C.4})$$

We could also assume this this equivalent to say the integral non linearity fits into the bounds for the desired accuracy. INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The INL-error magnitude then depends directly on the position chosen for this straight line. At least two definitions are common: 'best straight-line INL' and 'end-point INL'.

Best straight-line INL provides information about offset (intercept) and gain (slope) error, plus the position of the transfer function (discussed below). It determines, in the form of a straight line, the closest approximation to the ADC's actual transfer function. The exact position of the line is not clearly defined, but this approach yields the best repeatability, and it serves as a true representation of linearity.

End-point INL passes the straight line through endpoints of the converter's transfer function, thereby defining a precise position for the line. Thus, the straight line for an N-bit ADC is defined by its zero (all zeros) and its full-scale (all ones) outputs. The best straight-line approach is generally preferred, because it produces better results. The INL specification is measured after both static offset and gain errors have been nullified, and can be described as follows:

Let consider the case of the maximum error compared to a straight line passing by end-points of the transfer function:

$$INL = \max |V_{out}(code) - V_{out}(code_{min}) - (code - code_{min}) \times slope| \quad (\text{C.5})$$

where the slope is

$$slope = \frac{V_{out}(code_{max}) - V_{out}(code_{min})}{code_{max} - code_{min}} \quad (C.6)$$

For the sake of clarity, let us normalize voltages and codes between 0 and 1. As in a first order Incremental- $\Delta\Sigma$ the estimation is the average of output bits the normalized estimation of the output code is given to be $ec = \frac{1}{OSR} \sum_{i=1}^{OSR} b[i]$.

We deduce that the output estimation is the sum of ec and the residue weighted by 1/(2OSR). Considering $V_{out}(1)$ and $V_{out}(0)$ at a transition between two ‘extra’ codes, their are respectively given by $1 - V_{errormax}[n]$ and $V_{errormax}[n]$.

the INL being

$$INL = \max |V_{out}(ec) - V_{out}(0) - ec(V_{out}(1) - V_{out}(0))| \quad (C.7)$$

and replacing $V_{out}(1)$ and $V_{out}(0)$ by their value leads to

$$INL = \max |ec + V_{errormax}[n] + V_{error}[n, ec] - ec(1 - 2V_{errormax}[n])| \quad (C.8)$$

which admits a maximum of $4V_{errormax}[n]$

Therefore, to prevent a calibration with respect to the INL the DC gain constraint on the OTA is increased by 2-bits.

CLOCKED COMPARATORS METASTABILITY

Comparator metastability is ideally a deterministic process for initial ΔV_{out} of the cross-coupled inverters that is insufficient for regeneration to reach valid logic levels before the end of the available time T_{AVL} . In other words we can determine a ΔV_{out} range for which the time delay exceed the allotted time for the taking a decision. Unfortunately, the distribution of the differential input voltage and the noise [190] influence the distribution of the time delay. In consequence the likelihood of metastability is also affected. In this section we analyse both the differential input voltage distribution and the temperature impact on the metastability probability of comparators.

D.1 Input signal distribution dependency

The input probability distribution depends on the shape of the input voltage waveform. In this paper, we assume a laplace distribution over the full scale input range V_{FS} . In this case, the probability of comparator metastability is given by (D.1) for a Gaussian distribution of the delay at a given ΔV_{in} .

$$P(t > T_{AVL}, \Delta V_{in}) = \frac{1}{2} \left(1 - \operatorname{erf} \left(\frac{T_{AVL} - \mu_t(\Delta V_{in})}{\sqrt{2}\sigma_t(\Delta V_{in})} \right) \right) \quad (\text{D.1})$$

where μ_t is the average of the delay as a random variable, and σ_t the standard deviation of the delay assuming the law of large numbers applicable. In both the SA and the DT comparator the pre-amplification phase effectively multiplies the input range by a dynamic gain A_P [191], and one must subtract t_{lin} obtained in Section 4.2 from the T_{AVL} .

Considering that t_{lin} itself is a gaussian distributed random variable [191], errors on the estimation of the delay and its standard deviation can be translated into an error on the metastability probability. This error on the probability is given by (D.2) based on (D.1).

$$2\epsilon_{P_{met}} = \int_{-V_{FS}/2}^{+V_{FS}/2} \operatorname{erf} \left(\frac{T_{AVL} - \mu_t + \epsilon_\mu}{(\sigma_t + \epsilon_\sigma)\sqrt{2}} \right) P(\Delta V_{in}) d\Delta V_{in} - \int_{-V_{FS}/2}^{+V_{FS}/2} \operatorname{erf} \left(\frac{T_{AVL} - \mu_t}{\sigma_t \sqrt{2}} \right) P(\Delta V_{in}) d\Delta V_{in} \quad (\text{D.2})$$

In this equation, $P(\Delta V_{in})$ represents the probability to get a specific value of ΔV_{in} . In our case this is given by a laplace distribution of probability.

Clocked Comparators Metastability

Those general equation can be applied to other system based around a comparator by just changing the equation of the time delay (μ_t and σ_t).

D.2 Temperature variation

To consider the temperature impact on the comparators delay, we have considered that the temperature impact most the carrier mobility in the channel and the threshold voltage of transistors.

Assuming mobility variation take over threshold voltage variation, the probability sensitivity to the temperature of (D.1) is defined by equation (D.3) where A_P is the amplification factor $\Delta V_{out}(t_{lin})/\Delta V_{in}$.

$$\frac{d}{dT} P(t > T_{AVL}, \Delta V_{in}) = \frac{\exp\left(-\left(\frac{T_{AVL}-\mu_{delay}(T, \Delta V_{in})}{\sqrt{2}\sigma_{delay}(\Delta V_{in})}\right)^2\right)}{\sqrt{2\pi}\sigma_{delay}(\Delta V_{in})} \frac{d}{dT} t(T, \Delta V_{in}) \quad (\text{D.3})$$

$$\frac{d}{dT} t(T, \Delta V_{in}) \approx \frac{3\tau}{2T_0} \sqrt{\frac{T}{T_0}} \left(\log\left(A_P \frac{V_{logic}}{\Delta V_{out}(t_{lin})} \left(\frac{T}{T_0}\right)^{\frac{3}{2}}\right) + 1 \right) \quad (\text{D.4})$$

By being strictly positive, the increasing of temperature always inflates probability to be metastable. In consequence, the temperature will move the probability of metastability towards greater T_{AVL} .

D.3 Metastability of synchronizers

In ADCs, the comparator is most of the time followed by synchronizers to reduce the likelihood of logic errors propagating past the comparator. We chose to add digital flip-flops (DFF) to act as synchronizers, as show in the Figure D.1. The clock CLK is defined by his period T_{CLK} whose duty cycle is 50 %.

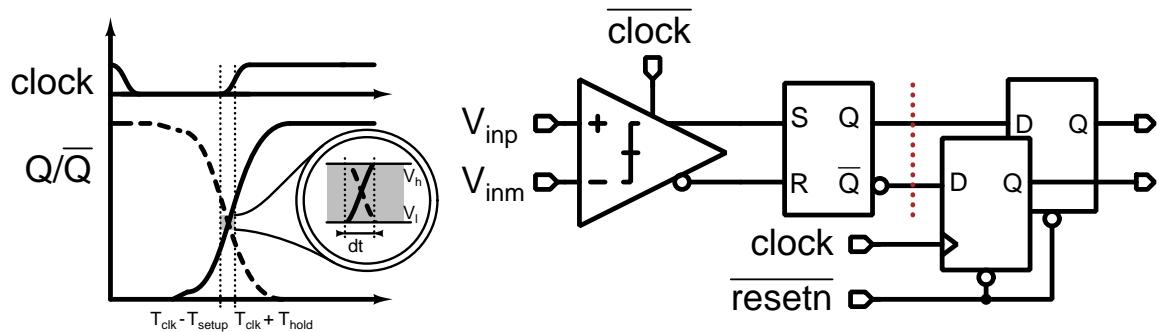


Figure D.1 Metastability input range and test circuit

Comparator metastability may engender the violation of the set-up and hold times of the DFF. In other words, the DFF clock transition may happen too close to the region where the DFF input is between V_l and V_h : the voltage metastable window. Assuming the independence of the probability to be in the forbidden voltage range and the probability to have a transition in the forbidden time span, the probability to be in this generating zone is defined by (D.5).

$$P(\text{MetastabilityZone}, \Delta V_{in}) = P\left(t \in \left[\frac{T_{clk}}{2} \pm \frac{T_{hold}}{T_{setup}}\right], \Delta V_{in}\right) \times P(V_{out} \in [V_l, V_h]) \quad (\text{D.5})$$

For the sake of simplicity, only the regeneration time is considered since the linear time of comparator can be subtracted to $T_{clk}/2$. And its variation is far less. Hence, the probability to be in the forbidden voltage range at any time is given by equation (D.6) where τ_{reg} is the regeneration time constant. This probability depends from the temperature due to $V_{out}(t_{lin})$.

$$P(V_{out} \in [V_l, V_h]) \approx \frac{\tau_{reg} \ln(V_h/V_l)}{\tau_{reg} \ln(V_{logic}/V_{out}(t_{lin}))} \quad (\text{D.6})$$

And, the probability to be in the forbidden time span is easily calculable with the cumulative probability function of the comparator's delay given by the equation (D.1)[191].

Therefore, the probability to be in the metastability generating zone is defined by (D.7) considering any differential input voltage distribution.

$$P(\text{MetastabilityZone}) = \int_{-V_{FS}/2}^{+V_{FS}/2} P(\text{MetastabilityZone}, \Delta V_{in}) P(\Delta V_{in}) d\Delta V_{in} \quad (\text{D.7})$$

In order to compare the SA and the DT comparators, all circuits have been simulated in $0.18\text{-}\mu\text{m}$ CMOS technology with $V_{DD} = 1.8\text{V}$. The comparators were designed for offset standard variation of 3 mV at the input common mode voltage of 0.9 V. For the following results, the test setup is depicted by the Figure D.1. The DFF time constraints are taken to be $t_{setup} = 135\text{ps}$ and $t_{hold} = 70\text{ps}$ while the metastability input range is less than $1\text{ }\mu\text{V}$ around 794 mV and varies with the temperature.

D.4 process and temperature variation on the metastability

The Figure D.2 depicts the probability for the DT and the SA latches, to enter the metastable zone of DFFs at the clock falling edge. As expected, increasing the temperature decreases the regeneration

Clocked Comparators Metastability

time constant, and the pre-amplification gain. In turn, the Probability Density Function (PDF) is shifted to lower clock frequencies as explained by the equation (D.3). This shift is not linear with the temperature but varies according to the variation of the mobility in the CMOS cross-coupled inverters. Based on (D.4) the estimated $\Delta T_{clk}/2\tau_{reg}$ is 3.3 while the simulation results provide a $\Delta T_{clk}/2\tau_{reg}$ of 3 from -50°C to $+175^{\circ}\text{C}$ for both comparators. Therefore, the temperature variation

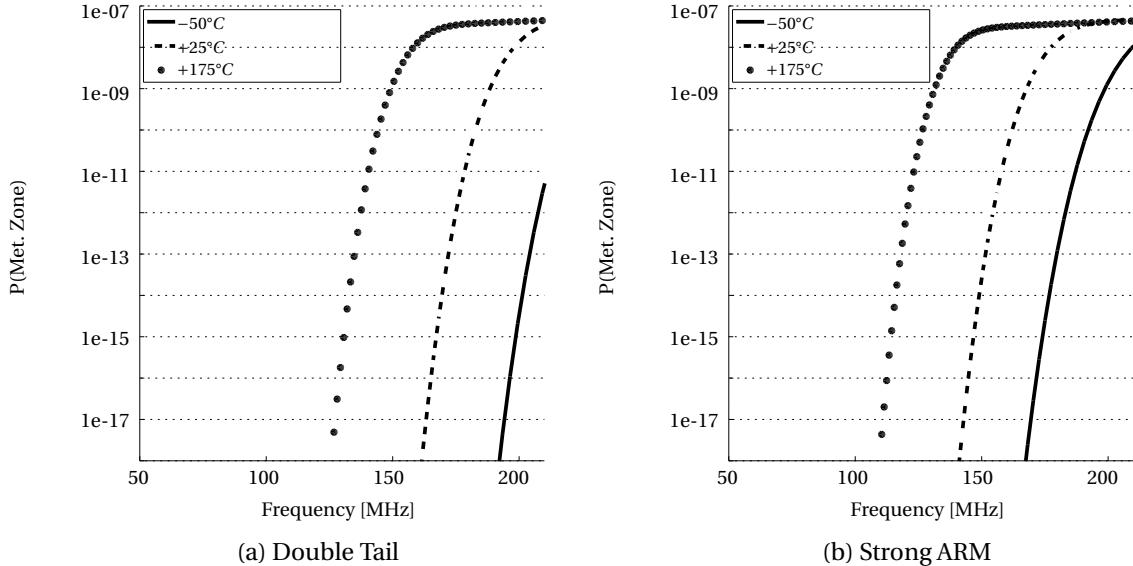


Figure D.2 $P(\text{Met}_Z)$ of DFFs for -50°C , $+25^{\circ}\text{C}$, $+175^{\circ}\text{C}$, $\Delta V_{in} \in \pm 450\text{mV}$

to generate metastability is more linked to the fabrication process than to the topology.

As a proof the derivative of the probability of metastability with respect to frequency versus the advancement in the rising of probability is represented in the Figure D.3.

Figure D.3 (a) compares the topology at 25°C . We conclude that the topology does not impact variation of probability.

Figure D.3 (b) represents the variation of the probability for the double tail for three different temperatures. The temperature impacts most the corner than the slope of the rising probability.

For both comparators, the variation of probability over temperature exhibited are similar and only the value of probability change due to a SA comparator being slower than the DT one. At 25°C and 175°C for a clock frequency of 150 MHz, the probability to generate metastable DFFs output is less than 10^{-18} and 5×10^{-10} for the DT. For the SA the probability is 2×10^{-17} and 3×10^{-9} .

Then the probability of comparators to be in a metastable state is depicted by the Figure D.4. Compared to previous probability, this probability rises up to 1 with the increasing clock frequency and the temperature shift the PDF to smaller clock frequencies. But it also demonstrates that transition from low to high probability is never instantaneous, and its slope does not depends on

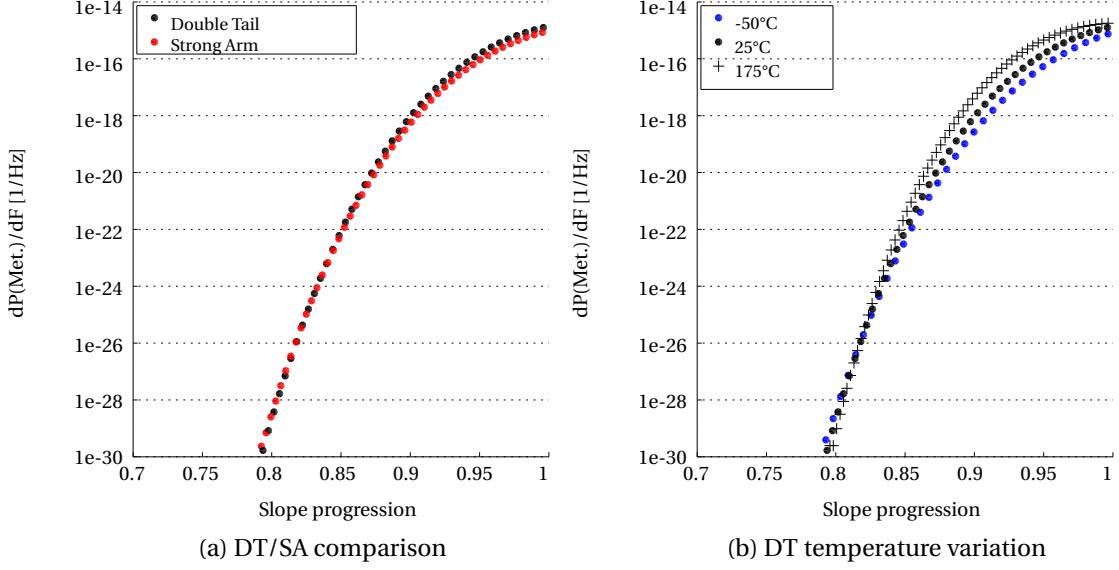


Figure D.3 Derivative of the probability to generate metastability

temperature. With layout respecting good-matching practices, the slope is a result of either the noise as reported in [191], or the process variation, or the repartition of ΔV_{in} as a random variable. In the results presented the noise is not taken into account.

From (D.2), those results in the absence of noise and hysteresis have an estimated error at 175°C of 1.6×10^{-13} and 3×10^{-13} respectively for the DT, Figure D.4a, and the SA, Figure D.4b, on the probability of metastability where the probability level is 10^{-9} .

Concerning the probability of generating metastability and to be metastable, they do not follow the same law of probability. Indeed, the PDF of generating metastability decreases for very high frequencies since delay is far much greater than the allotted time, and reach with an ever smaller probability the metastable zone of DFFs. Moreover, increasing the differential input shifts the PDF to high frequencies. Therefore, an slowly increasing top appears on the PDF.

Clocked Comparators Metastability

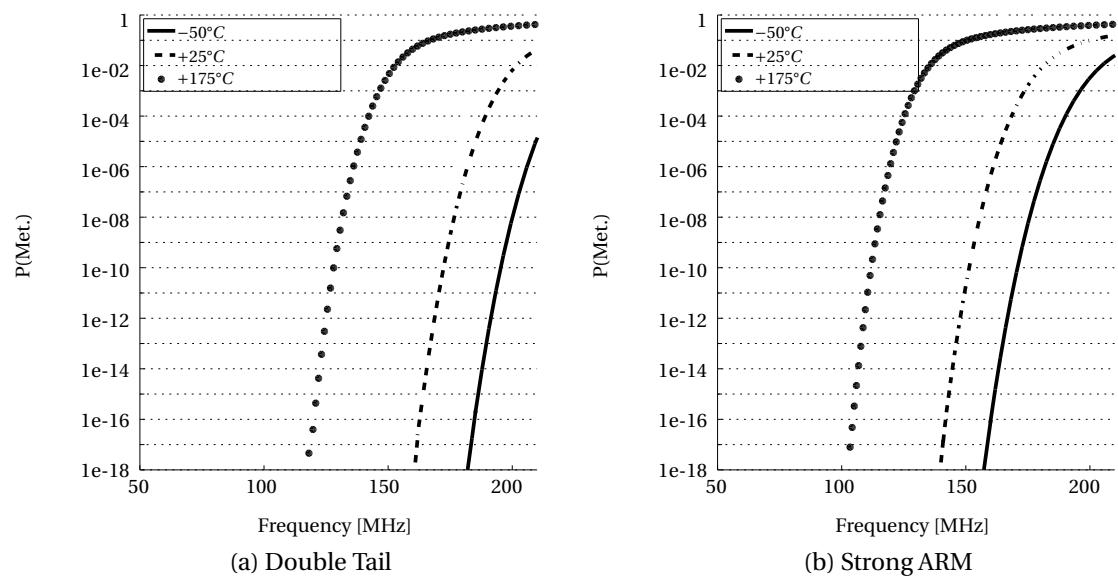


Figure D.4 $P(\text{Metastability})$ of latches for -50°C , $+25^{\circ}\text{C}$, $+175^{\circ}\text{C}$, $\Delta V_{in} \in \pm 450\text{mV}$

PACKAGING CONSIDERATIONS FOR HIGH TEMPERATURE

The temperature affects the printed circuit board in several manner which are decomposed into material intrinsic properties alteration and material-material interfaces phenomena. For tests and measurements, we should consider both the mechanical and the electrical properties of the IC and the of the test boards.

E.1 Package

The package of an integrated circuit is an interface to the environment surrounding the chip whose desirable properties are a low thermal resistance to prevent the heat to be trap inside the package degrading ever more the Silicon electrical performance. The target design is close to the operating region where the carrier density is getting as sparse as within an intrinsic silicon bloc. Therefore, the heat should be evacuated as quickly as possible while the selected package is as close as possible to the final one for relevant measurements. In addition to that, test under high temperature gives enough energy for most redox chemical reactions in which oxidations of contact and metals are expected to occurs.

Exposed to the environment, the package is thus selected based on its thermal-resistance to dissipate heat, its electrical insulation, and its protection from oxidation among many.

In order to output high frequencies signal for debug purpose, parasitic are intended to be minimized. This consider both the wire-bonding and the pins.

For the sake of simplicity, Table E.1 compares the properties of traditional package (plastic and ceramic) with fully closed encapsulation. Indeed, as large area of METTP is not allowed by the process manufacturing to prevent antenna effect, large area of metal have slits exposing the silicon based dielectric to the light. Partially closed or open IC allows visual verification of wire-bonding at the cost of substrate ionisation by the absorption of light being more likely as the temperature increase (E_g is decreasing and a band gap shift occurs with the temperature [192, 193] while the fermi-dirac distribution becomes wider).

For high temperature integrated circuits, the most physically robust solution is a ceramic package with a caution on the dielectric constant value which is have a large discrepancy with most PCB material. Therefore, the plastic package is thus the most appropriate for test temperature below 160°C. Willing to test the IC at 175°C, and a chip size of 1.3 mm x 1.3 mm while a CLCC68 package would be of 25.4 mm x 25.4 mm the inductance of a wire connected at a corner would

Packaging considerations for high temperature

Table E.1 Packing comparison for high temperature circuits

Mechanical Properties	Ceramic Package CLCC68	Plastic Package PLCC68 (PPS)	Glob Top S7503	Glob Top 50300HT
Young Modulus [GPa]	150 – 190	6 – 11	NC	NC
Vickers Hardness [GPa]	5.9 – 9	5	NC	NC
Viscosity [Pa.s @ 10 rpm]	NC	NC	80 – 100	120 – 140
Shore D	NC	NC	85	95
Water Absorption [%]	0	0.02	0.14	0.4
Thermal Properties				
Coefficient of Thermal Expansion [μK^{-1}]	9.6 – 11.5	33	193	18
Thermal Conductivity [W/mK]	2 – 5	0.29	0.22	0.63
Glass Transition Temperature Tg [°C]	>175	170	175	165
Electrical Properties				
Dielectric Constant [@25°C] and Loss tangent	6.5 / 0.0003 @ 1 MHz	3.0 / 0.0001 @ 1 kHz	3.1 / 0.0005 @ 1 kHz	3.2 / 0.0009 @ 1 kHz
Volume Resistivity [10^{14}]	0.01 – 4	0.1 – 10	1	3.3

be of 26 nH. a Glob Top solution is good compromise which allows a chip-on-board connection limiting the inductance to 7 nH.

Considering discrete buffers whose pin's capacitance are 20 pF, the capacitance of the PCB trace of 7 pF and a pad capacitance of the IC of 1.9 pF, the cut-off frequency is boosted from 180 MHz to 353 MHz in the worst case. From another point of view the sampling frequency of ADC being 20 MHz, the settling have 9 to 17 times the time constant of the line.

One precaution that have been overlooked in the design but have a deep impact on results is a protection for the Glob Top to reduce the sensitivity to air pressure variation. In order to use commercial on-the-shelves components on a motherboard, the test over temperature are performed with a thermal stream 5000 from MPI. The hot air is blown on the area delimited by its thermal enclosure. The temperature increasing the glob top tends to be malleable and the air pressure on the wire bonding. To limit the impact a cover have been placed over the daughter-board to let the air surrounding the IC heating but preventing a direct blown air on the IC as depicted by Figure E.1.

E.2 Boards

With regards to the PCB conception, the temperature increasing inflates the dielectric. The distance between metal layers changing, the dielectric constant is thus temperature dependant (at least from a geometrical point of view). Changes in z-axis CTE and dielectric constant as a function of

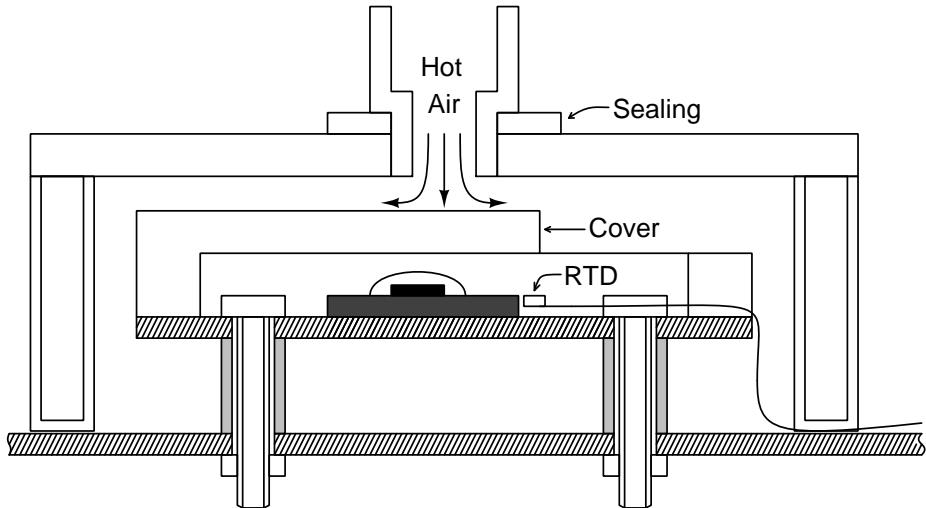


Figure E.1 Protection against the blown air pressure variation inside the thermal enclosure of the thermal stream

temperature can significantly impact the impedance of strip transmission lines fabricated on that material while engendering a mechanical stress on soldering points and vias.

Because a material can undergo such a drastic change in CTE, it becomes mechanically and electrically unstable when operating above a defined temperature T_g , when the dielectric become soft and malleable. The PCB should always be maintained below that temperature except for short-duration processing steps, such as solder reflow.

In the special of the motherboard, more precisely at connections points with the daughter-board, pins from one connector are soldered to transmission lines. The pins connectors and transmission lines being in copper while the soldering is a dissimilar metal, an electromotive force appear at the junction coming from a thermal difference between each metal. Also called Seebeck effect, for a Copper-Lead-Tin Solder the coefficient of the electromotive force is $5 \mu V/^\circ C$ which sufficient to generate an error of $500 \mu V$ for $100^\circ C$ between the two.

In order to perform the characterisation of the ADC whose accuracy reach 12-bits with an input excursion of $\pm 1 V$, the thermal difference shall not be higher than $24^\circ C$. One way to cope with this effect is by waiting the establishment of the temperature before a characterisation at a new temperature. In addition for sensitive nodes, differential signalling is recommended.

Even if differential signalling is done, a high speed signal over long trace is prone to power reflection. Impedance matching is consider in the design of the trace for both analog and digital signals from 25 MHz to 100 MHz. A solution based on motherboard for signal generation and reshaping and a daughter-board with only the test chips under temperature is the most effective way to achieve the matching with test devices.

Packaging considerations for high temperature

On transmission lines for high speed digital, bidirectional buffers are added to keep the signal end-to-end clean. Digital buffers benefits are three fold: First, they adapt the signal from a 1.8 V voltage domain to a more traditional 3.3 V to 5 V of digital test device (LVDS IP usually consider a 3.3 V voltage domain). Second, splitting the signal path into several chunk, the impedance matching is easier to realize between the IC and the buffers. And as the digital lines of test devices have an impedance of $150\ \Omega$ to $300\ \Omega$, the matching not being perfect from the test devices to the buffers will only have low-reflection capacitance. During the conception the maximum allowed power reflected is 10 % which correspond to a maximum VSWR (voltage standing wave ratio) equal to 1.22 which is in nutshell an error due to mismatch of $30\ \Omega$. Third without them, the digital pads of the IC should provide a large current to charge and pump the capacitance of test devices. The large transient current generate a large noise whose decoupling from the analog core is more difficult. By the addition of buffers, the capacitive load is reduced and the generated noise is decreased.

To enhance the performance, it is critical to place the reservoir capacitor close to the ADC's sensitive inputs. Among the most sensitive ones are reference input pins, input voltages, and power supplies. While the input pins are high speed signals, the impedance matching is suppose to be sufficient. For practical reason small capacitors are needed to filter out possible coupling noise.

But for DC signals such references and power supplies, the filtering network depends on the load and the current profile. For instance, on the SAR sub-ADC the power supply shall be feed large transient current the comparator while the reference drops only while the reference is connected to the DAC. The capacitor acts as a charge reservoir with charge pumped by the load and re-filled at a rate depending from the resistivity of the path for re-filling, Figure E.2. To decrease the minimum time to recover, decoupling capacitor have been split into one inside the IC chip and several outside. To prevent oscillations the ESR of decoupling capacitors is minimized by using multiple vias to a ground plane and using wide traces to connect them. Ceramic capacitors with X7R dielectric are a good choice close to IC where the temperature is the highest ($175\ ^\circ\text{C}$). Then outside at ambient temperature a large $470\ \mu\text{F}$ electrolytic capacitor filter the voltage provided by the power supply source, such as an Hameg HMP 4040.

For the sake of clarity others phenomena such as power derating, voltage derating, temperature drift,... are considered but not detailed.

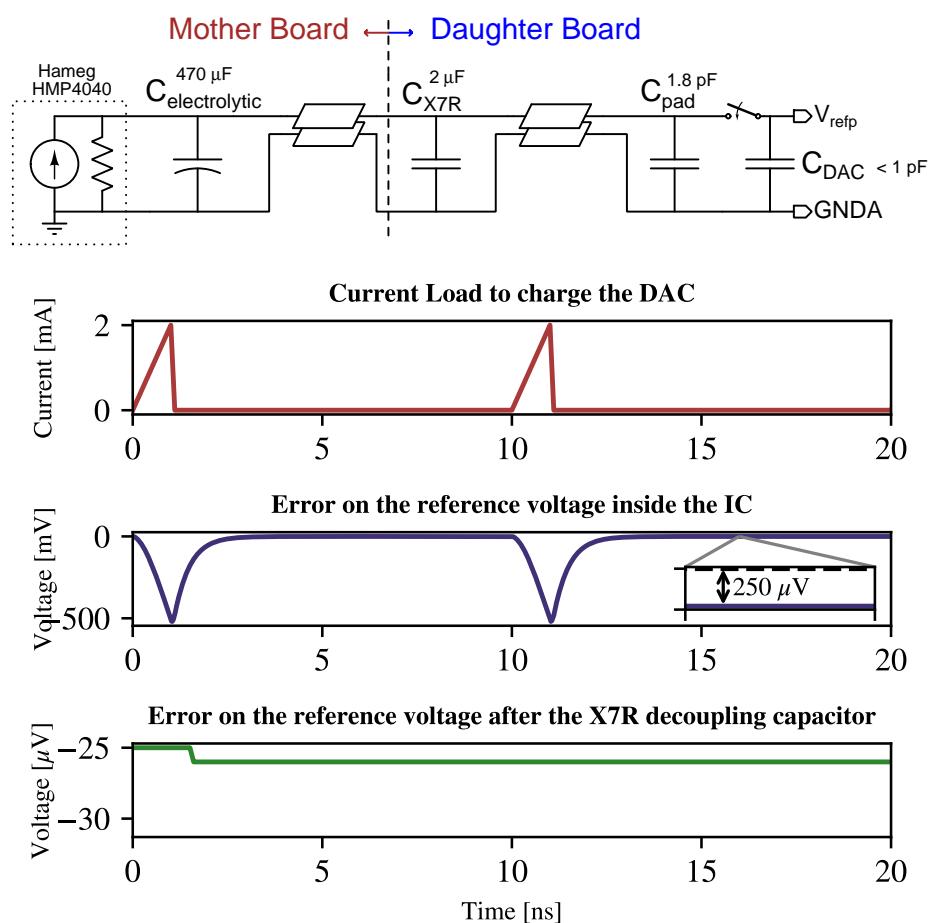


Figure E.2 Decoupling strategy to reduce recovery time and the settling error on references

ACCURACY NEEDED FOR COMPARATORS OFFSET MEASUREMENT

Let us assume, for the average voltage of the offset N samples ($x_i \sim N(\bar{x}^*, \sigma^2)$) The average and the standard deviation is thus given by:

$$\bar{x} = \frac{1}{N} \sum_{i=0}^{N-1} x_i \quad (\text{F1})$$

and

$$\sigma_{offset} = \sqrt{\frac{1}{N-1} \sum_{i=0}^{N-1} (x_i - \bar{x})^2} \quad (\text{F2})$$

The error committed with respect to the true offset value (\bar{x}^*) is calculated by:

$$\varepsilon_{\bar{x}} = \bar{x}^* - \bar{x} = \bar{x}^* - \frac{1}{N} \sum_{i=0}^{N-1} x_i \quad (\text{F3})$$

Thus a non-biased measure gives an expectation of the error tending to zero. This is equivalent to say that the probes have no offset and have been calibrated.

In consequence, the error for a given measure comes from the standard deviation of a measure: the precision of probes.

$$Var(\varepsilon_{\bar{x}}) = Var(\bar{x}^*) + Var() = \frac{1}{N^2} \sum_{i=0}^{N-1} \sum_{j \neq i} (x_i - x_j)^2 \quad (\text{F4})$$

Since each sample have the same variance and supposed sufficiently separated in the time to not be correlated (memory effect of the probe), the variance of the error can be simplified into

$$Var(\varepsilon_{\bar{x}}) = \frac{\sigma^2}{N} \quad (\text{F5})$$

So to limit the error on the offset to 5% of the expected offset's standard deviation for 10 samples, the σ should be less than

$$\sigma < \sigma_{offset} \sqrt{10} \frac{5}{100} = 3mV \times 0.158 = 474\mu V \quad (\text{F6})$$

FREQUENCY JITTER IMPACT ON THE DELAY MEASUREMENT CIRCUIT

This appendix has the goal to estimate the error on the delay measurement due to an error on the frequency measurement. We consider the error on frequency due to the jitter.

The estimated error on the delay is linked to the variation in frequency of the calculated DLY_FREQ frequency in each operating mode (calibration mode and run mode) as follows

$$\begin{aligned} \varepsilon_{t_{\text{delay}}+t_{\text{reset}}} &= \frac{1}{N} \left(\frac{1}{F_1} - \frac{1}{F_2} \right) \left(1 - \frac{1}{1 + \frac{F_{\text{jitter}1}}{F_1} + \frac{F_{\text{jitter}2}}{F_2} + \frac{F_{\text{jitter}1}}{F_1} \frac{F_{\text{jitter}2}}{F_2}} \right) \\ &\quad - \frac{1}{NF_1 F_2} \frac{\frac{F_{\text{jitter}1}}{F_1} + \frac{F_{\text{jitter}2}}{F_2}}{1 + \frac{F_{\text{jitter}1}}{F_1} + \frac{F_{\text{jitter}2}}{F_2} + \frac{F_{\text{jitter}1}}{F_1} \frac{F_{\text{jitter}2}}{F_2}} \end{aligned} \quad (\text{G.1})$$

where F_1 and F_2 are respectively the frequency measured due when CALIBN=1 and CALIBN=0, $F_{\text{jitter}i}$ is the measured frequency jitter on the frequency F_i , and N represents the frequency divider ratio.

If we consider $\frac{F_{\text{jitter}i}}{F_i}$ follows a centered normal distribution of variance σ_i^2 , thus the expectation of the error is approximately zero and the variance of the error is given by the following formula:

$$Var(\varepsilon_{t_{\text{delay}}+t_{\text{reset}}}) = \left(\frac{1}{N^2} \left(\frac{1}{F_1} - \frac{1}{F_2} \right)^2 + \frac{1}{(NF_1 F_2)^2} \right) (\sigma_1^2 + \sigma_2^2) \quad (\text{G.2})$$

This is based on the Taylor expansion to the first order of $1/(1+x)$. In consequence, bigger the number N is better is the accuracy of the measure with respect to the frequency jitter. Unfortunately, this comes at a price on the resolution of the frequency meter used and the cumulative noise of the frequency divider which alter the phase.

With a peak-jitter of 140 Hz on DLY_FREQ for a frequency generated of 6 MHz and 2.9 MHz, the estimated error coming from the jitter is 6.5 ps. Therefore, the error introduced by the jitter of the circuit is considered negligible if the error exceed 100 ps.

BIBLIOGRAPHY

- [1] P. M. Ferreira, H. Cai, and L. Naviner, "Reliability Aware AMS / RF Performance Optimization," in *Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design*, M. FAKHFAKH, E. Tlelo-Cuautle, and M. H. S. Fino, Eds., IGI-Global, 2014, p. 27.
- [2] K. Chain, J.-h. Huang, J. Duster, P. K. Ko, and C. Hu, "A MOSFET electron mobility model of wide temperature range (77 - 400 K) for IC simulation," *Semiconductor Science and Technology*, vol. 12, pp. 355–358, 1997.
- [3] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: High-temperature electronics," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 27, no. 3, pp. 164–176, Jul. 2004.
- [4] "Road vehicles — Environmental conditions and testing for electrical and electronic equipment — Part 4: Climatic loads," International Organization for Standardization, Standard, Apr. 2010.
- [5] H. Cai, H. Petit, and J.-F. Naviner, "A Hierarchical Reliability Simulation Methodology for AMS Integrated Circuits and Systems," *J. Low Power Electron.*, vol. 8, no. 5, pp. 697–705, Dec. 2012.
- [6] XFAB Mixed-Signal Foundry Experts. (2018). XT018 - 0.18 Micron Modular Trench Isolated SOI CMOS Technology, [Online]. Available: <https://www.xfab.com/technology/soi/018-um-xt018/> (visited on 08/29/2018).
- [7] B. Murmann. (2018). ADC Performance Survey 1997-2018, [Online]. Available: <https://web.stanford.edu/~murmann/adcsurvey.html> (visited on 08/29/2018).
- [8] R. J. V. D. Plassche and R. E. J. V. D. Grift, "A high-speed 7 bit a/d converter," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 6, pp. 938–943, Dec. 1979.
- [9] R. van de Grift, I. W. J. M. Rutten, and M. van der Veen, "An 8-bit video adc incorporating folding and interpolation techniques," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, pp. 944–953, Dec. 1987.
- [10] B. Nauta and A. G. W. Venes, "A 70-ms/s 110-mw 8-b cmos folding and interpolating a/d converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1302–1308, Dec. 1995.
- [11] P. Vorenkamp and R. Roovers, "A 12-b, 60-msample/s cascaded folding and interpolating adc," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1876–1886, Dec. 1997.
- [12] R. C. Taft, P. A. Francese, M. R. Tursi, O. Hidri, A. MacKenzie, T. Hoehn, P. Schmitz, H. Werker, and A. Glenny, "A 1.8 v 1.0 gs/s 10b self-calibrating unified-folding-interpolating adc with 9.1 enob at nyquist frequency," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3294–3304, Dec. 2009.

Bibliography

- [13] M. Buck, M. Grözing, R. Bieg, J. Digel, X. Q. Du, P. Thomas, M. Berroth, M. Epp, J. Rauscher, and M. Schlumpp, "A 6-gs/s 9.5-b single-core pipelined folding-interpolating adc with 7.3 enob and 52.7-dbc sfdr in the second nyquist band in 0.25- μ m sige-bicmos," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 414–422, Feb. 2017.
- [14] H. Pan, M. Segami, M. Choi, J. Cao, F. Hatori, and A. Abidi, "A 3.3 v, 12b, 50msample/s a/d converter in 0.6 μ m cmos with over 80 db sfdr," in *2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056)*, Feb. 2000, pp. 40–41.
- [15] W. E. M. Costa, S. A. Rodrigues, R. C. S. Freire, S. Y. Catunda, and F. R. de Sousa, "8-bit folding adc based on switched capacitor," in *2013 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, May 2013, pp. 1559–1563.
- [16] M.-J. Choe, B.-S. Song, and K. Bacrania, "An 8-b 100-msample/s cmos pipelined folding adc," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 2, pp. 184–194, Feb. 2001.
- [17] S. Hein and A. Zakhor, "On the stability of sigma delta modulators," *IEEE Transactions on Signal Processing*, vol. 41, no. 7, pp. 2322–2348, Jul. 1993.
- [18] R. T. Baird and T. S. Fiez, "Stability analysis of high-order delta-sigma modulation for adc's," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 41, no. 1, pp. 59–62, Jan. 1994.
- [19] N. S. R. 1956-, *Delta-Sigma data converters : theory, design, and simulation*, eng. New York: IEEE Press, 1996.
- [20] F. Medeiro, A. Pérez-Verdú, and A. Rodríguez-Vázquez, *Top-Down Design of High-Performance Sigma-Delta Modulators*. Kluwer Academic, 1999, p. 303.
- [21] J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental delta; sigma; converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 4, pp. 678–690, Apr. 2004.
- [22] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Markus, J. Silva, and G. C. Temes, "A low-power 22-bit incremental adc," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562–1571, Jul. 2006.
- [23] T. C. Caldwell and D. A. Johns, "Incremental data converters at low oversampling ratios," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1525–1537, Jul. 2010.
- [24] S. Au and B. H. Leung, "A 1.95-v, 0.34-mw, 12-b sigma-delta modulator stabilized by local feedback loops," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 321–328, Mar. 1997.
- [25] J. N. Babanezhad, "A low-output-impedance fully differential op amp with large output swing and continuous-time common-mode feedback," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 12, pp. 1825–1833, Dec. 1991.

Bibliography

- [26] R. T. Baird and T. S. Fiez, "A low oversampling ratio 14-b 500-khz delta; sigma; adc with a self-calibrated multibit dac," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 312–320, Mar. 1996.
- [27] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.
- [28] K. Yamamoto and A. Carusone, "A 1-1-1-1 mash delta-sigma modulator with dynamic comparator-based otas," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 8, pp. 1866–1883, Aug. 2012.
- [29] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. D. Muro, and S. W. Harston, "A cascaded sigma-delta pipeline a/d converter with 1.25 mhz signal bandwidth and 89 db snr," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1896–1906, Dec. 1997.
- [30] G. Cauwenberghs and G. C. Temes, "Adaptive digital correction of analog errors in mash adcs. i. off-line and blind on-line calibration," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 7, pp. 621–628, Jul. 2000.
- [31] B. K. Jeon, S. K. Hong, and O. K. Kwon, "A low-power 12-bit extended counting adc without calibration for cmos image sensors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. PP, no. 99, pp. 1–1, 2017.
- [32] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit delta; sigma; a/d and d/a converters using data weighted averaging," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753–762, Dec. 1995.
- [33] C. H. Chen, Y. Zhang, T. He, and G. C. Temes, "An incremental analog-to-digital converter with multi-step extended counting for sensor interfaces," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 77–80.
- [34] A. Agah, K. Vleugels, P. B. Griffin, M. Ronaghi, J. D. Plummer, and B. A. Wooley, "A high-resolution low-power incremental $\Sigma\Delta$ adc with extended range for biosensor arrays," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1099–1110, Jun. 2010.
- [35] L. Rossi, S. Tanner, and P. A. Farine, "Performance analysis of a hybrid incremental and cyclic a/d conversion principle," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1383–1390, Jul. 2009.
- [36] Q. Liu, A. Edward, D. Zhou, and J. Silva-Martinez, "A continuous-time mash 1-1-1 delta-sigma modulator with fir dac and encoder-embedded loop-unrolling quantizer in 40-nm cmos," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, no. 99, pp. 1–12, 2017.

Bibliography

- [37] F. Michel and M. S. J. Steyaert, "A 250 mv 7.5 μ w 61 db snr sc $\Delta\Sigma$ modulator using near-threshold-voltage-biased inverter amplifiers in 130 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 709–721, Mar. 2012.
- [38] S. Lee, A. P. Chandrakasan, and H. S. Lee, "A 12b 5-to-50ms/s 0.5-to-1v voltage scalable zero-crossing based pipelined adc," in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, Sep. 2011, pp. 355–358.
- [39] S. K. Lee, S. J. Park, H. J. Park, and J. Y. Sim, "A 21 fJ/conversion-step 100 ks/s 10-bit adc with a low-noise time-domain comparator for low-power sensor interface," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 651–659, Mar. 2011.
- [40] L. Brooks and H. S. Lee, "A 12b, 50 ms/s, fully differential zero-crossing based pipelined adc," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3329–3343, Dec. 2009.
- [41] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U. K. Moon, "Ring amplifiers for switched capacitor circuits," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012.
- [42] Y. Lim and M. P. Flynn, "A 100 ms/s, 10.5 bit, 2.46 mw comparator-less pipeline adc using self-biased ring amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct. 2015.
- [43] ——, "A 1 mw 71.5 db snr 50 ms/s 13 bit fully differential ring amplifier based sar-assisted pipeline adc," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015.
- [44] K. M. Megawer, F. A. Hussien, M. M. Aboudina, and A. N. Mohieldin, "An adaptive slew rate and dead zone ring amplifier," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 305–308.
- [45] Y. Cao, Y. Chen, T. Zhang, F. Ye, and J. Ren, "An improved ring amplifier with process- and supply voltage-insensitive dead-zone," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2017, pp. 811–814.
- [46] D. G. Nairn and C. A. T. Salama, "Current-mode algorithmic analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 997–1004, Aug. 1990.
- [47] Z. Wang, "Design methodology of cmos algorithmic current a/d converters in view of transistor mismatches," *IEEE Transactions on Circuits and Systems*, vol. 38, no. 6, pp. 660–667, Jun. 1991.
- [48] G. Khodabndehloo, M. Mirhassani, and M. Ahmadi, "An area-speed efficient method for current mode analog to digital converters," in *2009 European Conference on Circuit Theory and Design*, Aug. 2009, pp. 201–204.

Bibliography

- [49] V. Bhatia, N. Pandey, and A. Bhattacharyya, "Performance comparison of an algorithmic current-mode adc implemented using different current comparators," in *2011 International Conference on Multimedia, Signal Processing and Communication Technologies*, Dec. 2011, pp. 141–144.
- [50] B. Murmann and B. E. Boser, "A 12-bit 75-ms/s pipelined adc using open-loop residue amplification," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
- [51] K. Inoue, T. Matsuura, A. Hyogo, and H. San, "Non-binary cyclic and binary sar hybrid adc," in *2017 MIXDES - 24th International Conference "Mixed Design of Integrated Circuits and Systems"*, Jun. 2017, pp. 105–109.
- [52] M. H. Naderi and J. Silva-Martinez, "Algorithmic-pipelined adc with a modified residue curve for better linearity," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2017, pp. 1446–1449.
- [53] S. Lee, A. P. Chandrakasan, and H. S. Lee, "A 12 b 5-to-50 ms/s 0.5-to-1 v voltage scalable zero-crossing based pipelined adc," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1603–1614, Jul. 2012.
- [54] J. Lagos, B. Hershberg, E. Martens, P. Wambacq, and J. Craninckx, "A single-channel, 600msps, 12bit, ringamp-based pipelined adc in 28nm cmos," in *2017 Symposium on VLSI Circuits*, Jun. 2017, pp. C96–C97.
- [55] M. Anderson, K. Norling, A. Dreyfert, and J. Yuan, "A reconfigurable pipelined adc in 0.18 μm cmos," in *Digest of Technical Papers. 2005 Symposium on VLSI Circuits, 2005.*, Jun. 2005, pp. 326–329.
- [56] J. L. McCreary and P. R. Gray, "All-mos charge redistribution analog-to-digital conversion techniques. i," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371–379, Dec. 1975.
- [57] X. Yue, "Determining the reliable minimum unit capacitance for the DAC capacitor array of SAR ADCs," *Microelectronics Journal*, ELSEVIER, vol. 44, no. 6, pp. 473–478, 2013.
- [58] J. H. Mueller, S. Strache, L. Busch, R. Wunderlich, and S. Heinen, "The Impact of Noise and Mismatch on SAR ADCs and a Calibratable Capacitance Array Based Approach for High Resolutions," *International Journal of Electronics and Telecommunications*, vol. 59, no. 2, pp. 161–167, 2013.
- [59] N. Collins, A. Tamez, L. Jie, J. Pernillo, and M. P. Flynn, "A Mismatch-Immune 12-bit SAR ADC With Completely Reconfigurable Capacitor DAC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 7747, no. 1, pp. 1–1, 2017.
- [60] J.-S. Lee and I.-C. Park, "Capacitor array structure and switch control for energy-efficient sar analog-to-digital converters," in *2008 IEEE International Symposium on Circuits and Systems*, May 2008, pp. 236–239.

Bibliography

- [61] W. Yu, J. Lin, and G. C. Temes, "Two-step junction-splitting sar analog-to-digital converter," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, May 2010, pp. 1448–1451.
- [62] D. Zhang and A. Alvandpour, "Analysis and calibration of nonbinary-weighted capacitive dac for high-resolution sar adcs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 9, pp. 666–670, Sep. 2014.
- [63] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a sar converter with capacitive dac," in *2005 IEEE International Symposium on Circuits and Systems*, May 2005, 184–187 Vol. 1.
- [64] Z. Zhu, Y. Xiao, and X. Song, "Vcm-based monotonic capacitor switching scheme for sar adc," *Electronics Letters*, vol. 49, no. 5, pp. 327–329, Feb. 2013.
- [65] L. Xie, G. Wen, J. Liu, and Y. Wang, "Energy-efficient hybrid capacitor switching scheme for sar adc," *Electronics Letters*, vol. 50, no. 1, pp. 22–23, Jan. 2014.
- [66] D. Li, Q. Meng, and F. Li, "Improved dual-capacitive arrays dac architecture for sar adc," *Electronics Letters*, vol. 52, no. 12, pp. 1013–1015, 2016.
- [67] F. M. Yaul and A. P. Chandrakasan, "11.3 a 10b 0.6nw sar adc with data-dependent energy savings using lsb-first successive approximation," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 198–199.
- [68] S. Brenna, A. Bonfanti, A. Abba, F. Caponio, and A. L. Lacaita, "Analysis and optimization of a sar adc with attenuation capacitor," in *2014 37th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, May 2014, pp. 68–73.
- [69] R. Sekimoto, A. Shikata, T. Kuroda, and H. Ishikuro, "A 40nm 50s/s–8ms/s ultra low voltage sar adc with timing optimized asynchronous clock generator," in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, Sep. 2011, pp. 471–474.
- [70] Z. Zhu, Z. Qiu, M. Liu, and R. Ding, "A 6-to-10-bit 0.5 v-to-0.9 v reconfigurable 2 ms/s power scalable sar adc in 0.18 μ m cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 689–696, Mar. 2015.
- [71] Y. Shen, Z. Zhu, S. Liu, and Y. Yang, "A reconfigurable 10-to-12-b 80-to-20-ms/s bandwidth scalable sar adc," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 51–60, Jan. 2018.
- [72] Y. J. Chen, J. H. Tsai, M. H. Shen, and P. C. Huang, "A 1-v 8-bit 100ks/s-to-4ms/s asynchronous sar adc with 46fj/conv.-step," in *Proceedings of 2011 International Symposium on VLSI Design, Automation and Test*, Apr. 2011, pp. 1–4.

Bibliography

- [73] S. S. Wong, U. F. Chio, Y. Zhu, S. W. Sin, S. P. U, and R. P. Martins, “A 2.3 mw 10-bit 170 ms/s two-step binary-search assisted time-interleaved sar adc,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1783–1794, Aug. 2013.
- [74] P. C. Tung, D. T. Fan, and T. H. Tsai, “A 10-bit asynchronous sar adc with scalable conversion time in $0.18 \mu\text{m}$ cmos,” in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1454–1457.
- [75] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Brändli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, “A 3.1 mw 8b 1.2 gs/s single-channel asynchronous sar adc with alternate comparators for enhanced speed in 32 nm digital soi cmos,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3049–3058, Dec. 2013.
- [76] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti, “A 10-bit 100-ms/s reference-free sar adc in 90 nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.
- [77] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, “A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.
- [78] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, “A $26 \mu\text{w}$ 8 bit 10 ms/s asynchronous sar adc for low energy radios,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.
- [79] Y. Varshni, “Temperature dependence of the energy gap in semiconductors,” *Physica*, vol. 34, no. 1, pp. 149–154, 1967. arXiv: arXiv:1011.1669v3.
- [80] P. B. Allen and V. Heine, “Theory of the temperature dependence of electronic band structures,” *Journal of Physics C: Solid State Physics*, vol. 9, no. 12, p. 2305, 1976.
- [81] A. Manoogian and A. Leclerc, “Determination of the dilation and vibrational contributions to the energy band gaps in germanium and silicon,” *physica status solidi (b)*, vol. 92, no. 1, K23–K27, 1979.
- [82] K. P. O’Donnell and X. Chen, “Temperature dependence of semiconductor band gaps,” *Applied Physics Letters*, vol. 58, no. 25, pp. 2924–2926, 1991.
- [83] K. Lee, J.-S. Choi, S.-P. Sim, and C.-K. Kim, “Physical understanding of low-field carrier mobility in silicon mosfet inversion layer,” *IEEE Transactions on Electron Devices*, vol. 38, no. 8, pp. 1905–1912, Aug. 1991.
- [84] D. S. Jeon and D. E. Burk, “Mosfet electron inversion layer mobilities-a physically based semi-empirical model for a wide temperature range,” *IEEE Transactions on Electron Devices*, vol. 36, no. 8, pp. 1456–1463, Aug. 1989.

Bibliography

- [85] F. F. Fang and A. B. Fowler, "Hot electron effects and saturation velocities in silicon inversion layers," *Journal of Applied Physics*, vol. 41, no. 4, pp. 1825–1831, 1970. eprint: <https://doi.org/10.1063/1.1659111>.
- [86] S. M. Sze, *Physics of Semiconductor Devices*, 2nd. New York: Jonh Wiley 'Sons, 1981, p. 868.
- [87] S. M. Sze and K. K. Ng, *Semiconductor Devices: Physics and Technology*. 2006, p. 568.
- [88] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876–884, 2001.
- [89] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Body bias voltage computations for process and temperature compensation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, no. 3, pp. 249–262, Mar. 2008.
- [90] Y. Cheng, M.-C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. K. Ko, and C. Hu, "A physical and scalable i-v model in bsim3v3 for analog/digital circuit simulation," *IEEE Transactions on Electron Devices*, vol. 44, no. 2, pp. 277–287, Feb. 1997.
- [91] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical mos transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, Jul. 1995.
- [92] K. Joardar, K. K. Gullapalli, C. C. McAndrew, M. E. Burnham, and A. Wild, "An improved mosfet model for circuit simulation," *IEEE Transactions on Electron Devices*, vol. 45, no. 1, pp. 134–148, Jan. 1998.
- [93] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/id based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996.
- [94] J. Ou and P. M. Ferreira, "A gm/ID-Based Noise Optimization for CMOS Folded-Cascode," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 783–787, Oct. 2014.
- [95] J. Ou and P. M. Ferreira, "Design considerations of CMOS active inductor for low power applications," *Analog Integr. Circ. Sig. Process*, vol. 94, no. 3, pp. 347–356, Mar. 2018.
- [96] J. Ou and P. M. Ferreira, "Implications of Small Geometry Effects on gm/ID Based Design Methodology for Analog Circuits," *IEEE Trans. Circuits and Syst. II: Express Briefs*, vol. pp, no. pp, pp. 1–5, Jun. 2018.
- [97] J. Ou and P. M. Ferreira, "A CMOS Envelope Detector for Low Power Wireless Receiver Applications," in *IEEE New Circuits Syst. Conf.*, Montréal, Canada, Jun. 2018, pp. 44–47.
- [98] ——, "Design Considerations of a CMOS Envelope Detector for Low Power Wireless Receiver Applications," in *IEEE New Circuits Syst. Conf.*, Strasbourg, France, Jun. 2017, pp. 233–236.

Bibliography

- [99] C. P. C. Park, J. John, K. Klein, J. Teplik, J. Caravella, J. Whitfield, K. Papworth, and S. C. S. Cheng, "Reversal of temperature dependence of integrated circuits operating\at very low voltages," *Proceedings of International Electron Devices Meeting*, pp. 71–74, 1995.
- [100] F. Shoucair, "Design Consideration in High Temperature Analog CMOS Integrated Circuits," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 9, no. 3, pp. 242–251, 1986.
- [101] S. Chen and J. S. Yuan, "Adaptive gate bias for power amplifier temperature compensation," *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 3, pp. 442–449, Sep. 2011.
- [102] D. Gomez, M. Sroka, and J. L. G. Jimenez, "Process and temperature compensation for rf low-noise amplifiers and mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1204–1211, Jun. 2010.
- [103] D. Sira and T. Larsen, "Process, voltage and temperature compensation technique for cascode modulated pas," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 9, pp. 2511–2520, Sep. 2013.
- [104] D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, and D. P. Foty, "A cad methodology for optimizing transistor current and sizing in analog cmos design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 2, pp. 225–237, Feb. 2003.
- [105] A. Rahman, L. Caley, S. Roy, N. Kuhns, A. Mantooth, J. Di, A. M. Francis, and J. Holmes, "High temperature data converters in silicon carbide cmos," *IEEE Transactions on Electron Devices*, vol. 64, no. 4, pp. 1426–1432, Apr. 2017.
- [106] A. Fonseca, R. El Khattabi, W. Afshari, F. Barúqui, C. Soares, and P. Ferreira, "A Temperature-Aware Analysis of SAR ADCs for Smart Vehicle Applications," *J. Integr. Circuits Syst.*, vol. pp, no. pp, pp. 1–11, 2018.
- [107] C. Davis and I. Finvers, "A 14-bit high-temperature sigma; delta; modulator in standard cmos," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 976–986, Jun. 2003.
- [108] M. N. Ericson, M. Bobrek, A. Bobrek, C. L. Britton, J. M. Rochelle, B. J. Blalock, and R. L. Schultz, "A high resolution, extended temperature sigma delta adc in 3.3 v 0.5 mu;m sos-cmos," in *2004 IEEE Aerospace Conference Proceedings (IEEE Cat. No.04TH8720)*, vol. 4, Mar. 2004, 2608–2617 Vol.4.
- [109] Y. Yao, D. Ma, and F. Dai, "A 12-bit interleaved opamp-sharing pipeline adc for extreme environment applications," in *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology*, Nov. 2010, pp. 394–396.
- [110] K. Souri, Y. Chae, Y. Ponomarev, and K. A. A. Makinwa, "A precision dtmost-based temperature sensor," in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, Sep. 2011, pp. 279–282.

Bibliography

- [111] S. H. Lewis and P. R. Gray, "A pipelined 5-msample/s 9-bit analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, pp. 954–961, Dec. 1987.
- [112] M. Afghahi, "A robust single phase clocking for low power, high-speed vlsi applications," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 247–254, Feb. 1996.
- [113] K.-H. Cheng and Y.-H. Lin, "A dual-pulse-clock double edge triggered flip-flop for low voltage and high speed application," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 5, May 2003, V-425-V-428 vol.5.
- [114] S. L. Murotiya and A. Gupta, "Performance evaluation of cmtfet based dynamic dual edge triggered register," in *2013 International Conference on Advanced Electronic Systems (ICAES)*, Sep. 2013, pp. 180–183.
- [115] A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true-single-phase clock dual-edge-triggered flip-flop," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 1850–1853.
- [116] R. Hildebrandt. (2007). The pseudo dual-edge d-flipflop, [Online]. Available: http://www.ralf-hildebrandt.de/publication/pdf_dff/pde_dff.pdf (visited on 08/29/2018).
- [117] L. Sumanen, M. Waltari, and K. Halonen, "A mismatch insensitive cmos dynamic comparator for pipeline a/d converters," in *ICECS 2000. 7th IEEE International Conference on Electronics, Circuits and Systems (Cat. No.00EX445)*, vol. 1, 2000, 32–35 vol.1.
- [118] L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, "Cmos dynamic comparators for pipeline a/d converters," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, vol. 5, 2002, V-157-V-160 vol.5.
- [119] A. M. Abo and P. R. Gray, "A 1.5-v, 10-bit, 14.3-ms/s cmos pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
- [120] M. Yamashina, M. Mizuno, K. Furuta, H. Igura, M. Nomura, H. Abiko, K. Okabe, A. Ono, and H. Yamada, "A low-supply voltage ghz mos integrated circuit for mobile computing systems," in *Proceedings of 1994 IEEE Symposium on Low Power Electronics*, Oct. 1994, pp. 80–81.
- [121] M. Usama and T. Kwasniewski, "Design and comparison of cmos current mode logic latches," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, vol. 4, May 2004, IV-353-6 Vol.4.
- [122] X. Zhang, Y. Wang, S. Jia, G. Zhang, and X. Zhang, "A novel cml latch for ultra high speed applications," in *2014 IEEE International Conference on Electron Devices and Solid-State Circuits*, Jun. 2014, pp. 1–2.
- [123] A. Hajimiri and R. Heald, "Design issues in cross-coupled inverter sense amplifier," in *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on*, vol. 2, May 1998, 149–152 vol.2.

Bibliography

- [124] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.-T. Leung, "Improved sense-amplifier-based flip-flop: Design and measurements," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, Jun. 2000.
- [125] A. Yukawa, "A cmos 8-bit high-speed a/d converter ic," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 3, pp. 775–779, Jun. 1985.
- [126] A. Nikoozadeh and B. Murmann, "An analysis of latch comparator offset due to load capacitor mismatch," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.
- [127] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, Apr. 1993.
- [128] J. Montanaro, R. T. Witek, K. Anne, A. J. Black, E. M. Cooper, D. W. Dobberpuhl, P. M. Donahue, J. Eno, W. Hoeppner, D. Kruckemyer, T. H. Lee, P. C. M. Lin, L. Madden, D. Murray, M. H. Pearce, S. Santhanam, K. J. Snyder, R. Stehpany, and S. C. Thierauf, "A 160-mhz, 32-b, 0.5-w cmos risc microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.
- [129] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. V. der Plas, "A 2.2mw 5b 1.75gs/s folding flash adc in 90nm digital cmos," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2008, pp. 252–611.
- [130] S. W. M. Chen and R. W. Brodersen, "A 6-bit 600-ms/s 5.3-mw asynchronous adc in 0.13-*muhboxm* cmos," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.
- [131] K. Bult and A. Buchwald, "An embedded 240-mw 10-b 50-ms/s cmos adc in 1-*mm*²," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1887–1895, Dec. 1997.
- [132] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb. 2007, pp. 314–605.
- [133] V. Savani and N. M. Devashrayee, "Analysis amp; characterization of dual tail current based dynamic latch comparator with modified sr latch using 90nm technology," in *2015 19th International Symposium on VLSI Design and Test*, Jun. 2015, pp. 1–2.
- [134] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution adc consuming 1.9 *muw* at 1 ms/s," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.
- [135] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed adcs," in *2008 IEEE Asian Solid-State Circuits Conference*, Nov. 2008, pp. 269–272.

Bibliography

- [136] C. H. Chan, Y. Zhu, U. F. Chio, S. W. Sin, U. Seng-Pan, and R. P. Martins, "A reconfigurable low-noise dynamic comparator with offset calibration in 90nm cmos," in *IEEE Asian Solid-State Circuits Conference 2011*, Nov. 2011, pp. 233–236.
- [137] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343–352, Feb. 2014.
- [138] B. Nauta, "A cmos transconductance-c filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.
- [139] T. Chen, S. Rodriguez, J. Akerman, and A. Rusu, "An inductorless wideband balun-lna for spin torque oscillator-based field sensing," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2014, pp. 36–39.
- [140] K. Bult and G. J. G. M. Geelen, "A fast-settling cmos op amp for sc circuits with 90-db dc gain," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990.
- [141] R. Selby, T. Kern, W. Wilson, and T. Chen, "A $0.18\text{ }\mu\text{m}$ cmos switched-capacitor amplifier using current-starving inverter based op-amp for low-power biosensor applications," in *2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS)*, Feb. 2013, pp. 1–4.
- [142] A. Ismail and I. Mostafa, "A process-tolerant, low-voltage, inverter-based ota for continuous-time $\Delta\Sigma$ adc," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 9, pp. 2911–2917, Sep. 2016.
- [143] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Comparator-based switched-capacitor circuits for scaled cmos technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, Dec. 2006.
- [144] G. Olivera-Romero and J. Silva-Martinez, "A folded-cascode ota based on complementary differential-pairs for hf applications," in *Proceedings of the Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications (Cat. No.99EX303)*, 1999, pp. 57–60.
- [145] J. Adut and J. Silva-Martinez, "Cascode transconductance amplifiers for hf switched-capacitor applications," in *Circuits and Systems, 2003. ISCAS 03. Proceedings of the 2003 International Symposium on*, vol. 1, May 2003, I-365-I-368 vol.1.
- [146] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7v mosfet-only switched-opamp $\Delta\Sigma$ modulator," in *2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315)*, vol. 2, Feb. 2002, pp. 246–492.

Bibliography

- [147] G.-c. Ahn, D.-y. Chang, M. Brown, N. Ozaki, H. Youra, K. Yamamura, K. Hamashita, K. Takasuka, G. C. Temes, and U.-K. Moon, "A 0.6v 82db $\Delta\Sigma$ audio adc using switched-rc integrators," in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, Feb. 2005, 166–591 Vol. 1.
- [148] P. J. Quinn, K. van Hartingsveldt, and A. H. M. van Roermund, "A 10.7-mhz cmos sc radio if filter using orthogonal hardware modulation," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1865–1876, Dec. 2000.
- [149] Y. Chiu, P. R. Gray, and B. Nikolic, "A 14-b 12-ms/s cmos pipeline adc with over 100-db sfdr," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2139–2151, Dec. 2004.
- [150] K. Bult and G. J. G. M. Geelen, "The CMOS gain-boosting technique," *Analog Integrated Circuits and Signal Processing*, vol. 1, no. 2, pp. 119–135, Oct. 1991.
- [151] Y. Miyahara, M. Sano, K. Koyama, T. Suzuki, K. Hamashita, and B. S. Song, "A 14b 60 ms/s pipelined adc adaptively cancelling opamp gain and nonlinearity," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 416–425, Feb. 2014.
- [152] B. K. Thandri and J. Silva-Martinez, "A 92-mhz 13-bit if digitizer using optimized sc integrators in 0.35- μ m cmos technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 5, pp. 412–416, May 2006.
- [153] S. Zhang, Z. Zhu, H. Zhang, Z. Xiong, and Q. Li, "A 90-db dc gain high-speed nested gain-boosted folded-cascode opamp," in *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jun. 2015, pp. 357–360.
- [154] Y. Liu, E. Bonizzoni, and F. Maloberti, "A single op-amp 0+2 sigma-delta modulator," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2029–2032.
- [155] J. Sun and J. Wu, "A high speed pipeline adc with 78-db sfdr in 0.18 um bicmos," in *2016 International Symposium on Integrated Circuits (ISIC)*, Dec. 2016, pp. 1–4.
- [156] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.
- [157] B. Razavi, "The strongarm latch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, Spring 2015.
- [158] A. Khorami and M. Sharifkhani, "A high-speed method of dynamic comparators for sar analog to digital converters," in *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Oct. 2016, pp. 1–4.
- [159] A. Abidi and H. Xu, "Understanding the regenerative comparator circuit," in *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*, Sep. 2014, pp. 1–8.

Bibliography

- [160] A. V. Fonseca, R. E. Khattabi, W. A. Afshari, F. A. P. Barúqui, C. F. T. Soares, and P. M. Ferreira, “A temperature-aware analysis of latched comparators for smart vehicle applications,” in *2017 30th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Aug. 2017, pp. 1–6.
- [161] B. D. Sahoo and B. Razavi, “A 10-b 1-ghz 33-mw cmos adc,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1442–1452, Jun. 2013.
- [162] A. Bafandeh and M. Yavari, “Digital calibration of amplifier finite dc gain and gain bandwidth in mash *sigmadelta* modulators,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 4, pp. 321–325, Apr. 2016.
- [163] C. Y. Chu and Y. J. Wang, “A pvt-independent constant- *gm* bias technique based on analog computation,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 10, pp. 768–772, Oct. 2014.
- [164] R. E. Vallee and E. I. El-Masry, “A very high-frequency cmos complementary folded cascode amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 29, no. 2, pp. 130–133, Feb. 1994.
- [165] B. Lipka, U. Kleine, J. C. Scheytt, and K. Schmalz, “Design of a complementary folded-cascode operational amplifier,” in *2009 IEEE International SOC Conference (SOCC)*, Sep. 2009, pp. 111–114.
- [166] M. K. Hati and T. K. Bhattacharyya, “A power efficient and constant-gm 1.8 v cmos operational transconductance amplifier with rail-to-rail input and output ranges for charge pump in phase-locked loop,” in *2012 International Conference on Devices, Circuits and Systems (ICDCS)*, Mar. 2012, pp. 38–43.
- [167] D. B. Ribner and M. A. Copeland, “Design techniques for cascaded cmos op amps with improved psrr and common-mode input range,” *IEEE Journal of Solid-State Circuits*, vol. 19, no. 6, pp. 919–925, Dec. 1984.
- [168] J. M. Carrillo, J. L. Ausin, and J. F. Duque-Carrillo, “Cmos continuous-time cmfb circuit with improved linearity,” in *2007 18th European Conference on Circuit Theory and Design*, Aug. 2007, pp. 40–43.
- [169] J. M. Carrillo, G. Torelli, M. A. Dominguez, R. Perez-Aloe, J. M. Valverde, and J. F. Duque-Carrillo, “A family of low-voltage bulk-driven cmos continuous-time cmfb circuits,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 11, pp. 863–867, Nov. 2010.
- [170] F. Centurelli, P. Monsurrò, G. Parisi, P. Tommasino, and A. Trifiletti, “A fully-differential class-ab ota with cmrr improved by local feedback,” in *2017 European Conference on Circuit Theory and Design (ECCTD)*, Sep. 2017, pp. 1–4.
- [171] O. Choksi and L. R. Carley, “Analysis of switched-capacitor common-mode feedback circuit,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 12, pp. 906–917, Dec. 2003.

Bibliography

- [172] M. Conti, P. Crippa, S. Orcioni, and C. Turchetti, “Layout-based statistical modeling for the prediction of the matching properties of mos transistors,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 5, pp. 680–685, May 2002.
- [173] T. I. Incorporated, “Active fail-safe in ti’s lvds receivers,” in, 2005.
- [174] B. Goll, M. S. Durante, and H. Zimmermann, “A measurement technique to obtain the delay time of a comparator in 120nm cmos,” in *Proceedings of the International Conference Mixed Design of Integrated Circuits and System, 2006. MIXDES 2006.*, Jun. 2006, pp. 563–568.
- [175] J. P. Jansson, A. Mantyniemi, and J. Kostamovaara, “A cmos time-to-digital converter with better than 10 ps single-shot precision,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, Jun. 2006.
- [176] A. Jain, A. Veggetti, D. Crippa, and P. Rolandi, “On-chip delay measurement circuit,” in *2012 17th IEEE European Test Symposium (ETS)*, May 2012, pp. 1–6.
- [177] R. Rashidzadeh, M. Ahmadi, and W. C. Miller, “An all-digital self-calibration method for a vernier-based time-to-digital converter,” *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 2, pp. 463–469, Feb. 2010.
- [178] S. Pei, A. A. Rabehb, and S. Jin, “On-chip ring oscillator based scheme for tsv delay measurement,” in *2017 IEEE 26th Asian Test Symposium (ATS)*, Nov. 2017, pp. 11–16.
- [179] P. Keränen and J. Kostamovaara, “A wide range, 4.2 ps(rms) precision cmos tdc with cyclic interpolators based on switched-frequency ring oscillators,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 12, pp. 2795–2805, Dec. 2015.
- [180] P. Verma, R. Halba, H. Patel, and M. S. Baghini, “On-chip delay measurement circuit for reliability characterization of sram,” in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Jul. 2016, pp. 331–336.
- [181] T. W. Matthews and P. L. Heedley, “A simulation method for accurately determining dc and dynamic offsets in comparators,” in *48th Midwest Symposium on Circuits and Systems, 2005.*, Aug. 2005, 1815–1818 Vol. 2.
- [182] A. J. Ginés, E. Peralías, G. Leger, and A. Rueda, “Closed-loop simulation method for evaluation of static offset in discrete-time comparators,” in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2014, pp. 538–541.
- [183] N. D. Hindman, Z. Wang, L. T. Clark, and D. R. Allee, “Experimentally measured input referred voltage offsets and kickback noise in rhbd analog comparator arrays,” *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2073–2079, Dec. 2007.
- [184] J. Lu and J. Holleman, “A low-power high-precision comparator with time-domain bulk-tuned offset cancellation,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1158–1167, May 2013.

Bibliography

- [185] T. Forzley and R. Mason, "A 14b threshold configurable dynamically latched comparator for sar adcs," in *2013 26th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Sep. 2013, pp. 1–5.
- [186] B. B. A. Arrants and R. Reeder, "Understanding high speed adc testing and evaluation, an-835," in, 2015.
- [187] T. I. Incorporated, "Dynamic tests for a/d converter performance, an-sbaa002a," in, 2011.
- [188] A. Device, "The data conversion handbook: Testing data converters," in, 2005.
- [189] "Ieee standard for terminology and test methods for analog-to-digital converters," *IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000)*, pp. 1–139, Jan. 2011.
- [190] T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Noise analysis for comparator-based circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 3, pp. 541–553, Mar. 2009.
- [191] P. M. Figueiredo, "Comparator metastability in the presence of noise," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1286–1299, May 2013.
- [192] P. Lautenschlager, P. B. Allen, and M. Cardona, "Temperature dependence of band gaps in si and ge," *Phys. Rev. B*, vol. 31, pp. 2163–2171, 4 Feb. 1985.
- [193] K. M., F. C., and L. W., "Temperature dependence of band gaps in si and ge in the quasi-ion model," *Annalen der Physik*, vol. 504, no. 1, pp. 34–38, eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/andp.19925040107>.

Titre: Analyse d'une nouvelle topologie fiable de convertisseur analogique-numérique pour l'environnement automobile

Mots clés:

Résumé: Alors que l'électronique automobile voit une forte expansion de la demande de capteurs intelligents avec une intégration de plus en plus poussée, les interfaces entre les capteurs et les contrôleurs ayant la puissance de calcul se trouvent être rapprochées des capteurs. De ce fait, les contraintes de stress mécanique et thermique deviennent des facteurs importants lors de la conception de convertisseur analogique-numérique ou de convertisseur numérique-analogique.

Dans le cadre de cette thèse, nous nous focalisons sur la conception d'un convertisseur analogique-numérique servant pour la conversion de signaux issus de capteurs de température, pression, courant, mais aussi pour une future application en tant que convertisseur dans une chaîne de conversion de télécommunication. Le challenge de la conception d'un tel ADC réside dans la forte contrainte de rapidité et de résolution sur une plage de températures importantes: de -40 °C à +175 °C.

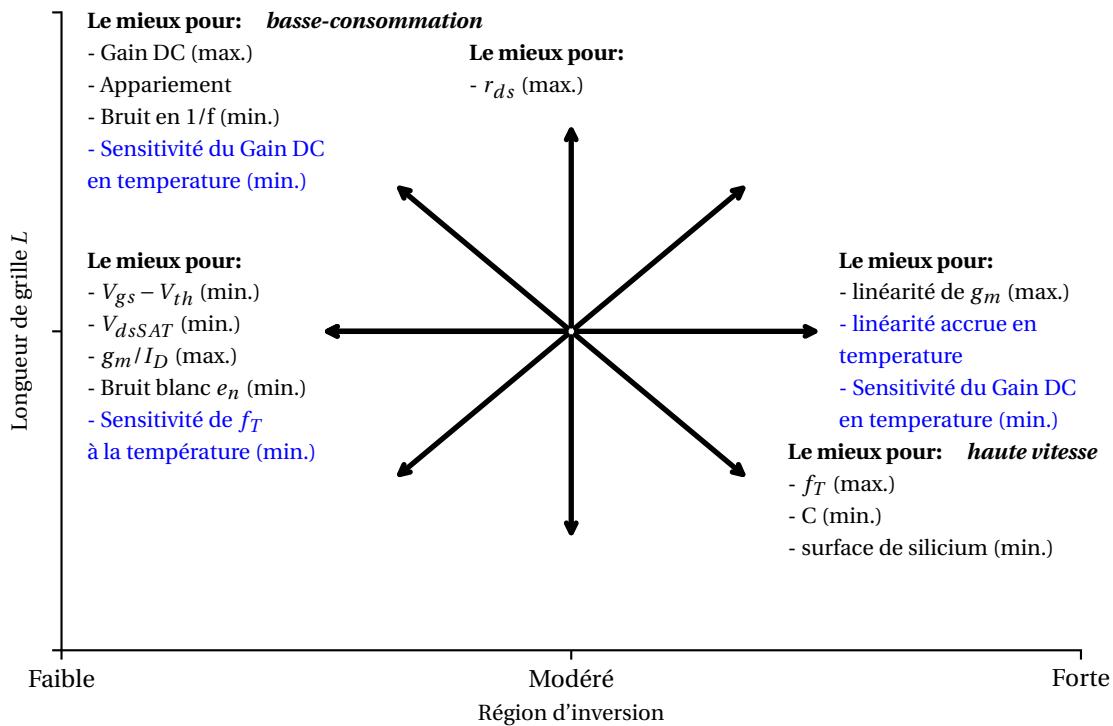
Ayant une contrainte économique d'autant importante, le coût réduit sera issu de la faible surface de silicium de ce composant allié à une économie d'échelle mondiale que le secteur automobile connaît. Comme exposé dans le tableau 6.2, la surface n'excédera pas 0.5 mm². Il est toutefois important de noter que le ratio entre la fréquence d'horloge maximale et la fréquence d'échantillonnage est seulement de 5. Ce ratio lié au sur-échantillonnage est très faible pour réaliser une conversion de 12-bit de résolution.

Critères	
Plage de Température	-40 °C – +175 °C
Tension d'alimentation	1.8 V ± 10 %
Plage de la tension différentielle d'entrée	± 1V
Surface	<0.5 mm ²
Fréquence d'échantillonnage	20 MSamples/s
Fréquence d'horloge maximum	100 MHz Duty-Cycle de l'horloge
40 – 60 %	
Latence	500 ns
Résolution	≥ 12-bit
DNL	<LSB/2
INL	<LSB/2 best-fit
Erreur d'Offset	<4 LSB
Erreur de Gain	<4 LSB
Erreur d'appariement entre deux ADCs	<4 LSB
Energie, $E_s = P/F_s$	0.75 nJ/échantillon

Suite à l'analyse architecturale de convertisseurs traditionnels et de leurs avancées dans le chapitre 2, les avantages et les sources source d'erreurs dans la partie analogique nous permettent de sélectionner

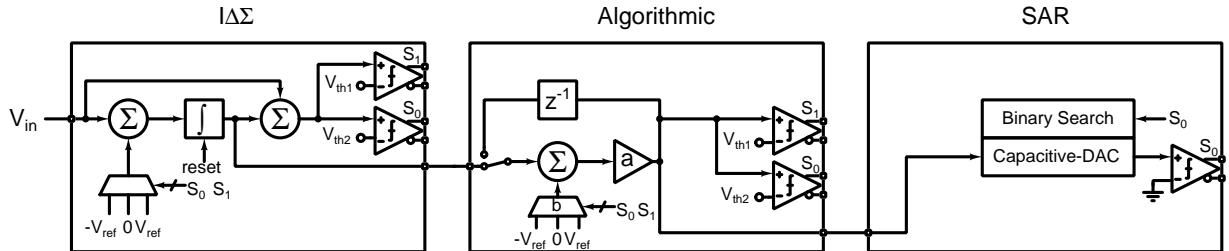
les architectures pour la haute température. Pour en nommer quelques un, on retrouve dans l'état de l'art des convertisseurs du type $\Sigma\Delta$, les SAR, et les convertisseurs Pipelined. Ceux-ci se trouvent être moins sensibles à la variation de performance de l'amplificateur s'il y a, et permettent avec une calibration en un seul point en température de compenser ces imperfections.

La section 2.2 discute les challenges que pose la conception analogique en température: que cela soit pour -40°C jusqu'à $+175^{\circ}\text{C}$. Les phénomènes physiques en jeu avec les températures sont analysés afin de déduire les compromis existant auquel nous devrons faire face. Base sur une méthodologie g_m/I_D , l'aperçu offert par cette analyse est directement exploitable pour la phase de conception analogique.

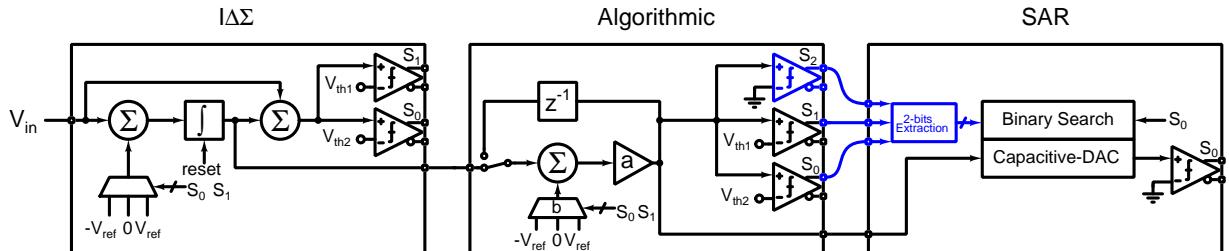


La contrainte de faible sur-échantillonnage limite l'utilisation à une architecture du type de pipelines pour atteindre une résolution d'au moins 12-bit. Ayant de nombreux étages, et amplificateurs, tant la consommation que la surface de silicium nécessaire peuvent être optimisées. La contribution de cette thèse réside dans le développement d'une nouvelle architecture reposant sur trois sous-convertisseurs d'une topologie différente. Ainsi, l'architecture globale proposée combine les forces de chaque sous-convertisseur pour réduire le bruit dans la bande de fréquences de conversion, diminuer la surface de silicium, réduire la consommation énergétique, et limiter la chute de résolution avec les variations de procédé de fabrication, de tension d'alimentation, et de température.

Commencant par un convertisseur $\Sigma\Delta$ -Incremental, le niveau de bruit se trouve être abaissé par un facteur de 8 au bout de 5 coups d'horloge. Et celui-ci nous permet d'extraire un équivalent de 3-bits sans souffrir des variations du procédé de fabrication si l'on considère une calibration numérique. Suivi par une algorithmique, le résidu de conversion subit 5 transformations consécutives afin d'extraire à nouveau 5-bits avec une contrainte de conception limiter à 9-bits. Ayant une technique permettant un appariement suffisant pour atteindre les 10-bits, la sensibilité de cet étage s'en trouve amoindrir pour correspondre aux dégradations de l'analogique due à la température et variation de dopage. Enfin, un SAR avec redistribution de charge permet d'extraire au maximum 4-bits supplémentaires avec une consommation énergétique réduite.



a) architecture originelle



b) amélioration

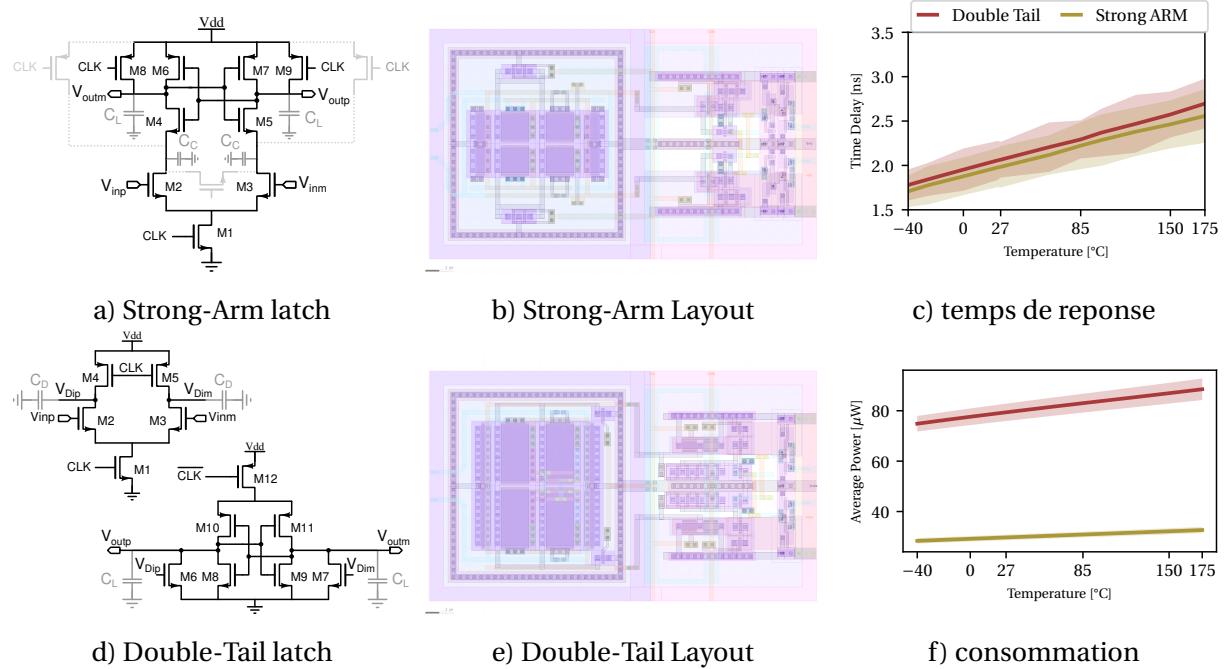
Fort de ceci, et des limitations en température qu'imposent les courants de fuites, des améliorations furent portées à l'architecture proposée. Dans un premier temps, un comparateur fut ajouté au sein de l'algorithmique. Ce dernier permet d'utiliser les derniers bits fournis aux derniers coups d'horloge d'un échantillon, comme les deux premiers bits issus de la conversion du SAR. La répartition des bits est donc 3.4.5.5 au lieu de 3-5-3.5. Le bit supplémentaire fut dans un second temps utilisé pour rendre la SAR moins sensible aux mauvaises décisions venant de l'algorithmique, et d'une génération des tensions de référence par suffisamment précise. En plus de cela, en changeant le radix, la sensibilité due aux courants de fuites est aussi diminuée puisqu'une redondance est introduite et que le pas du LSB est plus grand. Enfin, il fut envisager d'améliorer encore la résolution pour un sur-échantillonnage de 6 coups d'horloge au lieu de 5. L'utilisation d'un coup d'horloge supplémentaire permet d'atteindre la résolution de 13.9-bits.

En plus de l'optimisation de l'architecture, le Chapitre 3 présent les considérations prises lors du dimensionnement et lors du layout en vue d'une répétabilité accrue pour une moindre surface.

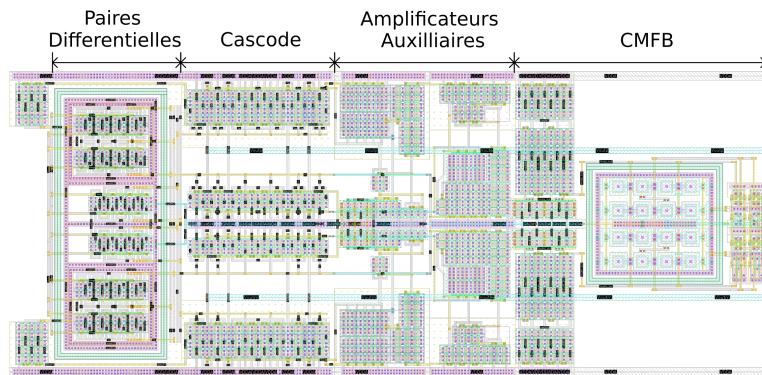
La fiabilité ne fut pas laisse en reste même si le dernier étage emploie un design pseudo asynchrone afin de relâcher la contrainte de temps sur la prise de décision du comparateur dépendant de la température. Suivant une approche top-down, l'architecture fut d'abord validée par une simulation MATLAB puis Spice Haut niveau. Cette dernière nous a permis d'estimer plus précisément les spécifications des sous-blocs analogiques principaux en utilisant des modèles Verilog-AMS. Puis ceux-ci furent remplacés par leur implémentation au niveau transistor, et par une netlist spice après extraction des parasites due au layout. Les performances statiques telles que la précision, le DNL, l'INL, ... sont le résultat d'un post-traitement MATLAB des simulations MATLAB et Spice.

Parmi l'ensemble des implémentations possibles décrit dans le début du chapitre 4, les sous-blocs analogiques principaux choisis sont le Strong ARM latch, le Double-Tail latch, et le Gain-Boosted Complementary Folded Cascode. Dans l'état de l'art, les deux latches choisies et leurs dérivés sont les plus choisies. Bien que les équations de conception sont connues, leur sensibilité à la température l'est beaucoup moins. Les deux comparateurs sont donc analysés et comparés afin de choisir le plus approprié pour chaque étage du convertisseur pour une variation de 6σ des paramètres du procédé de

fabrication. Issu de ce travail un nouveau modèle analytique pour le délai du Double-Tail fut présentée lors de l'ECCTD qui s'est tenu en 2017.

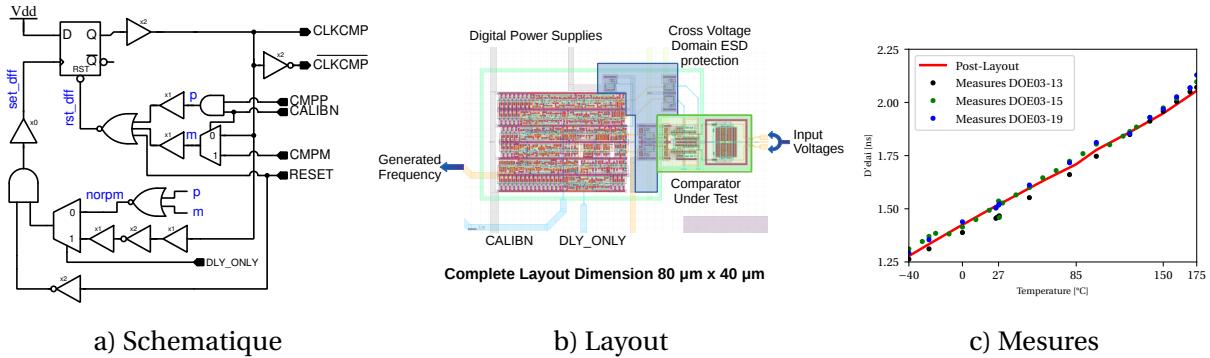


Quant à l'amplificateur, si l'on considère un processus en 180 nm, la plupart des publications ont été publiées entre 2001 et 2008. Sur cette période, le Folded-Cascode, les OTA à deux étages, et ceux basées sur du gain-Boosting sa légion avec une préférence pour un Folded Cascode suivit par un étage en source-follower pour améliorer l'excursion de sortie. Pour des raisons de rapidité et de stabilité, le gain-boosting d'un OTA de classe AB fut privilégié. Les choix de conception et les contraintes liées au layout représenté à la Figure 6.2 sont aussi discutés dans ce chapitre. En matière de bruit, l'OTA génère un bruit maximum estimé de $198 \mu\text{V}_{rms}$ correspondant à 82% du LSB d'un 12-bit sur l'excursion du résidu du premier étage. La consommation en courant n'excédant pas 1.8 mA, la consommation moyenne totale de l'analogique est estimée à 7 mW avec un maximum admis à -40 °C dans le corner FF de 14 mW.

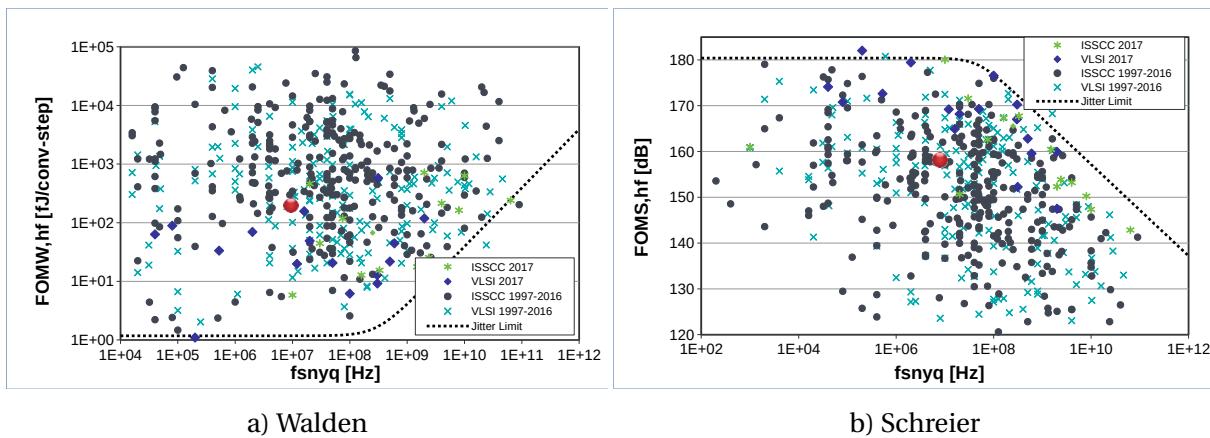


Étant donné la polyvalence souhaitée du convertisseur et en vue de sa réutilisation, chaque élément de sa composition est validé expérimentalement. Ainsi, trois puces de testés différents furent conçues et présentes dans le chapitre 5. La première permet de valider le délai, l'offset, le bruit, l'hystérésis des comparateurs. Au cours de sa conception, un circuit de mesure du délai des comparateurs synchrones fut présenté lors de l'ECCTD 2017. Les résultats en température obtenus pour ce circuit s'accordent avec

le modèle du délai pour et démontrent de bonne performance en raison de sa taille en comparaison des circuits existant tel que dépeint à la Figure 6.2. La seconde valide le fonctionnement pseudo asynchrone et les performances statiques du SAR en température. Suite aux améliorations de l'architecture, la testabilité du dernier étage se complexifie. Les procédures de testés s'en trouvent donc modifiées et sont présentées. Le SAR démontre en température une importante stabilité de la pondération de chaque bit. Ce résultat permet donc de réutiliser cet étage pour la calibration des précédents, comme de réduire le temps de test de cet étage. Enfin, la dernière puce permet de valider chaque étage indépendamment et le convertisseur dans sa globalité. Cette dernière n'est pas encore envoyée en fonderie, et par conséquent seulement la conception et les principes des tests à effectuer sont discutés.



Au final, les résultats préliminaires sont encourageants sur les capacités de l'architecture hybride proposée en vue d'une haute résolution à une vitesse d'échantillonnage modérée. Réalisée dans une technique SOI CMOS 180 nm, la sensibilité vis-à-vis de la température est moindre en comparaison de publication de convertisseur analogique-numérique en haute température subissant une chute de 2-bits sur la même plage de températures [108]. La résolution espérée serait de 11,2 bits et 13,2 bits pour respectivement un sur-échantillonnage de 5 et 6 coups d'horloge. Cela correspond à un facteur de mérite de Walden valant 124 ff/conversion et un facteur de mérite de Schreier valant 159. Ceci place la nouvelle architecture réalisée dans la frange moyenne des convertisseurs analogique-numérique selon le critère de Walden, et le critère de Schreier tel que représente dans la Figure 6.2.



Afin d'améliorer cela, l'OTA pourrait être remplacé par une architecture moins gourmande, tel qu'une source de courant pilotée par un comparateur en temps continue, ou un ring amplifier. En plus de cela, une calibration numérique permettrait de relâcher la contrainte de timing et de toujours atteindre le nombre de bits effectif.

Title: A New ADC topology for reliable conversion in the automotive environment

Keywords:

Abstract: In the automotive industry, the trend being to develop smart sensors and actuators, the on-board electronic has been ever more an artful work to combine analog electronics and the digital one. While many monitoring and control systems play a crucial role as well for the safety as for the comfort of passengers, small components, likeADCs, are mandatory as a building block or as an essential functionality integrated into smart actuators. To that extent, a low-cost, fast and accurate analog to digital converter operating in those harsh conditions is a good ally for equipment manufacturers. To decrease the cost, the area is of primary concern. Considering re-use of the ADC as an IP-bloc, the area has been limited to less than half a square millimeter for an low-oversampling ratio of 5 to output a 12-bit code at a sample rate of 20 MSamples/s, over a wide temperature range from -40°C to 175°C.

This work focuses on the design of high-precision, high-speed and energy efficient ADC under the harsh environment the automotive one represents. Our main contribution relies on the development of an new hybrid topology proposal using 3 stages to cope with such constraints based on a top-down approach: A first counting stage inherently linear, an algorithmic stage allowing to increase rapidly the precision, and a SAR stage, ideal in terms of area and consumption, for a low number of bits.

Based on a 40 years literature review, a new topology proposal has been validated by checking its static metric of non-linearity (DNL, INL) at different level of modelisation. Starting by a MATLAB implementation without analog limitations, we refined step by step the model till we reach a transistor level of the ADC. Thence, Verilog-A model allows us to fix the minimum requirements of the key analog building blocks, to wit comparators and OTA. The latter has been analysed in order to limit the settling error sensitivity to the temperature. Laid-out, parasitic extracted simulation results of these considering PVT variations, they replace then previous high-level model to give final performances. Meanwhile, two well-known comparator architectures have been assessed as IP blocs inside a first test chip. To perform the offset extraction, both a conventional and a feedback loop have been inspected. To assess, the delay a new asynchronous circuit has been proposed. A second chip tests the sensitivity of the SAR to validate both the pseudo-asynchronous digital scheme, and a Double-Tail comparator in real operating conditions.

For comparators, the new differential measurement circuit of the delay demonstrate an accuracy of 60 ps in the worst case, over a large temperature range for the smallest chip area known with respect to the technology node size. The temperature variation of the delay being temperature dependant, the choice of a Strong-ARM or a Double-Tail hinge on the noise, power, supply voltage, and kickback specification. For standard power supply voltage, the Strong-ARM latch targets low-power systems application with a high tolerance for differential kickback. To the contrary, a Double-Tail latch allows lower power supply voltage range, with low-differential kickback. Otherwise, the Double-Tail exhibit a higher noise due to the integration in its first stage. Tested from -40°C to 200°C, the last stage of the proposed ADC topology does not need calibration up to 180°C. The encouraging results on this stage allows the re-use of the SAR to calibrate the previous stages. And considering the ADC, we estimate a possible resolution of 11.2-bits in 5 clock cycles per sample with an extension to 13.3-bits in 6 clock cycles with an estimated area of 0.067 mm².

The ADC test chip not being fabricated yet, a first step is the characterization of the ADC. From the results of the planned measurement session, the main goal is to push the architecture at higher sampling rates to then leverage the digital processing to enhance the sampling rate without changing the analog.